Optimum Performance Controls of Multiport Converter for Transport Electrification Applications

by

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Contents

List of Acronyms

2D	2 Dimension
3D	3 Dimension
AC	Alternating Current
ACB	Active Current Balancing
AGD	Active Gate Driver
Al	Aluminum Electrolyte
BOPP	Biaxial Oriented PolyPropylene
CAGR	Compounded Annual Growth Rate
CFFC	Compensating Fringing Field Concept
COP26	Climate Change Conference 2026
CSR	Current Source Rectifier
D.O.E	Department Of Energy
DAB	Dual Active Bridge
DBC	Direct Bonded Copper
DC	Direct Current
dcA	Isolated Buck Converter
dcB	Interleaved Buck/Boost Converter
DCDC	DC to DC
DCM	Discontinuous Conduction Mode
DPT	Double-Pulse Test

DS	Drain-Source
DSC	Double Sided Cooling
EMC	Electro Magnetic Compliance
EMI	Electro Magnetic Interference
ES	Energy Storage
ESR	Equivalent Series Resistance
EV	Electric Vehicle
FE	Finite Element
FEA	Finite Element Analysis
FFT	Fast Fourier Transform
FW	Field Weakening
GHG	Greenhouse gas
HV	High Voltage
ICE	Internal Combustion Engine
inv	Inverter
IPMSM	Interior Permanent Magnet Machine
KPI	Key Performance Index
LPTN	Lumped Parameter Network
MLCC	Multi-Layer Ceramic Capacitor
MOOP	Multiple Objective Optimisation Problem
MPC	Model Predictive Control
MPPF	Metalized Polymer Films
MTPA	Maximum Torque Per Ampere
NBfL	New Bus for London
NEV	New Energy Vehicle

NVH	Noise Vibration Harshness
PCB	Printed Circuit Board
PD	Phase Displacement
PI	Proportional Integral
PMSM	Permanent Magnet Synchronous Machine
PS-PWM	Phase Shifted Pulse Width Modulation
PWM	Pulse Width Modulation
RC	Resistor-Capacitor
RMS	Root Mean Square
RPM	Revolutions Per Minute
Si	Silicon
SiC	Silicon Carbide
SW	Switching
TAB	Tripple Active Bridge
TH	Targeted Harmonic
THD	Total Harmonic Distortion
UK	United Kingdom
US	United States of America
VJT	Virtual Junction Temperature
VSI	Voltage Source Inverter

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Abstract

Environmental concerns and energy efficiency have been driving the transportation innovation in the past decades. In this framework, hybrid city transport has been receiving the attention of the industry. The challenges for this application, are the required high-power density, lower maintenance cost and the high-temperature environment due to the integration with the internal combustion engine.

The main goal of the thesis is to propose, demonstrate and verify a combination of control techniques to maximise the performance of the multiport converter in all phases of on-vehicle operation.

In the first part of this work, a multiport converter is proposed to realise the requirements of the automotive industry to achieve greater performance in driveline electrification. The platform suggests the combination of previously discrete power electronics converter modules into one physical package commonising parts such as the microcontroller, DC link, heatsink and busbars. Therefore, for completeness, the current state-of-the-art of converter technology is presented along with challenges and their mitigation within the industry.

The central part of the thesis focuses on the optimisation framework of the converter. Multi-objective Optimisation (MOO) techniques are used to define and describe the optimisation goals. A comprehensive simulation model is built and verified both at component (power module and inductor) and system level (complete multiport converter) satisfying the mandatory requirement for clear objectives and toolset for validation of the optimisation control techniques proposed. Three distinct strategies are investigated including Phase Deactivation,

Phase Displacement and the utilisation of the optimum parameter set derived from the MOO study.

In the latter part of the work the performance and optimisation gains are evaluated through a combination of simulation and experimental data. The results show a distinct improvement comparing against conventional, non-optimised operation, demonstrating strong applicability of the techniques derived in the development of a high efficiency and high energy density automotive multiport converter.

Acknowledgements

This work is dedicated to the memory of Dr. Alessandro Costababer, my supervisor originally assigned, who sadly passed away during the PhD. His immense knowledge, dedication and sound guidance laid the foundations for this work.

The last eight years spent pursuing a part-time PhD with the University of Nottingham UK, alongside a full-time job, have not been easy. However, when I reflect on my academic journey, through all the unknowns and difficulties along the way, I realise that these challenges have taught me so many skills and values which I will now take to my career and treasure for the rest of my life.

The PhD was made possible by the joint funding by Cummins Inc. and the University of Nottingham. Therefore, I would first like to thank Dr. Neil Brown, Brad Palmer and Krzysztof Paciura from Cummins Inc. and Professor Chris Gerada, Dr. Michael Galea and Dr. Gaurang Vakil from the University of Nottingham, as without their efforts the work wouldn't have even commenced.

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Chapter 1

Introduction

The electric transport sector is continuing to grow and assume increasing market share. Despite the proliferation of a global health pandemic, collective electric vehicle sales worldwide doubled in 2021 from the previous year to a new record of 6.6 million and continued growing strongly through 2022 particularly in China, Europe, and the United States as illustrated in Figure 1.1.

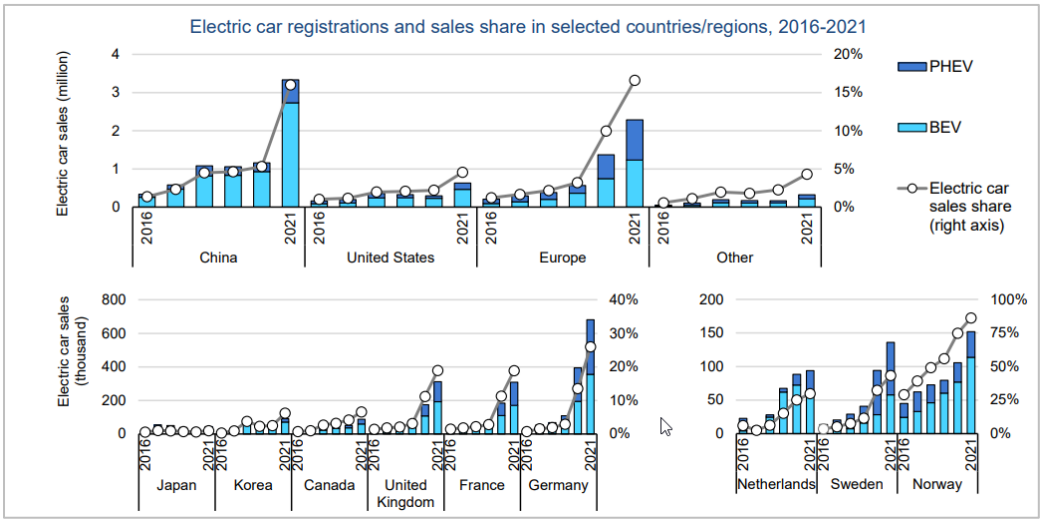

Figure 1.1: Electric car registrations and sales share in selected countries/regions, 2016-2021[1]

According to the International Energy Agency, the robust growth is driven by two key factors[2]: i) ever increasing support for transition to electric mobility, in the form of financial support for environmental regulatory measures such as policies set by the UN Climate Change conference (COP26) and China New Energy Vehicle (NEV) and ii) technological enablers such as electrical drive design architecture and developments in battery chemistry and manufacturing techniques;

both important factors in narrowing the cost gap between electric vehicles (EV) and their conventional Internal Combustion Engine (ICE) counterparts[1].

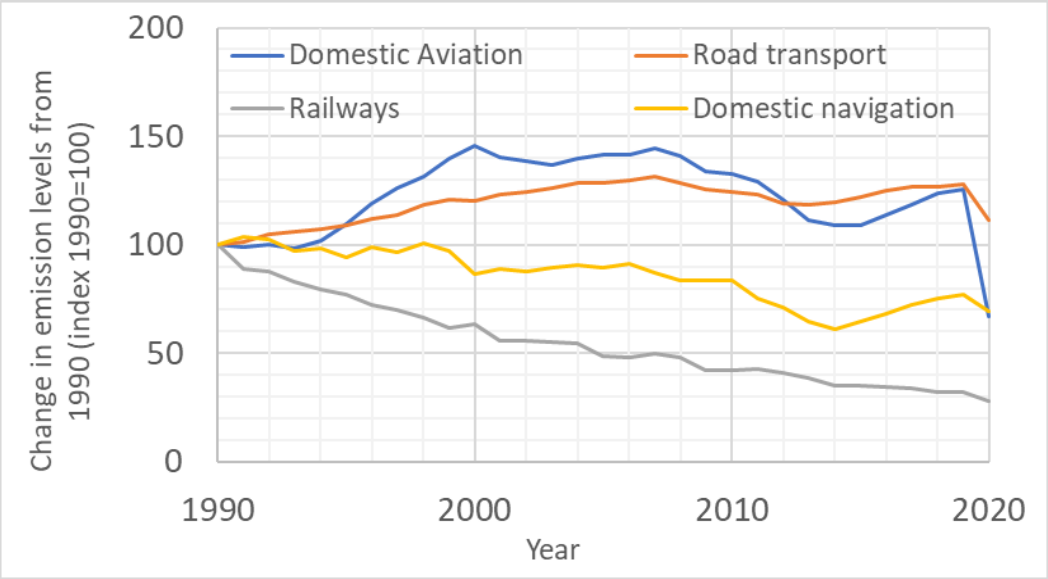

Figure 1.2. Greenhouse gas emissions from transport in the EU, by transport mode and scenario as published by the European Environment Agency[3].

1.1 Motivation for Carbon Reduction

Greenhouse gas (GHG) emissions within the road transport sector have been the highest in Europe since the 1990s compared to other modes of transport – such as aviation, maritime and rail according to data published by the European Environment Agency. This trend continued to rise, as shown in Figure 1.2, increasing by nearly 20% through the turn of the millennium before a drop in 2020 when the Covid-19 pandemic reduced travel significantly. While emissions from all other methods of transport plateaued and saw a significant reduction a decade prior, the road transport sector emissions remained high, accounting for 40.3% of all EU transport GHG in 2020. In order to address this issue, the European Commission, as part of the European Green Deal in 2023, is proposing a roadmap to reduce CO2 emissions from the heavy-duty road transport sector – trucks, city busses and long-distance busses which are responsible for over 6% of total EU GHG emissions and more than 25% of road transport GHG emissions in general. The proposed phased implementation

determines targets of 45%, 65% and 90% emissions reductions from 2030, 2035 and 2040 respectively. Due to the use case of the specific application scenario where they can be charged overnight and travel well defined and predictable routes, city busses in particular are targeted to transition to zero-emission by 2030 to further stimulate the adoption of electrification [4].

1.2 Strategy for Vehicle Electrification

Given its passenger carrying capability, one major point of growth in public road transport is driven by electrified busses, whereby the International Energy Agency claims that in 2018, there were approximately 460 000 electrified busses in operation around the world, up 100 000 from the year before [2]. In order to understand if the purchase and operation of these busses are to be commercially and financially viable, a lifecycle cost analysis has to be performed for the various applications of electrification technology within a bus. A study by Lajunen [5] showed, having compared 4 bus duty cycles including those from Finland and California that the cost over the lifetime, 12 years, of an electrified bus favoured hybrid variants over its conventional and fully electric counterparts due to lower cost. In order to reduce the cost impact of EVs, the United Kingdom (UK) government is providing funding support of more than 294 million pounds to local transport authorities which is aimed to subsidise the initial purchase, maintenance and infrastructure cost of 4000 zero emission busses from 2021 to 2023 [6].

The US Drive partnership, made up of the United States Department of Energy (D.O.E), Ford, General Motors and multiple other energy and utility companies published a roadmap along with trends affecting electrification of drivetrains to identify key challenges and propose solutions to resolve them. Among some of the trends seen is in the adoption of electrified skateboard chassis by major manufacturers that includes both electric traction drive and energy storage, in place of conventional drive train setups. This provides greater vehicle design freedom, the ability to achieve modularity and ease of scalability. Secondly, vehicle performance requirements are driving the demand for higher power drivetrains as customers

require faster acceleration and larger, more versatile vehicles. Based on these trends, US Drive proposes a technical target for 2025, based on 3 key matrices [7]:

1) Cost difference between an electrified vehicle and a comparable Internal Combustion Engine (ICE) vehicle should be no greater than 3 years of fuel savings.
2) Increase in power density of 8x to meet packaging constraints within Hybrid vehicles which include other DCDC converters and onboard chargers.
3) Twice the reliability of traditional automotive life - 300,000 miles, to enhance the longevity of the vehicle.

Electrified Vehicle manufacturers must ensure that achieving one of these matrices does not come at the cost of another. For example, as part of the US Department of Energy's (DoE) efforts to achieve energy security, the Clean Cities program was launched. It encountered concerns from the consumer regarding idle reduction, whereby, turning the vehicle on and off would result in premature wear and consequently failure of the starter motor and battery. Therefore, it is clear that the challenge faced with automotive electrification is in balancing performance and safety requirements against implementation cost, packaged within a design that optimises for power density and thermal performance [8].

The objective to achieve the electrification strategies places a growing electrical power requirement on vehicles, as referenced in [9], for the following reasons: the need for new and improved vehicle architectures, power conversion on demand, the use of precise electronics control and fast, high power motion onboard the vehicle. These requirements further the advent of driveline electrification in the automotive space with the integrated power electronic converters as the heart of the system since they offer improved power density with simplified integration for vehicle manufacturers [10]. Due to cost concerns, many electric vehicle functions in the past were realised actively avoiding power electronic components [9]. However, since the early 2000s until now, major strides in the development of power electronic converters pertaining to density, reliability, thermal performance and control algorithms have been achieved placing them as a viable solution to many of the

challenges faced with on-vehicle power requirements in all aspects of vehicle design-powertrain, safety management, body and convenience [11]. This growth is set to increase with the electrification of vehicle drivetrains in the coming years as the demand for fully electric vehicles increases. US Drive proposes a 2020 cost target of $3.3/kW and 13.4kW/l and a 2025 cost target of $2.7/kW and 100kW/l in [7] through a combination of component and multiphysics integration. Figure 1.3 illustrates a cost breakdown of an inverter as a proposed target to meet the 2025 cost target. With this increase comes further development in the power electronic converter space and the objective of reaching even higher power densities and efficiency [12].

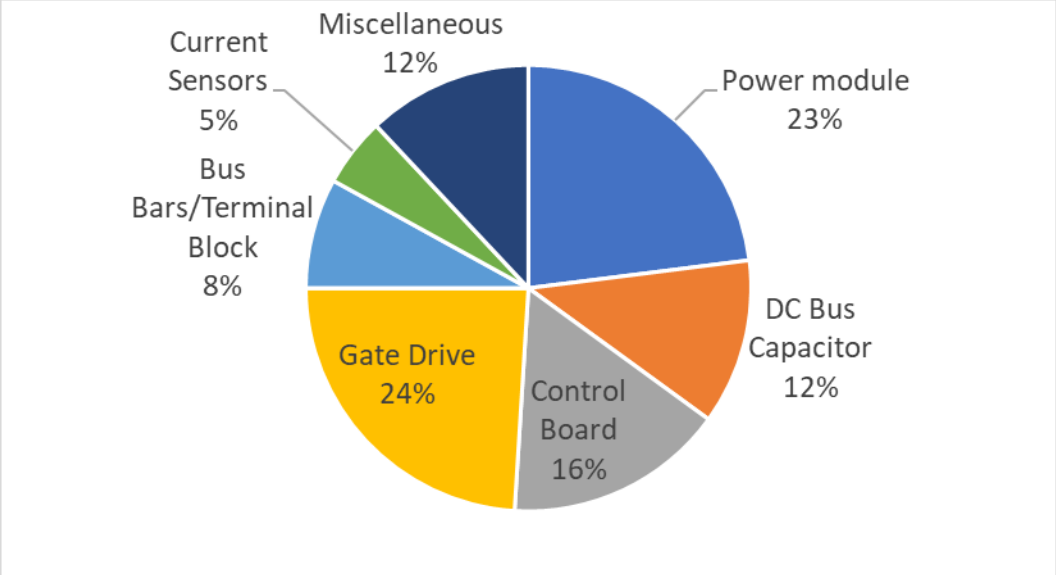

Figure 1.3 Inverter cost breakdown for a potential pathway to meet 2025 targets through the application of advanced integrated power modules; proposed DC link voltage range of 525-775V (650V nominal) and maximum current of 600A to achieve 100kW rating [7].

1.3 Industrial Association and Research Background

Given the current transition of the public transport sector to electrified drivetrains, the research effort was conducted with close links to Cummins Inc., the Tier-1 engine supplier of the 2016 Wrightbus Routemaster double-decker hybrid bus () to Transport for London, TfL [13]. Known also as the New Bus for London, NBfL, the drivetrain tuning and design would be optimised for routes in London, United Kingdom [14].

Figure 1.4. 2016 Wrightbus Routemaster Hybrid Bus (pictured) [14].

The goal of the research was to improve operational efficiency and manufacturability while reducing emissions, taking the parallel hybrid system consisting of a Cummins 4.5L Euro 5 diesel engine coupled to a Siemens electric drive [15] as a baseline. To this end, the engine would be upgraded to meet Euro 6 specifications, with maximum electrification to crank driven accessories, such as the alternator, cooling and lubrication pumps. Torque production by the engine would be supplemented by a Cummins electric motor which could also leverage regenerative energy as the vehicle is braking. Considering these objectives, the

research would iterate on the design and capabilities of the NBfL, by taking it as a technological and cost baseline to propose a fully optimised solution.

1.4 Thesis Outline

This thesis focuses on two topics. The first is the proposal of a multiport converter topology to meet the requirements of a London bus application and the second is to present the design and validation work of advanced control strategies to enhance the performance envelope, taking advantage of the integrated construction of the converter.

The stringent requirements of the London bus cycle provide strong justification and a requirements framework for vehicle manufacturers to meet. Baseline studies of pre-exiting converter technologies must be carried out to initially understand key enablers and identify developmental gaps. Next, a novel concept of an automotive multiport converter design is presented for evaluation. The Multiport converter is the amalgamation of 3 separate converter units- an inverter capable of bidirectional power flow to a PMSM (Permanent Magnet Synchronous Machine) and two DCDC converters for management of a shared DC bus and on-vehicle power conditioning. Each converter unit is validated and optimised individually to meet their specific functional requirements before adaptations are performed to physically integrate the multiport converter.

The second topic builds upon the baseline by studying the multiport converter performance attributes during simultaneous operation. To cope with the complexity of selecting an optimal control strategy for the inverter with trade-offs between conflicting performance objectives, the Multiple Objective Optimisation Problem (MOOP) solving technique based on a well-known economics theory, the Pareto Optimum, is applied. Advance control methodologies are developed to achieve the desired optimum operational point.

While studies on the advantages introduced by various multiport converter topologies [16] as well as efforts to improve general efficiency in hybrid vehicle topologies [17], [18] are well documented in literature, a fully multi objective optimisation of a hybrid vehicle solution- including energy storage power conditioning and management incorporated with the traction and low voltage bus, the complete hybrid vehicle electrical network, has not been presented before. Herein lies the novelty of this work whereby the optimum combination of singular converter units from conventional hybrid system architectures [19] into a multiport converter and collectively optimised according to specific operational requirements of the vehicle.

Design justifications as well as the results of simulation and experimental work carried out are presented, firstly to prove the effectiveness of the methods employed, and also so that the ideas presented may be further built on and deployed across a wider scope of electric drive applications. Concepts proposed within this thesis have been peer-reviewed as part of publications for which a list has been included in Appendix A.

In all, the thesis aims to:

- Propose the concept of a multiport converter through integration of standalone converters as a viable topology for hybrid buses.
- Demonstrate the utilisation of MOOP solving techniques within the specific context of automotive drive optimisation.
- Investigate and prove the effectiveness of advanced control techniques that improve individual components and collective performance and efficiency of the integrated design of the multiport converter.

To this end the thesis is outlined as below:

- Chapter 1 presents a general introduction to the current state of vehicle electrification and current motivations and strategies of governmental bodies behind global efforts.

- Chapter 2 gives a review of the state of the art of inverters and DCDC converters including the challenges faced by the respective technology implementations and mitigation actions taken to counteract them to bring them to market.
- In Chapter 3, a specific multiport converter design is proposed to satisfy the application requirements of a hybrid passenger bus. The multiport converter is separated into individual converter module for detailed analysis. Design methodology of each converter module is presented.
- The concept of simultaneous optimisation is presented in Chapter 4. MOOP is introduced to clarify the optimisation objectives. Key loss components identified are analysed within a simulation model and results of simulation sweeps are discussed. Advanced control strategies targeting the loss components are simulated and results presented. The optimal parameter set represented as a Pareto Front for multiple driving scenarios is presented along with performance gains obtained.
- Chapter 5 presents the experimental test rigs, used to validate design methodologies presented in the thesis.
- Finally, Chapter 6 presents general conclusions, considerations of limitations faced in this work and proposal for further work to be done.

Chapter 2

Review of Converter Technology

Legislation and proposed roadmaps by governmental and consumer entities drive requirements surrounding the design of automotive power electronics converters. It is clear that majority electric drivetrain manufacturers implement electrification technologies in 3 main areas: propulsion, hotel load supply and charging; where the propulsion converter space is dominated by the 3 phase, 2 level DC-AC inverter due to simplicity of control and low cost [20], while hotel load supply and onboard charging functionality is typically provided by DC-DC converters.

Taking the NBfL, as a baseline for further electrification [21], the need for power conditioning within between the drivetrain and hotel loads becomes apparent. This is driven by the requirements to supplement torque production by the 480Nm, Cummins B4.5 diesel engine [22] in propulsion mode, supply hotel loads (such as the cabin lighting and blown-air heating system), charge on-board energy storage devices (24V vehicle battery and ultracapacitor bank) during regenerative modes and finally to stop and restart the I.C.E when the vehicle is stationary. The functionality required is summarised in Table 1.

Table 1
FUNCTIONALITY OF CONVERTER COMPONENTS

	Functionality required	**Power flow direction**	**AC/DC**	**Voltage**	**Selected component**
Drivetrain	Propulsion and Regenerative Torque	Bidirectional	AC	275-400V	Inverter
Energy Storage	Charge and Discharge	Bidirectional	DC	250-400V	Bidirectional interleaved converter
Hotel Loads	Supply	Unidirectional	DC	24V (Galvanically Isolated)	Unidirectional isolated converter

AC driven drivetrain components such as the MG-inverter operate on a voltage bus approximately 30 times that of the DC driven hotel load components, making power conditioning and control between each node critical to system functionality. Differences in power flow direction, type and values are depicted as a simplified block diagram in Figure 2.1 showing the variety in type of electrical power needed to support vehicle functionality. The multiport converter co-locates all of this functionality within a comprehensive, single package, enabling optimisation through MOOP.

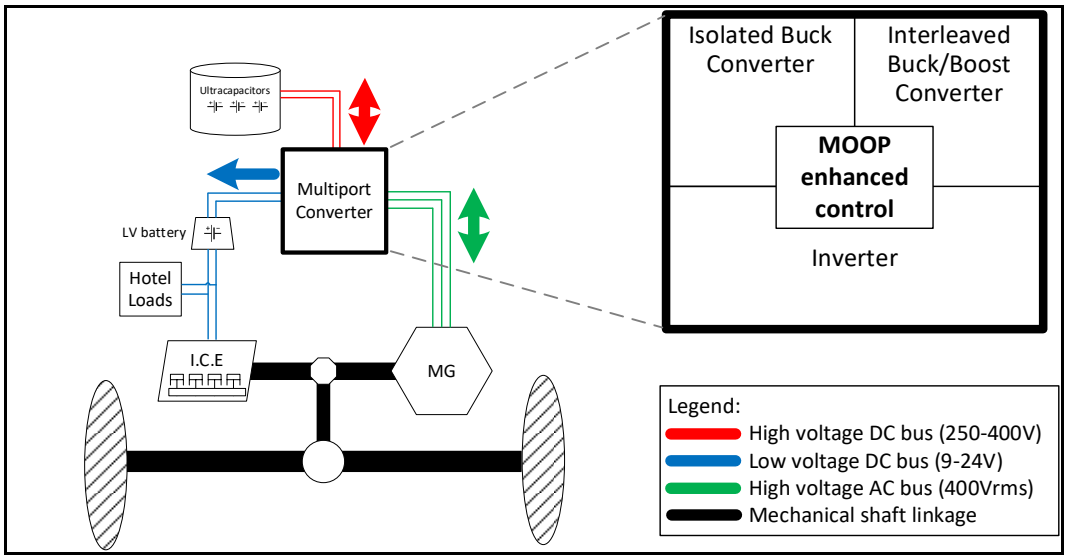

Figure 2.1: Vehicle component topology depicting multiple bus architecture supported by the proposed multiport converter governed by a unified controller operating the MOOP enhanced strategy to control power flow.

In this chapter, the multiport converter is analysed and presented according to functionality- propulsion inverters and DCDC converters to account for the differences in the state-of-the-art of technology between the two converter types, the trends and challenges faced and optimisation opportunities in hardware and software.

2.1 Electric drives and Propulsion Inverters

The traction inverter forms the central propulsion component within an electric drivetrain. As it is responsible for converting the DC power supplied by the vehicle energy storage into AC power in the electrical machine, the inverter is subject to great pressure for improvement, simultaneously requiring high power density, switching frequency, efficiency and high temperature operation capability over a wide load range.

2.1.1 High Voltage Trends and Silicon Carbide Technology

Recent trends show a shift towards 800V Electric Vehicle, EV powertrain architectures [20] as the increased voltage level allows for a reduction in weight and size of onboard power cables [23]. The increase in main voltage bus places the requirement for the blocking voltage of power modules to therefore increase, to at least 1200V to provide adequate margin. Silicon technology (Si) based switching devices have been under development for years and therefore has led to it being the dominant selection for power converter design. However, the development of better power modules in terms of current handling, efficiency and higher temperature has seen a reduction in pace as the material properties begin to reach a limit, restricting further progression, causing a subsequent migration to Silicon Carbide (SiC) technology, particularly in the recent decade [24].

The push for industrialisation of SiC technology by automotive applications [25] has led to the proliferation of challenges to established designs to allow for highly performant, compact, robust, and cost-effective solutions. As higher and higher voltages are favoured, at the greater switching frequencies enabled by SiC technology, the uniformity of current distribution becomes paramount to avoid lifetime degradation of the module, particularly at operation points close to peak ratings of the module. Therefore, it is important to design for mirror-symmetric cell layout of the commutation circuit formed with the DC link capacitor. Where perfect symmetry may be difficult to achieve due to hardware tolerances, approaches that utilise negative feedback from Kelvin sources of each chip connected via resistors on the gate-driver board [26]. The mechanism enables modules to compensate chip-

parameter deviations during the di/dt phase, subsequently bringing the modules to the same switching speed. This balances the currents and therefore the switching losses, avoiding critical overcurrent within the modules.

While dynamic control measures such as active compensation, Active Current Balancing (ACB) [27] and dead-time elimination schemes [28] and advanced baseplate such as pin-fin technology [29] may be utilised to allow high peak-power densities, high continuous power density of the inverter module relies on the thermal performance of the AC and DC interfaces, EMC filter, busbars and DC link capacitors. The DC link capacitor loss distribution can be expressed as:

$$P_{C,loss} = R_{ESR} I_C{}^2 \qquad (2.1)$$

where, $P_{C,loss}$ represents the losses in the elements of the capacitor, R_{ESR} is the equivalent series resistance (ESR) and I_C represents the RMS value of current. To optimise for the lowest $P_{C,loss}$, equation (2.1) clearly shows that both R_{ESR} and I_C must be reduced. R_{ESR} may be reduced through component selection and design, for example, a parallel configuration of film capacitors which is deliberately designed to avoid heat influx from its physical interfaces using a gap pad pictured in Figure 2.2 [25].

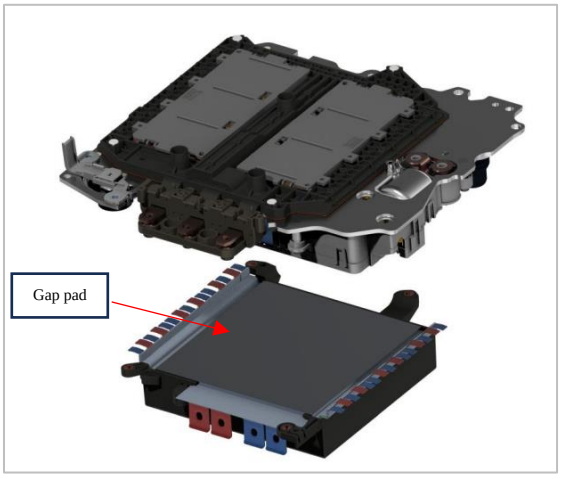

Figure 2.2. Parallel Bosch power stage and capacitor module with a gap pad to provide thermal separation [25].

Although I_C would be determined by the inverter operating point, sophisticated techniques which rely on phase shifting [30] the PWM pulses of one converter with respect to the other in a multi-converter setup may be used to lower the amplitude of capacitor ripple current which will in turn reduce I_C and therefore achieve loss reduction.

2.1.2 Module Packaging Trends

An early approach of a "sandwich" or Double Sided Cooling (DSC) structure automotive inverter power module is presented in [31] where designers target four main performance matrices – high temperature operation, reduction in thermal cycling, utilisation of silicon carbide and manufacturability. It is shown that by using the sandwich structure of connecting two Direct Bonded Copper (DBC) substrates, one on top of the device and one at the bottom, heat can be extracted by both sides. Furthermore, specific positioning of the substrates and dies has been performed such that uni-axial compressive force is applied to the dies during operation, increasing resistance to fatigue of the interconnects due to thermal cycling and therefore increasing the lifetime and reliability of the module.

Using similar key performance indicators (KPI), a review of a wide array of power modules developed by research institutes and industrial companies is presented in Figure 2.3, showing a clear increase in current handling capability from 2008 to present and a lower thermal resistance in DSC when compared

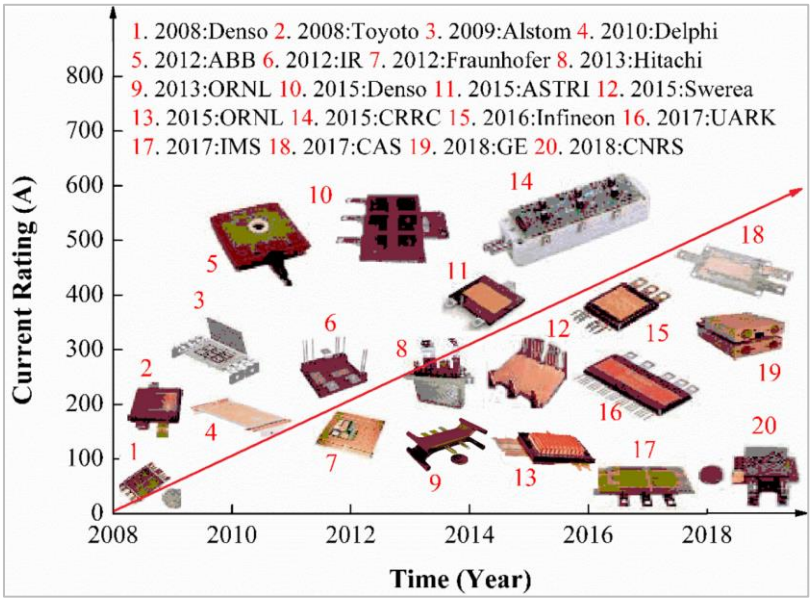

Figure 2.3. DSC Power Modules from institutes and companies [32]

to the single sided cooling counterpart. Each power module is then studied at a structural level as illustrated in by Figure 2.4, to identify the pros and cons of each packaging approach.

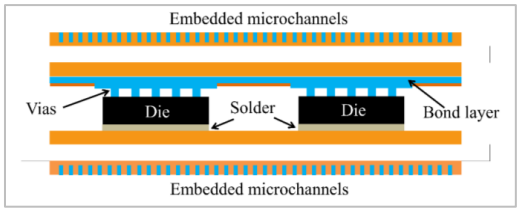

Figure 2.4. Power Module Structure [32].

Various packaging approaches and technologies are analysed according to their suitability for various different applications and tabulated in Table 2 for comparison.

Table 2
COMPARISON OF DSC POWER MODULE PACKAGING TECHNOLOGIES [32]

R&D Institutions	Packaging approach	Year	Pros	Cons
CPES	MPIPPS	1998	• Larger current handling capacity • Achieves direct die to module attachment. • Active cooling	• Copper posts need to be handled • Unreliable at high temperatures
	DAI	2001	• Better fatigue resistance • Better thermal management than the MPIPPS	• Dimpled copper plates need to be handled
	FCOF	2003	• Increased reliability because of the smaller contact area • Better thermal fatigue resistance	• Limited in voltage and current levels
	PowERazor	2014	• High temperature application • Stress relieving	• Rework is difficult • High cost because of silver paste
ECPE	Embedding technology	2012	• Multilevel integration • Improved thermal management • Light weight	• Complex and costly processing • Large thermal mismatch • Increased parasitic capacitance • Limited in voltage and current levels
ORNL	PBA	2012	• Integrated forced cooling capability • Shorter electrical paths	• Device top metallization • High thermal stress due to direct soldering
NCSU	PCoB	2016	• High integration • Ultralow parasitic inductance	• Chip top metallization • Complex structure
GE	POL	1995	• Shorter electrical paths • Multilevel integration for quasi-3D packaging	• Complex and costly processing • Large thermal mismatch • High thermal stress due to direct soldering
Alstom	Flip Chip	2000	• Shorter interconnect lengths • Lower cost than deposited metalization • Increased reliability	• Fatigue of solder sjoints • Limited in current and voltage levels
Denso	IPEM	2008	• Lower parasitic inductance • No base plate • Low cost	• Increased complexity • Low power density • Thermal grease is needed
Delphi	Viper	2008	• More flexible layout • High power density • Simple fabrication and assembly	• More susceptible to early failure • Thermal grease is needed

While the results demonstrate improvements in thermal performance of the inverter, the serial approach in the design of inverters, whereby power modules, gate drivers, converters, current measurement, passive components and converters are each developed in isolation, has begun to reach the limit. This presents the need for greater degrees of integration at the functional, structural and design level in order to enable the next step in the evolution of power electronics design. A study of key technological enablers for power module integration is presented in [33] where it is shown that the partitioning of power assemblies into substrate level blocks based on functional commutation cells provide low thermal resistance cooling and minimisation of commutation loop inductance. The integration of passive filter components at the substrate level also improves electromagnetic performance. It is however proposed that while sensing functions are easily accommodated on the power module substrates, the accompanying signal processing and gate drivers are implemented on a separate dedicated substrate using an appropriate technology.

2.2 DCDC Converters

PWM switching DCDC converters are used in the majority of DC-to-DC conversion applications due to continuous demand for smaller, lighter and more efficient power converters. Some popular topologies in the automotive space are illustrated in Figure 2.5 [34]. These are often found to have elementary PWM converters- buck, boost and buck-boost as building blocks- with various tweaks to configurations, numbers of parallel converters and circuit manipulation techniques. For instance, the cascade of the boost and buck converter led to the creation of the Cuk converter [35]. The use of other techniques include the inversion of the source and load [36], and differential or parallel connections of two or more converters [37].

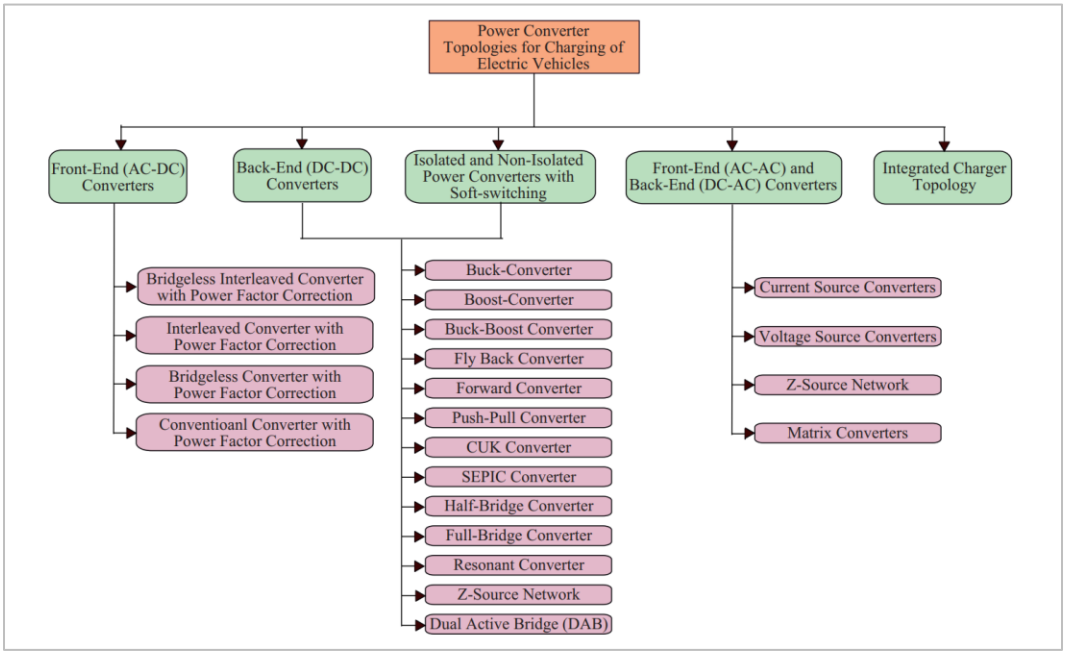

Figure 2.5. DCDC converter topologies [34].

2.2.1 Challenges Facing the State of the Art

The transition from conventional drive train setups to a more electric drivetrain has dramatically increased the number of providers as well as the demand for power electronic systems, namely sales volumes for modules, discrete devices and integrated circuits (IC) are the predicted to experience a compounded annual growth rate (CAGR) of 5.9% taking it from $26.07 Billion in 2023 to $43.67 Billion by 2030 [13]. This places enormous pressure on designers to optimise the entire vehicle power distribution network in terms of component utilisation by targeting cost and volumetric minimisation; with the key restrictions being application requirements. An example of a three-port multiport converter is presented in Figure 2.6; where the design has to condition power from 3 galvanically isolated sources- a high voltage (HV), low voltage (LV) and single phase AC grid connection for a vehicle onboard charging application. Here, the designers were able to integrate two dual active bridges (DAB) into a single Triple Active Bridge (TAB) converter thus achieving a component saving by commonising the isolation transformer and removing a H-bridge [38]. Despite this, the TAB is not ideal for the application due to the large operational voltage range of the each of the ports, making the design of the transformer nearly impossible to optimise for cost. This is a major concern as an added transformer or inductor implies additional cost and losses [40] within the DCDC converter which therefore have to be kept as low as possible so as to not compromise the advantages offered by the rest of the powertrain architecture [41].

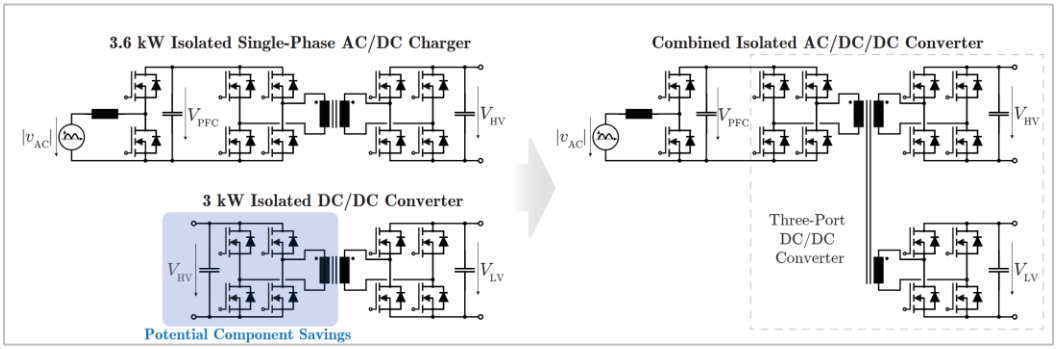

Figure 2.6: Potential component saving achieved through integrated converter design [38].

2.2.2 Cost Optimisation via Hardware

A key challenge facing the state of the art is that Electric Drive Vehicles should cost no more than comparable ICE vehicles [7]. All in all, the cost targets set as part of the US Drive 2025 target-setting process, the cost difference should be no greater than 3 years of fuel costs savings and this resulted in a $6/kW for a 100kW peak power drive system. This objective is further refined into a specific DCDC converter cost reduction target of $30/kW, a 40% reduction form the current cost in tandem with specific power increase of more than 300% to 4kW/kg by 2025. In this chapter, DCDC converters are selected due to the simpler scope of its function compared to the inverter, despite sharing nearly all its components with the DC-AC counterpart. This makes technical developments and cost savings for DCDC converters highly transferable to inverter designs. The mitigation approach taken appears two-fold: reduction of cost per kilowatt through component selection and design, and secondly, increase kilowatt per kilogram through efficiency improvements like advanced converter topologies and devices.

Power Modules and Gate Drivers

According to US Drive, Power Modules and their corresponding Gate Drive circuitry account for approximately half the cost of a traction inverter (graphically represented in Figure 1.3), making it a clear optimisation target for the industry. The cost of a power module can be divided into two main parts- the cost of the bare die and the packaging costs. When considering the manufacturing process of SiC power devices, four major factors, SiC substrate, cost of epitaxy, device fabrication and the yield are the main drivers of cost. As described in [42], the seeded sublimation process used to produce SiC is slow, requiring significant energy to enable the 2200°C growth process producing a final usable boule of no more than 25mm in length. There are also the additional costs of epitaxy - growth of a high quality SiC device layer on the substrate surface and device fabrication, both requiring higher temperatures and more expensive consumables. Finally, the yield, which is the percentage of good dies produced per wafer has a direct impact on the cost of production [43]. A larger chip

area would result in a lower yield and therefore result in higher cost as illustrated in Figure 2.7.

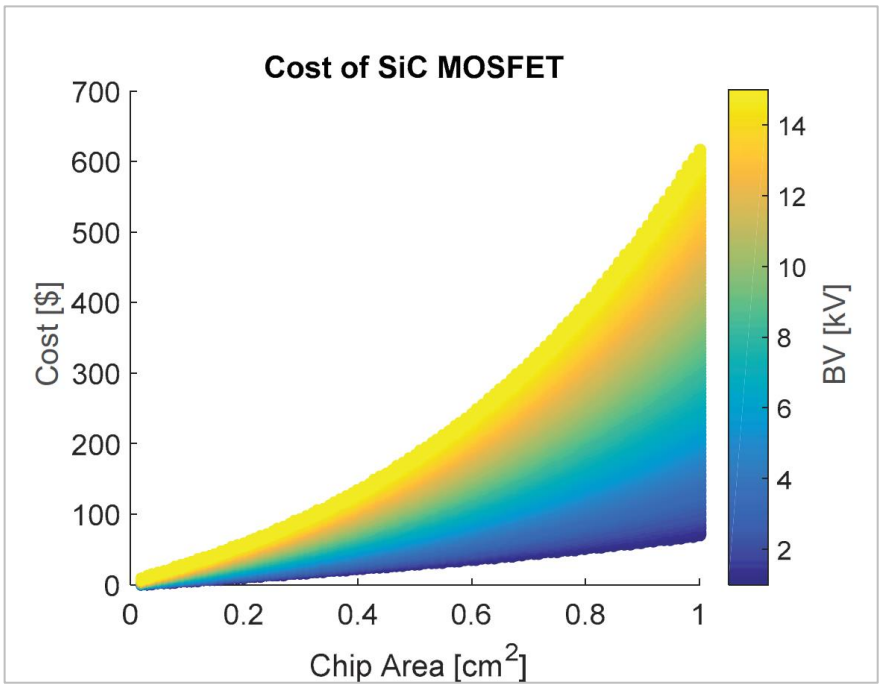

Figure 2.7. SiC MOSFET cost vs active chip area at different voltage levels.

While a year-on-year downward trend in cost (presented in Figure 2.8) is predicted due the increasing market penetration of SiC devices and corresponding supplier offerings, there are multiple steps designers can take to mitigate against the cost of power devices and drivers. One method is to incorporate SiC MOSFETs where possible to utilise the built-in body diode to eliminate the need for a separate anti-parallel diode. The application of SiC will also provide more efficient power conversion leading to reduced baseplate cooling requirement.

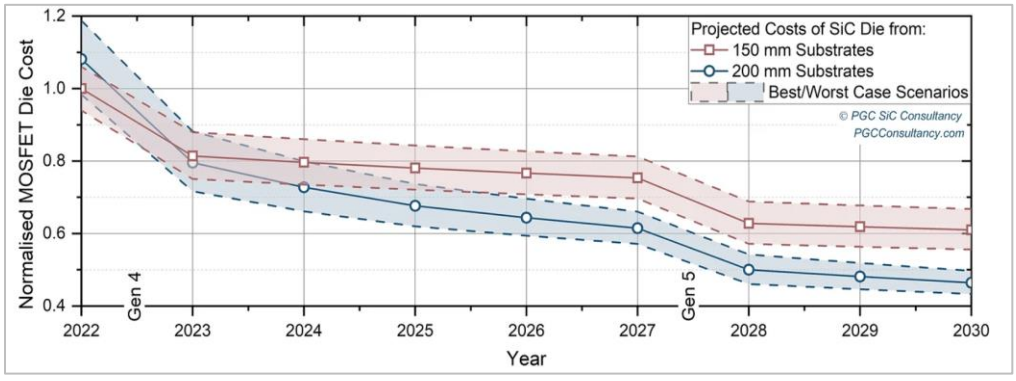

Figure 2.8: PGC Consultancy SiC cost forecast model based on a best-in-class 2021 1200V/100A device [42].

Several low-cost gate driver topologies have been proposed in literature that utilise novel techniques to achieve the same or better control performance of SiC MOSFETs, while providing sufficient bandwidth and voltage swing to appropriately drive the power module. One such approach is through the application of a method known as Active Gate Driver (AGD). While variants of this concept have been investigated and presented in gate driver optimisation studies - Lobsinger and Kolar [44] present a closed loop solution for Si IGBTs where dv/dt and di/dt are added to a single reference and Krishna and Hatua [45] propose a transistor based custom solution to circumvent the use of costly OPAMPs, these approaches fail to consider fast turn of SiC MOSFETs. The solution presented in [46] overcomes these weaknesses through the implementation of a turn-on methodology to arrest the current overshoot without reducing turn on di/dt through a transistor-based implementation. By performing closed-loop control of the gate driver, drain-source current and voltage can be accurately controlled during turn-off and turn-on transients. During turn-off switching transition, the turn-off voltage overshoot is limited by controlling turn-off di_{ds}/dt. Conversely, during the turn-on transition, control of drain current prevents drain current overshoot and fast switching speed. This concept demonstrates the possibility to achieve more efficient switching and less overall losses through a low-cost gate driver design.

Passive Components: Capacitors

US Drive lists capacitors as contributing 12% to the estimated overall cost of an inverter as illustrated in Figure 1.3. The challenge with DCDC converters however, is that different topologies entail varying numbers of capacitors needed, and the specific capacitance in order to realise the design. The three main capacitor technologies available today are: multi-layer ceramic capacitors (MLCC), metalized polymer films (MPPF) and Al electrolyte (Al). A comparison of energy densities versus cost is presented in [47] where, although Al electrolytic capacitors achieve the highest densities and MLCC offer high current ratings within a small package size, polymer film capacitors provide the most well balanced properties

regarding the key parameters such as ESR and operational temperature range ruggedness.

A comparison of the power density of the three capacitor technologies is presented in Figure 2.9 where it is shown that high purity biaxial oriented polypropylene (BOPP) film material capacitor achieves a very close energy density compared to Al electrolytic capacitors when the loss of energy storage density in the winding construction because of the overhead necessary to achieve self-healing property.

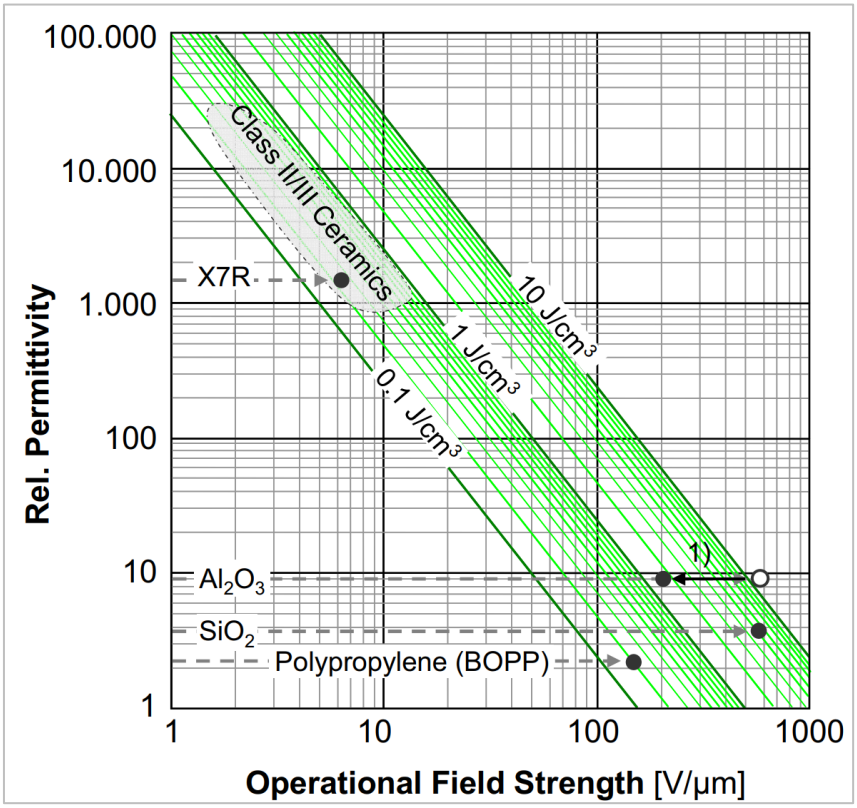

Figure 2.9: Energy storage capacity of various dielectric materials compared [47].

When compared cost wise, a study of capacitors of a similar voltage rating, lifetime and operational temperature showed that film capacitors were nearly 9.7 times (depicted in Figure 2.10) more costly than electrolytic capacitors [48].

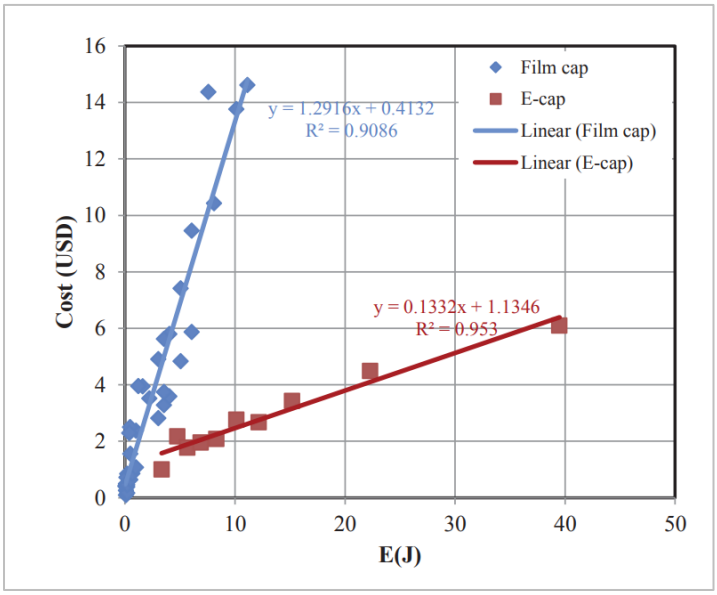

Figure 2.10: Statistical results of unit cost of standard film capacitors and Aluminium electrolytic capacitors [48].

When considering the trade-off in capacitor selection and sizing, it is important to weigh the cost against the following parameters:

i) Expected lifetime definition [49], [50], [51]: it is possible to select capacitor technology to achieve a certain lifetime target. Therefore, lifetime itself is not a deterministic factor on which capacitors should be chosen.

ii) Capacitance required: the primary selection criteria for capacitance required is typically driven by voltage ripple from initial analysis of a converter design.

iii) Electrical Stress: the voltage stress across the capacitor is a result of the system specification and the voltage ripple ratio due to the relationship between the modulation ratio and DC link voltage at a particular operating point.

iv) Power loss calculation: the power loss of a capacitor is dependent on ESR and ripple current stress. An equivalent electrical model can

be used to calculate the root mean square (RMS) value of the low frequency ripple. This topic is further explored in Chapter 4 along with a novel technique for mitigating against these losses through carrier phase displacement.

v) Thermal stress calculation: thermal stress is a critical factor that must be considered as it directly corelates to all aforementioned criteria, and results in permanent loss of performance due to degradation. A concise overview of capacitor failure modes across Al, MPPF and MLCC capacitor types is presented in [52] in which thermal stress caused by current ripple stress and ambient operating temperature are listed as critical stressors causing wear out failure- where electrical parameters such as capacitance, ESR, leakage current, dissipation factor and insulation resistance deviate from manufacturer's specifications causing the capacitor to prematurely reach end-of-life.

Passives Components: Inductors and Transformers

A possible cost mitigation on magnetic components is to avoid the usage of costly material such as Litz wire which typically has a poor winding-fill factor due to the insulation thickness [53] and requires the expensive wire trapping process and instead compensate for losses through design. As such, the industry has seen adoption of PCB winding transformers and inductors. However, due to the much smaller amount of copper present on the PCB, the existing copper must be used as efficiently as possible by reducing the number of turns, N as well as any high frequency (HF) current propagation effects- such as skin and proximity effect. Achieving the necessary large leakage inductance [54] value is done through the addition of discrete PCB-winding inductors that employ the compensating fringing field concept (CFFC) [53] which uses the y-component of an existing fringing field around the inductor air gap to compensate the y-component of the parasitic skin and proximity fields, and thereby reduces losses in the windings. An alternative approach to optimise the magnetic design of PCB-winding transformers is proposed in [55] where an

interleaved, split-core EI core structure is designed for a resonant converter application. This design is based on a conventional UI core transformer with an added centre post to provide a path for flux to flow, which is not fully coupled between primary and secondary windings and is therefore by definition, leakage flux, an essential component to the power conditioning capability of converters. Here, leakage flux is easily controlled by varying the reluctance of the centre post through selection of core material and geometric design. It is proposed that for a certain magnetising inductance, Lm, the leakage inductance value selected, Lk is optimised so that the sum of the losses due to deviation of the switching frequency to resonant frequency and core losses-derived from Steinmetz equations is minimised.

Some converter topologies may utilise the coupling inductance as the main mode of power transfer, for example in a conventional buck-boost DCDC converter. Here, an optimisation is proposed in [56] where the airgap width is increased to the maximum permitted, while preserving the winding fill factor, in order to reduce saturation in the airgap due to fringing flux and therefore, reduce copper losses. Depending on converter layout, designers may position the airgap at a location easily accessible by the cooling circuitry by taking advantage of advancements in additive manufacturing which allows for more design freedom at lower cost. The combined benefits of reduced losses and enhanced cooling at the core will offer the advantage of higher mass and volume savings.

2.2.3 Cost Optimisation via Software

Novel software-based solutions have also been developed to compensate for the shortcomings brought about by component and cost savings. Designers aim to match or improve upon the performance, efficiency, and feature set of multiple single converters by iterating on control schemes that enable multiport converters to operate collaboratively. One example of a multiport three phase current DC link AC-DC buck boost converter, composed of a three phase current source rectifier (CSR) front-end and a three level dc stage with 2 independent output ports is presented in [57], where, a synergetic control strategy is applied to coordinate the modulation of the CSR and

DCDC converter stage to retain all advantageous features such as seamless transitions between operating modes and modulation schemes and allow lost-optimum operation by reducing the number of switching instants. While synergetic control matches the performance of the conventional implementation within buck mode, a significant improvement in efficiency is demonstrated within boost mode compared to the state of the art, across a wide load range, from 95.7 to 96.9% at 2kW (20% load) and 97.9 to 98.4% at 10kW (100%load). This is achieved by utilising the DCDC converter stage to shape the DC link current into the six-pulse shape that would facilitate 2/3 PWM operation of the CSR stage. An important benefit that this method offers is that the inner DC link loop gain is not affected by transitions between buck and boost modes, ensuring resilient and robust DC link current tracking capability which is critical to provide a seamless transition during operation.

Therefore, despite the cost and technical challenges faced by the current state of the art, it is possible through specific component selection and design to achieve a compact, high efficiency, automotive multiport converter while maintaining a high power output [38].

Chapter 3

Proposal of Multiport Converter Design

The structure of the proposed multiport converter consisting of a 3-phase VSI, an isolated Buck converter, and an Interleaved Buck/Boost converter is shown in Figure 3.1. The DC-AC stage uses six N-Channel Silicon Carbide MOSFETs as top switches $(S1, S2, S3)$ and bottom switches $(\overline{S1}, \overline{S2}, \overline{S3})$ respectively.

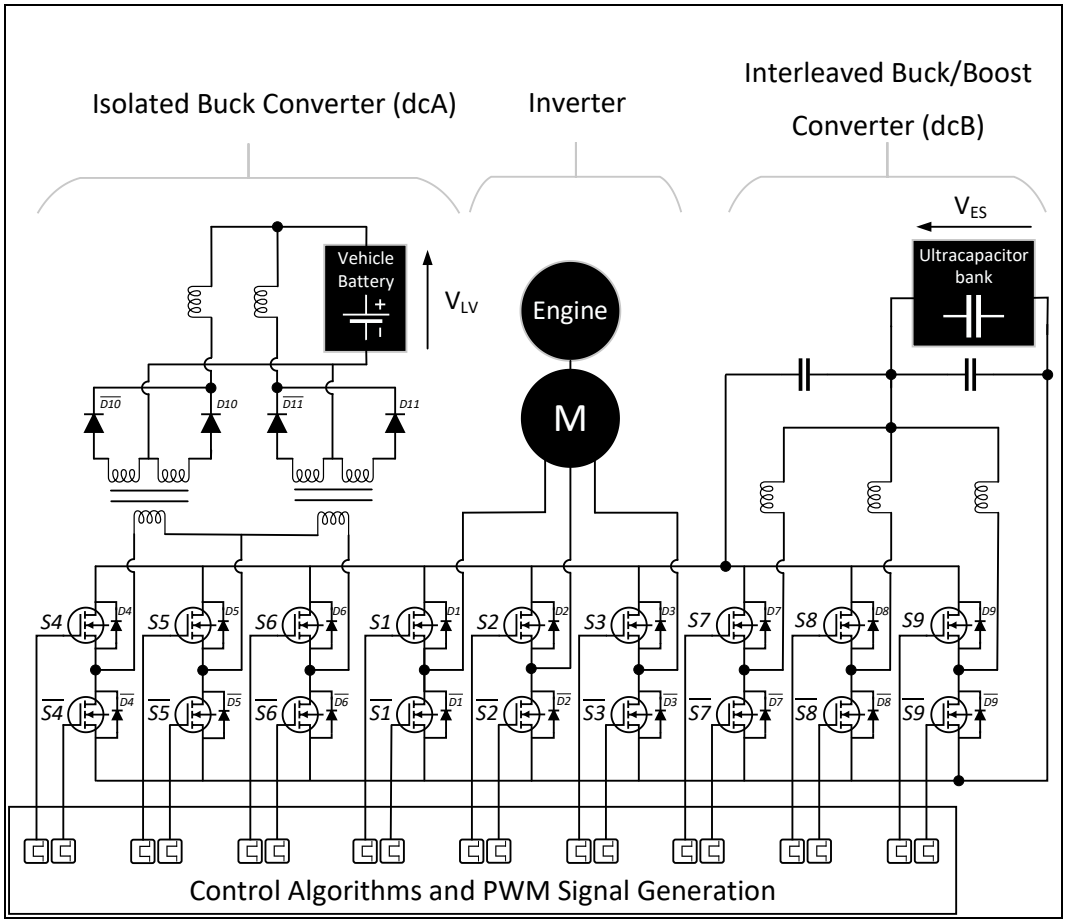

Figure 3.1: Multiport converter topology consisting of an Inverter, Inv, an isolated buck converter, dcA and a non-isolated interleaved buck/boost converter, dcB.

Similarly, the Isolated Buck and Interleaved Buck/Boost DCDC converter, hereon referred to as dcA and dcB respectively, follow the identical switch technology and arrangement where dcA uses top switches $(S4, S5, S6)$, bottom switches $(\overline{S4}, \overline{S5}, \overline{S6})$ and dcB uses top switches $(S7, S8, S9)$ and bottom switches $(\overline{S7}, \overline{S8}, \overline{S9})$. All switches share a common cooling plate and are distributed on both sides, together with magnetic components for full utilisation of the active cooling area.

As can be seen, the 2 level Inverter and dcB act together to condition power flow between the PMSM and ultracapacitor energy storage device. DcA provides further capability of charging the low voltage vehicle battery and supply hotel loads at a much higher efficiency compared to conventional belt-driven alternators.

The priorities determined when considering the design of the multiport converter are as follows:

1) Safety and efficiency. Parallel phase operation offers increased robustness in the overall converter operation since, should one phase be damaged, the remaining phases in parallel will allow the vehicle to continue safe operation. The selected design must deliver performance that balances the requirements for safety against the efficiency capability of the selected design to ensure vehicle range capabilities are met.
2) Modular and simple control design to facilitate easy scalability efforts in line with rated power requirements of different vehicle classes. Only topologies that allow additions or removal of physical hardware phases with minimum redesign effort and part cost are considered.

The topologies for each converter section are selected to meet the requirements. The simplicity of 3 Phase, 2 level inverter, only requiring 6 switches enabled the designer to take advantage of the commonly available 6 pack MOSFET or IGBT power modules widely available on the market from all main manufacturers such as Cree and Infineon [58]. While the efficiency of the selected topology is lower than multilevel inverters [59], the integrated design of the 6 pack power modules provide some gains in power density.

To match the power requirements of the inverter, dcB also implements 3 phases in parallel. DcA on the other hand, implements 2 phases in parallel through a split winding transformer which enables a high voltage conversion ratio, thus reducing stress on the power modules while also providing galvanic isolation. When comparing the selected DCDC converter topologies against other popular design approaches such as the Dual Active Bridge (DAB) and Series Resonance Converters (SRC), the trade-off is similar to that of the inverter, whereby some of the higher power density afforded by the DAB and efficiency by the SRC [60] is sacrificed for a simpler, redundant converter module design. Preliminary analysis was carried out in the early stages of the thesis work consisting of converter simulations corroborated by component-level hardware verification, confirming that the requirements would still be achievable despite compromises made in topology selection.

Finally, centralising the design of each of the converter modules on a single hardware design type- the 6 pack not only facilitated the converter to achieve the requirements but also eased planned manufacturing process and vehicle driveline serviceability through economies of scale.

3.1 Inverter and PMSM

The 2-Level inverter was proposed as a suitable solution to control a 3-phase interior permanent magnet synchronous machine (PMSM) due to the high degree of control achievable via vector control, where field oriented control techniques are used to optimally set up the flux for maximum torque performance based on the machine parameters as listed in Table 3.

Table 3
INVERTER AND PMSM PARAMETERS

Parameter	Value
Machine type	IPMSM
Polepairs	8
Base speed	1200RPM
Torque	200Nm (cont), 350Nm (peak)
Inverter	3ph 2-level inverter
Coolant inlet temperature	105 degrees C
Heatsink	Aluminum, Liquid cooled

For commercialisation purposes, the standard 2-level inverter is preferred for simplicity and relative ease of applying redundancy to achieve higher degrees of robustness due to the smaller component count [61]. Furthermore, it is expected that the majority of the loss reduction will be achieved through the application of SiC MOSFET over the silicone-based counterpart as presented in [62]. As the proliferation of wide-bandgap devices increases, it is expected that manufacturing and material cost will reduce, thereby increasing the viability of SiC multilevel automotive inverters in the future.

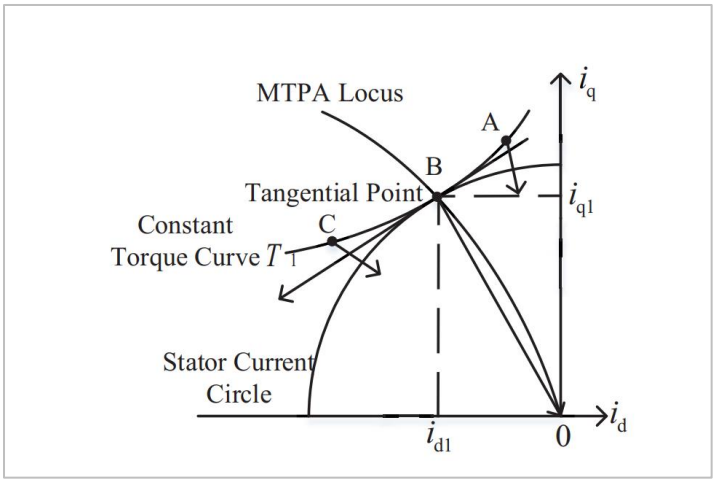

Figure 3.2: Maximum Torque Per Ampere MTPA with reference to the dq frame [63].

The mathematical model of the IPMSM, relationship between flux and current and the electromagnetic torque equations are provided:

$$\begin{bmatrix} v_d \\ v_q \end{bmatrix} = R_S \begin{bmatrix} -i_d \\ -i_q \end{bmatrix} + \begin{bmatrix} \frac{d}{dt} & -\omega_r \\ \omega_r & \frac{d}{dt} \end{bmatrix} \begin{bmatrix} \Psi_d \\ \Psi_q \end{bmatrix} \quad (2)$$

$$\Psi_d = L_d i_d + \Psi_f \quad (3)$$

$$\Psi_q = L_q i_q \quad (4)$$

$$T_e = \frac{3}{2} pp\left[\Psi_f + \left(L_d - L_q\right) i_d\right] \quad (5)$$

where T_e represents electromagnetic torque, pp is the number of pole pairs, ω_r is the rotor speed in electrical radians per second, Ψ_d, Ψ_q and Ψ_f are d-axis, q-axis and magnetic flux respectively. L_d, L_q and I_d, I_q are inductances and currents in the dq axis. Derivations of (2)-(5) taken from existing literature [64] are included in Appendix B for further reference.

This thesis will not focus on the design procedure of the PMSM as it is based on a preexisting design by Cummins Inc. Instead, validated machine parameters were taken and implemented within controls schemes developed as part of the thesis work. The software implementation is then validated firstly in

simulations and finally in a complete hardware setup prior to vehicle deployment as described in Chapter 5.

The inverter is controlled through a classic cascaded torque-current controller where the current references are determined via the Maximum Torque Per Ampere (MTPA) tracking strategy [51, 52] to precisely calculate control parameters taking variation of machine flux and inductances in the d and q axes into account-the basic principle of operation is to locate the tangential point between constant torque curve and stator current circle as illustrated in Figure 3.2. Therefore, the mathematical dynamic model of the PMSM has to be described in a synchronously rotating dq reference frame [66] for the controller model to function accurately. This is commonly done through projection of the abc frame to the dq rotating reference frame, pictured in Figure 3.3(a), as derived in [67] with the assumption that the armature flux linkages can be derived into 2 components-directly in phase with the magnets in the rotor, i_d and in quadrature with the rotor i_q. This relation is widely known as the Park and Clarke relation and is implemented to convert the abc frame to dq. The inverse is used to go from the dq frame to abc as shown in Figure 3.3(b).

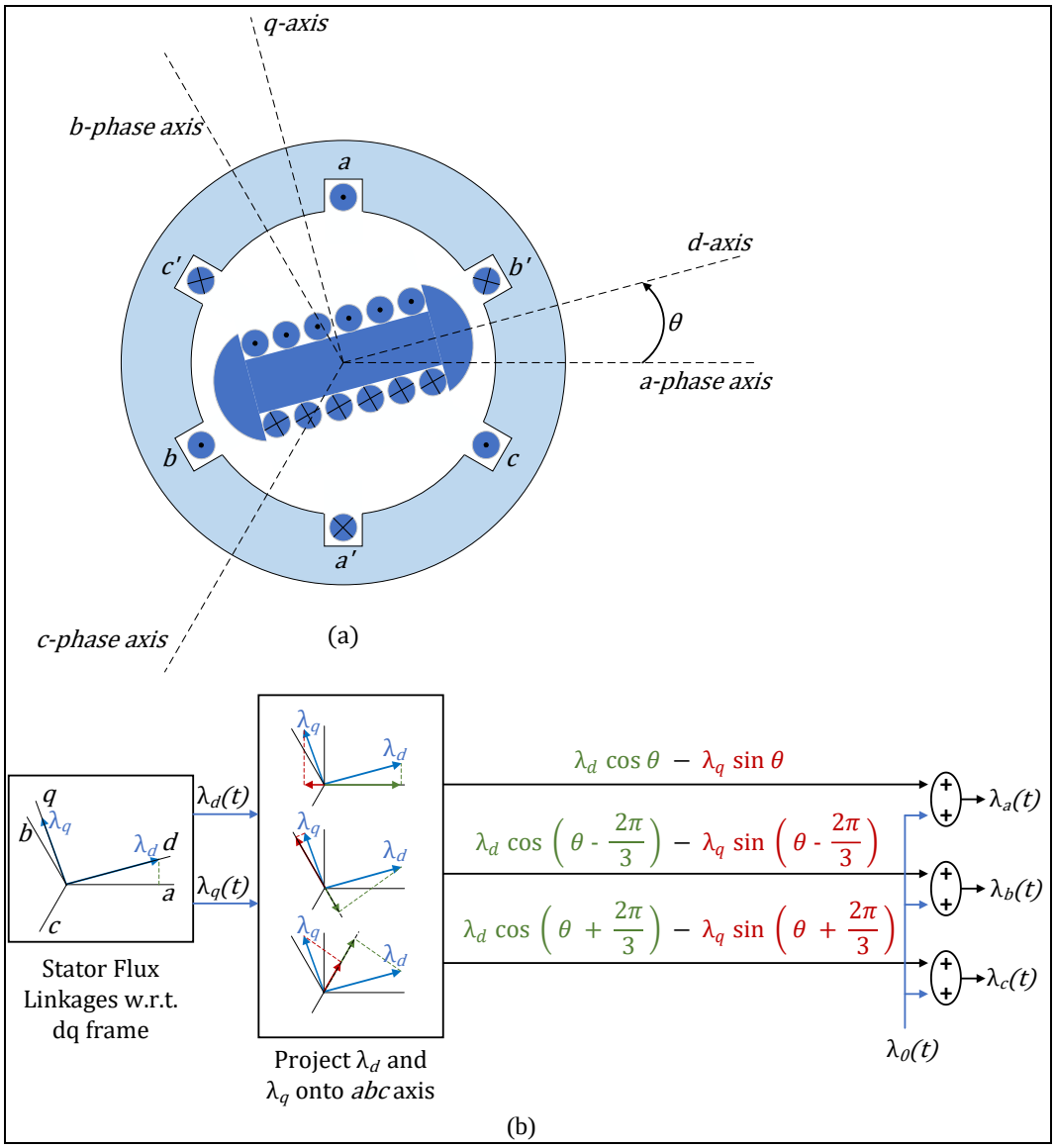

Figure 3.3: Illustration of Park transformation. (a) Three phase synchronous machine with magnetic axes labelled. (b) Park's derivation of the inverse transformation.

As machine speed increases, it is necessary to also consider voltage limitation to sustain control of the torque. To achieve this, the i_d current reference is selected to suppress the flux within the machine in a scheme known as field weakening. The cascaded controller is implemented with classical Proportional Integral (PI) controllers as illustrated in Figure 3.4.

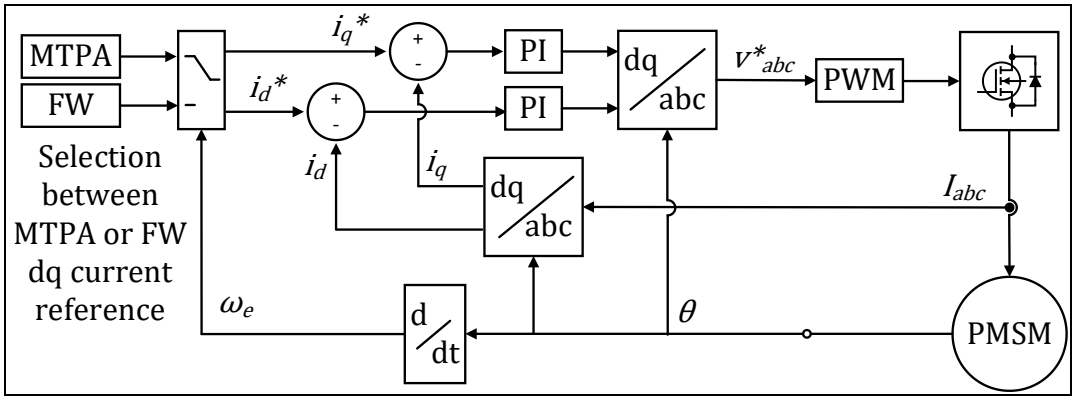

Figure 3.4: Inverter control algorithm structure.

3.2 Isolated Buck Converter (dcA)

The main function of this converter is as an alternator replacement, where, as seen in Figure 3.5, phases 4 and 6 are driving the primary side of a split winding planar transformer, which was added to enable four features:

1) Reduced commutation stress and losses in the rectification diodes, D10, $\overline{\text{D10}}$, D11, $\overline{\text{D11}}$.
2) High switching ratios to step from 800V (primary) to 28V (secondary).
3) Increased power density through direct thermal interface to the heatplate.
4) Parallel operation of current for higher total output current.

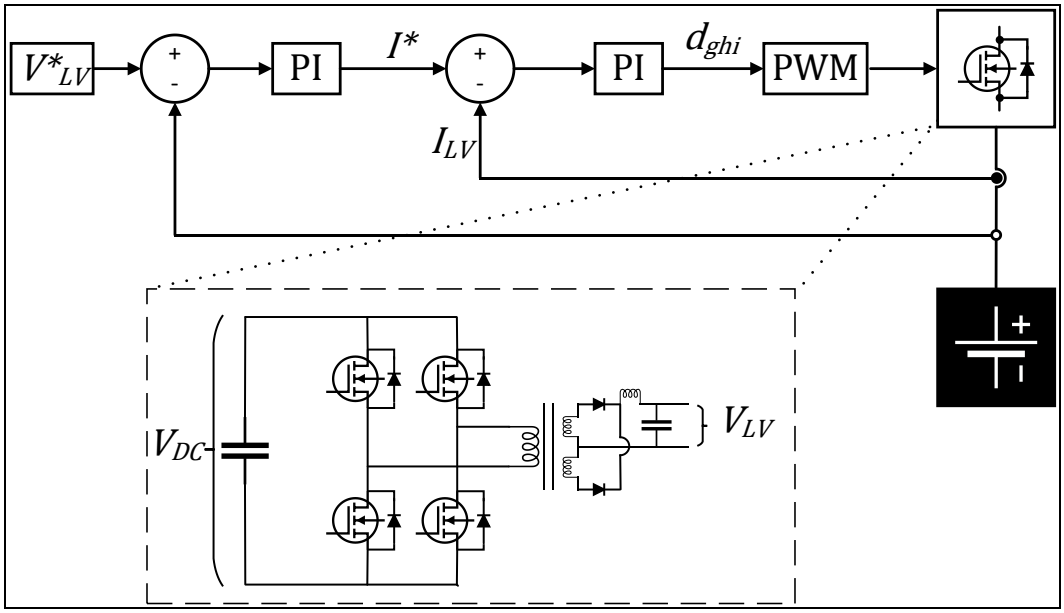

Figure 3.5: Isolated Buck Converter control algorithm structure.

The converter module only operates in Buck mode which is controlled through a cascaded voltage- current PI controller (illustrated in Figure 3.5). Power saturation limits are applied according to the engine power-speed profile to avoid engine overload. In low hotel load conditions or during engine start, the converter switching is also stopped to preserve efficiency.

The fundamental principle of control of the power flow within this converter is based on adjustments of the voltage drop across the main inductance component. This is controlled by phase shifting the voltages between the legs of the converter; phases d and f with respect to phase e.

Considering circuit component parameters, Equivalent Series Resistance, R_{dcA_ESR}, dcA inductor, L_{dcA} and capacitance, C_{dcA}, the desired LV battery voltage, V_{LV} is achieved by controlling the phase shift angle, θ applied to the converter plant model, $G_{\theta VdcA}$ (derivation given in Appendix C) for a DC link voltage $V_{DC:}$

$$G_{\theta VdcA} = \frac{V_{LV}(s)}{\theta} = \frac{V_{DC}}{s^2 L_{dcA} C_{dcA} + s\frac{L_{dcA}}{R_{dcA\_ESR}} + 1} \qquad (6)$$

As experimentally demonstrated in [68], the electrochemical impedance of lead acid batteries varies with state of charge (SOC). To ensure robustness in PI controller algorithm developed for the converter, a small signal model is developed based on (6) where the transfer function is:

$$SysTF_{dcA} = \frac{K_{pdcA}s + K_{idcA}}{s}\left(\frac{V_{DC}}{s^2 L_{dcA} C_{dcA} + s\frac{L_{dcA}}{R_{dcA\_ESR}} + 1}\right) \qquad (7)$$

Where K_{pdcA} and K_{idcA} are the proportional and integral gains of the controller respectively, V_{DC} is the DC link voltage, t_r corresponds to the transformer ratio and R_{dcA_ESR} is the Equivalent Series Resistance of the circuit, including track parasitics and ESR of the filter capacitors and lead acid battery.

Simulation derived bode plots are compared in Figure 3.6, by varying R_{dcA_ESR} from 1mΩ to 8mΩ while keeping the gains of the converter constant at $K_{pdcA} = 5.5$ and K_{idcA}=0.01. As can be seen, the open loop performance is shown to be stable throughout the operational range up to 10krads^{-1} with 86.9 degrees phase margin despite worst case variation of resistance.

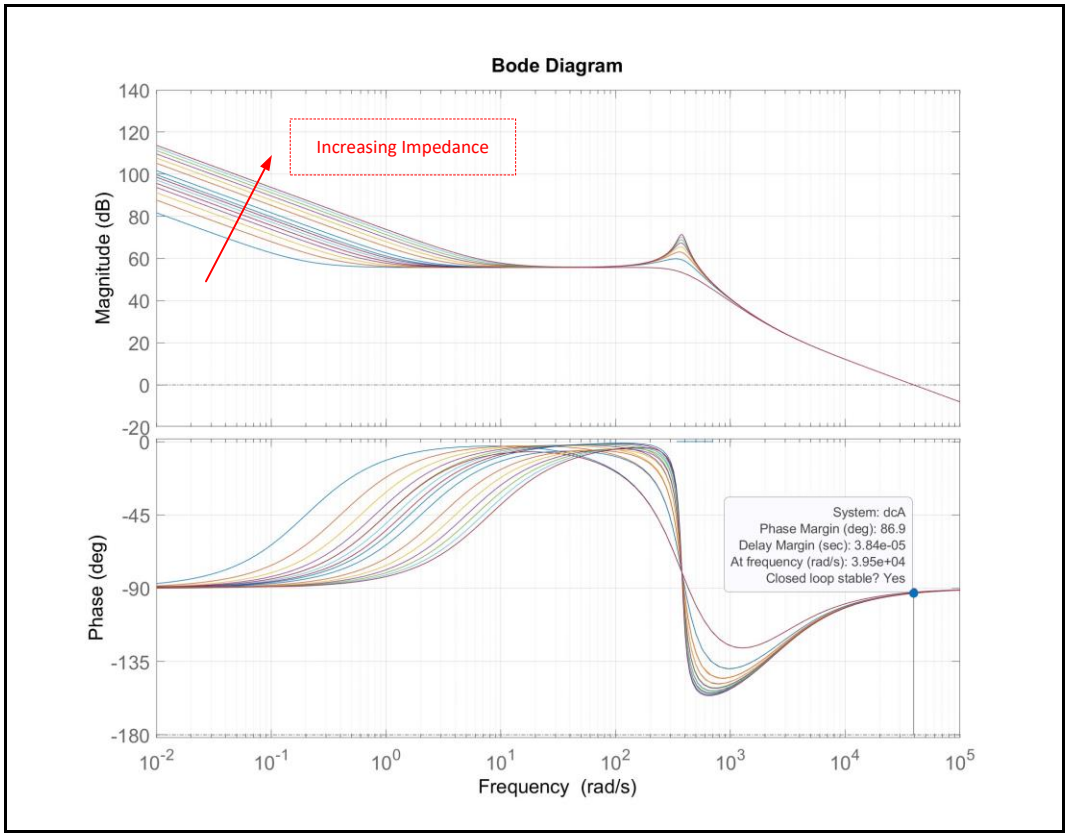

Figure 3.6: Isolated Buck Converter (dcA) frequency response as R_{dcA_ESR} is varied.

3.3 Interleaved Buck/Boost Converter (dcB)

The elementary building block of the converter is based on the typical PWM buck boost topology using two separate configurations of a half bridge - e.g S7, $\overline{D7}$ in buck mode and $\overline{S7}, D7$ in boost mode through a commonly shared inductor. Interpolating the currents of 3 half bridges with a symmetric, 120° offset increases the power density through parallel phase operation and allows some degree of ripple reduction and loss minimisation. It is shown in [69], that a maximum reduction of 27% in terms of capacitor current ripple is achievable through selection of the optimum phase angle between converters. This enables multiple benefits with no penalty to the design, such as the ability to reduce the size and weight of passive components such as filter inductors and capacitors as well as EMI emissions as described in [70]. From a robustness standpoint, higher numbers of phases were also considered as doing so would offer the added benefit of higher reliability through redundancy as the vehicle will still be able to operate at a reduced rating in order to return to be repaired; otherwise known as “limp home”.

The essential function of this converter is to control bidirectional current flow to charging and discharge the energy storage device. This is performed through cascaded voltage and current PI controllers in both directions. In Buck (charge) mode, the voltage across the ultracapacitor bank, V_{ES}, is regulated while the voltage of DC link, V_{DC} is controlled in boost (discharge) mode as illustrated in

Figure 3.7. Therefore, control of power flow is achieved by changing the references and feedback of the outer loop.

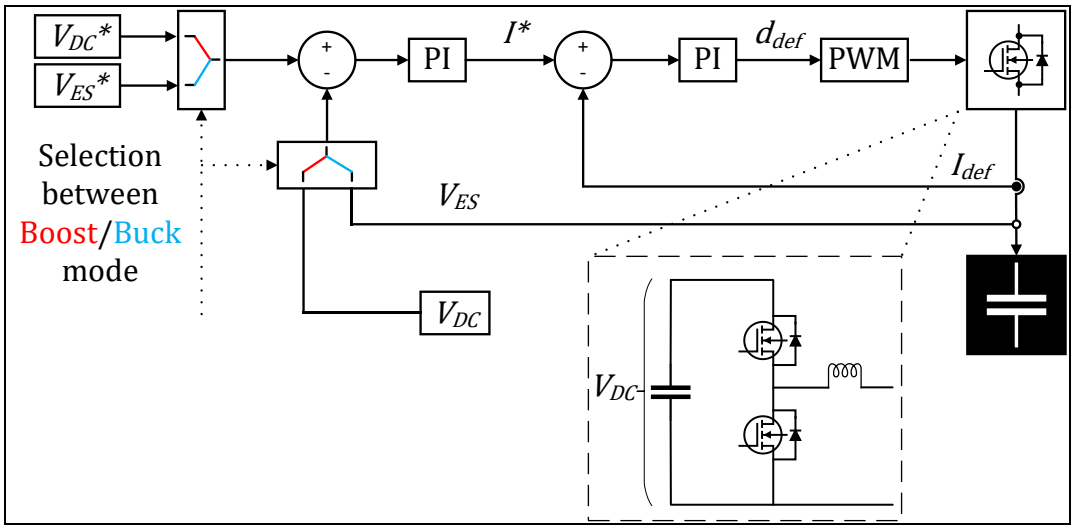

Figure 3.7: Interleaved Buck/Boost Converter (dcB) control algorithm structure in Boost (red) and Buck (blue) mode.

The input-output voltage relationship in continuous conduction mode [71] for buck and boost modes are provided are derived using the average switch model, derivations for which are provided in Appendix C. Therefore, the voltage gain of the interleaved buck/boost converter, $G_{dVdcdcB}$ in Buck mode:

$$G_{dVdcdcB\ (Buck)} = \frac{V_{ES}(s)}{d_p} = \frac{V_{DC}s}{s^2 L_{dcB}(C_{dcB} + C_{ES}) + s\frac{L_{dcB}}{R_{ESR}} + 1} \qquad (8)$$

and Boost mode:

$$G_{dVdcdcB\ (boost)} = \frac{V_{DC}(s)}{d_p}$$

$$= \frac{\frac{V_{ES}}{1-D}\left[1 - \frac{sL_{dcB}}{(1-D)^2 R_{dcB\_ESR}}\right]}{\left[\frac{s^2 L_{dcB} C_{DClink}}{(1-D)^2} + \frac{sL}{R_{dcB\_ESR}(1-D)^2} + 1\right]} \qquad (9)$$

are applied within the plant model of the converter, relating the values of Equivalent Series Resistance, ESR of dcB, R_{dcB_ESR}, inductance, L_{dcB}, output filter capacitance,

C_{dcB} and DC link capacitance, C_{dclink} with which the preliminary controller gains are first derived using classical control theory and later fine-tuned on vehicle.

Due to the use of ultracapacitors [72], $R_{dcB\_ESR} << R_{dcA\_ESR}$ thus $Z_{dcB} << Z_{dcA}$ therefore the effect of impedance variation during dcB operation is less of a concern. Instead, the key performance metric for dcB is the ability to achieve steady state control of the DC link voltage in less than 10ms to avoid delays in restarting the engine. Therefore, the converter is modelled in Boost mode, charging the DC link. During this mode of operation, the inverter is disabled, reducing the complexity in modelling the load components on the DC link. Referencing (9) as the transfer function of the plant, the open loop transfer function is calculated presented as $SysTF_{dcB}$:

$$\mathrm{SysTF_{dcB}} = \frac{K_{pdcB}s + K_{idcB}}{s} \left\{ \frac{\frac{V_{ES}}{1-D}\left[1 - \frac{sL}{(1-D)^2 R_{dcB\_ESR}}\right]}{\left[\frac{s^2 LC}{(1-D)^2} + \frac{sL}{R_{dcB\_ESR}(1-D)^2} + 1\right]} \right\}$$

where D is the duty cycle at the operating point and $K_{pdcB} = 0.6$ and $K_{idcB} = 0.006$ are the proportional and integral gains of the voltage controller respectively.

The initial behaviour of the circuit in dcB must be considered when designing the controller. For instance, when the ultracapacitor contactors are first engaged, current immediately begins to flow through the freewheeling diodes by means of passive rectification until the DC link voltage reaches equilibrium. This causes an interaction with the control loop so for clarity, the initial voltage rise in Figure 3.8 is ignored. Instead, the rise time is taken from 10% to 90% of the second voltage rise from 340V to 700V as indicated.

The two plots in Figure 3.8 illustrate the small signal model vs the complete component model results when controlled in closed loop with identical gains. The gains were obtained by firstly considering the requirement to achieve a critical or overdamped response (damping factor>1.0) and a rise time and steady state time of less than 50ms, translated from vehicle level requirements to avoid voltage overshoots to preserve converter component lifetime and achieve engine start within 0.5s respectively.

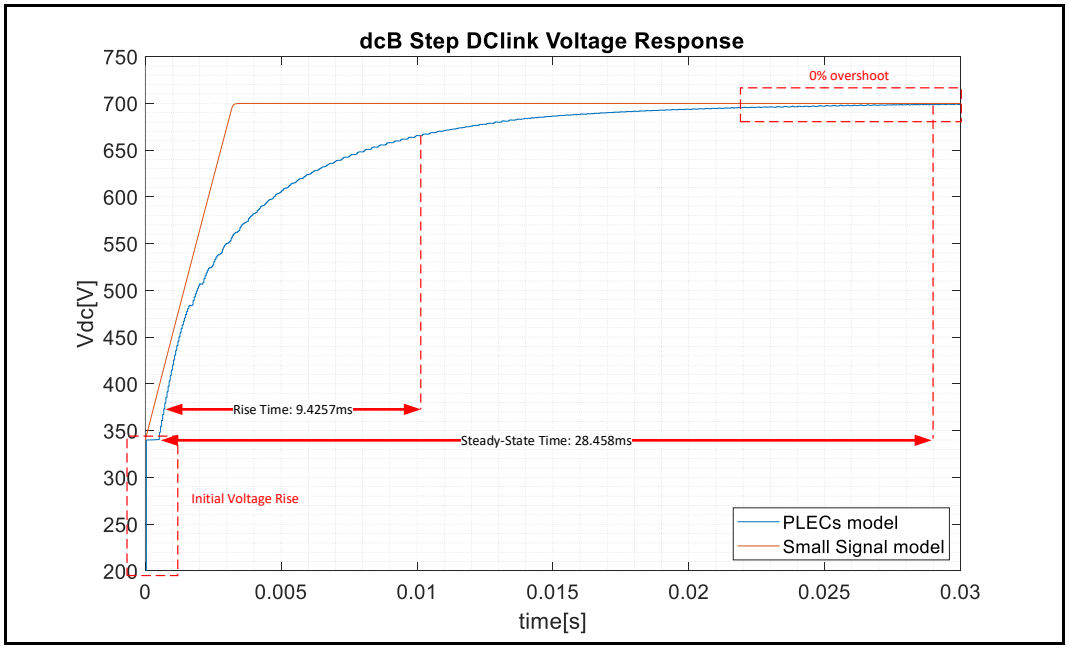

Figure 3.8: Interleaved Buck/Boost DC Converter (dcB) step response with optimized gains

The small signal model is used to obtain the initial gain settings and understanding of the preliminary behaviour of the converter components in isolation; giving us the blue plot in Figure 3.8. Once the complete model of the converter was built in PLECS, the gains are applied, and the second plot in orange is obtained. It can be observed that critical damping is preserved due to the absence of any overshoot. However, rise time significantly increased as a result. The discrepancies between the two plots are due to the following factors:

1) Hardware limitations. The small signal model has no consideration for maximum modulation index achievable due to the necessity to implement hardware deadtime protection. Also, in the complete model,

maximum device ratings are implemented within controller saturation limits.

2) Realistic behaviour of converter components. The small signal model operates on a fixed parameter set whereas the complete model more accurately encompasses dynamic behaviour of the components such as the aforementioned pre-charge of the DC link through rectification, the effect of switching behaviour and the need for filtering on the controller feedback, thermal interactions between energy storage- capacitors and inductors modelled.

Despite the discrepancies, the design requirements of 0% overshoot and 9.4257ms rise time and a time taken to achieve steady state of 28.458ms (below the threshold of 50ms) are met, providing a satisfactory starting point for further simulation work.

Chapter 4

Simultaneous System Characterisation and Optimisation

The design philosophy of the multiport converter is centred around modularity, where, a multi-bus architecture with the most commonly used bus voltages - 48V and 300V [73] on the vehicle battery and ultracapacitor terminals of dcA and dcB converter sections respectively share a common 800V DC link for bidirectional power flow. Aside from the core function of providing power transfer, the converter modules also share a physical aluminium housing and cooling plate which provides the advantage of power converter size and weight reduction. To truly harness the benefits of this approach, control schemes and algorithms must be developed that consider optimisations based on harmonics and loss reduction, taking into account the degrees of freedom permitted by the application. This requires that the interactions between each node on the shared bus are considered.

4.1 Optimisation Methodology

4.1.1 Multiple Objective Optimisation Problem Technique

The optimisation of the total operational efficiency, current harmonic content and capacitor ripple current of the multiport converter is the result of a trade-off between switching frequency of each converter in one hand, and the DC link voltage value in the other hand. Conventional optimisation methods with multi-criteria decision making suggest dividing multi-objective optimisations into multiple single-objective optimisations, by focusing on one optimisation at a time

[74]. Such methods may perform adequately well in preliminary capability studies but may be inaccurate when implemented in a real-world scenario as internal converter interactions are disregarded. Therefore, alternative techniques to effectively consider simultaneous optimisation of multiple incommensurable and contradicting objectives must be considered. Multiple multi-objective optimisation techniques are presented in [75] which consider the use of composite functions or move all but one objective into the constraint set. The former method has the drawback of complexity in the selection of the weights or the cost function and latter results in a single solution, rather than a set of solutions which decision-makers can utilise to examine the trade-offs in their design. Therefore, the Pareto optimal solution set is preferred to consider multiple solutions despite the inherent nature of the technique requiring a certain amount of sacrifice in achieving one objective to achieve a certain amount of gain in another.

In the most basic form, a general multiple objective optimisation problem may be expressed as:

$$\mathrm{Min}[f_1(x) \ldots f_N(x)]$$

$$\text{Subject to } x \in X$$

Where, the aim is to find a solution in the feasible set X that minimises the objective function comprising of f1(x),…,fN(x) illustrated graphically in Figure 4.1(A). Since simultaneous minimisation of these objective components cannot be done due to the often conflicting or opposing relationship of one function to another, there exists multiple optimal solutions for a single multi-objective problem. All these solutions may be optimal but offer different trade-offs among the objectives. The trade-offs are managed through using weights to balance the significance of the contribution of a certain objective within the optimal solution. Known as the Pareto optimal solutions, there are no solutions that achieve lower values for all objectives than the Pareto optimal solution. A set of all Pareto optimal solutions is called the Pareto front, or an optimal trade-off curve as depicted in Figure 4.1(B). One of the Pareto optimal solutions may be chosen depending on the

priorities of a certain application. However, it is less preferable to select an extreme solution that largely minimises one of the objectives but significantly degrades the others as such solutions deviate from the realistic behaviour of the system. Therefore, solutions with a balanced trade-off between objectives are sought.

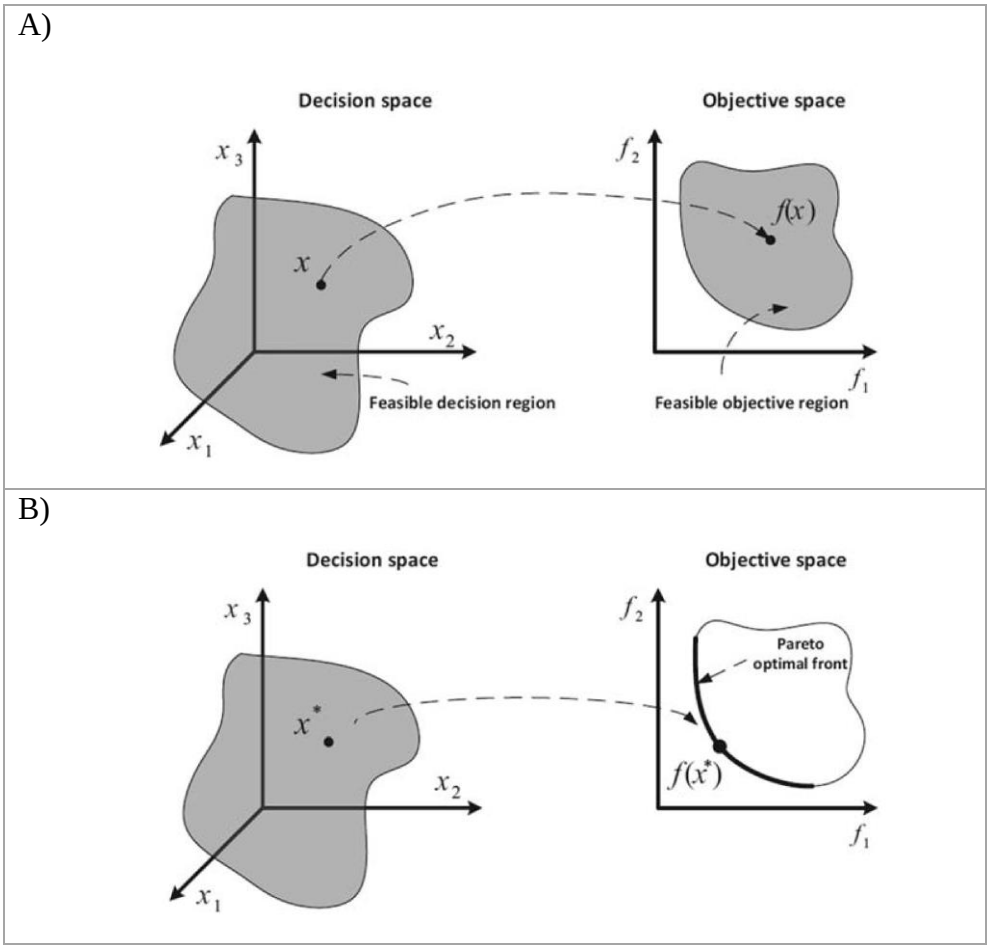

Figure 4.1: Pictorial representation of the objective functions within the solution space and objective function space (A). Definition of the Pareto optimal front (B) [76].

4.1.2 MOOP Application Example

Pareto optimality, is a measure of efficiency in multiobjective optimisation [77] where more than one conflicting objectives must be considered simultaneously. A design is considered Pareto optimal if there is no other design which improves the value of its objective criteria without deteriorating at least one other criterion [78].

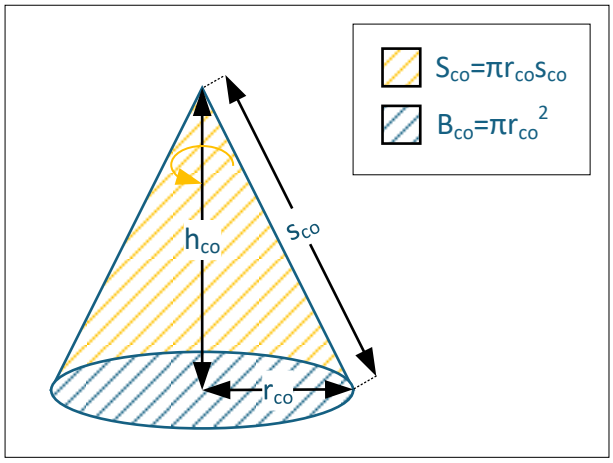

Figure 4.2. Example MOOP application on a right circular cone.

An example utilising a simple geometrical problem is now used to illustrate the application of MOO as shown in Figure 4.2. Given a problem definition of minimising both the lateral surface area, S_{co} and total surface area, T_{co} of a right circular cone of base radius r_{co}, height h_{co} and slant height s_{co}, subject to a minimum volume V_{co} constraint, we obtain the following relations shown in Table 4.

Table 4.
MOOP PARAMETERS

Input Variables	$r_{co} \in [0, 10]cm, h_{co} \in [0, 20]cm$
Optimisation Objectives	Minimise $S_{co} = \pi r_{co} s_{co}$ Minimise $T_{co} = S_{co} + B_{co}$ $= \pi r_{co}(r_{co} + s_{co})$
Constraint	$V_{co} > 200cm^3$

Next, the feasible points within the objective space are identified and collated so that the objective space may be mapped out, as shown as blue circles in Figure 4.3 (A). Here, points that do not meet the minimum volume constraint are marked in red. A closer look at the boundary (shown in Figure 4.3 (B)) between the feasible and unfeasible regions gives us the greatest minimisation of S_{co} and T_{co} as per the optimisation objectives. For clarity, this interface, also known as the Pareto Front is marked in green.

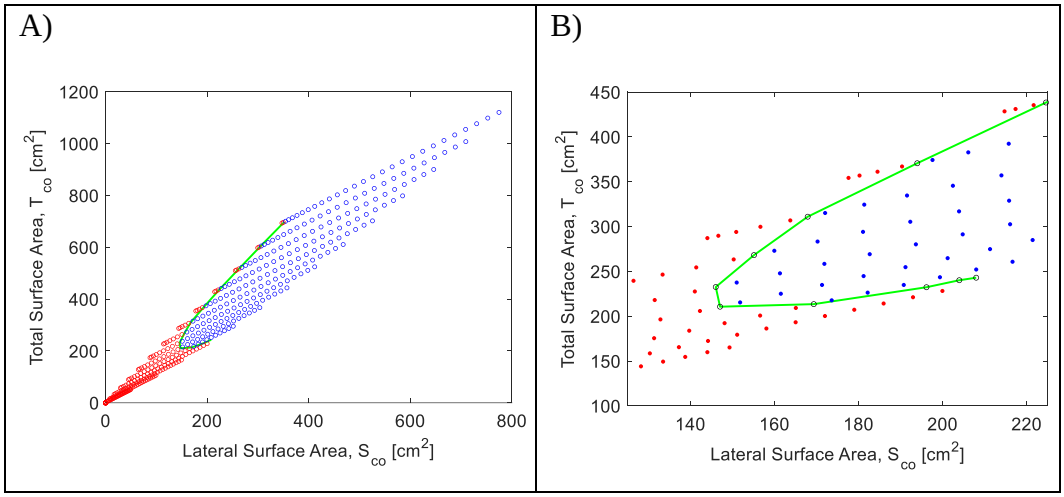

Figure 4.3. (A) MOOP Objective space encompassing the lateral and total surface area of a cone. Blue circles indicate the feasible region. Red circles denote vectors not satisfying the minimum volume constraint in Table 4 (B) Zoom on (A) illustrating the Pareto Front in green.

Many other optimization methods are well documented in literature such as the global criterion, the ε-constraint method [79] and the Multiple Objective Genetic Algorithm (MOGA) described in [78] which would each provide similar results for the optimization of the Multiport Converter. However, they each have drawbacks making application difficult and therefore out of consideration; global criterion method requires clear definition of desired goals and the high computational requirement needed by the ε-constraint method and MOGA.

4.2 Loss Estimation

When considering the efficiency of a power electronics converter, it is common practice to target the minimisation of losses. The losses may be divided into several categories - magnetic device core and winding losses, semiconductor switching and conduction losses as presented in [80]. Therefore, given efficiency is one of the optimisation objectives, it becomes evident that the Pareto optimal solution results will be highly influenced by the accuracy of the loss profile and calculations. Thus, a methodology is developed to comprehensively determine behaviour of the multiport converter design given device parameters and operating conditions.

The workflow as depicted in Figure 4.4, begins with parameterisation at component level. The switching behaviour of the MOSFET is reflected in the transitions of Drain-Source voltage and current, V_{DS} and I_{DS} respectively, over time as determined by its structural design, internal capacitances and the inner and outer resistances [26]. Next, power loss equations are applied to convert the device switching profiles into 3D parameter look-up reference tables considering operating conditions such as IGBT junction temperatures, for use within MATLAB/Simulink/PLECS system simulations.

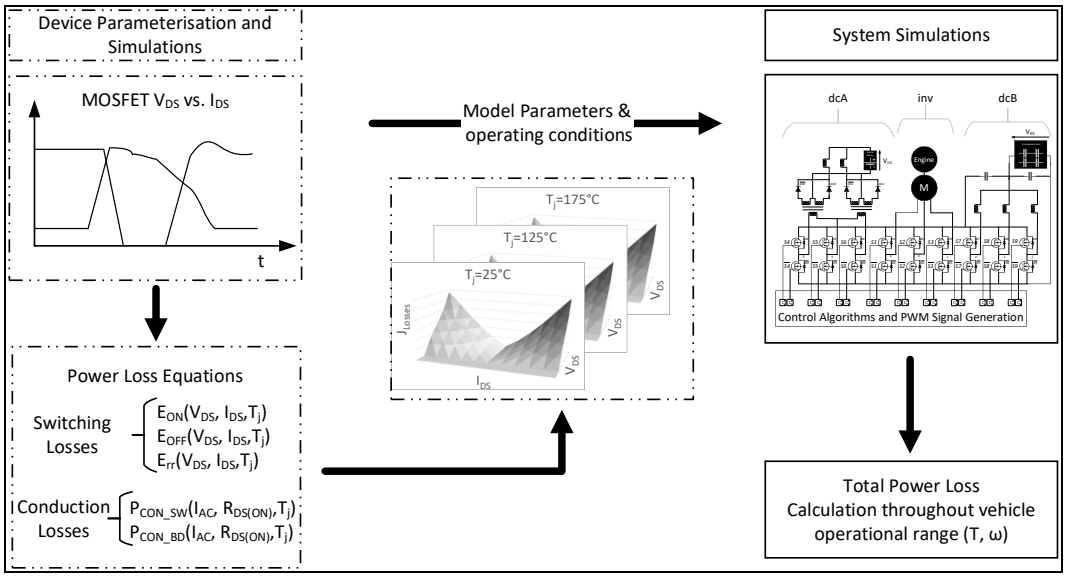

Figure 4.4: Multiport converter semiconductor loss calculation in MATLAB/SIMULINK.

Validation against both the industrial standard in-built loss calculation tools of PLECS and actual hardware test results (described in detail in Chapter 5.1) is carried out to increase confidence in the generated look-up tables. These workflow steps are then repeated for the freewheeling diodes, output rectifier diodes, DC link and filter capacitors and the magnetic devices such as the transformer in dcA and the output inductors of both DCDC converters.

The final detailed simulation model is presented in Figure 4.5, comprising the complete Multiport converter interfaced to a plant model is created using PLECs simulation tools for driveline level simulations considering vehicle level stimulus such as torque requests at a given speed.

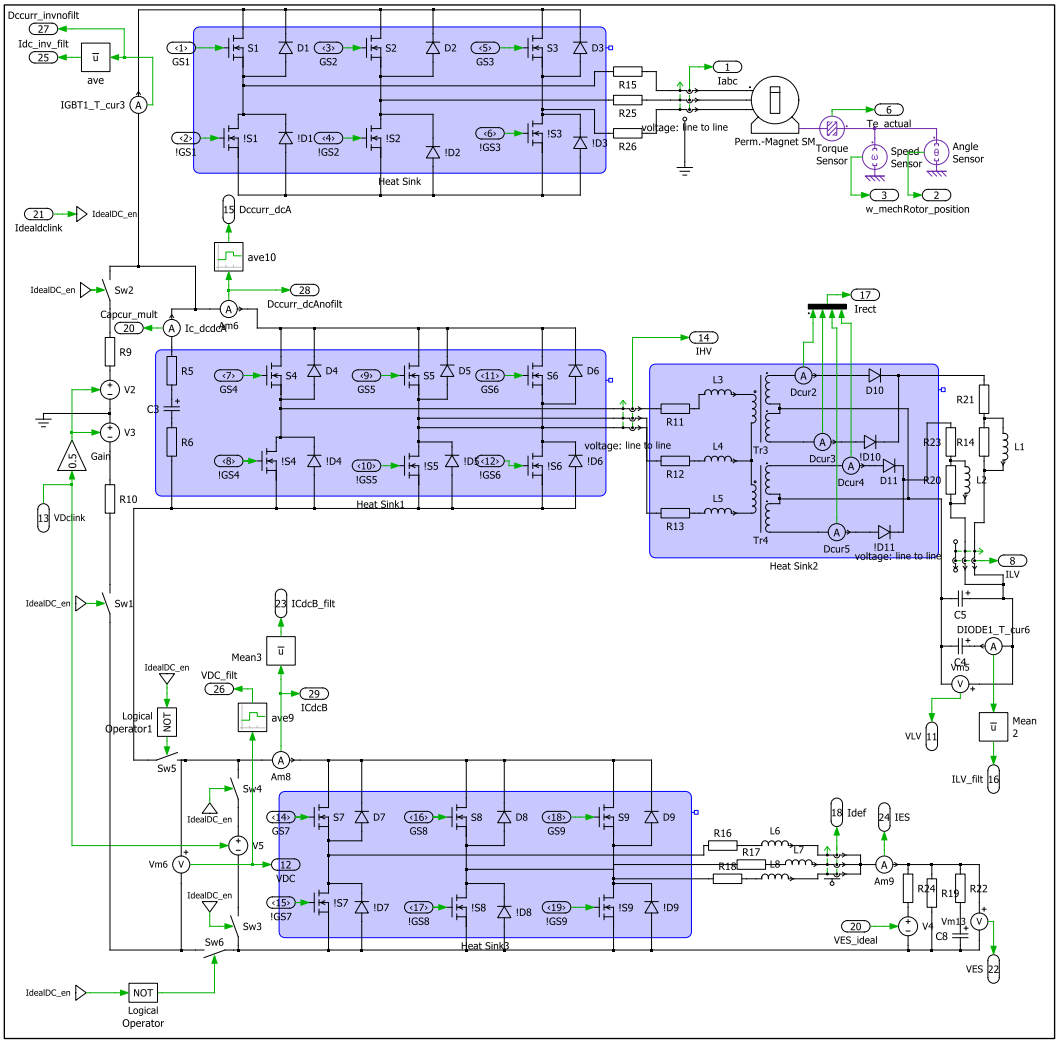

Figure 4.5. Component-level PLECs model implementation of the Multiport converter.

4.2.1 Conduction Losses

The Root Mean Squared (RMS) value of current through the switches is used when calculating conduction loss through the MOSFET. For simplification, a single half bridge of the inverter is analysed. In this case the complimentary pair, Sn and $\overline{Sn}$ will be considered where n represents switches 1-9 from Figure 3.1. Applying the very definition of RMS, the following relation is obtained:

$$I_{SnRMS} = \sqrt{\frac{1}{T_{AC}}\int_0^{T_{AC}} {I_{Sn}}^2(t)dt} = \sqrt{\frac{1}{T_{AC}}\int_0^{T_{AC}} {I_{AC}}^2(t)\, s(t)dt} \quad (10)$$

where s(t) represents the state of the MOSFET, s(t)=1 if switch is turned on and s(t)=0 if switch is turned off. $I_{AC}(t)$ is the instantaneous value of current with fundamental period T_{AC}. Integrating I_{AC} in (10) over the switching period, T_{SW} to remove harmonics at the multiples of switching frequency, the following relation is obtained:

$$I_{SnRMS} = \sqrt{\frac{1}{T_{AC}}\int_0^{T_{AC}} \left[\frac{1}{T_{SW}}\int_0^{T_{SW}} {I_{AC}}^2(t)\, s(t)dt\right] dt}$$

$$= \sqrt{\frac{1}{T_{AC}}\int_0^{T_{AC}} \left[{I_{AC}}^2(t)\frac{1}{T_{SW}}\int_0^{T_{SW}} s(t)dt\right] dt}$$

Given switching frequency is always much greater than the fundamental of current, $F_{SW}>>F_{AC}$, two assumptions are made:

1) I_{AC} is constant within switching cycle

2) $\overline{s} = d$

giving the RMS current flowing through the switch:

$$I_{SnRMS} = \sqrt{\frac{1}{T_{AC}}\int_0^{T_{AC}} \left[{I_{AC}}^2(t)d(t)\right] dt} \qquad (11)$$

Conduction loss of one main switch, $P_{Sncond} = (I_{SnRMS})^2 . R_{Dson}$

$$P_{Sncond} = \frac{1}{T_{AC}}\int_0^{T_{AC}} \left[{I_{AC}}^2(t).d(t)\right] dt. R_{DSon} \qquad (12)$$

The bottom switch $P_{\overline{Sncond}}$ is considered by replacing d in (12) with 1-d(t) giving:

$$P_{\overline{Sncond}} = \frac{1}{T_{AC}}\int_0^{T_{AC}} \left[{I_{AC}}^2(t).\left(1 - d(t)\right)\right] dt. R_{DSon} \qquad (13)$$

Equation (11) is also used to calculate freewheeling diode, D_n and body diode losses during ON state. Equation (12) and (13) are used to calculate losses of the 6 main switches in one fundamental period for each of the converter modules.

The values of conduction losses obtained from equations (12) and (13) are compared against results from PLECs simulations in Figure 4.6. The conduction loss profile is found to mimic the profile of phase current is expected. It is found that the discrepancy between the results of the two methodologies are minimised when more accurate values of R_{Dson} are used in equations (12) and (13). By including device junction temperature and drain source current dependencies-both of which are readily available in manufacturer documentation, as feedback to the conduction loss calculation, the correlation between temperature, resistance and resultant current flow is respected during simulation runtime leading to greater accuracy in results.

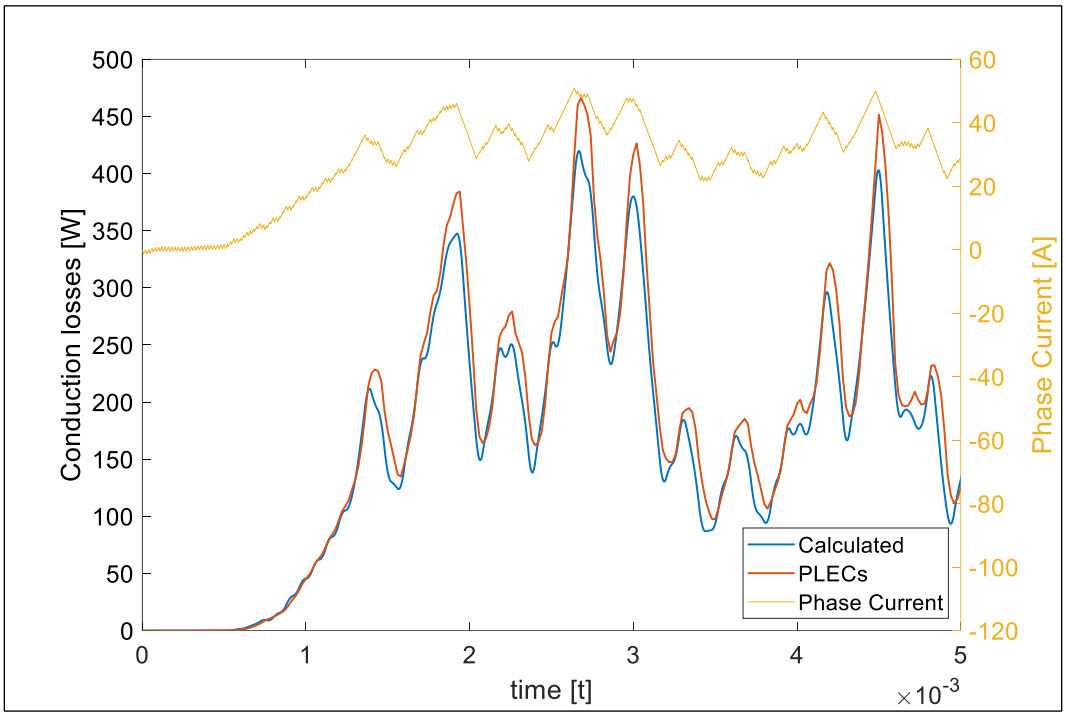

Figure 4.6. Comparison of conduction losses within dcB during Multiport converter Boost operation. Calculation method in blue, PLECs results in red, and converter phase current in yellow.

Validation of the conduction loss calculation algorithm is repeated for other operation points and finally integrated into the power loss equations used for power device parameterisation as discussed in Figure 4.4.

4.2.2 Switching Losses

The assumption is made that in a H-bridge, no matter the sign of the current, there is always one switch with turn on loss and one diode with reverse recovery due to the commutation of current from a freewheeling diode to the switch in its complementary pair. Similarly, the opposite is true for turn off- there is always 1 switch with turn off loss and one diode with turn on losses (negligible). Writing the commutation energy as a function of AC current and voltage across the H-bridge,

$$E = f(I_{AC}, V_{DC}) \qquad (14)$$

The equation for switching loss for a H-bridge during the positive cycle of current can be presented as:

$$P_{sw}(+) = F_{sw}.[E_{ON}(|I_{AC}(+)|) + E_{OFF}(|I_{AC}(+)|) + E_{RECOVERY}(|I_{AC}(+)|)]$$

$$\overline{P_{sw}}(+) = F_{sw}.\overline{[E_{ON}(|I_{AC}(+)|) + E_{OFF}(|I_{AC}(+)|) + E_{RECOVERY}(|I_{AC}(+)|)]} \qquad (15)$$

Assuming $\overline{P_{sw}}(+) = \overline{P_{sw}}(-)$,

the average switching losses across a half bridge for one complete cycle of current:

$$\overline{P_{sw}} = \overline{P_{sw}}(+) + \overline{P_{sw}}(-) \qquad (16)$$

Equation (16) is used to calculate losses of the 6 main switches in one fundamental period for each of the converter modules. To ensure accuracy of equations (14)-(16), the equations are compared to the equivalent loss calculation component

found in the component library within the PLECs software package. For comparison, this is presented in Figure 4.7.

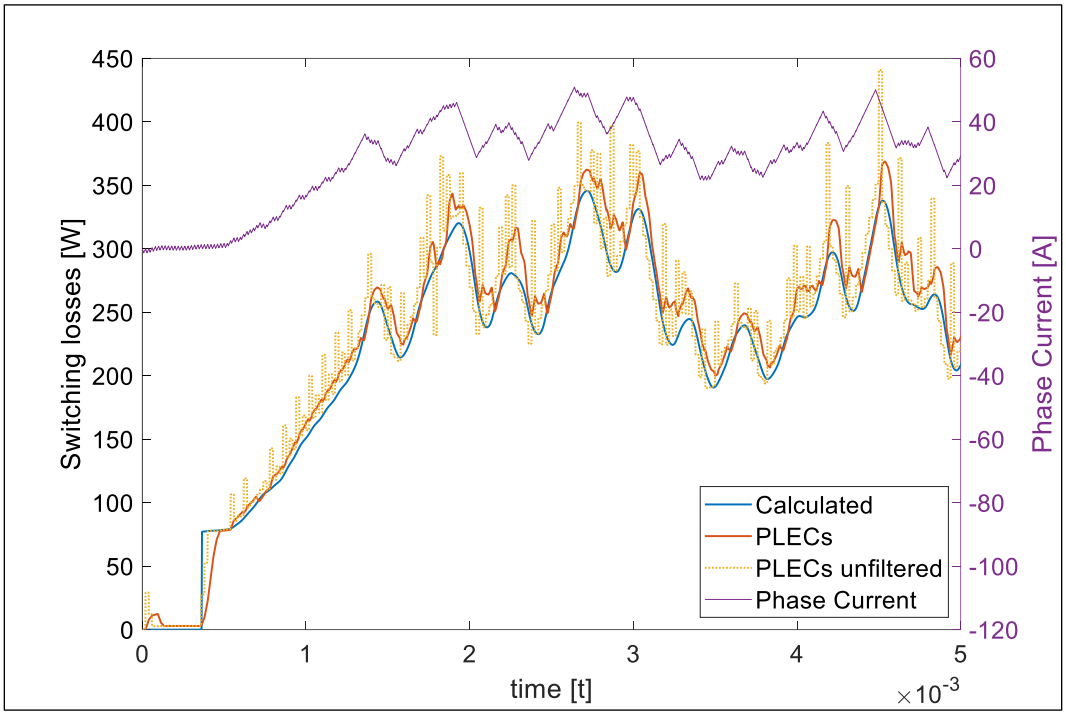

Figure 4.7. Comparison of switching losses within dcB during Multiport converter Boost operation. Calculation method in blue, PLECs results in red (with filter) and yellow (without filter).

As with conduction loss analysis in 4.2.1, the same overall profile of loss is presented by both the calculation and PLECs with some minor discrepancies as seen in Figure 4.7. These are attributed to filter attenuation and delays. The plot shows that the unfiltered PLECs result has a much faster initial rise time which is closer to the calculation method. The result however must be filtered to remove the effect of switching transients on efficiency results. Once reasonable confidence with switching losses calculation method is obtained, it is integrated into the overall multiport converter model as presented in Figure 4.4.

4.2.3 Magnetic Losses

As the highest load-bearing magnetic component in the multiport converter, the main power inductor of dcB is analysed to derive loss quantities. The plant model as described by equations (8) and (9) show that the inductance element is critical to the control behaviour and is therefore one of the main design elements for power transfer through the converter. This makes the understanding and the quantifying of the loss profile essential to inform the design of the inductor.

An analytical model is built based on classical inductor relationships where the losses were split into three components: DC winding loss, AC winding and total core loss (iron loss). A simulated current consisting of a DC and AC components is then applied to the model. The AC component consists of individual harmonics resulting from the geometric design of the airgap and winding of the inductor. An AC resistance, contributed by both the skin and proximity effect is found for each respective frequency of interest and is applied to the magnitude of the current harmonic. The equations used for these calculations are provided in equations (17) - (23).

Based on the work done in [81], the derived equation:

$$\delta = \sqrt{\frac{2\rho}{\omega\mu}} \tag{17}$$

is used to calculate skin depth, while:

$$R_{\frac{ac}{dc_\delta}} = \frac{C_w C_h}{C_w C_h - (C_w - 2\delta)(C_h - 2\delta)} \tag{18}$$

adapts this to a rectangular conductor cross section.

Dowell's equation taken from [82]:

$$R_{\frac{ac}{dc_{prox}}} = real(M_{IN}) + \left(N_{layers}{}^{2} - 1\right)\frac{Real(D_{IN})}{3} \quad (19)$$

is used to calculate the proximity effect in rectangular conductors through use of the following relations:

$$M_{IN} = \alpha C_h \coth(\alpha C_h) \quad (20)$$

$$D_{IN} = 2\alpha C_h \tanh(\alpha C_h) \quad (21)$$

$$\alpha = \sqrt{\frac{j\omega\mu_0\eta}{\rho}} \quad (22)$$

$$\eta = N_{layers}\frac{C_w}{SW} \quad (23)$$

Where, δ is the skin depth, ρ is the conductor material resistivity, ω is the angular frequency and μ is the conductor material permeability. R_{ac/dc_δ} is the ratio of AC resistance to DC resistance due to the skin effect, C_w is the conductor width and C_h is the conductor height. R_{ac/dc_prox} is the ratio of AC resistance to DC resistance due to the proximity effect, N_{layers} is the number of winding layers and SW is the slot width.

$$P_{core} = K_h f^{\alpha} B^{\beta} \quad (24)$$

The core losses are also dependent on frequency and therefore are calculated based on their respective harmonic components. For each frequency, the modified Steinmetz equation, (24) from [83] is used to calculate the losses from the flux density component using material data as provided by the manufacturer in [84], where P_{core} is the power loss per mass of the core, f is the frequency and B the flux density. K_h, α and β are constants supplied by the core manufacturer.

The analytical model study was validated against the 2D and 3D Finite Element Analysis (FEA). This required that all three models were ran with at the same operating point for an accurate comparison - depicted in Figure 4.7 and Figure 4.8 respectively. The results obtained from the 3 modelling techniques used are compared to gain an understanding of the robustness of the tools.

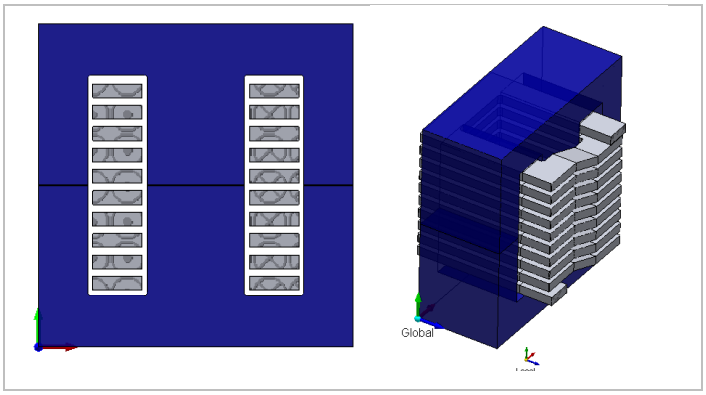

Figure 4.8: 2D and 3D FE Model of dcB inductor.

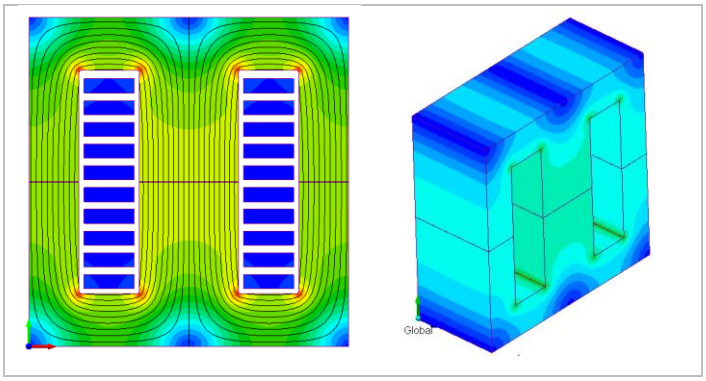

Figure 4.9: 2D and 3D FEA flux densities of dcB inductor.

The results of the analytical model study are compared with those from the numerical FE models and shown in Figure 4.8. Where, in Figure 4.10A, the inductance of the choke is compared as current increased to validate assumptions on how flux density is calculated.

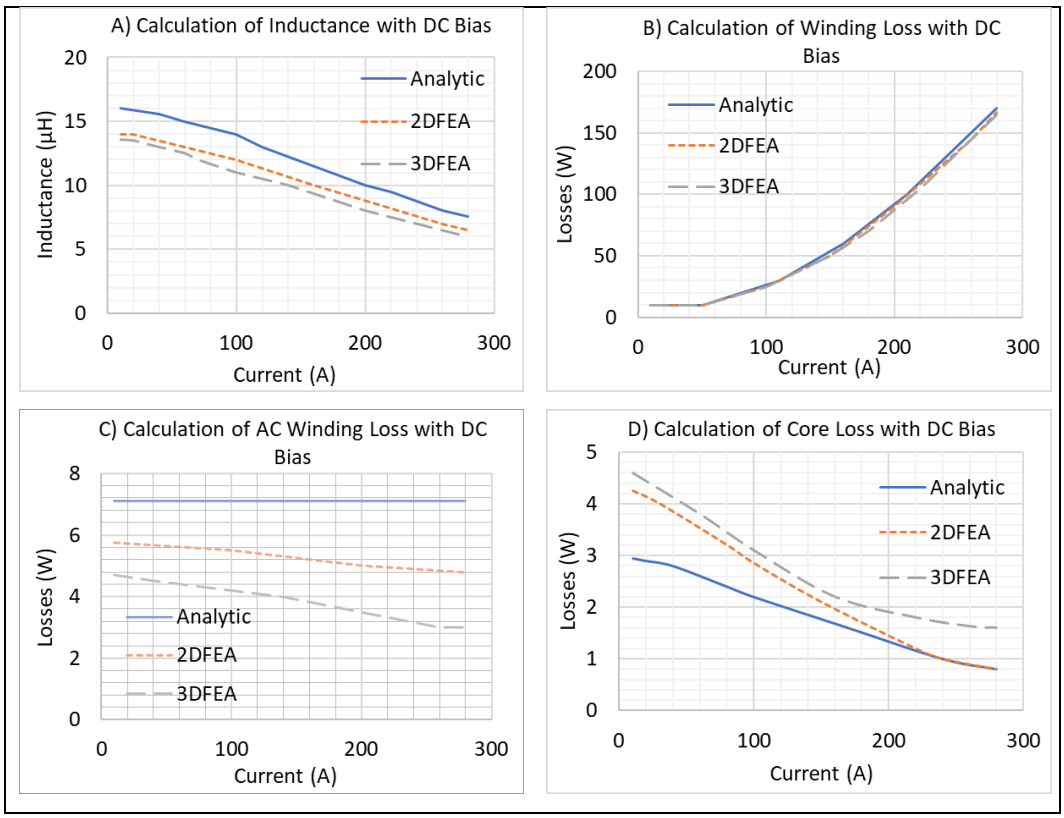

Figure 4.10: Comparison of results from Analytical, 2DFEA and 3DFEA for calculation of main inductance (A), DC winding loss (B), AC winding loss (C) and Core Loss (D)

The analytical model assumed an averaged uniform distribution of flux across the whole core. This is inaccurate as the 2D and 3D FEA results show much greater similarity to one another. On the other hand, the very nature of 2D assumes that there are no changes in flux density in the z axis (thickness of the core). While this assumption may be safely made without much impact to the accuracy of the model in most other cases, with this particular design, 3D FEA shows that there could be a change of up to 4% in the flux density of the core. Across the operating range, it is found that the analytical calculation shows a higher discrepancy to 3D FEA compared to 2D FEA at 23% and 6.1% respectively. In Figure 4.10B, the winding losses with increasing DC Bias current are shown. Here, a good correlation between all 3 methods is found where a maximum discrepancy of 4.7% is found at

280A. This is because winding losses are mainly dominated by DC losses which are calculated with similar techniques across all 3 methods. For this reason, Figure 4.10C is included to focus on the AC component of the losses. The method used to calculate the analytical AC losses are shown in (17) to (23) which do not consider the effect of DC bias and is known to provide a 'worst-case' overestimation and is therefore used as the control in this analysis. The averaging of the 2D FEA along the z-axis affects its accuracy as areas away from the core in application are at a much lower current density. Taking this into consideration, the 3D FEA result is taken to be the more accurate reference for comparison. At 280A, the analytical method shows 105% larger losses while 2D FEA losses are 47% larger. Core losses are presented in Figure 4.10D. The analytical and 2D FEA methods show that after a certain threshold, an increase in DC bias results in an almost linear decrease in core loss. Due to the increase in saturation, the core is becoming less sensitive to increasing AC load. Whereby, the increase of DC bias has resulted in a reduction of the B component in (24). Results obtained from 3D FEA show a similar trend but levelling off as DC biasing is increased and a higher overall core loss value.

The thermal performance of the proposed inductor design is evaluated through a Lumped Parameter Network (LPN). While more advanced methods are available such as thermal FEA, the LPN is sufficiently accurate for this particular use case [85], [86], [87]. A simplified model of this network is shown in Figure 4.11, and Table 5.

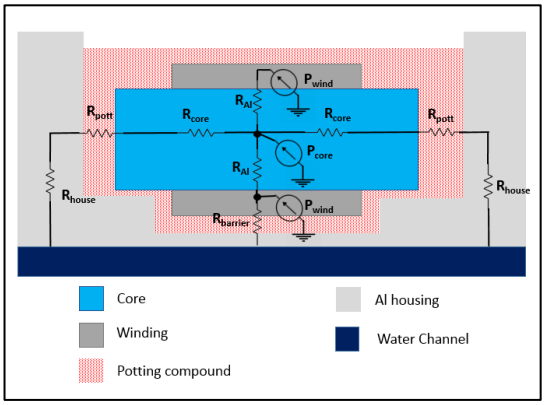

Figure 4.11: Simplified lumped parameter network.

Table 5.
THERMAL NETWORK PARAMETERS

Network Elements	Parameter representation
P_{core}	Core losses
P_{wind}	Winding losses
R_{core}	Core thermal resistance
R_{Al}	Winding thermal resistance
$R_{barrier}$	Core to base thermal resistance
R_{pott}	Potting material thermal interface
R_{house}	Housing thermal resistance

The inductor is impregnated in a moderate thermal conductivity potting compound within a water-cooled aluminium walled housing. Following the common approach for the design of inductors, the use of the potting compound adds thermal pathways, thermal mass and mechanical strength to the component [87]. The thermal compound selected was Robnor Resins PX439XS with a stated thermal conductivity of 1.3W/mK and a maximum operating temperature of 200˚C making it a suitable candidate for the operating envelope the inductor was intended for.

Experimental validation was carried out by building two inductor prototypes, Design 1 and Design 2, within fully functional multiport converter units to confirm the accuracy and robustness of the models. The initial inductor prototype, Design 1 as pictured in Figure 4.12 clearly shows the traditional approach of inductor design- a C-shaped amorphous core to handle high DC flux densities and thin foil conductors to minimise AC copper losses. As this design is bulky, it was only tested with the functional prototype converter which was not confined to an enclosure. This provided easy access to the device to mount measurement instruments for validation of design.

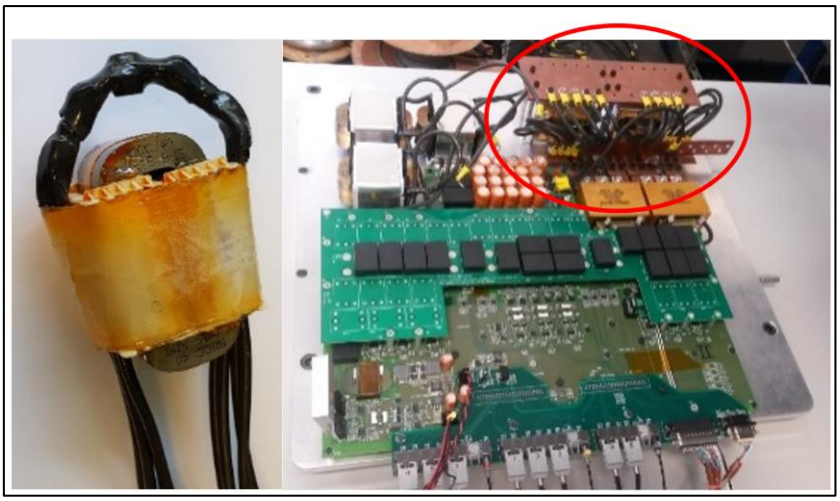

Figure 4.12. Inductor Design 1 separate (left), tested within functional prototype multiport converter (right).

The test methodology was divided in two. A low current test, specifically used for validating inductor and transformer designs as described in [88] is used to verify inductance and loss values were as expected. The second method was to validate the inductor design within a multiport converter prototype and operating within a realistic environment.

For clarity in comparison, experimental results are superimposed over plots from Figure 4.10. Figure 4.13(A) repeats the plot of Figure 4.10(A) with the addition of measured inductance.

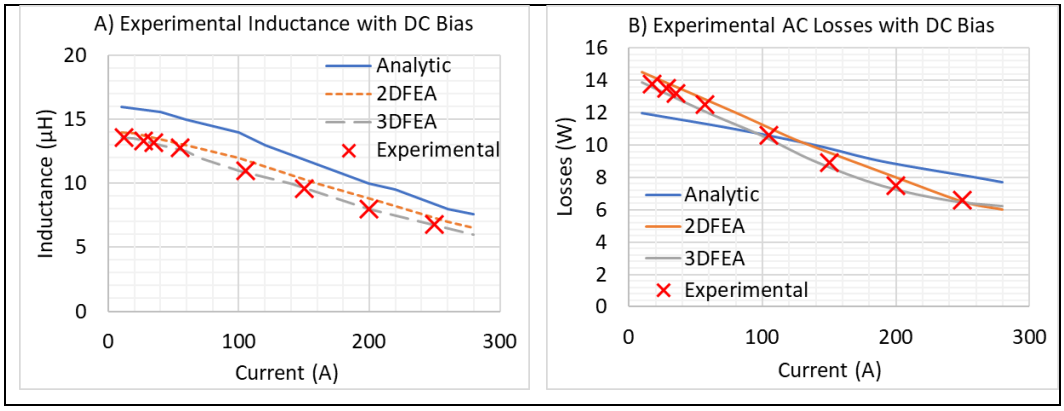

Figure 4.13: Experimentally measured inductance of Design 2 and AC losses as current is increased.

For reasons previously discussed, the measured data aligns very closely with the 3D FEA. Due to assumptions made in 2D FEA, the results are overestimated but this discrepancy is negligible and may be corrected through use of a small offset-type correction factor. Given the inconsistent discrepancy of the measured values to analytical results, this shows that the analytical model can only be used as a preliminary sizing tool, when accuracy of the results is not critical.

Loss values obtained experimentally are a sum total which may be broken down into individual AC and DC derived components. DC winding losses are easily calculated for a given temperature knowing the material properties, and can therefore be mathematically subtracted, thus leaving only the AC winding and core losses to consider, as proposed by [89]. For comparison between experimental and calculated results, the AC loss values in Figure 4.10B and C are summed and plotted against the measured values obtained through testing in Figure 4.13B. As can be observed, there is excellent similarity achieved between the experimental results and 3D FEA model. As with inductance the 2D FEA tool overestimates the AC losses as a result of a compounded error by initially overestimating the AC winding and core loss, illustrated by Figure 4.10(C) and (D) respectively.

The analytical model presents a completely different profile of losses when compared to experimental, 2D and 3D FEA results. At low values of DC bias, core losses are significantly lower as flux density is averaged through the geometry of the core. As DC bias increases, the analytical model losses decrease slowest, resulting in higher values at the end of the current range. This because the analytical model does not effectively take into account the decreasing AC winding losses as DC bias is increased.

In summary, this indicates limitations in the analytical mode, i.e, low accuracy at higher currents and corrective measures that may be used when using 2D FEA. This is however quite adequately compensated for by the highly accurate 3D FEA method. Apart from challenges faced with the tool, the results obtained confirms the significant performance improvements that the inductor design methodology brings compared to traditional designs. The results of experimental testing and the FEA tools were used to fine-tune the design- final inductor design parameters of Design 1 and Design 2 are presented in the Appendix D.

Using material properties, thermal simulations were ran over 10 drive cycles. As illustrated in Figure 4.14, the temperature stays below the maximum operating temperature of the core and potting compound proving that temperature is not the limiting factor when considering the minimization of inductor Design 2.

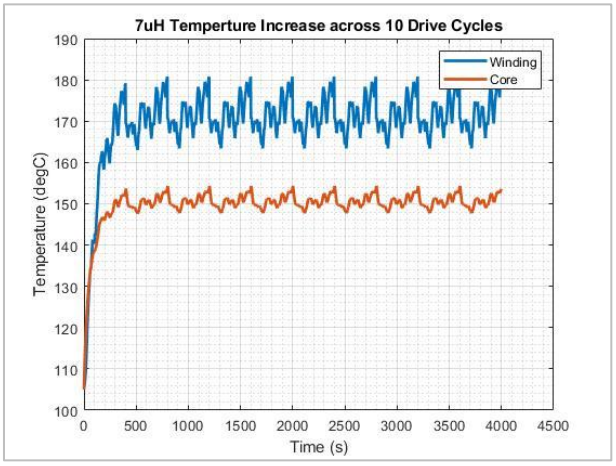

Figure 4.14: Simulation of dcB Inductor temperature across 10 drive cycles.

4.2.4 Performance Simulation Sweep

A loss calculation model (pictured in Figure 4.15) comprising magnetic core loss-(24), capacitive, power module conduction (red box) (12), (13) and switching losses (14) from preceding Chapters 4.2.1 to 4.2.3 is are integrated into a transient Simulink model in order to perform a parameter sweep study.

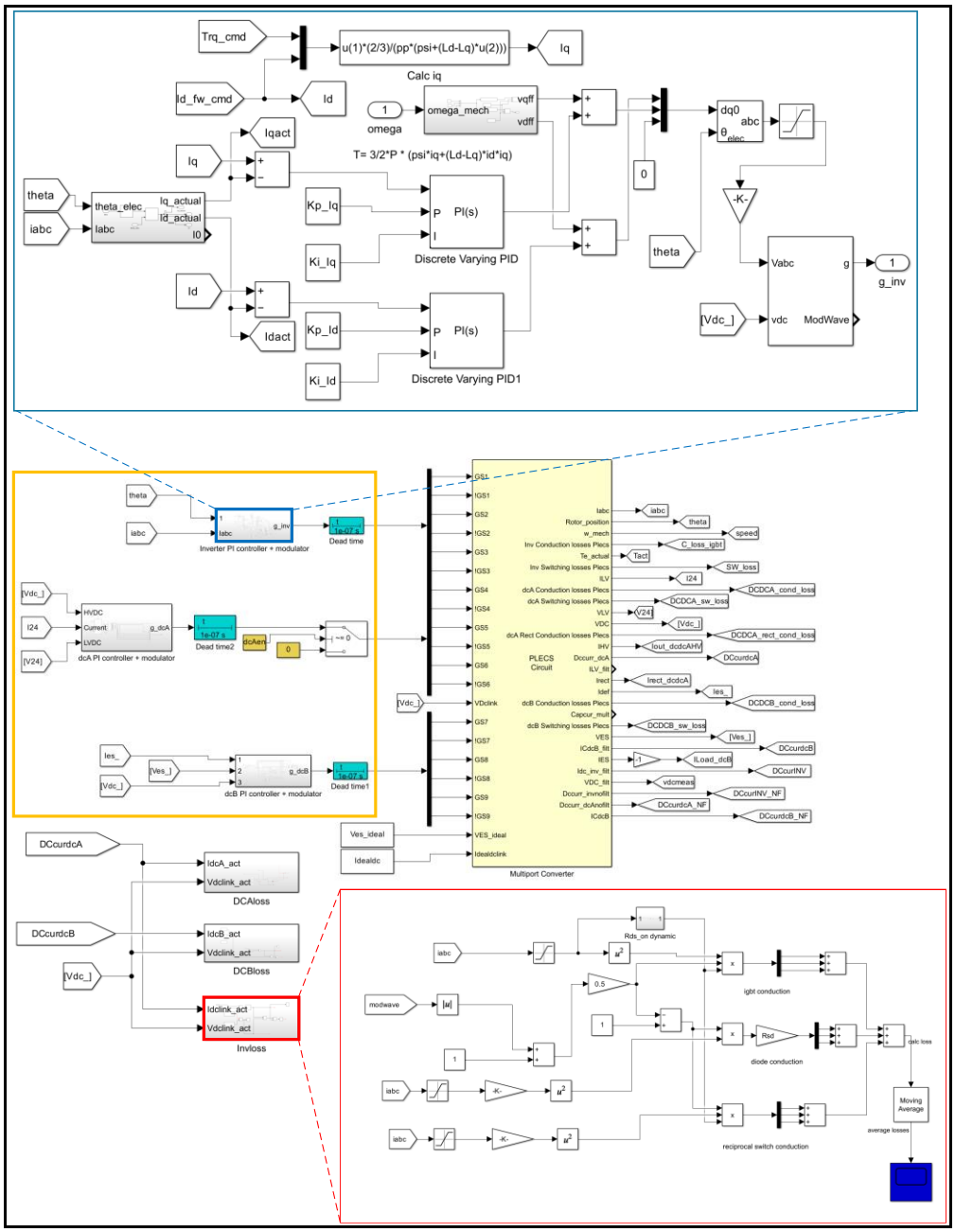

Figure 4.15. Loss calculation model of multiport converter. Refer to Figure 4.5 for PLECs circuit of Multiport Converter.

The objective of simulation sweeps was to investigate the behaviour of several key aspects of multiport converter performance during simultaneous operation. As elaborated in the introduction, converter power density and cost are universally used as benchmark criteria. Given their direct correlation, converter total efficiency, sys_{eff} , phase current ripple, quantified through Total Harmonic Distortion (THD), and DC link capacitor current, I_{DCrms} are selected as optimisation parameters.

Considering the multiport converter in the automotive application, the inverter operational point in terms of i_d and i_q reference values provided by the MTPA curve is of paramount importance to the function of the vehicle. This limits the degrees of freedom to the switching frequency of each of the converter modules- dcA switching frequency $F_{SW,dcA}$, dcB switching frequency $F_{SW,dcB}$, Inverter switching frequency $F_{SW,inv}$ and the DC link voltage, V_{DC}. Stating the optimisation parameters considering the degrees of freedom the following optimisation objectives are obtained:

$$sys_{eff} = f(F_{SW,dcA}, F_{SW,dcB}, F_{SW,inv}, V_{DC}) \quad (25)$$

$$THD = f(F_{SW,dcA}, F_{SW,dcB}, F_{SW,inv}, V_{DC}) \quad (26)$$

$$I_{DCrms} = f(F_{SW,dcA}, F_{SW,dcB}, F_{SW,inv}, V_{DC}) \quad (27)$$

Inputs to the functions, $F_{SW,dcA,}$ $F_{SW,dcB,}$ $F_{SW,inv}$ and V_{DC} are configured in the 'PI controller+Modulator' subsystems marked by the yellow box in Figure 4.15 for a given speed and torque point on the PMSM. The respective converter modules are then simulated concurrently with fixed reference voltage and torque values for the PI controllers- the inverter PI controller implementation is shown in the blue box. The outputs were calculated by passing model data to postprocessing scripts to calculate system efficiency, sys_{eff}, phase current total harmonic distortion, THD and DC link current, I_{DCrms} as per equations (25), (26) and (27) respectively. Setting the multiport converter input and output power as P_{total_in} and P_{total_out} respectively, system efficiency is defined as $P_{total\_out}/P_{total\_in} = (P_{total\_in}+P_{loss})/P_{total\_in}$, where P_{loss} represents the sum of the conduction, switching

and magnetic. THD and I_{DCrms} were calculated directly from the simulation model PMSM phase current and converter DC link current directly.

The weighted sum method is used to compile the contributions of optimisation objectives within a cost function for solving the MOOP [90]. The cost function where g is the optimum output can therefore be derived as:

$$g = w_1\, sys_{eff} + w_2 THD + w_3 I_{DCrms}$$

where $w_{1\text{-}3}$ represent the weight coefficients as described in [91]. The weights are assigned depending on the importance of the optimisation parameter in minimising g; which can also incorporate additional factors important to the performance of the system.

Considering the use case of the multiport converter within an electrified vehicle, both driving and energy recovery modes involve energy transfer and therefore setting the efficiency, sys_{eff} of the electric drive system as a critical performance criteria. This provides the first dimension in the optimisation process with its importance reflected in the setting of w_1. However, drive optimisation is rarely a one-dimensional improvement effort. Other factors such as driveability and component reliability must also be evaluated and refined for acceptance within the automotive space. The subject of Noise, Vibration and Harshness (NVH) [92] is a key factor when considering vehicle drivability. The use of PWM causes current harmonics which in turn create harmonic components of electromagnetic force resulting in noise and vibration within the PMSM as described in [93]. Harmonic content on PMSM phase current, measured as percentage Total Harmonic Distortion (THD) is therefore integrated in the cost function with w_2.

Finally, w_3 is assigned to the reduction of the RMS value of DC link capacitor current. The shared DC link design implies a greater dependency on reliability of the capacitor array. A review of capacitor failure modes presented [52] lists capacitor current stress as one of the critical stressors affecting failure and lifetime of the three dominant capacitor technologies, Al, MPPF and MLCC. This makes the reduction of DC link current highly beneficial to increase lifetime of the device and therefore achieve higher levels of robustness and reliability.

System Efficiency

When considering the system efficiency optimisation objective given in equation (25), the initial step in configuring the simulation sweep is to determine the range of optimisation parameters, V_{DC} and F_{SW} are realistic and within the operational limits. Taking for instance the DC link voltage value in this design, the maximum tolerable voltage on the DC link was set by the hardware limitation of the capacitor array. The minimum on the other hand was determined through consideration of the voltage limit curve to achieve continuous torque rating on the inverter-PMSM and the voltage conversion ratio capability of the DCDC converters. The maximum and minimum boundaries established as listed in Table 6, the results of the simulation sweeps.

Table 6
MAX/MIN VALUES FOR SIMULATION SWEEP

Parameter	Unit	Minimum	Maximum
V_{DClink}	V	525	900
I_a, I_b, I_c, I_d, I_e, I_f	A	0.0	75.0
$F_{SW,inv}$	kHz	1.0	50.0
$F_{SW,dcA}$	kHz	12.5	100.0
$F_{SW,dcB}$	kHz	12.5	100.0

The resultant multiport efficiency results shown in Figure 4.16(A)-(C), are considered to extract the V_{DC} and F_{SW} range for each converter resulting in the maximum multiport converter efficiency. All converter components show an inversely proportional relationship between total efficiency and the optimisation parameters due to increasing switching and conduction losses with the exception that the efficiency profiles of the inverter and dcB, Figure 4.16A and C respectively show limited loss savings below V_{DC} = 550V and $F_{SW,dcB}$ = 25kHz.

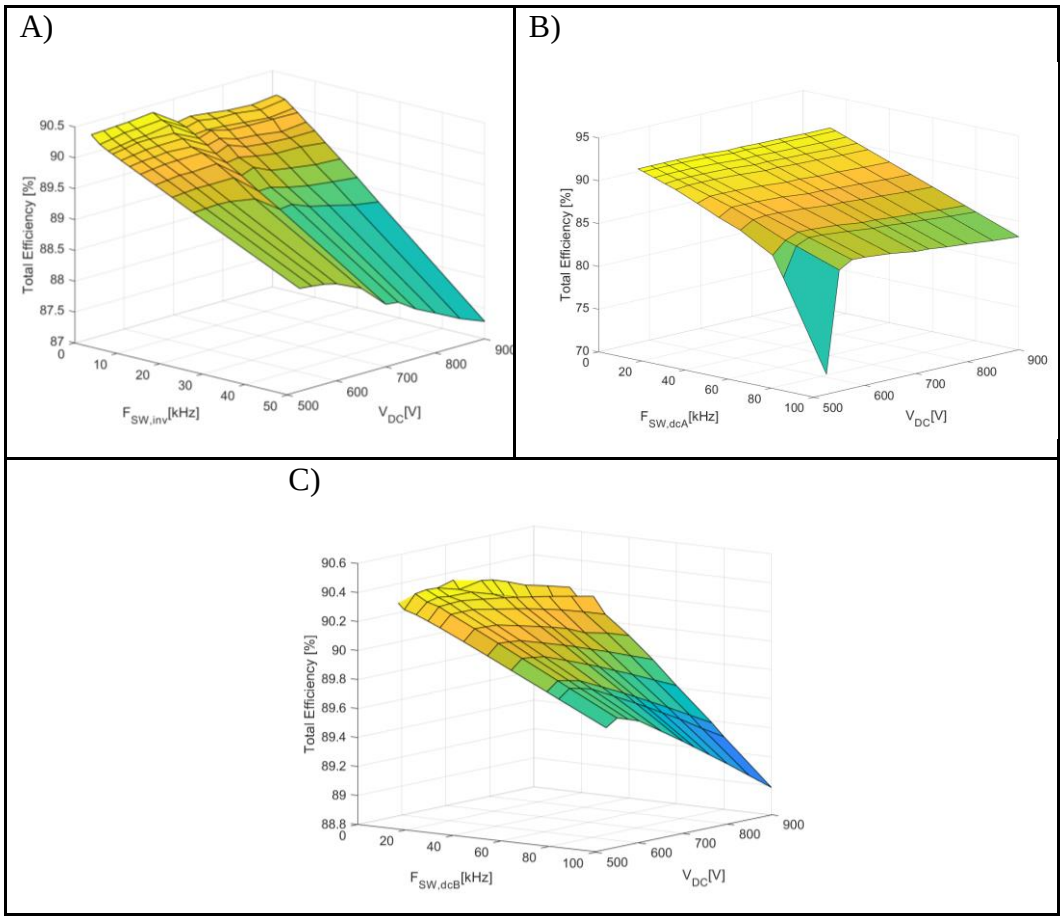

Figure 4.16: Total multiport converter efficiency when DC link voltage and (A) Inverter, (B) dcA and (C) dcB switching frequency is varied.

Comparing the results of all three converters within a sensitivity analysis, it is apparent that dcA shows the highest sensitivity to switching frequency variation despite the power rating of dcA being a third of dcB resulting in a lower HS current amplitude. This is due to the additional losses from the commutation and conduction of the rectifier stage diodes, connected to the LS of the isolation

transformer. This necessitates that $F_{SW,dcA}$ is kept to the minimum value of 12.5kHz to maximise resulting efficiency.

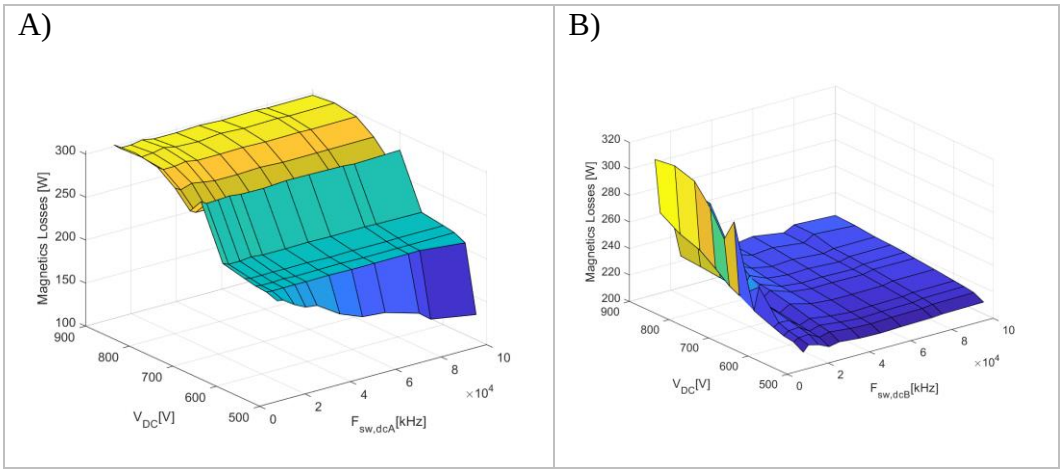

Figure 4.17: Magnetic component losses as DC link voltage and switching frequency is varied in (A) dcA and (B) dcB.

To estimate the magnetic losses within the multiport converter, the sum total of DC and AC winding losses, and core losses are calculated for all magnetic components- inductors and isolation transformers based on parameters extracted from validation activities in a laboratory environment (Figure 4.13). Results from simulation for dcA and dcB are illustrated in Figure 4.17A and B respectively where it can be observed that the losses increase with V_{DC} but display a flat profile at switching frequencies between 25kHz and 100kHz. As discussed in Chapter 4.2.3, inductor losses are a combination of DC and AC copper losses and core losses. Inductor design procedure reduces the number of turns with increasing frequency in order to achieve a minimum of total losses by means of balanced copper and core losses. Performance analysis of high frequency inductors presented in [94] showed a similar "flat behaviour" of losses vs frequency where effective core utilisation was already achieved, at the same time flux densities were close to saturation; making the ferrite material capability the limiting factor to further loss reduction.

Total Harmonic Distortion

While it may be desirable to reduce switching frequency for optimisation of sys_{eff}, the resultant increase on harmonic content must be considered. It is critical to avoid additional losses, torque ripple and electronics noise [95] resulting from additional harmonics when considering the space and cooling constraints on automotive drivetrains. It is expected that the main contributors to harmonics in this application are due to:

1) The switching action of the MOSFETs, located near the inverter switching frequency and its multiples.

2) The third, fifth and seventh multiples of the machine fundamental frequency.

The simulation model is swept for the cumulative THD content on inverter phase current. As expected, THD % is inversely proportional to V_{DC} and $F_{SW,inv}$ where it is observed in Figure 4.18 that THD content increases up to 8 times as V_{DC} and $F_{SW,inv}$ are reduced to the minimum levels preferred by the efficiency study.

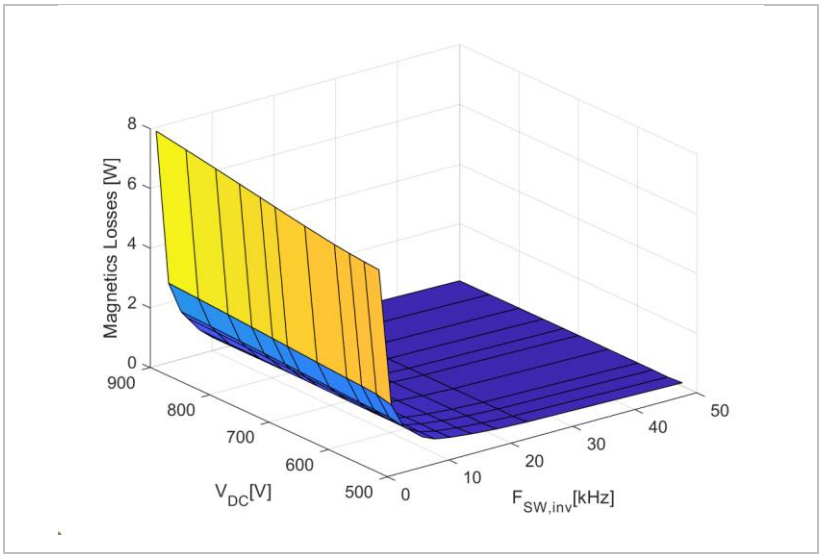

Figure 4.18: THD [%] content on inverter phase current as DC link voltage and inverter switching frequency is varied.

DC Link Losses

Losses within the DC link capacitor are investigated as part of the optimisation function given by equation (27). Harmonic current components and the equivalent series resistance (ESR) represent power loss in the converter as heat. With knowledge of the thermal impedance of the capacitor and ambient temperature, the overall hotspot temperature can be determined. This information is critical to the design of the converter as described in [52], the main stressors for capacitors are represented by the voltage, the temperature and the humidity. A common lifetime model for capacitors can be expressed as:

$$L = L_0 \left(\frac{V}{V_0}\right)^{-n} e^{\left(\frac{E_a}{k_B}\right)\left(\frac{1}{T}-\frac{1}{T_0}\right)}$$

where L and L_0 are the lifetime under the operational conditions and testing conditions (usually given by the manufacturer), respectively. The temperatures T and T_0 are defined in the same manner. k_B is the Boltzmann's constant. The activation energy E_a and the exponent n are specific for the capacitor type. For aluminum electrolytic capacitors n is about 3 to 5 and E_a is 0.94 eV.

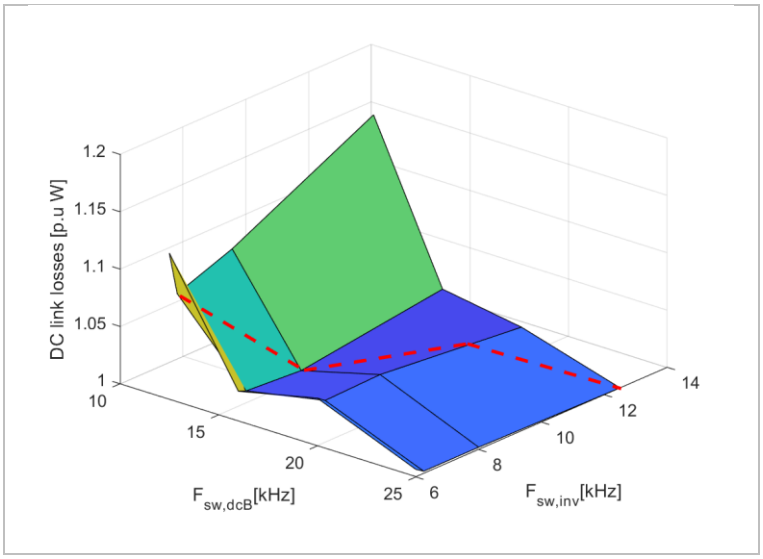

Figure 4.19: Per Unit (p.u.) DC link capacitor losses- calculated on base value: 70.77W as $F_{SW,inv}$ and $F_{SW,dcB}$ are varied.

The simulation model is swept for a fixed operational load point, 400Nm and 300RPM to ensure results obtained are directly a result from variation of

optimized parameters $F_{SW,inv}$ and $F_{SW,dcB}$. Besides the expected trend for losses to reduce with the increasing switching frequency due to reduced ripple amplitude resulting in lower $I_{C,RMS}$, it is clearly observable that the minimum per unit losses are obtained when the ratio of 2:1 is kept between $F_{SW,inv}$ and $F_{SW,dcB}$ as shown with the dotted red line in Figure 4.19. As dcA has been neglected in this simulation, inv and dcB have met the minimum requirement for Phase Displacement (PD), a loss reduction technique presented in [69]. This topic is further expanded upon in Chapter 4.3.2 where further loss reduction is possible through use of an optimum phase displacement angle. Although loss reduction is possible through application of the PD technique, its contribution to the final system efficiency improvement will be evaluated against other optimization techniques using Pareto tools to obtain the optimum outcome.

4.3 Optimisations

4.3.1 Phase Deactivation

The main characteristics sought after in automotive DC converters are efficiency modularity, reliability and fault tolerance [96]. As such, multiphase converters with phase interleaving provide advantages compared to other topologies. Parallel switching cells provide higher current capability and if carrier phase shifting is applied, input and output ripple decrease, reducing the hardware ratings of filters and power transfer inductors. Considering the multiple cells switching in parallel, some of them could be disconnected to improve efficiency when load demand is low. This may be achieved by activating or deactivating phases dynamically as a function of load current. For simplicity, each phase is assumed to be symmetric and therefore load current is distributed uniformly across each phase. This means that all phases share equal load and therefore have the same amount of losses. Therefore, assuming power losses in the input and output filter are low, the efficiency of the converter with all phases active will be the same as the efficiency of a single phase for the same amount of current as given in (28).

$$\eta\left(\frac{I}{M}\right) = \sum_{1}^{M} \eta(I) \tag{28}$$

Where η is converter efficiency, I is the load current and M is the number of phases.

Considering the majority of converters are design for peak efficiency at nominal power, the number of active phases may be selected at runtime based on the level of load current in order to consistently place the converter in its peak efficiency window.

In Figure 4.20, efficiency is represented versus normalized load current. In this particular example of a 4-phase multiport converter, it is shown that it is most efficient to operate a single phase during operation between 0-25% of rated load. The same is shown for two phases at 25-50% load, three phases at 50-75% load and four phases at 75-100% load. Tracing the peak efficiency of all four load ranges, the new efficiency curve provided when the optimal number of phases is selected is obtained as illustrated by the dotted line in Figure 4.20.

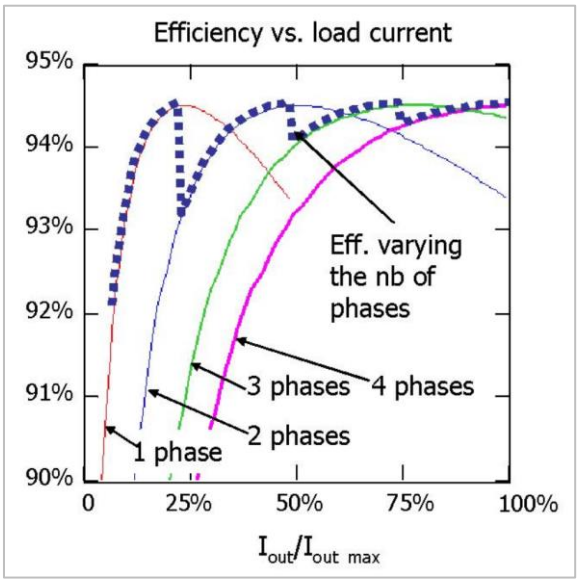

Figure 4.20: Multiphase converter efficiency for variation in the number of active phases [97].

While this simple methodology has been proven to provide some efficiency improvements at light load, the operating conditions of the remaining phases must be considered at load points at the deactivation threshold and higher towards maximum load for further efficiency gains. The effect of partial operation on the magnetic components must also be considered carefully when approaching higher values of power. FE (Finite Element) analysis supported by practical experimental work in presented in [98] showed the effect of partial saturation of a shared magnetic core leading to unsymmetrical flux distribution and lower maximum flux between the remaining active legs of the converter. This challenge may be resolved through either interleaving active and inactive phases on a shared magnetic core,

keeping ac and dc fluxes below saturation level of the core material or complete physical separation of the magnetic core - operating an isolated core per phase.

For obvious reasons, this methodology is only applicable to the DCDC components of the multiport converter. When considering the rated load capabilities of dcB is more than 3x that of dcA, the maximum benefit of this optimization may be obtained through load-based activation of the interleaved phases of dcB. The variable load will be determined by the torque requirement on the inverter as dcA operates at a fixed load when in operation. Therefore, taking the sum of the load applied by the inverter and dcA gives us the range of current dcB will have to supply in boost mode.

The efficiency of dcB in 3 Phase and 2 Phase operation is compared for the entire DC link voltage range of 550 to 900V through simulation and the results are presented in Figure 4.21. The rated current of 75A per phase is used as the base value for the per unit (p.u.) representation. For low values of power - product of dcB current and DC link voltage, it is shown that 2 Phase operation results in higher efficiency while the opposite is true for values of current above 0.5 p.u.. The transition points as marked by the magenta dotted line is defined in the controller software for automatic Phase Deactivation based on the operational power setpoint provided to dcB. The same methodology is applied to extract the Phase Deactivation Threshold for the 2 Phase to 1 Phase transition.

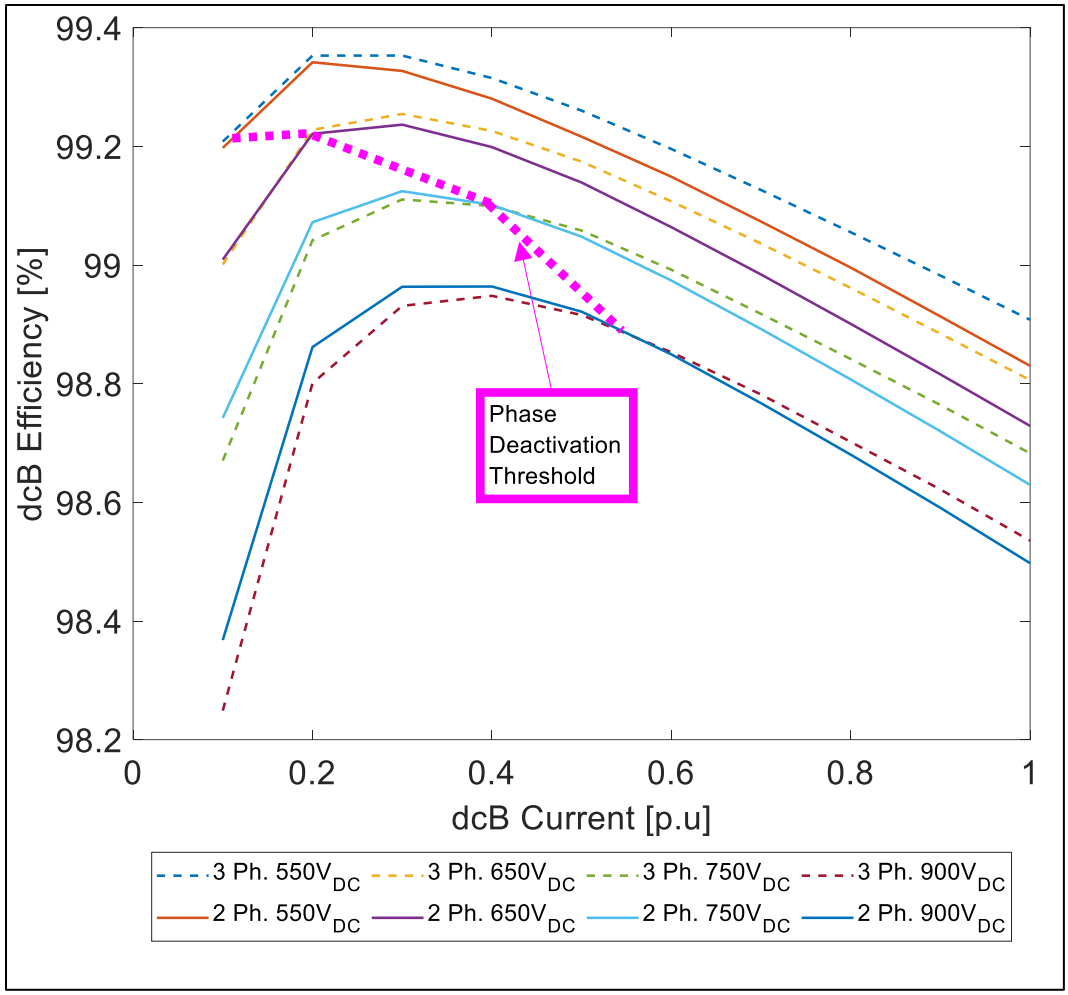

Figure 4.21: dcB efficiency as current in increased in 3-Phase and 2-Phase operation for various DC link voltages giving the threshold to enable/disable Phase Deactivation.

4.3.2 Phase Displacement

The Phase Deactivation optimisation technique presented in Chapter 4.3.1 is highly focussed on reducing losses localised within the converter unit. When considering a highly integrated design such as the multiport converter, which is fundamentally a combination of multiple converter units sharing key components, optimisations of the interfaces at the higher, converter level; the transfer of electrical power converter to converter through the shared interfaces must be performed to achieve a mature and comprehensive design. Hence, a further optimisation technique, Phase Displacement is introduced to complement the "local" optimisation technique, Phase Deactivation described in the preceeding chapter.

Considering the criticality of the DC link presented in the optimisation objectives in Chapter 4.2.4 (see equations (25), (26) and (27)) within the boundaries of cost-detailed in Chapter 2.2, a highly multi-disciplinary design of the 3 converter stages, exploiting the full potential hardware through software algorithms surrounding the shared DC link is sought.

A generalised optimisation study incorporating hardware selection, working voltage and power levels within the constraints of maximum voltage ripple and EMC emissions is presented in [99]. In the case of the multiport converter design however, the influence of the multiple phases of the integrated converter units on the capacitor ripple current stress must also be considered alongside [100], [101] due to the high level of interdependencies of a capacitor with the active power stages.

Apart from hardware-based methods, another way to achieve a reduction in capacitor current is via modulation strategies [69] which are presented in the following. A method to reduce current ripple is presented in [100]; while the reduction results achieved are acceptable, this method exacerbates the issue of capacitor stress depending on the operating modulation index and power factor. In [102], current ripple is minimised through control of the zero vector. However, switching losses are increased due to higher switching action. The study presented

in [103] builds upon this idea through the proposal of an optimal space vector modulation; demonstrating a 43.3% reduction in current harmonic content without increasing switching frequency or inductance. A carrier modulation method is presented in [104]; introducing a modified triangle carrier with a switching frequency twice of the inverter's, for synchronisation of the DCDC converter current to the SPWM inverter current. This method yielded a 50% reduction in current ripple. The application of adaptive phase shift technology [105], [106], [107] is proposed to improve the ratio of harmonic reduction even further.

For simplicity, only dcB and inv sections are analysed while dcA is ignored as shown in Figure 4.22. Here, $I_{C,dcB}$ is the DC-link current of dcB and $I_{C,inv}$ is the VSI demand current. The current through the capacitor is represented as I_C and can be expressed as equation (36). In a complex power conversion system such as a multiport converter, the capacitor stress of the shared DC-link is crucial to the reliability of the whole system and contributes heavily to the losses within the system as identified in Chapter 4.1. Thus, these three currents are key to the investigation. Also illustrated in Figure 4.22 are V_{ES} as an idealised voltage source, I_{abc} as the inverter phase current and converter inductor currents I_{def}.

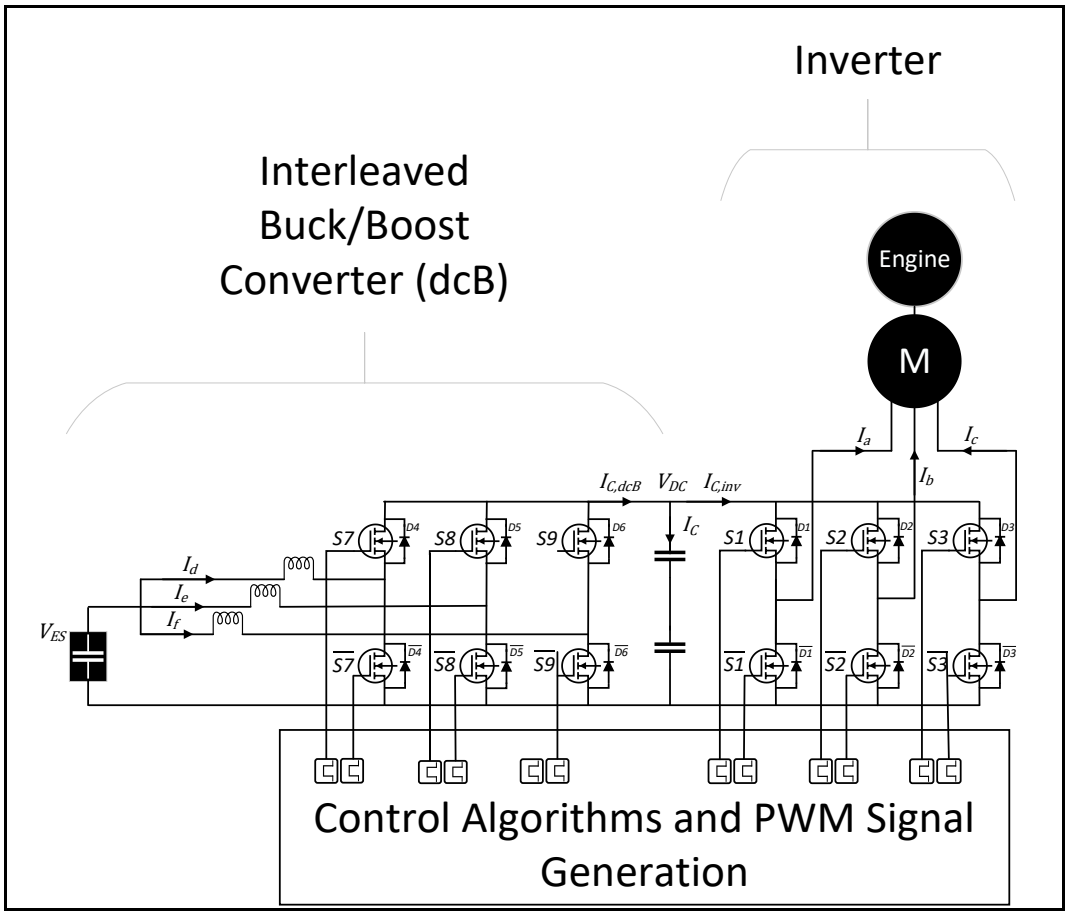

Figure 4.22: Simplified multiport converter composed of a three-cell boost converter (dcB in boost mode) and two-level VSI (inv in motoring mode).

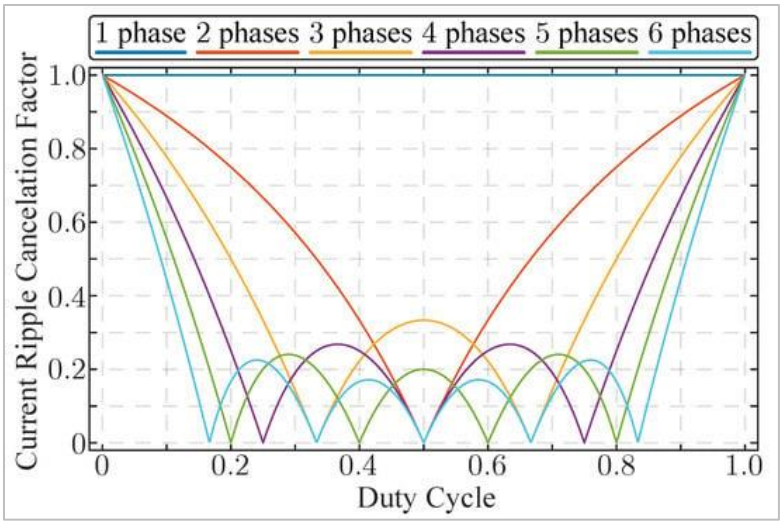

Figure 4.23: Capacitor current ripple cancellation factor as a function of duty cycle for a different number of active phases [69].

Parallel converters such as in the case of dcB are usually operated assuming equal power distribution among each of the parallel phases. It is also known that correct interleaved operation of the modules has the beneficial impact of reducing the peak to peak ripple of input and output currents [105], [108], [109]. The interleaved operation is achieved through use of a phase-displacement angle between the PWM carriers and the resulting modulation method is known as phase-shifted PWM (PS-PWM). In conventional interleaved operation of DCDC converters, the phase displacement angle, ∅ between two consecutive phases is determined as:

$$\emptyset = \frac{360}{N} \tag{29}$$

where N is the number of power cells connected in parallel. The PS-PWM strategy equally shares power loss among the power cells providing lifetime equalisation. In addition, it also presents a multiplicative effect in the effective switching frequency of the input and output waveforms, where the harmonic spectra of the resulting input and output currents present the first harmonic distortion component at N times PWM carrier frequency $F_{C,dcB}$ [110]. The relationship between current ripple cancellation factor and duty cycle variations is displayed in Figure 4.23. The current ripple cancellation factor is a normalised value of the overall reduction in

the peak-to-peak value of $I_{C,dcB}$ and $I_{C,inv}$. The duty cycle determines the voltage ratio between the converter input and output, V_{ES} and V_{DC} respectively as described in (8) and (9). The plot in Figure 4.23 therefore provides the optimal number of interleaved phases for a specific operational point. However, considering the cascaded structure of dcB and inv, the influence of the interaction between both converters needs to be considered to find the optimal number of interleaved phases. There also may be certain harmonic currents produced by dcB that could be used by inv and thus reduce DC link capacitor current.

Harmonic Analysis of the Current Injected by Interleaved DCDC Converters

The harmonic spectrum of the current produced by the dcB for the inverter consumption is best analysed by using the Fourier Series, because it is a uni-dimensional problem [52]. In the case of dcB, the duty cycles do not vary periodically with time in steady state, therefore, this mathematical tool is able to decompose any periodic signal into a DC component plus an infinite sum of cosines and sines as:

$$f(t) = \frac{a_0}{2} + \sum_{n=1}^{\infty} [a_n \cos(n\omega t) + b_n \sin(n\omega t)]$$

$$a_n = \frac{2}{T} \int_0^T f(t) \cos(n\omega t) dt$$

$$b_n = \frac{2}{T} \int_0^T f(t) \sin(n\omega t) dt$$

where ω is the carrier frequency of the converter, $2\pi F_{C,dcB}$ in this case and a_n and b_n are Fourier coefficients.

In an interleaved DCDC converter composing of multiple phases in parallel, the resulting output is determined by the summation of each leg and therefore highly influenced by the phase angle displacement adopted in the operation of the converter. This influence is determined by:

$$\sum_{j=1}^{N} i_j(t) = \sum_{j=1}^{N} \frac{a_{0j}}{2} + \sum_{j=1}^{N} \sum_{n=1}^{\infty} \left[a_{nj} \cos\left(n\omega t - n\emptyset_j\right) + b_{nj} \sin\left(n\omega t - n\emptyset_j\right) \right]$$

where $\emptyset_j$ is the phase displacement angle applied to the j-th phase. Using some mathematical manipulation, each harmonic component can be re-written as:

$$i_{cdcdc,n}(t) = \cos(n\omega t) \left[\sum_{j=1}^{N} \frac{a_{nj} - b_{nj} \tan\left(n\emptyset_j\right)}{\sqrt{1 + \tan\left(n\emptyset_j\right)^2}} \right] + \sin(n\omega t) \left[\sum_{j=1}^{N} \frac{b_{nj} - a_{nj} \tan\left(n\emptyset_j\right)}{\sqrt{1 + \tan\left(n\emptyset_j\right)^2}} \right]$$

$$= C_{1n} \cos(n\omega t) + C_{2n} \sin(n\omega t) = H_n$$

where magnitude and phase may be decomposed as:

$$\|H_n\| = \sqrt{{C_{1n}}^2 + {C_{2n}}^2} \qquad (30)$$

$$\angle H_n = \arctan\left(\frac{C_{2n}}{C_{1n}}\right) \qquad (31)$$

where index n represents a particular harmonic order; or in other words, a multiple of the carrier frequency. Coefficients values for a_{nj} and b_{nj} are determined by the specific DCDC converter topology.

In the case of dcB, the converter shown in Figure 4.22, if m is defined as the positive slope of inductor current and t_1 and t_2 as instants when the diode starts and ends its conduction mode, the following relationships may be derived:

$$m = -\frac{V_{DC} - V_{ES}}{L}$$

$$t_1 = -(1 - D)\frac{T}{2}$$

$$t_2 = (1 - D)\frac{T}{2}$$

Therefore, the carrier coefficients can be obtained as:

$$a_{nk} = \frac{2}{T}\int_{t_1}^{t_2} i_{1,k}(t)\cos(n\omega t)dt = \frac{2I_{Lnk}}{n\pi}\sin(n\omega(1 - D_k))$$

$$b_{nk} = \frac{2}{T}\int_{0}^{T} f(t)\sin(n\omega t)dt$$

$$= \frac{mT}{n^2\pi^2}\left[\sin(n\omega(1 - D_k)\right) + n\omega(1 - D_k)\cos(n\omega(1 - D_k))]$$

Harmonic Analysis of the Current demanded by the Inverter

Unlike the DCDC converter, the inverter is a two-dimensional problem because of the variation of the duty cycle during the fundamental period [111]. Considering the inverter, the resulting harmonic spectrum using the double Fourier Transform of the DC link current:

$$I_{C,inv}(t) = \frac{3}{4}MI_0\cos(\theta) + \sum_{m=1}^{\infty}\sum_{n=-\infty}^{\infty}[A'_{mn}\cos(m\omega_C t + n\omega_0 t) + B'_{mn}\sin(m\omega_C t + n\omega_0 t)] \quad (32)$$

Where M is the modulation index, I_0 is the fundamental output current and θ is the resulting power factor. Coefficients A'_{mn} and B'_{mn} are determined as:

$$A'_{mn} = A_{mn}\left[1 + 2\cos\left(n\frac{2}{3}\pi\right)\right]$$

$$B'_{mn} = B_{mn}\left[1 + 2\cos\left(n\frac{2}{3}\pi\right)\right]$$

$$\mu = \frac{I_0 \cos\left(\left(m + n\frac{\pi}{2}\cos(\theta)\right)\right)}{m\pi}$$

$$A_{mn} = \mu\left[J_{n+1}\left(m\frac{\pi}{2}M\right) - J_{n-1}\left(m\frac{\pi}{2}M\right)\right] \quad (33)$$

$$B_{mn} = \mu\left[J_{n+1}\left(m\frac{\pi}{2}M\right) + J_{n-1}\left(m\frac{\pi}{2}M\right)\right] \quad (34)$$

where coefficients m and n denote a specific harmonic group (m) and a particular harmonic component within it (n). As in (30) and (31), the separation into magnitude and phase of each harmonic component can therefore be performed:

$$\|Z_k\| = \sqrt{{A'_{mn}}^2 + {B'_{mn}}^2}$$

$$\angle Z_k = \arctan\left(\frac{B'_{mn}}{A'_{mn}}\right)$$

Remark: indexes m and n denote a different quantity in this section to the analysis presented in the section prior. index k is related to the specific harmonic order through the following:

$$k = mR + n \quad (35)$$

where R is the ratio between carrier and fundamental frequency.

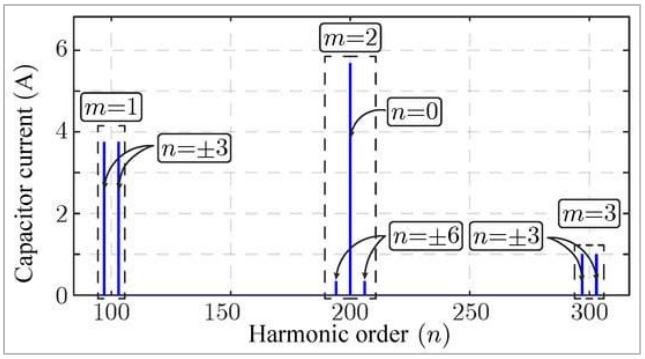

Figure 4.24: Capacitor current harmonic spectrum decomposition [110].

Analysing the relation derived in (32), it is clear the current demanded by the inverter consists of a DC component and a sum of harmonics introduced by the carrier and side band components. These harmonic components are influenced by

the operational point of the inverter, whereby A'_{mn} and B'_{mn} are determined by the fundamental component of the output current as well as power factor. Analysis of (33) and (34) in [110] shows that the main harmonic component of the capacitor current is located at m=2 and n=0, whereas the rest of the harmonic components are located as illustrated in Figure 4.24[111], [112], [113], [114].

Capacitor Current Harmonic Minimisation

Applying Kirchhoff's first law, it is possible to obtain the current flowing through the shared capacitor as a function of converter and inverter current:

$$I_C(t) = I_{C,dcB}(t) - I_{C,inv}(t) \qquad (36)$$

Thus, linking the two converter units and proving harmonic minimisation can be achieved if two conditions are met:

1) A specific carrier frequency ratio between converter and inverter is selected. Considering the system illustrated in Figure 4.22, the carrier frequency of both subsystems should fulfil:

$$2F_{C,inv} = NF_{C,dcB} \qquad (37)$$

Which will ensure that the main harmonic components of both subsystems will be located at the same frequency to enable any harmonic compensation or minimisation to occur.

2) The phase displacement angle resulting in the minimization of the resulting $I_C(t)$ should be applied. That is:

$$\varphi: \min (H_n + Z_k) \qquad (38)$$

Where coefficients H_n and Z_k represent current injected into the DC link by the interleaved DCDC converter and current drawn by the inverter respectively. The coefficients n and k are selected according to the specific harmonic component to be reduced.

The implemented control structure for dcB and inv is shown in Figure 4.25. This strategy builds upon the conventional control scheme proposed in Chapter 3.3; only varying the phase displacement angle between the two carriers within the modulators of the respective converters.

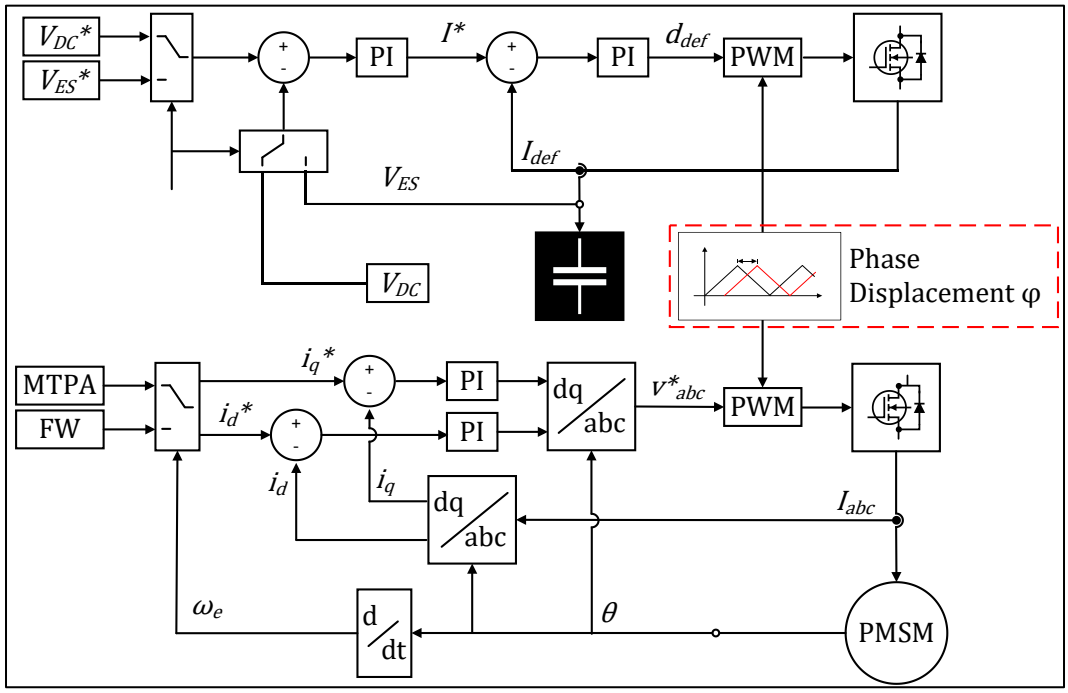

Figure 4.25: Phase Displacement implementation within Boost converter and inverter controller structure.

Results and Discussion

To validate the effectiveness of the phase displacement technique, the Simulink/PLECS model initially developed in Chapter 4.2 is simplified according to Figure 4.22. This reduced model of the multiport converter only includes the 3-cell Interleaved buck/boost dc boost converter (dcB) and conventional 2-level 3-phase inverter (inv) driving a PMSM.

A similar approach is taken to locate the optimum phase displacement angle based on the evaluations in [110]; where it was showed that in the case of a 3 cell converter, the optimum phase displacement angle, (38) was determined by the machine speed. Here, three different test cases made up of different speed and switching frequency values are investigated as listed in Table 7.

Table 7
EVALUATED STATES TO VALIDATE EFFECTIVENESS
OF PHASE DISPLACEMENT OPTIMIZATION [110]

Test Case	**Speed [RPM]**	**Torque [N/m]**	**Switching Frequency [kHz]**	
			Inverter	Boost
Case 1	600	200	6	4
Case 2	500	200	6	4
Case 3	600	200	6	7.2

As illustrated in Figure 4.26 by the black circles at 9° (Case 1) and 30° (Case 2) indicating the optimum point-value of phase displacement angle that resulted in the lowest value of capacitor RMS current.

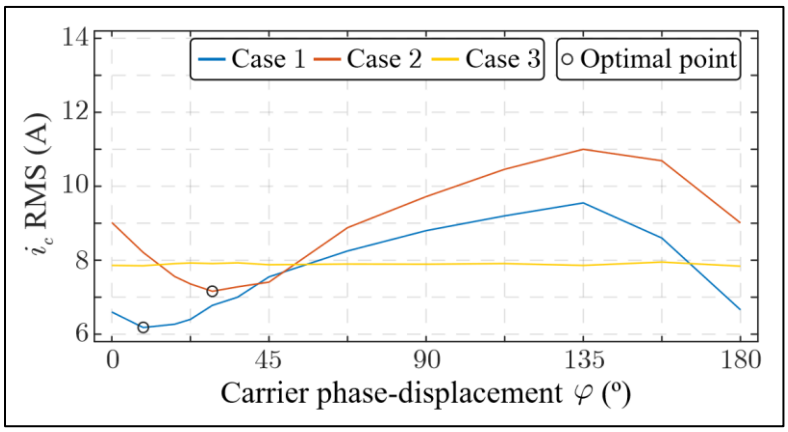

Figure 4.26: Evaluation of the effective current in the DC link capacitor of a 3-cell interleaved converter[110].

The results clearly demonstrated that maximum capacitor current reduction was only possible when equation (37) was obeyed in Case 1 and 2. Conversely, in Case 3, where the inverter and boost converter were operating with mismatched frequencies of 6kHz and 7.2kHz respectively, harmonic reduction was not achievable.

Although many fundamental framework elements are evaluated in [30], [69], [110], [114], it is imperative to consider that the inverter and DCDC converters have fundamentally very different operating principles. While the inverter sees limited benefit from increased switching frequency in governing the electric machine, it is common practice by industry to operate DCDC converters at higher frequencies as doing so allows volumetric and weight reductions [115], [116]. The analysis in in [55] only considers $F_{C,inv} \geq F_{C,dcB}$ which strictly limits the practical usefulness of this technique.

Table 8
EVALUATED OPERATIONAL POINTS
FOR PHASE DISPLACEMENT

Case	Speed [RPM]	$F_{C,inv}$(kHz)	$F_{C,dcB}$(kHz)	Target Harmonic (kHz)
A	100-800	6	4	12
B	100-800	6	8	24

Building on the work presented in [55], the simulated speed range is firstly extended beyond base speed of the machine (to 800RPM) to evaluate the effectiveness of harmonic reduction in the field weakening region of the machine. Next, higher values of $F_{C,dcB}$ are applied, selecting higher order Targeted Harmonics (TH) within I_C for reduction. To illustrate the effect of phase displacement on different harmonic spectrum locations (12kHz and 24kHz), Case A and Case B use 4kHz and 8kHz for the converter respectively while the inverter was kept at 6kHz. The DC link current spectra in Case A and Case B are provided in Figure 4.27 and Figure 4.28 across the speed range.

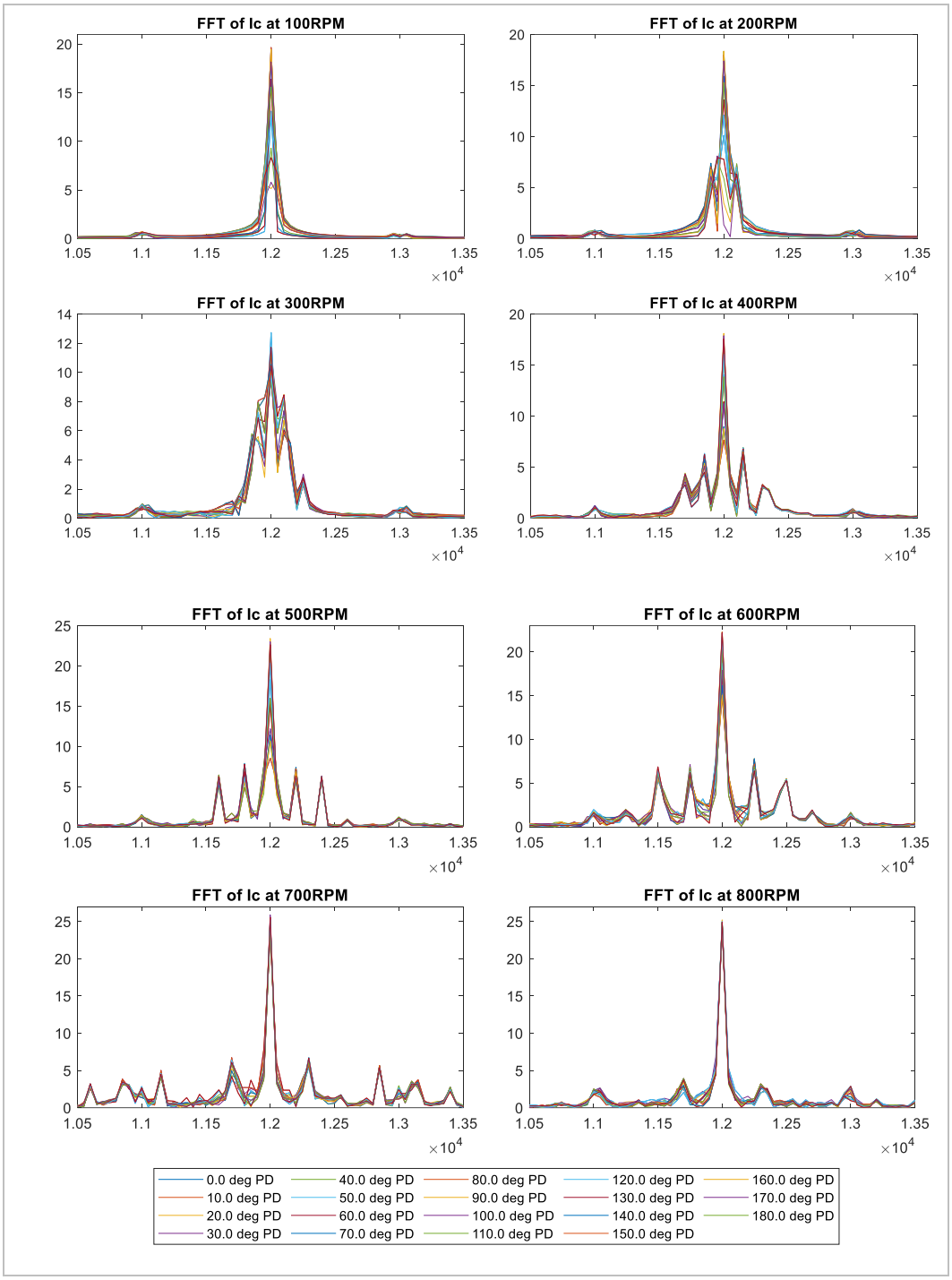

Figure 4.27: Resultant capacitor current spectrum at 12kHz (Case A) for Phase Displacement angles ranging from 0-180 degrees at PMSM speed ranging from 100-800RPM.

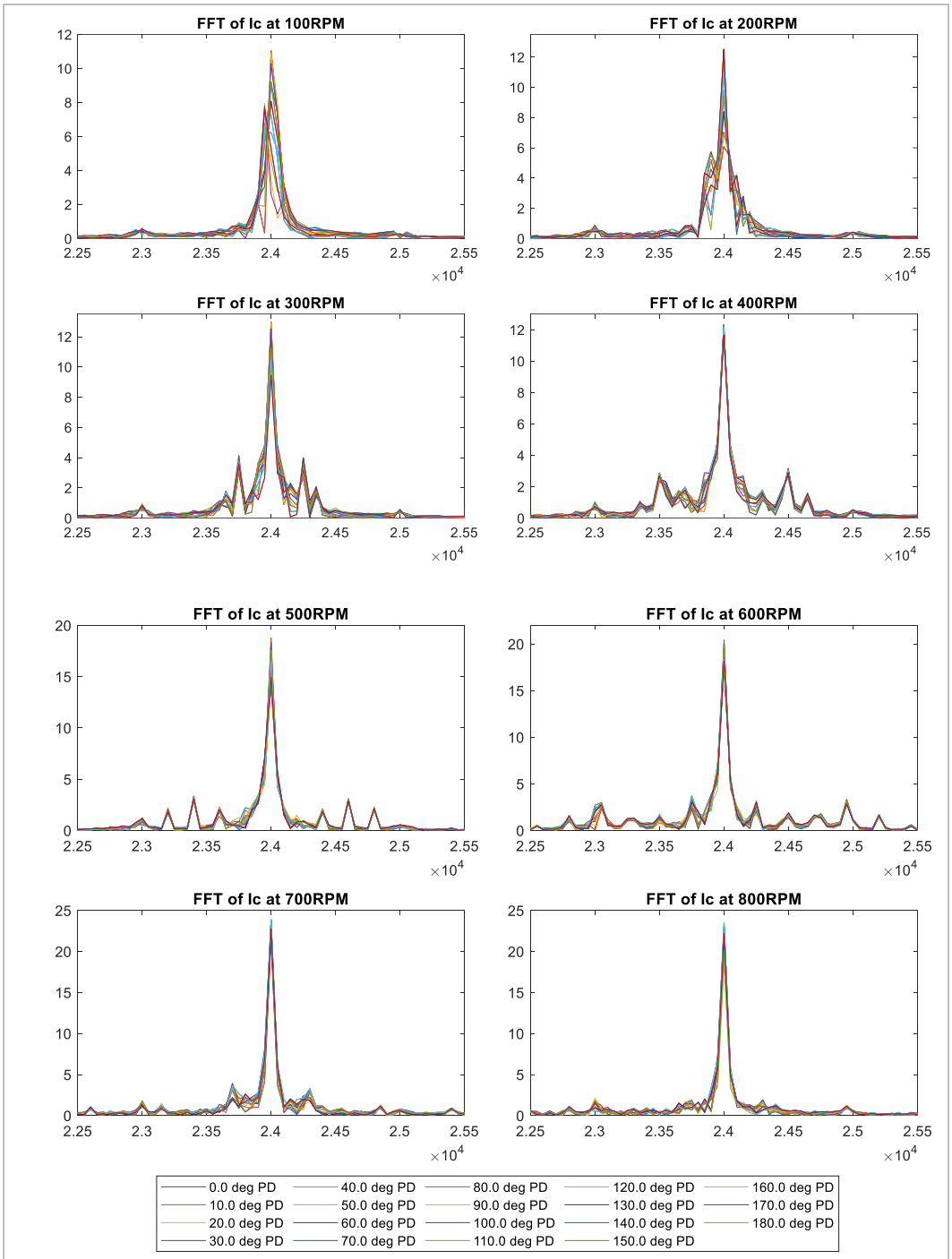

Figure 4.28: Resultant capacitor current spectrum at 24kHz (Case B) for Phase Displacement angles ranging from 0-180 degrees at PMSM speed ranging from 100-800RPM.

It can be observed in Figure 4.27 and Figure 4.28 that main component of energy in the harmonic spectrum of the current injected into the shared DC link is located at N times $F_{C.dcB}$ considering a balanced operation where N = 2 and 4 in Cases A and B respectively. The next key point relates to the contributions by the stationary dq-frame control strategy implemented within the inverter in Figure 4.25. As the speed of the PMSM is increased closer to base speed, the modulating voltage signal amplitude requested by the PI controllers of dq currents also increases to compensate for the armature reaction produced by the self-excited rotor, resulting in changes of modulation index, M. As it is necessary to synchronise M to the fundamental frequency of the machine throughout the operating range in order to achieve torque regulation, the amplitude and phase of the harmonic groups, m and components, n are highly dependent on current magnitude and power factor. Throughout the speed sweeps of Case A and Case B, it is observed in Figure 4.27 and Figure 4.28 that the sidebands, n of harmonic groups, m=1 to 3 increase in amplitude with proportion to speed and shift along the frequency axes according to M and power factor. Only the harmonic component located a m=2 and n=0 remains at a fixed position confirming the relations (32) and (35).

The plots in Figure 4.27 and Figure 4.28 are analysed to determine key parameters to prove the effectiveness of the Phase Displacement technique:

1) Optimal Angle, $\varphi_{opt.}$
2) RMS Capacitor current, I_C with φ_{opt} applied.
3) Targeted Harmonic peak value with φ_{opt} applied.
4) Worst-case maximum value of I_C.
5) Percentage reduction of Targeted Harmonic peak value with PD applied.

The resultant values from the FFT study of the waveforms shown in Figure 4.27 and Figure 4.28 are tabulated in Table 9 and Table 10 respectively for easy comparison.

Table 9
CASE A RESULTS: OPTIMUM PHASE DISPLACEMENT ANGLE FOR MINIMUM CAPACITOR CURRENT

Speed [Rpm]	φ_{opt} [°]	φ_{opt} $I_{C,RMS}$ [A RMS]	φ_{opt} TH [A peak]	Max I_C angle[°]	Max $I_{C,RMS}$ [A RMS]	Max I_C [A peak]	RMS Reduction [%]
100	100	9.5	4.773	160	11.7	14.8961	18.80
200	100	13.6	2.93629	160	17.7	17.472	23.16
300	100	16.8	4.76049	160	18.8	13.2992	10.64
400	150	17.3	8.10864	100	18.7	13.9438	7.49
500	40	16.7	6.98162	100	19.7	19.5621	15.23
600	150	16.9	10.7849	100	17.9	19.4943	5.59
700	160	15.7	14.6834	100	16	18.3936	1.88
800	50	12.3	15.0808	110	12.6	15.599	2.38

Table 10
CASE B RESULTS: OPTIMUM PHASE DISPLACEMENT ANGLE FOR MINIMUM CAPACITOR CURRENT

Speed [Rpm]	φ_{opt} [°]	φ_{opt} $I_{C,RMS}$ [A RMS]	φ_{opt} TH [A peak]	Max. I_C angle[°]	Max $I_{C,RMS}$ [A RMS]	Max I_C [A peak]	RMS Reduction [%]
100	90	10	2.12067	30	10.8	8.0736	7.41
200	30	12.9	4.19918	90	13.8	9.2693	6.52
300	90	14.6	7.38363	150	15.1	9.4544	3.31
400	200	15.5	9.49884	20	15.6	10.726	0.64
500	200	21	11.7887	20	21.6	14.922	2.78
600	30	22.3	14.6097	90	23.4	17.493	4.70
700	90	33.6	19.7663	150	34	22.255	1.18
800	140	39.7	24.2222	90	40.4	27.182	1.73

The maximum reduction of $I_{C,RMS}$, RMS Reduction, is obtained by comparing the RMS values of current when φ_{opt} is applied with the worst-case RMS current for a given PMSM speed. It is found that the reduction percentage when a higher order harmonic is targeted. This shows a potential limitation of the PD technique in practical application as PMSM connected 2-level inverters do not gain any performance benefit from high switching frequencies. Due to reasons discussed prior, inverters typically have a much lower switching frequency compared to DCDC converters therefore targeted harmonic frequencies must be higher, reducing the impact on $I_{C,RMS}$ reduction.

4.4 Discussion and Conclusions

4.4.1 MOOP Analysis

In the previous sections, a comprehensive model of the multiport converter loss quantities and optimization techniques has been presented, providing the essential framework necessary to perform the MOOP analysis.

The effectiveness of the optimization techniques and strategy is proven by collectively applying Phase Deactivation and Phase Displacement techniques in conjunction with active variation of the switching frequency and DC link charge level according to optimal parameter sets obtained through sweeps of the objective functions given in equations (25)-(27) described in Chapter 4.2.4.

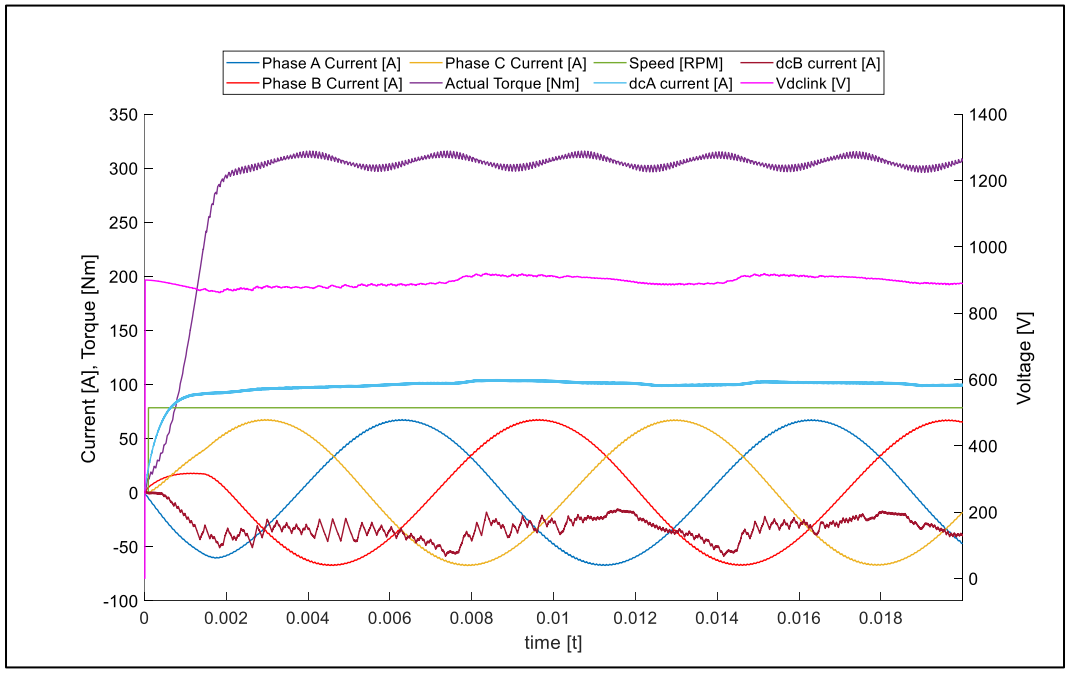

Figure 4.29. Simulink simulation of single operational point (750RPM and 300Nm) including all elements of design space.

To obtain the Pareto Front indicating the optimum solution, the Design Space (DS) is defined. A simulation run of a single operational point is shown in Figure 4.29 to correlate the Pareto tools to the simulation design and results.

The Design Space consists of:

1) **Machine Torque**- The multiport converter must be capable of supplying demanded torque to assist performance of the engine and regenerative torque during energy recovery events. This parameter is commanded by the driver of the vehicle and therefore out of the control of the converter. Therefore, the torque reference to the inverter PI controller is set constant throughout the duration of a single simulation run, illustrated in Figure 4.29. The actual mechanical torque, shown in purple, produced by the PMSM is shown for a reference of 300Nm.
2) **DC link charge level**- while conventionally the voltage of the DC link was kept at a constant level determined by voltage limits of the PMSM and hardware of the inverter, this value is actively varied to optimize for greater efficiency. DC link voltage and dcB current, I_d (as $I_d(t)=I_e(t)=I_f(t)$) are shown in magenta and brown respectively in Figure 4.29.
3) **Switching frequency** of the three converter modules- $F_{SW,inv}$, $F_{SW,dcA}$, $F_{SW,dcB}$. When considering the maximum and minimum bounds of the switching frequencies, it must be considered that the switching frequency of the inverter is bound by the frequency of the phase current to provide adequate control bandwidth. While the DCDC converters do not have this dependency, switching frequency must be carefully selected to avoid discontinuous conduction mode (DCM) [117] and remain in continuous-conduction mode due to better output voltage and reduction in inductor current ripple.
4) **Machine Speed**- the machine speed range was selected to match the engine. As described in Chapter 3.1, as rotor speed exceeds base speed, changeover from MTPA to FW operation is necessary, leaving only a small portion of DC link voltage available for torque regulation [118]. Knowing this, the DS sweeps only account for maximum continuous torque below base speed (600RPM). Requested torque is limited above base speed, in an operating range also known as the continuous power or field weakening region [119]. As the selected operational point in Figure 4.29 is within the field

weakening region, some i_d current is applied to keep the requested torque for the fixed speed (in green) of 750RPM.

5) **Total Harmonic Distortion (THD) Percentage, $\%_{THD}$.** A maximum limit of 5% was applied to the inverter phase currents throughout the operating range as the assumed requirement from Noise, Vibration and Harshness (NVH) studies [120]. To obtain this value from simulation, the thd function from MATLAB is used to post-process the phase currents, I_{abc}, shown in blue, red and yellow respectively in Figure 4.29. The average of the three THD values is taken for each simulation run. The THD of the maximum and minimum applied currents along the Pareto Front are presented.

The singular run presented in Figure 4.29 is repeated for key points of the PMSM operational speed and torque range- 500 to 1500RPM and 100Nm up to maximum available torque depending on the speed. The analysis is partitioned into CASES I-IV, as per Table 11. For each case, the simulation is reran as the Pareto input parameters, $F_{SW,inv}$, $F_{SW,dcA}$, $F_{SW,dcB}$ and V_{DC} are varied from their minimum to the maximum values as system efficiency and phase current THD values are recorded. The results from the simulation sweeps including the plotted Pareto fronts of CASES I-IV are depicted in Figure 4.30-Figure 4.33. The Pareto input parameters of each the Fronts are tabulated in Table 11 and marked in red.

Table 11
MOOP PARAMETERS

Case	Machine Speed [RPM]	Maximum Continuous Torque [Nm]	$F_{SW,inv}$ [kHz] Min=3.125 Max=12.5	$F_{SW,dcA}$ [kHz] Min=12.5 Max=100	$F_{SW,dcB}$ [kHz] Min=12.5 Max=100	Minimum V_{DC} [V]	Average System efficiency gain [%]*
I	500	450	3.125	12.5	25	600	4.02
II	750	450	3.125	12.5	25	650	6.26
III	1000	400	8	12.5	25	675	5.66
IV	1500	200	12.5	12.5	25	700	2.12

*****improvements vs baseline design parameters: $F_{SW,inv}$ =12.5kHz, $F_{SW,dcA}$ =50kHz, $F_{SW,dcB}$ =50kHz.

The following assumptions were made to simplify analysis:

1) The inverter efficiency difference between motoring and regenerative modes of operation is small enough to be neglected. Owing to the superior characteristics of SiC material, the antiparallel freewheeling SiC Schottky diodes have negligible reverse recovery loss[121], leading to much closer loss values between motoring and generating as presented in [122] ; therefore justifying this assumption.
2) The effect of temperature on the DC link capacitance value and losses is neglected.
3) Mechanical losses within the PMSM, such as rotor windage and bearing friction or electromagnetic losses such as eddy current or iron losses are ignored as this study focuses on the efficiency of the multiport converter.

Given these assumptions, Figure 4.30 illustrates the Pareto Front at 500RPM which is the setpoint speed for an engine crank event. Each point represented in the plot illustrates a unique set operational conditions - DC link voltage (colour) and PMSM torque (x-axis), against the resultant multiport converter efficiency (y-axis). Each point is only plotted if the percentage THD, $\%_{THD}$ is lower than the maximum of 5% as defined in the Design Space. The Pareto Front is marked by 'x's as the combination of operational conditions that result in the highest Total Efficiency. The same technique for data analysis and finding the Pareto Front is applied across CASEs II-IV.

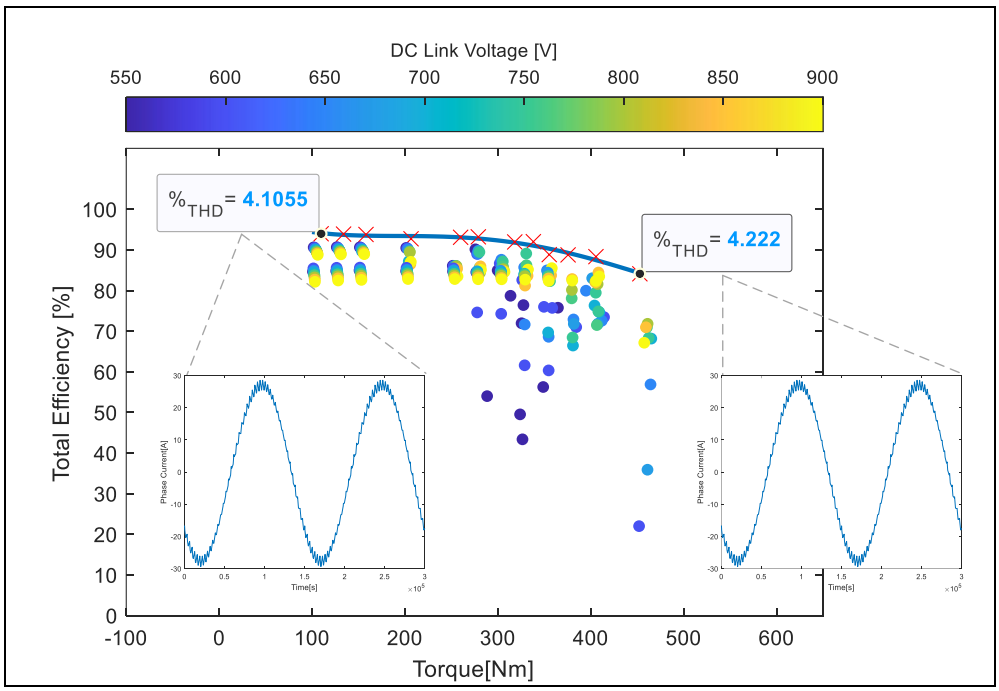

Figure 4.30. CASE I: Pareto Front of multiport converter operation for varying values of requested driver torque at 500RPM.

At speeds of more than 600RPM, engine fueling takes over and the engine controller regulates to the preset idle speed of 750RPM - CASE II illustrated in Figure 4.31 . At this speed, the performance sweeps from Chapter 4.2.4 showed that the optimal switching frequency of the inverter, dcA and dcB of 3.125kHz, 12.5kHz and 25kHz respectively provided the best balance between efficiency and controllability, the integer ratio of 1:4:8 necessary for Phase Displacement to be effective and for the inverter to produce low phase current ripple resulting in good torque response with minimal losses. At speeds above 750RPM, it is necessary to increase inverter switching frequency to maintain good controllability throughout the torque range.

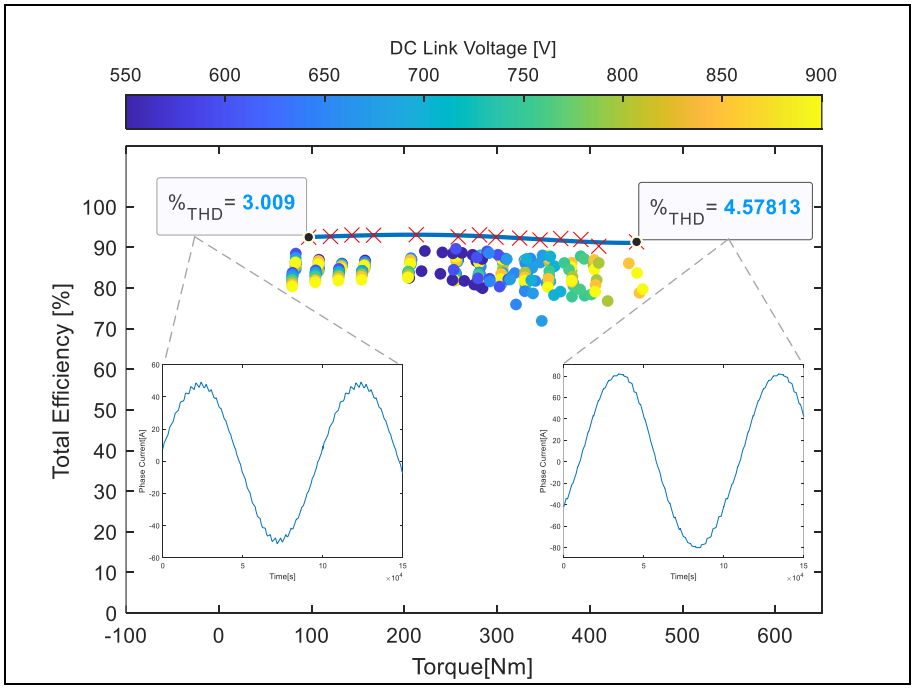

Figure 4.31. CASE II: Pareto Front of multiport converter operation for varying values of requested driver torque at 750RPM.

CASE III, pictured in Figure 4.32, presents a unique situation where the highest efficiency is achieved through a tradeoff between switching frequency selection and PD. Despite the preference to keep the integer switching ratio between converter switching frequencies for the PD technique to work, it was observed that setting $F_{SW,inv}$ =6.25kHz (ratio 1:2:4) was not viable due to the drop in current control quality at high speed and torque. Conversely, opting for the higher switching frequency of $F_{SW,inv}$ =12.5kHz (ratio 1:1:2) instead resulted in poor overall efficiency due to increased switching losses. Setting $F_{SW,inv}$ to 8kHz presented the best overall balance between control quality and system efficiency.

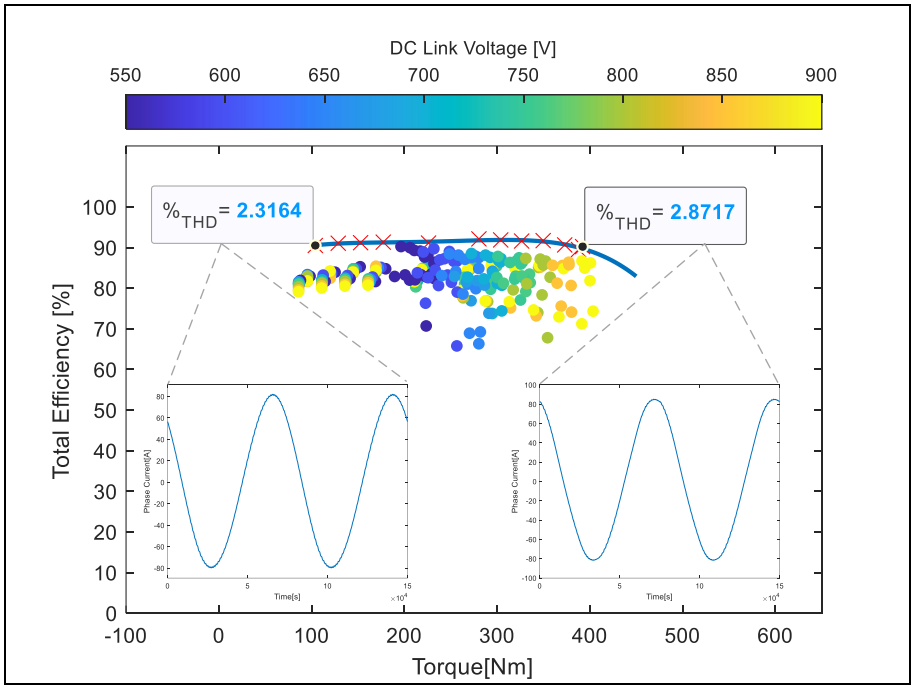

Figure 4.32. CASE III: Pareto Front of multiport converter operation with and without optimizations for varying values of requested driver torque at 1000RPM.

CASE IV, illustrated in Figure 4.33 presents the operation of the machine deep in the field weakening region. As listed in Table 11, maximum continuous torque is nearly half of rated torque. However, it is important to sustain a good level of controllability at this speed point to supplement the engine and increase the overall maximum torque capability of the driveline and to be able to perform energy recovery. As described in [118], the voltage limit of the PMSM is determined by the DC link voltage, therefore the minimum setpoint V_{DC} has to be increased with speed.

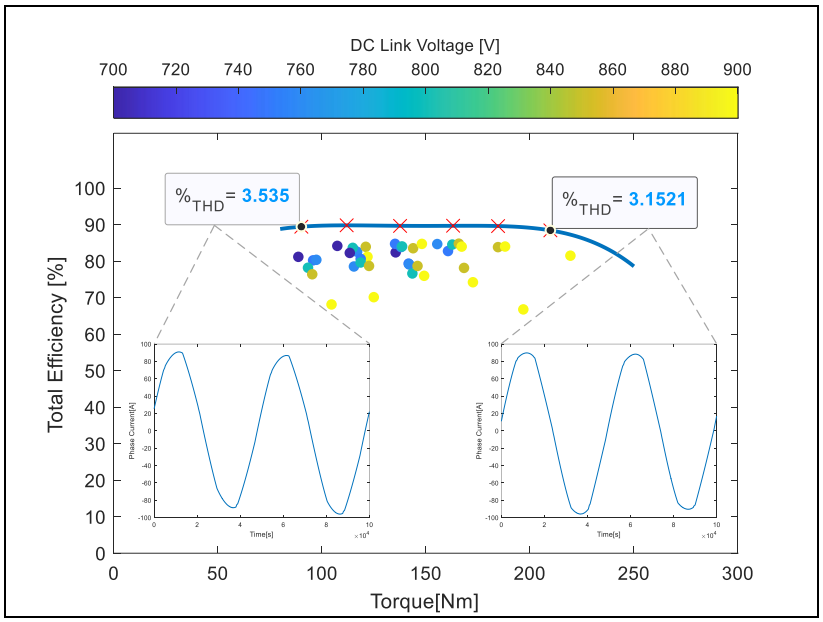

Figure 4.33. CASE IV: Pareto Front of multiport converter operation for varying values of requested driver torque at 1500RPM.

In order to finally gauge the benefit of optimisations achieved, an average system efficiency gain across the range of operational torque for each case is calculated. All cases demonstrate a positive system efficiency gain when compared to baseline parameters used in the initial multiport converter commissioning. A reduction in efficiency gain is seen as speed tends to the maximum value due to the increased current required in deep field weakening region.

4.4.2 Optimisation Summary

In this chapter, the Multi-objective Optimization Problem (MOOP) solving technique has been applied within the design and optimization of a proposed multiport automotive converter. Next, multiple modelling stages are followed for confirmation of design and subsequently, the execution of the MOO analysis. The results are verified against the commercially established PLECS software toolset, by applying manufacturer provided data implemented within the model blocks; guaranteeing a high degree of accuracy and close alignment with hardware. Once a clear parameter baseline is established, comprehensive system level simulation sweeps are carried out with the complete converter design and results are analysed to obtain a clear understanding of the interactions between the key parameters and MOO objective functions. Finally, the Phase Deactivation and Displacement techniques to reduce switching, conduction and capacitor losses were considered and compared with the standard implementation.

All in all, as tabulated in Table 11, through MOO of a state-of-the-art multiport converter design, it is demonstrated that a total efficiency improvement of up to 6.26% was possible through systematic identification of critical loss parameters and the application of a combination of techniques to counteract them. As the cost function determined that the DC link value was a highly contributing factor within the system control objectives, optimization was realised through the implementation of “smart” adaptation of the DC link where its value could be varied throughout the vehicle drive cycle depending on current and “future” load forecasts in a scheme similar to [123]. As expected, efficiency gains are reduced at high speed due to the high switching frequency settings needed to sustain inverter current controller bandwidth and high DC link voltage values required for Field Weakening control.

While the inverter operation is bound by the drive torque requests, the DCDC converter components exploit advanced control schemes-such as the Phase Deactivation or Phase Displacement techniques to further optimize efficiency gains

through elimination of capacitor current harmonics or reduction of power module losses. As these algorithms are independent of each other, they can be operated if the following two conditions are met:

1) A minimum of two multi-phase converter components is operated.

2) All control algorithms are executed in a single microprocessor unit for synchronization and minimization of communication delay.

Chapter 5

Hardware Prototyping and Validation

To have a good confidence level in the loss estimation models used for MOOP and control optimization proposal, it is important to systematically profile the converter power losses throughout its operating range. As described in Chapter 4.2, this is performed through obtaining conduction losses and switching losses independently. Firstly, the conduction losses are obtained through measurement of the virtual junction temperature while a constant DC current is applied through the power module for different coolant flow and temperatures. Next, switching losses are obtained by measuring E_{ON} and E_{OFF} for various amplitudes of sinusoidal current and switching frequencies while keeping modulation technique, power factor, modulation index, DC link voltage and coolant flow and temperature constant. Temperatures at key points-die surface, bus bar terminal, ambient, coolant inlet and outlet and heatplate are also measured to give additional confidence in the virtual junction temperature and loss measurements. These tests are repeated across modules from 4 different manufacturers and compared against in house test results to reduce sources of uncertainty such as delay, and measurement errors introduced by the test instrumentation and fine tune the test methodology.

Once the power modules have been thoroughly understood at the component level, the complete design can be implemented within the intended multiport converter package. Here, the complete converter model and simulated control scheme is comprehensively validated on a test bench and on-vehicle according to performance requirements. Finally, advanced control schemes can be

quickly implemented and simulated with a high degree of accuracy as the model has near one-to-one correlation to the physical counterpart.

5.1 Power Module Profile Test Setup

An instrumented test platform (pictured in Figure 5.1 A and B) is built per the schematic shown in Figure 5.2. The half-bridge is connected to a single inductive load and supplied from 2 parallel connected EA-PS 9040-340 high current (340A continuous) power supplies (Figure 5.1A).

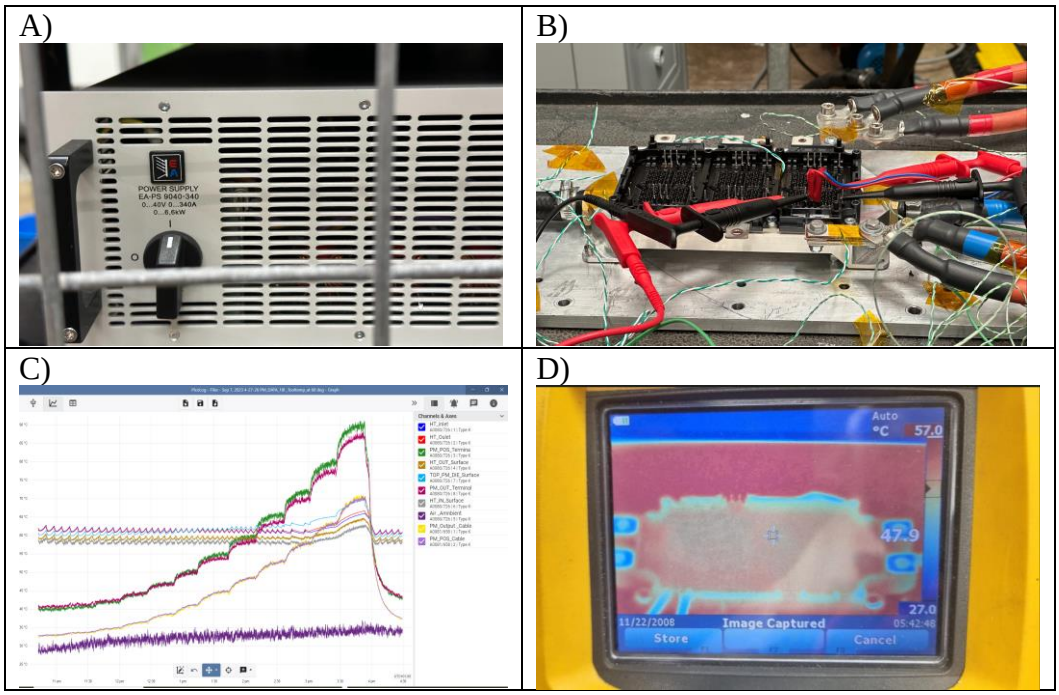

Figure 5.1. A) EA-PS 9040-340 Power Supply, B) instrumented power module test rig, C) thermocouple temperature measurement and D) Thermal imaging capture techniques.

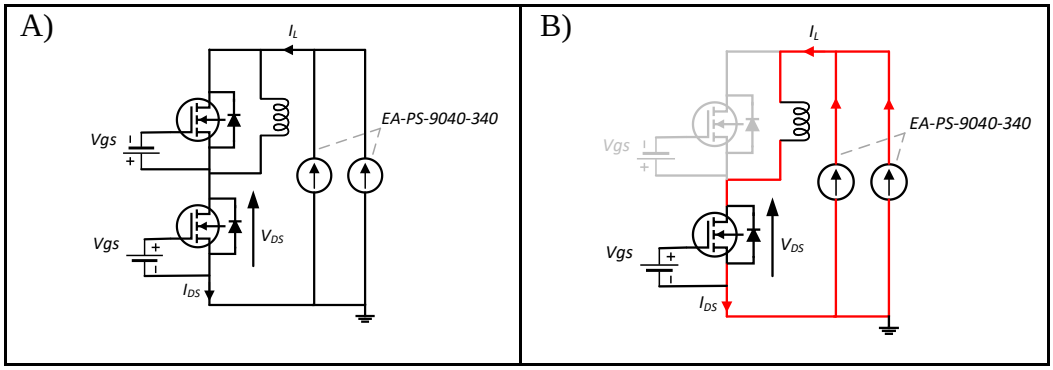

Figure 5.2. Schematic with power loss measurement points (A). Current flow direction during test operation.

The input DC current, I_L and gate pulse signal probe are fed into a state-of-the-art Textronix MSO58 oscilloscope. The Textronix oscilloscope has a high sample rate of 6.25 G Samples per second at 16-bit resolution and a bandwidth of 350MHz. It is also equipped with a configurable digital low-pass filter. Filter attenuation is accounted for in this chapter as it has an impact on the measured voltage and current during fast switching transients. SiC MOSFET 6 pack modules from 4 manufacturers, Leapers, Infineon, ST and Hitachi are individually tested in open loop mode where the top switch is constantly turned off while the properties of the bottom switch are measured in ON state. For the purposes of intellectual property protection, the exact model number of some of the power modules will not be revealed. The oscilloscope measures the conduction power loss, and the switching power loss. Summed together this gives an approximate total electrical loss value out of a single switch. This is then multiplied 6 times for loss within the inverter or 18 times for the multiport converter.

5.1.1 Conduction Losses Validation

This test is carried out at two coolant temperatures, 25°C and 65°C. The inductor current I_L is varied from 50A to 600A in steps of 50A while keeping the bottom switch of the H-bridge continuously turned ON and top switch continuously OFF. The collector-emitter voltage and current are recorded.

Table 12
CONDUCTION TEST PARAMETERS

Test parameter	**Value**
DC current	50-550A
Coolant temperature, T_{cool}	25°C, 65°C
Flow rate	10L/min

Experimental procedure

In the conduction loss tests, the constant turn-on pulse applied on the bottom switch causes a constant DC current to flow through the switch, I_{DS} as illustrated in Figure 5.2. The fixed-amplitude DC current causes temperature to rise according to the properties of the thermal interface between the MOSFET junction and the cooling medium; settling once a thermal equilibrium has been reached. The steady state V_{DS} and I_{DS} are used to calculate the on-state resistance, $R_{DS(on)}$ to give us the power dissipation of the device as per Equation (12). As DC current is applied, the AC time element is eliminated. The steps are repeated for current values of I_{DS} from 50A to 550A, increased in steps of 50A, for coolant temperatures of 25°C and 65°C. The resulting $R_{DS(on)}$ profiles are plotted as shown in Figure 5.3 and Figure 5.4 respectively.

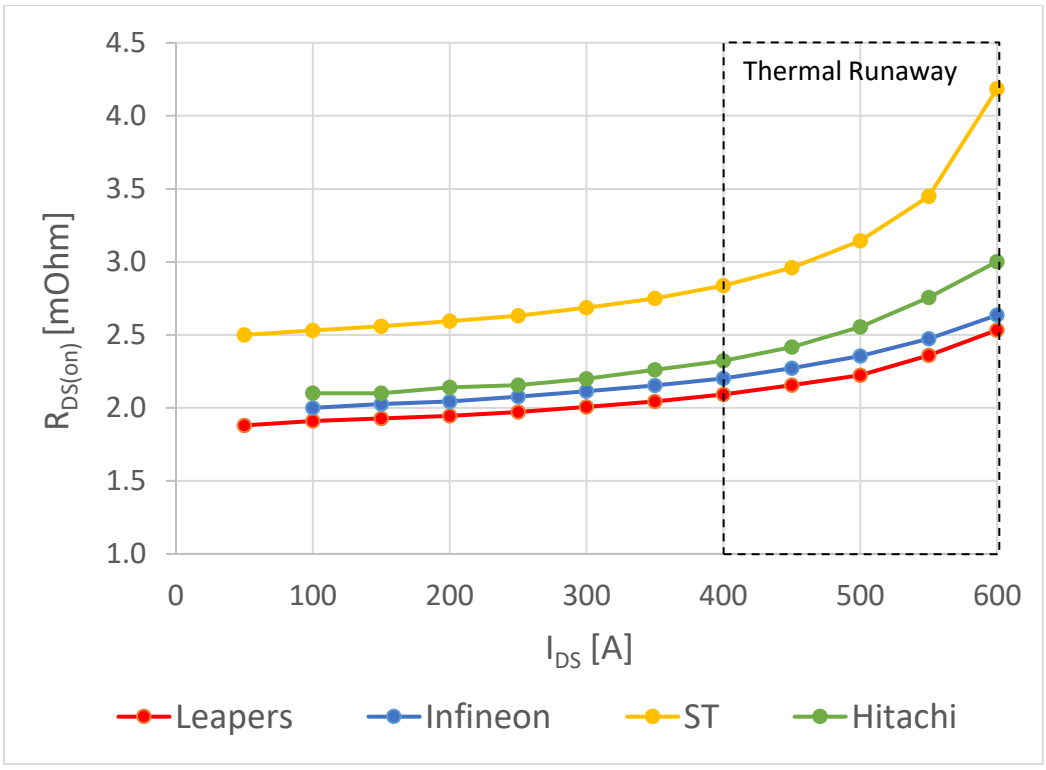

Figure 5.3. Experimentally derived $R_{DS(on)}$ profile vs I_{DS} characteristic at 25°C.

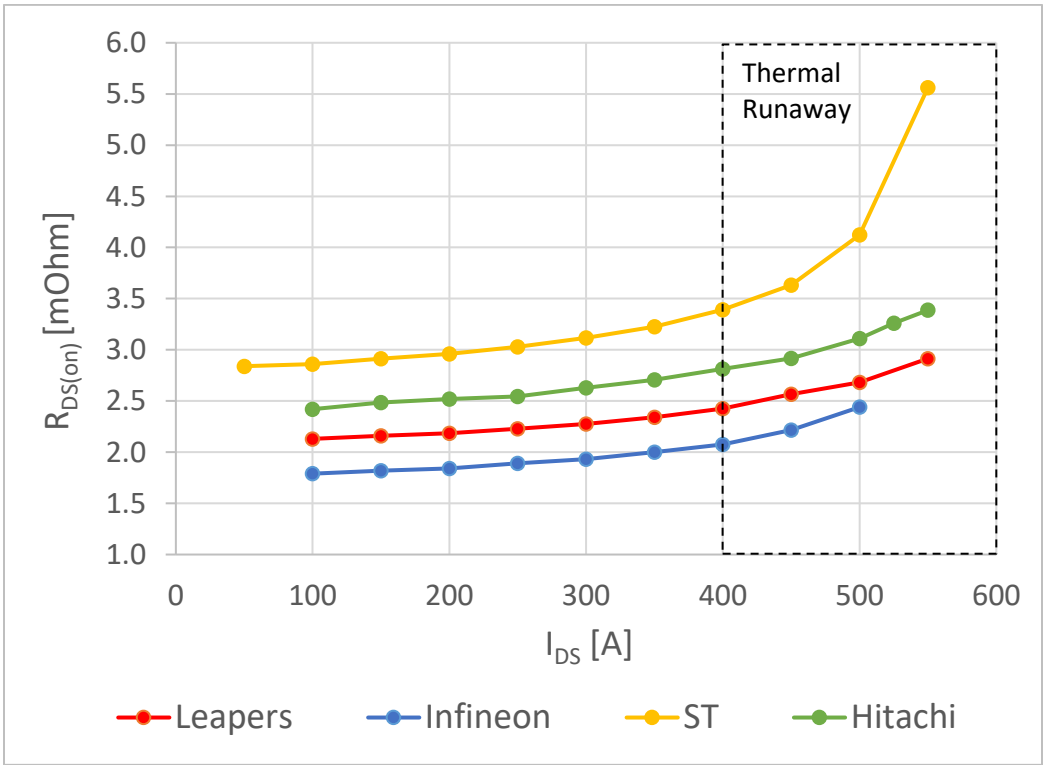

Figure 5.4. Experimentally derived $R_{DS(on)}$ profile I_{DS} characteristic at 65°C

Results Discussion

Comparing Figure 5.3 and Figure 5.4, it is observed that the temperature of all modules follow a linear upward trajectory between 100A and 400A before transitioning into an exponential increase at the higher values of current (>400A) with the ST power module demonstrating this behaviour the most. R_{DS} behaviour is influenced by two key factors [124]:

1) Junction temperature dependent R_{DS} behaviour. The combined effects of channel mobility and dopant concentration is described in [125] where the lowest on state resistance, R_{DSmin} appears at an optimal junction temperature.
2) I_{DS} dependent R_{DS} behaviour. As described in the experiment methodology, current and junction temperature are both allowed to settle before each measurement is taken. This is to allow for a dynamic power balance of transient power dissipation and the thermal path of the parallel dies to be achieved [126] through the directly proportional relationship between thermal conductivity and junction temperature. However, the balance may be unsettled by some overcurrent conditions resulting in thermal runaway observed in both Figure 5.3 and Figure 5.4. As this phenomenon is due to inadequate cooling action of the device package, device current should be kept within a safe limit to prevent its occurrence.

Power Dissipation

The temperature independent average power loss, P_{loss} estimated using Equation (12) from Chapter 4 is now verified against the experimental results shown in Figure 5.5 A) and B), giving further confidence in the simulation tools developed. Next, the Virtual Junction Temperature (VJT) profile for the same currents is extracted experimentally for development of the MOSFET temperature simulation models and lookup tables in the control algorithms. These are illustrated in Figure 5.5 C) and D). Collectively, the data in Figure 5.5 provides a base reference for all power and temperature calculations in simulations.

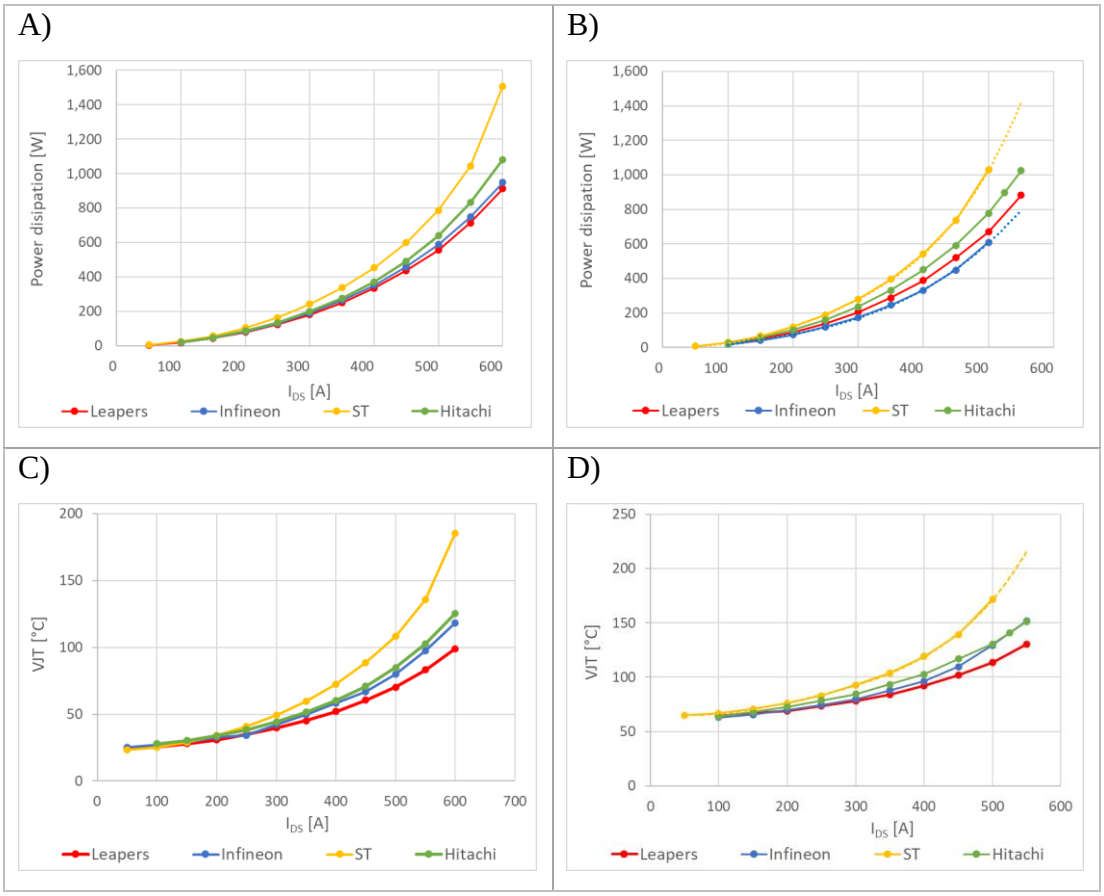

Figure 5.5. Power dissipation and Virtual Junction Temperature (VJT) of power modules as I_{DS} current is increased for 25°C (A and C respectively) and 65°C (B and D respectively) coolant temperature.

5.1.2 Switching Losses Validation

The experimental validation of the work described in Chapter 4.2.2 is realised using the Double Pulse Test [127]. Being a relatively well-known and mature test method [128], it is commonly applied to profile the parameters of power semiconductors, specifically around the switching behaviour of the device, specifically- turn-on delay time, rise time, turn-off delay time and the fall time which are mainly affected by the parasitic capacitance and inductance in the device and the working circuit. The recovery current amplitude and rate of change of the freewheeling diode can also be measured, providing a very comprehensive understanding of the whole power module. Due to its usefulness, this test method has been adapted by various organisations to cater to their test needs. Some examples of these in automotive and industrial electronics space are as presented in [129] where the trace/loop inductance are measured and compared to simulations at the layout stage of the design process and in [130] where some special properties such as dR_{DSon} during ZVS is compared against hard switching, ZVS turn on loss and dynamic reverse voltage drop are measured on a GaN cascode. The method employed here is closer to [131] where the power dissipation during turn on and off of a SiC MOSFET in a controlled experimental environment is measured and compared against simulation fed by manufacturer data.

Experimental Procedure

The DPT rig is set up as shown in Figure 5.6. The test is done using an inductor to replicate hardware parameters within the converter design and two voltage pulses with varying pulse widths [132] according to parameters found in Table 13.

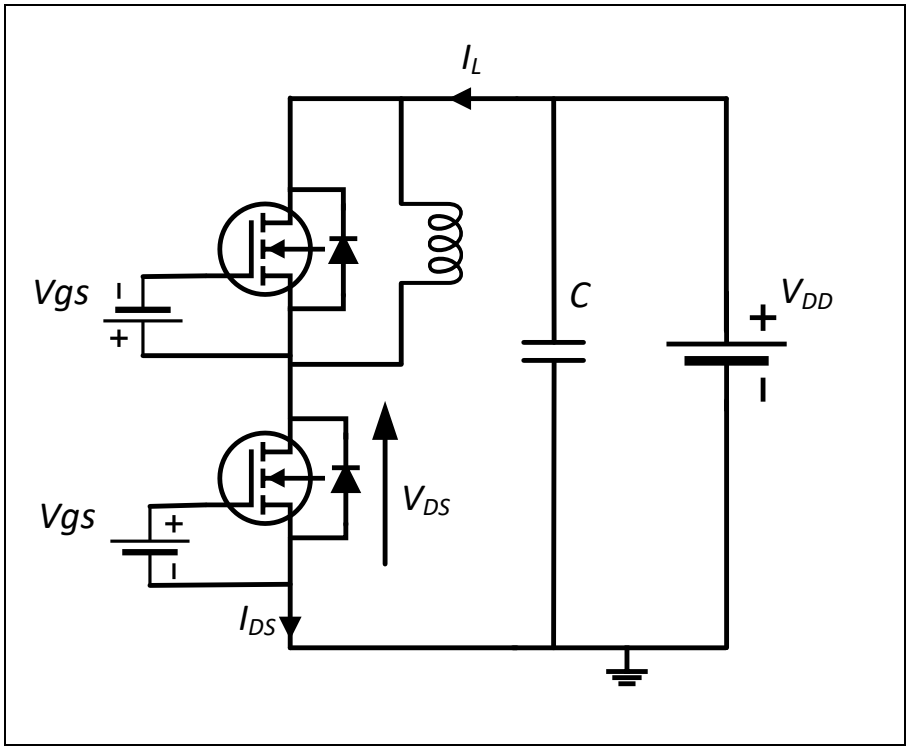

Figure 5.6. DPT hardware setup.

Table 13
SWITCHING LOSSES TEST PARAMETERS

Test parameter	**Value**
Modulation Technique	Sinusoidal PWM
L_{Load}	20μH
Power Factor	0.85
Modulation Index	0.8
DC link voltage, V_{DC}	750V
Coolant temperature, T_{cool}	65°C
Flow rate	10L/min
Switching frequency, F_{SW}	3-10kHz
Current, I_{DS} (RMS)	100-600A

The following equations are used to calculate the energy losses during the turn on and turn off transitions:

$$E_{ON} = \int_0^{t_{on}} V_{DS} I_{DS} dt \quad (39)$$

$$E_{OFF} = \int_0^{t_{off}} V_{DS} I_{DS} dt \quad (40)$$

To calculate the turn off parameters, timing between the falling edge of the first pulse and the rising edge of the second pulse is taken according to Figure 5.7 where,

$t_{d(on)}$: time interval between V_{gs} at 10% of its peak and V_{DS} at 90% of its peak amplitude.

t_r: Time interval between V_{DS} at 90% and 10% of its peak amplitude.

$t_{d(off)}$: time interval between V_{gs} at 10% of its peak and V_{DS} at 90% of its peak amplitude.

t_f: Time interval between V_{DS} at 90% and 10% of its peak amplitude.

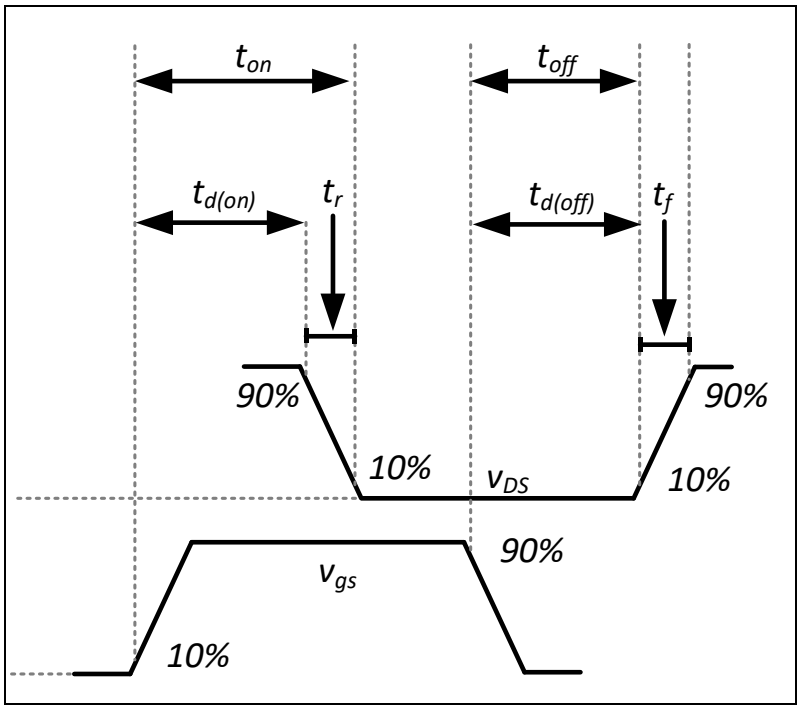

Figure 5.7. Industry standard to measure turn-on and turn-off parameters [132].

Results Discussion

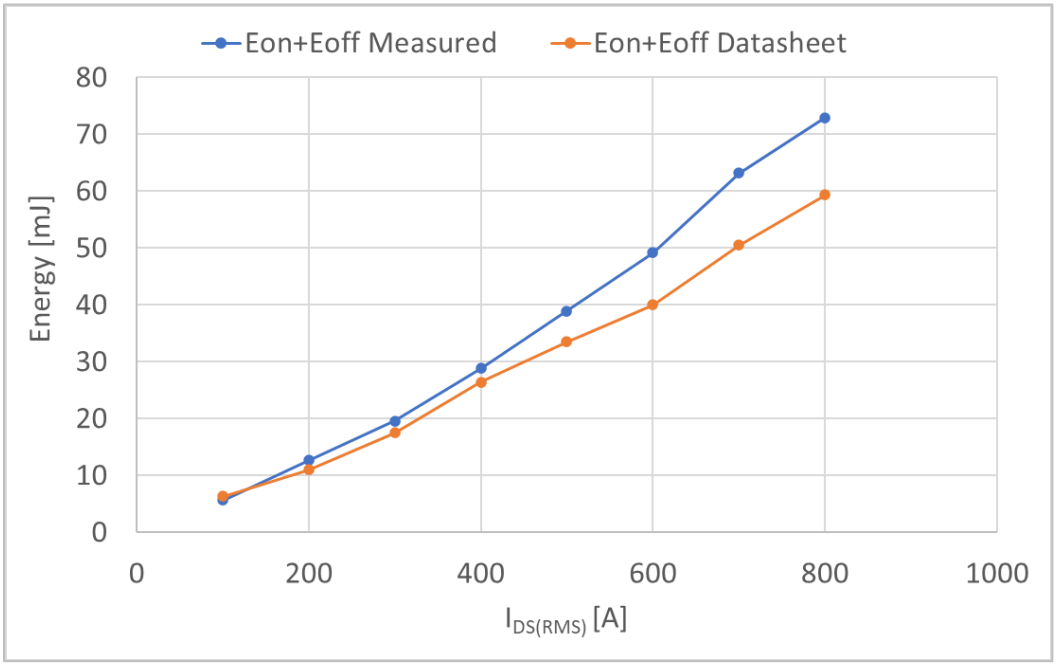

Figure 5.8. Datasheet vs. measured Leapers SiC DFS02FB12HDW1 HYBRIDPACK sum switching energy emissions at V_{DC} =600V, T_J=25°C.

The unidirectional switching losses as a sum of turn on (39) and turn off (40) energy dissipation over various I_{DS} at 600V for the Leapers power module is shown in Figure 5.8. It is observable that the measured data shows a steeper rise as current is increased. This is due to due to the higher inductance within the commutation loop [133] due to connected devices such as the load inductor, L_{LOAD}, bus bars and the DC link assembly. However, both experimentally obtained measurement data and provided manufacturer data show a close relation therefore validating the hardware for use in further testing of modules from other manufacturers, Infineon, ST and Hitachi.

As each power module manufacturer implements their proprietary technologies and manufacturing practices, the resulting switching behaviour at load is expected to be different. As described in Equation (15), switching loss, P_{SW} has a linear relation to switching frequency, F_{SW}.

Therefore, to gain a deeper understanding of the loss profile, switching losses are compared for two values of switching frequency, 3kHz and 10kHz, shown in Figure 5.9 and Figure 5.10 respectively.

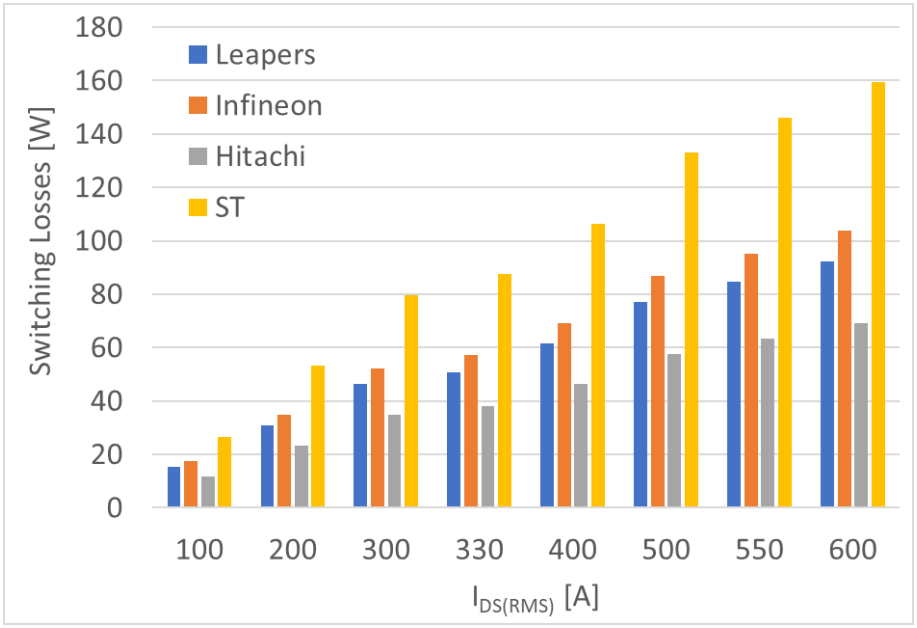

Figure 5.9. Tabulated switching losses for V_{DC} = 700V, F_{SW}= 3kHz for I_{DS} range : 100-600A

Figure 5.10. Tabulated switching losses for V_{DC} = 700V, F_{SW}= 10kHz for I_{DS} range : 100-600A

Although the results in the two figures initially favour the Hitachi power module at both extremes of switching frequencies, other factors such as heat sinking capability and module lifetime at temperature have to be taken into account when making a device selection, as these depend on the material choice and hardware design of the power module. The Double Pulse Testing may be repeated with the exact values of parasitic inductance as in the final production converter for better accuracy in the results.

5.2 Multiport Converter Test Setup

To verify the proposals and theoretical analysis presented in chapters preceding, a full-scale production- ready prototype multiport converter is tested within multiple different operational scenarios. This section presents the experimental results obtained within a laboratory environment which are compared to simulation results.

The test rig set up consisted of a multiport converter (Figure 5.11 A and B), an energy storage unit (Figure 5.11 D)- comprising of a 286Wh ultracapacitor bank and emulated vehicle driveline components- low voltage resistive load bank representing vehicle hotel loads and a load machine (Figure 5.11 C) replacing the engine.

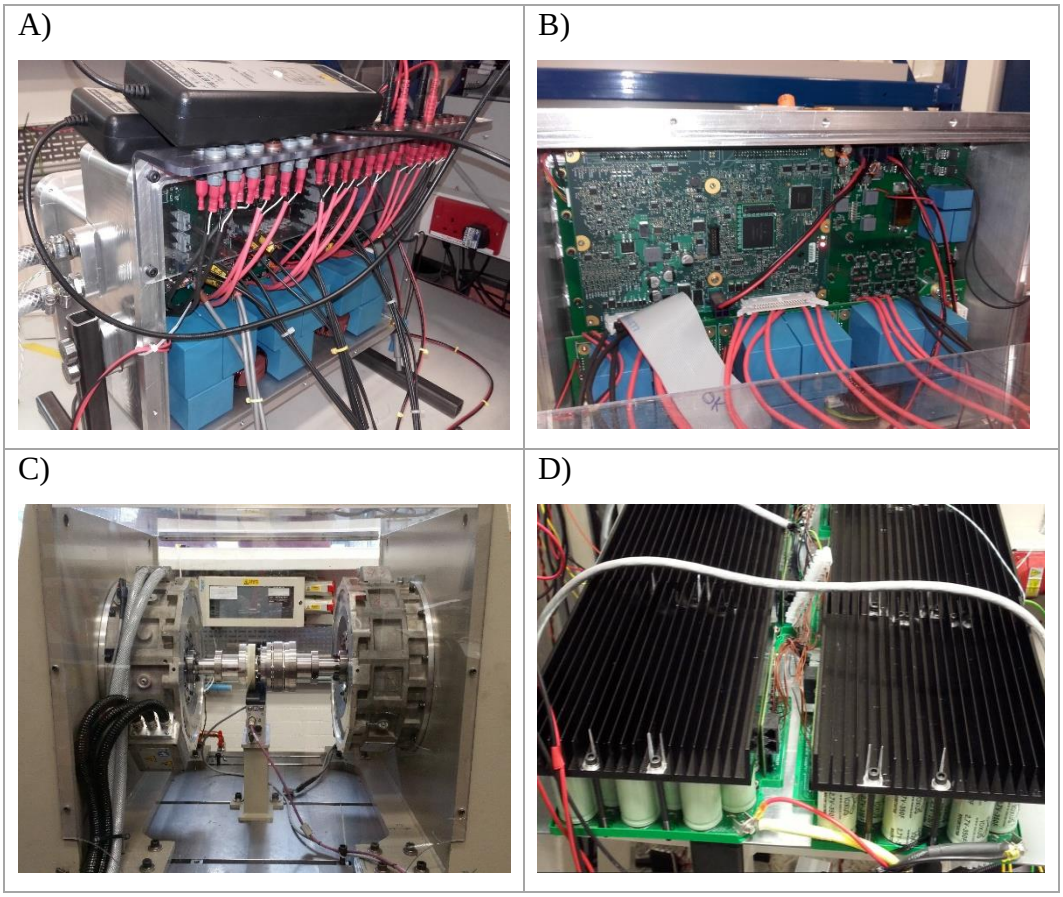

Figure 5.11. A) Multiport converter (D.U.T), B) Test instrumentation connections and converter controller, C) Back-to-back PMSM test bed and D) ultracapacitor bank during validation tests.

The experimental setup is ensured to provide complete test capabilities to validate every performance index of the multiport converter, the device under test (DUT). As illustrated in Figure 5.12, a Load motor driven by a Semikron SKAI II inverter and resistive load bank are used to emulate existing driveline components- the engine and 24V electrical bus respectively. The experimental tests were carried out with the exact Ultracapacitor bank performing the role of the Energy Storage device in the system, acting as the energy source during motoring events and storing energy during regenerative events.

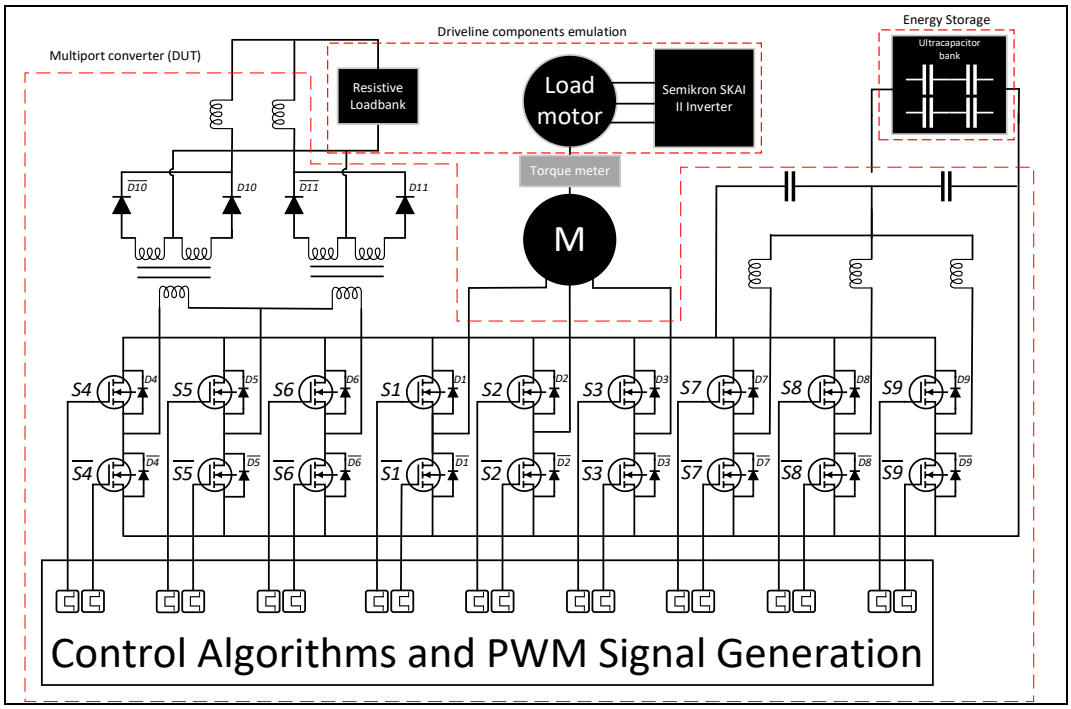

Figure 5.12. Multiport converter test setup.

The inverter and dcB are critical to enable Engine Run, Shutdown and Restart modes within the vehicle, as described in Figure 5.13 and Table 14. The converter pair realises this through two main modes of operation:

1) Motoring/boost – machine torque production in the same direction as machine rotation. Power flow direction from energy storage to machine.
2) Generating/buck - torque opposing direction of machine rotation. Power flow direction from machine to energy storage.

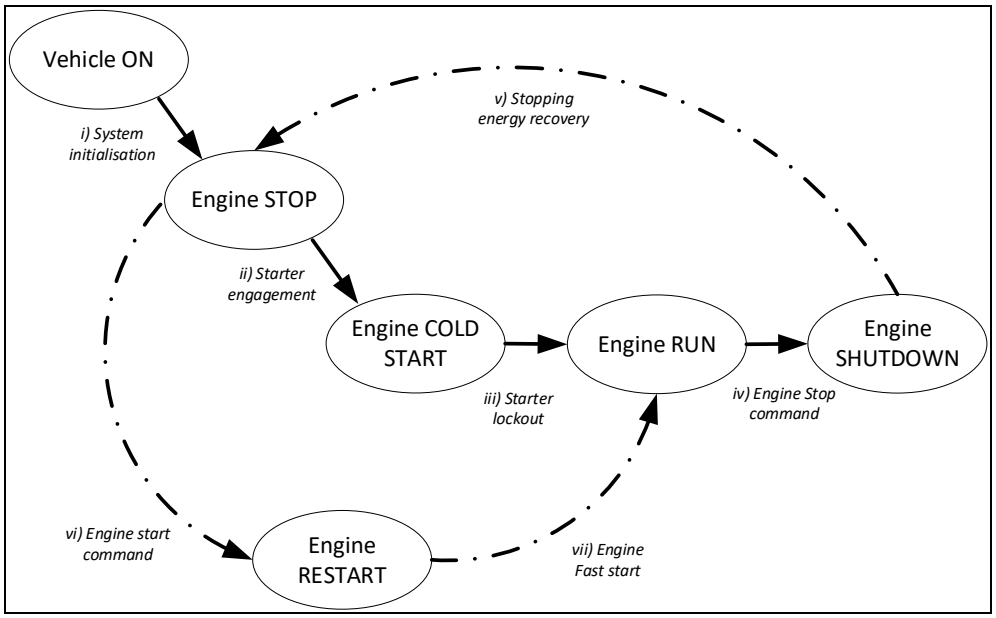

Figure 5.13. Hybrid drivetrain mode transitions.

Table 14
DRIVELINE MODE DESCRIPTION

Mode	Description
Vehicle ON	All system controller modules boot and in ready state. Multiport converter controller requests contactors close and pre-charge DC link (i). Inverter and PMSM in Standby.
Engine STOP	Engine and Inverter in Standby. System ready to start engine using ii) starter motor for cold start or vii) hybrid system for fast restart. Ultracapacitor energy is used to support LV battery and vehicle hotel loads- dcB in boost mode and dcA enabled.
Engine COLD START	Conventional engine start applied using low voltage starter (ii). On completion of engine crank, low voltage starter is locked out (iii) for remainder of the run cycle.
Engine RUN	Vehicle-in-motion. Engine speed> idle (700RPM). Engine in drive mode. Multiport converter controller calculates available electrical power according to engine power vs speed curve. Inverter and dcB enter regeneration/buck to charge the energy storage.
Engine SHUTDOWN	Vehicle stopped. Multiport converter sends engine shutdown request (iv). Engine begins shutdown routine. Hybrid system recovers energy and prepares for subsequent fast restart (v).
Engine RESTART	Hybrid system provides torque to crank to restart engine in less than 1s (vii).

In both operational modes, the inverter and dcB operate on a combination of optimisation schemes, realised through the fundamental closed loop control schemes shown in Figure 3.4 and Figure 3.7 respectively.

The Isolated Buck converter, dcA only operates in Buck mode in supplying accessory loads on the vehicle and charging the low voltage battery according to charging characteristic [134] as an alternator replacement. Therefore, the power flow within this device is only unidirectional throughout the operation of the vehicle. This enabled a much simpler control scheme as shown in Figure 3.5.

Given the control topologies of all three converter modules were based on the conventional cascaded PI controller configuration, the design process from implementation to commissioning is simplified. Gain selection of all controllers is performed as described in Chapter 3 considering that the sampling frequency of the outer voltage loops and inner current loops were always tied to the switching frequency. This ensures the highest controller bandwidth and therefore robustness against disturbances and transients. As all three converters operated with switching frequences which were integer multiples of each other, the switching periods could also be synchronised, enabling optimisations based on phase shifting of converter legs as described in Chapter 3.

5.2.1 Engine RESTART

During Engine RESTART, the peak motoring torque of 350Nm causing maximum current to be applied to the power devices of inverter momentarily. As dcB and the inverter are nearing their respective maximum power capability, dcA is commanded to stop switching to reserve complete utilisation of the DC link to the engine restart operation. This ensures the most efficient and fastest restart of the engine possible. Once sufficient speed has been achieved, the engine speed governor begins engine fuelling and takes control of engine speed. This transition point is marked as point vii) in Figure 5.13 and is completed just before Engine RUN mode. To verify the effectiveness of the schemes employed within the inverter, simulations are carried out in MATLAB/SIMULINK environment. The results are compared with those obtained experimentally as illustrated in Figure 5.14.

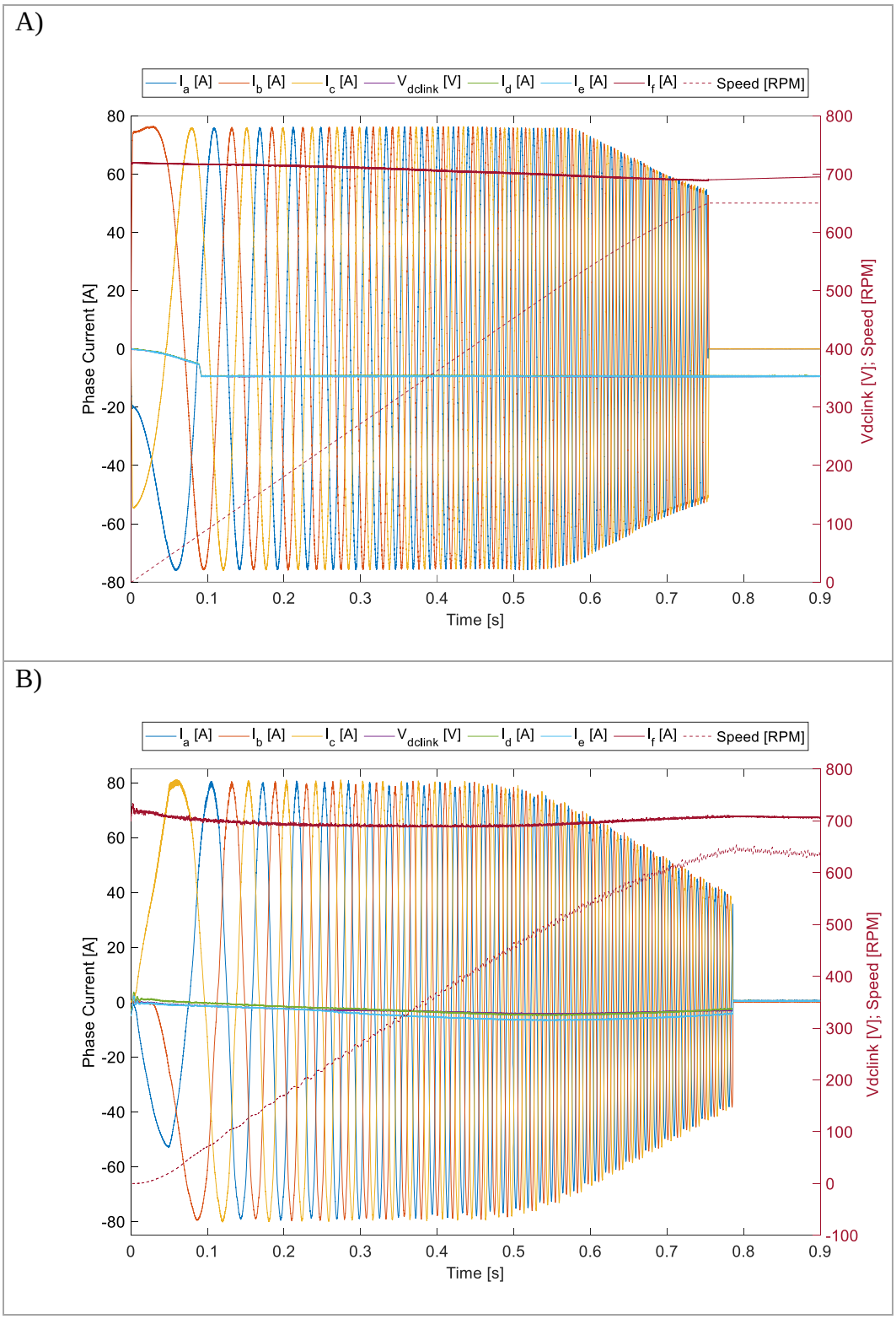

Figure 5.14. Speed, voltage and current profile of multiport electric drive during Engine Restart (Inverter-Motoring, dcB- Boost). (A) Simulated Results: Inverter current, I_{abc}, DC link voltage, machine speed and dcB current, I_{def} in motoring mode. (B) Experimental Results: Inverter current, I_{abc}, DC link voltage, machine speed and dcB current, I_{def}.

It can be observed in Figure 5.14 (A) and (B), that for equal values of phase currents, the resultant torque is the same and therefore the acceleration of the shaft to 600RPM follows an almost identical profile between simulation and experimental environments validating not only the electrical parameters but also the Multiphysics impact within the thermal (junction temperature increase) and mechanical (inertial load and windage losses) domain.

Some discrepancies are seen between simulated and experimental data. Firstly, the peak phase current applied by the inverter is larger experimentally versus simulation. Next, the time taken for the rotor to reach 650 RPM- 0.75s in simulation and 0.79s on the experimental rig. This can be attributed to multiple factors:

1) Different current controller accuracy where due to more idealistic conditions in simulation, the PI controller is able to track I_{dq} references more closely giving better overall tracking of the MTPA profile of the PMSM – see Figure 3.2 and equation (5). Therefore, a lower peak phase current is required for the same amount of torque.
2) Errors in machine parameters, primarily flux linkage between the stator and rotor due to inaccurate rotor temperature and/or magnetic model. Studies presented in [135], [136] show the effect of magnetic path saturation and cross coupling due to the structural design of the PMSM causing non-linearity of the MTPA profile. Despite detailed FEA analysis of the PMSM design, some of these effects may have inaccuracies which cause differences in peak current for a certain torque request and acceleration time.
3) Inaccuracies in simulated mechanical properties of the complete drive system such as moment of inertia and friction torque coefficients [137]. The simulation model considers a linear inertia profile for simplicity which discount effects such as windage, bearing oil viscosity, magnetic cogging due to the load PMRM and twisting of the driveshaft which cumulatively affect the mechanical properties of the load.

Finally, dcB phase current amplitudes in Figure 5.14 (B) are imbalanced as compared to Figure 5.14 (A). This can be attributed to electronic circuit tolerances present in the hardware which are not observable in the idealised simulated counterpart.

5.2.2 Engine RUN

As illustrated by the flow chart in Figure 5.13, once the minimum required crank speed is achieved, the system transitions over to Engine Run mode where the inverter operates in Regeneration mode. Here, the machine is operated in regeneration mode with the engine power limits governing the maximum current drawn by the inverter, and dcB in Buck mode, each assuming control of DC link and energy storage voltage respectively. DcA is activated to charge and assist the low voltage Lead Acid battery with vehicle loads. Experimental tests, pictured in Figure 5.15 are carried out to verify good regulation of Inverter and dcB phase currents, I_{abc} and I_{def} respectively, dcA output voltage, V_{LV} and current, I_{LV} and DC link voltage, V_{dclink} as machine speed increases.

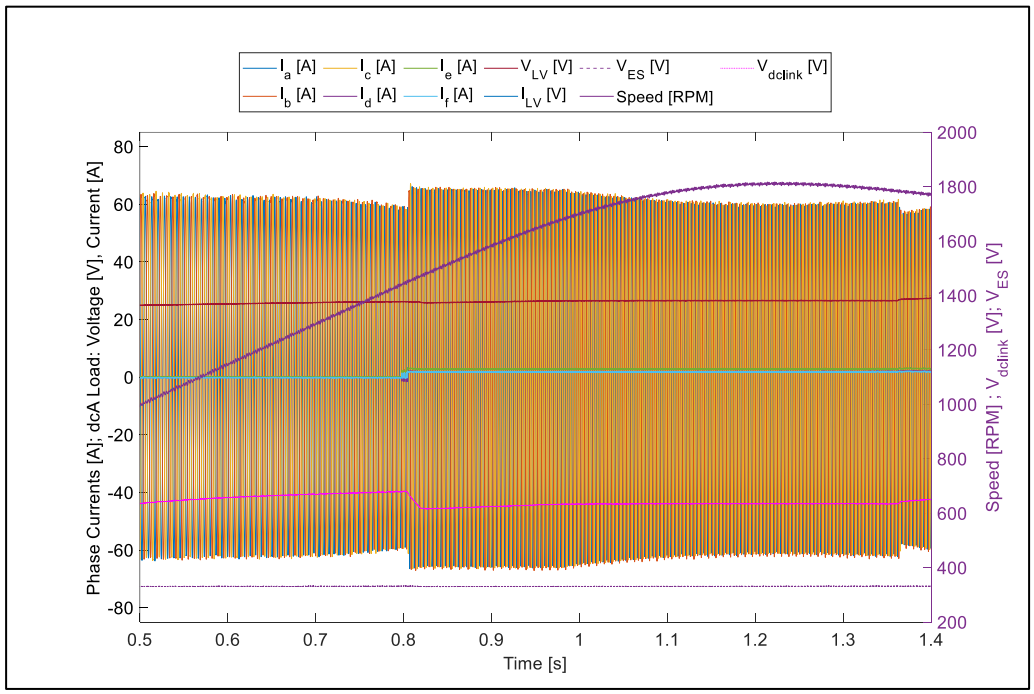

Figure 5.15. Experimentally measured phase currents of Inverter in regeneration mode, phase currents of dcB in Buck mode and output current of dcA in Buck mode.

While investigation into DC link voltage regulation requires analysis of the entire speed range as presented in Figure 5.15, a more detailed inspection of the parameters within the inverter, dcB and dcA is performed to ensure cohesiveness between simulation and experimental results. To this end, a time range between 0.74s and 0.84s is selected. Comparisons of the multiport converter operational parameters are presented in Figure 5.16-Figure 5.18.

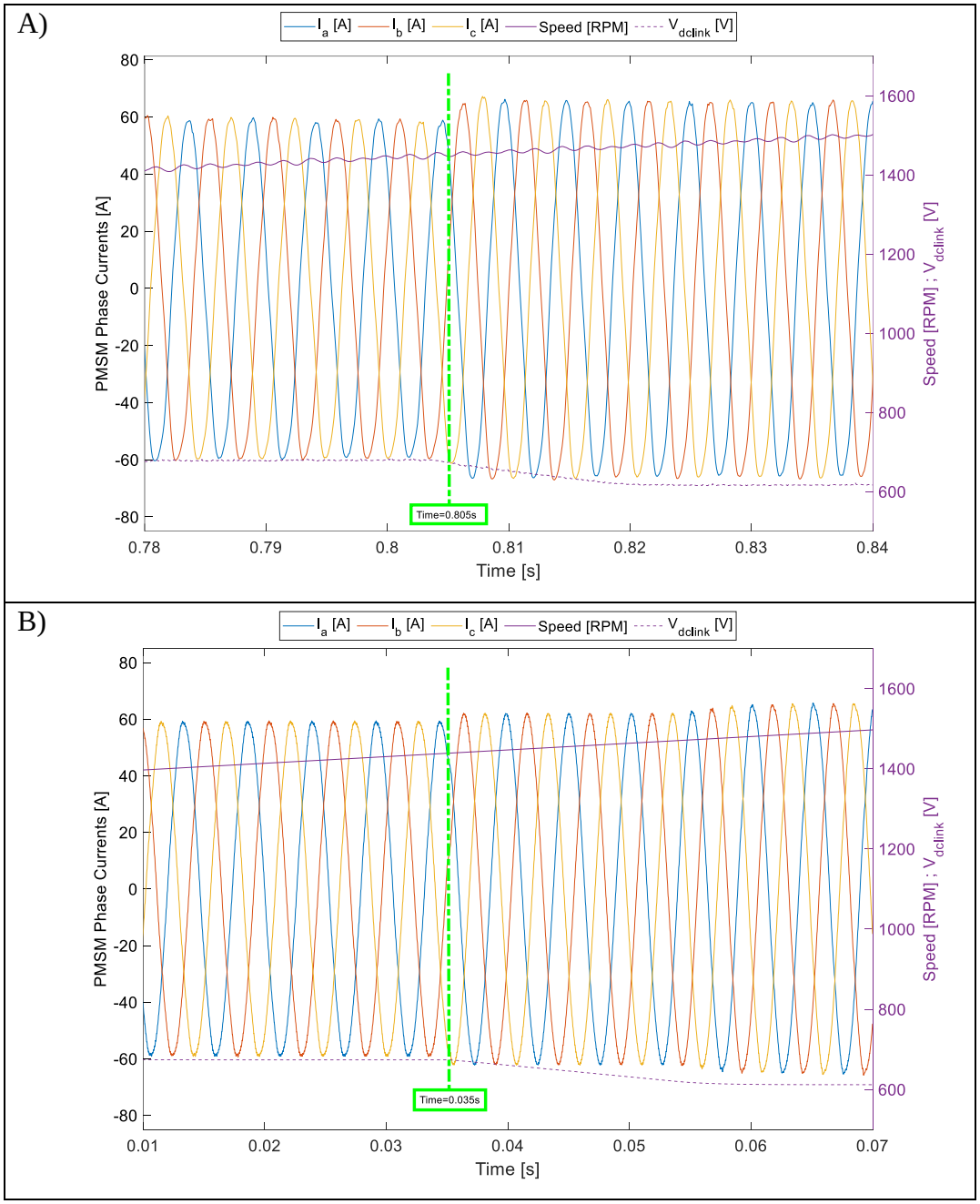

Figure 5.16. Experimental (A) and Simulated (B) inverter phase currents as DC link voltage and speed are varied during PMSM acceleration event.

The test is repeated using the simulation model (Figure 5.16 B) to assess coherence to the hardware. Similar behavioral relationship between simulation and experimental results presented in Chapter 5.2.1 are observed; whereby the PMSM phase currents in the simulated model is lower than experimental results (Figure 5.16 A). This would have been for the same reasons of current controller, PMSM tolerance and mechanical configuration which have been discussed at length. Both experimental and simulated data however show the expected increase in phase current reflecting the increase of i_d current demand as speed increases. The voltage on the DC link, V_{dclink} is controlled by adjusting the torque request. Applying equation (5) and accounting for the amplitude of i_d required for field weakening, the i_q reference is derived. Both current references are tracked by the current controllers in the inverter controller, giving a stable V_{dclink} throughout.

Differences between experimental results (Figure 5.17 A) and simulation (Figure 5.17 B) are prominent in dcB currents at the same test point. Although the cleaner measurement in the simulated converter shows a small current imbalance between the three phases, current I_e is clearly larger than currents I_d and I_f in the experimental data (Figure 5.17 A).

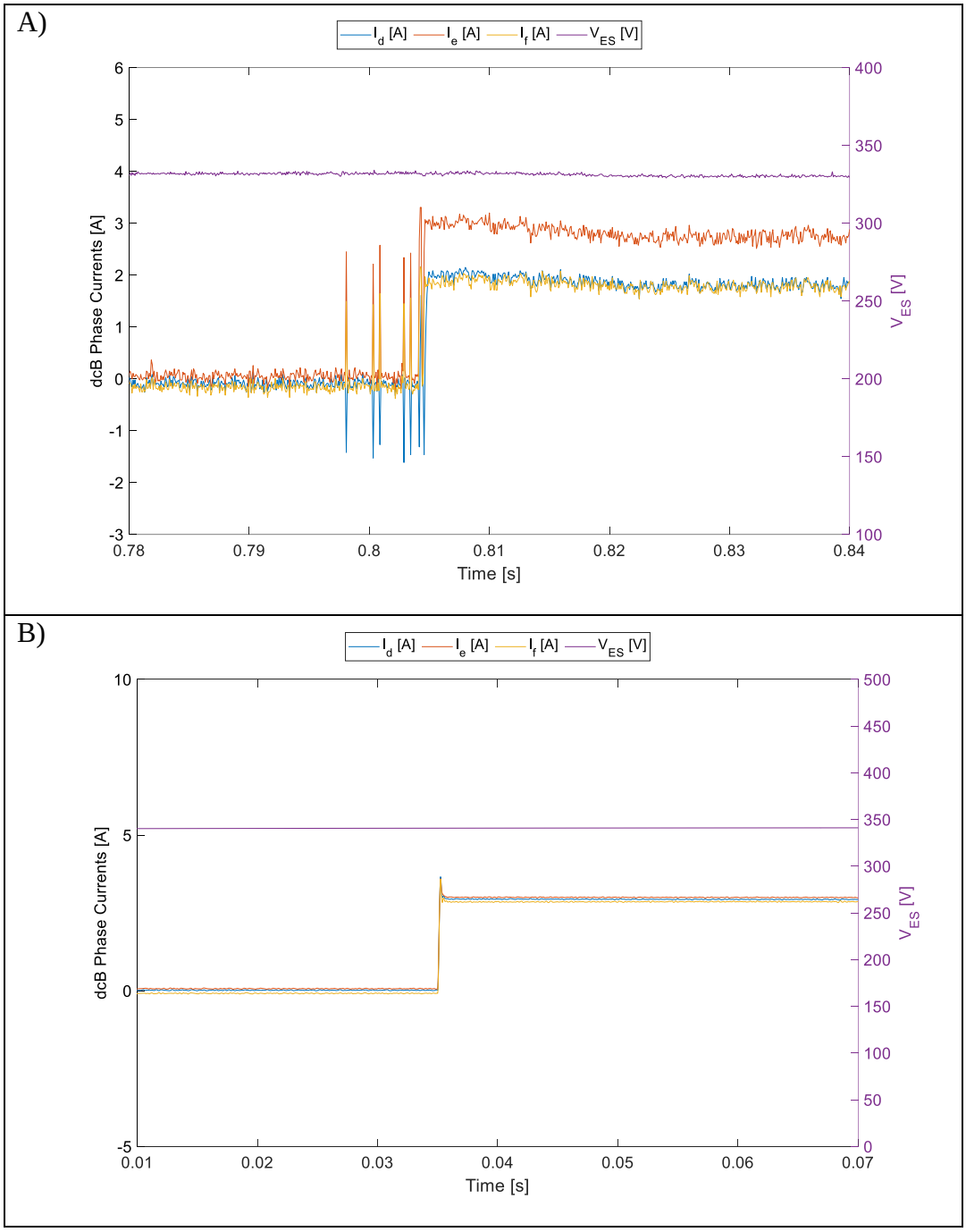

Figure 5.17. Experimental (A) and Simulated (B) dcB phase currents as DC link voltage and speed are varied during PMSM acceleration event.

The current imbalance is observed across all 5 prototype converters with different phase bearing the higher current in each converter. Therefore, it is determined to be a result of inductive and resistive mismatch due to device tolerances and converter design- a common issue faced by the industry with parallel connected power devices [138]. Parallel power device topologies are more common in DCDC converter design and therefore solutions have been presented to actively balance the current to avoid unequal heating effects leading to premature device failure as presented in [134-135]. As power cycle tests performed on the multiport converter power modules [141] showed that the devices would meet the design lifetime despite the imbalance, the decision was made to resolve the current imbalance in the future as an iterative design improvement.

The principle of operation within dcA requires that both phases are wound isometrically around a single isolation transformer instead of relying on independent inductors on each phase leg. This enables a more even distribution of load compared to dcB which is therefore achieved through design.

The resultant load current is presented in Figure 5.18. It is observed that, even as V_{dclink} is reduced, dcA voltage and current controllers maintain regulation of the 8.4kW load made of hotel load support and 24V battery charging. The load is reduced to 7.8kW as the DC link voltage is reduced to emulate a reduced hotel

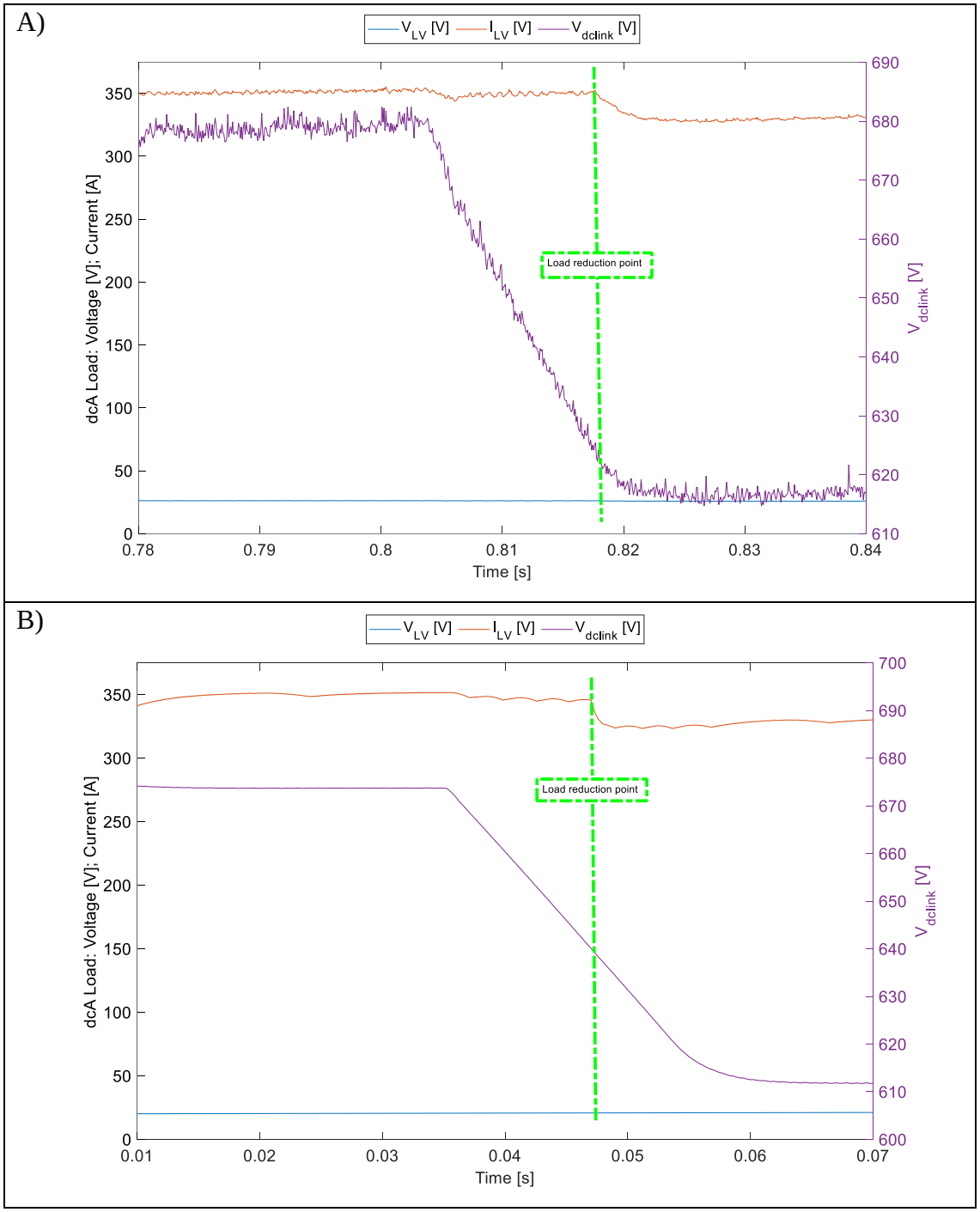

Figure 5.18. Experimental (A) and Simulated (B) dcA load current as DC link voltage and speed are varied during PMSM acceleration event.

load demand as indicated by the green line in Figure 5.18. Simulation and experimental data show that V_{dclink} voltage and dcA load current and voltage changes are achieved with 0% overshoot and nearly identical voltage and current values.

During steady-state operation of dcA and dcB, it is observed in Figure 5.17 and Figure 5.18 that the DC link voltage is kept within the design limit of +-10% throughout the operating speed range of the electrical machine (up to 1800RPM). The close corelation proves sufficient controller and plant model accuracy for further model-based efficiency mapping and for vehicle performance baseline work (pictured in Figure 5.19).

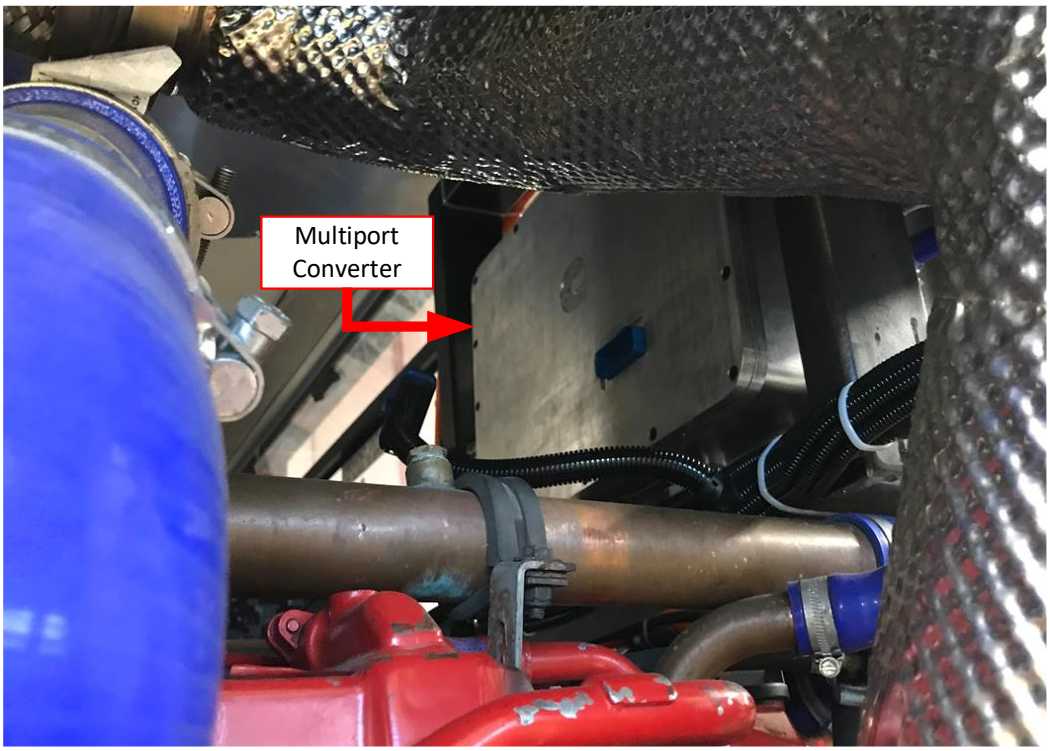

Figure 5.19. A full-scale production-ready Multiport converter mounted in the engine compartment of the test vehicle for vehicle performance baseline testing.

Chapter 6

Conclusions

A comprehensive literature review regarding the state of the vehicle electrification and the motivating factors behind governmental policies and milestone setting has been presented, making clear that the demand for high power density, efficiency, reliability and fault tolerant automotive power electronics has been growing over the last decade and will continue to do so with an accelerated pace in the future.

After systematically reviewing present-day automotive power electronic manufacturer trends in hardware and software design, a multiport converter design for a hybrid London Bus route application is presented. The main difference between the traditional discrete converter approach and a multiport converter is the level of integration in the design: where multiple converter stages are combined into one physical structure, sharing components such as cooling plates, the DC link and microcontroller.

6.1 Summary of Achievements

One of the aims of the thesis is to investigate the multiport converter design to maximise efficiency and power density in order to fully harness the benefits of an integrated design or, more specifically, to take into account key parameters which influence performance for a targeted approach to improving design. With that aim, the Multi-Objective Optimization (MOO) approach is proposed to evaluate innovative control schemes against the State-of-the-art. Without the coverage of simultaneous evaluation provided by the MOO tools, the multi-dimensional optimisation cannot be performed due to the limited information provided by a

single optimisation scheme or solution. Herein lies the novelty in this work whereby the state-of-the-art approach of optimising multiple singular converters for various functions of a hybrid electric drivetrain is replaced by a single multiport converter with all modules and components collectively optimised, bringing feature enhancements never seen before on electrified public transport applications.

A ground up design philosophy is hereby followed, starting with power module loss verification. Once the lost elements were identified, power module experimental validation was carried out to ensure coherency of the simulation tools in use. On completion of this stage, module parameter data is inserted into MATLAB/PLECS simulation model of the complete multiport converter for full operational sweeps to be carried out. Since the choice of model can affect the precision in estimation and therefore the outcome of the MOO analysis, the execution of the power electronic and magnetic models was verified using loss calculation methods found in literature. Here, the MOO tool is used to identify and prioritise key factors within the operation of the converter affecting the performance indices- efficiency, machine current THD and DC link capacitor current for the entire operational torque speed range of the driveline.

Given the MOO analysis showed switching frequencies of the 3 converters and the shared DC link voltage as critical factors that affect the performance indices, they are set as optimisation objectives. Simulation sweeps are then carried out to identify parameter values that provide optimal performance. The identified parameter values are implemented within the controller as part of an optimum performance algorithm whereby the controller will adjust the switching frequencies and DC link value according to its current and predicted next operational point. For further enhancement of this scheme, two optimisation techniques from literature are employed. Firstly, Phase Deactivation where the number of operational DCDC converter phases is adjusted according to the load, resulting in better efficiency. Secondly, the Phase Displacement is used to offset the carriers of the inverter and dcB providing the lowest DC link capacitor current for each operational point. Here, the MOO shows itself to be an invaluable tool in ensuring that all

performance indices are achieved, respecting the correlations between them. The validation of the MOO performance benefits is executed using a Pareto Analysis. It is shown for the given design space consisting of vehicle parameters and optimisation parameters, when compared against conventional techniques, the highest efficiency is always achieved for every operational point. An interesting finding was that the MOO was also useful in considering trade-offs between optimisation techniques, whereby optimum inverter switching frequency was prioritized over the execution of the Phase Displacement technique for better system efficiency at a particular operational point.

Finally, the components are assembled and 5 fully functioning multiport converter prototypes are built. The converters then enter multiple stages of experimental validation and tests prior to vehicle deployment. The close agreement between the measured and simulated performance proves multiple points, firstly, that the converter design is capable of meeting the vehicle requirements. Secondly, that the hardware is accurately represented in the simulation model and therefore granting credence to the corresponding MOO and Pareto Analysis. Lastly, the proposed optimisation scheme can indeed deliver the performance improvements if the conditions imposed in simulation are met.

All in all, this work confirms how important and necessary the optimisation study of the multiport converter approach is to fully utilise the full potential of the integrated design and reach an innovative, robust, high efficiency and high power density solution.

6.2 Proposals for future work

Some limitations were encountered during the execution of the work presented in this thesis, indicating potential for further research work:

- Measurement and modelling of exact circuit parameters such as parasitic inductance of busbars and DC link PCB for even higher simulation fidelity of switching behaviour.
- Replacing the PI controllers with Model Predictive Control (MPC) [142], [143]. As presented in Chapter 3, PI controllers routines are usually executed once every switching cycle to provide sufficient control bandwidth. MPC algorithms do not have this requirement and therefore can provide good controllability at lower switching frequencies, and therefore further reduce switching losses.
- Incorporation of machine and converter hardware design into MOO Analysis resulting in optimised hardware to meet the software.
- Application of the presented approach on a high-power converter. Converters within pure Electric Vehicles (EV) for example, typically have higher electrical ratings and efficiency requirements than their Hybrid counterpart as the electric drivetrain is the only source of torque. A replication or improvement of the 6% efficiency gain presented in this thesis within an EV would directly translate into vehicle travel range and therefore be very valuable.
- Application of more accurate power module loss measurement techniques, such as calorimetric validation [144].
- Due to time and cost limitations, the complete optimisation strategy was not validated on-vehicle. In the future it is proposed that on-vehicle calibration tasks include configuration of the optimisation strategy and verification within the real operational environment that the converter was designed for.

Appendix A

Peer-reviewed publications

1) **Choy, Wei Juin** & Costabeber, Alessandro & Buticchi, Giampaolo & Trentin, Andrew & Walker, Adam & Galea, Mikiel & Paciura, Krzysztof & O'Brien, John & Palmer, Bradford. (2021). A Multiport Power Electronics Converter for Hybrid Traction Applications. IEEE Access. PP. 1-1. 10.1109/ACCESS.2021.3089371..
2) **Choy, Wei Juin** & Buticchi, Giampaolo & M. Alcaide, Abraham & Galea, Mikiel & Leon, Jose. (2021). Optimized Phase-Shift Control for dc-link Current Minimization in Automotive Multi Converter Applications. 01-04. 10.1109/eGRID52793.2021.9662129.
3) Zhou, Xuanyi & **Choy, Wei Juin** & M. Alcaide, Abraham & Wang, Shuo & Guenter, Sandro & Leon, Jose & Monopoli, Vito Giuseppe & Franquelo, Leopoldo & Liserre, Marco & Galea, Mikiel & Gerada, Chris & Buticchi, Giampaolo. (2023). Common DC-Link Capacitor Harmonic Current Minimization for Cascaded Converters by Optimized Phase-Shift Modulation. Energies. 16. 2098. 10.3390/en16052098.

Appendix B

PMSM current, flux and voltage derivations

Given the relation of phase currents in the abc frame relation to the dq0 frame:

$$\mathrm{i_d} = k_d\left[i_a cos\theta + i_b cos\left(\theta - \frac{2\pi}{3}\right) + i_c cos\left(\theta + \frac{2\pi}{3}\right)\right] \tag{41}$$

$$\mathbf{i_q} = -\boldsymbol{k_d}\left[\boldsymbol{i_a sin\theta} + \boldsymbol{i_b sin}\left(\boldsymbol{\theta} - \frac{\boldsymbol{2\pi}}{\boldsymbol{3}}\right) + \boldsymbol{i_c sin}\left(\boldsymbol{\theta} + \frac{\boldsymbol{2\pi}}{\boldsymbol{3}}\right)\right] \tag{42}$$

With k_d and k_q equal to 2/3 for balanced sinusoidal conditions,

$$i_a = I_m sin\omega_s t$$

$$i_b = I_m sin\left(\omega_s t - \frac{2\pi}{3}\right)$$

$$i_c = I_m sin\left(\omega_s t + \frac{2\pi}{3}\right)$$

Substituting in ((41),

$$\begin{aligned}\mathrm{i_d} = k_d\Big[&I_m sin\omega_s t cos\theta + I_m sin\left(\omega_s t - \frac{2\pi}{3}\right) cos\left(\theta - \frac{2\pi}{3}\right)\\ &+ I_m sin\left(\omega_s t + \frac{2\pi}{3}\right) cos\left(\theta + \frac{2\pi}{3}\right)\Big]\\ =&k_d \frac{3}{2} I_m sin(\omega_s t - \theta)\end{aligned}$$

Similarly, from (42),

$$i_q = -k_q \frac{3}{2} I_m cos(\omega_s t - \theta)$$

A convenient third variable is the zero sequence current i0, associated with symmetrical components:

$$i_0 = \frac{1}{3}(i_a + i_b + i_c)$$

Under balanced conditions $i_a + i_b + i_c = 0$ and therefore, $i_0 = 0$

The transformation from abc phase variables to the dq0 variables can be written in the following matrix form:

$$\begin{bmatrix} i_d \\ i_q \\ i_0 \end{bmatrix} = \frac{2}{3}\begin{bmatrix} \cos\theta & \cos\left(\theta - \frac{2\pi}{3}\right) & \cos\left(\theta + \frac{2\pi}{3}\right) \\ -\sin\theta & -\sin\left(\theta - \frac{2\pi}{3}\right) & -\sin\left(\theta + \frac{2\pi}{3}\right) \\ \frac{1}{2} & \frac{1}{2} & \frac{1}{2} \end{bmatrix}\begin{bmatrix} i_a \\ i_b \\ i_c \end{bmatrix}$$

The inverse transformation is given by:

$$\begin{bmatrix} i_a \\ i_b \\ i_c \end{bmatrix} = \frac{2}{3}\begin{bmatrix} \cos\theta & -\sin\theta & 1 \\ \cos\left(\theta - \frac{2\pi}{3}\right) & -\sin\left(\theta - \frac{2\pi}{3}\right) & 1 \\ \cos\left(\theta + \frac{2\pi}{3}\right) & -\sin\left(\theta + \frac{2\pi}{3}\right) & 1 \end{bmatrix}\begin{bmatrix} i_d \\ i_q \\ i_0 \end{bmatrix}$$

$$\Psi_d = -\left(L_{aa0} + L_{ab0} + \frac{3}{2}L_{aa2}\right) i_d + L_{afd} i_{fd} + L_{akd} i_{kd} \quad (43)$$

$$\Psi_q = -\left(L_{aa0} + L_{ab0} - \frac{3}{2}L_{aa2}\right) i_q + L_{akq} i_{kq} \quad (44)$$

$$\Psi_0 = -L_0 i_0$$

Wherein $L_{aa}0$, L_{ab0}, are the winding self inductance of phase a and mutual inductance between phase a and b respectively. L_{afd}, L_{akq} and L_{akd} are the mutual inductance between the stator and rotor

Stator voltage equations with dq0 transformation applied:

$$v_d = \frac{d\Psi_d}{dt} - \Psi_q \omega_r - R_a i_d$$

$$v_q = \frac{d\Psi_q}{dt} - \Psi_d \omega_r - R_a i_q$$

$$v_0 = \frac{d\Psi_0}{dt} - R_a i_0$$

Where Ra is the armature resistance per phase and ω_r represents the angular velocity of the rotor.

Instantaneous 3-phase power output of the stator is:

$$P_t = v_a i_a + v_b i_b + v_c i_c$$

Eliminating phase voltages and currents in terms of dq0 component gives:

$$P_t = \frac{3}{2}\left(v_d i_d + v_q i_q + 2e_0 i_0\right)$$

Under balanced operation e0=i-=0 and the expression for power is given by:

$$P_t = \frac{3}{2}\left(v_d i_d + v_q i_q\right)$$

The air-gap torque Te is obtained by dividing power by rotor speed in radians per second giving:

$$T_e = \frac{3}{2}\left(\Psi_d i_q - \Psi_q i_d\right)\frac{\omega_r}{\omega_{mech}}$$

$$= \frac{3}{2}\left(\Psi_d i_q - \Psi_q i_d\right)n_p$$

Replacing flux linkage equations (43) and (44) gives:

$$T_e = \frac{3}{2} n_p\left[\Psi_f + \left(L_d - L_q\right) i_d\right]$$

Appendix C

Derivation of Buck Converter Plant Model

Given the generic Buck converter equivalent circuit in Figure C.1, the switch circuit is determined for averaging through a small signal model.

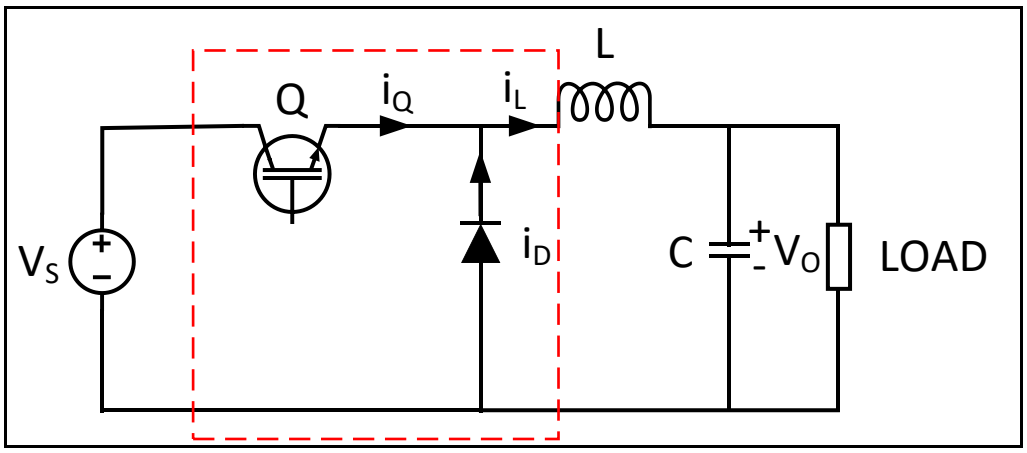

Figure C.1. Buck converter equivalent circuit. Switch circuit marked by red box.

The switch circuit marked by the red box in Figure C.1 is exacted for averaging using an equivalent average switch circuit with controlled sources as illustrated in Figure C.2.

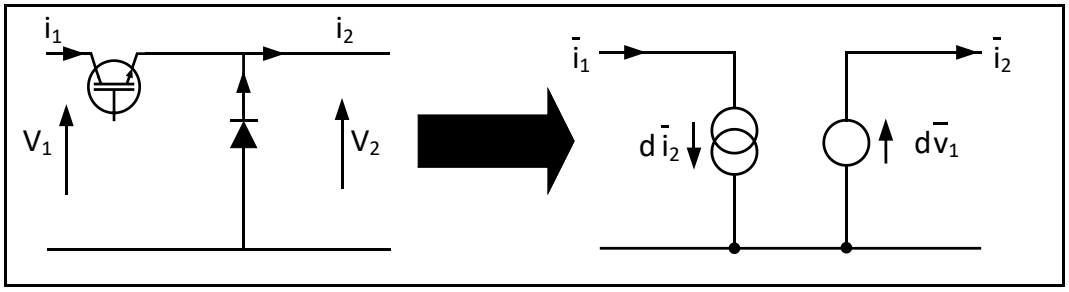

Figure C.2. Extracted switch model (left) and equivalent averaged switch circuit with controlled sources (right).

The inductor current, i_2 is assumed to be linear as illustrated by the red and blue lines in Figure C.3 due to only small variations of the supply and output voltage, V_S and V_O respectively, during the switching period, T.

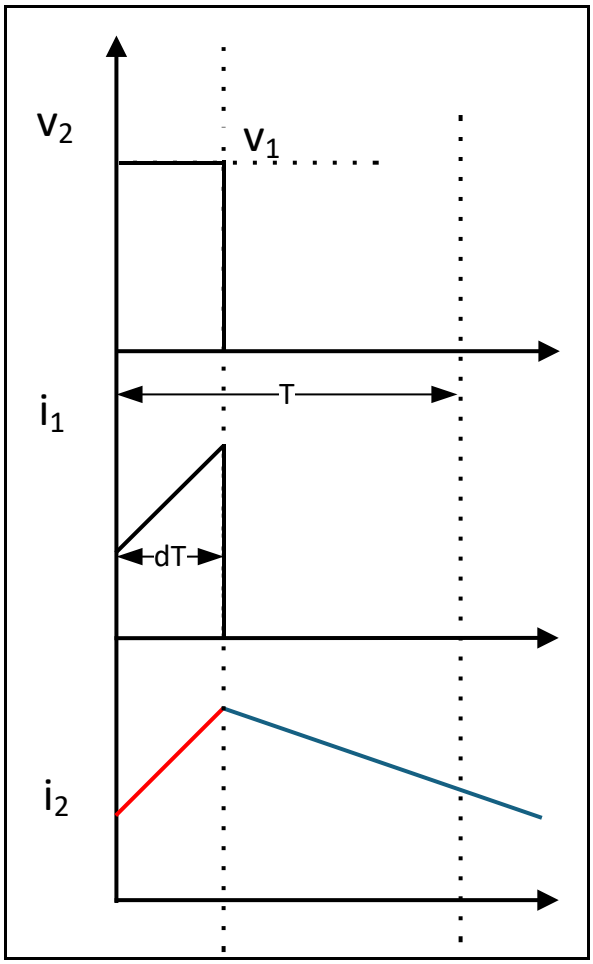

Figure C.3. Buck converter current and voltage waveform during one switching period, T.

From Figure C.3, the relation of output current to input current is derived as:

$$\overline{i_1} = d\overline{i_2}$$

and the relation of output voltage to input voltage is given as:

$$\overline{v_2} = d\overline{i_1}$$

where d is the duty cycle of the main switch, Q.

The equivalent averaged switch circuit is inserted into the section marked by the red box in Figure C.1 giving the final average model shown in Figure C.4.

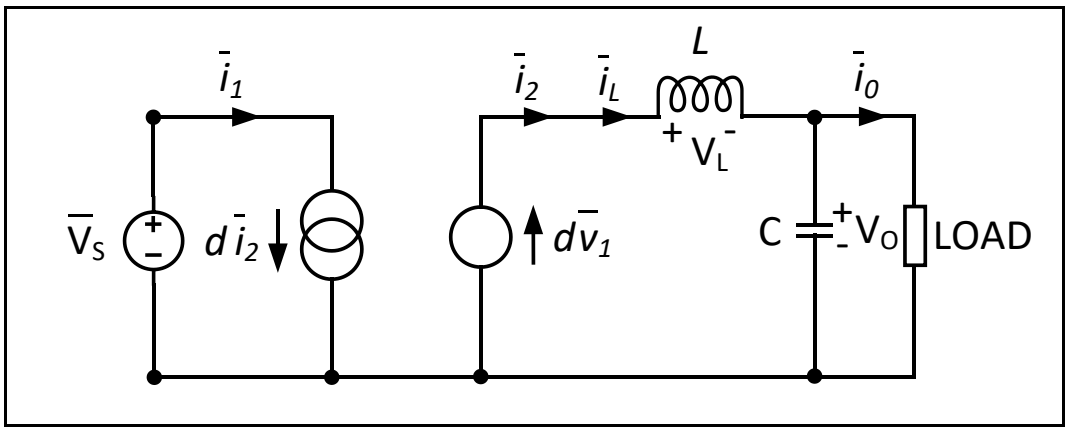

Figure C.4. Buck Converter average model.

Perturbation is done about an operating point:

$$V_O = (D + d_p)(V_S + v_{sp}) = d_p v_{sp} + d_p V_S + V_S D + D v_{sp} \quad (45)$$

whereby V_S represents the supply or input voltage to a converter, D represents the applied duty cycle, and v_{sp} and d_p represent perturbations to input voltage and duty cycle respectively.

Some assumptions are made to simplify calculations:

1) Perturbed values of duty cycle and input voltage are small. When multiplied together, they can be assumed to be zero, $d_p V_{sp} = 0$
2) Ideal input voltage source $V_{sp} = 0$,
3) DC terms have no correlation to controller behaviour, $V_S D$ is ignored.

Applying the assumptions to equation (45) we get:

$$V_O = d_p V_S + V_S D$$

Which are the AC perturbations which are represented in Figure C.5.

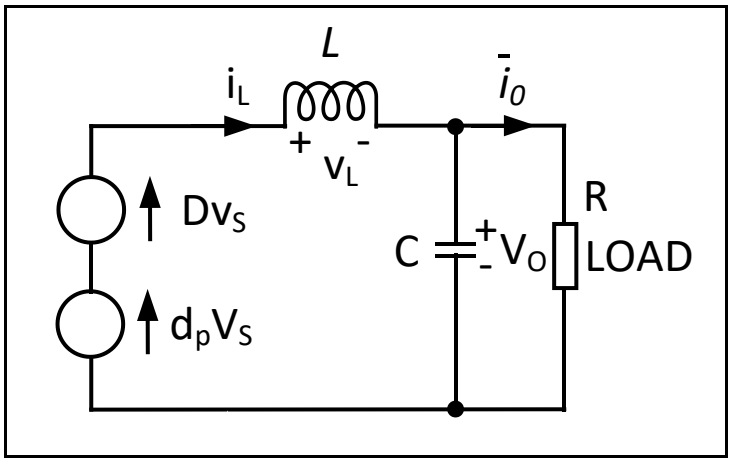

Figure C.5. Buck converter AC perturbation model.

The following output voltage equation for the Buck converter is given by:

$$G_{do(Buck)} = \frac{v_0(s)}{d_p(s)} = \frac{V_s}{s^2LC + s\frac{L}{R} + 1}$$

where v_S in Figure C.5 is assumed to be negligible.

From Figure C.3, the relation of output current to input current is derived as:

$$\overline{i_1} = d\overline{i_2}$$

and the relation of output voltage to input voltage is given as:

$$\overline{v_2} = d\overline{i_1}$$

Derivation of Boost Converter Plant Model

The same perturbation technique is applied on the Boost converter equivalent circuit illustrated in Figure C.6.

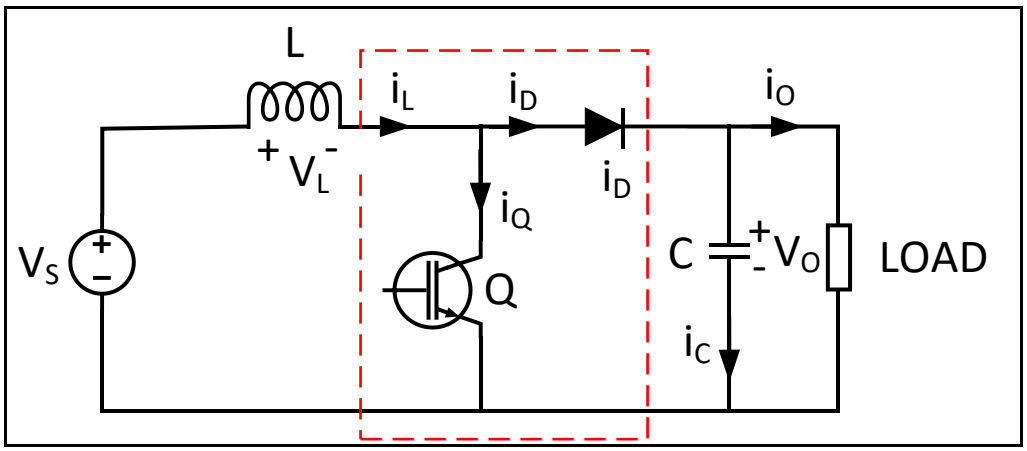

Figure C.6. Boost converter equivalent circuit. Switch circuit marked by the red box.

The voltage and current relations are derived from Figure C.6, and shown in

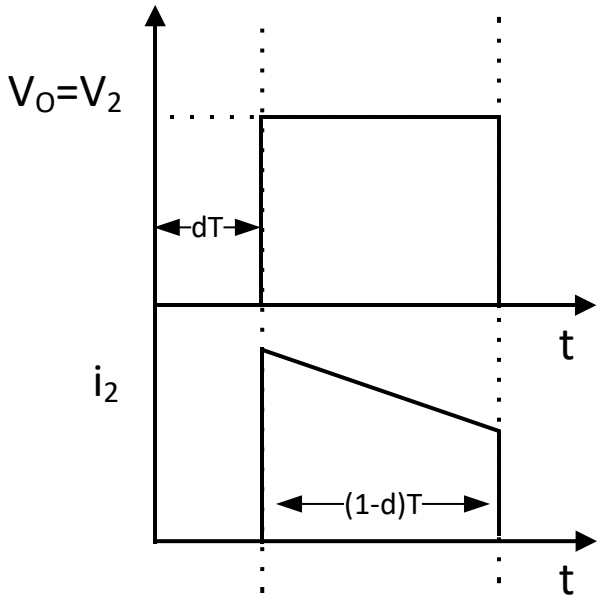

Figure C.7. Boost converter current and voltage waveform during one switching period, T.

From Figure C.7, the relation of output current to input current is derived as:

$$\bar{\imath_0} = \bar{\imath_2} = (1-d)\bar{\imath_1}$$

and the relation of output voltage to input voltage is given as:

$$\bar{V_1} = (1-d)\bar{V_0}$$

Perturbation is done about an operating point:

$$V_S = (1 - D - d_p)(V_O + v_{Op}) = d_p v_{sp} + d_p V_S + V_S D + D v_{sp}$$

giving the following perturbation models shown in Figure C.8.

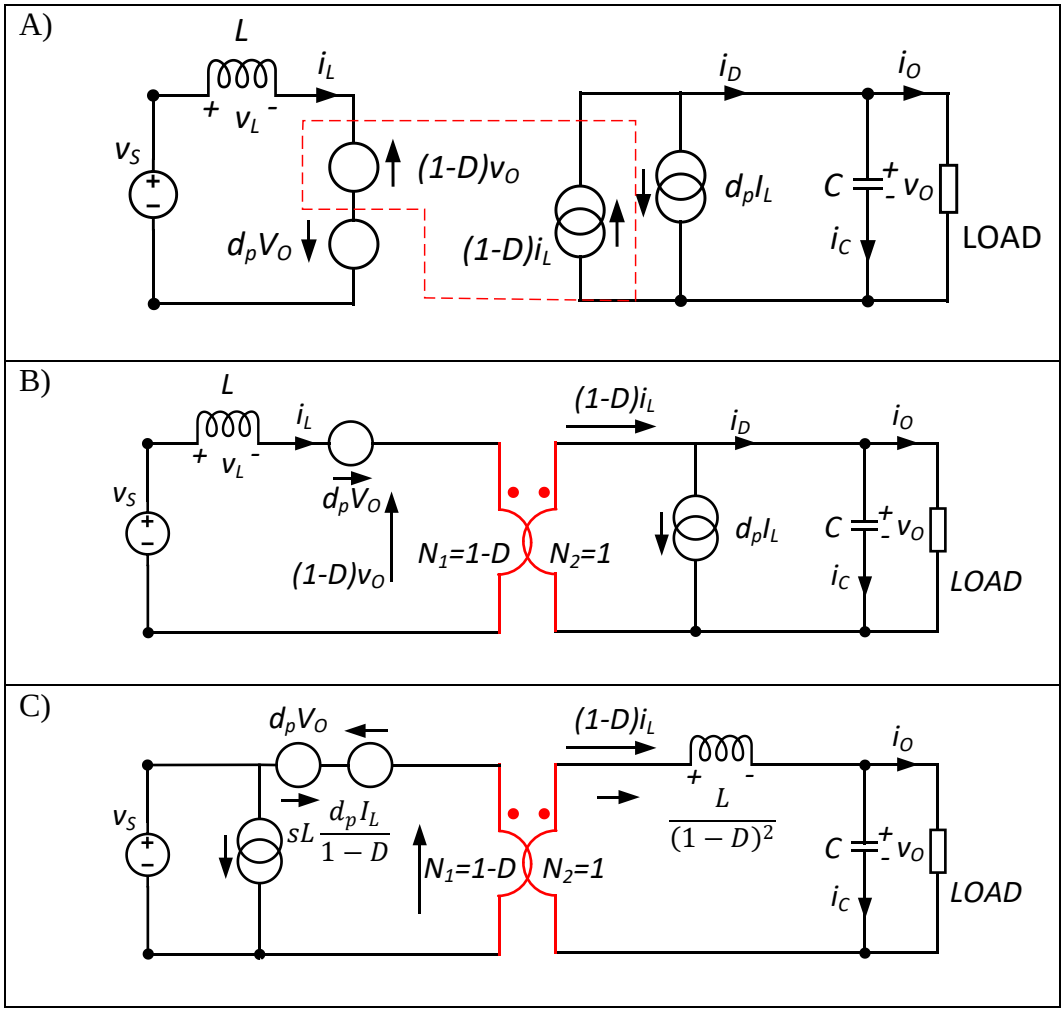

Figure C.8. Boost converter AC equivalent models: Initial perturbation model (A), introduction of the coupling relations (B) and final average model (C).

The equivalent averaged switch circuit with controlled sources is replaced in to the equivalent model from Figure C.6 giving Figure C.8A. Next, coupling relationships N1=1-d and N2=1 are using to link the two halves of the equivalent model giving Figure C.8B. Finally, as shown in Figure C.8C, the equivalent circuit is rearranged, moving d_pI_L to the primary side. The inductor is moved to the secondary side d_pV_O.

The output voltage equation for the Boost converter is derived from Figure C.8:

$$G_{do(Boost)} = \frac{v_0(s)}{d_p(s)} = \frac{\frac{V_O}{(1-D)}\left[1 - \frac{sL}{(1-D)^2R}\right]}{\frac{s^2LC}{(1-D)^2} + \frac{sL}{R(1-D)^2} + 1}$$

Appendix D

Component	Design 1	Design 2
Material	Metglass	Kool Mu
Core Shape	C core	E Core
Core	AMCC40	6527 26µ
Thickness (mm)	35	27
Core width (mm)	41	65.15
Core length (mm)	82	65.02
Volume (L)	0.117	0.114
Turns	7	10
Conductor width (mm)	50	10
Conductor height (mm)	0.4	2.8
Number of parallel conductors	4	1
Single Conductor cross sectional area (mm^2)	20	28
Total cross-sectional area (mm^2)	80	28
Mass (kg)	0.53	0.42

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