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Detection and Analysis of Series Arc Failure in DC Power Distribution Systems

Thesis submitted to the University of Nottingham for the degree of **Doctor of Philosophy, October 2024.**

Danny Robert Seeley

14247813

Supervised by

Mark Sumner
David W.P. Thomas
Steve Greedy

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Date _____ / _____ / _____

Abstract

With the increasing use of renewable power technologies, integration of offshore wind power generation and continuous improvement to battery energy storage systems for electric transport applications in the automotive, shipping and aerospace sectors, there is an increased use of DC power networks at higher voltage and power levels. These higher power DC systems are at greater risk from DC arc failure, caused by the degradation of conductor insulation, component failure or low-quality manufacturing. These arc failures present a significant risk to the reliability and safety of these power networks, burning at thousands of degrees and potentially starting electrical fires that could be catastrophic for electric transport applications. As such, there is a necessity for the development of fast, accurate DC series arc detection algorithms for future transportation and power distribution applications.

In this work the Windowed Fractal Dimension (WFD) arc detection technique is developed and tested against empirical arc data captures generated across multiple arc ignition types, numerous circuit loads and topologies, and a range of different environmental conditions to assess its capability for arc detection when compared to other methods in the literature. This work demonstrates the ability of the WFD technique to successfully dis-

tinguish DC series arc failures from healthy circuit behaviour through a change in the fractal dimension of circuit voltage and current waveforms at arc ignition, presenting a novel DC series arc detection technique focusing on the fundamental fractal behaviour of the arc. Throughout, the WFD technique is shown to improve upon existing arc detection methodologies in the literature, demonstrating an faster 1.5 ms detection time, improved resilience to nuisance trip conditions, and displaying continued efficacy to detecting arc failure in a broader range of load and environmental conditions.

Acknowledgements

It's no big secret that finishing a PhD is a laborious and time consuming process, as is dealing with all my nonsense. As such, those who've taken on the personal burden of helping me complete my doctoral degree deserve all the praise in the world, and a great big trophy to match. Sadly, since I don't have "Marie-Curie" PhD grant money we'll have to forgo the awards ceremony and honour their many sacrifices here instead.

I cannot thank my key supervisor Mark Sumner enough for his support throughout the duration of my PhD. Whilst my motivation ebbed and flowed like the tide, you have never faltered. I'll be the first to admit I'm not necessarily the most "cool-headed" at times, but your continued guidance has allowed me develop from a nuisance with a chip on his shoulder, to a fairly competent young academic. I wish you all the best with the rest of your career at the university - Shame you'll be spending it tidying up my mess of a module!

In a similar vein, thank you to my additional supervisors, David Thomas and Steve Greedy, who were usually on the receiving end of my frustrations with research paper revisions. A special thanks also goes out to Alan Watson at the PEMC for being effectively a fourth supervisor; helping me with issues in the office, with admin, and sanity checking me before I went off the rails on more than one occasion. I would also like to extend my thanks to the PEMC and EEE technical staff for their knowledge and support throughout my PhD. I like to think I wasn't the worst PhD student you had to deal with.

I'd also like to thank my partner, the soon to be Dr. Ellen Newman, for her mutual support during the later years of our PhD's. Your love, support,

and admittedly home-cooked lunches and dinners have been invaluable to me, and I'm grateful to have shared this journey with you. Long may it continue (the love and the meals, not the PhD...).

In a rather prideful manner, I'd also like to pause and thank myself. Pride drove me to start my PhD, and similarly, pride has helped me see it through. It's been a bloody long slog and I like to think that I've come away having done a pretty decent job. Well done Danny - now get a real job and stop patting yourself on the back. You've still got your viva yet!

Figure 0: Image from the Future of the Author at the Defense of his Thesis

It would be out of character of me to finish up without having complained at least a little bit, so lets go out with a bang. Absolutely no thanks are given to either the University HR, Finance or Payroll teams who actively worked to make my life harder throughout the duration of my studies. I have nothing but bile and vitriol for the lot of you. My life will significantly improve knowing I no longer have you; nor your superfluous bureaucracy, in it. If you're in any way frustrated by my comments, please email me and you'll receive an automatic reply letting you know that I'm very busy and that I'll get back to you in the next working week (*Hint hint: I won't*).

Contents

List of Tables

List of Figures

Abbreviations

AI Artificial Intelligence.

DCCM Discontinuous Current Mode.

DWT Discrete Wavelet Transform.

EMI Electromagnetic Interference.

FD Fractal Dimension.

FDTD Finite Difference Time Domain.

FFT Fast Fourier Transform.

FPGA Field Programmable Gate Array.

FPR False Positive Rate.

HMM Hidden Markov Model.

MEA More-Electric Aircraft.

PV Photo-Voltaic.

RH Relative Humidity.

ROC Receiver Operating Characteristic.

STFT Short-Time Fourier Transform.

TPR True Positive Rate.

WFD Windowed Fractal Dimension.

WPD Wavelet Packet Decomposition.

WT Wavelet Transformation.

Published Works

The following publications have been produced by the author as a result of the work in this thesis and are included for completion in Appendix A:

1. D. Seeley, M. Sumner, D. W. P. Thomas and S. Greedy, "DC Series Arc Fault Detection Using Fractal Theory", *IEEE International Conference on Electrical Systems for Aircraft, Railway, Ship Propulsion and Road Vehicles & International Transportation Electrification Conference (ESARS-ITEC)*, Venice, Italy, March 2023

2. D. Seeley, M. Sumner, D. W. P. Thomas and S. Greedy, "The Effects of Relative Humidity on DC Series Arc Generation and Detection", *IEEE Energy Conversion Congress & Expo (ECCE)*, Nashville TN, USA, October 2024

3. D. Seeley, M. Sumner, D. W. P. Thomas and S. Greedy, "Robust Series Arc Detection for DC MEA Power Systems Using Windowed Fractal Dimension", Accepted Subject to Revisions: *IEEE Journal of Emerging and Selected Topics in Power Electronics*, July 31st, 2024

The following co-authored publication was also produced independent of the work in this thesis, and is not included as an appendix:

1. A. Khilnani, L. Wan, D. Seeley, M. Sumner, D. W. P. Thomas, F. Grassi, "Self-Resonance in Ortho-Cyclical Multi-Layer Air-Core Inductors : Analytical Techniques and Optimisation", *IEEE Transactions on Electromagnetic Compatibility*, Oct 2024

Chapter 1

Introduction

Contents

1.1 Preamble

The early nineteen hundreds marked the start of global electrification and the rapid development of consumer and industrial electronics, with big names such as George Westinghouse, Guglielmo Marconi and Nikola Tesla ushering in an age of technological innovation. Their legacy has forever changed the way people live their lives and has enabled industrial expansion on a previously unimaginable scale. The challenges they left behind birthed an entirely new field of research for the next generation, and now, many years later, it is my turn to study electrical engineering. Rather ominously, all of these great men would later go on to die of heart failure.

In recent years the interest and use of DC distribution systems has grown as the global energy mix changes and the demand for increasingly electric infrastructure develops. In adding more renewable sources to power distribution systems there has been an increased use of smaller DC microgrids to interface with the existing grid and support these new resources, such as solar power [1, 2, 3, 4, 5, 6, 7]. These next generation 'Smart-Grids' interface additional distributed energy resources, producing their own energy from conventional and renewable sources. This has in turn lead to the production of energy at lower power-levels and increased the complexity of distribution level power networks, presenting a range of new challenges for power transmission and grid protection. [2, 4, 6, 7].

Similarly, the shift to more-electric transportation including automotive, aircraft and ships has led to increased research into the use of higher voltage DC distribution systems to improve system reliability [1, 2, 7, 8, 9]. This also serves to remove dependence on existing mechanical systems and

move to simpler DC electrical systems that do not require power factor correction, reducing design costs and complexity. Application of these higher power DC systems within electrified transportation exposes these networks to more hostile operating conditions including increased vibration, larger temperature swings, varied humidity and non-static pressures. With a higher voltage network also comes an inherently increased risk should the circuit fail as more energy can be supplied to the fault site itself. Combined, these factors indicate the need for additional research into fault protection schemes for DC power networks, as the damage extending from an electrical failure within these transport applications could not only be very financially damaging, but would also include the cost of human lives. [3, 10, 11, 12]

Arc failures are a specific type of electrical fault that are of special concern to these new higher power DC networks, being a leading cause of electrical fires. Arc failure commonly occurs as the result of component or insulation damage, wherein a conductor becomes exposed or breaks away from its designed path on the circuit. Should the electric field strength at the exposed conductor be sufficiently large across the air-gap between itself and any neighbouring conductive element, it will collapse the air into a ribbon of burning arc plasma, producing an electric discharge between them. These electric arcs can short out circuit components and burn at several thousands of degrees, leading to potentially irreparable circuit damage that can quickly escalate into a large electrical fire [1, 6, 13, 14, 15, 16, 17]. The increased mechanical disturbance and more hostile environmental conditions seen in electric vehicle applications escalate the chances of both component and insulation failure, and therefore arc failure. With their propensity to start fires, and the potentially fatal consequences should arcing occur, arc

failure detection and protection is becoming an increasingly important avenue of research as electric vehicle power systems mature.

The difficulty in detecting and preventing arc failures depends on the geometry of the arc fault itself, particularly where the arc has caused a change in current direction, shifting it from the designed path. Arcs in DC systems can be classified into three different categories based on their interaction with the circuit topology [6, 8, 15, 18, 19]. These categories are summarised in Figure. 1.1. The inclusion of diodes within these illustrative circuits is to prevent reverse power flow to the power supply, and should not adversely impact waveforms significantly offset above the diodes forward bia voltage and 0A as have captured for the purely DC tests that follow in this work:

- Parallel Arc Failure: Parallel arc faults occur when a circuit discontinuity results in an arc fault that occurs across the circuit load, in parallel, or between adjacent phases. These faults short out the load and result in a rapid increase in circuit current as the fault impedance is typically much smaller in magnitude than the load impedance. As such, they can be mitigated through the use of standard circuit over-current protection.

- Ground Arc Failure: A special case of parallel arc failure, ground arc faults occur between a live phase and an earthed terminal or a body/chassis earth. Similarly to parallel faults, the low impedance path to earth also results in a sudden increase in circuit current and can be protected using standard over-current protection.

- Series Arc Failure: Series arc failures differ in that the circuit discontinuity and arc occur in series with the load, in-line with the current carrying conductor, and do not direct current away from it's designed

path. These faults introduce additional impedance that sums with the load impedance, resulting in a series current reduction as the overall system impedance increases. As such these faults do not trip existing over-current protection, and will continue to burn and cause permanent damage unless specialist protection measures are in place.

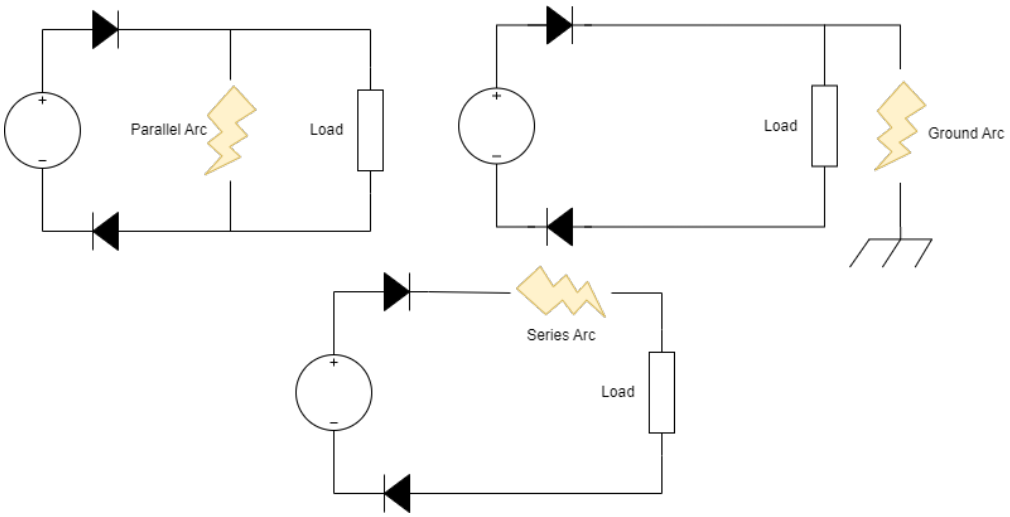


Figure 1.1: Comparison of Different Arc Fault Geometries

Of the fault types described, series arcs carry the greatest risk, potentially burning until total circuit failure occurs. These arc types are present in both AC and DC electrical systems, but present a greater threat in DC networks. Within a typical AC network, the circuit current continually reaches 0 (zero) amperes at the zero-crossing point occurring once every half-cycle. At this time the energy supplied to the arc reaches a momentary zero and the arc may collapse, ceasing burning as it can no longer sustain the arc plasma. There is a however a chance that the arc can reignite shortly after the zero crossing as voltage rises and the electrical potential across the fault site becomes sufficient to re-ionise the air-gap between the exposed or damaged conductors. Each arc collapse and re-ignition in an AC system produces a rapid change of current, and high di/dt as the characteristic arc impedance is introduced and removed from the conductive

path, whilst also suddenly connecting and disconnecting the circuit load. This effect is enhanced in capacitive or inductive loads where the stored energy in the load is quickly released upon arc ignition. The outcome is a distortion in the series current waveform shortly before and after each zero-crossing point that provides a clear indicator of ongoing arc failures, as can be seen for a range of arc types in Figure. 1.2, sourced from [20]. This periodic distortion, or 'shoulder', has been frequently used as an indicator of series arc failure in AC systems, and several detection methods have been published to distinguish these arc in AC networks [3, 19, 20, 21, 22, 23].

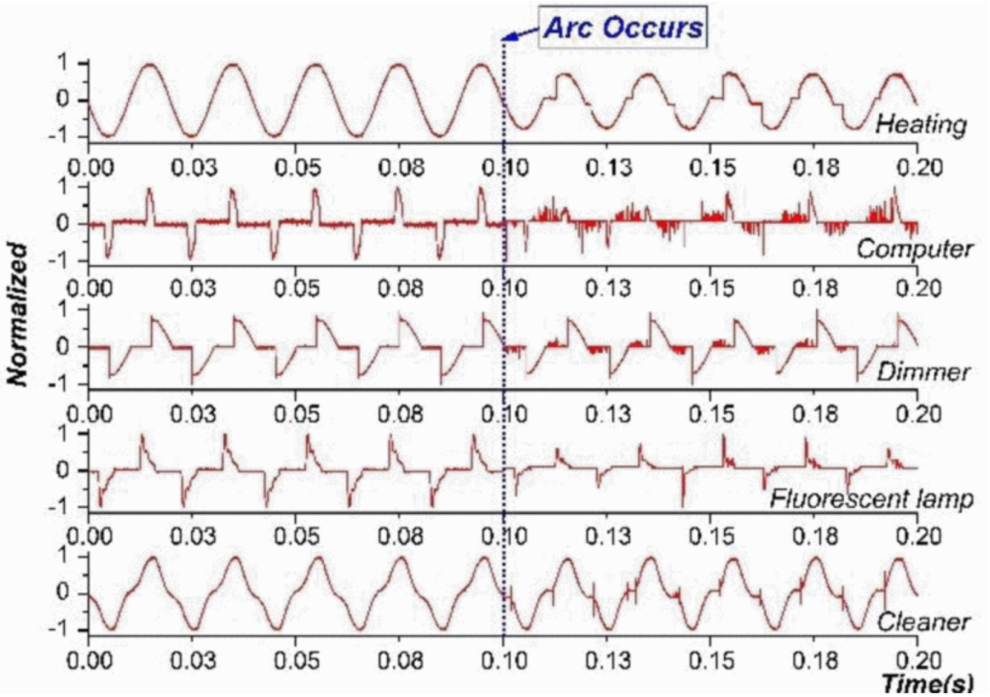


Figure 1.2: Normalised Current Waveforms Showing AC Arc Failures Across a Range of Load Types.

When considering DC series arcs, there are no zero-crossing features as seen in AC arcs, providing a less obvious target for arc detection methods, making them more difficult to detect and potentially dangerous when compared to their AC equivalent [1, 2, 4, 24, 25]. DC networks do not the have periodic current and voltage zero-crossings seen in AC networks, instead

providing a constant source of power to fuel the arc. As a result, the arc is much less likely to self-extinguish and will instead continue burning where an AC arc may not. The combination of a reduced presence in circuit current and voltage waveforms, alongside a constant input power to the arc and resulting in a smaller chance of self-extinguishing indicates that series arcs in DC power systems are a greater risk to power system reliability than those in AC networks.

1.2 Research Objectives

The continued growth of renewable, distributed energy, and the increased electrification of transport options worldwide has led to the introduction of more complex, higher power DC power networks operating in a much broader range of environmental conditions. When considering also the potential loss of human life, alongside the extensive financial and reputational losses that electrical failure may cause, the importance of continued research into DC arc fault protection schemes can be seen.

The aim of this thesis is to develop a novel DC series arc detection methodology and to demonstrate its efficacy across a range of different electrical and environmental operating conditions, whilst also investigating the behaviour of DC arc faults under these conditions to better understand the risks that they pose and to inform decisions on arc fault protection. In doing so, the author aims to develop a novel DC arc fault detection scheme robust to false positives across a range of load conditions as a tool for future arc fault circuit interrupters. This work is motivated by a need to improve on existing DC circuit protection with the increased use of DC

power networks in renewable energy and more-electric transport applications and the life-threatening consequences should they fail. The following research objectives have been developed to help satisfy the research aims:

- Production of an experimental rig to reproduce DC series arcs failures, allowing for variable arc types, a variety of electrical loads and user-defined environmental conditions.
- Development of a novel method of DC arc failure detection and demonstrate its viability across a range of different load conditions.
- Investigate the effects that different electrical and environmental conditions have on DC arc characteristics and the repercussions this has for DC arc detection and circuit protection.

The aforementioned objectives were addressed primarily through experimental work, captured at 2 MHz sampling frequency utilizing a range of different power supplies and circuit topologies. For results in Chapter. 6, environmental conditions were fixed using a Xi'an LIB THR10-150C environment chamber, with built in temperature and humidity control. Simulations have been used sparingly throughout this work, as they are unable to effectively capture arc transient behaviour at very small (µs) timescales as discussed later in Chapter. 3. All simulations and programming for this work was performed by the author in MATLAB/Simulink.

1.3 Thesis Novelty

The following works described in this thesis provide, to the best of the authors knowledge, a novel contribution to the field. All of the following have resulted in peer-reviewed publication:

- Development of a DC arc detection algorithm, capable of distinguishing arcs through calculating and monitoring the fractal dimension of arcing waveforms, assuming the chaotic, self-similar behaviour of the arc is comparable to the fractal behaviour seen in lightning discharge [1, 26].

- The implementation of the aforementioned arc detection algorithm to DC series arcs across an extensive range of different passive, active and power electronic loads, changing environmental conditions and differing arc ignition types [26].

- The investigation of the effects of changing relative humidity and ambient temperature on DC series arc characteristics, providing a suggestion of how this impacts arc generation and detection, with fixed temperature and electrical characteristics and highlighting the necessity for further work in this area [27].

1.4 Chapter Outline

This chapter has introduced the problems faced by growing DC architecture, and demonstrated the need for additional research into DC series arc detection, providing also the motivation and objectives of this work. The remaining thesis chapters are organised as follows:

Chapter 2 reviews the existing literature surrounding DC series arc detection. This review provides a comparison of existing impedance based, travelling wave, time-domain, frequency-domain, and machine learning based methods present in the literature. The merits and shortcomings of each are discussed, the typical points of failure are demonstrated.

Chapter 3 documents the construction of an adaptable experimental testbed, capable of reliably reproducing DC series arc failures whilst allowing for the use of different electrical loads, environmental conditions and arc ignition types. A comparison is also provided, contrasting experimentally produced arc waveforms and simulated arc waveforms, discussing the suitability of each.

Chapter 4 introduces the Windowed Fractal Dimension (WFD) algorithm as a novel method of DC series arc detection and indicates how it improves upon the shortcomings of existing methods presented in Chapter 2. This also includes a summary of the necessary background of fractal dimension and chaos theory, alongside an introduction to the required signal processing and windowing techniques used. Additionally, the required pre-processing, filtering and calculations are described providing context and justification for each.

Chapter 5 demonstrates results of applying the WFD algorithm to experimentally produced DC series arc failures. Results are shown and discussed for different arc ignition types and input voltages across passive, active and oscillating loads in addition to power electronic loads in both a normal and failing Discontinuous Current Mode (DCCM), 'burst mode' operating condition.

Chapter 6 identifies how changing environmental conditions can influence the detectability of a DC series arc through application of the WFD technique and analysis of the behaviour of an arcs in these differing environ-

ments. Arcs waveforms are produced across a range of varying relative humidities and ambient temperatures and analysed to determine the impact these conditions have on the arc characteristics, arc generation and consequences for arc detection. Experimental results are processed using the WFD method established in previous chapters to determine its efficacy in different environmental conditions, and to determine the effect that these environmental conditions have had on arc detection using the WFD method.

Chapter 7 provides context on how the proposed Windowed Fractal Dimension technique can be applied in a practical setting, giving guidance on tuning threshold and window size parameters and mitigating against possible nuisance trip conditions.

Chapter 8 gives a conclusion to the presented work, and presents proposals for future work in this area. The key findings and limitations of the work are presented and compared against the initial research objectives.

Chapter 2

Literature Review and Existing Work

Contents

The increased utilisation of DC power networks at increasingly higher power levels due to electrification of transportation, ever developing industrial applications, domestic-level micro-grid installation, and the increasing availability of renewable generation technologies has led to growing concerns over DC arc failure, and the consequences should arc failure occur. As such, several arc detection methodologies have been developed to mitigate against the risk of arc failure, attempting to observe the arc failure and trigger a circuit interruption before the fault can cause permanent damage.

This chapter presents a survey of existing arc fault detection methodologies, highlighting the merits and shortcomings of each approach. For later comparison, an impedance-based, time-domain fault detection methodology similar to those used in industry and in the literature is programmed by the author to demonstrate specific points of failure when tested against empirically captured arc fault data captures.

2.1 Existing Fault Detection Methodologies

Arc detection methodologies for DC power networks were initially derived from fault detection techniques applied to AC systems, typically utilising circuit line current and voltage measurements to discriminate arcing behaviour. These early detection methods have since been further developed to utilise much broader range of techniques including: impedance-based techniques, reflectrometry and travelling wave methods, frequency-domain techniques, time-frequency based techniques, statistical methods, machine learning approaches and other non-electrical methods such as optical, pres-

sure, thermal or acoustic detection. Modern approaches to fault detection often utilise several different techniques, and may consequently fall into more than one category.

2.1.1 Line Value and Impedance-Based Techniques

Whilst quite broad, time-domain line techniques are any arc fault detection methodology that extract time-series features from the circuit and either analyses these directly to detect an arc failure, or preforms some smaller measure of signal processing to detect the arc. These methods are amongst the oldest and most common in industrial settings, and often select multiple different features to classify arc behaviour and improve the robustness of the technique overall.

One such pure time-domain method is presented by Lu et al. in [28], where measurements of line voltage and current are directly utilised for DC arc fault detection. Here the line current drop at arc ignition, average change in line current throughout the arc and variability of line voltage and current measurements are used as classifiers to discriminate an arc fault. Whilst being verified against experimental arc failure data, the authors offer limited test criteria and do not highlight how the technique responds to changing load conditions, where a step-change in current caused by reducing circuit load could trigger a false detection by mimicking the line current drop expected by the detection algorithm.

Impedance-based fault detection techniques were some of the earliest tech-

niques adopted for arc protection within AC networks and transmission lines, and have been applied to DC power networks with limited success. Typically, these techniques involve a combination of conventional line current and voltage measurements, coupled with a pi-line model (or similar) of the transmission line. The impedance of the modelled line and the impedance calculated from the captured voltage and current measurements are compared, with deviations between the measured and predicted value being used to discriminate a fault [29]. In [30], similar measurements of line voltage and current are utilised to determine fault impedance, and compared to sections of modelled line impedance for circuits with multiple branches. This gives an indication of both fault presence through the deviation from the modelled impedance, and fault location through comparison of fault impedance magnitude to the modelled impedance of known circuit transmission line sections. However, this technique is heavily model dependent and loses accuracy in more complex power networks with additional power converters where simple line-models do not suffice. Impedance-based detection methods are typically implemented as either single ended methods, or double ended methods, with measurements taken at one or two points in the circuit respectively [2, 22, 29, 30]. In single ended methods, measurements are taken at only one point in the fault network, reducing the commissioning requirements but forcing an iterative approach to estimating fault impedance, leading to concerns about the accuracy of single-ended techniques. Comparatively, in double-ended methods such as [31], measurements are taken at both the supply and load ends of the circuit. Fault impedance estimations from each end of the circuit can then be compared to indicate a fault should the estimations show similar values, improving the accuracy over a single-ended approach, but introducing the requirement for additional measurements and computation that may slow the speed of fault detection, alongside the requirement for additional com-

missioning of both load and supply side sensors. Whilst impedance based techniques offer relatively fast fault detection versus other techniques, they are vulnerable to false positive detections in power networks with complex load behaviours where impedance is subject to change regularly and non-linearly.

2.1.2 Reflectrometry and Travelling Wave Techniques

Travelling wave and reflectrometry techniques are a subset of impedance based methods that exploit the time taken for waves on a transmission line to propagate as a means of fault detection. In [32], high-frequency electromagnetic waves produced on the transmission line by the introduction of a high impedance arc fault are captured at multiple terminals along the line. The fault is the detected through comparing the frequency domain and wavelet transformation response at each terminal, also providing an estimation of the fault location along the line through the wave propagation time to the terminals. Similarly, in [33] series arc faults are detected by directing the high-frequency travelling wave through a shunt capacitor with low impedance at these frequencies and measuring the fault current directly with a Rogowski coil current transducer. However the addition of shunt capacitance is not always feasible for all power networks, particularly those containing other high frequency signals or power line communications. In addition to monitoring for specific high-frequency waves introduced by the fault, some methods such as [34] introduce a known binary signal that has been modulated with a high-frequency sinusoidal carrier wave. This technique, known as spread-spectrum time-domain reflectrometry, determines the presence of a DC arc fault through auto-correlation of the known binary signal and its carrier with its reflection at the end of the transmission line.

The introduction of a fault impedance at arc ignition produces a change in the auto-correlation value between the two waves, indicating an ongoing arc fault, but requires unrealistically high (> 96 MHz) sampling frequencies for most practical implementations. Whilst reflectrometry techniques are capable of fast fault detection, and are even capable of fault location, they are often unsuitable for larger power distribution networks where multiple circuit taps and branches can introduce additional travelling wave reflections that interfere with attempts to detect the fault [2, 22, 35]. As such, travelling wave methods are likely more suitable for overhead lines and larger transmission networks with fewer parallel branches, but are yet to see widespread implementation due to the requirement for very high sampling rates that can massively increase installation, maintenance and commissioning costs.

2.1.3 Frequency and Time-Frequency Domain Techniques

Frequency and Time-Frequency arc detection techniques are amongst the most popular, covering a range of methods that attempt to extract features representative of the arc from increased frequency content following arc fault ignition. The simplest of these methods utilise the Fast Fourier Transform (FFT) to separate out the magnitude of specific arc-related frequency bands or the power spectral density of healthy and arcing systems to be compared for arc fault detection [36, 37, 38, 39, 40]. In [39], frequency component magnitude is compared between arcing and healthy conditions for five different frequency bands across 20-120 kHz using simulated arc fault data, with magnitude values across a pre-defined threshold being used to indicate a fault. Despite the detection of the simulated arcs in

each case, the specific frequency bands associated with the arc failure for the setup required identifying in advance, and may change with application to practical DC power networks leading to missed detection. Additionally, the method incorrectly models specific arc transient noise using a "random", Gaussian noise function as per the Uriarte-Gatozzi arc fault model in [41] where it was used as a placeholder. The method therefore does not correctly represent the chaotic and stochastic behaviour of the arc seen with experimentally captured arc data, and is potentially tuned to incorrect frequency bands that could result in missed detections with real world application [15, 41, 42, 43]. Similarly, in [44] the FFT is applied to a small DC Photo-Voltaic (PV) micro-grid to detect user generated arcs throughout. The arc is successfully detected from frequency domain content in the 40-80 kHz band, but results demonstrate a very slow 200 ms detection time, allowing ample time for the arc to ignite surrounding components and insulation in a practical application, and therefore start an electrical fire that may continue to burn even after the arc is quenched. Furthermore, very little information is given about the circuit loads, and leaves doubt about the efficacy of the technique when exposed to active/switching or non-linear load components. Despite the fairly straightforward application of the FFT to arc detection, these methods struggle to resolve the time at which the fault occurs as the information about the time of different arc harmonic components can be lost during the frequency-domain transformation. The loss of this information makes these methods undesirable for some electric transport applications, where post-fault investigations require as much information about the fault as possible to compare to the response of other electrical systems and ensure it isn't repeated, and lives aren't further endangered. Whilst the lack of time-series information still allows for monitoring of continuous faults, FFT based methods remain vulnerable to false positive or nuisance tripping (where in the method "detects" an arc

that is not present in the power network) in the presence of additional frequency components introduced by switching power-electronics, non-linear loads, or electromagnetic interference [2, 45, 46].

Time-frequency methods such as the Short-Time Fourier Transform (STFT) and Wavelet transform overcome the inherent shortcoming of the FFT by resolving overlapping, short-time windows of the signal, allowing for the time of the fault to also be determined. The STFT is utilised for arc detection in [47], decomposing the amplitude of frequency components present within each short-time window of series current and detecting a series arc from the sum of increasing magnitude frequency components below 50 kHZ. The inherent disadvantage with the STFT is the requirement for tuning of the window size used to capture each time-series portion of the signal, where each window must remain at the same size. Smaller windows result in greater time-domain resolution, making them ideal for faster transient (such as the series current drop at arc ignition), but reducing frequency resolution. Equivalently, a larger window produces lower time resolution, but greater frequency resolution, allowing for more accurate selection of arc frequency components, but sacrificing information about the arc ignition time [48]. With the use of overlapping signal windows, there is also a trade-off between computational complexity and detection time, with shorter windows requiring more calculations overall but yielding faster detection, versus larger windows reducing computational burden and potentially improving accuracy through the capture of broader frequency bands, but slowing the detection speed by increasing the amount of time between processing each different window of signal [48, 49].

Similarly to the FFT, Wavelet Transformation (WT) techniques including the Discrete Wavelet Transform (DWT) and Wavelet Packet Decomposi-

tion (WPD) have seen widespread application to arc detection [36, 37, 38, 50, 51, 52, 53, 54]. Wavelet techniques improve further over the shortcomings of the STFT through an adjustable window size, allowing for variable time and frequency resolution, but their performance is strongly dependant on the selection of a "mother" wavelet (a small oscillatory signal multiplied across the shifting time series window) that matches the transient behaviour of the input signal [48, 55]. In [54] series and parallel DC arc failures are detected by observing a change in the eigenvalues of a series of wavelet vector outputs from a 6-tier WPD. Despite the claims of accuracy by the author, experimental verification of the technique on empirical arc fault data is poorly documented and reported detection times are very poor, with packet analysis occurring only once every five minutes. In [53] the DWT technique was applied to high-impedance fault detection in power distribution networks utilising the Daubechies IV mother wavelet. This "mother" wavelet forms part of a set of Daubechies wavelets used widely in the field of signal procesing, as shown in Figure. 2.1 (sourced from [56]). The choice of mother wavelet is made is to match the shape of the selected mother wavelet to the shape of the signal to be isolated - however in the case of arc detection, this would require advanced knowledge of the "shape" of the arc failure, and does not lend itself to dynamic application across multiple differing arc types, environmental conditions and circuit topologies that may change the arc behaviour.

In [53], the energy spectrum of the first four detail coefficients produced as output from application of the DWT to line voltage and current measurements are analysed to determine the increase in energy in each time-frequency sub-band, with an increase in energy in higher-frequency sub-bands being used as an indicator for arc failure. Whilst demonstrating

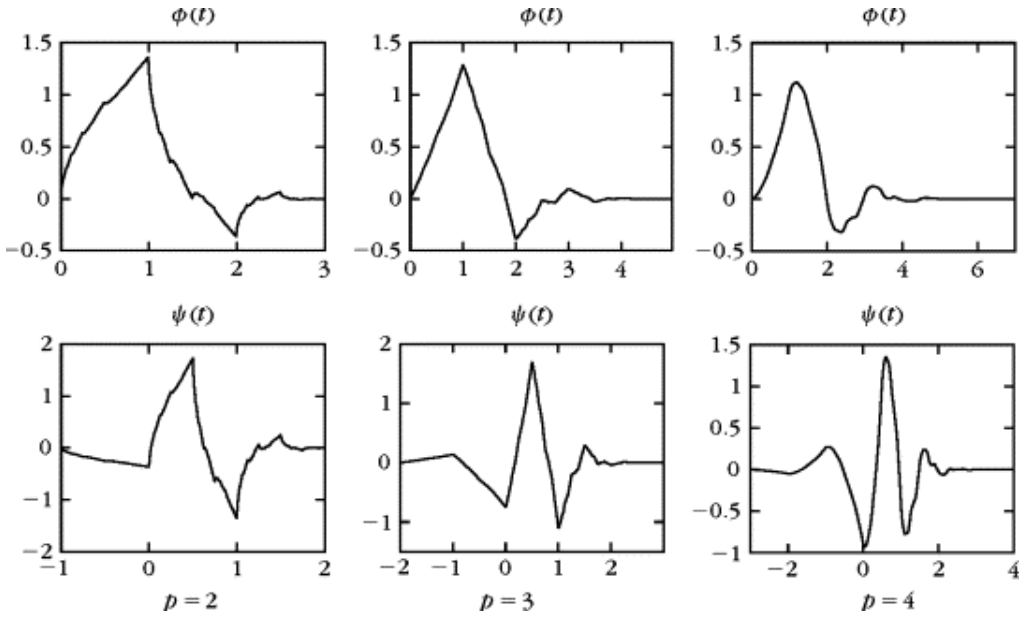


Figure 2.1: Example of Daubechies Wavelet Set from II to IV

a reduced computational burden versus WPD techniques through the reduced number of calculation steps required, this leaves the method vulnerable to high-frequency transient and power-electronic switching behaviours that cannot be properly resolved out of the detail coefficients for a low-level DWT, potentially leading to nuisance tripping and missed detections. Despite the adjustable window size, with each additional level of detail, the maximum resolvable frequency of the wavelet transformation halves, meaning that wavelet methods often require the use of very large sample frequencies and therefore expensive, high-sample rate data-loggers to be utilised effectively [48, 55]. There is also a trade-off between the computational burden of very detailed, multi-level wavelet transformation that can resolve higher frequency noise and are generally more accurate, versus the increased detection speed and lower computational requirements (and therefore implementation costs) for less detailed Wavelet Transformation. The WT also requires an understanding of how faults behave within the network to be protected, to inform the choice of a mother wavelet that matches the transient behaviour of the fault. This limits the generalisation

of wavelet methods to different power network architectures, and increases the required commissioning time in each case.

2.1.4 Statistical and Machine Learning Techniques

With the recent buzz around large-language models, Artificial Intelligence (AI) and machine learning techniques have boomed in popularity in almost every field, but have also seen regular use for arc fault detection, often utilising existing line, impedance, frequency domain or wavelet techniques as inputs [57, 58, 59, 60, 61, 62, 63]. In [57], authors presents a decision-tree model monitoring the V-I characteristics of a solar PV microgrid, reporting a 99.8% detection accuracy. The model required 764,529 records of fault data produced through simulated means on the specific setup to train, with the authors themselves remarking the unsuitability of the method due to the cost, potential safety issues with generating such a large dataset, and the feasibility of implementing such a large model. Similarly [59] uses empirical-mode decomposition to create binary classifiers for a support vector machine from line voltage and current measurements. Whilst producing a reported detection accuracy of 96%, the technique produced false-positive results in the presence of simple step load change event, with a comparatively slow detection time of 100 ms when compared to other, non machine learning based techniques in the literature. In [62], a combination of time domain and time-frequency based techniques are utilised as input to a Hidden Markov Model (HMM), training the model on approximate and detail coefficients from a DWT and a series current input. Whilst the use of a much smaller sampling frequency than other AI and time-frequency methods at 20 kHz (compared to the 200 kHz - 10 MHz recorded elsewhere) does lend itself to practical applications where lower sampling rates can cut

costs, this leads to the requirement for larger, 50 ms windows of input signal to provide enough signal samples to discriminate between arcing and healthy states. This increases the detection time in-excess of the 50 ms window, slowing the method considerably compared to non AI methods, with the authors remarking a high rate of false positives due to circuit transient events. This was addressed by the authors by forcing the algorithm to ignore fault events 100 ms after a normal circuit transient, which whilst reducing the rate of nuisance tripping, potentially leaves the protected system still vulnerable to arc failure, particularly in the presence of switching, non-linear or constant power loads where circuit transient events are common. Authors in [63] take a slightly different approach, utilising a probabilistic-approach using graph theory to generate a Bayesian network that represents the health of an electrical power system. This approach is unique in that it is compiled into an arithmetic model after training, such that it can be applied online elsewhere with significantly reduce computational burden. Whilst the model succeeds in successfully identifying when different sensors throughout the network are faulty, it is only concerned specifically with sensor health, and cannot correctly discriminate between types of fault (such as series arc failure) that have caused the sensors to fail. This is particularly dangerous in the application of series arc protection, as whilst the method allows for broad-scope fault detection, it also introduces the chance of a mis-diagnosis, where arc failure may be allowed to continue burning for extended periods of time, having wrongly been identified as an alternative type of high-impedance fault. Almost all AI and machine learning methods share the same shortcoming, requiring large, accurate training datasets for both normal and fault conditions and are specific to the system they are designed to protect. In many cases this data is impossible to practically acquire, and models trained on other system's data may not generalise well to different power networks. Utilising simulated

data using arc fault models is possible, but depends highly on the accuracy of the fault modelling. Where the data can be generated, it will result in a massive increase in commissioning time to produce simulated or empirical results, and the capture of practical test data may potentially damage the power network. Artificial Intelligence and machine learning techniques also demonstrate a considerable reduction in detection time versus more conventional line voltage and current methods, often due to increased computational burden required to run them. This suggests that AI methods are better tailored to ongoing fault conditions in grounded systems such as solar farms, where slower detection is tolerable and larger computers are easier to manage, though their usefulness for fast-transient fault detection (such as arc fault detection) will continue to grow as small-architecture computers become more powerful and arc simulation models become more accurate.

2.1.5 Non-Electrical Detection Techniques

Amongst the strangest of arc fault detection methodologies are those that employ non-electrical methods, typically utilising some combination of optical, acoustic, or environmental methods [64, 65, 66, 67, 68, 69]. In [69], a unique approach utilises radiated Electromagnetic Interference (EMI) at arc ignition as an indicator of arc onset, which is then confirmed by STFT time-frequency analysis of three separately measured acoustic signals produced by the arc. The unconventional approach taken by the authors succeeds in detecting the fault in their report, but does not explain how the method would respond in acoustically challenging environments, such as in More-Electric Aircraft (MEA) where other sounds and radiated EMI might cause nuisance tripping. A similar method is proposed in [65]

where a more thorough analysis of the acoustic properties of the arc is performed, taking into account factors such as wave propagation and attenuation through different materials. Detection of the arc however relies only on increased magnitude from the acoustic sensor, and is therefore also vulnerable to nuisance tripping in loud environments. Additionally, authors remark that the acoustic signal only becomes audible a short time after arc ignition, imposing an inherent delay on detection time that would allow for additional, unnecessary circuit damage prior to arc detection. In [64] an EMI approach is taken, distributing several hairpin current transducers to detect the radiated field from the introduction of high-impedance faults. Time sampled signals from these transducers are then passed to a Finite Difference Time Domain (FDTD) numerical simulation to resolve both the time of the fault and its position using spread spectrum sensors. Whilst promising for both fault detection and location, authors remark the method requires additional development with a more realistic test setting containing interference sources which may lead to false positives, and shielded environments that could occlude signals, leading to missed detections. Additionally, the method has a significant commissioning cost, requiring a large number of small and sensitive sensors to be spread across the power distribution network, limiting its feasibility in larger power systems. In [68], authors present one of the most unique approaches to arc fault detection in the literature, using a combination of thermal imaging optics, wide-band photo-sensors and pressure measurements to determine the onset of arc failure within capacitor banks in US Navy submarines. Fifteen volt digital logic outputs from each of the sensors are output and controlled within the switchboards and capacitor banks, producing a trip signal and effectively detecting the arc should all three non-electrical sensors produce a simultaneous response. Unfortunately, the response time of the logic circuit (and therefore fast fault detection time) are limited

through the use of non-electrical sensors. As in [65], the pressure and thermal changes required to detect an are only sufficient to produce a trip signal a short-time after the arc has ignited, imposing an inherent limit on the minimum detection time, with authors reporting faults being cleared as late as 250 ms after arc ignition. In this approach the combination of multiple sensor types helps reduce the risk of false positive detection through any single component failure, but risks missed detection should any one sensor fail to register the fault, or be damaged/faulty. Furthermore, whilst optical, thermal and pressure sensors are suitable for sealed environments, they do not generalise well to larger power networks where lights may cause false tripping of optical sensors and thermal and pressure sensors require a much greater change to respond due to the larger environment around them. Many non-electric detection schemes have been shown to have similar shortcomings, requiring the installation of large numbers of additional equipment that massively increases commissioning time and cost in larger power networks, and these techniques are particularly vulnerable to producing false positives due to unsealed operating environments or changing ambient conditions.

2.2 Demonstration of the Shortcomings of a Typical Time-Domain Arc Detection Method

To better highlight the shortcomings of typical arc detection methodologies in the literature, and to provide a point of comparison for later work, the following section demonstrates the application of an impedance based arc

fault detection technique (programmed by the thesis author in MatLab) to experimentally captured DC series arc data, and selected load conditions known for producing false positive detections. Experimental data capture of the traces used in this section is discussed later in Chapters 3, 4 and 5.

The method presented here is a modified form of the current variation method presented in [70] and [71], and is similar to some HV power substation overcurrent protection techniques, whereby DC arc faults are detected from the differential of series current at the point of arc ignition, as in (2.1). This method was modified by Dr. Jing Li and Dr. Chris Rose at the University of Nottingham to include a leaky integration step (shown in (2.2)) following calculation of the current differential. Should the output of the leaky integrator increase above a fixed threshold, the arc is considered as detected. For all following tests, the leakage rate of the leaky integrator (r in (2.2)) was fixed at 50 s^{-1}, as per Li's original work.

$$\Delta I[n] = \frac{\delta I}{\delta t} = max(I[n:N]) - min(I[n:N]) \quad \text{for a Hanning sampling window of N samples} \tag{2.1}$$

$$L_{[}n] = \Delta I[n] + L[n-1] \cdot (1 - \frac{1}{r}) \tag{2.2}$$

In Figure. 2.2 both the output current variation and the leaky integrator output can be seen for application of the method to a forced separation (drawn) DC series arc fault for a fixed-value, passive circuit load(the generation and data capture of which is discussed fully in Chapter 3). It can be seen in Figure. 2.2 that the method does function as intended, producing a

change in leaky integrator output at the point of arc ignition, going from a pre-arc base value of 15, to a peak value of 21 following arc ignition. From this change, a detection threshold value of 19 can be suggested, and the increased output value of 21 at arc ignition would be sufficient to detect the arc.

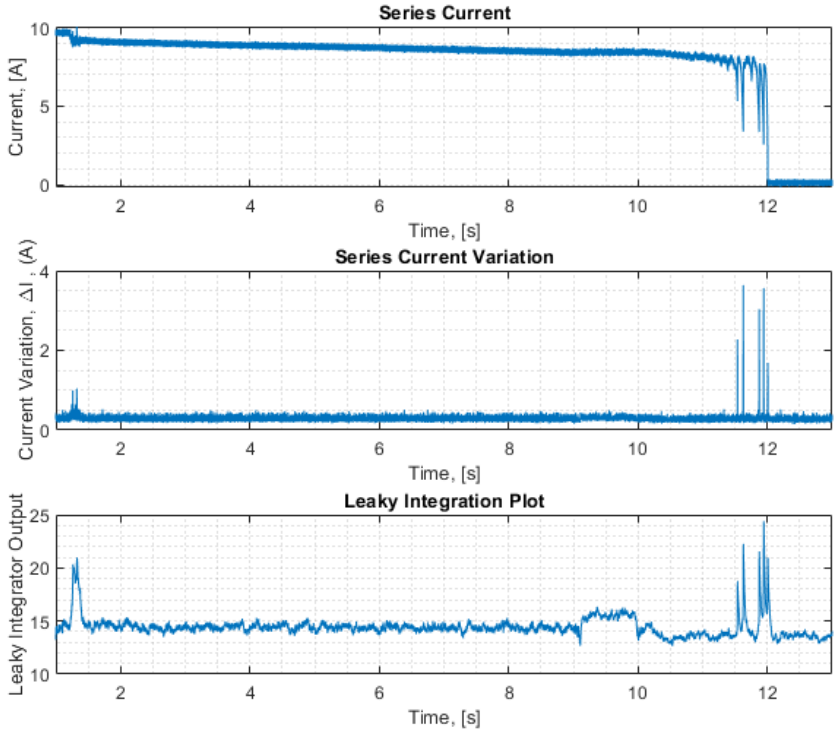


Figure 2.2: Test Application of Current-Variation & Leaky Integration Method to DC Series Arc Failure at 400V, 9.5A, with Forced-Separation Arc Ignition

Whilst the leaky integration modified method in Figure. 2.2 does correctly produce a change at arc ignition sufficient to detect the arc, it becomes clear in Figure. 2.3 that there is a 40 ms time delay between the increase in leaky integrator output and the initial transient change at arc ignition, occurring at t = 1.223 s. This time delay is an inherent part of the time-average leaky integration, as the integrator takes multiple sample windows to increase to a maximum value when a transient occurs before "leaking" back to a resting point. As such, the current-variation, leaky integration approach demonstrates a slow response to arc fault detection, quicker than

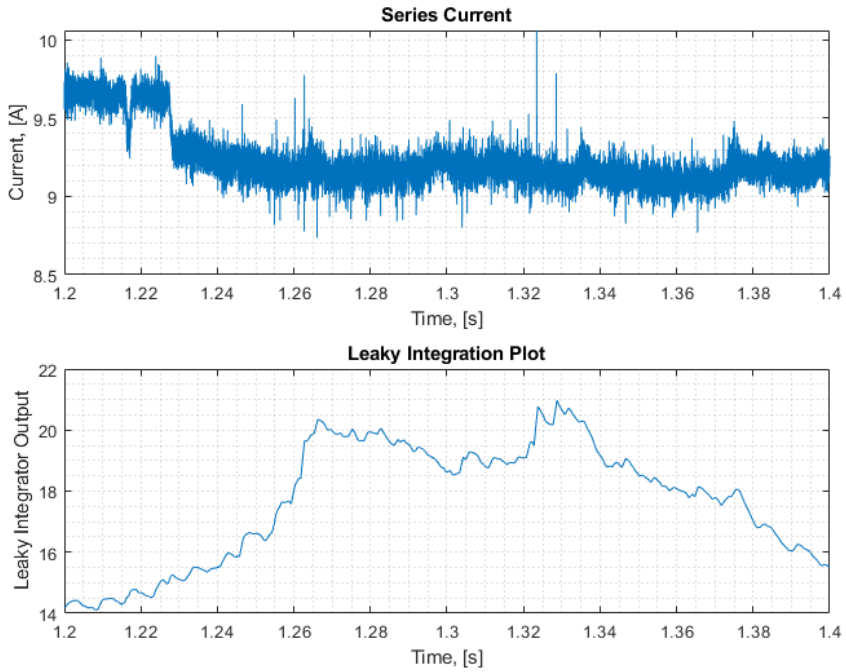


Figure 2.3: Test Application of Current-Variation & Leaky Integration Method to DC Series Arc Failure at 400V, 9.5A, with Forced-Separation Arc Ignition - Cropped to Show Detection Delay

many AI and machine learning methods, but still slower than other time and time-frequency domain techniques, leaving the circuit vulnerable to damage from the arc and from electrical fire ignition in this time. Ideally, the response time of an arc fault detection algorithm should be in the range of <20ms to prevent thermal shock and damage to components, and reduce the risk of components igniting and fires starting before the arc can be quenched, as there is still the additional time delay of the circuit breaking technology to be considered before the fault cna be cleared.

In Figure. 2.4 the current variation, leaky integrator method is applied to a repeated current step change, in the absence of an arc fault, simulating repeated step load change behaviour that has been highlighted to cause false detections in other methods in the literature [2, 4, 22, 35]. It can be seen clearly in Figure. 2.4 that the current variation approach produces an

increase in leaky integrator output at each rising and falling load current edge. Additionally, each increase in leaky integrator output response of 22 is comparable to the response of 21 produced at arc ignition in Figure. 2.2, suggesting that the current variation approach will be vulnerable to false positive detection in the presence of these load change events.

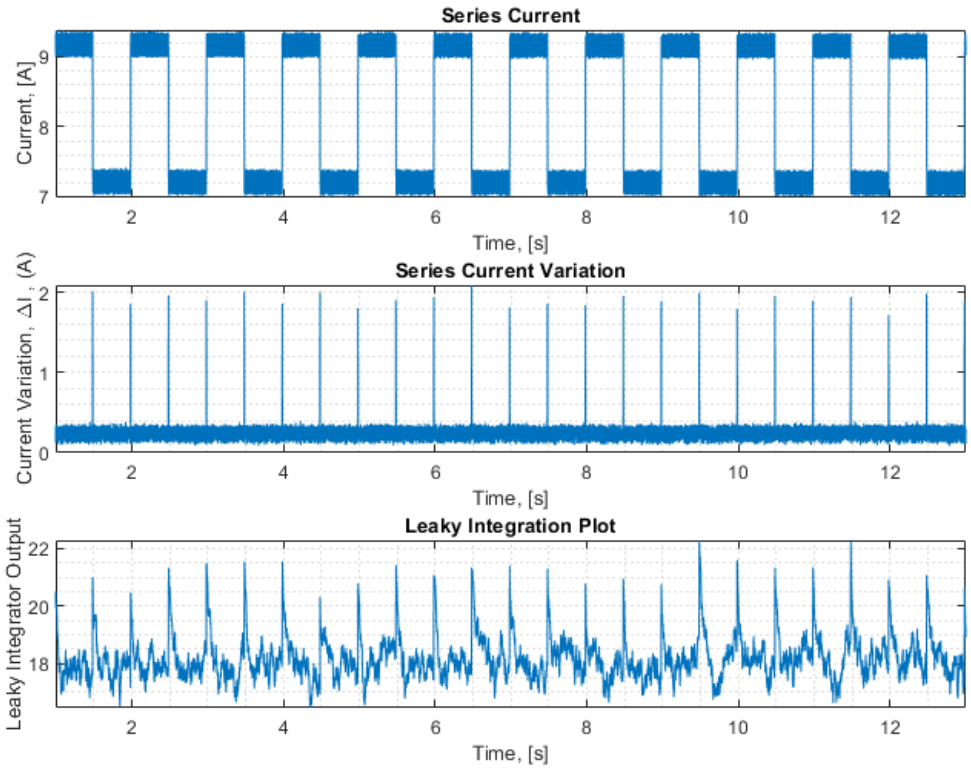


Figure 2.4: Test Application of Current-Variation & Leaky Integration Method to Repeated Step Load Changes at 400V, 9.5A - 7.2A

Further shortcomings of this type of impedance-based technique become apparent when applying the technique to arc failures in circuits containing loads with additional frequency content. In Figures. 2.5 and 2.6 the current-variation leaky integration technique previously demonstrated to work on passive circuit loads is applied to a forced separation DC series arc failure in a circuit with an active, controlled-resistance load oscillating at 1 Hz and and 5 kHz respectively (the generation and behaviour of the arc faults in these traces is covered later in the thesis, in Chapters. 3 and

5). Both leaky integration output traces in Figures. 2.5 and 2.6 show a similar response to the arc, reducing in output magnitude at arc ignition at t = 1.2 s in both cases and contrasting the behaviour seen earlier in Figure.2.2 for the passive load arc where output magnitude increases at arc ignition. This is possibly due to the change in peak-peak current before the arc fault, compared to during the fault when the additional arc impedance helps suppress smaller current transients. Irrespective of this, the change in the response of the detection algorithm to a reduction in magnitude, rather than the previously seen increase means that the arc faults in this active load network would not trigger a threshold based detection, and therefore result in a missed detection of the arc. This type of testing on loads with additional frequency content is often neglected by other methods in the literature, but results in Figs. 2.5 and 2.6 suggest that testing across these types of load conditions is equally as important as passive loads to determine the response of the detection technique to active components, switching behaviours and additional frequency content that may limit the efficacy of the detection technique.

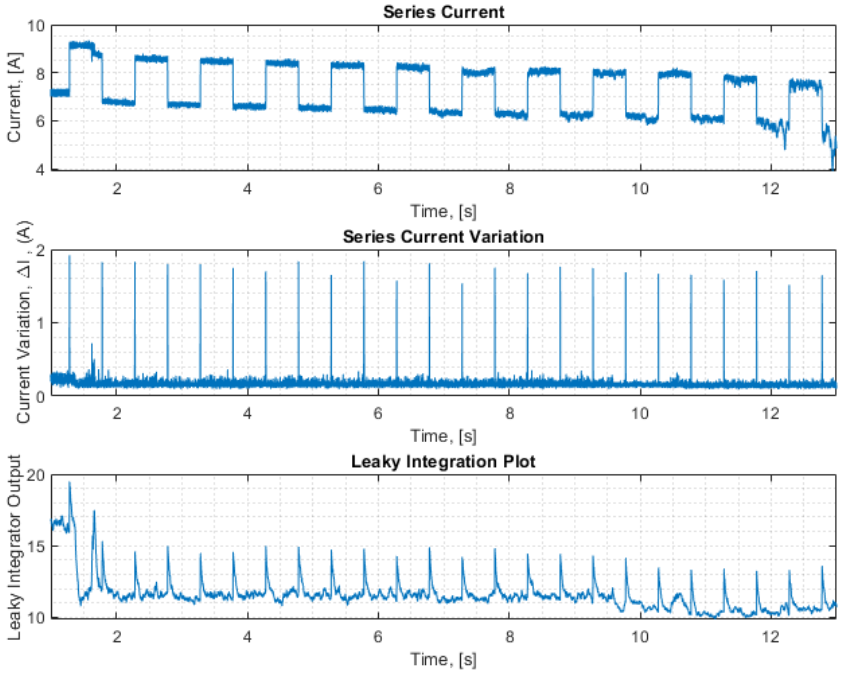


Figure 2.5: Test Application of Current-Variation & Leaky Integration Method to DC Series Arc Failure at 400V, Oscillating between 9.5 A and 7.25 A at 1 Hz, with Forced-Separation Arc Ignition

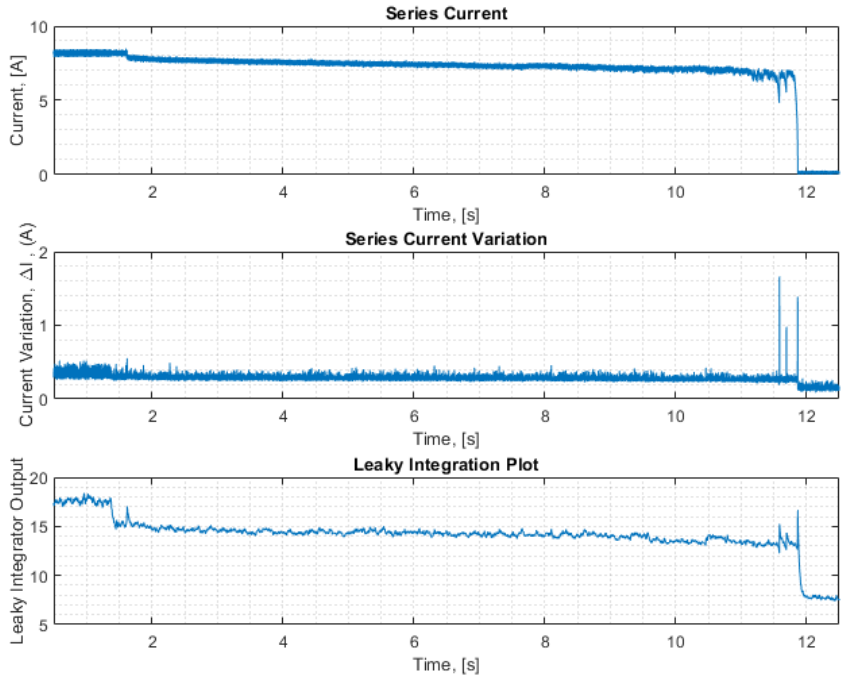


Figure 2.6: Test Application of Current-Variation & Leaky Integration Method to DC Series Arc Failure at 400V, Oscillating between 9.5 A and 7.25 A at 5 kHz, with Forced-Separation Arc Ignition

2.3 Chapter Conclusion

This chapter has presented a review of existing arc fault and high impedance fault detection methods utilising a range of different approaches. Additionally, this chapter has demonstrated the application of an impedance-based, time domain arc fault detection method to experimentally captured arc fault data and highlighted both its merits and shortcomings. From the literature surveyed, it can be seen that there is still a knowledge gap for fast DC series arc detection, resilient to typical false positive inducing conditions (such as step load changes) and fault occluding behaviours (such as significant load oscillation or frequency content) that can be generalised to a range of circuit loads and power network topologies, and that there is the need for more work in this field. Therefore, as stated in Chapter. 1, this thesis aims to develop a fast arc fault detection algorithm that is specific to the micro-scale fractal behaviour introduced by the arc itself, and to demonstrate its robustness across a range of circuit loads, topologies, arc ignition types, and environmental conditions, therefore providing a broad-application solution to DC series arc fault detection for multiple different electric transport applications and DC power network architectures.

Chapter 3

Construction of a DC Series Arc Experimental Rig

Contents

3.1 Producing Repeatable DC Series Arc Failure

Development of any signal processing methodology begins with an understanding of both the required inputs and outputs of the method. As such, before any consideration can be given to producing an arc detection technique, it is first necessary to develop a method of repeatably reproducing DC series arc failure that can be applied interchangeably to different circuit topologies and load types. These "arc generators" are designed to produce a deliberate break in the circuit, in series with the current carrying conductors, leaving an airgap between the conductors that can ionise to form the arc. The method used to produce this airgap is referred to as the mechanism of arc ignition and has significant impact on the behaviour of the arc both at the point of ignition and as the arc continues to burn.

This chapter documents the development of two different arc fault generators designed to repeatably produce controlled arc ignition and collapse at a user defined time, whilst also discussing typical arc behaviours produced for both types of arc ignition. Also discussed are the limitations of simulated arc fault data, and both the necessity for and the considerations taken for accurate, empirical data capture of arc failures for later experimentation.

3.1.1 Forced Separation (Drawn) Arc Generation

Forced separation, or "drawn" arc ignition is the most common arc ignition methodology in research and literature, and is the expected test-case for any UL1699B standard complaint arc fault circuit interrupter for DC systems [72, 73]. As such it is a necessity that any future arc detection algorithm be tested under forced separation ignition, such that it meets the required standards for practical implementation.

The process of forced separation arc ignition is designed to emulate a broken conductor "falling away" from the point it was initially bonded to the circuit and involves the inclusion of two electrodes within the circuit, usually one static and the other mobile and controllable. These electrodes are placed in series with a current carrying conductor and initially remain in contact to allow for "normal" current flow through the circuit. At a user-defined time, the mobile electrode begins to separate from the static electrode, often at a fixed speed, producing an airgap between the electrodes and breaking the flow of current. At this time, the airgap between the electrodes is very small. As the current quickly falls to zero, inductive elements of the circuit (typically line inductance or a simulation of it) produce a proportional reverse voltage across the airgap, reacting to the current change. If the electrical potential difference produced across the airgap is sufficiently large (greater than 352 V for air at 0.55 torr cm; equating to 357 V at standard pressure, at a distance of 7.5 µm [74, 75, 76]) then the airgap will ionise into arc plasma. The arc plasma, once ignited, requires a much smaller voltage to maintain and continues to burn between the two electrodes. These electrodes continue to separate, increasing the size of the air-gap and by extension the length of the arc itself. At a sufficiently large

electrode separation, the arc will collapse and the circuit will be broken, ceasing any further current flow and ending the fault. Several factors can contribute to arc collapse at the extremes of electrode separation, including [15, 74, 75, 76, 77]:

- Field collapse: The point voltage at the electrodes is no longer sufficient to sustain an electric field strong enough to maintain the arc.
- Thermal collapse: The arc cools down due to its increased surface area and the burning arc plasma itself can no longer be sustained.
- Arc deviation: As the arc moves, part of the arc length travels away from the electric field between the electrodes and is no longer supported by it.

Reliably reproducing forced separation arcs therefore requires the construction and programming of a device containing two replaceable electrodes; with at least one mobile electrode with speed and distance control. Ensuring electrodes can be replaced between experiments is particularly important as electrode geometry has a significant effect on the dynamics of arc ignition, and arcs produced with dissimilar initial electrode geometries will have inherently different electrical characteristics [4, 15, 72]. Shown in Figure. 3.1 is a forced separation arc generator built for purpose, containing both a single static electrode and a linear actuator coupled to a DC stepper motor allowing for positional and speed control of the mobile electrode.

The electrodes shown in Figure. 3.1 are connected in-line with the circuit current carrying conductors using appropriately rated, insulated terminal blocks. Additionally, electrodes are insulated from the steel casing of the

Figure 3.1: UL1699B Compliant Forced Separation (Drawn) Arc Generator

generator through ceramic blocks, in similar manner to the ceramic insulators seen in larger power networks. The steel body of the arc generator is deliberately left floating and is not connected to earth or any other conductor to further reduce the risk of stray arcs coupling to the device body. Both electrodes are made from tungsten, allowing for superior heat tolerance versus copper electrodes. This choice was deliberate, as copper electrodes melt very quickly under the heat of the arc fault at higher circuit power (4 kW at 400V and 10A for most experiments documented in this thesis to emulate supplies found in both small MEA applications and heavy-duty more-electric vehicles [78, 79, 80].), and the purpose of the arc generator is to test the forced separation of the arc and not the destruction of the conductors (this is covered in later forced failure arcs). As such, standard tungsten welding electrodes were used in place of copper to ensure that the electrodes could survive the full arc separation process. Both electrodes are 2mm in diameter, with the lower potential electrode remaining flat, and the higher potential electrode ground longitudinally to a point as can be seen in Figs. 3.1 and 3.2. Efforts were made to maintain this electrode geometry between experiments, due to its influence on arc generation [4, 15, 72]. Hence, electrodes are replaced after each experimental arc

failure, being cleaned of oxide and their profile reshaped using a grinding wheel and an angled jig as necessary.

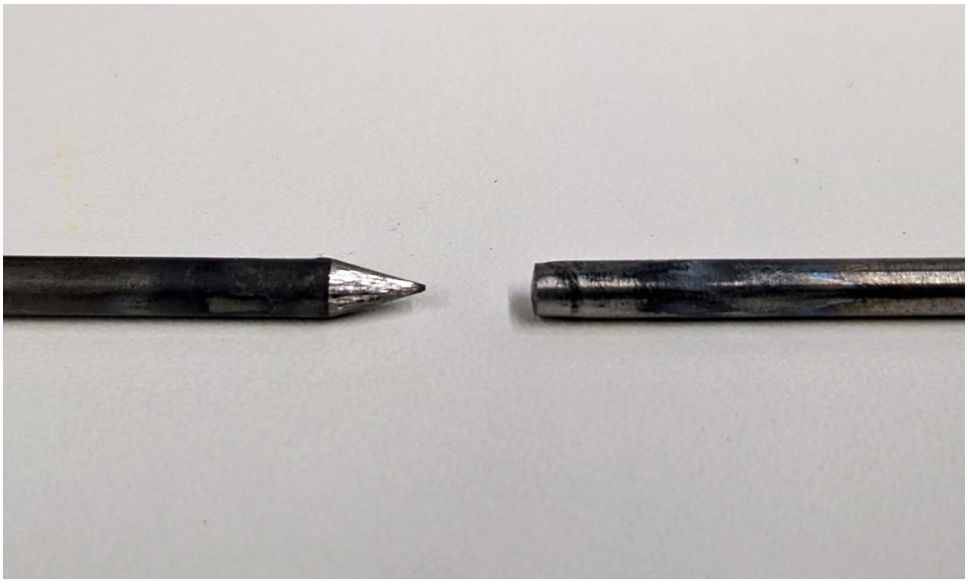


Figure 3.2: Close up of Forced Separation Arc Generator Electrodes

Control of the mobile arc electrode was achieved by coupling of the DC stepper motor and linear actuator to one axis of a TinyG-V8 CNC controller. A series of custom MatLab commands were developed to push serial communications in an interpretable format to the CNC controller through the DSUB20 connector on the arc generator. After considering the reduction ratio of the worm-drive created between the "trolley" containing the mobile electrode and motor axle, precise positional and speed control of the arcing electrode was achieved. When fully calibrated, this allowed for positional control to within ± 0.1 mm and enabled the pre-programming of experimental test conditions in MatLab to run automatically, enabling repeatability between tests.

The standard forced separation test condition used to generate forced separation arcs for work recorded in this thesis starts with the electrodes in

full contact with the circuit energised, as a 15 s data capture begins. A deliberate pause of 1 s keeps the electrodes in contact to capture a short time period of non-arcing behaviour is included in the data capture for comparison to later arcing behaviour. After 1 s has elapsed, the arcing electrodes begin separating at a uniform speed of 2 mm/s until they reach maximum the possible separation at 30 mm. This occurs after the data capture has ended, and after the arc has collapsed, occurring typically at around 20 mm when using this setup under normal lab conditions. After 15 s has elapsed, the data capture ends and the arc capture is completed. Due to the uniform separation speed of the electrodes, it is trivial to determine the position of the electrode at any point in the data capture.

The described arc generator was connected to a 400 V DC supply and a resistive load of 41.7 Ω as shown in the circuit diagram in Figure. 3.3. In these initial tests, the programmable load element R_{Prog} was disconnected, and the 41.7 Ω load was comprised entirely of passive resistive components. Also included in the circuit was a 0.2 Ω, 15.2 mH inductor to represent the combined influence of transmission line impedance of the wiring and other inductive effects in a DC distribution network. Before arc ignition, the load draws 9.55 A of current from the supply, approximating a 4 kW DC bus similar to those found in heavy-duty more-electric vehicles or small MEA applications [78, 79, 80].

Shown in Figure. 3.4 are the results of a typical forced separation arc with the arc generator embedded in the circuit in Figure. 3.3, following the standard test forced failure procedure as described. For clarity, the points of arc ignition and arc collapse have been highlighted. In Figure. 3.4, both the supply current and load voltage show a small step change in magnitude at the point of arc ignition. This reduction in series current is unique to DC

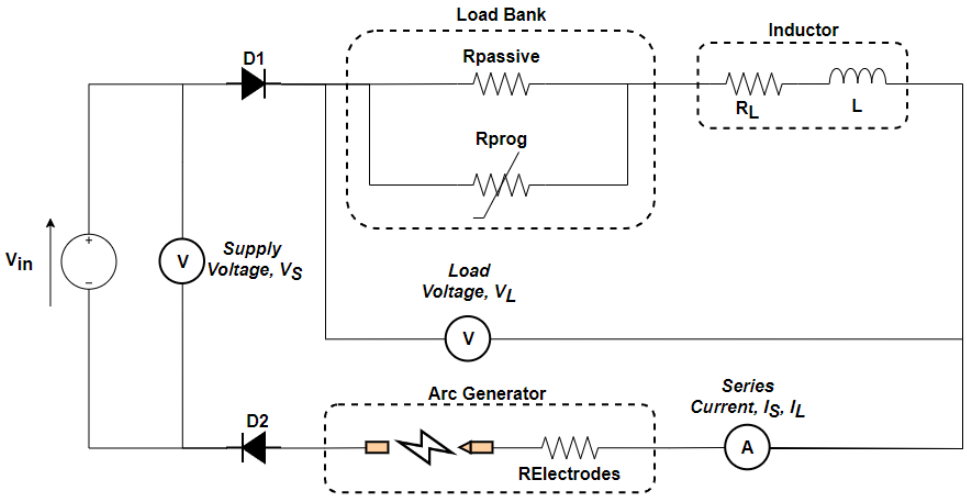


Figure 3.3: Passive and Active Load Arc Generation Circuit Diagram

series faults, and is not observed in parallel or ground arc failures. The reduction in magnitude is the result of the sudden introduction of additional impedance in series with the circuit load, caused by the impedance of the arc itself. The ionised air plasma that forms the arc has a resistance to the current flowing through it, resulting in a non-linear impedance proportional to the amount of arc plasma (and by extension the size of the arc) that works to reduce the current flow in the circuit [5, 15, 75, 81, 82, 83]. Both the series current and load voltage are then seen to reduce in magnitude as the arc continues to burn. This behaviour is typical of these type of forced failure (drawn) arcs, and occurs due to an increase in the arc impedance. As the electrodes as constantly separating, the length of the arc is also increasing, resulting in more arc plasma overall and therefore an increased arc resistance. As the arc length reaches approximately 20 mm at t = 11s in Figure. 3.4, it can be seen that both series current and load current become more unstable, resulting in oscillation of both waveforms and larger transient spikes. The transient spiking is the result of sudden collapse and re-ignition of the arc at it reaches the length limit at which it can be sustained. As the arc collapses and reignites the circuit is quickly broken and reconnected, resulting in the large drops in both load

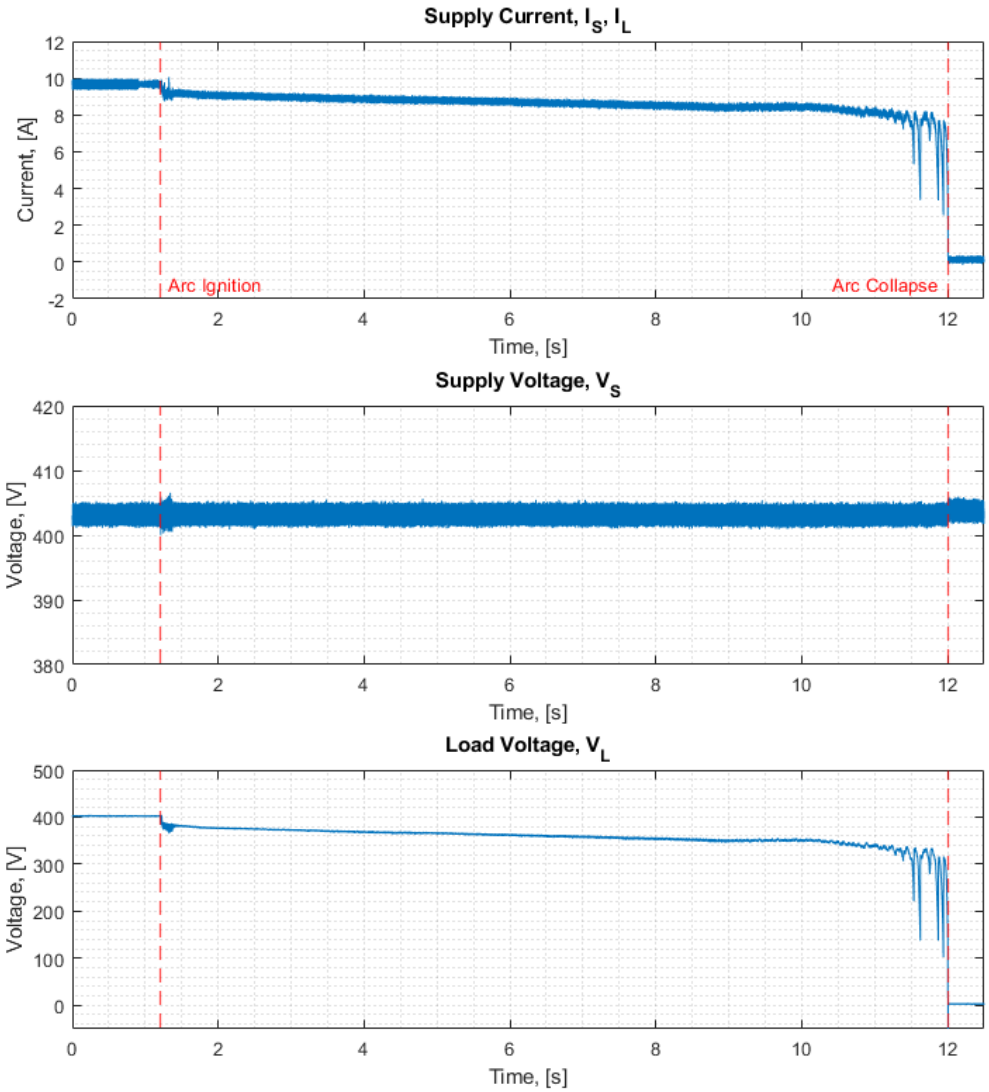


Figure 3.4: Typical DC Series Arc Waveforms - Forced Separation Ignition, Passive 41.7Ω Load, from t = 0s to t = 12.5s

voltage and series current as the circuit momentarily becomes open. The oscillatory behaviour seen alongside the transient spiking just before arc collapse at t = 12 s is in effect, an amplified form of arc noise seen throughout the entire arc. The chaotic behaviour of both ignition and the "steady state arcing" of both smaller arcs and larger lightning bolts (when referring the the movement of the arc plasma itself and the corresponding changes in arc electrical measurements) is well documented in the literature, and will be discussed in Chapter. 4 [2, 4, 15, 37, 82, 84, 85]. Due to chaotic nature of the arc and the semi-random distribution of the air around the

electrodes, the arc will form initially across the path of least resistance in the electric field between the two electrodes. Immediately following the arc forming, the arc begins to grow upwards away from the electrodes, as the heat produced from the arc itself forms convection currents in the air [15, 75, 86]. The arc both rises with the heated air, and moves in a pseudo-random, chaotic, and constantly changing path through the air between the electrodes. The constant changes in arc length are reflected as constant changes in arc impedance. At small arc lengths shortly after arc ignition, these changes in arc length are also small as there is very little space between the electrodes and the arc is constrained by the electric field. As the electrodes separate there is more arc plasma overall with a greater space for the arc to move, resulting in larger changes in both dynamic arc length and arc impedance, reflected as the increased magnitude oscillations seen in the arcing waveform in Figure. 3.4 as the arc nears collapse. As the arc collapses the circuit becomes open with no path remaining for current to flow, and both series current and load voltage reduce to zero.

The interaction between the constant separation speed of the electrodes and the chaotic movement of the arc due to convection heating has the additional effect of increasing arc length; and by extension arc impedance, to be greater than the fixed distance between the arc electrodes. Figure. 3.5 is included to provide a diagrammatic reference illustrating the difference in arc length with electrode separation, and to aide in understanding the relationship between these variables. Due to the constant separation speed of the arc electrodes at 2mm/s, the passage of time represents a greater separation of the arc electrodes. This electrode separation represents the **minimum** possible arc length at this time, as the shortest possible distance for the arc to travel is a straight line between the electrodes. At a very

small value of electrode separation the true length of the arc can be approximated to be equal to minimum arc length as shown in Figure.3.5. Here, the magnitude of the electric field supporting the arc is large (due to the small air-gap) and the physical space for the arc plasma to inhabit is very small, resulting in it occupying almost a direct path between the electrodes.

As the electrode separation increases, the arc will begin to travel away from the direct path between the two electrodes, caused by convective heating and as the arc completes a random walk between more combustible and conductive regions of air, causing the arc path to vary [15, 75, 86]. This has the effect of increasing the true length of the arc, typically vertically above the electrodes in a pseudo-parabola, such that it is no longer equal to the minimum arc length, and now exceeds it. In both cases, the electrode separation still provides an analog to the length of the arc at that time; indicating the minimum possible arc length, becoming less accurate as electrode separation increases. Consider now that the arc hypothetically moves perpendicularly to the electrodes by a percentage of its total length. As the electrode separation increases, the **minimum** arc length also increases, allowing for a greater percentage change in the true arc length. As such, the true arc length is likely to be much more dynamic at greater electrode separation, changing more frequently and therefore producing corresponding changes in arc impedance, such as those seen in Figure. 3.4 as the arc nears collapse at t = 11s.

The arc shown in Figure. 3.4 produced using the forced failure arc generator matches the arcing behaviour produced using UL1669B compliant arc generators in the literature [2, 4, 6, 10, 18, 81, 82]. Using the highlighted points of arc ignition and collapse in Figure. 3.4 as a reference, the

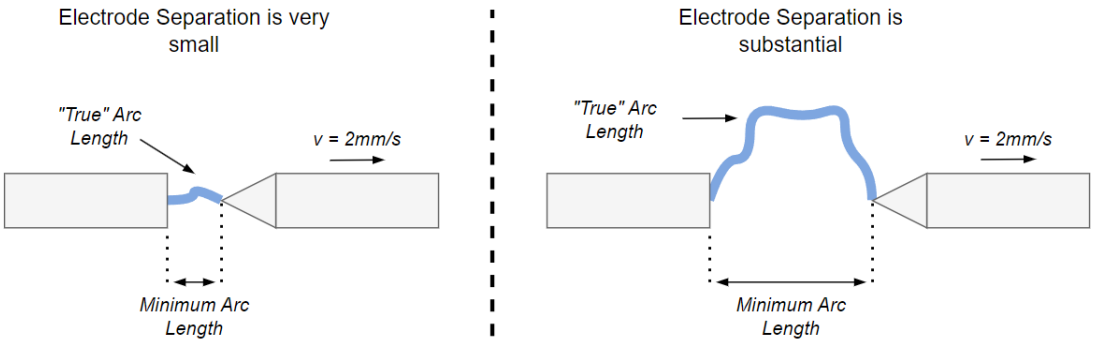


Figure 3.5: Diagram Representing the Relationship between True Arc Length and Minimum Arc Length as Electrode Separation Changes

behaviour of a typical DC series arc can be divided into five key phases; namely:

- Pre-Arc Phase: The time before arc ignition. Here the circuit is operating under normal conditions, in steady state.
- Arc Ignition: The moment the arc ignites to maintain current flow after the circuit is initially opened, causing a step-change in series current as the arc impedance is introduced.
- Steady State Arcing (Arc Burning): The period between arc ignition and arc collapse where the arc is sustaining the current flow to the circuit load.
- Arc Collapse: The point where the arc can no longer support the current flow. The ionised air plasma forming the arc breaks down, resulting in an open circuit.
- Post-Arc Phase: The period following arc collapse, where the circuit is broken by an non-ionised airgap.

Each of the different 'phases' of arcing display different characteristics, wherein a range of signal processing techniques could be applied to poten-

tially be used as indicators of an ongoing arc failure. The arc detection technique developed later in this thesis focuses specifically on the 'arc ignition' phase for arc detection, though still produces a response during the "steady state arcing" phase. Prioritising the "arc ignition" phase allows for the shortest possible detection time before arc onset, and helps minimise possible circuit time by reducing the amount of time for the arc to spread, shorting to other conductors or starting an electrical fire.

3.1.2 Forced Failure Arc Generation

The process of forced failure arc generation is a term coined specifically by the author to represent a contrasting type of arc ignition. Forced failure ignition differs from the UL1699B compliant process of forced separation arc ignition, in that no physical motion of circuit components are necessary. Where forced separation ignition is designed to emulate the outward movement of a recently disconnected component or conductor, forced failure ignition instead seeks to emulate the onset of an arc fault caused by the sudden destruction of an under-rated, damaged, or incorrectly installed component. With manufacturers and consumers increasingly motivated by cost, there is a drive to use "cheaper" components during electrical and electronics production, leading to a comparable reduction in quality. This reduction in component quality leaves a system more vulnerable to component failure, and by extension arc failure caused by sudden ignition of the component or conductor. In producing a mechanism of reliably generating forced failure ignited arc faults, an additional set of test conditions become available for the development of an arc fault detection method, covering a broader range of possible arc failure sources not currently addressed in

other methodologies in the literature.

The forced failure arc generator shown in Figure. 3.6 was custom built to allow repeatable production of DC series arc faults through forced failure arc ignition. The generator consists of two flat ended, 4 mm diameter copper electrodes spaced 20 mm apart. Current flow to the electrodes is controlled by two DC relays that can be switched by the operator at a time of their choosing, as shown in Figure. 3.7. With the first relay closed and the second open, current flow avoids the electrodes and underrated conductor. To trigger an arc, both relays are switched, with the first open and second closed, forcing current through the electrodes, allowing for arc formation at a user defined time.

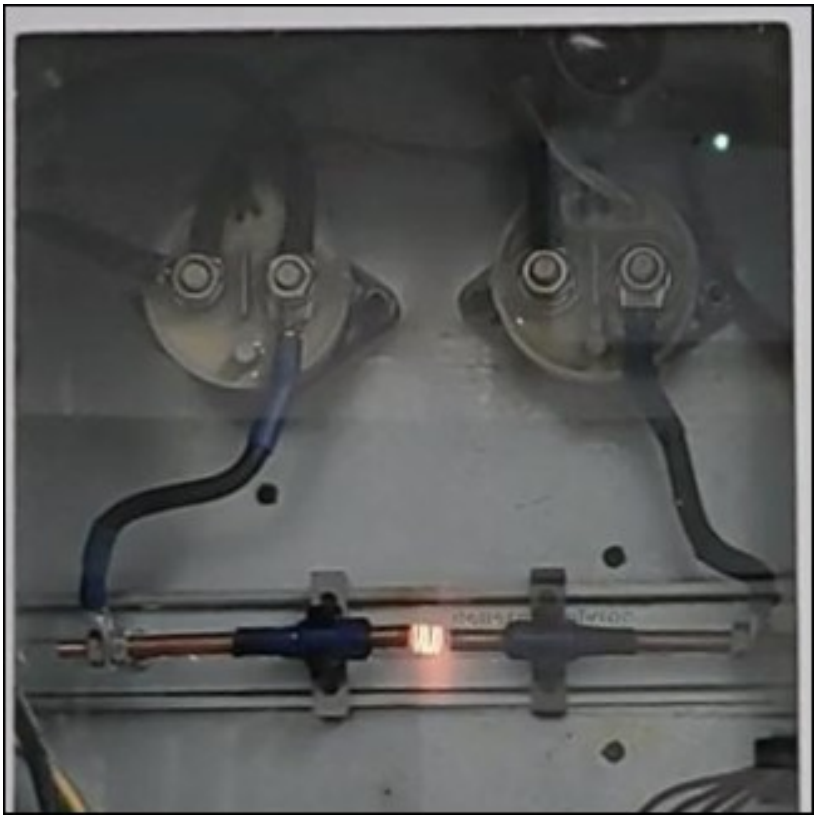
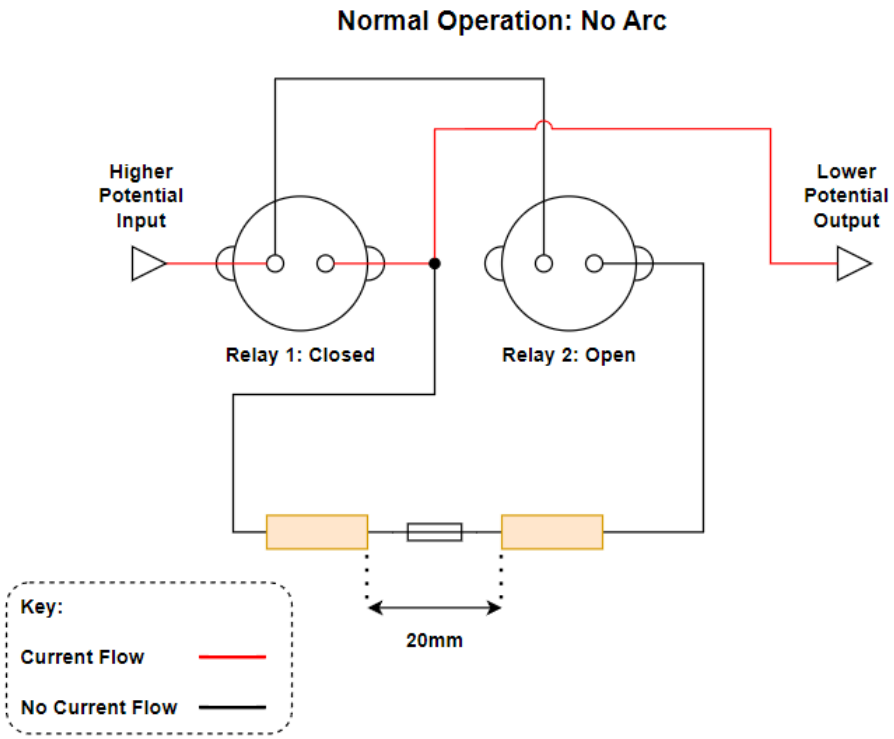
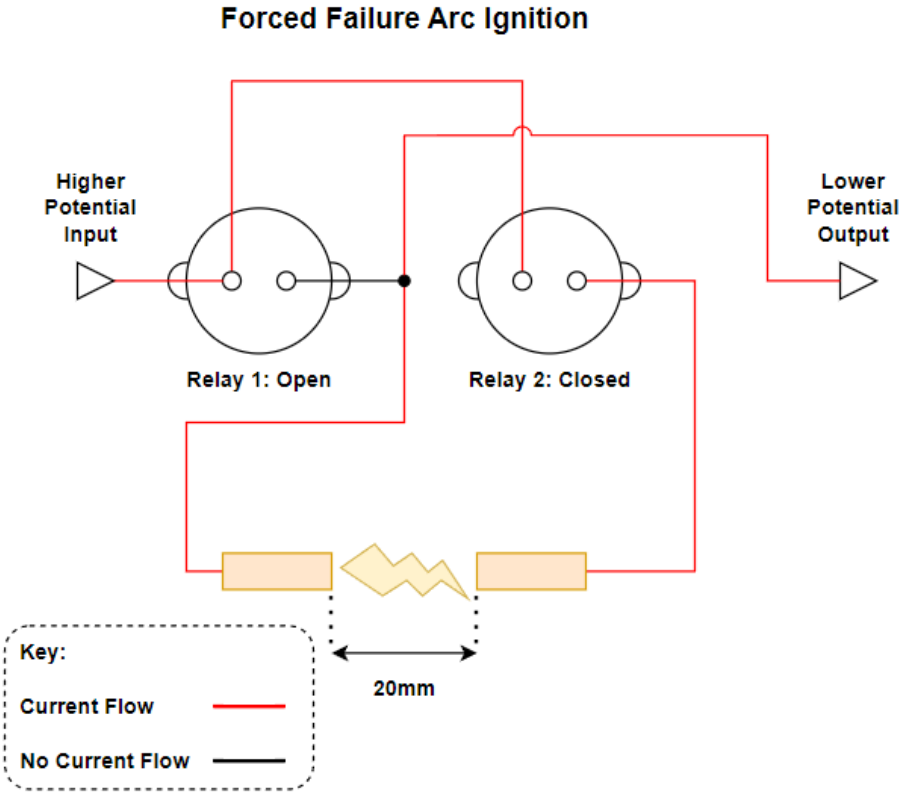


Figure 3.6: Forced Failure Arc Generator, Pre-Arc



(a)



(b)

Figure 3.7: Forced Failure Arc Generator Relay Behaviour Pre-Arc and at Arc Ignition

To produce a forced failure arc using the generator, a deliberately under-rated conductor is placed between the two copper electrodes as shown in Figure. 3.6. This is to simulate either a damaged, poorly manufactured, or poorly assembled component within the circuit. Initially current is controlled to bypass the electrodes through use of the DC relays. At a time convenient to the operator, the relays are switched, causing current to flow through the electrodes and the under-rated conductor. This quickly becomes very hot and melts, breaking the circuit. Similarly to the forced separation arc, if the electrical potential across the gap (boosted by the reverse voltage from circuit line inductance) is sufficiently large, the air-gap between the electrodes will ionise and produce an arc, as can be seen in Figure. 3.8.

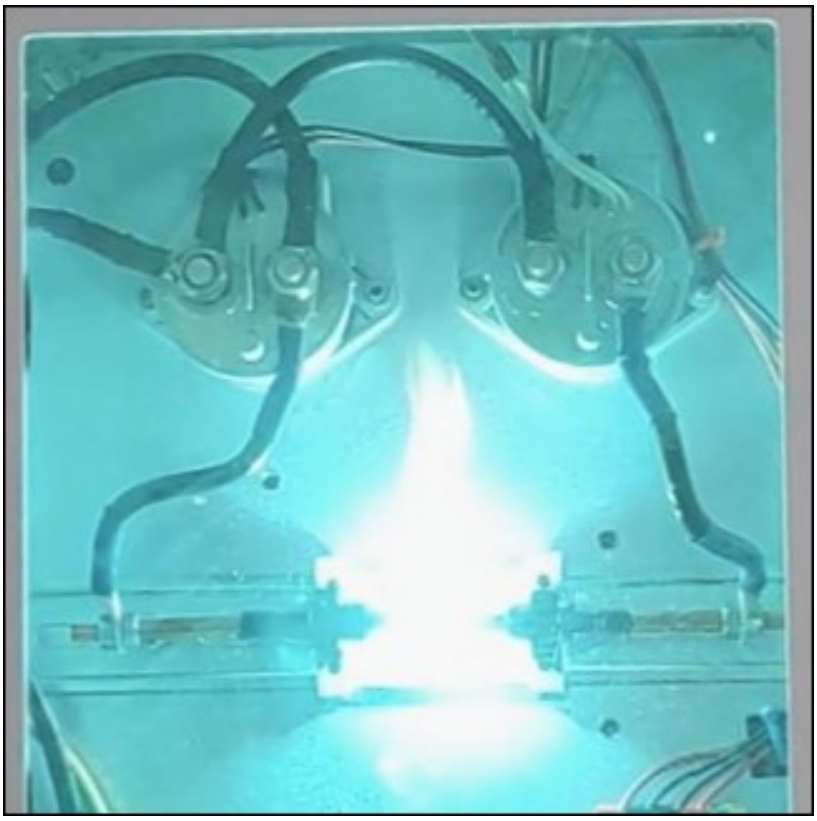


Figure 3.8: Forced Failure Arc Generator, Arc-Ignition

Whilst it would correct to be assume that the larger initial airgap of 20 mm

would require a much larger potential difference to ionise, it bears consideration that as the under-rated conductor first melts and breaks the circuit there is only a very small air-gap between its ends. This quickly grows to fill the full 20 mm space between the electrodes, as the arc rapidly expands and accelerates the melting of the remaining portion of the separating conductor. This results in a rather "violent" arc ignition, producing a large arc flash as the arc first ignites, before settling only after the remainder of the conductor is burnt away. Placing the forced failure into the circuit shown in Figure. 3.3 shows how clearly this violent form of arc ignition affects the circuit electrical behaviour. Highlighted in Figure. 3.9 are the series current, supply voltage and load voltage traces for a DC series arc fault produced using this setup.

It can be seen in the arc trace in Figure. 3.9 that the forced failure ignition produces a large transient in across all variables as the arc rapidly forms and the additional impedance of the ionised air-plasma is introduced to the circuit. After t = 5.5s the initial arc transient is suppressed and the arc waveforms stabilise, showing only slight oscillations but no further change in any of the captured variables. This is likely due to the fixed separation of the arc electrodes at 20 mm leading to an arc of mostly fixed length, and therefore impedance. Slight changes in arc length could explain the oscillations seen in the series current and load voltage waveforms, as these changes in length would correspond to slight changes in arc impedance when the burning arc moves due to convection heating of the air.

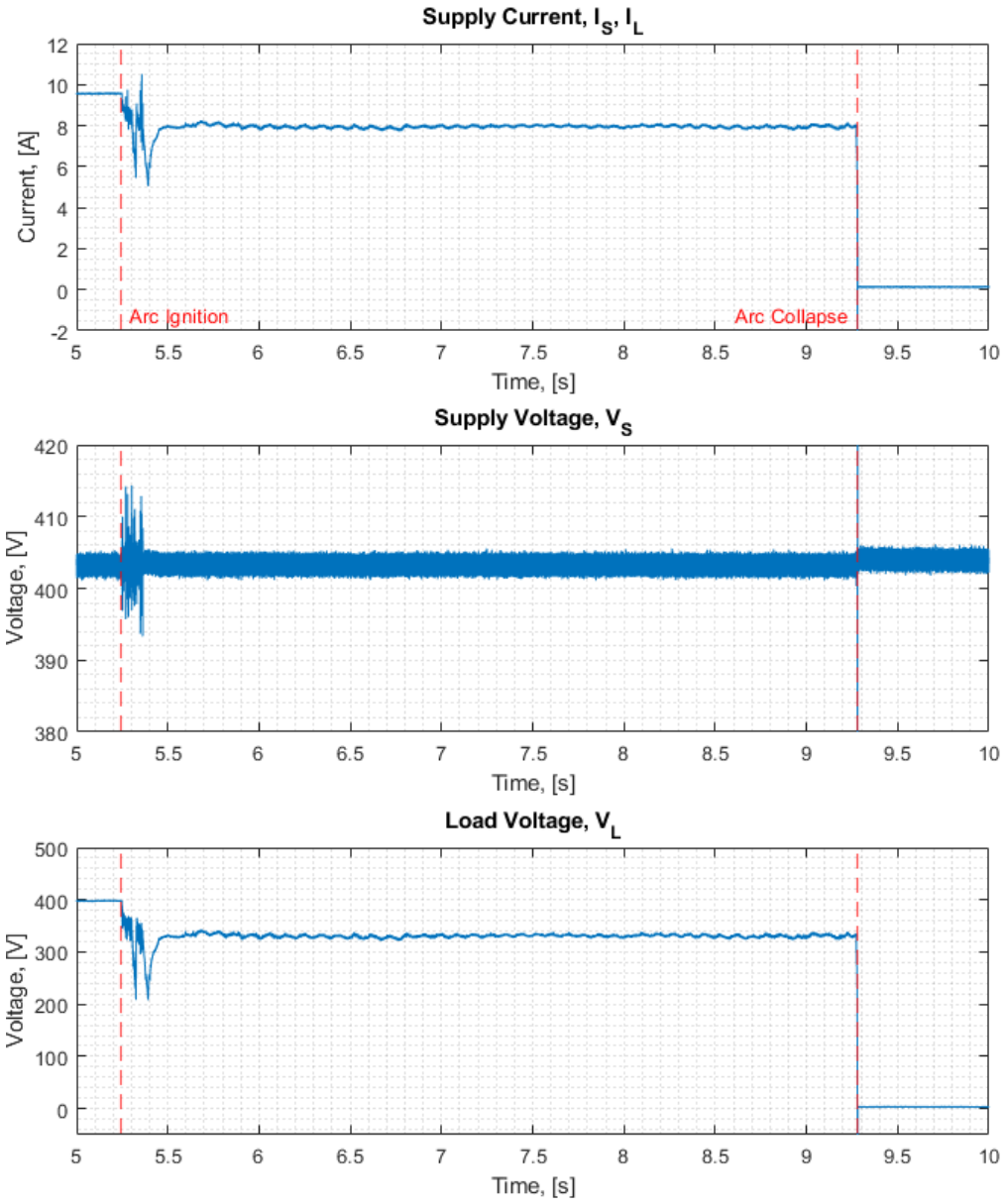


Figure 3.9: Typical DC Series Arc Waveforms - Forced Failure Ignition, Passive 41.7Ω Load, from t = 5s to t = 10s

3.1.3 Comparison of Typical Arcs Failures

When comparing both forced failure and forced separation arcs in Figs. 3.4 and 3.9 respectively, several key differences can be observed between the two, each with potential influence on the detectability of the arc.

The most obvious difference is the change in load voltage and series current at arc ignition between the two traces. In Figure. 3.4 the change upon arc ignition at t = 1.2s is very small when compared to the forced failure arc ignition seen at t = 5.3 in Figure. 3.9. This difference in initial transient behaviour can be explained by considering the length of each arc at ignition, and by extension the introduced impedance of the arc. The forced failure arc in Figure. 3.9 ignites and suddly grows to fill the 20 mm air-gap between the arc electrodes, compared to the µm scale air-gap created as the electrode just begin to separate for the forced separation arc in Figure. 3.4. The shorter air-gap requires a smaller voltage to ionise, and produces an arc with lower arc impedance (due to the short arc length at ignition), resulting in only a small change to the circuit waveforms as the arc forms. Conversely, the larger initial air-gap at arc ignition in Figure.3.9 requires a greater initial voltage to ionise, and produces an arc of greater initial length and arc impedance, resulting in a larger disturbance to all waveforms both at arc ignition and until arc collapse. The larger initial transient seen in the forced failure arcs is a possible boon to arc detection, providing a larger change from "normal" pre-arc behaviour at the point of arc ignition to be used as a reference of arcing behaviour.

As the electrodes in the forced separation arc in Figs. 3.4 are constantly separating, the arc length is continually increasing as the electrodes (and by extension the end points of the arc) move further apart, resulting in a

proportionally increasing arc impedance and a corresponding reduction in load voltage and series current. This is illustrated in Figure. 3.10 where the impedance of both the forced separation arc in Figure. 3.4 and the forced failure arc in Figure. 3.9 are plotted for comparison. Here, the arc impedance was determined through by division of the arc voltage (determined through Kirchoff's laws from the supply and load voltage measurements) by the circuit series current. In contrast to the steady reduction in both load voltage and series current observed only in forced separation arc failures, the forced failure arcs remain at a fixed size and see no macro-scale change in load voltage or series current after the initial arc transient has passed (after t = 5.5 s). This again can be attributed to the arc impedance and arc length, with the arc impedance shown to remain fairly constant after t = 5.5 s in Figure. 3.10. It is likely that the larger arc impedance seen throughout the arc in the forced failure ignition arc will prove easier to detect than the forced separation arc. The greater arc impedance throughout the fault would allow the arc behaviour to have a greater influence over the circuit voltage and current waveforms, and suggests that it will be easier to detect, with the arc behaviour being more easily distinguished from normal behaviour at these greater magnitudes.

The impedance of the forced separation arc and forced failure arc converge to a value of approximately 9 Ω after t = 11 s in the forced separation arc trace (or roughly 10 s after arc ignition at t = 1.1s). Because of the constant 2 mm/s separation speed of the electrodes, this amounts to an electrode separation distance of 20 mm, equal to that of the static forced failure arc electrodes. The similarities between arc impedance at equal electrode separation across both ignition types helps demonstrate that despite the different arc ignition types, both arcs behave similarly

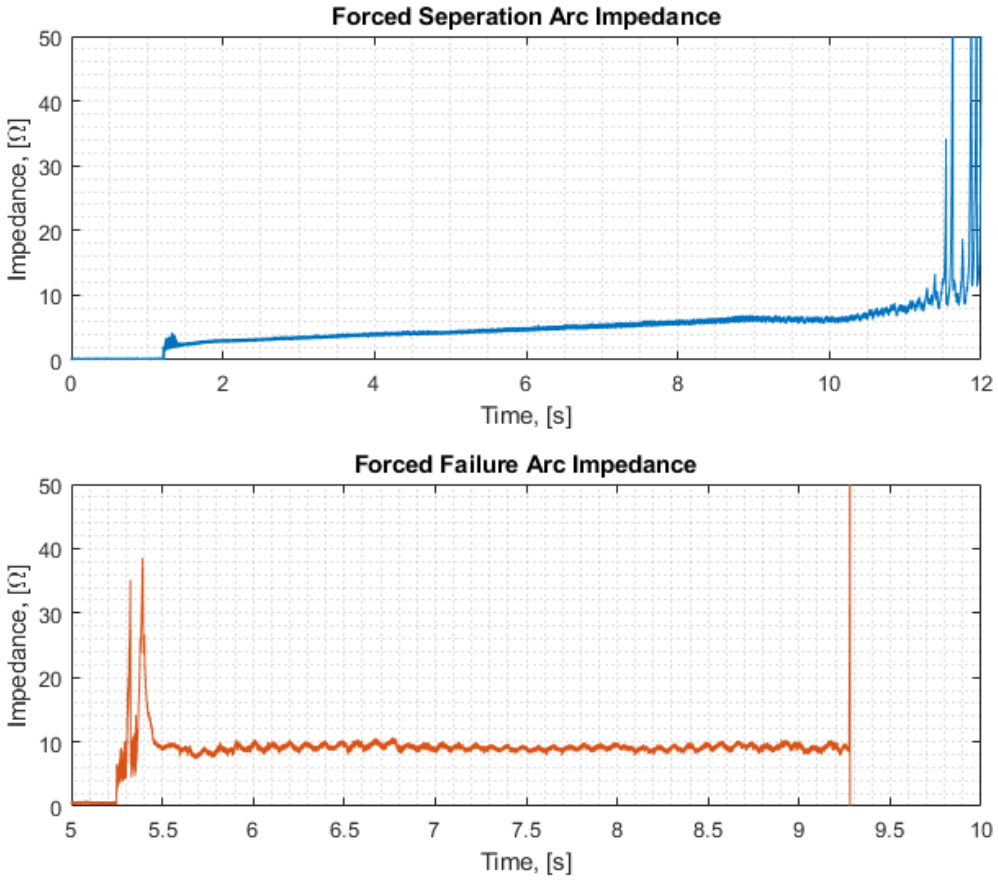


Figure 3.10: Comparison of Arc Impedance between Forced Failure and Forced Separation Arc Ignition Types and Passive Circuit Loads

post ignition when under similar conditions (fixed electrode separation and ambient temperature, pressure and humidity). As such, all future traces will record arc impedance at arc collapse, where the trends described here suggest that they can be best compared between ignition types. Hence, changes seen in arc behaviour in these later traces can be attributed to differences in electrical behaviour, rather than the specific influence of the different arc generators or arc ignition types, as they are measured at the similar point of arc collapse at approximately 20 mm electrode separation. The differences described in arc behaviour seen in Figs. 3.4 and 3.9 are consistent between all later data captures, and with other arc traces in the literature, providing a platform for production of further arc failures for the development and testing of an arc detection algorithm [2, 4, 6, 10, 18,

81, 82].

3.1.4 Data Capture Considerations

In order to allow for accurate capture of arc behaviour several steps were taken to allow for high-sampling rate data capture. This has the added bonus of extending the range of potential signal processing techniques for arc detection by capturing as much information about the arc as possible. Sampling at inherently higher sampling rates allows for the capture of additional frequency content so long as the Nyquist criterion is satisfied: that the sampling rate should be at least double the frequency of the highest frequency in the sampled signal, though in practice 5 to 10 times the highest frequency is used [48]. This criterion also applies to time-domain behaviours, meaning that to accurately capture sub-millisecond (1×10^{-5}) scale changes in arc noise, a sampling period of approximately 1 µs, or 1 MHz sampling frequency is required. This allows for the capture of both macro-scale arc behaviours, and micro-scale arc noise that typically goes overlooked in arc fault data captures in the literature. Additionally, the higher sampling rate ensures the accurate capture of other sources of noise and interference within the circuit that may contribute to false positive detections, wherein a detection method indicates a fault even though none is present. Capture of these alternative sources of noise is almost as important as capture of the arc waveform itself, as without accurate sampling of interfering waveforms and noise they cannot be mitigated against in an arc detection methodology.

For all empirical experimental results recorded in this work, data was captured using a PicoScope 5000 series oscilloscope, sampling at a frequency

of 2 MHz from a variety of different sensing equipment, utilising a 15-bit ADC. To ensure consistency between experimental tests, a custom set of API instructions were produced in MatLab to allow the control of the PicoScope and the data capture in MatLab. This overcomes the dependency of the PicoScope on external software, and allowed for greater control over the PicoScope settings, enabling the higher 2MHz sampling rate and ADC resolution despite using all four input channels of the scope. Additionally, this allowed programming of the PicoScope to be synchronised to the arc generator control commands (also in MatLab), ensuring all arc failure data captures begin at the same time relative to arc ignition. Through integration of all experimental control elements into MatLab, absolute consistency between the sampling and control of individual arc fault experiments was possible, helping to mitigate again the influence of human error in experimental timing. This in turn allows for more accurate comparison of individual arc fault data captures, easing the burden of data analysis when comparing arc faults across multiple different load conditions, ignition types and environmental conditions.

3.2 Simulated Arc Failure

To reduce the burden of acquiring a large range of arc fault data captures, it would be beneficial to produce a simulation representing a DC series arc fault which could then be implemented into a range of possible load conditions. Simulating the arc would require resolving the behaviour of an existing DC circuit with a condition dependant mathematical model of how an arc failure develops. The result of which would then be a set of discrete difference equations to show how the circuit behaviour changes

from one time step to another that could then be implanted within any later simulation. The Uriarte-Gattozi model was decided on as the best possible arc model for this simulation work, due to its specificity to DC series arc faults and use in other arc detection techniques in the literature [2, 4, 41, 85]. The Uriarte-Gattozi arc model was developed by Fabian Uriarte and Angelo Gattozzi et al at the University of Texas at Austin in 2012 to mathematically represent the behaviour of forced separation (drawn) DC series arcs in low voltage microgrids, and suggests that a DC series arc within a circuit can be represented by a point-voltage source in series with a non-linear resistance. Placing the Uriarte-Gattozi arc model components into a simple DC circuit consisting of a voltage source, load resistance and line impedance as shown in Figure. 3.11 allows for the discrete difference equations to be developed, whilst also emulating the passive circuit used for earlier arc experimentation shown earlier in Figure. 3.3.

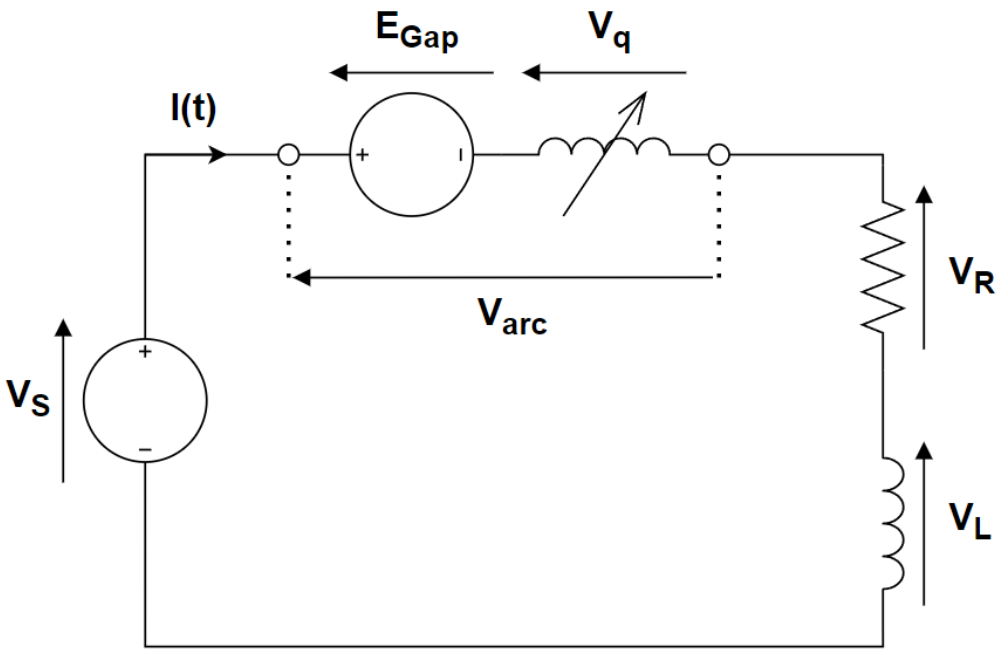


Figure 3.11: Simple DC RL Load Circuit with Uriarte-Gatozzi DC Arc Model

Application of Kirchoff's Voltage law to the arc containing circuit in Figure. 3.11 allows for the expression of the circuit source voltage as a function of time:

$$V_s(t) = V_R(t) + V_L(t) + V_{gap}(t) = I(t)R + L\frac{\delta I(t)}{\delta t} + V_{gap}(t) \tag{3.1}$$

To allow for the equation to be programmed and simulated, 3.1 must be discretised from continuous time, (t), to a series of N discrete time steps, $[n]$ (where square brackets indicate discrete time):

$$V_s[n] = I[n]R + L\left(\frac{I[n+1] - I[n]}{\Delta t}\right) + V_{gap}[n] \tag{3.2}$$

$$\text{Where} \quad V_{gap}[n] = E_{gap}[n] + V_q[n]$$

Rearranging 3.2 for $I[n+1]$ completes the discretisation, yielding an equation for the circuit series current at a future time step, from the circuit parameters in the present time-step:

$$I[n+1] = I[n]\left(1 - \frac{R\Delta t}{L}\right) + \frac{\Delta t}{L}V[n] - \frac{\Delta t}{L}V_{gap}[n] \tag{3.3}$$

$$\text{Letting} \quad \omega = \frac{\Delta t}{L} \quad \text{allows 3.3 to simplify to:}$$

$$I[n+1] = I[n]\left(1 - R\omega\right) + \omega V_s[n] - \omega V_{gap}[n] \tag{3.4}$$

The result is a discrete difference equation describing how the circuit changes from one time-step to the next in the presence of a DC arc failure. To fully describe the behaviour of the arc, the parameters $\mathrm{E_{gap}}$ and $\mathrm{V_q}$ that sum to

Variable	Units	Definition
V_{DC}	Volts, [V]	The initial voltage at the arc location, just before arc ignition.
α	Unitless	Scaling factor to control the slope of V_q. Provides an analogue to the speed at which arc electrodes burn away.
q	Unitless	Ratio equal to $x_{gap} \div x_{crit}$
$x_{gap}(t)$	Metres, [m]	Separation of electrodes at time t
x_{crit}	Metres, [m]	The electrode separation distance at which the arc begins to collapse
a	Unitless	Scaling factor for E_{gap}. Produces the initial voltage drop at arc ignition.
b	Unitless	Scaling factor for E_{gap}. Produces a voltage drop between arc ignition and collapse.
λ	Unitless	Scaling factor specifically to control the slope of E_{gap}.

Table 3.1: Variable Definitions for Uriarte-Gatozzi Series Arc Fault Model

produce the arc voltage V_{arc} are be substituted with their full expressions from Uriate's original publication [41]. For clarity, the variables defined in these expressions have been included in Table. 3.1.

$$V_q = V_{DC}\left(\frac{1}{2} + \frac{1}{2}\tanh\left(\alpha - q(t,x) - 1\right)\right) = V_{DC}\left(\frac{e^{2q(t,x)\alpha}}{e^{2q(t,x)\alpha} + e^{2\alpha}}\right) \quad (3.5)$$

$$E_{gap} = \frac{1}{2}(a + b \cdot x_{gap}(t))\left(\tanh\left(\lambda \cdot q(t,x)\right) - \tanh\left(\lambda \cdot (q(t,x) - 1)\right)\right) \quad (3.6)$$

$$\text{Where} \quad \alpha = -\frac{1}{2}\ln\left(\frac{R_{Electrodes} \cdot \left(\frac{V_{DC}}{R + R_{Electrodes}}\right)}{V_s[n=1]}\right)$$

In 3.5 and 3.6, the ratio q is a function of both electrode position (x) and time (t). Imposing the condition that the electrodes move at a constant

speed, s, (matching the fixed electrode speed used for empirical forced failure arc faults described in this work), then the position dependacy can be resolved, and q made purely time-dependant:

Hence,

$$q(t,x) = \frac{x_{gap}(t)}{x_{crit}} = \frac{t \cdot s}{x_{crit}}$$

Substituting this into 3.5 and 3.5 yields:

$$V_q = V_{DC}\left(\frac{1}{2} + \frac{1}{2}\tanh\left(\alpha - \frac{t \cdot s}{x_{crit}} - 1\right)\right) = V_{DC}\left(\frac{e^{2\frac{t \cdot s}{x_{crit}}\alpha}}{e^{2\frac{t \cdot s}{x_{crit}}\alpha} + e^{2\alpha}}\right) \quad (3.7)$$

$$E_{gap} = \frac{1}{2}(a + b \cdot t \cdot s)\left(\tanh\left(\lambda \cdot \frac{t \cdot s}{x_{crit}}\right) - \tanh\left(\lambda \cdot \left(\frac{t \cdot s}{x_{crit}} - 1\right)\right)\right) \quad (3.8)$$

Discretising 3.7 and 3.8 with $t = n \cdot \Delta t$ yields:

$$V_q = V_{DC}\left(\frac{1}{2} + \frac{1}{2}\tanh\left(\alpha - \frac{n\Delta t \cdot s}{x_{crit}} - 1\right)\right) = V_{DC}\left(\frac{e^{2\frac{n\Delta t \cdot s}{x_{crit}}\alpha}}{e^{2\frac{n\Delta t \cdot s}{x_{crit}}\alpha} + e^{2\alpha}}\right) \quad (3.9)$$

$$E_{gap} = \frac{1}{2}(a + b \cdot n\Delta t \cdot s)\left(\tanh\left(\lambda \cdot \frac{n\Delta t \cdot s}{x_{crit}}\right) - \tanh\left(\lambda \cdot \left(\frac{n\Delta t \cdot s}{x_{crit}} - 1\right)\right)\right) \quad (3.10)$$

The discretised forms of the gap voltage, E_{gap}, and variable resistance voltage drop, V_q can then be directly substituted into the circuit difference equation, 3.4, to produce an expression detailing how the series current

changes in the presence of a simulated arc fault with each time step:

$$
\begin{aligned}
&I[n+1] = I[n]\,(1 - R\omega) + \omega V_s[n] \;... \\
&-\;\omega\frac{1}{2}(a + b \cdot n\Delta t \cdot s)\left(\tanh\left(\lambda \cdot \frac{n\Delta t \cdot s}{x_{crit}}\right) - \tanh\left(\lambda \cdot \left(\frac{n\Delta t \cdot s}{x_{crit}} - 1\right)\right)\right) \;... \\
&-\;\omega V_{DC}\left(\frac{1}{2} + \frac{1}{2}\tanh\left(\alpha - \frac{n\Delta t \cdot s}{x_{crit}} - 1\right)\right)
\end{aligned}
\tag{3.11}
$$

Similarly, an expression for the load voltage at the current discrete time step can be derived for the circuit shown in Figure. 3.11 by application of Kirchoff's laws, and subsequent subtraction of the discretised arc voltage from the circuit supply voltage, V_s:

$$
\begin{aligned}
&V_{Load}[n] = V_R[n] + V_L[n] = V_s[n] - \;... \\
&-\;\frac{1}{2}(a + b \cdot n\Delta t \cdot s)\left(\tanh\left(\lambda \cdot \frac{n\Delta t \cdot s}{x_{crit}}\right) - \tanh\left(\lambda \cdot \left(\frac{n\Delta t \cdot s}{x_{crit}} - 1\right)\right)\right) \;... \\
&-\;V_{DC}\left(\frac{1}{2} + \frac{1}{2}\tanh\left(\alpha - \frac{n\Delta t \cdot s}{x_{crit}} - 1\right)\right)
\end{aligned}
\tag{3.12}
$$

Together, the expressions in 3.11 and 3.12 allow for the calculation of the series current and load voltage for a simulated DC circuit with a passive load, matching the recorded output values for the empirically captured DC series arc failure in Figure. 3.4. Additionally, through enforcing a fixed electrode speed on the simulated arc difference equations, the simulated failure therefore matches the experimental setup for the arc failures presented in Figure. 3.4, allowing for a direct comparison. Both 3.11 and 3.12 were programmed into a MatLab/Simulink simulation of the circuit shown in Figure. 3.11, and the simulated outputs compared directly to the empirical

Variable	Description	Simulation Value
V_{DC}	DC Supply Voltage	400 [V]
α	V_q Scaling Factor	2.67
s	Electrode Separation Speed	$2 \times 10^{-3}[ms^{-}1]$
x_{crit}	Arc Collapse Distance	$20 \times 10^{-3}[m]$
a	E_{gap} Ignition Scaling Factor	80
b	E_{gap} Collapse Scaling Factor	4000
λ	E_{gap} Slope scaling factor	1.05

Table 3.2: Fitting Values used in Simulated DC Series Arc Failure utilising Uriarte-Gatozzi Series Arc Fault Model

arc failure results as highlighted in Figures. 3.13 and 3.14. The scaling and fitting parameters used in the simulation are provided in Table. 3.2, where both the arc collapse point and electrode speed were set to match a typical forced separation arc as described in this work. For additional clarity, Figure. 3.12 highlights the effects of the key simulation fitting parameters on the simulated load voltage waveform also shown in Figure. 3.14. As per recommendation in the original publication by Uriarte, a small amount of broadband, Gaussian noise was added to q, to provide a crude simulacrum of the noise seen at arc collapse for typical DC series arc failures [41].

It can be observed in both Figure. 3.13 and Figure. 3.14 that the discrete difference equations 3.11 and 3.12 are capable of replicating the macro-scale behaviour of the arc fault seen in the empirically captured fault when embedded in a circuit simulation. Simulated traces show an initial reduction in both series current and load voltage at arc ignition, as well as a progressive reduction in magnitude throughout the arc fault, similar to that seen in the experimentally captured arc fault. It can however be observed that the simualted arc fault "overshoots" at arc collapse, resulting in negative value for both series current and load voltage not seen in the real arc data capture. Additionally, at the point of arc collapse the simulated current and voltage do not fall to zero as quickly as in the real arc data,

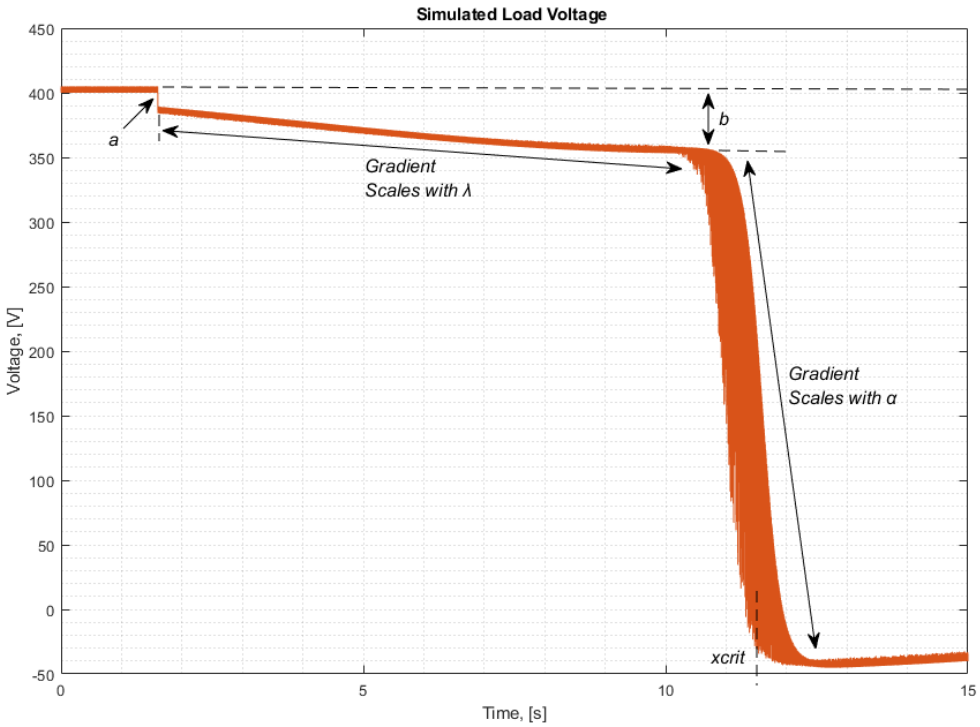


Figure 3.12: Annotated Load Voltage Trace for Simulated DC Series Arc Failure Utilising a Modified Uriarte-Gatozzi DC Arc Model

instead sloping off gradually. Whilst adjustment of the slope parameter λ can increase the rate at which the arc falls, this exacerbates the previously described overshoot after arc collapse, resulting in a much more negative current or load voltage that does not match the empirical data.

Whilst the fault model does appear to able to model the macro-scale behaviour of the arc, it falls short when considering the smaller, micro-scale behaviour of the arc. It can be seen that in both Figure. 3.13 and Figure. 3.14 the model fails to represent the momentary transient behaviour of the arc at ignition. This transient is present in all empirically captured arc failures, scaling in magnitude with the electrode separation at arc ignition, and is a fundamental feature of DC series arc faults. The non-inclusion of this behaviour in the simulated arc failures will potentially reduce its reliability for the testing of arc detection methods, as it is missing critical

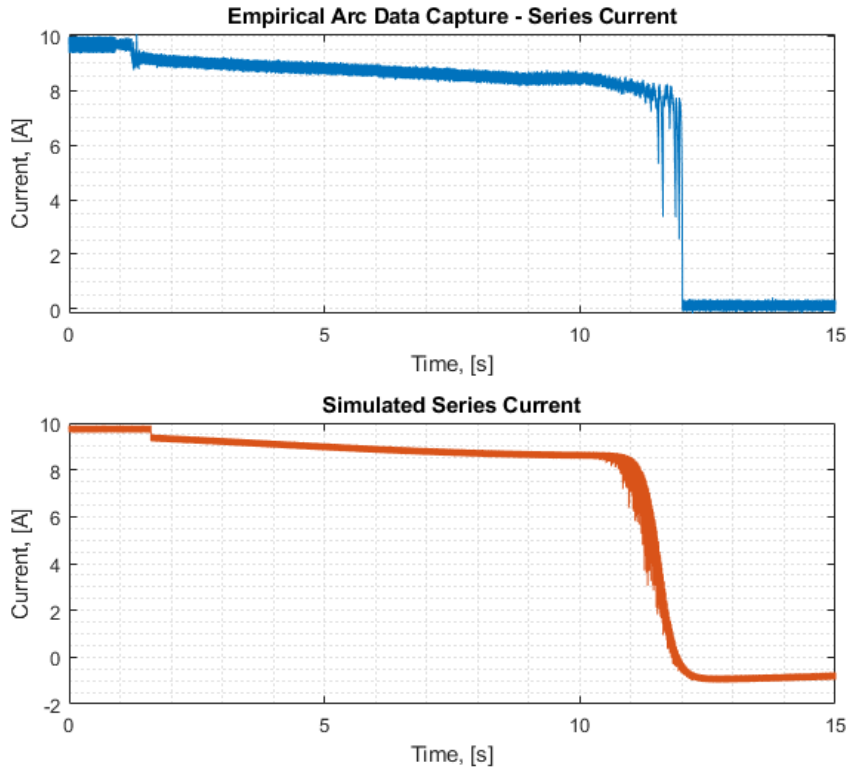


Figure 3.13: Comparison of Series Current for Simulated DC Series Arc Failure to Empirically Captured DC Series Arc Fault Data, Utilising a Modified Uriarte-Gatozzi DC Arc Model

information about the arc fault that is otherwise present in all other non-simulated, "real-world" arc failures. Therefore, detection methods built on this simulated data may be more vulnerable to missed detections than those built on empirically captured data, due to the fundamental differences between them. This is of greater concern with the difference between simulation and real data being so close to arc ignition, as the few moments following arc ignition are the most important for fast arc detection. Ideally, an arc detection method will react to the introduction of the fault in the milliseconds after the arc has formed, and hence the simulated data with its missing information is not conducive to producing an arc detection technique that focuses on the introduction of the arc to the circuit.

Similarly, the transient behaviour of the simulated arc data in Figs. 3.13

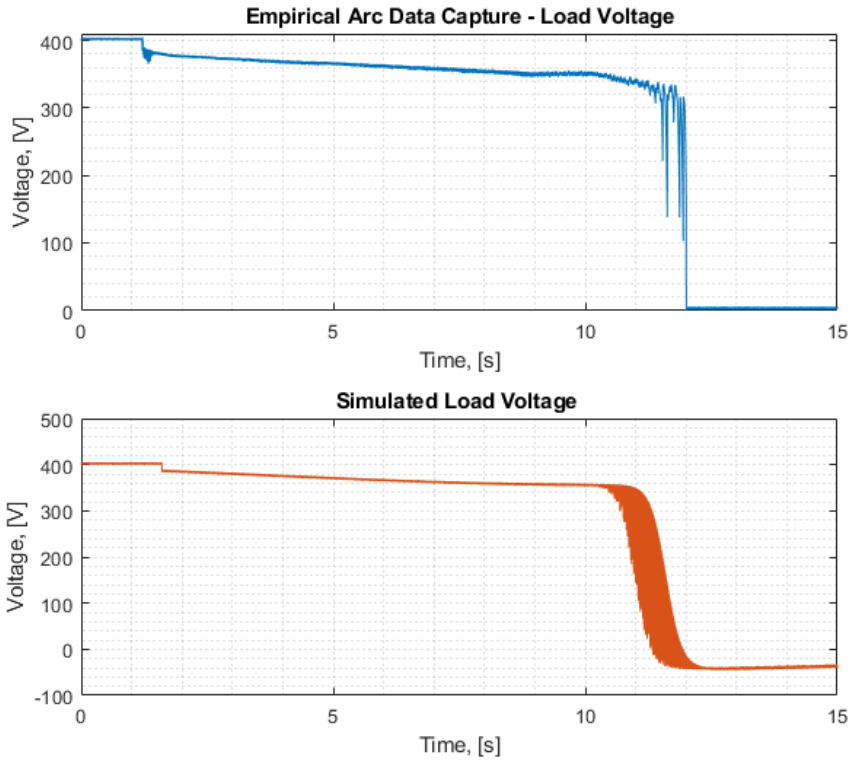


Figure 3.14: Comparison of Load Voltage for Simulated DC Series Arc Failure to Empirically Captured DC Series Arc Fault Data, Utilising a Modified Uriarte-Gatozzi DC Arc Model

and 3.14 near the arc collapse at 11 s >= t > 12s is in no way representative of the behaviour of the experimentally captured arc fault over the same period. Where the empirical data shows oscillation based on changing arc impedance and arc length, with intermittent spiking due to the sudden collapse and re-ignition of the arc, the simulated data shows only the application of broad-spectrum Gaussian noise added to q during the simulation setup. This added Gaussian noise is additionally present throughout the entire arc fault trace, only growing in scale as the simulated arc begins to collapse. Whilst the addition of Gaussian noise in the Uriarte model does serve to add some randomness to the arc fault trace, it does not accurately represent the behaviour of the arc near collapse, nor throughout the duration of the arc burning phase, and does not replicate the micro-scale behaviour seen in empirical arc fault data captures. This contrast to real world arc failure makes the current simulated arc model unsuitable for the

development of any arc detection algorithm that focuses on more than the macro-scale behaviour of the arc fault. Whilst there is the potential for the further development of the fault model in the future to include more representative arc fault behaviours at smaller time scales, these models do not currently exist in the literature, with many authors defaulting to zero-mean Gaussian distributions and choosing to neglect the chaotic behaviour of the arc [41, 42, 43]. As such development of an arc fault simulation that accurately represents the micro-scale behaviour of the arc is outside the scope of this work, and would require an entire project of future work to complete.

The intention of the work in this thesis is the development of an arc detection algorithm focusing not on the larger scale behaviour of the arc; as in existing impedance and machine learning based methodologies, but instead the smaller-scale circuit transients superimposed onto circuit waveforms by the arc itself. The attempt to produce a simulated version of DC series arc failure through the integration of a discretised Uriate-Gatozzi fault model to a simulated DC circuit has failed to produce an output that correctly represents small-scale arc fault behaviour that is the focus for arc detection in this work. Additionally, the many fitting and scaling factors in the Uriate model require specific tuning to each faulty system to correctly mimic arc behaviour, therefore limiting the proposed benefit of rapidly producing large fault datasets. For the reasons stated above, simulated arc failure is therefore unsuitable for the development of a new arc detection methodology in this case, and development and testing of the arc detection method described in Chapters. 4 and 5 will instead focus on empirically captured arc fault data using the arc generators previously described.

3.3 Chapter Conclusions

This chapter has covered the development of several methods of producing DC series arc failure both experimentally and through simulation. Two bespoke arc fault generators have been built and their capability for repeatable arc fault generation demonstrated through experimentation. The forced separation (drawn) arc generator in Figure. 3.1 was developed to satisfy the requirements for UL1669B compliant arc fault circuit interruption [72, 73], and produces DC series arcs through increasing electrode separation at a constant speed of 2 mm/s. The forced failure generator in Figure. 3.6 was produced to provide an alternative condition for DC series arc ignition, providing an analogue to arc ignition through sudden component failure due too poor manufacture, design or maintenance. Simulated arc faults were produced using a discretised Urairte-Gatozzi arc fault model integrated into a simple passive DC circuit simulation. The simulated results were found to correctly approximate the macro-scale behaviour of the arc, however the simulated model was deemed unsuitable for the development of a fast arc fault detection method, as it could not produce representative micro-scale transient behaviour representative of that found in experimentally captured arc failure. As any fast arc detection algorithm must operate at milli-second scales, the lack of representative arc transient behaviour at this scale that might provide a condition for arc detection was deemed unacceptable. This does highlight the potential for future work in improving the discretised Uriarte-Gatozzi fault model with a model of short-time scale arc transient behaviour that combines the influence of both electrode position, dynamic arc impedance, and stochastic/chaotic arc movement due to air-plasma convection and heating.

Chapter 4

Development of an Arc Detection Algorithm using Fractal Theory

Contents

4.1 Chapter Introduction

As global electrification continues DC circuit architecture is becoming further ingrained into the systems that support modern living, with the continued growth of renewable energy sources, the installation of HVDC sub-sea interconnects and the development of more-electric transportation applications in the automotive, rail, aerospace and shipping industries. Increased reliance on DC circuit architecture, particularly those at higher energy levels, inherently results in a greater risk from DC arc failure, with the potentially consequences of electrical arc failure extending to the loss of property, money, reputation and human life.

Despite the continued research into DC arc fault detection, no single method is a panacea, with each different methodology encountering one or more significant barriers to robust arc detection. Impedance based schemes often struggle to distinguish the arc from normal transient behaviour such as step load changes, or misinterpret nonlinear loads or switching power electronics resulting in false positive detections [2, 22]. Optical techniques require the introduction of expensive, invasive specialist equipment and are adversely impacted by changing ambient conditions, and can lead to false positives in unsealed operating environments. Frequency domain based techniques often require specialist knowledge about the fault and are easily confused in the presence of additional switching noise or circuit transients [2, 17, 36, 37]. Reflectrometry techniques cannot function correctly in large networks with multiple power converters and Machine Learning techniques require large, specific and difficult to acquire training datasets [57, 58, 59, 84].

The shortcomings of existing arc fault detection methodologies, coupled

with the increasing risk of DC arc failure indicates there is still the need for research into fast, reliable arc fault detection methodologies. This chapter documents the development of a novel DC arc detection algorithm that identifies arcing behaviour through detection of superimposed fractal noise. The Windowed Fractal Dimension (WFD) technique developed here was initially published and presented at the IEEE ESARS-ITEC conference in 2023 recorded in [1]. A second paper further developing the WFD method and demonstrating its efficacy across a range of different circuit and load architectures, arc ignition types, common false positive conditions and within networks containing power electronic converters is currently under review for the IEEE Journal of Emerging and Selected Topics in Power Electronics. The following chapter expands on the development of the method, covering the initial hypothesis and supporting theory that underpin the technique, alongside its development in MatLab and the signal processing, conditioning run-time considerations taken at each step.

4.2 Arc Faults and The Theory of Fractal Dimension

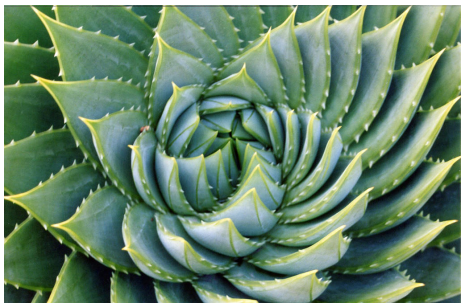
The WFD arc detection method developed in this chapter began as an initial hypothesis: That DC arc faults are essentially scaled-down lightning bolts, and should behave as such. Both are arc-plasma discharges of electricity through the air from a region of higher electrical potential, to a region of lower electrical potential (in the case of lightning, the clouds and the ground respectively). The primary difference between the two is physical size, but otherwise they should display similar characteristics;

characteristics which might be identifiable, and therefore hold the potential for use in arc detection.

One such shared characteristic of arc failures and lightning discharges is that they both been observed to behave chaotically. Intermittent ignition and exhaustion of the arc plasma can create unpredictable transient spikes when observing arcing series current or voltage, similarly the arc superimposes chaotic noise onto the circuit current and voltage waveforms when burning [2, 4, 15, 37, 82, 84, 85]. The chaotic changes seen on circuit waveforms when arcing are representative of changing arc impedance. As the arc burns, the path of the arc fault moves in unpredictable ways, carving a pseudo-random path through the air and changing the overall length of the arc. This in turn results in a change in arc impedance, as an arc of greater length will contain more air-plasma with the resistivity of this plasma determining the arc impedance [15, 75, 76, 77]. As such, the changing arc impedance is in-of-itself representative of the chaotic nature of the arc as it moves, and the consequent changes in circuit current and voltage will also carry that chaotic behaviour. This is paralleled in lightning bolts, as they have also been observed to exhibit chaotic features, specifically fractal behaviour [87, 88, 89, 90].

Fractal geometry is a recent discovery, an extension of chaos theory from Lorenz' work on the chaotic motion of weather patterns in 1963 and Mandelbrot's 1967 paper on mathematical self-similarity [87, 89, 91]. A fractal is defined as a shape with complex geometry, showing a degree of self-similarity at small scales; meaning that a magnified portion of the fractal is resemblant of the shape as a whole. Fractals can be seen readily in nature; in snowflakes, how tree branches form, in snail shells and ammonite fossils,

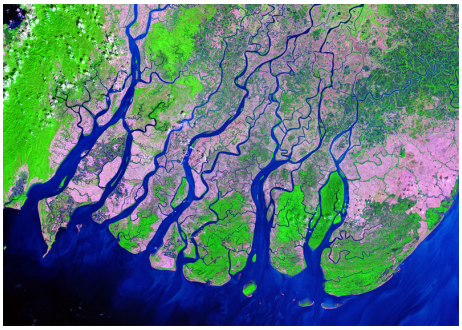
and as previously mentioned, in lightning bolts. In geometry, a fractal is any shape or waveform with a dimensionality that is not an integer value - it is instead, fractional – hence the name. This property of self-similarity at scale is better represented pictorially, in Figures. 4.1 and 4.2 showing fractal patterns in nature (sourced from [92]) and the synthetic fractal, the von-Koch snowflake curve.



(a) Fractal Pattern in Succulent Leaves

(b) Fractal Pattern in Romanesco Broccoli

(c) Fractal Pattern in Nautilus Shell



(d) Fractal Pattern in River Deltas

Figure 4.1: Representations of Fractal Patterns in Nature

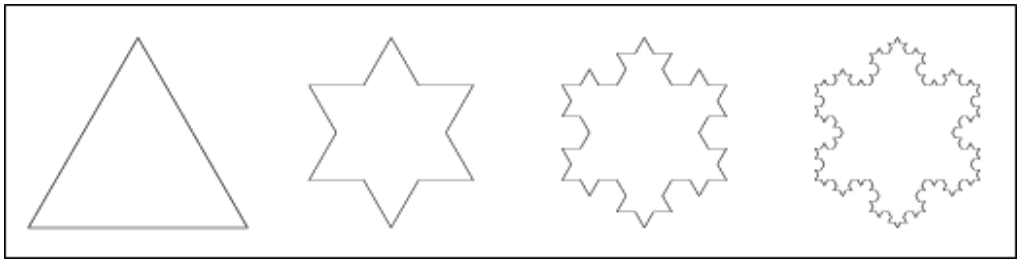


Figure 4.2: Increasing Complexity of Koch Snowflake Fractal Pattern

The Koch snowflake shown in Figure. 4.2 is constructed by taking an equilateral triangle and constructing another equilateral triangle on the inner

third of the length of each side. Repeating this process several times yields the Koch snowflake curve as seen in Figure. 4.2. It can be seen from observation that this curve already represents the fractal property of self-similarity. What is special about the Koch snowflake, is that whilst its original form as an equilateral triangle exists in exactly one dimension as a line on a plane, its more complex snowflake form has a calculated capacity/fractal dimensionality of 1.262 as the number of pattern iterations approaches infinity. This increase in fractal dimension indicates an increase in complexity with scale, and extends to not just the Koch curve, but to many different biological, chemical and electrical phenomena. For any waveform that exists in geometric shape, there is also a measurable dimensionality (separate to the traditional definition of geometirc dimension i.e. 3D represents a cube, 2D a square), capturing how the waveform extends and behaves within this space. If the waveform presents the core fractal properties and therefore has a non-integer fractal dimension, and the fractal dimensionality is associated with a specific system behaviour that can be measured, then fractal dimension can be used as a method of detecting that behaviour. This is becoming common practice in the field of medical electronics wherein fractal dimensions are being used to detect that the body is failing, before the patient shows visible signs [93, 94].

If an arc does behave as a scaled-down lightning bolt, and lightning bolts are observable fractals, then an arc should also behave as a fractal at scale, demonstrating a quantifiable response to measure of scale (fractal dimension), inherent self-similarity and a recursive subdivision of space. The object of this work however is not to empirically classify arcs as fractals through these three behaviours, but to utilise the fractal dimension of the arc as a classifying feature for arc detection. If arcs do behave as fractals

as theorised, then the superimposed arc behaviour injected into the circuit under failure will also be fractal as this is representative of the physical changes in arc length. As such, there should be a noticeable change in system fractional dimension at the onset of an arc failure (arc ignition) and throughout the arc burning phase. Furthermore, as the change in fractal dimension is solely representative of the micro-scale arc noise, it should be inherently be robust to macro-scale behaviours that regularly cause false positive detections in other arc detection methods, such as load step changes and switching, as these are not fractal by nature. Hence, the measurement of electrical system fractal dimension potentially presents a novel and robust methodology for the detection of DC series arc failure.

4.3 Initial Signal Processing and Arc Identification with Fractal Dimension

Before the fractal dimension can be calculated, it is necessary to perform a degree of signal processing and conditioning. Any sampled input signal can be considered as a as a discrete time vector, S[n], with N total samples.

$$S[n] = [s_1, s_2, \ldots, \ s_N] \tag{4.1}$$

The intention of the fractal arc detection method is to identify the change in fractal dimension caused by arcing behaviour, and to omit or disregard anything else. As such, it is beneficial to filter out as much of the non-arcing signal behaviour as possible before computing the fractal dimension. It has been shown from previous study that the significant frequency components

of the arc are below 3500 Hz [2, 8, 81, 84] and that information in this frequency band should be retained. Initially filtering the signal at 25 kHz removes some of the random noise present in the signal and removes components of the switching frequency used by power supplies or any other power electronic converters present (typically 20 kHz or above). As with all filtering, there is a trade off between ensuring signal fidelity and removing unwanted noise. In filtering at >5 times than the 3500 Hz arc content the risk of losing arc information due to weak stop-band attenuation is mitigated, whilst ensuring the removal of the majority of the high-frequency noise that may interfere with later signal processing.

To this end, the time-vector S[n] is then filtered through time domain convolution with a third-order digital low-pass finite-impulse response filter of impulse response h[n], as shown in Figure. 4.3, utilising a 25 kHz cutoff frequency and 60 dB stop-band attenuation. This yields a filtered form of the input signal, $S_{\text{filt}}[n]$:

$$S_{filt}[n] = S[n] * h[n] = \sum_{m=-\infty}^{\infty} h[m]S[n-m] \tag{4.2}$$

In order to allow for real-time arc detection, the input signal must be broken down into smaller, sequential time segments that collectively represent the whole signal in a process known as windowing. For an online method, these "windows" of signal are continuously produced by microcontrollers when fed information from system sensors, and are analysed in sequence, allowing for detection of a fault to occur near-immediately after that fault event depending on the window size. For fast arc fault detection, there is the requirement that the arc be detected a few milliseconds after arc ignition, to allow the time for circuit protection to trip before the arc can

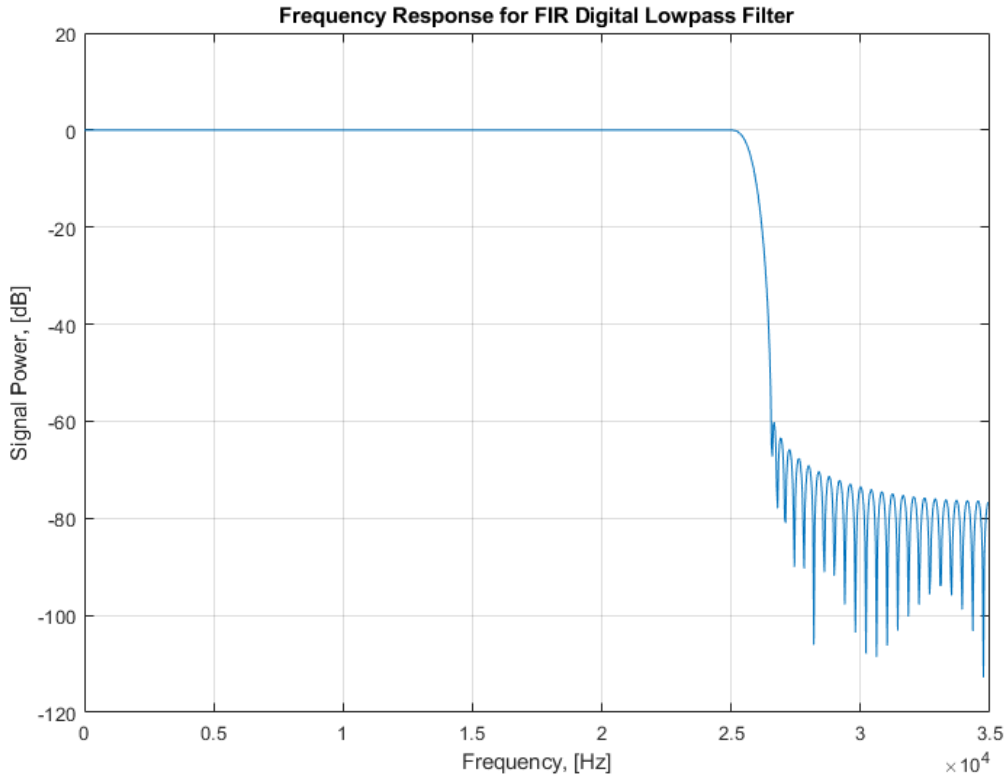
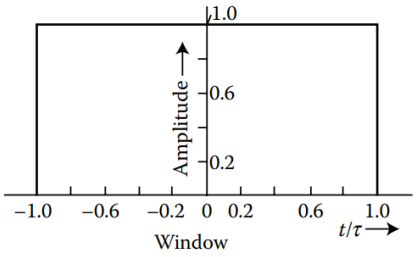


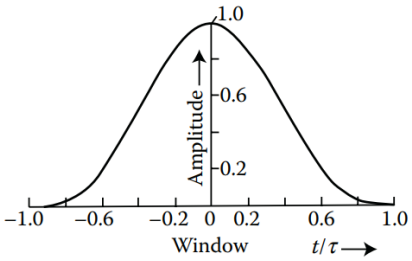
Figure 4.3: Digital Lowpass Filter Frequency Response for WFD Signal Pre-Processing

spread and cause further damage or start fires. Hence, the window size of the arcing signal is required to be small, partitioning the input signal into segments a few-milliseconds in length maximum. This by extension comes with a trade off, as whilst smaller signal windows will result in faster detection, they also contain less samples of the input data and by extension less information is available to identify faulty behaviour, and may therefore result in missed detections.

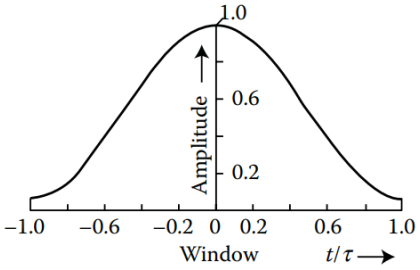
For pre-recorded data, windowing of the input signal is achieved through multiplication of the input signal with a windowing function, W[n], of the required length. The choice of window function varies depending heavily based on application and shown in Figure. 4.4 are several typical examples of filtering windows, including the Rectangular, Hamming and Hann win-



(a) Rectangular Window Function



(b) Hamming Window Function



(c) Hann Window Function

Figure 4.4: Examples of Different Signal Windowing Functions

dow functions, sourced from [49].

In many signal processing applications, a tapered window such as the Cosine-Sum Hamming or Hann windows shown are utilised, as the tapered shape of these window functions helps minimise spectral leakage - a phenomenon whereby new signal frequency components are created when multiplying through a signalling window, changing the relative magnitudes and phase of the frequencies present. Whilst beneficial for ensuring the frequency content of a signal remains unchanged due to spectral leakage, these typical windowing functions adjust the shape of the sampled waveform: Retaining the magnitude at the centre of the waveform, but attenuating it closer the the edge of the sampled window. This makes any type of tapered window function unsuitable for windowing when calculating fractal dimension, as this is a geometric calculation relying heavily on the shape of the input signal where any distortion to waveform geometry could ad-

versely affect accuracy of the calculation of fractal dimension [87, 89, 95]. As such, the rectangular window, despite its propensity towards spectral leakage, is the most appropriate choice for windowing before calculating fractal dimension as it allows the input signal to be windowed, without adversely impacting signal geometry [49].

Hence, windowing of the filtered signal $S_{filt}[n]$ is achieved through multiplication with a rectangular signalling window, W[n], with a window size, N_{win} of 0.5ms (1024 samples at Fs = 2 MHz). This results in a windowed form of the original signal $S_{wind}[n]$, with N_{win} samples, where $N_{win} < N$:

$$\begin{gathered} W[n] = [w(1), w(2), \ldots,\ w(N_{win})\ ] = 1 \\ for \quad 1 < n < N_{win} \end{gathered} \tag{4.3}$$

$$\begin{gathered} \therefore\ S_{wind}[n] = S_{filt}[n]W[n] = [s_{filt}(1), s_{filt}(2), \ldots,\ s_{filt}(N_{win})] \\ for \quad 1 < n < N_{win} \end{gathered} \tag{4.4}$$

In order to compute the fractal dimension, each signal window must be normalised to a unit square, such that the weighting of any units (e.g. Amperes, Seconds) is removed [95]. As fractal dimension is a geometric method, any inherent weighting of the units will skew the geometry of how the signal abscissa and ordinate interact, and therefore will adversely affect the calculated fractal dimension. Performing a unit-square normalisation of the windowed input signal $S_{wind}[n]$ and repeating both the windowing and normalisation for the corresponding discrete time vector t[n] yields a matched, normalised, windowed form of both the input signal and time

vector now ready to compute fractal dimension:

$$\begin{aligned} S_{Norm}[n] &= \frac{S_{wind} - min(S_{wind})}{max(S_{wind}) - min(S_{wind})} \\ &= [s_{Norm}(1), s_{Norm}(2), \ldots,\ s_{Norm}(N_{win})] \end{aligned} \tag{4.5}$$

$$\begin{aligned} t[n] &= [t(1), t(2), \ldots,\ t(N)\ ] \rightarrow t_{Norm}[n] \\ t_{Norm}[n] &= [t_{Norm}(1), t_{Norm}(2), \ldots,\ t_{Norm}(N_{win})] \end{aligned} \tag{4.6}$$

With signal pre-processing complete, it is possible to compute the fractal dimension of the windowed signal portion. Three separate methods were investigated to calculate fractal dimension, namely the Katz, Sevcik and Higuchi approaches [95, 96]. Whilst many approaches for calculating fractal dimension exist, these were selected as useful candidates for arc detection due to their previous applications in mechanical fault detection and medical electronics [93, 94, 97, 98, 99], both applications where-in real-time, online calculation of fractal dimension is necessary. Due to the application to fast arc fault detection, it was necessary to select a fractal dimension calculation that favours calculation speed over high-levels of accuracy, as the intention was to indicate a rapid change in fractal dimension, not to pinpoint record the exact value of fractal dimension for an arc fault. To this end, the Sevcik method of calculating fractal dimension was selected as the best choice for fast arc detection, requiring fewer calculation steps than either the Katz or Higuchi approaches whilst still producing a comparatively similar output value for fractal dimension [95].

The process of determining the fractal dimension of a waveform using the

Sevcik method first requires the calculation of the Euclidean length of the input signal, L from the normalised time and sample vectors. The output fractal dimension, FD, can then be determined using L and twice the number of sample steps in the signal window (N' = N_{win} - 1), added to the base value of object dimensionality for a 2-D line (a value of one):

$$L = \sum_{(n=1)}^{(N_{win}-1)} \sqrt{\begin{array}{l}((t_{Norm}(n+1) - t_{Norm}(n))^2 \ \ldots \\ \ + (S_{Norm}(n+1) - S_{Norm}(n))^2\end{array}} \tag{4.7}$$

$$FD = 1 + \frac{\ln(L)}{\ln(2 \cdot N')} \tag{4.8}$$

Following calculation of the fractal dimension for the first signal window, the windowing function moves half of the N_{win} samples (0.25ms) and the process is repeated. The process ends when either the the entire input signal length of N samples has been windowed, normalised and the fractal dimension determined, or runs continuously for an online system monitoring. The half N_{win} change in window position is deliberate, allowing for a 50% overlap of information between adjacent signal windows and is the maximum possible value of window movement that ensures no information about the arc fault is lost, whilst still reducing the required number of windowing steps to capture the entire input signal.

The calculation steps recorded in (4.1)-(4.8) including signal filtering, windowing, normalisation and the computation of fractal dimension collectively form the Windowed Fractal Dimension (WFD) technique for use in arc detection, whilst not yet considering a methodology for detecting arcs using this technique.

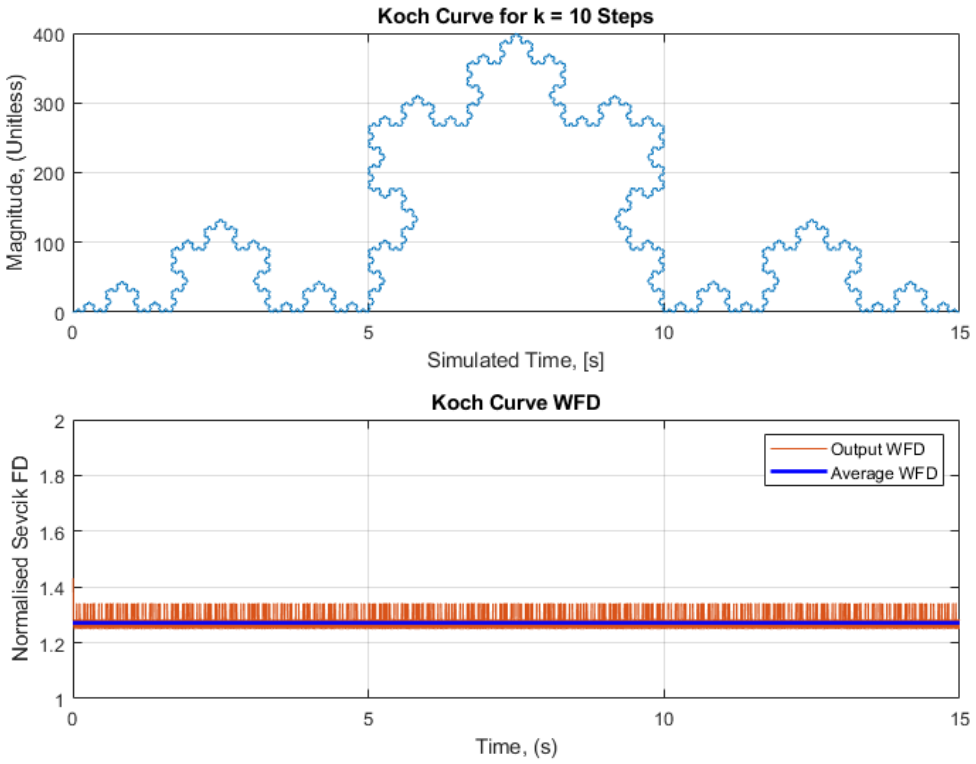


Figure 4.5: Test Application of Windowed Fractal Dimension to Koch Curve

Before application to arc fault detection, it is important to confirm if the WFD technique can accurately determine the fractal dimension of a waveform. Shown in Figure. 4.5 below is both a Koch Curve of known fractal dimension, and the output of the WFD algorithm programmed by the author in MatLab.

The Koch Curve in Figure. 4.5 has been produced with an axis of magnitude and a simulated time to resemble the approximate magnitude and length of the 400 V peak, 15 s arc fault data captures recorded in experimental work. It can also be seen that the Koch curve, due to it's nature as a purely geometric fucntion, has several magnitude values for a single instance in time (for example at t = 5.3s). Whilst his would never be

the case for a regular time domain signal in linear time, the fractal dimension of the Koch curve can still be computed, as despite having being non-linear in the time domain, it is still linear in the sampled, discrete domain; with each sample of time and each sample of magnitude aligning based on their sample number. The multiple magnitude values at equal time values do contribute to the "spikiness" of the output FD waveform however, occurring where each "time-reversal" in the Koch curve occurs. Simply averaging across the WFD output in Figure. 4.5 helps mitigate the influence of the spiking and indicates that the WFD algorithm is working as intended, yielding a fractal dimension of 1.27, very close to the known value of 1.262 for the Koch Curve, with the small difference being expected as the Koch curve was generated using only 10 steps, and only converges to 1.262 as the number of steps used to generate it becomes very large.

With confidence that the WFD technique can correctly identify the fractal dimension of a waveform, the next step is to confirm the initial hypothesis underpinning the detection technique: that arcs will superimpose fractal noise onto the circuit waveform, and produce a significant, detectable change in fractal dimension. Whilst the application of the WFD technique to different arcing waveforms and conditions will be covered in full in Chapter 5, Figure. 4.6 shows a DC series arc failure, produced using forced failure arc ignition from a 400V DC supply voltage and an initial 9.5 A current (pre-arc), to illustrate the response of the WFD algorithm to a typical arc failure.

Inspection of Figure. 4.6 shows clearly the change in fractal dimension at arc onset, and provides validation that the initial hypothesis was correct. It can be seen that the system maintains an RMS value of fractal dimen-

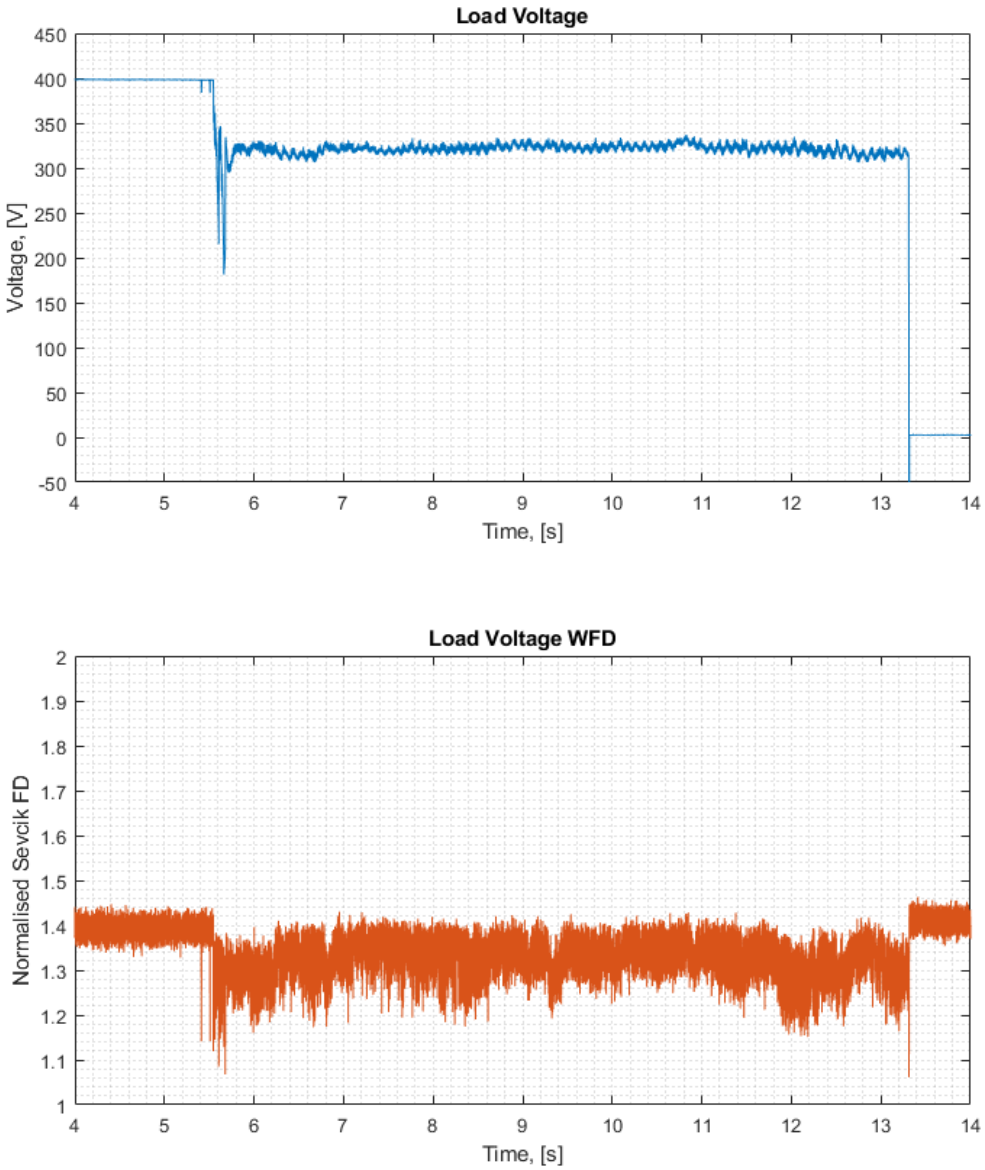


Figure 4.6: Test Application of Windowed Fractal Dimension to DC Series Arc Failure at 400V, 9.5A, with Forced-Failure Arc Ignition

sion of 1.41 during pre-arc behaviour, changing to a value of 1.15 at arc ignition, and retaining an RMS value of 1.26 throughout the arc burning phase. Here, RMS values are utilised as they provide a better representation of signal power than an average, which can be more heavily skewed by outlier results[48, 56]. The initial value of fractal dimension pre-arc is influenced by several factors, the most significant of which are the presence of switching power electronics in the circuit, the combination of noise sources in the circuit, and the window size, N_{win}, of the WFD algorithm itself. As the Chroma 61511 PSU DC power supply present in the circuit is a switched mode supply, it inherently injects regular and repeatable switching noise into the circuit current and voltage waveforms. The square (or sawtooth/triangle) waves used for switching control can be considered through Fourier theory as the sum of progressively reducing magnitude of increasing frequency sine waves. The periodicity of this noise injection alongside the likeness of the injected higher order harmonic frequency components satisfy the the fractal property of inherent self-similarity, and thus contribute to a higher resting value of fractal dimension for the system pre-arc. A further source contributing to the increased fractal dimension at rest (pre-arc) is the inevitable inclusion of fractal pink noise sources in electronic devices, particularly semiconductor devices or magnetic components with regular changes in magnetic domain orientation [100, 101]. The combination of these noise sources in unavoidable in modern electric power systems, and therefore any electric system should be expected to have some baseline, non-integer fractal dimension that differs from the topological dimension of one expected from a voltage/current-time trace (i.e. 2D for a line on a plane, 3D for objects extending out of the plane; where topological dimensions can only take integer values) .

Whilst it may seem counter-intuitive that the introduction of the arc and its fractal behaviour causes the overall fractal dimension to reduce, rather than increase, this is not a-typical behaviour and a reduction in fractal dimension with the presence of a fault or change in behaviour has been utilised elsewhere in medical and mechanical engineering fields for diagnosis of healthy and unhealthy systems [102, 103, 104]. The fractal dimension of a waveform quantifies its complexity as a ratio representing the change in detail of the signal, to a change in scale, and is not strictly a summative relationship [87, 89]. The introduction of additional chaotic features (such as the onset of an arc) to another waveform changes both the level of detail of the signal (i.e. through introducing small scale signal magnitude variations) and the level of scale (the frequency with which these self-similar variations occur). The exact interactions that produce the resulting fractal dimension of two combined continuous fractal functions is highly complex and is a subject of ongoing research and debate amongst mathematicians [105, 106, 107, 108]. Recent work in [105] remarks that for the sum of two continuous fractal functions, the function with the greater inherent fractal properties that define the limits of the calculation of fractal dimension (not directly meaning greater magnitude fractal dimension) will dominate the resultant fractal dimension of their sum. This suggests an explanation for the resulting reduction in fractal dimension at arc onset, seen at t = 5.5s in Figure. 4.6, in that if arc exhibits inherently more fractal behaviour than the base circuit waveform (as theorised) it will dominate the resulting output fractal dimension. Therefore, the change in fractal dimension when the circuit is arcing will likely represent the fractal dimension of the arc itself, rather than the base waveform, be that higher or lower (as observed in Figure. 4.6 and all later arcing WFD traces) than the pre-arc fractal dimension value.

The peak-peak noise on the output fractal waveform in Figure. 4.6 is a feature of the electronic switching and pink noise inherent in the system, but is also a function of the WFD window size, N_{win}. At larger window sizes, the WFD calculation receives a greater number of samples and records fractal dimension over a greater period of time. In a similar fashion to averaging over a larger number of data points, this has the effect of improving the accuracy of the fractal dimension calculation with fewer output results overall (as at larger window sizes N_{win} requires fewer iterations to cover the full N samples in the waveform). The trade-off here is that this massively increases the calculation time of the algorithm by having to process more data-points per window. Additionally the increased window size means a greater length of time between analysis of different signal windows, slowing the "reaction time" of the detection method and imposing a fixed limit on how fast failures can be detected. As detection time is of paramount importance in arc failure detection, a small window size is necessary and the peak-peak noise observable at smaller window sizes cannot be avoided. It is also observable in Figure. 4.6 that the peak-peak noise of the WFD waveform increases after arc ignition. This behaviour is to be expected, as it is representative of the fractal arc noise superimposed onto other circuit noise, increasing the peak-peak magnitude throughout. This in of itself is a boon for arc detection, providing another condition different to "normal" pre-arc behaviour that can be used as a discriminator for arcing behaviour.

The change in fractal dimension, particularly at arc onset, can form the basis for a method of arc detection using the WFD by observing the magnitude of the change in fractal dimension from the systems' baseline fractal dimension pre-arc. The WFD output trace in Figure. 4.6 changes by 18.4% at arc ignition to 1.15 from the pre-arc baseline RMS values of 1.41, and

remains at an RMS value of 1.26 throughout the arc burning phase a difference of 10.6%. A simple threshold-based detection scheme can therefore be employed, producing an output trigger and indicating an arc has been detected when a the threshold has been passed for a fixed period of time (or number of samples).

To that end, a threshold based detection scheme was applied to the existing WFD algorithm. The detection threshold is determined by first taking the RMS value of fractal dimension for normal, non-arcing behaviour during the first eight signal windows (4ms) to provide a baseline value of fractal dimension that is representative of the circuit to be protected. This step also serves to minimise commissioning time, as the threshold value can be programmed to be calculated automatically if preferred, reducing the requirement for manual tuning. The detection threshold is then set as $\pm$ 10% of this pre-arc baseline value. This value was determined by calculating the Receiver Operating Characteristic (ROC) for detection threshold values ranging from $\pm$ 5% to $\pm$ 17.5% of the pre-arc WFD RMS value. The ROC is an iterative graphical technique derived from broader signal processing theory, used in psychology, medicine and machine learning applications to assess the performance of a binary classification system (or compare diagnosis and misdiagnosis within the medical field), but also sees use in the tuning of detection thresholds, having more traditionally been applied to submarine and aerial radar during and after World War 2 - even the name of this technique "Receiver Operating Characteristic" is a holdover from its use in submarine applications [102, 109, 110]. To tune the detection threshold, the ROC is produced by first calculating the True Positive Rate (TPR) using (4.9) and False Positive Rate (FPR) using (4.10) from the number of true positive, false positive, false negative and

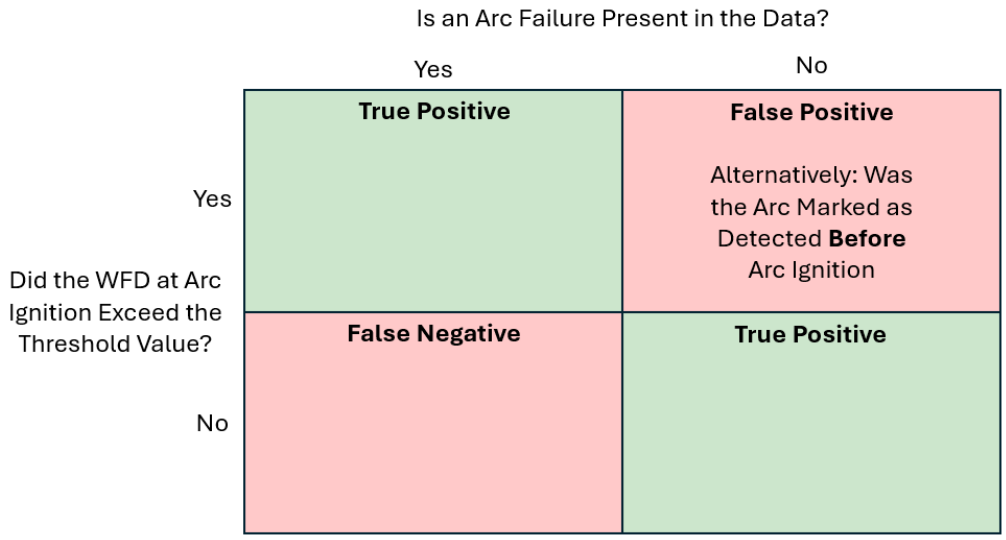


Figure 4.7: Decision Matrix for Classification of WFD Threshold Performance

true negative results for application to a range of test conditions at each different test threshold value. The ROC curve is the generated by plotting the TPR versus the FPR for all tested threshold values, with the threshold with the highest TPR and smallest FPR being the optimum choice, producing the most correct detections with the smallest rate of error [109, 111].

$$TPR = \frac{\#\text{ of True Positives}}{\#\text{ of True Positives} + \#\text{ of False Negatives}} \tag{4.9}$$

$$FPR = \frac{\#\text{ of False Positives}}{\#\text{ of False Positives} + \#\text{ of True Negatives}} \tag{4.10}$$

Each threshold was applied to 30 data records for passive load arc failures (produced using the circuit shown in Figure. 3.3 and described in Chapter. 3), consisting of 10 forced separation arcs, 10 forced failure arcs, and 10 data records where the circuit was run in the absence of an arc fault (under normal conditions). For each set of arc fault test data, potential threshold value and for both load voltage WFD and series current WFD outputs the

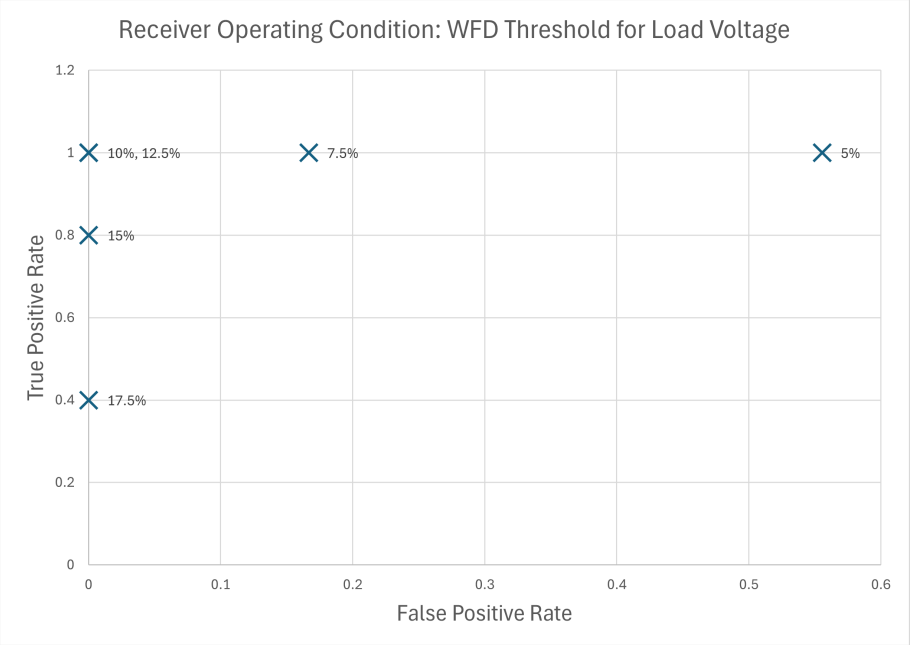


Figure 4.8: Receiver Operating Characteristic for Load Voltage WFD Detection Thresholds Ranging From ± 5% to ± 17.5%

response of the WFD method was recorded as either true positive, false positive, false negative or true negative as described in the decision matrix shown in Figure. 4.7, and the True Positive Rate (TPR) and False Positive Rate (FPR) calculated using (4.9) and (4.10). Figures. 4.8 and 4.9 show the annotated ROC curves comparing detection thresholds ranging from ± 5% to ± 17.5% for both load voltage WFD and series current WFD produced in this way.

It can be seen in Figure. 4.8 that a ± 10% and ± 12.5% both produced an ideal response from the ROC optimisation for load voltage WFD, with a TPR of 1 (meaning that all arcs were successfully identified) and a FPR of 0 (meaning that no erroneous results were identified). Similarly, in Figure. 4.9 a TPR of 1 and a FPR of 0 can also be observed for the ± 10% detection threshold. Also highlighted in both Figure. 4.8 and Figure. 4.9 is that a reduction in detection threshold value results in an increase rate of false positive detections (that would result in nuisance tripping in a practi-

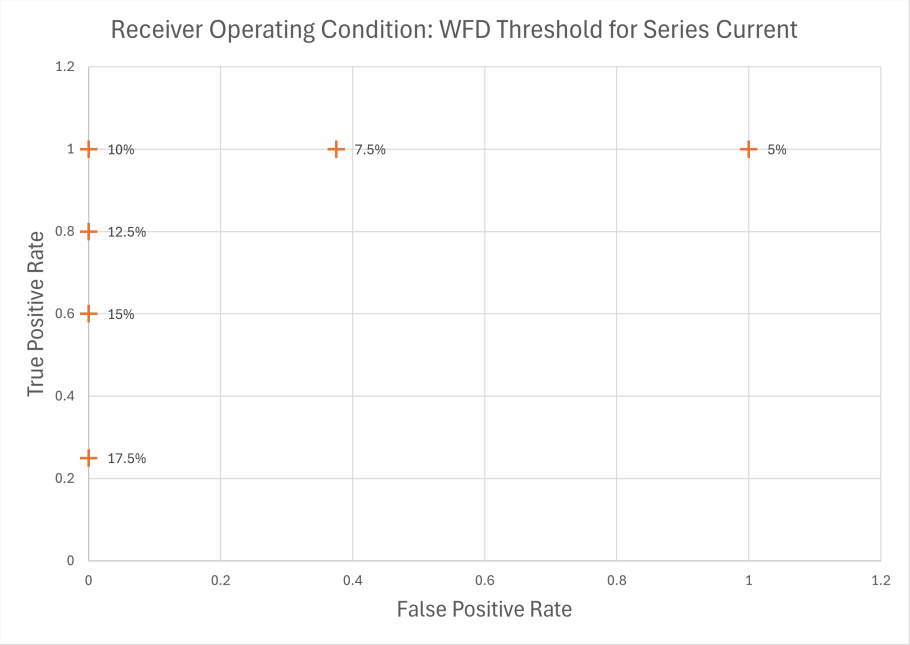


Figure 4.9: Receiver Operating Characteristic for Series Current WFD Detection Thresholds Ranging From ± 5% to ± 17.5%

cal setting). Similarly, an in increased value detection threshold reduces the True Positive Rate, corresponding to more missed detections and therefore allowing arcs that would continue to burn and potentially lead to circuit damage. Together, both Figs. 4.8 and 4.9 suggest an optimum detection threshold of ± 10%, providing a balance of accurate arc detection from the WFD output, whilst keeping false positives and missed detections to a minimum. Other threshold values similar to a ± 10% (for example ± 9%) are possible, but would require further testing to be added to the ROC chart, and provide no additional benefit as the ± 10% threshold shows ideal characteristics in both the load voltage ROC chart in Figure. 4.8 and the series current ROC chart in Figure. 4.9. The change of ± 10% is significant enough a change to detect a fault during both arc ignition and arc burning, as seen in Figure. 4.6, has been verified through comparison of the performance of several detection thresholds in Figs. 4.8 and 4.9, and is further validated on other arc fault traces later in Chapter. 5

If any window of the signal WFD output surpasses the detection threshold, therefore producing a change in fractal dimension greater than ± 10% from the pre-ignition RMS baseline value, an output trigger is recorded. Should the trigger have been firing for three consecutive windows or more, a signal interrupt is produced alongside a digital logic output, and the WFD calculation loop terminates. As each signal window is 0.5 ms in size, this yields a detection time of just over 1.5 ms to detect the arc from arc ignition. The digital logic output can then be used to trigger any existing circuit protection and to signal that an arc has been detected. The 3-window, 1.5ms detection time was deliberately chosen to provide fast arc detection from arc onset and was deemed sufficient for the test setup recorded in Chapter. 3, whilst being sufficiently large to disregard any short-time (µs) transient spikes in fractal dimension that may come about in the presence of large step changes in signal magnitude. Whist a detection time of 1.5 ms is possible, this is still dependant on a consistent change in WFD output magnitude at arc ignition. An arc with a rapidly changing initial transient as it ignites, perhaps caused by momentary ignition and collapse of the arc, can affect the value of the WFD, with the transient behaviour of ignition and collapse briefly disturbing the fractal noise imposed once the arc is established. In such cases detection would require more signal windows before detecting the arc to allow the transient behaviour to settle and the fractal dimension to be unobscured.

Application of the WFD and threshold based detection scheme to the same arcing load voltage waveform as in Fig 4.6 is shown in Figure. 4.10 and again in Figure. 4.11, cropped between t = 5.5s and t = 5.6s to better illustrate when arc detection occurs after arc ignition.

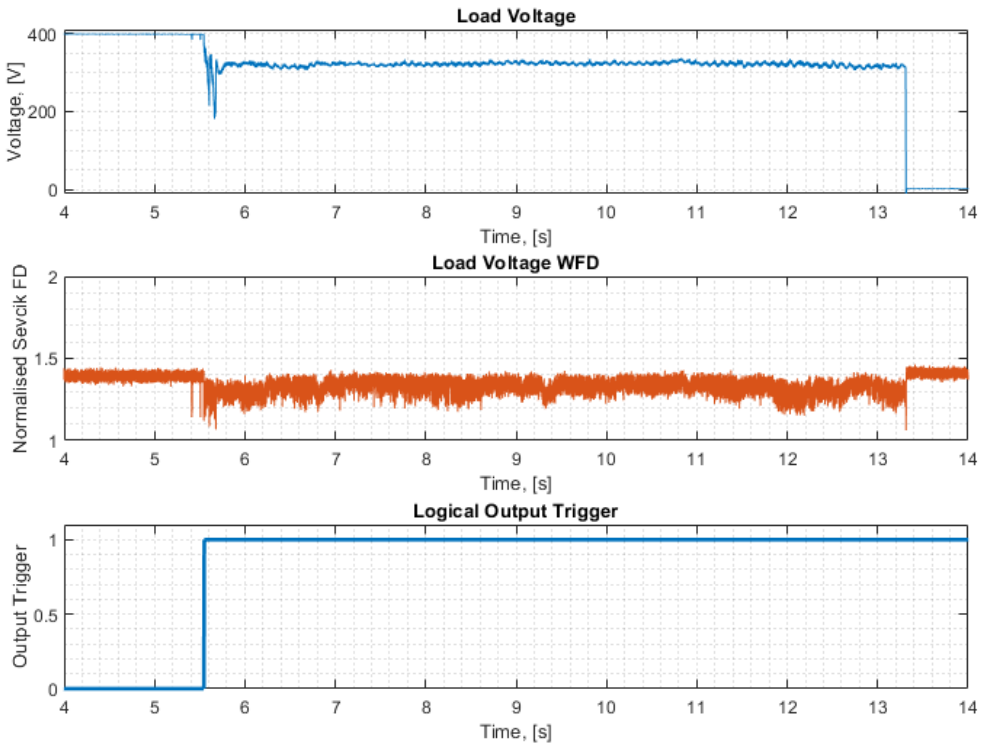


Figure 4.10: Test Application of Windowed Fractal Dimension to DC Series Arc Failure at 400V, 9.5A, with Forced-Failure Arc Ignition, with Detection Trigger

It can be observed in Figure. 4.11 that for this particular waveform the arc detection trigger is output, 0.00406s (or 4.06ms) following arc ignition, slower than the minimum possible detection time of 1.5ms, but not massively so. This is as described earlier, with the initial transients seen at the moment of arc ignition causing a momentary disturbance to the calculation of fractal dimension, but resolving quickly afterwards. The 2-3 ms increase in detection time due to arc ignition transients is inconsequential in practice, as a <5ms detection time is still fast when compared to the 30ms or more required for typical DC breakers to trip [76, 77], and when compared to other arc detection methodologies that regularly require more than 50 ms to indicate an arc failure [57, 58, 59].

The combination of both identification of fractal properties from short-time

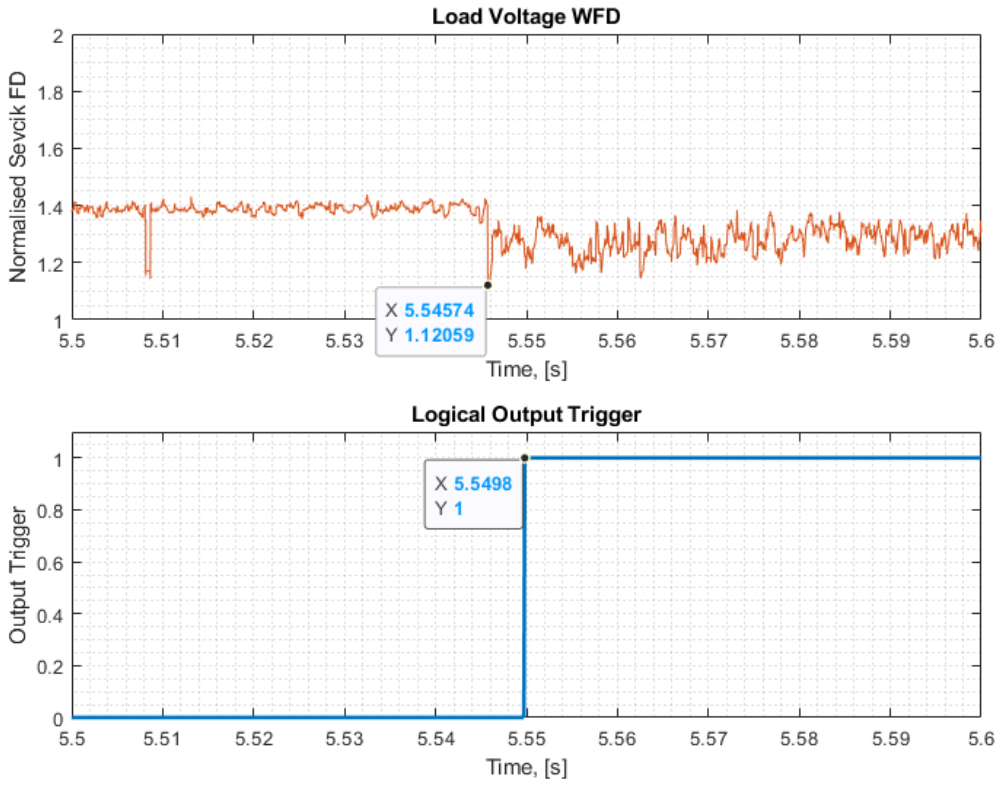


Figure 4.11: Test Application of Windowed Fractal Dimension to DC Series Arc Failure at 400V, 9.5A, with Forced-Failure Arc Ignition, with Detection Trigger, Cropped to t = 5.5s and t = 5.6s

signal windows and the production of a digital output using a threshold based detection scheme form the Windowed Fractal Dimension (WFD) arc detection algorithm in its completed form. The completed method is summarised as a flowchart in Figure. 4.12 where it is divided into both WFD calculation and arc detection steps for clarity.

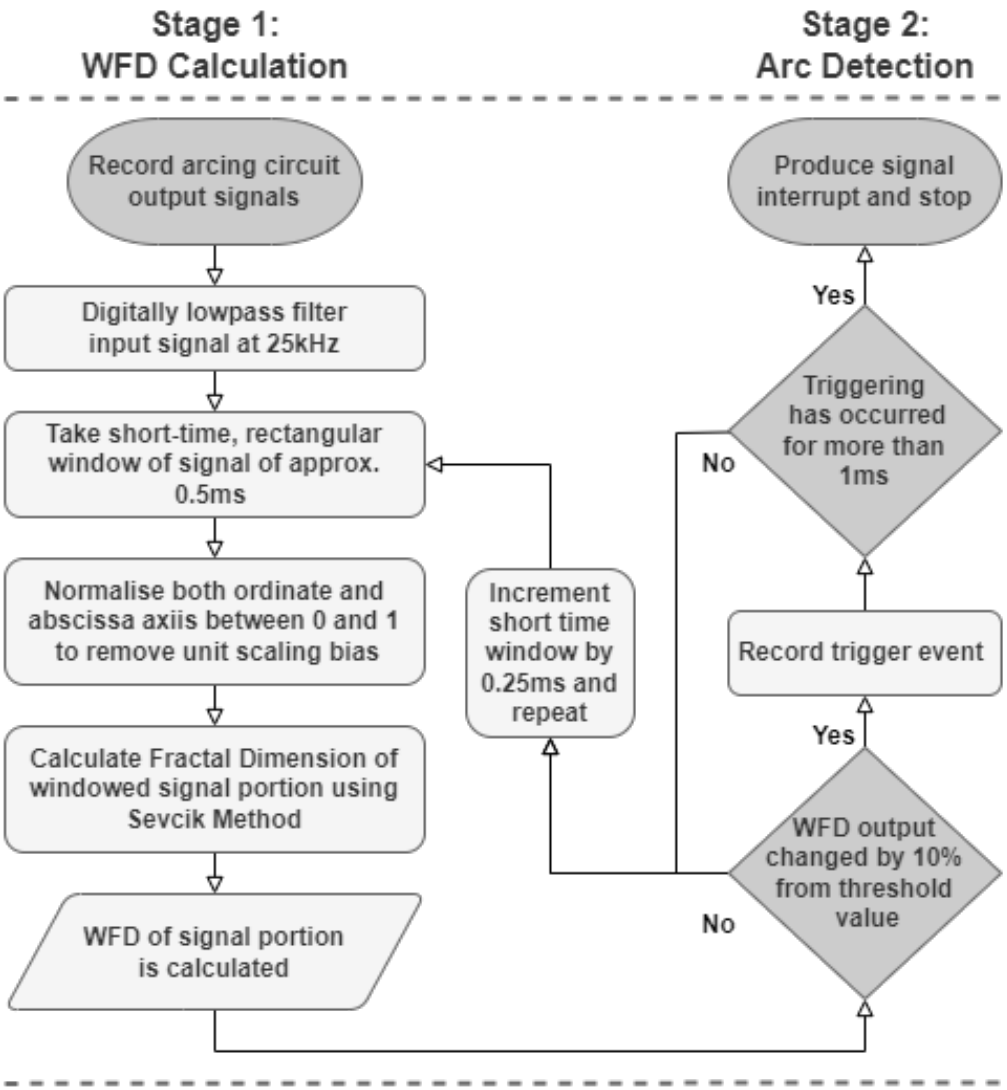


Figure 4.12: Flowchart Documenting the Process of the WFD Algorithm with Calculation and Detection Stages Highlighted

4.3.1 Run-Time and Signal Fidelity Considerations

Throughout the development of the WFD arc detection algorithm, several steps were taken to ensure that the runtime of the algorithm was minimised, as any introduced calculation delays would delay the detection of an arc failure.

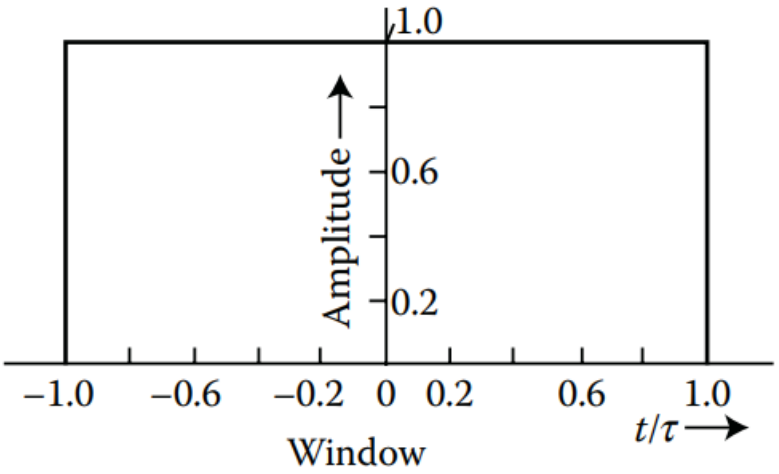
One such consideration was the sizing, overlap and frequency of input signal windows used to discretise input signals to the WFD algorithm. As previously discussed, signal windows of increased size result in a greater calculation time per window as the WFD algorithm is applied to a larger number of sampled data points. Too small a signal window however does not capture enough of the input data points to accurately calculate fractal dimension, as the windowed signal becomes functionally "blind" to the signal as a whole, and is less representative of the input signal in its entirety. As such, there is a trade-off between calculation accuracy and runtime when choosing window size. For the WFD algorithm documented in this chapter, a window size of 0.5 ms (or 1024 samples at Fs = 2 MHz) was deemed appropriate for arc detection. This allowed for accurate calculation of fractal dimension using the Koch Curve test waveform in Figure. 4.5 whilst retaining the detection speed of the algorithm, allowing for arc detection within a few milliseconds of arc ignition.

The amount by which signal windows overlap, and hence the frequency at which windowing occurs, also presents a trade-off between calculation speed and accuracy (specifically, window amplitude response flatness). In the WFD algorithm described here, signal windows of 0.5 ms in length are incremented by 0.25 ms in time before WFD calculation is repeated.

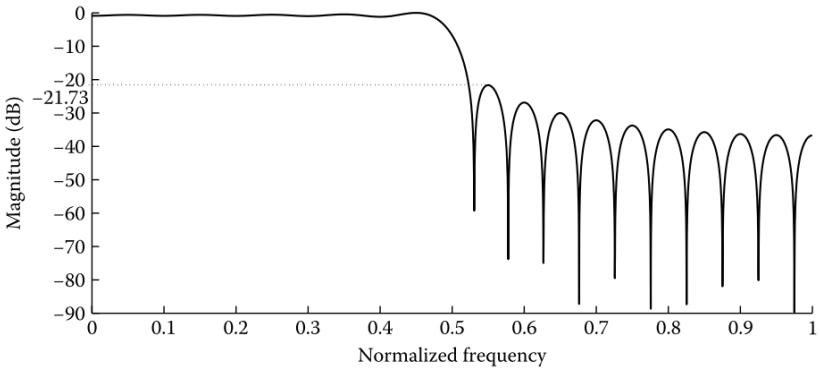
This allows for a 50% overlap of information between each adjacent signal window and is the minimum possible value of window overlap to ensure no information is lost and prevent amplitude losses for a rectangular window function (though this value of minimum overlap is higher for shaped window functions) [112]. Whilst the amplitude loss caused by insufficient window overlap may not seem obvious in the time domain (as a rectangular window has a constant value of 1 in the time domain), the effect is clearer in the frequency domain magnitude response, where it can be observed the windowed signal power is reduced at higher frequencies as shown in Figure. 4.13 (sourced from [49]).

At the edges of the signal window, spectral leakage results in the spread of signal power to higher frequency sidelobes that are inherently magnitude attenuated. This has the effect of obscuring the portions of the signal closer to the window edges as they experience an effective amplitude reduction. In overlapping the signal windows, the spectral leakage at the edges of window function becomes less of an issue, as the signal data at the window edge would be present in the centre of the next signal window as illustrated in Figure. 4.14. As such, no windowed portion of the signal is contributing more than another and the windowing process provides an unbiased representation of the signal as a whole.

The amount by which the signal windows overlap also influences the amount of windows of size N_{win} required to fully encapsulate a signal of N total samples. As seen in Figure. 4.14 reducing the overlap of neighbouring signal windows reduces the total number of windows required to fully process the input signal, therefore reducing the computational burden as fewer signal windows means fewer required calculations. This does however result in

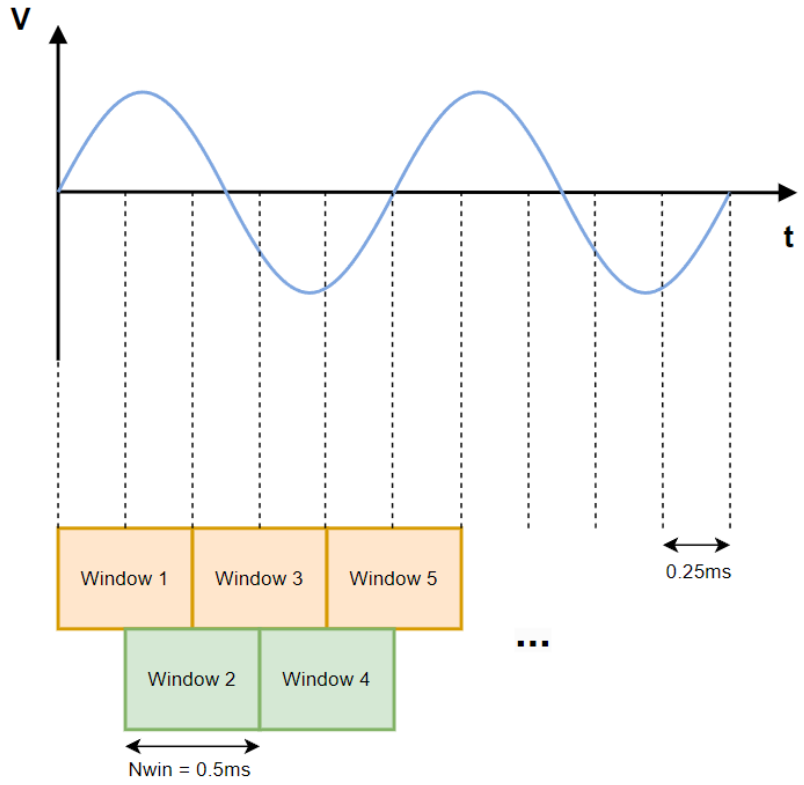


(a) Rectangular Window Function

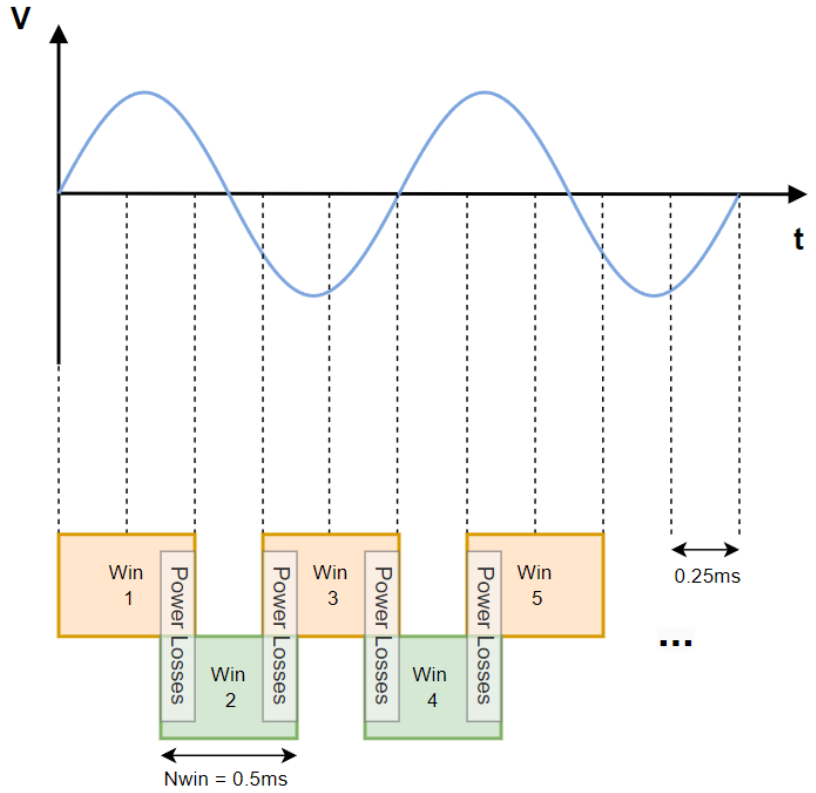


(b) Rectangular Window Normalised Frequency Magnitude Response

Figure 4.13: Rectangular Window Function and its Frequency Magnitude Response



(a) Signal Windowing with 50% Overlap



(b) Signal Windowing with Insufficient Overlap

Figure 4.14: Illustration of Spectral Leakage Power Loss with Insufficient Window Function Overlap

a reduction in signal fidelity as previously discussed. The converse is also true, with a greater window overlap resulting in a more accurate signal discretisation, but increasing the required number of calculations and potentially slowing the detection speed of the algorithm. Considering the trade off between runtime and accuracy, a window overlap of 0.25 ms (or 50% N_{win}) was deemed sufficient for the WFD calculation, allowing the minimum amount of overlap to maintain discretised signal fidelity, without significantly increasing runtime.

In this thesis, all WFD implementations demonstrated are performed offline in MATLAB using pre-recorded data. In order to determine the WFD algorithm's suitability for online implementation, the MatLab version of the WFD technique was profiled using MatLab's SoC blockset algorithm analyser. Results found the compiled code to require 492,000 floating point operations for each signal window, i.e. 1.968 million operations per millisecond. Modern mid-range field-programmable gate array (FPGA) integrated circuits are capable of calculating more than several thousand millisecond floating point operations per second (FLOPs). Noting that none of the code in this project has yet been optimised for real-time performance, there should be little issue running an online-optimised WFD implementation on modern FPGA architecture such as the Intel 7-Series FPGA (with a floating point performance of 2000 GFLOPs). Online implementation of the WFD algorithm for real-time arc detection can therefore be considered completely feasible for future projects and circuit protection, but was outside the scope of this work.

4.4 Chapter Conclusions

This chapter has documented the development of the Windowed Fractal Dimension algorithm for DC series arc detection, with MATLAB functions provided and captured in Appendix. B. The initial hypothesis that arc failures introduce detectable fractal noise has been confirmed, and the WFD algorithm has been assessed to determine accurate calculation of fractal dimension. A theoretical detection time of 1.5 ms from arc ignition has been predicted, with practical implementation on empirical arc fault data demonstrating an output trigger produced 4 ms after the arc begins. This highlights an improvement of several milliseconds over other detection methodologies, an order of magnitude in some cases, and indicates that the algorithm can provide rapid fault detection sufficient to trigger circuit protection. Special consideration has been made to ensure that signal fidelity is maintained whilst minimising both runtime and the number of required calculations in the WFD algorithm for future online-implementation. Algorithm profiling using MatLab's SoC blockset indicates that the WFD algorithm is capable of running on modern FPGA architecture for real time arc detection, and should see no reduction in theoretical detection time with future optimisation for real-time operation.

Chapter 5

DC Arc Detection using Windowed Fractal Dimension (WFD)

Contents

5.1 Chapter Introduction

Having defined the Windowed Fractal Dimension technique as a new arc detection methodology in Chapter. 4 it now becomes necessary to test its efficacy on a range of different series arc failures to determine its suitability for real-world application. In this chapter, the WFD algorithm is tested for robustness through application to multiple different circuit and load architectures, different arc ignition types, step load changes, non-linear loads and within networks containing power electronic converters. Throughout, each different condition tested is either representative of a typical more-electric transport power network or a specific fault condition known to frequently trigger false positives within other methods in the literature. Application to multiple arc fault ignition types is also included to go beyond the UL1699B standards for DC arc fault ignition and demonstrate efficacy during an additional, non-typical arc condition [113]. The intention of work presented in the chapter is to show that the WFD arc detection scheme can reliably indicate the presence of a DC arc failure by producing a substantial change in FD of $>= 10\%$ and produce an output trigger within 10 ms of arc ignition. The remainder of the chapter is structured to analyse each different load architecture in turn, including additional fault criteria throughout. Work presented in this chapter follows on from that previously published in [1] and has recently been accepted to the IEEE Journal of Emerging and Selected Topics in Power Electronics.

5.2 Application of Windowed Fractal Dimension for DC Series Arc Detection

5.2.1 WFD Application to Passive Loads

Before more complex load architectures can be considered the WFD algorithm first needs verifying on passive circuit loads, without active components, significant frequency content or switching power electronics. To produce repeatable empirical arc fault data captures for testing, both the forced separation and forced failure arc generators described in Chapter.3 were integrated into the simple circuit diagram shown in Figure. 3.3, also shown in Chapter.3. This initial setup utilises purely passive load components, with the programmable load R_{Prog} left disconnected and acting as an open circuit.

In these passive load experiments, V_{in} was set to supply 400 V DC to the circuit from a Chroma model 61511 power supply. The circuit load $R_{Passive}$ was fixed at 41.7 Ω using a combination of series and parallel connected resistors, with R_{Prog} left as an open circuit. With modern More-Electric Aircraft including several hundred kilometres of wiring at an estimated 1.1 mH/Km, the effects of line impedance also need to be considered [114, 115, 116]. To that end, also included in the test circuit in Figure. 3.3 was a 0.2 Ω, 15.2 mH inductor to represent a combination of stray inductance and transmission line impedance of the power network wiring in a typical More-Electric Aircraft. At 400 V DC the circuit draws 9.55 A of current in steady state, approximating a nearly 4 kW DC supply bus found in smaller MEA applications or heavy-duty more-electric vehicles [78, 79, 80].

A total of 28 experimental arc failures were performed under these conditions with 18 forced separation (drawn) arcs, and 10 forced failure arcs, using the setup described in Chapter.3. For all experiments, the circuit shown in Figure. 3.3 was initially energised, with electrode separation and arc ignition triggered automatically just after 1 s for the forced separation arcs. For forced failure arcs, arc ignition occurs sporadically anywhere between 1-5 s after the circuit is energised, allowing time for the underrated component acting as a fuse to overheat and fail. Repeated in Figures. 3.4 and 3.9 are DC series arc failures produced using the described setup and forced separation and forced failure arc ignition respectively, previously seen and described in Chapter. 3. All captures were recorded at 2 MHz using a Picoscope 5000 series oscilloscope with 15-bit ADC resolution, and are representative of other typical DC series arc failures found in other literature [1, 2, 4, 82, 83].

The load voltage traces for all 28 forced failure and forced ignition passive load arc fault traces were processed using the WFD technique as described in Chapter. 4 and summarised as a flowchart in Figure. 4.12. Shown in Figure. 5.1 and Figure. 5.2 are the WFD output traces for the arcing load voltage waveforms of Figs. 3.4 and 3.9 from Chapter. 3. Similarly, Figs. 5.3 and 5.4 show the WFD application to the series current waveforms of the same trace. Also shown in Figs. 5.1 - 5.4 is an output trigger for each waveform produced using the threshold based detection scheme supplimental to the WFD and described in Chapter. 4, indicating the point of arc detection. Additionally, Table. 5.1 also provides and collates key metrics from the 28 different passive load arc failures and their WFD transformations.

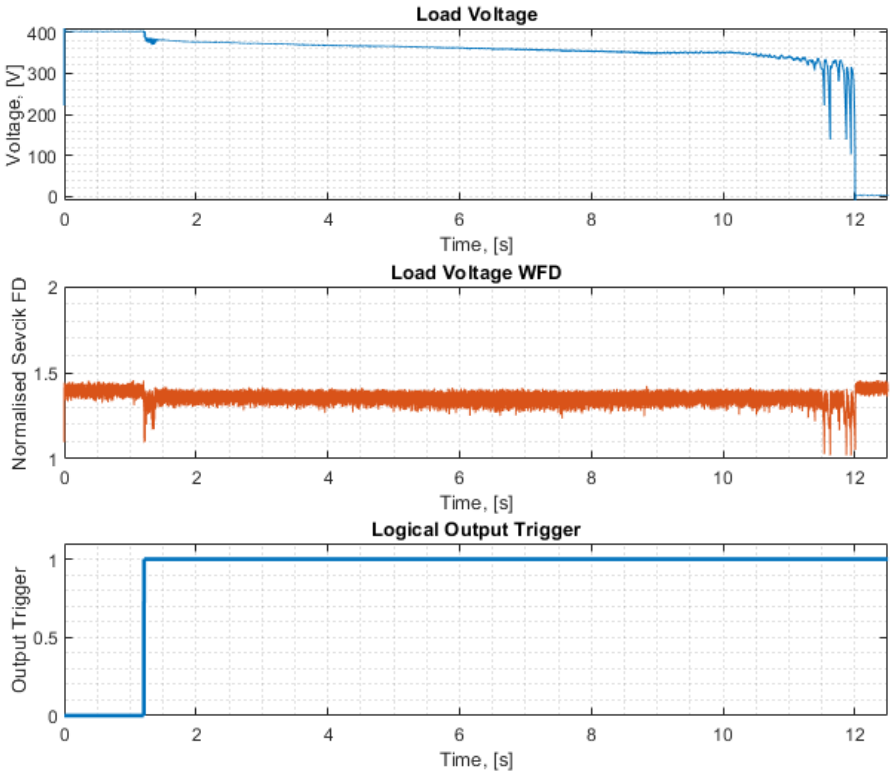


Figure 5.1: Application of WFD to Typical DC Series Arc Load Voltage Waveforms - Forced Separation Ignition, Passive 41.7Ω Load, from t = 0s to t = 12.5s

Table 5.1: Table of Passive Load Condition, Load Voltage, WFD Output Results

Ignition Type	**Mean Pre-Arc WFD Value**	**Mean Arc Ignition WFD Value**	**Mean Change in WFD [%]**	**Repeats**	**Success Rate [%]**
Forced-Failure	1.402	1.094	21.97	10	100
Forced-Separation	1.403	1.136	19.03	18	100

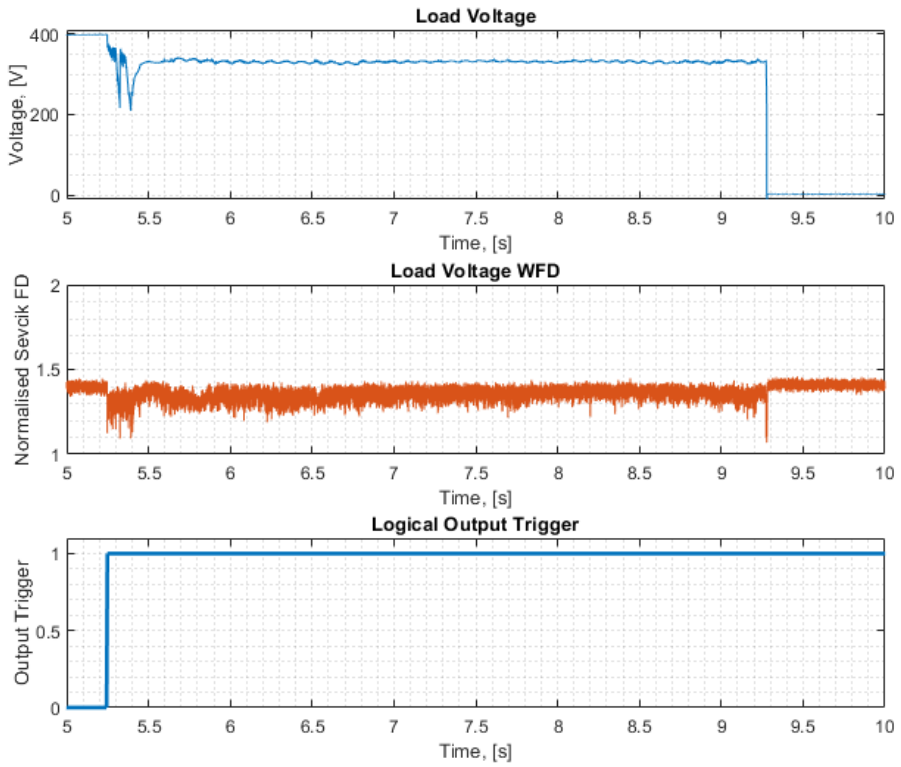


Figure 5.2: Application of WFD Typical DC Series Arc Load Voltage Waveforms - Forced Failure Ignition, Passive 41.7Ω Load, from t = 5s to t = 10s

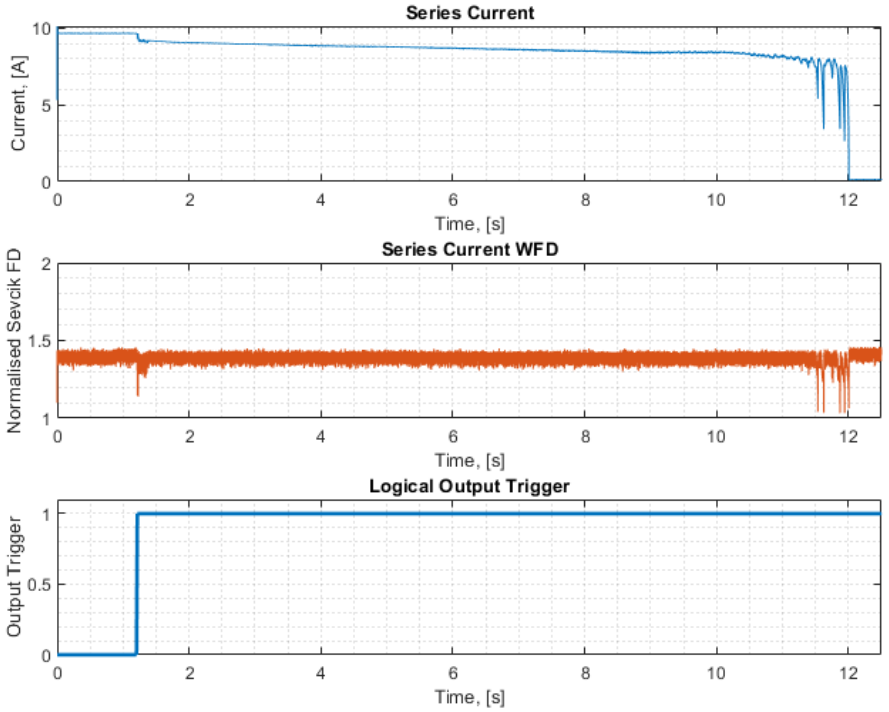


Figure 5.3: Application of WFD to Typical DC Series Arc, Series Current Waveforms - Forced Separation Ignition, Passive 41.7Ω Load, from t = 0s to t = 12.5s

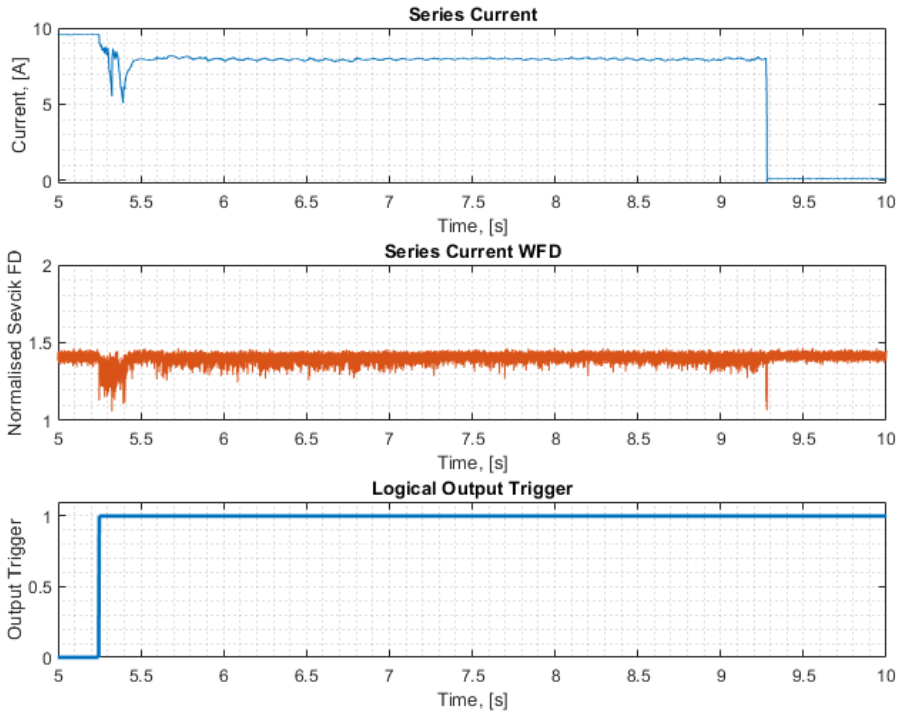


Figure 5.4: Application of WFD Typical DC Series Arc, Series Current Waveforms - Forced Failure Ignition, Passive 41.7Ω Load, from t = 5s to t = 10s

Table 5.2: Table of Passive Load Condition, Series Current, WFD Output Results

Ignition Type	**Mean Pre-Arc WFD Value**	**Mean Arc Ignition WFD Value**	**Mean Change in WFD [%]**	**Repeats**	**Success Rate [%]**
Forced-Failure	1.41	1.15	18.44	10	100
Forced-Separation	1.407	1.24	11.87	18	100

It can be seen in the load voltage WFD traces in Figs. 5.1 and 5.2 that both the forced failure and forced separation arcs produce a measurable change in fractal dimension at arc ignition, significant to detect the arc. In the forced separation arc in Figure. 5.1 the fractal dimension changes from a pre-arc initial RMS value of 1.39 to a value of 1.13 at the point of arc ignition at t = 1.2 s, a change of 18.71% that is significant enough to indicate an arc with the WFD's 10% detection threshold. Comparatively, the series current WFD waveforms in Figs. 5.3 and 5.4 can be seen to produce smaller changes in fractal dimension, both at arc ignition at t = 1.2 s, and throughout the arc burning phase. For the forced separation arc in Figure. 5.3 the WFD output changes by 11.34% from a pre-arc resting value of 1.41 to a value of 1.25 during the arc ignition phase. A reduced response from the series current WFD at arc ignition was seen across all 18 forced separation arc failures when compared to those produced using load voltage as highlighted in Tables. 5.1 and 5.2, with an average % change at arc ignition of 11.87% for series current WFDs, and 19.03% for load voltage WFDs.

Whilst the initial transient is sufficient for arc detection in both load voltage and series current WFD traces, the arc burning phase post-ignition and pre-collapse shows only a 6.5% change in fractal dimension versus the pre-arc resting point in the load voltage WFD in Figure. 5.1, and only a 3.54% change in the series current WFD, both of which would not trigger detection if the initial ignition transient was missed. In the load voltage WFD in Figure. 5.1 however, the change in fractal dimension does increase throughout the arc burning phase, becoming considerably larger during the arc transients near arc collapse starting at t = 11.3 s, where a change in excess of 10% can be seen. The steady increase in WFD output can be considered a result of the increasing arc impedance for the forced separa-

tion arc with increasing arc duration and length, as shown in Figure. 3.10 in Chapter. 3. The increased impedance of the arc causes it to have greater influence over the circuit load voltage waveform, therefore superimposing fractal arc behaviour onto the voltage and current waveforms at a greater magnitude. When processed with the WFD algorithm the larger magnitude transient arc behaviour produces a Euclidean length measure and Sevcik fractal dimension that better represents the fractal nature of the arc, as the arc is now more prominent in the input waveform. The change in fractal dimension just seen before arc collapse, whilst also sufficient to trigger arc detection, is of little use. Here the arc has already been burning for several seconds and would have had ample time to cause circuit damage, and as such arc indication at this point is no longer useful. This effect is not observed in the series current WFD in Figure. 5.3 which shows no additional change in fractal dimension with increasing arc length. The reduced WFD response from the series current WFD versus the load voltage WFD at arc ignition, in addition to limited change in fractal dimension at increasing arc length suggests that it is less suitable for arc detection for forced separation arcs using the WFD technique, as a larger magnitude response from the algorithm at arc ignition is conducive to fast arc detection.

The 18 passive forced separation arcs tested all showed similar behaviour, producing a large change in WFD in the first 0.15-0.2 s following arc ignition, followed by a lesser change in fractal dimension whilst burning that increased gradually over time (with increasing arc length) until arc collapse. Irrespective of the reduced magnitude change in fractal dimension during arc burning, an arc was detected at arc ignition for all 18 repeats, producing an average change in fractal dimension of 18.97%. Given the WFD algorithm can detect an arc within a theoretical 1.5 ms from exceed-

ing the detection threshold, the 0.15-0.2 s of increased WFD output seen shortly after arc ignition are more than sufficient for reliable detection. For the forced separation arc seen in Figure. 3.4 and Figure. 5.1, the fault was detected 1.75 ms after arc ignition as highlighted in Figure. 5.5, with the other 17 remaining showing similar detection times between 1.6 ms to 8.14 ms. It can be seen in Figs. 5.6 and 5.7 showing the WFD traces with the 1.6 ms and 8.4 ms respectively, that the difference in detection time between these traces is possibly due to the intensity of the initial arc transient and the corresponding effect on the WFD. In Figure. 5.6 the shorter 1.6 ms detection time corresponds to a larger period of transient behaviour at arc ignition in the WFD trace when compared to the shorter transient period in Figure. 5.7 and the corresponding 8.14 ms detection time. These results suggest that a series arc failure with a greater initial change at arc ignition (possibly from increased arc impedance due to a larger air-gap or environmental effects increasing the air-plasma resistivity), will likely be detected by the WFD algorithm quicker than an arc with reduced magnitude transient behaviour at arc ignition.

The load voltage WFD for the forced failure arc shown in Figure. 5.2 produces a slightly larger change in fractal dimension of 20% at arc ignition, from a pre-arc resting value of 1.40 to a value of 1.12 at the moment of arc ignition. The trend seen for the forced separation arcs is repeated here, with the series current WFD in Figure. 5.4 showing a reduced magnitude repsponse at arc ignition when compared to the load voltage WFD. In Figure. 5.4 the series current WFD reduces from a value of 1.41 pre-arc to a value of 1.14 at the point of arc detection, a change of 19.15%. The initial transient change at arc ignition lasts for 1.5 s, similar to that seen in the forced separation arc. After the initial transient, the arc burning

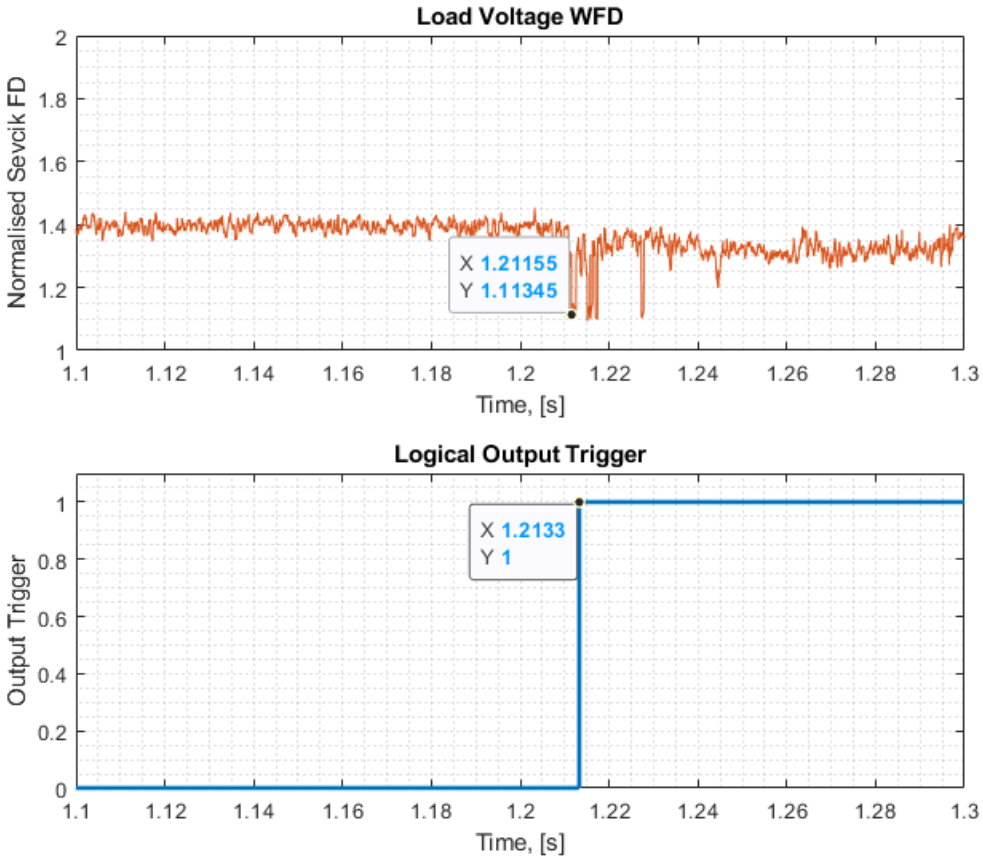


Figure 5.5: Application of WFD to Typical DC Series Arc Load Voltage Waveform - Forced Separation Ignition, Passive 41.7 Ω Load, Cropped to t = 1.1s and t = 1.3s

phase starts and the WFD output value regularly dips to a value of 1.26 from the load voltage WFD, producing a regular 10% change in fractal dimension significant enough to trigger arc detection throughout the arc burning phase. This behaviour does not repeat in the series current WFD in in Figure. 5.4 which does not show the same magnitude step-change in fractal dimension post-ignition, and would not therefore produce an output trigger if the initial transient was missed. As the distance between the arcing electrodes does not change in forced failure arcs, being maintained at 20mm post-ignition, the WFD value remains fairly constant post-ignition for both traces, after the initial step-change, and does not steadily increase as seen in the load voltage WFD, forced separation arc in Figure. 5.1. This is because at a fixed electrode separation the arc impedance remains fairly

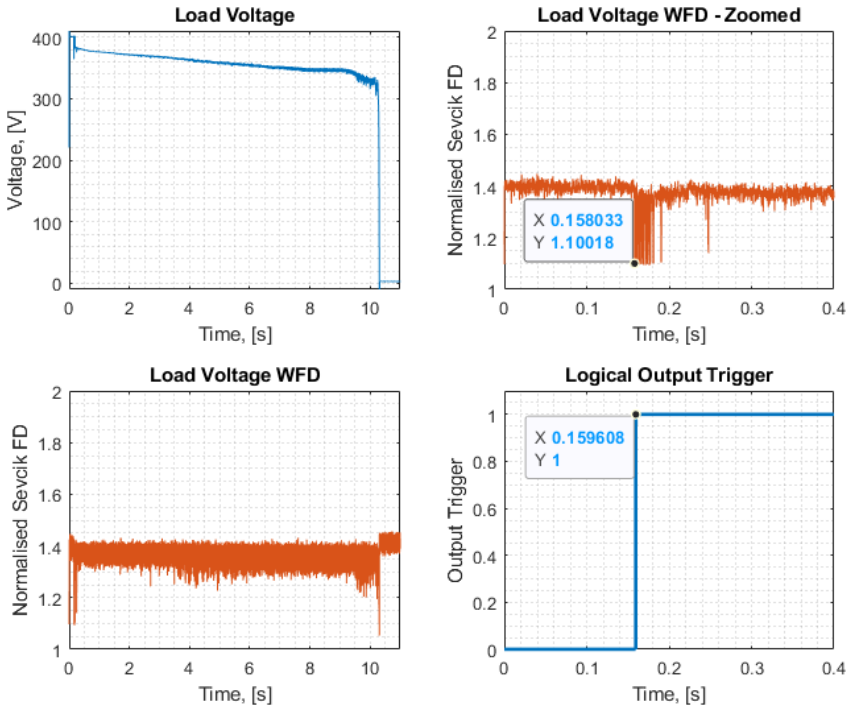


Figure 5.6: WFD Output and Trigger Highlighting 1.6 ms Arc Detection Time for Typical DC Series Arc Load Voltage Waveform - Forced Separation Ignition, Passive 41.7 Ω Load

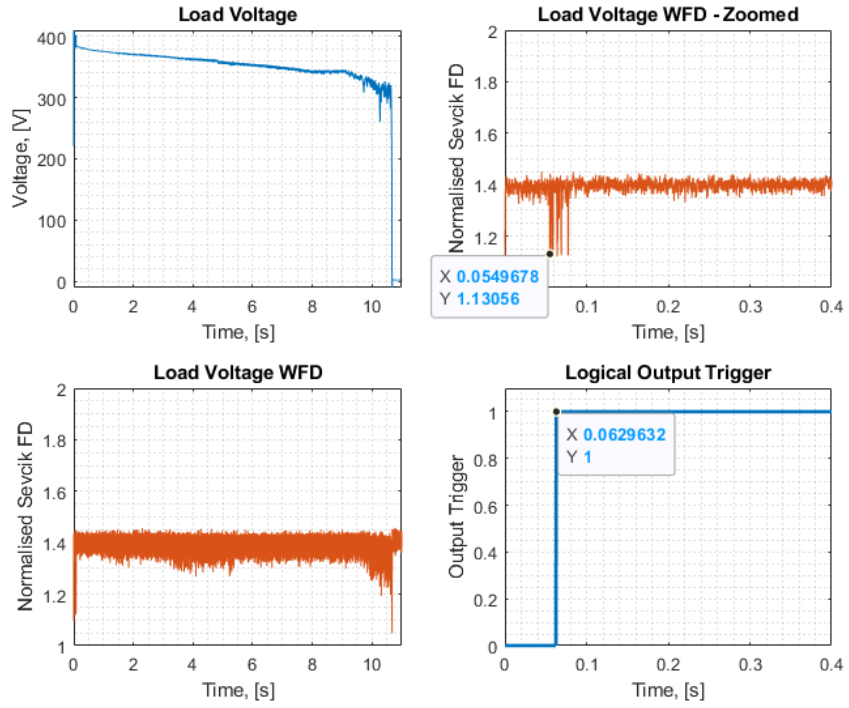


Figure 5.7: WFD Output and Trigger Highlighting 8.1 ms Arc Detection Time for Typical DC Series Arc Load Voltage Waveform - Forced Separation Ignition, Passive 41.7 Ω Load

consistent, as can be seen in Figure. 3.10, indicating a near constant 8.8 Ω impedance following arc ignition. A constant arc impedance means that the relative magnitude of the arc noise superimposed on the circuit waveforms goes unchanged, providing an explanation for the near constant change in fractal dimension seen in when utilising forced failure arc ignition. For the forced failure arc trace shown in Figs. 3.9 and 5.2 the arc was detected 2.07 ms following arc ignition, producing an output trigger at this time, as shown in the zoomed trace in Figure. 5.8. In all 10 repeats, the WFD algorithm successfully identified the arc within 7 ms of arc ignition, producing an average change in load voltage WFD of 21.97% at the point of arc ignition as highlighted in Table. 5.1, and an average change in series current WFD of 18.44% as highlighted in Table. 5.2. Each test displayed similar behaviours, with a clear step-change in fractal dimension at arc ignition that remained consistent whilst the arc was burning.

Across all tests, the forced failure arc produced a greater change in fractal dimension than the forced separation arcs at the point of arc ignition. This is likely due to the increased electrode separation and arc impedance of the forced failure arc at ignition. In Figure. 3.10 it can be seen that the forced failure arc has an impedance of 8.8 Ω following arc ignition, greater than the 3.5 Ω seen shortly after ignition in the forced separation arc. The larger arc impedance would have a greater influence over the circuit load voltage waveform versus the smaller impedance, and would therefore cause superimposed fractal arc noise to have a greater magnitude, resulting in the increased fractal dimension measurement. Another possible reason for the greater change in fractal dimension at ignition, is that the forced failure ignition is inherently more dramatic than the forced separation arc. The deliberate destruction of an underrated component and the subsequent arc

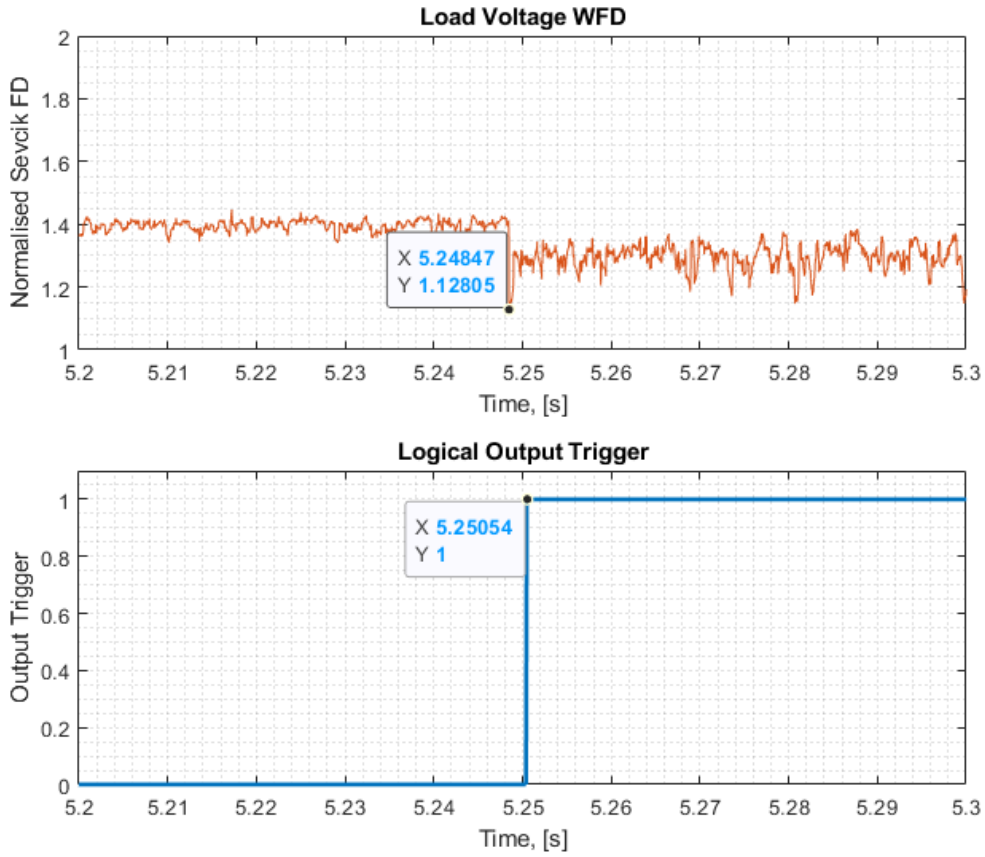


Figure 5.8: Application of WFD Typical DC Series Arc Load Voltage Waveforms - Forced Failure Ignition, Passive 41.7Ω Load, Cropped to t = 5.2s and t = 5.3s

formation over the full 20 mm gap between the electrodes results in a larger initial arc flash that is also reflected in the circuit impedance (as can be seen in Figure. 3.10). Comparatively, the formation of the forced separation arcs produce a smaller initial transient due to the reduced arc length and impedance at ignition.

Conclusions for Tests with a Passive Load

Results presented have indicated that the WFD arc detection scheme is capable of detecting DC series arc failures from simple power networks with passive loads using the circuit described in Figure. 3.3. For the load voltage WFD traces, an average change in fractal dimension of the 21.97%

was observed across the 10 forced failure ignition arcs, with a comparative 18.97% change in FD seen in the 18 forced separation ignition arcs, both greater than the required 10% detection threshold as highlighted in Table. 5.1. Similarly, an average change of 18.44% for forced failure arcs, and 11.87% for forced separation arcs was observed for the series current WFDs, as shown in Table. 5.2. The WFD algorithm successfully identified the arc failure in the 28 arc failures tested from both load voltage and series current waveforms, successfully producing an output trigger within several milliseconds of arc ignition. In all passive load cases, forced failure arcs provided a more reliable candidate for detection, displaying a larger initial change in FD, with a consistent change in FD displayed throughout the arcing period. Also observed across all 28 passive load tests was a reduced magnitude response from the series current WFD versus the load voltage WFD for across all points of the arc, for both arc ignition types. This suggests that load voltage measurements are more suitable for a practical arc detection implementation of the WFD technique, when compared to series current, as a larger response from the algorithm to the onset of an arc failure allows for faster detection whilst reducing the risk of missed detections.

5.2.2 WFD Application to Active & Switching Loads

As modern power networks have developed they have become more complex and have moved away from purely passive components to include additional active, switching and non-linear components. These new components and circuit behaviours, in addition to circuit load control and management, present a challenge for circuit protection, as they provide a

range of new conditions that may trigger a false-positive detection. Specific load behaviours, such as periodic step-load changes or loads with significant frequency content have been shown to frequently trigger false positive detection in other arc detection methods, and it is therefore necessary to test the efficacy of the WFD detection scheme under these conditions [36, 38, 57, 59].

In these tests the passive load, $R_{Passive}$ in Figure. 3.3 was left as an open circuit and the programmable load labelled as R_{Prog} was utilised to control the circuit load behaviour. As in earlier tests, V_{in} was fixed at 400 V DC. The ZSAC2826 programmable load used in these tests is capable of load resistance and current control through internal switching and control of field-effect transistors (FET), and as such introduces active circuit components in place of the existing passive components. Through programming of the ZSAC2826 the following test conditions were produced:

- Controlled Resistance Oscillation: The programmable load is set to oscillate at a user-defined frequency between resistances of 41.7 Ω and 57.1 Ω, drawing a series current of 9.55 A and 6.98 A from the 400 V DC supply when in series with the simulated cable impedance. The 41.7 Ω active load drawing 9.55 A was implemented to match the 41.7 Ω passive load tested previously and allow direct comparison. The 57.1 Ω, 6.98 A load provides a lower test current, but not substantially low enough of a sudden change in current to significantly reduce the power through the circuit, and by extension to the arc, maintaining the oscillatory test condition whilst avoiding premature arc collapse.

- Controlled Current Oscillation: The programmable load is set to oscillate at a user-defined frequency between fixed two user defined load

currents of by constantly adjusting the resistance of the FETs internal to the device.

The switching of both the controlled resistance and controlled current load types produces a square wave with a frequency defined by the user. In these experiments a range of switching frequencies from 1 - 5000 Hz were applied to simulate both step-load changes (< 1kHz low switching frequencies) and loads with significant frequency content (> 1kHz switching frequencies) that have been known to trigger false-positive detections for other arc fault detection methods [2, 4, 37, 117]. 12 arc fault data captures were conducted for each load type, and each arc fault ignition type (forced failure or forced separation), sweeping the 1 - 5000 Hz range, resulting in 48 total arc faults data captures across all conditions. In each test the system was energised and initial transients allowed to settle before the arc fault was introduced to the power network through forced separation or forced failure arc ignition. It its noteworthy that all test frequencies here were below the 25 kHz stopband of the digital lowpass filter applied by the WFD, and are therefore not filtered out before processing.

Active Load Test Condition #1: Controlled Resistance Oscillation

In total, twenty four arc fault data captures were produced using oscillating the resistance of the programmable load from 1 - 5 kHZ. In Figure. 5.9 and Figure. 5.10, the load voltage and series current waveforms are shown at the extremes of the tested oscillation frequency range (1 Hz and 5 kHz). For both Figs. 5.9 and 5.10 as the load switches, each rising edge the voltage changes at a rate of $\frac{\delta V}{\delta t} \approx 1120 V s^{-1}$ and the current at a rate of

$\frac{\delta I}{\delta t} \approx 1200 Is^{-1}$ (determined analytically through calculating the d/dt values from empirical data captured at each switching event using MatLab), similar to the transient currents and voltages for a small switched-mode power converter [118, 119, 120]. The arcs in these figures were formed through forced separation ignition and forced failure ignition respectively, with the 1 Hz oscillation simulating repeated step load changes, and the 5 kHZ oscillation superimposing significant frequency content to the waveform and at the limit of available load switching of the programmable load utilised in this work.

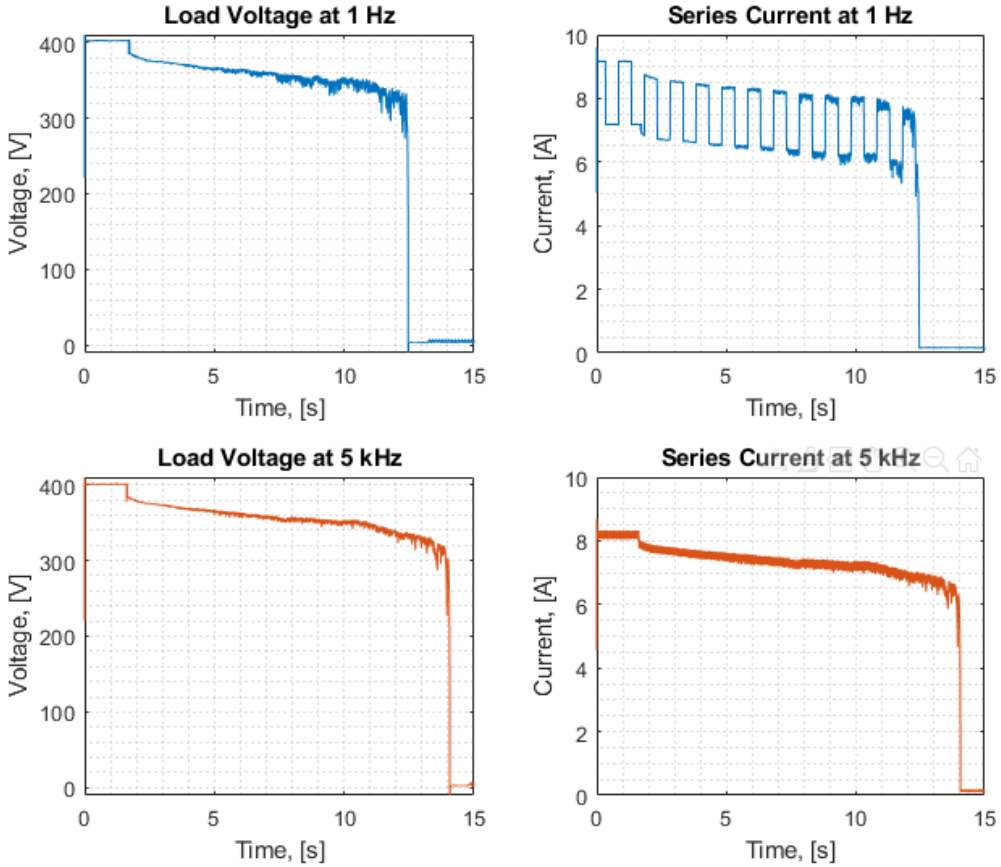


Figure 5.9: Typical DC Series Arc Waveforms For Active Circuit Load, Oscillating Resistance - Forced Separation Ignition - Switching At f = 1Hz and f = 5kHz

It can be seen in both Figure. 5.9 and Figure. 5.10 that the 1 Hz load oscillation produces a noticeable step change in the series current, with only

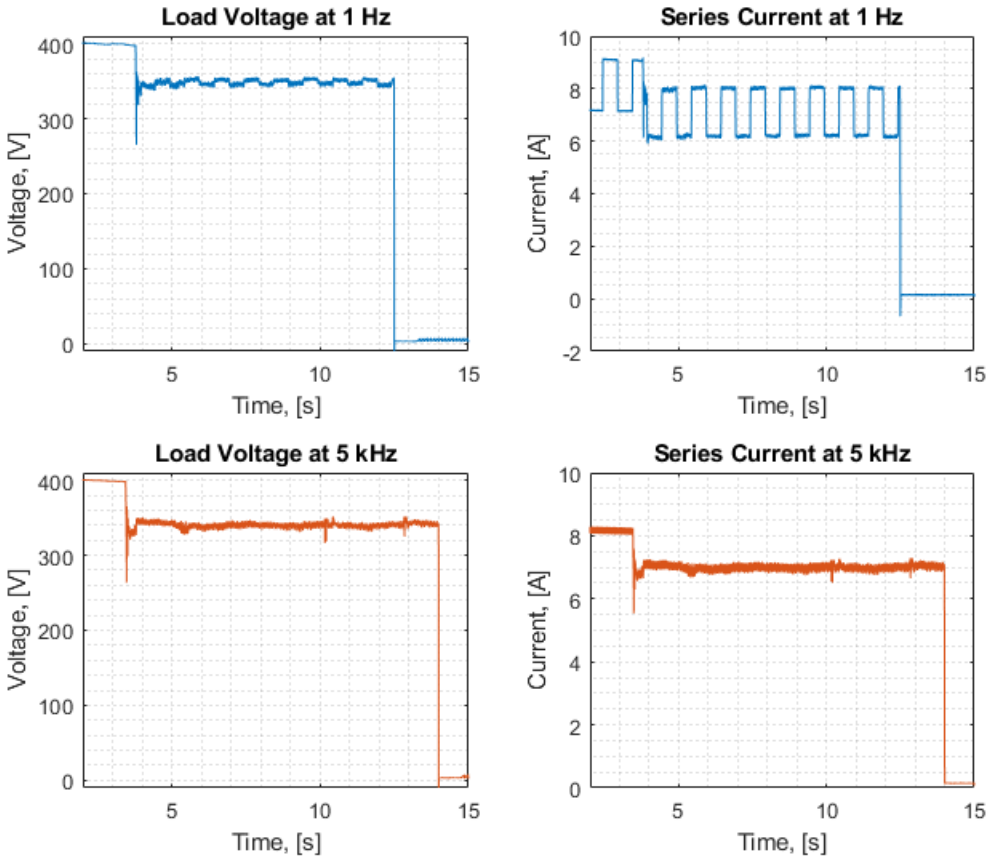


Figure 5.10: Typical DC Series Arc Waveforms For Active Circuit Load, Oscillating Resistance - Forced Failure Ignition - Switching At f = 1Hz and f = 5kHz

minor reflection on the circuit load voltage. The 1 Hz oscillation is more easily observed on the forced failure load voltage waveform in Figure. 5.10, than the forced separation arc in Figure. 5.9. This is likely due to the movement of the arc electrodes producing a constant change in arc length, and hence a change in arc impedance that reflects onto the load voltage waveform, obscuring any load oscillations whilst the electrodes are moving.

The 5 kHz oscillation is not directly visible at this scale, but still has a noticeable effect on the circuit current. In both Figure. 5.9 and Figure. 5.10 the series current waveforms for the 5 kHZ load oscillation are reduced to a magnitude of approximately 8.2 A pre-arc. This is due to the high fre-

quency current oscillations caused by a combination of the load changing being influenced by the inductance of the circuit line impedance resisting the rapid current change, and high-frequency switching making the waveform functionally AC and therefore making the reactance of the circuit non-negligible. In this case, the $5 \cdot \tau = 5 \cdot \frac{15.2 \times 10^3}{41.9} = 1.814\, ms$ rise time of the RL circuit formed through combination with the circuit line impedance and the load resistance is greater than 0.2 ms (the switching period of the load). This means that with each oscillation the current does not have enough time to reach the peak current of 9.55 A, or the minimum current of 6.98 A before the load switches again. The current therefore sits between these two values, at the effectively averaged current of 8.2 A.

The load voltage and series current waveforms for all 24 tested arc failures were then processed using the WFD arc detection scheme. For the load voltage waveforms, Table. 5.3 records key metrics from this testing, and separately Figures. 5.11, 5.12, 5.13 and 5.14 show the application of the WFD algorithm to the load voltage waveform in Figure. 5.9 and Figure. 5.10 for both the 1 Hz and 5 kHz oscillations under both forced separation and forced failure arc ignition. Additionally, Figures. 5.15 and 5.16 show the application of the WFD to series current waveforms for the 1 Hz and 5 kHz switching loads with a forced separation arc ignition, with Figures. 5.17 and 5.18 also showing application to the forced failure arcs, with Table.5.4 recording the key metrics.

Table 5.3: Table of Active Load Condition WFD Output Results - Load Voltage WFD - Controlled Resistance Load

Ignition Type	**Mean Pre-Arc WFD Value**	**Mean Arc Ignition WFD Value**	**Mean Change in WFD [%]**	**Repeats**	**Success Rate [%]**
Forced-Failure	1.41	1.112	19.69	12	100
Forced-Separation	1.40	1.168	17.13	12	100

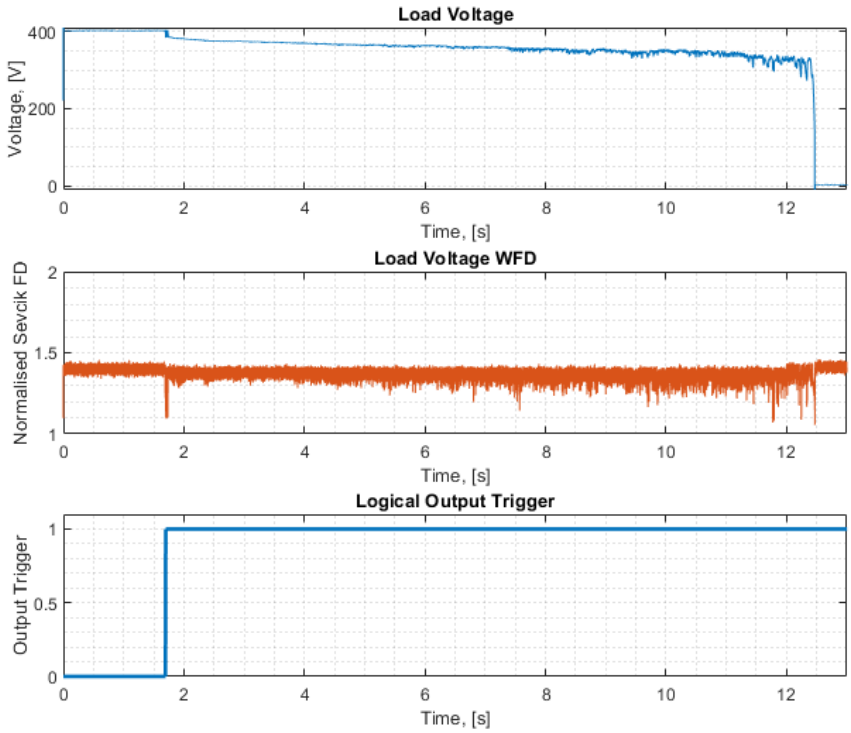


Figure 5.11: Application of WFD to Typical DC Series Arc Load Voltage Waveform with an Active Circuit Load, Forced Separation Ignition, Controlled Resistance Load Switching at f = 1 Hz

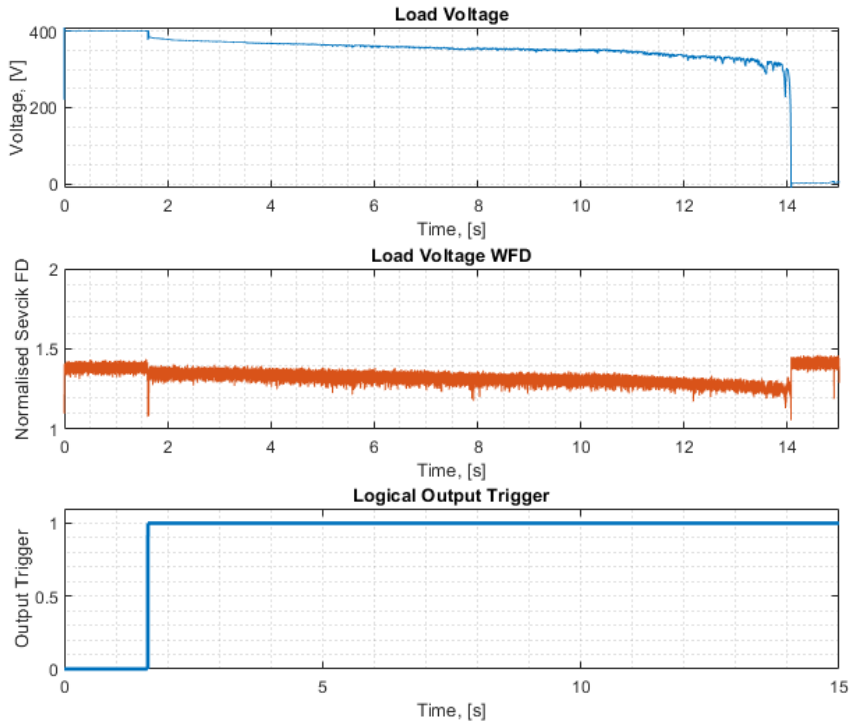


Figure 5.12: Application of WFD to Typical DC Series Arc Load Voltage Waveform with an Active Circuit Load, Forced Separation Ignition, Controlled Resistance Load Switching at f = 5 kHz

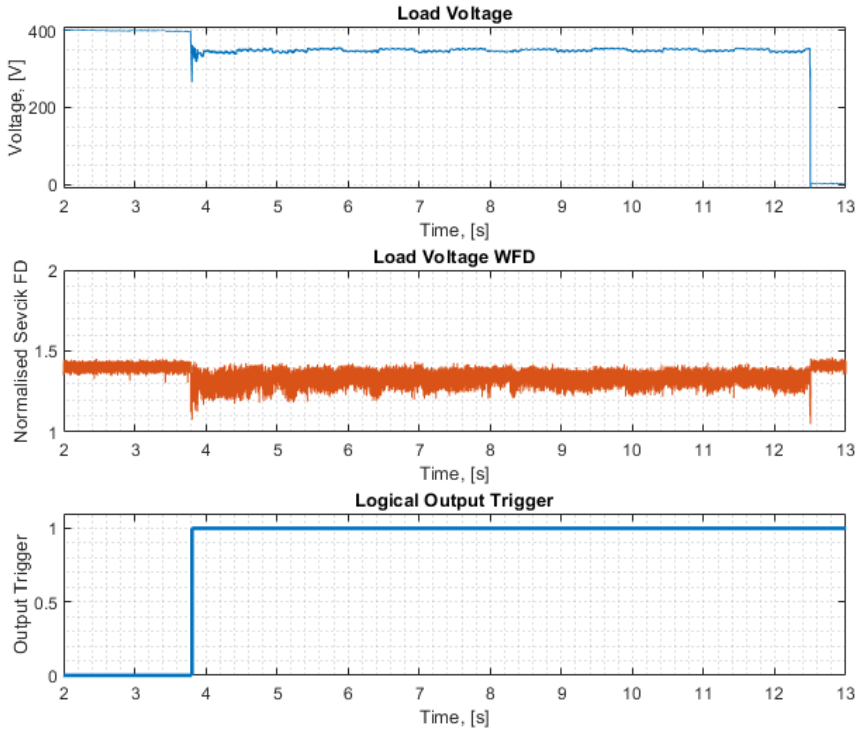


Figure 5.13: Application of WFD to Typical DC Series Arc Load Voltage Waveform with an Active Circuit Load, Forced Failure Ignition, Controlled Resistance Load Switching at f = 1 Hz

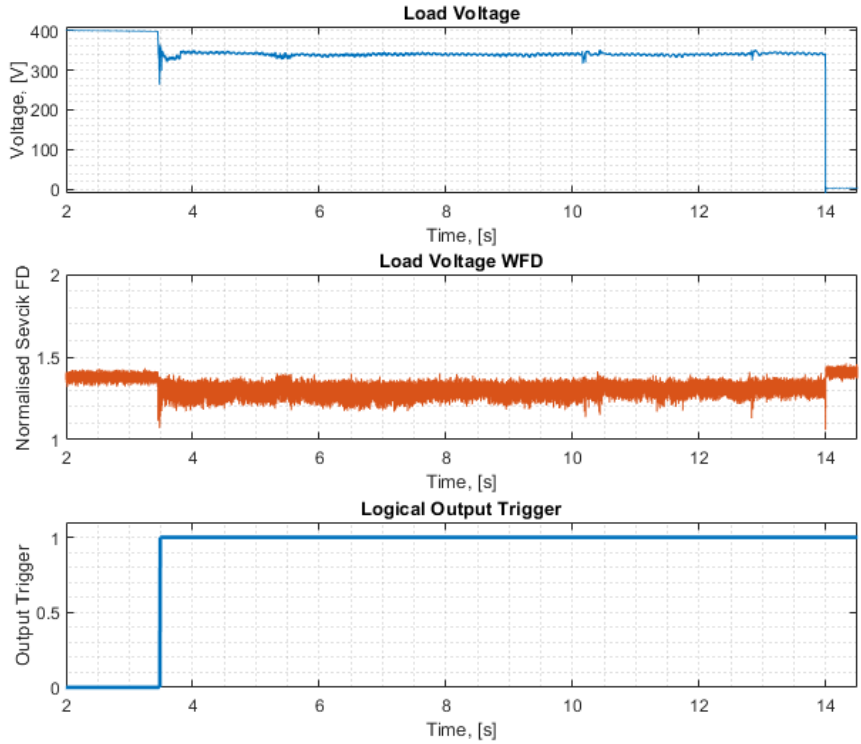


Figure 5.14: Application of WFD to Typical DC Series Arc Load Voltage Waveform with an Active Circuit Load, Forced Failure Ignition, Controlled Resistance Load Switching at f = 5 kHz

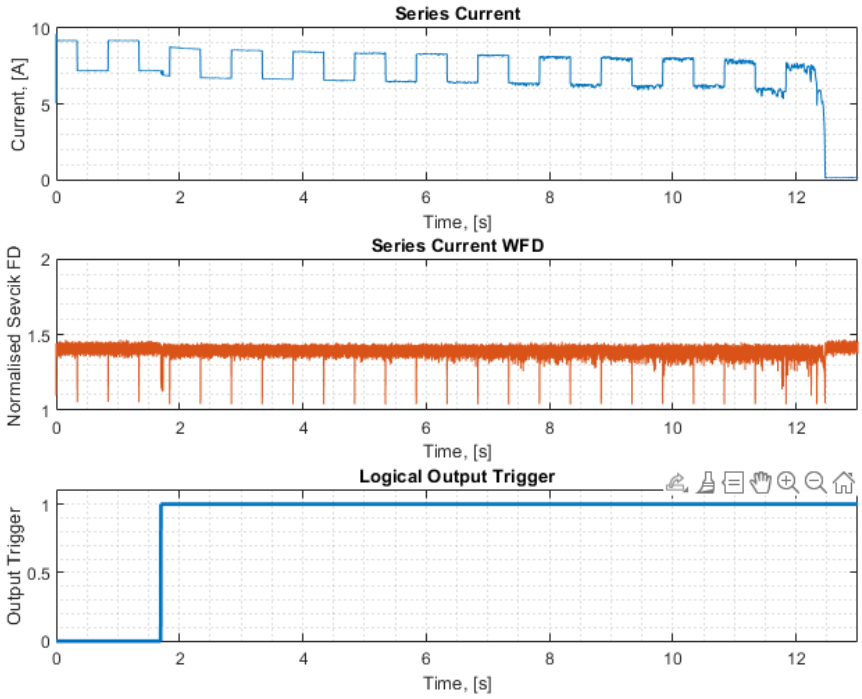


Figure 5.15: Application of WFD to Typical DC Series Arc Series Current Waveform with an Active Circuit Load, Forced Separation Ignition, Controlled Resistance Load Switching at f = 1 Hz

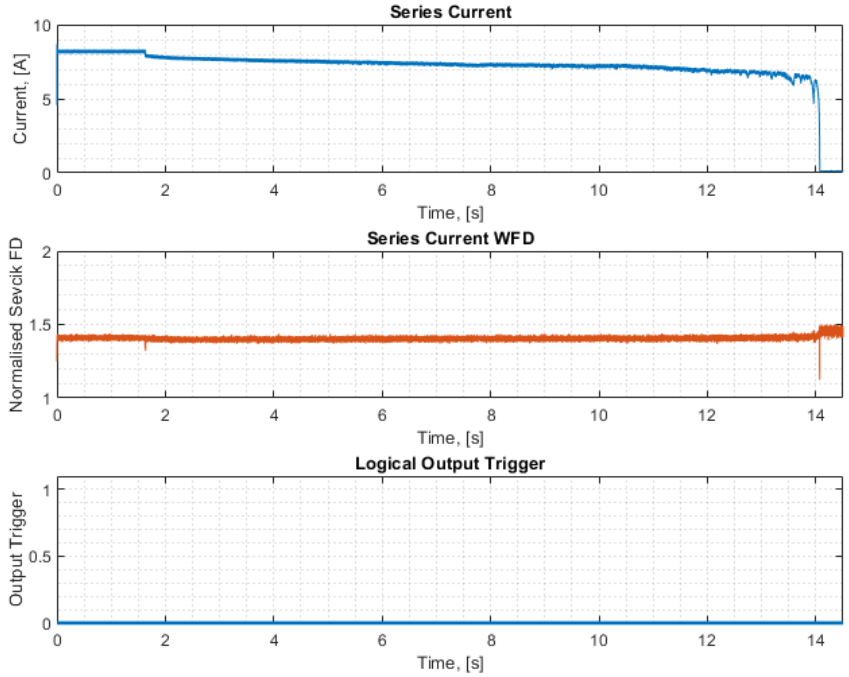


Figure 5.16: Application of WFD to Typical DC Series Arc Series Current Waveform with an Active Circuit Load, Forced Separation Ignition, Controlled Resistance Load Switching at f = 5 kHz

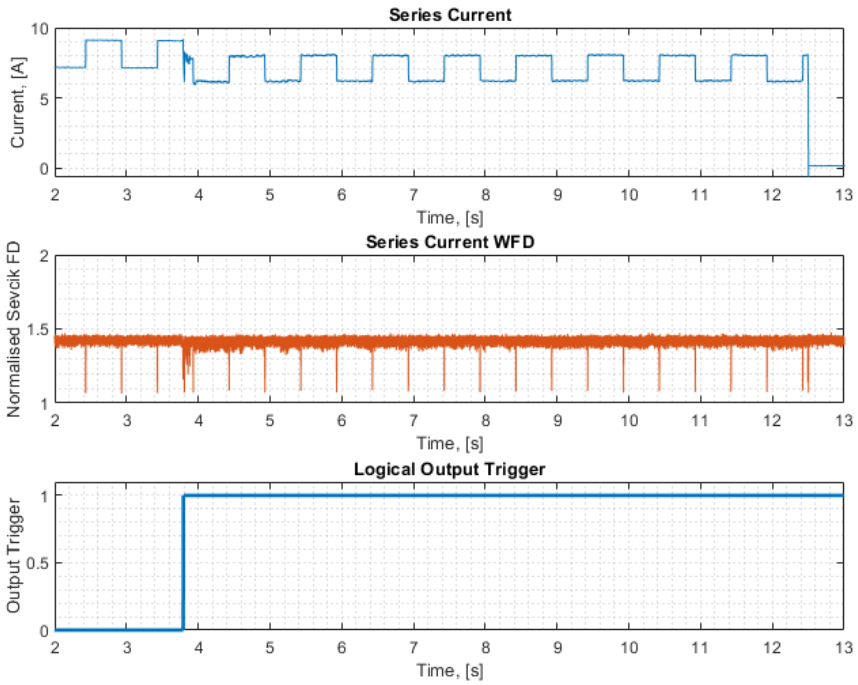


Figure 5.17: Application of WFD to Typical DC Series Arc Series Current Waveform with an Active Circuit Load, Forced Failure Ignition, Controlled Resistance Load Switching at f = 1 Hz

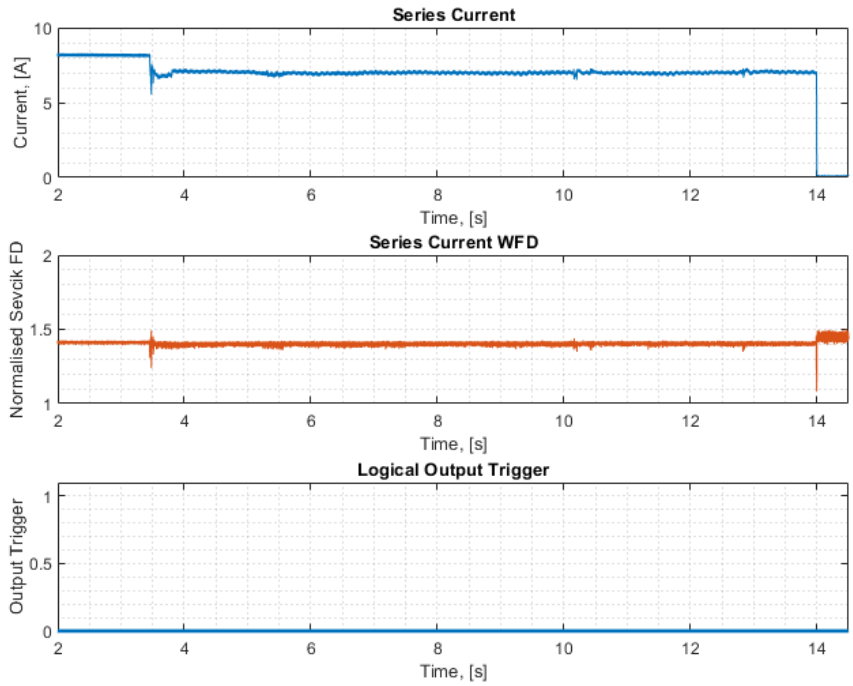


Figure 5.18: Application of WFD to Typical DC Series Arc Series Current Waveform with an Active Circuit Load, Forced Failure Ignition, Controlled Resistance Load Switching at f = 5 kHz

Table 5.4: Table of Active Load Condition WFD Output Results - Series Current WFD - Controlled Resistance Load

Ignition Type	**Mean Pre-Arc WFD Value**	**Mean Arc Ignition WFD Value**	**Mean Change in WFD [%]**	**Repeats**	**Success Rate [%]**
Forced-Failure	1.41	1.22	13.48	12	83.33
Forced-Separation	1.41	1.26	10.63	12	66.67

It can be seen for the load voltage WFD traces in Figs. 5.11 - 5.14 that the WFD technique successfully identifies the at the point of arc ignition in the presence of both the 1 Hz and 5 kHz load oscillations. The load step-changes introduced by the 1 Hz load switching behaviour are seen to have no effect on the WFD output in Figs. 5.11 and 5.13. The load voltage WFD value remains consistent for both forced failure and forced separation ignition types, appearing to be unaffected by the oscillating load. This in turn, demonstrates a robustness to step-load change behaviour that regularly causes false-positive detections within other methods documented in the literature [2, 22, 36]. Additionally, showing no response to the switching transients indicates that the larger spikes in WFD seen at arc ignition, collapse and occasionally during arc burning, are not responses to the sudden change in voltage caused by introduction of the arc impedance to the circuit. This adds an additional level of confidence in the use of the initial WFD transient spike at arc ignition for detection, indicating it is not the product of transient behaviour in the input load voltage waveform, but instead the fractal behaviour associated with the initial "arc flash" at ignition.

The additional frequency content imposed by the 5 kHz load in Figs. 5.12 and 5.14 can be seen to have a very subtle effect on the load voltage WFD output. Whilst the arc can still be detected from the initial WFD spike and subsequent step-change at ignition, the peak-to-peak value of the WFD and the frequency of WFD "spikes" is reduced. This is most obvious in the forced separation arc in Figure. 5.12 between t = 12 s and t = 14.1 s. Here the additional transient behaviour seen on the load waveform as the arc nears collapse is not reflected onto the load voltage WFD output trace, in contrast to that seen in other forced separation arcs, such as the passive load results in Figure. 5.1. This suppression of the transient is not

observed in any of the results for the forced separation arcs, and suggests that the reduced transient behaviour and peak-peak value of the WFD are the results of an interaction between the load switching behaviour and the constant movement of the arc electrodes, though more experimental work is required to confirm this. Irrespective of the reduced transient features, it can be seen in both Figs. 5.12 and 5.14 that the WFD algorithm is capable of detecting the arc, despite the increased frequency content.

For the series current WFD waveforms in Figs. 5.15 - 5.18 it can be seen that the addition of load switching behaviour and higher frequency content has adversely impacted the WFD output. In Figs. 5.15 and 5.17 the lower frequency 1 Hz load switching is reflected in the WFD output as a momentary increase in fractal dimension at each rising and falling edge of the current square wave. The specific pseudo-fractal behaviour that causes the increase in fractal dimension with step changes in load is discussed in full later in the chapter, in Section 5.2.3. Regardless, the transient change in fractal dimension with the changing load is undesirable, as it increases the risk of false-positive detections should the momentary changes in WFD output be mistaken for an arc. This is because the transient changes with each load step change are too short in time to trigger a detection from the WFDs threshold based detection scheme, however there is still the risk of false positive detection with longer transient changes. In all tests performed, the series current WFD produced no false positive detections from these periodic output spikes, detecting the arc in each case from the transient at arc ignition, producing a change of 19.15% from 1.41 to 1.14 in Figure. 5.15 and a change of 16.31% in Figs. 5.17 from 1.41 to 1.18 for the lower frequency load step changes. When considering the higher frequency 5 kHz load content in Figs. 5.16 and 5.18 it can be seen that the addi-

tional frequency content has had a significant influence on WFD output in both the forced separation and forced failure arcs. For both Figure. 5.16 and Figure.5.18 it can be seen that the transient spike at arc ignition has been heavily attenuated versus the lower frequency load oscillation traces in Figs. 5.15 and 5.17 for both arc ignition types, resulting in missed detections in each case. As reflected in Table. 5.4, the series current trace produced two missed detections for the false failure arcs (both at 5 kHz) and four missed detections for the forced separation arcs (two at 1 kHz and two at 5 kHz). As previously discussed, when switching at higher frequencies the $5 \cdot \tau = 1.814\,ms$ rise time of the circuit is less than the switching period of the load. This results in the circuit switching before the series current can reach its new steady state value before switching again. The reduction in series current WFD response at higher switching frequencies may be due to this interaction with the RL nature of the circuit, where fractal arc noise that would be picked up in steady state is distorted through interaction with the current switching. Alternatively, the circuit inductance, coupled with unknown input impedance to the programmable load may form a RL lowpass filter, potentially filtering out arc transient effects that would normally be picked up by the WFD.

For all of the active load results, similar trends were observed to those found in the passive load tests when comparing between the different arc ignition types. It is shown in Figures. 5.11, 5.12, 5.13 and 5.14 for load voltage WFDs, Figures. 5.15, 5.16, 5.17 and 5.18 for series current WFDs, and separately in Tables. 5.3 and 5.4 that in each case the arcs formed through forced failure ignition produced a larger change in WFD at arc ignition versus the forced separation arcs as previously seen in the passive load results. Similarly, the forced separation arc, load voltage WFD results in

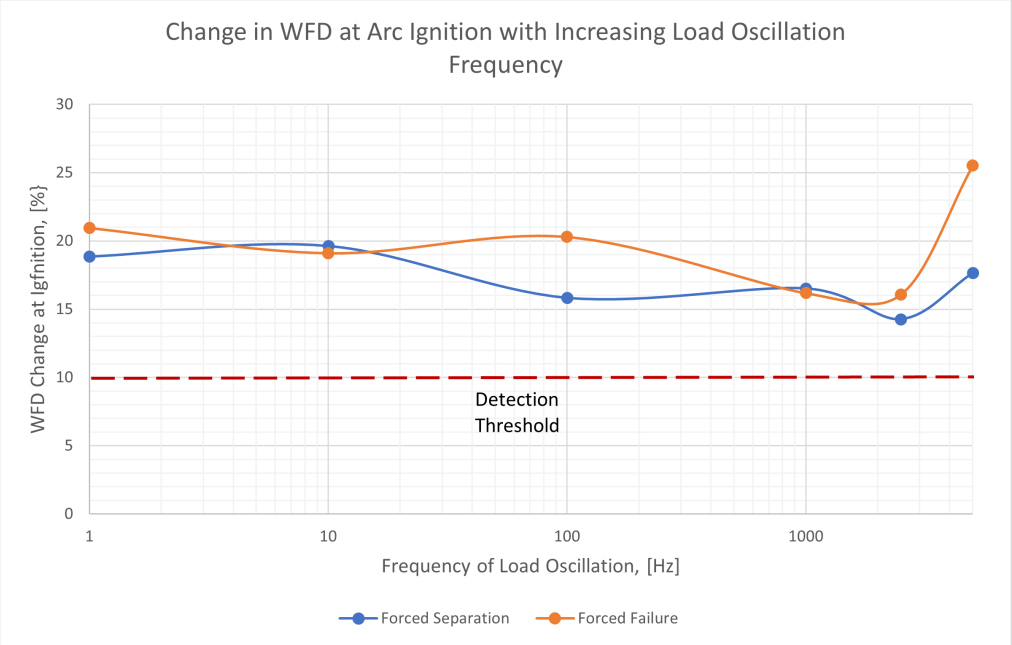


Figure 5.19: Change in Windowed Fractal Dimension with Increasing Load Oscillation Frequency for a Periodically Oscillating Controlled Resistance Load

Figs. 5.11 and 5.12 show an increased change in fractal dimension with increasing arc duration previously observed in Figure. 5.1 for the passive load arc failures. Consistency between the active and passive load results reinforces the previous suggestion that an increased arc length and impedance produces a stronger response from the WFD algorithm, indicating that the efficacy of the algorithm would increase with larger, more violent arc faults.

Similar results to those shown in Figures. 5.11 - 5.14 were seen across all different controlled resistance load oscillation frequencies, with a change in WFD significant enough for arc detection produced at each frequency tested. This is highlighted in Figure. 5.19 where the average WFD change at each frequency is plotted versus load oscillation frequency on a semi-log scale.

It can be seen in Figure. 5.19 that whilst the WFD produces a detectable response across all tested frequencies, there is a reduction of 5% in WFD output change at ignition as load oscillation increases to 2.5 kHz. The WFD response begins to increase again at the 5 kHZ switching frequency, and suggests that there is a specific loss of output as load frequencies approach 2.5 kHz. Whilst additional repeat testing is necessary to clarify this behaviour, the reduction in WFD change seen between 100 and 2500 Hz may be due to the switching behaviour having a similar time-period to the length of the windowing function used to process the WFD. At 2.5 kHz, the load oscillation has a switching period of 0.4 ms, comparable to the 0.5 ms between signal windows, N_{win}. At these frequencies, the load switching behaviour will occur 2-3 times per signal window and may impact the calculation of fractal dimension in that signal window by skewing the calculation of euclidean length in (4.7). This also would explain why at higher load switching frequencies this behaviour stops. As load switching frequency increases, the load switching period reduces such that it is much smaller than the windowing function length, and as such each signal window will capture more load switching events. Because the load switching is periodic, its influence on the WFD input signal is both positive and negative in magnitude, occurring repeatedly, and will average out in the euclidean length calculation when occurring multiple times in a signal window. As such, this suggests that load oscillation frequency becomes less influential on the WFD output as frequency increases further, however multiple additional tests at a broader range of test frequencies are required to confirm this.

Shown in Figures. 5.20 and 5.21 are comparisons of the active controlled resistance load (switching at 1 Hz) WFD outputs in Figs. 5.11 and 5.13 to the passive results in Figs. 5.1 and 5.2, for both load voltage and series

current. When considering the load voltage WFD traces in Figure. 5.20 similar results can be seen for both passive and active loads and both arc ignition types. All traces display a distinct step change in fractal dimension at arc ignition and collapse. The forced separation arcs shown for both the passive and active loads show the same increasing change in WFD as the arc duration (and length) increases. Similarly, both the forced failure arcs retain an almost constant change in WFD after the initial transient has passed, irrespective of load type. The similarity in load voltage WFD traces is contrasted however, by the differences seen between load types for the series current WFD traces in Figure. 5.21. Here, all four WFD traces show a reduced response and smaller change in WFD at all points in the trace when compared to the load voltage traces in Figure. 5.20. It can also be observed that the current WFD's produce a momentary transient change at 2 times the load oscillation frequency. This spike occurs at every rising and falling edge of the current waveform as the load resistance increases and decreases periodically. The change in WFD at these points is the result of the WFD algorithm responding to the pseudo-fractal behaviour of under-damped sinusoids formed as the circuit inductance resists the sudden change in current. This specific behaviour and methods to correct for it are discussed fully later in this thesis in Section 5.2.3, however it is clear that the addition of these transient spikes produce a less desirable response in the WFD output that could trigger false detections, suggesting that the load voltage WFD is better for use as arc discriminating behaviour. Furthermore, the four series current WFD traces all show very little change in WFD after arc ignition and throughout the arc burning phase, when compared to the load voltage WFD traces in Figure. 5.20. As such, a detection method utilising the current WFD values would leave the power network vulnerable to arc failure if the initial transient response at arc ignition was missed, whereas the continued step-change in WFD of the

load voltage WFD traces can still indicate a fault, further suggesting that load voltage WFD is more suitable for arc detection in this case.

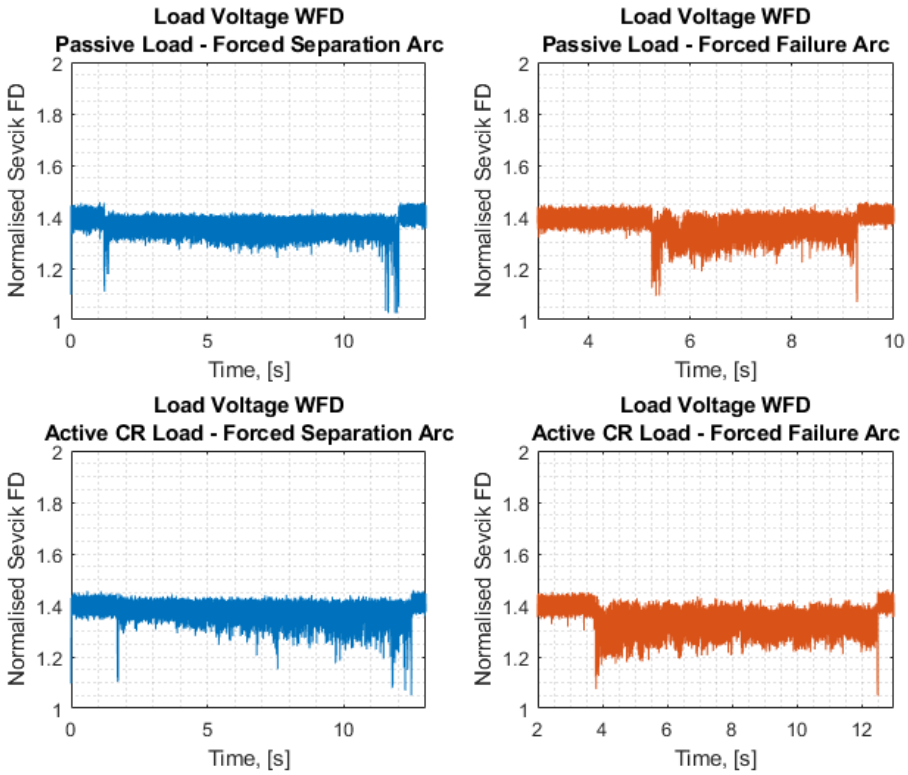


Figure 5.20: Comparison of Load Voltage WFD for Active Controlled Resistance Loads and Passive Loads

In Figures. 5.22 and 5.23 the four different arc fault traces shown previously in Figures. 5.20 and 5.21 are cropped to highlight the response of the WFD detection scheme to each arc ignition and load type before the arc begins. Only a very small change between passive and active loads for the eight waveforms can be seen, with a resting pre-arc WFD value of 1.4 in all passive load results changing to a value of 1.41 pre-arc in the active load results. This slight change in initial value is likely the result of the slight change in circuit topology, with the switch to the active load. It is likely that the resting fractal dimension will change further as circuit load topology becomes more complex with the addition of power converters or other non-linear components. All eight waveforms also show equivalent peak-

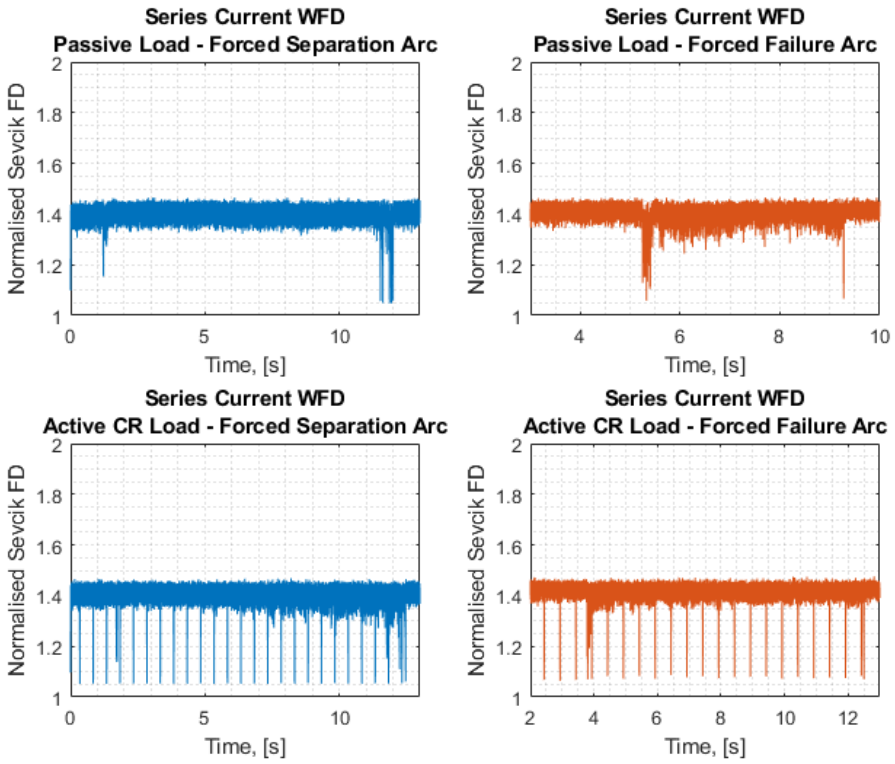


Figure 5.21: Comparison of Series Current WFD for Active Controlled Resistance Loads and Passive Loads

peak value for WFD output prior to arc ignition. The similarity observed between the WFD responses for the different loads and arc ignition types is beneficial for further development of the WFD detection method, as it suggests that changes observed in the WFD are either the direct results of arc behaviour, or circuit responses to that behaviour, rather than changes in the topology of the test circuit itself.

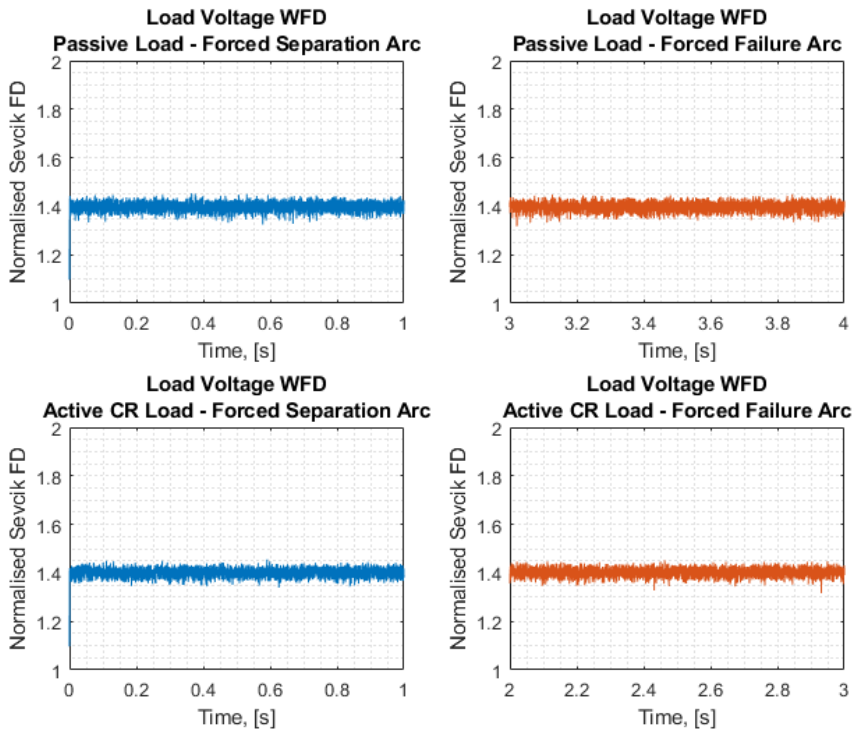


Figure 5.22: Comparison of Load Voltage WFD for Active Controlled Resistance Loads and Passive Loads - Cropped to show Pre-Arc Behaviour

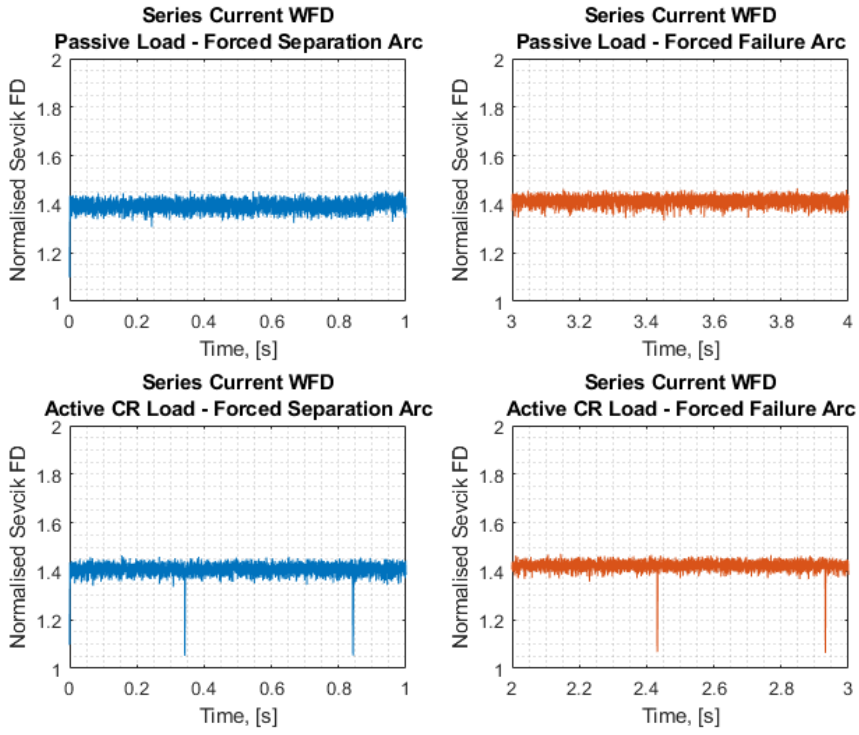


Figure 5.23: Comparison of Series Current WFD for Active Controlled Resistance Loads and Passive Loads - Cropped to show Pre-Arc Behaviour

Conclusions for Tests with Controlled Resistance Oscillating Load

Results of the controlled resistance oscillation testing have indicated that the WFD algorithm when applied to load voltage measurements is robust in the presence of active loads, to step-changes in load resistance, and has demonstrated a resilience to input signals with additional frequency content, showing no loss of load voltage WFD output or missed detections in these conditions. The WFD detection scheme identified the from the load voltage WFD output arc at arc ignition in all 24 waveforms tested, with forced failure arc showing on average a 2.56% greater changes in the magnitude of the WFD when compared to the forced separation arc ignition. Collectively, results indicate that the load voltage WFD algorithm is suitable for use on active, switching resistive loads, and may show increased efficacy with larger, or higher power arc faults where the introduced arc impedance has a greater effect on the behaviour of the circuit voltage waveforms. Application of the WFD method to series current waveforms resulted in 6 total missed detections from the 24 test cases, all at frequencies greater than 1 kHz. Additionally, series current WFD outputs produced on average a 6.21% smaller response at arc ignition for forced failure arcs when compared to the load voltage WFD, and a 6.5% smaller magnitude response for forced separation arcs.

When collectively considering the passive load results in Section 5.2.1 and the active load results presented in Section 5.2.2, it can be observed that the series current waveform consistently under-performs in comparison to the load voltage WFD. In both sets of results the series current WFD produces a reduced magnitude response to arc ignition compared to the load voltage WFD, showing on average a 3.53% reduction in output WFD change at arc

ignition for passive forced failure arcs, and a 7.16% reduction for passive forced separation arcs. This is mirrored by a 6.21% smaller response at arc ignition for active forced failure arcs, and a 6.5% smaller magnitude response for forced separation arcs, all when compared to the load voltage WFD of the same experiment. Furthermore, for the active load results in Section 5.2.2, the series current WFD has been observed to perform poorly in the presence of high frequency load switching, showing a large attenuation in WFD response across all of the arc, where the load voltage WFD remained unaffected. Here the series current WFD resulted in six missed detections that were accurately captured by the load voltage WFD. For these reasons, the series current WFD in its present form is insufficient for reliable arc detection across changing load conditions, and will not be considered further in this work. However, a discussion of the means to improve the series current WFD for practical application is included in Chapter. 7. Instead, remaining work will focus on application of the WFD method to load voltage waveforms for DC series arc detection.

Active Load Test Condition #2: Controlled Current Oscillation

In a similar manner to Section 5.2.2, work in this section aims to determine the efficacy of the WFD algorithm when applied to active circuit loads, containing both step-load changes and those with significant frequency content. In these experiments the programmable load, R_{Prog}, in Figure. 3.3, was set to operate as a controlled current load, oscillating at a range of user-defined frequencies, equivalent to those used in earlier controlled resistance oscillations. All other circuit parameters remain as described in from Section. 5.2.1. A total of 24 experimental arc failures were produced using this setup with the following experimental parameters:

- 12 experimental data captures using forced failure arc ignition with controlled load current fixed to oscillate between 8 A and 6 A, at frequencies ranging from 1 - 5000 Hz.

- 12 experimental data captures using forced separation arc ignition with controlled load current fixed to oscillate between 7 A and 5 A, at frequencies ranging from 10 - 1000 kHz.

The upper limit for controlled current oscillation was fixed at 8 A to ensure the programmable load did not exceeded its rated power in controlled current mode (3300 W), with the lower limit of 5 A selected to ensure that the arc would not collapse prematurely at increased arc lengths due to an insufficient supply of current. The fixed values chosen for current oscillation were chosen to be similar to those for the controlled resistance oscillation shown earlier to allow for ease of comparison, and to replicate the kind of current draw that might be expected from a tapped 400V DC bus in more-electric vehicle applications. In Figures. 5.24 and 5.25, the initial data captures for both the forced failure and forced separation arc ignition can be seen.

In both figures the effect of the current switching can be clearly observed on both the 1 Hz and 10 Hz waveform, producing periodic spikes and dips in the series current waveform on the rising and falling edges of the square wave. This is highlighted further in Figs. 5.26 and 5.27 where the 10 Hz and 5 kHz load voltage and series current waveforms shown in Figure. 5.24 are cropped to show only a handful of oscillations before arc ignition. The current transient spikes are only seen in the lower frequency waveforms, where the step changes in current produces a transient response as a result of the interaction between the circuit line inductance and the programmable load

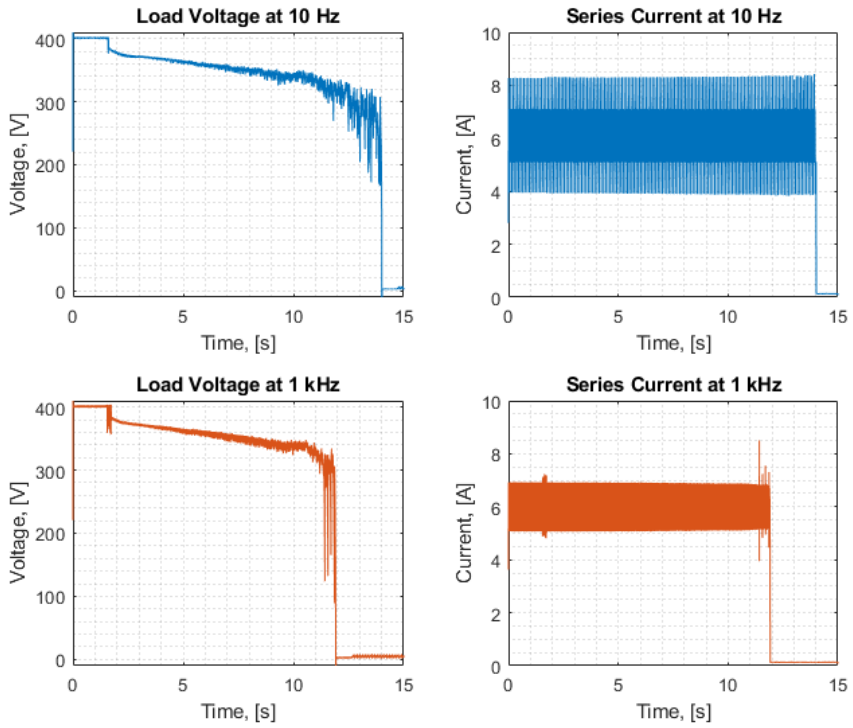


Figure 5.24: Typical DC Series Arc Waveforms For Active Circuit Load, Oscillating Current - Forced Separation Ignition - Switching At f = 10Hz and f = 1kHz

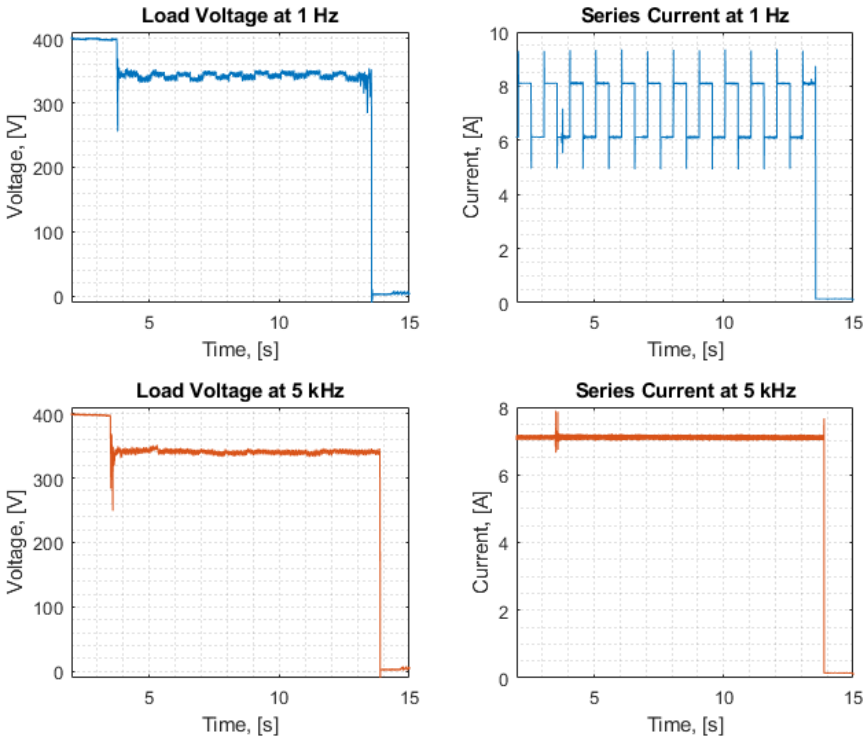


Figure 5.25: Typical DC Series Arc Waveforms For Active Circuit Load, Oscillating Current - Forced Failure Ignition - Switching At f = 1Hz and f = 5kHz

resistance. As the current step change occurs, the rate of current change increases and causes the line inductance to produce a reverse-voltage to resist the change. The programmable load then adjusts for this behaviour and overshoots, resulting in the initial current spike. Following this, the programmable load works to return the current to the programmed 7 A by producing a negative rate of change of current, and the process repeats until steady state is reached. This can be seen as a "ringing" in the current waveform appearing as an under-damped sinusoid between t = 0.5 s and t= 0.51 s in Figure. 5.27 and repeating on every rising and falling edge. This behaviour is additionally reflected onto the circuit load voltage in Figure. 5.26 that will be input to the WFD detection method, and is typical of that seen when switching on a transmission line and provides a useful test condition to determine the efficacy of the WFD algorithm against real-world conditions [121, 122].

Also observed in Figs 5.24, 5.25, 5.26 and Figure. 5.27 is the lack of transient spiking in the 1 kHz and 5 kHz waveforms. Here, the series current waveforms appears as a sinusoidal AC waveform with a fixed DC offset. At these higher switching frequencies, the programmable load cannot control the circuit current to return to steady before the current switches again. Instead, the $5\tau = 1.52\,ms$ charging time of the RL circuit formed with the inductor dominates, reducing the square wave to an AC sinusoid that retains the same switching frequency. This also results in the reduction of peak-peak current seen at 5 kHz in Figure. 5.25 when compared to the 1 kHz switching in Figure. 5.24, as the faster 5 kHz switching leaves even less time for the circuit current to rise/fall, resulting in a sinusoidal waveform that rests at the average value between the maximum and minimum switched current values, with reduced peak-peak magnitude. The reduction

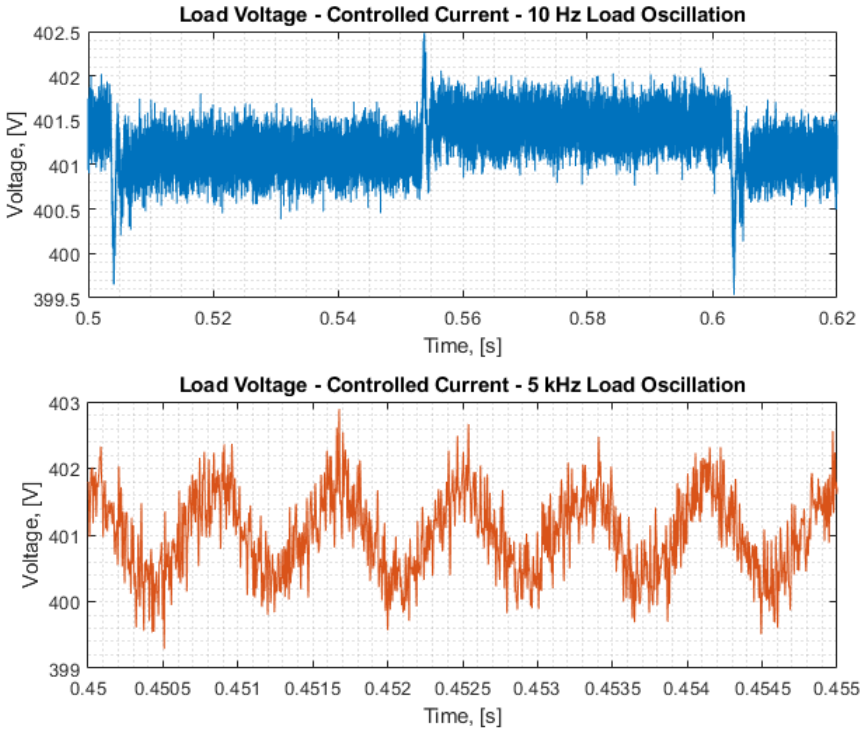


Figure 5.26: Load Voltage Waveforms Typical DC Series Arc Waveforms For Active Circuit Load, Oscillating Current - Pre-Arc Ignition - Switching At f = 1Hz and f = 5kHz. Cropped to Highlight Transient Behaviour

in current magnitude is likely also due to the influence of the reactance of the inductor within the circuit becoming non-negligible (as for pure DC) as load switching frequency increases, resulting in additional impedance and a reduced series current. The periodic change in current is also reflected in the load voltage waveform as seen in Figure. 5.26 and provides a useful test case as input to the WFD detection algorithm as a periodic AC waveform with fixed DC offset and significant frequency content.

Inspection of the lower and higher frequency controlled current switching behaviours in Figure. 5.24 and Figure. 5.25 has indicated that the addition of transient current behaviours and their reflection of circuit load voltage may present additional challenge for arc detection using the WFD algorithm when compared to the controlled resistance switching as in Section.

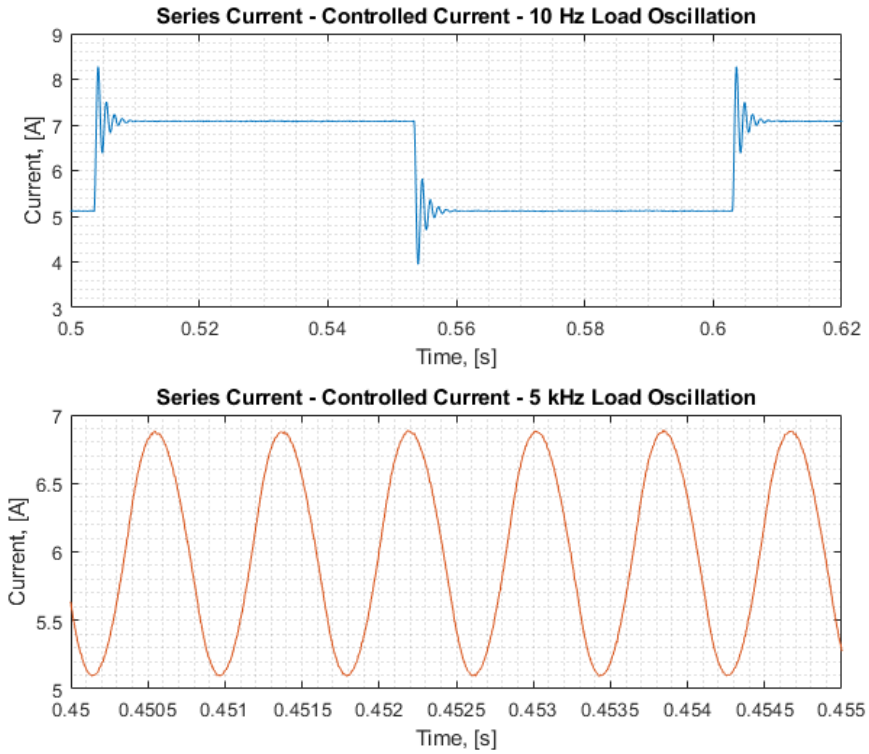


Figure 5.27: Series Current Waveforms for Active Circuit Load, Oscillating Current - Pre-Arc Ignition - Switching At f = 1Hz and f = 5kHz. Cropped to Highlight Transient Behaviour

5.2.2, yet provide useful test cases illustrative of real-world switching transient behaviour. All 24 data captures for controlled current switching were processed using the WFD detection method to test its capabilities against switching current loads, transmission line ringing and DC offset AC waveforms. Shown in Figures. 5.28 and 5.29 are the WFD output traces for the 10 Hz and 1 kHz forced separation arc faults in Figure. 5.24. Additionally, Figures. 5.30 and 5.31 demonstrate the results of applying the WFD detection sceme to the forced failure arcs at 1 Hz and 5 kHZ, as in Figure. 5.25. Table. 5.5 is also provided, highlighting key metrics for both the forced failure and forced separation arc failures.

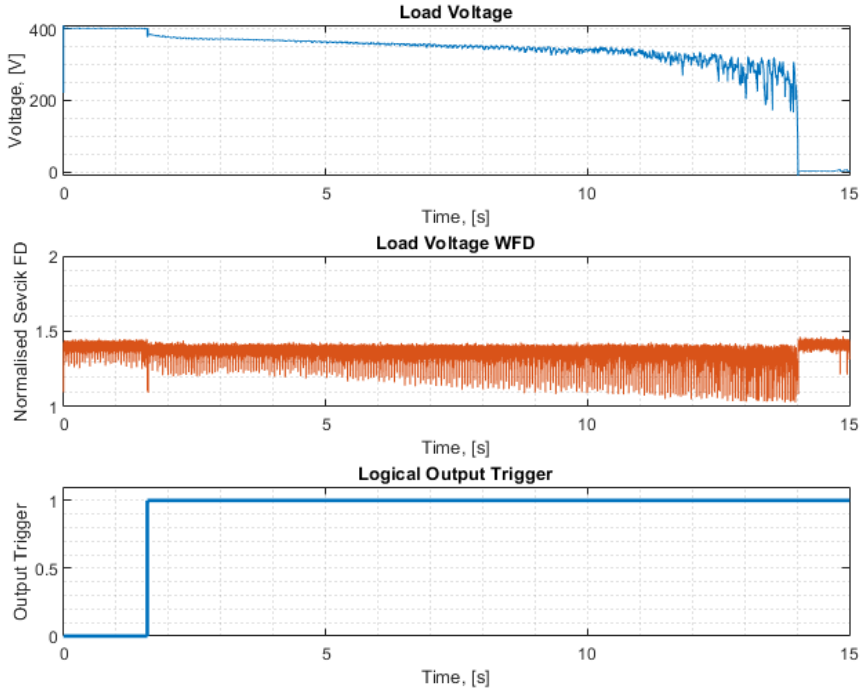


Figure 5.28: Application of WFD to Typical DC Series Arc Load Voltage Waveform with an Active Circuit Load, Forced Separation Ignition, Controlled Current Load Switching at f = 10 Hz

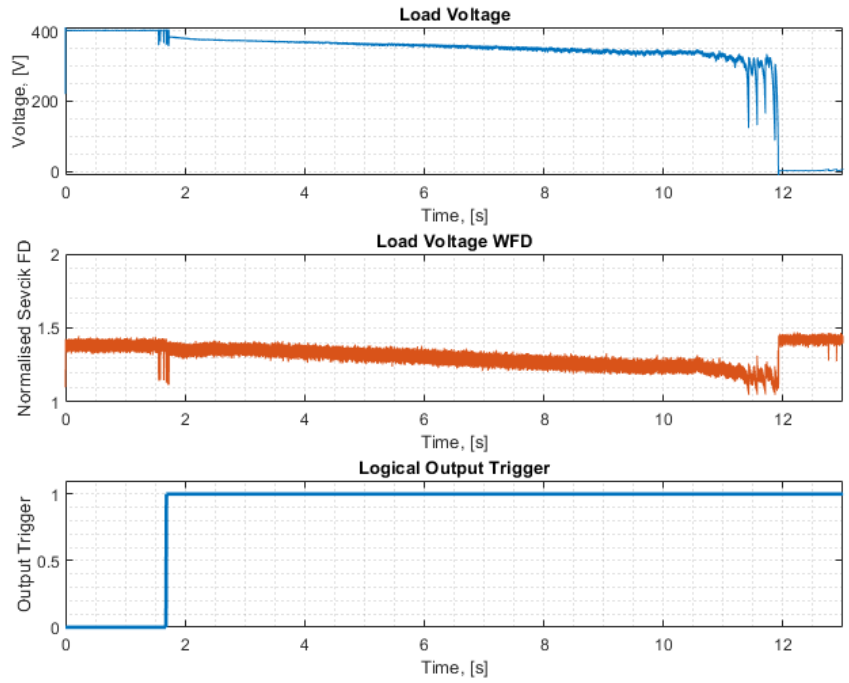


Figure 5.29: Application of WFD to Typical DC Series Arc Load Voltage Waveform with an Active Circuit Load, Forced Separation Ignition, Controlled Current Load Switching at f = 1000 kHz

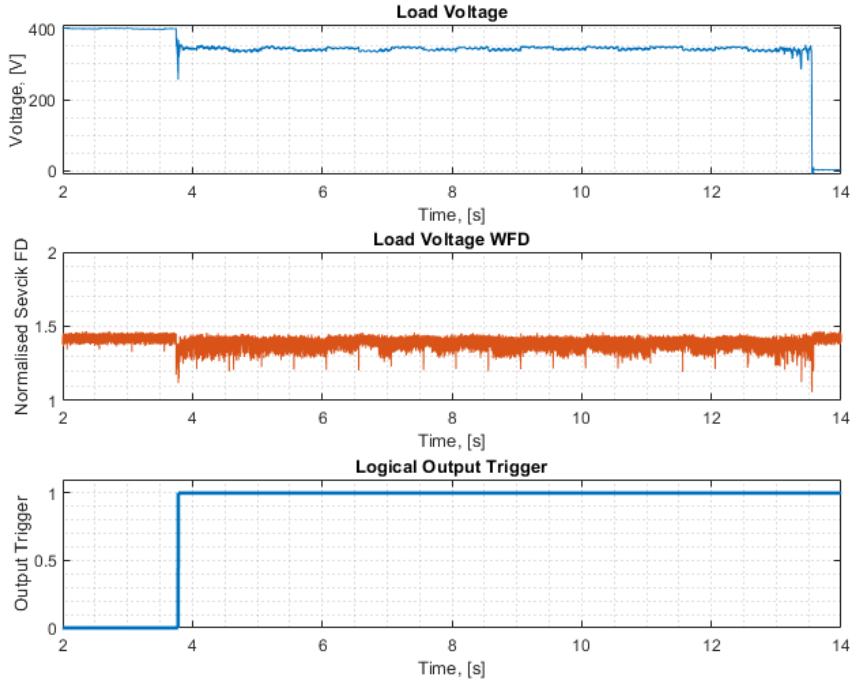


Figure 5.30: Application of WFD to Typical DC Series Arc Load Voltage Waveform with an Active Circuit Load, Forced Failure Ignition, Controlled Current Load Switching at f = 1 Hz

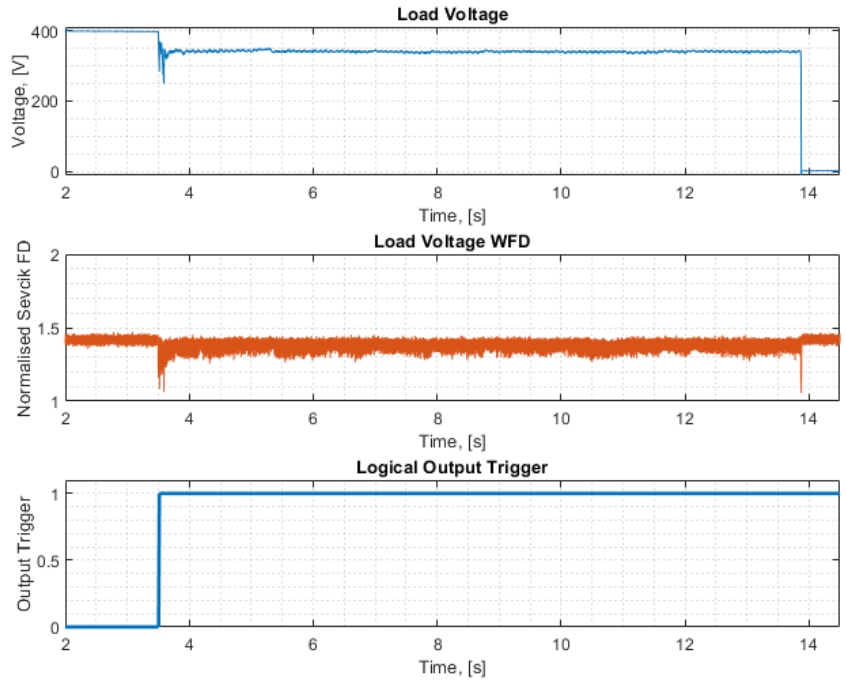


Figure 5.31: Application of WFD to Typical DC Series Arc Load Voltage Waveform with an Active Circuit Load, Forced Failure Ignition, Controlled Current Load Switching at f = 5 kHz

Table 5.5: Table of Active Load Condition WFD Output Results - Controlled Current Load

Ignition Type	**Mean Pre-Arc WFD Value**	**Mean Arc Ignition WFD Value**	**Mean Change in WFD [%]**	**Repeats**	**Success Rate [%]**
Forced-Failure	1.393	1.098	21.17	12	100
Forced-Separation	1.378	1.125	18.36	12	100

It can be seen in the WFD output trace in Figure. 5.28 that the 10 Hz current switching and transient transmission line ringing has had a significant impact on the WFD output trace, producing a negative spike in WFD output at the rising and falling edge of each current transient (a total of 20 times per second). This change in WFD is likely because the ringing transient displays several features that are representative of a fractal waveform, and as such will likely result in a change in fractal dimension. The under-damped sinusoid that occurs as the current switches displays the fractal property of self similarity at arbitrarily smaller scales, with the sine-wave reducing in magnitude but ringing at a fixed frequency. The additional fractal behaviour produced when switching is seen to sum with that of the waveform itself, producing larger spikes in WFD after arc ignition at t = 1.6 s than before. This behaviour can also be observed in the forced failure arc WFD output trace in Figure. 5.30, where the load switches at 1 Hz. Whilst the switching behaviour does produce a response in the WFD algorithm, these responses are very short lived producing only a 6.42 % change in fractal dimension in Figure. 5.28 where these transient spikes are most prominent. The 6.42 % change is not however significant enough of a change in fractal dimension to trigger a false detection before

arc ignition. After arc ignition, the transient spikes summate with the arcing fractal noise and produce a larger WFD response that is beneficial for detection, providing additional opportunities to produce a trigger and indicate an arc has been detected if the initial WFD transient at arc ignition is not sufficient. When not superimposed with arcing behaviour the short-time nature of the switching-induced spikes in WFD are ignored by the threshold based detection method within the WFD process. This requires a constant change in fractal dimension for at least three signal windows (1.5 ms) to trigger a detection, and does not consider the 0.5 ms transients sufficient to indicate an arc unless coupled with other arc induced fractal behaviour.

Despite the robustness of the WFD to this type of transient switching behaviour demonstrated in these test cases, it is clear that there is still the chance for a false-positive detection should the switching transients be longer lived. This could be the case in systems with longer transmission lines and greater line inductance and significant capacitance, producing a longer lived ringing effect when current switches and in turn potentially producing a longer duration change in fractal dimension that could incorrectly trigger an arc detection. A possible option to overcome this is to adjust the WFD to trigger using a different detection scheme, such as a leaky integration, rather than the current threshold based detection. This would average out the influence of the transient spiking over time and make false-positive detection less likely in this case, but would require more calculation steps and signal windows to detect an arc, therefore increasing detection time. Irrespective of the detection scheme applied to the WFD, the ringing caused by transmission line switching is a solved problem, regularly managed through active impedance matching of the transmission line

to the circuit load [121, 122]. As such is very unlikely that the WFD would encounter this particular issue in well-designed power networks, and should not be significantly changed based on this single test case.

In contrast to the issues caused by transient ringing behaviour in Figure. 5.28, the higher frequency load current switching events in both Figure. 5.29 and Figure. 5.31 have very little influence on the WFD output. The WFD algorithm appears not to change in response to the increased frequency content on these waveforms, matching similar results seen in the higher frequency controlled resistance loads in Section 5.2.2, with both responding similarly to passive results shown in Section 5.2.1. The controlled current oscillations for forced separation and forced failure arc ignition produced an average change in fractal dimension of 21.17 % and 18.36 % respectively, similar to the 19.69 % and 17.13 % changes in WFD response at arc ignition seen for the controlled resistance oscillations and 21.97 % and 19.03 % for passive load arcs. Highlighted further in Figure. 5.32 is the response of the WFD algorithm to oscillating controlled current loads at all tested frequencies, for both arc ignition types tested. It is likely that the decreased WFD response seen at lower load switching frequencies is due to the transient ringing caused by switching on the transmission line as previously discussed. This has the effect of making it appear that the WFD detection algorithm performs better on loads with increased frequency content, when in actuality it is the quasi-fractal behaviour of the underdamped sinusoids caused by the transmission line ringing at lower frequencies that is causing poorer performance at lower frequencies in this case. It is likely that without the ringing behaviour, the response of the WFD to increasing load switching frequency would look similar to that for the controlled resistance switching in Figure. 5.19. Regardless, further

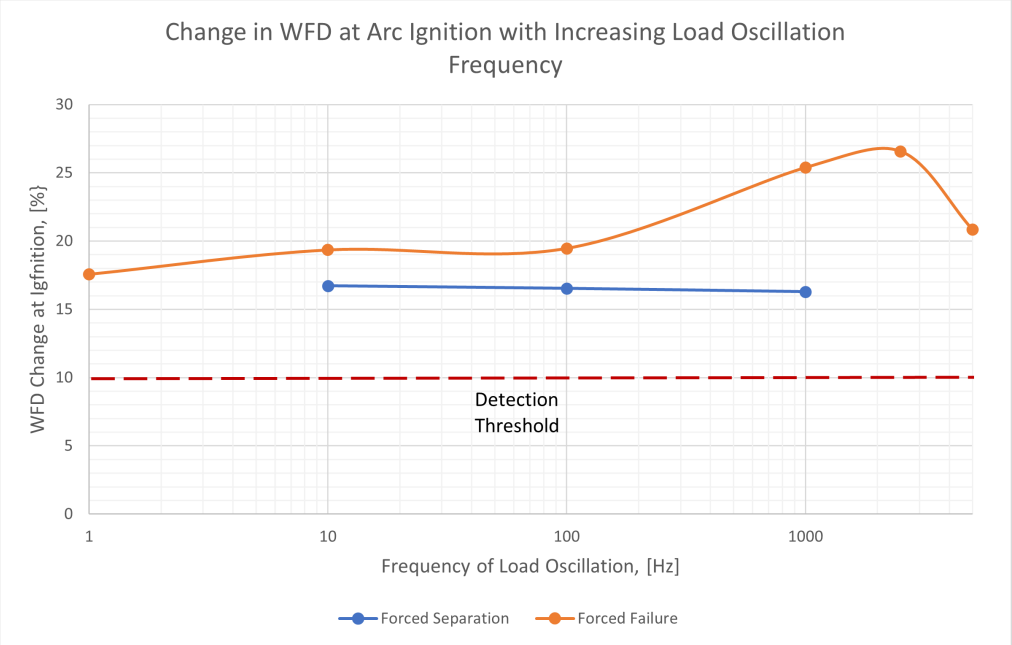


Figure 5.32: Change in Windowed Fractal Dimension with Increasing Load Oscillation Frequency for a Periodically Oscillating Controlled Current Load

experimental tests covering a greater range of load frequencies and specific load behaviours (such as transmission line ringing) are required to fully understand the interaction between the WFD output and load frequency content.

In Figure. 5.32, it is also shown that across all tested frequencies the forced failure arcs produced a greater change in WFD at arc ignition, versus the forced separation arcs. The trend in Figure. 5.32, alongside the tabulated metrics in Table. 5.5, arc consistent with results seen for both the controlled resistance oscillations in Table. 5.3 and the passive load arc fault testing in Table. 5.1. This suggests that irrespective of load frequency content, the dynamics of the arc ignition has a greater impact on the response of the algorithm. This is to be expected, given that the WFD method responds to increases in the fractal dimension caused by superimposed noise from arc failures, and therefore larger arc failures with greater influence over cir-

cuit dynamics and with more dramatic ignitions should produce a stronger output.

For the oscillating load current tests the arc was successfully detected from non-arcing behaviour using the WFD detection scheme in 100% of tested cases. Results have demonstrated both a robustness to increased load frequency content, step-load changes, and to transient transmission line ringing behaviours, providing further evidence to suggest the WFD is suitable for real-world use alongside other arc fault detection techniques. Despite the increased change in fractal dimension at arc ignition versus the controlled resistance load in Section. 5.2.2, oscillating controlled current loads have proved a greater challenge for arc detection, introducing additional transient behaviours to circuit voltage and current traces. Results have indicated that the WFD algorithm may be vulnerable to momentary changes in fractal dimension caused by quasi-fractal behaviour shown in some switching transients. This leads to the potential for further development of the WFD technique using alternative detection schemes, such as a leaky integration, to provide additional resilience against these quasi-fractal behaviours. This is demonstrated in Figs. 5.33 and 5.34 where a simple, unoptimised leaky-integration has been applied to the WFD output to the controlled current 1 Hz load oscillation forced failure arc from Figure. 5.30 and the more problematic 10 Hz load oscillation forced separation arc in Figure. 5.28. It can be seen in both Figs. 5.33 and 5.34 that the application of a leaky integration to the WFD output significantly reduces the influence of short-time pseudo-fractal behaviour on the detection method output, though the influence of this behaviour has not been completely removed. For the leaky integration output, the step-change in integrated output at arc ignition can still be used as the discriminator for arcing, but

would require the addition of a further threshold-based detection targeting the change in leaky integrator output. This in turn adds additional calculation steps and may adversely impact both the calculation speed and detection time of the algorithm, alongside the feasibility of its implementation to off-the-shelf FPGA architecture. Further inspection of the cropped, zoomed-in traces in Figs. 5.35 and 5.36 also highlight how the addition of the leaky integration can actively slow the detection time of the algorithm. In Figure. 5.35 the leaky integrator output for the forced failure arc reaches a minimum value 32.49 ms after arc ignition. Similarly, the for the forced separation arc in in Figure. 5.36 this results in a 18.82 ms delay in response to arc ignition. Hence, the application of a leaky integration has resulted in a practical detection times 21.67 and 12.55 times slower than the theoretical detection time with just a threshold based detection scheme in the current iteration of the WFD algorithm. Considering the leaky integration requires the application of a threshold-based detection method to produce an output trigger, the detection time for each will be reduced further yet, potentially allowing enough time for arc failure to cause permanent damage before detection occurs. As such, there is a trade off in the use of the leaky integration to quench the influence of transient pseudo-fractal behaviours and improve the resilience of the algorithm, versus overall arc detection time that needs exploring fully in future work.

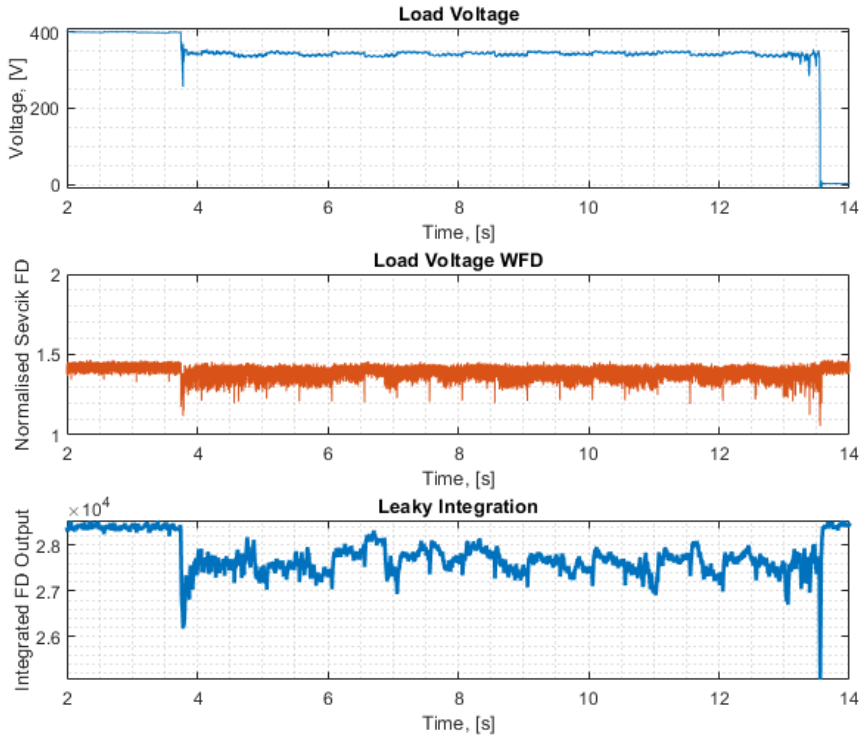


Figure 5.33: Application of Leaky Integration to Forced Failure Series Arc and WFD in Figure. 5.30, Controlled Current Load Switching at f = 1 Hz

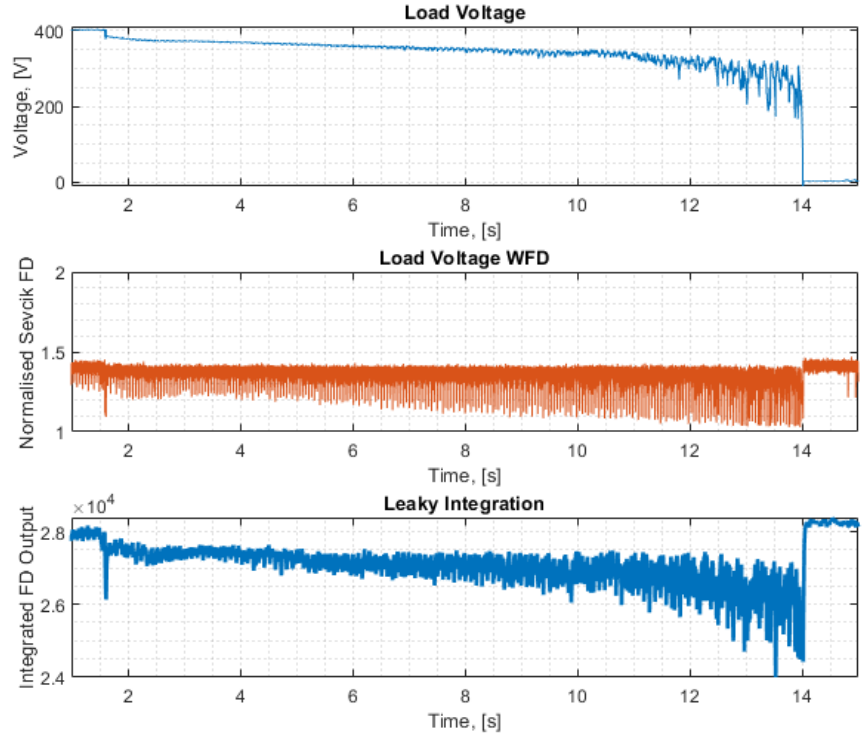


Figure 5.34: Application of Leaky Integration to Forced Separation Series Arc and WFD in Figure. 5.28, Controlled Current Load Switching at f = 10 Hz

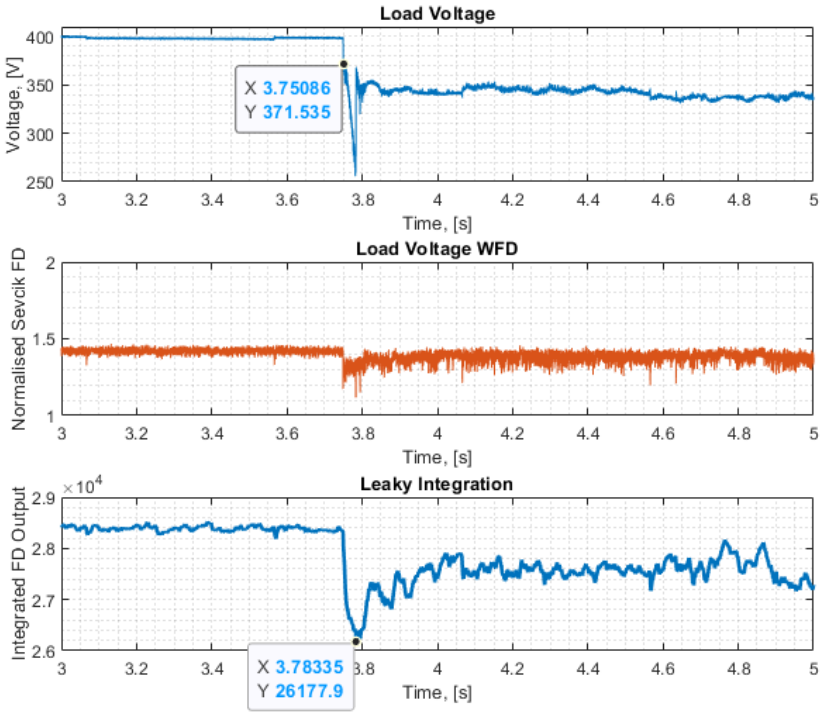


Figure 5.35: Application of Leaky Integration to Forced Failure Series Arc and WFD in Figure. 5.30, Controlled Current Load Switching at f = 1 Hz - Cropped to Highlight Detection Delay

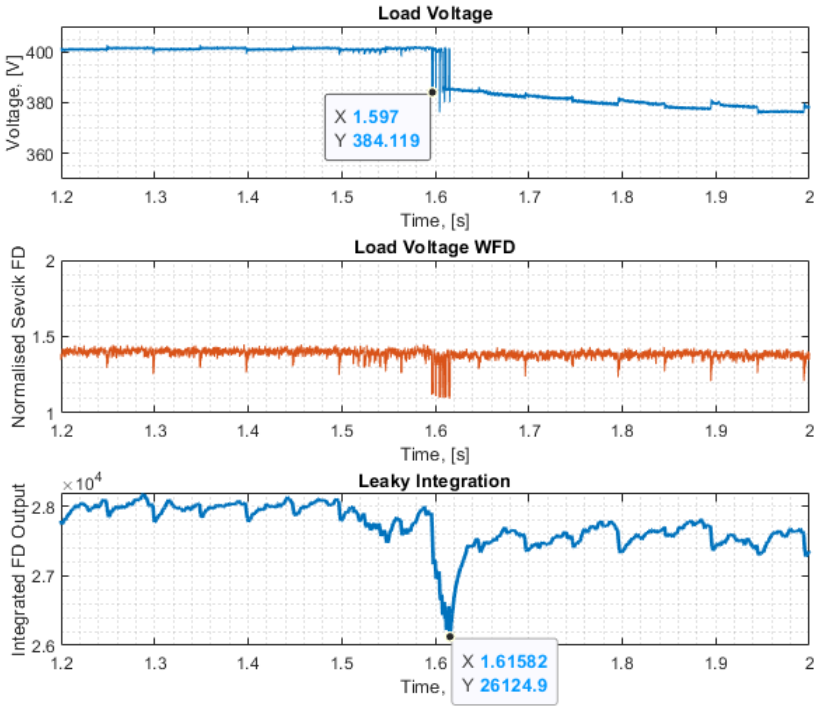


Figure 5.36: Application of Leaky Integration to Forced Separation Series Arc and WFD in Figure. 5.28, Controlled Current Load Switching at f = 10 Hz - Cropped to Highlight Detection Delay

Further experimental work with these alternative detection schemes would then be required to re-assess both the performance of the algorithm as a whole, and the impact the change has had on detection speed, and by extension the computational requirements and feasibility of FPGA implementation. Additional future work should consider testing against arc fault in circuits with a broader range of load frequency content up to the algorithm 25 kHZ lowpass filter cutoff frequency, performing more repeats at each step. This was not completed in the described work due to equipment availability. In testing a greater range of frequencies, the response of the WFD algorithm to a increasing load frequency content can be better understood, and decisions can be made about its suitability for real-world implementation at these higher load frequencies.

5.2.3 WFD Application to Power Networks with Switching Power Electronics

Previous sections have demonstrated the efficacy of the the WFD detection scheme when applied to arc faults in circuits with active and passive load components. These test cases are representative of where the power system transmission line terminates at the circuit load, but algorithm performance when pitted against more complex circuit topologies still need requires consideration. Modern power systems are typically built in a tiered system, stepping down higher voltages used for transmission to lower voltages for application. As such, any modern arc detection method requires validation both not just considering the load end of a power network, but within the network and in the presence of modern switching power converters. To that end, a new experimental setup was constructed as illustrated in

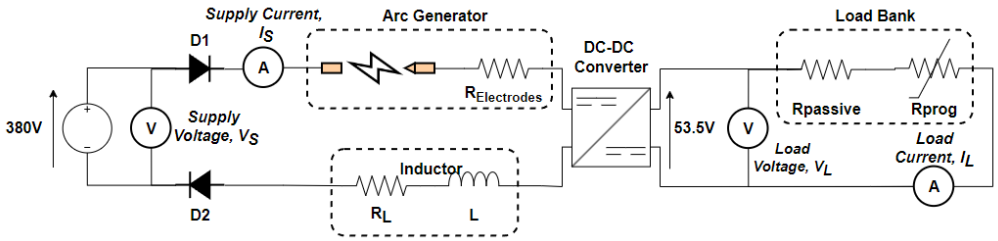


Figure 5.37: Arc Generation Circuit Diagram with DC-DC Power Converter

Figure. 5.37 to simulate a simple power network as may be seen in a more-electric aircraft or heavy-duty more electric vehicle. In Figure. 5.37, the 380 V DC supply voltage represents a higher-voltage DC bus, supplying a commercial DC-DC converter through a simulated transmission line. The converter produces a 53.5 V DC output, connected to a combination of passive and active circuit load components designed to represent a complex, low-power load for the simulated power network, such as an electronic actuator, fan or control system.

Using the experimental setup in Figure. 5.37 a total of 15 arc failures were produced and captured at 2 MHz using a Picoscope 5000 series oscilloscope. Of the 15 total experiments performed, 5 were produced under normal operating conditions with the circuit functioning as intended. The remaining 10 tests were performed with the commercial step-down DC-DC converter operating in Discontinuous Current Mode (DCCM). This low-power "burst mode" style of operation which triggers when the converter load is very small ($<$ 300 W), causing the load current of the DC-DC converter to reduced below the value of the current ripple, resulting in the convertor turning off and on throughout its operation and reduced duty cycle control of the output current and voltage, providing a further challenge for arc detection that may trigger a false or missed detection [118, 119]. These two different tests were designed to produce arc failures within the simulated

power network in both typical (normal) and failing conditions, providing challenging conditions with which to verify the WFD detection scheme. In these tests, all arc failures were produced using forced separation (drawn) arc ignition. As arc failure at the circuit load has been extensively tested, the arc was instead deliberately created between the supply voltage and the step-down converter, representing instead a fault in the transmission line between DC supply bus and the converter supplying the load, providing another test condition in which to assess the WFD arc detection method.

WFD Application under Normal Power Network Operation

Shown in Figures. 5.38 and 5.39 are the typical results of a forced separation arc for the circuit described in Figure. 5.37 for a 13.4 Ω passive load. Figure. 5.38 shows both the input side supply voltage and the circuit load voltage, whilst Figure. 5.39 shows the supply and load side current. In all traces, the arc ignites at t = 1.56 s, resulting in the large transient spike seen in all figures. Both the initial transient spike and the shape of the arc failure no longer match the typical shape of a forced separation arc failure as seen in Figs. 3.4, 5.9, 5.24 and elsewhere in this work and the literature, missing both the characteristic step-change at arc ignition, and the continued reduction in magnitude as the arc elongates and the arc impedance increases. This is likely due to the multiple control elements now present in both the programmable load and DC-DC converter, coupled with the circuit line inductance, reacting to the sudden introduction of the arcs non-linear impedance. The initial arc transient settles after one second, with all waveforms returning to their average value pre-arc, now superimposed with noise from the arc. As the arc noise still forms a significant component of the circuit waveforms (despite the differences produced by the control elements) the WFD detection method should function as

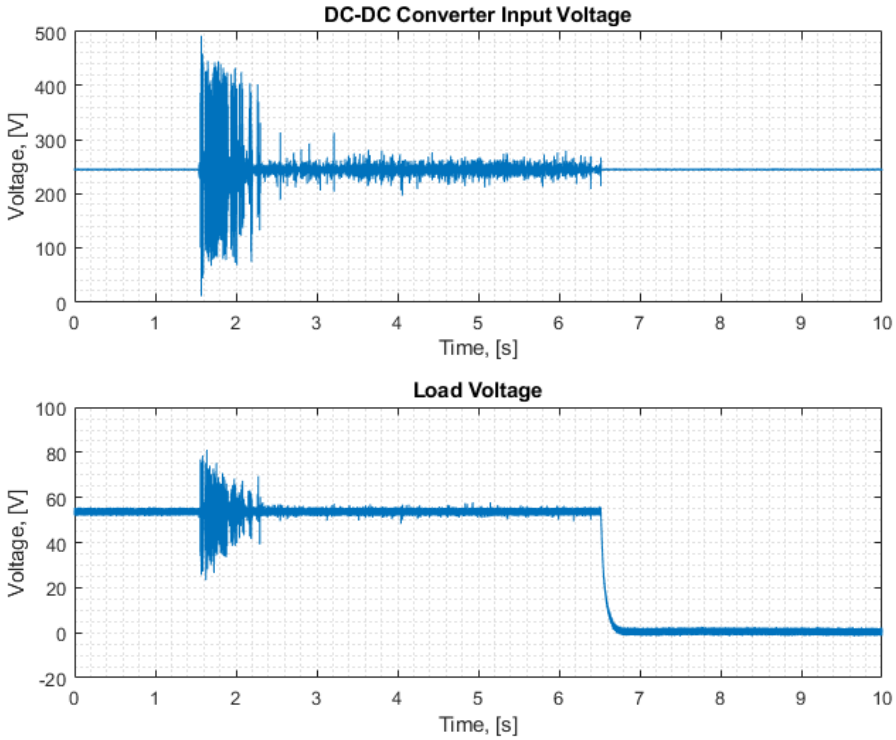


Figure 5.38: Typical DC Series Arc Supply and Load Voltage Waveform (V_s and V_L on Figure. 5.37) containing DC-DC Power Converters - Normal Mode of Operation

intended as it will still be capable of discerning the arc using the fractal behaviour of the superimposed arc noise. This is particularly noticeable on the supply voltage waveform in Figure. 5.38 where measurements were taken physically closer to the arc. All five traces produced in this manner showed similar behaviours, and should also prove to be detectable with the WFD method.

The WFD detection method was applied to all five separate data captures for normal converter operation, and to the voltage waveforms in each case. Shown in Figs. 5.40 and 5.41 are the results of application of the WFD method to the supply and load voltages shown previously in Figure. 5.38. Similarly, Figures. 5.42 and 5.43 show the WFD application to the supply and load currents in Figure. 5.39. It is noteworthy that in Figs. 5.40-5.43

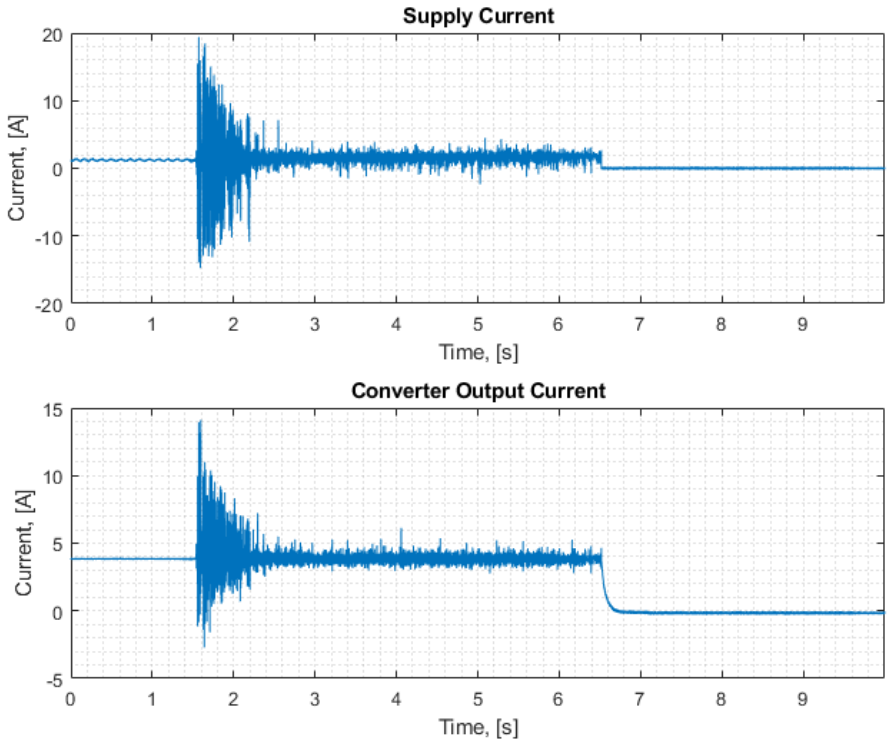


Figure 5.39: Typical DC Series Arc Supply and Load Current Waveforms (I_s and I_L on Figure. 5.37) containing DC-DC Power Converters - Normal Mode of Operation

the resting fractal dimension has increased from 1.41 in previous tests in Section. 5.2.1 and 5.2.3 for passive and active loads, to a new resting value of 1.61. This change in value is not unexpected, as the resting fractal dimension depends on the both circuit topology and the behaviour of the devices therein. In this case, it is likely that the addition of the DC-DC converter has introduced additional non-linear switching behaviours and pink noise that are increasing the base value of fractal dimension from 1.41 seen in earlier testing, to 1.6. This change in resting value with new circuit topology does not however have any impact on the implementation or commissioning required when using the WFD algorithm in a practical setting, as the base/resting RMS value of fractal dimension can be commissioned and adapted dynamically by the algorithm as the method is applied.

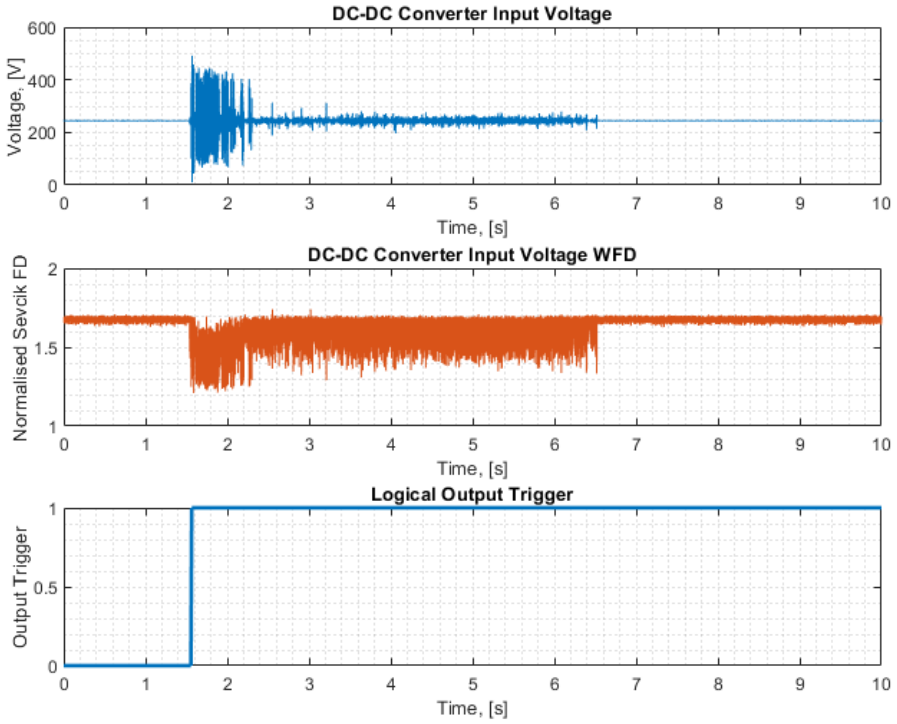


Figure 5.40: Application of WFD to Typical DC Series Arc Supply Voltage Waveform (V_s on Figure. 5.37) containing DC-DC Power Converters - Normal Mode of Operation

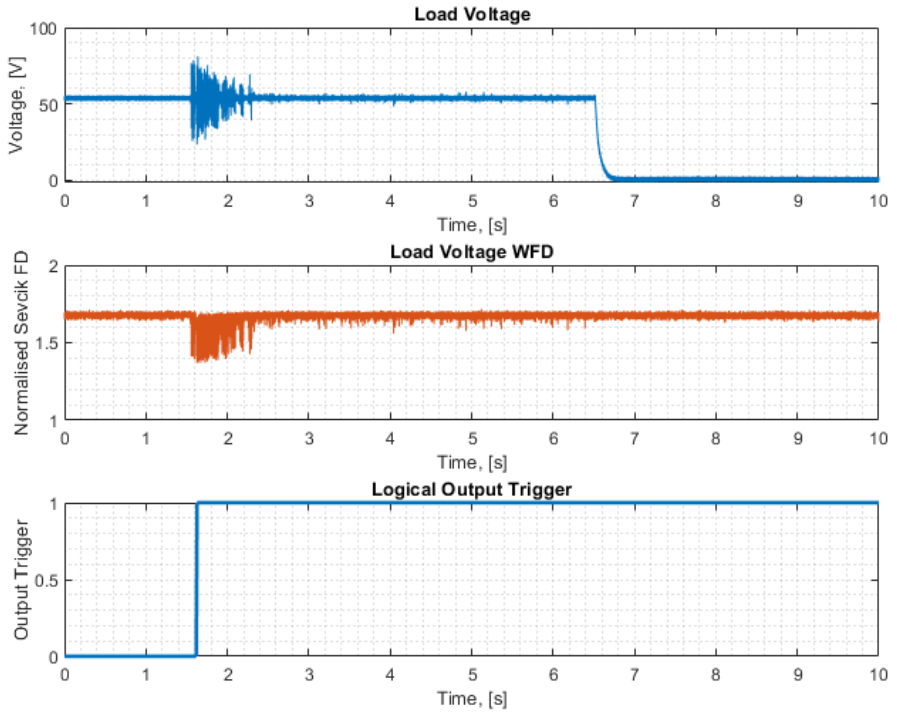


Figure 5.41: Application of WFD to Typical DC Series Arc Load Voltage Waveform(V_L on Figure. 5.37) containing DC-DC Power Converters - Normal Mode of Operation

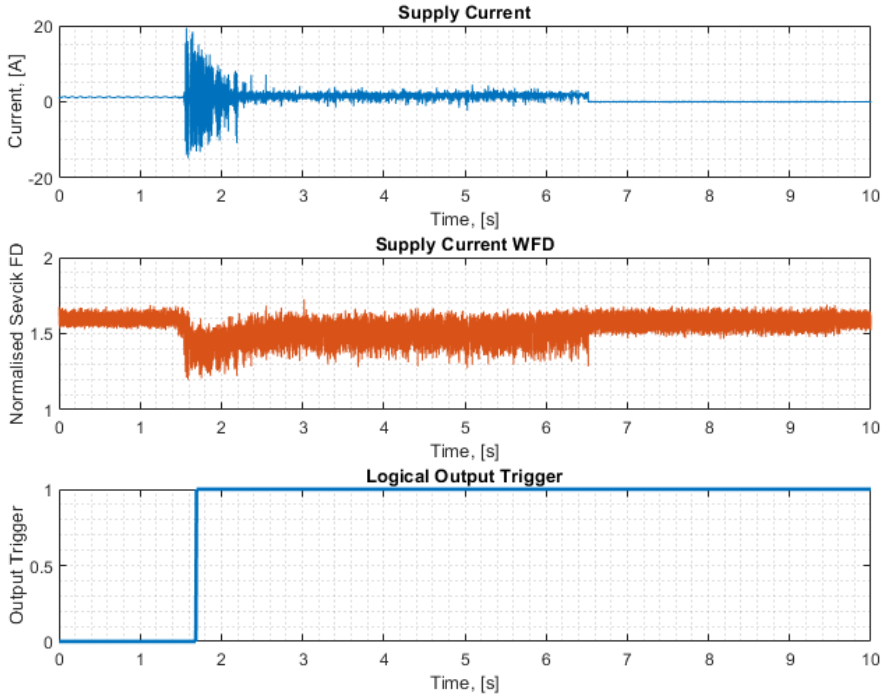


Figure 5.42: Application of WFD to Typical DC Series Arc Supply Current Waveform (I_s on Figure. 5.37) containing DC-DC Power Converters - Normal Mode of Operation

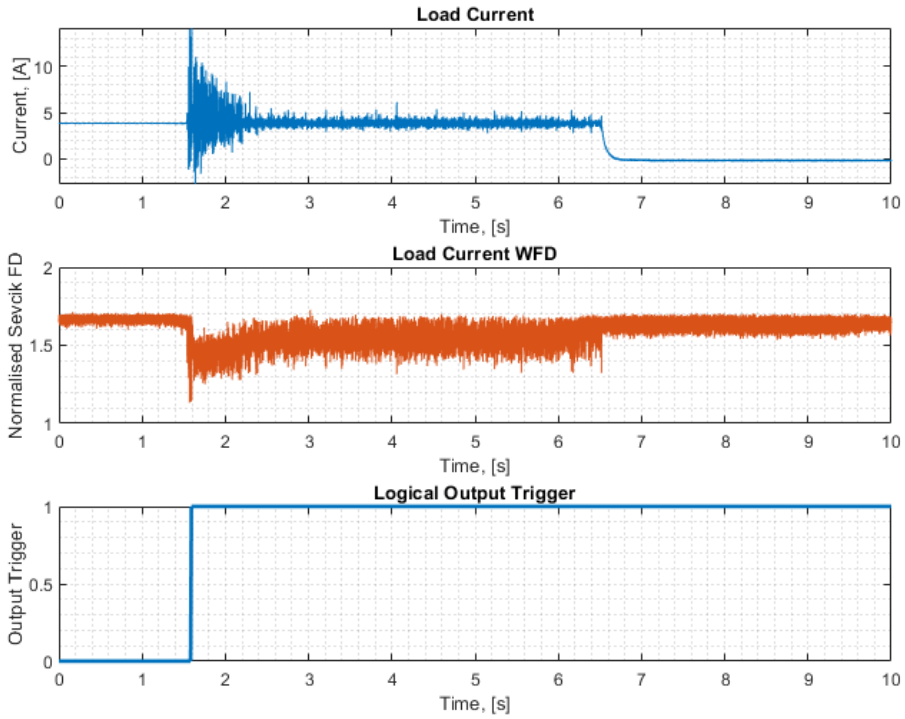


Figure 5.43: Application of WFD to Typical DC Series Arc Load Current Waveform(I_L on Figure. 5.37) containing DC-DC Power Converters - Normal Mode of Operation

It can be observed that for the voltage WFD traces in both Figure. 5.40 and Figure. 5.41 the arc is successfully identified from the initial arc transient behaviour. Both waveforms show a significant change in fractal dimension at arc onset, lasting the entire 1 s duration of the initial transient change at arc ignition. During this transient the WFD output for the supply voltage waveform changes to a value of 1.25, and the load voltage waveform to 1.37; changes of 22.36% and 14.91% respectively from the pre-arc resting value. Additionally, both voltage WFD output waveforms show a response to the superimposed arc noise, though this is considerably greater in Figure. 5.40. This is likely due to the supply voltage measurement being physically closer to the arc failure within the circuit setup, with the load voltage measurement being separated from the arc by the DC-DC power converter. Similar results were seen across all five traces, with the initial arc transient being significant enough for detection in each case, but is greater in magnitude and only produces a significant response to the arc after ignition in the supply voltage waveform.

The supply and load current WFD waveforms in Figs. 5.42 and 5.43 show similar results to the voltage WFD waveforms, producing a clear change in WFD magnitude and detecting the arc in each case. During the initial step change in WFD at arc ignition (t = 1.6 s), the supply current waveform in Figure. 5.42 shows a 25% change from a value of 1.6 pre arc, to a value of 1.2. Similarly, the load current WFD waveform in Figure. 5.43 changes from the pre-arc resting value of 1.6 to a value of 1.15, demonstrating a 28.12% change in WFD output corresponding to the arc ignition. The increased current WFD traces show a greater percentage change than the voltage WFD traces in Figures. 5.40 and 5.41, a results that contrasts earlier results in Section 5.2.1 for passive circuit loads, and Section 5.2.2 for

active circuit loads, where the current WFD waveforms typically displayed a smaller change at arc ignition versus the voltage WFD traces. Additionally, both the supply and load current WFD traces show a continuous change in fractal dimension for the duration of the arc failure, a behaviour not seen in the load side voltage WFD. The improved response of the supply and load current WFDs versus the supply and load voltage waveforms in this test power network is perhaps due to the addition of significant, irremovable capacitance internal to the DC-DC buck converter at the input and output terminals. These capacitors are included to reduce output ripple on the converter voltage waveforms, and their inclusion will likely filter out some of the arc transients, such that they are not reflected on the load side. This can be observed directly when comparing Figures. 5.40 and 5.41 after t = 2.5 s for both the supply and load voltage WFD traces. It can be observed that magnitude of the arc transient noise in the supply voltage WFD waveform in Figure. 5.40 is greater than that of the load voltage WFD in Figure. 5.41, suggesting it has been filtered out to some degree. Comparatively, this is not observed in the current WFD traces in Figs. 5.42 and 5.43, both of which display similar magnitude arc transient behaviour on the supply and load current waveforms after t = 2.5 s, and therefore a similar magnitude response from the WFD method for both supply and load side currents can be expected.

These initial results indicate that the WFD is not only capable of detecting an arc within a power network divided through the use of power electronic converters, but also that a fault can be detected at multiple points within the network. Separation by commercial power electronic circuits appears to attenuate, but not block the propagation of detectable arc noise throughout the power network, allowing for arcs to be detected remotely from the

fault location itself.

WFD Application under Discontinuous Current Mode (DCCM) "Burst-Mode" Power Network Operation

Unlike the "Normal" mode of operation, with a sufficiently large load resistance forcing a low current draw from the DC-DC converter (or $<$ 300 W of output power at 53.5 V) the converter enters Discontinuous Current Mode, a "burst" mode type of operation. Here, the step-down converter can no longer produce a stable output using its normal control methodology, as the converter current is lower in magnitude than the current ripple, leaving the converter current waveform at a zero value for a portion of the switching cycle. This in turn stops porper duty-cycle control of the output, but the converter continues to intermittently switch on and off to maintain some limited power flow to the load [118, 119]. This behaviour produces a difficult condition for arc detection, producing intermittent spikes of current and voltage as the converter switches on and off, that may trigger false positives in impedance based detection methods. The switching can be seen clearly t $<=$ 1.6 s in Figs. 5.44 and 5.45, showing the results of a forced failure arc produced whilst the converter is in burst mode, typical of the 10 total arc fault data captures under these conditions. The burst mode behaviour is of the greatest magnitude on the supply side of the converter, where it effectively operates as an intermittent load to the simulated 380 V DC bus. The regular and sudden changes in current caused by the burst mode operation interact with the circuit line inductance, therefore the producing large voltage spikes also seen when t $<=$ 1.6 s. Comparatively, load voltage and current waveforms do not show this behaviour as can be seen in Figs. 5.44 and 5.45, with no transient spiking of the load-side

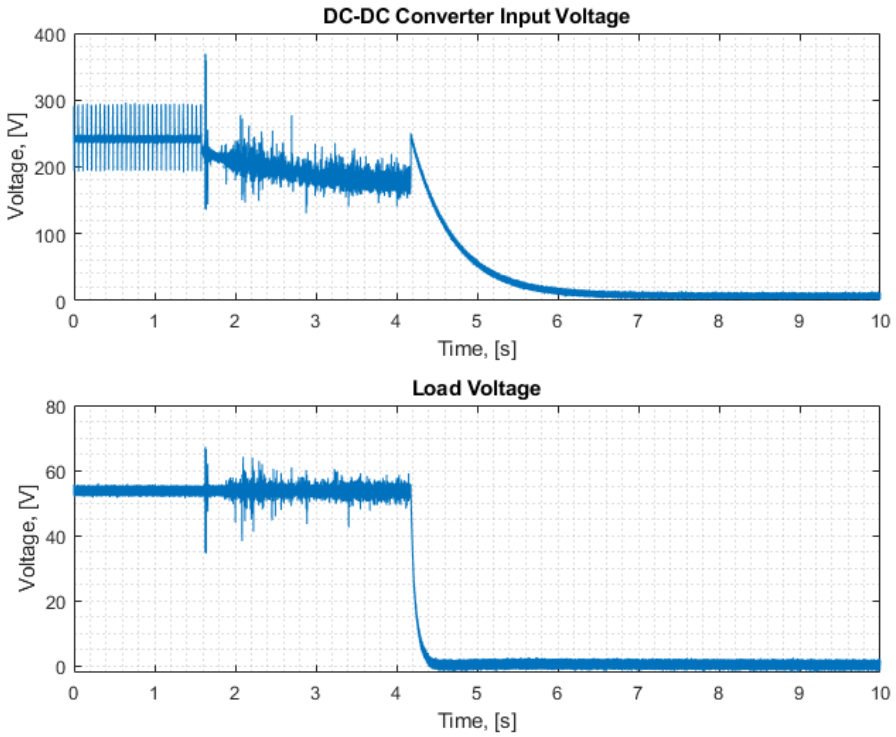


Figure 5.44: Typical DC Series Arc Supply and Load Voltage Waveforms (V_s and V_L on Figure. 5.37) containing DC-DC Power Converters - Burst Mode of Operation

waveforms before arc ignition at t = 1.6 s. This is further highlighted when comparing Figure. 5.52 showing a cropped trace of the pre-arc load voltage and load current waveforms to Figs. 5.50 and 5.51 showing cropped supply voltage and current, where it can be seen that the load side traces do not contain the intermittent switching characteristic of DCCM. The reduced burst-mode response at the load side is to be expected, as the burst mode operation will retain some, limited duty-cycle control of the converter output, despite the a-typical input side operation.

The burst mode arc in Figures. 5.44 and 5.45 show different arc characteristics to those seen during normal converter operation in Figs. 5.38 and 5.39, or in previous passive load and active load arc failures. Most prominent is the return of the gradual reduction in voltage with increasing arc du-

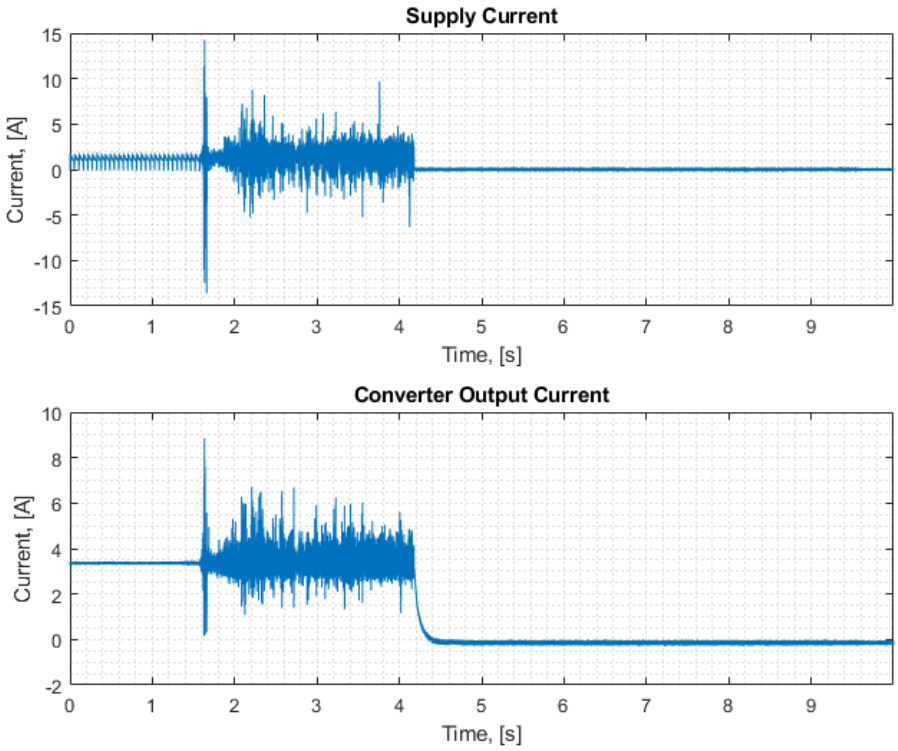


Figure 5.45: Typical DC Series Arc Supply and Load Current Waveforms (I_s and I_L on Figure. 5.37) containing DC-DC Power Converters - Burst Mode of Operation

ration (and arc length) as seen in Figure. 5.44. Under normal operation the switching duty-cycle control of the converter output waveforms would attempt to maintain a constant output, and would therefore attenuate superimposed arc behaviour, as in Figure. 5.38. When operating in burst-mode the level of converter output control is reduced, and can no longer function normally, allowing the reduction in voltage caused by increasing arc impedance to dominate. The additional series impedance introduced by the arc only drives the converter further into DCCM, by reducing the input power supplied to the converter further. Also observable is a large transient spike at arc ignition at t = 1.6 s, reminiscent of the transient step-change seen at arc ignition seen in previous traces for purely passive and active loads but at a considerably greater magnitude. When compared to normal converter operation, the burst mode arcs in Figs. 5.44 and 5.45 show a greater amount of the superimposed arc noise across all waveforms after

arc ignition. This is particularly contrasting in the load voltage waveforms for normal mode (Figure. 5.38) and burst mode (Figure. 5.44), where arc transient behaviour during arc burning is of much greater magnitude in the burst-mode arc. This is possibly due to the reduced level of voltage control of the converter during DCCM burst mode. When in DCCM the transfer function of the converter becomes non-linear, and massively reduces the efficacy of duty cycle control of converter output voltage [118, 119]. This may therefore allow for more of the arc noise to propagate through the converter, now being influenced less by the switching control of the output voltage, and therefore be more prominent on the load side of the converter.

All 10 burst mode traces were processed with the WFD detection method, with Figures. 5.46 and 5.47 showing the results of WFD application to the converter input voltage and circuit load voltage traces highlighted previously in Figure. 5.44, and Figures. 5.48 and 5.49 showing WFD application to the supply and load current waveforms in .Figure. 5.45

A clear contrast can be seen in the supply voltage WFD waveform Figure. 5.46, and in the supply current WFD waveform in Figure. 5.48 when compared to other arc failures without the burst mode spiking pre-ignition. It is obvious from these traces that the burst mode behaviour causes a noticeable increase in fractal dimension, reminiscent of the spikes in WFD seen previously with the low-frequency oscillating current loads in Figure. 5.28 from Section 5.2.2. The cause of the transient peaks in WFD output seen when $t < 1.6$ s in Figure. 5.46 becomes apparent when looking at the individual burst mode transients in the supply voltage and current waveforms. These are shown in Figure. 5.50 and 5.51 where the supply voltage and current waveforms have been cropped to highlight two individ-

ual burst-mode pulses. It can be seen that each transient pulse produces a "ringing" effect, resembling an under-damped sinewave, on the falling edge of each voltage pulse, and the rising edge of each current pulse, near identical to the transmission line ringing seen for the active, oscillating current load in Figure. 5.27. These voltage and current transients are produced as discussed in Section 5.2.2, but are likely the result of RLC oscillators formed through the combination of circuit resistance, line inductance and the converter input filter capacitance. With under-damped sinusoids being psuedo-fractal (Displaying only one of the properties required to be a fractal: self-similarity at increasingly smaller scales, and therefore not a "true" fractal) a change in WFD output is to be expected. Whilst this psuedo-fractal behaviour cannot be eliminated from WFD identification, as previously discussed in Section 5.2.2, the risk of false detection can be mitigated through the replacement of the existing threshold-based detection method to one with built-in averaging; such as a leaky integration. This change would inherently slow arc detection time and increase the number of operations required of the algorithm, and as such would be the subject of future work. Despite the WFD spiking caused by the burst-mode transients, it can be seen that the spikes do not trigger a detection as they do not produce a change in WFD that is long enough in time to be counted as significant by the WFDs threshold based detection scheme, as it does not appear in enough consecutive 0.5 ms windows of signal sampled as inputs to the WFD method.

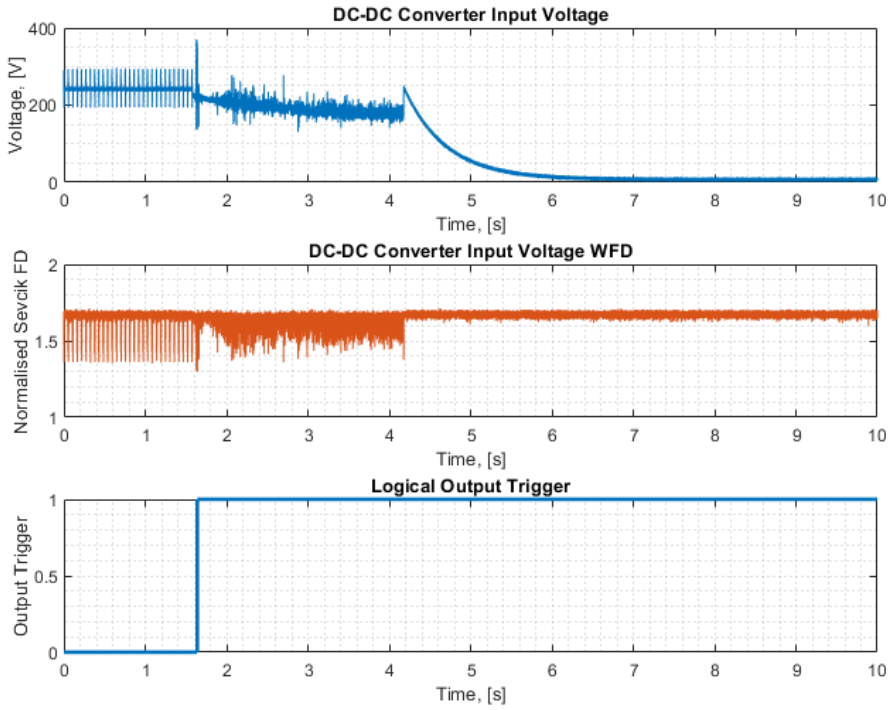


Figure 5.46: Application of WFD to Typical DC Series Arc Supply Voltage Waveform (V_S on Figure. 5.37) containing DC-DC Power Converters - Burst Mode of Operation

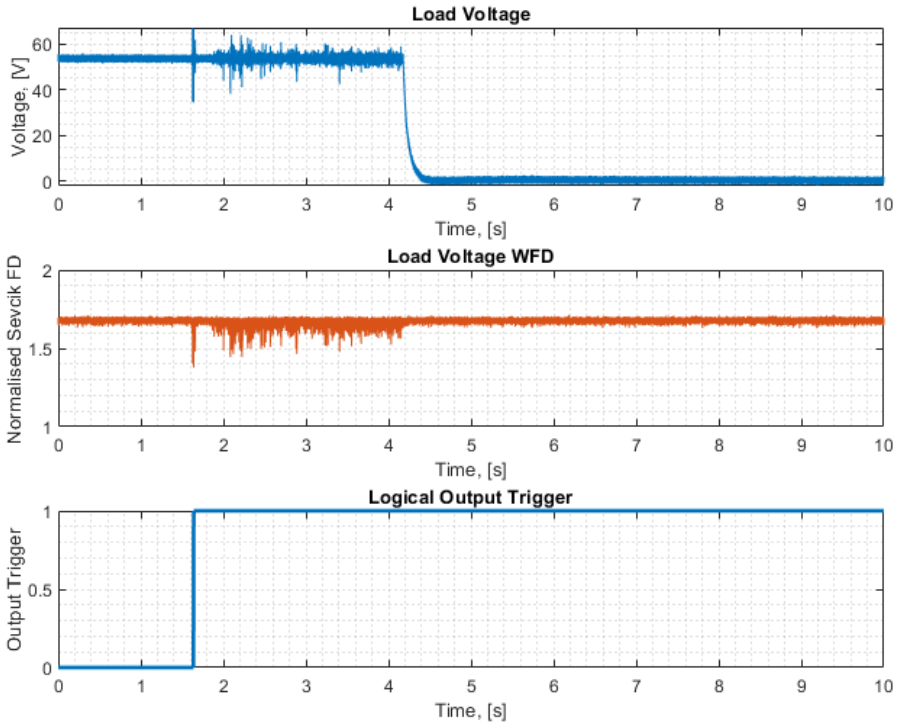


Figure 5.47: Application of WFD to Typical DC Series Arc Load Voltage Waveform (V_L on Figure. 5.37) containing DC-DC Power Converters - Burst Mode of Operation

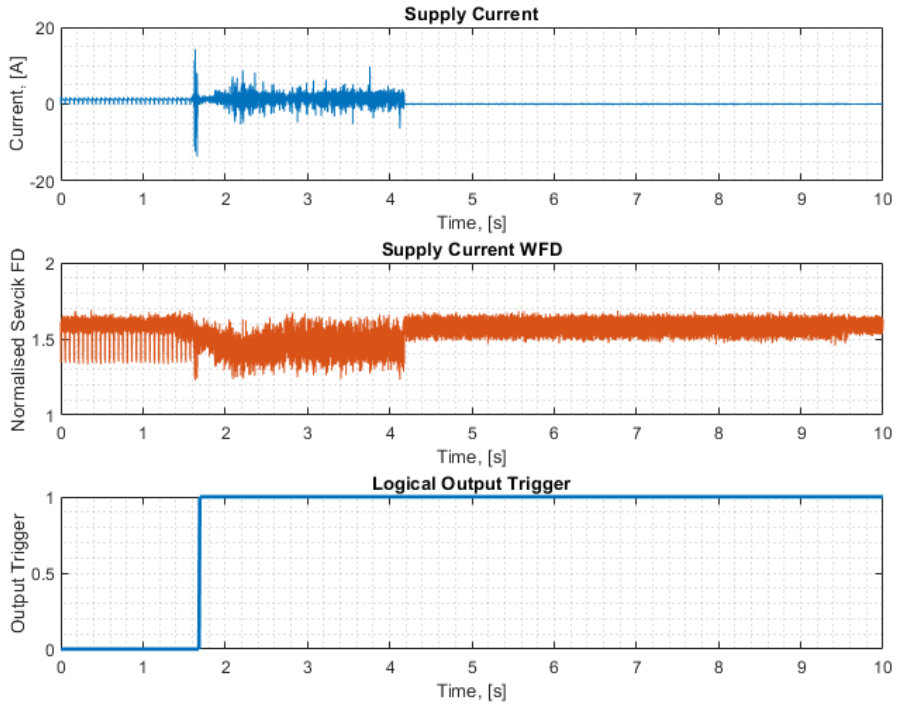


Figure 5.48: Application of WFD to Typical DC Series Arc Supply Current Waveform (I_S on Figure. 5.37) containing DC-DC Power Converters - Burst Mode of Operation

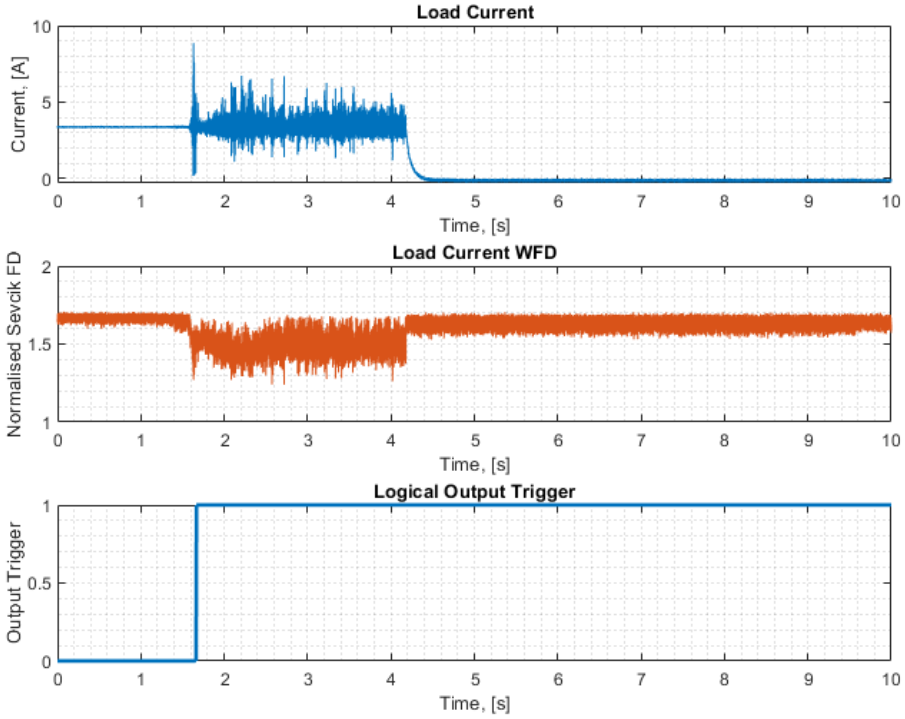


Figure 5.49: Application of WFD to Typical DC Series Arc Load Current Waveform (I_L on Figure. 5.37) containing DC-DC Power Converters - Burst Mode of Operation

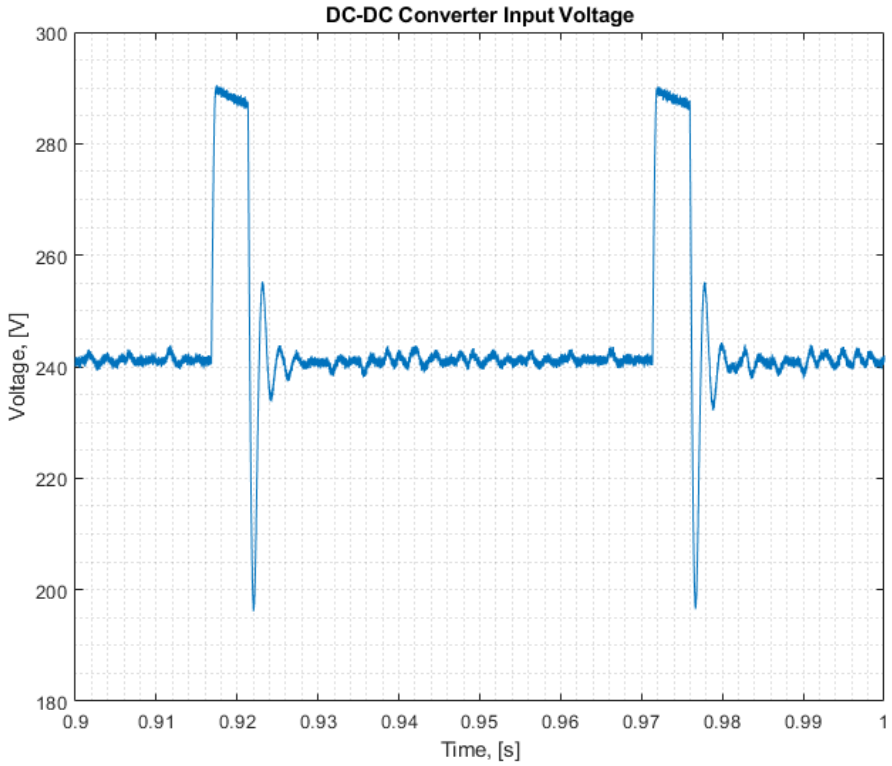


Figure 5.50: Typical DC Series Arc Supply Voltage Waveform (V_S on Figure. 5.37) containing DC-DC Power Converters - Burst Mode of Operation - Cropped to Show Burst-Mode Behaviour

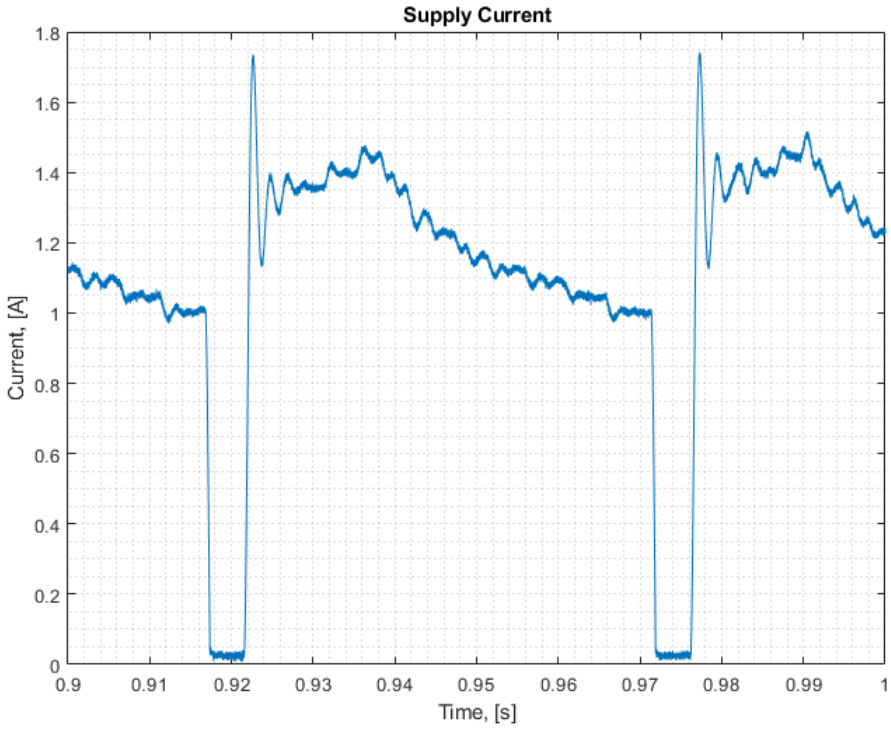


Figure 5.51: Typical DC Series Arc Supply Current Waveform (I_S on Figure. 5.37) containing DC-DC Power Converters - Burst Mode of Operation - Cropped to Show Burst-Mode Behaviour

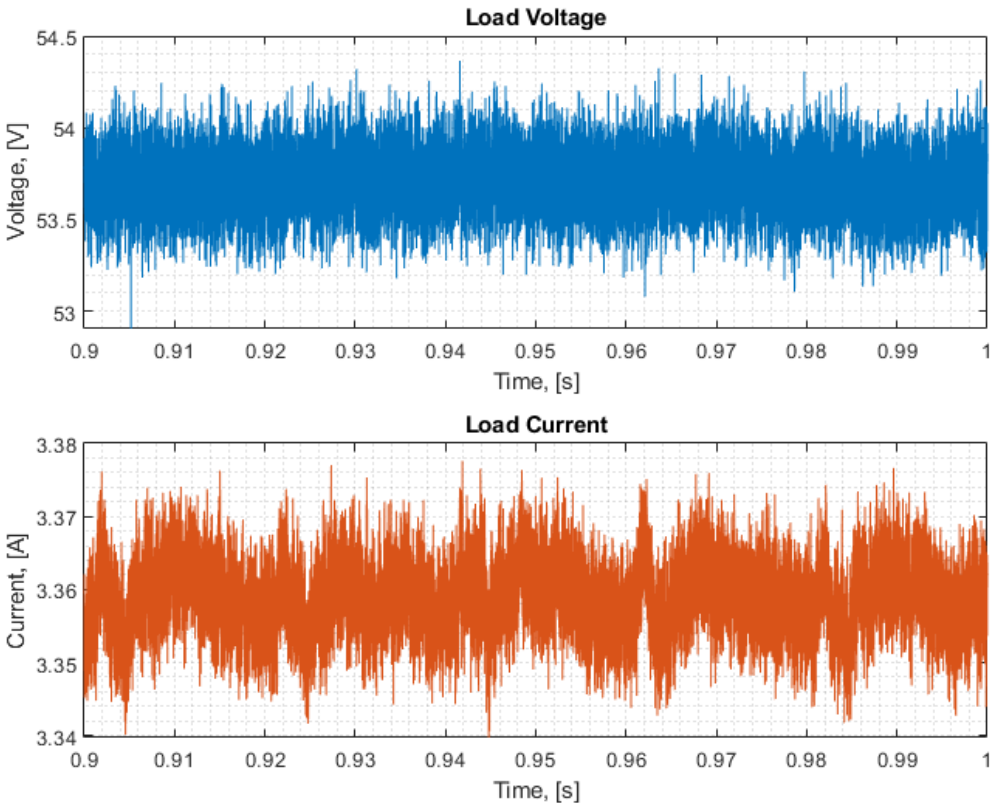


Figure 5.52: Typical DC Series Arc Load Voltage and Load Current Waveforms (V_L and I_L on Figure. 5.37) containing DC-DC Power Converters - Burst Mode of Operation - Cropped to Show Burst-Mode Behaviour

In both Figure. 5.46 and Figure. 5.47 for the supply and load voltage WFDs, the arc can be seen to be detected from the WFD trace at the point of arc ignition at t = 1.6 s. As previously seen with the normal-mode converter arcs at both the converter supply and load side produce a significant change in WFD at arc ignition, and produced a measurable response to the superimposed arc noise on both waveforms. Here, the WFD output value changes to a value of 1.32 in the supply side voltage WFD waveform, and 1.4 on the load voltage WFD; changes of 18.01% and 13.04% respectively from the 1.61 pre-arc resting value. The change in WFD is again greater in magnitude on the converter supply side in Figure. 5.46, physically closer to the arc itself than the load side voltage in Figure. 5.47, a trend seen across all 10 burst mode arcs tested. When compared to the normal-mode

converter arcs in Figs. 5.40 and 5.41, the volatge WFD burst-mode arcs in Figs. 5.46 and 5.47 show a reduced change in WFD at both arc ignition and throughout the arc burning phase. This occurs despite the superimposed arc noise being greater in magnitude in burst-mode during the arc burning phase for both supply and load side voltage waveforms. One potential cause of the reduction in WFD response is that the burst-mode response of the converter interferes with the behaviour of the arc and results in modification of the arc noise superimposed on the circuit voltage and current waveforms. This can be seen in Figures. 5.53 and 5.54 showing load voltage and load current for both converter burst-mode and normal-mode, cropped between 2-4 s to highlight the arcing behaviour. It can be seen in the burst-mode waveforms in Figs. 5.53 that when the arc is fully established after t = 3 s there is considerably more variation in the burst-mode load voltage and current waveforms during the arc burning phase than in the normal-mode load voltage and current in Figure. 5.54. However, it is unclear how the burst-mode converter responds to arc failure and therefore conclusions about the arc-converter interaction cannot be drawn at this stage, or without extensive additional testing.

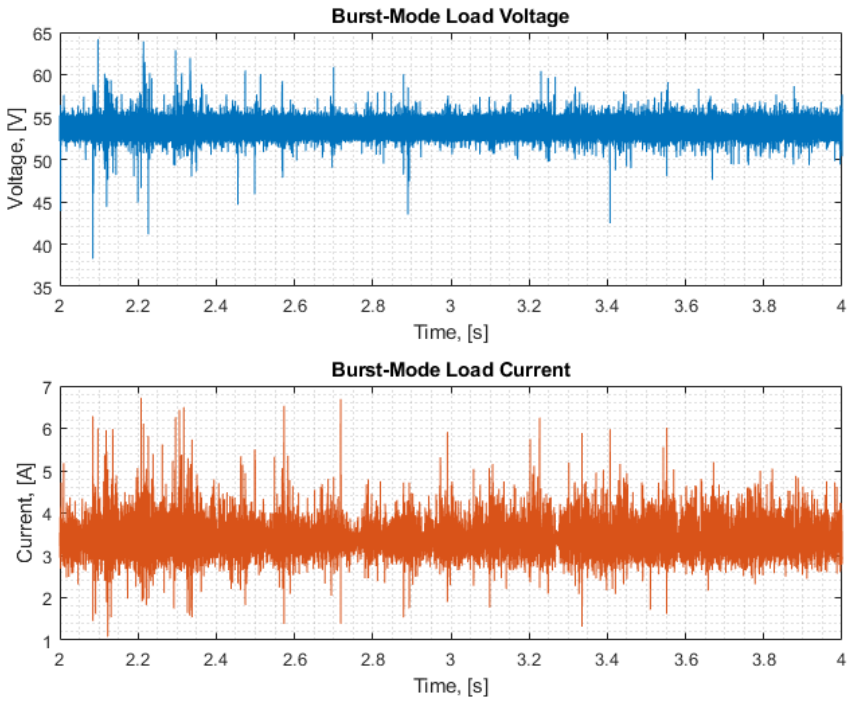


Figure 5.53: Typical DC Series Arc Load Voltage and Load Current Waveforms (V_L and I_L on Figure. 5.37) containing DC-DC Power Converters - Burst Mode of Operation - Cropped to Show Arc Behaviour

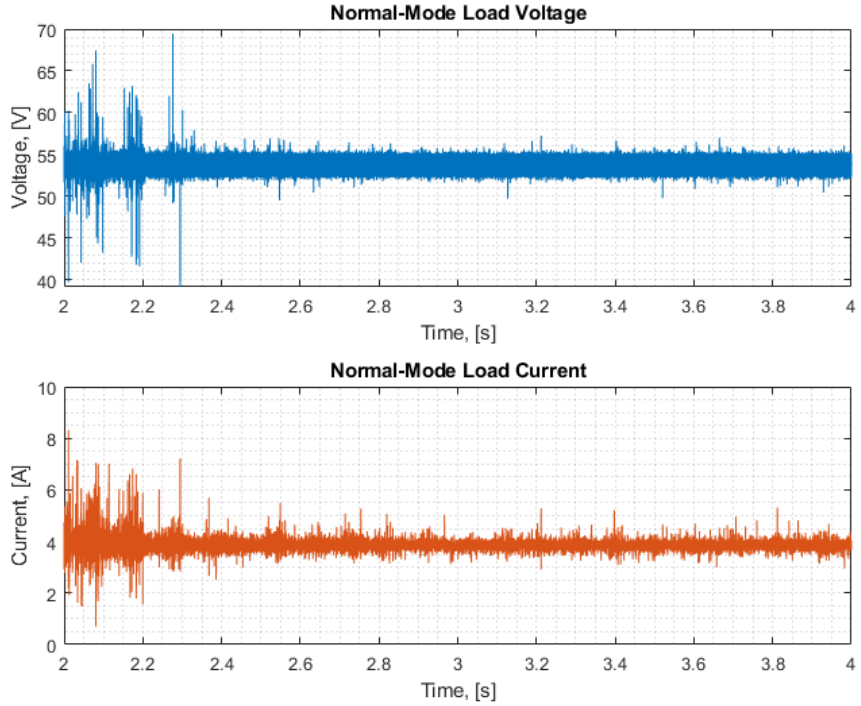


Figure 5.54: Typical DC Series Arc Load Voltage and Load Current Waveforms (V_L and I_L on Figure. 5.37) containing DC-DC Power Converters - Normal Mode of Operation - Cropped to Show Arc Behaviour

In Figures. 5.48 and 5.49 the WFD is applied to both the supply and load current waveforms. Both show similar trends to the supply and load voltage WFD counterparts, with burst-mode transients visible on the supply current WFD in Figure. 5.48 as it was for the voltage WFD in Figure. 5.46. Additionally, both supply and load current WFD waveforms are shown to detect the arc at arc ignition (t = 1.6 s), with the burst mode behaviour seen before t = 1.6 s being ignored by the threshold based detection scheme. A change in WFD of 19.38% is seen at arc ignition in Figure. 5.48, with a similar 23.75% change in WFD observed at the same point in Figure. 5.49, more that sufficient to indicate an arc has been detected. Both traces also display an ongoing change in fractal dimension throughout the arc burning phase, similar to that that was seen earlier in current WFD waveforms for the converter normal-mode arcs in Figs. 5.42 and 5.43. The convertor input and output capacitance appears to have continued influence the supply and load voltage WFD waveforms, resulting in a reduced response from the load voltage WFD in Figure. 5.47 versus the supply voltage WFD in Figure. 5.46. Both of these voltage WFD traces show a smaller magnitude response compared to the supply and load current traces in Figs. 5.48 and 5.49 as was previously seen during normal-mode operation, possibly as a result of the capacitive filtering.

Results in Figures. 5.46 - 5.49 for arcs in systems containing DCCM burst-mode operation converters have demonstrated that the WFD method is capable of discriminating an arc failure, despite the challenging detection conditions. Results also support the earlier observation that detectable fractal noise from arc failure can propagate through commercial DC-DC converters, despite some attenuation. This matches results seen in Figs. 5.40 and 5.41 for normal-mode converter arcing showing the same reduction

in signal strength with separation from the point of arc ignition by the DC-DC converter. It has also been observed that in the presence of switching power electronics with significant capacitance, application of the WFD method to circuit current measurements can produce a larger change in WFD magnitude compared to circuit voltage measurements, contrasting previous passive and active load results seen in Sections 5.2.1 and 5.2.2 of this chapter for passive and active load circuits without switching power electronics. Future work should consider methods to improve the application of the WFD to current measurements, such that the technique is applicable across additional load types, therefore allowing voltage WFD and current WFD measurements to be used in tandem to discriminate an arc, increasing the level of confidence of the algorithm, whilst reducing the chance of false or missed detections.

Application of a Typical Time-Domain Arc Detection Method to DC Series Arc Failure within A Power Network containing Switching Power Electronics in Discontinuous Current Mode (DCCM) "Burst-Mode" Operation

To provide a point of comparison for the application of the WFD method to switching power electronics, the impedance based current differential and leaky integration technique previously demonstrated in Chapter. 2 was applied to arc faults captured on the circuit in Figure. 5.37 during DCCM "burst mode" operation. Shown in Figure. 5.55 is applications of the current-differential leaky integration to the burst-mode supply current waveforms shown in Figure. 5.45. It can be seen in Fig 5.55 that the detection method produces a substantial response to the arc from the leaky integrator, increasing from a value of around 10, to in excess of 250 fol-

lowing arc ignition. This would be more than sufficient to indicate an arc had been detected using the same detection threshold of 19 (as required to detect passive load arc faults in Figure.2.2 in Chapter. 2). However, due to the large magnitude change of the leaky integration output in Figure. 5.55 the response of the technique to the burst mode behaviour is hidden.

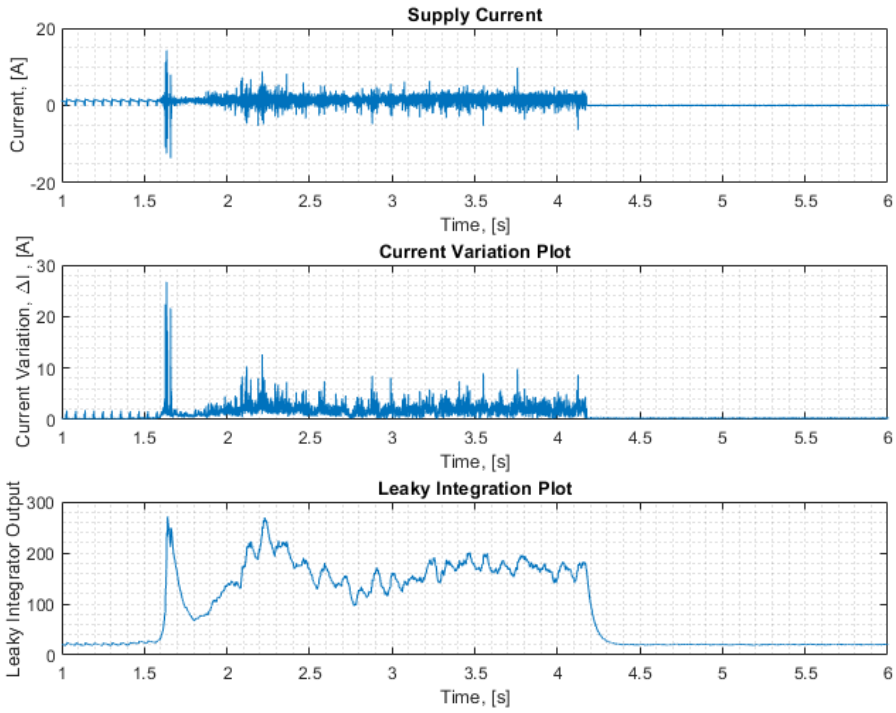


Figure 5.55: Application of Typical Impedance Based Detection Method to Typical DC Series Arc Supply Current Waveform (I_s on Figure. 5.37) containing DC-DC Power Converters - Burst Mode of Operation

Cropping this trace to the first second of pre-arc behaviour as shown in Figure. 5.56 highlights that the burst-mode transients pre-arc cause a similar rippling effect on the leaky integrator output. It can be seen in Figure. 5.56 that the leaky integrator output reaches a magnitude of 24 after several burst-mode transients, and would therefore trigger a false positive detection from non-arcing DCCM circuits when utilising the existing detection threshold magnitude of 19 established from passive load testing in Chapter. 2. Whilst tuning of this threshold variable to avoid false positives

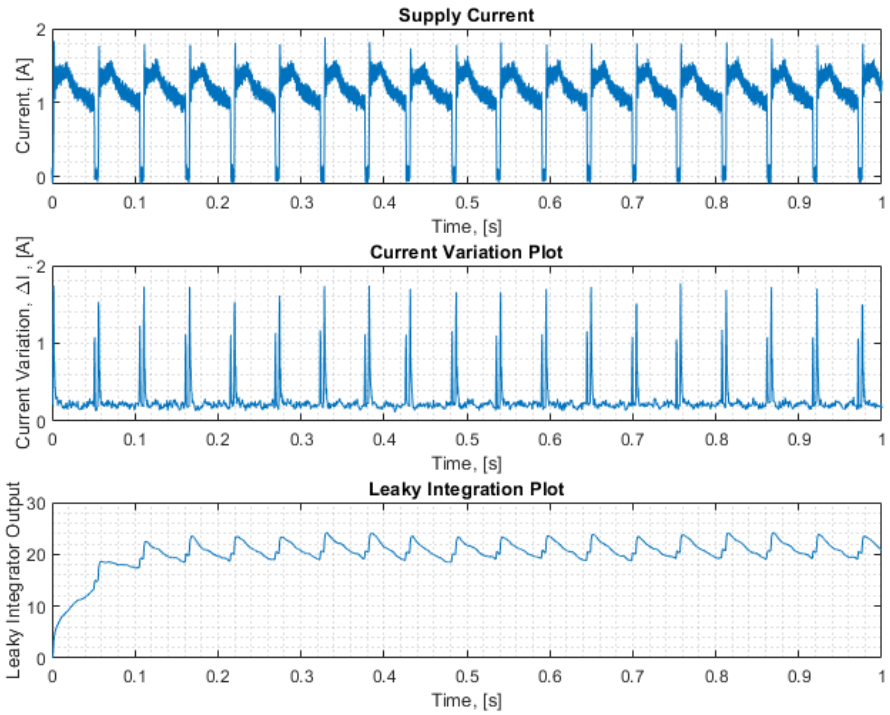


Figure 5.56: Application of Typical Impedance Based Detection Method to Typical DC Series Arc Supply Current Waveform (I_s on Figure. 5.37) containing DC-DC Power Converters - Burst Mode of Operation - Zoomed to Show Burst-Mode Response

is possible, it presents an additional challenge for commissioning, as there is an inherent trade-off between detecting arcs in passive networks where the output response of the detection technique to the arc is smaller, and to avoiding false-positives from other current transients. The method also continues to introduce a delay in detection time through the leaky integrator response, taking 40 ms to react to changes in current differential (as was also observed in Chapter. 2).

Avoiding false positives and producing a detectable change at arc ignition whilst maintaining fast arc detection are all challenges that make DC series arc fault detection more difficult when operating in a DCCM burst-mode operation. Compared to the typical impedance based method, the WFD method produces a faster response to the arc, reacting in as little as 1.5 ms

versus the 40+ ms in the impedance based method, and is more resilient to the current transients caused by DCCM switching behaviours, producing no false positives. Additionally, the WFD method has been shown to function without adjustment across a range of load topologies where the typical impedance based technique has either failed, or highlighted the need for additional tuning and commissioning.

Potential for Arc Location with WFD

Within the field of arc detection, the gold-standard is rapid, reliable arc failure detection and circuit interruption. Following the arc failure and circuit interruption, the faulty system will then be brought offline and inspected, followed by repairs and re-commissioning. For very large DC power networks, such as those in electric aircraft, this becomes a very laborious, time consuming, and expensive process. As such, determining the location of the failure within the network before the inspection and repairs process is advantageous, both from a financial perspective and also from the operation perspective, allowing the operator to shut down only fault afflicted systems, rather than the entire power distribution network.

Collectively, the results demonstrated in Figure. 5.40 and Figure. 5.41 for normal-mode DC-DC converter operation and Figures. 5.46 and Figure. 5.47 for burst-mode converter operation show two unique features that provide the foundations for utilising the WFD arc detection scheme for arc location within a broader power network:

- Arc fault fractal noise is capable of propagating through power-electronic converters and is detectable after propagation using the WFD method.

- The magnitude of WFD response decreases with increasing separation from the arc fault, showing a reduced magnitude after propagating through the DC-DC converter.

Consider then a larger DC distribution network with several step-down power converters in sequence, such as that shown in Figure. 5.57, containing also a battery and several loads. Here the regions between adjacent converters have each been highlighted with a different color. From findings in earlier experimental results (e.g. the converter normal mode traces in Figs. 5.38 - 5.39 and burst mode voltage traces in Figs. 5.44 - 5.45) it can be expected that an arc fault within this network, say between converters B and C as highlighted in the figure, would produce arc noise that is measurable throughout the network, despite the additional converters. If the WFD detection method is applied to voltage measurements between each converter in the network, it will produce a response proportional to its distance from the fault. By comparing the magnitude of the WFD response throughout the network, as in Figure. 5.58, it may be possible to determine where within the power network the arc failure has occurred, with the greatest magnitude response likely being closest to the arc, therefore indicating the position of the arc.

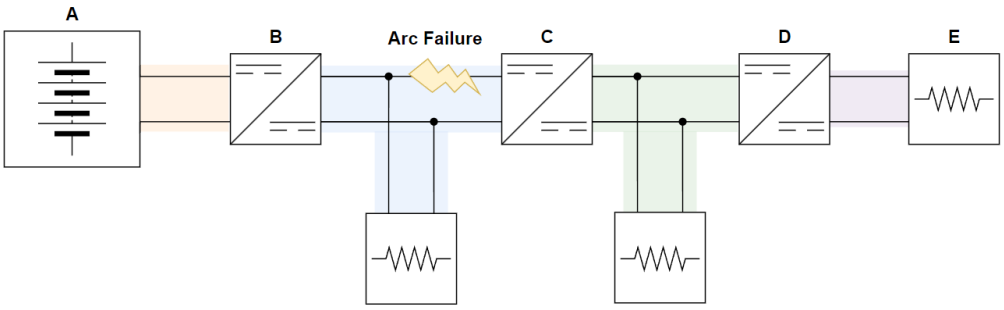


Figure 5.57: Example DC Power Distribution Network for Arc Location

Whilst this method of arc location using WFD is yet untested, it does have

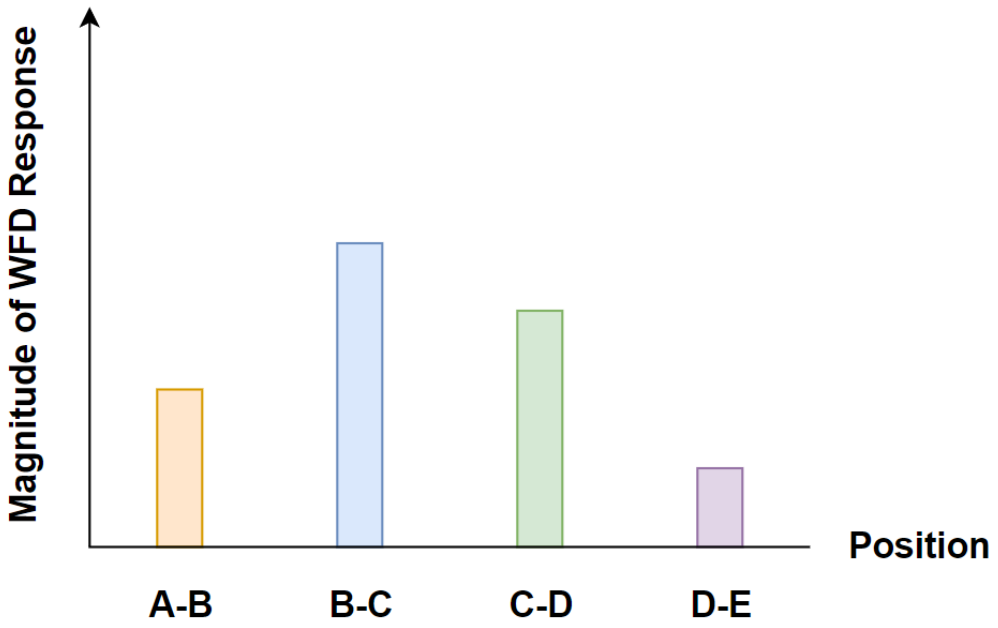


Figure 5.58: Example of Expected Distributed WFD Response to Arcing in a Larger DC Power Distribution Network

several additional merits that highlight its value as an avenue for future work. Firstly, no modification is required to the existing WFD detection method for its development as an arc location tool, as only the WFD output in its current form is required for location. Secondly, there would be no additional installation required for the arc location method to function, versus the detection method as it stands. For comprehensive arc protection, the WFD method would need to be applied to voltage measurements throughout the entirety of a power network anyway, meaning that there is already a distribution of WFD measurements across the network to utilise for fault location. As such, the future testing of the WFD method for arc location should be reasonably straightforward, producing a DC power network similar to that in Figure. 5.57, with a micro-controller monitoring voltage measurements at each circuit node; or a central larger processor continuously monitoring all points within the network (an architecture that may save on space and cost in larger networks). Arc fault generators (such as those described in Chapter. 3) can then be placed at different nodes

throughout the network and faults injected to determine the distributed response of the WFD, and by extension the position of the arc.

5.3 Chapter Conclusions & Future Work

Chapter. 5 has presented a comprehensive review of the efficacy of the WFD arc detection algorithm in detecting DC series arc failures across multiple different test criteria, including: passive load components, active load components, resistive load switching, current load switching, load step changes, loads with significant frequency content, power networks containing commercial DC-DC converters and power networks containing failing commercial DC-DC converters in a "burst-mode" mode of operation; considering both forced separation (drawn) arc ignition and forced failure arc ignition. A total of 91 experimental data captures have been analysed across all conditions, with the arc being successfully identified by the WFD detection method in each case, demonstrating a resilience to a broad range of circuit architectures and operating conditions. The WFD algorithm has demonstrated a theoretical minimum detection time of 1.5 ms from arc ignition, with practical detection times ranging from 2-8 ms from arc ignition. When compared to other methods in the literature, the WFD method has demonstrated an improvement in detection time of several milliseconds, and displayed a robustness to several load and circuit operating conditions that frequently trigger false positive detections in other methodologies [2, 22, 36, 37, 58, 59].

The results presented in this chapter have also highlighted several avenues of future work. The response of the WFD algorithm to pseudo-fractal be-

haviour presented by under-damped sinusoids has the potential to lead to false positive detections. Currently, this switching-induced pseudo-fractal behaviour occurs for only a very small time and is ignored by the WFDs threshold based detection scheme. However, this raises the concern that other longer-lived pseudo-fractal behaviour could incorrectly indicate that an arc has been detected. This can be mitigated through the exploration of applying other trigger-producing detection schemes to the base WFD calculation. Methodologies such as a leaky integration produce an output trigger in response to an increase in the averaged input value over time, and are inherently robust to sudden changes input, but due to the averaging process take longer to identify a fault. Future work investigating the influence of different detection schemes applied to the WFD could improve the overall resilience of the method to non-arcing behaviour, but would need to also characterise the impact this has on overall detection time and required computation power for online implementation. Initial conclusions presented in this chapter have also suggested that the WFD arc detection method has the potential for use as an arc location technique, wherein the magnitude of WFD response at several points within a power network can be used to identify the fault location, so long as the network architecture is known. Further study should investigate the response of the WFD algorithm to arc failures injected at several points within a much larger power network, observing how the fractal noise propagates, the effect this has on the WFD output, and use of distributed fractal magnitudes for arc location.

Chapter 6

The Effect of Ambient Temperature and Relative Humidity on DC Series Arc Behaviour and Detection

Contents

6.1 Chapter Introduction

When considering arc protection for more-electric transport applications it becomes important to consider how the changing environments these systems might operate in can affect arc behaviour, and the consequences this has for arc detection and circuit protection.

As an arc fault develops, the arc plasma that has been created can be considered a direct product of it's environment [15]. This behaviour is utilised in high-voltage switching and protection applications through the use of gas and liquid-insulated switchgear and expulsion fuses designed to either mitigate against arc failure, or extinguish ongoing arcs [76]. Despite the general understanding that arc failure is impacted by the surrounding environmental conditions very little work has been done to characterise arc behaviour in these different conditions. In their 2022 review paper, Psaras et al remark the distinct lack of formal research into how environmental conditions influence arc behaviour, and highlight a need for further work to be done [4]. Mentioned specifically in the work was that no studies had been conducted demonstrating how humidity can influence both arc behaviour and detection.

Collectively, the growth of more-electric transportation, the propensity of ambient humidity to change significantly for electric shipping and aircraft, the potential cost of arc failure within these applications (both financially and of human life), and the highlighted knowledge gap in understanding how arc failure can be influenced by relative humidity indicate a strong use case for research in this field.

The following chapter covers a series of experiments intended to demonstrate the efficacy of the described WFD arc fault detection algorithm on a range of DC series arc failures at different ambient temperatures and relative humidities, whilst considering the implications this might have on DC series arc formation, burning and behaviour in these environments. Directly following on from the earlier work by the author described in [27], the work presented in this chapter covers the application of the WFD arc detection algorithm to DC arc failures at relative humidities of 20-90% at 20° C, 40° C, 80° C and 100° C respectively. This allows for comparison between different fixed temperature operating conditions and whilst providing further validation of results published separately in [27] (and included in this thesis in Appendix A).

The author would like to make clear that despite their similarity, the results presented in this chapter and the data published in [27] cannot be included in the same comparison. Due to constraints on the use and supply of equipment necessary to conduct the described experiments, both tests were conducted several months apart, and using slightly different electrode materials. Because of the substantial influence of electrode material and geometry on arc generation, the decision was made to separate the two sets of experimental results, however comparisons can still be made between the trends shown in each case [15, 75, 76].

6.1.1 Generation of DC Series Arcs at Fixed Temperature and Humidity

To reproduce DC series arcs consistently as environmental conditions were varied the forced failure (drawn) arc generator seen in Figure. 3.1 and described in Chapter. 3 was placed within a Xi'an LIB THR10-150C environment chamber capable of controlling and monitoring both internal temperature and Relative Humidity (RH) to a precision of 0.1°C and 2.5% RH. It is noteworthy here that relative humidity is temperature dependant, (with 100% RH at higher temperatures representing a greater amount stored air moisture than 100% at lower temperatures) and that for each experiment the operating temperature was fixed first, before setting the relative humidity of the chamber and allowing the experiment to run. For each experiment, the Xi'an Lib chamber calculates relative humidity at each temperature setpoint using the temperature difference between both a dry-bulb, and a wet bulb thermocouples internal to the chamber, forming a psychrometer. Under normal conditions, evaporation of water from the wet-bulb thermocouple results in a lower measured temperature versus the dry bulb. As relative humidity increases, the rate of evaporation reduces as the air can hold less moisture, leading to both the wet and dry bulb thermocouples showing an equal temperature at 100% RH. Using preprogrammed information from the machine calibration, the chamber can then calculate the internal relative humidity by comparing the wet and dry bulb temperatures.

As shown in Figure. 6.1, the arc generator was connected to a 400V DC supply. To ensure consistency between experiments, the arc generator and supply were connected in series to a 42Ω load resistance and a 15.2mH

inductor forming a component of the load, included to emulate the cable inductance of long, lower wire-gauge transmission lines within these systems and other inductive effects within the system. The load was comprised of passive components to avoid the influence of switching behaviour introduced using some programmable loads on the arc that may occlude or interfere with changes caused by environmental effects.

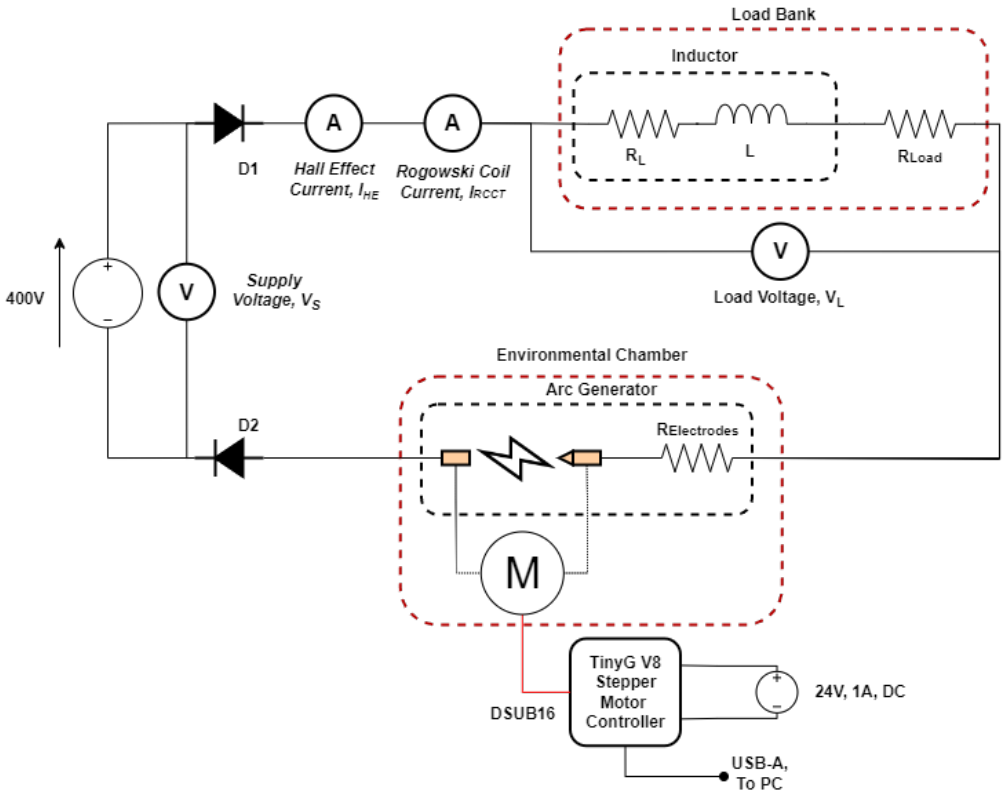


Figure 6.1: Forced Separation Arc Generation Circuit Diagram with Humidity Chamber

For this series of experiments, the arc generator was fitted with 2mm diameter tungsten electrodes, with the higher electrical potential electrode being ground longitudinally to a point, leaving the lower (zero) potential electrode flat, as shown previously in Figure. 3.2 in Chapter. 6. Electrodes were cleaned of oxide and re-ground between experiments to maintain their geometry, as this has been shown to influence arc generation, and should

be kept as consistent as possible between experiments [4, 15, 84].

To achieve arc ignition, a forced separation arc ignition method was employed. Electrodes are initially in contact to allow continuous current flow, and begin separating at a constant speed of 2mm/s after two seconds has elapsed. When the electrodes separate, the arc forms and continues to grow with electrode separation. Once the electrode separation becomes sufficiently large, the arc collapses and the individual experiment ends after 15 s. Each test records both supply and load voltage measurements using differential voltage probes, alongside two measurement of series current using both a Rowgowski coil current transducer (RCCT) and a hall-effect (HE) current probe, sampled at 2MHz with a Picoscope 5000 Series Oscilloscope.

For all experiments recorded in this chapter, arc ignition was achieved though forced separation of the electrodes as arc ignition can be more reliably achieved and controlled. Similarly, this allowed for the recording of electrode separation, giving an indication of the possible minimum arc length, and allowing for comparisons between the minimum possible size of the arc and other recorded variables, as discussed later in this chapter.

Table 6.1: Table of Measurements for DC Series Arcs in Changing Environmental Conditions

Measurand	**Unit**	**Precision**	**Variable Type**
Supply Voltage	[V]	1:1000	Dependant
Load Voltage	[V]	1:1000	Dependant
Hall-Effect Current	[A]	1:100	Dependant
Rogowski Coil Current	[A/s]	1:1000	Dependant
Ambient Temperature	[°C]	0.1	Independent/Control*
Relative Humidity	No Units	2.5%	Independent
Load Resistance	[Ω]	0.001	Control
Load Inductance	[H]	0.05	Control

Table. 6.1 is provided as a reference, recording all the variables captured during these experiments:

* Ambient Temperature is held constant as a control variable for individual 20-98% sets of humidity sweeps, but is an independent variable between sets of experiments at different temperatures.

6.2 Multiple Temperature Humidity Sweep: DC Series Arc Failure at 20°C, 40°C, 80°C and 100°C and 20-98% RH

The work documented in this sub-chapter directly follows on from the study performed in [27]. Here, DC series arcs are produced at relative humidities of 20-98% in steps of 10% for fixed ambient temperatures of 20°C, 40°C, 80°C and 100°C using the previously described Xi'an LIB THR10-150C environment chamber. The WFD arc detection algorithm described in Chapters. 4 and 5 is applied to arc load voltage waveforms under all environmental conditions tested to determine both the impact these new conditions have on fault detection, as well as to further test the efficacy of the detection method itself. Additionally, general trends observed between arc faults at different relative humidities and temperatures are highlighted.

To reiterate the earlier point regarding the difference in electrode materials, note that in this section whilst the experimental method is the same as in [27], due to constraints on the supply of equipment, both tests were conducted using slightly different electrode materials, both tungsten though of

a marginally different alloy and from different manufacturers. This oversight was not noticed until after experimental work had long since concluded, and because of the handover of laboratory space and equipment, could not be accounted for with an additional set of experiments before the submission of this thesis. Because of the differences in electrode material and the effect that this has on arc behaviour, a comparison cannot be directly made between the results in [27] and those presented here [15, 75]. Despite the lack of direct comparison, the trends seen in both sets of experiments can will be compared and contrasted to draw meaningful conclusions from both studies.

6.2.1 DC Series Arcs Failure at 20°C, 40°C, 80°C and 100°C and 20-98% RH

In this study, the methodology described in Chapter 6.1 was repeated at different fixed temperature values, to determine the effect this had on arc behaviour and to allow for the testing of the effect of relative humidity at different temperatures, and by extension, levels of air saturation. The Xi'an LIB environment chamber was set to 20°C, 40°C, 80°C and 100°C in turn, and was swept through the full range of relative humidities within it's capability. At each fixed temperature, relative humidity was initially set to 20% and increased by 10% after a set of five individual arc failures were recorded, up to the final humidity set-point of >98%. The result is 45 records of DC series arc failure for each fixed temperature tested, spanning the full humidity range of 20-98% RH, for a total of 180 arc failures captured. For brevity, and given the volume of traces to analyse, representative results from each set of experiments are displayed and discussed together. Shown in Figures. 6.2, 6.3, 6.4 and 6.5 that follow are load volt-

age traces at 20%, 60% and 98% relative humidity for the 20°C, 40°C, 80°C and 100°C fixed ambient temperatures to allow for qualitative comparison of the arc behaviour across both increasing temperature and humidity. Also included are Tables. 6.2, 6.3, 6.4 and 6.5, highlighting key metrics captured from each set of experiments, with the average value taken across all five arc traces captured at each individual fixed temperature and humidity set-point to allow for additional quantitative analysis. In these tables the peak arc impedance is determined at the time of arc collapse from division of the arc voltage (found through application of Kirchoff's laws to Figure. 6.1) by series current.

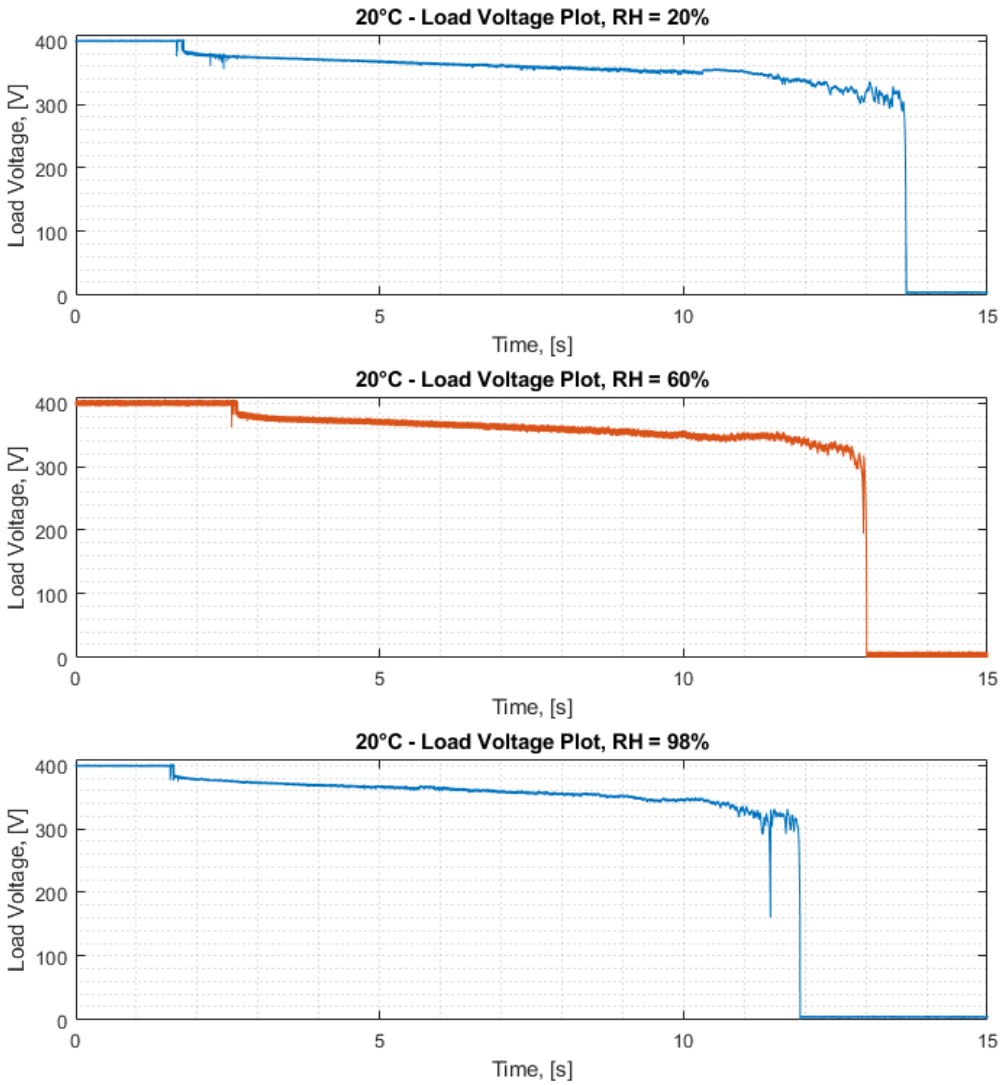


Figure 6.2: Comparison of Load Voltage at 20%, 60% and 98% RH for a 20°C Temperature Setpoint

Table 6.2: Table of Key Metrics for DC Series Arcs at 20°C

Relative Humidity, [%]	**Arc Duration, [s]**	**Electrode Separation, [mm]**	**Peak Arc Impedance, [Ω]**	**Change in WFD at Arc Ignition, [%]**
20	11.60	23.19	25.19	19.15
30	10.29	20.59	24.14	19.15
40	10.41	20.82	29.66	18.72
50	10.14	20.28	22.73	18.55
60	10.67	21.34	30.94	18.32
70	10.19	20.39	28.28	19.71
80	10.26	20.53	29.31	18.76
90	10.23	20.45	34.10	18.52
98	9.89	19.78	35.52	18.29
Average	10.41	20.82	28.87	18.80

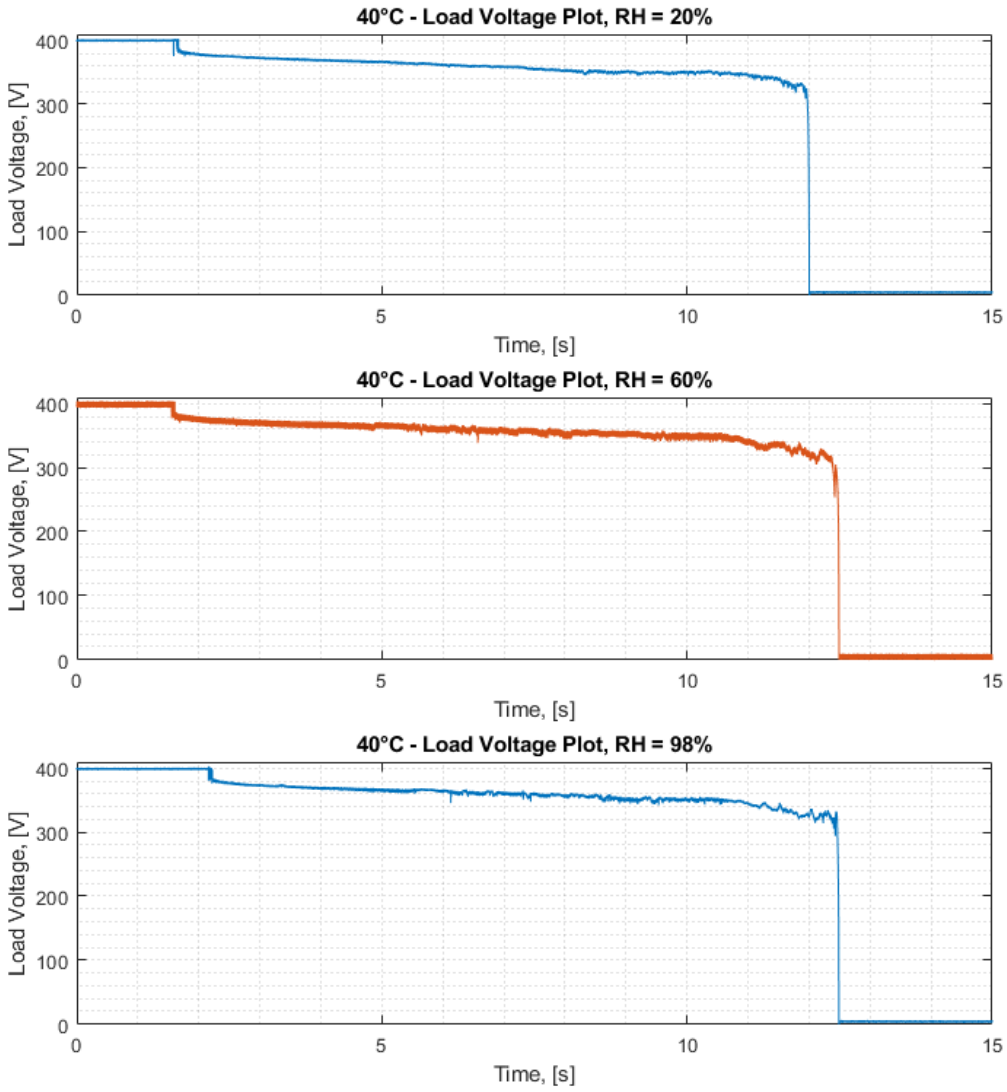


Figure 6.3: Comparison of Load Voltage at 20%, 60% and 98% RH for a 40°C Temperature Setpoint

Table 6.3: Table of Key Metrics for DC Series Arcs at 40°C

Relative Humidity, [%]	**Arc Duration, [s]**	**Electrode Separation, [mm]**	**Peak Arc Impedance, [Ω]**	**Change in WFD at Arc Ignition, [%]**
20	10.39	20.79	26.55	19.10
30	9.95	19.91	33.79	19.10
40	10.43	20.86	24.48	18.52
50	9.85	19.71	30.35	18.76
60	10.14	20.29	35.82	17.82
70	10.39	20.77	32.55	19.23
80	10.24	20.49	38.62	18.96
90	10.64	21.29	35.54	18.76
98	10.49	20.98	36.89	19.95
Average	10.28	20.56	32.73	18.91

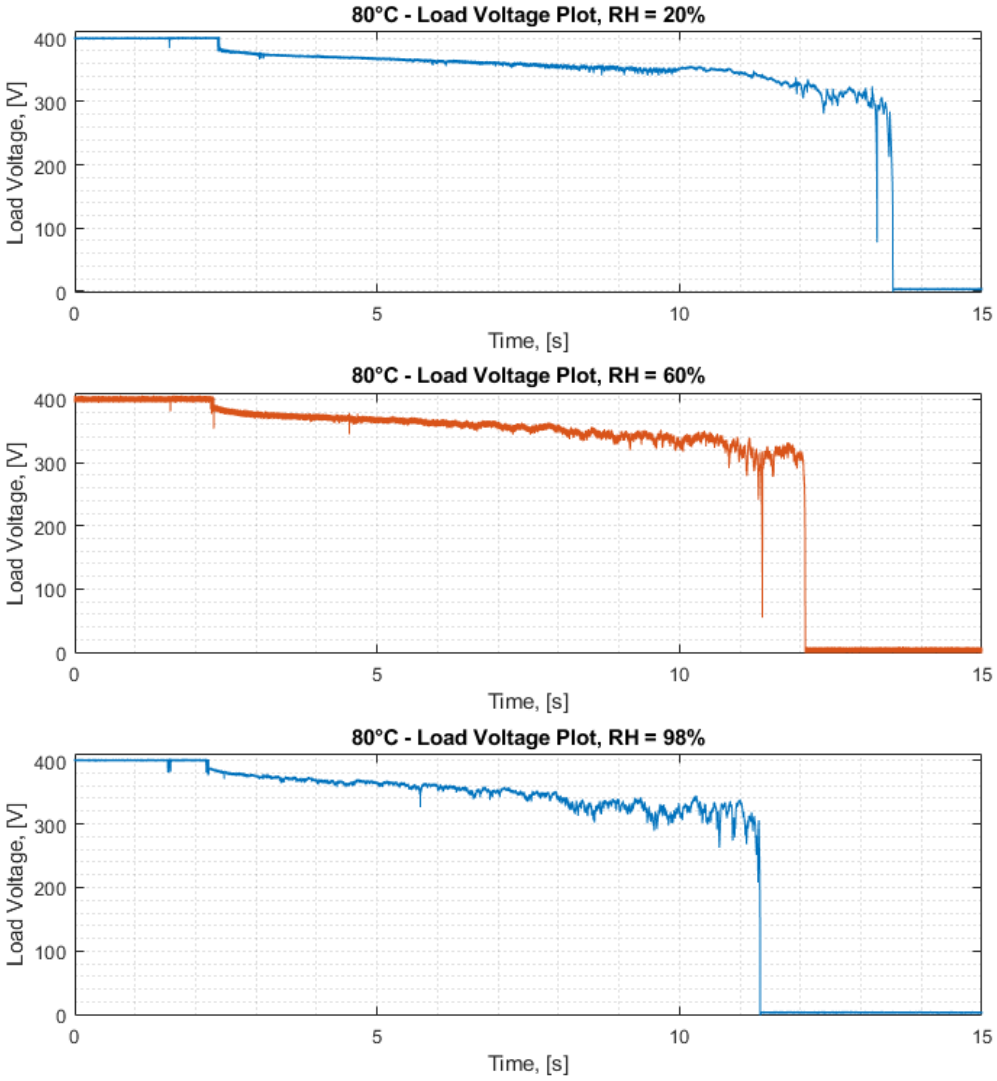


Figure 6.4: Comparison of Load Voltage at 20%, 60% and 98% RH for a 80°C Temperature Setpoint

Table 6.4: Table of Key Metrics for DC Series Arcs at 80°C

Relative Humidity, [%]	**Arc Duration, [s]**	**Electrode Separation, [mm]**	**Peak Arc Impedance, [Ω]**	**Change in WFD at Arc Ignition, [%]**
20	10.44	20.88	34.82	20.14
30	10.71	21.42	35.19	20.14
40	10.28	20.57	35.17	18.48
50	9.89	19.77	26.90	19.90
60	10.05	20.11	31.38	18.01
70	9.94	19.88	39.18	18.48
80	10.08	20.17	43.10	19.86
90	9.64	19.27	37.93	18.20
98	9.54	19.08	40.34	19.15
Average	10.06	20.13	36.00	19.15

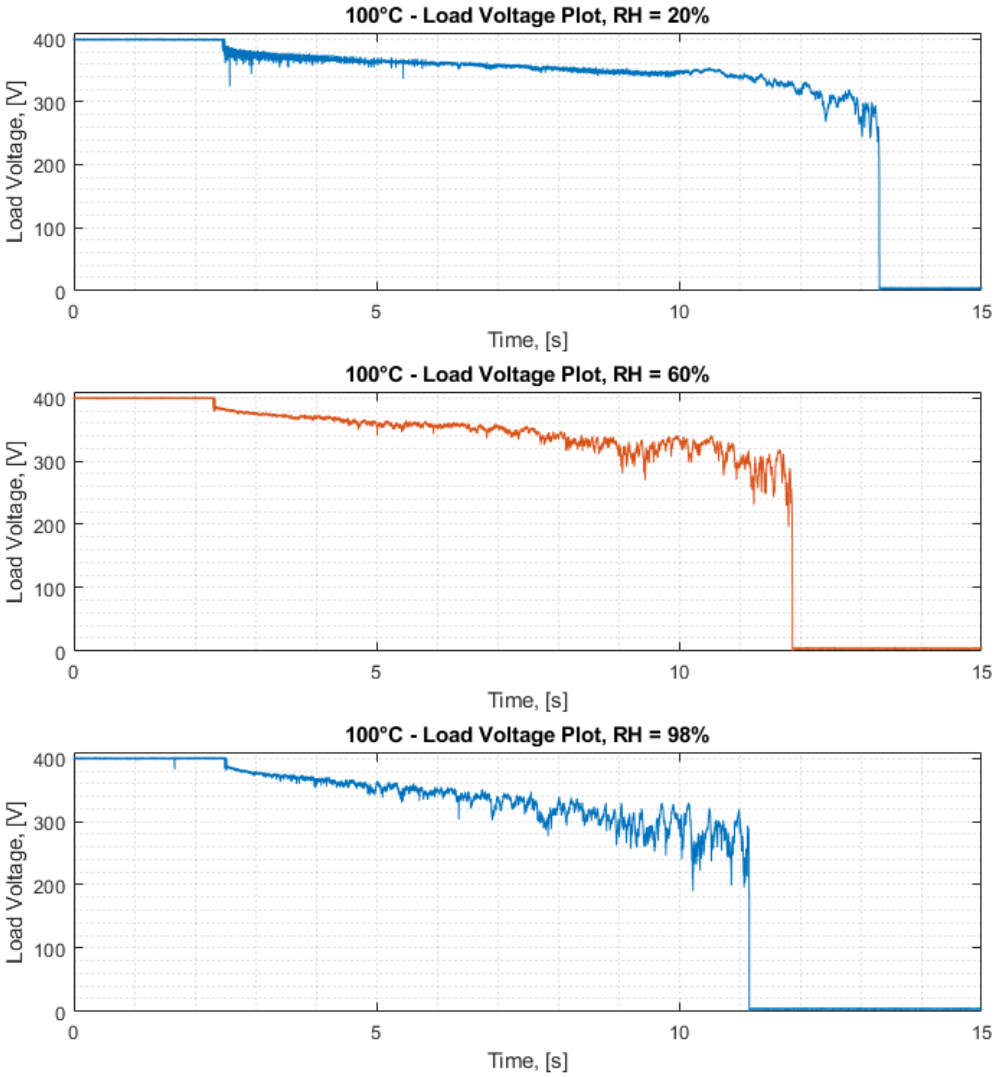


Figure 6.5: Comparison of Load Voltage at 20%, 60% and 98% RH for a 100°C Temperature Setpoint

Table 6.5: Table of Key Metrics for DC Series Arcs at 100°C

Relative Humidity, [%]	**Arc Duration, [s]**	**Electrode Separation, [mm]**	**Peak Arc Impedance, [Ω]**	**Change in WFD at Arc Ignition, [%]**
20	10.57	21.14	40.35	19.91
30	10.52	21.04	48.62	19.91
40	9.92	19.83	40.35	19.67
50	9.69	19.38	48.97	17.77
60	9.38	18.75	37.93	20.14
70	9.45	18.90	48.28	17.30
80	9.10	18.21	40.34	20.14
90	9.22	18.44	53.45	20.14
98	8.99	17.97	42.41	20.38
Average	9.65	19.30	44.52	19.48

Initial inspection of the arc fault traces shows several key trends similar to those described in [27], the first of which is the reduction in arc duration with increasing relative humidity for the 20°C, 80°C and 100°C traces shown in Figs. 6.2, 6.4 and 6.5 respectively. The reduction in arc duration with increasing humidity is consistent across all data captures for each of the 20°C, 80°C and 100°C. This is not the case however for the 40°C arc traces shown in Figure. 6.3, wherein arc duration remained approximately constant with relative humidity, as can also be observed in when looking at the averaged arc duration for each RH value in Table. 6.3. At this time it is unclear whether the consistent arc duration seen in 40°C results is anomalous, or whether there is a specific influence on arc behaviour at an ambient temperature of 40°C. Plotting the arc duration versus relative humidity for the 20°C, 40°C, 80°C and 100°C temperatures on the same figure, as shown in Figure. 6.6 demonstrates these features, showing clearly the reduction in arc duration with increasing RH for the 20°C, 80°C and 100°C results, whilst highlighting the disparity of the 40°C results. Note that due to time constraints on use of the equipment, the 40°C results could not be repeated to verify the differences seen, however efforts should be made to produce repeat experiments for verification in future work.

Average arc duration can also be observed to reduce with increasing temperature from inspection of Figure. 6.6 where curves representing higher ambient temperature sit lower in the figure, corresponding to a reduced arc duration (discounting for now the results at 40°C). Figure. 6.7 further highlights this trend, plotting the arc duration at all relative humidities at their temperature set points in a box and whisker chart, clearly showing a decrease in both average and outlier arc duration for increasing ambient temperature.

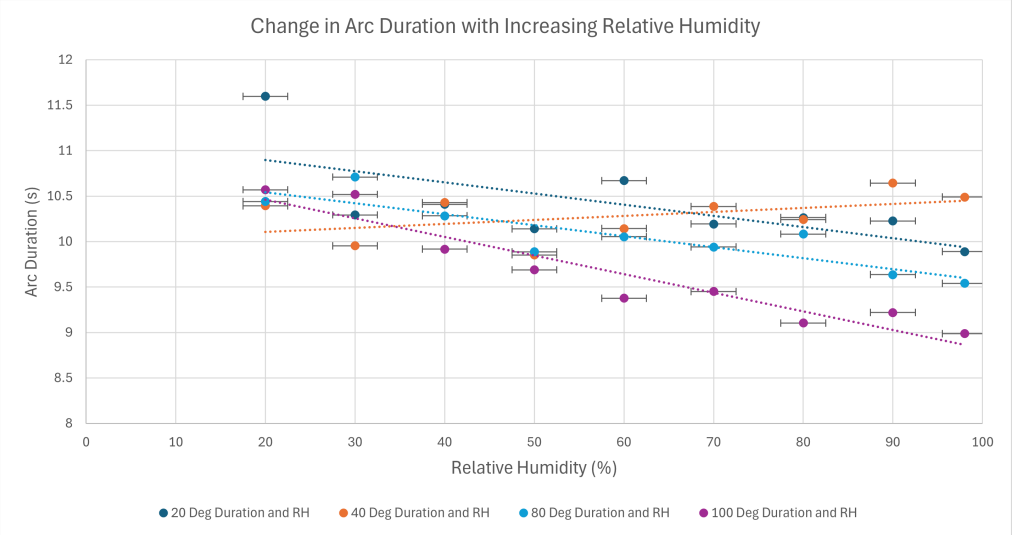


Figure 6.6: Variation in Arc Duration with Increasing Relative Humidity at 20°C, 40°C, 80°C and 100°C

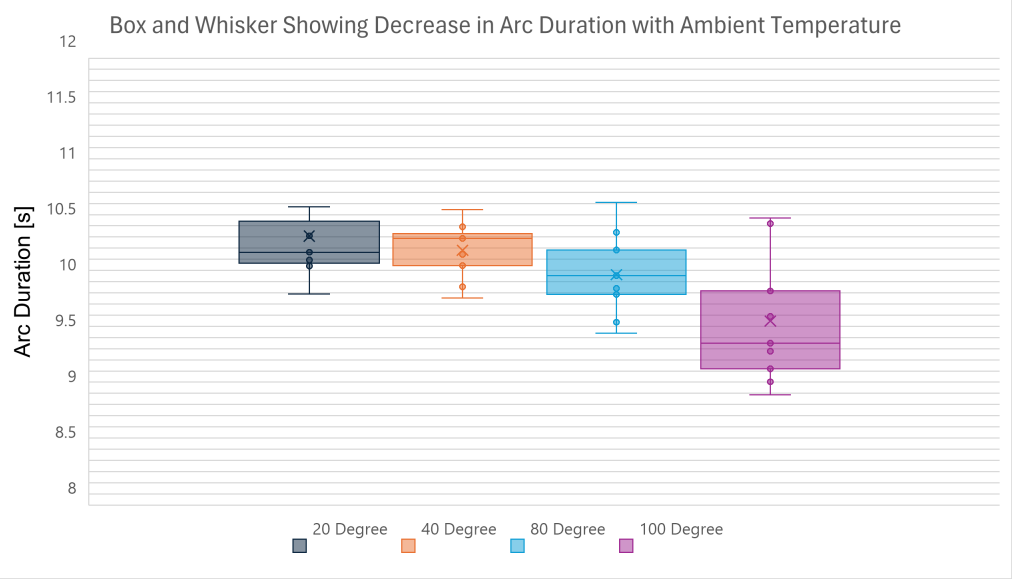


Figure 6.7: Distribution of Average Arc Duration with Increasing Fixed Ambient Temperature for 20->98% Relative Humidity

Whilst the difference in arc duration of 0.76 s seen as fixed temperature increases from 20°C to 100° from Tables. 6.2 to 6.5 may seem unremarkable and innocuous at first, it is worth considering that arc fault detection is designed to operate on the millisecond scale, as it takes only fractions of a second for an arc to short adjacent conductors and destroy them, or

ignite adjacent material and start an electrical fire [1, 6, 13, 14, 15, 16, 17]. As described earlier in Chapter. 3, and highlighted in Figure. 3.5, for a forced separation arc the passage of time also represents an increase in the separation of the arc electrodes and by extension the minimum arc length. Hence, due to the constant separation speed of the electrodes used in these experiments, the 0.76 s also corresponds to a 1.52 mm reduction in electrode separation and minimum arc length between the arc failures at 20°C and 100°. This means that the 20°C arcs can travel further and potentially short conductors or ignite flammables at a greater distance from the site of their initial fault. As such, these results suggest that arcs at a lower ambient temperature would therefore pose more of a threat to system reliability than arcs present at a higher ambient temperature, and that the operating temperature of DC circuit architecture should be considered when arc fault protection is designed and commissioned. Not considered however is how this behaviour may change at zero and sub-zero temperatures, alongside at very low (20%-0%) relative humidities. These conditions were not tested due to equipment limitations, but should be considered for future work.

Furthermore, also observable in Tables. 6.2, 6.3, 6.4 and 6.5 is that the overall average arc duration at 40°C once again starts to correlate with the other tested temperatures and humidities, showing an averaged arc duration of 10.28s: lower than the 10.41s result at 20°C, but larger than the 10.06s result at 80°C. This provides an indication that whilst the duration of the 40°C arc traces does not scale with humidity as expected, it does scale with temperature, and that future work should consider more repeat experiments at temperatures around 40°C, capturing more individual repeat arc failures at each humidity to determine whether the observed increase in arc duration is truly anomalous.

It can also be seen in Figs. 6.2, 6.3, 6.4 and 6.5 that across all tested temperatures there is an increase in arc transient behaviour with increasing relative humidity, matching that seen previously in [27]. These transient effects are seen to increase in magnitude and frequency later in the arc waveform after ~10s when the arc nears collapse. Transient behaviour is also seen to vary with fixed temperature, increasing in magnitude and beginning sooner in the arc at higher temperatures. This may possibly be the result of increased arc impedance seen at higher temperature setpoints as can be seen in Tables 6.2 - 6.5 and in Figure. 6.8 wherein arc impedance at arc collapse is plotted at all recorded relative humidities for each fixed temperature. In Figure. 6.8, it becomes clear that there is not only an increase in mean arc impedance, but an increase in arc impedance generally irrespective of relative humidity as ambient temperature increases.

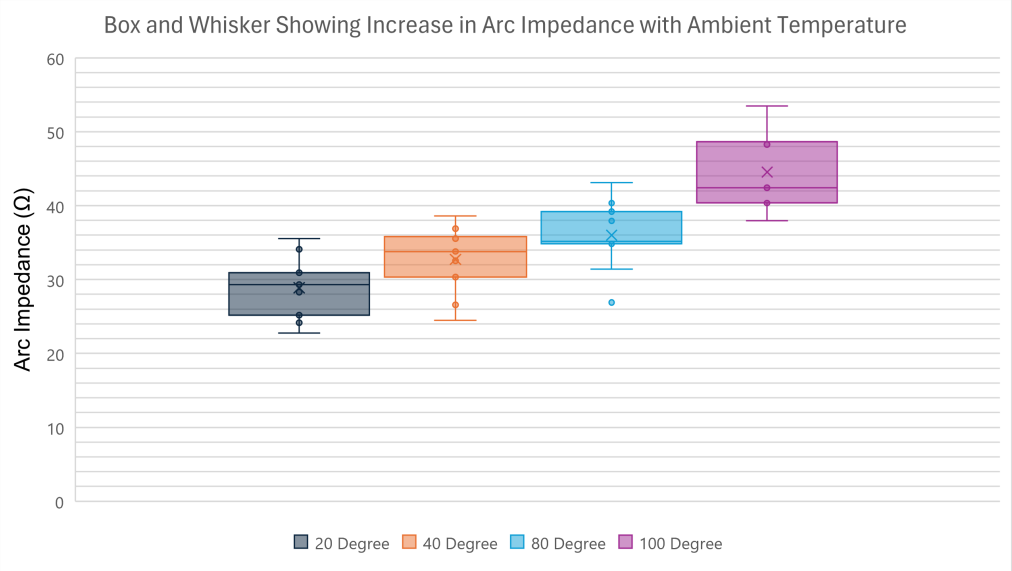


Figure 6.8: Distribution of Average Peak Arc Impedance with Increasing Fixed Ambient Temperature for 20->98% Relative Humidity

The full effect of increasing arc transient behaviour at higher temperatures and relative humidities can be seen in the four, three-dimensional plots

highlighted in Figures. 6.9, 6.10, 6.11 and 6.12; each showing nine arcing load voltage traces, one for each relative humidity tested across all four ambient temperatures tested. Comparison both between individual results within a single figure, and between figures themselves shows how arc transient behaviour increases in magnitude and time-frequency with both increasing relative humidity and increasing ambient temperature. Together, these outcomes indicate a clear difference in arcing behaviour between cold and dry environmental conditions, when compared to warm and wet environmental conditions, and indicate that the operating environment of electrical equipment should be a serious consideration when designing protection against arc failure and arc flash hazards.

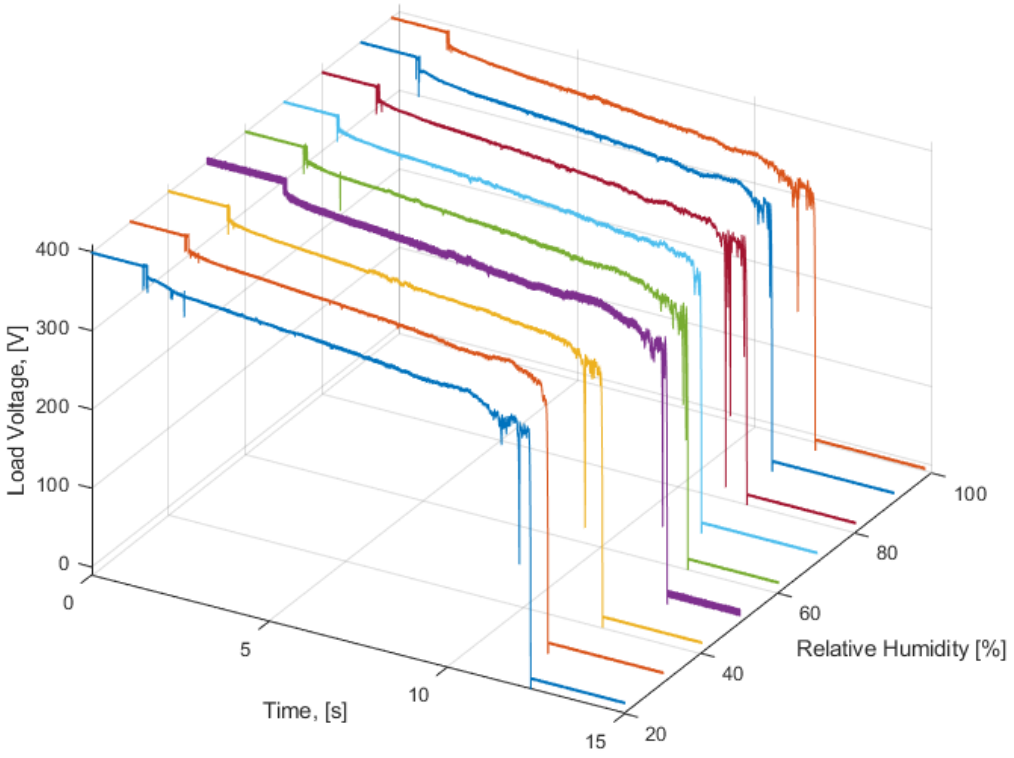


Figure 6.9: 3-D Plot of Nine Arcing Load Voltage Versus Time Traces against Relative Humidity at 20°C

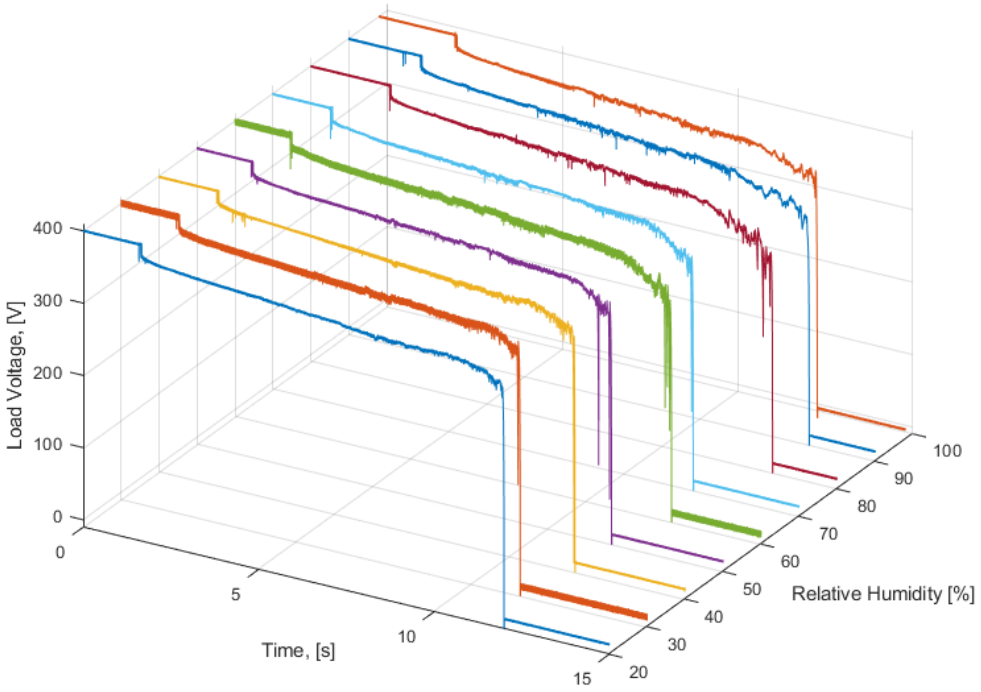


Figure 6.10: 3-D Plot of Nine Arcing Load Voltage Versus Time Traces against Relative Humidity at 40°C

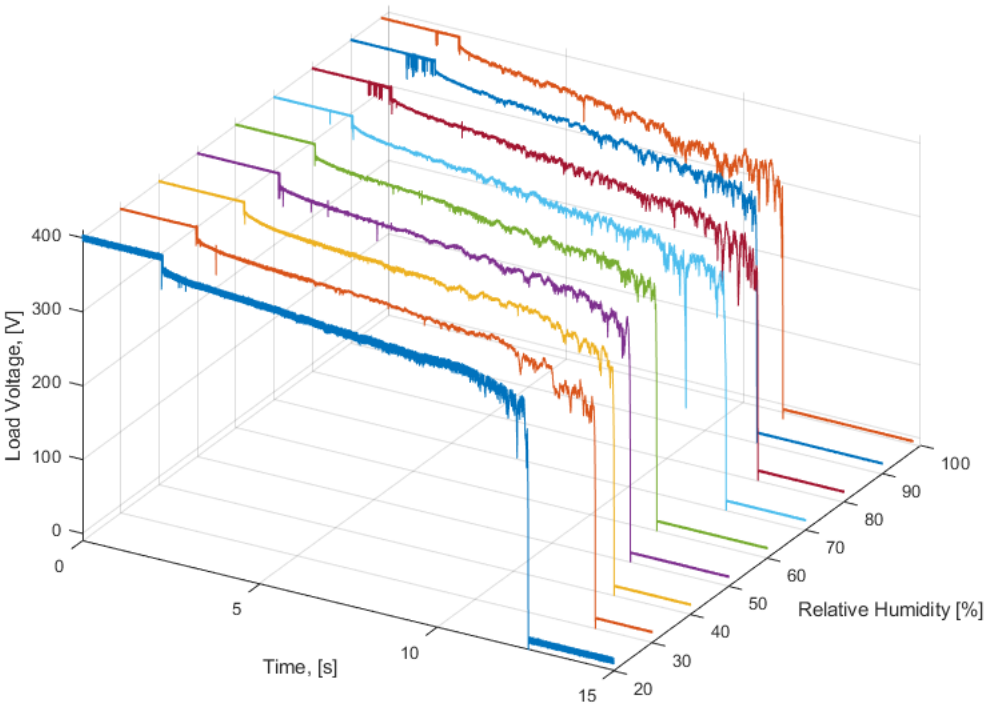


Figure 6.11: 3-D Plot of Nine Arcing Load Voltage Versus Time Traces against Relative Humidity at 80°C

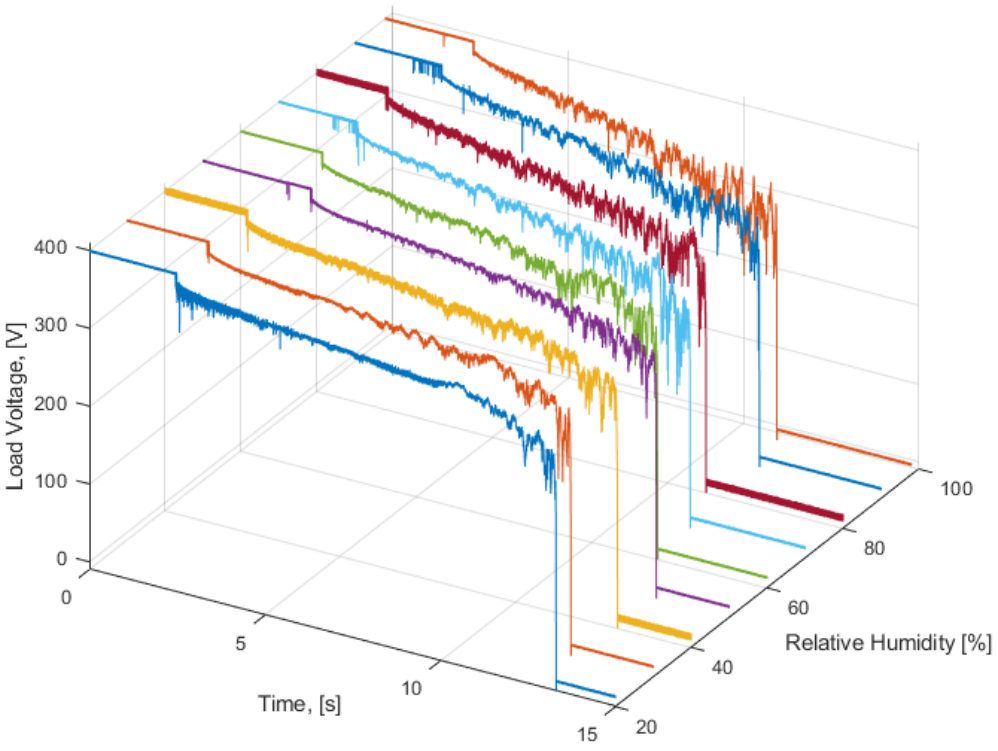


Figure 6.12: 3-D Plot of Nine Arcing Load Voltage Versus Time Traces against Relative Humidity at 100°C

6.2.2 DC Series Arc Detection using Windowed Fractal Dimension at 20°C, 40°C, 80°C and 100°C for 20-98% RH

Earlier results have highlighted the increased magnitude, frequency and duration of arc transient features with both increasing relative humidity and ambient temperature that could prove beneficial to arc detection. Repeating the methodology in [27], arc fault traces at 20°C, 40°C, 80°C and 100°C were passed through the Windowed Fractal Dimension arc detection method described in Chapters 4, 5 and in [1]. Figures. 6.13-6.20 below show the traces of load voltage, load voltage WFD and a binary output trigger at the point of arc detection, for arc faults at 20% and >98% RH at each temperature set point.

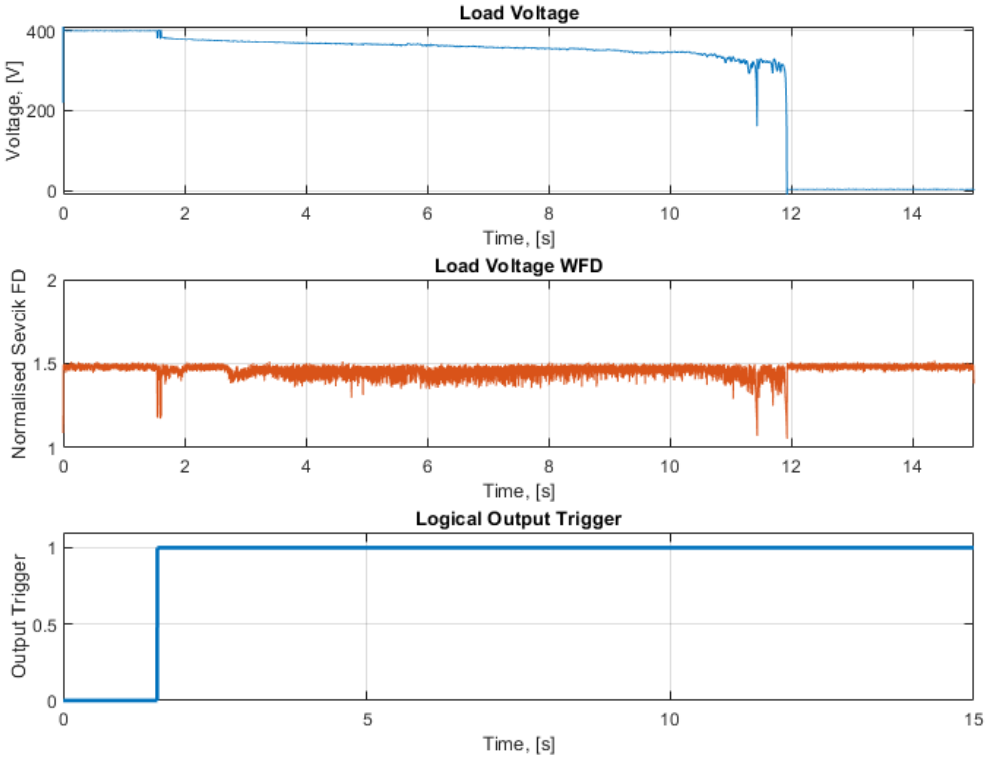


Figure 6.13: Arc Detection using WFD of Arc Load Voltage Waveform at 20% RH at 20°C Ambient Temperature

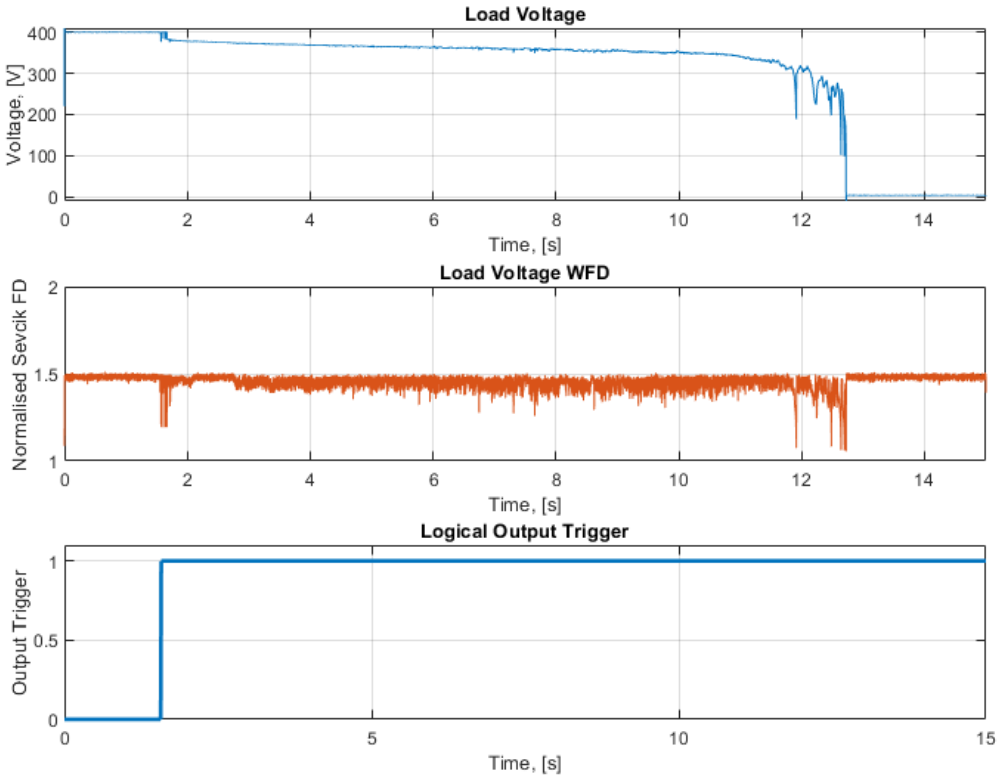


Figure 6.14: Arc Detection using WFD of Arc Load Voltage Waveform at 98% RH at 20°C Ambient Temperature

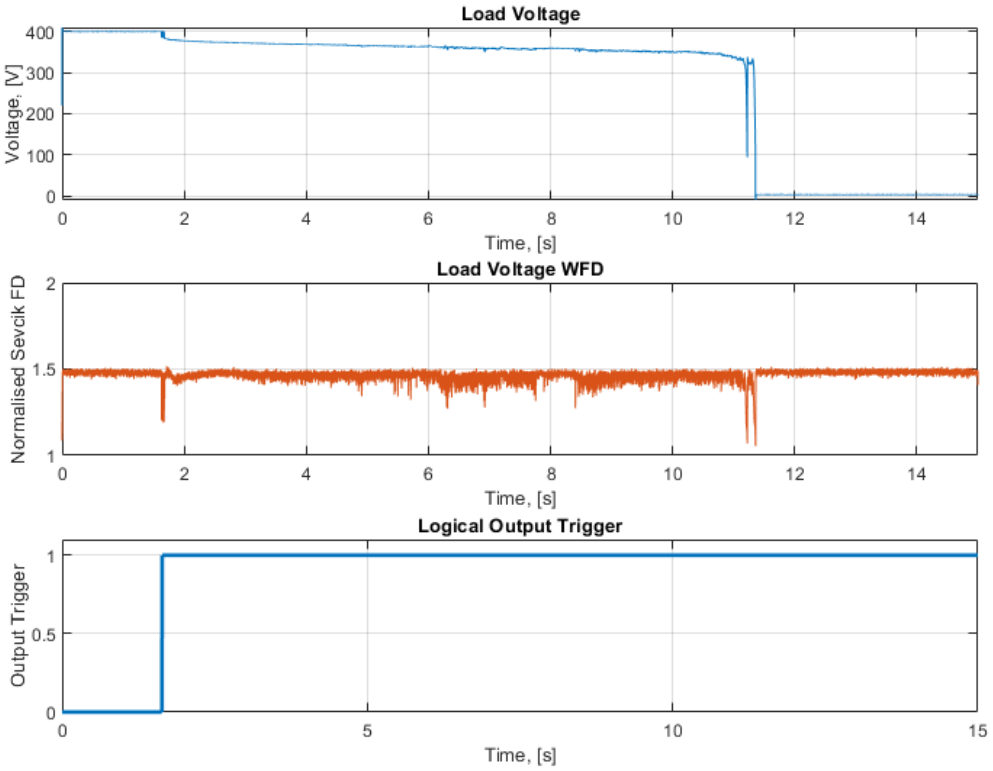


Figure 6.15: Arc Detection using WFD of Arc Load Voltage Waveform at 20% RH at 40°C Ambient Temperature

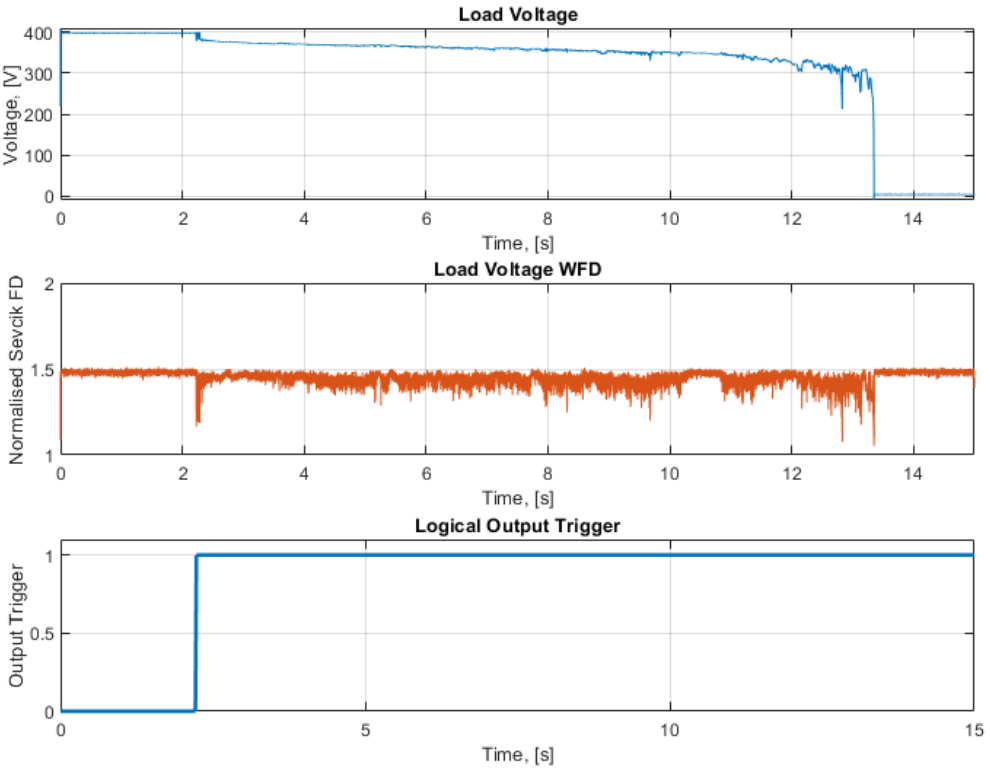


Figure 6.16: Arc Detection using WFD of Arc Load Voltage Waveform at 98% RH at 40°C Ambient Temperature

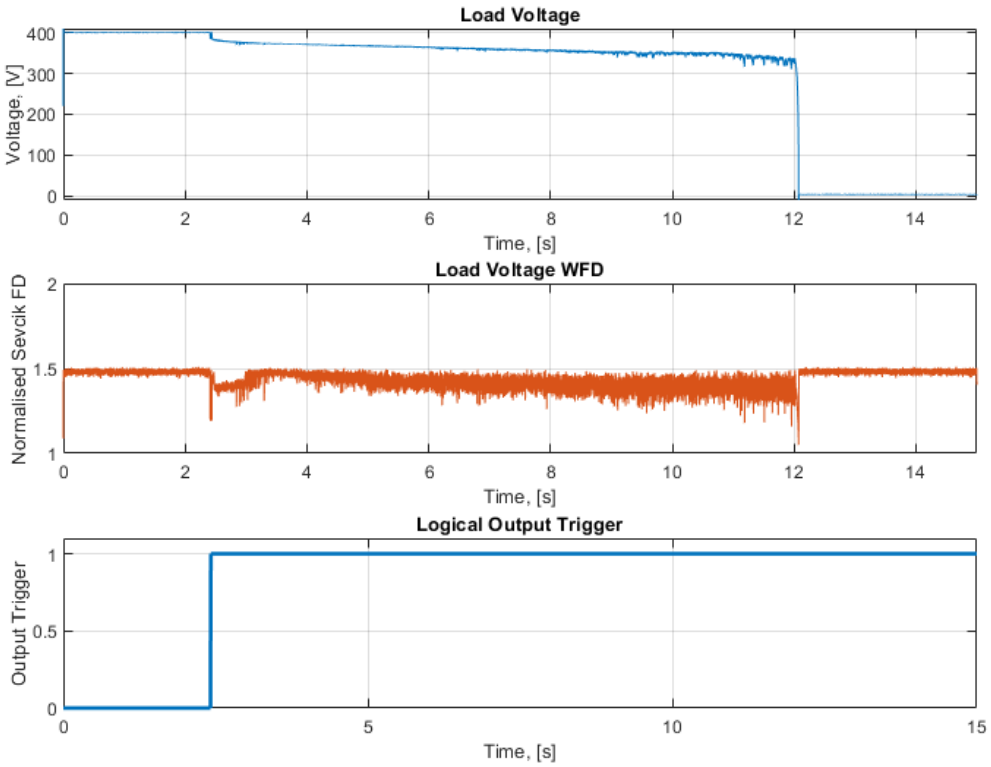


Figure 6.17: Arc Detection using WFD of Arc Load Voltage Waveform at 20% RH at 80°C Ambient Temperature

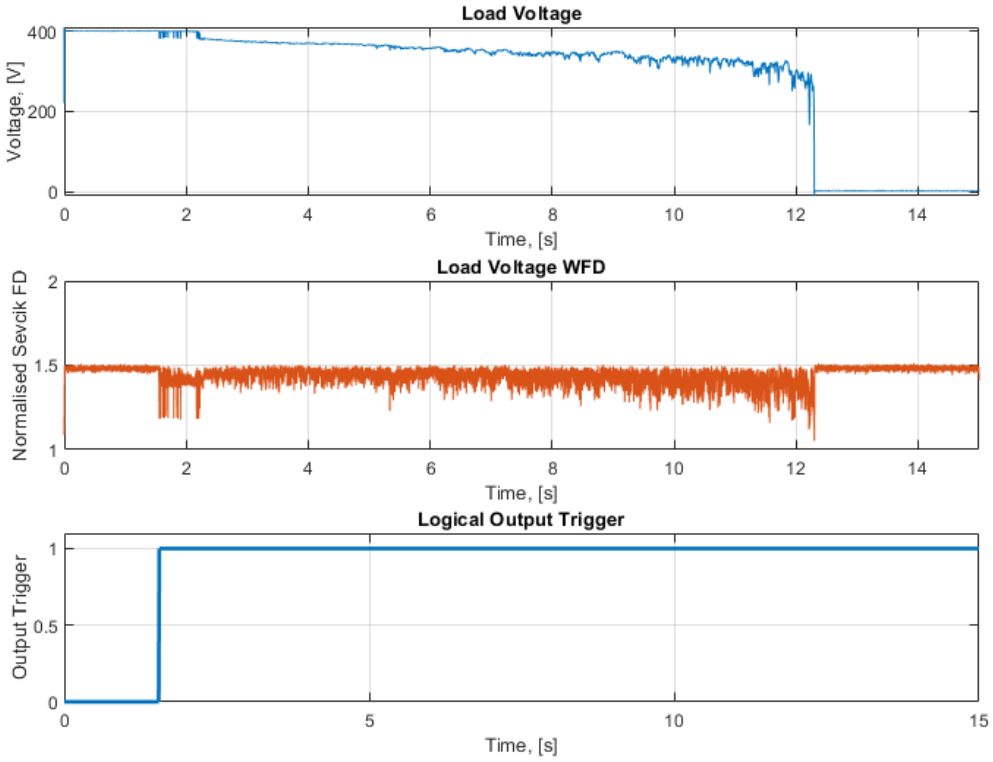


Figure 6.18: Arc Detection using WFD of Arc Load Voltage Waveform at 98% RH at 80°C Ambient Temperature

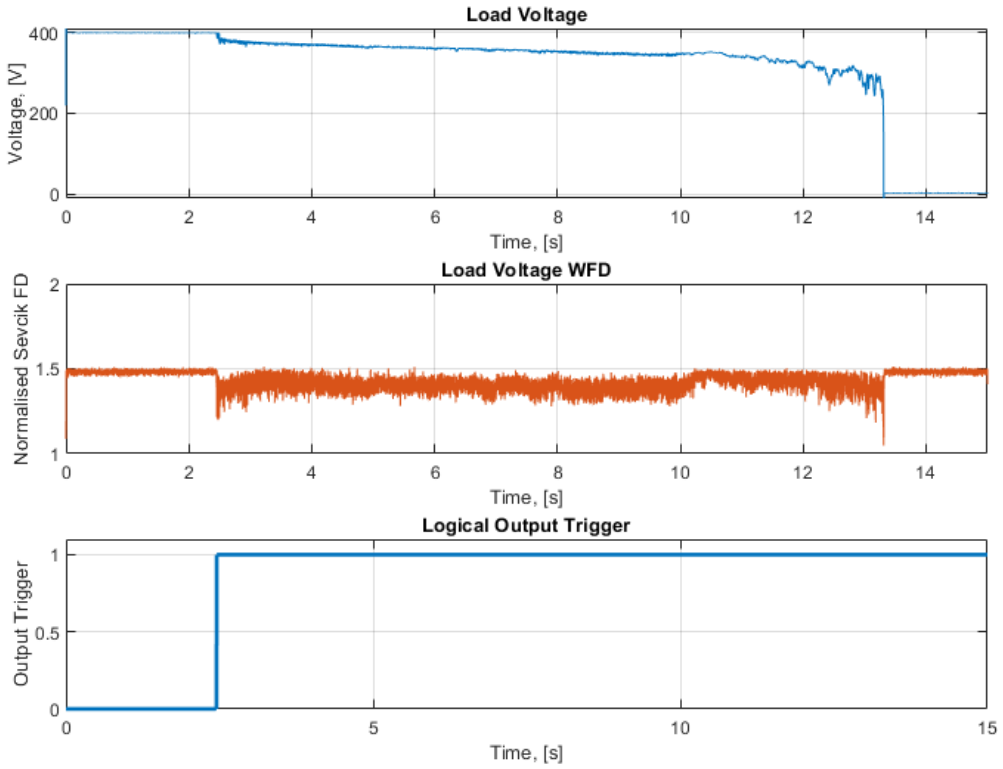


Figure 6.19: Arc Detection using WFD of Arc Load Voltage Waveform at 20% RH at 100°C Ambient Temperature

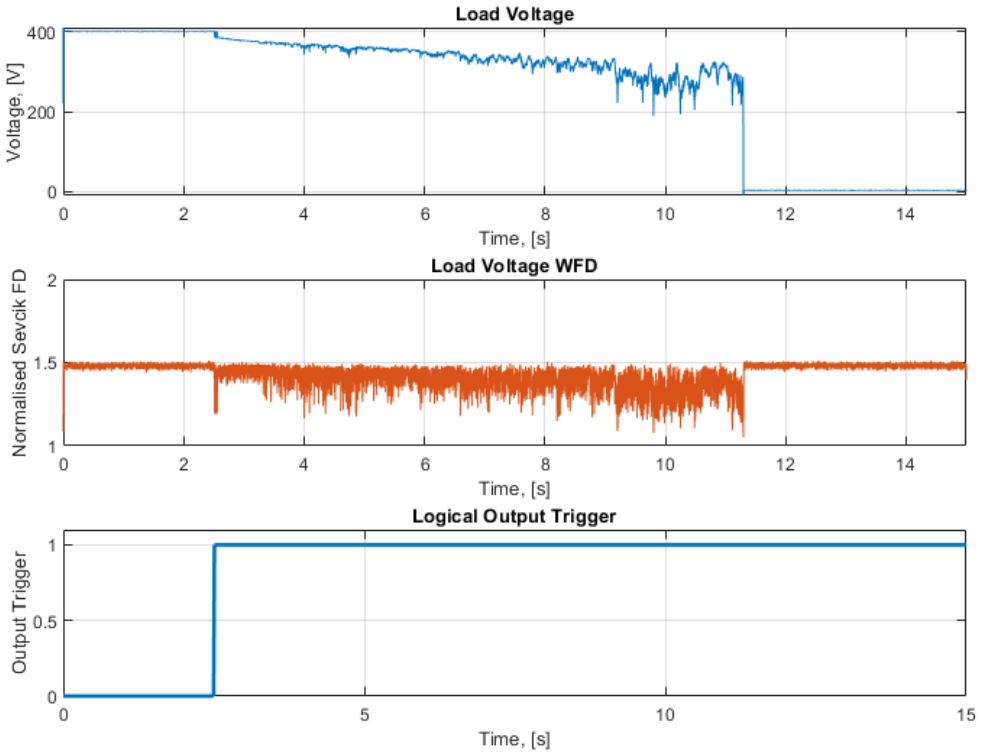


Figure 6.20: Arc Detection using WFD of Arc Load Voltage Waveform at 98% RH at 100°C Ambient Temperature

In Figures. 6.13-6.20 the magnitude of the load voltage WFD increases with increasing arc duration and arc transient behaviour, particularly as the arc duration increases and the arc nears collapse. For each trace the increase in transient behaviour at greater arc duration is indicative of a greater arc length as the electrode separation increases, and by extension leads to an increased arc impedance as previously discussed. The increased arc impedance has a greater effect on the load voltage traces, with smaller and more frequent changes in arc length now producing bigger changes in load voltage, leading to the arc behaviour being more heavily superimposed onto the load voltage waveform. As the WFD detection method highlights fractal noise in the load voltage waveform inherent to the arc, the increase in WFD response seen at greater arc duration can be attributed to the increased arc impedance and therefore superimposed arc noise on the load voltage. This is consistent across all other WFD traces and provides quantitative evidence that arc fault detection becomes easier at higher arc impedance and arc length, a result that cannot be understated for the more common impedance-based arc fault detection techniques. However, as arc detection is required in the first few milli-seconds of arc ignition, it is unlikely that the increased detectability with greater arc duration will be of any practical use in arc-fault circuit interruption.

It can also be seen in Figs. 6.13 - 6.20 that the magnitude of the change in WFD output increases at greater relative humidity, irrespective of fixed temperature. In each of the traces shown, the WFD output for during the arc burning phase (after ignition) is seen to increase in magnitude, and is more easily distinguished from both pre-arc and post-arc behaviour. This is again likely due to the increase in arc behaviour reflected on the load voltage waveform due to the increased arc impedance seen at higher relative

humidity, for a fixed temperature as indicated earlier in Tables. 6.2, 6.3, 6.4 and 6.5. The increase in WFD output with increasing relative humidity matches the results discussed previously recorded in [27] and provides supports the conclusion there-in, that arc faults are easier to detect at higher relative humidities.

In slight contrast to the above, and the increased WFD output with increasing humidity in Figs. 6.13 - 6.20, the results from Tables.6.2, 6.3, 6.4 and 6.5 across the full range of relative humidities indicate that the change in WFD specifically at the point of at arc ignition remains fairly consistent irrespective of relative humidity. This is better observed in Figure. 6.21, where the average change in WFD at ignition is plotted at each relative humidity tested. Most likely, this is due to the arc length of all arcs tested being very small at the point of arc ignition, resulting in a similarly small difference in their impedance.

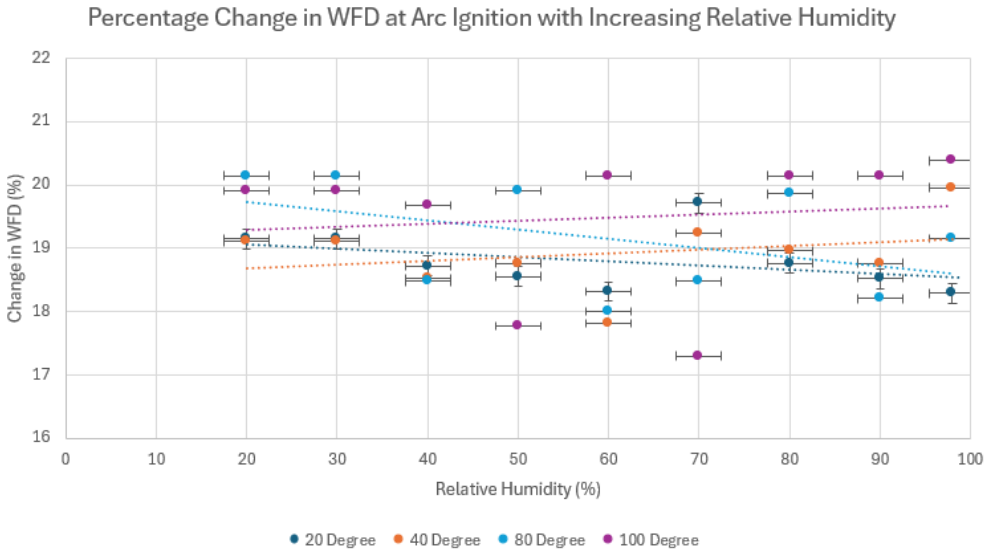


Figure 6.21: Average Percentage Change in WFD at Arc Ignition versus Relative Humidity at 20°C, 40°C, 80°C and 100°C

The clearest of the trends seen in Figs. 6.13 - 6.20 however, is the increase

in WFD change as ambient temperature increases, making the arc considerably easier to distinguish from "normal", pre-arc conditions at higher temperatures. This is observed across all points of the arc, including both the arc burning phase, and at arc ignition with Tables. 6.2, 6.3, 6.4 and 6.5 clearly indicating an increased change in WFD at arc ignition at higher ambient temperatures, increasing from an average of 18.8% at 20°C to 19.48% at 100°C. When considering the earlier results in Figure. 6.8 indicating an increase in arc impedance with increasing ambient temperature, it can be postulated that the increased impedance at higher ambient temperature has again led to an increase the magnitude of arc noise superimposed on the load voltage waveform. The increased arc transient behaviour results directly in an increase in WFD change throughout the arc and therefore makes arc detection easier due to the larger change between arcing and non-arcing conditions. These results also further highlight the danger of not fully considering environmental factors when designing arc fault protection, as the magnitude of detectable arc features is seen to reduce with ambient temperature, alongside the magnitude of the arc detecting response, leading to an increased risk to system safety from arcs in cooler environments.

6.2.3 Results Summary

The broad-scope study presented in Chapter. 6.2 has demonstrated how both the behaviour and detectability of DC series arc failures varies with both increasing relative humidity and ambient temperature, and illustrates the potential consequences this has for DC arc protection. Analysis of DC series arcs under these changing environmental conditions has demon-

strated the following behaviours that differentiate arc faults under varying relative humidity and ambient temperature:

- DC series arc failures burn for a longer duration and reach greater arc lengths at both a lower relative humidity as highlighted in Figs. 6.2, 6.4, 6.5 and 6.6, and a lower ambient temperature; as indicated in Figs. 6.2 - 6.5, Figure. 6.6 and separately in Tables. 6.2 - 6.5.
- There is an increase in arc impedance at arc collapse for both increased relative humidity as shown in Figs. 6.2 - 6.5, and increased ambient temperature, highlighted in Figure. 6.8 and Tables. 6.2 - 6.5.
- There is a significant increase in the magnitude and frequency of arc transient behaviour across all stages of the arc as relative humidity and ambient temperature increase. This is demonstrated in Figures. 6.2 - 6.5, in the 3D plots of load voltage, time and relative humidity shown in Figures. 6.9 - 6.12.
- In the WFD output plots in Figures. 6.13 - 6.20 the increased transient features provide an aid to arc detection, and demonstrate an increase in Windowed Fractal Dimension output with increasing transient behaviour as relative humidity increases, and an increase to WFD output with higher ambient temperature independent of other factors.

It has been shown that series arc failures burn for longer and achieve greater minimum arc lengths as both relative humidity and ambient temperature decrease. Additionally, arc faults at lower relative humidity and ambient temperature are shown to display smaller and less frequent transient features when the arc is burning, potentially due to a reduction in arc

impedance. A reduction in transient features has been shown to be of consequence to arc detection, with an observable reduction in the magnitude of output response from the WFD arc detection algorithm as temperature and relative humidity decrease. When considered together, these results strongly suggest that DC series arc failures are more dangerous and more difficult to detect at lower temperatures and relative humidities, and that care should be taken in understanding the effect of the environment on arc failure for future arc fault circuit interruption.

These results have also indicated the need for further work in two prospective areas. Firstly, a study concerning how the ambient environmental conditions affect air-plasma resistivity, in an effort to better understand and quantify the changes in arc impedance with increasing humidity and temperature seen in this work. Secondly, a broad-scope study of how other existing arc fault detection methods react to the increased arc transient behaviour, and the increased arc impedance at higher temperature and relative humidities to canvass their reliability across a range of environmental conditions, and assess the impact that this may have on the currently installed arc fault circuit interruption in industrial applications.

6.3 Chapter Discussion and Future Work

The work recorded in this chapter has documented a series of experiments intended to characterise how changing ambient temperature and relative humidity might influence DC series arc detection. This was identified as an existing knowledge gap in [4] and has potential benefit for the electrifica-

tion of transportation, and the installation of DC microgrids. Additionally, work intended to clarify the implications of changing environmental conditions for arc fault protection, and the ramifications that this would have in a practical or industrial setting when designing and commissioning arc fault detection schemes.

Results presented in this chapter have demonstrated that changing relative humidity and ambient temperature can have a significant effect on DC series arc faults, influencing both the arc duration and length, as well as the arc impedance, transient behaviour and detectability.

It has been seen across all results presented that a reduction in ambient temperature produced an increase in arc duration and minimum arc length. This presents a considerably more dangerous condition than the contrary, as longer duration arcs have a greater window in which to cause component failure due to overheating, or to start electrical fires through the ignition of surrounding components, cladding or conductors. Similarly, the observed increased minimum arc length infers that arc faults in less humid, cooler environments can travel greater distances from the point of initial failure before the arc collapses. This in turn would allow the arc to damage other circuit elements further from the fault, or short to another conductor at differing potential and trigger a further parallel or ground arc fault. As such, it can be concluded that industrial applications with controlled climate conditions such as data centres, where humidity and temperature are kept artificially low due to thermal considerations, are at increased risk of damage from arc failure. Hence, both renewed risk assessment and the application of a proper DC arc fault circuit protection scheme should be considered a priority in industrial settings moving forward, especially as the

cost of fault detection installation is very low compared to the financial, personal and reputational damage that could come about as the results of an arc induced electrical fire.

It is also clear from the results in this chapter that there is an increase in arc transient behaviour and arc impedance at higher relative humidity and temperature. These effects have been demonstrated to result in a notable increase in arc detectability, yielding an increased magnitude output response from the Windowed Fractal Dimension arc detection technique. Following this, it is a fair assumption that the increased magnitude and frequency of transient arc features and the increased arc impedance will result in easier detection of the arc irrespective of the detection method used. The additional arc features seen provide a more significant disturbance from normal circuit behaviour, and can help discriminate the arc from both normal operation and from false-positive causing events such as step load changes. It can thus be concluded that arc detection techniques utilising impedance-based methods, or those directly discriminating using superimposed arc noise such as the WFD technique, should see an improvement in their efficacy as arc impedance and transient behaviour increases at higher relative humidities and temperatures. Conversely, there is then an additional risk of arcs in lower temperature, lower humidity environments, with the arc being harder to discriminate, increasing the potential of missed detections, therefore directly resulting in an increased risk posed by arc failure.

The reduction in arc duration and noticeable increase in both arc impedance and arc transient behaviour with increasing temperature and relative humidity highlighted in all figures and tables of this chapter together show

an unusual trend. Lower arc impedance is to be expected when considering arcs of shorter duration and length, but direct comparison of the box and whisker charts in Figure. 6.7 and Figure. 6.8 indicates that arc impedance continues to increase despite a reduction in arc duration. This is also shown in Figure. 6.22 plotting a scatter of the averaged values of peak arc impedance versus electrode separation from Tables. 6.2, 6.3, 6.4 and 6.5 for comparison, where clusters of results at 20°C and 100°C have been highlighted.

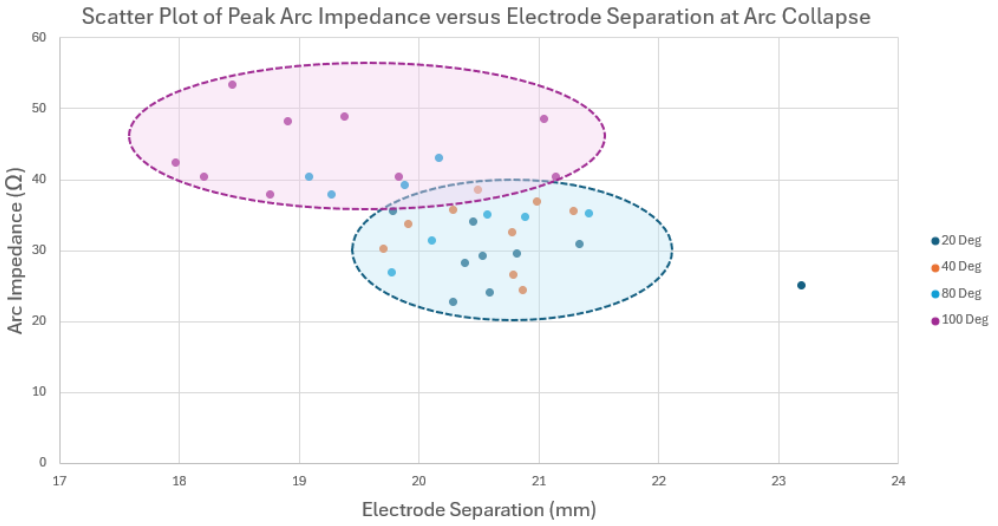


Figure 6.22: Scatter Plot of Peak Arc Impedance versus Electrode Separation at Arc Collapse

The spread of 20°C and 100°C results shown in the scatter-plot in Figure. 6.22 indicate that the arc faults at 20°C have reduced impedance, despite their larger minimum arc length, when compared to arc faults at 100°C. Whilst more experimental results may be necessary to determine the true relationship between arc impedance, temperature and electrode separation, collectively Figs. 6.7, 6.22, and 6.22 demonstrate that there may be a correlation between these variables that warrants further study. Given the popularity of impedance-based arc fault detection methods, these

results also highlight a potential oversight in the design of these detection methods, as the magnitude of arc impedance and the transient effects shown is not constant, but instead varies significantly under different environmental conditions. As such, impedance-based methods would need to be re-calibrated across a broad spectrum of environmental conditions to ensure their continued efficacy.

The reduced arc detectability in lower temperature, lower humidity environments also poses a challenge for industry, bringing into question the efficacy of existing, installed arc detection techniques. Most arc detection methods are reliant on specific parameters defined at the point of design, or during commissioning, and may only be capable of discriminating arc failures at the conditions they were initially designed/tested in. By extension, these existing detection methodologies should be subject to additional scrutiny, and should be re-tested across a range of environmental conditions to ensure their continued efficacy. This specific outcome has a particular consequence for for electric transport applications that frequently experience a change in environmental conditions, such as more-electric aircraft or ships. Given the variability of the operating environment of these applications, it can no longer be assumed that an arc detection system installed or commissioned at one location will continue to function as expected when in transit or at another location. The necessity for the calibration of arc detection algorithms to differing environmental conditions becomes obvious, when considering the potential logistical and financial ramifications of an arc induced electrical fire during shipping, or the loss of human life during an electric aircraft fire.

Despite a 100% detection rate using the WFD arc detection algorithm

during the tests performed in this chapter, further work is necessary to understand how other commercially available and theoretical arc detection methods react to changing environmental conditions, and the potential scale of the problem this poses to industry. Preliminary results from this work indicate that impedance-based arc detection methods, or those that discriminate specific arc behaviour may be particularly vulnerable to changes in environment due to the variable magnitude of arc-related transient features and arc impedance seen with changing ambient temperature and relative humidity. Without further study it is unclear how other arc detection techniques, such as optical, reflectrometry, frequency based and machine learning based methods will react to change in arc behaviour with changing environment. It can be postulated at this time that frequency and optical based methods may be more affected, with the variable magnitude of transient arc noise potentially influencing the measurable frequency content of the arc, and the differing environment potentially occluding the arc from optical methods. The response of machine learning methodologies are at this time an unknown, as the response of the technique to changing arc behaviour will depend heavily on the algorithm inputs, hyper-parameters and the range/suitability of the training dataset used for the model. Collectively, this highlights a new knowledge gap in understanding the suitability of a broad-range of arc detection techniques within variable environmental conditions, laying the foundations for future work in this area.

In this work, the relative humidity and ambient temperature of the arc environment were considered, disbarring other environmental factors such as pressure and gas volume due to equipment availability. This requires the usage of specialist environmental chambers and monitoring equipment and was outside the budget of this project, hence its exclusion within the body

of this work. There is therefore the opportunity for further work in this area, controlling more features of the gaseous environment surrounding the arc and studying the impact this has on arc electrical behaviour and on arc detection.

6.4 Chapter Conclusions

This chapter has presented a novel study on the impact of changing relative humidity and ambient temperature on the behaviour of DC series arc faults and the consequences this has for arc detection. Based on the results discussed, the following conclusions can be drawn:

- The WFD arc detection technique is suitable for use in environments of changing relative humidity and temperature in its current state, achieving a 100% detection rate, successfully identifying arc failure from pre-arc conditions in all 180 arc fault data captures.
- DC Series Arc Failures produce a larger change in WFD at arc ignition in higher relative humidity environments, and at higher ambient temperatures, versus those tested at lower temperature and relative humidity. Results also suggest arcs should also be more easily detected under these conditions using impedance-based or noise-based arc detection techniques.
- DC Series Arc Failures have a longer duration and arc length when burning at lower relative humidities, and at lower ambient temperatures; indicating a heightened risk of damage from arc failure as arcs can reach greater distances from the source to ignite other compo-

nents, though additional experimental work with more environmental control factors is necessary to validate these findings.

- DC Series Arc Failures have shown greater arc impedance at lower relative humidities, and at lower ambient temperatures. This is reflected onto circuit voltage and current waveforms as transient spikes of greater magnitude and time-frequency. Further experimental work with more environmental control factors is also required here to validate these findings.

- The risk to DC power system from series arc failure increases with decreasing relative humidity, and with decreasing temperature, presenting a greater physical threat due to larger size and duration faults that have greater capacity to start electrical fires through prolonged heating of surrounding components and insulation, alongside a having a higher threat potential due to the reduction in detectability.

  Future work in this area should focus on repeating of the existing experiments at 40°C and 60°C with consistent electrode materials to determine if the outlier results seen at 40°C are consistent, and to verify whether the 60°C results would follow the pattern seen at other temperatures and humidities. Similarly, further work should consider additional environmental control factors such as ambient pressure that may also contribute to differing arc behaviour, that proved outside the scope of work in this thesis due to equipment constraints.

Chapter 7

Practical Implementation and Commissioning Considerations

Contents

This thesis has presented the Windowed Fractal Dimension (WFD) arc detection method, demonstrating its capability across a range of arc ignition type, circuit load topologies and environmental conditions, within a laboratory setting. This chapter serves to expand upon the changes and considerations that are required for implementation of the WFD in a practical industrial, power generation/distribution, or electric transportation setting, whilst also identifying where future work is required.

7.1 Commissioning of WFD Variables

When considering practical application of the WFD technique it is important to consider how the variables internal to the method might need adjusting to fit the to-be protected power network during the commissioning process. These two variables are the sampling window size, N_{win}, and the threshold for arc detection. Both of these variables and the selection of their final value for testing within work in this thesis has been discussed previously in Chapter. 4, but bare further consideration for applications outside of a laboratory setting. Commissioning considerations will be discussed for each variable in turn, with the potential repercussions highlighted.

7.1.1 Sampling Window Commissioning

The sample window size, N_{win}, determines the number of data points input to the WFD technique in each discrete time instance, and is the namesake of the "Window" in Windowed Fractal Dimension (WFD). These data points

are then processed to determine the fractal dimension at that discrete time point, before the window is shifted by half N_{win} samples and the process repeated, sampling either an entire waveform or running continuously for online operation. For commissioning of an appropriate sampling window size, it is necessary to understand the factors it is reliant on, how changing this value will affect the output WFD response, and how these changes might influence arc detection with the WFD technique.

The first consideration is the sampling frequency of the sensors and DAQ input to the device running the WFD technique. For all the work in this thesis, N_{win} was fixed to capture a 0.5 ms window of the input signal, capturing a fixed 1024 samples at a sampling frequency of 2 MHz. The dependency on sampling window on sampling frequency becomes clear when considering now if this 2 MHz example sampling frequency was halved to 1 MHz. The 1024 samples captured by N_{win} now represent a 1 ms window of the signal, rather than 0.5 ms. Any adjustment in sampling frequency will therefore inherently change the amount of signal captured by each sampling window, and additionally, will increase the discrete time step between each adjacent sampling window of N_{win} samples. As the sampling window moves by half N_{win} samples during each discrete time step, a halving of sampling frequency also corresponds to a halving of the required number of signal windows to process a signal of N total samples. This is represented diagrammatically in Figure. 7.1 where the effects of changing both sample frequency and window size can be seen. From Figure. 7.1 it can also be seen that the increased discrete time size of the sampling window caused by a reduced sampling rate can be rectified by halving the number of samples in the window i.e. in Figure. 7.1 $F_S = 2$ MHz and $N_{win} = 1024$ samples is equivalent to $F_S = 1$ MHz and $N_{win} = 512$ samples, requiring

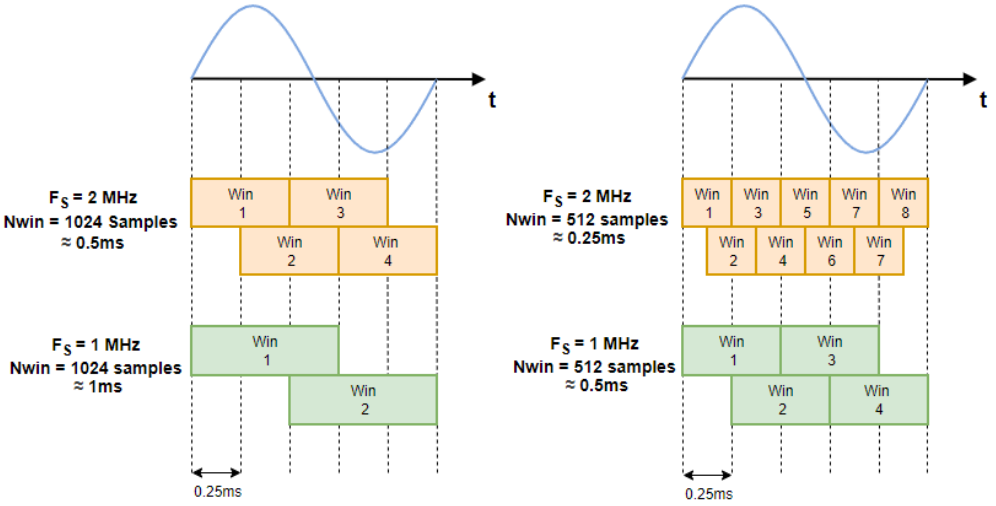


Figure 7.1: Illustration of Window Function Dependency on Sampling Frequency

the same number of signal windows to fully sample a signal of N samples without spectral leakage.

Whilst the number of samples in the sampling window N_{win} can be adjusted to compensate for changing sampling frequency, this is not necessarily the best decision. In changing both the size of the window (and therefore the frequency of the sample windows) there will be a corresponding change in computational burden and calculation speed, therefore affecting the detection time of the technique. Additionally, changing window size will have a further impact on the accuracy of the fractal dimension calculation, with the potential to exclude some of the higher frequency arc behaviours if reduced to a point where the Nyquist sampling criterion is no longer satisfied. Both of these consequences were discussed earlier in Chapter. 4, but lead to a trade-off between calculation accuracy and runtime when choosing window size, with smaller windows reducing both calculation and detection time, but also resulting in lower accuracy of the fractal dimension representation of the signal by limiting the amount of signal (and therefore

fractal behaviours) that are captured in each window.

The primary concerns for commissioning of the WFD window size are therefore the sampling frequency input to the WFD method, and the detection time-to-accuracy trade off that comes with adjusting the window size to compensate for a change in sampling frequency. In an ideal situation, input to the WFD should utilise a sampling frequency as high as possible, in the mega-hertz range (using the 2 MHz sampling rate recorded in this thesis as an example of a suitably large sampling frequency). This is not outside the realm of reason for power electronics based distribution systems, as any sampling of pulse-width modulated or switching waveforms requires a sampling rate at least 5x larger than the highest frequency present [48]. With modern power electronic switching frequencies already in the 20 kHz - 2 MHz range, use of an existing voltage and current tap sampling in the MHz range for WFD input should be possible [120]. This removes the sampling frequency as a limiting factor for WFD, allowing the commissioning engineer to decide on the appropriate trade-off between detection accuracy and speed by adjusting the size of the sampling window, N_{win}. As a sampling window size (in time) of 0.5 ms can achieve a theoretical detection time of 1.5 ms (as demonstrated in this thesis), there is little requirement for reducing the window size further for faster arc detection, as 1.5 ms is already very fast when considering the 30ms or more required to trip typical DC circuit breakers and switchgear [76, 77]. With the upper limit for detection speed defined, commissioning can focus on window size adjustment for slower, but potentially more reliable fault detection. Whilst rapid, 1.5 ms fault detection is necessary on power networks in MEA and electric transport applications where the consequences of a fault extend to human life, for applications in solar micro-grids or data centres a slower

detection time with a greater degree of confidence may be more appropriate, reducing the potential for expensive downtime due to false detections whilst still ensuring (comparatively) fast fault detection compared to other arc fault detection techniques discussed in Chapter. 2.

When confronted with a lower sampling rate (e.g 10kHz) a larger sampling window should be utilised to ensure the accuracy of detection, as an entirely missed fault detection is more consequential than a slow detection. A potential compromise to improve accuracy whilst maintaining faster detection time with smaller windows is to run multiple WFD approaches in parallel throughout the power network. Whilst increasing the installation time and cost, this reduces the chances for a missed detection from the method due to the smaller window size by capturing the WFD at multiple points for comparison. Results in Chapter. 5 have indicated a stronger response by the WFD algorithm when measurements are taken physically closer to the arc. Utilising a spread of measurements from throughout a power system as inputs to the WFD increases the likelihood that one of the measurements will be close to the arc and display an increased response from the WFD at arc ignition, mitigating the risk of missed detection posed by smaller sampling window size (and the corresponding uncertainty in fractal dimension accuracy). There is also the possibility for further processing of these multiple WFD measurements for arc location (as discussed in Chapter. 5) or as to improve the confidence of the detection through logical comparison techniques or cross correlation, though the implementation of both of these techniques the topics of future work.

7.1.2 Detection Threshold Commissioning

Perhaps the more obvious variable that bears consideration during commissioning of the WFD is the detection threshold value. This threshold value acts as the boundary that discriminates between normal circuit behaviour and an arc failure, indicating the presence of an arc fault when the fractal dimension of the WFD output waveform crosses the boundary. In tests recorded within this thesis, and as discussed in full in Chapter. 4, the threshold value is fixed at ± 10% of the pre-arc RMS fractal dimension value, and was selected as the ideal threshold for binary classification of an arc failure fault through characterisation using Receiver Operating Characteristic analysis. Initial ROC characterisation was carried out in Chapter. 4 for both current and voltage WFD outputs, utilising 30 different data captures per threshold across both arcing and normal conditions, for results captured on passive circuit loads. In advance of any commissioning, one method to improve the detection threshold value for the WFD method is to re-apply the ROC characterisation, with a considerably broader set of captured arc failure results including several different load and environmental conditions for arcing and non-arcing loads. For example, inclusion of 10 arc fault data captures and 10 healthy data captures for each of the load topologies in this thesis (disregarding for now the many sets of arc fault data capture in different environmental conditions) in addition to the existing passive results input to the ROC would result in 60 healthy and 60 faulty data records for threshold characterisation for both voltage and current WFD waveforms.

The increased range of circuit behaviours, alongside the greater number of inputs to the ROC characterisation would allow the determination of a new

detection threshold value that is better suited to this broad range of load types, rather than only being characterised on passive results. This in turn improves the generalisability of the WFD method to any future power system, as the new detection threshold will have been statistically determined as the best option for arc detection across a larger range of input conditions. Whilst this method serves to improve the detection threshold in all cases, it will be a very time consuming analysis to perform, requiring the processing of 120 data captures for combined arcing and healthy results for each different detection threshold tested. For example, testing detection thresholds in increasing 2.5% increments from 5% to 17.5% as in this thesis would require processing of 720 different data captures, increasing dramatically as the ROC analysis becomes more granular, testing smaller and smaller detection threshold increments. Despite being laborious in nature, this analysis would not be a feature of regular commissioning, and would only require completing once to provide a more reliable and generalisable detection threshold, applicable to (and verified against) multiple different power network topologies once completed. Manual adjustment of the detection threshold during WFD commissioning is inadvisable, as until a fault has occurred (potentially damaging the power network) it is unknown whether the manually adjusted threshold will be suitable to detect the arc. It is unfeasible to produce and test against empirical fault conditions within each power network to be tested, as this becomes very labourious with increasing scale, and has the potential to significantly damage any power network during the commissioning process. Therefore a pre-calibrated WFD threshold using laboratory captured results is a preferred solution to ease future commissioning burden.

As DC series arc fault models improve, there is the likelyhood that hardware-

in-the-loop style simulations and testing will be capable of reproducing a facsimile of empirical arc failure, representing both macro-scale behaviour and micro-scale arc burning behaviour. This opens up new options for the commissioning and manual tuning of WFD detection thresholds, as simulated fault data can be combined with simulations of healthy power network operation, or even directly injected into the power network. In this way, a commissioning engineer can observe the response of the WFD on this new power network to the fault, and can make an informed decision on how best to adjust any detection criteria. It would also become plausible to perform bespoke ROC characterisation for faults on these networks, and produce specifically tuned WFD detection thresholds unique to that power network, this will however drastically increase commissioning time as previously discussed, but is a viable approach for human safety-critical systems.

The primary concern for commissioning the WFD detection threshold (outside of performing bespoke ROC characterisation) is the capture of non-arcing, "baseline" WFD values, as the detection threshold to indicate an ongoing arc failure is determined as deviating from this baseline value. As discussed in Chapter. 4 earlier in this thesis, the WFD algorithm dynamically determines the pre-arc baseline value by from the first 8 N_{win} sampling windows. For a 2 MHz sampling frequency, this corresponds to $N_{win} = 0.5$ ms, resulting in the baseline value being determined from the first 4 ms of input signal. Due to the dependency on N_{win}, this initial time window where the baseline value is calculated is subject to change with different sampling windows and N_{win} commissioning/tuning. Additionally, this introduces the requirement that the variable N_{win} is commisioned in advance of the detection threshold value. Whilst the current dynamic commission-

ing of this value does ease the requirement for manual commissioning, it leaves the system vulnerable when restarting following another fault condition or shutdown. If the system is still faulty shortly being restarted, the WFD as it stands will record the faulty system value as normal, and would therefore not indicate the presence of the ongoing fault. This can be rectified through a small change to the WFD to store and utilise a user-defined pre-arc baseline value. This can be determined in advance through offline application of the WFD to healthy system data captures, and then stored by the commissioning engineer in the processor controlling the WFD protection for future systems. This also removes the dependency of dynamically calculating this variable on N_{win}, simplifying commissioning by allowing each variable to be fixed independently. Whilst increasing the reliability of the system, this does introduce the requirement for additional human interaction, and would need repeating should the power network architecture change significantly, as this may adjust the resting fractal dimension.

7.2 Additional Considerations for Practical Implementation

This final section discusses further considerations that can be made during commissioning to improve the level of confidence in the WFD method for fault detection, and ways in which the WFD and its inputs might be modified to potentially improve the response from the algorithm in future applications.

It has been demonstrated in Chapter. 5 that whilst showing a consistent response to arc failure from voltage waveforms, the WFD algorithm does not respond consistently to arc fault current waveforms, in some cases showing reduced change in fractal dimesion at arc ignition when compared to load voltage (as seen in controlled resistance load results in Chapter. 5, Section 5.2.2), and other cases showing an greater change in fractal dimension at arc ignition (as seen for normal and DCCM, "burst-mode" arcs in Chapter. 5, Section 5.2.3). For practical implementation, line current measurements would be preferred as the use of hall effect current type sensors is less invasive than the installation of bespoke voltage sensors to terminal bushings and taps, reducing the overall commissioning burden and cost. One possible reason for the difference in voltage and current WFD response during testing in this thesis is the disparity in measurement bandwidth between the differential voltage probes and hall-effect current clamp used during the data capture. Whilst both voltage and current are filtered at 25 kHz as part of the WFD processing, the initial measurement bandwidth of the differential voltage probes is 10 MHz, versus the only 5 kHz for the hall effect current clamps. Despite suggestions from the literature that most significant arc frequency components are below 3500 Hz, there will likely be some component of the arc behaviour imposed onto the circuit as higher frequency signals [2, 8, 81, 84]. As such, it is likely that the bandwidth-limited current traces contain less information about the arc on a ms-µs timescale versus the high bandwidth voltage traces before they are filtered. Therefore, it might be possible to improve the WFD response to current measurements by utilising current probes with a greater bandwidth, up to the 25 kHz filter cutoff frequency. Whilst further work is necessary to verify the exact effect increasing current measurement bandwidth will have on the WFD output, any increase in the amount of arcing behaviour that can be captured in the current traces should improve the performance of

the WFD in discriminating the arc, capturing more fractal behaviour that the WFD method can capture.

Another, more specific consideration for practical application is the typical response of the power network to step-changes and parasitics, and the influence this might have on the WFD. In Chapter. 5 it was highlighted that the pseudo-fractal behaviour of under-damped sinusoids produced through RLC oscillation or overshoot of power-electronic converter control causes a change in WFD output, and whilst managed by the existing threshold based detection method should still be mitigated against where possible. This behaviour should be addressed fully in future work, however there are several different interim options that can be explored to mitigate the chances of a false-positive detection caused by these pseudo-fractal spikes. The first option is understanding how the to-be-protected circuit reacts to step load changes, and the regularity with which these events occur. Many power networks are already impulse tested at high voltages to determine their response to lightning strikes and transient voltage. Utilising the existing impulse test data can give an indication about how the circuit responds to sudden transient events, and data captures can be processed with an offline version of the WFD technique to determine whether or not they will be problematic for arc detection using the technique by assessing if they produce a significant change in fractal dimension.

For power networks with regular load step changes or intermittent load switching, an alternative approach must be considered as the risk of false positive detection increases with the frequency of these potentially problematic transient step changes. One such method to mitigate against false positive results in these conditions, and to generally improve the level of

confidence of the WFD across all power network configurations is to implement arc protection that combines the WFD with another arc detection method. A simple logic controller with an AND gate, monitoring the output of each detection method for a logical high can serve as a reasonably cheap option to mitigate against the false-positive conditions of either of the detection methods, whilst also allowing the use of two detection techniques and eliminating any single point of failure. Whilst fairly simple in concept, this approach does however introduce additional commissioning cost, requiring the setup and testing of an entirely separate arc detection approach, as well as the additional material cost. Furthermore, this has ramifications on the detection time of the arc failure, as the combined approach will be limited to the slower of the two arc detection methods, plus any additional time delay introduced by the logic controller. An alternative approach, which does not sacrifice the fast detection time of the WFD approach is to monitor the WFD of both voltage and current waveforms as inputs to the logic controller, rather than a separate detection method, as both methods then share the same minimum theoretical detection time. It was demonstrated in Chapter. 5 (using Figure. 5.21 as one of many examples) that transient switching events that produce a change in WFD output for one measurement (e.g. current) do not necessarily produce it for the other, due to circuit filtering effects caused by components such as power converter input capacitance or similar. Both current and voltage waveforms have however been shown to produce a significant response to arc fault ignition in Chapter. 5. With the potential improvements to the response of the WFD to current measurements as previously discussed, both voltage WFD and current WFD measurements used in tandem becomes an option to help mitigate against false positive detections in more challenging power networks (such as those with irregular intermittent switching or step load changes). This approach will require the installation of voltage probes as

well as current probes, but reduces the commissioning challenge of introducing an additional detection method, and may still be manageable with a single FPGA or microcontroller as the technology improves.

One possible consideration that can help reduce the computational burden of the WFD approach in a practical setting is the replacement of the digital lowpass filter with a physical filter equivalent on the input channels to the WFD processing controller. The current implementation performs time-domain convolution of the impulse response of a third-order 25 kHz FIR lowpass filter with the incoming WFD signal windows within the programming of the WFD itself. Implementing this filter architecture instead using cascaded first and second order Butterworth lowpass filters built from op-amps and passive components will take very little space on a PCB (also containing a microcontroller/FPGA and the rest of the arc fault circuit interrupter). This removes a calculation from every input signal window to the WFD and the requirement to store the FIR filter coefficients internal to the microcontroller, reducing the overall computational burden and therefore potentially facilitating the use of a less expensive microcontroller and reducing therefore the material cost of implementing the technique.

Chapter 8

Conclusions

Contents

This thesis has developed and presented the Windowed Fractal Dimension technique for detecting DC series arc failures within DC power distribution systems. The work described in this thesis has covered the development of multiple systems for repeatably generating DC series arc failure for experimentation, and has highlighted the insufficiency of simulated arc fault models for reliably recreating micro-scale arc transient behaviour. The development of the WFD technique has been presented, with all relevant signal processing and data conditioning considerations taken into account, theorising that upon ignition an arc fault will introduce to the circuit waveforms fractal behaviour that is fundamental to the arc, and that this behaviour can be used to discriminate arcing and healthy conditions. The developed WFD technique has been shown to be effective in successfully discriminating an arc fault when applied to multiple arc ignition types, passive circuit loads, active switching circuit loads, to loads with significant frequency content and to circuits containing switching power electronics operating in both a normal-mode of operation and in a DCCM "burst-mode" of operation, showing resilience to false-positive detections. Additionally, the efficacy of the WFD technique has been demonstrated across a range of changing environmental conditions, sweeping a range of different ambient temperatures and relative humidities and providing suggestions about how these environmental factors can influence arc protection. Finally, considerations for the implementation and commissioning of the WFD technique in a practical setting have been discussed.

This chapter aims to conclude the work described in this thesis, providing comparison to the specific research aims in Chapter. 1 and how they have been achieved, alongside providing suggestions for future work.

8.1 Comparison to Research Objectives

In Chapter. 1 of this thesis, the following research objectives were outlined:

1. Production of an experimental rig to reproduce DC series arcs failures, allowing for variable arc types, a variety of electrical loads and user-defined environmental conditions.

2. Development of a novel method of DC arc failure detection and demonstrate its viability across a range of different load conditions.

3. Investigate the effects that different electrical and environmental conditions have on DC arc characteristics and the repercussions this has for DC arc detection and circuit protection.

Each of the research objectives will now be revisited, comparing them against the key findings of the work and demonstrating how they have been addressed.

8.1.1 Objective 1

The first objective was addressed primarily in Chapter. 3, but features throughout this thesis. To satisfy this objective, two different arc generators were produced: a forced separation (drawn) arc generator shown first in Figure. 3.1 and a forced failure arc generator shown in Figure. 3.6. The forced separation arc generator in Figure. 3.1 was designed to be user controllable, allowing for the ignition of an arc fault through the separation of two (initially touching) electrodes to produce a circuit airgap to be ionised into arc plasma, by controlling one electrode to move through the use of a programmable DC stepper motor. The stepper motor was controlled

through the use of a TinyGV8 CNC controller and a custom set of serial commands in MatLab, allowing for precise positional and speed control of the mobile electrode. In linking the forced separation controller to MatLab it became synchronised with the experimental data capture, allowing for arc failures to be reproduced at exactly the same time, using the same forced separation generator settings, removing user error in the timings. The forced failure arc generator in Figure. 3.6 was designed to provide an alternate means of arc ignition, simulating sudden component failure, in contrast to the steady drawn arc of the forced separation arc generator. This was achieved through deliberate destruction of an underrated conductor placed between two copper electrodes, at a fixed 20 mm separation. The arc could be ignited at a user defined time through switching relay control (highlighted in Figure. 3.7) by switching current from a non-faulty path to the underrated conductor, which upon receiving the circuit current would rapidly melt, leaving an ionised airgap and forming the arc failure.

Arc failures produced using these generators have been demonstrated throughout this thesis in a range of circuit different circuits including: For passive and active switching loads in Figure. 3.3, for circuits containing switching power electronics in Figure. 5.37 and for circuits contained within a controlled climate chamber, as shown in Figure. 6.1. DC series arc failures produced using these generators have shown to be consistent between results within this thesis, and with other DC arcs in the literature, and have provided a reliable foundation for arc fault generation and data capture for the works within this thesis [2, 4, 6, 10, 18, 81, 82]. In addition to the production of both arc generators, simulations were performed to determine their suitability for generating large volumes of DC series arc fault data for testing. Despite being able to represent the macro-scale current

and voltage behaviours of the arc to a reasonable degree of accuracy, the simulations could not properly resolve the micro-scale (ms-µs) chaotic behaviours of the arc fault [41, 42, 43]. As the focus of this thesis was the design of a detection method that discriminates arc failure based on the fundamental fractal behaviour of the arc, the simulated arc results that did not correctly represent this behaviour were deemed unsuitable, and work instead focussed on use of empircal arc fault data captures using the arc generators as described.

8.1.2 Objective 2

The second research objective was primarily addressed in Chapter. 4 where the development of the WFD arc detection technique was documented, and in Chapter. 5 where the WFD technique was then applied to detect DC arc failure across a range of circuit loads and arc ignition types. The efficacy of the developed WFD technique was demonstrated further, for a variety of environmental conditions in Chapter. 6, highlighting its capability in a range of different ambient temperatures and relative humidities.

In Chapter. 4 it was theorised arc faults are equivalent to scaled-down lightning bolts, and will display similar properties. Both lightning bolts and arc failures have been recorded in the literature as chaotic, with lightning specifically noted as having fractal behaviour [87, 88, 89, 90]. Therefore, if the arc did behave as scaled down lightning, it too would demonstrate fractal behaviour that would be superimposed on circuit waveforms and could provide therefore a discriminator for arc detection if measured. The WFD arc detection method was constructed based on this initial hypothesis, calculating the fractal dimension of normalised, short-time (0.5 ms)

windows of input signal, and monitoring the output for a change. If the change in fractal dimension of any three consecutive input signal windows (from a resting value determined from the RMS fractal dimension value of the first eight signal windows) exceeded a 10% threshold (determined as most suitable through Receiver Operating Characteristic analysis of several possible detection thresholds) then an output trigger would be produced, signalling the presence of an arc failure with a theoretical 1.5 ms minimum detection time.

The WFD method produced practical detection times as low as 1.6 ms (as shown in Figure. 5.6) when applied to empirically captured DC series arc failures as described in Chapter. 5. In this chapter, the WFD method was shown to successfully discriminate DC series arc failure in circuits with purely passive loads (Figs. 5.1 and 5.2), active switching circuit loads for both controlled resitance oscillations (Figs. 5.11 and 5.13) and controlled current oscillations (Figs. 5.28 and 5.30), to loads with significant frequency content (Figs. 5.12 - 5.14 and Figs.5.29 - 5.31) and to circuits containing switching power electronics operating in both a normal-mode of operation (Figs. 5.40 and 5.41) and in a DCCM "burst-mode" of operation (Figs. 5.46 and 5.47). The WFD technique therefore has demonstrated the capability to distinguish between healthy and arcing (faulty) circuits across a broad range of circuit loads and arc ignition types, displaying a robustness to typical nuisance trip conditions and a faster detection time than other methods in the literature [57, 58, 59, 60, 61, 62, 63, 65]. Whilst the pseudo-fractal behaviour of RLC "ringing" effects on some load conditions produced a measurable change in WFD output, the technique successfully discriminated these short-time transients from the change is WFD output with arc ignition, and suggestions were made to improve the resilience of the technique against this behaviour through the application of a leaky integration

technique. Though demonstrated in Figs. 5.33 and 5.34, the full effects of applying the leaky integration are the subject of future work, to determine its influence on arc detection time and other load behaviours.

8.1.3 Objective 3

Research objective three was addressed in Chapter. 6, where the arc faults were generated at a range of fixed ambient temperatures and relative humidities, with the WFD technique being applied to the voltage waveforms at each set of environmental conditions. In the described tests, ambient temperature was fixed at 20°C, 40°C, 80°C and 100°C in turn. Relative humidity was swept from 20-98% in 10% increments, performing five forced separation arc fault data captures at each increment, for a total of 225 data captures across all environmental conditions. The WFD technique produced an output sufficient to distinguish the arc fault from healthy circuit behaviour in 100% of the 225 different environmental conditions tested. Results highlighted increased arc duration and length (Figure. 6.7 and Figure. 6.6), alongside reduced arc impedance at lower relative humidity and ambient temperature despite their increasing length (shown in Figs. 6.22 and 6.8) when compared to arcs in higher temperatures or higher relative humidities. The reduced arc impedance at lower temperatures and humidities is seen to reduce the influence of arc transient behaviour on circuit waveforms and suggests that impedance-based arc detection methods will not perform as well under these conditions. This was observed in WFD output traces, where a greater change in WFD output was produced at arc ignition for arcs at higher ambient temperatures and relative humidities, versus those in lower temperature and lower relative humidity

(Figures. 6.13 - 6.20). Collectively, results presented in Chapter. 6 have highlighted the suitability of the WFD technique for use across a range of different environmental conditions. Results also suggest that there is an increased risk from DC series arc failure in environments of lower ambient temperature and relative humidity, where arc faults present a greater physical threat due to larger arc size and duration, and an increased threat potential due to the reduction in detectability through the demonstrated reduced arc impedance and WFD response. This also suggests that electrical systems operating in variable environments (such as MEA) are at increased risk from arc failure, with the potential for changing arc behaviours across different operating environments to elude arc fault detection techniques commissioned elsewhere. Additional work is required in this area, controlling more environmental factors (e.g. pressure, air circulation) as arcs are generated to determine the full effect that environmental conditions have on arc generation, detection and propagation, and the consequences this has for circuit protection.

8.2 Research Outcomes

Having considered all of the research objectives and the work to date captured within this thesis, the outcomes of the work can now be summarised. Repeated below from Chapter. 1 are the main contributions of this thesis to the field, each of which has been the result of peer reviewed publication; all of which are available in Appendix. A:

- Development of a DC arc detection algorithm, capable of distinguishing arcs through calculating and monitoring the fractal dimension of

arcing waveforms, assuming the chaotic, self-similar behaviour of the arc is comparable to the fractal behaviour seen in lightning discharge. This work resulted in publications [1] and [26].

- The implementation of the aforementioned arc detection algorithm to DC series arcs across an extensive range of different passive, active and power electronic loads, changing environmental conditions and differing arc ignition types. This work contributed heavily to the publication of [26].

- The investigation of the effects of changing relative humidity and ambient temperature on DC series arc characteristics, providing a suggestion of how this impacts arc generation and detection, with fixed temperature and electrical characteristics and highlighting the necessity for further work in this area. This work was presented at a conference and published in the proceedings in [27].

8.3 Suggestions for Future Work

Throughout this thesis the limitations of the work therein has been discussed, and suggestions for future work made. Whilst partly addressed in Chapter. 7, this final section aims to reiterate the weaknesses of the work and to suggest both solutions and potential avenues of future work.

The clearest avenue of future work is the physical implementation of the WFD technique to an FPGA or microcontroller for real time arc detection. Whilst results of code profiling using MatLab's SOC Toolbox in Chapter. 4 suggest that the WFD technique is suitable for implementation on modern "off-the-shelf" FPGA architecture, there is still the scope to prop-

erly optimise the code for online implementation. Application of the WFD for real time arc detection following the commissioning considerations in Chapter. 7 will give additional insight into the techniques suitability for industrial/practical use outside of a laboratory setting, and will further demonstrate the value of the technique over others in the literature. Practical implementation of the technique should also consider the improvement of input current measurements to the WFD, as these were demonstrated to produce a smaller response from the WFD at arc ignition than input voltage measurements in Chapter. 5. Current measurements are less invasive than voltage measurements and will ease commissioning of the technique, whilst also providing an addition discriminator for arcing behaviour, potentially improving the resilience to false-positive detections if used in tandem with arcing voltage measurements. As proposed in Chapter. 7, improving the bandwidth of input current measurements to the WFD may improve the response of the algorithm by capturing more of the transient arc behaviour on a smaller time-scale, therefore retaining more of the arcs fractal behaviour in the current waveforms and potentially improving the WFD response. There is also the potential that alternative, more complex loads could impact the WFD calculation, possibly though the introduceion of other chatic noise. Therefore, additional testing of the WFD technique on representative electric aircraft and electric vehicle loads should be conducted, to determine if the more complex load behaviours and geometry will impact the WFD output.

As previously discussed in Chapters 5 and 6, there is still the scope to test the efficacy of the WFD in its current form on additional circuit measurements and environmental conditions, including environments with controlled pressure in particular due to the influence this may have over arc

burning and the specific consequence this may have for More-Electric Aircraft applications and aerospace applications as a whole. Generation of further arc failures in environments with more controlled conditions will yield better results on both the nature of arc faults within these environments, and the response of the WFD to these additional environmental conditions. This in turn further informs decisions regarding suitable application environments for the WFD method, whilst also providing suggestions about how environmental factors can leave DC power systems at greater risk from arc failure. Additionally, future work should consider testing of the response of the WFD algorithm to arc failures in power networks with increasingly higher load frequency content, up to the 25 kHz filter cutoff frequency, to better understand the response of the technique when faced with non-linear switching loads and higher-frequency PWM switching transients. Additionally, it has been demonstrated in Chapter. 5 that there is the potential to revise the WFD technique to include alternative detection criteria, such as in the leaky integration in Figs. 5.33 - 5.36. Whilst initial testing of these techniques has highlighted an increased robustness to the response of the WFD to intermittent pseudo-fractal behaviours, they also introduce an inherent time-delay on arc detection, and will require thorough repeat testing across a similar range of load conditions to that presented in this thesis to fully determine their usefulness for future implementations.

Further work should also consider the application of the WFD technique to arc location. As suggested in Chapter. 5, the fractal arc noise produced from a DC series arc failure can propagate through switching power electronics, showing a reduced magnitude with increasing distance from the arc. There is therefore the potential for arc location by comparing the magnitude of WFD output responses for measurements taken across a larger

power network, with the larger magnitude changes observed in the WFD output traces at arc ignition being those that are physically closer to the arc in the circuit. This would first require the development of a larger test power network (similar in scale to the example network in Figure. 5.57) containing additional circuit loads and DC power converters, with the capability to produce empirical arc failure throughout the network. Both the scale of the network design, and the equipment costs of these tests, will prove to be a challenge during this future work.

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Appendices

Appendix A: First-Author Publications

DC Series Arc Fault Detection Using Fractal Theory

Danny Seeley
Power Electronics, Machines and Control Group
The University of Nottingham
Nottingham, United Kingdom
danny.seeley@nottingham.ac.uk

Mark Sumner
Power Electronics, Machines and Control Group
The University of Nottingham
Nottingham, United Kingdom
mark.sumner@nottingham.ac.uk

David W.P. Thomas
George Green Institute for Electromagnetics Research
The University of Nottingham
Nottingham, United Kingdom
dave.thomas@nottingham.ac.uk

Stephen Greedy
George Green Institute for Electromagnetics Research
The University of Nottingham
Nottingham, United Kingdom
steve.greedy@nottingham.ac.uk

***Abstract*—Arc faults, often caused by insulation or component failure, result in a discharge of electricity through the air between conductors. These failures are often the cause of electrical fires and pose an enhanced risk to system reliability, and this is becoming a growing problem with the uptake of more electric automotive and aircraft technologies. DC series arcs are of a particular concern as they do not trip existing circuit overcurrent protection. Arc detection is becoming increasingly difficult as DC voltages increase to meet the higher power demands of renewables, transport and series applications. This paper proposes a novel method to detect DC series arcs by monitoring the fractal dimension of the supply and load current and voltage waveforms. DC series arc faults were reproduced across a range of different setups using a 42V supply and a resistive-inductive load. The Windowed Fractal Dimension (WFD) method; implemented in MATLAB, shows a clear change in fractal dimension when an arc is sustained, providing both a means of arc fault detection and evidence that arcs have fractal properties.**

***Index Terms*—arc detection, DC protection, series arc, arc fault, fractal**

I. Introduction

An electrical arc occurs as an electric discharge between two conductors when the electric field strength between the conductors is sufficient to ionise the air separating them [1]–[3]. The arc discharge causes the circuit current to short through the air instead of it's designed path and burns hot enough that extended periods of arcing can lead to lasting component damage and start electrical fires. [4]–[7]

This work was supported by the Engineering and Physical Sciences Research Council (EPSRC).

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Many arc faults are caused by insulation failure, or by broken connections between cables and components [5], [8]. These component failures, and the subsequent arc faults, are more common in mechanical or moving systems such as aircraft or in cars, where the vibration of the vehicle can rattle components or wires loose over time [6], [7]. With the shift to more-electric automotive and aircraft, the use of higher voltage DC distribution systems is becoming more common, and with that comes an increased risk of DC arc faults [1], [8], [9].

A DC series arc occurs when a discontinuity within the circuit appears in line with a current carrying conductor, on the same conductive path. The difficulty in detecting DC series arcs comes about due to the topology of the fault itself. When the arc ignites, it introduces an additional impedance to the circuit representative of the resistance of the air plasma the current must now travel through [3]. This impedance adds in series to that of the existing circuit load, and therefore reduces the circuit current [3], [6], [8], [10], [11]. The reduced circuit current will never trigger traditional overcurrent protection and as such leaves the electrical system vulnerable to continued arc failure.

During the arcing process, the DC system becomes non-linear. Intermittent ignition and exhaustion of the arc fault can create unpredictable current spikes. Both the shape of the arc plasma and the electrical noise it produces are chaotic, as has been suggested many times in literature [1], [7], [10], [12]–[16]. It is also well grounded in literature that lightning bolts; essentially large-scale arcs, behave as fractals and demonstrate chaotic properties [17]–[20].

With arcs displaying inherently chaotic features, it may

be possible to use fractal theory, a branch of modern chaos theory, to detect arc failures. Fractal methods are already commonly employed in the field of medical electronics wherein fractal dimensions are being used to detect that the body is failing, before the patient shows visible signs [21]–[23]. In monitoring the fractal dimension of the arc it may be possible to indicate the presence of a DC series arc failure within a power electronics based distribution system.

This paper proposes a novel method of detecting ongoing DC series arc failures by monitoring the fractal dimension of the supply current and power waveforms of the arcing circuit. Section II describes the experimental method used to produce consistent DC series arc failures and additionally outlines the process of calculating the Windowed Fractal Dimension (WFD) for arc monitoring. Section III presents the results of applying the WFD method to representative DC arc failure data. Section IV provides a discussion of the experimental results. Finally, Section V concludes the paper, presenting the key findings of the work done and discussing future research.

II. Experimental Method

A. Series Arc Generation

In order to generate data representative of an arc failure, an experimental rig was constructed to repeatably produce DC series arc failures. This experimental setup consists of a controlled 42V DC supply voltage connected to a resistive-inductive load and then returned to ground through a drawn arc generator as seen in Fig. 1. The drawn arc generator shown in Fig. 2 consists of two electrodes and a stepper motor, allowing the position of the electrodes to be remotely controlled during normal circuit operation.

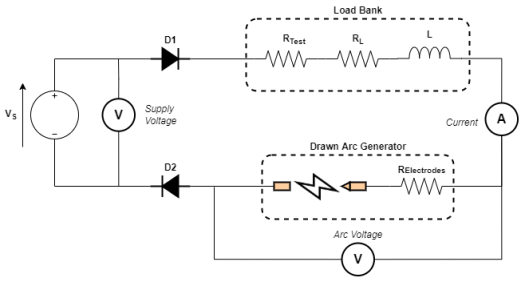

Fig. 1: DC Series Arc Generation Rig Circuit Diagram

To initiate an arc, the circuit is energised and allowed to reach steady state with the electrodes touching. Once steady state has been achieved, the electrodes are separated at a constant speed, causing the current to drop sharply as the circuit becomes open. The inductive load resists the sudden change in current and produces a reverse-voltage across the airgap between the electrodes. This in turn ionises the air and produces an arc between the electrodes that maintains the current flow within the circuit [2], [8], [12].

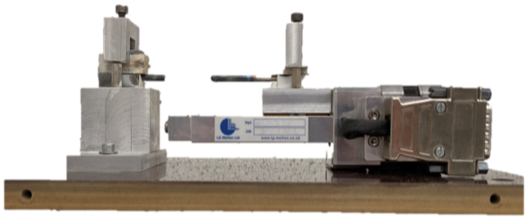

Fig. 2: Drawn Arc Generator

A series of experiments were performed to gather data representative of a DC series arc failure across a range of different failure conditions. Eight different experimental setups were explored and repeated, covering different electrode separation speeds, electrode stopping distances and electrode materials as can be seen in Table I. Each of these experimental setups were repeated 10 times and used the same electrical parameters, with a 42V DC supply and a 10.7Ω, 15.2mH series load.

TABLE I: Arc Experimental Setup Conditions

Setup Number	Electrode Material	Separation Speed, [mm/s]	Stopping Distance, [mm]
1	Tungsten	2.5	2
2	Tungsten	2.5	1
3	Tungsten	2.5	3
4	Tungsten	2	2
5	Tungsten	1.5	2
6	Tungsten	3	2
7	Tungsten	3.5	2
8	Copper	2.5	2

For all experiments, supply and arc voltage were measured using differential probes, and supply current with a hall-effect current clamp; sampled at a rate of 500kHz using an NI9222 DAQ, over a 10-20s period dependant on electrode speed.

The supply voltage, supply current and arc voltage traces were found to be consistent with those found in other literature [8], [10], [12], [24]–[26]. This is illustrated in Fig. 3 using data from Setup 8 outlined in Table I. Note that in Fig. 3 and Fig. 4 supply voltage has been plotted between 40V and 50V to better illustrate how the waveform changes throughout the arcing period. Using these traces, Ohm's Law and Kirchoff's Voltage and Current Laws, separate traces were created for supply power and impedance, alongside load voltage, power and impedance for further testing.

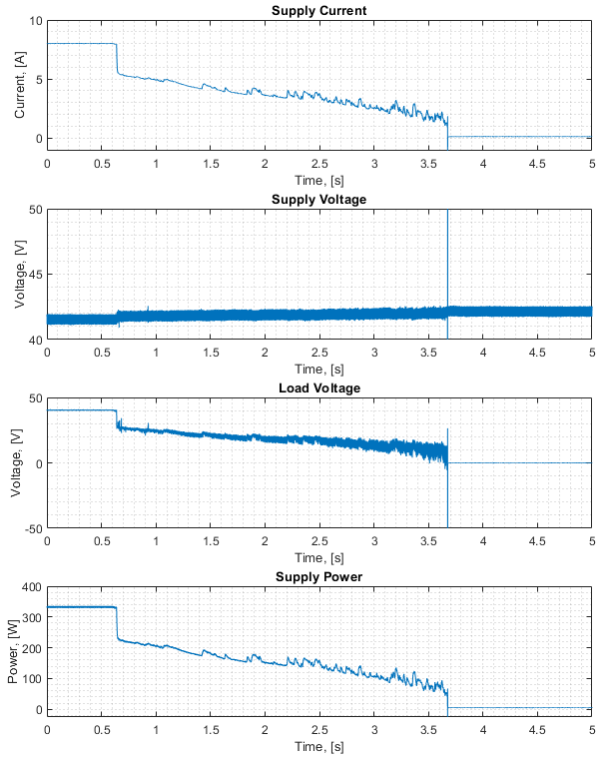

Fig. 3: Typical DC Series Arc Waveforms, Experimental Setup 8, from t = 0s to t = 5s

B. Calculating Windowed Fractal Dimension (WFD)

Before a fractal dimension transformation can be performed to determine the fractal dimension of the arcing waveform, a degree of signal conditioning is necessary. Consider a sampled, discrete time signal S(n) with N total samples:

$$S(n) = [s_1, s_2, \ldots, \ s_N] \tag{1}$$

For the sampled signal, S[n], the fractal dimension should be calculated for a short-time window of N_{win} samples, where $N_{win} < N$. This windowing allows the short-time sections of the sampled signal to be analysed in sequence, rather than the waveform as a whole.

As fractal methods are heavily dependent on waveform geometry, the window function should not distort the shape of the original waveform [17], [19]. To this end, a simple rectangular windowing function was selected. Multiplying the original signal, S(n), by the rectangular window function, W(n), yields a windowed form of the original signal, h(n).

$$\begin{gathered} W(n) = [w_1, w_2, \ldots, \ w_{N_{win}} \ ] = 1 \\ for \quad 1 < n < N_{win} \end{gathered} \tag{2}$$

$$\therefore h(n) = S(n)W(n) = [s_1, s_2, \ldots, \ s_{N_{win}}] \tag{3}$$

Each windowed section is then normalised between 0 and 1. This is repeated for both the signal datum on the ordinate axis, h(n), and the corresponding time datum on the abscissa, t(n), mapping it to a unit square. Normalising both axis' removes any skew in the shape of the data based on the weighting of the units and is necessary to compute the fractal dimension [27].

$$h_{Norm}(n) = \frac{(h - h_{min})}{(h_{max} - h_{min})} \tag{4}$$

Repeating the windowing and normalisation process for the corresponding time vector t(n), yields:

$$\begin{gathered} t(n) = [t_1, t_2, \ldots, \ t_N \ ] \rightarrow t_{Norm}(n) \\ for \quad 1 < n < N_{win} \end{gathered} \tag{5}$$

The fractal dimension of the normalised signal window can then be calculated using the Sevcik method [27]. First the Euclidean length of the normalised signal window is calculated as described in (6):

$$L = \sum_{(n=1)}^{(N_{win}-1)} \sqrt{\begin{gathered}((t_{Norm}(n+1) - t_{Norm}(n))^2 \ \ldots \\ + (h_{Norm}(n+1) - h_{Norm}(n))^2\end{gathered}} \tag{6}$$

The fractal dimension, D, can then be calculated for the current windowed signal portion using the Euclidean length, and the number of steps, $N' = N_{win} - 1$, as described in (7).

$$D = 1 + \frac{\ln(L)}{\ln(2 \cdot N')} \tag{7}$$

With the fractal dimension calculated for the current window, the window can then be shifted by N_{win} samples, and the process repeated to produce the windowed fractal dimension (WFD) for a signal of fixed length, N, or run continuously for online monitoring of a live system.

III. Experimental Results And WFD Application

The WFD method described in Section II-B was then applied to the current, voltage, power, and impedance waveforms for both the supply and load side, across all the eight experimental setups and the repetitions documented in Table I.

Shown in Fig. 4 and Fig. 5 are the Windowed Fractal Dimension of the current, voltage and supply power waveforms, as these showed the most obvious change during the arcing period from t = 0.6s to t = 3.7s . The data illustrated in Fig. 5 is recorded from Setup 8 to mirror that

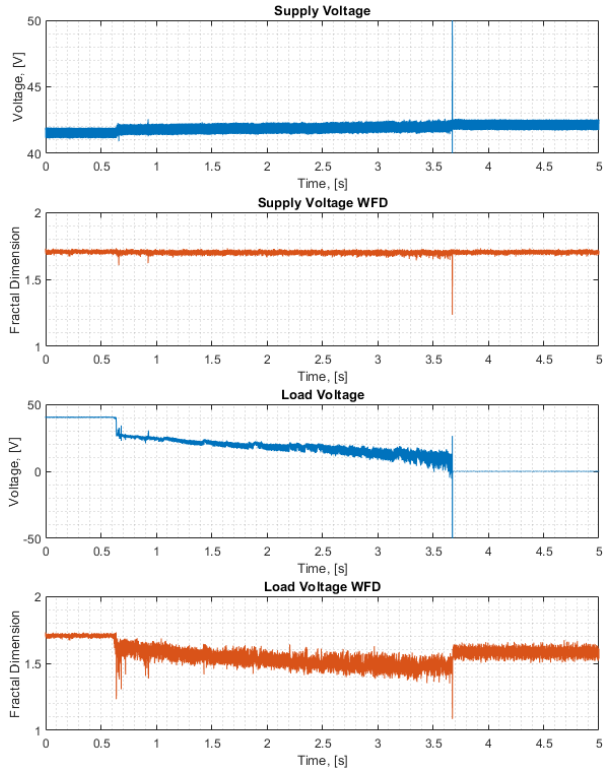

Fig. 4: Comparison of Supply Voltage and Load Voltage with Windowed Fractal Dimension (WFD), Experimental Setup 8, from t = 0s to t=5s

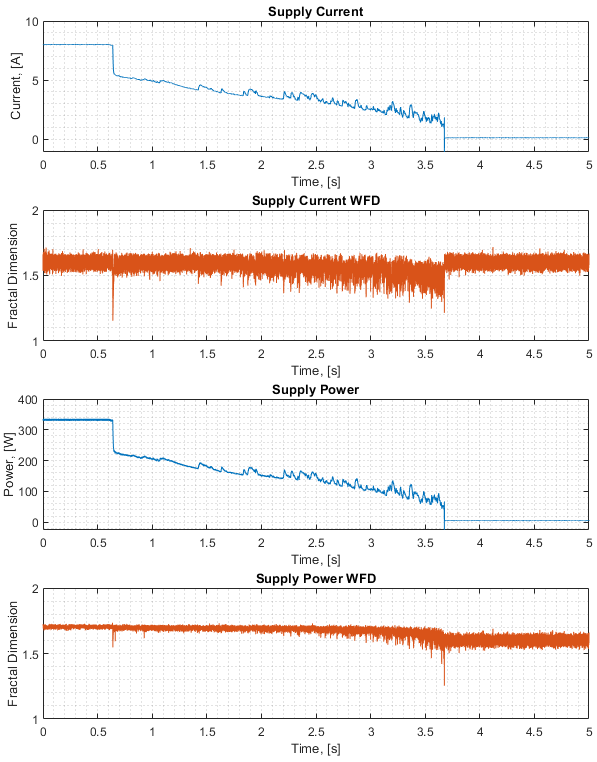

Fig. 5: Comparison of Supply Current and Power with Windowed Fractal Dimension (WFD), Experimental Setup 8, from t = 0s to t=5s

shown in Fig. 3

Both Fig. 4 and Fig. 5 show traces with a clear change in fractal dimension during the arcing period that is consistent throughout the entire arc. The change in WFD observed in the load voltage WFD trace in Fig. 4, is not seen in the corresponding supply voltage WFD trace. This is because the WFD algorithm responds to chaotic changes in signal geometry, and the supply voltage trace seen in Fig 3 and Fig 4 produces only a slight change during the arcing period. The minor change seen is the response of the controlled voltage source to the reduced load current through the circuit as the impedance of the arc is introduced.

In the absence of an arc, the supply voltage WFD is maintained at a resting value of around 1.7. Here the WFD algorithm is showing a value for fractal dimension representative of the switching in the switched-mode power supply (SMPS) used to supply the test circuit. The switching introduces an inherent non-linearity to all supply waveforms and as such any SMPS supplied circuit will show an increased resting value of fractal dimension.

It can be seen in Fig. 5 that the fractal dimension returns to its pre-arc resting value after the arc finishes at t = 3.7s for the supply current WFD waveform, but not for the supply power WFD. This is due to the influence of the supply voltage waveform used to generate the supply power. As the circuit becomes open after arc collapse, the influence of the current reduces, and the minor changes in supply power WFD when $t > 3.7$ are instead reflections of the supply voltage WFD at the output of the SMPS supplying the experiment.

The same effect is seen with the load voltage WFD trace in Fig. 4, where, as the circuit becomes open after $t >= 3.7$s, the value of load voltage WFD matches that of the supply voltage WFD. With the circuit open and no current flow there is no change in voltage across the load and therefore load voltage and supply voltage become equivalent, explaining the transition in resting WFD seen before and after the arc.

In calculating the WFD for each waveform the target was to observe a change in WFD of +/- 10% or more during the arcing period that clearly distinguishes the arc from normal circuit operation. The results of this experimentation are recorded in Table II and show that a significant change

was seen in all WFD waveforms, excluding supply voltage. Here, any change noted as significant is marked with a 'Y', and insignificant changes with a 'N' . The lack of significance seen in supply voltage is to be expected as the controlled voltage supply maintains a near constant output, and does not reflect the chaotic behaviour of the arc well enough to be picked up by the WFD algorithm.

TABLE II: Significance of Windowed Fractal Dimension (Y/N), Showing Consistent Change of $\pm 10\%$ during arcing period in $1 <$WFD< 2 range, by Setup Condition

	Setup Number							
Measurand	1	2	3	4	5	6	7	8
Current	Y	Y	Y	Y	Y	Y	Y	Y
Supply Voltage	N	N	N	N	Y	Y	Y	N
Supply Power	Y	Y	Y	Y	Y	Y	Y	Y
Supply Impedance	Y	Y	Y	Y	Y	Y	Y	Y
Load Voltage	Y	Y	Y	Y	Y	Y	Y	Y
Load Power	Y	Y	Y	Y	Y	Y	Y	Y
Load Impedance	Y	Y	Y	Y	Y	Y	Y	Y

IV. Discussion

Whilst the WFD method can successfully identify a DC series arc failure using fractal theory, producing a measurable change, more work is required to determine the robustness of the method for use in circuit protection. Additional experimentation should be performed to test the algorithm performance in the presence of load changes and non-linear loads, in addition to more complex electrical loads and transmission line lengths. The WFD algorithm also needs an extension to produce circuit interruption in the event of an arc, allowing it to be compared to the strengths and shortcomings of existing arc failure detection methods.

Further to this, additional methods of generating an arc failure should be explored to determine the effectiveness of WFD algorithm to different arc ignition types. Options include arcs introduced on a shaker table, or through forced destruction of a component, providing analogues to continuous arcs from vehicle vibrations and conductor contact, to arcs forming spontaneously through component or conductor failure.

It may be possible to improve the response of the WFD algorithm by re-testing using arc fault data with a greater current bandwidth. The Hall-Effect current probe used in the experiments described in this paper has a bandwidth of 5kHz, meaning that higher frequency components of the signal may have been occluded. Similarly, there is evidence to suggest that arc failures introduce high frequency interference [28], [29], and recapturing test data at a higher sampling rate may allow this interference to be observed by the WFD algorithm for detection. Whether this would improve or worsen the WFD response is not yet fully understood.

A point to consider in further work is the response of the WFD algorithm to the switching and non-linearity of power supplies to the test circuit. Changes in resting fractal dimension have already been shown in the supply power WFD in Fig. 5 and could become an issue as the test circuit becomes more complex, with more power electronic converters introduced. Further testing using a constant battery supply or SMPS with the switching frequencies filtered out will provide insight into how different power sources affect the WFD. During this testing, it is important to ensure that any filters introduced do not also filter out interference produced by the arc itself, as this would lessen the effectiveness of the WFD method.

Another option is further processing or filtering of the WFD output itself. As can be observed in the load voltage and load voltage WFD in Fig. 4, the arc ignition at t=0.6s produces not only a step change in magnitude for the WFD output, but also an increase in peak-peak noise on the waveform. Application of an active filtering method with a ongoing feedback, such as a Kalman filter, would work to reduce the peak-peak noise at the WFD output and make the change in fractal dimension when arcing easier to distinguish. It is important to note however, that whilst filtering might improve the chances of arc detection it would adversely affect the value of fractal dimension at the output, such that it is no longer representative of the true value of fractal dimension for the system.

Methods should also be explored to extend the WFD method to include a means of detecting the arc from the WFD output, and produce a reliable digital logic output trigger. This could then be used to communicate with peripheral electronics and warn users or trip circuit protection as appropriate. Suitable options could include a simple threshold-based detection scheme, similar to the $\pm 10\%$ condition outlined in Table. II, producing a trigger when the fractal dimension changes by a fixed amount; or, a leaky integration centered on the resting, pre-arc value of fractal dimension, summating any changes in the fractal dimension until they are sufficient to indicate an arc fault.

V. Conclusions

This paper has proposed a novel method to detect DC series arc failures using fractal theory by measuring the fractal dimension of short-time signal windows. A method to produce the windowed fractal dimension has been described and results show that a significant ($>10\%$) change in fractal dimension occurs throughout the period

of the arc failure. This yields strong evidence that fractal theory can provide a means of arc detection.

Future work should consider the impact of switched-mode power supplies on the WFD algorithm, ensuring that any filtering or switching is taken into account as the method is tested over a larger range of load conditions, and extended to produce a robust method of arc fault circuit interruption. Additional methods of arc ignition and the impact these have on the WFD output should also be explored. Work to develop the algorithm further should include the application of a simple detection schema to the WFD output to produce a logical output trigger on arc detection, giving a clear indication of arcing within the circuit.

ACKNOWLEDGMENTS

This work was supported by the UKRI Engineering and Physical Sciences Research Council. The author would also like to acknowledge the support of Prof. Serhiy Bozhko, whose feedback encouraged this publication.

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The Effects of Relative Humidity on DC Series Arc Generation and Detection

Danny Seeley
Power Electronics, Machines and Control Group
The University of Nottingham
Nottingham, United Kingdom
danny.seeley@nottingham.ac.uk

Mark Sumner
Power Electronics, Machines and Control Group
The University of Nottingham
Nottingham, United Kingdom
mark.sumner@nottingham.ac.uk

David W.P. Thomas
George Green Institute for Electromagnetics Research
The University of Nottingham
Nottingham, United Kingdom
dave.thomas@nottingham.ac.uk

Stephen Greedy
George Green Institute for Electromagnetics Research
The University of Nottingham
Nottingham, United Kingdom
steve.greedy@nottingham.ac.uk

***Abstract*—Electrification of aircraft, ships and rail has led to an increased use of DC power networks and at higher operating voltages. Arc faults in these higher voltage systems have increased energy levels and can potentially cause significant damage and destruction. These DC power systems are used across a wide range of environmental conditions, and there is a need to understand how the environment affects arc generation and arc detection. Experimental results indicate a clear difference in arc behaviour between humid and dry environments, suggesting a reduction in the transient features used for arc detection and an increased arc duration, resulting in a heightened risk as relative humidity decreases. Results also indicate a reduced response from arc detection algorithms from arcs in drier environments. This has highlighted the need for additional work regarding the change in arc characteristics with varying environmental conditions. and the impact this has on detection and power network protection.**

***Index Terms*—DC Series Arc, Arc Generation, Arc Protection, DC Protection, Humidity**

I. Introduction

The growth of renewable energy sources, battery energy storage, and the electrification of mechanical systems within more electric automotive, aircraft and shipping industries has led to an increased use of DC circuit architecture at higher voltages such as 400V. There is an increasing need for reliable circuit protection schemes, as the consequences of an electrical failure can extend from financial damages to destruction of infrastructure and the loss of human life [1]–[3].

Series arc faults within DC systems are a specific concern as these faults do not trip circuit over-current or surge protection devices. These arc faults result in a discharge of electricity through the air and pose a serious threat to system reliability, damaging nearby components and conductors whilst also presenting a major fire hazard [3]–[5]. The most common cause of arc failure is the degradation or damage of components or conductors, causing a break in the circuit where an arc can form. This most often occurs where circuit elements are exposed to adverse environmental conditions, excessive movement, vibration, or aging that will deteriorate cable insulation and connectors. The introduction of DC-DC power converters, longer transmission lines and greater operating voltages within more-electric aircraft, ships and solar application have expanded the scope of operating conditions for these DC networks, and by extension the range of challenges for arc detection [1], [6].

Application of DC power networks in electric aircraft, ships and solar applications has exposed these systems to more hostile and potentially damaging environmental conditions that could incite an arc failure, and the need to understand how environmental factors impact arc generation has developed [2], [7], [8]. In their 2022 review paper, Psaras et al remarked the distinct lack of research into how environmental conditions influence arc failure, and highlighted the need for additional work in this field with the development of more-electric aircraft to simulate the environmental conditions experienced during flight [1]. Specifically mentioned was the lack of any reported testing into how relative humidity (RH) affects arc failure. The difference in ambient humidity seen between electric aircraft and ship power systems could potentially create conditions more favorable for arc generation, and would therefore require additional consideration during the design and commissioning stages.

This work was supported by the Engineering and Physical Sciences Research Council (EPSRC).

This work aims to show how different environmental conditions can affect DC series arc generation, and how those changes then influence arc detection. DC series arcs are experimentally generated across a range of relative-humidity values, scaling from 20-98% RH, at fixed temperature and an increased supply voltage of 400V representative of more-electric ship, aircraft and solar farm bus voltages.

The remainder of the paper is organised as follows: Section II documents the experimental setup and how series arcs were reliably reproduced for the experiments describes. Section III highlights the key results of the experiments, showing changes in arc behaviour and how this impacts arc detection using the Windowed Fractal Dimension (WFD) method [9]. Section IV provides a discussion of the results presented, with Section V giving conclusions and suggestions for future work.

II. Generation of Series Arcs at Fixed Humidity

An arc generation rig was constructed to produce DC series arc failures consistently with a 400V supply voltage and a 42Ω, 15.2mH resistive-inductive load. Arc ignition is achieved using a drawn arc generator shown in Fig. 1 consisting of two 2mm ϕ tungsten electrodes that can be remotely separated with a stepper motor to open the circuit and achieve arc ignition. Drawn arcs burn until the electrode separation is great enough that the electric field can no longer support the arc, or until thermal effects cool the plasma sufficiently for the arc to collapse. As such, arcs can be extinguished by rapidly separating the electrodes.

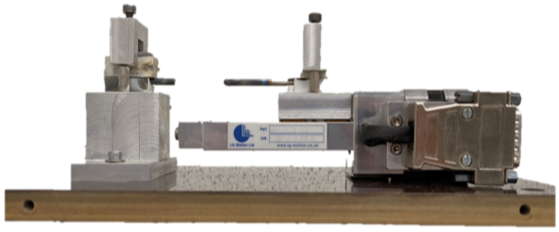

Fig. 1: Drawn Arc Generator

The arc generator in Fig. 1 was placed inside a Xi'an LIB THR10-150C environment chamber, capable of controlling and monitoring both internal temperature and relative humidity to a precision of 0.1°C and 2.5% RH. As RH is temperature dependant, a fixed operating temperature of 60°C was selected for all preliminary experiments, as this was the lowest temperature allowing for use of the full RH range without condensation.

Electrode geometry has been shown to influence arc generation, and should be kept as consistent as possible between testing [1], [4], [10]. As such, the electrodes used in this work were ground longitudinally such that the mobile electrode came to a sharp point, contacting a flat surface on the stationary electrode as show in Fig. 2. The electrodes were cleaned of oxide build up between each experiment and re-ground regularly to maintain their set geometry and ensure consistency between experiments.

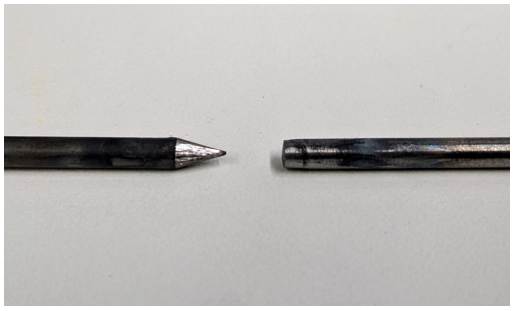

Fig. 2: Arc Generator Electrodes

The arc generator was connected to the circuit shown in Fig. 3, with a 400V supply voltage, constant 2mm/s electrode separation speed and fixed temperature of 60°C. Each test records supply and load voltage, with two measurements of series current using both a Hall-Effect (HE) probe and a Rogowski coil current transducer (RCCT) sampling at 2MHz with a Picoscope 5000 Series oscilloscope.

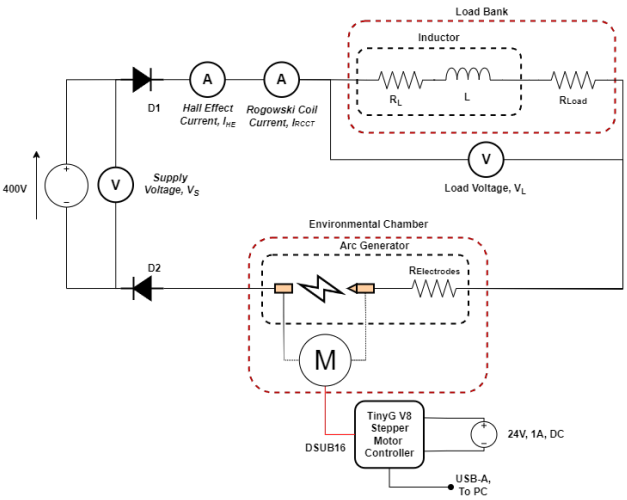

Fig. 3: Arc Generation Rig Circuit Diagram

III. Experimental Results

A. Impacts on Arc Generation and Arc Characteristics

Tests using the setup described in Section.II were conducted at 10% RH increments from 20% to 98% RH with five repeats at each increment. Shown in Fig. 4 are three HE current traces captured at 20%, 50% and 90% RH respectively to highlight the differences in arc behaviour in each case.

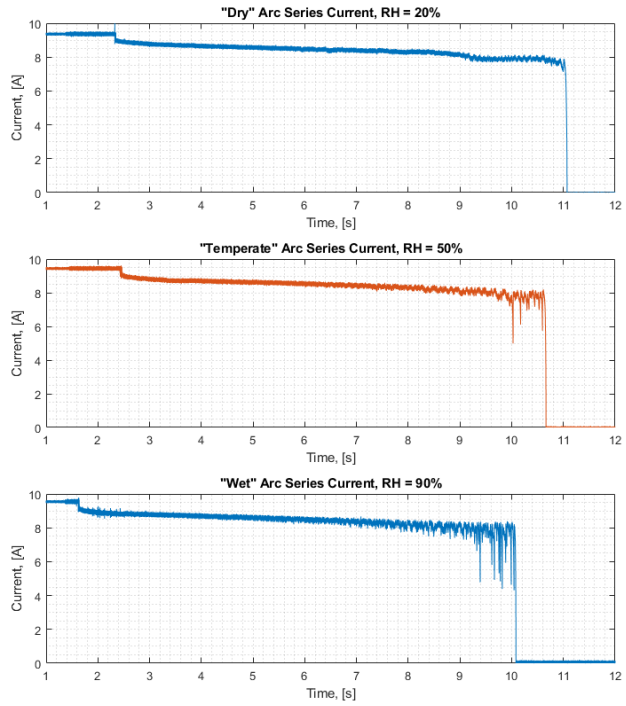

Fig. 4: Comparison of HE Series Current at 20%, 50% and 90% RH

It can be seen in Fig. 4 that there is an reduction in arc duration as relative humidity increases. In all experiments, arcs were controlled to ignite at approx. t = 2.25s, with the electrodes continuing to separate at uniform speed. In Fig. 4 the 'wet' arc collapses at t = 10.07s and the 'dry' arc at t = 11.06s with a 0.99s difference in arc duration. This translates to a 1.98mm difference in electrode separation at arc collapse. A similar reduction in arc duration as RH Increases is seen across all results, and provides an indication that arcs in drier environments can reach a greater arc lengths before collapsing.

Fig. 5 provides further evidence, comparing the average arc duration for each RH value across the full range of humidity values tested. The change in arc duration can be observed across all arcs captured, with a greater reduction occurring as RH humidity increases past 80%. The reduction in arc duration seen may result from the increased thermal conductivity of the air at higher relative humidity, leading to increased cooling of the arc plasma and earlier arc collapse [11]. Longer-lived arcs pose a more severe risk to system reliability as the arcs have a bigger window in which to short to neighbouring conductors, components or cladding and start electrical fires. As such, these preliminary results indicate there may be a heightened risk from arcs in drier environments.

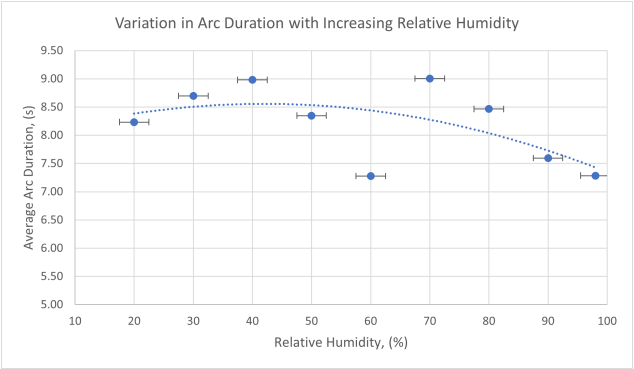

Fig. 5: Variation in Arc Duration with Increasing Relative Humidity

Also observable in Fig. 4 is the change in the transient features of the arc as relative humidity increases. These current transients result from the changing impedance of the arc plasma as the arc length varies, whilst moving chaotically through the air. These transients typically become larger and more obvious at greater electrode separations and arc lengths. In Fig. 4 the current transients seen at arc collapse at t>=9s in the 'wet' arc trace are of a greater magnitude than those seen from t>=9s in the 'dry' and 'temperate' arc traces. Similar differences in current transient magnitude can be seen at arc ignition around t=2.25s for all traces, with the 'wet' arc displaying slight transient features shortly after ignition not seen in the other traces.

One possible explanation for this behaviour is that at a higher RH the air may have a higher resistivity than at lower RH values. This would be reflected as a larger change in arc impedance for a fixed change in arc length, and would therefore explain the larger deviations in series current for the 'wet' arc. The amplified transient features of the 'wet' arc may serve as useful tool for arc detection, reflecting changes in the arc itself without mimicking other normal circuit behaviour that could trigger false positives. By contrast, the lack of transient features in the 'dry' arc may make it more difficult to distinguish from events such as a step load change, resulting in a missed detection.

The increased arc impedance suggested by the larger transients in the 'wet' arcs current trace is in direct contrast to what would be expected given the shorter arc duration. With a shorter lived arc the electrodes separation is also smaller, and thereby the length of the arc itself is smaller. The expected result is that a reduced arc length would be made up of less arc plasma and the arc would therefore have less impedance, however the results in Fig. 4 instead indicate an increasing arc impedance.

To better understand how arc impedance is changing with humidity, in Fig. 6 the average arc impedance at the point of arc collapse is plotted alongside average arc duration with both compared to relative humidity. The results shown reaffirm what was seen in Fig. 4 with arc impedance increasing with relative humidity despite the reduction in arc duration and drawn arc length. These results suggest that the change in resistivity of the air at higher humidity has a significant influence over the electrical characteristics of arc itself, resulting in a more dynamic arc waveform with more obvious transient features that may be useful for arc detection. Conversely, arcs in drier environments have been shown to display less transient features and be potentially more challenging for arc detection.

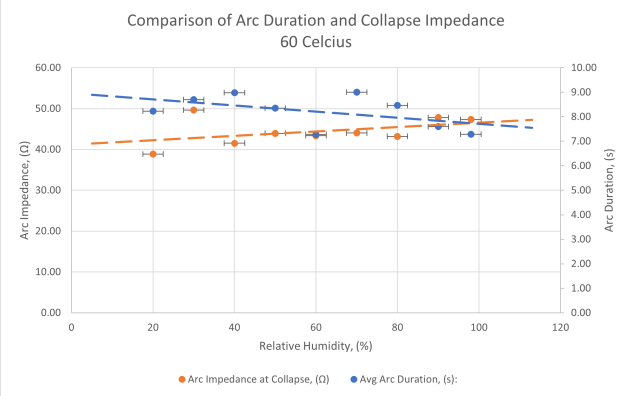

Fig. 6: Comparison of Arc Duration and Collapse Impedance at 60°C

An extension to the results above is to repeat earlier experiments at different fixed temperatures to observe if there is any further change in arc behaviour. Preliminary results from a series of several repeats conducted at 100°C at 20%, 50% and 90% RH can be seen in Fig. 7 and Fig. 8. Additional testing is required to cover the full RH range, however initial results show trends matching those seen in the earlier 60°C testing. Fig. 7 shows the a similar reduction in arc duration with increasing humidity as seen in Fig. 4, and the comparison of arc duration and collapse impedance in Fig. 8 matches that seen at 60°C in Fig. 6.

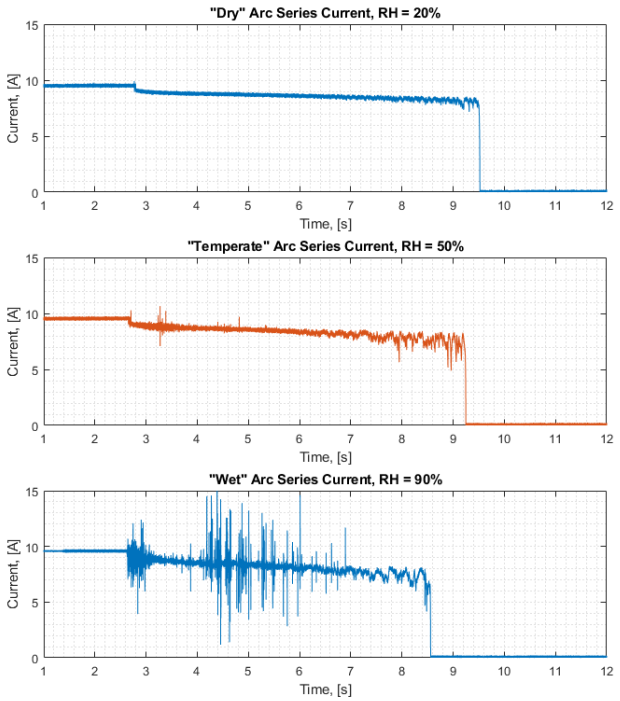

Fig. 7: Comparison of HE Series Current at 20%, 50% and 90% RH at 100°C

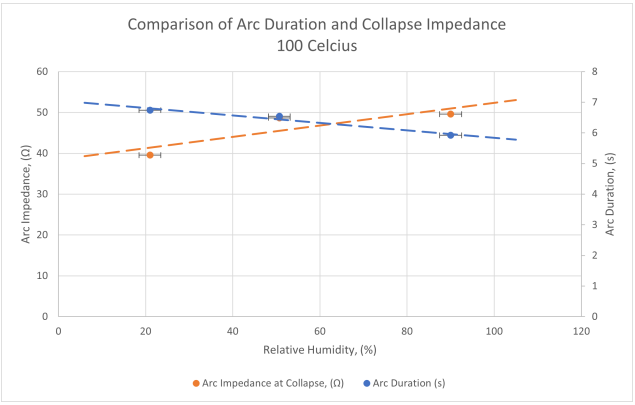

Fig. 8: Comparison of Arc Duration and Collapse Impedance at 100°C

More drastic changes are observed in the transient behaviour of the arcs seen in Fig. 7 as relative humidity increases. All of the arcs recorded at 90% RH displayed very large current transients both at ignition and throughout the arc lifetime, several of which experienced very early arc collapse around 1s after arc ignition. Additional work at higher temperatures is required to better understand these transient events, though it is possible that the higher ambient temperature during arcing has caused increased convection flow in the air and a greater disturbance of the

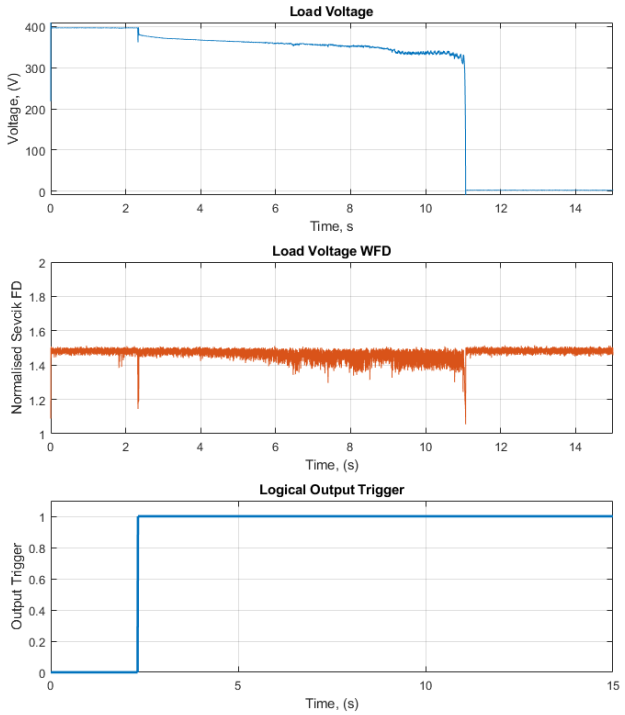

Fig. 9: Arc Detection using WFD of 'Dry' Arc Load Voltage Waveform at 20% RH at 60°C

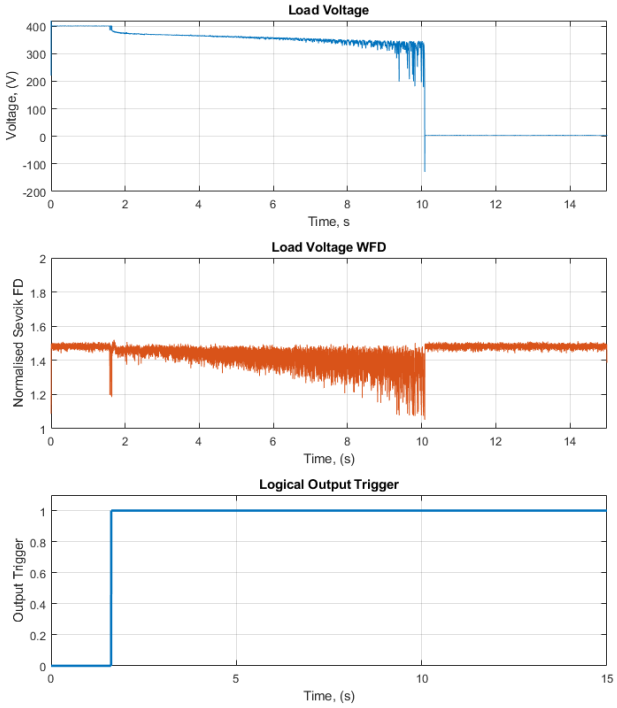

Fig. 10: Arc Detection using WFD of 'Wet' Arc Load Voltage Waveform at 90% RHat 60°C

arc plasma. The rapid changing of the arc length, coupled with the observed increase in arc impedance at higher relative humidity could potentially result in the increased transient behaviour seen in the 100°C arcs in Fig. 7.

B. Arc Detection with Windowed Fractal Dimension (WFD)

To understand how changing relative humidity impacts arc detection, all experiments described were processed using the Windowed Fractal Dimension (WFD) arc detection algorithm. In this approach, short-time windows of the arcing load voltage are normalised and their fractal dimension (FD) computed to indicate the onset of fractal noise superimposed onto the waveform by the arc itself. Significant changes in fractal dimension compared to normal behaviour observed before the arc is then used to discriminate arcs from non-arcing conditions [9]. For these experiments, a ±10% change in FD was used as the threshold for arc detection.

Shown in Fig. 9 and Fig. 10 are the load voltage and corresponding WFD waveforms for the 'dry' and 'wet' arcs at 60°C seen previously in Fig. 4, alongside an output trigger to indicate the point of arc detection. In both figures 9 and 10, arcs were detected from the WFD within 1.5ms of arc ignition and show continuous change in fractal dimension whilst the arc is sustained. The change in FD increases in proportion to the arc noise superimposed on the load voltage by changing arc impedance. This can be observed to be much larger in the 'wet' arc trace in Fig. 10, and provides a better discriminator for arc detection when compared to the smaller changes observed in the 'dry' arc shown in Fig. 9.

These tests were repeated for the load voltage traces of the 100°C 'wet' and 'dry' arcs as presented earlier in Fig. 7, and can be seen in Figures 11 and 12. These show the same features as previously seen in Fig. 9 and Fig. 10 with a change in fractal dimension increasing with arc duration, alongside a larger change at higher humidity in the 'wet' arc trace. Noteworthy however is the difference in both 'wet' arc traces seen in Figures 10 and 12, with the 100°C arc seen in Fig. 12 displaying a larger initial step change in fractal dimension at arc ignition around t=2.25s, but a smaller change in fractal dimension at arc collapse. These differences suggest that the increased temperature whilst at higher relative humidity may also have an impact on the transient features of the arc that aide arc detection. Additionally, as the changing fractal dimension represents a change in superimposed arc noise caused by varying arc impedance, the greater step change in fractal dimension at arc ignition in Fig. 12

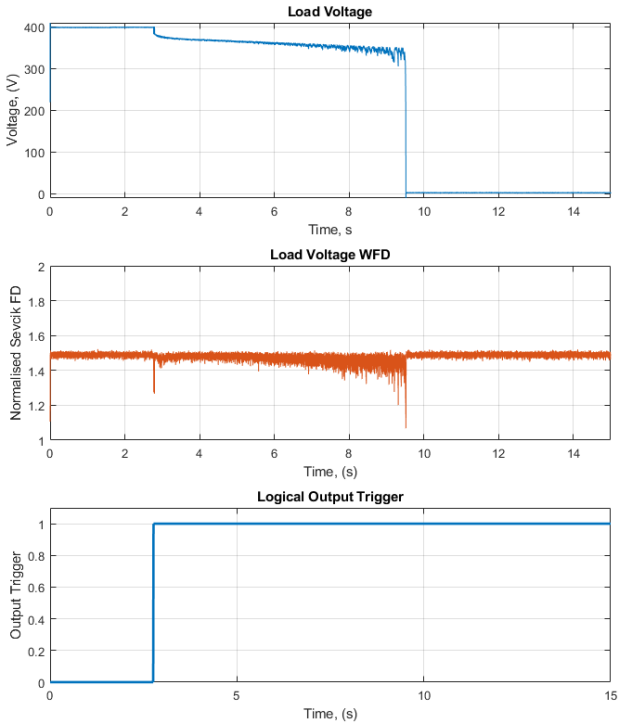

Fig. 11: Arc Detection using WFD of 'Dry' Arc Load Voltage Waveform at 20% RH at 100°C

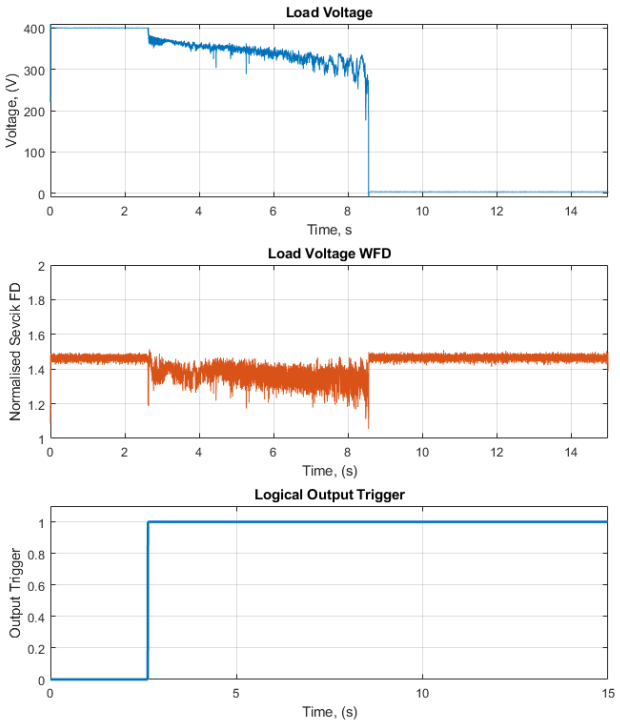

Fig. 12: Arc Detection using WFD of 'Wet' Arc Load Voltage Waveform at 90% RH at 100°C

can be interpreted as the 100°C arc having higher initial arc impedance than it's 60°C counterpart. This supports the earlier conclusion that arc impedance increases with relative humidity despite reduced arc duration, and indicates that the increased ambient temperature may also influence the arc characteristics, potentially through a varying arc impedance or increased movement of the air and arc plasma.

The WFD detection algorithm was applied to all 48 data captures spanning the full humidity range tested and achieved a detection accuracy of 100%, distinguishing the arc from normal, pre-arc behaviour in every test. In each case, the magnitude of the changes in fractal dimension increased proportionally to arc duration, produced the largest changes at the most dynamic points of the arc (ignition and collapse), and showed larger voltage and WFD transients at higher relative humidity as seen in previous results. Fig. 13 shows the average percentage change in fractal dimension at the point of arc ignition from the pre-arc resting value calculated for all repeats at each different relative humidity value, showing a clear increase in WFD at arc ignition with increasing relative humidity. Together, Figures. 9, 10 and 13 provide evidence to suggest that arcs are easier to detect in a more humid environment, displaying more exaggerated features when compared to arcs in a drier environment possibly due to increased air resistivity and therefore arc impedance.

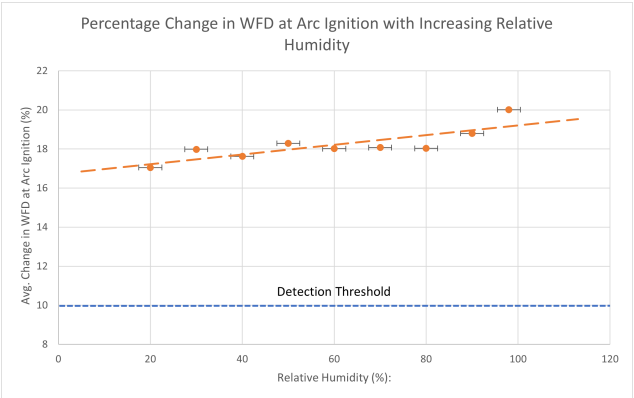

Fig. 13: Percentage Change in WFD at Arc Ignition with Increasing Relative Humidity

IV. Discussion

Results presented in Section.III have demonstrated how the characteristic features of a DC series arc failure change with increasing relative humidity and also how this impacts the features used for arc detection using an established arc detection method.

Figures. 4 and 7 illustrate that the transient features of the arc, particularly just before arc collapse, are of greater magnitude at a higher relative humidity and only become larger with an increased ambient temperature. Similarly, Figures. 9, 10, 12 and 11 have highlighted that the greater magnitude transient features seen at higher RH values are reflected as a greater change in WFD, becoming a more reliable discriminator for arc detection. This is demonstrated directly in Fig. 13 where it can be seen how the change in WFD increases proportionally to increasing RH. Collectively, results indicate that there are enhanced magnitude arc features seen at higher relative humidity values that directly improve the chances of arc detection by providing a greater contrast to normal, non-arcing conditions. Conversely, this suggests that there is an increased risk associated with arc fault protection in drier environments as the features that can be used for identifying the fault are smaller in magnitude and produce a reduced response from the tested detection algorithm. They may therefore elude some detection methods and result in component damage or electrical fires.

Highlighted in Fig. 4, Fig. 7 and separately Fig. 5 is the reduction in arc duration with increasing relative humidity. All the arcs recorded in this work are drawn arcs, with the electrodes continuing to separate at a uniform speed of 2mm/s irrespective of other experimental conditions. This means that a reduced arc duration also infers a reduced electrode separation at arc collapse, and by extension a reduced arc length. The reduction in arc duration and length is potentially due to the increased thermal conductivity of the air at higher relative humidity values resulting in increased cooling of the arc and its earlier collapse [11]. Another possible reason for the reduction in arc duration could be increased arc impedance. Figures 6 and 8 show an increased arc impedance at higher relative humidity that may be indicative of greater air resistivity at larger values of RH. The additional resistivity may limit the maximum length of the arc by causing the arc to reach a larger impedance at a shorter arc length, such that the electric field between the electrodes can no longer produce a sufficient current flow to keep the arc burning. Irrespective of the mechanism causing it, the increased arc duration and arc lengths seen in 'dry' arcs at lower relative humidity indicate that they can potentially be much more dangerous than arc in a wetter environment at higher RH. The 'dry' arcs are sustained for longer, giving more opportunity to start electrical fires, and the increased arc length before collapse heightens the risk that the arc will short to neighbouring conductors and components and damage them.

The increased impedance and reduced arc duration at higher relative humidity observed in Fig. 6 and Fig. 8 appear to directly contradict each other when considering that all arcs tested are drawn arcs separating at a uniform speed. The expected result is that the reduced arc duration produces a smaller electrode separation and shorter arc length, meaning a reduced arc impedance, rather than the greater impedance shown. What can be understood from these results is that the increasing relative humidity has a greater impact on arc impedance than the changing length of the arc, either directly or through a combination of other factors. This may again be the result of increased cooling of the arc plasma caused by the improved thermal conductivity of the air at higher humidity causing additional cooling of the arc and earlier collapse, alongside increased air resistivity producing an increased arc impedance at that time. Future work in this area could include additional measurements of the gaseous environment containing the arc in an attempt to quantify the resistivity of the air and clarify the reasons for this seemingly contradictory behaviour.

Another possible avenue of future work is repeating the experiments varying relative humidity described in this work at different fixed temperature values. Preliminary experimentation in this area has already begun, with select repeats being conducted at 100°C to observe the changes to the characteristic features of the arc. Figures 7, 11 and 12 document how arc features change at 100°C indicate that for the same fixed relative humidity the transient features of the arc have an increased magnitude versus their lower temperature 60°C counterparts in Fig. 4, Fig. 9 and Fig. 10. This is reflected both in the physical features of the arc; with larger current and voltage transients seen at higher temperatures, and in the response of the WFD detection algorithm, showing a larger initial change in fractal dimension. These results provide evidence to suggest that a change in ambient temperature also has a significant effect on the behaviour of the arc, and additional experiments should be conducted to observe how the arc characteristics change at different fixed temperatures with changing humidity, alongside separate work fixing relative humidity and varying ambient temperature.

V. Conclusions

This paper set out to describe the effects of changing relative humidity on DC series arc generation and detection. Results have highlighted several key features that differentiate arc faults within dry and humid environments, for a fixed temperature, load and supply voltage; these include:

- Arcs have an increased lifetime and arc length in drier environments.
- Arcs in humid environments show an increase in arc impedance at arc collapse, despite a reduction in arc duration and arc length when compared to drier environments.
- All transient features of the arc current and load voltage have increased magnitude in humid environments and are an aide to arc detection, showing a proportional improvement in the discriminating variables used for arc detection with the Windowed Fractal Dimension algorithm.

The combination of increased arc duration, length, and the reduced magnitude of transient arc features recorded for arcs in drier environments indicates that they are higher much risk than arc in humid environments. The lack of transient features may result in missed detection, and the extended arc length and duration have increased potential to damage neighbouring components and start electrical fires. This suggests that particular care should be taken in electric aerospace and solar farming applications where lower relative humidity is common and the impact of DC arc failure could cause excessive damage to property and loss of life.

Future work should investigate how arc behaviour changes with relative humidity at different fixed temperature values, focusing on how the differences in arc impedance at each stage. Preliminary results presented in this paper indicate that increased ambient temperature can also result in increased magnitude current and voltage transients on the arc waveform, amplifying those seen with increasing relative humidity.

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Robust Series Arc Detection for DC MEA Power Systems Using Windowed Fractal Dimension

Danny Seeley, *Member, IEEE,* Mark Sumner, *Senior Member, IEEE,*
David W.P Thomas, *Senior Member, IEEE,* Steve Greedy, *Senior Member, IEEE,*

***Abstract*—The rapid development of more-electric transportation has led to increased use of higher voltage DC circuit architecture and battery storage. These developing technologies create a higher risk of DC arc failure resulting from component or insulation degradation. Arc faults present a risk to system reliably and safety, starting electrical fires that could prove catastrophic in transportation applications. To ensure ongoing passenger safety the development of rapid DC arc fault detection methods is necessary. This article further develops the Windowed Fractal Dimension (WFD) arc detection method for a range of linear and non-linear loads, including networks containing switching power convertors [1]. Results consistently show a substantial change in WFD at arc onset, and whilst the arc is sustained, for all load conditions. The outcome is a new method of fast DC arc detection requiring fewer calculation steps, fewer parameter settings and reduced commissioning when compared to other arc detection methods, and can be used in tandem with existing protection schemes to provide a clear and robust indication of DC arc failure and prevent circuit damage.**

***Index Terms*—arc detection, DC protection, series arc, arc fault, fractal, more electric aircraft**

I. Introduction

THE growth of more electric technologies within the aerospace, automotive and rail industries and the need for larger sources of renewable energy has led to an increase in the use of DC power systems. For example in small to medium sized more-electric aircraft (MEA) applications there is a need for new energy storage systems at 400V DC, which then requires new energy protection strategies [2]–[4]. A specific cause of system failure within DC systems is arc failure, wherein current strays from its designed path and instead discharges through the air. Arc faults are often caused by component failure or breakdown in cable insulation, leaving an air-gap between two exposed conductors [2], [5], [6]. This is of particular concern in the growing electric aircraft and automotive industries, where conductors are subject to vibration and movement, and may be exposed to adverse environmental conditions. The combination of these factors, and the use of new, higher voltage DC distribution systems (which results in higher energy dissipation in the arc), increases the chance of an arc failure with potentiality fatal consequences [3], [4], [7]. Such failures are becoming more costly, with series arcing initiating the failure and the crash of a USAF F22 fighter jet in 2013, at a projected cost of over $100 million [8]. This incident however is not unique, with the US Navy seeing approximately two in-flight fires per month caused by wiring faults; and with the growth of MEA for civilian applications similar results can be expected on commercial aircraft [3], [9], [10].

With the growing use of battery-energy storage systems, hydrogen fuel-cells as well as electric traction, actuation and ventilation systems, DC circuit architecture and its protection is becoming commonplace within MEA [11]–[14].

Series arc failure is a specific fault where in an arc is produced in series with the circuit load, maintaining current flow to the load despite the current now passing through the air. In AC systems, arcs can be detected by the patterns they create in the current waveform as they are extinguished twice per cycle by the zero crossing of the current. This does not occur in DC systems, making the detection much more challenging. The arc can be represented as a nonlinear impedance introduced in series with the load, reducing the circuit current. These arcs are of a particular concern as they are difficult to detect, mimicking a simple step reduction in load, and therefore go ignored by traditional overcurrent protection. Undetected, the arc will continue to burn until it causes further damage or catastrophic system failure [2], [4], [15], [16].

Multiple methods have been developed to address the challenges of DC arc detection including impedance based, reflectrometry and optical techniques. Impedance-based schemes are most common and monitor for a change in system impedance at arc onset. These techniques whilst often non-invasive, struggle to differentiate the arc onset from other changes in system impedance such as irregular switching or load changes, and do not function well in the presence of switching power electronics or non-linear loads, producing false-positives [4], [17]. Reflectrometry (or travelling wave) based techniques are capable of distinguishing both arc faults and fault location through monitoring the return time of a travelling wave incident on a transmission line. Travelling wave techniques begin to fail in larger power networks, where longer transmission lines are regularly separated by power converters, and require the installation of additional expensive and invasive circuitry to install, scaling with the size of the network, increasing both commissioning and upkeep costs [4], [18]. Optical and non-electric detection schemes have similar shortcomings, requiring the installation of additional equipment and regularly producing false positives due to unsealed operating environments or changing ambient

This work was supported by the Engineering and Physical Sciences Research Council (EPSRC)

conditions. There is therefore still a need for research into novel, non-invasive methods of DC arc detection robust to false positives in the presence of switching power electronics, variable loads, or in more complex power networks.

Frequency domain and wavelet decomposition are popular methods for detecting series arc faults within DC networks. Discrete Fourier transforms (DFTs) have been used to identify the frequency components injected by arc failure to indicate a fault and Short-Time Fourier Transforms (STFT) extend this to include both time and frequency domain information to enhance detection capability, yet both suffer from the same shortcoming, in that the specific frequency bands associated with arc failure need identifying in advance. Wavelet methods yield time-frequency information about the arc that can be used for detection, but are heavily reliant on the selection of a mother wavelet. As arc behaviour and waveform shape can change significantly depending on the power network architecture, wavelet methods require specialist knowledge about the system and fault in advance, additional commissioning, and do not generalise well outside of specific test cases. Both frequency domain and wavelet methods can become easily confused in the presence of additional power electronic switching noise, and can lead to missed detection and false positives. [4], [19]–[21]

Impedance-based, frequency domain, wavelet and statistical methods have been used as inputs for AI and machine learning based arc detection solutions. One method presents a decision-tree model monitoring the V-I characteristics of a solar PV array, reporting a 99.8% detection accuracy [22] but requiring 764,529 records of fault data on that specific setup to train. The authors remark the unsuitability of the method due to the cost, potential safety issues with generating such a large data-set, and the feasibility of implementing such a large model. Similarly [23] uses empirical-mode decomposition to create binary classifiers for a support vector machine, yet produced false-positive results in the presence of simple step load change events despite a reported detection accuracy of 96% . From the machine learning methods surveyed [7], [22]–[24], all share the same shortcoming, requiring large training datasets for both normal and fault conditions and are specific to the system they are designed to protect. In many cases this data is impossible to practically acquire, and models trained on other system's data may not generalise well to different power networks. Where the data can be generated, it will result in a massive increase in commissioning time, and may potentially damage the power network when generating test fault data.

The need for non-invasive arc fault protection has led to methods relying on more conventional line current and voltage measurements. In [25] a statistical method is developed based on the Paukert equation, fitted with experimental data from another series of experiments utilising the Uriate arc fault model in [26]. The method utilises 50ms time windows (and up to 50 windows required for total confidence) leading to potential detection times in excess of 2s - adequate time for the arc to cause significant damage. Whilst results showed success across several load conditions (constant resistance, constant power and with a PV array), each of the five threshold conditions required manual changes based on system statistical knowledge for each test setup, pointing towards a longer and more problematic commissioning phase for the method. The authors remark that their method is based on work by Uriate, fit with a 10% error, but fail to acknowledge the operating conditions of those experiments at line currents in excess of 175A; outside the scope of their own experimental work (<25A), where increased heating, convection and electrode deformation will have a greater influence on the arc characteristics. [26] This provides a possible explanation for the number of thresholds and processing steps required for this approach, and suggests that the method may not be suitable for most power networks without specific tuning to the network operating conditions and significant commissioning.

Similar techniques are presented in [21], monitoring the line current for a steep change in gradient before comparing the relative magnitude of frequency domain components introduced by the arc to those recorded in a non-arcing case. Whilst the initial current gradient monitoring cannot discriminate load change events from arcs, the relative magnitude comparison successfully identifies the arc within 16ms. Results are excellent for the given experimental setup, however the method presented carries the same shortcomings of other frequency domain approaches, requiring intimate knowledge of the injected arc frequency bands in advance. The method also risks producing false positives as the power network becomes more complicated and more noise sources are introduced. As with the method described in [25] the relative magnitude comparison method requires the tuning of several detection thresholds and user defined gain values to allow for accurate arc detection. As such there is a nontrivial amount of setup and commissioning required to implement this method onto different test-beds and power networks.

Arc failures have been observed to behave chaotically, causing random changes in circuit current. This non-linear behaviour, coupled with sporadic arc ignition and collapse results in a complex current waveform that displays several chaotic, transient features [2], [4], [6], [7], [15], [21], [25], and fractal behaviours [27]–[30]. Therefore, it may be possible to detect arc faults by monitoring a measure of the chaotic noise superimposed on to the circuit waveforms by using fractal theory. Chaotic changes in arc length should result in measurable changes in fractal dimension that can be used to indicate a sudden arc failure. Fractal methods have found application in the fields of medical electronics and physics as an indicator of sudden change or failure in biological systems [31], [32]. This paper expands upon the Windowed Fractal Dimension (WFD) presented first at IEEE ESAR-ITEC 2023 in [1] developing the method further and testing for robustness across multiple different circuit and load architectures representative of MEA DC battery and post-rectifier bus voltages, different arc ignition types,

step load changes, non-linear loads and within networks containing power electronic converters. The WFD method presented in this work aims to improve upon the shortcomings of existing methods. It requires fewer calculation steps and predefined thresholds than other line voltage and current methods, and has a faster arc detection time when compared to other time-domain methods, with no need for extensive training datasets as for machine-learning methods and no requirement for knowledge of injected arc frequency bands, whilst continually demonstrating a resilience in the presence of a broad range of circuit load types. The outcome is an arc detection method reliant on the intrinsic, chaotic behaviour of the arc itself that can be used alongside other arc detection methods to improve the level of confidence in future arc fault circuit interrupters.

The rest of the paper is structured as follows: Section II describes the experimental methods of producing arc faults, outlining the different arc types and load configurations. Section III documents the WFD method for arc monitoring. Section IV highlights the results of of WFD application to different circuit conditions and architectures. Section V then offers a discussion of the results and future work. Section VI provides a conclusion to the paper and presents the key findings of the research.

II. Experimental Setup for Arc Creation

A. Series Arc Generation and Fault Types

Air-gap ionisation is most easily achieved by introducing an inductive circuit element in series with the fault location. An open circuit then induces a large reverse-voltage which is sufficient to ionise the air-gap of the open circuit and produce a stable arc. All arc faults in this work are generated in this way, using a 0.2Ω, 15.2mH inductor. Two separate methods for generating the series arc fault were used: Forced Separation ignition (also referred to as a drawn arc), and Forced Failure ignition.

1) Forced Separation Ignition: The test circuit is connected through a drawn arc generator consisting of two electrodes which can be moved using a stepper motor as shown in Fig. 1. The circuit is energised with the electrodes in full contact, then separated to introduce and control the arc. Drawn arc faults resemble a conductor or component falling away from its designed position after arc ignition. This results in an air-gap of variable size, and is the most common type of DC series arc [2], [4]. Arcs in this paper use 2mm diameter tungsten electrodes, separating at a speed of 2.5mm/s until arc collapse.

2) Forced Failure Ignition: This involves the deliberate destruction of an under-rated component or small-gauge wire to generate an arc. Here, current is allowed to flow through a rated conductor before being switched to flow through smaller-gauge wire (e.g. wire wool) suspended between two 4mm diameter copper electrodes, separated at a distance of 20mm, as shown in Fig. 2. Resistive heating of the wire causes it to melt, creating an air gap and subsequent series arc. This

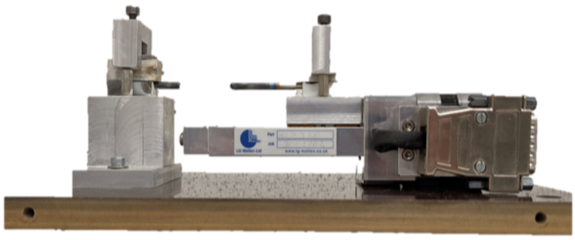

Fig. 1: Forced Separation, 'Drawn', UL1699B Compliant, Arc Generator

simulates the sudden destruction of poorly designed, installed or damaged components. The result is a relatively large arc across a fixed-size airgap, with a sudden and dramatic ignition. The use of forced failure arc ignition is included to emulate a different arc ignition scenario with differing arc behaviour at onset. Robustness against this form of arc ignition is not typically addressed in other series arc detection methodologies in the literature despite its relevance in mimicking failing or underrated components, and therefore provides a unique set of additional arc ignition conditions under which to validate the WFD technique for practical use.

Fig. 2: Forced Failure Arc Generator

B. Load Configurations and Standard Arc Characteristics

Two arc generation rigs were constructed; allowing for either forced failure or forced separation arc ignition types. Rig. A, seen in Fig. 3, employs a 400V DC supply alongside a programmable, non-linear load, R_{Prog} and passive resistive loads, to allow a variety of load configurations and transients to be explored, representative of those found in smaller MEA distribution systems, for both arc ignition types [12], [33], [34].

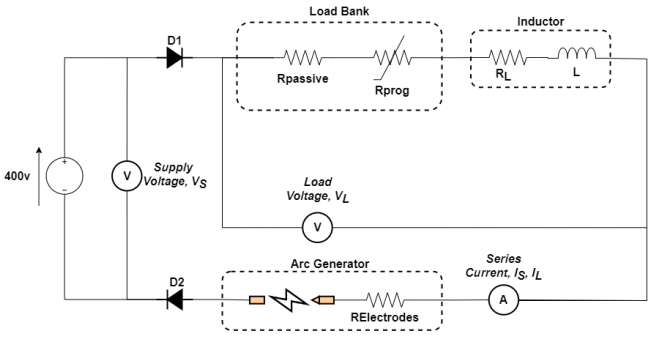

Fig. 3: Arc Generation Circuit Diagram
Rig A: Passive Loads

Rig. B, Fig. 4, uses a 400V-53.5V DC-DC buck converter as part of the load, similar to those at the output of a MEA DC bus, to allow evaluation of the circuit response to an arc between cascaded power converters. This converter transitions to a 'burst mode' on its supply side under light loading

(<300w output power with a 380V input voltage), producing a stable 53.5V output voltage after startup irrespective of burst mode condition. Arcs are produced between the 380V supply and DC-DC step-down converter, to observe the circuit response on both the converter input and output sides.

TABLE I: Table of Load Configurations

	Setup Name	Load Description	Rig Type
1	Passive Resistance	Series combination of resistors totalling 41.7Ω	Rig A
2	Oscillating Resistance	Fixed resistance load with controlled oscillation between 41.7Ω and 57.1Ω	Rig A
3	Oscillating Current	Fixed current load with controlled oscillation between 8A and 6A	Rig A
4	Cascaded Converter	Supply feeds DC-DC converter powering a 13.38Ω passive load	Rig B
5	Converter Burst-Mode	Supply feeds DC-DC converter in burst mode, powering 3A controlled load	Rig B

To test the robustness of the WFD algorithm for arc detection, a range of load responses and arc failures were recorded. Each of the load configurations summarised in Table I were recorded under arcing and non-arcing conditions, and produce output traces consistent with those found in other literature [2], [4], [15], [35]. Shown in Fig. 5 and Fig. 6 respectively are typical results of a series arc fault produced using Setup 1 for both unique ignition types. These traces have been labelled to better illustrate the key phases of a DC series arc fault. With reference to the annotations in Fig. 5, these are:

- Pre-Arc: The time before arc ignition, circuit is operating under normal conditions, in steady state.
- Arc Ignition: The moment the arc ignites to maintain current flow, causing the initial transient response.
- Steady State Arcing: The period between arc ignition and arc collapse where the arc is sustaining the current flow.
- Arc Collapse: The point where the arc can no longer support the current flow, resulting in an open circuit.
- Post-Arc: The period following arc collapse, where the circuit is broken by an non-ionised airgap.

Each 'phase' of arcing displays different characteristics, each of which could potentially be used as indicators of an ongoing arc failure. This work focuses on the 'arc ignition' phase, for arc detection. This allows for the shortest possible time before arc onset and detection. All data was recorded using a Picoscope 5000 Series oscilloscope at a sampling frequency, F_s, of 2.0492MHz with 15bit ADC resolution.

Initial inspection of these traces shows a contrast in arc behaviour, governed mostly by the differences in arc impedance between the different ignition types. The forced separation arc shown in Fig. 5 does not produce a large change across all variables upon arc ignition at t = 1.2s compared to the forced failure arc seen at t = 5.3 in Fig. 6. This is most likely due to the different arc lengths at ignition, and by extension the different arc impedances introduced to the circuit. The forced ignition arc begins as soon as the electrodes are separated with a very small air-gap (μm scale) and initial arc impedance. The shorter air-gap requires a smaller voltage to ionise (approx. 3kv/mm [5]), a value less than the circuit supply voltage, resulting in only a marginal disturbance to the recorded waveforms as the arc forms.

The forced failure ignition arc in Fig.6 has a larger air-gap of 20mm at the point of arc ignition, and therefore a greater arc impedance. The ionising voltage required to create an arc discharge is much larger due to the additional separation of the electrodes [2], [5]. This produces a bigger disturbance in the recorded waveforms as the arc ignites. The arc length here remains fairly constant at around 20mm as the electrodes are immobile. There are minor changes in length as the arc rises due to convection flow in the air. This results in a very stable output trace, with no additional features until the arc is de-energised through removal of the supply at t = 9.3s.

In the forced separation arc in Fig. 5 the arc length is constantly increasing, with the electrodes separating at a fixed speed. This is mirrored in the output traces as a reduction in load voltage and current as the arc impedance increases. When the arc reaches a sufficient size at 11s (approx. 22.5mm separation) the arc can no longer be sustained, resulting in the intermittent arc collapse and ignition seen from t = 11s to t = 12s. The arc collapse seen here results from a combination of factors, namely:

- Field collapse: The point voltage at the electrodes is no longer sufficient to sustain an electric field strong enough to maintain the arc.
- Thermal collapse: The arc cools down due to its increased surface area and the arc plasma itself can no longer be sustained.
- Arc deviation: As the arc moves, part of the arc length travels away from the electric field between the electrodes and is no longer supported by it.

III. Windowed Fractal Dimension (WFD)

Fig. 7 shows a flowchart outlining the process for calculating the WFD of a waveform, and has been split into two key stages; Calculation and Detection. The calculation of the signal WFD, begins with initial signal processing. The sampled input signal can be considered as a discrete time vector, S(n), with N total samples. S(n) is then passed through a digital low-pass filter, with a 25kHz cutoff frequency, 60dB stopband attenuation, and impulse response h(n). Filtering at this frequency retains the significant frequency components of the arc (described as below 3500 Hz in the literature [4], [7], [16], [36]) whilst significantly attenuating the random noise present in the signal and eliminating other high frequency components that may interfere with the superimposed arc noise, such as power electronic converter switching (modern DC-DC converters operating at 20 - 200kHz [37]), high frequency switching harmonics, power line carrier waves (signals used for power line communication at or above 58 kHz [38]) or resonant effects within the power network. Time domain

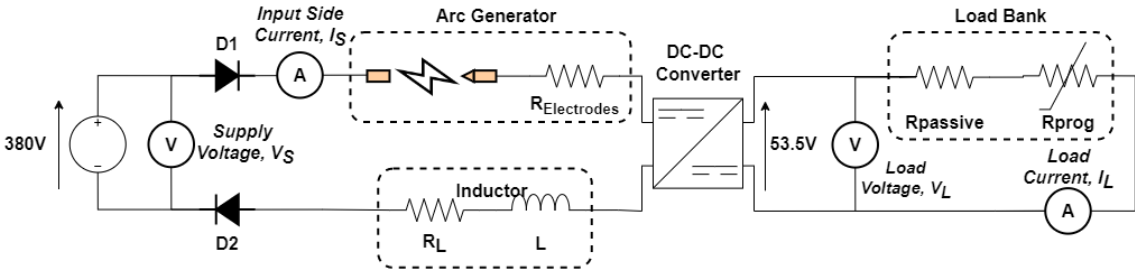

Fig. 4: Arc Generation Circuit Diagram
Rig B: Cascaded DC-DC Converter

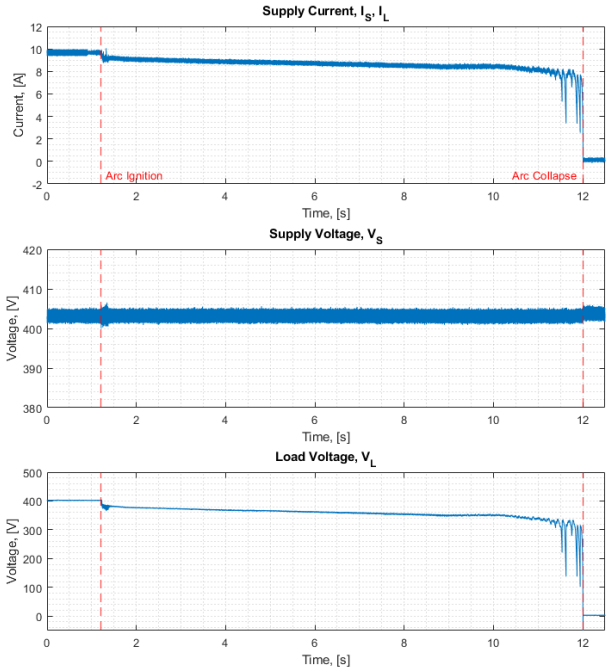

Fig. 5: Typical DC Series Arc Waveforms - Forced Separation Ignition, Setup 1, from t = 0s to t = 12.5s

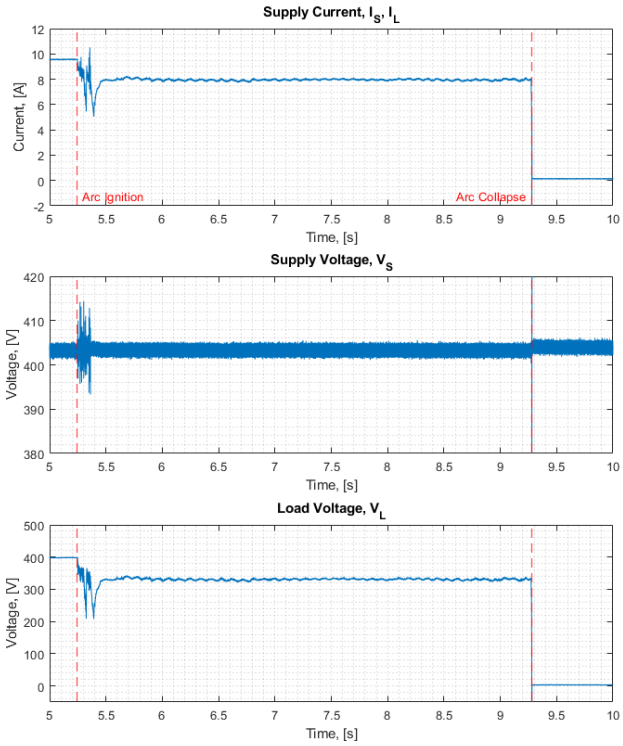

Fig. 6: Typical DC Series Arc Waveforms - Forced Failure Ignition, Setup 1, from t = 5s to t = 10s

convolution of the input signal S(n) with the filter impulse response, h(n), yields a filtered form of the input signal, $S_{filt}(n)$:

$$S_{filt}(n) = S[n] * h[n] = \sum_{m=-\infty}^{\infty} h[m]S[n-m] \quad (1)$$

$S_{filt}(n)$, is then partitioned into short-time segments of approx. 0.5ms (1024 samples at Fs = 2MHz) through multiplication with a simple rectangular windowing function, W(n). The rectangular windowing function was selected instead of a shaped window as fractal methods rely heavily on the shape of the waveform, and any distortion in waveform geometry will adversely affect the WFD output [27], [29], [39]. This operation results in a windowed form of the original signal, $S_{wind}(n)$, with N_{win} samples, where $N_{win} < N$:

$$W(n) = [w(1), w(2), \ldots, \ w(N_{win}) \ ] = 1 \quad for \quad 1 < n < N_{win} \quad (2)$$

$$\therefore \ S_{wind}(n) = S_{filt}(n)W(n) = [s_{filt}(1), s_{filt}(2), \ldots, \ s_{filt}(N_{win})] \quad (3)$$

To compute the fractal dimension using the Sevcik method, the weighting of any units must be removed by normalising the data to a unit square [39]. The normalisation process is repeated for both the signal datum and the corresponding time vector. Mapping the information in this way provides a better representation of how the waveform geometry changes, without undue 'skew' due to unit weight.

$$S_{Norm}(n) = \frac{S_{wind} - min(S_{wind})}{max(S_{wind}) - min(S_{wind})} \quad (4)$$

The windowing and normalisation process as described in (1-4) above is then repeated for the time vector t(n):

$$t(n) = [t(1), t(2), \ldots, \ t(N) \ ] \rightarrow t_{Norm}(n) \quad for \quad 1 < n < N_{win} \quad (5)$$

With the signal pre-processing complete, it is possible to calculate the fractal dimension of the normalised signal window using the method described by Carlos Sevcik [39]. This process is completed by first calculating the euclidean

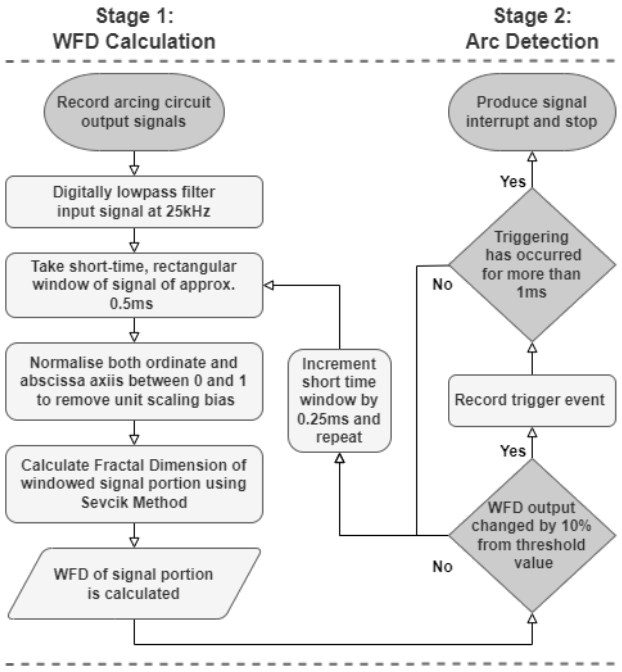

Fig. 7: Flowchart documenting process of the WFD algorithm with calculation and detection stages

length of the input signal, L, and taking it's natural logarithm, then dividing this by the natural logarithm of the number of sample steps, $N' = N_{win} - 1$, within the signal length:

$$L = \sum_{(n=1)}^{(N_{win}-1)} \sqrt{\begin{array}{l}((t_{Norm}(n+1) - t_{Norm}(n))^2 \ \ldots \\ + (S_{Norm}(n+1) - S_{Norm}(n))^2\end{array}} \quad (6)$$

$$FD = 1 + \frac{\ln(L)}{\ln(2 \cdot N')} \quad (7)$$

The output fractal dimension (FD) represents a measure of self-similarity and chaos within the signal window. A resting value of FD will exist for the measured system whist in steady state operation, and given the presence of switching electronics introducing some non-linearity, this will likely exceed the expected topological dimension of 1. For example, using the setups described in this publication the resting value of FD is 1.41, and can be seen in figures throughout. With the onset of an arc, chaotic, fractal noise should dominate the signal and an observable change in FD will be seen to differentiate its from normal, resting value. With the first 0.5ms window calculated, the sampling window then shifts by 0.25ms (or half N_{win} samples) and the process is repeated. For the calculation stage, this ends when the full signal length of N samples has been transformed to produce the signal WFD, but can also be run continuously for online system monitoring. Signal windows have deliberately shifted by a maximum of half N_{win} samples as this ensures at least a 50% overlap of datum within each window, ensuring no loss of information whilst also reducing runtime.

Detection of the arc, follows a simple threshold based detection scheme. The threshold is set by taking the RMS value of the WFD over the first 8 signal windows, as an indicator of the resting fractal dimension for the system before an arc fault. To be classified as sufficient to indicate an arc, the WFD transform must show a change in FD value greater than $\pm$ 10% from the pre-ignition RMS FD value, and an output trigger is then recorded. The $\pm 10\%$ detection threshold was determined as the optimal detection threshold value by performing a Receiver Operating Characteristic (ROC) analysis, a statistical technique for the tuning of detection thresholds [40], [41]. The analysis compared several different detection threshold values (from $\pm 2.5\%$ to $\pm 17.5\%$) on 20 total passive arcing and non-arcing data captures using the circuit shown in Fig. 3, for both described arc ignition types, to determine the suitability of each possible threshold. The $\pm 10\%$ detection threshold determined from the ROC is significant enough to distinguish the arcing behaviour from normal operation, and to set a standard for the threshold based detection that follows. Should the trigger have been firing continuously for 1ms (or $2 \times Nwin$ samples) or more, a signal interrupt is produced and the WFD calculation loop terminates, giving a trigger time of just over 1ms from arc ignition. A high valued digital logic signal is then output that can be used to trigger existing circuit protection to prevent any further damage. The 1ms detection time was chosen as it is large enough to ignore any short-time (µs) transient spikes in fractal dimension seen in the presence of specific switching behaviours, whilst still detecting the arc and producing an interrupt before the arc can change length and travel away from the point of arc ignition. The 1ms detection time was determined to be appropriate for the specific test setup in this paper, similar to the feed from a DC battery or fuel cell output. Further work is required to determine its suitability for other power networks, however this is easily modified and detection time is unlikely to increase as the base algorithm does not vary.

IV. WFD Application and Results

The performance of the proposed WFD method was evaluated through the following tests:

A. Passive and Controlled Oscillation Load - Rig. A

1) Passive Load - Setup 1: The supply is connected to a simple 41.7Ω resistive load, and an arc is created and allowed to extinguish. The WFD algorithm is applied to the output current and load voltage to assess the effectiveness of the WFD in producing a measurable change in fractal dimension (FD) during arcing across both measurements. An example of both input traces and WFD outputs for a forced failure arc under these conditions are shown in Fig. 8:

It can be observed that both the current and load voltage traces in Fig. 8 produce a measurable response to the arc fault at t = 5.15s. The current WFD shows a 13.5% change in fractal dimension from a resting value of 1.41 to a value of 1.22 at arc ignition. A similar change of 16.4% from 1.4 to 1.17 is seen in the load voltage WFD, demonstrating that the WFD can produce significant enough change for detection at arc ignition for both waveforms. The load voltage WFD produces a greater change at both arc ignition, collapse and throughout the 'steady state arcing' phase versus the

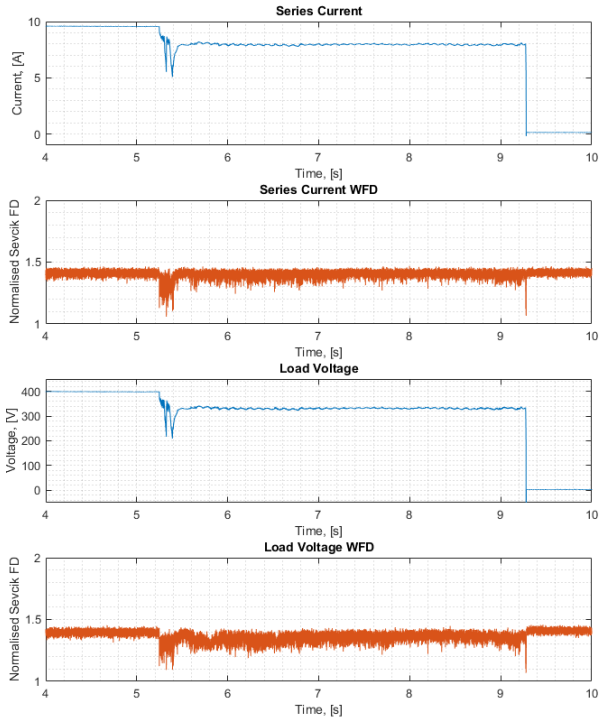

Fig. 8: DC Series Arc Passive Load Waveforms and WFDs for Forced Failure Ignition, Setup 1, from t = 4s to t = 10s

current WFD, providing options for detection outside of arc ignition and a clearer indication of continued arcing behaviour. The described tests were repeated for a total of 10 forced separation and 5 forced failure arcs, with the key metrics given in Table. II. Results consistently show a greater change in load voltage WFD when compared to series current WFD, with an average of 8.22% improvement seen in forced separation arcs, and 2% in forced failure arcs. In the case of forced failure arcs, both the series current and load voltage WFDs produce a significant ($>= \pm 10\%$) change in FD across all tests. This is not the case in the forced separation arcs, where a significant change is seen in 100% of load voltage WFDs, but in only 20% of the series current WFD's.

Results from this initial testing indicate that the WFD algorithm is capable of producing a significant and detectable change during an arc event for both arc ignition types, sufficient for arc detection, with improved results when monitoring the WFD of the load voltage waveform.

2) Controlled (Oscillating) Loads - Setups 2 & 3: For the following tests, data was captured from Rig. A with the programmable load set to impose regular step changes on the load at a user defined frequency. The aim of these tests was to show that the WFD algorithm was was able to distinguish between load changes (or loads with a significant frequency content) and arc faults. These types of load frequently trigger false-positives in other arc detection methods [19], [20], [22], [23]. Shown in Fig. 9 is a load voltage trace of a forced failure arc, using load Setup 3 alongside it's WFD transformation. The fixed current load (not seen) step changes between 8A and 6A at a rate of 2.5 kHz. Here, the FD remains constant during the pre-arc period (4s - 5.4s in Fig. 9) even though the load itself is oscillating, It then changes by 22.8% from it's resting value of 1.4 pre-arc to a minimum value of 1.08 at arc ignition, and maintains a consistent value of FD throughout the arcing period. The clear change in FD is seen across both 'arc ignition' and 'steady state arc' phases and is sufficient to be used for arc detection.

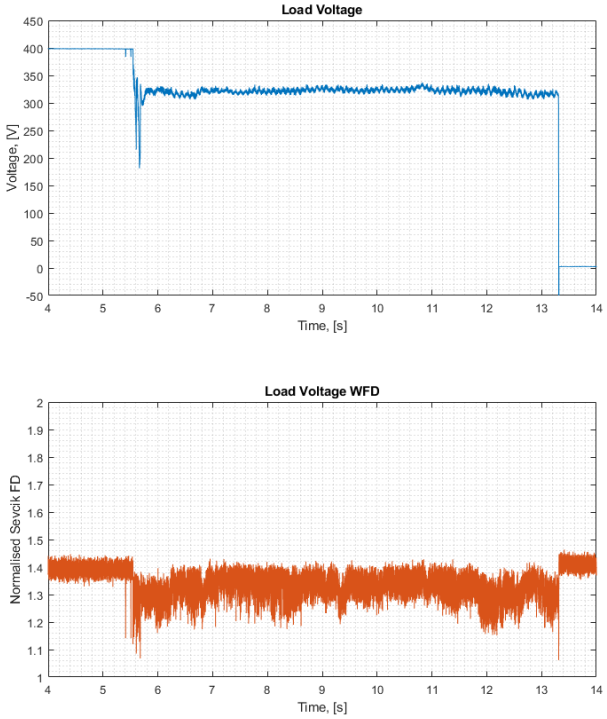

Fig. 9: DC Series Arc Load Voltage Waveform and WFD for Forced Failure Ignition, Setup 3, from t = 4s to t = 14s

A total of 71 repeats were conducted across Setups 1, 2 & 3, spanning a range of frequencies from 100-5000Hz and covering both arc ignition types. During each test, the WFD was assessed on four criteria to determine its effectiveness; Does the WFD show: a) A change of FD $> \pm 10\%$ when arcing, b) A consistent change of $> \pm 5\%$ at arc ignition, c) in steady state, and, d) at arc collapse. These were selected to identify a large enough change in FD to detect an arc, and to indicate a continuous change in FD whilst the arc is sustained. The success rate of the algorithm is defined by how many of the four possible criteria are satisfied for each individual repeat. The additional success criteria b, c and d were included to identify how the performance of the WFD algorithm changes with the varied load conditions during the different arc phases outlined in Section II.B

Across all tests a success rate of 100% was observed when monitoring the load voltage WFD waveform for these defined changes. The resultant success rate provides a strong indication that the WFD algorithm produces a measurable sign of arc ignition under all tested load conditions. Table. II highlights key metrics from these repeats to better illustrate the effectiveness of the WFD algorithm across a broad range of load configurations. It can be observed from the results

in Table. II that the WFD algorithm produces an average change in fractal dimension of 19.85% for all the tested setups and arc ignition types, successfully identifying all arc failures. These average results surpass the required $\pm$ 10% threshold for arc detection, even in the presence of a relatively large pk-pk noise, demonstrating the capability of the algorithm to indicate the onset of series arc failure across a variety of load conditions. Noteworthy, is that the average percentage change in WFD is greater in all forced failure arc ignition types versus drawn arcs. This is most likely due to forced failure arcs being more 'violent' at ignition on account of the increased initial arc length and impedance versus a drawn arc. The greater arc impedance results in a larger arc flash and bigger transient on the load voltage waveform, producing a greater change in WFD as the arc becomes established. The clear difference between the two suggests that the performance of the WFD algorithm would only improve with larger and more dramatic; and therefore damaging, arc failure events.

B. Cascaded DC-DC Converter WFD Results - Rig. B: Setups 4 & 5

Fig. 10 shows the converter input voltage and load traces captured during a forced separation, series arc failure event between the supply and step-down converter of Rig. B, Fig. 4, and its WFD transformation as described in Setup 4 in Table. I. Both voltage traces show a clear indication of the arc fault, resulting in a change of 27.5% at the input side, and 16.07% on the load at arc ignition at t = 1.55s. Important to note for Fig. 10 is that the recorded load voltage is physically separated from the arc event by a commercial 400-53.5V DC-DC step-down converter. It can be observed that the WFD algorithm can still producing a change to identify the arc fault from the signal that has propagated through the DC-DC converter, despite the physical separation from the arc.

In Fig. 11 a simple threshold based trigger as described in Section. III was applied to series current data captured from Rig.B, Setup 5; showing the input current, its WFD and the output triggers produced. During this test, the step-down converter was forced to operate in burst-mode by using a low circuit load (<300W). This causes periodic switching and spiking on the input-side waveforms, resulting in very noisy output signals, even before arc ignition at t = 1.61s. This mode of operation can be very challenging for arc detection as it can trigger 'false positives' i.e. the detection of an arc when no arc is present in the system. Fig. 11 highlights how the combination of a simple trigger and the WFD algorithm can be used to discriminate between the noise produced by arcing, and that from the circuit burst-mode operation. The supply side current data was selected here as it is the most directly affected by the burst mode operation of the converter, and better demonstrates how the WFD algorithm and threshold-based trigger can discriminate an arc event from burst mode noise. It can be seen from Fig. 11 that trigger events occur both at the point of arc ignition and throughout the 'steady state arcing' phase, ensuring a stable output for detection. The triggering portion of the algorithm detects

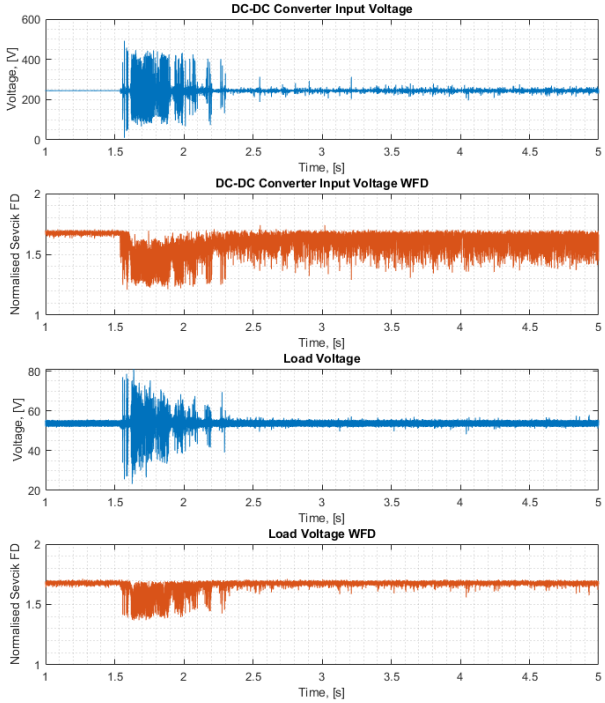

Fig. 10: Cascaded Converter Voltage Waveform and WFD for Forced Separation Ignition in Normal Operating Mode, Experimental Setup 4, from t = 1s to t = 5s

the arc from the WFD output and consistently produces a response within 1.5ms of arc ignition, which can then trip appropriate protection.

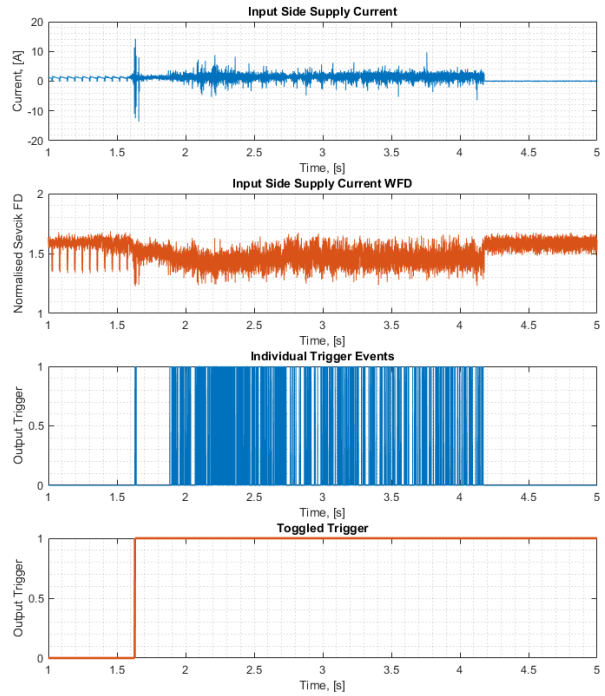

Fig. 11: Cascaded Converter Supply Current Waveform and WFD for Forced Separation Ignition in Burst Mode with Trigger, Experimental Setup 5, from t = 1s to t = 5s

In both Setup 4 and Setup 5, and as can be seen in Fig.10,

TABLE II: Table of WFD Output Results across Rig.A Load Configurations

Setup Number	Arc Ignition Type	Typical Mean Load Voltage WFD Value Pre Ignition	Typical Pk-Pk Noise Value Pre-Ignition	Typical Load Voltage WFD Value Post-Ignition	Average Percentage Change in WFD, [%] At Igniton	Number of Repeats	Success Rate, [%]
1	Forced Failure	1.404	0.056	1.098	21.70	5	100
1	Forced Separation	1.403	0.054	1.136	18.97	18	100
2	Forced Failure	1.398	0.049	1.12	19.86	12	100
2	Forced Separation	1.384	0.049	1.12	19.05	12	100
3	Forced Failure	1.393	0.052	1.098	21.17	12	100
3	Forced Separation	1.378	0.061	1.125	18.37	12	100

the measurements taken physically closer to the arc; such as input voltage and supply side current, produced a larger change in the WFD versus the load current and voltage measurements that were separated from the arc by the power converter. The reduced change in WFD seen during arcing on load-side measurements failed to produce a trigger after propagating through the converter, however the arc was still successfully identified from the supply-side current and voltage measurements in each case. This indicates that the algorithm is better suited to protection when used throughout a power network, as the magnitude of WFD change at arc ignition is seen to vary with distance from the arc and might not be sufficient to trigger detection with increasing distance from the fault (or the addition of more power converters). In utilising the WFD method throughout a power network the risk of missed detections is mitigated, and it may be possible to locate the arc by examining the change in magnitude of the WFD output to give an indication of distance to the fault, however further work is needed to examine this in detail.

V. Discussion

A. Results

The challenges for any detection algorithm are associated with repeatability (i.e. false detection), and identifying levels associated with healthy and abnormal behaviour (i.e. commissioning). The results presented in this work have demonstrated the WFD Fault Detection scheme can produce reliable and repeatable information on the presence of an arc fault in a circuit, for a variety of load conditions, when it is correctly commissioned. A success rate of 100% is seen for voltage WFDs across all experiments undertaken, detecting the arc from the threshold value, whilst also producing a detectable continuous change whilst the arc remains burning. When comparing against other techniques in the literature, the WFD technique shows an improved detection time, with capability to detect the arc within 1.5 ms of arc ignition, versus 16 ms in [21] and in excess of 50 ms in [25], and has been demonstrated on empirically captured arc failure data, rather than purely simulated data presented by other methods in the literature [22], [25], [42]. The WFD technique also demonstrates a reduced commissioning burden versus other techniques in the literature, not requiring large training datasets as with modern machine learning based techniques [4], [7], [22], [23], and requiring only two commissioned values, fewer than the five plus commissioned values in other conventional line value and frequency domain techniques in the literature [19]–[21], [25].

It can be seen in results presented throughout this work that the WFD output value reduces in magnitude at the point arc ignition. Whilst it may seem counter-intuitive that the introduction of the arc and its fractal behaviour causes the overall fractal dimension to reduce, rather than increase, this is not a-typical behaviour and a reduction in fractal dimension with the presence of a fault or change in behaviour has been utilised elsewhere in medical and mechanical engineering fields for diagnosis of healthy and unhealthy systems [43]–[45]. The exact interactions that produce the resulting fractal dimension of two combined continuous fractal functions is highly complex and is a subject of ongoing research and debate amongst mathematicians [46]–[49]. Recent work in [46] remarks that for the sum of two continuous functions, the function with the greater inherent fractal properties that define the limits of the calculation of fractal dimension will dominate the resultant fractal dimension of their sum. This suggests an explanation for the resulting reduction in fractal dimension at arc onset, in that if arc exhibits inherently more fractal behaviour than the base circuit waveform (The working assumption for the WFD technique) then it will dominate the resulting output fractal dimension and will represent the fractal dimension of the arc itself, rather than the base waveform, be that higher or lower in value.

B. Calculation Time

Results have shown how the WFD method, relying exclusively on the fractal properties introduced by the arc itself, can improve upon the shortcomings of existing arc detection methods and demonstrates a measurable change in fractal dimension across in 100% of tested cases and for all load conditions. The WFD algorithm demonstrates a clear improvement in detection time compared to other time domain methods and requires only one initial detection threshold value calcluated at the start, versus the 4-5 commonly required, and therefore an associated reduction in commissioning time. For the work in this paper, all WFD implementations were performed offline on MATLAB using prerecorded data with experimental results yielding a theoretical minimum detection time of 1.5ms from arc onset, outperforming other reported time domain arc detection algorithms by several milliseconds, and in some cases an order of magnitude, leaving less time for the arc to propagate and cause further damage before it is detected. The MatLab algorithm was profiled using MatLab's SoC Blockset algorithm analyser and found the compiled

code to require 492,000 floating point operations for each signal window, i.e 1.968 million operations are required each millisecond (noting that none of the programming in this project has been optimised for real time performance). Modern mid-range FPGA's are capable of calculating over 1000 million floating point operations per second: E.g. the Intel 7-Series FPGA has floating point performance of 2000GFLOPs; and would be capable of directly implementing the WFD algorithm as an online method. With optimisation for real-time, online operation the WFD approach will have little issue running on modern, current FPGA architecture, with a presumed minimum impact on arc detection time. [50]

C. Commissioning Considerations

For these experiments, the baseline (healthy) value for the WFD measurement, made at a particular point in the circuit was obtained at startup. The RMS value of WFD is calculated over 4ms under the assumption that no fault is present on the the circuit initially. In this work, a WFD magnitude variation of $> \pm 10\%$ has been used to create the threshold for arc detection, based on experience gained whilst setting up the experiment and through ROC analysis of several different detection thresholds tested against both arcing and non-arcing conditions. The $> \pm 10\%$ threshold produced the best results from the ROC analysis, and can successfully discriminate the arc in all test cases. The detection threshold value may vary between implementations and further work performing a more extensive ROC analysis with additional different input test cases specific to the systems to be protected (such as circuits with switching power electronics or cascaded power converters) are required to identify what the optimal detection threshold might be. In characterising the detection threshold against more circuit conditions in advance of commissioning, the commissioning can be eased as the detection threshold should not require manual tuning at implementation, having undergone thorough statistical analysis in advance. As such, further characterisation of the WFD technique and detection thresholds should be considered for future work. There may also be the requirement for commissioning of the window size, N_{win} of the WFD. The time window of signal analysed by the WFD method depends on both N_{win} and the sample rate of input signals to the WFD, with a reduction in either reducing the amount of signal windowed and therefore limiting the accuracy of the technique, but possibly increasing the speed of calculation for each signal window. Furthermore, any change of window size will then vary the detection speed of the algorithm, as this too is dependant on the size of N_{win}. As such, commissioning of N_{win} presents a trade off between the calculation speed, detection speed and accuracy of the technique that the commissioning engineer must consider, but this does offer the flexibility for allowing faster detection in life-critical applications such as MEA, versus slower and potentially more accurate detection in cost-critical applications such as solar power distribution. Ideally, input to the WFD should utilise a sampling frequency as high as possible, allowing for a smaller window size without loss of accuracy, regardless of application.

D. Arc Location

A subject of further work is to explore how the WFD algorithm could be applied locating an arc within a distribution network. The focus of the work presented in this paper was to demonstrate the viability of a new method of arc detection, however experiments have indicated that arc location may be a possible extension. The results of experiments performed and illustrated in Fig. 10 have shown how the fractal arc characteristics can propagate through a power converter. The WFD measured closer to the arc (converter input) was stronger than that measured at the converter output, and by comparing relative magnitudes of the changes in WFD measured at different points in a power network, it may be possible to determine specifically where the fault has occurred within said network.

E. Challenges

Load voltage has predominantly been used here for arc detection as it has consistently produced stronger measurements versus the load current. Current measurement does still produce useful results in some cases and would be more convenient and potentially non-invasive. However, circuit transients and oscillations are more prominent in the load current waveform. This can be addressed with application specific filtering, or the use of techniques such as a "leaky integration" to create trip signals versus the existing fixed threshold. Further work is required here.

VI. Conclusion

Fractal theory was proposed to detect DC series arc failures across a range of load conditions and arc ignition types. The WFD algorithm can produce a measurable change in fractal dimension whilst an arc is sustained, and has been verified for both passive and non-linear loads, and in the presence of commercial power electronic converters, at voltages representative of small-medium future MEA. Results demonstrate that series arc failures can be detected within 1.5ms of arc ignition and that detection is robust against changing and complex load conditions, with the potential for online implementation on modern, mid-range FPGAs with limited impact on arc detection time. Additionally, the WFD algorithm can discern arc faults from measurements made after the arc has propagated through a commercial DC-DC converter. This gives evidence to support the use of the WFD algorithm as an arc location tool. Further work will focus on improving the signal-to-interference ratio of the algorithm through the introduction of improved peripheral filtering of input waveforms, and using the WFD algorithm for arc location. Additionally, there is still the scope to test the efficacy of the WFD technique on specific more-electric transport power networks, including those sourced from HV batteries, with drive-controlled DC motors, or significant radiated electromagnetic interference. Monitoring of the steady state arc phase and the application of an additional detection scheme, such as a leaky integration may improve the indication of arc ignition to further increase the robustness of this approach.

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Appendix B: WFD Functions and Code

The following appendix serves to record the primary functions used throughout this thesis to generate the Windowed Fractal Dimension from a set of discrete sampled data. All functions are written, decared and compiled in MATLAB. Shown in Figure. 8.1 is the main function used to calculate the WFD from a pair of corresponding input signal and time vectors. Nested within this are three additional functions, each used to perform a smaller element of the WFD calculation: The function in Figure. 8.2 performs adjustment of the overall signal length to accommodate for the additional size of the user-defined windowing function. In Figure. 8.3 the function shown performs the unit-square normalisation required for accurate calculation of fractal dimension. Finally, in Figure. 8.4 the fractal dimension of the input signal is calculated using the Sevcik method. Collectively, these functions form the basis for calculating the Windowed Fractal Dimension of a signal, allowing for the application of a dectition scheme of choice by the user.

```
function WFDOutput = DS_WFDCalc_Sevcik(ordinateSignal, abscissaSignal, Nwin, inc)

N = length(abscissaSignal); % Define number of input signal samples
WFDOutput = zeros(N,1); % Create Output vector

% Input signal length is adjusted to accomodate the additional sample size of the moving signal window

abscissa_LengthAdjust = DS_lengthNorm(abscissaSignal, Nwin); % Input Time Signal Length Adjusted

ordinate_LengthAdjust = DS_lengthNorm(ordinateSignal, Nwin); % Signal Length Adjusted

for m = 1:inc:N % Moving window at inc steps

    abscissaWin = abscissa_LengthAdjust((m:m+Nwin),:); % window the abscissa
    norm_abscissaWin = DS_unitNorm(abscissaWin); % normalise the window

    ordinateWin = ordinate_LengthAdjust((m:m+Nwin),:); % window the ordinate
    norm_ordinateWin = DS_unitNorm(ordinateWin); % normalise the window

    WFDOutput(m) = DS_sevcikFD_Calc(norm_ordinateWin,norm_abscissaWin); % find FD of windows

end

WFDOutput(1:inc) = WFDOutput(1); % Save the current window WFD

% Remaining code removes influence of initial length adjustment in the output signal required for moving window

for n = 2:(length(WFDOutput)/inc)

    WFDOutput((n-1)*inc:(n*inc)) = WFDOutput(((n-1)*inc)+1);

end

WFDOutput(end-inc:end) = WFDOutput(end-inc-1);

  end
```

Figure 8.1: MatLab Function to Calculate Windowed Fractal Dimension

```
function lengthAdjSig = DS_lengthNorm(inputSig, Nwin)

% Funciton adjusts input signal length is adjusted to accomodate the
% for the additional sample size of the moving signal window in the main
% WFD calculation function.

N = length(inputSig);

if ~mod(Nwin,2) % Is the window size even?

    % First half Nwin points
    BeginningExtension = inputSig((1:Nwin/2),:);


    % Last half Nwin points
    EndExtension = inputSig(( (N-((Nwin-2)/2)):N),: );


    % Adjust lengths appropriately
    lengthAdjSig = vertcat(BeginningExtension, inputSig, EndExtension);


else % Window size is odd

    % First half Nwin points
    BeginningExtension = inputSig((1:((Nwin-1)/2)),:);


    % Last half Nwin points
    EndExtension = inputSig((N-((Nwin-1)/2 )):N, :);


    % Adjust lengths appropriately
    lengthAdjSig = vertcat(BeginningExtension, inputSig, EndExtension);

end

end
```

Figure 8.2: MatLab Function to Perform Vector Length Adjustment as Input to the Windowed Fractal Dimension Function

```
function unitNorm_inputSignal = DS_unitNorm(inputSignal)

% Function normalises the input signal between values of 1 and 0 to remove
% unit weighting in later WFD calculation

inputMax = max(inputSignal); % Find max and minimum of input signal
inputMin = min(inputSignal);

sigLength = length(inputSignal); % Define signal length and create output vector
unitNorm_inputSignal = zeros(size(inputSignal));

for n = 1:sigLength % Normalise each value across whole input signal

    unitNorm_inputSignal(n) = (inputSignal(n) - inputMin) / (inputMax - inputMin);

end

end
```

Figure 8.3: MatLab Function to Perform Unit-Square Normalisation as Input to the Windowed Fractal Dimension Function

```
function sevcikFD = DS_sevcikFD_Calc(sigWin, timeWin)

% Calculated fractal dimension using the Sevcik method.

% Inputs are windowed, normalised signal and windowed, normalised time
% vectors


Nwin = length(sigWin);
sevcikLength = 0; % Create output vector

for n = 1:(Nwin-1) % Calculate Euclidean length of input signal window

    sevcikLength = sevcikLength + sqrt( ((timeWin(n+1) - timeWin(n))^2) + ((sigWin(n+1) - sigWin(n))^2)  );

end

% Calculate Sevcik FD
sevcikFD = 1 + ( log(sevcikLength) / (log(2*(Nwin-1))) );

end
```

Figure 8.4: MatLab Function to Perform Calculation of Sevcik Fractal Dimension as Input to the Windowed Fractal Dimension Function