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High-Frequency Power Conversion for Photovoltaic Module Applications

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I know that I know nothing.

Abstract

As world governments focus on transitioning to renewable energy production, power electronics are a mandatory tool in facilitating this transition. Power electronic converters are needed in all types of renewable energy production, whether that is wind, solar, geothermal, or wave energy.

This work focuses on solar energy generation in the residential market segment. In this segment, it is valuable to have individual control of each solar panel module, as environmental conditions can vary significantly at each neighbouring panel. This typically leads to the need to regulate the photovoltaic panel voltage across a wide voltage range, preferably with a favourable power conversion efficiency, to increase the annual energy yield from the installed panels.

Various actions were undertaken within this work to improve on the existing state of the art. First, a literature review of existing converters in this application area is presented. The benefits of wide-bandgap devices are also explored. Some of the Gallium Nitride devices typically used in this application area have been characterised for their performance, as this transistor technology has shown promising results in recent years and has led to the creation of breakthrough conversion systems in terms of size and efficiency.

In addition, a topology-morphing converter is proposed, achieving broad input voltage regulation with high efficiencies and constant operating frequency. The operation analysis and experimental verification are presented in the chapters of this thesis. Several design pitfalls are also presented, along with avenues to increase the performance of the designed solutions. The designed converter achieved a peak efficiency of 98.5% while also keeping the efficiency over 90% with a wide range of input voltages (8-35 V).

Finally, the proposed converter is redesigned to work in the MHz frequency range. The redesigned converter benefits from the use of planar magnetics, resulting in a slim converter profile. A low-profile conversion system can enable integration of the power conversion system with the photovoltaic panel, providing several benefits, such as easy and scalable installation. Most importantly, it allows an integrated solution for photovoltaic building materials, which have stringent dimension requirements. The size reduction is highlighted in the thesis, and experimental results are presented for this case. A peak efficiency of over 95% is seen in the redesigned conversion system, which also has a minimal height profile of 9.1 mm.

Acknowledgements

My journey through this PhD work has been one filled with learning experiences, excitement and disappointment, frustrations, and moments of enlightenment. I would like to thank my supervisory team, Prof. Mark Johnson, Prof. Lee Empringham, and Dr. Liliana de Lillo, for giving me this opportunity to take on this work and for their guidance throughout the past few years.

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List of Publications

1. Sergentanis G, de Lillo L, Empringham L, Johnson C.M. "**A Topology-Morphing Series Resonant Converter for Photovoltaic Module Applications**". In: the 24th European Conference on Power Electronics and Applications (EPE 2022 ECCE Europe) Hannover, Germany, September 2022. [Chapter 3]

2. Sergentanis, G., Řomulo de Novaes, Y., de Lillo, L., Empringham, E. and Johnson, C.M. "**Dynamic Characterization of of 650V GaN HEMT Transistors**". In 17th Brazilian Power Electronics Conference and 8th Southern Power Electronics Conference, Florianopolis. Brazil, November 2023. [Chapter 4]

Contents

List of Tables

List of Figures

Chapter 1

Introduction

The world's governments are aiming to increase the contribution of renewable energy sources (RES) to the energy production mix. The main reason is the world-wide desire to reduce greenhouse gas emissions and attempt to limit the predicted average temperature increase (global warming). This may be seen from the Paris Agreement, where currently 196 countries have agreed to take steps to limit the world's temperature increase to a maximum of 2°C compared to pre-industrial levels by reducing their greenhouse gas emissions by at least 43% until 2030 [1]. Closer to home, the UK government has committed to becoming a net-zero country by 2050 [2] with the increased use of RES and nuclear energy. Furthermore, based on the most recent government study [3], on-ground solar farm installations currently have a competitive cost of electricity and are predicted to be the cheapest RES per MWh in the near future.

Another aspect that requires attention and finding a solution in RES is energy security. It is beneficial to be shielded against malicious actors that could influence the country's access to cheap energy via the restriction of sales, as was the case in the recent war in Ukraine (2022), or via cyber warfare. The UK government, for this reason, aims to decentralise energy production, with a particular emphasis on residential installations of photovoltaic (PV) systems, which allow local production of energy [4]. In the published policy papers, the aim is to increase fivefold the production of solar energy by 2035, to have a capacity of 70 GWp, enough to power

20 million average homes.

In pursuit of this goal, the government is attempting to incentivise households and small businesses to install rooftop solar arrays using advantageous financing schemes. Finally, another benefit of the decentralisation of energy production is the reduced amount of losses due to the transmission and distribution of energy. Ideally, the energy produced can be used by the household or by other persons in the near vicinity. This would also lower the stress on the power grid infrastructure, as less power will need to be delivered by power plants. Currently, there are valid concerns about grid stability and black-start capabilities with a high penetration factor of RES. However, this research area is heavily funded at the moment, and interesting solutions to uphold grid stability have already been proposed, such as the sychronverter [5], which mimics the properties of synchronous generators using advanced controls and energy storage elements. This is projected to allow a very high penetration level of RES in energy production and move towards a 100% RES-based grid.

Therefore, based on the benefits presented, solar energy is deemed worthy of examination within this PhD work. The competitive cost of energy production, improved energy security, and advantageous financing mean that residential solar applications show potential for a surge in growth. Thus, moving on to the structure and behaviour of a solar panel, its utilisation within a typical residential installation will be examined.

1.1 Photovoltaic Panels & Problem Statement

The solar cell is an electrically nonlinear element that converts insolation energy to a voltage differential based on the photoelectric effect. Due to its nonlinear nature, a maximum power point tracking (MPPT) algorithm typically needs to be used to extract the largest possible percentage of the insolation energy. Since the solar cell produces a relatively small voltage on its terminals and, therefore, a low output power, photovoltaic (PV) panels are created using solar cells connected in series,

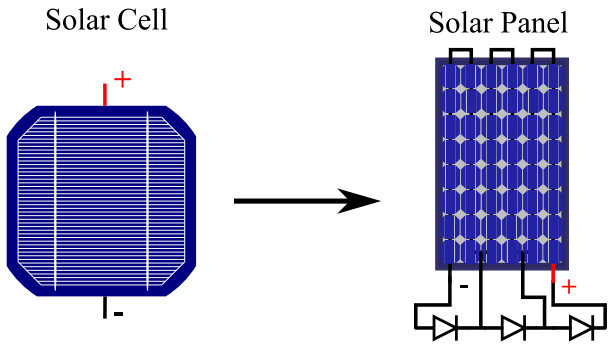


Figure 1.1: The solar cell and its utilisation in a typical PV panel.

typically comprising sixty or seventy-two cells as shown in Figure 1.1.

The aspects that affect the performance of an assembled panel are varied. The most significant performance factor is naturally the received irradiation on the solar cells. This might be diminished by natural or artificial shading, soiling of the panel, reflection losses, and spectral mismatch losses [6]. Accounting for this phenomenon, the effective irradiance may be computed, and the electrical behaviour of a PV panel, considering its effective irradiance, can be seen in Figure 1.2a. Another variable that affects the panel's behaviour is its temperature, and this dependency can be witnessed for the same panel in Figure 1.2b. From the previous figures, it might be noted that, generally, a PV panel will stay within a narrow maximum power point (MPP) voltage range, especially when the insolation is the primary variable.

As the solar cells are connected in series, they are forced to share the same amount of current. Considering uneven irradiation conditions between cells, it is possible that some cells might reverse their voltage polarity if a high enough current and insufficient insolation are provided. This will consume energy and create hotspots on the solar panel, which ideally should be avoided. Therefore, PV panels typically come with the addition of bypass diodes that can shunt the current away from the problematic areas. Ideally, every individual solar cell would have a bypass diode. Still, due to cost concerns owed to increased wiring and component count, only a few are placed in the panel's junction box, with a typical arrangement being seen in Figure 1.1. Should one of the installed bypass diodes be conductive due to a localised shading area, it would considerably curtail the panel's output voltage and, thereby,

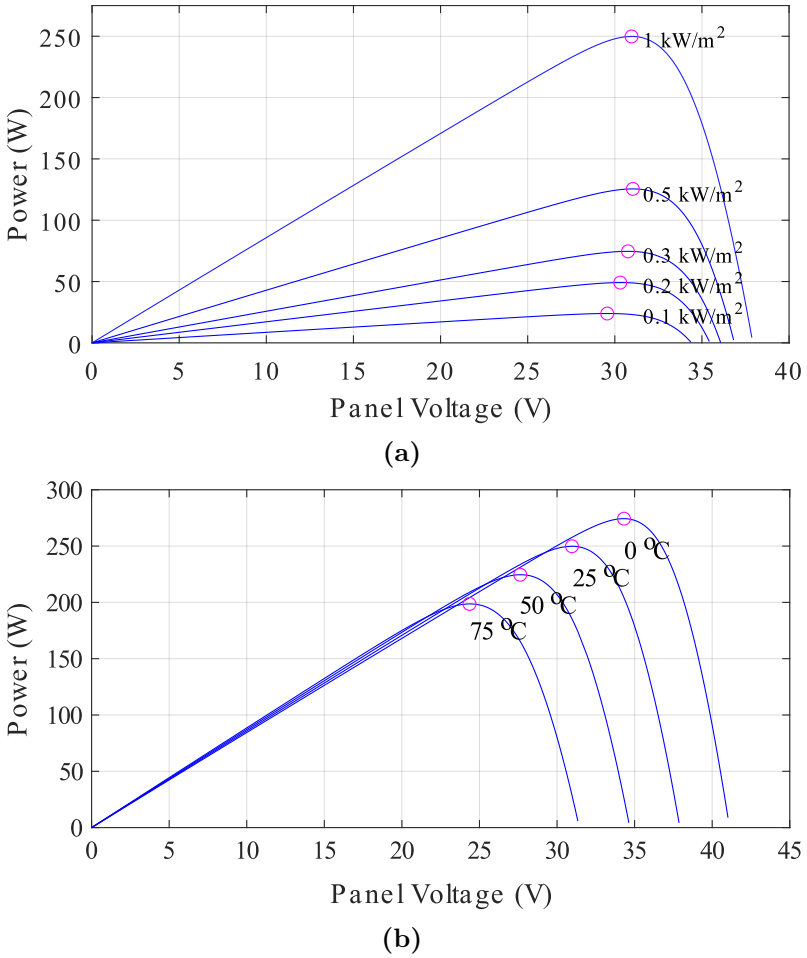


Figure 1.2: Typical 60-cell PV panel characteristic output power curves, which show dependency on irradiation variation and temperature variation.

its MPP voltage level.

However, even without the conduction of a bypass diode, shading can have detrimental effects on a panel. Since a panel is comprised of a large number of cells in series, if only a part of it is shaded due to nearby objects, peculiar phenomena can occur. The MPP voltage level can shift considerably towards the lower voltage levels, as can be seen in the simulation in Figure 1.3. To explain this intuitively, if a higher voltage is used with some sub-strings being shaded, the shaded substrings get forced into a low output power region, so it is beneficial to bring the panel to a lower voltage level where all solar cells contribute to energy production.

The methodology for calculating the merit of a power converter efficiency for PV panels differs on the area of the world you are based in. For example, in the United States, more weight is placed on high irradiance conditions. In Europe, the

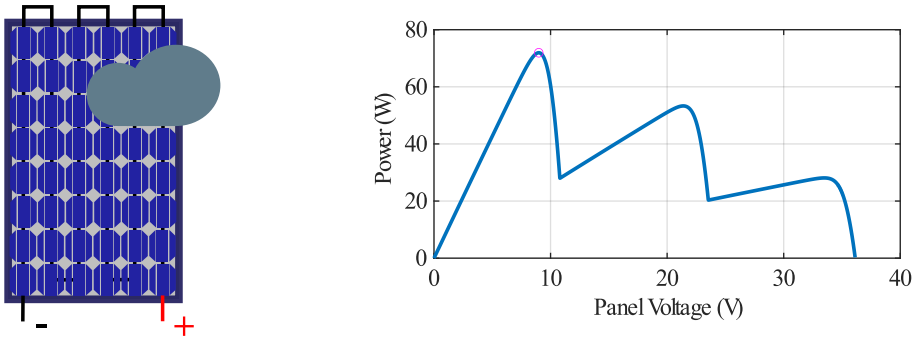


Figure 1.3: Effects of a partially-shaded panel. The MPP voltage has shifted considerably from its nominal value.

PV converter efficiency is weighted more heavily towards shaded conditions. The different metrics used can be seen in (1.1) and (1.2), with the first being the efficiency metric used in the US, created by the California Energy Committee and the latter being the efficiency metric in Europe, found in the EN 50530 standard. The variable η represents the power converter efficiency, while the subscript denotes the percentage of the rated power that is outputted.

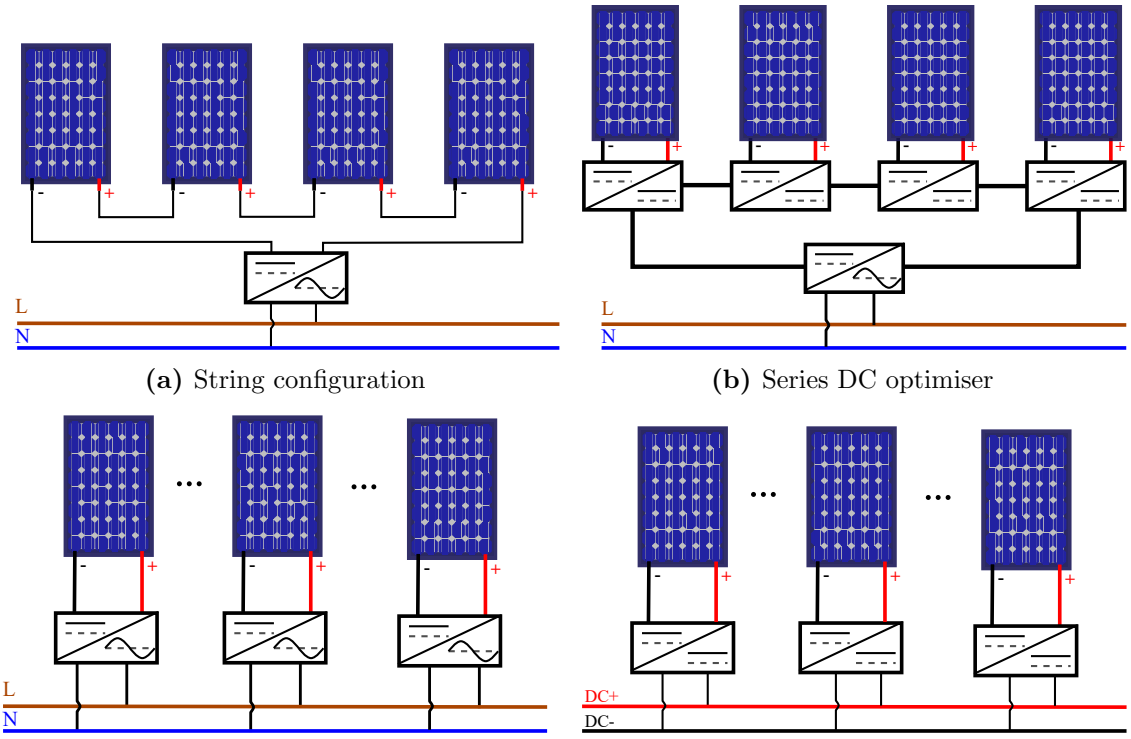
$$\eta_{CEC} = 0.04\eta_{10\%} + 0.05\eta_{20\%} + 0.12\eta_{30\%} + 0.21\eta_{50\%} + 0.53\eta_{75\%} + 0.05\eta_{100\%} \quad (1.1)$$

$$\eta_{EUR} = 0.03\eta_{5\%} + 0.06\eta_{10\%} + 0.13\eta_{20\%} + 0.10\eta_{30\%} + 0.48\eta_{50\%} + 0.20\eta_{100\%} \quad (1.2)$$

Generally, shading plays a central role as the PV installations are placed in an urban environment. In these cases, houses and businesses usually are placed in close proximity to one another. Therefore, shading from nearby buildings can be expected. Shading can also occur from nearby trees or from debris that lands on a PV panel. Since the shaded conditions are easy to appear and might lead to a considerably lower voltage MPP, it would be beneficial to create a power conversion system that can convert power efficiently from the PV panel, even when the MPP point is considerably lowered compared to nominal conditions.

1.2 Photovoltaic System Architectures

In the residential market of solar arrays, there are a variety of power architectures used to connect PV panels to the electricity network [7]. These configurations offer various advantages each, and a brief overview of their arrangement can be seen in Figure 1.4. The selection of the suitable power architecture for each installation must account for the historical insolation data, the orientation of the installation area, the possible shade-producing environment, the frequency of cleaning, as well as the cost of electricity to determine which of the presented architectures is preferable in each scenario.



(a) String configuration

(b) Series DC optimiser

(c) Microinverter

(d) Parallel DC optimiser

Figure 1.4: Different photovoltaic architectures that may be found in the residential segment.

As a short presentation, the string configuration in Figure 1.4a places a multitude of PV panels in series and converts the resulting high-voltage output into usable power using an inverter system. It benefits from being the cheapest solution as the electronics required are minimal. Since a large voltage step-up is not needed, the power converter efficiencies tend to be high. Its drawback lies in the fact that the PV

panels are not controlled independently; hence, in case of a power output mismatch, the whole system's efficiency suffers.

The concept of a series-connected DC optimiser shown in Figure 1.4b solves the issue mentioned above, which is that a power mismatch can deteriorate the system's efficiency. Instead, each panel has its own DC-DC conversion system at its terminals, which tracks the MPP of the panel to provide maximum energy harvesting. The benefit of this approach is that it has the potential for individual panel MPP tracking. Because the DC-DC converters do not need a high voltage step-up capability, typically, these solutions propose a very high conversion efficiency. The drawbacks include the smaller installation flexibility, as multiple panels need to be grouped, and the challenging control strategies required to achieve a local MPP in a system with numerous connected converters [8].

Finally, in Figure 1.4c, the concept of a microinverter is shown. In this scenario, each panel has individual voltage control, allowing for MPP tracking. The same holds for the parallel DC optimiser shown in Figure 1.4d. The difference is that the former connects directly to the AC utility grid, while the latter connects to a DC bus. The DC bus can be connected to an inverter to create a voltage compatible with a utility grid or be used within the concept of a DC microgrid. Both of these architectures allow for better solar energy yield but suffer naturally from increased costs due to the high number of electronics required. Also, both of these options have converters operating independently, which allows maximum flexibility in the installation and scalability of a PV array and inherent fault tolerance, as the failure of one panel or power electronic module doesn't affect the rest of the system's performance. Monitoring software might also be used to notify users of any issues with a specific panel, and panel-level protection systems such as rapid shutdown can be implemented in these configurations, as is the case with the recent Enphase IQ8 microinverter.

However, what makes the architecture of parallel-type DC optimisers unique is their flexibility in connecting to a DC bus. In recent years, the idea of installing

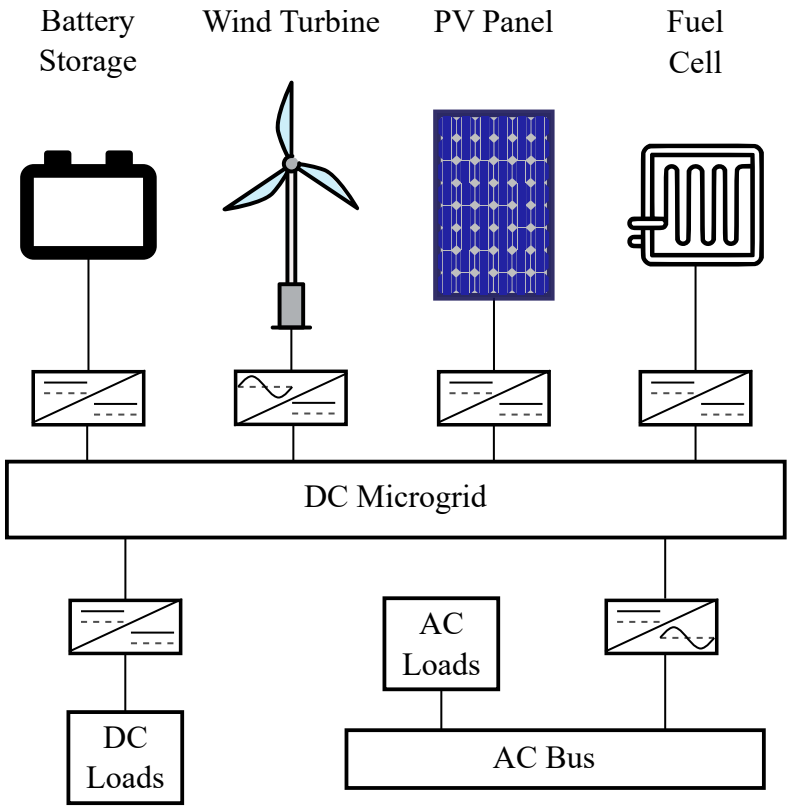


Figure 1.5: The concept of a DC microgrid.

a DC microgrid in conjunction with AC power has taken off. This happened due to the rapid increase in equipment that is inherently based on DC voltage, such as energy-storage batteries, solar panels, LEDs, and electric cars, which could be used more efficiently if a DC power system is used. Directly utilising the generated solar power via a DC microgrid, as shown in Figure 1.5, has already shown to have case studies where it makes financial sense [9]. At the present moment, in the European continent, the Netherlands are leading the way in using a hybrid AC/DC power system approach in buildings. Innovative companies such as DC Systems, now part of Schneider Electric, are currently developing DC microgrids to combat the rapid increase of energy demand in the country [10]. It might be noted that even at home, the UK currently suffers problems due to insufficient power grid infrastructure [11], to which DC microgrids could offer some relief.

Adding to the use of solar panels within a DC microgrid, another benefit can be found within the realm of Building Integrated PV (BIPV) panels. These are PV panels that may be used as building materials without affecting the appearance

of buildings considerably. Thus, they allow for a much larger solar energy harvest compared to a building installation comprising simply rooftop panels. This aligns with the goals of the EU to create net-zero public buildings [12], as well as the UK Future Homes Standard [13], which aims to reduce carbon emissions created by buildings.

Concerning the BIPV implementation, existing literature has found the limitations of the state-of-the-art conversion systems in the case of BIPV curtain walls. It is found that the current offerings of module-level converters currently lack the correct dimensions to allow for panel embedding, plus they shut down during operation due to thermal concerns. This happens as these converters need to be passively cooled, so thermal management becomes a challenge. Combined with the high ambient temperatures (sometimes exceeding 75° C), the system's over-temperature protection becomes active and shuts down the conversion system. Furthermore, in the case of panel-embedded parallel-type DC optimisers, the time and cost of BIPV installation can be reduced since a qualified electrician is not needed, nor is a detailed study in the geometry of the structure as the panels operate independently [14].

Another concern with BIPV designs is that of reliability. A thorough overview of the reliability concerns of the BIPV conversion system can be seen in [15]. The reliability concerns in this application area are of increased importance, first because the PV converter is integrated with the panel, making it more costly to replace, and second, because of the increased ambient temperatures of the system due to environmental exposure.

To achieve long-term (25+ years) reliability, a low component count in the converter is prioritised, as transistors and their gate drive are components that account for a significant cause of failure. Furthermore, capacitors are also a common failure point, with MLCCs being the most reliable capacitor technology and showing good tolerance to high temperatures. Still, they can get damaged from PCB bending due to thermal cycling. To combat this, J-lead capacitors might be used to prevent MLCC cracking. Magnetic components have been found to be very reliable over the

years. However, they typically offer low power density figures, which might cause conflict with the dimension requirements [16].

1.3 Thesis Aim & Outline

Based on the discussion in the previous section, it is evident that improvements can be made to the parallel-type DC optimiser. Currently, there is a lack of slim converters in this category. Plus, the high ambient temperatures leave little headroom for temperature increase in the converter, forcing the conversion system to shut down. Therefore, the aim of this thesis is to improve the state of the art in this area.

This is intended to be achieved by using Gallium Nitride (GaN) transistors and proposing a topology that is poised to extract the maximum benefit from their application. The beneficial material properties of GaN devices will be examined in detail in later sections, but there is already evidence in the literature of their application-oriented benefits. The parallel-type DC optimiser comprises low-voltage and high-voltage (typically 100 V and 650 V, respectively) rated transistors. Both of these types of transistors have been benchmarked favourably in the literature when compared with silicon devices [17, 18]. In these references, some of the beneficial properties discovered are the absence of reverse recovery phenomena, very low gate driving losses, and low switching losses.

Based on the discussion above, the objectives of the proposed conversion system are:

- Offer a high voltage step-up ratio to allow connection to an inverter DC-link or, alternatively, a DC microgrid.
- Have compact dimensions to allow for the application within the BIPV concept. The lateral dimensions of the converter are of secondary importance, while the height should be minimised to fit into BIPV frameworks [19].
- Allow for a wide range of input voltage regulation to extract solar power even under partially shaded conditions.

- Provide high efficiency over a wide input voltage range, again to allow for a better solar energy yield.

- Allow for operation under high temperatures; this can be achieved mainly by creating an efficient conversion system to keep losses low, as heatsinks would increase the overall dimensions.

- Provide galvanic isolation to protect the operator when performing maintenance and to limit the leakage currents that can trip RCDs while also conforming to grid-connection regulations without the need for bulky common-mode filters.

The conversion system will be assumed to be concerning a typical 60-cell solar panel, with 300 W output power. However, this converter will be scalable to other power levels with minor design alterations. The overall design aims can be seen in Table 1.1. The maximum available profile has been taken from the literature in order to laterally fit in BIPV facade elements [14]. However, values smaller than this maximum dimension are desirable to allow better opportunities for cooling. It has been found in [20], that the space behind the PV panel inside a facade framework can be used for convection cooling. Therefore, space should be available to allow ventilation.

The efficiency goals depend on the maximum heat extracting capabilities of the system, which is difficult to model without knowing the precise cooling setup. Based on the available solutions in the literature, a competitive figure was selected. With a 98% efficiency, the converter will be generating 6 W of heat at nominal power, allowing for a modest goal of converter to ambient thermal impedance. Nevertheless, thermal design is outside the scope of this thesis.

The presented thesis comprises seven chapters. Its structure is as follows:

Chapter 1 presents the worldwide desire to limit greenhouse gas emissions by using various RES, such as solar. It shows the structure of the solar panel and the variables that affect its performance. Residential solar panel installations are shown to be an interesting choice, and an overview of various installation methods is

Table 1.1: Summary of targeted converter design values.

Design Variable	**Desired Value**
Input Voltage	8-35 V
Nominal Power	300 W
Output Voltage	350-400 V
Maximum Height	29 mm
Efficiency (full load)	$\geq$ 98%

displayed.

Chapter 2 showcases the beneficial properties of GaN transistors. Then, a survey of various solutions for the parallel DC optimiser applications found in the literature is presented.

Chapter 3 provides the proposed converter's schematic, operational logic, and a detailed description of its operational states. Furthermore, the design procedure for the magnetic components is shown, along with a verification of the theoretical analysis using the simulation software PLECS.

Chapter 4 examines the benefits of GaN transistors experimentally. Critical parameters for the efficient operation of the converter, such as the $C_{oss}(V)$ and the switching loss during turn-off, are tested experimentally.

Chapter 5 shows the converter's creation in a lab environment and several pitfalls faced by the author. Solutions are proposed to overcome the design challenges, and results are taken that are consistent with theoretical predictions.

Chapter 6 attempts to recreate this conversion system with a considerably higher switching frequency. More design pitfalls are presented, along with solutions. The experimental results of a slim, 1 MHz converter are shown, and avenues to improve its performance are suggested.

Chapter 7 summarises the work undertaken and the achievements within the PhD time frame. Extensions to this research are also suggested.

Chapter 2

Literature Review

2.1 Introduction

As per the title of this thesis, the aim is to create a slim converter for parallel-type DC optimiser applications, by utilising high-frequency switching conversion. The newer Gallium Nitride devices are expected to enable high-frequency conversion, as they allow for much faster switching intervals. Therefore, in this chapter, an overview of the technology behind GaN High Electron Mobility Transistors (HEMTs) is first provided. Their benefits compared to silicon devices are also shown. Afterwards, a survey of various solutions found in the literature is conducted concerning the implementation of a parallel DC optimiser. This will help identify the research gap that is available and the benefits of the proposed converter compared to other implementations.

2.2 GaN High Electron Mobility Transistors

Up to about a decade ago, most power electronic conversion systems were based on Silicon power semiconductors. This was after a giant leap forward in the 1960s with the creation of silicon power MOSFETs, which offered considerable advantages compared to bipolar junction transistors (BJTs) and allowed switching frequencies in the order of tens or even hundreds of kiloHertz. A similar leap forward has been

Table 2.1: Properties of the most common semiconductor materials [21].

	Silicon	**GaN**	**SiC**
Band Gap (eV)	1.12	3.39	3.26
Critical Field (MV/cm)	0.23	3.3	2.2
Electron Mobility ($cm^2/V \cdot s$)	1400	1500	950
Thermal Conductivity ($W/cm \cdot K$)	1.5	1.3	3.8

made in recent years by the manufacturing of wide band gap (WBG) devices, which, due to their inherent properties, allow for efficient power conversion at even higher frequencies, permitting even smaller conversion systems with high efficiency. The intrinsic advantages of the popular Gallium Nitride and Silicon Carbide devices may be seen in Table 2.1.

To give a better understanding of the benefits highlighted in Table 2.1, the band gap is the minimum energy required to move an electron from the valence band to a conduction band. A higher band gap is generally associated with lower leakage currents in a device, along with a higher tolerance to high temperatures. The critical field is the electric field required to create impact ionisation, and a high value indicates that a smaller drift region is necessary to block a specified voltage level. This leads to more compact devices for the same voltage rating, reducing the associated junction capacitances of a transistor. Similarly, a smaller drift region requirement to a lower $R_{ds,on}$ for a device of the same die area is based on the fact that the high critical field allows for smaller drift regions and with a higher carrier concentration. For a more thorough presentation of the claims in this paragraph, the underlying equations behind these statements may be found in Baliga's work [22].

Based on the discussion presented, it would be reasonable to expect that Gallium Nitride devices will show the best performance based on the fact that they possess the highest critical field values and high electron mobility. The high electron mobility is partly achieved by the concept of the Two-Dimensional Electron Gas (2DEG) in lateral devices. Because a thin layer of AlGaN is grown on top of the GaN crystal structure, a strain is created due to the crystal lattice mismatch. Based on the crystal's inherent polarisation and the piezoelectric effect, this heterojunction creates

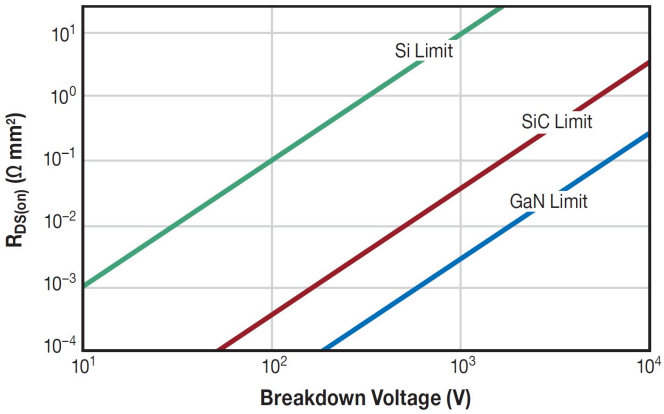


Figure 2.1: Least possible device on resistance per square millimetre, against its blocking voltage, shown for Si, SiC and GaN devices [21].

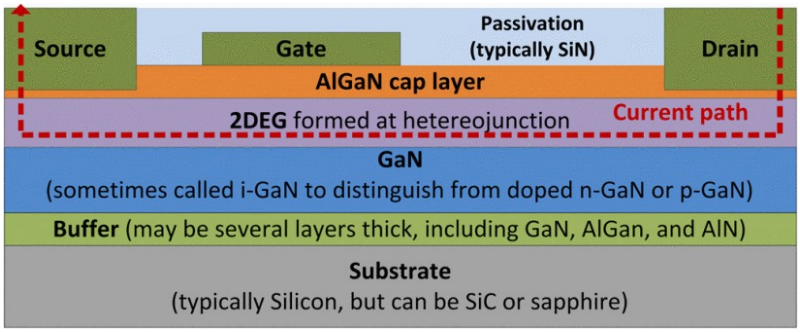


Figure 2.2: Construction of a lateral GaN HEMT [23].

an area with a high number of conductive electrons [21]. Indeed, looking at Figure 2.1, it is seen that the device theoretical limits for GaN devices allow for a smaller die size for an equal voltage and $R_{ds,on}$ rating, rendering them ideal as fast-switching devices to be used in high-frequency power conversion.

Based on the creation of the 2DEG, there is an inherent conduction channel in GaN HEMTs, rendering them a normally-on device. The typical lateral GaN HEMT device construction may be seen in Figure 2.2, in which the creation of a conductive channel may be seen. This is known as a depletion mode (d-mode) device, and a negative voltage on the gate relative to the source and drain pins has to be applied to cut out the conduction channel. A normally-on device isn't desirable when using voltage-source converters due to reliability concerns, as without controls, the devices would short-circuit the input source.

Since a normally-on device isn't usually desired, various methods of converting the devices into normally-off devices have been created. To alter the gate voltage

threshold on a device level, the methods to increase the gate threshold voltage to positive levels can be summed up as either thinning the AlGaN layer to create a smaller voltage differential due to the piezoelectric effect, injecting additional atoms below the gate to make a trapped negative charge, or creating a p-doped GaN layer below the gate, that has a voltage differential larger than the one caused by the piezoelectric effect [21].

Another method is by cascading a GaN HEMT with a low voltage Si MOSFET, with the MOSFET's source being connected to the GaN device's gate pin. With this method, if the Si device is in the OFF state, it will automatically force the GaN HEMT to turn off due to its negative V_{gs}, owing to the voltage drop on the Si MOSFET. Naturally, this method of cascading two devices will result in higher $R_{ds,on}$ and junction capacitances; however, it has its merits due to the improved noise immunity owed to the higher threshold voltage of Si MOSFETs, so they might find their use in applications with very high dV/dt transients, with increased ruggedness requirements [24]. However, in this work, efficiency is prioritised, so the enhanced mode (e-mode) GaN HEMTs will be used. It has already been shown that for high-frequency and soft-switching applications, e-mode GaN HEMTs possess the highest performance [25], showcased as a lower amount in total losses when compared with other cascode GaN and SiC devices.

Similar conclusions to the superiority of GaN e-mode HEMTs in the literature have been made by Li et al. [26] when compared with similarly rated SiC devices. In this work, the 650 V GaN device obtains lower conduction and switching losses versus a similarly rated SiC MOSFET. Furthermore, there is currently a wealth of publications in the literature that have proven experimentally that GaN HEMTs provide the highest performance in applications up to 400 V, compared with available Si and SiC devices [27–30]. This further cements the decision to move forward with their usage in this thesis.

One of the challenges that might occur with the use of the GaN devices that have been reported in the literature is the current collapse effect, otherwise known

as dynamic $R_{ds.on}$ [31, 32]. This effect causes temporary increased channel resistance or even permanent channel resistance increase, depending on where the electron trapping occurs. The cause behind this phenomenon is the high electric fields seen between the gate and drain pins of a GaN HEMT, which can provide enough energy for the electrons to jump to the passivation layer or even the GaN or buffer layers of the device pictured in Figure 2.2. The electrons that get ejected into the passivation layer typically recombine with the gate, but electrons that have jumped to deeper layers can cause lasting $R_{ds,on}$ increase [33].

Of course, this can be a significant threat to the applicability of a high-frequency GaN converter for the examined application. Thankfully, device manufacturers have lowered the impact of the dynamic $R_{ds,on}$ by using field plates to spread the electric field more evenly within the device [33]. This is why it is common for sold GaN devices to have their substrate connected to the source, with the inconvenience of more challenging thermal management, as heatsinks would need to be isolated.

Another challenge that's expected to be faced in this thesis is centred around EMI concerns. The low junction capacitances of GaN HEMTs will allow for fast switching intervals and, therefore, create a higher frequency noise sprectrum. These transitions limit the applicability of the commonly used leaded transistor packaging technologies, as those increase the switching losses and limit the switching frequencies considerably [34]. Instead, flip-chip and QFN packages tend to get used, which offer minimal lead inductance, allowing for fast and efficient switching if paired with a low-inductance PCB routing layout [33].

To ensure that the converter that will be proposed within this thesis has a good chance of being reliable for the typical 25-year warranty given by solar panel manufacturers, reliability data was sought. EPC corporation are very active in releasing reliability data for their devices, and luckily, they are also releasing reliability data tailored to the solar market in their recently published reports. In their latest report [35], the solar applications are examined in section 4.1, which provides reliability data for a microinverter or DC-optimiser scenario. They have shown,

via accelerated ageing tests, that gate voltage stresses and dynamic $R_{ds,on}$ effects don't pose a threat to the 25-year expected lifespan. The most significant danger to the GaN reliability for solar was identified as solder cracking due to thermal cycling. Nevertheless, by selecting a suitable underfill material with an equal thermal expansion coefficient as the solder joints, they have been shown to achieve good reliability with their devices for up to $70° C$ of thermal cycling. The result is that GaN transistors are again deemed suitable for use in this application, based both on performance and reliability data.

2.3 PV Module Power Converters

In the examined application area and power conversion systems in general, there are two main categories of conversion systems used. Those are the PWM-controlled conversion systems and resonant converters, which depend on tuning a resonant network. Within the PWM-based conversion systems, the interface between the switching devices and the energy source (capacitor, inductor, etc.) alters the behaviour of the converter. Therefore, in this section, various PWM-based converters will be presented, with different energy interface components (voltage, current, and impedance source). The advantages and drawbacks of each system for the examined application area will be explained. This will assist in the decision of the conversion system to be implemented in this thesis.

2.3.1 Flyback Conversion Systems

With the requirements for an isolated, high-voltage step-up conversion system and relatively low power outputs required, the Flyback converter would immediately spring to mind. Its typical schematic may be seen in Figure 2.3, and it does benefit from a very low semiconductor count, plus the ability to perform PWM, thus keeping a constant switching frequency and simplifying the magnetics design. However, the flyback converter suffers from some inherent problems. One of them is that

the magnetic component utilisation is low, as the transformer is excited at one time period, and the power transfer to the secondary side occurs at another time period. This results in reduced efficiencies and a larger magnetic core size [36]. Another inherent problem is that the energy stored in the leakage inductance of the transformer has nowhere to go when the active device turns off and, therefore, produces considerable ringing formed by leakage inductance and the active device's junction capacitance. This results in additional heat dissipation, active device derating, increased susceptibility to dynamic $R_{ds,on}$ phenomena, as well as EMI concerns [37].

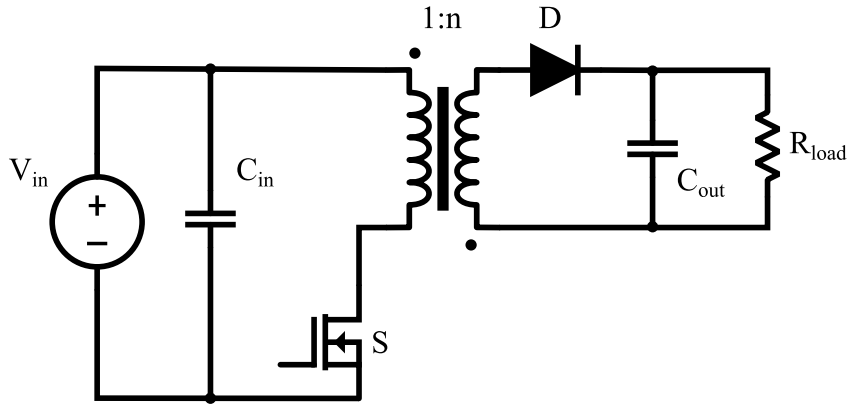


Figure 2.3: Flyback step-up converter.

Naturally, engineers and researchers have worked around the mentioned problems to increase the performance of flyback converters. The most fundamental improvement is the introduction of the active-clamp flyback (ACF) converter [38], shown in Figure 2.4, which has the capability to recycle the energy stored in the leakage inductance and provide ZVS turn-on for the active devices. This is a significant improvement on the flyback converter with a minor addition of components. Another method used to recycle the energy stored in the transformer's leakage inductance is by using a two-switch flyback conversion system [39]. This solution has two diodes in series conducting the leakage energy when the active switches turn off, and therefore adds considerable conduction losses, while not solving the issue of low magnetic utilisation, so the ACF conversion solution tends to be more attractive when the input voltage isn't considerably high.

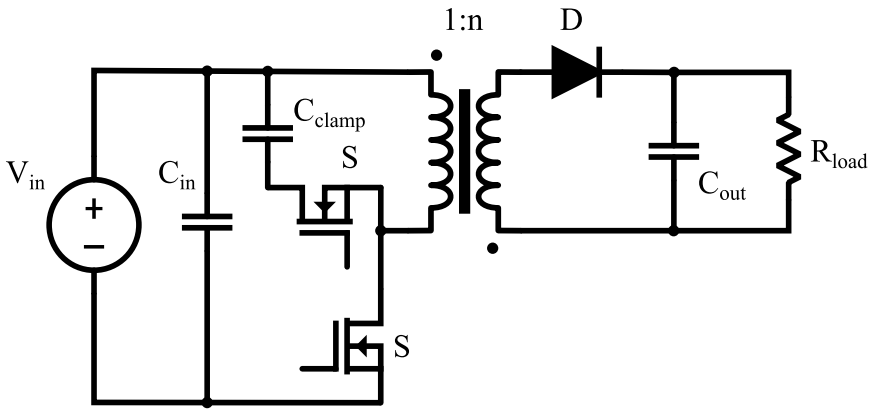


Figure 2.4: Flyback converter, with an active clamping branch.

From the introduction of the ACF converter to today, various additional methods have been proposed to extract more efficient power conversion from the flyback converter family. Some researchers have constructed interleaved flyback conversion systems [40], while the concept of integrating two types of conversion systems has been explored by combining the principle of the boost converter and the flyback in [41]. In addition, the concept of adding a resonant capacitor to extract the benefits of the series resonant converter (SRC), with the addition of a voltage doubler cell, has been explored in [42, 43]. Finally, the concept of performing frequency modulation to extend the percentage of time in which power transfer occurs has been proposed in [44].

Despite the interesting proposals that have been made thus far, the maximum efficiency found in the mentioned works was 96.7% in [43]. This is a very high efficiency, especially for a flyback-based conversion system. However, in general, the proposed solutions do not upkeep these high-efficiency numbers in a wide range of voltage and power scenarios.

2.3.2 Current-Source Conversion Systems

Apart from flyback converters, current-source converters might be considered for this application. Indeed, current-source converters have an inherent advantage in the voltage step-up application area. This is because their intrinsic mechanism is to boost an input voltage source, as an inductor is interfaced between the energy

source and the switching devices [45]. This is in opposition with voltage-source conversion systems, where their inherent mechanism is to chop an input voltage source provided by the input capacitor. Similar to the Flyback conversion systems presented previously, this family of converters are normally controlled using PWM, with a fixed switching frequency. A typical example of a current-source conversion system is provided in Figure 2.5, and it shares similar problems to the Flyback converter, which is that the power conversion efficiency is reduced due to the high amount of V_{ds} ringing, owed to the leakage inductance of the transformer, plus hard switching events on the primary-side devices.

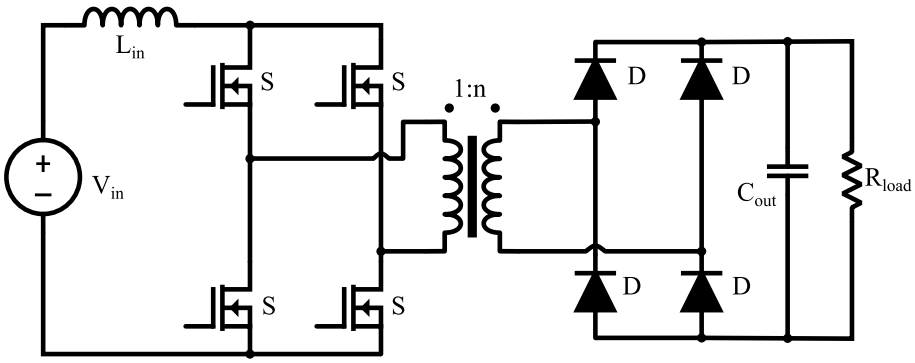


Figure 2.5: Full bridge current source converter.

Naturally, there are various ways to remedy the problems mentioned above. Much research has focused on voltage clamping techniques, which can stop the switch from ringing in a non-dissipative manner, with an example being shown in Figure 2.6. In addition, these techniques can also permit the ZVS turn-on of the primary-side power switches, thus increasing the conversion efficiency [46, 47]. Furthermore, Prasanna et al. presented a novel half-bridge current-source converter that kept the benefits of soft-switching and zero V_{ds} ringing, which was achieved by controlling an active full-bridge on the secondary side of the converter [48, 49]. This proposal achieved high efficiencies with a wide load and input voltage range. However, it still has some operating regions where the ZVS turn-on is lost, thus limiting its efficiency.

Rathore et al. proposed an L-L type converter to achieve ZVS turn-on with a wide input voltage range [50]. Still, it has a high number of active switching devices (eight), and the primary-side switches turn off while conducting load current,

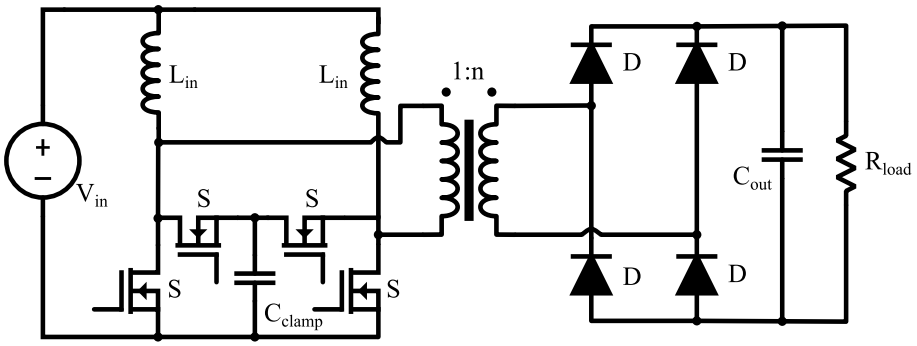


Figure 2.6: Current source converter with an active clamping branch.

providing additional losses. Later work from this researcher added an LC resonant tank, and this allowed the converter to achieve ZVS and ZCS on the primary-side devices while using frequency modulation [51]. Nevertheless, in a recent review paper of the current-source converter family [52], the more efficient choice is said to be the naturally clamped option, with an example being the work in [49]. While this conversion system may achieve high efficiencies with a wide load and input voltage range, it still lacks efficiency when compared with the efficiency numbers that can be offered by resonant power conversion. Plus, having an input inductor can pose a threat to the requirement for a low-profile conversion system.

2.3.3 Impedance-Source Conversion Systems

Another PWM-controlled converter family that is usually examined for this application area is the impedance-source converter. This type of conversion system has the inherent advantage of being able to provide both buck and boost capabilities, as the interface between the energy source and the active devices comprises both inductors and capacitors [53], as shown in Figure 2.7. Because of this, they have gathered research interest due to their flexibility in providing voltage step-up or step-down. Some of their weaknesses, such as the high passive component stress and the discontinuous input current, have been addressed by rearranging the quintessential elements of the impedance tank, creating the quasi-Z-source (qZS) converter family [54].

A variety of impedance tanks have been studied in the literature. In the cases

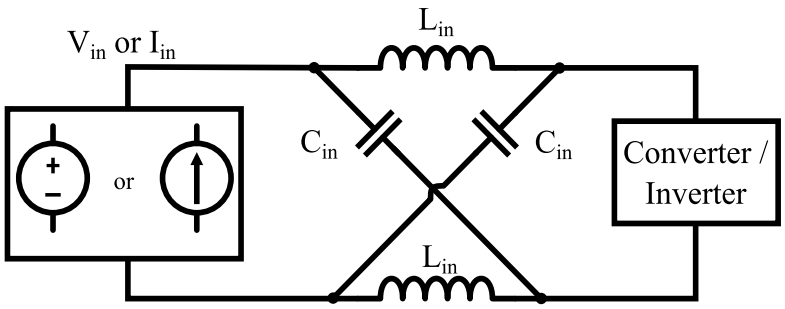


Figure 2.7: Typical schematic of impedance-source conversion systems.

where a wide voltage gain ratio is offered, like in the qZS converters or the Y-source converters [55], the energy that needs to be stored in the tanks' inductors make these types of converters unattractive for achieving a high volumetric power density. Vinnikov et al. [56–58] have proposed an attractive solution to this problem. They have configured the two inductors of the qZS into a coupled inductor pair in a manner that generates less maximum flux within the core. This enables the use of smaller magnetic cores and allows for more power-dense solutions.

In their proposals, to provide voltage step-down, phase shift modulation is used to limit the voltage excitation on the step-up transformer. To provide voltage step-up, they utilise the shoot-through mode of the qZS converter, effectively short-circuiting the impedance tank to store energy similar to the boost converter principle. While they achieve wide input voltage regulation, with high efficiencies and relatively compact converter dimensions, the boosting function is delegated to the primary-side devices, which is not ideal in a high voltage step-up converter system. This is because the current values are considerably higher on the primary side, so it would make more sense from the point of efficient power conversion to have the secondary-side devices provide the boosting function. This is the case, as the high-voltage devices on the secondary side, owing to their smaller junction capacitances, may turn off faster, even though the $V_{ds} \cdot I_{ds}$ is constant, enabling lower turn-off switching losses. This would allow for better efficiency at high switching frequency conditions.

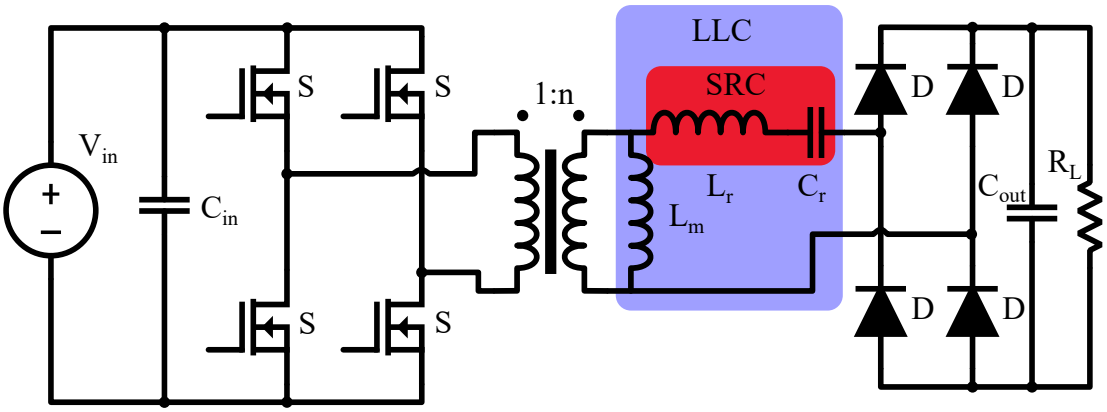


Figure 2.8: The most common resonant conversion systems are the LLC and the SRC. It may be seen that schematic-wise, they are the same, but the resonant components involved differ.

2.3.4 Resonant Conversion Systems

Another category of conversion systems that can be used in this application area is resonant converters. The most well-used resonant conversion systems are the series resonant converter (SRC) [59] and the series-parallel LLC converter [60]. These have gotten much attention due to their high reported efficiencies of over 98%. The schematics for both of the mentioned conversion systems may be seen in Figure 2.8. In the schematic shown, the defining characteristic of the conversion system is the resonant tank, and the primary-side and secondary-side devices can be replaced by a half-bridge, push-pull, active full bridge or other topologies.

Both converters typically achieve voltage regulation by pulse frequency modulation (PFM), which controls the converter by altering its switching frequency. Concerning the SRC, its most efficient operating point is at a switching frequency that's slightly lower than the tank's resonant frequency [61]. At this operating point, energy is transferred from the energy source on the primary side to the load on the secondary side for almost the entirety of the switching period. Some extra time is added to aid in achieving ZVS turn-on the primary-side devices. However, this is usually negligible compared to the total switching period. Additionally, near-ZCS is achieved on the primary-side devices, and ZCS turn-off is achieved on the secondary-side devices at this operating point. Therefore, it may be understood that this is an excellent topology for applications with a fixed input and output voltage level, such

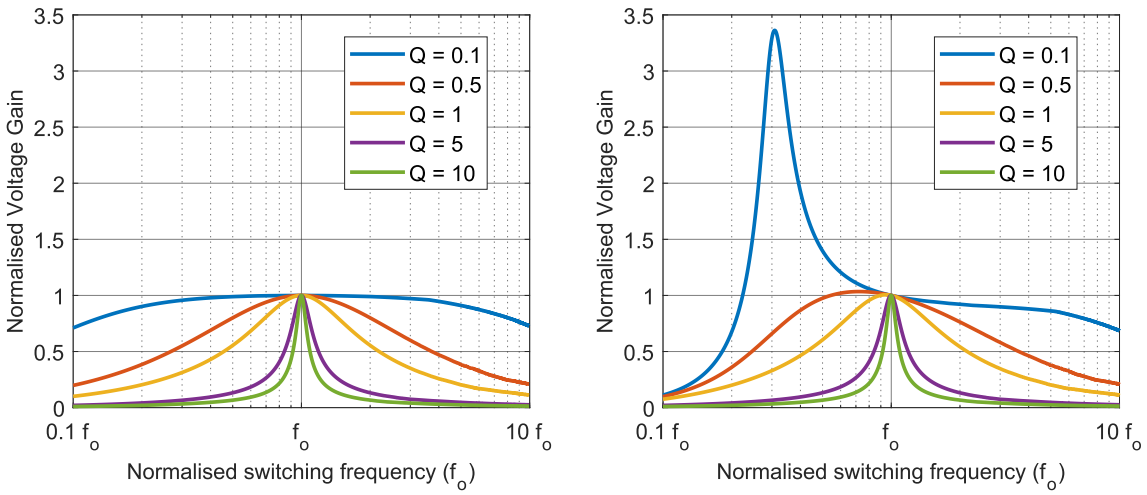


Figure 2.9: The power conversion voltage gain shown for the SRC conversion system (a) and the LLC conversion system (b) for $L_m/L_r = 10$. It may be seen that the SRC has only step-down regulation, while the LLC provides both step-up and step-down regulation at light loads. Q signifies the power outputted by the converters, with the relation of $Q = Z_r/R_e$. It can be seen that lower Q factors mean low power output.

as the DC transformer (DCX) applications [62]. The weakness of this topology is that it only performs voltage step-down when PFM is attempted [63].

Research has shown that using a three-element resonant tank is an enabler of both wide input voltage and wide load range regulation [64]. The LLC is the one that will be investigated in this research, as it has higher reported efficiency compared with the LCC conversion system [65]. It is shown pictorially in Figure 2.9 that the LLC can provide both voltage step-up and step-down functionalities. The pitfall in this converter's design is that the regulation is influenced by the relation of the magnetising inductance and the leakage inductance ($m = L_m/L_r$), with a lower value of m offering a wider input voltage regulation range. However, designs with a low value of m signify a smaller magnetising inductance, which translates to higher values of circulating currents in the primary-side bridge. Plus, the used frequency modulation will complicate the transformer's design, as it will need to take into account a range of operating frequencies, each having a different value of magnetic flux swing.

As indicated above, both the SRC and the LLC converters can achieve high efficiencies, with the downside of having a limited input voltage regulation range or

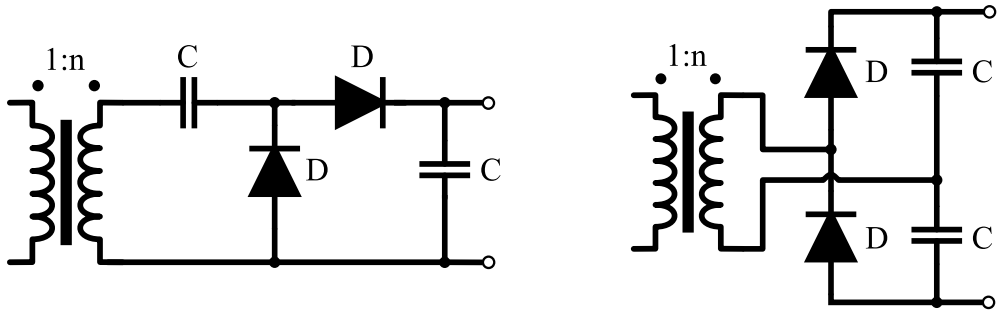


Figure 2.10: Most used voltage doubling techniques, the Greinacher circuit on the left, and the Delon circuit on the right.

reduced efficiencies with a wide voltage regulation range. Researchers have focused on topology-morphing conversion systems to extend the benefit of the high efficiency of the resonant converters to a wide voltage range regulation. For example, Hu et al. have proposed an LLC converter with a second transformer, which is controlled by a bidirectional switch, while also allowing the reconfiguration of the primary-side devices from a full-bridge (FB) to a half-bridge (HB) configuration [66]. Jovanović et al. have also proposed on-the-fly topology morphing of the LLC converter, switching between a FB and HB front-end, to achieve an efficient regulation with a wide input voltage range [67]. Shen et al., in a similar fashion, also proposed a reconfigurable primary bridge [68, 69]. However, instead of utilising a second transformer to increase the voltage regulation range, they chose to have a reconfigurable rectifier that can enter a "voltage-doubling" mode. The most common voltage doubling circuits found in the literature may be seen in Figure 2.10.

Furthermore, the research conducted by Shen et al. has been extended to include a variable DC-bus voltage [70], resulting in an even wider input voltage regulation. However, this solution only has merit in microinverter applications and not in the case where a fixed DC-bus voltage is required. Another proof of concept for the reconfigurable primary bridge is found in [71], where modulation is achieved by switching between an HB and FB topology. Still, it offers an insufficient regulation range for PV applications. The follow-up work found in [72] combined the reconfigurable primary bridge with a dual-mode resonant tank enabled by the use of two transformers. While it improved on the regulation range, the increased

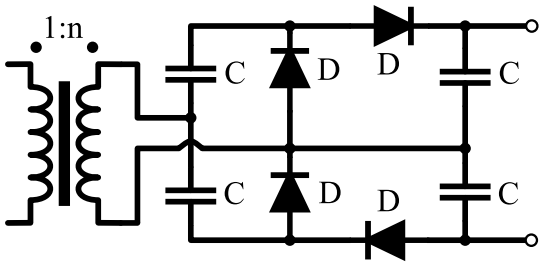


Figure 2.11: Voltage quadrupler, by combining multiple Greinacher doublers.

number of magnetic components is a considerable downside.

Aside from reconfiguring the primary bridge and using dual-mode resonant tanks, some researchers have chosen to regulate the parameters of the resonant tank. For example, Wei et al. propose altering the series inductor's inductance in the LLC converter by inserting a DC current bias [73, 74]. This proposal would require higher safety margins concerning the inductor's core saturation, thus lowering the achievable power densities. The same concept has been used to alter the value of the resonant capacitor by applying a DC-biasing voltage [75] to change the value of capacitance, with another option being to use switches to reconfigure the resonant capacitor [76]. The capacitor-altering techniques do offer a voltage regulation extension, but not enough to make them an excellent parallel-type DC optimiser.

Next, many researchers have suggested the use of a reconfigurable voltage-multiplier rectifier on the secondary side [77–81]. The main idea is to use active switches to reconfigure the topology of the secondary-side bridge in order to alter the voltage step-up of the conversion system. What is typically done is that the rectifying bridge may change from a full bridge to one of the voltage doubling circuits shown in Figure 2.10, which sometimes are also combined to perform a four-fold amplification of the input voltage, with a circuit such as in Figure 2.11. This type of solution offers a good regulation range, albeit at the cost of increased component count.

Finally, another way to increase the regulation range of the resonant converters is to combine their modulation with the principles of PWM conversion systems. For example, Mao et al. combined pulse frequency modulation with a phase-shifted

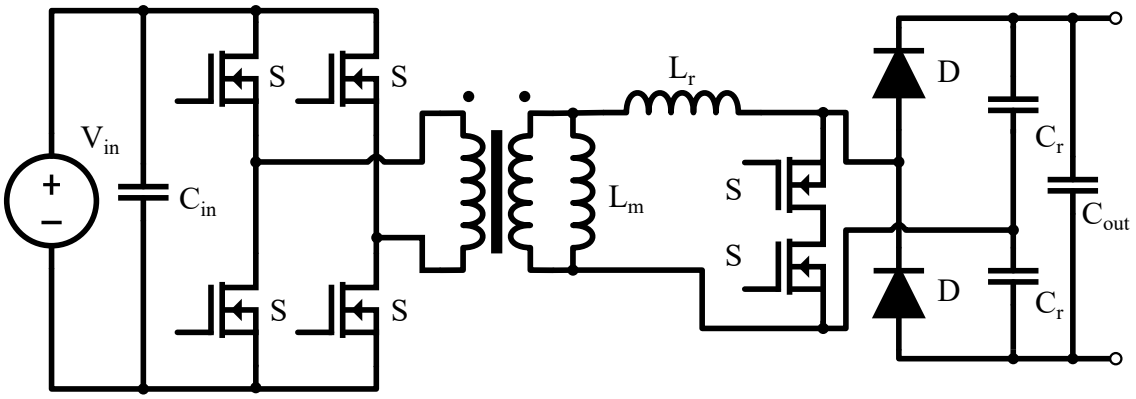


Figure 2.12: Converter proposed by LaBella et al.

PWM to provide increased efficiency when the LLC converter operates above its resonant frequency [82]. Using phase-shift modulation to step down the voltage in resonant converters is a recurring theme in the literature [83–85], and it was found to be the most efficient method to step-down voltage in the SRC [86]. To provide voltage step-up, LaBella et al. first proposed the concept of using the resonant inductance in a manner similar to the boost converter. That is, using a bidirectional switch, the transformer is momentarily shorted to store energy in the resonant tank inductance, which then provides voltage step-up without the need for frequency modulation [87, 88]. The schematic of the implementation may be seen in Figure 2.12, and in his works, high efficiency was achieved with a wide load range and a relatively wide input voltage range.

Moving on from this conversion principle, Bakeer et al. modified this converter by rearranging the position of the resonant capacitors [89]. This led to the creation of an even wider input voltage regulation range, again with high efficiencies throughout. Furthermore, this concept is applicable in three-port conversion systems, with an example shown in [90]. Zhao et al. improved on this concept by integrating the function of the bidirectional switch into the rectifying devices, using a novel modulation mechanism [91, 92]. This way, the component count was decreased while achieving even higher efficiencies due to the reduced number of loss-generating components. The converter with the reduced number of devices may be seen in Figure 2.13, with the two active devices on the secondary side shorting the transformer to

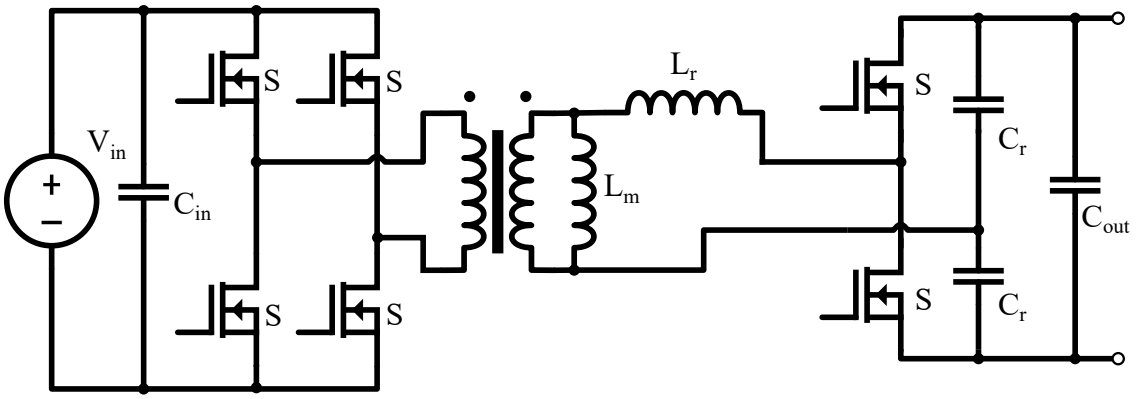


Figure 2.13: Converter proposed by Zhao et al.

create the boosting effect.

Another resonant conversion system, which is typically found in inductively-linked resonant power applications, might be of use in this application area. This is the class E^2 conversion system, which comprises the back-to-back combination of the class E inverter circuit with the class E rectifying circuit, as seen in Figure 2.14. This converter operates with two active switches, therefore allowing the potential high power density conversion in space-constrained applications like the one examined in this thesis. Plus, this conversion system has a very high theoretical efficiency, as it may achieve soft switching on both the inverter and rectification stage [93].

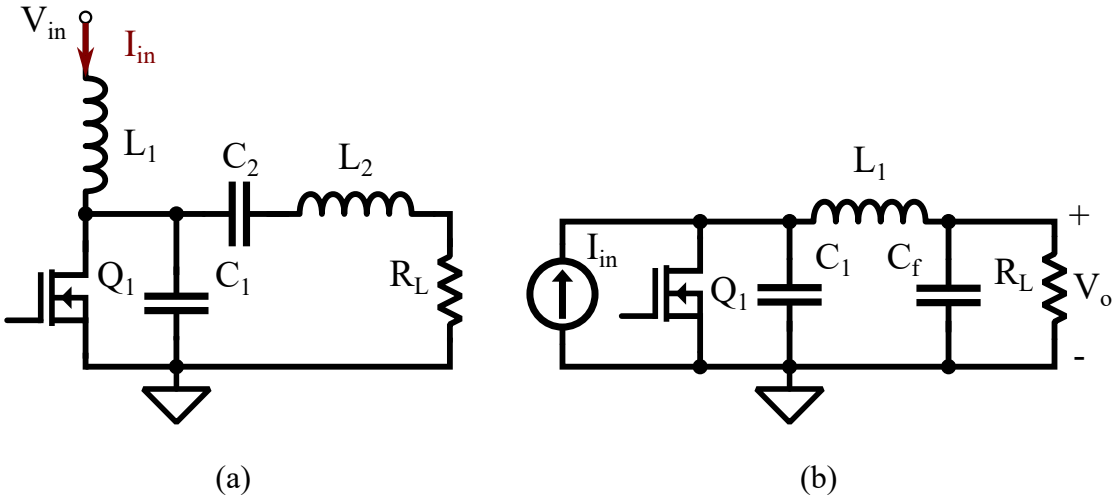


Figure 2.14: Class E converter comprised of a class E inverter (a), and a class E rectifier (b).

The manner in which class E^2 conversion systems operate is by having a DC input current at L_1 as seen in Figure 2.14(a), which is modulated using PWM at

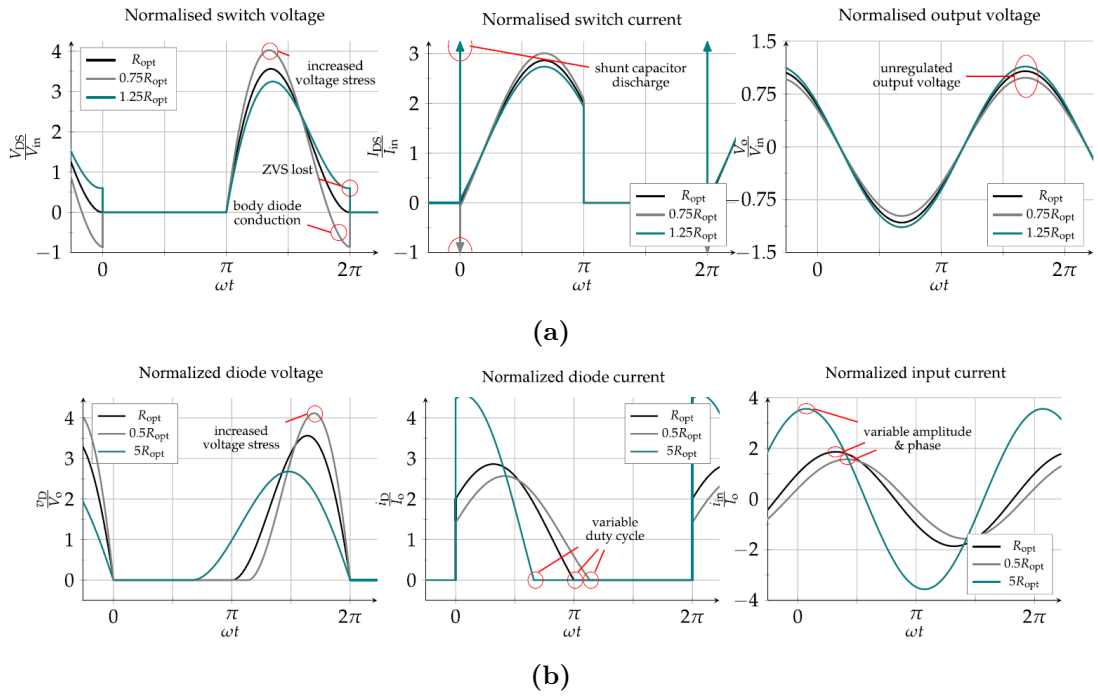


Figure 2.15: Characteristic waveforms of the class E inverter stage (a), and the class E rectifying stage (b) [94].

the resonant frequency of the LC network parameters. This results in the inverter outputting a sinusoidal AC voltage and current to the load, the frequency of which is the inverter's resonant frequency. The class E rectifier operates in the same way, but it takes the AC current input and translates it to DC voltage and current by modulating the active switch. The characteristic waveforms of the resonant inverter and rectifier can be seen in Figures 2.15a and 2.15b, respectively.

From these figures, one weakness of the class E converter can be seen, which is that there is a load dependence for the achievement of soft-switching. Plus, the V_{ds} on the active device is a multiple of the input voltage, thus requiring the use of higher voltage-rated devices. Nevertheless, this topology has seen wide acceptance in the inductive power transfer area due to the reduced driving losses it offers at high-frequencies, owed to the minimal use of active devices [95]. Also, with a careful design of the passive components, a load-independent soft-switching behaviour has been shown to be achievable in [94, 96]. Plus, high power levels are shown to be achievable by paralleling class E inverters in [97].

Nevertheless, to achieve high efficiencies over a wide load range combined with a

wide voltage input range, advanced modulation techniques such as the combination of pulse and frequency modulation [98], or ON-OFF control [94] would need to be implemented. This would increase the complexity of the magnetic and control design, so other solutions were pursued. Besides, to the author's knowledge, class E converters in the literature do not approach the extremely high-efficiency (98+%) levels seen by series and series-parallel resonant converters.

Thus, the idea of using a resonant converter with a boosting rectifier has been identified as a good idea for applications requiring wide input voltage regulations by other researchers [99]. Therefore, this thesis will attempt to exploit this modulation method by combining a resonant converter with a boost converter. The proposals by Labella and Zhao, while being very attractive, would require excessive duty cycles should the PV voltage be curtailed by partial shading, thus reducing their performance.

2.4 Summary

In this chapter, investigations were made into the benefits of Gallium Nitride devices. It has been found that they are good candidates for high-frequency power conversion for the voltage levels this thesis examines. This is due to their reduced die area for the same voltage ratings, which leads to smaller junction capacitances and much faster transition rates. Furthermore, the literature has been surveyed for conversion solutions when faced with a system that requires efficient wide input voltage regulation. It was found that while resonant converters offer the highest efficiency numbers, they are challenging to get them to work with a wide input-voltage regulation effectively. The concept of reconfigurable voltage multiplying rectifiers seems like an interesting solution, albeit at the cost of a higher semiconductor count. Similarly, integrating the function of the boost converter into a resonant conversion system has provided good results but would require excessive duty cycles if the input voltage is reduced considerably. Therefore, a new proposal should be made to address the issues being faced.

Chapter 3

Proposed Converter Topology

3.1 Introduction

While a variety of solutions are proposed in the literature for the examined problem, they suffer from some drawbacks. Converters based on the Flyback converter provide slightly lower efficiencies. Current-fed converters, while they do provide a broad voltage step-up ratio, suffer from hard-switching transitions, limiting the achievable efficiencies. In order to achieve soft-switching, solutions requiring additional circuitry are proposed, which add to the overall dimensions and the design complexity. Solutions with voltage multiplier cells require an increased number of semiconductor devices, taking up more PCB area and increasing the overall cost.

Existing duty-cycle modulated resonant solutions, like those from LaBella and Zhao, have shown promising results with overall high-efficiency power conversion. This helps harvest most of the solar energy and contributes to modest temperature increases while the converter is operating. However, they do not use Topology Morphing Control in conjunction with their duty-cycle control. This would allow for an extension of their applicability to partially shaded conditions, which would normally require a high duty cycle, lowering their power conversion efficiency.

At the same time, it would be ideal to limit the number of semiconductor devices, mostly because of the increased cost but also the aspect of long-term reliability. Therefore, the converter in Figure 3.1 is proposed. It is based on a simple Series

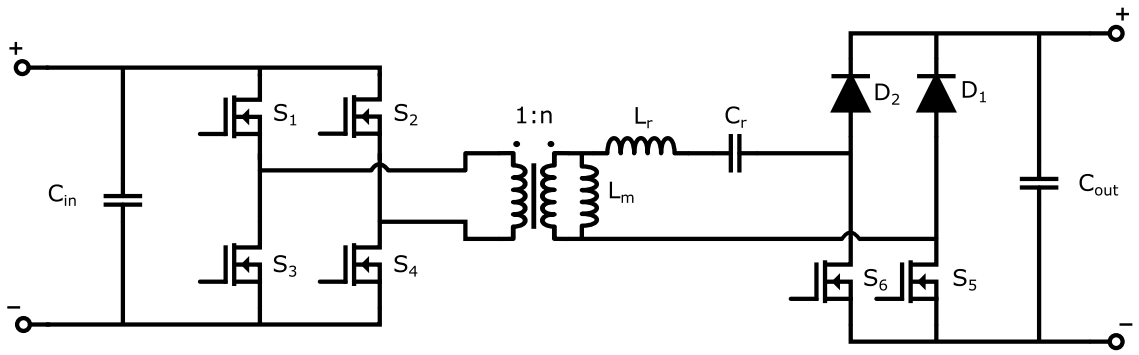


Figure 3.1: The proposed topology.

Resonant Converter (SRC), with the inclusion of active bottom switches on the rectifying bridge. The converter has three different operation modes, depending on the input voltage.

1. **DC Transformer (DCX) Mode** - At the nominal design voltage, the converter operates as a series resonant converter, thus operating at the optimum efficiency.

2. **Voltage Boosting Mode** - The devices S_5, S_6 have their PWM duty cycle extended. This turns the resonant inductance into an equivalent boost inductor, operating at a switching frequency double the PWM switch frequency.

3. **Greinacher Boosting Mode** - The device S_5 is left constantly ON. The circuit is now morphed into a single-stage Greinacher circuit. This creates a voltage bias on C_r, which helps step up the voltage for the required V_{in}.

3.2 Converter Operation Modes

As mentioned before, there are three distinct operation modes in the proposed converter. These will be analysed in detail in this section. The analysis will be conducted using state-plane modelling of the resonant tank, as this allows for an elegant extraction of the operating variables (voltage, current) in the LC resonant tank without the need for advanced mathematical operations. Instead, retrieving the resonant tank waveforms is a matter of geometry, with different topological changes modelled as arcs or lines in the state-plane diagram. The basis behind applying this method is that each topological state in a resonant circuit can be modelled as a circular movement in the state plane, with the centre being the DC solution of the circuit and a radius of the total AC+DC voltage, moving at an angular velocity shown in (3.4). To the author's knowledge, this was first introduced in [100] to analyse the operation of a series resonant converter and was then extended by Oruganti et al. [101] to present the Optimal Trajectory Control of the LLC converter. In this work, it will be used to derive the analytical equations of $i_{Lr}(t)$ and $v_{Cr}(t)$, as well as the converter's step-up ratio.

3.2.1 State-Plane Analysis

The basis of the state-plane analysis, when looking into a series resonant converter, is that each topological state normally comprises the LC resonant tank, excited by some value of "averaged" DC voltage, which can be named V_{in}. The DC current will be considered as zero. However, this technique easily extends to the LLC family of converters by considering an additional current source of the magnetising current. In the series LC arrangement, by performing Kirchhoff's laws, two equations may be acquired:

$$L_r \frac{di_{Lr}(t)}{dt} = V_{in} - v_{cr}(t) \tag{3.1}$$

$$C_r \frac{dv_{cr}(t)}{dt} = i_{Lr} \tag{3.2}$$

Considering that the resonant capacitor has a zero average value, its voltage fluctuates according to the voltage swing Δv_{cr}. To aid in this analysis, the resonant tank's impedance and angular frequency are defined in (3.3), (3.4). Additionally, the angular displacement of the resonant tank is calculated as (3.5).

$$Z_r = \sqrt{\frac{L_r}{C_r}} \tag{3.3}$$

$$\omega_r = \frac{1}{\sqrt{L_r C_r}} \tag{3.4}$$

$$\theta = \omega_r \cdot t \tag{3.5}$$

Using (3.3), (3.4), it is possible to rewrite the resonant tank equations as:

$$\frac{Z_r}{\omega_r} \cdot \frac{di_{Lr}(t)}{dt} = V_{in} - v_{cr}(t) \tag{3.6}$$

$$\frac{1}{Z_r \omega_r} \cdot \frac{dv_{cr}(t)}{dt} = i_{Lr} \tag{3.7}$$

Using the Laplace transform, it is possible to solve the system of equations above easily. For added clarity to the reader, the equations in the frequency domain are:

$$\frac{Z_r}{\omega_r} \cdot sI_{Lr}(s) = \frac{V_{in} - sV_{cr}(s)}{s} \tag{3.8}$$

$$\frac{1}{Z_r \omega_r} \cdot (sV_{cr}(s) - \Delta v_{cr}) = I_{Lr}(s) \tag{3.9}$$

By performing the inverse Laplace transform, the time-domain equations, which

are the generalised solution for this system, become:

$$v_{cr}(t) = V_{in} - (V_{in} - \Delta v_{cr}) \cos \omega_r t \tag{3.10}$$

$$i_{Lr}(t) = \frac{V_{in} - \Delta v_{cr}}{Z_r} \cdot \sin \omega_r t \tag{3.11}$$

The resonant tank current may be multiplied by the resonant tank impedance so that it possesses the unit of Volts. Using this substitution, it may be seen that the equations (3.10) and (3.11) define a circle, with a radius of $V_{in} - \Delta v_{cr}$. Analytically, this means that the following holds true:

$$(v_{cr} - V_{in})^2 + (i_{Lr})^2 = (V_{in} - \Delta v_{cr})^2 \tag{3.12}$$

All in all, this justifies that the values of $v_{cr}(t), Z_r i_{Lr}$ will be forming circles in their state-plane diagram, with centres defined by the DC voltages applied, and radii defined by the DC+AC response. Naturally, some simplifications must be made to aid in conducting the analysis when implementing this strategy on the examined conversion system.

- The output capacitor C_{out} is large enough to allow the consideration of the output voltage (V_o) as fixed. Similarly, the input capacitor C_{in} is large enough to consider the input voltage (V_{in}) to be fixed.
- The output capacitor is much larger than the resonant capacitor ($C_{out} \gg C_r$), so there isn't an influence on the operational dynamics.
- The stored energy, in the form of junction and output capacitance (C_j, C_{oss}), is modelled as a constant capacitor, and non-linearity is ignored.
- Similarly, the ringing associated with parasitic capacitances during DCM periods will not be considered.
- Third-quadrant conduction of the GaN HEMTs will be modelled as a diode, as it has similar electrical characteristics, even though there isn't a physical pn junction inside the devices.

The converter is run at a frequency only slightly lower than the LC tank resonant frequency. This is done so that the converter transfers power from the input source to the output in the maximum percentage of time possible. The switching frequency is not the same as the LC tank's resonance frequency to allow the use of dead-time periods without losing ZCS. The converter will be modelled with an ideal transformer. However, the magnetising inductance L_m has been added to allow for the later derivation of the zero-voltage transitions. The magnetising inductance is modelled on the HV side, as it is anticipated that since it has a higher inductance value on this side, it will eventually be more accurate to verify its value in experimental work.

3.2.2 DCX Mode

During the DC transformer mode (DCX), the converter operates as a pure series-resonant converter (SRC). The converter's voltage transfer ratio is close to 1, as $f_{sw} \approx f_r$ [63]. In this application, as the utilised transformer has a built-in step-up ratio based on its turn ratio (n), this translates to the relationship of output and input voltage, as seen in (3.13).

$$M = \frac{V_o}{nV_{in}} = 1 \Leftrightarrow V_o = nV_{in} \tag{3.13}$$

The different topological states of the converter may be seen in Figure 3.2, and the operational waveforms in Figure 3.3. The converter may be broken down into its topological states to assist in deriving the operational waveforms.

Topological state 1 $(t_0 - t_1)$: During this state, S_1, S_4 are turned on, thereby exciting the transformer with $+V_{in}$. This causes the LC tank to resonate. Initially, the resonant tank doesn't conduct current, and the resonant capacitor is at its lowest voltage point; these conditions are seen in (3.14), (3.15). The initial conditions have been marked as point A in the state-plane trajectory, shown in Figure 3.5.

$$i_{Lr}(t_0) = 0 \tag{3.14}$$

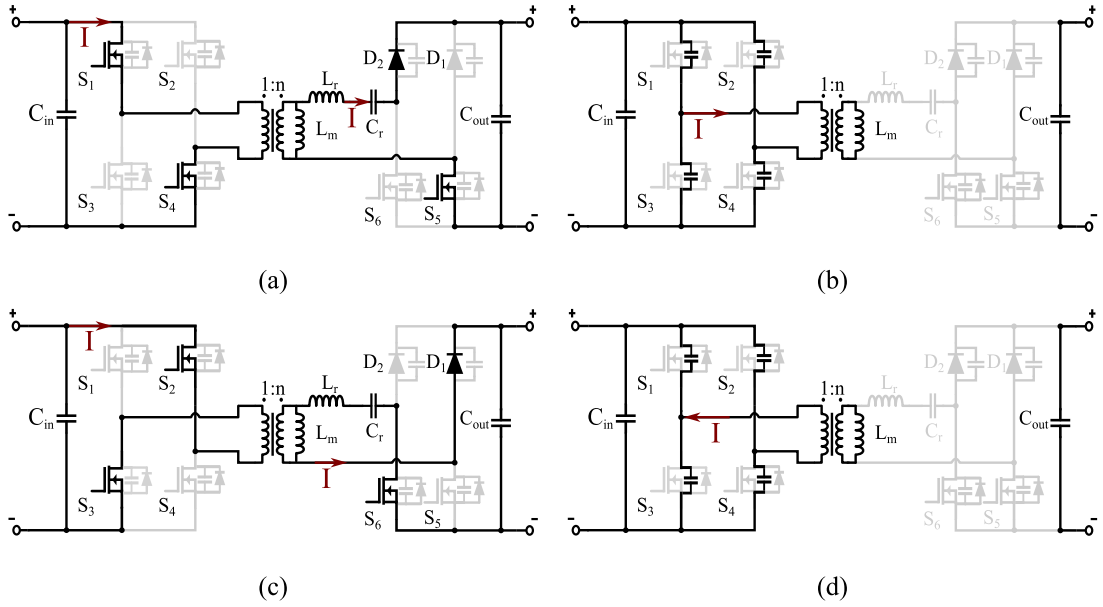


Figure 3.2: The four topological states of the DCX operation, in sequential order from (a) to (d).

$$v_{Cr}(t_0) = -\Delta v_{Cr} \tag{3.15}$$

The resonant capacitor's voltage swing Δv_{Cr} can be found, considering that all output power has to pass through this component.

$$\Delta v_{Cr} = \frac{P_o T_{sw}}{4 n V_{in} C_r} \tag{3.16}$$

Based on the equivalent circuit during this state, shown in Figure 3.4(a), the resonant tank's trajectory may be described by a circle, with a centre of $O_1 : (0, 0)$, and a radius $R_1 = \Delta v_{Cr}$. The state-plane trajectory path is from point A to point B with the orientation of travel shown by the markers in Figure 3.5. This orientation happens as the circuit is excited with a positive AC voltage, so the current will have to increase initially, i.e. follow the path from the upper half-plane on the x-axis.

The state equations may be calculated as follows:

$$v_{Cr}(t) = R_1 \cdot cos(\pi - \omega_r(t - t_0)) = -R_1 \cdot cos(\omega_r(t - t_0)) \tag{3.17}$$

$$i_{Lr}(t) = \frac{R_1}{Z_r} \cdot sin(\pi - \omega_r(t - t_0)) = \frac{R_1}{Z_r} \cdot sin(\omega_r(t - t_0)) \tag{3.18}$$

The magnetising current is linearly increasing from its minimum point, and

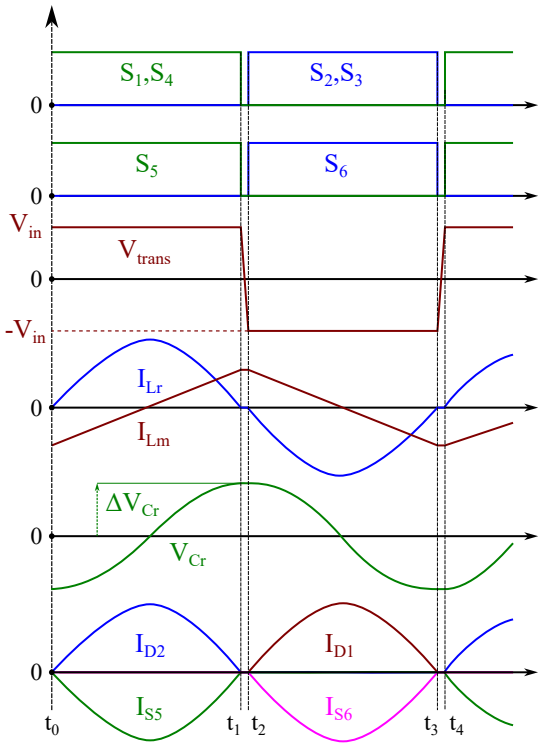


Figure 3.3: The operational waveforms of the converter in the DCX mode.

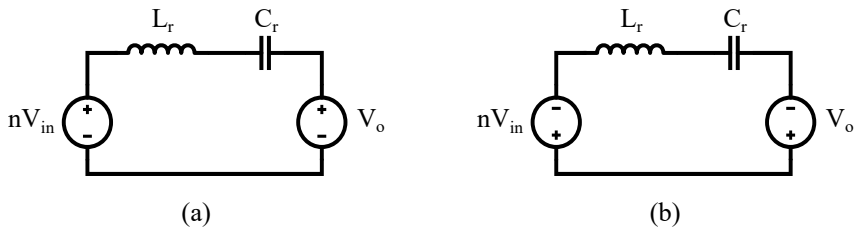


Figure 3.4: Equivalent circuits during the topological state 1 (a) and state 3 (b).

power is transferred to the output via the D_2, S_5 conduction path. Concerning the magnetising current flowing through the magnetising inductance, it may be approximated as linearly increasing since nV_{in} is applied at its terminals. With this knowledge and the initial condition shown in (3.19), the analytical equation for the magnetising current is expressed in (3.20).

$$I_m(t_0) = -\frac{nV_{in}}{4f_{sw}L_m} \tag{3.19}$$

$$I_m(t) = \frac{nV_{in}}{L_m}(t - t_0) + I_m(t_0) \tag{3.20}$$

The converter eventually will reach point B in the state-plane diagram at the time instant t_1. As the switching frequency is set according to the LC resonant

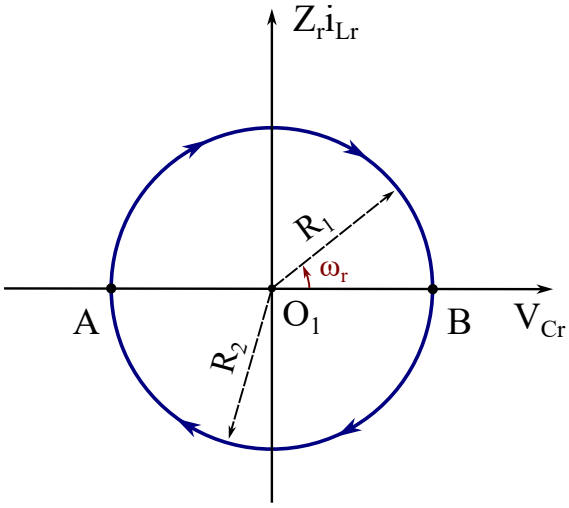


Figure 3.5: State-plane trajectory during DCX mode.

frequency, the devices S_1, S_4, S_5 will turn off at the same time. In terms of switching loss, the devices S_5, D_2 will have ZCS, as the resonant tank current will be zero at this time. However, the devices S_1, S_4 will be conducting the magnetising current during their turn-off instant. As there is no load current during this time, they can be considered to achieve partial ZCS since the magnetising current is typically smaller than the load current.

Topological state 2 $(t_1 - t_2)$: During this state, all the active devices are in their off state. Power is not being transferred from the input to the output terminals. Hence, the current in the resonant inductor and the voltage of the resonant capacitor are considered constant. The transformer has its maximum magnetising current at this time, which is approximated to be constant, considering that this time period is short. The magnetising current at this time is:

$$I_{Lm} = \frac{nV_{in}}{4f_{sw}L_m} \tag{3.21}$$

This current will be flowing through the devices S_{1-4}, charging $S_{1,4}$ and discharging $S_{2,3}$. With enough time in this period, $S_{2,3}$ will be fully discharged, leading to their ZVS turn-on. Considering the magnetising current as a constant current source and all parasitic capacitances as a fixed value, the voltages of $S_{2,3}$ will decay linearly until they reach zero. The slope of this linear decay will depend on the value of the

capacitance seen at the transformer's terminals and the value of the magnetising current. The mechanism behind ZVS creation will be analysed in detail in a later section; however, going forward, it will be assumed that the dead time is long enough to allow ZVS turn on.

Topological state 3 (t_2−t_3) : In the beginning of this state, S_2, S_3, S_6 are turned on. The transformer's input terminals are excited with $-V_{in}$, and the magnetising inductance with $-nV_{in}$. This state can be modelled as the circuit in Figure 3.4(b). This circuit corresponds to a circle in the state-plane of $O_1 : (0, 0)$ and a radius $R_2 = \Delta v_{Cr}$. The initial point in the state-plane trajectory is B, and it corresponds to the resonant tank's initial conditions (3.22), (3.23).

$$i_{Lr}(t_2) = 0 \tag{3.22}$$

$$v_{Cr}(t_2) = \Delta v_{Cr} \tag{3.23}$$

The trajectory path of the state plane is moving towards point A, in the direction indicated by the markers of Figure 3.5. The analytical tank equations may be formulated as (3.24), (3.25) for this time period.

$$i_{Lr}(t) = \frac{R_2}{Z_r} \sin\left(-\omega_r(t - t_2)\right) = -\frac{R_2}{Z_r} \sin\left(\omega_r(t - t_2)\right) \tag{3.24}$$

$$v_{Cr}(t) = R_2 \cos\left(-\omega_r(t - t_2)\right) = R_2 \cos\left(\omega_r(t - t_2)\right) \tag{3.25}$$

The magnetising current decays linearly due to the applied voltage excitation, and the expression for this current is:

$$I_m(t) = \frac{nV_{in}}{4f_{sw}L_m} - \frac{nV_{in}}{L_m}(t - t_2) \tag{3.26}$$

Topological state 4 ($t_3 - t_4$) : The load current flowing through the resonant tank has decayed to zero, and S_2, S_3, S_6 are turned off. Devices $S_{2,3}$ are turned off with low current, while S_6 has ZCS.

During this time, the magnetising current will charge the output capacitance of

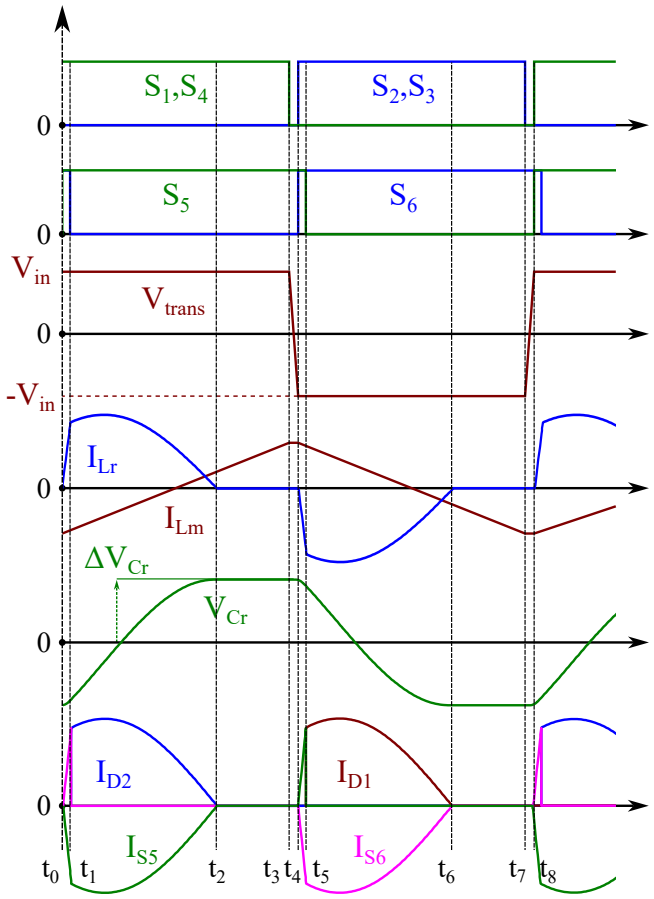


Figure 3.6: The operational waveforms of the converter in the Boosting mode.

$S_{2,3}$ and discharge that of $S_{1,4}$. The value of the magnetising current during this time is:

$$I_{Lm} = -\frac{nV_{in}}{4f_{sw}L_m} \tag{3.27}$$

The timing of this period will be selected to achieve ZVS on the active devices. Meanwhile, the resonant tank state parameters stay constant, as no power is transferred. Hence, the state-plane trajectory stays at point A.

3.2.3 Voltage Boosting Mode

The converter provides a voltage step-up function during this mode, so the following holds true.

$$M = \frac{V_o}{nV_{in}} > 1 \Leftrightarrow V_o > nV_{in} \tag{3.28}$$

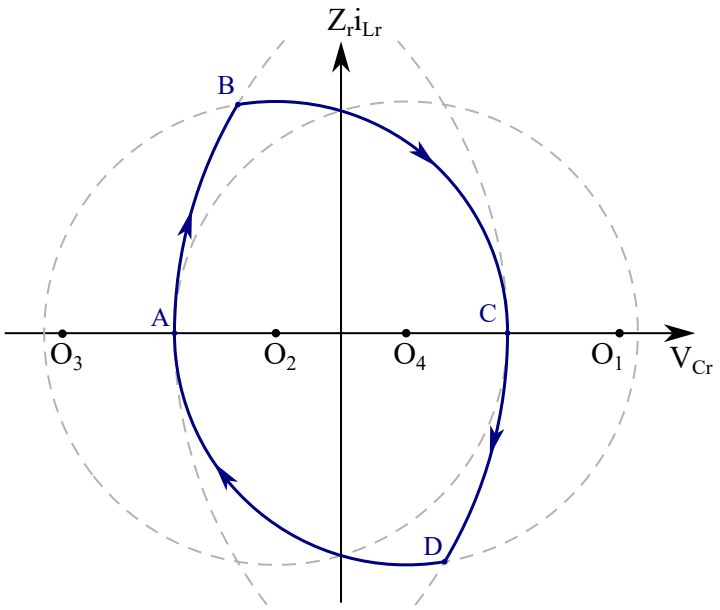


Figure 3.7: Resonant tank state-plane trajectory during Boosting Operation.

There are four distinct topological states for each of the half-periods. First, the resonant inductor gets charged from the input voltage source, as shown in Figure 3.8(a). Afterwards, the stored energy is transferred to the output (Figure 3.8(b)). Eventually, the resonant tank current decays to zero, so power stops being transferred to the output as shown in Figures 3.8(c),(d).

The idealised operating waveforms can be seen in Figure 3.6. In this figure, timestamps have been placed at the transition points of the converter to aid the analysis. The state-plane trajectory of the resonant tank during a period can be seen in Figure 3.7. This will be used to extract the analytical equations of the resonant tank during operation.

Topological state 1 $(t_0 - t_1)$: During this state, the devices S_1, S_4, S_5, S_6 are in their on state. The primary of the transformer gets excited with V_{in}, and the secondary of the transformer will be at nearly zero voltage, as it is short-circuited by the conduction path formed by S_5, S_6 and the resonant tank. Prior to the beginning of this period, the resonant inductor current is zero, and the resonant capacitor's voltage is at its minimum value, as seen in Figure 3.6. This time period is similar to a typical PWM boost converter, hence the name given to this mode. One may imagine a typical boost converter, with nV_{in} input voltage, operating at double the

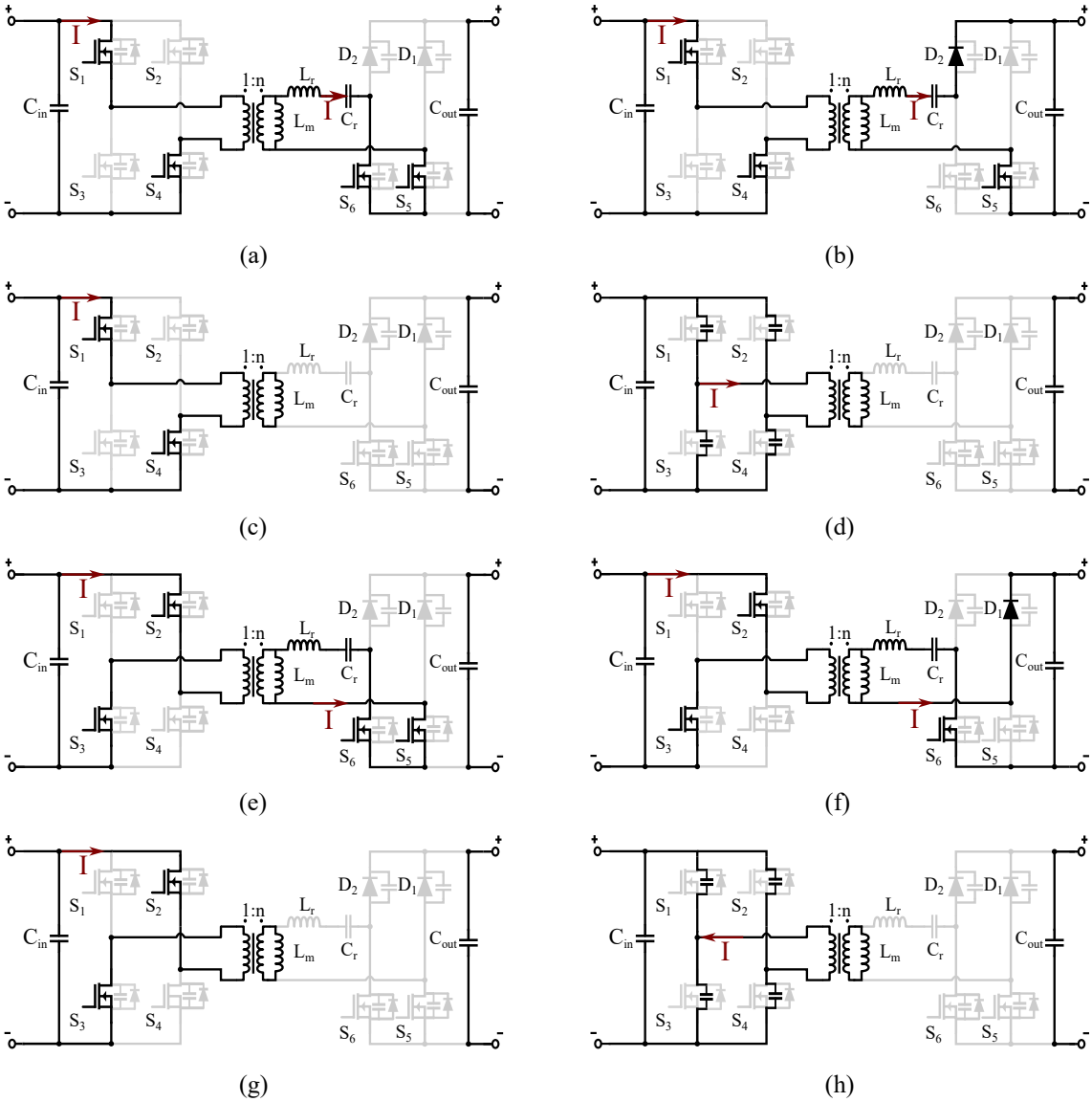


Figure 3.8: Topological states of the Boosting operation, in sequential order from (a) to (h).

switching frequency, and the current through the inductor would be similar to the one derived here.

State plane analysis is used to retrieve the analytical equations of the resonant tank. The equivalent circuit during this time period, as well as the state-plane trajectory path, is shown in Figure 3.9. From the equivalent circuit, it is seen that the trajectory path will be defined by a circle with $O_1 : (nV_{in}, 0)$ and a radius $R_1 = nV_{in} + \Delta v_{Cr}$. The resonant tank's analytical equations may be written as:

$$i_{Lr}(t) = \frac{R_1}{Z_r} \sin(\pi - \omega_r(t - t_0)) \tag{3.29}$$

$$v_{Cr}(t) = nV_{in} + R_1 \cos(\pi - \omega_r(t - t_0)) \tag{3.30}$$

Concerning the magnetising current, which in this analysis is flowing through L_m, it is initially at its lowest point; however, at t_0, it gets excited with a positive voltage, so it will begin increasing linearly. The analytical equations can be easily found as (3.31), (3.32).

$$i_{Lm}(t_0) = -\frac{nV_{in}}{4f_{sw}L_m} \tag{3.31}$$

$$i_{Lm}(t) = i_{Lm}(t_0) + \frac{nV_{in}}{L_m} \cdot (t - t_0) \tag{3.32}$$

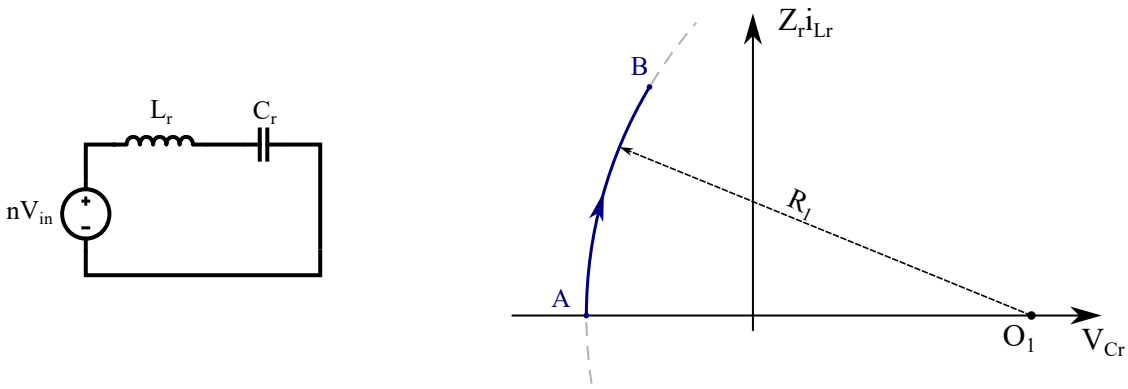


Figure 3.9: Equivalent Circuit during state 1 (left), and state plane trajectory (right).

Topological state 2 $(t_1 - t_2)$: At the time instant t_1, the device S_6 turns off, which in turn forward biases the diode D_2 into conduction. Power is now transferred to the output capacitor in a series resonant fashion. The initial current of the resonant inductor during this time will be found with the use of the angle δ, shown in Figure 3.10, using simple trigonometry. The equivalent circuit is seen in the same image, which can be defined by a circle with $O_2 : (nV_{in} - V_o)$ and a radius of $R_2 = V_o - nV_{in} + \Delta v_{Cr}$. Since the converter is boosting the input voltage, it is evident that O_2 belongs to the negative half of the x-axis.

The resonant tank moves along the trajectory path from point B to point C in the circle previously defined. With the definition of angle δ, the analytical resonant tank equations can be formulated as:

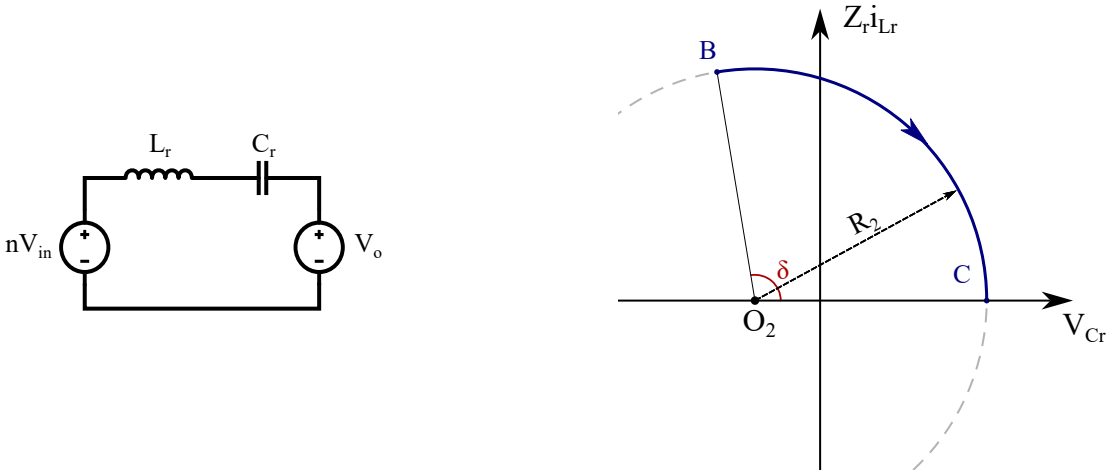


Figure 3.10: Equivalent circuit during state 2 (left), and state-plane trajectory (right).

$$i_{Lr}(t) = \frac{R_2}{Z_r}\sin(\delta - \omega_r(t - t_1)) \tag{3.33}$$

$$v_{Cr}(t) = (nV_{in} - V_o) + R_2\cos(\delta - \omega_r(t - t_1)) \tag{3.34}$$

The initial angle δ may be found as:

$$\delta = \begin{cases} \pi - \sin^{-1}(\frac{Z_r i_{Lr}(t_1)}{R_2}), & O_{2x} > v_{Cr}(t_1) \\ \sin^{-1}(\frac{Z_r i_{Lr}(t_1)}{R_2}), & O_{2x} \leq v_{Cr}(t_1) \end{cases} \tag{3.35}$$

At this state, the transformer input continues to get a positive voltage excitation of V_{in}, so the magnetising current is linearly increasing according to (3.32).

Topological state 3 $(t_2 - t_3)$: The resonant tank current has reached zero at t_2. Since there is no conductive path for the tank current to oscillate to negative values, the current remains zero during this period. Power doesn't flow towards the output, so the resonant capacitor voltage is constant at Δv_{Cr}. The magnetising current keeps its linear increase, according to (3.32). At the end of this period, the devices S_1, S_4 will turn-off at t_3 with the magnetising current as calculated in (3.36).

$$n \cdot I_m(t_3) = n \cdot \frac{nV_{in}}{4f_{sw}L_m} \tag{3.36}$$

Topological state 4 $(t_3 - t_4)$: While the devices $S_{1,4}$ have been turned off at t_3, the magnetising current continues to flow. The magnetising current will be

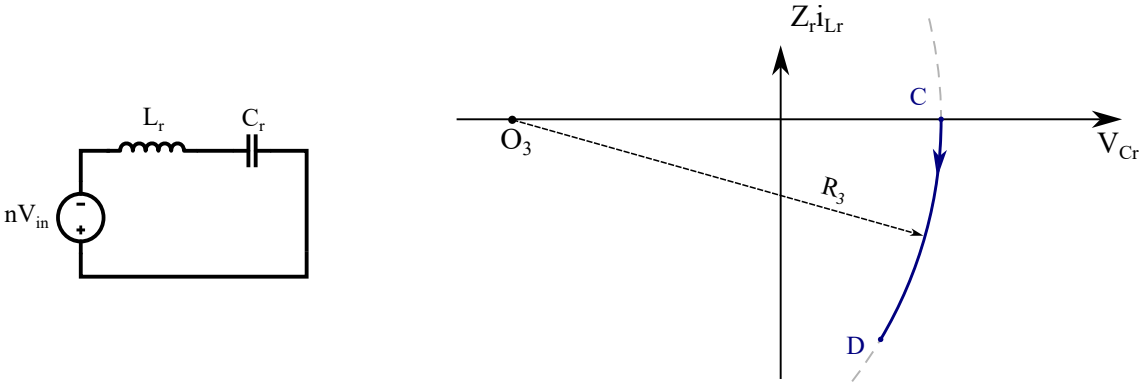


Figure 3.11: Equivalent circuit during state 5 (left), and corresponding state-plane trajectory (right).

discharging the equivalent output capacitances of $S_{2,3}$ while charging that of $S_{1,4}$. Eventually, with enough time, the capacitances of $S_{2,3}$ will be fully discharged, and they will be conducting via their "body diode". Once this has occurred, the transformer's input voltage will have successfully changed sign from V_{in} to $-V_{in}$, and $S_{2,3}$ can be turned on with ZVS.

Topological state 5 ($t_4 - t_5$) : At this state, devices $S_{2,3}$ turn on at t_4. The transformer is getting excited on the primary side with $-V_{in}$, while on the secondary side, it is short-circuited by the conductive path formed by $S_{5,6}$ and the resonant tank. Similarly to before, this state can be shown in the state-plane trajectory as the path that connects point C with point D. The path and the equivalent circuit model are shown in Figure 3.11. It is seen from the equivalent circuit that the trajectory path is defined by a circle with $O_3 : (-nV_{in}, 0)$ and a radius of $R_3 = nV_{in} + \Delta v_{Cr}$. The resonant tank's analytical equations for this time period can be written as:

$$i_{Lr}(t) = \frac{R_3}{Z_r} \sin(-\omega_r(t - t_4)) \tag{3.37}$$

$$v_{Cr}(t) = -nV_{in} + R_3 \cos(-\omega_r(t - t_4)) \tag{3.38}$$

Starting at t_4, with the transformer being excited with a negative voltage, the magnetising current will start decreasing from its positive peak value linearly, with

its value expressed in (3.39).

$$I_m(t) = I_m(t_3) - \frac{nV_{in}}{L_m} \cdot (t - t_4) \tag{3.39}$$

Topological state 6 ($t_5 - t_6$) : At the beginning of this state, the device S_5 gets turned off with the current $i_{Lr}(t_5)$. The turn-off of this switch will forward bias the diode D_1, which will form a conductive path to the output side. To find the analytical equations of the resonant tank's current and voltage, their initial value must be computed. As the modulation of the converter is symmetric, the angle δ found in the analysis of state 2 may be reused. Therefore, the analytical tank equations can be formulated based on this fact, and the equivalent circuit is shown in Figure 3.12.

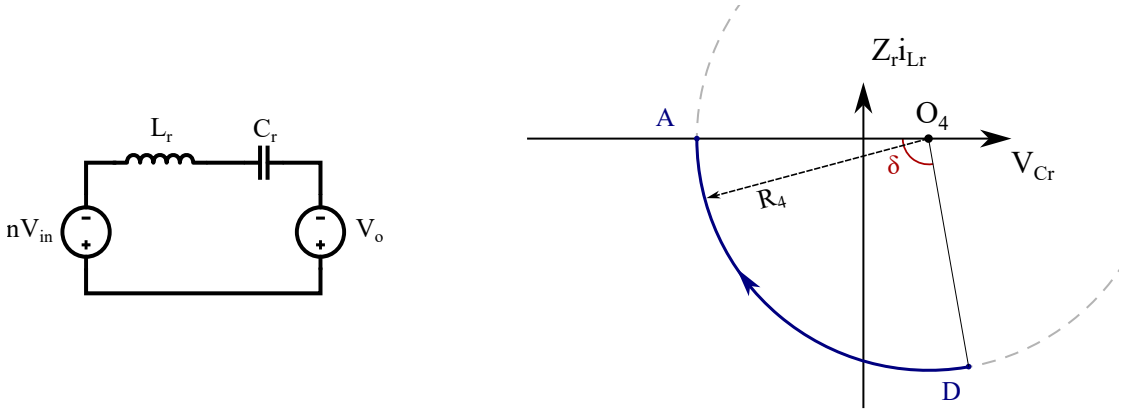


Figure 3.12: Equivalent circuit during state 6 (left), and corresponding state-plane trajectory (right).

The circuit's state-plane trajectory is defined by a circle with $O_4 : (V_o - nV_{in}, 0)$ and a radius of $R_4 = V_o - nV_{in} + \Delta v_{Cr}$. The state variables are moving from point D to point A and may be expressed in their time format as:

$$i_{Lr}(t) = \frac{R_4}{Z_r} \sin(\delta - \pi - \omega_r(t - t_5)) \tag{3.40}$$

$$v_{Cr}(t) = V_o - nV_{in} + R_4 \cos(\delta - \pi - \omega_r(t - t_5)) \tag{3.41}$$

At this time period, the transformer is still getting excited by $-V_{in}$, so the magnetising current is still expressed by the formula in (3.39). This period will

continue until the resonant tank reaches zero current at t_6.

Topological state 7 ($t_6 - t_7$) : At the beginning of this period, the resonant tank current has reached zero. Furthermore, since there isn't a conductive path to the output, the resonant tank current remains at zero. This also means that the resonant capacitor's voltage remains constant at $-\Delta v_{Cr}$ as no power is transferred through it. At the end of this period, the devices S_2, S_3 will turn off at t_7 with the peak magnetising current, as found in (3.31).

Topological state 8 ($t_7 - t_8$) : With all the devices in the primary bridge switched off, the magnetising current continues to freewheel in the primary side of the converter. The magnetising current will be discharging the equivalent output capacitances of $S_{1,4}$ while charging those of $S_{2,3}$. If enough dead time is selected, eventually, the devices $S_{1,4}$ will experience third-quadrant conduction via their "body diode". At this point, the transformer input voltage will have fully changed from $-V_{in}$ to V_{in}, and $S_{1,4}$ can be turned on with ZVS. After this period, the converter has finished an operating period, and the states described here are repeated.

3.2.4 Voltage Boosting Conversion Ratio

While the operation of the converter has been thoroughly analysed in the previous section, the efficacy of the converter in boosting the input voltage to the required output voltage remains to be found. The relation between the duty cycle and the step-up ratio is integral to the converter's performance, as lower duty cycles are typically associated with lower RMS currents, switching losses and overall higher efficiencies. State-plane diagrams will be utilised to find this relation.

First, the duty cycle must be defined. In this operation, it is defined as the time period $t_1 - t_0$, as during this time, the converter operates in a boost converter manner, as shown in Figure 3.6. Therefore, the duty cycle may be defined as in (3.42).

$$t_1 - t_0 = t_b = d_b T_{sw} \Leftrightarrow d_b = \frac{t_b}{T_{sw}} \tag{3.42}$$

After defining the duty cycle for this operation, it remains to find its relation

with the input voltage. The method used in this work is by solving for the state-plane trajectories. It can be seen upon inspection that the origins and radii of the state-plane trajectories are influenced by the input voltage, as well as the output power. The influence of the output power is seen indirectly via the resonant capacitor's voltage swing. The two different circles in the topological states 1 and 2, shown in Figures 3.9 and 3.10, intersect at point B. This will give a system of two equations for the two state variables at the intersection point. The circles may be expressed algebraically as in (3.43), (3.44).

$$(v_{Cr} - nV_{in})^2 + (Z_r i_{Lr})^2 = R_1^2 \tag{3.43}$$

$$(v_{Cr} - nV_{in} + V_o)^2 + (Z_r i_{Lr})^2 = R_2^2 \tag{3.44}$$

Solving these equations for the intersection point, the expressions for the boosting time period and the normalised voltage gain may be derived. It is shown in (3.45) that the required boosting time period, t_b, is dependent on the output power and the resonant tank parameters. The dependencies formed in (3.46) can be seen graphically in Figures 3.13, 3.14.

$$t_b = \frac{1}{\omega_r} \cdot \cos^{-1}\left(\frac{4V_o^2 C_r + P_o T_{sw} M(2-M)}{4V_o^2 C_r + M^2 P_o T_{sw}}\right) \tag{3.45}$$

$$M(d_b) = \frac{P_o T_{sw} + \sqrt{(P_o T_{sw})^2 + 4P_o T_{sw} V_o^2 C_r (1 - \cos^2(\omega_r d_b T_{sw}))}}{P_o T_{sw}(\cos(\omega_r d_b T_{sw}) + 1)} \tag{3.46}$$

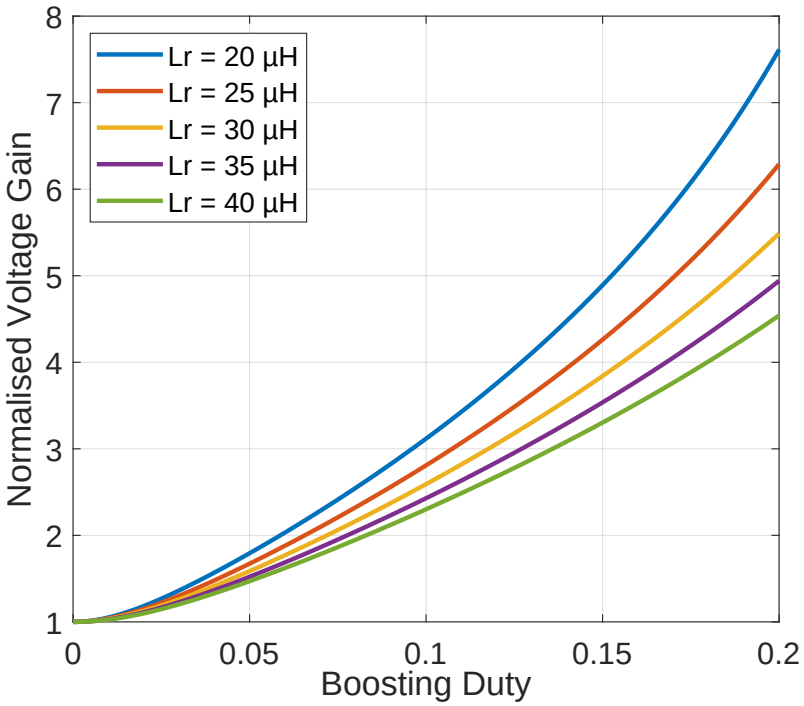


Figure 3.13: Converter voltage step-up, with a constant resonant frequency but with variable L_r.

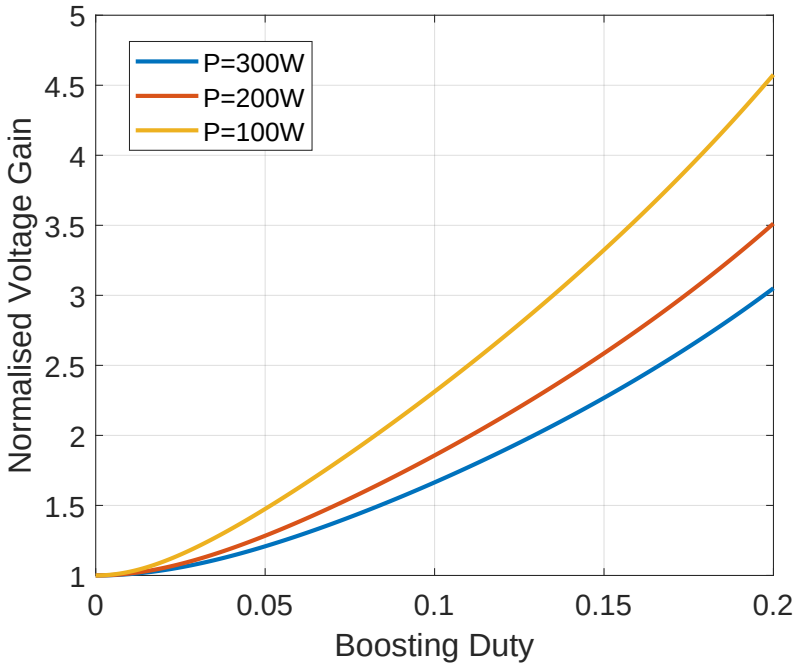


Figure 3.14: Converter voltage step-up, with all parameters staying constant apart from the output power.

3.2.5 Greinacher Boosting Mode

In this mode, the converter provides voltage step-up synergistically in two different ways. The first way is by extending the duty cycle of a secondary-side active device in order to short-circuit the resonant inductor in a manner similar to a boost converter. The second way is by biasing the resonant capacitor with a DC voltage (written as $\bar{V}_{Cr}$), and this is achieved by keeping one of the secondary-side devices constantly in its on state. Upon closer inspection of the circuit, it can be seen that by this modification, the resulting circuit is almost the same as the circuit used by Heinrich Greinacher [102] to double an input AC voltage. Based on the two methods used to step up the voltage, the author decided to name this mode "Greinacher Boosting Mode".

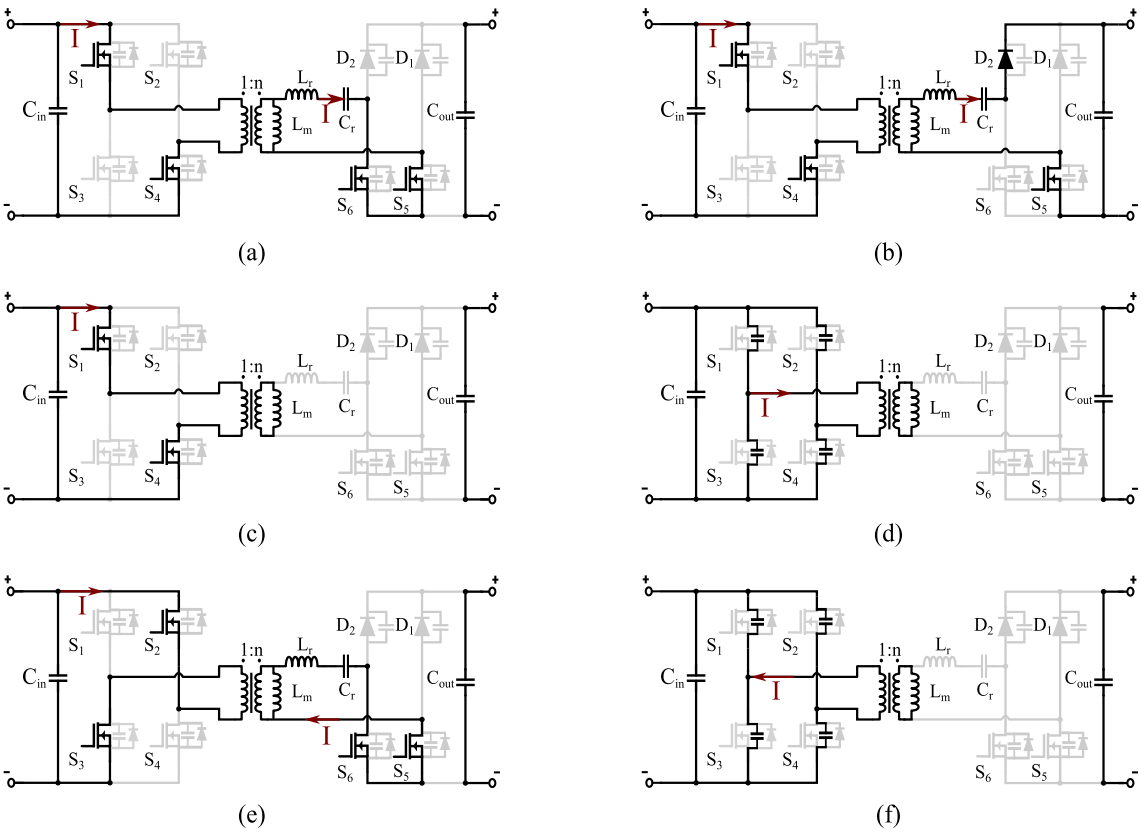


Figure 3.15: Topological states of the Greinacher Boosting operation, in sequential order from (a) to (f).

There are six distinct topological states, which can be seen in Figure 3.15. The paths in which current is passing are shown with black lines, whilst the paths with zero current are greyed out. The idealised operating waveforms may also be seen

in Figure 3.16, and the complete state-plane trajectory of the converter is seen in Figure 3.17. It should be noted that the state-plane analysis here deals with the AC voltage of the resonant capacitor, and therefore in the analytical equations $\bar{V}_{Cr}$ will be added to the capacitor's voltage. The converter's operation in these topological states will be analysed in the following discussion, and the analytical formulae will be derived for the resonant tank's state parameters.

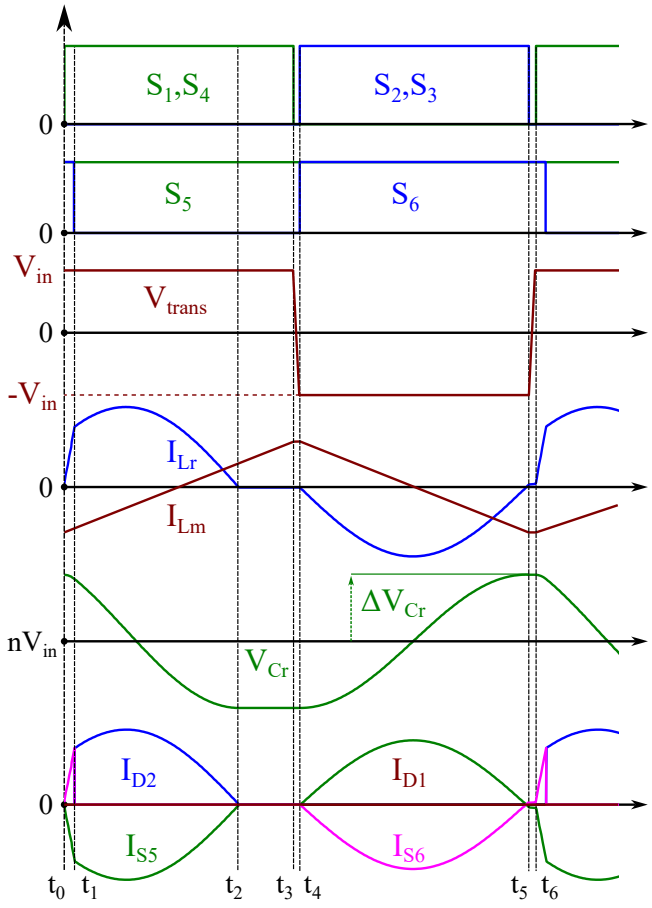


Figure 3.16: The idealised operational waveforms of the converter in the Greinacher Boosting mode.

Topological state 1 $(t_0 - t_1)$ **:** Prior to the beginning of this period, the resonant inductor current was zero, and the resonant capacitor's voltage was at its maximum point. At t_0, devices S_1, S_4 are turned on, and therefore the transformer is getting excited with V_{in}. At the secondary side, devices S_5, S_6 are also turned on, effectively short-circuiting the transformer's secondary side along with the resonant tank.

To find the analytical equations at the resonant tank, the equivalent circuit

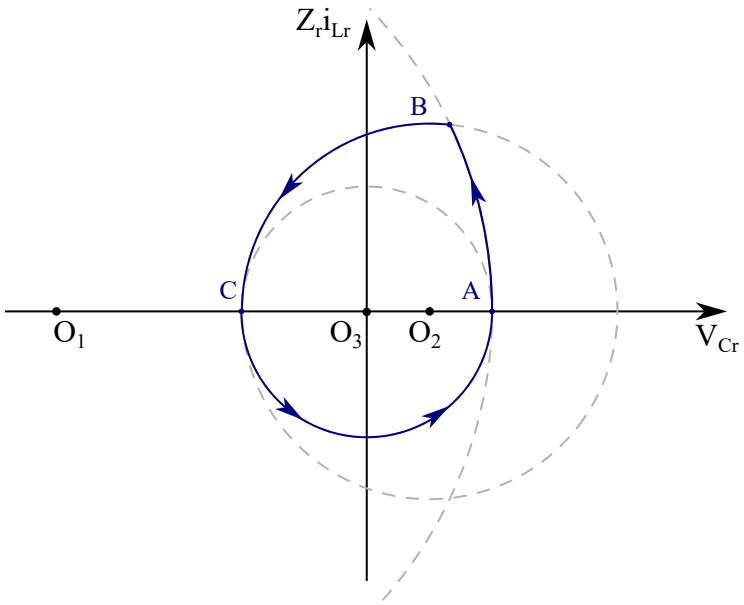


Figure 3.17: Resonant tank state-plane trajectory during Greinacher Boosting operation.

during this state may be found in Figure 3.18. From the equivalent circuit, it can be deduced that the state-plane trajectory path will be defined by a circle with $O_1 : (-nV_{in} - \bar{V}_{Cr}, 0)$ and a radius of $R_1 = nV_{in} + \bar{V}_{Cr} + \Delta v_{Cr}$. Based on this, the following holds true during this state:

$$i_{Lr}(t) = \frac{R_1}{Z_r} \cdot \sin(\omega_r(t - t_0)) \tag{3.47}$$

$$v_{Cr}(t) = -nV_{in} - \bar{V}_{Cr} + R_1 \cos(\omega_r(t - t_0)) + \bar{V}_{Cr} \tag{3.48}$$

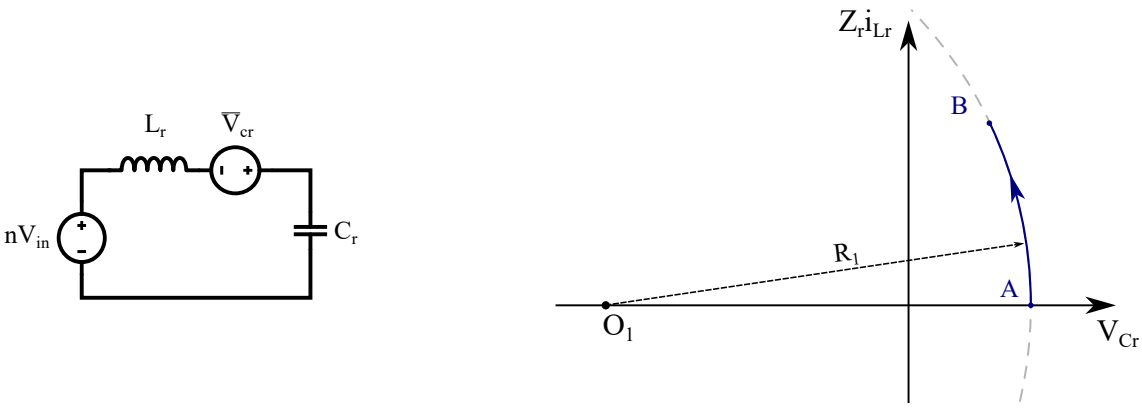


Figure 3.18: Equivalent circuit during state 1 (left), and corresponding state-plane trajectory (right).

Concerning the magnetising current, at the beginning of this period, it is at the minimum value, and since the positive voltage is being applied, it will increase

linearly as shown in (3.49). This period finishes once the specified boosting time is completed in order to achieve the required voltage step-up.

$$i_{Lm}(t) = \frac{nV_{in}}{L_m}(t - t_0) - \frac{nV_{in}}{4f_{sw}L_m} \tag{3.49}$$

Topological state 2 $(t_1 - t_2)$: The state commences with the turning off of device S_6. The current that is flowing through S_6 at t_1, will commutate to the diode D_2. At this state, power is being transferred to the output via the conduction path formed by S_5, D_2. To find the initial conditions of the resonant inductor current and the resonant capacitor voltage, once again, the angle δ is defined. Using simple trigonometry, it will be possible to express this angle in terms of resonant tank parameters.

The equivalent resonant circuit may be seen in Figure 3.19. From the circuit it is possible to derive that the trajectory path will be defined by a circle, with a centre of $O_2 : (V_o - nV_{in} - \bar{V}_{Cr}, 0)$ and a radius of $R_2 = V_o - nV_{in} - \bar{V}_{Cr} + \Delta v_{Cr}$. Since the average resonant capacitor voltage $\bar{V}_{Cr}$ can't be higher than nV_{in}, based on the operating principle of the Greinacher circuit, it can be deduced that O_2 belongs to the positive half plane of the x-axis.

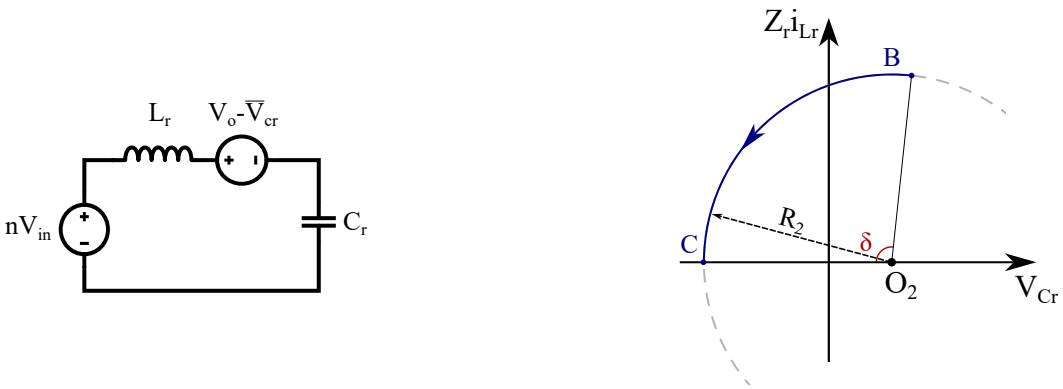


Figure 3.19: Equivalent circuit during state 2 (left), and corresponding state-plane trajectory (right).

The resonant tank will move along the trajectory path from point B to point C in a sinusoidal fashion. Using the previously defined initial angle δ, the analytical resonant tank equations for this state may be formulated as:

$$i_{Lr}(t) = \frac{R_2}{Z_r} \cdot \sin(\pi - \delta + \omega_r(t - t_1)) \tag{3.50}$$

$$v_{Cr}(t) = V_o - nV_{in} - \bar{V}_{Cr} + R_2 \cos(\pi - \delta + \omega_r(t - t_1)) + \bar{V}_{Cr} \tag{3.51}$$

The initial angle may be found as follows:

$$\delta = \begin{cases} \pi - \sin^{-1}(\frac{Z_r i_{Lr}(t_1)}{R_2}), & O_{2x} \leq v_{Cr}(t_1) \\ \sin^{-1}(\frac{Z_r i_{Lr}(t_1)}{R_2}), & O_{2x} > v_{Cr}(t_1) \end{cases} \tag{3.52}$$

Additionally, at this state the transformer is experiencing a positive voltage excitation of V_{in}. In turn, the magnetising current of the transformer keeps increasing linearly, according to (3.49).

Topological state 3 ($t_2 - t_3$) : At t_2, the resonant tank current reaches zero. The conduction path from the transformer to the output ceases to exist, so power is not being transferred. This means that for this period, the resonant capacitor voltage remains constant at $\bar{V}_{Cr} - \Delta v_{Cr}$, and the resonant inductor current remains at zero. The magnetising current keeps increasing according to (3.49), and eventually, at t_3, the devices S_1, S_4 will turn off with a turning off current of:

$$n \cdot I_m(t_3) = n \cdot \frac{nV_{in}}{4f_{sw}L_m} \tag{3.53}$$

Topological state 4 ($t_3 - t_4$) : In this period, all primary side devices are in their off state while the magnetising current is still flowing through them. This causes the discharge of the output capacitance of devices $S_{2,3}$ while $S_{1,4}$ are getting charged. With enough time in this state, $S_{2,3}$ will be fully discharged and will be conducting via their "body diode", and may turn on with ZVS. Also, at this time, the transformer switches polarity from V_{in} to $-V_{in}$.

Topological state 5 ($t_4 - t_5$) : At t_4, the devices $S_{2,3}$ turn on, and the transformer is getting fed a voltage input of $-V_{in}$. On the secondary side, the devices $S_{5,6}$ are constantly on during this state, effectively short-circuiting the transformer. However, in this short-circuit, high current is not expected, as the DC voltage of the

resonant capacitor has an opposite polarity to the transformer's output voltage. This can be seen in Figure 3.20, along with the trajectory path followed by the resonant tank.

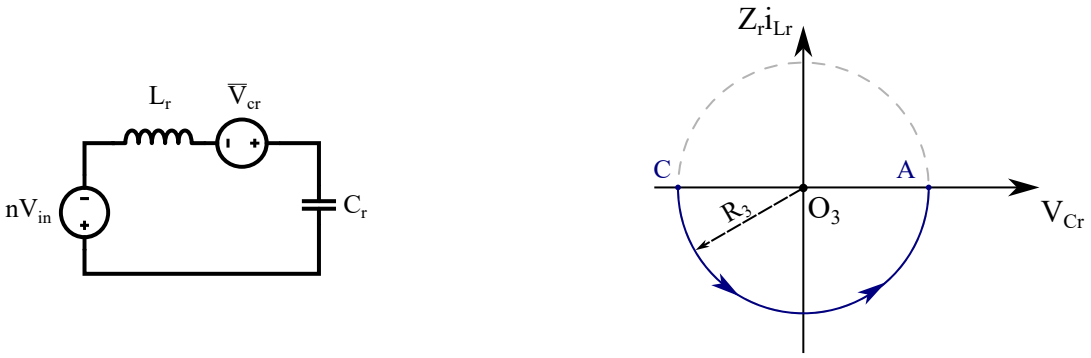


Figure 3.20: Equivalent resonant tank circuit during state 5 (left), and corresponding state-plane trajectory (right).

It can be seen from Figure 3.20 that the trajectory path followed by the resonant tank is a circle, defined by a centre of $O_3 : (nV_{in} - \bar{V}_{Cr}, 0)$ and a radius of $R_3 = nV_{in} - \bar{V}_{Cr} + \Delta v_{Cr}$. Based on this state plane trajectory, the time-based analytical equations of v_{Cr}, i_{Lr} are:

$$i_{Lr}(t) = \frac{R_3}{Z_r} \cdot \sin(\pi + \omega_r(t - t_4)) \tag{3.54}$$

$$v_{Cr}(t) = nV_{in} - \bar{V}_{Cr} + R_3 \cdot \cos(\pi + \omega_r(t - t_4)) + \bar{V}_{Cr} \tag{3.55}$$

During this period, power is not transferred to the output, but some power is transferred to the resonant capacitor in a series resonant way to charge its voltage up by $2 \cdot \Delta v_{Cr}$. This capacitor acts as an energy storage element, as this energy will be released during states 1 and 2. During this period, the magnetising current is decreasing linearly, as the transformer is getting excited by $-V_{in}$, and is expressed as (3.56).

$$i_{Lm}(t) = \frac{nV_{in}}{4f_{sw}L_m} - \frac{nV_{in}}{L_m}(t - t_4) \tag{3.56}$$

Topological state 6 $(t_5 - t_6)$: At t_5, the devices $S_{2,3}$ turn off with the magnetising current. While they are off, the magnetising current continues to

freewheel via their parasitic output capacitance. The magnetising current will be charging $S_{2,3}$ and discharging $S_{1,4}$, as may be seen from the direction of the current. As these changes occur, the transformer's primary voltage is transitioning from $-V_{in}$ to V_{in}. With enough time in this period, the stored energy in $S_{1,4}$ will be depleted, and they will be conducting in their third quadrant so that they may be turned on with ZVS.

3.2.6 Greinacher Boosting Conversion Ratio

While the analysis of the converter operation has been made in section 3.2.5, there is an unknown variable in its operating formulae. This is the DC voltage with which C_r is biased and allows for a higher voltage step-up. This analysis will be made in state 5, as the fact that the converter completes half a sinusoidal period will be exploited. Based on this fact, between $t_4 - t_5$, the average current flowing through the resonant tank can be expressed as a function of the peak current as:

$$\bar{I}_{Lr} = \frac{2}{\pi} I_{Lr,peak} = \frac{2}{\pi} \cdot \frac{R_3}{Z_r} \tag{3.57}$$

Also, during this time period, the resonant capacitor gets charged from $\bar{V}_{Cr} - \Delta v_{Cr}$ to $\bar{V}_{Cr} + \Delta v_{Cr}$. Using the fundamental capacitance equation leads to a second relation for the average current, as shown below.

$$\begin{aligned} &\Delta Q = C\Delta V = 2\Delta v_{Cr} \Rightarrow \\ &\Rightarrow \bar{I}_{Lr} = 4\Delta v_{Cr} C_r / T_{sw} \end{aligned} \tag{3.58}$$

Combining the equations (3.57), (3.58), along with the expression for the capacitor's voltage swing (3.16), and performing some simple algebraic manipulations, the result for this DC voltage is:

$$\bar{V}_{Cr} = nV_{in} \tag{3.59}$$

Now that the DC value of the resonant capacitor voltage has been found, the equations found in section 3.2.5 may be simplified, and the conversion ratio is found.

Similar to the analysis made for the voltage boosting operation, the state plane analysis will be used to retrieve the voltage step-up function. The circles defined in state 1 and state 2 intersect at t_1. This allows the solution of the following system of equations:

$$(v_{Cr}(t) + 2nV_{in})^2 + (Zi_{Lr}(t))^2 = (2nV_{in} + \Delta v_{Cr})^2 \tag{3.60}$$

$$(v_{Cr}(t) + 2nV_{in} - V_o)^2 + (Zi_{Lr}(t))^2 = (V_o - 2nV_{in} + \Delta v_{Cr})^2 \tag{3.61}$$

Inputting the time as t_1 and some algebraic manipulation, the capacitor's AC voltage may be found. This gets changed to the real voltage by the addition of $\bar{V}_{Cr} = nV_{in}$.

$$v_{Cr}(t_1) = \Delta v_{Cr}\left(\frac{4nV_{in}}{V_o} - 1\right) + nV_{in} \tag{3.62}$$

Replacing this value into the analytical equation for v_{Cr} of state 1, it is found:

$$-nV_{in} + (2nV_{in} + \Delta v_{Cr})\cos(\omega_r(t_1 - t_0)) = \Delta v_{Cr}\left(\frac{4nV_{in}}{V_o} - 1\right) + nV_{in} \tag{3.63}$$

And considering that $t_1 - t_0$ is equal to the "boosting" time (t_b):

$$t_b = \frac{1}{\omega_r} \cdot \cos^{-1}\left(\frac{\Delta v_{Cr}(\frac{4nV_{in}}{V_o} - 1) + 2nV_{in}}{2nV_{in} + \Delta v_{Cr}}\right) \tag{3.64}$$

From (3.64), it is possible to find the normalised voltage step-up as a function of the duty ratio $d_b = t_b/T_{sw}$. This is expressed as:

$$M(d_b) = 2 \cdot \frac{nP_oT_{sw} + \sqrt{(nP_oT_{sw})^2 + 2n^2P_oT_{sw}V_o^2C_r(1 - \cos^2(\omega_r d_b T_{sw}))}}{nP_oT_{sw}(1 + \cos(\omega_r d_b T_{sw}))} \tag{3.65}$$

As shown in (3.65), the voltage step-up accomplished by this converter is a function of output power and the resonant tank parameters. The relation between these two parameters and the resulting voltage gain can be seen pictorially in Figures 3.21, 3.22.

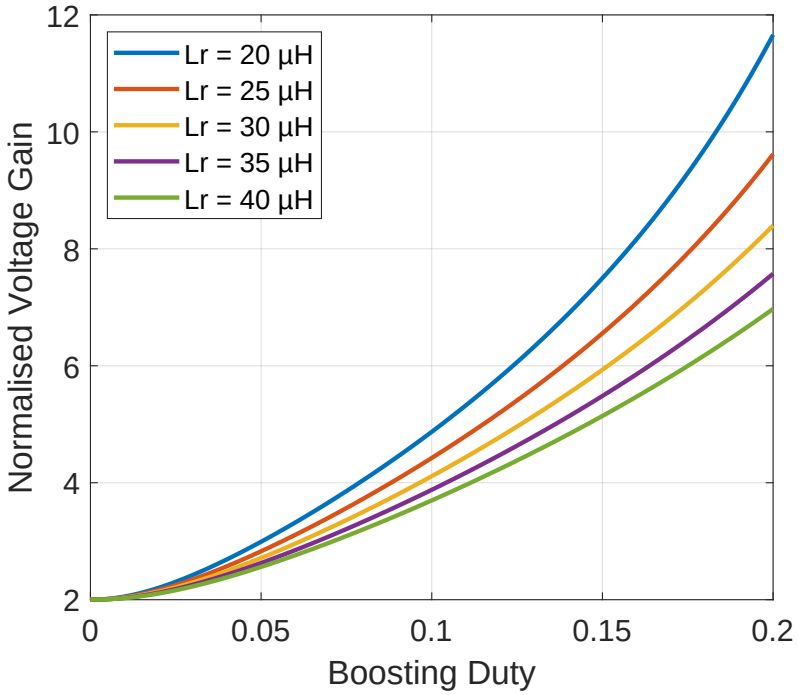


Figure 3.21: Converter voltage step-up, in Greinacher mode, with a constant resonant frequency but a variable L_r.

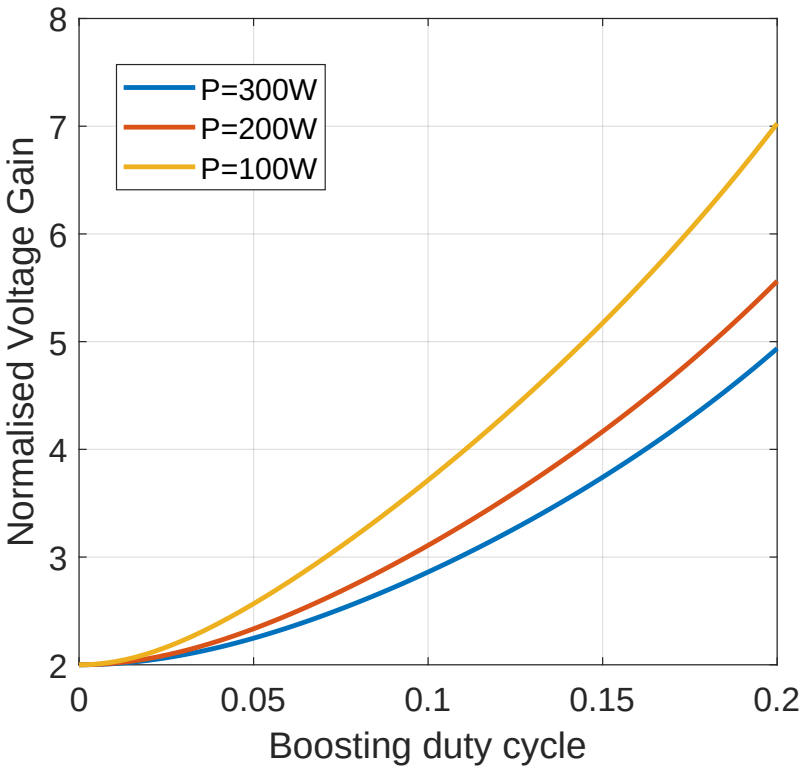


Figure 3.22: Converter voltage step-up in Greinacher mode, with all parameters staying constant apart from the output power.

3.3 Magnetic Component Design

As outlined in the previous discussions, there are several factors to consider when designing the magnetic components. First, the transformer is required for galvanic isolation and voltage step-up. The external resonant inductor is required to tune the LC filter. The transformer's leakage inductance could have taken the role of the resonant inductor, but this was not selected due to efficiency/cost concerns. In order to get a sizeable leakage inductance value out of a transformer to be used as a resonant inductor, the windings would need to be more loosely coupled; therefore, interleaving in the transformer layers wouldn't be an option, raising the cost of Litz wire to counteract the resulting R_{ac} increase, or otherwise simply increasing the copper loss. Similarly, a low resonant inductance would create high RMS currents in voltage-boosting modes; hence, an external inductor was designed. Since the application under study aims to extract the most available power from PV panels, it is reasonable to design the transformer and inductor in a way that achieves the least power dissipation.

Another effect that must be taken into consideration is that the transformer and resonant inductor will influence the achievement of the ZVS turn-on. The transformer's magnetising inductance is critical to achieving the ZVS turn-on for the primary-side bridge. The transformer's parasitic capacitance can also play a significant role, depending on the ratio of the capacitive loading due to the transformer and that of the primary bridge devices. Similarly, the transformer's leakage inductance, plus the resonant inductor placed in series, affects the dead time needed to turn the secondary-side active devices on with ZVS. Therefore, an analysis of the dead-time design is presented in the following section.

3.3.1 Dead-Time Selection for ZVS

Accurate dead-time selection is required to achieve soft switching for the proposed converter under all its operating modes. Insufficient or excessive dead time will result in rapid heating of the switches S_{1-6}, either from turn-on losses or from third

quadrant conduction, respectively. The methodology of achieving ZVS via dead time is explained with the help of Figure 3.23 and is consistent in all three operating modes of the converter.

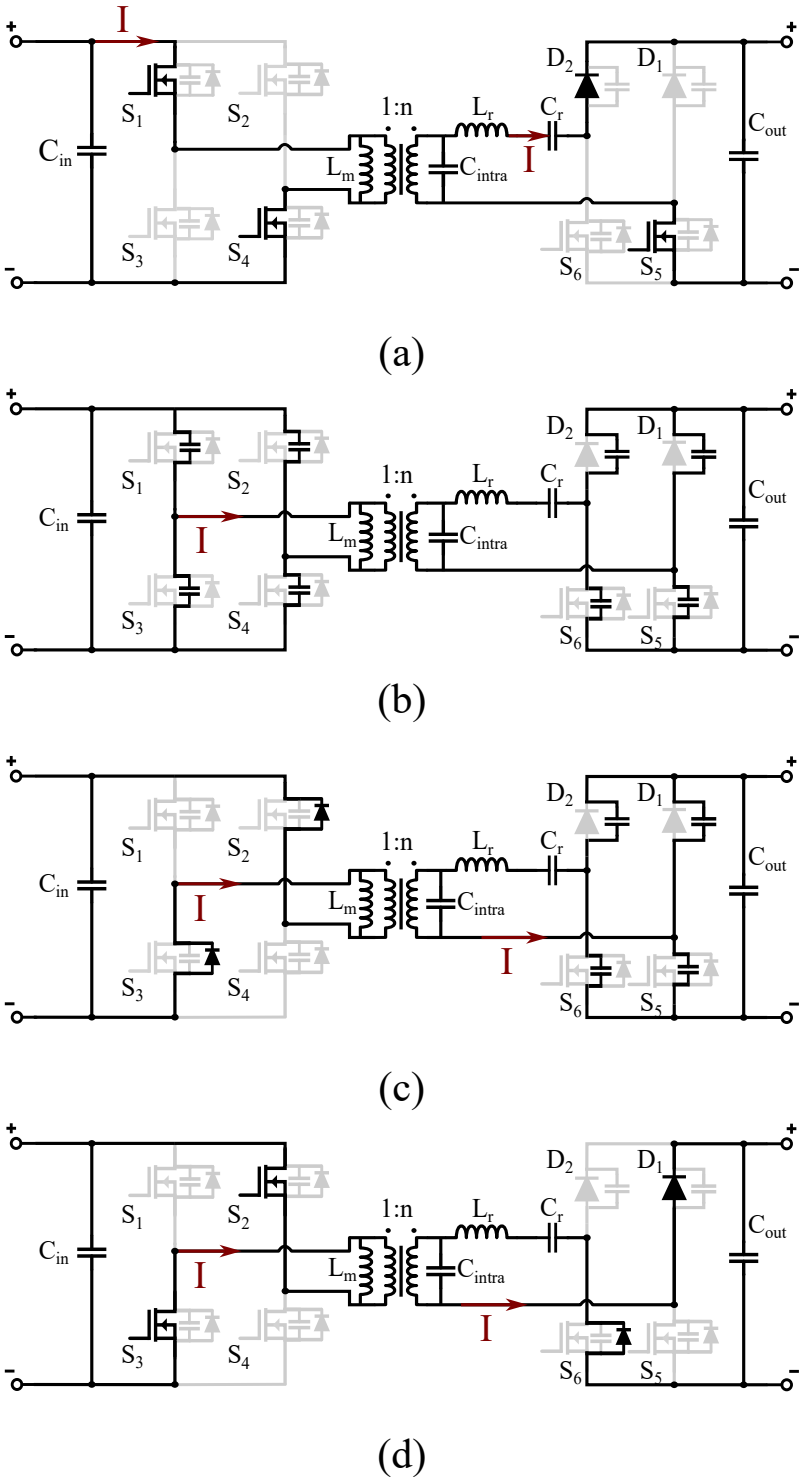


Figure 3.23: Sequence of conductive paths to achieve ZVS during dead-time intervals.

The qualitative explanation of ZVS proceeds as follows:

1. Power is being transferred via the conductive path created by $S_{1,4,5}, D_2$. The input current of the transformer is the summation of the load current plus its magnetising current (Figure 3.23(a)).

2. The load current, flowing through L_r, eventually decays to zero. Therefore, the transformer's current is now equal to the magnetising current. This is followed by $S_{1,4}$ being also turned off (Figure 3.23(b)). During this time, the current flowing through L_m charges the output capacitance of $S_{1,4}$, while discharging the capacitance of $S_{2,3}$. At the same time, this current also flips the polarity of the transformer's voltage, which is modelled as the lumped intrawinding capacitance, C_{intra}.

3. Once the output capacitance of $S_{2,3}$ is fully discharged, the devices conduct in their third quadrant, and the transformer's polarity has been flipped. During this time, $S_{2,3}$ may be turned on with ZVS (Figure 3.23(c)).

4. On the secondary side, the transformer's voltage will create a resonant circuit via L_r and the output capacitances of the semiconductor devices. Once the voltage of S_6 falls to zero, it will become clamped to the device's third quadrant operation and can be turned on with ZVS (Figure 3.23(d)).

With a qualitative understanding of the mechanism of ZVS creation, the mathematical expressions may be formulated. For the ZVS of the primary bridge, the magnetising current must provide enough energy to charge/discharge devices in the primary bridge and enough energy to flip the voltage polarity of the transformer. The result is that the current has to charge a total capacitance of $C_{oss} + n^2 C_{intra}$ from $-V_{in}$ to V_{in}, with the logic behind this derivation can be seen pictorially in Figure 3.24.

During the dead-time period (t_{dt}), the magnetising current is assumed to be constant due to the inertia provided by the magnetising inductance and the small time periods this analysis concerns. To achieve sufficient current to perform the charging of the aforementioned capacitances, the minimum value of the magnetising

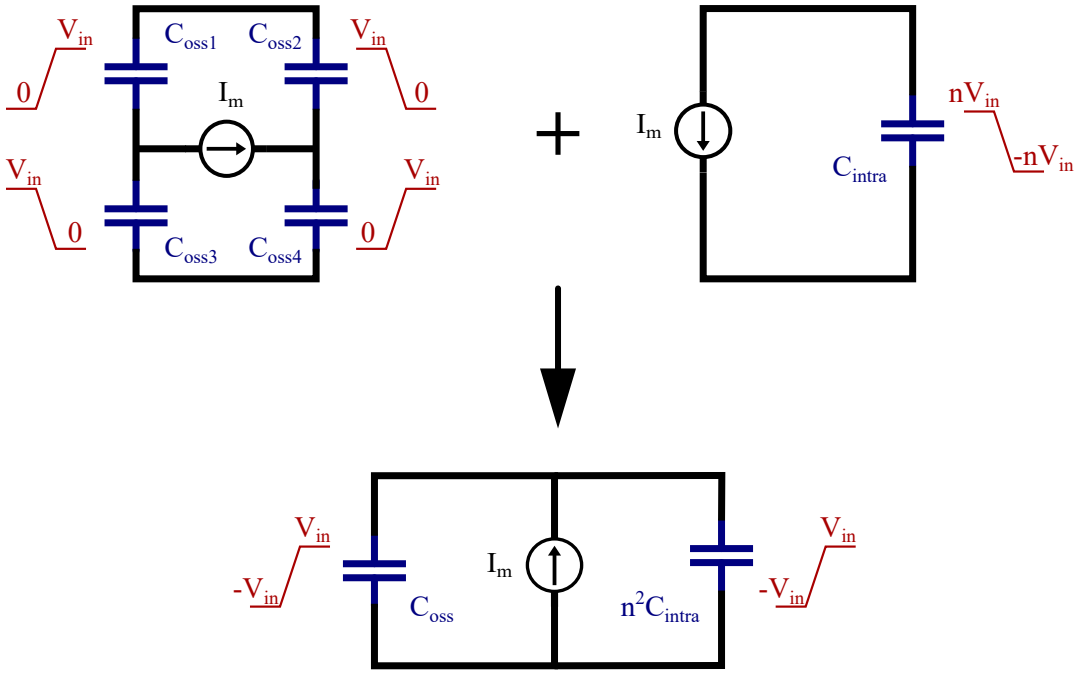


Figure 3.24: Primary-side voltage transitions during dead-time to achieve ZVS turn on.

current may be expressed as:

$$I_m \geq (C_{o(tr)} + n^2 C_{intra}) \cdot \frac{2V_{in}}{t_{dt}} \tag{3.66}$$

Considering that the magnetising inductance is modelled in the HV side of the transformer, the absolute value of the magnetising current during dead time is:

$$I_m = \frac{nV_{in}}{4L_m f_s} \tag{3.67}$$

Combining the formulae (3.66),(3.67), the maximum value of the magnetising inductance may be found to aid in the design of the transformer.

$$L_m \leq \frac{n^2 t_{dt}}{8f_s(C_{oss} + n^2 C_{intra})} \tag{3.68}$$

Concerning the required dead-time for the HV active devices S_5, S_6, the analysis begins after the conditions for achieving ZVS on the primary side are achieved, so that the voltage has reached $\pm nV_{in}$ on the secondary side full-bridge. Considering the limited dead-time value, the resonant capacitor's voltage is assumed constant during this period. The diode junction capacitances and the active device output

capacitances form a full bridge capacitor circuit, which may be simplified as shown in Figure 3.25. Not considering any manufacturing deviation, the dead-time capacitance formed is found in (3.69).

$$C_{dt} = \frac{C_j + C_{oss}}{2} \tag{3.69}$$

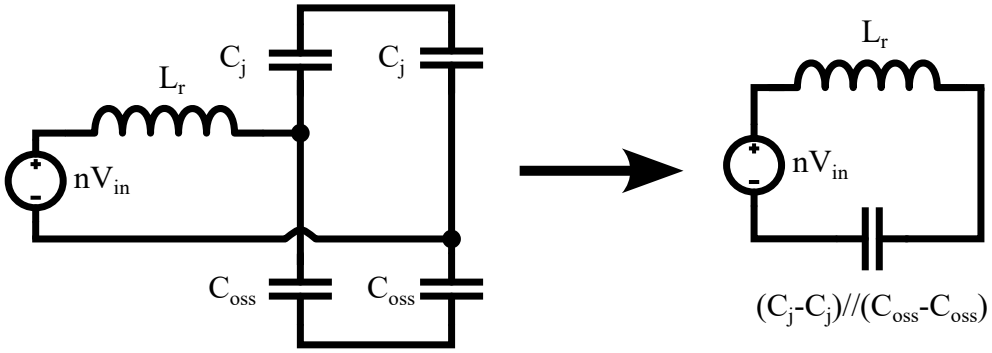


Figure 3.25: Equivalent dead-time circuit for the secondary-side devices.

The current flow in Figure 3.23 is used in this analysis. However, the result will be correct in all switching events, as the mechanism and LC resonant tank remain the same. The initial voltage on C_{dt} during dead time is the input voltage ($+nV_{in}$). The transformer changing voltage polarity will enter a voltage excitation of $-nV_{in}$. This will trigger a sinusoidal current in L_r and a sinusoidal voltage in C_{dt}. This system will hold true until the voltage on C_{dt} becomes equal to zero, after which the voltage will be clamped in the third-quadrant operation of S_6.

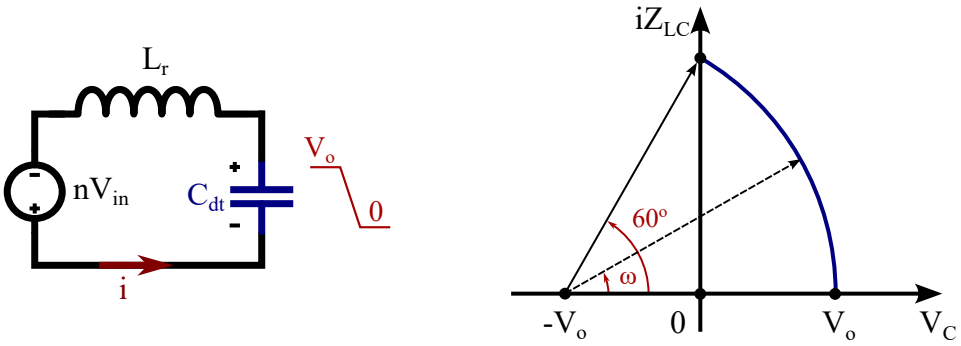


Figure 3.26: Secondary-side device voltage transition (left) and state-plane diagram (right), during its dead-time period.

State plane analysis is performed under the worst possible conditions to achieve ZVS. This is the condition of DCX operation, as in the boosting regions, the pre-

existing current in the resonant tank will aid in faster C_{oss} discharging. In this condition, the transformer and resonant capacitor will provide a pulse equal to the output voltage ($nV_{in} = V_o$). Performing state-plane analysis, the trajectory of the resonant tank will follow a circle with $O(-V_o, 0)$ and a radius $r = 2V_o$, with the initial capacitor voltage being equal to V_o. It may be seen from Figure 3.26, that the condition for ZVS turn-on is achieved at phase angle of 60°, or $\pi/3$ radians. Therefore, the additional dead time required for the secondary-side device ZVS (t_{dt2}) may be calculated as:

$$\frac{1}{\sqrt{L_r C_{dt}}} \cdot t_{dt2} = \frac{\pi}{3} \tag{3.70}$$

3.3.2 Transformer Design

The first step in designing a transformer is selecting an appropriate step-up ratio. The appropriate step-up ratio will be dependent on the type of PV panels under examination, however for a typical 60-cell module, a 35 Volt nominal voltage is considered. The aim of doing this is to allow the nominal conditions of the PV panel to be within the converter's most efficient operation mode, which is in DCX mode. Considering (3.71), it is found that a step-up ratio slightly below 11 is desirable.

$$n = \frac{V_o}{nV_{in,nom}} \tag{3.71}$$

The next step in designing a transformer is selecting a desired core shape. In this work, RM core shapes were chosen due to their good shielding properties, protecting nearby circuits from near-field EMI while still providing a generous copper winding area. Once the core shape is selected, another task is deciding the type of wire to be used to wind the transformer. Two effects have a sizeable impact on the selection of the wires, the first being the skin effect and the other being the proximity effect. The skin effect is characterised by the skin depth, which is the distance between the outer boundary of the conductor to an area where the current density is lowered by $1/e$. The formula for retrieving the skin depth is shown in (3.72), and setting an

upper design frequency limit for the converter at 140kHz, it is found that current is mainly limited at depths of $0.175\,mm$. The proximity effect is much harder to model. Still, it is based on the energy minimisation principle, in which adjacent conductors, depending on their corresponding current flow directions, cause localised increased current densities, which can be modelled as an increase of the wire's resistance when AC current is flowing through.

$$\delta = \sqrt{\frac{\rho}{\pi f \mu_0 \mu_r}} \tag{3.72}$$

To counteract the increase of the wire's AC resistance caused by the aforementioned effects, thinly stranded Litz wire may be used to minimise the skin effect. An upper limit of approximately $0.08\,mm$ is set for the wire strand diameter, which corresponds to a wire gauge of 40, to offset the resistance rise due to the skin effect. Indeed, using the estimation formula for R_{ac}/R_{dc} provided by New England Wires [103], on the upper-frequency limit of $140\,kHz$, there is merely a 6% increase in the wire's resistance with an AWG40 wire, compared to its DC value.

Litz wire combines a lot of these thin strands of wires and is usually sold with the solid wire equivalent gauge. Setting a current density limit of $5\,A/mm^2$ for the nominal power conditions, the total copper area required for the wires is approximately $2\,mm^2, 0.2\,mm^2$ for the primary and secondary wires, respectively. Additionally, Litz wire that is bundled and twisted, instead of a simple twisting operation of the strands, provides protection against the resistance increase due to the proximity effect. With the statements made in the previous paragraphs, based on the available stock in the UK market during the time of the ordering, the wires BXL2031 (435/40 AWG) and BXL2009 (300/46 AWG) were used, as they fulfil the strand diameter requirement, the available copper area requirement, and they provided bundled and twisted strands for the mitigation of proximity effects.

After selecting the type of magnetic core shape, an appropriate magnetic material ought to be selected. As the PV application operates under exposure to outside elements, high ambient temperatures may be expected, with a wide temperature

variation. Therefore, apart from selecting a material with a low core loss density, it is beneficial to have a material that performs well under high temperatures, with a relatively constant power loss density over a wide temperature. Several ferrites correspond with this requirement, so materials such as N95, N97, 3C95, and 3C97 are all suitable and may be selected according to availability. For the theoretical design below, the core material 3C95 was chosen due to its high-temperature loss behaviour.

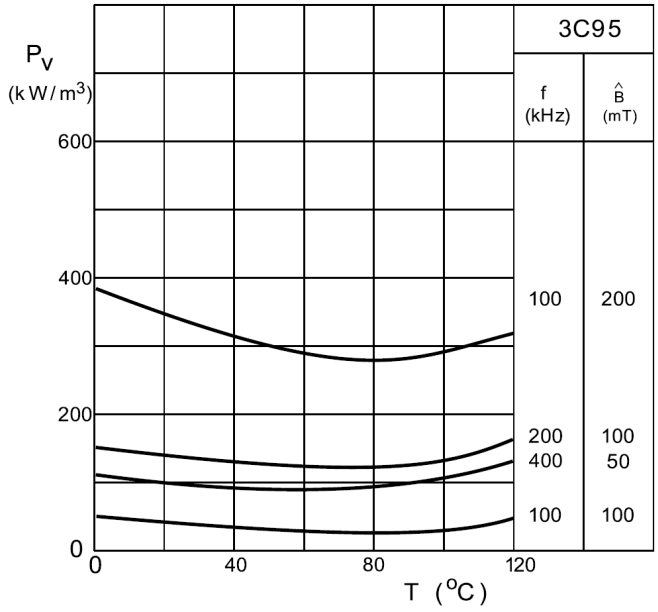


Figure 3.27: Ferroxcube 3C95 core loss density to temperature graphs, taken from the manufacturer datasheet.

With the magnetic material and wire type selected, the transformer design follows the iterative process described in Figure 3.28. Based on this flowchart, a core size is selected, and then the transformer is designed to minimise energy loss. If this results in an acceptable window fill factor, the solution is accepted, otherwise the process is repeated with a smaller, or larger core size. A small fill factor would result in a design that is taking up unnecessary space, while a high fill factor could result in the inability to fit the wires in the transformer's winding window. The fill factor of 30% is taken from the available literature as an estimate, as with round conductors, a lot of the winding window will be left empty. Plus, the use of Litz wire also degrades the possible fill factor, considering that each strand is circular and has an insulation

layer.

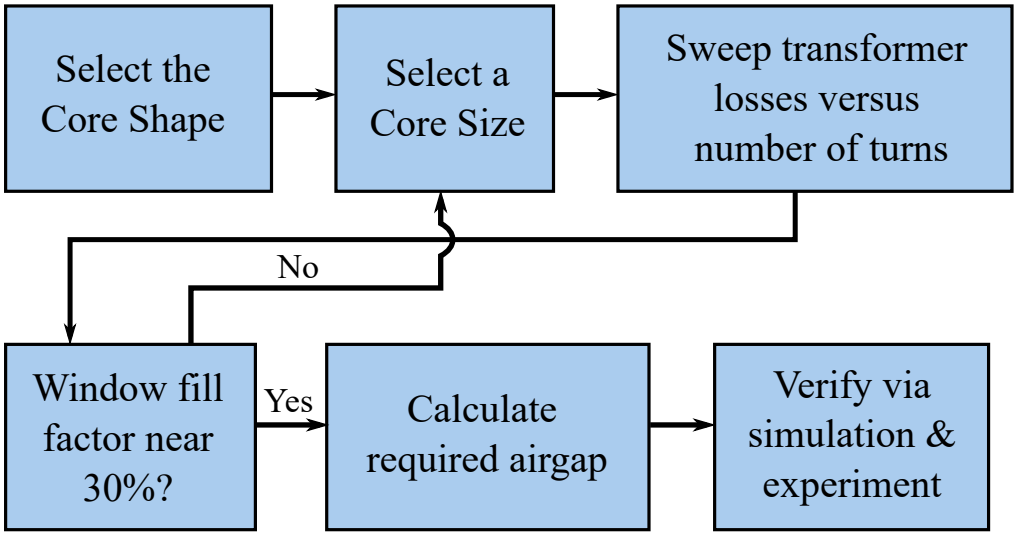


Figure 3.28: Transformer design methodology used to achieve high efficiency.

To calculate the losses in the windings, the AC resistance R_{ac} is used based on the assumption of a 140 kHz excitation. Naturally, higher-order harmonics are present, but considering the copper losses are proportional to the square of the RMS current, the first harmonic having the highest amplitude has the most significant effect on these losses. The total copper losses in the winding may be expressed as in (3.73). The wire's resistance is calculated by the Litz wire equivalent gauge resistivity, multiplied by the Mean Length per Turn (MLT) of the selected core size, the selected number of turns (N), and also multiplied by the AC scaling factor found in [103], as shown in (3.74).

$$P_{wind} = R_{prim,ac} \cdot i^2_{prim,RMS} + R_{sec,ac} \cdot i^2_{sec,RMS} \tag{3.73}$$

$$R_{ac} = \frac{R_{ac}}{R_{dc}} \cdot \rho_{Cu} \cdot \frac{MLT}{A_{eq}} \cdot N \tag{3.74}$$

This method of calculating the winding resistance isn't highly accurate, as it forgoes the addition of proximity losses. Typically, researchers use Dowell's equations [104] to retrieve a more precise scaling factor inclusive of proximity losses. However, the derived equations are based on the assumption of a 1D magnetic field in the winding area. It is already known that the designed transformer will have an air gap,

which will create magnetic field curvature on the windings positioned near the air gap. This is well-known to cause significant errors, and researchers continuously strive to publish improved R_{ac}/R_{dc} models to improve the design accuracy [105, 106]. As litz wire is used, which partially mitigates the proximity effect, and the transformer is wound in an interleaved fashion as seen in Figure 3.29, which also partially mitigates the proximity effects, it was decided not to pursue complex models for the transformer sizing, making the design procedure simpler to be implemented.

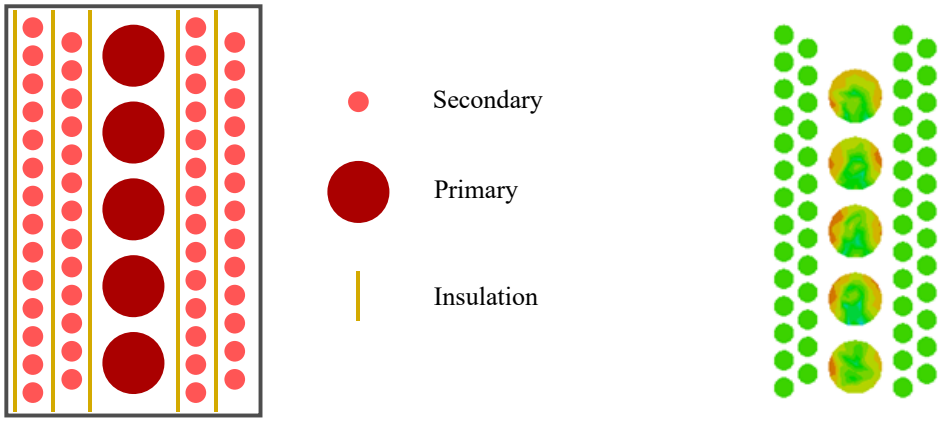


Figure 3.29: Transformer winding configuration used (left), and ANSYS 3D simulation showing the effect of interleaving on a solid primary wire (right).

For the core losses, the peak magnetising flux may be found for a square-wave voltage excitation as (3.75). During this stage, care must be taken to limit the value of B_{pk} to be within the ferrite material's linear region to avoid saturation. Having found this value, the volumetric power loss density is extracted using the manufacturer-provided Steinmetz parameters, according to (3.76). Multiplying this result by the volume of the core will give the total core loss in the selected transformer size. It should be noted that (3.76) is typically used for sinusoidal voltage excitation. However, for a square wave voltage excitation with minimal periods of zero voltage, it doesn't produce significant errors [107].

$$B_{pk} = \frac{V_{in}}{4n_1 f_{sw} A_c} \tag{3.75}$$

$$P_{core} = k \cdot f^{\alpha} \cdot B^{\beta} \tag{3.76}$$

Following the algorithm in Figure 3.28, the optimal solution was initially found

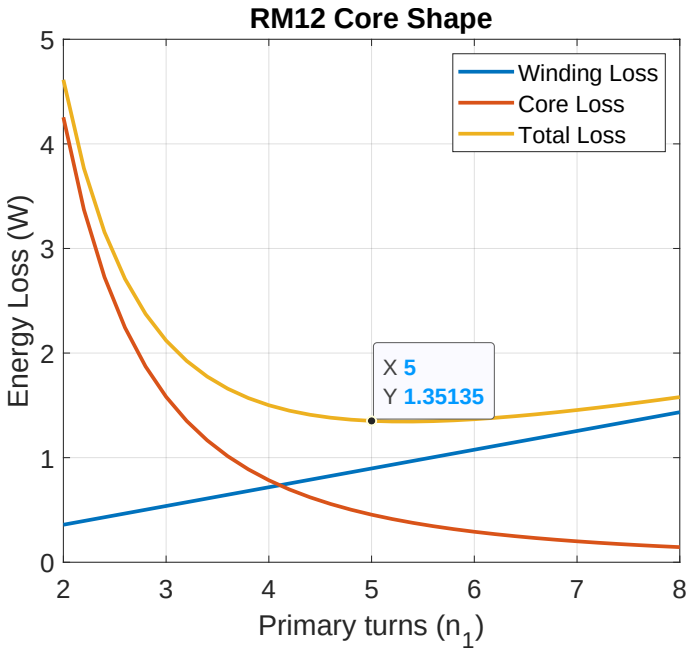


Figure 3.30: Parametric sweep of RM12 core size, with 3C95 material.

in the RM14/LP core size. Still, due to supply constraints, RM12 size was selected, with minimal efficiency trade-off ($< 1\%$). Allowing for an integer number of primary windings, the optimal solution is a turns ratio of $n_1 : n_2 = 5 : 54$, as seen in Figure 3.30.

Finally, to validate that without the use of complex R_{ac}/R_{dc} modelling didn't produce significant errors, the empirical formula in [103] is compared with ANSYS Maxwell 3D FEA results, using its integrated Litz wire modeller. A voltage excitation is provided, and the losses are computed by finding the total ohmic losses via the fields calculator for each winding and using this to extract the AC resistance ($R_{ac} = P_{ac}/I_{rms}^2$). Considerable error was found in the secondary-side resistance, but this might be expected due to the smaller turn radii used in the simulation, compared to the MLT, amplified by the high number of turns. The results are summed up in Table 3.1 considering a temperature of 25° C.

Table 3.1: Calculated & Simulated R_{ac} values

	Simple Calculation Primary/Secondary	**ANSYS 3D FEA** Primary/Secondary
$\mathbf{R_{ac}}$	$2.9\,m\Omega/305\,m\Omega$	$3.1\,m\Omega/253\,m\Omega$

After the transformer is designed, the air gap may be selected according to the dead-time requirements. Equation (3.68) will be used as a rough guideline without the inclusion of C_{intra}, as the total intrawinding capacitance is currently unknown. Setting an upper dead-time limit of 1% of the switching period, an upper limit on the secondary side L_m may be found. Using this limit and applying (3.77) [108], the required air gap may be found and then will be rounded up to correspond with standardised length values. It is preferable to use standardised sizes in order to have the air gap placed in the centre leg only. This allows for better shielding of nearby circuits from near-field EMI without the need for tooling equipment to grind down the ferrite centre leg. The summary of the designed transformer may be found in Table 3.2.

$$l_g = \frac{\mu_0 A_c n_2^2}{L_m} - \frac{l_c}{\mu_{rc}} \tag{3.77}$$

Table 3.2: Components used for the wire-wound transformer design.

Design Variable	Value	Design Variable	Value
Core type	RM12/3C95	Air Gap	$0.7\,mm$
Primary Wire	14 AWG (435/40)	Secondary Wire	22 AWG (300/46)
Turn ratio	5:54	$L_{m,HV}$	$740\,\mu H$

3.3.3 Resonant Inductor Design

Designing the resonant tank inductor is an iterative process similar to the methodology used in the previous section. Several demands need to be satisfied by the resonant inductor. First, the created LC tank must fulfil the criterion for ZCS of the secondary side devices. In a standard SRC, this is achieved by tuning the series LC filter to have a higher frequency than the PWM switching frequency. In addition to this, in the converter examined, this requirement needs to be fulfilled in the other two operational modes. For the boosting mode, a mathematical limit may be expressed as (3.78), using the initial angle δ found in Figure 3.10.

$$T_{sw}/2 \geq d_b T_{sw} + \delta/\omega_r = d_b T_{sw} + \sin^{-1}(R_2\, sin(\omega_r d_b T_{sw}))/\omega_r \tag{3.78}$$

Whilst (3.78) provides an extra requirement in theory, practically, the requirement in the SRC mode is stricter, thereby making (3.78) redundant. One might observe that in both voltage step-up modes, such as in Figure 3.10, the centre of the circle formed by the state-plane trajectory, when S_5, S_6 are both ON, is always further away from the axis origin. As the rotational speed of the state plane (ω_r) is constant during conduction periods, having part of the trajectory travelled by a circle of larger radius and then transition to a smaller circular path means the current increased at a faster rate than if it was moving in a fixed circular path. Therefore, ZCS is guaranteed for both the voltage boosting mode and the Greinacher boosting mode by fulfilling the SRC requirement for ZCS.

The selection of the inductor's inductance value is a trade-off between efficiency at the DCX mode versus efficiency during the step-up modes. As shown in the previous sections, a higher L_r will require a higher duty cycle for the same voltage step-up. In this way, the current flows through a larger percentage of the operation; hence, RMS currents are lower. In addition, as the power transfer is extended over a more significant percentage of the period, the turn-off currents of all the active devices will be lower with a higher resonant inductor. Plus, a broader duty cycle will make the converter easier to control. Nevertheless, inductors come with additional losses in the form of winding and ferrite core loss. A value of approximately $30\,\mu H$ was selected as a guideline since this value will limit the duty cycle range between 0-10% for a normalised voltage step-up ratio of 4:1.

The design of a resonant inductor resembles very closely the methodology followed in Figure 3.28. Once again, the RM core shape is selected, with 3C95 ferrite material for a wide-temperature operation range. Loss minimisation was the objective, and with the minimised loss solution, a winding window fill factor of 30% was aimed to make good use of the available space. The result of these parametric sweeps is an RM7 inductor shape, with 16 turns, as seen in Figure 3.31. After the turn number is

decided, the air gap is then selected to conform to the inductance value of L_r, using (3.77). The designed inductor's parameters can be seen in Table 3.3.

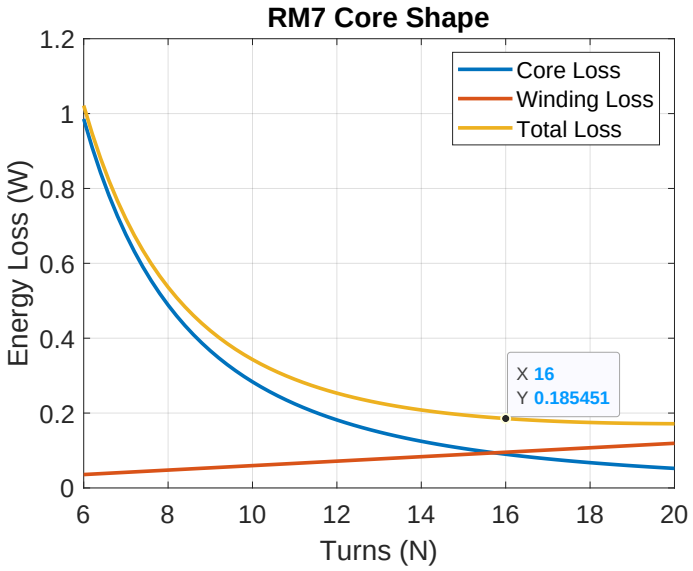


Figure 3.31: Parametric sweep of RM7 core size, with 3C95 material.

Table 3.3: Components & values used for the wire-wound inductor design.

Design Variable	Value
Core Type	RM7/3C95
Turns	16
Winding Wire	22 AWG (300/46)
Air-gap	$0.5\,mm$
L_r	$27\,\mu H$

3.4 Converter Verification via Simulation

The power electronic simulation tool PLECS has been used to verify the proposed converter's validity. At this point, all the modelling will be done with ideal components to provide results similar to the theoretical analysis conducted in this chapter.

The circuit used can be seen in Figure 3.32, in which the converter is fed an input voltage and a PI controller is used to adjust the duty cycle to achieve a $380\,V$ output voltage. The load resistor can be adjusted to demand the requested power. The simulation was run at DCX Mode, with $300\,W$ power being delivered to the

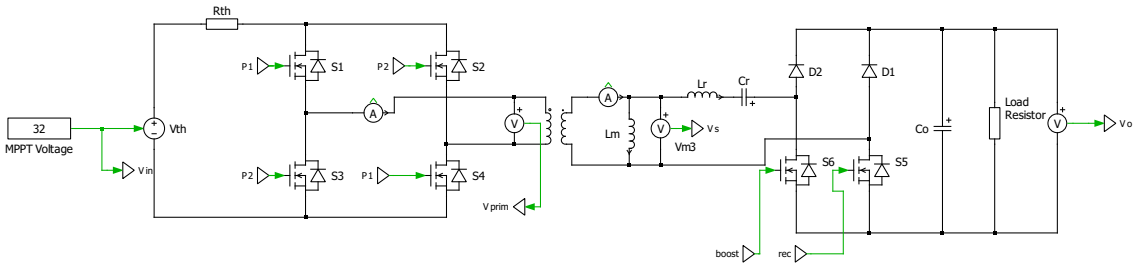


Figure 3.32: PLECS simulation circuit with ideal components, used to create the simulation graphs in this chapter.

load resistor, at boosting mode with $32\,V$ input voltage and $300\,W$ output power, and at greinacher boosting mode with $16\,V$ input voltage and $200\,W$ output power. The transformer step-up ratio used is $5:54$, as decided in the previous section.

When running these simulations, first, the state-plane trajectory is verified. This is done by probing V_{Cr}, I_{Lr} and multiplying the latter by the resonant tank impedance. Feeding the capacitor voltage in the x-axis and $Z_r I_{Lr}$ in the y-axis of an XY scope block, it is possible to create the state-plane trajectories during converter operation. It is shown in Figure 3.33 that the retrieved state-plane trajectories have a similar shape compared to the theoretical analysis conducted in this chapter. Similarly, the time-based signals of the two boosting modes that have been analysed theoretically before appear consistent with the simulation results in Figure 3.36.

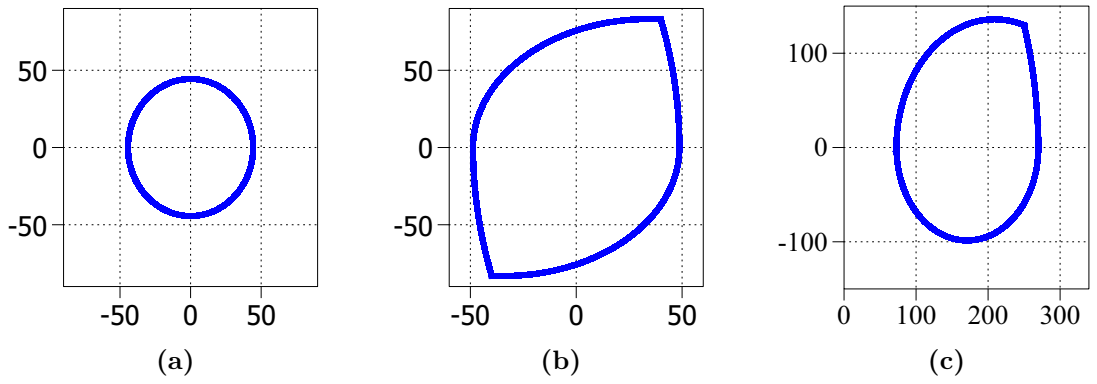


Figure 3.33: X-Y diagrams generated by PLECS simulation, for the SRC mode (a), the boosting mode (b), and the greinacher boosting mode (c).

Finally, the validity of the duty cycle derivation is tested. This is done by generating a voltage step-up versus duty cycle curve via MATLAB using the theoretical duty cycle equations (3.46), (3.65), and keeping the output power and resonant tank

parameters constant. Then, using the PLECS model in Figure 3.32 with the same parameters as those used to solve the equations, the input voltage is altered to change the voltage step-up, while its PI controller fixes the output voltage at 380 V. The load resistor sets the output power at the desired level. Following this methodology, it is found that the simulation results in an excellent agreement compared to the theoretical analysis, as seen in Figures 3.34, 3.35. The plotted lines correspond to the theoretically calculated values, while the asterisks represent values acquired by running the simulation circuit. Some minor discrepancies can be seen, which might be attributed to the rounding error when logging the values.

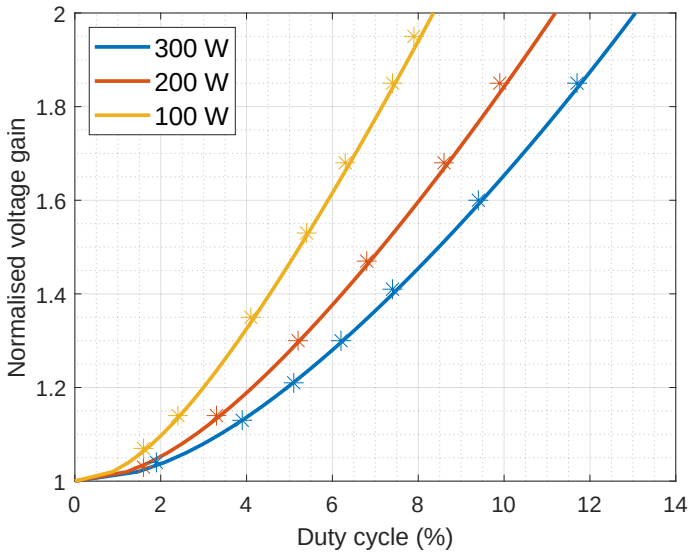


Figure 3.34: Gain to duty cycle ratios for the voltage boosting mode.

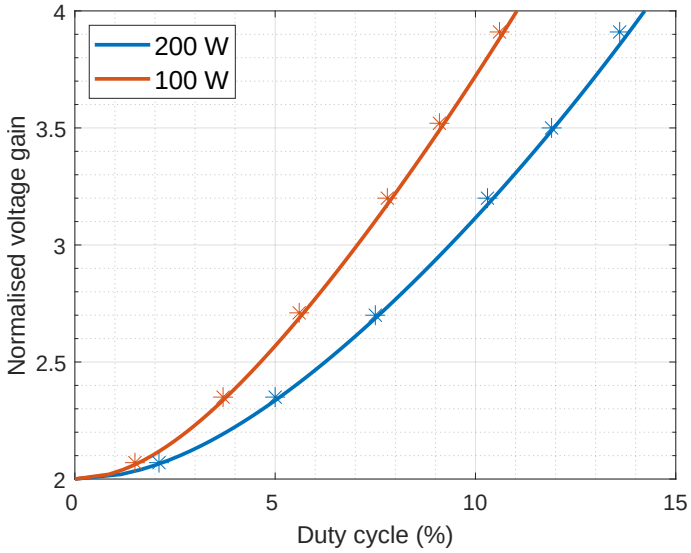


Figure 3.35: Gain to duty cycle ratios for the greinacher boosting mode.

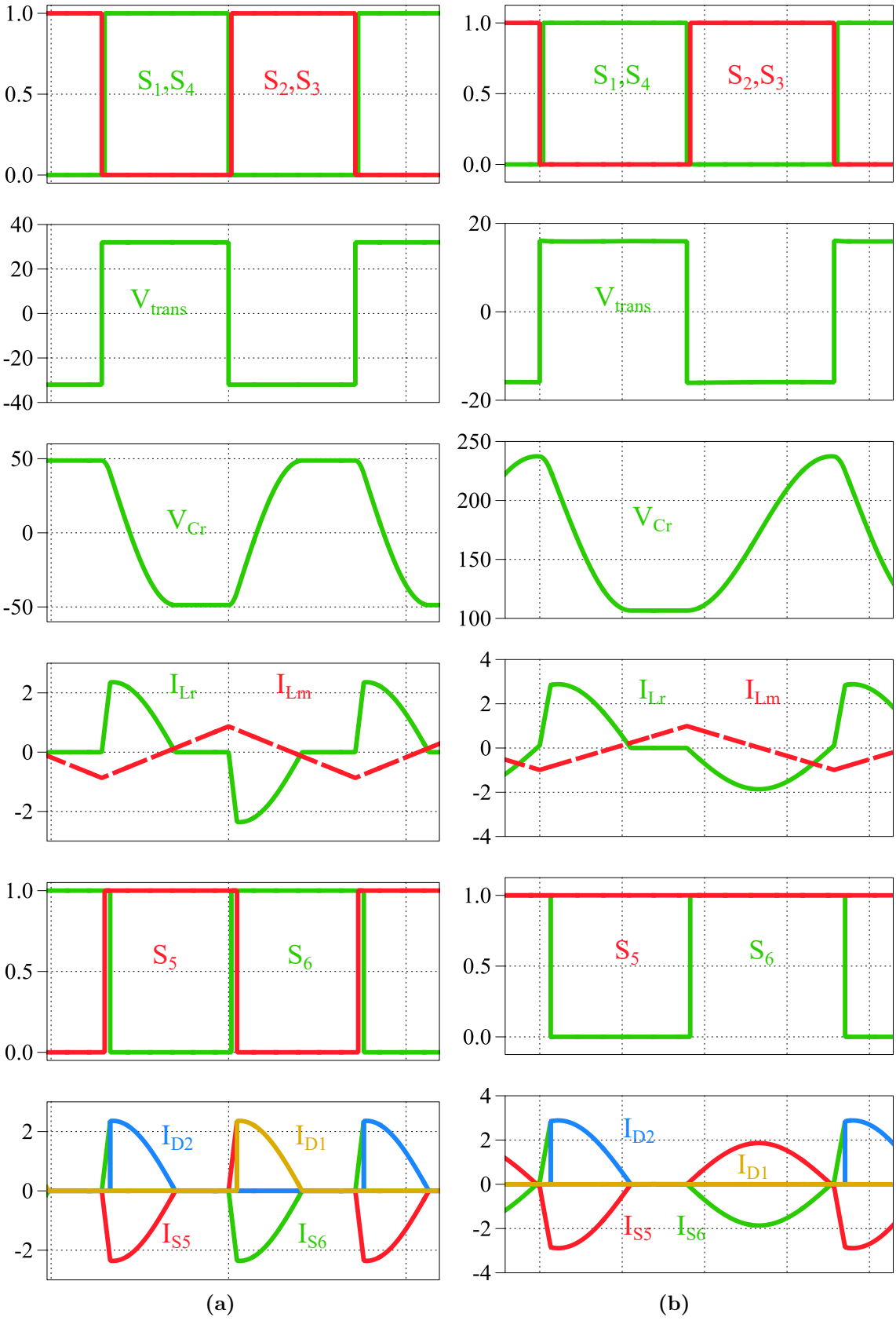


Figure 3.36: Converter providing voltage step-up capabilities in its boosting mode (a), and the greinacher boosting mode (b).

3.5 Summary

A topology-morphing series resonant converter has been proposed in this chapter. The three distinct modes of operation have been analysed in detail. The soft-switching characteristics have been analysed, and the magnetic design required to fulfil the soft-switching requirements has been detailed. It is seen that soft-switching is achieved in all operation modes, with no load dependency, thereby making the converter efficient in a wide range of voltage step-up ratios. The theoretical analysis is then cemented by verifying its accuracy via PLECS simulation. Good agreement is shown, and therefore, the concept will be further proven by experimental results in a later chapter.

Chapter 4

Performance Evaluation of GaN Devices

4.1 Introduction

The proposed converter operates in ZVS in all operating conditions while achieving ZCS in some conditions. Its efficient performance and even its applicability rely on low switching loss, as it's meant to be able to operate in high-temperature conditions with no active cooling. Therefore, it is wise to verify the datasheet values of the GaN devices to ensure that the converter obtains the expected performance.

The most major parts of the converter's efficient operation are the ZVS that is expected on the primary side full-bridge and the turn-off loss on the secondary side GaN Devices. For the former, the energy stored in the primary-side transistors in the form of the equivalent output capacitance is critical to achieving ZVS turn-on. This is important, as during the dead-time period on the primary side, no power transfer occurs, so predicting the time it takes to achieve ZVS is a crucial parameter. For the secondary-side devices, ZVS occurs with current flowing through them and transferring their stored energy to the output load, so the accurate characterisation of their C_{oss} is of lesser importance. However, they will be performing hard switching turn-off transients, with a variety of current levels as the converter's duty cycle

changes.

Therefore, the junction capacitance of EPC2021 is characterised in this chapter, as its value is crucial in obtaining ZVS via the magnetising current during dead time. In addition, dynamic characterisation is performed on two different 650V GaN HEMT devices with two aims. Firstly, to retrieve a more reliable figure for turn-off losses, as the only available source in the literature are SPICE models, which may fail to take into account the actual circuit layout, assembly errors, inaccurate SPICE modelling, etc. Secondly, there is a growing shift in the power electronics community, which is to replace the traditional combination of a power FET and gate driver with an integrated power IC. These types of devices provide monolithic integration of the gate driver with the power device, allowing for the minimum possible parasitic inductance in the gate-source loop, which, in principle, should reduce the switching losses. Thus, this chapter compares the switching performance of similarly rated devices in terms of voltage and current rating, GS66502B from GaN Systems and NV6115 from Navitas, to examine any potential efficiency benefits from the monolithic integration.

4.2 Junction capacitance characterisation

The transistor's junction capacitances are an essential metric, as they store energy that will be lost in a hard-switching converter. Also, from the fundamental circuit theory, smaller capacitances require less charge to change their voltage, according to $Q = C \cdot V$. This means that smaller capacitances, apart from minimising potential energy loss, allow for higher voltage transition rates.

In principle, since a FET is a three-terminal electrical device comprising of drain, source and gate, there are three junction capacitances of interest, C_{gd}, C_{gs}, C_{ds}. However, for power electronic designers, it is more typical to use the input (C_{iss}) and output (C_{oss}) capacitance. The input capacitance is the capacitance seen at the gate terminal when the drain and source are shorted. Likewise, the output capacitance is the capacitance seen at the drain terminal when the gate is shorted with the source terminal. The relation of those capacitances with the fundamental capacitance values is as follows:

$$\begin{aligned} C_{iss} &= C_{gd} + C_{gs} \\ C_{oss} &= C_{dg} + C_{ds} \end{aligned} \tag{4.1}$$

For the successful ZVS turn-on transition, the output capacitance is the metric of interest, and from equation (4.1), it is seen that the drain to source and gate to drain capacitance must be measured to construct the function of the output capacitance. The output capacitance varies significantly with voltage, as with increased voltage stress between drain and source, the electrons in the 2DEG get depleted. To achieve ZVS at a specific voltage level, power electronic designers use the charge equivalent output capacitance of the device, which may be calculated as:

$$C_{oss} = \frac{\int_0^V C_{oss}(V)\, dV}{V} \tag{4.2}$$

Using equation (4.2), it is possible to more accurately predict the dead-time requirements versus using the default data-sheet parameters, which concern only one

operating state of the device.

4.2.1 Experimental Setup

Since the selected Device Under Test (DUT), EPC2021, comes in a Land-Grid Array (LGA) passivated die package, a PCB was created in order to facilitate the measurements. The PCB is designed in a way that produces the least amount of parasitic capacitance in the measurements, so a single-layer PCB is selected. It should be noted that EPC devices consist of multiple GaN HEMTs in parallel, so all pins need to be connected to the drain and source pads to retrieve an accurate measurement. At the exposed pads shown in Figure 4.1, connections were made with thin wire (AWG 40) to minimise parasitic capacitive loading.

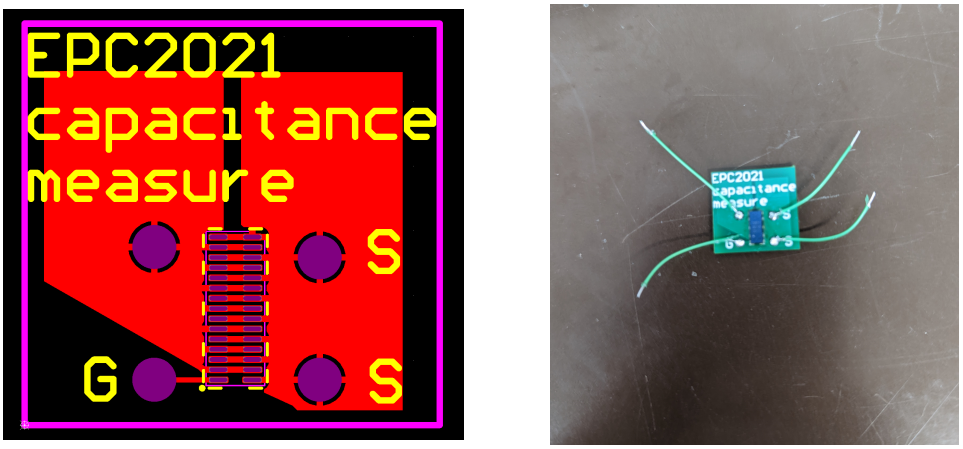


Figure 4.1: The designed PCB (left) and the received PCB with the test leads soldered (right).

Proceeding to the measurement setup, an impedance analyser, Keysight E4990A, along with the 16047E Test Fixture, is used to measure leaded components. Open and short compensation was done in the instrument to minimise the measurement error. Open compensation was achieved by attaching the identical wire strands, with the same length, to the Text Fixture and running the built-in Open compensation function. This, in principle, should clear any residual capacitance owed to the test fixture, as well as the capacitance between the wires. Afterwards, short compensation was done by connecting the Source terminals to the "High" and "Low" connections of the fixture and then running the built-in short compensation function. Similarly,

this is to compensate for any error arising due to the parasitic inductance of the fixture and the wires.

To enable the measurement of two ports in a three-port device, the impedance analyser provides a guard connection. A guard connection can be used to compensate for current flowing through the third terminal, away from the measured current value [109]. For example, in the case of the DUT, if the Drain and Source are connected to the text fixture and, therefore, have an excitation voltage applied between them, some current would flow through the capacitive coupling to the gate. By connecting the gate to the guard terminal, these currents get fed into the impedance analyser, avoiding the path in which the current is measured. This feature enables the acquisition of accurate two-port measurements in three-port devices and is used in this work.

Based on equation 4.1, since the research aims to confirm the output capacitance of the DUT, C_{ds}, C_{dg} must be measured. The schematics of the connections with the Impedance Analyser are seen in Figure 4.2, for both the C_{ds} and the C_{dg} measurement.

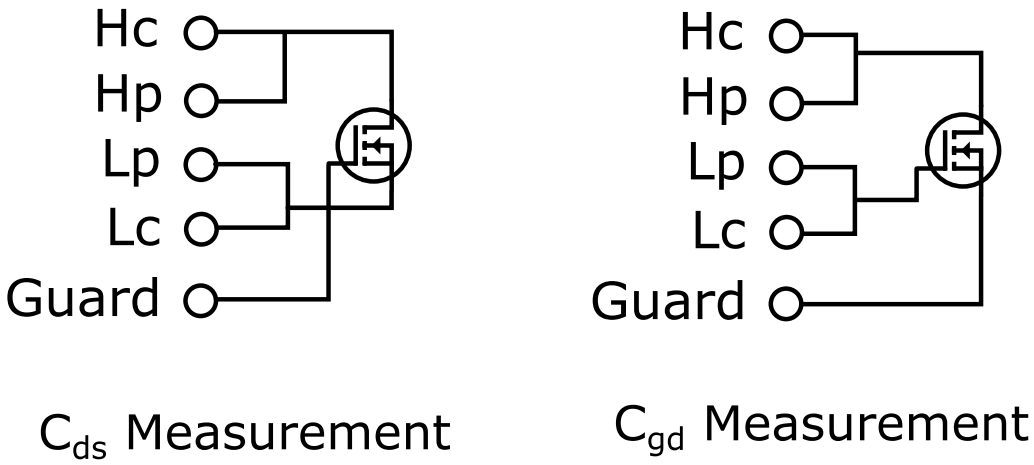


Figure 4.2: Capacitance measurement schematics, for connection to the Keysight E4990A.

The measurements are facilitated by the E4990A's in-built DC voltage bias module. It can perform measurements with a biasing voltage within the ranges of $\pm 40\,V$. Also, it can be set up to perform a DC voltage sweep, with the exciting voltage's amplitude and frequency being fixed values. Based on this, a DC voltage

sweep was performed along the range of $0 - 40\,V$, with an exciting voltage frequency of 1 MHz and a voltage amplitude of 50 mV. The experimental setup can be seen in Figure 4.3, and the resulting waveforms for C_{ds}, C_{dg} shown in Figure 4.4.

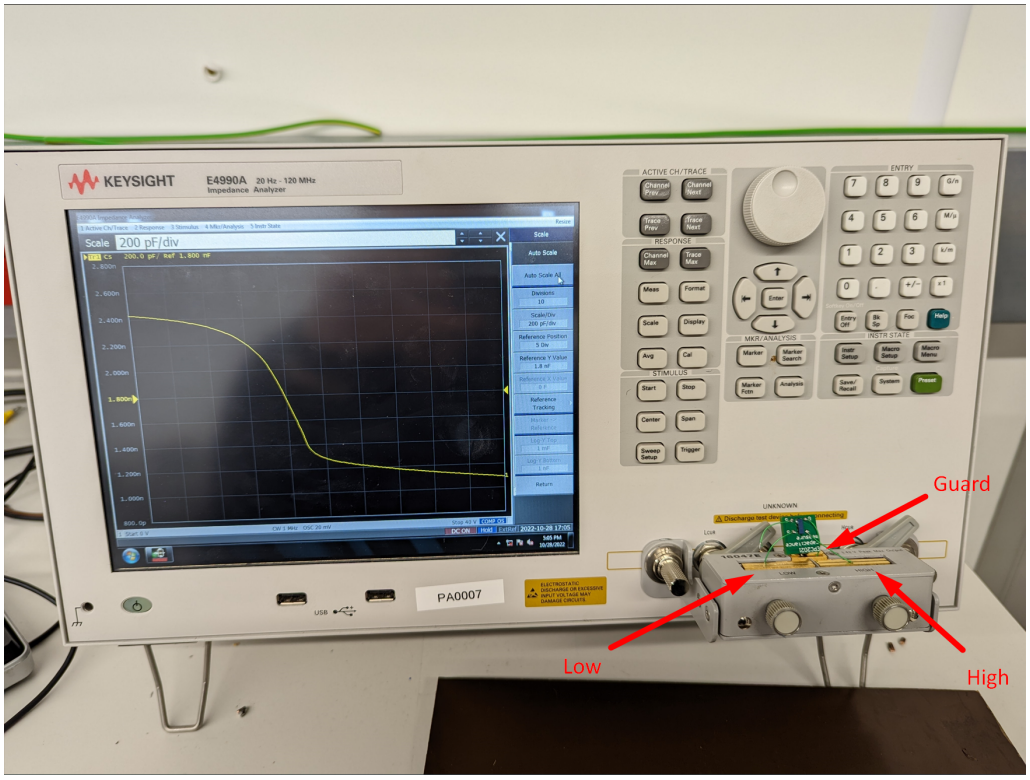
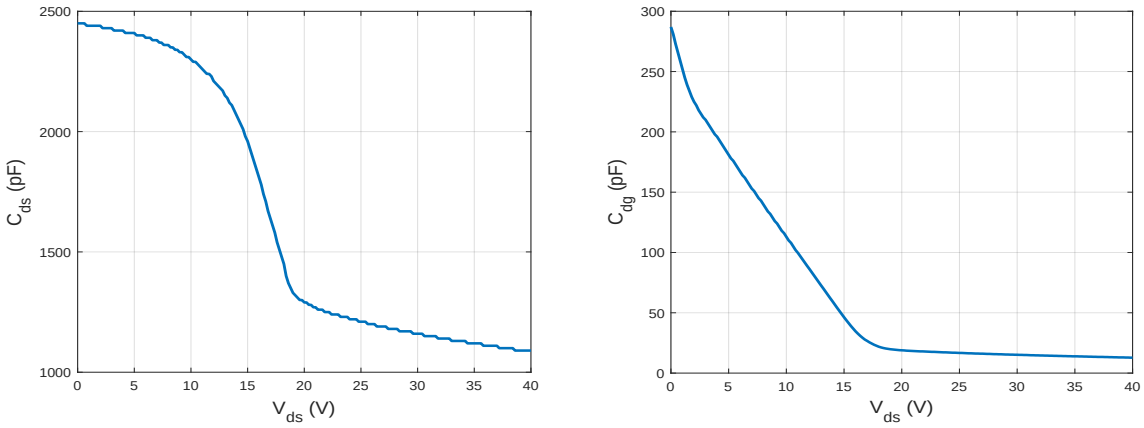


Figure 4.3: Image of the performed voltage sweep



(a) C_{ds} Sweep **(b)** C_{dg} Sweep

Figure 4.4: Voltage sweep of C_{ds}, C_{dg} with Keysight E4990A

Having measured these two capacitances as a function of voltage, C_{oss} is calculated according to equation 4.1. The results are compared with the data-sheet values in Figure 4.5, and have a good agreement, with the only difference being that the 2DEG

fully depletes faster than expected, as shown by the capacitance "knee" being at a slightly lower voltage, compared to the manufacturer's values. This can be expected with manufacturing differences between each die. Still, the capacitance at low voltage and the capacitance beyond the knee are converging, which leads to the conclusion that the manufacturer-provided data is reliable.

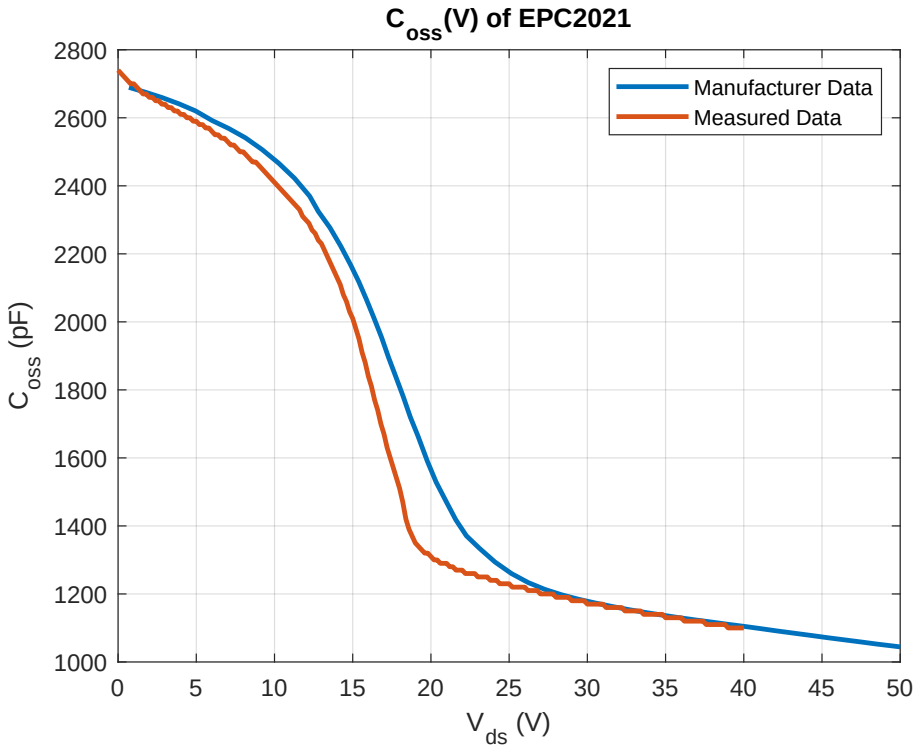


Figure 4.5: Measured versus given C_{oss} characteristic.

4.3 Dynamic Characterisation of 650V GaN HEMTs

Another aspect of the device behaviour that is deemed worthy of examination is the switching performance of the high-voltage devices. It is anticipated that these devices might be contributing significantly to the overall losses in the two voltage step-up modes. This is because they hard switch during turn-off in the presence of higher voltage levels compared to the primary devices. Furthermore, experimental switching loss data for the devices of interest seems to be lacking in the available literature. Plus, to the author's knowledge, there isn't an available publication comparing the switching performance of a similarly rated discrete GaN HEMT with one with an integrated gate drive. Therefore, this was taken as an opportunity to compare two similarly rated GaN devices, one with an integrated gate driver and one without. The integrated drive device used is NV6115 from Navitas Semiconductor, and the discrete GaN HEMT is GS66502B from GaN Systems Inc.

The switching device performance is tested using a well-known procedure called double pulse testing (DPT). The test comprises a half-bridge switching cell, a load inductor to provide the testing current stability, bulk capacitors to provide the testing voltage stability, and additional decoupling capacitors for high-frequency noise attenuation. The methodology behind the design of these components is widely available, and for this work, the methodology provided by [110] is used. The equations used won't be presented here, but may be found in the mentioned publication, however the idea behind the sizing is to allow the voltage and current levels during the switching intervals to stay within an arbitrary agreeable range by providing large enough values in the load inductor and capacitor.

For the half-bridge module, two active devices or a combination of an active device and a diode can be used. Typically, the module used must be in agreement with the intended end-use application circuit. This will provide the most valuable results, as it will be shown later in this work that the selection of the complimentary

device alters the results. Since the converter studied has a lower side active device and an upper side diode, the schematic shown in Figure 4.6 is used. The testing comprises of firing a gating pulse to the Device Under Test (DUT), in order to charge the load inductor to the desired testing current. When this is achieved, the device is rapidly turned off and then on, allowing sufficient time for any switching noise to subside. Using the captured waveforms, the turn-off and turn-on losses may be determined.

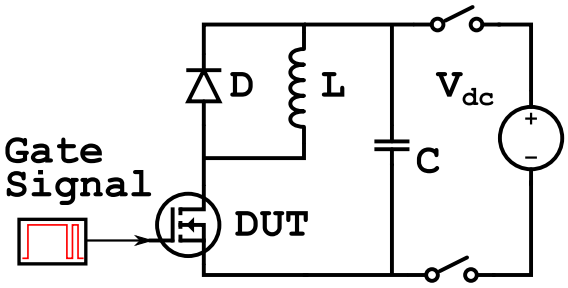


Figure 4.6: Schematic of the DPT Circuit.

A simple model was constructed in the LTSpice environment to test this concept in a simulation environment. The schematics of this model can be seen in Figure 4.7. The resulting waveforms on the DUT can be seen in Figure 4.8, in which the DUT's voltage V_{ds} and its source current I_{ds} is measured, and the instantaneous power loss is computed by multiplying those two values.

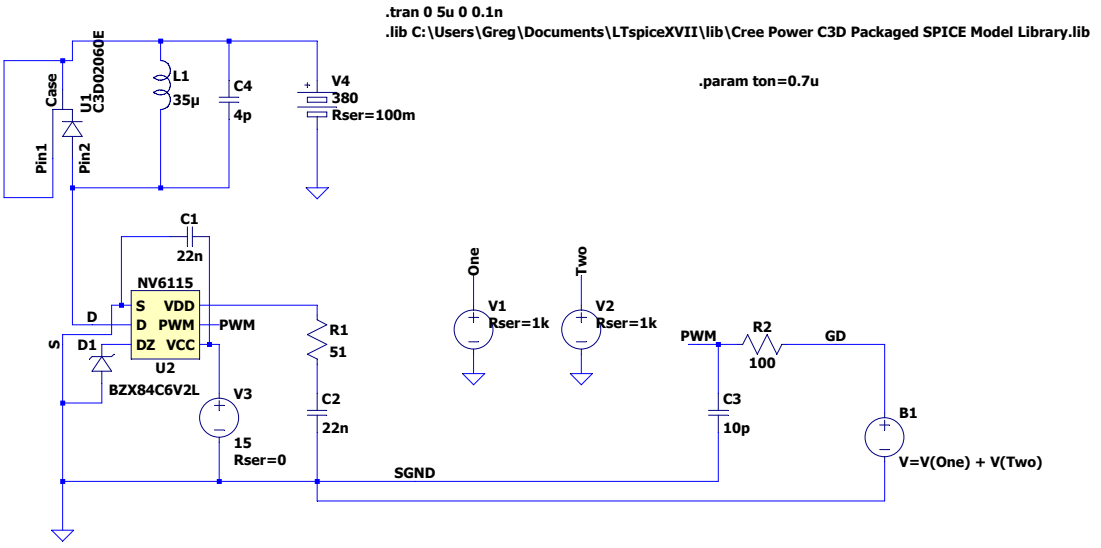


Figure 4.7: Simple LTSpice DPT model.

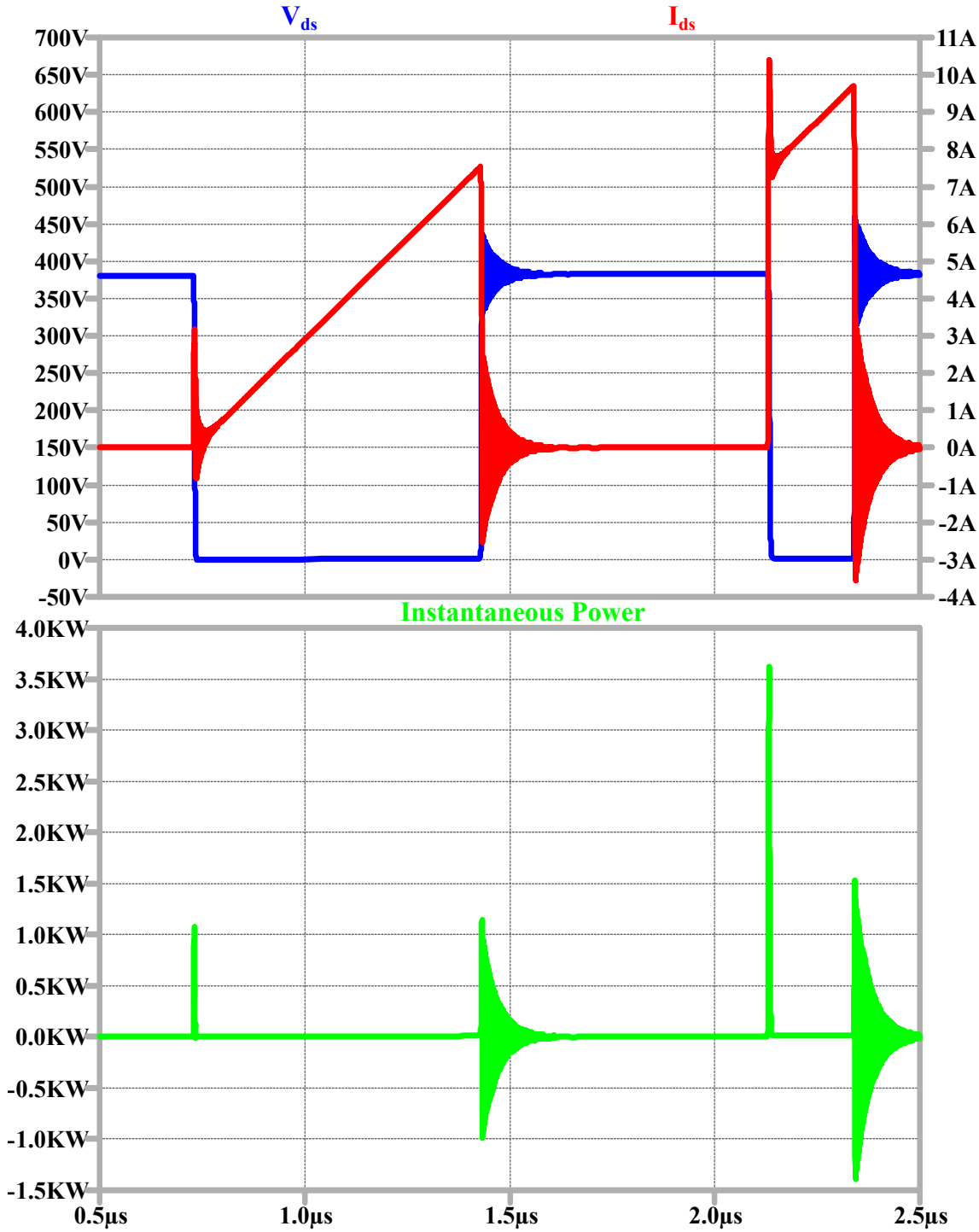


Figure 4.8: Resulting DPT waveform from LTSpice Simulation.

While the idea behind this test is relatively straightforward, some aspects of it need further consideration. As part of this research work, the author has designed and tested two versions of the DPT boards, which can be found in the Appendix A. However, both of these designs have their flaws, with the first iteration having a catastrophic fault based on its layout. This fault created false triggering of the devices, manifesting as a series of false turn-on instances as an effect of the added inductance shared between the gate drive loop and the power loop. In the second design, while there are no problems concerning the device operation, the layout selected produces inaccurate turn-off energy results due to an altered current reading. The reasons behind this will be explained in more detail in a later section.

4.3.1 Component Values & Instrumentation

As mentioned before, the dimensioning of passive components was done using the existing guidelines from [110]. Using those guidelines, a voltage/current ripple of 5% was estimated for the dimensioning of L, C. For the load inductor, an air-core inductor was chosen to ensure a linear magnetisation curve, i.e. a constant inductance value over the whole current range. The inductor was wound on a readily available PVC tube, and a single-layer structure was selected to minimise the inductor's parasitic parallel capacitance value. Upon constructing the inductor, it was measured using the Keysight E4990A impedance analyser and using its low-frequency value and the resonant frequency, the inductance was found at $192.8\,\mu H$ and the parallel capacitance at $4.8\,pF$. Concerning the DC-Link capacitors, film capacitors were connected in parallel to form an equivalent capacitance of $2.2\,\mu F$.

Furthermore, decoupling capacitors equivalent to $70\,nF$ were used to limit the noise during switching intervals. The package size of the decoupling capacitors used was 0603 in an effort to limit their added parasitic series inductance, as this was the smallest package found with a suitable voltage rating. The shunt resistor for current measurement is selected at the highest value that can still display the required current. A higher resistor value will produce a higher voltage drop, which will require

less amplification when entering the oscilloscope, improving the signal-to-noise ratio. In this regard, a coaxial current shunt of value $0.5\,\Omega$, SSDN-50 is selected.

Concerning the matter of instrumentation, one of the most important parameters is their available bandwidth. GaN HEMTs switch extremely fast, pushing the limits of the available instrumentation. For this reason, the data acquisition system should have the highest possible sampling rate to capture enough data points during the fast switching transitions. To gain an appreciation for the required bandwidth, equation (4.3) can be referred from [110]. Using this equation, for an accurate representation of a voltage transition of $2\,ns$, a bandwidth of approximately $800\,MHz$ is required. The selection of $2\,ns$ has been made following LTSpice simulations, in which it seems to be the highest switching speed during turn-off intervals for the devices to be examined. In addition, this is approximately the bandwidth limit of available instruments in the lab. Based on this analysis, for voltage sensing, passive probes possessing bandwidth of $1\,GHz$ are used, and a non-isolated oscilloscope with the same bandwidth, with a sampling rate of $5\,GSa/s$. The coaxial current shunt used also has a bandwidth of $800\,MHz$ according to its manufacturer. Finally, it was decided that all waveforms captured be an average of four one-shot events, as this will further improve the signal-to-noise ratio by minimising the random noise readings.

$$BW_{instr} = 5 \cdot \frac{0.35}{\min(t_r, t_f)} \tag{4.3}$$

4.3.2 PCB Layout

The PCB layout is of critical importance when conducting DPT on GaN HEMT devices. This is owed to their fast switching transitions, which create large voltage and current slew rates, amplifying the effect of any parasitics in the switching circuit.

Initially, the PCBs for double pulse testing were constructed using a lateral power loop layout, which means that the switching currents flow on a circular path on the PCB defined by the path $C_{dec} \rightarrow D \rightarrow DUT \rightarrow R_{sense}$, which can be better understood by referencing Figure 4.9. This comes with the drawback that the power

loop inductance will be quite high [21], slowing down the current transition rates. Nevertheless, this shouldn't be posing a threat to the normal operation of the DUT. However, the author made the catastrophic error of allowing power currents to partly flow with gate currents, in effect creating a Common Source Inductance (CSI).

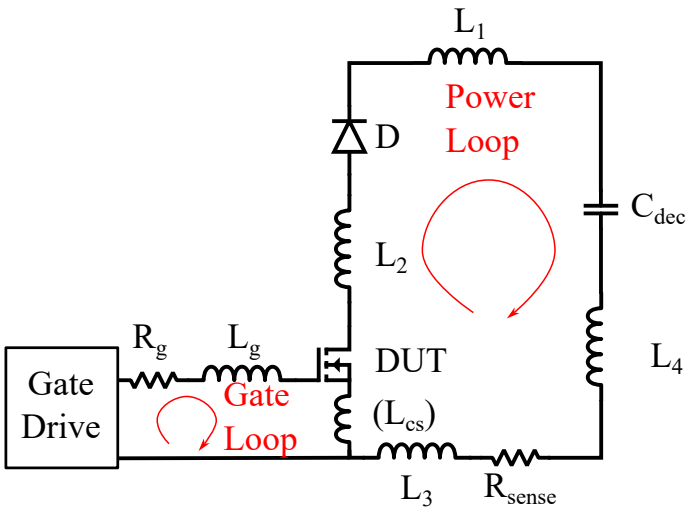
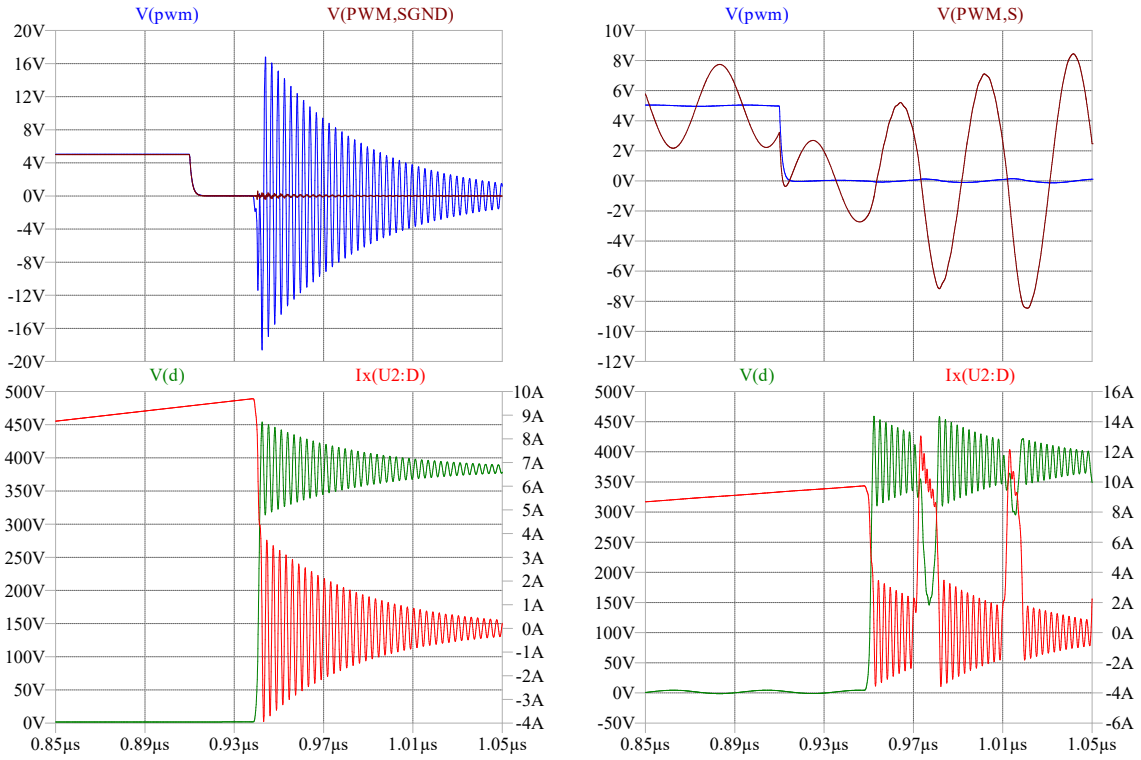


Figure 4.9: The power loop and gate loops of the used half-bridge, with added parasitic inductances.

The reason that a CSI becomes a catastrophic error when performing layout on GaN HEMTs lies once more in the high current slew rates experienced during the device turn-off. When the device is undergoing a hard turn-off event, a voltage oscillation will be triggered in the CSI, which in turn will be seen in the gate driver output loop. With a sufficient slew rate, this oscillation will have an amplitude large enough to create false turn-on events. To showcase this, the simple model of Figure 4.7 was run with two scenarios. In one, a source inductance of $2\,nH$ was added, while the gate driving signals had a direct connection to the DUT, and in another, this $2\,nH$ inductance acted as a CSI.

The simulation graphs shown in Figure 4.10 display in the upper graphs the direct voltage measurement of V_{gs} in burgundy, while in blue is the voltage between the gating signal and the "true ground". It can be seen that the initial voltage spike during turn-off is attenuated successfully in the gate path when there is no CSI; however, it triggers a low-frequency oscillation in the case of CSI. This effect became apparent during lab testing as the turn-off current increased due to the



(a) **(b)**

Figure 4.10: In the first case (a), the added inductance is only in the power loop, and the switching noise is attenuated in the gate loop shown in burgundy colour in the top graph. In the second case (b), the oscillations triggered by the turn-off events create an oscillation on the gate-source path, leading to a series of false turn-ons.

higher turn-off speeds at higher currents. Naturally, the higher gate threshold voltage of the integrated gate drive device means that it exhibits a false turn-on at a higher turn-off current, making it more robust against bad layout practices. An example resulting waveform from this faulty layout may be seen in Figure 4.11, in which the V_{ds}, V_{gs} are displayed, and the false turn-on phenomenon due to CSI may be seen.

Following this error, the next iteration of PCBs took the minimising of the CSI into account. Additionally, there was a focus on also minimising the power loop inductance, based on guidance provided by GaN Systems Inc. [111]. In order to minimise the power loop inductance, a four-layer PCB design was selected to utilise the effect of magnetic self-cancellation between the forward and return current path while providing enough clearance distance for the voltage level studied ($380\,V$). Additionally, to address the matter of the CSI, two techniques were used in the second design to make it as close to zero as possible. First, while the examined

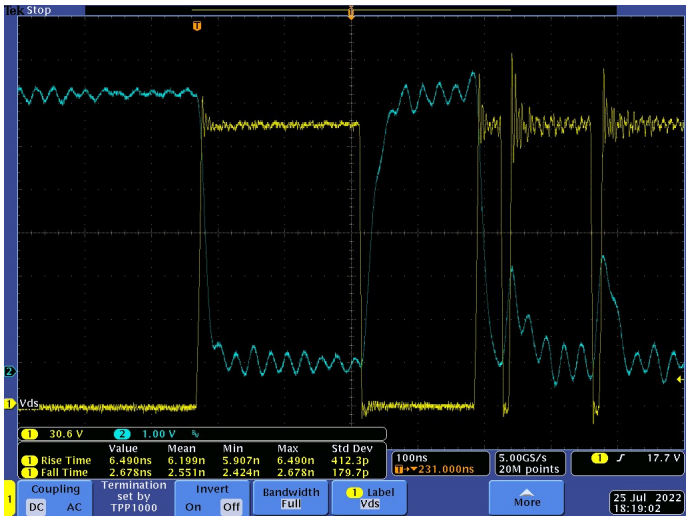


Figure 4.11: Experimental NV6115 false turn-on events, in the first version of the DPT PCB. In blue is the gating signal, bandwidth limited for clarity, while in yellow is the V_{ds}. The threshold voltage for turn-on for the NV6115 device is approximately 2.4 V.

devices don't have a Kelvin Source connection, it is possible to mimic its effects by using the via-in-pad technology. This means that a via is routed in the most "quiet" spot on the source pad of the devices. The electrically quietest spot refers to the fact that the location of this spot has as little power current flowing through it as possible. This way, the physical CSI is reduced. Also, to account for any CSI caused by near-field coupling, the gate driving currents and the power loop currents are routed in a way that allows them to flow orthogonally. This routing, in principle, offers zero mutual inductance between the two traces, eliminating the noise propagation from the power loop path into the gate loop path. These design choices may be seen pictorially in Figure 4.12 and in Appendix A.

4.3.3 Measurement Errors

While conducting this research, two main sources of measurement error are anticipated. First, the high voltage transition rates dV_{ds}/dt created by the DUT have the potential to create Common Mode (CM) currents, which can cause spurious oscillations when acquiring the measurements via the oscilloscope [110]. The second important error comes in the form of the measuring instruments themselves, altering the behaviour of the DUT. This occurs because of the circuit loading caused by the

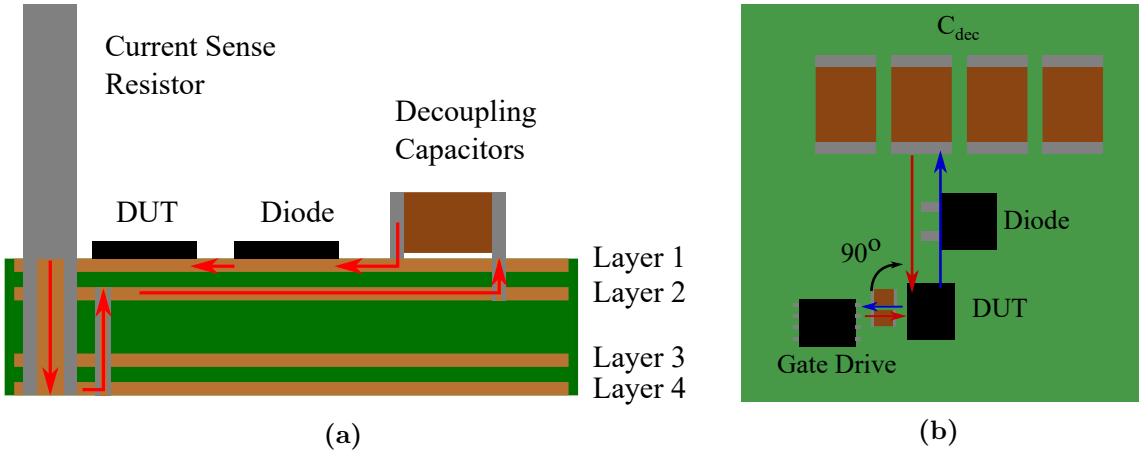


Figure 4.12: The PCB design followed can be seen in these photos. In (a), the design of the power loop current for magnetic cancellation is shown. In (b), the orthogonal design to minimise inductive coupling between power and gating signals is shown.

instruments to be used for voltage and current sensing, which typically slows the switching transitions of the DUT.

Diving deeper into the issue of the CM currents, it is known that they are created by rapid dV_{ds}/dt transitions. These transitions, if allowed, will create displacement currents going into the grounding system. In a test bench setup, there are a plethora of paths for displacement current to circulate. For example, while -most- lab power supplies are isolated, the created CM current is of high frequency and can bypass the galvanic isolation via the transformer's parasitic capacitances. Similarly, the long wires needed to connect the instruments to the PCB might offer another path, as the whole lab bench is grounded for safety reasons. Finally, the main reason why CM currents can be a problem is the connection arrangement of the probes used. The connection can be seen in Figure 4.13, where the common point of the probes is a noisy node between the DUT and the current sensing resistor. Thus, this noise can enter the common power ground by flowing through the oscilloscope.

The choice of this connection is made due to its simplicity, as the values of V_{gs}, V_{ds} are directly measured, while I_{ds} can be acquired by inverting the probe readings. These connections could be made resistant to CM noise by the use of differential or optical probes. However, differential probes tend to have a lower bandwidth. Additionally, optical probes currently are considerably more expensive compared to

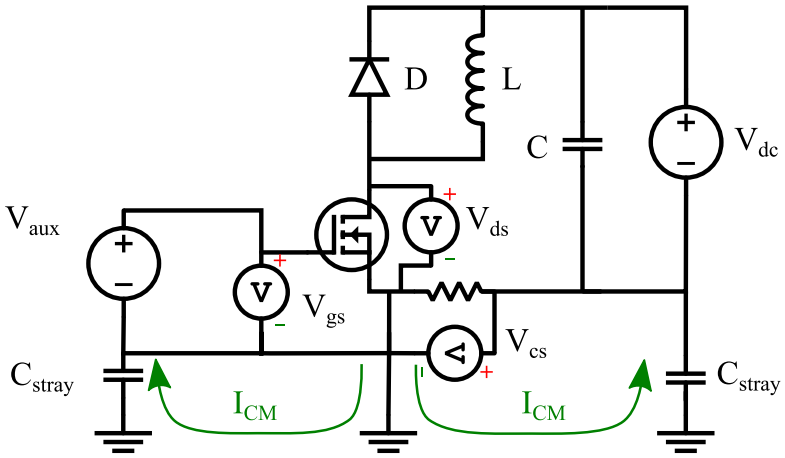


Figure 4.13: In this figure, the creation and circulation paths of CM currents are shown via green arrows.

passive probes. Instead of opting for the much pricier optical probes, it was decided to cut off the CM circulation paths. This was accomplished by various actions taken by the researcher, listed below.

- PCB relays are added to the DC+ and DC- terminals of the DC-Link Power Supply Unit (PSU). They disconnect the PSU prior to the DPT, allowing for sufficient time between the two events to eliminate any transient phenomena.

- Ferrite clamps are used in all probes used in the setup and are selected due to their high impedance to CM signals at high frequencies. It is expected that because they are placed outside of a coaxial cable, this will not affect the differential-mode impedance of the cabling. This is because a differential signal through a coaxial cable produces near zero fields outside its structure, thanks to the outer conductor sleeve.

- The gating signals going to the devices are first passed through an isolator with high Common Mode Transient Immunity (CMTI).

- A Power line filter was used to power the oscilloscope and the auxiliary PSU. This provides a high CM impedance for lower frequency signals in the conducted EMI range ($150\,kHz - 30\,MHz$). Plus, ferrite clamps were also added to the power cable to create a high-impedance path across the whole frequency

spectrum.

The second problem, which is the influence of the measuring instruments on the DUT's performance, is more challenging to negate. The voltage probes add a capacitive load to the probed component, which, in this case, is an extra capacitance imposed upon the drain-source and gate-source pins. The current measuring system increases the power loop inductance in two different ways. The added physical size of the commutation loop is increased to accommodate the connection of the sensing device, and the sensing device also normally has some self-inductance, adding to the total power loop inductance. In this research work, the current sensor's self-inductance was not measured, as its value is low considering its coaxial structure. Therefore, specialised equipment and test setups would be required for an accurate result, which is beyond the scope of this thesis.

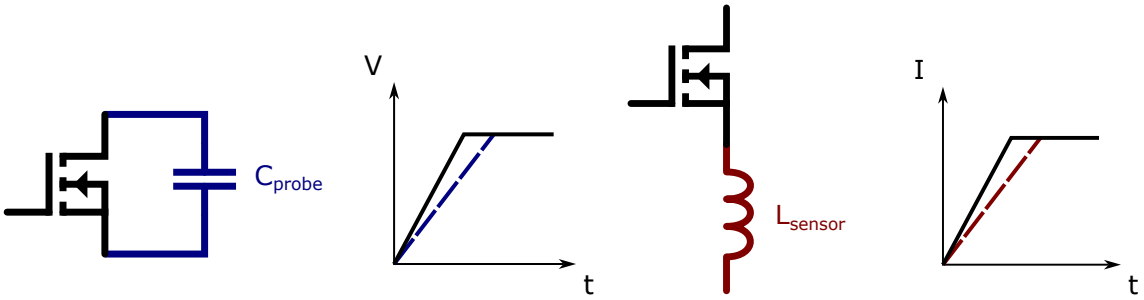


Figure 4.14: Influence of the voltage probe during voltage switching transitions (a), and influence of the current sensor during the current switching transitions (b).

The relative error caused by the effect of the sensors has been quantified by previous research [112],[113]. Based on this existing research, the relative error formulae for the voltage and the current error may be found using equations (4.4), and (4.5) respectively. In these equations $C_{o(ER)}$ represents the energy-equivalent output capacitance of the DUT at the examined voltage level, C_{probe} is the capacitive loading of the DUT by the probe's input capacitance, L_{loop} corresponds to the power loop inductance, without the sensor's influence, and L_{sensor} represents the added inductance due to the insertion of the current sensing instrument.

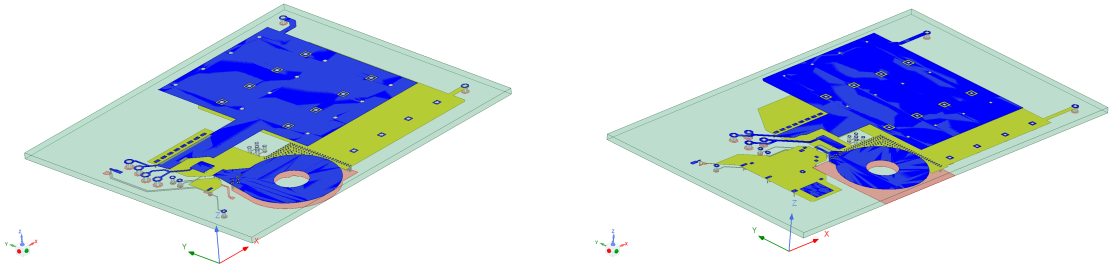
$$\Gamma_C = \frac{1}{\frac{C_{o(ER)}}{C_{probe}} + 1} \tag{4.4}$$

$$\Gamma_L = \frac{1}{\frac{L_{loop}}{L_{sensor}} + 1} \tag{4.5}$$

The values required to solve (4.4) can be easily extracted from available DUT and probe datasheets. This becomes slightly less straightforward when dealing with (4.5), which requires knowledge of the PCB copper parasitic inductance and the individual components' parasitic series inductance to get an accurate result. Due to inherent difficulties measuring low values of inductance using the available instrumentation, the consideration of component self-inductances was omitted in this work. For a possible accuracy extension, the best solution found to measure parasitics on the PCB using the E4990A impedance analyser is using the 42941A probing test fixture [114], which could include the component parasitics as well. In this work, only copper pour inductances are considered.

The copper pour series inductances can be found in a straightforward manner using ANSYS Q3D extractor. To facilitate the creation of the models, the designed PCBs in Altium Designer were exported to ".edb" files, which are able to get imported into the ANSYS Electronics Desktop environment while maintaining the correct geometry and material properties. Naturally, the layer stack-up used in Altium was the one given by the PCB manufacturer. The result of these importing actions can be seen in Figure 4.15.

Using the Q3D extractor AC RL solver, the inductance matrix for the different power loops may be computed. The simulation frequency was kept at the default value of $100\,MHz$, as for the 1 Oz copper boards that were ordered, this value is high enough to give results away from the transition region of the DC-AC signals. The trace self-inductance is numbered similarly to Figure 4.9, with the trace self-inductance noted as L_{ii} while the mutual inductance between traces is noted as L_{ij}. The total inductance matrix retrieved by the simulation software appears in the form



(a) **(b)**

Figure 4.15: DPT PCBs imported into the AEDT environment via their .edb files. Shown in (a) is the GS66502B PCB, and in (b) the NV6115 PCB design.

of (4.6), and the results for all the simulations ran are in Table 4.1.

$$\begin{bmatrix} L_{11} & L_{12} & L_{13} & L_{14} \\ L_{21} & L_{22} & L_{23} & L_{24} \\ L_{31} & L_{32} & L_{33} & L_{34} \\ L_{41} & L_{42} & L_{43} & L_{44} \end{bmatrix} \tag{4.6}$$

Table 4.1: Inductance matrices of NV6115 and GS66502B DPT boards.

	Version 1 (nH)	**Version 2 (nH)**
GS66502B PCB	$\begin{bmatrix} 2.30 & 0.08 & -0.16 & 0.09 \\ 0.08 & 1.40 & -0.11 & 0.00 \\ -0.16 & -0.11 & 4.04 & -0.46 \\ 0.09 & 0.00 & -0.46 & 1.29 \end{bmatrix}$	$\begin{bmatrix} 0.22 & 0.01 & 0.00 & -0.21 \\ 0.01 & 0.87 & 0.07 & -0.97 \\ 0.00 & 0.07 & 1.78 & -1.11 \\ -0.21 & -0.97 & -1.11 & 3.79 \end{bmatrix}$
NV6115 PCB	$\begin{bmatrix} 3.63 & 0.11 & -0.19 & 0.03 \\ 0.11 & 1.46 & -0.03 & -0.08 \\ -0.19 & -0.03 & 5.22 & -0.30 \\ 0.03 & -0.08 & -0.30 & 1.36 \end{bmatrix}$	$\begin{bmatrix} 0.54 & 0.03 & 0.01 & -0.63 \\ 0.03 & 1.19 & 0.03 & -0.81 \\ 0.01 & 0.03 & 1.16 & -0.30 \\ -0.63 & -0.81 & -0.30 & 2.54 \end{bmatrix}$

To extract the total power loop inductance, the "JoinSeriesMatrix" setup was used, which basically performs the calculation shown in (4.7), because $L_{ij} = L_{ji}$ as there are no magnetic saturation effects in air. The power loop inductance for the two different PCBs used to test the devices may be seen in Table 4.2. From this table, it can be appreciated that the magnetic cancellation layout has had a sizeable impact on the total loop inductance. It can also be seen that while the power loop inductances are dissimilar in the first PCB attempt, in the second iteration, they

managed to be close to being equal.

$$L_{loop} = L_{11} + L_{22} + L_{33} + L_{44} + 2 \cdot (L_{12} + L_{13} + L_{14} + L_{23} + L_{24} + L_{34}) \quad (4.7)$$

Table 4.2: Power loop inductances of the constructed DPT PCBs.

	Version 1	**Version 2**
GS66502B PCB	$L_{loop} = 7.89\,nH$	$L_{loop} = 2.26\,nH$
NV6115 PCB	$L_{loop} = 10.76\,nH$	$L_{loop} = 2.08\,nH$

Finally, it has been confirmed that the two PCBs have a similar power loop inductance and that it is quite small in value. To compute the relative measurement errors related to the effects of the measuring equipment used, Q3D AC RL simulations were run without the impact of the current sensing resistor. This was accomplished by connecting the DUT's source with the ground directly with vias from the footprint of its source pad. This would be the ideal switching cell case if the need for a sensing resistor were gone. The retrieved power loops, are $L_{loop} = 1.67\,nH$ and $L_{loop} = 1.52\,nH$, for the GaNSystems and Navitas boards, respectively. Now, utilising the equations from Sprunck et al. (4.4), (4.5), it is possible to show the relative errors created by our measurement tools.

Table 4.3: Calculated Measurement Errors

	Voltage Error	**Current Error**
GaN Systems PCB	12.9%	26.1%
Navitas PCB	13.5%	26.9%

The computed measurement relative errors are displayed in Table 4.3, and it is found that there's considerable voltage and current error. However, the measurement errors between the two different PCBs are similar, therefore it is possible to proceed with the testing, as any performance difference owed to the DUT, will be visible. These high errors indicate that the viewed switching transitions will be slower compared to their "real" values. This is an indication that the devices will perform better within a converter environment, where there might not be any sensing equipment connected in the switching loop.

4.3.4 Test Results

The double pulse setup was set up in the lab environment, and DPT was carried out. The test setup may be seen in Figure 4.16, which shows the exact configuration used during the conducted tests, and Figure 4.17 shows an example waveform as appears on the oscilloscope. Data was acquired from the oscilloscope and passed into the MATLAB environment for post-processing. The main equipment used is summed up in Table 4.4.

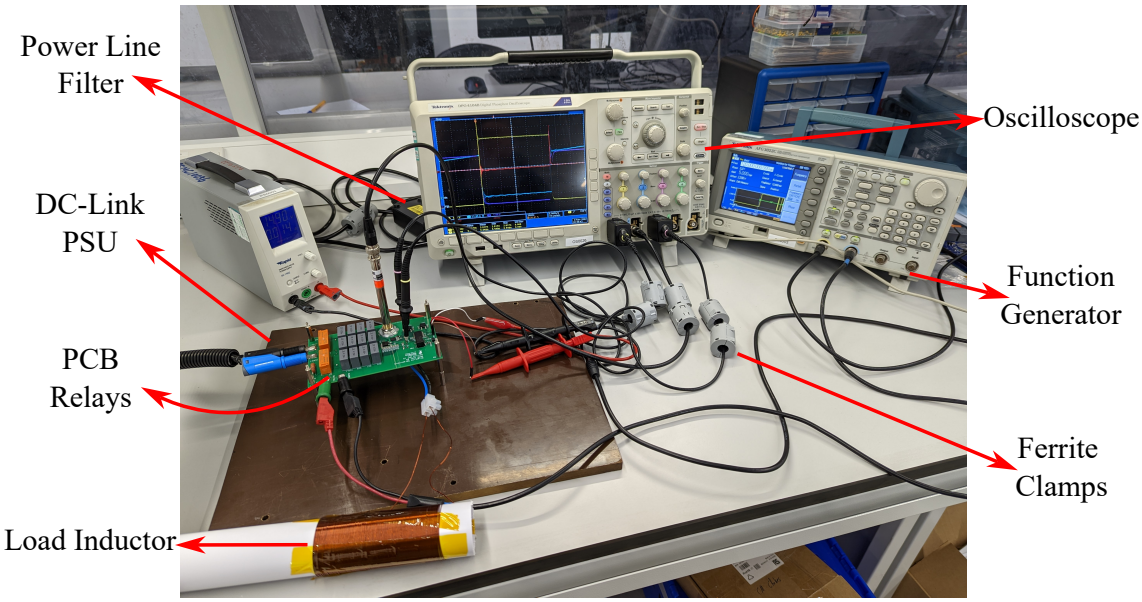


Figure 4.16: The used DPT test bench setup.

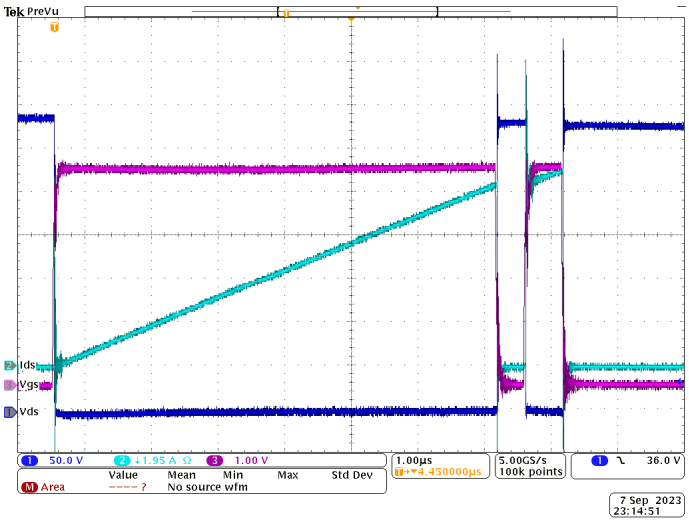


Figure 4.17: Example DPT waveform, seen on the DPO4104 oscilloscope.

Table 4.4: Test Bench Equipment & Devices

Passive Probes	TPP1000
Current Sense Resistor	SSDN-50
Oscilloscope	DPO4101B
DUT	NV6115/GS66502B
Gate Drive	Integrated/ADUM4121ARIZ
PWM Isolation	ISO7820DW/ADUM4121ARIZ
High-Side Diode	C3D02060E
PCB Relays	RY611005
Ferrite Clamps	ZCAT3035-1330

One of the most fundamental aspects of an accurate DPT is waveform deskewing. Measured waveforms from the PCB have different propagation delays, which can be caused by the difference in the probe type, the measuring sensor, the type of cable, the measurement voltage range, or simply a difference in cable length. It is of utmost importance to have time-aligned voltage and current waveforms in order to measure power loss accurately during the switching intervals. This becomes especially true when testing GaN devices, which are extremely fast at switching, and therefore, any time misalignment would cause significant errors [110].

There are various ways to deskew the voltage and current waveforms found in the literature, and manufacturers do sell deskewing fixtures to aid power electronic engineers. However, it isn't within the scope of this work to analyse the different ways one might deskew these waveforms, and the most common method was used, which is the alignment of waveforms based on known V-I relations of the GaN HEMT [110, 115, 116].

It is well-known that during the turn-on intervals for diode-clamped GaN HEMTs, the load current must commutate first before the voltage is rapidly reduced. During this short interval, a slight voltage dip is observed in the V_{ds}, caused by the device parasitic inductance and the rapid current level change. Based on this, one might deskew the waveforms in order to align the beginning of the current slope rise with the voltage dip on the V_{ds}, as is recommended in [110, 115]. Another well-known V-I alignment method is utilising the device turn-off instance. During turn-off, a V_{ds} overshoot is expected, and this occurs at the same time that I_{ds} experiences

its first zero crossing [117], as after the zero crossing, voltage owed to the parasitic inductances will switch polarity, and start decreasing the voltage measured at the drain to source of the DUT.

Based on the experience of conducting the DPT on these devices, both methods delivered similar deskewing timing recommendations. However, the second method, which aligns the waveforms based on the turn-off switching events, was preferred. This recommendation is based on two reasons, the first one being that devices with low parasitic inductances, such as the ones examined in this paper, have a small V_{ds} dip during low turn-on currents. This makes aligning the V-I waveforms quite challenging. One might align the waveforms with a high current level, as recommended in [115], but keeping the timing delays on the oscilloscope channels constant whilst changing the measuring range of the channel to ensure high ADC accuracy might lead to wrong readings. However, the V_{ds} peak and the current zero crossing are easy to identify within the whole load range, ensuring correct time alignment across the entire load range. The second reason is that if one desires to create a fully automatic DPT rig with corresponding data acquisition and post-processing, detecting a signal's peaks and zero crossings is quite simple, using MATLAB's signal processing toolbox. Trying to do this based on the turn-on instances would be more challenging, particularly in the low current tests.

After the deskewing procedures, the data was transferred to the MATLAB environment, and the instantaneous power loss curves were computed. An example of the waveform behaviour retrieved may be seen in Figure 4.18. After calculating the device's instantaneous loss for the switching intervals, numerical integration is performed on the data. To do this, integration limits must be set and kept constant for consistency of the results. In this work, the integration limits were set as follows:

- Turn-on transitions
  - Start at 2% of the load current.
  - End at 5% of the DC bus voltage.

- Turn-off transitions
  - Start at 1% of the DC bus voltage.
  - End at 2% of the load current.

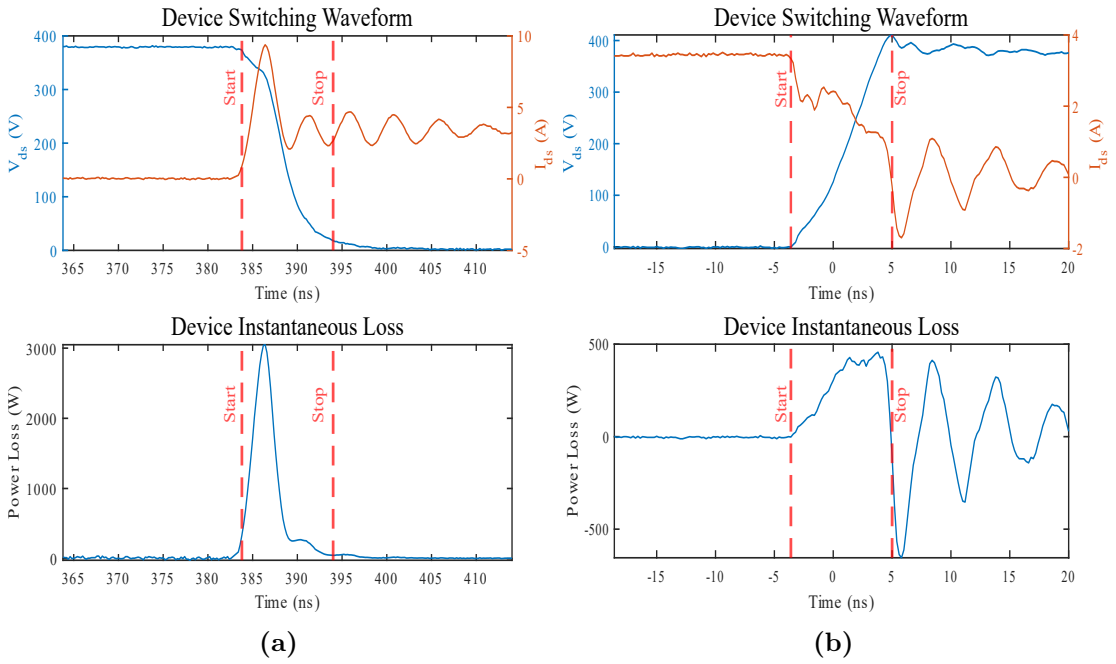


Figure 4.18: An example of the waveforms retrieved from DPT. In (a), a turn-on instance is seen, and in (b), a turn-off instance is displayed.

To create the graphs of the DPT results, two MATLAB scripts were used that can be found in Appendix B. Various metrics were evaluated, such as the switching energy loss, the switching transition times, and the voltage overshoots during the hard turn-off events. Concerning the turn-on losses, some benefit was seen on the NV6115 device, as it displayed slightly lower energy dissipation, as seen in Figure 4.19. The turn-on switching time is defined as the time taken by the V_{ds} on the device terminals to transition from 95% to 5% of the testing voltage. The results for the turn-on switching times are seen in Figure 4.20 and show that NV6115 typically turns on faster than GS66502B, which is consistent with the power loss measurements.

Moving forward with the turn-off energy dissipation, almost zero divergences were observed, as can be seen in Figure 4.21. The two devices have very low turn-off energy dissipation and are nearly identical in value to each other. Also, it might be observed that the turn-off loss is nearly constant throughout the whole load

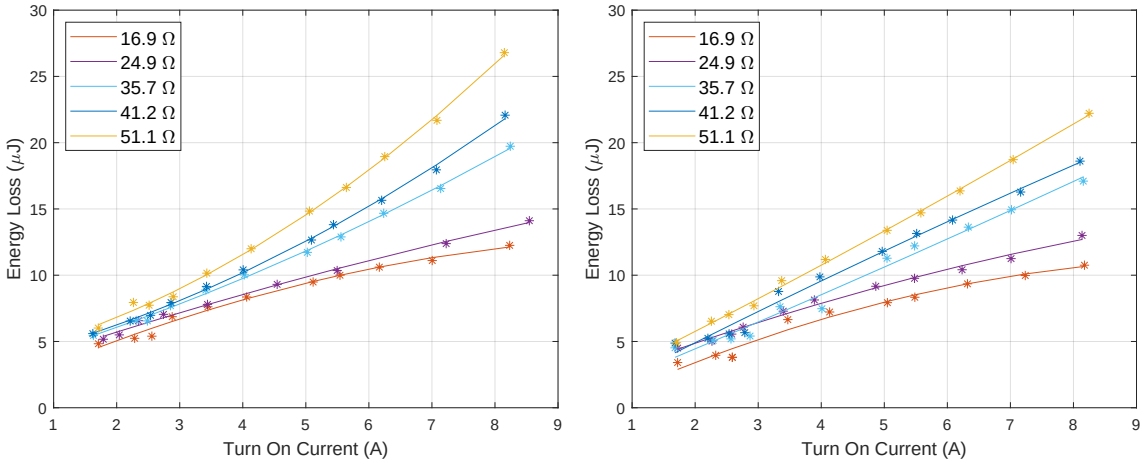


Figure 4.19: Turn-on losses for a variety of turn-on resistors and different turn-on currents. On the left (a) are the data retrieved by testing the GS66502B device, and on the right (b) is the NV6115 device.

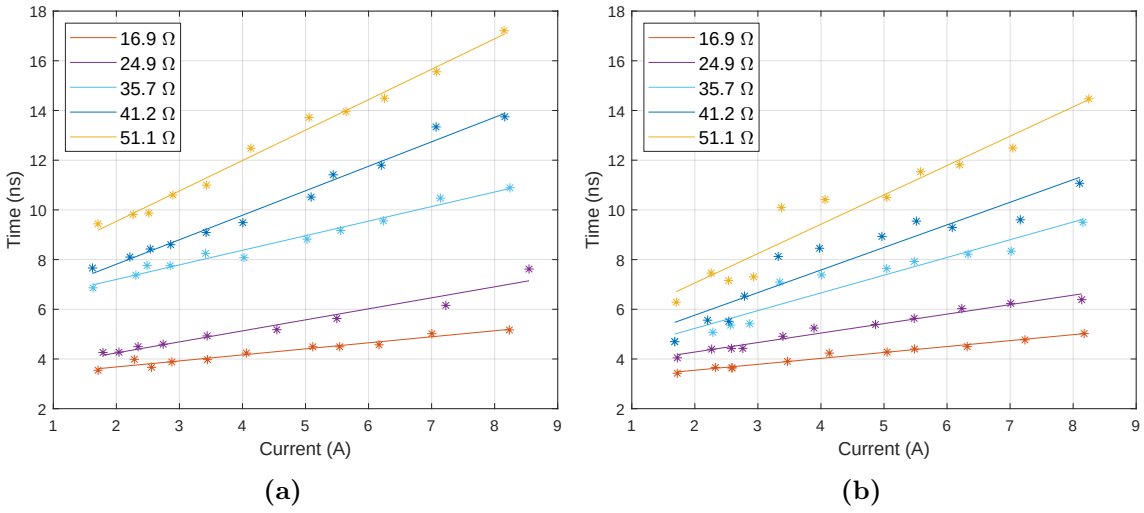


Figure 4.20: Turn-on switching speed for the GS66502B device (a), and the NV6115 device (b).

range. This may be explained as an effect of the energy stored in the equivalent output capacitance C_{oss} getting discharged increasingly faster with the load current, combined with the low intrinsic junction capacitances of these devices.

The very low intrinsic junction capacitances, along with the discharge of C_{oss} being helped by the load current, allow for extremely fast switching transitions during the turn-off events. The speed of the transition, which is defined as the time difference between 95% and 5% of V_{dc} can be seen pictorially in Figure 4.22a, and it is seen that at the rated current the turn-off event lasts approximately 2 ns. The fact that this transition is slowed down due to the voltage probe capacitive load means

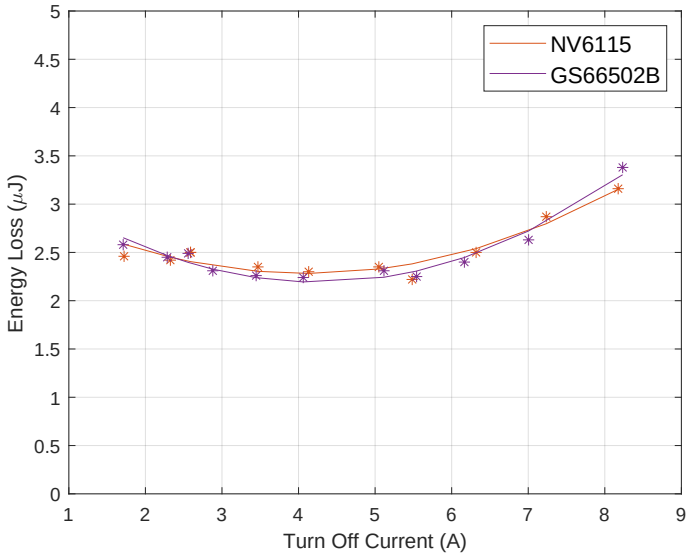
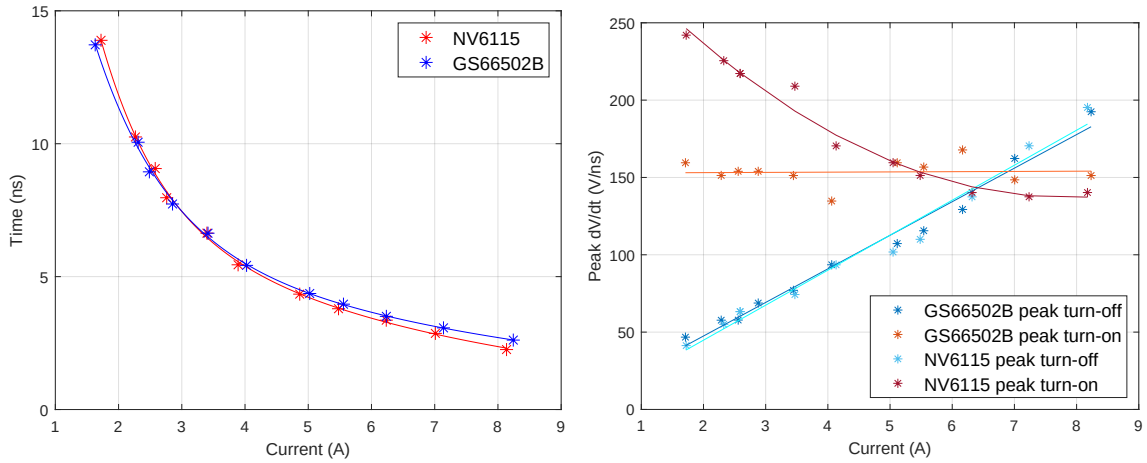


Figure 4.21: Measured turn-off energy dissipation for both GaN HEMT devices.

that the devices likely switch faster than that when they're not under measurement. Also, a good curve fit for the voltage rise times was achieved by using the two-term power curve fitting included in MATLAB.



(a) **(b)**

Figure 4.22: Voltage rise times as measured during DPT (a), and peak voltage transition rates detected during switching events (b).

Moving forward, the instantaneous voltage slew rates were measured to see the scale of the dV/dt that the designer will have to contend with. The results are shown in Figure 4.22b, and it can be seen that most transitions have dV/dt peaks of over $100\,V/ns$, which is a typically high CMTI offered by instruments. Nevertheless, no issue with false firings was experienced despite these transitions in excess of $200\,V/ns$ in some cases. These data points were retrieved by scanning the V_{ds} waveform

one sample at a time and calculating the slew rate of each sample based on its neighbouring samples. Samples were taken every $0.2\,ns$ based on the limitation of the oscilloscope.

Finally, since the device turn-off losses appear to be identical, it was decided to move forward with the use of the NV6115 device for the proposed converter. It displayed more tolerance to layout imperfections, and it takes up little space on the PCB, as the ancillary components needed on board are all small passive components, saving space and design effort compared to a dedicated gate driver. However, the benefits of GS66502B are that the turn-off transition speeds may be reduced with a turn-off resistor, enabling more manoeuvrability when looking into EMI regulation compliance. Also, the proprietary GaNPX packaging found in GS66502B provides a smaller junction to ambient thermal resistance compared to NV6115; however, more recent Navitas devices have improved in this aspect.

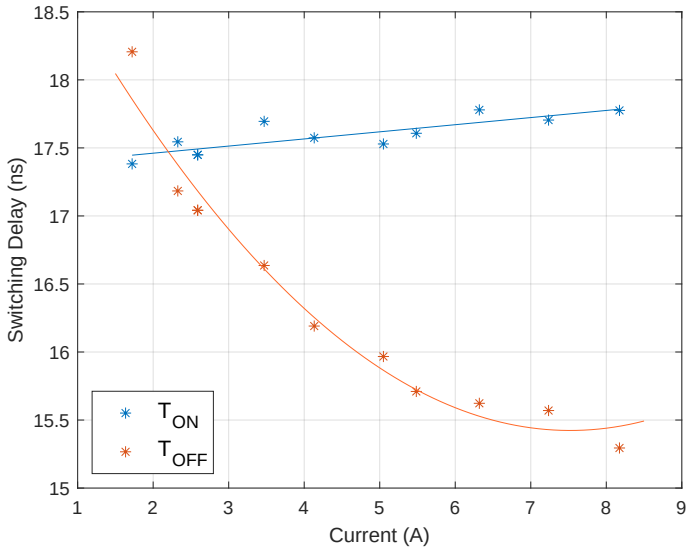


Figure 4.23: Switching time delay as captured by TPP1000 probes in DPT. The logic pin has an RC filter of $100\,\Omega$ and $100\,pF$ attached to prevent ground bounce.

Another concern that arose in the use of NV6115 was the timing delay between the logic input of the device and the actual switching action. Switching actions correspond to different V_{gs} levels in GaN HEMTs; however, seeing this device is monolithically integrated, this is impossible to measure/probe. Also, the manufacturer-provided time delay data doesn't include an RC filter at the PWM input [118], which is

useful to prevent false turn-on from ground bounce when having a shunt resistor in the source pin's path. The time delay data is of critical importance when dealing with high-frequency conversion, seeing that a small unexpected timing delay of $1\,ns$, for example, accounts for 0.1% of the full switching period when designing a $1\,MHz$ converter. Therefore, an unforeseen turn-on delay can allow third quadrant conduction for a relatively large part of the converter's switching period, deteriorating efficiency significantly.

For this reason, the timing delay data was captured and is displayed in Figure 4.23. In this figure, the time delay is quantified in the same manner as found in the device datasheet [118]. This means that the turn-on delay is defined by the time between the mid-point crossing of V_{pwm} and the crossing at 90% of the V_{ds}. Similarly, the turn-off time delay is the time between the 50% crossing of V_{pwm} and 10% of V_{ds}. Upon inspecting Figure 4.23, it is seen that the time delays are larger compared to the values given by the datasheet, which is expected as there is the addition of the RC filter in the DUT's logic pin. Additionally, it is seen that the turn-on delay is relatively constant throughout the whole load range, which is desirable as this makes the dead-time design simpler, as it may be kept constant without a significant efficiency penalty. Some extra leeway will be required due to the temperature dependency in the dead-time design, but the delay time increase concerning the device temperature is provided within the datasheet.

4.3.5 Discussion on Further Future Improvements

Two main aspects would be very beneficial to improve in this chapter; however, they weren't pursued due to the PhD time constraints. Both of these improvements are focused on current sensing; one concerns the impact of the added current sensor, and the second concerns the impact of the layout on the current signal acquisition. The missed opportunities for better DPT realisation are laid out in the sections below and constitute planned improvements that will be implemented in future work.

Current sensing technologies

It has been analysed in section 4.3.3 that any voltage or current sensing system will influence the DPT switching circuit. For current sensing, coaxial shunt resistors tend to be the first choice for engineers and researchers due to their high bandwidth, precise calibration and inherent shielding, making them an attractive and easy-to-use tool for current sensing. However, while conducting this work, the author found out that they are an inadequate tool in the DPT of GaN devices if a high degree of precision is required on the switching loss characterisation. The proof for this statement may be witnessed in Table 4.3, wherein the current relative error due to the shunt insertion is severe.

This problem arises partly due to the packaging normally used for GaN HEMTs. They typically come as SMD components with a small PCB footprint, which in itself is a desirable property. This allows for small commutation loops with a low power loop inductance, typically in the $1-2\,nH$ range, in which any insertion inductance of the sensor will cause high errors according to equation 4.5. Naturally, researchers are looking into the best compromise between the different sensing techniques as a trade-off between bandwidth and insertion inductance [119, 120]. Usually, it is found that small package SMD resistors in parallel are the ideal compromise. Additionally, recently, it has been reported that the coaxial shunt resistors actually have a significant self-inductance [121], which would make the error figures even higher than those reported in this work, while also increasing the current ringing oscillation as seen on the oscilloscope. Plus they have shown to possess a lower bandwidth compared to their rated value as sold [122]. Therefore, this leads to the conclusion that the developed test rig could be significantly improved by changing the current sensing device from the coaxial shunt resistor to an array of small SMD resistors.

Impact of PCB Layout on the Current Signal

Another aspect of the DPT measurements is the impact of the layout. Based on the previous discussions, the effects of the parasitic inductances and inductive couplings have been well understood. However, the parasitic capacitances found within the DPT rig also affect the measured values. One side of the equation is the extra energy that gets charged/discharged within the dielectrics of the PCB, which has been analysed thoroughly in [123]. Another side of the parasitic capacitance effects has not been investigated in the literature, at least to the author's current knowledge.

This problem finds itself in the individual stages of a GaN HEMT commutation event. The PCB parasitic capacitances offer a low impedance path during the switching transients, which enables the current to circumvent the path defined by the DUT. This appears as a current deformation in the current signal, as seen on the oscilloscope. In fast enough transitions, i.e. high turn-off currents, the turn-off transition appears to be unaligned compared to the voltage waveform. To better understand this seemingly bizarre phenomenon, a rough outline of a GaN HEMT's turn-off switching transient will be shortly presented. The main events during a DUT turn-off may be summed up as follows.

1. The gate driver pulls its output voltage voltage to $0\,V$. This, in turn, discharges the input capacitance of the device, lowering the V_{gs}. This stage is commonly referred to as the delay time between the gating command and the actual switching transition. The ending of this period depends on the threshold voltage of the DUT, as well as the load current that is to be commutated and the DUT's transconductance curves. Numerically, the endpoint of this period is expressed in the equation below, after which the main switching event takes place.

$$V_{gs} = V_{th} + \frac{I_L}{g_{fs}} \tag{4.8}$$

2. During the initial switching period, the DUT's channel current decreases

according to the V_{gs} value and the transconductance. However, as the GaN HEMTs have a low input capacitance, the current drop observed in measurement will be much slower, as the power loop inductances will slow the transition down. The difference between the observed current and the channel current will commence charging the C_{oss} of the DUT.

3. Once the V_{gs} crosses the DUT's threshold voltage, the channel's current will rapidly drop to zero. If the upper-side device is allowed to commutate (in this test rig, this would mean a positive voltage bias on the diode), the current is rapidly commutated and shows ringing centred at zero. If the upper-side device isn't conductive yet, the current will be flowing in the output capacitances of the two devices in a decreasing fashion, as seen by the DUT.

4. At the end of the switching transition, the upper device conducts the load current. An oscillation is seen on the DUT's terminals, the frequency of which is determined by the power loop inductance and the device output capacitance.

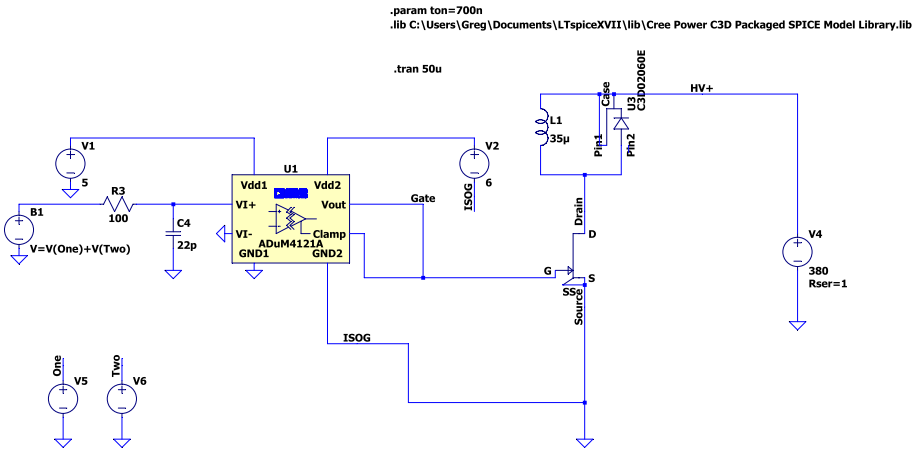


Figure 4.24: DPT idealised setup on LTSpice, using the GS66502B device.

To further display this switching behaviour, a DPT simulation was run in LTSpice featuring the GS66502B device, for which the schematic may be seen in Figure 4.24. The same gate driver drove the signals used in the DPT test rig, as seen in Table 4.4. The turn-off waveforms can be inspected in Figure 4.25, with the different states described previously being visible and marked with horizontal lines. While looking

at this turn-off waveform, one can notice that high dv/dt are created on the V_{ds} of the DUT while most of the load current is still flowing through the DUT.

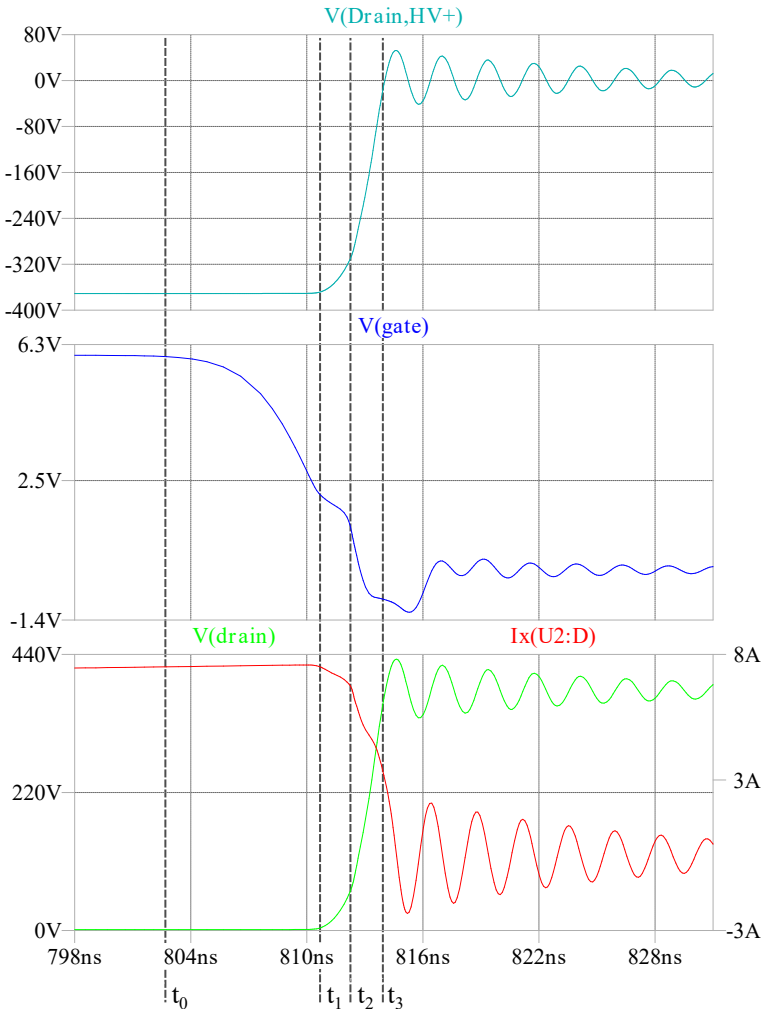


Figure 4.25: The different stages during a GaN HEMT turn-off transition.

Focusing on the PCB layout used, magnetic cancellation was used to route the forward and return current traces. This technique is widely recommended by manufacturers [111], and offers a low power loop inductance solution which can help with dampening the turn-off voltage overshoot, as well as any false triggering effects. However, it does provide a direct connection of the drain node to the ground via the PCB stray capacitance. The value of this capacitance is non-negligible for the layout used and would likely have a significant effect even if a vertical power loop layout is used. This added coupling has caused the creation of current signals that are inaccurate, which can be quickly inspected upon looking at the turn-off transition acquired in Figure 4.18b. Unfortunately, this means that the turn-off energy loss

data retrieved are not accurate, and more research is needed to create a better DPT rig for GaN HEMTs. The turn-on waveforms do not suffer from this effect, as they tend to be considerably slower, and the load current is commutated first before any significant dV_{ds}/dt occurs. Nevertheless, based on the error formulae provided in equations (4.4), (4.5), it seems that for low current rated GaN HEMTs, an accurate characterisation based on the DPT method is currently impossible, with the existing instrumentation. Their junction capacitances are considerably low, enough to create a significant error with even the bleeding edge of available instrumentation [124], while their small packages create very small loop inductances that are also of the same magnitude as the state-of-the-art current sensor insertion inductance [120].

4.4 Summary

This chapter aimed to characterise key performance metrics for the GaN transistors to be used in the proposed power converter. Initially, a test setup was used to confirm the output capacitance values of the low voltage, high current devices to be used in the primary side of the converter. The measurements showed good agreement with the manufacturer-provided datasheet, which indicates that the ZVS behaviour of the converter can be achieved. Next, a DPT rig was set up to examine the turn-off losses of the devices on the high-voltage side of the converter. Two devices were compared to determine if a device with an integrated gate driver had a performance benefit concerning the turn-off transitions. Unfortunately, due to the challenging nature of characterising GaN HEMTs, accurate data wasn't retrieved for the turn-off losses. Still, a fair comparison was made, and it showed that for the turn-off losses, there isn't a performance benefit in using a device with an integrated gate drive.

Chapter 5

Experimental Design & Results

5.1 Introduction

In chapter 3, the converter operation has been verified analytically and via simulation. Furthermore, the behaviour of the GaN devices to be used has been examined in chapter 4. In this chapter, the goal is to present the operation of the converter via experiment. The design challenges faced are presented in the following sections, as well as the results retrieved. In this chapter, a more modest switching frequency is pursued to make wire-wound magnetics a viable choice. With the wire wound magnetics, any design changes can be more easily applied, and it provides a solid basis to develop a slim and high-frequency power converter later.

5.2 Layout of the PCBs & Assembly

For the work in this chapter, the author created three converter prototyping boards. This is due to the malfunctions faced with the first two attempts at creating a working prototype. This section aims to provide an insight into the challenges faced by the designer, despite using resources available in the literature to create a working design, and provides further insight than what is easily available in the relevant literature [21]. The challenges presented here are all derived from the use of the low voltage GaN devices, as the high voltage ones from Navitas are quite robust against layout imperfections, owed to their integrated gate driver, as presented in chapter 4. The first prototype was unsuccessful due to assembly difficulties, while the second attempt was unsuccessful at providing results due to a layout error. Therefore, the reasons for the failure are analysed in the following subsections. Also, the design of the designed boards can be inspected in Appendix C.

5.2.1 GaN HEMT & Gate Driver Assembly

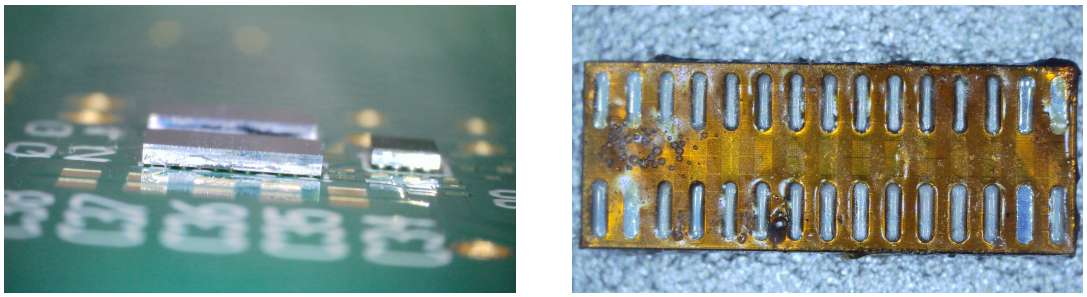
It is expected that designs done within an academic or small enterprise setting will be assembled in-house due to cost concerns. Based on the author's experience, robust in-house assembly of low voltage GaN HEMTs and their associated gate drivers is a considerable challenge on its own. At the same time, there are a lot of resources on GaN HEMT assembly in the form of application notes. Still, they typically concern fabrication houses, and the equipment needed is not normally found in university labs or SMEs. As mentioned at the beginning of this section, considerable challenges faced in the first design iterations rendered the first converter prototype ineffective. In this section, the assembly challenges will be divided into two key parts, which are the errors made assembling the GaN HEMTs and the associated gate drive. Advice is then provided to potential future power electronic designers to enable faster prototyping.

GaN HEMT Assembly

The component used for the low voltage side of the converter is EPC2021 from Efficient Power Conversion Corporation (EPC). It comes in a passivated die package with a Land-Grid-Array (LGA) soldering pattern comprising 30 pads arranged in a 2x15 matrix. The pad widths, as well as the spacing between pads, is approximately 0.2 mm. Obviously, this is a challenging task based on the solder bump dimensions. Using the available assembly advice from EPC, a 0.1 mm thick stencil was ordered, which has been electropolished to allow better precision on the stencil opening design.

Using the ordered stencil, proper solder paste deposition proved to be a big challenge. Naturally, a type 5 paste was used to provide the best ability to flow in small openings. However, using the basic stencil printer found within the PEMC group and with various attempts to use the stencil manually, proper solder deposition was rarely achieved. The author believes this is due to the inability to get a completely flat attachment of the stencil to the PCB without using advanced stencil printers based on vacuum technology. In the infrequent successes at correct solder deposition, the paste spreading during the reflow process made solder bridges or solder balls that either made the transistor short-circuit or violated the clearance distances and created the destruction of the transistor when using it with the nominal voltages. It was also difficult to assess the quality of the assembly that was undertaken by visual inspection. For reference, in Figure 5.1, an apparent well-soldered EPC2021 device that was destroyed in tests is shown. When removed, it was seen that some paste was actually attached to the package, rendering it unable to be used at its nominal voltage ranges.

Finally, after an unsuccessful soldering attempt, reusing the same PCB proved difficult. To create good joints with BGA and LGA components, a flat surface is required. Attempts to re-flatten the footprints proved difficult, as the surrounding solder-resist material was getting worn out. The solder resist layer is critical for correct voltage clearance and solder bump formation. Therefore, the ordered PCBs had to be discarded.



(a) **(b)**

Figure 5.1: Assembled EPC2021 devices, pictured with a portable electronic microscope, with discernible solder bumps that are not bridging (a), and the EPC2021 after removal, which shows paste residue on the left side of the transistor (b).

Gate Driver Assembly

For the gate driver, the LM5113 from Texas Instruments was used. This is a driving chip directly aimed at low-voltage GaN transistors, and it is sold in two different packages. Initially, the Die Size Ball Grid Array (DSBGA) package was used in an attempt to reduce the probability of excessive ringing on the gate-source waveforms. The size and layout of this package allow for the creation of very compact loops, which limit the creation of stray inductance and, therefore, aid in cleaner V_{gs} waveforms. Nevertheless, assembly problems did arise when following the manufacturer datasheet recommendations.

Within the datasheet, it is recommended that the solder mask openings be designed as "non-solder mask defined". This means that the solder-resist openings are slightly larger than the copper pad. This is a justifiable design choice, as this option allows the solder to connect to the sides of the pads, augmenting the current transferring capacity of the joint and its mechanical robustness. However, following this recommendation, the solder resist material between the pads is a mere 0.15 mm. Once again, this led to unexpected failures of the gate driver, especially when using a hot-air gun for assembly purposes. Therefore, in later design iterations, solder mask-defined pads were used when assembling BGAs, with satisfying results as seen in Figure 5.2, and no issues were encountered in terms of the current handling capability.

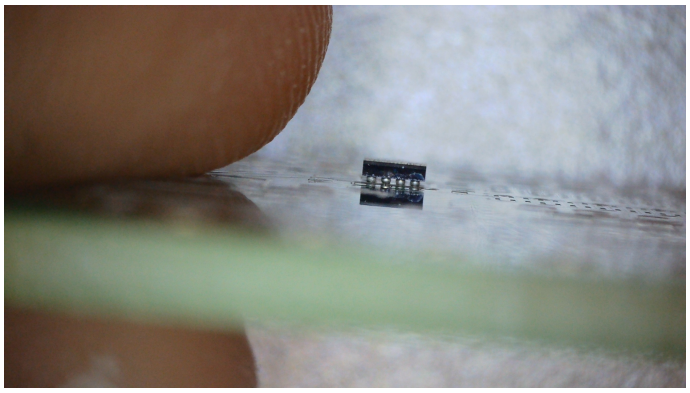


Figure 5.2: Solder mask defined BGA solder.

Assembly Recommendations

The author's assembly experience can be summarised in a few points, which are shown below. The author recommends these assembly actions, which are believed to help accelerate the prototyping phase when a designer is inexperienced in using these components and is required to perform their own PCB assembly.

- It is preferable to use an immersion gold (ENIG) or immersion silver PCB pad finish technology. This ensures a flat soldering surface for any LGA/BGA components, allowing for symmetric solder joints.

- The use of stencils is not advised for the small openings in these devices (0.2 mm or less) unless the designer has access to speciality stencil printing equipment.

- The use of solder mask-defined pads is extremely useful, especially in the case of the assembly via a hot air gun station, where the device is mechanically disturbed to check for reflowed solder.

- An easier assembly became possible from the use of Rosin Mild Activated (RMA) flux, compared with a no-clean one. This type of flux requires cleaning, but it doesn't harm short-term reliability if improperly cleaned.

- The solder balls used in SMD components typically are SnAgCu alloys to allow for RoHS compliance. Generally, their melting point is in the 260° C range. Good results were achieved via a basic reflow oven by heating the PCB

to 270° C for approximately 12 seconds. Using the hot air gun, a wide tip that covers the device is recommended, and good assembly was achieved using temperatures of approximately 340° C with low airflow.

- Tack flux is preferred for two reasons. First, it prevents device movement due to vibrations due to its adhesive nature. Secondly, it is possible to use a basic reflow oven to do dual-sided reflowing. This is achieved by glueing components on their pads with the flux and positioning them in a reflow oven with stand-offs.

5.2.2 Low Voltage GaN HEMT Layout

As mentioned previously, layout-related issues were faced in the performance of the EPC2021 component. In the second iteration of the prototype, a vertical power loop layout was used [21], and the gate drive was routed closely to the devices, with return current polygons on the adjacent layers, to provide a low inductance gate-source path. Despite this, voltage spikes were seen in the measured V_{ds}, which sometimes led to false turn-on events and, thus, device failure. This voltage spike appeared when the complementary device in a half-bridge was switched on after the dead time had elapsed. Typically, it is assumed that the miller capacitance causes this [125] -and indeed, sometimes it is- but this thesis will show that it might be owed to parasitic inductance effects.

In order to prove that the voltage spike seen in the V_{gs} isn't necessarily owed to the rate of change of voltage on the devices' drain pin, the operational waveforms will be examined using different turn-on resistors. During a device turn-on interval, the current first gets commutated before the voltage transition of the V_{ds} takes place, as the voltage is clamped to a specific value by the complimentary device that is conducting. The rate of change of current during device turn-on is mostly dependent on the power loop inductance and, to a smaller degree, on the gate turn-on resistor. Therefore, to test this theory, the converter was run with no output load and a 35V input voltage. This means that in the primary bridge, only a magnetising current of

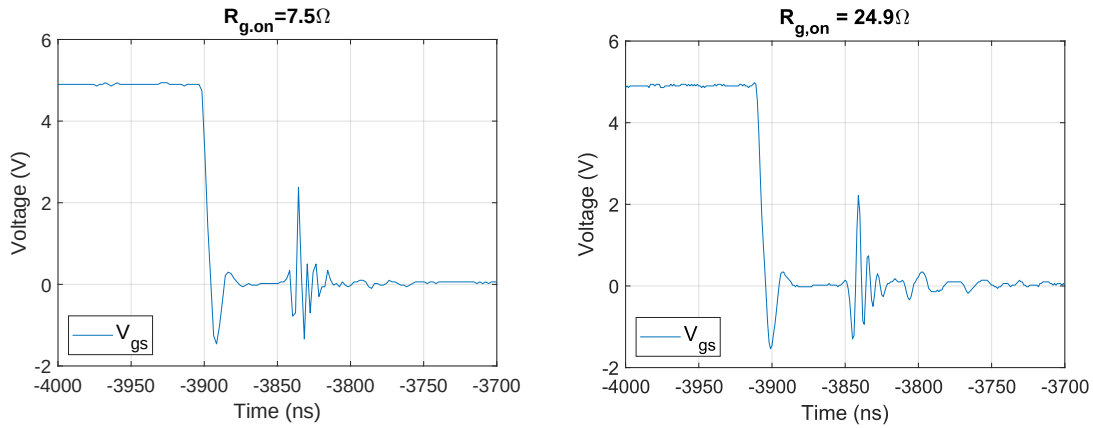


Figure 5.3: V_{gs} spike possibly owed to di/dt effects. It can be seen that even with a dramatic increase in gate driver turn-on resistance, the voltage spike amplitude and waveform persist.

equal value is flowing for both tests. It can be seen in Figure 5.3 that slowing any V_{ds} transients by an increase in the device turn-on resistor has zero effect. An attempt to increase the turn-off resistors was impossible, as a pad for turn-off resistors wasn't routed in this PCB prototype.

To avoid the appearance of this voltage spike, the mechanism behind it needs to be identified and addressed. This is behaviour typical of the existence of Common Source Inductance (CSI) between the power and driving loops, as analysed in the previous chapter. It may be seen in Figure 5.4, that in the second iteration the same vias that route the power current are used in the gate return path. Initially, during the design phase, it was thought that this would cause no problems, seeing that it is a mere 0.2 mm shared path between power and driving loops. Nevertheless, it appears to have caused serious problems with the driving stability. In the second iteration, seen in Figure 5.4 on the right side, dedicated vias transfer the gate return current directly from the nearest source pad on the top layer. Also, polygon cutouts were used to ensure that power currents wouldn't be flowing in the same areas as gate-driving currents. Using the revised layout, zero switching defects were faced in the third -and final- iteration of the converter.

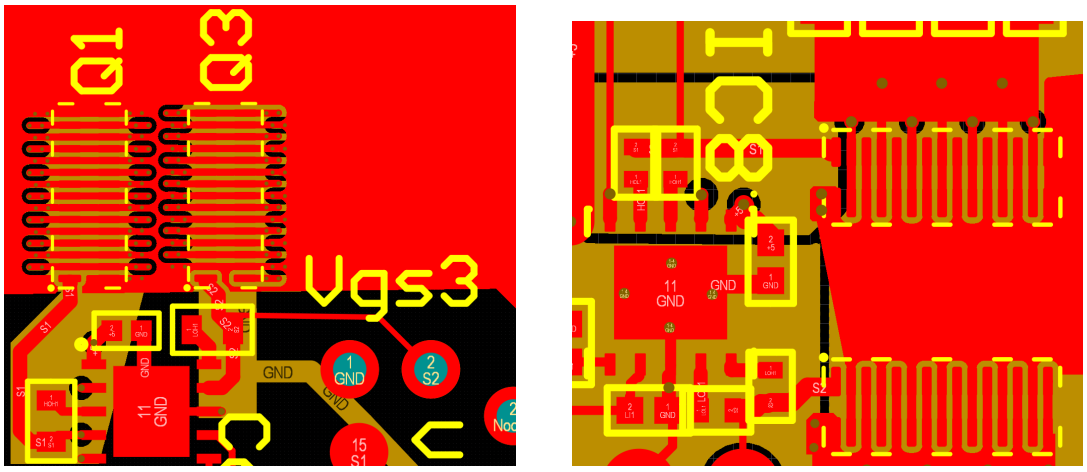


Figure 5.4: Gate drive design change from the second (left) to the third (right) built prototype. In the third iteration, the gate drive current path gets isolated from the power currents on the top layer instead of the mid-layer.

5.3 Experimental Setup

The assembled converter board can be seen in Figure 5.5. After the complete assembly and verification of proper operation of the individual components, the LC resonant tank needs to be tuned. The resonant inductance comprises the transformer's leakage inductance, as seen from the high-voltage side, plus the designed resonant inductor. The resonant capacitors are placed in parallel to allow for the combination of different values and enable fine-tuning of the resulting series capacitance value. It is critical for the effective operation of the converter that high-quality class 1 capacitors are used here, with the ideal case being C0G(NP0) capacitors. This capacitor type allows for the least capacitance change when temperature changes are present, plus it has a fairly constant capacitance rating for different load voltages. This is a crucial property, as most capacitors experience decreased capacitance with an applied voltage bias. This would lead to a notable shift in the LC tank resonant frequency and, therefore, reduce the operating efficiency considerably.

The end result for the total resonant inductance is 61.9 μH, and for the resonant capacitor, it's valued at 28.8 nF. The resonant inductance owed to the transformer was measured using the E4990A Keysight impedance analyser by performing a short-circuit test, and the same instrument was used to measure the inductor's inductance at the frequency of interest. The capacitance value was confirmed by measurements

Figure 5.5: The converter PCB under testing.

using a digital multimeter on the PCB to confirm that the stated values of the capacitors used were correct. It may be noted that the resulting resonance frequency of the applied LC tank is a mere 120 kHz, while the switching frequency was altered to 135 kHz to achieve current conduction for the maximum possible time period, during full load in DCX mode. In the theoretical analysis of the converter, these two frequencies should be close to each other, but in practice, the superposition of the magnetising current of the transformer with the load current shifts the needed LC tank resonant frequency compared to the switching frequency.

To evaluate the efficiency and the potential of the converter to step up an input DC voltage, four multimeters were initially used, each measuring either a DC voltage or a DC current. The results were logged in a notebook, and it was found that when creating the efficiency curves of the converter, the graphs had some random errors, likely due to the digitisation errors and the timing mismatch of acquisition by hand. Therefore, a precision power analyser was used, specifically the PPA5530 sold by "Newtons4th Ltd". It is used to monitor the voltages on the energy storage capacitors C_{in}, C_{out} as well as the currents at the input and output of the converter, and automatically log the values into an Excel spreadsheet. For current sensing, its internal shunts resistors were used, and the whole setup can be seen in its schematic

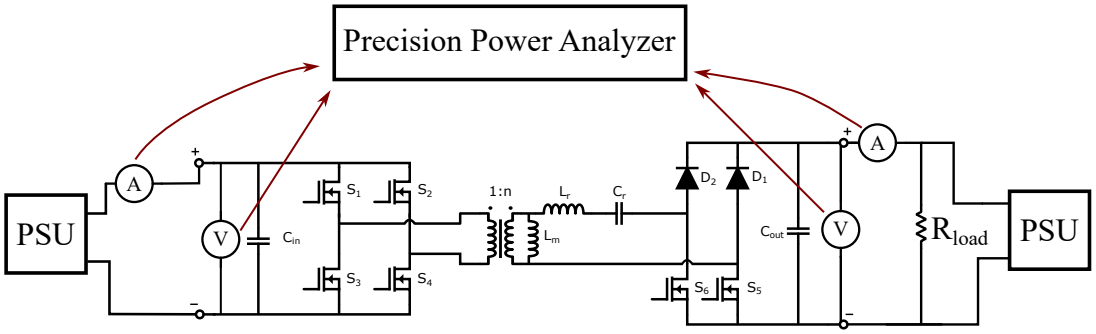


Figure 5.6: Schematics of the lab testing rig.

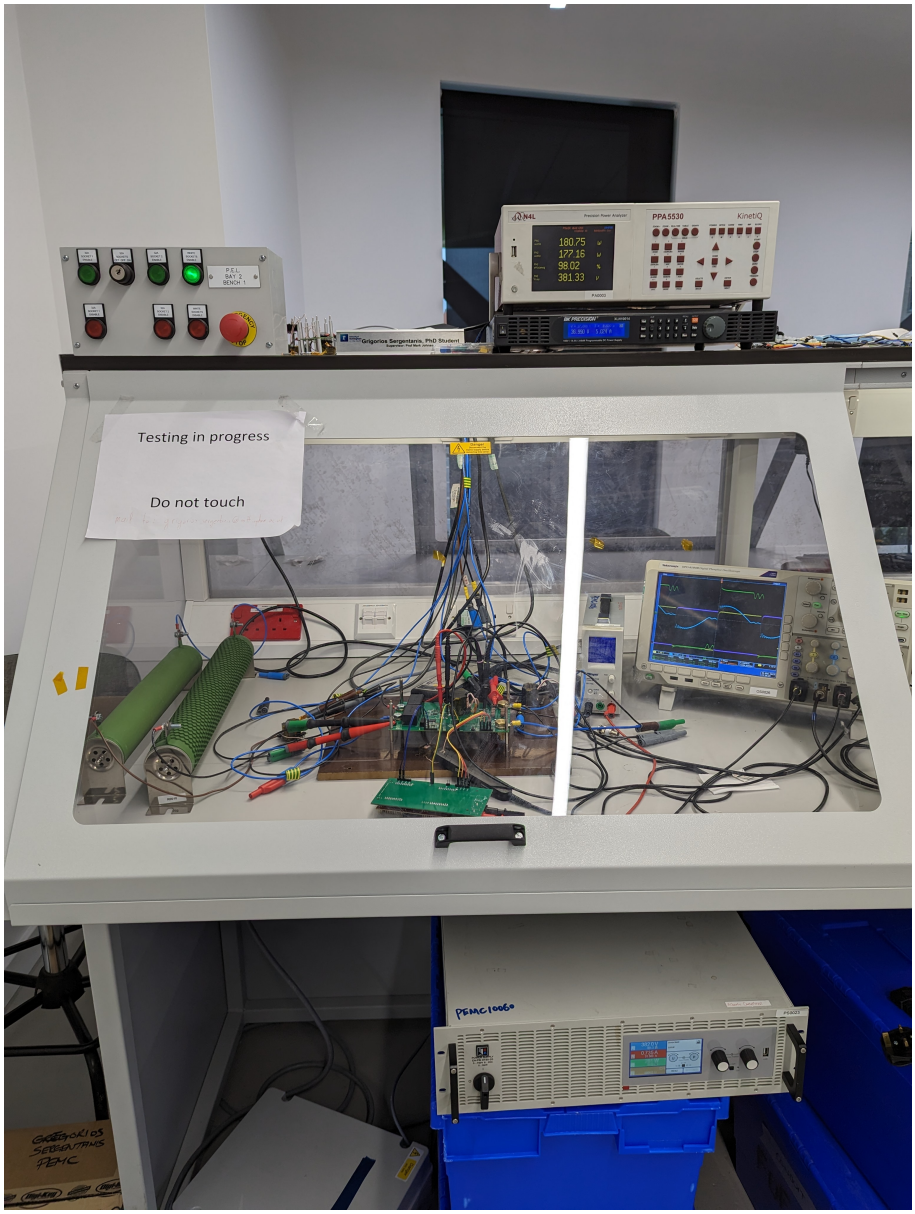


Figure 5.7: The designed converter in operation within the test rig.

format in Figure 5.6 and the assembled rig in Figure 5.7.

5.3.1 Implementation of the gating commands

To test the validity and performance of the proposed converter, PWM signals must be applied to drive the transistors. In this work the Texas Instrument LaunchPad™ F28379D, featuring the C2000™ Delfino™ MCU was used. A separate PCB was designed to host the controller in order to have the Launchpad powered by a PSU, thus avoiding noise from the PC entering the converter. Plus, the required PWM signals were conveniently arranged to provide an easier connection to the converter's respective needs. Open loop tests were run by setting specific duty cycles and dead times within the controller's ePWM modules. The internal structure of an ePWM module is summarised in Figure 5.8, and the associated manual is found in [126].

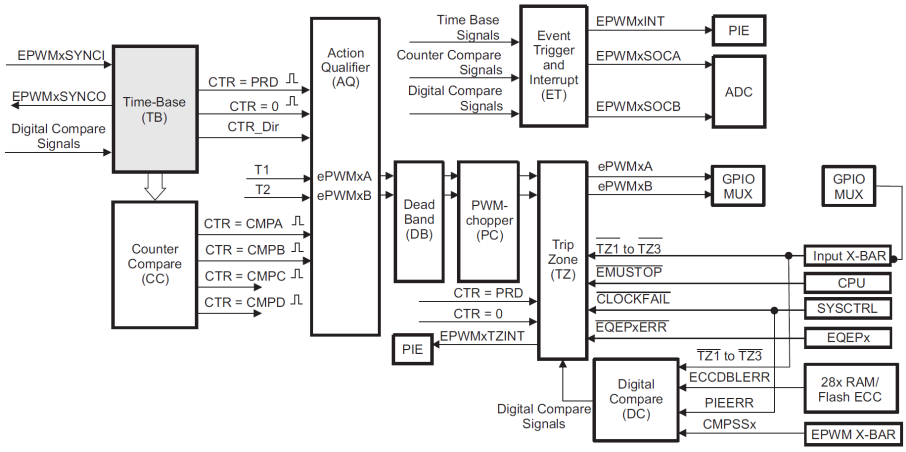


Figure 5.8: Internal structure of the C2000™ PWM block [126].

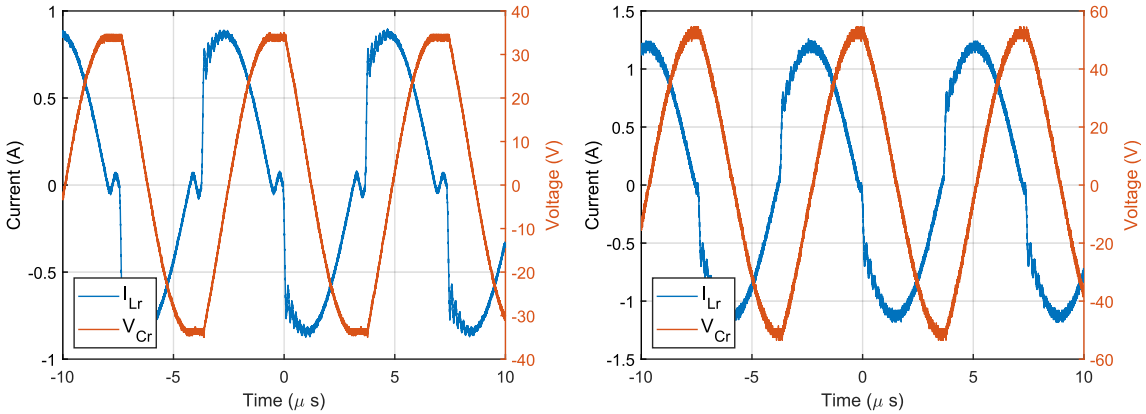
From the ePWM module, the Time-Base (TB) module is used to create the PWM carrier waves and their frequency by passing flags to the Action Qualifier (AQ) when the carrier reaches its limits. Also, the Counter Compare (CC) module is used to compare the carrier wave with up to four different threshold values (CMPA-CMPD), and flags are passed to the AQ accordingly. The Action Qualifier (AQ) is used to set the output of EPWMxA/B according to a certain logic table, with inputs being the flags incoming from TB and CC. Finally, the Dead Band (DB) module is used to assign dead time to the PWM signals output from the AQ in order to create

the required PWM signals to be fed into the converter. Two ePWM modules are used for the primary bridge, one for each leg, and two more are used to control the secondary-side FETS. Naturally, the PWM pulses being sent to the secondary side are passed through an optical isolator to prevent damage to the MCU. All PWM pulses were synchronised using Time-Base Clock Synchronisation.

5.4 Results

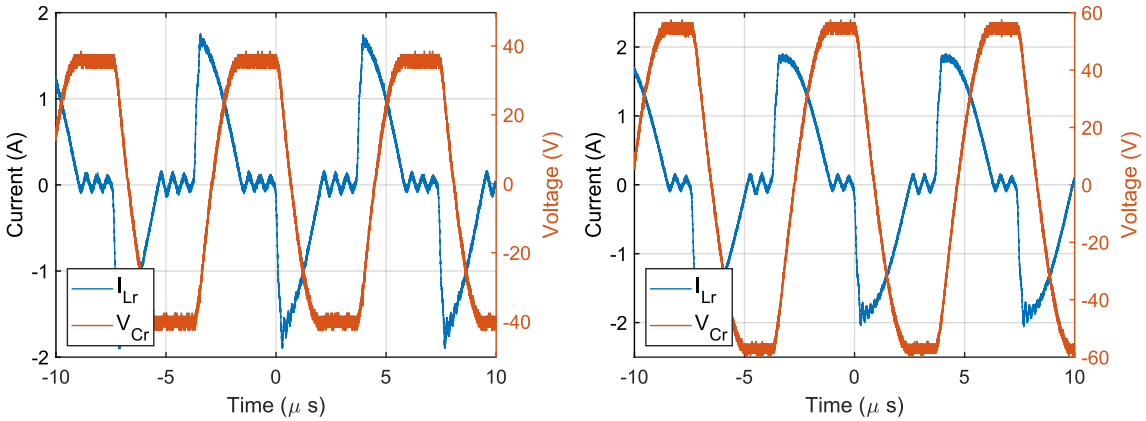
First, the LC tank state parameters were verified. It was noted that the waveforms look slightly different compared to the theoretical analysis presented in chapter 3; however, this was expected. The deviation originates from modelling the transformer as an ideal transformer when conducting the analysis, specifically from the positioning of the magnetising inductance as an extra component parallel to the transformer. In real applications, this property is integrated into the windings. Therefore, the magnetising current flows through the secondary winding and into the resonant tank when the secondary side is conductive, which wasn't the case in the simulation. This manifests in the waveforms as an initial current value through the resonant tank at the moment of conduction. Nevertheless, the operational waveforms are in agreement with the theoretical analysis, and an array of example waveforms acquired in the lab bench may be seen in Figures 5.9, 5.10, 5.11.

After the verification of the converter's operational waveforms was completed, the soft-switching behaviour needs to be examined. The strength of the proposed converter is that ZVS may be achieved throughout the whole load range. This can be seen by examining equations (3.68), (3.70) from chapter 3, in which the input voltage and power play are not included in the dead time calculations. Therefore, tests were run at 100% (300 W) load and 10% (30 W) load to validate that the ZVS behaviour is consistent. To do this, the converter was placed in the DCX Mode, and varying the input voltage level, the input power was altered. Since the mechanism for ZVS is the same in all operation modes, the ZVS waveforms for the boosting and greinacher modes are not presented here. Still, it was validated when conducting



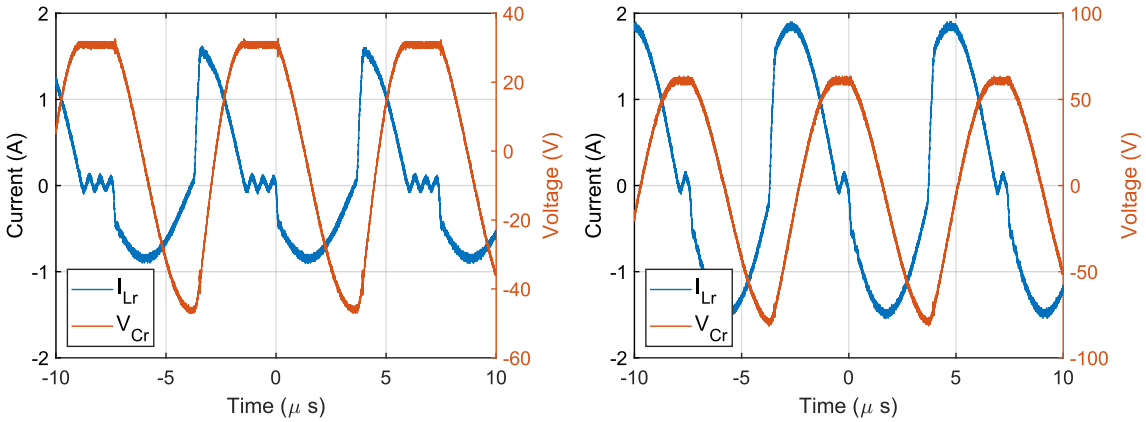
(a) $P_{in} = 200\,W$ **(b)** $P_{in} = 300\,W$

Figure 5.9: Measured resonant tank waveforms in DCX mode.



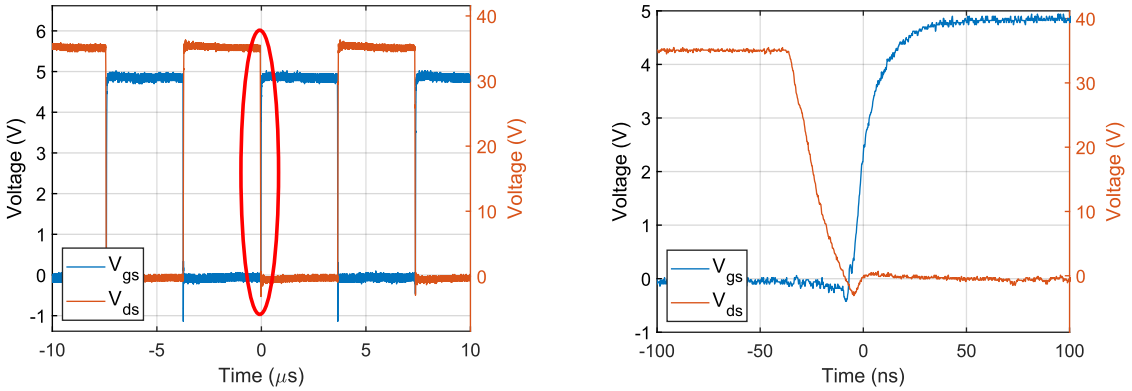
(a) $P_{in} = 200\,W$ **(b)** $P_{in} = 300\,W$

Figure 5.10: Measured resonant tank waveforms in Boosting mode.

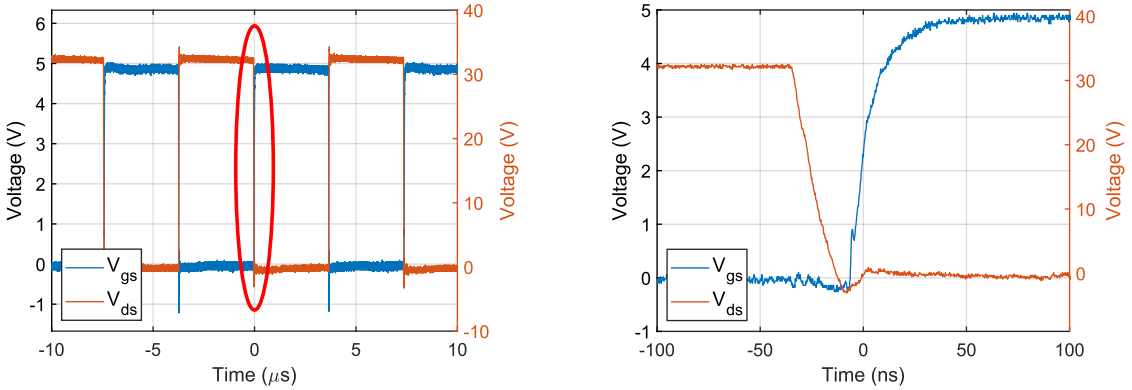


(a) $P_{in} = 100\,W$ **(b)** $P_{in} = 200\,W$

Figure 5.11: Measured resonant tank waveforms in Greinacher mode.



(a) ZVS turn-on at 300W.



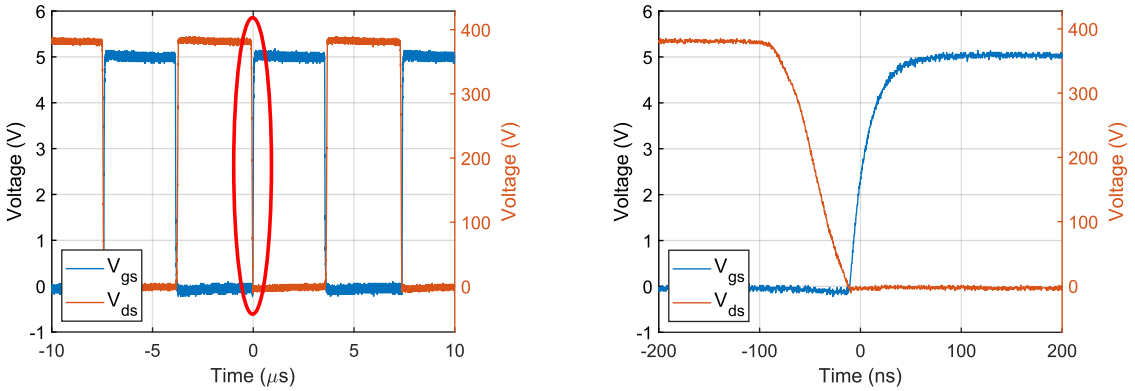
(b) ZVS turn-on at 30W.

Figure 5.12: EPC2021 soft switching turn-on transitions, for 100% and 10% input power.

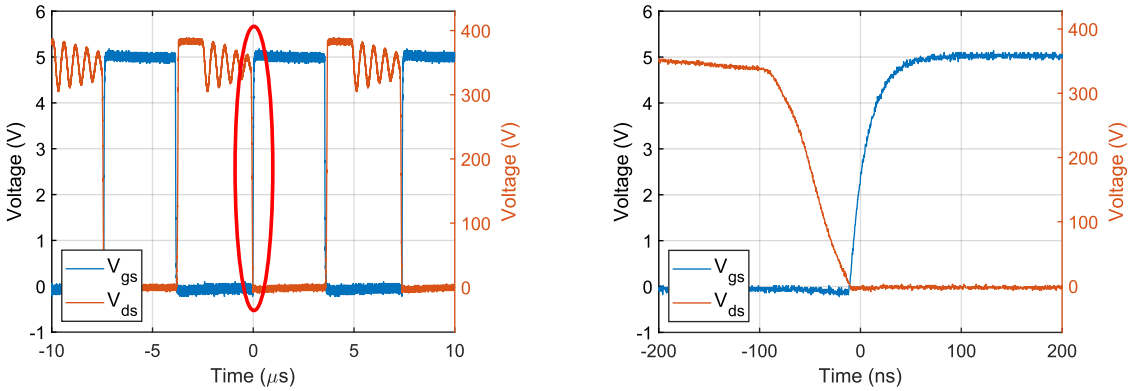
this work that they also were consistent in achieving ZVS.

The resulting waveforms (V_{ds}, V_{gs}) from the presented tests for ZVS are shown in Figures 5.12 and 5.13. It may be seen that for the EPC2021 devices in Figure 5.12, the ZVS turn-on is upheld in high and light load scenarios, albeit with a minor time difference. This minor time difference might be explained by the lowered voltage, which leads to lowered levels of stored energy in C_{oss}. For the NV6115 devices, ZVS turn-on was also achieved in the whole load range (Figure 5.13), and the time taken to achieve the ZVS event appears constant, as it's affected by the LC resonant tank.

The converter's operation waveforms and ZVS behaviour have been verified thus far. The aspects that remain to be verified are the voltage step-up capabilities and the efficiency achieved. Both of these may be evaluated by the power analyser, as it monitors the input and output terminals, sensing their voltage and currents. To estimate the expected losses, the models shown in the Tables 5.1, 5.2 and 5.3 were used. With these models, the loss distributions were computed for each operating



(a) ZVS turn-on at 300W.



(b) ZVS turn-on at 30W.

Figure 5.13: NV6115 soft switching turn-on transitions, for 100% and 10% input power.

state, with the results being shown in Figures 5.14, 5.15 and 5.16.

To verify the theoretical loss distributions that were retrieved, experimental temperature data was logged. The instrument used to see the temperatures during operation was the "Fluke Ti25 Thermal Imager". The temperatures retrieved by using a thermal camera are often not very accurate unless inspecting a uniform material. This is because of the fundamental operation of a thermal camera, which is to read infrared radiation and deliver temperature estimates based on the infrared radiation level. To do this, it needs to know how much a body is capable to radiate (thermal emissivity), and how far the object is (focusing) to estimate the temperature based on the infrared radiation captured.

To retrieve correct temperature readings, the thermal emissivity constant (ε) used within the thermal camera for the calibration should be the same as the material examined. To retrieve the measurements, a reasonable estimate of $\varepsilon = 0.9$ was used. This is a typical value used for plastic material, however anything that has

Table 5.1: Loss Breakdown for DCX Mode

Loss Mechanism	**Formula**
S_{1-4} conductive losses	$4 \cdot \mathrm{I}^2_{\mathrm{S1,rms}} \cdot \mathrm{R}_{\mathrm{ds,on}}$
S_{1-4} switching losses	$2 \cdot \mathrm{V}_{\mathrm{in}} \cdot \mathrm{I}_{\mathrm{Lm}} \cdot \mathrm{t}_{\mathrm{r}} \cdot \mathrm{f}_{\mathrm{sw}}$
$S_{5,6}$ conductive losses	$2 \cdot \mathrm{I}^2_{\mathrm{S5,rms}} \cdot \mathrm{R}_{\mathrm{ds,on}}$
$D_{1,2}$ conductive losses	$2 \cdot (\mathrm{V}_{\mathrm{T}} \cdot \mathrm{I}_{\mathrm{D,avg}} + \mathrm{I}^2_{\mathrm{D,rms}} \cdot \mathrm{R}_{\mathrm{T}})$
Transformer winding losses	$\mathrm{I}^2_{\mathrm{prim,RMS}} \cdot \mathrm{R}_{\mathrm{prim,AC}} + \mathrm{I}^2_{\mathrm{sec,RMS}} \cdot \mathrm{R}_{\mathrm{sec,AC}}$
Transformer core losses	$\mathrm{k} \cdot \mathrm{f}^{\alpha} \cdot \mathrm{B}^{\beta} \cdot \mathrm{V}_{\mathrm{e}}$
Resonant inductor losses	$\mathrm{k} \cdot \mathrm{f}^{\alpha} \cdot \mathrm{B}^{\beta} \cdot \mathrm{V}_{\mathrm{e}} + I^2_{sec,RMS} \cdot R_{Lr,AC}$

Table 5.2: Loss Breakdown for Boosting Mode

Loss Mechanism	**Formula**
S_{1-4} conductive losses	$4 \cdot \mathrm{I}^2_{\mathrm{S1,rms}} \cdot \mathrm{R}_{\mathrm{ds,on}}$
S_{1-4} switching losses	$2 \cdot \mathrm{V}_{\mathrm{in}} \cdot \mathrm{I}_{\mathrm{Lm}} \cdot \mathrm{t}_{\mathrm{r}} \cdot \mathrm{f}_{\mathrm{sw}}$
$S_{5,6}$ conductive losses	$2 \cdot \mathrm{I}^2_{\mathrm{S5,rms}} \cdot \mathrm{R}_{\mathrm{ds,on}}$
$S_{5,6}$ switching losses	$\mathrm{V}_{\mathrm{out}} \cdot \mathrm{I}_{\mathrm{S5,off}} \cdot \mathrm{t}_{\mathrm{r}} \cdot \mathrm{f}_{\mathrm{sw}}$
$D_{1,2}$ conductive losses	$2 \cdot (\mathrm{V}_{\mathrm{T}} \cdot \mathrm{I}_{\mathrm{D,avg}} + \mathrm{I}^2_{\mathrm{D,rms}} \cdot \mathrm{R}_{\mathrm{T}})$
Transformer winding losses	$\mathrm{I}^2_{\mathrm{prim,RMS}} \cdot \mathrm{R}_{\mathrm{prim,AC}} + \mathrm{I}^2_{\mathrm{sec,RMS}} \cdot \mathrm{R}_{\mathrm{sec,AC}}$
Transformer core losses	$\mathrm{k} \cdot \mathrm{f}^{\alpha} \cdot \mathrm{B}^{\beta} \cdot \mathrm{V}_{\mathrm{e}}$
Resonant inductor losses	$\mathrm{k} \cdot \mathrm{f}^{\alpha} \cdot \mathrm{B}^{\beta} \cdot \mathrm{V}_{\mathrm{e}} + I^2_{sec,RMS} \cdot R_{Lr,AC}$

Table 5.3: Loss Breakdown for the Greinacher Mode

Loss Mechanism	**Formula**
S_{1-4} conductive losses	$4 \cdot \mathrm{I}^2_{\mathrm{S1,rms}} \cdot \mathrm{R}_{\mathrm{ds,on}}$
S_{1-4} switching losses	$2 \cdot \mathrm{V}_{\mathrm{in}} \cdot \mathrm{I}_{\mathrm{Lm}} \cdot \mathrm{t}_{\mathrm{r}} \cdot \mathrm{f}_{\mathrm{sw}}$
S_5 conductive losses	$\mathrm{I}^2_{\mathrm{sec,rms}} \cdot \mathrm{R}_{\mathrm{ds,on}}$
S_6 conductive losses	$\mathrm{I}^2_{\mathrm{S6,rms}} \cdot \mathrm{R}_{\mathrm{ds,on}}$
S_6 switching losses	$0.5\mathrm{V}_{\mathrm{out}} \cdot \mathrm{I}_{\mathrm{S5,off}} \cdot \mathrm{t}_{\mathrm{r}} \cdot \mathrm{f}_{\mathrm{sw}}$
$D_{1,2}$ conductive losses	$2 \cdot (\mathrm{V}_{\mathrm{T}} \cdot \mathrm{I}_{\mathrm{D,avg}} + \mathrm{I}^2_{\mathrm{D,rms}} \cdot \mathrm{R}_{\mathrm{T}})$
Transformer winding losses	$\mathrm{I}^2_{\mathrm{prim,RMS}} \cdot \mathrm{R}_{\mathrm{prim,AC}} + \mathrm{I}^2_{\mathrm{sec,RMS}} \cdot \mathrm{R}_{\mathrm{sec,AC}}$
Transformer core losses	$\mathrm{k} \cdot \mathrm{f}^{\alpha} \cdot \mathrm{B}^{\beta} \cdot \mathrm{V}_{\mathrm{e}}$
Resonant inductor losses	$\mathrm{k} \cdot \mathrm{f}^{\alpha} \cdot \mathrm{B}^{\beta} \cdot \mathrm{V}_{\mathrm{e}} + I^2_{sec,RMS} \cdot R_{Lr,AC}$

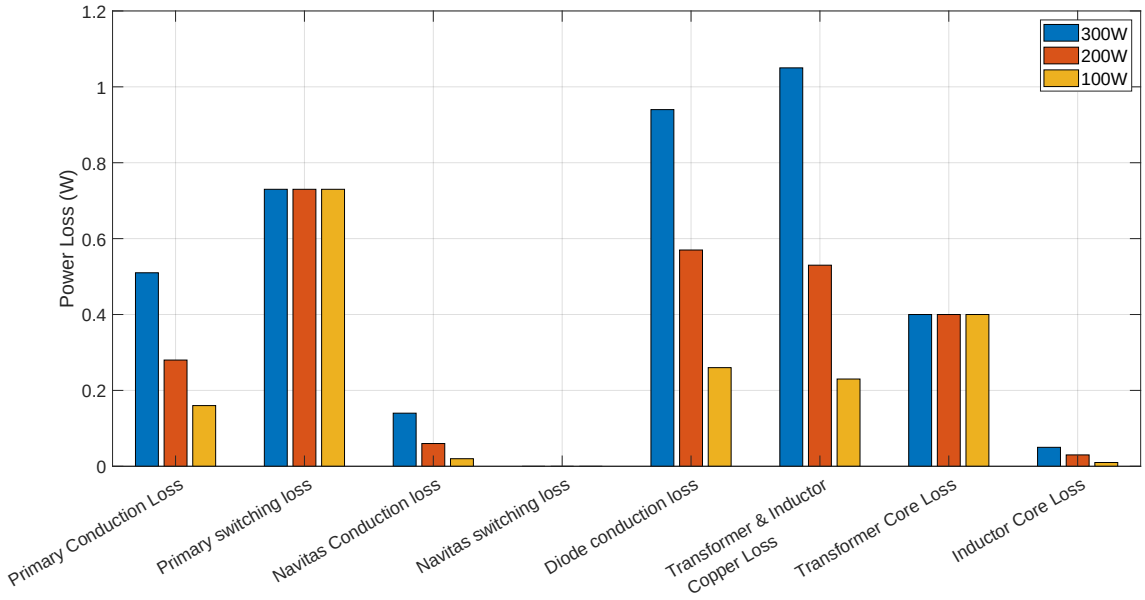


Figure 5.14: Loss distributions at SRC operation.

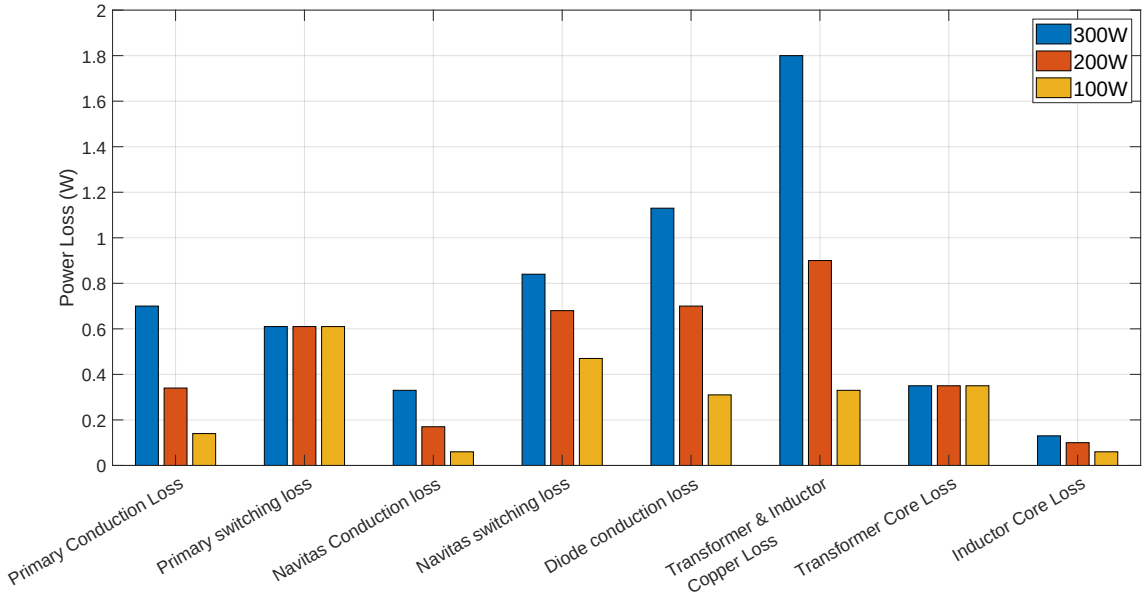


Figure 5.15: Loss distributions at boosting operation with normalised voltage gain equal to 1.1.

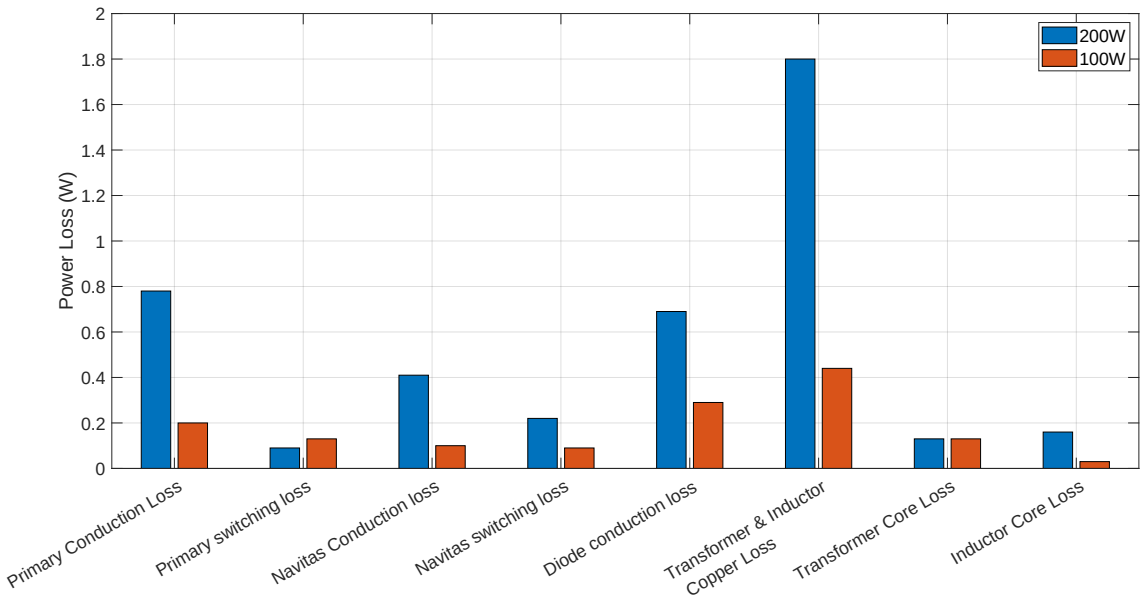
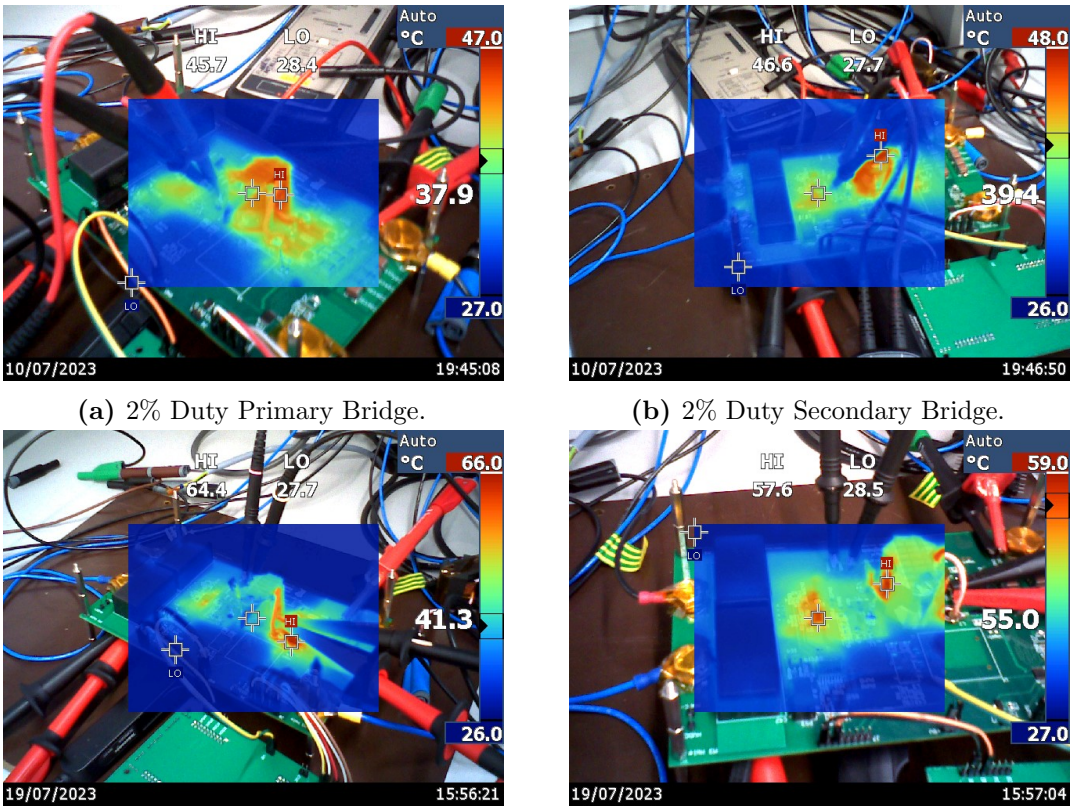


Figure 5.16: Loss distributions at Greinacher operation with normalised voltage gain equal to 2.

exposed metal will appear colder than it is in reality. To aid in the focusing of the thermal image and therefore provide accurate readings, the camera possesses Fluke proprietary software that combines an image on the visible spectrum with the infrared image. Therefore, calibration was made based on this interpolation using the included dial.

The thermal performance of the constructed converter was examined with the camera after reaching its thermal equilibrium. This means that the captured images shown in this chapter were taken after the converter was operating for a few minutes, after which no temperature variations were observed. The reason that necessitated this added waiting time was mainly that the transformer was slower to reach its thermal equilibrium based on its larger dimensions. The steady-state temperature rises may be inspected in Figures 5.17 and 5.18. From these figures, it is possible to evaluate the validity of some of the theoretical loss distribution effects. Another aspect to take into consideration is that the junction temperatures of the semiconductors are impossible to inspect. For the reader's visibility, the given thermal resistances from junction to case are 0.4 °C/W and 2 °C/W for the EPC2021 and the NV6115 devices respectively.

For starters, examining the operation near the normal voltage, it may be seen in



(a) 2% Duty Primary Bridge.

(b) 2% Duty Secondary Bridge.

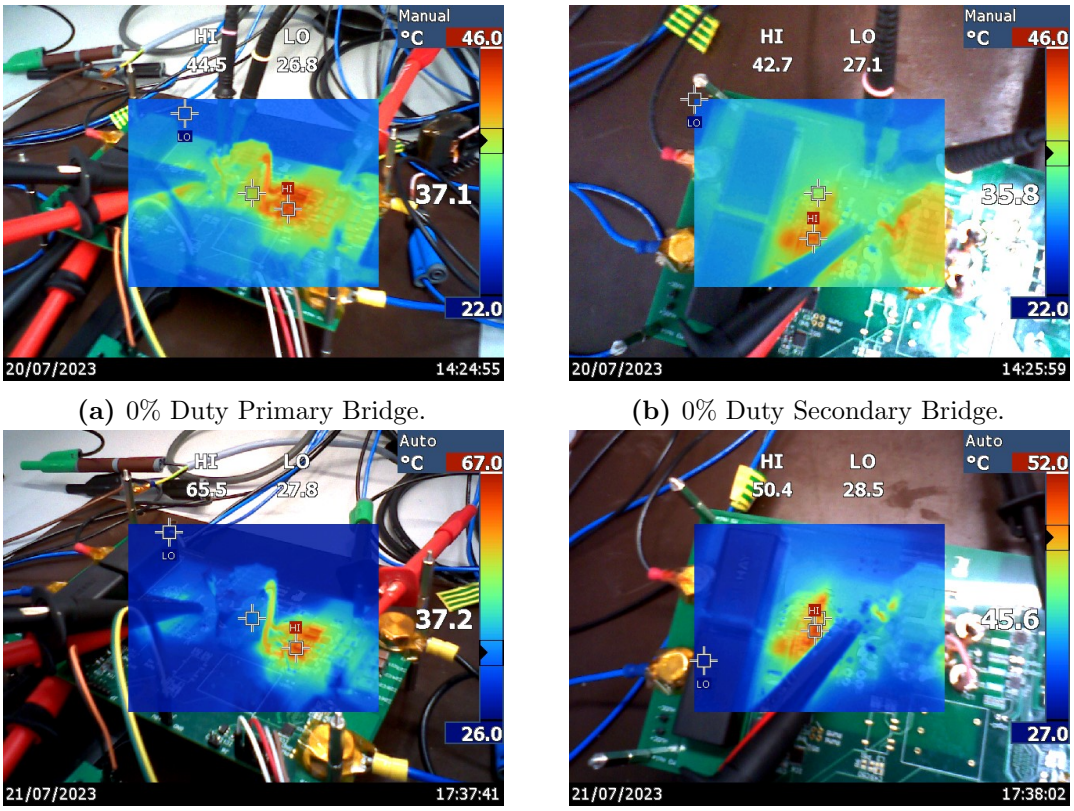
(c) 10% Duty Primary Bridge.

(d) 10% Duty Secondary Bridge.

Figure 5.17: Thermal Images in voltage boosting mode, with 300W input power.

Figure 5.17a that the temperatures of the transformer core and winding don't show a large temperature gradient. However, once the duty cycle is increased, the magnetic winding losses and the primary bridge's conduction losses become prominent loss-generating components, as can be witnessed in Figure 5.17c, wherein the transformer wires and EPC devices pop out in the image as hotpots. Also, from the same figure, the realisation that the cooling of the EPC devices using vias connected to copper pours isn't very effective as there is a considerable temperature gradient between the devices and the surrounding PCB. This is to be expected, as vias typically have a high thermal resistivity due to their thin copper surface.

Another conclusion that may witnessed from the thermal images is that the NV6115 devices have a very low turn-off loss. Unfortunately, when the attempt was made to characterise these devices in detail in chapter 4, the retrieval of accurate results was impossible due to the instrumentation error, plus the errors induced by their ultra-fast switching transients. However, it may be appreciated that when



(a) 0% Duty Primary Bridge.

(b) 0% Duty Secondary Bridge.

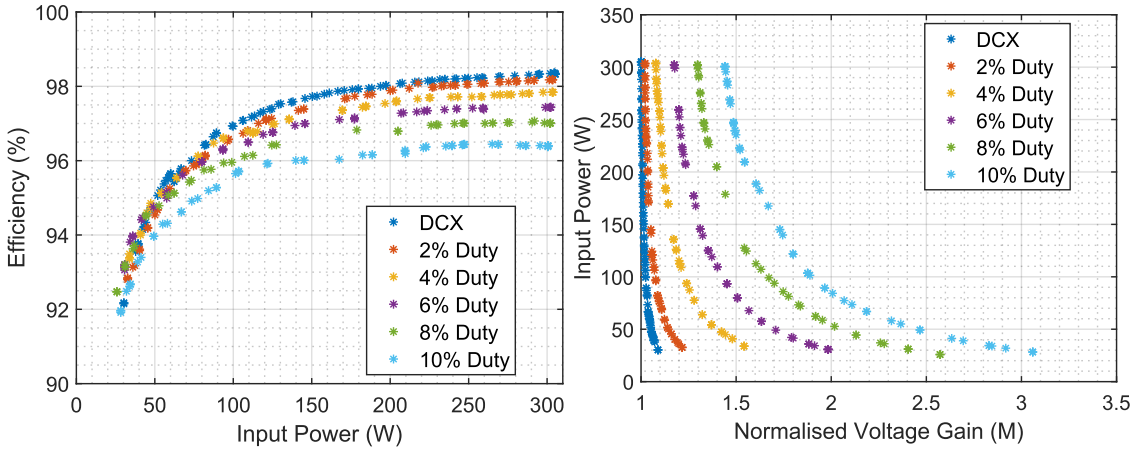
(c) 10% Duty Primary Bridge.

(d) 10% Duty Secondary Bridge.

Figure 5.18: Thermal Images in Greinacher mode, with 200W input power.

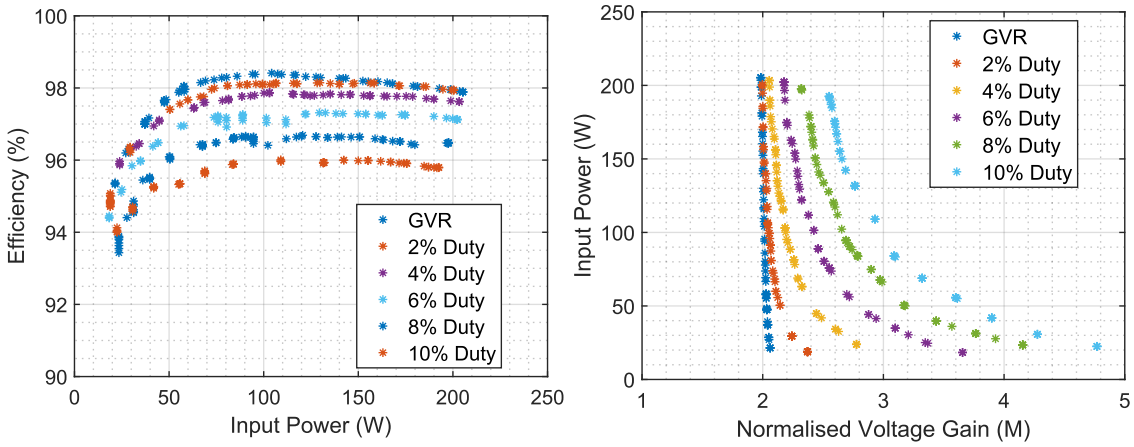
comparing Figures 5.17b and 5.17d, the NV6115 devices showcase an approximate 15°C increase. This modest increase is owed to both the increased conduction losses as well as the increased turn-off current, which normally is associated with an increase in switching loss. If the thermal impedances of the device to the ambient were known, this would be an opportune moment to verify the device switching loss. However, this is considered to be outside the scope of this thesis. Nevertheless, the relatively constant turn-off loss behaviour witnessed in Figure 4.21 appears to have some merit. Finally, from the retrieved images, it may be seen that the maximum temperature seen is near 65°C, which means that the temperature rise compared to the ambient temperature was less than 40°C. This confirms the converter's ability to be used in high-temperature scenarios.

The expected peak efficiency of the converter using the theoretical loss models has been found to be approximately 98.7% at full load [127]. Naturally, a peak efficiency somewhat lower than this is expected, as the loss model constructed does



(a) **(b)**

Figure 5.19: Experimental Efficiencies (a) & Voltage Step-Up (b) in Voltage Boosting Mode. Data points that were acquired using the PPA5530 are plotted as asterisks.



(a) **(b)**

Figure 5.20: Experimental Efficiencies (a) & Voltage Step-Up (b) in Greinacher Boosting Mode. Data points that were acquired using the PPA5530 are plotted as asterisks.

not account for temperature rise-related losses, third quadrant conduction losses on the active devices, or the added harmonic losses experienced by the magnetic components. The peak efficiency observed experimentally is slightly below 98.5% as shown in Figure 5.19a. Also, the experimental efficiency graph shapes and peaks seem consistent with the theoretical predictions the author made in [127]. Finally, the non-linear relation of the voltage step-up with the input power and the duty cycle can be seen pictorially in Figures 5.19b and 5.20b. The step-up ratios retrieved are lower compared to the values graphed in chapter 3, but this was expected, seeing that the resonant inductor value was considerably enlarged by the transformer's leakage inductance.

5.5 Summary

The goal of this chapter was to confirm the validity of the proposed converter in a lab environment. The proposed converter was designed and assembled into a test rig to confirm its operation and performance. The main design challenges faced in the assembly and layout of the converter have been presented, and solutions have been proposed for the reader. With the waveform examination of the converter, the soft-switching behaviour of the converter has been verified, along with the operational waveforms of the LC resonant tank. The loss mechanisms have been reaffirmed by the use of thermal imaging and appear to hold true. The capability of the converter to provide high power conversion efficiency with a simultaneous high voltage step-up ratio has been confirmed using a precision power analyser, and it has shown good agreement with the expected values.

Chapter 6

Scaling Up the Frequency - Implementation at 1 MHz

6.1 Introduction

Thus far, this thesis has provided a novel proposed converter for PV module applications. It has been theoretically analysed in Chapter 3 for its operation. Furthermore, efficiency has been theoretically and experimentally verified in Chapter 5, and so have the converter's operational waveforms. Due to the properties of GaN transistors, as shown partly in Chapter 4, it is possible to create efficient power conversion using high-frequency PWM. That is the case since their low junction capacitances allow unprecedented small dead times to achieve ZVS turn-on. This allows for the creation of slim power conversion systems, which will be the aim of this chapter.

The significant challenges faced when augmenting the switching frequency, compared to those encountered in Chapter 5, will be presented. Furthermore, converter prototypes have been designed and tested, and the various problems that arose will also be presented. Finally, solutions will be given to improve the behaviour of the proposed converter, as the results retrieved within the time frame of this thesis leave room for improvement.

6.2 Converter Design

With the scaling of the converter to a higher frequency, a lot of the previous work from Chapter 5 can be reused. For example, the layout of the primary-side devices is primarily kept the same, as fast and clean switching waveforms have already been achieved. Naturally, the size of all passive components, such as the transformer and energy storage capacitors, may be reduced owing to the higher operating frequency. Particularly for the magnetic elements, with the increase of the frequency, the skin effect becomes more prominent. This means that thinner wire strands than those used previously would need to be used, with a steep increase in cost. Therefore, in high-frequency power conversion designs, planar transformers tend to be used, which allows for PCB tracks to be used as the winding material. This usually also allows for slimmer converters, better heat dissipation owed to their lower thermal resistance, and predictable parasitic behaviour when facing mass manufacturing [128].

Based on the facts mentioned above, work was conducted to design a planar transformer, which is presented in this Chapter. Also, when dealing with higher power conversion frequency, effects that generally have a minor impact become more critical; this includes effects such as third-quadrant conduction of active devices as well as PCB track parasitics. The effects of parasitic components become even more prominent when dealing with isolated high-voltage step-up (or step-down) conversion systems. Therefore, to allow for efficient high-frequency conversion, additional care must be shown when designing the PCB, which now extends beyond the simple commutation cell. Thus, the challenges faced in this regard are displayed in this Chapter, along with guidelines for PCB layout design.

6.2.1 Magnetic Design

Concerning the design of the planar transformer, the workflow presented in chapter 3 was once again used. The first step taken was the selection of the ferrite core material. As the aim of this work is to have a high energy yield from the PV panels, it was considered a priority to ensure minimum ferrite core losses. In this

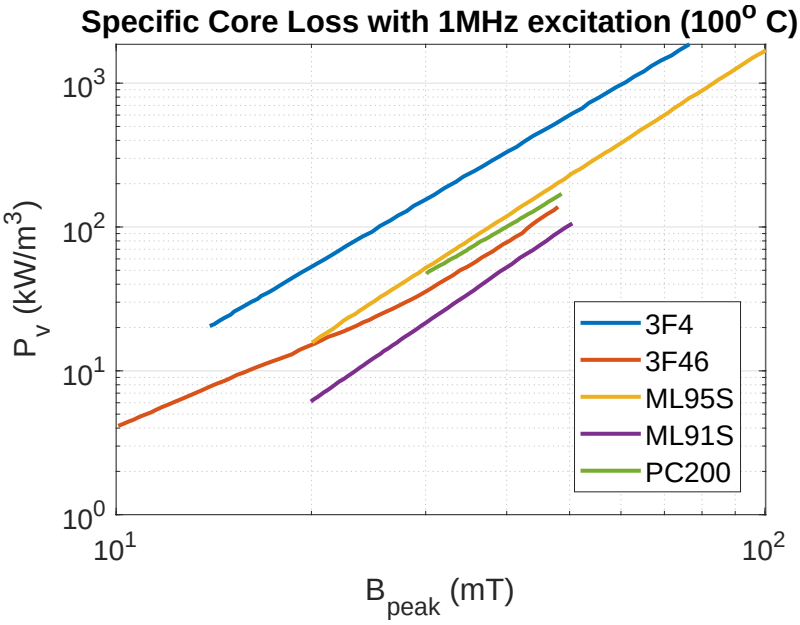
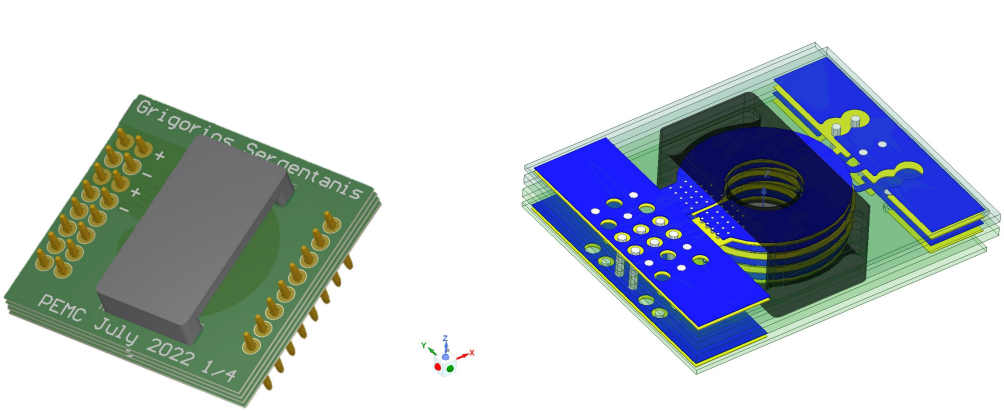


Figure 6.1: The specific core loss of various high-frequency ferrite materials.

wavelength, a small survey of the available ferrite materials marketed as suitable for high-frequency power conversion was undertaken. The results of this search may be seen in Figure 6.1, wherein the ML91S material from Proterial Ltd. seems to be the most advantageous in terms of loss minimisation. The displayed data was retrieved from the respective datasheets of the various materials, and the comparison was made at 100°C since there was more data available at this temperature.

After selecting the core material, the core shape is to be chosen. While this stage was relatively simple when using wire-wound magnetics, there are several aspects to be considered here. Based on the existing literature on planar transformers, a cylindrical centre-leg is preferred over a rectangular one [129], as this leads to reduced AC resistance for the same conductor dimensions. This occurs because of the current crowding experienced on the edges of the rectangular conductors.

After inspecting the core shapes available in the widely known electronic retailers (Digikey, Mouser, etc.), it was found that the core shapes for this material consist of EE(R), EI(R), and RM core shapes. Concerning the copper windings, the skin depth at the frequency of the main harmonic (1 MHz) is approximately 0.065 mm, which is close to the equivalent thickness of a 2 Oz copper track within the PCB. As it is possible to benefit from the introduction of thicker copper tracks, the design



(a) **(b)**

Figure 6.2: A multi-board PCB transformer was designed in Altium Designer (a) and then imported to the Ansys Electronics environment (b).

will consider an upper limit of 4 layers for the PCB under consideration. This is done as it is challenging to order multi-layer PCBs with thick traces, and it requires speciality PCB manufacturers with long associated lead times. Therefore, the limit on the layers was set in order to achieve valuable results within the allocated time frame of the PhD.

Since the number of layers and, therefore, of available turns is limited, in this chapter, the transformer will be designed with the aim of a 1:10 voltage step-up ratio. This is done to avoid the use of fractional turns, which would further complicate the design. Considering a 35 V input voltage, the DCX output will be 350 V, which is still a usable voltage for an inverter. Moving on, when the magnetic design flowchart (Figure 3.28) is used with these parameters, it was found that the copper loss dominates the total overall losses of the transformer. This is not an ideal scenario. Thus, the idea of assembling a transformer comprising four 2-layer PCBs to increase the available copper area was examined, as shown in Figure 6.2. In this transformer, the transformer turns ratio is 2:20, with the primary side benefiting from parallel turns connected using via stitching.

The idea of using two-layer PCBs to assemble an efficient planar transformer seems relatively straightforward. However, it has a rather insidious issue. The two-layer multi-board structure benefits from the easy paralleling of the primary side tracks. However, the current isn't shared equally between the turns. This happens

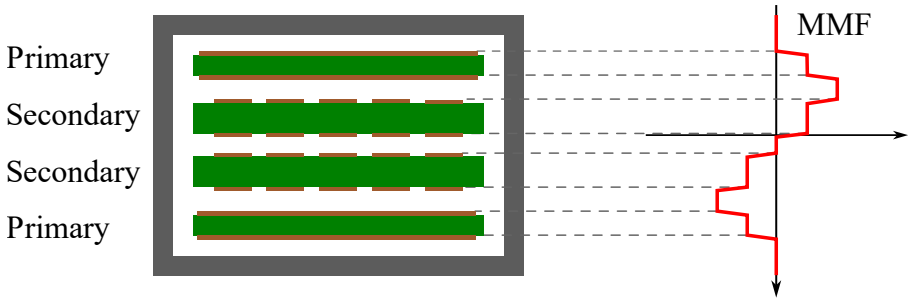


Figure 6.3: Partially interleaved structure of the multi-board planar transformer.

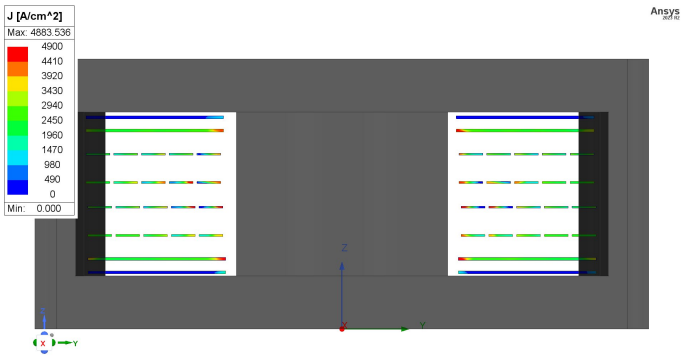


Figure 6.4: Uneven current sharing on parallel windings. The winding nearest to the secondary-side conductor will take a higher proportion of the load current.

because the winding nearest to the secondary-side winding has a lower resistance due to the proximity effects since the windings are partially interleaved, as seen in Figure 6.3. The uneven current sharing between windings will lead to thermal hotspots, which may impact the reliability of the transformer. In any case, this leads to a worse utilisation of the available winding space. To showcase this problem, the transformer was simulated using Ansys Maxwell 3D FEA, with the transformer delivering approximately 260W to an external load on the high-voltage side. It may be seen in Figure 6.4 that the majority of the input current is conducted via the conductors nearest to the secondary-side windings. To get an understanding of the grand imbalance that occurs, the current density was integrated with the surface of winding cutouts visible in Figure 6.4. It was found that one turn carries a sine wave with a peak current of 12.9 A, while the other winding carries just 0.8 A. Naturally, this was considered inappropriate to use within the designed converter, and alternative solutions were devised.

An interesting solution found in the literature is the concept of the matrix trans-

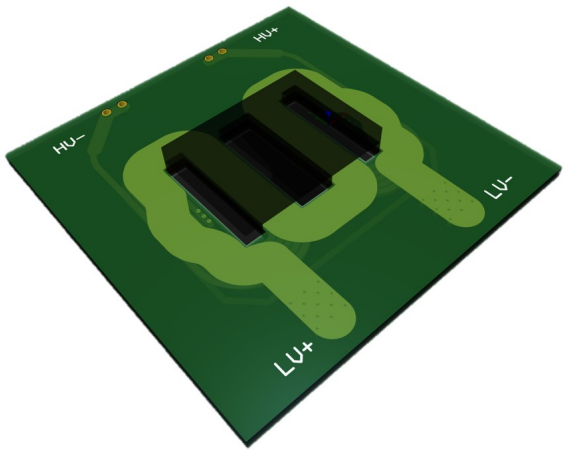


Figure 6.5: Matrix Transformer Designed in Altium Designer.

former. The idea behind the matrix transformer is to create an assembly of multiple modular transformers, either connected in series or in parallel, depending on the application requirements. This allows for an array of elemental transformers, with each of them processing only a part of the required power. Researchers have widely used the idea of the matrix transformer, and an excellent overview of this topic is provided in [130]. Matrix transformers have already been used to provide breakthrough efficiency and power-density results in isolated step-down power conversion systems [131].

In this thesis, a matrix transformer will be employed to increase the available winding window based on the readily available ML91S cores. Based on the desire to achieve a slim converter profile, one PCB will be used to allow for a converter-embedded transformer. Therefore, an EI core will be used, as it has a slimmer profile. Based on the survey of the available core sizes, EI 21.8-8.2-15.8 was selected, as it possessed the widest winding window from the available cores. A PCB was designed by using the outer legs of this core as the centre leg of modular 1:10 transformers connected in series. The resulting PCB can be seen in Figure 6.5.

In the designed matrix transformer, the side-leg comprises two parallel primary-side turns located on the outer layers of the PCB for better heat dissipation, as well as ten secondary-side turns. Naturally, the transformer was inserted into the ANSYS Maxwell 3D software to check for the current sharing capabilities of the

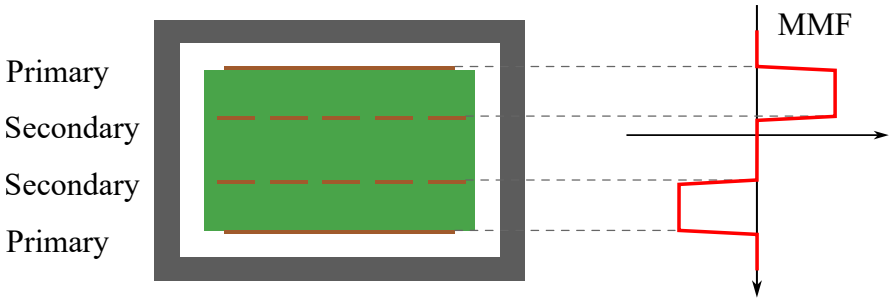


Figure 6.6: Matrix transformer designed winding stack-up. It may be seen from the MMF graph that the paralleled primary windings should have an equal impedance for balanced current sharing.

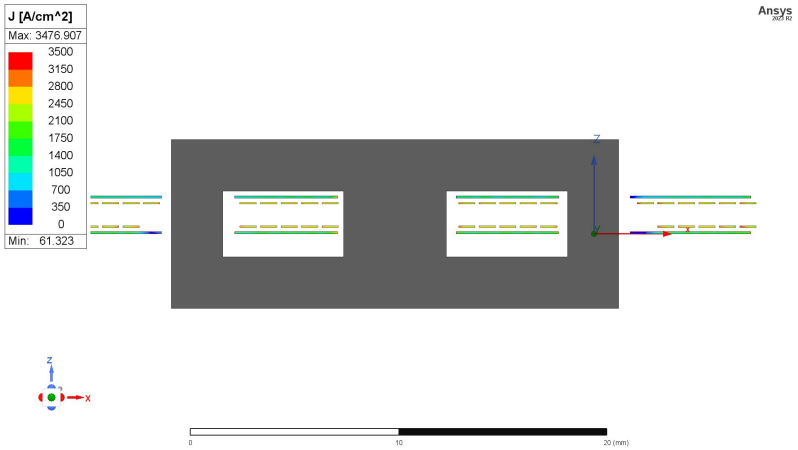


Figure 6.7: Even current sharing on parallel windings. The MMF changes on the paralleled current branches are equal, so the current is evenly shared between them.

paralleled windings. In this design, the paralleled primary side windings experience the same MMF changes in their proximity, as seen in Figure 6.6. This, in turn, provides good load current sharing capabilities as seen via simulation in Figure 6.7. It's worth noting that the simulation parameters stayed the same with the previous transformer design, i.e. the transformer is excited with a 40 V peak sine voltage, and it is outputting 260 W on the high-voltage side. Therefore, comparing Figures 6.4 and 6.7 shows a significant reduction in current -and therefore temperature- hotspots, which is a beneficial property.

Finally, after deciding on the transformer layout, other design aspects must be taken into consideration. One design choice is the copper weight to be used on the transformer. Based on the high operating frequency, increasing the copper weight will eventually have diminishing returns, as the R_{ac} will eventually stay constant with increasing copper thicknesses as the current gets crowded to the edges.

Table 6.1: Properties of the designed planar matrix transformer.

Design Variable	Value	Design Variable	Value
Core type	EI/ML91S	Air Gap	$2 \cdot 0.07\,mm$
Copper Weights	2 Oz	Coupling Factor	98.5 %
Turn ratio	2:20	$L_{m,HV}$	$68.86\,\mu H$
$C_{intra,HV}$	$15.2\,pF$	C_{inter}	$223\,pF$
$R_{ac,prim}$	$6.4\,m\Omega$	$R_{ac,sec}$	$597.4\,m\Omega$

Simulations were run in ANSYS Q3D extractor to find that the value of R_{ac} at 1 MHz decreases considerably up to 3 Oz copper weight. Nevertheless, 2 Oz copper was used throughout as a compromise between performance and ease of assembly. Another design choice is the layer stack-up to be used. Extensive simulations were run in ANSYS Maxwell using the AC Conduction and Electrostatic solvers to understand the effect of the stack-up on the resulting parasitic capacitances. While these are not presented here for the sake of brevity, it was found that the ideal stack-up spaces the windings at equal distances. This not only provides a moderate lumped interwinding capacitance but also provides the least intrawinding capacitance, which is of critical importance for ZVS realisation, as shown in section 3.3.1.

Having done the procedures described above, the final step is to add an air gap to aid in the ZVS realisation of the primary-side devices. The air gap is designed using the same procedures as section 3.3.2. The resulting transformer was ordered, and its simulated values have been verified using the E4990A Impedance Analyser to be similar to the values received from FEA simulations. The transformer's properties can be inspected in Table 6.1. It may be noted that the winding resistances are considerably higher compared to the wire-wound transformer, as found in Table 3.1. Therefore, high efficiency isn't anticipated with the design in its current form, but the proof-of-concept was prioritised initially. The idea is that once the converter is operational as expected, then improvements can be investigated in the transformer design.

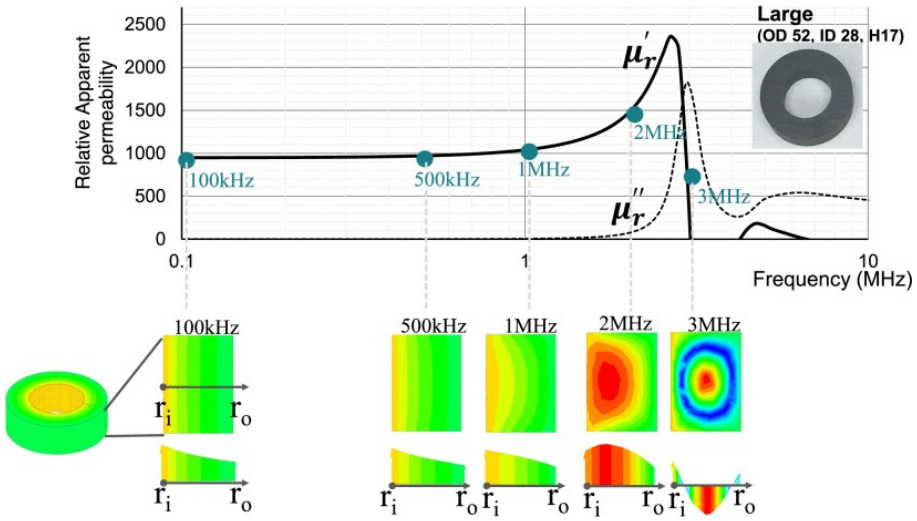


Figure 6.8: Magnetic field distribution within an ML91S core with varying excitation frequencies [132].

High-Frequency Core Effects

The design of the planar transformer to be used within this converter has been presented. The various challenges associated with the winding layout have been presented in the previous section. Unfortunately, when designing an isolated converter to be used at high switching frequencies, additional challenges arise even within the core size design. In wire-wound transformers thus far, a core shape is selected based on the intended converter size factors, its winding window and its shielding capabilities. However, as switching frequencies rise along with the associated higher-order harmonics, certain simplifications that are typically done by power electronic designers stop being true.

In the case of the core, what might stop being true is that the magnetic flux within the core is uniformly distributed. With high enough excitation frequency or high enough transformer core dimensions, the core can begin to experience what is commonly referred to as "dimensional resonance", during which the magnetic flux density is non-uniform and might even reverse polarity. The values that create this phenomenon lie in the permeability and permittivity values of the core materials.

One convenient way to understand this effect is to think of the flux density as a standing wave, of which only a snapshot centred around the core centre-leg is visible. If the wavelength of this wave is large, it will appear reasonably uniform

to the observer. However, as the frequency rises, its status as a wave begins to be visible, and this can be seen in Figure 6.8. This aspect would typically not be examined by the author, first because retrieving the permittivity (ε) of a ferrite core material is a challenging task, and secondly because the used core has relatively small centre-leg dimensions, so dimensional resonance effects are not likely. Thankfully, other researchers have published the required data in recent times [132]. In the same work, a guideline is provided when designing high-frequency magnetics in order to avoid any dimensional resonance phenomena, which is shown in equation (6.1). In this equation, μ' is the real permeability of the material at the examined frequency, while ε' is the real permittivity of the material at the same frequency.

$$d \leq \frac{\pi}{2\omega\sqrt{\mu'\varepsilon'}} \tag{6.1}$$

For the designed transformer at 1 MHz excitation, (6.1) gives a limit of 13 cm for the smallest cross-sectional dimension, which is much larger than the used core dimensions, thus allowing predictable inductive behaviour even in higher order harmonics. In the cited research [132], two more factors to consider to achieve relatively uniform flux density are presented (skin effect and eddy effect), and it was confirmed that the designed transformer does not suffer significantly from these effects. Generally, it appears that high-frequency core effects require careful consideration, but mostly at higher power levels than those examined in this work.

The proposed design, while it does not suffer from dimensional effects, is expected to have a core loss higher than is expected by its Steinmetz parameters predict, because it is operated at slightly higher peak flux densities (70 mT) than those recommended by the manufacturer (50 mT) based on the constraints of the design and the difficulty in winding parallelisation. It is expected this will be manifested as reduced efficiency in the voltage boosting modes, which cross the manufacturer-provided flux density limit and will be particularly visible at low power levels.

6.2.2 Layout Considerations

The reduction of magnetic component dimensions comes with its own set of risks. With a planar transformer with a low turn count, the inductances that are associated with it are naturally considerably lower. Suddenly, the capability of the PCB layout to have a significant effect on the converter behaviour is enabled. This situation becomes even more challenging to manage, based on the fact that planar transformers are generally associated with higher parasitic capacitances as well.

Additional caution is required when facing a high-frequency but simultaneously high-voltage step-up converter. From basic transformer theory, some relationships define how an impedance is reflected on the opposite side of a transformer. When having a voltage step-up transformer with a step-up ratio of n, the inductances of the primary side appear magnified from the perspective of the secondary side, according to Equation (6.2). Similarly, the capacitances of the secondary side appear magnified when viewed from the primary side of the transformer, according to Equation (6.3). These relations define the main challenge points of interest when performing the PCB layout and will be analysed in the following sections.

$$L_{sec} = n^2 L_{prim} \tag{6.2}$$

$$C_{prim} = n^2 C_{sec} \tag{6.3}$$

Inductive Parasitic Effects

One risk that arises when designing the layout for the proposed converter is owed to the PCB track parasitic inductances. This becomes an increasing risk with increasing switching frequencies as the size of the magnetic components decreases, and therefore, so do their associated inductances. In the designed converter, for example, the leakage inductance may be found using the values found in Table 6.1 and Equation (6.4). Then, using Equation (6.2), it is found that the total leakage inductance, as seen on the primary side, is close to $20\,nH$. This is comparable to the inductances one might expect from PCB traces, as seen in Chapter 4.

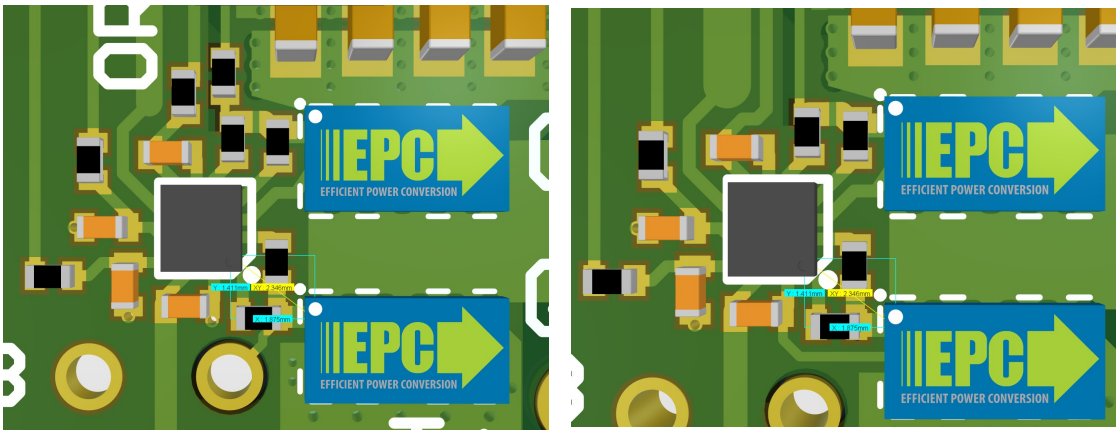
$$L_{lk,HV} = L_{m,HV} \cdot (1 - k^2) \approx 2\,\mu H \tag{6.4}$$

The low value of the series inductances requires additional care to ensure that the conduction paths in both half-cycles of the primary bridge are of equal length. This issue has been thoroughly analysed in [133], and layout guidelines are provided in the cited work, which was implemented when conducting the PCB layout. The designed PCBs for this chapter may be inspected in Appendix D. The main reason that care is required to equalise the track inductances for both states of the primary-side bridge is to prevent an asymmetric current in the resonant tank in each half-period. This would increase the converter's RMS currents for the same power level and thus lower its efficiency [133].

Capacitive Parasitic Effects

In a similar fashion to the previous effect, the parasitic capacitances on the secondary side of the converter create a notable impact on the primary side. For example, the lumped intrawinding capacitance of the designed transformer has been simulated and measured in Table 6.1. This capacitance, when reflected on the primary side, will be approximately $1.5\,nF$. Based on the measured values of the EPC device junction capacitances in section 4.2, and their equivalent role in successful ZVS turn-on as seen in section 3.3.1, the transformer's capacitance will actually have a more significant impact on ZVS behaviour, than the active devices.

Therefore, a paradigm shift is noticed. Whereas in the typical resonant converter design, ZVS turn-on is defined mainly by the equivalent output capacitance C_{oss} of the active devices, in high step-up isolated converters, it can be dominated by the transformer design. This means that to achieve a good design, the transformer design procedure, which is followed for energy minimisation, cannot be based simply on core and winding losses but also on dead-time-related losses. Finally, at the same wavelength, the switching nodes on the secondary side of the converter should not have any unnecessary overlaps with the DC nets, as it would increase the dead-time



(a) **(b)**

Figure 6.9: Gate drive loop for the low-side device, with a magnetic-cancellation layout (a) and a lateral layout in (b). It may be seen that the distances between the gate driving output pin and the gate pin have been kept constant.

requirements, as explained in [133].

Gate Driver Layout Investigation

In section 5, the designed converter used the gate driver LM5113 by Texas Instruments to drive the EPC FETs. The author used the WSON packaging instead of the DSBGA package in the later prototyping for easier assembly, utilising magnetic cancellation current flows to reduce the gate loop inductance. This part is obsolete, and Texas Instruments recommends the LMG1205 as its suitable replacement. This gate drive benefits from improved startup performance and from an integrated bootstrap circuit to aid in driving the upper-side FET. The LMG1205, however, comes only in the DSBGA package, which has dimensions of approximately 1.8x1.8 mm. Also, 0402 packages were used for the accompanying passive devices, allowing for a very compact gate driving loop, the size of which may be appreciated in Figure 6.9.

Therefore, the question of whether magnetic-cancellation traces are worth it in these small distances arose. While allowing the return current to cancel some of the inductance with the forward current, there is the added inductance from using a via to route the return current. Therefore, it might be advantageous to keep the gate path routing on the outer layer without using any vias. To this goal, the layouts shown in Figure 6.9 have been imported into the Ansys Q3D environment to validate

Table 6.2: LMG1205 gate drive turn-off loop inductance.

	Loop Inductance
Lateral Layout	1.84 nH
Overlapping Layout	1.03 nH

the best design choice in terms of parasitic inductance in the gate driving path. The loop inductances during the turn-off path were simulated, as this is the most advantageous scenario for the lateral gate driving design since the loop area is very small. Nevertheless, it appears that even in this scenario, the magnetic-cancellation design provides a lower gate drive loop inductance, as seen in the results in Table 6.2.

Based on these results, the magnetic-cancellation layout was used for the bottom-side devices. For the upper-side devices, a lateral layout was used to avoid any capacitive coupling, as it is a node with high dv/dt transients. It might be noticed that in the previous chapter, an overlapping gate driving circuit was selected for the high-side devices. However, based on the lower inductance values compared to the lower-frequency design, higher-frequency ringing is anticipated, so the author has taken a more cautious approach to this design. Finally, the full PCB designs may be seen in Appendix D.

6.3 Experimental Setup

The designed prototypes were assembled using the guidelines proposed in this thesis. They were tested for correct behaviour prior to providing any power in the converter circuit (see Figure 6.10). The LC tank was tuned via trial and error, as was done in the previous chapter. The lab test rig to evaluate the converter performance is the same as the previous chapter and may be seen in Figure 5.6. A minor difference is that this time, the control board was connected directly to the converter PCB. This was done to avoid any additional noise pickup from the use of jumper wires, as higher frequency oscillations are anticipated thanks to the more compact transformer.

Figure 6.10: The tested 1 MHz converter.

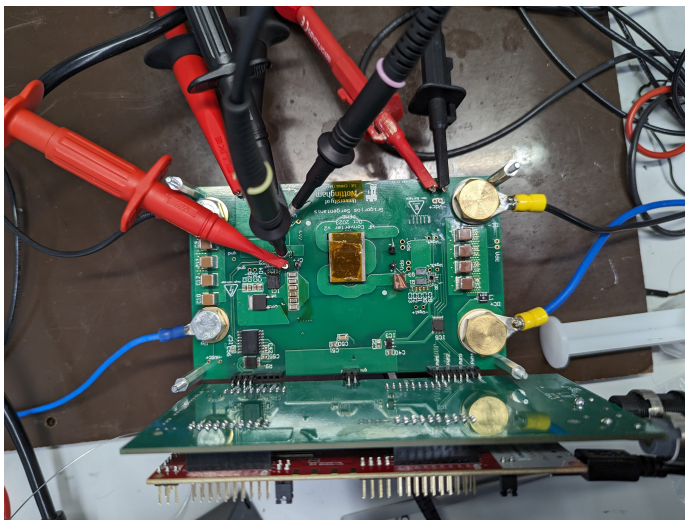
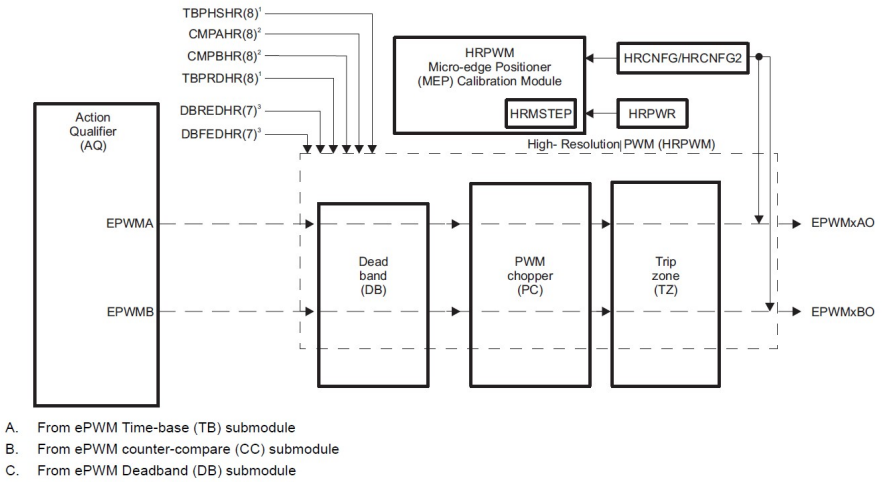


Figure 6.11: The implemented connection of the controller card.

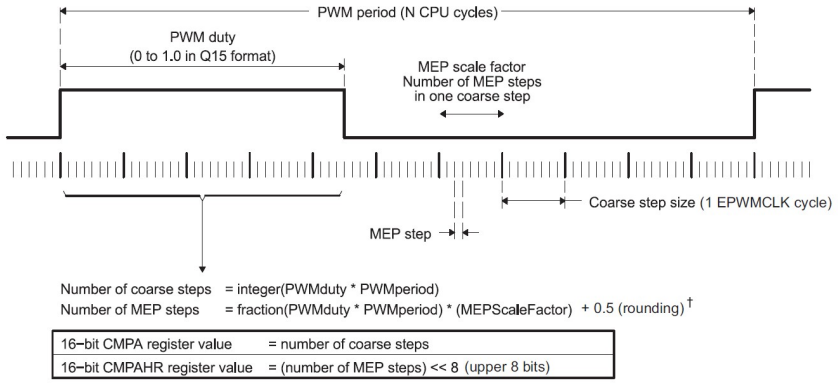
Additionally, the control board is designed as a Faraday cage by using a 4-layer PCB, with the two outer layers being the ground. Plus, the two ground planes were connected using via stitching on the outer edge of the board, using two rows of vias in a diagonal arrangement to enclose the included tracks from high-frequency noise pickup fully. The connection made within the test rig can be seen in Figure 6.11. This setup should, in theory, shield the TI Launchpad and the signals it produces from high-frequency noise pickup.

6.3.1 Implementation of the gating commands

It was found while setting up the lab tests that the gating commands generated by the used MCU were quite inaccurate compared to the desired values. This stems from the fact that even by using an ePWM clock frequency of 100 MHz, this leaves just 99 clock cycles for the TB sub-module of the ePWM to generate the gating commands, so the duty cycles created are not accurate. The same problem arises with the creation of dead time. Thankfully, the used MCU provides the ability to increase the resolution of the duty cycle and dead-band using its High-Resolution PWM (HRPWM) capabilities, as seen in Figure 6.12. The use of the HRPWM increases the pulse and dead-band resolution to sub-nanosecond levels using the Micro Edge Positioner (MEP) technology [126].



(a)



(b)

Figure 6.12: The C2000™ High-Resolution PWM block diagram (a). and the MEP technology used to achieve precise timing controls (b) [126].

The use of the same PWM modules and time synchronisation is used as in section 5.3.1. The HRPWM capabilities of the same PWM modules are enabled using some extra registers. The transition to HRPWM was facilitated by the included "Auto-Conversion Mode", which can be enabled in the MCU. If this operation mode is enabled, the MEP scale factor, as seen in Figure 6.12b, is calculated automatically without requiring extra code to achieve the duty cycle required. The calculation of the MEP scale factor is done by calling the scale factor optimisation (SFO) function, which determines the least amount of MEP steps to get the required accuracy.

In the results presented in this chapter, the high-resolution duty cycle control was enabled, as the converter under examination is duty-cycle controlled. Similarly, the high-resolution deadband was enabled. For all the ePWM registers used to provide commands to the active devices, the HRPWM edge control mode is on the rising edge, as an up counter is used. For the primary-side devices, a high-resolution deadband was enabled on the rising and falling edges, as complimentary EPWMA/B outputs feed the devices. For the secondary-side devices, a high-resolution deadband was only enabled for the rising edge, as an EPWMA output controls each of them.

6.4 Experimental Challenges & Results

Within the boundaries of the PhD timeframe, two 1 MHz converter prototypes were constructed. The first iteration couldn't be used to transfer power efficiently, as some oscillatory effects were seen in the primary-side devices during the dead-time periods. The problem statement and the avenues to avoid this effect are shown in the following sections. Afterwards, the second iteration of prototyping was shown to have more favourable behaviour while not wholly eliminating this phenomenon. Nevertheless, the converter is used to showcase the possibility of using the proposed converter with a 1 MHz switching frequency, and avenues to improve the design further are detailed.

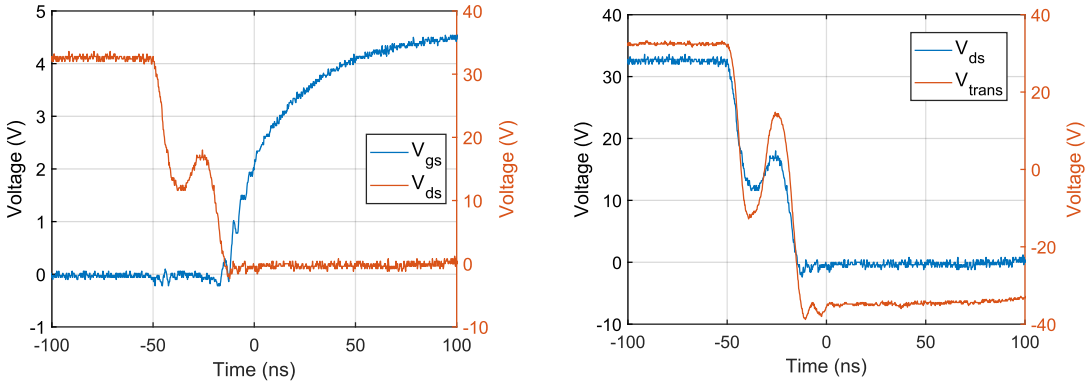


Figure 6.13: V_{ds} oscillation during the dead-time interval. This creates a long dead time to achieve ZVS (a) and also appears on the transformer's terminals as an oscillation (b).

6.4.1 Dead Time Oscillatory Effects

The first converter prototype couldn't be utilised to transfer the entire input power to the load due to thermal problems with the low-voltage GaN devices approaching their thermal limit. Upon inspection of the device waveforms in the dead-time period (V_{ds}, V_{gs}), it was found that the ZVS turn-on was not achieved. Furthermore, increasing the dead time, in theory, should allow for the realisation of soft-switching, but at the cost of a lower voltage step-up ratio and reduced efficiency power conversion, as a high dead time allows for a smaller period of power transfer compared to the overall switching period. This problem merits further investigation.

To begin the investigation, the problem must be first visualised. In Figure 6.13, the waveform of the lower device's V_{ds} is seen, along with the corresponding transformer voltage transition. It appears that there is an oscillation present centred around 0 V, as seen from the transformer's terminals. This slows down the realisation of ZVS turn-on considerably. Certain tests were performed to find the root cause of this phenomenon. To see how a change in transformer parameters affects this phenomenon, a change in the in-circuit leakage inductance was attempted. In the first revision of the converter, the planar transformer is connected by an arrangement of connection headers in an interleaved fashion, as can be seen in Appendix D.

The connection headers were removed from the primary side to change the leakage inductance of the transformer path. After this, the author made a direct

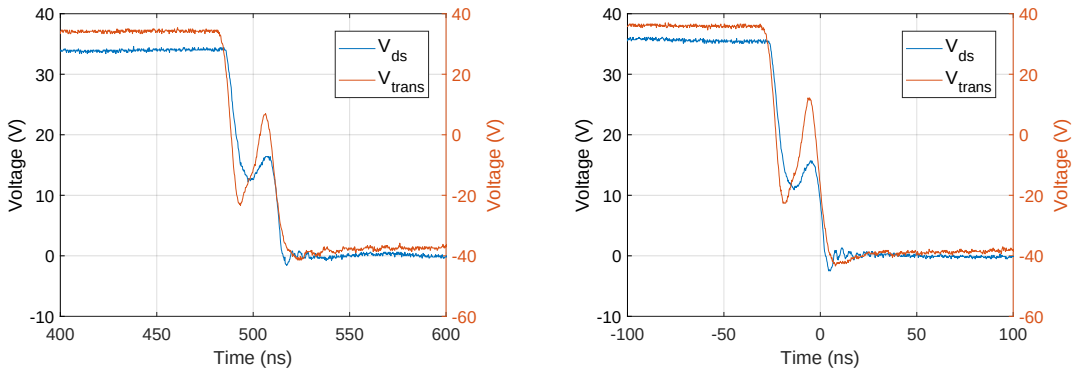


Figure 6.14: Shortening the transformer's connection to the PCB. The graph in (a) shows the waveforms before the shortening procedure, while those in (b) show the ones after the shortening.

solder connection to the pads, lowering the total path traversed by the current. The results for the same transformer, with the converter being in DCX mode with nominal voltage, may be inspected in Figure 6.14. Within that figure, it appears that the lowering of the leakage inductance does not have a positive effect. In fact, the amplitude of the oscillation increased slightly and didn't seem to have a measurable impact on the time it took to make the V_{ds} equal to zero. Therefore, the connection method of the PCB to the transformer isn't to blame.

After this test, other tests were devised. First, capacitors were added on the primary side of the transformer to try to lower its voltage transition rates. However, this aggravated the problem. What seemed to fix this ringing problem was when the author connected the transformer to the PCB via jumper wires, as seen in Figure 6.15. It was also seen that with a lower number of jumper wires in parallel, V_{ds} was dropping to zero more smoothly. Therefore, it appeared that an added inductance to the primary side aids the achievement of ZVS turn-on. Thus far, it seemed that this phenomenon was dampened by an increased leakage inductance and worsened by an additional capacitive load in the transformer's terminals.

At this point, it was evident that, somehow, the magnetising current was having some oscillation, based on the observations made above. Measuring the transformer's primary-side current was impossible due to its compact nature and the lack of forethought to include a current measurement point on the primary side. To find

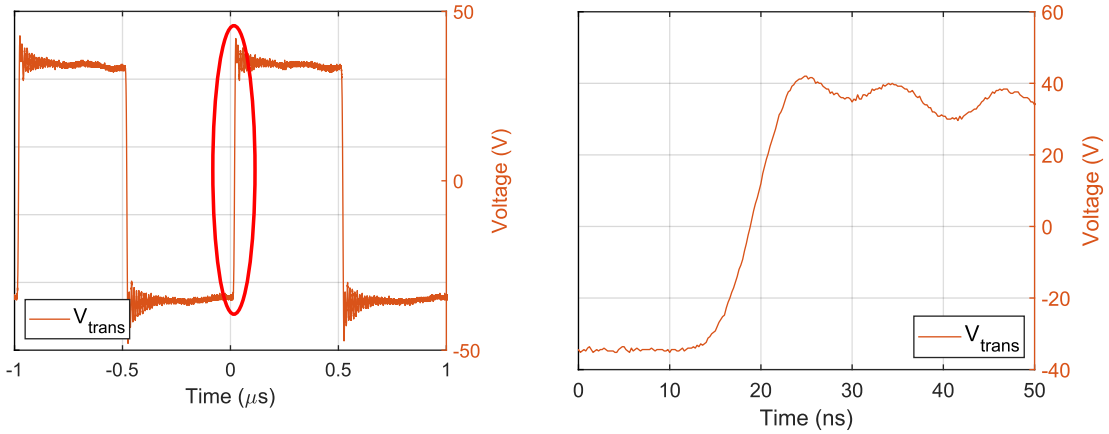


Figure 6.15: Smooth transformer voltage transitions, facilitated by 20 cm jumper wires.

another way to prove this point, the existing literature was surveyed to see if other researchers had faced this challenge.

The result of this search pointed out that this problem was analysed previously but had escaped the attention of the author [134, 135]. Based on the literature search, it appears that this is a common issue in high step-up DC-DC conversion systems and is owed to the high reflected values of the intrawinding and junction capacitances of the high-voltage side. The work by Wen [134] also showcases that the reverse recovery effect of diodes can cause the same problem, but as SiC Schottky diodes were used in this work, this possibility was dismissed.

Naturally, reducing the device junction capacitance is a double-edged sword. This would be achieved by selecting devices with higher $R_{ds,on}$, which would reduce the power conversion efficiency. Similarly, the transformer has already been designed with the least intrawinding capacitance possible for the available PCB stack-ups. Therefore, the author took two actions to face this dead time oscillation. First, the PCB layout on the first prototype was carefully examined for possible optimisation. Second, in the next iteration, pads are placed in series on the primary side of the transformer, with the intent to use them to increase the leakage inductance if needed.

Concerning the first part of the problem mitigation, an overlapping layer that might be removed was found. It concerns the connection of the secondary-side switch nodes to the DC-net and would appear as a parallel capacitance to the NV6115 devices. This exists because, initially, the magnetic cancellation layout was used to

provide a low commutation loop inductance and facilitate faster switching intervals for the NV6115 devices. This commutation loop was imported into the ANSYS Q3D environment and underwent capacitance/conductance solver testing. The end result is that there is indeed a strong capacitive coupling between these two nodes, and it is equal to $C_{par} = 10.8\,pF$. The device's effective output capacitance is approximately $C_{O,er} \approx 24\,pF$, so the increased capacitive load on the device's terminals is increased by nearly 50%.

To showcase the creation of this problem, an equivalent LTSpice circuit was made in Figure 6.16. The simulation uses the values found within this chapter for the intrawinding capacitance on the transformer's secondary side, the manufacturer provided junction capacitance for the upper-side diode, and the manufacturer provided output capacitance of the active devices augmented by the parasitic capacitance of the layout. The results of this simulation, seen in Figure 6.17, show that the magnetising current experiences a dip during the dead time. This current dip even causes the current to reverse polarity, therefore giving the characteristic transformer voltage oscillation. This dip is caused by the change of the topological state of the converter when the devices in the primary bridge are all in the off state, and mathematical analysis is performed in the previous works [134, 135]. The oscillation wasn't noticed in the previous converter designs due to the larger inductance values associated with the wire-wound transformer.

6.4.2 Revised Converter Results

In the second iteration of the converter, the switching half-bridge cell on the secondary side has been changed to a lateral layout. Using this layout, the parasitic capacitance C_{par} in parallel to the NV6115 devices should be near zero. Using the LTSpice simulation shown in Figure 6.16, it was seen that the dead-time oscillation was nearly diminished with the lowered capacitance on the secondary devices. However, it did decrease the level at which the V_{ds} started the oscillation, so overall, it had a positive effect.

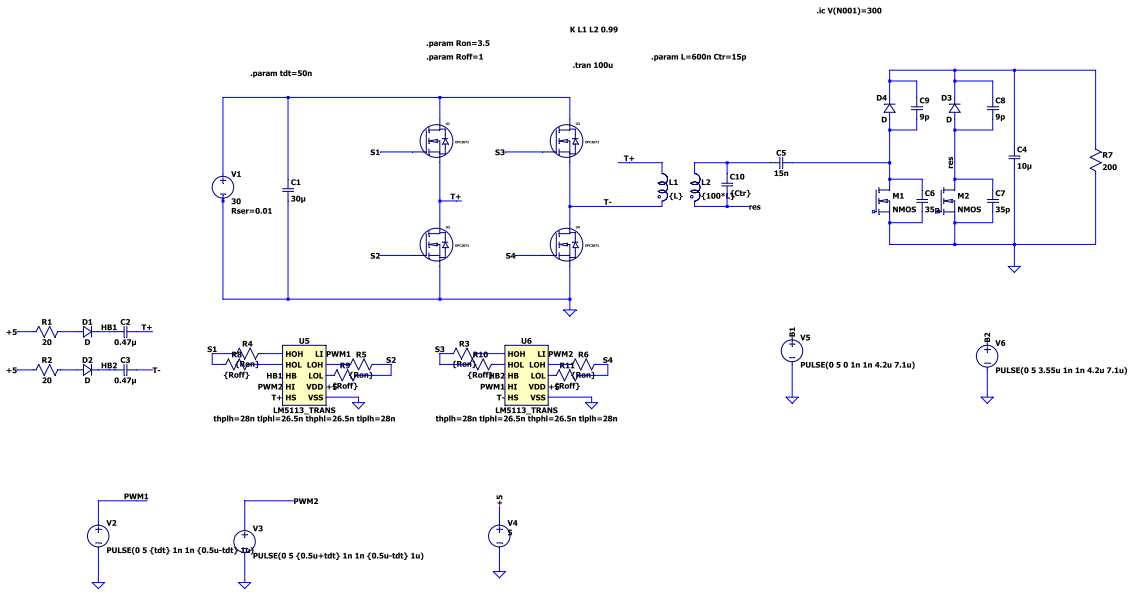


Figure 6.16: LTSpice model for the dead-time oscillation phenomenon.

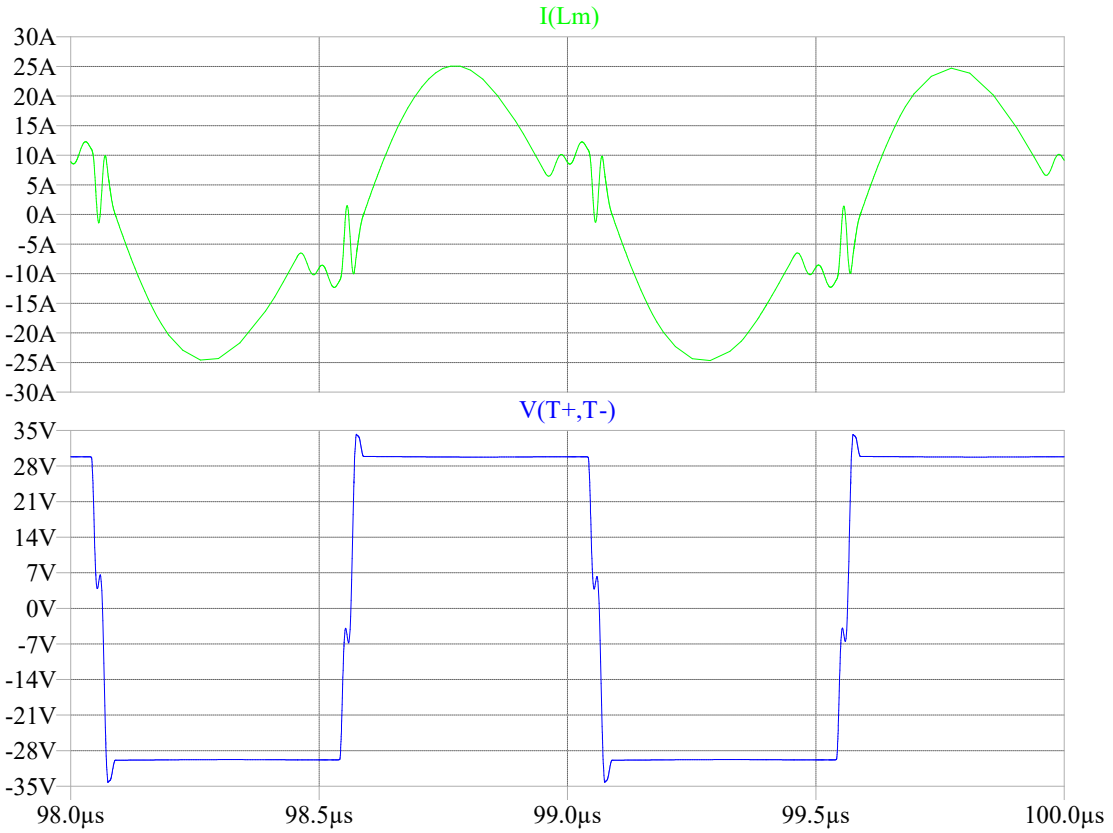


Figure 6.17: Resulting waveforms from the LTSpice simulation. It is seen that the magnetising current experiences a dip during dead time.

To further aid the inertia of the primary-side magnetising current during the dead-time periods, a pad was added to connect an inductor to the transformer's primary path. In the design phase, this was intended to be used to attach a ready-made CoilCraft inductor from their XGL series, which possesses low losses and high-frequency operation. In practice, two things were noted when this was attempted to improve the performance. First, selecting their smallest packages with a low inductance while aiding the converter to achieve ZVS was unacceptable to be used due to thermal constraints. While the dead-time waveforms improved, the small packaging likely has a considerable thermal resistance, so attempting to pass the total power through it led to overheating. Second, their larger-sized XGL packages were tested, which fixed the overheating issue even with similar resistive values. However, their larger inductors also possessed higher inductance, which acted as a voltage divider to the transformer, providing a considerably reduced voltage step-up.

A compromise was made, which may be seen in the photo of the converter in Figure 6.10 by using a piece of 0.1 mm copper foil to add a small amount of added inductance, with minimal resistance increase. This was found to assist the V_{ds} transition towards zero, but it was not enough. This led to further simulation investigations, as with the model made in Figure 6.16, a small added inductance in the order of a couple of nano henries seemed to eliminate the ringing issue. Therefore, it was decided to examine the effect of the interwinding capacitance of the transformer on the operation of this converter. To this end, the simulation schematic shown in Figure 6.18 was examined. In this schematic, a simple transformer simulation was used, in which the total interwinding capacitance is equally split in the top and bottom terminals of the transformer.

In the transformer that was designed and ordered, the total interwinding capacitance was found to be 223 pF, which means an equal split of around 111 pF in each interwinding capacitance of the simulation model of the transformer. It was found that using the transformer's value for the interwinding capacitance, the behaviour of the converter in the LTSpice model deteriorated. The dead-time requirements

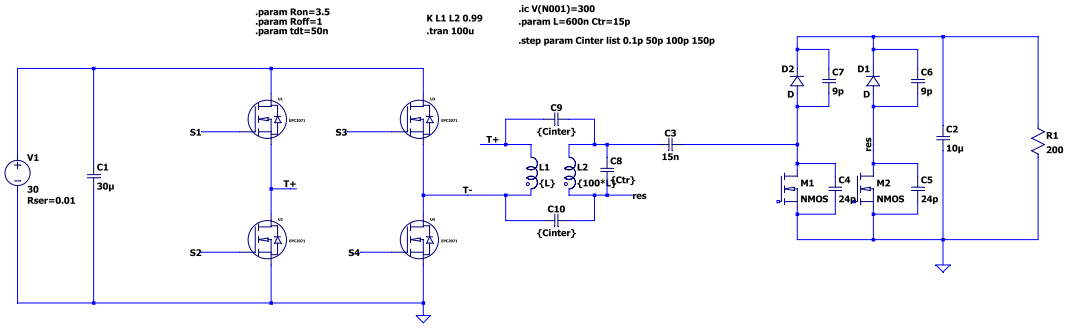


Figure 6.18: LTSpice simulation inclusive of the transformer interwinding capacitances.

increased, and so did the amplitude of the dead-time oscillation. To showcase this, a sweep of different interwinding capacitance values was run, and the resulting waveforms can be seen in Figure 6.19.

Looking at the waveforms in Figure 6.19, the increased amplitude of the voltage oscillations with the increased interwinding capacitance may be seen. This is caused by an increased oscillation amplitude in the magnetising current, as seen on the primary side of the transformer, during the dead time period. Furthermore, this increased oscillation also leads to a different initial current value when the conduction period starts. This changes the required LC filter from the designed value, as may be seen from the waveforms, further complicating the design process.

Inspecting the LTSpice results, we see that this phenomenon seems to be owed to the displacement currents flowing via the interwinding capacitances. Therefore, in theory, a shielding scheme should resolve this big issue in the next iteration of this prototype by returning the displacement currents to the primary side of the converter system. Unfortunately, due to the finite time available for this work, this will be attempted at a later time. For the results shown in this chapter, this problem is not addressed, but valuable proof-of-concept results have been acquired. The increased inductance owed to the copper strip used in the transformer path, along with suitable dead-time timing to allow for turn-on during the valley of the V_{ds} oscillation, permitted the operation of the converter with the total input power, albeit at heightened temperatures and, therefore reduced efficiency, due to partial ZVS turn-on of the primary-side devices. Adding to the additional losses due to

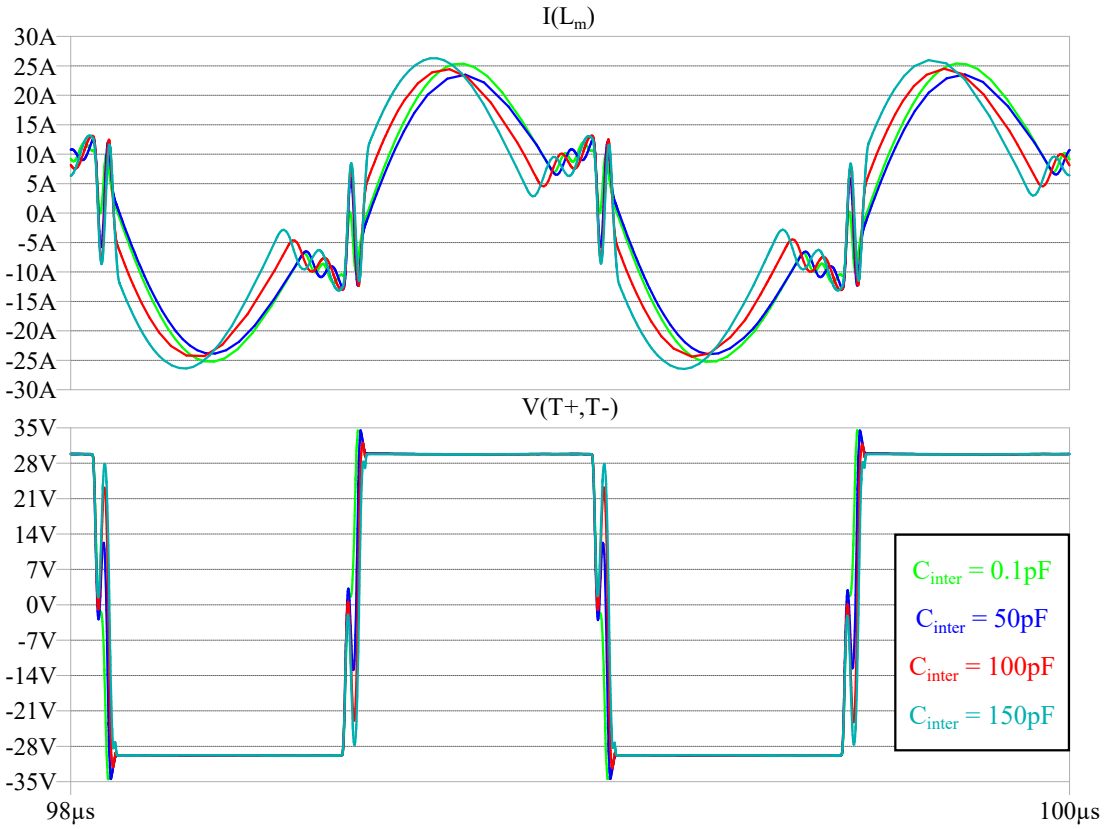


Figure 6.19: LTSpice converter operation for various interwinding capacitance values.

partial ZVS are the increased transformer copper losses due to a non-optimal copper weight trace to accelerate the development time.

With the discussed problem still in place, the converter was tested, and its operational waveforms are presented below. The converter was using a resonant capacitance of 9.4 nF, and the resonant inductance was 2 μH from the leakage inductance of the transformer, plus the PCB trace inductance from the primary-side. As was done in the previous chapter, the ZVS behaviour is first presented. The presented waveforms are taken in the DCX mode in the nominal power rating, as the mechanisms of ZVS stay consistent in the other two operational modes.

Concerning the ZVS turn-on behaviour of the primary side devices, the waveforms shown in Figure 6.20 have been acquired. As analysed in this chapter, unfortunately, even with the increased leakage inductance added to the circuit, the complete transition of V_{ds} to zero wasn't achieved without oscillations. Instead, what was done was to fine-tune the circuit via trial and error. This was done by trying different

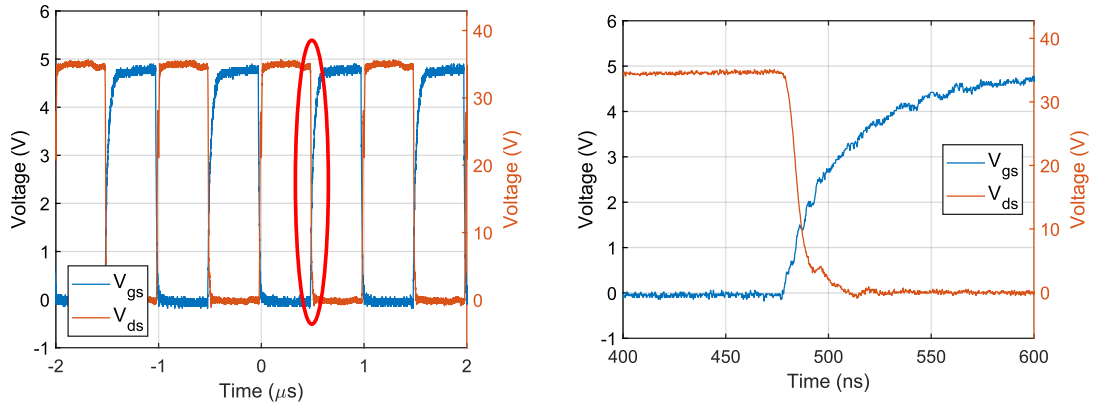


Figure 6.20: Low-side primary-side device V_{ds}, V_{gs} shown in (a). In (b), it may be seen that the device achieves near ZVS.

dead-time intervals until it was found that the gate threshold voltage (in this case, it is approximately 1.6 V) was crossed at the same time as the valley in the oscillation of V_{ds}. This results in a relatively acceptable near-ZVS transition without requiring extensive dead-time periods.

Concerning the ZVS turn-on behaviour of the secondary-side active devices, the captured waveforms may be inspected in Figure 6.21. When examining the soft-switching behaviour of this device, no strange phenomena were observed, as the magnetising current doesn't affect its ZVS behaviour. Instead, the ZVS turn-on is primarily achieved by the resonant inductance, which, in this case, is relatively small. For this reason, the V_{ds} drops to zero considerably faster compared to the previous prototypes. The only issue observed with this device was some overheating, which was easily troubleshooted. The overheating was caused by the considerably large -in the context of a 1 MHz converter- third quadrant conduction time. As the NV6115 device has an integrated gate drive, the actual switching interval is delayed compared to the viewed waveforms on the oscilloscope. Therefore, the delay data acquired from Chapter 4 had to be used to lower the excessive dead-time losses by providing accurate dead-time tuning.

Another check that had to be implemented was that the converter was designed to be as balanced as possible. The primary concern for the designer was the equalisation of the parasitic inductance on the primary side for each half-period. If the design

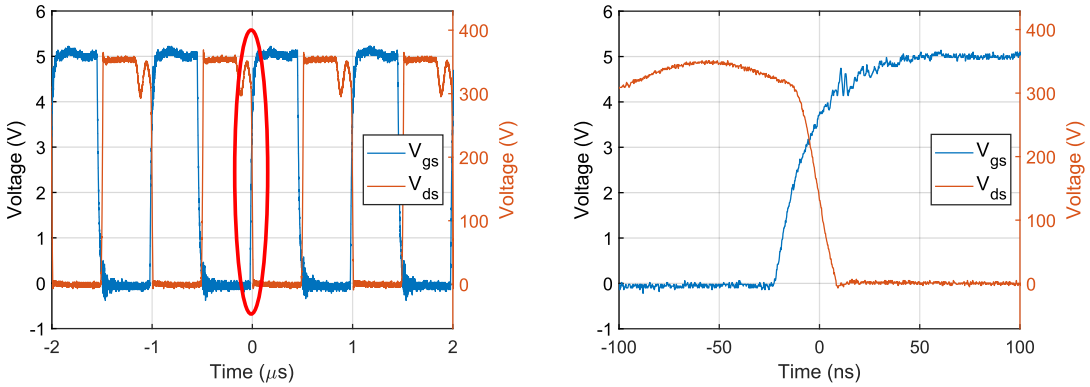


Figure 6.21: Low-side secondary-side device V_{ds}, V_{gs} shown in (a). In (b), it may be seen that the device achieves ZVS turn-on.

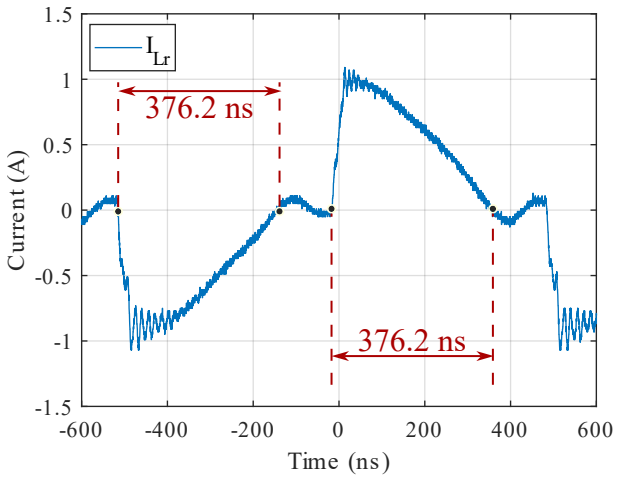


Figure 6.22: Symmetric resonant current conduction times.

is done correctly, the conduction periods, as seen on the secondary-side inductance, will be symmetric and conduct for the same time. Therefore, the converter was run in its DCX mode, and the current waveform was examined using a Tektronix TCP312A current probe on a small wire connected in series to the transformer's secondary path. The results of this test, seen in Figure 6.22, show good symmetry in terms of conduction time for each half-period. The noise within these waveforms is asymmetric, and this is suspected to be caused by the intense effects of the interwinding capacitances of the transformer.

Finally, some of the operational waveforms of the converter have been captured to show the feasibility of the proposed converter in a high-frequency operation. The converter was run with a 350 V output voltage, and a suitable input voltage was

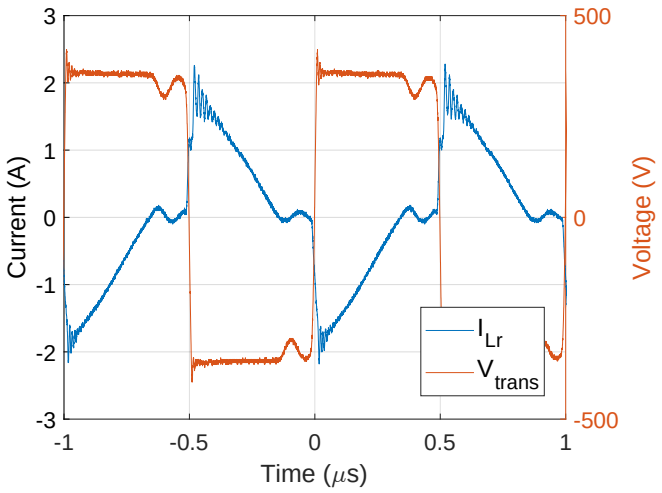


Figure 6.23: 1 MHz converter - Example DCX waveform.

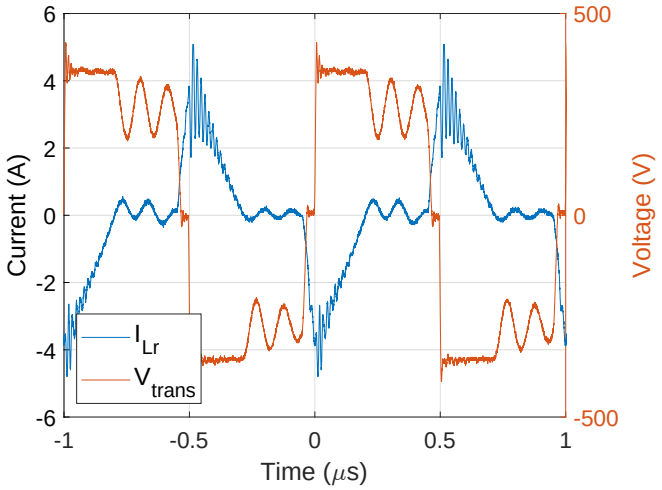


Figure 6.24: 1 MHz converter - Example Voltage Boosting waveform.

given to show the operation. The converter was run at full input power, that is, 300 W for the DCX and Voltage Boosting modes and 200 W for the Greinacher mode. These waveforms may be found in Figures 6.23, 6.24 and 6.25. It may be noted that the resonant tank current is considerably more noisy compared to the design with the wire-wound transformer due to the increased interwinding capacitances. Similarly, because of the mentioned capacitances, it was challenging to make the current spread over a high percentage of the operating period. An exception to this is the Greinacher mode, which showed less noisy current signals due to the smaller voltage transient effects on the primary side, leading to smaller amounts of displacement currents in the transformer.

Finally, the performance of the designed converter was examined using the

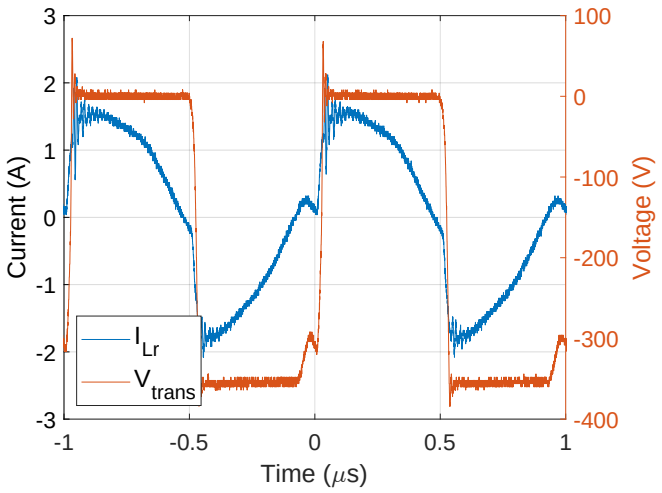
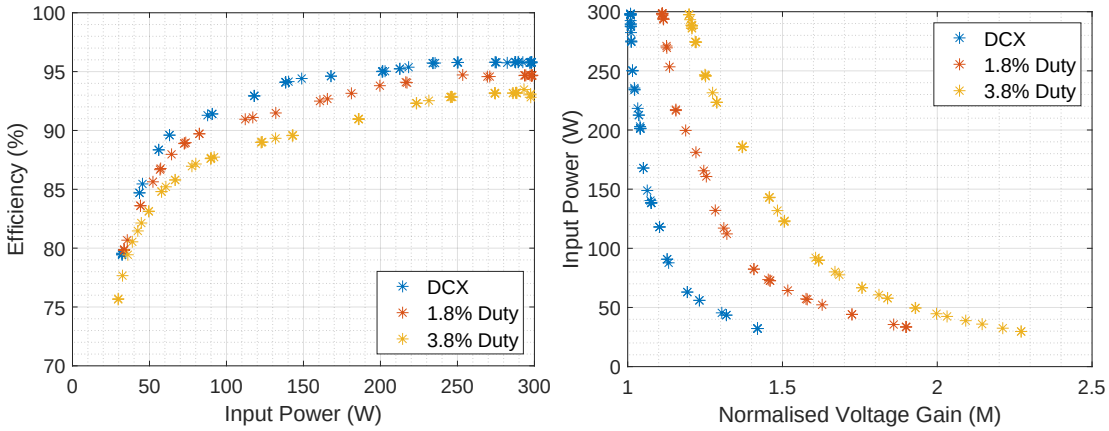


Figure 6.25: 1 MHz converter - Example Greinacher waveform.

PPA5530 precision power analyser in the same way as in the previous chapter. The results of these tests can be seen in Figures 6.26 and 6.27. The decreased efficiency, which was mentioned before, can be easily seen by the efficiency charts, with the major causes of this being the near-ZVS of the primary devices, the high winding resistances of the used transformer, plus displacement current effects. The near-ZVS behaviour is expected to present a constant additional power loss, so it particularly degrades performance at low power levels, which can be witnessed in the results that were retrieved. Furthermore, results with higher duty cycles are not taken, as the devices would increase their temperatures to dangerous levels, so a limited dataset is presented.

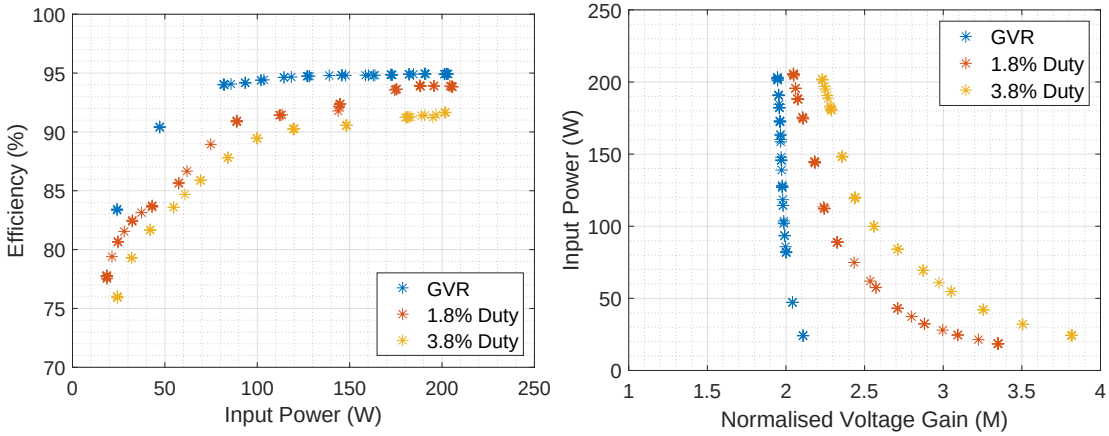
Another notably peculiar result is that the converter provides considerable voltage step-up in the DCX mode at low power levels. It is suspected that this is owed to the effects of the displacement currents, which alter the starting current of the resonant tank, as seen in the LTSpice simulations. This belief is further cemented by seeing that this effect is less pronounced in the Greinacher mode, where the created displacement currents are lower, and the voltage step-up with varying power stays more constant,

Overall, the designed converter, while not perfect in its current form, shows potential to become an attractive proposition with further work. The last aspect that has yet to be examined in this chapter is the potential to shrink the converter



(a) **(b)**

Figure 6.26: Experimental efficiency (a) and voltage step-up (b) in the Voltage Boosting mode. The results were acquired using the PPA5530 power analyser, and data points were plotted as asterisks.



(a) **(b)**

Figure 6.27: Experimental efficiency (a) and voltage step-up (b) in the Greinacher mode. The results were acquired using the PPA5530 power analyser, and data points were plotted as asterisks.

down. To this aim, the 3D models of the latest versions of available PCBs in Altium Designer are compared. This comprises the third iteration of the low-frequency converter and the second iteration of the high-frequency converter, both of which may be seen in detail in the appendices of this work.

The lateral dimensions of the PCB are not worthy of examining, as the wire-wound converter also has added components to enable further extensions of the work presented here, which the 1 MHz version does not. Nevertheless, a slightly smaller area will be required in the higher frequency converter, primarily because of the reduced need for energy storage capacitors. The critical metric is the height of the

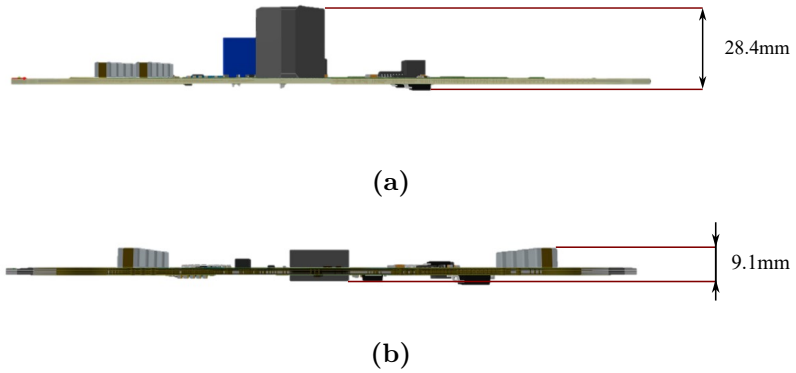


Figure 6.28: The converter expected heights, with (a) being the designed lower frequency converter and (b) the 1 MHz conversion system.

converter system because this is the current bottleneck for BIPV, as mentioned in the introductory chapter. It may be seen in Figure 6.28 that in the wire-wound transformer converter, the total height is about 28.4 mm, while for the planar transformer-based converter, it is 9.1 mm.

If we consider two converters with similar lateral dimensions and the same power rating, the power density is improved by a factor of three. For the examined 1 MHz converter, the achieved power density is approximately equal to 3 kW/L. The allure of high-frequency switching can now be clearly seen, as the converter height has shrunk considerably using the same topology. It is also worth noting that this thesis has improved the state of the art in the area. From the converters examined in the literature, the slimmest solution was the one proposed by Zhao, which had a height profile of approximately 12 mm.

6.5 Summary

In this chapter, the aim was to increase the switching frequency of the proposed converter to achieve a slim design. A matrix planar transformer was designed, and different problems that arise from the design of planar magnetics were analysed. Furthermore, additional layout guidelines are provided compared to the previous sections, tailored to higher frequency power conversion. Plus, the rarely discussed problem of dead-time oscillation has been presented, and solutions have been proposed to mitigate this problem. The presented converter does not possess favourable performance within this chapter, but solutions to improve its performance have been given. Overall, this chapter has contributed to a deeper understanding of the phenomenon of dead-time oscillation and PCB layout, plus it has proposed a slim 300 W converter that exceeds what has been achieved before in terms of height profile.

Chapter 7

Conclusions and Further Work

With the use of fossil fuels being gradually phased out due to environmental and security concerns, solar energy is expected to experience huge growth. In the residential market segment, PV panels with integrated module-level power electronics are also expected to grow due to their energy harvesting efficiency, scalability, and fault tolerance. This thesis has worked on the parallel type DC power optimiser, which is meant to be used in this application area. The proposed converter in this work can be used to connect a PV panel to a DC microgrid, an inverter's DC-link, or as the first stage in a two-staged microinverter. The designed converter has shown good power conversion efficiency and low-temperature rise in tests with a wide input voltage, making it a promising solution for a wide range of applications.

The breakthrough efficiency achieved over a wide load range and a broad voltage input allowed for a high-performing general-purpose parallel-type power optimiser. Furthermore, due to the unprecedented slim profile of this converter, it opens the pathway to panel integration, which is beneficial, especially for BIPV applications. This way, the cavity in the building envelope, which is typically used to prevent the solar panels from overheating by allowing ventilation to occur, may also be used to remove some heat from the conversion system. As was seen in the introduction of this thesis, the converter shut down due to excessive heating for safety reasons, which is the primary factor that prevents the extraction of solar energy. Therefore, the integrated, high-efficiency converter studied in this thesis could be a potential

breakthrough for extracting energy from BIPV applications.

Plus, even when considering the typical residential PV panel architecture, the proposed solution of integrating the conversion system with the panel allows for easier wiring, shorter installation times, easy scalability of the system and increased fault tolerance. This also includes the benefit that is owed to the converter's wide regulation range; the individual panels will now be shade-tolerant, so they can be used effectively even when partially shaded, which isn't usually the case. Nevertheless, the increased cost owed to the higher number of electronic components must be off-scaled by the expected lifetime energy generation gains. This can be examined on a case-by-case basis according to the place of installation and the expected insolation data, plus the local tariffs for electric power.

7.1 Main Contributions

The work has improved the understanding of the available solutions for parallel-type DC optimiser converters and provided new insights on using Gallium Nitride devices within their context. The contributions this piece of work provides can be summed up in the following list.

- Chapter 2 provides a critical investigation of existing solutions for parallel-type DC optimisers.

- Chapter 3 proposes a topology-morphing resonant converter and its gating method to be used for solar module-level applications. A thorough examination of its operation is performed, in addition to the inclusion of design guidelines.

- Chapter 4 confirms the validity of the stored energy in the EPC2021 device junction capacitances, further cementing its applicability to the soft-switching converter systems. Plus, novel experimental data on the switching performance have been provided for the NV6115 and GS66502B GaN HEMT devices. Issues concerning the dynamic characterisation of GaN devices, such as the current

signal degradation and the influence of the sensing equipment, which are rarely found in the literature, have been identified, and solutions have been proposed.

- Chapter 5 provides PCB assembly insights for in-house reflow work that are rarely found in the literature. Furthermore, specialised layout advice for using GaN HEMTs is included, and the proposed converter is successfully verified for its operation and performance in a laboratory setting, achieving breakthrough power conversion efficiencies (98.5%) and a low-temperature increase whilst in operation. This desirable performance is extended over a variety of input voltages and power levels thanks to the converter's inherent ability to achieve soft-switching over the whole operational voltage range.

- Chapter 6 provides additional layout guidelines focused on high switching frequency conversion systems. A little-known problem when paralleling turns in planar transformers, which is the potential uneven current sharing, is shown and explained, and guidelines for planar transformer design are given. Concerning the operation of the high-frequency converter, another less-known issue, dead-time oscillation, is presented. While existing literature has proposed that parallel-style capacitances (intrawinding & device junction capacitances) are the culprit behind this behaviour, this thesis showcased how interwinding capacitances accentuate this problem and cause unexpected resonant current behaviour. Finally, the operation of the converter at a 1 MHz switching frequency is displayed. It is also noted that a considerable reduction is achieved in the converter height, making it a promising candidate for BIPV applications or PV panel embedding in general.

7.2 Limitations and Suggestions for Further Improvements

Naturally, there is still scope for various improvements based on this thesis. The most obvious improvement comes from the application of newer GaN devices, as

at the time of performing this work, GaN devices were far from their theoretical performance limits. Already, a mere few years after starting this work, breakthroughs have been made in device performance, such as the low-voltage EPC2361, which is suitable for the examined application. It features considerably reduced $R_{ds,on}$ to minimise losses, and it offers a package better suited to apply a heat-spreader on top effectively. This would reduce primary-side conduction losses and allow for better temperature performance of the transformer and primary-side devices. This would provide a lower temperature rise during operation, which translates to a more rugged converter in high-temperature scenarios such as those examined in this work. Similar improvements can be found in newer 650 V GaN HEMTs and SiC Schottky diodes.

In terms of research explorations, it is worth expanding this work by testing various MPPT algorithms on the proposed converter. It is also worth researching how to effectively provide closed-loop control when faced with a switching frequency of 1 MHz, which leaves the MCU with little computational headroom between the switching events. It is also worth performing more thorough research into the effects of transformer parasitic capacitances when facing an isolated high-voltage step-up converter system. In this thesis, the problems caused were highlighted, but an in-thorough analysis is currently missing from the literature and, due to time constraints, was not pursued.

Finally, in terms of system-level extensions, it would be worthwhile to perform case studies in real PV applications to examine the proposed conversion system's energy and financial benefits. It's also worth extending this work with communication protocols, such as algorithms to diagnose problematic PV panels that require maintenance attention and protection mechanisms to perform rapid voltage shutdown during faults.

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Appendix A

Double Pulse Testing PCBs

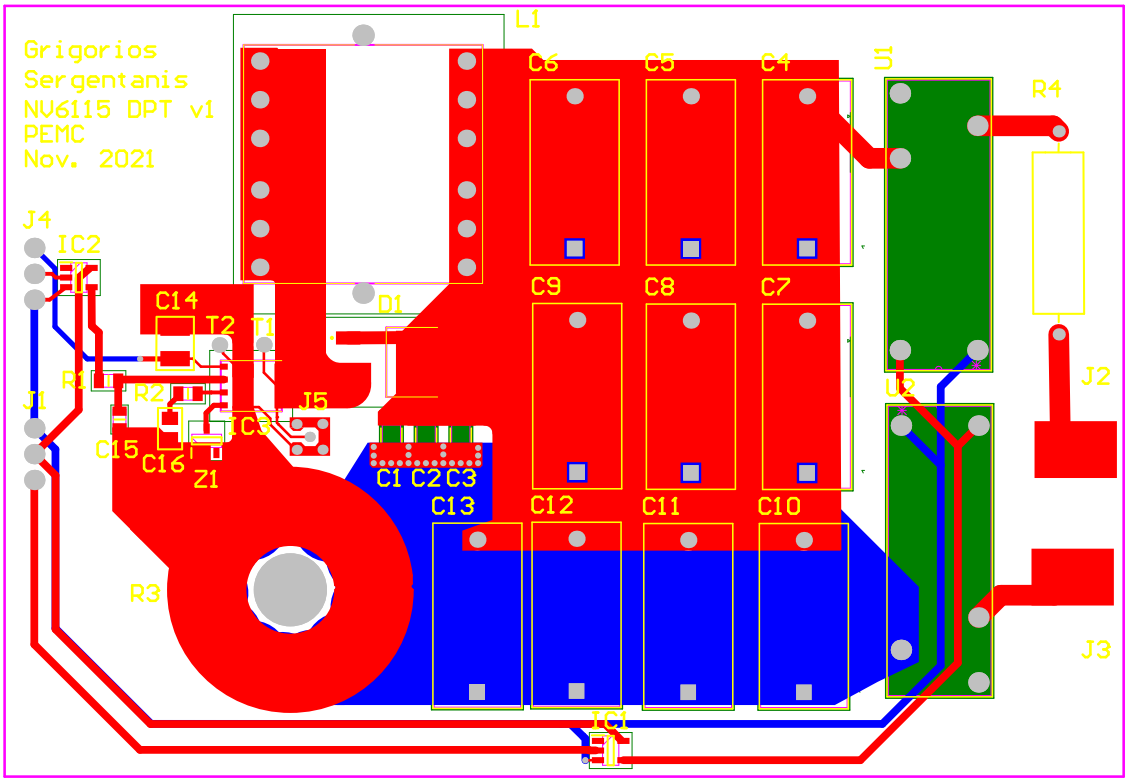


Figure A.1: Navitas DPT board - Version 1.

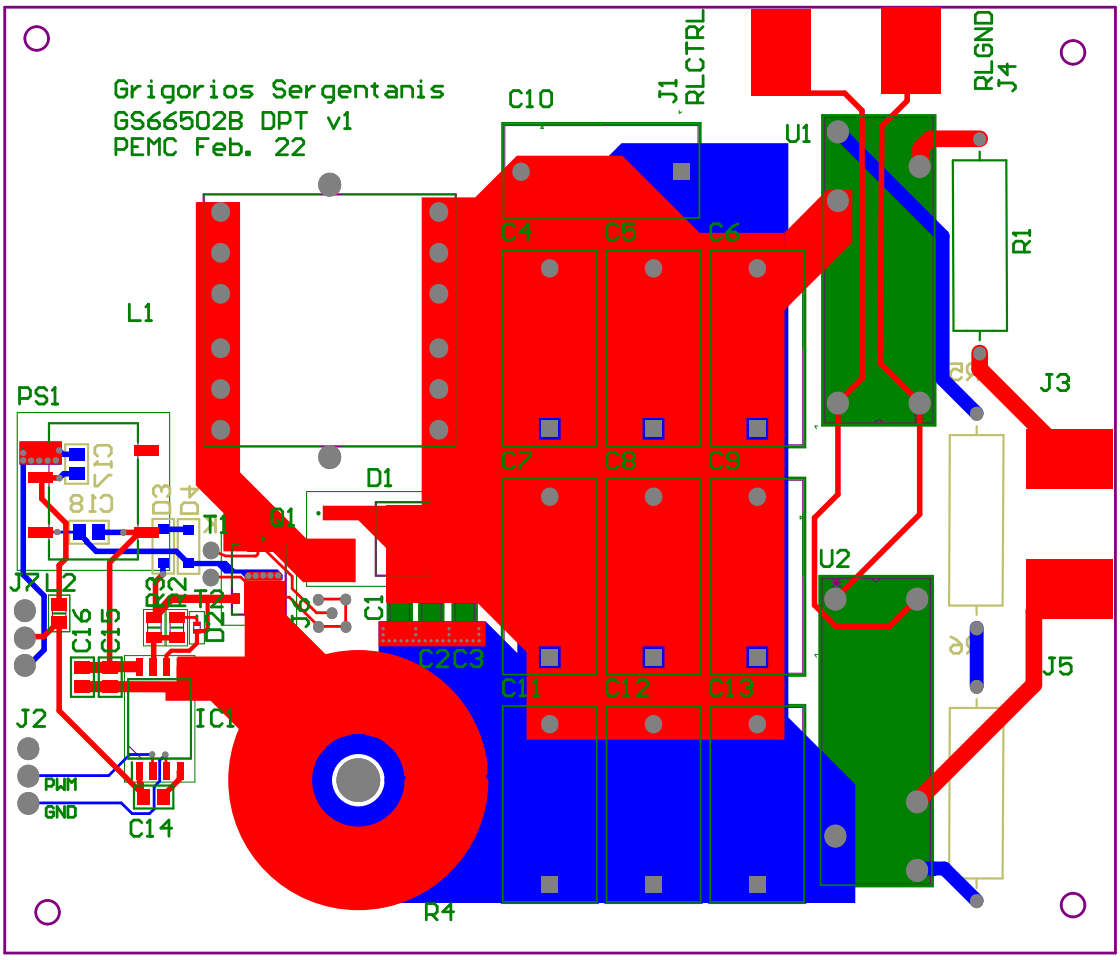


Figure A.2: GaN Systems DPT board - Version 1.

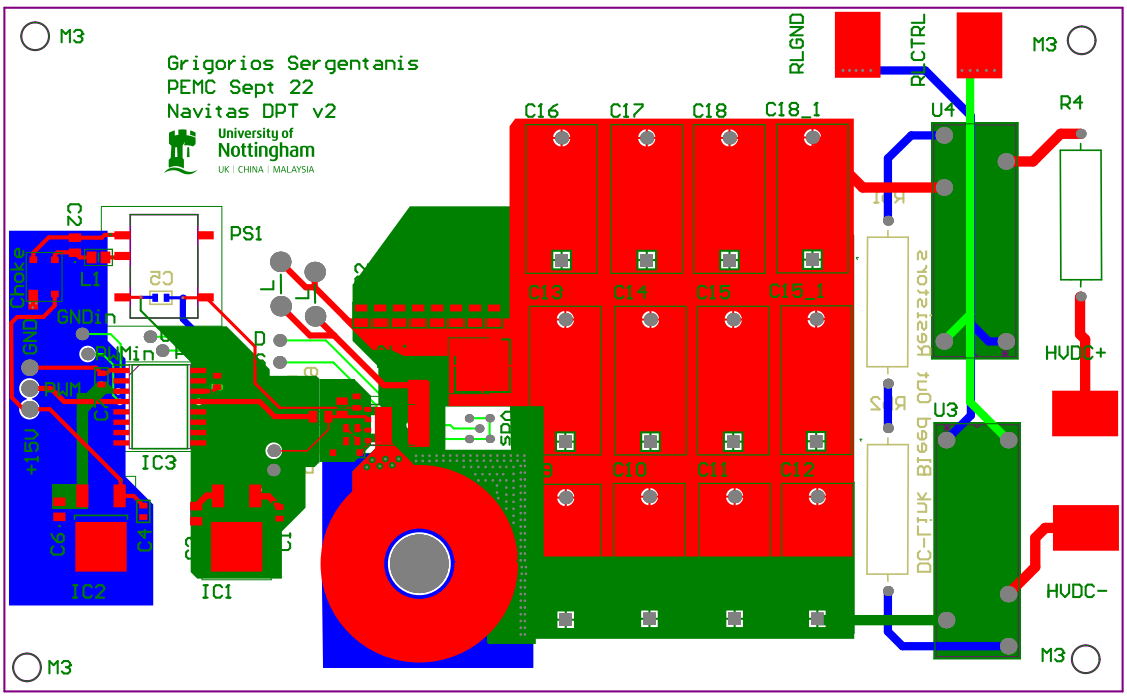


Figure A.3: Navitas DPT board - Version 2.

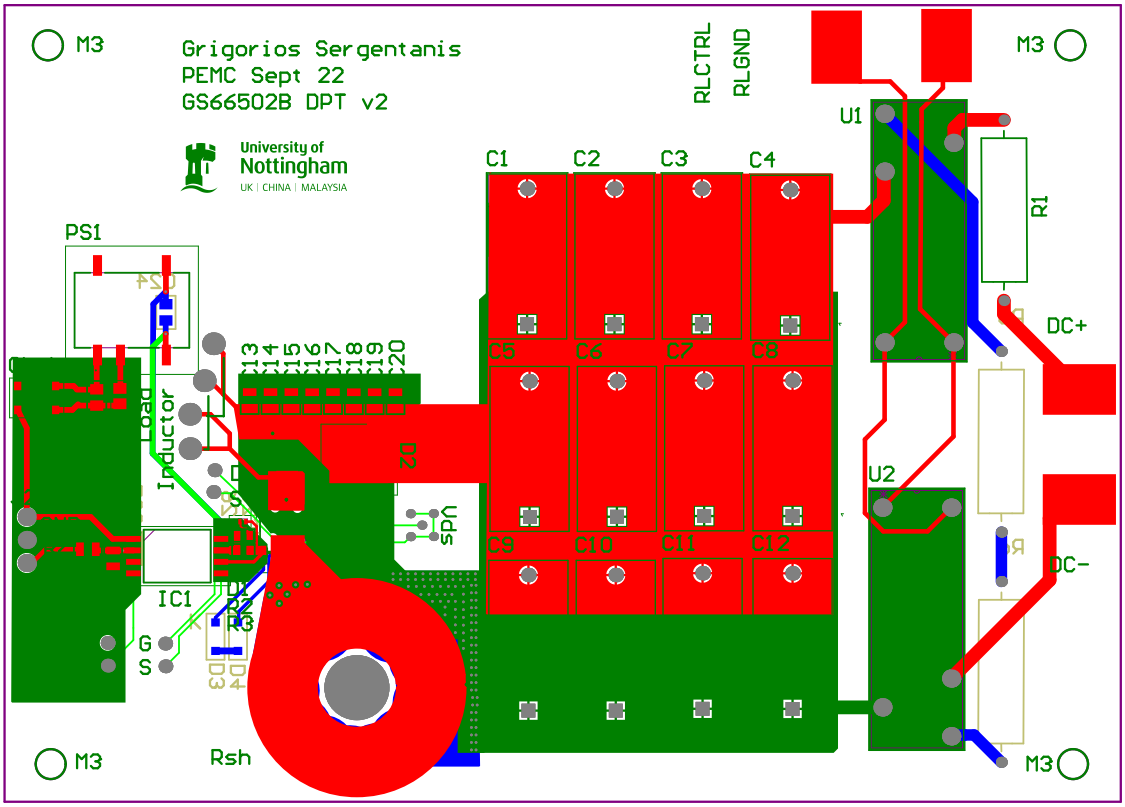


Figure A.4: GaN Systems DPT board - Version 2.

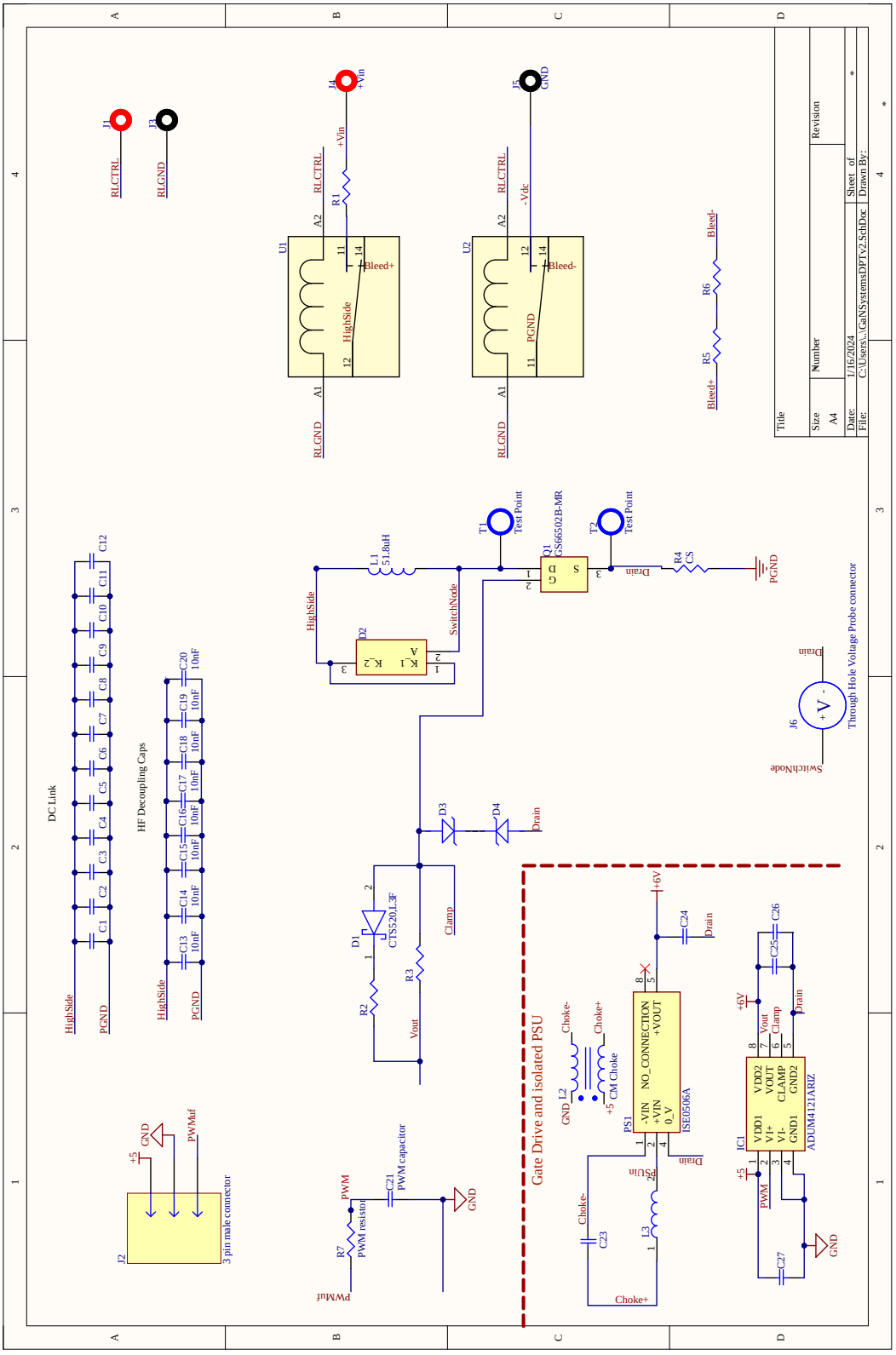


Figure A.5: GaN Systems DPT Schematics.

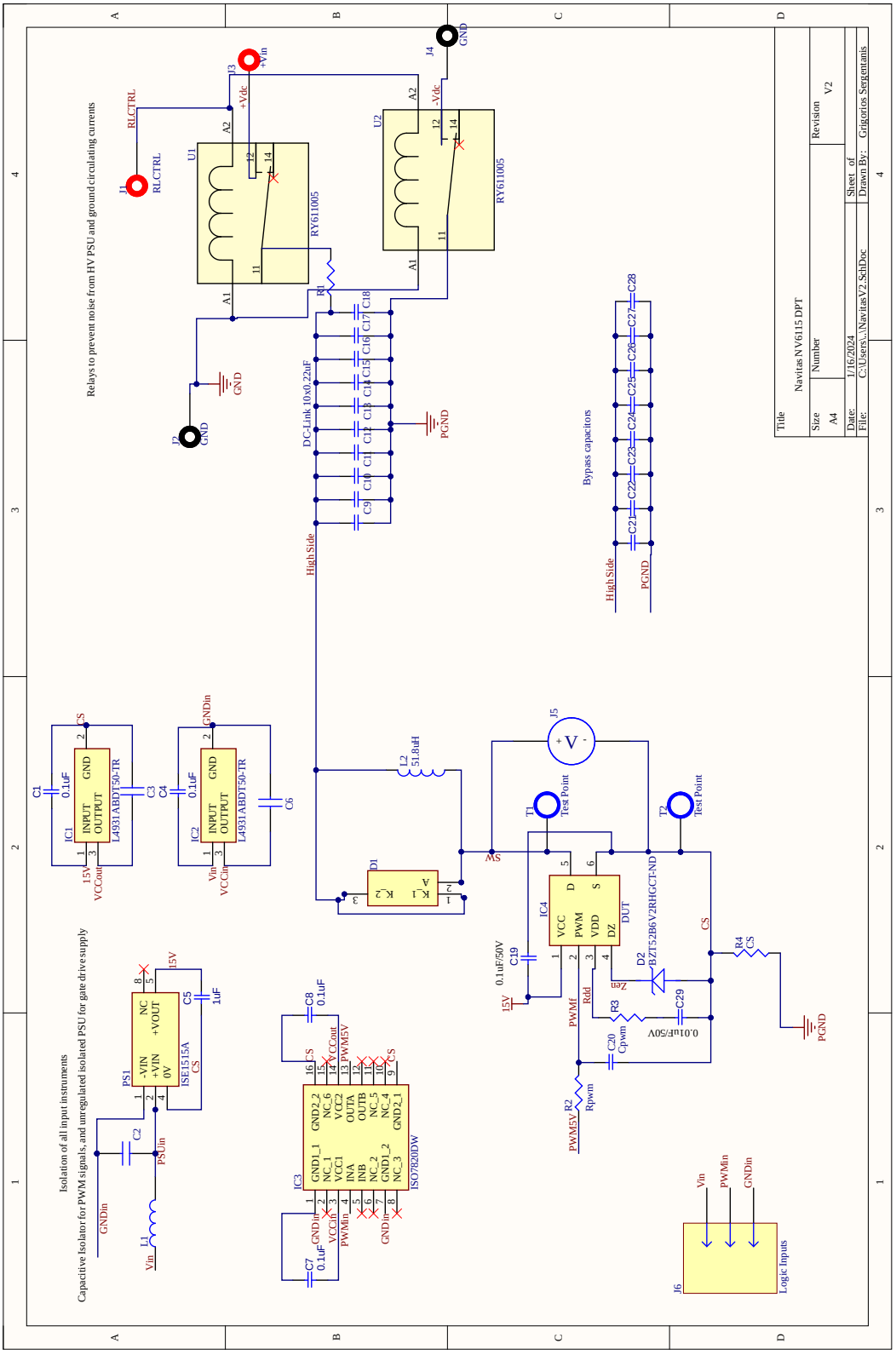


Figure A.6: Navitas DPT Schematics.

Appendix B

Double Pulse Testing Post-Processing Scripts

DPTResults.m

```
%% Run the dynamic DPT analysis on all the files in the folder.
%
%  Creator: Grigorios Sergentanis

files = dir('*.csv');           % Load all the CSV files captured
temp = struct2cell(files);      % in the folder
fileName = temp(1,:);
size = length(fileName);

tr = zeros(1,size);             % Initialize the variables to be stored for
tf = zeros(1,size);             % faster looping.
% dVp = zeros(1,size);
% dVn = zeros(1,size);
Eon = zeros(1,size);
Eoff = zeros(1,size);
over = zeros(1,size);
I = zeros(1,size);

for i = 1:1:size
    [tr(i),tf(i),Eon(i),Eoff(i),over(i),I(i)] = dynamicDPT(char(fileName(i)));
end

clear files temp fileName size
[~,name,~] = fileparts(pwd);
Folder = fullfile(cd,'..');
save(fullfile(Folder,name))
```

dynamicDPT.m

```
function [ tr, tf, Eon, Eoff, over,I ] = dynamicDPT(fileName)

% Analyzes DPT data gathered from DPO4xxx tektronix oscilloscopes (two
% channels, CH1 being voltage and CH2 current)
% Nov 2022 update: CH3 is the gate-source signal, and will be used to
% measure the time delays between turn-on and turn-off signals
% Creator: Grigorios Sergentanis

% close all

%% Read data from the CSV file, can be changed according to test rig
table = readtable(fileName);
time = table{:,4};
voltage = table{:,5};
current = table{:,11};
gate = table{:,17};

% Compensate the current DC Bias, owed to the scope needing professional calibration.

levels = statelevels(current);
current = current - levels(1);
levels = statelevels(current);

CurH = levels(2);
CurL = levels(1);

levels = statelevels(voltage);
VolH = levels(2);
VolL = levels(1);

%% Eon and Eoff measurements
power = voltage.*current;

[~, locs] = findpeaks(power,time,'Npeaks',4,'SortStr','descend','MinPeakDistance',80e-9,'MinPeakWidth',1e-9);

index = zeros(4,1);

for i = 1:4
    index(i) = find(time==locs(i)); % return the peak indices
```

```
40 end
41
42 temp    = sort(index); % lower index means lower time
43 first   = find(index==temp(1)); % get the index for the
      corresponding event
44 second  = find(index==temp(2));
45 third   = find(index==temp(3));
46 fourth  = find(index==temp(4));
47
48 %% Eoff Calculation
49
50 temp = index(second); % vector index of high current
      switching transition
51 dVp = (voltage(temp)-voltage(temp-1))/(0.2);
52 while 1
53     temp = temp - 1;
54     dVp(2) = (voltage(temp)-voltage(temp-1))/(0.2);
55     if dVp(2)>dVp(1)
56         dVp(1) = dVp(2);
57     end
58     if voltage(temp)<3
59         OffL = temp; % start of integration limits
60         break
61     end
62     if temp<=0
63         break
64     end
65 end
66 I = current(OffL-50);
67 % Now TEMP is located at the start of the time period of
      interest. Now it
68 % is increased until the current has dropped close to
      zero
69 while 1
70     temp = temp + 1;
71     dVp(2) = (voltage(temp)-voltage(temp-1))/(0.2);
72     if dVp(2)>dVp(1)
73         dVp(1) = dVp(2);
74     end
75     if current(temp) <= (0.02*I)
76         OffH = temp;
77         break
78     end
79     if temp >= 1000000 % 1M data points in total
80         break
81     end
82 end
83 maxrise = dVp(1);
```

```
84
85  Eoff = trapz(time(OffL:OffH),power(OffL:OffH));
86  temp = [time(OffL) time(OffH)];
87  OffL = OffL-75;  % Increase time frame for plotting.
88  OffH = OffH+75;
89
90  %% Plot the Eoff calculation Window
91
92  figure('Name', 'Turn Off Transition', 'NumberTitle','off'
        );
93  subplot(2,1,1)
94  plot(1e9*time(OffL:OffH),voltage(OffL:OffH));
95  ylabel('V_{ds} (V)')
96  yyaxis right
97  plot(1e9*time(OffL:OffH),current(OffL:OffH));
98  ylabel('I_{ds} (A)')
99  xlabel('Time (ns)')
100 title('Device Switching Waveforms',FontSize=12)
101 ax1 = gca;
102 xline(1e9*temp(1),'--r','LineWidth',1,'Label','Start');
103 xline(1e9*temp(2),'--r','LineWidth',1,'Label','Stop');
104 subplot(2,1,2)
105 plot(1e9*time(OffL:OffH),power(OffL:OffH));
106 ylabel('Power Loss (W)')
107 xlabel('Time (ns)')
108 title('Device Instantaneous Loss',FontSize=12)
109 ax2 = gca;
110 linkaxes([ax1 ax2],'x')
111 xline(1e9*temp(1),'--r','LineWidth',1,'Label','Start');
112 xline(1e9*temp(2),'--r','LineWidth',1,'Label','Stop');
113 xlim(1e9*[time(OffL) time(OffH)])
114
115 %% Eon Calculations
116
117 temp = index(third); % vector index of high current
        switching transition
118 dVn = (voltage(temp)-voltage(temp-1))/(0.2);
119 index = 0;
120 while 1
121     temp = temp - 1;
122     dVn(2) = (voltage(temp+1)-voltage(temp-1))/(0.2);
123     if dVn(2)<dVn(1)
124         dVn(1) = dVn(2);
125         index = temp;
126     end
127     if current(temp)<0.02*I
128         OffL = temp; % start of integration limits
129         break
```

```
130     end
131     if temp<=0
132         break
133     end
134 end
135 % Now TEMP is located at the start of the time period of
       interest. Now it
136 % is increased until the current has dropped close to
       zero
137 while 1
138     temp = temp + 1;
139     dVn(2) = (voltage(temp+1)-voltage(temp-1))/(0.4);
140     if dVn(2)<dVn(1)
141         dVn(1) = dVn(2);
142         index = temp;
143     end
144     if voltage(temp) < 0.05*VolH
145         OffH = temp;
146         break
147     end
148     if temp >= 1000000 % 1M data points in total
149         break
150     end
151 end
152
153 Eon = trapz(time(OffL:OffH),power(OffL:OffH));
154
155 %% Plot the Eon Transition
156 %
157 temp = [time(OffL) time(OffH)];
158 OffL = OffL-100;
159 OffH = OffH+100;
160
161 plottime = time(OffL:OffH);
162 plottime = plottime.*1e9;
163 figure('Name', 'Turn On Transition', 'NumberTitle','off')
       ;
164 subplot(2,1,1)
165 yyaxis left
166 plot(plottime,voltage(OffL:OffH));
167 ylabel('V_{ds} (V)')
168 yyaxis right
169 plot(plottime,current(OffL:OffH));
170 ylabel('I_{ds} (A)')
171 xlabel('Time (ns)')
172 title('Device Switching Waveforms',FontSize=11)
173 ax1 = gca;
174 xline(1e9*temp(1),'--r','LineWidth',1,'Label','Start');
```

```
175 xline(1e9*temp(2),'--r','LineWidth',1,'Label','Stop');
176 subplot(2,1,2)
177 plot(plottime,power(OffL:OffH));
178 ylabel('Power Loss (W)')
179 xlabel('Time (ns)')
180 title('Device Instantaneous Loss',FontSize=11)
181 ax2 = gca;
182 linkaxes([ax1 ax2],'x')
183 xline(1e9*temp(1),'--r','LineWidth',1,'Label','Start');
184 xline(1e9*temp(2),'--r','LineWidth',1,'Label','Stop');
185 xlim([1e9*time(OffL) 1e9*time(OffH)])
186
187 %% Rise and Fall times, plus slew rate calculation
188
189 % Voltage Rise
190 [R,LT,UT,LL,UL] = risetime(voltage,time,
       PercentReferenceLevels = [5 95]);
191 if length(R)<2
192     tr = R(1);
193     slewU = (UL-LL)/(UT(1)-LT(1));
194 else
195     tr = R(2); % Second voltage transition has the
          current of interest
196     slewU = (UL-LL)/(UT(2)-LT(2));
197 end
198 tr = R(1);
199 slewU = slewU*1e-9; % Convert to V/ns
200
201 % Voltage Fall
202 [F,LT,UT,LL,UL] = falltime(voltage,time,
       PercentReferenceLevels = [5 95]);
203 if length(F)<2
204     tf = F(1);
205     slewD = (UL-LL)/(UT(1)-LT(1));
206 else
207     tf = F(2);
208     slewD = (UL-LL)/(UT(2)-LT(2));
209 end
210
211 slewD = abs(slewD)*1e-9; % fix sign plus convert to V/ns
212
213 % Voltage overshoot at second turn-off
214 OVST = overshoot(voltage,time);
215 over = OVST(2); % overshoot expressed in percentage terms
216 dVp(2) = [];    % delete unnecessary temp var for the
       output to work
217 dVn(2) = [];
218 end
```

Appendix C

Low Frequency Converter PCBs

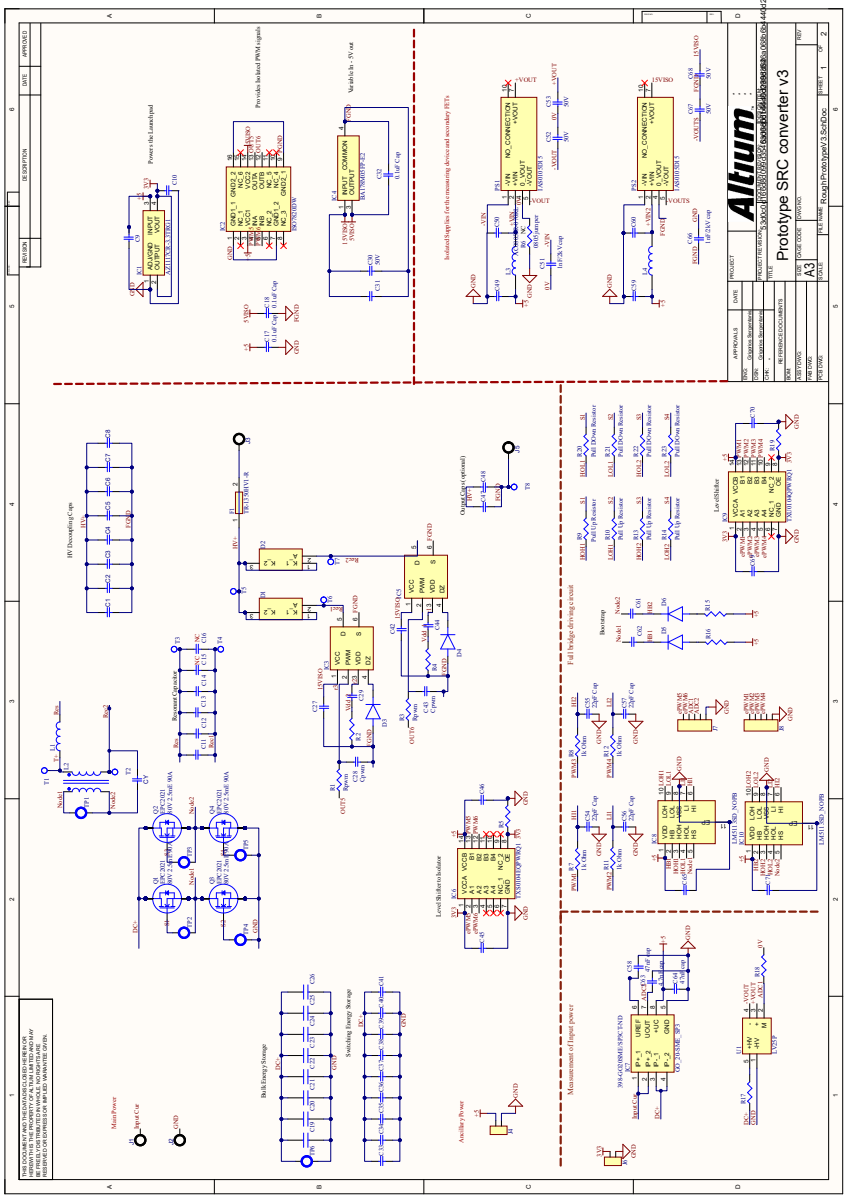


Figure C.1: Converter Schematics.

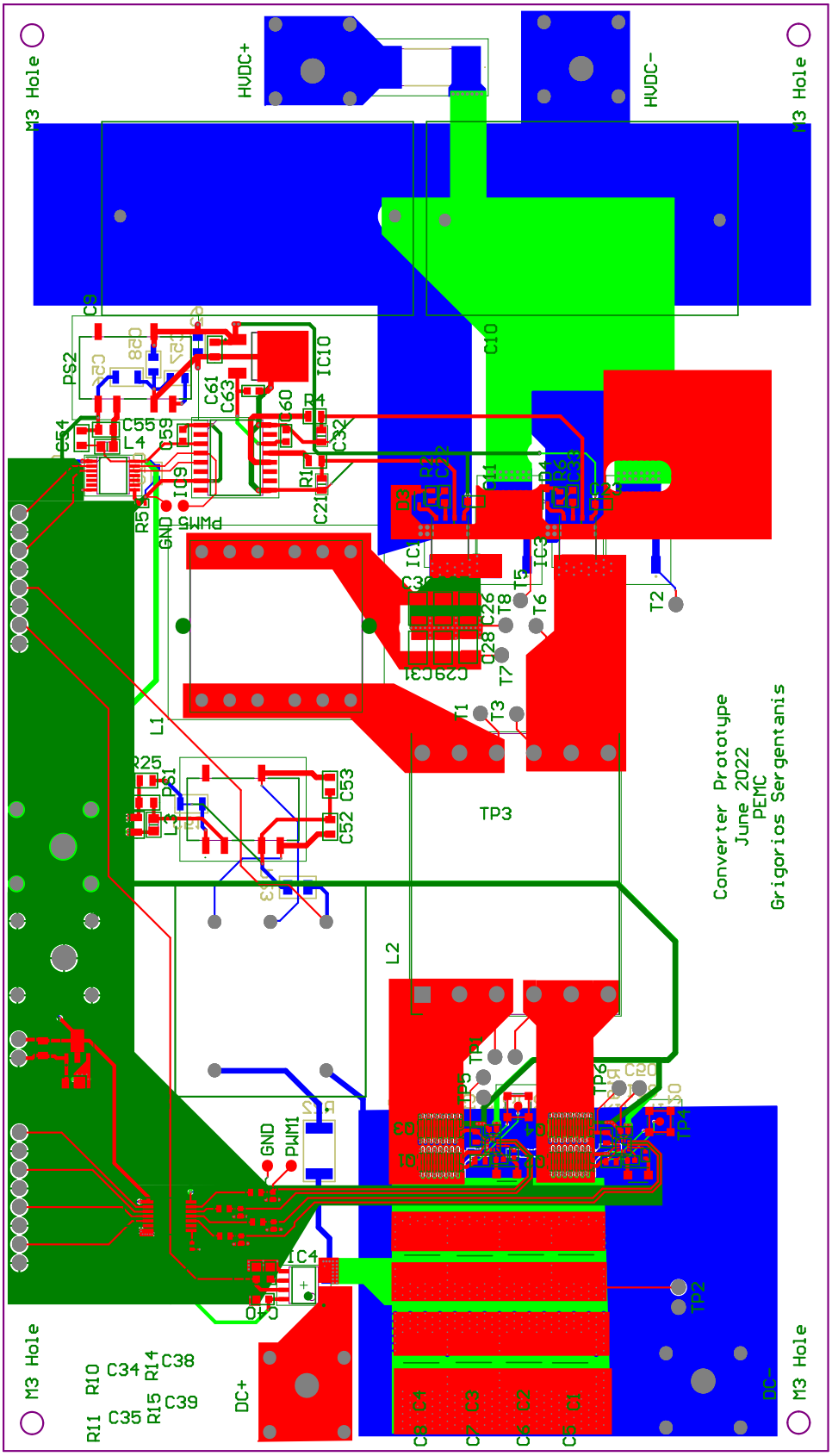


Figure C.2: Prototype PCB - Version 1.

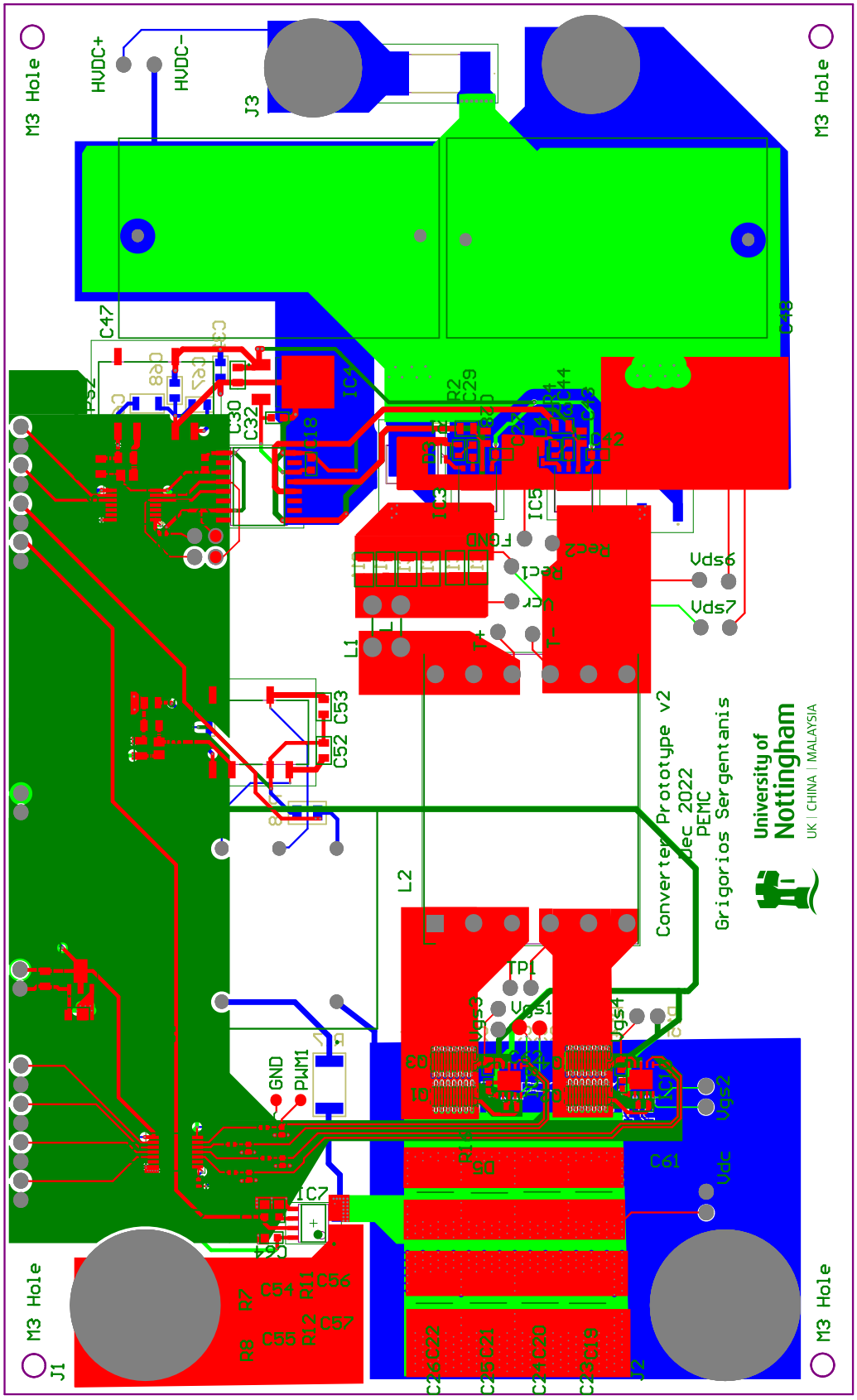


Figure C.3: Prototype PCB - Version 2.

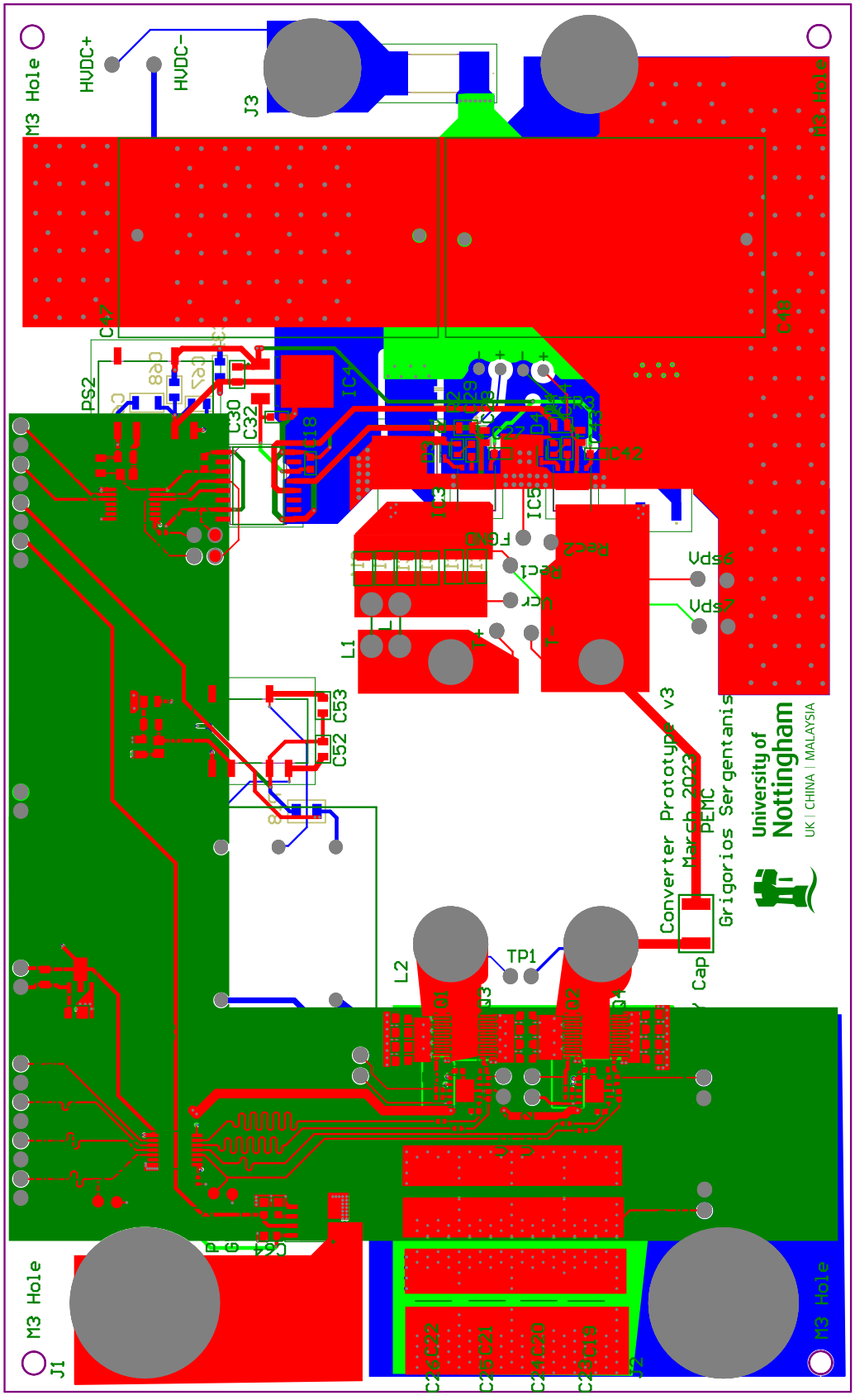
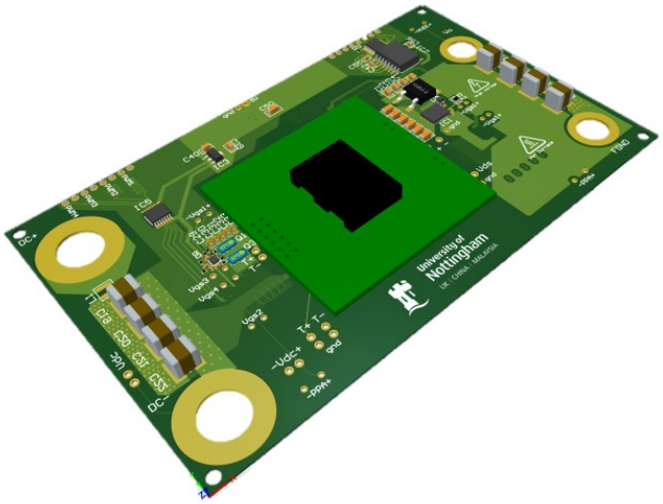


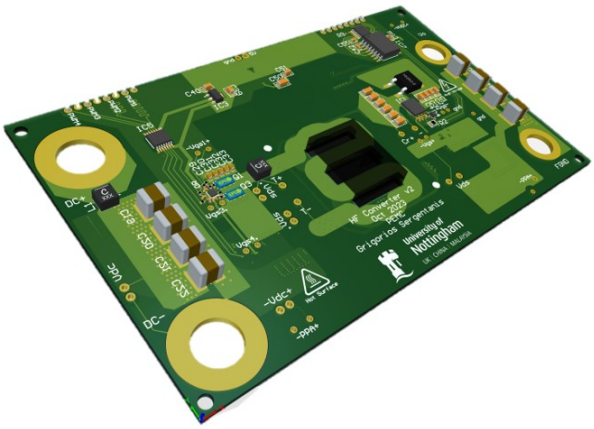
Figure C.4: Prototype PCB - Version 3.

Appendix D

High Frequency Converter PCBs



(a)



(b)

Figure D.1: Designed 1 MHz prototypes. The first iteration (a), had a plug-in transformer for easy measurement and alterations. The second iteration (b) integrates the transformer to form one PCB.

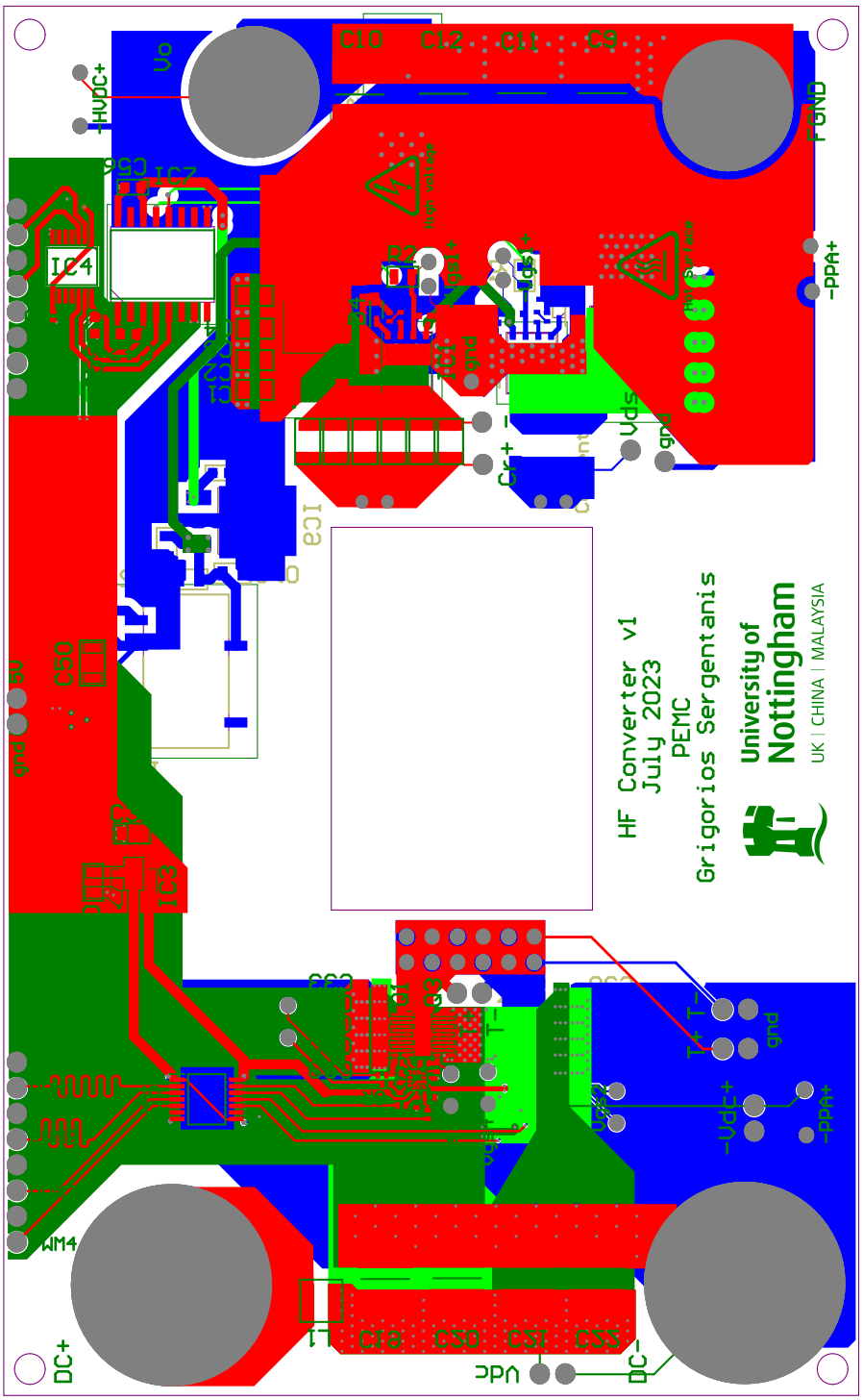


Figure D.2: 1 MHz converter PCB - Version 1.

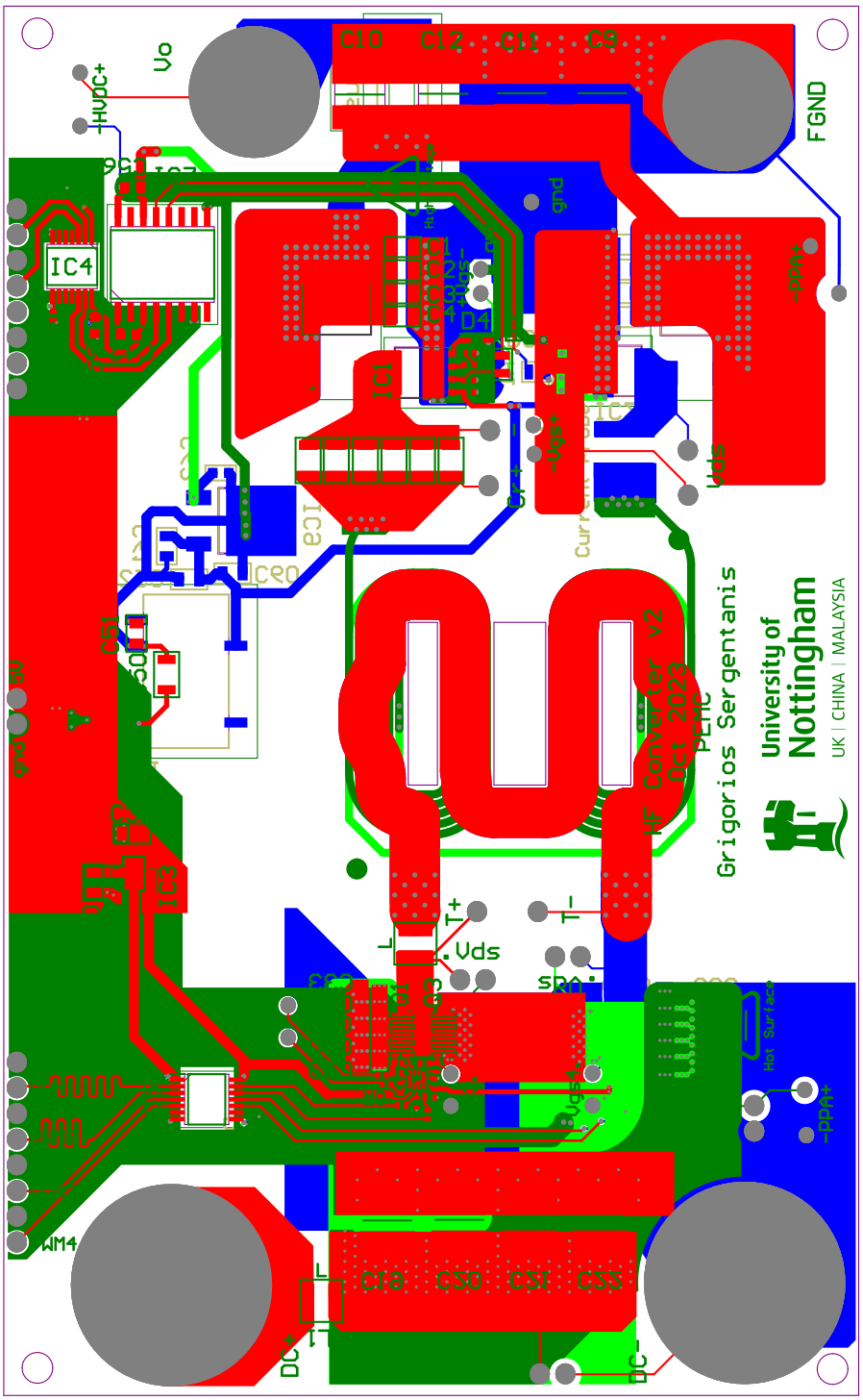


Figure D.3: 1 MHz converter PCB - Version 2.

Appendix E

List of Used Equipment in Converter Testing

Table E.1: Chapter 5 Bench Test Equipment & Devices. The input and output capacitors are overdimensioned to get accurate efficiency measurements.

Passive Probes	TPP1000	S_{1-4}	EPC2021
Current Sense	TCP312A & TCPA300	$D_{1,2}$	C3D02060E
Oscilloscope	DPO4101B	$S_{5,6}$	NV6115
Gate Drive	LM5113	C_{in}	$8 \cdot 10\,\mu F$
PWM Isolation	ISO7820DW	C_{out}	$2 \cdot 10\,\mu F$
Differential Probe	THDP0200	L_r/C_r	$61.9\,\mu H/28.8\,nF$

Table E.2: Chapter 6 Bench Test Equipment & Devices. The input and output capacitors are overdimensioned to get accurate efficiency measurements.

Passive Probes	TPP1000	S_{1-4}	EPC2071
Current Sense	TCP312A & TCPA300	$D_{1,2}$	C3D02060E
Oscilloscope	DPO4101B	$S_{5,6}$	NV6115
Gate Drive	LMG1205	C_{in}	$4 \cdot 10\,\mu F$
PWM Isolation	ISO7820DW	C_{out}	$4 \cdot 1\,\mu F$
Differential Probe	THDP0200	L_r/C_r	$2\,\mu H/9.4\,nF$