Silicon Carbide (SiC) Insulated Gate Bipolar Transistors (IGBTs) for High Voltage Applications

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Abstract

The significant interest that SiC has attracted over the last decades, coupled with the ease of voltage control and low conduction losses of the IGBTs, have led to their development and sample fabrication. Although these devices demonstrated the advantages that SiC IGBTs can bring in High Voltage power applications, their characteristics are not yet fully understood and their structure is far from optimised. This thesis addresses specific gaps in knowledge around accurate device modelling and optimisation of SiC IGBTs considering efficiency and ruggedness.

Firstly, an experimentally validated Technology Computer-Aided Design (TCAD) model was developed to study the behaviour of SiC IGBTs in a wide range of nominal and failure conditions. To achieve good predictive capability of the TCAD model, the modelled SiC material properties and device behaviour were verified by comparing the simulation results against published experimental data. The most critical parameters for performance optimisation were identified and several optimisation trade-off relationships were studied. Additionally, the SiC IGBT structure was optimised to improve its ruggedness in regards to false turn-on, short circuit and Electromagnetic Interference (EMI). Furthermore, a novel device structure is proposed with the ability to enhance the device's ruggedness and simplify the optimisation process without sacrificing efficiency.

The optimisation conclusions were generalised for all SiC IGBT devices rated at 10-40 kV, and specific optimisation recommendations of each voltage class were summarised. Last but not least, a behavioural model for SiC IGBT was proposed for the first time, by modifying the commonly used MOSFET behavioural model and including current- and temperature-dependence on the parasitic capacitances. Its high accuracy, convergence and speed make it an essential tool for converter-level simulations to accelerate device demand and drive commercialisation.

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Abbreviations

CO_2 Carbon dioxide.
N_B Buffer layer doping concentration.
SiO_2 Silicon Dioxide.
W_B Buffer layer thickness.
2D Two-Dimensional.
AC Alternating Current.
ADM Aperture Density Modulation.
AI Artificial Intelligence.
ASIC Aplication-Specific Integrated Circuit.
BJT Bipolar Junction Transistor.
BV Breakdown Voltage.
CSL Charge Storage Layer.
CTE Thermal expansion coefficient.
EMI Electromagnetic Interference.
ETO Emitter turn-off.
FEM Finite Element Method.
FFR Floating Field Rings.
GaN Gallium Nitride.
GTO Gate turn-off.
HDB Higher Doped Buffer region.
HDD Higher Doped Drift region.
HVDC High Voltage Direct Current.
IC Integrated Circuit.
IGBT Insulated Gate Bipolar Transistor.
IGCT Integrated gate turn-off Thyristor.
IP Intellectual property.
JFET Junction Field Effect Transistor.
LDB Lower Doped Buffer region.
LDD Lower Doped Drift region.

MOS Metal Oxide Semiconductor.
MOSFET Metal Oxide Semiconductor Field Effect Transistor.
MRL Manufacturing Readiness Level.
MZ-JTE Multi-Zone Junction Termination Extension.
NPT Non-Punchthrough.
PT Punchthrough.
PV Photovoltaic.
RC Resistive-Capacitive.
SCWT Short Circuit Withstand Time.
SiC Silicon Carbide.
SM-JTE Space Modulated Junction Termination Extension.
SZ-JTE Single Zone Junction Termination Extension.
TCAD Technology Computer-Aided Design.
TRL Technology Readiness Level.
UHV Ultra-high voltage.
UIS Unclamped Inductive Switching.

Chapter 1

Introduction

1.1 Background

1.1.1 The Role of Power Electronics in Achieving Decarbonisation Targets to Tackle Climate Change

The prosperity of modern society heavily relies on consuming vast amounts of energy for transportation, manufacturing, heating, and cooling, thus facilitating everyday activities. The primary source of this energy over the last few decades has been the burning of non-renewable fossil fuels to produce electricity or refine them for use as fuels. However, this process produces Carbon dioxide (CO_2), which is a significant contributor to global climate change, resulting in extreme weather conditions, temperature rise, wildfires, etc. [27]. In response to this, global efforts have been made to combat climate change [28, 29]. Solutions to achieve this goal involve increasing renewable energy sources and decarbonising energy-intensive activities such as manufacturing and transportation, with electrification playing a pivotal role.

Consequently, there is an expected significant increase in electricity demand, ne-

cessitating new solutions in all aspects of electrical systems, including generation (e.g., wind turbines and solar panels), transmission (e.g., High Voltage Direct Current (HVDC) and Alternating Current (AC) transmission systems), or consumption (e.g., electric vehicles). As a result, innovative solutions in power converters are required, with power semiconductor devices lying at the heart of every power electronics system.

1.1.2 Silicon and Wide Bandgap Materials

The invention of the first Silicon power bipolar transistor and, more importantly, the commercialisation of the Silicon Thyristor in the 1950s led to the replacement of bulkier and inefficient vacuum and mechanical switches. Later, the development of fully controlled power semiconductors such as the Gate turn-off (GTO) Thyristor, power Metal Oxide Semiconductor Field Effect Transistor (MOSFET), and Insulated Gate Bipolar Transistor (IGBT), and more recently Integrated gate turn-off Thyristor (IGCT), made high-power converters possible. The improvement in the efficiency of applications utilising Silicon power semiconductor devices led to their extensive deployment in a broad spectrum of applications. As shown in Fig. 1.1, silicon devices can handle powers higher than 10 MVA or switch at frequencies of tens of kHz, serving applications such as HVDC, electric vehicles, power supplies, and more.

The ability of Silicon to serve such a broad and diverse spectrum of applications led to extensive study of its properties and characteristics. Consequently, large-area wafers of excellent quality have become readily available, fabrication technology has matured, and multiple power devices have been invented, demonstrated, and optimised to a great extent. The high Technology Readiness Level (TRL) and Manufacturing Readiness Level (MRL) of silicon devices resulted in an abundance of highly optimised, highly efficient, low-cost power devices flooding the market,

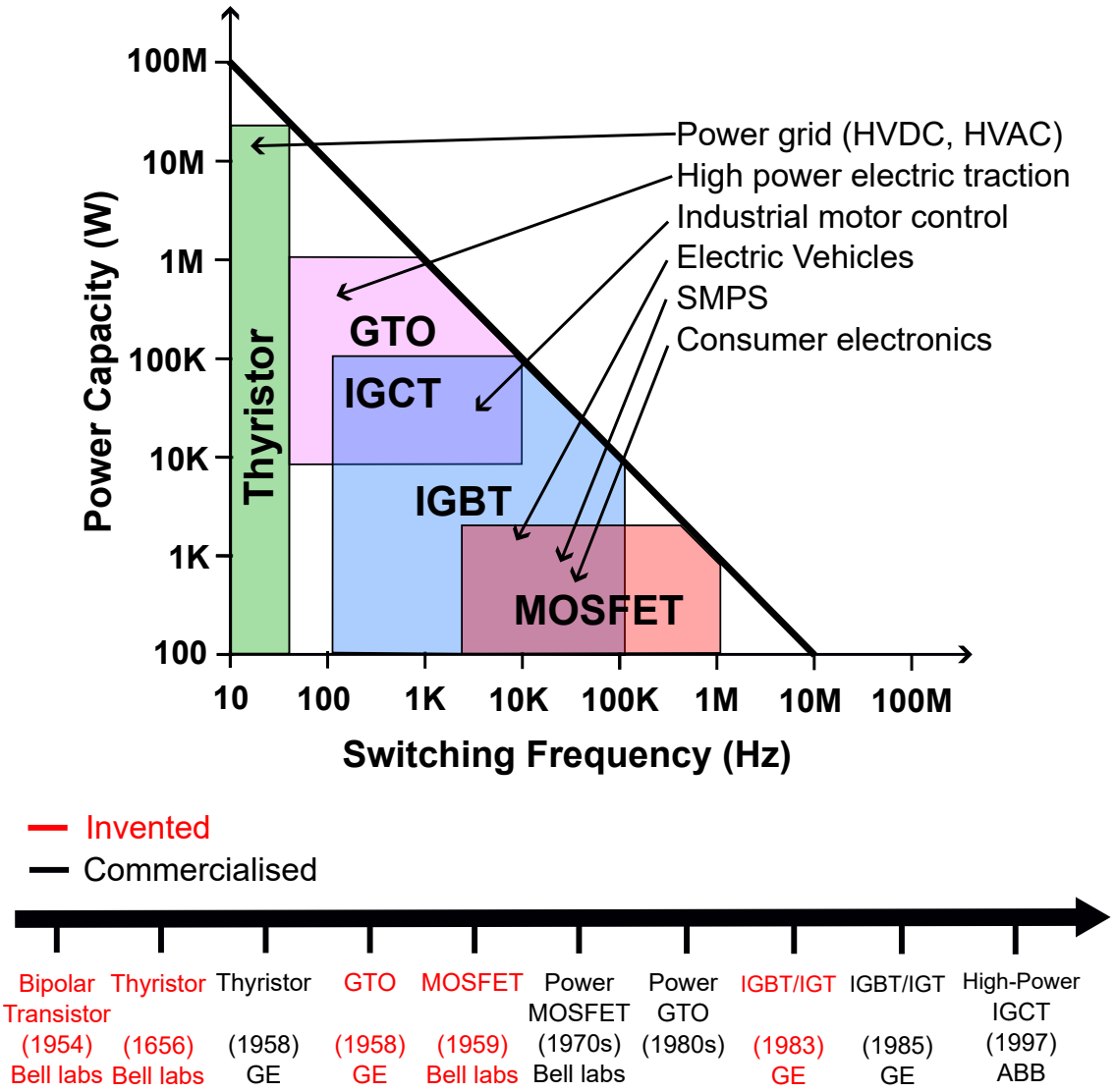


Figure 1.1: Typical applications of Silicon power semiconductor devices and their evolution.

capable of serving the requirements of a diverse spectrum of applications. However, in specific applications, the mass, volume, efficiency, power density, and reliability requirements exceed what can currently be achieved with Silicon. A fundamental step improvement in power electronics can be achieved by utilising wide bandgap semiconductors to form power electronic devices.

Wide bandgap semiconductor materials

Due to their superior electrical characteristics, new and emerging semiconductor materials with wide bandgaps have begun replacing Silicon in specific applications.

Figure 1.2 compares the material properties of significant power semiconductors with Silicon. The larger bandgap and critical electric field, as well as improved thermal conductivity and achievable saturation velocity of these materials, underpin power devices of significantly higher operating temperature, switching speed, voltage, and current density levels. Systems employing such wide bandgap devices can be more efficient, simpler, compact, and significantly lighter. Furthermore, they may require reduced cooling and the passive and active components needed in such power electronic systems can be reduced in number and dimensions, leading to a significant improvement in power density.

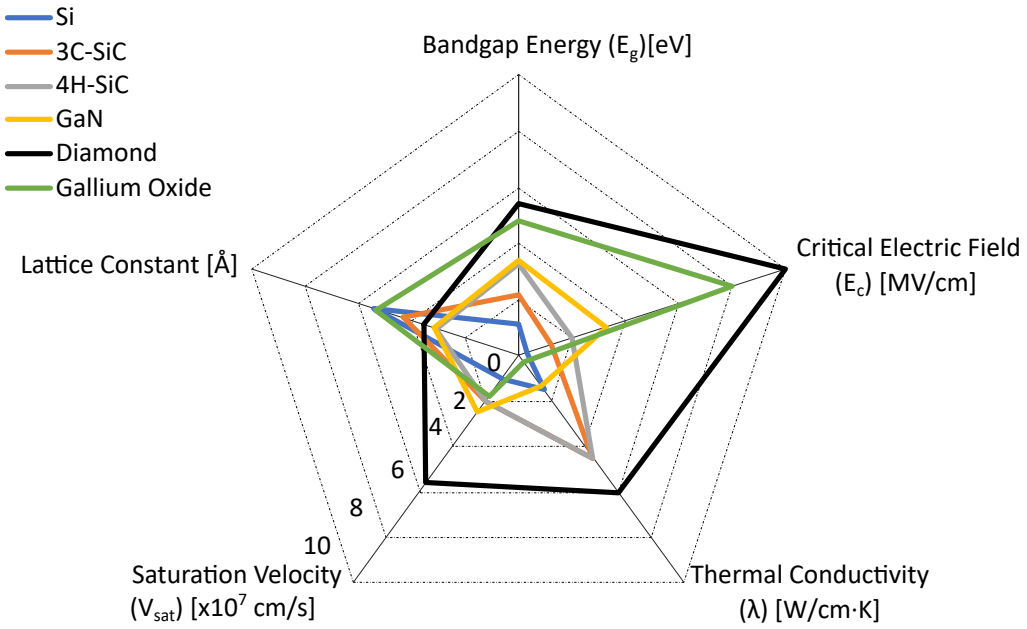


Figure 1.2: Material properties of significant power semiconductor materials [4, 5, 6, 7, 8].

Silicon Carbide (SiC) and Gallium Nitride (GaN) are the wide bandgap materials that have been studied the most, and their TRL and MRL are relatively high. On the other hand, although semiconductor devices on Gallium Oxide and Diamond have been demonstrated [30, 31, 32, 33, 34, 35, 36], they are not expected to commercialise as power electronic devices due to the high activation energies of currently known dopants, low thermal conductivity (Gallium oxide) and high cost (Diamond).

1.1.3 Silicon Carbide Power Electronic Devices

SiC is an IV-IV compound material composed of Silicon and Carbon atoms. It is a rare mineral, but it has been mass-produced since 1892, using the Acheson process [37]. Initially, the produced material was used for industrial applications such as cutting, grinding, and polishing, but in 1955, relatively pure SiC crystals were produced using a sublimation technique [38], allowing for research into SiC as a semiconductor material for electronic devices.

Material properties

Silicon carbide exhibits polymorphism, meaning its chemical composition exists in more than one form, either amorphous or structured (known as polytypes). The three most studied SiC polytypes are the 3C-SiC, 4H-SiC, and 6H-SiC. Due to different crystal structures, the physical properties of polytypes can vary significantly. For example, the bandgap energy of 3C-SiC is about 2.3 eV, while that of 4H-SiC is 3.26 eV. Critical properties of 4H-SiC, 3C-SiC, and 6H-SiC are summarised and compared with Silicon in Table 1.1.

Table 1.1: Critical material properties of silicon and silicon carbide polytypes [1, 2, 3].

	Silicon	**4H-SiC**	**3C-SiC**	**6H-SiC**
Bandgap Energy (eV)	1.12	3.26	2.2-2.4	3.02
Critical electric field (MV/cm)	0.29	2-2.8	1.2-1.4	3
Electron mobility ($cm^2/V \cdot s$)	1350	1020	1000	450
Relative dielectric constant	11.9	10.32	9.72	10.03
Thermal Conductivity (W/cmK)	1.5	3.8-4.5	3.2-4.5	4.9

As seen in Table 1.1, parameters such as the high critical electric field strength and thermal conductivity of all SiC polytypes are higher than those of Silicon, explaining the significant scientific interest in SiC development and utilisation in high voltage applications. Despite the advantages, several reasons explain why silicon devices are still widely used in power electronics. Firstly, the fabrication

process of SiC devices is not yet mature, and the manufacturing cost per area is higher than Silicon. Although this is not expected to reduce to the silicon level due to the more complex and energy-intensive fabrication steps required, significant progress has been made in SiC power device manufacturing over the last 30 years and manufacturing costs are expected to reduce as fabrication techniques improve significantly and market share expands. Additionally, when considering the life cycle cost of a power converter, SiC systems are found to achieve lower costs due to the increased power density and efficiency and lower component count over the silicon counterparts [39].

Evolution of Silicon Carbide devices

One of the first SiC power devices reported was a 400 V 6H-SiC Schottky diode and a MOSFET [40, 41]. In 1995, a 6H-Silicon Carbide Schottky diode with a blocking voltage of 1000 V was demonstrated [42]. Later, high-voltage silicon carbide JFETs were introduced and operated in cascade configuration with low-voltage silicon normally-off MOSFETs [43]. By the end of the 1990s, the first planar MOSFET and the first p-channel trench-gate 4H-SiC IGBT were demonstrated [44] and [45], respectively.

The commercialisation of SiC devices began in 2001 with the first Schottky diode produced at scale by Infineon [46]. The next device marketed was a 1200V SiC JFET by SemiSouth Laboratories in 2008, initially used in a cascade configuration, offering high voltage and current capability with low on-state resistance. The list of commercially available SiC devices expanded in 2011 with the first 1200V power SiC MOSFET by CREE (CMF20120D). Currently, there is a relatively wide range of SiC power devices on the market from different manufacturers, such as 3.3 kV-rated MOSFETs and Schottky diodes (CPM3-3300-R050A, G2R50MT33-CAL, GC50MPS33-CAL), 15kV/1A PiN diode (GA01PNS150-220), or 3.3 kV MOSFET half-bridge power modules rated higher than 750 A (FMF750DC-66A and

CAB600M33LM3).

Additionally, devices with higher voltage capabilities are in the research and development stage. Notable examples include the demonstration of 10 and 15 kV-rated power MOSFETs [47], >10 kV-rated Bipolar Junction Transistor (BJT) [48], 22 kV-rated SiC Emitter turn-off (ETO) Thyristor [49], and 27 kV 4H-SiC n-type IGBTs [10]. Devices with voltage ratings exceeding 10 kV, usually termed Ultra-high voltage (UHV) devices, are considered important for SiC as they serve a voltage rating territory where Silicon's performance is limited by its material properties.

This thesis focuses on the design and optimisation of the SiC IGBT due to its unique characteristic of combining the improved on-state performance of bipolar devices and the ease of voltage control of MOS-based devices with the potential to become a critical power electronic device for high-power applications.

1.1.4 Evolution of silicon carbide IGBTs

Figure 1.3 presents the most important milestones in the SiC IGBT evolution. An early study comparing a trench-gate MOSFET with a trench-gate IGBT on a 6H-SiC substrate was presented in [50] more than 25 years ago. Although the fabricated samples were only able to block voltages up to 200V due to breakdown failure at the trench corners, these early IGBTs demonstrated a tenfold increase in conductivity modulation in the drift region compared to MOSFETs, highlighting their potential in high-voltage applications. Subsequent advancements in fabrication processes and the adoption of 4H-SiC substrates led to the creation of a 10kV-rated p-type trench-gate IGBT with low specific on-resistance, as showcased in [51]. However, the necessity for thick gate oxide to withstand high electric fields at trench corners resulted in high gate threshold voltages. The shift to planar IGBT structures allowed for achieving similar high breakdown voltages with thinner gate oxides,

resulting in devices with lower threshold voltages, as demonstrated in [52, 53].

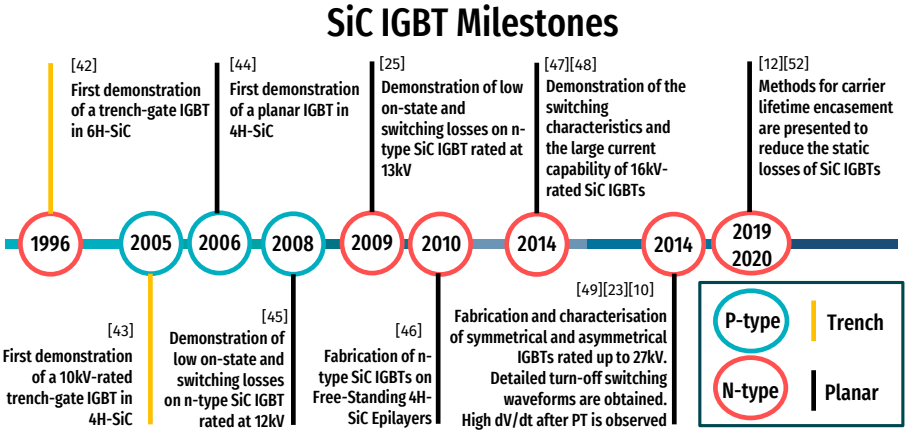


Figure 1.3: SiC IGBT evolution.

A significant breakthrough in IGBT technology was the fabrication of a 13kV-rated n-type IGBT, with very low differential on-resistance, detailed in [25]. The development of n-type IGBTs, which benefit from the higher mobility of electrons compared to holes, was initially hindered due to the unavailability of low-resistance, high-quality p-type substrates. This changed with the introduction of a method for fabricating n-type IGBTs using commonly available n-type substrates, where both n and p-type layers are epitaxially grown, and the initial substrate is subsequently removed, as described in [54]. This innovation spurred the development of a range of n-type IGBT devices with ratings up to 27kV from various research groups [10, 23, 55, 56, 57]. These devices displayed detailed on-state and switching characteristics during operation, confirming their suitability for high-voltage applications [58, 59]. The most recent milestone in SiC IGBT development has been the enhancement of carrier lifetime to improve forward conduction characteristics, achieved through methods outlined in [12, 60].

As a result, the main fabrication issues that SiC IGBTs were facing over the al-

most 30 years of their development have been tackled to a great extent. Additionally, reliability challenges like poor oxide/semiconductor interface quality or bipolar degradation, have been studied extensively and the fabrication processes have been optimised and nearly eliminated. Therefore, with the maturity of SiC fabrication processing that has been achieved, research focus and investment are now being shifted to ultra-high voltage devices.

1.2 Objectives and Contributions

The general aims of this work are to expand the current understanding of the SiC IGBT's behaviour, to propose optimised structures and to provide accurate modelling tools that are not currently available. More details about the objectives and contributions of this thesis are given below:

- **Objective 1:** Develop a Technology Computer-Aided Design (TCAD) model of a SiC IGBT, validated based on experimental data, to investigate the device's behaviour, predict the impact of various parameters, and pinpoint failure mechanisms. This allows for an in-depth assessment and optimisation of the SiC IGBT's behaviour without fabricating the actual device, reducing fabrication iterations, saving costs, and accelerating device optimisation.

  Contribution 1: A validated SiC IGBT model was developed, achieving very good predictive capability verified by comparing simulation results with literature data from fabricated devices. The validation process followed is presented in this thesis, which can provide guidelines for validating different device structures. This validation process consists of two stages. In the first stage, the most critical material properties for the SiC IGBT behaviour have been unidentified (carrier mobilities, incomplete ionisation of dopants, oxide/semiconductor interface properties, etc.), and their TCAD model pa-

rameters have been fine-tuned based on experimental data. In the second stage, static and dynamic characteristics from fabricated IGBTs have been used to estimate the unknown structural and process-dependent parameters. This validation establishes a strong foundation for TCAD models' prediction capability, with expected high validity of conclusions.

- **Objective 2:** Study the behaviour of IGBTs rated at 10-40 kV under normal and single event failure conditions to identify unknown phenomena and investigate the impact of various device parameters on performance and ruggedness.

  Contribution 2: Firstly, the static and the dynamic behaviour of SiC IGBTs rated at different voltages was presented and analysed, linking several physical mechanisms with the electrical characteristics. Subsequently, failure mechanisms such as unintentional turn-on caused by high dV/dt during switching transients or the parasitic thyristor latch-up during a short circuit event were presented in detail using Two-Dimensional (2D) TCAD simulations, enhancing the current scientific understanding of the SiC IGBT's operation and limitations.

- **Objective 3:** Identify different trade-offs for achieving optimum performance-ruggedness for a particular application, considering both nominal and fault operating conditions.

  Contribution 3: Several optimisation trade-offs are discussed throughout this thesis, and the parameters that can effectively control them have been identified. In addition to the well-known trade-off between the static and the dynamic losses of an IGBT, further trade-offs were studied for the first time, including the trade-off between the maximum switching frequency and the maximum dV/dt during the inductive turn-off, the on-state voltage drop and Short Circuit Withstand Time (SCWT), the switching speed and the unintentional turn-on robustness etc. The strong interdependencies between

different trade-offs were highlighted, presenting the challenges of optimisation SiC IGBTs. However, by performing parameter sensitivity analysis of numerous parameters using TCAD simulations, those trade-offs were decoupled to a great extent by selecting different structural and process-dependent parameters to control different characteristics.

- **Objective 4:** Propose a new device structure achieving improved performance and ruggedness compared to conventional or other suggested structures in the literature.

  Contribution 4: A novel SiC IGBT device structure featuring a stepped drift and buffer layer doping profile was proposed, achieving lower dV/dt and better short circuit and unintentional turn-on characteristics without sacrificing efficiency or complicating the fabrication process. In addition to this, this device structure provides a straightforward approach for device performance and ruggedness optimisation by controlling the parameters of the four different drift and buffer layer areas, which cannot be achieved with the conventional structure due to the strong coupling of the buffer layer parameters on several different characteristics. The efficiency of the proposed device structure was studied on different virtually fabricated IGBTs rated at 10-40 kV.

- **Objective 5:** Developing a fast behavioural model that converter designers or application engineers can use to assess the benefits that SiC IGBTs can bring to power electronic systems, boosting demand and commercialisation.

  Contribution 5: This objective has been achieved by proposing the first-ever behavioural model for SiC IGBT. This model can capture the unique static and dynamic characteristics of SiC IGBTs and does not require the knowledge of any structural or process-dependent parameter. It is an extended version of the commonly used behavioural model for power MOSFETs, with the distinction that it uses voltage-, current- and temperature-dependent capacitances. Its parameters can be estimated with electrical characterisation

measurements such as forward and switching waveforms of terminal voltages and currents. As a result, in addition to simplifying the parameter extraction process required by physics-based IGBT models, it makes it attractive to device manufacturers because they can release a fast and accurate model without disclosing structural and process details, protecting the company's Intellectual property (IP).

1.3 List of Publications

Published Academic Journal Papers

- **I. Almpanis**, M. Antoniou, P. Evans, L. Empringham, P. Gammon, F. Undrea, P. Mawby, N. Lophitis, "Silicon Carbide n-IGBTs: Structure Optimisation for Ruggedness Enhancement," in IEEE Transactions on Industry Applications, Jan. 2024, doi: 10.1109/TIA.2024.3354870.
- **I. Almpanis**, P. Evans, M. Antoniou, P. Gammon, L. Empringham, F. Udrea, P. Mawby, N. Lophitis. "10kV+ Rated SiC n-IGBTs: Novel Collector-Side Design Approach Breaking the Trade-Off between dV/dt and Device Efficiency", Key Engineering Materials, May 2023, doi: https://doi.org/10.4028/p-21h5lt.
- N. Lophitis, **I. Almpanis**, P. Wheeler, "Are we on the brink of a post-silicon era in aircraft power electronics?", Jun. 2022 Institute of Materials, Minerals and Mining (IOM3).

Peer-reviewed Conference Papers

- **I. Almpanis**, P. Evans, K. Li and N. Lophitis, "Behavioural SiC IGBT Modelling Using Non-Linear Voltage and Current Dependent Capacitances," 2023

IEEE Design Methodologies Conference (DMC), Miami, FL, USA, 2023, pp. 1-6, doi: 10.1109/DMC58182.2023.10412584.

- **I. Almpanis**, M. Antoniou, P. Evans, L. Empringham, P. Gammon, F. Undrea, P. Mawby, N. Lophitis, "Influence of Emitter Side Design on the Unintentional Turn-on of 10kV+ SiC n-IGBTs," 2022 IEEE Energy Conversion Congress and Exposition (ECCE), Detroit, MI, USA, 2022, pp. 1-6, doi: 10.1109/ECCE50734.2022.9947492.

- **I. Almpanis**, P. Evans, M. Antoniou, P. Gammon, L. Empringham, F. Undrea, P. Mawby, N. Lophitis, "Short-Circuit Performance Investigation of 10kV+ Rated SiC n-IGBT," 2022 IEEE Workshop on Wide Bandgap Power Devices and Applications in Europe (WiPDA Europe), Coventry, United Kingdom, 2022, pp. 1-6, doi: 10.1109/WiPDAEurope55971.2022.9936475.

Conference Paper In Review

- F. Pizzimenti, **I. Almpanis**, P. Evans, N. Lophitis, F. G. Capponi and F. Palone "Technical Evaluation on the Prospective Use of High-Voltage Silicon Carbide (SiC) Power Devices in Transmission-Type STATCOMs," 2024 IEEE Energy Conversion Congress and Exposition (ECCE), Phoenix, AZ, USA, 2024, **in peer-review**.

Technical Report

- N. Lophitis, **I. Almpanis**, P. Wheeler, "Post-Silicon Power Semiconductors for High Voltage Aerospace Electrical Power Systems", Dec. 2021, ATI Fly-Zero.

1.4 Thesis Outline

The rest of this thesis is organised as follows:

Chapter 2 presents the fundamental structures of Insulated Gate Bipolar Transistor (IGBT)s and explains their operating principles across various operational states, including blocking, conducting, and transient.

Chapter 3 provides a literature review on efforts to optimise the performance and ruggedness of SiC IGBTs. Additionally, it details the simulation tools currently employed for predicting and enhancing device performance.

Chapter 4 outlines the methodology employed for accurately modeling SiC IGBTs. It details the key functionalities of the TCAD tools utilised and demonstrates modelling accuracy by correlating simulation results with experimental data from fabricated devices.

Chapter 5 describes the mechanisms causing spikes in the gate electrode that can lead to unintentional turn-on. It subsequently presents the role of emitter side design in mitigating gate voltage spikes and explores the impact of system parameters such as temperature, gate resistance, or current density.

Chapter 6 conducts a detailed analysis of IGBT behavior under short-circuit conditions and elucidates different failure mechanisms. It also explores how various device and circuit parameters influence the short-circuit behaviour of SiC IGBTs to pinpoint the most critical parameters for short-circuit performance optimisation.

Chapter 7 proposes a novel SiC IGBT device structure capable of independently controlling maximum dV/dt during switching transients and efficiency. It demonstrates the structure's ability to achieve a better trade-off relationship between switching speed and maximum dV/dt while improving short-circuit and unintentional turn-on robustness.

Chapter 8 provides a comprehensive overview and predicts the performance of SiC IGBTs rated at 10-40 kV.

Chapter 9 presents a behavioural model achieving fast computational speed and accuracy by using non-linear voltage-, current-, and temperature-dependent capacitances to simulate SiC IGBT's characteristics.

Chapter 10 presents conclusions and future work.

Chapter 2

Structures and Operation

This chapter presents the basic structures of Insulated Gate Bipolar Transistor (IGBT)s and explains their operating principles across various operational states, including blocking, conduction, and transient. While the subsequent chapters focus exclusively on n-type IGBTs, the same structural designs apply to p-type IGBTs. The reason for concentrating on n-type IGBTs stems from their superior electrical characteristics. This superiority is primarily due to the higher mobility of electrons in Silicon Carbide (SiC), making n-type IGBTs an effective solution for power electronic applications.

2.1 Basic structures

IGBT structures can be categorised in terms of their current flow direction as lateral and vertical devices, in terms of their epitaxial wafer technology as symmetrical (Non-Punchthrough (NPT)) and asymmetrical (Punchthrough (PT)) devices, and in terms of their gate structure as planar and trench gate devices. Lateral devices consume a large amount of die area to support high voltages and are not typically preferred for power switches. As a result, this chapter focuses solely on vertical

devices.

2.1.1 Symmetrical and asymmetrical IGBT structures

Asymmetrical and symmetrical IGBTs differ significantly in their fabrication processes, structures, and operations. Figure 2.1 shows the cross-sections of the NPT and PT IGBT half-cells, highlighting typical doping concentrations and dimensions for the drift and buffer layers. The PT IGBT structure requires additional fabrication steps for the epitaxially grown, highly-doped buffer layer. This buffer layer significantly alters the device's operation in all blocking, conducting, and transient states. More specifically, the buffer layer allows the device to support a given Breakdown Voltage (BV) with a thinner drift layer compared to the symmetrical IGBTs, strongly influencing the on-state and transient characteristics. The physical mechanisms behind these differences are explained in detail in subsections 2.2 to 2.4.

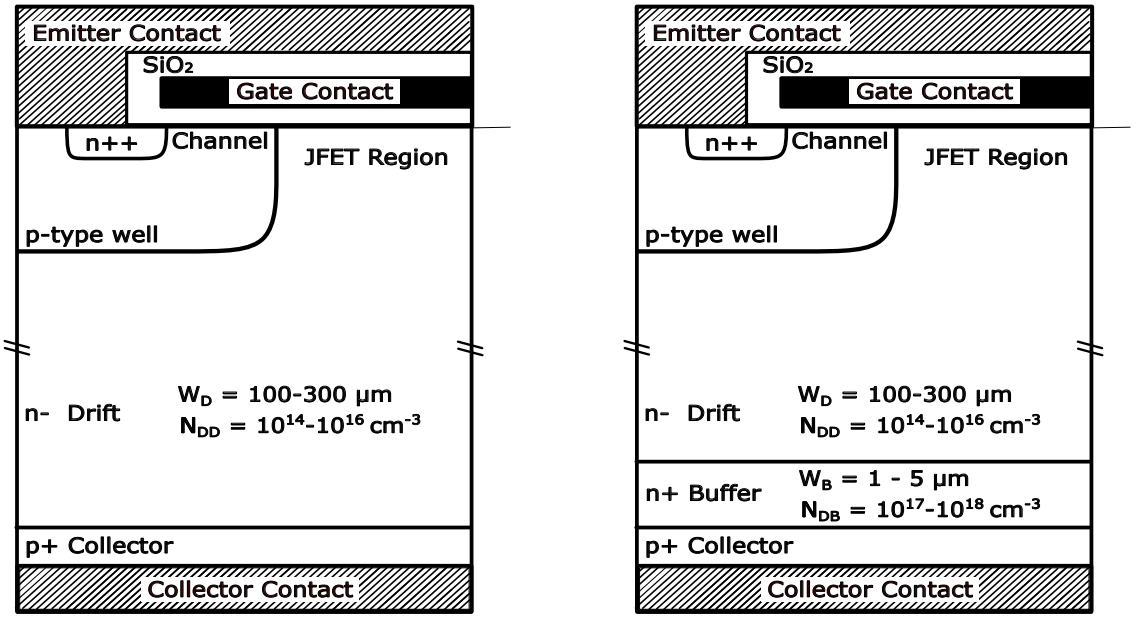


Figure 2.1: Planar IGBT structures: (a) symmetrical (NPT) IGBT and (b) Asymmetrical (PT) IGBT. Typical dimensions and doping concentrations for IGBTs rated at $> 10kV$ are included in the figure.

2.1.2 Planar and trench gate IGBTs

The devices discussed in section 2.1.1 featured planar gate structures. The on-state performance of these devices can be enhanced by adopting a trench gate structure, as illustrated in Fig. 2.2. Utilising trench gates allows for a reduction in cell pitch, enabling the placement of more cells within a given die area and thereby increasing the device's current density. Furthermore, this structure eliminates the Junction Field Effect Transistor (JFET) region in the IGBT, reducing on-state resistance compared to the planar gate structure.

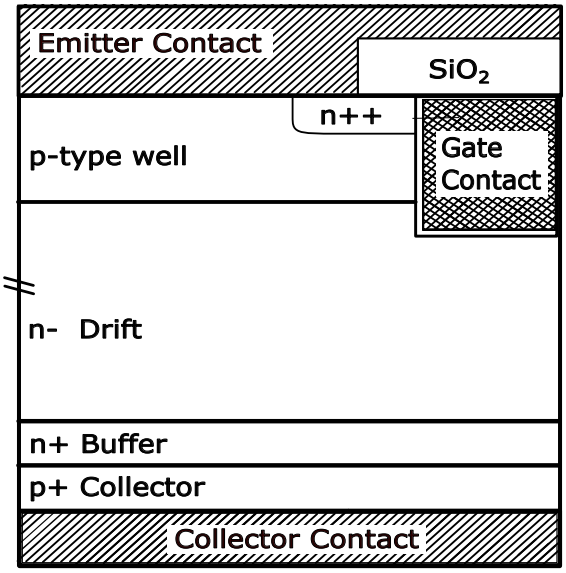


Figure 2.2: Trench gate IGBT structure.

Theoretically, both planar and trench gate IGBTs should exhibit similar breakdown characteristics when using epitaxial wafers with identical doping concentrations and thicknesses. However, the process of trench and the gate oxide formation on their sidewalls require advanced fabrication techniques. These processes can lead to higher leakage currents and a degradation in breakdown characteristics.

2.2 Blocking characteristics

The IGBT operates in the forward blocking mode when the gate and emitter terminals are shorted, and a positive bias is applied to the collector terminal. The reverse-biased PN junction supports the collector voltage between the p-type well and the n-type drift region in this mode. A depletion region is formed in the p-well and n-drift regions to support the collector voltage, predominantly expanding within the drift layer due to its lower doping concentration. Figure 2.3 illustrates a typical depletion region spreading within the active and termination areas of the IGBT. This chapter focuses solely on the active area while acknowledging the termination area's critical role in the breakdown characteristics of the IGBT, as it smoothly terminates the depletion region at the die's surface. Detailed discussions on termination area design are presented in subsection 3.3.4.

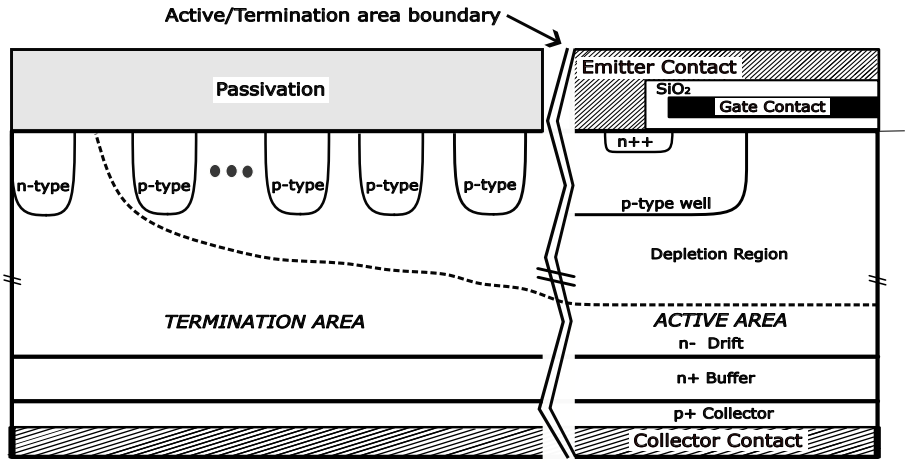
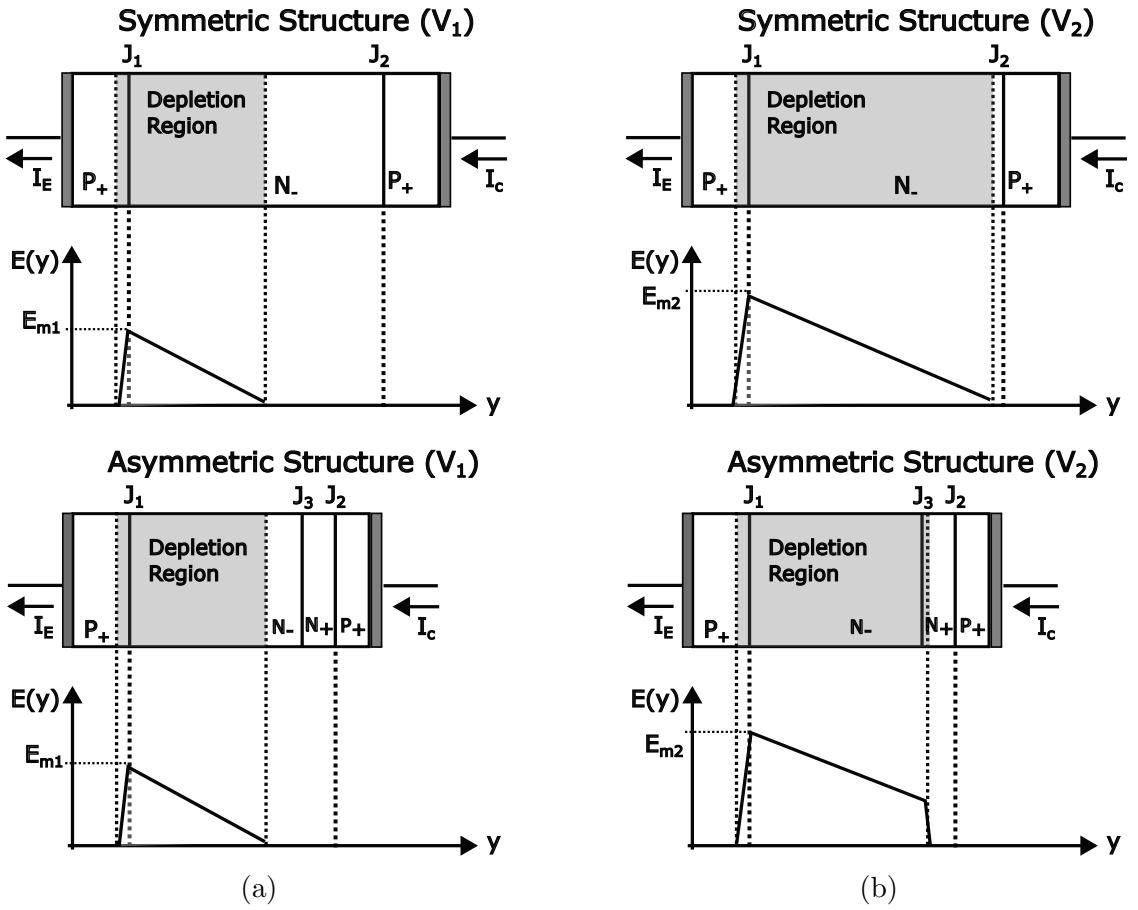


Figure 2.3: Depletion region within the active and edge termination area of the IGBT during the forward blocking mode.

A comprehensive analysis of the forward blocking capability is available in [21], which examines breakdown voltage for both symmetrical and asymmetrical IGBTs, considering factors like leakage current and the internal parasitic PNP transistor's current gain. However, it is crucial to quantitatively highlight the differences in breakdown physics between asymmetrical and symmetrical structures. Figure 2.4 presents 1D representations of symmetrical and asymmetrical IGBTs across the

active/termination area boundary of Fig. 2.3 at different collector voltages with $V_1 < V_2$. Excluding the PNP transistor current gain, the IGBT device may fail due to either avalanche breakdown, caused by the electric field peak in junction J1 exceeding the critical electric field of SiC, or reach-through breakdown, occurring when the depletion region extends through the P+ collector region.



(a) (b)

Figure 2.4: Electric field distribution during the forward-blocking mode at different collector voltages V_1 and V_2, for $V_1 < V_2$.

The prevention of reach-through breakdown in asymmetrical structures is achieved when the Buffer layer doping concentration (N_B) and thickness W_B adhere to Eq. 2.1, where $E_c(N_B)$ represents the critical electric field of SiC material for a doping concentration N_B. In contrast, for symmetrical structures, the reach-through breakdown is averted by employing a drift region with a width and doping concentration according to Eq. 2.2, where $BV_{av}(N_D)$ is the avalanche breakdown voltage of SiC for a doping concentration N_D.

$$N_B W_B > \frac{\epsilon_s E_c(N_B)}{q} \tag{2.1}$$

$$W_D > \sqrt{\frac{2\epsilon_s B V_{av}(N_D)}{q N_D}} \tag{2.2}$$

The doping concentration notably influences both the electric field and avalanche breakdown voltage. Analytical models for calculating avalanche breakdown and critical electric field as functions of doping density have been proposed by various researchers. Equations 2.3 and 2.4 feature Baliga's approximations for these parameters according to [21]:

$$BV_{av}(N_D) = 3.0 \times 10^{15} N_D^{-\frac{3}{4}} \tag{2.3}$$

$$E_c(N_D) = 3.3 \times 10^4 N_D^{\frac{1}{8}} \tag{2.4}$$

Consequently, a thicker drift region is required for the symmetrical IGBT structure to achieve a given blocking voltage compared to the asymmetrical structure. This adversely affects the on-state and switching performance, as is elaborated in subsections 2.3 and 2.4. Therefore, the asymmetrical structure, due to its superior characteristics, is favoured for SiC IGBTs and will be the focus of this thesis.

2.3 On-State Characteristics

The on-state characteristics of the IGBT are elucidated by examining the equivalent circuit depicted in Fig. 2.5, where discrete circuit components are superimposed onto its structure. The device operation can be modelled by a MOSFET, which sup-

plies the base driving current for the internal PNP transistor. Consequently, when a positive gate bias exceeds the gate threshold voltage, electrons are injected from the emitter through the channel, causing the injection of holes from the collector. This bipolar carrier flow enhances the conductivity of the drift region, allowing IGBTs to operate at significantly higher current densities than unipolar power MOSFETs.

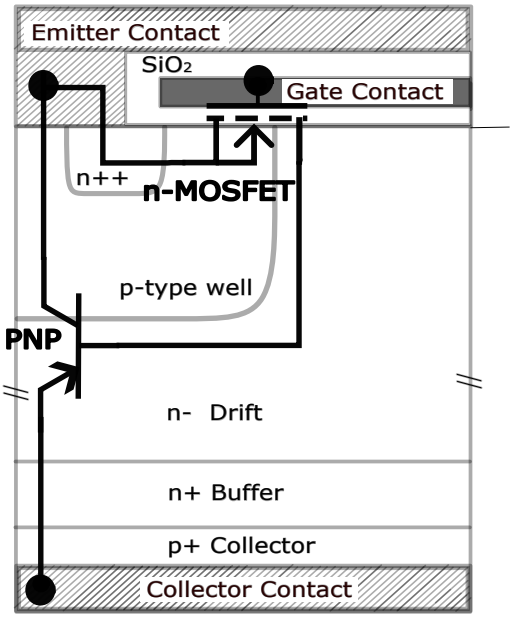


Figure 2.5: Equivalent circuit for the IGBT.

Figure 2.6 illustrates the typical forward conduction characteristics of a simulated IGBT at varying gate voltages (more details about the simulation details are given in Chapter 4). At low gate voltages, the equivalent MOSFET enters its saturation region due to channel pinch-off, leading to the saturation of the IGBT's current-voltage characteristics. The IGBT exhibits a diode-like behaviour at higher gate voltages. Unlike power MOSFETs, SiC IGBTs exhibit a voltage drop of around 3 V even at low current densities, due to the built-in potential of the PN junction between the collector and the buffer layer. The on-state voltage drop of the IGBT is determined using Eq. 2.5, where V_{PN} is the voltage drop across the PN junction, V_{NB} across the internal PNP transistor base region, and V_{MOSFET} across the MOSFET portion. The latter can be further decomposed into contributions from the JFET region, accumulation layer, and channel as per Eq. 2.6.

$$V_{on} = V_{PN} + V_{NB} + V_{MOSFET} \tag{2.5}$$

$$V_{MOSFET} = V_{JFET} + V_{ACC} + V_{CH} \tag{2.6}$$

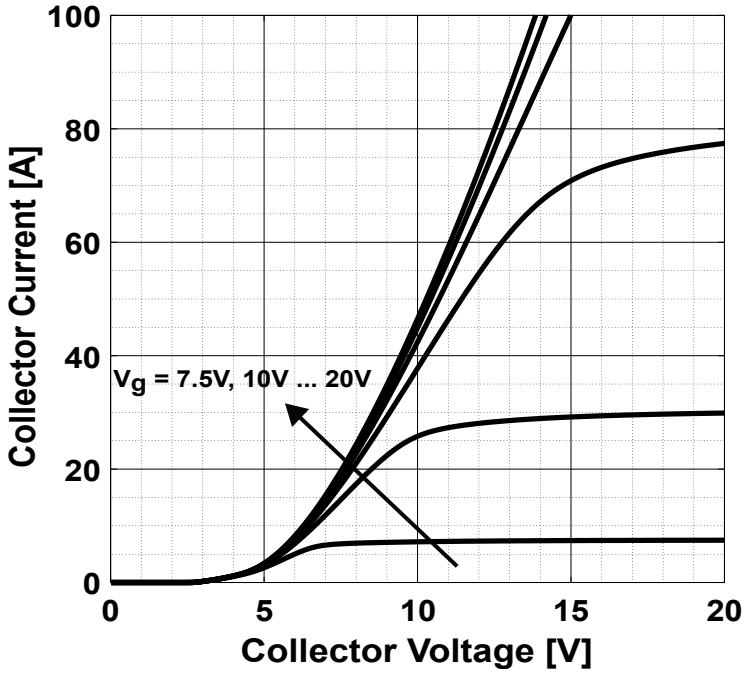


Figure 2.6: Typical forward conduction characteristics of simulated SiC IGBT for different gate voltages.

Understanding the carrier distribution within the various IGBT layers under different operational conditions is essential for comprehending the device's operation. While the off-state carrier distribution can be directly inferred from the doping concentrations of the various layers, during the on-state and transient conditions, this distribution alters due to the conductivity modulation in the drift region.

Figure 2.7 shows the electron and hole concentration profiles during the on-state of the IGBT across its PNP region. The electron and hole concentrations on the drift layer are equal due to the charge neutrality and the low doping concentration. This principle also applies to the buffer layer, albeit with the distinction that the buffer layer's doping concentration is substantially higher. Thus, charge neutrality

leads to a higher electron concentration, as described by Eq. 2.7, where n, p, and N_B represent the electron, hole, and buffer layer doping concentrations.

$$n = N_B + p \tag{2.7}$$

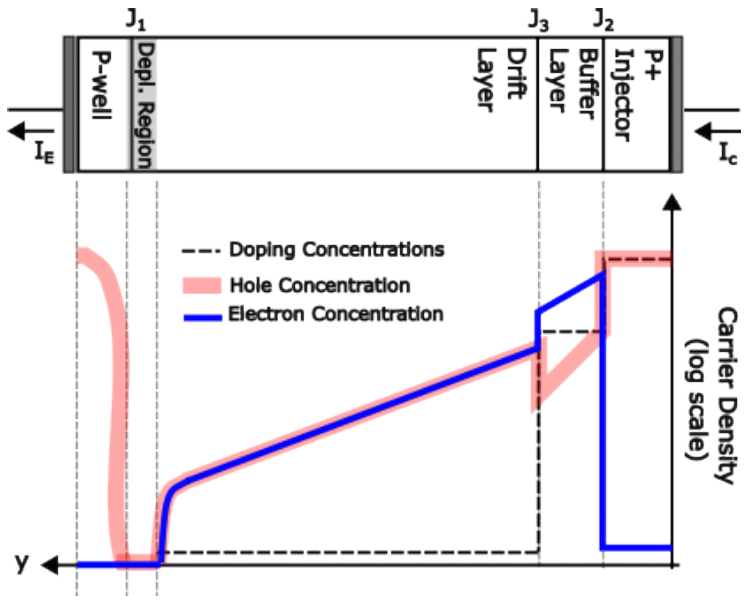


Figure 2.7: Carrier distributions during the on-state of the asymmetrical IGBT structure along the PNP section.

2.4 Switching Characteristics

The switching performance of power semiconductor devices is critically important, particularly for applications that demand high switching frequencies (typically higher than 1 kHz), such as motor control. A typical H-bridge topology driving an inductive load is depicted in Fig. 2.8, featuring two IGBTs and two freewheeling diodes in each leg. During operation, current commutation occurs from D_{2H} to $IGBT_{1L}$ during the turn-on transient, and from $IGBT_{1L}$ to D_{1H} during the turn-off transient of $IGBT_{1L}$. Similar switching transients are prevalent in most converters that drive inductive loads, such as motors, making it imperative to understand IGBT's behaviour under these conditions.

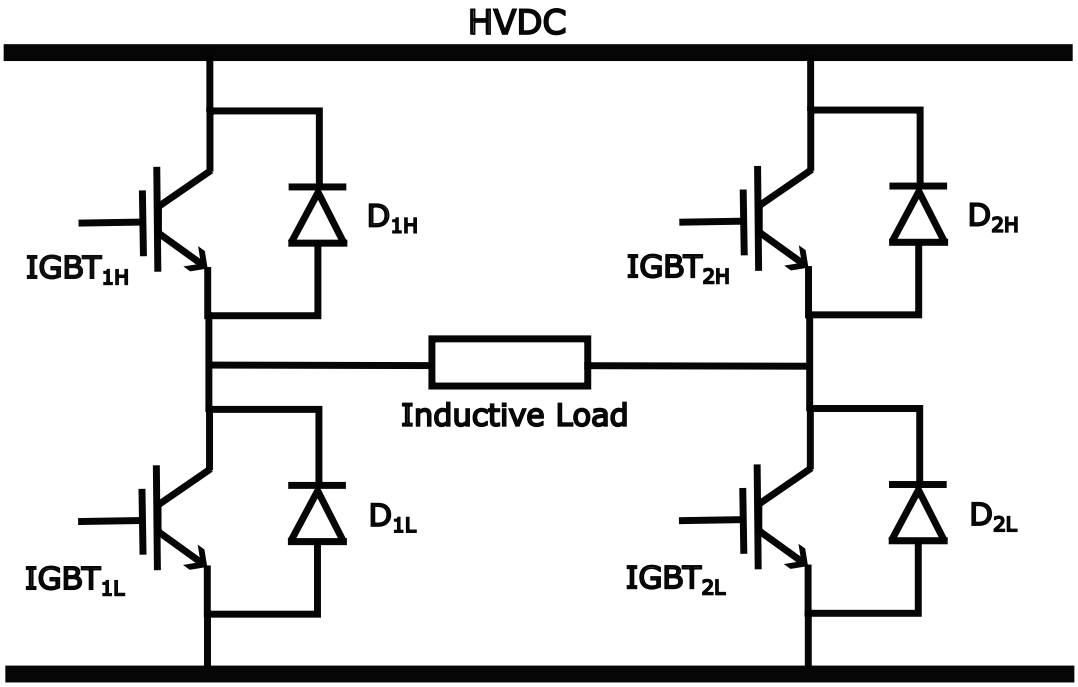


Figure 2.8: IGBT-based H-bridge topology.

Figure 2.9 presents typical waveforms for the collector voltage and current of a SiC IGBT during turn-on and turn-off under inductive load conditions. The type and characteristics of the freewheeling diode strongly influence the current peak amplitude and the duration of the turn-on process, as explained in Section 2.4.2 by comparing the inductive turn-on behaviour when using PiN and Schottky type diodes. In contrast, the turn-off behaviour is primarily determined by the structural characteristics of the IGBT. In particular, the asymmetrical IGBT structure exhibits unique characteristics not observed in other devices.

2.4.1 Inductive load turn-off

Figure 2.10 illustrates a detailed examination of the turn-off process. This process can be divided into four phases: two voltage-rising phases followed by two current-falling phases. The total emitter current is split into its electron and hole components, representing the equivalent MOSFET (through the channel) and PNP transistor (through the p-well) currents. The evolution of internal carrier distribu-

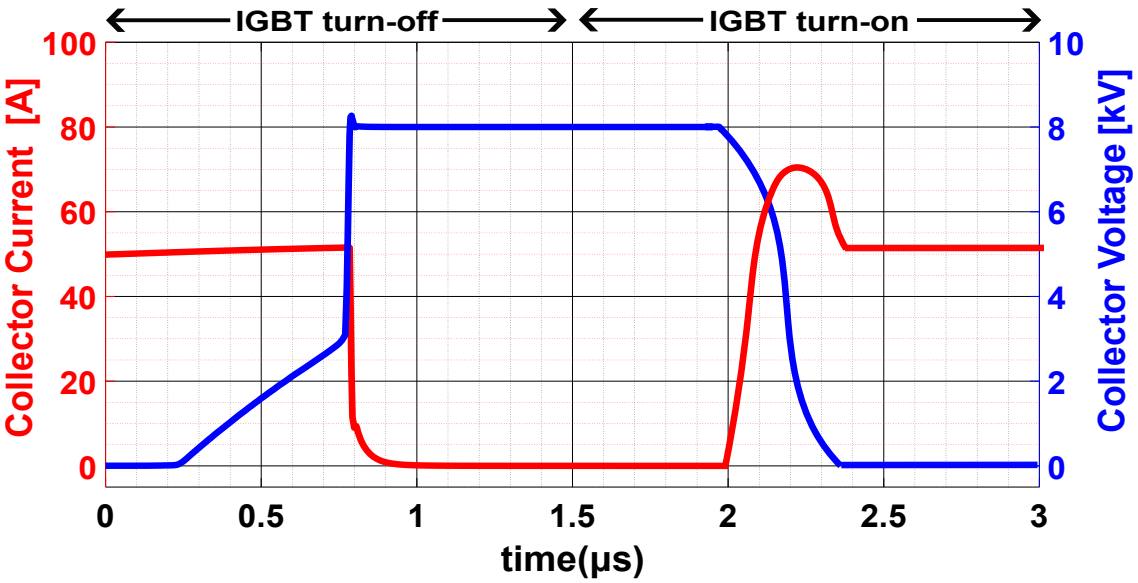


Figure 2.9: Simulated turn-on and turn-off switching transients of SiC IGBT under inductive load.

tion during the turn-off process is coupled with physical equations to explain these phases.

Figure 2.11 displays the electron and hole distributions within the device, along with the electric field at different instants during the turn-off switching process. Initially, the depletion region expands towards the collector side by removing holes at the boundary. According to the charge control principle, the charge removed by the expansion of the depletion region must equal the charge removed due to the collector current flow, as explained in [61] and expressed in Eq. 2.8. Integrating this equation and applying the boundary conditions, as detailed in [61], enables the determination of the depletion region's evolution over time, as given by Eq. 2.9.

$$J_{C,on} = q \cdot p_{depl,boundary}(t) \frac{dW_{depl}(t)}{dt} \tag{2.8}$$

$$W_{depl}(t) = L_a \cdot acosh \left\{ \frac{J_{C,on} sinh(\frac{W_N + W_B}{L_a})}{q \cdot L_a \cdot p(W_{B+})} t + cosh(\frac{W_{depl}(0)}{L_a}) \right\} \tag{2.9}$$

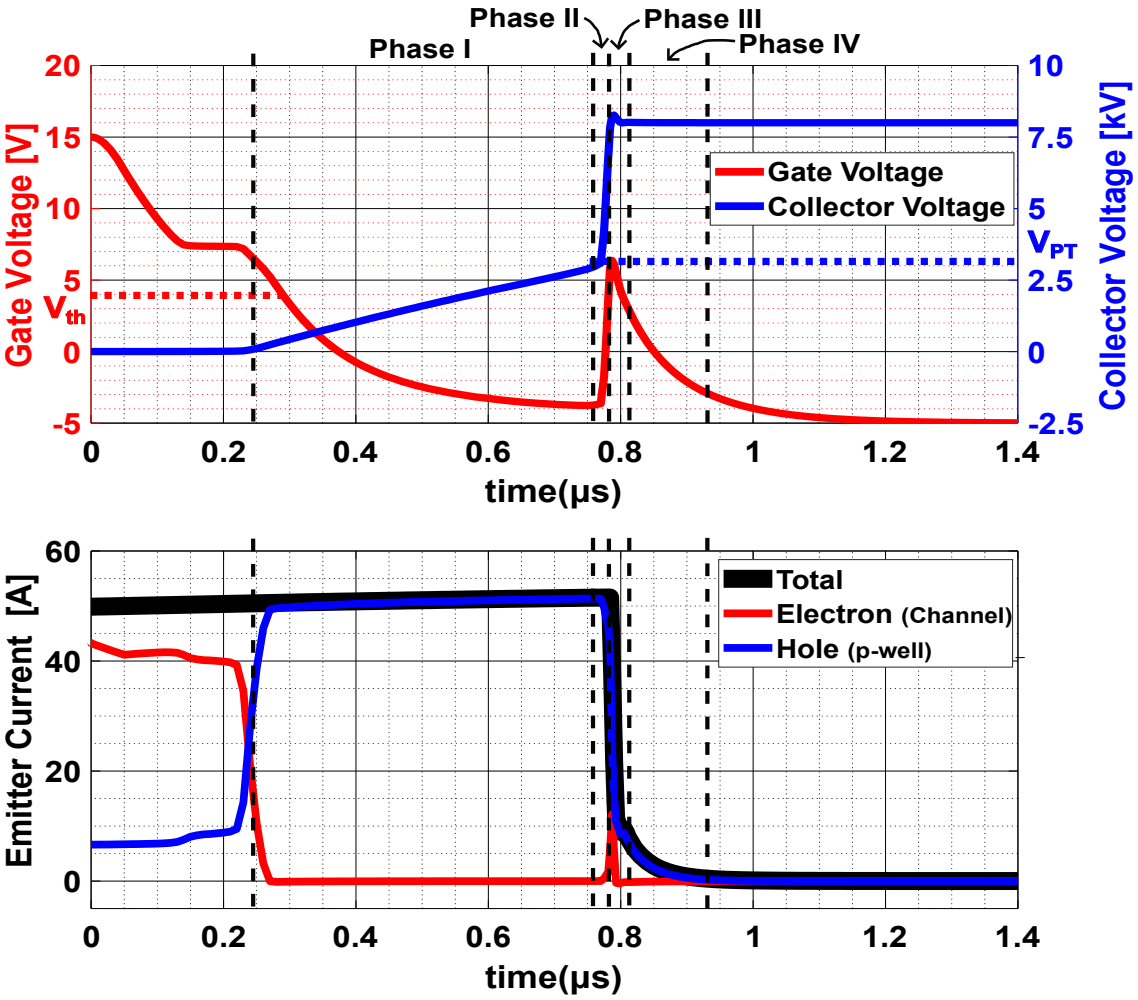


Figure 2.10: IGBT voltages and currents during the inductive turn-off process.

Where $J_{C,on}$ is the collector current density at the beginning of the turn-off process, defined as the collector current normalised to the active area of the device, $p_{depl,boundary}$ is the hole density at the depletion region boundary, $W_{depl}(t)$ is the evolution of the depletion region with time, L_a is the ambipolar diffusion length in the drift region, $W_{depl}(0)$ the space charge region width at the beginning of the turn-off process and $p(W_{B+})$ the hole density in the boundary between the drift and buffer layer.

The collector voltage is related to the depletion region width by Eq. 2.10, taking into account the positive charge in the depletion region due to the collector current flow, as specified in Eq. 2.11, and assuming that the holes are moving at their saturation drift velocity ($v_{sat,p}$) due to the high electric field in the depletion region.

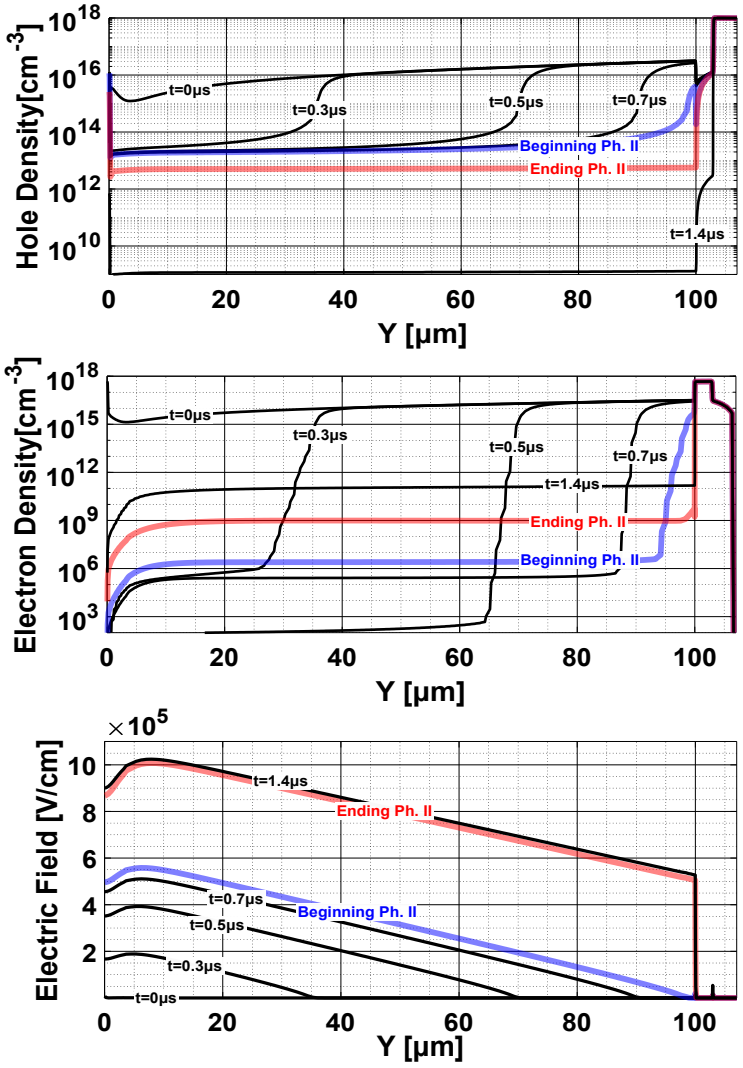


Figure 2.11: Hole distribution, electron distribution and electric field across the IGBT for different time instances during the inductive turn-off process.

$$V_C(t) = \frac{q \cdot (N_D + p_{depl}) W_{depl}^2(t)}{2\epsilon_s} \tag{2.10}$$

$$p_{depl} = \frac{J_{C,on}}{q \cdot v_{sat,p}} \tag{2.11}$$

Thus, the space charge width and collector voltage increase at a rate determined by the injected hole concentration and the total current density. Additionally, the electric field slope is constant according to Poisson's equation (Eq. 2.12).

$$\frac{dE}{dx} = \frac{\rho}{\epsilon_s} = \frac{q(N_d + p_{depl})}{2\epsilon_s} \tag{2.12}$$

The slow voltage rising phase ends when the space charge region reaches the buffer layer. The voltage at which the space charge region reaches the buffer layer (PT voltage V_{PT}) is given by Eq. 2.13, where replacing the $W_{depl}(t)$ with W_N in Eq. 2.10. After that time, the electric field slope increases according to Eq. 2.12 due to the higher doping density of the buffer layer and the Electric field takes a trapezoidal shape.

$$V_C(t) = \frac{q \cdot (N_D + \frac{J_{C,on}}{q \cdot v_{sat,p}}) W_N^2}{2\epsilon_s} \tag{2.13}$$

The time required for the collector voltage to reach the DC bus voltage after the punch-through can be given by integrating the charge control principle equation (Eq. 2.8), applying boundary conditions at the beginning and end of the second phase of the voltage-rising period, leading to Eq. 2.14:

$$\Delta t = \frac{q}{J_{C,on}} \Delta W_{depl,buffer} [p(starting) - p(ending)] \tag{2.14}$$

In this equation, $p(starting) - p(ending)$ represents the change in hole concentration during this period, and $\Delta W_{depl,buffer}$ is the depletion region width within the buffer layer, calculated using Eq. 2.10 with $N_D = N_B$ and $\Delta V_c = (V_{CC} – V_{PT})$.

The origin of the high $\frac{dV}{dt}$ can be explained by examining the hole density at the beginning and end of the high voltage rising phase in Fig. 2.11. This figure shows the hole density and electric field at the beginning and end of the fast voltage rising phase in blue and red, respectively. As expected by the analytical description above, the space charge region width and the amount of holes to be removed are

small, leading to a fast voltage transient. This fast collector voltage transient causes a voltage spike on the gate electrode due to the capacitive coupling between the gate and the collector, as shown in Fig. 2.10, a phenomenon explained in detail in Chapter 5.

After the collector voltage reaches the DC bus voltage, the diode can be forward-biased and conduct current. However, the current does not instantaneously drop to zero due to the remaining plasma in the drift and buffer layers of the IGBT. The recombination of this plasma, occurring at different rates owing to the different doping concentrations in these layers, results in two distinct phases: a fast exponential current decay (Phase III) and a subsequent slower phase (Phase IV) during the current falling period of the inductive turn-off process.

2.4.2 Inductive load turn-on

Figure 2.12 shows the voltage and current waveforms of the low-side IGBT ($IGBT_{1L}$) and a high-side freewheeling PiN diode (D_{1H}) during the turn-on process of $IGBT_{1L}$ of Fig. 2.8 under an inductive load of 20 A. A generic SiC PiN model was used for this simulation results to quantitatively present the inductive turn-on phases. The turn-on process of the IGBT can be divided into two phases, as depicted in Fig. 2.12. Before the turn-on process, the load current flows through D_{1H}. The turn-on process is initiated by applying a gate voltage higher than the threshold voltage of the IGBT. When the gate voltage surpasses the threshold, the IGBT 's current begins to increase, transferring the load current from the diode to the IGBT (Phase I). However, similar to the IGBT turn-off process, the injected plasma in the intrinsic region of the diode needs to be removed for the diode to support the DC bus voltage. The removal of this plasma is indicated by a negative current (i_{AK}) between the anode and cathode of the diode during Phase II, known as the reverse recovery current, which increases the turn-on switching losses of the IGBT.

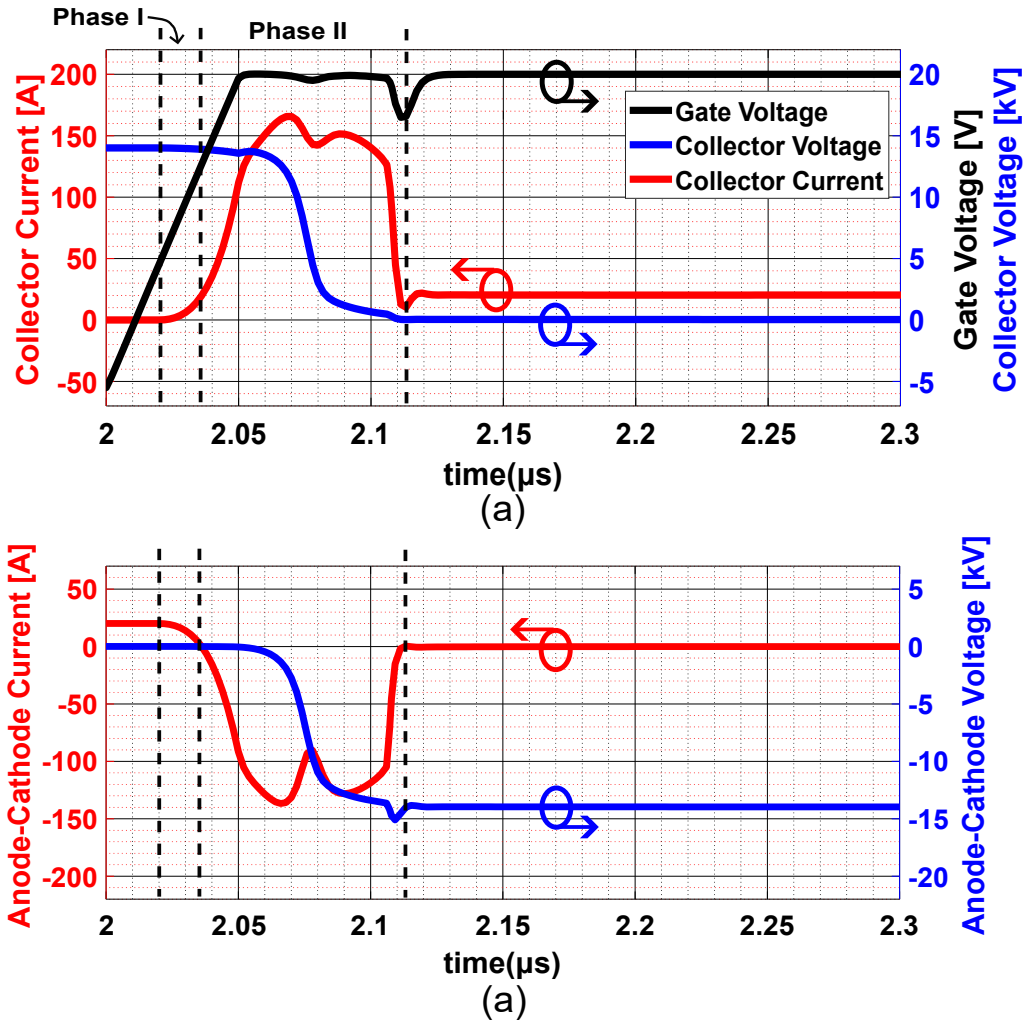


Figure 2.12: (a) IGBT and (b) diode voltages and currents during the inductive turn-on process.

The reverse recovery charge of the diode is a crucial characteristic determining the converter losses. This charge can be calculated by integrating the reverse recovery current from the beginning to the end of Phase II. After this phase, the IGBT is fully turned on and conducts the load current.

It is important to note that the choice of diode significantly influences the turn-on characteristics of the IGBT. Figure 2.13 compares the collector current and voltage waveform during the inductive turn-on of an IGBT using either a SiC Schottky or SiC PiN diode as the freewheeling device. A larger current overshoot is observed with the PiN diode, attributed to its higher reverse recovery charge. Thus, the IGBT structure does not significantly impact the turn-on switching characteristics,

allowing for independent optimisation of the IGBT by only considering the turn-off switching transient.

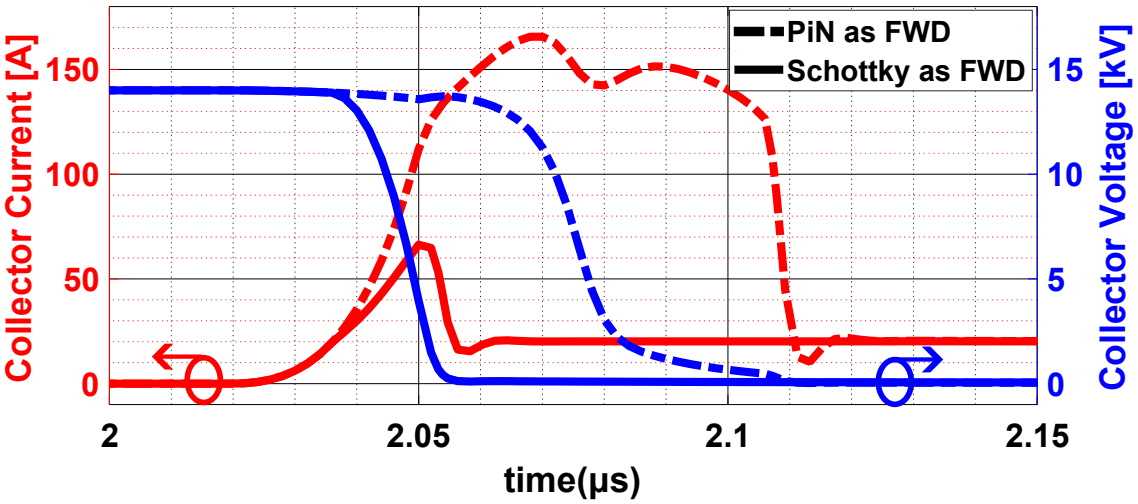


Figure 2.13: Simulated inductive turn-on switching comparison of an IGBT using PiN and Schottky freewheeling diodes.

2.5 Concluding remarks

This chapter presented an overview of the SiC IGBT structures that have been proposed, along with their static and dynamic characteristics. The reduced drift region thickness required for the asymmetrical IGBT structure to achieve a given breakdown voltage reduces the on-state and switching losses and makes it the preferred structure. This is the reason why this thesis is focused on the asymmetric, planar, n-type IGBT structure.

Chapter 3

Performance and Ruggedness

The previous chapter introduced and explained the operational characteristics of SiC IGBTs. This chapter presents a literature review on efforts to optimise the performance and reliability of SiC IGBTs. Given that optimisation typically involves numerous simulation iterations before actual device fabrication, this chapter initially details the simulation tools currently employed for predicting and optimising device performance.

3.1 SiC IGBT device modeling

Despite nearly three decades of research on SiC IGBTs, these devices remain in the development stage. Challenges associated with the Electromagnetic Interference (EMI), the SiC/SiO_2 interface properties and low manufacturing yield hinder their commercialisation. Consequently, virtual prototyping and accurate modelling of SiC IGBTs are crucial for device and circuit designers to comprehend their characteristics, optimise device structure, and predict their performance and reliability.

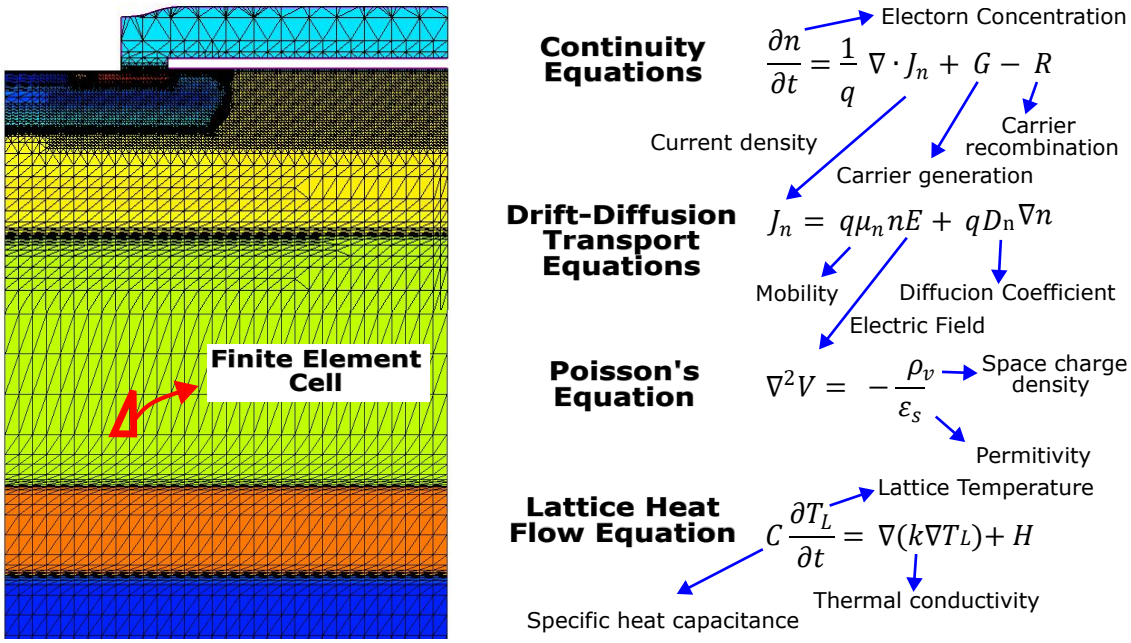
Power electronic device models are typically categorised into two primary groups.

The first group includes analytical Finite Element Method (FEM) Technology Computer-Aided Design (TCAD) models, which offer valuable insights into the physical phenomena within an elementary cell. These models are instrumental in optimising cell design but are not suitable for simulating power converter topologies due to their computational intensity. The second group comprises compact models divided into physics-based and behavioural subcategories. These models are mathematical representations designed to simulate a specific device's current and voltage waveforms without delving into cell design details.

3.1.1 Finite element TCAD modeling

The two most prominent commercially available software packages for SiC-based power electronic devices are Sentaurus TCAD from Synopsys and Silvaco. Both offer functionalities for simulating fabrication and characterising virtually fabricated devices under various conditions.

This modelling approach involves dividing the device geometry into finite elements (cells), a process known as meshing (see Fig. 3.1(a)), and solving fundamental physics-based electrical. thermal and mechanical equations for each element as depicted in Fig.3.1(b). These equations require parameters such as mobility, doping concentration, or thermal conductivity, which depend on other variables like temperature or fabrication conditions. Due to the complex interdependencies of these models, substantial effort is required to validate them, ensuring the simulation results are accurate and the model can effectively predict the device's performance. Chapter 4 delves into the accuracy of TCAD models in capturing the SiC material properties and the characteristics of IGBTs.



(a) (b)

Figure 3.1: (a) Typical meshing of an IGBT half-cell, (b) Physics-based equations for TCAD simulations.

3.1.2 Compact modeling

Several compact models for SiC IGBTs have been developed, offering faster simulation times compared to TCAD by employing equivalent circuits and simplified mathematical equations. Most of these models are physics-based variations of the silicon IGBT model introduced by Hefner et al. [62]. Hefner's model describes the operation of an n-IGBT as a power MOSFET providing the base driving current for a PNP transistor, as detailed in Section 2.3. Figure 3.2 presents a detailed equivalent circuit superimposed on the IGBT cell, which includes the parasitic capacitances of both the BJT and MOSFET components.

Several variations of Hefner's model have been proposed for both silicon [63] and SiC IGBTs [64], all based on the equivalent circuit in Fig. 3.2. The initial physical model specifically for SiC IGBTs was proposed by [65], accurately modelling the static and dynamic behaviours of symmetrical IGBT structures. [66] focused on the distinctive characteristics of asymmetrical SiC IGBT structures during inductive

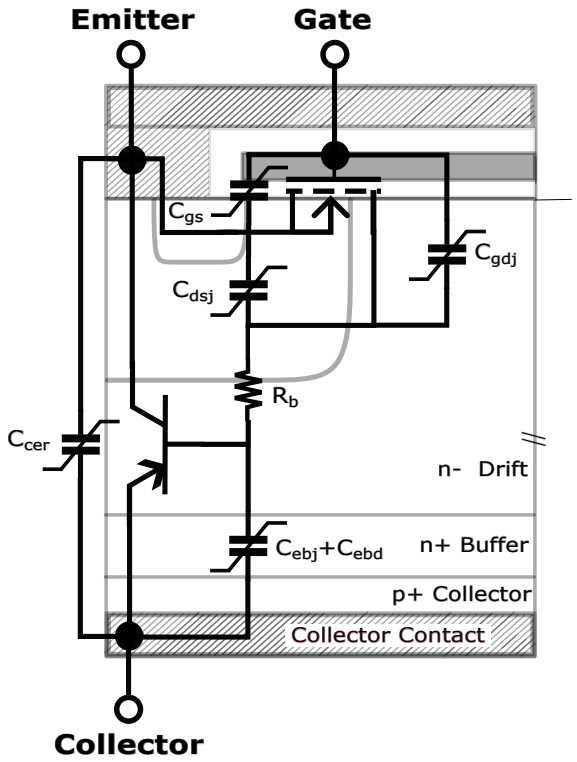


Figure 3.2: Equivalent circuit of IGBT used in Hefner's compact model.

turn-off, elucidating punch-through behaviour through finite element simulations. The developed model accurately predicts the asymmetrical IGBT behaviour by modelling the carrier distribution within the buffer and drift layers. This model was later expanded in [67] to include temperature variation impacts on carrier density, lifetime, and interface traps. Other researchers, such as [68] and [69], have also conducted similar studies, highlighting the speed advantage of these models over finite element-based counterparts. However, it's important to note that the accuracy of these models is far from perfect, and parameter extraction can be complex. This issue is addressed by our proposed compact model, the first behavioural model for SiC IGBTs, which is introduced in Chapter 9.

3.2 Static and dynamic performance optimisation

The static and dynamic performance of SiC IGBTs has been thoroughly investigated through finite element simulations and experimental validation. A key focus is the trade-off relationship between on-state and switching performance in SiC IGBTs, primarily due to the conductivity modulation's opposite effects during the conduction and switching states. Enhanced on-state performance, achieved by injecting higher levels of plasma into the drift region, leads to increased turn-off duration and switching losses, as this plasma must be removed during turn-off. This subsection provides a literature review on strategies proposed to control this trade-off, the influence of various structural IGBT parameters on on-state and switching characteristics, and innovative designs intended to improve IGBT performance.

Figure 3.3 illustrates the conventional optimised IGBT structure. For clarity, the device structure is divided into three sections: the collector side, the drift layer, and the emitter side, with optimisation strategies for each section detailed below.

3.2.1 Collector side optimisation

The collector side comprises the p_{++} injector (or collector) and the n_{+} buffer layer. While both components significantly influence the conductivity modulation of the drift layer, there is a lack of studies focusing on the optimisation of injector parameters. Conversely, considerable research has been directed towards optimising the buffer layer. An early study by Tomohiro et al. [70], using 2D numerical simulations, was among the initial efforts to explain the punch-through behaviour of SiC IGBTs by examining the internal carrier distribution within the drift and buffer layers during inductive turn-off. Their findings indicated that modulating the minority carrier lifetime in the buffer layer between 0.02 and 0.5 μs significantly alters on-state and switching characteristics. Increasing the minority carrier lifetime from 0.1

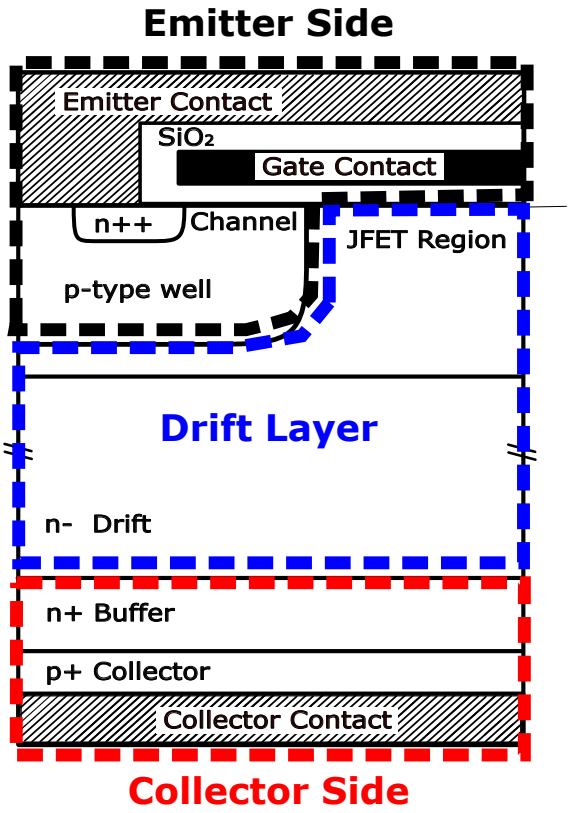


Figure 3.3: Conventional SiC IGBT structure.

to 0.5 μs resulted in a 250% rise in stored excess carriers and nearly a 500% increase in turn-off duration at 175°C, showing the importance of developing techniques to control carrier lifetimes in the buffer layer.

Similar effects on the on-state and switching performance are observed with buffer layer doping concentration and thickness variations, as discussed in [9, 71]. Figure 3.4 displays typical trade-off curves between on-state voltage drop and switching losses for simulated IGBTs with different buffer layer doping concentrations and thicknesses.

These results have also been experimentally validated in [72], where the authors controlled the backside carrier injection by controlling the buffer layer concentration and thickness. Although carrier lifetime control in the buffer layer is feasible, as reported in [73], the preference for controlling doping concentration and thickness is attributed to the challenges in achieving localised lifetime control.

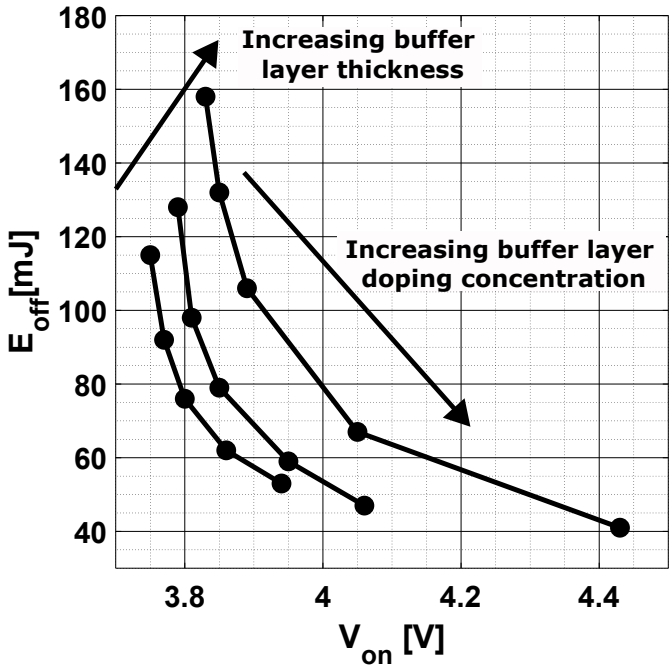


Figure 3.4: Simulated on-state voltage drop and turn-off switching losses trade-off curves for different buffer layer doping concentrations and thicknesses of a simulated 10 kV-rated SiC IGBT.

3.2.2 Drift layer optimisation

The doping concentration and thickness of the drift region in IGBTs are primarily dictated by the desired blocking voltage and the specific type of IGBT structure, whether symmetrical or asymmetric. For asymmetrical IGBT structures, the breakdown voltage is linked to the drift layer's doping concentration, its thickness, and the current gain of the wide base parasitic PNP transistor, as elaborated in Subsection 2.2. A study by Tamaki et al. [9] conducted a quantitative analysis of p-type IGBTs. It demonstrated that a specific breakdown voltage can be achieved with various combinations of drift layer doping concentrations and thicknesses, as illustrated in Fig.3.5, where the horizontal line at 19 kV crosses multiple curves.

Tamaki et al.'s study indicated that the selection of doping concentrations and thicknesses at the 19 kV intersection points did not significantly impact the on-state voltage drop. However, subsequent research by Deng et al. [74] suggested that opting for the lowest drift layer doping concentration within the range of

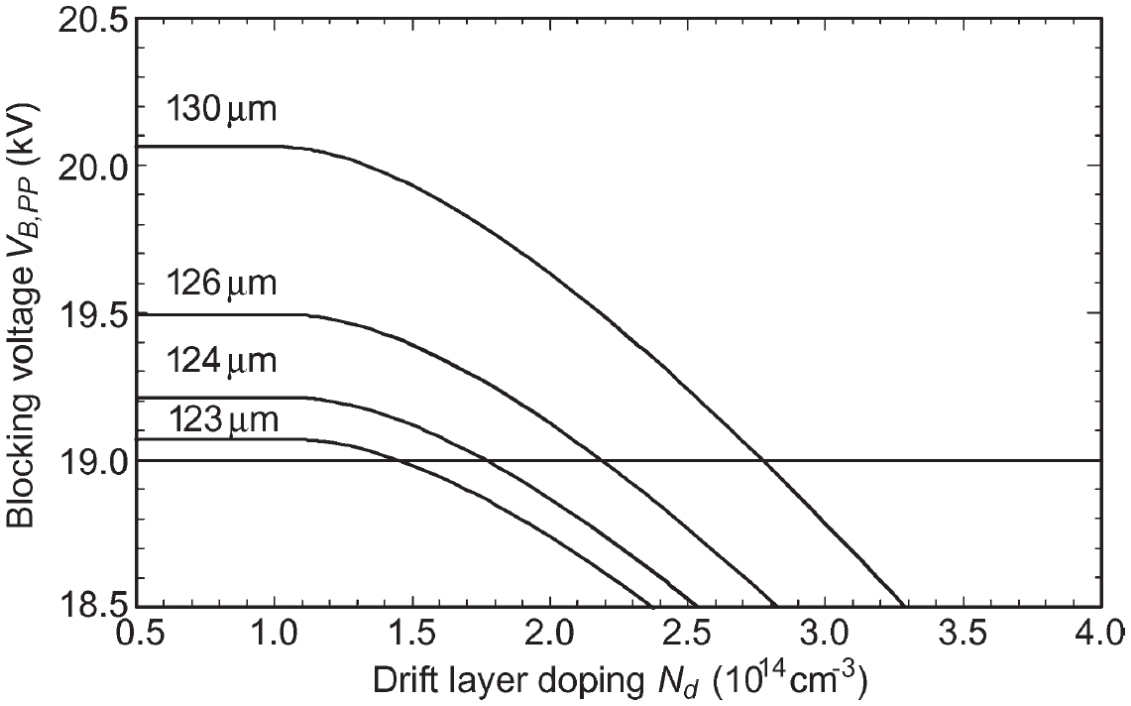


Figure 3.5: Dependence of breakdown voltage (around 19 kV) on drift layer doping for different drift layer thicknesses [9].

$1 - 4 \times 10^{14} cm^{-3}$ results in an improved trade-off between static and dynamic losses. This improvement is attributed to a thinner drift layer and reduced carrier injection. In addition to doping concentration and thickness, the lifetime within the drift region also influences conductivity modulation levels, thereby affecting the trade-off between on-state and switching characteristics. This relationship has been confirmed through both simulation [74, 75] and experimental studies [10, 12, 60].

3.2.3 Emitter side optimisation

Optimising the emitter side of an IGBT, alongside the buffer and drift layers, can significantly enhance its performance. Studies indicate that the emitter side design predominantly affects the on-state performance, while its impact on dynamic performance is less studied.

Using a highly doped layer on top of the drift layer can reduce the on-state voltage

drop by decreasing the resistance in the JFET region due to the more effective current spreading at the corner of the p-well and enhanced electron injection from the emitter side. Both n-type and p-type IGBTs have utilised this highly doped layer, with thicknesses ranging from 0.3 to 3.0 μm and doping concentrations between 8×10^{15} and $2 \times 10^{17} cm^{-3}$ [52, 76, 77, 78]. Researchers have referred to this layer using various terms like current spreading layer (CSL), current enhancement layer (CEL), or Charge Storage Layer (CSL), but they essentially serve the same purpose.

Figure 3.6 illustrates the carrier distribution during the on-state and the electric field during the blocking state in a vertical cutline on the JFET region of the structure shown in Fig.3.3. Figure3.6(a) depicts the impact of the CSL on carrier distribution due to enhanced carrier injection from the emitter side through the channel. However, as seen in Figure 3.6(b), the higher doping concentration in the CSL leads to an increased electric field peak, reducing the blocking capability.

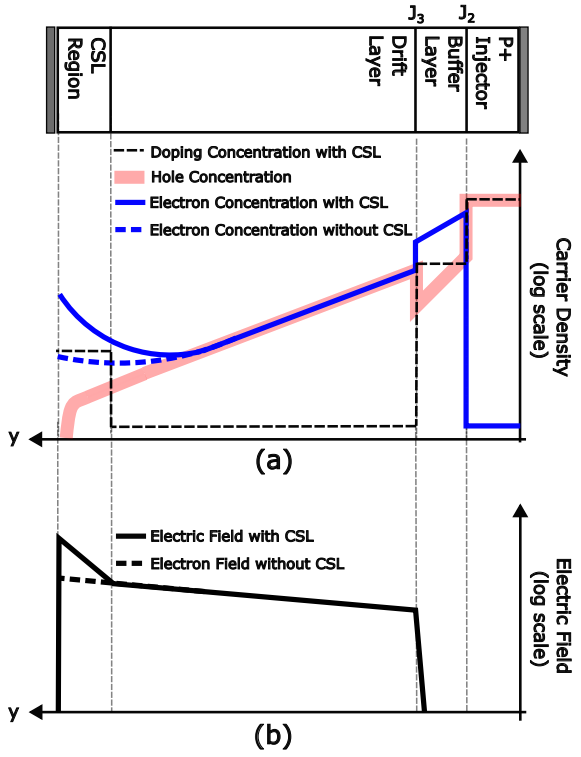


Figure 3.6: (a) Carrier density during the on-state and (b) electric field distribution during the blocking state for the IGBT structure with and without the usage of the Charge Storage Layer (CSL). Cut along the JFET region.

Two other optimisation parameters are the channel and JFET region widths. Smaller channel width reduces the channel resistance and, therefore, the on-state voltage drop. The fabrication process determines the minimum channel width and is limited to about 0.5μm. Even smaller channel width is possible to be fabricated, similarly to what happens to lower voltage SiC MOSFETs, but the on-state voltage drop reduction saturates after a point due to the small portion of the channel voltage drop out of the total on-state voltage drop.

The influence of JFET width on the on-state voltage drop is more complex. A wider JFET width reduces the JFET resistance and the on-state voltage drop of the JFET portion. Conversely, a larger JFET width increases the cell pitch, leading to fewer parallel cells per die area, which raises the on-state voltage drop [9, 76]. Lastly, cell layout optimisation at the die level can further improve on-state performance. As reported in [79], the on-state voltage drop of a 6.5 kV-rated SiC IGBT at 100 A/cm^2 current density was reduced from 4.81V to 3.98V by replacing the stripe layout with a box layout and implementing a hole-barrier layer to enhance conductivity modulation by preventing hole flow out of the emitter. However, this study did not present results regarding switching performance.

3.2.4 Novel SiC IGBT structures

This subsection presents recent studies on innovative device structures designed to surpass the performance and ruggedness of conventional SiC IGBTs. These novel designs primarily focus on modifications to the emitter side, collector side, or the drift region of the SiC IGBT (refer to Fig. 3.3).

Improvements targeting the collector side of IGBTs are focused towards enhancing turn-off switching characteristics by facilitating faster plasma extraction. Yan-Juan Liu et al. [80] introduced a structure incorporating an n-p-n collector to create

an electron extraction path. Similar approaches, such as the multi-zone collector design with alternating high and low-doped p-regions, were explored in [81, 82]. These designs aim to form lower potential barriers at the buffer-collector interface, thus accelerating carrier extraction during turn-off. A complex structure proposed in [83] uses poly-silicon-filled trenches in the collector to improve turn-off switching losses. Additionally, Erjun Wang et al. [84] suggested a heterojunction IGBT integrating a poly-silicon region in the buffer layer to create a natural potential well for excess carrier storage during turn-off. These simulation studies indicated potential turn-off energy loss reductions exceeding 80%, albeit with decreased on-state performance and increased fabrication complexity.

For emitter side optimisations, trench gates (as discussed in Chapter 2) and the Charge Storage Layer (CSL) (refer to Fig. 3.3) have proven effective in IGBTs and are now considered conventional. Xiaochuan Deng et al. [85] proposed a hybrid IGBT structure that combines vertical and horizontal channel paths, merging the benefits of trench-gate and planar IGBTs. This structure exhibited enhanced performance in both on-state and turn-off conditions due to improved electron injection and an additional hole current path during turn-off. A similar performance boost in conduction and switching states was achieved with the trench-gate clustered IGBT structure [86].

Finally, structural modifications are also feasible apart from only optimising the doping concentration and thickness of the drift region. The super-junction IGBT structure, successful in silicon devices, can be adapted for SiC IGBTs to achieve a better trade-off between on-state and switching performance, as indicated in [87]. However, the technology to fabricate uniform n and p pillars in long drift regions required for SiC IGBTs is not available yet.

3.3 Challenges and concerns of SiC IGBTs

The static and dynamic behaviour of SiC IGBTs has been extensively studied as described in the previous sections based on experimental and simulation studies. Additionally, the performance of IGBTs rated for up to 50kV has been predicted using TCAD simulations [88], and these devices seem to be the most favourable for high-voltage and high-current grid applications. However, there are several less studied IGBT characteristics, such as the high dV/dt produced during the switching transients, the short-circuit capability, the high voltage isolation requirements and the reliable parallel operation of the devices. The following subsections present the undergoing research focused on understanding these characteristics and proposing ways to address them.

3.3.1 EMI and ruggedness issues caused by the extremely high dV/dt

Chapter 2.4 detailed the switching behaviour of SiC IGBTs, highlighting the high dV/dt rates encountered during inductive turn-off, often reaching several hundred $kV/\mu s$. These rates present several challenges in power module packaging and converter design. Primarily, they are a significant source of EMI, potentially disrupting nearby circuits and indirectly affecting IGBT 's reliability. They also complicate gate driver circuit design, necessitating high voltage isolation with minimal coupling capacitance [89]. In applications involving electric motors, such high dV/dt rates can lead to insulation failure in motor windings, compromising system reliability [90]. Additionally, these rates can directly damage the IGBTs themselves, as capacitive coupling between the gate and collector may trigger false turn-on and short-circuiting [91].

Various solutions have been proposed to address these challenges. At the topology

level, strategies include implementing large EMI filters [92], advanced gate drivers to control gate voltage and switching speed [89, 91], novel isolated power supplies to reduce coupling noise [93, 94], and capacitors between the gate and emitter of SiC IGBTs to enhance false turn-on ruggedness [88]. While these techniques improve system reliability, they increase complexity and cost and reduce efficiency.

In contrast, device-level solutions aim to tackle the root causes of high dV/dt issues. For example, Watanabe et al. [95] demonstrated a 6.5 kV-rated IGBT featuring a two-step drift layer with varied doping concentrations, which can limit the depletion region during turn-off within the drift region, thereby reducing the high dV/dt phase. Similarly, Liu et al. [96] showed that a buffer layer with stepped doping concentration can control charge removal, reducing the maximum dV/dt during turn-off. However, these studies have not fully explored the impact of reduced dV/dt on the trade-off between on-state and switching losses.

3.3.2 SiC IGBT behaviour under short-circuit conditions

The reliability of power converters heavily depends on the performance of power electronic devices under short-circuit conditions. Studies indicate that IGBTs account for approximately 34% of failures in converter systems, with short-circuit being a prevalent mode of failure [97, 98]. These failures often stem from external factors such as false gate triggering or load short-circuiting. A short circuit can permanently damage an IGBT due to the simultaneous high voltage and current, causing excessive power losses and elevated lattice temperatures. Furthermore, the push for increased power density in IGBTs, achieved through conductivity modulation in the drift region, leads to smaller chip sizes. This miniaturisation, however, reduces the Short Circuit Withstand Time (SCWT) capability of SiC IGBTs.

Current research on the short-circuit behaviour of SiC IGBTs is limited. Kumar et

al. [99] provided experimental data suggesting that SiC IGBTs may not withstand a short-circuit condition for the standard 10 μs duration expected of silicon IGBTs. Similar findings are published in studies by Konishi et al. and Kim et al. [100, 101]. In response, there has been a focus on developing new device structures to enhance SCWT [86, 102], optimising cell layouts [100] and designing gate drivers capable of detecting and resolving short-circuit faults in under 3 μs [89, 103]. Despite these efforts, a comprehensive understanding of the SiC IGBT 's short-circuit phenomenon remains incomplete.

3.3.3 Parallel operation of SiC IGBTs

High-power applications require devices capable of handling several kilovolts (kV) and kiloamperes (kA). Unlike silicon thyristors, which can be produced on four-inch silicon discs to manage over three kA, SiC IGBTs face a limitation in active area size, typically not exceeding a few square centimetres. This limitation arises from the complexities in fabrication and lower manufacturing yields for larger-area devices. To date, the larger area SiC IGBTs demonstrated include those by Ryu et al. [57] and Brunt et al. [23], with active areas of 0.42 cm^2 and 0.37 cm^2 respectively. Consequently, achieving a kA rating in SiC IGBTs often requires paralleling multiple dies in a power module, and for higher power applications, paralleling multiple modules may be necessary. Thus, the ability to operate SiC IGBTs in parallel is crucial.

A key characteristic for devices to be effectively paralleled is the positive temperature coefficient of the on-state voltage drop [104, 105]. A negative temperature coefficient of the on-state voltage drop can cause uneven current distribution among paralleled dies, power modules, or cells within a die, jeopardising system reliability. Ryu et al. [105] observed that the temperature coefficients for electron and hole current paths in an IGBT differ: hole current increases at higher temperatures due

to increased plasma injection and carrier lifetimes, while electron current decreases due to reduced mobility, similar to unipolar devices. Consequently, the overall temperature coefficient of an IGBT is influenced by its structure and fabrication conditions. For instance, IGBT structures with CSL discussed in [105] and the 13kV IGBT in [100] exhibited negative temperature coefficients, whereas the 27kV IGBTs in [10] showed positive coefficients. However, a detailed study encompassing the temperature coefficient across different IGBT structures and the influence of device parameters on it is yet to be conducted in the literature.

3.3.4 High voltage blocking capability

The high voltage blocking capability of a SiC IGBT is primarily determined by its active and edge termination region design, as shown in Fig. 2.3. While the breakdown voltage in the active area of the IGBT is mainly dictated by the buffer and drift region doping concentrations and thicknesses, as explained in subsection 2.2, this analysis overlooks two critical aspects. The electric field crowding at the corner of the p-well and the peak electric field at the gate oxide during the blocking state, as illustrated in Fig. 3.7, are common failure points in high voltage blocking states, prompting numerous studies aimed at enhancement.

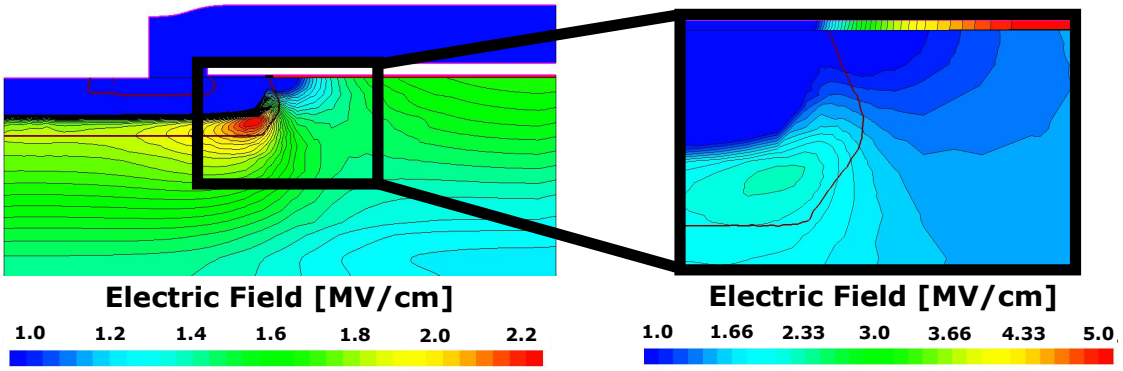
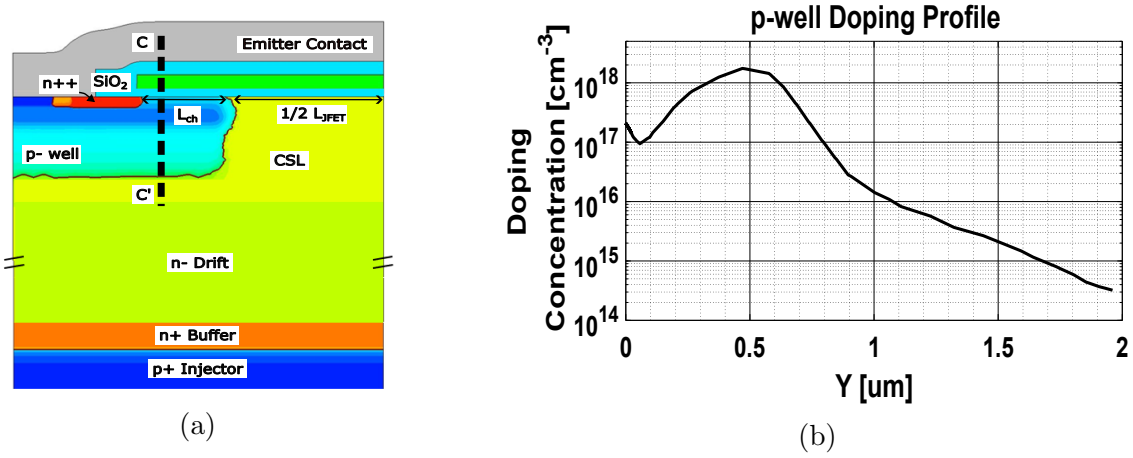


Figure 3.7: Electric field distribution during the IGBT blocking state around the p-well corner and on the gate oxide.

Amit K. Tiwary et al. [106] extensively analysed the use of a retrograde p-well in

SiC IGBTs rated above 10 kV, using TCAD simulations. The retrograde doping profile in the p-well has a lower doping concentration in the channel region, with a peak concentration at about 0.5 μm depth, which gradually decreases, as shown in Fig. 3.8. This profile improves breakdown characteristics in three ways. Firstly, it allows independent adjustment of the doping concentration at the channel and peak regions through different implantation doses and energies. This enables the use of various channel doping and oxide thickness combinations to achieve the desired gate threshold voltage. For instance, a 5-7 V threshold voltage can be attained with a 100 nm thick gate oxide, compared to the 50 nm required for a conventional p-well, reducing the peak electric field and increasing IGBT 's reliability. Secondly, the lower doping concentration at the bottom and corner of the p-well effectively reduces the electrostatic distribution's curvature and electric field crowding during the blocking state. Thirdly, the high peak doping concentration in the p-well eliminates the possibility of punch-through in the emitter region.



(a) (b)

Figure 3.8: (a) IGBT cell structure and (b) p-well doping profile across cutline C-C'.

In addition to the p-well, the JFET region significantly influences the breakdown characteristics of SiC IGBTs. An optimally designed JFET region can effectively shield the gate oxide from the electric field from adjacent p-well regions, thus impacting the device's performance. Meng Zhang et al. [107] highlighted the trade-off between the on-state voltage drop and the peak electric field at the gate oxide.

IGBTs with narrower JFET widths are better at shielding the gate oxide from electric fields, but they increase the on-state voltage drop due to increased JFET resistance. To address this, they proposed the incorporation of multiple floating p-islands within the JFET region. This design protects the gate oxide and allows for using longer JFET regions. The proposed structure demonstrated an improved trade-off between on-state voltage drop and maximum electric field at the gate oxide without necessitating additional fabrication steps compared to conventional structures.

However, it is essential to note that the maximum breakdown voltage achievable in the active area of an IGBT is typically not fully achieved in real devices. This reduction, often ranging from 5-20%, is attributable to edge termination's efficiency. Moreover, the edge termination length in devices rated over 10 kV can exceed 1 mm, occupying a significant portion of the die area. As depicted in Figure 3.9, a termination region with a length of 1 mm can consume up to 36% of the total die area of a $1cm^2$ die. Consequently, both the efficiency and the size of the termination area indirectly influence the trade-off between the conduction and blocking characteristics of the IGBT, making these factors crucial in the design and optimisation of high-voltage SiC IGBTs.

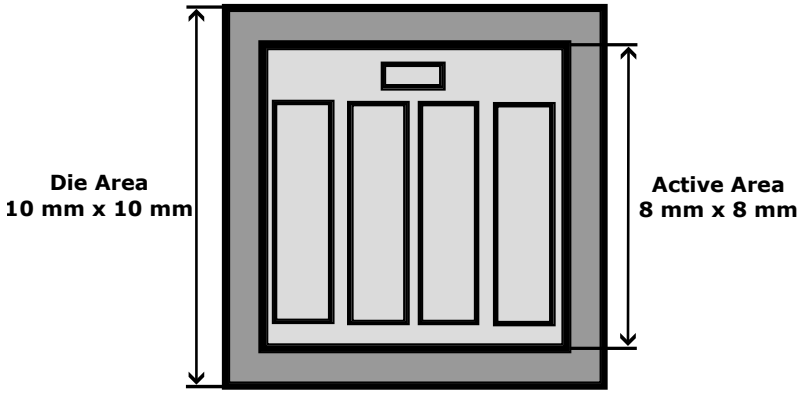


Figure 3.9: Active and edge termination area of a die with a total area of 1 cm^2.

Devices with breakdown voltages exceeding 10 kV are typically fabricated using edge termination techniques that fall into three main categories: implantation,

etching, or a combination of both, as shown in Fig. 3.10. Floating Field Rings (FFR) and Single Zone Junction Termination Extension (SZ-JTE) represent the simplest ion implantation techniques. Devices utilising FFR have achieved breakdown voltages up to 27kV [10, 23, 108, 109], but the technique requires numerous rings and consumes a significant die area (as high as 1.6mm for a 22kV-rated IGBT [23]). SZ-JTE, while requiring less area, faces limitations due to a narrow optimal implantation dose window and sensitivity to interface charges [11, 110].

To address the narrow implantation dose window, Multi-Zone Junction Termination Extension (MZ-JTE) structures with two [11, 111, 112], three [113], or more zones [72, 114] have been introduced. MZ-JTE structures offer a wider optimal dose window but increase fabrication complexity and cost, as each additional zone necessitates an extra mask and implantation step. Additionally, careful optimisation of zone lengths is required to prevent electric field peaks at zone interfaces.

The Space Modulated Junction Termination Extension (SM-JTE) [12, 115, 116] is a highly efficient ion implantation-based technique that combines the low area consumption of SZ-JTE and MZ-JTE with the wider implantation dose window of FFR. Using this method, a 27 kV-rated SiC IGBT was fabricated with a termination length of just 700 μm [12].

Etching techniques offer an alternative approach, as demonstrated in [13] with the use of a V-shaped blade to achieve breakdown voltages around 10 kV. However, the hardness of SiC material can lead to increased leakage current and reduced breakdown voltages. However, achieving the necessary small bevel angles for high-efficiency termination, such as the estimated 0.05^o angle for devices rated above 30 kV [117], is challenging with conventional etching.

A more practical etching approach is the multiple-step etching [14], which forms zones of varying depths and lengths in the termination region. While sensitive to etching depth, adding micro-trenches within these zones can improve breakdown

characteristics and reduce sensitivity to fabrication uncertainties [15, 118, 119, 120]. The Aperture Density Modulation (ADM) technique [16, 121] represents a simplified one-step approach, utilising direct photolithography and etching (P/E) with a single graded mask, resulting in a customised slope profile after post-baking.

Lastly, simulation studies have explored composite implantation-etched techniques, combining the advantages of various methods. For instance, shallow trenches in floating field rings have been proposed to enhance breakdown voltage and reduce edge termination area [122, 123]. However, these techniques often require multiple additional fabrication steps, adding complexity to the manufacturing process.

3.4 Concluding remarks

This chapter presented a literature review of the work that has been done on SiC IGBT, including structure optimisation for loss reduction and enhancement of the safe operational area. The impact of the most critical structural parameters on the IGBT characteristics was identified. The challenges that need to be faced were summarised, including EMI problems caused by the high dV/dt, reduced short withstand capabilities compared to silicon IGBTs, the need for efficient edge termination methods and lack of fast and accurate simulation models.

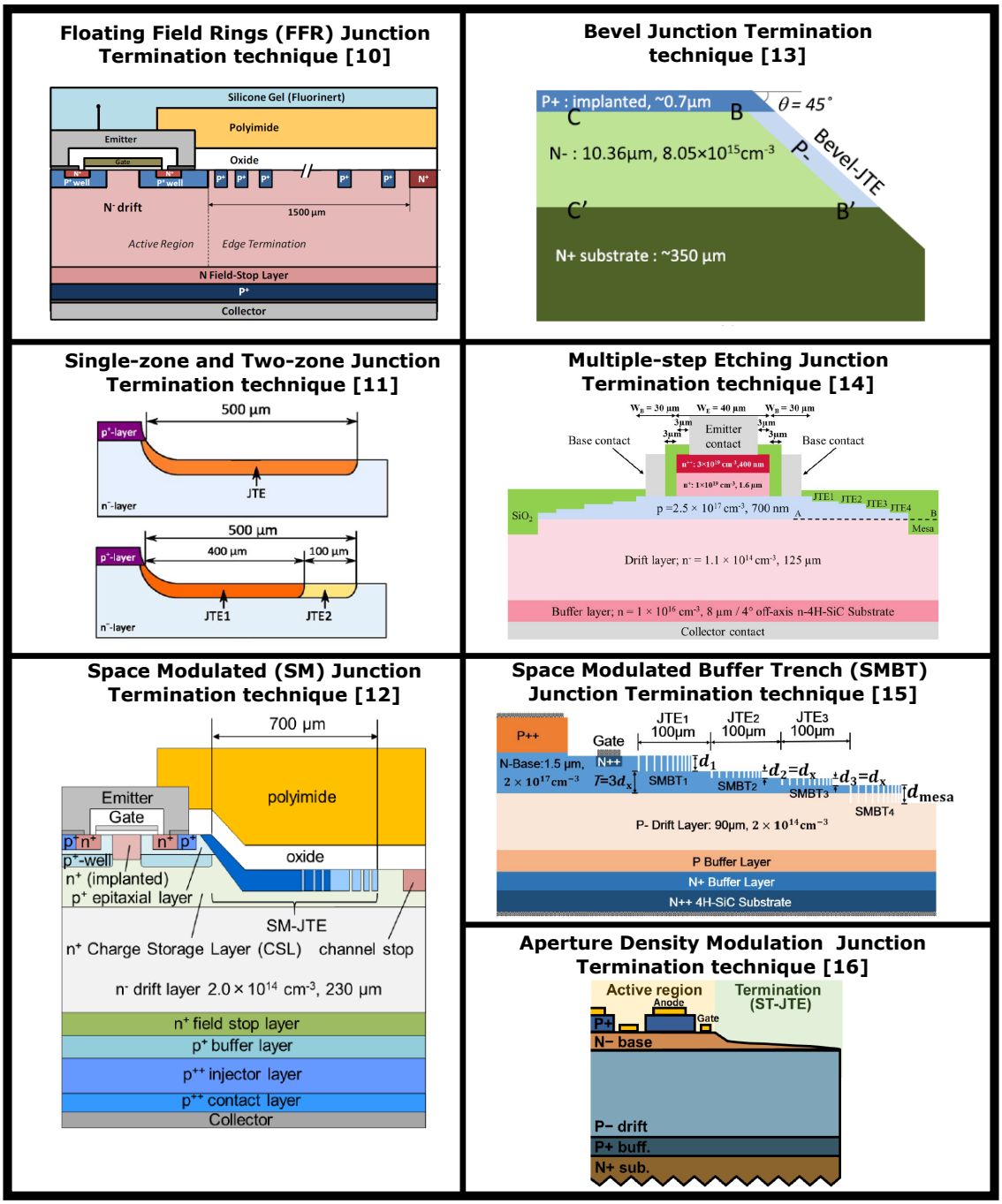


Figure 3.10: Junction termination techniques for SiC devices rated at >10 kV ([10, 11, 12, 13, 14, 15, 16]).

Chapter 4

TCAD Modeling and Characterisation

This chapter outlines the methodology employed for accurately simulating and predicting SiC IGBT performance. The Sentaurus TCAD suite from Synopsis was utilized, employing the SPROCESS tool for simulating the fabrication process and the SDEVICE for characterizing the virtually fabricated devices. Sections 4.1 and 4.2 detail the key functionalities of the SPROCESS and SDEVICE tools in SiC IGBT modelling. Section 4.3 demonstrates the model's accuracy by correlating simulation results with experimental data from fabricated devices.

Part of the work presented in this chapter has been published in *I. Almpanis et al., "Silicon Carbide n-IGBTs: Structure Optimisation for Ruggedness Enhancement," in IEEE Transactions on Industry Applications, Jan. 2024.*

4.1 Fabrication process simulation

The fabrication of a SiC IGBT involves numerous steps, such as epitaxial growth, multiple p-type and n-type implantations at varying doses and energies, SiC oxidation, chemical etching of various materials, and high-temperature annealing. These processes are comprehensively described in the textbook by Kimoto [1]. Various fabrication methods for SiC IGBTs, each incorporating distinct steps, are documented in the literature [25, 55, 76, 78].

Figure 4.1 illustrates the sequence of fabrication steps implemented in Sentaurus TCAD. For the simulation results presented in this thesis, the fabrication process starts from a p-type substrate and not from the n-type, as described in [54], achieving identical modelling accuracy and reduced simulation time. Although the IGBT structure could be alternatively modelled using Sentaurus's SDE tool, which requires only the geometry and doping concentrations, the SPROCESS tool was chosen to construct more representative models. For instance, the geometry of the p-well is influenced not just by the implantation mask but also by the lateral straggling of aluminium dopants at various implantation energies and doses [124, 125]; a phenomenon modelled well using SPROCESS. The models used to simulate the different fabrication steps have been previously calibrated based on experimental results [126, 127].

Device meshing is also critical, impacting the model's speed, accuracy, and convergence. The mesh must be denser at interfaces between different materials, layers with varying doping concentrations or regions with high current density (e.g., the channel region). Conversely, dense meshing does not necessarily enhance model accuracy in large, uniform areas like the drift region. Figure 4.1 also depicts typical device meshing, highlighting in darker areas the denser meshing applied selectively in critical regions to balance accuracy and simulation speed.

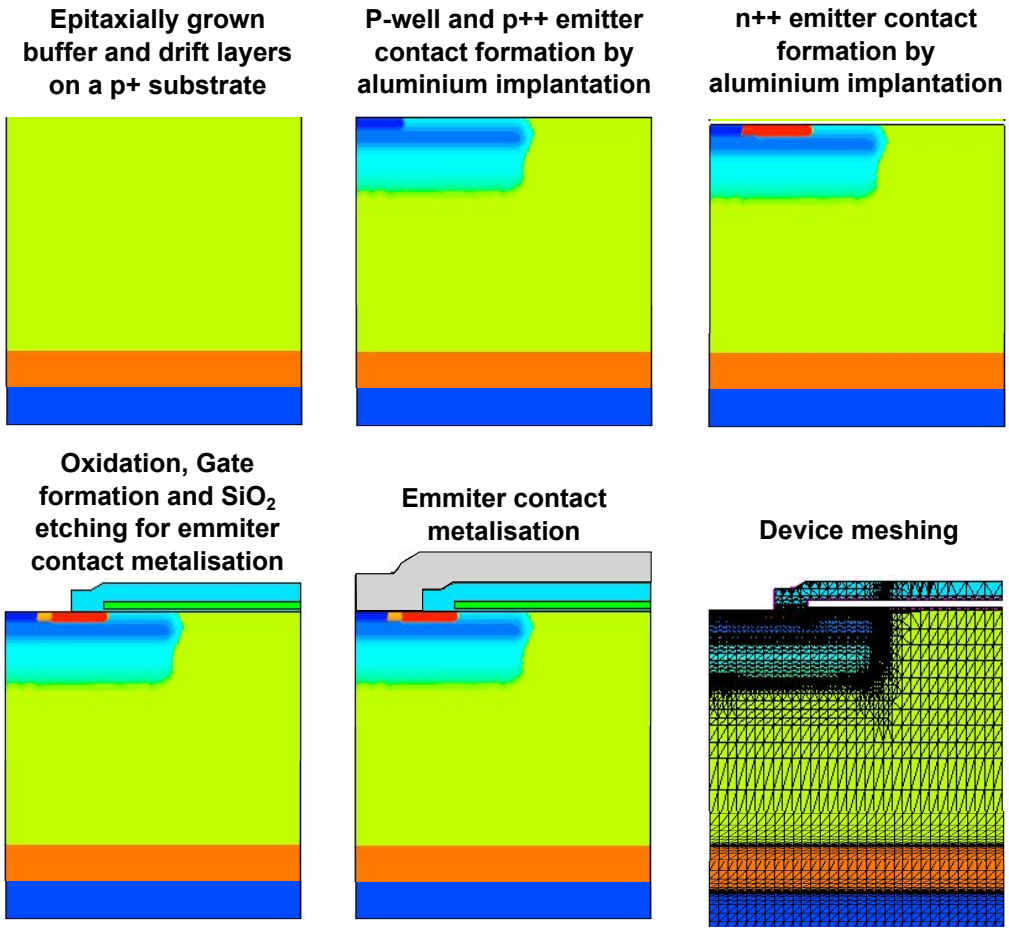


Figure 4.1: Sequential steps in the simulation of the SiC IGBT fabrication process.

4.2 Device characterisation using validated models for material properties

Following the virtual fabrication and meshing of the device, its performance is evaluated by applying various electrical and thermal boundary conditions externally or by integrating it into a Spice-like network, as depicted in Fig. 4.2. As detailed in subsection 3.1.1, for each simulation step and at every mesh node, a series of electrical and thermal equations are solved (refer to Fig. 3.1). The parameters employed in these equations are material-specific and are influenced by factors such as doping concentration, temperature, and fabrication conditions. Accurate simulation results depend critically on the ability of TCAD models to accurately reflect these dependencies.

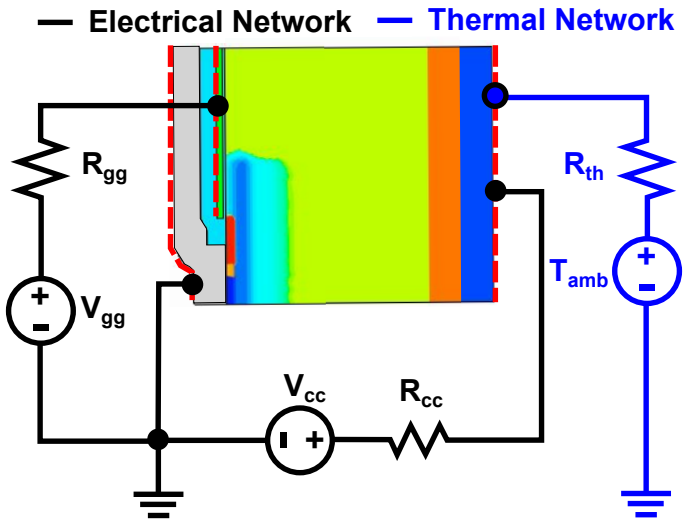


Figure 4.2: Illustration of a Spice network connecting the virtually fabricated IGBT cell with external components for device characterization.

Key material properties that significantly influence the behaviour of SiC IGBTs include electron and hole mobilities, saturation drift velocity, incomplete ionization of donors and acceptors, minority carrier lifetimes in both drift and buffer layers, and the presence of fixed charges and traps at the oxide/semiconductor interface.

4.2.1 Carrier mobilities

The dependencies of electron and hole mobilities on doping and temperature are influenced by scattering mechanisms due to interactions of free carriers with lattice atoms or ionized donor and acceptor atoms. Sentaurus TCAD models the temperature dependence of mobility using Eq.4.1. Additionally, several models for doping-dependent mobility are supported in TCAD simulators, including the Masetti model [128] and the Arora model [129]. This study employs the Masetti model, as described by Eq. 4.2, with coefficients calibrated using experimental results published for 4H-SiC material.

$$\mu_{const} = \mu_L \left(\frac{T}{300K} \right)^{-\zeta} \tag{4.1}$$

$$\mu_{dop} = \mu_1 + \frac{\mu_{const} - \mu_2}{1 + \left(\frac{N_{A,0}+N_{D,0}}{C_r}\right)^a} \tag{4.2}$$

Figure 4.3 illustrates electron and hole mobilities' doping and temperature dependence under low electric fields, as modelled in TCAD. The experimental data have been taken from [17, 18, 19], where simple test structures were employed for carrier mobility measurements.

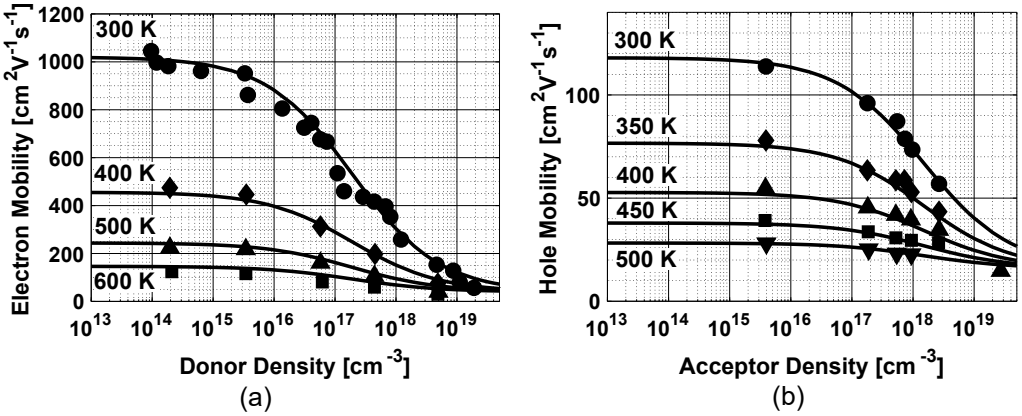


Figure 4.3: Depiction of low-field electron and hole mobility across regions with various donor and acceptor doping concentrations. Solid lines represent TCAD-modelled mobilities, while discrete experimental points are taken from [17, 18, 19].

The carrier velocity is proportional to the electric field in low electric fields. However, under high electric fields during IGBT operation, carriers accelerate, and their interaction with optical phonons leads to saturation in drift velocity [1]. To model this saturation effect in high electric fields, the Canali model [130] is utilized in TCAD simulations, as defined by Eq. 4.3. The parameters b and v_{sat} in this model are temperature-dependent, as indicated in Eq. 4.4 and 4.5.

$$\mu(E) = \frac{\mu_{low}}{\left[1 + \left(\frac{\mu_{low} E}{v_{sat}}\right)^{\beta}\right]^{1/\beta}} \tag{4.3}$$

$$\beta = \beta_0 \left(\frac{T}{300K}\right)^{\beta_{exp}} \tag{4.4}$$

$$v_{sat} = v_{sat,0} \left(\frac{300K}{T} \right)^{v_{sat,exp}} \tag{4.5}$$

TCAD models for drift velocity under high electric fields have been validated against experimental data presented in [20] at temperatures of 296 K (23 °C) and 593 K (320 °C), as depicted in Fig. 4.4.

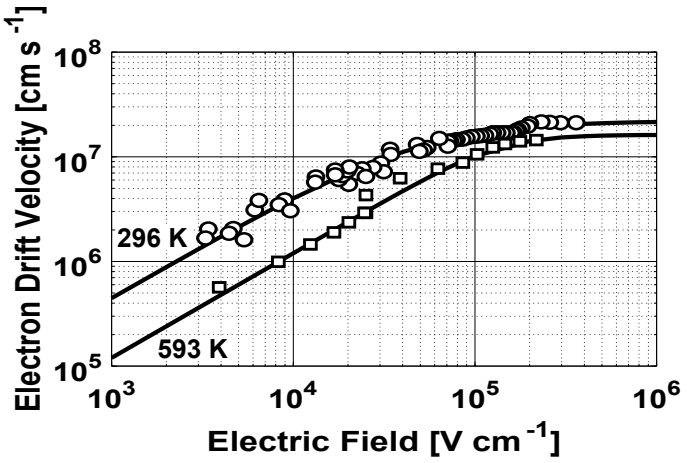


Figure 4.4: Comparison of TCAD modelling and experimental data [20] for electron drift velocity versus electric field at various temperatures.

4.2.2 Incomplete ionisation of dopants

In contrast to silicon, where dopants are mostly fully ionized at room temperature, dopants in SiC exhibit relatively deep levels, necessitating the consideration of incomplete ionization. For instance, Aluminium, the primary p-type dopant in 4H SiC, has an ionization energy of approximately 200 meV. Nitrogen and phosphorus, commonly used as n-type dopants, have ionization energies of around 60 meV. Owing to their lower ionization energies, n-type dopants are often considered fully ionized at room temperature. However, accurately modelling the incomplete ionization of aluminium dopants is crucial for the precision of the model. Sentaurus TCAD models the activated donor and acceptor atoms as per Eq. 4.6 and 4.7. These equations account for temperature and doping dependence, reflecting

bandgap narrowing effects on activation energy.

$$N_D = \frac{N_{D,0}}{1 + g_D \frac{n}{N_c exp\left(-\frac{\Delta E_D}{kT}\right)}} \tag{4.6}$$

$$N_A = \frac{N_{A,0}}{1 + g_A \frac{p}{N_v exp\left(-\frac{\Delta E_A}{kT}\right)}} \tag{4.7}$$

The incomplete ionization models implemented in Sentaurus TCAD have been calibrated using analytical functions detailed in [1]. Figure 4.5 displays the ionized fractions of Aluminium and nitrogen atoms across various doping concentrations and temperatures ranging from 300 K to 600 K, as indicated by solid lines. The dashed lines represent the TCAD-modelled ionized dopant fractions for typical doping concentrations in buffer and injector layers of SiC IGBTs. The simulation results indicate that 83% of the buffer dopants and only 4% of the collector dopants are activated at room temperature.

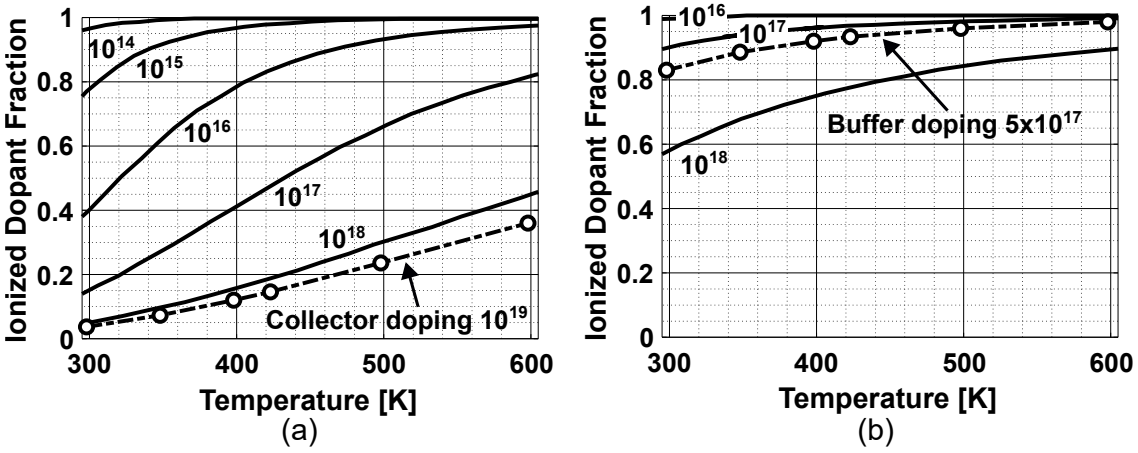


Figure 4.5: Ionization fractions for (a) Aluminium acceptors and (b) Nitrogen donors at different doping concentrations and temperatures. Solid lines denote values calculated by analytical functions from [1], while dashed lines represent TCAD-modelled results.

4.2.3 Minority carrier lifetime

The recombination of free carriers significantly influences device characteristics. This effect is particularly pronounced in bipolar devices like IGBTs, where high levels of minority carrier injection occur during operation. The dominant recombination mechanisms are deep-level and Auger recombination, as schematically represented in Fig. 4.6.

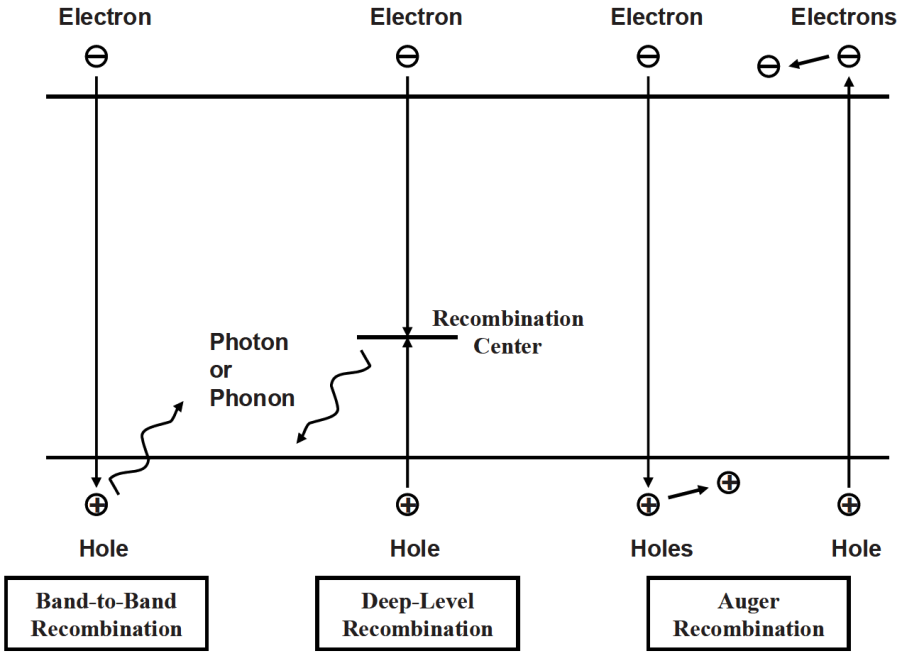


Figure 4.6: Recombination processes in a semiconductor [21].

Deep-level recombination, also known as Shockley-Read-Hall (SRH) recombination, involves an electron from the conduction band and a hole from the valence band recombining via a recombination centre within the energy band gap. Sentaurus TCAD implements this process as per Eq. 4.8, where E_{trap} denotes the energy difference between the intrinsic level and the deep level. The lifetimes τ_n and τ_p are modelled as functions of doping and temperature, as indicated in Eq. 4.9.

$$R_{net}^{SRH} = \frac{np - n_{i,eff}^2}{\tau_p \left[n + n_{i,eff} exp\left(\frac{E_{trap}}{kT}\right)\right] + \tau_n \left[p + n_{i,eff} exp\left(\frac{-E_{trap}}{kT}\right)\right]} \tag{4.8}$$

$$\tau(T, N_{A,0} + N_{D,0}) = \tau_{min} + \frac{\tau_{max} - \tau_{min}}{1 + \left(\frac{N_{A,0}+N_{D,0}}{N_{ref}}\right)^{\gamma}} \left(\frac{T}{300K}\right)^{\alpha} \tag{4.9}$$

Auger recombination becomes significant in heavily doped regions or under high-level injection conditions in lightly doped areas. This process, wherein the energy and momentum from electron-hole recombination are transferred to a third particle, is modelled in Sentaurus TCAD as per Eq. 4.10, with temperature-dependent coefficients C_p and C_n.

$$R^A_{net} = (C_n n + C_p p)(np - n^2_{i,eff}) \tag{4.10}$$

Considering both recombination processes, the effective recombination lifetime is calculated using Matthiessen's rule (Eq. 4.11), with τ_{SRH} and τ_A defined as per Eq. 4.12 and 4.13 [21]. The excess electron and hole concentrations are represented by δn and δp, respectively. It is assumed for the drift region of the IGBT, which operates under high plasma injection levels, that $\delta n = \delta p$ to maintain charge neutrality. However, this assumption does not hold for the buffer layer, which operates under low-level injection conditions (refer to Fig. 3.6). Figure 4.7 illustrates the temperature dependence of minority carrier lifetimes in the drift and buffer layers of an asymmetrical SiC IGBT, as modelled in TCAD. These results align well with findings published in literature [1, 21, 88].

$$\frac{1}{\tau_{eff}} = \frac{1}{\tau_{SRH}} + \frac{1}{\tau_A} \tag{4.11}$$

$$\tau_{SRH,n} = \frac{\delta n}{R^{SRH}_{net}} \quad and \quad \tau_{SRH,p} = \frac{\delta p}{R^{SRH}_{net}} \tag{4.12}$$

$$\tau_{A,n} = \frac{\delta n}{R^A_{net}} \quad and \quad \tau_{A,p} = \frac{\delta p}{R^A_{net}} \tag{4.13}$$

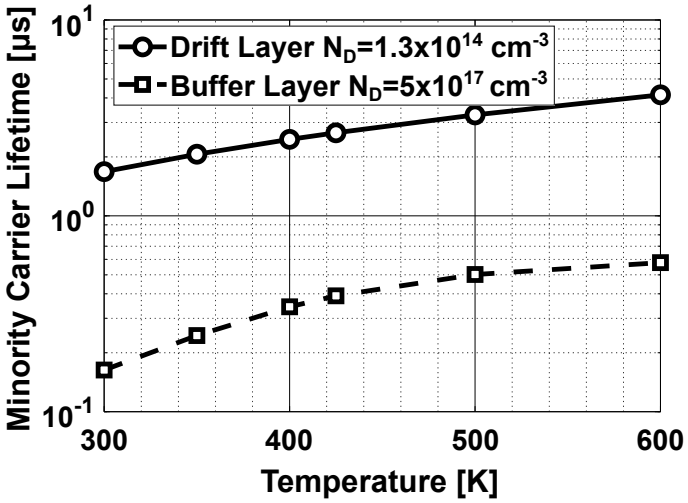


Figure 4.7: Temperature dependence of the minority carrier lifetimes on the drift and the buffer layer of an asymmetrical SiC IGBT.

4.2.4 Fixed charges and traps at the oxide/semiconductor interface

Substantial research efforts have focused on comprehending and precisely modelling the SiC/SiO_2 interface, which significantly influences the channel characteristics of Metal Oxide Semiconductor (MOS) devices. During SiC's thermal oxidation, various charges are generated in the SiO_2, SiC, or their interface. Notably, immobile charges near or at the interface, commonly known as fixed charges, are pivotal in shaping device characteristics. They serve as scattering centres, reducing channel mobility and affecting the threshold voltage. Concurrently, interface charges with energy levels within the silicon carbide's band gap can exchange carriers to and from the semiconductor. These are termed interface traps. When their energy level is close to the conduction band, they noticeably impact semiconductor device performance. These traps, either donor-like or acceptor-like, resemble doping impurities when occupied. Figure 4.8 schematically illustrates the distribution of

interface states in different SiC polytypes [1]. According to [1], donor-like interface states near the valence band are charged by trapped holes when the Fermi level is below their energy levels and act as positive fixed charges influencing the threshold voltage. However, they do not impact channel mobility, as they become neutral when the Fermi level moves up [131].

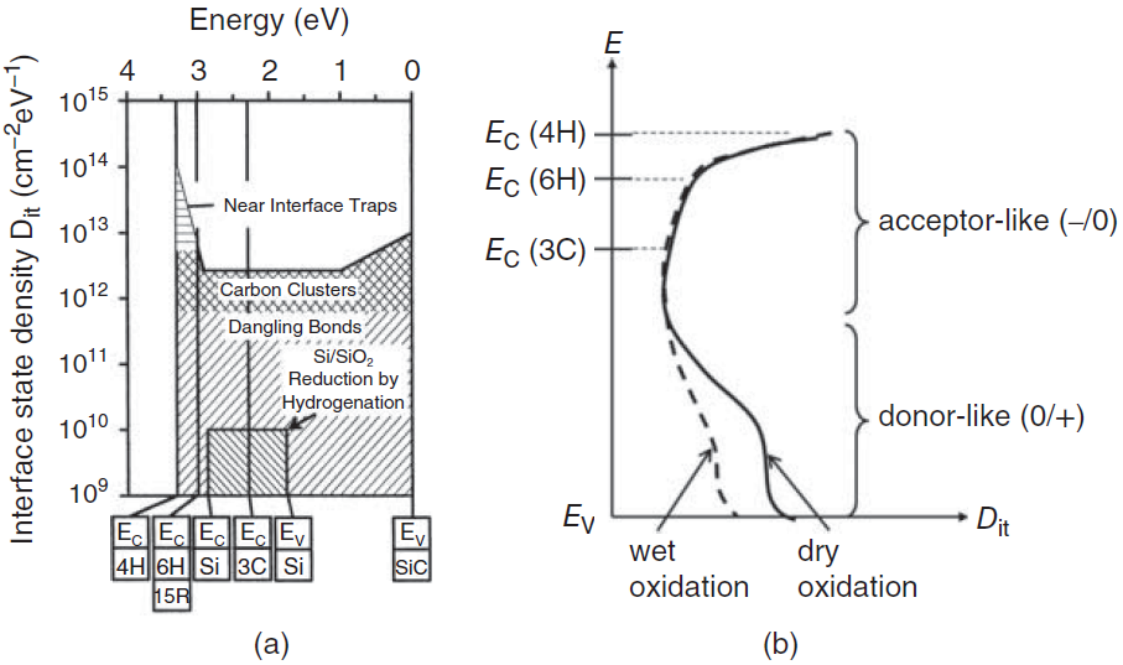


Figure 4.8: Schematic representations of interface states within the band gaps of different SiC polytypes. (a) Illustrates a model for the high density of interface state in SiC and its dependence on polytype, and (b) shows the schematic distribution of interface states in SiC MOS structures formed by dry or wet oxidation[1].

Conversely, traps near the conduction band, which are acceptor-like, become negatively charged with trapped electrons when these states are below the Fermi level. This electron trapping in the channel region adversely affects channel mobility. Hence, the high level of interface traps in 4H-SiC material contributes to the extremely low channel mobility, which can be as low as $5 - 8cm^2V^{-1}s^{-1}$ [1] in the absence of proper annealing.

It is acknowledged that, despite numerous studies on SiC interface states, their precise origins are not well known. Nonetheless, both the oxidation process and subsequent annealing significantly influence the density of interface traps. This

is evidenced in Fig. 4.9, which shows four different trap distributions near the conduction band [22]. Consequently, accurate TCAD modelling of IGBT's characteristics should incorporate both fixed charges and realistic interface trap profiles. Sentaurus TCAD facilitates this by including fixed charges, acceptor-like traps, and donor-like traps, thereby effectively modelling the oxide-semiconductor interface's physics. The trap distribution profile can be modelled using exponential distributions, Gaussian distributions, or a user-defined lookup table.

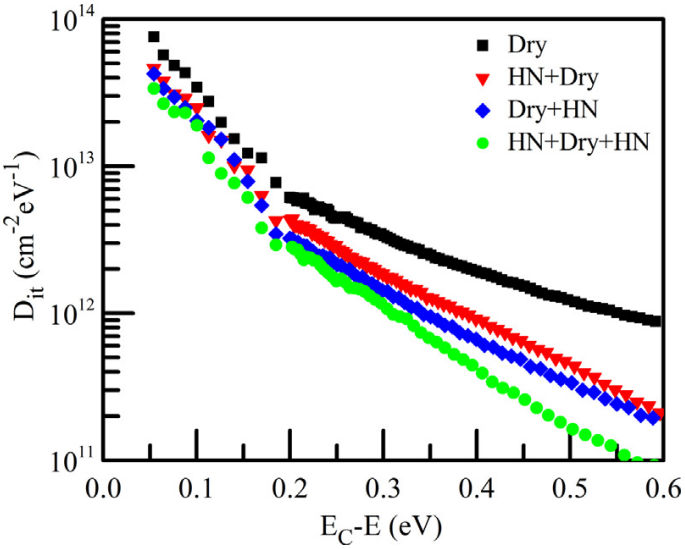


Figure 4.9: Distributions of interface trap density (D_{it}) ranging from 0.06 eV to 0.6 eV below the SiC conduction band in SiC MOS capacitors [22].

4.3 Modelling accuracy validation based on experimental results of fabricated SiC IGBTs

Developing an accurate SiC IGBT model is essential for exploring its electrical and thermal properties. This task necessitates an in-depth understanding of how material properties, fabrication process conditions, and structural parameters influence various device characteristics. The three pivotal characteristics of an IGBT are the blocking voltage capability, the on-state, and the switching performance. Table 4.1 summarises the effects of critical structural and process-dependent parameters on

SiC IGBT's characteristics, according to the literature review presented in Chapter 3. The analysis of Table 4.1 indicates that some parameters predominantly affect one characteristic, such as constant carrier generation and channel doping concentration. However, many parameters impact multiple characteristics, such as the buffer layer doping concentration and thickness that determine the trade-off relationship between the conduction and switching losses as depicted in Figure 3.4.

Table 4.1: Impact of the most critical structural and process dependent parameters on the IGBT characteristics.

Parameter	Blocking state	Conduction state	Turn-off switching
Collector thickness	minor	moderate	minor
Collector doping	minor	major	major
Buffer thickness/doping	moderate	major	major
Drift thickness/doping	major	minor	major
CSL thickness/doping	major	major	minor
Channel width	minor	moderate	minor
Channel doping	minor	major	minor
P-well doping	moderate	moderate	moderate
Oxide thickness	major	major	moderate
Carrier lifetimes	minor	major	major
Carrier mobilities	minor	major	moderate
Saturation velocity	minor	major	major
Interface fixed charge	minor	major	minor
Interface traps	minor	moderate	minor
Constant carrier generation	major	minor	minor

In the device model validation conducted for this study, an extensive set of published experimental data on SiC IGBT's behaviour was employed [10, 23, 24]. The determination of unknown structural and process-dependent parameters was guided by the iterative process outlined in the flowchart of Fig.4.10. Each iteration in this validation process involved conducting electrothermal TCAD simulations, analyzing the data, and selecting parameter values based on an in-depth understanding of the fundamental physical mechanisms and IGBT operation. The test circuit depicted in Fig. 4.11 (a) was utilized for static characterization (on-state and blocking state), while the chopper circuit in Fig. 4.11 (b) was used for dynamic characteri-

zation. The following subsections detail the various stages of the iteration process in developing a validated SiC IGBT model.

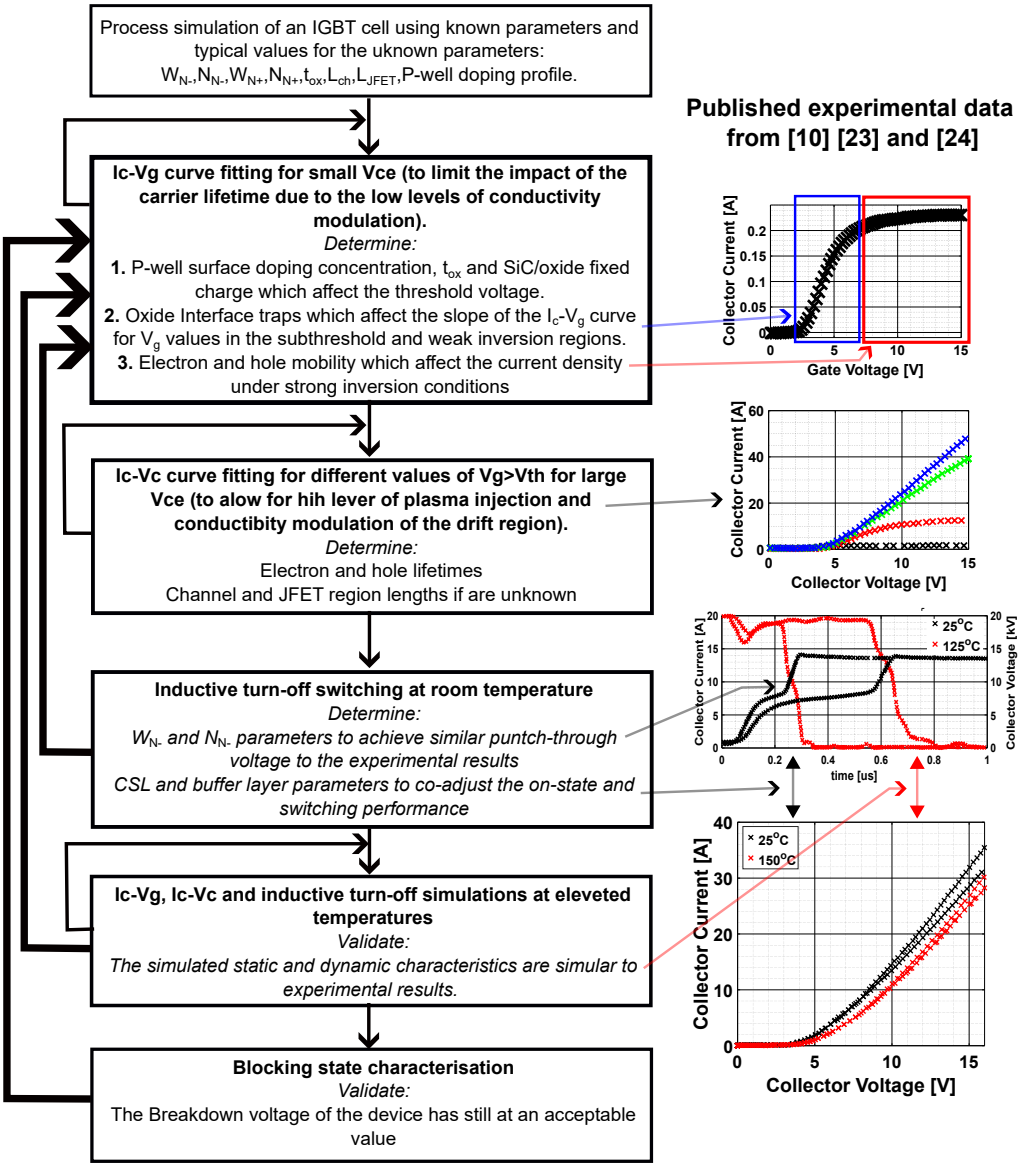
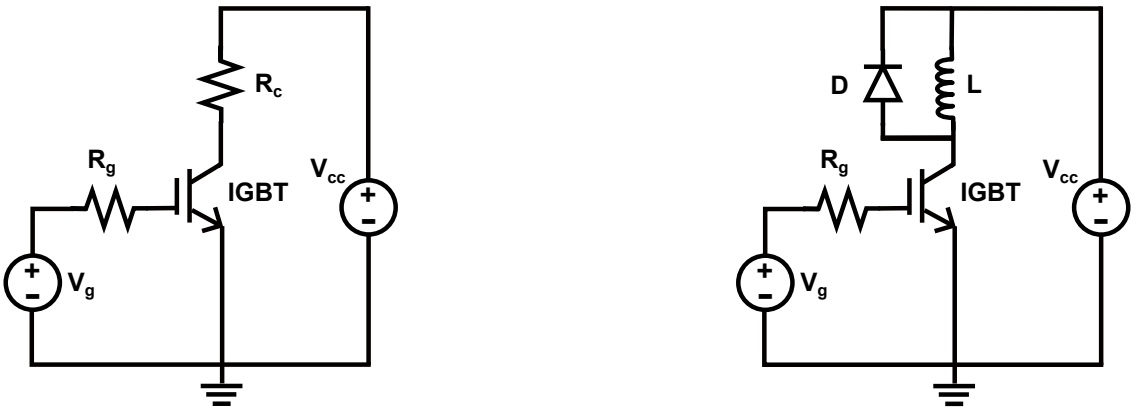


Figure 4.10: Flowchart outlining the validation process for the modelled IGBT performance, referencing experimental results from [10, 23, 24].

4.3.1 Fixed charges and traps in the oxide/semiconductor interface

The influence of fixed charge density at the oxide/semiconductor interface on the $I_c - V_{ge}$ transfer characteristics of the IGBT is highlighted in Fig. 4.12, with ex-



(a) (b)

Figure 4.11: Test circuits used for (a) static and (b) dynamic characterization of the IGBT.

perimental data derived from [24]. Since a low positive bias of 3.2 V has been used as V_{cc} of Fig. 4.11(a) for both simulation and experimental setup, the saturation current density and the minority carrier injection are low. As a result, the $I_c - V_{ge}$ curve is dominated by the channel characteristics, and thus, they can be determined. The simulated gate threshold voltage aligns well with the experimental data when using positive fixed charges with sheet concentration of $4.7 \times 10^{12} cm^{-2}$. However, the simulated $I_c - V_{ge}$ curve exhibits a significantly steeper slope compared to the experimental data. The gradual slope observed experimentally can be attributed to the trapping of electrons by acceptor-like traps near the conduction band, as depicted in Fig. 4.8, due to band bending induced by the positive gate voltage.

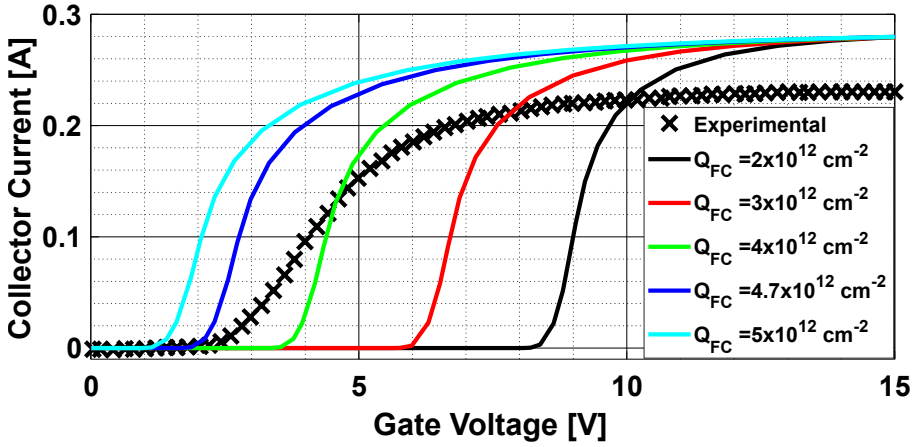


Figure 4.12: Effect of positive fixed charges on the $I_c - V_{ge}$ characteristics of the IGBT. The experimental data have been taken from [24].

Figure 4.13 illustrates the impact of different realistic trap distributions on the $I_c - V_{ge}$ curve's slope at low gate voltages. By employing a uniform distribution of interface traps with a density (D_{IT}) of $8 \times 10^{12} cm^{-2} eV^{-1}$ for energy levels $E_c - 0.1 < E < E_c$, a slope almost identical to the experimental data is achieved in the simulation.

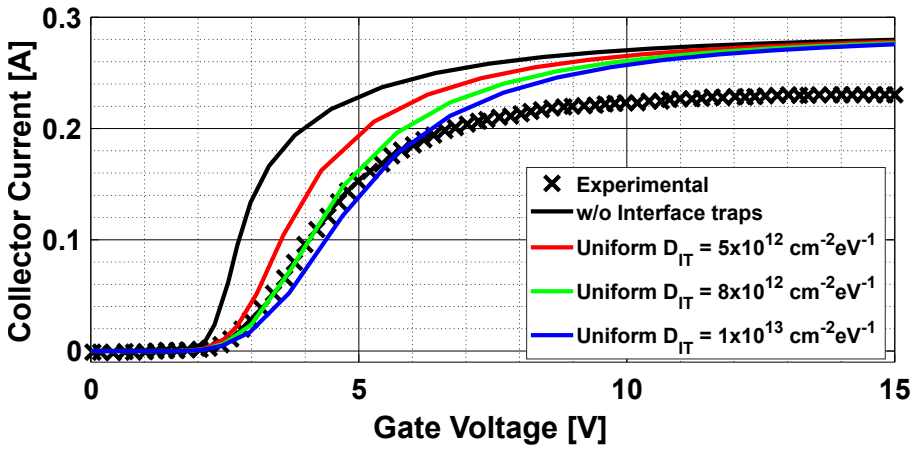


Figure 4.13: $I_c - V_{ge}$ curves for different interface trap distributions on the energy levels $E_c - 0.1 < E < E_c$.

However, it is important to note that interface traps located close to the conduction band edge within the band gap do not significantly influence the IGBT's behaviour during the on-state. This is evident as they are nearly fully occupied for gate voltages exceeding 8 V, as shown in Fig. 4.14.

4.3.2 Process-dependent electron and hole lifetimes

The electron and hole carrier lifetimes are also process-dependent parameters and significantly influence the conductivity modulation in the drift region, thereby affecting the on-state and switching performance of the IGBT. Figure 4.15 presents the impact of carrier lifetimes on the $I_c - V_{ce}$ characteristics of the IGBT, comparing simulation results with experimental data from [24] for various gate voltages.

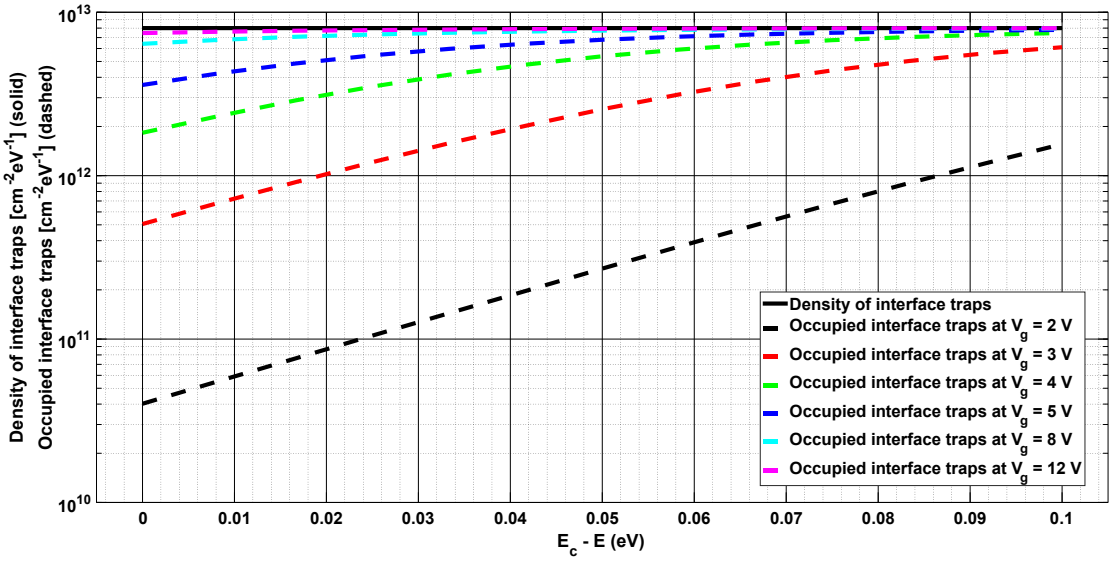


Figure 4.14: Interface trap distribution close to the conduction band (E_c) and number of occupied traps at different gate voltages.

4.3.3 Process-dependent electron and hole mobility

The complex IGBT's fabrication process may lead to reduced carrier mobility compared to simpler structures, as noted in [17, 18, 19] (see Fig. 4.3). Figure 4.16 illustrates that by decreasing the maximum electron and hole mobility parameters ($\mu_{L,e}$ and $\mu_{L,h}$ in Eq. 4.1) by 10%, the simulation results closely align with the experimental data.

4.3.4 Buffer layer doping concentration and thickness

Experimental data from Van Brunt et al. [10] have been utilized to validate the switching behaviour of the modelled device. Given that the devices presented in the works of both Hinojosa et al. [24] and Van Brunt et al. [10] were fabricated by Cree during the same period (2014-2015), it is rational to employ the previously tuned process-dependent parameters as initial inputs for the flowchart in Fig. 4.10.

The injected plasma in the drift region is primarily controlled by the buffer layer's doping concentration and thickness. Although the authors in [10] do not provide

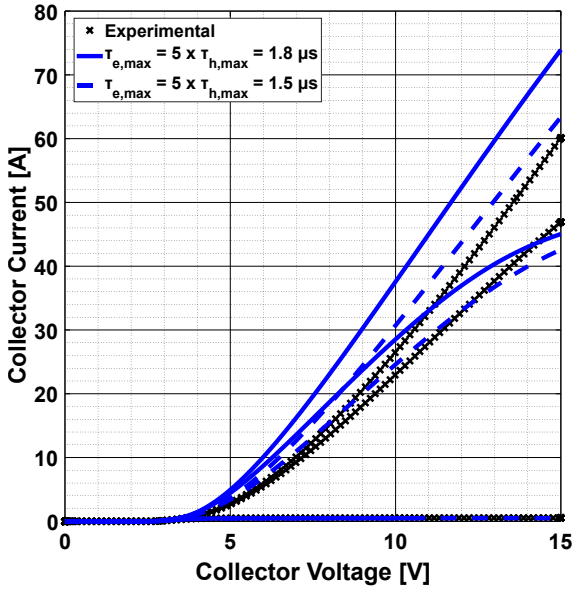


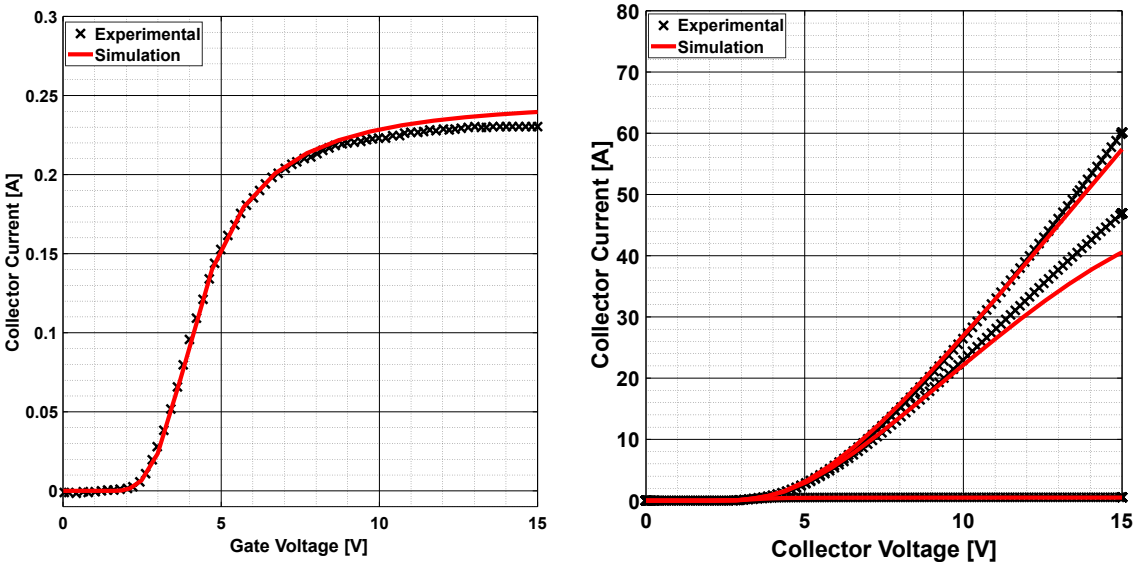
Figure 4.15: Impact of the carrier lifetimes on the $I_c - V_{ce}$ characteristics.

detailed information about these parameters, presumably due to measurement challenges, these parameters can be estimated by fitting the static and dynamic waveforms of the modelled and fabricated devices.

Figure 4.17 displays the impact of the buffer layer doping concentration and thickness on the on-state and turn-off behaviour of the IGBT. The best fit between the simulation and experimental data is achieved using $N_B = 5 \times 10^{17}\text{cm}^{-3}$ and $W_B = 1\mu\text{m}$.

4.3.5 Hole saturation drift velocity

As discussed in subsection 2.4.1, the punch-through voltage of the IGBT during the inductive turn-off process is influenced by factors such as the doping concentration and thickness of the drift region, current density, and the hole saturation drift velocity (see Eq. 2.13). The drift layer doping concentration and thickness of the fabricated 27 kV-rated IGBT in [10] were $1 \times 10^{14}\text{cm}^{-3}$ and $210\mu\text{m}$, respectively. However, the hole saturation drift velocity has not yet been experimentally measured. Figure 4.18(a) shows the inductive turn-off behaviour of an IGBT with



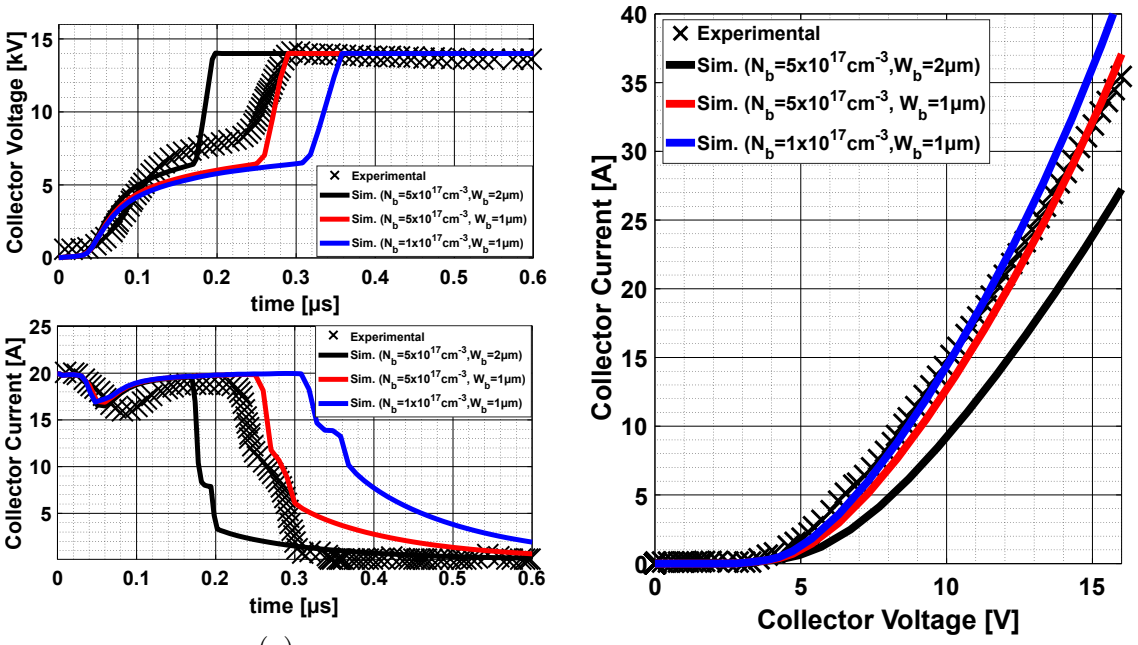
(a) (b)

Figure 4.16: Effect of carrier mobility on the (a) $I_c - V_{ge}$ and (b) $I_c - V_{ce}$ characteristics.

drift layer parameters identical to those in [10], but varying the hole saturation drift velocity. The best match between experimental and simulation results was achieved with a hole saturation velocity, $v_{sat,h} = 6 \times 10^6 \text{cm} \cdot \text{s}^{-1}$, which is lower than that of electrons due to the higher effective mass of holes. As expected, the saturation drift velocity of holes does not influence the on-state characteristics (Fig. 4.18(b)).

4.3.6 Operation at elevated temperatures

The ability of the device modelling to predict the IGBT characteristics at elevated temperatures, specifically up to 425 K, has been validated using experimental data from [10], as illustrated in Fig. 4.19. Furthermore, adding this step to the validation iteration process is necessary to decouple the effects of different parameters on the same operational characteristics. For example, both the buffer layer doping concentration and carrier lifetimes have a strong impact on the injected plasma in the drift region, which affects the on-state and switching characteristics. However, by using data for different temperatures, the impact of those parameters is decoupled



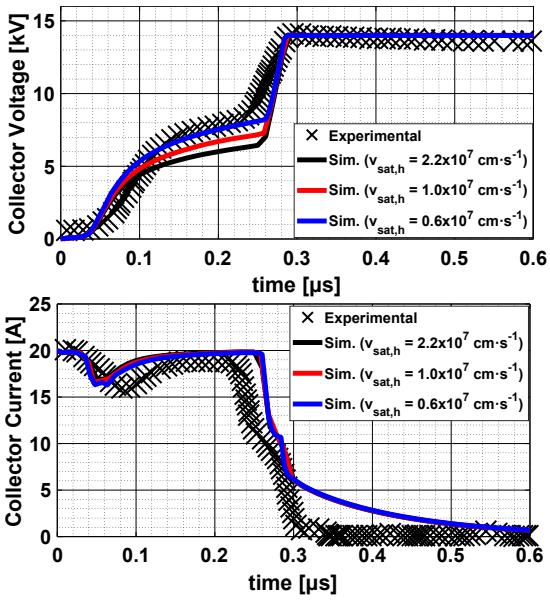
(a) (b)

Figure 4.17: Impact of buffer parameters on the (a) turn-off and (b) on-state behaviour of the IGBT.

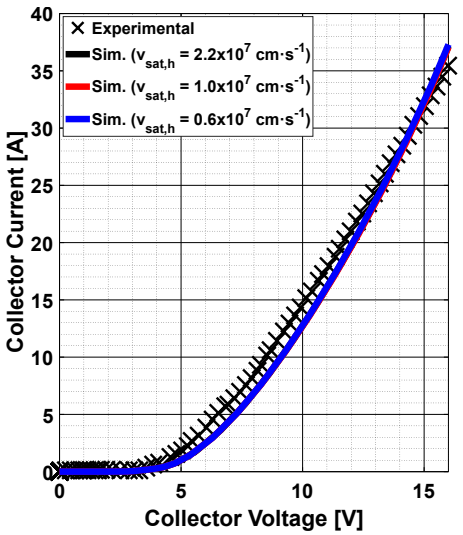
due to their different temperature dependence as presented in Figures 4.15 and 4.5. As a result, this validation process confirms that the model encompasses all major physical phenomena relevant to IGBT's operation and that the model parameters are accurately calibrated.

4.3.7 Breakdown characteristics

This thesis is mainly focused on the active cell design, therefore physical phenomena linked to the edge termination (such as increased leakage current during the blocking state) region have not been studied. As a result, the simulated breakdown voltage of the active cell is expected to be higher and the leakage current lower than the fabricated die, when neglecting the impact of the edge termination. Nonetheless, it is important to check that the breakdown characteristics of the simulated device are within the expected range at the final step of the iteration process of Fig. 4.10. Figure 4.20 compares experimental and simulated breakdown characteristics of a



(a)



(b)

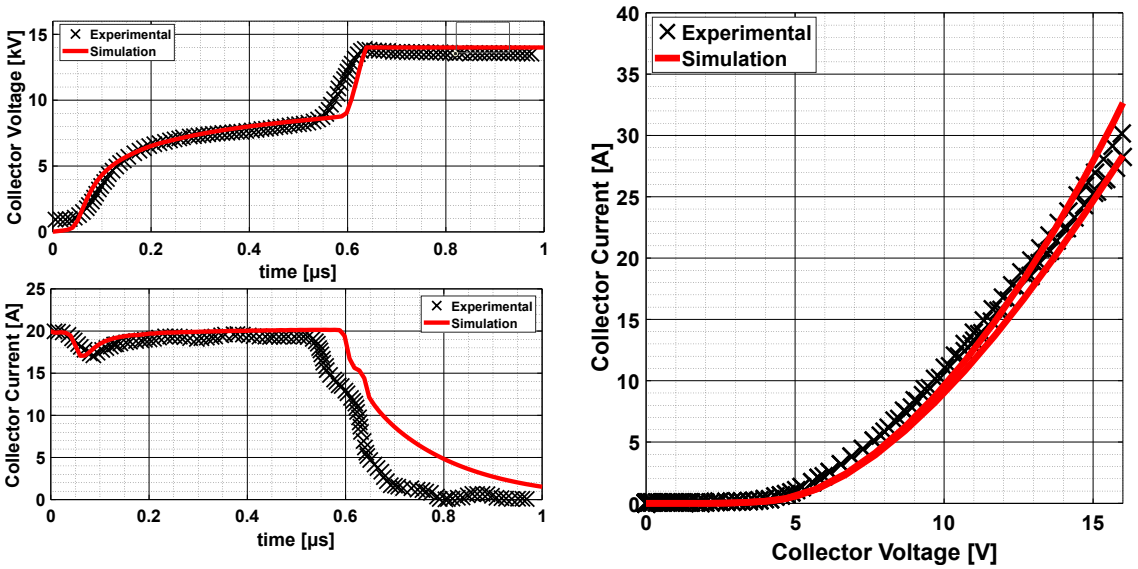
Figure 4.18: Impact of the hole saturation drift velocity on the on-state and turn-off behaviour of the IGBT.

22 kV rated SiC IGBT [23], showing that the modelled device has the expected blocking voltage capability. It is worth noting that the Okuto-Crowell model [132], with previously validated parameters (see Appendix A), has been used to simulate the avalanche characteristics.

Finally, for the rest of this thesis, wherever the current density is displayed in the simulation results, the total current is scaled to the active area.

4.4 Concluding remarks

This chapter presented the validation process followed for the TCAD simulation models based on previously presented experimental results, which is required to ensure good predicting capability. The validation has been performed in two stages. In the first stage, the most critical fundamental material properties were identified, and the simulation models used to describe them were fine-tuned based on published experimental data. In the second stage, an IGBT model was devel-



(a) (b)

Figure 4.19: (a) Turn-off behaviour at 400 K and (b) on-state behaviour at 425 K of the IGBT. Comparison between simulation and experimental data ([10]).

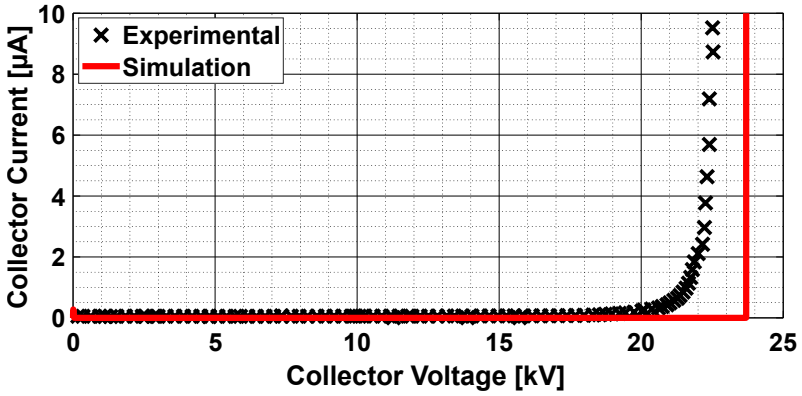


Figure 4.20: Comparison between TCAD modelled and experimental breakdown behaviour of a 22 kV-rated SiC IGBT [23].

oped with characteristics that align well with fabricated devices rated up to 27 kV. An iteration process that decouples the impact of various parameters from different electrical characteristics was followed to estimate the unknown structural and process-dependent parameters from the currently available experimental data.

Chapter 5

Unintentional turn-on phenomenon and structure optimisation to mitigate it

The high dV/dt rates during the switching transients of the SiC IGBT reduce its ruggedness and are the source of several failure mechanisms as was explained in subsection 3.3.1. The false gate triggering of the gate electrode is one of those mechanisms and can lead to increased losses or even permanent device destruction, but it has not been studied in the literature. Section 5.1 aims to describe the mechanisms causing spikes in the gate electrode and can lead to false turn-on. Subsequently, the role of the emitter side design in mitigating the gate voltage spike is presented, and the impact of system parameters such as temperature, gate resistance or current density are also studied in Section 5.2. Finally, Section 5.3 concludes the chapter. It should be noted that the false turn-on phenomenon is usually also referred to in the literature as unintentional turn-on or cross-talk.

For the simulation results presented in this chapter, an asymmetrical planar SiC IGBT has been used, featuring a drift layer with a thickness of 100 μm and doping

concentration of $3 \times 10^{14} cm^{-3}$ to be able to operate at blocking voltages higher than 10 kV. This device has been virtually fabricated using the SPROCESS tool of Sentaurus TCAD and characterised using the chopper circuit topology of Fig. 4.11(b). The accuracy of the most critical material properties modelling has been validated based on experimental data as shown in Chapter 4.

Part of the work presented in this chapter has been published in *I. Almpanis et al., "Influence of Emitter Side Design on the Unintentional Turn-on of 10kV+ SiC n-IGBTs," 2022 IEEE Energy Conversion Congress and Exposition (ECCE).*

5.1 Gate voltage spike due to the capacitive coupling between the gate and the collector electrodes

The SiC IGBT exhibit two different voltage rising phases during the turn-off transient, a slow and a fast, as has been explained in Section 2.4.1. Due to the fast collector voltage rising rate after the punch-through and the capacitive coupling between the collector and the gate, a voltage spike appears in the gate electrode, as shown in Fig. 5.1. This figure also shows the collector voltage and current during the inductive turn-off process of a simulated 10 kV-rated IGBT.

For the case shown in Fig. 5.1, the voltage spike peak reaches about 5 V, which is close to the threshold voltage and thus is not enough to fully turn on the channel and cause electron injection, as verified by Fig. 5.1 from the electron and hole current components of the total emitter current. The mechanisms of this gate voltage spike generation can be understood by looking at Fig. 5.2(a), which shows a bridge leg configuration where the capacitances C_{gc} and C_{ge} represent the equivalent gate parasitic capacitances of the IGBT. The capacitive coupling between the high-side

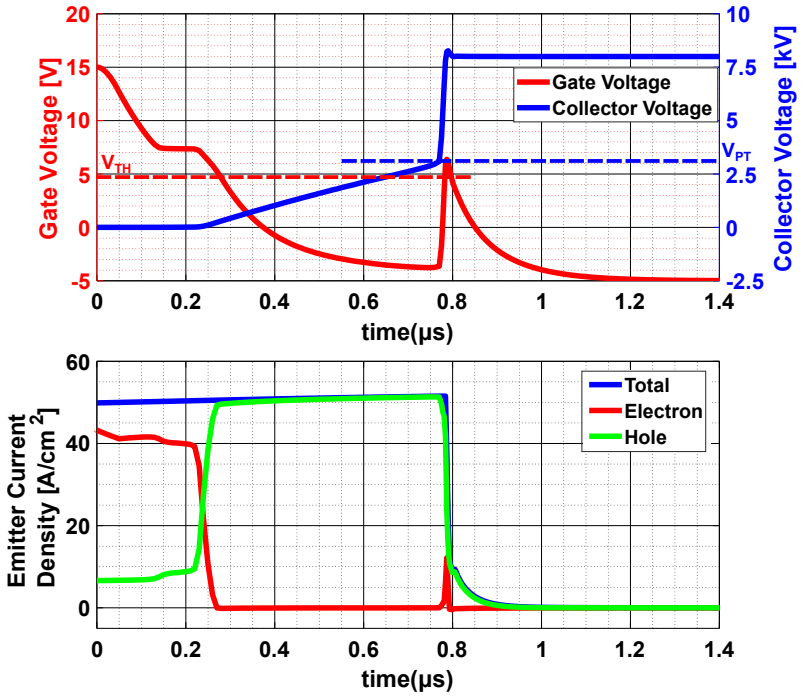


Figure 5.1: Gate and collector voltage (top), total, electron and hole current density at the emitter contact (bottom) during inductive turn-off.

(HS) and low-side (LS) switching components in this bridge-leg configuration can give a positive and a negative voltage spike in the gate of the LS IGBT during the turn-off and turn-on transient of the HS IGBT as shown in Fig. 5.2(b). Although both voltage spikes stress the oxide and cause reliability issues, the positive spike can cause unintentional turn-on, leading to increased switching losses, short-circuiting the V_{cc} or even destruction of the device.

Figure 5.3 shows the simplified equivalent IGBT Resistor-Capacitor (RC) circuit during the switching transient. The differential equation which describes the relationship between the gate and collector voltage is Eq. 5.1, and assuming that the dV_c/dt value during the fast voltage rising phase is constant and is given by Eq. 5.2, a simplified solution of the gate voltage spike amplitude is given by Eq. 5.3. The Δt in these equations is the duration of the fast voltage rising period given by Eq. 2.14. It can be concluded that a higher gate–emitter capacitance (C_{ge}) and a lower gate resistance (R_g) can improve the unintentional turn-on robustness because they reduce the amplitude of the gate voltage spike.

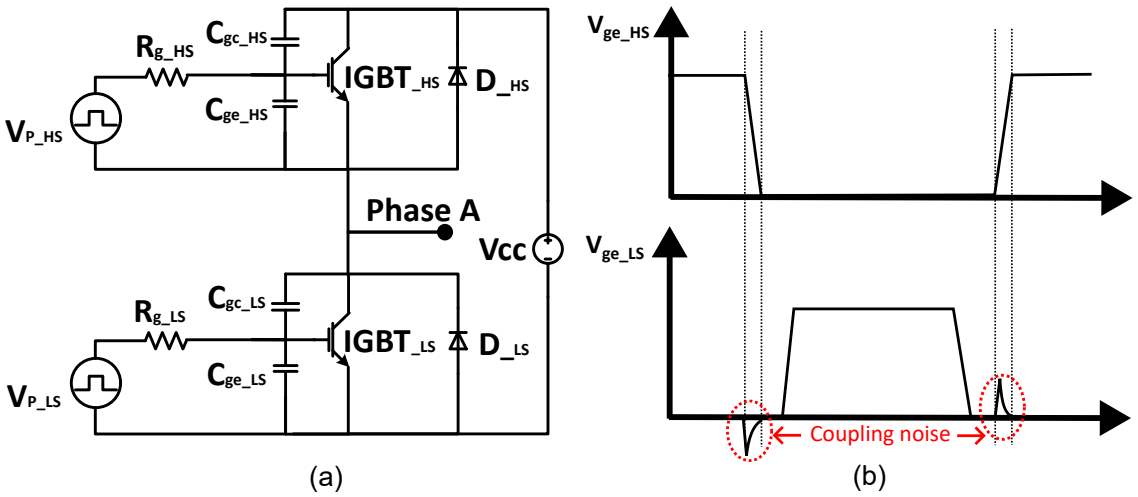


Figure 5.2: (a) Bridge-leg configuration including the parasitic gate capacitances and (b) timing diagram showing the coupling noise induced in the gate of the low-side IGBT during the switching transients of the high-side IGBT.

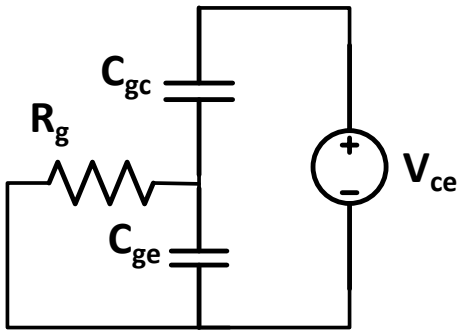


Figure 5.3: Simplified equivalent RC circuit of the IGBT (during switching).

$$\frac{dV_{ge}}{dt} + \frac{1}{(C_{gc,sp} + C_{ge,sp}) \cdot R_g} \cdot V_{ge} = \frac{C_{gc,sp}}{(C_{gc,sp} + C_{ge,sp})} \cdot \frac{dV_{ce}}{dt} \tag{5.1}$$

$$\frac{dV_{ce}}{dt} = \frac{\Delta V_c}{\Delta t} = \frac{V_{cc} - V_{PT}}{\Delta t} \tag{5.2}$$

$$V_{spike} = C_{gc,sp} R_g \frac{V_{cc} - V_{PT}}{\Delta t} \left\{ 1 - e^{-\frac{\Delta t}{(C_{gc,sp} + C_{ge,sp} \cdot R_g)}} \right\} \tag{5.3}$$

When the gate voltage spike is high, the gate voltage might increase above the threshold voltage causing electron current injection through the channel, as seen

in Fig. 5.4(a). However, because the total current is constant, the hole current component reduces, and thus, the hole carrier removal becomes slower, causing a change in the slope of the collector voltage rising. Figure 5.4(b) shows the internal current distribution (total, electron and hole) at the beginning of the turn-off process (t_1), at the slow voltage rising period when the channel is turned off (t_2), and during the unintentional turn-on (t_3). The electron current distribution at t_3 shows the electron current injection from the channel due to the unintentional turn-on.

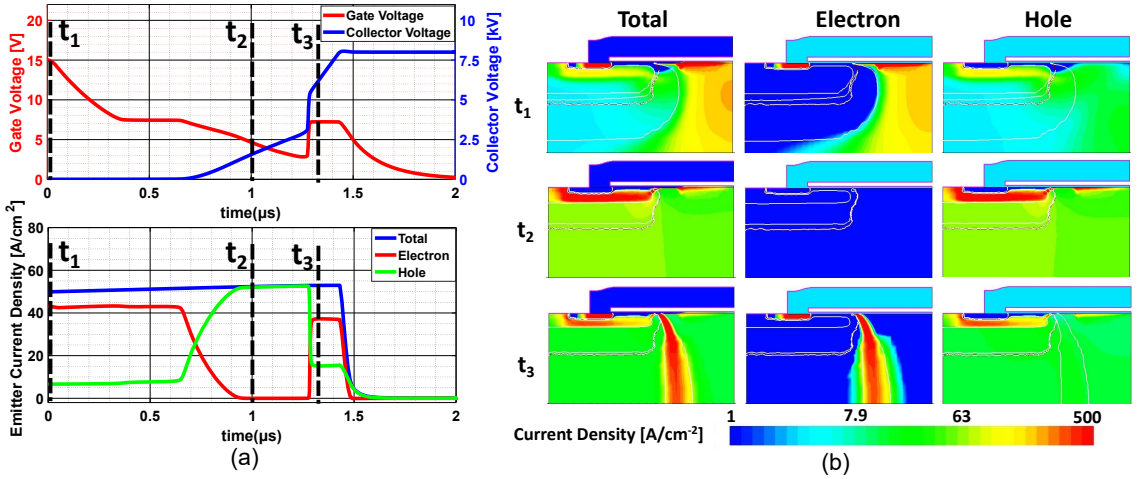


Figure 5.4: (a) Gate and Collector voltage (top). Total, Electron and Hole current density at the emitter contact (bottom) and (b) Total, electron and hole current distribution within the device at the beginning of the turn-off process (t_1), during the slow voltage rising period (t_2) and during the unintentional turn-on (t_3).

5.2 Impact of structural and circuit-related parameters on the unintentional turn-on

The above analysis explained the origins of the high dV/dt and gate voltage spike generation. This section presents how the device structure can be optimised to improve the unintentional turn-on robustness by adjusting the threshold voltage and gate capacitances according to Eq. 5.3. To achieve this, a modified retrograde doping profile is used in the p-well, which in addition to offering the blocking characteristics improvement (see subsection 3.3.4), allows independent control of the

threshold voltage and gate capacitance.

5.2.1 Threshold Voltage and Gate Capacitance co-Adjustment

The modified retrograde p-well design allows for a specific threshold voltage to be achieved at different values of gate oxide thickness (t_{ox}) when concurrently adjusting the p-well surface doping, from $5 \times 10^{16} cm^{-3}$ to $5 \times 10^{17} cm^{-3}$. As shown in Fig. 5.5(a), when keeping the surface doping concentration fixed at about $5 \times 10^{16} cm^{-3}$ and increasing the t_{ox}, the threshold voltage also increases. However, the combination of p-well doping profiles shown in Fig. 5.5(c - d) and t_{ox} values in Fig. 5.5(b) give approximately the same threshold voltage of 5.5 V, chosen to be neither too small to increase the noise immunity of the device nor too high for long-term gate oxide reliability. As a result, this special doping profile of the p-well allows the independent adjustment of the threshold voltage and the gate capacitance.

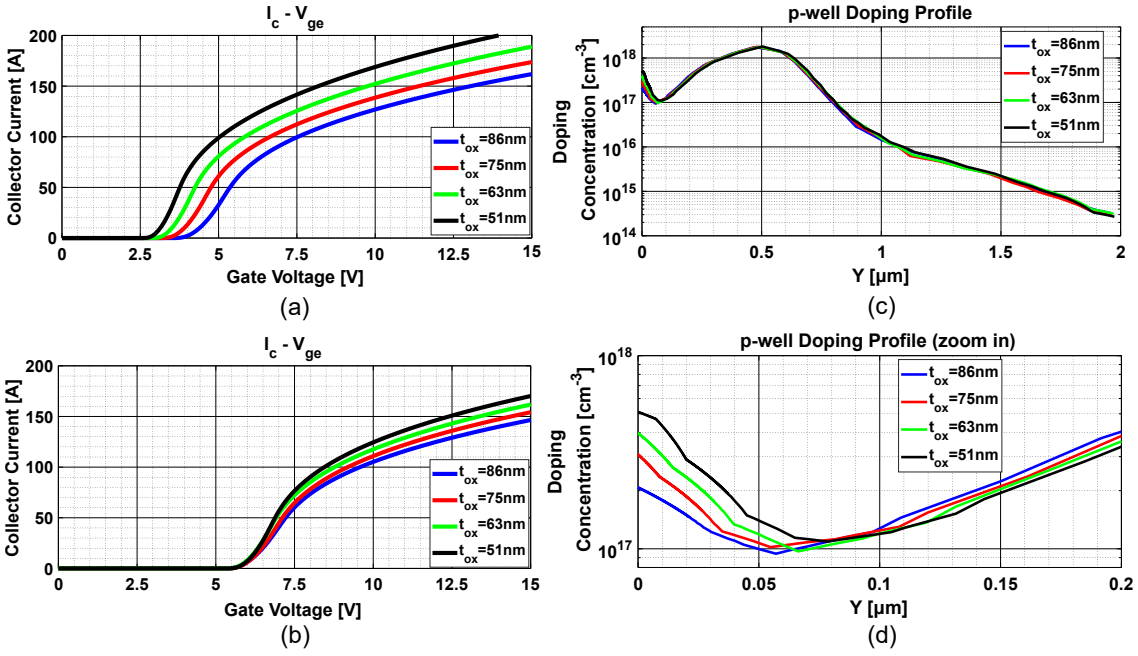


Figure 5.5: (a) $I_c - V_{ge}$ curves for different oxide thickness and same p-well surface doping concentration; (b) $I_c - V_{ge}$ curves for different oxide thickness and different surface doping concentrations to achieve same threshold voltage; (c) doping concentration profile for the cases shown in (b); and (d) doping concentration profile for the cases shown in (b) at the surface of the p-well.

The combinations mentioned above of oxide thickness and doping profile were carried forward for further assessments, where the channel length (W_{ch}), JFET length (W_{JFET}) and intermetal oxide thickness (t_{IE}) were also varied to modify the parasitic gate capacitances. To keep the half-cell pitch constant at 9 μm, the sum of the W_{ch} and $(1/2)W_{JFET}$ was kept constant at 6 μm. Thus $(1/2)W_{JFET}$= 6 - W_{ch}. The dynamic response of the IGBT was assessed at 50 Acm^{-2} (inductive) and testing voltage 8 kV with a gate driving voltage of 15 V for all cases. Additionally, negative gate bias (-5 V) is used for the turn-off to increase the noise immunity of the IGBT without adding significant complexity to the gate driving circuit.

According to Eq. 5.3, the gate-to-emitter capacitance directly influences the gate voltage spike and, as a result, can be optimised to reduce it. The Gate-to-Emitter capacitance is determined by the overlap between the gate contact and the p-well and n_{++} region, and the intermetal capacitance between the gate and emitter electrodes, as shown in Fig. 5.6.

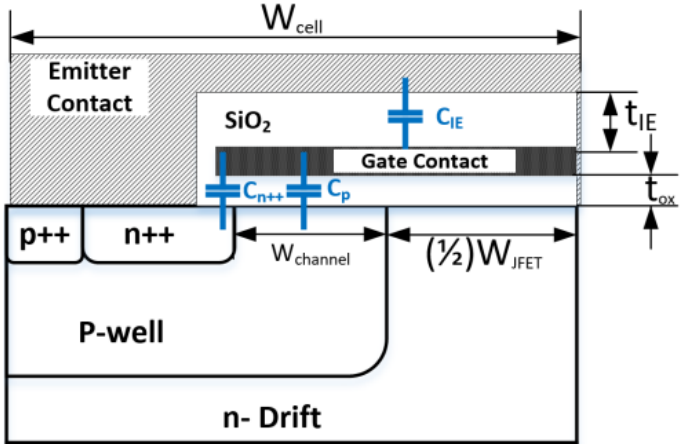


Figure 5.6: Capacitance components of C_{ge} in the IGBT structure.

Equation 5.4 gives the total gate-to-emitter capacitance and can be related to the device's geometry according to Eq. 5.5, where the C_{n++} component is very small and has been neglected.

$$C_{ge,sp} = C_p + C_{n++} + C_{IE} \tag{5.4}$$

$$C_{ge,sp} = \frac{W_{ch}}{W_{cell}} \cdot \frac{\epsilon_{SiO_2}}{t_{ox}} + \frac{W_{ch} + W_{JFET}}{W_{cell}} \cdot \frac{\epsilon_{SiO_2}}{t_{IE}} \tag{5.5}$$

Fig. 5.7(a)-(c) shows the influence of variations in channel length (W_{ch}), gate oxide thickness (t_{ox}) and intermetal oxide thickness (t_{IE}) on the gate voltage spike. The results agree with the abovementioned analysis, meaning that as the gate capacitance increases, the gate voltage spike reduces, and the unintentional turn-on robustness is improved.

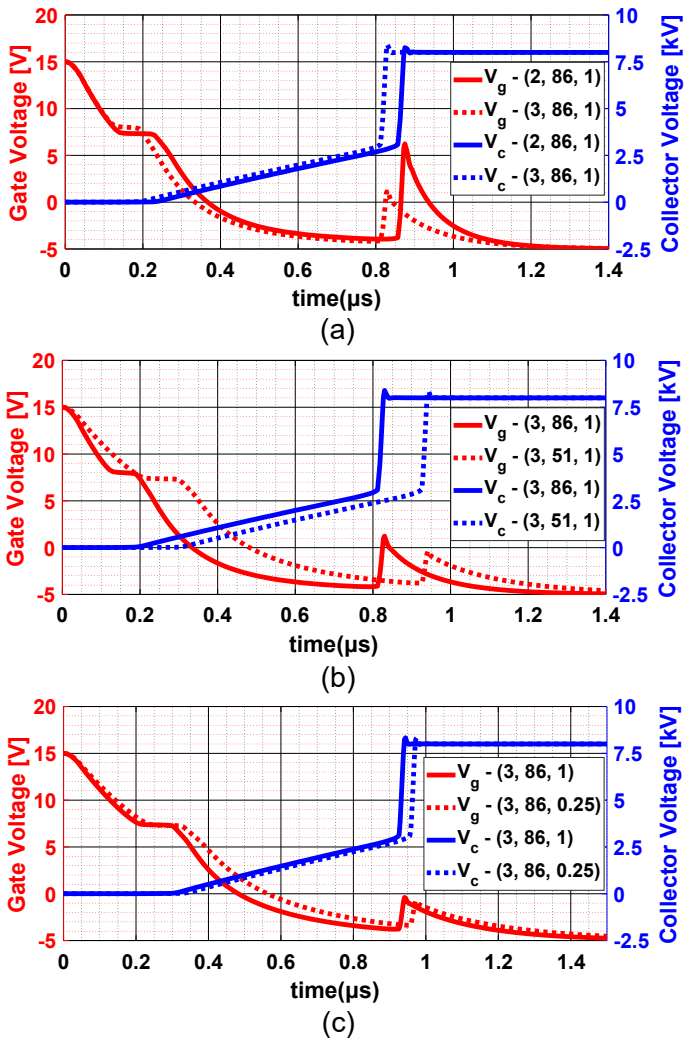


Figure 5.7: $V_c(t)$ and $V_g(t)$ during the turn-off of SiC n-IGBTs having (a) different W_{ch}, (b) different t_{ox}, and (c) different t_{IE}; The values inside the legend parenthesis denote for (W_{ch} [μm], t_{ox}[nm], t_{IE}[μm]).

Table 5.1 summarises the impact of the gate capacitance variation on the on-state

voltage drop, turn-off switching losses, gate voltage spike and dV/dt values for the above cases. It can be seen that the gate voltage spike amplitude was reduced by 78% by only increasing the on-state voltage drop by 15% and without affecting the switching losses. As a result, this gate voltage spike suppression allows for significant unintentional turn-on improvement without sacrificing efficiency.

Table 5.1: Electrical characteristics of IGBTs showing the gate voltage spike amplitude reduction achieved by optimising the emitter side design

$W_{channel}$ $[\mu m]$	t_{ox} $[nm]$	t_{IE} $[nm]$	V_{on} $[V]$	E_{off} $[mJ]$	dV/dt $[kV/\mu s]$	V_{spike} $[V]$
2	86	1	3.95	53	396	10.26
3	86	1	4.88	52	431	5.3
3	51	1	4.74	52	422	3.37
3	51	0.25	4.64	53	414	2.26

It should be noted that the above-mentioned modifications slightly increase the gate charge and therefore the losses in the gate driver. However, these losses can be counterbalanced by reducing the negative gate voltage amplitude during the off-state, which is possible due to the gate voltage spike mitigation.

5.2.2 Gate resistance variation

Figure 5.8 shows the transient waveforms for an IGBT with ($W_{ch}[\mu m]$,$t_{ox}[nm]$, $t_{IE}[\mu m]$) = (2,86,1) when using gate resistors of 2.5 Ω, 7.5 Ω and 30 Ω. It can be seen that the voltage spike increases with the increase of the gate resistance. Especially for the 30 Ω case, the gate voltage (Fig. 5.8(a)) rose above the threshold voltage, leading to unintentional turn-on indicated by the channel current rise (I_{ch} in Fig. 5.8(b)) at the fast-rising phase of the collector voltage.

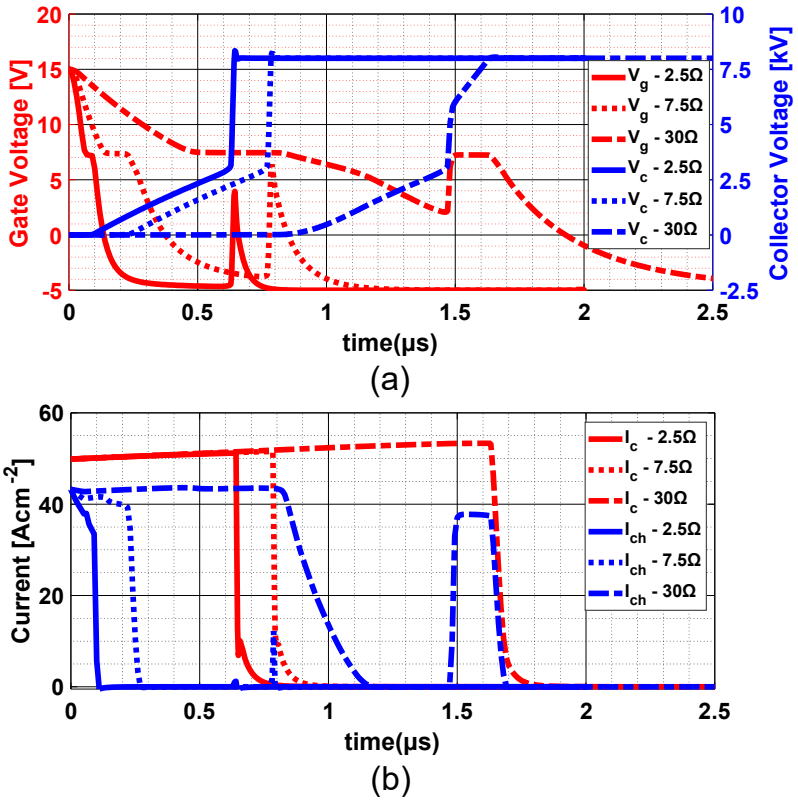


Figure 5.8: (a) $V_c(t)$ and $V_g(t)$; (b) $I_c(t)$ and $I_{ch}(t)$ for different gate resistances.

5.2.3 Impact of Collector Current Density

Figure 5.9 shows the gate and collector voltage during the IGBT turn-off at different collector current densities. As can be seen, the gate voltage spike amplitude reduces as the current density increases because the PT voltage also increases (Eq. 2.13) and thus the ΔV in Eq. 5.2-5.3 is smaller. However, the peak gate voltage remains relatively unaffected due to the faster switching transient at higher current densities. As a result, suppressing the gate voltage spike is necessary independently of the current density.

5.2.4 Impact of Temperature

Finally, the temperature dependence of the gate voltage spike is shown in Fig. 5.10, where the IGBT is turned off at temperatures between 373 K and 500 K. It can be

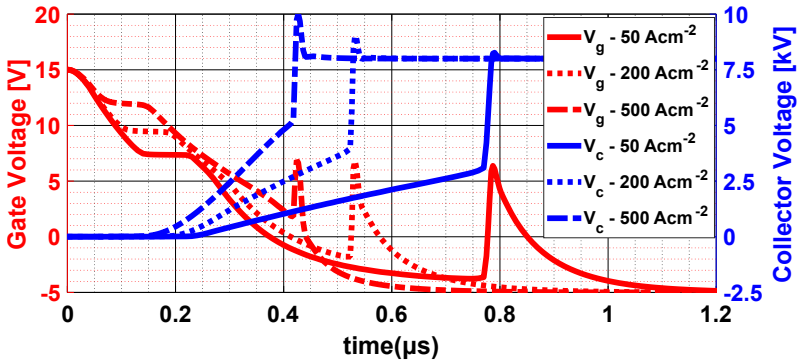


Figure 5.9: Vc(t) and Vg(t) during the IGBT turn-off at different collector current densities.

seen that the gate voltage spike is relatively unaffected by the temperature variation. The slight voltage spike reduction at higher temperatures can be explained by the fact that the plasma injection is enhanced, and thus, more holes need to be removed from the buffer layer during the fast voltage rising period, which means that the dV/dt reduces according to the analysis presented in section 2.4.1.

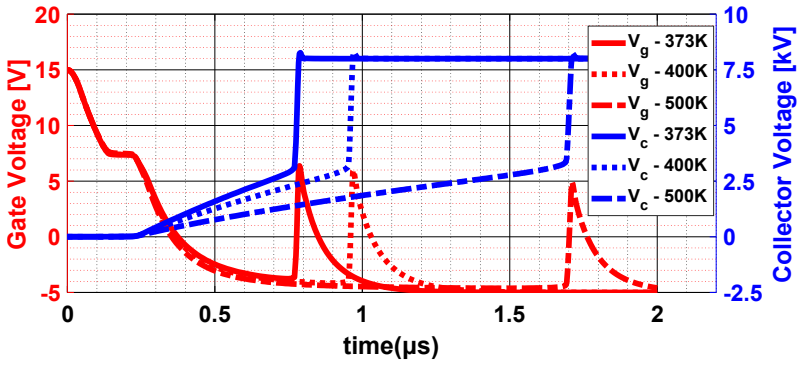


Figure 5.10: $V_c(t)$ and $V_g(t)$ during the IGBT turn-off at different collector current densities.

5.3 Concluding remarks

The influence of emitter side design on the unintentional turn-on of SiC n-IGBTs was investigated using process and mixed–mode TCAD simulations. The phenomenon can increase the losses but can also lead to operation under short circuit conditions which can be catastrophic; it should hence be suppressed. It was shown

that the gate voltage spike responsible for the unintentional turn-on was reduced by adjusting the gate oxide thickness and channel length due to the influence of these design parameters on the gate–emitter capacitance. Further, the doping profile of a modified retrograde p-well can be tweaked to maintain the gate threshold voltage, oxide reliability and overall performance at the desired level. Consequently, the immunity of SiC IGBTs to turn on unintentionally during switching can be improved via an appropriate design of the emitter side.

Chapter 6

Short-Circuit Performance Optimisation

Apart from nominal operating conditions, power semiconductor devices can also operate under short-circuit conditions, where they conduct extremely high currents for a short duration (in the μs range). For reliable operation, the IGBT must withstand these conditions long enough for the control circuit to detect the short circuit and safely deactivate the device. The literature review in subsection 3.3.2 suggests that SiC IGBTs exhibit less robust short-circuit capabilities compared to Silicon IGBTs, potentially hindering their widespread use in power converters. Notably, a detailed examination of SiC IGBTs' short-circuit behaviour is absent from existing literature.

This chapter aims first to conduct such an analysis and then elucidate the failure modes under short-circuit conditions (Section 6.2-6.3). Following this, Section 6.4 will explore how different device and circuit parameters influence the short-circuit behaviour of SiC IGBTs, aiming to pinpoint the most critical of them. Finally, Section 6.5 concludes the chapter.

Part of the work presented in this chapter has been published in *I. Almpanis et al., "Short-Circuit Performance Investigation of 10kV+ Rated SiC n-IGBT," 2022 IEEE Workshop on Wide Bandgap Power Devices and Applications in Europe (WiPDA Europe).*

6.1 TCAD models accuracy beyond the experimentally validated region

Accurately simulating short-circuit conditions is challenging due to the extremely high temperatures generated within the device. Reports indicate that temperatures inside a SiC MOSFET during short-circuit operation can exceed 1500 K [133]. However, validating models at such high temperatures is difficult due to the lack of corresponding data in the literature. Consequently, the most critical material parameter models, presented in Section 4.2, have been extrapolated for temperatures beyond the experimentally verified range (up to 600 K).

Figure 6.1 illustrates the extrapolated values for electron mobilities, acceptor ionisation rates, and minority lifetime for the material models used in TCAD simulations. These parameters adhere to expected trajectories based on current semiconductor knowledge and thus provide reasonable confidence in the accuracy of extrapolating material parameters beyond the validated range.

For this chapter's simulation results, an asymmetrical planar SiC IGBT was used, featuring a 100 μm thick drift layer with a doping concentration of $3 \times 10^{14} cm^{-3}$, enabling operation at blocking voltages above 10 kV. This device was virtually fabricated using the SPROCESS tool of Sentaurus TCAD. Unlike the simulations in Chapter 5, this chapter employs non-isothermal modelling to account for the rapid temperature increases during short-circuit conditions.

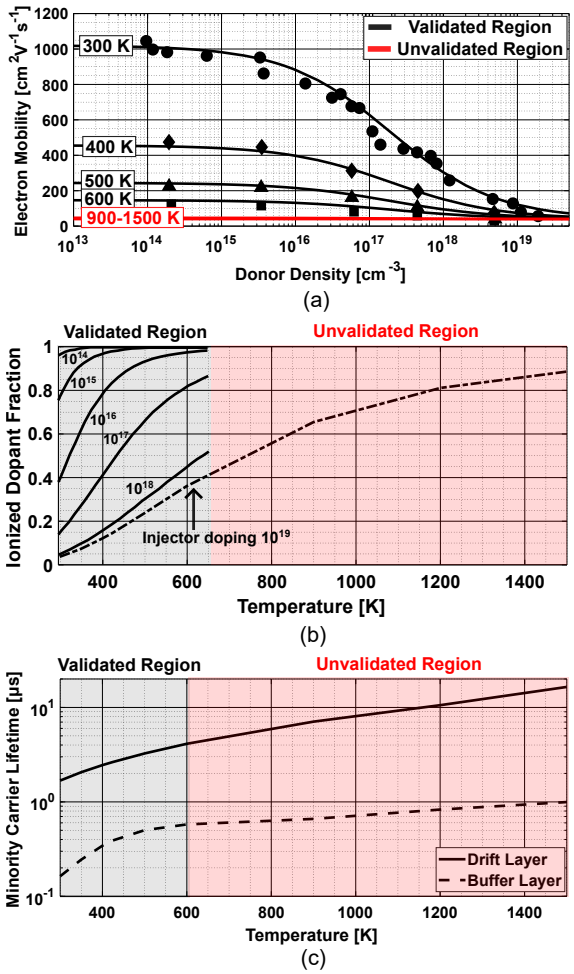


Figure 6.1: Extrapolated modelled values for the (a) electron mobilities, (b) acceptor ionisation rates and (c) minority carrier lifetimes beyond the validated region presented in Section 4.2.

6.2 IGBT operation under short circuit conditions and temperature dependence of characteristics

The IGBT equivalent circuit shown in Fig. 6.2 is used to study the internal current distribution and to understand the device's behaviour under short circuit conditions. As explained in Section 2.3, the IGBT's behaviour can be modelled by a MOSFET, which supplies the base driving current for the internal PNP transistor. Additionally, the IGBT structure has an internal NPN transistor, which does not

contribute to the conductivity during nominal operational conditions due to its low base voltage.

Consequently, the electron current (I_n) flowing through the channel serves as the base current for the wide-base PNP transistor. This induces a hole current (I_p) that flows through the p-well region, as described by Eq. 6.1. Here, β_{PNP} represents the common emitter current gain, and α_{PNP} denotes the common base current gain of the parasitic PNP transistor. The total current at the collector and emitter is the sum of the electron and hole current components, as defined in Eq. 6.2. The maximum collector current is set by the MOS channel saturation current, detailed in Eq. 6.3, leading to the overall collector saturation current as stated in Eq. 6.4.

In these equations, C_{ox} refers to the gate oxide capacitance, V_{th} is the gate threshold voltage, μ_n indicates the channel mobility, W_{CH} is the channel length, and Z represents the width of the device orthogonal to its cross-section.

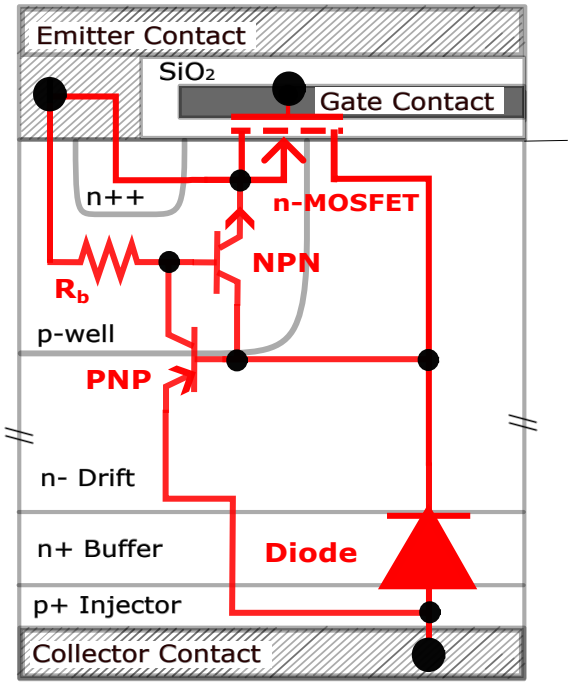


Figure 6.2: Equivalent circuit illustrating the parasitic components within the IGBT device structure.

$$I_p = \beta_{PNP} \cdot I_n = \frac{\alpha_{PNP}}{1 - \alpha_{PNP}} \cdot I_n \tag{6.1}$$

$$I_E = I_C = I_n + I_p = \frac{I_n}{1 - \alpha_{PNP}} \tag{6.2}$$

$$I_n = \frac{\mu_n C_{ox} Z}{2W_{CH}} (V_{GE} - V_{th})^2 \tag{6.3}$$

$$I_C = \frac{\mu_n C_{ox} Z}{2W_{CH}(1 - \alpha_{PNP})} (V_{GE} - V_{th})^2 \tag{6.4}$$

The hole current passing through the p-well in the IGBT structure causes a voltage drop across the parasitic resistance R_b. This resistance can be estimated using Eq. 6.5, where N_{p-well} denotes the peak doping concentration of the p-well, D_p represents the diffusion coefficient of holes, W_{n++} is the length of the n_{++} emitter region, and μ_p is the hole mobility. In Eq. 6.6, the symbol k represents the Boltzmann constant, T denotes the temperature, N_{n++} is the doping concentration in the n_{++} region, and n_i is the intrinsic carrier concentration.

During short-circuit conditions, high current densities may lead to a significant increase in this voltage drop across the R_b, potentially exceeding the built-in potential (as described in Eq. 6.6) of the base-to-emitter junction of the parasitic NPN transistor. If this occurs, the parasitic NPN transistor becomes active, leading to a latch-up of the parasitic thyristor structure formed by the PNP and NPN transistors. Consequently, control over the gate electrode is lost, resulting in an uncontrolled increase in current and a rapid temperature increase within the IGBT structure. Therefore, it is crucial to examine the behaviour of critical areas within the IGBT structure under such extreme temperatures to understand its operation

during short-circuit conditions fully.

$$R_b = \frac{W_{n++}}{q\mu_p N_{p-well} D_p Z} \tag{6.5}$$

$$\varphi_{bi} = \frac{kT}{q} ln\left(\frac{N_{p-well} N_{n++}}{n_i^2}\right) \tag{6.6}$$

Figure 6.3 illustrates the temperature dependence of the current-voltage characteristics of a PiN diode over a range from 300 K to 1200 K. It is observed that as the temperature increases, the intrinsic carrier concentration (n_i) also increases, leading to a reduction in the built-in potential of the diode (φ_{bi}) as described by Equation 6.6.

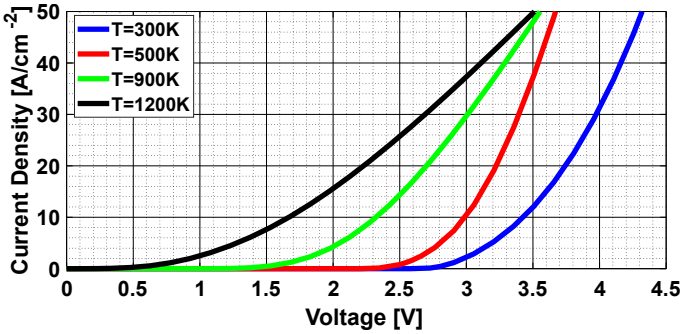


Figure 6.3: Temperature dependence of the built-in potential in a PiN diode.

Additionally, the threshold voltage of the MOS structure is a complex function of the doping concentration, contact-semiconductor work function, fixed oxide charge, and interface traps. These parameters are temperature-dependent and alter the gate threshold voltage at elevated temperatures. Consequently, the threshold voltage is strongly temperature-dependent and reduces at higher temperatures, as shown in Fig. 6.4. Finally, the current gain of the IGBT increases with temperature due to higher dopant activation and increased minority carrier lifetimes at elevated temperatures.

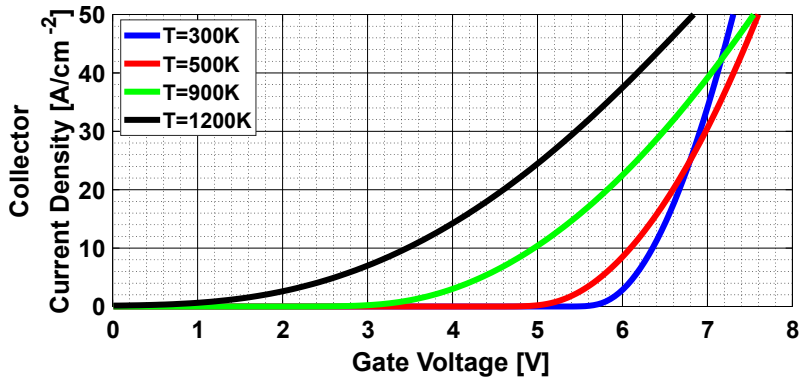


Figure 6.4: Temperature dependence of the gate threshold voltage on a SiC IGBT.

6.3 Failure mechanisms under short circuit conditions

The general characteristics of short circuits are analysed using the circuit shown in Fig. 6.5, with parasitic inductances representing typical application conditions. The DC bus voltage (V_{cc}) is set to 5 kV, approximately 40% of the device's breakdown voltage. The amplitude of the gate voltage pulse (V_p) is 15 V, and the gate resistance (R_g) is set at 7.5 Ω. The stray inductance (L_s) and the parasitic emitter inductance (L_e) are 100 nH and 10 nH, respectively. The thermal boundary conditions were established by employing a thermal electrode on the collector side with an initial temperature of 373 K (100 °C) and a surface thermal resistance of 0.034 $\mathrm{K \cdot cm^2/W}$, comparable to parameters used in studies for SiC MOSFETs [133, 134]. These parameters set the starting structure but are varied in the parameter sensitivity analysis conducted in subsection 6.4.

While the primary cause of IGBT destruction in a short-circuit event is high power dissipation leading to an increase in device temperature, the specific processes leading to failure may vary depending on the structural characteristics and operational conditions, as described below.

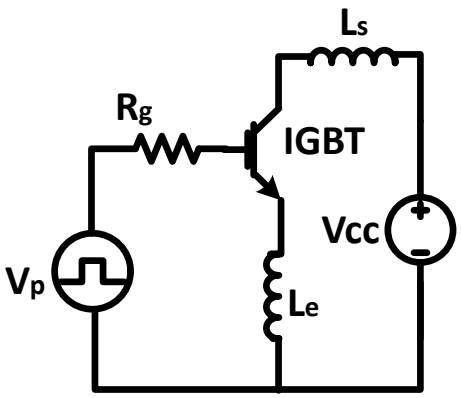


Figure 6.5: Circuit topology used for studying the short-circuit behaviour of the IGBT.

6.3.1 Parasitic thyristor latching during on-state

Figure 6.6 displays the emitter current, gate and collector voltages, and the maximum temperature within the device. Analysing the equivalent circuit representation of the IGBT, depicted in Fig. 6.2, along with the internal temperature, electron, hole, and total current density inside the device at various stages of the short-circuit event (as shown in Fig. 6.7), facilitates understanding of the failure mechanisms.

The short-circuit current waveform can be divided into three distinct phases:

Phase I (3-6 μs): Initially, during the short-circuit event, the current rapidly increases due to the small inductance, driving the device into the saturation region. The current continues to rise, predominantly due to enhanced ionisation rates of dopants and increased carrier lifetimes at elevated temperatures, as elaborated in Fig. 6.1(b-c). This results in stronger conductivity modulation of the drift region at elevated temperatures.

Phase II (6-23 μs): Operating under high voltage and current conditions, the device's temperature surpasses 600 K. Here, the current waveform starts to decline, influenced predominantly by strong Coulomb scattering that reduces the carrier mobilities, as demonstrated in Fig. 6.1(a).

Phase III (23 μs to failure): In this final phase, the device's maximum temperature exceeds 1300 K. Thermal phenomena within the device initiate a positive feedback loop of current increase, ultimately leading to failure. Specific mechanisms include:

- The reduction of the MOSFET's gate threshold voltage (Fig. 6.4) results in enhanced electron injection into the drift region, serving as the base current of the PNP transistor.
- The decrease in the built-in potential of all PN junctions with rising temperature (Fig. 6.3) causes:
  - The NPN transistor to activate at a lower base voltage.
  - Increased hole injection from the PiN diode, acting as the base current for the NPN transistor.
  - An increase in the current gain of the PNP transistor, thus injecting more holes, which serve as the base current for the NPN transistor.
- The carrier generation increases with temperature, contributing to the device's conduction. As cited in [135] a temperature above 1400 °C is necessary to generate an intrinsic carrier concentration of around 3.5×10^{15} cm^{-3}, increasing the conductivity of SiC and eventually leading to thermal runaway.

6.3.2 Parasitic thyristor latching during blocking state

Apart from the previously described failure mechanism, the IGBT can also fail several microseconds after turn-off. This behaviour is not unique to SiC IGBTs; it has been observed in silicon IGBTs [136] and SiC MOSFETs [137] as well. Figure 6.8(a) illustrates an IGBT which turns off $3\mu s$ before its destruction at $t = 30\mu s$. Despite decreasing collector current once the gate voltage falls below the threshold,

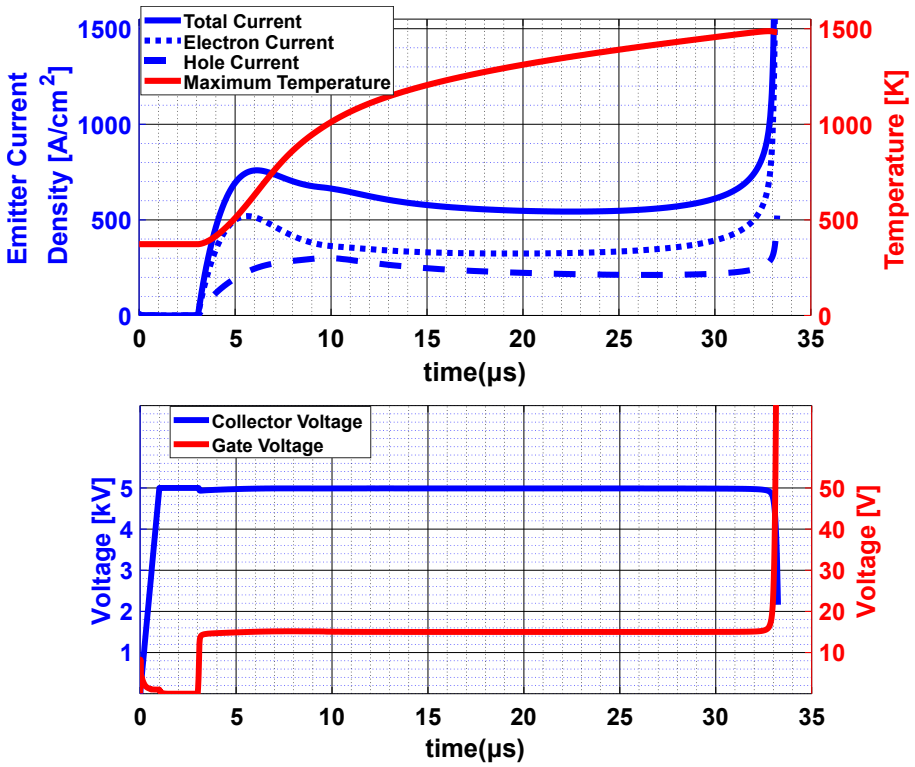


Figure 6.6: Short circuit current and maximum device temperature (top); collector and gate voltage (bottom) during the short circuit failure.

the device's high temperature leads to a significant leakage current ($18A/cm^2$). This high leakage current is attributed to increased carrier generation and a reduction in threshold voltage at higher temperatures, as previously discussed.

Additionally, in the current conduction mode, the maximum temperature location is typically near the gate oxide in the JFET region (see Fig. 6.7), mainly due to the higher proportion of electron current passing through the channel (Fig. 6.6). In contrast, during the blocking state, the heat begins to spread towards the thyristor part of the IGBT, as depicted in Fig. 6.8(b). Consequently, more carriers are generated in the p-well region, decreasing the built-in potential of the NPN transistor's base-to-emitter junction. This leads to the activation of the NPN transistor, causing an uncontrollable rise in current. The parasitic thyristor then latches, resulting in the device's failure.

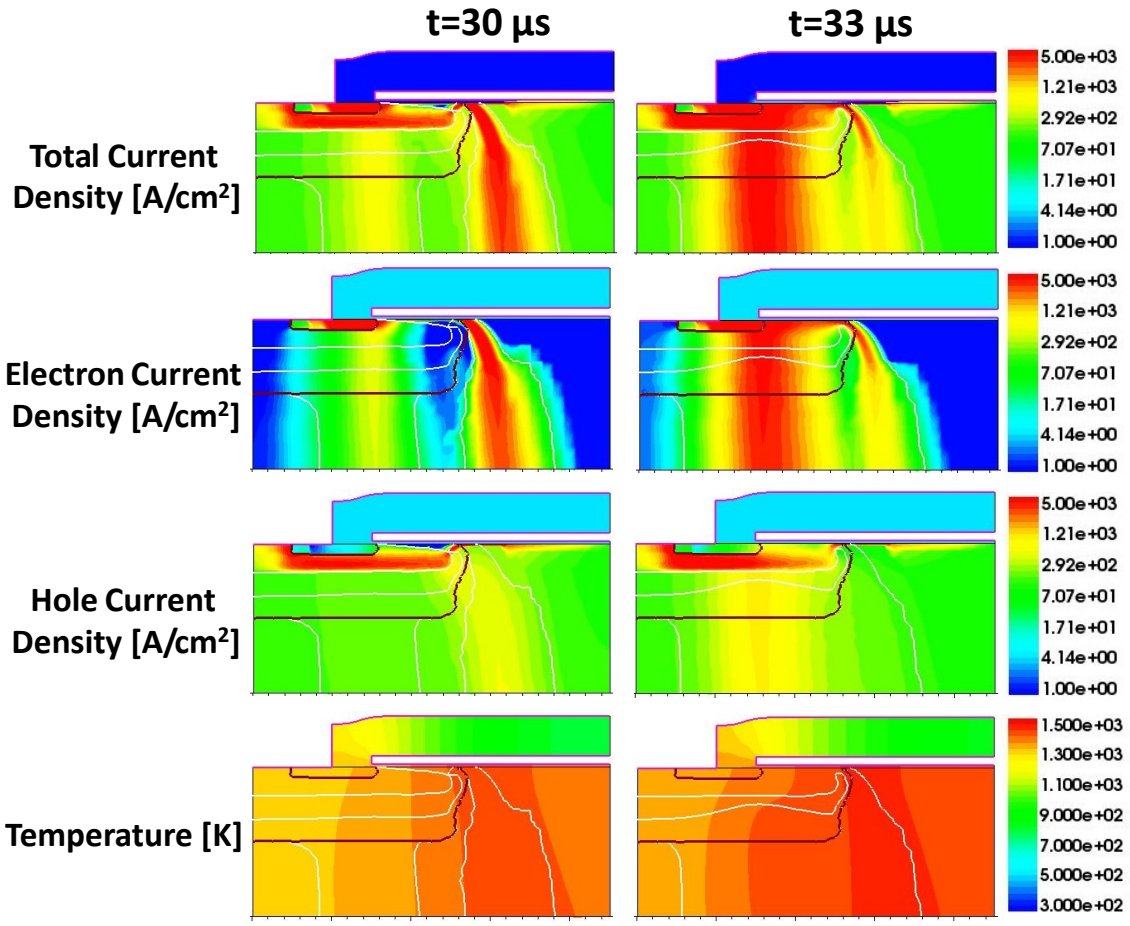


Figure 6.7: Internal device current densities and temperature distribution before and after short-circuit failure.

6.3.3 Device failure due to the emitter contact melting or gate oxide cracking

Finally, the IGBT is susceptible to failure due to mechanical damage in its emitter contact or gate oxide. This type of damage can occur by melting the emitter contact under high temperatures or cracking the gate oxide. The latter often results from the different Thermal expansion coefficient (CTE) between SiC and SiO_2. While these failure mechanisms are well-documented in SiC MOSFETs, similar comprehensive studies on SiC IGBTs remain lacking.

Figure 6.9 extends the illustration of the short circuit phenomenon from Fig. 6.6 by including the temperature at the emitter contact. Aluminium, commonly used

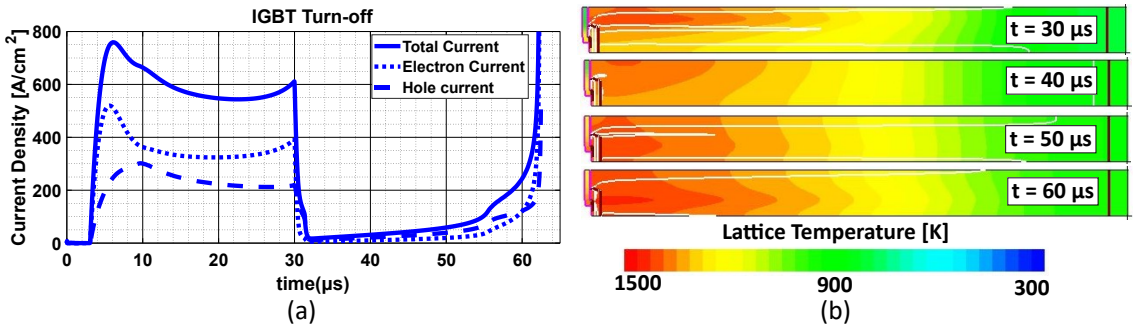


Figure 6.8: (a) Emitter electron, hole and total current density before and after turn-off at 30 μs; (b) Lattice temperature at various instants after IGBT turn-off.

in power electronics for metallisation, has a melting temperature of approximately 933 K. Consequently, when aluminium is used for emitter contact metallisation, its destruction due to melting may become the primary failure mode, preceding the onset of parasitic thyristor latch-up. Moreover, since the failure occurs rapidly (in less than 10 μs, a duration often referred to as Short Circuit Withstand Time (SCWT)), this scenario typically precludes gate oxide cracking as a failure mechanism.

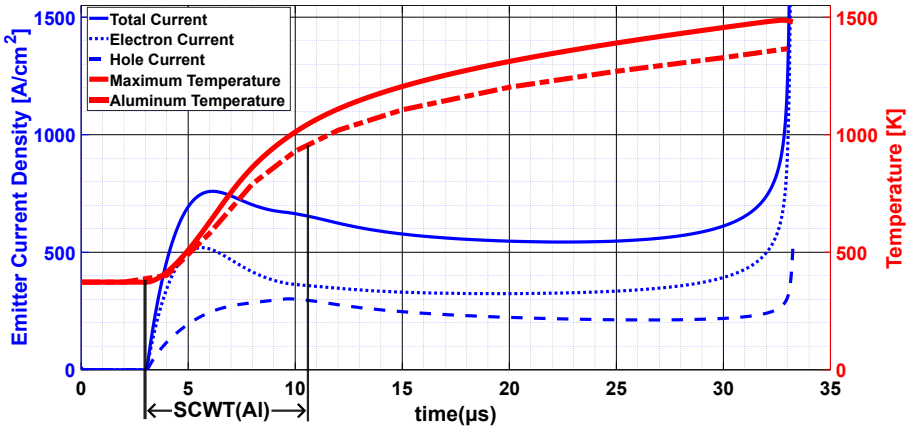


Figure 6.9: Short circuit current, maximum device temperature and temperature of the emitter contact

However, in cases where different metallisation materials with higher melting points are used, such as silver (1235 K) or gold (1337 K), or in operational conditions that result in longer SCWT (due to factors like DC bus or gate voltage variations), gate oxide cracking might become the prevalent failure mechanism.

6.4 Device and circuit level parameters sensitivity analysis

The previously presented analysis and equations 6.1-6.6 highlighted that many circuit and device-related parameters impact the short-circuit robustness of the IGBT. The impact of each of them is presented and discussed below:

6.4.1 DC bus voltage

Figure 6.10 shows the impact of the DC bus voltage variation. The duration until the parasitic thyristor latching varies from $5\mu s$ at 8 kV to almost $100\mu s$ at 2 kV. The apparent reason is that the power dissipation is higher for higher DC bus voltage, leading to a faster increase in the lattice temperature. Additionally, the maximum temperature at the time of failure decreases as the DC bus voltage increases. This phenomenon can be explained by considering the behaviour of the internal PNP transistor within the IGBT structure. As the collector voltage rises, the depletion width of the drift region increases, leading to an enhanced current gain in the PNP transistor. This results in a higher hole current density through the p-well, allowing the parasitic thyristor to latch at a lower temperature.

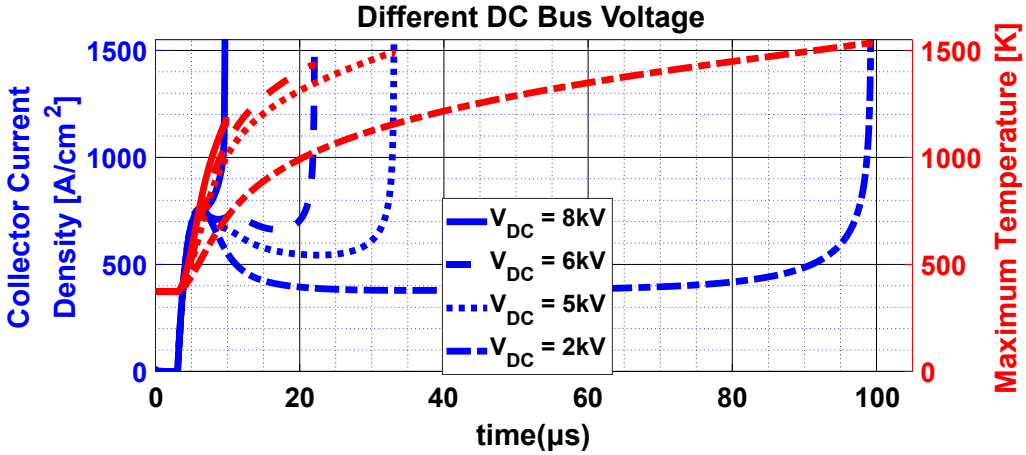


Figure 6.10: IGBT short-circuit behaviour with different DC bus voltages.

6.4.2 Gate Voltage

The gate voltage strongly affects the short-circuit ruggedness of the IGBT as it controls the electron current density through the channel. Therefore, by reducing the gate voltage of an IGBT, the magnitude of the fault current is reduced, and the SCWT is extended, as shown in Fig. 6.11.

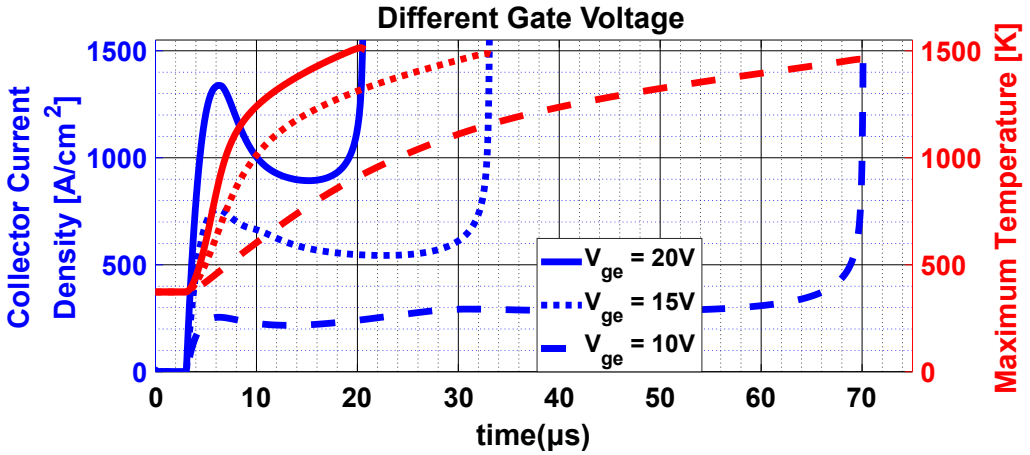


Figure 6.11: IGBT short-circuit behaviour with different gate voltages.

6.4.3 Gate resistance, stray inductance and lattice temperature

Figure 6.12 shows the impact of the gate resistance, stray inductance, and lattice temperature on the short-circuit behaviour. The two first parameters slightly affect the transient behaviour at the beginning of the short circuit phenomenon and do not contribute significantly to the temperature rise of the IGBT. Additionally, the short circuit energy is independent of the initial lattice temperature before the short-circuit, as shown in Fig. 6.12(c), where an initial temperature increase from 373 K to 900 K does not significantly influence the short circuit behaviour. Finally, the heat transfer properties of the backside packaging have minor effects on the SCWT due to the fast evolution of the short-circuit event.

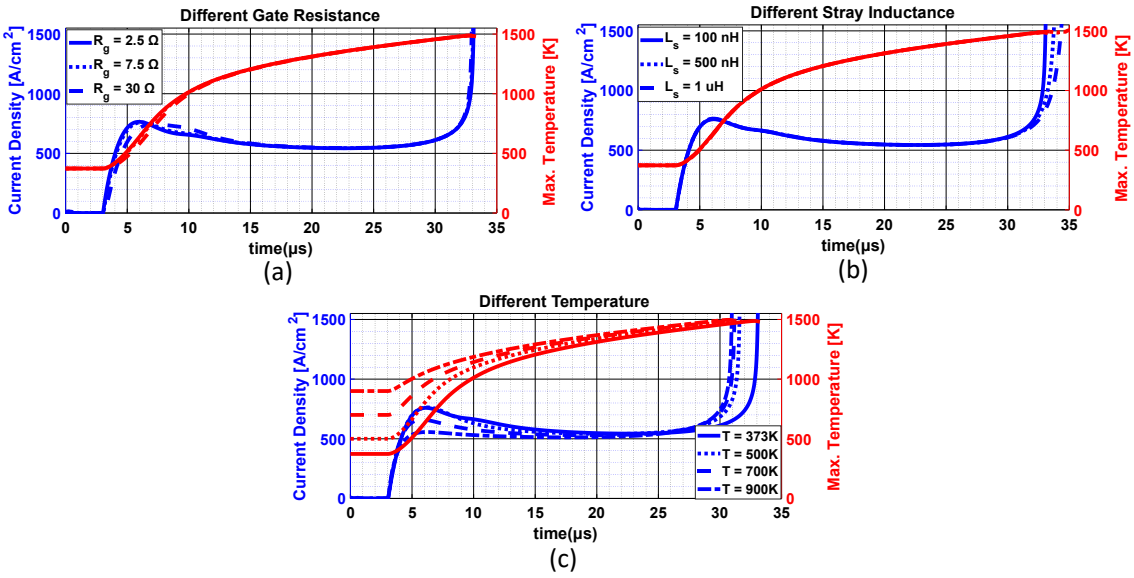


Figure 6.12: The influence of the gate resistance, stray inductance and lattice temperature on the short circuit robustness of the IGBT.

6.4.4 Channel and JFET width

Figure 6.13 shows the impact of the channel and JFET width on the short circuit behaviour. To keep the cell pitch constant for all the scenarios, the sum of the JFET and the channel width is kept at $6\mu m$. A shorter channel width increases the channel saturation current, and a longer JFET width reduces the JFET region resistance. As a result, IGBTs with small channel widths are less robust during short-circuit events.

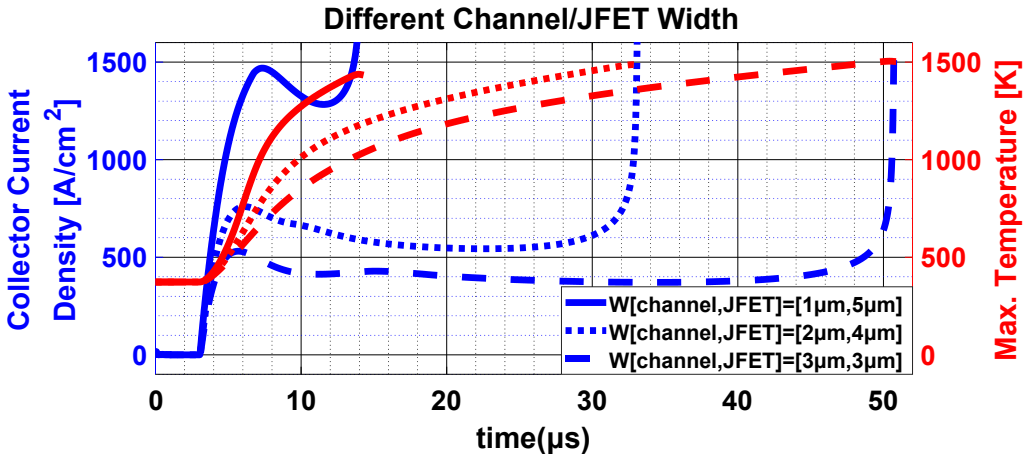


Figure 6.13: IGBT short-circuit behaviour with different channel and JFET width.

6.4.5 Buffer layer doping concentration

The Buffer layer doping controls the plasma injection into the drift region and the current gain of the PNP transistor. Therefore, the buffer layer doping density can also control the short circuit robustness. As a result, achieving IGBTs featuring low $V_{ce,on}$ comes with the cost of lower SCWT, as shown in Fig. 6.14.

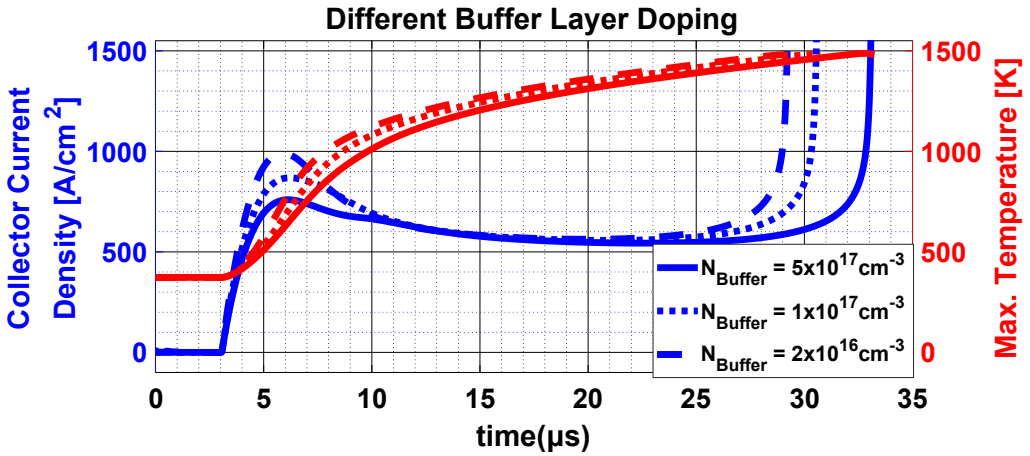


Figure 6.14: IGBT short-circuit behaviour with different buffer layer doping density.

6.4.6 P-well bottom doping concentration

The highly doped region of the p-well improves the latch-up immunity of the IGBT by reducing the equivalent base resistance (R_b in Fig. 6.2). Consequently, the voltage drop across this resistance is lower for higher peak doping concentration of the p-well, resulting in the thyristor latching up at a higher temperature, as shown in Fig. 6.15.

6.4.7 N++ emitter region width

Variation in the width of the n_{++} emitter region has the same result as the peak doping concentration of the p-well in the equivalent base resistance R_b. Therefore, the equivalent p-well resistance is also reduced by reducing the n_{++} emitter width

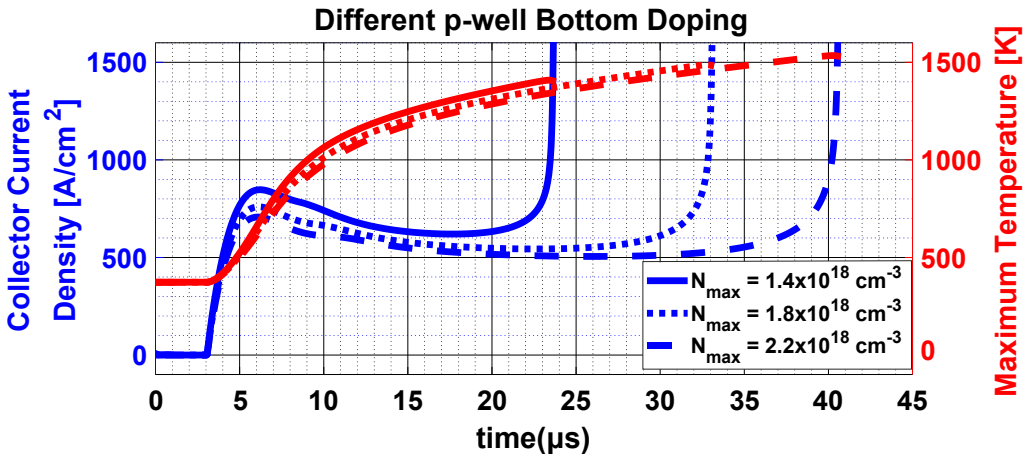


Figure 6.15: IGBT's short-circuit behaviour with different peak doping concentration on the p-well N_{max}.

and the SCWT increases (Fig. 6.16).

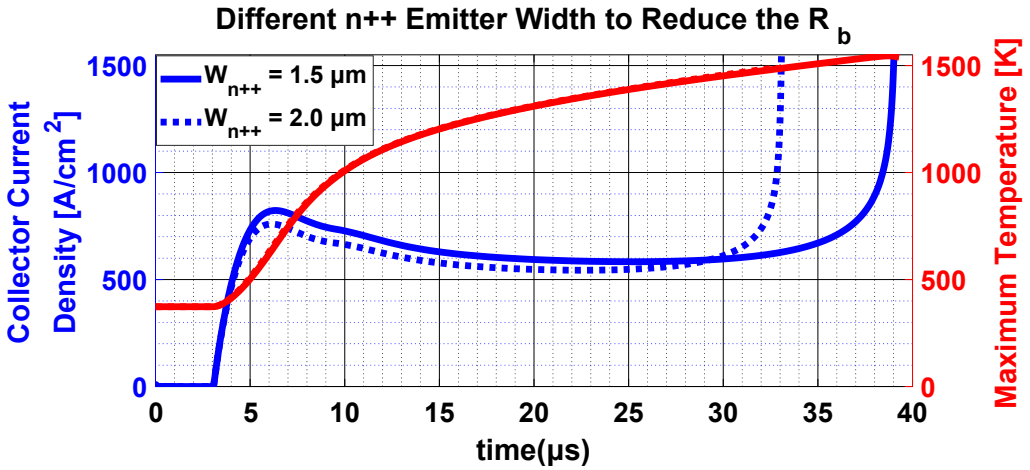


Figure 6.16: IGBT short-circuit behaviour with different n++ emitter region width.

6.4.8 Different turn-off time

Moreover, it is worth pointing out the necessity of detecting and clearing the short circuit event as fast as possible to avoid high temperature and high leakage current generation during the blocking state. As shown in Fig. 6.17, even if the IGBT is turned off $6\mu s$ before its parasitic thyristor latch-up, the positive feedback mechanism of leakage current increase eventually leads to failure after hundreds of microseconds.

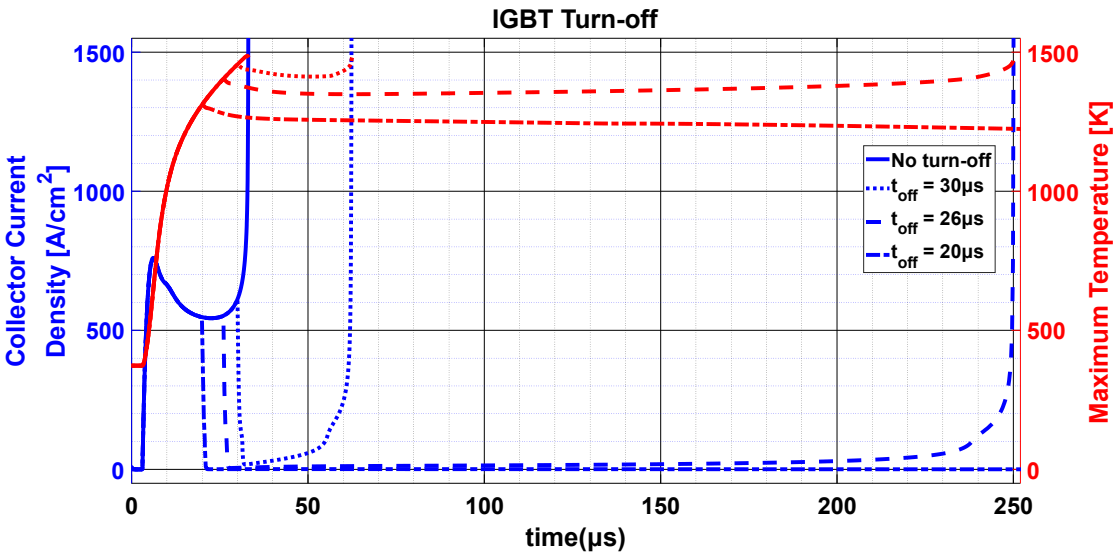


Figure 6.17: IGBT short-circuit behaviour after turn-off at different times.

6.5 Concluding remarks

In this chapter, the short circuit performance of a 10 kV-rated SiC IGBT has been investigated by electrothermal simulations. The internal current density and temperature distributions revealed that the parasitic thyristor latch-up is the failure mechanism of the IGBT when the maximum temperature in the p-well region is about 1500 K. Furthermore, failure mechanisms due to the emitter contact melting or gate oxide cracking were discussed and the importance of detecting and clearing a short-circuit event in the initial stages of the phenomenon has been highlighted. Additionally, the influence of several circuit and device level parameters on the short circuit robustness was studied. It can be concluded that various device parameters can be adjusted accordingly to achieve the desired short-circuit withstand time for specific applications and system requirements.

Chapter 7

Novel Collector-Side Design Approach Breaking the Trade-off Between Maximum dV/dt and Device Efficiency

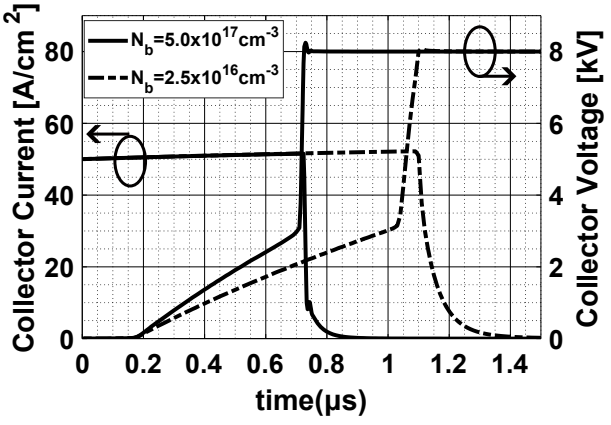
This chapter initially explores the trade-off between the maximum dV/dt during switching transients and the device's efficiency. Subsequently, it proposes a novel SiC IGBT device structure which can independently control the maximum dV/dt and the efficiency, achieving a better trade-off relation compared to the conventional IGBT structure. Finally, subsection 7.3.2 shows how the novel structure can further improve the unintentional turn-on robustness and short-circuit behaviour of a SiC IGBT, phenomena explained in detail in Chapters 5 - 6.

Part of the work presented in this chapter has been published in *I. Almpanis et al., "10kV+ Rated SiC n-IGBTs: Novel Collector-Side Design Approach Breaking the Trade-Off between dV/dt and Device Efficienc", Key Engineering Materials, May 2023* and *I. Almpanis et al., "Silicon Carbide n-IGBTs: Structure Optimisation for*

Ruggedness Enhancement," in IEEE Transactions on Industry Applications, Jan. 2024.

7.1 Trade-off between maximum dV/dt and device efficiency

As demonstrated in Chapter 3, SiC IGBTs, much like their silicon counterparts, exhibit a trade-off relationship between their on-state and switching losses. Subsection 2.4.1 delved into the turn-off behaviour of SiC PT-IGBTs, illustrating how this trade-off can be controlled through adjustments in buffer layer parameters or carrier lifetimes. However, the relationship between the maximum dV/dt and efficiency remains less explored. Figure 7.1 illustrates this complex relationship by comparing the switching waveforms, on-state voltage drop, and maximum dV/dt of two 10 kV-rated IGBTs with varying buffer layer doping concentrations (N_B). The table in this figure depicts that low switching losses, achieved by using higher buffer layer doping concentration, come with the cost of higher on-state voltage drop and extremely high dV/dt rates.



N_b [cm^{-3}]	V_{on} [V]	E_{off} [mJ]	dV/dt [kV/µs]
5.0x10^{17}	3.94	53	420
2.5x10^{16}	3.75	115	91

Figure 7.1: I_c and V_c curves during the inductive turn-off of IGBTs with different buffer layer doping concentrations, and table summarising their conduction and switching characteristics.

To compare the performance of different IGBT designs directly considering their

on-state losses, switching losses and maximum dV/dt, these quantities must be clearly presented. For silicon IGBTs, the commonly used E_{off}–V_{on} trade-off curves (similar to what is shown in Fig. 3.4) are sufficient because the maximum dV/dt is not a parameter of concern. However, in SiC IGBT, the maximum dV/dt is also a quantity that needs to be optimised. Figure 7.2 is used to clearly represent these three optimisation parameters, with the colour of each point indicating the maximum dV/dt during inductive turn-off under a current density of 25 A/cm^2. Thirty IGBTs with different buffer designs are compared in this figure, each of them having a different buffer layer doping concentration and thickness. It is evident that lower dV/dt always comes with the cost of higher switching losses, and all three depicted quantities are strongly coupled.

Another method to compare different IGBT designs involves calculating the maximum achievable switching frequency for a given thermal limitation. Assuming the maximum power dissipation on losses (P_{max}) is limited by the packaging heat extraction capability at $300W/cm^2$ and with a duty cycle (δ) of 50%, the maximum switching frequency (f_{max}) can be determined using Eq. 7.1. This approach simplifies the three-variable optimisation problem to a two-variable one, revealing an almost linear relationship between maximum switching frequency and dV/dt, as illustrated in Fig. 7.2(b) for various IGBT designs and current densities.

$$f_{max} = \frac{P_{max} - \delta \cdot V_{on} \cdot J_c}{E_{off}} \tag{7.1}$$

7.2 Proposed Structure

The proposed structure, which decouples dV/dt from the $V_{on} - E_{off}$ trade-off, is depicted in Fig. 7.3. With this structure, the switching speed of an IGBT can be

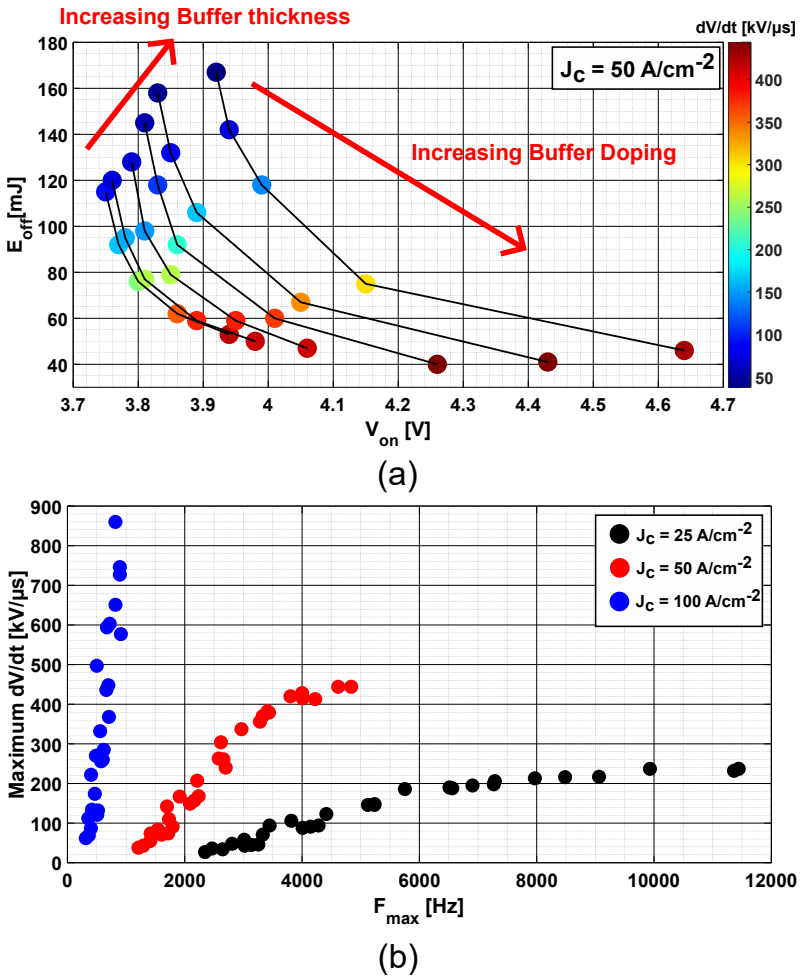


Figure 7.2: (a) V_{on}–E_{off}–dV/dt trade-off curves for different IGBT designs and (b) the relationship between maximum achievable switching frequency and maximum dV/dt of conventional PT-IGBT designs under different current densities.

increased without being constrained by high dV/dt and EMI-related issues. This structure is similar to the conventional one, with the difference of using a stepped doping profile in the drift and the buffer layer and consists of four n-type layers that can be fabricated using standard processes. The roles of these layers are as follows:

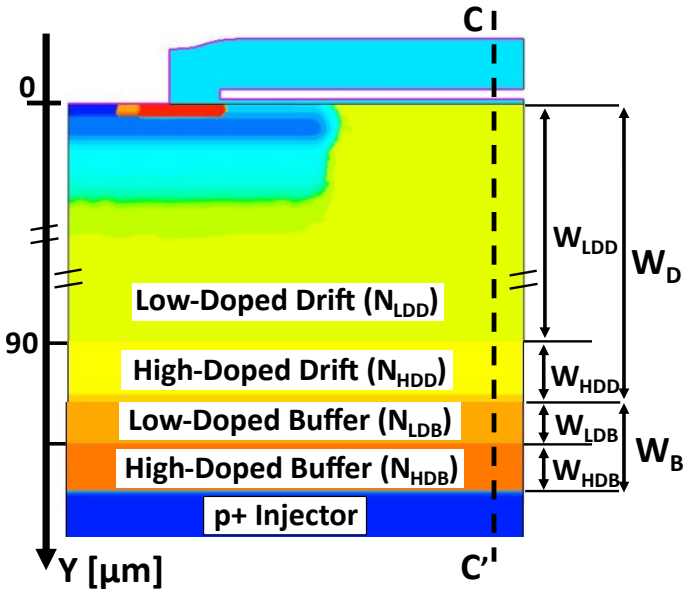
- The Higher Doped Buffer region (HDB) prevents the depletion region from reaching through to the injector region during the forward blocking state. It provides the minimum buffer charge, as described by Eq. 2.1.

- The Lower Doped Buffer region (LDB) controls the plasma injection into the drift layer. Varying its doping density or width adjusts the trade-off between

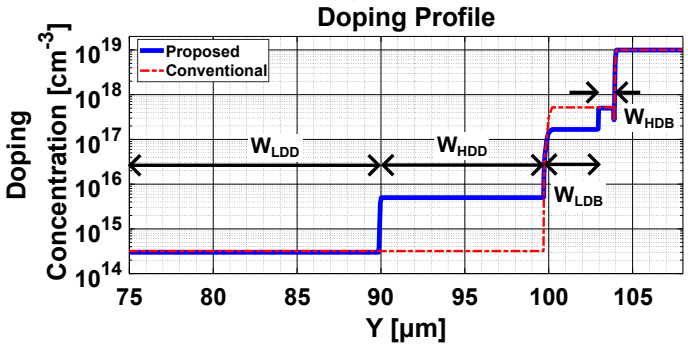
the on-state and switching losses.

- The Higher Doped Drift region (HDD) prevents the depletion region from punching through to the buffer layer during the voltage-rising phase of the turn-off process. As a result, it controls the maximum dV/dt by increasing the amount of minority carriers to be removed during the fast voltage transient phase.

- Finally, the Lower Doped Drift region (LDD) governs the breakdown characteristics and the PT voltage of the IGBT.



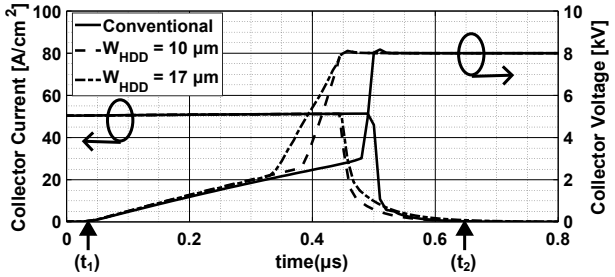
(a)



(b)

Figure 7.3: (a) Novel collector-side IGBT design featuring a stepped doping profile for the buffer and drift layers, (b) doping profile comparison between the conventional and proposed structures across the c-c' cut.

This simple device structure offers the advantage of almost independent control of the trade-off between on-state losses, switching losses and maximum dV/dt. Figure 7.4 shows how the high dV/dt phase during the inductive turn-off process can be controlled with the appropriate selection of doping density and width of the HDD. In this case, the electric field changes slope in the interface between the LDD and HDD regions, instead of the interface between the drift and buffer layer of the conventional structure as shown in Fig. 7.5. As a result, the depletion region does not reach the buffer layer, leading to an 87% reduction of the maximum dV/dt without significantly affecting the on-state voltage drop and the turn-off switching losses of the IGBT.



(a)

	V_{on} [V]	E_{off} [mJ]	dV/dt [kV/µs]	F_{max} [Hz]
Conventional	4.06	47	413	4223
W_{HDD}=10 µm	4.1	49	86	4031
W_{HDD}=17 µm	4.08	46	52	4304

(b)

Figure 7.4: (a) Turn-off comparison of $I_c(t)$ and $V_c(t)$ curves between the conventional IGBT and those with different Higher Doped Drift region (HDD) to reduce dV/dt during the rapid voltage rise phase, and (b) table summarising their on-state and switching characteristics.

Figure 7.6 shows how the Lower Doped Buffer region (LDB) affects the trade-off between $V_{on} - E_{off}$. It is evident that the optimum $V_{on} - E_{off}$ for a desired application can be chosen without significantly affecting the dV/dt.

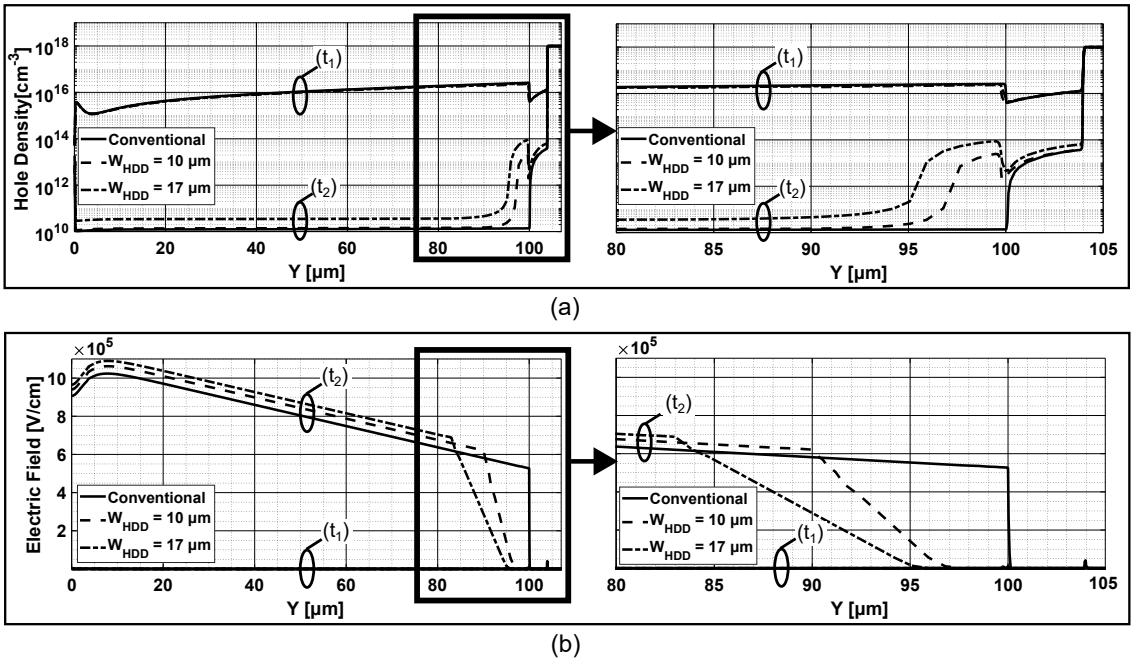
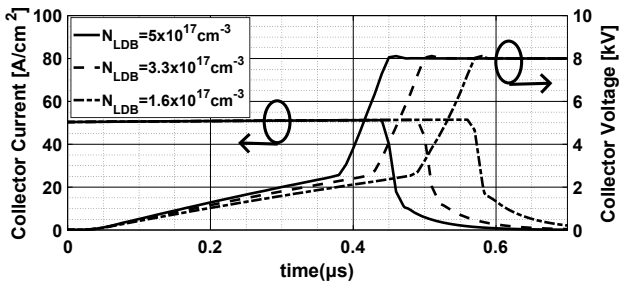


Figure 7.5: Comparison of the (a) hole densities and (b) electric field inside the conventional IGBT and IGBTs with different Higher Doped Drift region (HDD) at the beginning and ending of the turn-off process.

7.3 Comparisson between conventional and proposed structure

7.3.1 Trade of relationship between switching losses and maximum dV/dt

The effectiveness of the proposed device structure in reducing the maximum dV/dt is evident in Figures 7.7(a) and 7.7(b). The coloured dots within the diamond symbols in Figure 7.7(a) symbolise different variants of the proposed IGBT structure. Compared to traditional designs, the maximum dV/dt of these proposed IGBT structures shows a significant improvement. Additionally, the reduction in dV/dt at a specific switching frequency, achieved through the new design, is illustrated in Figure 7.7(b). Here, red points denote conventional IGBT designs, while black and blue points represent two distinct versions of the proposed design. The maximum



(a)

N_{LDB} [cm^{-3}]	V_{on} [V]	E_{off} [mJ]	dV/dt [kV/µs]	F_{max} [Hz]
5x10^{17}	4.1	49	86	4031
3.3x10^{17}	4.04	55	77	3618
1.6x10^{17}	3.95	64	67	3145

(b)

Figure 7.6: (a) Turn-off comparison of $I_c(t)$ and $V_c(t)$ curves between IGBTs with different Lower Doped Buffer region (LDB) for $V_{on} - E_{off}$ trade-off control, and (b) table summarising their on-state and switching characteristics.

switching frequency for each simulated device, operating under an inductive load of $25A/cm^2$, was calculated using Equation 7.1.

7.3.2 Unintentional turn-on and short circuit ruggedness

For the results presented in this section, the device that was used to present the unintentional turn-on and short circuit phenomena in Sections 5.1 and 6.3 was initially optimised according to the analysis presented in Chapters 5 and 6 (Conv. optimised) and further optimised by adjusting the four epitaxial layers of the proposed structure (novel optimised). During the optimisation process, several device parameters were varied to improve the ruggedness of the IGBT, while ensuring the on-state and switching losses remain relatively unaffected.

Chapter 5 showed that the optimisation of the emitter side of the SiC IGBT can reduce the gate voltage spike, caused by the high dV/dt, by up to 78%. In addition, the reduced dV/dt achieved by the proposed structure can nearly eliminate unintentional turn-on chances with the 90% reduction of the gate voltage spike, as shown in Fig. 7.8.

Chapter 6 showed that several structural parameters can be modified to improve the short-circuit robustness of a SiC IGBT. In addition to this, the proposed structure can further improve the short circuit behaviour due to the reduction of the peak

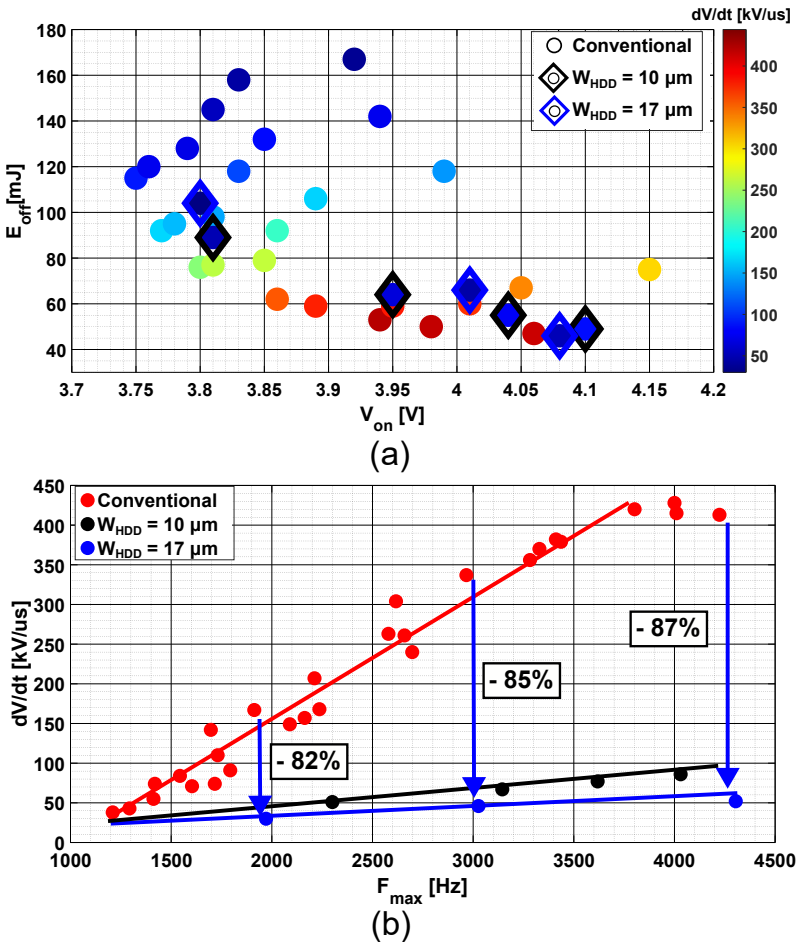


Figure 7.7: Comparison between the conventional and the proposed structure with $W_{HDD} = 10\mu m$ and $W_{HDD} = 17\mu m$ using (a) the V_{on}–E_{off}–dV/dt trade-off curves and (b) F_{max}–dV/dt trade-off curves

current density at the initial stages of the short circuit and reduced saturation current density, as shown in Fig. 7.9.

7.4 Concluding remarks

This chapter presented a novel device structure which can mitigate the high dV/dt produced during the turn-off process of SiC PT-IGBTs. By using a four-step n-type doping profile on the collector side, the IGBT efficiency and dV/dt can be controlled independently. Furthermore, this device structure simplifies the IGBT optimisation procedure because it provides a straightforward relationship between

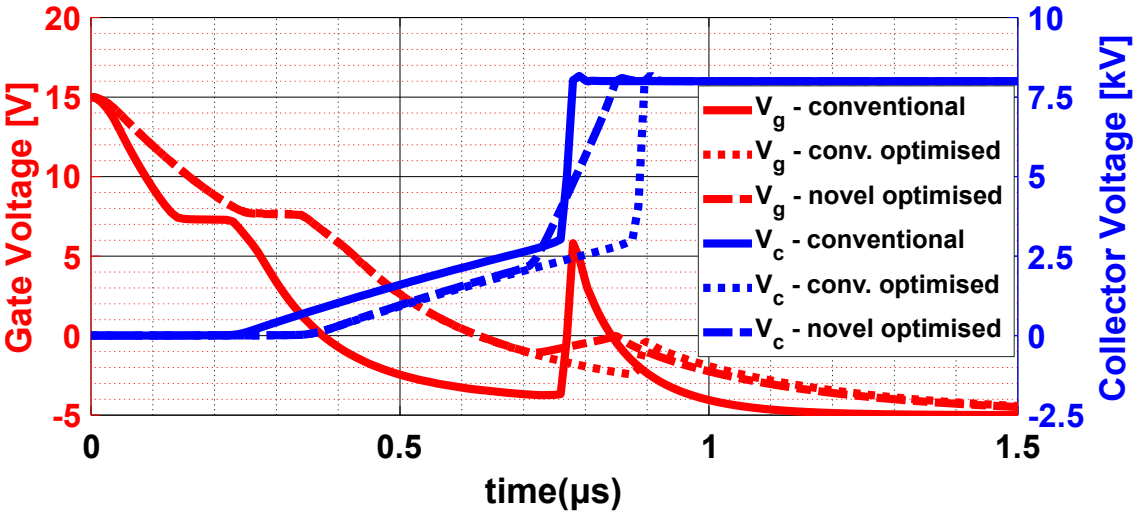


Figure 7.8: Gate voltage spike reduction during the inductive turn-off of an IGBT by employing emitter side optimisation and the novel device structure.

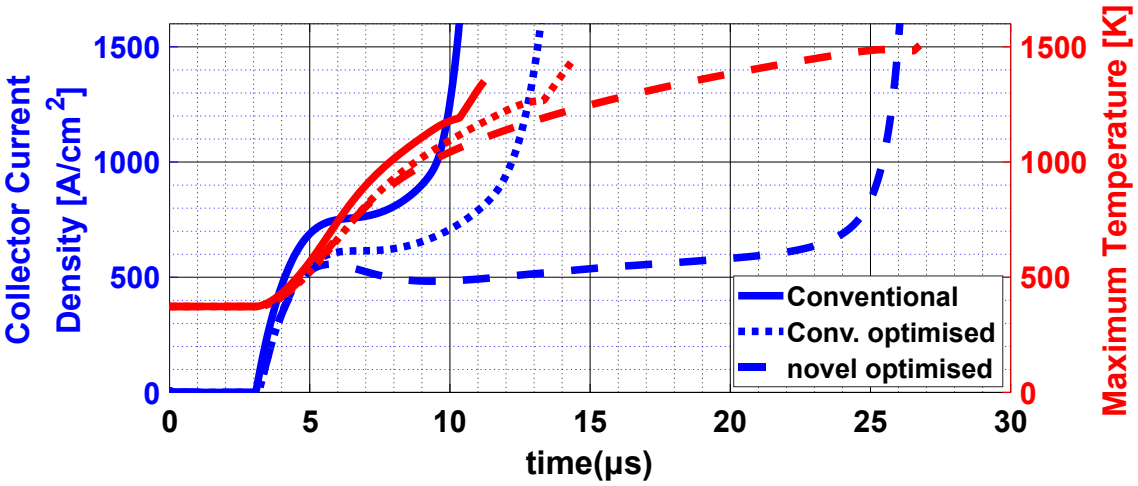


Figure 7.9: Short-circuit behaviour improvement achieved by using the proposed SiC IGBT structure (at $V_{dc} = 10kV$).

the device parameters and operational characteristics. As a result, an optimal device can be designed for specific application requirements.

Chapter 8

Performance Prediction and Optimisation of SiC IGBTs Rated at 10-40 kV

Chapters 2-7 have demonstrated that several trade-offs must be considered when optimising device structures, as many parameters influence different operational characteristics. Furthermore, the broad range of potential application conditions makes it impossible to optimise a device structure to meet all requirements (such as efficiency, ruggedness, cost, etc.). Similar limitations existed during the early development of Integrated Circuit (IC) and led to the successful concept of Aplication-Specific Integrated Circuit (ASIC), where a chip is optimised for a specific application to enhance performance and cost-efficiency. However, although the optimisation process of power semiconductor devices is more complicated and the application conditions cannot be easily standardised, an understanding of the potential behaviour of ultra-high voltage ($> 10kV$) SiC IGBTs can be used as an input to the design of future high-power converters. Therefore, this chapter aims to provide a comprehensive overview and predict the performance of SiC IGBTs rated at 10-40

kV.

To achieve this, four different drift epitaxial layers were studied with their doping concentrations and thicknesses detailed in Table 8.1, alongside the validated 27kV IGBT [10]. The same material and process-dependent parameters have been used across all devices, following the validation process outlined in sections 4.2-4.3. All five devices' simulated Breakdown Voltage (BV) are consistent with the simulation results and analytical solutions in [88]. Additionally, the static and dynamic performance of the 13 kV and 20 kV rated devices align well with the performance of the fabricated devices presented in [25, 26, 100].

Table 8.1: Doping concentrations and widths of drift layers for IGBTs rated at 13-40 kV

Breakdown Voltage	**Drift region width**	**Drift region doping**
13 kV [25, 100]	100 μm	3×10^{14} cm^{-3}
20 kV [26]	160 μm	1.75×10^{14} cm^{-3}
27 kV[10]	210 μm	1.3×10^{14} cm^{-3}
30 kV	260 μm	1.5×10^{14} cm^{-3}
40 kV	360 μm	1.25×10^{14} cm^{-3}

Part of the work presented in this chapter has been published in *I. Almpanis et al., "Silicon Carbide n-IGBTs: Structure Optimisation for Ruggedness Enhancement" in IEEE Transactions on Industry Applications, Jan. 2024.*

8.1 On-state performance

Figure 8.1 illustrates the $I_c - V_c$ characteristics of IGBTs rated at 13-40 kV at room temperature. The plot's red line represents the $300W/cm^2$ heat transfer limit of the packaging for on-state losses, a standard benchmark in power devices. While this limit could be increased with innovative substrates or packaging techniques [138], our study adheres to the $300W/cm^2$ limit.

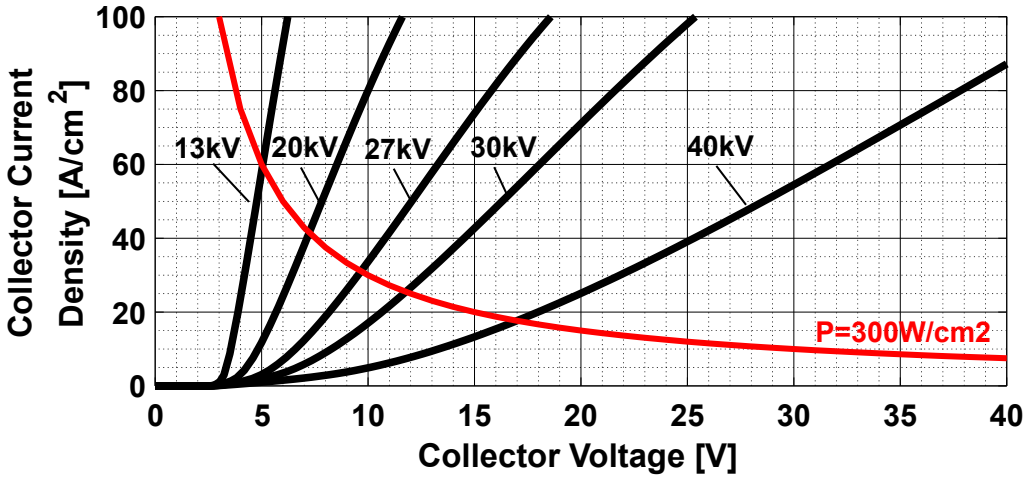


Figure 8.1: $I_c - V_c$ characteristics of IGBTs rated at 13-40 kV.

Notably, the on-state voltage drop increases for IGBTs with higher ratings due to the thicker drift regions and lower doping concentrations required to withstand higher electric fields. Consequently, the maximum operating current density of these devices is constrained by the packaging's heat transfer capabilities, decreasing from $60A/cm^2$ for 13 kV devices to $17A/cm^2$ for those rated at 40 kV.

8.2 Switching performance

Figure 8.2 presents the turn-off characteristics of 13-40 kV devices at their maximum operational current density within the $300W/cm^2$ limit. The DC bus voltage is 60 per cent of the breakdown voltage for all devices, reflecting the typical operating condition for high-voltage power devices.

For all IGBTs, the space charge region extends to the buffer layer before the collector voltage reaches the DC bus voltage, resulting in a high dV/dt phase. Hence, the analysis in Chapter 5 and the novel device structure proposed in Chapter 7 can be generalised for all PT-IGBTs rated at 13-40 kV. For example, Fig. 8.3 demonstrates the gate voltage spike mitigation for IGBTs rated at 13 kV and 40 kV through optimisation of C_{ge}, as discussed in Chapter 5. Similar voltage spike suppression

was observed across all voltage classes.

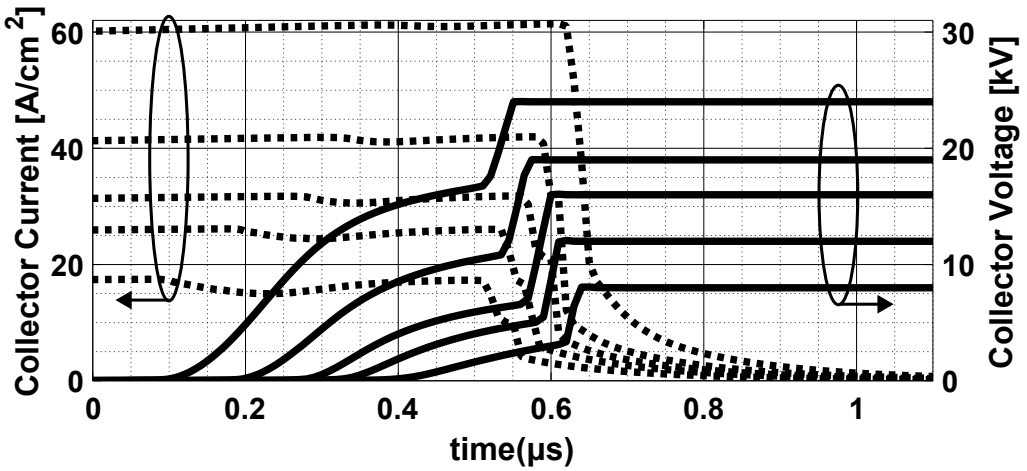


Figure 8.2: Collector current and collector voltage during inductive turn-off of IGBTs rated at 13-40 kV.

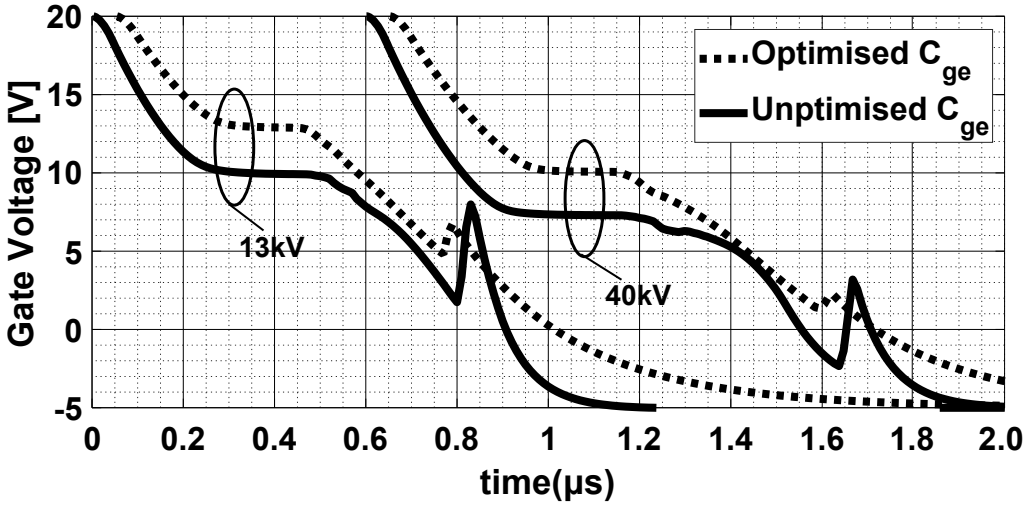


Figure 8.3: Gate voltage spike during the fast voltage rising phase of the IGBT turn-off process.

8.3 On-state voltage drop and turn-off switching losses trade-off curves

This section illustrates the trade-off curves between on-state voltage drop and switching losses for devices rated between 13 and 40 kV. To achieve this, the maximum carrier lifetime parameters t_p and t_n (see Eq. 4.8-4.9) have been modified to

control the conductivity modulation of the drift region. The ratio $t_n/t_p = 5$ has been kept constant across all device structures, in line with the ratio used during the validation process outlined in Chapter 4.

Figure 8.4 presents the trade-off curves between the on-state voltage drop and turn-off switching losses for current density defined by the $300W/cm^2$ power limit and DC bus voltage equal to 60 per cent of the breakdown voltage. These curves demonstrate that while design performances align with technology trends, selecting an optimal design requires consideration of specific application requirements, such as switching frequency, DC bus voltage, or converter topology. Nonetheless, these curves offer valuable guidelines for estimating the power losses in a particular application and determining the optimal device.

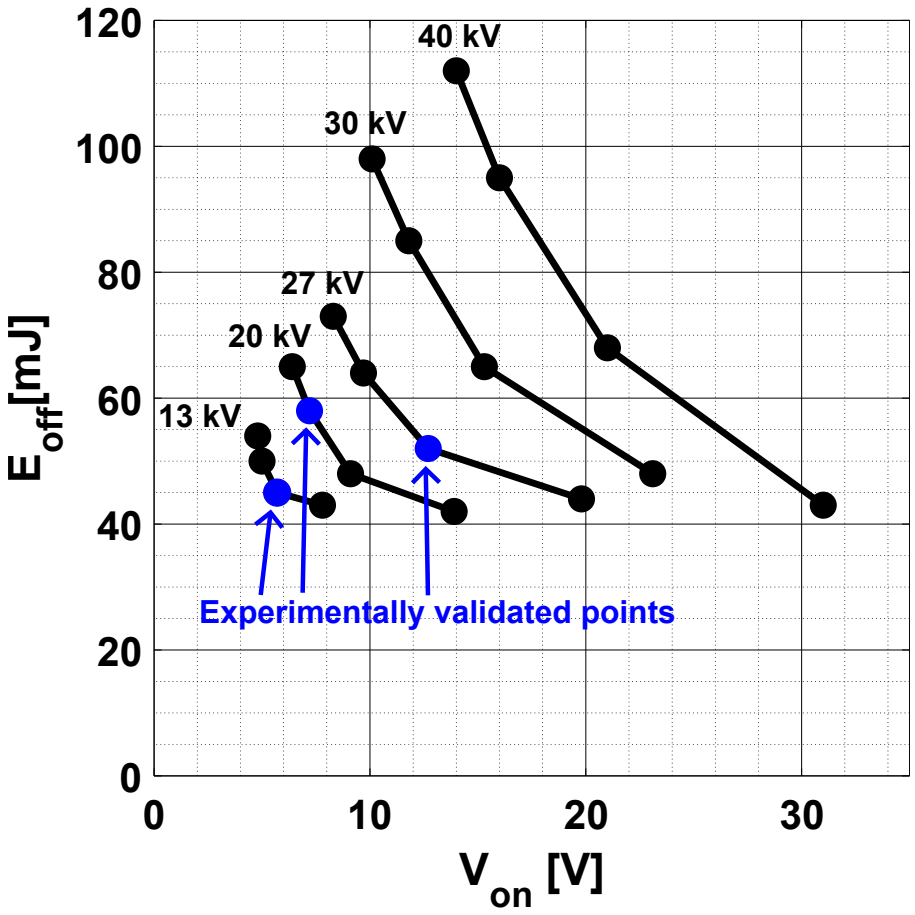


Figure 8.4: Trade-off curves between the on-state voltage drop and turn-off switching losses of IGBTs rated at 13-40 kV at room temperature. The experimentally validated points are for the fabricated devices demonstrated in [10, 25, 26].

8.4 Short Circuit behaviour

Figure 8.5 shows the short circuit behaviour of the 13-40 kV rated IGBTs at 60% of their breakdown voltage through a stray inductance of 100 nH. The lower voltage devices suffer from shorter SCWT due to higher internal PNP transistor current gain, thinner drift region and faster temperature rise.

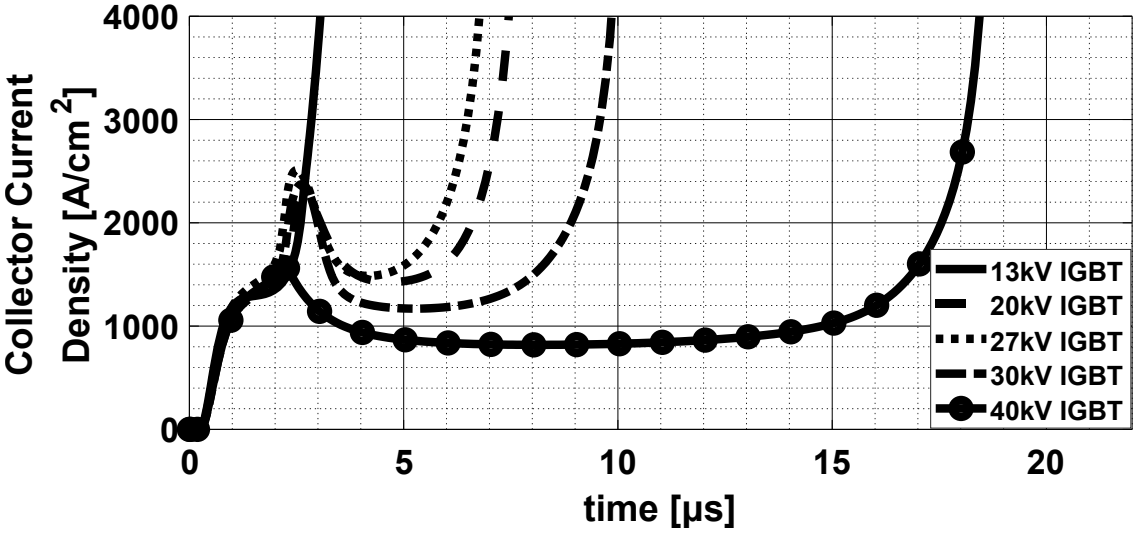


Figure 8.5: Short-circuit behaviour of IGBTs rated at 13-40kV.

The short circuit performance can be enhanced through the incorporation of the HDD layer and optimisation of the emitter side parameters, as detailed in Chapters 5-7. However, the simulation results presented in this section and Chapter 6 highlight a critical challenge: achieving the typical 10 μs SCWT required for silicon IGBTs in SiC IGBTs is difficult without compromising device efficiency. For instance, meeting this SCWT requirement at the device level may involve modifying the buffer layer or adjusting carrier lifetimes in the drift region to decrease the internal PNP transistor current gain, albeit at the expense of increased on-state voltage drop.

8.5 Active and edge termination area optimisation

This thesis primarily discusses the design and optimisation of the IGBT active cell. However, a power semiconductor device comprises many paralleled cells on a die. Determining the maximum die area involves complex considerations, including material quality, manufacturing capabilities, performance and reliability of active and edge termination area, costs, and production volume, which are beyond the scope of this study. This section, nevertheless, aims to provide a quantitative analysis of the trade-offs involved in deciding the area of a power semiconductor device.

Firstly, the edge termination length for a SiC device rated at over 10 kV typically ranges from 500 to 1500 μm, as highlighted in the literature review in subsection 3.3.4. Shorter termination lengths, achieved through advanced fabrication techniques, may increase production costs. However, these techniques enable more efficient use of the die area, allowing for larger active areas and indirectly improving the device's conduction characteristics. It is also important to note that devices with thicker drift regions necessitate larger edge termination areas, which should also be considered in deciding the optimum device for a particular application.

Regarding the total die area, a trade-off exists between the maximum size and manufacturing yield; as the die area increases, the likelihood of material and processing defects also rises, reducing yield [139]. Consequently, the maximum active area for SiC MOS-based devices is typically around $1cm^2$, requiring paralleling of multiple dies for high-power applications. Moreover, the epitaxial growth of thick drift regions (200-400 μm) can compromise the crystal structure [1], further impacting manufacturing yield and limiting the maximum feasible die area for higher voltage devices.

8.6 Parallel operation

According to what was discussed in Sections 8.1 and 8.5, the predicted maximum current density for a SiC IGBT die is summarised in Table 8.2, considering a die area of 1 cm^2, an edge termination length of 500 μm, and the active area's maximum current densities in light of the packaging heat transfer limit of $300W/cm^2$. As a result, it is essential for these dies to be connected in parallel to create a power module able to handle currents in the range of several hundreds of amperes. Similar requirements exist in other MOS-based devices, such as 3.3 kV-rated SiC MOSFETs where 40 dies have been connected in parallel to achieve a total current of 900 A [140].

Table 8.2: Predicted maximum current per die, for SiC IGBTs rated at 13-40 kV

Breakdown Voltage	**Maximum current per die**
13 kV	49 A
20 kV	33 A
27 kV[10]	26 A
30 kV	22 A
40 kV	14 A

Achieving reliable parallel operation necessitates a positive temperature coefficient of the on-state voltage drop, as discussed in Section 3.3.3. However, Fig. 8.6 demonstrates that devices rated at 13 kV and 20 kV exhibit a negative temperature coefficient, whereas higher voltage devices show a positive one. This happens because of using the same carrier lifetime parameters ($\tau_e = 5 \times \tau_h = 1.55\mu s$) across all simulations, which were validated for the 27 kV IGBT but may not be optimal for all voltage classes. Although higher voltage IGBTs might require higher carrier lifetimes to modulate the conductivity of their entire drift regions, which are 300-400 μm long, for the lower voltage IGBT, a high carrier lifetime makes the hole current component of the emitter current the dominant contributor of the IGBT's conduction and leads to the negative temperature coefficient of the on-state voltage drop. To ensure a positive temperature coefficient across all devices rated at 10-40

kV, a co-adjustment of carrier lifetimes [141, 142] and carrier injection through the emitter side [143] and the collector side [57, 77, 144] is required.

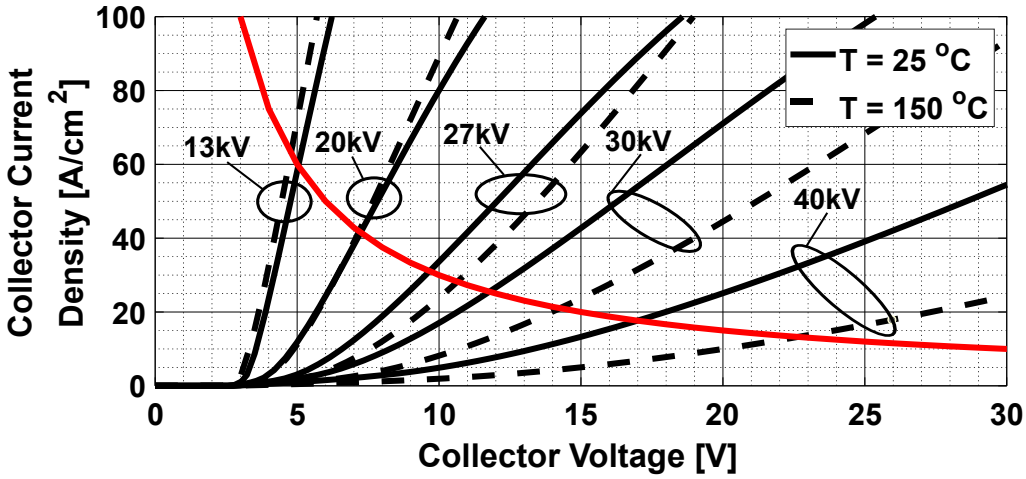


Figure 8.6: $I_c - V_{ce}$ characteristics of 13-40kV IGBTs at 25 °C and 150 °C.

8.7 Concluding remarks

This chapter analysed SiC IGBTs rated at 10-40 kV, covering their static and dynamic characteristics and short circuit behaviour. While it is impossible to propose an optimum IGBT design that meets all application requirements, the comprehensive range of results presented here provides valuable guidance for semiconductor and converter designers in optimising device structures and estimating converter performance. The critical insights derived from this chapter are summarised as follows:

- The predicted maximum current per die varies by voltage class, ranging from 10 to 50 A. This necessitates the parallel operation of such devices, underscoring the importance of considering this aspect early in the device design process.

- Achieving a positive temperature coefficient of the on-state voltage drop is crucial for reliable parallel operation. This requirement demands careful at-

tention to the IGBT structure and parameters, especially for SiC IGBTs rated up to 20 kV, where the conductivity modulation of the drift region must be controlled to ensure positive temperature coefficient.

- High dV/dt during switching transients poses reliability issues, such as EMI or unintentional turn-on, across all voltage classes of SiC IGBTs. As discussed in Chapters 5 and 7, optimising the device structure can address these concerns.

- While methods detailed in Chapters 6 and 7 can improve SiC IGBT's short circuit behavior, meeting the typical 10 μs SCWT requirement without compromising efficiency remains challenging.

- Efficient edge termination design is vital for high-voltage devices, ensuring robust blocking capability and its indirect impact on the die's conductivity characteristics. Effective termination techniques free up more area for active use, enhancing the device's overall performance.

Chapter 9

Behavioural SiC IGBT Modelling Using Non-Linear Voltage, Current and Temperature Dependent Capacitances

The previous chapters analysed and predicted performance and ruggedness aspects of SiC IGBTs and proposed methods for optimising their structure. Instrumental to achieve that was the usage of calibrated FEM simulations. However, as explained in Section 3.1, although FEM modelling is a very useful tool for device-level simulations to optimise the cell design or provide insights into the semiconductor behaviour, it is not suitable for power converter topologies simulations due to its low computational speed. Compact models , which are mathematical models that aim to represent a particular device's current and voltage waveforms without considering the cell design details, are more appropriate for this task. Subsection 3.1.2 showed that although several physics-based compact models have been proposed for SiC IGBTs, there is yet no reported behavioural model in the literature. This

chapter aims to present such a model, achieving very fast computational speed and accuracy by using non-linear voltage and current-dependent capacitances to model the behaviour of the SiC IGBT.

The rest of this chapter is structured as follows. Section 9.1 briefly describes the proposed behavioural model and the discrete components that it uses. Sections 9.2-9.3 present the mathematical equations used to describe the non-linear relationships of the discrete components and show the modelling accuracy by comparing the behavioural model results with that of the validated 27 kV-rated SiC IGBT TCAD model presented Chapter 4. Finally, Section 9.4 demonstrates the ability of the proposed model to be used in topology-level simulations, and Section 9.5 concludes the chapter.

Part of the work presented in this chapter has been published in *I. Almpanis et al., "Behavioural SiC IGBT Modelling Using Non-Linear Voltage and Current Dependent Capacitances," 2023 IEEE Design Methodologies Conference (DMC).*

9.1 Behavioural model description

Figure 9.1(a) shows the IGBT structure with the internal parasitic components, including a MOSFET, two bipolar transistors, a PiN diode, a resistance and three capacitances. Similar equivalent circuits have been used for the physics-based models mentioned in subsection 3.1.2, where each discrete component is modelled using physical equations and parameters. However, the proposed behavioural model shown in Fig. 9.1(b) is a simplified variation of the physics-based model with the ability to operate at faster computational speeds and without requiring physical parameters and device structure details.

The static performance of the IGBT is represented in the proposed model by the

gate and collector voltage-dependent current source (I_{st}), similar to what is widely used for unipolar devices [145]. The current tail of the IGBT is modelled by a dependent current source (I_{rc}), where the current exhibits an exponential decay with two different time constants τ_1 and τ_2, each of them simulating the minority carrier recombination process in the drift and the buffer layer respectively. Finally, since the injected plasma depends on the total current flowing within the device, and the depletion region width depends on the collector voltage (2.9), it makes physical sense to represent the effective gate-to-collector capacitance (C_{gc}) and collector-to-emitter capacitance (C_{ce}) capacitances with non-linear capacitances, dependent both on the collector current and the collector voltage.

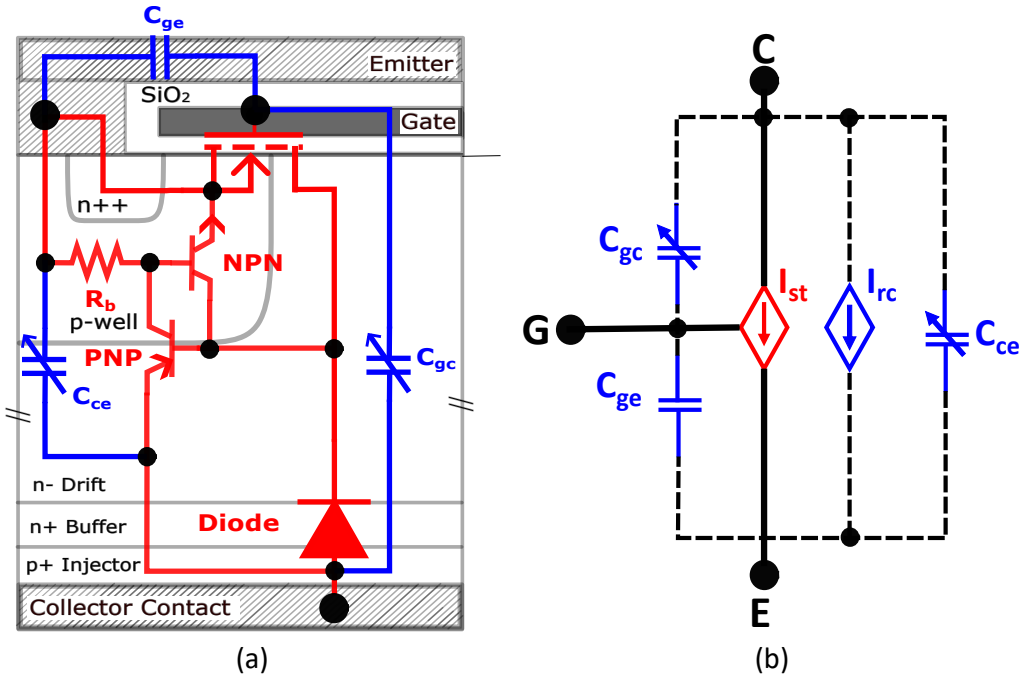


Figure 9.1: (a) IGBT cell structure and internal parasitic components representation, (b) IGBT compact model.

A detailed description of each of the circuit mentioned above components is given in the following sections. This behavioural model has been implemented and tested in Simulink (see Appendix C), but it can be easily transferred to other simulation platforms like LTspice.

9.2 Static modeling

9.2.1 Isothermal at 300 K

The TCAD results for static $I_c - V_{ce}$ characteristics of the SiC IGBT at 300 K are shown in Fig. 9.2. The area below the power limit of $300W/cm^2$ or $500W/cm^2$ is the safe operational area of the IGBT under normal conditions. It can be seen that the IGBT 's static characteristics are similar to MOSFETs 's, with the only difference of a V_{ce} offset of about 3 V, which is the built-in potential of the parasitic PN diode between the injector and the buffer layer.

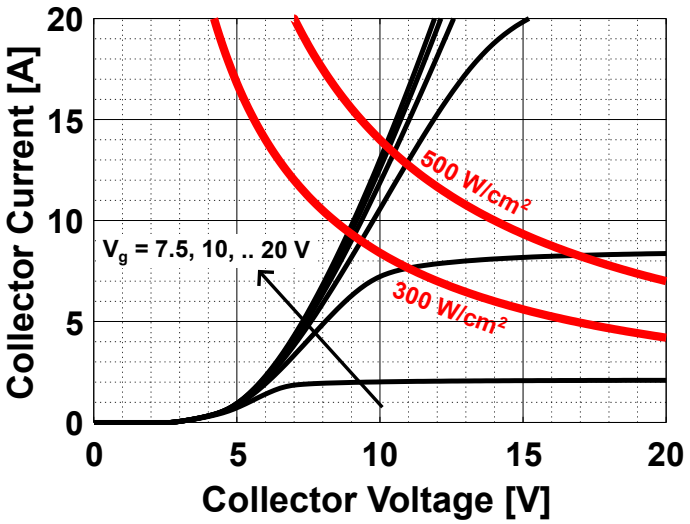


Figure 9.2: TCAD results for static $I_c - V_{ce}$ characteristics of the IGBT at different gate voltages.

Previous work presented in [145] showed that the static behaviour of a SiC MOSFET can be modelled by the set of equations 9.1 and 9.2. The parameters a, b and c in equation 9.1 depend on the gate voltage, and their values can be obtained from Eq. 9.2 with s being any of the parameters a,b,c and s_1,s_2,s_3,s_4 being fitting parameters. Figure 9.3 proves that the same equations can also accurately model the static characteristics of a SiC IGBT when using the parameters shown in TABLE 9.1.

$$I_{st} = a - \frac{a}{1 + \left(\frac{V_{ce}}{b}\right)^c} \tag{9.1}$$

$$s = \frac{s_1}{1 + \left(\frac{V_{ge} - V_{th}}{s_2}\right)^{s_3}} + s_4 \tag{9.2}$$

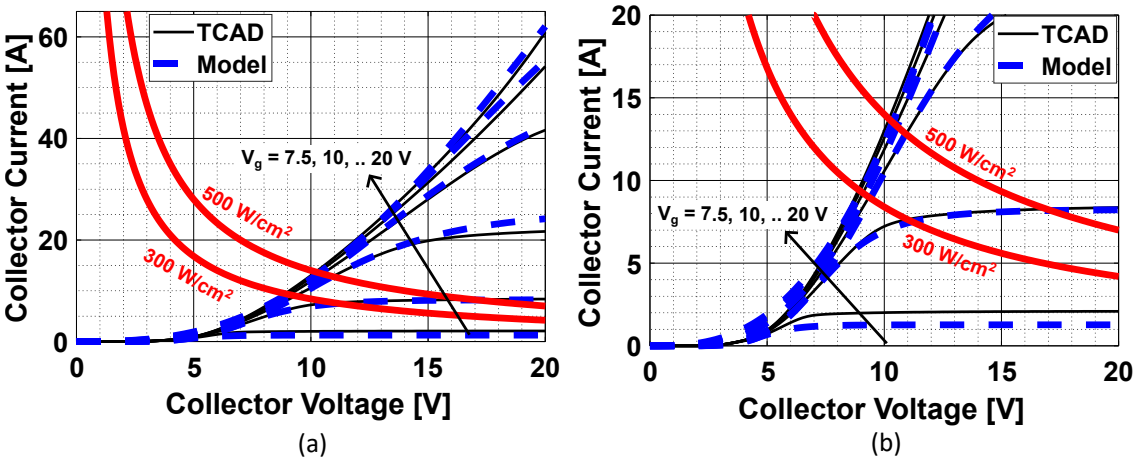


Figure 9.3: Comparison between TCAD and behavioural modelled $I_c - V_{ce}$ characteristics under different gate voltages.(a) For currents up to 60 A and (b), zoom in for currents close to the safe operational area.

Table 9.1: Parameter values for the static modelling

	a	**b**	**c**
s1	-21200	7027.2	7.5989
s2	70.1627	446.2525	6.7377
s3	3.0832	-1.6997	3.4622
s4	21200	3.4751	2.5620

9.2.2 Temperature-dependent static characteristics

Although the previously presented model is good at predicting the static IGBT behaviour at 300 K, the situation changes when the temperature increases due to the temperature dependence of various parameters as explained in Chapter 3.1.1. Figure 9.4 shows the temperature dependence of the threshold voltage, which can be modelled by the linear equation 9.3, with only two parameters $V_{th|300K}$ and

$V_{th|450K}$. These parameters are the threshold voltage at temperatures 300 K and 450 K, respectively.

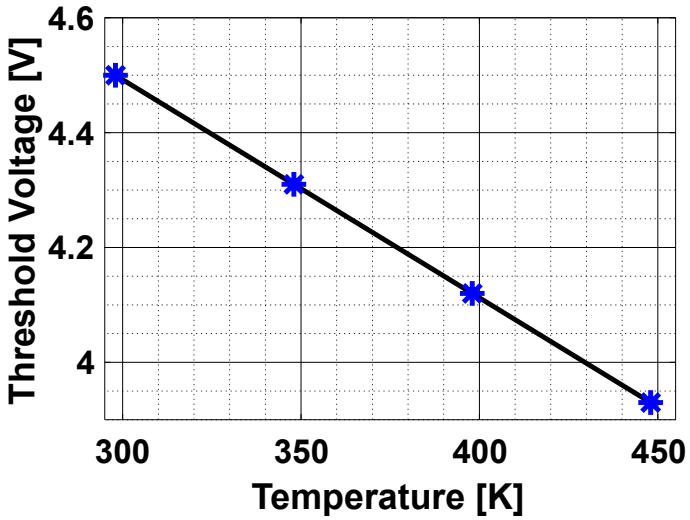


Figure 9.4: Temperature dependence of the gate threshold voltage.

$$V_{th}(T) = V_{th|300K} + \frac{(T - 300) \cdot (V_{th|450K} - V_{th|300K})}{150} \tag{9.3}$$

The model described in equations 9.1 and 9.2 can be modified to include the temperature dependence. Firstly, the V_{th} parameter is replaced by the linear equation 9.3. Additionally, a temperature-dependent parameter d is added in 9.1, as shown in Eq. 9.4. This parameter, d, is described by the non-linear equation 9.5. Figure 9.5 shows very good agreement between the TCAD and behavioural model results over a wide temperature range of 300-450K when using $d_1 = -0.31$, $d_2 = 118$, $d_3 = 4.6$ and $d_4 = 1.31$

$$I_{st} = a - \frac{a}{1 + \left(\frac{V_{ce}}{b \cdot d}\right)^c} \tag{9.4}$$

$$d(T) = \frac{d_1}{1 + \left(\frac{T-300}{d_2}\right)^{d_3}} + d_4 \tag{9.5}$$

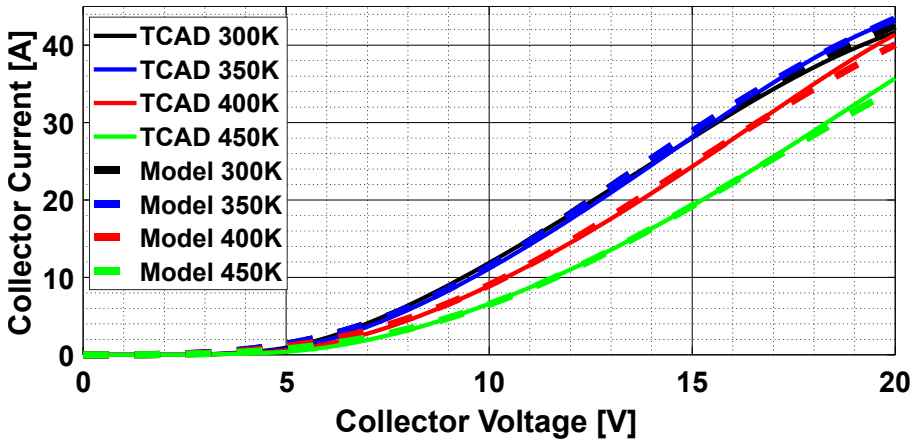


Figure 9.5: Comparison between TCAD and behavioural modelled $I_c - V_{ce}$ characteristics at different temperatures for $V_{ge} = 15$V.

9.3 Dynamic modeling

9.3.1 Non-linear C_{gc} and C_{ce} capacitances modelling

The non-linear capacitances C_{gc} and C_{ce} for different collector currents and voltages can be calculated using measurable currents and voltages during the inductive turn-off process. By applying Kirchhoff's laws to the equivalent circuit of Fig. 9.6 and assuming constant C_{ge}, the capacitances C_{gc} and C_{ce} can be calculated using equations 9.6 and 9.7. Therefore, the calculation of the C_{gc} and C_{ce} is possible by only knowing the assumed constant C_{ge} and the IGBT terminal voltages and currents under different conditions.

$$C_{gc} = \frac{i_g - C_{ge}\frac{dV_{ge}}{dt}}{\frac{dV_{gc}}{dt}} \tag{9.6}$$

$$C_{ce} = \frac{i_c + i_g - i_{st}(V_{ge}, V_{ce}) - C_{ge}\frac{dV_{ge}}{dt}}{\frac{dV_{ce}}{dt}} \tag{9.7}$$

Mixed-mode Sentaurus TCAD simulations were used to obtain the terminal voltages and currents of the validated IGBT under the inductive turn-off process. Particu-

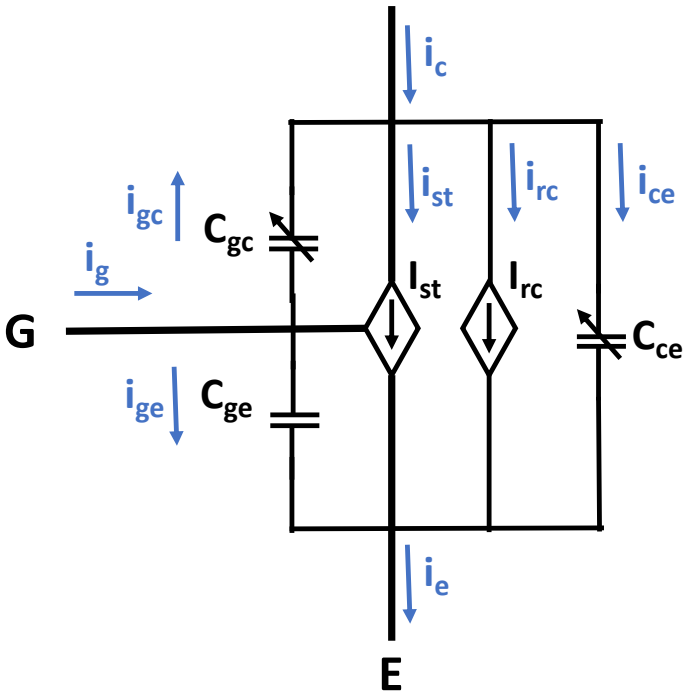


Figure 9.6: IGBT equivalent circuit.

larly, the modelled IGBT with an active area of $0.28cm^2$ (similar to [10]) was turned off at currents 0-15 A, and the voltage and the current dependency of the C_{gc} and C_{ce} are shown in Fig. 9.7. It can be seen that the C_{ce} reduces abruptly after the collector voltage reaches the punch-through voltage of the IGBT due to the much higher doping concentration of the buffer layer. Additionally, the C_{ce} changes non-monotonically with the collector voltage and increases for collector voltages close to the PT voltage (V_{PT}). This can be explained by the higher plasma concentration in the collector side of the drift region, as shown in Fig. 2.11. As a result, the depletion region expansion is slower for collector voltages closer to the V_{PT}, leading to an increased effective C_{ce}. The current dependence is unique to this IGBT model and is not found in existing MOSFET models with a similar structure. These capacitances are implemented in Simulink using 2D lookup tables with the collector voltage and current as inputs.

Figure 9.8(a-e) shows a comparison of the inductive turn-on and turn-off switching behaviour of the IGBT under different current densities and gate resistances. In Figure 9.8(f), the total switching losses for these cases are compared, confirming the

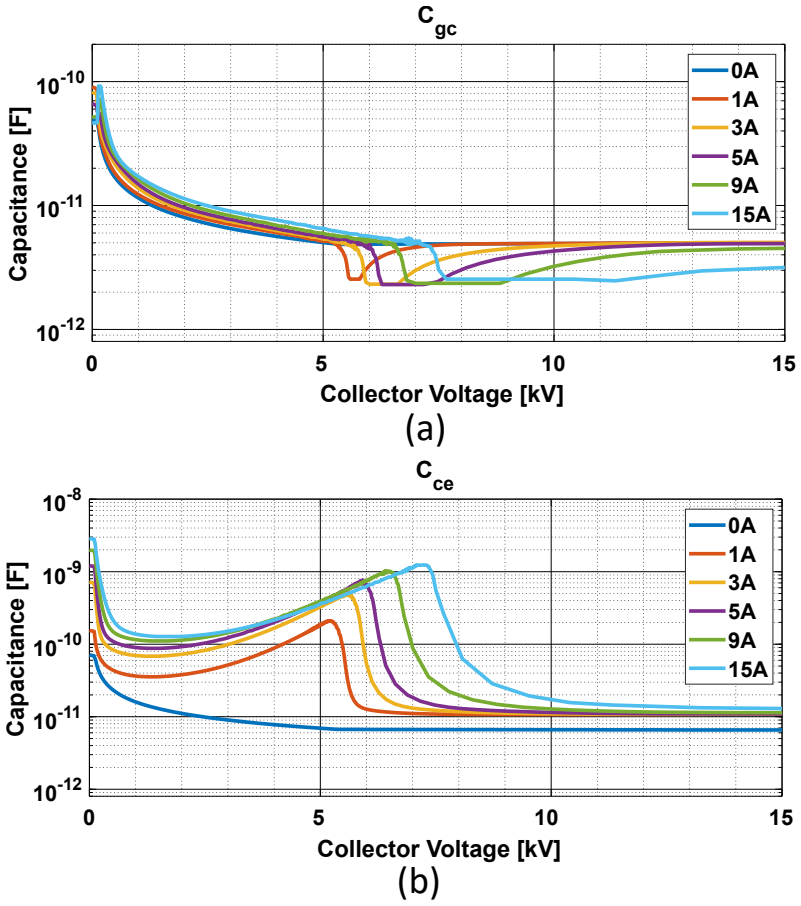


Figure 9.7: Voltage and current dependence of the (a) C_{gc} and (b) C_{ce}.

high accuracy of the proposed model. Thus, it can be concluded that the proposed model can accurately capture the unique characteristics of SiC IGBTs. It is worth noting that the time required for the Simulink model to run a turn-on and turn-off switching transient is 200 ms, where numerical TCAD simulations require 1-2 hours. This is a simulation time reduction of 4-5 orders of magnitude.

The plasma injection is enhanced at higher temperatures due to the increased number of activated dopants and, as a result, the turn-off switching process is slower. The calculated effective C_{ce} capacitance at temperatures in the range 300-450 K is shown in Fig 9.9 (a) and (b) for a collector current of 5 A and 15 A, respectively. The apparent noise in the calculated capacitances at higher temperatures comes from the discretized TCAD voltage and current waveforms that were used in equations 9.6 and 9.7 and can be reduced using either smaller simulation timestep or

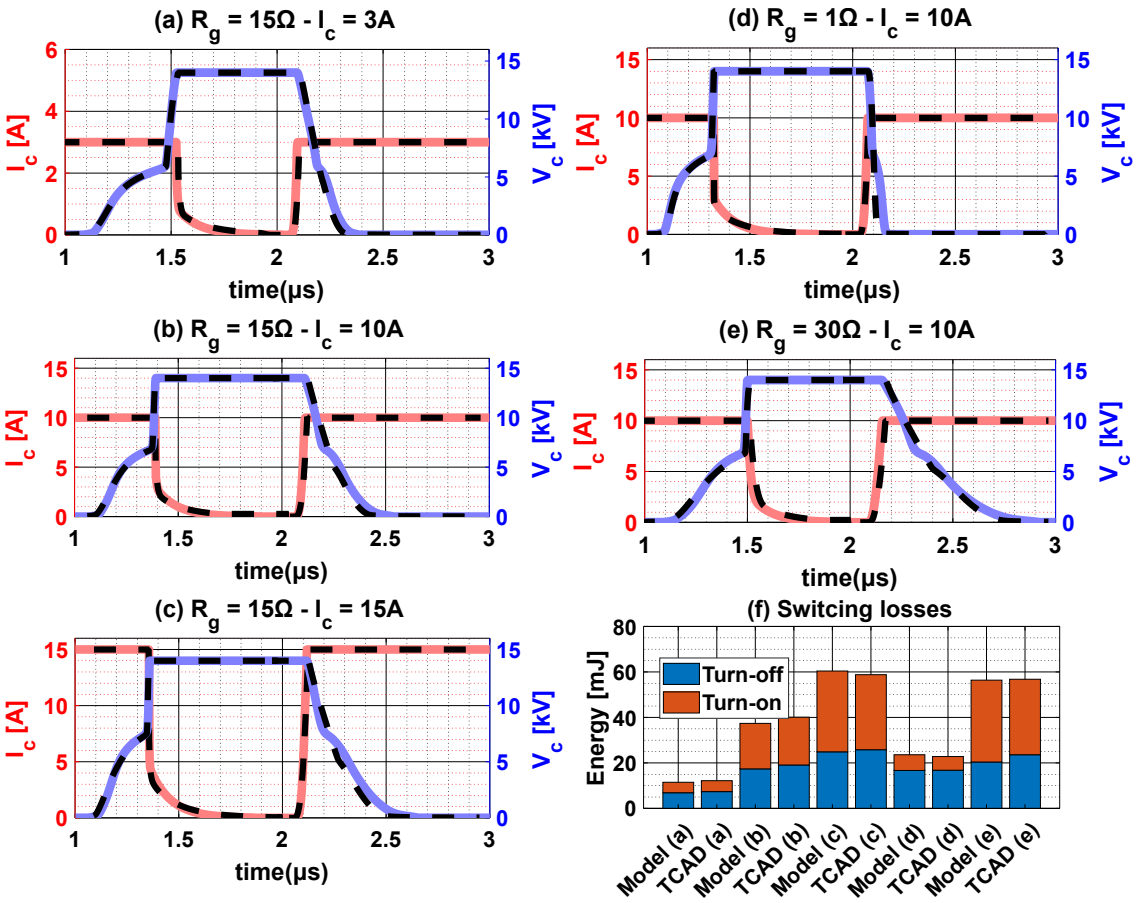


Figure 9.8: Switching behaviour comparison between the behavioral model (dashed lines) and the TCAD simulation results (solid lines).

reducing the solver tolerance. This shows the necessity of filtering the noise from the measurement probes when acquiring switching waveforms from a fabricated device.

The noise in the calculated capacitances of Fig. 9.9 is filtered and the temperature dependence of the capacitances is modelled by adding the temperature as a third input in the lookup tables. These increased capacitances lead to higher turn-off switching losses at elevated temperatures, as shown in Fig. 9.10, which compares the behavioural model and the TCAD simulation results.

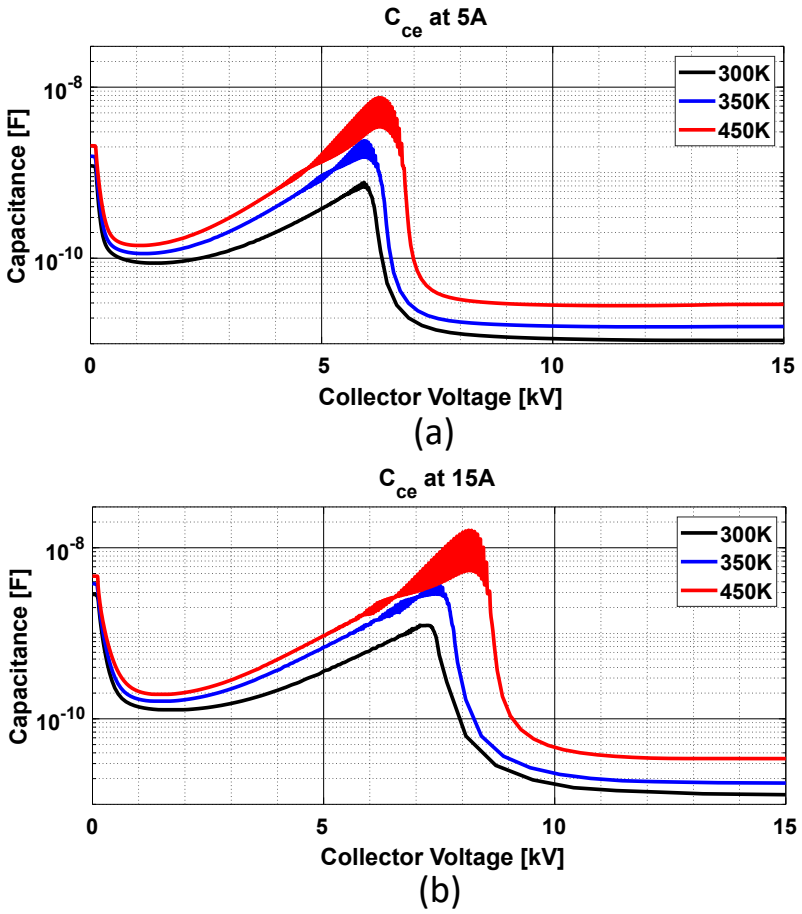


Figure 9.9: Temperature dependence of the C_{ce} at collector current of (a) 5A and (b) 15A.

9.3.2 Current tail modelling

The current tail during the turn-off process is a critical part of the IGBT behaviour and determines the turn-off switching losses. In contrast to unipolar devices, in IGBTs, the collector current cannot be abruptly reduced to zero when the collector voltage reaches the DC bus voltage because the minority carriers stored in the drift and buffer layer must be removed. Due to the different doping concentrations on these layers, their carrier recombination speeds are different, and as a result, the current has an initial fast decaying phase followed by a slow decaying phase (tail current), as explained in Section 2.4.1.

In the proposed model, the current decaying behaviour is modelled as a two-stage Resistive-Capacitive (RC) discharging circuit with different time constants, a slower

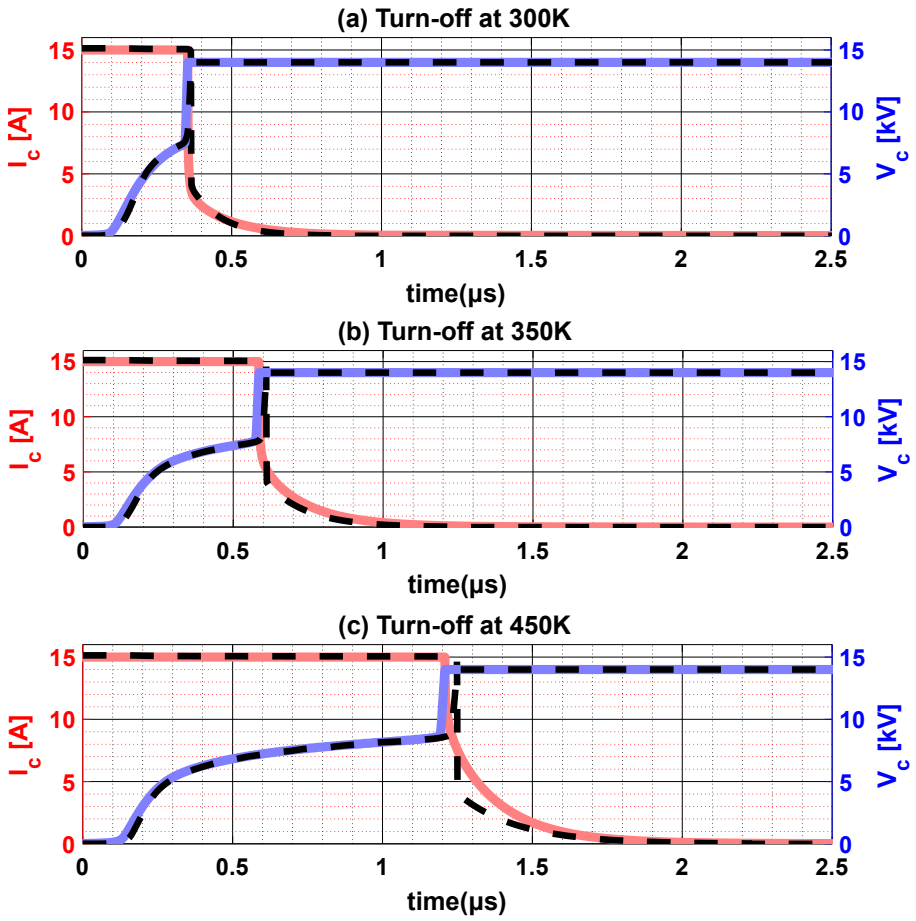


Figure 9.10: Inductive turn-off process comparison between the behavioural model (dashed lines) and the TCAD simulation results (solid lines) at temperatures 300-450 K.

and a faster one to simulate the minority carrier recombination in the drift and buffer layers, respectively. The Simulink implementation of this current decaying behaviour uses a Matlab function calculating the I_{rc} current according to equation 9.8. The quantity I_0 is the initial current at the beginning of the current falling phase (t_o), the parameter C is an arbitrary capacitance parameter, the $f_{initial}$ and f_{tail} are the percentages of the fast and slow decaying currents phases, and the parameters R_1 and R_2 are temperature dependent parameters according to Eq. 9.9.

$$I_{rc} = I_0 \left[f_{initial} \cdot e^{-\left(\frac{t-t_0}{R_1(T)\cdot C}\right)} + f_{tail} \cdot e^{-\left(\frac{t-t_0}{R_2(T)\cdot C}\right)} \right] \tag{9.8}$$

$$R_{1,2}(T) = R_{1,2|300K} + \frac{(T - 300) \cdot (R_{1,2|450K} - R_{1,2|300K})}{150} \tag{9.9}$$

9.4 Topology-level simulation

The IGBT model is evaluated in a topology simulation to test the model in a broader range of operational conditions. The results not only prove the convergence of the model but also demonstrate the ability to use a detailed model to simulate and optimise the design of a converter instead of the commonly used approach of using ideal switches and calculating the losses using lookup tables. The simulation results show that in addition to estimating the total semiconductor losses, the proposed model can predict further ruggedness reduction mechanisms such as false turn-on due to a voltage spike into the gate electrode (a phenomenon comprehensively explained in 5) or overvoltage due to the parasitic inductances and the high dV/dt.

The topology chosen in this case study is a buck converter, which is very important in HVDC or PV-powered applications, such as green hydrogen electrolysis, which has gained interest during recent years to contribute to meeting the net-zero targets [146].

Figure 9.11 shows the buck converter topology simulated in Simulink, using the proposed model and considering layout parasitics. The input-output requirements of the converter are shown in TABLE 9.2 and were used as a reference to show the optimisation curves of the converter.

Figure 9.12 shows terminal voltages and currents during a turn-off instance of the IGBT. The ability of the proposed model to capture high dV/dt, dI/dt and voltage spikes helps identify bad designs that can cause oscillations or false gate triggering at an initial product development phase, saving costs and time.

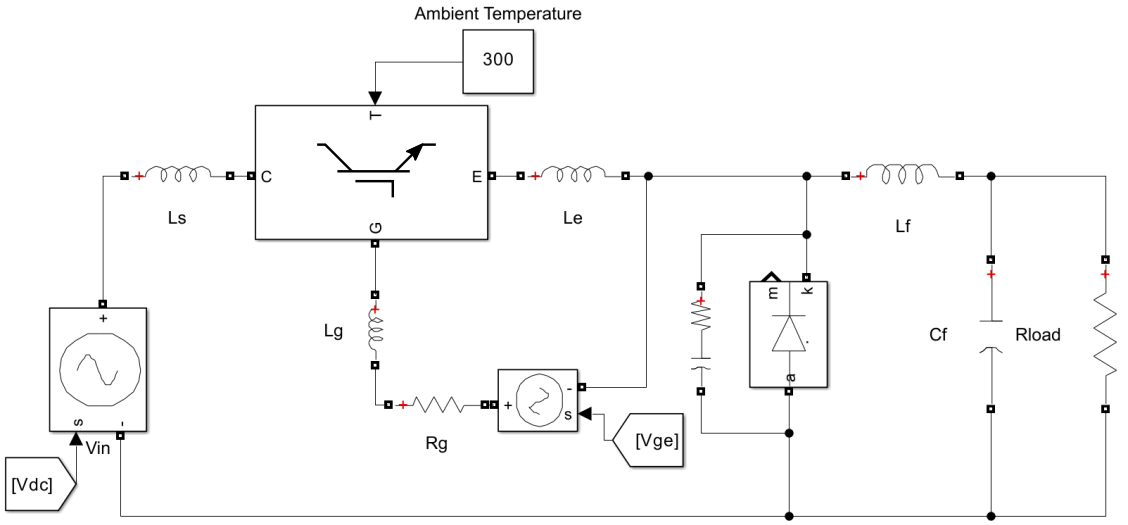


Figure 9.11: Simulink implementation of a buck converter using the proposed model as the switching device.

Table 9.2: Buck converter requirements

Input Voltage	**14 kV**
Output Voltage	**7 kV**
Output Current	**30 A**
Output Voltage Ripple	**100** V_{P-P}
Switching Frequency	**2 kHz**
Converter Operation	**CCM**

Finally, Fig. 9.13 shows some optimisation curves that can be identified with simulations and used to optimise the converter's efficiency. For example, Fig. 9.13(a) shows the impact of the device's active area on the static and dynamic losses. In contrast to MOSFETs, where there is a linear relationship between the static losses and the active area, in IGBTs, the situation is different due to the non-linear $I_c - V_{ce}$ characteristics. Additionally, due to the current dependence on equivalent parasitic capacitances of the IGBT, the switching losses cannot remain unchanged by simply scaling the gate resistance with the active area. As a result, an optimum total semiconductor active area can be found for a particular application, and a further increase in the active area leads to increased total losses. Finally, Fig. 9.13(b) demonstrates the non-linear relationship between the gate resistance and the switching losses of the IGBT.

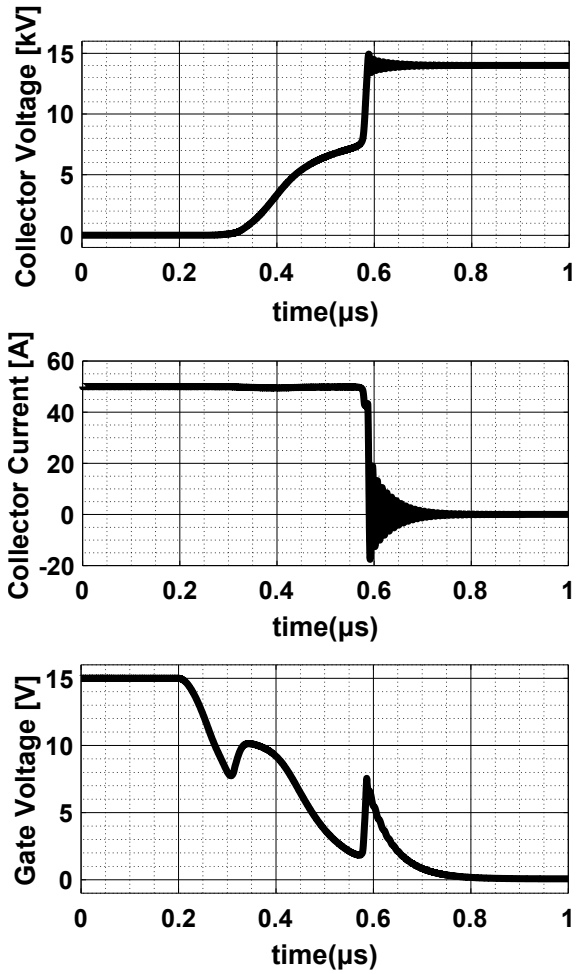


Figure 9.12: IGBT waveforms during the buck converter operation.

9.5 Concluding remarks

This chapter presented a new modelling method for SiC IGBTs. By using voltage and current-dependent capacitances and an equivalent circuit similar to that of unipolar devices, the static and dynamic performance of SiC IGBTs can be accurately predicted for a wide range of application conditions. Additionally, a buck converter topology with layout parasitics was simulated to demonstrate the model's suitability for topology-level simulations and to capture transient phenomena such as high dV/dt, oscillations and gate voltage spikes. The proposed model proved fast, robust and accurate and can be a valuable tool for virtual prototyping of future SiC IGBT-based high voltage applications.

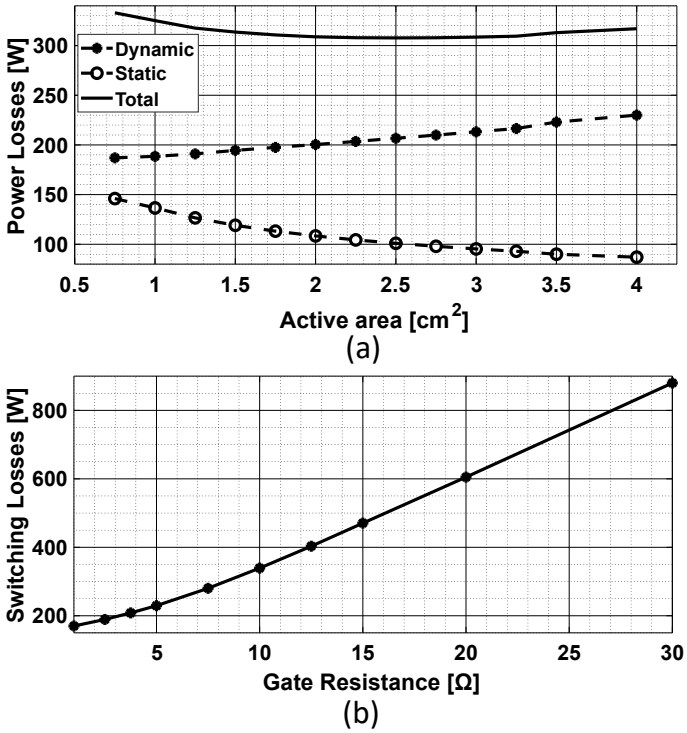


Figure 9.13: Optimisation curves between (a) active area and power losses, (b) gate resistance and switching losses.

Chapter 10

Conclusions and Future Work

This chapter provides the conclusions of the research conducted in this thesis and reports on future research directions.

10.1 Conclusions

The conducted research work presented in this thesis has focused on SiC IGBT modelling and characterisation. Initially, a TCAD model of a SiC IGBT has been developed and validated using experimental data from the SiC material properties and IGBT behaviour. The modelled device proved to be accurate in predicting the static and dynamic characteristics of demonstrated IGBTs, allowing the characterisation of the device under a wide range of application conditions and understanding the impact of device-, process- and circuit-dependent parameters on the IGBT's performance and ruggedness (Chapter 4).

Several challenges and concerns about the mass adoption of SiC IGBT were analysed in detail, the root causes of different failure mechanisms were identified, and the device structure was optimised to address them. One of those failure mecha-

nisms is the false turn-on of the IGBT caused by the extremely high dV/dt rates occurring during the switching transients, which can lead to increased switching losses or even short-circuiting of the device. By running extensive TCAD simulations (Chapter 5), the false turn-on ruggedness of the SiC IGBT was shown to improve by optimising the emitter side of the device to increase the gate-to-emitter capacitance. The improved ruggedness was achieved by co-adjusting several structural and process-dependent parameters, such as the gate oxide thickness and the p-well doping profile, without sacrificing the device's efficiency.

Additionally, the short circuit behaviour of SiC IGBTs was studied for the first time using validated TCAD simulations in Chapter 6. The simulation results showed the trade-off relationship between the on-state voltage drop and Short Circuit Withstand Time (SCWT), and the failure mechanisms were identified. Similarly to silicon IGBT, the SiC IGBT can fail under short circuit conditions due to the parasitic thyristor latch-up. Additionally, the SiC IGBT can fail even for several microseconds after detecting a short circuit event and turning it off because of the high leakage current and increased lattice temperature. In addition, unlike silicon IGBTs, the temperature within the semiconductor can reach as high as 1500 K. This will cause premature failure when aluminium is used as the metallisation material as the contact temperature exceeds its eutectic temperature, necessitating the need for considering the usage of other metalisation materials to exploit the full potential of SiC IGBT. Finally, a sensitivity analysis presented the impact of several device and circuit parameters on the short circuit behaviour and suggested the best ways to optimise the ruggedness without sacrificing efficiency.

Furthermore, a novel IGBT structure was proposed in Chapter 7, being able to mitigate EMI-related issues by controlling the high dV/dt rates. The proposed structure uses a stepped doping concentration in the drift and buffer layers to prevent the electric field from punching through to the buffer layer during the inductive turn-off, thus reducing the high dV/dt. Additionally, this structure decouples the impact of

the drift and buffer layer parameters on the on-state losses, switching losses, breakdown voltage and maximum dV/dt, offering a straightforward approach for device structure optimisation. Apart from the above, the proposed structure can further improve the false turn-on robustness and short circuit behaviour without sacrificing the device's efficiency.

Moreover, Chapter 8 presented a comprehensive examination of the impact of the optimisation strategies presented in chapters 5-7 on the performance and ruggedness of SiC IGBTs rated at 10-40 kV. This chapter summarised the expected performance and ruggedness of devices rated at such a wide voltage range, highlighting the most efficient methods of optimising them according to the voltage rating.

Last but not least, the first behavioural model for SiC IGBT was proposed in Chapter 9, and its ability to accurately predict the device's behaviour was demonstrated. In contrast to any other SiC IGBT model that has been proposed in the literature, this model does not require the knowledge of structural and process-dependent parameters, making it attractive for device manufacturers because they can release an accurate model without disclosing structural device information. Additionally, the easy parameter fitting method using only electrical characteristics of the device operation under static and dynamic conditions was presented, and its fast performance and good convergence were demonstrated in a topology-level simulation.

10.2 Future Work

There are five directions that the future work can be guided:

- **On the device optimisation level**. Additional single event and long-term degradation failure phenomena can be studied, such as the Unclamped Inductive Switching (UIS) condition, bipolar degradation or shifting in charac-

teristics during the pulsed operation or stressing the device beyond the safe operational area. Furthermore, as presented in this thesis, power electronic devices consist of many parallel cells to form a die or paralleled dies to form a power module. As a result, the parallel operation in both cell and die level is very important to be studied. Finally, since SiC IGBTs operate at voltages that exceed the currently available capabilities of the packaging solutions, more research is required towards new packaging approaches and materials to meet the high voltage isolation and heat extraction requirements. Instrumental to this future work will be using the validated TCAD models and fast behavioural models presented in this thesis.

- **On the converter and system level**. The predicted behaviour and the behavioural model of SiC IGBTs can be used as input to the converter and system-level applications to demonstrate the performance and ruggedness improvement that those devices can bring. This is essential in creating demand and driving the commercialisation of every emerging power semiconductor device. Typical applications that can take advantage of using SiC IGBTs are green energy generation (PV or wind power) and HVDC transmission.

- **On the fabrication optimisation and experimental level verification**. The fabrication process of SiC IGBTs should be optimised to achieve higher manufacturing yields and larger area devices. This will allow the proposed device structures to be assessed experimentally and the IGBTs to be used in future converter-level applications.

- **On the modelling level**. The proposed behavioural model can predict the static and dynamic operation of the SiC IGBT. Extending this model to be able to predict the device's behaviour under operational conditions beyond the safe operational region (such as under short circuit conditions) will be a useful addition that does not exist in currently available behavioural models of power semiconductor devices. Additionally, replacing the lookup table

implementation of the parasitic capacitances modelling described in Chapter 9 with functions will make the model compatible with other circuit simulators, like LTSPICE.

Furthermore, the validation process of the TCAD modelling requires several iterations of virtual fabrication, characterisation under various operational conditions, evaluation of the device behaviour and modifying several parameters to achieve the best convergence between the simulation and experimental data. The same device characteristics under various operational conditions (either from real or virtually fabricated devices) are also used for the behavioural models to find the modelling function parameters that achieve the best curve fitting. These two problems might potentially be tackled using AI in future works to allow for much faster development of TCAD and behavioural models.

- **On the applicability of the current research findings to silicon IGBTs**. The proposed device structure, featuring a 4-layer stepped doping profile on the drift and buffer layer, can also be used for silicon IGBTs to control the current tail during the inductive turn-off process and short circuit behaviour. Additionally, in contrast to silicon carbide where deep diffusion is not possible and this structure can be implemented by controlling the doping concentration during the buffer and drift region epitaxy, the ease of dopants diffusion in silicon allows for generalisation of this structure where there is a continuously variable doping density for the HDB, LDB, HDD and LDD regions.

  Finally, since the operational principles of silicon and SiC IGBTs are identical, the applicability of the proposed behavioural model on silicon IGBT can be studied to develop a unified behavioural model for Si/SiC IGBTs, which also lucks from the current literature.

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Appendices

Appendix A

Sentaurus process script

```
## Simulation Initialization - substrate definition
region SiliconCarbide xlo= top xhi= bottom ylo= left yhi= right substrate
init field= @Sub_Species@ concentration= @Sub_Doping@ miscut.tilt= 4.0
miscut.toward= {1 1 0}

### Epi 1: Nitrogen buffer layer
deposit SiliconCarbide anisotropic thickness= @Nbuff_Thickness@
species= Nitrogen concentration= @Nbuff_Doping@
diffuse temperature=1600 time=360

### Epi 2: Nitrogen drift layer
deposit SiliconCarbide anisotropic thickness= @Ndrift_Thickness@
species= Nitrogen concentration= @Ndrift_Doping@
diffuse temperature=1600 time=360

### Epi 3: Nitrogen JFET layer
deposit SiliconCarbide anisotropic thickness= @NJFET_Thickness@
species= Nitrogen concentration= @NJFET_Doping@
diffuse temperature=1600 time=360
```

```
## P-Body implantation
implant Aluminum dose= 8.30e11 energy= 8 tilt= 0.0
implant Aluminum dose= 1.59e12 energy= 20 tilt= 0.0
implant Aluminum dose= 2.91e12 energy= 50 tilt= 0.0
implant Aluminum dose= 4.90e12 energy= 100 tilt= 0.0
implant Aluminum dose= 7.49e12 energy= 170 tilt= 0.0
implant Aluminum dose= 3.4e12 energy= 300 tilt= 0.0
implant Aluminum dose= 3.8e12 energy= 410 tilt= 0.0
implant Aluminum dose= 1.8e13 energy= 535 tilt= 0.0 smooth

## ENHANCED P-Body implantation at the source contact sides
implant Aluminum dose= 1e14 energy= 50 tilt= 0.0
implant Aluminum dose= 2e14 energy= 100 tilt= 0.0
implant Aluminum dose= 3e14 energy= 150 tilt= 0.0 smooth

## N+ Source implantation
implant Nitrogen dose= 1e15 energy= 30 tilt= 0.0
implant Nitrogen dose= 1.2e15 energy= 70 tilt= 0.0
implant Nitrogen dose= 2e15 energy= 120 tilt= 0.0 smooth

## High Temperature Annealing
diffuse time=@Diffusion_time@<min> temperature=@Diffusion_temperature@<C>

## Gate oxidation -- THERMAL oxidation
diffuse time= @Oxidation_time@<min> temp= 1300<C> O2

## Poly gate formation
deposit PolySilicon anisotropic mask= POLYsi_gate thickness= 0.2

## ILD deposition
deposit Oxide thickness= @tox2@ isotropic
```

```
## Etch source contact
etch Oxide thickness= $etch_th anisotropic mask= contact

## Aluminum deposition for the source contact
deposit Aluminum thickness= 1.0 isotropic
```

Appendix B

Sentaurus device scripts

B.1 Physics Section

```
Physics {
  Fermi
  AreaFactor = !(puts $AREAF )!
  Recombination (
    SRH(DopingDep TempDependence)
    Auger
    Avalanche(OkutoCrowell )
    ConstantCarrierGeneration (value = @CarrierBG@)
  )
  Aniso (
    eMobilityFactor (Total) = 0.83
    hMobilityFactor (Total) = 1.00
    Avalanche
    direction(SimulationSystem) = (1,0,0)
  )
  Mobility (
    DopingDependence
```

```
    HighFieldSaturation
    ThinLayer(IALMOB)
    Enormal(Lombardi Coulomb2D InterfaceCharge
      NegInterfaceCharge(SurfaceName="S1")
      PosInterfaceCharge(SurfaceName="S1")
    )
  CarrierCarrierScattering(ConwellWeisskopf)
  )
  IncompleteIonization
  EffectiveIntrinsicDensity ( oldSlotboom NoFermi )
  Temperature = @Device_Temp@
  Thermodynamic}
  Physics(MaterialInterface= "SiliconCarbide/Oxide") {
  Traps ((FixedCharge Conc=@Charge@)
    (eNeutral uniform Conc=@Interface_traps@ fromCondBand EnergyMid=0.05
    EnergySig=0.1 eXsection=1e-10 hXsection=1e-10))}
Math {
..
  Surface "S1" (MaterialInterface="SiliconCarbide/Oxide")
..
}
```

B.2 Parameter File

```
    !(set Tau_h "[expr (@Tau_e@/5)]"  )!
!(set e_mob_per "[expr (@e_mob@/0.83)]" )!
!( set Vsat0_h_per "[expr (@Vsat0_h@/1.16)]" )!
!( set Vsat0_e_per "[expr (@Vsat0_e@/1.16)]" )!
Material = "SiliconCarbide"
{
Epsilon #perp. to c-axis
```

```
{epsilon = 9.76}

Epsilon_aniso #parallel to c-axis
{epsilon = 10.32}
Kappa #perp. to c-axis
{ Formula = 0
1/kappa = 2.5e-3
1/kappa_b = 2.75e-4
1/kappa_c = 1.3e-6    }
Kappa_aniso #parallel to c-axis
{ Formula = 0
1/kappa = -0.1882
1/kappa_b = 1.637e-3
1/kappa_c = -2.711e-20 }
LatticeHeatCapacity
{ cv  = -2.139
cv_b  = 2.242e-2
cv_c  = -3.130e-5
cv_d  = 1.546e-8 }
Bandgap
{ Chi0  = 3.24
Bgn2Chi  = 0.5
Eg0  = 3.285
alpha  = 0.033
beta  = 1.0e5 }
Slotboom
{ Nref = 1.e+17
Ebgn = 0.009 }
eDOSMass
{ Formula = 1
a = 10.2429
```

```
ml = 10.2429
mm = -33.049
Nc300 = 1.9150e19 }
hDOSMass
{ Formula = 1
a = 1
b = 6.92e-2
c = 0.
d = 0.
e = 1.88e-6
f = 0.
g = 6.58e-4
h = 0.
i = 4.32e-7
mm = 0.
Nv300 = 1.0752e20 }
ConstantMobility
{ mumax = @e_mob@,@h_mob@
Exponent = @exponent@,@exponent@ }
ConstantMobility_aniso
{ mumax = !(puts $e_mob_per )!,@h_mob@
Exponent = @exponent@,@exponent@ }
DopingDependence
{ formula = 1,1
mumin1 = 40,15.9
mumin2 = 40,15.9
Pc = 0,0
Cr = 1.94e17,1.5e18
alpha = @alpha_e@,@alpha_h@
mu1 = 0,0
Cs = 3.43e20,6.1000e20
```

```
beta = 2,2  }
EnormalDependence
{ B = 1e6,9.92e06
C = 280,2.95e03
N0 = 1,1
lambda = 0.125,0.0317
k = 1,1
delta = 5.82e14,2.0546e14
A = 2,2
alpha = 0.0,0.0
N1 = 1,1
nu = 1,1
eta = 5.82e30,2.055e+30
l_crit = 1.0e-06,1.0e-06 }
HighFieldDependence
{ beta0 = 1.2,1.2
betaexp = 1,1
Vsat_Formula = 1,1
vsat0 = @Vsat0_e@,@Vsat0_h@
vsatexp = @Vsat_exp@,@Vsat_exp@ }
HighFieldDependence_aniso
{ beta0 = 1.2,1.2
betaexp = 1,1
Vsat_Formula = 1,1
vsat0 = !(puts $Vsat0_e_per )!,!(puts $Vsat0_h_per )!
vsatexp = @Vsat_exp@,@Vsat_exp@ }
Scharfetter
{ taumin = 0.0,0.0
taumax = @Tau_e@,!(puts $Tau_h )!
Nref = 3.0e17,3.0e17 # [94Ruf]
gamma = @gama@,@gama@ # [94Ruf]
```

```
Talpha = @T_alpha@,@T_alpha@
Etrap = 0.0000e+00 }
Auger
{ A = 5e-31,2e-31
#A = 3e-29,3e-29
B = 0.0,0.0
C = 0.0,0.0
H = 0.0,0.0
N0 = 1.0e+18,1.0e+18 }
OkutoCrowell
{ a = 0.1,4.828e6
b = 6.346e6,1.334e7
c = 0.0,0.0
d = 0.0,0.0
gamma = 1,0.0
delta = 2,1.0 }
Ionization
{ Species ("NitrogenConcentration") {
type  =  donor
E_0 = 0.0709
alpha = 3.3800e-08
g = 2.0
Xsec = 1.0000e-12 }
Species ("AluminumConcentration") {
type  =  acceptor
E_0 = 0.265
alpha = 3.60e-08
g = @gA@
Xsec = 1.0000e-12 }}}
```

Appendix C

SiC IGBT behavioural model implementation

The behavioral SiC IGBT model presented in Chapter 9 implemented in Simulink in order to assess its accuracy and speed and be used in converter topologies. As shown in Fig. C.1, two dependent current sources are used to model the static and the recombination characteristics of the IGBT, while two dependent capacitances (C_{gc} and C_{ce}) and one constant capacitance (C_{ge}) to model the dynamic characteristics. This figure also shows the three electrical terminals, namely the gate, collector and emitter.

The dependent capacitance component has two electrical terminals and one control terminal and is implemented using a controlled current source as shown in Fig. C.2, where the current is calculated according to Eq. C.1. As explained in Chapter 9, the C_{gc} and C_{ce} capacitances are voltage-, current- and temperature dependent and are implemented using the 3D lookup tables shown in Fig. C.3.

$$I_c = C \cdot \frac{dV_c}{dt} \tag{C.1}$$

The good static modeling accuracy of the SiC IGBT was achieved by selecting the parameters a,b,c,d of Eq. 9.4 to fit the experimental or TCAD simulated behaviour

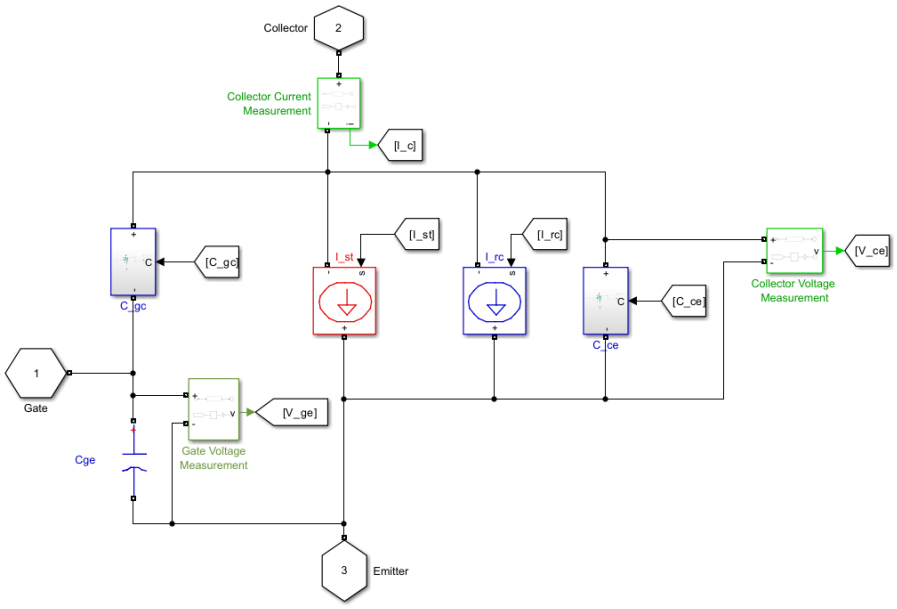


Figure C.1: SiC IGBT model implementation in Simulink.

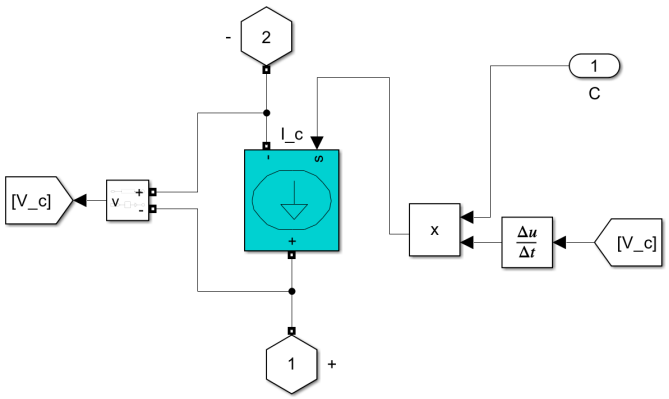


Figure C.2: Dependent capacitance implementation in Simulink.

under different gate voltages and temperatures. Figure C.4 shows the obtained a,b,c and d parameters from the curve fitting process and how they are modelled using the functions of Eq. 9.2 and 9.5. Finally, Fig. C.5 shows the simulink implimentation of the controlled current source I_{st} using a simple matlab function.

Similarly, the Matlab function implementation of the I_{rc} current source is shown in Fig. C.6. In this case, the collector current derivative is used to detect the current falling period during the turn-off switching transient, and the two different current falling rates are modelled with two different RC time constants. Finally, Fig. C.7 shows the buck converter configuration, in which the behavioural model is connected with components from the Simscape library of Simulink to evaluate the

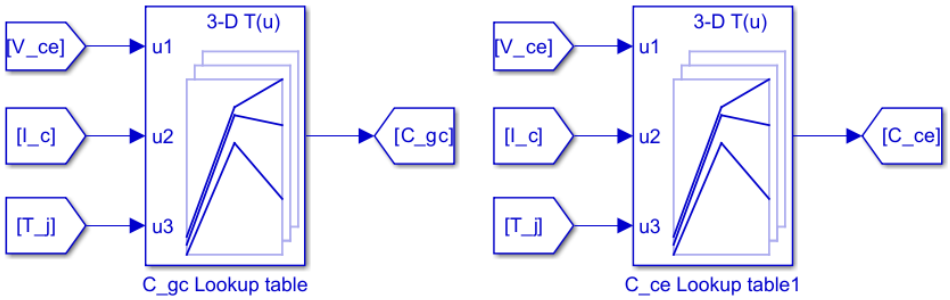


Figure C.3: 3D capacitances lookup tables.

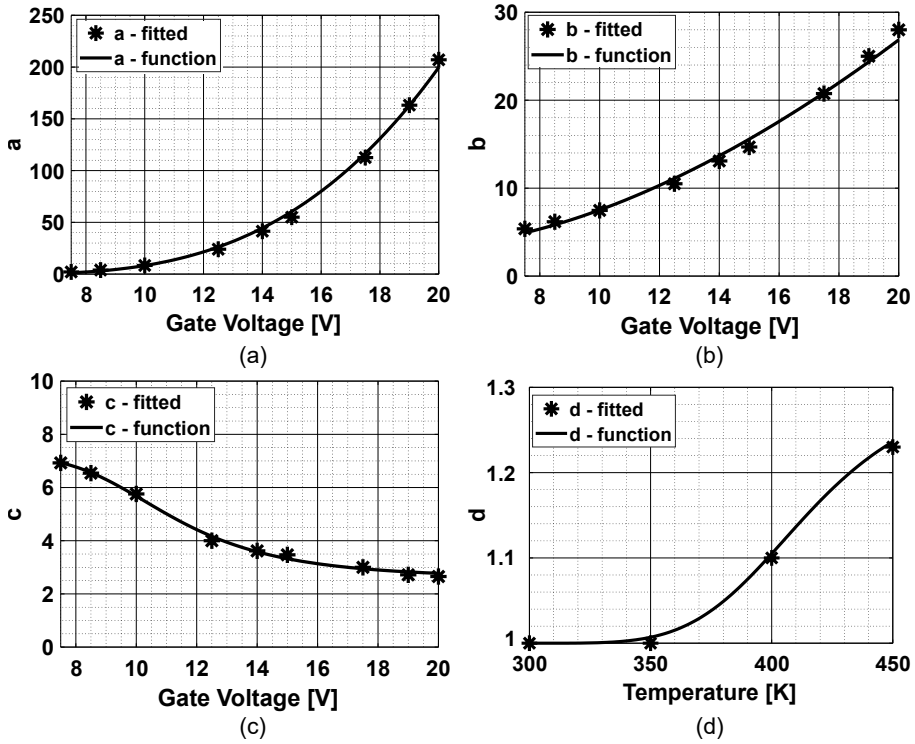
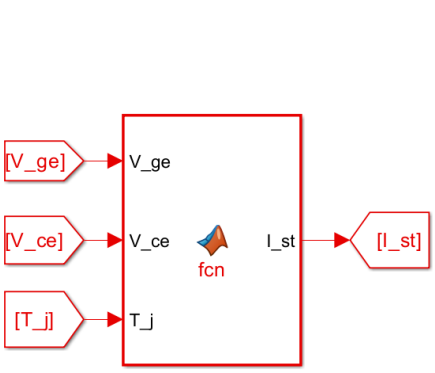


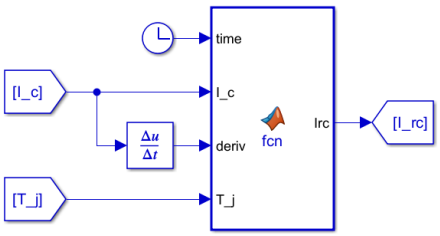
Figure C.4: Comparison between the obtained parameters from curve fitting and the modelled functions.

convergence and speed of the developed model in circuit-level simulations.




```
function I_st  = fcn(V_ge, V_ce, T_j)
%% Modeling parametrs
    Vth_298 = 4.5;
    Vth_448 = 3.93;
    s1a     = -21200.0;
    s2a     = 70.1627;
    s3a     = 3.0832;
    s4a     = 21200.0;
    s1b     = 7027.2;
    s2b     = 446.253;
    s3b     = -1.697;
    s4b     = 3.4751;
    s1c     = 4.5989;
    s2c     = 6.7377;
    s3c     = 3.6422;
    s4c     = 2.562;
    s1d     = -0.31;
    s2d     = 118;
    s3d     = 4.6;
    s4d     = 1.31;
%% Functions implementation
    Vth     = 4.5+(T_j-298)*(Vth_448-Vth_298)/(448-298);
    if (V_ge <= Vth)
        I_st     = 0;
    else
        a       = s4a + s1a/(1.0+((V_ge-Vth)/s2a)^s3a);
        b       = s4b + s1b/(1.0+((V_ge-Vth)/s2b)^s3b);
        c       = s4c + s1c/(1.0+((V_ge-Vth)/s2c)^s3c);
        d       = s4d + s1d/(1.0+((T_j-298)/s2d)^s3d);
        I_st     = (a - a/(1+(V_ce/(b*d))^c));
    end
```

Figure C.5: Implementation of the controlled current source I_{st} for the SiC IGBT static operation.




```
function Irc  = fcn(time,I_c,deriv,T_j)
%% Modeling parameters
    C = 1e-9;
    R_298K = 100;
    R_448K = 200;
%% Function implementation
    R = R_298K + (T_j- 298)*(R_448K - R_298K)/150;
    if (Current_tail == 0)
        if ((deriv <= -1e6)&&(Irc1==0))
            Current_tail = 1;
            t_start = time;
            Irc=0.3*I_temp*(exp(-((time-t_start)/(R*C))))+0.7*I_temp*(exp(-(500*(time-t_start)/(R*C))));
            Irc1=Irc;
        else
            Irc=0;
            Irc1=Irc;
            I_temp = I_c;
        end
    elseif (Current_tail == 1)
        if ((time-t_start)>(5*R*C))
            Current_tail = 2;
            Irc=0;
            Irc1=Irc;
        else
            Irc=0.3*I_temp*(exp(-((time-t_start)/(R*C))))+0.7*I_temp*(exp(-(500*(time-t_start)/(R*C))));
            Irc1=Irc;
        end
    else
        if ((deriv >= 1e6))
            Current_tail = 0;
            I_temp = 0;
        end
        Irc=0;
        Irc1=Irc;
    end
```

Figure C.6: Implementation of the controlled current source I_{rc} for the SiC IGBT current tail.

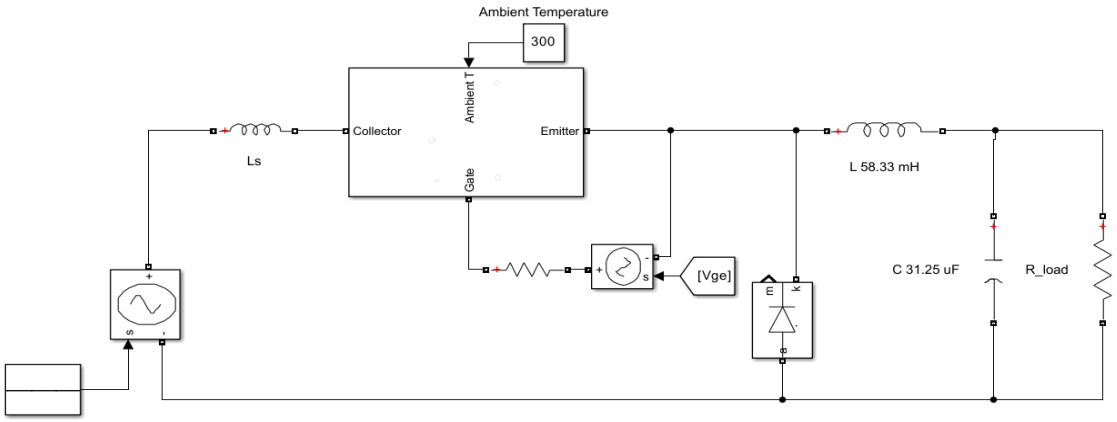


Figure C.7: Buck converter simulation using the developed behavioural model and components from the Simscape library of Simulink.