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Modular Multilevel DC-DC Converters for HVDC Grid Interconnection

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Abstract

Since the introduction of voltage source converters, VSCs, which provide bidirectional power flow without reversing the DC voltage, high voltage direct current grids, HVDC girds, are becoming interest solution for expanding the existed ac grids. HVDC systems are preferred over the high voltage alternative current, HVAC, for long distance high power transmission due to lower total investment, lower power losses and HVDCs are technically and environmental superior. Additionally, they have been chosen as solutions for interconnecting off-grid communities, asynchronous AC grids and transmitting power from offshore winds. Because of the HVDC technology advantages and the absence of operational voltage standards, many point to point HVDC links have been established at different voltage levels. Developing these point to point HVDC systems to HVDC grids will require high voltage and high power DC-DC converters to interconnect different voltage levels and provide isolation.

In the earlier of the last decade, modular multilevel converter, MMC, was introduced and this led to a bread of non isolated and isolated modular multilevel DC-DC converters, MMC-DC-DC, for HVDC grids. In modular multilevel topologies, half bridge submodule blocks, SM, are assembled to a chain-link which produces desired voltage rating. However, the number of the required submodule increases as the voltage rating increase. Recently, modular multilevel DC-DC converters with trapezoidal operation (quasi two-level operation) were introduced to reduce the size of the submodlue capacitor and accordingly the footprint, weight and cost of SM are reduced. In comparison to dual active bridge converters (DAB), trapezoidal operation has also reduced $\frac{dv}{dt}$ stress across the transformer in isolated modular multilevel DC-DC converters whereas the reduction in $\frac{dv}{dt}$ stress is limited.

In the first part of this work, a trapezoidal modulation of modular multilevel DC-DC converter is investigated and a modified trapezoidal operation is proposed. Additionally, a control schemes that support the proposed operation of converter under transient conditions are demonstrated. This work also investigates the limitation of transformer $\frac{dv}{dt}$ and semiconductor device utilisation.

The second part of this work presents a new modular multilevel series chain-link DC-DC converter, SCC-DC-DC, which requires only 33% SMs and lower device current rating as compared to modular multilevel DC-DC converter topologies. In the proposed topology many single phase transformers are used instead of one three phase transformer and this permits the generation of voltage with controllable $\frac{dv}{dt}$ across the transformer. Furthermore, the structure of the topology helps to operate the converter at higher fundamental frequency which reduces the overall converter footprint.

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List of Publications

1. Saleh, B.M., Costabeber, A., Watson, A., Tardelli, F. and Clare, J., 2019, September. A New Capacitor Voltage Balancing Method for Trapezoidal Operation of Modular Multilevel DC-DC Converters. In 2019 21st European Conference on Power Electronics and Applications (EPE'19 ECCE Europe) (pp. P-1). IEEE.

2. Saleh, B.M., Costabeber, A., Watson, A.J. and Clare, J.C., 2020, November. A Series Chain-Link Modular Multilevel DC-DC Converter For High Voltage and High Power Applications. In 2020 IEEE 21st Workshop on Control and Modeling for Power Electronics (COMPEL) (pp. 1-6). IEEE

3. Saleh, B.S., Costabeber, A., Watson, A., Tardelli, F. and Clare, J., 2020, December. AN ENERGY CONTROL METHOD FOR MODULAR MULTILEVEL DC-DC CONVERTERS OPERATING WITH TRAPEZOIDAL WAVEFORMS. In The 10th International Conference on Power Electronics, Machines and Drives (PEMD 2020) (Vol. 2020, pp. 158-163). IET

4. Saleh, B.M., Merlet, F.D., Costabeber, A., Watson, A.J. and Clare, J.C., 2021, October. Trapezoidal operation of modular multilevel DC-DC converter for HVDC interconnections. In IECON 2021–47th Annual Conference of the IEEE Industrial Electronics Society (pp. 1-6). IEEE

List of Terms

AAC	Alternative Arm Converter
AAC-DC-DC	Alternative Arm DC-DC Converter
C_{bP}	Primary Blocking Capacitance
C_{bS}	Secondary Blocking Capacitance
C_b	Per Phase Effective Blocking Capacitance
CSC	Current Source Converter
CTB	Controlled Transition Bridge
C_{eqP}	Primary Effective Capacitance Per Chain-Link When All SMs are Inserted
C_{gP}	Primary Effective Capacitance Per Voltage Level
C_{SM}	Sub-module Capacitance
C_{SMP}	Primary Sub-module Capacitance
C_{SMS}	Secondary Sub-module Capacitance
DAB	Dual Active Bridge
E_{ch}	Chain-Link Stored Energy
E_{LP}	Stored Energy in Primary Arm Inductor
E_{LS}	Stored Energy in Secondary Arm Inductor
E_T	Total Stored Energy

E_{CL}	Tank Stored Energy
FB	Full-bridge
f_o	Fundamental Frequency
f_r	Resonant Frequency
f_{sort}	Sorting Frequency
f_{sw}	Switching Frequency
g_{UAi}	SM Gate Signal for Upper Arm of Phase A, $i = 0, 1, 2, ..., N_{SM} - 1$
HB	Half-bridge
H_C	Capacitance Constant
H_{CMMC}	MMC-DC-DC Converter Capacitance Constant
$H_{CMTrMMC}$	MTrMMC-DC-DC Converter Capacitance Constant
H_{CTrMMC}	TrMMC-DC-DC Converter Capacitance Constant
H_{CTrSCC}	TrSCC-DC-DC Converter Capacitance Constant
H_b	Base Capacitance Constant
HTAC	Hybrid Transition Arm Converter
HVAC	High Voltage Alternating Current
HVDC	High Voltage Direct Current
i_{ac}	Per phase AC Link Current
I_{ChP}	Primary Chian-Link Current
I_{ChS}	Secondary Chian-Link Current
$\hat{I_{ChP}}$	Peak of Primary Chian-Link (Arm) Current
I_{DC}	DC Link Current

i_L	Lower Arm Current
i_U	Upper Arm Current
IGBT	Insulated Gate Bipolar Transistor
IGCT	Insulated Gate Commutated Thyristor
K_f	Frequency Factor
LCC	Line Commutated Converter
L_{dc}	DC Inductance
L_{eq}	Effective Per Phase Inductance
L_P	Primary Arm Inductance
L_S	Secondary Arm Inductance
L_{k_i}	Per Phase Effective Tank Inductance
L_{kP}	Primary Tank Inductance
L_{kS}	Secondary Tank Inductance
L_k	Leakage Inductance
MF	Medium Frequency
m_p	Primary Modulation Index
m_s	Secondary Modulation Index
MMC	Modular Multilevel Converter
MMC-DC-DC	Modular Multilevel DC-DC
MTAC	Modular Transition Arm Converter
MTrMMC-DC-DC	Modified Trapezoidal Operation of Modular Multilevel DC-DC
n	Transformer Turns Ratio

N_{arm}	Number of Arms
N_L	Number of Sub-module Per Voltage Level
N_{on}	Number of Inserted SMs Per Chain-Link
N_{off}	Number of Bypassed SMs Per Chain-Link
N_{phase}	Number of Phases
N_{SM_P}	Number of SMs per Primary Chain-Link
N_{SM_S}	Number of SMs per Secondary Chain-Link
N_{SM_T}	Total Number of SMs
N_{st}	Number of Voltage Level
P_{av}	Average Power
P_{Ch}	Chain-Link Power
P_{Con}	Conduction Power Loss of a Chain-Link
P_{sw}	Switching Power Loss of a Chain-Link
P_r	Rated Power
Q2L	Quasi Two Level
R_{dc}	DC resistance
R_P	Winding resistance of the primary arm inductor
R_S	Winding resistance of the secondary arm inductor
SM	Sub-modules
SCC	Series Chain-link DC-AC Converter
SCC-DC-DC	Series Chain-link DC-DC Converter
STAC	Modular Shunt Transition Arm Converter
STATCOM	Static Synchronous Compensator

T_d	Dwell Time
T_L	Total Power Loss
T_{ph}	Time Difference Between Phases
T_t	Transition Time
TAC	Transition Arm Converter
TrCTB-DC-DC	Trapezoidal Operation of Controlled Transition Bridge DC-DC Converter
TrMMC-DC-DC	Trapezoidal Operation of Modular Multilevel DC-DC
TrSCC-DC-DC	Trapezoidal Operation of Series Chain-link DC-DC Converter
VA	Devices Voltage and Current Product
VA_{MMC}	MMC-DC-DC Device Voltage and Current Product
VA_{MTrMMC}	MTrMMC-DC-DC Devices Voltage and Current Product
VA_{TrSCC}	TrSCC-DC-DC Devices Voltage and Current Product
VA_{TrMMC}	TrMMC-DC-DC Devices Voltage and Current Product
VSC	Voltage Source Converter
V_{ch}	Chain-Link Voltage
$\hat{V_{ch}}$	Peak of Chain-Link Voltage
$\hat{v_{Cb}}$	Peak Voltage of Per Phase Effective Blocking Capacitor
V_{DC}	DC Link Voltage
V_{DCP}	Primary DC Link Voltage
V_{DCS}	Secondary DC Link Voltage
V_L	Lower Chain-Link (Arm) Voltage
V_{PT_P}	Per Phase Primary Transformer AC Voltage

V_{SM}	Sub-module Voltage
V_{SM_P}	Primary Sub-module Voltage
V_{SM_S}	Secondary Sub-module Voltage
V_{ST_S}	Per Phase Secondary Transformer AC Voltage
v_T	Tank Voltage
V_U	Upper Chain-Link (Arm) Voltage
Z_b	Impedance Factor
ω	Angular Frequency
ω_r	Tank Angular Resonant Frequency
Δe_{Ch}	Chain-Link Energy Variation
ρ_g	DC Voltage Gain
θ	Dwell Angle Between Voltage Level
δ_{pp}	Per Unit Peak-to-Peak SM Capacitor Voltage fluctuation
ϕP	Primary Phases, A, B, C
ϕS	Secondary Phases, U, V, W
ΔQ_{UAi}	SM Capacitor Net Charge for Upper Arm of Phase A, $i = 0, 1, 2, ..., N_{SM} - 1$
φ	Voltage Angle Between Primary and Secondary Chain-Link Voltage

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Chapter 1

Introduction

1.1 Motivations for the research project

High Voltage Direct Current (HVDC) transmission systems are now considered a viable option for the expansion of the modern electricity grid. This is a result of the advantages that HVDC approaches to electrical transmission have in comparison to HVAC transmission as well as recent advances in the development of HVDC grids.

Unfortunately, as a result of the differences between HVDC links with respect to elements such as voltage, for example, the development of HVDC grids has still been plagued with technical challenges which were solved in AC based grids decades ago. Although, organisations such as CIGRE, the IEEE, and the IEC are developing guidelines to standardize HVDC grids, many non standardised point to point HVDC links have been planned and commissioned [14, 15]. The future development of HVDC grids will include the connection of existing HVDC links which may have different voltage levels, HVDC technology and grounding schemes. As a result, the development of HVDC grids will require DC-DC power converters (or similar technology) which will provide DC voltage scaling and regulation. In addition, the application of DC-DC power converters to HVDC grids can also provide fault isolation capabilities, bidirectional power flow and interfaces between differ-

ent HVDC transmission schemes such as bipolar and monopolar links [16, 17].

The recognised importance of the DC-DC power converters in the HVDC grids has led to a significant increase in research effort in this area, considering the further development of existing or the invention of new approaches to DC-DC conversion. Modular multilevel converter based DC-DC converter topologies are a very promising topology for HVDC interconnection. Recently, a family of modular multilevel DC-DC converters utilising trapezoidal waveform operating mode were proposed, where comparative elements include a reduction in energy storage, losses and overall footprint when compared to conventional operation of Modular multilevel based DC-DC converters. However, there are several limitations and implementation issue with the trapezoidal operation of the modular multilevel DC-DC converter (TrMMC-DC-DC):

- The requirement for a high number of half-bridge submodules (high quantities of gate drive circuits, submodule capacitors, power supplies, etc) which makes the control more complex

- The requirement of sorting the submodules capacitor at high frequency, up to $30kHz$, which makes the implementation of the control very challenging

- Voltage stress, including high $\frac{dv}{dt}$, applied to the transformer of the DC-DC converter can have an impact on insulation lifetime. As a result, the operation of the converter at a fundamental frequency greater than 500Hz, with high power density, is difficult.

- High overall semiconductor device ratings (voltage and current requirements) which impacts the cost semiconductors used in the system

- Poor submodule devices utilisation which impacts on the losses and consequently the cooling system requirements

- Semiconductor power losses

The main motivation of the work presented in this thesis is to develop a modular multilevel DC-DC converter that provides low dv/dt stress on the transformer insulation, high fundamental frequency operation (up to a few kHz, to achieve high power density), low energy storage requirements, a low number of submodules to simplify the control, and a low frequency sorting routine for the submodule capacitors in order to make the approach practically viable. The final motivation is to achieve a high submodule device utilisation to evenly distribute semiconductor losses and simplify the cooling system requirements.

1.2 Project objectives

This Ph.D. work is aimed to design a high-voltage (hundreds of kV), high-power (hundreds of MW) bidirectional DC-DC converter for:

- Interconnecting HVDC systems with different voltage levels, different HVDC configurations and different converter topologies
- Segmentation of a large DC grid into the smaller DC protection zones which can improve reliability when faults occur

The main objectives are firstly, to further the research into the trapezoidal operation of the MMC-DC-DC converter which was recently proposed for HVDC interconnection [18]. Secondly, undertake a detailed investigation of a new modular multilevel series chain-link DC-DC converter, SCC-DC-DC, operated with a trapezoidal wave-shaping for HVDC grid interconnection. This new DC-DC power converter design is derived from the recently proposed multilevel series chain-link SCC converter. This converter was originally investigated by researchers at the University of Nottingham for AC/DC conversion in HVDC systems [19].

The outcomes of the following objectives are presented in this thesis:

- The review of existing modular multilevel DC-DC converters suitable for use in HVDC interconnection applications

- The investigation and analysis of the trapezoidal operation of modular multilevel DC-DC converters, identifying the challenges associated with control complexity, high $\frac{dv}{dt}$ insulation stress, high sorting algorithm frequency, poor submodule device utilization, high semiconductor device current ratings and semiconductor power losses

- Development of a modified trapezoidal operation for the MMC-DC-DC converter which reduces the complexity in the practical control implementation by significantly reducing the submodule capacitor sorting frequency requirement, reduces current ratings of the devices and provides better devices utilisation

- An investigation into the relevant control schemes, required to ensure the safe operation of the modified trapezoidal modulation of the modular multilevel DC-DC converter, MTrMMC-DC-DC

- The development of the trapezoidal operation of a series chain-link modular multilevel DC-DC converter (TrSCC-DC-DC) in order to simplify the control implementation by significantly reducing the number of submodules and the sorting frequency of the submodule capacitor voltages. This is achieved whilst improving device utilisation, achieving a higher power density and a reduction in the $\frac{dv}{dt}$ stress across the transformer insulation by conducting the current between the submodule devices, operating at a higher fundamental frequency and increasing the number of the converter phases, respectively.

- The development of any necessary control schemes to ensure safe operation of the TrSCC-DC-DC converter

- A comparative analysis for the TrSCC-DC-DC and the demonstration of any potential advantages of this new modular multilevel DC-DC converter

- The construction of laboratory scale for both MTrMMC-DC-DC and TrSCC-DC-DC prototypes for experimental validation of the proposed converters

1.3 Thesis Structure

This thesis work is organised into the following chapters:

Chapter 2 presents an overview of HVDC transmission, showing the advantages of the HVDC systems in terms of economical, environmental and technical aspects for various applications. It also describing the possible HVDC grid scenarios where DC-DC converters are required.

Chapter 3 describes the high power DC-DC converters that have been proposed in the literature for HVDC grid applications. It mainly focuses on the review of the different operations of the modular multilevel DC-DC converters which are suitable for HVDC interconnection.

In Chapter 4, the newly developed operation of a modular multilevel DC-DC converter named as modified trapezoidal operation of modular multilevel DC-DC converter, MTrMMC-DC-DC, is introduced. The operating principles, mathematical modelling, required semiconductor device ratings and the size of the submodule capacitor are presented. The reduction in the size of the submodule capacitors are given and the increased utilisation of the semiconductor devices for the converter are explained. Furthermore, the control loops required to safely operate the MTrMMC-DC-DC under different operational conditions are developed and described. The required submodule capacitor voltage balancing methods are described and their effects on the balancing process are discussed.

Chapter 5 shows a comprehensive comparison between the MMC-DC-DC converter configurations, TrMMC-DC-DC, MTrMMC-DC-DC and the sinusoidal MMC-DC-DC, in terms of power device utilisation, energy storage requirement, semiconductor current rating, semiconductor power losses and device current stress during DC fault events. The validation of the identified control schemes and the submod-

ule capacitor voltage balancing methods are shown using simulation results for a 400kV(DC-DC)/800MW system with the MTrMMC-DC-DC converter configuration.

In chapter 6 the trapezoidal operation of a resonant modular multilevel series chain-link converter (TrSCC-DC-DC) is described. Three operational methods for the TrSCC-DC-DC are modelled. The design of the resonant tank circuit, converter models and the required control methodology are presented. The requirements for the TrSCC-DC-DC in terms of components specification, power device utilisation, energy storage requirement, semiconductor current rating and transformer $\frac{dv}{dt}$ stress are described.

In chapter 7 Simulation results are presented to validate the proposed operating modes and theoretical calculation in a 400kV(DC-DC)/800MW system. These simulations are implemented using the PLECS simulation environment, by PLEXIM. A technical comparison between the TrSCC-DC-DC operating modes and other isolated modular multilevel DC-DC converters using trapezoidal modulation are also presented in terms of the transformer $\frac{dv}{dt}$ stress, semiconductor power losses, energy storage requirements, the number of SMs and the device *VA* requirement (*VA* influences the cost and area of semiconductor) of the converters. The effect of the chosen operating frequency and its impact on the converter transformer voltage stress, energy storage requirement and overall converter footprint are also considered. In addition, other derived topologies from the TrSCC-DC-DC applicable for high voltage ratios are shown. DC fault performance of the TrSCC-DC-DC is also briefly described in this chapter.

Chapter 8 shows the experimental trapezoidal modulation operated laboratory-scale prototype for the three phase modular multilevel converter (MTrMMC-DC-DC), and the 4 phase resonant modular multilevel series chain-link converter (TrSCC-DC-DC). The description of the control platform and software implementations are

included in this chapter. The main part of this chapter presents experimental results of the AC link current, DC current, chain-link voltage, submodule capacitor voltage and other necessary waveforms for the MTrMMC-DC-DC and TrSCC-DC-DC set up.

Chapter 9 presents the conclusions of this project where after considering the main design objectives, it summaries the advantages and challenges associated with each converter and each operational mode. It also concludes that the TrSCC-DC-DC converter operating with mode B is the most appropriate option for the targeted application, considering the main design objectives. Additionally, this chapter summarises the work which may further develop what has been presented in this thesis such as the design and analysis of the transformer used in each topology and the cooling system requirement for both submodule devices and transformers.

1.4 Contribution of the thesis work

The main outcome of this project is the development of two modular multilevel DC-DC converters, the MTrMMC-DC-DC and TrSCC-DC-DC. The simulation results and experimental validation of the MTrMMC-DC-DC highlights the following contributions to knowledge:

- A new trapezoidal waveform approach for modular multilevel DC-DC converters.In comparison to the existing modular multilevel converters operating with trapezoidal wave-shaping, the MTrMMC-DC-DC provides a better submodule semiconductor device utilisation which helps to distribute the losses between the devices, hence,a simpler cooling system is required

- Lower device current rating requirement which reflects on the cost and the area of silicon used in the converter

- Reduction in the energy storage requirements in comparison to non trapezoidal wave-shaping through careful design of the submodule (SM) capaci-

tors and arm inductors to achieve resonance between the effective equivalent capacitor of each arm and the arm inductor at a frequency below twice the fundamental operating frequency.

- Reduction of control complexity by reducing the sorting frequency of the submodule capacitor voltages

The simulation and experimental results validate the operation of the novel modular multilevel DC-DC power converter topology, the modular multilevel series chain-link resonant DC-DC converter, TrSCC-DC-DC, demonstrate the following contributions to knowledge:

- A significant reduction (66%) in the number of submodules, and the required components of the submodules such as gate drive circuit, power supply, transmitter and receivers, buffers, sensors and etc
- A much simpler control system in comparison to any other modular multilevel DC-DC converter due to the significant reduction in number of submodules and a reduction in the sorting frequency of the submodule capacitor voltages
- A significant reduction in $\frac{dv}{dt}$ voltage stress on the transformer insulation
- The semiconductor losses are shared between the submodule devices by better utilisation of the devices over the the fundamental period without additional switching losses
- A significant reduction in energy storage requirements and a potential for higher power density due the capability of operating the converter at a higher fundamental frequency
- A reduction in devices current rating (VA requirement) which reduces the area and the cost of the silicon used for the submodule devices
- Adapted easily to a high power, high voltage system with a small, medium and high DC voltage ratio

Additional contributions to the knowledge have been achieved as following:

- A new capacitor voltage balancing method for the trapezoidal wave-shaping
- A novel energy control method for the modular multilevel DC-DC converters operating with trapezoidal waveforms and this allows the control of the DC current during system transients

Chapter 2

Background of HVDC systems

2.1 Introduction to HVDC Transmission

High voltage direct current (HVDC) transmission systems have the potential to become the preferred choice for transmitting the electrical energy as a result of their advantages in comparison to high voltage alternate current (HVAC) transmission systems. These advantages can be mainly classified into two groups.

Firstly, from an economic perspective, for distances longer than break even distance shown in figure 2.1, an HVDC transmission system is more cost effective than conventional HVAC. This is a result of their requirement for reduced transmission line numbers and an increased transmission efficiency for DC Transmission. This last point is due to the absence of the skin effect and the reactive power in the DC systems [20]. In addition, the voltage at the end of a very long AC transmission line ($> 200km$) could increase up to 50% relative to the sending end at low load and this limits the length of the AC transmission line. This phenomenon is called "Ferranti Effect" which occurs due to the LC impedance of the AC transmission line at low load.

Secondly, from a technical perspective, the issue with the reactive power is exacer-

bated when the transmission lines need to be under water. The capacitance of these cables is significant and hence the charging current for these cables can be very high. Since the current is continuous for AC transmission, the capacity of the cable for real power flow is reduced. As a result, the break even distance is shorter when implementing a transmission line underwater. In addition, the interconnection of asynchronous AC grids (networks with different operating frequency) much more easily with the use of the back-to-back HVDC transmission systems[21].

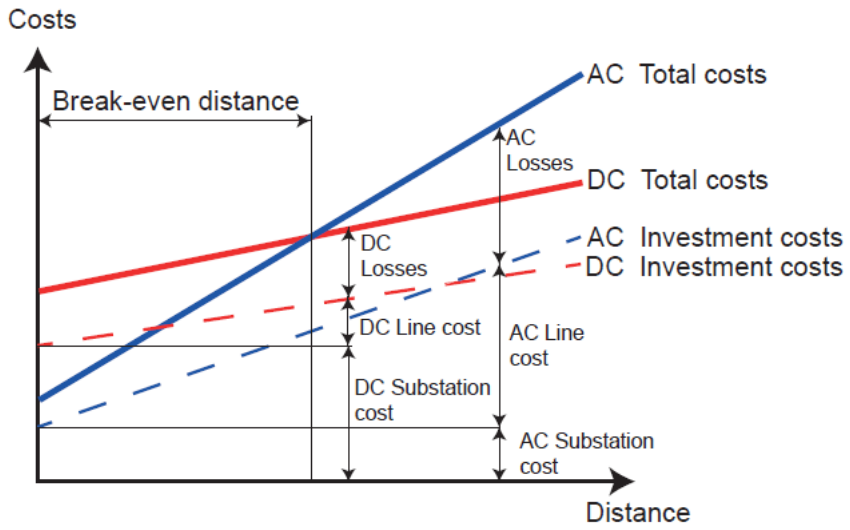


Figure 2.1: *Cost versus transmission line distance of HVDC and HVAC [1]*

HVDC transmission system consists of several elements and the HVDC technology is mainly characterised by the type of the power converter used between the AC and DC connections. There are two main power conversion schemes for HVDC systems, those utilising current source converters (CSC) and others using voltage source converters (VSC). Thyristor devices are often used in the CSC based HVDC. In these applications they are more commonly known as Line Commutated Converters (LCC) since the thyristor device commutations are based on the polarity and angle of the voltage of the AC grid. Alternatively, the Voltage Source Converter based HVDC (VSC-HVDC) uses self/force-commutated semiconductor devices, such as Insulated Gate Bipolar Transistors (IGBTs) [22].

There are various ways in which HVDC stations can be configured, depending on the operational requirements and required functionality. The following configurations can be implemented using LCC HVDC and VSC HVDC based systems and are commonly presented in the literature [23–25]:

- **Monopolar HVDC Configuration:** Monopolar systems have three main sub-configurations as shown in figure 2.2, depending on the implementation of the current return line. These three sub-configurations are ground return, metallic grounded return and un-grounded metallic return (Symmetric Monopolar).

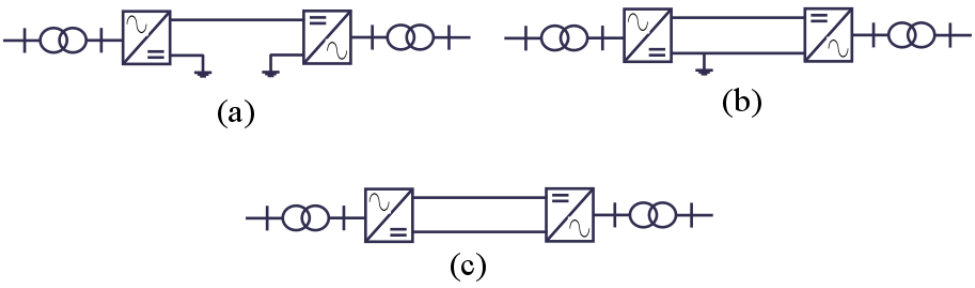


Figure 2.2: *Monopolar HVDC configurations: (a) asymmetric monopolar with ground return, (b) asymmetric monopolar with metallic return, (c) symmetric monopolar*

- **Bipolar HVDC Configuration:** A Bipolar configuration is formed by using two asymmetric monopolar systems which can be operated independently, thus adding redundancy to the system at half of the rated power. Figure 2.3 shows the possible bipolar configurations which are bipolar with ground return and bipolar with metallic return. Under normal operating conditions when both monopolar systems share the transferred power equally, ideally there would be zero current in the return path (under realistic conditions there is always a small current flowing as a result of the parameter mismatch in the system components).

- **Back-to-Back HVDC Configuration:** In a Back-to Back HVDC system the converters are located in the same station and there is no DC transmission lines. This configuration is suitable for connecting asynchronous AC systems together.

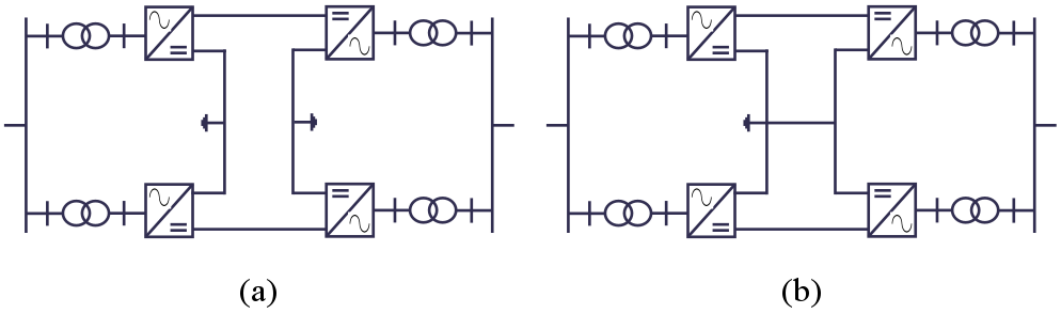


Figure 2.3: *Bipolar HVDC configurations: (a) bipolar with ground return, (b) bipolar with metallic return*

2.2 Line Commutated Converters: LCC-HVDC

LCC based HVDC was the first technology developed for the HVDC transmission over the long distances. It was installed in Gotland, Sweden in 1954 [23]. Although originally it was operated using Mercury Arc Rectifiers, these have been replaced with Thyristors . Thyristors still represent the most efficient implementation of the HVDC transmission at very high powers as a result of the low losses associated with the operation. HVDC applications use 6 pulse thyristor bridges such as the one shown in figure 2.4. Although only one thyristor is shown in each arm of the bridge, these would typically be constructed of many series connected thyristors to form an equivalent "valve" with increased voltage rating. Snubber circuits are required for each series connected thyristor, firstly, to ensure that all of the thyristors share the voltage equally when the valve is in the off state. Secondly, they protect the thyristor devices from over voltage, high $\frac{dv}{dt}$, and high $\frac{di}{dt}$. Although the thyristor can be triggered to turn on, it is turned off naturally as a result of the operation of the electricity grid. As a result, the valve can only be used to control active power and the AC grid current is characterised by a poor waveform quality and a low power factor [24]. As a result LCC based stations tend to require local bulky passive filter and power factor correction components or Static Synchronous Compensator (STATCOM) circuits.

Furthermore, The commutation in the LCC converters requires a very high syn-

chronous voltage source, hence hindering its use for a feature known as "black start" and it has also caused AC voltage stability issues in the weak AC grids. Power reversal from one station to another can be achieved only by inverting the polarity of the DC voltage and keeping the direction of the current constant in the LCC stations. Hence, the development of DC grids is prevented to the difficulty of achieving the power reversal in complex multi-terminal HVDC using LCC configurations [4, 26].

In order to reduce the size of the filters and improve the power quality six pulse rectifiers can be connected in parallel on the AC side via a phase shifting transformer. Similarly, 12 and 24 pulse thyristor rectifiers are common in literature [3, 27]. For instance, in the Neptune RTS project based on the LCC configuration [3], two six-pulse converters have been connected as shown in figure 2.5. This arrangement eliminates the 5^{th} and 7^{th} current harmonics on the AC side and the 6^{th} harmonic on the DC side. Figure 2.6 depicts the Neptune RTS station and it can be observed that filters determine the overall footprint of the station even when a two six-pulse LCC configuration is used. Consequently, the LCC technology is not the preferred for the HVDC transmission at low power application and in offshore environments, where space is limited and expensive (on an offshore platform for example).

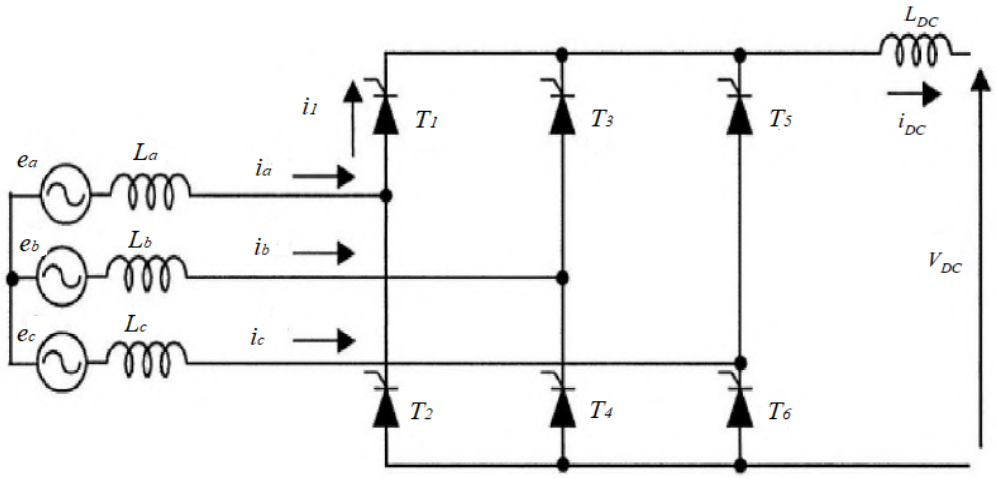


Figure 2.4: *Six pulse LCC configuration [2]*

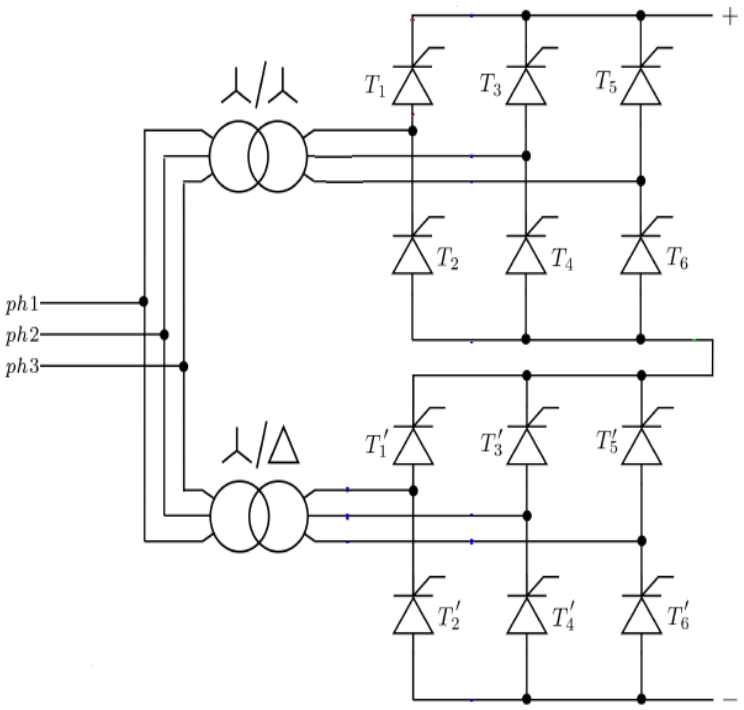


Figure 2.5: *12 pulse LCC configuration*

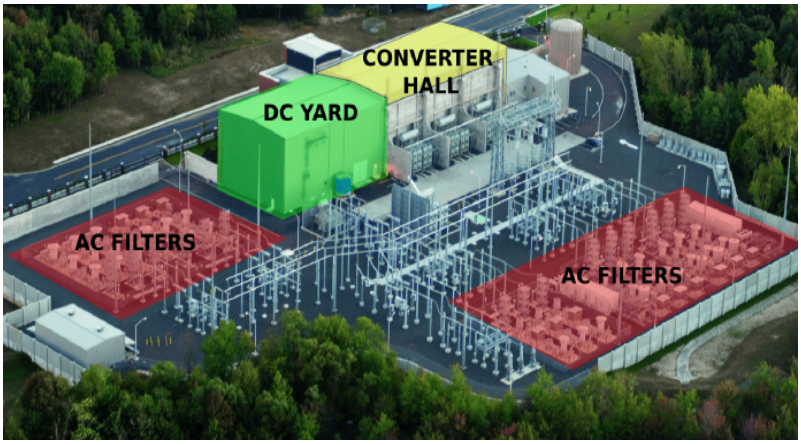


Figure 2.6: *two six pulse LCC configuration [3]*

2.3 Voltage source converter: VSC-HVDC

In comparison to LCC-HVDC systems, VSC-HVDC technologies offer many advantages:

- The presence of the electricity grid is not critical to the commutation of the switching devices because the semiconductors used in the VSC HVDC can be controlled to turn on and off. As a result, commutation failure is not an issue in the VSC HVDC [24].

- Reactive power compensation is not required in the VSC HVDC because the active and reactive power can be independently and rapidly controlled by the VSC. As a result, the AC system stability is improved [28].

- The VSC HVDC can generate an independent AC voltage without the presence of an AC grid voltage hence it can be used for a black start operation. This capability of a black start operation is useful in connecting offshore wind energy to the onshore AC grid [29, 30].

- Power flow can be reversed without changing the polarity of the voltage terminals in the VSC HVDC and this is essential to achieve bidirectional power flow in the HVDC grids. It also enables the use of modern cable technology which cannot be used for the LCC-HVDC.

- The VSC HVDC requires very little AC side filtering which reduces its physical footprint, making it more viable as an option for the offshore wind systems.

In the voltage source converters, the utilised switching devices can be controlled to switch on and off. Two main VSC typologies were originally considered for the HVDC transmission. The first group comprises a Two-level or a three-level converters. The two level converter is shown in figure 2.7 where a large number of low voltage (3kV), fully controlled, semiconductor devices are series connected to form a valve with the required voltage rating for the HVDC system. Pulse Width Modulation (PWM) techniques are used to develop the switching demands for the valves and this produces a two level phase voltage (referred to the midpoint of the DC bus) as shown in 2.8-a. These techniques inherently produce harmonics at the valve switching frequency and therefore filters are required to ensure that an appropriate current waveform quality is achieved on the AC side [24]. In order to reduce the size of these filters the semiconductor devices are switch at high frequency, resulting in increased losses as a result of the inefficiency of this switching process.

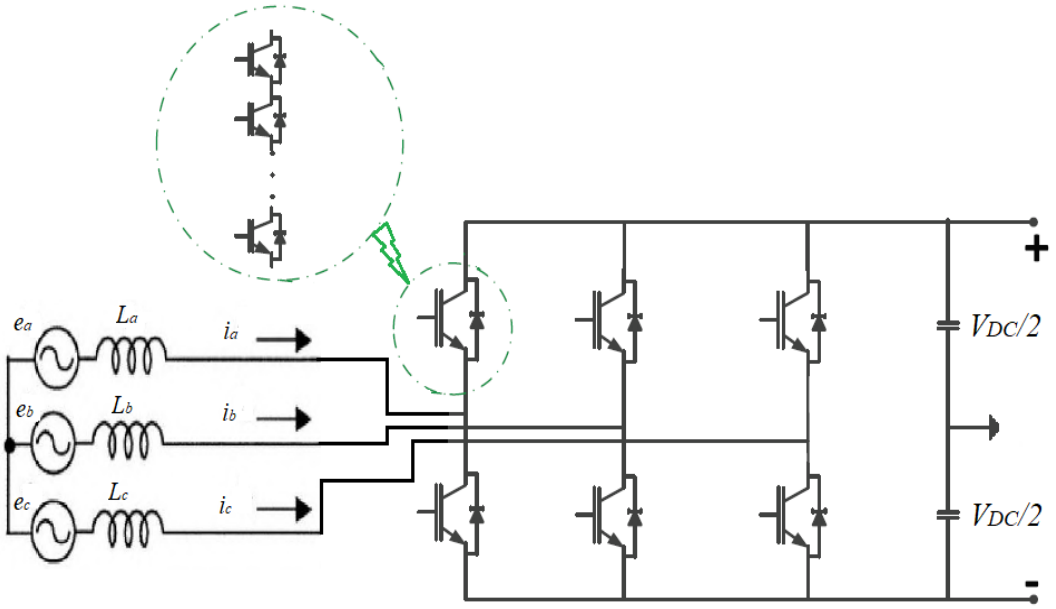


Figure 2.7: *Two level converter*

The AC current waveform harmonics can be reduced without excessive filtering by using multilevel converter topologies which form the second group of the VSC based converters considered for the HVDC transmission. The AC voltage of a multilevel converter is generated in small steps as shown in figure 2.8-b and as the number of the level increases the accuracy of the generation of a sine wave is increased meaning that the harmonic content is reduced. These converters which tend to be modular also generally don't require the use of series connected switches and its associated issues since they are formed by series connected, locally voltage clamped cells. In addition, the switching frequency of the individual semiconductor devices is lower than the effective switching frequency observed in the full waveform produced (in HVDC applications the device switching frequency can be low as fundamental frequency) and accordingly, switching losses are lower. Diode clamped, Cascaded H-bridge and Capacitor clamped converters were the initial multilevel converter topologies [31–33]. Over the last three decades many multilevel converter topologies have been considered for applications in this field.

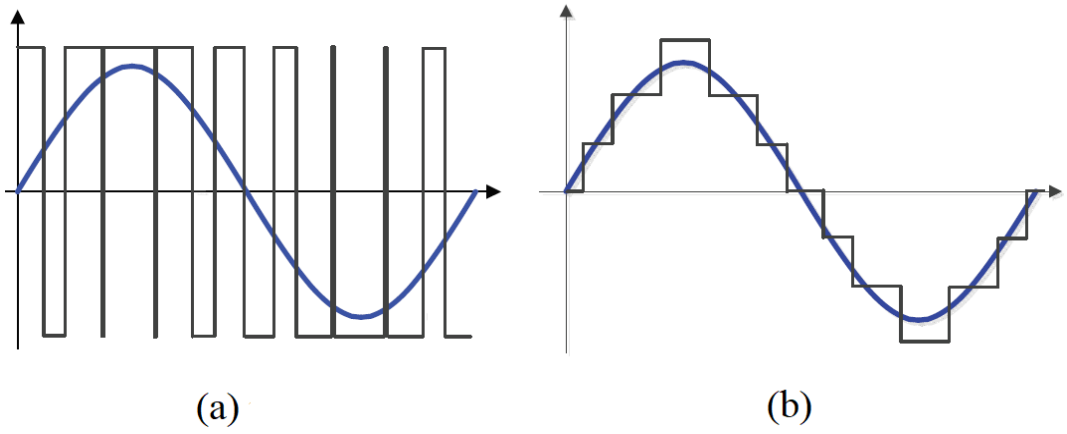


Figure 2.8: *AC voltage waveforms: (a) two level, (b) multilevel*

2.4 Applications of HVDC Technology

Originally HVDC was developed to tackle issues associated with asynchronous grid interconnection and bulk power transmission over long distances. However, since its inception, other applications have been considered, including:

- **HVDC tapping:** Tapping energy from HVDC transmission lines to feed energy to the local off-grid areas that are close to the lines has gained interest due to the environmental and economical advantages [17, 34]. Up to 10% of the HVDC system rated power can be extracted to feed electricity to the nearby off-grid communities without disturbing the HVDC system [35].

- **Offshore wind energy farms interconnection:** The amount of power that can be generated by offshore wind technology is increasing every year and the distance of this renewable energy source from the shore is usually longer than the break-even distance previously discussed. Due to the various environmental, technical and economical advantages, HVDC transmission systems have been the favourable method of connection between the most offshore wind power stations and the onshore grids [36, 37].

- **Multi-terminal HVDC technologies and HVDC grids:** Multi-terminal HVDC technologies enable multiple HVDC links to be joined together to form a DC network capable of facilitating power exchange between terminals. Although the first multi-terminal HVDC system was installed based on the LCC-HVDC

system in 1986 in Italy, the LCC-HVDC technology is usually used when the direction of power flow is dominant in one direction since the DC terminal voltage must be inverted when the power direction is reversed[38]. Since the introduction of the VSCs, which can reverse the power flow direction without the reversal of the converter terminal voltage, multi-terminal HVDC systems have gained increased interest.This is mainly a result of the advantages that they present with respect to cost, power losses in conversion station and reliability [39, 40].

Recently, DC and HVDC grids have gained significant academic and industry interest as subjects of study and the first technical guidelines for HVDC grids was introduced by the European HVDC study group in September 2010 [15]. Later, guidelines to standardize HVDC and DC grids have been developed by CIGRE, IEEE, and the IEC [14, 15]. The motivations for developing HVDC grids are numerous and they can be summarised into environmental and economical considerations. From the environmental point of view, the use of large scale renewable energy sources as an alternative to the use of fossil fuels to reduce greenhouse gas emissions and support the growth of electrical power demands. These large scale renewable energy sources are mainly far from the load center and have stochastic generation characteristic [41]. Section 2.1 discussed the advantages of the HVDC systems with respect to their environmental friendliness and economical superiority when compared to the HVAC for the bulk electrical energy transmission. For these reasons many Point-to-Point (P2P) HVDC systems have been established and the concept of the HVDC grids has become important because the currently congested AC grids can be upgraded and expanded with the addition of the HVDC grids. The HVDC grids also add flexibility, stability and redundancy to the systems. Additionally, different market areas can be interconnected including off-grid urban areas and the asynchronous AC grids [35, 42, 43].

The development of the HVDC grids will involve many multi-terminal HVDC sys-

tems and the presence of the many non standard P2P HVDC systems with different HVDC technologies and schemes. As a result, high power DC-DC converters and DC circuit breakers will be required for the voltage matching, fault ride-through and to support the segmentation of the large DC grid into the smaller DC protection zones which can improve reliability when faults occur [14, 15, 17, 41, 42].

The next chapter describes the high power DC-DC converters that have been proposed in the literature so far for the HVDC grid applications.

2.5 Summary

This chapter presented the advantages of the HVDC systems in terms of the economical, environmental and technical aspects for various applications such transmitting and integrating renewable energy sources, tapping energy to local area, multi-terminal HVDC and HVDC grids. It also showed the possible HVDC configurations, bipolar HVDC, monopolar HVDC and back to back HVDC, where these configurations are mainly determined by the application. The concept of the HVDC types based on converter stations were shown and the advantages of the VSCs converter over the LCC converter were explained in terms of the quality waveforms, power losses, reactive power control in AC/DC systems and bidirectional power flow which is required in developing multi-terminal HVDC system and HVDC grids. This chapter has also presented the importance of multi-terminal HVDC systems in terms of cost, power losses in converter station, reliability and developing to future HVDC grids for expanding the existing AC grids. The requirement of the DC-DC converters in the HVDC interconnections in an effort to achieve multi-terminal HVDC and HVDC grids was described and this highlighted where DC-DC converters are required to achieve voltage regulation, isolation in the non standard HVDC systems and the splitting of the large DC networks into the small protection zones to prevent the entire breakdown of the grid when a DC fault occurs.

Chapter 3

High Power DC-DC Converters in HVDC Grid Applications

3.1 Introduction

This chapter focuses on the high power DC-DC converters that have been introduced in the literature. It shows the general description, advantages and disadvantages of the high power DC-DC converters. The proposed high power DC-DC converters can be classified into two main groups: isolated high power DC-DC converters, and non isolated high power DC-DC converters.

3.2 Isolated high power DC-DC converters

The isolated high power DC-DC topologies proposed in the literature are based on two conversion stages, DC-AC conversion and AC-DC conversion. Transformers are used to provide galvanic isolation and voltage scaling between the AC stages. Isolation is required to achieve interconnection between the HVDC systems with different voltage level particularly at medium and high DC transformation ra-

tios (1.5 $\leq$ medium DC ratio $<$5, high DC ratio $\geq$5) and the voltage matching is achieved by adjusting the ratio of the transformer. Having isolation offers the interconnection of the HVDC systems with different configurations and schemes. Although some of these tasks can also be achieved by means other than galvanic isolation, using an isolated structure allows simplification in the design and increased safety. Other advantages of an isolated topology is the inherent DC-fault blocking capability that provide the reliability to the system. In the following sections various isolated high power DC-DC converters are briefly described.

3.2.1 Two-level high voltage DAB converters

The two-level high voltage DAB converter is constructed by interconnecting the two VSCs via a medium frequency transformer, up to a few kilohertz, the aim of the latter is to reduce the physical footprint of the overall converter. Figure 3.1 shows a three phase two-level high voltage DAB converter where each arm of the VSC consists of a number of the series connected semiconductor devices (usually IGBTs), in order to create an equivalent HV valve. Conventionally, the devices in each arm operate with a fixed 50% duty cycle and the power flow is transferred by introducing a phase shift between the VSC1 and VSC2 as shown in 3.2-a [44–46]. Soft switching of the devices is possible at zero current over a wide operational power range resulting in reduced switching loss, but this is achieved at the cost of operating with a high circulating reactive current in the MF AC link[44].

The per-phase primary and the secondary AC voltage across the transformer, $V_{ao1}(t)$and $V_{uo2}(t)$, can be mathematically expressed as shown in equation 3.1 where φ is the phase angle between the primary and secondary voltage. Considering an ideal converter which operates with zero losses, the AC link current can be expressed as 3.2 where L_k is the leakage inductance of the transformer and n is the transformer turns-ratio. Equation 3.3 represents the average exchange power between the two VSCs.

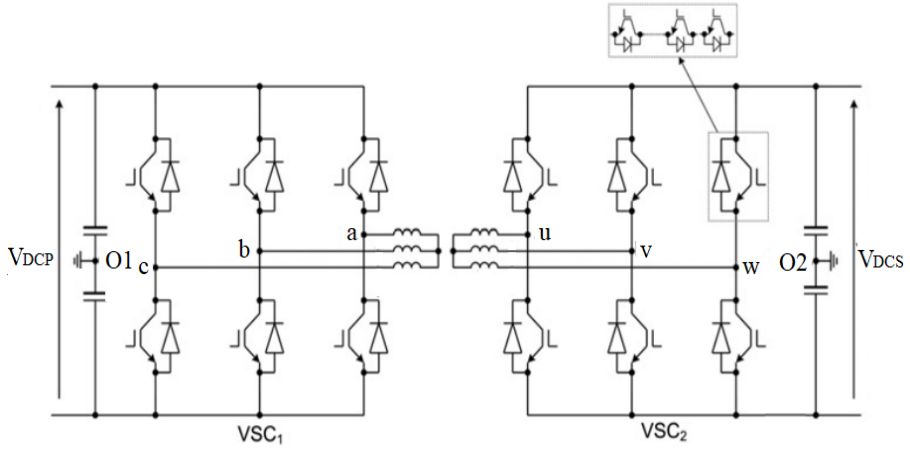


Figure 3.1: *Two-level high voltage DC-DC Converter*

$$
\begin{aligned}
v_{ao1}(t) &= \frac{2V_{DCP}}{\pi} \sum_{k=1,3,5}^{\infty} \frac{sin(k\omega t)}{k} \\
v_{uo2}(t) &= \frac{2V_{DCS}}{\pi} \sum_{k=1,3,5}^{\infty} \frac{sin(k\omega t + k\varphi)}{k}
\end{aligned}
\tag{3.1}
$$

$$
\begin{aligned}
i_{ao1}(t) = \frac{1}{\omega L_k} * (-\sum_{k=1}^{\infty} \frac{2V_{DCP}}{\pi k^2} sin(k\omega t + \frac{1}{2}\pi) + \\
n \sum_{k=1}^{\infty} \frac{2V_{DCS}}{\pi k^2} sin(k\omega t + \frac{1}{2}\pi + k\varphi))
\end{aligned}
\tag{3.2}
$$

$$
P_{av} = \frac{1}{T} \int 3 v_{ao1}(t) i_{ao1}(t) \quad = n \frac{6 V_{DCP} V_{DCS}}{\pi^2 \omega L_k} \sum_{k=1}^{\infty} \frac{sin(k\varphi)}{k^3} \tag{3.3}
$$

Another modulation scheme for this converter, selective harmonic elimination (SHE) has been considered in an effort to minimise the circulating reactive current and control the power flow by using the phase shift and notching the VSC voltages, $V_{ao1}(t)$ and $V_{uo2}(t)$, as depicted in 3.2-b. The inherent soft switching range with this modulation technique is reduced and switching losses are increased when compared to the previously described control method [4, 47].

The use of a two-level high voltage converter has several disadvantages in HVDC applications. The first is that the two-level voltage imposes a high $\frac{dv}{dt}$ resulting in electromagnetic interference and significant insulation stress on the transformer.

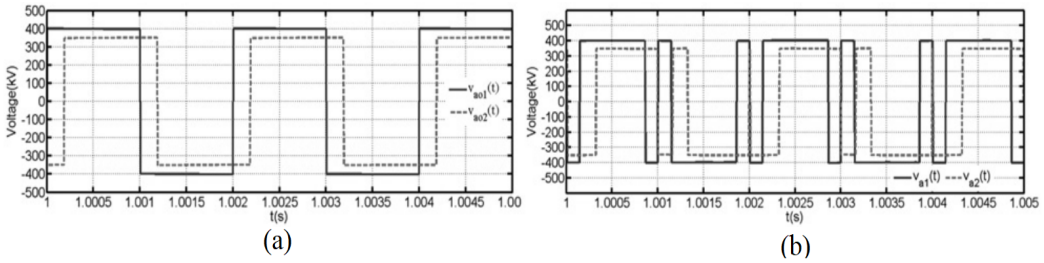


Figure 3.2: *Voltage waveforms of two-level high voltage DAB with modulation schemes: (a) phase shift modulation (b) SHE modulation [4]*

Secondly, to achieve static and dynamic sharing among the semiconductor devices in each arm, snubber circuits and active IGBT gate-drive techniques are required [48].

3.2.2 Modular Multilevel Converter based DC-DC converters

Modular multilevel converter based DC-DC converters are the preferred choice for medium/high power applications. In particular, They are rapidly becoming the most attractive topologies for HVDC systems due to the advantageous features of the MMCs. These features include:

- **Scalability** MMC based DC-DC converters can be scaled to meet any required voltage level by varying the quantity of the series connected submodules (SMs) in the arms of the converter. Increasing these SM numbers also results in a higher quality waveform being produced by the VSC. This results in fewer harmonics, reduced $\frac{dv}{dt}$ stress across transformer and a much reduced electromagnetic interference. With a higher number of levels, it is also possible to operate at low device switching frequency. However, a limitation with number of SMs is the control complexity and the cost of the converter [49, 50].

- **Efficiency** Its high efficiency due to a large number of the levels which leads to a low switching frequency requirement and this is a significant advantage in the high power applications [51].

- **Modularity** Since the SMs used in the converter arms are identical, the converter has a high level of modularity. With this consideration, the use of identical SMs means that in the case of a SM failure, it can be bypassed and replaced. It is also easy to build redundancy by simply adding more SMs than required [52].

- **DC Bus capacitance** A bulky DC link capacitor is not required in some of the modulation schemes since the DC voltage and current are smooth [53].

In MMC based DC-DC converters, the medium frequency transformer is used to provide galvanic isolation and the voltage matching between the DC ports. Operation at medium frequency means a potential reduction in the size of the transformer and other passive components of the converter such as SM capacitors, the SMs themselves, and the arm inductors. Different operating modes have been introduced in the literature, the main two being sinusoidal operation and trapezoidal operation of an MMC-DC-DC (Q2L).

3.2.2.1 Sinusoidal operation of the Modular Multilevel DC-DC converters

Figure 3.3 shows an MMC-DC-DC topology that operates with sinusoidal waveforms. Sinusoidal operation of the MMC-DC-DC will be used as a benchmark for the comparison with the other modulation methods. The topology comprises two three phase MMC. The AC sides of these converters are connected together via a medium frequency, three phase, star connected transformer. The basic operation of an MMC is given in [54] and is summarised here. Each MMC consists of three phase legs which are further split into the upper and lower arms. Each arm contains a number of the series connected identical SMs, N_{SM}, forming one "chain-link", a series inductor, (L_P or L_S), and a resistor, (R_P or R_S), which represents the winding resistance of the inductor. P and S represent the primary side and secondary side of the converter, respectively. The SMs in each arm are switched to produce the desired AC phase voltage with a DC offset of the half of the DC link voltage. The arm inductor is included to minimise the ripple in the arm currents and to limit the

inrush current which may occur in the presence of a DC side fault.

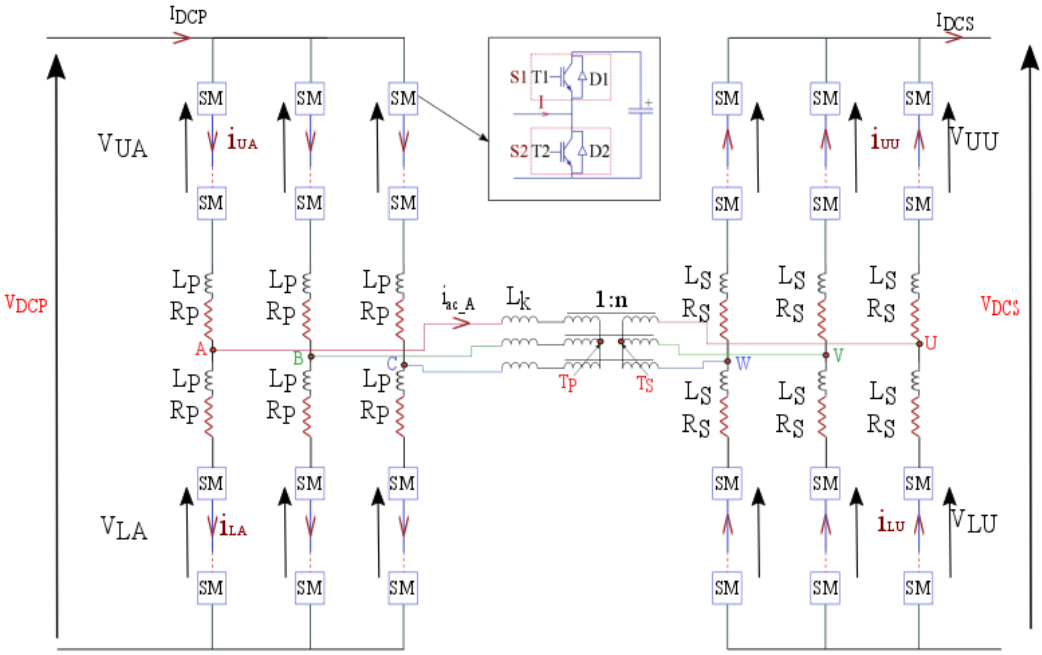


Figure 3.3: *MMC DC-DC Converter*

Each chain-link supports the full DC port voltage and each SM capacitor average voltage is controlled at nominal voltage, ideally $V_{SM\_P} = \frac{V_{DCP}}{N_{SM\_P}}$ and $V_{SM\_S} = \frac{V_{DCS}}{N_{SM\_S}}$. The insertion of the SM capacitors into the converter arm is controlled so that in each leg, the arms are complementarily inserted to control the power flow. Two independent control loops are generating the reference for inserting the SMs. Equation 3.4 and equation 3.5 represent the instantaneous insertion of the SMs of the primary phases and secondary phases, respectively, where m_p is the primary modulation index, m_s is the secondary modulation index, $\beta_{\phi P} = \frac{V_{\phi RefP}}{V_{DCP}}$ and $\beta_{\phi S} = \frac{V_{\phi RefS}}{V_{DCS}}$. $V_{\phi RefP}$ and $V_{\phi RefS}$ are the average of the sum of the total SM capacitor voltages of each arm of the primary and secondary side MMC, respectively. The instantaneous upper and lower chain-link voltages, $V_{U\phi P}$ and $V_{L\phi P}$, of the primary phases and the instantaneous upper and lower chain-link voltages, $V_{U\phi S}$ and $V_{L\phi S}$, of the secondary phases are shown in equation 3.6 and equation 3.7, respectively, where ϕP represents the primary MMC phases (A, B, C) and θ_{ip} represents 0, $\frac{\pi}{3}$, $\frac{2\pi}{3}$ for the phases A, B, C, respectively. The secondary MMC phases (U, V, W) are represented by ϕS

and θ_{is} represents 0, $\frac{\pi}{3}$, $\frac{2\pi}{3}$ for the phases U, V, W, respectively. [55–57].

$$\begin{aligned} n_{U\phi P}(t) &= \frac{N_{SM\_P}}{2}(\beta_{\phi P} - m_p * sin(\omega t + \theta_{ip})) \\ n_{L\phi P}(t) &= \frac{N_{SM\_P}}{2}(\beta_{\phi P} + m_p * sin(\omega t + \theta_{is})) \end{aligned} \tag{3.4}$$

$$\begin{aligned} n_{U\phi S}(t) &= \frac{N_{SM\_S}}{2}(\beta_{\phi S} - m_s * sin(\omega t + \varphi + \theta_{is})) \\ n_{L\phi S}(t) &= \frac{N_{SM\_S}}{2}(\beta_{\phi S} + m_s * sin(\omega t + \varphi + \theta_{is})) \end{aligned} \tag{3.5}$$

$$\begin{aligned} V_{U\phi P}(t) = n_{U\phi P}(t) * V_{SM} &= \frac{V_{DCP}}{2}(\beta_{\phi P} - m_p * sin(\omega t + \theta_{ip})) \\ V_{U\phi P}(t) = n_{U\phi P}(t) * V_{SM} &= \frac{V_{DCP}}{2}(\beta_{\phi P} + m_p * sin(\omega t + \theta_{ip})) \end{aligned} \tag{3.6}$$

$$\begin{aligned} V_{U\phi S}(t) = n_{U\phi S}(t) * V_{SM} &= \frac{V_{DCS}}{2}(\beta_{\phi S} - m_s * sin(\omega t + \varphi + \theta_{is})) \\ V_{L\phi S}(t) = n_{L\phi S}(t) * V_{SM} &= \frac{V_{DCS}}{2}(\beta_{\phi S} + m_s * sin(\omega t + \varphi + \theta_{is}))) \end{aligned} \tag{3.7}$$

Under the normal operating conditions, $V_{RefP} = V_{U\phi P} + V_{L\phi P}$ and $V_{RefS} = V_{U\phi S} + V_{L\phi S}$ are regulated at V_{DCP} and V_{DCS} respectively in order to facilitate the power flow between the AC and DC sides of the each MMC. Considering a lossless converter, the AC voltage $v_{\phi PTP}$ and $v_{\phi STS}$ are generated by subtracting the upper arm voltage from the lower arm voltage as shown in equation 3.8. The power flow between the AC side of the primary MMC and the AC side of the secondary MMC is controlled by imposing the m_p and controlling both the m_s and the φ [55, 56]. The average power flow between the MMCs can be approximated as shown in 3.9 where $L_{eq} = \frac{1}{2}L_P + \frac{1}{2}L_S + L_k$.

$$\begin{aligned} v_{\phi PTP}(t) = V_{L\phi P}(t) - V_{U\phi P}(t) &= \frac{V_{DCP}}{2} * m_p * sin(\omega t + \theta_{ip}) \\ v_{\phi STS}(t) = V_{L\phi S}(t) - V_{U\phi S}(t) &= \frac{V_{DCS}}{2} * m_s * sin(\omega t + \varphi + \theta_{is}) \end{aligned} \tag{3.8}$$

$$P_{av} = n\frac{3m_p m_s V_{DCP} V_{DCS}}{\omega L_{eq}} sin(\varphi) \tag{3.9}$$

The current is continuous in each arm and it comprises an AC and DC component. The differential-mode currents, $i_{ac\phi} = i_{U\phi P} - i_{L\phi P} = \frac{1}{n}(i_{U\phi S} - i_{L\phi S})$, are used to transfer power between MMCs. The common-mode currents, $i_{com\phi P} = \frac{1}{2}(i_{U\phi P} + i_{L\phi P})$ and $i_{com\phi S} = \frac{1}{2}(i_{U\phi S} + i_{L\phi S})$, circulate between lower and upper arms and are used to transfer power between the DC port and the MMC. In MMC converters, additional controllers (or alternative methodologies) are required to eliminate the second order harmonic in the arm current which leads to an increase in the SM capacitor size and power device losses (conduction and switching loss) [58, 59].

Sinusoidal operation of an MMC-DC-DC converter provides a DC fault blocking and black start capability by controlling the voltage in the AC link since the modulation index range is fully available. Additionally, sinusoidal operation significantly reduces the $\frac{dv}{dt}$ stress on the transformer insulation. However, operation at a low modulation index increases the SM capacitor voltage ripple and therefore in order to keep the SM capacitor voltage ripple within the desired levels and prevent an increase in voltage stress on the semiconductor devices, the capacitance must be oversized and hence the variation of the modulation index is limited . As previously mentioned, the higher frequency operation of the AC link reduces the size of the transformer in the MMC-DC-DC converter. However, an increase in the operating frequency of the AC link will also result in higher switching losses and accordingly a reduction in the overall DC-DC converter efficiency. Therefore, operating frequency up to $350Hz$ has been proposed in literature consequently lower power density is expected under sinusoidal operation of an MMC-DC-DC converter when compared with that of a two level high voltage DAB converter [5, 55].

The AC component of the arm current circulates in the SM capacitors and produces ripple in the SM voltage. When the MMC converter is operating correctly, the desired chain-link voltage is produced only if the SM voltage ripple is limited within

a certain range. The size of the SM capacitor, C_{SM}, is the key component for limiting this voltage ripple. The required capacitance for the primary and secondary SMs can be analytically derived as shown in equation 3.10, where Pr is rated power and δ_{pp} is the peak to peak SM voltage ripple [60, 61]. The energy storage, E_T, can be expressed based on equation 3.11 where N_{arm} is the number of the converter arms. However, in the literature, the converter energy storage is expressed as a per unit value of the converter power rating and is known as the capacitance constant, H_{cMMC}, as shown in equation 3.12. The capacitance constant, H_{cMMC}, is a function of the frequency, ω, modulation index, m_p and m_s, and voltage angle, φ [62, 63].

$$\begin{aligned} C_{SMP} &= \frac{Pr}{3V_{SM}N_{SM}m_p\delta_{pp}\omega}(1-(\frac{m_p}{2})^2)^{\frac{3}{2}} \\ C_{SMS} &= \frac{Pr}{3V_{SM}N_{SM}m_s\delta_{pp}\omega cos(\varphi)}(1-(\frac{m_s\cos(\varphi)}{2})^2)^{\frac{3}{2}} \end{aligned} \tag{3.10}$$

$$E_T = \frac{1}{2}N_{SM}V_{SM}^2 Narm(C_{SMP}+C_{SMS}) \tag{3.11}$$

$$H_{cMMC} = \frac{E_T}{Pr}[s] \tag{3.12}$$

The arm inductance is selected to reduce the $\frac{di}{dt}$ of the DC current when a fault occurs on the DC side of the converter and to reduce the circulating currents among the phases of the MMC. However, the selection of the arm inductor must avoid any resonance between the effective arm capacitance and the chosen arm inductance. In [64], the author identified the expression 3.13 which is the relationship between C_{SM} and L, in order to select the desired inductance and avoid the resonance where $L = L_P$ or/and $L = L_S$ for the corresponding primary or/and secondary arm inductance. The required energy storage for the sinusoidal operation of the MMC-DC-DC can be calculated from equations 3.10, 3.11 and 3.12 and it is between 15-20 ms for a 250Hz operating frequency.

$$LC_{SM} > \frac{5N_{SM}}{48\omega^2} \tag{3.13}$$

3.2.2.2 Trapezoidal operation of the Modular Multilevel DC-DC converters

Trapezoidal operation was proposed for the modular multilevel converters in [5]. Figure 3.4 shows the two possible configurations of the three phase trapezoidal MMC-DC-DC converter that can be used for HVDC interconnection. The three phase trapezoidal MMC-DC-DC converter is considered in detail since it will be used as a benchmark for comparison between the trapezoidal operating modes of the different converters. In trapezoidal configurations, the SMs in each arm are inserted for half of the waveform cycle and bypassed for the other half. The insertion and the bypass of the SMs are in a particular order and with a short transition time, T_t, in order to form a staircase transition in the output AC voltage of each phase from $-V_{DCP}/2$ to $V_{DCP}/2$ and vice versa as described in figure 3.5. The dwell time, T_d, is the time required between two voltage level transitions and it must be sufficiently small to minimise the size of the SM capacitors for a desired voltage ripple. On the other hand, the choice of the dwell time, T_d, must be large enough to prevent undesirable $\frac{dv}{dt}$ stress on the transformer and the range $5\mu s$ to $25\mu s$ has been chosen for T_d in the literature [5, 65]. However, increasing T_d leads to an increase in the SM capacitor value and the magnitude of sixth harmonic component in the DC current. As a result, the energy requirements of the TrMMC-DC-DC and converter footprint will increase [4].

In the configuration shown in figure 3.4-a, the transformer is star connected on both sides of the dc-dc converter and as a result there is no path for triplen harmonic currents to flow. Hence, the transformer winding voltage and current waveforms have a sinusoidal waveform appearance as shown in figure 3.6-a,b where the transformer voltage has a six-step waveform.

In the configuration figure 3.4-b, the transformer is installed with the neutral point of both of the star connections grounded. This results in a return path for the triplen harmonic currents, and resulting the transformer voltage waveform to have two

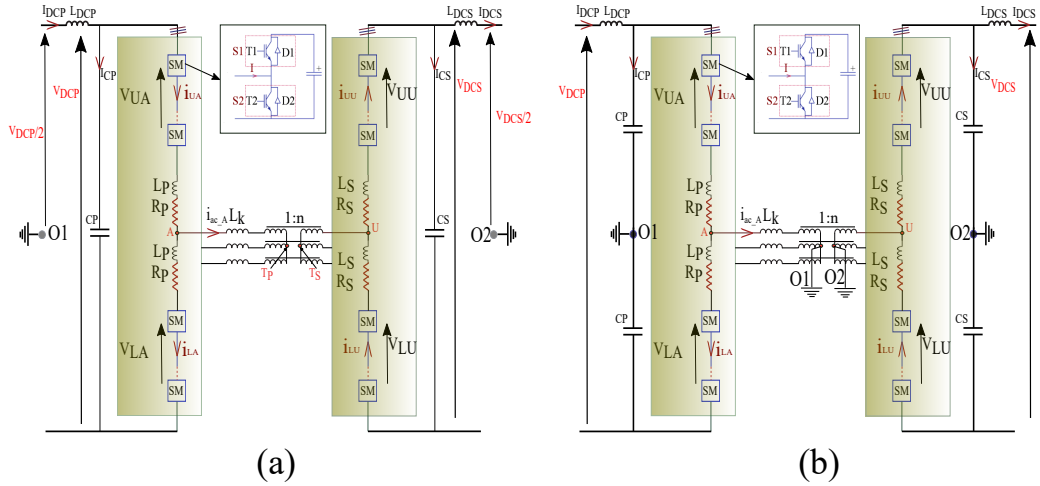


Figure 3.4: *Trapezoidal MMC DC-DC converter configurations: (a) Ungrounded transformer mid point (b) Grounded transformer mid point*

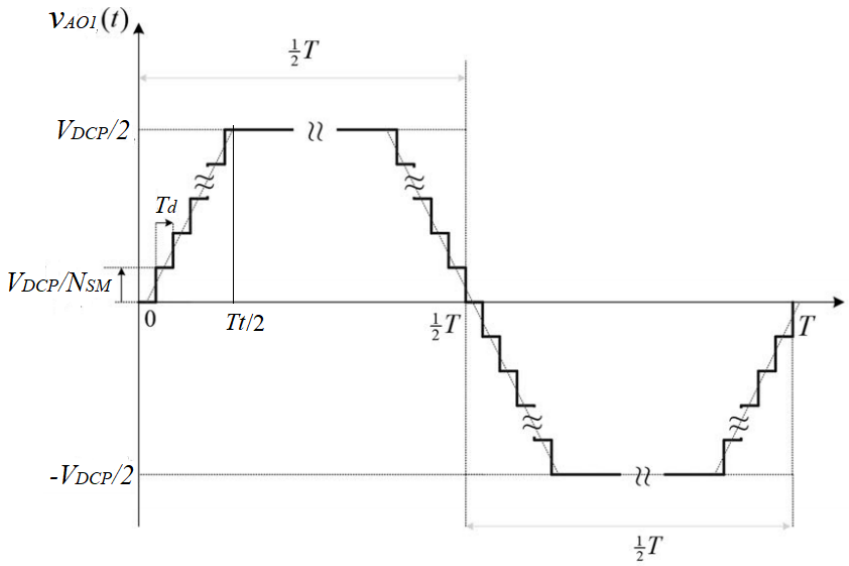


Figure 3.5: *Phase voltage with respect to O1 [5]*

dominant levels at $\pm V_{DCP}/2$ as presented in figure 3.6-c,d where the lower voltage was chosen for the secondary side of the converter. Considering the same power flow, configuration b requires less current and a slightly lower device current rating when compared to the configuration a. However, as a result of the presence of the triplen harmonic components in the configuration b, bulky DC side filters are required and this makes the configuration undesirable [5].

The current in the TrMMC-DC-DC is discontinues where each arm conducts for the half cycle when the SMs are bypassed. The arms are conducting together only

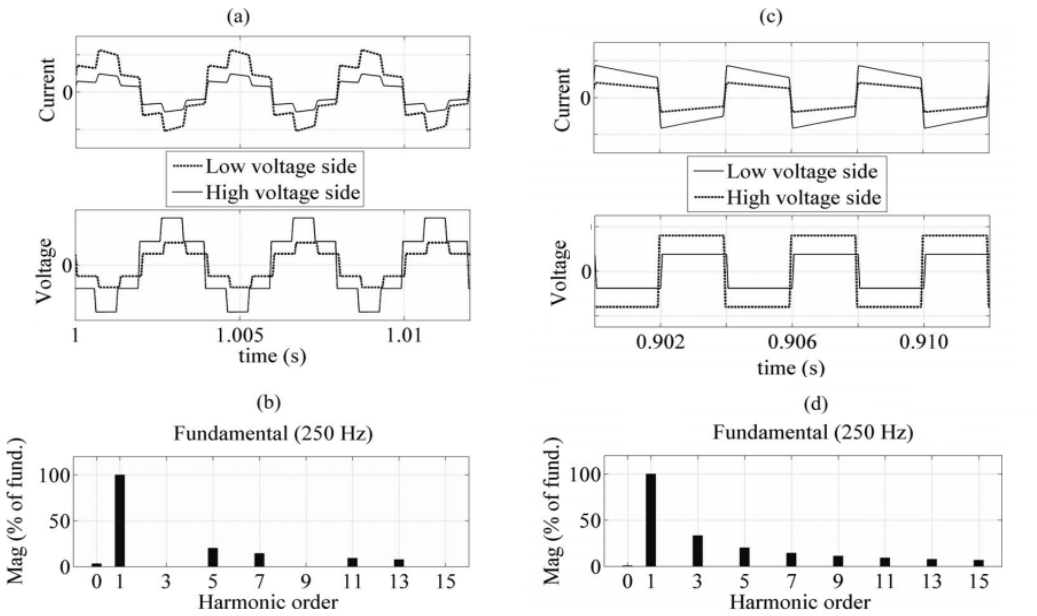


Figure 3.6: *Voltage and current waveforms: (a) Configuration a, transformer voltage and AC link current (b)Configuration a, FFT analysis of transformer voltage (c) Configuration b, transformer voltage and AC link current (d) Configuration b, FFT analysis of transformer voltage [5]*

during the transition period, T_t. The upper and lower arm currents are shown in figure 3.7 for the configuration shown in figure 3.4-a. Similar to a standard three phase DAB converter, the ideal DC current has a sixth harmonic component which results from the summation of the arm currents as shown in figure 3.8-a,b.

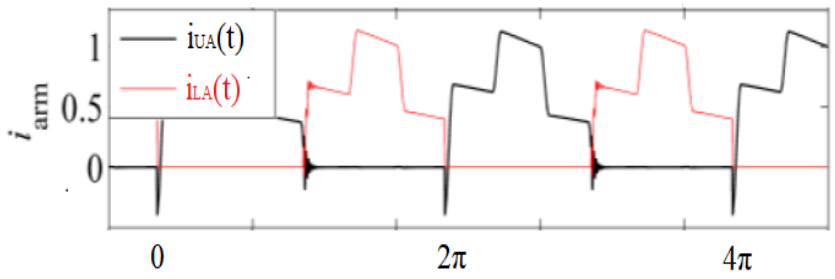


Figure 3.7: *Upper and lower arm currents [6]*

The primary side phase voltage, secondary side phase voltage and the average transferred power between the two MMCs can be expressed as shown in equation 3.14 and equation 3.15 respectively where $\alpha_{pG} = 1/2\omega(N_{SM\_P} - 1)T_d$ and $\alpha_{sG} = 1/2\omega(N_{SM\_S} - 1)T_d$. The choice of T_t for the primary and secondary MMCs

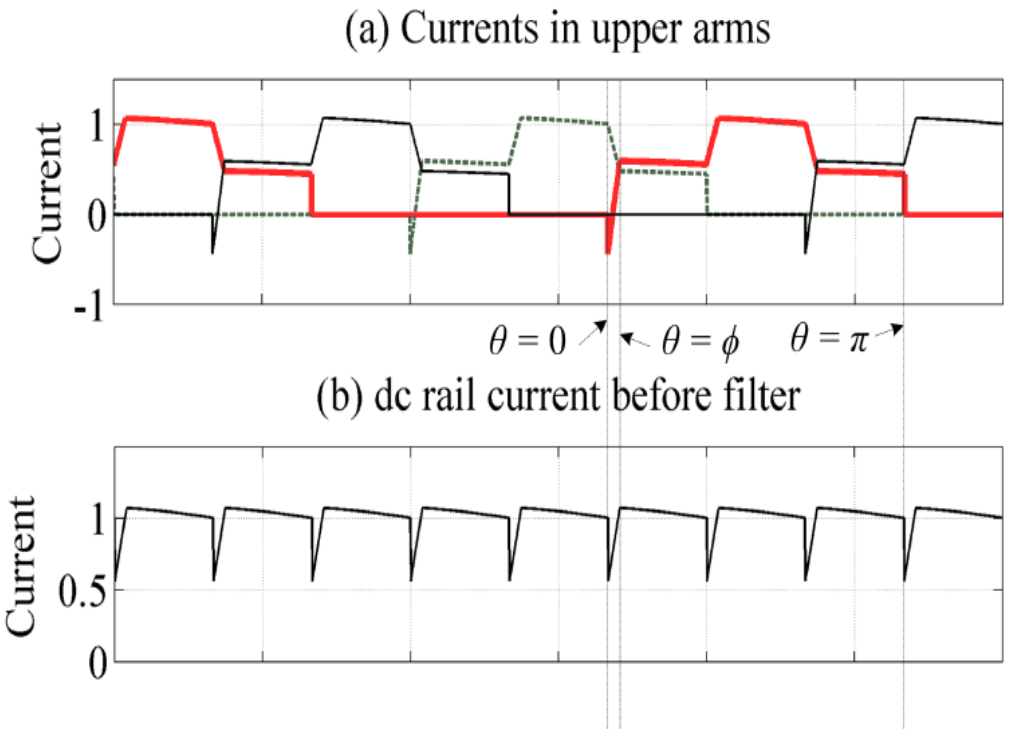


Figure 3.8: *Current waveforms: (a) Upper arms current (b) DC current without filter*

can be varied when the DC port voltages are not matched and it is selected based on the DC link voltage, AC link frequency and the choice of the voltage steps which will limit the $\frac{dv}{dt}$ stress on the transformer. The selection of T_t is always a trade-off in HVDC applications where a higher T_t will result in a lower voltage step and consequently a lower $\frac{dv}{dt}$ stress but a higher T_t will increase the energy storage requirements due to the increase in the SM capacitance and the size of the DC link filters. Additionally, the modulation index is lower with higher T_t and accordingly higher current rating devices are required for transferring the demanded power. Moreover, as a result of the lower voltage ratings of the semiconductor device and the requirements of the high number of the SMs in HVDC applications, the grouping of the SMs in each chain-link is essential to ensure that T_t is within an acceptable range. For example, in [4], the author suggested $T_t = 0.15\pi$ and $f = 250Hz$ for a 1.6GVA, 800kV DC port with a voltage step of 38kV. As a result, if each SM operates at 1.9kV and $T_d = 15\mu s$, 400 SMs are required in each arm and 20 SMs must be fired together at each step instant. Additionally, the required energy storage for the all SMs, H_{SM}, is, in this case, 6.4 ms assuming unity transformer turn ratio.

$$
\begin{aligned}
v_{AO1}(t) &= \frac{2V_{DCP}}{\pi} \sum_{k=1,3,5}^{\infty} \frac{sin(k\alpha_{pG})}{k^2\alpha_{pG}} sin(k\omega t) \\
v_{UO2}(t) &= \frac{2V_{DCS}}{\pi} \sum_{k=1,3,5}^{\infty} \frac{sin(k\alpha_{sG})}{k^2\alpha_{sG}} sin(k\omega t + k\varphi)
\end{aligned}
\tag{3.14}
$$

$$
P_{av} = n\frac{6V_{DCP}V_{DCS}}{\pi^2\omega L_k} \sum_{k=1}^{\infty} \frac{sin(k\alpha_{pG})sin(k\alpha_{sG})}{k^4\alpha_{pG}\alpha_{sG}} sin(k\varphi) \tag{3.15}
$$

The main advantage of the Trapezoidal operating mode over the sinusoidal operating mode is the reduction in the energy storage requirement which results in the reduction in the overall converter footprint. Theoretically, the TrMMC-DC-DC provides a significant reduction in the energy storage requirement, up to 85%, when compared to the sinusoidal operation of the MMC-DC-DC considering same peak to peak SM capacitor voltage ripple (10%). However, practically (even in simulation) a high sorting rate and low peak to peak SM capacitor voltage ripple (below $\leq$5%) are required in the TrMMC-DC-DC in order to avoid the high deviation of the SM capacitor voltage from nominal value. As a result, practically only up to 70% reduction in the energy storage requirements might be achievable in the HVDC systems.

However, there are some disadvantages of the trapezoidal operating mode in comparison to the sinusoidal mode. Firstly, the modulation index is limited to a narrow range and this means that the fundamental harmonic component of the ac voltage is fixed . Secondly, semiconductor device utilisation and current stress becomes significant, for example, one of the two semiconductor switches of each SM experiences the entire arm current and the arm current passes through the other switch only during transition period, T_t. Thirdly, the reduction in $\frac{dv}{dt}$ stress is limited and determined by T_d and T_t. Fourthly, a high sorting frequency (sorting almost at each level), and low peak to peak capacitor voltage ripple are required to prevent the divergence of the SM capacitor voltages reaches to an unacceptable value. This is

because during T_t, and a result of the small values of the SM capacitors, arm current can vary the SM capacitor voltages rapidly during T_t. This high sorting frequency will highly affect the switching losses and practically might be difficult to be implemented in the cases were only a few μs between voltage levels during T_t are present. Finally, the presence of the sixth harmonic in the DC current means that a bulky DC side filter is required and the semiconductor devices will experience high current stress during DC fault events. More details will be given in chapter 5 about the DC link filter and DC fault blocking performance of different converters.

3.2.2.3 Trapezoidal operation with soft switching for a single phase Modular Multilevel DC-DC converters

A single phase TrMMC-DC-DC with the soft switching capability is shown in figure 3.9. This was proposed by the authors of [65]. The soft switching is achieved by adding a small lossless snubber capacitor in parallel with each IGBT device. The voltage produced by each arm is similar to that of the two level three phase TrMMC-DC-DC shown previously in figure 3.4-b where the SMs are inserted and bypassed in order within a short period of time, T_t, and the SMs are inserted for only half of the cycle. The SMs in the upper and lower arms are inserted and bypassed in a complementary manner. However, the arm currents are continuous and this continuous arm current is achieved with the use of a bulky arm inductor and additional inductance in the AC link.

The advantage of this operating mode is that the continuous current in the converter arms provides better utilisation of the IGBT devices and there are a lower number of SMs when compared to two level, three phase trapezoidal operation. However, the added control complexity and the requirements of a bulky DC link filters and arm inductors combined with the challenge of building only one single phase transformer to support the full power flow are the main drawbacks of this operation even though the converter can be operated at higher fundamental frequency. The overall energy storage requirements are higher when compared to the three phase TrMMC-

DC-DC even at higher operating frequency.

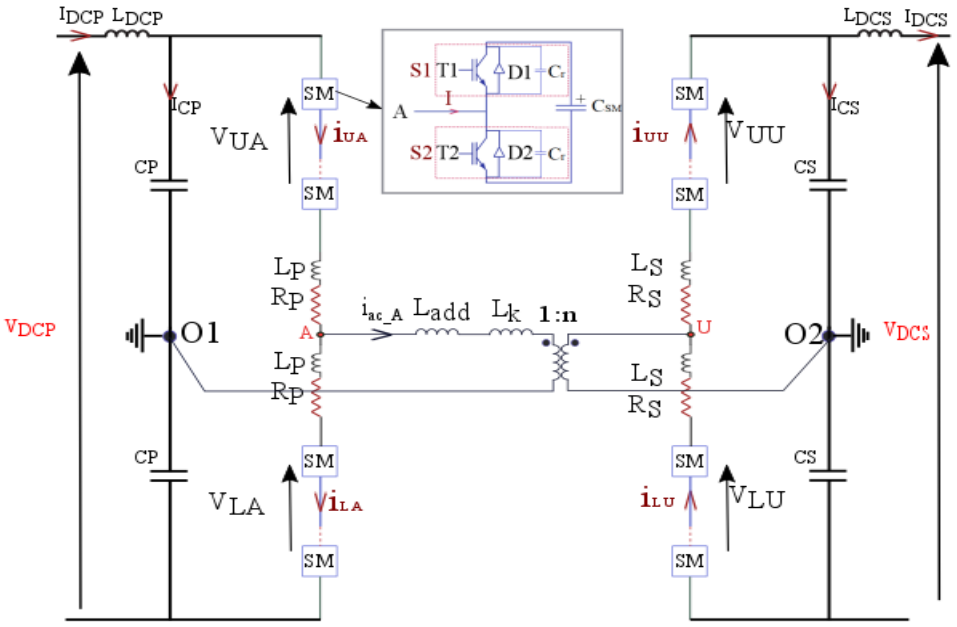


Figure 3.9: *Single phase MMC-DC-DC*

3.2.2.4 Alternative Arm Modular Multilevel DC-DC converter

The Alternative arm converter modular multilevel converter, AAC, was firstly proposed for the high voltage AC/DC conversion in [66] and was later adopted for the high voltage medium frequency (up to 400 Hz) DC-DC conversion in [57]. Figure 3.10 shows an alternative arm modular multilevel converter, AAC-DC-DC, where each arm consists of a number of series connected full-bridge submodules, FB-SMs, and a number of series connected "director" switches. Each arm operates for half of the cycle, π, and the phases are shifted by $2\pi/3$. Considering one phase, the director switches of both arms are overlapping for a short period to facilitate the smooth current commutation and SM voltage control. The use of the full-bridge SMs also enables the DC fault blocking capability. In comparison to the FB-MMC, an FB-AAC requires less full-bridge SMs, FB-SMs, as a result of the necessary voltage wave shaping being achieved in each arm of the converter. However, snubber circuits are required for the director switches in order for them to share the voltage stress during the off state.

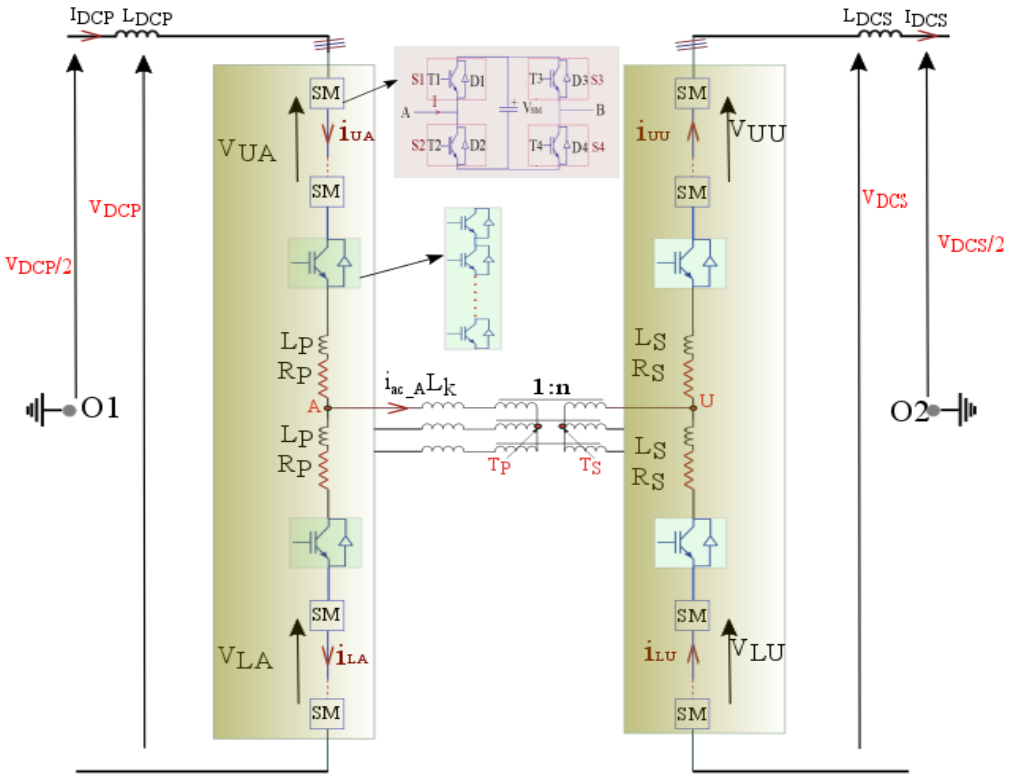


Figure 3.10: *Alternative Arm MMC-DC-DC*

Another advantage of the reduction in the number of FB-SMs is that the AAC-DC-DC converter requires a smaller physical footprint and has lower device losses when compared to the FB-MMC. Further reductions in the energy storage requirements is achieved when AAC-DC-DC is operated with trapezoidal modulation due to reduction in SM capacitor and arm inductor size. As a result, the trapezoidal ACC-DC-DC converter can be used in HVDC applications. However, it is less likely to be used in DC-DC converters because of its efficiency which is lower than the half bridge TrMMC-DC-DC converter even though the director devices are operated at zero voltage. The reason is mainly due to the use of a significant number of series connected devices in the conduction path resulting from the formation of these director switches.

3.2.2.5 Trapezoidal operation of the controlled transition bridge DC-DC converter (TrCTB-DC-DC)

The controlled transition bridge, CTB, converter was initially proposed with a trapezoidal modulation for the HVDC AC/DC conversion in [67]. The trapezoidal operation of the Control transitioned bridge DC-DC, TrCBT-DC-DC, shown in figure 3.11 was adopted later in [4]. Similar to a two level high voltage DC-DC series connected, director switches are used in each arm of the converter. However, a number of the series connected full-bridge SMs are used between DC link mid point (O1) and the output of the phase (A, B, C) to form a trapezoidal voltage waveform across the transformer with reduced $\frac{dv}{dt}$ stress. The FB SMs in each chain-link is used to produce $2N_{SM}+1$ levels and the chain-link is used only to block half of the DC link voltage in order to obtain a gradual stepped transition between $-V_{DC}/2$ to $+V_{DC}/2$ and vice versa. Therefore, the SM capacitors are designed for a voltage of $\frac{V_{DC}}{2N_{SM}}$ which is half of the SM capacitor voltage of the TrMMC-DC-DC.

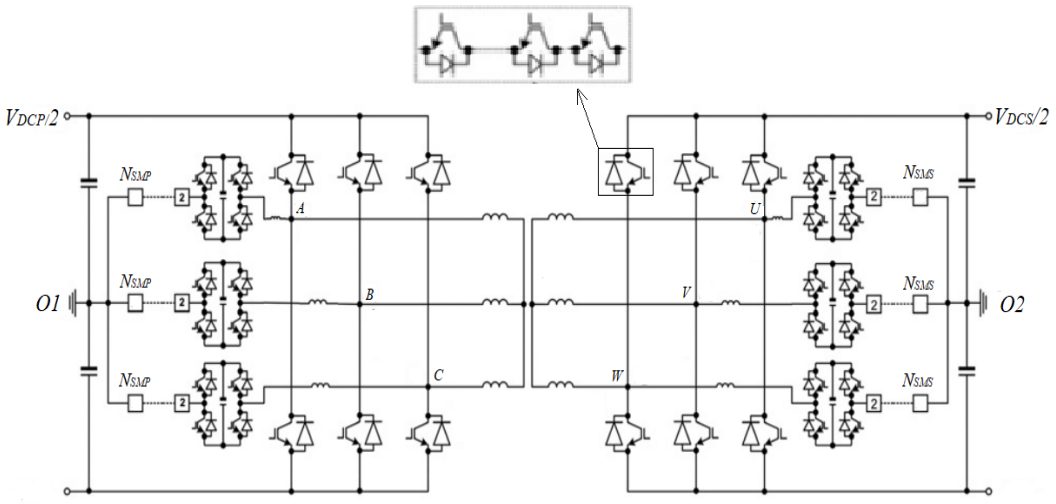


Figure 3.11: *Control transition bridge DC-DC Converter*

A Selective harmonic elimination (SHE) modulation scheme is used to minimize the circulating current and control the power flow through the converter. As a result, the operation of the converter is limited to a fundamental frequency in the $\leq 250Hz$ range. Bulky DC capacitor filters are required to smooth the DC current on both

sides of the converter as a result of the presence of a significant second harmonic component in the DC current.

Another trapezoidal mode of operation has been introduced in [6] as shown in figure 3.12. In this case, for the primary CTB, there is no connection between the FB chain-links (A, B, C) and the DC link mid point (O1). Similar to the previous TrCTB-DC-DC operation, trapezoidal operation of the FB chain-links produce $2N_{SM}+1$ levels and the SM capacitor voltage is $\frac{V_{DC}}{2N_{SM}}$. However, since there is no path for third harmonic component in the AC link current, arm current (direct switch current) and transformer voltage waveform will be very similar to that of the TrMMC-DC-DC. The advantage of this trapezoidal operation of the CTB is a reduction in the size of the DC link filters when compared to the operation shown in 3.11.

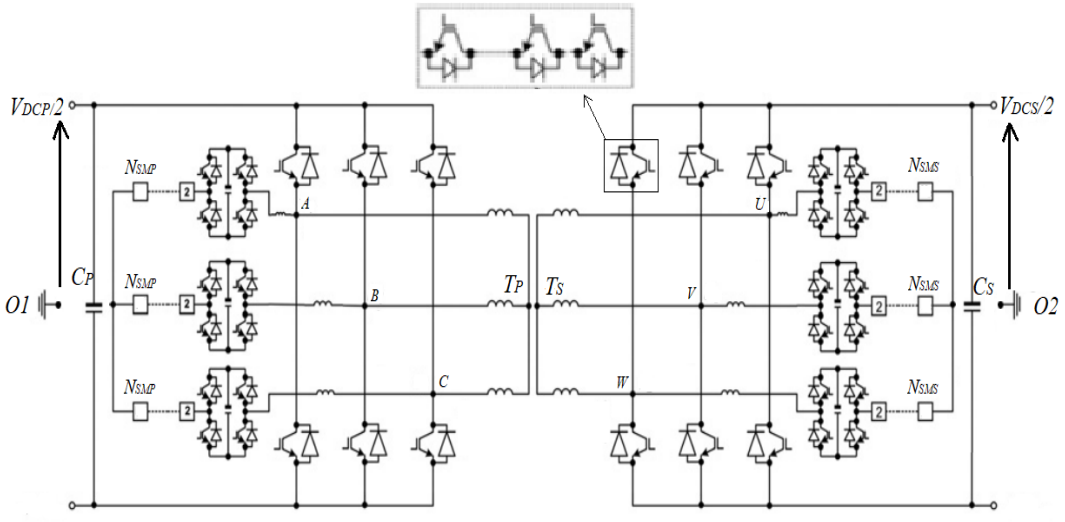


Figure 3.12: *Control transition bridge DC-DC Converter*

The main drawbacks of the TrCTB-DC-DC converter is the discharge of its DC link capacitors when a DC fault occurs which can cause high current stresses in the diodes of the director switches. The author in [6] suggested the use of the thyristor based valves instead of using the IGBTs in the director switches in an effort to overcome the problem of high current stress. However, using the thyristor devices may result in an increase in the energy storage requirements as a result of the lower

frequency harmonics present. This is a consequence of their inability to operate at high switching frequencies. In addition, small snubber circuits are required to share the voltage stress equally across the series connected director devices during transients, even though the voltage across the director valves increases gradually [6]. Finally, conventional high speed sorting is required almost at every voltage level in order to keep the SM capacitor voltages within an acceptable ripple envelope.

3.2.2.6 Transition arm DC-DC converter (TAC)

The Transition arm DC-DC converter shown in figure 3.13 was proposed in [68] for HVDC applications to achieve a further reduction in the overall energy storage requirements and physical footprint in comparison to the TrMMC-DC-DC, and TrCTB-DC-DC shown in [4, 5]. The upper arm of each of the phase consists of a series connection of the half-bridge SMs (HB-SMs) whereas a series connection of the semiconductor devices (IGBT) forms the lower arm. The HB-SMs in the upper arm are inserted for the majority of a half cycle and bypassed for the other half to achieve a control stepped transition between $-V_{DC}/2$ and $+V_{DC}/2$ (and vice versa) at the output of a phase in order to reduce the transformer $\frac{dv}{dt}$ stress. However, the director switches of the lower arm are only conducting when all of the SMs of the upper arm are bypassed (this is happening in phase A when $V_{AO1} = -V_{DC}/2$, for instance). The upper arm voltage, AC link current and the transformer voltage waveforms are similar to the TrMMC-DC-DC. However, only half of the HB-SMs are required for the same operating ratings in a TAC converter, resulting in a smaller footprint.

The drawbacks of the TAC converter are the loss of modularity on the lower arm, the requirement for snubber circuits to share the voltage stress across the director switches, and finally the high device current during a DC fault when the DC link capacitors discharge. The author in [6] proposed three different modified versions of the TAC converter to overcome the aforementioned disadvantages of the TAC and these modified structures are called, the hybrid TAC (HTAC), modular

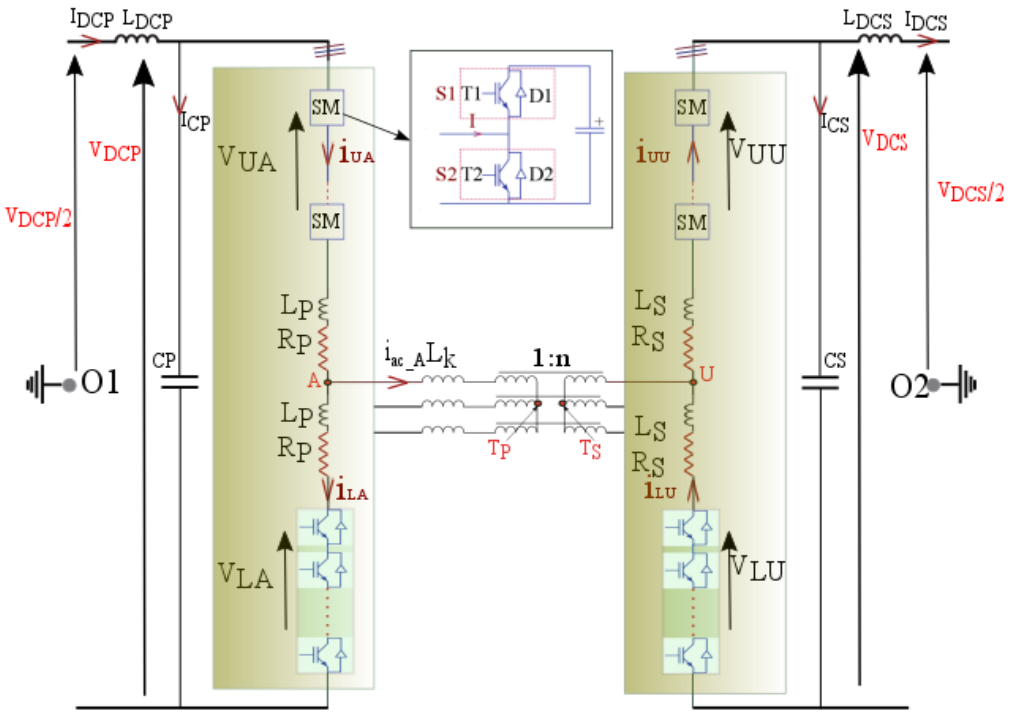


Figure 3.13: *Transition arm DC-DC converter*

TAC (MTAC) and the modular shunt TAC (STAC). These are shown in figure 3.14-a,b,c respectively. For all of the modified TAC structures, the AC link current and transformer voltage waveforms remain the same as those in the conventional TAC. However, the main differences include the structure of the arms, methods of the conduction in the arms and the SMs structure.

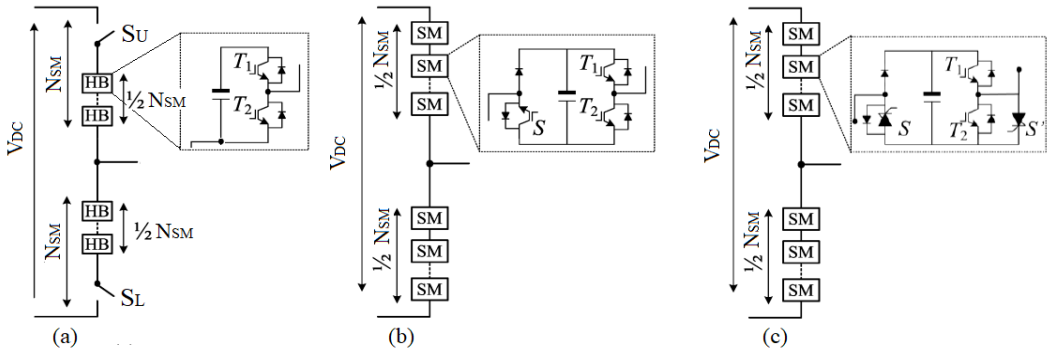


Figure 3.14: *Phase of transition arm DC-DC converter structures: (a) Hybrid TAC (b) Modular TAC (c) Modular shunt TAC [6]*

In a hybrid TAC structure, the HB-SMs and the series connected director switches are splitted between the upper and lower arms where the HB-SMs in each arm are

inserted for the half of the cycle and in a complimentary manner with the other arm. The series connected semiconductor devices S_U and S_L switch in a complimentary manner except for a short period where both series connected switches are ON as shown in figure 3.15. Integrated gate commutated thyristor (IGCT) devices are suggested for use in the director valves in an effort to cope with the high current stress during DC fault events. The modularity is divided between TAC arms but the arms are not fully modular and snubber circuits are still required for sharing voltage stress across the series connected devices.

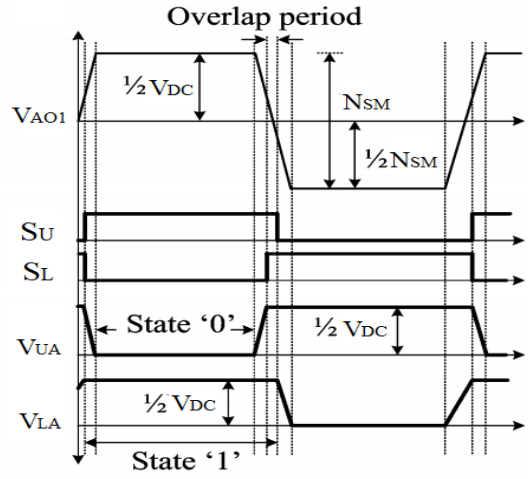


Figure 3.15: *Phase voltage, arm voltage and schematic sequence of HTAC and MTAC [6]*

In the modular TAC structure, the HB SMs are replaced by other SMs shown in 3.14-b. The arm voltage is similar to the HTAC where the conduction of the S in each SM of the upper and lower arm is similar to the S_U and $S_L$in the HTAC, respectively. In addition to the reduction in the energy storage requirements, the advantage of this approach is the full modularity and the absence of snubber circuits. The installed semiconductor VA requirement is almost the same as that for the TAC and HTAC. Similar semiconductor VA is required in TAC, HTAC and MTAC in comparison to the TrMMC-DC-DC and TrCTB-DC-DC configurations.

In a modular shunt TAC structure, the SMs are modified further as shown in figure 3.14-b. Integrated gate commutated thyristor (IGCT) is used to stand for the high $\frac{di}{dt}$

stress during a DC fault. Additionally, another IGCT, S', is used in parallel to one IGBT device, T2. as shown in figure 3.14 where IGBT devices are only used during the short period to achieve a control stepped transition whereas the IGCTs are used during most of the cycle. Since the conduction losses for IGCTs are usually lower than those for IGBTs (considering same power rating), this operation provides a higher efficiency in addition to the low energy storage requirements in comparison to the TrMMC-DC-DC and TrCTB-DC-DC. However, it requires a higher installed semiconductor VA requirement (roughly 12%) under the same operating conditions and has a lower semiconductor utilisation [6]. Finally, in order to keep the SM capacitor voltages within a low peak to peak voltage ripple (below 5%), a high speed sorting algorithm is needed. The limitation in reducing the $\frac{dv}{dt}$ stress across transformer and the use of integrated gate commutated thyristors (IGCTS) can force the converter to operate at a fundamental frequency of $\leq 250Hz$. These are the drawbacks of the TAC topologies.

3.2.2.7 Trapezoidal operation of hybrid cascaded two-level DC-DC converter

Figure 3.16 shows the DC-DC version of a Hybrid cascaded two level converter which was proposed in [69, 70]. The FB SMs in the AC path produce the two level voltage across the transformer with a small controlled, stepped transition between them to limit $\frac{dv}{dt}$. The number of FB SMs and the SM capacitor ratings are similar to the TrCTB-DC-DC shown in figure 3.11. However, the trapezoidal operation of the hybrid cascaded two-level DC-DC converter offers reverse DC blocking capability. The main drawbacks of this converter include:

- The high conduction loss, where twice the number of the SMs are in the conduction path when compared to the TrCTB-DC-DC.
- The significant DC link filtering requirements
- The non modularity of the director switches,
- The requirement of the snubber circuits to share the voltage stress among the

director switches

- The switching device current stress during DC fault events

Therefore, as a result of these issues, the hybrid cascaded two-level DC-DC converter is unlikely to be used in HVDC interconnections.

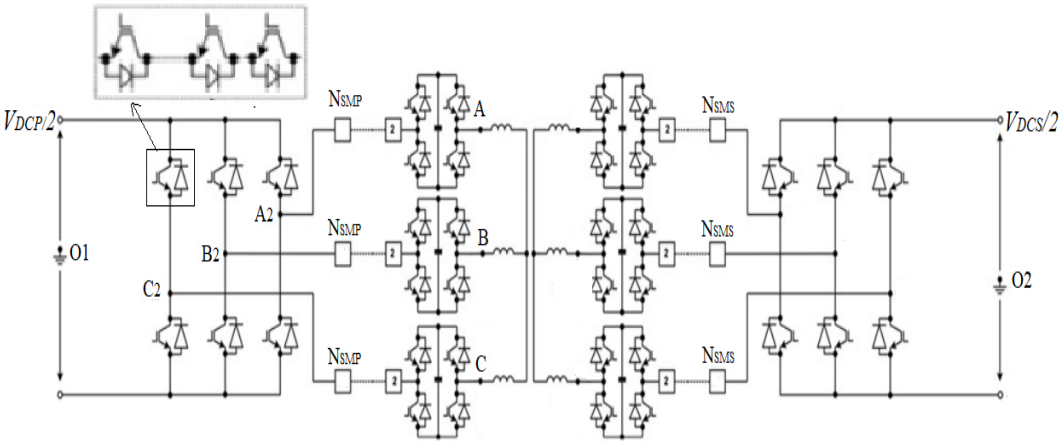


Figure 3.16: *Hybrid cascaded two level DC-DC converter*

3.2.3 Cascaded multi DAB DC-DC converters

Low voltage, low power DAB converters have been used as elementary cells to structure high voltage, HV, in cascaded multi DAB DC-DC converters [71]. Each DC-DC cell handles a portion of the total power and blocks a part of the high DC voltage. As a result, a series connection of the semiconductor devices is not required and lower current ratings can be used in comparison to the modular multilevel DC-DC converter structures.

Depending on the requirements of the application, the DC-DC converter cell can be connected in different ways as shown in figure 3.17. In a low voltage application, the parallel scheme is used (3.17-d), where the current is controlled to be distributed equally among the DAB cells. In a high voltage low power scenario, the series scheme is used (3.17-a), where the DC link voltage is shared between

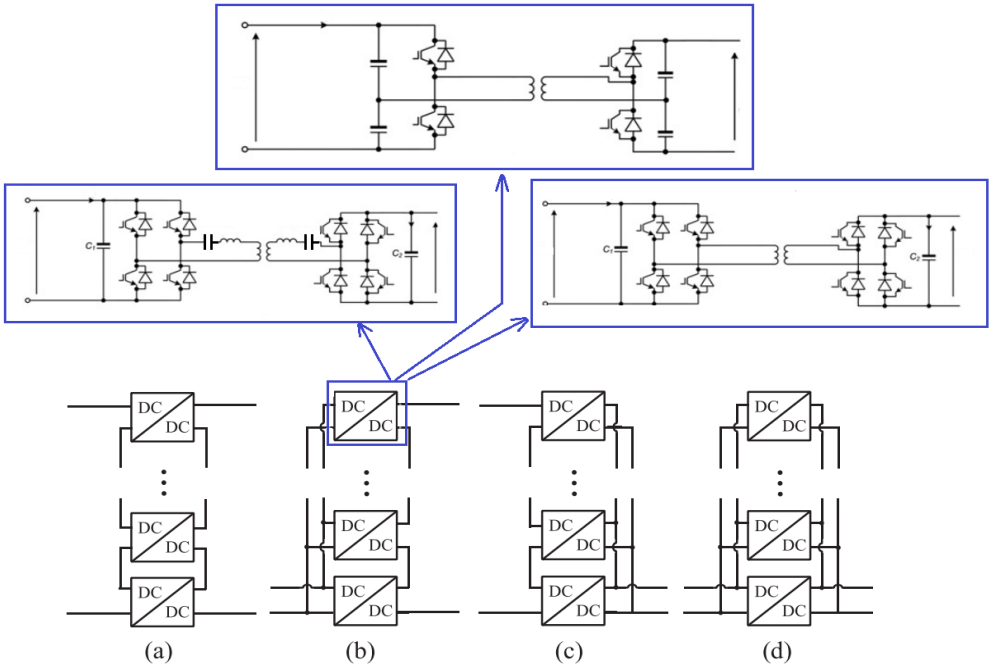


Figure 3.17: *Cascaded multi DAB DC-DC converter*

the DAB cells equally. For the high voltage applications with a DC transformation ratio, the structures shown in 3.17-b,c can be used for the power applications up to a few MW[72, 73]. However, in HVDC applications, the parallel and series schemes must be combined to achieve the high voltage and high power requirements [74, 75].

Different configurations of the DAB cell have been proposed in the literature, including the full-bridge cell, half-bridge cell and resonant full-bridge cell shown in figure 3.17 [76, 77]. Considering the same operating conditions, the half-bridge cells require less semiconductors but a much larger DC filter in each of the cell when compared to a full-bridge cell; therefore full-bridge cells are preferred. The soft switching capability of the resonant cells make the operation of the DAB possible at a higher frequency in comparison to the other cells (full-bridge or half-bridge cells). This can help to reduce the size of the converter components such as the transformers and filters. However, the main drawbacks of the resonant full-bridge cells is the high voltage across the series resonance tank component and the more complex control requirements over a wide load range.

In comparison to a modular multilevel structure, the cascaded multi DAB DC-DC converter can be operated with a higher fundamental frequency (usually $f > 1kHz$) and lower rated semiconductor devices. However, the main disadvantage associated with the cascaded multi DAB DC-DC converters, especially when used for HVDC applications, is the need for a large number of transformers with varying isolation levels to the real ground as a result of the cascaded nature of the structure. Therefore, the use of cascaded multi DAB DC-DC converters is usually limited to the medium voltage applications although it has been proposed for the use in the HVDC systems [40].

3.3 Non isolated high power DC-DC converters

There is a large number of the non isolated DC-DC converter topologies which were proposed for HVDC applications. This section will briefly focus only on the DC-DC converter topologies employed for HVDC interconnections where the DC voltage ratio is in the low, $0.8-1.5$, and medium, $1.5-5$, ranges. The non isolated DC-DC converters is classified as a type of DC auto-transformer but includes some resonant and modular based DC-DC converters.

3.3.1 DC auto transformer

Two high voltage DC-AC converters are connected in series from the DC sides and interconnected through a low or medium frequency transformer, $f = 50\ Hz - 500\ Hz$, on their AC sides to produce a DC auto-transformer as shown in figure 3.18. The existing high voltage converters, two level, three level, MMC and LCC converters are applicable to a DC auto transformer implementation. The AC link in the DC auto transformer topologies is used to transfer a portion of the power and the other fraction of the DC power flows directly through the common mode DC currents. The main features of the DC auto-transformer include a reduced voltage rating of the semiconductor devices, lower transformer ratings (voltage and power) and the reduced power losses [7, 8]. However, these features are less significant as

the DC transformation ratio is increased. Therefore the use of DC auto transformer is limited to the low transformation ratios in HVDC interconnections and medium transformation in the MVDC systems when isolation is not required.

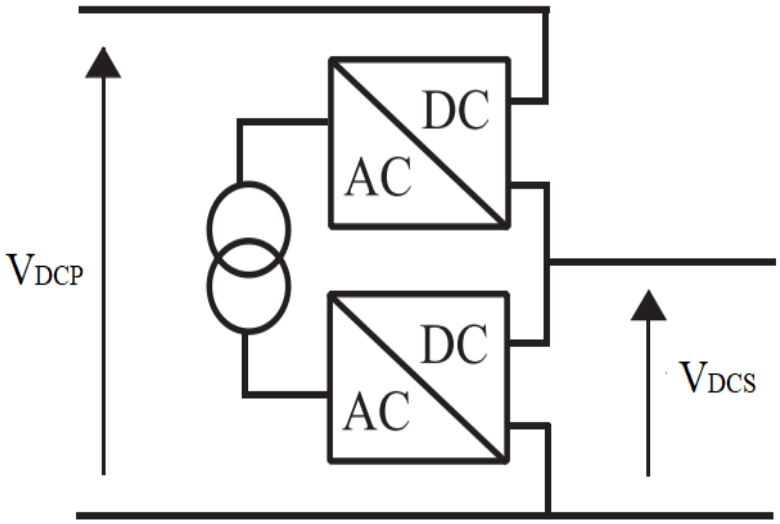


Figure 3.18: *DC auto transformer [7, 8]*

Figure 3.19 shows the MMC based DC auto transformer and the power transferred through AC link is, $P_{ac} = (V_{DCP} - V_{DCS})I_{DCP} = P_{DCP}(1 - N_{dc})/N_{dc}$ where $N_{dc} = V_{DCP}/V_{DCS}$. The remaining power is transferred through the common mode DC currents in each phase of the MMCs [9].

3.3.2 Resonant high voltage DC-DC converters

Resonant LC tanks are used to achieve voltage regulation and soft switching of the semiconductor devices at the same time in HVDC applications where a medium and high transformation ratio is required. The resonant high voltage DC-DC converters can be mainly divided into the single stage and multi stage systems based on the number of the required LC tanks.

3.3.2.1 Resonant single stage DC-DC converters

Figure 3.20 shows a single stage resonant HV DC-DC converter proposed in [10] where the connection of the two thyristor based full bridges is used to provide bidi-

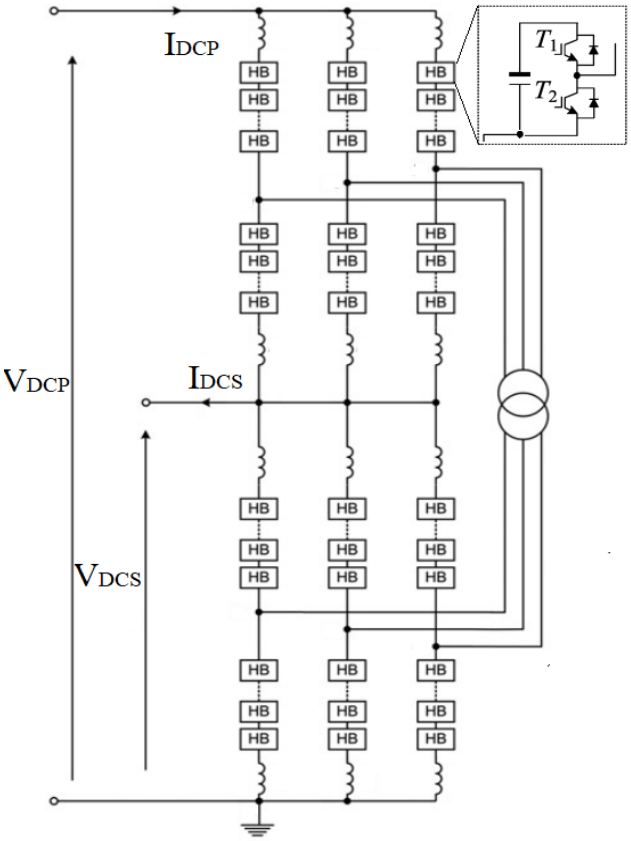


Figure 3.19: *Modular multilevel DC auto-transformer [9]*

rectional power flow. The LCL resonant tank is used to achieve a step up in the voltage and the potential for the soft switching of the semiconductor devices. In [78], the author proposed a parallel resonant LC tank with a voltage doubler to achieve the voltage regulation and the soft switching of the devices.

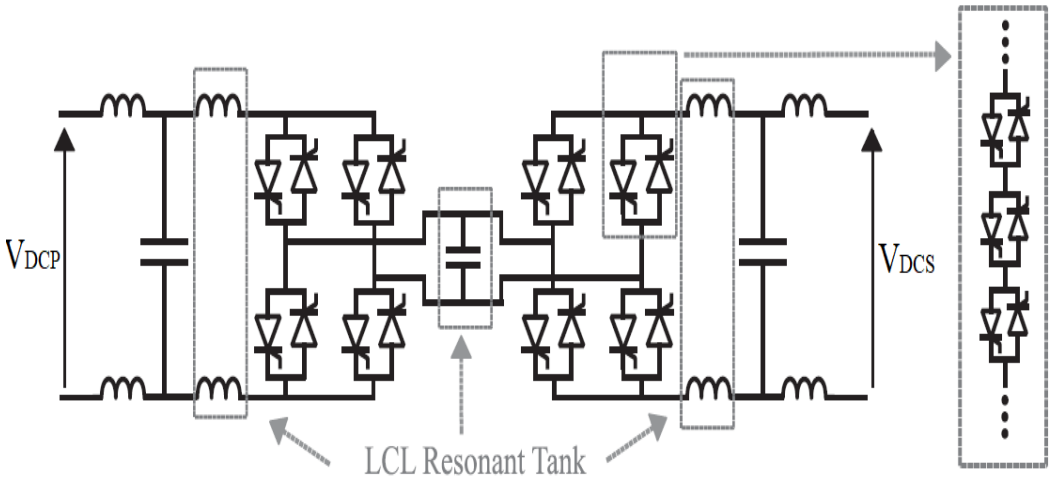


Figure 3.20: *Resonant single stage HV DC-DC converter [10]*

These single stage resonant converters are proposed for the high and medium transformation ratios without the need of isolation. However, the issues of this type of the converter is the high electrical ratings of the resonant tank components- they must be rated for the high voltage and the high current. Another disadvantage of these converters is the poor utilisation of the semiconductor devices which are placed on the lower voltage side where the series connected thyristors must be rated at maximum voltage across the capacitor of the resonant tank (1.2 to 1.4 higher than nominal rated voltage). As a result, the single stage resonant converters are limited to the medium power and medium transformation ratio.

3.3.2.2 Resonant multi stage DC-DC converters

In the resonant multi stage DC-DC converters several low power resonant tanks are used instead of using one central high rated high power resonant tank. The tanks will be activated sequentially and the power will be successively transferred between the tanks until it reaches the other side of the converter. Consequently, the complexity of the tank will be reduced in comparison to the single stage [34, 79–81]. In [81], the low voltage AC is generated on the low voltage DC link side and several capacitors are charged to regulate the voltage on the other side of the converter. In [34, 79] the capacitors are charged to a relatively low voltage when they are connected in parallel and then deliver the power when they are connected in series at a higher voltage.

The high electrical stress on the resonant components is reduced in a resonant multi stage DC-DC converter, even at high transformation ratios. However, the main issue is the unequal voltage and current distribution stress across the semiconductor devices. As a result, the modular structure cannot be achieved, even with resonant multi stage converters, hence, it is unlikely to be used in HVDC interconnections.

3.3.3 Non isolated modular DC-DC converters

The modular concept of an MMC is employed in plenty of the non isolated DC-DC converters which can be used for HVDC applications. These modular DC-DC converters can be classified into two main sub groups. DC modular multilevel, DC-MMC, is the first group, where the topologies operating principle is based on the MMC. The second group of the converters operates similar to a chopper in the lower power circuits and the DC motor drives.

3.3.3.1 DC modular multilevel converters

Similar to an MMC, the principle operation of the topologies in this group is based on the chain-links which produce a controllable voltage source at the required frequency. In these converters two current loops, a DC current loop and an AC current loop, ensure converter operation where the AC current loop is used to balance the stored energy in the chain-links and the DC current loop is used to transfer the power between the DC links [82–87]. Based on the operation of the topology, either filters or control actions and more SMs are required to avoid the presence of the AC current component in the DC link where filters have been used in the topologies proposed in [82, 84, 87]. Control actions with more SMs were used in the topologies proposed in [83, 85, 87].

The advantages of the DC-MMC converters are modularity, reliability and scalability to meet the requirements of HVDC applications. Although, large numbers of the series connected SMs are used in the DC-MMCs, the DC-MMCs cannot be operated above the medium frequency ($\approx 250Hz$) due to the hard switching of the SM semiconductor devices. As a result, the requirements of the bulky filters, large numbers of the SMs and the SMs with a high energy storage are the main drawbacks of these topologies. DC-MMCs are limited to the low and medium transformation ratios due to the potentially high AC circulating currents which increase the energy storage requirements and the losses in the converters.

3.3.3.2 Chopper based modular DC converters

The principle operational difference of chopper based modular DC converters is simply the use of the series connected SMs instead of switches as in the classical choppers. The use of the chain-links in the choppers provides more features in control and operation [11–13, 88]. The employment of the SMs and energy storage elements splits the chopper based modular DC-DC converter into the capacitive accumulation choppers (hybrid cascaded DC converters) and inductive accumulation choppers.

Hybrid cascaded DC converters (modular capacitive accumulation choppers)
The principle operation of a hybrid cascaded DC converter is based on the charging and discharging of the SM capacitors in order to transfer power between DC ports. The author in [11] proposed three possible cascaded DC converters as shown in figure 3.21. In figure 3.21-a the positive terminal of the DC ports are connected by a six pulse bridge of a two level converter and the half-bridge SMs are connected to the negative terminal of the DC ports or ground. The chain-links are rated at the HVDC link voltage levels in order to be able to provide the alternative switching between the DC links. The voltage across the series connected semiconductor devices is difference between the DC link voltages and this reduces the loss of the converter. However, the main disadvantage is the modularity since the hybrid cascaded DC converter are not fully modular due to the use of the six pulse bridge two level converter in their operational modes. Another disadvantage is the high current stress in both the diodes of the director switches and the main switches of the SMs during a DC fault. As a result, this configuration is less likely to be adopted for HVDC interconnection.

In figure 3.21-b and 3.21-c the two level converter is employed in a high voltage DC terminal ($V_{DCP} > V_{DCS}$) and the SMs at a low voltage DC terminal. The use of FB chain-links generates bipolar AC voltage and produces a low voltage DC termi-

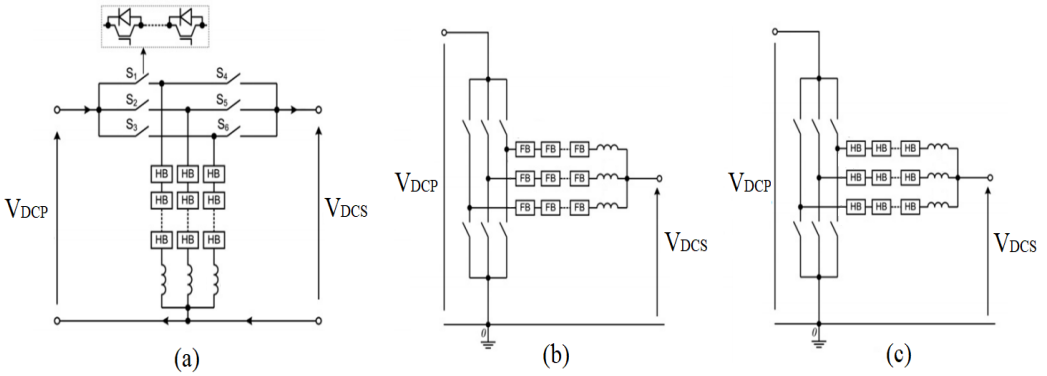


Figure 3.21: *Non isolated hybrid cascaded DC-DC converters [11]*

nal without ripple. However, the use of HB SMs produces uni-polar AC voltage. In both types the chain-links must be rated to support the HVDC side and the series connected semiconductor devices must block the full HV terminal. As a result, more devices are required in comparison to the configuration shown in 3.21-a, Furthermore, an increased umber of the devices in the conduction path, resulting in higher conduction losses. However, the advantage of these configurations (b, C) is the DC fault blocking capability.

Modular inductive accumulation choppers

The inductor is the key element, required to transfer energy between DC ports in modular inductive choppers. The SMs are used to facilitate charging and discharging the central inductors. The insertion of the SMs depends on the applications where in the topology proposed in [88], trapezoidal insertion of SMs is used to change between the charging state and discharging state of the central inductor. The interleaved insertion of the SMs was proposed in [12] and [13] in order to achieve the resonant operation and resonant discontinuous conduction operation, respectively. Soft switching of the SMs is partially achieved in the resonant operating mode where IBGTs are hard turn-off and soft turn-on, and Diodes are soft switching. The soft switching of the SMs is achievable under the trapezoidal operation of the modular inductive chopper only at operating conditions with high AC circulating current which significantly increases the conduction losses in addition to the increase in the energy storage requirements.

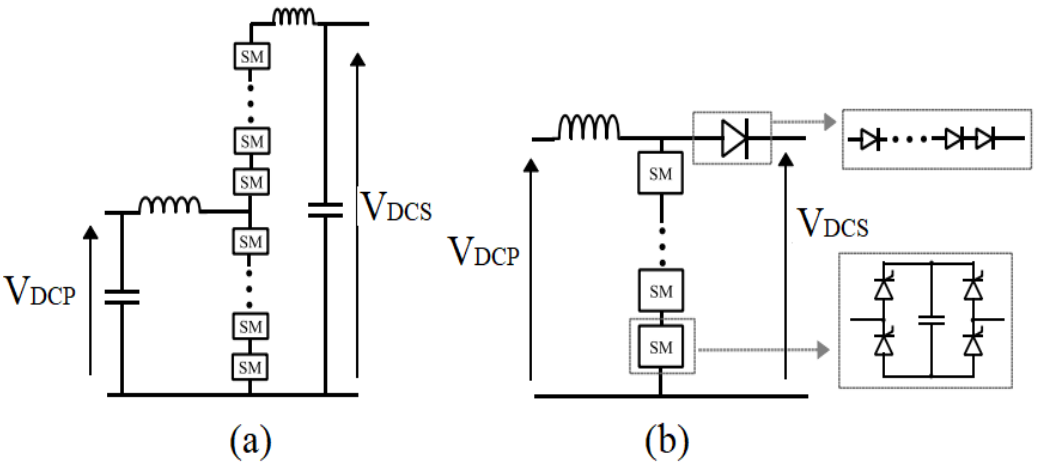


Figure 3.22: *Modular inductive choppers: (a) proposed in [12], (b) proposed in [13]*

Although, the modular inductive choppers provide modularity and a high transformation ratio, the requirement of extreme bulky DC link filters and central inductors limits their operation at low power. Therefore, they are unlikely to be used for HVDC interconnection and they can be adopted only for tapping energy from the HVDC systems.

3.4 Summary

This chapter focused on the DC-DC converters which are able to be applied in HVDC interconnection applications. The isolated DC-DC converter topologies and non isolated DC-DC converter topologies were explained in detail. Although, the absence of a transformer in most of the non isolated topologies gained interest in terms of the converter footprint, the requirements of significant filters in some of them and non modularity in others made their use limited. It was shown that in addition to the voltage regulation and isolation, the use of the isolated DC-DC converters helps to achieve the fault blocking capability and interconnect HVDC systems with different configurations, different converter types and various grounding schemes.

Moreover, the advantages and challenges of the different operating modes and topologies of the DC-DC converters were shown. The two level and modular multilevel

converters were explained where the main challenges of the two level topology were the $\frac{dv}{dt}$ stress on the transformer insulation, non modularity, and the requirements of the auxiliary snubber circuit to share the voltage stress among the individual switches. It was also shown that the use of the conventional operation of a modular multilevel DC-DC converter overcomes the problems of $\frac{dv}{dt}$ stress, reliability and modularity. However, this may be at the cost of the high energy storage components and high semiconductor *VA* product requirement (*VA* reflects the cost and area of the semiconductor). As a result, the conventional operation of the MMC-DC-DC converters ends with a large footprint.

In addition, this chapter presented the trapezoidal operation of the modular multilevel converters which reduced the size of the SM capacitors. However, large DC link filters are required under these conditions and the converter has a poor device utilisation. Furthermore, a group of the recent modular multilevel converters, TAC, TrCTB-DC-DC, that operate with trapezoidal waveforms was shown and these converters provided further reduction in the semiconductor *VA* product requirement, energy storage requirements and semiconductor losses. However, the challenges with the trapezoidal operating modes for the modular multilevel topologies are the devices current stress during DC faults, DC link filter requirements and the requirement of the high speed sorting algorithms to prevent the divergence of the SM capacitor voltages during the transition period, T_t.

In next chapter a modified trapezoidal operation of the modular multilevel DC-DC converter based on the resonant operation will be presented where the DC link filters will not be required and better utilisation of the semiconductor devices with lower devices current rating is achieved. Furthermore, the SM capacitor voltages will be sorted at the fundamental frequency with no additional switching losses.

Chapter 4

Modified Trapezoidal Operation of the Modular Multilevel DC-DC Converter

4.1 Introduction

Trapezoidal operation of the three phase modular multilevel DC-DC converter, TrMMC-DC-DC, was presented in the literature review and is one of the most promising topologies for HVDC interconnection due to its modular structure, reliability and low energy storage requirements. However, the poor semiconductor device utilisation and the need for a bulky DC link filter are significant drawbacks. Additionally, the need for a high sorting frequency during the transition period is likely to give rise to increased semiconductor losses. To address these issues, a modified trapezoidal mode is introduced in this Chapter. In this modified mode a dc filter is not required and better semiconductor devices utilisation is achieved. Additionally, a lower sorting frequency of SM capacitors (SMs are sorted at fundamental frequency) is possible, and the required semiconductor *VA* is reduced.

A detailed description of the modified trapezoidal operation of the three phase mod-

ular multilevel DC-DC converter topology is provided in this chapter, showing an analysis of arm, phase and ac link voltage and current waveforms. This chapter also addresses the converter energy storage and the selection of the MTrMMC-DC-DC components. A new method for submodule capacitor voltage balancing is presented, along with a novel approach for controlling arm energy. In addition, the device utilisation is considered.

4.2 Principle of operation of the MTrMMC-DC-DC

Trapezoidal operation of the three phase MMC-DC-DC converter was briefly introduced in the previous chapter where it was shown that the operation is similar to the Alternate Arm Converter (AAC) with the converter arms conducting for half of the AC supply period [5]. This mode of operation reduces the $\frac{dv}{dt}$ stress of the converter but with some limitations and requires high sorting frequency for inserting/bypassing the SMs during the transition period to achieve low energy storage requirement. However, this new trapezoidal operation is based on the resonance between equivalent effective capacitor of the arm converter with the arm inductors to keep firstly the low energy storage requirements. Secondly, it provides continuous conducting of the converter arms which results better semiconductor devices utilisation and reduces the semiconductor *VA* requirement. The continuous conduction of the converter arms using the proposed mode eliminates the dc link filters where the dc link current will be smooth even if the transmission line inductance is neglected. In addition, the SMs are inserted and bypassed at fundamental operating frequency with the modified trapezoidal operating mode.

A three phase DC-DC converter with a Y-Y coupling transformer is considered in this chapter and, based on the transformer neutral point with respect to the dc link midpoint, either two-step or six-step trapezoidal ac voltage can be produced across the transformer. Figure 4.1 shows two possible configurations of the converter. In the arrangement of 4.1-a the transformer neutral is connected to the DC link mid-

point and 2-level waveforms are produced across the transformer. A significant disadvantage of this connection is that triplen harmonics flow into the neutral connection and they also appear in the DC link current. Therefore the configuration of 4.1-b is preferred where the transformer neutral is floating. Waveforms corresponding to this arrangement are shown in Figure 4.2-a.

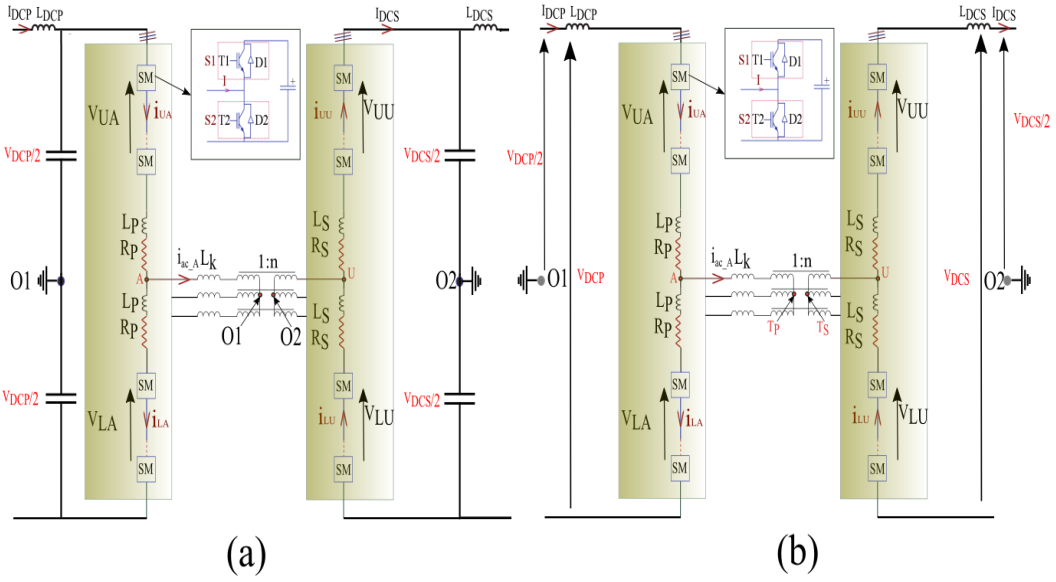


Figure 4.1: *Modified trapezoidal operation of MMC-DC-DC configurations:(a) Grounded transformer mid point (b) Ungrounded transformer mid point*

Frequency spectra of the six-step trapezoidal ac voltage waveforms and the ac link current waveform are shown in figure 4.2-b where it can be observed that the triplen components are eliminated. This configuration eliminates dc link filters but considering the same transferred power, the peak current is higher than the two-step trapezoidal ac voltage configuration. Additionally, it was demonstrated in [89], that the flux pattern generated by the six-step ac voltage in the transformer core is close to the flux pattern produced by the sinusoidal voltage and this is another advantage of six-step voltage configuration over the two-step voltage configuration if iron loss of the transformer is considered. More analysis can be done on the transformer design, however, since the focus here is on the operation of the converter, the component size, semiconductor *VA* requirement and semiconductor device utilisation, the three phase transformer design will not be considered in this thesis.

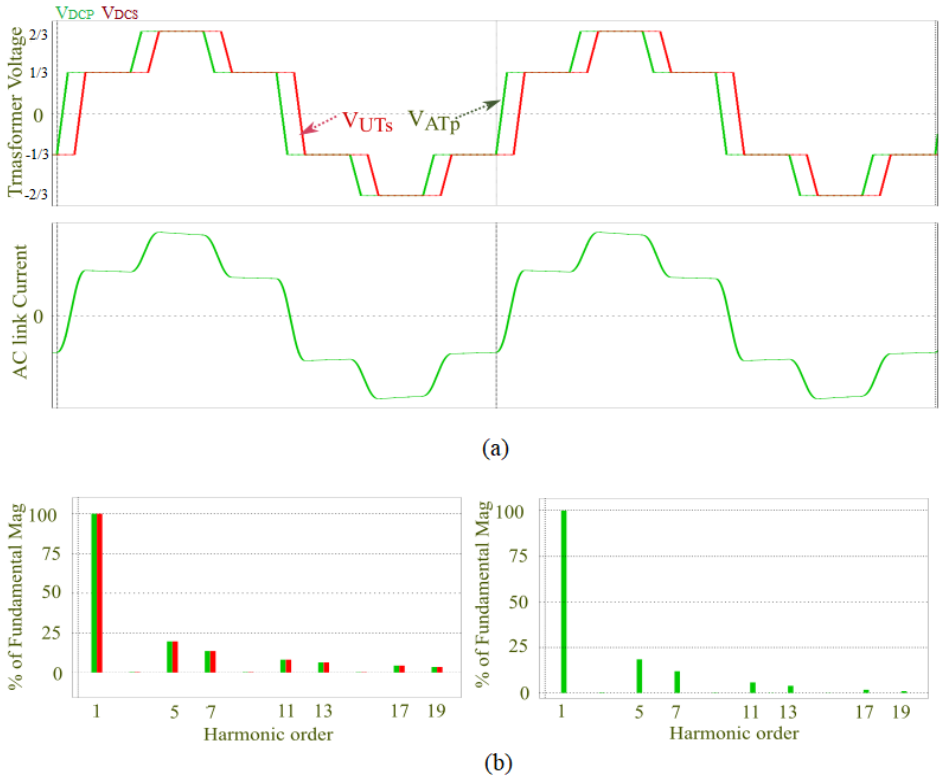


Figure 4.2: *MTrMMC-DC-DC with six-step AC link voltage waveforms: (a)Trapezoidal ac link voltage and current (b) FFT of six-step AC link voltage and AC link current waveforms*

4.2.1 Arm and phase trapezoidal voltage waveform

The ideal arm voltage waveforms of the primary and secondary MMC are trapezoidal using half bridge SMs in each arm. Table 4.1 shows the possible conduction states of the devices depending on whether the SM is inserted or not. Figure 4.3 shows phase A of the primary MMC where each arm is operated using trapezoidal modulation shown in figure 4.4 where ω is the angular frequency and T_t is the transition time between 0 and V_{DCP}. The arm voltage waveforms of the phases B and C are lagging the arm voltage waveforms of the phase A by $2\pi/3$ and $4\pi/3$, respectively. As shown, the SMs in each arm are inserted for the majority of the half of the cycle and are bypassed for the other half of the cycle. The insertion pattern is complimentary between the upper and lower arms. The transition between voltage levels 0 and V_{DCP} of the arm voltage is stepped over a short transition time during which the phase voltage steps between $-V_{DCP}/2$ and $+V_{DCP}/2$ with respect to dc link midpoint, V_{AO1}.

Table 4.1: Half bridge possible states

I →	V_{AB}	On Switch	On Device
A → B	V_{SM}	S_1	D_1
A → B	0	S_2	T_2
A ← B	V_{SM}	S_1	T_1
A ← B	0	S_2	D_2

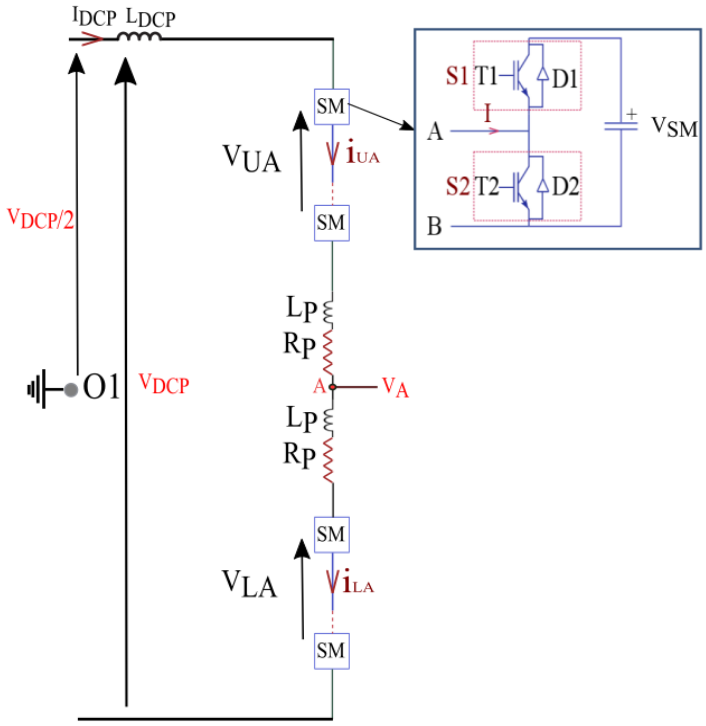


Figure 4.3: *Phase A structure of MTrMMC-DC-DC*

The multilevel arm voltages waveform can be generated using N_{SM} (N_{SM} is the number of the SMs per arm) fixed 50% duty cycle signals, shifted by a small angle θ, at fundamental frequency to gate the submodule switches as presented in figure 4.5-a [90]. However, the Author presented a method with uneven distribution of duty cycle to modulate the submodule switches in [91]. Figure 4.5-b shows the duty cycles of the N_{SM} gate signals for this uneven distribution method. The gating pattern starts with the maximum duty cycle $\pi + (N_{SM} - 1)\theta$ and reduces by 2θ for each SM until it ends with the minimum duty cycle of $\pi - (N_{SM} - 1)\theta$. This method of modulated arm signal is preferred since the submodule capacitors voltage are balanced faster

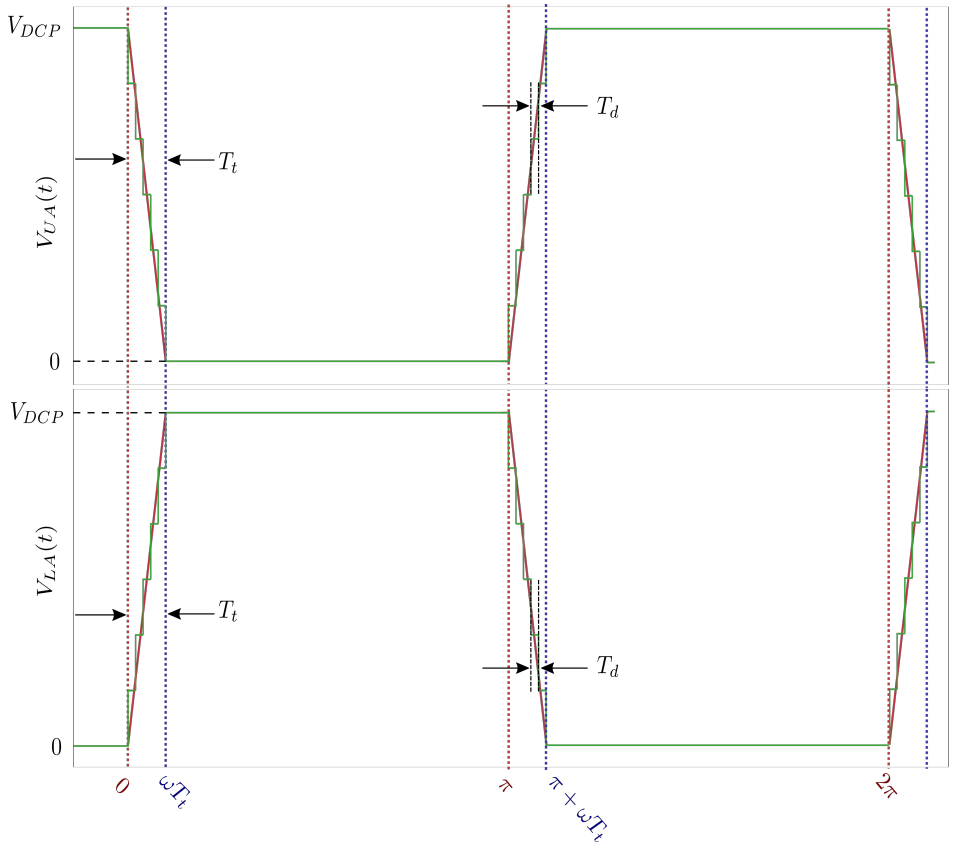


Figure 4.4: *Ideal upper and lower arm voltage waveforms of phase A MTrMMC-DC-DC*

than previous method. Additionally, this method is more adaptable with the proposed energy controller of the SM capacitors since no additional switching could be achieved during the transient period until the control over the energy is achieved. A new energy control method for the SM capacitors is proposed by the Author and it is explained in detail in later sections of this chapter. Additionally, the capacitor voltage balancing method will be explained and supported by theoretical analysis of the charge distribution and by a PLECS simulation.

The selection of dwell time, $T_d = \theta/\omega$, between voltage level transitions must be as small as possible to reduce the size of the SM capacitors for a desired voltage ripple. Accordingly the converter footprint will be reduced but the switching speed compatibility of the devices (IGBTs) must be considered when T_d is selected. On the other hand, $\frac{dv}{dt}$ stress across the transformer insulation is determined by T_d and therefore it must be large enough to prevent unacceptable $\frac{dv}{dt}$ stress. An analysis

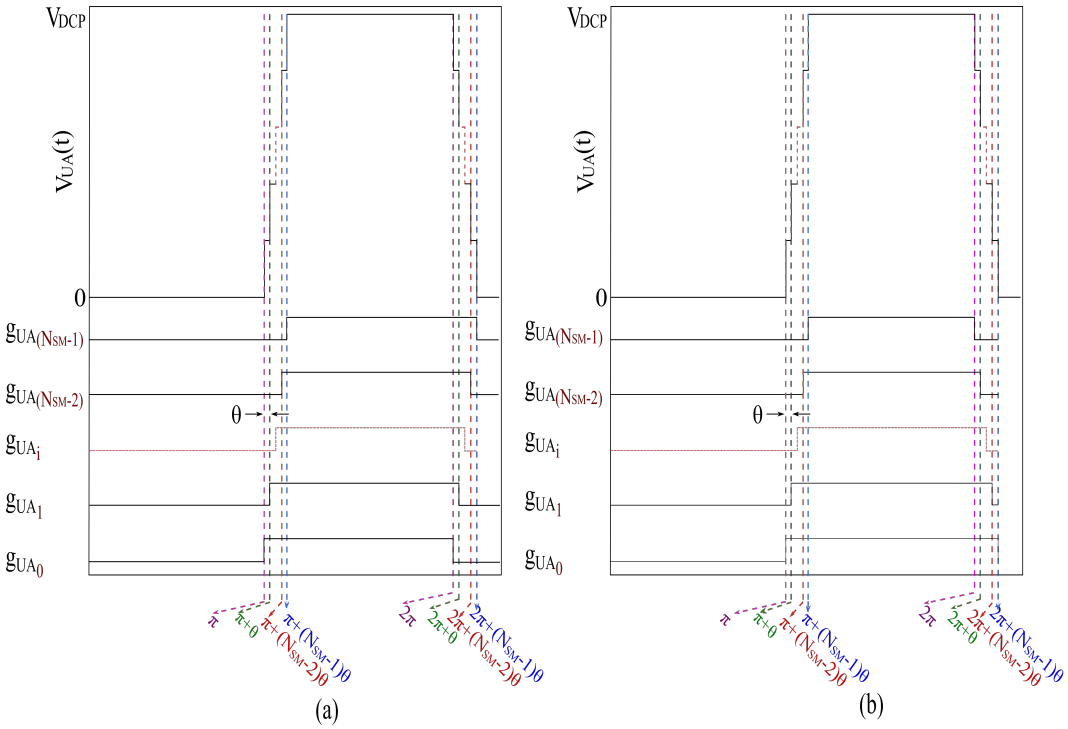


Figure 4.5: *Arm voltage generation: (a) fixed 50% duty cycle of gate signals (b) uneven distribution of different gate signals*

concerning the effect of the selection of both T_d and T_t on the trapezoidal phase voltage waveforms and energy storage requirements will be shown in next sections.

4.2.1.1 Grouping of submodules in trapezoidal arm voltage waveforms

The DC link voltages are several hundreds of kV in HVDC applications and considering the voltage rating, a few kV, of the insulated gate bipolar transistors, IGBTs, hundreds of half bridge SMs will be required in each converter arm to block the dc link voltage. Sequential switching of hundreds of SMs in each arm with even a small dwell time, $T_d = 5\mu s$, will result in a high transition time interval, T_t, between the two dominant voltage levels, 0 and V_{DCP}. As a result, a significant part of the fundamental period will be occupied by T_t even at medium operating frequency, $250Hz$. Consequently, the fundamental component of the ac voltage will be reduced and for the same transferred power, higher current will flow through the SM capacitors. In order to keep the SM capacitors voltage ripple within a certain limit, higher capacitance will be required. Ultimately, the converter footprint will be excessive due to the extra required energy and higher IGBTs current rating.

In order to overcome the stated challenges, T_t must be reduced and, theoretically, reducing T_d to 1µs or less can minimize the T_t. However, the value of T_d is bounded by switching delays of the IGBTs and a violation of $\frac{dv}{dt}$ stress must be avoided. For instance, consider a case when the FZ1500R33HL3 3.3kV 1500A IGBT module is used in the half bridge SMs and the IGBT devices are switched with a dead time ≈ 0.5µs to insert and bypass the SM. From the datasheet it is found that the required time to turn off the device including fall time is, $t_{off}+t_f = 5$µs and the turn on time including rise time is, $t_{on}+t_r = 1$µs. Therefore, in order to alter the state of the SM at any instant the switching process of the SM must be initiated $t_{off}+t_f$ before that instant. It may be possible to choose $T_d < t_{off}+t_f$ since all IGBTs are subjected to turn-off delay and this may be achieved by initiating the gate to switch the next SM state before the current SM has actually switched its state. However, since the delay in the gate driver circuit and $t_{off}+t_f$ of the devices are not identical, choosing $T_d < t_{off}+t_f$ could overlap voltage steps and consequently a violation in $\frac{dv}{dt}$ stress could occur.

Alternatively, the reduction in transition time, T_t, can be achieved by grouping SMs and choosing $T_d \geq t_{off}+t_f$ where each group consists of number of SMs which are inserted or bypassed at the same instant. As a result the arm and phase voltage levels will be reduced from $N_{SM}+1$ to $N_{st}+1$ where N_{st} is determined as equation 4.1 and N_L is the number of SMs per group or per voltage level. Figure 4.6 shows the effect of grouping SMs on the output voltage of phase A, V_{AO1}. It can also be seen that grouping SMs reduces T_t with selecting sufficient T_d. T_t can be mathematically expressed as equation 4.2. Consequently, the fundamental voltage is increased, extra energy storage and higher current rating IGBT devices are not required, however $\frac{dv}{dt}$ stress has increased. Therefore, the selection of T_t and T_d is always a trade-off between energy storage requirements, operating frequency and $\frac{dv}{dt}$ stress. This is discussed further in the following sections. Moreover, the SM capacitor voltages in each group may face slight unbalance due to the gating delay. However, a capacitor voltage balancing method has been proposed by the Author to overcome this issue

and will be clarified in subsection 4.3 later in this chapter.

$$N_{st} = \frac{N_{SM}}{N_L} \tag{4.1}$$

$$T_t = (N_{st} - 1)T_d \tag{4.2}$$

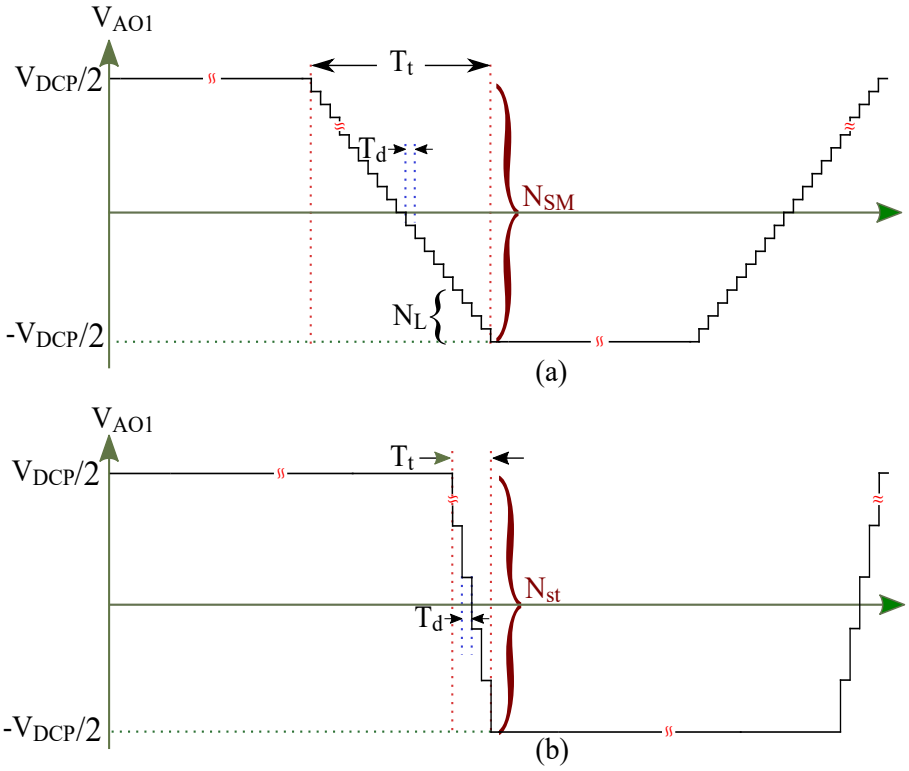


Figure 4.6: *The effect of grouping SMs on phase voltage with respect to DC link midpoint: (a) phase voltage without grouping SMs (b) phase voltage with grouping SMs*

4.2.1.2 Mathematical analysis of the trapezoidal phase voltage

The impacts of N_{st}, ω, T_t and T_d on the trapezoidal waveform, energy storage requirements and semiconductor *VA* requirement (semiconductor devices current rating) have been explained in the previous section. This section analyses the effect of N_{st}, ω, T_t and T_d on the fundamental and other harmonics of the trapezoidal waveform.

The harmonic contents of the trapezoidal ac voltage has been analysed using Fourier series expansion shown in equation 4.3. The following investigations are valid for any trapezoidal AC waveform. However, the trapezoidal ac voltage of phase A of the primary MMC has been chosen for the analysis. As shown previously in figure 4.6, the phase A trapezoidal ac voltage is half-wave symmetry $f(t) = -f(t+T/2)$. Consequently there is no dc component, $a_o = 0$, and sinusoidal components of odd harmonic orders are decomposed from the trapezoidal ac waveform.

$$
\begin{aligned}
&f(t) = a_o + \sum_{k=1}^{\infty} a_k cos(kt) + \sum_{k=1}^{\infty} b_k cos(kt) \\
&\text{where;} \\
&a_o = \frac{1}{2\pi}\int_0^{2\pi} f(t)dt \\
&a_k = \frac{1}{\pi}\int_0^{2\pi} f(t)cos(kt)dt \\
&b_k = \frac{1}{\pi}\int_0^{2\pi} f(t)sin(kt)dt
\end{aligned}
\tag{4.3}
$$

Therefore, considering the magnitude, $V_{DCP}/2$, of the phase A trapezoidal voltage and applying equation 4.3 the result shown in equation 4.4 is obtained where δ is the duty ratio (δ=0.5).

$$
v_{AO1}(t) = 2V_{DCP}\delta \sum_{k=1,3,5,\ldots}^{\infty} \frac{sin(k\pi\delta)}{k\pi\delta}\frac{sin(k\pi fT_t)}{k\pi fT_t} cos(k\omega t) \tag{4.4}
$$

The magnitude of any harmonic order, k^{th}, of the phase voltage, v_{AO1}, can be determined using equation 4.5 where $\alpha_p = \pi f T_t$.

$$
v_{AO1}(kf) = 2V_{DCP}\delta\frac{sin(k\pi\delta)}{k\pi\delta}\frac{sin(k\alpha_p)}{k\alpha_p} \tag{4.5}
$$

Then, by substituting $k = 1$ in equation 4.5 the fundamental value $v_{AO1}(f)$ is determined as equation 4.6 and the modulation index can be calculated as equation 4.7.

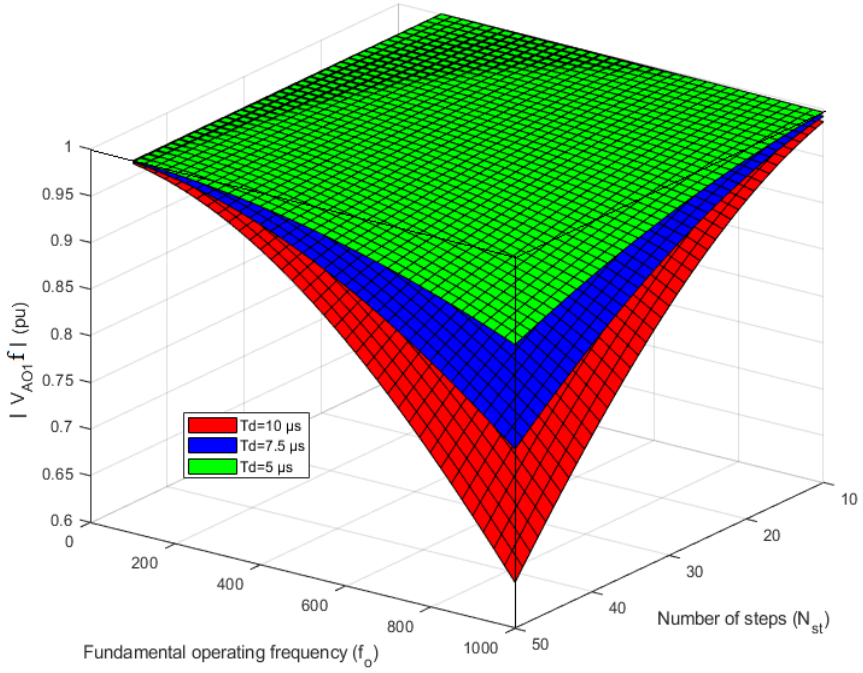
$$v_{AO1}(f) = \frac{2V_{DCP}}{\pi}\frac{sin(\alpha_p)}{\alpha_p} \tag{4.6}$$

$$m_p = \frac{2v_{AO1}(f)}{V_{DCP}} = \frac{4}{\pi}\frac{sin(\alpha_p)}{\alpha_p} \tag{4.7}$$

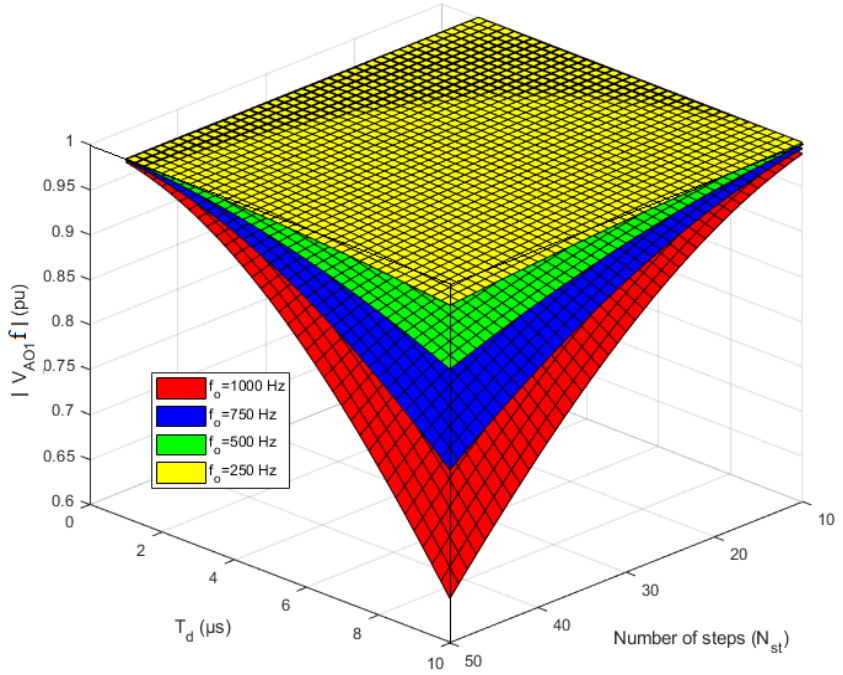
The maximum modulation index can be approximated to $\frac{4}{\pi}$ at small angle α_p which is obtained at small values of ω, N_{st} and T_d and accordingly the operation will be similar to square wave modulation. Increasing any parameter of ω, N_{st} and T_d leads to an increase in the angle α_p and consequently the fundamental modulation index will be reduced, $m_p < \frac{4}{\pi}$. Reduction in fundamental modulation index will be used to avoid unacceptable rise in current during transients and this is achieved by controlling over N_{st} and T_d which can be also used to control the energy in SM capacitors. More analysis and explanations about the control over N_{st} and T_d will be shown in the energy control section 4.4.2.

In order to graphically show the impact of ω, N_{st} and T_d on the fundamental output voltage, $v_{AO1}(f)$, a per unit representation has been used with $\frac{2V_{DCP}}{\pi}$ chosen as the base value. Equation 4.6 can be restated as equation 4.8. Figure 4.7 shows the value of $v^{pu}_{AO1}(f)$ for different values of f, N_{st} and T_d and as discussed previously increasing any of the parameters, f, N_{st} and T_d, will lead to a reduction in $v^{pu}_{AO1}(f)$. Reduction in $v^{pu}_{AO1}(f)$ will increase the load current for a particular power transfer value and consequently there will be penalties in semiconductor current rating, energy storage requirements due to higher SM capacitor values, and efficiency due to higher losses (semiconductor losses and copper losses).

$$v^{pu}_{AO1}(f) = \frac{sin(\alpha_p)}{\alpha_p} \tag{4.8}$$



(a) *discrete* T_d



(b) *discrete* ω

Figure 4.7: *Fundamental phase voltage with various* T_d, T_t *and* ω

The results also show that increasing any of the parameters within a certain range, $f \leq 250$, $N_{st} \leq 20$ and $T_d \leq 5\mu s$ will insignificantly affect the fundamental output voltage and this provides a margin for different design conditions for MVDC applications.

4.2.2 Selection of the converter components and semiconductor devices utilisation

This subsection will focus on the energy storage requirements, SM capacitor voltage balancing, semiconductor device rating and utilisation. Initially, the trapezoidal ac link voltage and current are analysed, these are important to determine the instantaneous power of each chain-link from which the peak to peak variation of the energy of the SMs can be calculated. Knowing the energy variation of the SMs and setting the converter to resonate at close to twice the fundamental operating frequency (between the equivalent effective capacitor and the inductor of each arm) will enable the required energy in the inductor arm to be determined. Additionally, the analysis shows the optimum operating point in terms of energy storage requirements and semiconductor device ratings, which depend on the voltage rating of the converter and the trapezoidal arm current waveform. Moreover, a new proposed SM capacitor voltage balancing method will be introduced which balances the SM capacitor voltages at fundamental frequency to reduce the switching losses. The new proposed method balances the SM capacitor voltage more effectively, particularly, during transients. A theoretical analysis of the charge distribution will be shown to support the effectiveness of the SM capacitors voltage balancing method.

4.2.2.1 Trapezoidal AC link voltage and current waveforms

Figure 4.8 depicts an ideal three phase MTrMMC-DC-DC converter where L_P represents the primary arm inductance, L_k represents the leakage inductance of the three phase transformer with respect to the primary side and L_S represents the secondary arm inductance. The per phase ac equivalent circuit of the MTrMMC-DC-DC can be derived as shown in figure 4.9 by taking KVL between O_1 and T_P for each phase of the primary side of the converter and similarly between O_2 and T_S for each phase of the secondary side of the converter where $L'_S = L_S/n^2$ represents the secondary arm inductance with respect to the primary side of the converter and L_{eq} (shown in equation 4.9) represents the effective inductance of the per phase equiv-

alent circuit. Additionally, the per phase primary ac voltage, $V_{PT_P}\text{-}\phi P(t)$, and the per phase secondary ac voltage, $V_{ST_S}\text{-}\phi S(t)$, can be derived as equation 4.10 and equation 4.11, respectively, where ϕP represents phases A, B, C of the primary side and ϕS represents phases U, V, W of the secondary side of the converter.

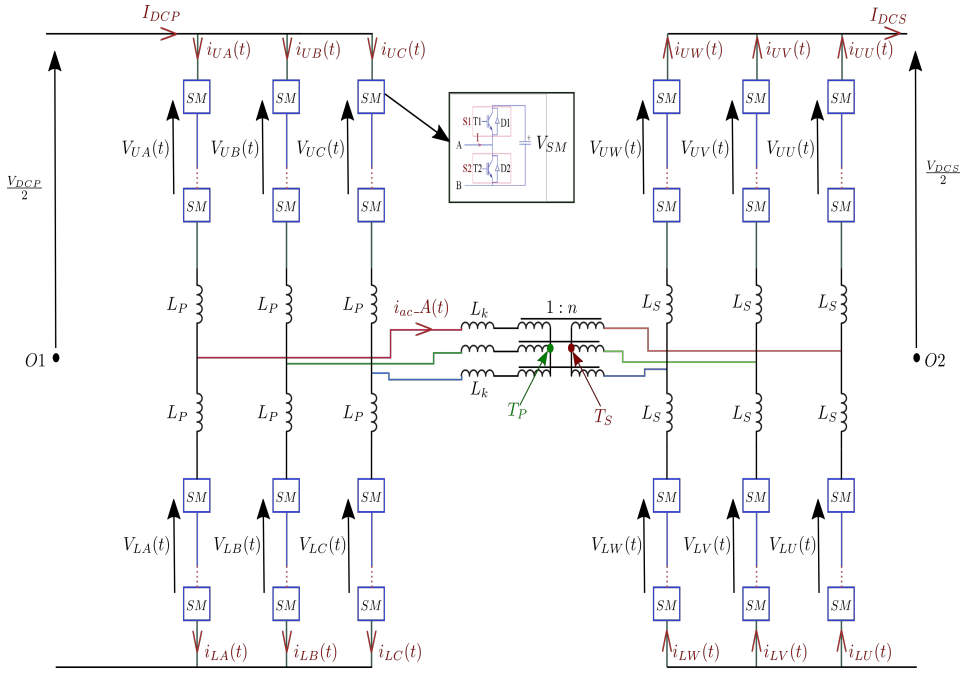


Figure 4.8: *MTrMMC-DC-DC*

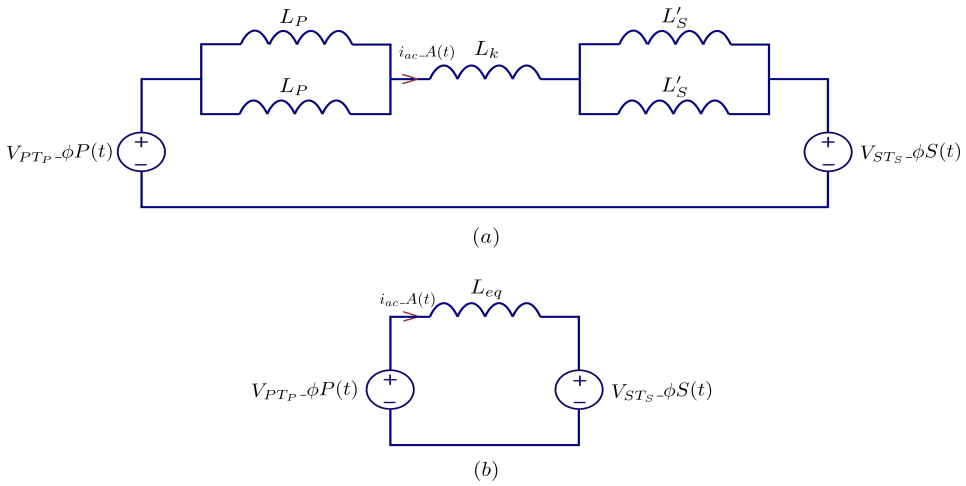


Figure 4.9: *Per phase equivalent circuit of MTrMMC-DC-DC*

$$L_{eq} = \frac{L_p}{2} + L_k + \frac{L'_S}{2}$$
$$L'_S = \frac{L_S}{n^2} \tag{4.9}$$

$$
\begin{aligned}
V_{PT_P}\_\phi P(t) &= \frac{V_{L\phi P}(t) - V_{U\phi P}(t)}{3} - V_{T_P} \\
V_{T_P} &= \frac{(V_{LA}(t) - V_{UA}(t)) + (V_{LB}(t) - V_{UB}(t)) + (V_{LC}(t) - V_{UC}(t))}{3}
\end{aligned}
\tag{4.10}
$$

$$
\begin{aligned}
V_{ST_S}\_\phi S(t) &= n * (\frac{V_{L\phi S}(t) - V_{U\phi S}(t)}{3} - V_{T_S}) \\
V_{T_S} &= \frac{(V_{LU}(t) - V_{UU}(t)) + (V_{LV}(t) - V_{UV}(t)) + (V_{LW}(t) - V_{UW}(t))}{3}
\end{aligned}
\tag{4.11}
$$

Figure 4.10 presents the primary phase A voltage, $V_{PT_P}\_A(t)$, the secondary phase U voltage , $V_{ST_S}\_U(t)$, and the primary ac current where similar transition period, $T_{tp} = T_{ts} = T_t$, is applied for both the primary and secondary. The phase shift, φ, between the primary and secondary phase voltages determines the voltage, $V_{L_{eq}}(t)$, across the equivalent effective inductance and hence the magnitude and the direction of the power can be controlled by controlling the voltage angle, φ. From the primary and secondary phase voltage waveforms, the current equations can be analytically derived for each portion of α from 0 to π using equation 4.12, considering the limitation of the voltage angle, φ, and for simplicity the stair case portion of the waveform is approximated to a line.

$$
i_{ac}\_A(\alpha) = i_{ac}\_A(0) + \frac{1}{\omega L_{eq}} \int_{\alpha_0}^{\alpha} (V_{PT_P}\_A(\alpha) - V_{ST_S}\_U(\alpha)) * d\alpha
\tag{4.12}
$$

Tables 4.2 and 4.3 show the current profiles for half of the fundamental cycle, 0 to π, when $\omega T_t \leq \varphi \leq \frac{\pi}{3} - \omega T_t$ and ρ_g (the DC voltage gain) is set to $\frac{nV_{DCS}}{V_{DCP}}$, which impacts the voltage across the leakage reactance of the transformer and hence the current profiles will be affected. The ac link current, $i_{ac}\_A(\alpha)$, is symmetric with zero dc value around x-axis hence the expression 4.37 can be used to calculate $i_{ac}\_A(0)$ as shown in equation 4.38. Then substituting $i_{ac}\_A(0)$ in tables 4.2 and 4.3 the expression for each portion of $i_{ac}\_A(\alpha)$ can be obtained. Similarly, all ac link currents of the other phases can be derived.

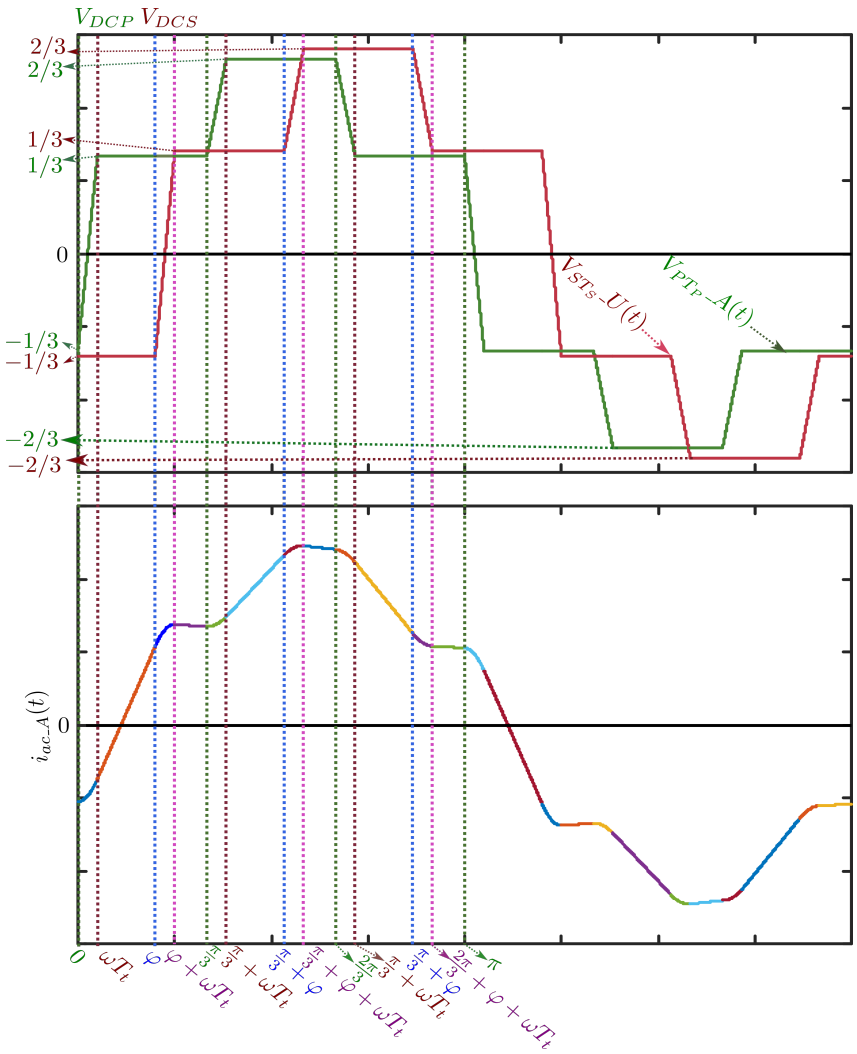


Figure 4.10: *MTrMMC-DC-DC AC link voltage and current waveforms*

The ac link current profiles in the intervals $\frac{\pi}{3}+\omega T_t \leq \alpha \leq \frac{\pi}{3}+\varphi+\omega T_t$ and $\frac{2\pi}{3} \leq \alpha \leq \frac{2\pi}{3}+\omega T_t$ are important for the semiconductor device current ratings when $\rho_g \geq 1$ and $\rho_g \leq 1$, respectively. Moreover, the ac link current profiles in the intervals $\varphi \leq \alpha \leq \varphi+\omega T_t$ and $\pi \leq \alpha \leq \varphi$ are important for calculating the size of the SM capacitors when $\rho_g \geq 1$ and $\rho_g \leq 1$, respectively. Further details about the sizing of SM capacitors will be shown in section 4.2.2.3, later in this chapter.

$$i_{ac\_A}(0) = -i_{ac\_A}(\pi) \tag{4.37}$$

$$i_{ac\_A}(0) = \frac{V_{DCP}}{3\omega L_{eq}}((\rho_g-1)\frac{2\pi}{3}+(1-\rho_g)\frac{\omega T_t}{2}-\rho_g\varphi)... \quad \text{when } \omega T_t < \varphi < \frac{\pi}{3}-\omega T_t \tag{4.38}$$

Table 4.2: $i_{ac}\_A(\alpha)$ profile for half fundamental cycle when $\omega T_t < \varphi < \frac{\pi}{3} - \omega T_t$

α	$i_{ac}\_A(\alpha)$	
$0 \leq \alpha \leq \omega T_t$	$i_{ac}\_A(0) + \frac{V_{DCP}}{3\omega L_{eq}}(\frac{\alpha^2}{\omega T_t} + (\rho_g - 1)\alpha)$	(4.13)
$\omega T_t \leq \alpha \leq \varphi$	$i_{ac}\_A(\omega T_t) + \frac{V_{DCP}}{3\omega L_{eq}}((\rho_g + 1)(\alpha - \omega T_t))$	(4.14)
$\varphi \leq \alpha \leq \varphi + \omega T_t$	$i_{ac}\_A(\varphi) + \frac{V_{DCP}}{3\omega L_{eq}}((\rho_g + 1)(\alpha - \varphi) - \frac{\rho_g}{\omega T_t}(\alpha - \varphi)^2)$	(4.15)
$\varphi + \omega T_t \leq \alpha \leq \frac{\pi}{3}$	$i_{ac}\_A(\varphi + \omega T_t) + \frac{V_{DCP}}{3\omega L_{eq}}((1 - \rho_g)(\alpha - \varphi - \omega T_t))$	(4.16)
$\frac{\pi}{3} \leq \alpha \leq \frac{\pi}{3} + \omega T_t$	$i_{ac}\_A(\frac{\pi}{3}) + \frac{V_{DCP}}{3\omega L_{eq}}((1 - \rho_g)(\alpha - \frac{\pi}{3}) + \frac{1}{2\omega T_t}(\alpha - \frac{\pi}{3})^2)$	(4.17)
$\frac{\pi}{3} + \omega T_t \leq \alpha \leq \frac{\pi}{3} + \varphi$	$i_{ac}\_A(\frac{\pi}{3} + \omega T_t) + \frac{V_{DCP}}{3\omega L_{eq}}((2 - \rho_g)(\alpha - \frac{\pi}{3} - \omega T_t))$	(4.18)
$\frac{\pi}{3} + \varphi \leq \alpha \leq \frac{\pi}{3} + \varphi + \omega T_t$	$i_{ac}\_A(\frac{\pi}{3} + \varphi) + \frac{V_{DCP}}{3\omega L_{eq}}((2 - \rho_g)(\alpha - \frac{\pi}{3} - \varphi) - \frac{\rho_g}{2\omega T_t}(\alpha - \frac{\pi}{3} - \varphi)^2)$	(4.19)
$\frac{\pi}{3} + \varphi + \omega T_t \leq \alpha \leq \frac{2\pi}{3}$	$i_{ac}\_A(\frac{\pi}{3} + \varphi + \omega T_t) + \frac{V_{DCP}}{3\omega L_{eq}}((2 - 2\rho_g)(\alpha - \frac{\pi}{3} - \varphi - \omega T_t))$	(4.20)
$\frac{2\pi}{3} \leq \alpha \leq \frac{2\pi}{3} + \omega T_t$	$i_{ac}\_A(\frac{2\pi}{3}) + \frac{V_{DCP}}{3\omega L_{eq}}((2 - 2\rho_g)(\alpha - \frac{2\pi}{3}) - \frac{1}{2\omega T_t}(\alpha - \frac{2\pi}{3})^2)$	(4.21)
$\frac{2\pi}{3} + \omega T_t \leq \alpha \leq \frac{2\pi}{3} + \varphi$	$i_{ac}\_A(\frac{2\pi}{3} + \omega T_t) + \frac{V_{DCP}}{3\omega L_{eq}}((1 - 2\rho_g)(\alpha - \frac{2\pi}{3} - \omega T_t))$	(4.22)
$\frac{2\pi}{3} + \varphi \leq \alpha \leq \frac{2\pi}{3} + \varphi + \omega T_t$	$i_{ac}\_A(\frac{2\pi}{3} + \varphi) + \frac{V_{DCP}}{3\omega L_{eq}}((1 - 2\rho_g)(\alpha - \frac{2\pi}{3} - \varphi) - \frac{\rho_g}{2\omega T_t}(\alpha - \frac{2\pi}{3} - \varphi)^2)$	(4.23)
$\frac{2\pi}{3} + \varphi + \omega T_t \leq \alpha \leq \pi$	$i_{ac}\_A(\frac{2\pi}{3} + \varphi + \omega T_t) + \frac{V_{DCP}}{3\omega L_{eq}}((1 - \rho_g)(\alpha - \frac{2\pi}{3} - \varphi - \omega T_t))$	(4.24)

Similarly, an analysis for the ac link current of phase A has been performed when $\varphi < \omega T_t$ as shown in tables 4.4 and 4.5 where $i_{ac}\_A(0)$ shown in equation 4.63 was found based on equation 4.37 due to the symmetry of $i_{ac}\_A(\alpha)$ with zero mean value. In addition, an analysis can be done when $\varphi > \frac{\pi}{3} - \omega T_t$ however a high voltage angle, $\varphi > \frac{\pi}{3} - \omega T_t$, is not common in HVDC applications. Therefore, a voltage angle in the range $\varphi \leq \frac{\pi}{3} - \omega T_t$ will be considered for the energy storage requirements and device rating calculation in the rest of this section.

$$i_{ac}\_A(0) = \frac{V_{DCP}}{3\omega L_{eq}}((2\rho_g - 2)\frac{\pi}{3} + (1 - \rho_g)\frac{\omega T_t}{2} - \rho_g\varphi)... \quad \text{when } 0 < \varphi < \omega T_t \tag{4.63}$$

Table 4.3: $i_{ac}\_A(\alpha)$ profile at the end of each segment when $\omega T_t < \varphi < \frac{\pi}{3} - \omega T_t$

α	$i_{ac}\_A(\alpha)$	
ωT_t	$i_{ac}\_A(\omega T_t) = i_{ac}\_A(0) + \frac{V_{DCP}}{3\omega L_{eq}}(\rho_g \omega T_t)$	(4.25)
φ	$i_{ac}\_A(0) + \frac{V_{DCP}}{3\omega L_{eq}}((\rho_g + 1)\varphi - \omega T_t)$	(4.26)
$\varphi + \omega T_t$	$i_{ac}\_A(0) + \frac{V_{DCP}}{3\omega L_{eq}}((\rho_g + 1)\varphi)$	(4.27)
$\frac{\pi}{3}$	$i_{ac}\_A(0) + \frac{V_{DCP}}{3\omega L_{eq}}((1-\rho_g)(\frac{\pi}{3} - \omega T_t) + 2\rho_g \varphi)$	(4.28)
$\frac{\pi}{3} + \omega T_t$	$i_{ac}\_A(0) + \frac{V_{DCP}}{3\omega L_{eq}}((1-\rho_g)(\frac{\pi}{3}) + \frac{1}{2\omega T_t} + 2\rho_g)$	(4.29)
$\frac{\pi}{3} + \varphi$	$i_{ac}\_A(0) + \frac{V_{DCP}}{3\omega L_{eq}}((\rho_g + 1)\varphi + (1-\rho_g)(\frac{\pi}{3} - \omega T_t) + \varphi - \frac{1}{2\omega T_t})$	(4.30)
$\frac{\pi}{3} + \varphi + \omega T_t$	$i_{ac}\_A(0) + \frac{V_{DCP}}{3\omega L_{eq}}((1+\rho_g)\varphi + \varphi + (1-\rho_g)(\frac{\pi}{3} + \frac{\omega T_t}{2}))$	(4.31)
$\frac{2\pi}{3}$	$i_{ac}\_A(0) + \frac{V_{DCP}}{3\omega L_{eq}}((3-3\rho_g)\frac{\pi}{3} + 3\rho_g \varphi + (2+2\rho_g)\omega T_t + (1-\rho_g)\frac{\omega T_t}{2})$	(4.32)
$\frac{2\pi}{3} + \omega T_t$	$i_{ac}\_A(0) + \frac{V_{DCP}}{3\omega L_{eq}}((3-3\rho_g)\frac{\pi}{3} + 3\rho_g \varphi - \frac{\rho_g \omega T_t}{2})$	(4.33)
$\frac{2\pi}{3} + \varphi$	$i_{ac}\_A(0) + \frac{V_{DCP}}{3\omega L_{eq}}((1+\rho_g)\varphi + (\rho_g - 1)\omega T_t + (3-3\rho_g)\frac{\pi}{3} + \frac{\rho_g \omega T_t}{2})$	(4.34)
$\frac{2\pi}{3} + \varphi + \omega T_t$	$i_{ac}\_A(0) + \frac{V_{DCP}}{3\omega L_{eq}}((1+\rho_g)\varphi + (3-3\rho_g)\frac{\pi}{3})$	(4.35)
π	$i_{ac}\_A(\pi) = i_{ac}\_A(0) + \frac{V_{DCP}}{3\omega L_{eq}}((4-4\rho_g)\frac{\pi}{3} + (\rho_g - 1)\omega T_t + 2\rho_g \varphi)$	(4.36)

4.2.2.2 Semiconductor devices rating and utilisation

The maximum arm current determines the rating of the devices and it comprises part of the dc current and half of the ac link current as shown in equation 4.64 for the upper arm of phase A. Considering a lossless converter, the DC current can be calculated as shown in equation 4.65 where P_{av} is the average power which is calculated from the product of the primary phase voltage, $V_{PT_P}\_A(t)$, and ac link current profiles, $i_{ac}\_A(t)$, during each segment over the half of the fundamental cycle, 0 to π, as shown in equation 4.66.

$$i_{UA}(t) = \frac{I_{DCP}}{3} + \frac{i_{ac}\_A(t)}{2} \tag{4.64}$$

Table 4.4: $i_{ac}\_A(\alpha)$ profile for half fundamental cycle when $\varphi < \omega T_t$

α	$i_{ac}\_A(\alpha)$	
$0 \leq \alpha \leq \varphi$	$i_{ac}\_A(0) + \frac{V_{DCP}}{3\omega L_{eq}}(\frac{\alpha^2}{\omega T_t} + (\rho_g - 1)\alpha)$	(4.39)
$\varphi \leq \alpha \leq \omega T_t$	$i_{ac}\_A(\varphi) + \frac{V_{DCP}}{3\omega L_{eq}}((\frac{(\alpha-\varphi)^2}{\omega Tt} - (\alpha-\varphi))(1-\rho_g) + \frac{2\varphi}{\omega T_t}(\alpha-\varphi))$	(4.40)
$\omega Tt \leq \alpha \leq \varphi + \omega T_t$	$i_{ac}\_A(\omega Tt) + \frac{V_{DCP}}{3\omega L_{eq}}((1+\rho_g)(\alpha-\omega T_t) - \frac{\rho_g(\alpha-\omega T_t)^2}{\omega T_t} - \frac{2\rho_g(\alpha-\omega T_t)(\omega T_t-\varphi)}{\omega T_t})$	(4.41)
$\varphi + \omega T_t \leq \alpha \leq \frac{\pi}{3}$	$i_{ac}\_A(\varphi + \omega T_t) + \frac{V_{DCP}}{3\omega L_{eq}}((1-\rho_g)(\alpha-\varphi-\omega T_t))$	(4.42)
$\frac{\pi}{3} \leq \alpha \leq \frac{\pi}{3} + \varphi$	$i_{ac}\_A(\frac{\pi}{3}) + \frac{V_{DCP}}{3\omega L_{eq}}((1-\rho_g)(\alpha-\frac{\pi}{3}) + \frac{1}{2\omega T_t}(\alpha-\frac{\pi}{3})^2)$	(4.43)
$\frac{\pi}{3} + \varphi \leq \alpha \leq \frac{\pi}{3} + \omega T_t$	$i_{ac}\_A(\frac{\pi}{3}+\varphi) + \frac{V_{DCP}}{3\omega L_{eq}}((1-\rho_g)((\alpha-\frac{\pi}{3}-\varphi) + (\frac{(\alpha-\frac{\pi}{3}-\varphi)^2}{2\omega T_t})) + \frac{\varphi(\alpha-\frac{\pi}{3}-\varphi)}{\omega T_t})$	(4.44)
$\frac{\pi}{3} + \omega T_t \leq \alpha \leq \frac{\pi}{3} + \varphi + \omega T_t$	$i_{ac}\_A(\frac{\pi}{3}+\omega T_t) + \frac{V_{DCP}}{3\omega L_{eq}}((2-\rho_g)(\alpha-\frac{\pi}{3}-\omega T_t) - \frac{\rho_g}{2\omega T_t}(\alpha-\frac{\pi}{3}-\omega T_t)^2 - \frac{(\alpha-\frac{\pi}{3}-\omega T_t)(\omega T_t-\varphi)}{\omega T_t})$	(4.45)
$\frac{\pi}{3} + \varphi + \omega T_t \leq \alpha \leq \frac{2\pi}{3}$	$i_{ac}\_A(\frac{\pi}{3}+\varphi+\omega T_t) + \frac{V_{DCP}}{3\omega L_{eq}}((2-2\rho_g)(\alpha-\frac{\pi}{3}-\varphi-\omega T_t))$	(4.46)
$\frac{2\pi}{3} \leq \alpha \leq \frac{2\pi}{3} + \varphi$	$i_{ac}\_A(\frac{2\pi}{3}) + \frac{V_{DCP}}{3\omega L_{eq}}((2-2\rho_g)(\alpha-\frac{2\pi}{3}) - \frac{1}{2\omega T_t}(\alpha-\frac{2\pi}{3})^2)$	(4.47)
$\frac{2\pi}{3} + \varphi \leq \alpha \leq \frac{2\pi}{3} + \omega T_t$	$i_{ac}\_A(\frac{2\pi}{3}+\varphi) + \frac{V_{DCP}}{3\omega L_{eq}}((2-2\rho_g)(\alpha-\frac{2\pi}{3}-\varphi) - (1-\rho_g)(\frac{(\alpha-\frac{2\pi}{3}-\varphi)^2}{2\omega T_t}) - \frac{\varphi(\alpha-\frac{2\pi}{3}-\varphi)}{\omega T_t})$	(4.48)
$\frac{2\pi}{3} + \omega T_t \leq \alpha \leq \frac{2\pi}{3} + \varphi + \omega T_t$	$i_{ac}\_A(\frac{2\pi}{3}+\omega T_t) + \frac{V_{DCP}}{3\omega L_{eq}}((1-2\rho_g)(\alpha-\frac{2\pi}{3}-\omega Tt) - \frac{\rho_g}{2\omega T_t}(\alpha-\frac{2\pi}{3}-\omega T_t)^2 + \frac{\rho_g(\omega T_t-\varphi)(\alpha-\frac{2\pi}{3}-\omega Tt)}{\omega T_t})$	(4.49)
$\frac{2\pi}{3} + \varphi + \omega T_t \leq \alpha \leq \pi$	$i_{ac}\_A(\frac{2\pi}{3}+\varphi+\omega T_t) + \frac{V_{DCP}}{3\omega L_{eq}}((1-\rho_g)(\alpha-\frac{2\pi}{3}-\varphi-\omega T_t))$	(4.50)

$$I_{DCP} = \frac{P_{av}}{V_{DCP}} \tag{4.65}$$

Table 4.5: $i_{ac}\_A(\alpha)$ profile at the end of each segment when $\varphi < \omega T_t$

α	$i_{ac}\_A(\alpha)$	
φ	$i_{ac}\_A(\varphi) = i_{ac}\_A(0) + \frac{V_{DCP}}{3\omega L_{eq}}((\rho_g - 1)\varphi + \frac{\varphi^2}{\omega T_t})$	(4.51)
ωT_t	$i_{ac}\_A(0) + \frac{V_{DCP}}{3\omega L_{eq}}(\rho_g(2\varphi - \frac{\varphi^2}{\omega T_t})$	(4.52)
$\varphi + \omega T_t$	$i_{ac}\_A(0) + \frac{V_{DCP}}{3\omega L_{eq}}((\rho_g + 1)\varphi)$	(4.53)
$\frac{\pi}{3}$	$i_{ac}\_A(0) + \frac{V_{DCP}}{3\omega L_{eq}}((1 - \rho_g)(\frac{\pi}{3} - \omega T_t) + 2\rho_g\varphi)$	(4.54)
$\frac{\pi}{3} + \varphi$	$i_{ac}\_A(0) + \frac{V_{DCP}}{3\omega L_{eq}}((1 - \rho_g)(\frac{\pi}{3} - \omega T_t) + \frac{\varphi^2}{2\omega T_t} + (\rho_g + 1)\varphi)$	(4.55)
$\frac{\pi}{3} + \omega T_t$	$i_{ac}\_A(0) + \frac{V_{DCP}}{3\omega L_{eq}}((1 - \rho_g)(\frac{\pi}{3} + \frac{1}{2\omega T_t}) + 3\rho_g\varphi - \frac{\rho_g\varphi^2}{2\omega T_t})$	(4.56)
$\frac{\pi}{3} + \varphi + \omega T_t$	$i_{ac}\_A(0) + \frac{V_{DCP}}{3\omega L_{eq}}((1 - \rho_g)(\frac{\pi}{3} + \frac{1}{2\omega T_t}) + (2 + \rho_g)\varphi)$	(4.57)
$\frac{2\pi}{3}$	$i_{ac}\_A(0) + \frac{V_{DCP}}{3\omega L_{eq}}((3 - 3\rho_g)\frac{\pi}{3} + 3\rho_g\varphi + (\rho_g - 1)(\frac{\omega T_t}{2} + \omega T_t))$	(4.58)
$\frac{2\pi}{3} + \varphi$	$i_{ac}\_A(0) + \frac{V_{DCP}}{3\omega L_{eq}}((3 - 3\rho_g)\frac{\pi}{3} + (\rho_g - 1)(\frac{\omega T_t}{2} + \omega T_t) + (2 + \rho_g)\varphi - \frac{\varphi^2}{2\omega T_t})$	(4.59)
$\frac{2\pi}{3} + \omega T_t$	$i_{ac}\_A(0) + \frac{V_{DCP}}{3\omega L_{eq}}((3 - 3\rho_g)\frac{\pi}{3} + 2\rho_g\varphi + \frac{\rho_g\varphi^2}{2\omega T_t})$	(4.60)
$\frac{2\pi}{3} + \varphi + \omega T_t$	$i_{ac}\_A(0) + \frac{V_{DCP}}{3\omega L_{eq}}((1 + \rho_g)\varphi + (3 - 3\rho_g)\frac{\pi}{3})$	(4.61)
π	$i_{ac}\_A(\pi) = i_{ac}\_A(0) + \frac{V_{DCP}}{3\omega L_{eq}}((4 - 4\rho_g)\frac{\pi}{3} + (\rho_g - 1)\omega T_t + 2\rho_g\varphi)$	(4.62)

$$
\begin{aligned}
P_{av} &= \frac{3}{\pi}\int_0^{\pi} V_{PT_P}\_A(\alpha) * i_{ac}\_A(\alpha) * d\alpha \\
P_{av} &= \frac{-(\rho_g V_{DCP}^2(\omega^2 T_t^2 + 6\varphi^2 - 8\pi\varphi))}{12\omega L_{eq}\pi} \text{ when } \omega T_t < \varphi < \frac{\pi}{3} - \omega T_t \\
P_{av} &= \frac{-(\varphi\rho_g V_{DCP}^2(4\omega T_t + \frac{4\varphi^2}{\omega T_t} - \frac{\varphi^3}{\omega^2 T_t^2} - 8\pi))}{12\omega L_{eq}\pi} \text{ when } 0 < \varphi < \omega T_t
\end{aligned}
\tag{4.66}
$$

The nominal current rating of the semiconductor devices which is the peak value of the arm current can be calculated based on the equation 4.64, ρ_g and φ. Table 4.6 shows the segment where the arm current reaches a maximum for different operating conditions.

Table 4.6: Peak of the arm current

φ	ρ_g	α	$i_{UA}\_A(\alpha)$	
$\omega T_t \leq \varphi \leq \frac{\pi}{3} - \omega T_t$	$\rho_g \geq 1$	$\frac{\pi}{3} + \varphi \leq \alpha \leq \frac{\pi}{3} + \omega T_t + \varphi$	$i_{UA}\_A(\alpha) = \frac{\text{Equ.4.65}}{3} + \frac{\text{Equ.4.19}}{2}$	(4.67)
$\omega T_t \leq \varphi \leq \frac{\pi}{3} - \omega T_t$	$\rho_g < 1$	$\frac{2\pi}{3} \leq \alpha \leq \frac{2\pi}{3} + \omega T_t$	$i_{UA}\_A(\alpha) = \frac{\text{Equ.4.65}}{3} + \frac{\text{Equ.4.21}}{2}$	(4.68)
$0 < \varphi \leq \omega T_t$	$\rho_g \geq 1$	$\frac{\pi}{3} + \omega T_t \leq \alpha \leq \frac{\pi}{3} + \omega T_t + \varphi$	$i_{UA}\_A(\alpha) = \frac{\text{Equ.4.65}}{3} + \frac{\text{Equ.4.45}}{2}$	(4.69)
$0 < \varphi \leq \omega T_t$	$\rho_g < 1$	$\frac{2\pi}{3} \leq \alpha \leq \frac{\pi}{3} + \varphi$	$i_{UA}\_A(\alpha) = \frac{\text{Equ.4.65}}{3} + \frac{\text{Equ.4.47}}{2}$	(4.70)

Figure 4.11-a shows the ideal current and voltage waveform of the upper arm of phase A with IGBT utilisation when power is transferred from the primary DC link to the secondary DC link (positive power flow). Considering the half bridge SM which was previously shown in figure 4.3 and when all SMs are bypassed during the majority of half of the cycle (ωT_t to π) transistor, T2, is conducting. During transition period, T_t, transistor, T2, is conducting when SMs are bypassed and diode, D1, is conducting when SMs are inserted. In the half of the period where the SMs are all inserted, device D1 is ON when the arm current is positive and transistor T1 is ON when the arm current is negative. With this operation both switches, S1 and S2, are conducting continuously and D2 is not used in S2. However, if the power is transferred from the secondary DC link to the primary DC link (negative power flow), the transistor T2 will not be used and the diode D2 will be conducting instead as can be observed in figure 4.11-b. Therefore in unidirectional power flow, D2 in the primary SMs and T2 in the secondary SMs can be removed and this will reduce the semiconductor requirement. Moreover, transistor, T1, is soft switching at zero current (observe fig. 4.11-a) and this is an additional advantage of this proposed trapezoidal operation in terms of switching loss considerations.

4.2.2.3 Selection of the converter components

As previously discussed, in trapezoidal operation apart from T_t, all SMs are inserted for half of the period, $1/2f_o$, and bypassed for the other half period in each arm. When the SMs are inserted the arm of the MTrMMC-DC-DC can be represented as an LC resonant arm as shown in figure 4.12 where C_{eqP} is the primary arm

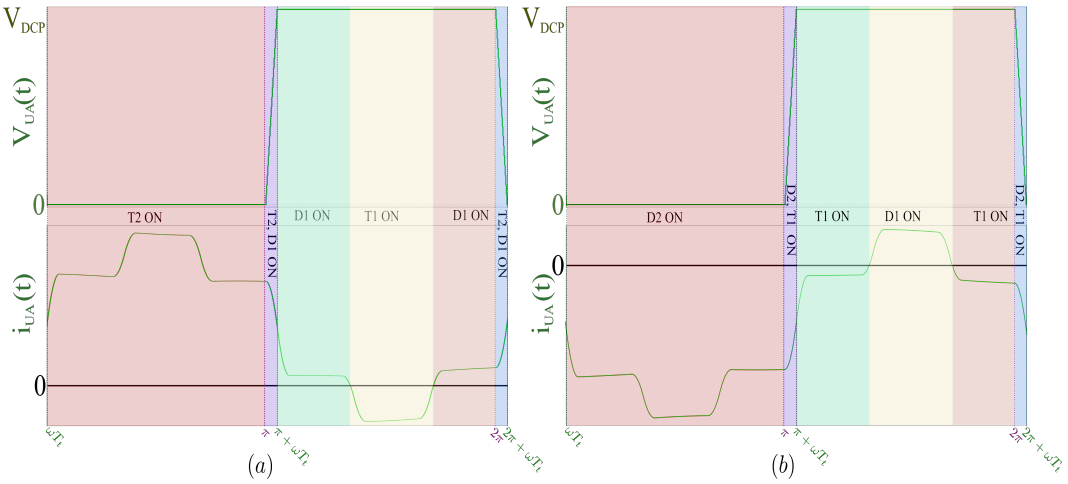


Figure 4.11: *Arm voltage and current waveforms: (a) positive power flow (b) negative power flow*

equivalent SM capacitance. When the SMs are bypassed the arm can be represented as an inductive arm where L_P represents the primary arm inductance. Continuous conduction of the arm current is achieved by keeping the resonant frequency, f_r, between C_{eqP} and L_P below twice the output frequency with a margin for safety ($fr \leq \frac{2f_o}{1.5}$), where the resonant frequency, f_r, of series LC circuit is shown in equation 4.71.

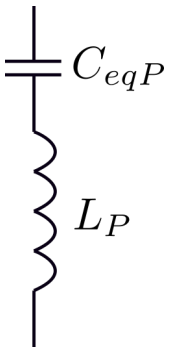


Figure 4.12: *Primary equivalent arm circuit when all SMs are inserted*

$$f_r = \frac{1}{2\pi\sqrt{L_P C_{eqP}}} \tag{4.71}$$

In subsection 4.2.2.1, it was explained that considering $\omega T_t \leq \varphi \leq \frac{\pi}{3} - \omega T_t$ (figure 4.10) the ac link current profiles in intervals $\varphi \leq \alpha \leq \varphi + \omega T_t$ and $\pi \leq \alpha \leq \pi + \omega T_t$

are important for calculating the size of SM capacitors when $\rho_g \geq 1$ and $\rho_g \leq 1$, respectively. Similarly, taking the voltage angle, $0 < \varphi \leq \omega T_t$ into consideration, the AC link profiles in segments $\omega T_t \leq \alpha \leq \varphi + \omega T_t$ and $\pi + \varphi \leq \alpha \leq \pi + \omega T_t$ are important for calculating the size of SM capacitors when $\rho_g \geq 1$ and $\rho_g \leq 1$, respectively. Table 5.4 shows the size of the primary equivalent arm SM capacitance, C_{eqP}, at different operating conditions where $\gamma \geq 1$ is the correction factor to take the effect of device series resistance and common mode current into account and δ_{pp} is the per unit peak to peak SM capacitor voltage ripple. Considering unity ρ_g, the expressions 4.76 and 4.77 show the size of the equivalent arm SM capacitance, C_{eqP}, at voltage angle $0 < \varphi \leq \omega T_t$ and $\omega T_t \leq \alpha \leq \varphi + \omega T_t$, respectively. The primary equivalent capacitance per group, C_{gP}, and the secondary equivalent capacitance per group, C_{gS}, can be found as presented in equation 4.78 and equation 4.79, respectively. The expressions 4.80 and 4.81 show the primary SM capacitance and secondary SM capacitance, respectively.

Table 4.7: Primary equivalent arm SM capacitance

φ	ρ_g	α	C_{eqP}	
$\omega T_t \leq \varphi \leq \frac{\pi}{3} - \omega T_t$	$\rho_g \geq 1$	$\varphi \leq \alpha \leq \omega T_t + \varphi$	$C_{eqP} = \frac{\gamma}{\omega * V_{DCP} * \delta_{pp}} \int_{\alpha=\varphi}^{\alpha=(\omega T_t+\varphi)} (\frac{\text{Equ.4.65}}{3} + \frac{\text{Equ.4.15}}{2}) d\alpha$	(4.72)
$\omega T_t \leq \varphi \leq \frac{\pi}{3} - \omega T_t$	$\rho_g < 1$	$\pi \leq \alpha \leq \pi + \omega T_t$	$C_{eqP} = \frac{\gamma}{\omega * V_{DCP} * \delta_{pp}} \int_{\alpha=\pi}^{\alpha=(\pi+\omega T_t)} (\frac{\text{Equ.4.65}}{3} - \frac{\text{Equ.4.13}}{2}) d\alpha$	(4.73)
$0 < \varphi \leq \omega T_t$	$\rho_g \geq 1$	$\omega T_t \leq \alpha \leq \omega T_t + \varphi$	$C_{eqP} = \frac{\gamma}{\omega * V_{DCP} * \delta_{pp}} \int_{\alpha=\omega T_t}^{\alpha=(\omega T_t+\varphi)} (\frac{\text{Equ.4.65}}{3} + \frac{\text{Equ.4.41}}{2}) d\alpha$	(4.74)
$0 < \varphi \leq \omega T_t$	$\rho_g < 1$	$\pi + \varphi \leq \alpha \leq \pi + \omega T_t$	$C_{eqP} = \frac{\gamma}{\omega * V_{DCP} * \delta_{pp}} \int_{\alpha=\pi+\varphi}^{\alpha=(\pi+\omega T_t)} (\frac{\text{Equ.4.65}}{3} - \frac{\text{Equ.4.40}}{2}) d\alpha$	(4.75)

$$C_{eqP} = \frac{\gamma \varphi^2 (\frac{\varphi^3}{\omega T_t} - 4\varphi^2 - 4\omega^2 T_t^2 + 14\pi\omega T_t - 2\pi\varphi)}{36 L_{eq} \delta_{pp} \pi \omega^3 T_t} \tag{4.76}$$

$$C_{eqP} = \frac{\gamma T_t (14\pi\varphi - 2\pi\omega T_t - \omega^2 T_t^2 - 6\varphi^2)}{36 L_{eq} \delta_{pp} \omega \pi} \tag{4.77}$$

$$C_{gP} = N_{st} C_{eqP} \tag{4.78}$$

$$C_{gS} = \rho_g^2 n^2 C_{gP} \tag{4.79}$$

$$C_{SMP} = N_{LP} C_{gP} \tag{4.80}$$

$$C_{SMS} = N_{LS} C_{gS} \tag{4.81}$$

The minimum energy storage for the chain-link can be described by equation 4.82 assuming perfect energy sharing among the SMs in the corresponding chain-link. Equation 4.83 shows the energy of the arm inductor where $\hat{I_{UA}}$ is the peak of the upper arm primary phase A current which was calculated in table 4.6 considering different operating conditions. The energy constant required, H_c, can be then described as in equation 4.84.

$$E_{ch} = \frac{1}{2} C_{SM} N_{SM} V_{SM}^2 [J] \tag{4.82}$$

$$E_{LP} = \frac{1}{2} L_P (\hat{I_{UA}})^2 [J] \tag{4.83}$$

$$H_c = \frac{6(E_{chP} + E_{chS}) + 6(E_{LP} + E_{LS})}{P_{av}} [s] \tag{4.84}$$

Considering unity $\rho_g = 1$, $n = 1$ and from equation 4.9, expression 4.85 is achieved. Using per unit average transferred power, $P_{av}(p.u)$, L_{eq} can be found at different voltage angle, φ from equation 4.66. Assuming leakage inductance of transformer 10% and from equations 4.85, 4.76, 4.77, 4.71 and 4.84, L_P, C_{eqP}, f_r and $H_c(p.u)$ can be found, respectively. Figures 4.13-a and 4.13-b show $H_c(p.u)$ and f_r/f_o at different T_t and different φ, respectively. As previously stated at the beginning of this section, in order to keep the arm currents conducting continuously $\frac{f_r}{f_o} \leq (\frac{2}{1.5} = 1.334)$ therefore φ has been changed until $\frac{f_r}{f_o} \leq 1.334$. It can be demonstrated that the phase shift $\frac{\varphi}{\pi} = 0.2148$ at $T_t = 0.1\pi$ and $\frac{\varphi}{\pi} = 0.1612$ at $T_t = 0.15\pi$ shown in figure 4.13-b are the operating points where the minimum energy required to maintain continuous conduction and keep the SM capacitor voltage ripple within the desired range which is evaluated as shown in figure 4.13-a. Figure 4.13-c shows the required L_{eq} with respect to the assumed leakage inductance of the transformer, L_k.

$$L_P = L_S = L_{eq} - L_k \tag{4.85}$$

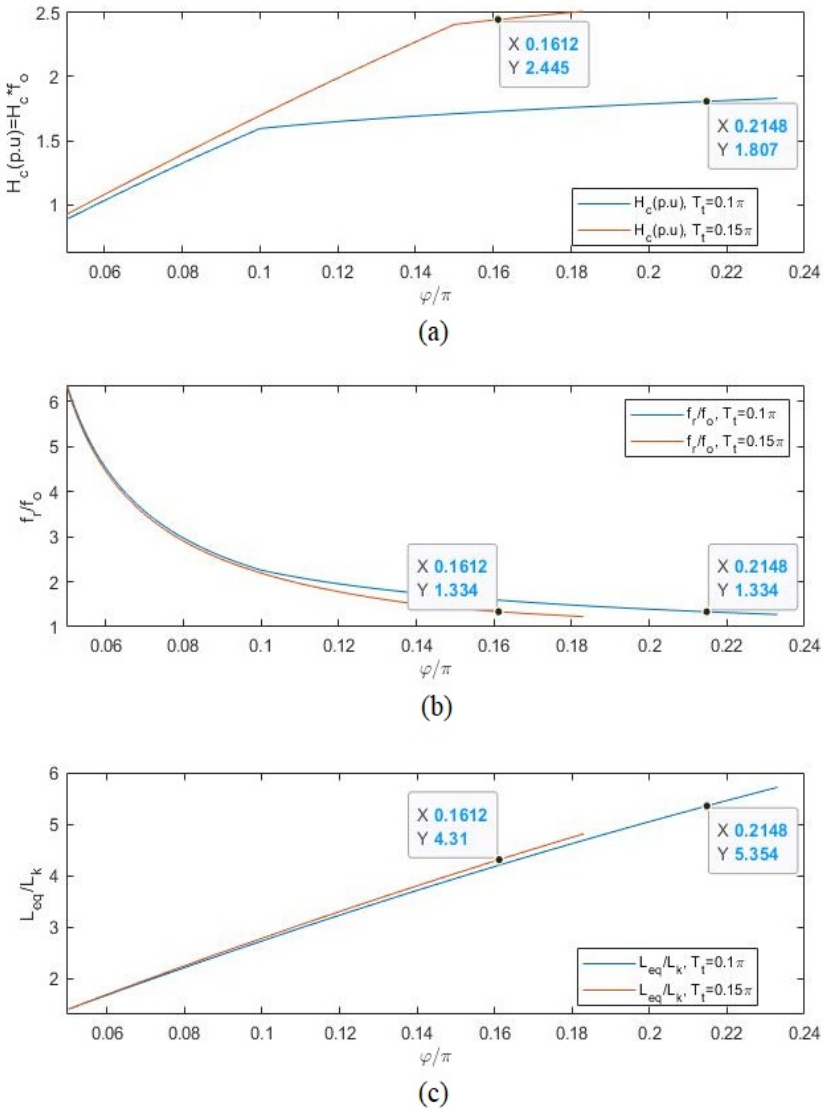


Figure 4.13: *(a) Energy storage requirement (b) Resonant frequency (C)* L_{eq}

4.3 Submodule capacitor voltage balancing

In trapezoidal wave-shaping, all the SMs are inserted for most of the half cycle and bypassed for the other half, making the balancing process of SM capacitor more challenging. The Author has proposed a new capacitor voltage balancing method by controlling the equivalent duty cycle of each SM. This control is made by the exploitation of the ramps in the trapezoidal voltage waveforms, which allows an unequal power flow to be imposed in the different SMs. The individual duty-cycles are assigned according to the voltage sorting order, where the duty cycle which causes highest net charge is assigned to the SMs where the capacitors have lowest voltage. As a result, balancing is achieved more effectively particularly during

transients in comparison to the fixed 50% duty cycle method which was introduced previously in figure 4.5-a. This section provides a theoretical analysis of the charge distribution among the SMs to support the effectiveness of the proposed balancing method and to compare it with the fixed 50% duty cycle method.

For the purpose of the analysis $N_{SMP} = 4$ was assumed for each arm in the primary side of the MTrMMC-DC-DC and $N_{SMS} = 3$ for the secondary side. However, $N_{SMP} = 4$ and $N_{SMS} = 3$ can be any number based on the voltage, power requirements and $\frac{dv}{dt}$ voltage stress across the transformer, and a similar analysis can be applied. Figure 4.14 depicts the gate signals and the produced multilevel voltage waveform for $V_{UA}(t)$ when different duty-cycles are used. The primary transformer phase A voltage, $V_{PT_P}\_A(t)$, and the secondary transformer phase U voltage, $V_{ST_S}\_U(t)$, are shown in figure 4.15 where $\rho_g < 1$. Knowing $V_{PT_P}\_A(t)$ and $V_{ST_S}\_U(t)$ at each interval and by applying the general expression 4.12, the voltage across L_{eq} and the ac link current, $i_{ac}\_A(t)$, can be analytically found for each interval, α, during half of the fundamental cycle as shown in table 4.8.

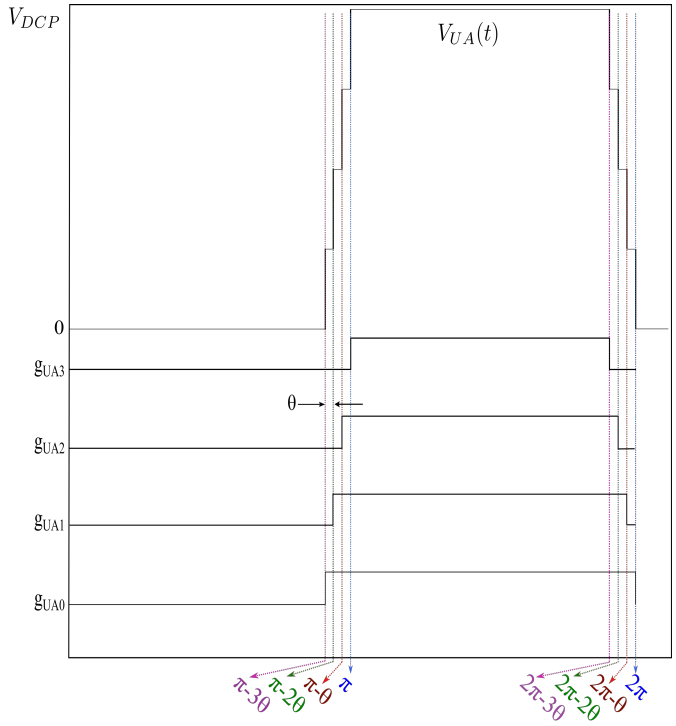


Figure 4.14: *Upper arm voltage of phase A*

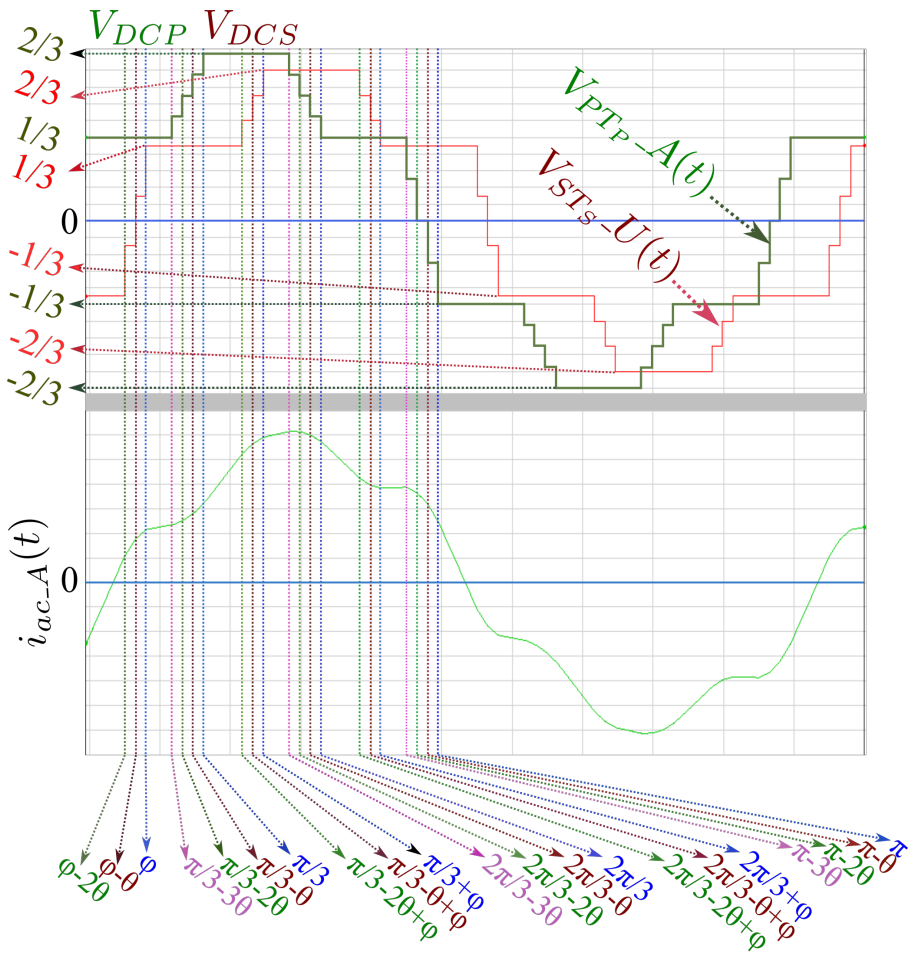


Figure 4.15: *AC link voltage and current waveforms of MTrMMC-DC-DC*

The analysis of the balancing method is discussed only for the upper arm of phase A. A similar analysis can be made for the lower arm and for the other phases. Figure 4.16 shows the phase A upper arm current, $i_{UA}(t)$, with the gate signals for the corresponding SMs. Each capacitor will be charged/discharged only when its corresponding gate signal is high and the net charge ΔQ in each capacitor will depend on the operating point and on the duty-cycle of each SM. The net charge ΔQ of each capacitor can be calculated analytically by taking the time integral of the arm current $i_{UA}(t)$ during the period when its corresponding gate signal is high. Analytically $i_{UA}(t)$ can be calculated by applying 4.64, where I_{DCP} and P_{av} are found using equation 4.108 and equation 4.107, respectively. Knowing the arm current, the analytical expression of the charge variation in each SM capacitor can be found as shown in equation 4.109.

Table 4.8: $i_{ac}\_A(\alpha)$ profile for half fundamental cycle, 0 to π, when $N_{SMP} = 4$ and $N_{SMS} = 3$

α	$i_{ac}\_A(\alpha)$	
$0 \leq \alpha \leq \varphi - 2\theta$	$i_{ac}\_A(0) + \frac{V_{DCP}(1+\rho_g)}{3\omega L_{eq}}\alpha$	(4.86)
$\varphi - 2\theta \leq \alpha \leq \varphi - \theta$	$i_{ac}\_A(\varphi - 2\theta) + \frac{V_{DCP}(1+\frac{\rho_g}{3})}{3\omega L_{eq}}(\alpha - (\varphi - 2\theta))$	(4.87)
$\varphi - \theta \leq \alpha \leq \varphi$	$i_{ac}\_A(\varphi - \theta) + \frac{V_{DCP}(1-\frac{\rho_g}{3})}{3\omega L_{eq}}(\alpha - (\varphi - \theta))$	(4.88)
$\varphi \leq \alpha \leq \frac{\pi}{3} - 3\theta$	$i_{ac}\_A(\varphi) + \frac{V_{DCP}(1-\rho_g)}{3\omega L_{eq}}(\alpha - \varphi)$	(4.89)
$\frac{\pi}{3} - 3\theta \leq \alpha \leq \frac{\pi}{3} - 2\theta$	$i_{ac}\_A(\frac{\pi}{3} - 3\theta) + \frac{V_{DCP}(\frac{5}{4}-\rho_g)}{3\omega L_{eq}}(\alpha - (\frac{\pi}{3} - 3\theta))$	(4.90)
$\frac{\pi}{3} - 2\theta \leq \alpha \leq \frac{\pi}{3} - \theta$	$i_{ac}\_A(\frac{\pi}{3} - 2\theta) + \frac{V_{DCP}(\frac{3}{2}-\rho_g)}{3\omega L_{eq}}(\alpha - (\frac{\pi}{3} - 2\theta))$	(4.91)
$\frac{\pi}{3} - \theta \leq \alpha \leq \frac{\pi}{3}$	$i_{ac}\_A(\frac{\pi}{3} - \theta) + \frac{V_{DCP}(\frac{7}{4}-\rho_g)}{3\omega L_{eq}}(\alpha - (\frac{\pi}{3} - \theta))$	(4.92)
$\frac{\pi}{3} \leq \alpha \leq \frac{\pi}{3} + \varphi - 2\theta$	$i_{ac}\_A(\frac{\pi}{3}) + \frac{V_{DCP}(2-\rho_g)}{3\omega L_{eq}} * (\alpha - (\frac{\pi}{3}))$	(4.93)
$\frac{\pi}{3} + \varphi - 2\theta \leq \alpha \leq \frac{\pi}{3} + \varphi - \theta$	$i_{ac}\_A(\frac{\pi}{3} + \varphi - 2\theta) + \frac{V_{DCP}(2-\frac{4\rho_g}{3})}{3\omega L_{eq}}(\alpha - (\frac{\pi}{3} + \varphi - 2\theta))$	(4.94)
$\frac{\pi}{3} + \varphi - \theta \leq \alpha \leq \frac{\pi}{3} + \varphi$	$i_{ac}\_A(\frac{\pi}{3} + \varphi - \theta) + \frac{V_{DCP}(2-\frac{5\rho_g}{3})}{3\omega L_{eq}}(\alpha - (\frac{\pi}{3} + \varphi - \theta))$	(4.95)
$\frac{\pi}{3} + \varphi \leq \alpha \leq \frac{2\pi}{3} - 3\theta$	$i_{ac}\_A(\frac{\pi}{3} + \varphi) + \frac{V_{DCP}(2-2\rho)}{3\omega L_{eq}}(\alpha - (\frac{\pi}{3} + \varphi))$	(4.96)
$\frac{2\pi}{3} - 3\theta \leq \alpha \leq \frac{2\pi}{3} - 2\theta$	$i_{ac}\_A(\frac{2\pi}{3} - 3\theta) + \frac{V_{DCP}(\frac{7}{4}-2\rho_g)}{3\omega L_{eq}}(\alpha - (\frac{2\pi}{3} - 3\theta))$	(4.97)
$\frac{2\pi}{3} - 2\theta \leq \alpha \leq \frac{2\pi}{3} - \theta$	$i_{ac}\_A(\frac{2\pi}{3} - 2\theta) + \frac{V_{DCP}(\frac{3}{2}-2\rho_g)}{3\omega L_{eq}}(\alpha - (\frac{2\pi}{3} - 2\theta))$	(4.98)
$\frac{2\pi}{3} - \theta \leq \alpha \leq \frac{2\pi}{3}$	$i_{ac}\_A(\frac{2\pi}{3} - \theta) + \frac{V_{DCP}(\frac{5}{4}-2\rho_g)}{3\omega L_{eq}}(\alpha - (\frac{2\pi}{3} - \theta))$	(4.99)
$\frac{2\pi}{3} \leq \alpha \leq \frac{2\pi}{3} + \varphi - 2\theta$	$i_{ac}\_A(\frac{2\pi}{3}) + \frac{V_{DCP}(1-2\rho_g)}{3\omega L_{eq}}(\alpha - \frac{2\pi}{3})$	(4.100)
$\frac{2\pi}{3} + \varphi - 2\theta \leq \alpha \leq \frac{2\pi}{3} + \varphi - \theta$	$i_{ac}\_A(\frac{2\pi}{3} + \varphi - 2\theta) + \frac{V_{DCP}(1-\frac{5\rho_g}{3})}{3\omega L_{eq}}(\alpha - (\frac{2\pi}{3} + \varphi - 2\theta))$	(4.101)
$\frac{2\pi}{3} + \varphi - \theta \leq \alpha \leq \frac{2\pi}{3} + \varphi$	$i_{ac}\_A(\frac{2\pi}{3} + \varphi - \theta) + \frac{V_{DCP}(1-\frac{4\rho_g}{3})}{3\omega L_{eq}}(\alpha - (\frac{2\pi}{3} + \varphi - \theta))$	(4.102)
$\frac{2\pi}{3} + \varphi \leq \alpha \leq \pi - 3\theta$	$i_{ac}\_A(\frac{2\pi}{3} + \varphi) + \frac{V_{DCP}(1-\rho_g)}{3\omega L_{eq}}(\alpha - (\frac{2\pi}{3} + \varphi))$	(4.103)
$\pi - 3\theta \leq \alpha \leq \pi - 2\theta$	$i_{ac}\_A(\pi - 3\theta) + \frac{V_{DCP}(\frac{1}{2}-\rho_g)}{3\omega L_{eq}}(\alpha - (\pi - 3\theta))$	(4.104)
$\pi - 2\theta \leq \alpha \leq \pi - \theta$	$i_{ac}\_A(\pi - 2\theta) + \frac{V_{DCP}(-\rho_g)}{3\omega L_{eq}}(\alpha - (\pi - 2\theta))$	(4.105)
$\pi - \theta \leq \alpha \leq \pi$	$i_{ac}\_A(\pi - \theta) + \frac{V_{DCP}(-\frac{1}{2}-\rho_g)}{3\omega L_{eq}}(\alpha - (\pi - \theta))$	(4.106)

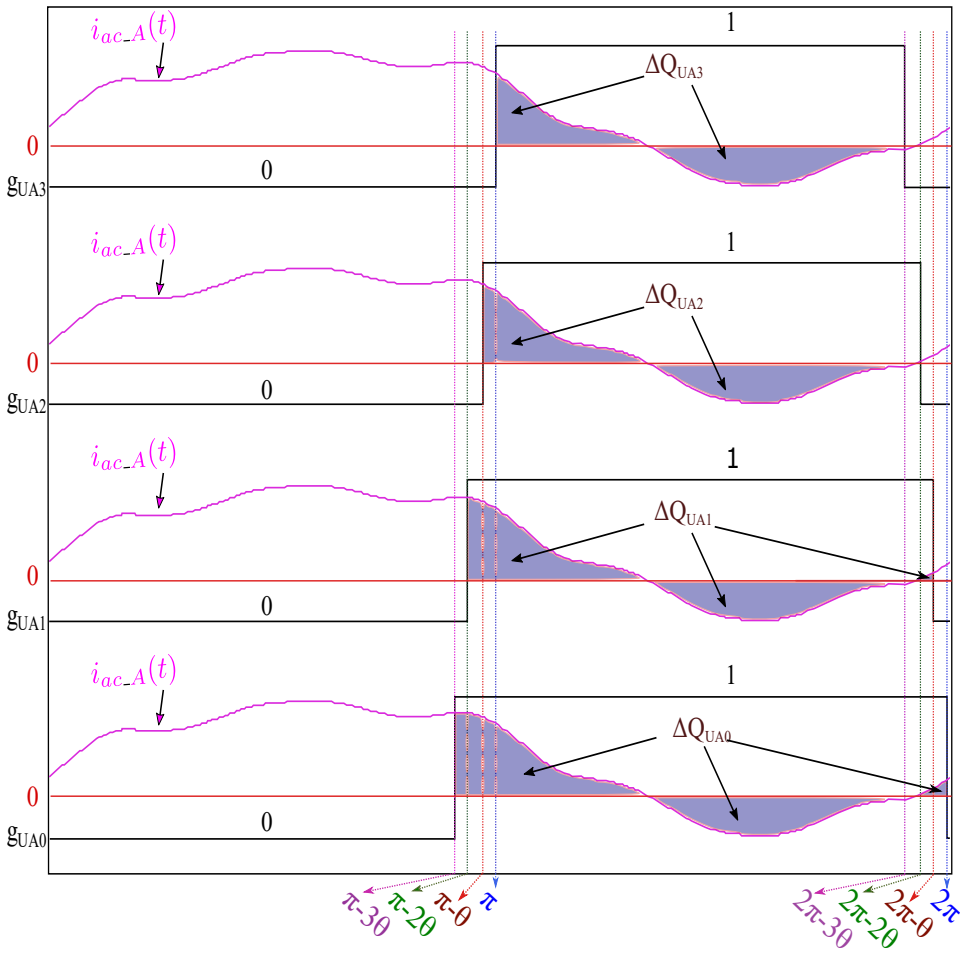


Figure 4.16: *Capacitors charge difference under uneven distribution of the duty cycles*

$$\begin{aligned} P_{av} &= \frac{3}{\pi}\int_0^{\pi} V_{PT_P}\_A(\alpha) * i_{ac}\_A(\alpha) * d\alpha \\ &= \frac{-(\rho_g V_{DCP}^2(13\theta^2+\varphi\theta-4\pi\theta+6\varphi^2-8\pi\varphi))}{12L_{eq}\omega\pi} \end{aligned} \tag{4.107}$$

$$\begin{aligned} I_{DCP} &= \frac{P_{av}}{V_{DCP}} \\ &= \frac{-(\rho_g V_{DCP}(13\theta^2+\varphi\theta-4\pi\theta+6\varphi^2-8\pi\varphi))}{12L_{eq}\omega\pi} \end{aligned} \tag{4.108}$$

$$\Delta Q_{UAi} = \frac{1}{\omega}\int_0^{2\pi} i_{UA(\alpha)} * g_{UAi} * d\alpha = \begin{cases} \frac{-(\rho_g\theta V_{DCP}(13\theta^2+6\theta\varphi-6\pi\theta+6\varphi^2-8\pi\varphi))}{12\omega^2 L_{eq}\pi} & i=0 \\ \frac{-(\rho_g\theta V_{DCP}(13\theta^2+6\theta\varphi+2\pi\theta+6\varphi^2-8\pi\varphi))}{36\omega^2 L_{eq}\pi} & i=1 \\ \frac{(\rho_g\theta V_{DCP}(13\theta^2+6\theta\varphi-10\pi\theta+6\varphi^2-8\pi\varphi))}{36\omega^2 L_{eq}\pi} & i=2 \\ \frac{(\rho_g\theta V_{DCP}(13\theta^2+6\theta\varphi-2\pi\theta+6\varphi^2-8\pi\varphi))}{12\omega^2 L_{eq}\pi} & i=3 \end{cases} \tag{4.109}$$

Summation of ΔQ_{UA1} to ΔQ_{UA4} results in zero and it is obvious that the subomdule voltage is $\Delta V_{SM} = \frac{1}{C_{SM}}\Delta Q$. Therefore, the sum of ΔV_{SMUA1}, ΔV_{SMUA2}, ΔV_{SMUA3} and ΔV_{SMUA4} will be zero and this proves the balance between the upper and lower arm voltages. It can be also observed that the ΔQ_{UAi} is a function of ρ_g, θ, φ, and the gate signal duty cycles, represented by the index i, where $i = 0$ indicates the lowest duty-cycle. Under steady state operation ρ_g, θ cannot be modified and φ is selected based on the power flow requirement. Therefore, the only factor that can be changed to balance the capacitor voltages is the duty-cycle of the gate signals. In case of power flowing from the primary to secondary, the balancing can be achieved by assigning the highest to lowest duty cycle gate signals to the ascending sorted SMs. The block diagram in figure 4.17 shows the implementation details of the new capacitor balancing approach where V_{SM_Max} and V_{SM_Min} are the maximum average SM voltage and minimum average SM voltage over the fundamental period, respectively. The SM voltages are sorted at fundamental frequency and this leads to switching the SMs at fundamental frequency. Consequently, device switching losses will be small in comparison to device conduction losses when $f_o \leq 500Hz$ hence high efficiency can be achieved in HVDC applications when this method of balancing is implemented.

Similar approach is used to derive the expressions for the charge distribution among the SMs using the fixed 50% duty cycle method shown in figure 4.5-a. Equation 4.110 shows the charge variation in each SM capacitor, ΔQ_{UAi_FD}, where FD represents fixed duty cycle.

$$\Delta Q_{UAi\_F} = \frac{1}{\omega}\int_0^{2\pi} i_{UA(\alpha)} * g_{UAi} * d\alpha = \begin{cases} \frac{(\theta V_{DCP}(4\pi - 7\theta + 6\rho_g\varphi - 4\pi\rho_g + 5\rho_g\theta))}{12\omega^2 L_{eq}} & i = 0 \\ \frac{-(\theta V_{DCP}(6\theta - 4\pi - 6\rho_g\varphi + 4\pi\rho_g + 3\rho_g\theta))}{36\omega^2 L_{eq}} & i = 1 \\ \frac{-(\theta V_{DCP}(4\pi - 6\theta + 6\rho_g\varphi - 4\pi\rho_g + 9\rho_g\theta))}{36\omega^2 L_{eq}} & i = 3 \\ \frac{-(\theta V_{DCP}(4\pi - 7\theta + 6\rho_g\varphi - 4\pi\rho_g + \rho_g\theta))}{12\omega^2 L_{eq}} & i = 3 \end{cases} \tag{4.110}$$

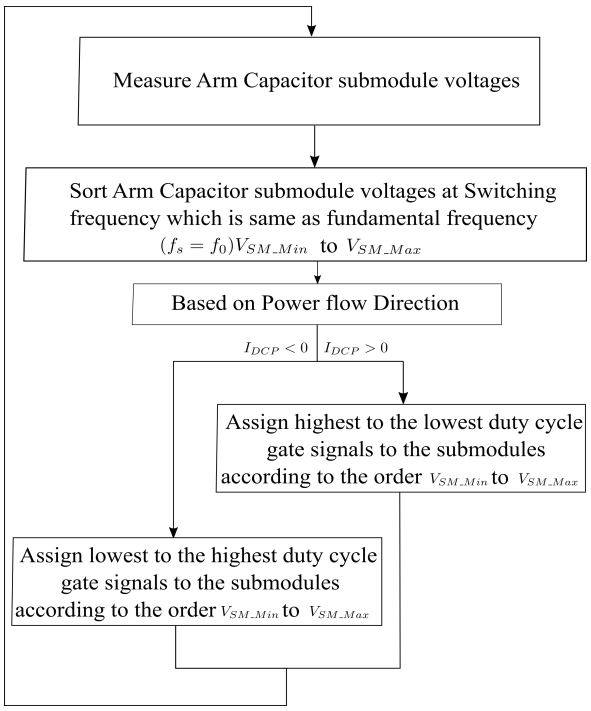


Figure 4.17: *Capacitor voltage balancing method*

The specification shown in table 4.9 have been substituted in equations 4.109 and 4.110 to calculate the net charge of each SM capacitor for both the individual-duty cycle method and fixed 50% duty cycle method, respectively. Table 4.10 shows the net charge of each SM capacitor for both the methods and it can be seen that the net charge for the gate signal, g_{UA0}, is higher when the individual-duty cycle method is used and the net charge for the gate signal, g_{UA3}, is smaller when the individual-duty cycle method is used. Therefore, by assigning the gate signal with a higher net charge to the SM capacitor with the lowest voltage and vice versa, a faster SM capacitor voltage balancing will be achieved.

Table 4.9: System specifications and parameters

Parameters	Value
V_{DCP}	$400kV$
f_o	250 Hz
ρ_g	1
L_{eq}	10 mH
N_{st}	4
$T_{dP} = T_{dS}$	15µs
θ	0.0075π
φ	0.05π

Table 4.10: Net charge of SM capacitors

g_{UAi}	ΔQ_{UAi} (C)	ΔQ_{UAi_F} (C)
g_{UA0}	0.0427	0.0285
g_{UA1}	0.0122	0.0077
g_{UA2}	-0.0152	-0.0107
g_{UA3}	-0.0397	-0.0255

4.4 Control of the MMC-DC-DC with trapezoidal modulation

This section will focus on the control structure of the MTrMMC-DC-DC. Firstly it presents the average power flow control. Secondly, it shows the novel energy control for trapezoidal wave-shaping.

4.4.1 Power flow control

Transferred power between the two DC-link ports can be controlled by controlling the voltage angle, φ, between the primary and secondary arm modulation signals which determines the phase shift between the primary and secondary transformer voltages, $V_{PT_P}\_\phi P(t)$, $V_{ST_S}\_\phi S(t)$. From equation 4.66, the voltage angle, φ, can be determined as a feed-forward signal. A PI controller can then be used to generate a correction, $\Delta\varphi$, to account for losses etc, so that the correct power is transferred. Figure 4.18 shows the schematic control diagram of the AC power flow control where the gain $K_s = \frac{\rho_g V_{DCP}^2 (2\pi - 3\varphi)}{3 L_{eq} \omega \pi}$. The arm modulation signals of the primary are fixed and the secondary arm modulation signals are shifted by φ_{ref} to deliver the desired power.

In the applications where control of the DC link voltage ports and fast power flow control are not required, the control structure of the MtrMMC-DC-DC will be only use power flow control by controlling φ slowly. The method presented in the previous section, section 4.3, can be used to balance the voltage of the submodule

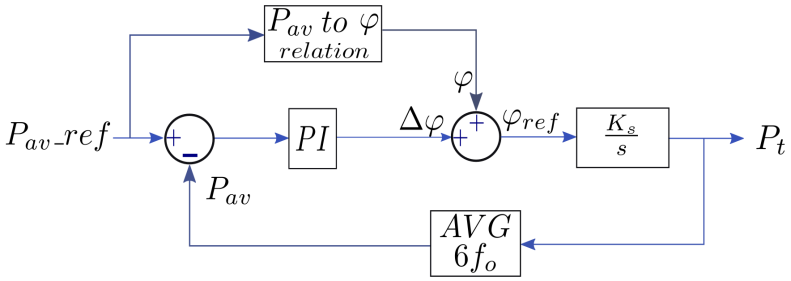


Figure 4.18: *Power flow control scheme*

capacitors. Controlling φ between the primary and secondary chain-link voltages and using SM capacitor voltage balancing method will force the chain-link slowly to the voltage that is required to drive the power demand in steady state without controlling the voltage of the chain-links.

4.4.2 Chain-link Energy and DC Current Control in MTrMMC-DC-DC

It is essential to control the voltage of the chain-link capacitors during transients, when the power demand is changed rapidly, to prevent an unacceptable rise and oscillations in the SM capacitor voltages and the DC current can happen because of two main reasons. Operating at $fr = \frac{2f_o}{1.5}$ is essential to keep the arm current continuous and to operate at minimum energy requirements for the converter. Accordingly, taking the size of the passive elements into account, the choice of the arm inductors and the arm equivalent SM capacitance makes the total DC loop impedance small when the power demand changes the mean voltage of the chain-links will change to drive the desired power from one port to another. Any change in the voltage of the chain-links causes an unacceptable rise or fall in DC current because of the low DC loop impedance, if the change of the voltage of the chain-links is not controlled.

Secondly, considering one phase, all SMs of one chain-link are either inserted for the majority of half the period and bypassed for the other half and the duty ratio of SMs is unchanged over the period. Therefore, considering one phase, at the instant when the step change in power demand occurs, the voltage of the inserted chain-

link, either the voltage of the lower arm SM capacitors or the voltage of the upper arm SM capacitors, will be forced to change. As a result, divergence between the voltage of the upper chain-link and lower chain-link will occur for many cycles in case of uncontrolled chain-link voltages. The sorting and balancing the SM capacitor voltages will eventually balance the voltage across the SM capacitors of upper and lower chain-links after many cycles. Additionally, the divergence between the uncontrolled voltage of the chain-links will increase as the step change of power demand change increases. The divergence between the uncontrolled voltage of the chain-links reaches a maximum in the first cycle and can create significant oscillations in the DC and arm currents. The voltage error also affects the common mode current during transients and can result in significant increase and oscillation in the AC link current response.

Therefore, although the trapezoidal MMC DC-DC converter can operate without voltage control of the chain-links in steady state and during slow transients, it is essential to implement chain-link voltage control to deal with fast transients for the reasons outlined above.

Finally, in applications where one of the DC sides is a load (not a fixed DC voltage), controlling the voltage of the SMs of the load side is essential even if the power changes slowly.

A novel approach is proposed to modify the modulation signals of the SMs in order to achieve the voltage control of the SM capacitors. A per phase controller is used where the total energy stored in each arm tracks the required reference value through an outer voltage loop which provides a DC current reference for an inner loop as presented in figure 4.19. The plant transfer functions for the DC loops are shown in figure 4.20 where L and R represent L_p and R_p for the primary MMC and L_s and R_s for the secondary MMC. A PI compensator is used to generate the signal ΔV which is compared to a fundamental frequency carrier signal to modify the

switching signal of the corresponding chain-link.

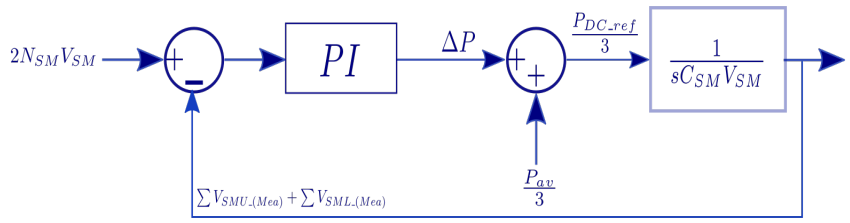


Figure 4.19: *Per phase energy control scheme*

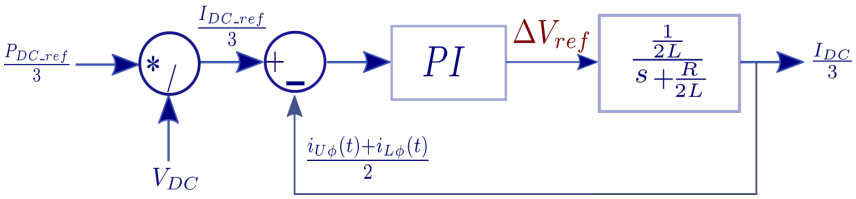


Figure 4.20: *Per phase DC current control scheme*

Furthermore, since the parasitic resistance (R_p and R_s) of the arm inductor is very small, the resistive voltage drop will be small and this voltage is required to drive the necessary current to deliver the desired power. Accordingly, modifying one of the levels of the arm modulation waveform is enough to correct the total voltage of the chain-link (total arm voltage) in order to control the stored energy. For this reason, ΔV_{ref} is compared with a carrier waveform fundamental frequency to modify the arm modulation waveform as shown in figure 4.21 in more detail. Then, based on the level of the modified arm modulation waveform and applying the balancing algorithm presented in the previous section, section 4.3, the SMs will be inserted or bypassed. In addition, modifying more than one level is achievable if required, in case of a large transient, by comparing the number of levels with a triangle carrier which may be at a higher frequency than fundamental frequency if required. A delay time must be introduced between each level to ensure the stair case which is essential for preventing high $\frac{dv}{dt}$ stress across the transformer. The energy and current control is applied only at transients when the power demand changes rapidly. During steady state the proposed balancing method will be enough to keep the SM capacitor voltages well balanced at the desired value.

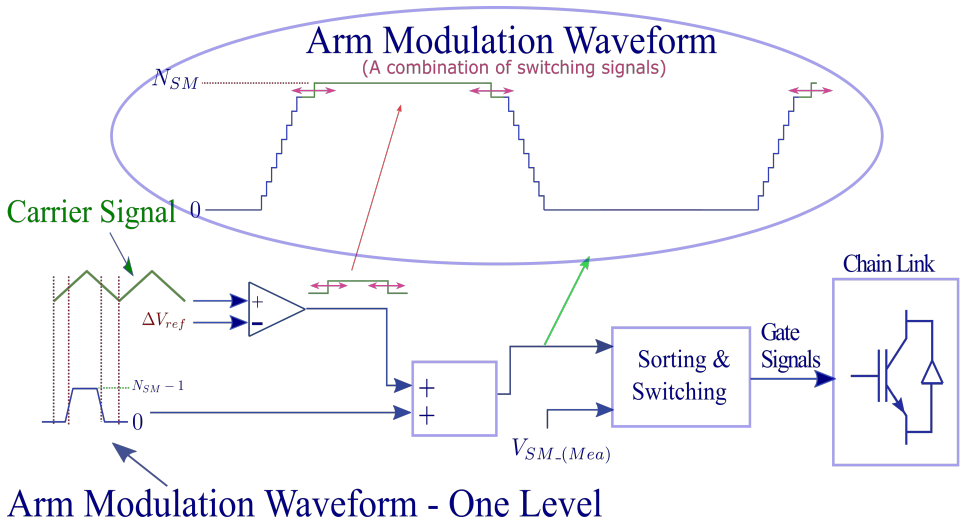


Figure 4.21: *Schematic of proposed energy control*

4.5 Summary

This chapter focused mainly on introducing a modified trapezoidal operation of the modular multilevel DC-DC converter for HVDC system interconnection. It showed the principle operation of the proposed topology where continuous conduction of the arm currents was achieved due to the resonant between the arm inductance and equivalent capacitance of the inserted SMs. It also presented the intensive analysis of the voltage and current waveforms and from the analysis, the passive components, arm inductor and SM capacitor, were designed. Additionally, the voltage and current ratings of the semiconductor device were shown. The produced stair case voltage waveform applied to the transformer was shown and the trade-off selections between operation frequency, transition period, T_t, energy storage requirement, voltage stress, $\frac{dv}{dt}$, across the transformer, were demonstrated.

Furthermore, a new SM capacitor voltage balancing method was introduced with an analytical charge distribution support. The requirements for controlling the current and chain-link energy were clarified and an energy control approach was proposed.

In the next chapter, a comprehensive comparison will be demonstrated between the sinusoidal MMC-DC-DC, TrMMC-DC-DC and the MTrMMC-DC-DC configurations in terms of the semiconductor power losses, *VA* product requirement which reflects on the cost and area of semiconductor, energy storage requirements, transformer voltage stress, device current stress and device utilisation. Additionally, an HVDC system with power of 800MW and DC link voltages of 400kV ($\pm 200\ kV$) will be built in PLECS software to validate the proposed operating mode, theoretical analysis for the component design, the proposed balancing SM capacitor voltage and the proposed energy control.

Chapter 5

Comparison and Simulation Results

5.1 Introduction

This chapter demonstrates a comprehensive comparison between three operating modes of the MMC-DC-DC, sinusoidal MMC-DC-DC, TrMMC-DC-DC and MTrMMC-DC-DC, in terms of semiconductor power loss, energy storage requirement, device utilisation, semiconductor *VA* requirement, DC fault performance, transformer $\frac{dv}{dt}$ stress and semiconductor device current stress.

An HVDC system with both the TrMMC-DC-DC and MTrMMC-DC-DC operating modes will be built in PLECS software to firstly support the comparison results. Secondly, to validate the MTrMMC-DC-DC mode, theoretical analysis for the component design, the proposed balancing SM capacitor voltage described in section 4.3 and the proposed energy control presented in section 4.4.2.

5.2 Comparison and simulation results

This section focuses on a comprehensive comparison between the following options for HVDC applications:

- Sinusoidal operation of the modular multilevel DC-DC converter
- Trapezoidal operation of the modular multilevel DC-DC converter, TrMMC-DC-DC, introduced in the literature (section 3.2.2.2)
- Modified trapezoidal operation of the modular multilevel DC-DC converter, MTrMMC-DC-DC, which was proposed in previous chapter

Comparisons are made on the bases of energy storage requirements, semiconductor device switching and conduction losses, semiconductor device ratings, semiconductor device utilisation and $\frac{dv}{dt}$ stress across the transformer. Sinusoidal operation of MMC-DC-DC is chosen as a benchmark since it is a well know configuration and is considered as a promised conversion solution in the literature for HVDC interconnections. The TrMMC-DC-DC presented in subsection 3.2.2.2 was chosen due to its attractive advantages in terms of reduced energy requirements in comparison to non-trapezoidal operating modes, modularity and device current rating in comparison to other trapezoidal operating modes introduced in the literature.

Semiconductor power loss is an important aspect to be addressed in all three operating modes for the purpose of comparison. Therefore, the loss evaluation will be presented for all operating modes. Conduction and switching losses are considered separately. An analytical approximation of the power losses will be derived for all operating modes.

In all three operating modes of the MMC-DC-DC converter, half-bridge SMs are used which consist of two IGBT devices with anti-parallel diodes. The possible conduction states of the half-bridge SMs was shown in table 4.1 which also indicated the conduction device and the direction of the current. The number of "on" SMs and "off" SMs can be approximated as shown in equation 5.1 and equation 5.2, respectively where $v_{ch}(t)$ is the instantaneous chain-link voltage to be produced.

$$N_{on}(t) = \frac{v_{ch}(t)}{V_{SM}} \tag{5.1}$$

$$N_{off}(t) = N_{SM} - N_{on}(t) \tag{5.2}$$

In order to evaluate conduction losses a constant voltage drop in series with a resistance is used to approximate the forward characteristic of the devices. Equation 5.3 gives the instantaneous conduction losses, $Pc_{device}(t)$, of each device approximately where $Vd_{device}(t)$ is the instantaneous voltage drop of the device, $i(t)$ is the instantaneous current flowing through the device. Additionally, Vf and Rf are the voltage drop and the equivalent device resistance , respectively, and can be derived from the device datesheet. The expression in 5.4 presents the total instantaneous conduction losses, $P_{Con}(t)$, of each chain-link.

$$\begin{aligned} Pc_{device}(t) &= Vd_{device}(t) * i(t) \\ vd_{device}(t) &= Vf + Rf * i(t) \end{aligned} \tag{5.3}$$

$$P_{Con}(t) = \begin{cases} N_{on}(t)P_{diode}\big(i_{ch}(t)\big) + N_{off}(t)P_{IGBT}\big(i_{ch}(t)\big),\ if\ i_{ch}(t) \geq 0 \\ N_{off}(t)P_{diode}\big(i_{ch}(t)\big) + N_{on}(t)P_{IGBT}\big(i_{ch}(t)\big),\ if\ i_{ch}(t) < 0 \end{cases} \tag{5.4}$$

In each SM two types of commutation will occur. In the first commutation an IGBT turns off and a diode turns on and the switching losses can be evaluated as given in expression 5.5 where E_{off} is the Turn-off energy loss of the IGBT. In the second commutation type an IGBT turns on and a diode turns off. In this case, the switching losses can be evaluated as given in equation 5.6 where E_{on} and E_r are the energy loss of the IGBT during turn on and energy recovery loss of the diode during turn off, respectively. E_{off}, E_{on} and E_r are given in the manufacture datasheets at nominal voltage, V_n and nominal current, I_n. They are assumed to be proportional to voltage and current for normalisation to different operation condition. Considering sinusoidal operation, the instantaneous switching loss can be derived as expression 5.7, assuming that all SMs are switching at the sorting frequency. In trapezoidal operation, the switching actions occur only during T_t and equation 5.7 is applicable only at voltage levels where sorting the SMs is enabled. However for voltage levels where SM sorting is disabled equation 5.8 is used where N_L is the number of the

SMs per chain-link voltage level as defined in section 4.2.1.1.

$$E_{SWoff}(t) = \frac{E_{off}|i_{ch}(t)|V_{SM}}{V_n I_n} \tag{5.5}$$

$$E_{SWon}(t) = \frac{(E_{on}+E_r)|i_{ch}(t)|V_{SM}}{V_n I_n} \tag{5.6}$$

$$P_{sw}(t) \approx \left\{ \quad f_{sw} N_{on}(t) \left(\frac{(E_{off}+E_r+E_{on})|i_{ch}(t)|V_{SM}}{V_n I_n} \right) \right. \tag{5.7}$$

$$P_{sw}(t) \approx \left\{ \quad f_{sw} N_L \left(\frac{(E_{off}+E_r+E_{on})|i_{ch}(t)|V_{SM}}{V_n I_n} \right) \right. \tag{5.8}$$

Total power losses are determined by summing the individual commutation losses over a fundamental cycle. Table 5.1 shows the HVDC system specifications and parameters that are used for the purpose of the comparisons between all three operating modes. The DC link voltage of $400kV$ $(\pm 200kV)$ has been chosen as it is one of the HVDC voltage standard used in the UK. Table 5.2 shows the semiconductor device characteristics chosen for the half bridge SMs, HiPak IGBT module 5SNA 1800E330400. In the MMC-DC-DC operating modes, the number of the SMs is calculated as $N_{SM} = \frac{V_{DC}}{V_{SM}}$ where the nominal SM voltage, $V_{SM} = 2kV$, is chosen based on the recommended applied voltage across the IGBT from datasheet. The parameters N_{st}, N_L and T_d are only relevant to the TrMMC-DC-DC and MTrMMC-DC-DC operating modes and the selection is made based on the their trade-off impacts on the transformer $\frac{dv}{dt}$ stress, energy storage requirement, chain-link voltage waveform modulation index and device current rating described in sections 4.2.1.1, 4.2.1.2, 4.2.2.2 and 4.2.2.3.

5.2.1 Sinusoidal Operation of the MMC-DC-DC semiconductor power Losses and Sizing Evaluation

Sinusoidal operation of the MMC-DC-DC was explained in subsection 3.2.2.1 and the necessary mathematical equations and waveforms regarding voltages, currents

Table 5.1: HVDC system specifications and parameters

Parameters	Value
$V_{DCP} = V_{DCS}$	$400kV(\pm 200kV)$
P_r	800 MW
f_o	250 Hz
Turns ratio (n)	1
$L_k 10\%$	8.6 mH
V_{SM}	2kV
N_{SM} *Per Chain-Link*	200
N_{st}	20
$N_{LP} = N_{LS}$	10
$T_{dP} = T_{dS}$	15µs

Table 5.2: HiPak IGBT module 5SNA 1800E330400 characteristics at $T_j = 125°C$

Parameters	Value	Unit
Vf_{IGBT}	2.7578	V
Rf_{IGBT}	1.05	mΩ
Vf_{Diode}	2.2	V
Rf_{Diode}	0.6633	mΩ
E_{on}	4.3	J
E_{off}	4	J
E_r	2.3	J
V_n	1800	V
I_n	1800	V

and energy were presented. In order to compare the semiconductor requirements For each configuration, the total device VA product with respect to the rated power for the converter, VA_{MMC}, is defined as equation 5.9 where $\hat{Ich_{MMC}}$ is peak of the chain-link current. This gives a simple way of comparing the relevant cost and area of the semiconductors used.

$$\begin{aligned} VA_{MMC} &= \frac{12N_{SM}V_{SM}\hat{Ich_{MMC}}}{Pr} \\ \hat{IchP}_{MMC} &= \frac{2Pr}{3\frac{V_{DCP}}{2} * m_p} + \frac{Pr}{3V_{DC}} \end{aligned} \tag{5.9}$$

Table 5.1 gives HVDC specifications and the calculated parameters for the MCC-DC-DC modes. The value of the SM capacitor, arm inductor and the energy requirements for the sinusoidal MMC-DC-DC can be calculated using equations 3.10, 3.13 and 3.12, respectively, where the per unit peak to peak SM voltage ripple, $\delta_{pp} = 10\%$, is considered based on the optimum possible region of operation. The

modulation index of the primary side, m_p, of the converter is imposed and through a standard dq control structure the modulation index of the secondary side and the power flow are controlled. The chain-link energy requirements of both sides of the converter is controlled accordingly to achieve power flow control. With sinusoidal operation a wide rang of modulation index is achievable if required particularly for the purpose of control during transients or fault events.

The total average semiconductor power losses, $T_{L\_MMC} = \frac{Losses_{AVG}}{Pr} * 100$, are evaluated considering that the switching frequency of the SMs is the same as the sorting frequency, $f_{sw} = f_{sort} = 10 * f_o$.

Sinusoidal operation provides reasonable semiconductor devices utilisation by inserting and bypassing the required SMs at every voltage level of chain-link voltage.

Table 5.3 shows the evaluation of the semiconductor power losses (T_{L_MMC}), VA_{MMC}, and the energy requirements of the sinusoidal operating mode where H_{cMMC} is the capacitance constant for the sinusoidal configuration.

Table 5.3: Specifications and parameters of the sinusoidal mode

Parameters	Value
VA_{MMC}	12.42
$L_P = L_S$	3.6 mH
$C_{SMP} = C_{SMS}$	3 mF
δ_{pp}	10%
H_{cMMC}	18.4 ms
m_p	0.95
T_{L_MMC}	1.91%

5.2.2 TrMMC-DC-DC semiconductor power Losses and Sizing Evaluation, and Simulation Results

Trapezoidal operation of the MMC-DC-DC shown in figure 5.1 was introduced in subsection 3.2.2.2. Here, the mode is investigated in more detail since it will be used as a benchmark for the comparisons. As clarified in subsection 3.2.2.2, apart from the transition period, T_t, only one arm is conducting in this mode and the arm current equal to the ac link current during the conduction period as shown in figure 3.7. Therefore, equations 4.72-4.81 are modified to equations 5.10-5.19, respectively in order to determine the SM capacitor value where $\_G$ at the end of each parameter refers to this mode of operation. Considering unity ρ_g, the expressions 5.14 and 5.15 show the value of the equivalent arm SM capacitance, C_{eqP}, at voltage angles $0 < \varphi \leq \omega T_t$ and $\omega T_t \leq \alpha \leq \varphi + \omega T_t$, respectively.

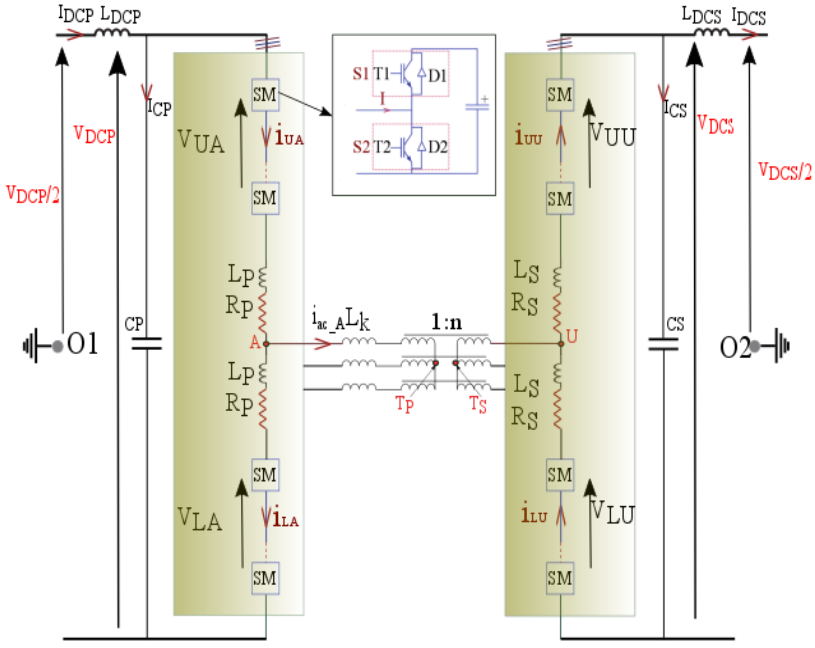


Figure 5.1: *Trapezoidal MMC DC-DC converter*

$$C_{eqP\_G} = \frac{\gamma\varphi^2(1-\frac{\varphi}{3\omega T_t})}{3L_{eq}\delta_{pp}\omega^2} \tag{5.14}$$

$$C_{eqP\_G} = \frac{\gamma T_t(3\varphi-\omega T_t)}{9L_{eq}\delta_{pp}\omega} \tag{5.15}$$

Table 5.4: Primary arm equivalent SM capacitance

φ	ρ_g	α	C_{eqP_G}	
$\omega T_t \leq \varphi \leq \frac{\pi}{3} - \omega T_t$	$\rho_g \geq 1$	$\varphi \leq \alpha \leq \omega T_t + \varphi$	$C_{eqP\_G} = \frac{\gamma}{\omega * V_{DCP} * \delta_{pp}} \int_{\alpha=\varphi}^{\alpha=(\omega T_t+\varphi)} (\text{Equ.4.15}) d\alpha$	(5.10)
$\omega T_t \leq \varphi \leq \frac{\pi}{3} - \omega T_t$	$\rho_g < 1$	$\pi \leq \alpha \leq \pi + \omega T_t$	$C_{eqP\_G} = \frac{\gamma}{\omega * V_{DCP} * \delta_{pp}} \int_{\alpha=\pi}^{\alpha=(\pi+\omega T_t)} (\text{Equ.4.13}) d\alpha$	(5.11)
$0 < \varphi \leq \omega T_t$	$\rho_g \geq 1$	$\omega T_t \leq \alpha \leq \omega T_t + \varphi$	$C_{eqP\_G} = \frac{\gamma}{\omega * V_{DCP} * \delta_{pp}} \int_{\alpha=\omega T_t}^{\alpha=(\omega T_t+\varphi)} (\text{Equ.4.41}) d\alpha$	(5.12)
$0 < \varphi \leq \omega T_t$	$\rho_g < 1$	$\pi + \varphi \leq \alpha \leq \pi + \omega T_t$	$C_{eqP\_G} = \frac{\gamma}{\omega * V_{DCP} * \delta_{pp}} \int_{\alpha=\pi+\varphi}^{\alpha=(\pi+\omega T_t)} (\text{Equ.4.40}) d\alpha$	(5.13)

$$C_{gP\_G} = N_{st} C_{eqP\_G} \tag{5.16}$$

$$C_{gS\_G} = \rho_g^2 n^2 C_{gP\_G} \tag{5.17}$$

$$C_{SMP\_G} = N_{LP} C_{gP\_G} \tag{5.18}$$

$$C_{SMS\_G} = N_{LS} C_{gS\_G} \tag{5.19}$$

The arm inductors L_P and L_S represent the total series inductance of the devices and the additional inductors which limit the arm current during transient/fault conditions for both the primary and secondary sides of the converter, respectively. The arm inductor should be large to limit the current during transient or fault events however, to prevent high current oscillation, the resonance between the arm inductor, (L_P, L_S) and the equivalent SM capacitance when all SMs are inserted, C_{eqP_G}, has to be designed according to equation 5.20 and as a result the arm inductor will be small. Consequently, the arm inductor cannot limit the inrush current sufficiently during DC fault events and this can be considered as one of the disadvantages of this mode. As a result, inductive filters are required to limit the current inrush and to protect the semiconductor devices (diodes) form damage at DC fault events.

$$fr_G = \frac{1}{2\pi\sqrt{L_P C_{eqP\_G}}} \geq 15 * 2 f_o \tag{5.20}$$

The parameters and specifications required for the TrMCC-DC-DC mode calculated considering the HVDC specifications and parameters given in table 5.1. The value of the SM capacitor, (C_{SMP_G},C_{SMS_G}) and arm inductor (L_P,L_S) calculated based

on 5.14-5.20. The energy requirements for the TrMMC-DC-DC calculated based on equations 4.82-4.84 where the per unit peak to peak SM voltage ripple, $\delta_{pp} = 5\%$, is chosen considering that the SMs can be sorted at high frequency, $f_{sort} \geq \frac{1}{2T_d}$ (every two voltage levels), during the transition period, T_t, assuming that all SMs are switching at sorting frequency. Notably, sorting 2400 SMs required for defined system at every $f_{sort} = \frac{1}{2T_d} \approx 33.333kHz$ during transition period, T_t, can be practically difficult therefore to reduce sorting frequency higher SM capacitor value is needed hence the peak to peak SM voltage ripple will be smaller and higher energy storage the system will be. Choosing $\delta_{pp} > 5\%$ is challenging since the SM capacitance will be very small and this results in high impedance of the SM when it is inserted even at $f_o = 250Hz$. Since high current passes through the inserted SMs during the transition period, T_t, the SM capacitor voltage reaches to unacceptable value even if the SMs can be sorted and grouped at every voltage level, T_d.

Table 5.5 presents the specifications and parameters of the TrMMC-DC-DC where the total average semiconductor power losses, $T_{L\_TrMMC} = \frac{Losses_{AVG}}{Pr} * 100$, is evaluated using equations 5.1-5.8 at different sorting frequency and the total device VA product as a percentage of rated power for the TrMMC-DC-DC mode, VA_{TrMMC}, calculated using equation 5.21 where according to the operating conditions, the peak value of the chain-link current, $\hat{Ich_{TrMMC}}$, can be varies. Table 5.6 shows the intervals where the TrMMC-DC-DC arm current reaches the maximum value according to the operating conditions.

$$VA_{TrMMC} = \frac{12N_{SM}V_{SM}\hat{Ich_{TrMMC}}}{Pr} \tag{5.21}$$

An HVDC conversion system with the specifications defined in table 5.1 has been simulated in PLECS software to validate the analytical derivation of the SM capacitances (C_{SMP_G}, C_{SMS_G}), the arm inductances (L_P, L_S), the TrMMC-DC-DC capacitance constant (H_{cTrMMC}) and VA_{TrMMC}. Figure 5.2 shows the waveforms of the

Table 5.5: Specifications and parameters of the TrMMC-DC-DC

Parameters	Value
$L_{p\_G} = L_{s\_G}$	20µH
$C_P = C_S$	5.7µF
$C_{SMP\_G} = C_{SMS\_G}$	0.7mF
$C_{gP\_G} = C_{gS\_G}$	70µF
φ	0.0355π
δ_{pp}	5%
H_{cTrMMC}	6 ms
T_{L_TrMMC} ($f_{sort} = \frac{1}{T_d}$)	1.42%
T_{L_TrMMC} ($f_{sort} = \frac{1}{2T_d}$)	2.3%
VA_{TrMMC}	13

Table 5.6: TrMMC-DC-DC Peak arm current

φ	ρ_g	α	$i_{UA}\_A(\alpha)$	
$\omega T_t \leq \varphi \leq \frac{\pi}{3} - \omega T_t$	$\rho_g \geq 1$	$\frac{\pi}{3} + \varphi \leq \alpha \leq \frac{\pi}{3} + \omega T_t + \varphi$	$i_{UA}_A(\alpha) = \lvert$Equ.4.19$\rvert$	(5.22)
$\omega T_t \leq \varphi \leq \frac{\pi}{3} - \omega T_t$	$\rho_g < 1$	$\frac{2\pi}{3} \leq \alpha \leq \frac{2\pi}{3} + \omega T_t$	$i_{UA}_A(\alpha) = \lvert$Equ.4.21$\rvert$	(5.23)
$0 < \varphi \leq \omega T_t$	$\rho_g \geq 1$	$\frac{\pi}{3} + \omega T_t \leq \alpha \leq \frac{\pi}{3} + \omega T_t + \varphi$	$i_{UA}_A(\alpha) = \lvert$Equ.4.45$\rvert$	(5.24)
$0 < \varphi \leq \omega T_t$	$\rho_g < 1$	$\frac{2\pi}{3} \leq \alpha \leq \frac{\pi}{3} + \varphi$	$i_{UA}_A(\alpha) = \lvert$Equ.4.47$\rvert$	(5.25)

phase A upper chain-link voltage, $V_{UA}(t)$, phase A lower chain-link voltage, $V_{LA}(t)$, primary DC link current, I_{DCP}, three phase AC link current, $i_{ac}(t)$, phase A upper arm current, $i_{UA}(t)$, phase A lower arm current, $i_{LA}(t)$, sum of upper SM capacitor voltages per group (level), $V_{CgP\_GU}(t)$, and sum of lower SM capacitor voltages per group (level), $V_{CgP\_GL}(t)$, respectively. The chain-link voltage waveforms, the AC link current waveforms, the 5% peak to peak SM voltage ripple, the discontinuous arm current and small oscillation of the arm current during T_d, validate the TrMMC-DC-DC configuration and the parameter selection analysis. During the steady state operation when the SM capacitors per group (level), $V_{CgP\_G}(t)$, are bypassed, a slight voltage divergence can be observed for the last couple of groups. However, the SM capacitor voltages per group become balanced when they are re-inserted. This occurs because the SM capacitor voltages are not sorted at every voltage level and during bypass operation of the SMs of last few groups a significant current passes through the SM capacitors, resulting in divergence in the SM capacitor volt-

ages of the last few groups (levels) with respect to the SM capacitor voltages of the other bypassed groups.

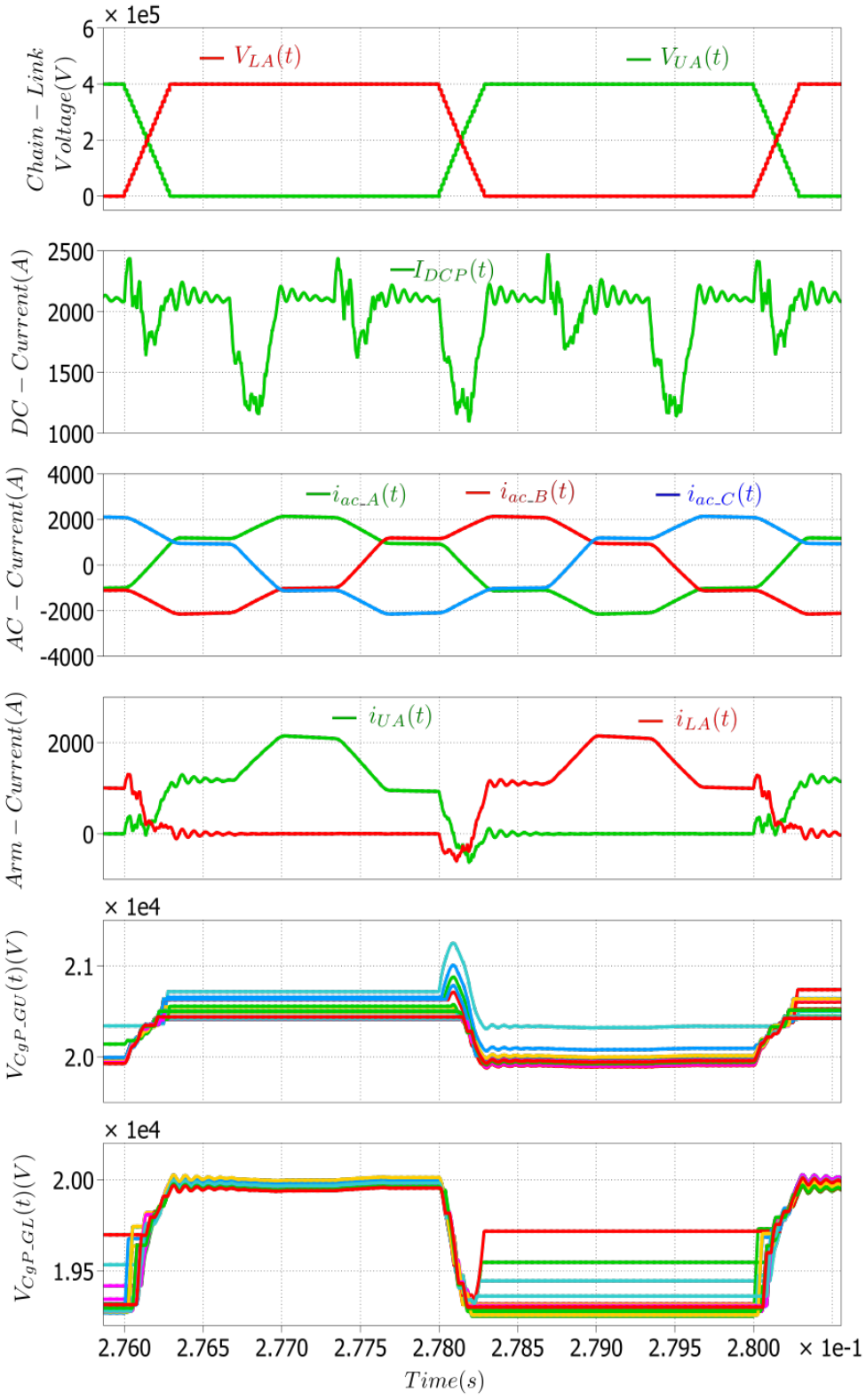


Figure 5.2: *TrMMC-DC-DC waveforms*

Ideally, when there is no energy fluctuation between the upper and lower arms (SM capacitor voltages remain fixed over the fundamental cycle), the transition period, T_t, is very small and sorting is implemented at every chain-link voltage level, the DC current contains the multiple of the sixth harmonics (6^{th}, 12^{th}, etc) as shown in section 3.2.2.2-figure 3.8. However, due to the small energy fluctuation between the arms, the DC current contains tripln harmonics (3^{rd}, 9^{th}, etc) in addition to the sixth harmonics. Figure 5.3 shows the dominant harmonics of the primary DC current, I_{DCP}, and three phase AC link currents, i_{ac}. The tripln harmonics (3^{rd},& 9^{th}) and the multiple of the sixth harmonics (6^{th}, 12^{th},& 18^{th}) can be seen in the DC current while only apart from the tripln harmonics, the other odd harmonics (5^{th}, 7^{th}, 11^{th}, etc) can be seen in the AC currents.

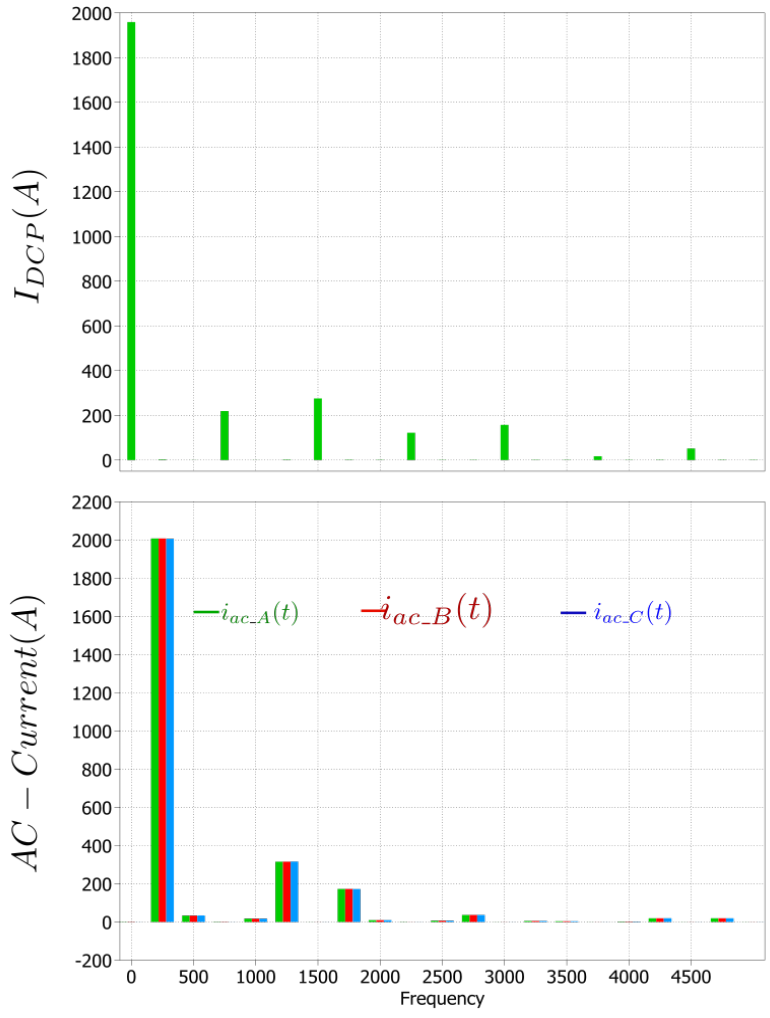


Figure 5.3: *FFT of DC and AC current in TrMMC-DC-DC*

Since the arm current is discontinuous in the TrMMC-DC-DC, the DC current contains significant ripple at frequencies, $3f_o$ and $6f_o$, DC link filters are required. Using only inductive filter is not possible due to the resonance between the inductance of the filter and the equivalent SM capacitance even at low inductance value as can be demonstrated using equation 5.20. Hence, the author in [92] derived equations 5.26 to calculate the size of the DC link filter, C_X, to keep the DC current ripple within the acceptable range, $\delta_{dc} \leq 5\%$, where δ_{dc} is per unit peak to peak voltage ripple across the DC link capacitor. However, using only a capacitive filter results significant device current stress during fault. As a result, in addition to the capacitive filter, inductive filter is required to limit the current inrush and to protect the semiconductor devices (diodes) form damage at DC fault events. Equation 5.27 is derived to calculate the required DC link inductance, L_{dc}, for the TrMMC-DC-DC operating mode.

$$C_P = \gamma \frac{\varphi^2}{2\omega^2 L_{eq} \delta_{dc}} \tag{5.26}$$

$$3f_o \geq 1.25 \frac{1}{2\pi\sqrt{L_{dcX} C_X}} \tag{5.27}$$

Figure 5.4 shows the waveforms of the $V_{UA}(t)$, $V_{LA}(t)$, I_{DCP}, $i_{ac}(t)$, $i_{UA}(t)$, $i_{LA}(t)$, $V_{CgP\_GU}(t)$, and $V_{CgP\_GL}(t)$ with the LC DC-link filters, respectively, when $L_{dc} = 0.015H$. As designed the peak to peak DC current ripple is reduced to 5% with respect to the nominal value of the DC current at rated power. This is a significant reduction in the DC current ripple in comparison to the TrMMC-DC-DC shown in figure 5.2 where the DC-link filters are not used.

5.2.3 MTrMMC-DC-DC semiconductor power Losses and Sizing Evaluation, and Simulation Results

The first aim of this subsection is to validate the methodology for determining the SM capacitance (equations 4.76-4.81) and arm inductance (equation4.71) for the modified trapezoidal operation of MMC-DC-DC described earlier. Secondly, it will

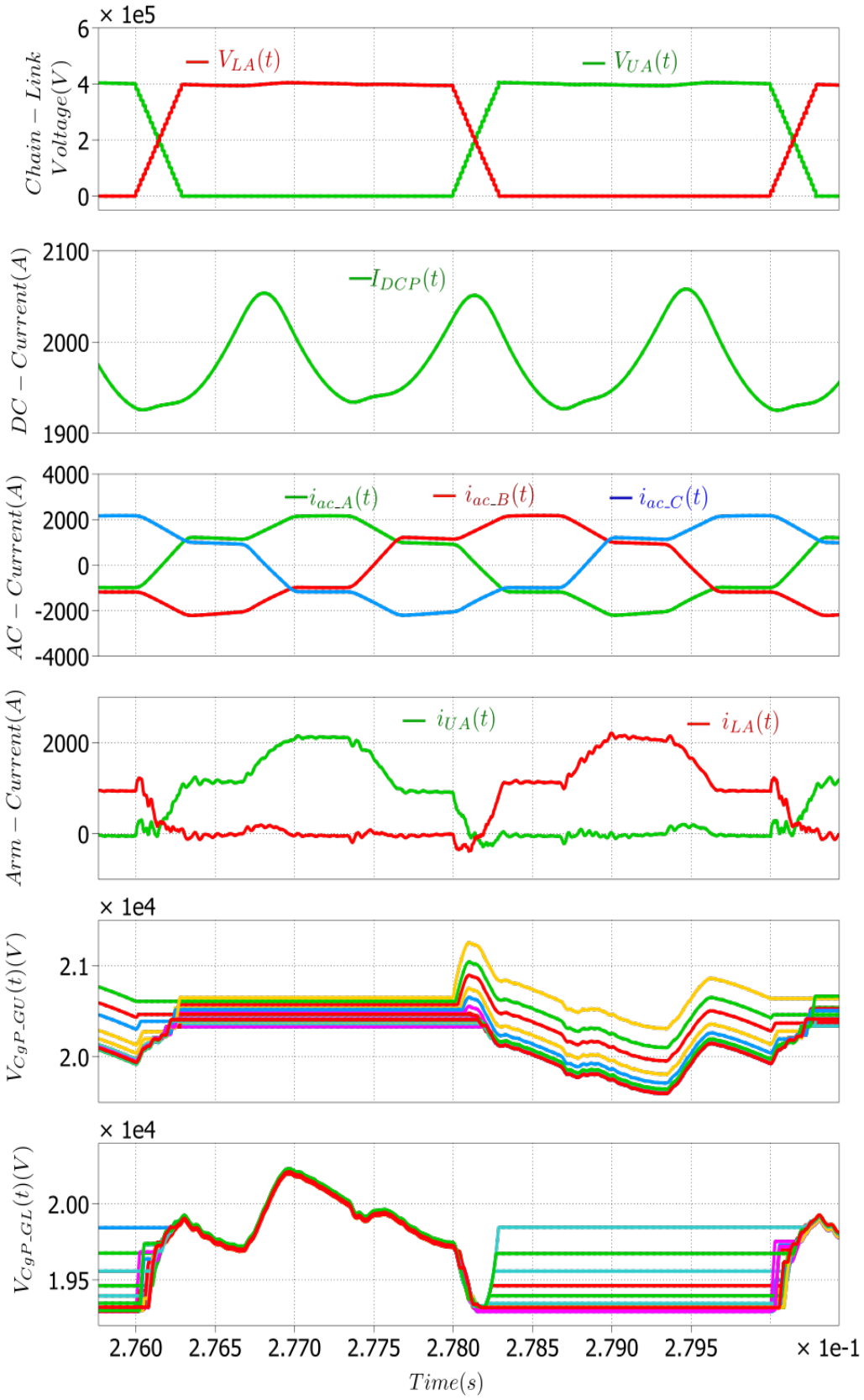


Figure 5.4: *TrMMC-DC-DC waveforms with DC-link LC filters*

validate the proposed SM capacitor voltage balancing method, power flow control and proposed energy control introduced in sections 4.3 and 4.4.2, respectively. For these purposes an HVDC conversion system with the specifications defined in table 5.1 has been modelled in PLECS software.

Figure 5.5 shows the waveforms of the phase A upper chain-link voltage, $V_{UA}(t)$, phase A lower chain-link voltage, $V_{LA}(t)$, primary DC link current, $I_{DCP}(t)$, three phase AC link currents, $i_{ac}(t)$, phase A upper arm current, $i_{UA}(t)$, phase A lower arm current, $i_{LA}(t)$, sum of upper SM capacitor voltages per group (level), $V_{CgP\_U}(t)$, and sum of lower SM capacitor voltages per group (level), $V_{CgP\_L}(t)$, respectively. It can be seen from the arm current that the arm conducts continuously. The very small ripple in the DC current at dominant frequencies f_o, $2f_o$ and $6f_o$ is due to the SM capacitor voltage sorting which introduces a small mismatch between the arm currents at those frequencies. As designed, the 10% peak to peak SM capacitor voltage ripple is achieved when they are inserted, and the balanced SM capacitor voltages of each group, $V_{CgP}(t)$, shows the effectiveness of the proposed balancing method where the SMs are sorted at the fundamental frequency. The SM capacitor voltage ripple introduces a second harmonic in the arm current but the second harmonic current is cancelled at both the AC and DC ports for both the primary and secondary sides of the MTrMMC-DC-DC.

Figure 5.6 shows the dominant harmonics of the I_{DCP}, i_{ac}, i_{UA}, i_{LA}. The second harmonic arm current amplitude will be reduced by reducing the peak to peak SM capacitor voltage ripple and vice versa.

The average semiconductor power losses of the MTrMMC-DC-DC as a percentage of rated power, T_{L_MTrMMC}, at sorting frequency, $f_{sort} = f_o$, was determined using the method described in equations 5.1-5.8 to be 0.92%.

Furthermore, the total device VA requirement as a percentage of rated power for the

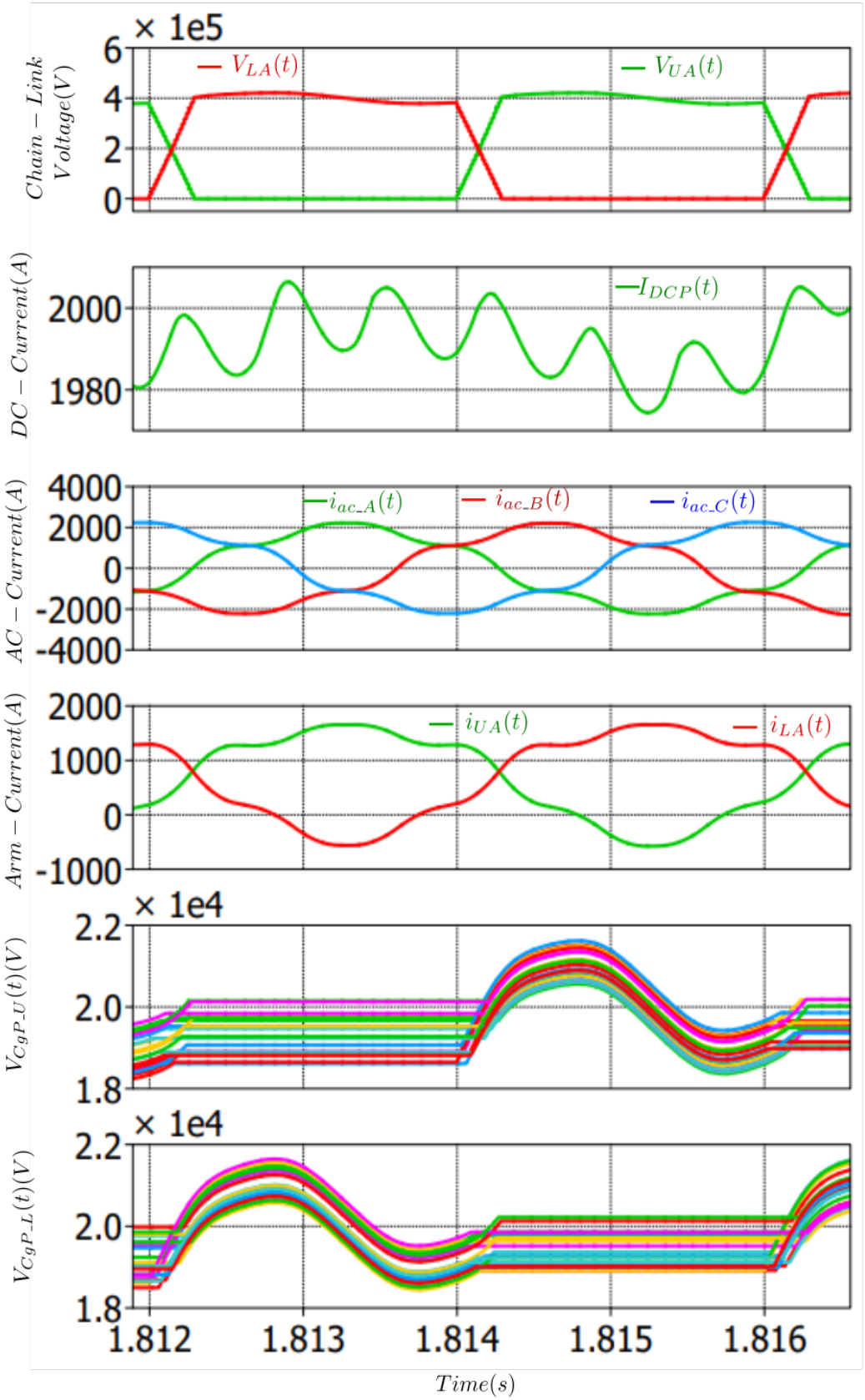


Figure 5.5: *MTrMMC-DC-DC waveforms*

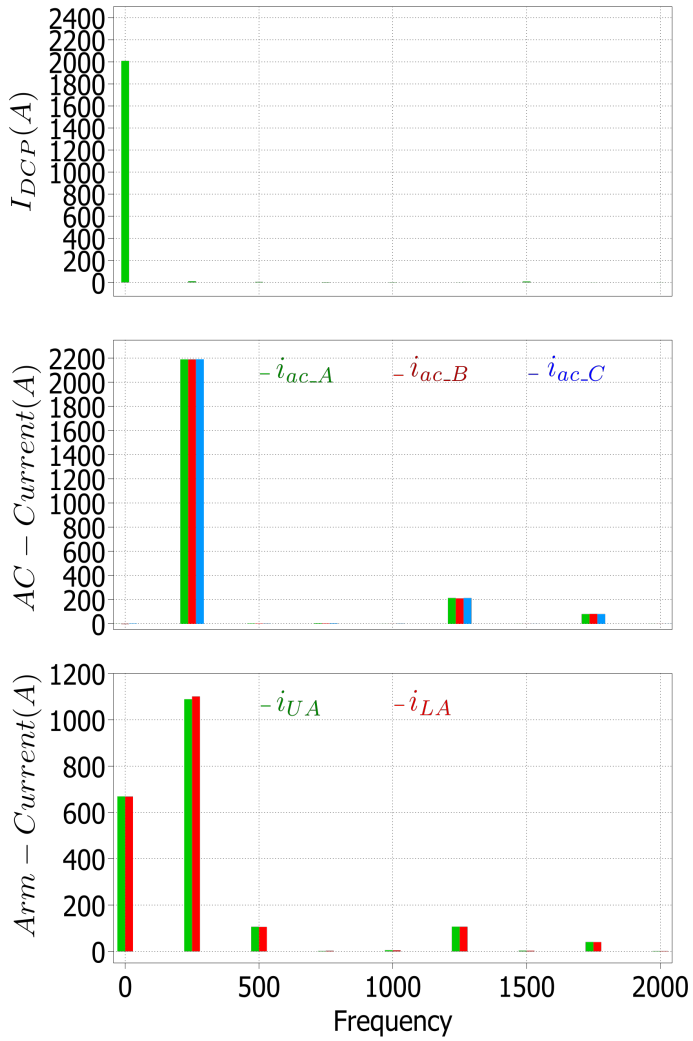


Figure 5.6: *FFT of DC, AC and arm currents in MTrMMC-DC-DC*

MTrMMC-DC-DC mode, $VA_{MTrMMC} = 10$, calculated using equation 5.28 where according to the operating conditions, the peak value of the chain-link current, $\hat{Ich}_{MTrMMC}$, can be varies as described in table 4.6.

$$VA_{MTrMMC} = \frac{12 N_{SM} V_{SM} \hat{Ich}_{MTrMMC}}{Pr} \tag{5.28}$$

Table 5.7 summaries the results that have been calculated for the MTRMMC-DC-DC using the analytical equations described earlier to achieve the HVDC conversion system defined in table 5.1.

It was explained in section 4.4.2 that the MTrMMC-DC-DC can operate by controlling only power flow when both DC voltages are fixed and SM capacitor voltage

Table 5.7: MTrMMC-DC-DC specifications and parameters

Parameters	Value
$L_p = L_s$	28.45mH
$C_{SMP} = C_{SMS}$	1.6 mF
$C_{gP} = C_{gS}$	0.16 mF
φ	0.13π
$\frac{fr}{fo}$	1.334
δ_{pp}	10%
$H_{cMTrMMC}$	9.78 ms
T_{L_MTrMMC} $(f_{sort} = f_o)$	0.92%
VA_{MTrMMC}	10

balancing is applied during smooth power transients. Figure 5.7 shows simulation results for $I_{DCP}(t)$, $i_{ac}(t)$, $i_{UA}(t)$, $i_{LA}(t)$, $V_{CgP\_U}(t)$, and $V_{CgP\_L}(t)$ of the MTrMMC-DC-DC when the power is controlled smoothly and slowly (more than 60 fundamental cycles) from 400MW to 800MW by applying the control structure which was introduced previously in figure 4.18. Consequently, a simple control structure is recognised for the MTrMMC-DC-DC configuration.

However, in the case of a step change in power demand high amplitude oscillations occur in $I_{DCP}(t)$, $i_{ac}(t)$, $i_{UA}(t)$, $i_{LA}(t)$, $V_{CgP\_U}(t)$, and $V_{CgP\_L}(t)$ as shown in figure 5.8. As shown the DC current reaches 150% of the demanded value and greater than 50 cycles are required to reach to steady state. The device current and arm current increased to 135% of the required value.

Therefore, energy and current control is essential in the case of a step change in power demand. It is also necessary in case when the DC voltage is not fixed or one of the DC ports is connected to a passive load. Figure 5.9 shows simulation results for $I_{DCP}(t)$, $i_{ac(t)}$, $i_{UA}(t)$, $i_{LA}(t)$, $V_{CgP\_U}(t)$, and $V_{CgP\_L}(t)$ of the MTrMMC-DC-DC for a step change in power demand with the control approach in section 4.4.2 implemented. As can be seen the overshoot and oscillations are almost eliminated and the energy and current reach steady state in a few cycles. This demonstrates the effectiveness of the proposed control schemes.

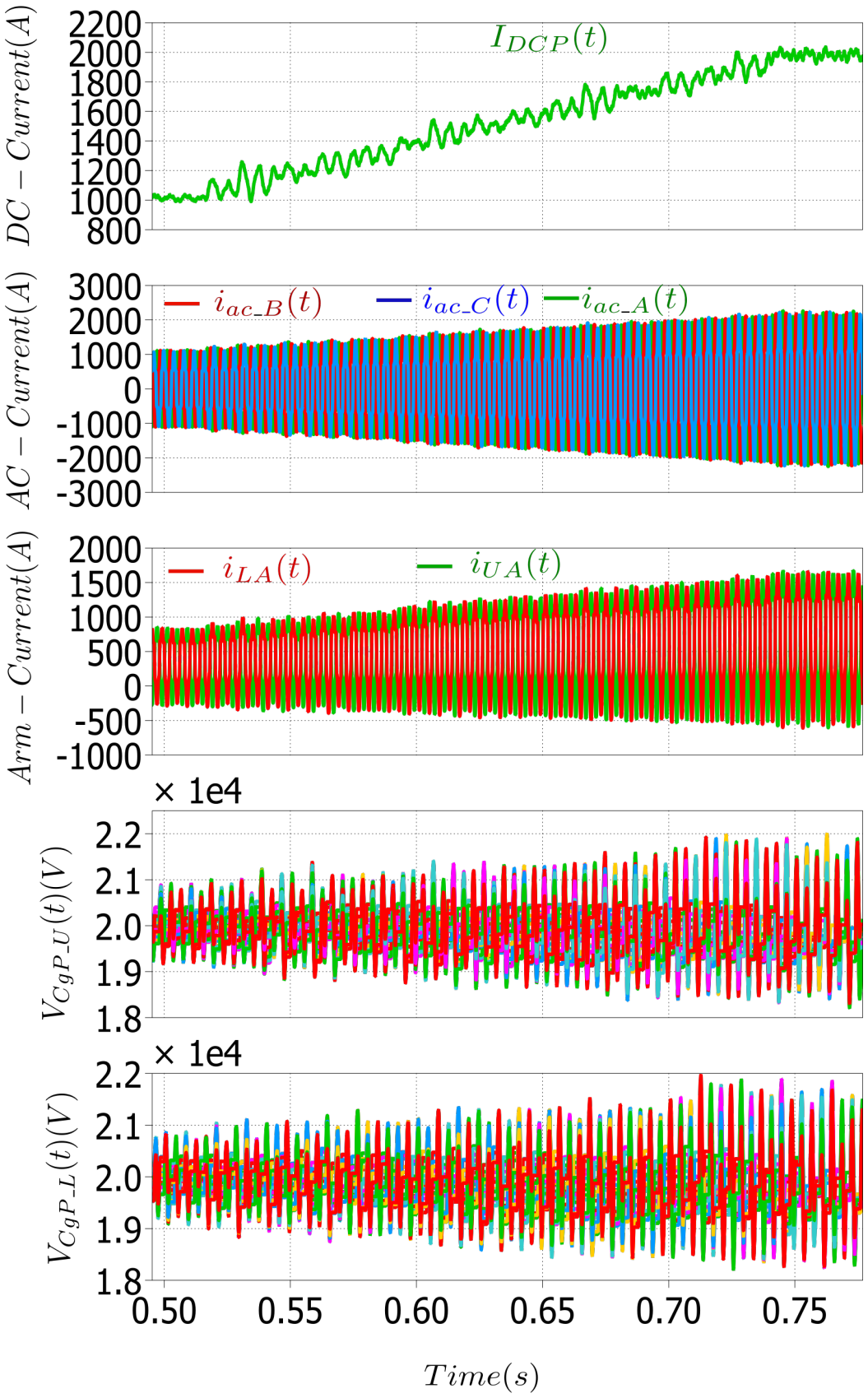


Figure 5.7: *MTrMMC-DC-DC waveforms with only slow power flow control*

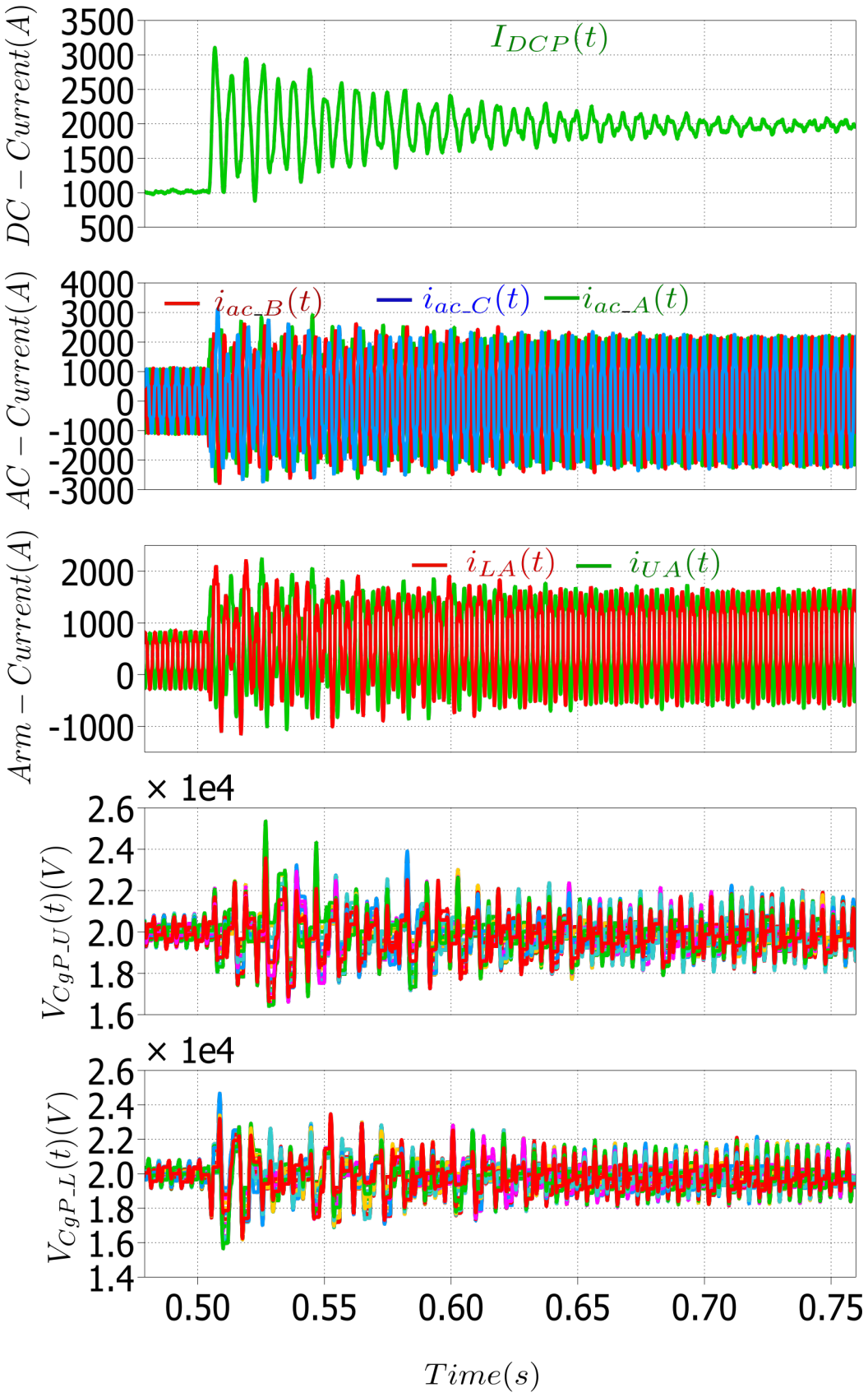


Figure 5.8: *MTrMMC-DC-DC waveforms with only fast power flow control*

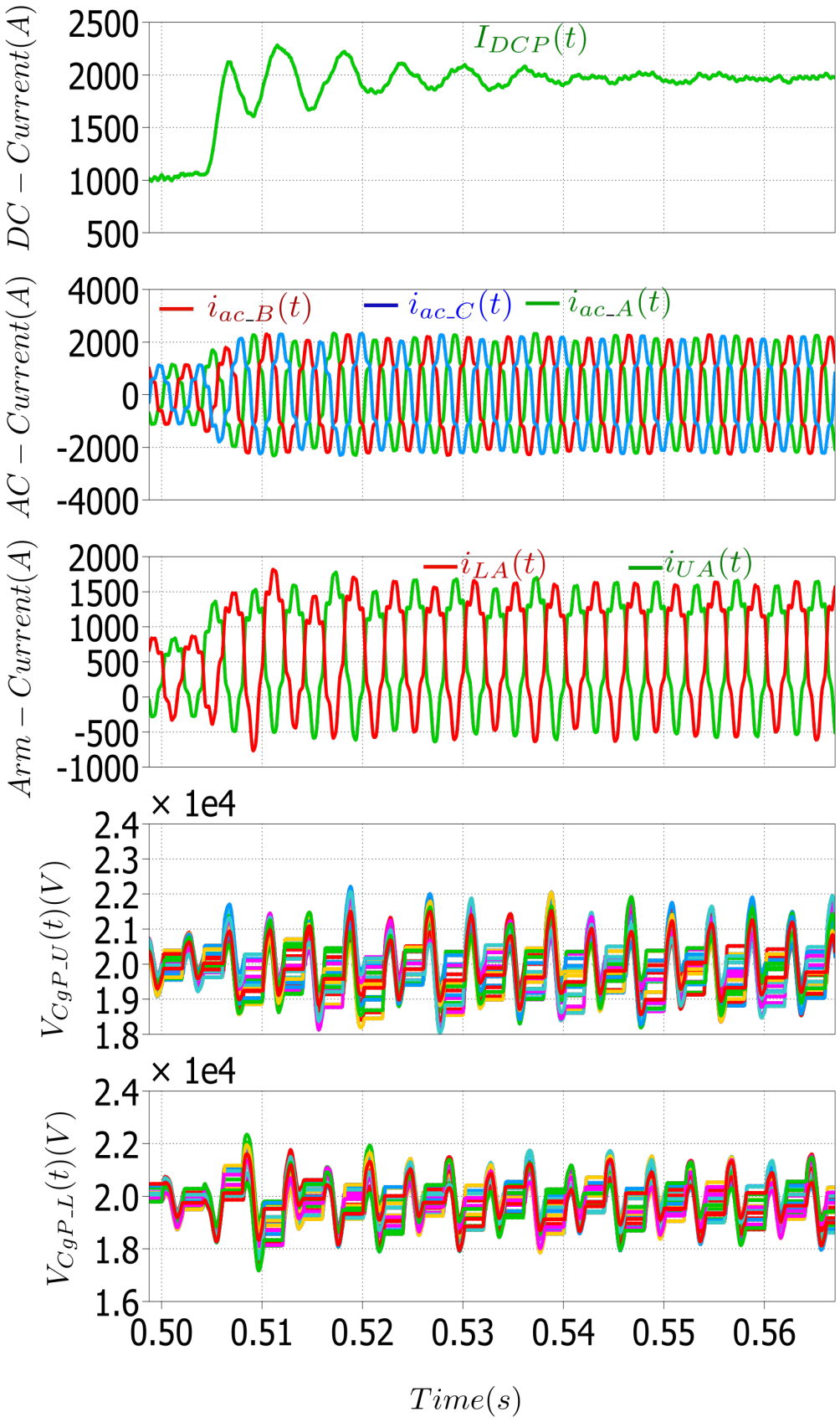


Figure 5.9: *MTrMMC-DC-DC waveforms with energy control, current and fast power flow control*

5.2.4 DC fault protection

DC fault protection in DC grids is a challenge protecting when HVDC-VSC converters are used. Hence, there have been a lot of proposed solutions to address the DC fault capabilities of HVDC-VSC converters [93–96]. Therefore, it is important to look at fault capabilities of the DC-DC converters if they are going to be installed in a DC grid.

Table 5.8 shows the DC cable parameters of a CIGRE test system [97] which have been used to demonstrate the performance of both the TrMMC-DC-DC and MTrMMC-DC-DC under a DC fault where L_m, C_m and R_m represent the DC cable inductance, capacitance and resistance, respectively. The fault location determines the DC cable impedance to fault and accordingly, it determines the value of the fault current that passes through the freewheeling diodes. The fault current become more destructive as the fault location become closer to the converter station. Therefore, a close fault location, $3km$, from the converter station was chosen as an example for simulation studies for both the TrMMC-DC-DC and MTrMMC-DC-DC.

Table 5.8: CIGRE DC cable parameters

Parameters	Value
L_m	2.111 mH/km
C_m	0.2104μF/km
R_m	9.5 mΩ/km

In both converters when a DC fault is detected, all SMs of both the primary and secondary chain-links will be gradually (during T_t) set into the idle state where both IGBT devices of the SMs will be turned off. Table 5.9 shows the DC link parameters of the TrMMC-DC-DC for different cases, no inductive filter, an inductive filter 1, L_{dcP1}, and an inductive filter 2, L_{dcP2}, when a DC fault is detected at the primary side of the TrMMC-DC-DC as shown in figure 5.10 where R_{dcP} represents the parasitic resistance of the filter, R_{tP} represents the total primary DC link resistance, L_{tP} represents the total primary DC link inductance, and C_{tP} represents the total primary

DC link capacitance.

Table 5.9: TrMMC-DC-DC DC link parameters under a DC fault condition

L_{tP}	R_{tP}	C_{tP}	Comment
L_m	R_m	C_m	no inductive filter
$L_m + L_{dcP1}$	$R_m + R_{dcP}$	$C_m + C_P$	inductive filter 1
$L_m + L_{dcP2}$	$R_m + R_{dcP}$	$C_m + C_P$	inductive filter 2

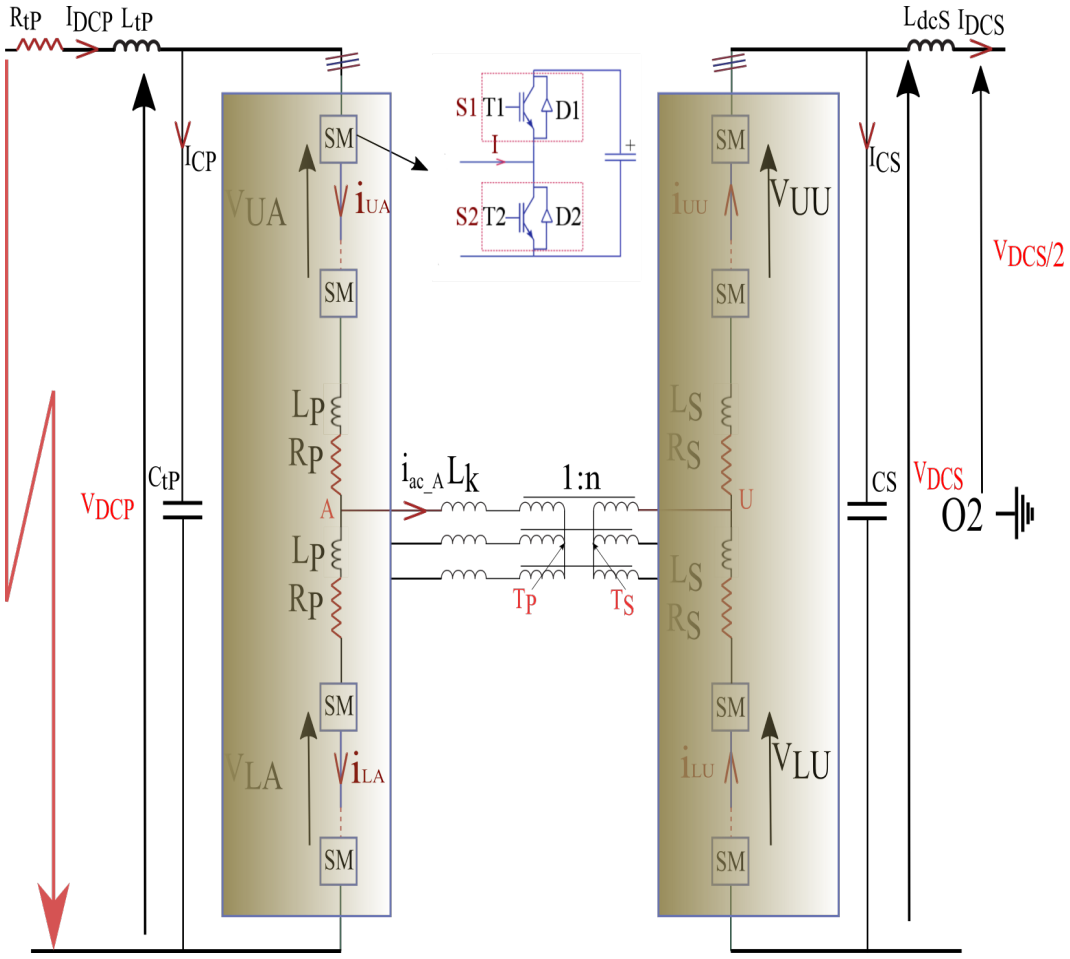


Figure 5.10: *TrMMC-DC-DC with a primary DC fault event*

Figure 5.11 shows the performance of the TrMMC-DC-DC with no inductive filter where V_{CP} is the voltage of the primary DC-link capacitor. As it can be seen V_{CP} discharges through the DC cables and I_{DCP} reaches the maximum value ($\approx$ 6.3 times higher than the rated DC current) at the instant where V_{CP} reaches zero. There is no current passing through the diode during the discharge period of the DC link capacitor however when V_{CP} reaches zero the stored energy in the L_{dcP} will force the current to pass through the freewheeling diodes of the faulty side accordingly the

SM diodes will experience high current ($\approx$ 3.5 times higher than the nominal maximum arm current). Figure 5.11 also shows that the AC link currents will smoothly reach zero and the SM capacitor voltages will ideally remain at the nominal value when the IGBTs are turned off.

In order to reduce the devices current stress during a DC fault, an inductive filter, $L_{dcP1} = 0.015H$, is designed according to equation 5.27 where the $L_{dcP1} = 0.015H$ and $C_P = 5.7\mu F$ resonates at $2.18f_o$. Figure 5.12 shows the performance of the TrMMC-DC-DC with the inductive filter 1 under a DC fault and it can be seen that the devices still experience high current stress ($\approx$ 2.25 times higher than the nominal maximum arm current). Hence, higher inductance has been chosen for the inductive filter 2, $L_{dcP2} = 0.06H$, which resonates with $C_P = 5.7\mu F$ at $1.09f_o$ and figure 5.13 shows the performance of the TrMMC-DC-DC with the inductive filter 2. As it can be noticed that the devices current stress has been reduced to the $\approx$ 1.28 times higher than the nominal maximum arm current. However, an overshoot in the DC link capacitor voltage, V_{CP}, can be observed with of $\approx$ 12.5% of the V_{CP} nominal value. As a result, if both the DC link inductance and the overshoot voltage in the DC link capacitor are considered for the energy storage requirement calculation, the TrMMC-DC-DC capacitance constant $H_{cTrMMC} = 6ms$ wiil be required with high sorting frequency, $f_{sort} = \frac{1}{2T_d} \approx 33.333kHz$, and per unit peak to peak SM capacitor voltage ripple $\delta_{pp} = 5\%$. Practically, achieving high sorting frequency with thousands of SMs could be challenging and to reduce the sorting frequency keeping the SM capacitor voltage ripple with an acceptable range, higher SM capacitance is required. Therefore, higher energy storage will be required however $H_{cMTrMMC} = 6ms$ has been used for the comparison purposes assuming the high sorting frequency is possible.

Figure 5.14 shows the MTrMMC-DC-DC converter under a DC fault at the primary side of the converter where L_{dcP} represents L_m, R_m and C_m have not been included in the figure to prevent confusion with the TrMMC-DC-DC topology however, they

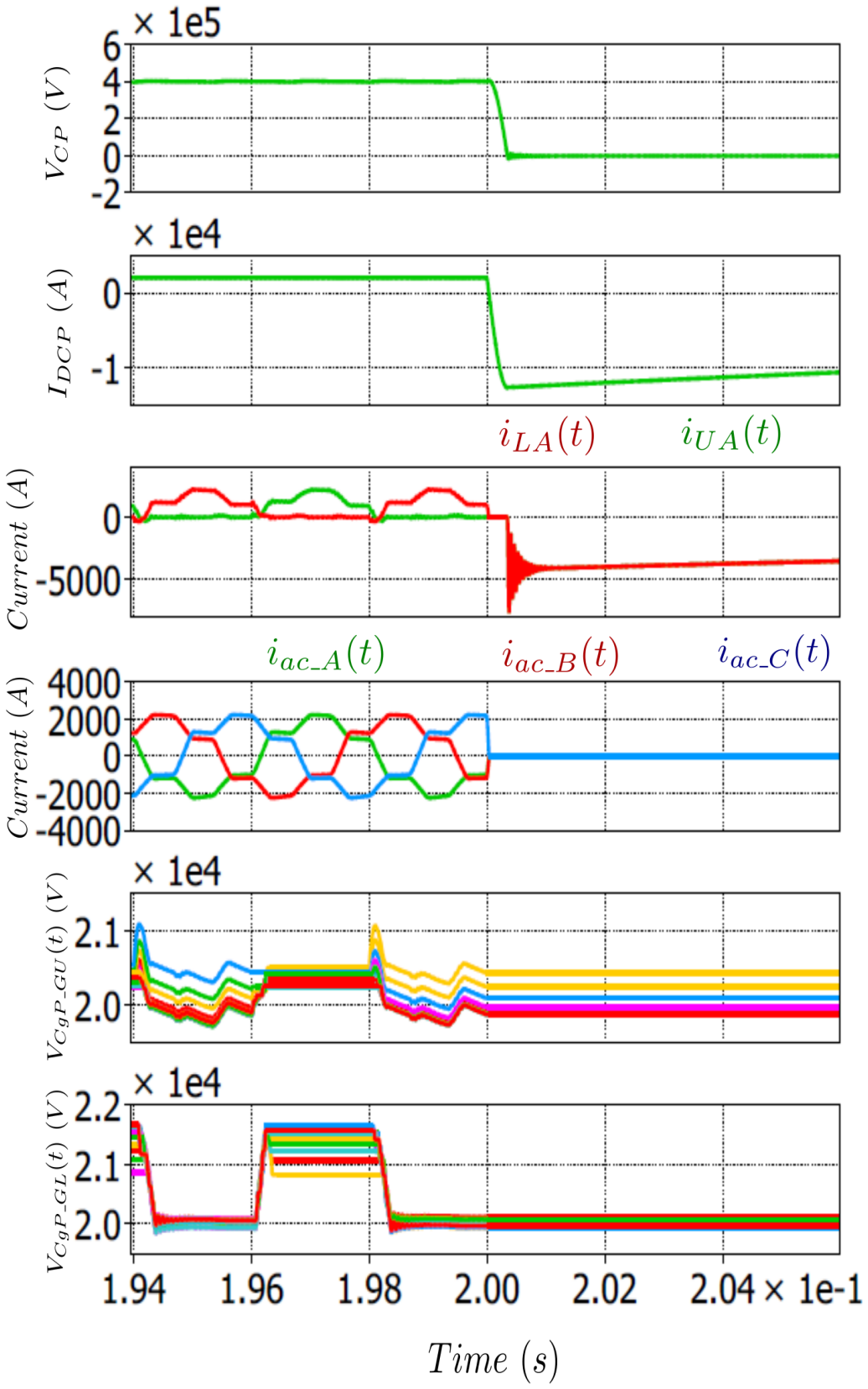


Figure 5.11: *TrMMC-DC-DC waveforms at DC fault events*

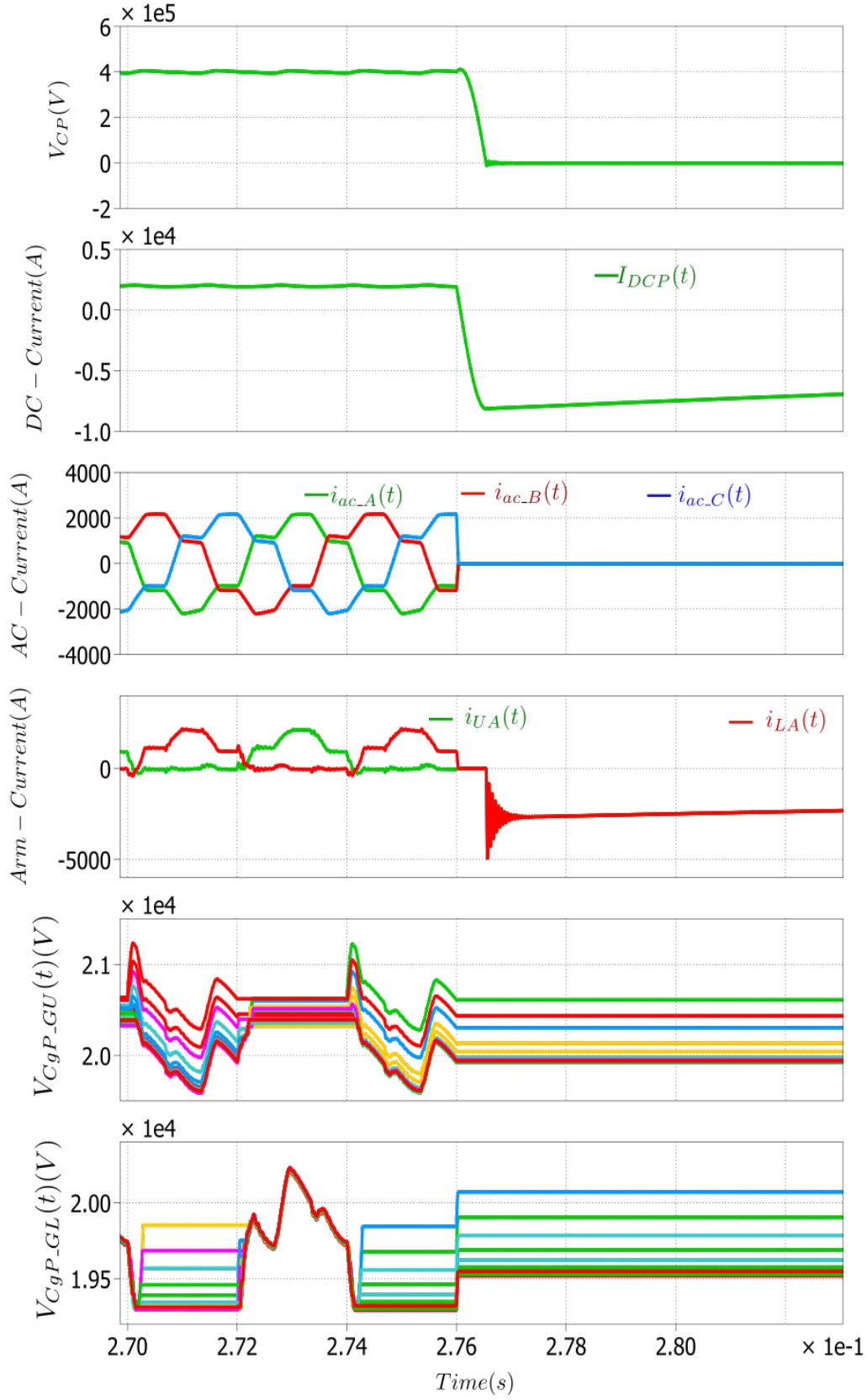


Figure 5.12: *TrMMC-DC-DC waveforms at DC fault events*

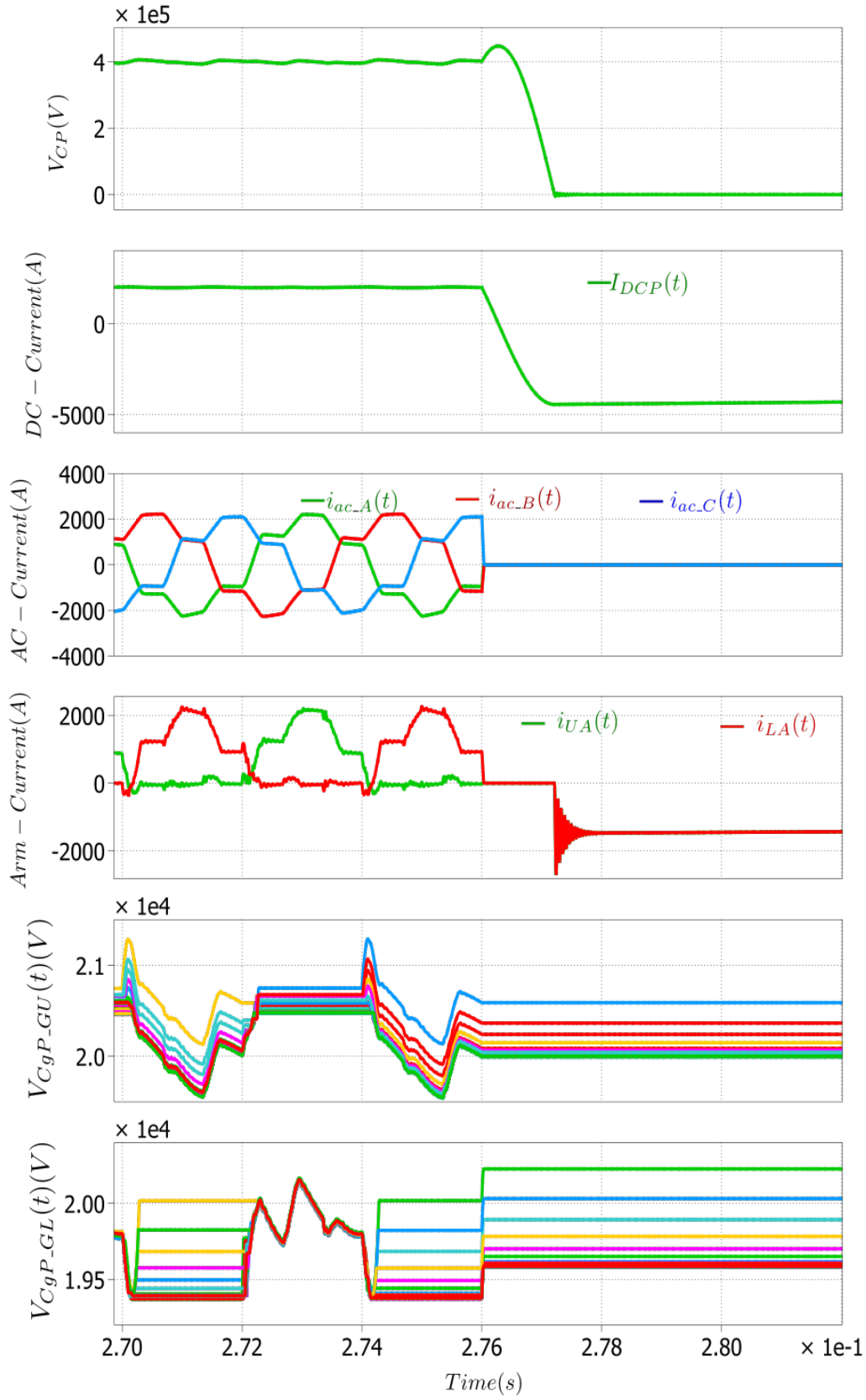


Figure 5.13: *TrMMC-DC-DC waveforms at DC fault events*

have been considered in the simulation circuit. The most important current and SM voltage waveforms of the MTrMMC-DC-DC when a DC fault occurs, 3*km*, away from the converter station are shown in figure 5.15. It can be observed that the arm current (current passes through the SMs diodes) smoothly falls to zero and the SM diodes will not experience any current stress. The reason behind this is mainly due to the absence of the DC link filters and the presence of the arm inductor which is big enough to prevent current inrush through the diodes. Figure 5.15 also shows that the AC link currents and phase A arm currents of the non-faulty side will smoothly fall to zero and the SM capacitor voltages will ideally remain at the nominal value when the IGBTs are turned off. The results show that the DC fault blocking capability of the MTrMMC-DC-DC is achieved with no additional device current stress and hence extra filtering is not required.

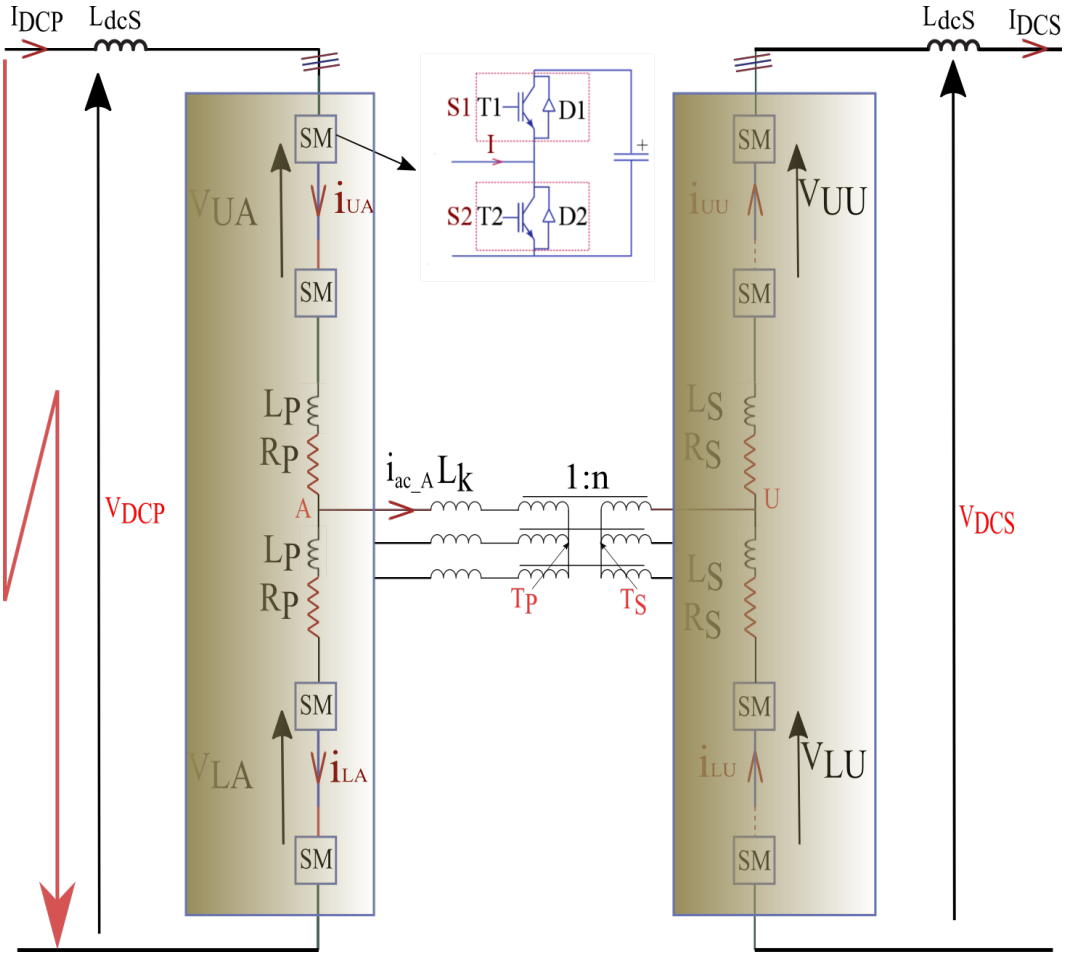


Figure 5.14: *MTrMMC-DC-DC with a primary DC fault event*

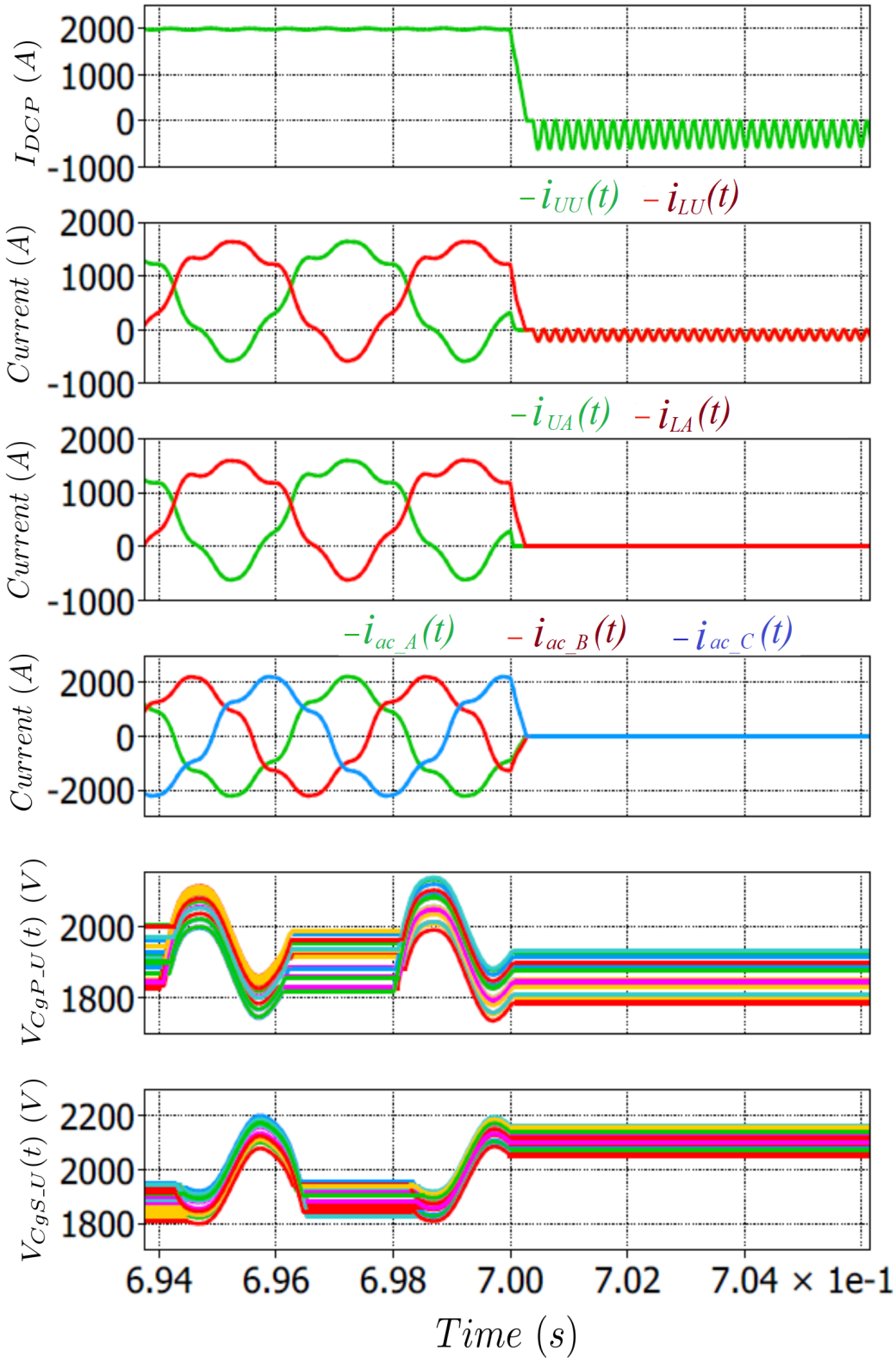


Figure 5.15: *MTrMMC-DC-DC waveforms at DC fault events*

5.2.5 Comparison

Table 5.10 shows the requirements and comparison between the three operating modes of the modular multilevel DC-DC converters, sinusoidal MMC-DC-DC, TrMMC-DC-DC and MTrMMC-DC-DC. It can be noticed that the MTrMMC-DC-DC provides the lowest semiconductor *VA* requirement (*VA* reflects the cost and area of the semiconductor) where approximately 19.5% $\downarrow$ and 23.3% $\downarrow$ reduction in the *VA* is achieved in comparison to the sinusoidal MMC-DC-DC and TrMMC-DC-DC operating modes, respectively. This is mainly due to the lowest device current ratings which results in because of the continuous conduction current in the arms and the trapezoidal waveform. The MTrMMC-DC-DC also provides the lower semiconductor losses where approximately 51.67% $\downarrow$ & 34.9% $\downarrow$ reduction in the semiconductor losses can be achieved in comparison to the sinusoidal MMC-DC-DC and TrMMC-DC-DC operating modes, respectively, and this is due to the low sorting frequency requirements, trapezoidal voltage and current wave-shaping. Consequently, the most simple cooling system will be required for the SM devices when MTrMMC-DC-DC is used. Additionally, due to the presence of the large arm inductor in the MTrMMC-DC-DC configuration, semiconductor devices will not experience any current stress during a DC fault event.

The TrMMC-DC-DC provides the lowest energy storage requirement, H_c, where considering high sorting frequency for a few thousands of the SMs is achievable, $f_{sorting} = 1/(2T_d) = 33.333kHz$, approximately 67.39% $\downarrow$ & 38.65% $\downarrow$ reduction in H_c can be achieved in comparison to the sinusoidal MMC-DC-DC and MTrMMC-DC-DC operating modes, respectively. Reducing the sorting frequency will reduce the control complexity and semiconductor losses however higher energy storage, H_c, will be required to keep the SM capacitor voltage ripple within the acceptable range. Poor device utilisation can be observed in the TrMMC-DC-DC since according to the power flow direction, one of the SM devices is used only during the transition period.

The main advantage of the sinusoidal MMC-DC-DC operating mode is the voltage level, $\frac{dv}{dt}$, which reflects the $\frac{dv}{dt}$ voltage stress across the transformer. However, the bulky energy storage requirements, semiconductor losses, semiconductor *VA* and cooling requirements are the drawbacks of the sinusoidal MMC-DC-DC configuration.

One of the main drawbacks of both the TrMMC-DC-DC and MTrMMC-DC-DC operating modes is the high voltage level, $\frac{dv}{dt}$, which prevents the converters from operating at high fundamental frequency.

Table 5.10: Comparison between the three operating modes, sinusoidal MMC-DC-DC, TrMMC-DC-DC, MTrMMC-DC-DC

Requirements & Parameters	MMC-DC-DC	TrMMC-DC-DC	MTrMMC-DC-DC	Comments
$f_{sorting}$	$10f_o$	$1/(2T_d)$ during T_t	f_o	MTrMMC-DC-DC ✓
$H_c(ms)$	18.4	6	9.78	TrMMC-DC-DC ✓
VA	12.42	13	10	MTrMMC-DC-DC ✓
$T_L\%$	1.91	1.42	0.92	MTrMMC-DC-DC ✓
dv	2kV	20kV	20kV	MMC-DC-DC ✓
N_L	1	10	10	MMC-DC-DC ✓
T_t	-	$0.15\pi - T_d$	$0.15\pi - T_d$	MMC-DC-DC ✓
Device current stress	✓✓	✓	✓✓✓	MTrMMC-DC-DC ✓
Device utilisation	✓✓✓	✓	✓✓✓	MTrMMC-DC-DC ✓& MMC-DC-DC ✓
Cooling requirements	✓	✓✓	✓✓✓	MTrMMC-DC-DC ✓

5.3 Summary

This chapter demonstrated a comprehensive comparison between the sinusoidal MMC-DC-DC, TrMMC-DC-DC and the MTrMMC-DC-DC configurations in terms of the semiconductor power losses, semiconductor *VA* requirement which reflects on the cost and area of semiconductor, energy storage requirements, transformer voltage stress, device current stress, device utilisation and cooling system requirements. It was shown that the TrMMC-DC-DC provides a lower energy storage requirement and the sinusoidal MMC-DC-DC provides a lowest voltage stress, $\frac{dv}{dt}$. However, the MTrMMC-DC-DC provides a better performance in other aspects,

low sorting frequency of the SM capacitor voltages which reduce the control complexity, semiconductor power losses, semiconductor *VA* requirement, device current stress, device utilisation and cooling requirements.

The proposed operating mode, MTrMMC-DC-DC, passive component theoretical design, the proposed balancing SM capacitor voltage and energy control were validated in PLECS software where an HVDC system with power of 800MW and 400kV for DC link voltages was built.

Growing number of SMs, up to a few thousands of SMs, by increasing the voltage rating of the HVDC system will increase the control complexity for all the configurations though the SMs in the MTrMMC-DC-DC operating mode are sorted at the fundamental frequency and this can be considered as the main disadvantages of these typologies. Another disadvantage is the limitations of increasing the fundamental frequency due to the potentially high semiconductor losses in the sinusoidal MMC-DC-DC mode, high $\frac{dv}{dt}$ stress across the transformer and the semiconductor losses in the TrMMC-DC-DC mode and high $\frac{dv}{dt}$ stress across the transformer in the MTrMMC-DC-DC mode.

Therefore, to overcome the high number of the SMs, low $\frac{dv}{dt}$ stress, high fundamental operating frequency and high power density, another topology will be proposed in the next chapter.

Chapter 6

Series Chain-Link Modular Multilevel DC-DC Converter: Topology, Analysis and Control

6.1 Introduction

The trapezoidal operating modes of the modular multilevel DC-DC converter namely, TrMMC-DC-DC and MTrMMC-DC-DC were explained and compared in chapters 4 and 5. The advantages of these modes, particularly MTrMMC-DC-DC, were shown in terms of the semiconductor power losses, energy storage requirement, device utilisation and semiconductor VA requirement. However, operating at a fundamental frequency higher than $250Hz$ to increase the transformer power density is challenging due to the potentially high transformer $\frac{dv}{dt}$ stress. Additionally, the need for a high number of SMs is one of the other main challenges of operating in the trapezoidal mode.

Moreover, in HVDC systems and high voltage DC networks such as, multi-terminal HVDC systems, the voltage levels are hundreds of kV and the power rating is up to a few GW. For all of the aforementioned modular multilevel topologies in the pre-

vious chapters, either one three phase transformer or one single phase transformer is required. Building a cooling system at a high voltage and high power rating can be challenging since the performance of the cooling system is an important factor for prevention of the lifetime reduction of a transformer. The cooling system also impacts the cost and the size of the transformer [98]. There are other reasons which can make building a transformer at a rating of hundreds of kV with a few of GW may not be practical particularly at medium and high operating frequency, however, they will not be discussed further since it is not the main aim of this work. In addition to the MMC based DC-DC converters, there are a number of non MMC based DC-DC converter structures in literature, for instance, the cascaded multi DAB converter was proposed in [71] for HVDC applications. However, it can be practically difficult to implement as a result of the non modularity of the structure and the requirement of a high number of elementary cells to reach the required high voltages. Each of these cells comprises a low voltage single phase transformer and either a full-bridge or half-bridge converter. Accordingly, the MMC structures are more preferable for HVDC applications.

In this chapter, a new modular multilevel DC-DC converter named series chain-link modular multilevel DC-DC converter (TrSCC-DC-DC) are proposed with three trapezoidal operating modes. This new topology provides a significant reduction in the number of SMs and a reasonable number of single phase transformers with a lower voltage and power rating can be used. Additionally, operating frequencies up to 1kHz are achievable with low $\frac{dv}{dt}$ voltage stress across the transformer by increasing the number of phases. Higher operating frequency will reduce the energy storage requirement, the size of the passive components of the resonant tank, transformers and SM capacitors. In addition to high operating frequency, further reduction in SM capacitor size will be achieved by trapezoidal wave-shaping.

It should be noted that the considerations for the design and analysis of the number of single phase transformers required for the TrSCC-DC-DC converter and the

three phase transformer required for MMC-DC-DC structure with different trapezoidal operating modes are beyond the scope of the work in this thesis.

The rest of this chapter introduces three possible TrSCC-DC-DC operating modes and provides a detailed analysis to indicate the optimum operating region in terms of energy storage requirement, power density, semiconductor power losses and device *VA* requirement. Finally, the required control loops to operate the TrSCC-DC-DC modes are discussed and designed.

6.2 Trapezoidal operation of the series chain-link DC-DC converter

The structure of the TrSCC-DC-DC is shown in figure 6.1 where a 4 phase version is illustrated with a fixed DC source on both sides of the converter. A 1:1 (n:turn ratio=1) single phase with a medium frequency transformer ($f_o \leq 1kHz$) is considered in the AC link for each phase. Each phase consists of two chain-links; a primary chain-link and a secondary chain-link, and each chain-link consists of a series connection of the half-bridge SMs. This series connection produces $\frac{1}{N_{phase}}$ (N_{phase} is the number of the phases) of the DC side voltage and an AC voltage. Considering each side of the converter, the sum of the AC chain-link voltages must be zero. Figure 6.2 shows the ideal chain-link voltage waveform where the transition time, T_t, is the time required to insert the SMs in each chain-link and dwell time, T_d, is the time between voltage level transitions. The peak voltage of the chain-link, $\hat{V_{ch}}$, can be expressed as equation 6.1 and the instantaneous primary and secondary chain-link current is given by equations 6.2 and 6.3, respectively, where i represents the phases from $1,...,N_{Phase}$, and ideally $I_{DCP} = \frac{P_{av}}{V_{DCP}}$ and $I_{DCS} = \frac{P_{av}}{V_{DCS}}$. In each phase, L_{kP} and L_{kS} represent the primary leakage inductance and secondary leakage inductance of the transformer in addition to the tank inductance, respectively. The primary and secondary blocking capacitors, C_{bP} and C_{bS}, will block the DC voltage of each

chain-link and, accordingly, the ideal transformer voltage will be as shown in figure 6.3 with only an AC component. The power flow is enabled by introducing a phase shift between the primary and secondary chain-link voltages. The chain-link current comprises the DC current and the AC current which is circulating between the primary and secondary chain-links in each phase. The proposed TrSCC-DC-DC converter is derived from [19] which has been proposed for AC/DC conversion in HVDC application. In [19] the AC link tank comprises passive components, inductors and capacitors, and a full-bridge based chain-link in order to have full control of the power factor. However, in the TrSCC-DC-DC, the control of the reactive power is not required and therefore, the full-bridge chain-link is eliminated.

$$\hat{V_{Ch}} = \frac{2V_{DC}}{N_{Phase}} \tag{6.1}$$

$$I_{ChP\_i}(t) = I_{DCP} - i_{ac\_i}(t) \tag{6.2}$$

$$I_{ChS\_i}(t) = I_{DCS} - i_{ac\_i}(t) \tag{6.3}$$

The number of SMs in one chain-link, N_{SMx_i}, and the total number of required SMs, N_{SM_T}, in the SCC-DC-DC converter can be calculated as equation 6.4 where V_{SM} represents the nominal voltage of the SM and x represents the primary and/or secondary side of the converter. In comparison to the sinusoidal MMC-DC-DC, TrMMC-DC-DC, MTrMMC-DC-DC converters, the TrSCC-DC-DC requires only 33% of the SMs which are required for the other addressed MMC-DC-DC configurations. The total number of SMs in the MMC-DC-DC operating modes can be calculated as shown in equation 6.5. Furthermore, the number of the phases in the TrSCC-DC-DC can be increased as required and by increasing the number of the phases, the number of single transformer increases whilst the total number of SMs in the TrSCC-DC-DC will remain the same, keeping V_{SM} fixed. Additionally, increasing the number of phases will lead to a reduction in the total chain-link voltage ripple which reflects the reduction in the DC current ripple- further explanation is

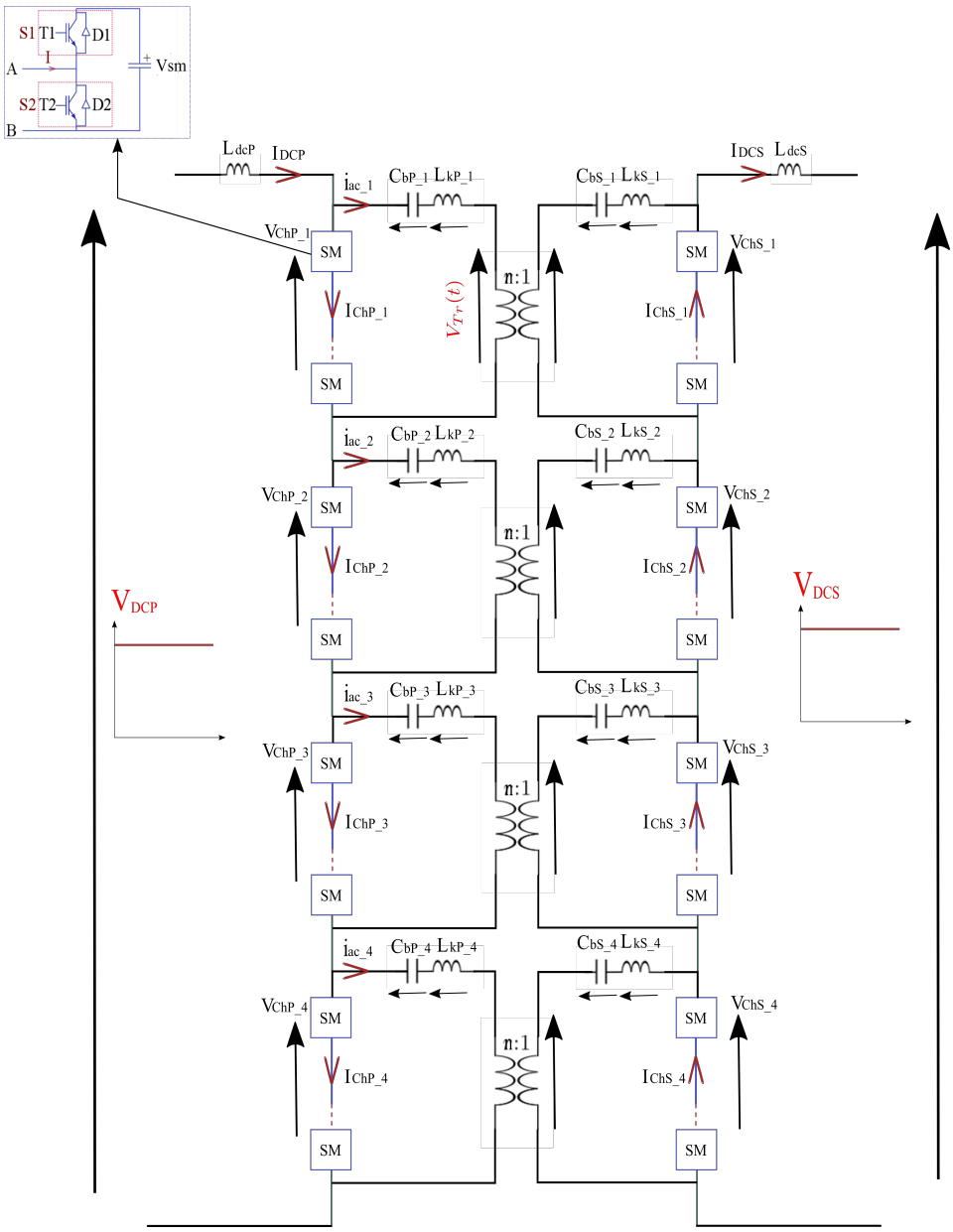


Figure 6.1: *4 phase TrSCC-DC-DC converter*

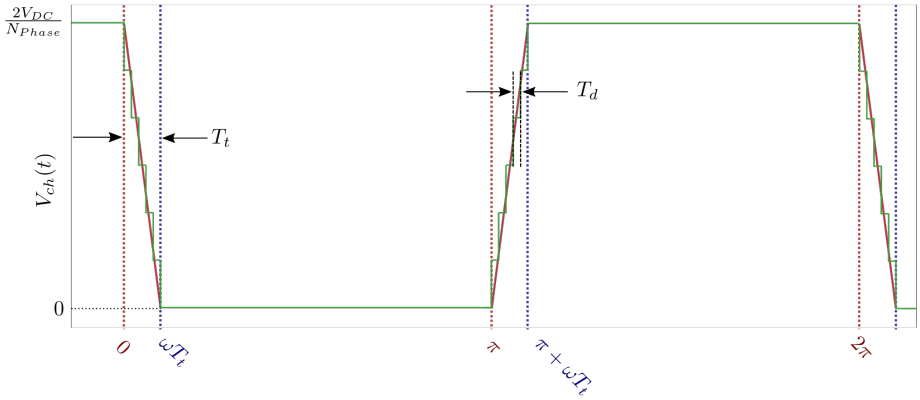


Figure 6.2: *Ideal chain-link voltage of TrSCC-DC-DC*

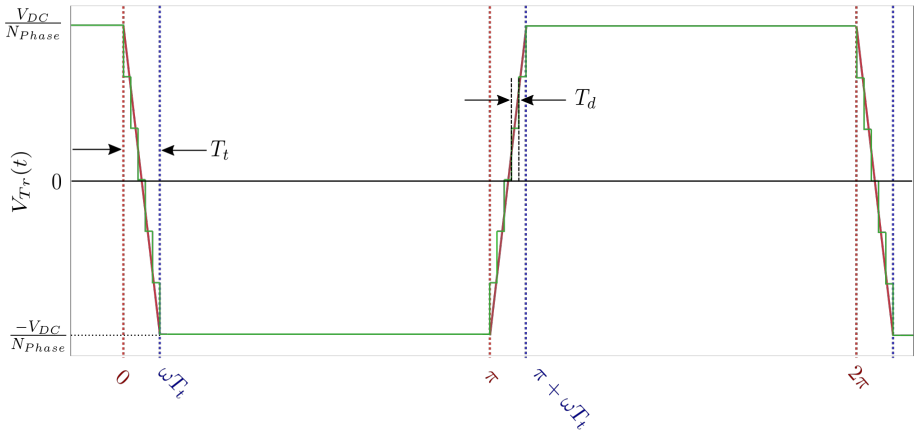


Figure 6.3: *Ideal transformer voltage of TrSCC-DC-DC*

given in this section. Accordingly, building high voltage DC-DC converters with several single transformers can overcome the challenge of building one three phase high voltage transformer and may help to overcome the cooling challenging due to the lower voltage rating and power transformer rating.

$$N_{SMx\_i} = \frac{2 * V_{DCx}}{Nphase * V_{SMx}}$$

$$\begin{aligned} N_{SM\_T} &= Nphase * (\frac{2 * V_{DCP}}{Nphase * V_{SMP}} + \frac{2 * V_{DCS}}{Nphase * V_{SMS}}) \\ &= \frac{2 * V_{DCP}}{V_{SMP}} + \frac{2 * V_{DCS}}{V_{SMS}} \end{aligned} \tag{6.4}$$

$$N_{SM\_MMC\_T} = 6 * (\frac{V_{DCP}}{V_{SMP}} + \frac{V_{DCS}}{V_{SMS}}) \tag{6.5}$$

Figure 6.4 shows the primary chain-link voltages of three different operating modes of the TrSCC-DC-DC. In mode A, the phases have been divided into two groups and the chain-link voltage of first group is in anti-phase with respect to second group. In mode B, each group comprises a pair of phases with 180° phase difference between their chain-link voltages. The phase difference between the groups in mode B is $T_{ph} = \frac{T}{N_{Phase}}$. The modes A and B are applicable only to an even number of phases. Considering ideal operation, there is theoretically no difference between

mode A and mode B at converter level. However, when the SM voltage ripple is considered, the ripple frequency of the total chain-link voltage in mode A is $2f_o$ and the ripple frequency of the total chain-link voltage in mode B is $N_{Phase}f_o$. Mode C is applicable to both an even and odd number of phases (when $N_{Phase} > 2$) and then the transition period and the phase difference between the phases is given by $T_t = T_{ph} = \frac{T}{N_{Phase}}$. The ripple frequency of the total chain-link voltage in mode C is the same as mode B.

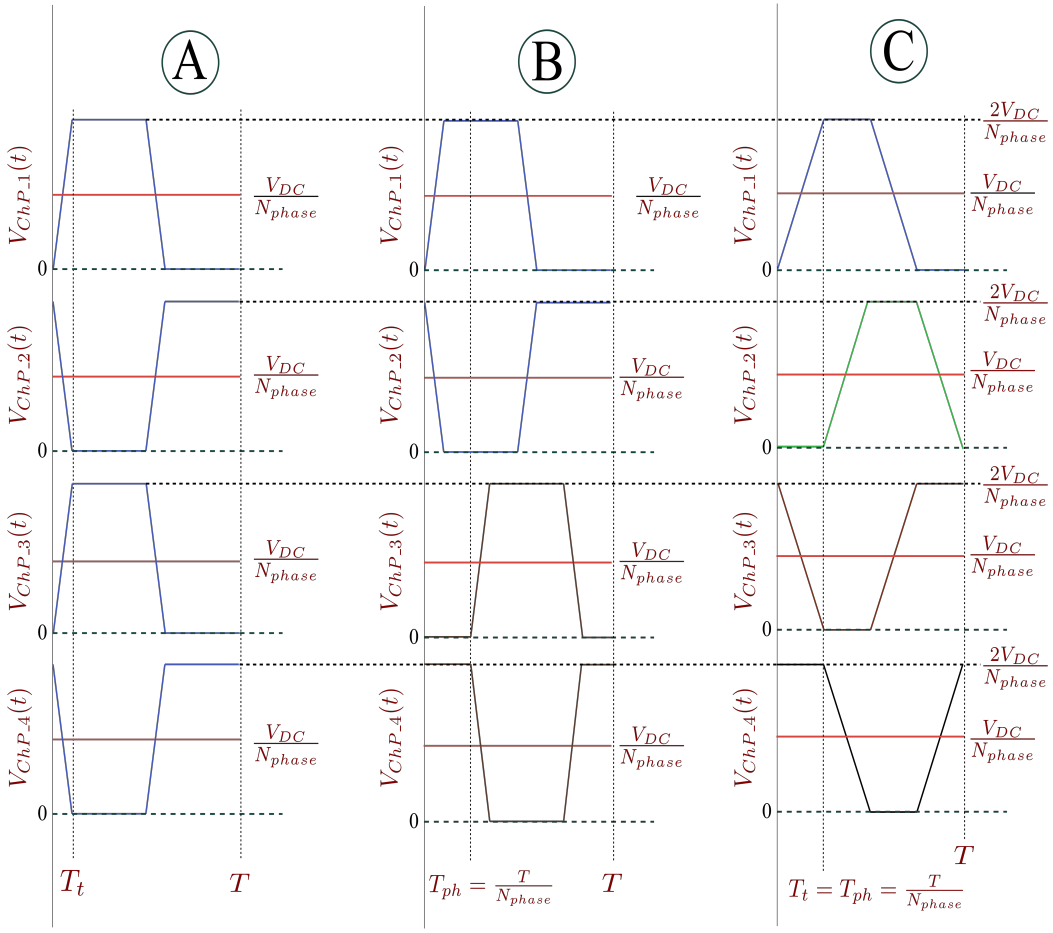


Figure 6.4: *4 phase TrSCC-DC-DC converter operating modes*

The transition period, T_t, in modes A and B is independent of N_{Phase} and is chosen based on the optimum operating region in terms of energy storage requirement, semiconductor power losses, voltage stress across the transformer ($\frac{dv}{dt}$ per chain-link voltage level), and the device *VA* requirement. However, the transition period, T_t, in mode C is dependent on the number of phases, $T_t = \frac{T}{N_{Phase}}$. The impact of

N_{Phase} and T_t on the optimum operating region will be analysed and clarified in the following sections.

6.3 Converter modelling

6.3.1 DC side equivalent model

The DC circuit of the primary and secondary sides of the TrSCC-DC-DC converter can be represented as shown in figure 6.5 assuming ideal chain-link voltage waveforms where R_{dc} and L_{dc} represents the parasitic resistance and parasitic inductance of the DC loop, respectively. The AC components in the chain-link voltages cancel due to the phase shift and do not appear on the DC side. As a result the DC equivalent circuit can be represented as shown in figure 6.6.

6.3.2 Per phase AC side equivalent model

The per-phase AC circuit of the TrSCC-DC-DC converter can be represented as shown in figure 6.7 assuming ideal chain-link voltage waveforms. Accordingly, the per-phase AC equivalent circuit can be represented as shown in figure 6.8 assuming unity transformer turns ratio, $n = 1$, where C_{b_i} and L_{k_i} are obtained from equations 6.6 and 6.7, respectively.

$$C_{b\_i} = \frac{C_{bP\_i} C_{bS\_i}}{C_{bP\_i} + C_{bS\_i}} \tag{6.6}$$

$$L_{k\_i} = L_{kP\_i} + L_{kS\_i} \tag{6.7}$$

In order to evaluate the tank energy, semiconductor power losses and the semiconductor *VA* requirement which affects the area and the cost of the devices, analytical expressions for the tank voltage, $v_T(t)$, tank current, $i_{ac}(t)$, and equivalent DC blocking capacitor voltage, $v_{Cb}(t)$, are required. It should be noted that the tank voltage, $v_T(t)$, and equivalent DC blocking capacitor voltage, $v_{Cb}(t)$, comprise only

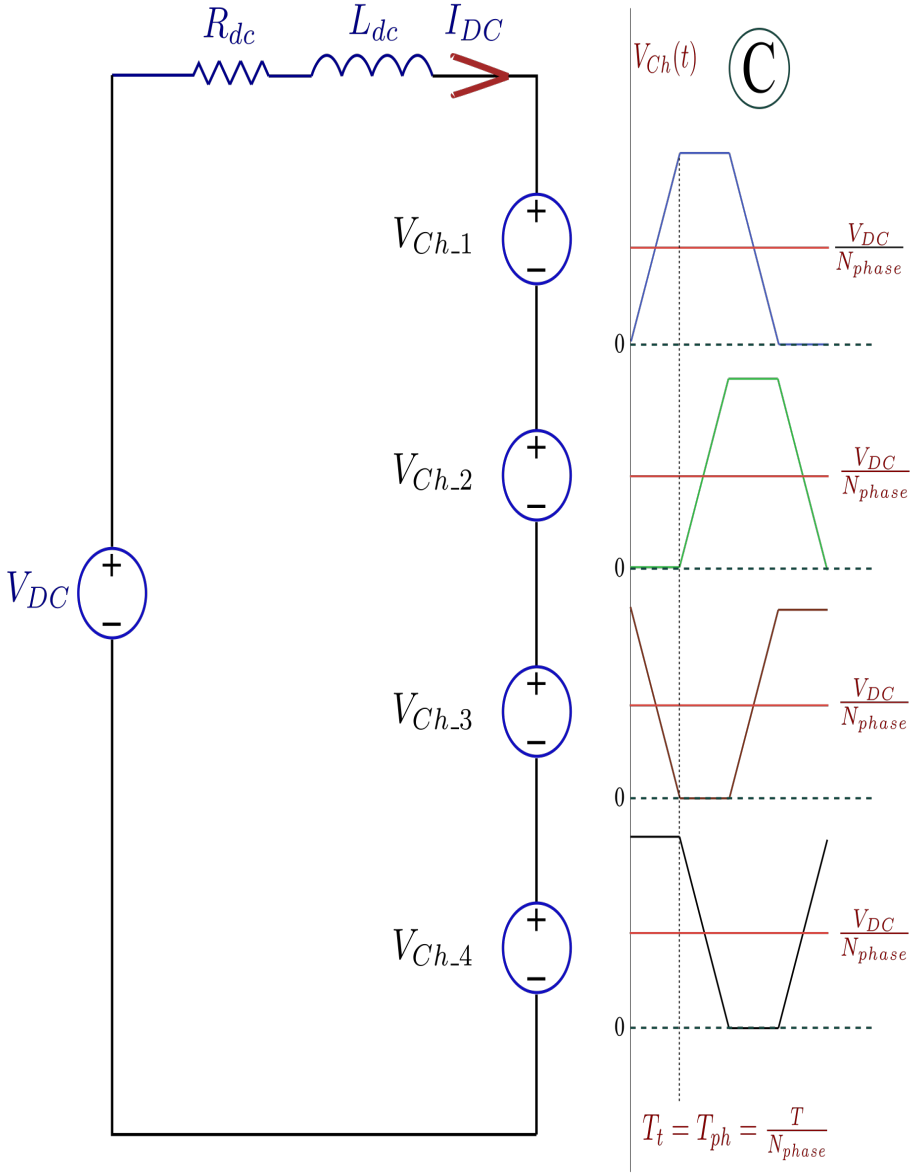


Figure 6.5: *DC equivalent circuit of TrSCC-DC-DC*

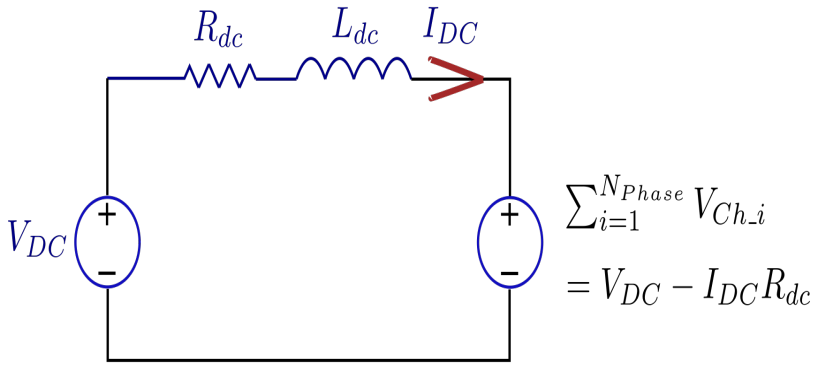


Figure 6.6: *DC circuit of TrSCC-DC-DC*

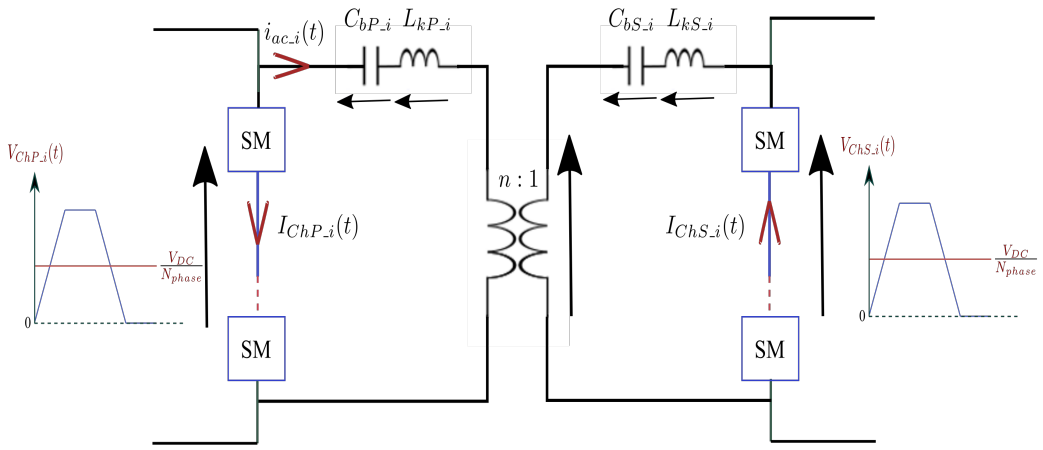


Figure 6.7: *Per-phase AC circuit of TrSCC-DC-DC*

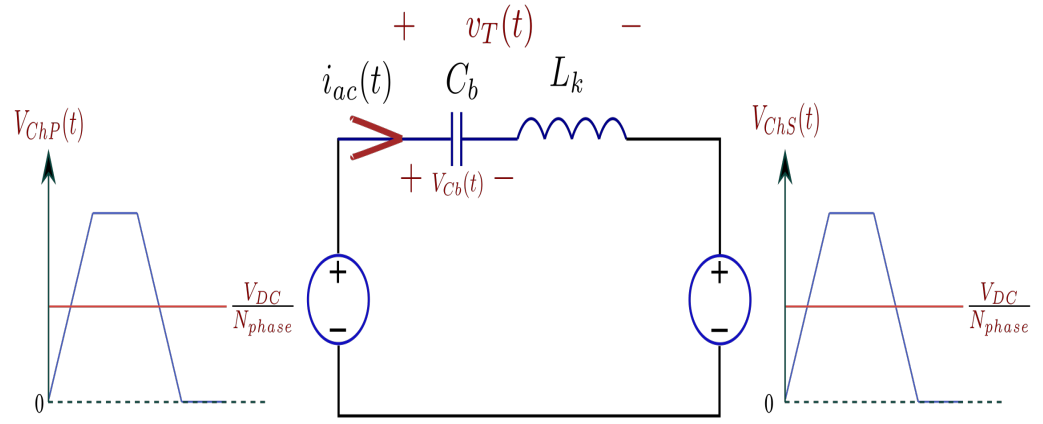


Figure 6.8: *Per-phase AC equivalent circuit of TrSCC-DC-DC*

the AC part of the voltage in the ideal circuit shown in figure 6.8. However, in the actual circuit shown in figure 6.1, the blocking capacitors, C_{bP_i} and C_{bS_i}, have to support $\frac{V_{DCP}}{N_{phase}}$ and $\frac{V_{DCS}}{N_{phase}}$, respectively, in addition to half of the AC voltage of $v\hat{_{Cb}}$. Considering the per phase equivalent circuit shown in figure 6.8, power flow is enabled by introducing a phase shift, T_{sh}, between the primary and secondary chain-link voltages within the phase. According to the phase shift introduced, three different tank voltages can be produced as shown in figure 6.9. The phase shift between the chain-link voltages is $T_{sh} \leq \frac{T}{2} - T_t$ for the cases X and Y. The time intervals t_1, t_2 and t_3 can be summarised as equation 6.8.

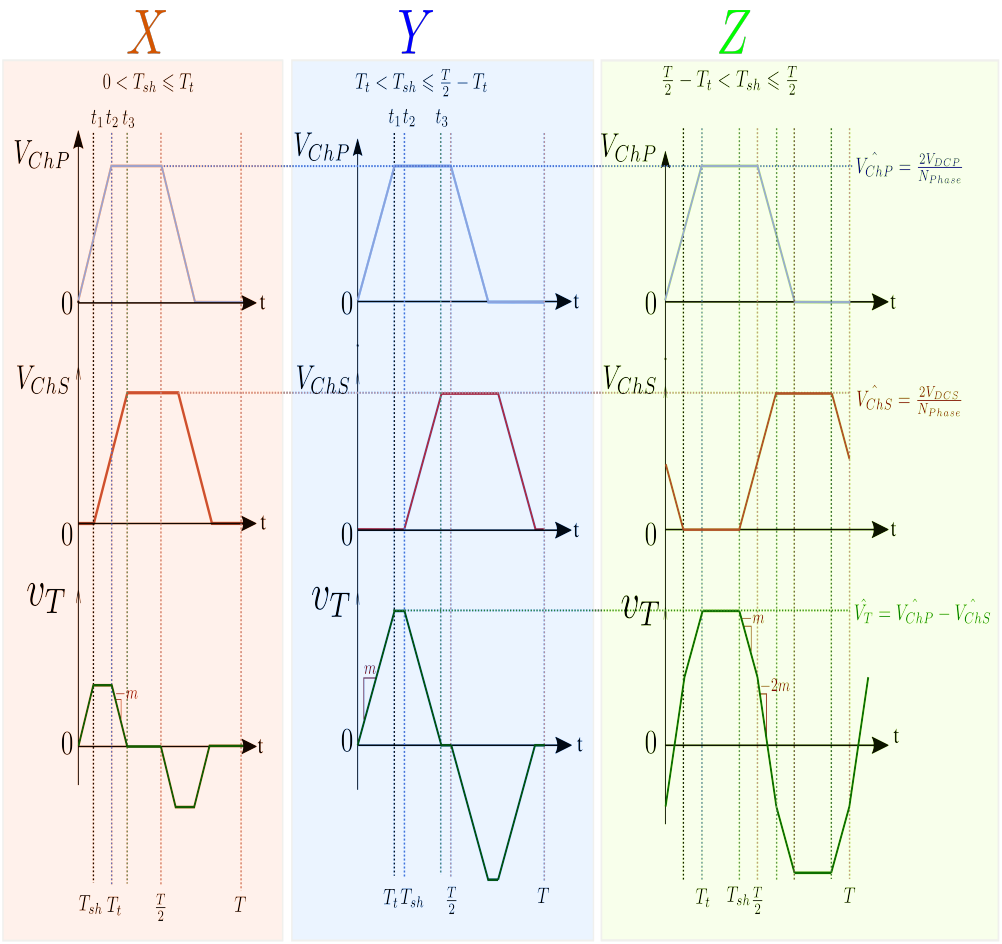


Figure 6.9: *Possible ideal tank voltage waveform, $v_T(t)$,*

$$t_i = \begin{cases} t_1 = \begin{cases} T_{sh} \text{ if } T_{sh} < T_t \\ T_t \text{ if } T_{sh} > T_t \end{cases} \\ t_2 = \begin{cases} T_t \text{ if } T_{sh} < T_t \\ T_{sh} \text{ if } T_{sh} > T_t \end{cases} \\ t_3 = t_1 + t_2 \end{cases} \tag{6.8}$$

The voltage of the tank, $v_T(t)$, for both cases X and Y, is generalised as shown in figure A.1-a where the phase shift between the chain-link voltages is $T_{sh} \leq \frac{T}{2} - T_t$. Calculation of the resonant tank current, $i_{ac}(t)$, and the equivalent DC blocking capacitor voltage, $v_{Cb}(t)$, are based on a Laplace analysis.

The detail of the calculations can be seen in section A.1 in the appendix and the final expressions for the $i_{ac}(t)$ and $v_{Cb}(t)$ for the cases X and Y are shown as equation 6.9 and equation 6.10, respectively, where the factors f_a, f_b, f_c, f_d, f_e, and f_f can be seen in the same section, A.1, in the appendix.

$$\begin{aligned} i_{ac}(t) = mC_b\Big\{&(1-\cos(\omega_{r1}t)) - (1-\cos(\omega_{r1}(t-t_1))) - (1-\cos(\omega_{r1}(t-t_2))) \\ &+ (1-\cos(\omega_{r1}(t-t_3)))\Big\} - \frac{(1-f_c)f_d + f_f f_a}{(1-f_c)(1-f_e) - f_b f_f}\omega_{r1}C_b\sin(\omega_{r1}t) \\ &+ \Big(\frac{(1-f_e)f_a + f_b f_d}{(1-f_c)(1-f_e) - f_b f_f}\Big)\cos(\omega_{r1}t) \end{aligned} \tag{6.9}$$

$$\begin{aligned} v_{cb}(t) = m\Big\{&\Big(t - \frac{1}{\omega_{r1}}\sin(\omega_{r1}t)\Big) - \Big((t-t_1) - \frac{1}{\omega_{r1}}\sin(\omega_{r1}(t-t_1))\Big) \\ &- \Big((t-t_2) - \frac{1}{\omega_{r1}}\sin(\omega_{r1}(t-t_2))\Big) + \Big((t-t_3) - \frac{1}{\omega_{r1}}\sin(\omega_{r1}(t-t_3))\Big)\Big\} \\ &+ \Big(\frac{(1-f_c)f_d + f_f f_a}{(1-f_c)(1-f_e) - f_b f_f}\Big)\cos(\omega_{r1}t) \\ &+ \omega_{r1}L_k\Big(\frac{(1-f_e)f_a + f_b f_d}{(1-f_c)(1-f_e) - f_b f_f}\Big)\sin(\omega_{r1}t) \end{aligned} \tag{6.10}$$

Figure 6.10 shows the tank voltage, $v_T(t)$, for the half of the period for the case Z where the phase shift is $\frac{T}{2} - T_t < T_{sh} \leq \frac{T}{2}$. The time intervals t_1, t_2, t_3 and t_4 can be summarised as in equation 6.11.

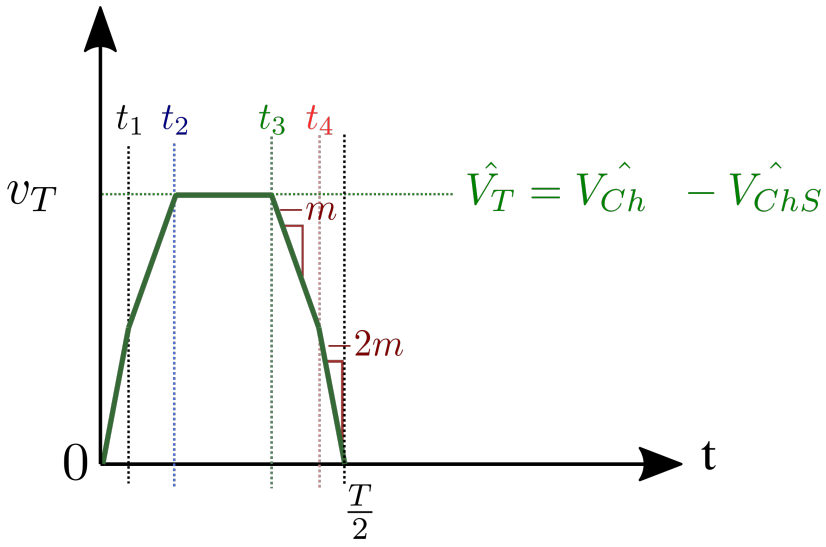


Figure 6.10: *Tank voltage of case Z*

$$t_i = \begin{cases} t_1 = \frac{-\frac{T}{2}+T_t+T_{sh}}{2} \\ t_2 = T_t - t_1 \\ t_3 = \frac{T}{2} - t_2 \\ t_4 = \frac{T}{2} - t_1 \end{cases} \tag{6.11}$$

The detail of the calculations can be seen in section A.2 in the appendix and the final expressions for the $i_{ac}(t)$ and $v_{Cb}(t)$ for the case Z are shown as equation 6.12 and equation 6.13, respectively, where the factors f_a, f_b, f_c, f_d, f_e, f_f, f_g, and f_p can be seen in the same section, A.2, in the appendix.

$$\begin{aligned} i_{ac}(t) = mC_b\Big\{ & 2(1-\cos(\omega_{r1}t)) - (1-\cos(\omega_{r1}(t-t_1))) - (1-\cos(\omega_{r1}(t-t_2))) \\ & - (1-\cos(\omega_{r1}(t-t_3))) - (1-\cos(\omega_{r1}(t-t_4)))\Big\} \\ & - (\frac{(1-f_c)f_p + f_f f_g}{(1-f_c)(1-f_e) - f_b f_f})\omega_{r1}C_b\sin(\omega_{r1}t) \\ & + (\frac{(1-f_e)f_g + f_b f_p}{(1-f_c)(1-f_e) - f_b f_f})\cos(\omega_{r1}t) \end{aligned} \tag{6.12}$$

$$\begin{aligned} v_{Cb}(t) = m\big\{ & (2t - \frac{1}{\omega_{r1}}\sin(\omega_{r1}t)) - ((t-t_1) - \frac{1}{\omega_{r1}}\sin(\omega_{r1}(t-t_1))) \\ & - ((t-t_2) - \frac{1}{\omega_{r1}}\sin(\omega_{r1}(t-t_2))) - ((t-t_3) - \frac{1}{\omega_{r1}}\sin(\omega_{r1}(t-t_3))) \\ & - ((t-t_4) - \frac{1}{\omega_{r1}}\sin(\omega_{r1}(t-t_4)))\big\} + (\frac{(1-f_c)f_p + f_f f_g}{(1-f_c)(1-f_e) - f_b f_f})\cos(\omega_{r1}t) \\ & + \omega_{r1}L_k(\frac{(1-f_e)f_g + f_b f_p}{(1-f_c)(1-f_e) - f_b f_f})\sin(\omega_{r1}t) \end{aligned} \tag{6.13}$$

6.3.3 Chain-link power and stored energy dynamic modelling

In order to evaluate energy storage requirements, semiconductor *VA* requirement, semiconductor switching and conduction losses and other aspects of the TrSCC-DC-DC with the proposed configurations, the average power, chain-link power dynamics, energy dynamics, chain-link voltage and current dynamics are required and they will be addressed in this section. The energy dynamics of the tank components, L_kP_i, L_kS_i, C_{bP_i}, and C_{bS_i}, and the chain-link SM capacitance, C_{SMP} and C_{SMS},

can be found using the expressions for the tank current, equivalent DC blocking capacitor voltage and the chain-link voltages which were modelled in the previous section.

The chain-link energy variation, $\Delta e_{Chx}(t)$, can be derived by integrating the instantaneous chain-link power, $P_{Chx}(t)$, over the fundamental period as described in equation 6.14 where x represents primary and/or secondary. Referring to the equations 6.2 and 6.3, chain-link current contains DC current which can be ideally expressed as $I_{DCx} = \frac{P_{av}}{V_{DCx}}$ where the average transferred power, P_{av}, can be expressed as equation 6.15. The equations 6.16 and 6.17 show the rated transferred power, P_{av}, when phase shift is in intervals $0 \leq T_{sh} < T_t$ and $T_t \leq T_{sh} < T/2 - T_t$, respectively. Considering lossless converter and $N_{phase} > 2$, the expressions for the instantaneous primary first chain-link power, $P_{ChP\_1}(t)$, for the cases X and Y have been found and readers can find them in the tables A.1 and A.2 in section A.3 in the appendix. The instantaneous chain-link power can be found in the same way for all the chain-links.

Similar approach has been followed to find the rated transferred power and instantaneous chain-link power expressions for case Z. However, the expressions are not presented in this thesis since firstly, they are too long. Secondly, the case Z ($T/2 - T_t \leq T_{sh} < T/2$) is not preferred due to high energy storage requirements, high circulating current, high semiconductor current rating, etc.

$$\Delta e_{Chx\_i}(t) = \int P_{Chx\_i}(t)dt = \int V_{Chx\_i}(t) I_{Chx\_i}(t)dt \tag{6.14}$$

$$P_{av} = \frac{N_{phase}}{T/2} \int_0^{T/2} (V_{Chx\_i}(t) - \frac{V_{DCx}}{N_{phase}}) i_{ac\_i}(t)dt \tag{6.15}$$

$$\begin{aligned}P_{av} =& 2V_{DCP}(2I_0 cos(\omega_r T_t) - 2I_0 - 2C_b m cos(\omega_r T_t) + 2C_b m cos(\omega_r (T_{sh} - T_t)) \\ &+ C_b V_0 \omega_r^2 T_t + C_b \omega_r^2 m T_{sh}^2 - 2C_b V_0 \omega_r sin(\omega_r T_t) + I_{0t} sin((T\omega)/2) \\ &- C_b \omega_r m T_t sin((T\omega)/2) + C_b \omega_r m T_t sin((\omega_r (T - 2T_{sh}))/2) \\ &+ C_b \omega_r m T_t sin((\omega_r (T - 2T_t))/2) + C_b V_0 \omega_r^2 T_t cos((T\omega)/2) - 2C_b \omega_r^2 m T_{sh} T_t \\ &+ C_b \omega_r m T_t sin((\omega_r (2T_{sh} - T + 2T_t))/2))/(T\omega_r^2 T_t) \; When \rightarrow 0 \leq T_{sh} < T_t \end{aligned} \tag{6.16}$$

$$\begin{aligned}P_{av} =& 2V_{DCP}(2I_0 cos(\omega_r T_{sh}) - 2I_0 - 2C_b m cos(\omega_r T_{sh}) + 2C_b m cos(\omega_r (T_{sh} - T_t)) \\ &+ 2I_0 \omega_r T_{sh} sin(\omega_r T_{sh}) - 2I_0 \omega_r T_t sin(\omega_r T_{sh}) + C_b V_0 \omega_r^2 T_t - C_b \omega_r^2 m T_t^2 \\ &- 2C_b V_0 \omega_r sin(\omega_r T_{sh}) + I_0 \omega_r T_t sin((T\omega_r)/2) - C_b \omega_r m T_t sin((T\omega_r)/2) \\ &- 2C_b \omega_r m T_{sh} sin(\omega_r T_{sh}) + 2C_b \omega_r m T_t sin(\omega_r T_{sh}) \\ &+ C_b \omega_r m T_t sin((\omega_r (T - 2T_{sh}))/2) + C_b \omega_r m T_t sin((\omega_r (T - 2T_t))/2) \\ &+ C_b V_0 \omega_r^2 T_t cos((T\omega_r)/2) + 2C_b \omega_r m T_{sh} sin(\omega_r (T_{sh} - T_t)) \\ &- 2C_b \omega_r m T_t sin(\omega_r (T_{sh} - T_t)) + 2C_b V_0 \omega_r^2 T_{sh} cos(\omega_r T_{sh}) - 2C_b V_0 \omega_r^2 T_t cos(\omega_r T_{sh}) \\ &+ C_b \omega_r m T_t sin((\omega_r (2T_{sh} - T + 2T_t))/2))/(T\omega_r^2 T_t) \; When \rightarrow T_t \leq T_{sh} < T/2 - T_t \end{aligned} \tag{6.17}$$

The instantaneous energy in the chain-links, $E_{Chp}\_i(t)$, can be described as in equation 6.18 considering ideal energy sharing between the submodules within the corresponding chain-link where C_{SM} is the SM capacitance. The instantaneous SM capacitor voltage comprises a nominal voltage component (constant voltage) and an alternating voltage component, $\Delta V_{SM_x}(t)$. Considering the perfect energy sharing between the SMs, the energy variation can be expressed as a function of the alternating voltage component, $\Delta V_{SM_x}(t)$, as equation 6.19. Having the expression for the energy variation, selecting a desired C_{SM} will limit the peak to peak variation in the SM voltage ripple, $\Delta V_{SM_x}(t)$, as equation 6.20 where δ_{pp} is the per unit peak to peak SM voltage ripple normalised with the nominal V_{SM}. The per phase chain-link stored energy, E_{Ch}_i can be approximated as equation 6.21.

$$E_{Chx}\_i(t) = \frac{1}{2} C_{SMx} N_{SMx} V_{SMx}(t)^2 \tag{6.18}$$

$$\Delta e_{Chx\_}i(t) \approx C_{SMx}N_{SMx}V_{SMx}\Delta V_{SMx}(t) \tag{6.19}$$

$$C_{SMx} \geq \frac{\Delta e_{pp\_}Chx}{N_{SMx}V_{SMx}^2\delta_{pp}} \tag{6.20}$$

$$E_{Ch\_}i \approx \frac{\Delta e_{pp\_}ChP + \Delta e_{pp\_}ChS}{2\delta_{pp}} \tag{6.21}$$

Furthermore, the energy requirements of the tank can be analytically calculated as equation 6.22 where $V_{C_{bP\_}i(t)}$ and $V_{C_{bS\_}i(t)}$ can be found as equations 6.23 and 6.24, respectively.

$$\begin{aligned} E_{CL\_TrSCC\_}i = 0.5C_{bP}\hat{V_{C_{bP\_}i}}^2 + 0.5C_{bS}\hat{V_{C_{bS\_}i}}^2 \\ + 0.5\hat{i_{ac\_}i}^2(L_{kP} + L_{kS}) \end{aligned} \tag{6.22}$$

$$V_{C_{bP\_}i}(t) = \frac{V_{DCP}}{N_{Phase}} + 0.5v_{Cb}(t) \tag{6.23}$$

$$V_{C_{bS\_}i}(t) = \frac{V_{DCS}}{N_{Phase}} + 0.5v_{Cb}(t) \tag{6.24}$$

The expression 6.25 shows the energy requirements of the trapezoidal SCC-DC-DC configuration where considering lossless converter the full load average transferred power is equal to the rated power, $P_{av} = P_r$.

$$H_{cTrSCC} = \frac{N_{Phase}(E_{CL\_}i + E_{Ch\_}i)}{P_r} \tag{6.25}$$

6.4 Energy storage requirements, semiconductor losses and device rating

This section focuses on the energy storage requirements, semiconductor losses, semiconductor device rating and transformer $\frac{dv}{dt}$ stress. Unity transformer turns ratio has been assumed and in order to show the optimum operating points for every scenario, further factors have been considered as following:

- Frequency factor, $K_f = \frac{f_o}{f_r}$, where f_o is the operating frequency and f_r is the resonant frequency between L_k and C_b
- Impedance factor $Z_b = \frac{L_k}{L_s}$ where L_s is the series inductance of the single phase transformer, assuming a 10% impedance.

In order to investigate the influence of different parameters and to determine optimum selections, a search amongst different candidate solutions was performed as defined in table 6.1. Energy storage requirements, semiconductor losses and semiconductor device rating were calculated analytically at every value of K_f, T_{sh}, T_t and Z_b.

Table 6.1: Parameters and their investigated range

Parameters	Value	Comment
K_f	$1 < K_f \leq 4$	$K_f > 1$ to avoid amplification of tank current harmonic components
T_t	$T_t = \frac{T}{40}$, $T_t = \frac{T}{20}$ & $T_t = \frac{T}{4}$	
φ (T_{sh})	$0.05\frac{\pi}{2} \leq \varphi \leq \frac{\pi}{2}$	
Z_b	$2 \leq Z_b < 25$	L_k & C_b are chosen to keep constant power for all conditions

Furthermore, the peak to peak SM capacitor voltage ripple with respect to the nominal voltage was assumed to be $\delta_{pp} = 5\%$ (more clarification about this assumption will be shown in simulation section, 7.2). Figures, 6.11, 6.13 and 6.12 show the per unit energy requirements at different operation points (rated power is maintained at each operation point), $H_{CTrSCC}(PU) = \frac{H_{cTrSCC}}{H_b}$, where $H_b = \frac{1}{f_o}$ is the base capacitance constant.

It can be observed in figures 6.11 that H_{cTrSCC} reduces with reducing T_t when $\varphi > 0.05\pi$, when $K_f = 1.25$. Figure 6.12 shows that the optimum φ to achieve minimum H_{cTrSCC} differs with different values of T_t and K_f and the optimum region of φ is $0.075\pi \rightarrow 0.35\pi$. Furthermore, figure 6.13 shows that decreasing T_t is less effective

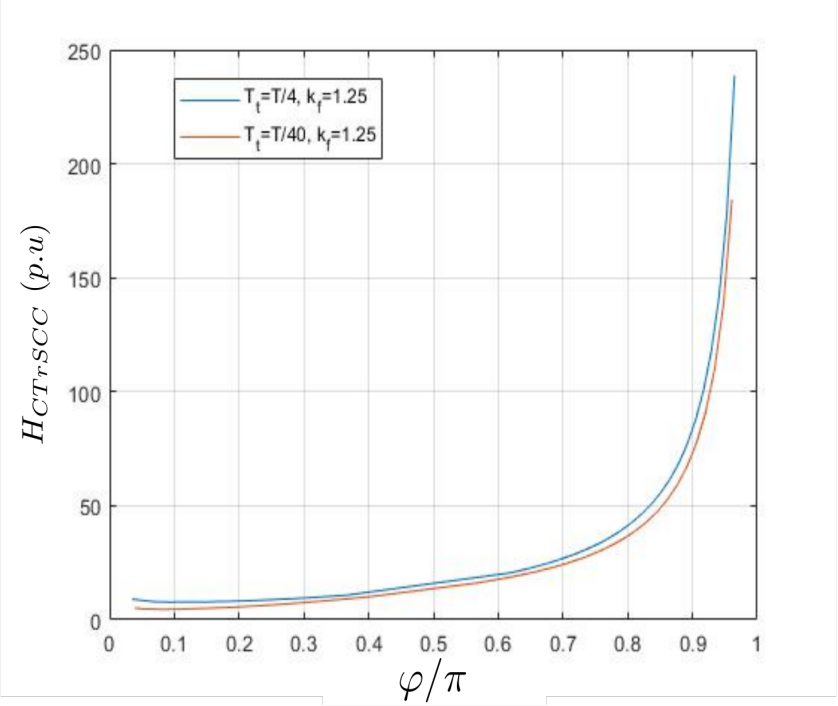


Figure 6.11: *Energy requirements at different operating points*

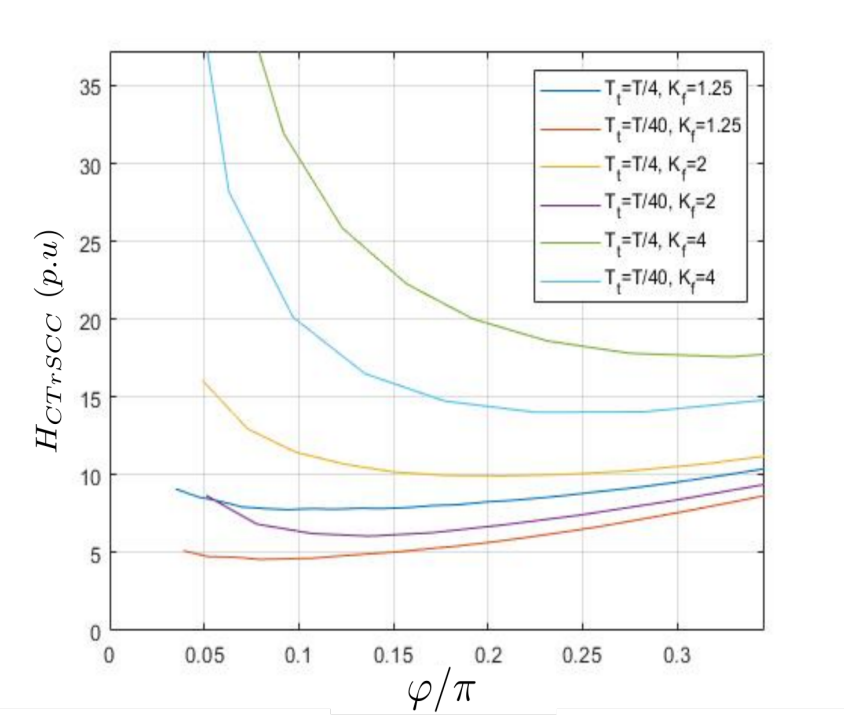


Figure 6.12: *Energy requirements at different operating points*

in achieving H_{cTrSCC} reduction when $T_t \lessapprox T/20$. Reducing T_t can have a negative impact on $\frac{dv}{dt}$ stress across the transformer. However the possibility of increasing the number of the phases can overcome the negative impact of T_t reduction as discussed later.

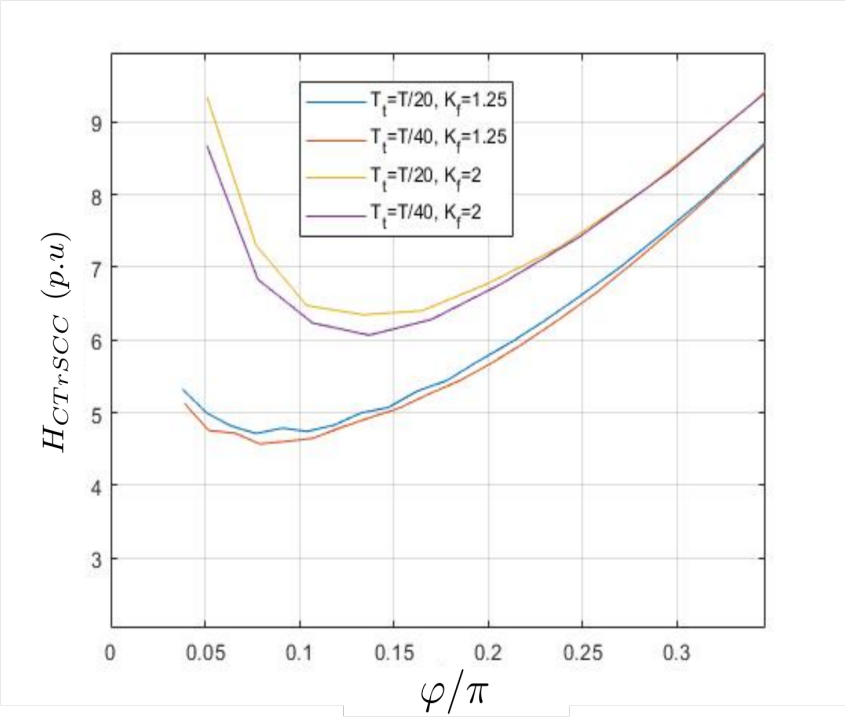


Figure 6.13: *Energy requirements at different operating points*

Figure 6.14 shows the chain-link capacitance constant, H_{ch}, and tank capacitance constant, H_{tnk}, at different K_f and $T_t = T/40$ where it can be observed that increasing φ will lead to an increase in H_{ch} whereas H_{tnk} will reduce up to a certain point according to the value of K_f. On the other hand, increasing K_f leads to an increase in H_{tnk} but a reduction in H_{ch} up to $\varphi \leq 0.25\pi$. In conclusion, it can be observed that keeping K_f and T_t as small as possible will provide low energy storage requirement at a particular φ, however as previously explained the harmonic component of the tank current could be excessive if $K_f < 1.25$ due to resonance where the power flow cannot be controlled. Additionally, reducing T_t is easy in the TrSCC-DC-DC and a very small T_t can be achieved even at high operating frequency without affecting the $\frac{dv}{dt}$ stress across the transformer by increasing the number of phases, as discussed and demonstrated later.

Regarding the semiconductor *VA* requirement which reflects semiconductor area and cost, similar to other modes shown in previous chapters, equation 6.26 has been used to show semiconductor *VA* requirement.

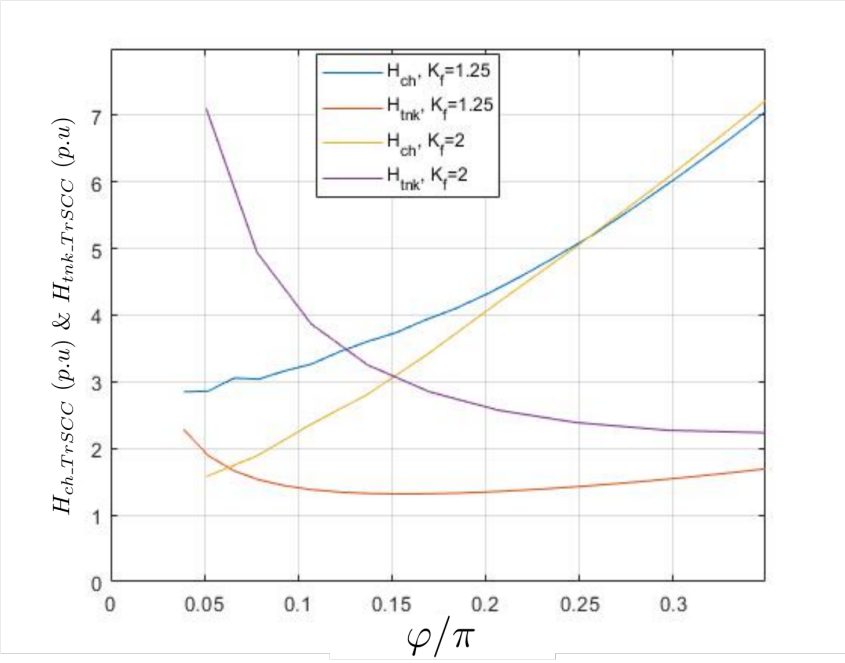


Figure 6.14: *Chain-link and tank energy requirements at $T_t = T/40$*

$$VA_{TrSCC} = \frac{2N_{Phase}N_{SM}V_{SM}\hat{I_{Chx\_i}}}{Pr} \tag{6.26}$$

Figure 6.15 shows the VA_{TrSCC} with respect to the rated power where it can be seen that reducing T_t leads to a reduction in VA_{TrSCC} mainly because lower order odd harmonics, $3^{rd}, 5^{th}, 7^{th}, etc$, of the chain-link voltages will contribute in transferring power between the primary and secondary chain-links. As a result, less current is required to transfer the same power. Figure 6.15 also shows that increasing K_f leads to a reduction in VA_{TrSCC} due to operation further away from resonance which again results in the lower order odd harmonics of the tank current to contributing to power flow. Accordingly, peak current of the chain-link current, $\hat{I_{Chx\_i}}$, will reduce, considering same demanded power flow. Additionally, it can be observed that reducing T_t below a specific limit, $T_t \lessapprox T/20$, will slightly reduce VA_{TrSCC}.

Semiconductor loss analysis is undertaking as previously described using equations 5.1-5.8. The SMs are sorted at fundamental frequency in all studies including practical validation for all TrSCC-DC-DC modes. Table 6.2 shows the specifications of the HVDC system where the same power, P_r, and DC-link voltage

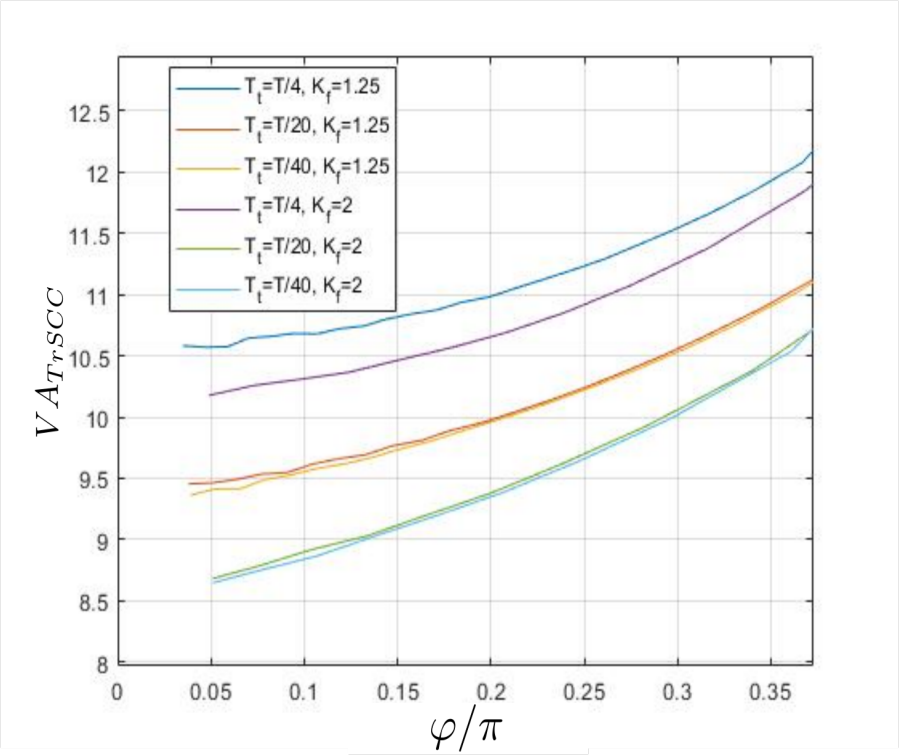


Figure 6.15: *TrSCC-DC-DC total VA semiconductor at different operating points*

used in the TrMMC-DC-DC and MTrMMC-DC-DC studies in chapter 4-section5.2, are considered. Furthermore, the semiconductor parameters from chapter 4 (E_{on}, E_{off}, E_r, V_f, R_f, etc) are assumed for the devices (HiPak IGBT module 5SNA 1800E330400).

Table 6.2: HVDC system specification and parameters of the TrSCC-DC-DC

Parameters	Value
$V_{DCP} = V_{DCS}$	400kV
P_r	800MW
V_{SM}	2kV
N_{SM} *Per Chain-Link*	$\frac{2V_{DCx}}{N_{phase}*V_{SM}}$
δ_{pp}	5%
$f_{sorting}$	f_o

Figure 6.16 shows the percentage total semiconductor power losses, T_L, switching power losses and conduction power losses, with respect to rated power at different T_t, K_f, φ and fixed $f_o = 500Hz$. It can be noticed that a reduction in T_L is achieved by reducing T_t because of increase in lower odd harmonic orders as T_t reduced. As a result, less tank current is required to transfer rated power between the primary and

secondary chain-links. Additionally, the instants of the SM switching actions with respect to the chain-link current move to a more favourable locations. These effects reduce both the conduction and switching losses. Moreover, increasing K_f leads to a reduction in T_L up to $\varphi \lessapprox 0.22\pi$ when T_t is small. However for large T_t, T_L can increase as shown in figure 6.16 where $T_t = T/4$. The reason is mainly due to the chain-link voltage and the tank current waveform where firstly, as T_t increases the magnitude of the odd harmonics in chain-link voltages will reduce, hence, higher tank current will be required to transfer the demanded power. Secondly, increasing K_f at low values of T_t will slightly increase the magnitude of the odd harmonic in the chain-link current, and accordingly, the SM switching actions during T_t will be at unfavorable locations with respect to the chain-link current values.

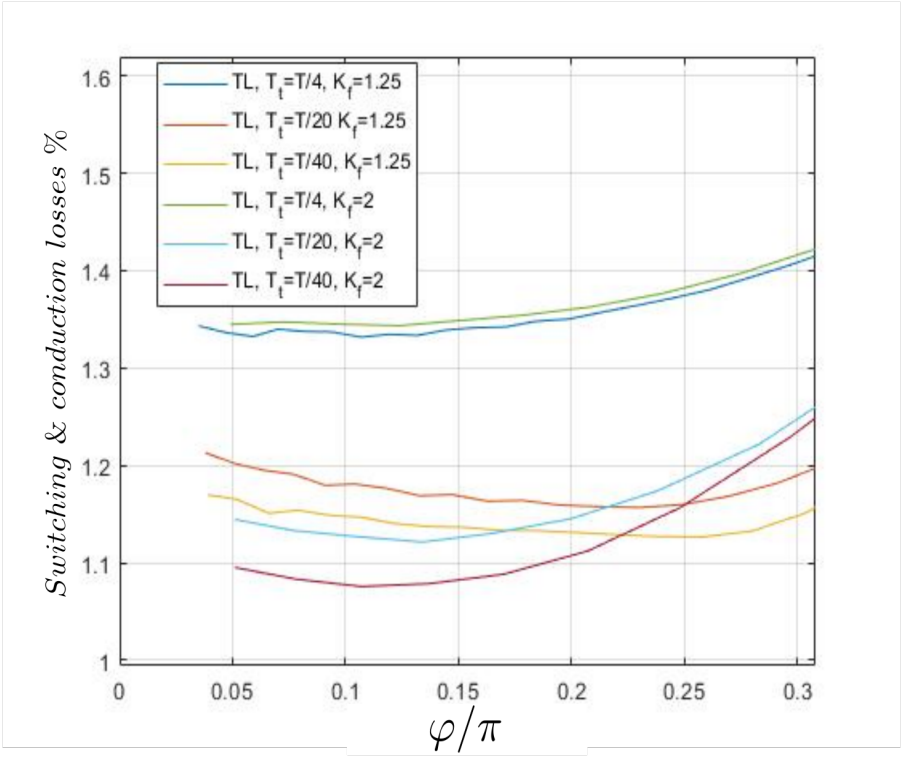


Figure 6.16: *Semiconductor losses of TrSCC-DC-DC at different K_f, φ and T_t*

Figure 6.17 shows T_L at different operating frequencies where it can be observed that percentage conduction losses, *CnL*, dominates the semiconductor losses when $f_o \leq 500Hz$. Considering all of the discussion above and semiconductor losses only, the total losses will remain low, $T_L < 2\%$, even if the system operates at $f_o = 1kHz$.

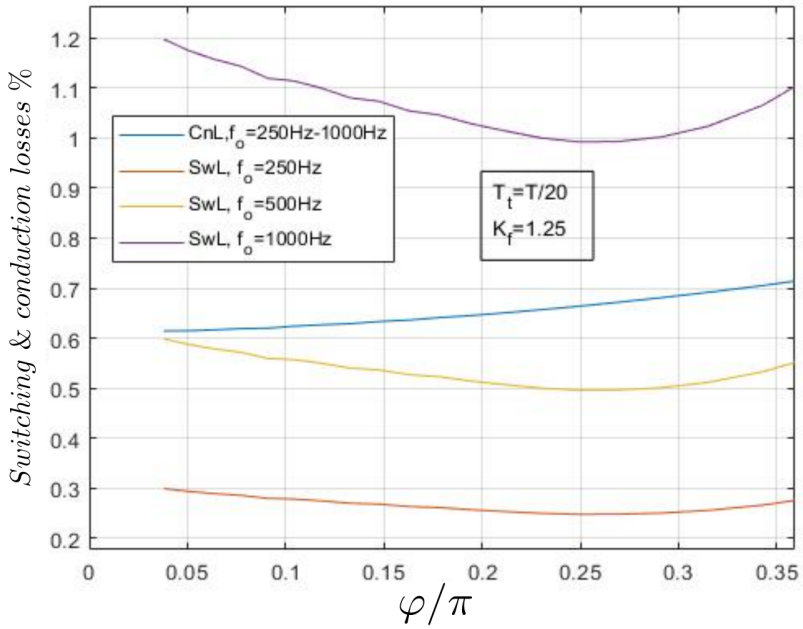


Figure 6.17: *Semiconductor losses of TrSCC-DC-DC at different* f_o, φ $T_t = T/20$ *and* $K_f = 1.25$

Moreover, considering that power flow is from the primary to secondary, the turn-off losses dominates the switching losses as shown in figure 6.18 where SwL_{on} and SwL_{off} are the percentage turn-on losses and turn-off losses with respect to rated power, respectively. Additionally, it may be possible to further reduce the turn-off losses using capacitor snubbers, that is not explored further in this thesis.

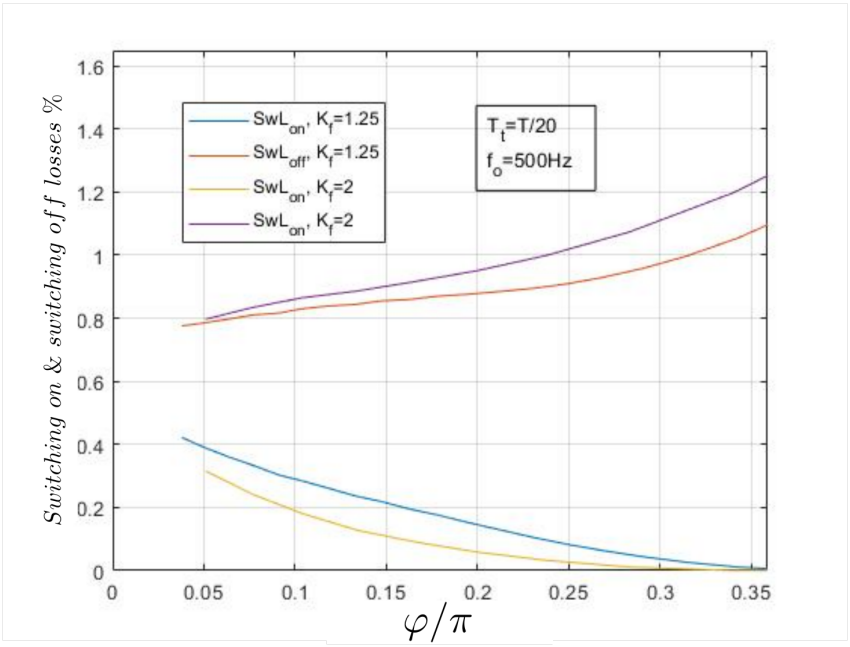


Figure 6.18: *Switching on/off losses of TrSCC-DC-DC*

When the power flow is from the primary to secondary, the turn-on power loss, SwL_{on}, is very small, and it can be eliminated at certain φ based on the operating conditions of the system which can be potentially interesting for unidirectional power flow applications. Figure 6.19 shows the ideal instantaneous primary chain-link voltage and current waveforms of one phase, considering the HVDC system shown in table 6.2, where it can be observed that the chain-link current $I_{Chx}(t)$ is > 0 during the insertion period of the SMs, T_t, at both $\varphi = 0.1\pi$ and $\varphi = 0.3\pi$. Referring to figure 6.20, the $I_{Chx}(t)$ path commutates from T_2 to D_1 when the SM is inserted. As a result, S_1 has a soft turn-on and S_2 has a hard turn-off. During the transition when the SMs are bypassed and $\varphi = 0.1\pi$, only a few devices have soft turn-on since $I_{Chx}(t) > 0$ for most of the transition and hence the device T_2 in each SM will experience a hard turn-on. However when $\varphi = 0.3\pi$, $I_{Chx}(t) < 0$ for all of the transition and all devices have soft turn-on. Unfortunately, whilst it may seems that $\varphi = 0.3\pi$ is favourable from the point of view of switching losses, the energy storage requirements, semiconductor current rating (VA_{TrSCC}) and conduction losses are increased in comparison to $\varphi = 0.1\pi$.

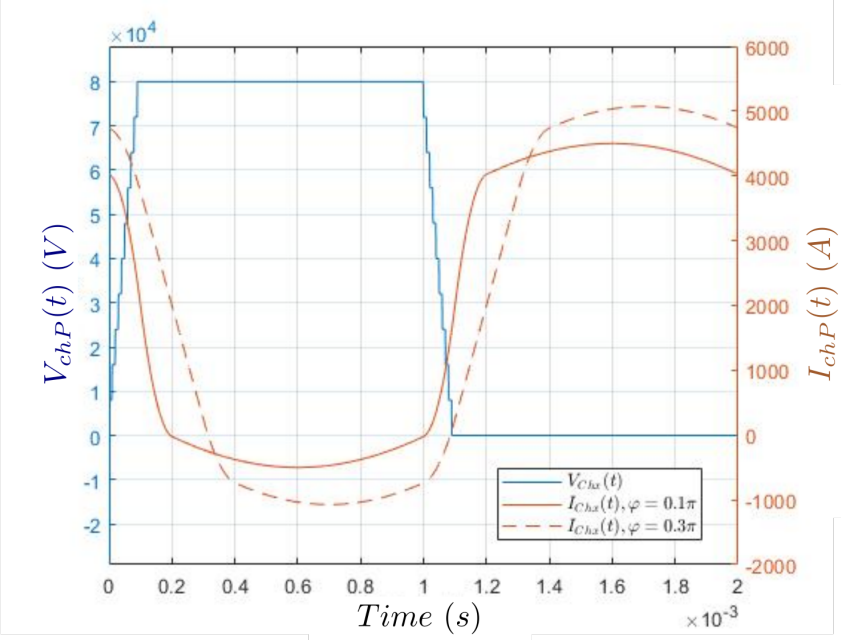


Figure 6.19: *Ideal chain-link voltage and current waveforms at* $K_f = 2$, $f = 500$ *and* $N_{phase} = 10$

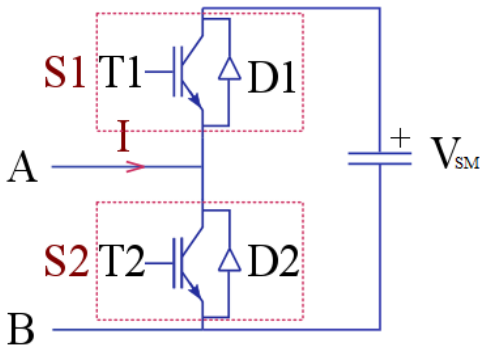


Figure 6.20: *Half bridge SM*

Regarding the semiconductor device utilisation, similar to the MTrMMC-DC-DC, the chain-link current conducts continuously in the TrSCC-DC-DC converter as can be observed in figure 6.19. Hence the TrSCC-DC-DC provides reasonable device utilisation where both the upper and lower devices are carrying the chain-link current during one fundamental cycle.

In conclusion, the optimum operating region is when $\varphi = 0.05\pi - 0.2\pi$, $K_f = 1.25 - 2$ and $T_t \lessapprox T/20$ where minimum energy storage requirement is achieved at $\varphi = 0.075\pi$, $K_f = 1.25$ and $T_t \lessapprox T/20$. However, the minimum semiconductor device current rating, VA_{TrSCC}, is achieved at $\varphi = 0.05\pi$, $K_f = 2$ and $T_t \lessapprox T/20$. Considering the semiconductor power losses, the TrSCC-DC-DC operates more efficiently at $K_f = 2$, $T_t \lessapprox T/20$ and $\varphi \approx 0.15\pi$. Therefore, $K_f = 1.5$ and $\varphi \approx 0.1\pi$ have been chosen for the comparison studies.

6.5 Converter control

This section focuses on the control structure that is required to operate the TrSCC-DC-DC. The primary and secondary chain-link modulation signals are imposed and the power transferred between the chain-links is controlled by controlling the phase shift, $\varphi(T_{sh})$, between the primary and secondary chain-links. The system conditions will determine whether controlling the chain-link voltages and DC current control are required or not. Therefore, the control structure of the TrSCC-DC-DC can be divided into the following types.

6.5.1 AC power flow control

The power transferred between the two DC-link ports can be regulated by controlling the phase shift, $\varphi(T_{sh})$ between the primary and secondary modulation signals to produce a phase shift between the primary and secondary transformer voltages. Equations 6.16 and 6.17 show the relationship between the transferred power and $\varphi(T_{sh})$ based on the operating conditions. By applying a small signal analysis and using a PI controller, the amount of required $\Delta\varphi(\Delta T_{sh})$ will be added to $\varphi(T_{sh})$ to give the desired power flow as illustrated in figure 6.21.

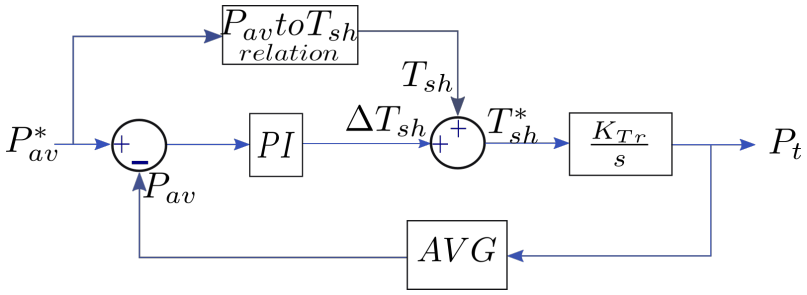


Figure 6.21: *Power flow control scheme*

The primary chain-link modulation signals are fixed and the secondary chain-link modulation signals are shifted by the reference phase shift, T^*_{sh}, to deliver the desired power, P^*_{av}. There are two possible methods of implementing the power flow control, per phase AC power flow control and total power flow control. Measuring the AC current of each phase and taking the average of the product between the AC current and the AC part of the chain-link voltage will provide the per phase average AC power flow, $\overline{i_{ac\_i}(t)V_{chx\_ac}(t)} \approx \frac{P_{av}}{N_{phase}}$. Considering the fact that the resonant tank elements, inductors and blocking capacitors, and transformer leakage inductance, losses and magnetisation inductance are not identical between the phases hence the impedance of the phases are not equal. Implementing per phase AC power control ensures equal power flow sharing between the phases as a result the AC currents will approximately cancel out each other from the DC side. However, implementing per phase control will introduce different T_{sh} between the phases and considering one side of the converter, the AC components of the chain-link voltages will not cancel

and spurious voltage levels can be introduced. Ultimately, unwanted voltage levels can cause significant ripple in the DC currents and can also cause significant transient disturbances in the case of high $\frac{dv}{dt}$.

In the total power flow control, only the DC current measurement is required to calculate the total power flow, P_{av}, and the control will introduce the same T_{sh} between the primary and secondary for all phases. As a result, ideally, there will be no spurious voltage levels produced due to different T_{sh}. Although the impedance mismatch between the phases will result in different power flows, with a reasonable number of phases with mode B or C will help to provide harmonic cancellation based on the number of phases which will be explained in section 7.3. Considering that non ideal gate drives are used to drive the semiconductor devices, spurious voltage levels can be produced for very short periods, $\lessapprox 1(\mu s)$, even with total power flow control. However, due to their short duration their impact is negligible. Based on these considerations, total power flow control is implemented in simulation and the experimental tests in this research.

In the applications where DC-link voltage ports are fixed, fast power flow control is not required and, when the SM peak to peak voltage ripple, δ_{pp}, is small, the control structure of the TrSCC-DC-DC will only include power flow control. Additionally, by using the balancing method presented previously in chapter 4-section 4.3 the voltage of the submodule capacitors can be balanced.

6.5.2 Chain-link energy and DC current control in the TrSCC-DC-DC

When the voltage at one side of the DC ports is not fixed it is necessary to control the voltage of the chain-links (sum of the SM capacitor voltages). This is also necessary when there is a fast transient in the power demand (a step change of roughly 15% of the rated power).

In this case a similar approach to that shown in chapter 4-figure 4.21 can be used for the TrSCC-DC-DC energy control. Figure 6.22 shows the scheme in which the total energy control (outer loop) provides a reference to the DC current control loop (inner loop). The DC equivalent circuit shown previously in figure 6.6 is used to determine the transfer function of the DC current controller for each side of the TrSCC-DC-DC. One voltage level of the chain-link waveforms is modified to achieve the control of the SM voltage as previously shown in figure 4.21. More voltage levels can be modified if required however the time between level transitions must be maintained at T_d to prevent high $\frac{dv}{dt}$ stress across the transformer.

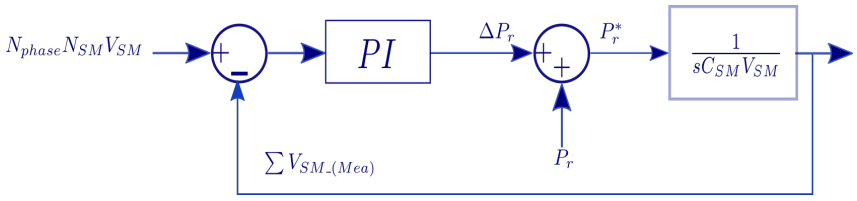


Figure 6.22: *Energy control scheme*

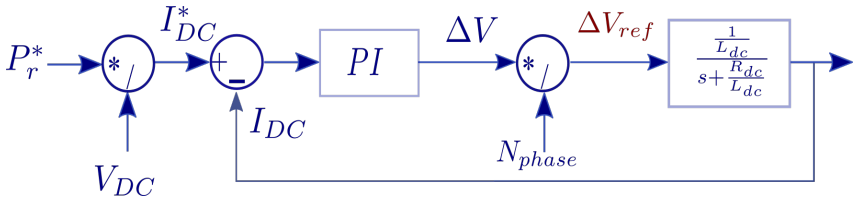


Figure 6.23: *DC current control scheme*

Since the total energy control (total SM capacitor voltage) in the TrSCC-DC-DC is a similar method to that shown in chapter 4-figure 4.21 and the validation of the approach was shown through simulation for the MTrMMC-DC-DC in figure 5.9, therefore, the energy control method will be only practical validated for the TrSCC-DC-DC.

Finally, the energy control must be applied during transient only otherwise spurious voltage levels can be produced in steady state.

6.6 Summary

Trapezoidal operation of the series chain-link modular multilevel DC-DC converter was introduced in this chapter and three possible trapezoidal operating modes were addressed. A comprehensive model of the converter was developed and the required expressions for chain-link voltage, chain-link current, AC link current (tank current) and blocking capacitor voltage were found, considering all intervals and different phase shifts between primary and secondary chain-link voltage.

The dynamics of stored energy, the chain-link power, semiconductor power losses and required *VA* of the semiconductor device were determined at different operating conditions. Taking all aspects into account, the optimum operating region was $\varphi = 0.05\pi - 0.2\pi$, $K_f = 1.25 - 2$ and $T_t \lessapprox T/20$ where minimum energy storage is achieved at $\varphi = 0.075\pi$, $K_f = 1.25$ and $T_t \lessapprox T/20$. However, the minimum semiconductor device current rating, VA_{TrSCC}, is achieved at $\varphi = 0.05\pi$, $K_f = 2$ and $T_t \lessapprox T/20$. Considering the semiconductor power losses, the TrSCC-DC-DC operates more efficiently at $K_f = 2$, $T_t \lessapprox T/20$ and $\varphi \approx 0.15\pi$.

Power flow control, energy control and DC current control design of the TrSCC-DC-DC were discussed. Considering an HVDC interconnection application, controlling only total power flow smoothly in the TrSCC-DC with capacitor SM voltage balancing method are enough to achieve power flow when the SM capacitor peak to peak voltage ripple is $\delta_{pp} \leq 5\%$.

The next chapter will focus on a simulation study to validate all the three TrSCC-DC-DC operating modes, theoretical analysis and the control loops by modelling an HVDC system in PLECS software. A comprehensive comparison between the TrSCC-DC-DC modes and the addressed MMC-DC-DC operating modes (Sinusoidal MMC-DC-DC, TrMMC-DC-DC and MTrMMC-DC-DC) will be presented in the next chapter.

Chapter 7

Series Chain-Link Modular Multilevel DC-DC Converter: Simulation Study and Evaluation

7.1 Introduction

This chapter focuses on the validation of the TrSCC-DC-DC operating modes and theoretical analysis through simulation where a system is modelled in PLECS software.

It also shows a comprehensive comparison between the TrSCC-DC-DC operating modes in terms of energy storage requirement, transformer $\frac{dv}{dt}$ stress, power density, semiconductor power losses and device *VA* requirement. Additionally, a comparison between the TrSCC-DC-DC configurations and MMC-DC-DC configurations (sinusoidal MMC-DC-DC, TrMMC-DC-DC and MTrMCC-DC-DC) discussed in chapters 4 and 5 will be presented.

Finally, the DC fault blocking capability of the TrSCC-DC-DC will be briefly discussed and illustrated through simulation.

7.2 Simulation results

An HVDC system with the specifications shown in table 7.1 has been built in PLECs software to validate the TrSCC-DC-DC operating modes and basic design calculations. The HVDC specifications are the same as those used for the other topologies in chapter 4-section 5.2

Table 7.1: HVDC system specifications and parameters of TrSCC-DC-DC

Parameters	Value
$V_{DCP} = V_{DCS}$	400kV ($\pm 200kV$)
P_r	800MW
V_{SM}	2kV
N_{phase}	10
N_{SM} *Per Chain-Link*	$\frac{2V_{DCx}}{N_{phase} * V_{SM}}$
f_o	1kHz
δ_{pp}	5%
T_d	10μs
K_f	1.5
$H_{cTrSCC-B}$	4.9 ms
$H_{cTrSCC-C}$	5.58 ms
$H_{cTrSCC-A}$	4.9 ms

7.2.1 Mode A simulation results

Figure 7.1 shows the phase 1 primary and secondary voltage waveforms, $V_{ChP\_1}(t)$ and $V_{ChS\_1}(t)$, primary inductor voltage and blocking capacitor voltage waveforms, $V_{LkP\_1}(t)$ and $V_{CbP\_1}(t)$, primary and secondary SM voltages per voltage level waveforms, $V_{CgP\_1}(t)$ and $V_{CgS\_1}(t)$ for steady state operation in mode A. The chain-link and the SMs peak to peak voltage ripple, $\delta_{pp} = 5\%$, verifies the design methodologies.

The circuit configuration of mode A produces a noticeable second harmonic ($\approx 5\%$ of the DC link voltage) in the overall chain-link voltage waveform, $\sum_{i=1}^{10} V_{ChP\_i}(t)$. Accordingly, the operation is suitable only for a long distance where the HVDC

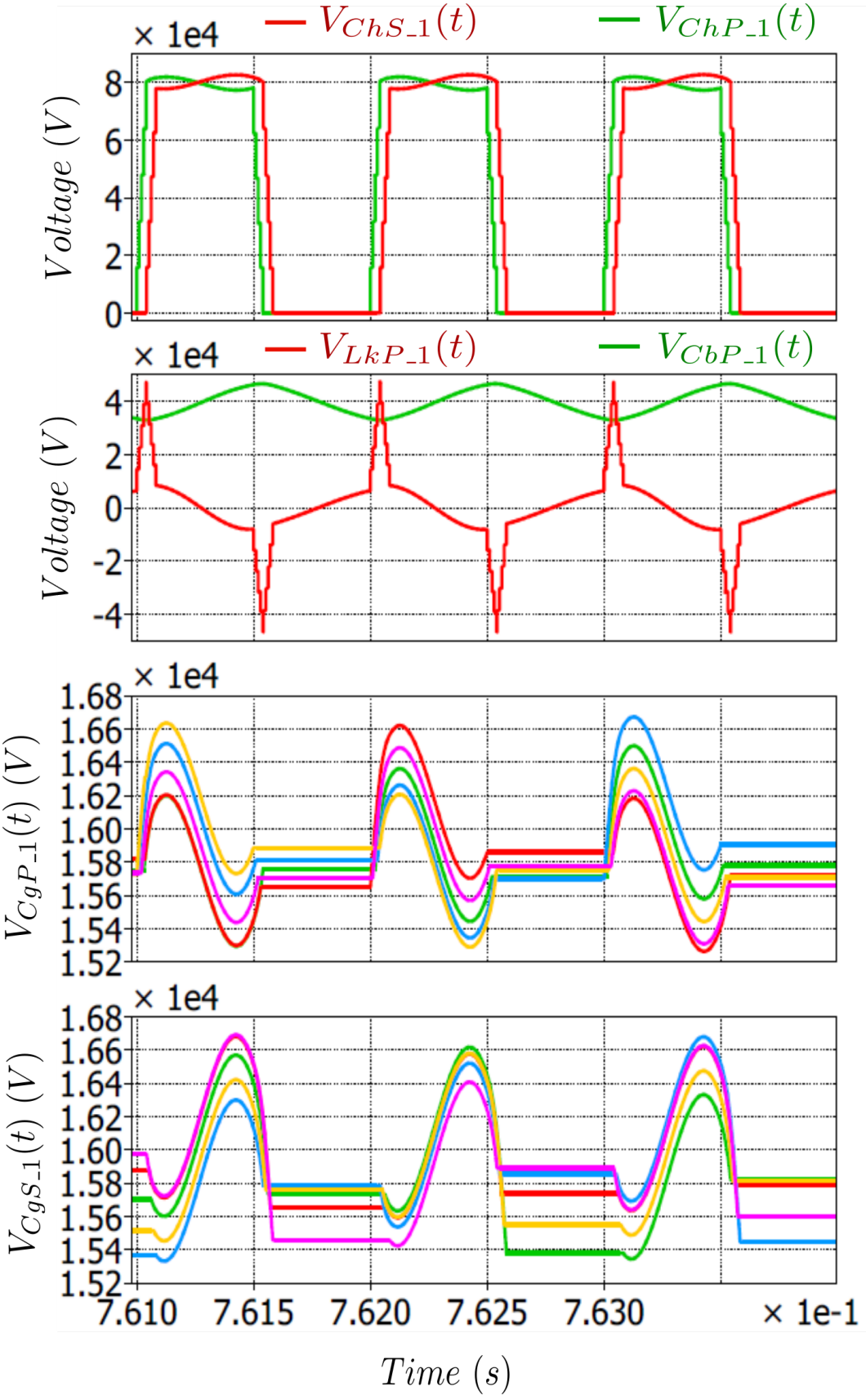


Figure 7.1: *Mode A steady state voltage waveforms*

cable inductance is large enough to smooth the DC current. otherwise additional filtering will be required. Figure 7.2 shows the overall chain-link voltage waveform, $\sum_{i=1}^{10} V_{ChP\_i}(t)$, instantaneous primary chain-link current waveform, $I_{ChP\_1}(t)$, tank AC current wavefrom, $i_{ac\_1}(t)$, and primary DC current waveform, I_{DCP}. It can be noticed that there is approximately 5% difference between the positive peak and negative peak values of $i_{ac\_1}(t)$. This is due to the chain-link voltage ripple (SMs capacitor voltage ripple) which introduces second harmonics in $i_{ac\_1}(t)$. Therefore, $\delta_{pp} \leq 5\%$ is preferred to prevent significant asymmetry in the tank current.

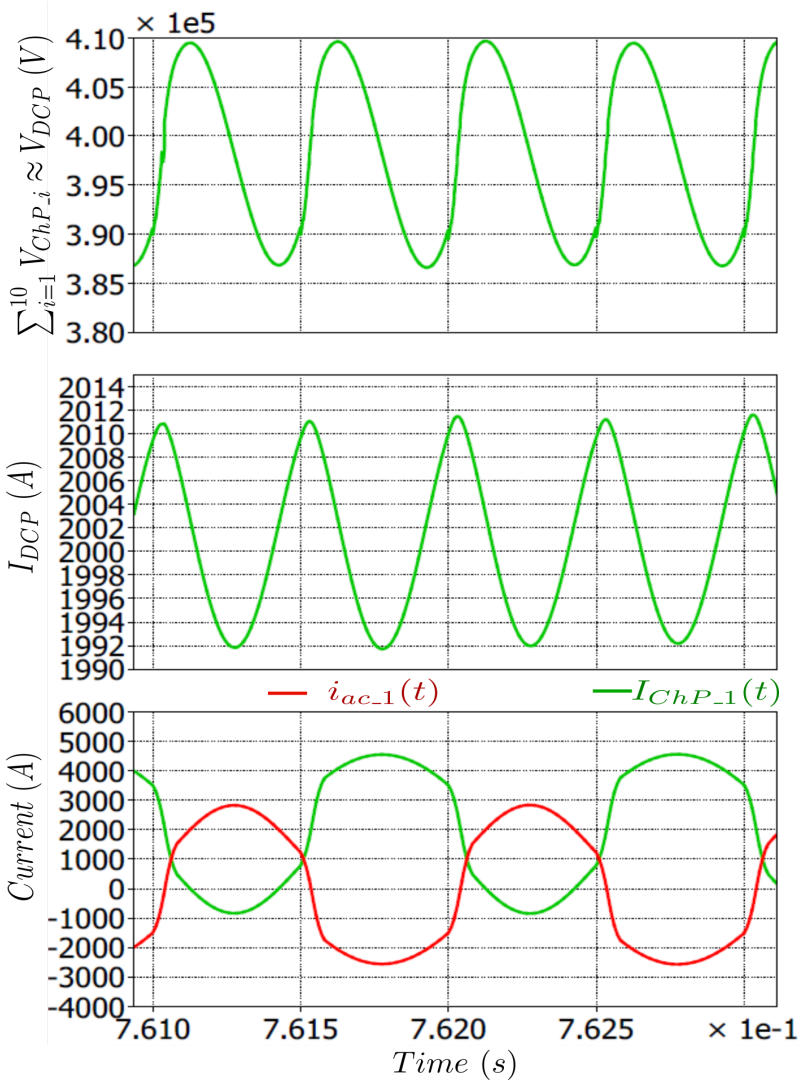


Figure 7.2: *Mode A steady state currents and overall chain-link voltage waveforms*

Figure 7.3 shows transient waveforms when the power flow is changed smoothly from 440MW to 800MW where only power flow control applied with the SM capacitor voltage balancing method introduced in 4-section 4.3. A high DC induc-

tance value, $L_{dcP} = 100mH$, is required to achieve smooth variation in the current waveforms and keep the SM capacitor voltage ripple within the acceptable limits, $\delta_{pp} \leq 5\%$.

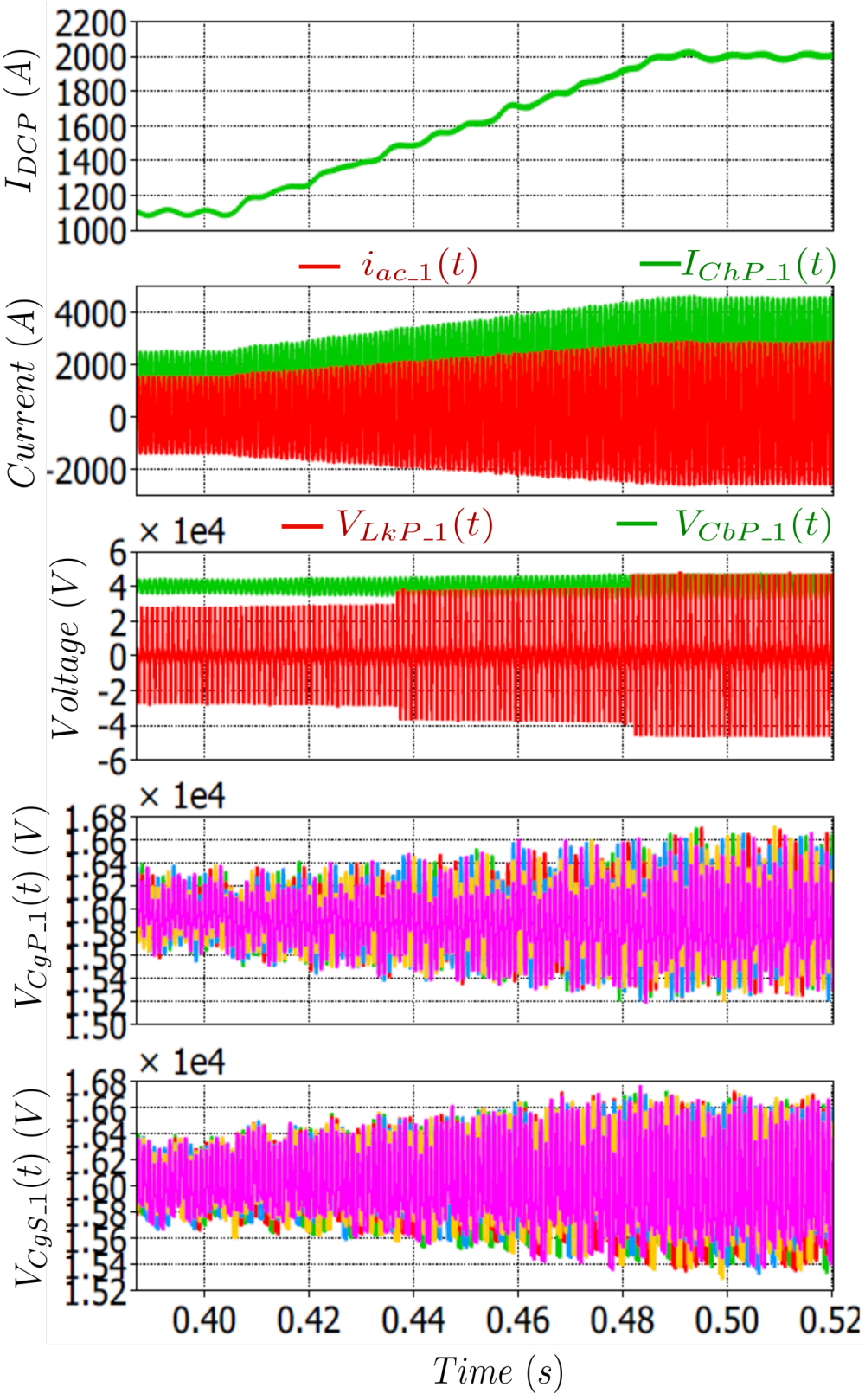


Figure 7.3: *TrSCC-DC-DC mode A response under 45% of power change*

7.2.2 Mode B simulation results

Figure 7.4 shows the phase 1 primary and secondary voltage waveforms, $V_{ChP\_1}(t)$ and $V_{ChS\_1}(t)$, primary inductor voltage and blocking capacitor voltage waveforms, $V_{LkP\_1}(t)$ and $V_{CbP\_1}(t)$, primary and secondary SM voltages per voltage level waveforms, $V_{CgP\_1}(t) = N_L * V_{SMP}(t)$ and $V_{CgS\_1}(t) = N_L * V_{SMS}(t)$ for mode B operation in steady state. It can be seen that C_{bP_1} blocks the DC voltage of the chain-link and the SMs peak to peak voltage ripple is $\delta_{pp} = 5\%$ which verifies the design calculations.

The overall chain-link voltage waveform, $\sum_{i=1}^{10} V_{ChP\_i}(t)$, instantaneous primary chain-link current waveform, $I_{ChP\_1}(t)$, tank AC current wavefrom, $i_{ac\_1}(t)$, and primary DC current waveform, I_{DCP}, are shown in figure 7.5. It can be seen that $i_{ac\_1}(t)$ is slightly asymmetrical about the x-axis with approximately 5% difference between the positive peak and negative peak values. This is due to the chain-link voltage ripple (SMs capacitor voltage ripple) which introduces second harmonics in $i_{ac\_1}(t)$ as shown in FFT figure 7.6. Consequently, $\delta_{pp} \leq 5\%$ is preferred to prevent significant asymmetry in the tank current which can cause problems in the transformer such as saturation, vibration, noise, etc. However, thanks to the circuit configuration of the TrSCC-DC-DC, mode-B, gives approximate cancellation of the second harmonics in the overall chain-link voltage as shown in figure 7.5 where the only harmonic $N_{phase} * f_o = 10 * f_o$ can be seen but its value is very small ($< 0.1\%$). As a result, the ripple in I_{DCP} is negligible even with very low DC inductance values ($L_{dcP} = 1mH$ is assumed in this simulation).

Figure 7.7 shows transient waveforms when the power flow is changed smoothly from 400MW to 800MW where only the power flow control applied with the SM capacitor voltage balancing method introduced in 4-section 4.3 and it can be noticed that the SM capacitor voltage ripple remains within the acceptable limits, $\delta_{pp} \leq 5\%$ and the current waveforms increase smoothly even with a low DC inductance value ($L_{dcP} = 1mH$).

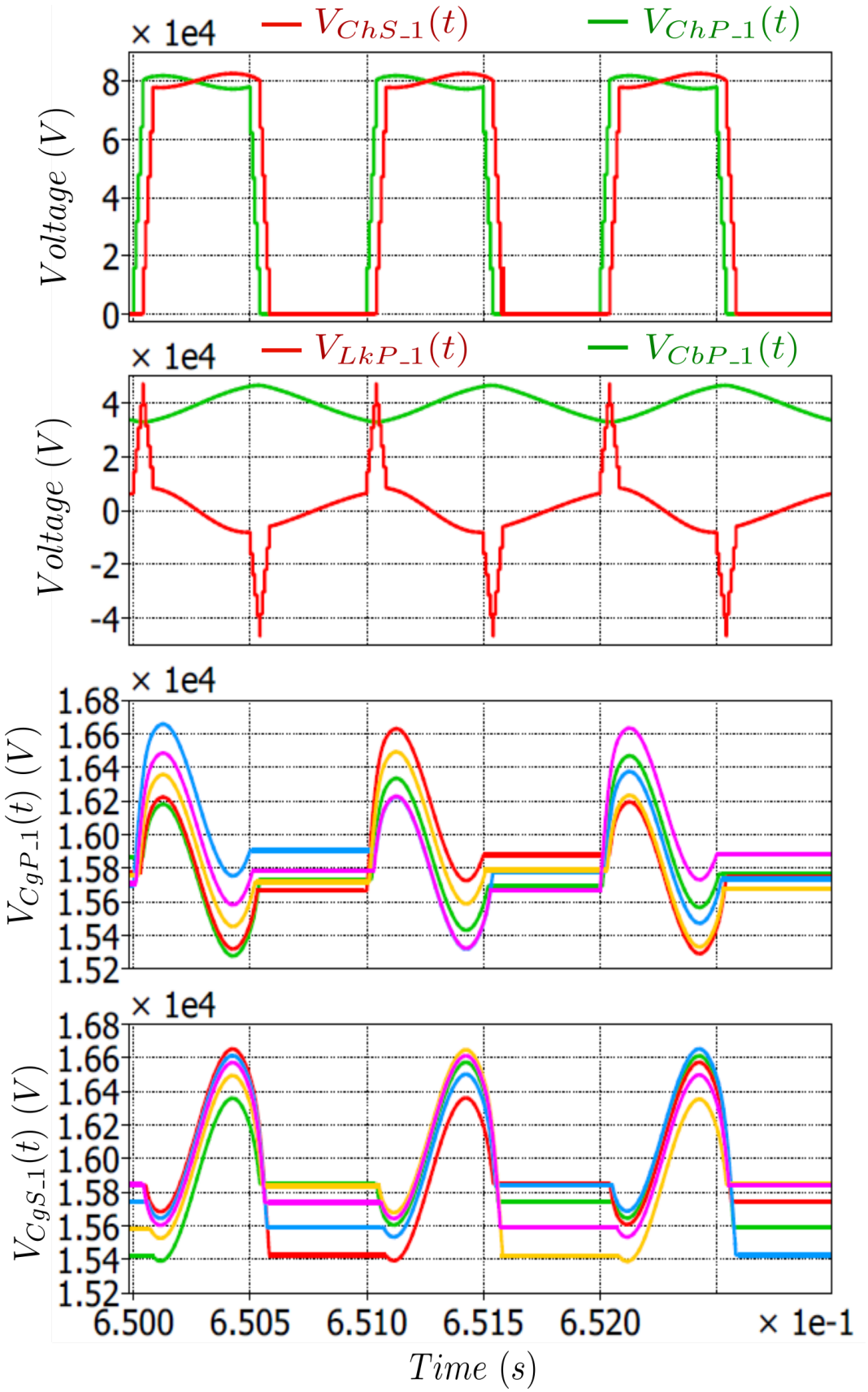


Figure 7.4: *Mode B steady state voltage waveforms*

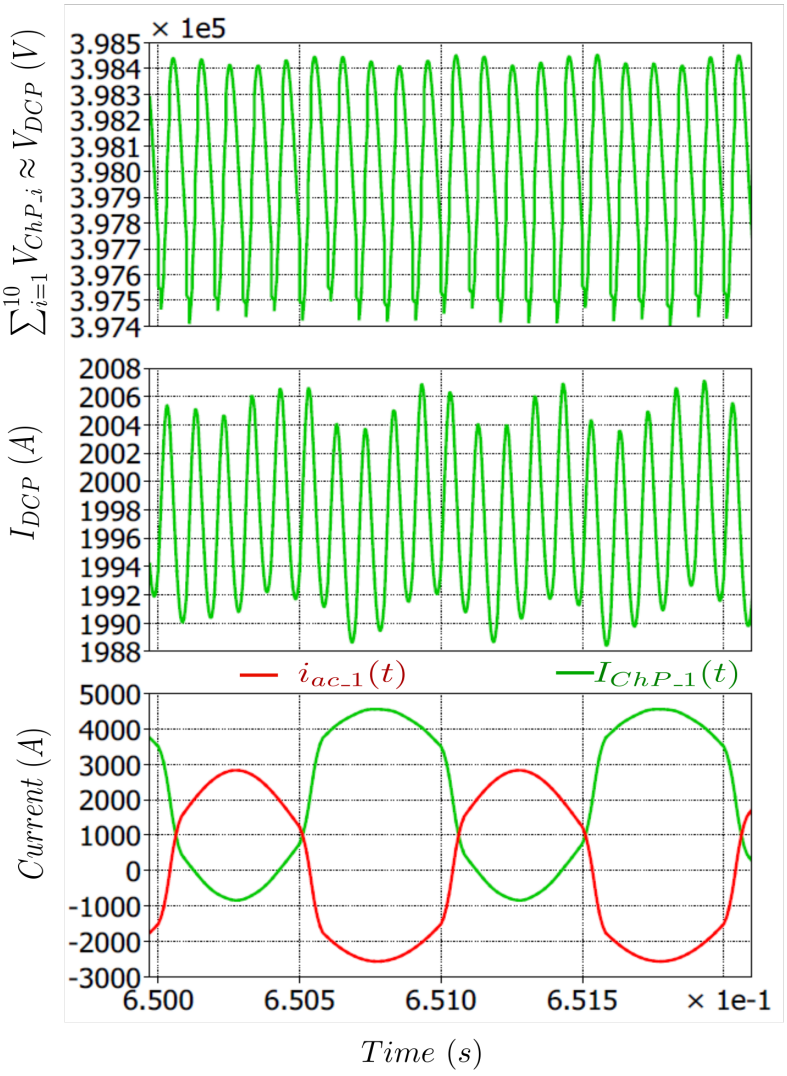


Figure 7.5: *Mode B steady state currents and overall chain-link voltage waveforms*

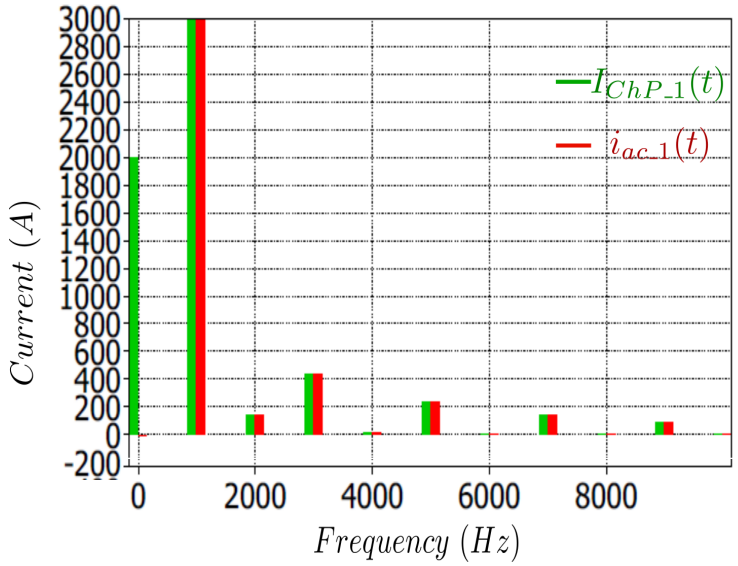


Figure 7.6: *Mode B: FFT of chain-link and tank currents*

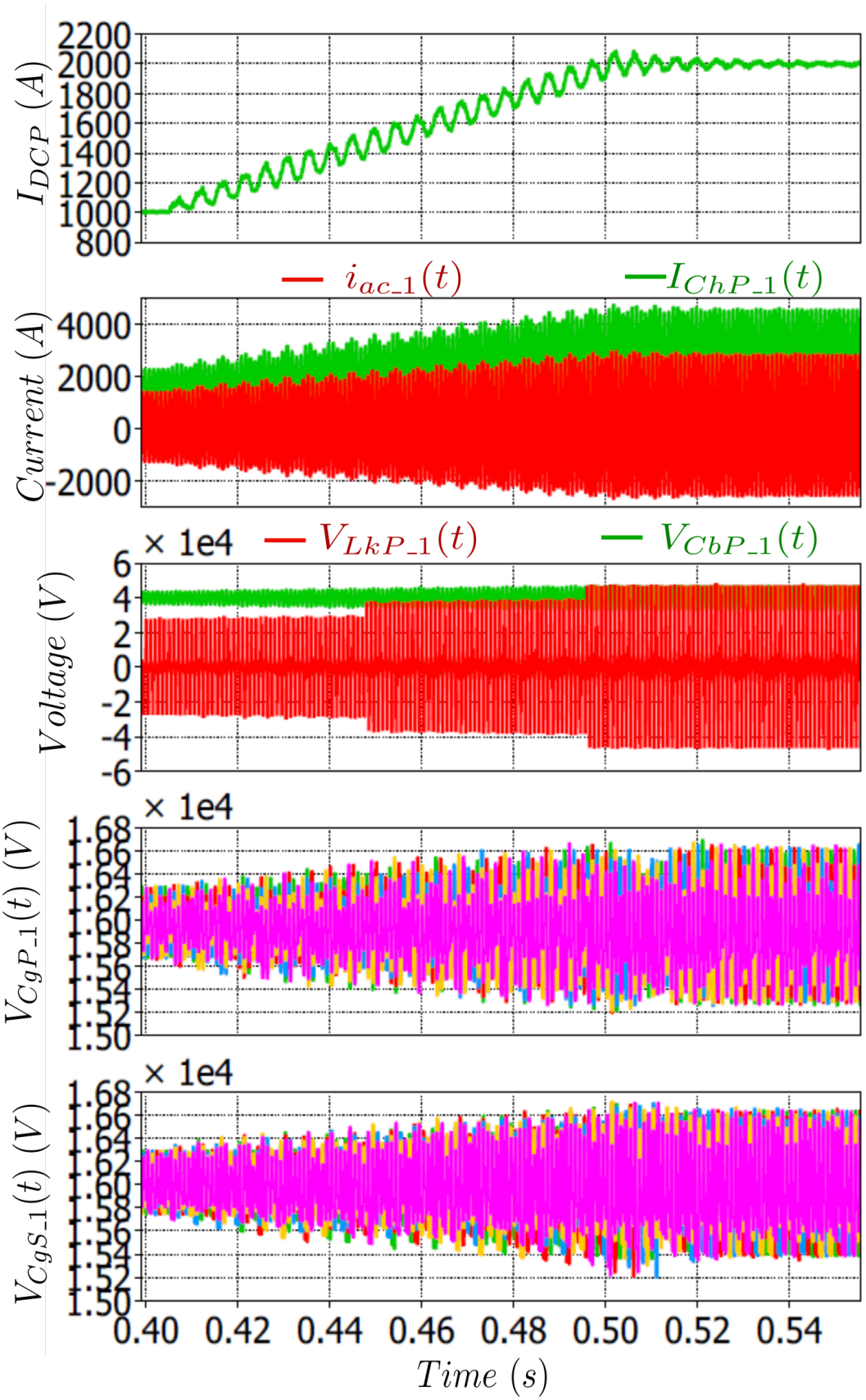


Figure 7.7: *TrSCC-DC-DC mode B response under 50% of power change*

7.2.3 Mode C simulation results

Figure 7.8 shows the phase 1 primary and secondary voltage waveforms, $V_{ChP\_1}(t)$ and $V_{ChS\_1}(t)$, primary inductor voltage and blocking capacitor voltage waveforms, $V_{LkP\_1}(t)$ and $V_{CbP\_1}(t)$, primary and secondary SM voltages per voltage level waveforms, $V_{CgP\_1}(t)$ and $V_{CgS\_1}(t)$ for steady state operation in mode C. It can be observed that C_{bP_1} blocks the DC voltage of the chain-link and the SMs peak to peak voltage ripple is $\delta_{pp} = 5\%$ which verifies the design calculations.

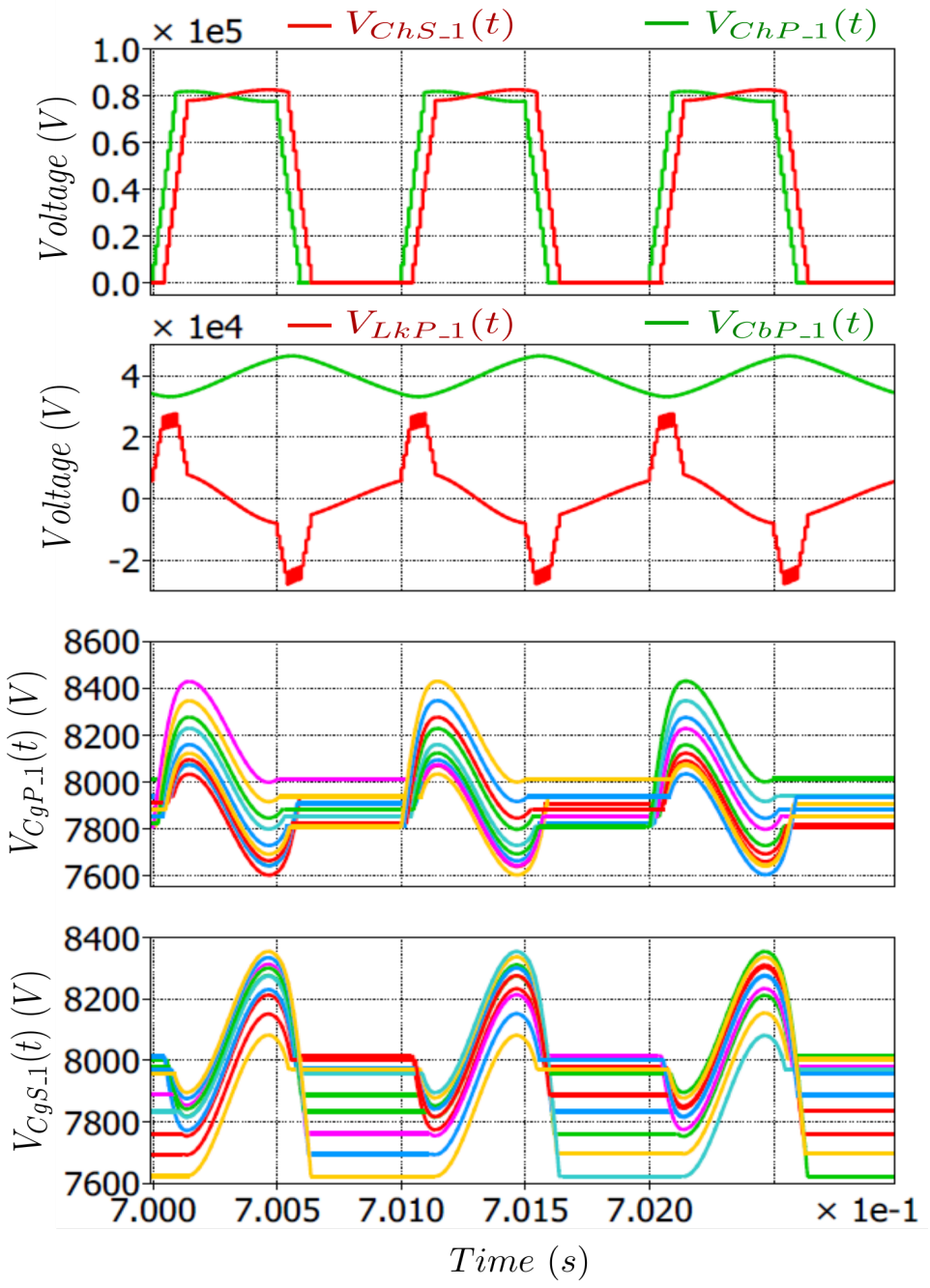


Figure 7.8: *Mode C steady state voltage waveforms*

The overall chain-link voltage waveform, $\sum_{i=1}^{10} V_{ChP\_i}(t)$, instantaneous primary chain-link current waveform, $I_{ChP\_1}(t)$, tank AC current wavefrom, $i_{ac\_1}(t)$, and primary DC current waveform, I_{DCP}, are shown in figure 7.9. Similarly to mode B, $i_{ac\_1}(t)$ is slightly asymmetrical about the x-axis with approximately 5% difference between the positive peak and negative peak values. This is again due to the chain-link voltage ripple (SMs capacitor voltage ripple) which introduces a second harmonic in the $i_{ac\_1}(t)$. Similar to mode B the circuit configuration of the TrSCC-DC-DC, mode C, approximately cancels the second harmonic in the overall chain-link voltage as shown in figure 7.9 where only harmonic $N_{phase} * f_o = 10 * f_o$ can be seen but its value is very small ($< 0.1\%$). As a result, the ripple in I_{DCP} is negligible even with a very low DC inductance value ($L_{dcP} = 1mH$).

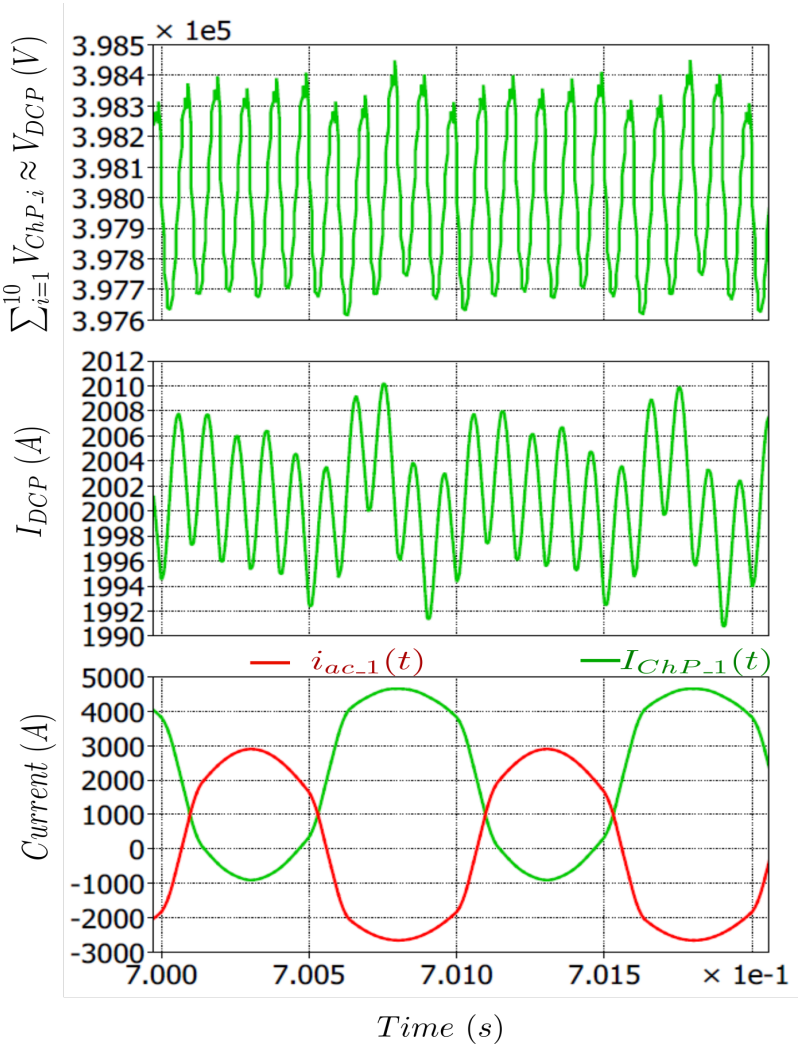


Figure 7.9: *Mode C steady state currents and overall chain-link voltage waveforms*

Figure 7.10 shows transient waveforms when the power flow is changed smoothly from 400MW to 800MW where only power flow control applied with the SM capacitor voltage balancing method method introduced in 4-section 4.3. Similar to mode B the SM capacitor voltage ripple remains within the acceptable limits, $\delta_{pp} \leq 5\%$ and the current waveforms increase smoothly even at the low DC inductance value.

The difference between mode B and mode C are the energy storage requirements, H_{cTrSCC}, and the voltage across the tank inductor. Mode B provides approximately 12.1% reduction in energy storage requirements in comparison to mode C. However, the peak voltage across the tank inductor in mode C is roughly half of the peak voltage across the tank inductor in mode B.

7.3 Comparison

This section focuses on the comparison of the TrSCC-DC-DC operating modes in terms of number of phases, $\frac{dv}{dt}$ stress, DC voltage ripple and DC current ripple. Ultimately, it shows the comprehensive comparison between all of the considered topologies. For comparison purposes, an HVDC system with similar parameters to those considered previously, $V_{DCP} = V_{DCS} = 400kV$ and $P_r = 800MW$, are assumed.

Referring to figure 6.4, theoretically, there is no difference between mode A and mode B in the TrSCCC-DC-DC in terms of energy storage requirements, semiconductor losses and device current rating. However, when the peak to peak voltage ripple, $\delta_{pp} = 5\%$, for SM capacitor voltage is considered, then the instantaneous overall chain-link voltage ripple (i.e. the ripple of the DC voltage) will change according to the mode. Equation 7.1 gives the peak amplitude and the frequency of the DC voltage ripple, $\hat{Vr_{DCx}}$ and Hr_{or}, for mode A. Due to the existence of the second harmonic, the ripple in the DC voltage is noticeable. Equation 7.2 gives Hr_{or} for mode B where $\hat{Vr_{DCx}}$ depends on the number of phases. Operation in this

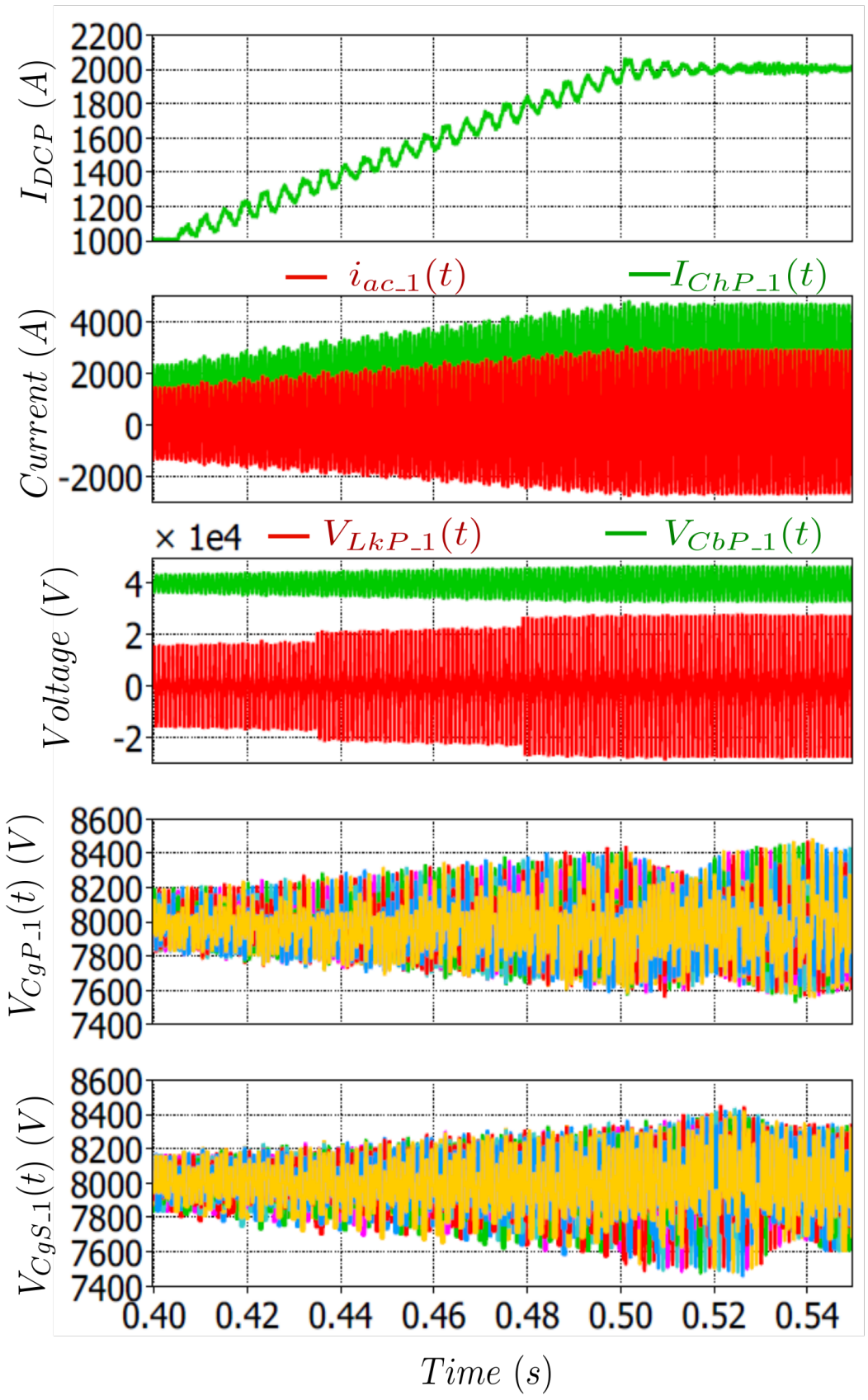


Figure 7.10: *TrSCC-DC-DC mode C response under 50% of power change*

mode leads to harmonic cancellation according to the number of phases. For instance when $N_{phase} = 8$, the 8^{th} harmonic will be the first to appear in $\hat{Vr_{DCx}}$ and hence the ripple in the DC voltage is negligible as is the ripple seen in the DC current. Consequently, mode B is better than mode A when $N_{phase} > 2$ particularly for HVDC systems with low DC inductance, L_{DCx}, since additional DC filtering could be required in case of mode A and eventually the energy storage requirements of the converter will be increased. As a result, N_{phase} can have indirect impact on the energy storage requirements for modes A and B. However in the case when the DC inductance is sufficient to smooth the DC current ripple caused by $\delta_{pp}V_{DCx}$, the impact of N_{phase} is confined to the $\frac{dv}{dt}$ stress across the transformer. As the number of N_{phase} increases, the $\frac{dv}{dt}$ stress will be reduced if the T_t and T_d are fixed.

$$\begin{aligned} \hat{Vr_{DCx}} &\approx \frac{\delta_{pp}V_{DCx}}{2} \\ Hr_{orA} &= 2f_o \end{aligned} \tag{7.1}$$

$$Hr_{orB} = N_{phase}f_o \tag{7.2}$$

Regarding the mode C shown previously in figure 6.4, N_{phase} directly influences the energy storage requirements, semiconductor losses, devices current rating and $\frac{dv}{dt}$ stress across the transformer. The reason is mainly due to the transition period in mode C which is dependent on the number of phases, $T_t = \frac{T}{N_{phase}}$. With small N_{phase} the converter will require excessive energy storage due to the SM capacitors and tank energy, H_{cTrSCC}, high current rating for the semiconductor devices and tank components and accordingly, the semiconductor power losses will be very high. In case of high number of phases, $N_{phase} \gtrapprox 20$, then the energy storage requirements, semiconductor losses, devices current rating and $\frac{dv}{dt}$ stress across the transformer will be approximately the same as mode B. Additionally, the ripple in the DC voltage of the TrSCC-DC-DC with mode C is similar to mode B where the ripple frequency depends on the number of phases, $Hr_{orC} = N_{phases}f_o$.

Regarding the $\frac{dv}{dt}$ stress across the transformer, there is flexibility to limit the $\frac{dv}{dt}$ stress in the TrSCC-DC-DC modes A and B even at high f_o and low T_t by increasing the number of phases, N_{phases}. Table 7.2 shows the $\frac{dv}{dt}$ for modes A and B at different N_{phase}, f_o, fixed $T_d = 10\mu s$ and fixed $T_t = (T/20 - T_d)$ where N_L is the number of SMs per voltage level. It can be seen that even at $f_o = 1kHz$ a lower $\frac{dv}{dt}$ stress is achieved, $\frac{dv}{dt} = 8kV$, when $N_{phase} = 20$ in comparison to the operation with $f_o = 250Hz$ and $N_{phase} = 4$.

Table 7.2: $\frac{dv}{dt}$ at $T_d = 10\mu s$, $T_t = (T/20 - T_d)$ and different f_o and N_{phase}

N_{phase}	$f_o = 250Hz$		$f_o = 500Hz$		$f_o = 1kHz$	
	$\frac{dv}{dt}$	N_L	$\frac{dv}{dt}$	N_L	$\frac{dv}{dt}$	N_L
2	20kV	10	40kV	20	80kV	40
4	10kV	5	20kV	10	40kV	20
10	4kV	2	8kV	4	16kV	8
20	2kV	1	4kV	2	8kV	4

Table 7.3 shows the $\frac{dv}{dt}$ for mode C at different N_{phase}, f_o, fixed $T_d = 10\mu s$. It can be demonstrated that the $\frac{dv}{dt}$ stress always remains lower in comparison to the other modes since even at high $f_o = 1kHz$ and low $N_{phase} = 4$, the $\frac{dv}{dt} = 8kV$. However, it can be also observed that T_t increases as f_o and N_{phase} are reduced and this causes a highly negative impact on the energy storage requirement, H_{cTrSCC}, semiconductor power losses, T_L and semiconductor device current rating, VA_{cTrSCC}.

Table 7.3: $\frac{dv}{dt}$ at $T_d = 10\mu s$, $T_t = (T/N_{phase} - T_d)$ and different f_o and N_{phase}

N_{phase}	$f_o = 250Hz$			$f_o = 500Hz$			$f_o = 1kHz$		
	$\frac{dv}{dt}$	N_L	$T_t = (T/N_{phase} - T_d)$	$\frac{dv}{dt}$	N_L	$T_t = (T/N_{phase} - T_d)$	$\frac{dv}{dt}$	N_L	$T_t = (T/N_{phase} - T_d)$
4	2kV	1	990µs	4kV	2	490µs	8kV	4	240µs
10	2kV	1	390µs	4kV	2	190µs	8kV	4	90µs
20	2kV	1	190µs	4kV	2	90µs	8kV	4	40µs

Table 7.4 gives the parameters of an HVDC system and an associated TrSCC-DC-DC converter where an HVDC system with similar parameters, V_{DCx}, P_r, V_{SM}, considered for previous topologies (TrMMC-DC-DC and MTrMMC-DC-DC) are used and other parameters are chosen according the optimum operating region of the

TrSCC-DC-DC discussed in section 6.4. Table 7.5 shows the difference between TrSCC-DC-DC operation in modes B and C in terms of H_{cTrSCC}, T_L, VA_{cTrSCC} and $\frac{dv}{dt}$, considering the assumed HVDC system. It is clear that, mode B provides better performance than mode C in all aspects apart from $\frac{dv}{dt}$ stress. As N_{phase} is increased the performance of both modes converges with similar performance obtained when $N_{phase} \gtrapprox 20$ or when the same T_t is used for both modes as shown in table 7.5.

Table 7.4: HVDC system specification and parameters of TrSCC-DC-DC

Parameters	Value
$V_{DCP} = V_{DCS}$	400kV
P_r	800MW
V_{SM}	2kV
N_{SM} *Per Chain-Link*	$\frac{2V_{DCx}}{N_{phase} * V_{SM}}$
δ_{pp}	5%
T_d	10µs
$\varphi(T_{sh})$	0.1π
K_f	1.5

Table 7.5: TrSCC-DC-DC operating modes B & C requirements

Requirements	$N_{phase} = 10$				$N_{phase} = 20$			
	$Mode - B$		$Mode - C$		$Mode - B$		$Mode - C$	
	$f_o = 500Hz$	$f_o = 1kHz$	$f_o = 500Hz$	$f_o = 1kHz$	$f_o = 500Hz$	$f_o = 1kHz$	$f_o = 500Hz$	$f_o = 1kHz$
$H_{cTrSCC}(ms)$	9.8	4.9	11.16	5.58	9.8	4.9	9.8	4.9
Si_{cTrSCC}	9.231	9.23	9.41	9.39	9.231	9.23	9.231	9.23
$\frac{dv}{dt}$	8kV	16kV	4kV	8kV	4kV	8kV	4kV	8kV
N_L	4	8	2	4	2	4	2	4
T_t	T/20-T_d(90µs)	T/20-T_d(40µs)	T/10-T_d(190µs)	T/10-T_d(90µs)	T/20-T_d(90µs)	T/20-T_d(40µs)	T/20-T_d(90µs)	T/20-T_d(40µs)

Taking the optimum operating condition for all the modular multilevel DC-DC converter topologies and modes considered for an HVDC system with $V_{DCx} = 400kV$ and $P_r = 800MW$, the key performance parameters for every topology are summarised in table 7.6. The following observations can be made from the table 7.6:

- The high number of SMs, N_{SM_T}, high energy storage requirements, H_c, are the main issues in the sinusoidal MMC-DC-DC even though it is possible to

operate at high peak to peak SM capacitor voltage ripple $\delta_{pp} = 10\%$. High semiconductor power losses, $T_L \approx 1.9\%$, prevents the converter from operating at high frequency.

- The energy storage requirements, H_{cTrMMC}, are significantly reduced in TrMMC-DC-DC mode where 67.4% reduction in the H_{cTrMMC} is achieved in comparison to the sinusoidal mode even if only low $\delta_{pp} \leq 5\%$ is possible. However, the requirement for high sorting frequency during the transition period, $f_{sorting} = 1/(2T_d)$, is a significant issue. Many hundred of SMs have to be sorted and grouped in less than $100(\mu s)$ and this is one of the main challenges for the TrMMC-DC-DC. Additionally, the number of SMs, N_{SM_T}, is high and roughly only 55% of the semiconductor devices are utilised with the remainder only conducting during T_t. In addition to high sorting frequency and semiconductor power losses, high $\frac{dv}{dt}$ stress across the transformer prevents TrMMC-DC-DC operation at high fundamental frequency. Finally, resonance between the equivalent capacitance of the inserted SMs with the stray inductance of the assembling devices can prevent the option of increasing the SM capacitance in order to reduce the sorting frequency.

- The high sorting frequency issue in the TrMMC-DC-DC is solved in the MTrMMC-DC-DC where the SMs are sorted only when all SMs are inserted or bypassed and there is a plenty of time for sorting and grouping to be performed. Additionally, in comparison to the TrMMC-DC-DC, the MTrMMC-DC-DC provides better device utilisation since the arm current is continuous, lower *VA* and lower semiconductor power losses are achieved but the energy storage requirement, $H_{CMTrMMC}$, will be higher by 34.9%. The high $\frac{dv}{dt}$ stress prevents the MTrMMC-DC-DC from operating at higher fundamental frequency. Also a high number of SMs is required in the MTrMCC-DC-DC.

- Sinusoidal operation of the series chain-link modular multilevel DC-DC converter, SCC-DC-DC, was studied in details by the author. The required control loops were developed to ensure the safe operation under different condi-

tions. The operating mode and the developed control loops were validated in [99]. The results show that the number of SMs in the sinusoidal SCC-DC-DC is reduced by 66% and there is no concern about the $\frac{dv}{dt}$ stress. However, a very high energy storage is required in the sinusoidal SCC-DC-DC even though it is possible to operate at high peak to peak SM capacitor voltage ripple $\delta_{pp} = 10\%$. Semiconductor power losses prevent the sinusoidal SCC-DC-DC from operating at higher fundamental frequency in an attempt to overcome the energy storage requirements. Consequently, the auther has considered it only for the comparison purposes in this thesis.

- Operating at high fundamental frequency, $f_o = 1kHz$, low sorting frequency and a high number of phases, $N_{phase} \geq 20$, in the TrSCC-DC-DC can overcome the challenges of high $\frac{dv}{dt}$, achieve lowest energy storage, lowest VA. In addition, a substantial reduction in number of SMs is possible in the TrSCC-DC-DC with 66% reduction achieved in comparison to the sinusoidal MMC-DC-DC, TrMMC-DC-DC and MTrMMC-DC-DC modes.

- The possibility of operating at higher fundamental frequency in the TrSCC-DC-DC reduces the size of the transformer and accordingly increases the power density of the converter. It is recognised that the transformer design may be more challenges at higher frequency but this aspect was not considered further. Detailed work on transformer design left for further work.

In conclusion, the TrSCC-DC-DC converter can be considered as a very attractive for interconnecting HVDC systems. It requires only 33% SMs in comparison to the sinusoidal MMC-DC-DC, TrMMC-DC-DC, MTrMMC-DC-DC modes hence significant simplicity in control structure can be realised and noticeable reduction is achieved in number of sensors, gate drives and isolated DC-DC power supply for gate drives, etc. Furthermore, apart from semiconductor power losses, the TrSCC-DC-DC provides lower energy storage requirement, higher power density, lower VA and lower $\frac{dv}{dt}$.

Table 7.6: Summary of all topologies performances, requirements and characteristics

Requirements & Parameters	MMC-DC-DC	TrMMC-DC-DC	MTrMMC-DC-DC	SCC-DC-DC	TrSCC-DC-DC
f_o	$250Hz$	$250Hz$	$250Hz$	$250Hz$	$1kHz$ ($N_{phase}=20$)
$f_{sorting}$	$10f_o$	$1/(2T_d)$ during T_t	f_o	$10f_o$	f_o
$H_c(ms)$	18.4	6	9.78	25.08	4.9
N_{SM_T}	2400	2400	2400	800	800
VA	12.42	13	10	12.42	9.23
$T_L\%$	1.91	1.42	0.92	1.95	1.64
$\frac{dv}{dt}$	smooth	16kV	16kV	smooth	8kV
N_L	-	8	8	-	4
$\delta_{pp}\%$	10%	5%	10%	10%	5%
$T_d(\mu s)$	-	10	10	-	10
T_t	-	$0.15\pi - T_d$	$0.15\pi - T_d$	-	T/20-T_d(40µs)
Devices Utilisation	✓✓✓	✓	✓✓✓	✓✓✓	✓✓✓
Cooling requirements	✓	✓✓	✓✓✓	✓	✓✓

7.4 TrSCC-DC-DC with high DC voltage gain

In order to interconnect HVDC systems with different voltage levels, MMC-DC-DC structures rely only on transformers to achieve DC voltage gains, $\rho_g = \frac{nV_{DCS}}{V_{DCP}}$. Taking the high power and high voltage systems into account, it could be challenging to build a three phase transformer for DC voltage gain $\rho_g \geq 5$. This can be the case in future DC networks when interconnection between HVDC and MVDC systems are required or in the case of integrating renewable energy systems to HVDC systems. In the case of SCC-DC-DC converters (sinusoidal and trapezoidal modes), high DC voltage gain is achievable with different connections of SCC-DC-DC converter phases using only unity turn ratio transformers. Figure 7.11 shows an example of the TrSCC-Dc-DC system with $\rho_g = 2$ where as depicted the chain-link voltages of the secondary side (lower DC side), V_{ChS_1} and V_{ChS_2}, are out of phase by 180^o.

Furthermore, apart from number of total SMs, all the other theoretical and numerical analysis are still valid and all three TrSCC-DC-DC operating modes are applicable. The number of total SMs, N_{sm_T}, expression can be modified to equation 7.3. Additionally, a combination of both a low transformer turns-ratio and series-parallel connection can be used to achieve very high DC voltage gain, ρ_g, whilst keeping the total number of SMs low. These concepts are validated in a simulation study in next subsection. Experimental results are shown later in chapter 8.6.4.

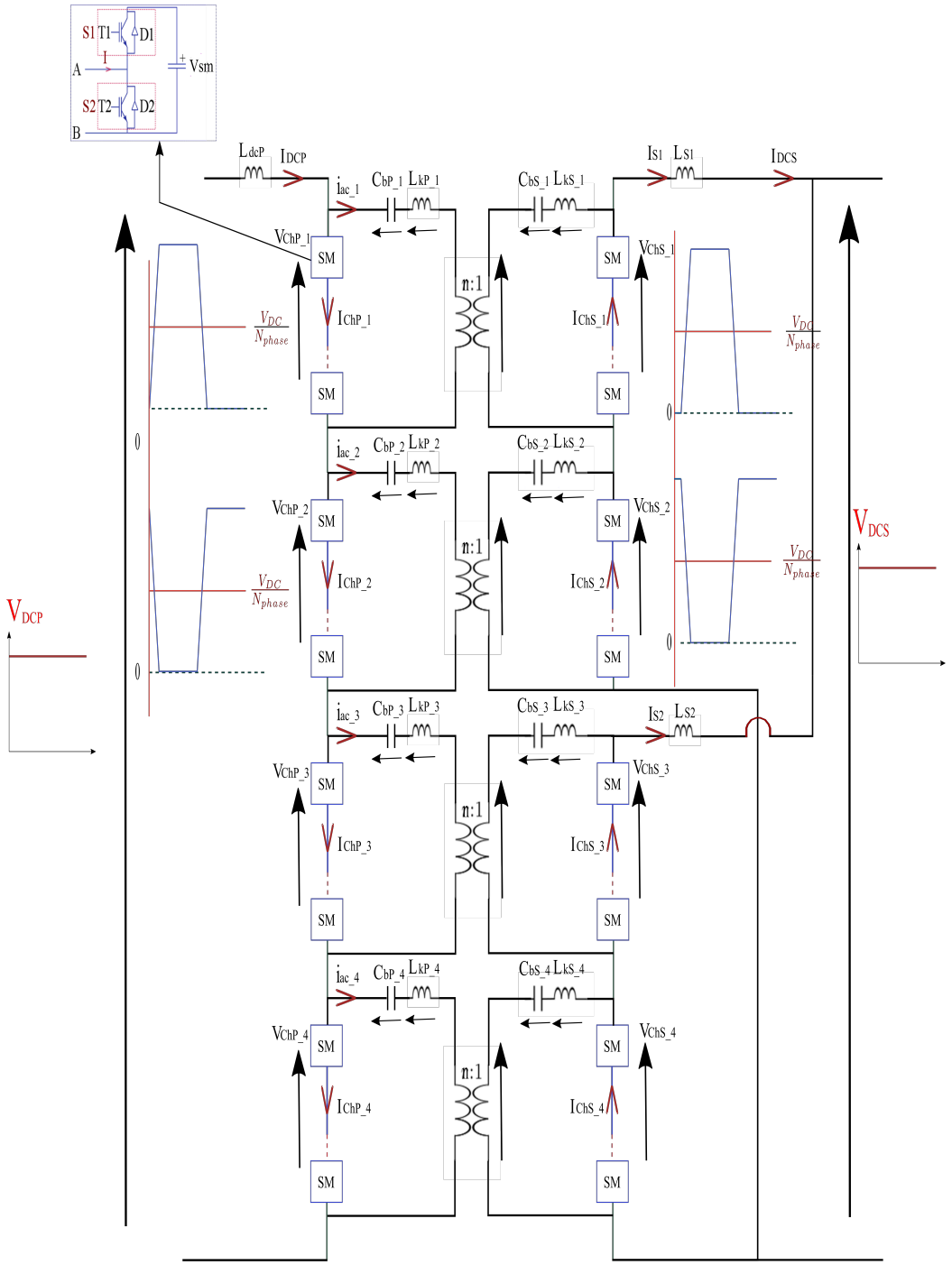


Figure 7.11: *TrSCC-DC-DC configuration for a different DC voltage gain ($\rho_g = 2$)*

$$N_{SMx\_T} = \frac{2 * V_{DCP}}{V_{SMP}} + \frac{\rho_g * 2 * V_{DCS}}{V_{SMS}} \tag{7.3}$$

7.4.1 Mode B simulation results with $\rho_g = 5$

In this sub section, a system with a high DC voltage ratio, $\rho_g = 5$, was simulated in PLECs software to show the effectiveness of the TrSCC-DC-DC topology for HVDC-MVDC interconnection. Table 7.7 shows the system parameters that were used in simulation.

Table 7.7: System specifications and parameters of TrSCC-DC-DC

Parameters	Value
V_{DCP}	400kV ($\pm 200kV$)
V_{DCS}	80kV ($\pm 40kV$)
P_r	800MW
V_{SM}	2kV
f_o	1kHz
N_{phase}	10
ρ_g	5
N_{SM} *Per Chain-Link*	$\frac{2V_{DCx}}{N_{phase}*V_{SM}}$
δ_{pp}	5%
T_d	10μs
K_f	1.5
L_{dcx}	1mH

Figure 7.12 shows key waveforms for the phase 1 $V_{ChP\_1}(t)$, $V_{ChS\_1}(t)$, $V_{LkP\_1}(t)$, $V_{CbP\_1}(t)$, $V_{CgP\_1}(t)$ and $V_{CgS\_1}(t)$ for B operation. It can be noticed that the voltage of the SMs per voltage level of the secondary chain-link, V_{CgS_1}, are greater than the voltage of the SMs per voltage level of the primary chain-link, V_{CgP_1}, accordingly, $\hat{V_{ChS\_1}} > \hat{V_{ChP\_1}}$. The reason behind this is the voltage drop across the inductors, V_{LkS_i}, which is compensated by the chain-link voltage. Referring to figure 7.11, since the secondary chain-link voltages of each leg is 180° out of phase and apart from transition period, T_t, only the SMs of one chain-link are inserted in each leg, a noticeable second harmonic is presented in the overall chain-link voltage in each leg. As a result, a second harmonic component will be produced in the leg current, I_{S_i}, which will cause extra voltage drop across the inductors, L_{kS_i}. Inductors are required to prevent voltage mismatch between the legs due to non ideal components and they are also required to limit the current during a DC fault. The inductors, L_{kS_i}, can be shared between the AC and DC loops in order to prevent high voltage drop across them, achieve voltage matching between legs and limit the current during

fault.

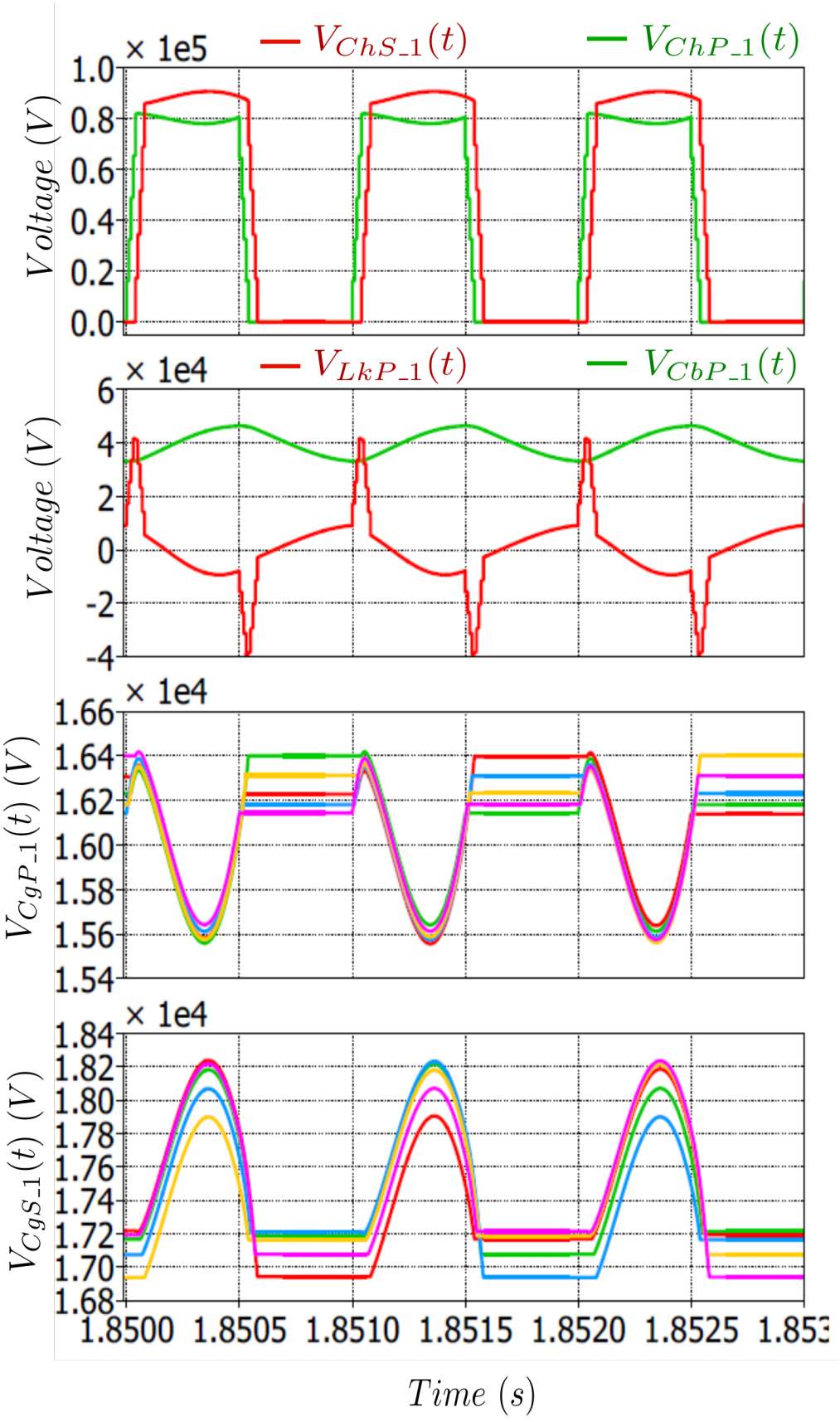


Figure 7.12: *Mode B steady state voltage waveforms with* $\rho_g = 5$

Figure 7.13 shows the secondary DC current, I_{DCS}, and leg currents, I_{S_i}. The second harmonic components can be observed in the leg currents whereas, due to the circuit configuration of mode B, a negligible $N_{phase}f_o = 10f_O$ harmonic can be seen in the DC currents.

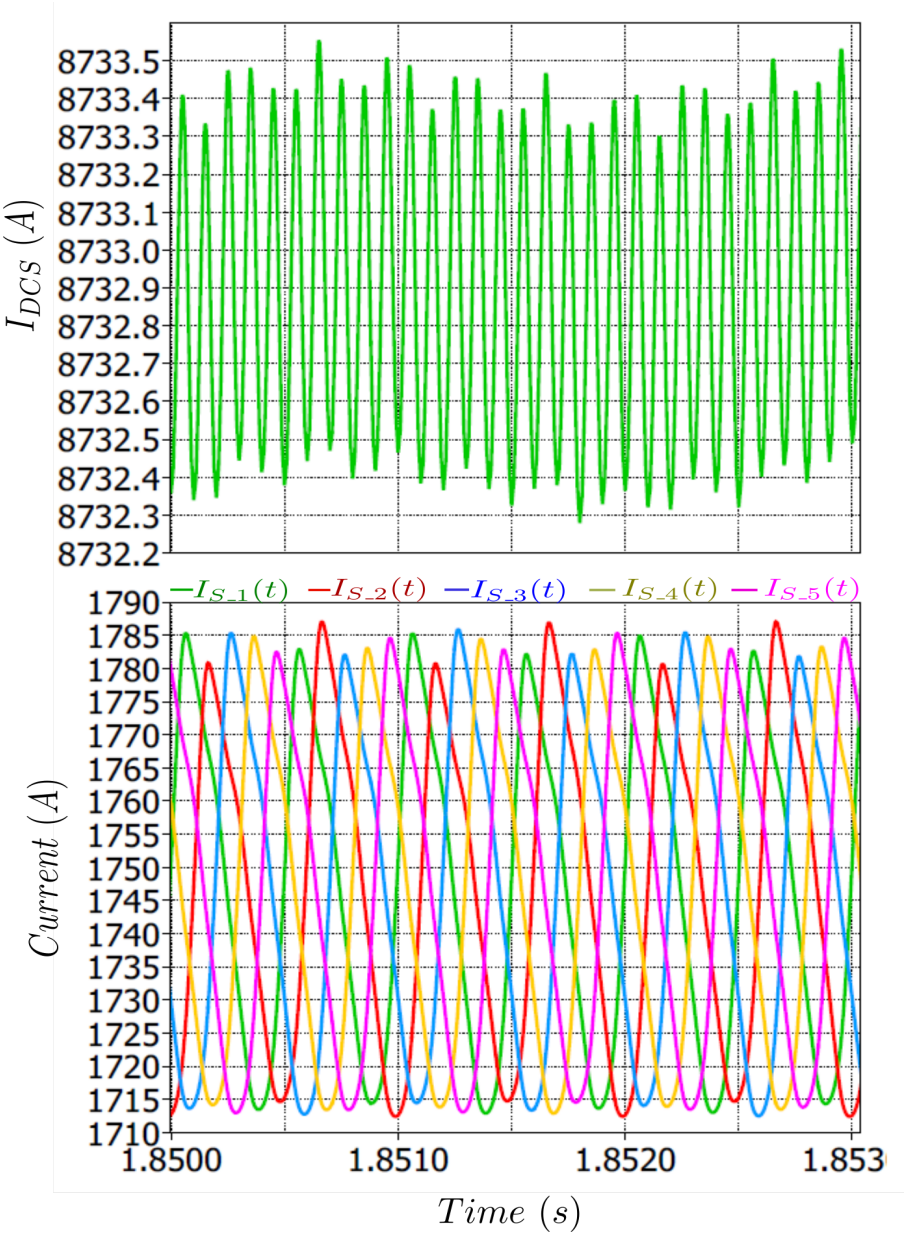


Figure 7.13: *Mode B steady state secondary currents waveforms with* $\rho_g = 5$

Figure 7.14 shows the primary DC current, I_{DCS}, primary and secondary chain-link current, $I_{ChP\_1}(t)$ and $I_{ChS\_1}(t)$, and tank AC link current, $i_{ac\_1}(t)$. The simulation shows the effectiveness of the TrSCC-DC-DC converter for achieving high DC voltage gain using transformers with unity turns-ratio.

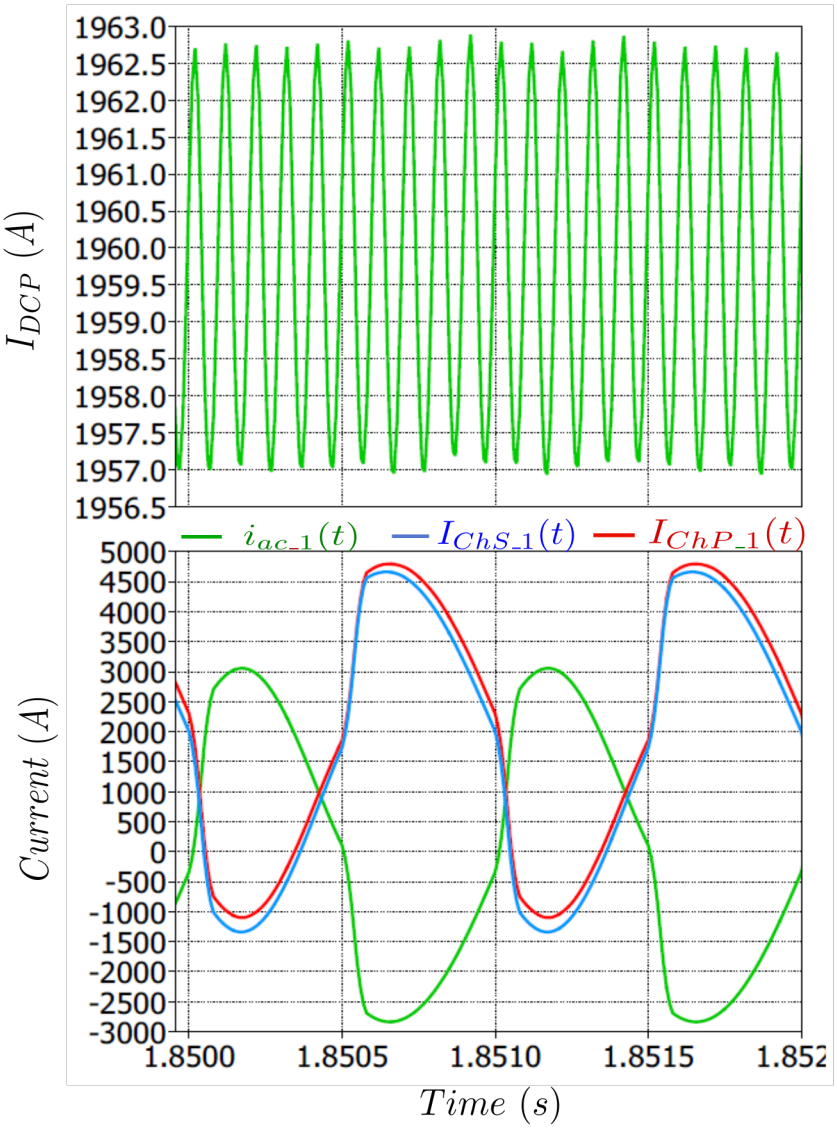


Figure 7.14: *Mode B steady state currents waveforms with* $\rho_g = 5$

7.5 TrSCC-DC-DC DC fault Performance

DC fault protection of the TrSCC-DC-DC is addressed in this section. Similar to DC fault protection study of the TrMMC-DC-DC and the MTrMMC-DC-DC shown in chapter 4-section 5.2.4-table 5.8, the CIGRE test system DC cable parameters have been considered to show the performance of the TrSCC-DC-DC with a DC fault. When a DC fault is detected all SMs of both the primary and secondary chain-links will be gradually (during T_t) set into the idle state where both IGBT devices of SMs will be turned off. The devices will experience higher current as the location of the fault moves closer to the converter station due to the reduction in the DC cable inductance.

Figure 7.15 shows the TrSCC-DC-DC converter under a DC fault at the primary side of the converter where L_m, R_m and C_m are the DC cable parameters. A close fault location, $3km$, from the converter station was chosen.

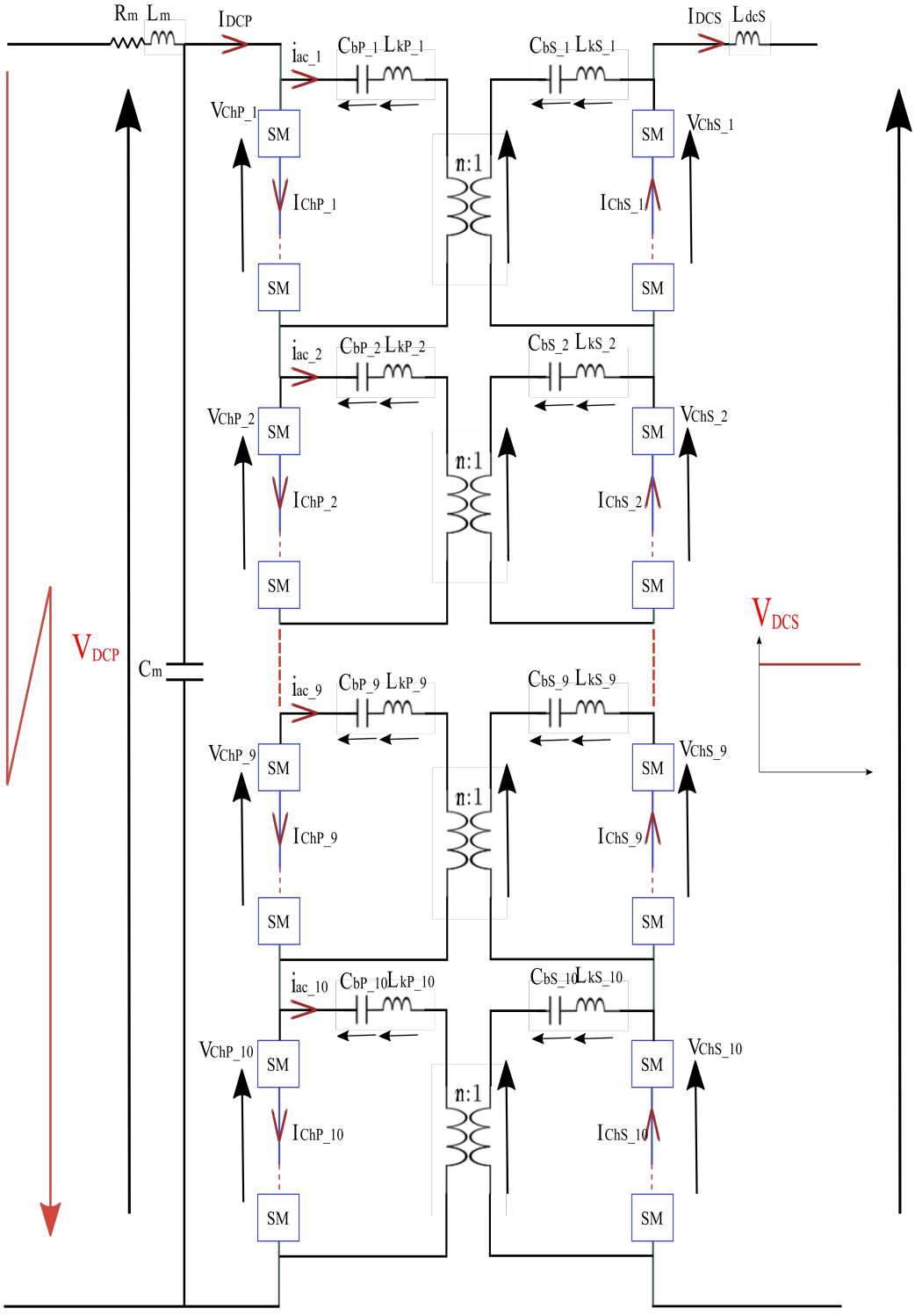


Figure 7.15: *TrSCC-DC-DC mode B with a primary DC fault event*

Figure 7.16 shows the voltage and current waveforms of the TrSCC-DC-DC, mode B, when a DC fault is detected at the primary side of the converter. It can be seen that the maximum faulty side chain-link current, $I_{ChP\_1}(t)$, (free wheeling diode current) reaches approximately 1.3 higher than the nominal maximum chain-link current during the fault instant and this is mainly due the discharge of DC blocking capacitor voltage. Figure 7.16 also shows that the secondary chain-link currents of the non-faulty side will smoothly reach zero and the SM capacitor voltage will ideally remain at their value when both IGBTs are turned off. The DC fault blocking capability of the TrSCC-DC-DC, mode A, is better than the TrSCC-DC-DC mode B due to the bulky DC inductor which is required in mode A. In mode C, however, in the case of a small number of phases, the devices will experience higher current stress due to the chain-link voltage waveforms which have a long T_t hence the requirement of the current for delivering the same power will increase. Additionally, in mode C, when a DC fault is detected, the SMs will be gradually set into the idle state during T_t which is usually long in case of a low number of phases and this could cause problems to discharge/charge the SM capacitor voltages.

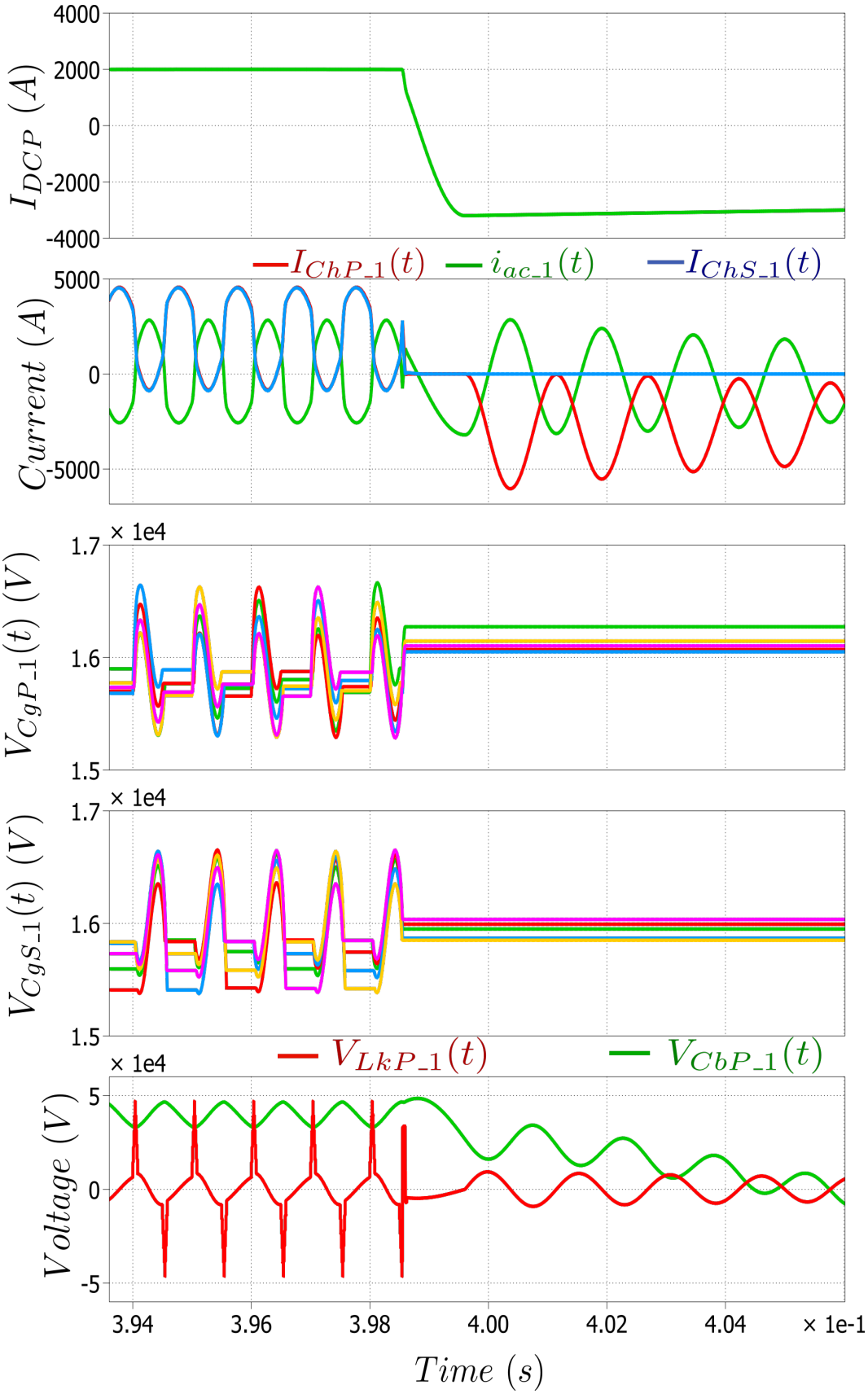


Figure 7.16: *TrSCC-DC-DC mode B waveforms with a primary DC fault event*

7.6 Summary

This chapter validated the TrSCC-DC-DC operating modes and theoretical analysis through simulation where HVDC systems with the TrSCC-DC-DC converter were simulated in PLECS software. The simulation results showed the effectiveness of all operating modes, considering, steady state conditions, transient conditions with the total AC power flow control and DC fault conditions.

A comprehensive comparison between the TrSCC-DC-DC modes was also presented showing that all three modes provide promising performance when a high number of phases and $N_{phases} \gtrapprox 20$, a high DC link inductance (for mode A) are considered. However, mode B was found to be the most promising one since it provides lowest energy storage requirements with a low number of phases in comparison to mode C. In comparison to mode A, mode B provides harmonic cancellation in the overall chain-link voltage, $\sum_{i=1}^{N_{phase}} V_{ChP\_i}(t)$, where only harmonic $N_{phase} * f_o$ appears in mode B whereas in mode A harmonic $2 * f_o$ appears.

In comparison to the TrMMC-DC-DC and the MTrMMC-DC-DC, operation at high fundamental frequency was achieved in the TrSCC-DC-DC with lower $\frac{dv}{dt}$ stress across the transformers, lower number of SM, lower energy storage requirements, and lower device *VA* requirements. The TrSCC-DC-DC has 66% reduction in number of the SMs, 50% reduction in transformer $\frac{dv}{dt}$ stress, approximately 29.2% and 26.5% reduction in *VA* semiconductor requirements in comparison to the TrMMC-DC-DC and the MTrMMC-DC-DC, respectively, approximately 19.5% and 50% reduction in energy storage requirement in comparison to the TrMMC-DC-DC and the MTrMMC-DC-DC, respectively. A higher power density when it is operated at $f_o = 1kHz$ and $N_{phase} = 20$, considering the same T_d between voltage level transitions.

This chapter briefly discussed the possibilities of achieving high DC voltage gain with the TrSCC-DC-DC topology using unity ratio transformers. A system with a

high DC voltage gain, $\rho_g = 5$, was simulated in PLECS software and the simulation results showed the effectiveness of the proposed topology.

Finally, since the theoretical analysis and simulation results showed the effectiveness of the TrSCC-DC-DC modes to provide the main aims of this research, namely low number of SMs, low $\frac{dv}{dt}$ stress, low semiconductor *VA* requirements, high power density and low energy storage requirements, a small scale prototype with was developed in the lab to validate the TrSCC-DC-DC modes practically. The next chapter will briefly explain the prototype rig and present the experimental results which demonstrate the practical validation of the MTrMMC-DC-DC and TrSCC-DC-DC configuration concepts.

Chapter 8

Experimental Results

8.1 Introduction

The experimental validation of the work presented in the previous chapters is crucial to ensure that the novel modular multilevel DC-DC converter operates as expected, practically. In general, laboratory prototypes of HVDC circuits are scaled down to facilitate the test at lower voltages, as a result of the significant costs and safety considerations required when constructing at high voltage. Testing at low voltage means a reduction in the number of the series-connected SMs without compromising the quality of the results and their validity as practical verification of the desired converter operation.

The main parts of the experimental rig, the scaled-down SMs and the control platforms, used for this work, were designed and constructed by Dr. Francesco Tardelli and Dr. Alessandro Costabeber at the University of Nottingham for a three-phase, 50 Hz, 4.5 kW, AC/DC conversion demonstrator. The details of the SM design and the control platform choice development were first documented in [100]. The connection of the SMs is flexible so that they can be used to construct various multilevel AC/DC converter circuits for different applications. However, to configure a TrSCC-DC-DC converter circuit, some hardware had to be developed and added to

the rig. These included AC link tank elements (blocking capacitors and tank inductors), single phase medium frequency transformers and additional current sensors.

This chapter provides a brief description of the experimental configuration of the MTrMMC-DC-DC and TrSCC-DC-DC converters. It also presents the experimental results of the TrMMC and TrSCC-DC-DC converters under all three operational modes when $\rho_g = 1$ as well as TrSCC-DC-DC converter operation in mode B with $\rho_g = 2$.

Originally, the aim of the experimental work for this project was to design and construct a new laboratory-scaled prototype converter for the experimental validation of the theoretical and simulation work of the earlier chapters in this thesis. However, as a result of the global COVID-19 pandemic, there was a significant shortage in the availability of some of the required electronic components and limited access to the university laboratories. As a result, the experimental rig introduced in previous chapter, originally designed for operation at 50 Hz as an AC/DC converter was re-configured and used for validating the TrMMC and TrSCC-DC-DC converter control methods. As a result of the reconfiguration of an older hardware prototype, the following points should be considered when reviewing the results for the MTrMMC and TrSCC-DC-DC converter operations:

- The 5.28 mF SM capacitors, were originally designed to achieve 20 % peak to peak voltage ripple at rated power when operating at a fundamental frequency of 50 Hz for AC/DC conversion. Consequently, the voltage ripple across the SM capacitors when tested at 250 Hz for the TrMMC and 500 Hz for the TrSCC-DC-DC converter operation is negligible.

- Each SM capacitor is comprised of 16 capacitors connected in parallel to achieve the required ripple current rating. Resultingly, a total of 384 capacitors are used to form the 24 SMs of the converter. Again, considering the impact of the COVID-19 pandemic, there was insufficient time to replace all

the capacitors and achieve a reasonable voltage ripple across the SM capacitors for the DC-DC converter work.

- The semiconductor devices and SM capacitor current and voltage ratings provide safe operation of the TrMMC and TrSCC-DC-DC converter configurations at up to 3kW

In order to support the results obtained experimentally, a simulation model with the same devices, components, voltage and power ratings as the experimental hardware has been developed in the PLECS simulation software. The results from both simulation and experimental results are described and compared in this chapter. The intentions of the experimental tests performed with the developed laboratory prototype are:

- Practical validation of the operation of a modified trapezoidal waveform for a modular multilevel DC-DC converter, MTrMMC-DC-DC, where the arm currents conduct continuously over a certain range of the resonant frequency between the arm inductor and equivalent inserted SM capacitors, $fr \leq \frac{2f_o}{1.5}$.

- Practical validation of the new capacitor SM voltage balancing method

- Proof of the practical feasibility of the TrSCC-DC-DC converter under all three operational modes

- Practical validation of the high gain operation of the TrSCC-DC-DC converter configurations with a unity transformer turn ratio

In order to meet the requirements of the above points different tests have been performed under various operating conditions, including under steady-state conditions and with system transients.

8.2 Experimental Setup

The experimental rig consists of three converter "stacks" where each stack comprises 8 flexible SMs which can be connected to form the desired number of the converter chain-links according to the required converter configuration. The stack also has a back-plane PCB which connects the 8 SM PCBs to a secondary micro-controller unit, MCU. The SMs are flexibly designed to operate as either a half-bridge or full-bridge. However, since half-bridge SMs are required in all MTrMMC-DC-DC converter and TrSCC-DC-DC converter operational modes the SMs are all configured as half-bridges for this work. Figure 8.1 shows the three SM stacks and the MCUs, which are connected to a central micro-controller unit (primary MCU) via optical fibres.

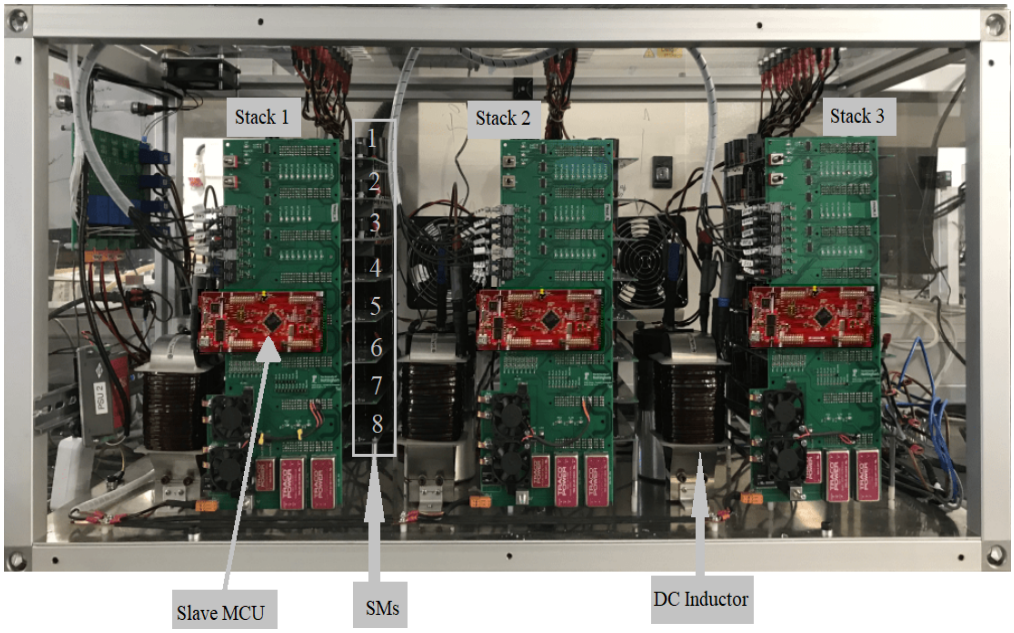


Figure 8.1: *SM stacks*

The MTrMMC-DC-DC and TrSCC-DC-DC converter topologies and their respective control methodologies have been tested using the same power electronics rig. However, other elements, such as the tank inductors, blocking capacitors and AC link transformers, have been added for the TrSCC-DC-DC configuration, as required.

Figure 8.2 shows the MTrMMC converter practical setup where the current transducers seen in each phase are used for over-current protection purposes. The SMs in the stack 1, stack 2 and stack 3 are phase A, phase B and phase C, respectively. SM1-SM4 are the SMs used for the upper arm and SM5-SM8 are used for the lower arm of each phase, respectively. In comparison to the configuration of the MTrMMC-DC-DC converter shown in chapter 4 and considering the practical limitations, only a three-phase primary MMC has been configured, with the secondary side represented by a three-phase AC load which is used to impose the power flow requirements on the AC side of the converter. As a result, the power flows from the DC to the AC side and the converter acts as an inverter. The secondary side MMC and the three-phase AC transformer are not implemented as a result of the limited availability of the SMs.

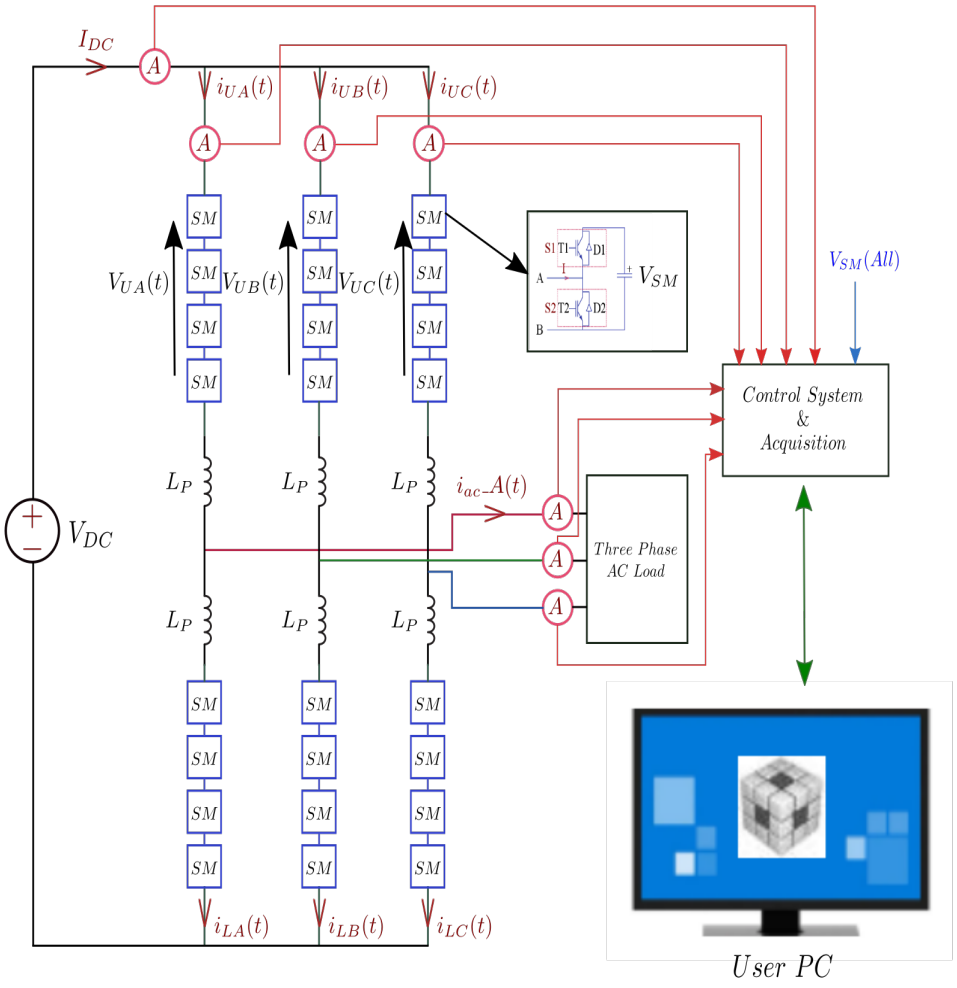


Figure 8.2: *MTrMMC practical setup*

The practical setup of the four phase TrSCC-DC-DC converter is shown in figure 8.3 for operation with a unity DC voltage gain $\rho_g = 1$ and a unity transformer turns-ratio. Figure 8.4 shows the experimental setup of the TrSCC-DC-DC with a DC voltage gain of $\rho_g = 2$ and a unity transformer turns-ratio.

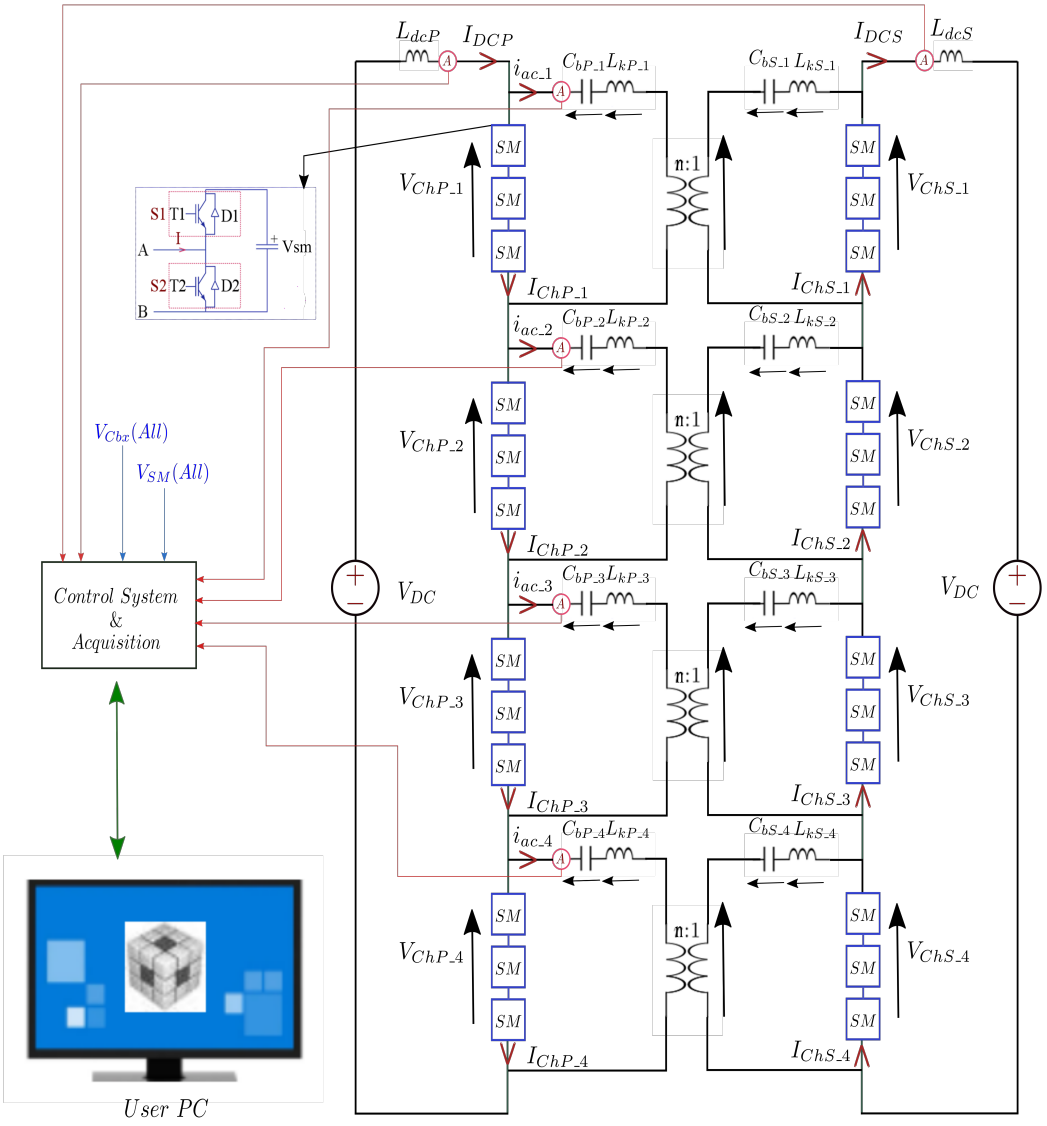


Figure 8.3: *TrSCC-DC-DC practical setup with* $\rho_g = 1$

Each chain-link in the TrSCC-DC-DC converter comprises three SMs as shown in figures 8.3 and 8.4. Table 8.1 shows the configuration of the chain-links taking the SM stacks into account.

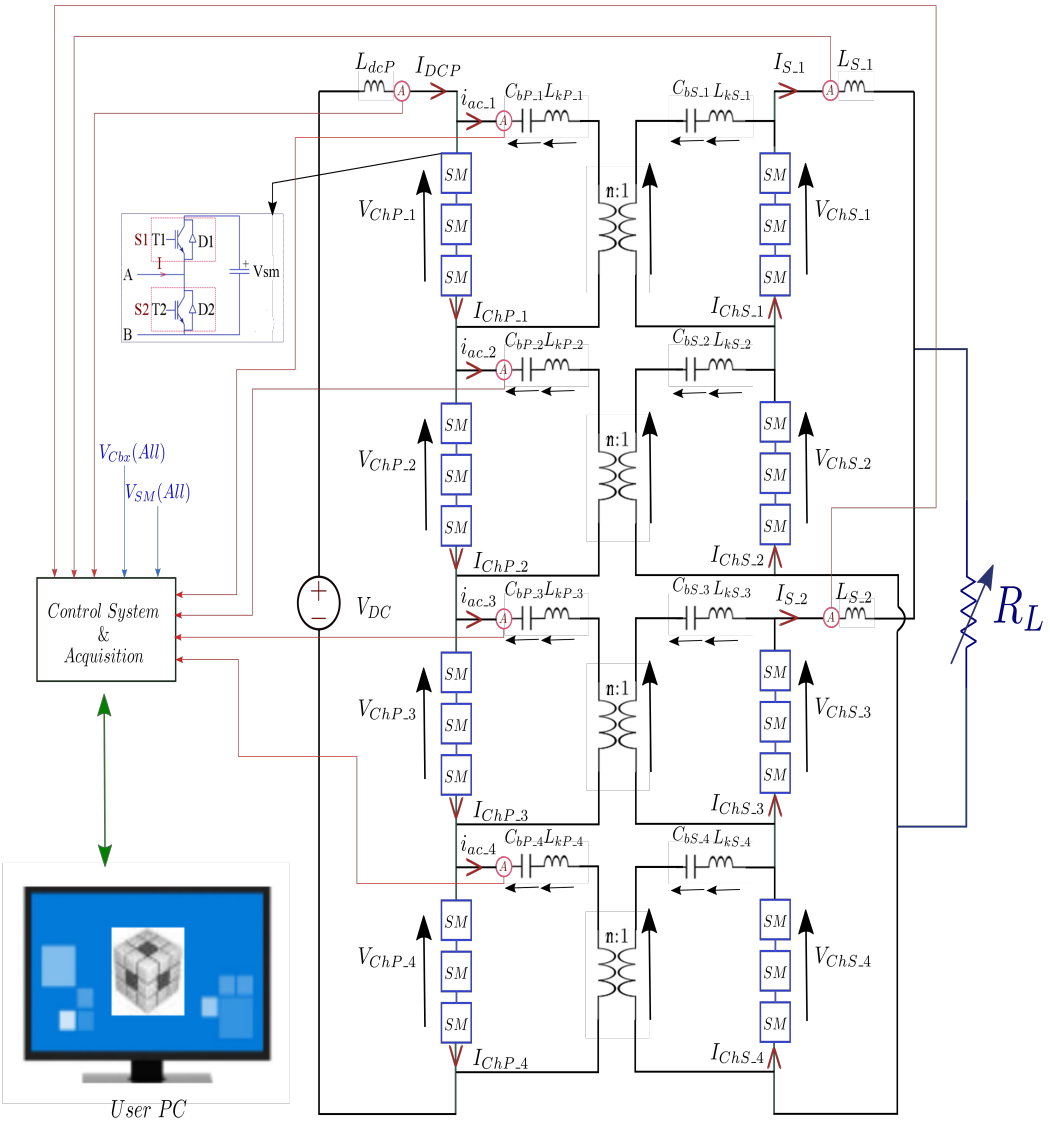


Figure 8.4: *TrSCC-DC-DC practical setup with* $\rho_g = 2$

Table 8.1: TrSCC-DC-DC chain-links configuration

Chain-link	SM #	Stack #
Ch_{P_1}	SM1-SM3	Stack 1
Ch_{S_1}	SM4-SM6	Stack 1
Ch_{P_2}	SM1-SM3	Stack 2
Ch_{S_2}	SM4-SM6	Stack 2
Ch_{P_3}	SM1-SM3	Stack 3
Ch_{S_3}	SM4-SM6	Stack 3
Ch_{P_4}	SM7-SM8 & SM7	Stack 1 & Stack 2
Ch_{S_4}	SM8 & SM7-SM8	Stack 2 & Stack 3

8.3 SM design

The SM is the main component of a modular multilevel converter and figure 8.5 shows the SM PCB used for this work. The SM uses 150V, 100A low on-resistance discrete MOSFET devices (IPB072N15N3). The SM capacitor is implemented using a parallel connection of 16 general purpose electrolytic capacitors, each capacitor is rated at 330µF. The overall capacitance of the SM is 5.28mF. Fans are added to the SM to help cool the MOSFETs when operating the converter. Three isolated DC/DC converters, with an output voltage of $\pm 15V$, are used to supply the onboard gate drivers and a connector interconnects between the SM and the back plane PCB.

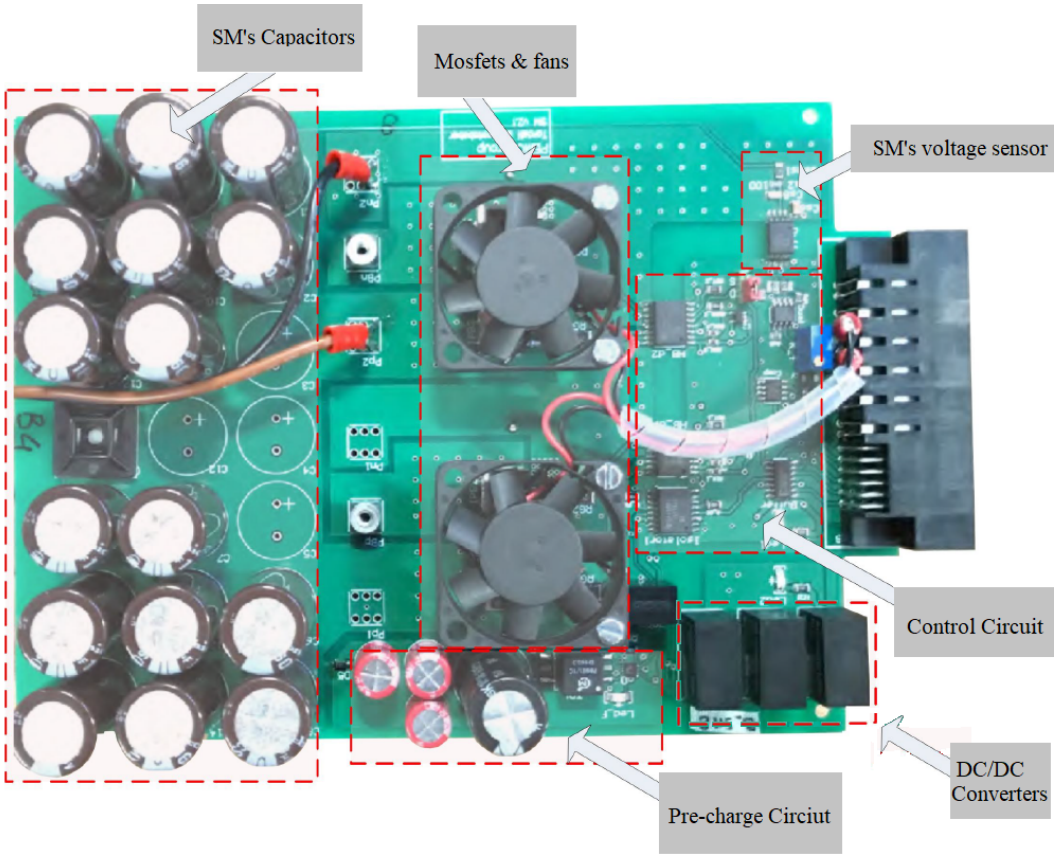


Figure 8.5: *SM PCB*

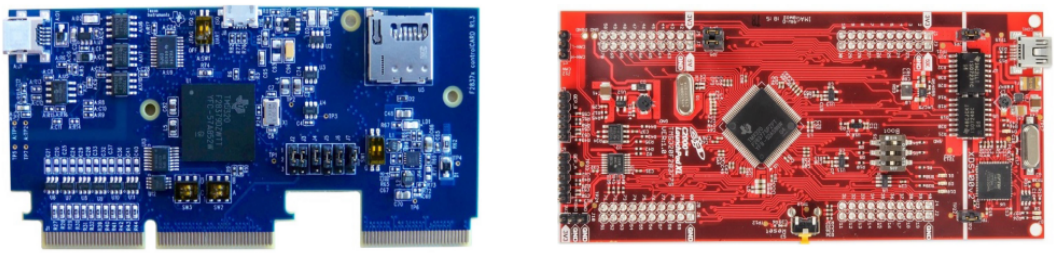
8.4 Control architecture

Low cost micro-controller units are used in the prototype control system. The quantity of the real time measurements, SM capacitor voltages, AC currents, DC currents, etc., are essential to modular multilevel converter operation. In order to be able to have enough analogue to digital converter channels on the control platform, a primary-secondary control structure is used.

A Texas Instruments F28379D MCU and F28377S MCU are employed for primary (central) controller and secondary (local) controllers, respectively. A TMS320F28379D controlCARD development board shown in figure 8.6-a hosts the F28379D MCU and a LAUNCHXL-F28377S LaunchPad development board shown in figure 8.6-b hosts the F28377S MCU. The MCU development boards were chosen to achieve the following features:

- Secondary controller, the F28377S MCU, provides more than the 8 PWM signals required to turn on/off the SM half bridge devices of one stack
- Secondary controller, the F28377S MCU, provides more than the 8 ADC channels required to monitor the SM capacitor voltages of one stack
- Primary controller, the F28379D MCU, provides more than the 15 ADC channels required to monitor the necessary voltages and current quantities according to the topology configuration such as DC blocking capacitor voltages, AC currents, DC currents, arm current and secondary phase currents.
- Compatible communication peripherals for both the primary and secondary controllers to achieve a high speed interface between the two
- Both F28379D MCU and F28377S MCU have a USB JTAG emulator for programming and debugging via a serial connection between a computer (PC) and the MCUs.

Figure 8.7 shows the implementation of the control structure in the practical setup.



(a) (b)

Figure 8.6: *(a) TMS320F28379D MCU controlCARD (b)F28377S MCU LaunchPad*

The primary controller functions vary according to the topology configuration. However, in all configurations the primary controller initiates and finalises the interrupt service routine, ISR, of the secondary controllers. It also provides protection to the converter by handling the over-voltage or over-current trip signals and resetting all of the secondary MCUs in the event of a trip. The functions of the primary MCU can be summarised according to the topology configurations in the following tasks:

- In the MTrMMC converter configuration, the primary MCU receives the measurements of the 3 phase AC currents, 3 upper arm currents and primary DC current from ADCs and uses the information for the protection purposes and imposing power at the AC electronic load

- In the TrSCC-DC-DC converter configurations, the primary MCU receives the measurements of the 4 phase AC currents, DC currents from ADCs and uses them for protection purposes. Additionally, it uses the secondary converter side DC current to implement overall power control by providing the required phase shift, $T_{sh}(\phi)$, to the secondary MCUs through the serial peripheral interface (SPI) ports

- In the TrSCC-DC-DC converter configurations, the primary MCU receives the 6 SM capacitor voltages from phase 4 of the converter secondary controllers, 2 SM capacitor voltages per controller, and the primary MCU interrupt routine sorts the SM voltages and sends the modulation index of phase 4 to the secondary MCUs via the SPI ports

- In the TrSCC-DC-DC converter configuration with $\rho_g = 2$, the primary MCU

receives the all of the SM voltages of the secondary converter side chain-links and implements the SM voltage control by providing the required phase shift, $T_{sh}(\varphi)$, to the secondary MCUs and imposing a DC electronic load.

The secondary controllers receive all SM voltages in each phase stack via its ADCs in all topology configurations and according to the topology configuration it communicates the necessary information with the primary MCU. The main functions of the secondary controller, according to the topology configuration, can be summarised in the following tasks:

- In the MTrMMC converter configuration, each secondary MCU sorts the received upper and lower SM voltages
- In the MTrMMC converter configuration, the modulation signals are provided by the secondary MCU and according to the SMs sorted index, the PWM signals are generated from the modulation signals
- In the TrSCC-DC-DC converter configurations, the secondary MCU sorts the 3 SM voltages of the primary converter chain-link and 3 SM voltages of the secondary converter chain-link, and sends the last 2 used SM numbers to the primary MCU
- In the TrSCC-DC-DC converter configurations, the secondary MCU generates PWM signals according to the SMs sorted index, receives the phase shift, $T_{sh}(\varphi)$, from primary MCU and introduces the phase shift between the primary and secondary converter chain-link modulation signals
- In the TrSCC-DC-DC converter configurations, the secondary MCU receives the modulation signals of phase 4 from the primary MCU via the SPI, the generation of the PWM signals and implementation of the phase shift between primary and secondary converter chain-link modulation signals are performed in the secondary MCU
- In the TrSCC-DC-DC converter configuration with $\rho_g = 2$, the secondary

MCU sends the all SM voltages of the secondary converter chain-links and receives $T_{sh}(\varphi)$ and the modulation signals of the SMs

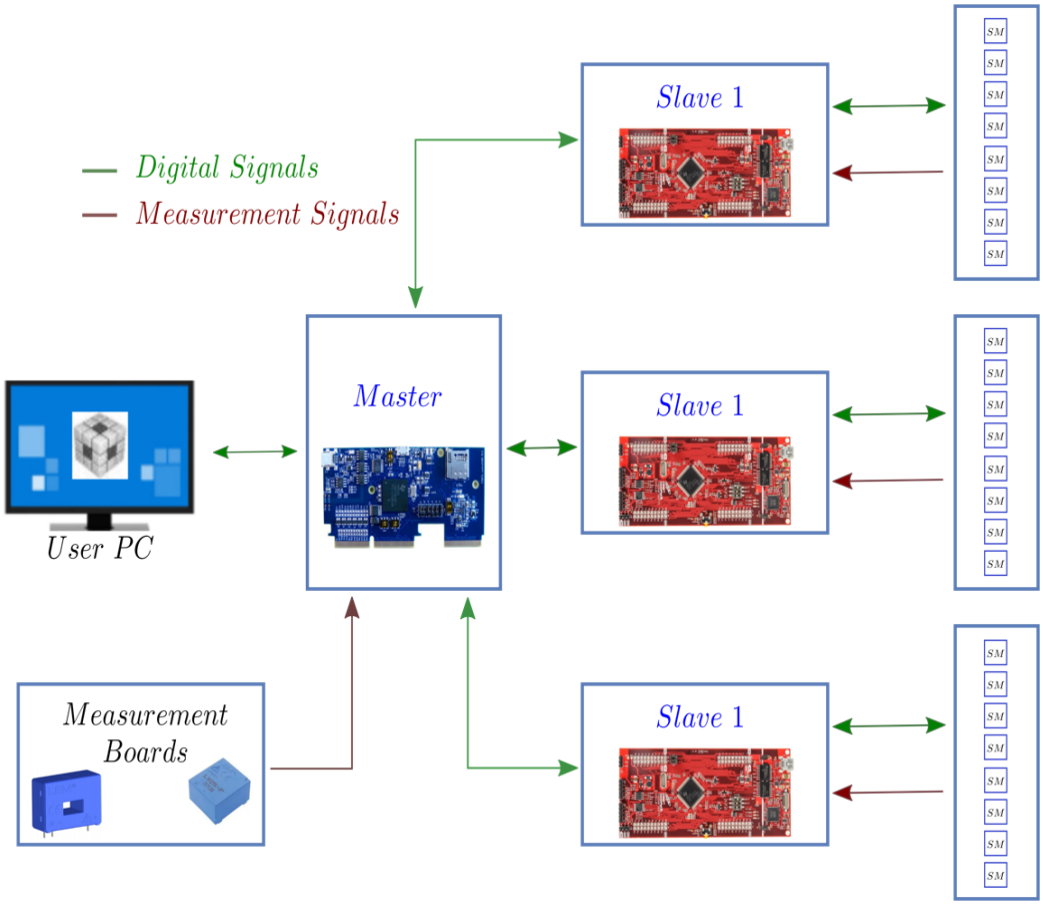


Figure 8.7: *Control architecture*

The details about the voltage sensing circuit of the SM capacitors, gate drives, pre-charge circuit of the SM capacitors, transformer design, selection of the resonant tank components and measurement boards can be found in appendix B.

8.5 Practical results for the MTrMMC converter

Table 8.2 shows the parameters of the experimental setup for the MTrMMC converter. The system is operated at $\approx 2.6\ kW$ for DC-AC conversion with 260 V imposed on the DC side and a three-phase resistive load of 16.2 Ω on the AC side of the converter. Considering the HVDC applications and the work in chapter 4, 250 Hz is chosen for operating frequency with a transition period of $T_t = 0.15\pi = 300\ \mu s$, to insert/bypass all SMs.

Table 8.2: DC-AC MTrMMC system parameters

Parameters	Value
V_{DC}	260 V
Active Power	$\approx 2.6\ kW$
V_{SM}	65 V
C_{SM}	$5.28\ mF$
N_{SM} *Per Chain-Link*	4
N_L	1
f_o	250 Hz
f_r	$\approx 142.5\ Hz$
T_t	$0.15\pi = 300\ \mu s$
T_d	$100\ \mu s$

8.5.1 Steady-state operation

Figure 8.8 shows the practical results of the three phase upper chain-link voltages, $V_{U\phi}(t)$, three phase lower chain-link voltages, $V_{L\phi}(t)$, three phase AC currents, $i_{ac\_\phi}(t)$, upper arm current of phase A, $I_{UA}(t)$, lower arm current of phase A, $I_{UA}(t)$, and the DC current, I_{DC}, where ϕ represents phases A, B, C. Results from simulation for the same operational conditions are depicted in figure 8.9. It can be seen that the practical results match well with those from the simulations.

Practical results for the upper and lower SM voltages are shown in figure 8.10-a and 8.10-b, respectively. Simulation results for the upper and lower SM voltages are shown in figure 8.10-c and 8.10-d, respectively, where it can be seen that the peak to peak voltage ripple on the SM capacitors is almost 0.25 V. This is a result of the high capacitance used in the prototype SMs.

The effectiveness of the proposed balancing method for the SM capacitor voltages, $V_{SM\_U\phi}(t)$ and $V_{SM\_L\phi}(t)$, is shown in figure 8.11 where balancing of the SM voltages is disabled at 0.02s and enabled again at 0.144s. It can be observed that the SM voltages diverge initially and then re-converge when the balancing control is re-enabled.

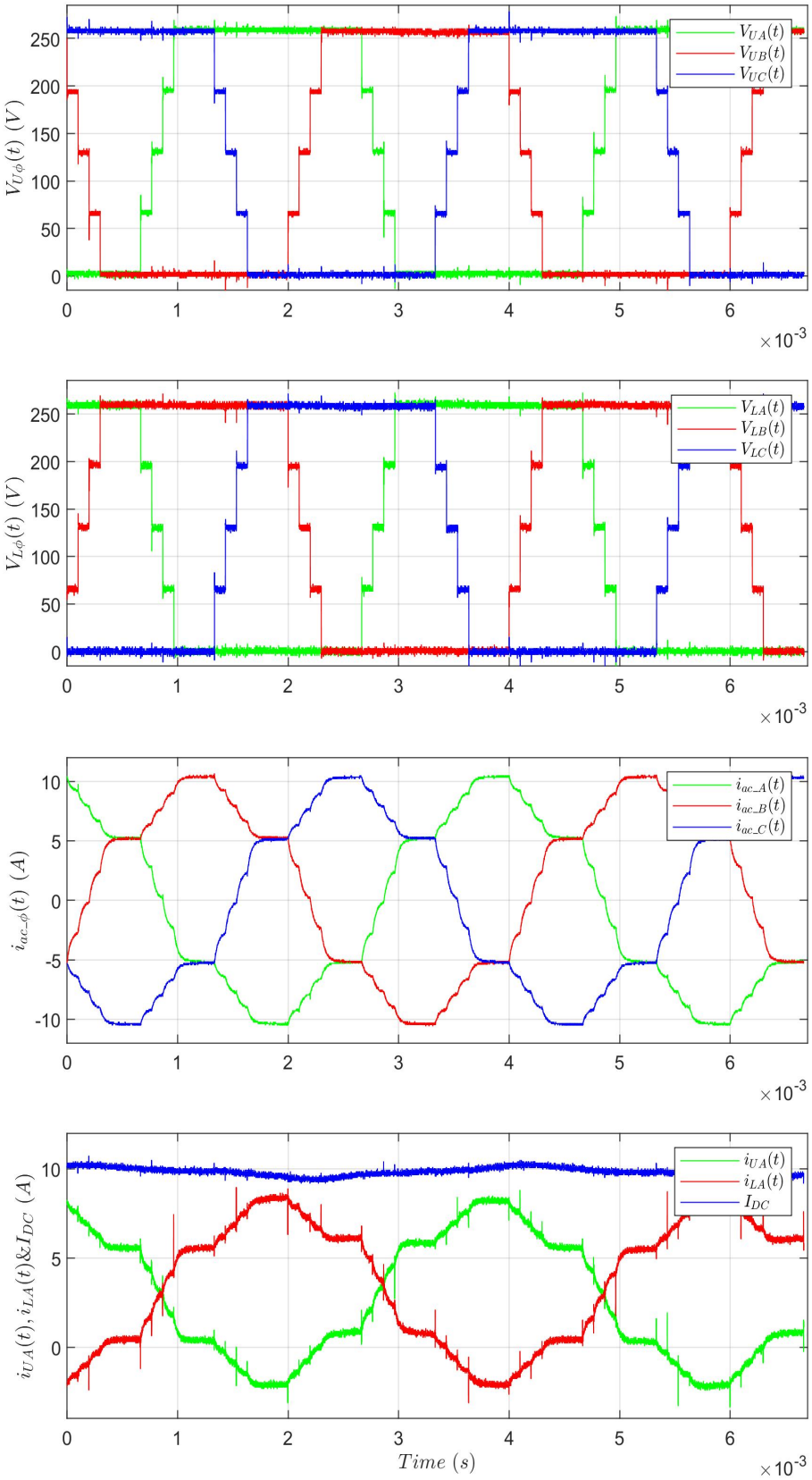


Figure 8.8: *Practical results of MTrMMC upper chain-link voltages, lower chain-link voltages, three phase AC current, phase A upper and lower arm currents and DC current*

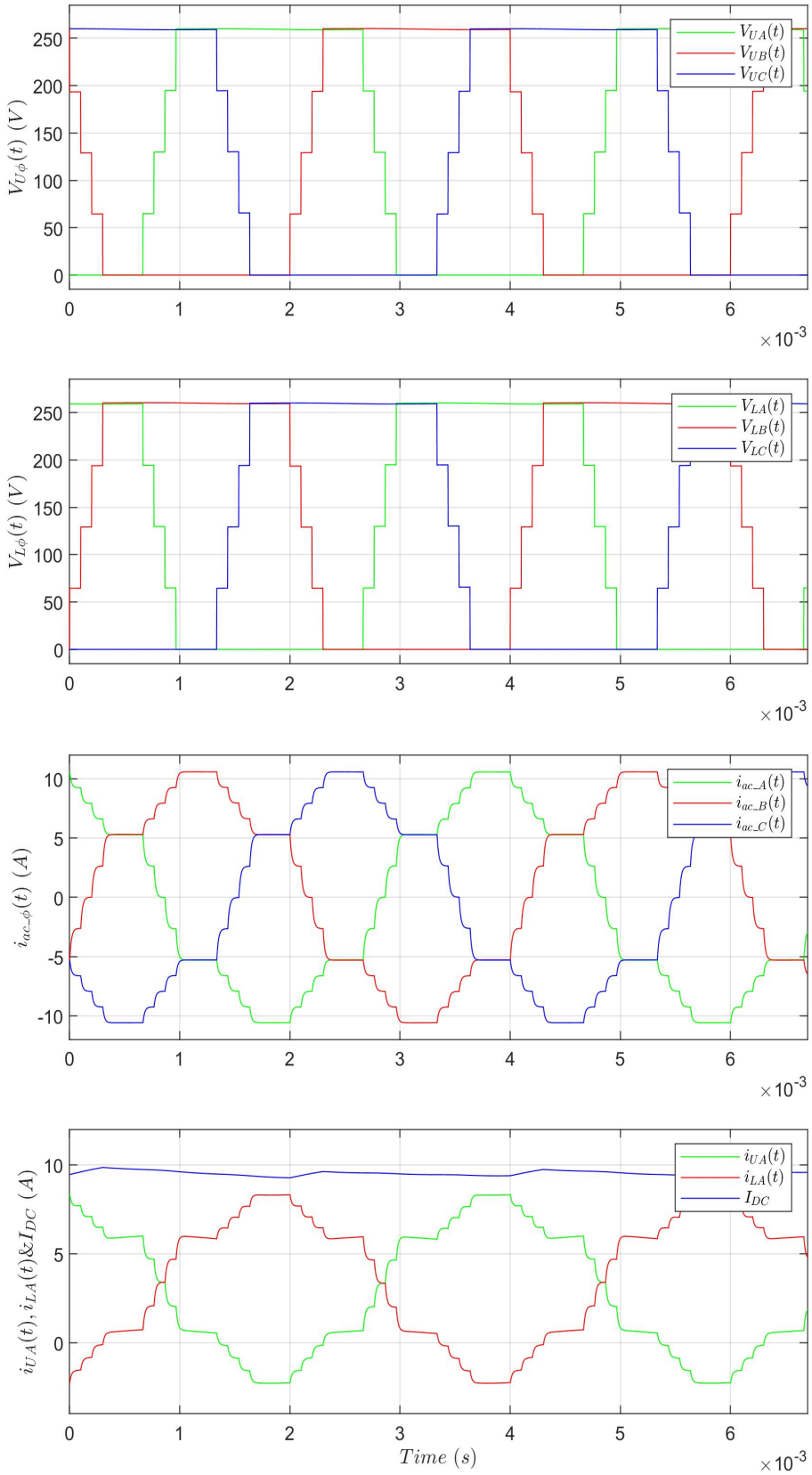


Figure 8.9: *Simulation results of MTrMMC upper chain-link voltages, lower chain-link voltages, three phase AC current, phase A upper and lower arm currents and DC current*

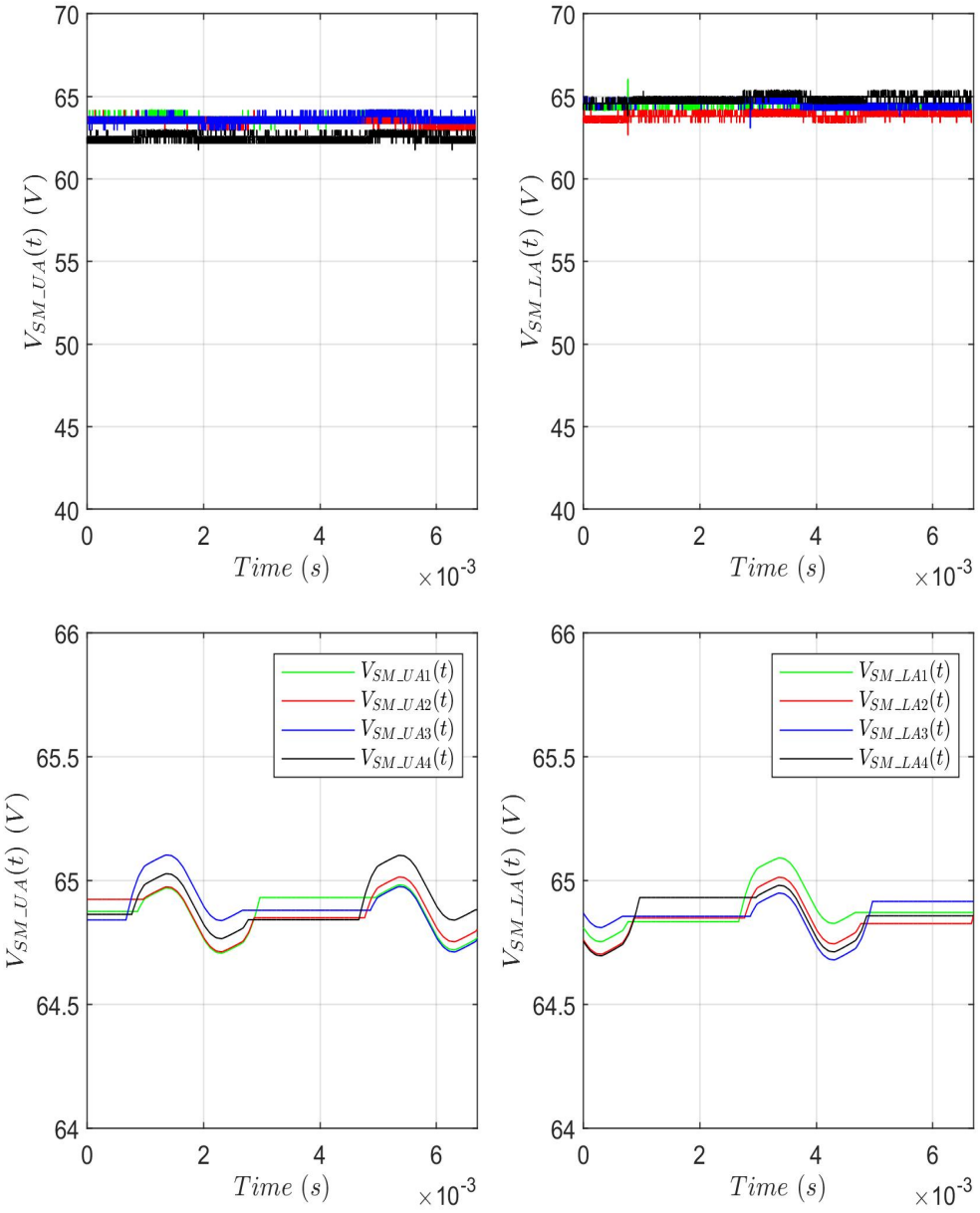


Figure 8.10: *Practical results of phase A upper SM voltages, practical results of phase A lower SM voltages, simulation results of phase A upper SM voltage and simulation results of phase A lower SM voltages*

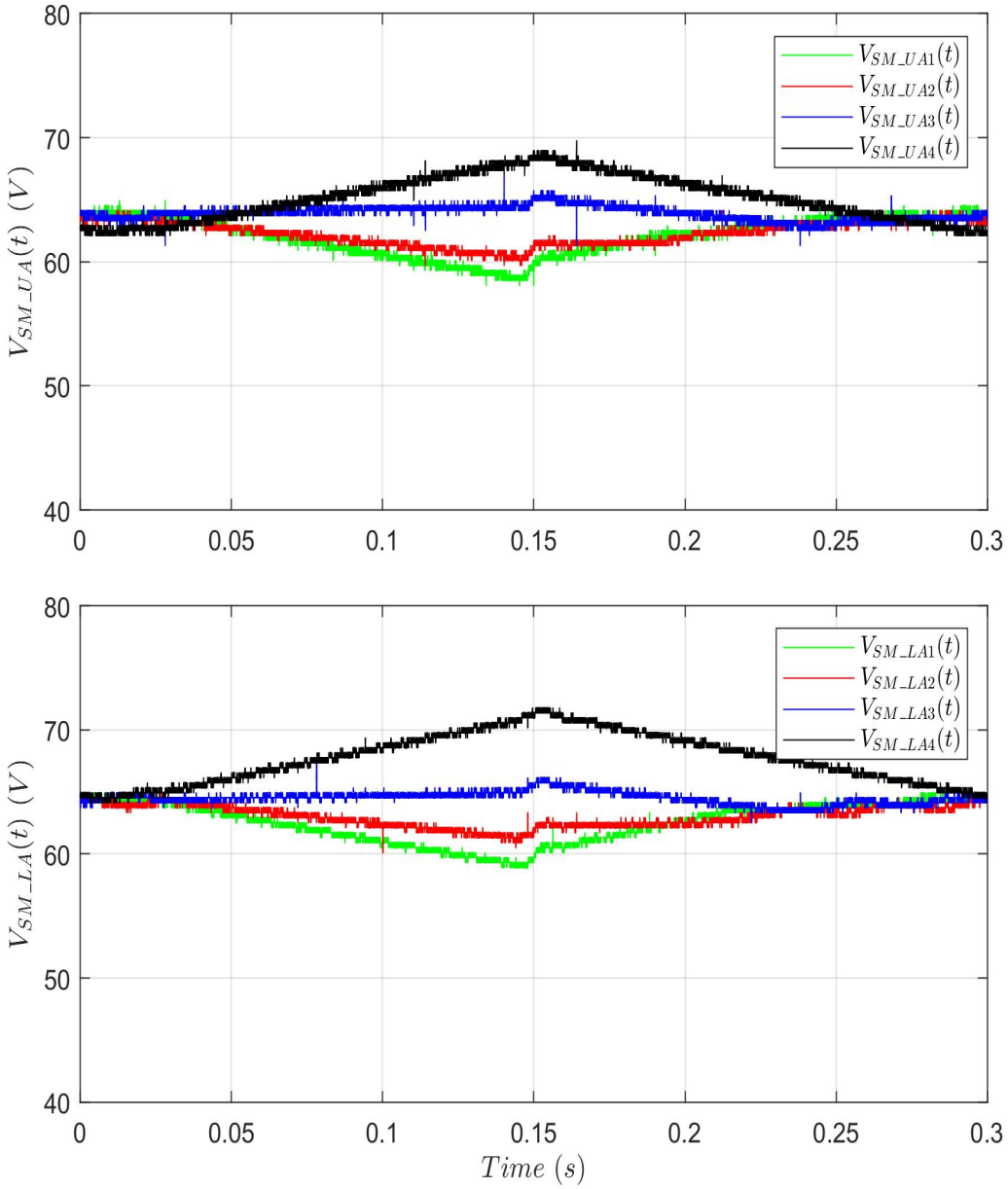


Figure 8.11: *Practical results of balancing phase A upper and lower SM voltages, balancing is disabled at 0.02s and enabled again at 0.144s*

8.5.2 Transient results

A load step response is practically applied from 1.7 kW to 2.6kW during continuous operation in order to show the dynamic response of the MTrMMC converter. Figure 8.12 shows the transient response of the $V_{U\phi}(t)$, $V_{SM\_U\phi}(t)$, $i_{ac\_\phi}(t)$, $I_{UA}(t)$, $I_{UA}(t)$, and I_{DC}. By observing these responses, it is clear that the balancing method for the SM capacitor voltages and the controlled MTrMMC operate as expected.

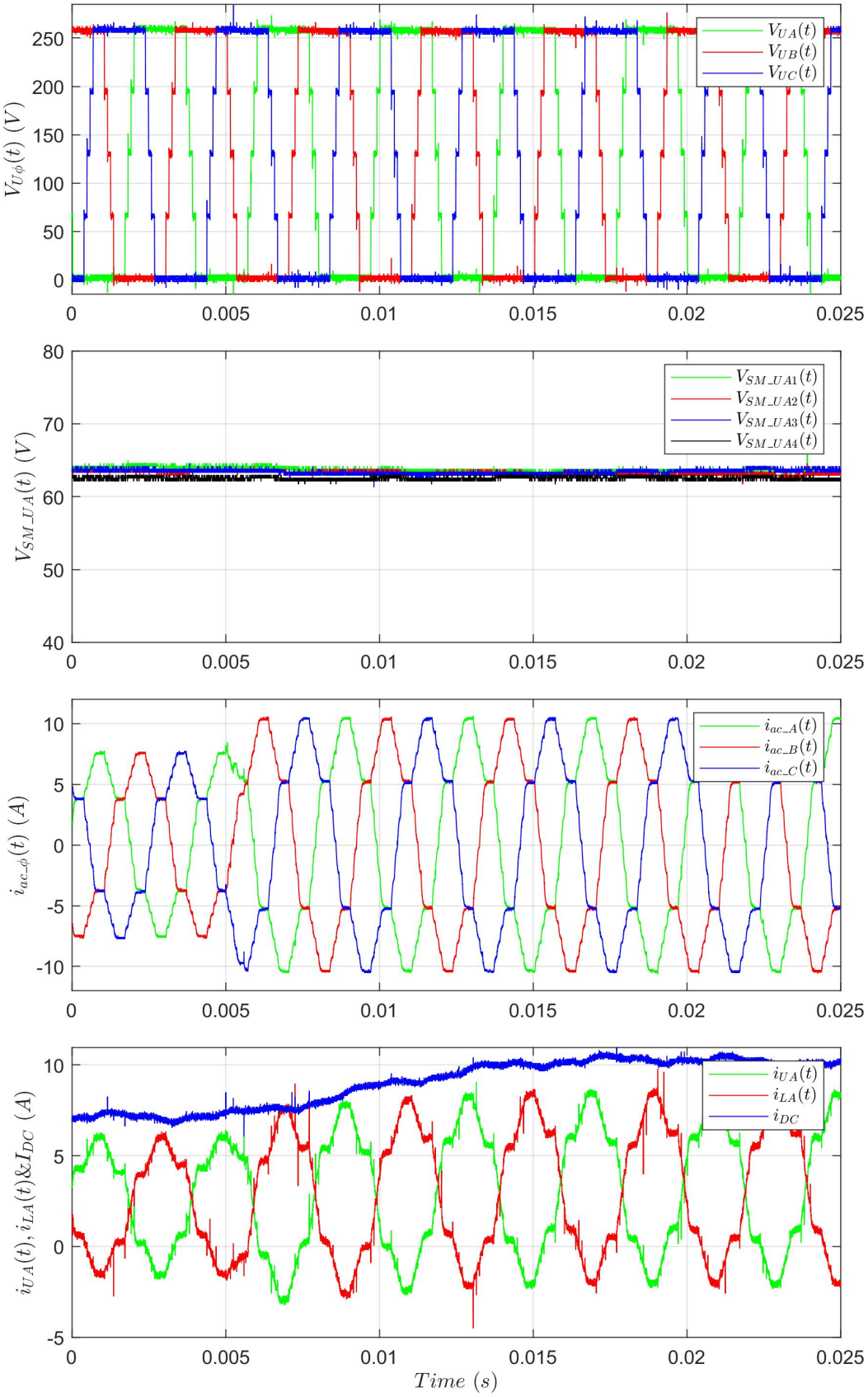


Figure 8.12: *Practical results of MTrMMC upper chain-link voltages, phase A upper SM voltages, three phase AC current and phase A upper and lower arm currents and DC current at step load from 1.7 kW to 2.5kW and it is applied at 0.005s*

8.6 Practical results for the TrSCC-DC-DC converter operation

Table 8.3 shows the parameters of the experimental setup for the TrSCC-DC-DC converter. The system is operated at $\approx 2.8\ kW$ for DC-DC conversion with 400 V imposed on both DC sides. The phase shift, φ (T_{sh}), between the primary and secondary chain-link voltages is controlled in order to transfer the required power. For the operation of the TrSCC-DC-DC converter, $T_t = 20\ \mu s$ and $T_d = 10\ \mu s$ have been selected for both operational modes A and B. In operational mode C, T_t and T_d depend on the number of the phases and SMs in each chain-link hence, $T_t = 500\ \mu s$ and $T_d = 250\ \mu s$.

Table 8.3: TrSCC-DC-DC system parameters

Parameters	Value
$V_{DCP} = V_{DCS}$	400 V
Active Power	$\approx 2.8\ kW$
V_{SM}	$\approx$ 66.5V
C_{SM}	5.28 mF
$C_{bP} = C_{bS}$	220 µF
L_k	0.95 mH
$L_{dcP} = L_{dcS}$	0.95 mH
N_{SM} *Per Chain-Link*	3
N_L	1
N_{ph}	4
f_o	500 Hz
k_f	≈ 1.44

8.6.1 Practical results for the TrSCC-DC-DC converter under operational mode A

8.6.1.1 Steady-state operation

The results of the phases 3 and 4 are identical to phase 1 and phase 2 of the converter, respectively, and hence only the practical results of phase 1 and 2 are shown. Figure 8.13 shows the practical results of the phase 1 and phase 2 primary chain-link voltages, AC link currents, and the primary and secondary DC currents of the TrSCC-DC-DC under operational mode A, respectively. A SM ripple at 1 $kHz = 2f_o$ can be observed in both DC current responses. In comparison to operational mode B which will be shown in the following section, the current ripple is higher due to, firstly, the existence of the lower frequency voltage ripple in total chain-link voltage of one side of the converter, and secondly, the non ideal AC link components which results in a slightly different impedance between the phases. As a result, the AC link currents are not cancelled perfectly as explained in detail in chapter 6. Figure 8.14 shows the practical results of the phase 1 primary and secondary chain-link voltages, blocking capacitor voltages, primary tank inductor voltage, and the primary and secondary SM voltages, respectively. The phase shift between the primary and secondary chain-link voltages, $\varphi(T_{sh})$, can be observed and it can be also seen that the blocking capacitors, C_{bP} and C_{bS}, block the DC component of the chain-link voltages effectively.

The same results from the simulation are depicted in figures 8.15 and 8.16. It can be seen that the practical results match these well. In comparison to operational mode B which will be shown in the following section, as expected, under operational mode A there is a higher ripple in the DC currents at 1 $kHz = 2f_o$.

8.6.1.2 Transient response

The power demand is changed from 1.7 kW to 2.8kW during operation in order to demonstrate the total power flow control and dynamic response of the converter.

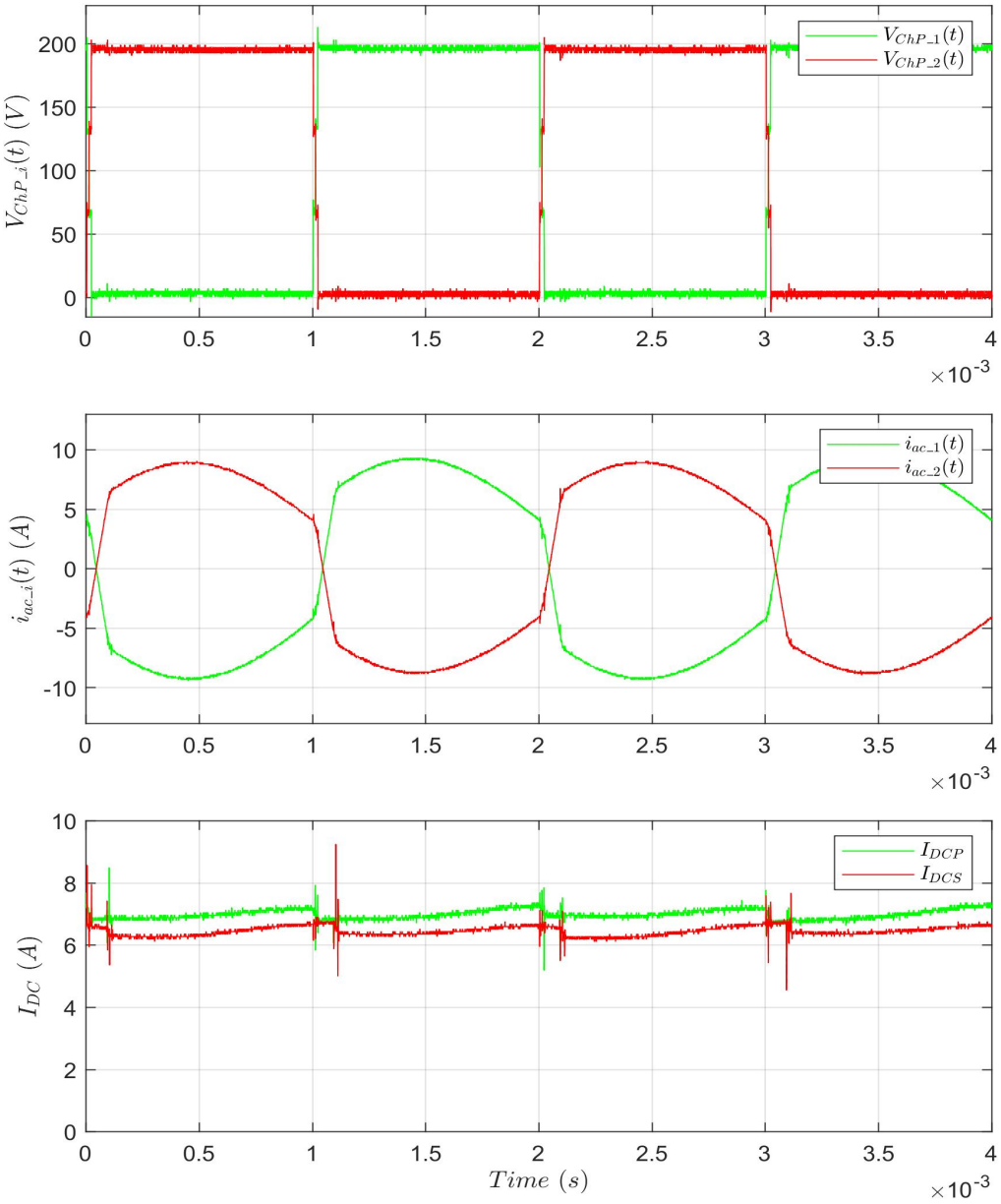


Figure 8.13: *Practical results of primary phase 1 and phase 2 chain-link voltages, AC currents and DC currents waveforms for TrSCC-DC-DC mode A*

Figure 8.17 shows the transient response of the phase 1 and phase 2 primary chain-link voltages, AC link currents, and the primary and secondary DC current, respectively. Figure 8.18 shows the transient response of the phase 1 waveforms which include the primary and secondary chain-link voltage, DC blocking capacitor voltages, primary tank inductor voltage, and the primary and secondary SM voltages. By observing the response of each, and how well these results match it is clear that the total power flow control of the TrSCC-DC-DC under operational mode A works as expected.

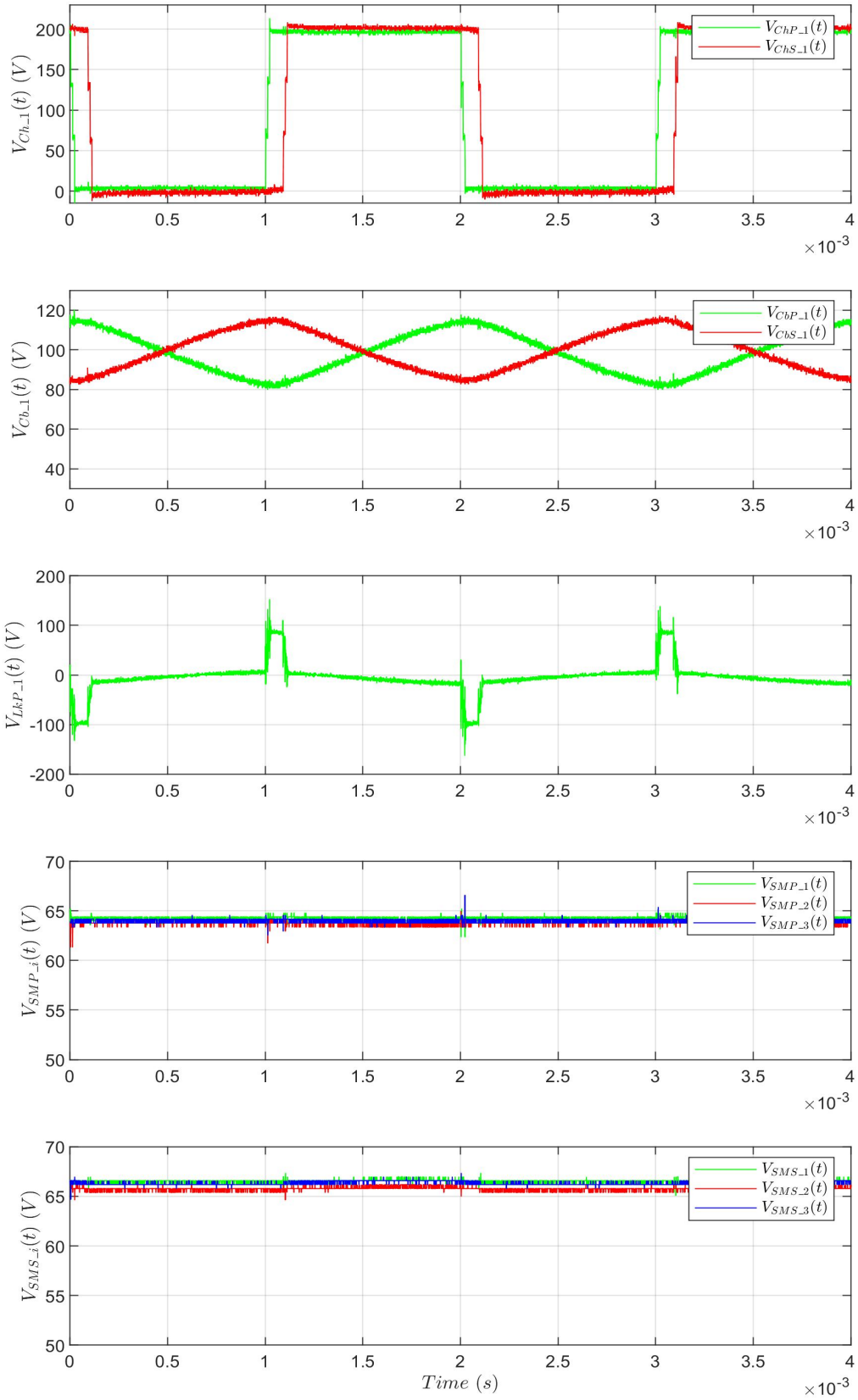


Figure 8.14: *Practical results of phase 1 chain-link voltages, blocking capacitor voltages, primary tank inductor voltage, primary and secondary SM voltage waveforms for TrSCC-DC-DC mode A*

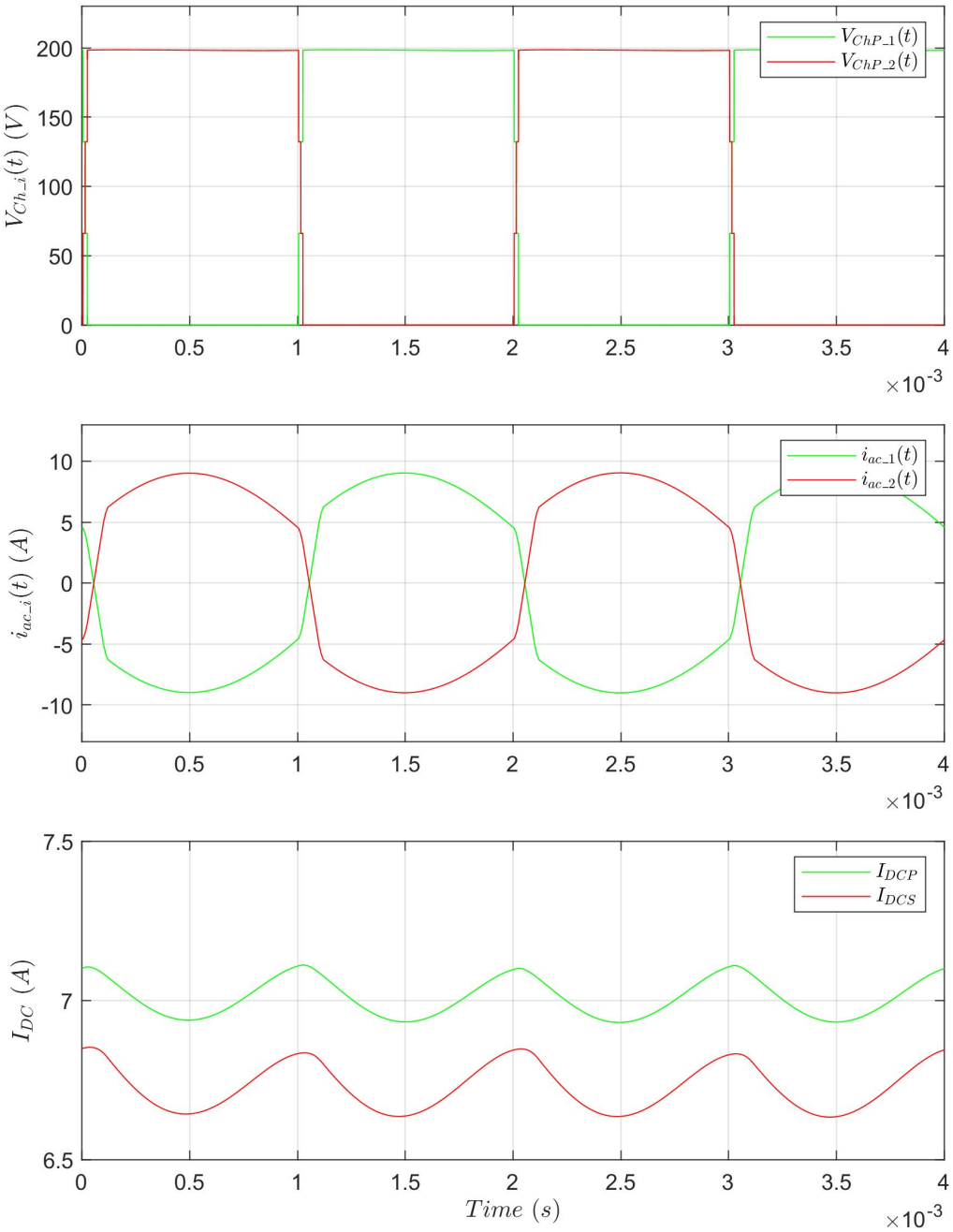


Figure 8.15: *Simulation results of primary phase 1 and phase 2 chain-link voltages, AC currents and DC currents waveforms for TrSCC-DC-DC mode A*

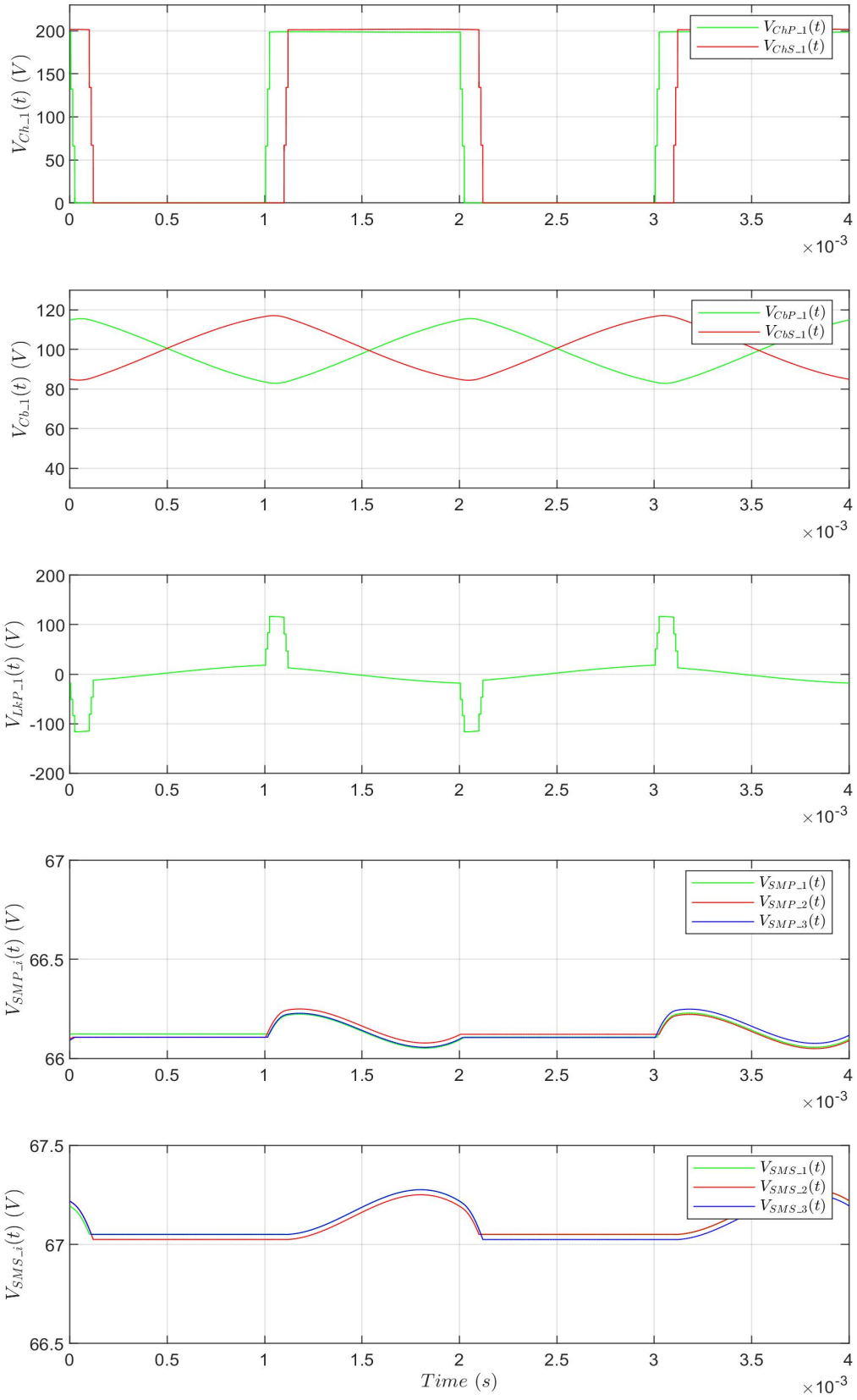


Figure 8.16: *Simulation results of phase 1 chain-link voltages, blocking capacitor voltages, primary tank inductor voltage, primary and secondary SM voltage waveforms for TrSCC-DC-DC mode A*

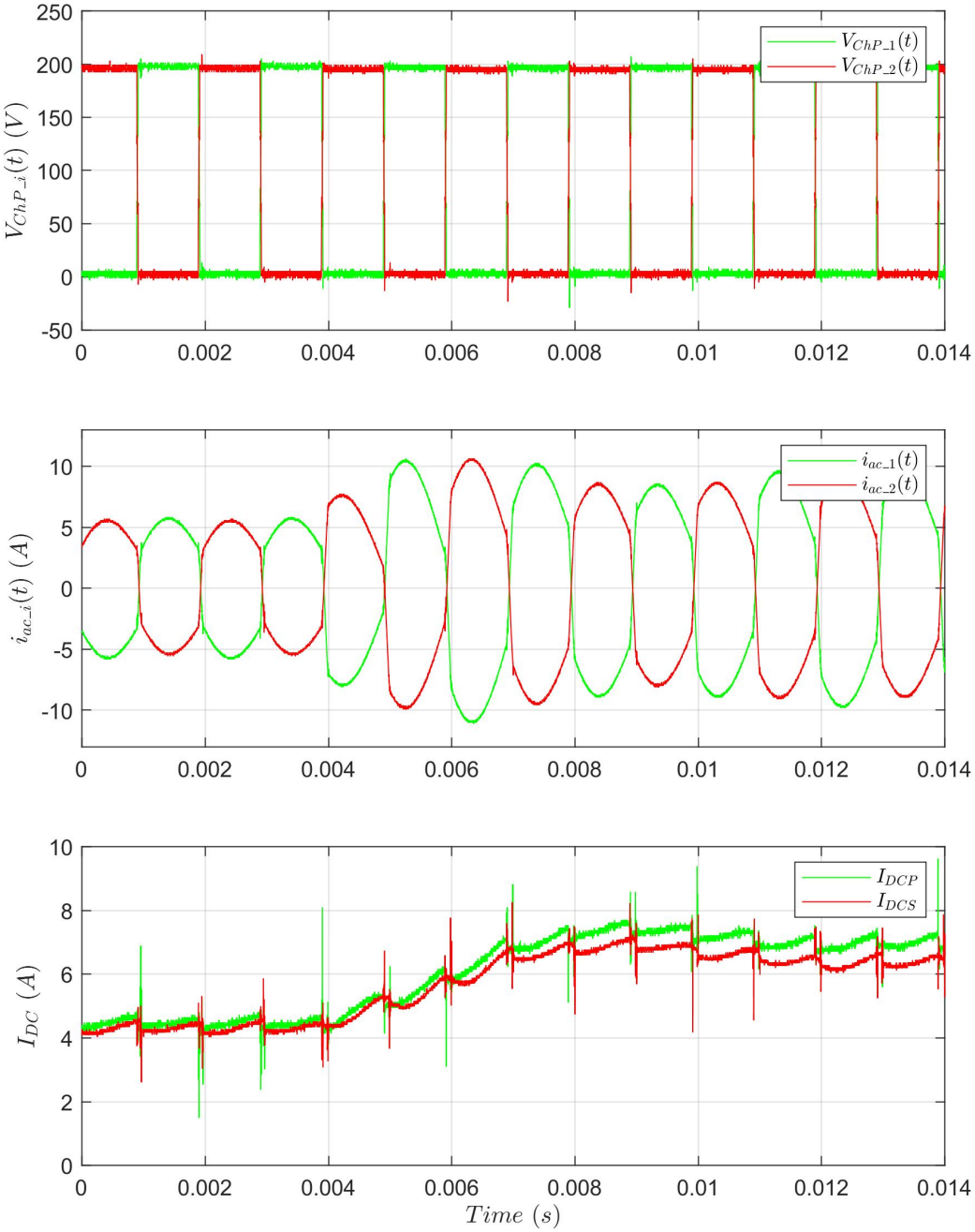


Figure 8.17: *Practical results of priamry phase 1 and phase 2 chain-link voltages, AC currents and DC current waveforms for TrSCC-DC-DC mode A at step load from 1.7 kW to 2.8kW*

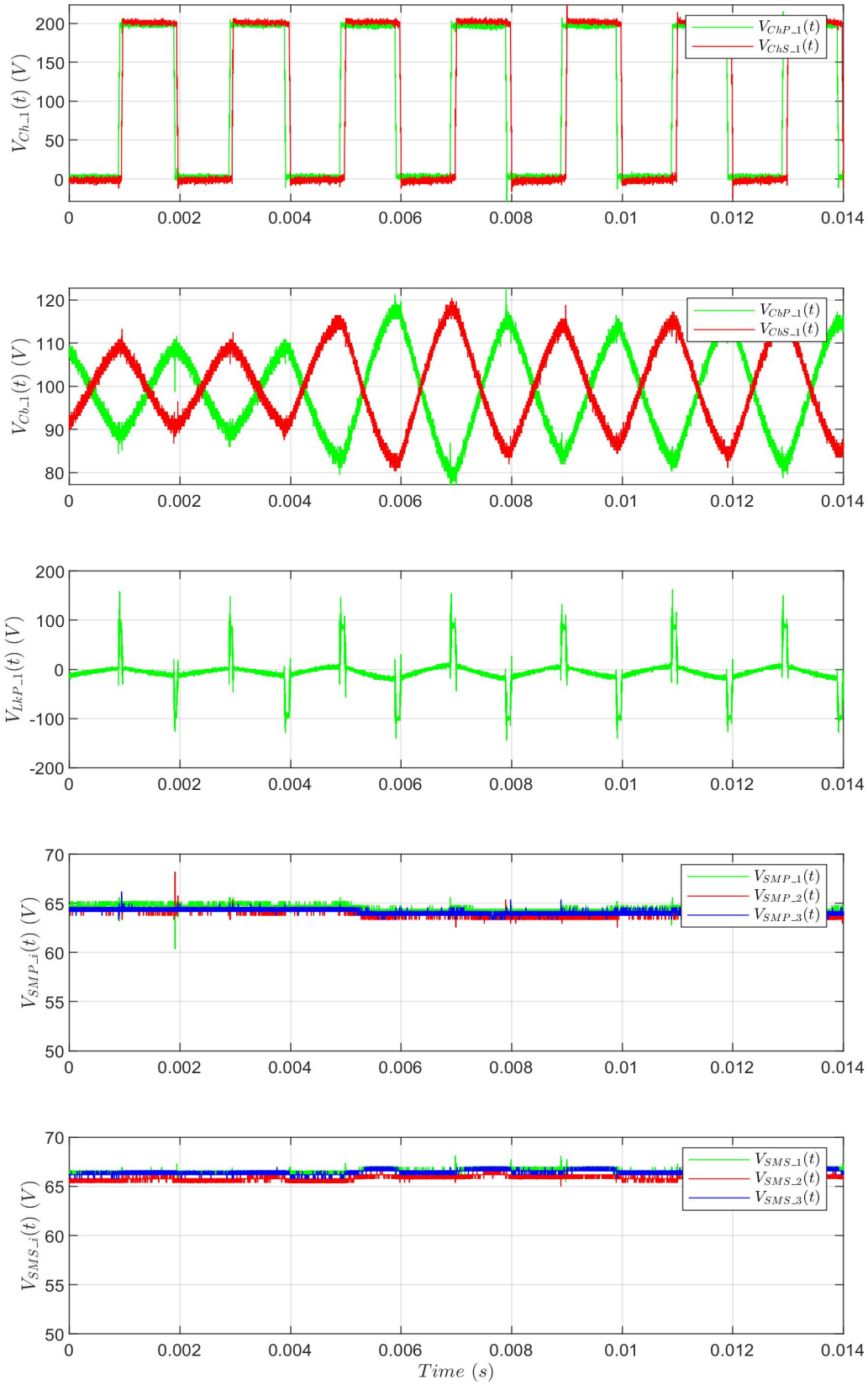


Figure 8.18: *Practical results of phase 1 chain-link voltages, blocking capacitor voltages, primary tank inductor voltage, primary and secondary SM voltage waveforms for TrSCC-DC-DC mode A at step load from 1.7 kW to 2.8kW*

8.6.2 Practical results for the TrSCC-DC-DC converter in operational mode B

8.6.2.1 Steady-state operation

Figure 8.19 shows the practical results of the primary chain-link voltages, AC link currents, and the primary and secondary DC currents of the TrSCC-DC-DC converter under operational mode B, respectively. A SM ripple frequency component at 2 $kHz = 4f_o$ can be observed in both DC current responses. Figure 8.20 shows the practical results of the phase 1 primary and secondary chain-link voltages, the blocking capacitor voltages, the primary tank inductor voltage, and the primary and secondary SM voltages, respectively. The phase shift between the primary and secondary chain-link voltages, $\varphi(T_{sh})$, can be observed and it can be also seen that the blocking capacitors, C_{bP} and C_{bS}, block the DC part of the chain-link voltages effectively. Furthermore, the same balancing method was implemented for all TrSCC-DC-DC converter operational modes and this is clearly effective. Again, since the SM capacitors are larger than required, the ripple voltage is very small.

The same results from simulation work are depicted in figures 8.21 and 8.22. The practical and simulation results match well. The ripple in the DC current responses is at 2 $kHz = 4f_o$ as expected. The voltage ripple, $\approx 0.22V$, across the SM capacitors matches in both sets of results.

8.6.2.2 Transient response

The power demand is changed from 1.7 kW to 2.8kW during operation to show the total power flow control dynamic response for the converter. Figure 8.23 shows the transient response of the primary chain-link voltages, AC link currents, and the primary and secondary DC currents, respectively. Figure 8.24 shows the transient response of the phase 1 voltages and currents which include the primary and secondary chain-link voltages, DC blocking capacitor voltages, primary tank inductor voltage, and the primary and secondary SM voltages.

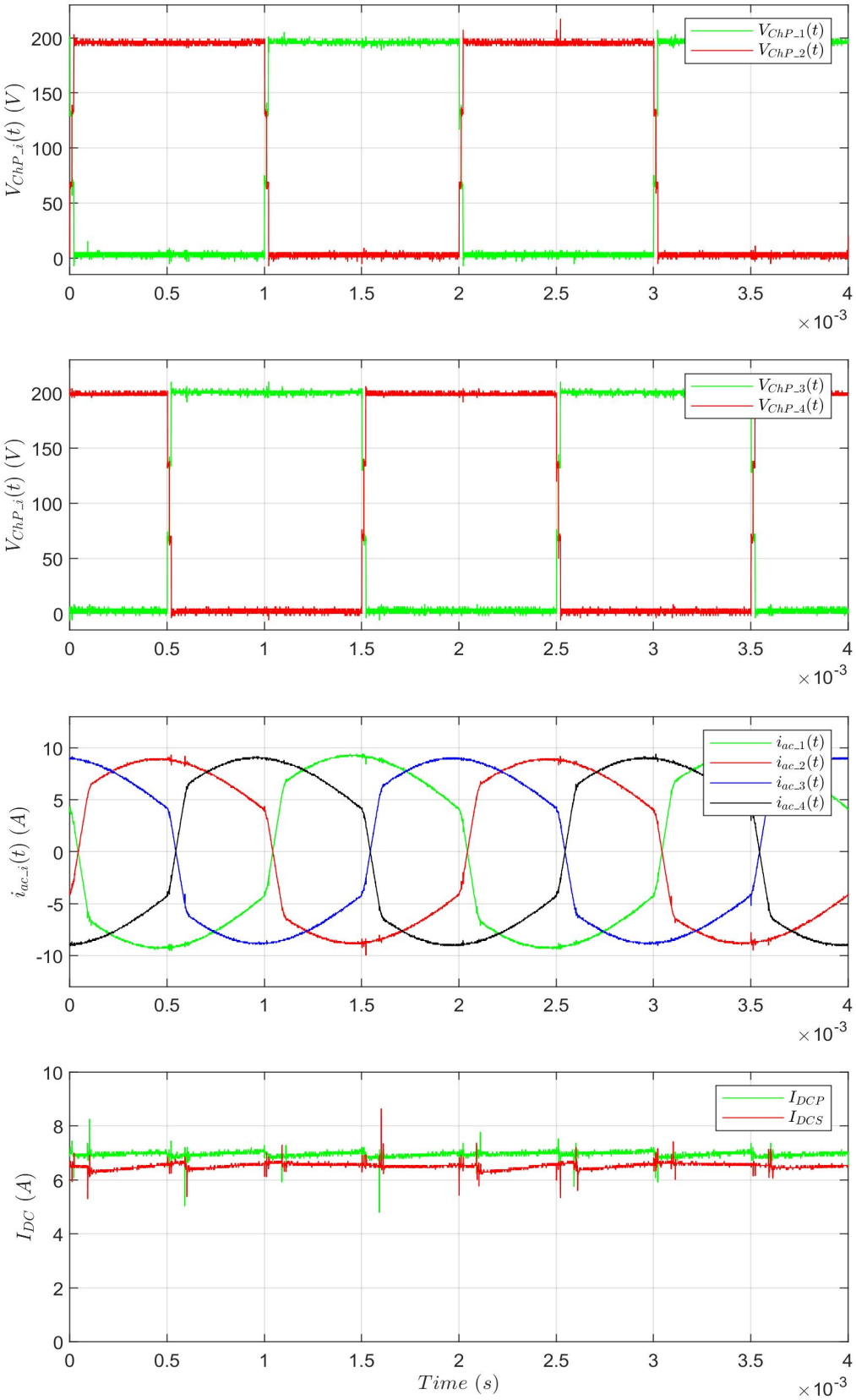


Figure 8.19: *Practical results of primary chain-link voltages, AC currents and DC currents waveforms for TrSCC-DC-DC operation B*

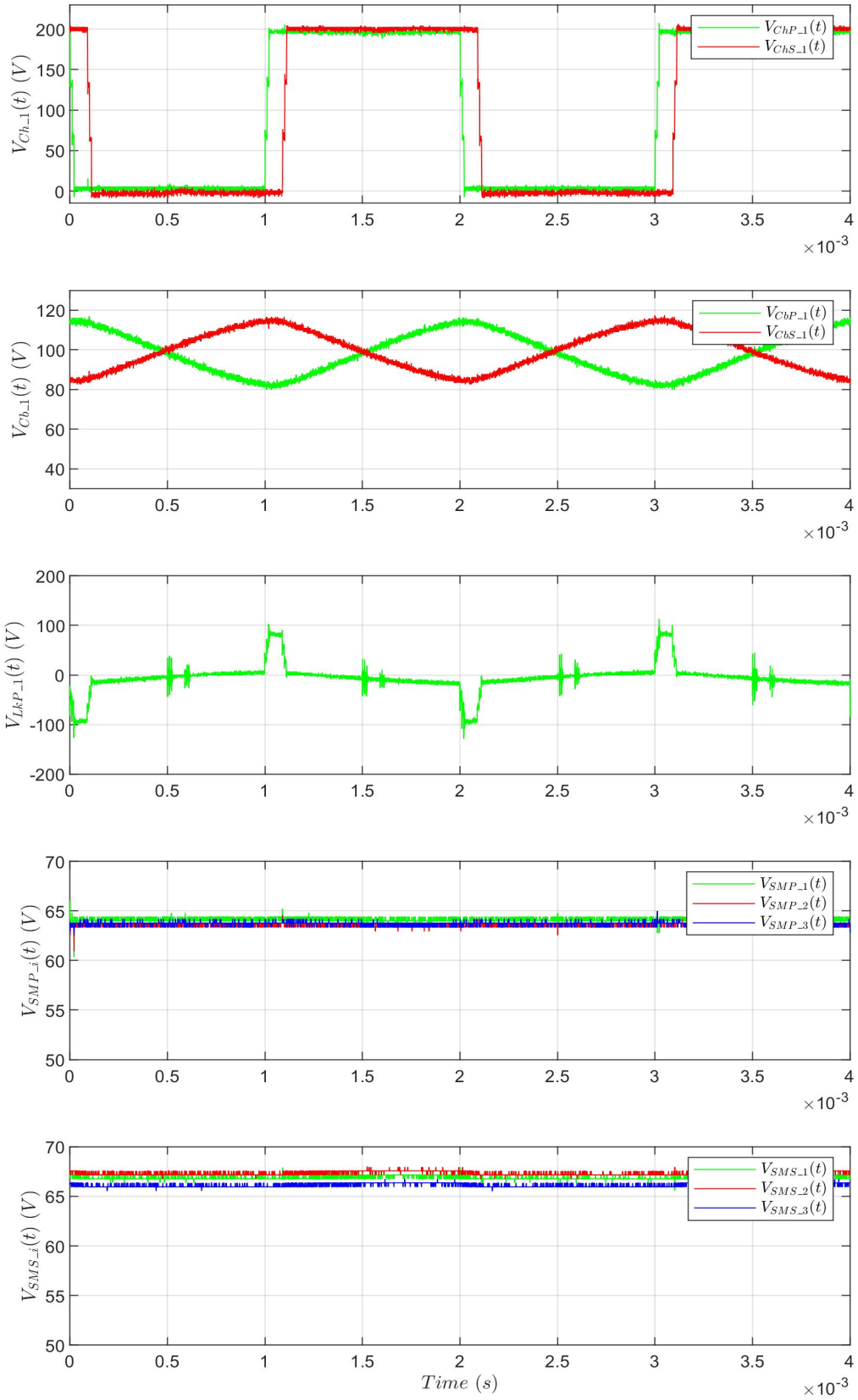


Figure 8.20: *Practical results of phase 1 chain-link voltages, blocking capacitor voltages, primary tank inductor voltage, primary and secondary SM voltages waveforms for TrSCC-DC-DC mode B*

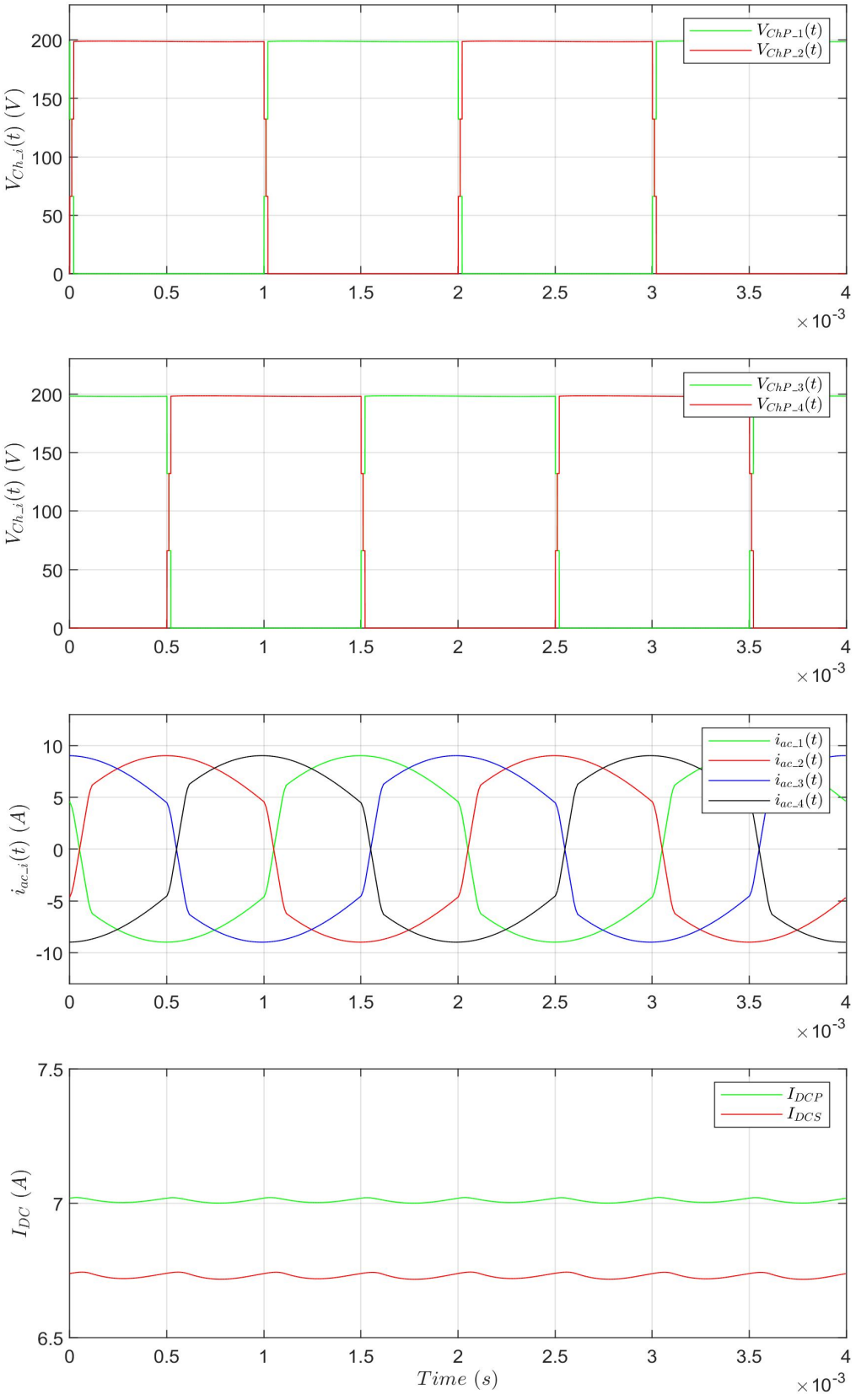


Figure 8.21: *Simulation results of primary chain-link voltages, AC currents and DC currents waveforms for TrSCC-DC-DC mode B*

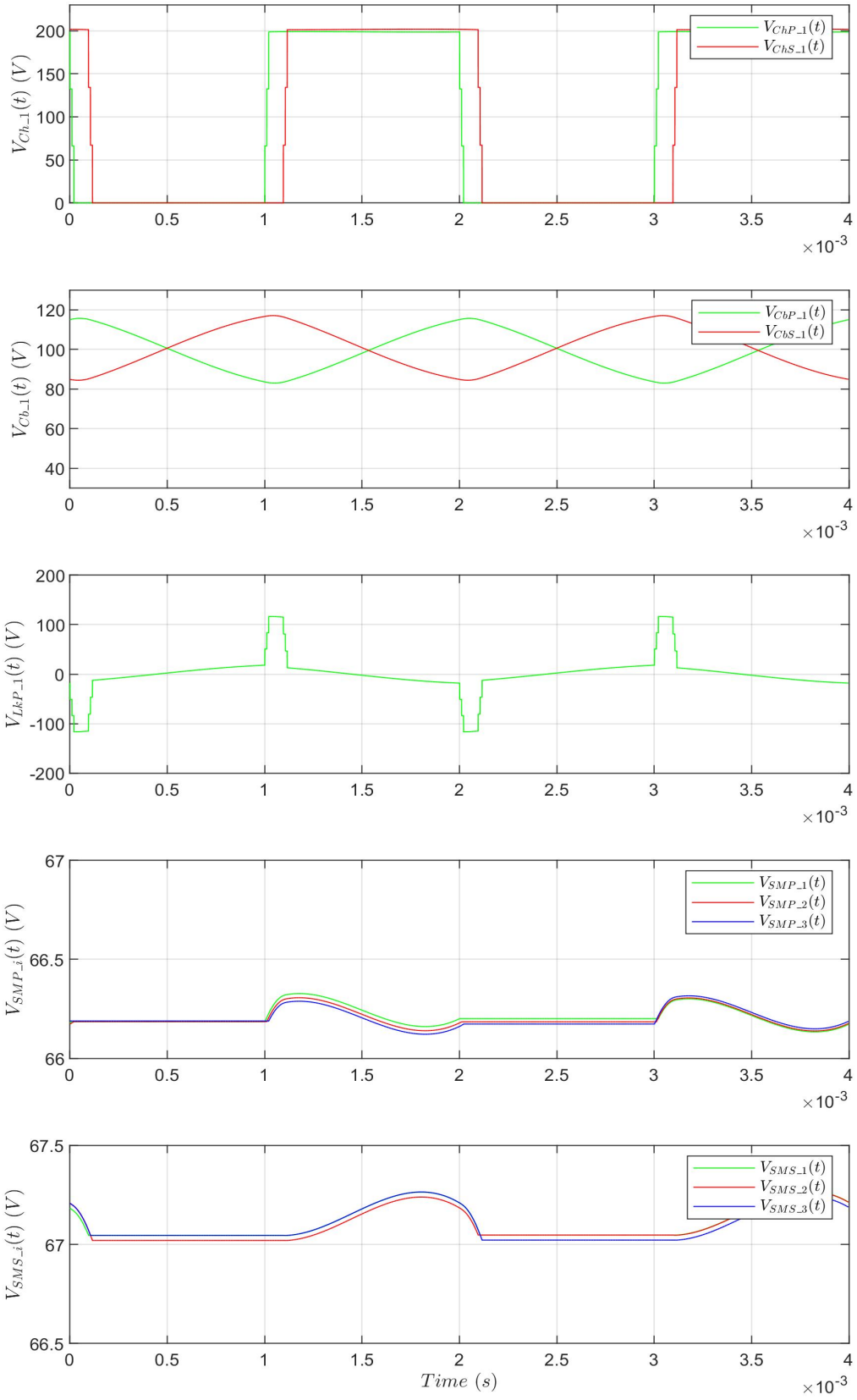


Figure 8.22: *Simulation results of phase 1 chain-link voltages, blocking capacitor voltages, primary tank inductor voltage, primary and secondary SM voltages waveforms for TrSCC-DC-DC operation B*

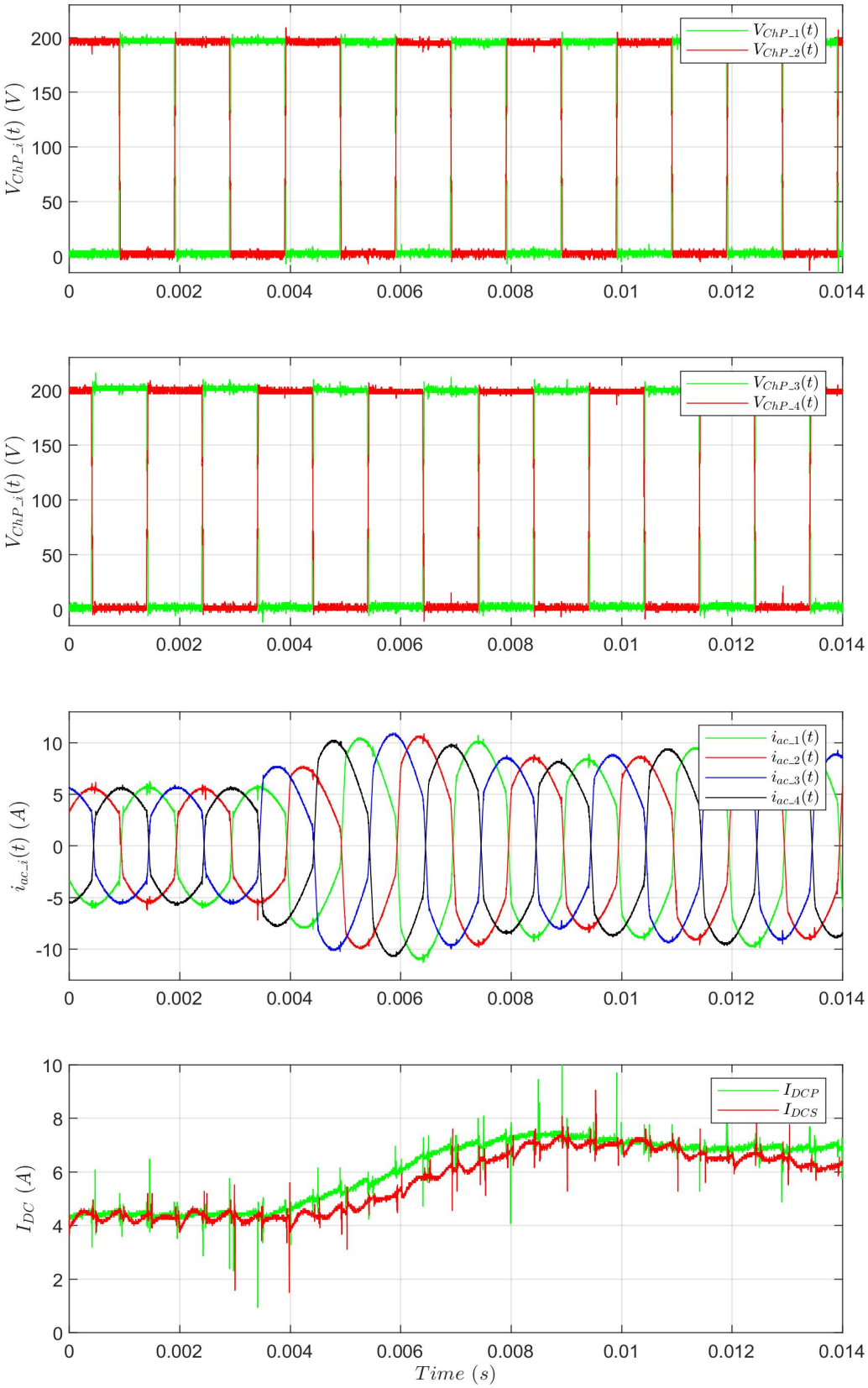


Figure 8.23: *Practical results of primary chain-link voltages, AC currents and DC currents waveforms for TrSCC-DC-DC mode B at step load from 1.7 kW to 2.8kW*

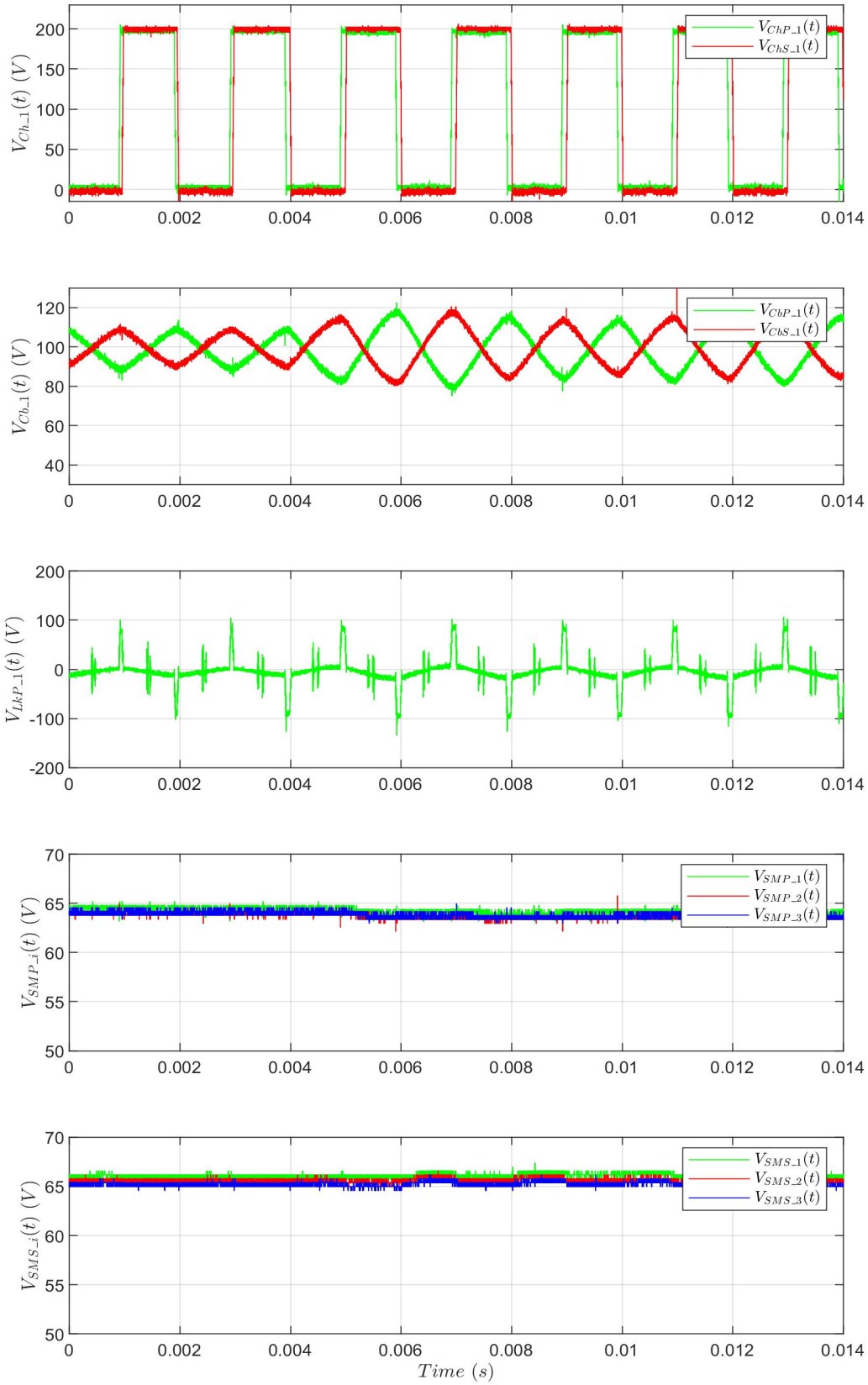


Figure 8.24: *Practical results of phase 1 chain-link voltages, blocking capacitor voltages, primary tank inductor voltage, primary and secondary SM voltage waveforms for TrSCC-DC-DC mode B at step load from 1.7 kW to 2.8kW*

8.6.3 Practical results of the TrSCC-DC-DC converter under operational mode C

8.6.3.1 Steady-state operation

Figure 8.25 shows the practical results of the primary chain-link voltages, AC link currents, and the primary and secondary DC currents of the TrSCC-DC-DC under operational mode C, respectively. The rig is tested at power level equal to 2.5kW for operational mode C due to the higher per-phase AC current which is required to transfer the power. Considering the SM capacitor current rating and its safety margin, the power transfer of 2.5kW is the maximum possible testing power with operational mode C. This is because the SM capacitors conduct the per-phase AC current plus DC current, and therefore run closer to the SM capacitor current ratings. Figure 8.26 shows the practical results of the phase 1 primary and secondary chain-link voltage, blocking capacitor voltages, primary tank inductor voltage, and the primary and secondary SM voltages, respectively. The phase shift between primary and secondary chain-link voltages, $\varphi(T_{sh})$, can be observed and considering that there is less power flow, and it is higher than that of the other two operational modes. The higher AC current can also be observed in the AC current response. Furthermore, it can be seen that the blocking capacitors, C_{bP} and C_{bS}, block the DC part of the chain-link voltages effectively and the tank inductor voltage, V_{LkP}, peak voltage is lower when compared to the other TrSCC-DC-DC operational modes.

The same results from simulation are depicted in figures 8.27 and 8.28. It can be seen that the practical results match these well and this demonstrates the effectiveness of the proposed TrSCC-DC-DC converter operation under mode C.

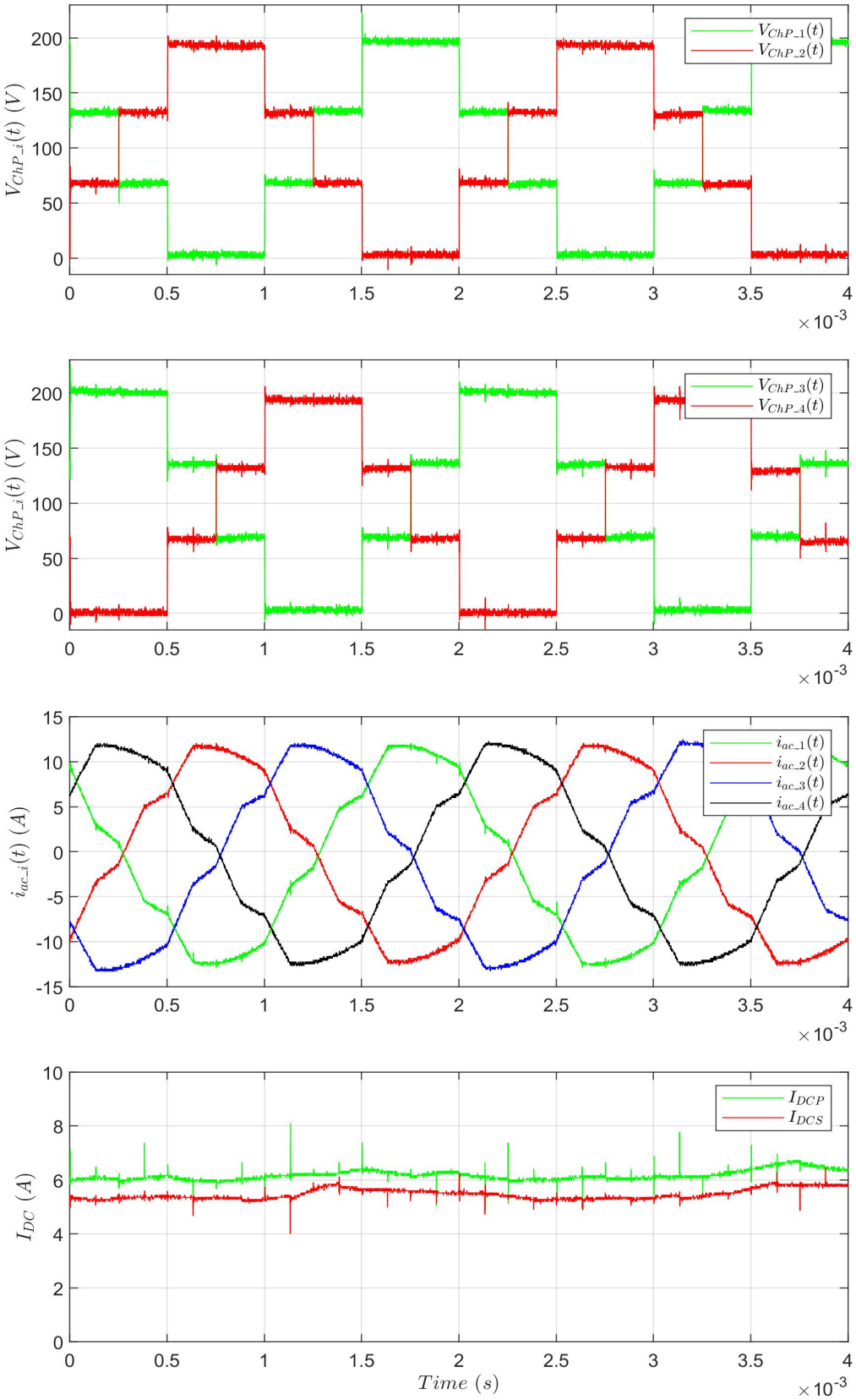


Figure 8.25: *Practical results of primary chain-link voltages, AC currents and DC currents waveforms for TrSCC-DC-DC mode C*

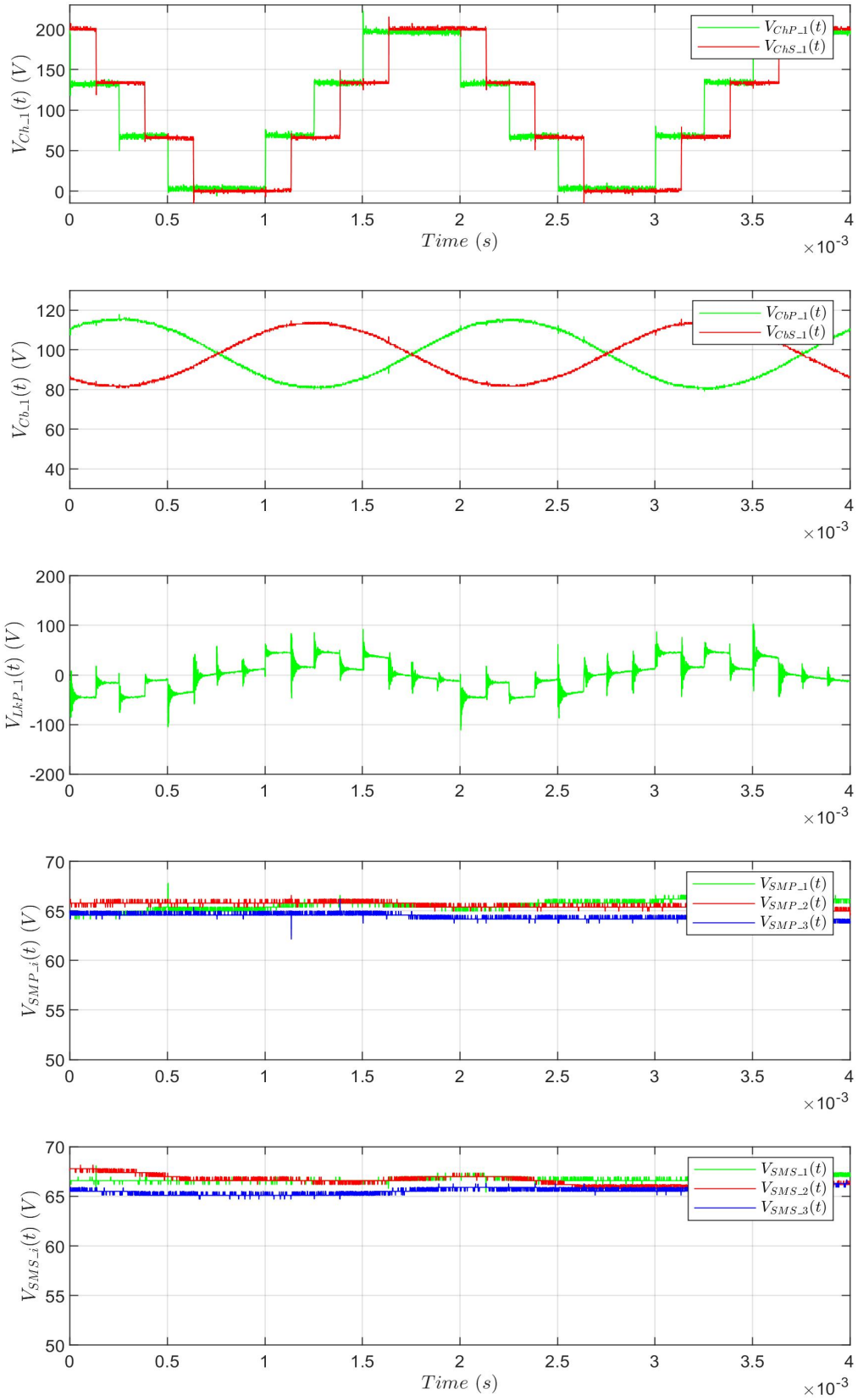


Figure 8.26: *Practical results of phase 1 chain-links voltage, blocking capacitor voltages, primary tank inductor voltage, primary and secondary SM voltage waveforms for TrSCC-DC-DC mode C*

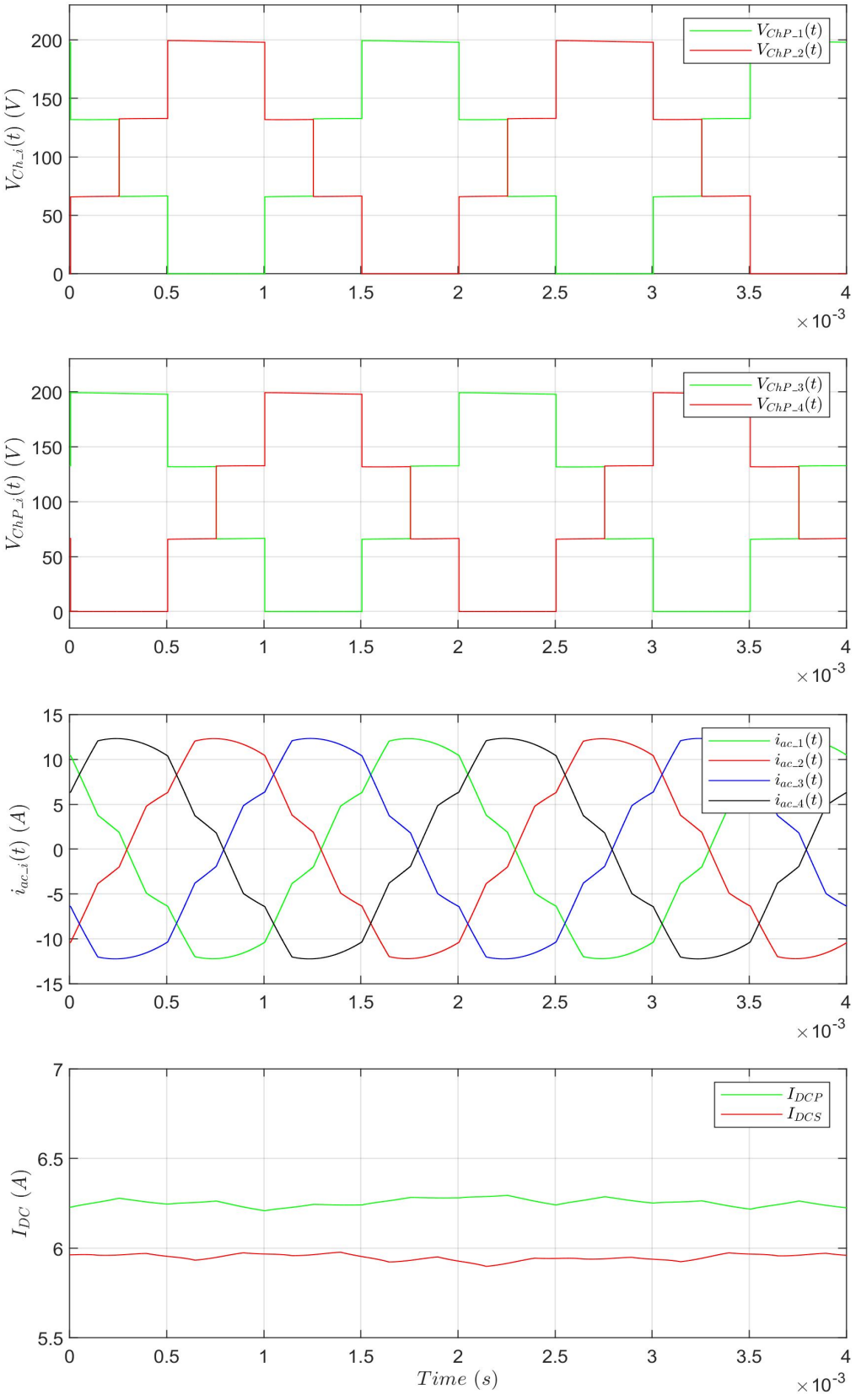


Figure 8.27: *Simulation results of primary chain-link voltages, AC currents and DC currents waveforms for TrSCC-DC-DC mode C*

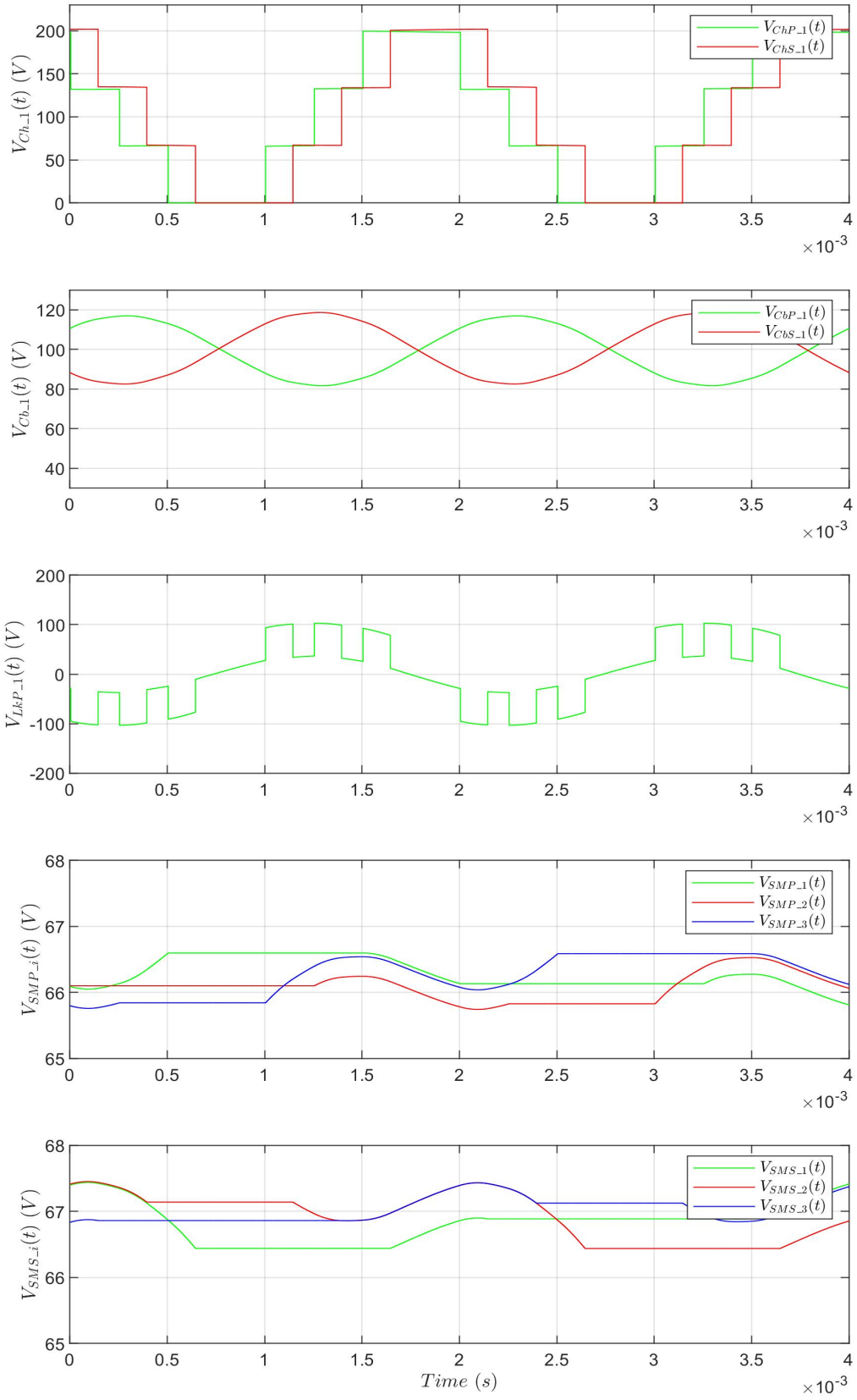


Figure 8.28: *Simulation results of phase 1 chain-links voltage, blocking capacitor voltages, primary tank inductor voltage, primary and secondary SM voltage waveforms for TrSCC-DC-DC mode C*

8.6.3.2 Transient responses

The power demand is changed from 1.7 kW to 2.5kW during operation to show the total power flow control and dynamic responses of the converter. Figure 8.29 shows the transient response of the primary chain-link voltages, AC link currents, and the primary and secondary DC currents, respectively. Figure 8.30 shows the transient response of the primary and secondary chain-link voltages, DC blocking capacitor voltages, primary tank inductor voltage, and the primary and secondary SM voltages. The total power flow control of the TrSCC-DC-DC under operational mode C is clearly operating as expected.

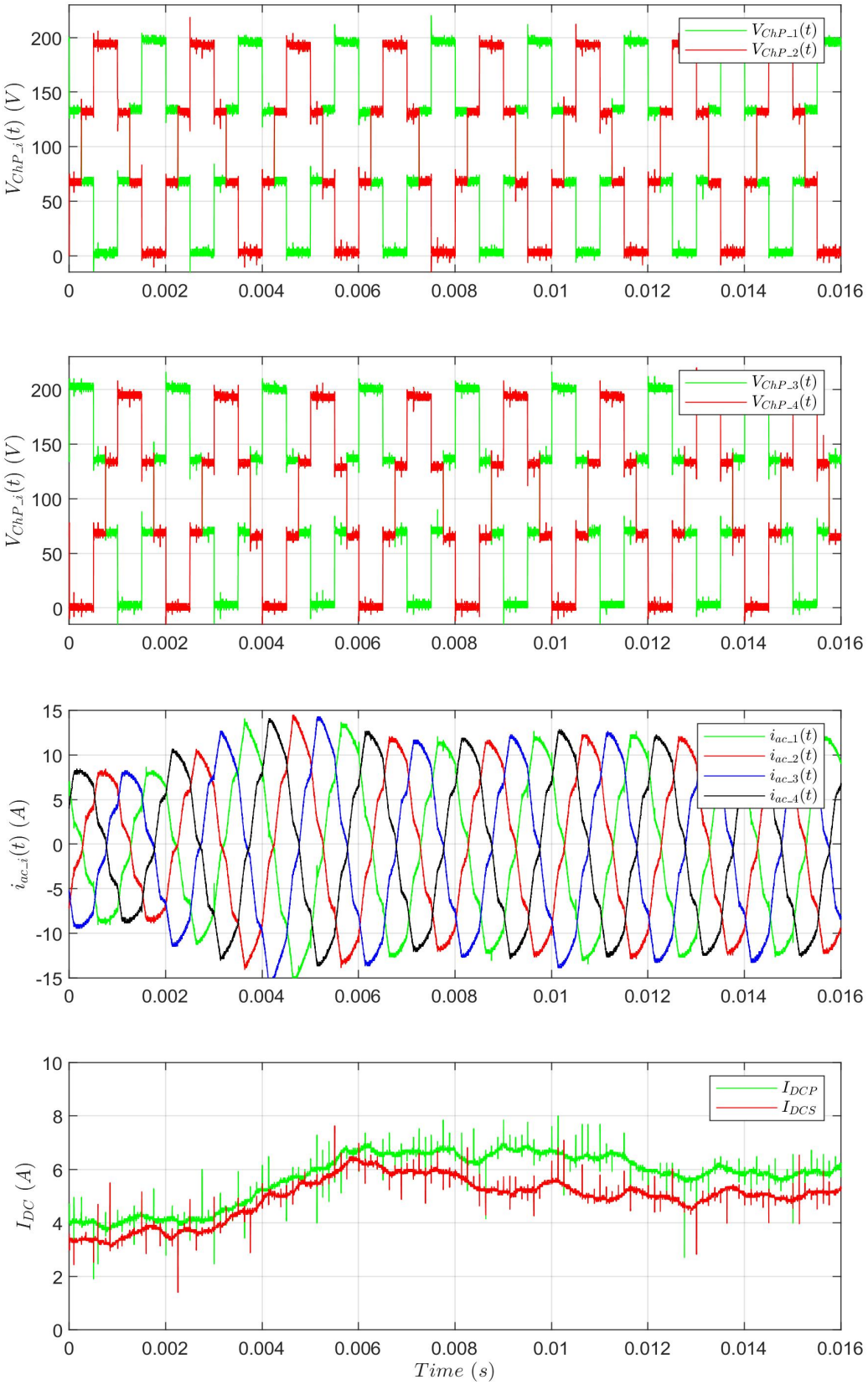


Figure 8.29: *Practical results of primary chain-link voltages, AC currents and DC current waveforms for TrSCC-DC-DC mode C at step load from 1.7 kW to 2.5kW*

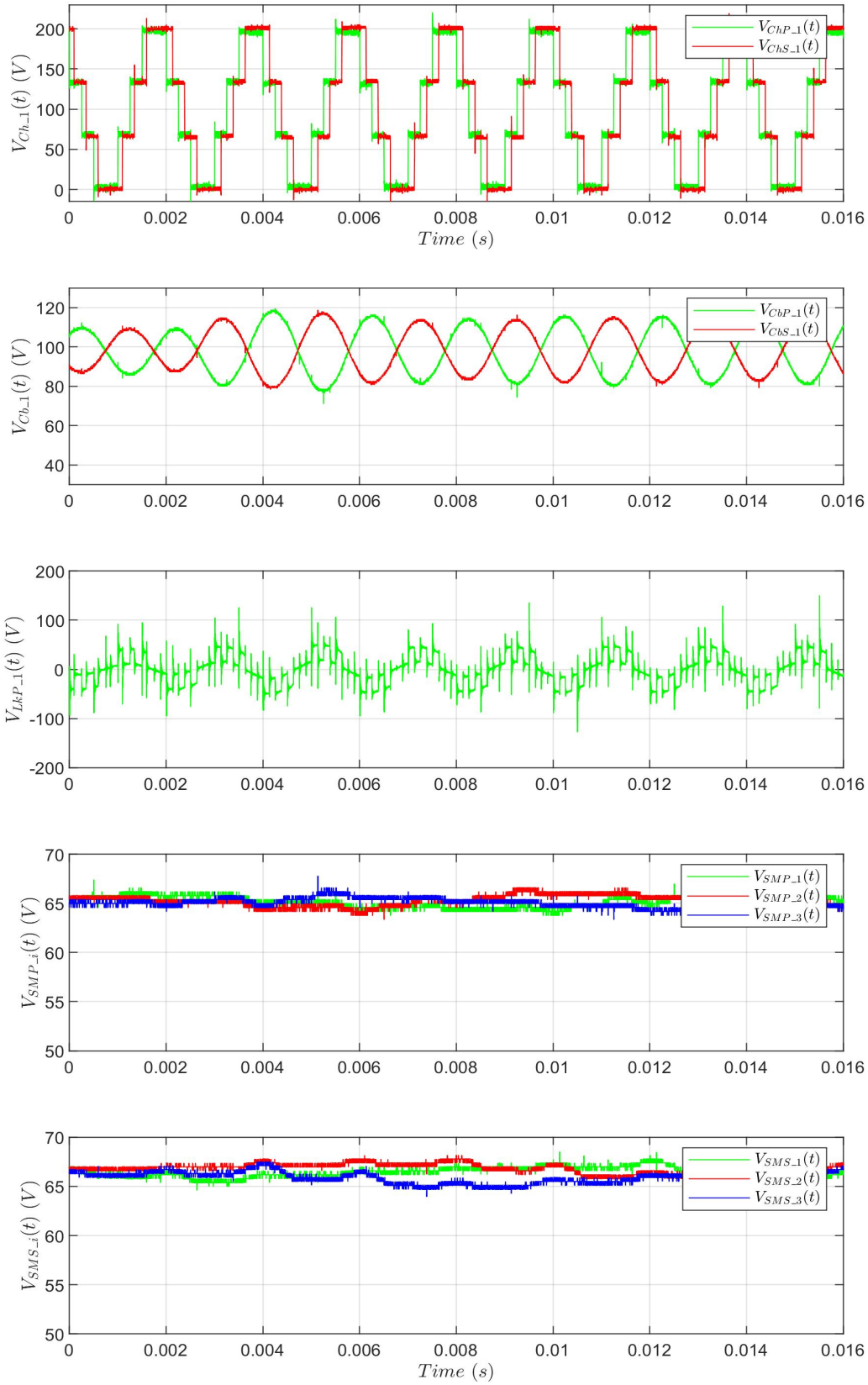


Figure 8.30: *Practical results of phase 1 chain-link voltages, blocking capacitor voltages, primary tank inductor voltage, primary and secondary SM voltage waveforms for TrSCC-DC-DC mode C at step load from 1.7 kW to 2.5kW*

8.6.4 Practical results of the TrSCC-DC-DC converter under operational mode B with $\rho_g = 2$

The DC gain voltage, $\rho_g = 2$, is achieved through the connection of the chain-links with a transformer which has a unity turns ratio as previously shown in figure 8.4. Figure 8.31 shows the practical results of the primary chain-link voltages, AC link currents, and the primary and secondary DC currents of the TrSCC-DC-DC under operational mode B with $\rho_g = 2$, respectively. It can be observed that the secondary DC current is almost twice the primary DC current as expected. Figure 8.32 shows the practical results of the phase 1 primary and secondary chain-link voltages, blocking capacitor voltages, primary tank inductor voltage, and the primary and secondary SM voltages, respectively. Here, it can be seen that the resonant tank voltage and current responses are the same as for TrSCC-DC-DC converter operation under mode B with $\rho_g = 1$ and hence only the practical results are shown.

Since the secondary side of the TrSCC-DC-DC with $\rho_g = 2$ is loaded resistively as shown in the previous chapter, figure 8.4, the SM capacitor voltages of the secondary chain-links must be controlled. The energy control shown in chapter 6, 6.22, is implemented where the phase shift between the primary and secondary chain-links is derived from the average transferred power. The power is changed from 1.8kW to 2.5kW and figure 8.33 shows the transient responses of the primary DC current, phase 1 primary SM capacitor voltages, secondary DC current and the phase 1 secondary SM capacitor voltages. The effectiveness of the control of the secondary chain-link capacitor voltages and their dynamic response is clear.

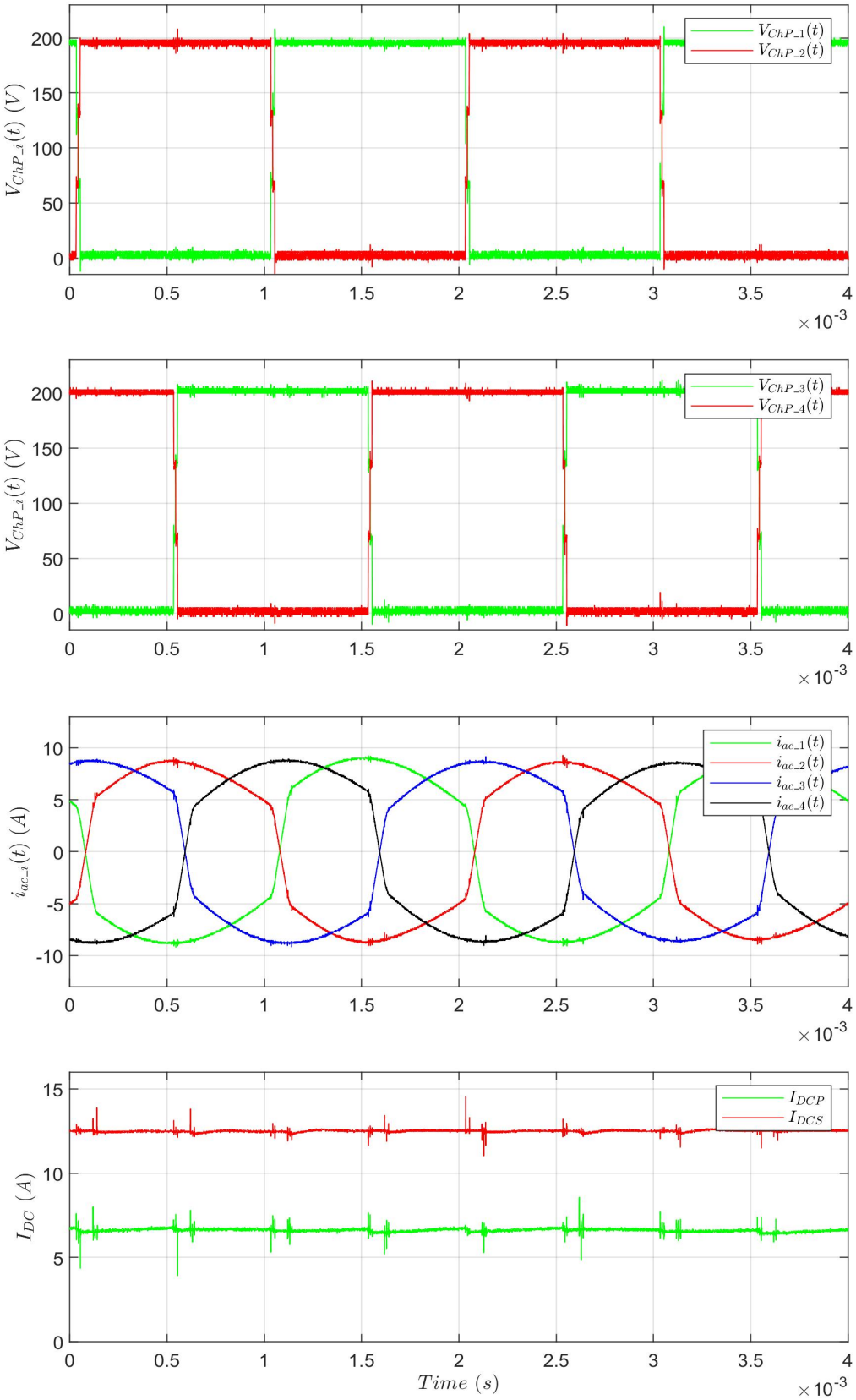


Figure 8.31: *Practical results of primary chain-link voltages, AC currents and DC currents waveforms for TrSCC-DC-DC Operation B when* $\rho_g = 2$

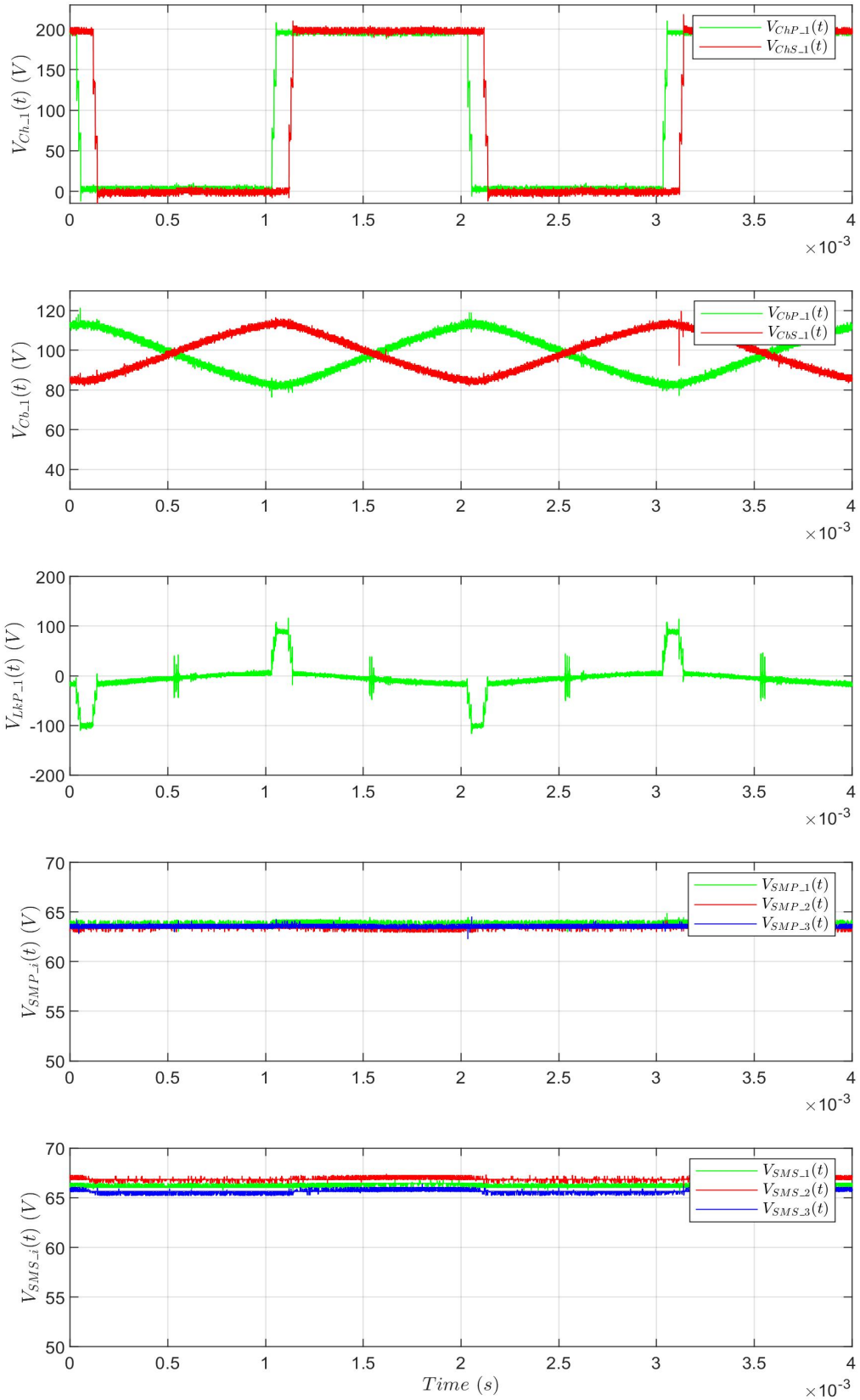


Figure 8.32: *Practical results of phase 1 chain-link voltages, blocking capacitor voltages, primary tank inductor voltage, primary and secondary SM voltages for TrSCC-DC-DC operation B when* $\rho_g = 2$

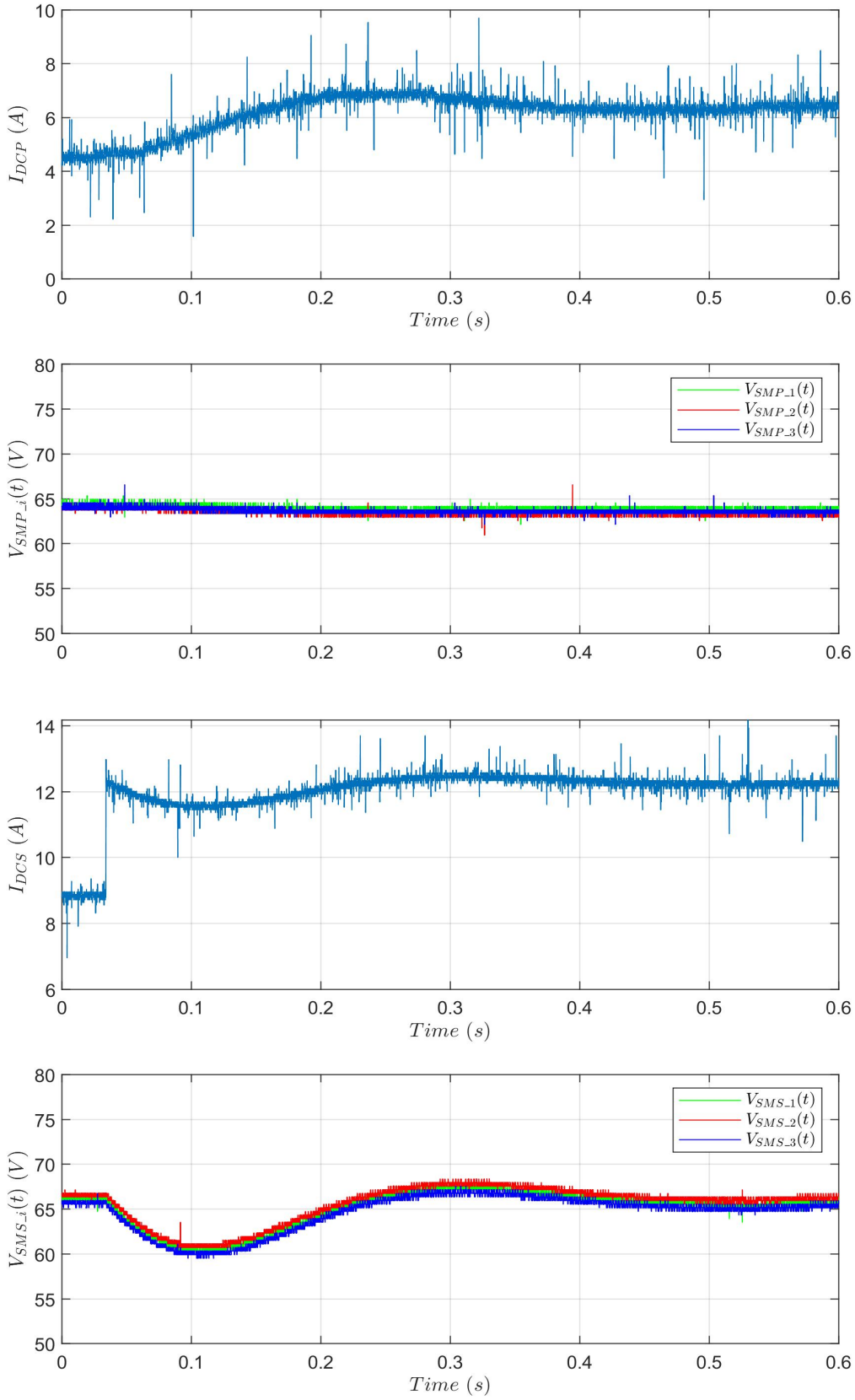


Figure 8.33: *Practical results of primary DC current, phase 1 primary SM capacitor voltages, secondary DC current and phase 1 secondary SM capacitor voltages for TrSCC-DC-DC under operational mode B with* $\rho_g = 2$ *and a step load from 1.8kW to 2.5kW*

8.7 Summary

This chapter briefly described the configuration of the experimental set up for both TrMMC and TrSCC-DC-DC converters. It also describes the master-slave control architecture of the rig that is used for experimental validation. This chapter mainly focused on the experimental results which are presented to validate the operation of the TrMMC and TrSCC-DC-DC converters. The experimental prototype is operated at a power equal to 2.8 kW for TrSCC-DC-DC converter operational modes A and B and it is operated at a power level of 2.5kW for operational mode C. The TrMMC prototype is tested at the power of 2.6kW. Simulation results from the PLECS software environment for the TrMMC and TrSCC-DC-DC converters using the same ratings as the experimental system are also shown. The transient response of the TrSCC-DC-DC is demonstrated to verify the total power flow control and dynamic responses for the TrSCC-DC-DC under each operational mode. Overall, the results from the experimental work match with the simulation results well, and therefore also validate the converter topologies, trapezoidal wave-shaping approach and operational modes discussed in Chapters 4 and 6.

Chapter 9

Conclusions

In high voltage direct current (HVDC) grids and multi-terminal HVDC systems, high voltage DC-DC converters are required to interconnect existing point to point HVDC systems to eachother, especially when they operate at different voltage levels, with different station technologies and using different grounding schemes. High Voltage DC/DC converters can also be used to support voltage regulation techniques and implement isolation between different HVDC systems. There are many modular multilevel DC-DC converter topologies that have been proposed in literature to meet these objectives. However, the control complexity defined by the series connection of large numbers of modules, minimisation of energy storage, increase of power density, requirements for DC fault blocking capability and the minimisation of $\frac{dv}{dt}$ stress effects on transformer insulation have led to the development of other approaches.

Since the introduction of the MMC, novel modular multilevel DC-DC converters have been proposed to adapt the original concept to other applications. Recently, a new breed of MMC-DC-DC converters, utilising trapezoidal waveform operation, have been proposed to achieve low energy storage requirement and use a lower number of submodules. Chapter 3 reviewed the recent work in the trapezoidal operation of MMC-DC-DC converters which were based on the parallel connected chain-links, where the lower number of submodules could be used by either reduc-

ing the converter modularity or by allowing the switching devices to experience an unacceptably high current stress under DC fault conditions. The most promising topology among those reviewed provides modularity with a low energy storage requirement but the same number of submodules, lower semiconductor device utilisation, and a higher device current stress under DC fault conditions when compared to standard sinusoidal operation of the MMC-DC-DC.

The work in this thesis presents a MMC-DC-DC converter operating with trapezoidal modulation which has an improved device utilisation and lower DC fault device current stress in addition to low energy storage requirement. The proposed MTrMMC-DC-DC control methodology is based on the operation around the resonant frequency of the equivalent capacitance of a converter arm and the corresponding arm inductance. This resonant operation allows the current to conduct continuously in the arm and as a result both switches in the half bridge submodules are utilised. The devices are also rated at lower current and the zero current soft switching of one of the switches is naturally achieved. Furthermore, the approach applies the sorting and switching of the submodules at the fundamental frequency, reducing both the switching losses and the control complexity of the converter.

A capacitor submodule voltage balancing method utilising a new energy control approach has been proposed to operate the converter safely under different operating conditions. An 800MW MTrMMC-DC-DC simulation was developed in the PLECS simulation software environment allowing the control methodology to be investigated. To validate the results of the simulation, a 2.6kW laboratory-scaled prototype MTrMMC was built and tested practically to prove the effectiveness of the proposed MTrMMC-DC-DC operation and capacitor submodule voltage balancing method.

High $\frac{dv}{dt}$ values, which can impact transformer insulation lifetime, high number of SMs resulting in complex control implementation and operation at low AC link fre-

quencies, resulting in high converter footprints, are common issues with MTrMMC-DC-DC and other converters proposed in literature which utilise trapezoidal modulation. In order to attempt to solve these issues a novel modular multilevel DC-DC converter, based on the series connection of converter chain-links, has been proposed in this work.

The modular multilevel Series Chain-link Converter, SCC, was previously introduced by researchers at the University of Nottingham for a three-phase $50Hz$, AC/DC converter. The SCC converter includes a transverse chain-link comprised of H-bridge submodules in the AC link to achieve improved control of reactive power. However, since the reactive power control is not required in a DC-DC converter, the transverse chain-links can be eliminated and the passive components required in the converter can be designed to form a resonant circuit in order to reduce the energy storage requirements of the converter. Furthermore, the number of the phases have been increased and the impact of this reduces the energy storage requirement, $\frac{dv}{dt}$ stress on the transformer, device current ratings, semiconductor losses and the harmonic order in the converter DC voltage and DC current under various operational conditions.

A significant part of the work presented in this thesis was the implementation of the trapezoidal waveform operation of an SCC-DC-DC converter, TrSCC-DC-DC. Chapter 6 presents three possible trapezoidal SCC-DC-DC operational modes. The operation of the TrSCC-DC-DC at a high fundamental frequency was achieved with a lower $\frac{dv}{dt}$ voltage stress across the transformers, a lower number of submodules, lower energy storage requirement, and lower semiconductor VA requirement than the other addressed converters. For instance, operation of the TrSCC-DC-DC at $f_o = 1kHz$ and with $N_{phase} = 20$ phases, provides a 66% reduction in the number of submodules, a 50% reduction in the $\frac{dv}{dt}$ voltage stress across the transformers, and a higher power density and lower energy storage requirement in comparison to the TrMMC-DC-DC and MTrMMC-DC-DC, considering the same T_d between voltage

level transitions.

The modelling of the TrSCC-DC-DC and the required expressions for the chain-link voltage, chain-link current, AC link current (tank current) and blocking capacitor voltage have been determined, considering possible intervals at different phase shifts between the primary and secondary chain-link voltages. From the current and voltage expressions, the energy storage requirements, semiconductor power losses and semiconductor area requirements (device *VA*) have been theoretically and numerically obtained at an optimum operating condition. A comprehensive comparison between all TrSCC-DC-DC operational modes has been presented and promising performance under all these modes has been realised when using a high number of phases, $N_{phases} \gtrapprox 20$. A TrSCC-DC-DC under operational mode B was found to be the most promising since it provides a lower energy storage requirement whilst using a lower number of phases in comparison to operational mode C, and provides more effective harmonic cancellation in the overall chain-link voltage when compared to operational mode A. In modes B and C, the overall chain-link voltage, $\sum_{i=1}^{N_{phase}} V_{ChP\_i}(t)$, seen from DC side, contains harmonic ripple at $N_{phase} * f_o$ whilst under operation mode A the overall chain-link voltage contains harmonic ripple at $2 * f_o$.

The necessary control loops that safely operate the TrSCC-DC-DC converter under different conditions have been demonstrated and a peak to peak voltage ripple across the submodule capacitors of $\delta_{pp} \leq 5\%$ with respect to nominal submodules voltage was achieved. It was also shown that implementing the total power flow and the capacitor submodule voltage balancing methods was enough to operate the converter safely in case of a slow transient in power demand.

Steady-state operation, transient responses and DC fault response capabilities for all of the TrSCC-DC-DC converter modes have been demonstrated using simulation results for HVDC systems which were developed in the PLECS simulation

software for both a unity DC and higher DC voltage gain ($\rho_g = 5$).

A 2.8kW laboratory-scale prototype TrSCC-DC-DC with 4 phases was built and tested practically. Experimental results have been presented to validate the proposed TrSCC-DC-DC converter under various operational modes.

9.1 Summary of achievements

The main achievements of this research work can be summarised as follows:

- Analysis and design of the most promising proposed topology in literature, trapezoidal operation of a modular multilevel DC-DC converter, TrMMC-DC-DC, and identifying the challenges associated with the TrMMC-DC-DC such as the control complexity due to high number of SMs (2400) and the requirements of sorting the SM capacitor voltages at a high frequency ($\gtrapprox 33kHz$), the requirement of a high current rating of the devices ($VA_{TrMMC} = 13$) due to the discontinuous current in the arm, poor SM device utilisation which leads to a complex cooling requirement for the SM devices, and a high $\frac{dv}{dt}$ stress across the transformer insulation ($\frac{dv}{dt} = 16kV$)

- Proposal of a modified trapezoidal operation for an MMC-DC-DC, MTrMMC-DC-DC, which reduces the control complexity by reducing the sorting of the SM capacitor voltages at the fundamental frequency ($250Hz$), reduces the requirement of the current rating of the devices ($VA_{MTrMMC} = 10$) due to the continuous current in the arm and provides a better SM device utilisation

- The identification of the optimum operating region of an MTrMMC-DC-DC converter which achieves low energy storage requirement whilst making the converter arm currents continuous and thus achieving better devices utilisation, is presented

- Identifying the challenges of the MTrMMC-DC-DC where a high number of SMs (2400) is required and a high $\frac{dv}{dt} = 16kV$ stress across the transformer insulation can be noticed

- Proposal of a new modular DC-DC converter topology, the TrSCC-DC-DC converter, which has a reduced number of submodules and converter complexity

- The presentation of three trapezoidal waveform arrangements for a TrSCC-DC-DC converter which reduce semiconductor current ratings ($VA_{TrSCC} = 9.23$), $\frac{dv}{dt}$ voltage stress on the transformer insulation ($\frac{dv}{dt} = 8kV$), and energy requirements ($H_{CTrSCC} = 4.9ms$)

- Identification of the optimum operation region of a TrSCC-DC-DC converter in order to achieve low energy storage requirement

- A comprehensive comparison between the three trapezoidal operational modes of an SCC-DC-DC converter with respect to energy storage requirement, semiconductor current stress, device current rating and resonant tank component ratings and identifying that TrSCC-DC-DC mode B is the most promising operating mode

- A comprehensive comparison between a sinusoidal MMC-DC-DC, TrMMC-DC-DC, sinusoidal SCC-DC-DC and TrSCC-DC-DC converters in terms of energy storage requirement, $\frac{dv}{dt}$ voltage stress on the transformer insulation, semiconductor power losses, semiconductor current rating, device utilisation and DC fault capability responses

- Proposal of a new capacitor submodule voltage balancing method which adapts with the trapezoidal wave-shaping

- Proposal of a new energy control method for trapezoidal operation of a modular multilevel converter

9.2 Future work

The following points have been identified by the author as areas that would have been further developed given more time in the project. As such they represent areas in which the work can be further advanced:

- The optimum analysis and design, with respect to efficiency for a three phase transformer which is designed to operate with the trapezoidal wave-shaping of the MTrMMC-DC-DC.
- The design and analysis of the cooling system required for the three phase transformer used in the MTrMMC-DC-DC converter in an effort to improve, and potentially optimise, the overall power density of the converter
- The design and analysis of a single phase transformer for a TrSCC-DC-DC converter operating with trapezoidal waveforms so as to allow the estimation of the overall efficiency of the TrSCC-DC-DC converter
- A study the effects of increasing the number of phases and the operating frequency of the single phase transformer required for the TrSCC-DC-DC converter with trapezoidal waveforms in an effort to find and optimum with regards to efficiency and power density.
- The design and analysis of the cooling system requirements for the single phase transformer used in the TrSCC-DC-DC converter so as to allow the estimation of the overall efficiency and power density of the converter
- The design and analysis of the cooling system requirements for the submodule devices in all addressed modular multilevel DC-DC converters so as to allow the estimation of the overall power density of the converters
- A detailed investigation of the DC fault blocking capabilities of the MTrMMC-DC-DC and TrSCC-DC-DC converters under different fault conditions (e.g., pole-to-ground and pole-to-pole, considering different fault locations).

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Appendix A

Calculations of the tank current and equivalent DC blocking capacitor voltage of TrSCC-DC-DC

A.1 Cases X and Y

The current response comprises two parts where the first part of the current, $i'_{ac}(t)$, is due to the response of the tank to the tank voltage, $v_T(t)$, with zero initial conditions for the inductor current and capacitor voltage, $i_{ac}(0) = 0$ and $v_{cb}(0) = 0$. The second part of the tank current is due to the response of the tank passive components initial conditions, $i_{ac}(0) = I_0$ and $v_{cb}(0) = V_0$, considering zero tank voltage, $v_T(0) = 0$. By taking the Laplace transform of the AC equivalent circuit as shown in figure A.1-b and simply finding the total impedance in frequency domain, $Z_T(s) = \frac{sC_b}{1+s^2L_kC_b}$, the first part of the tank current can be found in frequency domain, $I'_{ac}(s)$. Then, by taking the inverse Laplace transform of the $I'_{ac}(s)$, the first part of the AC link current, $i'_{ac}(ts)$, can be found in time domain as shown in figure A.2.

A.1.1 Tank response to input voltage with zero initial conditions for cases X and Y

The tank voltage waveform shown in figure A.1-a and represented the cases X and Y, can be expressed in time domain as equation A.1. Equation A.2 describes the Laplace transform of the tank voltage. Considering equation A.3 and following the equations A.4-A.6 the main equation for the $i'_{ac}(t)$ was found and the full $i'_{ac}(t)$ can be composed by considering the delays in the time domain and $T_{sh} \leq \frac{T}{2} - T_t$ as shown in equation A.7.

$$v_T(t) = m(t - (t - t_1) - (t - t_2) + (t - t_3)) \tag{A.1}$$

$$v_T(s) = m(\frac{1}{s^2} - \frac{1}{s^2}e^{-st_1} - \frac{1}{s^2}e^{-st_2} + \frac{1}{s^2}e^{-st_3}) \tag{A.2}$$

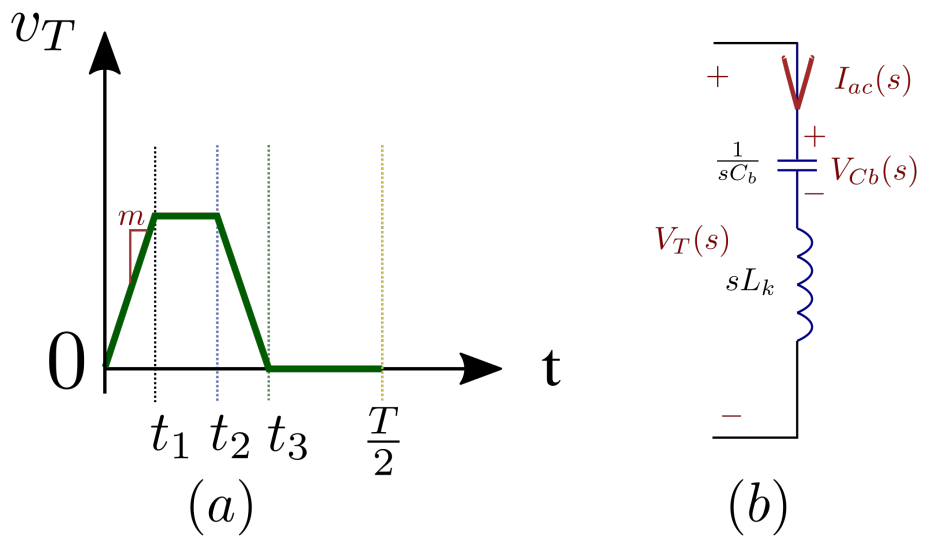


Figure A.1: *(a) General tank voltage of cases X and Y (b) Laplace transform of the per-phase AC equivalent circuit*

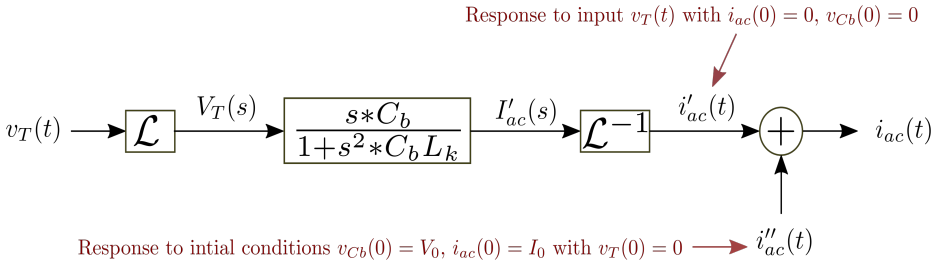


Figure A.2: *Tank current parts*

$$T(s) = \frac{1}{s^2} e^{-st \text{ with } t=0,t_1,t_2,t_3} \tag{A.3}$$

$$\begin{aligned} G(s) &= \frac{1}{s^2} e^{-st\frac{sC_b}{s^2C_bL_k}} \\ &= \frac{1}{s} e^{-st\frac{C_b}{s^2C_bL_k}} \text{ where } e^{-st}\text{: Just a delay in the time domain} \\ &= \frac{1}{s}\frac{C_b}{s^2C_bL_k} \end{aligned} \tag{A.4}$$

$$\begin{aligned}
\mathscr{L}^{-1}(G(s)) &= \mathscr{L}^{-1}(\frac{1}{s}\frac{C_b}{s^2 C_b L_k}) \text{ where } \omega_{r1}^2 = \frac{1}{L_k C_b} \\
&= \mathscr{L}^{-1}(\frac{1}{s}\frac{C_b}{\frac{s^2}{\omega_{r1}^2}}) \\
&= \mathscr{L}^{-1}(\frac{1}{s}\frac{\omega_{r1}^2 C_b}{s^2+\omega_{r1}^2}) \\
&= \mathscr{L}^{-1}(\frac{1}{s}\frac{1}{L_k}\frac{1}{s^2+\omega_{r1}^2}) \\
&= \frac{1}{L_k}\mathscr{L}^{-1}(\frac{A}{s}+\frac{Bs+C}{s^2+\omega_{r1}^2}) \\
&= \frac{1}{L_k}\mathscr{L}^{-1}(\frac{As^2+A\omega_{r1}^2+Bs^2+Cs}{s(s^2+\omega_{r1}^2)})
\end{aligned} \tag{A.5}$$

$$\begin{aligned}
\mathscr{L}^{-1}(G(s)) &= \frac{1}{L_k}\mathscr{L}^{-1}(\frac{1}{s\omega_{r1}^2}-\frac{\frac{s}{\omega_{r1}^2}}{s^2+\omega_{r1}^2}) \\
&= \frac{1}{L_k\omega_{r1}^2}\mathscr{L}^{-1}(\frac{1}{s}-\frac{s}{s^2+\omega_{r1}^2}) \\
&= C_b(1-\cos(\omega_{r1}t))
\end{aligned} \tag{A.6}$$

$$\begin{aligned}
i'_{ac}(t) = mC_b\Big\{&(1-\cos(\omega_{r1}t))-(1-\cos(\omega_{r1}(t-t_1)))-(1-\cos(\omega_{r1}(t-t_2))) \\
&+(1-\cos(\omega_{r1}(t-t_3)))\Big\} \text{ for } 0<t<\frac{T}{2}
\end{aligned} \tag{A.7}$$

The full first part of the capacitor tank voltage, $v'_{Cb}(t)$, can be found by taking the integral of the first part of the tank current, $i'_{ac}(t)$, as shown in equation A.8 considering $T_{sh} \leq \frac{T}{2} - T_t$.

$$\begin{aligned}
v'_{Cb}(t) &= \frac{1}{C_b}\int i'_{ac}(t)dt \\
&= m\big\{(t-\frac{1}{\omega_{r1}}\sin(\omega_{r1}t))-((t-t_1)-\frac{1}{\omega_{r1}}\sin(\omega_{r1}(t-t_1))) \\
&-((t-t_2)-\frac{1}{\omega_{r1}}\sin(\omega_{r1}(t-t_2)))+((t-t_3)-\frac{1}{\omega_{r1}}\sin(\omega_{r1}(t-t_3)))\big\} \\
&\text{for } 0<t<\frac{T}{2}
\end{aligned} \tag{A.8}$$

A.1.2 Tank response to initial conditions with zero input voltage to the tank for cases X and Y

The second part of the inductor current (tank current), $i''_{ac}(t)$, and capacitor voltage, $v''_{Cb}(t)$ can be found by looking at the state space model of the resonant equivalent circuit as shown in equations A.9 and A.10.

$$\frac{di''_{ac}(t)}{dt} = -\frac{1}{L_k} v_{Cb}(t) \tag{A.9}$$

$$\frac{dv''_{Cb}(t)}{dt} = \frac{1}{C_b} i_{ac}(t) \tag{A.10}$$

Then, taking the Laplace transform of the second part of both the tank current, $i''_{ac}(t)$, and capacitor voltage, $v''_{Cb}(t)$, as equations A.11 and A.12, respectively, where $I_0 = i_{ac}(0)$ and $V_0 = v_{Cb}(0)$ are the initial values of the inductor current and the capacitor voltage considering zero input voltage, $V_T(0) = 0$.

$$sI''_{ac}(s) - I_0 = -\frac{1}{L_k} V''_{Cb}(s) \tag{A.11}$$

$$\begin{aligned} &sv''_{Cb}(s) - V_0 = \frac{1}{C_b} i''_{ac}(s) \\ &s^2 v''_{Cb}(s) - sV_0 = \frac{s}{C_b} i''_{ac}(s) \textit{ multiply both sides by } C_b \textit{ and rearrange it} \\ &-sI''_{ac}(s) = sC_bV_0 - s^2 C_b V''_{Cb}(s) \end{aligned} \tag{A.12}$$

By adding the equations A.11 and A.12, the expression for independent state $V''_{cb}(s)$ can be found as described in equation A.14. Then, the second part time domain of the capacitor voltage, $v''_{cb}(t)$, is found by taking the inverse Laplace transform of $V''_{cb}(s)$ as equation A.14. The second part time domain of the tank current, $i''_{ac}(t)$, is found by substituting the equation A.14 into equation A.10 and the result is determined as equation A.15.

$$\begin{aligned} &sC_bV_0 - V''_{cb}(s)\left(\frac{1}{L_k} + s^2 C_b\right) = -I_0 \textit{ multiply both sides by } L_k \textit{ and rearrange it} \\ V''_{cb}(s) &= \frac{sL_kC_bV_0}{1 + s^2 L_k C_b} + \frac{L_k I_0}{1 + s^2 L_k C_b} \\ &= V_0 \frac{s}{s^2 + \omega_{r1}^2} + \omega_{r1} L_k I_0 \frac{\omega_{r1}}{s^2 + \omega_{r1}^2} \end{aligned} \tag{A.13}$$

$$\begin{aligned} v''_{cb}(t) &= \mathscr{L}^{-1}(V''_{cb}(s)) \\ &= V_0 \cos(\omega_{r1} t) + \omega_{r1} L_k I_0 \sin(\omega_{r1} t) \end{aligned} \tag{A.14}$$

$$\begin{aligned} i''_{ac}(t) &= -V_0 \omega_{r1} C_b \sin(\omega_{r1} t) + \omega_{r1}^2 L_k C_b I_0 \cos(\omega_{r1} t) \\ &= -V_0 \omega_{r1} C_b \sin(\omega_{r1} t) + I_0 \cos(\omega_{r1} t) \end{aligned} \tag{A.15}$$

The full tank current shown in equation A.16, $i_{ac}(t)$, comprises the parts which were found in equations A.7 and A.15 considering $T_{sh} \leq \frac{T}{2} - T_t$. Similarly, the full capacitor voltage, $v_{cb}(t)$, consists of the parts which were determined in equations A.8 and A.14 considering $T_{sh} \leq \frac{T}{2} - T_t$. The initial conditions for the tank current (inductor current), I_0, and capacitor voltage, V_0, are unknown up to this stage since only half of the period was considered until this point due to the symmetrical waveforms of both tank voltage and tank current.

$$i_{ac}(t) = i'_{ac}(t) + i''_{ac}(t) \text{ where } V_0 \text{ and } I_0 \text{ are unknown} \tag{A.16}$$

$$v_{Cb}(t) = v'_{Cb}(t) + v''_{Cb}(t) \text{ where } V_0 \text{ and } I_0 \text{ are unknown} \tag{A.17}$$

Considering the symmetry about X-axis of both tank current and capacitor voltage, the equations A.18 and A.19 can be applied. As a result, the full steady state waveform of both the inductor current and capacitor voltage can be obtained by only analysing the first half of the period. Following the equations A.20-A.23, the initial conditions for the tank current (inductor current), I_0, and the capacitor voltage, V_0 can be found where the colour of the functions, f_a, f_b, f_c, f_d, f_e and f_f in the equations A.20-A.21 represents the portion of the equation with the correspondent colour. Substituting I_0 and V_0 in the equations A.16 and A.17 the instantaneous tank current, $i_{ac}(t)$, and the instantaneous equivalent blocking capacitor voltage, $v_{cb}(t)$,can be obtained as equations A.24 and A.25, respectively.

$$i_{ac}(t=0) = -i_{ac}(t=\frac{T}{2}) \tag{A.18}$$

$$v_{Cb}(t=0) = -v_{Cb}(t=\frac{T}{2}) \tag{A.19}$$

$$\begin{aligned} I_0 = {} & mC_b\Big\{\cos(\omega_{r1}\frac{T}{2}) - \cos\left(\omega_{r1}(\frac{T}{2}-t_1)\right) \\ & - \cos\left(\omega_{r1}(\frac{T}{2}-t_2)\right) + \cos\left(\omega_{r1}(\frac{T}{2}-t_3)\right)\Big\} \\ & + V_0\omega_{r1}C_b\sin(\omega_{r1}\frac{T}{2}) - I_0\cos(\omega_{r1}\frac{T}{2}) \\ = {} & f_a + f_bV_0 + f_cI_0 \end{aligned} \tag{A.20}$$

$$\begin{aligned} V_0 = {} & m\Big\{-\frac{T}{2} + (\frac{T}{2}-t_1) + (\frac{T}{2}-t_2) - (\frac{T}{2}-t_3) \\ & + \frac{1}{\omega_{r1}}\sin(\omega_{r1}\frac{T}{2}) - \frac{1}{\omega_{r1}}\sin\left(\omega_{r1}(\frac{T}{2}-t_1)\right) \\ & - \frac{1}{\omega_{r1}}\sin\left(\omega_{r1}(\frac{T}{2}-t_2)\right) + \frac{1}{\omega_{r1}}\sin\left(\omega_{r1}(\frac{T}{2}-t_3)\right)\Big\} \\ & - V_0\cos(\omega_{r1}\frac{T}{2}) - I_0\omega_{r1}L_k\sin(\omega_{r1}\frac{T}{2}) \\ = {} & f_d + f_eV_0 + f_fI_0 \end{aligned} \tag{A.21}$$

$$V_0 = \frac{f_d + f_fI_0}{1 - f_e}$$

$$I_0 = \frac{(1-f_e)f_a + f_bf_d}{(1-f_c)(1-f_e) - f_bf_f} \tag{A.22}$$

$$V_0 = \frac{(1-f_c)f_d + f_ff_a}{(1-f_c)(1-f_e) - f_bf_f} \tag{A.23}$$

$$i_{ac}(t) = mC_b\Big\{(1-\cos(\omega_{r1}t)) - (1-\cos(\omega_{r1}(t-t_1))) - (1-\cos(\omega_{r1}(t-t_2))) + (1-\cos(\omega_{r1}(t-t_3)))\Big\} - \frac{(1-f_c)f_d + f_f f_a}{(1-f_c)(1-f_e) - f_b f_f}\omega_{r1}C_b\sin(\omega_{r1}t) + \Big(\frac{(1-f_e)f_a + f_b f_d}{(1-f_c)(1-f_e) - f_b f_f}\Big)\cos(\omega_{r1}t) \tag{A.24}$$

$$v_{cb}(t) = m\Big\{(t - \frac{1}{\omega_{r1}}\sin(\omega_{r1}t)) - ((t-t_1) - \frac{1}{\omega_{r1}}\sin(\omega_{r1}(t-t_1))) - ((t-t_2) - \frac{1}{\omega_{r1}}\sin(\omega_{r1}(t-t_2))) + ((t-t_3) - \frac{1}{\omega_{r1}}\sin(\omega_{r1}(t-t_3)))\Big\} + \Big(\frac{(1-f_c)f_d + f_f f_a}{(1-f_c)(1-f_e) - f_b f_f}\Big)\cos(\omega_{r1}t) + \omega_{r1}L_k\Big(\frac{(1-f_e)f_a + f_b f_d}{(1-f_c)(1-f_e) - f_b f_f}\Big)\sin(\omega_{r1}t) \tag{A.25}$$

A.2 Case Z

A.2.1 Tank response to input voltage with zero initial conditions for case Z

The time domain and the frequency domain of the tank voltage are represented in equations A.26 and A.27, respectively. Following the similar approach as shown for cases X and Y, the first part of the current was found as equation A.28 for case Z, considering $0 < t < \frac{T}{2}$.

$$v_T(t) = 2mt - m(t-t_1) - m(t-t_2) - m(t-t_3) - m(t-t_4) \tag{A.26}$$

$$v_T(s) = m\Big(\frac{2}{s^2} - \frac{1}{s^2}e^{-st_1} - \frac{1}{s^2}e^{-st_2} - \frac{1}{s^2}e^{-st_3} - \frac{1}{s^2}e^{-st_4}\Big) \tag{A.27}$$

$$i'_{ac}(t) = mC_b\Big\{2(1-\cos(\omega_{r1}t)) - (1-\cos(\omega_{r1}(t-t_1))) - (1-\cos(\omega_{r1}(t-t_2))) - (1-\cos(\omega_{r1}(t-t_3))) - (1-\cos(\omega_{r1}(t-t_4)))\Big\} \; for \; 0 < t < \frac{T}{2} \tag{A.28}$$

Taking the integral of the first part of the tank current, $i'_{ac}(t)$, provides the first part of the capacitor tank voltage, $v'_{Cb}(t)$, as equation A.29 considering $\frac{T}{2} - T_t < T_{sh} \leq \frac{T}{2}$.

$$
\begin{aligned}
v'_{Cb}(t) &= \frac{1}{C_b}\int i'_{ac}(t)dt \\
&= m\Big\{(2t - \frac{1}{\omega_{r1}}\sin(\omega_{r1}t)) - ((t-t_1) - \frac{1}{\omega_{r1}}\sin(\omega_{r1}(t-t_1))) \\
&- ((t-t_2) - \frac{1}{\omega_{r1}}\sin(\omega_{r1}(t-t_2))) - ((t-t_3) - \frac{1}{\omega_{r1}}\sin(\omega_{r1}(t-t_3))) \\
&- ((t-t_4) - \frac{1}{\omega_{r1}}\sin(\omega_{r1}(t-t_4)))\Big\} \; for \; 0 < t < \frac{T}{2}
\end{aligned}
\tag{A.29}
$$

A.2.2 Tank response to initial conditions with zero input voltage to the tank for case Z

The second part of the inductor current (tank current), $i''_{ac}(t)$, and the capacitor voltage, $v''_{Cb}(t)$ for case Z can be found by following the equations A.9-A.19 which were previously presented for cases X and Y. The initial conditions for the tank current (inductor current), I_0, and capacitor voltage, V_0 were found as described in equations A.30-A.33 where the colour of the functions, f_g, f_b, f_c, f_p, f_e and f_f in the equations A.30-A.31 represents the portion of the equation with the correspondent colour. Equations A.34 and A.35 show the instantaneous tank current, $i_{ac}(t)$, and instantaneous equivalent blocking capacitor voltage, $v_{cb}(t)$, respectively, considering case Z in figure 6.9.

$$
\begin{aligned}
I_0 &= mC_b\Big\{2 + 2\cos(\omega_{r1}\frac{T}{2}) - \cos\left(\omega_{r1}(\frac{T}{2} - t_1)\right) \\
&- \cos\left(\omega_{r1}(\frac{T}{2} - t_2)\right) - \cos\left(\omega_{r1}(\frac{T}{2} - t_3)\right) \\
&- \cos\left(\omega_{r1}(\frac{T}{2} - t_4)\right)\Big\} + V_0\omega_{r1}C_b\sin(\omega_{r1}\frac{T}{2}) - I_0\cos(\omega_{r1}\frac{T}{2}) \\
&= f_g + f_bV_0 + f_cI_0
\end{aligned}
\tag{A.30}
$$

$$
\begin{aligned}
V_0 &= m\Big\{-2\frac{T}{2} + (\frac{T}{2} - t_1) + (\frac{T}{2} - t_2) + (\frac{T}{2} - t_3) + +(\frac{T}{2} - t_4) \\
&+ \frac{2}{\omega_{r1}}\sin(\omega_{r1}\frac{T}{2}) - \frac{1}{\omega_{r1}}\sin\left(\omega_{r1}(\frac{T}{2} - t_1)\right) \\
&- \frac{1}{\omega_{r1}}\sin\left(\omega_{r1}(\frac{T}{2} - t_2)\right) - \frac{1}{\omega_{r1}}\sin\left(\omega_{r1}(\frac{T}{2} - t_3)\right) \\
&- \frac{1}{\omega_{r1}}\sin\left(\omega_{r1}(\frac{T}{2} - t_4)\right)\Big\} - V_0\cos(\omega_{r1}\frac{T}{2}) - I_0\omega_{r1}L_k\sin(\omega_{r1}\frac{T}{2}) \\
&= f_p + f_eV_0 + f_fI_0 \\
V_0 &= \frac{f_p + f_fI_0}{1 - f_e}
\end{aligned}
\tag{A.31}
$$

$$
I_0 = \frac{(1-f_e)f_g + f_bf_p}{(1-f_c)(1-f_e) - f_bf_f} \tag{A.32}
$$

$$
V_0 = \frac{(1-f_c)f_p + f_ff_g}{(1-f_c)(1-f_e) - f_bf_f} \tag{A.33}
$$

$$
\begin{aligned}
i_{ac}(t) = mC_b\Big\{ & 2(1-\cos(\omega_{r1}t)) - (1-\cos(\omega_{r1}(t-t_1))) - (1-\cos(\omega_{r1}(t-t_2))) \\
& - (1-\cos(\omega_{r1}(t-t_3))) - (1-\cos(\omega_{r1}(t-t_4)))\Big\} \\
& - (\frac{(1-f_c)f_p + f_f f_g}{(1-f_c)(1-f_e) - f_b f_f})\omega_{r1}C_b \sin(\omega_{r1}t) \\
& + (\frac{(1-f_e)f_g + f_b f_p}{(1-f_c)(1-f_e) - f_b f_f})\cos(\omega_{r1}t)
\end{aligned}
\tag{A.34}
$$

$$
\begin{aligned}
v_{Cb}(t) = m\big\{ & (2t - \frac{1}{\omega_{r1}}\sin(\omega_{r1}t)) - ((t-t_1) - \frac{1}{\omega_{r1}}\sin(\omega_{r1}(t-t_1))) \\
& - ((t-t_2) - \frac{1}{\omega_{r1}}\sin(\omega_{r1}(t-t_2))) - ((t-t_3) - \frac{1}{\omega_{r1}}\sin(\omega_{r1}(t-t_3))) \\
& - ((t-t_4) - \frac{1}{\omega_{r1}}\sin(\omega_{r1}(t-t_4)))\big\} + (\frac{(1-f_c)f_p + f_f f_g}{(1-f_c)(1-f_e) - f_b f_f})\cos(\omega_{r1}t) \\
& + \omega_{r1}L_k(\frac{(1-f_e)f_g + f_b f_p}{(1-f_c)(1-f_e) - f_b f_f})\sin(\omega_{r1}t)
\end{aligned}
\tag{A.35}
$$

A.3 phase 1 primary instantaneous chain-link power

Table A.1: phase 1 primary Chain-link power when $0 \leq T_{sh} < T_t$ (case X)

t	$P_{ChP\_1}(t)$	
$0 \leq t < T_{sh}$	$(2V_{DCP}t(4I_0cos(\omega_r T_t) - 4I_0 - 4C_b mcos(\omega_r T_t) + 4C_b mcos(\omega_r(T_{sh} - T_t)) + 2C_b V_0 \omega_r^2 T_t + 2C_b \omega_r^2 mT_{sh}^2 - 4C_b V_0 \omega_r sin(\omega_r T_t) + 2I_0 \omega_r T_t sin((T\omega_r)/2) - 2C_b \omega_r mT_t sin((T\omega_r)/2) + 2C_b \omega_r mT_t sin((\omega_r(T - 2T_{sh}))/2) + 2C_b \omega_r mT_t sin((\omega_r(T - 2T_t))/2) - C_b T\omega_r^2 mT_t + 2C_b V_0 \omega_r^2 T_t cos((T\omega_r)/2) - 4C_b \omega_r^2 mT_{sh}T_t - I_0 T\omega_r^2 T_t cos(\omega_r t) + 2C_b \omega_r mT_t sin((\omega_r(2T_{sh} - T + 2T_t))/2) + C_b TV_0 \omega_r^3 T_t sin(\omega_r t) + C_b T\omega_r^2 mT_t cos(\omega_r t)))(N_{phase} T\omega_r^2 T_t^2)$	(A.36)
$T_{sh} \leq t < T_t$	$(2V_{DCP}t(4I_0cos(\omega_r T_t) - 4I_0 - 4C_b mcos(\omega_r T_t) + 4C_b mcos(\omega_r(T_{sh} - T_t)) + 2C_b V_0 \omega_r^2 T_t + 2C_b \omega_r^2 mT_{sh}^2 - 4C_b V_0 \omega_r sin(\omega_r T_t) + 2I_0 \omega_r T_t sin((T\omega_r)/2) - 2C_b \omega_r mT_t sin((T\omega_r)/2) + 2C_b \omega_r mT_t sin((\omega_r(T - 2T_{sh}))/2) + 2C_b \omega_r mT_t sin((\omega_r(T - 2T_t))/2) + 2C_b V_0 \omega_r^2 T_t cos((T\omega_r)/2) - 4C_b \omega_r^2 mT_{sh}T_t - I_0 T\omega_r^2 T_t cos(\omega_r t) + 2C_b \omega_r mT_t sin((\omega_r(2T_{sh} - T + 2T_t))/2) + C_b TV_0 \omega_r^3 T_t sin(\omega_r t) + C_b T\omega_r^2 mT_t cos(\omega_r t) - C_b T\omega_r^2 mT_t cos(\omega_r(t - T_{sh}))))/(N_{phase} T\omega_r^2 T_t^2)$	(A.37)
$T_t \leq t < T_t + T_{sh}$	$(2V_{DCP}(4I_0cos(\omega_r T_t) - 4I_0 - 4C_b mcos(\omega_r T_t) + 4C_b mcos(\omega_r(T_{sh} - T_t)) + 2C_b V_0 \omega_r^2 T_t + 2C_b \omega_r^2 mT_{sh}^2 - 4C_b V_0 \omega_r sin(\omega_r T_t) + 2I_0 \omega_r T_t sin((T\omega_r)/2) - 2C_b \omega_r mT_t sin((T\omega_r)/2) + 2C_b \omega_r mT_t sin((\omega_r(T - 2T_{sh}))/2) + 2C_b \omega_r mT_t sin((\omega_r(T - 2T_t))/2) + C_b T\omega_r^2 mT_t + 2C_b V_0 \omega_r^2 T_t cos((T\omega_r)/2) - 4C_b \omega_r^2 mT_{sh}T_t - I_0 T\omega_r^2 T_t cos(\omega_r t) + 2C_b \omega_r mT_t sin((\omega_r(2T_{sh} - T + 2T_t))/2) + C_b TV_0 \omega_r^3 T_t sin(\omega_r t) + C_b T\omega_r^2 mT_t cos(\omega_r t) - C_b T\omega_r^2 mT_t cos(\omega_r(t - T_{sh})) - C_b T\omega_r^2 mT_t cos(\omega_r(t - T_t))))/(N_{phase} T\omega_r^2 T_t)$	(A.38)
$T_t + T_{sh} \leq t < T/2$	$(2V_{DCP}(4I_0cos(\omega_r T_t) - 4I_0 - 4C_b mcos(\omega_r T_t) + 4C_b mcos(\omega_r(T_{sh} - T_t)) + 2C_b V_0 \omega_r^2 T_t + 2C_b \omega_r^2 mT_{sh}^2 - 4C_b V_0 \omega_r sin(\omega_r T_t) + 2I_0 \omega_r T_t sin((T\omega_r)/2) - 2C_b \omega_r mT_t sin((T\omega_r)/2) + 2C_b \omega_r mT_t sin((\omega_r(T - 2T_{sh}))/2) + 2C_b \omega_r mT_t sin((\omega_r(T - 2T_t))/2) + 2C_b V_0 \omega_r^2 T_t cos((T\omega_r)/2) - 4C_b \omega_r^2 mT_{sh}T_t - I_0 T\omega_r^2 T_t cos(\omega_r t) + 2C_b \omega_r mT_t sin((\omega_r(2T_{sh} - T + 2T_t))/2) + C_b TV_0 \omega_r^3 T_t sin(\omega_r t) + C_b T\omega_r^2 mT_t cos(\omega_r t) - C_b T\omega_r^2 mT_t cos(\omega_r(t - T_{sh})) - C_b T\omega_r^2 mT_t cos(\omega_r(t - T_t)) + C_b T\omega_r^2 mT_t cos(\omega_r(T_{sh} - t + T_t))))/(N_{phase} T\omega_r^2 T_t)$	(A.39)
$T/2 \leq t < T/2 + T_{sh}$	$(V_{DCP}(T - 2t + 2T_t)(4I_0cos(_t) - 4I_0 - 4C_b mcos(_t) + 4C_b mcos(\omega_r(T_{sh} - T_t)) + 2C_b V_0 \omega_r^2 T_t + 2C_b \omega_r^2 mT_{sh}^2 - 4C_b V_0 \omega_r sin(_t) + 2I_0 \omega_r T_t sin((T\omega_r)/2) - 2C_b \omega_r mT_t sin((T\omega_r)/2) + 2C_b \omega_r mT_t sin((\omega_r(T - 2T_{sh}))/2) + 2C_b \omega_r mT_t sin((\omega_r(T - 2T_t))/2) + C_b T\omega_r^2 mT_t + 2C_b V_0 \omega_r^2 T_t cos((T\omega_r)/2) - 4C_b \omega_r^2 mT_{sh}T_t - I_0 T\omega_r^2 T_t cos(\omega_r t) + 2C_b \omega_r mT_t sin((\omega_r(2T_{sh} - T + 2T_t))/2) + C_b TV_0 \omega_r^3 T_t sin(\omega_r t) + C_b T\omega_r^2 mT_t cos(\omega_r t) - C_b T\omega_r^2 mT_t cos(\omega_r(t - T_{sh})) - C_b T\omega_r^2 mT_t cos(\omega_r(t - T_t)) - C_b T\omega_r^2 mT_t cos(\omega_r(T/2 - t)) + C_b T\omega_r^2 mT_t cos(\omega_r(T_{sh} - t + T_t))))/(N_{phase} T\omega_r^2 T_t^2)$	(A.40)
$T/2 + T_{sh} \leq t < T/2 + T_t$	$(V_{DCP}(T - 2t + 2T_t)(4I_0cos(\omega_r T_t) - 4I_0 - 4C_b mcos(\omega_r T_t) + 4C_b mcos(\omega_r(T_{sh} - T_t)) + 2C_b V_0 \omega_r^2 T_t + 2C_b \omega_r^2 mT_{sh}^2 - 4C_b V_0 \omega_r sin(\omega_r T_t) + 2I_0 \omega_r T_t sin((T\omega_r)/2) - 2C_b \omega_r mT_t sin((T\omega_r)/2) + 2C_b \omega_r mT_t sin((\omega_r(T - 2T_{sh}))/2) + 2C_b \omega_r mT_t sin((\omega_r(T - 2T_t))/2) + 2C_b V_0 \omega_r^2 T_t cos((T\omega_r)/2) - 4C_b \omega_r^2 mT_{sh}T_t - I_0 T\omega_r^2 T_t cos(\omega_r t) + 2C_b \omega_r mT_t sin((\omega_r(2T_{sh} - T + 2T_t))/2) + C_b T\omega_r^2 mT_t cos(\omega_r(T/2 - t + T_{sh})) + C_b TV_0 \omega_r^3 T_t sin(\omega_r t) + C_b T\omega_r^2 mT_t cos(\omega_r t) - C_b T\omega_r^2 mT_t cos(\omega_r(t - T_{sh})) - C_b T\omega_r^2 mT_t cos(\omega_r(t - T_t)) - C_b T\omega_r^2 mT_t cos(\omega_r(T/2 - t)) + C_b T\omega_r^2 mT_t cos(\omega_r(T_{sh} - t + T_t))))/(N_{phase} T\omega_r^2 T_t^2)$	(A.41)
$t \geq T/2 + T_t$	0	(A.42)

Table A.2: Phase 1 primary instantaneous chain-link power when $T_t \leq T_{sh} < T/2 - T_t$ (case Y)

t	$P_{ChP\_1}(t)$	
$0 \leq t < T_t$	$(2V_{DCP}t(4I_0cos(\omega_r T_{sh}) - 4I_0 - 4C_b mcos(\omega_r T_{sh}) + 4C_b mcos(\omega_r(T_{sh} - T_{sh}))$ $+ 4I_0\omega_r T_{sh}sin(\omega_r T_{sh}) - 4I_0\omega_r T_t sin(\omega_r T_{sh}) + 2C_b V_0\omega_r^2 T_t - 2C_b\omega_r^2 mT_t^2$ $- 4C_b V_0\omega_r sin(\omega_r T_{sh}) + 2I_0\omega_r T_t sin((T\omega_r)/2) - 2C_b\omega_r mT_t sin((T\omega_r)/2)$ $- 4C_b\omega_r mT_{sh}sin(\omega_r T_{sh}) + 4C_b\omega_r mT_t sin(\omega_r T_{sh}) + 2C_b\omega_r mT_t sin((\omega_r(T - 2T_{sh}))/2)$ $+ 2C_b\omega_r mT_t sin((\omega_r(T - 2T_t))/2) - C_b T\omega_r^2 mT_t + 2C_b V_0\omega_r^2 T_t cos((T\omega_r)/2)$ $+ 4C_b\omega_r mT_{sh}sin(\omega_r(T_{sh} - T_{sh})) - 4C_b\omega_r mT_t sin(\omega_r(T_{sh} - T_{sh}))$ $+ 4C_b V_0\omega_r^2 T_{sh}cos(\omega_r T_{sh}) - 4C_b V_0\omega_r^2 T_t cos(\omega_r T_{sh}) - I_0 T\omega_r^2 T_t cos(\omega_r t)$ $+ 2C_b\omega_r mT_t sin((\omega_r(2T_{sh} - T + 2T_t))/2) + C_b TV_0\omega_r^3 T_t sin(\omega_r t)$ $+ C_b T\omega_r^2 mT_t cos(\omega_r t)))/(N_{phase}T\omega_r^2 T_t^2)$	(A.43)
$T_t \leq t < T_{sh}$	$(2V_{DCP}t(4I_0cos(\omega_r T_{sh}) - 4I_0 - 4C_b mcos(\omega_r T_{sh}) + 4C_b mcos(\omega_r(T_{sh} - T_t))$ $+ 4I_0\omega_r T_{sh}sin(\omega_r T_{sh}) - 4I_0\omega_r T_t sin(\omega_r T_{sh}) + 2C_b V_0\omega_r^2 T_t$ $- 2C_b\omega_r^2 mT_t^2 - 4C_b V_0\omega_r sin(\omega_r T_{sh}) + 2I_0\omega_r T_t sin((T\omega_r)/2)$ $- 2C_b\omega_r mT_t sin((T\omega_r)/2) - 4C_b\omega_r mT_{sh}sin(\omega_r T_{sh}) + 4C_b\omega_r mT_t sin(\omega_r T_{sh})$ $+ 2C_b\omega_r mT_t sin((\omega_r(T - 2T_{sh}))/2) + 2C_b\omega_r mT_t sin((\omega_r(T - 2T_t))/2)$ $+ 2C_b V_0\omega_r^2 T_t cos((T\omega_r)/2) + 4C_b\omega_r mT_{sh}sin(\omega_r(T_{sh} - T_t)) - 4C_b\omega_r mT_t sin(\omega_r(T_{sh} - T_t))$ $+ 4C_b V_0\omega_r^2 T_{sh}cos(\omega_r T_{sh}) - 4C_b V_0\omega_r^2 T_t cos(\omega_r T_{sh}) - I_0 T\omega_r^2 T_t cos(\omega_r t)$ $+ 2C_b\omega_r mT_t sin((\omega_r(2T_{sh} - T + 2T_t))/2) + C_b TV_0\omega_r^3 T_t sin(\omega_r t) + C_b T\omega_r^2 mT_t cos(\omega_r t)$ $- C_b T\omega_r^2 mT_t cos(\omega_r(t - T_t)))))/(N_{phase}T\omega_r^2 T_t^2)$	(A.44)
$T_{sh} \leq t < T_t + T_{sh}$	$(2VDCP(4I_0cos(\omega_r T_{sh}) - 4I_0 - 4C_b mcos(\omega_r T_{sh}) + 4C_b mcos(\omega_r(T_{sh} - T_t))$ $+ 4I_0\omega_r T_{sh}sin(\omega_r T_{sh}) - 4I_0\omega_r T_t sin(\omega_r T_{sh}) + 2C_b V_0\omega_r^2 T_t$ $- 2C_b\omega_r^2 mT_t^2 - 4C_b V_0\omega_r sin(\omega_r T_{sh}) + 2I_0\omega_r T_t sin((T\omega_r)/2)$ $- 2C_b\omega_r mT_t sin((T\omega_r)/2) - 4C_b\omega_r mT_{sh}sin(\omega_r T_{sh}) + 4C_b\omega_r mT_t sin(\omega_r T_{sh})$ $+ 2C_b\omega_r mT_t sin((\omega_r(T - 2T_{sh}))/2) + 2C_b\omega_r mT_t sin((\omega_r(T - 2T_t))/2) + C_b T\omega_r^2 mT_t$ $+ 2C_b V_0\omega_r^2 T_t cos((T\omega_r)/2) + 4C_b\omega_r mT_{sh}sin(\omega_r(T_{sh} - T_t)) - 4C_b\omega_r mT_t sin(\omega_r(T_{sh} - T_t))$ $+ 4C_b V_0\omega_r^2 T_{sh}cos(\omega_r T_{sh}) - 4C_b V_0\omega_r^2 T_t cos(\omega_r T_{sh}) - I_0 T\omega_r^2 T_t cos(\omega_r t)$ $+ 2C_b\omega_r mT_t sin((\omega_r(2T_{sh} - T + 2T_t))/2) + C_b TV_0\omega_r^3 T_t sin(\omega_r t)$ $+ C_b T\omega_r^2 mT_t cos(\omega_r t) - C_b T\omega_r^2 mT_t cos(\omega_r(t - T_{sh}))$ $- C_b T\omega_r^2 mT_t cos(\omega_r(t - T_t)))))/(N_{phase}T\omega_r^2 T_t)$	(A.45)
$T_t + T_{sh} \leq t < T/2$	$(2VDCP(4I_0cos(\omega_r T_{sh}) - 4I_0 - 4C_b mcos(\omega_r T_{sh}) + 4C_b mcos(\omega_r(T_{sh} - T_t))$ $+ 4I_0\omega_r T_{sh}sin(\omega_r T_{sh}) - 4I_0\omega_r T_t sin(\omega_r T_{sh}) + 2C_b V_0\omega_r^2 T_t - 2C_b\omega_r^2 mT_t^2$ $- 4C_b V_0\omega_r sin(\omega_r T_{sh}) + 2I_0\omega_r T_t sin((T\omega_r)/2) - 2C_b\omega_r mT_t sin((T\omega_r)/2)$ $- 4C_b\omega_r mT_{sh}sin(\omega_r T_{sh}) + 4C_b\omega_r mT_t sin(\omega_r T_{sh}) + 2C_b\omega_r mT_t sin((\omega_r(T - 2T_{sh}))/2)$ $+ 2C_b\omega_r mT_t sin((\omega_r(T - 2T_t))/2) + 2C_b V_0\omega_r^2 T_t cos((T\omega_r)/2) + 4C_b\omega_r mT_{sh}sin(\omega_r(T_{sh} - T_t))$ $- 4C_b\omega_r mT_t sin(\omega_r(T_{sh} - T_t)) + 4C_b V_0\omega_r^2 T_{sh}cos(\omega_r T_{sh}) - 4C_b V_0\omega_r^2 T_t cos(\omega_r T_{sh})$ $- I_0 T\omega_r^2 T_t cos(\omega_r t) + 2C_b\omega_r mT_t sin((\omega_r(2T_{sh} - T + 2T_t))/2) + C_b TV_0\omega_r^3 T_t sin(\omega_r t)$ $+ C_b T\omega_r^2 mT_t cos(\omega_r t) - C_b T\omega_r^2 mT_t cos(\omega_r(t - T_{sh})) - C_b T\omega_r^2 mT_t cos(\omega_r(t - T_t))$ $+ C_b T\omega_r^2 mT_t cos(\omega_r(T_{sh} - t + T_t)))))/(N_{phase}T\omega_r^2 T_t)$	(A.46)
$T/2 \leq t < T/2 + T_t$	$(VDCP(T - 2t + 2T_t)(4I_0cos(\omega_r T_{sh}) - 4I_0 - 4C_b mcos(\omega_r T_{sh}) + 4C_b mcos(\omega_r(T_{sh} - T_t))$ $+ 4I_0\omega_r T_{sh}sin(\omega_r T_{sh}) - 4I_0\omega_r T_t sin(\omega_r T_{sh}) + 2C_b V_0\omega_r^2 T_t - 2C_b\omega_r^2 mT_t^2$ $- 4C_b V_0\omega_r sin(\omega_r T_{sh}) + 2I_0\omega_r T_t sin((T\omega_r)/2) - 2C_b\omega_r mT_t sin((T\omega_r)/2)$ $- 4C_b\omega_r mT_{sh}sin(\omega_r T_{sh}) + 4C_b\omega_r mT_t sin(\omega_r T_{sh}) + 2C_b\omega_r mT_t sin((\omega_r(T - 2T_{sh}))/2)$ $+ 2C_b\omega_r mT_t sin((\omega_r(T - 2T_t))/2) + C_b T\omega_r^2 mT_t + 2C_b V_0\omega_r^2 T_t cos((T\omega_r)/2)$ $+ 4C_b\omega_r mT_{sh}sin(\omega_r(T_{sh} - T_t)) - 4C_b\omega_r mT_t sin(\omega_r(T_{sh} - T_t))$ $+ 4C_b V_0\omega_r^2 T_{sh}cos(\omega_r T_{sh}) - 4C_b V_0\omega_r^2 T_t cos(\omega_r T_{sh}) - I_0 T\omega_r^2 T_t cos(\omega_r t)$ $+ 2C_b\omega_r mT_t sin((\omega_r(2T_{sh} - T + 2T_t))/2) + C_b TV_0\omega_r^3 T_t sin(\omega_r t) + C_b T\omega_r^2 mT_t cos(\omega_r t)$ $- C_b T\omega_r^2 mT_t cos(\omega_r(t - T_{sh})) - C_b T\omega_r^2 mT_t cos(\omega_r(t - T_t)) - C_b T\omega_r^2 mT_t cos(\omega_r(T/2 - t))$ $+ C_b T\omega_r^2 mT_t cos(\omega_r(T_{sh} - t + T_t)))))/(N_{phase}T\omega_r^2 T_t^2)$	(A.47)
$T/2 + T_t \leq t < T/2 + sh$	$(VDCP(T - 2t + 2T_t)(4I_0cos(\omega_r T_{sh}) - 4I_0 - 4C_b mcos(\omega_r T_{sh}) + 4C_b mcos(\omega_r(T_{sh} - T_t))$ $+ 4I_0\omega_r T_{sh}sin(\omega_r T_{sh}) - 4I_0\omega_r T_t sin(\omega_r T_{sh}) + 2C_b V_0\omega_r^2 T_t - 2C_b\omega_r^2 mT_t^2$ $- 4C_b V_0\omega_r sin(\omega_r T_{sh}) + 2I_0\omega_r T_t sin((T\omega_r)/2) - 2C_b\omega_r mT_t sin((T\omega_r)/2)$ $- 4C_b\omega_r mT_{sh}sin(\omega_r T_{sh}) + 4C_b\omega_r mT_t sin(\omega_r T_{sh}) + 2C_b\omega_r mT_t sin((\omega_r(T - 2T_{sh}))/2)$ $+ 2C_b\omega_r mT_t sin((\omega_r(T - 2T_t))/2) + 2C_b V_0\omega_r^2 T_t cos((T\omega_r)/2) + 4C_b\omega_r mT_{sh}sin(\omega_r(T_{sh} - T_t))$ $- 4C_b\omega_r mT_t sin(\omega_r(T_{sh} - T_t)) + 4C_b V_0\omega_r^2 T_{sh}cos(\omega_r T_{sh}) - 4C_b V_0\omega_r^2 T_t cos(\omega_r T_{sh})$ $- I_0 T\omega_r^2 T_t cos(\omega_r t) + 2C_b\omega_r mT_t sin((\omega_r(2T_{sh} - T + 2T_t))/2) + C_b T\omega_r^2 mT_t cos(\omega_r(T/2 - t + T_t))$ $+ C_b TV_0\omega_r^3 T_t sin(\omega_r t) + C_b T\omega_r^2 mT_t cos(\omega_r t) - C_b T\omega_r^2 mT_t cos(\omega_r(t - T_{sh}))$ $- C_b T\omega_r^2 mT_t cos(\omega_r(t - T_t)) - C_b T\omega_r^2 mT_t cos(\omega_r(T/2 - t))$ $+ C_b T\omega_r^2 mT_t cos(\omega_r(T_{sh} - t + T_t)))))/(N_{phase}T\omega_r^2 T_t^2)$	(A.48)
$t \geq T/2 + T_{sh}$	0	(A.49)

Appendix B

Experimental Rig

B.1 Introduction

This chapter provides a brief description of the experimental configuration of the MTrMMC-DC-DC and TrSCC-DC-DC operational strategies. The hardware structures are described, including the design of the SMs, the selection of the AC link tank components and the design of the AC link medium frequency transformer. Finally, the control hardware and interface boards are presented.

B.2 Hardware Structure

B.2.1 Voltage sensing circuit of SM capacitor

The measurement of the SM voltages is required as an input to the SM capacitor balancing strategy and to control the stored energy/voltage of the SMs. The SM voltage sensing circuit shown in figure B.1 comprises a simple voltage divider and an isolation amplifier. The isolation amplifier, TI AMC1301, has an input range $\pm 250mV$ with a gain equal to 8.2 and a 7 kV reinforced isolation barrier between the input and output. The output of the isolation amplifier is connected to one of the ADC pins of the secondary MCU via the SM PCB connector. In addition, in order to provide "fast" over-voltage protection, the output of the isolation amplifier is compared with a threshold voltage to provide a trip signal to the local and central controllers in case an over-voltage event is detected.

B.2.2 SM MOSFET Gate drivers

Figure B.2 shows the Texas Instrument gate driver, UCC21520, that is used to control the MOSFETs. The UCC21520 is a dual-channel device with a 6 A peak output current and a reinforced isolation up to 5.7 kV. The input supply of the gate driver is 3.3 V and the outputs are connected to the isolated $\pm 15V$ DC-DC converters on the PCB. The two MOSFETs of the SM are controlled to operate in a complimentary manner. Therefore, one PWM signal is used for the upper device of the half-bridge and the lower device PWM signal is generated by inverting the upper PWM signal. Suitably designed RC filters are used for both PWM signals to reduce the ringing

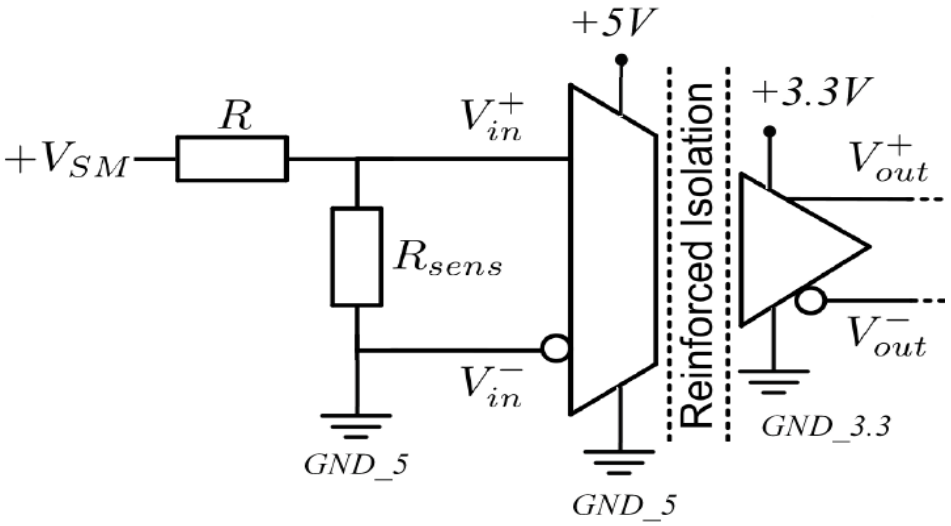


Figure B.1: *Voltage sensing circuit*

effects of the PCB layout before connecting them to the inputs of the gate driver.

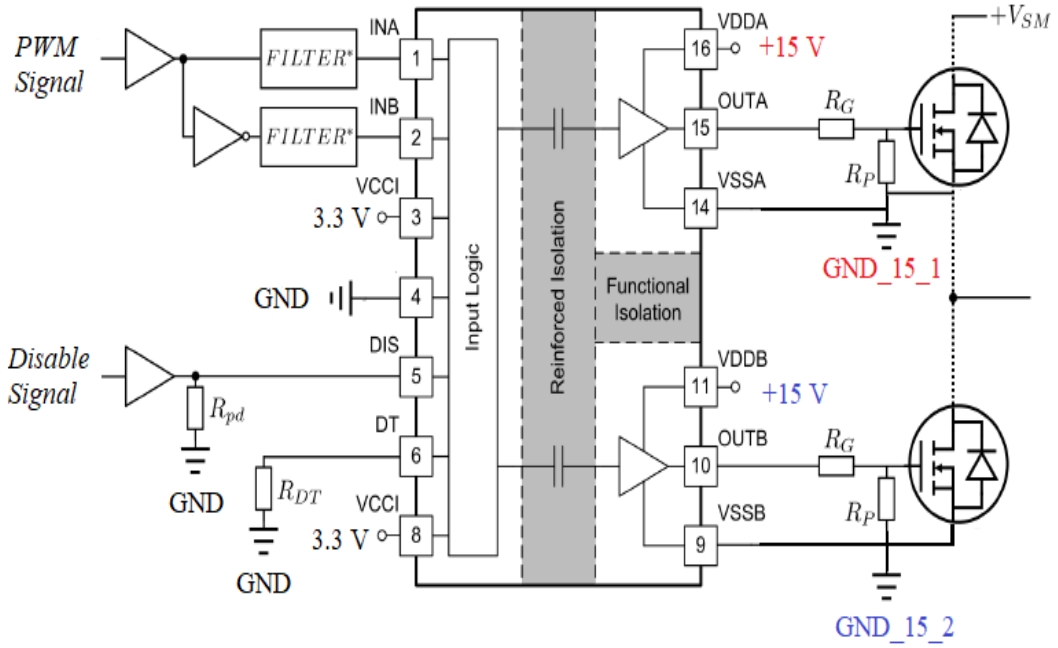


Figure B.2: *Gate driver*

The operation of the SM is enabled and disabled through a signal provided by the local controller and that signal is connected to the 'disable' pin of the gate driver through a buffer. Shoot-through must be avoided between the upper and lower MOSFET devices of the half-bridge SM and the choice of an appropriate dead-time, DT, prevents this. Equation B.1 shows the relationship between the dead time, DT, and R_{DT} where the units for the DT and R_{DT} are ns and kΩ, respectively. Considering the turn on/off delay of the MOSFET, 1 μs is chosen for the DT. The impact of the chosen dead-time on the chain-link voltage is negligible since the PWM duty cycle signal duration is much larger than that of the DT. A 20Ω gate resistor for

the MOSFET gate drive is selected, based on the recommended operation example given in the datasheet of the MOSFET. A resistor of 10kΩ is placed between the gate and the source of the MOSFET to prevent unwanted turn-on of the device in the absence of the gate signal.

$$DT = 10.R_{DT} \tag{B.1}$$

B.2.3 Pre-charge circuit of SM capacitors

It is essential to charge the SM capacitors to the desired voltage level in multilevel converters before enabling the control. This avoids significant and potentially damaging pulses of the current flowing when the fixed DC or AC power supplies are connected, caused by the presence of the anti-parallel diodes on the MOSFETs. As previously mentioned, the SMs were designed for the grid frequency AC-DC conversion and the pre-charge circuit was designed and implemented on the SM PCB to support the experimental tests. The pre-charge circuit shown in figure B.3 is based on a Cockcroft-Walton voltage multiplier generator (CWG) where the auxiliary supply is a $V_a = \pm 15$ square wave which drives the multiplier stages, resulting in a pre-charge voltage of $|V_{out}| = 60V$, on the SM capacitors. The diode, D_5 is placed to prevent power flow from SM's capacitor back to the CWG.

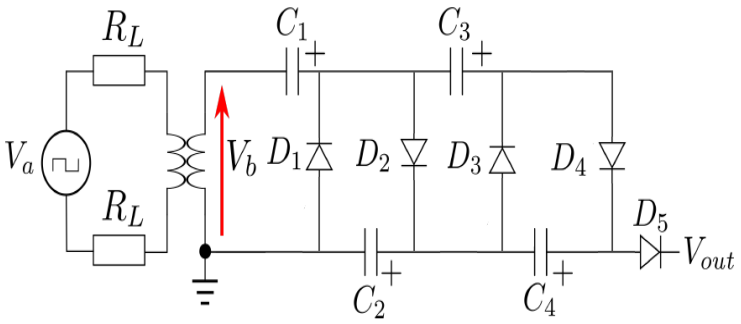


Figure B.3: *Pre-charge circuit*

However, in testing the MTrMMC and TrSCC-DC-DC prototype configuration shown previously in figures 8.2, 8.3 and 8.4, the pre-charge circuit is disabled since the conversion is DC-AC in both configurations. Instead, a variable DC power supply is used on the primary side of each setup. The SMs can be pre-charged by varying the DC voltage slowly from zero to desired voltage. Then, the power flow is imposed according to the experimental tests where in the MTrMMC prototype a three-phase load is used, and in the TrSCC-DC-DC setup, a phase shift is introduced between primary and secondary chain-link voltages.

B.2.4 TrSCC-DC-DC AC Link components

The AC link components of each phase of the TrSCC-DC-DC comprises the primary tank components (C_{bP} & L_{kP}), secondary tank components (C_{bS} & L_{kS}) and a single phase transformer. Figure B.4 shows the TrSCC-DC-DC AC link components. This section focuses on the single phase transformer design and the selection

of the tank components.

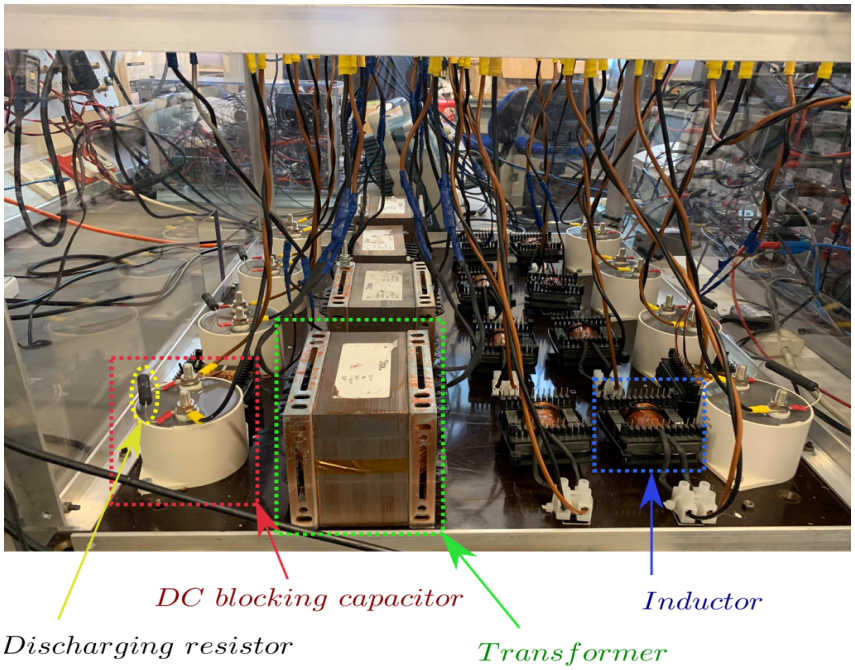


Figure B.4: *Four phases TrSCC-DC-DC AC link components*

B.2.4.1 Transformer design

The transformer for the TrSCC-DC-DC converter has not been optimally designed as a result of the need to use available cores from the lab. Four single phase transformers have been designed and built based on the available cores, $EI-175$, and bobbins. The main aim of the experimental tests was to validate the operational concept of the converter and hence the optimum design of the transformer was not crucial for the TrSCC-DC-DC concept validation.

Table B.1 shows EI-175 core parameters and table B.2 shows the design parameters and design assumptions. The operating frequency, output voltage and output power of the transformers were chosen so that they can be implemented in all topologies. However, during the experimental tests, the transformers were only used on the TrSCC-DC-DC topologies due to the limited number of the available SMs. The standard approach is used to design and construct the transformer as detailed in [101].

In order to determine if the available EI-175 core is suitable or not, the required core geometry constant, K_{gr}, to design a transformer with the parameters listed in table B.2 is calculated as shown in equation B.2 where P_t is the total power and K_e is the electrical conditions constant. The P_t and K_e components are calculated as shown in expressions B.3 and B.4, respectively. Since the EI-175 core geometry, K_g, is bigger than required core geometry, K_{gr}, the EI-175 is suitable for the transformer design.

Table B.1: EI-175 core parameters

Parameters	Symbol	Value
core geometry coefficient	K_g	81.656 cm^5
Area product	A_p	278.145 cm^4
Window area	W_a	14.818 cm^2
Effective cross section	A_c	18.77 cm^2
surface area	A_t	652 cm^2
Magnetic path length	MPL	26.7 cm
Mean length turn	MLT	25.6 cm
Iron weight	W_{tfe}	3711 g
Copper weight	W_{tcu}	1348 g

Table B.2: Transformer design parameters

Parameters	Symbol	Value
Input voltage	V_{in}	240 V
Output voltage	V_{out}	240 V
Output current	I_{out}	15 A
Output power	P_o	3.6 kW
Operating frequency	f_o	250 Hz
Form factor	K_{fo}	≈ 4
Regulation	Reg	5%
Efficiency	η_{trn}	95%
Window utilization factor	K_u	0.4
Alternating current flux density	B_{ac}	1.6 T

$$K_{gr} = \frac{P_t}{2.K_e.Reg.100}\ [cm^5] \qquad K_{gr} = 19.907[cm^5] \tag{B.2}$$

$$P_t = P_o.(\frac{1}{\eta_{trn}} + 1) \qquad P_t \approx 7.39\ [kW] \tag{B.3}$$

$$K_e = 0.145.K_{fo}^2.f_o^2.B_{ac}^2.10^{-4} \qquad K_e = 37.12 \tag{B.4}$$

The expressions B.5 and B.6 shows the primary number of turns, N_{tp}, and the secondary number of turns, N_{ts}, respectively.

$$N_{tp} = \frac{V_{in}.10^4}{K_{fo}.B_{ac}.f_o.A_c} \qquad N_{tp} = 80 \tag{B.5}$$

$$N_{ts} = \frac{N_{tp}.V_{out}}{V_{in}}.(1+Reg) \qquad N_{ts} = 84 \tag{B.6}$$

Equations B.7 and B.8 show the calculation of the required primary winding wire area , $A_{wp(B)}$, and secondary winding wire area, $A_{ws(B)}$, for both the primary winding and secondary winding, respectively, where J is the current density and I_{in} is the input current. The equations B.9 and B.10 present the J and I_{in} calculations respectively.

$$A_{wp(B)} = \frac{I_{in}}{J} \qquad A_{wp(B)} = 38e-3\ [cm^2] \tag{B.7}$$

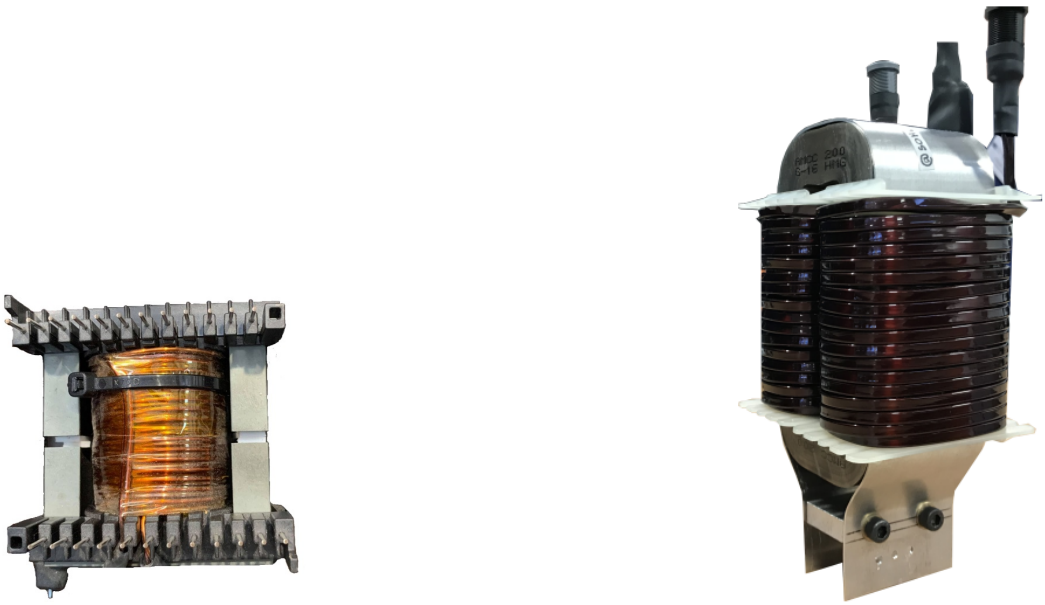
$$A_{ws(B)} = \frac{I_{out}}{J} \qquad A_{ws(B)} = 36.1e-3\ [cm^2] \tag{B.8}$$

$$J = \frac{P_t}{K_{fo}.K_u.B_{ac}.f_o.A_p} \qquad J = 415.11\ [A/cm^2] \tag{B.9}$$

$$I_{in} = \frac{P_o}{V_{in}.\eta_{trn}} \qquad I_{in} = 15.78\ [A] \tag{B.10}$$

Considering the available wire in the laboratories, 3 strands of a wire with a diameter of $D_w = 0.132\ cm$ have been used where the area of the selected wire is $A_w = (\frac{D_w}{2})^2.\pi\ cm^2 = 0.01368cm^2$ and the 3 strands area is $3*0.0136841cm^2$ which is bigger than $A_{wp(B)}$ and $A_{ws(B)}$.

Although, the converters are operated at medium frequency, it is worth considering the largest bare wire area that can be operated at medium frequencies, $f_o = 250\ Hz$ & $f_o = 500$. Based on equations B.11 and B.12 the largest bare wire area, $A_{wL(B)}$, is calculated where ε is the skin depth which is equal to the radius of the largest bare wire area and K is the material factor which is $K = 1$ for copper. The largest wire area, $A_{wL(B)}$, is $0.55\ cm^2$ at $f_o = 250\ Hz$ and it is $0.275\ cm^2$ at $f_o = 500$. The selected wire area for the converter is much smaller than the largest wire diameter, hence, there is no concern about the skin effect with the selected wire if the transformer is operated at those frequencies for power flow below or equal to the rated power of $3.6\ kW$.



(a) *AC inductor* **(b)** *DC inductor*

Figure B.5: *Rig inductors*

$$\varepsilon = \frac{6.62}{\sqrt{f_o}}.K\ [cm] \tag{B.11}$$

$$A_{wL(B)} = \varepsilon^2.\pi\ [cm] \tag{B.12}$$

B.2.4.2 Resonant tank components and DC inductor selection

The resonant tank inductor shown in figure B.5a is chosen based on the design of the tank to operate at the optimum region (discussed in section 6.4) for the TrSCC-DC-DC. Two inductors have been used for each phase, one on the primary and the other on the secondary side. The calculated inductance value is 0.95 mH and the inductance of the constructed inductors is between 0.92 mH to 0.99 mH when measured with an LCR meter. A further six of the TrSCC-DC-DC tank inductors are used in the MTrMMC arms.

The inductor shown in figure B.5b is chosen to connect the TrSCC-DC-DC converter to a unidirectional DC power supply. The DC inductor is chosen to limit di/dt and it has the inductance of 1.7 mH which is chosen based on availability of the inductors in the laboratory. The current rating at the operating frequency for both tank inductor and DC inductor is higher than the current for the operating conditions of the tests .

The DC blocking capacitor shown in figure B.6 is chosen to be 220 μF which makes the resonant frequency of the equivalent phase tank less than the operating frequency, $k_f = \frac{f_o}{f_r} = 1.44$. As discussed in section 6.4, $k_f = 1.44$ is included in the optimum design region of the tank. Based on the commercially available capacitors

a 220 μF Polypropylene capacitor manufactured by Kemet, C4DEHPQ6220A8TK, is selected. This can operate up to 600 VDC and its rated RMS current is 65 A at 65^o C. The ESR of the selected capacitor is 1 mΩ and the screw terminals of the blocking capacitor is connected to a 100 kΩ discharging resistor, for safety, which results in a time constant of 22 s.

Figure B.6: *DC blocking capacitor*

B.3 Control system design

B.3.1 Primary PCB

Figure B.7 shows the primary control board which comprises a F28379D controlCARD and expansion boards which are connected through 180-pin edge connectors. The primary controller can provide the following features:

- 25 AVAGO AFBR-1624 optic transmitters. 15 of the optic transmitters utilised where 12 of the optic transmitters are used for the SPI communication channels (3 SPI transmitters to each secondary controller), 3 of the optic transmitters are used for the interrupt time (1 transmitter for each secondary controller) and 3 of the optic transmitters are used for the trip channels (1 transmitter for each secondary controller)

- 6 AFBR-2624 optic receivers where three of the optic receivers are used for SPI communication channels (1 receiver for each secondary controller) and three of the optic receivers are used for trip channels (1 receiver for each secondary controller)

- 20 ADC channels are available. A maximum of 15 ADC channels are used in the TrSCC-DC-DC converter with $\rho_g = 2$, 8 ADCs are used for monitoring the DC blocking capacitor voltages, 4 ADCs are used for monitoring the AC link tank currents, 1 ADC is used for monitoring the primary converter DC current and 2 ADCs are used for monitoring the secondary converter phase current

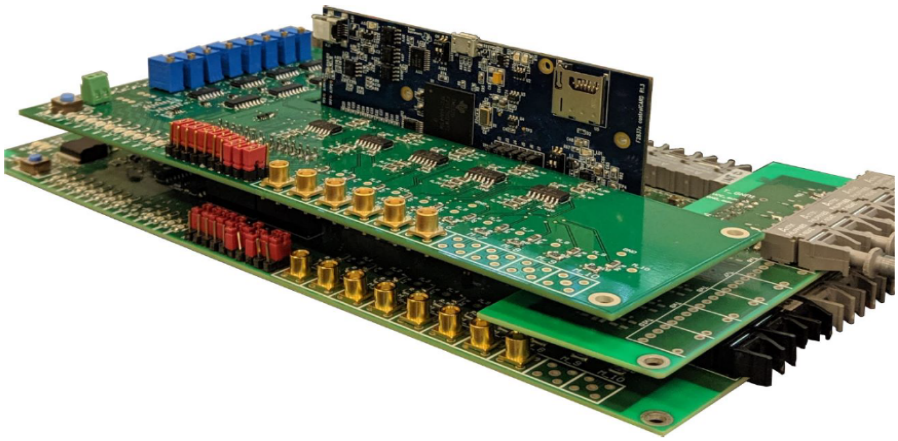


Figure B.7: *Master PCB*

B.3.2 Back-plane PCB

Figure B.8 depicts the back-plane PCB which has three main functions. Firstly, there are 8 female connectors, a SM connector area, that provides the connection between 8 SMs and the back-plane PCB forming a SM phase stack. Secondly, the back-plane PCB hosts the local micro controller F28377S launchpad, secondary MCU. Thirdly, there are a number of communication channels between local MCU (secondary) and central MCU (primary) implemented via optical fibers. These channels are necessary to achieve protection through trip lines, synchronous operation via the same interrupt signal provided by the primary MCU and the control system implementation where information is communicated between the local MCUs and central MCU (such as SM capacitor voltages, modulation signals, etc.).

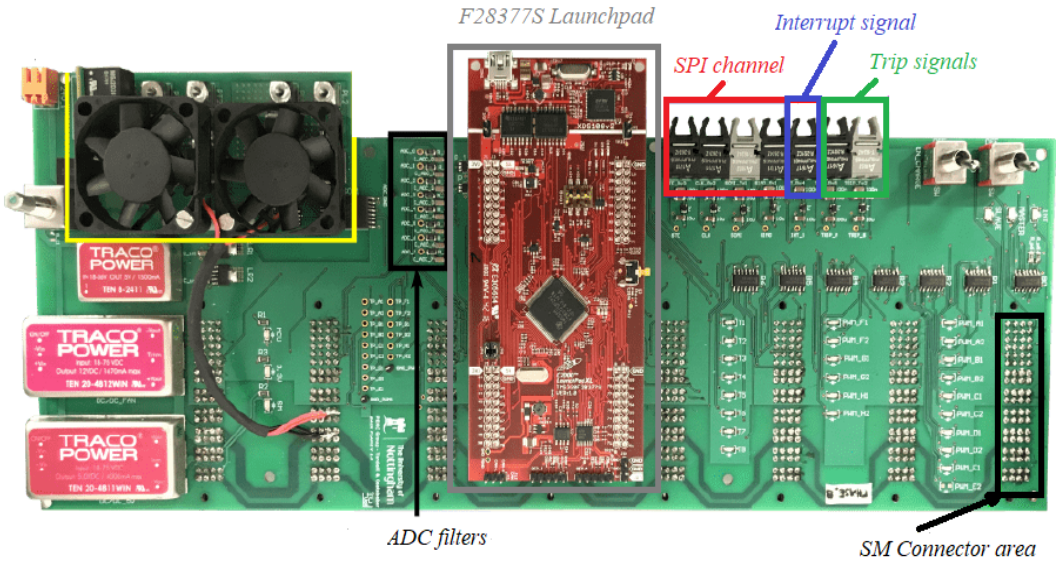


Figure B.8: *Back-plane PCB*

In order to provide fast protection for the converter devices and components, the converter is shut-down in case of having an active over-voltage trip signal from any SM. The back-plane collects the over-voltage signals and feeds them into a

multiple input AND gate. The output of the AND gate is connected to the 'reset' of the F28377S launchpad, and accordingly, the MCU resets if an over-voltage occurs on any of the SM capacitors. The central MCU is informed about the status of the secondary MCUs via an optical fiber and acts accordingly to reset all the MCUs.

B.3.3 Measurement boards

In the MTrMMC prototype setup, 7 external current sensors are required to monitor the 3 output AC currents, 3 upper currents and the input DC current. The current sensor data is used to provide a digital protection to the hardware devices, where in case of any failure that makes the current reach a predefined threshold value, the MCUs reset the PWM signals and switch the SMs into a safe neutral state. However, only the three phase AC currents and DC side currents are required for the balancing of the SM capacitor voltages and the DC/AC power flow control. LEM LA 55-P current transducers, such as the one shown in figure B.9 are used to measure the currents. These are rated at 50 A nominal current and provide a range of $\pm 25mA$ at the output.

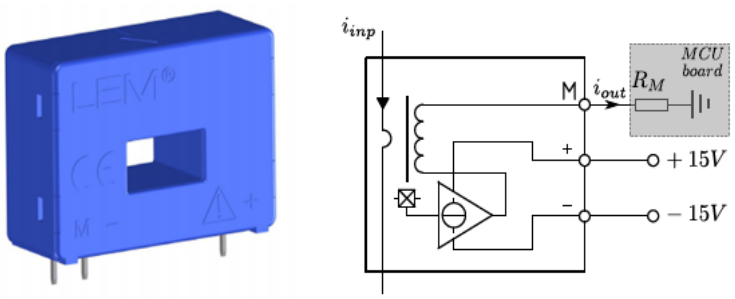


Figure B.9: *Current transducer*

In the TrSCC-DC-DC prototype setup 8 external voltage sensors, 6 external current sensors when $\rho_g = 1$ (2 for DC currents and 4 for AC currents) and 7 external current sensors when $\rho_g = 2$ (1 for primary DC current, 2 for secondary phase currents and 4 for AC currents) are required to monitor 8 DC blocking capacitor voltages, 4 AC currents, 2 DC side currents when $\rho_g = 1$ and the primary DC current with 2 secondary phase current if $\rho_g = 2$. The current and voltage sensors are use to provide digital protection to the hardware devices. However, the measurement of the DC currents are required to also provide overall power flow control and if per-phase power flow control is required, AC current measurements are also required. Similar to the MTrMMC setup, LEM LA 55-P current transducers are used in the TrSCC-DC-DC converter. Figure B.10 shows an LV 25-P voltage transducer that is used for measuring the DC blocking capacitor voltages. The LV 25-P voltage transducer converts the measured voltage to the range of $\pm 14mA$ through a primary internal resistor, R_{inp}, and provides an output current with a conversion gain of 2.5. The burden resistor, R_M, converts the output current into a voltage which is adjusted and routed to the ADCs of the primary MCU through conditioning circuits placed on the master interface board.

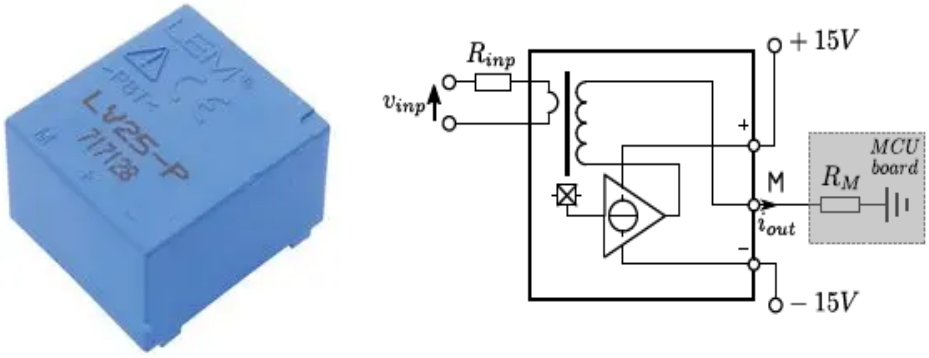


Figure B.10: *Voltage transducer*