THE UNIVERSITY OF NOTTINGHAM

DEPARTMENT OF ELECTRICAL AND ELECTRONIC ENGINEERING



MULTIDOMAIN MODELLING OF MULTICHIP SiC POWER MODULES

Mr Olufisayo Abimbola Olanrewaju

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То

The Almighty God,

ABSTRACT

Increasing energy demands in different application fields of power electronics (e.g. Photovoltaics, Traction, Aerospace) have led to increased demand for power electronic systems with higher conversion efficiency, higher power density, reliability and higher operating temperatures among other needs. Given that power devices are an essential component of power electronic systems and their operation cuts across multiple energy domains (e.g. electrical, thermal, mechanical), efficient multidomain design of power electronic devices is crucial to meeting the increased energy demands. Simulation is a key tool for the development of novel technology and for preliminary assessment of its performance in power electronic applications. However, for simulation to be an effective tool, compromise between accuracy and computational efficiency is required.

This thesis presents an overall modelling methodology for the use of simulation in virtual prototyping of multichip power modules with an optimum compromise between accuracy and computational efficiency. Semiconductor models for the electrical domain, discretised structural models for the thermal domain and analytical models for the mechanical domain are created based on the overall modelling methodology and validated. The models created for the electrical, thermal and thermomechanical domains were coupled in realistic power electronic simulation scenarios. Parametric studies were also conducted on the combined electro-thermomechanical model by varying electrical, thermal, geometry, material properties and observing their multidomain effects in circuit level simulation. The results show that the proposed methodology is a time and cost-saving tool to be incorporated in the design of power modules before physical prototyping of the design is conducted.

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Publications

The work presented in this thesis has resulted in the following publications

Conference Papers

First Author

- 1. **O. Olanrewaju**, B. Mouawad, A. Castellazzi, and R. Kraus, "VHDL-AMS modelling of multi-chip SiC power modules," in *2016 IEEE 4th Workshop on Wide Bandgap Power Devices and Applications (WiPDA)*, 2016, pp. 347-352.
- O. Olanrewaju and A. Castellazzi, "VHDL-AMS Thermo-Mechanical Model for Coupled Analysis of Power Module Degradation in Circuit Simulation Environments," in 2018 International Conference on Simulation of Semiconductor Processes and Devices (SISPAD), 2018, pp. 309-313.
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Co-Author

- F. Stella, O. Olanrewaju, Z. Yang, A. Castellazzi, and G. Pellegrino, "Experimentally validated methodology for real-time temperature cycle tracking in SiC power modules," *Microelectronics Reliability*, vol. 88-90, pp. 615-619, 2018.
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List of Terms

- 1D 1 Dimensional
- 2D 2 Dimensional
- 3D 3 Dimensional
- A Area [m²]
- BJT Bipolar Junction Transistor
- C Elasticity tensor
- C_{ds} drain source capacitance [F]
- C_{gd} gate drain capacitance [F]
- C_{gs} gate source capacitance [F]
- C_{OX} Oxide capacitance [F]
- Cth Thermal capacitance [J/K]
- Cs Specific heat capacity [J/(Kg K)]
- CTE Coefficient of Thermal Expansion [K⁻¹]
- CTN Compact Thermal Network
- D Depth [m]
- DAE Differential and Algebraic Equation
- D.U.T Device Under Test
- E Electric Field [V/m]
- E_C –Critical electric field [V/m]
- ε Strain
- F-Force [N]
- FDM Finite Difference Method
- FEA Finite Element Analysis
- FEM Finite Element Method
- FVM Finite Volume Method
- GaN- Gallium Nitiride
- GUI Graphic User Interface
- H Height
- HDL Hardware Description Language

H i, j, k – Heat (power loss) $[W/m^2]$

 I_{ds} – Drain- Source current [A]

IGBT – Insulated-Gate Bipolar Transistor

K – Thermal conductivity [W/ (mK)]

Ke – Stiffness [N/m]

 σ – Stress [N/m²]

L – Length [m]

MAST – MAST Hardware Description language

MOSFET – Metal-Oxide-Semiconductor Field-Effect Transistor

MOR – Model Order Reduction

N - Carrier concentration [m⁻³]

 N_d – Intrinsic Carrier concentration [m⁻³]

 N_i – Dopant concentration [m⁻³]

NR – Newton Raphson method

 θ – Change in temperature [K]

ODE – Ordinary Differential Equation

P – Density [Kg/m³]

PEMC- Power Electronics, machines and Control Research group, University of Nottingham

PDE – Partial Differential Equation

q – Charge [C]

R - Resistance [Ohms]

REPI- Power MOSFET Epilayer resistance

RAJ- Power MOSFET voltage dependent resistance in JFET and accumulation regions

Rth – Thermal resistance [K/W]

Si – Silicon

SiC – Silicon Carbide

SPICE – Simulation Program with Integrated Circuit Emphasis

T-Temperature [K]

Ta – Ambient temperature [K]

Tnom – Nominal temperature [K]

Tref – Reference temperature [K]

U – Deformation [m]

 μ – Mobility [m²/(V s)]

 μ_n – Mobility (electron mobility) [m²/(V s)]

v – Poison's ratio

V – Electrostatic potential [V]

 V_{bd} – Breakdown voltage [V]

 V_{ds} – Drain source voltage [V]

VDMOS – Vertical Double- diffused MOSFET

 V_{qs} – Gate source voltage [V]

Vto – Threshold voltage (at room temperature) [V]

Vth – Temperature dependent threshold voltage [V]

Verilog- AMS – VERILOG Hardware Description Language- Analogue Mixed Signals

VHDL-AMS – Very high speed integrated circuit Hardware Description Language-Analogue Mixed Signals

W – Width [m]

WBG – Wide Band Gap

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CHAPTER 1: INTRODUCTION

Power electronics is an enabling technology that uses the switching of semiconductor devices to efficiently process and control the flow of electrical energy from one form to another to meet the needs of a specific application. The block diagram of a power electronics system is shown in Fig.1. 1a. The power processor unit (power converter) comprises of semiconductor switches, inductors, transformers and capacitors which convert electrical energy from one form to another (e.g. ac to dc) or one magnitude to another (e.g. higher voltage to low voltage). The controller unit of the power electronic system is used to monitor the conversion process and send signals to control the semiconductor switches. An example of a power electronic system is shown in Fig.1. 1b. The converter in this case, efficiently converts DC input voltage into AC voltage output through the switching of the semiconductor devices which can then be used by AC loads such as grids, ship micro grids and railway traction systems.

Given that power electronics is currently the major enabling technology for efficient processing and control of electrical power, increasing power demands have resulted in increased demands for power electronic systems. It is estimated that in the year 2030, as much as 80% of all electric power will have power electronics technology between generation and consumption[1]. The increased demand for power electronic systems also results in increased demand for power electronic systems with higher conversion efficiency, high operating temperature and higher power density systems [2].





Fig.1. 1: (a)Block diagram of a power electronic system ; (b) Example of a power electronic system which includes a multichip power module

Semiconductor power devices (switches) are an essential component of power electronic systems and the main contributor of power losses thus, the design of semiconductor devices is critical to meeting increased energy demands. Semiconductor switches with lower conduction and switching losses result in higher power conversion efficiency. Semiconductor devices manufactured using materials with lower intrinsic carrier concentration (see chapter 3) at room temperature will result in semiconductor devices with the capability to operate with higher operating temperatures. With higher power conversion efficiency and higher operation temperature capability partly derived from recently developed semiconductor devices, cooling and passive requirements are reduced resulting in higher power density power electronic systems. Conventional semiconductor devices manufactured using Silicon (Si) are capable of being used in a wide range of applications. Fig.1. 2 [1] shows the application range for power semiconductor devices are capable of handling the voltage and current required. However, in many traction and utility applications, single chip devices cannot meet the voltage and current handing requirements.



Fig.1. 2: Voltage and current ratings for power electronic applications

Hence multiple chips (i.e. multiple power semiconductors) need to be combined to achieve the required voltage and current handling requirements. The multiple chip

assembly consisting of more than one chip interconnected with other layers (usually performing electrical, thermal or mechanical functions) used to achieve this purpose for use in a power converter is referred to as a multichip power module.

A multichip power module package is shown in Fig.1. 1b in which the four power semiconductors- 2 MOSFETs and 2 diodes (highlighted in the grey area) can be found. A multichip power module contains more than one chip in a package. The chips are usually connected in a way that results in the possibility of either higher current conduction when the device is turned ON or higher voltage blocking when the device is turned OFF in comparison to a single chip package. It is easy to infer that the operation of the power module is purely electrical; in reality however, the operation of the power module involves different multi-domain effects which interact with each other during the operation of the power module and the magnitude of the interaction is significantly determined by design parameters used in the design of the power module. An example of a multidomain effect is the temperature (thermal domain). When the device is turned ON, the power loss from the chip region increases the operating temperature of the device. This results in an increase in the value of onstate resistance (and onstate voltage) modifying the electrical current value (electrical domain) and resulting in higher value of power loss- a vicious cycle which further increases the temperature of the device. Thus, the thermal domain has to be considered in the design of the power module in order to ensure that the device temperature rise is within acceptable limits. As the temperature of the device changes, the strain and stress (mechanical domain) values at different regions in the multichip module package change. If certain thresholds (for example maximum Yield

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stress) for the materials used in the components in the power module are exceeded, the components may fail or begin to exhibit different mechanical characteristics from what the power module requires, leading to the failure of the power module. Thus, the design of the power module would also require the mechanical domain to be considered.

Despite the established use of Si chips in power modules, limitations arising from its material properties have resulted in constraints in important properties such as thermal conductivity, operating temperature and voltage blocking capability thus limiting the magnitude of the power density that is achievable in Si power modules. Large amount of research has been undertaken in the use of alternative materials in the manufacture of the chips in power modules [3]. Research was conducted on new materials with wide band gap (WBG) such as Silicon Carbide (SiC) with a view to replacing Si in the manufacture of chips in power devices from which it has been shown that SiC Power devices can be physically smaller than their Silicon (Si) counterparts for the same power ratings due to their material properties[4]. The application power and switching frequency range for Si, and WBG devices such as (SiC and Gallium Nitride GaN) is shown in Fig. 1.3. It shows that alternative materials such as SiC and GaN provide competition to Si in the 1kW- 10kW power and 10kHz-100kHz switching frequency range.

An example of a relatively new SiC multichip power module is shown in Fig.1. 4. It is a SiC half-bridge prototype capable of blocking up to 2.5kV[4]. However, these (smaller physical size and higher switching frequency) benefits in multichip modules [4] lead to highly localized heat generation rates and accounting for the resulting effect on thermomechanical stress becomes very important. The understanding of these

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effects is very critical in the design of power electronic systems that make use of multichip SiC power modules.



Fig.1. 3: Application power and switching frequency range of power semiconductors [5, 6]

From the explanation above, one can observe how two factors- temperature change and physical size (geometry) determine the operation of the power module. There are other factors ranging from electrical, thermal, mechanical, material and geometrical which also determine the operation of the power module. To observe and understand the effect of these factors in the design stage before vast amount of resources are committed to experimental testing, the availability of an analysis/ synthesis simulation tool to implement coupled analysis of multi-domain relationships (electrical, thermal and mechanical points of view) is needed.



Fig.1. 4: High Frequency SiC Half bridge module reprinted from [4]

1.1 RESEARCH MOTIVATION, METHODOLOGY, AIMS AND OBJECTIVES

Synthesis/ analysis simulation tools for multi-domain analysis of power modules need to meet two main usability criteria. First, a synthesis/ analysis simulation tools must possess the ability to produce accurate result. In the design stage of power modules (the application target for this work), results which are qualitatively accurate across the power module but not accurate quantitatively are still acceptable. Secondly, the computational cost (i.e. simulation time) of using the tool should be acceptable to the design engineer based on the intended application. Due to the large number of parameter iterations involved during the design stage, it is important that the analysis tool is solvable in times acceptable to the design engineer [7, 8].

Currently available commercial software tools used for design and analysis of power module are capable of showing results in electrical, thermal and mechanical domains but there is currently no commercially available software package with fully coupled electro-thermo-mechanical simulation capability during the simulation [9]. These simulation tools also tend to prioritize one of the two usability criteria at the expense of the other. For instance, tools which use Finite Element Analysis (FEA) are known to generate highly accurate result when compared to experimental result of the same simulated tests but the computational cost is usually very high [9, 10]. On the other hand, tools which generate easily solvable models do so at the expense of the accuracy of the results (the term "accuracy" here implies the detail of the results; for instance a simple RC thermal network solves more quickly than a detailed FEA thermal model for the same semiconductor device package structure but does not give detailed information about the temperature in different layers in a power semiconductor package). In this project, a more reasonable balance was generated between the need for accuracy and reduction in computational cost. This balance is the project methodology (referred to as overall modelling methodology in this project/thesis) as shown in Fig.1. 5. Fig.1. 5 highlights the interaction between the electrical, thermal and mechanical domains in the operation of a power module. The logic and drive control signals control the switching of the power device based on inputted design parameters and feedback from the electrical, thermal and mechanical domains designated to ensure the safe operation of the device. In the electrical domain, the equations in the compact model determine the power loss which is input to the thermal model and leads to a rise in temperature in the device which is feedback into the electrical model equations to modify the temperature dependent parameters in the electrical model (such as onstate resistance). The thermal model also influences the temperature differential in the mechanical domain through which the displacement across the constituent layers in the power module changes. This is also feedback into the thermal model modifying the geometry of the power module in calculating the temperature values for different regions in the power module.

Each domain (aspect) has a set of fundamental equations governing their operation. In the electrical domain, the fundamental equations are the Poison's and carrier equations, for the thermal domain, the fundamental equation is the heat equation and for the mechanical domain, the fundamental equation is Hooke's law. In this project, these complex fundamental equations are approximated into a set of equations that can be solved with minimal computational effort in any standard circuit simulator. Once all the equations are written, they are then compiled and validated using steady state and transient simulations which are solved using a simulator software capable of solving non-linear ordinary differential equations (ODEs). Unlike software tools that involve the use of FEA, in the proposed modelling methodology (see Fig.1. **5**), the use of Computer Aided Design (CAD) is eliminated and replaced with the use of equations and parameters on which parametric analysis can be easily conducted.

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Fig.1. 5: Overall modelling methodology approach used in this work

1.2 POWER ASSEMBLY

In this thesis, the term "power assembly" is frequently referred to. A power assembly can be described as the fundamental building block of the power module[11]. It is used in this project to simplify the analysis of power module structures. The fully packaged power module comprises one or more power assemblies and other components such as interconnects, bond wires and casing. In this project, interconnects, bond wires and casing are not considered as the focus of this work is proposing a tool which is useful to the design and analysis of power module design with respect to the physical layout, electrical, thermal and mechanical parameters of the layers in a power assembly structure such as shown in in Fig.1. 6. The top and side



Fig.1. 6: Structure of the power assembly - (a) Top view and (b) side view

view of a power assembly with two chips is shown in Fig.1. 6. It shows the chip (the active part of the power assembly) layer and other layers in the power assembly. Apart from the chip layer, the other layers are also critical to the operation of the power module.

1.3 Aim and Objectives of this Project

The aim of this PhD project is to introduce improvements in the field of Virtual Prototyping for Power electronics by presenting a methodology through which complex multichip power module structures consisting of multiple chips can be analyzed and designed with multidomain effects observed simultaneously with their electrical characteristics.

The objectives of this project are as follows:

- (1) Review existing modelling methodologies and derive an overall modelling methodology for multidomain simulation of multichip power modules
- (2) Review modelling language and platforms and select a modelling language and platform to use in implementing the overall modelling methodology
- (3) Review numerical solution methods to understand numerical solution methods for the models developed based on the overall modelling methodology
- (4) Develop and validate a Physics based electrical model for the SiC Power MOSFET in line with the overall modelling methodology.
- (5) Develop and validate a thermal model in line with the overall modelling methodology.
- (6) Develop and validate a thermo-mechanical model in line with the overall modelling methodology.
- (7) Conduct parametric studies with the electrical, thermal and mechanical models using realistic design scenarios to showcase the usability of the overall modelling approach in the design and analysis of multichip power modules.

1.4 Thesis outline

The thesis comprises of seven chapters. A brief overview of the chapters (excluding chapter 1) is given in this section.

1.4.1 Overview of chapter 2

In this Chapter, an explanation of ordinary differential equations and their solution methods is given. The modelling language used in this project (VHDL-AMS) is discussed in detail. Simulation terms such as stability, convergence which can determine the accuracy and computational cost of a simulation are also discussed.

1.4.2 Overview of chapter 3

The electrical model developed in this project is discussed in chapter 3. A review of exiting models is given and the justification for the modelling method used is given. The model is validated in steady state simulations and its capability for use in transient simulation is shown.

1.4.3 Overview of chapter 4

The thermal model developed in this project is discussed in chapter 4. A review of exiting models is given and the justification for the modelling method used is given. The model is validated using experiment and FEA analysis in three examples- a chip level (one layer structure) coupled simulation, a multilayer (power assembly) uncoupled simulation and a full power module package coupled simulation.

1.4.4 Overview of chapter 5

The thermo-mechanical models developed in this project are discussed in this chapter. A review of approaches to modelling mechanical effects is given. The 1D and 3D versions of the model are discussed and their validation with FEA is shown.

1.4.5 Overview of chapter 6

In this chapter, parametric studies are conducted with the electrical, thermal and mechanical models coupled and used in power electronic simulations. Various electrical, thermal, material and geometrical properties are varied and their effects across different domains are observed and explained.

1.4.6 Overview of chapter 7

In this chapter conclusions drawn from the work done and results obtained in this project are explained. Possible future work are also outlined.

CHAPTER 2- MODELLING LANGUAGE AND REVIEW OF SIMULATOR SOLUTION PROCESS

2.1 Modelling language

In circuit simulation, once the constituent equations for the models have been derived, the equations need to be coded in a computer language and implemented in a circuit simulator. For instance, to use the popular SPICE program in simulating a custom MOSFET model (i.e. a model not in the internal component library of the SPICE platform used for simulation), model equations are written in SPICE modelling language which are then solved using the SPICE simulator program. Apart from SPICE, there are other modelling languages available for description of compact models such as C/C++, FORTRAN, MATLAB and hardware description languages (HDLs) such as MAST, Verilog AMS and VHDL-AMS. Thus, a choice had to be made on the modelling language to be used for this project. From, the overall modelling methodology of this project (discussed in Chapter 1), it is important that the language with which the equations of models would be written meet certain requirements. The requirements are discussed in the next subsection.

2.1.1 Requirements for modelling language

(1) Multi-domain capability: The language must be able to describe electrical, mechanical, thermal domain equations to be used in multidomain simulation without having to convert equations in one domain to equivalents in another domain (for example, the language should have the ability to interpret and solve thermal equations without the need to convert the thermal equations to electrical equivalents).

(2) Multi-level abstraction: An advanced power device model as presented in this project can be connected to the most basic voltage/power source to run simulations over different timescales (ms to s).

(3) Portability Models created in the modelling language should be useable in a wide range of simulators with minimal or no compatibility issues.

2.1.2. VHDL-AMS

Consider a power electronic system such as an Inverter as shown in Fig.2. 1. The 3 phase inverter contains 3 legs of switching power devices and each leg of devices is packaged in a power module. The power module assembly structure of one of the legs is shown with the blue arrow in Fig.2. 1. All other legs have a similar power module assembly.

Using the methodology proposed in this work, a set of electrical domain equations will be written for the switching devices in Fig.2. 1. The capacitor in the inverter is also an electrical device and will need a model comprising of electrical equations (electrical model). The voltage source input is also an electrical device, and would require a model with electrical equations although with relatively low level of abstraction compared to that of the power devices. To simulate the thermal effects, a structural model based on discretized partial differential equations (PDE) is used. To simulate thermomechanical effects, an analytical model which takes the temperature at each node from the discretized thermal model as input and then derives stress and strain values. Finally, the inverter requires control signals to turn ON and OFF the power devices. Control of power devices usually require digital

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Fig.2. 1: System level simulation of an inverter with models of different level of abstraction

functions (such as Boolean expression, logic gates) and thus a model comprising digital functions and expressions is required. To simulate a system level circuit as shown in Fig.2. 1 to capture the multidomain effects explained above, a language is required which could handle mixed signal (digital and analogue), multi-abstract (complex thermal and electrical models in the same circuit with simple models such as voltage source) and multidomain (electrical equations in the same circuit with thermal equations and mechanical equations) equations without additional complexity which would hamper the solvability of the circuit. SPICE was originally designed to handle microelectronic integrated circuits [12, 13] and is a very good modelling language to use in the electrical domain. However, for multidomain simulation, relationships in other domains will have to be converted to electrical domain equivalents which may not be trivial to perform. The SPICE languages is tightly

knitted with the SPICE simulation solver- this limits the ability of models developed in SPICE to be used in non-SPICE solver environments with little adjustments needed. The possibility of using popular coding languages such as C/C++, FORTRAN was also investigated. However, using this languages would require that the numerical algorithms for solving the model equations would also have to be written which is an error prone and intensive task on its own[14]. The next option was to investigate the use of hardware description languages (i.e. HDLs such as MAST, Verilog AMS and VHDL-AMS). These languages have multi-domain capability [15] and are capable of simulating circuits consisting of models with different levels of abstraction[14, 16]. VHDL-AMS AND Verilog-AMS have been standardized by the Institute of Electrical and Electronic Engineers [14, 15]. Thus, they can be used in a wide range of simulators such as SABER[17] and SIMPLORER [18]. VERILOG-A (a subset of VERILOG-AMS for handing analogy models) in [14] is identified as the *de facto* language for coding compact models. However, in this project, VHDL-AMS was chosen because despite having the same benefits of Verilog-A, the circuit network equations for models with internal nodes are automatically handled By the VHDL-AMS compiler (and do not need to be written in the model code), it provides the possibility to do complex modelling of digital and logic relations (which may be required in designing the control of power electronic circuits) for multidomain simulation. The author of this thesis had also had some prior experience in using VHDL-AMS and thus, saving the time that would have been used in learning to use Verilog-A. Snapshots of the VHDL-AMS equations for the components of Fig.2. 1 are shown in Fig.2. 2, Fig.2. 3, Fig.2. 4, Fig.2. 5 and Fig.2. 6.

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VHDL-AMS description of a simple capacitor model		
Library IEEE;	-library declarations that enable the use of predefined packages	
Library STD;	library declarations that enable the use of predefined packages	
USE IEEE.math_real.all;	specific aspect of the standardized IEEE library is called	
ENTITY Capacitor IS		
GENERIC (cap: REAL:= 1.	De-3);a parameter " cap" to signify capacitance is defined with a value of 1mf	
PORT (TERMINAL p,m: ELECTRICAL); PORT defines inputs and outputs; capacitor has 2 electrical terminals		
END Capacitor;		
ARCHITECTURE behav O	F Capacitor IS	
QUANTITY u_c ACROSS i	_c THROUGH p TO m;quantities across/though the terminals p and m (i.e. voltage and current)	
BEGIN		
l_c == cap*u_c'd	lot; simultaneous statement describing current voltage characteristic in a capacitor	
END behav;	observe how all statements are terminated by a semicolon	
QUANTITY c11: REAL;	free quantity. VHDL-AMS is case INSESNSITIVE	
BREAK c11:=> CAP;	BREAK statement used here to initialize the quantity C11 to the value of "cap" i.e. 1E-3	

Fig.2. 2: VHDL-AMS equation syntax with comments for capacitor

```
LIBRARY Jeee;
use leee.electrical_systems.ALL;
ENTITY pulse_thermalsource IS
GENERIC (
TD: REAL = 10.0e-9;
                                                     --DELAY TIME
Period: REAL = 5.0e-6-Period );
PORT (TERMINAL p,m: THERMAL); END;
----- ARCHITECTURE-----
ARCHITECTURE arch_pulse_thermalsource OF pulse_thermalsource IS
QUANTITY Tempa ACROSS powera through p TO m;
signal pulse_signal : REAL ;
BEGIN
pulse_signal<= power_high;
 if domain = quiescent_domain or domain = time_domain use
 powera == sign_power* pulse_signal'ramp(TR, TF); -- create rise and fall transitions
 else
 powera == sign_power* ac_mag* 2.0* 3.142*(ac_phase/360.0) ; -- used for Frequency (AC)
 end use;
CreateEvent : process
begin
 Wait until domain = time_domain;
 Wait for TD;
 loop
 pulse_signal <=power_high;
 wait for (PW + TR);
 pulse_signal <= power_low;
 wait for (period - PW - TR);
 end loop;
end process CreateEvent;
END ARCHITECTURE arch_pulse_thermalsource;
   ----- END VHDLAMS MODEL ----
```

Fig.2. 3: Equations for control signal to power device in VHDL-AMS language. The equations include digital relations and analogue equations

----- MOSFET model equations-----

Rnon_linear == RDO * (1.0+ TRS1*(T - Tnom) +TRS2* (T-Tnom) **2.0); -- temperature dependent drain resistance Kptmos == KP* (T/Tnom)**-kpx; -- temperature dependent transconductance Vtox == Vto- ktox*(T/Tnom); -- temperature dependent transconductance

Fig.2. 4: Temperature dependent MOSFET equations in VHDL-AMS language

VHDL-AMS (Very high speed integrated circuit Hardware Description Language-Analogue Mixed Signals) was used to describe the equations of the models created in this project. VHDL-AMS is an extension of the original VHDL (IEEE standard 1076-1993) which only described digital and logic circuits (i.e. discreet value-discreet time and continuous value-discreet time events). VHDL-AMS (IEEE standard 1076.1-1999) was created to include description and simulation of analogue mixed circuits [15, 16, 19] in addition to the discreet value-discreet time and continuous value-discreet time events that VHDL could already simulate.

The structure of a model created in VHDL-AMS model is the same as that of a model created with VHDL Language. It consists of an *entity* (In the entity, *ports* which represent the points of interface to the input or outputs of other models and *generics* where the model parameters are defined) and one or more *architectures*.

----- some mechanical equations

curvature_mech_6 == (6.0* E_Layer_6 * Thickness_layer6 *(alpha_layer_6 -alpha_layer_1)
*(Temp_AVG_Layer6- TREF)) *inv_Es_ts2 ;
TOTAL_STRAIN_mech_6 == C_mech + (hy_3 + hy_4 + hy_5 - TB_mech)* curvature_mech_1;
S_4_11_4 == E_layer_6 * (Total_strain_mech_11 - alpha_layer_6 * (T_4_11_4-TREF));
----stress for node 4_11_4

Fig.2. 5: Snapshot of some of VHDL-AMS mechanical equations used for description of one of the modules in Fig.2. 1

 $\begin{array}{l} T_1_1_1'dot == (\mbox{ const_mat_1}^{+} (T_2_1_1-T_1_1_1)/((X2-X1)^{+}(X2-X1)) \) \ -(\mbox{ hside}^{+}(T_1_1_1-Ta)/(X2-X1) \) \ + (\mbox{ const_mat_1}^{+} (T_1_2-T_1_1_1)/((Z2-Z1)^{+}(Z2-Z1)) \) \ -(\mbox{ hside}^{+}(T_1_1_1-Ta)/(Z2-Z1) \) \ + (\mbox{ const_mat_1}^{+} (T_1_2_1-T_1_1_1)/(hy_1 \ hy_1) \) \ - (\mbox{ hbot}^{+} (T_1_1_1-Ta)/hy_1 \); \end{array}$

 $\begin{array}{l} T_3_{13}'dot == (\ const_mat_7 \ ^{(T_4_{13}_3 - T_3_{13}_3)/((X4-X3)^*(X4-X3)) \) & - (\ const_mat_0 \ ^{(T_3_{13}_3 - T_2_{13}_3)/((X3-X2)^*(X3-X2)) \) + (\ const_mat_7 \ ^{(T_3_{13}_4 - T_3_{13}_3)/((Z4-Z3))^*(Z4-Z3)) \) & - (\ const_mat_7 \ ^{(T_3_{13}_3 - T_3_{13}_2)/((Z3-Z2)^*(Z3-Z2)) \) + \ PK_1/hy_{13} \ - (\ const_mat_7 \ ^{(T_3_{13}_3 - T_3_{12}_3)/(hy_{12} \ ^{hy_{12}}) \); \end{array}$

 $\begin{array}{l} T_14_13_2'dot == (hside^{+}(Ta - T_14_13_2)/(X14-X13)) & -(const_mat_7^{+}(T_14_13_2 - T_13_13_2)/((X14-X13)^{+}(X14-X13))) & + & (const_mat_7^{+}(T_14_13_3 - T_14_13_2)/((Z3-Z2)^{+}(Z3-Z2)))) & - & (const_mat_0^{+}(T_14_13_2 - T_14_13_1))/((Z2-Z1)^{+}(Z2-Z1))) & + & PK_2/hy_13 - & (const_mat_7^{+}(T_14_13_2 - T_14_12_2)/(hy_12^{+}hy_12))); \end{array}$

 $\begin{array}{l} T_14_13_3' dot == (hside^{+} (Ta - T_14_13_3)/(X14 - X13)) & -(\ const_mat_7^{+} (T_14_13_3 - T_13_13_3)/((X14 - X13)^{+} (X14 - X13))) & + & (\ const_mat_7^{+} (T_14_13_4 - T_14_13_3)/((Z4 - Z3)^{+} (Z4 - Z3))) & - & (\ const_mat_7^{+} (T_14_13_3 - T_14_13_2) / ((Z3 - Z2)^{+} (Z3 - Z2))) & + & PK_2/hy_13 & - & (\ const_mat_7^{+} (T_14_13_3 - T_14_12_3)/(hy_12^{+} hy_12))); \end{array}$

Fig.2. 6: Snapshot of some of discretized VHDL-AMS Thermal equations

used for description of one of the modules in Fig.2. 1

The architecture describes the operation of the component being modelled. This description could be coded in a structural description, behavioural description or a combination of both structural and behavioural description. A structural description
decomposes a model into several sub-components and shows the interconnections between the sub components (e.g. describing nonlinear voltage source using an ideal voltage source model in series with an ideal resistor model). Behavioural modelling description uses concurrent statements to describe event driven behaviour and simultaneous statements to describe continuous behaviour (e.g. differential and algebraic equations).

VHDL-AMS supports conservative systems- these are systems that obey energy conservation laws. To enable conservative system simulations, four features which have not been included in VHDL were added [19, 20]. These features are explained below and an example of their use is shown in Fig.2. 2 with comments shown after the dash"--"sign.

Simultaneous statements-These are statements used to describe continuous behaviour.

Quantities-These are the unknown parameters in Differential and Algebraic equations (DAEs). Their definition could be constrained to particular terminals or be unconstrained in which case they are known as *free quantities*.

Terminals- defines the through and across quantities in a domain

Break statements –used to manage discontinuities in a model description.

Models can be designed (i.e. written) with simple equations (as in Fig.2. 2 for the capacitor or can be made more complex to include additional effects such as temperature and geometry). Table.2. 1 [20] describes the *through* and *across* of various domains widely used in VHDL-AMS modelling. From the table, it can be seen that a multidomain system such as an aerospace or traction system with electrical

input, electric machines (which include a magnetic aspect) and mechanical shafts can be modelled using VHDL-AMS language.

	•	-
NATURE	ACROSS	THROUGH
Electrical	Voltage (V)	Current (A)
Thermal	Temperature (K)	Power (W)
Mechanical	Position (m)	Force (N)
Mechanical	Angular Velocity (rad/sec)	Torque (Nm)
(rotational)		
Magnetic	Magnetic force (Tesla)	Flux(Weber)

Table.2. 1: Technological domains of VHDL-AMS [20]

2.2 Numerical solution of ODEs

A model is simply a set of **mathematical** equations used to describe important characteristics of a device or system which when complied together and run in a simulator will display the output result expected of the device or system in real life operation. In power electronic applications, this can be further defined as a set of equations that provide an accurate description of dependent variables (such a current, temperature) as a function of independent variables (such as voltage, power). Given this definition, knowledge of advanced mathematics is important in this project. The equations generated in this project are classified as non-linear Ordinary Differential Equations (ODEs). While some equations used in the model may be simple linear equations, the most complex equations to be solved in this project are nonlinear ODEs. Thus, the simulator to solve the VHDL-AMS model equations must be capable of solving non-linear ODEs. The solution of non-linear ODEs is an in-depth field on its own. Interested readers are referred to [21],[22],[23]. However, a brief summary of the process of solving non-linear ODEs is given in this report because it enables model designers to design models that are computationally efficient and useable over a wide range of operating conditions.

The process of numerical solution of nonlinear ODEs is shown in Fig.2. 7. The circuit description and model equations are compiled into a netlist. Then, the nonlinear ODEs are resolved to nonlinear algebraic equations using numerical integration methods such as Euler, trapezoid or gear methods. Iterative techniques are then used to resolve the nonlinear algebraic equations into a system of linear equations. Once the linear equations have been derived, they can be solved using direct matrix techniques such as LU factorization or indirect matrix techniques such as the Gauss-Seidel method.



Fig.2. 7: Numerical solution process of ODEs [21],[23].

Generally, nonlinear ODE solvers (also known as nonlinear solvers) follow the numerical solution process in Fig.2. 7 although they may use different techniques at each step (i.e. a simulator may use Euler method for its numerical integration while another uses the Gear method). Nonlinear solvers could be custom built for solving nonlinear ODEs however, in this project, the portability benefit of VHDL-AMS allowed for the use of a commercial simulator already available in industry.

The three solution methods (numerical integration, iterative techniques and matrix techniques) were reviewed with focus on the methods used by the chosen commercial simulator [18]. Linear algebraic equations are usually relatively (compared to numerical integration and iterative techniques) easily solved. However, the numerical techniques and iteration techniques are usually the processes that require the bulk of computational effort. They are usually the cause of simulator issues such as error and non-convergence which have to be resolved in other to have computationally efficient simulation models. These simulation issues are discussed in the next subsection.

2.2.1 Common simulator issues

In this project, a review of numerical methods raised important concepts needed to achieve a reasonable balance between accuracy and computational efficiency when designing models. These concepts are error, convergence, consistency and stability.

Error is the difference between the exact solution of the original ODE and that of the numerical solution. Numerical integration involved the use of time discretization and the magnitude of the errors is related to the time step chosen. The obvious solution would be to ensure that the time step are as small as possible. However, such implementation would have a drastic effect on the computational cost. The balance was to use automatic time step control which would reduce the step size around regions of fast transition and increase the step size around regions of slow transition. This feature was available in the commercial solver used. However, the maximum (Hmax) and minimum (Hmin) time step must be set by the user. As a general rule in this project, Hmax was set at 1/20 of the simulation duration $\left(\frac{\text{End time}}{20}\right)$ and Hmin was set as $\left(\frac{\text{Hmax}}{10}\right)$.

Convergence (with respect to the numerical solution of ODEs) is a measure of how well the numerical solution approaches the exact solution of an ODE with a further increase in the number of iterations. In this project, it was monitored by observing the number of iterations that was needed by the simulator to solve the model equations in order to produce results within the tolerance limits set by the user. In the course of the project, the simulator will usually produce an error message-"*unable to converge, simulation aborted after Itermax Number of iterations*" (*Itermax* is a number which represent the maximum number of iterations parameter which is set by the user) implying that the model was unable to converge in a simulation. The knowledge of numerical solution methods was important to understand the equations which caused the error message and make the needed adjustments. In line with the knowledge gained about convergence, emphasis was given when designing models to design any model in this project in such a manner that it converges as fast as possible when used in simulation.

Iterative techniques used in this project (Newton Raphson method) never converge to give the exact solution. There would always be an error between the exact solution and the result from the iterative solution. Thus, a tolerance parameter is used. The simulator compares the difference between successive iteration solution values. If the difference is less than the tolerance value, the simulator halts the iteration process and uses the most recent result as its solution otherwise, it continues the iteration process. Clearly, the smaller the tolerance value, the less the error but at the expense of added computational effort. The reverse is the case for large tolerance values (i.e. low computational effort but higher error).

Another issue encountered with the use of the solution process in Fig.2. 7 is the presence of discontinuities. Consider the equation for Newton Raphson solution (NR) below.

$$x_{i+1} = x_i - \frac{f(x_i)}{f'(x_i)}$$
(2.1)

Here, f is the function and the solution required is x. $f(x_i)$ is the value of the function using the x value from the *i*th iteration the while $f'(x_i)$ is the derivative of the function using the x value from the *i*th iteration. When $(x_{i+1} - x_i)$ is less than a pre-set tolerance value, the x_{i+1} value is accepted as the solution for x else the iteration continues. Although the NR method is one of the best methods available for solving nonlinear algebraic equations (the commercial simulator used in this project uses the NR method), a number of issues can be highlighted from (2. 1). First, the denominator of the second term must not be zero nor a very low number else the solution will not converge. Next the initial guess i.e. x_0 has to be close to true solution x otherwise, it would take a long time to converge or the solution may not converge or may converge to a wrong value. Lastly, the nature of the denominator of the second term in (2.1) means the NR solution will struggle to solve functions which do not have continuous derivatives. Examples of such functions include conditional statements which give different values to a dependent variable for different conditions with sharp transitions between the different values, nonlinear functions and functions that are not piecewise continuous i.e. functions where for the same value of an independent variable, there could be more than one value for the dependent variable. Unfortunately, in power electronics, such functions occur a lot in the course of switching power devices. For instance, drain voltage values in a power MOSFET can switch from having high values in kV range to 0 almost instantaneously. Non-linear functions also occur in power electronics. An example below is an expression for drain resistance for the electrical model (see Chapter 3 for more on the electrical model)

$$r_{d_1} = (Rd_oL_r + \frac{V_{rd_1}}{ISAT})A_r$$
 (2.2)

At this point, it is not important to know what the terms in (2. 2) mean. All that needs to be known at this point is that V_{rd1} is the independent variable while r_{d_1} is the dependent variable- the drain resistance. Equation (2. 2) seems like a trivial equation to solve algebraically however, the summation of the first two terms (the first two



Independent variable

Fig.2. 8: Type of equation functions to be solved by the simulator

terms on the right side of the equal sign in (2. 2)) results in a function that is not piecewise continuous. The NR solver in the simulator will struggle to solve such equation. Fig.2. 8 summarises the possible type of model equations encountered in

this work in graphical form. The best type of equations for the NR solver are linear functions and piecewise linear equations because they are smooth, continuous and without steep gradients. Thus, in the course of the projects, emphasis was placed on linearizing equations as much as possible or using piecewise linear equations.

Repeatedly having to deal with "problematic" equations, a checklist was developed in this project which help to rewrite such equations in a way that they can be handled by the simulator with minimal computational effort. This is discussed in the next subsection.

2.2.2. Guide for writing model equations in VHDL-AMS

In the course of the project, from the study of the processes in Fig.2. 7, review of material such as [17, 18, 22, 23] as well as trial and error, a number of lessons have been gained when solving non-linear ODEs in power electronic applications. Some could be as simple as initializing all independent variables to a non-zero value to prevent the value of $f'(x_i)$ in (2. 1) from being zero. Others involved replacing conditional statements with the use of mathematical functions to avoid discontinuity [24].

Thus, based on this experience, a checklist was created. This checklist was used in developing solution to modelling/ convergence issues that limited the solvability of the models developed in this project. The checklist can be seen in Table.2. 2.

Table 2 2. MODEL DESIGN CHECKLIST	14 22 25
TUDIC.2. 2. WODEL DESIGN CHECKEIST	

S/N	CHECKLIST ITEM	DONE?
	SYNTAX/BODMAS	
1	Check all equations for syntax errors.	
	Simulators may not be good at pointing out simple comma or	
	semicolon termination errors.	
2	Check All Brackets (), multiplication and division in equations	
	and confirm that they follow BODMAS rules.	
	If unchecked this may not affect convergence but lead to	
	wrong results	
3	Check that the code is segmented reasonably	
	Keep temperature dependent equations, initializations in	
	together	
4	Give meaningful names to variables and parameters that can	
	make any end user have an intuition of what each variable	
	represents/ is doing.	
	Using <i>Temp</i> to indicate inductance is not good model design-	
	most engineers associate <i>Temp</i> with temperature	
	CIRCUIT/ QUANTITY DECLARATION/ CONSERVATION LAWS	
5	Check component connections and across/through quantity	
	declarations are defined correctly.	
6	Check in VHDL-AMS models that NO across quantities are	
	defined in parallel with each other and no Current sources in	
	series with each other.	

	If such connections exist, one will have to use series resistor	
	(for voltage sources in parallel) and shunt resistor (current	
	sources in series) when necessary.	
	NOTE:	
	in SIMPLORER [18] VHDL-AMS simulator algorithm:	
	Capacitor is treated as a voltage source	
	Inductor is treated as a current source	
7	Check that every defined VHDL-AMS quantity has a matching	
	equation	
	For the conservative quantity, at least one of the across/	
	through quantity MUST be used in equation.	
	For the free quantities- it must also have an equation. Even if	
	initialized at definition. An equation must still be given in the	
	architecture of the model	
8	Check every ENTITY parameter (input parameters) used in	
	model has been initialized to non-zero values.	
	Even though some parameters may have zero values,	
	possibility of division by zero leading to convergence issues	
	have caused us to prefer to initialize all parameters in the	
	model to non-zero values (instead of 0, we use a small value	
	like 0.001)	
9	Draw the model according to quantity across and through	
	declarations in the VHDL-AMS architecture and ensure	
	conservation laws are met.	

	This provides a check and helps identify possible sources of	
	convergence errors even before simulation commences.	
10	Assign a range to your model parameters to avoid "Garbage	
	in, Garbage out".	
	For each of your architecture parameters know the Limit with	
	respect to the model- how far positive or negative their values	
	can be and limit as such	
	(for entity parameters since they don't change in simulation	
	just put limit in commentfor end users);	
11	Watch for derivatives of built-in functions such abs(x), sqrt(x)	
	etc because their first derivatives are discontinuous around	
	x=0.	
	Either add 0.01 to the argument(x) in the function	
	OR	
	force function to a value when the argument is 0	
12	Substitute expensive functions like exp(x), pow(a,b) with	
	limited exponential functions that limits the maximum and	
	minimum exponential term.	
	In VHDL-AMS, exponent terms should not be lower than -34 or	
	higher than +34 for convergence.	
13	Add a small value with the variable in a Log or Ln function	
	which can attain zero value.	
	Dependent_variable=ln(Independent_variable +small value)	
14	For Electrical model equations with 'dot (differential	
	equations)	

	In capacitor 'dot equation; DO NOT put 'dot in if then else or	
	other conditional statements;	
	Use c=0 in DC and c= 1in TR in an if-then-else statement;	
	and then put a single i= c*V'dot equation instead of	
	conditional statements	
	Do same for inductor (with the current value rather than	
	voltage as done in the capacitor equation above)	
15	Use BREAK to assign values to dependent variables in regions	
	of discontinuity (In VHDL-AMS models).	
	By forcing the simulator to start iteration from a defined value,	
	convergence occurs faster	
16	When doing a power function a^2 , DO NOT use a**2.0	
	rather than put $a^{**2.0}$ It is computational cheaper to put a^{*a}	
	CHECKING EQUATIONS IN NON CONVERGING MODELS	
17	When faced with convergence errors or unusually large or low	
	results for across or through quantities	
	Check all OUTPUT parameters for unusually large or	
	unusually low parameters.	
	From experience, they are usually the likely cause.	
18	Check for any equation where a calculated quantity in one	
	time step is also required to calculate another derived	
	equations in the SAME time step? (For example, a derived	
	current from current equation in a current source used to	
	calculate voltage drop across resistor in series with it)	
	such occurrences should be removed or modified immediately	

19	Remove all DAEs from the model; replace large equations	
	with v=0; the equivalent of a wire.	
	Gradually place and recompile the equations beginning with	
	simple equations, then ODEs and then nonlinear equations;	
	The equation(s) that after you add and recompile the model	
	that leads to error is most likely the problematic equation(s).	
20	Check that DAEs causing the error from checklist 15 (above)	
	can easily produce a result with standard numerical	
	integration methods	
	This can be done using standard numerical integration check	
	tools available online.	
21	If the DAE fails the check above, it is most likely there is a	
	discontinuity	
	Check using numerical integration tools (available online) or	
	by adjusting the values to your simulation for the range of	
	input values where discontinuities exist	
	One could then implement simple changes to fix the output at	
	the range of discontinuity allowing the simulator algorithm to	
	run only outside the discontinuity range	
22	Check to see if adding a small constant (in the 0.001- 0.01	
	range) multiplied by every independent variable or quantity	
	in the problematic DAE leads to convergence.	

	OTHER GOOD PRACTICES				
23	For temperature dependent electrical equations , it is				
	suggested that the equations can be in the form of				
	" (T/Tnom)**constant "				
	rather than				
	(T-Tnom)** constant				
	Thus, it will not matter if model users enter temperature in K				
	or ^o C, the result will be the same.				
	Although writing temp dependent equations in "				
	(T/Tnom)**constant " form leads to non-linear equations, in				
	our experience this has not given us issues				
24	For complex electrical models such as used in this project for				
	power devices, it is a good idea to implement a scheme in the				
	VHDL-AMS model to initialize all capacitor currents to zero in				
	the quiescent (DC) domain.				
	This has been seen to aid convergence for DC simulations				
	It is also good to initialize inductor voltages to zero in quiescent				
	(DC) domain.				

2.3 CONCLUSION

In this chapter, two critical constituents of this project- the modelling language and numerical solution of Ordinary Differential equation (ODEs) were reviewed. The requirements for the modelling language to be used to describe the equations of the models generated in the project were discussed. The reason for the choice of VHDL-AMS as the modelling language was also discussed.

The presence of nonlinear ODEs in some of the equations in the models generated in the project required the knowledge of numerical solutions in order to design models that can be solved relatively easily by standard nonlinear ODE solvers. Based on the understanding of nonlinear ODE simulation process and experience gained during the project, a guide for designing complex device models for use in power electronic applications was presented in this chapter. The models designed in this work based on this guide are presented in the following chapters.

CHAPTER 3- SEMICONDUCTOR DEVICE MODELS (ELECTRICAL ASPECT OF MODELLING METHODOLOGY)

3.1 INTRODUCTION

The semiconductor power device model represents the chip (chip layer) and is used to produce results for analysis in subsequent chapters. The chip layer is the primary source of heat (power loss) in the power module (see the description of power module assembly in Chapter 1 for more information) and the value of power loss from the chip layer is influenced by the physical and electrical characteristics of the chip layer. Thus, it is important that this layer is discussed in full detail. In this chapter, the main factors that guide the electrical design of power devices are outlined, existing device models are reviewed and the semiconductor model designed by the author is presented. The model is designed to predict the output characteristics and power loss values of a SiC MOSFET power device. The model is validated on the basis of static simulations and the capability of the model for use in multichip transient simulation is shown.

3.2 Physical and Electrical Properties

When designing a semiconductor device for power electronic applications (ideally zero current when OFF and zero on-state voltage when ON), there are two major factors that must be considered usually with trade-offs between them for achieving optimum device performance. These properties are current conduction (on- state) and voltage blocking performance. In this project, the main device modelled electrically is the power MOSFET. It is currently realised using the VDMOS (Vertical Double- diffused MOSFET) structure shown in Fig.3. 1.



Fig.3. 1: Structure of Power MOSFET reprinted from [26]

The on-state performance equation for a unipolar device as is the case of power MOSFETs (only electron conduction) with current flow primarily due to the drift mechanism is shown in (3. 1) [27].

$$\vec{j} = q\mu_n N_d \,.\,\vec{\nabla}V \tag{3.1}$$

Here, *j* is the current density A/m²], *V* is the electrostatic potential , *q* is electronic charge , μ_n is the electron mobility (the equation above assumes that the electron is the majority carrier), N_d is the dopant carrier concentration (cm⁻³).

A direct relationship between current density and electrostatic potential can be derived from (3. 1). This relationship is known as the specific resistance (ohm/cm²).

$$R_s = \frac{W}{q\mu_n N} \tag{3.2}$$

Here, W represents the width of the drift region (see Fig.3. 1) and N is the total concentration.

It is desirable to have the specific resistance value as low as possible because it leads to lower conduction losses. It can be seen from (3. 2) given that q and μ_n are fixed, that in order to have low R_s values, it would be necessary to have high levels of doping to increase the carrier concentration and also necessary for the width of the drift region to be as small as possible.

The second factor to consider is the voltage blocking performance. Optimum blocking performance necessitates that the doping level (of the material to be used to manufacture the power device) be as low as possible. The blocking performance is the ability of the device to withstand high voltages without breaking down when the device is OFF. The device breakdown voltage is inversely related to the carrier concentration as shown in (3. 3) [27].

$$V_{bd} \propto \frac{\varepsilon_r}{2qN_d} E_c \tag{3.3}$$

Here, V_{bd} is the breakdown voltage, ε_r is the relative dielectric is constant, E_c is the value of the critical electric field.

It can be seen from (3. 3) that a high value of breakdown voltage necessitates the doping and carrier concentration to be as low as possible which is contrary to the high doping requirement for low specific resistance (see (3. 2)). The voltage blocking is contained across the width of drift region of the device [27] thus, there is a minimum width that the device must have for voltage blocking capability. The value of the minimum width depends on the blocking voltage and the relationship is shown in (3. 4) [27]

$$W_{min} \propto \sqrt{\frac{2\varepsilon_r}{qN_d}} V_{bd}$$
 (3.4)

which implies that because the width cannot have a value of zero (as would be favourable for low specific resistance (see (3. 2)), there will definitely be on-state voltage loss in the device (see (3. 2)).

The search for better solutions rather than being limited to trade-offs using Silicon (Si) led to the development of alternative materials to use instead of Si. One of the alternative materials is Silicon Carbide (SiC). The potential for SiC arises from a number of its material properties. These properties are highlighted in Table.3. 1.

3.2.1 Comparison of Si and SiC material properties

The critical electric field for SiC is about 7 times higher than that of Si. Thus from (3. 3), it is theoretically possible to get higher values of V_{bd} for the same device area or for the same V_{bd} value, the value of N_d can be greatly increased which (3. 2) will result in better on-state performance (i.e. lower on-state resistance) than in Si.

The intrinsic carrier concentration (N_i) of SiC is far less than that of Si (approximately 18 times). Power devices are fully controllable when N_d is greater than N_i . ("controllable" here means operating within safe operating area (SOA) conditions; At room temperature, the N of a device majorly consists of N_d enabling ability to set and expect a specified range of electrical characteristics; however with increased operating temperature when N_i becomes comparable to N_d , N no longer consists majorly of N_d and the device becomes unstable – resulting in outside of SOA operation (e.g. avalanche, short circuit) close to the occurrence of device failure).

Property	Silicon	4H-SiC
Band gap, Eg(eV)	1.12	3.26
Intrinsic Carrier concentration N _i	1.45 X10 ¹⁰	8.2 X10 ⁻⁹
(cm⁻³) at room temperature		
Electric critical field, E_c (kV/cm)	300	2200
Electron mobility, μ _n (cm²/Vs)	1500	1000
Thermal conductivity, K (W/cm K)	1.5	4.9
Saturated electron drift velocity,	1	2
Vsat(x10 ⁷ cm/s)		

Table.3. 1: Physical Characteristics of Si and SiC [3, 27]

The temperature of a power device increases during operation of the device and N_i has a direct relationship with temperature. Thus, a significantly lower value for N_i at room temperature theoretically implies that SiC power devices can operate at higher temperatures than Si (though practically the operating temperature of a power device is limited to that of the materials used to package the device) or for the same performance, devices can be made to block higher voltages (see (3. 3)).

The bandgap of SiC is about 3 times than that of Si. The bandgap is the energy required for electrons in the valence band of a material to break into the conduction band increasing the current density of the material. With a higher bandgap, few intrinsic electrons N_i will possess the bandgap energy even at high temperatures (recall than when N_i equals N_d in a material , a device made with such material becomes unstable) resulting in a higher temperature operation limit of a material

[26]. Device failure mechanisms such as avalanche failure are related to the activation of the parasitic BJT (see Fig.3. 1) due to the reduction in the p-n junction forward bias voltage with increasing temperature[27]. SiC is more robust to handle these condition due to its wide bandgap because more energy is required in avalanche conditions to result in device failure than in Si.

The thermal conductivity of SiC is also 3 times higher than that of Si. The temperature rise in a device is described by (3. 5)[27]:

$$\Delta T = P_D R_{th}$$

(3.5)

$$R_{th} = \frac{1}{K} d$$

Where ΔT represents temperature rise, P_D represents dissipated power density, d represents device thickness, λ_0 represents thermal conductivity and R_{th} represents thermal resistance.

The relationship in (3. 5) shows that a material (such as SiC) with higher thermal conductivity will have a lower thermal resistance and thus a lower temperature rise for the same power dissipated compared to a material with lower thermal conductivity (such as Si) resulting in smaller heatsinks, smaller thermal management designs, smaller electro-magnetic filters. This leads to power converter designs with smaller weight and high power density which is beneficial in space-constraint power electronic applications such as aerospace applications. In order to observe the advantages of SiC in manufacturing power devices explained above for device level and system level simulations, it is important to generate accurate compact models for

use in simulation. To model the SiC power MOSFET, a compact SiC power MOSFET model was created.

3.3 SIC POWER MOSFET

The chip layer in the multilayer power assembly (see chapter 1) may comprise of a single chip or a number of chips (multi-chip modules). In the case of multichip modules, an electrical model can be used to represent multiple chips if the chips are of the same semiconductor (e.g. for two identical SiC MOSFETS in a module- the electrical model will be the same for both of them). In this section a review of SiC power MOSFET models available in literature is presented and a discussion on the model designed in this work - explaining its electrical characteristics, important equations and parameters is given.

3.3.1 Main Behavioural Features

The main behavioural features of the SiC MOSFET are derived from its physical structure. The physical structure used in the MOSFET model described in this chapter is the VDMOS (Vertical Double- diffused MOSFET). The VDMOS structure is shown in Fig.3. 1. The structure consists of three main terminals- the gate, source and drain terminals. Five main layers can be seen in Fig.3. 1 namely the n+ substrate (at the bottom), the n- drift region, the p-body (or p-base), the n+ (source) region and the gate. The interaction between these layers and the movement of electrons through these layers produce some features which are responsible for the nominal (output and transfer) characteristics of the SiC Power MOSFET.

One of these features is the on-state resistance [28]. Although it is not the only cause of voltage drop in the device, it is responsible for significant amount of voltage drop in the device. The on-state resistance R_{DSON} is a sum of all the resistances to the

movement of electrons from the source to the drain (see Fig.3. 1). This includes the resistance in the channel region (channel resistance), resistance at the source (source resistance), resistance at the drift region (drift resistance) and resistance at the substrate region (substrate resistance).

Another important feature is capacitance [29]. Capacitance effect also occur due to the structure of the MOSFET. The interaction between the gate, gate-oxide and drift region results in a gate-drain capacitance C_{gd} while the interaction between the drift layer and p-body results in a drain-source capacitance C_{ds} . The interaction between the gate, gate-oxide and the N+ region of the source creates a gate-source capacitance C_{gs} . These capacitances need to be charged and discharged when turning ON and OFF the MOSFET- thus they determine the switching speed (and transient characteristics of the MOSFET). In conjunction with any parasitic inductances in power electronic circuits the capacitances also lead to voltage overshoot during switching transitions which can damage the MOSFET if the peak voltage of the overshoot is higher than the breakdown voltage of the MOSFET.

It is important that the model chosen in this project capture these features in circuit simulation. In choosing the model to use, it was important to review existing models in literature. This is discussed in the next sub-section.

3.3.2 Compact Models

3.3.2.1 Types of Models and need for accurate physical compact models

Mantooth [30] stated it best with the following description of a compact model. "The basic objective of a compact device model is to produce a predictive description of the current flow through the device as a function of applied voltages across the device, currents, environmental conditions (e.g. temperature) and physical characteristics (e.g. geometry). A compact model is a model that can be used in circuit

simulators [30] ". There are five major types of models [30] used in simulation of Power electronic devices and circuits. They are

- (a) Empirical
- (b) Semi-empirical (or semi-physical)
- (c) Physical
- (d) Semi numerical
- (e) Numerical

Empirical models are models that comprise of curve-fitted equations. The parameters in the model are not related to the physical effects (main behavioural effects) that determine the operation of the device but such models are used in practice because they are computationally fast to simulate and give the needed results in applications where the user is not interested in observing physics based effects (a typical situation would be when a power electronic designer is at the topology selection phase of a power converter design where detailed information on switching transients is not usually required[8]).

Semi-empirical models involve some physics based equations (i.e. equations of physical effects which determine the static and dynamic characteristics of the device) but still have equations that have no direct relation to the physics of the device (i.e. non-physics based equations).

Physical models consist of physics based equations. Though some of the equations describing significant physical effects in the device may be simplified [30], the equations still have direct physical relation to the operation of the device.

Semi numerical models are partly physical and partly numerical models while numerical models directly solve complex equations that govern a specific domain (for example, transport equations for electrical domain and heat equation for thermal domain) over the geometry of the device based on detailed information of the device's material properties and geometry. The results from numerical models are usually very accurate due to the level of detail used in the model. However, this approach has a high computational cost as simulators require more time to handle the partial differential equations that need to be solved when using numerical models.

In choosing what kind of model to use for the electrical characteristics of the Power MOSFET in this project, a number of power MOSFET models were reviewed. Three criteria were used for evaluating the models- accuracy, computational efficiency and the ease of use in multi-domain simulations. The comparison of the reviewed models is summarised in Table.3. 2. Six models were reviewed- one is a semi-numerical model and five are physics based models (although some had some empirical functions added to them).

Potbhare [31] proposes a semi-numerical model. It presents a detailed description of SiC physical effects – interface trap densities, columbic interface scattering, surface roughness scattering, phonon scattering, velocity saturation was presented as well as the dependence of these effects on temperature and bias [31]. The model is very accurate however, it is computationally expensive to simulate a model with that level of detail for large complex power electronic simulations such as the multidomain simulations done in this project.

The model proposed by Hefner [32] is a physics model for a Si IGBT device. Although the model is for a Si device, it was reviewed because many other models in use in research/industry have been built based on the parameters/equations used in the model. The model's MOSFET characteristics were derived from lateral MOSFET models and adjusted for the vertical structure of power MOSFET.

McNutt [25] presents a physical model which builds on the principles in Hefner [32] with parameters adjusted for SiC material. A major contribution in this model was improvement in the channel current description by an enhanced linear region transconductance. A number of non-physical equations/parameters were added to fit the static characteristics of SIC MOSFETs which includes the use of high and low transconductance parameters for both the linear and saturation region. The model is accurate and computationally efficient. However, the JFET region resistance is not described physically and the use of multiple equations for the a channel current can lead to convergence issues due to discontinuities that could arise in transitioning from linear to saturation region of operation of the power MOSFET when the model is used in simulation.

Fu [33] also presents a physical model. It describes the JFET region in the MOSFET using a nonlinear voltage source and a resistance network. This contributes to the accuracy of the model. One equation is used to describe the main MOSFET current eliminating the need for multiple equations to describe current thus improving the model computational efficiency. The model was also presented to show good matching with FEA and experiment. However, the resistance network and nonlinear voltage sources introduce extra nonlinearity to the model equations which require added computational effort to solve. This will lead to increased simulation time when used in multi-domain simulations.

	mouchi	ing methodology o		
First Arthur	Model Level	Contributions	Advantage to	Disadvantage
			modelling	to modelling
			methodology	methodology
Hefner[32]	Physics	MOSFET	accurate; most	SiC MOSFET has
		characteristics	SIC MOSFET	some features
		represented in the	models are	that this model
		IGBT model: uses	based on ideas	does not capture.
		lateral	presented in	
		microelectronic	this approach	
		equations (BSIM	tine appiedent	
		SPICE models) but		
		with adjustments		
		for Power devices		
McNutt[25]	Physics	built on	Accurate: fast	IFFT region drain
Menuel[25]	T Try Sico	Hefner[32]	simulation	resistance not
		equations	time	described.
		adjusted for SiC	usable in	multinle
		temperature	multidomain	equations for
		denendent	simulations	drain current can
		material	simulations,	lead to
		nronerties:		
		improvement in		issues which
		channel current		need to be
		description by		nronerly
		enhanced linear		managed
		region		managea.
		transconductance:		
		High and low		
		transconductance		
		for both linear		
		and saturation		
		regions		
Pothhare[31]	Semi-	Detailed SIC	Accurate	computationally
1 0 00101 0[01]	numerical	physical effects –	detailed model.	expensive due to
		interface trap		the level of detail
		densities		in the model.
		coulombic		cannot be used
		interface		in complex PF
		scattering among		circuits with
		others.		many other
		othersi		components:
				coupling to other
				domains not
				possible.
Riccio[34]	Physics	Validation at high	accurate	Dependence on
	,	temperatures and		datasheet may
		out of safe		not be feasible
		operation region		for all devices
		conditions:		
		influence of		Computational
		interface traps on		expensive in
		threshold voltage		multidomain
		and channel		simulations
		mobility		

Table.3. 2: Comparison of Published SiC Power MOSFET models based on the modelling methodology of this project

First Arthur	Model Level	Contributions	Advantage to modelling methodology	Disadvantage to modelling methodology
			methodology	псспосоюду
Kraus[35]	Physics	influence of interface traps on electron density and mobility; RJFET resistance	Significant SiC physical effects mentioned; usable in multidomain simulations; accurate, computationally efficient	subcircuit nature of model could lead to numerical convergence issues during simulation
Mudhalkar	Dhusies	builds on	Accurates	Not foosible for
[36]	Physics	Mcnutt [25] and introduces transition parameter for gradual transition of drain current from linear to saturation;	Fast; All equations written as one model- no subcircuit model thus reducing possibility of convergence issues.	not feasible for new devices with no comprehensive datasheet; JFET effect not captured physically; no mention of interface traps.
Fu[33]	Physics	Describes non-	One equation	Drain resistor
		uniform current distribution in JFET region of MOSFET using nonlinear voltage source and resistance network.	for main MOSFET channel current; Accuracy- good matching with FEA and Experiment	network adds extra nonlinearity to the model equations which require high computational effort to solve.
Shintani[37]	Physics	MOSFET model	Current voltage	Complex surface
		based on surface potential.	and capacitor voltage validated over a wide range of operating conditions	potential equations require high computational effort in multidomain simulations Modelling of interface trap I limited
Sun[28]	Physics	Low temperature validation (as low as 248K); Negative gate drive voltage is taken into account	Accurate	subcircuit description for C_{gd} will require high computational effort when used in coupled multidomain simulation

Table.3.2: Published SiC Power MOSFET models (continued)

Sun [28] proposes a physics based model using temperature dependent voltage and current source to describe the static characteristics of the SiC MOSFET. Low temperature validation as low as 248K is presented and negative gate-drive voltage for SiC MOSFET is taken into account. However, the subcircuit description for C_{gd} will require high computational effort when used in coupled multidomain simulation.

Mudholkar [36] builds on the model presented in McNutt [25] and presents a physics model with a transition parameter for gradual transition of the MOSFET current from linear to saturation region. A parameter extracting strategy requiring only the device datasheet (no experimental characterization needed) to characterize the device was introduced in this work. The equations of all components in the model were written out without the use of internal nodes thereby reducing the possibility of convergence issues that come with the design of models as sub-circuit composition of models. The model is accurate and fast to simulate. The However, the JFET region resistance was not described with physics-based equations.

Kraus [35] provides a compromise between the models presented above. It builds on the model equations presented in Mudholkar [36] and McNutt [25] but still describes important SiC physical effects such as interface traps and JFET resistance using the ideas presented in Potbhare [31] and Fu [33]. Interface traps are accounted for in the channel current equation by the reduction in the mobility and electron density equations. Also the JFET region in the MOSFET can be modelled as a subcircuit component (individual resistance) rather than a resistor network as done in Fu [33]. This approach produces a model that is accurate enough to be used in multidomain simulations while being computationally efficient. However, the sub-circuit

composition of the model introduces convergence issues which have to be properly managed with when using the model in multidomain simulations.

Shintani [37] proposed a physics based sic mosfet model based on surface potential. The interface traps in the oxide-semiconductor interface are described. Also, the current- voltage and capacitor-voltage characteristics of the MOSFET are validated over a wide range of operating conditions. However, the modelling of interface trap is limited because it is treated as a linear function of temperature which is not the case throughout the temperature range [31, 34]. The surface potential model equations are relatively complex (compared to other physical compact models reviewed in this sections) and would require high computational effort to solve when used in multidomain coupled simulations.

Riccio [34] presents a physics based electro-thermal power MOSFET model with the static characteristics derived from physics based equations while the transient characteristics were described by curve-fitted capacitance equations. An analytical exponential expression is given for the temperature dependence of threshold voltage although no dependence of threshold voltage on gate-source voltage[35] is given. The model is validated at high temperature ranges (>470 K) and even out of safe operating area (SOA) operations such as avalanche and short circuit conditions. Significant effort is also put into deriving expressions for the mobility taking into effect the positive temperature coefficient effect at low temperature and negative temperature coefficient at high temperature.

After reviewing the models above, the approach of Riccio [34] was chosen to build the Power MOSFET model. The reasons for this choice include the representation of the effect of interface traps on the threshold voltage and electron mobility in the transistor channel; the ability to use one subcircuit component (individual resistance)

to model the resistance effects in the drain region (such as the JFET effect in the drain region), ease of model parameter calibration and the accuracy of the model in transient tests presented in [34]. Compared with the model presented in [35], the approach in [34] does not have logarithmic functions which from the author's experience (and in discussions with the simulator software designers are currently difficult to solve on the SIMPLORER [18] platform) Where empirical equations were used to represent physical effects, the parameters are still closely related with physical effects the equations describe thus, providing a good trade-off of usability in multichip simulations with reasonable computational effort while still allowing for the investigation of the physical parameters in power electronic applications.

3.3.3 Power MOSFET Model

Using the approach in Riccio [34], the model used in this project for the power MOSFET is a subcircuit of controlled current sources, nonlinear and linear passive elements. The structure of the model is shown in Fig.3. 2.. The capacitance from gate to source C_{gs} shows very little change with voltage and is thus assumed constant while the drain–source capacitance and drain –gate capacitance are dependent on the drain–source voltage. In this work, the SiC MOSFET modelled is the SiC Power MOSFET 1200-36A manufactured by Wolfspeed [38]. The model is parametric model-the end user does not need to understand or adjust any of the equations. Rather, all the user needs to do is amend the parameters which are in the VHDL-AMS entity (see Chapter 2) which are easily adjustable from the schematic of the simulator being used to simulate the test circuit. Thus, the proposed implementation (Fig.3. 2) can in principle be applied to any other SiC power MOSFET with similar physical effects provided that the parameter values are calibrated just as the parameters of the 1.2kV SiC MOSFET of [34] were modified and used to model a 3.3kV SIC MOSFET as shown

in [39] . In this section, the Device under Test (D.U.T) whose experimental results the proposed model aims to replicate is the Wolfspeed SiC 1200-36A [38].



Fig.3. 2: Power MOSFET model

3.3.3.1 MOSFET equations

This section describes the equations in the power MOSFET model.

(1) Threshold voltage

The threshold voltage is an important parameter in fully controlled semiconductor devices such as the power MOSFET. This is because it determines the formation of the channel [35] through which electrons can flow through the device (the current flow). The threshold voltage for SIC MOSFETs is highly dependent on the density of interface traps on the oxide-semiconductor interface (SiO₂/SiC interface) which is temperature dependent [34] and also dependent on the gate voltage [35].

Interface states exist in the energy bandgap of SiO₂/SiC interface increasing towards the conduction band edge [34] [35] and any electron that occupies

those states is "trapped' there by reducing the electron density free to flow across the MOSFET channel. As temperature increases, less interface states are occupied with electrons [40] leading to more electrons in the depletion region[34]. The occupation of interface trap states with electrons increases with increasing V_{gs} . Until all trap states are filled [35]. Temperature depended of threshold voltage is defined in the equation below

$$V_{t0x} = V_{t0} - k_{tox} \frac{T}{T_{nom}}$$
(3.6)

here, V_{t0x} (unit V) is the temperature dependent threshold voltage, V_{t0} is the threshold voltage at room temperature, T is the device temperature, T_{nom} is the nominal (ambient) temperature and k_{tox} is the threshold voltage coefficient.

(2) Transconductance

The Transconductance is an important parameter that determines the current handling performance of controlled devices (such as BJT, MOSFET, and IGBT). It is dependent on material properties (mobility and geometry) and is defined as:

$$K_p = \mu_n C_{OX} \frac{w}{l} \tag{3.7}$$

here, K_p represents Transconductance at nominal temperature, μ_n represents conductivity, C_{OX} represents oxide capacitance, $\frac{w}{l}$ is the width to length ratio of the device (see Fig.3. 1).Transconductance is also temperature dependent and this relation is defined as:

$$K_{pt} = K_p * \left(\frac{T}{T_{nom}}\right)^{-xk}$$
(3.8)

here, K_{pt} is the temperature dependent Transconductance parameter, xk is the transconductance temperature coefficient, T and T_{nom} are device temperature and nominal temperature respectively.

(3) On-state resistance

On-state resistances has been discussed under section 3.3.1. The temperature dependent equation for the on- state resistance R is defined as

$$R = R_{D0} (1.0 + T_{RS1} (T - T_{nom}) + T_{RS2} (T - T_{nom})^2$$
(3.9)

here, R_{D0} is resistance at nominal temperature, T_{RS1} and T_{RS2} are temperature coefficients.

(4) Body-diode saturation current

The Power MOSFET has an internal body diode from the p-n junction in its structure (see Fig.3. 1). To calculate the diode equation, we require the saturation current parameter. This parameter is temperature dependent and is defined as

$$Isot = ISO\left(exp\left(\left(\frac{T}{T_{nom}} - 1\right)EG\frac{N}{Vt}\right)\left(\frac{T}{T_{nom}}\right)^{\frac{XTI}{N}}\right)$$
(3.10)

(5) Avalanche breakdown generation rate

Power devices do not have zero current through when OFF as in ideal conditions. In normal operation of a power MOSFET, a low magnitude current (reverse leakage current) flows through the device when OFF. However, if the voltage across the device in the OFF condition exceeds a threshold, the electric field across a junction in the semiconductor exceeds a threshold known as the critical electric field. When this happens, a sizeable amount of electrons (or holes) will possess enough energy to break free valence electrons from their bonds allowing them to move into the conduction band. The newly free electrons also possess the energy to break free other electrons giving rise to a cascading effect regarded as impact ionization or avalanche generation [41-43]. When this occurs, the device begins to conduct a large current when OFF leading to the destruction of the semiconductor. The avalanche generation rate parameter *Gav* is required to compute the value of the reverse (breakdown) current. *Gav* has an exponential relationship which defined in [35] as:

$$Gav = a \exp \frac{-b}{E}$$
(3. 11)

here, a and b are constants which are determined based on material properties and E is the electric field in the region.

(6) JFET region Resistance

The JFET region resistance is an important physical effect to consider in SiC power MOSFETs fabricated using the structure in Fig.3. 1. As it can be seen in Fig.3. 1, the current from the channel has to flow through a relatively small

area (with respect to other regions in the path of current flow) therefore, the resistance in the JFET region will be higher than other regions in the path of current flow. The resistance of the JFET region is calculated [35] using

$$R = \frac{W}{q \,\mu \, N_d \,A} \tag{3.12}$$

Here, q is charge, μ is mobility, W is the width of the JFET region (the region in the drain of the MOSFET where current flow is constricted because of the expansion of the depletion region with increasing drain voltage [35]), N_d is electron concentration and A is area. Deriving the value of l and A is usually not trivial but it can be done analytically through physics based mathematical equations as done in [35].

3.3.3.2 Parameter List

The SiC MOSFET power device model is designed as a parametrized model. Thus, it makes it easy for engineers with little modelling experience to use the model and make adjustments with ease. This approach also makes it possible to model new devices when one may not have accompanying datasheets when they were released by the manufacturer. To extract the parameters in the SiC MOSFET model deigned in this work, the steps below were used.

- (1) Based on main behavioural features, equations are generated with parameters to be derived.
- (2) The needed experiments were performed or extracted to obtain needed measured results.
- (3) Based on visual observation or calculations (slope, intercept of graphs, derivatives) on the measured results, values for the parameters at room temperature were derived.
- (4) Results at different temperatures were compared and temperature dependent coefficient- parameters were calculated.
- (5) The room temperature values of the parameters and the temperature dependent coefficient parameters were inserted into the model and used in simulations. After which a comparison was done between the simulation results with experimental results.
- (6) The parameter values were optimized to get parameter values that make the difference between experimental and simulated results as small as possible.

Applying the steps above to the MOSFET model (SiC Power MOSFET 1200-36A manufactured by Wolfspeed [38]), the equations in the model are highlighted in section 3.3.1. DC calibration of the model was conducted using transfer characteristic and output characteristic tests at constant temperature. K_p was extracted from the slope of the transfer characteristic at room temperature. V_{tox} was extracted from the intercept of the transfer characteristic at room temperature. The channel length modulation parameter (*LAMBDA*) was derived from the output characteristic at low V_{gs} in saturation mode ($V_{ds} >> V_{gs} - V_{tox}$) [34, 44]. The transfer and output characteristic were then repeated at different temperatures [39, 44] from where the threshold voltage coefficient aTH and bTH was derived. r_0 , r_1 and r_2 were obtained from output characteristic values extracted at different temperatures using optimization (or curve fitting).

The Capacitance, and gate resistance were derived from an LCR meter. C_{ds} was extracted from an AC measurement of C_{oss} [45] C_{gd} , was extracted from an AC

measurement of C_{rss} [45] and C_{gs} was extracted from an AC measurement of C_{iss} [45] from which the relation $C_{gs} = C_{iss} - C_{rss}$ was used to derive C_{gs} [45]. Due to the availability of a datasheet [38] and the same device being modelled in [34], the capacitance parameters from the datasheet and the work done in [34] were used. The parameters were then optimized using the optimization toolbox in MATLAB making use of the FMINCON optimization function [46].

Parameter	Description	Caliberation details	Values	Unit
Kp0	Transconductance factor	DC transfer characteristic; slope of graph; and optimization with DC output characteristic (room temperature) at different Vgs	1.18	A/ V²
VT0	Zero- bias threshold Voltage	DC transfer characteristic; intercept of graph	3.3	v
THETA1	Transverse electric field factor	Optimized from DC Output characteristics (room temperature) curve at different Vgs	0.028	V ⁴
THETA2	Parallel electric field factor	Optimized from DC Output characteristics (room temperature) curve	0.019	V ⁴
LAMBDA	Channel Length Modulation	DC output characteristic curve at low Vgs (10V) and optimization with DC output characteristic (room temperature) at different Vgs	0.05	V ¹
KF	Non-uniform channel doping factor	optimization with DC output characteristic (room temperature) at different Vgs	0.75	
RAJ10	RAJ1 drain resistance parameter at T0	optimization with DC output characteristic (room temperature) at different Vgs	0.254	a
RAJ20	RAJ2 drain resistance parameter at T0	optimization with DC output characteristic (room temperature) at different Vgs	0.339	α
REP10	REP1 at TO	optimization with DC output characteristic (room temperature) at different Vgs	0.011	α
V1	Drain resistance parameter	optimization with DC output characteristic (room temperature) at different Vgs	12.99	۷
V1	Drain resistance parameter	optimization with DC output characteristic (room temperature) at different Vgs	0.0606	۷
П	Drain resistance coefficient	optimization with DC output characteristic (room temperature) at different Vgs	2.7034	
CGD0	Zero bias gate-to-drain capacitance	Datasheet [38] and calibration of same device in [34]	0.6E-9	ш
CGDMIN	Minimum gate-to-drain reversed biased capacitance	Datasheet [38] and calibration of same device in [34]	0.01E-9	Ł
Vgd*	Gate-to-drain capacitance parameter	Datasheet [38] and calibration of same device in [34]	2.0	٧
CDS0	Zero bias drain to source parameter	Datasheet [38] and calibration of same device in [34]	2E-9	Ŀ
CDSMIN	Minimum gate-to-drain reverse biased capacitance	Datasheet [38] and calibration of same device in [34]	0.06E-9	Ľ
Vds*	Drain-to-source capacitance parameter	Datasheet [38] and calibration of same device in [34]	10	٧
CGS	Gate-to-source capacitance	Datasheet [38] and calibration of same device in [34]	1.05E-9	F
am	Kp0 temperature parameter	Best fit of transconductance factor equation at different temperatures	1.007	
bm	Kp0 temperature parameter	Best fit of transconductance factor equation at different temperatures	0.9720	
cm	Kp0 temperature parameter	Best fit of transconductance factor equation at different temperatures	1.007	
dm	Kp0 temperature parameter	Best fit of transconductance factor equation at different temperatures	0.9482	
aTH	VT0 temperature parameter	Best fit of threshold voltage equation at different temperatures	0.004	K ⁻¹
ЬТН	VT0 temperature parameter	Best fit of threshold voltage equation at different temperatures	0.87	٧
r0	REP1 temperature coefficient	optimization with DC output characteristic (at higher temperatures) at different Vgs	2.42	
rl	RAJ1 temperature coefficient	optimization with DC output characteristic (at higher temperatures) at different Vgs	0.94	
r2	RAJ2 temperature coefficient	optimization with DC output characteristic (at higher temperatures) at different Vgs	0.55	
alpha_i	REP1 RAJ1 RAJ2 high temperature coefficient	optimization with DC output characteristic (at higher temperatures) at different Vgs	0.1661	

Table.3. 3: SiC Power MOSFET 1200- 36A parameter list table

3.3.4 MOSFET Model DC Validation

The DC characteristics of the MOSFET are the output (Drain-source current I_{ds} vs V_{ds}) and transfer (Drain-source current Idsvs Gate-source Voltage V_{gs}) characteristics. The test circuit used to extract the DC characteristics is shown in Fig.3. 3.



Fig.3. 3: Steady state DC circuit for Output and DC Characteristics

The curve-tracer (a high power curve tracer with high resolution voltage and current measurements of 50µV and 1pA respectively; see appendix A.1 for additional information) used for experimental DC results enables users to perform voltage sweeps across the terminals of the MOSFET and record the values of drain current for different voltages for each sweep. In order to perform measurement at temperatures other than room temperature, the SiC MOSFET being characterized was kept on a hotplate which has an adjustable temperature. The temperature is adjusted on the hotplate to the required temperature and then the output and transfer measurements are repeated on the curve tracer to extract the output and transfer characteristics in a similar manner to how the room temperature measurements were conducted.



Fig.3. 4: Output Characteristics (at room temperature 27°C) for different Vgs from 10V to 20V in steps of 2V. Solid lines represent model results while symbols refer to measured results

The model's DC result was calculated using MATLAB [46]. This be done because the simulator [18] used in this work has poor handling capability for parametric DC simulation of VHDL-AMS models which could not be addressed after numerous consultation with the support and software design team of [18] (who are aware of this issue and are proposing changes in upcoming versions of the ANSYS SIMPLORER software). The ANSYS SIMPLORER software is however able to simulate the transient characteristics of the model and was used for the transient simulation of the models generated in this work. The output characteristics at room temperature are shown in Fig.3. 4 for *Vgs* from to 20V. As expected, we see the increase with drain current with increase in *Vgs*. A rapid increase is observed in drain current in the linear region and

then a decrease in the rise of drain current as the device enters the saturation region at large *Vds* values. The model's drain current result show good fitting with the experimental results across the range of values displayed (see Appendix A.1 for additional information). The output characteristics at different temperatures (*Vgs* = 20V) are shown in Fig.3. 5. At higher temperatures, the resistance of the drain region increases, leading to lower value of current flowing through the drain region. This can be observed in Fig.3. 5 with the drain current at 200°C lower than the drain current at room temperature (27 °C) throughout the whole *Vds* range. It was important to note that as with many SiC power devices, most of the external drain source voltage is dropped on the drain region resistance resulting in a much lower amount of voltage across the internal drain source region (between d1 and s1 in in Fig.3. 2) of the MOSFET . In Fig.3. 5, the model produced closer results to the experimental results at increased *Vgs* values.

The transfer characteristics of the MOSFET were also measured and simulated. In collecting experimental results for the transfer characteristics, *Vds* was fixed at 10V and the measured drain current values recorded for each *Vgs* value were extracted from the output characteristic curve. Drain current values were not experimentally collected at low *Vgs* values (less than 10V) in the output characteristic but with good matching between the model and experimental values at higher *Vgs* values, and knowledge that no drain current exists below threshold voltage, the drain current values at low *Vgs* values were interpolated. The experimental/interpolated and simulation result are shown in Fig.3. 6. The model show good matching with experimental/interpolated results.

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Fig.3. 5: Output characteristics (at 200°C) for different Vgs from 10V to 20V in steps of 2V. Solid lines represent model results while symbols refer to measured results



Fig.3. 6: Transfer Characteristics of the MOSFET. Vds = 10V.

3.3.5 Capabilities of the model in relation to multichip model development

Power Electronics applications are transient (time- domain applications). Thus, it was important to check the usability of the Power MOSFET model in transient applications. A double pulse test set-up was used to perform this function. The test setup used is shown in Fig.3.7. The test conditions are Vds = 500V; Vgs = 18V (ON) and -6V (OFF); Lstray = 200nH; gate signal rise time and fall time of 100ns [34]. First pulse ON time of 99µs and second pulse after 20µs [34].

The turn off results are shown in Fig.3. 8 and show that the model is capable or predicting the drain current and drain source voltage values. The drain current shows

good matching and the oscillation in drain source voltage is comparable to that of the experimental results data extracted from [34].



Fig.3. 7: Double pulse test circuit.

The turn ON results of the double pulse test are shown in Fig 3. 9. The model 's drainsource voltage and drain-source current value overshoot show good matching with the experimental results extracted from [34].



Fig.3. 8: Double pulse test waveforms at turn off (a), Drain-source current (b) Drain-source voltage. Solid lines represent model results while dashed lines refer to experimental data from



Fig.3. 9: Double pulse test waveforms at turn off (a) Drain-source current (b) Drain source voltage(Fig 3.9(a)), Uneven chip inductance values (Fig 3.9(b) and (c)) and a zoom in of Fig 3.9(b,c) at turn-off (Fig 3.9(d)).

3.4 CONCLUSION

In this chapter, the model used to describe the electrical characteristics of the chip layer used in the multilayer power assembly was explained. The blocking and switching performance advantages of using SiC over Si for fabricating power devices were highlighted and the advantages were related to physical properties of SiC. A detailed description was also given of the type of semiconductor chip modelled in this project- the power MOSFET. A number of important physical phenomena due to the structure of the SiC power MOSFET which significantly affect the output and transient characteristics of the SiC power MOSFET were also discussed.

A review of power MOSFET models with different modelling methodologies was conducted to determine which of the model methodologies was best suitable to use in this project. The methodology judged to provide the best compromise between accuracy, computational effort and use in multichip simulations was used to create a compact SIC power MOSFET model focusing on the main behavioural features for nominal performance of the SiC MOSFET.

The created SiC power MOSFET model shows good matching with the experimental transfer and output current- voltage characteristic curves. The model also shows good matching with the current and voltage extracted experimental data in transient simulation. While the electrical model methodology used in this chapter is used in detailed electro-thermal simulations (and compared to other reviewed models in this chapter presents a physical model which provides a good balance between computational speed and accuracy), its use in parametric electro-thermo-mechanical coupled simulation could be limited because of the fast speed requirement typically required in parametric analysis.

In this chapter, the chip temperature was kept fixed during each simulation. In reality, the operation of power devices produces power losses which results in changes in operation temperature. This is discussed in full detail in the next chapter.

CHAPTER 4- COUPLED FUNCTIONAL/STRUCTURAL ELECTROTHERMAL MODELLING (THERMAL ASPECT OF MODELLING METHODOLOGY)

4.1 INTRODUCTION

This chapter describes the thermal model developed in this project. The thermal model represents the package of power semiconductor device which could be as simple as a single layer substrate package or as complex as a multichip power module package. The thermal model input is the heat loss (power loss) from the electrical model (see Chapter 3) and the main output from the thermal model is temperature for all regions inside the package (i.e. the temperature value of the semiconductor devices(s) and other components in the package). The temperature results allow power electronic engineers to monitor all regions in the power device package for safe mode of operation (monitor potential high temperature gradient regions and ensure they do not exceed maximum operating temperature). The temperature results are also used to modify the temperature dependent parameters in the electrical model and are used as input into the thermo-mechanical model (see chapter 5). In this chapter, we review existing thermal models and describe the methodology used in designing the thermal model created in this project. A novel scheme for reducing the computational effort for simulating numerical thermal models was also discussed in this chapter. The model is validated on the basis of steady state and transient simulations.

4.2 HEAT EQUATION

The flow of heat (leading to increase/decrease of temperature) in power semiconductor devices occurs primarily due to conduction with convection happening at the geometrical boundaries of the device [47]. Conduction in power electronic devices is governed by the heat equation. The heat equation for three dimensional (3D) structures is given as

$$\rho. \operatorname{Cs} \dot{T}(\vec{X}, t) = \lambda \tau h \left(\frac{\partial T^2(\vec{X}, t)}{\partial x^2} + \frac{\partial T^2(\vec{X}, t)}{\partial y^2} + \frac{\partial T^2(\vec{X}, t)}{\partial z^2} \right) + H(\vec{X}, t)$$

$$(4.1)$$

Here, T and H are both continuous functions of position (\vec{X} indicates X,Y,Z spacial resolution) and time t. T represents the temperature , \dot{T} represents the first derivative of temperature with respect to time while H represents the heat-generation rate (the power loss from the power semiconductor devices) ; ρ , Cs and $\lambda \tau h$ represent the material density, specific heat and thermal conductivity parameters respectively which are assumed constant and independent of temperature for the temperature range used in this project [48]. The Temperature (T) value is what is solved for in (4. 1). The objective of thermal models for power electronic devices is to solve (4. 1) efficiently across the device based on the application need. In choosing the thermal modelling methodology to use in building the thermal model, it was important to review existing models in literature. This is discussed in the next section.

4.3 REVIEW OF THERMAL MODELLING METHODOLOGIES

Three major solution methods are used in solving (4. 1) for power semiconductor devices. They are

- (a) Analytical solution
- (b) Thermal networks
- (c) Numerical solution

Analytical solutions involve the use of functions to approximate the heat equation on a geometry based on the boundary and initial conditions. The relationship in (4. 1) is a partial differential equation (PDE) and thus, standard analytical methods for solving PDEs such as separation of variables, use of green functions etc. will also be able to solve the heat equation. The resulting approximate equation is then used to determine the temperature value at different points in the structure. The limitation however, is that these methods are only useful in solving structures with simple geometry. Power devices have relatively complex geometry which can be non-trivial to solve using this method. Hence, analytical solution methods were not chosen in this project as the method to solve the heat equation.

Thermal networks involve the use of analogous electrical circuits to approximate the conduction through a geometry [47-49]. Two major types of thermal networks exist-the Foster and Cauer network.

The Foster network is derived from a thermal transient curve. The thermal transient curve is derived from a thermal response measurement of the power device. Through curve fitting, thermal resistance (Rth) and thermal capacitance (Cth) values are derived for all the layers in a power device. The advantage of this approach is that the network is relatively easy to derive and can be easily implemented in circuit

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simulators. However, it is not possible to derive temperature maps (also known as thermal maps) across the different layers in device structure using this approach.

Unlike the Foster network that is not physics based, the Cauer network is physics based (i.e. its Rth and Cth values are calculated from thermal and geometrical properties for each layer in the structure[47]). The Cauer network like the Foster network is also easy to implement in circuit simulators. However, like the Foster network approach, it is not possible to get temperature maps from this approach. The need to be able to easily extract temperature maps is vital to our modelling methodology thus thermal networks could not be used in designing the thermal model in this project. Due to the limitations of the analytical and thermal network solutions to our multidomain modelling methodology, it was important to review numerical solutions for the heat equation.

Numerical solutions produce algebraic equations based on a discretization method used as approximation to the exact solution. All numerical solution methods are capable of producing temperature maps with ease. Therefore, other criteria were used to select the solution method to use such as *speed of the numerical solution*, *ease of implementation* and *ease of coupling with other domains*. Three numerical solution methods were reviewed- Finite Element Method (FEM), Finite Volume Method (FVM) and the Finite Difference Method (FDM). A summary of all the reviewed models is given in Table.4.1.

The field of thermal (and electro-thermal) modelling continues to be an acitive research field in power electronics with different contributions to take the thermal problem in power electronic applications. Recent contributions are based on improvements to the methods presented above. To evaluate the state of the art, a number of these contributions were reviewed.

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Table.4. 1: Comparison of published Thermal models based on modelling methodology

First Arthur	Model Level	Contributions	Advantage to modelling	Disadvantage to modelling
			methodology	methodology
Shaeri	Exact solution	Use of analytical	accurate	Unusable for
[50]	(analytical)	functions to		complex
		solve the heat		geometries such
		equation		as power
				modules
Nance	Thermal	Use of Rth and	Fast simulation	Inability to
[47]	network (Foster)	Cth values to	time.	generate
		depict		temperature
		impedance		maps
		along layers in		
		the power		
		device		
	Thermal	Use of Rth and	Accurate	Inability to
[51]	network (Cauer)	Cth values to	junction	generate
		depict	temperature	temperature
		Impedance	prediction,	maps
		the new or	Fact simulation	
		dovico	time	
		uevice	time.	
Mouawad	Numerical	Use of elements	Accurate, easy	Computationally
[52]	solution (FFM)	to discretise the	to generate	expensive:
[02]		heat equation	temperature	Inability to
			maps	couple with
			- 1	electrical and
				mechanical
				domains in real-
				time coupled
				multidomain
				simulation
Olanrewaju	Numerical	Use of nodes to	Easy to	Accuracy(with
[53]	solution (FDM)	discretise the	generate	respect to other
		heat equation	temperature	numerical
			maps	solution
				methods) is low
			Easy to couple	
			to other	
			domain	
Chapra	Numerical	Use of volume	Easy to	Computationally
[54]	solution (FVM)	to discretise the	generate	expensive
		heat equation	temperature	
		•	1 ma a m c	
			maps	

Table.4. 1: Comparison of published Thermal models based on modelling methodology (continued)

First Arthur	Model Level	Contributions	Advantage to modelling methodology	Disadvantage to modelling methodology
Boteler[55]	Thermal Network	Discretized 3D thermal model using resistance network	Fast to solve	Coupling with electrical domain not shown
Codecasa[49]	Compact Thermal Network (derived by MOR technique)	Nonlinear thermal parameters can be handled efficiently	Fast simulation time compared to other MOR CTN thermal models	Use of FEM to derived CTN parameters is not compatible with methodology of this project
Falco[56]	Numerical	Iterative scheme implemented for implementation with compact electrical model	Coupling with electrical model possible	Involves the use of FEAM which is not compatible with the methodology of this project and is computationally expensive with for the target application of the project methodology

Boteler [55] presents a numerical-analytical thermal model. The model is discretized and using a 3D thermal network ensuring that each node is connected to surrounding nodes using thermal resistance coefficients. The temperatures at each node are calculated using an energy balance of the resistances around the node similar to Kirchhoff's first law in electronics circuit theory. This approach has been shown in [57] to reduce computation time by 100X while temperature values are within 5°C of a similar model in FEA. With respect to the aim of this PhD project, the major downside is that (as at the time of the publication of this thesis,) coupling with electrical domain has not been shown.

Codecasa [49] presents a nonlinear compact thermal network (CTN) model for circuit simulation of power devices. The components of the CTN are extracted from FEM analysis using a model order reduction (MOR) technique. Unlike in other MOR CTN models such as [9] which are limited to linear systems (thermal parameters assumed to be temperature insensitive), the MOR technique is able to efficiently handle nonlinear thermal parameters in shorter simulation time than conventional MOR derived CTNs. This method provides accurate results but includes the use of FEM in calculating the parameters of the thermal network that is not compatible, which could not be included in this PhD project methodology as the methodology is intended for circuit simulation environments.

Falco [56] presents a numerical (FEM) thermal model with capability of coupling with a compact electrical model though an interactive scheme in MATLAB. The capability of this approach to analyse a power converter was shown. However, the approach

Involves the use of FEM which needs to be done outside a circuit simulation environment and is computationally expensive to be used in the methodology proposed in this PhD project.

The FEM approximates a PDE (such as the heat equation in (4. 1)) by using approximation functions based on the element used to discretize the analysed structure. The approximation functions are weighted and summed to approximate the PDE with minimal error. The flexibility and rigorous mathematics behind this solution technique produces accurate results- the ability to use elements of different complexity makes the FEM approach flexible for solving PDEs on a wide range of structure shapes and wide range of boundary conditions. Element size can be reduced (refined) around regions where more accuracy is needed easily leading to very accurate solutions.

The limitations of the FEM in respect to this project is that the computational cost is too high for the proposed modelling methodology to be viable due to the large amount of equations that need to be solved to get accurate results. Currently available simulation platforms do not provide the ability to do real- time coupled FEM thermal and electrical simulations on the same platform (There are approaches available were FEM thermal models are coupled with SPICE electrical models but that involves the use of an FEM platform and a SPICE platform such as [49, 56]). Although, FEM is not used in the proposed methodology of this project, in this project, simulations were made with FEM to validate the VHDL-AMS models built for thermal and mechanical simulations.

The Finite difference Method (FDM) solves (4. 1) by using an abbreviation of the Taylor series to approximate the derivatives in (4. 1). The heat equation for 3D parallelepipeds [48] is shown in (4. 2).

$$\rho C_{s} \frac{\partial T_{i,j,k}}{\partial t} = \lambda_{Th} \left(\frac{T_{i+1,j,k} - 2T_{i,j,k} + T_{i-1,j,k}}{\Delta x^{2}} + \frac{T_{i,j+1,k} - 2T_{i,j,k} + T_{i,j-1,k}}{\Delta y^{2}} + \frac{T_{i,j,k+1} - 2T_{i,j,k} + T_{i,j,k-1}}{\Delta y^{2}} \right) + H_{i,j,k}$$

$$(4.2)$$

The Power loss $H_{i,j,k}$ (comes from the electrical model in coupled simulations) is inputted as point heat source. The heat sources in the mesh are placed in the exact i, j, k position in the geometry where the power devices are located ensuring the simulation is as realistic as possible.



Fig.4. 1: Finite difference (a), Finite volume (b), Finite element

(Tetrahedral) (c) mesh approach



Fig.4. 2: 3D geometry discretized for the finite difference algorithm [48]

There are several methods (schemes) of writing the FDM approximation equation such as Crank- Nicolson scheme (an implicit scheme) where future terms are used (see [54, 58] for more information). However, the scheme in (4. 2) is called the explicit finite different scheme. For numerical stability of the scheme, it is important to have a maximum time step size that fulfills the condition

$$\Delta t_{max} < \frac{\rho. \operatorname{Cs}}{\lambda \tau h} \left(\frac{\Delta x^2 \,\Delta y^2 \,\Delta z^2}{\Delta x^2 + \Delta y^2 + \Delta z^2} \right) \tag{4.3} [59]$$

FDM is relatively easy to implement compared to FEM and FVM. It is very easy to couple with other domains. It can generate accurate results for a reasonable range of geometry dimensions and boundary conditions. However, it struggles with geometries other than parallolepids (rectangle and square shapes) and to remain computationally efficient, it must be modified to handle structures that comprise of different materials and mesh structures with different mesh step sizes [60].

The Finite Volume Method (FVM) is the third method of numerical solution that was reviewed. While the FDM calculates the value of a dependent variable at a node by using the value of the dependent variable at surrounding nodes, the FVM also known as control volume method or volume integral approach) approximates a PDE by using a volume around a point [54] (see Fig.4. 1b). FVM is relatively easy to implement compared to FEM, can handle structures with different materials and different mesh stepsize with relative ease compared to the FDM approach. However, like the FDM approach, the FVM approach also struggles in handling irregular structures. With respect to our modelling methodology, the number of equations that would be generated to solve a multilayer assembly such as a power module will exceed the limit of the number of solvable equations per simulation cycle in most commercial circuit simulators.

After reviewing the thermal methodologies above, the FDM method was chosen mainly due to the low computational effort required and its ability to be easily used in coupled multidomain simulation. The scheme was modified in other to handle its

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drawback with respect to the thermal analysis of multilayer structures. The drawbacks and solution are discussed in detail in the next section.

4.4 Modified Finite Difference Method for solving Heat equation

FDM approach has been briefly explained in the previous section. The equations presented in the earlier section for the FDM ((4. 2) and (4.3)) are based on the constant mesh step approach. This means the Δx , Δy and Δz values are fixed at the beginning of the simulation and are equal throughout the X-axis, Y- axis and Z- axis for a 3D structure.

4.4.1 Constant mesh step size

In a constant step mesh FDM approach, the values of Δx , Δy and Δz are calculated as shown in Eqn.(4. 4) below

$$\Delta x = \frac{W}{nx-1} \quad \Delta y = \frac{H}{ny-1} \quad \Delta z = \frac{D}{nz-1}$$
 (4.4)

here *W*, *H*, *D* are the width, height and depth of the structure and nx, ny, nz are the number of nodes (points) in the X axis, Y axis and Z axis. In the previous section, it was stated that FDM as presented in (4. 2) will need to be modified to handle structures with multiple materials and different stepsize. Power assembly structures comprise of multiple materials and different thickness values which vary over a wide range (for example the baseplate thickness is far higher than the thickness of the solder layer). Using a constant step mesh would require Δy value (see Fig.4. 2 for the X Y Z axis configuration) to be based on that of the layer with the smallest thickness. This will lead to large amount of unnecessary mesh steps in the layers with larger thickness therefore increasing computational cost with little increased benefit in accuracy. Secondly, In power assembly structures, there are regions of higher interest

to power electronic designers (e.g. regions with high temperature gradient or high power gradient) and regions which may not be of much interest to power electronic designers (e.g. low temperature gradient regions). Attempting to satisfy the requirement for high resolution using the constant step mesh will lead to a similar computational cost issue- all other parts of the module structure (including regions of low interest to power designer)will have to be given high resolution (small value of nx, ny, nz) meaning more number of nodes in the mesh. This would mean increased accuracy of results but there will be a lot of unnecessary added accuracy in regions of low interest with high computational cost. The problem of resolution and compromises between accuracy and computational efficiency in FDM schemes could be improved by using non-constant step sizes for nx, ny, nz across the X axis, Y-axis and Z-axis respectively[61-63]. In this project, the non-constant mesh step (manual moving of step-sizes) and moving mesh (automatic moving of step-sizes) were implemented to solve the heat equation.

4.4.2 Non-constant step mesh size algorithm

The structure of a non-constant mesh step in use to solve a FDM problem is shown in Fig.4. 3(a). The FDM approach explained earlier is still used by the non-constant mesh step. The main difference here, is that the stepsize values are not the same along the axes. The heat equation for a 3D non-constant step mesh based on the X-Y-Z convention in Fig.4. 3(b) is shown in [63]).

$$\begin{split} \rho \ C_s \frac{\partial T_{i,j,k}}{\partial t} \\ = \lambda_{Th} \begin{pmatrix} -2T_P \left(\frac{1}{h_1 h_2} + \frac{1}{h_3 h_4} + \frac{1}{h^2}\right) + 2T_N \left(\frac{1}{h_3 (h_3 + h_4)}\right) &+ 2T_W \left(\frac{1}{h_2 (h_1 + h_2)}\right) \\ &+ 2T_S \left(\frac{1}{h_4 (h_3 + h_4)}\right) + 2T_E \left(\frac{1}{h_1 (h_1 + h_2)}\right) + \frac{T_A}{h^2} + \frac{T_B}{h^2} + H_{i,j,k} \end{pmatrix} \end{split}$$

(4.5) [63]

The green region in Fig.4. 3(a) represents the location of the power device die (i.e. chip). The chip region is indicated as point heat sources on the nodes around that region (i.e. on "power" nodes that are in the region of the power devices in the mesh structure, $H_{i,j,k}$ will have a non-zero value which will be dependent on the power loss from the devices; for other "non-power "nodes, their $H_{i,j,k}$ value will be zero). The dimension of the nodes in the chip region is kept fixed because it is important to keep the geometry of the chip region intact. It is also important to observe that since the stepsize in the axes are not constant one cannot use the convention as used in constant mesh (4. 2) but rather use h_1, h_2, h_3 and h_4 as shown in Fig.4. 3(b) for difference between nodes. (e.g. h_1 is the difference between the next node to the east of the current node and the node under analysis)



Fig.4. 3: (a) volume meshing using a non-constant mesh step. The convention used is shown in (b).

One can observe from Fig.4. 3(a) that the region around the power devices section (power devices are in the area coloured green in Fig.4. 3(a)) has smaller mesh step sizes (finer mesh) compared to the regions close to the border of the structure (coarse mesh). Thus, on simulation, it is expected to observe more accurate results around the chip region than at the boundary region. Multichip SiC devices usually have highly localized heat generation regions with high temperature gradients [53] therefore, by

manually adjusting the stepsize to be fine around such high temperature gradient regions and coarse around the border regions, the temperature results will show more accuracy around the power device regions and less accuracy around the boundary regions for the same simulation speed[53]. For power electronic designers, this is a compromise that is acceptable. The total number of points generated by the mesh using this approach does not change. Thus, from a simulator point of view, the simulator is solving the same number of equations per simulation cycle. This approach gives better resolution around important areas in the structure while trading off the accuracy in non-important (with respect to importance of having accurate results) parts of the structure under analysis. The non-constant mesh step was used in the beginning stages of this project [53] as a building block for the moving mesh algorithm. Once the moving mesh algorithm was implemented, the temperature map comparisons were made between constant step mesh, moving mesh step and FEA/ experimental results.

4.4.3 Moving mesh step algorithm

The mesh adjustment in the non-constant mesh step approach is implemented manually before the simulation cycle. Once the simulation starts, the stepsize cannot be modified until the simulation ends. However, there are some applications where the region(s) requiring high degree of accuracy changes at different points during the operation cycle. For example, in a power module, with heat flow from the chip down to the baseplate and heatsink, it is possible that the hottest regions and regions of high temperature gradient change from one part of the module to another in the course of the operation of the power module. It would be of great value therefore to have a mechanism in which the regions of fine mesh in the structure under analysis are always at the regions of "importance" at every time step in the simulation cycle. The moving mesh approach is designed to perform this automatic "real time remeshing" to meet the resolution needs at various regions in the structure under analysis as the simulation advances. This approach is similar to adaptive meshing techniques [64] (adaptive re-meshing) in that it also has a technique of identifying regions that require higher resolution. However, the moving mesh method does not superimpose finer grids on regions that need higher resolution as is done in adaptive meshing.

$$X = \frac{Lenght}{\int_{0}^{x_{max}} \left[\left| \frac{\partial T_{x}}{\partial x} \right| + K \right]^{-mx} dx} \cdot \int_{0}^{x} \left[\left| \frac{\partial T_{x}}{\partial x} \right| + K \right]^{-mx} dx$$

$$(4. 6) [60]$$

$$Z = \frac{Width}{\int_0^{z_max} \left[\left| \frac{\partial T_z}{\partial z} \right| + K \right]^{-mz} dz} \cdot \int_0^x \left[\left| \frac{\partial T_z}{\partial z} \right| + K \right]^{-mz} dz$$

(Here, X, Z represent nodes; mx and mz determine mesh coarseness; K is to prevent convergence errors. x_max and z_max are the total number of nodes in the X and Z axis respectively).

$$X = \Delta x(x-1) + m_x(T_{x+1} - T_{x-1})$$

$$Z = \Delta z(z-1) + m_z(T_{z+1} - T_{z-1})$$

$$m_x \le \frac{\Delta x_{max}}{(T_{x+1} - T_{x-1})_{max}} \tag{4.7}$$

$$m_z \le \frac{\Delta z_{max}}{(T_{z+1} - T_{z-1})_{max}}$$

The moving mesh algorithm simply rearranges the mesh lines in the mesh towards the regions where higher resolution is needed at the expense of other regions. This means that the total number of nodes remains the same thus the simulator still has to solve the same number of equations leading to increase computational savings compared to adaptive meshing.

The moving mesh algorithm like the non-constant mesh step solves the heat equation for a 3D structure using (4.5)). However, because the dimensions of the nodes change during simulation, the h_1 , h_2 , h_3 and h_4 values in (4.5)) will change at every time step. The main equations guiding the algorithm are shown in (4.6)[60]. Initially a dense mesh is applied on the regions of power dissipation and heat generation. The nodes in the vertical (*Y*) direction and the nodes where the power dissipation is applied to the chip region are kept fixed (as done in the non-constant step mesh algorithm). While the stepsize in the *X* and *Z* axes move during simulation, the stepsize in the Y axis is constant during simulation because the heat sources are mounted at the top of the Y axis of the structure (see Fig.4. 3a). The algorithm automatically moves the location of the nodes in the mesh (i.e. it modifies the mesh step sizes) in real-time during transient simulation, based on the temperature gradient between adjacent nodes in the *X* and *Z* axes. The algorithm is designed to measure the temperature difference across the nodes in the mesh, find the regions where the most extreme temperature differences are and make the mesh lines closer around those regions thus producing greater accuracy in those regions. In line with the design goal of obtaining a compromise between accuracy and computational efficiency, the algorithm trades off accuracy in other regions but this is a reasonable compromise as the regions of high temperature gradient are of most importance to design engineers.

Implementing (4. 6) with the proposed thermal model (4. 5) in a circuit simulator environment [18], it was observed that the simulation time of coupled electrothermal models increased significantly. On further observation, it was observed that the absolute (i.e. | |), exponential (mx and mz) and integration ($\int dx$, $\int dz$) terms were responsible for more than 75% of the simulation time (taking more computational effort to solve than even the finite difference equations (4.5)). If there was to be any benefit from the moving mesh algorithm, a simpler derivation for the X and Zdimension values that was simpler for the simulator to solve while remaining effective enough the adjust the meshes around based on temperature gradient was needed. A more efficient solution is seen in (4. 7) where m_x and m_z are not exponential terms but linear terms. Δx and Δz are calculated using the same formula as (4. 4). The m_x and m_Z terms still determine mesh movement- the greater their values, the tighter the mesh gets around regions of large temperature gradient. The minimum value that m_x and m_z can be is zero (in which case it will generate a constant step mesh i.e. the mesh lines will not move if in the X axis if m_x zero and the mesh lines will not move in the Z axis if m_Z is zero). The terms x and z remain designated as node but the K, exponential, abs and integration terms in (4. 6) are not needed. The $(T_{x+1} - T_{x-1})_{max}$ term implies the maximum temperature difference between the node after and the node before a given node in *X* axis. while the $(T_{z+1} - T_{z-1})_{max}$ term implies the maximum temperature difference between the node after and the node before a given x node .To get each T_{x+1} or T_{x-1} term, one would need to add all the temperatures in the Z axis along that x node (vice versa for T_{z+1} or T_{z-1}) i.e. $T_{x+1} = T_{x+1,y_{max},z1} + T_{x+1,y_{max},z2} + T_{x+1,y_{max},z3} \dots T_{x+1,y_{max},z_{-max}}$ and $T_{x-1} = T_{x-1,y_{max},z1} + T_{x-1,y_{max},z2} + T_{x-1,y_{max},z3} \dots T_{x-1,y_{max},z_{-max}}$.

Thus, for each node, if the total temperature of the node after a given x node is greater than the total temperature of the node before it, that particular x node will shift towards the node after it and if the total temperature at the node after a particular x node is less than the total temperature of the node before it, the node will shift towards the node before it (the similar process works for any z node). How much each node will move is still determined by the m_x and m_z terms. For this method to work, the restriction in in (4. 7) must be observed. Also, Δx_{max} and Δz_{max} used in the derivation of mx and mz must not be greater than Δx and Δz derived from (4. 4). It may not possible to know the value of $(T_{x+1} - T_{x-1})_{max}$ and $(T_{z+1} - T_{z-1})_{max}$ beforehand so initially we use m_x and m_z value of zero (i.e. the initial mesh discretization inputted by the user). After the initial simulation once the $(T_{x+1} - T_{x-1})_{max}$ and $(T_{z+1} - T_{z-1})_{max}$ values are known, they can then be used to derive optimum m_x and m_z values.

4.4.3.1 Accuracy of the moving mesh algorithm

The accuracy (error) of this approach is similar to that of the constant mesh step algorithm. In fact, if one uses $h_1 = h_2$ and $h_3 = h_4$ in (4. 5), then (4. 5) will simplify to (4. 2). Thus, just like the error in the constant step mesh is of order $O(h^2)$, in this case h is stepsize, the moving mesh algorithm also has a similar second order accuracy of $O(h^2)$. Given that the non-constant mesh step and moving mesh have different step sizes on the same axis, the stepsize (h) value, the largest stepsize in each axis is used in determining the $O(h^2)$ value. The maximum error will be at the regions with larger stepsize and the minimum error will be at regions with smaller stepsize which is exactly what the algorithm was designed to achieve.

4.4.3.2 Convergence of the moving mesh algorithm

As explained earlier, convergence simply means that an approximation to a PDE approaches the true solution as the time stepsize and spacial stepsize approach zero $\Delta t \rightarrow 0$; $h \rightarrow 0$. It has been shown that an approximation to a PDE will converge if the approximation is **consistent and stable** [54]. Thus the finite difference approximation in (4. 5) was checked for consistency and stability. Consistency means that as Δt , Δx , Δy , $\Delta z \rightarrow 0$ then the finite difference approximation approaches the true solution. For the approximation in (4. 5), our derivation shows that as Δt , Δx , Δy , $\Delta z \rightarrow 0$ the difference between the true solution and the scheme (4. 5) approaches zero. This implies that our finite difference algorithm is unconditionally consistent.

Stability implies that any errors (perturbations) in the course of the simulation (computation) are not amplified but remain bounded (i.e. the errors are reduced as the computation progresses) [54]. For the FDM approximation in (4. 5)), the scheme will be stable based on the condition shown in (4. 8). The time step used in simulation must be equal to or less than the value on the right hand side of (4. 8). The numerator of the right hand side of (4. 8) uses the square value of the minimum stepsize found in the mesh. The values of Δx , Δy , Δz used in (4. 8) are calculated based on the mesh of Fig.4. 3.

Given that the moving mesh algorithm is unconditionally consistent, therefore, if the conditions for stability are met, the simulation is guaranteed to converge to the true solution.

$$\Delta t_{max} \le \frac{\min(\Delta x^2, \Delta y^2, \Delta z^2)}{2\frac{\lambda \tau h}{\rho. \operatorname{Cs}}}$$
(4.8)

$$\Delta x^{2} = 0.5 h_{1} (h_{1} + h_{2}) \text{ or } 0.5 h_{2} (h_{1} + h_{2})$$

$$\Delta y^{2} = h^{2}$$

$$\Delta z^{2} = 0.5 h_{3} (h_{3} + h_{4}) \text{ or } 0.5 h_{4} (h_{3} + h_{4})$$
(4.9)

4.4.3.3 VHDL-AMS code module

As explained in Chapter 2 of this thesis, the models were written in VHDL-AMS modelling language. Unlike the electrical aspect of the methodology with relatively few equations, FDM direct implementation of the heat equation using either the constant step mesh, non-constant step mesh or moving mesh algorithm generates a large number of equations (compared to the number of equations from the electrical model) which can be very intensive and error prone if they are implemented manually. Thus, a graphic user interface (GUI) module was created in MATLAB [46]. All the user needs to do is enter physical, geometry and meshing parameters into the module. Once this has been done, the VHDL-AMS code is automatically generated in a file which can then be compiled in any simulator environment (capable of simulating VHDL-AMS models) such as SIMPLORER [18] or SABER [17].

4.5 Parameter List

The thermal model has more equations than the electrical model. However because most of the equations are either differential equations or mesh adjustment equations, the number of parameters the model requires are few- majorly material, geometry and initial/boundary condition parameters. The table below (Table.4.2) highlights a number of parameters used in the thermal model.

The use of a numerical solution in the non-constant step mesh or moving mesh thermal model eliminates the need for rigorous parameter extraction- the material and boundary condition parameters are generic and can be found from books or online resources. There is no need to conduct time-intensive parameter extraction processes. The geometry and initial condition parameters are specific to the structure being analysed and can be derived trivially. It is important to ensure that the units of the parameters is consistent in the model. (For example if using cm for dimensions then all parameters that have dimension in them must be in cm).

Table.4. 2: Thermal model parameter table

PARAMETER	DESCRIPTION	COMMENT	
Та	Ambient temperature (initial condition)	Defined by operating environment	
Width	Width of the structure under analysis (the <i>X</i> - axis dimension)	Defined by the geometry of the structure	
Height	Height of the structure under analysis (the Y- axis dimension)	Defined by the geometry of the structure	
Depth	Depth of the structure under analysis (the Z axis dimension)	Defined by the geometry of the structure	
htop	Convection coefficient for the top of the structure (boundary condition).	Very low value to reflect very low lateral heat flow	
hside	Convection coefficient for the side of the structure (boundary condition).	Very low value to reflect very low lateral heat flow	
hbot	Convection coefficient of the bottom layer of the structure (boundary condition). Usually represents the heatsink convection coefficient	The convection coefficient value for any material can be found in books/online/other resources	
nx	Number of nodes in the x axis	Defined by the user	
ny	Number of nodes in the y axis	Defined by the user	
nz	Number of nodes in the z axis	Defined by the user	
λ	Thermal conductivity	Material property based on the material	
ρ	Density	Material property based on the material	
Cs	Specific Heat capacity	Material property based on the material	
m _x	mesh coarseness in X axis	See Equation (4. 7)	
mz	mesh coarseness in Z axis	See Equation (4. 7)	

4.6 Validation / Application of Thermal methodology



4.6.1 Coupled single-layer Electro-thermal application)

Fig.4. 4: (a) Top view of smart-power integrated circuit reprinted from [65] (b) 3D view and (c) 2D side view of simplified structure of (a) used for analysis in this work.
The first step in the validation of the proposed thermal model outlined in this chapter (see section 4.3 and 4.4) was to use it in a single layer (chip level) simulation. The smart-power chip concept designed for automotive application (as a short circuit current limiter in automotive applications to ignite gas lamps[65]) and presented in [65] can be analysed as a chip level structure simulation. The smartpower chip is an integrated circuit which includes an electrical device (power MOSFET), control (logic) circuitry and temperature sensor. Of paramount importance to the designers of the smartpower chip is the monitoring of the temperature of the power MOSFET as well as the regions around the power MOSFET. The control of the circuit is not of importance to us in this project. Rather, we use the experimental results from [65] to validate the thermal model created in the project.

The test circuit is shown in Fig.4. 5. The test conditions were similar to those used in [65] (same dimensions, *Vds* of 14V and *Vgs* of 18V was used). To model the gatedrive circuit to the MOSFET, a gate pulse of applied at time= 1ms which is ON for 3ms was used. The capacitances in the electrical model were turned off [60], thus, the power loss is mainly from the drain region resistance.

Once the details of the structure and mesh dimensions are input into the GUI (see section 4.4.3.3 for information on the GUI), thermal model equations are outputted and input into the simulator where they are compiled into a simulator model. When the simulation is run, the simulator's solver solves the equations in the schematic and outputs the temperature values on each node for all time steps in the simulation. Using the results, one then plots the temperature maps at the time steps that are of interest. All results at each time step are available to users, thus, any user of the model can plot temperature maps at timepoints that are of interest to them.

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Fig.4.5: Test setup for smartpower chip test. Due to the use of VHDL-AMS modelling language, models from different domains can be "connected" like circuit components as done above between the electrical and thermal model which both have a thermal node tj. The electrical model outputs power values and receives temperature through its thermal node tj and the thermal model receives power values and outputs temperature values to the electrical node through its thermal node tj.

In order to have a comparison of accuracy and speed, between the constant mesh and moving mesh algorithms with respect to the experimental results, a mesh structure was created - both meshes use a X - Y - Z discretization of 15-4-10 respectively (600 finite difference equations to solve).

Each node (point) in the mesh has its FDM equation ((4. 2) for constant step mesh and (4. 5)) for moving mesh step FDM equation). The meshes and dimensions are shown in Fig.4. 6. (Due to the small thickness of the whole smartpower structure, the structure in can be approximated to be a single layer (copper) with a heat generation region (where the Power MOSFET is). The simulation is a coupled electro-thermal simulation. The temperature of the chip (MOSFET) region is fed back into the electrical

model to change the temperature-dependent parameters in the electrical model (Chapter 3). It is important to note that the temperature fed back to electrical model can be selected by the user to be the temperature at any node, or an average as the user desires. This application is known as a single layer fully coupled application because of the combination of electro-thermal simulation and single layer approximation. Thus, electrical and thermal results are generated from the simulation. The current vs time results are shown in Fig.4. 7 for both constant mesh Fig.4. 7(a) and moving mesh Fig.4. 7(b). The results show that the moving of the meshes in the constant mesh result does not significantly alter the current of the structure while (as is explained below) attempting to generate a more accurate thermal result.

The temperature maps at 2 different time steps (2.5ms and 3ms) in the simulation of the smartpower structure based on the test circuit in Fig.4. 5 are shown in Fig.4. 9 *and* Fig.4. 10. The thermal maps show the temperature across all regions in the top surface of the structure.



Fig.4. 6: mesh discretization of the smartpower chip



Fig.4. 7: smart power chip test result of current vs time graph for constant step mesh and moving mesh algorithm



Fig.4. 8: The movement of nodes during simulation time is shown for (a) X8- X7 and (b) Z3-Z2 stepsizes

The temperature maps for both the constant step mesh and the moving mesh at 2.5ms are shown in Fig.4. 9 and the temperature maps for the constant and moving mesh steps at the 3ms timepoint are shown in Fig.4. 10. It was observed that that the junction temperature values are similar (533K (constant step mesh) vs 541K (moving

mesh step) for 2.5ms and 599K (constant step mesh vs 592K (moving mesh step) vs at 3ms). It was also important to observe that at the point of highest temperature gradient the mesh lines in Fig.4. 9(b) and Fig.4. 10(b) become closer together. This enables the algorithm to get a reduced temperature gradient across the MOSFET unlike the constant mesh results in Fig.4. 9(a) and Fig.4. 10(a). In Fig.4. 8, the movement of the mesh is shown with respect to time for two stepsizes- the stepsize between nodes 7 and 8 on the X axis and the stepsize between nodes 3 and 2 on the Z axis (see Fig.4. 6 as a guide see the position of nodes; note that the nodes are counted from 1 starting at the bottom left of the mesh in Fig.4. 6 for both the X and Z axis). It was observed that the node x7 moves towards the right when the chip is turned ON (reducing the step between x7 and x8) because the region of high temperature gradient is towards the chip on the right side of x7. When OFF, the x7node shift back towards the left. The same occurrence is found in the step between z_2 and z3 nodes with z2 moving upwards as the region of high temperature gradient is above the initial position of the z^2 node when the chip is turned ON. In Fig.4. 8, the mesh movement can be observed to represent over 40% change (from the initial stepsize value at time = 0 ms) in the stepsize value in the direction of the temperature gradient which the device is turned ON.





Fig.4. 9: Thermal maps for the short-circuit schematic in Fig.4. 5(a); at 2.5ms with(a) Constant step mesh and (b)Moving mesh results





Fig.4. 10: Thermal maps for the short-circuit schematic in Fig.4. 5(a); at 3ms with (a) Constant step mesh and (b)Moving mesh results



Fig.4. 11: Junction temperature and sense temperature compared for the constant step mesh (a) and moving mesh (b) algorithms

A comparison of speed and accuracy of the constant step mesh, moving mesh step and experimental result is shown in Table.4. 3. The Tsense point (in Fig.4. 5, Fig.4. 6, Fig.4. 9, Fig.4. 10) is used to control the gate signal to the chip to ensure that excessive temperature thresholds are not exceeded [65]. The results in Table.4.3 show that the presented thermal models are able to get close values to the values presented in [65] for Tj values (The moving mesh result presenting a closer value than that of the constant step mesh in comparison to the experimental value of Tj at 3ms). However, the cost of increased accuracy of the Tj value is the increased simulation time of the moving mesh algorithm which is required to calculate temperature gradients and move the mesh nodes at each time point during the simulation cycle.

METHODOLOGY	ACCURACY	SIMULATION	
	Tjmax	Tsense	TIME
	(maximum	At the	(seconds)
	junction	selected	
	temperature	point	
	in the chip		
	layer)	(at time 3ms)	
	(at time		
	3ms)		
Experiment [65]	588K	-	—
Constant mesh	599K	444K	64
solution			
Moving mesh	592K	410K	95
solution $(m_x =$			
1.1E-5 and m_z =			
1.4E-5)			

Table.4. 3: Simulation speed and accuracy comparison

It is also important to know the optimum value of m_x and m_z to use in the moving mesh thermal model simulation. Fig.4. 12 shows a comparison of simulation speed and accuracy (Tjmax) values. The error in temperature is calculated based on the absolute value difference of Tjmax for each m_x and m_z value with respect to the experimental result. In Fig.4. 12a, m_z is fixed while m_x is varied and vice versa in Fig.4. 12b. An increase in accuracy (reduction in error) is observed moving from a m_x value of 2.0E-5 with a peak in accuracy around 5.0E-5. Above 5.0E-5, the accuracy reduces with increasing m_x values. The simulation time is a straight line graph increasing from the lowest to the highest m_x values. Both lines meet around the 3.0E-5 point. A similar situation can be found while varying m_z (Fig.4. 12 (b)). Thus, the optimum m_x and m_z value is value is around 3.0E-5 and 2.2E-5 respectively.



Fig.4. 12: comparison of speed and accuracy for different (a) m_x (m_z fixed at 1.4E-5) and (b) m_z (m_x fixed at 1.1E-5) values in the moving mesh algorithm

4.6.2 Power Assembly (Uncoupled multilayer thermal application)

The second validation step was to validate the described thermal model methodology on a multilayer power assembly. The details of the power assembly have been explained in Chapter 1. In this section, validation is done using FEA [66] simulation. A power assembly could represent a power module (it contains all the layers in a power module) or the building block of larger power module structures [11]. Given that FEA thermal models are not fully coupled electro-thermally, the constant mesh step and moving mesh step thermal models were not coupled to the electrical model rather, arbitrary uniform heat sources were placed on the chips in Fig.4. 13 -hence the title*uncoupled multilayer thermal application*. The geometry of the power assembly in Fig.4. 13a is symmetrical, hence it can be divided into two with one half analysed and the result will be similar in the other half. The side view of half of the power assembly is shown in Fig.4. 13b.



Fig.4. 13: Structure Power Assembly used for thermal validation. Top view (a) Side view of half of the power assembly (b)



Fig.4. 14: Test circuit for power assembly validation

The test conditions are 100W power loss input of 12s ON time and 8s OFF time. The convection coefficient for the bottom surface is 10,000 W/m²K (1 W/cm²K) with an ambient temperature of 300K. The test circuit is shown in Fig.4. 14. Heatsource_1 sends the power pulse to one chip and Heatsource_2 sends the power pulse to the second chip in the assembly (for geometrical symmetry reasons, only half of the assembly in Fig.4. 13 is being analysed). The thermal and geometrical properties for each layer are given in the table below.

Layer	Thermal Properties			Thickness	Width
	Thermal	Density	Specific	(cm)	(cm)
	Conductivity		Heat		
	(W cm ⁻¹ K ⁻¹)	(g cm ⁻³)			Х
			(Jg ⁻¹ K ⁻¹)		
					Height
					(cm)
chip (SiC)	1.6	2.3	0.7	0.05	0.8 X 0.8
solder	0.5	12.0	0.25	0.005	0.8 X 0.8
copper (top)	4.01	8.94	0.385	0.03	1.0 X 1.0
dielectric	2.85	3.26	0.82	0.064	3.0 X 3.0
(AIN)					
Copper	4.01	8.94	0.385	0.03	3.0 X 3.0
(bottom)					
Heatsink	2.3	3.26	0.74	1.03	3.0 X 3.0

Table.4. 4: Thermal and Geometrical properties of layers in the power assembly

In order to have a comparison of accuracy and speed between the constant mesh step and the moving mesh algorithms with respect to the FEA results, their respective mesh structures were created- the constant and moving mesh step algorithms both use a X - Y - Z 16–10–16 (a maximum of 2560 FDM equations to solve). The mesh and dimensions for the top layer of the constant mesh and moving mesh assembly is shown in Fig.4. 15. The mesh structure used for the FEA solution is shown in Fig.4. 16 and consist of 6932 nodes.



Fig.4. 15: Mesh for the VHDL-AMS power assembly thermal model (a) Constant mesh (b), moving mesh with node dimensions.



Fig.4. 16: FEA mesh for power assembly

The thermal maps at one time step (time= 10 seconds) on simulation of the power assembly structure based on the test circuit in Fig.4. 14 are shown in Fig.4. 17 and Fig.4. 18.

Fig.4. 17 shows the comparison between the VHDL-AMS constant/moving mesh step and the FEA simulation at the top of the chip layer. The maximum temperature in the FEA is 379K while that of the constant mesh step is 382.1K and that of the moving mesh step is 382.7K .The FEA solution has a higher temperature gradient (difference between the maximum temperature and minimum temperature) than the other two solutions which is likely due to its finer mesh. All the solutions show that the maximum temperature is at the centre of the device and the lowest temperature values are at the corner of the device. Given that the main goal of the methodology of this project is for parametric (comparative studies) with minimum computational cost, both VHDL-AMS (constant step mesh and moving mesh step) solutions are valuable as they both show the right trend (show exactly the positions of maximum and minimum temperature and give a good description of the flow of heat across the layer) of result across the chip to make fast parametric analysis possible. The maximum temperature of both VHDL-AMS solutions are within 4K of the FEA solution.

Fig.4. 18 shows the comparison between the VHDL-AMS constant/moving mesh step and the FEA simulation at the middle surface of the AiN (dielectric) layer. The maximum temperature in the FEA solution is 372K while the maximum temperature is 380.7K and 381.3K for the constant step mesh and moving mesh algorithms. Both VHDL-AMS solutions show maximum temperature to be at the region directly under the chip layer and the region in the middle having the lowest temperature. The temperature gradient in the AiN region exceeds that of the constant step mesh and moving mesh step result.

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Fig.4. 17: Chip layer Temperature comparison (a) FEA, (b) constant mesh step and (c)moving mesh algorithm



1.4 cm





Fig.4. 18: AiN Temperature comparison in (a) FEA, (b) constant step mesh (c) moving mesh step algorithms



Fig.4. 19: The movement of nodes during simulation time is shown for (a) X8-X7 and (b) Z7- Z6

In order to highlight the movement of mesh lines in the moving mesh step algorithm solution, the step between node 7 and 8 in the *X* axis and the step between node 6 and node 7 in the *Z* axis are shown in Fig.4. 19(a) and Fig.4. 19(b) respectively (see Fig.4. 15 as a guide see the position of nodes x7, x8, z6 and z7; note that the nodes are counted from 1 starting at the bottom left of the mesh in Fig.4. 15 for both the *X*

and Z axis). When the power pulse is turned on (the chip region is switched ON), x8 shifts towards the chip region on its left side because region of high temperature gradient is towards its right thus the decrease in the x8 - x7 value when ON. When OFF, a reduction in temperature gradient sends the mesh lines moving in the opposite direction. A similar occurrence is seen in the z6 and z7 nodes. Thus, when the chip is turned ON, z7 moves further downwards away towards z6 leading to a decrease in the z7 - z6 value. The opposite effect happens when the chip is turned OFF. As a percentage of the initial special step (0.2cm), we observe maximum mesh step movement of 40% for z6 - z5 and 45% for x8 - x7. Although these represent significant moves in stepsize, , because the temperature gradient on the chip layer is very low and the maximum junction temperature solution of the constant mesh solution is very close to that of the exact solution (benchmarked by the FEA solution), these mesh movements do not produce significant change in junction temperature or temperature gradient.

A comparison of speed and accuracy of the VHDL-AMS solutions and the FEA solution (using the FEA solution as a benchmark) is done in Table.4. 5. The maximum temperature at the chip layer temperature and simulation time were observed. The Tjmax values are within 4K of each other. The FEA produces the most accurate results but also has a higher simulation time than the VHDL-AMS solutions.

It is also important to know the optimum value of m_x and m_z to use in the moving mesh thermal model simulation. Fig.4. 20 shows a comparison of simulation speed and accuracy (Tjmax) values. The error in temperature is calculated based on the absolute value of the difference of Tjmax for each m_x and m_z value with respect to the result in the FEA solution. An increase in accuracy (reduction in temperature difference) is observed with decreasing m_x (and m_z) values although the

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temperature difference is very low. The simulation time reduces with increasing m_x (and m_z) values.

METHODOLOGY	ACCURACY	SIMULATION TIME
		(seconds)
	Tjmax (maximum	
	junction	
	temperature in the	
	chip layer)	
	(at time 10 s)	
FEA solution	379.3K	147
Constant mesh solution	382.1K	73
Moving mesh solution (at m_x	382.7K	86
and m_z = 7.0E-5)		

Table.4. 5 : comparison of solution methods for the power assembly

The optimum m_x and m_z point obtained from the crossover points in Fig.4. 20(a) and (b) respectively is about 7.0E-5 for both m_x and m_z . This is partly due to the symmetrical nature of the structure used in this application.





Fig.4. 20: speed and accuracy comaprison for different m_x and m_z values

4.6.3 Multichip Power Module (experimentally validated fully coupled multilayer Electro-thermal application)

The final validation step of the thermal modelling methodology was to use it in a fully coupled multilayer electro-thermal application. This section is discussed fully in the appendix.

4.7 CONCLUSION

In this chapter, the thermal aspect of the modelling methodology used in this work was described in detail. The thermal problem was explained and possible approaches to solving the thermal problem for a multilayer and multichip structure such as a power module were reviewed with their advantages and disadvantages with respect to the overall modelling methodology discussed. The Finite Different method (FDM) was explained and a number of FDM schemes currently in use were also mentioned. Contributions to the FDM scheme were explored - non constant step meshes (The non-constant mesh step and the moving mesh algorithms) designed to maximize the compromise between simulation speed and accuracy. The non-constant step mesh involves manual mesh movement which does not change during simulation while the moving mesh step algorithm involves the automatic movement of meshes during simulation in response to a particular factor which in this work was set as temperature gradient.

The thermal models built in this project were validated using with both uncoupled and coupled Electro-thermal problems using FEA and experimental results as benchmarks. In the first application example of a single layer structure, the magnitude of temperature gradient in the layer for the VHDL-AMS solutions is similar to what was obtained in the benchmark. Thus, the moving mesh solution was able to produce significant differences to the temperature result however at the cost of increased simulation time which could be justified based on the maximum chip temperature getting closer to the value of the benchmark. With multilayer structures such as the case in the second application example, the magnitude of the temperature gradient in all layers for the VHDL-AMS solutions are smaller in comparison to the benchmark. Thus, despite significant movement of mesh lines, there was no significant increase

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or decrease in temperature values in the layers and the increase in simulation time is not justified. Thus in this case, constant step mesh solution could be a better compromise to use.

In all application examples, the thermal model is able to predict the maximum temperature in each layer (within 3% of benchmarked result), the trend and location of minimum and maximum temperature in each layer at faster speed compared to FEA and experimental methods. Thus, the methodology presented in this chapter can help system designers to place chips or temperature sensors to get relevant reading or with selection of materials to use during the design of a power module assembly.

CHAPTER 5- THERMO MECHANICAL MODEL (MECHANICAL ASPECT OF MODELLING METHODOLOGY)

5.1 INTRODUCTION

The reliability of power assembly structures is highly dependent on residual stresses [67] . These stresses are generated during the operation of the power assembly due to thermal mismatch (difference in coefficient of thermal expansion) of the different layers that comprise the power assembly as the temperature rises from ambient temperature to operation temperature. The repeated temperature cycle resulting from the operation of the power module (switching of the chip layer) lead to repeated stressing on the power module which overtime lead to fatigue or failure of components in the power module [68, 69]. It is therefore important to develop a model to predict thermo-mechanical (also known as thermal stress) effects from the design stage thus enabling device designers to observe the effect of their electrical, thermal, material and geometrical designs on the mechanical domain (stress, deformation) of the power module.

Two major issues cause scepticism about thermo-mechanical simulations in the power electronics field- first, the effect of mechanical deformation on the temperature (i.e. feedback to the thermal domain from the mechanical domain) and secondly, the effect of temperature/ temperature changes on the mechanical properties of the materials that make up the different layers of the power module assembly. In this work, the first issue (feedback from mechanical domain to thermal domain) is ignored because quantifying the changes in temperature values from feedback of mechanical deformation and stress is extremely challenging for a power

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module assembly [69]. Also, the values of strain generated in power electronics applications do not cause a significant change in geometrical and material parameters used in the thermal model [70]. On the second issue, a review of [68] indicates that mechanical properties in power modules can be assumed constant between -55°C degrees and 125°C. The maximum temperature of thermal results presented in this work are less than 125°C. Thus, in this work, the mechanical properties of materials are kept constant [68, 69]. Working with this background information, a simplified thermomechanical model was designed in line with the overall modelling methodology for this project. The model takes as input the results from the thermal model (see Chapter 4 for description of the thermal model) and outputs stress values based on the temperature difference from the room temperature value, mechanical properties, mechanical equations and geometry.

5.2 HOOKE'S LAW

As with other domains (e.g. electrical, thermal), the mechanical domain is based on its fundamental set of equations (Hooke's law) which relates the stress and strain of a material. The generalized Hooke's law is given as

$$\sigma - \sigma_0 = C : (\varepsilon - \varepsilon_0 - \alpha \theta) \tag{5.1} [71]$$

Here,

$$\varepsilon = 0.5 (\nabla u - (\nabla u)^T)$$
$$\theta = T - T_{ref}$$

T (unit Kelvin) represents Temperature, T_{ref} (unit Kelvin) represents the reference (room) temperature, σ (unit Pascal) represents stress, σ_0 (unit Pascal) represents initial stress, ε (unit dimensionless) represents strain, ε_0 (unit dimensionless) represents initial strain, α (unit K⁻¹) represents coefficient of thermal expansion (CTE) and u represents displacement (unit cm). The objective of mechanical models for power electronic devices is to solve (5. 1) efficiently across the device based on the application need. In choosing the mechanical model, it was important to review existing models in literature. This is discussed in the next section.

5.3 REVIEW OF THERMO-MECHANICAL MODELLING METHODOLOGIES

There are two major methods for solving (5. 1). They are

- (a) Numerical Solution
- (b) Analytical solution

Numerical solutions produce algebraic equations based on a discretization method used as approximation to the exact solution. The most popular numerical method used in thermomechanical simulations in industry currently is the Finite Element Method (FEM). The FEM method has been discussed in Chapter 4 with respect to solving the heat equation and the same principle holds with respect to solving (5. 1). The possibility of using elements of different shapes gives the FEM method flexibility to analyse a wide range of power electronic device geometries in detail. It is also possible to capture nonlinearities in material properties of the different layers in power devices using standard FEM software packages as shown in [72, 73].

It is also possible to create customized FEM packages to handle thermo-mechanical simulation or fully coupled electro-thermo-mechanical simulations as done in [74, 75]. In [74, 75] a customized platform called *SESES* was created where the fundamental electrical, thermal and mechanical equations are solved using FEM. Typical number of elements used per analysis ranged from 10,000 to 1,000,000. The fundamental

electrical, thermal and mechanical equations were solved for each node simultaneously and adaptive meshing was used in regions where higher resolution was needed in order to keep the simulation computationally efficient.

Numerical solutions (FEM in particular) produce very accurate result. Their limitation however, is the computational cost which is too high for the proposed modelling methodology and application needs of this project.

Analytical solutions involve the use of functions and equations based on theoretical study of thermal and mechanical effects on materials and structures. These solutions include the use of beam bending theory [76, 77] and the study of structures as elastic multilayer systems [67, 70]. These solutions generate algebraic equations which when solved correctly produce exact solutions for stress and strains. However, the resulting set of non-linear algebraic equations are usually not trivial to solve and usually solved by use of computer. Despite this limitation, approximations can be made based on geometry of the structure under analysis that result in simpler equations to solve.

After reviewing the methodologies above (see Table 5.1), an analytical solution was chosen. This was because it eliminated the need for meshing or the use of other additional Computer Aided Design (CAD). Having created the thermal model using a discretization method, using a discretization method for the mechanical model would further increase the computational cost of the overall modelling methodology which would not be an acceptable compromise for the intended use of the overall modelling methodology. Further study was conducted to find the best analytical methods with relatively simplified equations which required only temperature input from each node in the thermal model and made use of common mechanical properties (Young's modulus, coefficient of thermal expansion, Poisson ratio, Yield strength) to output stress values at each node.

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Increased computational effort by at least two times the computational effort for the FEA thermal model presented in L's work.	High simulation time compared to analytical solution methods.	Inability to generate 3D stress map; Reduction in accuracy compared to FEA solution.	Increased complexity when extended to structure with more than two layers resulting in large computational effort to solve.	Assumes uniform temperature difference across the whole structure. Thus there will be reduced accuracy when used to analyse a power assembly structure.
Provides more accurate results compared to the other methodologies reviewed in this project.	Provides more accurate results compared to the other methodologies reviewed in this project.	Eliminates CAD and meshing; Simple to solve.	Simple and easy to solve formulas generated	eliminates CAD and meshing; complexity does not increase with increased number of layers (Only three parameters to solve for regardless of the number of layers in the system); Simple formulas which are simple to solve.
Use of CAD tools/ meshing to describe layers of power devices in full detail; Detailed description of material properties including non-elastic regions of materials.	Use of CAD tools/ meshing to describe layers of power devices in full detall; Possibility of use in coupled Electro- thermo- mechanical simulation; Use of adaptive meshing for regions in a structure that require additional resolution to minimize computational effort.	Use of beam bending theory.	Analyses structure as elastic multilayer system bonded at the ends and subjected to change in temperature.	analyses structure as elastic multilayer system with the ends fixed; Allows for difference in certain mechanical properties (Young's modulus, and CTE).
Numerical (FEM)	Numerical (FEM)	Analytical	Analytical (closed form)	Analytical (closed form)
Li [72]	Wachutka [75]	Hetnarski (76)	Suhir [70]	Hseuh [67] Boteler[56]

Table.5. 1: Comparison of published thermo-mechanical models based on the modelling methodology of this project

Contributions

Model Level

First Author/ year of publication

Advantage to modelling methodology Disadvantage to modelling methodology

5.4 1D- THERMOMECHANICAL MODEL

The first thermo-mechanical model created in this project is a one- dimensional thermo- mechanical model. The assumptions and analysis to make such approximation are detailed in subsequent sub-sections

5.4.1 Assumptions

The following assumptions were made to analyse a 3D structure (such as power assembly in Fig.5. 1a) as a 1D structure [78].

- Heat flow is considered 1D from top of chip to the bottom of power module assembly.
- (2) The only source of strain comes from thermal (temperature changes).Plastic and elastic creep was assumed to be zero.
- (3) The co-efficient of thermal expansion is constant. It does not change with temperature.
- (4) The mechanical model is NOT changing any variable in the thermal model.(The reasons for this assumption has been discussed in section 5.1).

Based on these assumptions, Fig.5. 1 can be treated as a 1D beam and each layer as a node on the 1D beam as seen in Fig.5. 1b.

5.4.2 Analysis

Each node is given a corresponding thermal force derived from the highest temperature value of that layer in the thermal model using (5. 2). Each layer is also given individual stiffness values which are calculated using (5.3). From the individual force and stiffness values, individual linear Force –Stiffness– Displacement matrix are generated for each layer which includes the interface between adjacent layers. The individual matrices are then added together, coded in VHDL-AMS and solved to

generate the displacement (u) values for each layer. For mechanical boundary conditions, the bottom layer (heatsink) is kept fixed [71] (i.e. equate the u value for the bottom layer to zero).

$$F_{Thermal} = E A \,\alpha\theta \tag{5.2}$$

$$K = \frac{AE}{L}$$
(5.3)

$$F = \mathrm{K}u - F_{Thermal} \tag{5.4}$$

$$\sigma = \frac{F}{A} ; \qquad \varepsilon = \frac{u - u_0}{u_0} \tag{5.5}$$



Fig.5. 1: 1D Force – Stiffness matrix node network (b) for the power assembly in (a) (drawing is not to scale)

From the equations above, A (unit m²) represents area of each layer, α represents coefficient of thermal expansion (CTE), L represents thickness of the layer (see Fig.5. 1); σ represents stress; ε represents strain; u represents displacement and u_0 (unit cm) represents initial displacement of each layer. Once the displacement values have been generated, equation (5.4) is used to generate the mechanical force in each layer while stress and strain values for each layer are generated using equation (5.5).

5.4.3 Validation

To validate this approach, a thermal load of 100W (typical power loss of the chips of the size in Fig.5.1) was applied to the chip layer in Fig.5. 1 with an ON time of 12 second and a total period of 20 seconds. Convection coefficient for the bottom surface was 10,000 W/m²K with an ambient and reference temperature of 300K. For validation of the thermal and mechanical model, the power assembly in Fig.5. 1 (the same structure in Section 4.6.2) was simulated in FEA [66]. The thermal properties for each layer are the same as used in Table 4.4 (Section 4.6.2) in Chapter 4. The mechanical and geometrical properties of each layer are given in the table below.

LAYER	Young's	Poisson	CTE (K^-1)	Dimensions
	modulus	ratio		(Length* Width*
	(Mpa)			Thickness) in cm
Chip (SiC)	4.3E5	0.14	4.0E-6	0.8 X 0.8 X 0.05
Solder	5.0E4	0.36	2.2E-5	0.8 X 0.8 X 0.005
Copper (Top)	1.1E5	0.33	1.64E-5	1.0 X 1.0 X 0.03
AIN	3.31E5	0.22	4.6E-6	3.0 X 3.0 X 0.064
Copper (bottom)	1.1E5	0.33	1.64E-5	3.0 X 3.0 X 0.03
Aluminium (Heatsink)	7.0E4	0.33	2.3E-5	3.0 X 3.0 X 1.03

Table.5. 2: Mechanical and geometrical properties of layers in the power assembly

The temperature comparison at the centre node of one of the chips in the chip layer is shown in Fig.5. 2. Due to symmetry, the temperature at similar regions of the chips have the same value. The results show that the model does not show close matching with the FEA result after the ON phase begins but produces a closer match as the simulation approaches the end of the ON phase. The temperature result from the centre node of the chip layer was passed on to the mechanical model to generate strain and stress values. The strain and stress values against time in the chip layer for the VHDL-AMS and FEA models are shown in Fig.5. 3 and Fig.5. 4 respectively. While the temperature values at the initial and final phases of the heating time period (0-12 seconds) show good matching, the temperature difference at other time points are significantly different. The differences in strain and stress values also show the weakness of the 1D thermomechanical model in relation to accuracy. The model results accuracy produce a maximum difference of 30% and should only be used when speed of simulation is of utmost importance.



Fig.5. 2: Maximum Temperature comparison between the FEA model and the VHDL-AMS model for the chip layer of Fig.5. 1



Fig.5. 3: Strain comparison between the FEA model and the VHDL-AMS model for the chip layer of Fig.5. 1



Fig.5. 4: Stress comparison between the FEA model and the VHDL-AMS model for the chip layer of Fig.5. 1

5.4.4 Speed and Accuracy comparison

A comparison of speed and accuracy of the two models based on the test conditions described above is done in Table 5.3. The FEA mechanical model mesh of Fig.5. 1 has 7336 nodes meaning 7336 equations to be solved numerically. The corresponding number for the VHDL-AMS model is 7. The increase in the number of nodes for the FEA mechanical model (compared to the number of nodes used in the FEA thermal simulation of the same structure) was done as based on the simulation best practice of using a higher order of meshing for sequential thermomechanical simulations based on discussion with experts in thermo-mechanical modelling in the course of the project although minimal benefit in accuracy was observed with the increase in the order of mesh elements used in the mechanical modelling for the structure in this application. The difference in maximum chip temperature is 2K and the difference in maximum stress values between both models is 10% thus, the VHDL-AMS 1D thermo-mechanical model provides a good trade-off between accuracy and computational efficiency for thermo-mechanical simulations with long simulation time where accuracy of within 10%- 30% is within the tolerance of the application need.

Table.5. 3: Speed and	accuracy compa	arison at time	= 10 s timepoint
	, , ,		

MODEL	NODES	Max Temp. (K)	Max Stress	Total
	(mechanical		(Mpa) on Chip	simulation
	model)		layer	time (Secs)
FEA	7336	379	198	1457
VHDL-AMS	7	381	179	11

5.5 3D- THERMO-MECHANICAL MODEL

The 1D thermo-mechanical model is suited to application needs where specific regions in a power assembly have been designated to be monitored before the simulation has commenced (for example a specific node on the centre of the chip layer could be monitored if it is known from previous experiment or FEA analysis to be the region of highest temperature or highest stress). It is also suitable in scenarios where simple projections can be made from calculated values of a particular node. For instance, the stress at the centre of the chip layer could be calculated from the 1D model and it could be assumed that the maximum stress on the chip would be no more than a 30% deviation from the value of stress from the centre of the chip. Results shown in [11] show that this is a reasonable projection to make.

However, in situations where relative comparisons are to be made across a whole layer (e.g. comparing what the relative change in stress values in the top chip layer surface when Si is used instead of SiC) or where information on both lateral and bending strain is needed, a more detailed mechanical model is required.

In this project an energy balance method was used in deriving the 3D mechanical model. The assumptions and analysis required are explained in subsequent subsections.

5.5.1 Assumptions

In deriving the 3D mechanical model, the following assumptions were made

- The only source of strain comes from thermal (temperature changes). Plastic and elastic creep was assumed to be zero.
- (2) There are no shear forces acting on the system.
- (3) There was no twisting or buckling.
- (4) The deformations are small.

- (5) The co-efficient of thermal expansion is constant. It does not change with temperature.
- (6) The mechanical model is NOT changing any variable in the thermal model.(The reasons for this assumption has been discussed in section 5.1).
- (7) Stresses and strains are low enough for a linear elastic approach to be used[70].
- (8) The individual layers in the power assembly can be treated as elongated rectangular beams experiencing small deflections and the theory of bending could be used to evaluate the strains and stresses [70].
- (9) Energy is conserved across the structure.
- (10) The structure under analysis is a symmetrical square structure.

Based on these assumptions, Fig.5. 1a can be analysed as an elastic multilayer system as shown in Fig 5.5.

5.5.2 Analysis

Consider a multilayer system as shown in Fig. 5.5 with n layers of film (a film is a layer with relatively small thickness compared to the bottom layer) on top of a substrate (i.e. bottom layer) with a far large thickness than all the other layers. This model is a good representation of the power assembly geometry dimensions in Fig.5. 1 (other layers with relatively small thickness on a heat spreader (heatsink) with far larger thickness). The term t_i represents the thickness of each layer where i is the layer number of each layer which increases from 1 to n with 1 being the substrate layer. The X - Y - Z axis convention used in Chapter 4 is repeated here with h_n being the dimensions in the y axis.


Fig.5. 5: Elastic multilayer system (X-Y axis view).

The system in Fig. 5.5 is considered to be at rest at room temperature. Then as the device is turned ON, the system experiences unconstrained expansion due to the ΔT (temperature change) resulting in thermal strains different for each layer in the system due to different coefficient of thermal expansion (α) values for each layer (seen Fig.5. 6a). Next, uniform tensile stress (or compressive force as the case may be) is imposed on the individual layers to achieve displacement compatibility such that the strain in the system is constant *C* (see Fig.5. 6b). The net force on the system remains zero. This force leads to the generation of non-symmetric stresses which lead to the bending of the layers as seen in Fig.5. 6c [79].



Fig.5. 6: (a) Unconstrained expansion in each layer with rise in temperature; (b) External forces constraining the dimensions to maintain displacement compatibility; (c) Bending; reprinted from [79]

As ΔT increases, the bending will be higher. The resultant bending of the system can be treated as an arc of a circle having a radius R (see Fig.5. 6c). Thus, this implies that the more bending that occurs, the smaller the R value will be (since R is inversely proportion to the magnitude of bending, another term proportional to the bending is introduced- this term is called *curvature* and is designated as 1/R). The point of origin of R changes with ΔT and thus cannot be relied on to determine the bending strain. However, this issue can be circumvented by using a point regarded to as the bending axis. This is a line in the cross section of the multilayer system (in Fig.5. 6c) where the bending strain is zero. This point is independent of ΔT and remains static regardless of the value of ΔT . Given that strain is a ratio, one can simply estimate the strain in any layer using the formula below

$$\varepsilon = C + \frac{y - t_b}{R} \tag{5. 6) [67]}$$

where the C value represents the contribution to the overall strain from lateral strain (along the X and Z axis) while the remaining terms on the right side of (5. 6) represent the contribution from the bending strain to the overall strain for each layer. Given that the bending component is inversely proportional to the radius of curvature and directly proportional to the bending axis, even though one may not know the actual value of elongation, by using two fixed points the t_b value and the y value for each layer), a bending strain value can be determined for each layer. Once the values of C , t_b and R have been calculated, the stress values for each node in the layer can then be calculated using

$$\sigma_i = E'_i (\varepsilon - \alpha_i \Delta T_i)$$
(5.7) [67]

The ΔT_i is the difference of temperature from each node in the thermal model from the reference temperature (usually the room temperature or initial operating temperature). Thus to get the stress map for each layer, the temperature values at different nodes are inputted into the equation above and the resulting solution is the stress value at that node. The E_i parameter in the equation above represents the Young's modulus values for each layer. For a biaxial structure [67] such as that of a power assembly, the Poisson ratio is considered in determining the effective Young's modulus to be used in the equation above. The effective Young's modulus is calculated by

$$E'_{i} = \frac{E_{i}}{(1 - v_{i})}$$
(5.8) [67]

Based on the above description of Fig.5. 5 and Fig.5. 6 three main forces can be identified. The uniform lateral forces, a bending force and a bending moment. If energy conservation (i.e energy balance) is maintained in the system, it means the sum up of the lateral uniform force, bending force and bending moment values will be zero.

The energy balance for the lateral uniform forces is derived from the 1^{st} term on the right hand side of (5. 6) and used to calculate the value of C.

$$\sum_{i=1}^{n} E'_{i} (\mathbf{c} - \alpha_{i} \Delta T_{i}) t_{i} = 0$$
(5.9) [67]

The energy balance for the bending forces (resulting from bending strain) on the structure is derived from the 2nd term on the right hand side of (5. 6) and used to calculate the value of t_b :

$$\sum_{i=1}^{n} \int_{h_{i-1}}^{h_i} \frac{E'_i(y - t_b)}{R} \, dy = 0 \tag{5.10} \ [67]$$

The energy balance for the bending moment (see "M" in Fig.5. 6c) i.e. the resultant bending moment is described with the equation below and is used to solve for R (radius of curvature).

$$\sum_{i=1}^{n} \int_{h_{i-1}}^{h_i} \sigma_i \left(y - t_b \right) \, dy = 0 \tag{5.11} [67]$$

It is also important to calculate the deflection of each layer.

Once, the R value has been calculated using (5.11), the defection value for each layer in the power assembly can be calculated using the formula below:

$$d_{\nu} = R - \sqrt{R^2 - \frac{l_0^2}{4}}$$
(5.12)

Here, d_v is the deflection (unit cm), l_0 (unit cm) is the initial length of the layer in the lateral axis (*X* axis) and *R* (unit cm) is the radius of curvature.

With this analysis, testing were carried out to validate this model. The validation is detailed in the next subsection.

5.5.3 Validation

In this project, it was not feasible to provide experimental validation of stress and strain values for the power assembly. However, it was possible to perform FEA thermo-mechanical simulation which is an acceptable benchmark to use in industry [73]. The test conditions remain the same as those used in the validation done in section 4.6.2 (Chapter 4). The geometrical properties remain the same. The mechanical properties were added in order to generate the stress and strain results. These mechanical properties remain the same as used in Table 5.2.





Fig.5. 7: (a) FEA and (b) VHDL-AMS constant mesh temperature results for chip layer of power assembly (section 4.6.2)



Fig.5. 8: (a) FEA and (b) VHDL-AMS constant mesh temperature results for half of the AiN (dielectric) layer of power assembly test (section 4.6.2)





Fig.5. 9 shows the stress map at the chip layer (derived at the t= 10 second time step). The VHDL-AMS solution shows a maximum stress value of 202Mpa while the maximum stress result of the FEA solution is 198Mpa. Despite the difference in values, the VHDL-AMS solution trend (i.e. where the maximum and minimum values are located) is similar to that of the FEA solution with the largest stress values being at the edges of the chip layer. This shows the VHDL-AMS model is capable of also capturing the stress value trend in the chip layer.



Fig.5. 9: Stress Comparison on Chip Layer in the (a) VHDL-AMS model and (b) FEA model

Similarly, in the AiN region (Fig.5. 10), the VHDL-AMS also captures the spread of stress values. The maximum stress value being away from where the region that is directly underneath the chips. The maximum stress value in the VHDL-AMS solution is 202.3Mpa compared to 237.2Mpa maximum stress in the FEA solution. The FEA stress solution has a wider value range over the AiN due to the larger temperature gradient in the FEA temperature solution and the top and bottom left corner region values which are not accounted for by thermal strain- thus are not captured by the VHDL-AMS thermal model [11] . Despite the difference in values, the VHDL-AMS solution trend is similar to that of the FEA solution with the lowest stress in both the VHDL-AMS model is capable of also capturing the stress value trend in the AiN (dielectric) layer.



Fig.5. 10: Stress Comparison on (a) AiN Layer FEA model and (b) VHDL-AMS model

Fig 5.11 shows the curvature of the whole system. As predicted with increasing temperature values, the magnitude of curvature increases, and then returns to a value of zero at room temperature.



Fig.5. 11: Curvature plot for VHDL-AMS model over the simulation cycle

Deformation

The deformation of each layer (a value of the amount of bending from the original length for each layer) is a result of importance to power module designers for evaluating power module designs. Using the formula given for deformation in (5. 12), deformation for individual layers could be derived. The values for deformation (deflection) in the Chip, AiN, Copper (top) and solder layers are shown below.



Fig.5. 12: deformation (vertical displacement for AiN, Copper (Top), Solder and Chip layer of the power assembly based on test conditions

The highest deformation magnitude could be seen in the AiN layer. The deformations are very small and thus confirming the assumption of *small deformation* (see section 5.5.1) in deriving the 3D model is valid.

5.4.4 Speed and Accuracy comparison

A comparison of speed and accuracy of the FEA and 3D VHDL-AMS model solutions based on the test conditions described earlier is done in Table 5.4. The FEA mechanical model mesh of Fig.5. 1 has 7,336 nodes meaning 7,336 equations to be solved numerically. The corresponding number for the VHDL-AMS model is 2560 but unlike the FEA model, these equations are algebraic and require less computational effort. The difference in temperature is 3K while the difference in maximum chip layer stress values between both models is within 2%. Although the difference in stress value is large in some regions of the AiN layer, the VHDL-AMS model is able to derive results in the right qualitative trend across the layers which is very useful for parametric analysis (as discussed in Chapter 1). The increase in the number of nodes for the FEA mechanical model (compared to the number of nodes used in the FEA thermal simulation of the same structure) was done as based on the simulation best practice of using a higher order of meshing for sequential thermomechanical simulations based on discussion with experts in thermo-mechanical modelling in the course of the project although minimal benefit in accuracy was observed with the increase in the order of mesh elements used in the mechanical modelling for the structure in this application.

Table.5. 4: speed and accuracy comparison

MODEL	NODES	Max Temp	Max Stress	Total simulation
		(К)	(Mpa)	time(seconds)
			(Chip layer)	
FEA	7336	379	202	1604
VHDL-AMS	2560	382	198	86

5.6 CONCLUSION

The thermo-mechanical models created in this work as part of the overall modelling methodology were described in detail in this work. The fundamental equation to be solved in the mechanical domain was given and a review of thermo-mechanical models was given. Two thermo-mechanical models were created- the 1D and 3D thermo-mechanical models. The assumptions used in deriving the models were also given.

The 1D model provides a rough estimate of stress in each layer in the power assembly. Where simulation speed is of critical priority and specific regions in a power assembly have been designated to be monitored before the simulation has commenced (for example a specific node on the centre of the chip layer could be monitored if it is known from previous experiment or FEA analysis to be the region of highest temperature or highest stress), it could be used. However, in thermo-mechanical or electro-thermo-mechanical parametric studies, where more detail is required in the layers of the power module, a more detailed 3D model was created to be used. The principle of energy balance was used to derive three parameters which determined the strain value and from which the stress value could be calculated. The equation used to extract vertical deformation values in order to observe the deflection in the *Y* axis direction in qualitative terms was highlighted in this chapter.

The 1D and 3D thermomechanical models built in this project were compared with uncoupled FEA simulations. On comparing the accuracy of the stress values the 1D model maximum stress results were within 30% accuracy while the 3D results were within 10%. Improvements could be made on the VHDL-AMS model to get more accurate values. The 3D model could be improved to handle effects not due to thermal strain as observed in the bottom corner of the AiN layer results. However, the 3D model is able to detect the position of the maximum, minimum stress and the qualitative value of stress gradient across layers. Thus, the model could be used in parametric analysis. The thermo-mechanical model and coupled electro-thermo-mechanical model are used for parametric analysis in Chapter 6.

CHAPTER 6 – PARAMETRIC ANALYSIS OF POWER MODULE DESIGN USING ELECTRICAL, THERMAL AND MECHANICAL MODELS

6.1 INTRODUCTION

A major application for the overall modelling methodology proposed in this thesis is for parametric analysis of power module design either during the design of new power modules [80, 81] or in analysis of existing power modules [81, 82]. The electrical, thermal and mechanical models have been described in chapter 3, 4 and 5 respectively. In these three chapters, some multidomain simulation results have been shown. However, in these cases, the design parameters (in the *entity* of the VHDL-AMS electrical, thermal and mechanical models) have been fixed. In parametric analysis, parameters are varied to observe the effect in their domain as well as their effects on other energy domains.

Having validated the electrical, thermal and 3D mechanical models in Chapter 3, chapter 4 and chapter 5 respectively, the aim of this chapter is to showcase the benefit of the multidomain modelling methodology presented in this work in analysing coupled multidomain power electronic design scenarios.

6.2 DESIGN SCENARIOS

In this section, the different design scenarios, test conditions and parameter sweep are detailed. The results are shown and are discussed in this section. The structure to be used for the parametric analysis in this subsection is the power assembly (see Section 1.2 in chapter 1 and Section 4.6.2 of chapter 4 of this thesis). The test structure



and the test circuit to be used are reproduced below.

Fig.6. 1: Power assembly test structure for parametric analysis



Fig.6. 2: Test circuit for Electro-Thermomechanical parametric analysis

The approach used in the parametric analysis is to have a standard benchmark to compare against. The benchmark used is a SiC device in the chip layer and other layers in the power module assembly. Fig.6.1 is intended to show the generic structure of a power module assembly and doesn't not indicate connection of any of the four MOSFETs in an electrical topology.

TEST CONDITIONS

The design scenarios in this section belong to either a Thermo- mechanical parametric test or an electro-thermo-mechanical parametric test. In each design scenario the parametric test is mentioned. For the electro-thermo-mechanical test, a power cycling setup (shown in Fig.6. 2 is used). In order to observe significant temperature deviation from room temperature on the chip layer, a current of 350A is fed to the chips over a time period of 5ms second ON and 5ms OFF with delay, rise time and fall times each lasting 0.2ms. *Vgs* = 18V (ON) and 0V (OFF). In order to realise this, a voltage input of 350V is applied across the resistor R1 (1 Ω) in series with the D.U.T. which is the module assembly in Fig.6.1. The results are compared for different parameters at time T= 5 ms. The parameter property values of the layers in the power module assembly from chapters 3, 4 and 5 reproduced in this section.

The thermomechanical parametric tests also represent realistic design scenarios and provide an opportunity to validate the VHDL-AMS model in parametric tests that was not available for electro-thermo-mechanical parametric tests during the course of the project. The test condition for the thermomechanical test is a power load pulse of 100W for 12 seconds and an OFF period of 8 seconds (the same test used in section 4.6.2 and section 5.5). The results are compared for different parameters at time T= 10 seconds.

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The benchmark thermal parameter values can be seen in Table.6. 1 while the benchmark electrical parameter values can be seen in Table.6. 2. The mechanical model used is the 3D mechanical model (section 5.5) and the benchmark parameter values can be seen in Table 6.3.

Layer	Thermal Properties			Thickness	Width
	Thermal	Density	Specific		(cm)
	Conductivity		Heat		
	(W cm ⁻¹ K ⁻¹)	(g cm ⁻³)			х
			(Jg ⁻¹ K ⁻¹)		
					Height
					(cm)
chip (SiC)	1.6	2.3	0.7	0.05	0.8 X 0.8
solder	0.5	12.0	0.25	0.005	0.8 X 0.8
copper (top)	4.01	8.94	0.385	0.03	1.0 X 1.0
dielectric	2.85	3.26	0.82	0.064	3.0 X 3.0
(AiN)					
Copper	4.01	8.94	0.385	0.03	3.0 X 3.0
(bottom)					
Heat sink	2.3	3.26	0.74	1.03	3.0 X 3.0

Table.6. 1: Thermal parameter values (benchmark)

Table.6. 2: electrical parameter values (benchmark)

Parameter	Description	Values	Unit
КрО	Transconductance	1.18	A/ V ⁻²
	factor		
VT0	Zero- bias threshold	3.3	V
	Voltage		
THETA1	Transverse electric field	0.028	V ⁻¹
	factor		
THETA2	Parallel electric field	0.019	V ⁻¹
	factor		
LAMBDA	Channel Length	0.05	V ⁻¹
	Modulation		
KF	Non-uniform channel	0.75	
	doping factor		

RAJ10	RAJ1 drain resistance	0.254	Ω
	parameter at TO		
RAJ20	RAJ2 drain resistance	0.339	Ω
	parameter at TO		
REP10	REP1 at TO	0.011	Ω
V1	Drain resistance	12.99	V
	parameter		
V1	Drain resistance	0.0606	V
	parameter		
η	Drain resistance	2.7034	
	coefficient		
CGD0	Zero bias gate-to-drain	0.6E-9	F
	capacitance		
CGDMIN	Minimum gate-to-drain	0.01E-9	F
	reversed biased		
	capacitance		
Vgd*	Gate-to-drain	2.0	V
	capacitance parameter		
CDS0	Zero bias drain to source	2E-9	F
	parameter		
CDSMIN	Minimum gate-to-drain	0.06E-9	F
	reverse biased		
	capacitance		
Vds*	Drain-to-source	10	V
	capacitance parameter		
CGS	Gate-to-source	1.05E-9	F
	capacitance		
am	Kp0 temperature	1.007	
	parameter		
bm	Kp0 temperature	0.9720	
	parameter		
cm	Kp0 temperature	1.007	
	parameter		
dm	Kp0 temperature	0.9482	
	parameter		
aTH	VT0 temperature	0.004	K-1
	parameter		
bTH	VT0 temperature	0.87	V
	parameter		
rO	REP1 temperature	2.42	
	coefficient		
r1	RAJ1 temperature	0.94	
	coefficient		
r2	RAJ2 temperature	0.55	
	coefficient		
alpha_i	REP1 RAJ1 RAJ2 high	0.1661	
	temperature coefficient		

The benchmark mechanical properties can be seen in Table.6.3.

	Young's	Poisson	CTE	Dimensions (Length*
LAYER	modulus (Mpa)	ratio	(K^-1)	Width* Height) in cm
Chip (SiC)	4.3E5	0.14	4.0E-6	0.8*0.8*0.05
Coldon		0.20	2 25 5	
Solder	5.0E4	0.36	2.2E-5	0.8*0.8*0.005
Copper	1.1E5	0.33	1.64E-5	1.0*1.0*0.03
(top)				
AIN	3.31E5	0.22	4.6E-6	3.0*3.0*0.064
Copper	1.1E5	0.33	1.64E-5	3.0*3.0*0.03
(bottom)				
Heat sink	7.0E4	0.33	2.3E-5	3.0*3.0* 1.0

Table.6. 3: mechanical parameter values (benchmark)

Other parameters used in the benchmark result include

Ambient Temperature (Ta) = 300K

Zero stress reference temperature = 300K

Bottom coefficient of convection (hbot) = $1 \text{ W/ cm}^2 \text{ K}$

Top coefficient of convection= 0.001 W/ cm² K (natural convection)

Side coefficient of convection= 0.001 W/ cm² K (natural convection)

Once the analysis is done for a given power assembly structure using the above parameters it became a benchmark against which results from the parametric analysis could be compared.

6.2.1 DESIGN SCENARIO 1: Thermal parameter

The bottom convection coefficient is determined by the nature of thermal management design implemented for the power assembly. Ideally, one would prefer the solution that results in the smallest rise in temperature in operating conditions. However, other factors such as weight and cost usually need to be considered. Thus arises a possible design question- is the proposed added thermal management component worth the cost in terms of additional cooling benefit?

The test conditions and parameter sweep for this scenario are detailed below.

Test circuit: Thermo- mechanical simulation

Test conditions: Benchmarked test conditions and parameter values

Parameter sweep: *hbot* (bottom coefficient) varied from 1 to 10 W/ cm^2 K.

One result is observed for each (thermal and mechanical) domain- maximum temperature in the power assembly (thermal) and maximum stress in the chip layer (mechanical). Although these are the only results displayed here, any other information such as deflection, temperature at other layers in the power assembly can also be derived from the models as required by the user. Fig.6. 3a shows the temperature result for different changes in *hbot* values. The maximum temperature is in the chip layer. The results show that increasing hbot (which usually depicts more complex cooling/thermal management), results in a lower value of the maximum temperature. However, it was observed that from 6 W/ cm² K, there is relatively little additional reduction in temperature for the additional complexity in thermal management system. Thus, a complex cooling with more than 6W/ cm² K would not be useful for the structure and dimensions of Fig.6. 1 if the goal is to design compact and efficient power electronic systems.

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The maximum chip stress result for the parametric sweep of hbot are shown in Fig.6. 3b. It is shown that with increased *hbot* values, a decrease in chip layer stress values is observed. The VHDL-AMS model provides a better match with temperature at lower *hbot* values and produces a good match with the FEA result over the whole range of *hbot* values.





Fig.6. 3:Temperature (a), Current (b) and Stress (c) comparison for different values of hbot

6.2.2 DESIGN SCENARIO 2 – Electrical parameter

The threshold voltage (*Vto*) of a power MOSFET is the minimum voltage value which must be exceeded by the gate-source voltage (*Vgs*) before the MOSFET can begin conducting current. It is a very important parameter and is considered at the initial phases in the design of a power module. Even when Vto values have been fixed for the MOSFETs in a power module, in reality due to manufacturing process, *Vto* values could deviate from the originally designed *Vto* values. Thus arises a possible design question- what is the effect of varying the *Vto* value in the electrical domain, what is its effect on temperature and what is its effect on stress values in the power module?

The test conditions and parameter sweep for this scenario are detailed below.

Test circuit: Coupled Electro- thermo- mechanical using transient test setup in Fig.6.2.

Test conditions: Benchmarked test conditions and parameter values

Parameter sweep: *Vto* (Threshold voltage at room temperature) varied from 2V to 6V.

The maximum chip temperature result for different values of *Vto* is shown in Fig.6. 4a indicating a positive change in temperature for changes in *Vto*. The effect of change of *Vto* with respect to the value of chip current is shown in Fig.6. 4b to be a reduction of current with increasing *Vto* values. The change in value of stress at the point of maximum stress in the chip layer is shown in Fig.6. 4c. A negative relation with changes in *Vto* is also observed.





Fig.6. 4: Temperature (a), Current (b) and Stress (c) comparison for the

combined electro-thermo-mechanical

6.2.3 DESIGN SCENARIO 3- Material parameter

Given the choice of different materials to use for the different layers in the power module, a power module or power electronic system designer may be interested in observing and comparing the magnitude of multidomain effects for different materials. A possible design scenario could be to observe the relative magnitude of maximum temperature and stress value in the chip layer if Si was used in the chip layer rather than SiC. To conduct this study, the 3D thermo-mechanical model is simulated with Si properties instead of SiC.

The test conditions and parameter sweep for this scenario are detailed below.

Test circuit: Thermo- mechanical simulation

Test conditions: Benchmarked test conditions and parameter values

Parameter sweep: Si Thermal (thermal conductivity 1.35 W cm⁻¹K⁻¹; Density 2.34 g cm⁻³; Specific heat capacity 0.735(J g⁻¹ K⁻¹) and mechanical (Young's modulus 1.8E5 Mpa; CTE 2.5E-6 and Poisson's ratio 0.22) replacing their respective values for SiC. The chip size was also adjusted for Si(by using 0.12 cm by 0.12cm for the area of the chip as against 0.8 cm by 0.8cm for SiC) [83]

The comparison for results for both materials is shown in Fig.6. 5. SiC has a larger temperature rise over the heating phase than Si for the same power input. With a larger Young's modulus values than that of Si, Sic also experiences larger stress values than Si. This information is useful in determining the operating limits of the power devices.

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Fig.6. 5: Temperature and Stress comparison for Si and SiC

6.2.4 DESIGN SCENARIO 4- Geometry parameter

The different layers in the power assembly structure have different geometrical dimensions. The dielectric layer for instance has a relatively higher thickness compared to the copper layers on either side of it in order to enable it perform its electrical isolation function. A possible design study of interest to a power electronic designer would be to know the optimum thickness of the layers in the power assembly. For instance, a designer might be interested in knowing the optimal thickness value of the dielectric layer that will give the optimum maximum temperature and stress values. This information impacts factors such as power density and cost.

To answer this question, a range of thickness values were simulated for which the maximum stress values at and maximum temperature values in the chip layer observed for each thickness values. The test conditions are detailed below:

Test circuit: Thermo- mechanical simulation

Test conditions: Benchmarked test conditions and parameter values

Parameter sweep: AiN (dielectric layer) thickness varied from 0.02cm to 0.18cm

The comparison for results for both materials is shown in Fig.6. 6 below.

The maximum chip temperature result for different values of AiN thickness (Fig.6. 6a) shows minimal change. Thus, over the test period, there was no significant change to the chip temperature despite varying the thickness of the dielectric although one can observe the slight increase in temperature with increasing thickness of the dielectric because the thermal resistance of the dielectric increases with thickness [11]. A decrease in the maximum value of stress on the chip layer values was observed with increasing thickness layer (Fig.6. 6b).

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Fig.6. 6: (a) Temperature and (b) Stress for different values of AiN thickness

6.2.5 DESIGN SCENARIO 5- Mechanical parameter

Important design case studies could be observed by varying parameters in the mechanical model. For example, it is possible to have a material with different orientation with each orientation having different mechanical parameter values [84]. If one orientation of a material was to be replaced by another orientation of the same material in the manufacture of a layer of the power module, it is important to observe the multidomain effects of such replacement. Consider, the dielectric layer- what would be the effect on maximum chip temperature and stress if the coefficient of thermal expansion (CTE) was changed due to use of a material with different orientation? To obverse this in the overall modelling methodology, a multidomain simulation would be run with a parametric sweep of the CTE value for the dielectric layer.

The test conditions and parameter sweep for this scenario are detailed below.

Test circuit: Thermo- mechanical simulation

Test conditions: Benchmarked test conditions and parameter values

Parameter sweep: CTE for dielectric layer varied from 4.2E-6 to 5.4E-6

Given that the results in the mechanical model are not currently fed back into any other domain (see section 5.1), the temperature results remain unchanged across the structure and are not shown in this design scenario. The stress value however changes across the power assembly structure and the change in stress value for the point of maximum stress on the chip layer is shown in Fig.6. 7 where a positive relationship between stress and dielectric CTE is observed. In this scenario, it was possible to obtain a similar simulation using FEA and the VHDL-AMS model is seen to show good qualitative and quantitative matching with the FEA solution.



Fig.6. 7: Stress comparison for different values of CTE of dielectric

6.2.6 DESIGN SCENARIO 6- Circuit parameter

Another interesting study to observe is the effect of external circuit parameters on results across multiple domains. External circuit parameters refer to other variables which are not part of the electro-thermo-mechanical model but are present in the circuit schematic. From Fig.6. 2, external circuit parameters such as drain voltage value and gate- source voltage values can be observed. A possible design scenario could be- what is the effect of the change in gate voltage on temperature, current and stress values on the chip layer during the operation of the power module.

The test conditions and parameter sweep for this scenario are detailed below.

Test circuit: Coupled Electro- thermo- mechanical using transient test setup in Fig.6.2.

Test conditions: Benchmarked test conditions and parameter values

Parameter sweep: *Vgs* varied from 16V to 20V.

The maximum temperature result for different values of Vgs is shown in Fig.6. 8a indicating a linear change in temperature with changing Vgs values. The positive linear relationship between current and Vgs in Fig.6. 8b is as expected with increasing Vgs values. The maximum stress value on the chip layer is also shown to change linearly increasing Vgs (Fig.6. 8c) in this particular test. Given that the power module assembly is a stack of layers connected together, because of the short test period, there is little temperature rise in the lower layers of the module thus those layers experience very little or no contraction. This constrains the movement of the chip layer and thus causes it to experience a compressive (negative) force. With increasing Vgs (and all other conditions fixed), there is less loss (because of more conduction in the MOSFET channel), thus the chip temperature reduces and thus, there is lower compressive stress on the chip [83] . This is important information to power module and power converter designers in determining the operating limits of the power module.





Fig.6. 8: Temperature (a), Current (b) and Stress (c) comparison for different values of Vgs

6.3 SIMULATION TIME FOR DESIGN SCENARIOS

The table below shows the average simulation time for the design scenarios in the previous section (section 6.2). The thermo-mechanical parametric tests on an average lasted 90 seconds to simulate every time a parameter was varied in a design scenario. In contrast, benchmark FEA simulation such as the thermo mechanical FEA solution (see section 5.5.3) which simulated in 1604 seconds. The coupled Electro-thermomechanical simulations had longer simulation period for each parameter change. This was due to the electrical model which included voltage dependent resistance equations required to represent the reduction in electron mobility in SiC MOSFETS due to oxide interface traps. However, as can be seen below (in Table.6.4), the simulation time for the combined VHDL-AMS Electro-thermo-mechanical model simulation was still less than the simulation time of the FEA thermo-mechanical while providing valuable information on thermal interactions in the power assembly as well

as the effect of the thermal interactions, CTE mismatch and other mechanical properties on the stresses present during operation of the module.

DESIGN SCENARIO	SIMULATION TIME (secs)
1	86
2	886
3	86
4	90
5	86
6	726

Table.6. 4: Simulation time for design scenarios

This indicates that the coupled electro-thermo-mechanical model derived from the overall modelling methodology is also computationally efficient to be used in parametric studies for the design and analysis of multichip power modules.

6.4 CONCLUSION

The electrical, thermal and mechanical models generated in previous chapters as part of the overall modelling methodology proposed for the design and analysis of multichip power module structures were coupled and used in realistic power electronic simulations. A number of design and analysis scenarios for which a parametric sweep of specific parameters was required were discussed. Although a wide range of results could be generated by the parameter sweep for each scenario, in this thesis, the result for the maximum temperature, current and maximum stress in the chip layer were analysed as these are common results required by power module and power electronic system designers. The effect of varying specific parameters differed in magnitude and relationship order. While some had a linear relationship, some had exponential relationships with different gradients along the parameter sweep. The results also show how current, stress and temperature values are affected by different phenomena with different order (e.g. positive linear, negative linear, exponential) and magnitude relations to the parameter that is being varied.

Thermal maps, stress maps and detailed explanation of the results have not been presented in this chapter because the aim of this chapter is not necessarily to explain the foundational phenomena underlying the results but to demonstrate the capability of the modelling methodology to be used in multidomain parametric study of power module structures. The results can then be used in determining the optimum operating limits of the power module, optimum material and geometric layout of the structure and to incorporate other parameters such as cost.

The simulation time is also in the order of seconds with the longest simulation taking 886 seconds. This shows that the simulation methodology presented in this work is capable as being used as a tool to provide answers to design questions and analyse alternative design solutions quickly.

CHAPTER 7: CONCLUSION AND FURTHER WORK

Increasing energy demands in different application fields of power electronics (e.g. Photovoltaics, Traction, aerospace) have led to increased demand for power electronic systems with higher conversion efficiency, higher power density, reliability and higher operating temperatures among other needs. To meet these demands, packages are being designed with multiple chips to increase power rating and power density of power devices. Multiple chip packages (multi-chip) packages are complex structures that operate over multiple energy domains (e.g. electrical, thermal, mechanical domains) which must all be considered when designing these packages. Building physical prototypes to investigate the resulting effects from the multi domain operation of multichip modules early in the design process can be immensely cost and time expensive. Simulation provides a cost effective alternative to observe electrical, thermal and mechanical behaviour of designs, compare designs and observe the effect of varying electrical, thermal, material, mechanical, geometric properties on electrical, thermal, mechanical behaviour.

In order to maximize the benefit of simulation, an overall modelling methodology for using simulation to observe these multi-domain effects in multichip power module structures is needed and the methodology should provide an optimum balance between accuracy and computational efficiency. A review of modelling methodologies used in currently available software and their downsides with respect to speed and accuracy was discussed in Chapter 1. Knowledge from the review was used to propose an overall modelling methodology for efficient software design and analysis of power module designs which was discussed in Chapter 1. The presented overall methodology eliminated the use of CAD drawing tools and complex meshing
that is used in commercial software. Implementing the overall modelling methodology required a modelling language therefore, a review of modelling language and platforms was conducted by a literature study and the rationale for the selected modelling language was given in chapter 2.

Models consist of differential equations that need to be solved numerically. Thus, numerical solution methods was reviewed through literature study for knowledge to build models with equations that would be solved efficiently. The literature study of numerical methods highlighted some pitfalls which negatively affect computational efficiency and solutions to the pitfalls were proposed in Chapter 2.

The device model used for the electrical aspect of the overall modelling methodology is described in chapter 3. Power MOSFET models in literature were reviewed to select a modelling approach which presented the best compromise between accuracy and computational efficiency. A power device model was then developed based on the selected modelling approach, validated in steady state simulations and the model's capability for use in transient simulation was also shown in Chapter 3.

The model used for the thermal aspect of the overall modelling methodology is described in Chapter 4. Thermal models in literature were reviewed in order to select a modelling approach which presented the best compromise between accuracy and computational efficiency. A thermal model based on a discretized solution of the heat equation was created in this work. The moving mesh algorithm which is designed to increase the spacial resolution of high temperature gradient regions in the thermal model without increasing the number of equations to be calculated is explained in Chapter 4. The thermal model could be configured as a constant mesh step model or moving mesh step model by varying a few parameters and this was discussed in detail in chapter 4. The thermal model was used in coupled and uncoupled thermal

simulations and validated with FEA and experiment. The thermal model results show maximum temperature values within 10% accuracy in each layer of test structure when compared with the FEA or experimental result used for validation. For the same tests and producing similar levels of accuracy in maximum temperature results, the thermal model in moving mesh configuration was shown to improve the result in a single layer structure (device level simulations) providing a justification for the increase computational effort required to calculate the temperature gradient and move the meshes. However, in a multilayer power module structure, the constant mesh thermal model was within 3K of the benchmarked values and the moving mesh did not produce considerable benefit in terms of accuracy and simulation speed.

The model used for the thermo- mechanical aspect of the overall modelling methodology is described in Chapter 5. Mechanical models available in literature were reviewed to select a modelling approach with provided the best compromise between accuracy and computational efficiency. Two thermo- mechanical models were built- 1D and 3D thermomechanical models. The comparative advantages and disadvantages of the 1D and 3D thermomechanical models as well as the validation of the models in simulation is shown in Chapter 5. The assumption of square and symmetrical structure for the power assembly enabled the 3D power assembly to be treated as a 1D problem using a set of analytical equations which were presented in chapter 5. Using the nodal temperature derived from the thermal model as input, the analytical equations for the 3D model were used to generate stress and strain values which could then be plotted as 2D maps. Although the 1D model is unable to produce 2D stress maps, it was shown to produce maximum chip stress results within 30% of the FEA result and a reduction in simulation time of for the test condition used. The 3D mechanical model provided better matching with the benchmarked FEA values

and was able to predict the position of the maximum and minimum values of stress in the layers of the power assembly structure.

The overall modelling methodology is used in realistic design scenarios in chapter 6. Parametric studies with thermo-mechanical and combined electro-thermomechanical models where electrical, thermal, mechanical, material, geometrical properties are varied and their effect across multiple domains are observed. This was implemented by inserting the electrical, thermal and mechanical models into a circuit simulation environment and running parametric simulation in the same manner as with any other model in any circuit simulator. Combined with the low simulation time of the coupled simulations, the results and capabilities presented in this thesis show that the overall modelling methodology is a time and cost-saving tool to be incorporated in the design of power modules before physical prototyping of the design is conducted.

7.2 FUTURE WORK

The following areas could be further investigated:

- **Coupling with advanced electro-magnetic model**: This would enable variation of inductance values during simulation.
- Improved accuracy of the boundary regions for temperature in the thermal model away from the device region: if implemented without adverse effect on computational efficiency, it increases the accuracy of maximum temperature value in each layer of the power module assembly structure under analysis.

- Removal of symmetrical square assumption used in thermomechanical model: This would enable the analysis of generic types of structures with different aspect ratios and shapes.
- More user- friendly VHDL-AMS code interface: Adding pop-up information features to the VHDL-AMS code interface to guide users will improve usability of the code interface.
- Building a solver (simulator) with better numerical solution performance for power electronic applications: The guide for writing model equations detailed in Chapter 2 could be implemented in a designing a new simulator which could be specialized for power electronics simulations. Thus, improving the computational efficiency when simulating power device models such as the models generated in this project.
- Inclusion of bond wires and interconnects in the thermal model of the power module. The thermal model presented in this work could be improved to include bond wires, casing and other interconnects.

SCIENTIFIC CONTRIBUTION

A methodology for the development and preliminary multidomain performance assessment of novel multichip packaging technology for Wide Band Gap devices capable of use in circuit simulation environments is implemented in this work. The methodology is based on the use of physics- based analytical semiconductor models coupled with distributed structural modelling of the package for the thermal effects also coupled with analytical mechanical models to observe stress and strain effects.

A scheme was implemented for the thermal aspect of the methodology which enables to operate with a fixed number of equations while redistributing the nodes in the mesh as a function of critical variables and their derivatives over space (e.g. temperature distribution and temperature gradient during transient analysis). The energy conservation principle was used to generate analytical equations which compute the value of stress and strain based on the temperature values from the thermal aspect of the methodology.

The coupled electro-thermo-mechanical model are used in a circuit simulation environment to simulate realistic design scenarios where design parameters were varied and corresponding effect were observed in multiple domains. The results show that trade-off between computational efficiency and accuracy currently used in commercial simulation tools for power electronic design can be improved resulting in increased cost and design time savings.

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APPENDIX

A.1: Electrical Model Measurements

A.1.1. Curve Tracer

The curve tracer used for the static characterisation of the device in Chapter 3 is the Tektronix 371A [85] programmable high power curve tracer. It provides high resolution voltage and current measurements (down to 1 pA and 50 μ V) [85].

When configured in *sweep measure* mode, the curve tracer uses low duty cycle pulses in deriving the characterization result thereby obtaining output results without excessively heating the device.

For higher temperature- a hotplate was used to heat up devices to the required temperature which was verified by a thermocouple connected as close as possible to the junction of the device before characterization measurements were obtained.

A.1.2 Output characteristic model and measurement result comparison Room Temperature (27 °C)

	ERROR%	0	7.730769	11.16949	11.8	10.375	9.498584	6.741627	3.51046	1	2.706485	3.131148
	Model	0	11.1	19.5	27.7	35	38.3	44.2	49	53.5	57.6	59.7
Vgs=20V	Measure	0	10.4	17.7	25	32	35.3	41.8	47.8	53.5	58.6	61
	ERROR%	0	1.980392	6.202312	7.557377	7.430868	7.122449	5,187192	3.159827	1.193424	2.410935	2.528014
	Model	0	10.3	18.2	26	33.1	36.4	42.3	47.3	51.8	55.9	58
Vgs=18V	Measure	0	10.2	17.3	24.4	31.1	34.3	40.6	46.3	51.7	56.7	58.9
	ERROR%	0	6.050505	2.190476	2.702128	4.020134	4.343465	4.359173	2.818182	1.408163	1.559701	1.897666
	Model	0	9.4	16.6	23.9	30.7	34	40	44.8	49.2	53.3	55.2
Vgs=16	Measure	0	9.9	16.8	23.5	29.8	32.9	38.7	44	49	53.6	55.7
	ERROR%	0	12.90476	8.432432	5.225352	1.722022	1.325733	2.098901	2.216545	1.881057	1.407332	1.196464
	Model	0	8.4	14.8	21.3	27.7	30.7	36.4	41.1	45.4	49.1	50.9
Vgs= 14V	Measure	0	9.4	15.9	22.2	27.9	30.6	36	40.6	45	48.9	50.8
	ERROR%	0	24	18.29545	13,69863	5.241935	2.962963	0.320513	0.859599	1.570681	1.703163	1.173709
	Model	0	1.9	7.19	12.6	23.5	26.2	31.1	35.2	38.8	41.8	43.1
VGS=12V	Measure	0	2.5	8.8	14.6	24.8	27	31.2	34.9	38.2	41.1	42.6
	ERROR%	0	24.67532	17.88618	11.84049	6.428571	3.857143	0.847458	0.700389	0.010909	3.780069	6.040268
	Model	0	5.8	10.1	14.37	18.34	20.19	23.4	25.88	27.497	28	28
Vgs = 10V	Measure	0	7.7	12.3	16.3	19.6	21	23.6	25.7	27.5	29.1	29.8
vds		0	1	2	ŝ	4	5	9	7	∞	6	10

Temperature = 200°C

	ERROR%	0	22.875	20.81982	18.30769	14.5	11.33058	8.117438	5.402516	3.549575	2.036269	1.240385
	Model	0	7.8	13.3	18.3	22.7	26.7	30.1	33.2	36.2	39	41.7
Vgs=20V	Measure	0	6.4	11.1	15.6	20	24.2	28.1	31.8	35.3	38.6	41.6
	ERROR%	0	16.625	15.54545	13.90323	11.10101	8.531381	6.035971	4.194888	2.436782	1	1.487805
	Model	0	7.4	12.6	17.5	21.8	25.7	29.2	32.3	35.3	38.1	40.8
Vgs=18V	Measure	0	6.4	11	15.5	19.8	23.9	27.8	31.3	34.8	38.1	41
	ERROR%	0	10.52381	10.25926	9.552632	7.701031	5.680851	3.930403	1.974026	1.292398	2.340483	3.233251
	Model	0	6.9	11.8	16.5	20.7	24.6	28.1	31.1	34.1	36.8	39.4
Vgs=16	Measure	0	6.3	10.8	15.2	19.4	23.5	27.3	30.8	34.2	37.3	40.3
	ERROR%	0	2.587302	2.834862	2.973684	2.554404	1.434783	1.757576	3.040816	4.095975	4.428571	5.266667
	Model	0	6.3	10.9	15.2	19.3	23	26.4	29.4	32.3	35	37.5
Vgs= 14V	Measure	0	6.2	10.7	14.9	19	22.9	26.6	30	33.3	36.2	39.1
	ERROR%	0	8.196721	5.825243	5.555556	5.434783	5.429864	5.859375	6.597222	7.232704	7.514451	34,94624
	Model	0	5.6	9.7	13.6	17.4	20.9	24.1	26.9	29.5	32	24.2
VGS=12V	Measure	0	6.1	10.3	14.4	18,4	22.1	25.6	28.8	31.8	34.6	37.2
	ERROR%	0	17.24138	16.16162	15.32847	14.45087	13.59223	13.55932	14.01515	13.84083	14.74359	15.06024
	Model	0	4.8	8.3	11.6	14.8	17.8	20.4	22.7	24.9	26.6	28.2
Vgs = 10V	Measure	0	5.8	9.9	13.7	17.3	20.6	23.6	26.4	28.9	31.2	33.2
Vds		0	1	2	3	4	5	9	7	~~	6	10

A.2: Multichip Power Module (experimentally validated fully coupled multilayer Electro-thermal application)

The final validation step of the thermal modelling methodology was to use it in a fully coupled multilayer electro-thermal application. The multilayer structure used for the validation is a 1.7kV power module supplied by SuperGrid Institute [86]. The power module consists of MOSFETs and diodes inside a structure shown in Fig.A.2. 1. The MOSFETS are positioned adjacent to each other and separated from the diodes which are also adjacent to each other. Drain source input voltages are supplied via the large terminals at the side of the power module and conducted to individual MOSFETs via the busbar. The MOSFETs are individually controlled via the separate gate and source pins. While full description of the module is given in [86], the aim of this chapter is to explain the relevance of the power module to this project, explain the experimental procedure and validate the thermal model created in this project with the experimental results.

The relevance of the power module to this project is its use in generating experimental thermal maps. Unlike in section 4.6.2 where validation was done against FEA simulation of a generic power assembly structure, using a real power module provides the ability to perform experimental multidomain tests on a multilayer multichip power assembly structure – the chip(s) in the module electrically providing current to heat up the power devices, and the resulting temperature change modifying the temperature dependent parameters in the chip(s) which in turn modify the current output value from the device.





(c)



Fig.A.2. 1: (a) SiC Power module with close control board on top; (b) Its internal structure with the region captured by the thermal camera in tests

conducted in this project (c) Internal structure in (b) shown in more detail

Layer	Thermal Propert	Dimensions			
	Thermal	Density	Specific	(Length X	
	Conductivity		Heat	breath	
	(W cm ⁻¹ K ⁻¹)	(g cm ⁻³)		thickness)	
			(Jg ⁻¹ K ⁻¹)	(cm)	
Chip (SiC)	1.6	2.3	0.7	0.7 X 0.4 X 0.04	
Solder	0.5	12.0	0.25	0.7 X 0.4 X 0.01	
Copper (Top)	4.01	8.94	0.385	1.0 X 1.5 X 0.03	
Dielectric	2.85	3.26	0.82	1.0 X 1.5 X	
				0.065	
Copper	4.01	8.94	0.385	1.0 X 1.5 X 0.02	
(bottom)					
Solder (bottom)	0.5	12.0	0.25	1.0 X 1.5 X 0.02	
Baseplate	1.5	3.0	0.803	1.0 X 1.5 X 0.3	

Table.A.2.1: Material and Geometry properties in multi-chip module (Section of the module captured by the thermal camera)

The material properties of the different layers in the power module are highlighted in Table.A.2.1.

A.2.1 EXPERIMEMNTAL PROCEDURE – module preparation, thermal camera and

thermal camera code

The experimental procedure used in deriving the thermal maps involved the use of oscilloscope, Infrared (IR) camera, high voltage supply and gate drive to the power module. The set-up can be seen can be seen in Fig.A.2. 2. The procedure had been used by the author in creating temperature maps for the work presented in [87, 88] but had to be slightly modified to get temperature maps for the SuperGrid power module. The first step in the procedure was to ensure equal emissivity through all regions to be measured in the power module. The different layers in a power module

have different emissivity values therefore, measurements using an IR camera would give wrong values because of the different emissivity values in the module [89]. In order to prevent this effect, all regions to be observed (picture taken) in the power module were painted black with black coating (black paint).



Fig.A.2. 2: Experimental fast- imaging temperature measurement set-up

The next step was the calibration of the thermal camera to ensure that the results generated were valid. This was done by measuring the temperature at specific points in the bus bar region and chip region while comparing the results to similar measurements taken at the same time with a thermocouple. This measurement was repeated at different temperatures by placing the module on a hotplate, varying the temperature over the required application range and recording measurement from the thermal camera and thermo couple. An analysis of the recorded results showed that the maximum temperature deviation observed over the application range was 3K. This test showed the IR camera was calibrated to give reasonably accurate results.

Steady state testing was then conducted on the power module by connecting its terminals to a programmable DC supply and turning on one of the chips. A temperature increase of less than 20K was observed using a 14A DC current (the maximum DC current of a programmable power supply available in the Laboratory) into the power module for 30 minutes.

The reason for this low temperature increase is the relatively large size of the power module compared to the power module used in [87]. This valuable information from the steady state test led to adjustments in doing the transient test- the heatsink was removed and a short circuit test was performed in order to get reasonable rise in temperature over the test pulse.

Finally, the transient (short circuit) test was conducted using a High Voltage (HV) power supply. The test circuit is shown in Fig.A.2. 3. Test conditions were *Vgs* 18V, *Ids* 350A; ambient temperature 27°C; Time pulse- 200µs; bottom surface convection (natural convection). In this test, just one of the chips in the power module was turned ON in order to obtain a sizeable increase in temperature while maintaining safety standards in the laboratory.

The temperature pictures were collected from the thermal camera software and post processed using a customized post-processing code in MATLAB [46], [87]. Direct camera images can be used but the current capability of the thermal camera used in this work does not allow one to capture the legend together with the captured image together in a picture. Hence the use of the post-processing code to present both the captured images and the legend of the pictures.



Fig.A.2. 3: Test circuit schematic for the transient test

A.2.2 THERMAL CAMERA

The thermal camera is central to the experimental procedure detailed in the previous section. In this project, the thermal camera used is the Cedip titanium produced by FLIR [91] which provides 320 pixel X 256 pixel images. The camera operates on the principle of Infrared Thermography. The principle of infrared Thermography is based on the ability of objects to naturally emit radiation. The intensity and spectrum of the emitted radiation of the body is dependent on temperature [90, 91]. Thus, if the intensity of emitted radiation is measured (which the thermal camera does), the temperature at various point in the surface can be calculated. The intensity of the semitted radiation (spectral emittance) is related to temperature by the Stefan-Boltzmann equation

$$W = \varepsilon \sigma T^4 \tag{A.2. 1) [90]}$$

Here, *W* is spectral emittance (W/m³), ε is emissivity, σ is a constant (5.7. 10^{-8} Wm⁻ ² K⁻⁴) and *T* is the temperature. If ε (always between 0- 1) is known and *W* is measured, *T* can then be calculated. Different materials have different emissivity values (a body painted lack has an emissivity of 1.0 while SiC has an emissivity of 0.85). When measuring bodies with different materials such as a multichip power module, this must be considered otherwise the wrong result will be measured (see (A.2. 1)). In this work, this issue is resolved by painting black the regions to be measured in the power module.

The thermal images are captured by the camera through the use of a software called *ALTAIR* [91]. The software helps with camera pre-processing operations (i.e. tasks such setting of emissivity value, informing the camera to trigger on internal or external signals), processing operations (such as the giving instruction to the camera to commence taking pictures or videos) and post-processing activities (such as legend for the temperature images, use of data points at specific points in the image, conversion of videos to picture frames). The thermal camera and the ALTAIR software (labelled as IR camera Temperature display) can be seen in Fig.A.2. 2.

A.2.3 THERMAL CAMERA CODE

The thermal camera has an internal trigger which is used to automate the rate at which the camera takes pictures (camera image frame rate). The maximum frequency that the camera can provide internally is 383Hz (2.61 ms) which is not adequate for transient power electronic testing. Thus, an external triggering of the camera is needed to be able to automate the triggering of the camera to take pictures. The external triggering solution must also trigger the gate drive to the chips in the power module in addition to triggering the camera to take pictures in order to achieve synchronization between the control of the chips in the module and the camera.

Synchronization is needed in order to know the exact time points at which images are taken during the test cycle. The solution used by [92, 93] was also used in this project. An Arduino microcontroller was used to generate the control signals for both the chips in the power module and the external trigger on the thermal camera. The Arduino microcontroller was programmed by the use of Arduino IDE platform software to be able to perform this function.

The initial draft of the software code was written by an ex-member of the PEMC research group. However, there were amendments to be made to be able to able to meet the demands of this project. There was also need to for the gate control and measurement code to be validated. The author of this thesis made the amendments to the code, did the initial validation and then worked with a summer placement student (a co-author in [87, 94]) to use the gate control code on simple test case studies.

The code is designed to take multiple measurements of fast occurring events e.g. short circuit. The code is very user friendly as the ON time, OFF time, measurement time, camera settling time and many other variables are easily amendable by the user. The code makes use of three pins- a start pin (controlled by a pushbutton) which starts the process, a gate drive pin connected to the gate drive circuit and a measurement pin connected to the external trigger port of the camera. The flowchart in Fig.A.2. 4 describes the algorithm of the code [87].



Fig.A.2. 4: Flowchart description of microcontroller control code



Fig.A.2. 5 : Sample gate signal for microcontroller control



Fig.A.2. 6: Arduino board (a), connection from Arduino to thermal camera trigger (b) and the external trigger connection point on the thermal camera (c)

To fully understand the algorithm of the code, consider a test gate signal to turn the power device on for 5µs and off for 4µs as shown in Fig.A.2. 5. Once the button is pressed, the gate signal ON time will be divided into equal number of steps (this number is set by the user). Two initial blank shots are sent to clear the memory of the camera to rid the camera of previously captured images that may still be present in the camera memory. For each step the gate signal value (ON- 5V or OFF 0.0V) is sent to the gate drive circuit, turning on the chip in the power module thus, enabling the transient test to be done. At the time step, a signal is sent to the external trigger of the camera which instructs the camera to take a picture. A delay is set for the camera to process the measurements and for the device to cool down. The process is then repeated for the next time step until pictures have been taken at equal time step for the measurement period (as set by the user).

Prior, to the use of the Arduino controller for the experimental validation of the power module, the code was validated using a transient test with a period of 5μ s and number of time steps selected as 6. This meant that between the beginning and the end of the test period there will be 6 images captured (the initial 2 blank shots

are not part of the 6 images) with a time step of 1 μ s (i.e. $\frac{5\mu s}{6-1}$). The microcontroller signals were observed on an oscilloscope to ensure that the output signals to the gate drive and thermal camera external trigger port occurred in the right sequence as programmed by the code.

Validated microcontroller results for 3 time steps based on the test conditions mentioned above are shown in Fig.A.2. **7**. The blue signal is the gate drive signal and the orange signal is the measuring signal- i.e the external trigger to the thermal camera to take pictures. One can observe in the three pictures , a change in the measuring signal relative to the gate signal . This validates the description given earlier of what the code is intended to perform i.e take measurements at different points in the power module (the test object) in order to obtain temperature maps.



Fig.A.2. 7: Validation of microcontroller signals to be used for experimental validation of the thermal model

A.2.4 STEADY STATE EXPERMINATAL VALIDATION

The first step of the experimental validation was to observe the capability of the thermal model in steady state electrothermal simulation. The test condition was *Vgs* 16.4V, DC current of 14A, ambient temperature of 27°C (300K), natural convection at the Top, sides and bottom with a cooling rate of 10W/m²K. Because of the size of the power module and the corresponding amount of power loss required to observe significant increase in temperature, no heatsink was used and only two chips were turned on. Although the standard unit of temperature used through this project is Kelvin (K), the results from the thermal model have been converted to °C in order to make comparison with the experimental results (the results from the thermal camera were obtained in °C) easier. The constant mesh structure used to discretize structure used to discretize the region in the power module observed by the thermal camera is an X - Y - Z 11 -11 -16 mesh (a maximum of 1936 FDM equations to solve) in Fig.A.2. 8. The moving mesh step result is not shown here because there is little change in temperature with respect to time in steadystate conditions.

The Experimental result and the constant mesh step (VHDL-AMS solution) can be seen in Fig.A.2. 9. A good match is observed in the maximum temperature recorded with both results having maximum temperature around 49°C. The scale of the legend of the pictures in Fig.A.2. 9a and Fig.A.2. 9c are different because the experimental result captures the temperature at the other aspect of the power module such as the casing (the right edge of Fig.A.2. 9a) which is not part of the discretised structure in the VHDL-AMS model (Fig.A.2. 8) because it is not of importance to the usability of the methodology developed in this project. However, it remains possible to do comparison between the experiment and VHDL-AMS results based on the legend for their respective images. It can be seen from Fig.A.2. 9c that the VHDL-AMS model is able to capture the spread of temperature across other regions in between the chips (the chip region is demarcated with the red box in Fig.A.2. 9a) and in other regions in the power module. At steadystate, the heat spread to copper region around the chips in the VHDL-AMS model as seen in the experimental result can be observed. During the heating-up phase to steadystate, it was observed that the chips did not heat up uniformly (i.e. temperature spread across the chip was not uniform). However, on reaching steadystate, the heat spread across the chip became uniform. The result shows the ability of the VHDL-AMS model to be produce matching result for multi-chip and multilayer structures (such as a power module).



Fig.A.2. 8: constant mesh step discretization of Power module for steadystate test





Fig.A.2. 9: Thermal maps- experimental result for steady state testing (a)post processed (b) raw camera data (c) VHDL-AMS constant mesh step model result

To validate the thermal model in a transient simulation the short circuit test setup (

A.2.5 TRANSIENT EXPERIMENTAL VALIDATION

Fig.A.2. 3) was used. The test conditions were Vgs 18V, ambient temperature of 27°C, natural convection at the Top, sides and bottom with a cooling rate of 10W/m²K. Because of the size of the power module and the corresponding amount of power loss required to observe significant increase in temperature, no heatsink was used. Unlike in the steadystate simulation where 2 devices were turned ON, to generate significant increase in temperature while remaining within safety limits of current in the laboratory, only one chip could be turned on. With only one chip turned on, the multilayer accuracy and simulation speed capability of the VHDL-AMS thermal could be verified for one chip. However, this provided an opportunity to

observe if there were any notable multichip effects in transient operation between a chip that is ON and an adjacent chip that is OFF throughout the operation.

The constant mesh step structure used to discretize the region in the power module observed by the thermal camera is an X - Y - Z 11 -11 -16 mesh (a maximum of 1936 FDM equations to solve) shown in Fig.A.2. 10.

The thermal maps at the 200µs time point can be seen in Fig.A.2. 11. Fig.A.2. 11a shows the post-processed experimental result while Fig.A.2. 11b shows the image directly captured from the camera. One can observe that most of the temperature rise at this time is concentrated around the chip region. The temperature rise on the chip is non-uniform. While there are "patches" in the chip region which show significant temperature rise, there are other regions (e.g. the top left region of the chip) with very little temperature rise. Although this effect has been attributed to the design of the chip, it is also possible that regions on the chip with the bond wires directly above them record lower temperature values because the bond wires prevent infrared rays of the camera from reaching the surfaces directly under them.



Fig.A.2. 10 : mesh discretization of Power module for transient test

The temperature at the other regions outside the chip region (chip region is demarcated by the red box in Fig.A.2. 11a) experience very little temperature rise above room temperature clearly indicating that most of the heat flux is concentrated around the chip in transient application. The VHDL-AMS solution (Fig.A.2. 11c) is able to get a good match with the experimental maximum junction temperature. However, it struggles to get the non-uniformity of the temperature rise in the chip region.







Fig.A.2. 11: Thermal maps for transient test at the 200µs time point (a) Experiment (post-processed); (b) Direct image from camera (c) constant mesh step results.

A speed and accuracy comparison for the experimental results and the VHDL-AMS thermal results is summarised in Table.A.2. 2. The constant step mesh discretization has 1936 equations (X - Y - Z nodes of 11 – 11 – 16 respectively). The constant meh step solution provides good matching with the maximum temperature experimental results.

METHODOLOGY	ACCURACY	SIMULATION TIME	
	Tj (middle of	Minimum	(seconds)
	MOSFET)	temperature i	n
		the chip region	
	(at time 200µs)		
	°C		
EXPERIMENT	55	28	-
CONSTANT MESH	53	53	86

Table.A.2. 2: speed and accuracy cor	nparison of s	olution met	thods
--------------------------------------	---------------	-------------	-------

The constant mesh step results produce a maximum chip temperature close to the experimental results. However, due to the short time of the test and the way the power loss is applied in the thermal model (uniformly on all nodes), there is very little temperature gradient across the chip layer. With the constant mesh model producing close matching junction temperature, the moving mesh algorithm would provide little benefit in this simulation. The VHDL-AMS thermal model does not capture the patches observed in the experimental results and are better suited to helping power electronic designers to place chips in a power module or with selection of materials for designing the power module.