A Practical Investigation of Wideband Impedance Based Fault location Technologies

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Abstract

This thesis presents a thorough investigation of newly developed impedance-based estimation techniques that use the fault generated transient in order to locate faults in Integrated Power Systems (IPS) or Microgrids such as those existing in modern ships and aircraft. The methods studied use the high frequencies generated by the fault.

Two new fault location techniques are investigated. A double-ended and a single-ended technique. The double-ended technique needs the voltage and current measurements from two ends of the protected cable. The single-ended technique needs the measurements from only one end. The double-ended method uses a simple algorithm, and it has a high accuracy. However, the technique has no ability to locate the fault on any tapped lines. The technique is demonstrated using simulation and experimental investigation. The single-ended technique needs assumptions to be made and requires an iteration process to minimise the error caused by the assumptions. This method is able to estimate the fault distance on the main cable or tapped lines. However, it has no ability to discriminate between the two possible fault locations. The simulation tests have shown an excellent result while the experimental tests have shown that the technique is adversely affected by shape of the fault transient, and therefore a modification to the single-ended method is proposed and validated, to address this issue.

The advantages and limitations of both techniques are presented using different system conditions. The advantage of combining both methods in order to locate a fault on a tapped line is presented. A major limitation is the effect of a high number of tapped loads which require compensation. Therefore, both techniques are developed to consider tapped load compensation. Both the simulation and the experimental results validate the proposed changes. Furthermore, the addition of an inverter-based Distribution Generation (DG) has a limited effect on both techniques. It is shown that a DG source supplying 50% of the system load increases the error by 4% in the worst case.

Acknowledgement

I would like to thank all those who have helped me through the past four years.

In particular, I would like to express my gratitude to my supervisors: Professor Mark Sumner and Professor Dave Thomas for their guidance, support and inspiration in every stage of my Ph.D. work.

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CONTENTS

LIST OF FIGURES

LIST OF TABLES

Chapter 1 - Introduction

1.1 Introduction

Microgrids can be considered to be one type of Integrated Power System (IPS) which consists of multiple sources, a distribution network, and multiple loads. Moreover, it can be operated as a grid-connected "independent" subsystem or intentionally in islanded mode utilizing smart management and control (interface-capable and coordinated system, with automatic protection and reconfiguration features) [1].

A typical architecture of a low voltage microgrid is shown in Figure 1-1. The system is composed of several renewable energy sources (RES) such as photovoltaic panels, wind turbines, and thermal energy plants all in the form of distributed generation (DG) [2]

In recent years, increasing attention has been paid to the implementation of microgrid systems because of the many advantages both from the perspective of users and from the perspective of power utility supplier [3] [2]. For example, network power quality, can be achieved by employing microgrid concepts when connected to the grid [2] [4]. From the perspective of the electric utility provider, the benefits of microgrid implementation with distributed micro-generation include the ability to reduce the power flow on transmission lines which results in a system cost reduction for additional power. Furthermore, the load on the grid can be reduced by eliminating the problem of meeting the electricity needs from central sources as well as helping in network maintenance in the case of faults [2].

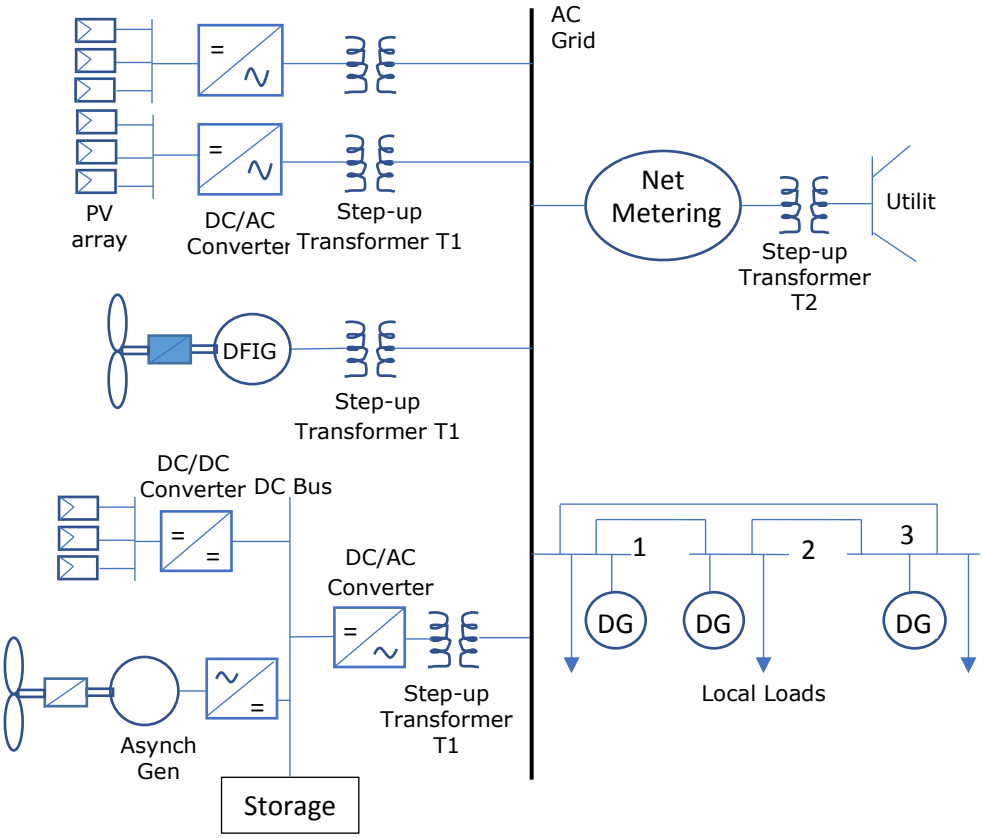


Figure 1-1 Architecture of AC microgrid

The electrical distribution system of transport systems including the emergence of More Electric Vehicles (MEV) [5] can be considered to be a specific application of microgrid concepts, especially for ships and "more electric" aircraft. Modern MEV systems are now being used in aircraft (for example the Boeing 787), land, and marine vehicles (e.g. UK Navy Type 45 Frigate) as they offer advantages such as high efficiency and survivability. In comparison with traditional vehicles systems, MEVs utilize the electrical system instead of mechanical, hydraulic, and pneumatic systems to optimize the vehicles' efficiency, emissions, performance, and reliability [5]. As a result, larger capacity and more complex configurations of electric power distribution system have been implemented to facilitate the increasing electrical demands in MEV power systems [6].

A typical configuration for an MEV system is shown in Figure 1-2. The electric loads and the mechanical loads receive their power from the power supply bus. The supply bus receives the electric power generated by the generators, fuel cells, and energy storage units (e.g. batteries). Different loads and power supplies can be connected by distribution cables and interface equipment using power electronic converters.

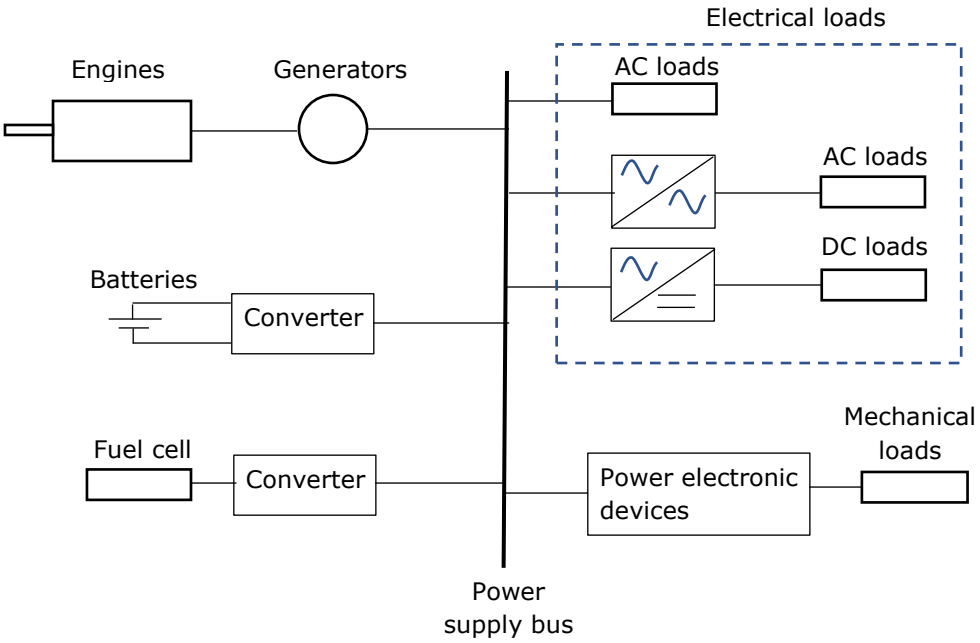


Figure 1-2 Typical configuration of MEV power distribution system

Using this concept, the traditional mechanical propulsion system is replaced by the electric propulsion system [7] [8] as shown in Figure 1-3 in order to reduce noise as well as to enhance system efficiency and decrease CO2 emissions. However, the system survivability in the presence of electrical faults is very important for the MEV system. Hence, it is required to design a fast and precise fault location technology in order to quickly recover the system and create a robust system for the vehicle's Integrated Power System (IPS).

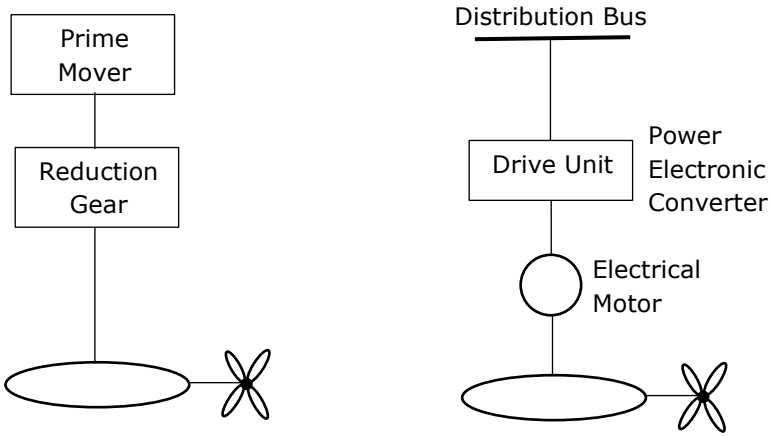


Figure 1-3 Propulsion system

Short circuit faults can cause overheating or damage to a power system's equipment due to the flow of a large fault current. In transport applications, faults can cause fatalities. Therefore, short circuit faults in microgrids such as marine power systems should be detected and located as fast and accurately as possible for fault removal and system recovery. There is more focus on fault detection and isolation in traditional protection schemes rather than accurate location. The detection of the fault in an IPS or MEV can be easily achieved by monitoring the system current, whilst the precise location of a fault is a more challenging task.

Traditional strategies for fault location have employed techniques to estimate the power system impedance at the system's fundamental frequency, and use this as a measure of the distance to the fault. However, for complex systems with power electronic loads and distributed generation, these techniques can easily fail. The DG supplied power adversely affects the estimation process if not compensated in these fault location techniques. Therefore, a new fault location technique is required that provides accuracy within a few metres of the faults as fast as possible and is not influenced by tapped loads or DG penetration. Finally, the authors in [9, 10, 11] devised a new wideband impedance fault location techniques which offer a high

accuracy and ease of use when applied to a simple IPS, and overcame some of the challenges in traditional techniques.

1.2 Aims and objectives of the research

This research aims to thoroughly investigate the "wideband" impedance-based fault location techniques developed in [9, 10, 11] in order to address the strengths and limitations of the techniques when applied to a complex low voltage IPS/Microgrids (such as those found in large ships) employing distributed generation (DG). The authors only experimentally validated the technique on a simple circuit composed of a 25V source, a 20m control cable and a linear/non-linear load.

The main research objectives are:

i. To develop and simulate a microgrid, which is composed of an appropriate architecture and representative loads and distributed generation.
ii. To determine an appropriate technique for fault location in the microgrid utilizing wideband impedance estimation methods with a minimum number of transducers.
iii. To investigate the effect of tapped loads and laterals on the accuracy of the fault location methods proposed in [9, 10, 11].
iv. To investigate factors affecting the application of the proposed fault location methods to a complex microgrid with additional renewable source between the two ends.
v. To investigate how impedance based fault location can discriminate between different possible fault locations when they have a similar path impedance.
vi. Validating the simulation work through experimental work.

1.3 Research Novelties and contributions

This section summarises the main novelities and contributions presented in this PhD work. Points 1-5 present the main novel contribution have been made in this works while Points 6-8 preset an imprtant evaluation to the the studied techniques:

1. Proposing a new Double-Ended Fault Location Technique (DEFLT) with tapped load compensation, section 4.5.
2. Proposing an enhancement to the DEFLT in terms of the number of required measurements. The new suggestion is to apply the DEFLT with only three measurements and ignoring the receiving end current, section 4.4.
3. Proposing a new modification to the Single-Ended Fault Location Technique (SEFLT) to address the issue of estimation error caused by a non pure fault transient (i.e. fault step contains some bounce or ripple), section 6.4.2.
4. Proposing a new combined method of SEFLT and DEFLT in order to locate faults on a multi tapped system using only measurements from two ends, sections 5.5 and 6.5.
5. Proposing a modified SEFLT with tapped and receiving end load compensation when Rf is Large, section 5.3.
6. Proposing a SEFLT with approximate of multiple tapped loads compensation which achieves a simple solution to the exact technique when the number of tapped load are more than four, as presented in seciton 5.2.2.
7. Investigating the influence of the inverter-based DG on the DEFLT.
8. Investigating the inlfuence of the inverter-based DG on the SEFLT.

1.4 Thesis structure

Chapter 2 reviews the background work related to electrical fault location, especially the impedance estimation approaches, travel waves and intelligent techniques. This chapter starts with reviewing the development of impedance estimation methods for a power system - both passive and active methods. Active method offers controllable transient and high signal to noise ratio for the measurement used compared to passive techniques which use system generated transients. The chapter reviews the application of impedance estimation for locating a fault within a power system, specifically in microgrid/IPS. Then, the influence of distributed generation on impedance-based fault location techniques is considered. The strengths and weaknesses points of the previous studies are discussed. Then, a short review of the application of travelling wave for fault location is presented. Finally, knowledge-based techniques are reviewed and summarised.

Chapter 3 introduces the wideband impedance based fault location techniques devised by Ke Jia in [9, 10, 11]. The chapter starts by introducing the Double-Ended Fault Location Technique (DEFLT) using a simple circuit with a method demonstration using a Matlab simulation. The second part introduces the Single-Ended Fault Location Technique (SEFLT) using a similar circuit. Finally, a conclusion summarises the required evaluation in order to address the strength and limitation of the two techniques.

Chapter 4 investigates comprehensively the DEFLT based on the higher harmonic content of the generated fault transient. A simulation based analysis of the technique is presented. Moreover, the effect of system noise, tapped loads, source impedance, and fault impedance are investigated. The advantages and restrictions of the technique are explored. Additionally, the

DEFLT is modified to include tapped load compensation in order to compensate for the load tap currents. Finally, the effect of an inverter-based DG on the proposed DEFLT is investigated through simulation. Different DG scenarios are presented and discussed.

Chapter 5 investigates thoroughly the SEFLT that uses the generated current and voltage transient measured only from the source end introduced in chapter 3. The method is firstly presented by simulation of a simple 50m length cable IPS. The method is further investigated for a more complex IPS by adding three tapped loads and tapped lines between the source end and receiving end. A compensated method is proposed to compensate the tapped loads imposed and this is verified through simulation. Moreover, the effect of the inverter-based DG on the proposed SEFLT is also discussed. Finally, a combined method of SEFLT and DEFLT is proposed to locate the fault on a multi-tapped distribution line.

Chapter 6 presents the experimental setup used to validate the double-ended and single-ended methods explored in chapter 3 and chapter 4. The experimental work shows the reliability of the double-ended technique and its accuracy in estimating fault distance on the main line in a multi-tapped line. The effect of tapped load on the accuracy is explored as well as validating the proposed method of tapped load compensation. The single-ended theory is also explored using the experiment setup, and some modifications are explored using the experiment system and a new method is proposed and validated to address non-ideal fault transients. Factors affecting the single-ended technique are discussed at the end. The combined estimation approach to locate fault in multi-tapped line system is then

demonstrated using the experimental setup. Finally, the influence of an inverter-based DG on the d-ended and single-ended technique is studied.

Chapter 7 present a summary of the research performed during the course of the thesis and the PhD. It summarises the main contributions and the strengths of the work performed in this thesis, as well as the limitations and weak points for applying the proposed technique in an IPS/Microgrids. Finally, a few recommendations for further research are presented.

1.5 Publications

The work in this thesis has been presented and published as follow:

1. Hayder K. Jahanger, David W.P. Thomas, Mark Sumner, "Combining fault location estimates for a Multi-tapped distribution line" IEEE PES Innovative Smart Grid Technologies Conference Europe (ISGT-Europe), Turin, Italy, 2017.
2. Hayder K. Jahanger, David W.P. Thomas, Mark Sumner, Christopher Rose, "Impact of an inverter-based DG on a double ended fault location method," *IET The Journal of Engineering*, vol. 2018, no. 15, pp. 1078-1083, 2018.
3. Hayder K. Jahanger, Mark Sumner, David W.P. Thomas, "Influence of DGs on the Single-Ended Impedance Based Fault Location Technique," IEEE International Conference on Electrical Systems for Aircraft, Railway, Ship Propulsion and Road Vehicles & International Transportation Electrification Conference (ESARS-ITEC), Nottingham, UK, 2018.

4. Hayder K. Jahanger, David W.P. Thomas, Mark Sumner, "An Investigation into the Robustness of a Double-Ended Wideband Impedance-Based Fault Location Technique," intention to submit to IEEE Transaction on Power system.

Chapter 2 – Literature Review

2.1 INTRODUCTION

In this chapter, a literature survey will be presented on the use and development of system impedance estimation and then its application to fault location, specifically in distribution systems and integrated power systems. It should be noted that techniques which employ measurement of voltage and current at only one node in the distribution system will be called "Single-Ended" methods. Those that require measurements at two different nodes, will be called "Double-Ended" methods. Moreover, the chapter will also explore other common fault location techniques such as travelling wave and Expert techniques.

1.2 Impedance estimation

The development of power system impedance estimation techniques has been considered over three decades and more [12]. Effective and accurate estimation of the source, line, and load impedance for a certain frequency range from a particular point of measurement is an important and challenging task. The basic principle of the impedance measurement technique is to apply Ohm's law to the measured current and the measured voltage data from a particular Point Of Measurement (POM) as shown in Figure 2-1 where Z_x is the impedance from POM to the fault location.

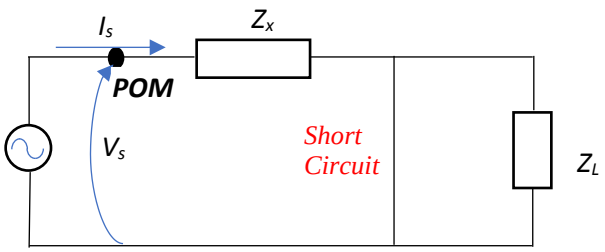


Figure 2-1 Electricity circuit with short circuit

This estimation of impedance can be made over a wide frequency range using the Fast Fourier Transform (FFT) of the signals as shown in (2.1)

$$\widehat{Z_x} = \frac{FFT(V_S)}{FFT(I_S)} \quad (2.1)$$

Vs, Is: are voltage and current measurements at POM while $\widehat{Z_x}$ is the estimated impedance between the POM and the short circuit location.

The impedance estimation method is considered one of the simplest, easiest, and most cost-effective techniques for fault location. The method can be characterized in four ways associated with **measured frequency** (Fundamental frequency or wide frequency range [13, 14, 15, 16, 17]), **excitation source** (Passive or active methods [18, 19, 20]), **system state:** (Online or off-line measurements [13, 21, 22, 23]) and the **data processing technique used** (For example, Fourier Transform (FT) [22, 23], Wavelet Transform (WT) [17], and Power Spectral Density (PSD) [24, 25]). This basic approach has been utilized and developed for fault location by dividing the estimated impedance by the known per-metre line impedance. The following sections will describe the active and passive approaches to impedance estimation.

2.1.1 Passive impedance estimation

Passive techniques utilize the transients generated during system operation such as load switching, capacitor switching, etc. to estimate the system impedance. (2.1) presents the simplest approach. Consider the circuit presented in Figure 2-2, when the load is connected to the circuit. The transient generated by load switching is captured and analysed over a defined frequency range using (2.2).

$$Z_L = \frac{FFT(V_S)}{FFT(I_S)} \quad (2.2)$$

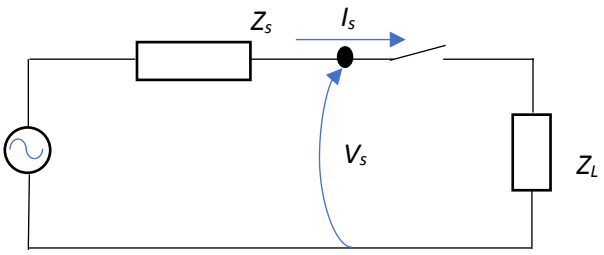


Figure 2-2 Passive impedance estimation using load switching

Research has been conducted to estimate system short circuit impedance using the passive approach. Pederson et al. [26] used the disturbance generated by a short circuit in order to estimate the circuit impedance. They used the Thevenin equivalent of the power system as shown in Figure 2-3 where Z is the equivalent Thevenin impedance of the short circuited system including the non-linear load, R is the load impedance, and U and I are the load voltage and current, E is the supply voltage.

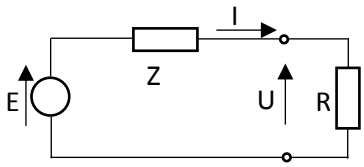


Figure 2-3 Simple model of short-circuit impedance

The calculation is performed using measurement at the fundamental frequency by applying (2.3) [26].

$$R = \frac{U_{50Hz}}{I_{50Hz}} \tag{2.3}$$

Although it is a simple approach to estimate system impedance, this approach is based on assuming that the high frequency of a transient has faded and that system regulation such as voltage control, is not affected by an event.

Furthermore, the researchers in [27] also utilised the Thevenin non-linear equivalent circuit to estimate the system impedance ($Z_s(f)$ in Figure 2-4) over a wide frequency range. Based on a system state change such as a load change, the authors estimated $Z_s(f)$ as (2.4):

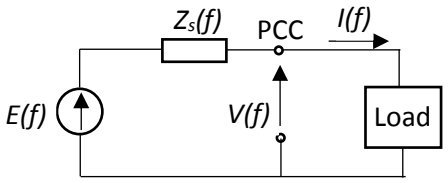


Figure 2-4 Thevenin model of the Power System presented in the Frequency Domain

$$Z_s(f) = \frac{V'_{(f)} - V_{(f)}}{I'_{(f)} - I_{(f)}} \tag{2.4}$$

Where $V_{(f)}$ and $I_{(f)}$ are the measurements for the original state (load1), while $V'_{(f)}$, $V'_{(f)}$ are the measurement for the second state (load2) [27]. Moreover, $E(f)$ and $Z_s(f)$ are assumed to be constant during the measurement. The main drawback of this technique is that the differences between harmonics in two load states are usually very small which results in a high estimation error.

In 2014, Eidson [28] and his team suggested a method that utilizes negative sequence measurements to estimate system impedance at the fundamental frequency. The negative sequence voltage and current measurement of a three-phase system and the equivalent circuit as seen by the load for one phase are presented in Figure 2-5.

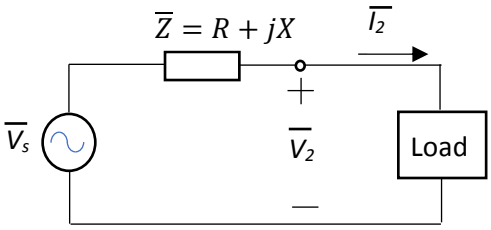


Figure 2-5 System equivalent circuit as seen by a load

Based on this circuit, and assuming $\overline{Z}$ is constant over sequential cycles k and $k-1$, (2.5) and (2.6) are derived [28].

$$V_s - \bar{I}_{2,k-1}\overline{Z} = V_{2,k-1} \quad \text{and} \quad V_s - \bar{I}_{2,k}\overline{Z} = V_{2,k} \tag{2.5}$$

$$\overline{Z} = \frac{\overline{V}_{2,k} - \overline{V}_{2,k-1}}{\bar{I}_{2,k} - \bar{I}_{2,k}-1} \tag{2.6}$$

where $\overline{Z}$ is the estimated system impedance. k is the present cycle and k-1 is the previous cycle. The main weakness of this approach is that the estimate is unreliable when the change in the real power at the load is very small. However, if there is a sufficient change, a reliable estimate is achievable. Therefore, it is important to set a proper power change threshold in order to correctly estimate the impedance.

In summary, the passive method is a simple and cost-effective method that could be utilized to estimate system impedance [23, 24, 25]. However, proper estimation requires a high Signal to Noise Ratio (SNR) and can only be used on a simple radial system as the method accuracy is highly affected by tapped lines, loads and distributed generation found in more complex distribution systems.

2.1.2 Active impedance estimation

The Active Impedance Estimation (AIE) approach unlike the passive method uses an externally injected signal to the system and then measures the system response from the injection point in order to estimate the system impedance. Therefore, in this section, a brief review regarding the development of active impedance estimation will be explored.

Rhode, et al [29, 30, 18], presented a power-electronic tool to inject a small sinusoidal current into the line at a certain frequency, and the line impedance is estimated at this injected frequency using the phase and angle of the injected current and the resultant voltage transient. Figure 2-6 shows the equivalent line circuit where a current signal with a frequency different to the fundamental voltage V_L is injected through an Isolation transformer of turns ratio (1:1). Current and Voltage transducers are used to measure the current and voltage disturbance resulting from the injected current. The measured signals are fed to a narrow-band filter in order to extract the frequency of interest and exclude the line and harmonic components.

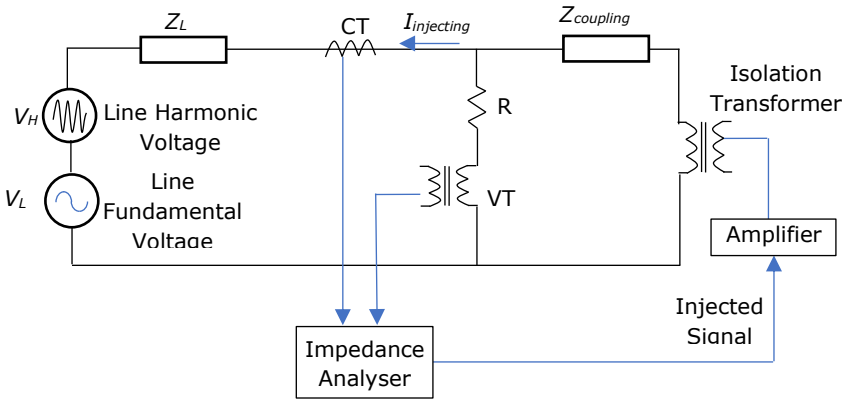


Figure 2-6 Active impedance analyser equivalent circuit

Using the extracted magnitude and angle of the measured voltage and current, the impedance analyser calculates the impedance using (2.7):

$$|Z_L(fI)| = \frac{|V_L(fI)|}{|I_L(fI)|} \tag{2.7}$$

where, $|Z_L(fI)|$ is the estimated impedance magnitude at the injected frequency, $|V_L(fI)|$ and $|I_L(fI)|$ are the measured voltage and current magnitude. The angle of the estimated line impedance is calculated as (2.8):

$$\angle Z_L(fI) = \angle V_L(fI) - \angle I_L(fI) \tag{2.8}$$

A group of researchers within the University of Nottingham developed an active impedance estimation based on a range of non-fundamental frequencies between 2000 and 2006 [13, 15, 20, 21, 27, 28, 29, and 30]. An electronic circuit was designed and used to control the injection of a small current disturbance to an energized power circuit as shown in Figure 2-7 [19]. The response of the system to the injected disturbance at the Point of Common Coupling (PCC) was measured and used to estimate the system impedance based on (2.1) [19]. This injection unit could be a standalone tool or embedded into some system component such as active shunt filter (ASF) or any power electronic interface.

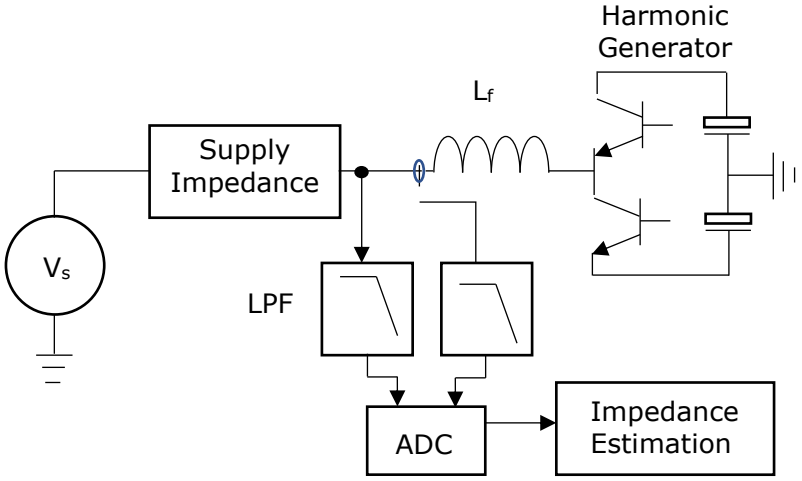
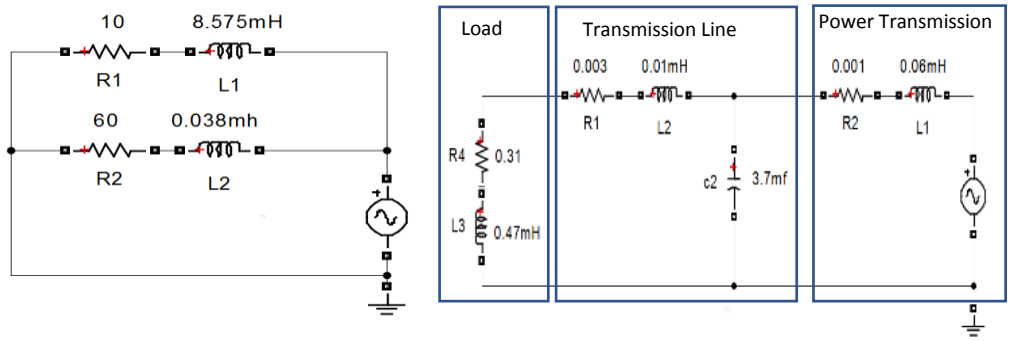


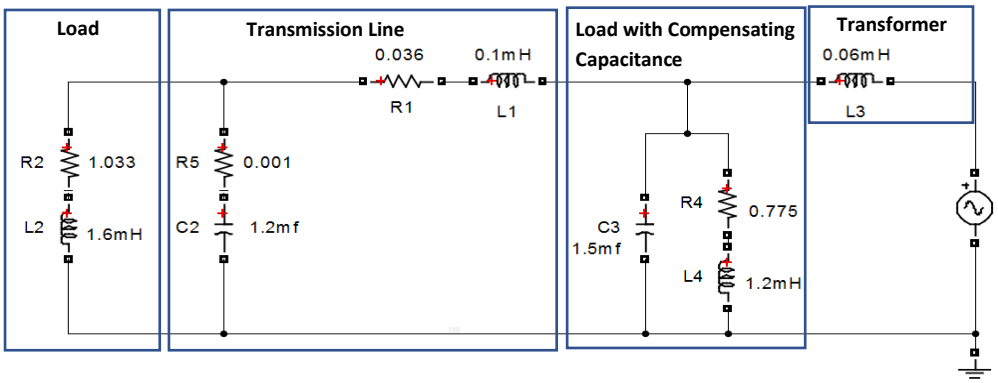
Figure 2-7 System with active injecting unit

A similar approach is used in [24] and [25], but utilizes the injection of a step voltage disturbance and was tested on different loads as given in Figure 2-8. The voltage step is injected at the load terminals and the current response is measured at the same point. A MATLAB simulation as well as experimental validation is performed. The captured data are firstly filtered using an anti-aliasing filter and then analysed in the frequency domain using the Discrete Fourier Transform (DFT) and the Power Spectral Density (PSD) transformation packages embedded in the Transfer Function Estimation (TFE) function of MATLAB. The system transfer function is estimated using

the TFE function. The measured input and output quantities using Walech's Averaged Periodogram method are used with the TFE function [24]. The TFE method divides the measured voltage and current into overlapping sections, the edge of the data section is then smoothed using a Hanning window, and finally, the output frequency resolution is improved by increasing the length of the data using zero-padding. The transfer function of the system can be derived by dividing the PSD of the input quantities P_{xx} (which is the square of the voltage magnitude at each frequency calculated from a DFT) and Pxy (which is the cross-correlation between the input and the output quantities). The correlation process before the DFT improves the SNR by filtering out the uncorrelated noise and in this particular case reduces the large absolute errors in the impedance estimate at the frequencies where the voltage and current signal strengths are low. The experimental impedance estimation results showed a high accuracy.



(a) Load Model 1 (b) Load Model 2



(c)Load Model 3

Figure 2-8 Load models for impedance estimation used by [21]

In [31], a three-phase fully controlled power converter is used to inject a voltage disturbance. The length of the voltage transient is extended to eight cycles in order to have a good resolution (6.25Hz) in the frequency domain. The experimental setup of Figure 2-9 was used to perform the analysis [31].

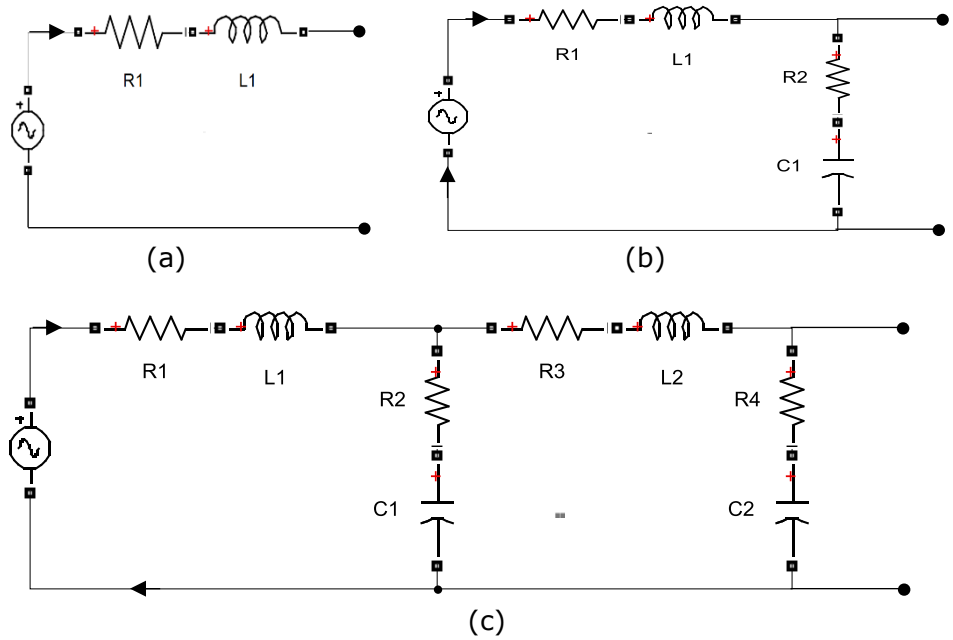


Figure 2-9 Experiment circuit setup for [28]

The three circuits presented represent different circuit representation of a length of cable. Figure 2-9 (a) represents only the source impedance while Figure 2-9 (b and c) include resonance caused by parasitic cable capacitance. A steady-state compensation is used to compensate for the supply voltage at the fundamental frequency. Eight cycles (160 ms) of the voltages and the currents were recorded in the steady-state, and then these are subtracted from the subsequent transient voltage and current. This procedure will eliminate the influence of the harmonics in the system existing before injection and also removes the edges of the steady-state waveforms so that no further edge smoothing windows (Hanning window or Harming window) is needed. The impedance is estimated using the Transfer Function Estimation (TFE) model and the DFT. The results presented showed that the

TFE is more suitable for a noisy condition compared to using the simple DFT equation (2.1). Although the system impedance and the resonant peaks can be identified accurately, this technique has the limitation that the supply voltage discontinuities caused by power electronic equipment (particularly capacitively smoothed rectifiers) will result in inaccuracy in the results and also the 160ms voltage disturbance injection may cause significant influence normal operation of the tested network. Furthermore, in a real system, the source harmonics can change from period to period and cannot be accurately compensated for.

An alternative injection approach was studied by the same group in [32] and [33] to overcome the limitation in the aforementioned approach using a long injected voltage transient. Therefore, they utilised a short duration injected current pulse operated by modifying the voltage applied to the coupling inductor of an Active Shunt Filter (ASF) [32, 33]. A 550 μs triangular current pulse was injected into the system, and the system impedance was derived from the measured current and voltage using (2.1). This approach works for both linear and non-linear load systems. This short-term injection method can be widely utilized in power systems because it can fully control the amplitude and the duration of the injected current spikes. However, the major drawback is when the injection unit is connected directly next to a voltage-source-type load, such as a capacitively smoothed diode bridge. In this case, the spike can penetrate the bridge, resulting in incorrect estimation.

A Continuous Wavelet Transform (CWT) was investigated in [17, 34] as an alternative approach for processing the data. The CWT needs a much shorter data window (5ms) compared to the DFT and TFE explored earlier in order

to give a comparable frequency resolution. The mother wavelet and the length of the window could be adjusted to suit the frequency range of interest. However, the application of CWT takes a longer processing time.

In 2007, Timbus [35] and his colleague suggested an approach to estimate power system impedance using power variation caused by a distributed generation (DG) at the point of common coupling (PCC). The approach uses the fundamental frequency component of the power variation. Active power is used to estimate the system resistive part whereas the reactive power is used for the inductive part of the impedance. They used the dq component of the measured voltage and current at the PCC. Based on Figure 2-10 and two operating conditions, (2.8) and (2.9) can be written:

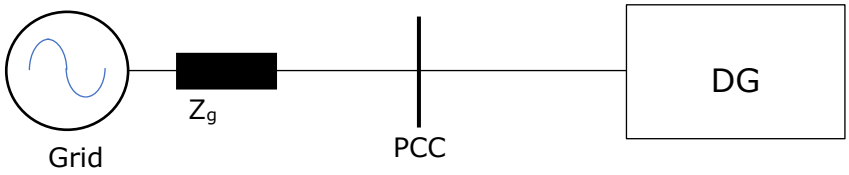


Figure 2-10 Grid with coupled DG as used by [32]

$$V_{pcc1} = V_s(1) - Z.i_{pcc1} \tag{2.9}$$

$$V_{pcc2} = V_s(2) - Z.i_{pcc2} \tag{2.10}$$

where V_{pcc1} and V_{pcc2} are the measured voltage at PCC for two different power conditions, V_s is the grid source voltage, i_{pcc} is the measured current at PCC at two different load power conditions. Therefore, the line impedance is calculated using (2.11):

$$Z = \frac{\Delta V_{pcc}}{\Delta i_{pcc}} = \frac{V_{pcc1} - V_{pcc2}}{I_{pcc1} - I_{pcc2}} \tag{2.11}$$

where ΔV_{pcc} and Δi_{pcc} are the voltage and the current difference between the two power conditions [35]. This approach is based on power variation delivered by the renewable sources. Hence, the delivered power could be

attenuated at the output of wind turbine due to variable wind speed which could adversely affect the accuracy of the technique. Photovoltaic (PV) systems should operate at unity power factor all the time, hence the reactive power oscillations necessary for line impedance detections should be small and for a short period of time. Thus, this technique is more suited for wind power application.

In (2017) [36] AlyanNezhadi and his colleague studied an approach that used an active impedance estimation for an energized system. They injected a low power and high-frequency signal into a noisy system, and the impedance is estimated as a ratio of the measured voltage and current signals. However, the energy of the injected signal in a noisy system must be adequate for an accurate estimation. Therefore, they proposed a denoising approach of the measured voltage and current signals using stationary wavelet, without increasing the energy of the injected signal. Figure 2-11 shows the approach in both active and passive systems. To overcome the problem of the source voltage in an active system, a set of two injections is used and the impedance is estimated using the following formula:

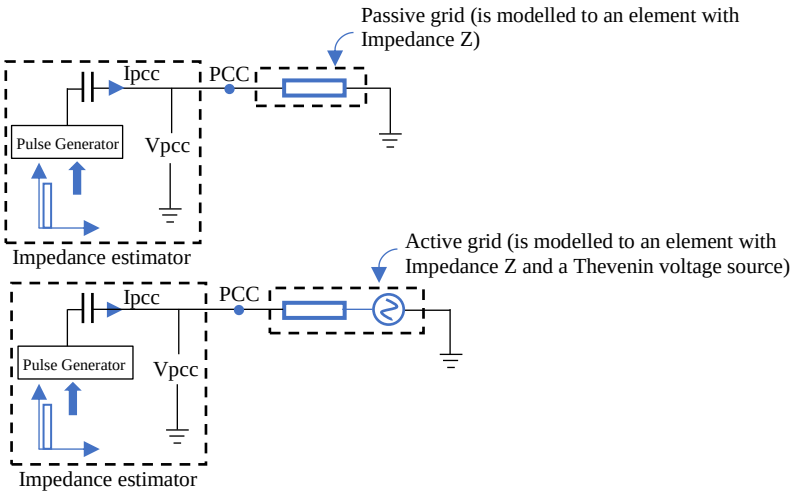


Figure 2-11 Schematic diagram of impedance estimation for passive and active grid networks [33]

$$Z_g = \frac{V_{pcc,n1}(\omega) - V_{pcc,n2}(\omega)}{I_{pcc,n1}(\omega) - I_{pcc,n2}(\omega)} \quad (2.12)$$

where $V_{pcc,n1}(\omega)$ and $I_{pcc,n1}(\omega)$ are the voltage and current signal of the first injection, $V_{pcc,n2}(\omega)$ and $I_{pcc,n2}(\omega)$ are the voltage and current signals of the second injection. ω is the injected frequency [36].

In conclusion, the active methods show a higher accuracy than the passive method. However, a few disadvantages may be encountered, such as firstly the extra cost due to the extra electronic components required. Secondly, the injected transient could influence the operation of the energized system by imposing undesirable noise on to the system, and increasing distortion and losses within the power system.

2.2 Impedance based fault location

In this section, the utilization of impedance estimation for fault location in microgrids and Integrated Power Systems (IPS) with be explored. It starts with a review of the passive fault location methods and then the active methods. Finally, it presents a conclusion on the advantages and disadvantages of each method.

2.2.1 Passive techniques

The transients produced by the switching of system components such as capacitor switching, load switching, power converter switching have been utilized for system impedance estimation. Realizing this concept, impedance estimation has been used for the estimation of a fault location in power systems (transmission and distribution). However, this section will consider

the application of Impedance-Based Fault Location (IBFL) in distribution networks which is covered by the many works summarized in [37]-[48].

In 2010 Krishnathevar and Ngu presented a new impedance-based method to locate faults in radial distribution systems (DS) with single-phase and two-phase laterals [37]. The method is based on measuring the fundamental phasor components of the voltage and current signals at the substation end only. The multi-estimation problem (i.e. there is more than one possible location) is solved using the magnitude of the fault current in the healthy phase. However, the proposed method cannot be used for a three-phase fault as the method is sensitive to load impedance [37]. They also present a method based on the fault current in the healthy phases to solve the problem of multi-estimation in single end impedance-based fault location [38]. Depending on the fault type, the fault current of the healthy phase(s) with a minimum index error is the correct faulted feeder. Though a solution to solve this problem has been presented in [38] by using the load current information in the non-faulted phases, the fault distance calculated becomes inaccurate if the load current in the faulted phases is neglected.

A study conducted by Liao (2014) for fault location in multi-source and multi-end distribution system uses the measurements at the substation terminal. He proposed a method that utilizes the concept of the bus impedance matrix for fault location. During the fault and at any bus, the voltage and current quantities can be expressed in terms of the bus impedance matrix of the faulted network, which is a function of the fault location. The sum of the magnitude of the fault currents of the healthy phases is obtained in the case of multiple fault location estimates. The smaller the computed value, the higher the associated fault location is ranked, and the more likely the fault location is the true one. However, in the case of faults that fall on two

identical laterals, the scheme is not capable of deciding which one is the faulted lateral, if only the local measurements are available [39].

The research [40, 41] by Daisy and Dashti (2015) proposed two steps to locate a fault in the power distribution system. Firstly, the impedance-based method is utilized to estimate the impedance from the measurement point (source end) to the fault location. The voltage and current at the sending end were used for this step. Secondly, in order to solve the multi-estimation problem, the researchers present a matching algorithm between voltage magnitude and phase difference at the measuring end for a system simulation compared with practical data. The closest match gives the true fault location. The proposed method showed high accuracy (less than 0.5%) for different fault distances and different inception angles (0-170 degree) [40]. However, to achieve this accuracy a high number of pre-simulated faults along the network with steps of 0.1km should be available.

The proposed method by Mirsaeidi, et al (2016) [42] used a Phase Measurement Unit (PMU) and Central Protection Unit (CPU) to protect and locate faults in sectionalized microgrids using positive sequence impedance. Voltage and current phasors (magnitude and their angle) were extracted by the PMU at both ends of each line section [42]. Their work depends on the communication system between the measuring devices and the CPU. Any failure in communication leads to protection failure. The technique needs to sectionalize the line to make the protection and section locating easier. It needs recording devices on both sides of each section.

Ramírez, et al presented impedance based fault location in distribution systems using measurements at one end [43] or two ends [44]. For the single-ended method, they proposed an iterative approach that works

section by section in order to reduce the problem causes by multi-tapped. For the two ended approach, the load flow was used to calculate the voltages and currents for each phase for both ends of the section. Then, using an impedance matrix and circuit analysis from calculated data, the location indices were calculated, and the average of these indices represents the fault location [44].

An analytical non-iterative impedance fault location method based on measurements made at one end (voltage and current) was studied in [45]. The methodology decomposes the three-phase measurements and circuit model to a single-phase equivalent circuit model applying a transformation formula. Then two second-order formulae are derived for a single line fault and other forms of faults. Finally, solving this formula will result in a pair of solutions where one of them represent the estimated distance. However, this methodology is only applicable to a single-sectioned circuit. Therefore, for a multi-section system (due to tapped loads or laterals) the process requires a load flow calculation to estimate the system loads in order to compensate for the voltage drop from the measuring station to the faulted section terminal. Another disadvantage of the proposed method is that an extra sensor is required on each lateral or tapped line to discriminate between possible locations.

Liu, et al in [46, 47, 48] suggested an approach that uses a two-end method for impedance estimation to locate a fault in a three or more terminal system. The approach requires a voltage measurement from each terminal in order to find a new sending end voltage for the faulted section. This new calculated voltage is used with the receiving end voltage of the section to find the fault distance. As a result, the faulted section is located and then the fault distance is calculated based on the estimated virtual voltage at the

section terminals. In summary, the approach needs synchronized multi-terminal measurements which is not a cost-effective method. Furthermore, the process is performed section by section; hence it is a time-consuming process. On the other hand, the approach can easily discriminate between possible estimated locations due to measurements from all the available terminals [48].

Jia, et al in [9, 10, 11] proposed a new single-ended and double-ended fault location methods that use the wideband frequency content of the fault generated transient. They introduced the single-ended method in [10]. The method requires a voltage and current from the source end and the voltage at the fault location is assumed as a pure step voltage. Then an iterative process is applied in order to minimise the error caused by the assumed step voltage at the fault location. The method is demonstrated in simulation and experimentally using a very low voltage system. The double-ended technique is introduced in [11]. This method requires a voltage and current measurements from two ends of the protected line and no assumption is made. The technique is validated in simulation and the same experimental system used for the single-ended technique. Both techniques showed a very good estimation accuracy. However, they only evaluated the techniques through simulation and low voltage (25V) experimental studies. They did not evaluate the technique under more realistic condition, i.e., higher power and voltage levels, tapped loads and lines, DG, and more realistic fault shapes.

Overall, these studies highlighted the need for more research in the area of the multi-estimation problem using impedance-based fault location methods in distribution networks with multi lines as well as the load current effect on the accuracy of the estimation.

2.2.2 Active techniques

These methods use the disturbance created in the system by an external source that injects a current or voltage transient through a coupling impedance and measures system response in order to estimate the impedance. This section will give a brief review regarding the application of Active Impedance Estimation (AIE) for fault location.

Mohanty et al. (2015 and 2016) [49, 50] proposed a portable off-line injection scheme for fault location in a low voltage DC microgrid based on the relationship between the attenuation constant of the damped probe injected current response and the fault distance. They added an extra impedance probe to solve the problem of close end (the end near the point of measurement) estimation error. They also considered the effect of noise on the injected signal and they showed it does not affect the accuracy, which remained up to 99.72%. However, the proposed technique requires first to de-energize the line and then manually connect the PPU to the line end to locate the fault. Furthermore, no experimental work has been performed to test the reliability of the method [49].

Park, et al. (2013) [51] presented a method to protect and locate the fault in a DC ring–bus microgrid. The location technique is based on Probe Power Unit (PPU) current injection to the isolated line and computing the fault distance-based attenuation factor in the injected current. However, their study showed that the methodology is affected by high fault resistance (1.5 Ω) in very short fault distances. Moreover, it was shown that the estimation result is quite sensitive to the accuracy of parameters and measurements, especially when there is not enough information due to the fast decay of the probe current [51]. There is also a high apparatus cost.

Wang et al. (2008) [52] presented a protection scheme for a zonal distribution system for marine application based on active impedance estimation (AIE). The method was based on injecting a transient pulse current and measuring the system voltage and current to locate the fault using Ohm's law. The result showed good accuracy with fault resistances between (0.1 – 0.6) Ω and was tested with a double line fault [52]. He also extended his work to consider more cases such as all loads connected and disconnected as well as an open circuit and short circuit fault with a Wavelet Transform (WT) as the processing algorithm [52].

In 2008, Wang et al., continued their study [53] by modifying the system to a two bus system with a Bus Interface Unit (BIU) which connects the load to either bus depending on the zone state. They tested the scheme with different loads; simple RL, capacitive smoothed rectifier, and a combination of both. As soon as a transient or fault occurs on the bus, the BIU will detect the voltage drop. The BIU then measures the system's impedance by injecting a very short transient current (40 A, 2 ms duration) onto the system and analysing the transient response of measured voltage and current. However, the presented method proposed injection in each zone, and they did not test the algorithm with Single Line to Ground (SLG) fault [53].

Jia, et al. (2012) [54] proposed an active impedance estimation method in order to locate a first earth fault in High impedance grounded (non-earthed source) IPS. They proposed to inject a 30μs and low magnitude current pulse through the source earth when a fault is detected and then measuring the current and voltage response at the source end. The fault is then estimated by dividing the frequency domain response of the voltage over the current and compare it to the line per-metre impedance. The study showed an

acceptable fault location accuracy. However, it is not applicable to the system when the earthing is not accessible. Additionally, the accuracy drops significantly when the equivalent impedance of the healthy phases is close to the faulted phase impedance.

Arevalo, et al. (2015) [55] presented a portable injection unit for online and offline fault location in a marine distribution system. The proposed method was tested on a power system with a twin DC bus and gave good accuracy for the de-energized system while the energized test showed acceptable accuracy (less than 3%) for frequencies between 400-800 Hz. The researchers applied two AIE units to the system and they captured the voltage and current transient with Fs = 50 kHz and 8ms widow length. The research developed a portable Current Injection Unit (CIU) composed of a full bridge rectifier to inject a triangular current pulse (1ms width) to the system and monitor the resultant transient voltage. The FFT was used to convert both signals to the frequency domain and using Ohm's law to compute the impedance which then separated the resistance and reactance. The reactance was used to locate the fault. The proposed scheme was applied to both a de-energized passive load and an energized system [55]. Another injection method was used to select the faulted feeder in a multi-feeder distribution system based on comparing the magnitude of the injected sinusoidal current signal in the faulted feeder with the healthy feeder [56], where the injected current in the healthy feeder will decay to a very low magnitude due to the transition impedance of lines. However, the study assumed the fault resistance was zero and for overhead lines which have branches or with uneven line parameters further study is required. Moreover; they only considered the SLG fault type [56].

In conclusion, despite the requirement for extra equipment to apply the AIE technique, it has been developed because of its controllable operation and high flexibility, and it shows good accuracy.

2.3 Influence of DG on impedance based fault location

There is an increasing demand for renewable energy sources (RES) such as inverter-based systems as solar or wind power. Therefore, this section will review the studies that considered the effect of DG on impedance based fault location technique.

Recently, research has been conducted to investigate the effect of synchronous DGs on fault location techniques in distribution systems or microgrids. Swagata Das, et al. [57, 58] investigated the effect of DG on the single-ended impedance-based method based on the radial system of Figure 2-12. The upstream and downstream faults from the DG were studied. The accuracy of the locating algorithm is greatly affected when faults occur downstream from the DGs. The percent error depends on several factors such as the magnitude of the DG and the distance of the fault to the DG [57]. Figure 2-13 presents factors that affect the accuracy of the estimated impedance and (2.13) explain these factors.

$$Z_{app} = \frac{V_G}{I_G} = mZ_{L1} + (m-d)Z_{L1}\frac{I_{DG}}{I_G} + R_F\left(\frac{I_F}{I_G}\right) \quad (2.13)$$

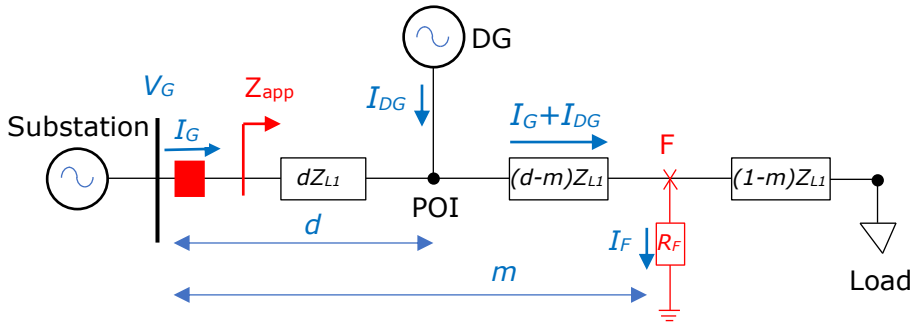
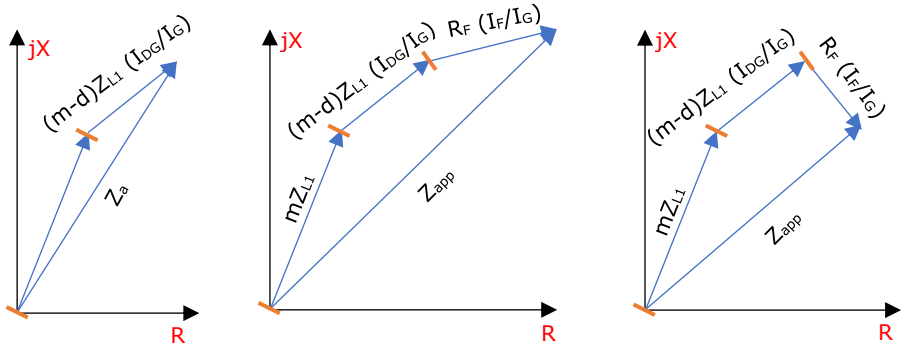


Figure 2-12 Radial Feeder with fault located downstream from DG [57]

where Z_{app} is the estimated apparent impedance from the measuring point to the fault location, V_G and I_G are the voltage and current measured at the substation terminal, I_{DG} is the DG injected current to the system. Z_{L1} is the positive sequence line impedance.



(a)R_F = 0Ω (b)R_F ≠ 0Ω, I_F leads I_G (c)R_F ≠ 0Ω, I_F lags I_G

Figure 2-13 Estimated apparent impedance [57]

Figure 2-13 summarizes the effect of Fault Resistance (R_F), and I_{DG} on the estimated apparent impedance using (2.13). Figure 2-13(a) shows the effect of the I_{DG} and how it leads to overestimating the Z_{app} by $(m-d)Z_{L1}\frac{I_{DG}}{I_G}$ when $R_F = 0\Omega$. On the other hand, Figure 2-13(b and d) show the effect of both I_{DG} and R_F and how it could lead Z_{app} to be overestimated when I_F (fault current) leads IG or underestimate the Z_{app}. It is evident that these two factors have a significant effect on the studied methodology.

Orozco-Henao and his colleagues in [59] studied the effect of the inverter-based DG in radial systems. They proposed a fault location method for power distribution networks in the presence of Inverter-Interfaced DER when these are working at current limit. The proposed technique uses a fault model of the inverter to consider its impact on the fault location. Thus, it is assumed that the inverter always operates in limiting current mode when a fault event occurs. It allows the estimation of its current contribution to the fault point.

The inverter equivalent model during the fault limitation mode is presented in Figure 2-14.

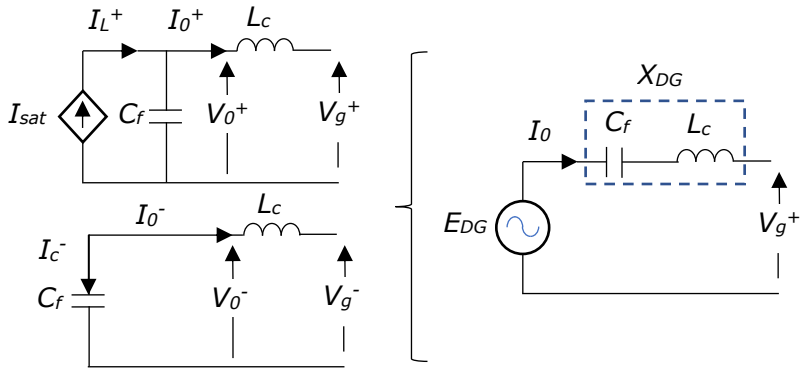


Figure 2-14 Equivalent circuit in phase components during current limitation operation [59]

where E_{DG} and X_{DG} are given by (2.13) and (2.14).

$$E_{DG} = \frac{1}{jwC_f} I_{sat} \tag{2.13}$$

$$E_{DG} = jwL_c + \frac{1}{jwC_f} \tag{2.14}$$

Two DG locations were investigated. Firstly, the DG is placed between the measuring end and the fault, and then the DG is placed downstream of the fault. The study showed that neglecting the contribution of the DG current or using an inaccurate electrical model will significantly influence the accuracy of the fault locator at the fundamental frequency.

In [60], the influence of synchronous DG on the distribution system is studied. It is proposed to modify the algorithm to include the effect of the DG at fundamental frequency [60]. A synchronous DG model is used in this study. The contribution of the DG to the load is calculated and included in the modified algorithm. The algorithm splits the system using a multi-section approach before and after the DG in order to locate the fault within the section as shown in Figure 2-15. The results show a reasonable accuracy.

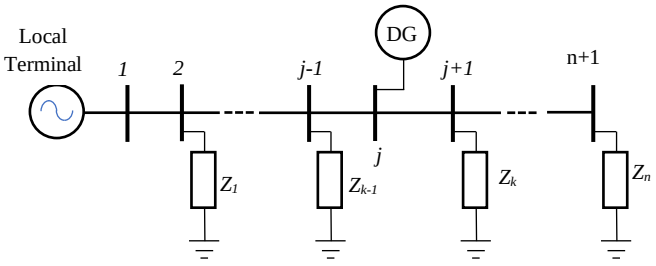


Figure 2-15 Distribution system with distributed generation [60]

A fault locating technique was proposed based on the voltage-sag between two points and the current measurement at the substation to estimate the fault distance [61]. The method derivation and process does not require any measurement from the DG due to the voltage measurements from both sides of the fault which represents the actual condition. The algorithm used is based on (2.16) and Figure 2-16:

$$x = \frac{A}{Z_0 . I_F} \tag{2.16}$$

A is given in (2.17):

$$A = \left(\begin{bmatrix} V_{S0fa} \\ V_{S0fb} \\ V_{S0fc} \end{bmatrix} - \begin{bmatrix} V_{S1fa} \\ V_{S1fb} \\ V_{S1fc} \end{bmatrix} \right) - l_0 . \begin{bmatrix} Z_{aa} & Z_{ab} & Z_{ac} \\ Z_{ba} & Z_{bb} & Z_{bc} \\ Z_{ca} & Z_{cb} & Z_{cc} \end{bmatrix} . \left(\begin{bmatrix} I_{Sfa} \\ I_{Sfb} \\ I_{Sfc} \end{bmatrix} - \begin{bmatrix} I_{Fa} \\ I_{Fb} \\ I_{Fc} \end{bmatrix} \right) \tag{2.17}$$

where x is the distance to the fault location, I_{Sf} is the sending end current during the fault, V_{S0f} the sending end voltage during the fault, V_{S1f} the voltage at the end of the line during the fault, l_0 is the line length, Z_0 is the line impedance matrix, and Z_{ij} is the mutual impedance matrix [61].

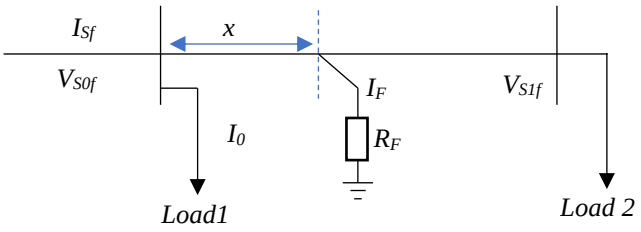


Figure 2-16 A simple model of the distribution network during-fault

The effect of inverter-based DG and synchronous DGs on the single-ended fault location technique was investigated in [62]. A few cycles of voltage and current before and after the fault are measured. The voltage and current signals measured during the fault are passed through a low-pass filter to eliminate their transient terms and only the fundamental frequency components are used. Two DG scenarios upstream and downstream are studied as shown in Figure 2-17 [62].

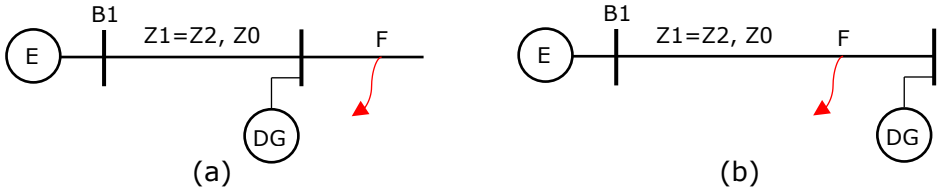


Figure 2-17 (a) DG Unit placed upstream (b) DG Unit placed downstream [62]

Based on (2.18), the fault distance is calculated from B1 to F.

$$D = \frac{R_{app}\, M - X_{app}\, L}{R_1\, M - X_1\, L} \tag{2.18}$$

where: $L = \frac{I_d\, I_{s1} - I_q\, I_{s2}}{I_s^2}$, $M = \frac{I_d\, I_{s2} - I_q\, I_{s1}}{I_s^2}$

Note that I_d, I_q are the direct and quadratic zero sequence current passing through the fault resistance. I_{s1}, I_{s2} are the positive and negative sequence current measured at B1. R_{app}, X_{app} are the resistance and inductance part of the estimated Impedance whereas R_1, X_1 are the positive sequence resistance and inductance of per unit of line length. Considering the contribution of the DG to the fault current, the study showed that the accuracy of the impedance-based method is affected. Moreover, they showed that the inverter-based DG has less effect than the synchronous DG due to a lower fault current contribution. In addition, the upstream scenario has a more negative impact than the downstream scenario.

Another study investigated a fault location algorithm with the effect of an ideal DG and a realistic DG using positive sequence impedance at fundamental frequency [63]. The case studied assumed that the DG was connected upstream of the fault as shown in Figure 2-18 and the measurements are made at the main source terminal. The contribution of the DG to the fault current was estimated assuming that the voltage across the DG current path is equal to the primary source current path voltage. The impedance to the fault location is estimated using (2.19).

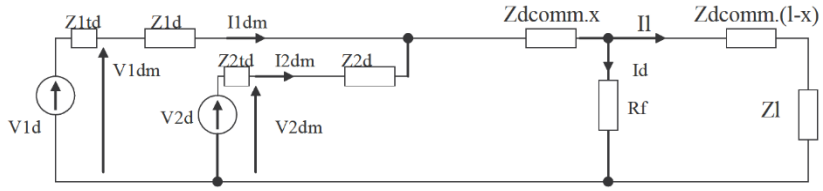


Figure 2-18 Direct sequence scheme for two sources network

$$Z_f = \frac{V1d}{\mathrm{I1dm}} = (Z1td + Z1d) + \frac{Z1td+Z1d+Z2t+Z2d}{Z2td+Z2d}.\ \mathrm{Zdcomm.x} \qquad (2.19)$$

Where Vd1 and I1dm are the voltage and current measured at source 1 terminal. x represents the fault distance and Zdcomm is the line impedance. The simulation results demonstrated that the DG affects the accuracy of the fault location when it has a common path with the fault seen from the measurement point. The results show that the error could reach as high as 42% when the DG contribution to the fault current is 67%.

Bretas and Nunes in their works [64] - [65] studied an extended impedance based fault location method that considered synchronous DG and it was compared to the traditional technique without DG. They developed an approach that considered the contribution of the DG to the fault current in order to compensate for the DG effect. According to Figure 2-19, the distance to the fault location (x) is calculated using (2.20):

$$x = \frac{V_{Sar} . I_{Fai} - V_{Sai} . I_{Far}}{M . I_{Fai} - N . I_{Far}} \quad (2.20)$$

where subscripts r and i represent the real and imaginary part of the voltage and current phasor, respectively. The real and imaginary part of the line parameters are given by M and N, which are obtained using (2.21), (2.22) [65]:

$$M = \sum_{k=\{a,b,c\}} [Z_{akr} . I_{Skr} - Z_{aki} . I_{Ski}] \quad (2.21)$$

$$N = \sum_{k=\{a,b,c\}} [Z_{akr} . I_{Ski} - Z_{aki} . I_{Skr}] \quad (2.22)$$

where Z_{akr} and Z_{aki} are the real and imaginary part of the line impedance matrix. I_{Skr} and I_{Ski} are the real and imaginary part of the measured current at S bus.

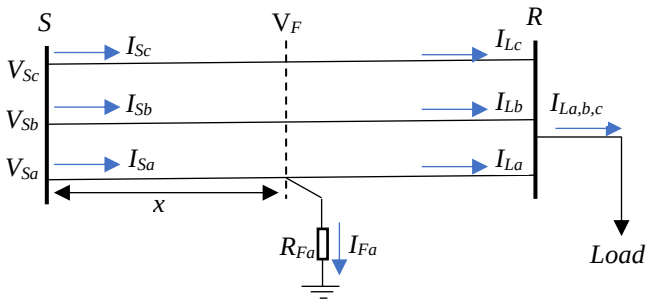


Figure 2-19 ground fault on line-a [65]

Bretas and Nunes considered the DG as an active source when the fault is upstream and passive when the fault is downstream of the DG as shown in Figure 2-20 . The DG is modelled as a 3-ph synchronous generator with a star connection.

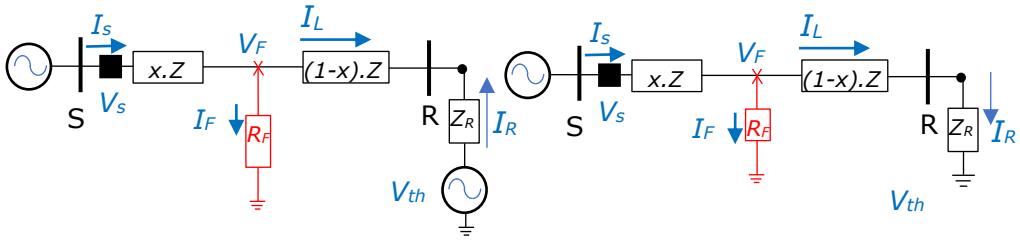


Figure 2-20 Distribution system with DG (a) Fault is upstream the DG (b) Fault is downstream the DG

Three DG power levels were considered, 10%, 20 % and 30% of the load demand as well as various fault types. The results showed an enhanced accuracy compared to the traditional method under a short circuit test, while under high fault resistance (10 Ω) the method showed lower accuracy in some cases than the traditional technique especially under 10% and 20% DG power level [65].

More recent research [66] studied the effect of a doubly-fed induction generator (DFIG) on the single-ended impedance-based fault location method at non-fundamental frequencies. A measurement from the DG was required in the proposed scheme. The equivalent circuit of Figure 2-21 is used to derive (2.23) which is utilized to locate the fault distance.

$$x_f + (1+\Delta 1)x_{1f} + (1+\Delta 2)x_{2f} + \cdots + (1+\Delta N)x_{Nf} = imag\left[\left(\frac{V_{pre-f}-V_f}{I_f}\right)\Big/ Z_{line\_p}\right] \quad (2.23)$$

where: V_f, I_f are the measured voltage and current at the POM, V_{pre-f} is the assumed fault transient at the fault location. Z_{DG} is the DG coupling impedance, Z_{line_p} is the line per metre impedance and $x_f - x_{Nf}$ is the distance of the line in each section. Furthermore, $\Delta 1 - \Delta N$ represents the ratio of the DG current to current measured at POM as given in (2.24):

$$\Delta 1 = \frac{I_{DG1}}{If}, \Delta 2 = \frac{I_{DG2}}{If}, \ \Delta N = \frac{I_{DGN}}{If} \quad (2.24)$$

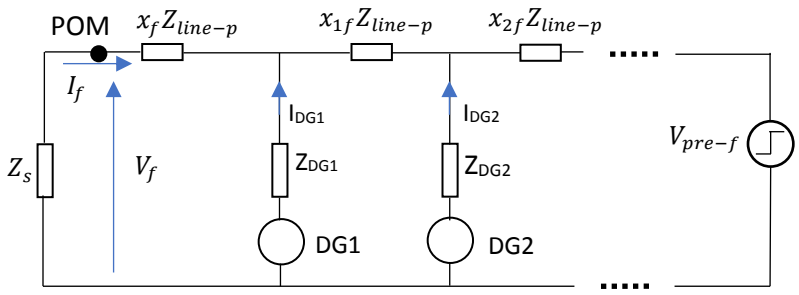


Figure 2-21 The distribution system with multiple DG in high frequency

The authors investigated the technique on a medium voltage distribution system with eleven 1.5MW DFIGs located throughout the system. Nine faults were randomly located at the beginning, middle and the end of the faulted line. A fault locator unit (FLU) is embedded in each DG to help increase the accuracy of the estimated distance using the FLU in the main terminal. The fault location results indicated a good accuracy. However, the technique searches for the fault location section by section in order to minimize the error created due to lateral connection and other DG.

The research presented in this section show that DG has an adverse influence on traditional fault location techniques based on estimation at a fundamental frequency while recently proposed methods require a measurement from the DGs. Therefore, further investigation is required into techniques that are not significantly affected by DG and requires no measurements from the DG.

2.4 Travelling wave techniques

The fault location techniques based on the travelling wave are well known for its fast and accurate fault location on transmission lines [10]. When a fault occurs on the transmission line, the voltage at the fault location suddenly drops. This change in the voltage causes a high frequency travelling waves at the fault point. The travelling waves propagate away along the transmission line in both directions from the fault location at speed close to the speed of light as shown in Figure 2-22. The fault distance is calculated based on measuring the wave and its reflection arrival times at one or both ends of the line using (2.25) [67].

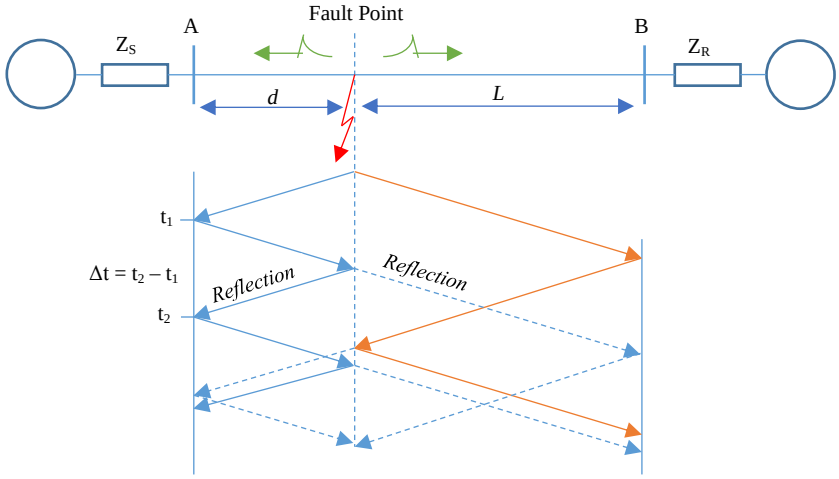


Figure 2-22 A Bewley Lattice diagram depicting a fault

$$d = v * \frac{\Delta t}{2} \tag{2.25}$$

Where, v is the speed of the travelling wave in the line. Δt is the time difference between the arrival of the first wave and its reflection. Equation (2.25) is for the single-ended techniques [68, 69, 70, 71]. If the double-ended technique is used [68, 72, 73, 74], (2.26) is used to calculate the fault distance using the arrival time of the initial wave at both ends. L is the

total length of the line and d is the distance to the fault measured from A end.

$$d = \frac{v*\Delta t+L}{2} \tag{2.26}$$

The double-ended techniques do not require a multiple reflections from the remote terminal of the line and it is more suitable for lines with complex configuration [70]. However, most of the double-ended techniques require a synchronised measurement from both ends. On the other hand, the single-ended techniques address the issue of synchronisation, and is cheaper to implement, which is suitable for simple overhead lines [70]. Moreover, laterals have adverse influence on the presented techniques because it imposes multiple reflection points which decreases the accuracy of the estimation fault location [68, 69]. All the presented techniques are been proposed for long distance distribution lines. Therefore, its application to a small distribution system, such as those exists in marine vessel IPS, limited because the accuracy is within hundreds of metres. Thus, a very high speed and resolution data acquisition units are required in order to increase the accuracy to within a few metres [9, 10].

2.5 Knowledge based fault location

The knowledge-based protection techniques such as expert systems [75] and Artificial Neural Networks [76, 77] use a heuristic method to solve the problem that could not be solved using a traditional algorithm. The knowledge-based techniques have the ability to cover complex structure networks, so they are used in distribution networks to cover a large portion of the system instead of covering single line sections using a traditional scheme.

2.5.1 Expert systems

Expert systems are intelligent interactive computer systems which act like human experts. The system configuration, geographical information, experimental cases, and rules were used to create pre-set data that is utilized to make a decision on the fault location [75]. However, the main drawback of this technique is the requirement of a communication system to gather information from the relays and the protection units throughout the network.

2.5.2 Artificial Neural Network (ANN)

Recently, research have considered the use of Artificial Neural Networks (ANN) for fault location in power distribution systems. The Artificial Neural Network (ANN) [76] is a computational network which has many nodes, connections, and layers based on the neural network of a brain. The ANN model has to be pre-trained according to different fault situations and modified to achieve the predicted results. Similar to an expert system, an ANN model contains details of the system information, but the ANN can self-learn after training without fixed rules. For example, a system contains N layers of nodes and connections with input from the first layer and an output from the last layer. The training procedure chooses nodes and connections to form different paths from the first layer to the last layer according to different fault situations; then the self-learning process can form its own paths. It does not have to be told a specific set of rules like expert systems but instead establishes its own set of rules based on the data it is trained with. Once sufficient training has been performed, the neural networks can make accurate (but not 100% accurate) fault predictions of fault locations under a variety of fault conditions and fault resistances [76, 77].

Chanda (2011) [78] presented a method for classifying and locating faults in the MVDC shipboard distribution system based on the transient information in the fault voltage and current. A sampled current was used as the input to the ANN classifier. Voltage and current were used as the input to the ANN fault locator. Depending on the fault type, an appropriate ANN fault locator is selected and tested to provide the location of the fault in per unit (percentage of the total length) [78]. Nevertheless, the proposed method has some limitations:

- Extensive data sets are required as an input to the ANN which represent different conditions from the healthy condition with different load values. For fault conditions, the fault location is varied from 0-1 Pu as well as the fault resistance (0, 2, 4, 6, 8 and 10) and three fault types.
- The maximum error occurs at the end of the line with high fault resistance.

In 2011, research by Yan, et al. [79], proposed a neural network (NN) approach to overcome the difficulty of multi estimation in multi-lateral Distribution systems (DS) using the Travelling Wave fault location method. Multiple simulation data from each branch were used to train the NN to make the decision on the faulted line.

Zhang Tong, et al. (2015) [80] proposed a Back Propagation NN to identify and locate the fault in active DS with Distribution Generation (DG) using the pattern of the voltage and current amplitude. However, the results showed that the error increases as the fault resistance increases as well as the work did not show the amount of data used to train the network [80].

Dehghani and Nezami (2013) also presented an ANN to locate a fault in a 34 bus IEEE non-homogeneous multi-lateral DS. A one cycle pre-fault and three cycles during-fault voltages, currents, and active power at the substation were used as input data to the ANN [81]. Data for different fault locations, fault resistance (0-50 Ohm) and the unbalanced load were considered. The complete amount of data used was 2366 measurements, 75% used for training and the rest for testing the network [81].

In conclusion, although the knowledge techniques can offer a good fault location accuracy in a various systems and fault conditions, the techniques require a large training data sets in various condition and point throughout the system in order to offer the required reliability. Any changes in the system condition requires new data set and retraining of the using intelligent technique.

2.6 Summary

The most common technique concerning the fault location in IPS/ Microgrid and distribution network have been considered, which include impedance based methods, Travelling wave methods and Expert techniques. The major focus was on impedance based techniques which was divided to passive active methods, DG influence on the impedance based techniques. The passive method utilizes the disturbance created by the fault itself, while the active method uses additional devices to inject a disturbance into the system in order to locate the fault. DG and laterals represent an increased challenge for the traditional methods that estimate the fault location at fundamental frequency (50 or 60) Hz. The lateral causes a problem for finding the correct fault path without measurements from the laterals. The current injection from the DG at fundamental frequency if ignored causes a high estimation error due its large magnitude compared to main supply, while considering it requires extra measurements from each DG.

The second common technique which is the travelling wave based techniques have been developed with accuracy within hundred metres. Therefore, its application to a small distribution system or IPS/microgrid, such as those exists in marine vessel IPS, is limited. Thus, a very high speed and resolution data acquisition units are required in order to increase the accuracy to within a few metres which add more complexity and cost. Furthermore, the lateral causes an issue for the travelling waves due to the number of reflections from multiple terminals. The last common techniques, ANN uses a pattern recognition and training data to locate the fault within the system. This technique requires a large amount of data with various fault condition and location throughout the system in order to train the NN so that it offers a high accuracy.

It is clear that the majority of the authors in the above literature were aware of the challenges in locating fault in an IPS /microgrid. They have focused on locating the fault in simple circuits. Therefore, it is crucial to investigate fault location in a more complex IPS/Microgrid as well as considering challenges such as how to discriminate between different fault locations when they have similar path impedance. Furthermore, considering the effects of tapped loads on the accuracy of any proposed method is also very important, and determining a reliable fault location with a minimum number of measuring devices represents a challenging issue. Finally, developing an impedance technique that is not highly influenced by inverter-based DG is of highly important in order to ignore the DG current and voltage measurement.

Finally, the authors in [9, 10, 11] only evaluated the proposed wideband impedance based fault location techniques through simulation and low voltage (25V) experimental studies. Therefore, the main aim of this work is to thoroughly evaluate the techniques under more realistic conditions such as:

- Higher power and voltage levels.
- Tapped loads and lines.
- DG in the system.
- More realistic fault shapes.

Chapter 3 – Wideband Fault Location Techniques

3.1 INTRODUCTION

In this chapter, the double-ended and single-ended impedance-based fault location techniques for Integrated Power Systems (IPS) will be reintroduced based on the work presented in [9, 10, 11], analysed, and demonstrated. Firstly, a simple circuit will be used to derive the fault location model. Secondly, factors that could affect the proposed estimation algorithm will be studied, for example, the magnitude of the fault resistance, tapped loads, measurement noise, the presence of tapped lines, and the influence of inverter-based DG will be studied. Finally, a double-ended method which neglects the receiving end current will be explored.

3.1 Double-Ended Fault Location Technique (DEFLT)

The impedance-based fault location technique based on measurements at two nodes within the power system (DEFLT) developed in [9, 11] will be introduced and demonstrated using a simple circuit. Figure 3-1 shows a single line diagram with a short circuit fault. The equivalent circuit at non-fundamental frequencies during a fault is presented in Figure 3-2. The supply source is considered a short-circuit at non-fundamental frequencies while the fault is represented as a transient voltage source at non-fundamental frequencies [82, 11, 9].

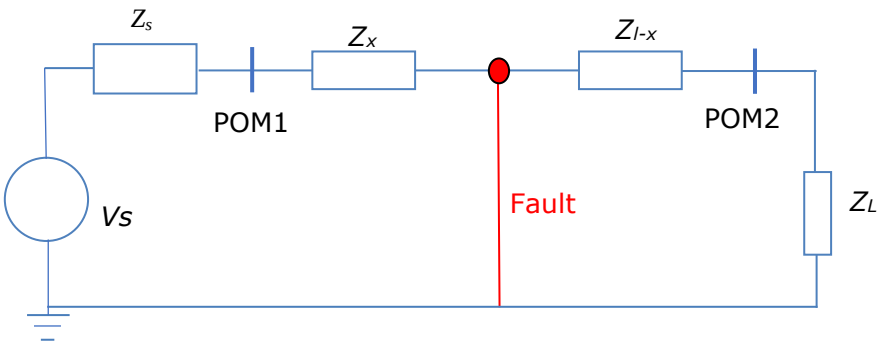


Figure 3-1Single phase circuit with a phase to ground fault

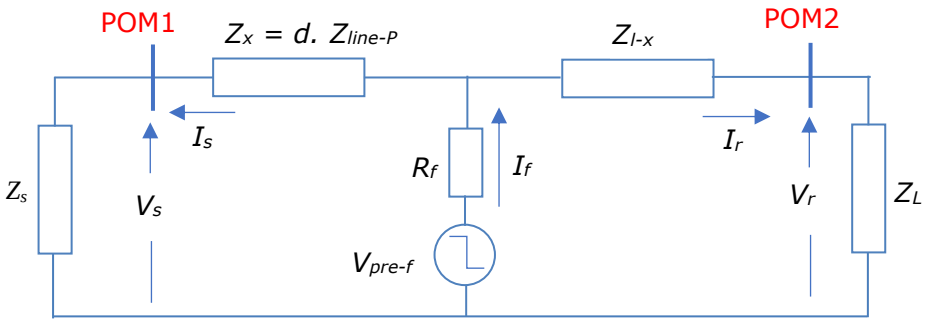


Figure 3-2 System at non-fundamental frequency during a fault: measurements at both ends

The fault creates a transient voltage (V_{pre-f}) at non-fundamental frequencies and R_f is the fault resistance. POM1 is the point-of-measurement at the source end, while POM2 is the point-of-measurement at the receiving end. Kirchhoff's Laws are applied to the measured voltage and current during a fault for the measurements at both ends of the line to calculate the impedance between POM1 and the fault (Z_x). Kirchhoff's voltage law is applied to Figure 3-2 to derive (3.1).

$$V_s + I_s.Z_x + I_f.R_f = V_r + I_r.Z_{l-x} + I_f.R_f \quad (3.1)$$

where V_s, I_s are the voltage and current measurements at the source end of the line and V_r, I_r are the measured voltage and current at the receiving (load) end. The total impedance of the line is $Z_l = Z_x + Z_{l-x}$. Rearranging (3.1) for Z_x, gives:

$$Z_x = \frac{V_r - V_s + I_r . Z_l}{I_s + I_r} \quad (3.2)$$

$$d = \frac{imag(Z_x)}{imag(Z_{line-p})} \quad (3.3)$$

The impedance between the fault point and source end is estimated using (3.2). The distance in metre (d) to the fault location can be found by dividing the estimated impedance by the known per-unit-length impedance (Z_{line-p}) of the line at each non-fundamental frequency using (3.3). The final distance estimate is then the average of all the estimates over a specific frequency range. However, the impedance is dominated by the reactance at high-frequencies; and therefore, the distance is calculated using only the reactance, and the resistance is neglected. Furthermore, (3.2) shows that the fault resistance information, as well as the knowledge of the load impedance or the supply impedance are not required by the proposed double-ended method.

3.1.1 Simulation Studies for the DEFLT

A model of a simple system was created using MATLAB/Simulink software. The single line diagram of the power system fault demonstrator at the 'Flex Elec' Laboratory-based IPS/microgrid at the University of Nottingham is shown in Figure 3-3 [83], while the simulated demonstrator is shown in Figure 3-4. The system consists of four sections with zone 1, 2 and 4 of 10m in length while zone 3 is 20 m. Each section is represented by lumped series resistance and inductance while the line capacitance is ignored due to the size and length of the cable used in the demonstrator. The current limiter and the load are also represented by pure resistance and inductance in series whereas the busbar and the power transformer are represented by a simple AC supply as shown in Figure 3-4.

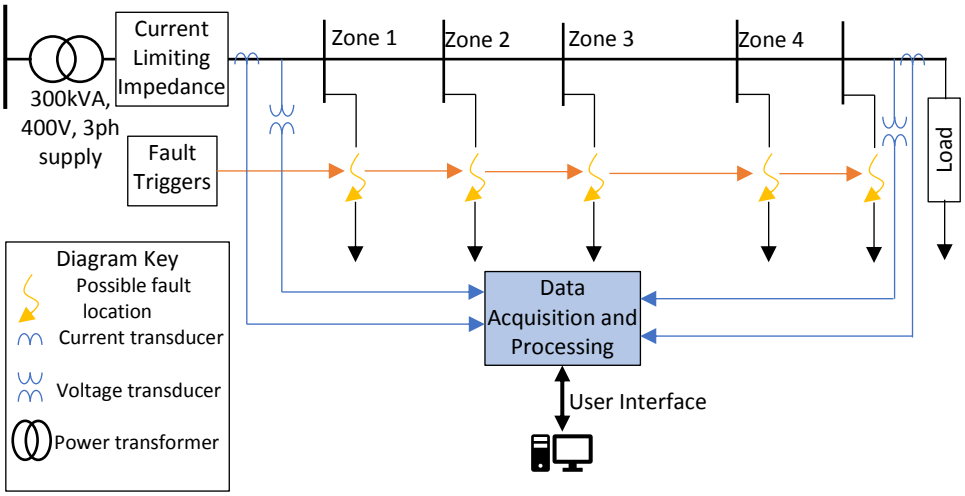


Figure 3-3 Fault demonstrator at the University of Nottingham

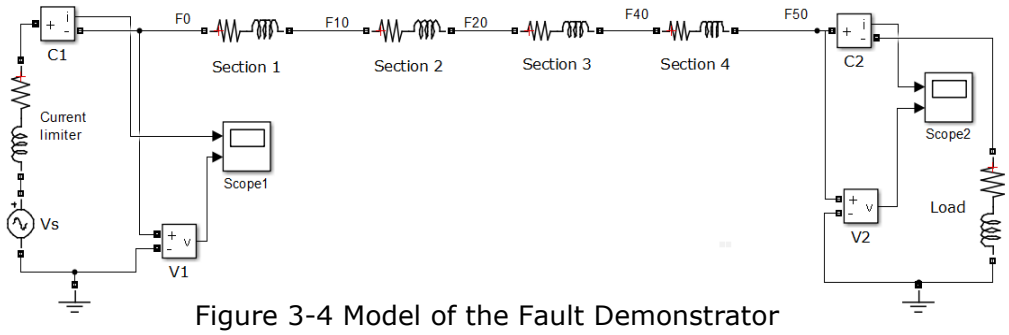


Figure 3-4 Model of the Fault Demonstrator

The per-unit-length resistance and inductance for each section are 1.15 mΩ/m and 0.82 μH/m [83], respectively. The load magnitude is (22+0.157j) Ω and the current limiting impedance is (0.5 + 0.0157j) Ω at 50Hz. Voltage and current transients measured at both ends, as shown in Figure 3-5, are captured for 10ms at a sampling frequency of 50 kHz. The signals are then processed by multiplying it with a Blackman window, which is shown in Figure 3-6, in order to remove the effect of the edges of the measured waveforms. The windowed signals are shown in Figure 3-7. Finally, a Fast Fourier Transform (FFT) is used to transform the time domain signals to frequency domain and these are then used in (3.2).

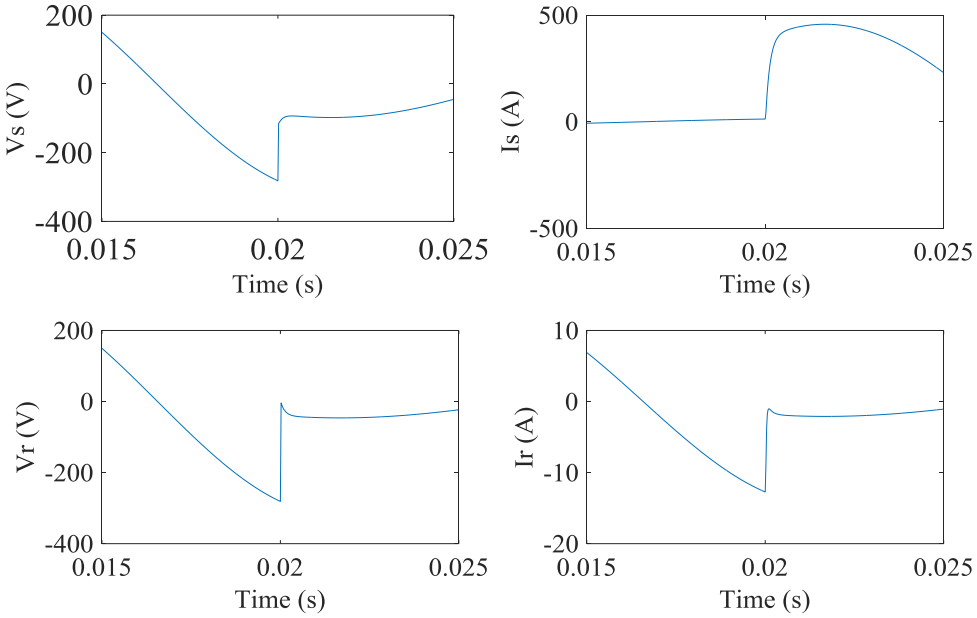


Figure 3-5 Captured signals from POM1 and POM2 in Fig. 3-4 during a fault

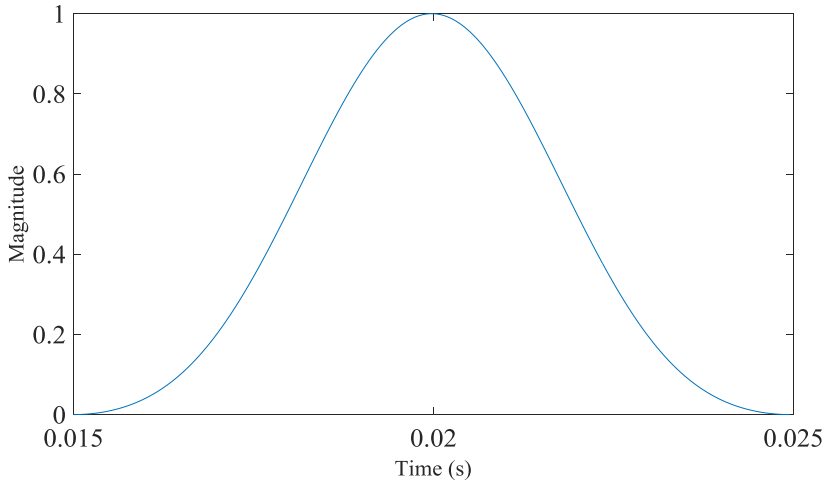


Figure 3-6 Blackman window

The frequency domain representation of these transients are derived using the FFT from the time domain signals and are shown in Figure 3-8 with a frequency range up to 5 kHz. Five locations have been selected to create a line to ground fault through a 0.1Ω resistance as marked in Figure 3-4: F0, F10, F20, F40, and F50. F0 represents a fault at the source end while F50 is a fault at the receiving (load) end which is 50m from the source end. The data window is selected so that the fault transient is at the centre of the captured window as shown in Figure 3-5. 5ms of pre-fault and 5ms of during-fault of data is utilized for the fault location algorithm. Figure 3-8

shows the frequency domain representation of the captured signals of Figure 3-5.

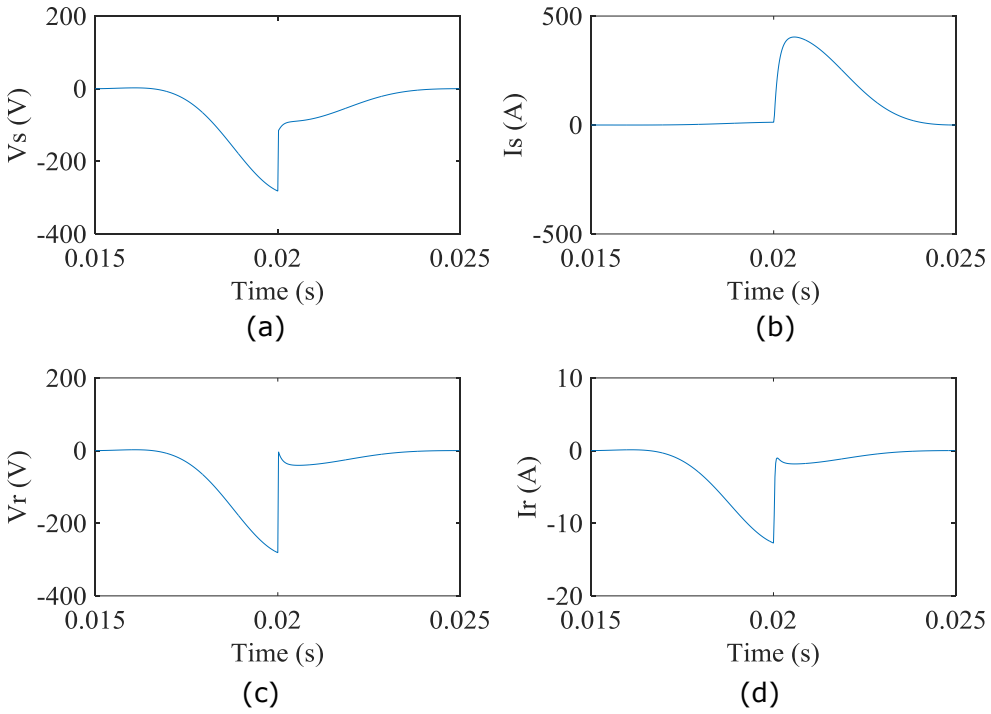


Figure 3-7 Blackman windowed data (a) source end voltage (b) source end current (c) receiving end voltage (d) receiving end current

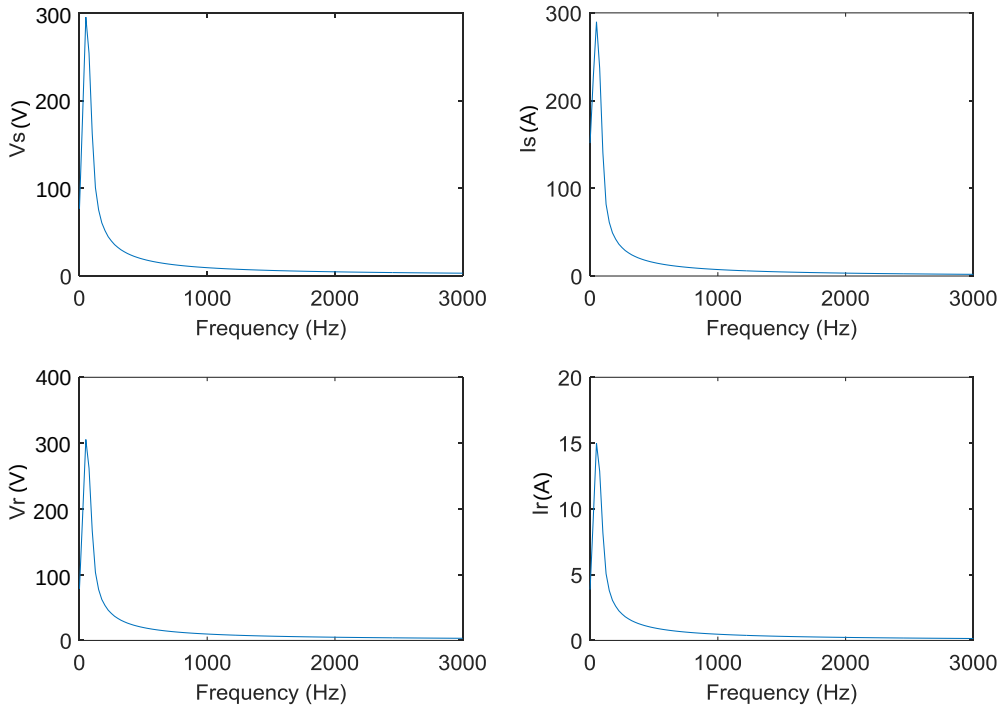
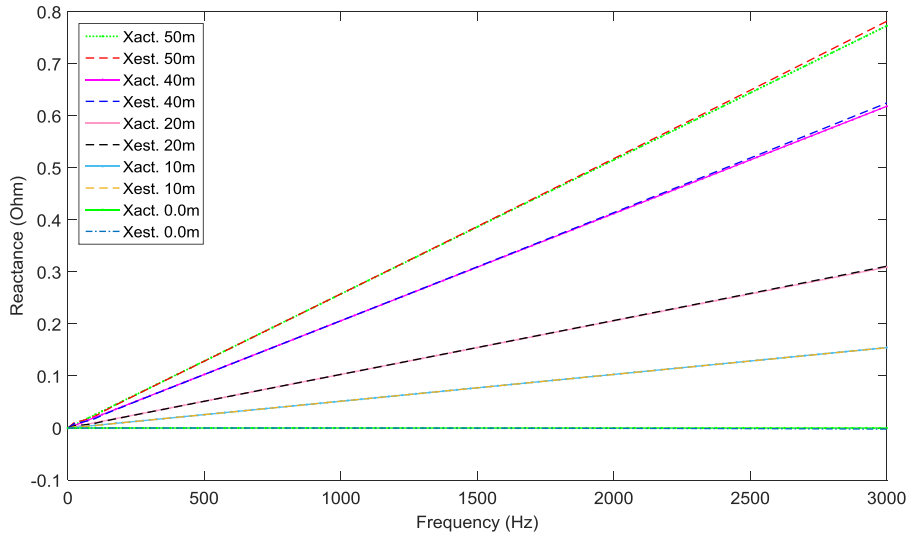
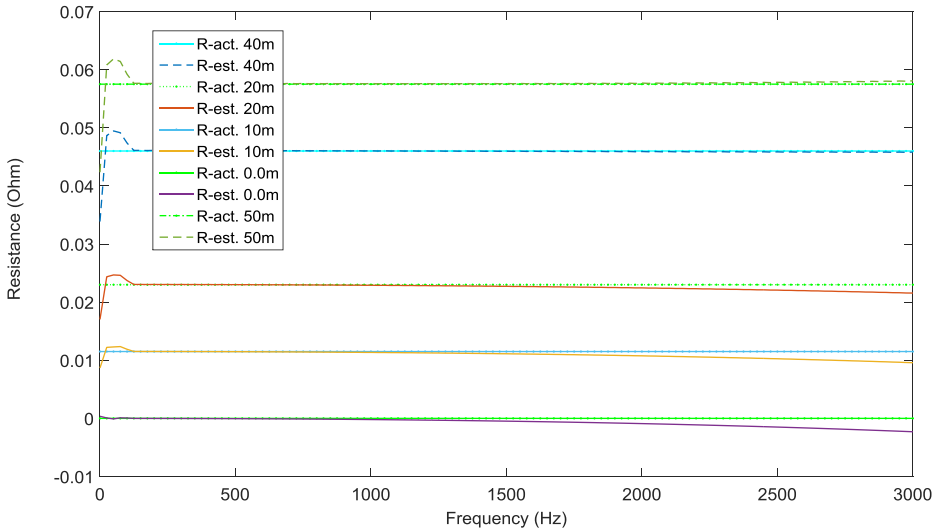


Figure 3-8 Normalised Frequency domain representation of the measured signals from sending and receiving ends

The impedance estimated for the five fault locations in the frequency domain up to 3 kHz is shown in Figure 3-9(a) which is the imaginary part while Figure 3-9 (b) is the real part of the impedance. These estimated magnitudes represent the value of impedance between the source end and the fault location at non-fundamental frequencies, which is Z_x as indicated in Figure 3-1. The solid lines represent the actual values used in the model (Xact.), while the dashed lines are the estimated values (Xest.) using the DEFLT.



(a)



(b)

Figure 3-9 Estimated impedance using DEFLT. (a) Inductance part of the estimated Impedance, (b) resistance part of the estimated Impedance

It was found that the technique regarding the reactance part shows a strong match between estimated and actual values in the higher frequency range up to 3000 Hz while the resistance shows poorer accuracy than the reactance in the high frequency range. This is because in the high frequency range, the reactance is many times bigger than the resistance and any small error in the angle identified by the FFT process causes a significant error in the estimated resistance. However, the resistance can be ignored because the value of reactance is much higher than the resistance. Hence, the reactance is selected to locate the fault by dividing it with the per-metre reactance of the line at different frequencies. Table 3-1 shows the estimated fault distance error as well as the percent error calculation for the estimated reactance using (3.4) (i.e. as a percentage of the total line length). It is clear from Table 3-1 that the maximum error is less than 0.5m , i.e. less than 1% of the total line length.

$$percent\ error = \frac{Estimated\ distance - actual\ distance}{Line\ length} \times 100\% \qquad (3.4)$$

Table 3-1 Error calculation for the distance and percent error of the reactance estimation

Fault Dist. (m)	**Calculated Dist. (m)**	**Error (m)**
0.0	-0.09	-0.09
10	9.982	-0.12
20	20.075	0.075
40	40.26	0.26
50	50.36	0.36

The technique is further tested with a Double Line (DL) fault and Double Line to Ground (DLG) fault using the 3-phase system shown in Figure 3-10. The system has the same cable and load parameters (mutual effect and line capacitance are neglected due to the short cable length and low voltage rating) as in the single phase system shown in Figure 3-4. The faults are

performed with the same location of those described for the single line to the ground faults which are, F0, F10, F20, F40, and F50 respectively. A phase to phase voltage and phase current are measured to estimate the impedance up to the fault location. Figure 3-11 presents the real and imaginary part for a DL fault at 40m from the source measuring end while Figure 3-12 shows the estimation for a DLG at the same location using phase voltage and line current.

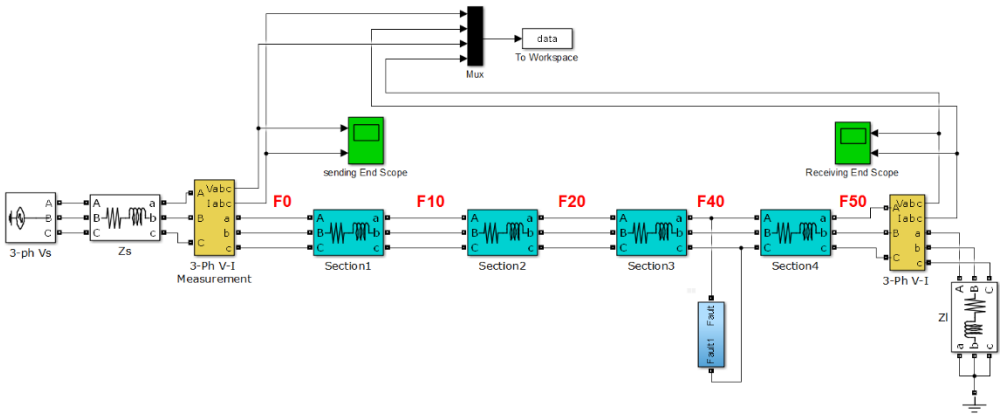


Figure 3-10 Three-phase system with DL fault at 40 m

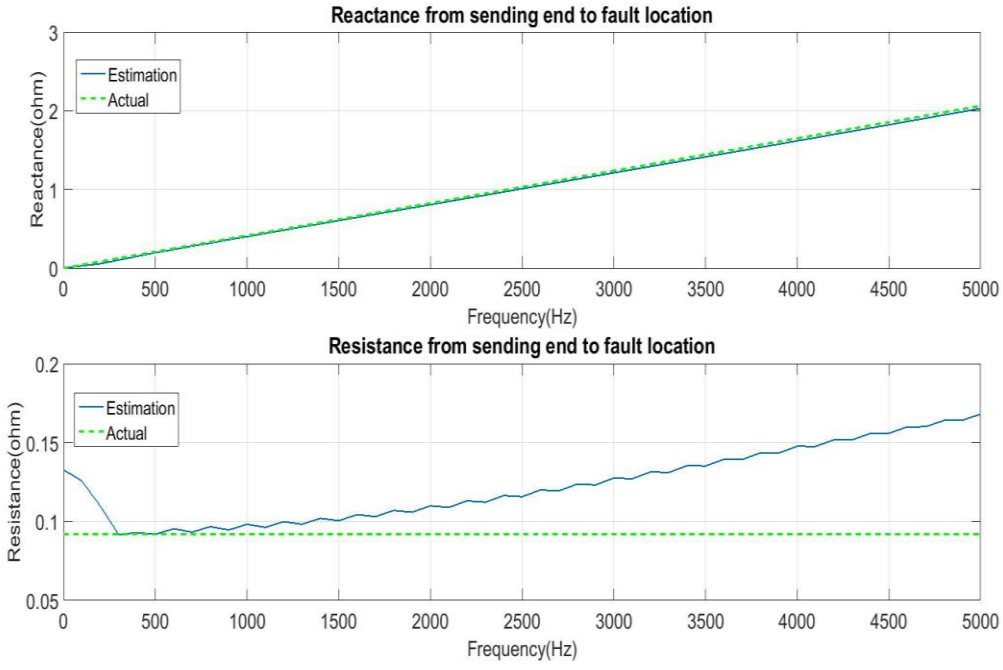


Figure 3-11 Double line fault between phase A and B at 40m

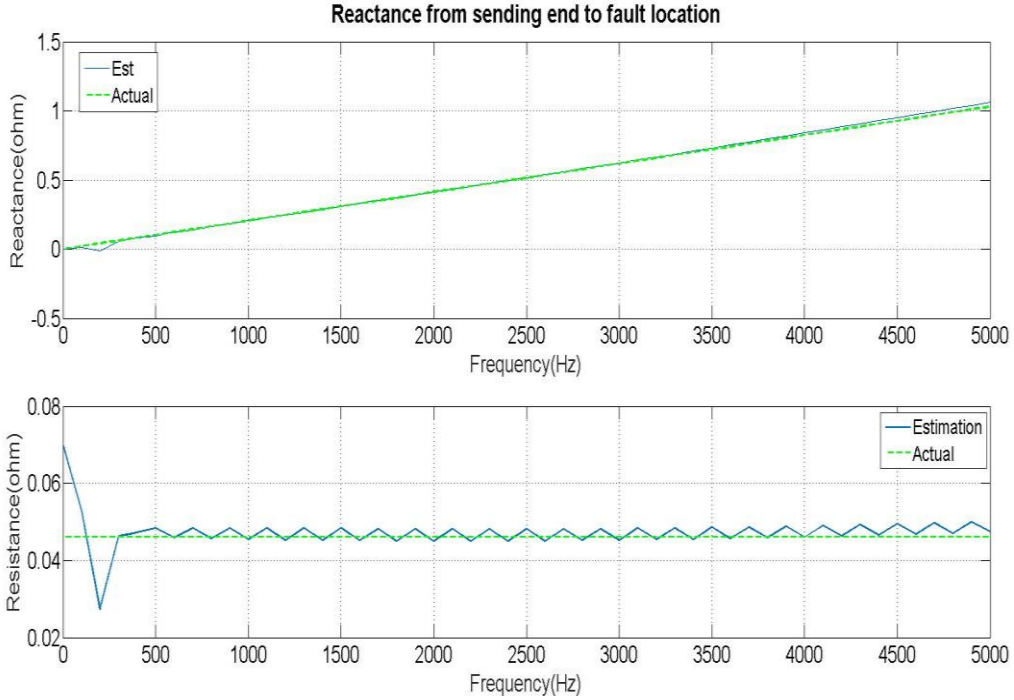


Figure 3-12 Double line to a ground fault between phase A and B at 40

It can be seen from the figures above that the estimation in the case of the reactance yield a very close match with actual line reactance with a small divergence around 5 kHz. However, the error is still less than 3% of the total line reactance or 1m as a distance. The resistance shows more error than the reactance, and it diverges as the frequency increases in the case of the DL fault. As mentioned earlier, the resistance can be ignored due to the low magnitude at higher frequencies when compared to the reactance. The reactance estimation at the other locations for a DL fault are presented in Figure 3-13 with a maximum calculated percentage error of 3% for a frequency range of 3 kHz. Finally, a three phase to ground fault is also tested at multiple location and the resulted reactance estimation is presented in Figure 3-14. Figure 3-14 shows a high accuracy of the estimated reactance using the DELFT. The maximum error for the three-phase fault is 1.12% for fault imposed at the receiving end with Rf = 4.5Ω. The error is presented on the legend of Figure 3-14.

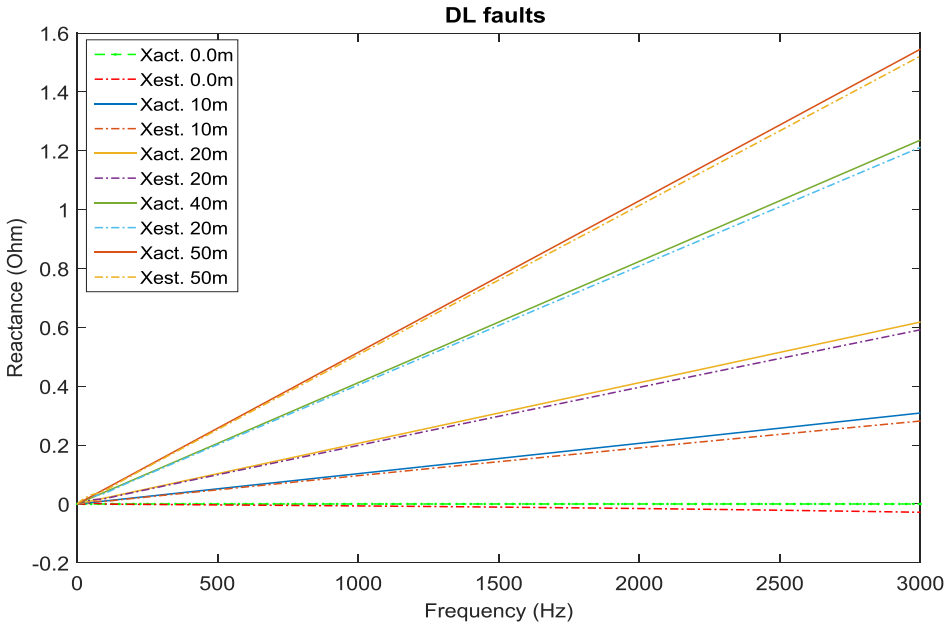


Figure 3-13 Estimated impedance for DL faults at all test locations

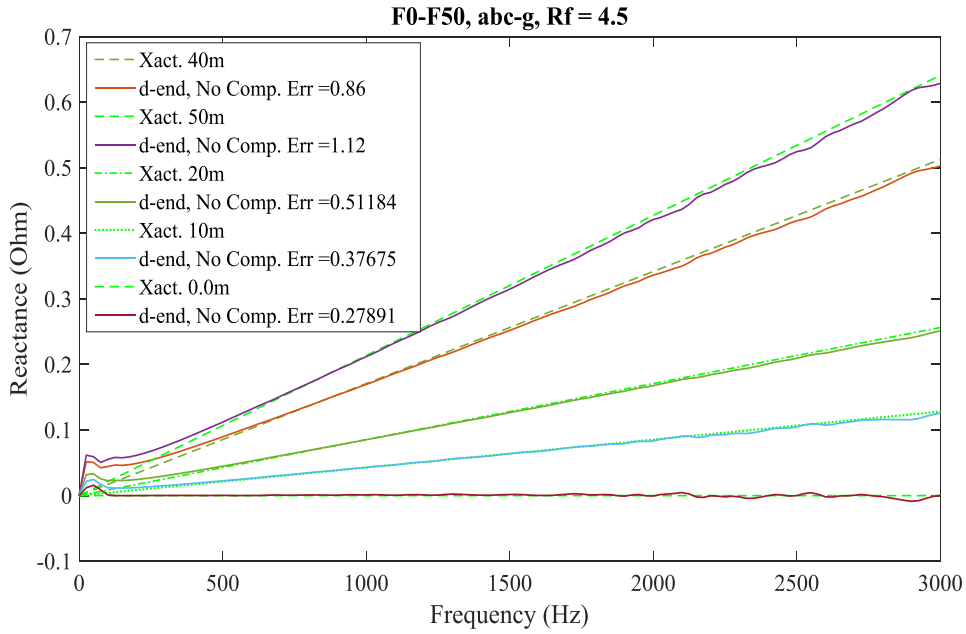


Figure 3-14 The reactance estimated for a three-phase to ground fault

In conclusion, the results of this investigation show that the DEFLT offers high accuracy for different fault types (the maximum computed error is within 3% of the actual total line value used in the simulation) for the calculated line reactance when a fault occurs at any location along the line. Furthermore, only 5ms of data is required to locate the fault, which makes

it faster than other double-ended methods. However, this technique is not evaluated under more complex system. Therefore, a thorough investigation will be cared out in the next chapter which will study the effects of tapped loads/lines on the DEFLT in order to evaluate the accuracy of the DEFLT when a tapped load is presented. Moreover, what will happen if there is a fault on the tapped line. Finally, how will the DEFLT perform under a second source (DG) penetrated the system.

3.2 Single-Ended Fault Location Technique (SEFLT)

In this section, the impedance-based fault location technique based on measurements at one node within the power system (SEFLT) developed in [9, 10] will be introduced and demonstrated using a simple circuit. A single-phase circuit with a short circuit on the distribution line, is shown in Figure 3-15, and is used to introduce the basis of this method. The supply impedance is represented by Z_s, while Z_L is the equivalent load impedance. The cable impedance between the fault and the source end is Z_x and the remaining impedance Z_{l-x} represents the cable impedance from the fault point to the receiving end of the line. Note that the earth and the neutral are connected together.

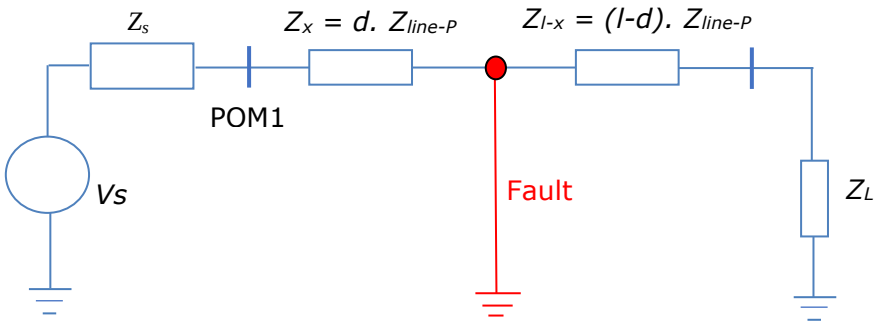


Figure 3-15 Single phase circuit with a phase to ground fault

The fault can be considered as a voltage source which creates voltage and current transients that contains information over a wide frequency range when the fault occurs. The supply source at non-fundamental frequencies behaves as a short circuit, as shown in the Thevenin equivalent circuit of Figure 3-16, while the fault is represented as a transient source which creates an equal and opposite voltage to the instantaneous pre-fault voltage (V_{pre-f}) at the fault location [10, 84, 9]. It is assumed that the full circuit is dominated by the supply side as normally $Z_s << Z_L$, and therefore Z_L can be considered an open circuit. This assumption will be revised later.

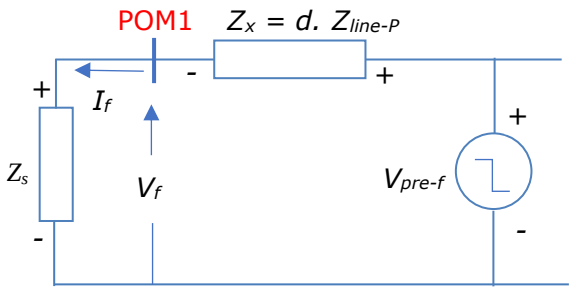


Figure 3-16 System at non-fundamental frequencies during a fault situation

Applying Kirchhoff's Voltage Law (KVL) to the non-fundamental equivalent circuit in Figure 3-16 in order to calculate the voltage drop from the measuring point (POM1) to the fault location yields (3.5):

$$V_f - I_f . Z_x - V_{pre\_f} = 0 V_f + I_f . Z_x = V_{pre\_f} \quad (3.5)$$

Where V_f and I_f are voltage and current at the source end (POM1), Rearranging (3.5) to estimate the impedance between POM1 and the fault location Z_x, gives (3.6):

$$Z_x = \frac{V_{pre\_f}}{If} - \frac{V_f}{I_f} \quad (3.6)$$

The fault distance is calculated by dividing Z_x by the per-meter impedance of the line (Z_{line-p}), as given in (3.7). The imaginary part of the impedance

only is used because the reactance is not influenced by the fault resistance, and at higher frequencies, the reactance dominates the overall impedance more than the resistance.

$$d = imag\left(\frac{\frac{V_{pre\_f}}{If} - \frac{V_f}{I_f}}{Z_{line-p}}\right) \quad (3.7)$$

V_{pre-f} in (3.6) is a created step voltage with a value equal to the measured pre-fault voltage at the POM1, assuming that the voltage drops between the POM1 and the fault location is negligible. Based on this assumption, there is an error in the fault distance estimation. Therefore, an iterative process is required to create an improved estimate of $V_{pre-f,}$ and so the initially estimated distance (d) from (3.7) is used to calculate a new value for V_{pre-f} as in (3.8):

$$V_{pre-f(new)} = V_{pre-f(POM)} - I_{pre-f}.d.Z_{line-p} \quad (3.8)$$

The fault distance is estimated again using (3.7) and this estimated distance is used to calculate a new V_{pre-f} at the fault location using (3.8). The fault location is then re-estimated using (3.7) and the updated calculation of V_{pre-f}. This iteration process is repeated until the two successive fault location estimates converge to within an acceptable tolerance of each other, for example, $d_{n+1} - d_n < 0.5m$.

3.2.1 Simulation of the single-ended method

A three-phase low voltage IPS with a source, main line of 50m and load is simulated as shown in Figure 3-17. The details of the circuit are given in Table 3-2. The system is simulated using MATLAB Simulink. The source frequency is 50Hz.

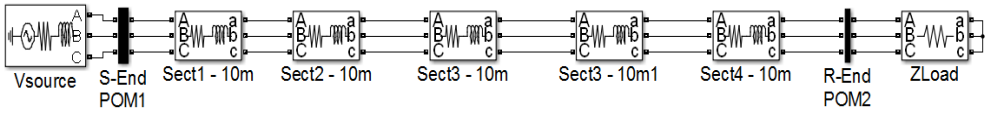


Figure 3-17 Simulated IPS

Table 3-2 the simulated IPS parameters

Circuit parameter	**Value**
Source voltage (ph-ph)	440 (V)
Source impedance	0.0011 + 0.0096j Ω
Line per-meter resistance at 50Hz	30 μΩ
Line per-meter inductance at 50Hz	0.24 μH
R-end load	100 kW
Sampling frequency	100 kHz

The required voltage and current signals are measured from the sending end (POM1) of the main line of the system as shown in Figure 3-17 with a sampling frequency of 100 kHz. A window of two cycles is used to capture the required signals with one pre-fault cycle and one post-fault cycle as shown in Figure 3-18. The captured signals are then windowed with a Blackman window to remove the effect of edge leakage as shown in Figure 3-19. The length of the window is equal to the length of the captured signals with minimum value starting from zero on the edges to a maximum value of one in the middle of the window.

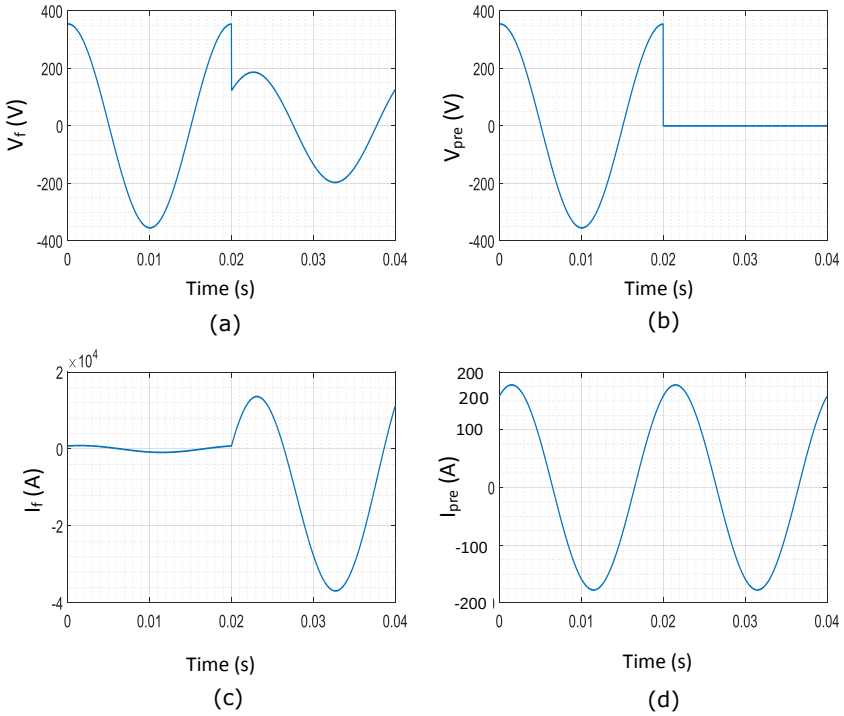


Figure 3-18 The captured signals (a) voltage at the POM1 (b) the created voltage at the fault location V_(pre-f) (c) Current at the POM1 (d) pre-fault current

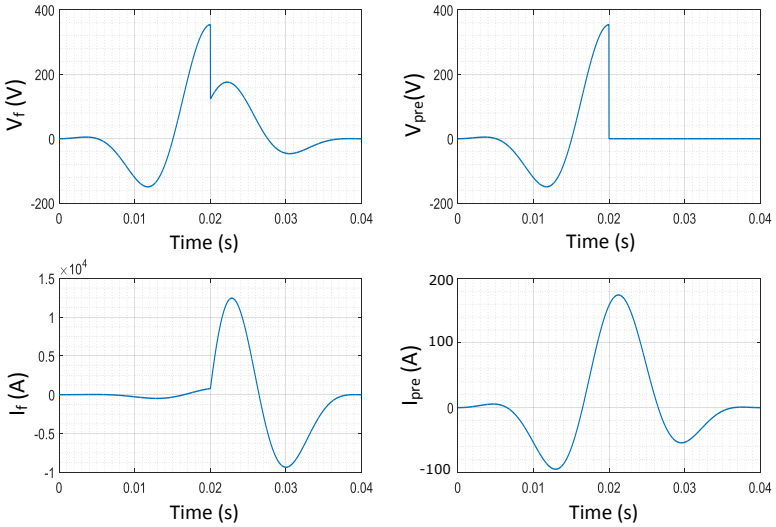


Figure 3-19 The measurement processed by a Blackman window

The next stage is to process the required signals using a Fast Fourier Transform (FFT) to transfer the time domain signals to the frequency domain. The frequency domain equivalent of Figure 3-19 is presented in Figure 3-20. Finally, the iterative method is applied to calculate the distance to the fault at each frequency from 50 Hz to 3 kHz and then to estimate the voltage at the fault location only at the fundamental frequency. The flowchart in Figure 3-21 summarizes the SEFLT process.

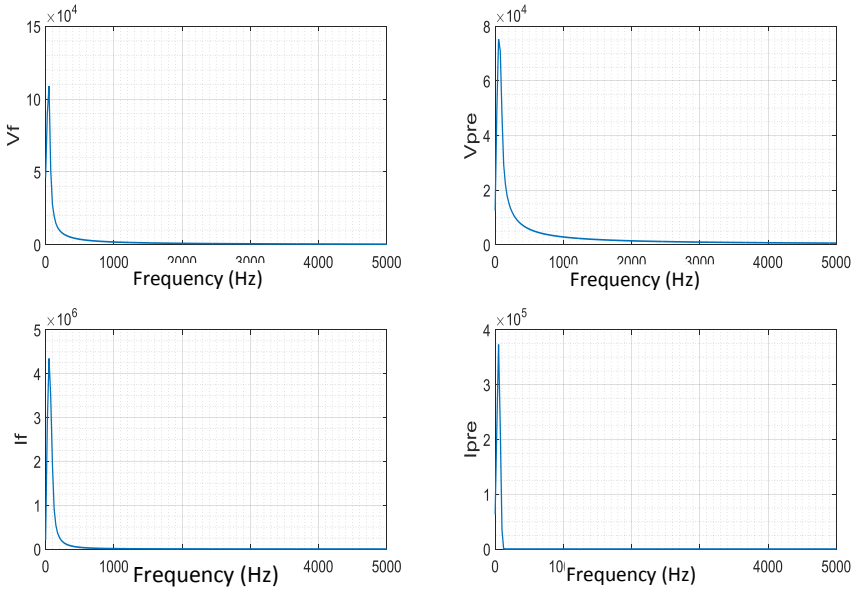


Figure 3-20 the magnitude part of the signal shown in Figure 3-18 in the frequency domain

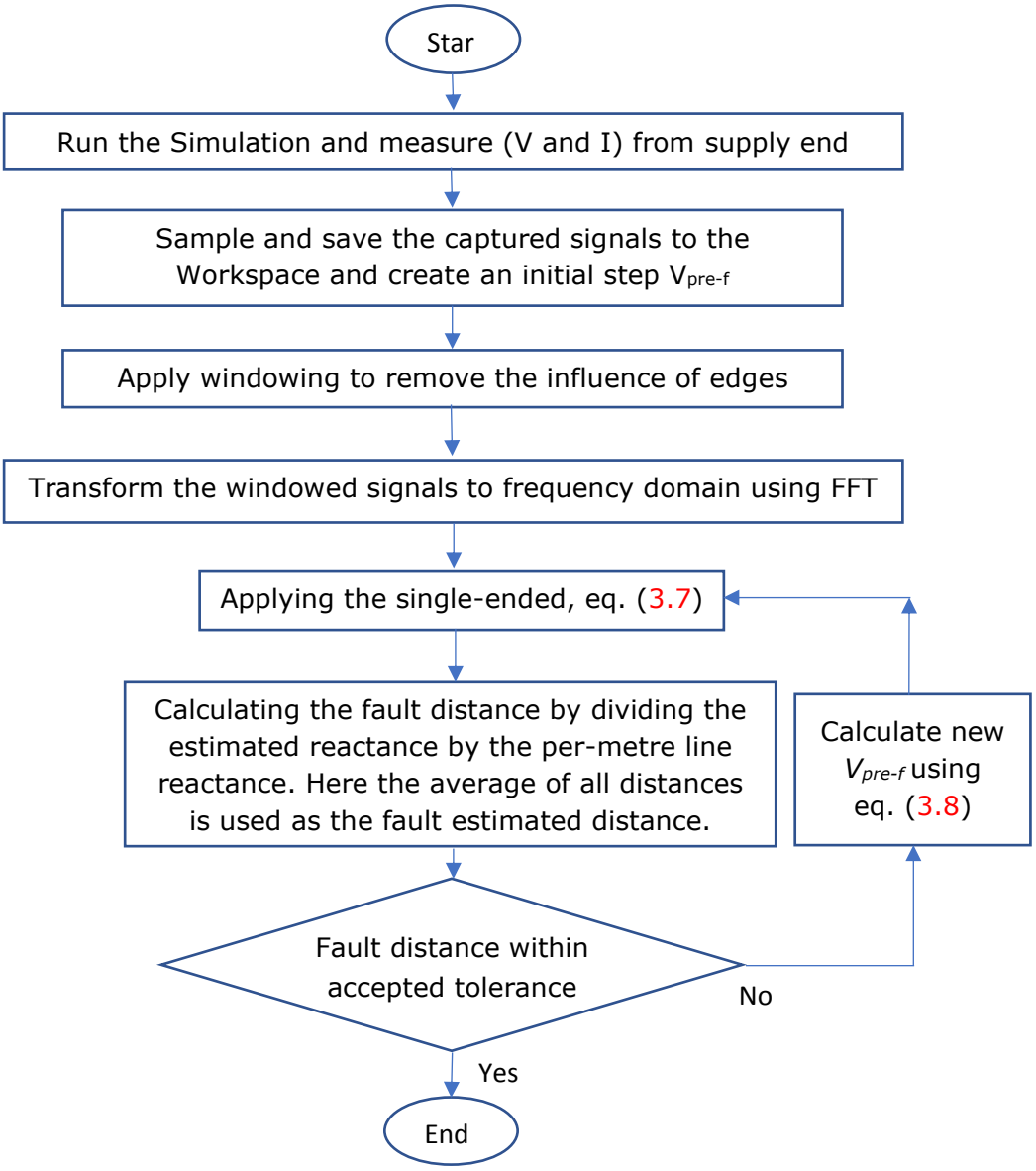


Figure 3-21 The methodology of SEFLT

Different types of fault using a fault resistance of 0.01Ω are applied to the system of Figure 3-17 at two locations to verify the proposed method for fault location. First, a fault at the source end is applied, and Figure 3-22 (a, b and c) shows the estimated reactance using the SEFLT summarized in Figure 3-21. Figure 3-22 (a) shows a Line-to-Ground (SLG) fault, while Figure 3-22 (b and c) show a Double-Line-to-Ground (DLG) and a Double-Lines (DL) fault, respectively. Likewise, Figure 3-22 (d, e and f) presents the results of the fault applied at the load end with the same fault conditions.

It is noticeable that the estimated reactance shows high accuracy with a maximum error of less than 2%. A summary of the percentage error for SLG and DL faults throughout five locations of the transmission line is presented in Table 3-3 and Table 3-4. The percentage error is calculated according to (3.4).

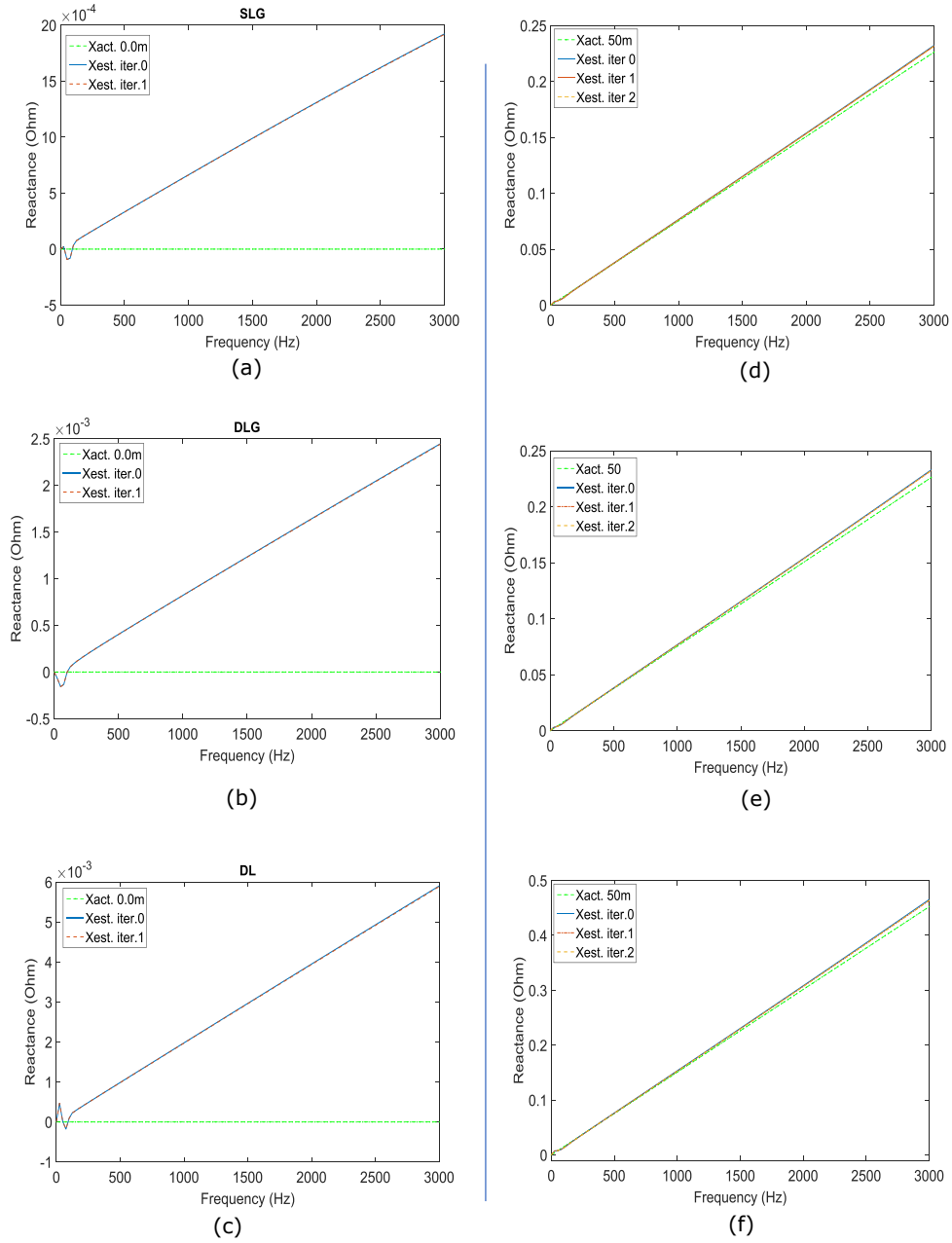


Figure 3-22 Estimated reactance: (a) SLG fault on Source-end, (b) DLG on Source-end (c) DL on Source-end (a) SLG fault on Load-end, (b) DLG on Load-end (c) DL on Load-end

The "Xact." on the legend is the actual reactance from the POM1 to the fault location while "Xest." is the estimated reactance. Furthermore, the term "iter." Refers to iteration. Interestingly, the proposed method usually needs only 2 or 3 iterations to converge to the pre-set tolerance between two consecutive iterations. It is shown in Figure 3-22, that the required number of iterations in the given example is two iterations which shows the reliability of the process to reach the final value in a short time.

Table 3-3 Percent error calculation for SLG faults

Actual distance (m)	Estimated distance (m)	Error (%)
00	0.128	0.25
10	10.175	0.35
20	20.18	0.35
30	30.26	0.52
40	40.35	0.7
50	50.45	1.4

Table 3-4 Percent error calculation for DL faults

Actual fault distance (m)	Estimated distance (m)	Error (%)
00	0.21	0.42
10	10.10	0.20
20	20.10	0.20
30	30.124	0.25
40	40.125	0.25
50	50.142	0.285

3.2.1.1 Influence of fault inception angle

The test above was performed with the fault applied at the maximum point of the supply voltage waveform of phase A (i.e. an inception angle of 90˚). Here, the fault inception angle will be varied from 30˚ to 180˚ to investigate how the proposed method will perform under different conditions. A SLG fault at the load terminal of the line is considered for this demonstration, and the percentage error calculation is presented in Table 3-5.

Close inspection of Table 3-5 shows that the SEFLT is reliable with different fault inception angles as the maximum registered error is around 3%. On the other hand, the highest error is achieved when the fault is applied at the zero-crossing point or up to 5° around the zero-crossing point, where the error is increased to 5.5%. This amount of error is still within an acceptable tolerance. It should be noted that faults occurring around the zero-crossing point present a problem for other fault location methods as the fault transient will be small and the Signal to Noise Ratio (SNR) will also be low.

Table 3-5 influence of fault inception angle on the single-ended method.

Inception angle (degree)	error (%)
30	1.2
60	0.9
90	0.9
120	0.92
145	0.3
165	0.81
175	2.7
178	4.7
180 (Zero crossing)	5.5

3.2.1.2 Influence of the fault resistance on the SEFLT

This case study seeks to examine the reliability and validity of the proposed fault location technique with different fault resistances. Hence, the fault calculation process is performed, increasing the fault resistance by a fixed step between simulations, and maintaining all the other parameters in the studied system. The fault resistance is varied from 0.01Ω to 0.3Ω and the load is kept as 1.11Ω (175kW). The error calculated for each resistance are summarized in Figure 3-23. The test fault was on the end of the line.

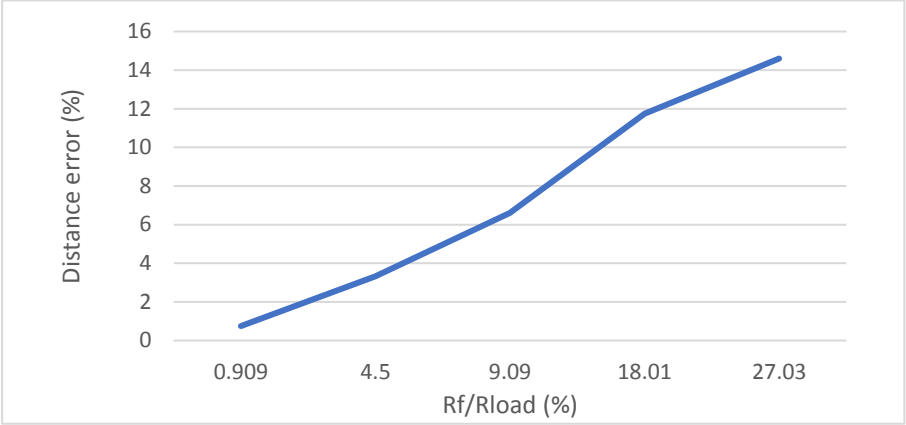


Figure 3-23 Percentage error with varied fault resistance

It can be seen that the error rises to more than 10% when the fault resistance becomes large enough to be compared to the load resistance. In this case, the fault resistance is about 18% of the load resistance, which leads to a significate amount of the fault current passing through the load terminal; this is neglected in the calculation. A further demonstration is made by fixing the fault resistance at 0.1Ω and increasing the load resistance. Figure 3-24 shows the plot of the error calculation against the ratio of the fault resistance to the load resistance. It shows that the error does not change significantly when the ratio of fault resistance to load resistance is 0.03 or less. If the ratio is around 9%, the fault location error is about 6.5%.

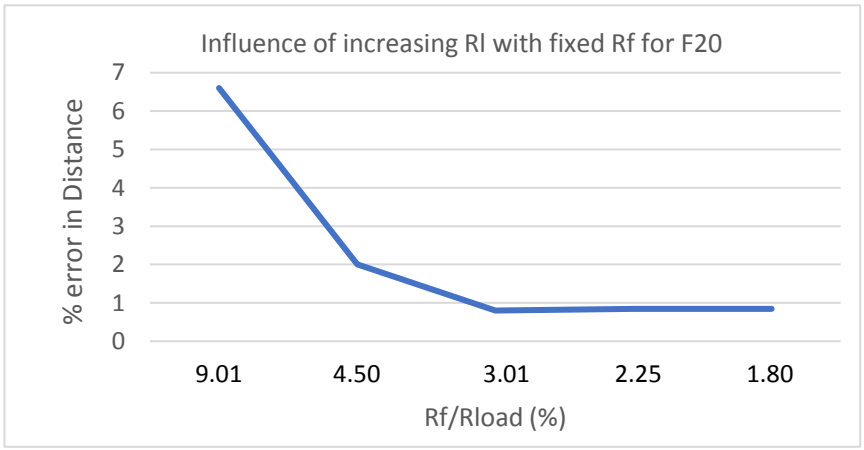


Figure 3-24 Effect of the ratio of the fault resistance to the load resistance

3.2.2 SEFLT which compensates for high fault resistance

The study carried out in section 3.4 showed that the error of the single-ended fault location method increases as the fault resistance increases because the current which flows in the load is neglected in the estimation equations (3.7 and 3.8). Hence, an estimation approach that considers the compensation for the receiving end current will be introduced and demonstrated in this section. A power system at fundamental frequency with considerable fault resistance is shown in Figure 3-25(a) while the system at non-fundamental frequencies is shown in Figure 3-25(b). As described earlier, Z_s, Z_x, Z_{l-x} are the impedances of the source, to the fault location and from the fault point to the line terminal respectively. The difference between this non-fundamental system with the short circuit or low resistance fault equivalent circuit explored in section 3.3 is that the load terminal is included, and the fault resistance is not negligible.

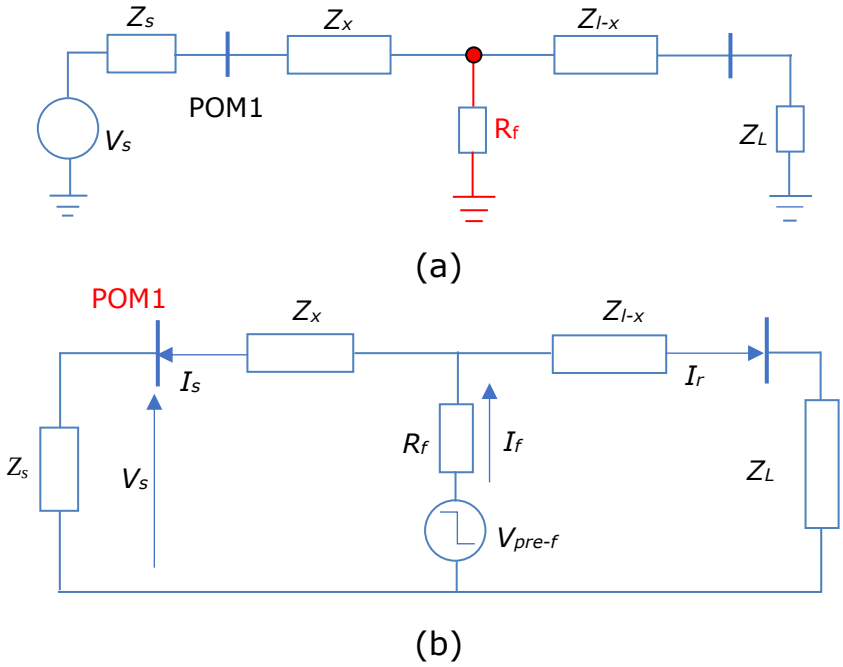


Figure 3-25(a) System at the fundamental frequency with high fault resistance (b) Equivalent circuit at non-fundamental frequencies

The circuit theory as applied to the equivalent circuit of Figure 3-25(b) yields:

$$V_s + I_s.Z_x + I_f * R_f = V_{pre\_f} \quad (3.9)$$

Rearranging for Z_x, yields (3.10):

$$Z_x = \frac{V_{pre_f} - V_s - I_f * R_f}{Is} \quad (3.10)$$

$I_f = I_s + I_r$, and substituted into (3.10) gives:

$$Z_x = \frac{V_{pre-f} - V_s - (I_s + I_r) * R_f}{Is} = \frac{V_{pre-f} - V_s}{Is} - R_f - \frac{I_r}{Is} R_f \quad (3.11)$$

Where V_s and I_s are measured at POM1, V_{pre-f} is the assumed step waveform at the fault location using the pre-fault value of V_s. R_f can be calculated assuming that ($R_x << R_f$), hence:

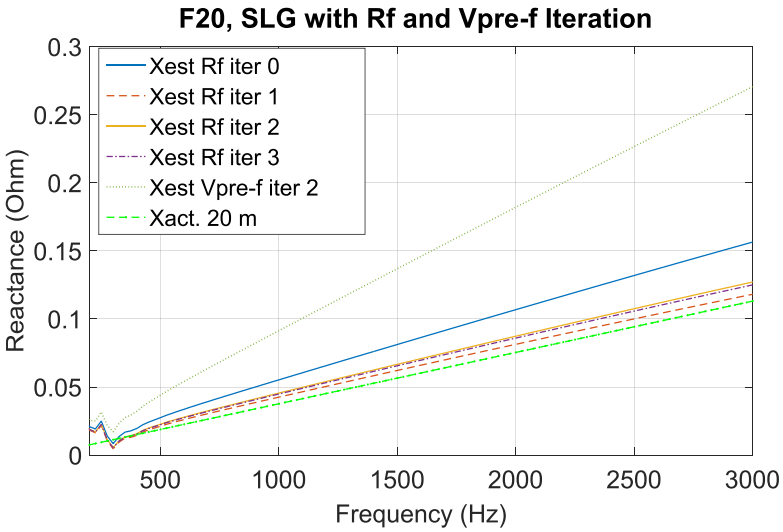
$$R_f \approx real\left(\frac{V_{pre-f} - V_s}{Is}\right) \quad (3.12)$$

The ratio of the receiving end current to the source end current is calculated using the current divider rule, and the source impedance is calculated as given in (3.13):

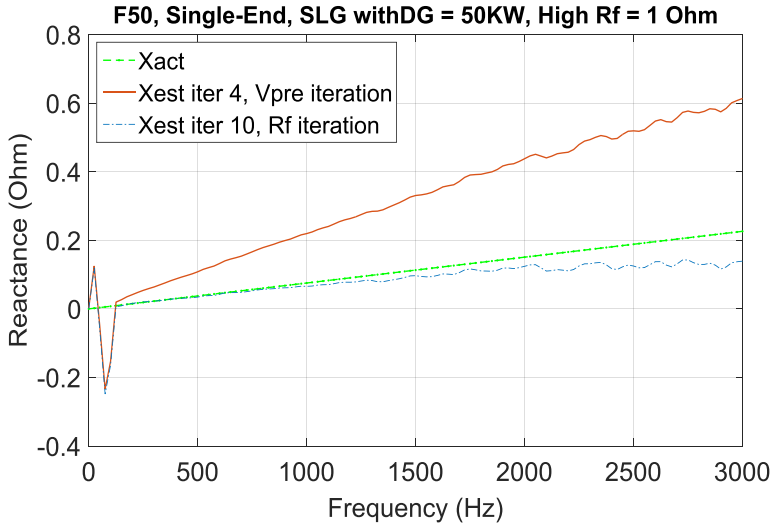
$$\frac{I_r}{Is} = \frac{Z_s + Z_x}{Z_L + Z_{line} - Z_x}, \text{ and } Z_s = \frac{V_s}{I_s} \quad (3.13)$$

In (4.9), Z_{line} is the total line impedance, Z_L is the load impedance which can be estimated using pre-fault (steady state) measured *V* and I at the source end. As a consequence of the high R_f, a new iteration method is adopted using (3.11) if the estimated R_f is large enough and comparable to the received end load (which leads to high estimation error). Z_x is assumed zero in the first iteration and (3.13) is calculated. Then Z_x is estimated using (3.11). This estimated Z_x is used to calculate a new ratio of $\frac{I_r}{Is}$ which is then re-used to calculate a new Z_x in (3.11). This iterative process is repeated until the tolerance between two iterations converges to a pre-set value of

0.5m. This is a similar process to what was performed with the pre-fault voltage (V_{pre-f}) iteration methodology, as in section 3.3.



(a)



(b)

Figure 3-26 Estimated reactance for the load compensated method versus non-compensated method (a) 20 m from POM1 (b) fault on the load end

The described methodology is applied to the system of Figure 3-17 with a SLG fault 20m from the POM1 and then on the receiving end with a fault resistance of 1Ω and load resistance of 1.92Ω. Figure 3-26 (a) shows the estimated reactance using the R_f iteration against the V_{pre-f} iteration for a fault at 20m. The final value using the R_f iteration is plotted in the dash-

dotted purple colour while the dotted line is for the V_{pre-f} iterative method. Figure 3-26(b) presents the estimated reactance plotted using the blue dash-dotted line and compared to the pre-fault voltage iterative method given with the solid red line for a fault at 50m. A large error is present due to the (ignored) current flow to the load, but the proposed R_f compensated method reduced this error significantly. A summary of the error calculation for various fault resistances which compares the R_f iterative compensation method to the V_{pre-f} iterative compensation method for the same fault at the load-end is given in Table 3-6 and the improvement in distance estimation can clearly be seen.

Table 3-6 Error comparison of R_f iterative compensation method versus V_{pre-f} compensation method

R_f (Ω)	V_{pre-f} Iterative compensation		R_f Iterative compensation	
	Est. Distance (m)	**Error (%)**	Est. Distance (m)	**Error (%)**
0.01	50.7	**1.42**	-	-
0.1	56.1	**12.22**	49.33	**-1.4**
0.5	78.9	**57.94**	47.44	**-5.1**
1.0	102.36	**104.7**	45.44	**-9.11**
2.0	135.55	**171.1**	42	**-15.98**

Finally, the SEFLT with R_f iteration algorithm offers a good compensation for the error caused by the neglected receiving end current under high fault resistance.

3.3 Summary

In this chapter the DEFLT and SEFLT based on the work presented in [9, 10, 11] is represented and demonstrated. The chapter started with introducing the DEFLT. The technique validated based on Matlab simulation of simple circuit. The simulation showed a high fault distance accuracy with different fault locations and types throughout the system. The second part of this chapter introduced the SEFLT. The technique is validate using Matlab simulation on a simple circuit. The simulation showed a high fault distance accuracy with different fault locations throughout the system. However, the investigation of the fault resistance showed that the accuracy drops as the fault resistance increases. Therefore, the SEFLT with compensation for the receiving end current under high fault resistance was reintroduced and validated using the same system.

Finally, both techniques were reintroduced and demonstrated on a simple system consists of a one line. Therefore, the main aim of the following chapters is to thoroughly investigate the devised techniques on more complex microgrid that includes tapped load/lines and inverter-based DG. The techniques' strength and weak points will be presented using a thorough evaluation of inserting multiple tapped loads and lines between the POMs. This will show how the performance of the techniques and if they are capable of locating different fault with high accuracy under these realistic system parameters. Consequently, a solution will be proposed to address the limitations. Finally, the effect of DGs on fault location are of vital important due to the increase use of the renewable resources. Therefore, the influence of the inverter based DG on both technique will be evaluated in the following chapters.

Chapter 4 - Double-Ended Fault Location Technique (DEFLT)

4.1 INTRODUCTION

In this chapter, the wideband DEFLT introduced and explored in chapter three will be thoroughly investigated on more complex microgrid. Few factors will be studied in order to investigate the strength and limitation of the technique. Then, a solution to some of the limitation will be presented and demonstrated through simulation. Finally, investigating the inverter-based DG on the suggested technique.

4.2 Factors affecting the DEFLT

The previous section analysed the DEFLT based on [11] used a simple circuit which is composed of a source, distribution line, and a simple load. This section will investigate factors that could affect the accuracy of the proposed method. Four cases will be analysed which include added tapped loads, the effect of random measurement noise, the effect of source impedance, and finally the value of the fault impedance.

4.2.1 Influence of tapped load on the DEFLT

The investigation of the tapped-load effect on the DEFLT will be carried out in this section. Therefore, three tapped loads are added to the circuit of Figure 3-4 as shown in Figure 4-1. The magnitude of the tapped load impedances are 10, 20, and 30 times the receiving end impedance as indicated in Figure 4-1 by 10*Zl, 20*Zl, and 30*Zl. The algorithm is tested for the same five fault locations and compared with the case without the tapped loads. A summary of the reactance estimated is presented in Figure

4-2. The sold line is without the tapped loads while the dashed line is with the tapped loads.

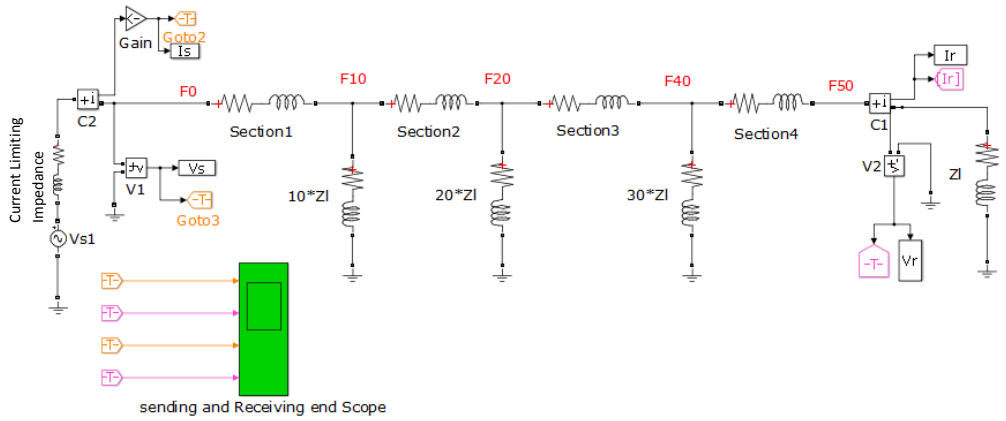


Figure 4-1 Single phase circuit with tap loads

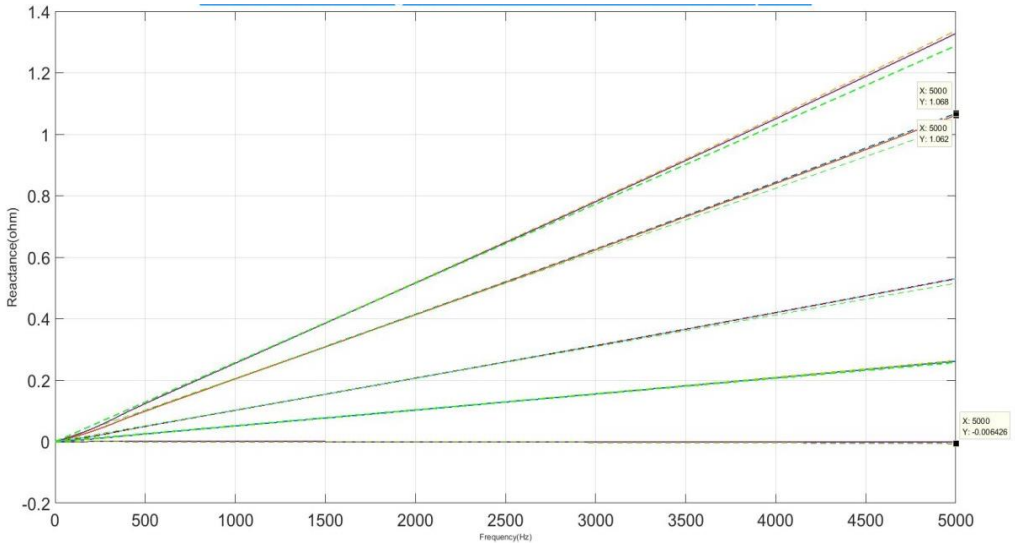


Figure 4-2 Single phase circuit with tapped loads

The percentage error presented in Table 4-1 shows that there is a little increase in the error at higher frequencies as shown in Figure 4-2. The maximum error is 3.7% in an increase by 0.7% compared to the case without tapped loads. The calculation is performed for a single frequency sample (3 kHz) which represents the highest error in the full useful frequency range. The reason behind the error increasing is that the algorithm did not consider the current consumed by the tapped loads. The

error will be affected by the magnitude of the tapped loads compared to the receiving end magnitude. It was found that when the receiving end load (Larger load) magnitude is changed to 10*Zl and then changed to 20*Zl, the error increases to 8% as given in Table 4-2. When a low impedance load (compared to the receiving end load) is placed on the taps, the DEFLT ignores a large tap current, which causes a larger error in the estimated fault location as summarized in Table 4-2. i.e. for an accurate estimate, the formulation of (3.1) and (3.2) should include the current drawn by the tapped load. It will be demonstrated in the following sections that under higher source impedance the tapped load will have a large adverse effect.

Table 4-1 Percent error calculation with and without tapped loads

Fault Dist.(m)	**Est. dist. without Tapped Load (Ω)**	**Error (%)**	**Est. dist. with Tapped Load (Ω)**	**Error (%)**
0.0	-0.08	-0.16	-0.245	-0.49
10.0	10.245	0.49	10.16	0.31
20.0	20.57	1.14	20.59	1.17
40.0	41.22	2.44	41.46	2.91
50.0	51.54	3.09	51.885	3.77

Table 4-2 Error calculation with maximum load position changed

Fault Location (m)	**Max. Load at the R end**		**Max. Load at Tap T1**		**Max. Load at Tap T2**	
	Est. Dist. (m)	**Error (%)**	Est. Dist. (m)	**Error (%)**	Est. Dist. (m)	**Error (%)**
0	-0.25	-0.5			-1.16	-2.33
10	10.16	0.31	0.24	0.48	10.31	-0.62
20	20.59	1.17	21.2	2.4	20.68	1.36
40	41.46	2.91	43.15	6.30	42.81	5.629
50	51.89	3.79	54.13	8.26	53.88	7.771

4.2.2 Influence of measurement noise

In this section, the efficiency of the DEFLT dealing with the effect of measurement noise will be studied and demonstrated through simulation. A random White Gaussian noise is used for this purpose. The noise has been added to the captured voltage and current measurements at both terminals as shown by the simulated circuit of Figure 4-3. The magnitude of the added

noise is varied from 0.1% – 2.0% of the peak value of the captured signals (these values are the usual amount of noise presented by measurements) in order to visualize how the DEFLT is going to perform in a realistic system.

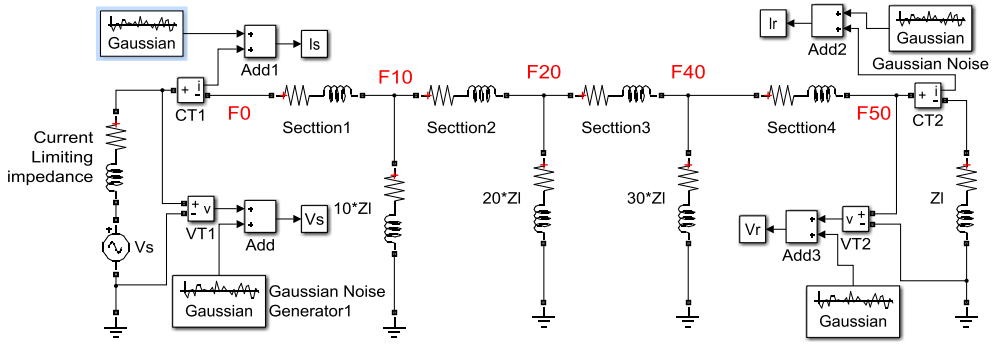


Figure 4-3 Single phase system with Gaussian noise added to the measurement

A SLG fault is used at 40m from the sending end to investigate the influence of measurement noise on the estimated reactance. The reactance estimated with different added random noise values is plotted in Figure 4-4 for comparison. The reactance estimated shows that there is some adverse influence from the added noise, especially at higher frequencies (over 3000 Hz). This specific pattern is because the measured signal, especially, the voltage has smaller Signal to Noise Ratio (SNR) at these frequencies. A closer view shows that the error increases proportionally to the magnitude of the added noise. However, the maximum error calculated with the largest added noise is 4.27%. An important note is that not all of this error is from the Gaussian noise. In this system, there are three tapped-loads which are ignored in the DEFLT calculation and this causes some error as demonstrated in the previous section.

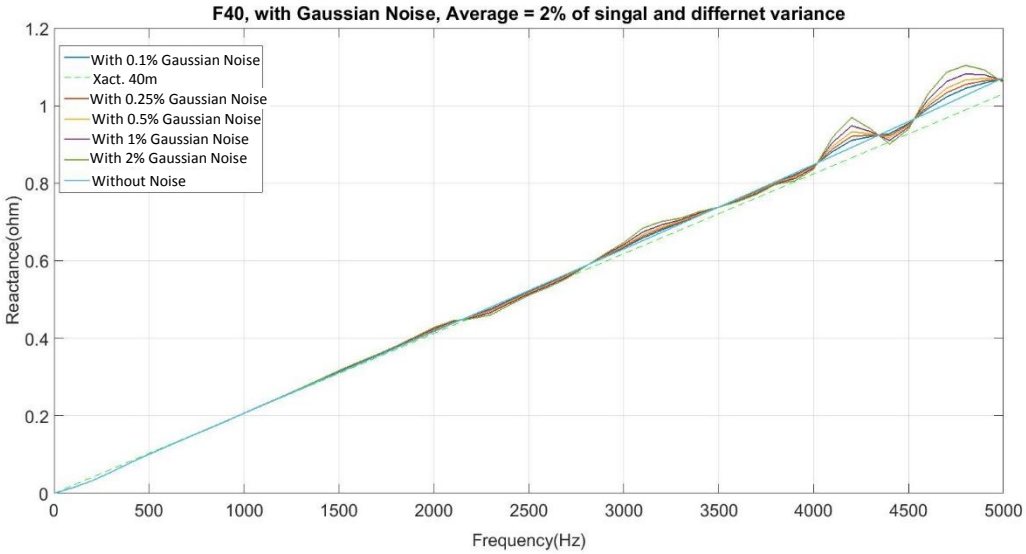


Figure 4-4 Estimated reactance with Gaussian noise added to the measurement

4.2.3 Influence of source impedance

The ratio of the source impedance (Z_s) to the receiving end impedance (Z_r) will be investigated in this section. Based on a single fault test at 40m from the source end with R_f = 1.5Ω, the source impedance is gradually increased while keeping the load impedance the same in order to investigate the limitation of the technique for different source impedances. The summary of the test is presented in Table 4-3. It is evident that the error increased significantly when the ratio of (Z_s/Z_r) goes beyond to 27%. This is because the generated fault current and voltage transients are limited with the high source impedance which leads to a lower SNR at high frequencies, and therefore a lower estimation accuracy. It should be noted that the source inductance is kept at 0.0314Ω for most of the test. When the source inductance increased ten times as presented in the highlighted rows whilst keeping a small resistance, the error increased five times to 9%. Examining the recorded data showed that the high inductance not only limits the fault transients but also smoothes out the transient which works as a low pass filter that filters out most of the useful wideband frequency information. In

conclusion, the DEFLT method offers a high accuracy when the Z_s/Z_r ratio is less than 15%.

Table 4-3 impact of Z_s/Z_r ratio on the accuracy of the d-ended method

Zs (Ω)	Zr (Ω)	Act. Dist. (m)	Act. Dist. (m)	Error (%)
0.00051+j0.00314	37+j0.5	40	40.22	0.416
0.0051+j0.0314			39.3	-1.39
0.051+j0.0314			39.25	-1.46
0.51+j0.0314			39.0	-2.01
1.0+j0.0314			38.7	-2.52
2.0+j0.0314			38.13	-3.75
0.051+j0.314			35.5	-8.97

4.2.4 Influence of fault resistance

Fault impedance has a critical role in most fault location techniques. Therefore, its effect on the DEFLT will be investigated in this section. The source impedance is set to (0.5+j0.0314Ω) through the whole test as well as the load impedance is kept the same (37+j0.5 Ω). A summary of the R_f changes, the estimated fault distance, and the calculated percentage error are presented in Table 4-4. The table shows that the DEFLT is not highly affected by the magnitude of the fault resistance for this value of source impedance. The error increased from 0.36% to 3.9% when the fault resistance increased 24 times from 1.5Ω to 36Ω which is almost equal the receiving end resistance. The technique is further tested by adding fault inductance as shown in the last three rows. The error is slightly influenced when the inductance increased from 3.14mΩ to 0.314Ω. This outcome demonstrates that the fault impedance has a limited impact on the DEFLT.

Table 4-4 influence of R_f on the estimated fault distance accuracy

Zf (Ω)	Zr (Ω)	Act. Dist. (m)	Act. Dist. (m)	Error (%)
1.5	37+j0.5	40	39.85	-0.3
4.5			39.82	-0.36
9			39.45	-1.12
18			38.85	-2.31
27			38.4	-3.2
36			38.05	-3.9
36+j0.00314			39.7	-0.59
36+j0.0314			39.36	-1.28
36+j0.314			40.17	0.33

4.3 Inclusion of a tapped line

The DEFLT with the fault on the tapped line will be explored and demonstrated in this section. The system in Figure 3-1 is amended to include one tapped line with the load as shown in Figure 4-5. A short circuit fault is applied at the end of the tapped line. Z_T is the tapped line impedance and $Z_{T\text{-}L}$ is the tapped line load.

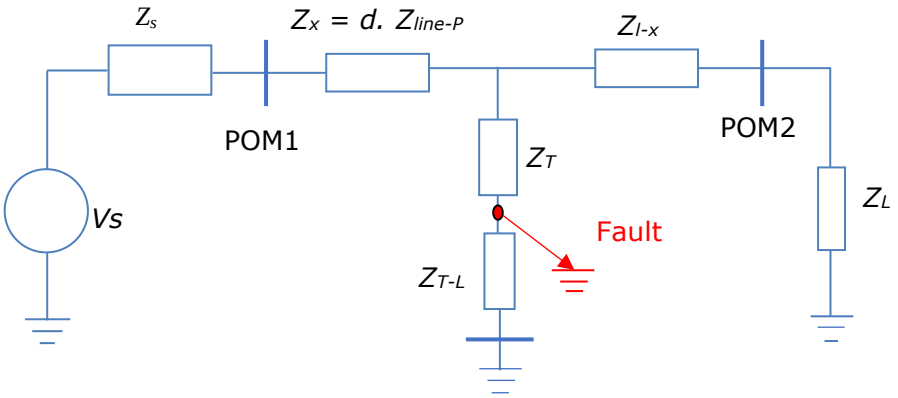


Figure 4-5 Single line diagram with a short circuit fault on the tapped line

Similarly, the equivalent circuit at non-fundamental frequencies will be amended to include the tapped line as shown in Figure 4-6. It is assumed that the tapped load is short-circuited by the fault (i.e. $R_f << Z_{T\text{-}L}$). (3.1) is also amended based on Kirchhoff's Voltage Law (KVL) to give (3.4):

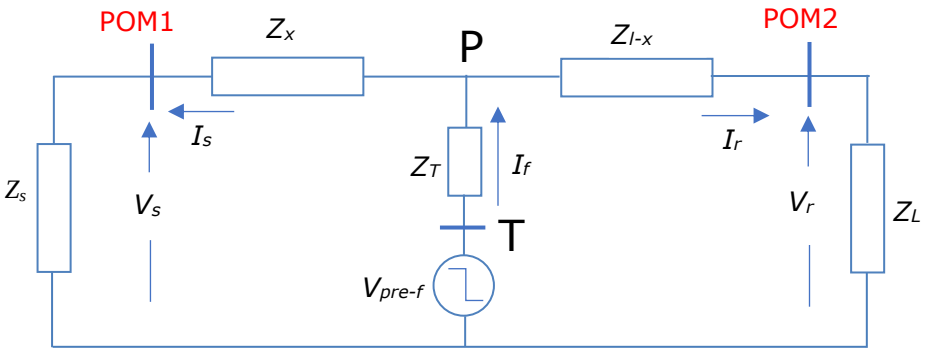


Figure 4-6 System at non-fundamental frequency during a fault on the tapped line using double-ends measurements

$$V_s + I_s.Z_x + I_f.Z_T = V_r + I_r.Z_{l-x} + I_f.Z_T \quad (4.1)$$

Rearranging (3.4) in order to calculate the value of Z_x produces (3.5):

$$Z_x = \frac{V_r - V_s + I_r.Z_l}{I_s + I_r} \quad (4.2)$$

An interesting conclusion can be made from (4.2) that the DELFT does not require details of the tapped line and its load. Hence, the tapped line is considered as a part of the fault impedance according to the DEFLT, and the distance estimated to the fault is the distance from the POM1 to point P in Figure 4-6. Consequently, the DEFLT is unable to locate faults on the tapped line. However, it has the ability to locate the faulted tapped line. So, it could be utilised to discriminate between possible fault locations calculated using a single-ended technique.

4.3.1 Demonstration through simulation

The circuit of Figure 4-1 is further developed by adding more tapped-lines between the main line and the end loads as shown in Figure 4-7. The length of the added tapped lines is shown in Figure 4-7 with the same per-metre impedance as the main line. The first tapped line to the source is 40m in length while the third tap line is 10m and is close to the receiving end. As in the basic circuit, the signals are measured at both ends of the main line with 50kHz sampling frequency. A Blackman window is applied to remove the effect of the signal's edges.

The DEFLT is applied to a SLG fault on the end of each tapped line as marked in Figure 4-7 by F1, F2, and F3. It was found that the method is unable to estimate the fault location on the tapped line. However, the technique is able to indicate the faulted tapped line instead of the estimated location as shown in Figure 4-8. It can be helpful if the faulted line is located and disconnected to keep the power supply to the other part of the system until the fault is removed. The application of this will be further explored in section 4.8.

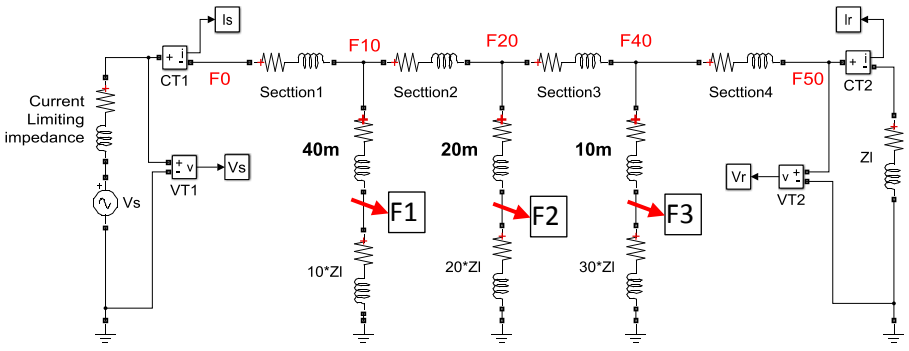


Figure 4-7 the proposed circuit with additional tapped lines

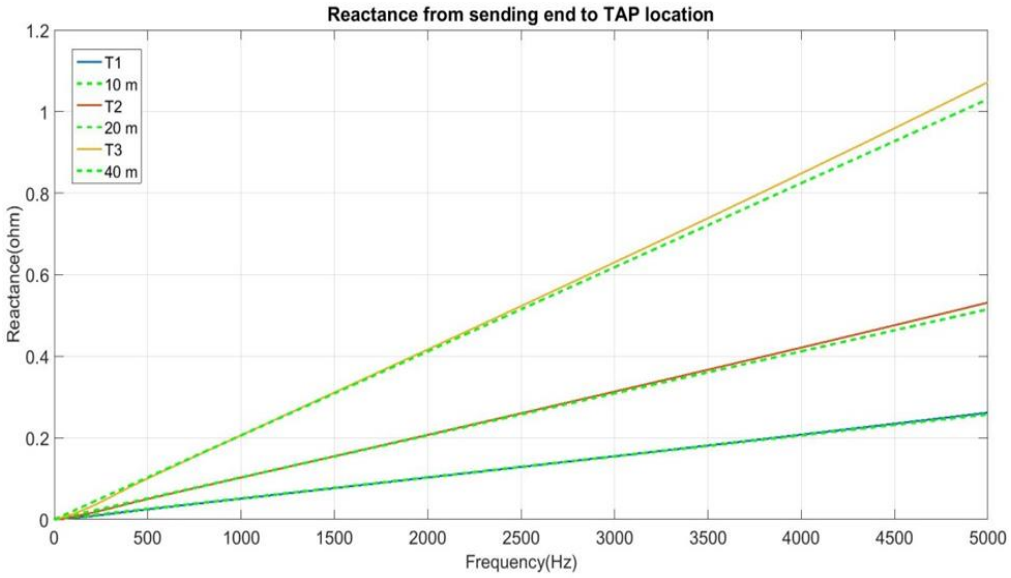


Figure 4-8 the reactance estimation for faults on the tapped line

4.4 Implementing the DEFLT, ignoring Ir

It is proposed that the DEFLT can be implemented using only three measurements. In this approach, the source end voltage and current, as well as the receiving end voltage, will be required. (3.2) is approximated by (4.3), which will be used in this section.

$$Z_x = \frac{V_r - V_s}{I_s} \tag{4.3}$$

where V_s, I_s are the source end voltage and current, V_r is the receiving end voltage. Compared to (3.2), I_r is neglected in the denominator because at non-fundamental frequencies, it is assumed that $I_r << I_s$. Similarly, $I_r * Z_{line}$ in the numerator of (3.2) will be very small compared to $V_r - V_s$, hence, neglecting it has a limited influence on the estimated reactance.

Two line-neutral fault tests (F20 and F40) are imposed with R_f = 4.5Ω in order to demonstrate this approach. In Figure 4-9 shown for F20, the

estimated reactance using (3.7) (the solid blue line) is compared to the estimation using (3.2) (the dash-dotted red line). There is an obvious match between the two estimations. This behaviour is verified by looking at the frequency domain of the signals using in Figure 4-10 which shows that $I_r(f) \ll I_s(f)$ as well as $I_r * Z_{line} \ll V_r - V_s$. There is a small reduction in the accuracy when a fault was imposed 40m from the source-end (F40), which is shown in Figure 4-11 and Figure 4-12. However, the increase in the percentage error is less than 1%.

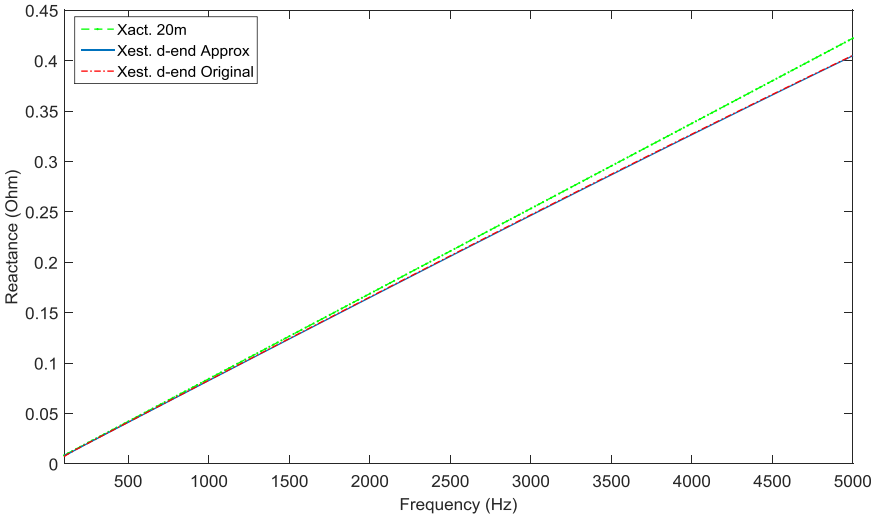
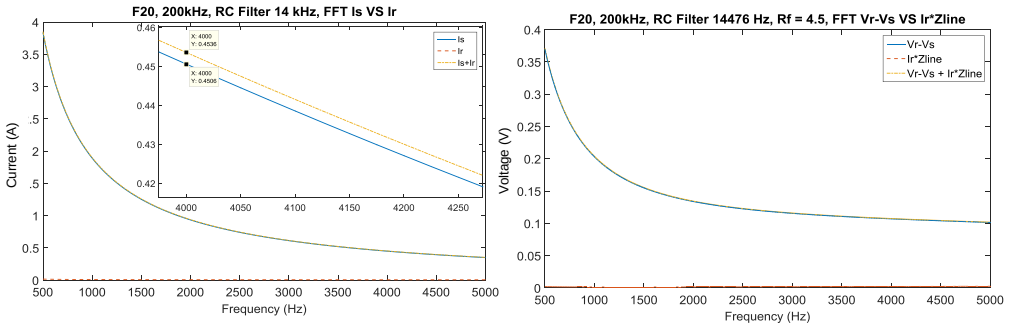


Figure 4-9 Estimated reactance using (3.2) versus (3.6) for fault at 10m



(a) (b)

Figure 4-10 Frequency domain representation of the measured signals for fault at 10m (a) Is, Ir and Is+Ir, (b) Vr-Vs, Ir*Zline, and Vr-Vs+Ir*Zline

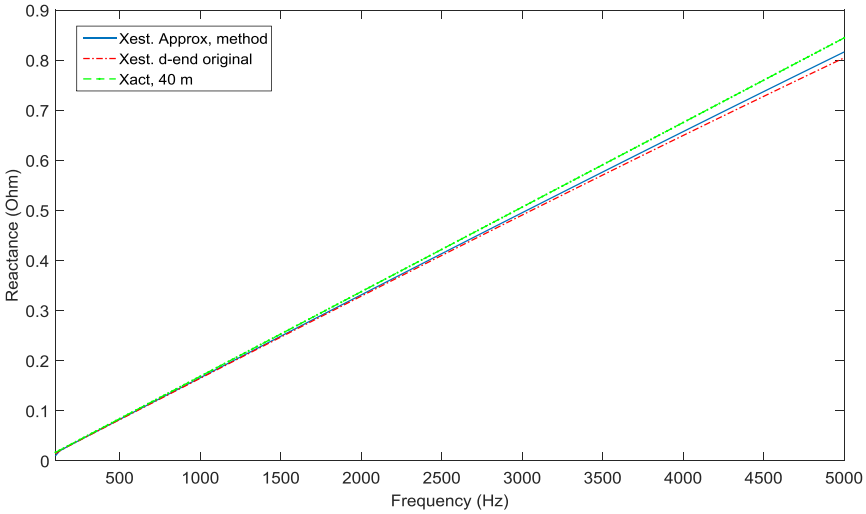
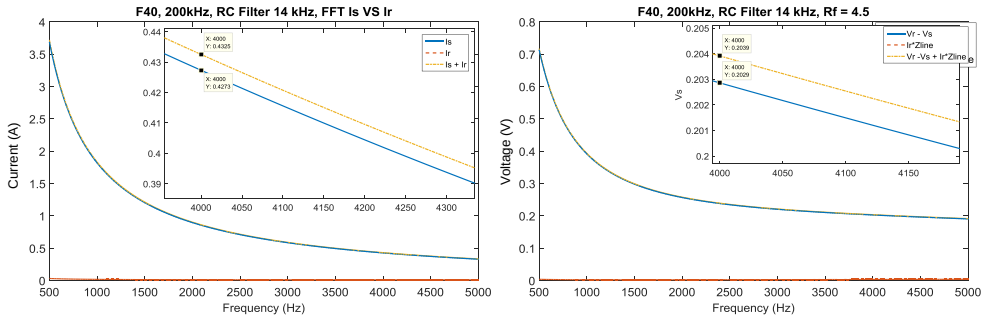


Figure 4-11 Estimated reactance using (3.2) versus (3.6) for fault at 40m



(a) (b)

Figure 4-12 Frequency domain representation of the measured signals for fault at 40m (a) Is, Ir and Is+Ir, (b) Vr-Vs, Ir*Zline, and Vr-Vs+Ir*Zline

A comparison of the distance and the percentage error estimated using the DEFLT with all the measurements against the DEFLT with three measurements is presented in Table 4-5. It is evident that the accuracy of the DEFLT with neglected Ir increases as the fault distance increases. this can be explained as the fault becomes closer the receiving end, the ignored current and voltage drop between the fault and receiving end drops which results in higher accuracy.

Table 4-5 Summary of the distance and percentage error estimated using two DEFLT approaches

Act. Fault	4 measurement DEFLT		3 measurement DEFLT	
	Est. dist,	Error (%)	Est. dist,	Error (%)
0	0.1	0.1	-1.44	-1.44
10	9.9	-0.2	9.1	-1.4
20	19.75	-0.5	19.1	-1.45
40	39.63	-0.75	39.34	-1.31
50	49.61	-0.78	49.6	-0.80

4.5 The DEFLT with tapped load compensation

This section explores the DEFLT with compensation for the tapped loads. The tapped load between the POM1 and the fault can be compensated by modifying the estimation algorithm. Consider Figure 4-13(a) where Z_{x2} is the impedance between the tapping point and the fault. I_T is the tapped-load current, and (4.4) can be derived:

$$Z_x = Z_{x1} + Z_{x2} = \frac{V_r - V_s + I_r * Z_{line} - I_T * Z_{x2}}{I_s + I_r} \tag{4.4}$$

I_T can be estimated assuming the voltage across the tap is equal to the source voltage according to (4.5):

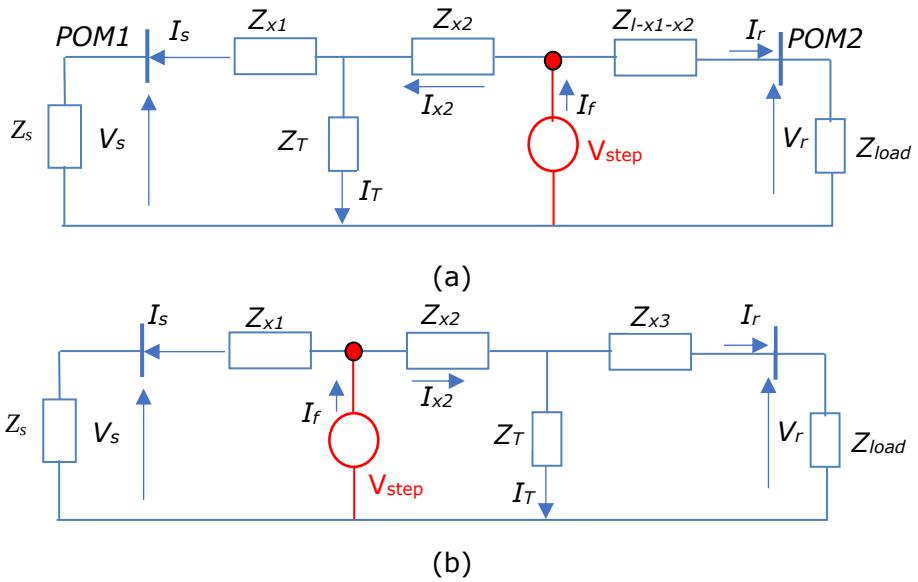


Figure 4-13 System at non-fundamental frequencies (a) tap between POM1 and fault (b) tap between fault and POM2

$$I_T = \frac{V_s + (I_s * Z_{x1})}{Z_T} \quad (4.5)$$

Z_{x1} is the impedance between POM1 and the tap point. If the tap is between the fault and the POM2 as in Figure 4-13(b), the estimation equation becomes (4.6), and IT calculated as in (4.7):

$$Z_{x1} = \frac{V_r - V_s + I_r * Z_{line} + I_T * Z_{x2}}{I_s + I_r} \quad (4.6)$$

$$I_T = \frac{V_r + (I_r * Z_{x3})}{Z_T} \quad (4.7)$$

This new technique (the DEFLT with tapped load compensation) is processed as follow:

1-Initial distance (d_0) estimation based on the non-compensated DEFLT (3.2) in order to locate the fault with respect to the tap position.

2- Using the pre-fault voltage and current measurements, the total load is estimated as ($Z_{total} = \frac{V_s(f)}{I_s(f)}$) while the receiving end load is estimated from the receiving end measurements as ($Z_{load} = \frac{V_r(f)}{I_r(f)}$). The tapped load is then calculated by ($Z_T = \frac{Z_{total} * Z_{load}}{Z_{load} - Z_{total}}$).

3- Using the knowledge of the tap location to select a compensation technique.

(a) Fault after the tapped load, I_T is estimated based on the calculated distance using (4.5).

(b) Fault before the tapped load, I_T is estimated based on the calculated distance using (4.7).

4- Calculate Z_{x2} based on the calculated distance (d_{k-1}).

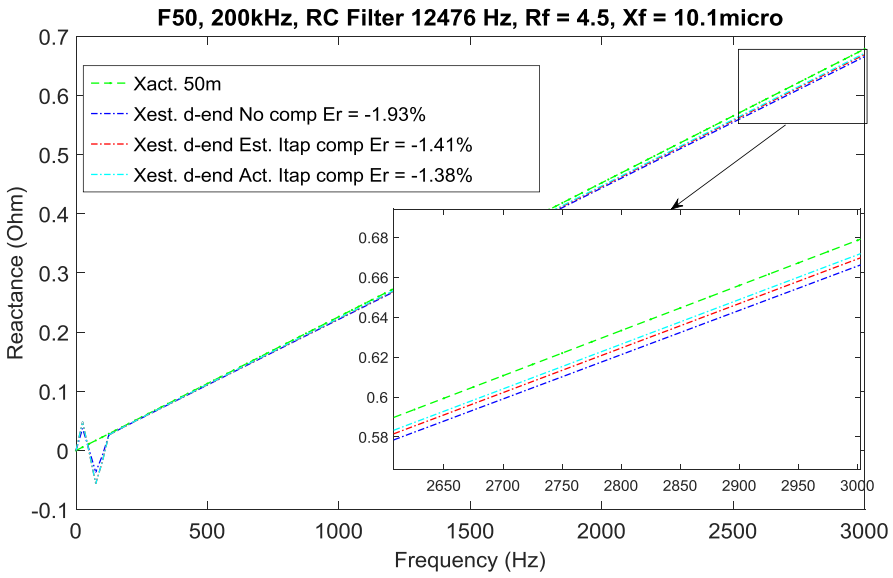
5- Calculate $I_T * Z_{x2}$.

6- Calculate new Zx (impedance between the POM1 and the fault).

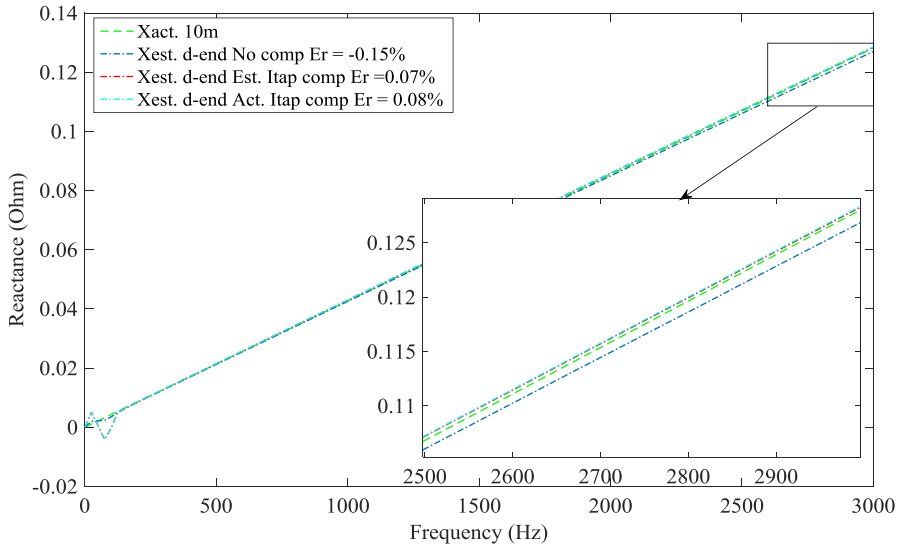
7- Divide Z_{x2} by the per-meter impedance of the line and then average the result in order to find a new distance d_k.

8 – Repeat steps 2 to 7 until the pre-set tolerance converges (d_k - d_{k-1} < 0.5m).

To test this algorithm, two faults have been imposed with only one tapped load (10Ω) connected 20m from the source end. The receiving end load is 37Ω, and the fault resistance is 4.5Ω in order to demonstrate the derived theory. The first fault test is between POM2 and the tapped load. The estimated reactance for this test is presented in Figure 4-14(a). This Figure shows the compensated DEFLT (dash-dotted red line) and is compared to the non-compensated DEFLT (Blue dash-dotted line). There is clear compensation in the high-frequency range (2-3 kHz). The other test is for faults between the tap position and POM1. The estimated reactance for F10 is presented in Figure 4-14(b). The dash-dotted red line is with tapped load compensation, and the dash-dotted blue line is without compensation. Moreover, the reactance estimated using estimated I_T is compared to the estimation using actual tapped load current measured from the simulation. In both cases, the compensation is very close to the actual estimation, which verifies the effectiveness of the compensation algorithms.



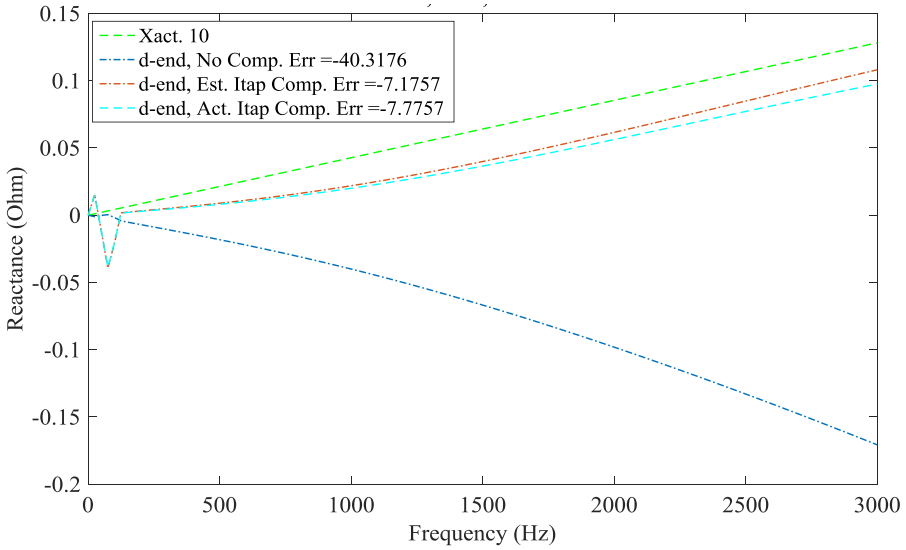
(a)



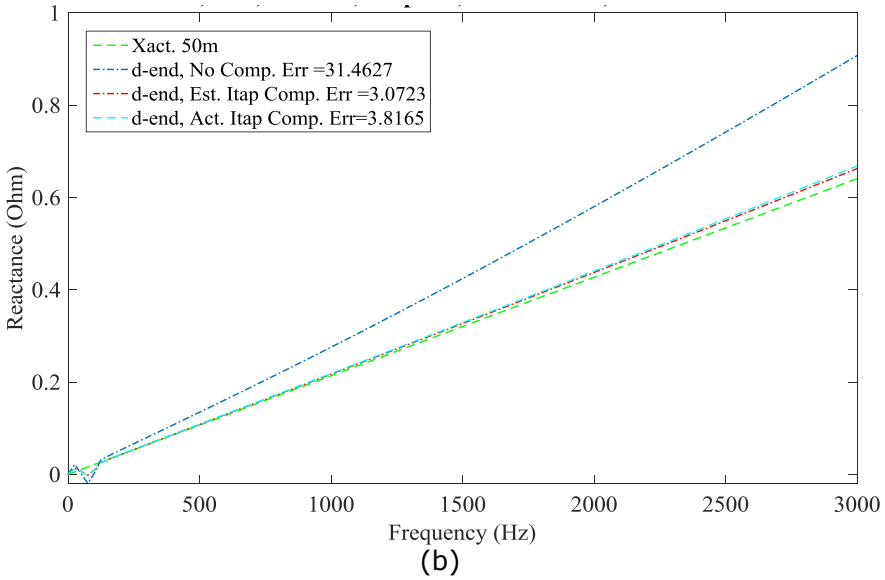
(b)

Figure 4-14 Reactance estimated with tapped load compensation (a) F50 (b) F10

Further investigation is performed by increasing the source resistance to 0.1+0.314jΩ in order to limit the fault current, whereas the fault resistance, the tapped load, and the receiving load are kept the same. Two faults are imposed at F10 and F50 separately, and the reactances estimated are summarised in Figure 4-15. The percentage error (of the full line length) is increased as the source impedance increases, especially with the fault close to the source end as presented in Figure 4-15 (a).



(a)



(b)

Figure 4-15 Reactance estimated with and without tapped load compensation (a) F10, (b) F50

Table 4-6 Estimated distance and percentage error for compensated and non-compensated d-ended method for fault 50m with various Z_{tap}

Z_{tap}	Act. Dist. (m)	Est. dist. No comp.	Error (%)	Est. dist. comp.	Error (%)	Error (%)
17.5	50	58.04	16.09	50.75	1.51	1.8
13		60.84	23.68	50.75	1.50	2.2
10		65.9	31.4	51.53	3.07	3.81
6.5		75.95	49.89	48.09	3.66	-5.23
4		91.72	83.44	47.55	6.46	10.0

Table 4-7 Estimated distance and percentage error for compensated and non-compensated d-ended method for fault 10m with various Z_{tap}

Z_{tap}	Act. Dist. (m)	Est. dist. No comp.	Error (%)	Est. dist. comp.	Error (%)	Error (%)
17.5	10	-15.3	-30.6	7.55	-4.9	-4.6
13		-17.9	-35.4	7.45	-5.5	-5.68
10		8.4		6.43	-7.14	-7.73
6.65		-26.0	-52	4.95	-8.1	-8.0
4		-36.5	-73.0	5.0	-10.0	-12.4

The proposed compensation technique for the error caused by the neglected tapped current was compensated correctly (as shown by the dash-dotted red line), which is closer to the actual value (dashed green line). Moreover, the actual tapped current measured from the simulation and used in (4.4)

and (4.6) yields a very close estimation to the algorithm when the tapped current is estimated using (4.5) and (4.7). A comparison between compensated and non-compensated DEFLTs with different tapped impedance values are summarized in Table 4-6 for the fault on the receiving end and Table 4-7 for the fault 10m from s-end using Zs =0.1+0.314jΩ. Both tables show as the tapped resistance decreases (load increases), the estimation error increases using the non-compensated technique.

On the other hand, the compensated technique shows a bigger compensation as the tapped load increases. Moreover, the compensation using estimated tapped current (as described earlier in point 2) in is very close to the estimation using actual measured tapped load, which demonstrates accurate tapped current estimation using (4.5) and (4.7). In conclusion, the d-ended algorithm with tapped load compensation offers a robust and accurate compensation for the neglected tapped load. Different faults tested with different conditions verified the proposed technique even with a high ratio of tapped load current to source end current as well as the ratio of the tapped load to receiving end load.

4.6 The influence of DG on the DEFLT

In recent years, increased attention has been directed to the development and use of renewable energy sources. The current distribution system a large penetration of inverter-based DG such as solar cells and wind energy. Therefore, the influence of an inverter-based DG on the proposed DEFLT will be investigated and demonstrated in this section.

4.6.1 DG modelling

A grid-connected PWM inverter has been simulated to represents an inverter-based DG as shown in Figure 4-16. Figure 4-16 represents the basic structure of the grid forming power converter [85]. A Proportional and Integral (PI) current controller working in the dq reference frame is used to control the output power of the DG in order to limit the output to the rated power during fault condition. The parameters used for this model are given in Table 4-8. The operation of the DG is tested during normal and abnormal conditions. The controller response in both conditions is shown in Figure 4-17 while a sample of the grid-connected converter output after filtering with RC filter is presented in Figure 4-18. It is clear from Figure 4-17 and Figure 4-18 that the converter works as required during normal and abnormal conditions with a minimal distortion in the grid current. This can be further reduced by designing a proper LCL filter to replace the coupling impedance ($Z_{coupling}$ = 0.001+0.910j). The simulated converter behaviour is then typical of DG performance [86].

Table 4-8 DG parameters

Parameter	**Value**
V_{dc}	1.2 × $V_{L\text{-}L(grid)}$
Coupling impedance	0.001+0.910i
Proportional gain	2.663
Integration gain	395
Carrier frequency	10 kHz

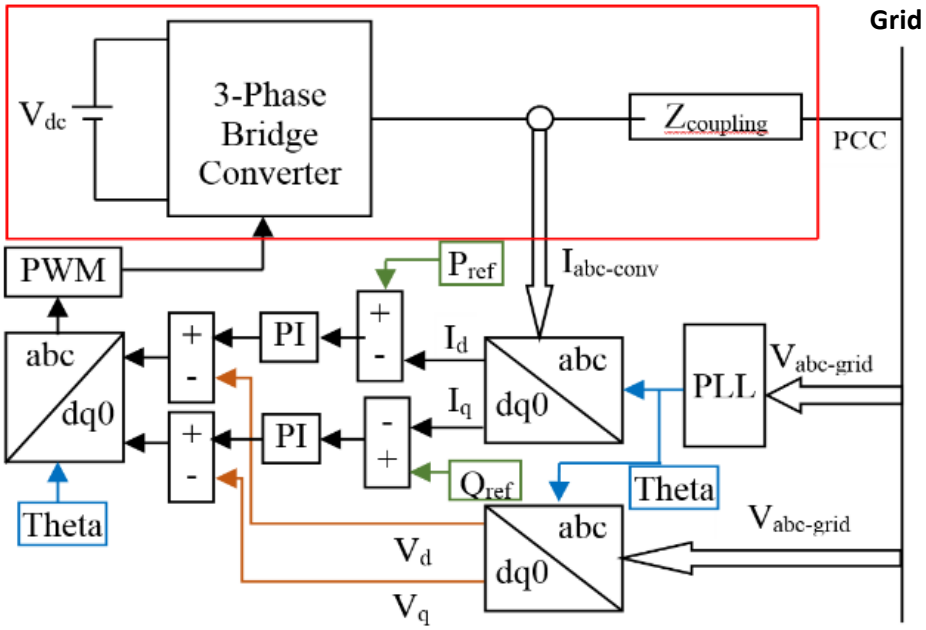
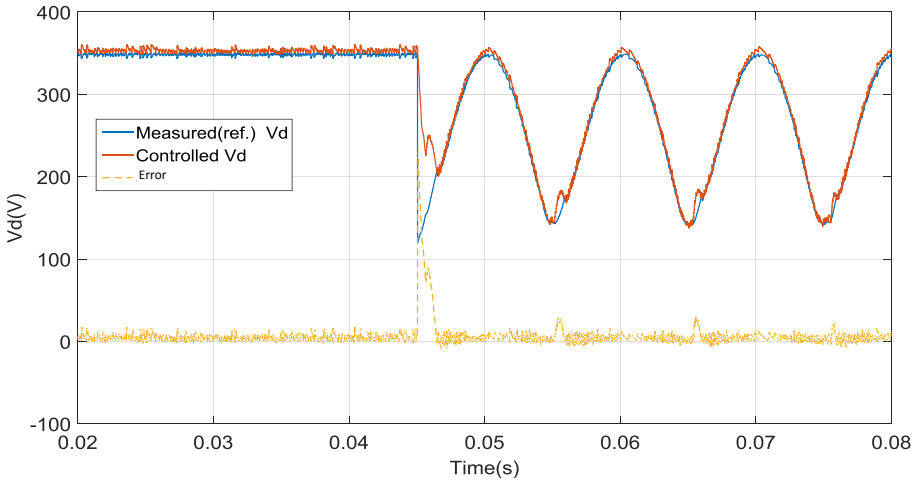
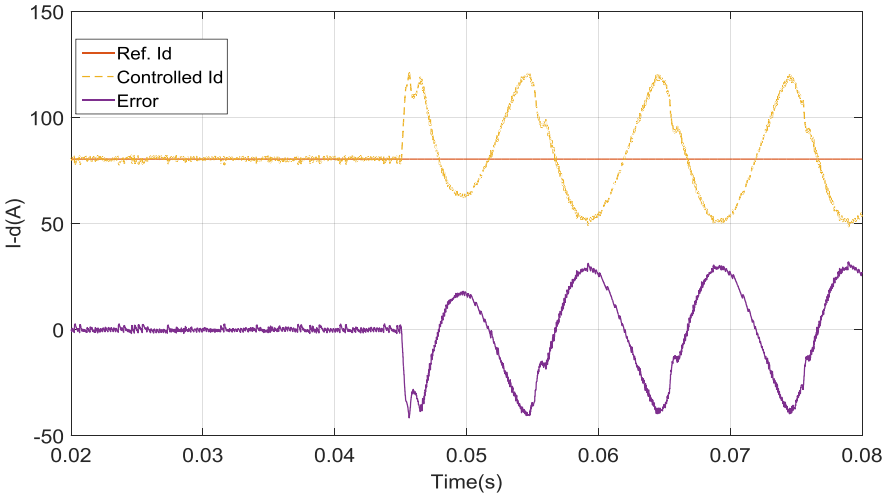


Figure 4-16 Basic structure of grid-connected power converter



(a)



(b)

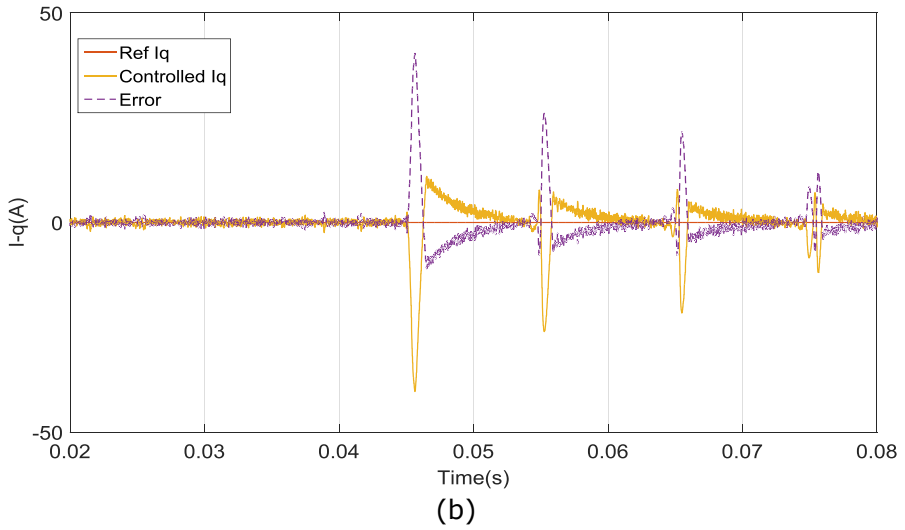


Figure 4-17 Controller parameters during a short circuit condition (a) d-axis current (b) q-axis current (c) d-axis Voltage

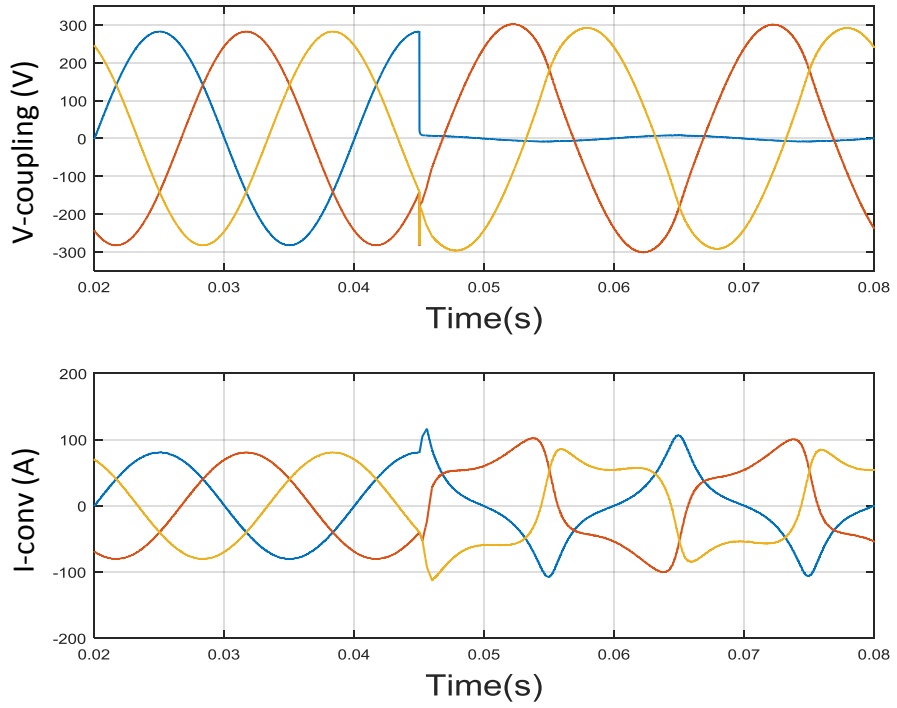


Figure 4-18 Grid-connected inverter output voltage after the coupling impedance versus the converter current during a short circuit condition

4.6.2 Demonstration of DG behaviour

In this section, the influence of the Modelled DG on the DEFLT will be shown. Therefore, the system used in section 3.2 of Figure 3-10 is used here but with inverter-based DG included as shown in Figure 4-19. The DG model is shown in Figure 4-20.

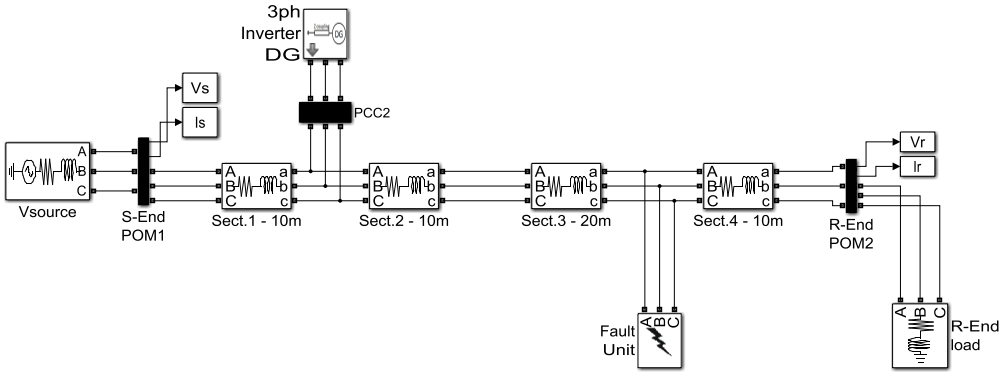


Figure 4-19 Simulated IPS with Inverter based DG

Different fault types with different DG scenarios are proposed to validate the influence of the DG on the higher harmonic content of the DEFLT. The first scenario is to place a 2kW DG 10m from POM1 whereas the nominal system load is 3kW. A single line-to-ground (SLG) fault is applied to four locations downstream, and upstream of the DG which are 0.0m, 20m, 40 and 50m. The reactance estimated is then plotted on the same figure for the scenario without DG in the system for comparison and analysis. The summary of the four fault locations is presented in Figure 4-21. The DG shows an apparent effect over a frequency range of 2-3 kHz as marked by the solid lines with blue, orange, and green colours.

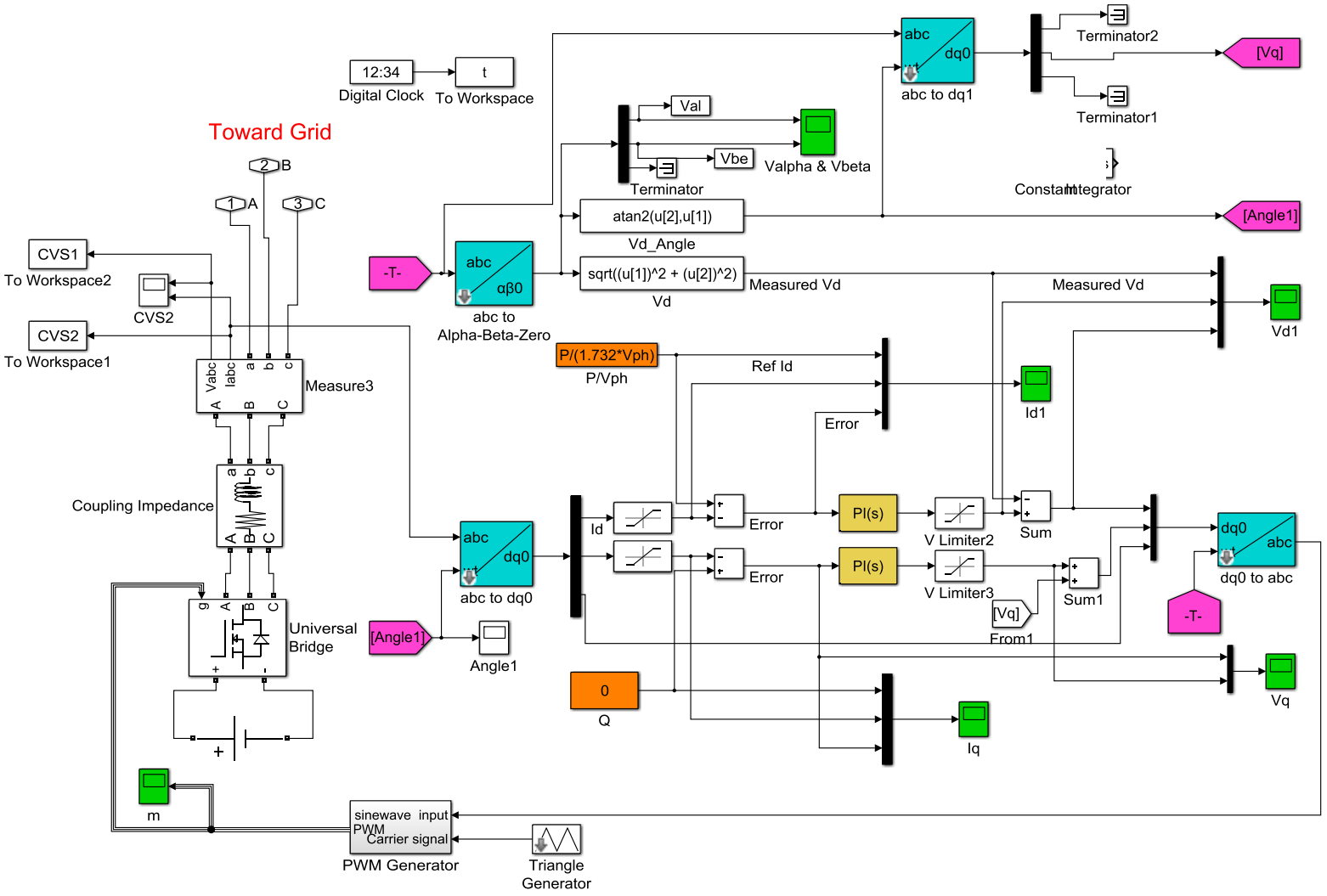


Figure 4-20 DG model

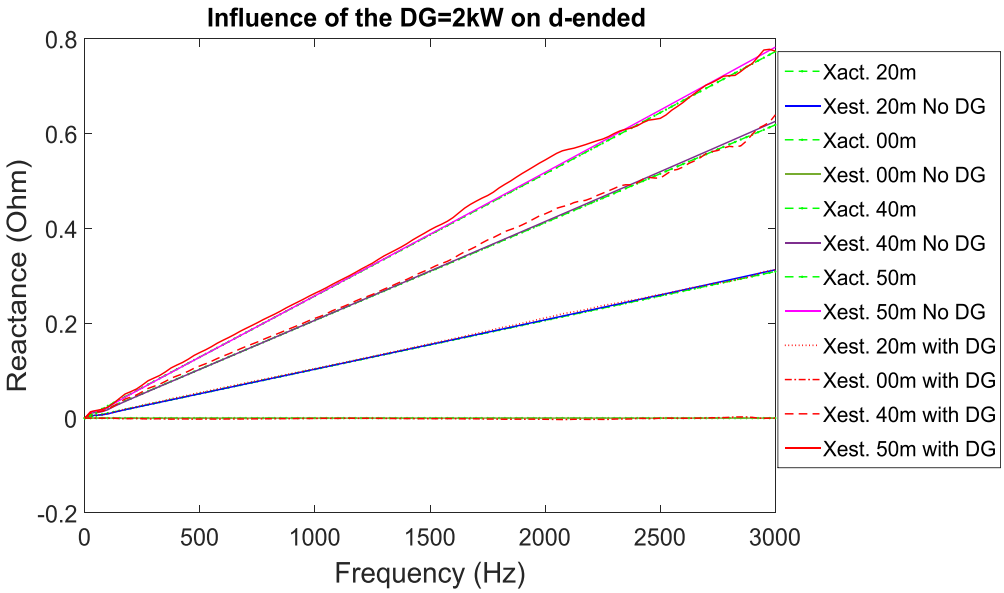


Figure 4-21 Estimated reactance with and without DG supply

However, the effect is not significant for the case without DG plotted in dash-dotted red lines. The percentage error calculation given in Table 4-9 shows a small increase because of the DG presence and contribution to the fault current. The reactance is estimated using (3.2), and then the distance is calculated using the average of the divided (3.2) result by the line per-meter impedance.

Table 4-9 Error (%) for the d-ended method with and without 2 kW DG

Actual Fault distance (m)	Estimated dist. Without DG (m)	Error (%)	Estimated dist. With DG (m)	Error (%)
0.0	-0.0038	-0.007	-0.19	-0.38
20	20.083	0.17	20.35	0.75
40	40.18	0.36	40.91	1.835
50	50.23	0.45	51.31	2.62

The DG supplied current transient has been converted to the frequency domain and normalized to the actual value in order to understand the reason behind this outcome. Figure 4-22 shows that the inverter-based DG has a

small contribution to harmonic content of the current between 1500 – 3000 Hz, but is larger for the frequency range lower than 1500 Hz. This neglected DG transient current resulted in the pattern of the estimated reactance using the DEFLT. This is for a DG which supplies 2 kW power of the 3kW system nominal load power.

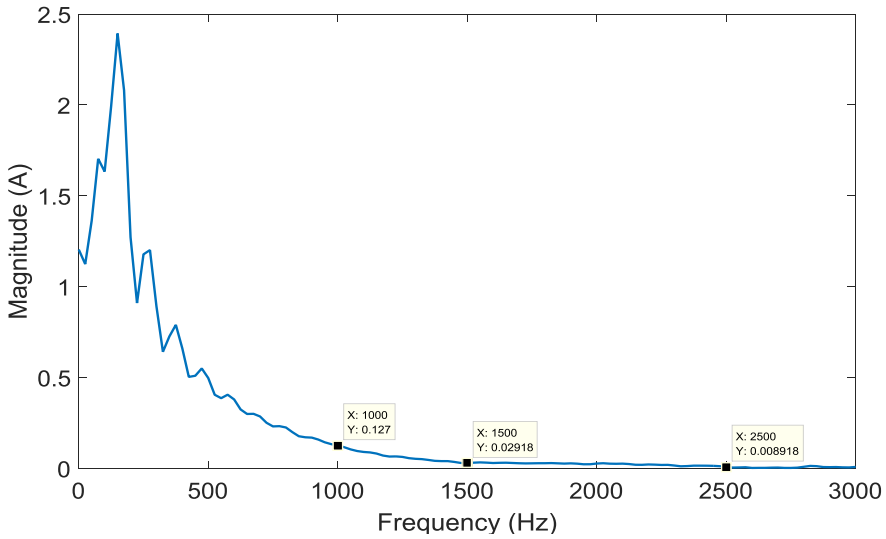


Figure 4-22 frequency content of the utilized DG during fault transient

The second scenario for further investigation is to study the influence of the supplied power by the DG. Thus, the DG is placed 20m from POM1, and the DG power increased from 200 W to 2 kW in steps. A SLG fault at the load terminal is used to study this case. The estimated reactance using (3.2) for all DG supplied power is plotted and presented in Figure 4-23. The green dashed line is the actual fault reactance, while the other lines are the estimated reactance with the various levels of DG in the system. Figure 4-23 at frequencies over 2 kHz shows a small change in the reactance estimated with each DG power increases while there is a lower effect at lower frequencies. The percentage error calculation showed that the error is only increased by 0.15% when the DG power level is changed. The maximum error became 2.6% which is very reliable for such a system and condition.

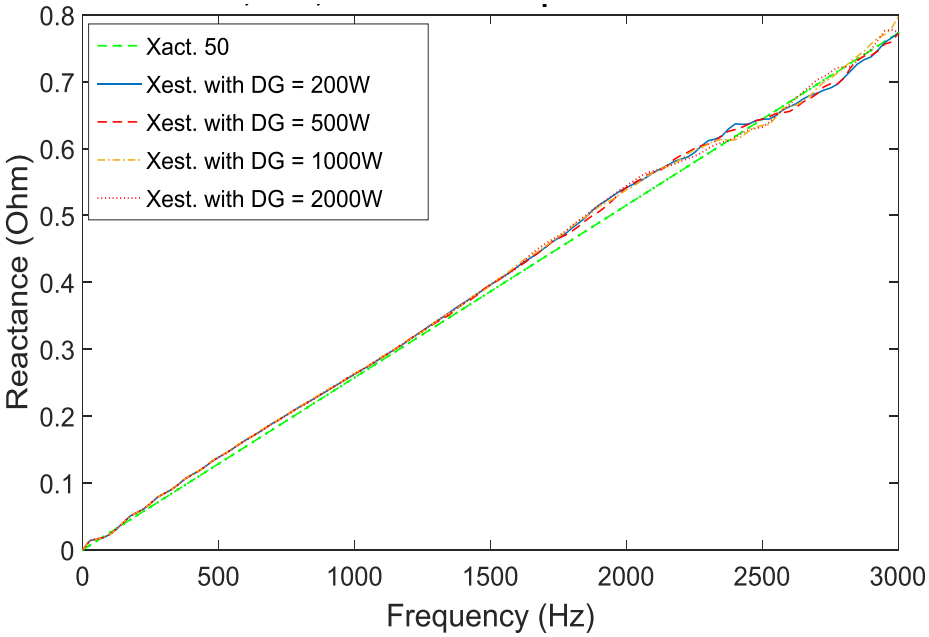


Figure 4-23 Estimated reactance with different DG power levels

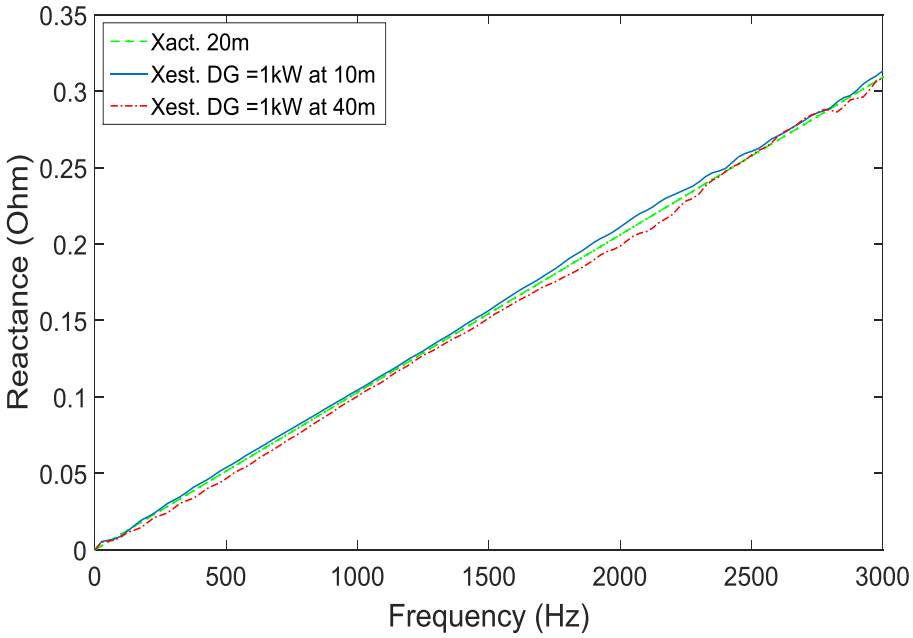


Figure 4-24 Influence of DG location on the DEFLT

The last scenario is to study the influence of the DG location on the DEFLT of equation (3.2). Hence, for the same fault, the DG is placed Upstream (DG between POM1 and fault) and then moved to Downstream (DG between POM2 and fault). Figure 4-24 shows the estimated reactance for a SLG fault 20m from POM1. The difference between the two cases is very small as

marked by the dash-dotted line for a DG at 40m from POM1 while the solid blue line for DG at 10m from POM1. The percentage error is changed by 1.5%. The DG supplies 2kW power, which represents almost half of the load demand.

Further simulation is performed to demonstrate the impact of the DG with higher supplied power. Therefore, the system parameters used are changed as follows: the line parameters are changed to 30μΩ/m resistance and 0.24μH/m inductance in order to use a higher load. The load is set to 100kW, and the DG supplied power is also changed to 50kW. The first scenario is to place a 50 kW DG 10m from POM1. A SLG fault is applied to three locations upstream of the DG which are 20m, 40 and 50m. The reactance estimated is then plotted on the same figure in addition to the case without DG in the system for comparison. The summary of the three fault locations is presented in Figure 4-25. The DG shows a clear effect in the frequency range of 2-3 kHz as marked by the solid lines with blue, orange, and green colours.

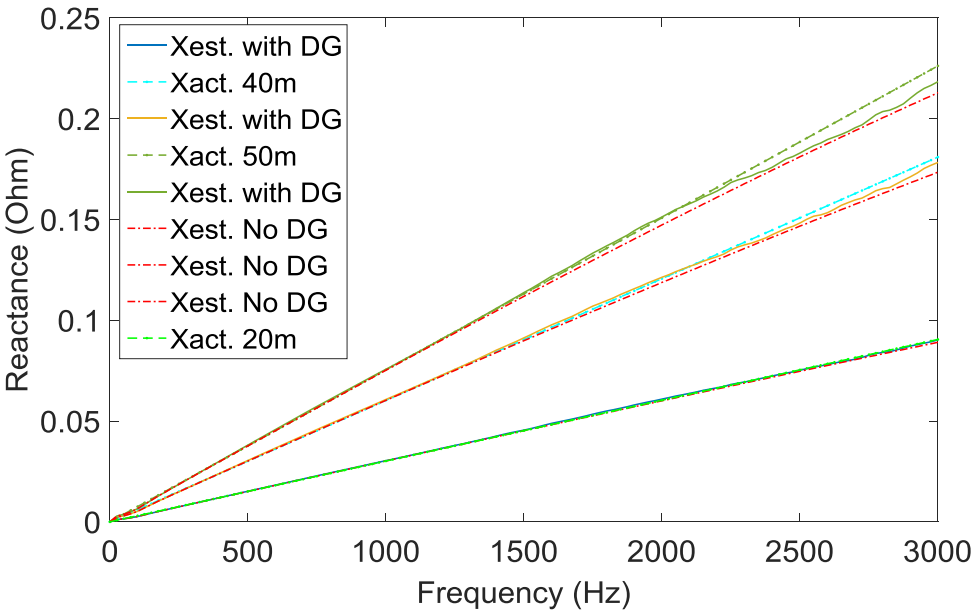


Figure 4-25 Estimated reactance with and without DG at different fault locations

Similarly, the effect is not significant for the case without DG plotted in dash-dotted red lines, the percentage error calculation given in Table 4-10 shows a larger error due to the DG presence. The reactance is estimated using (3.2), and then the distance is calculated using the average result divided by the line per-meter impedance.

Table 4-10 Error calculation for the DEFLT with and without DG

Actual Fault distance (m)	**Estimated dist. Without DG (m)**	**Error (%)**	**Estimated dist. With DG (m)**	**Error (%)**
20	20.083	0.16	20.083	0.16
40	39.44	-1.1	39.99	-0.01
50	48.98	-2.04	49.71	-2.56

The DG supplied current transient has also been converted to the frequency domain and compared to the current supplied by an ideal DG (controlled ideal voltage source, see Appendix A - Ideal DG) to understand the reason behind this outcome. The zoomed part of Figure 4-26 shows that the inverter-based DG (Real DG in orange line) has small higher harmonic supplied current compared to the ideal DG (in blue line) which has zero supplied current at the higher harmonic due to the absence of the electronic components. Both have the same fundamental magnitude, but the inverter-based DG also shows some supplied current in frequency range less than 1kHz due to electronic components used to construct the inverter.

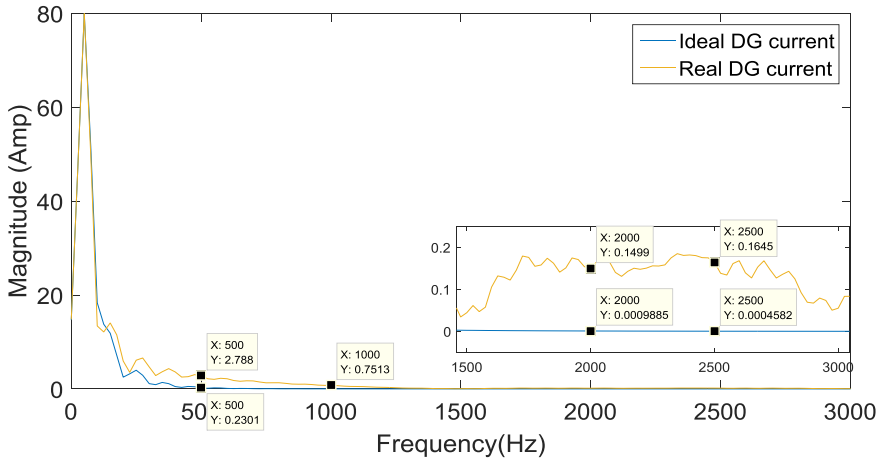


Figure 4-26 frequency content of the utilized DG during fault transient

The second scenario for further investigation is to study the influence of the DG supplied power. Thus, the DG is placed 20m from POM1 and the power varied from 15kW to 100 kW in four steps to supply a nominal system load of 100kW. A SLG fault at the load terminal is used to study this condition. The reactance estimated using (3.2) for all DG supplied power is plotted and presented in Figure 4-27. The green dashed line is the actual fault reactance, while the dash-dotted line is the estimated reactance with the DG compared to the solid red line for the reactance estimated without DG in the system. The zoomed part of Figure 4-27 at frequencies over 2 kHz shows small changes in the estimated reactance with each DG power change while there are fewer changes at lower frequencies. The percentage error calculation showed that the rate of change is only 1% and the maximum error is 2%, which is very reliable for such a system and condition.

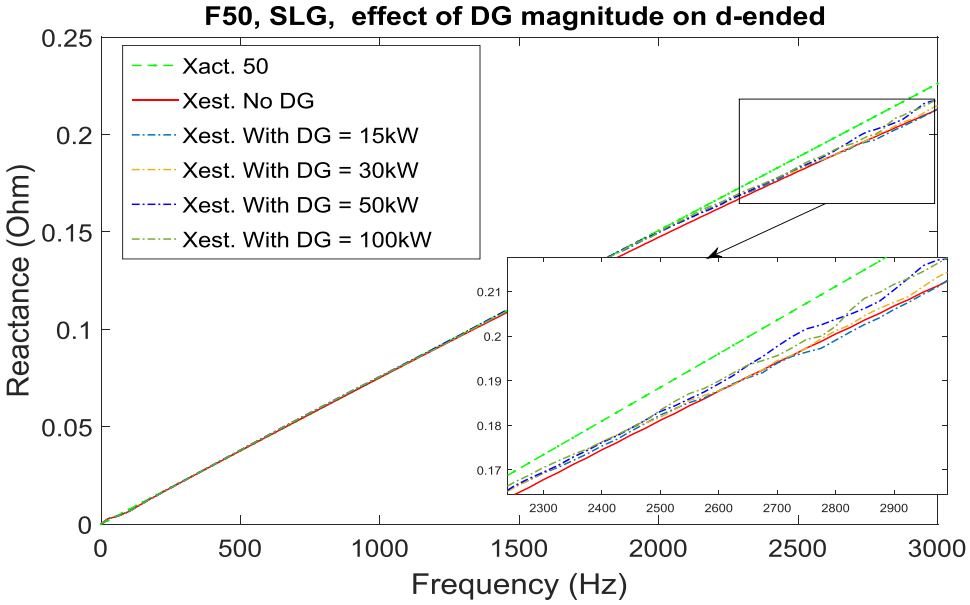


Figure 4-27 Estimated reactance with different DG supplied power

The last scenario is to study the effect of the DG location on the proposed DEFLT using (3.2). Hence, for the same fault, the DG is placed upstream and then moved to Downstream. Figure 4-28 shows the reactance estimated for

SLG fault 20m from POM1. The difference between the two cases is very small as marked by the two dash-dotted lines but with red and blue colours.

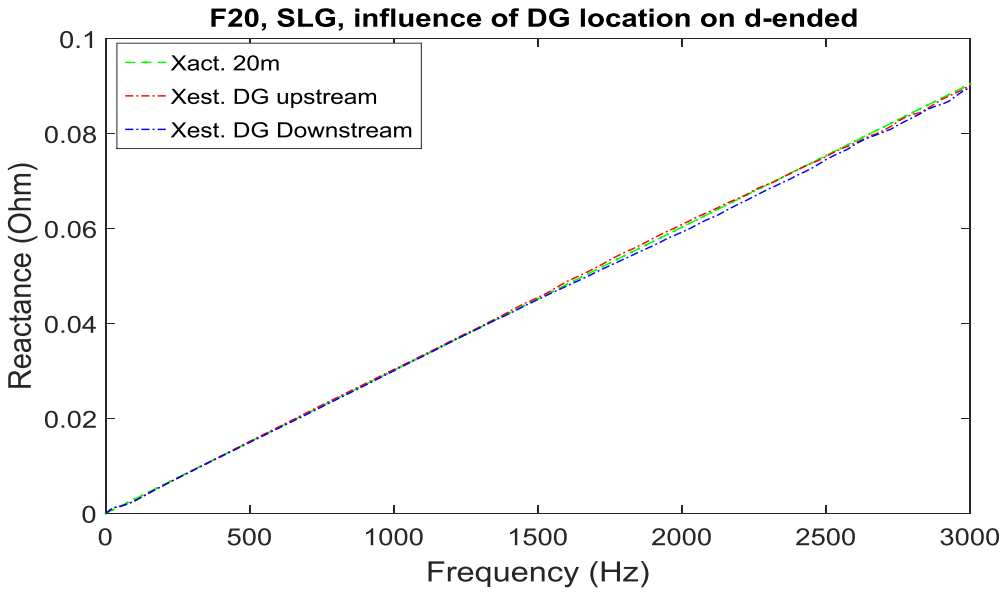


Figure 4-28 Influence of DG location on the double-ended method

Finally, the study of the inverter-based at two different system rates showed that the DG has a small adverse impact on the DEFLT. The maximum percentage error increased by 2% compared to the condition without the DG presence in the system. Another interesting finding is that the DG location also showed a very small negative effect on the DEFLT. This can be explained as the internal control loop of the inverter limits the fault current during any fault condition which results a very small higher harmonic injected by the fault transient compared to the methods presented in section 2.3 which showed that neglecting the DG current at fundamental frequency will have a significant adverse influence on the proposed methods. They also showed that the effect level is proportional to the level of the injected current by the DG, while the investigated DEFLT is not significantly affected by the Level of the DG current as seen in Figure 3-40.

4.7 Summary

In this chapter, a thorough evaluation of DEFLT in an IPS/Microgrid was performed. Based on the fundamental approach which derived using a simple power circuit in chapter 3. A few factors that could affect the method (such as fault resistance, source impedance, system noise and tapped loads/lines) are studied and demonstrated through simulation. The DEFLT with tapped load compensation is then proposed and demonstrated. Moreover, the DEFLT with ignored receiving end current is proposed and verified. Finally, the effect of DG on the studied technique is investigated. None of these effects were stated in [11].

The investigation shows that the fault resistance has a limited effect on the DEFLT. The tapped-load has little influence on the fundamental fault locating algorithm when the ratio Z_{tap}/Z_r is less 50%. The addition of 40% tapped load resulted in 2% increases in error for the d-ended estimation. However, when the ratio is increased by more than 100%, the error increased to more than 8%. Therefore, the tapped load has a small influence on the d-ended method and can be neglected when its value is less than the receiving end load. Moreover, the source impedance plays a vital role on the accuracy of the d-ended method because the generated fault transients decrease as the source impedance increases, which limits the useful wideband frequency in the measured transients. Thus, the DEFLT offers high accuracy with error is less than 6% if the Z_s/Z_r ratio is less than 15% as well as a low source inductance. Furthermore, a compensation approach is developed to compensate for the tapped load in case the ratio of the tapped current to the source end current is high. The simulation results showed that the approach worked accurately and reduced the error caused by the tapped load. The main drawback of DEFLT is that it is not able to locate faults on a

tapped line. However, the method can locate the faulted tapped line, which could be disconnected to keep the power supply to the rest of the system.

Finally, the DEFLT is also investigated with the addition of a second power source. An inverter-based DG has been simulated for this aim. This DG is then connected to the distribution line, and the DELFT is tested with various scenarios such as the DG location and DG power level. The simulation results showed that the proposed DEFLT has a high estimation accuracy considering that the DG supplied up to 50% of the load and the DG current is neglected in the estimation algorithm. Additionally, the DG connection position with respect to the fault location has limited influence and the error could increase by 0.5%. The maximum error added by neglecting the DG current is less than 3% for the simulation undertaken. This is emphasis the important of the used wideband approach for modern IPS/Microgrid where high penetration of inverter-based DG is predicted. This is because the inverter-based DG inject a limited magnitude of current at higher frequencies during fault which results in a minimal effect on the proposed wideband DEFLT.

Chapter 5 - Single-Ended Fault Location Technique (SEFLT)

5.1 INTRODUCTION

In this chapter, the single-ended impedance-based fault location technique (SEFLT) introduced in chapter 3 will be thoroughly evaluated using a more complex IPS/Microgrid. The study will start with factors that could affect the proposed estimation algorithm, such as the presence of tapped loads, measurement noise, the tapped lines/loads, and DG. These were not investigated in [10]. Then, a proposed technique to overcome some of the issues imposed by these factors is introduced and verified.

5.1.1 The effect of measurement noise on the SEFLT

The investigations, as mentioned in section 3.2, were performed without considering any realistic factors for the electrical system. Hence, in this section, the SEFLT is evaluated considering the effect of the measurement noise using the same circuit in Figure 3-17 . Firstly, Gaussian white noise is included in the measured signals from the simulation to represent equipment noise. Figure 5-1 shows the measured voltage and current signal at the source end with and without 2% of Gaussian noise (2% of the RMS value of the original data). The blue line is the original signals without noise and the red (or orange) lines when the noise is added to the measured signals.

A SLG fault is applied 20m from the source end with the measured signals with noise added. The estimated reactance is shown in Figure 5-2 and compared to the original case without the Gaussian noise. There is a clear difference between the two conditions at frequencies higher than 1500 Hz. The blue line is without the noise while the red line is with Gaussian noise.

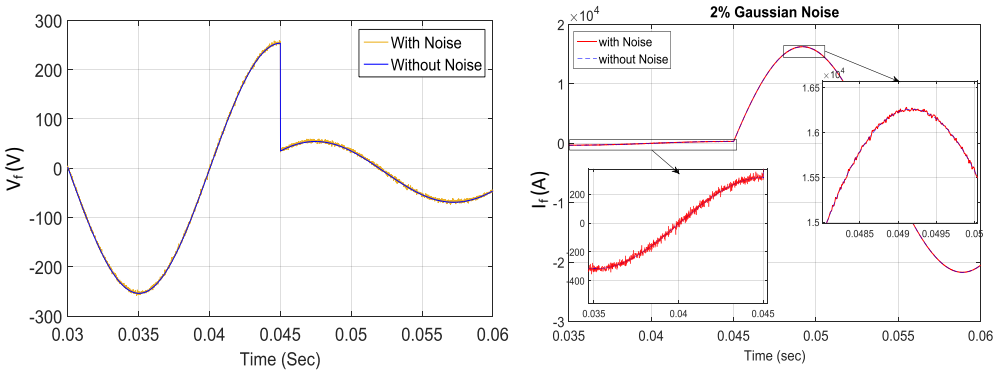


Figure 5-1 Measured voltage and current with Gaussian noise

The error calculation based on (3.4) where curve fitting is used to fit the data with Gaussian noise to a first order least square curve, shows the error increases to 2.8%. Another fault test was carried out at the load-end and is presented in Figure 5-3, and shows similar behaviour because of the measurement noise. The maximum error after the curve fitting is 4%. The main reason for this behaviour is that the SNR at higher frequencies reduces significantly, which results in this evident fluctuation in the estimations. As the noise is Gaussian, the effect is "smoothed" when the first order least square root curve fitting is applied.

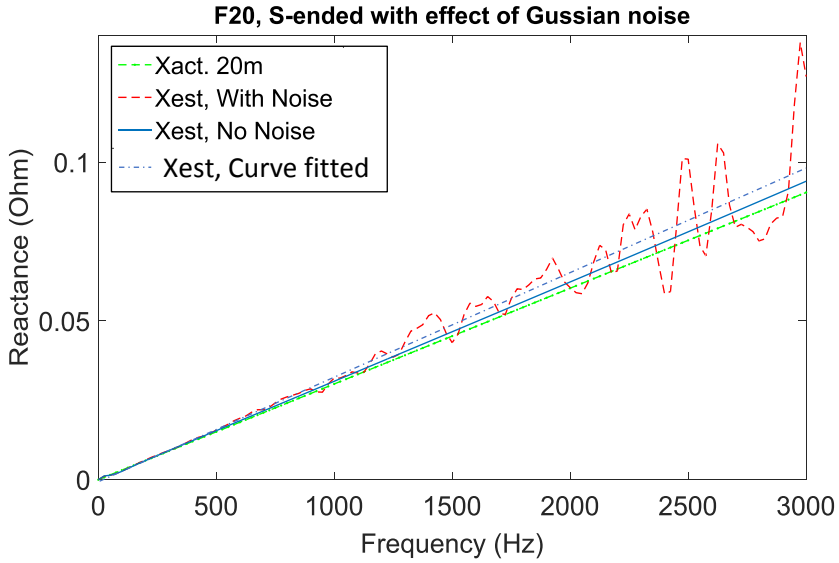


Figure 5-2 Single-ended reactance estimation with measurement noise – fault at 20m from POM1

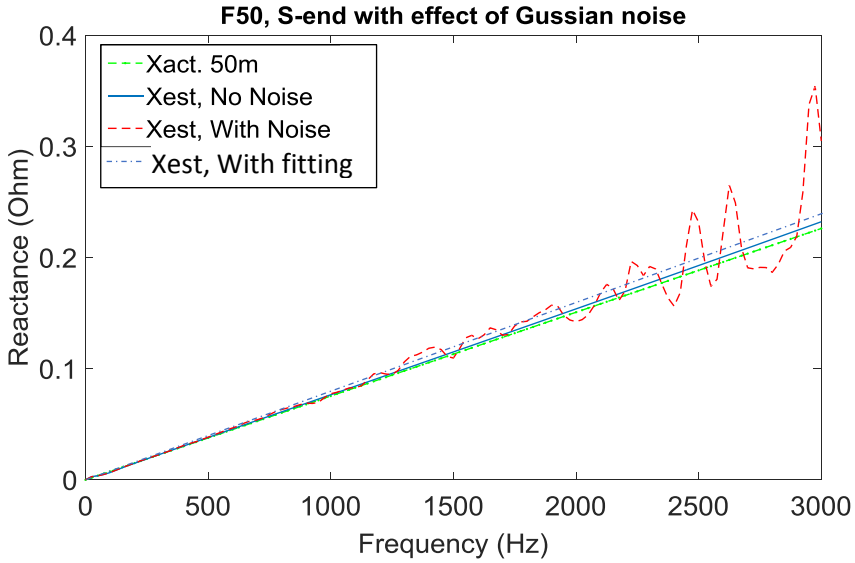


Figure 5-3 Single-ended reactance estimation with measurement noise, fault at the load-end

To investigate further, the Gaussian noise is reduced gradually to examine the performance of the single-ended method for a SLG fault at the load-end. The estimated reactance outcomes with the noise of 2%, 1%, 0.5%, and 0.1% are presented in Figure 5-4, which indicate that fluctuation reduces as the noise is reduced. The registered percentage error is reduced by 1.5% when the noise reduced, moving from 2% to 0.1%. Some error is present due to the neglected load current.

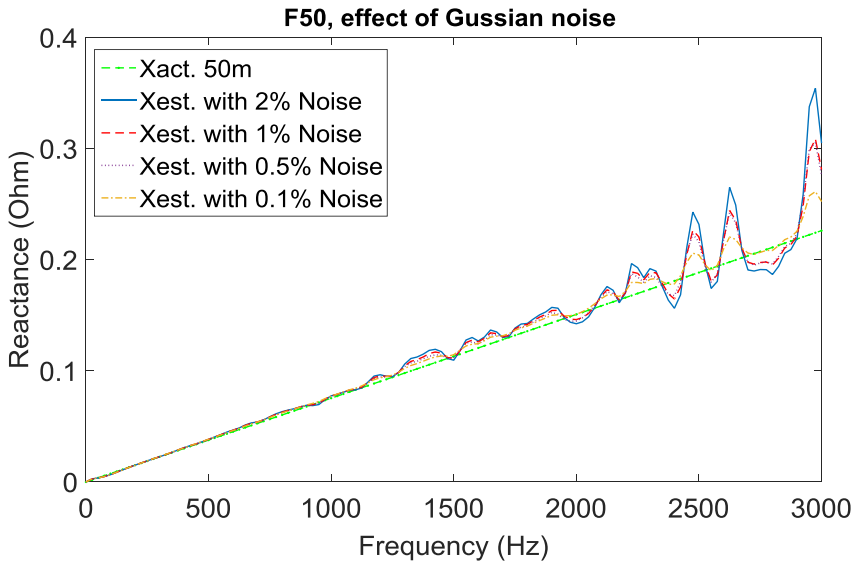


Figure 5-4 Reactance estimated with amount various measurement noise

The quantization noise associate with the Analog-to-Digital Converter (ADC) also been studied. A 10-bit and 12-bit ADC quantization have been used to test the performance of the SEFLT as these are commonly found in existing data acquisition units for power systems. An example of the output of a 10-bit ADC is shown in Figure 5-5, and it is compared to the ADC input. Figure 5-6 summarizes the estimated reactance for the two cases and indicates that the 12-bit ADC imposes lower error due to smaller step size, which results in lower added quantization error. The fault is 20m from the source end, which is similar to the fault estimation shown in Figure 5-2.

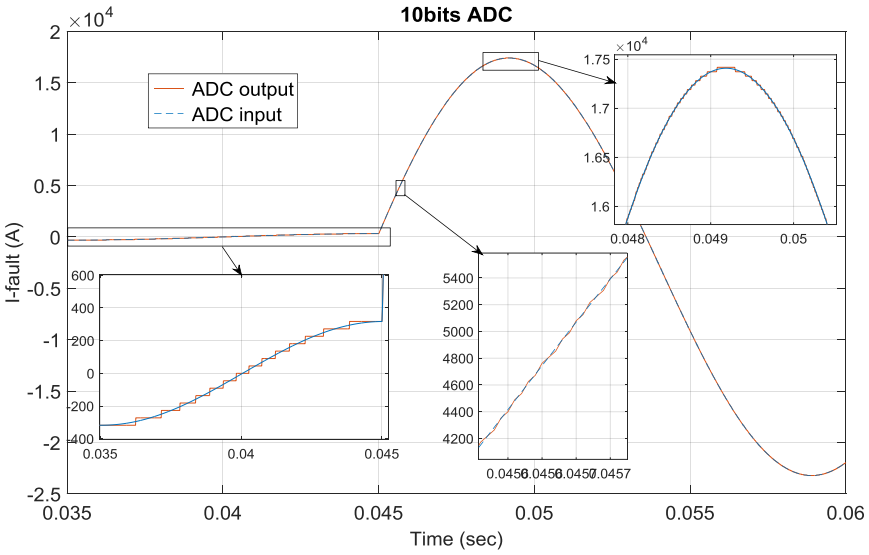


Figure 5-5 Input and output of a 10-bit ADC

In conclusion, the presence of the measurement noise will have an adverse impact on the proposed SEFLT, especially at high frequency range as the SNR will drop. The data acquisition unit will have a similar behaviour due to the ADC quantization noise. The magnitude of the added error is affected by the bit rate of the used ADC. However, the 12-bit ADC showed an acceptable accuracy.

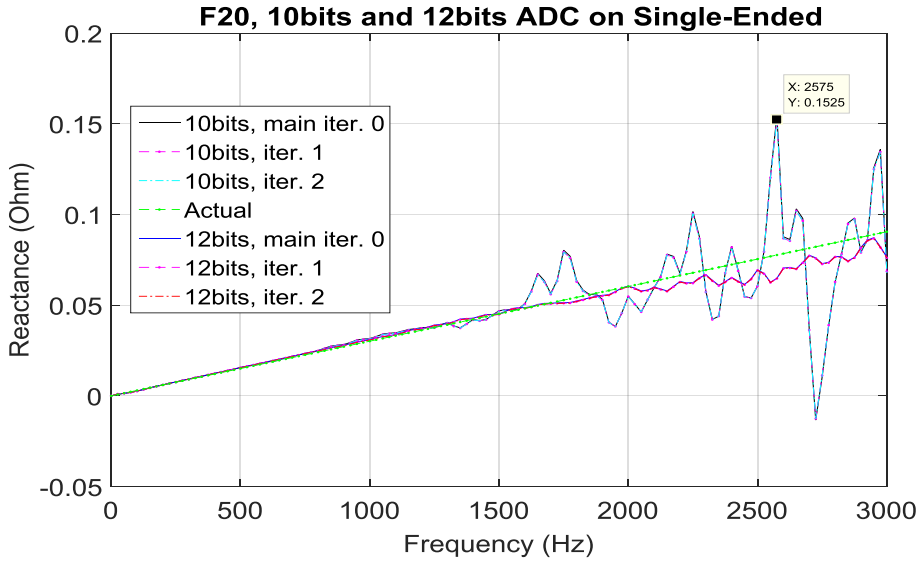


Figure 5-6 Estimated reactance with the effect of ADC quantization noise

5.1.2 Influence of tapped load on SEFLT

In this section, the performance of the SEFLT is investigated with the presence of tapped loads between the source and receiving ends. Therefore, the simulation system in Figure 3-17 is changed slightly as shown in Figure 5-7. The length of the transmission line is increased to 100 metres, and five tapped loads are placed at different positions as marked in Figure 5-7. The system voltage is 440v (RMS phase to phase), and the line parameters are unchanged. The load at the receiving end is 100 kW.

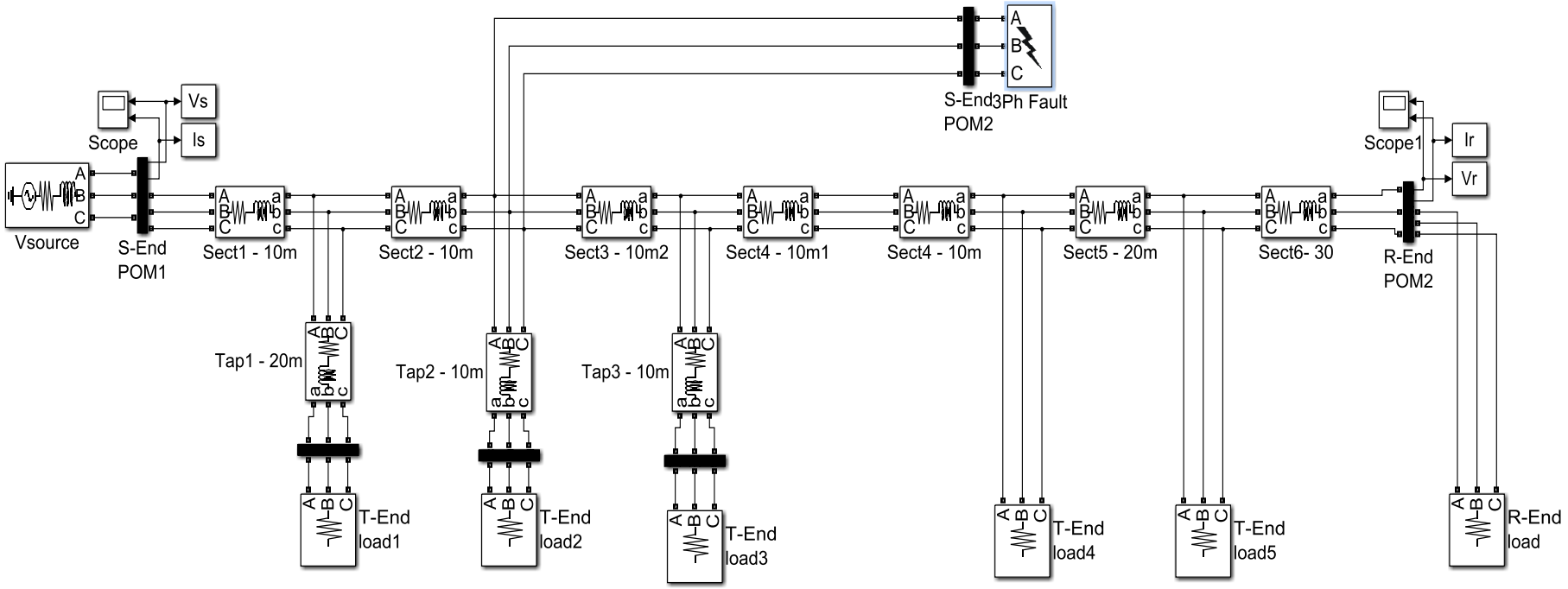


Figure 5-7 Power system with several tapped load

Two scenarios are investigated to quantify how the single-ended method is influenced by the tapped loads when they are not considered in the calculation process. First, the five tapped loads are equally set to 20 kW, and the percentage error is registered for various short circuit faults placed from the source end to the load end (POM2). Then, the scenarios are repeated but with the tapped loads now changed to 100 kW each. All the cases are performed with a short circuit and with inception angle of 90˚. The receiving end load is kept at 100 kW. The summary of the percentage error is given in Table 5-1.

Table 5-1 Percentage Error calculation with tapped load influence

Actual Fault Distance (m)	Number of tapped loads between fault and POM1	When each Tapped load = 20 kW		When each Tapped load = 100 kW	
		Estimated distance (m)	**Error (%)**	**Estimated distance (m)**	**Error (%)**
0	0	0.16	0.16	0.388	0.388
10	0	11.01		10.48	0.48
20	1	21.2	1.2	20.96	0.96
30	2	32.36	2.36		
40	3	42.7	2.7	43.54	3.54
50	3	55.12	5.12		
70	4	78.5	8.5	80	10.00
100	5	108.95	8.95	119.1	19.1

An interesting finding in Table 5-1 is that the accuracy of the single-ended fault location method decreases slightly when the non-considered tapped loads between the measuring end and the fault location are equal to the receiving end load. Another noticeable finding is that the error increases proportionally as the number of tapped loads between the fault and measuring end increases. This is because of value of the neglected current increases, and hence, the error increases. For example, when the fault is applied 20m from POM1, there will be one tapped load between the fault and POM1 while there will be three tapped loads when the fault is applied further from POM1 such as at 40m or 50m. The final column on the right shows

that when a 500kW tapped load (each tapped load is 100 kW which is equal the receiving end load) is neglected, the maximum error for a fault at the receiving end is increased to 11% compared to when the total of tapped loads was 100 kW. As a conclusion, the single-ended method showed an acceptable accuracy when the neglected tapped load is lower than the receiving end load, but the error increases proportionally as the tapped loads increases.

5.2 SEFLT with tapped load compensation

In this section, a new solution to the error caused by the tapped load is introduced. Therefore, a single line system with two tapped loads between the POM and the fault will be used to derive the mathematical model for compensating the tapped loads, and is shown in Figure 5-8(a). The system at non-fundamental frequencies is shown in Figure 5-8(b). The receiving end load is neglected considering all the fault current at non-fundamental frequencies flows toward the source end because $Z_S << Z_L$.

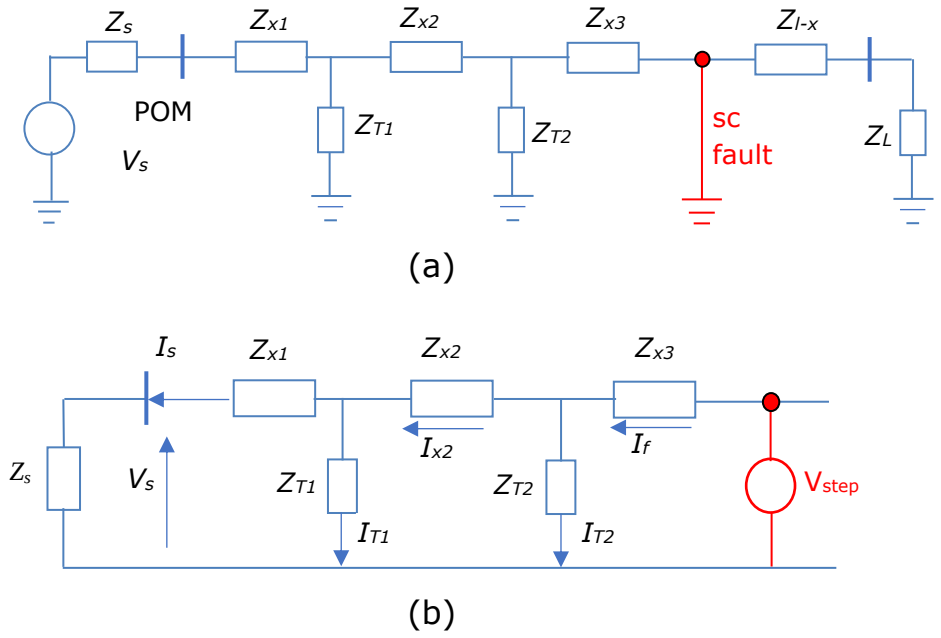


Figure 5-8 Power system with 2 taps before the fault (a) at fundamental frequency (b) at non-fundamental frequencies

$$V_s + I_s.Z_{x1} + I_{x2} * Z_{x2} + I_f * Z_{x3} = V_{pre\_f} \quad (5.1)$$

$I_f = I_{x2} + I_{T2}$ and $I_{x2} = I_s + I_{T1}$, substituted into (5.1) and rearranged gives:

$$I_s * Z_{x1} + (I_s + I_{T1}) * Z_{x2} + (I_s + I_{T1} + I_{T2}) * Z_{x3} = V_{pre_f} - V_s \quad (5.2)$$

Dividing both terminals by I_s gives

$$Z_{x1} + \left(1 + \frac{I_{T1}}{I_S}\right) * Z_{x2} + \left(1 + \frac{I_{T1}+I_{T2}}{I_S}\right) * Z_{x3} = \frac{V_{pre_f} - V_s}{I_s} \quad (5.3)$$

Based on the current divider rule, the ratio of the tapped load current to the source end could be approximated as follows:

$$\frac{I_{T1}}{I_S} = \frac{Z_S}{Z_{T1}}, \text{ and } \frac{I_{T1}+I_{T2}}{I_S} = \frac{Z_S}{Z_{T1}+Z_{T2}} \quad (5.4)$$

Generally, for more than two tapped loads:

$$X_{x1} + \left(1 + \frac{I_{T1}}{I_S}\right) * X_{x2} + \left(1 + \frac{I_{T1}+I_{T2}}{I_S}\right) * X_{x3} + \cdots + \left(1 + \frac{\sum_{n=1}^{N} I_{Tn}}{I_S}\right) * X_{xn} = imag\left(\frac{V_{pre_f} - V_s}{I_s}\right) \quad (5.5)$$

$$\frac{\sum_{n=1}^{N} I_{Tn}}{I_S} = \frac{Z_S}{\sum_{n=1}^{N} Z_{Tn}} \quad (5.6)$$

The fault is located by applying (5.5 and 5.6) as well as (3.8) to calculate a new V_{pre-f} using one of two methods, namely "exact" and "approximated" which will be described in the next sections.

5.2.1 Exact tapped load compensation for SEFLT

The first adopted method is the "Exact Compensation", which assumes the tapped load power is known and Z_{Tn} can be calculated. If the tapped load is unknown, it can be estimated using the pre-fault measurements at the

source end. The tapped load is subtracted from the total estimated load (assuming the receiving end load is known) and then the total tapped load is distributed equally over the number of taps for simplicity.

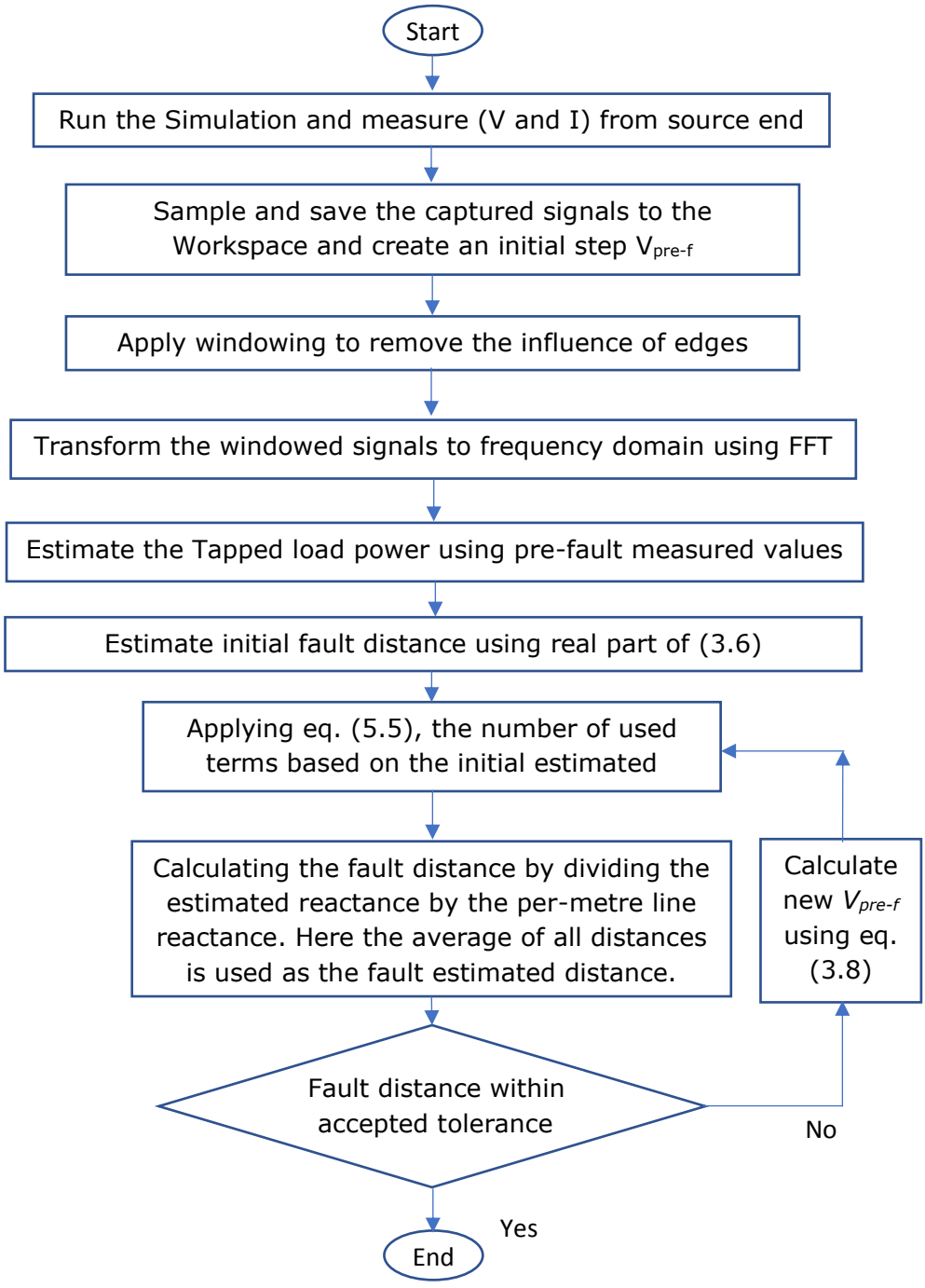
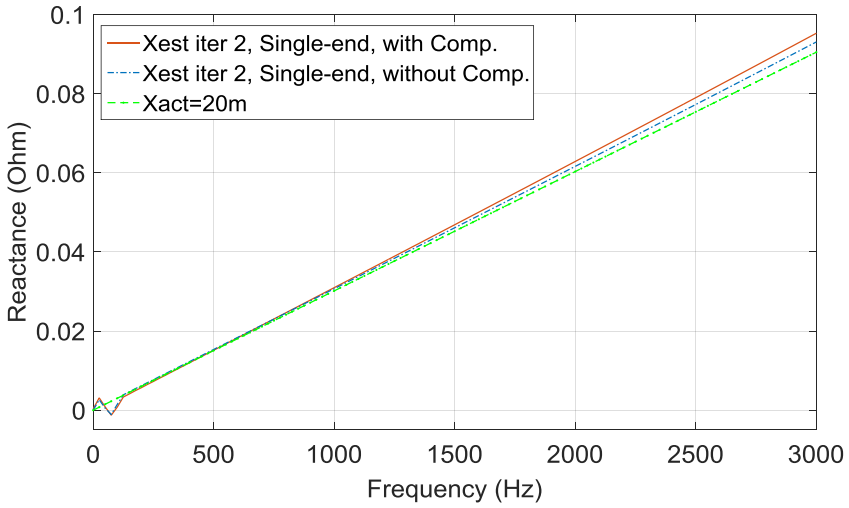


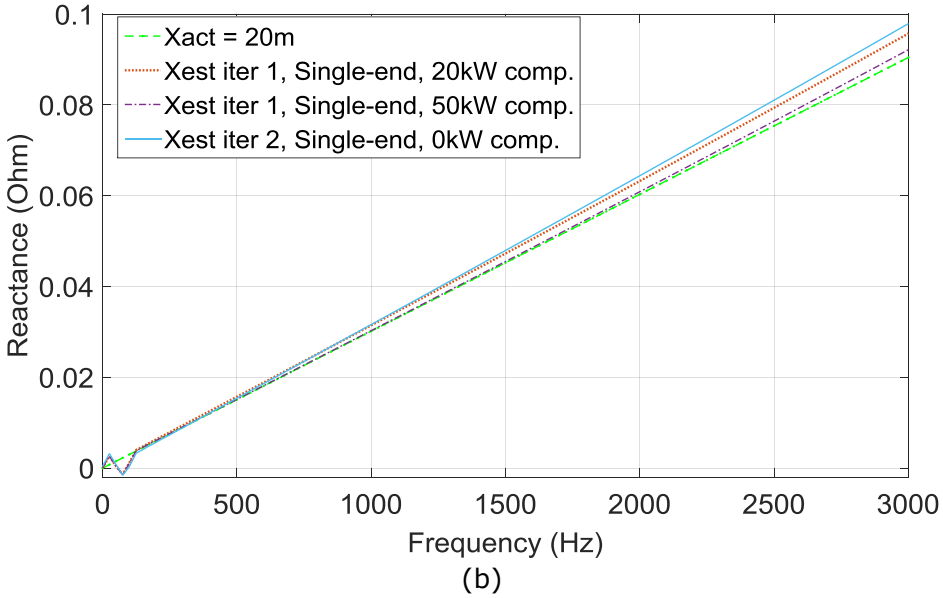
Figure 5-9 Flowchart of the SEFLT with tapped load compensation

An initial distance to the fault is estimated using (3.7) in order to find the number of tapped loads between the POM1 and the fault. Then, the correct number of terms for (5.5) can be used. An iterative method utilising (5.5) and (3.8) is then performed with a similar set of processes as in the non-compensated model. The flowchart in Figure 5-9 summarizes the algorithm.

The simulated IPS system shown in Figure 5-7 is considered here. Several fault tests are applied to demonstrate the suggested approach. Figure 5-10 shows the estimated reactance with and without compensation for a fault 20m from source end. The fault resistance used is 0.01Ω. There is only one tapped load between the POM1 and the fault. The tapped load is changed from 20 kW in Figure 5-10(a) to 50 kW in Figure 5-10(b). The magnitude of the compensation required increases with the tapped load current. There is still some error present after the compensated method has been applied, which is due to neglecting the current flowing downstream of the fault (toward the receiving end load). Figure 5-10(b) clearly demonstrate that when the tapped load power increases, the compensation obtained is larger.



(a)



(b)

Figure 5-10 SLG fault with one tapped load compensation (a) tapped load1 is 20kW (b) tapped load1 is 50kW

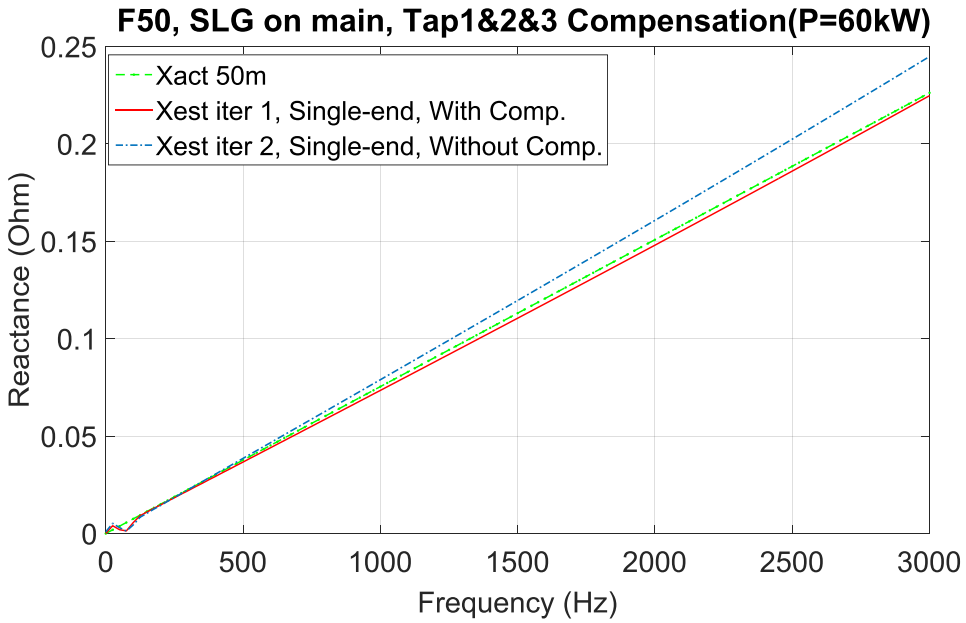


Figure 5-11 SLG fault 50m from POM1 with three tapped load compensation

A further example is presented in Figure 5-11, where the fault is 50m from POM1, and three tapped loads are between the fault and the measuring end. The total load of these tapped loads is 60 kW. In this case, the magnitude of the neglected tapped load is 30% of the total load demand on the system. The non-compensated SEFLT shows an error presented by the blue dash-

dotted line. On the other hand, the compensated estimate shows a significant enhancement in the estimation accuracy as presented by the red solid line. The green dashed line is the actual impedance to the fault location. The only disadvantage of this methodology is the increased complexity of calculation required when the number of the tapped loads is larger than five.

5.2.2 Approximate tapped load compensation for SEFLT

A simpler compensation model is introduced and analysed in this section to overcome the complexity presented when there are a large number of tapped loads between the fault and the measuring end. In this approach, a single equivalent tapped load is assumed. A similar process is used to estimate the total tapped load power. The initial fault distance is estimated using (3.7). Then, the tapped load is estimated based on the pre-fault measurements. Based on the initial fault distance and the assumption of tapped load location knowledge, the number of the tapped loads between the initial fault distance and POM1 is assumed as a one equivalent tapped load placed in the middle of the initial distance between POM1 and the fault as shown in Figure 5-12. In this case, equation (5.5) only includes the first term ($\frac{I_{T-Eq}}{I_S}$) which leads to a simpler calculation. The new distance estimated using (5.5 and 5.6) is used to update the location of the equivalent tapped load. This iteration is repeated until the tolerance between two successive iterations is within pre-set value (such as 0.5m)

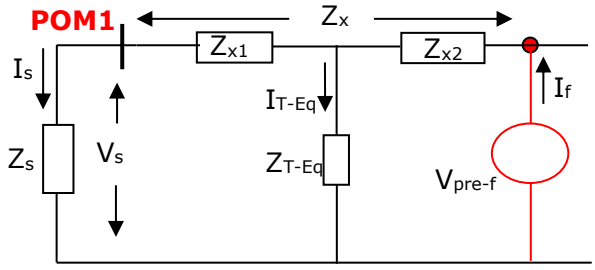


Figure 5-12 Non-fundamental circuit with one equivalent tapped load

A SLG fault 30m from POM1 is applied to the system shown in Figure 5-7, and the estimated reactance for the different compensation scenarios is presented in Figure 5-13. The first scenario is to compensate the two tapped loads between the fault and POM1 as a single equivalent tapped load. The estimated reactance is plotted as a dotted dark green line (Xest iter2, Eq. 2Tap comp. 2% error) with an error of 2.0% calculated using (3.4), and compared to the non-compensated reactance plotted in blue solid line (Xest iter2, No comp. 2.36% error). The next scenario which is plotted as a red dash-dotted (Xest iter2, Eq. 5Tap comp. -1.1% error) line is when all the tapped loads are presented as a single equivalent tapped load. The estimation shows some improvement with an error of -1.1%. Finally, the total system load (tapped loads and receiving end load) is compensated, which is plotted by the solid orange line which matches the actual reactance in green dashed line. This last scenario presented the best estimation accuracy with around 0.1% error as all the load current is approximately compensated.

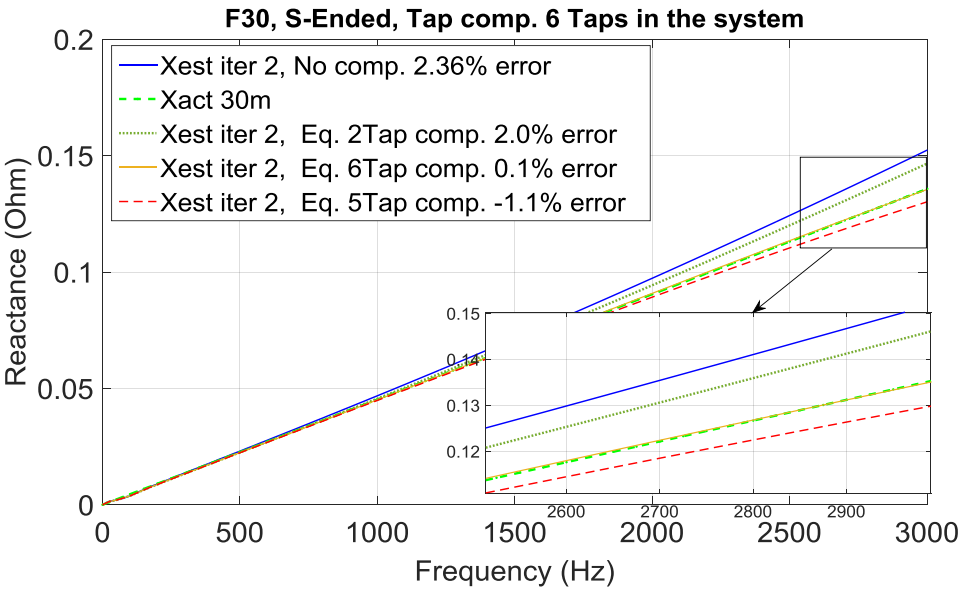
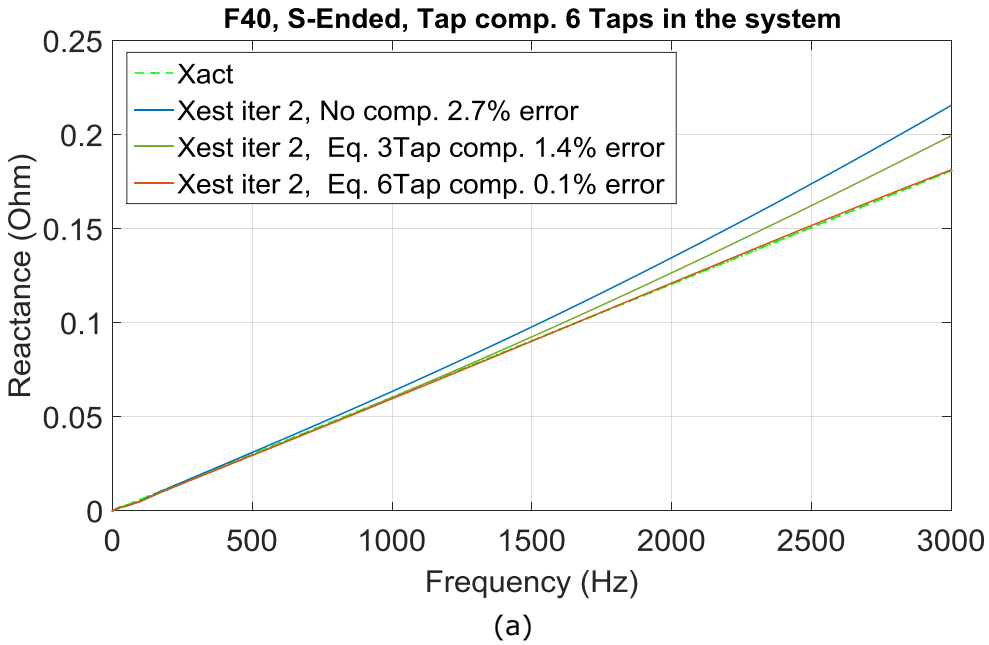
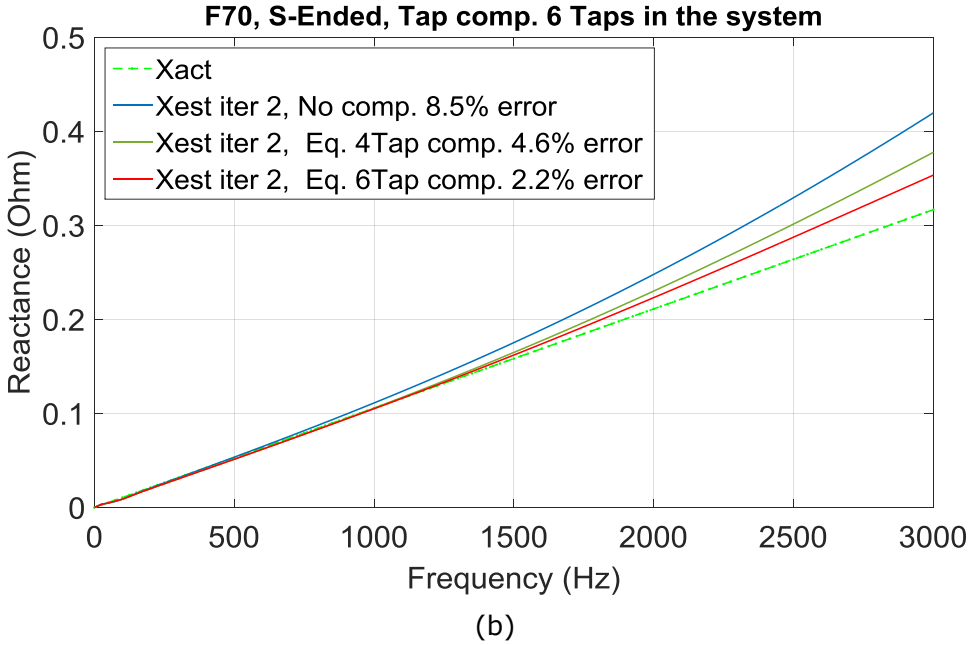


Figure 5-13 Estimated reactance with equivalent tapped load compensation for SLG fault 30m from POM1



(a)



(b)

Figure 5-14 Impedance estimated with tapped load compensation (a) SLG 40m from POM1 (a) SLG 70m from POM1.

Two more faults are considered for further verification. The faults are applied at 40m and 70m from POM1 with two tapped loads, and four tapped loads respectively between the fault location and the POM1. Figure 5-14 summarizes the estimated reactance for three assumptions: no compensation (blue line), only two or four tapped loads between the fault and POM1 (dark green line) are compensated, and finally the total system

load (all tapped loads plus the receiving end load) is compensated (red line). Again, the total load compensation shows the best estimation with a maximum error of 2.2% compared to a non-compensated error of 8.5% for the fault applied at 70m from POM1. In conclusion, this assumption of "approximate" tapped-load compensation offers a simple and reliable method to improve the accuracy of the SEFLT when the system includes multiple unknown tapped-loads in the system.

5.3 SEFLT with tapped load compensation when R_f is Large

In this section, the SEFLT with tapped load and receiving load compensation will be introduced. The circuit used in section 5.2.2 is considered but with one tapped load placed between the measuring end (POM1) and the fault location, as shown in Figure 5-15.

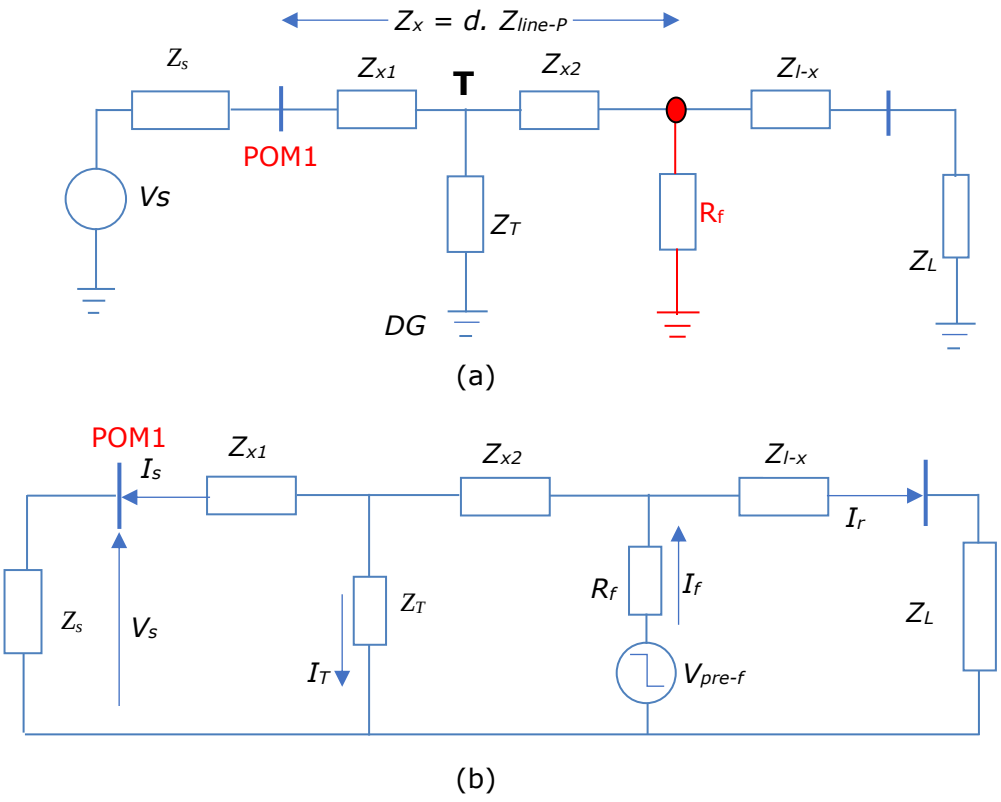


Figure 5-15 Single tapped system with High fault resistance (a) at the fundamental frequency (b) the system at a non-fundamental frequency

The same derivation methodology applied in section 3.2.2 is used in this section. The impedance between the POM1 and the fault location can be estimated as follows:

$$Z_{x1} + Z_{x2}\left(1 + \frac{I_T}{I_s}\right) = \frac{V_{pre-f} - V_s}{I_s} - R_f - \left(\frac{I_T + I_r}{I_s}\right)R_f \qquad (5.7)$$

Where $\frac{I_T}{I_s} = \frac{Z_s + Z_{x1}}{Z_T}$, $\frac{I_r}{I_s} = \frac{(Z_T)(Z_{eq} + Z_{x2})}{Z_T + Z_L + Z_s + Z_{x1} + Z_{l-x}}$ and $Z_{eq} = \frac{(Z_s + Z_{x1})Z_T}{Z_T + Z_s + Z_{x1}}$ (5.8)

Thus, the load compensated iteration will be used instead of the pre-fault voltage at the fault location iteration when the fault resistance is high and comparable to the receiving end load. The same system as described in section 3.2.1 is used in addition to one tapped load with 50kW power placed 10m from POM1. A SLG fault with 0.1Ω resistance is applied 20m from POM1 in order to test the methodology. The estimated reactance with compensation (blue line) is compared to the non-compensated outcome (red line) and is shown in Figure 5-16. The single-ended technique with tapped load and receiving end load compensation results in a significant improvement in the accuracy due to compensation for the neglected tapped and received load current applied in the voltage iteration method of section 3.2.1.

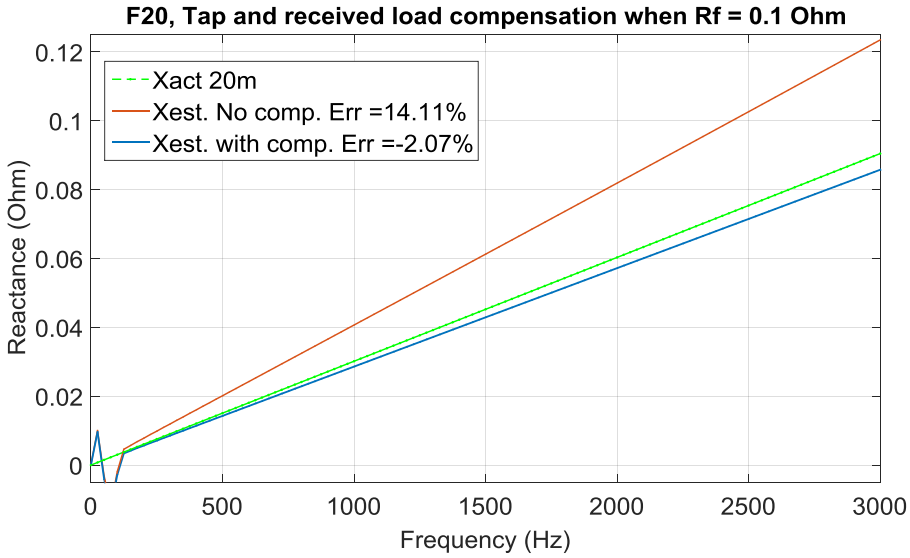


Figure 5-16 Estimated reactance with tapped and received load compensation

As a further demonstration, the fault resistance is increased to 0.5Ω which is large and comparable to the load resistance of 1.936Ω (100 kW) and tapped load of 3.87Ω (50 kW) in the studied system. Three SLG faults at 20m, 40m, and 50m are used. The estimated reactance for all the fault cases is plotted in Figure 5-17. The compensated method shows again a significant error reduction as it compensates by the neglected loads current in the pre-fault voltage iteration. The dashed lines present the actual reactance (Xact.) to the faults while the solid lines present the estimated reactance (Xest.). The red, grey, and orange lines indicate the single-ended with the non-compensated outcome while dark green and blue, light blue are the estimated reactance using the single-ended method with compensation. Note that the percentage error for the fault at 50m is reduced from 18% to 4.21%, for the fault at 40 the error decreased from 15.75% to 3.5%, and the error reduced from 12.1% to -3.05% for the fault at 20m from POM1.

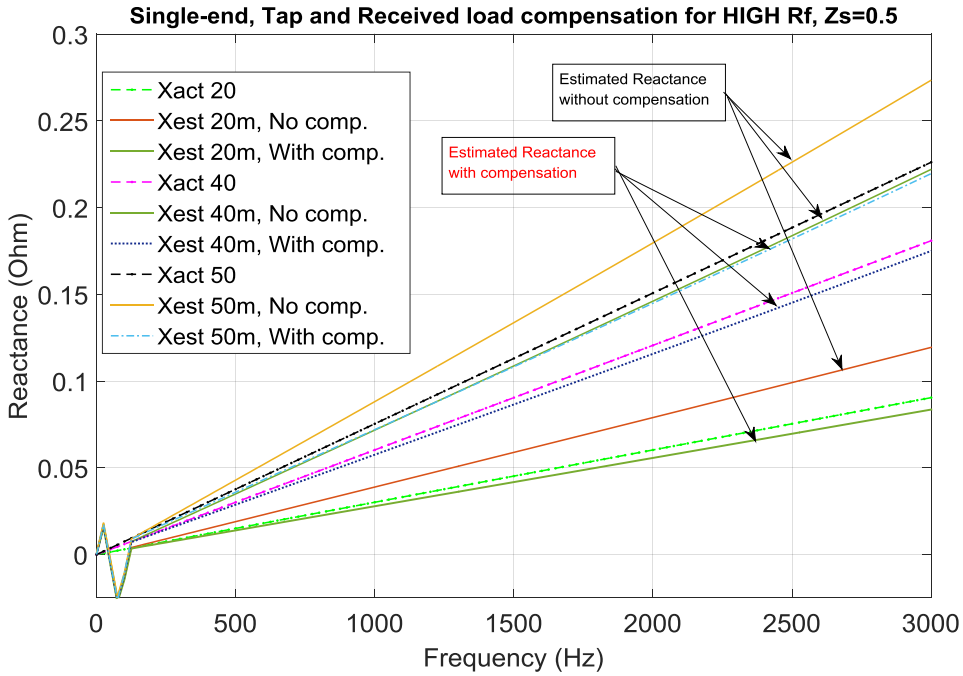


Figure 5-17 Estimated reactance with tapped load and receiving end load compensation when Rf = 0.5Ω

In conclusion, the estimated reactance demonstrates that the compensated methodology reduced the error to an acceptable level despite the high fault resistance as shown in Figure 5-17. The error calculation for the three cases shows that the maximum error is reduced from 18% to -4.21% based on (3.4).

5.4 Influence of DG on the SEFLT

As with the study of the DEFLT, the influence of the inverter-based DG on the SEFLT looking at the higher frequency contents of fault transient will be studied in this section. Factors such as: DG supplied power, DG location, and the number of DG units will be considered.

5.4.1 SEFLT with DG theory

The diagram of Figure 5-18 is considered, which represents an upgrade of the system used to derive the mathematical model of section 3.2. The system includes one DG between the fault location and the measuring end (POM1). The DG is connected to the system through a coupling impedance (Z_c) at the point **d**. The system at non-fundamental frequencies including the DG is shown in Figure 5-19, where the DG is represented as a current source at higher frequencies.

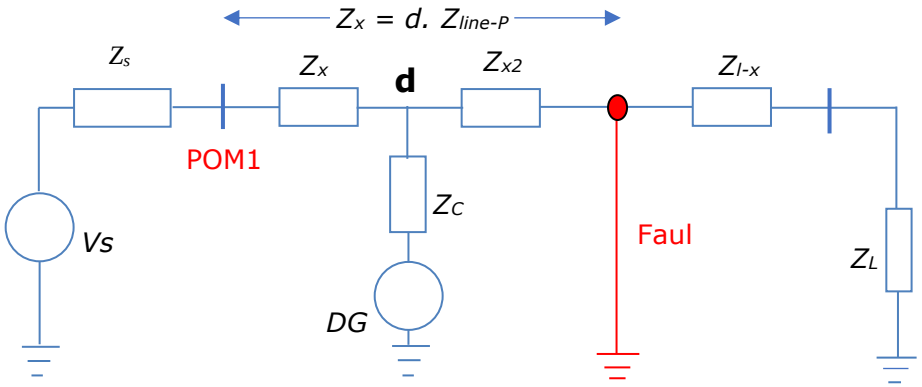


Figure 5-18 Single-line diagram for power system with DG

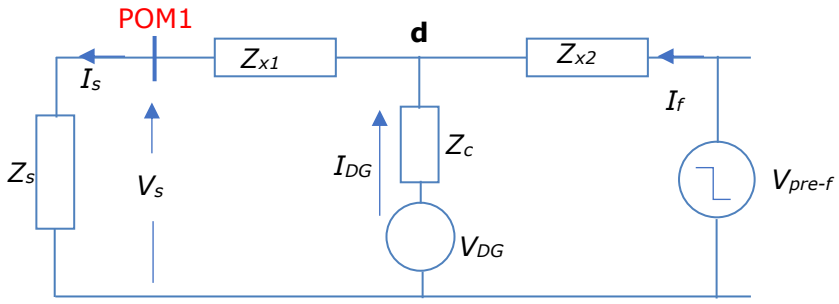


Figure 5-19 System with DG at non-fundamental frequencies

Mathematically, the derivation of the impedance estimation is similar to what was used in section 3.2 but with some minor changes. Applying circuit theory to Figure 5-19 gives:

$$V_s + I_s * Z_{x1} + I_f *. Z_{x2} = V_{pre\_f} \quad (5.9)$$

$As\ I_f = I_s - I_{DG}$, substituting into (5.9) and rearranging yields:

$$Z_{x1} + \left(1 - \frac{I_{DG}}{I_s}\right) * Z_{x2} = \frac{V_{pre\_f} - V_s}{I_s} \tag{5.10}$$

$$Z_x = Z_{x1} + Z_{x2} = \frac{V_{pre_f} - V_s}{I_s} + \left(\frac{I_{DG}}{I_s}\right) * Z_{x2} \tag{5.11}$$

Whereas $\frac{I_{DG}}{I_s}$ can be approximated using the current divider rule as follows:

$$\frac{I_{DG}}{I_s} = \frac{Z_s + Z_{x1}}{Z_{DG}} \tag{5.12}$$

It can be seen that the difference between (5.11) and (3.6) is only the ratio of the DG current to the measured current at POM1 multiplied by the impedance between the fault and the DG coupling point d. The fault distance is calculated in the same way by dividing (5.10) by the line per-metre impedance in each frequency over a 3 kHz range. A similar iterative process will be performed using (3.8 and 5.11) until the estimated distance converges to the pre-set tolerance of 0.5m.

5.4.2 Simulation and results

An inverted based DG has been added to the MATLAB/Simulink system of Figure 3-17, which leads to Figure 5-20 [84]. The system parameters are 100kw load, 50m of transmission line with 0.24H/m and 30μΩ inductance and resistance respectively. The source impedance is (0.0011+0.0096j Ω) with line-line supply voltage of 440V as presented in Table 3-2 in section 3.2.1. The sampling frequency is 100kHz. The DG model is a simulated three-phase inverter as described in chapter 4.6.1.

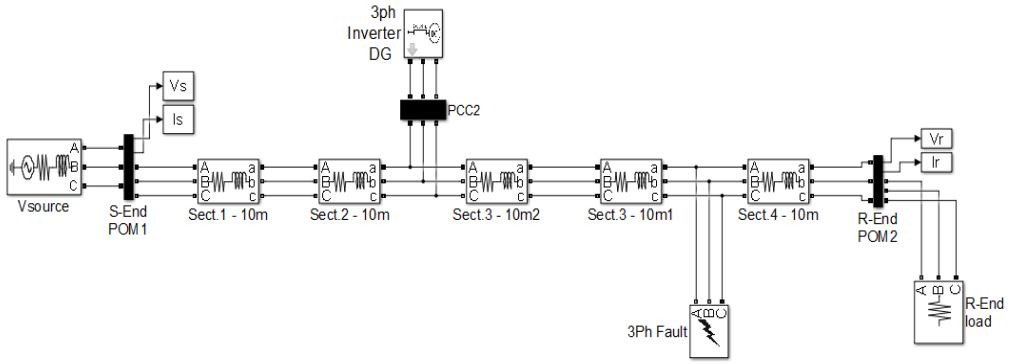


Figure 5-20 Simulated three phase system with DG

A short circuit SLG fault at 40m from POM1 as presented in Figure 5-20 and a DG with a power rating of 50 kW is used to demonstrate the compensation algorithm. Three cases are considered for analysis and comparison as follows: SEFLT without DG in the system, a SEFLT with DG in the system but is not considered in the calculation using (3.7), and finally, a SEFLT with DG current is considered in the calculation using (5.11). Figure 5-21 shows the estimated reactance for the three cases when a 50 kW DG is added to the system. The zoomed view shows that the effect of the DG is potentially small. Interestingly, (3.7) and (5.11) result in a very close estimation as given in the solid dark green line and dashed orange line, respectively. The closer inspection identifies that the DG has a small influence in total. A short circuit between phases A and B has also been considered as shown in Figure 5-22. Again, the DG supplying 50% of the load only causes about 1% error to the original single-ended estimation process described in section 3.2. On the other hand, using (5.10) showed negligible outcome due to the ratio of DG current to POM1 current is very small at higher frequencies.

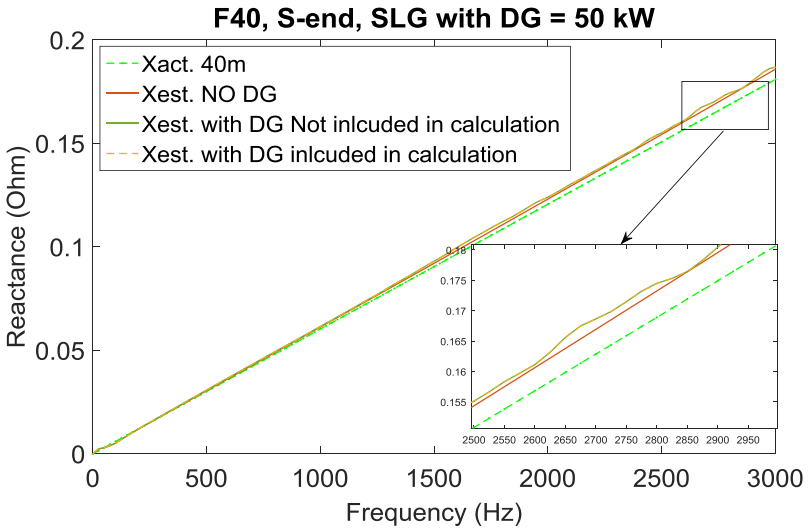


Figure 5-21 Influence of DG on SEFLT, SLG fault

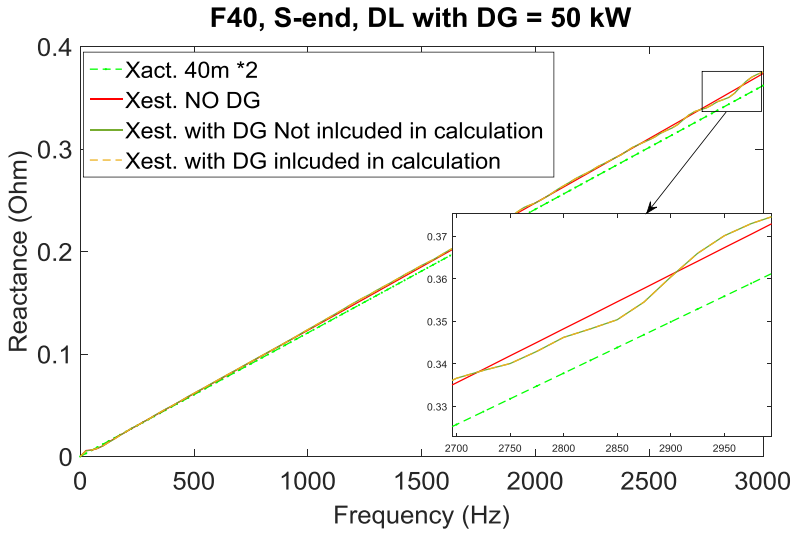
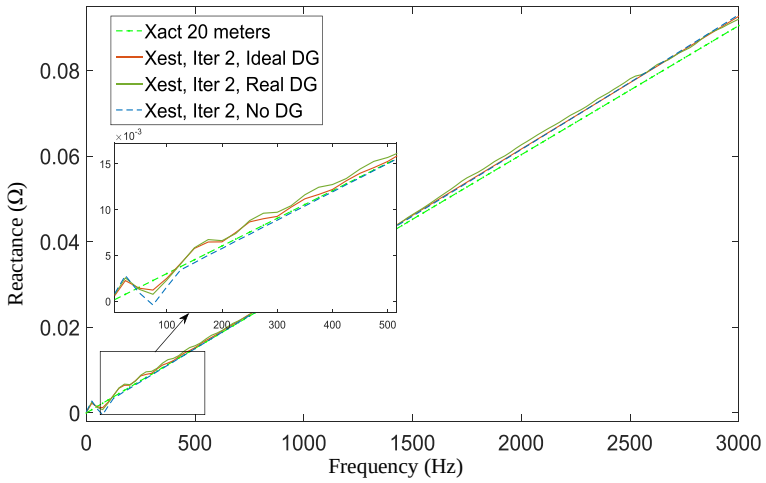
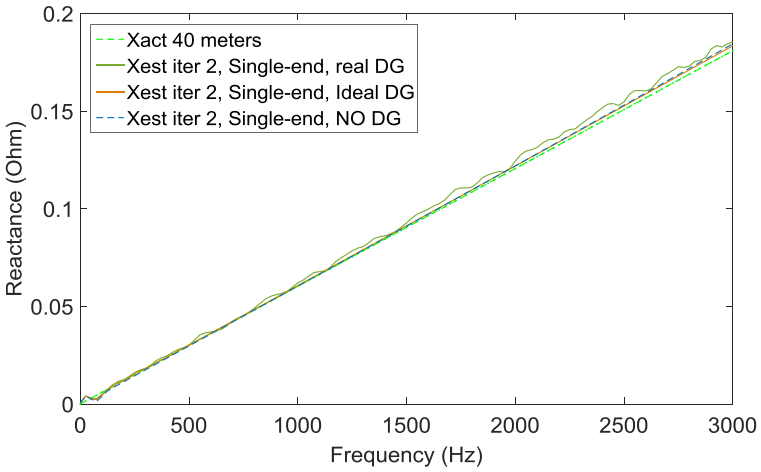


Figure 5-22 Influence of DG on SEFLT, DL fault

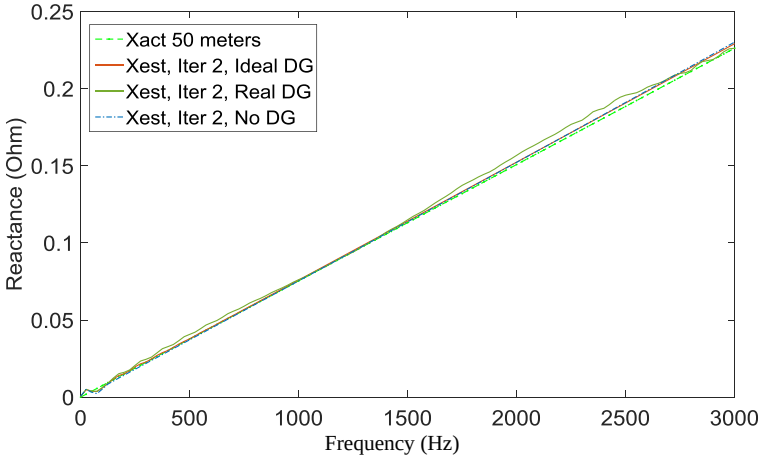
Moreover, the effect of a realistic inverter-based DG (DG that contains electronic switching components and dc supply) is compared to the effect of ideal DG (Controlled ideal voltage source in red solid line, see Appendix A - Ideal DG) as shown in Figure 5-23. Table 5-2 summarizes the estimated distance for all the tested fault positions and the calculated error for a DG place, 10m from POM1. This Table also shows the comparison of the case with DG to the case without DG.



(a)



(b)



(c)

Figure 5-23 estimated Reactance using the SEFLT with the effect of the DG; (a) fault at 20m (b) fault at 40m and (c) fault at the received end

The estimated reactance is divided by the line's per-metre reactance at each higher frequency to find the distance to the fault. Consequently, the distance is calculated using the average distance through the total 3 kHz frequency range considered in this study. Then the percentage error is calculated using (3.4).

Table 5-2 Estimated distance and the percentage error

Actual Fault Distance	**Average estimated distance**			**Percentage Error**		
	No DG	**Ideal DG**	**Real DG**	**No DG**	**Ideal DG**	**Real DG**
00	0.128	0.53	0.47	0.25	1.08	0.95
10	10.175	10.55	10.52	0.35	1.1	1.04
20	20.18	20.78	20.92	0.35	1.6	1.85
40	40.36	41.00	41.7	0.7	2.1	3.44
50	50.45	50.9	52.4	1.4	2.2	4.2

The results presented in Table 5-2 show that the proposed SEFLT at higher frequencies can work with high accuracy even when the DG has been added to the system and not compensated for in the protection design process. It is noticeable that the maximum increase in percentage error is only 2.8% when the DG supplies 50 kW to the system and is connected 10m from POM1. This minimum influence is explained by the fact that the DG current has a small magnitude at higher frequencies and only has a small influence even if it has being neglected using (3.7). A comparison of the frequency content of the realistic DG at 10m to the ideal one is shown in Figure 5-24. It is clear that the neglected non-fundamental frequencies injected by the DG are the source of the small increased error.

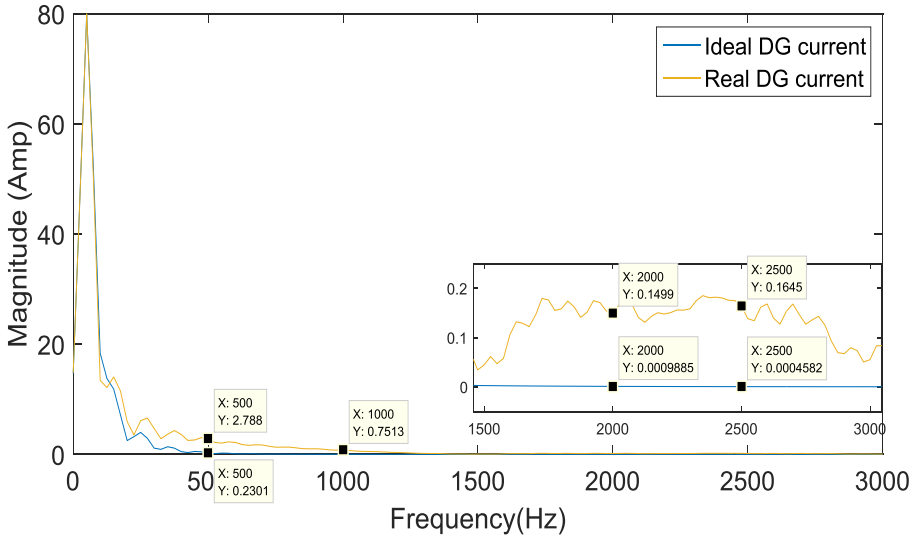


Figure 5-24 Frequency content of the DG current during fault transient

The effect of the DG location has also been investigated by changing the location of the DG first upstream the fault (between the POM1 and the fault) and then downstream of the same fault (between POM2 and the fault). Therefore, a fault is initiated 20m away from POM1, with the DG placed at 10m from POM1 and then moved to 40m from POM1. Figure 5-25 shows the estimated reactance when the DG location is changed. The difference between the two cases is very small with an error of lower than 0.5%, which can be considered negligible. The reason is that the DG has very small non-fundamental current components at higher frequencies that have been shown in Figure 5-24, which cause only a small influence on the estimated reactance at these frequencies.

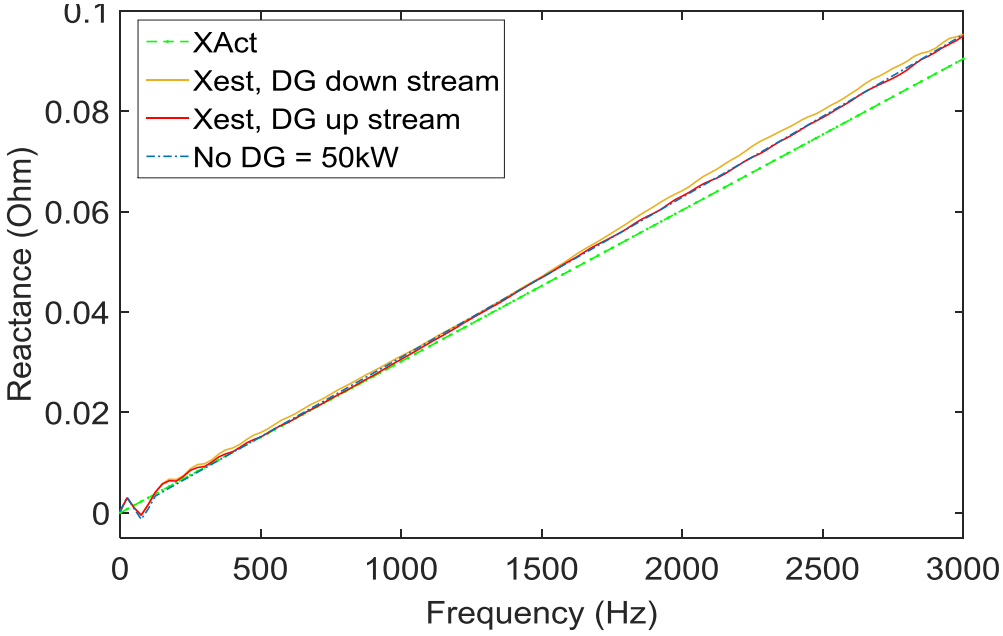


Figure 5-25 Influence of DG location on the single-ended method

This study showed that the inverter-based DG has a small influence on the SEFLT that uses wideband frequency range compared to the studies presented in chapter 2.3 showed that the DG has a significant negative impact on the studied techniques that use fundamental frequency to locate the fault unless the effect has been properly included in the estimation algorithms. The studies also showed that error level is proportional to the level of the injected current by the DG. The error increases as the DG level increases if not being compensated properly. This is because the magnitude of the DG current at fundamental frequency is large enough to create a significant effect on the estimated fault distance.

5.5 Combined fault location estimate

Multi-tapped lines are common in IPS/Microgrids, which supply variable loads between the main source and the main load. Adopting a cost-effective and efficient method for fault location is important for fast power recovery and improving system reliability [82]. Moreover, locating faults on the multi-tapped line systems presents an issue for the single-ended method. Therefore, in this section, a new methodology that utilizes a combination of the single-ended method studied in this chapter for the fault locating as well as the double-ended technique studied in chapter 3 for fault discrimination. This technique will lead to the minimization of the number of required measurements compared to traditional fault location methods.

The flowchart [82] shown in Figure 5-26 describes the methodology of locating a fault in a multi-tapped line IPS. First, after capturing and processing the required voltage and current measurements from the main line terminal, the SEFLT is applied using (3.7 and 3.8) as shown by the iterative loop. However, when the iteration converges, and the distance is calculated, there will be a multi-possible fault location to the fault path. Secondly, the DEFLT is used to discriminate between the possible locations. As described in section 4.3, the DEFLT can locate a faulted tapped line. Consequently, if the DEFLT estimated distance is equal or very close to the SEFLT estimated distance, then the fault is on the main line while if the difference between the two methods is large, then the fault is on the tapped-line located by the DEFLT. The fault distance from POM1 is based on the single-ended result.

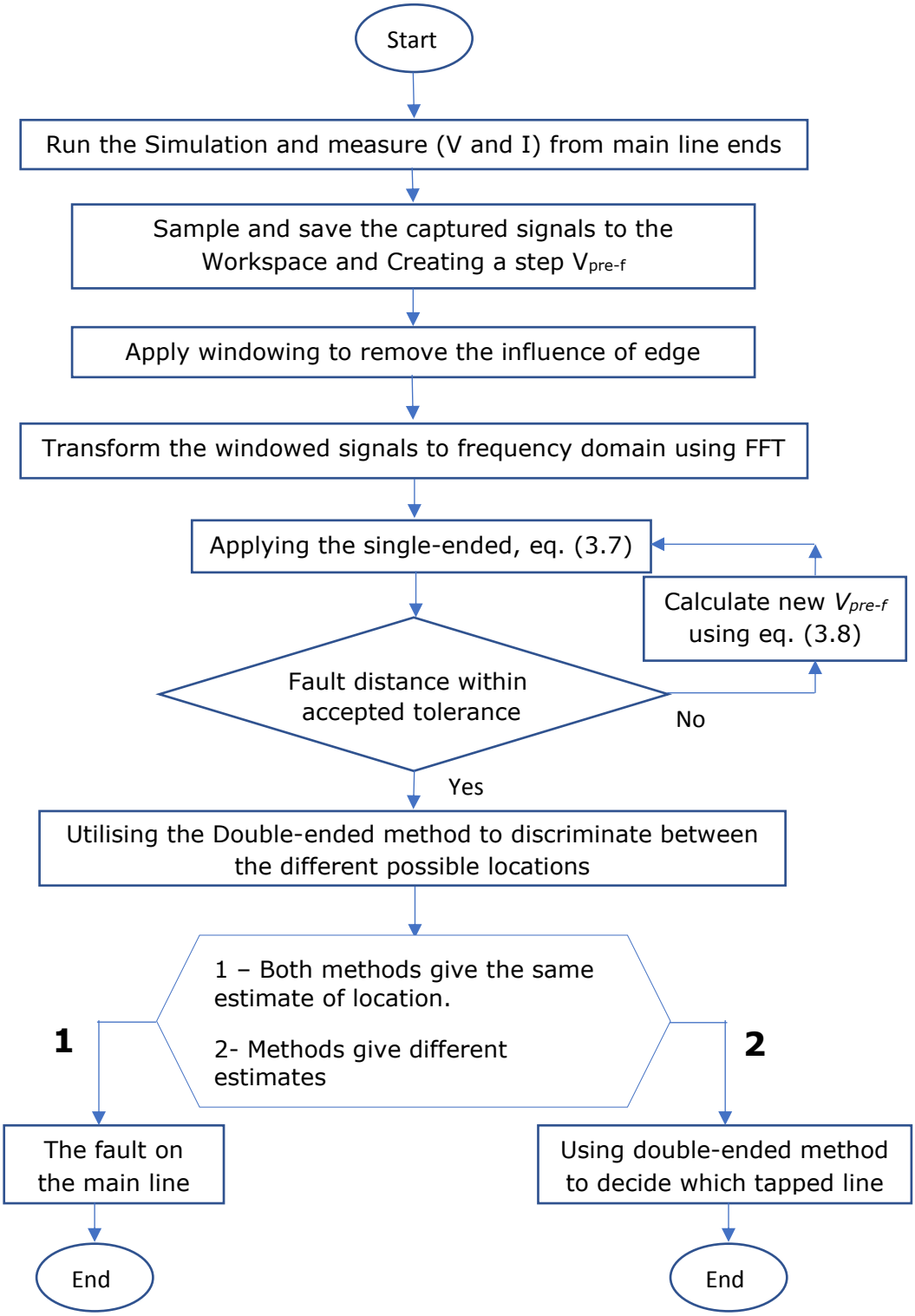


Figure 5-26 Combined fault location flowchart

5.5.1 Verification through simulation

A simulation was used to verify the described combined fault location methodology for a multi-tapped line IPS. Therefore, the simulation of section 3.2.1 is used with the three tapped-lines as shown in Figure 5-27. The parameters of the system are kept unchanged. The tapped-line loads are between 20-30 kW and the receiving end load is 100kW. The voltage and current are measured from buses POM1 and POM2. The length of Tapped-line1 is 20m, Tapped-line2 and tapped-line3 are 10m. Different fault types and locations are applied to the system to validate the proposed method for locating faults on tapped lines as well as the main line using only two sets of measurements.

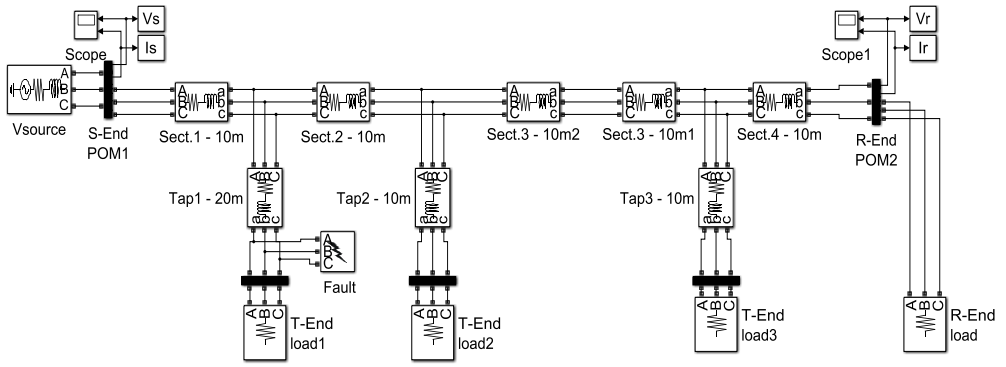
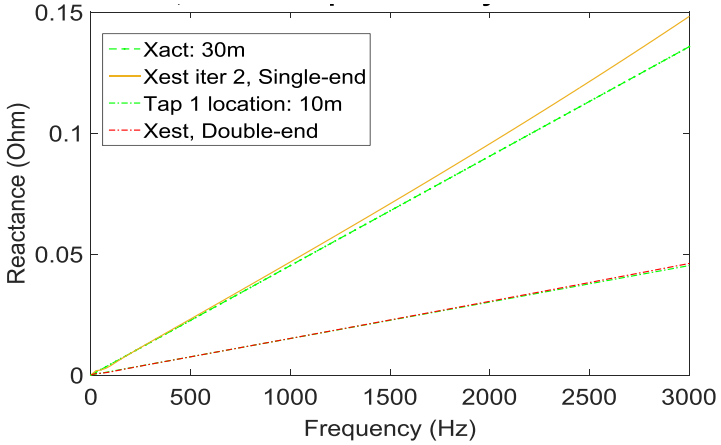


Figure 5-27 IPS with three tapped lines

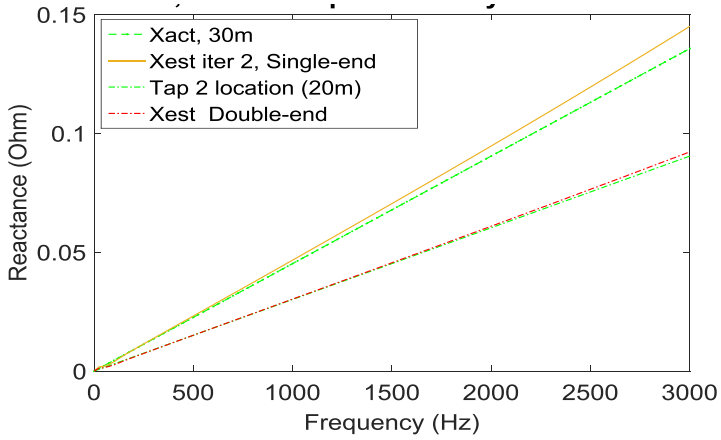
A SLG fault was initiated 30m away from POM1 firstly on tapped-line 1, secondly on tapped-line 2 and then on the main line to verify the suggested procedure. In Figure 5-28(a) the fault was on Tap 1, and the single-ended method estimated a fault 31.3m away. At this distance, there are three possible fault locations: on Tap 1, Tap 2 and the main line. Hence, the double-ended method was used to discriminate between the possible locations: the estimated fault location was 10m from the supply using the double-ended method, which corresponds with tapping location 1. As a result of combining both methods, the fault is found to be on tap line 1, which is

the correct choice. The same process in Figure 5-28(b and c) shows the estimated fault distance and how it has been discriminated from the other possible location using the double-ended method. The calculated distance is 31.3 m, while the actual distance is 30 m, which gives an error of 2.6%.

(a)



(b)



(c)

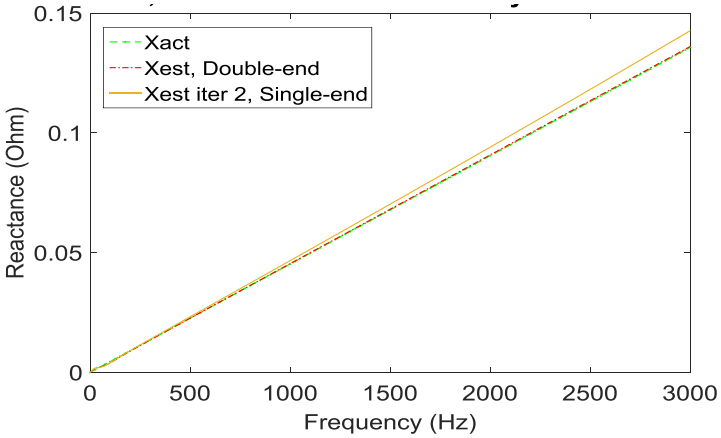
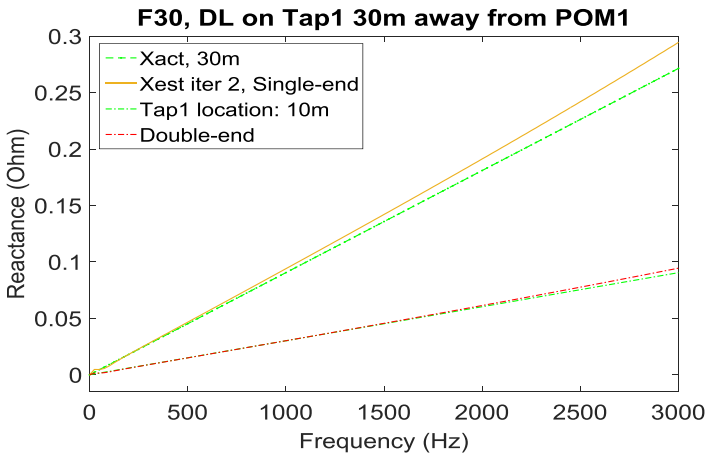


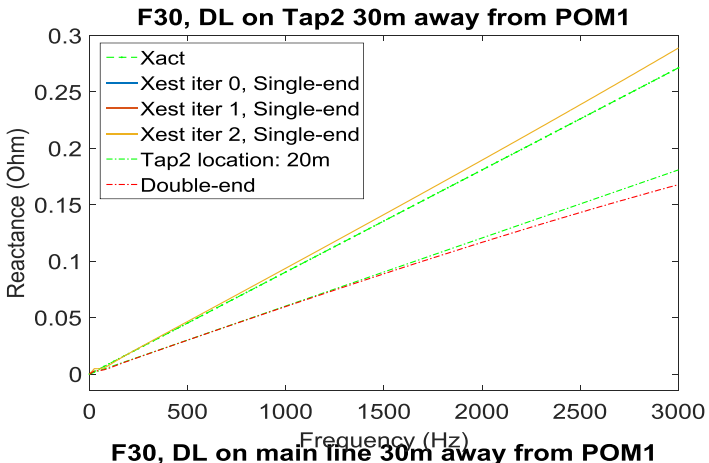
Figure 5-28 SLG fault 30m away on a different location (a) On Tapped line 1 (b) On Tapped line 2 and (c) On the mainline

The same steps are repeated with a DL fault and DLG fault, which further shows the capability of combining the two methods to locate different fault types on the tapped lines without any measurement from the taps. Figure 5-29 presents the estimation results obtained when the DL is applied to a different location, and Figure 5-30 provide the DLG results.

(a)



(b)



(c)

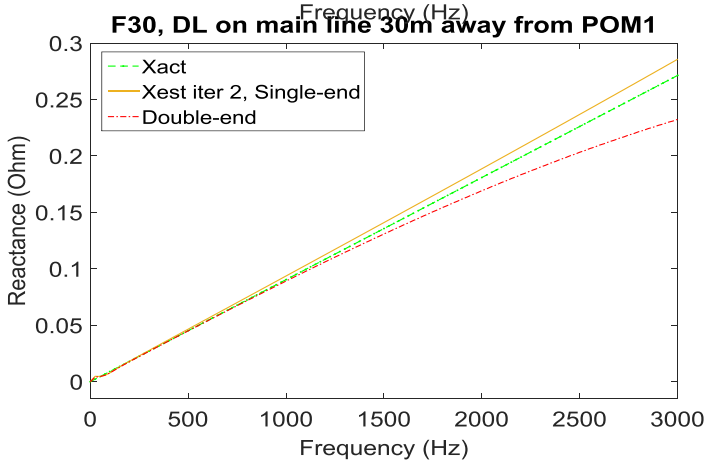


Figure 5-29 DL fault 30m away from POM1 (a) On Tapped line 1 (b) On Tapped line 2 and (c) On the mainline

The magnitude of the fault resistance used for all cases was 0.01Ω, which is very low when compared to the system load impedance. The actual reactance Xact is the green dashed line, and Xest is the estimated reactance while "iter" is the required number of iterations for the single-ended method. The final iteration of the single-ended method is presented in the figures, which shows only two iterations were required for the error to coverage to within a pre-set tolerance.

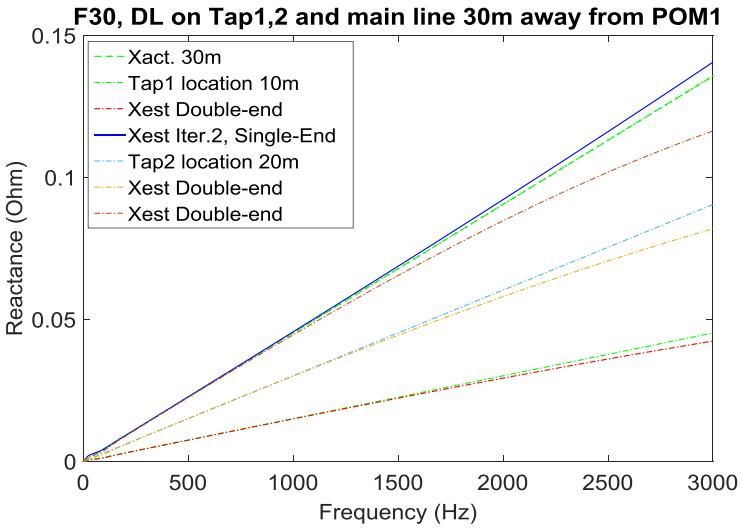


Figure 5-30 DLG fault on Tap1, Tap2 and Main Line

It is obvious from Figure 5-29 and Figure 6-30, there is a slightly high error resulted from the DEFLT at the high frequency range when the fault is on the main line. This is caused by the neglected tapped line between the fault location and the POM1. Also, the SEFLT offers a slightly larger accuracy at the high frequency due to the larger transient added by the created step voltage at the fault location. Further simulations were performed using different fault locations in order to investigate the accuracy and reliability of the method presented. The percentage error calculation using (3.4) are summarized in Table 5-3 and Table 5-4 for SLG and DL faults in all the possible fault locations throughout the system and compared to the

estimated distance using the DEFLT. The last column to the right shows the decision based on the estimated distance from the two methods.

Table 5-3 Percent error calculation for SLG faults

Actual Fault distance (m)	Estimated distance (m) using SEFLT	Error (%)	Estimated distance (m) using DEFLT	Decision on the fault location
10	10.175	0.35	10.2	On Main line
30	30.26	0.52	30.15	On Main line
50	50.45	1.4	50.25	On Main line
30	30.68	1.36	10.2	On Tap Line 1
30	30.44	0.9	30.15	On Tap Line 2
50	50.6	1.2	50.25	On Tap Line 3

Table 5-4 Percent error calculation for DL faults

Actual Fault distance (m)	Estimated distance (m) using SEFLT	Error (%)	Estimated distance (m) using DEFLT	Decision on the fault location
10	10.10	0.20	9.9	On Main line
30	30.124	0.25	9.85	On Main line
50	50.142	0.285	38.7	On Main line
30	30.50	1.00	9.9	On Tap Line 1
30	30.275	0.55	9.85	On Tap Line 2
50	50.225	0.45	38.7	On Tap Line 3

It is apparent from the results presented in Table 5-3 and Table 5-4 that the single-ended method shows a high accuracy to estimate the distance to the fault location with a maximum percentage error of less than 2%. The calculation based on the single-ended estimation and the estimated distance is the average of the distance over the 3 kHz frequency range of Figure 5-28 — Figure 5-30. Moreover, the percentage error increased as the fault moved toward the end of the line. This is because a larger tapped line current is neglected in the utilized scheme as well as the SNR decreases because of reduced amplitude of the fault transient step.

5.6 Summary

The SEFLT for an IPS/Microgrid introduced in chapter 3 has been thoroughly evaluated in this chapter. Firstly, the practical factors that could affect the reliability and efficiency of the technique were investigated. Secondly, a new solution was adopted to overcome the issues such as compensating for tapped loads in a tapped system or compensating for the tapped and receiving end loads in case of high fault resistance. Then, investigating the effect of inverter-based DG on the SEFLT. Finally, proposing a new combined technique to locate fault in multi-tapped system using only measurement from two ends.

The simulation study showed that the fundamental technique offers a high accuracy for a short circuit or a very low fault resistance (much lower than the receiving end resistance). The achieved accuracy is better than 1.5% for a noise free system. The addition of 2% noise in the measurement resulted in a maximum error increase of 2%. Moreover, the technique offers a high accuracy for most of the fault imposed angles except 5 degrees around the zero crossing point.

The effect of a tapped load was also studied. The SEFLT showed an acceptable accuracy of 9% when the tapped load was equal to the receiving end load. On the other hand, the error doubled when the tapped load is increased 5 times. Therefore, a compensation technique for a high tapped load condition was proposed and demonstrated. The technique reduced the 9% error to 2.2% when the full tapped load is compensated.

The influence of inverter-based DG on the fundamental SEFLT was studied. The SEFLT demonstrated a high reliability in spite of the added error because of the DG penetration. The error was increased by less than 3% to 4.2% when the DG supplied 50% of the system load. The SEFLT also interestingly was not affected by the DG location or Power level. The error changed by less than 1% when the DG location is changed, or the supplied power increased from 15% to 50%. This is because the inverter-based DG inject a limited magnitude of current at higher frequencies during fault which results in a minimal effect on the proposed wideband SEFLT. This is emphasis the important of the used wideband approach for modern IPS/Microgrid where high penetration of inverter-based DG is predicted.

Finally, a new combined methodology of using the SEFLT and DEFLT to locate and discriminate between possible fault locations in the multi-tapped line was studied and demonstrated via simulation. The SEFLT is used to estimate the distance to the fault while the DEFLT is used to discriminate between the possible fault locations. Combining both techniques actively located the fault on multi-tapped system using only the measurements from two ends.

Chapter 6 - Experimental Validation

6.1 INTRODUCTION

Experimental validation will be explored in this chapter, which starts with a description of the system, setup, and calibration. Data collection and processing will then be described followed by the validation of the DEFLT and SEFLT approaches.

6.2 Experimental system

6.2.1 System overview

A simple tapped circuit is used for the experimental verification. The circuit consists of 16 mm 5 core transmission cable as well as two tapped cables with the same cross-section area, and a resistive load connected to the main cable terminal as shown in Figure 6-1. The exact lab setup is presented in Figure 6-1(a). Figure 6-1(b) presents the single-line diagram which shows that the main cable is subdivided into four sections of which three sections have the same length. Moreover, the two tapped cables are connected to the end terminal of section 2 "bus 3".

The rig is supplied directly form the local transformer at 415V, 50 Hz. Each bus interconnect is contained in a plastic box, including all connectors and control equipment as shown in Figure 6-1(a). The load is connected in star with 64Ω per phase to the receiving end which is bus 5. Note that the sending end (POM1) represents the source-end where the power flows from, while the receiving end is the end where the load is connected and the power flows toward it.

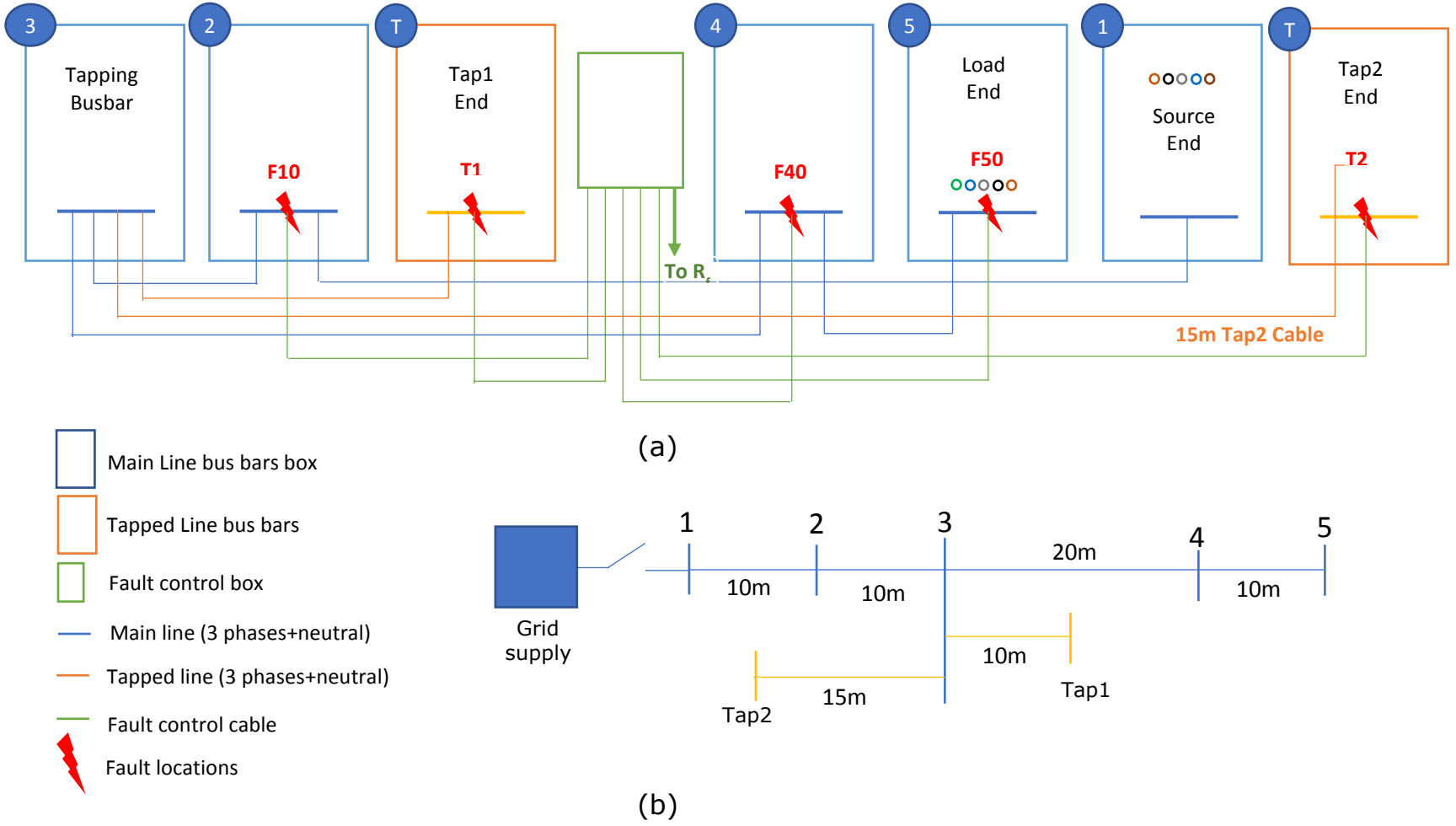


Figure 6-1 structure of the Rig: (a) Lab Setup (b) Single-line diagram of the setup

Line to neutral and Line to Line faults can be imposed separately at five locations as marked in Figure 6-1 in order to create various fault conditions. Two sets of voltage and current sensors are placed in box 1 and box 5. The final setup is shown in Figure 6-2.

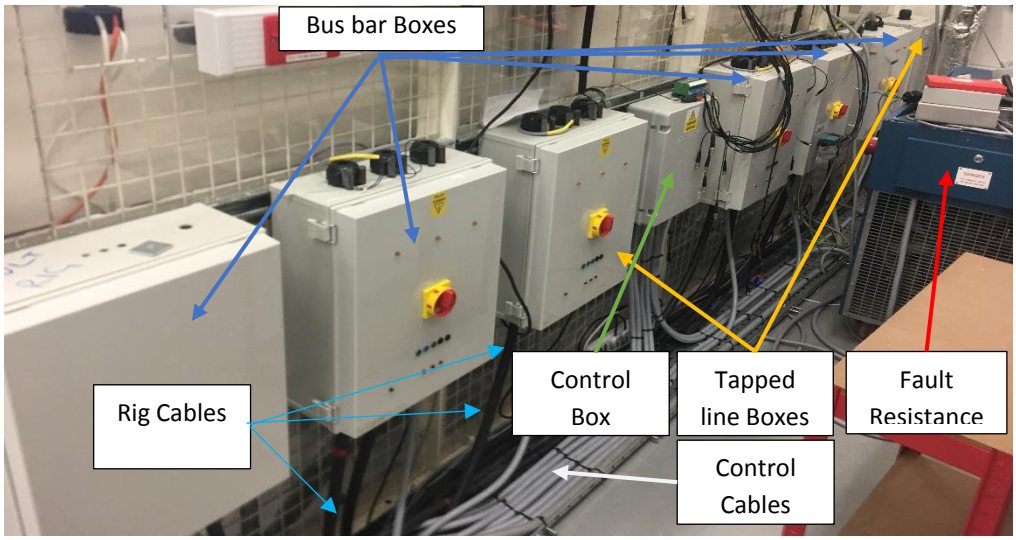


Figure 6-2 Final Setup

Mechanical contactors placed in the control box are used to impose the fault in any of the five possible places. The Rig Cables are placed under the boxes inside the laboratory cable trenches while the control cables connect directly between fault location and the fault resistance.

6.2.2 The calibration of the cable impedance

A precise knowledge of the cable impedance is very crucial for this kind of fault location approach as discussed in earlier chapters. The distance is calculated by comparing the estimated impedance with the calibrated per-metre line impedance. Therefore, the cables used in the rig have been calibrated over a specific of frequency range using an impedance estimating tool, the Impedance Analysis Interface (IAI) [87] shown in Figure 6-3.

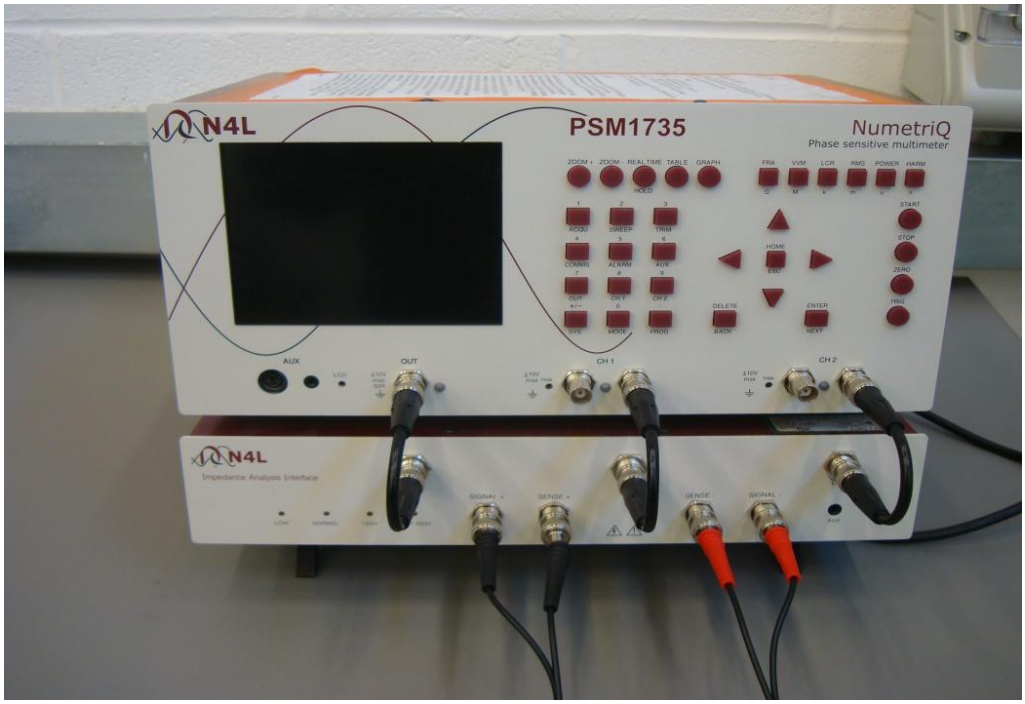


Figure 6-3 Impedance Analysis Interface (IAI)

The equipment is composed of a N4L impedance analyser with an LCR measurement capability attached to a PSM1735 phase sensitive multimeter [87]. The IAI provides a wide range frequency. An accurate calibration is achievable. The open and short circuit calibration function reduces the effect of the contact resistance on the impedance measured by the IAI. A frequency range between 500Hz to 5000 Hz is used for the calibration due to the better SNR characteristic over this range, and it is a similar range to that used by the DEFLT and SEFLT. The calibration results are summarized in Table 6-1 for Brown-Blue cores and Brown-Black cores while Table 6-2 is between black-blue cores. The calibrated cable distance is shown in the top row of the Tables while the calibration frequency is given in the left column. The second column from the left presents the calibrated value of inductance and resistance in μH and mΩ respectively for each single calibration frequency.

Table 6-1 IAI calibration for brown-blue cores and brown-black cores

Freq. \ length		10	20	40	50
500	L (μH)	7.83	14.69	27.2	34.7
	R (mΩ)	28.5	54.2	108.4	142.8
1000	L (μH)	7.7	14.85	26.9	34.0
	R (mΩ)	29.7	25.8	114.9	150.9
1500	L (μH)	7.54	14.6	26.4	33.4
	R (mΩ)	32.7	64	125.2	163.8
2000	L (μH)	7.44	14.4	25.9	32.8
	R (mΩ)	35.36	70.0	136.8	178.3
2500	L (μH)	7.36	14.1	25.4	32.3
	R (mΩ)	38.7	76.4	150	194.4
3000	L (μH)	7.25	13.9	25.07	31.8
	R (mΩ)	42	83.5	162.5	210.7
3500	L (μH)	7.17	13.77	24.7	31.32
	R (mΩ)	47.5	94.4	175.6	227.8
4000	L (μH)	7.08	13.53	24.4	30.8
	R (mΩ)	49.9	97.7	189	244.2
4500	L (μH)	7.0	13.42	24.0	30.5
	R (mΩ)	52.7	104.5	201.89	260.9
5000	L (μH)	6.93	13.36	23.7	20.2
	R (mΩ)	56.5	111.6	214.0	277.2

It is important to notice that the calibration shows the reactance slightly decreases proportionally as the frequency increases. This is because the injected magnitude of the current is not controllable and reduces with frequency. For example, for a smaller impedance measured at higher frequency, the result is less accurate than that measured at lower frequency because of the low signal strength and SNR in the high frequency range. As seen in both Table 6-1 and Table 6-2, as the calibrated distance increases, the inductance and the resistance increase proportionally. Due to mutual effects and the separation between the calibrated cores, the black and blue cores show bigger impedance than the impedance of the brown-blue core.

Table 6-2 IAI calibration for black-blue cores

Freq. \ length		10	20	40	50
500	L (μH)	10.5	20.5	37.3	46.9
	R (mΩ)	29.0	55.3	106.1	132.9
1000	L (μH)	10.33	19.8	36.8	46.3
	R (mΩ)	31.4	62.16	118.0	148.2
1500	L (μH)	10.1	19.34	36.0	45.3
	R (mΩ)	35.6	70.7	134.6	169.1
2000	L (μH)	9.9	19.0	35.2	44.33
	R (mΩ)	40.2	80.0	154.0	192.6
2500	L (μH)	9.7	18.6	34.5	43.3
	R (mΩ)	45.5	90.5	173.6	217.0
3000	L (μH)	9.52	18.3	33.7	42.6
	R (mΩ)	50.5	100.7	194.0	242.7
3500	L (μH)	9.4	18.0	33.15	41.9
	R (mΩ)	55.9	111.2	213.3	267.0
4000	L (μH)	9.25	17.7	32.6	41.16
	R (mΩ)	61.6	121.7	233.1	292.0
4500	L (μH)	9.12	17.4	32.1	40.5
	R (mΩ)	66.7	132.3	252.0	316.0
5000	L (μH)	9.0	17.2	31.0	40.00
	R (mΩ)	72.00	14303	270.6	340.0

The brown, black, grey, blue and earth presents phase a, phase b, phase c, the neutral and system earth respectively. Therefore, brown-black impedance value means the impedance of phase a and the neutral.

6.2.3 Date acquisition

A National Instrument (NI) data acquisition unit has been used to collect data from the experiment rig and store it on the PC for analysis. The unit used is presented in Figure 6-4. The unit consists of two main parts; NI CompactDAQ Four-Slot USB Chassis (NI cQAD-9147) [88] and the acquisition part (NI 9222) [89].

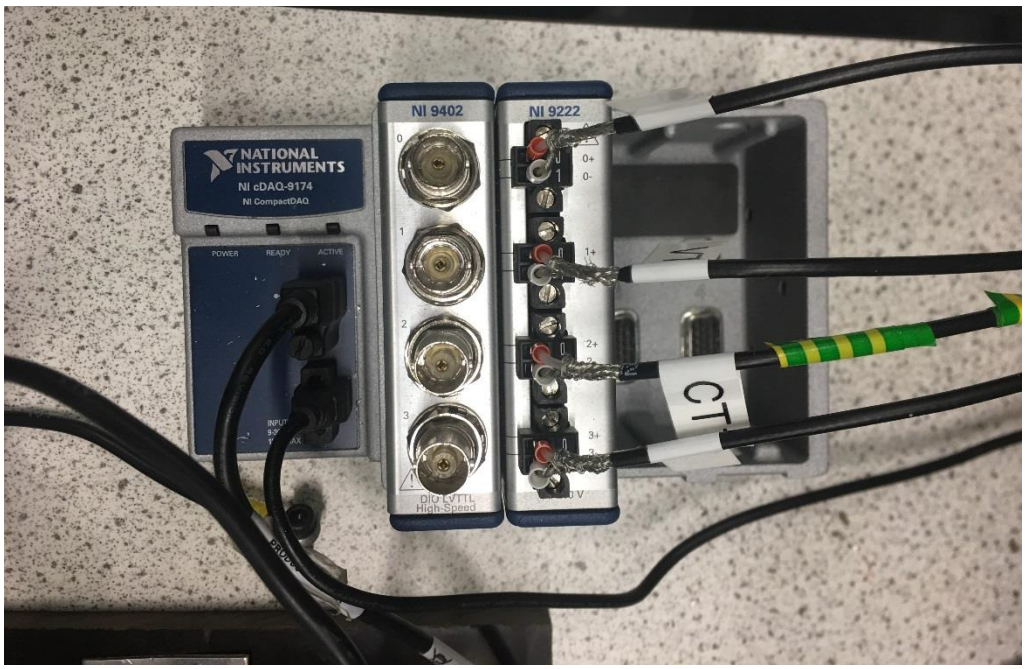


Figure 6-4 NI data acquisition unit

The chassis has slots for four acquisition units. Figure 6-4 shows two docked units. However, only one NI 9222 unit is used in the experiment which is enough to capture two sets of voltage and current from both terminals of the main cable of Figure 6-1. The maximum achievable sampling time of this unit is 500k/s with a 16 Bit Analog to Digital Converter (ADC) which offers a high resolution. The Main advantage of this data acquisition unit is the ease of interface to MATLAB which is the software used for storing and analysing the fault data. The unit is connected to the PC through a USB connector. Input signals on each channel are buffered, conditioned, and then sampled

by an ADC as shown in Figure 6-5. Each Analog Input (AI) channel of the NI-9222 provides an independent signal path and ADC, enabling the sampling of all channels simultaneously.

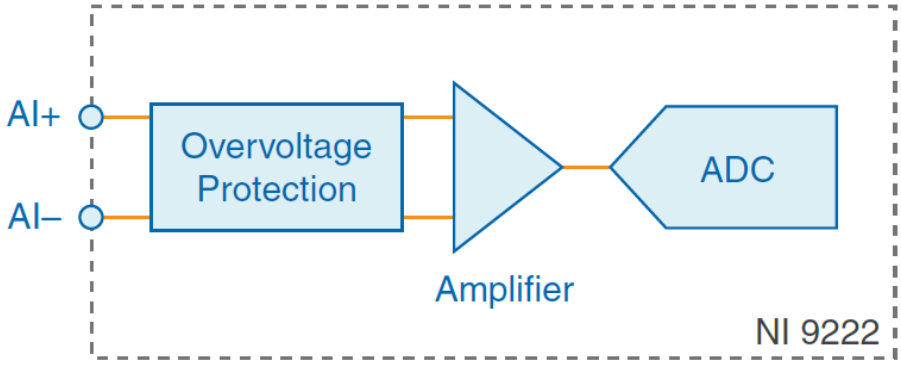


Figure 6-5 NI 9222 Input circuitry [89]

6.2.4 Data processing

An analogue low pass filter (LPF) is used to filter the measured voltage and current from both terminals in order to reduce the effect of the noise and also to eliminate aliasing effects. The filter type is presented in Figure 6-6 which is a first order RC filter with a cut-off frequency of 12 kHz. The signals are sampled and stored in the PC using the data acquisition tool described in section 6.2. A sampling frequency of 200 kHz is used to capture the data because it offers a good SNR for the required frequency range of interest.

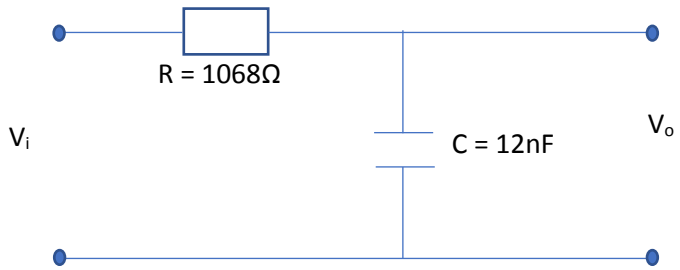


Figure 6-6 First order LPF

6.3 Experimental Verification for DEFLT

In this section, the experimental validation of the DEFLT is carried out. The SEFLT is then demonstrated. Finally, the combined approach of the single-ended and double-ended methods for locating a fault on a tapped line will be presented.

6.3.1 Demonstration of DEFLT

The double-ended fault location technique will be demonstrated in this section. Two sets of voltage and current are measured from the source end (Bus 1) and the receiving end (Bus 5) of Figure 6-1 (b). The captured data from both ends for a typical fault between line and neutral are shown in Figure 6-7 while for a line-line fault are shown in Figure 6-8. According to the double-ended theory presented in chapter 3, only the measurements of the faulted phases are required for the calculation of the fault location and will be presented throughout this section.

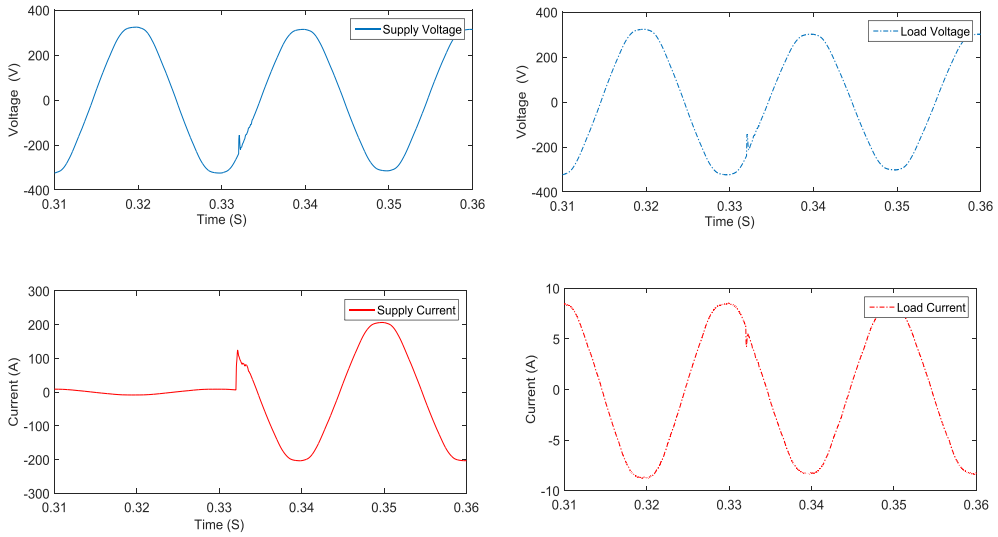


Figure 6-7 Typical measured data from both ends for the line-to-neutral fault

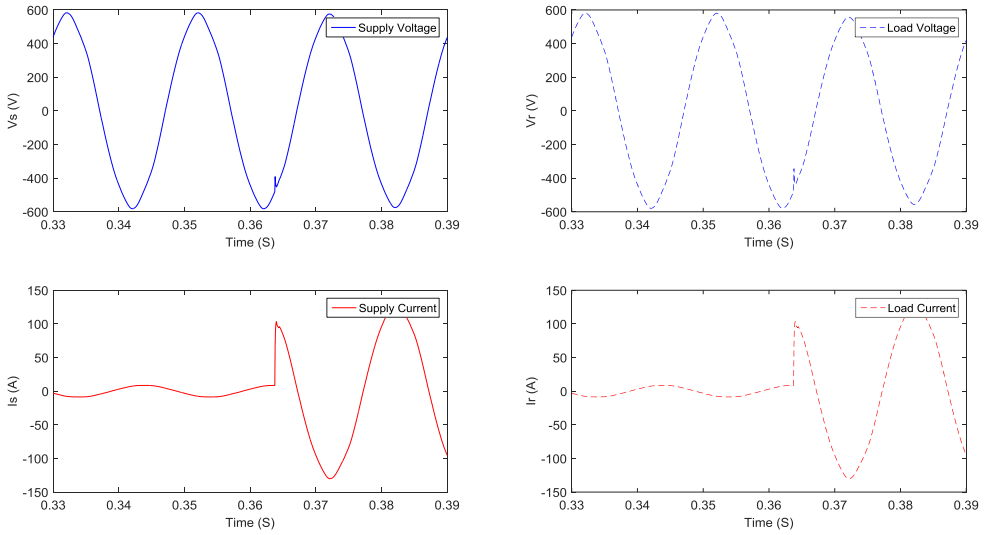


Figure 6-8 Typical data from both ends for the line-line fault

6.3.2 DEFLT using all measurements available

To verify the DEFLT, a fault with a finite fault resistance is applied in the system by a manually controlled a mechanical contactor [90] as shown in Figure 6-9 in order to emulate a realistic fault. The first test is carried out with a line-to-neutral fault and a resistive load at the receiving end (bus 5) as described in the experimental setup. Different fault resistances are imposed separately at five different locations of the system.

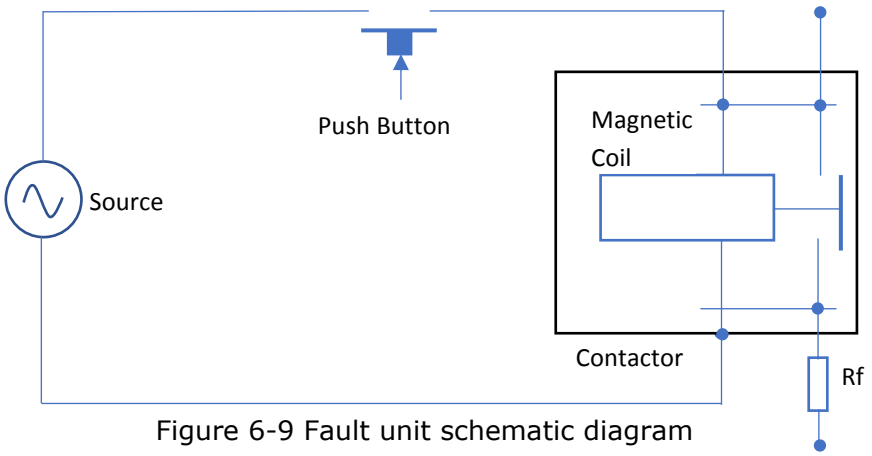
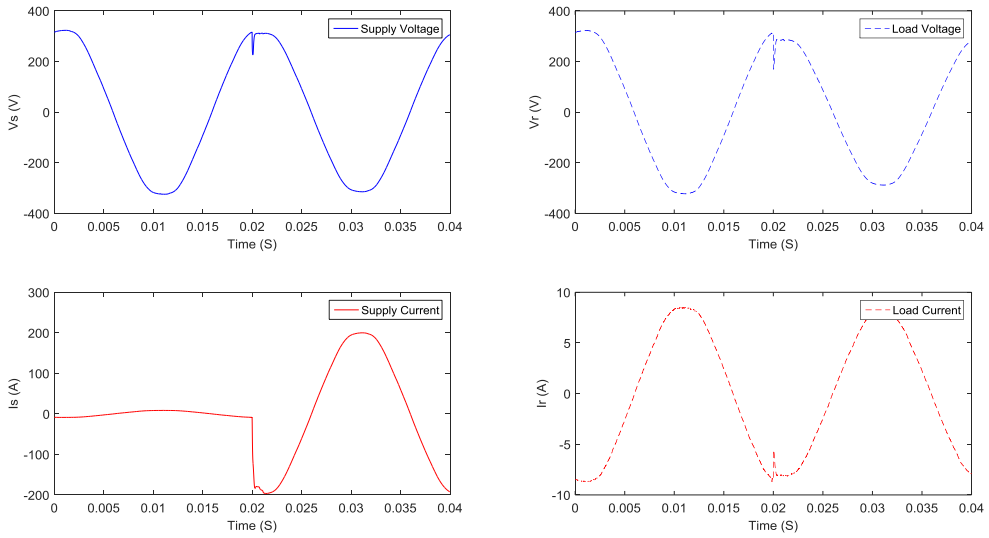
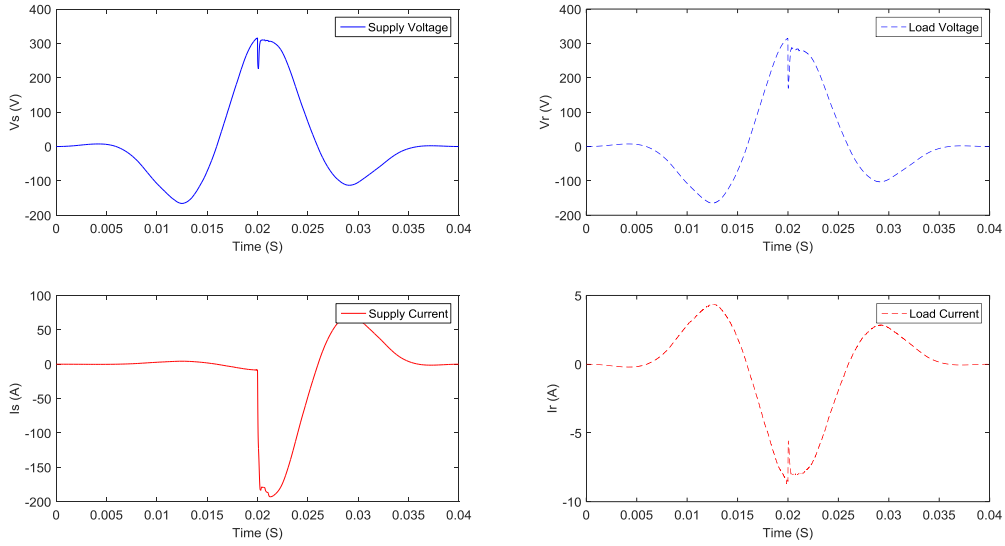


Figure 6-9 Fault unit schematic diagram

Two cycles of voltage and current from both terminals are measured, low pass filtered and then sampled in order to be digitally processed. The two cycles consist of a pre-fault cycle and a during fault cycle. A Blackman window is applied to the data in order to remove the effect of edge leakage. A fault condition between line and neutral with 1.45Ω resistance was imposed at the receiving end terminals F50, and the measured data are shown in Figure 6-10.



(a)



(b)

Figure 6-10 (a) Measured waveforms (b) windowed waveforms

The windowed data is then transferred to the frequency domain using the FFT algorithm available in MATLAB [91]. The magnitude of these measurements in the frequency domain is shown in Figure 6-11. The receiving end current is clearly more affected by the noise compared to other signals as it has a much smaller amplitude. On the other hand, the source end current is less affected by the noise due to the significant step transient generated by the fault in which gives a better SNR over a wide frequency range.

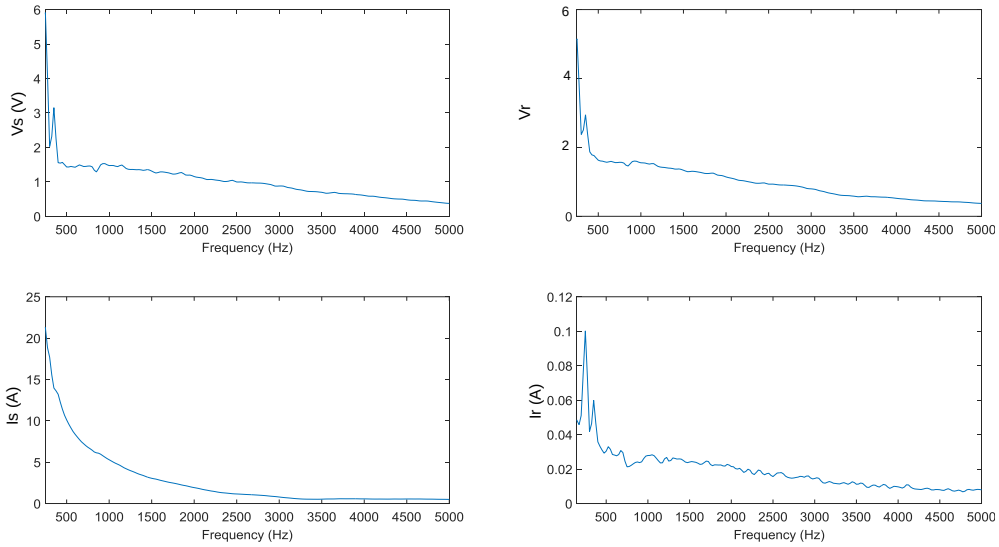


Figure 6-11 The magnitude of the measured data in the frequency domain for a fault a the receiving end (F50)

Finally, the reactance between the source end (bus 1) and the fault location is calculated using (3.2). The estimated reactance (red dash-dotted line) (Xest.) is given in Figure 6-12 and compared with actual line reactance (green dashed line) (Xact.) and the calibrated reactance (blue solid line) (X-calibration from Table 6-1). The difference between Xact. and X-Calibration is that Xact. uses the inductance at 1kHz from X-calibration and assume it is the same over the 50-3000Hz range. The distance is calculated by dividing the estimated reactance by the per-metre inductance of Xact., in this case, the distance is 50.1m. As mentioned in the simulation chapter, the

resistance is neglected because the reactance dominates at higher frequencies as well as to remove the effect of the fault resistance on the final estimation.

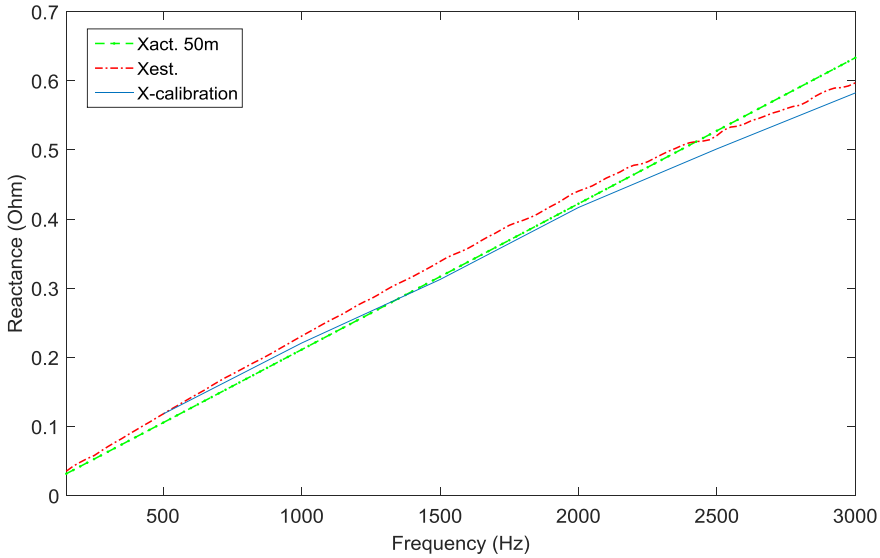


Figure 6-12 Estimated reactance using (3.2)

Close observation of Figure 6-12 shows a good match between the actual and the estimated reactances. Three more line-to-neutral fault tests at F10 (10m from Source end), F20 (20m from source end, the fault is on tapped line) and F40 (40m from source end) were carried out. The estimated reactance for the three tests is summarized in Figure 6-13. The estimated fault distance for the three tests is 38.75m, 20.3m and 9.36m respectively. The distance is calculated by dividing the estimated reactance by the actual reactance at each frequency and then taking the average. The presented results show a good accuracy, with the largest error in distance being 1.25m. The same test procedure was repeated but with a higher fault resistance (Rf = 4.5Ω) in order to demonstrate the double-ended technique under different fault resistances. The estimated reactance using (3.2) is summarised in Figure 6-14. Compared with the calibrated reactance, the estimated reactance shows an excellent accuracy. On the other hand, the accuracy is slightly reduced when compared to the "actual" line reactance. This is

because the actual reactance assumes the same inductance value at each frequency, whereas the calibration shows the inductance reduces with frequency.

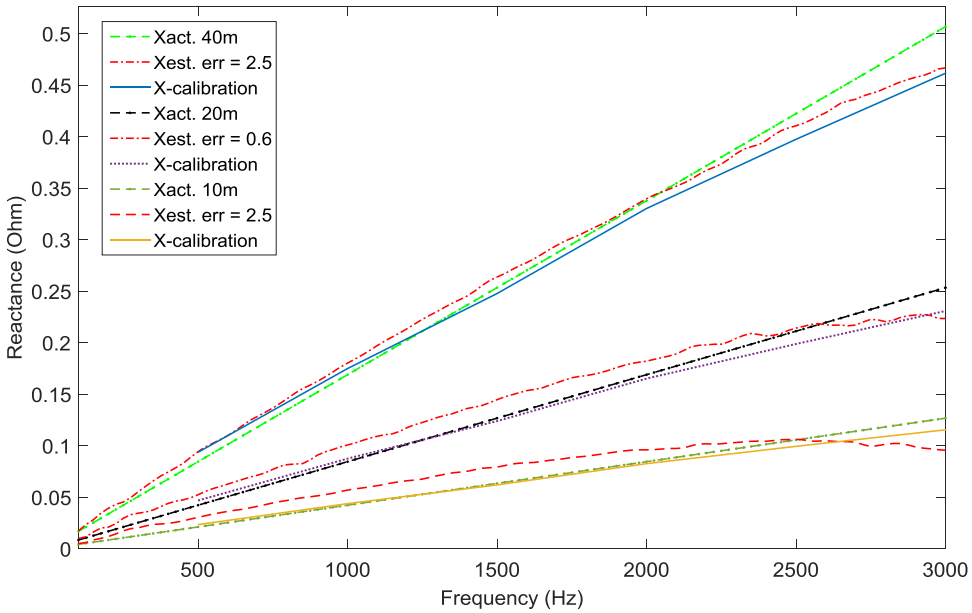


Figure 6-13 Estimated reactance for three fault tests, Rf = 1.45Ω

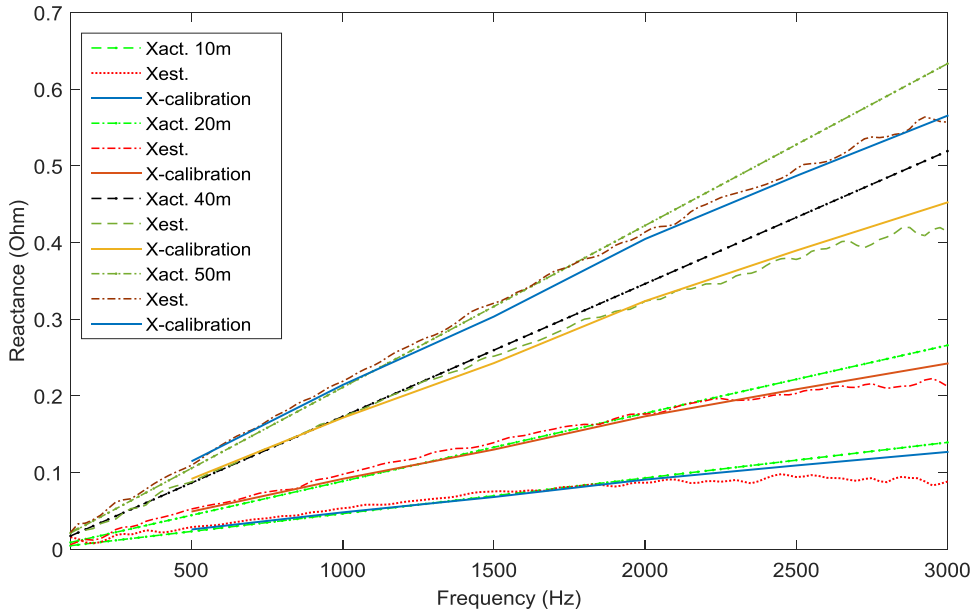


Figure 6-14 Estimated reactance for four fault tests, Rf = 4.5Ω

It is necessary to point out that the F20 test is actually imposed on the tapped line of the system of Figure 6-1. The estimated reactance using (3.2)

showed that the fault is 20m from the source end. This demonstrates the theory studied in Section 4.3. The double-ended method considers the tapped line as part of the fault resistance. The estimated distance and the calculated percentage error of the total distance for a line-neutral fault with R_f = 1.45Ω and R_f = 4.5Ω are summarised in Table 6-3. The error increases when R_f increases. This is due to the weaker generated fault transient as R_f increases. However, the maximum error is 4% which is still within an acceptable range of distance error of 2m.

Table 6-3 Estimated distance and percentage error

Act. Fault distance (m)	**(Rf = 1.45Ω)**		**(Rf = 4. 5Ω)**	
	Est. Fault distance (m)	**Error (%)**	**Est. Fault distance (m)**	**Error (%)**
10	9.36	-1.28	9	-2.0
20	20.3	0.6	19.23	-1.5
40	38.75	-2.5	38.0	-4.0
50	50.1	0.2	48.05	-3.9

The DEFLT is further tested with a line-line fault. The fault resistance used for this test is 4.5Ω in order to limit the fault current to the rating of the Current Transducers (CT). A sample of the captured data is shown in Figure 6-15. The estimated reactance for all the possible fault locations is summarised in Figure 6-16. The results show a high accuracy compared to the calibrated reactance. The most significant error in estimated fault distance is 1.25m with an estimated distance of 8.75m for F10.

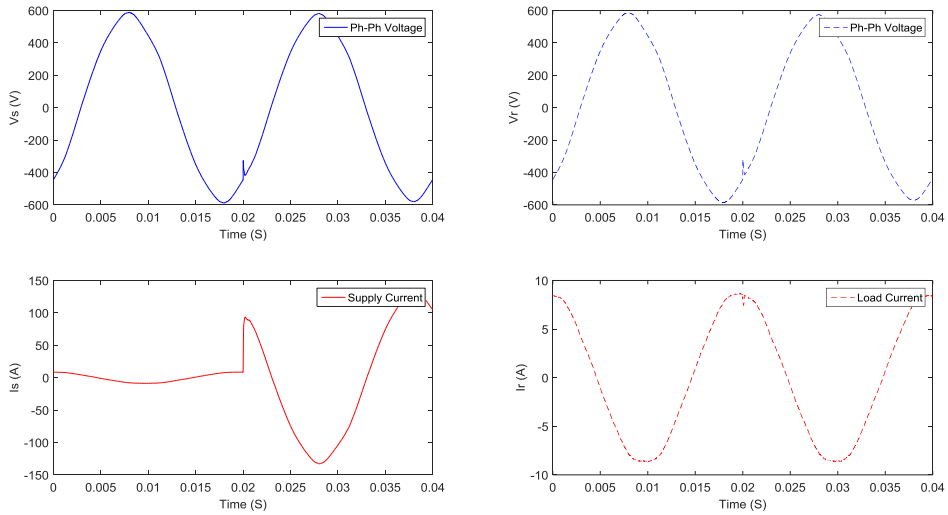


Figure 6-15 Captured time domain data for a typical Line-Line fault

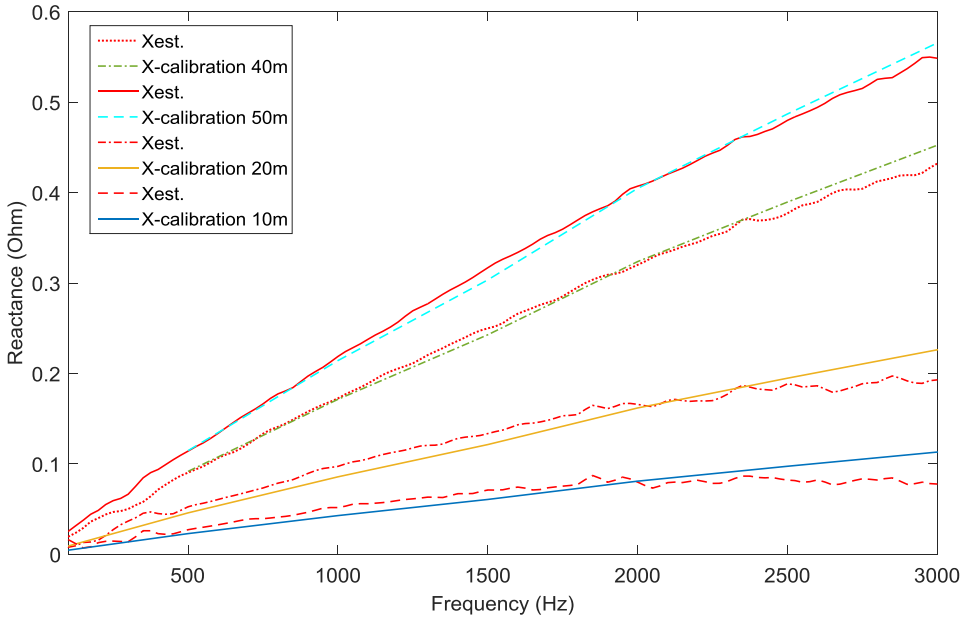


Figure 6-16 Estimated reactance for Line-Line fault using (3.2)

6.3.3 DEFLT ignoring Ir

The DEFLT will be implemented in this section using only three measurements. In this approach, the source end voltage and current as well as the receiving end voltage will be required. Equation (3.2) will be approximated by (6.1) which will be used in this section.

$$Z_x = \frac{V_r - V_s}{I_s} \tag{6.1}$$

where V_s, I_s are the source end voltage and current, V_r is the receiving end voltage. Compared to (3.2), I_r is neglected in the denominator because at non-fundamental frequencies, $I_r << I_s$. Similarly, $I_r * Z_{line}$ in the nominator of (3.2) will be very small compared to $V_r - V_s$, hence, neglecting it has a limited influence on the estimated reactance.

Two line-neutral fault tests (F20 and F40) are used in order to demonstrate this approach. In Figure 6-17 for F20, the estimated reactance using (6.1), blue solid line is compared to the estimation using (3.2), the dash-dotted red line. It is clear that the difference is very small and only appears in the frequency range of 2-3 kHz. This is verified looking at the frequency domain of the signals used in Figure 6-18 which shows that $I_r(f) \ll I_s(f)$ as well as $I_r * Z_{line} \ll V_r - V_s$. Similar behaviour resulted when a fault was imposed 40m from the source-end (F40) which is shown in Figure 6-19 and Figure 6-20.

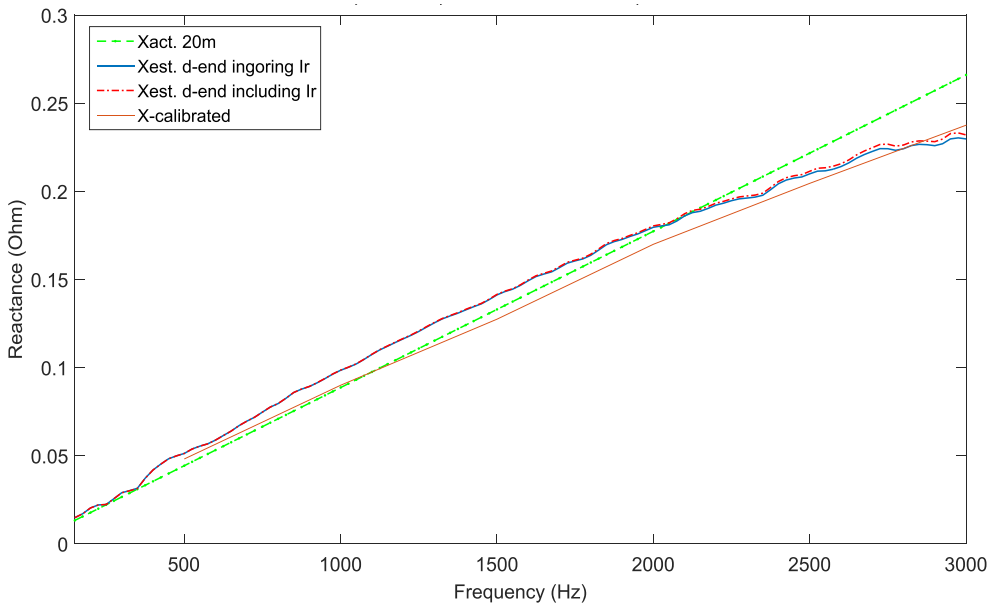
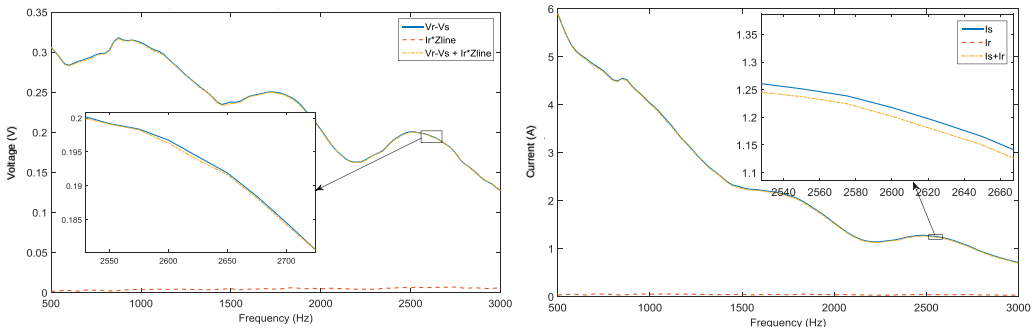


Figure 6-17 Estimated reactance using approximated DEFLT for fault at F20



(a) (b)

Figure 6-18 Comparison of captured data in the frequency domain for F20 for DEFLT(a) $I_r * Z_{line}$ and $V_r - V_s$ (b) $I_r(f)$ and $I_s(f)$

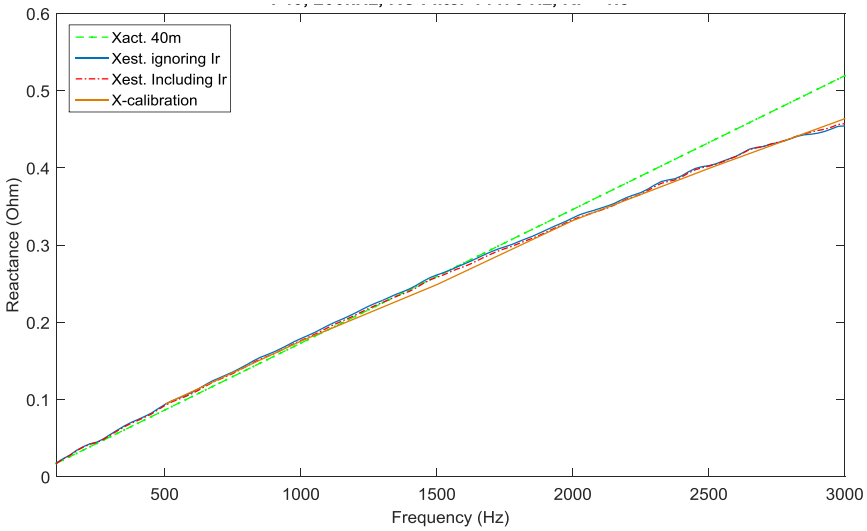
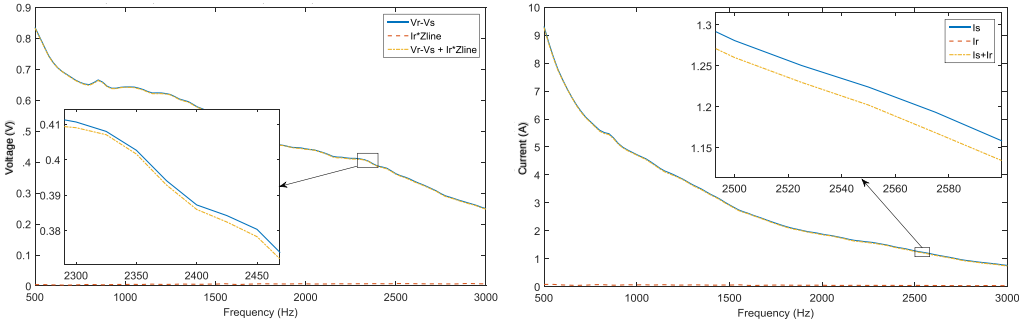


Figure 6-19 Estimated reactance using ignored Ir approach for F40



(a) (b)

Figure 6-20 Comparison of captured data in the frequency domain for F40 for DEFLT (a) $I_r * Z_{line}$ and $V_r - V_s$ (b) $I_r(f)$ and $I_s(f)$

6.3.4 Effect of tapped loads

The investigation of the tapped load effect on the full DEFLT is investigated in this section. A 10Ω resistor is used as a load on the Tap1 terminal and a 91Ω on the Tap2 terminal in addition to the 37Ω main load on the receiving end terminal (Bus 5). Faults on the main line with Rf = 4.5Ω are used for testing the double-ended method. Examples of the measured signals are shown in Figure 6-21 with the frequency domain shown in Figure 6-22.

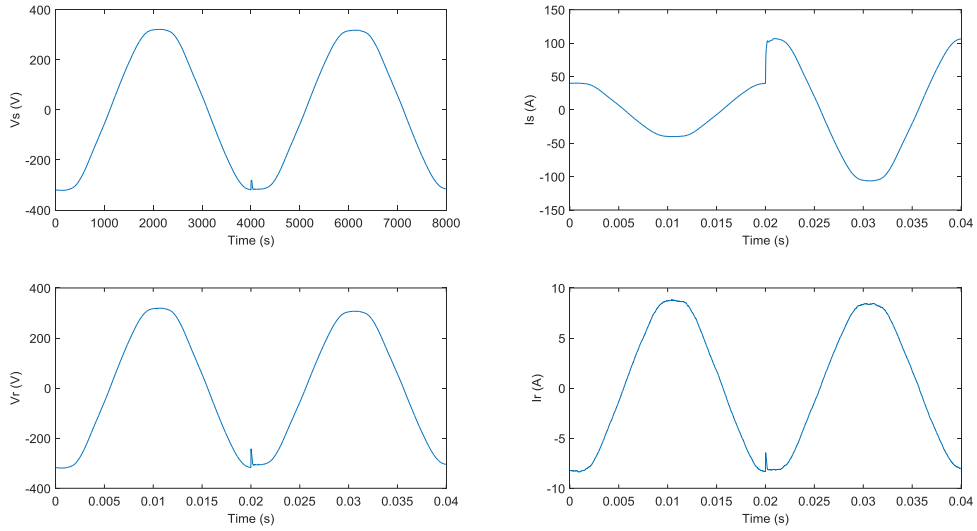


Figure 6-21 Measured signals from both ends for F50 for fault with tapped load

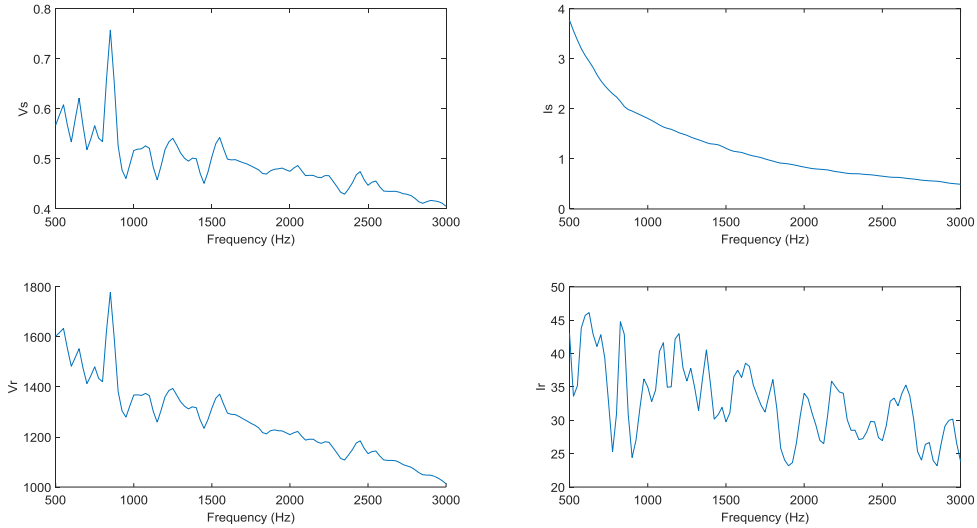


Figure 6-22 Measured signals from both ends for F50 in Frequency domain for fault with tapped load

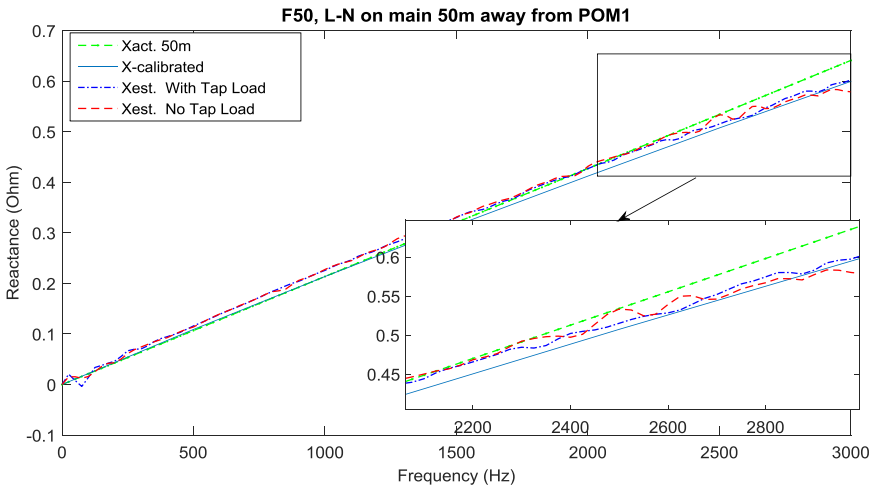


Figure 6-23 Estimated reactance for F50 using the d-ended method

The estimated reactance (blue dash-dotted line) is shown in Figure 6-23 and compared to the case with an unloaded tapped line (red dashed line). It is obvious there is a very small effect from the ignored tapped load on the accuracy of the estimated reactance and distance. The percentage error difference between the two conditions is less than 1%. Furthermore, the estimated reactance for F40 and F10 on the main line are shown in Figure 6-24 and Figure 6-25 respectively.

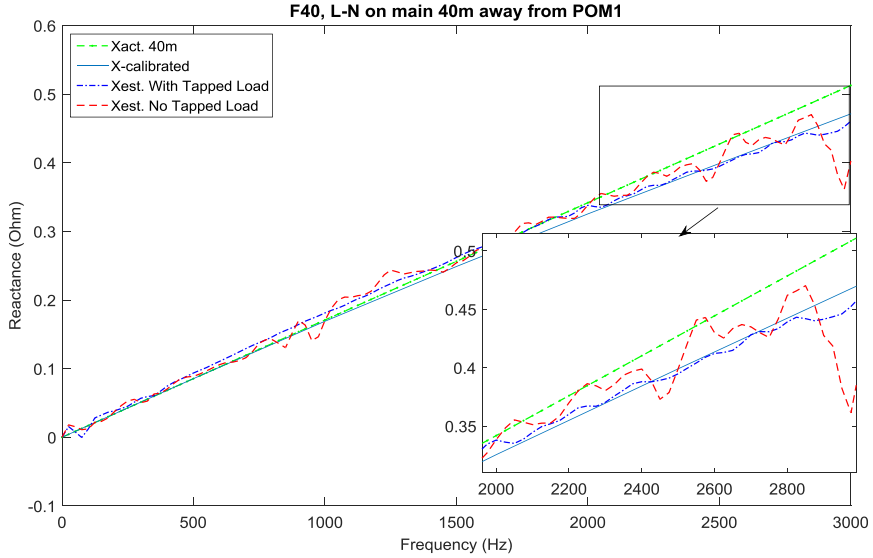


Figure 6-24 Estimated reactance for F40 using the d-ended method

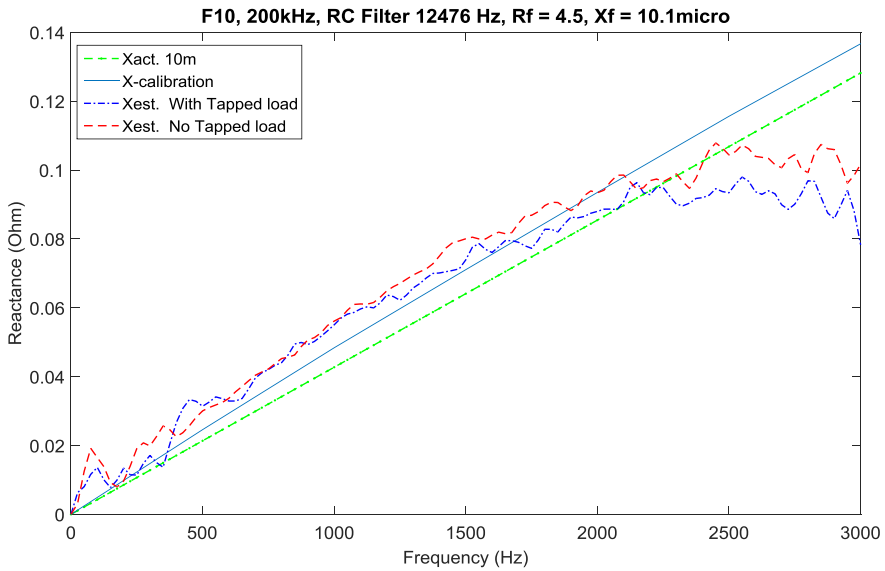


Figure 6-25 Estimated reactance for F10 using the d-ended method

The three fault tests shown above demonstrate that the DEFLT works reliably with the presence of the tapped load between the POMs. Although, the resistance at Tap1 is three times smaller than the resistance at receiving end in the three tests, the percentage error is only influenced by 2% for F10 especially in the frequency range 2-3 kHz. It is less than 1% for F40 and F10 for the same fault condition. The percentage error is summarised in Table 6-4.

Table 6-4 percentage error calculation

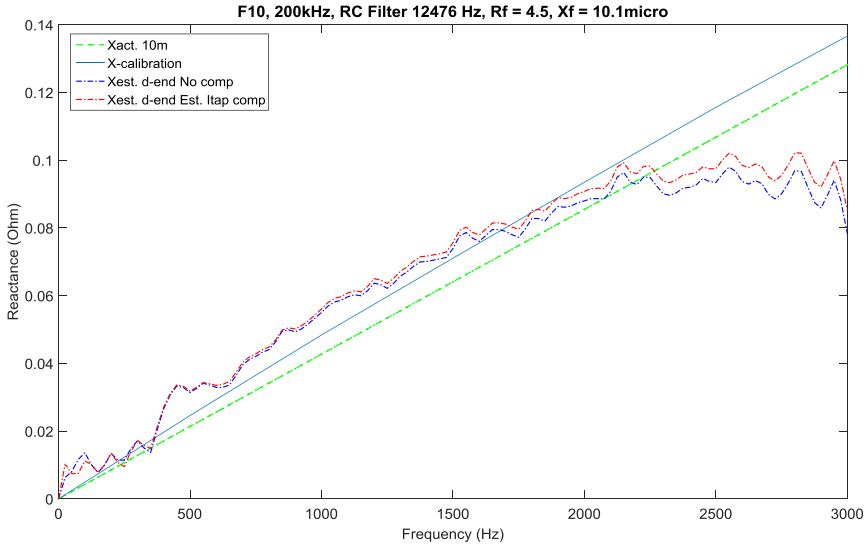
Act. Fault distance (m)	**Rtap = none**		**Rtap = 10 Ω**	
	Est. Fault distance (m)	**Error (%)**	**Est. Fault distance (m)**	**Error (%)**
10	9.0	-2	8.9	-2.2
40	38.0	-4	38.0	-4.0
50	48.05	-3.9	48.0	-4.0

In conclusion, the DEFLT offers a high accuracy estimation. Due to experimental rig CT limitation and available resistance, the tapped load was further increased in simulation from 10Ω to 1Ω in 4 steps, and the results estimated only showed a limited increase in the error up to 6%.

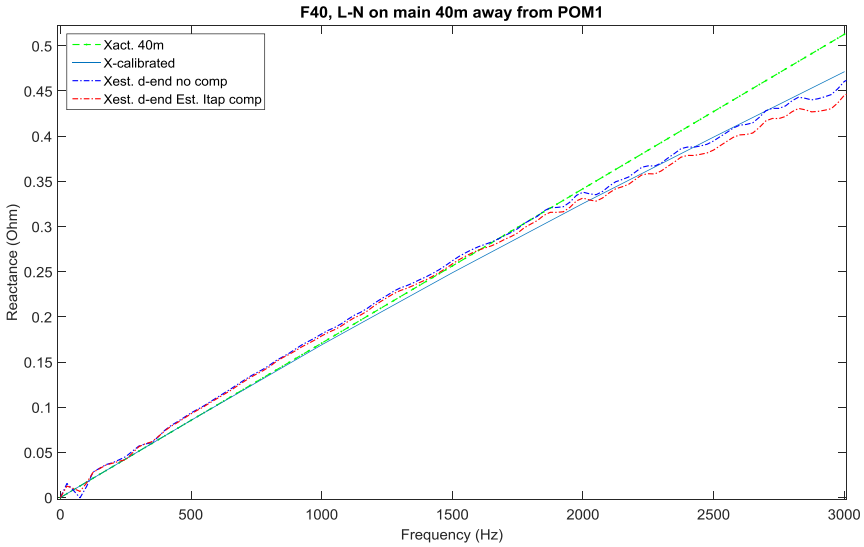
6.3.5 DEFLT with tapped load compensation

The experimental validation of the DEFLT with tapped load compensation will be explored in this section. Therefore, the same conditions used in the simulation will be applied in the experimental measurement and analysis.

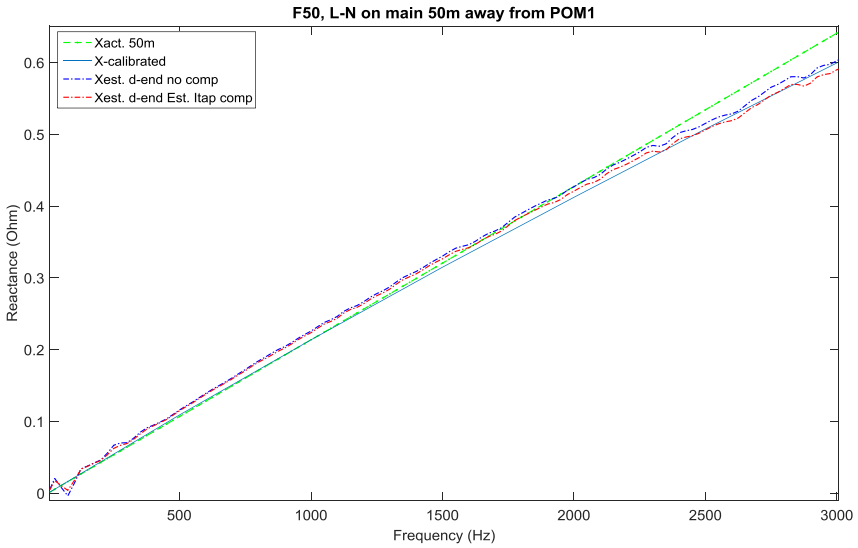
Three fault tests have been created with the same tapped load (10Ω), receiving end load (37Ω) and fault resistance (4.5Ω) in order to demonstrate the simulation results in chapter 3.5. The first fault test is between POM1 and the tapped load and the reactance estimated is presented in Figure 6-26 (a). This Figure shows the estimate from the compensated DEFLT (Red dash-dotted line) and is compared to the estimate from the non-compensated DEFLT (Blue dash-dotted line). There is clear compensation in the high-frequency range (2-3 kHz). The other two tests are for faults between the tap location and the POM2. The estimated reactance for F40 and F50 are summarised in Figure 6-26 (b and c). The Red dash-dotted line is with tapped load compensation and the Blue dash-dotted line is without compensation.



(a)



(b)



(c)

Figure 6-26 Estimated reactance compensated vs non-compensated (a) tap load between POM1 and fault (b) tap load between Fault and POM2

All the three tests show noticeable compensation even if the compensation magnitude is not exact. The reason is that the DEFLT is not highly affected by the tapped load current as demonstrated in the simulation chapter 3 and in the previous experimental test section.

6.4 Experimental validation of SEFLT

The single-ended method will be investigated in this section using the experimental setup. The section will start by applying the same approach used to estimate the fault distance in the earlier chapters (simulated results). Then, a modified approach that overcomes the main issue in the original single-ended method process will be discussed and verified. Finally, an analysis of some of the factors that affect the accuracy of the single-ended method will be presented.

6.4.1 Single-ended method

The single-ended fault location approach will be demonstrated in this section using the same experiment set up as described for earlier experimental work. The required data measurements are only the source end voltage and current. A similar approach to the d-ended method is used to impose the fault on the rig, measure the data, and filter the measurements. A sample of the captured voltage and current as well as the assumed fault voltage are shown in Figure 6-27. A fault at the load terminal (F50) is used to investigate the approach used to estimate the reactance to the fault location described in chapter 3. The measured voltage and current from POM1 are shown in Figure 6-27 (a and b) while the assumed voltage at the fault location as well as the estimated voltage for the last iteration are shown in Figure 6-27 (c) and the zoomed window in Figure 6-27 (d). These signals are windowed with a Blackman window in order to remove the effect of edge leakage. The signals are then transferred to the frequency domain as shown in Figure 6-28. Based on the algorithm used in chapter 4, the estimated reactance is presented in Figure 6-29. It is obvious there is a significant error between the actual (green dashed line) and the estimated reactance (purple dashed line).

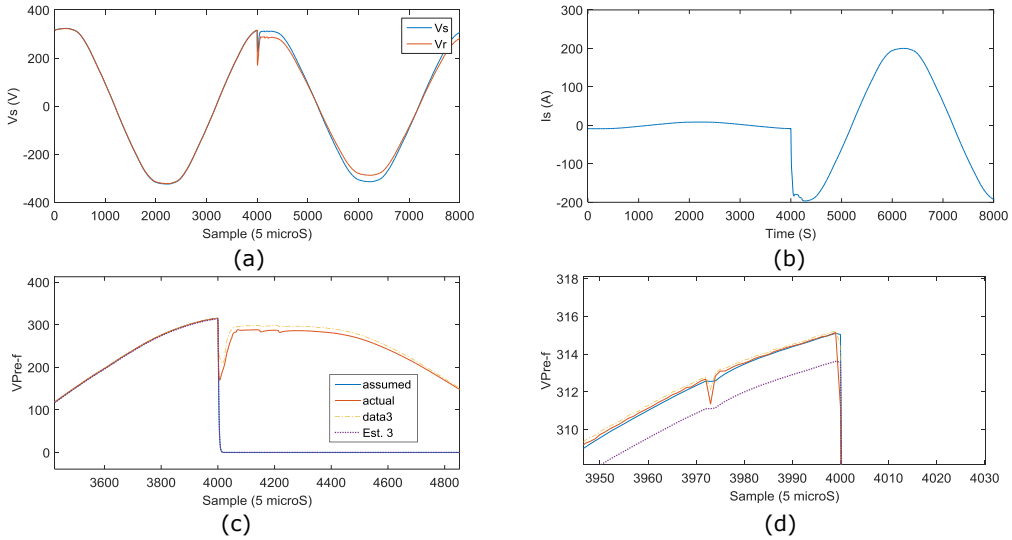


Figure 6-27 Captured and measured data for SEFLT (a) measured Voltage (b) measured current (c) assumed, measured and estimated Vpre-f for fault at F50 (d) zoomed window of Vpre-f

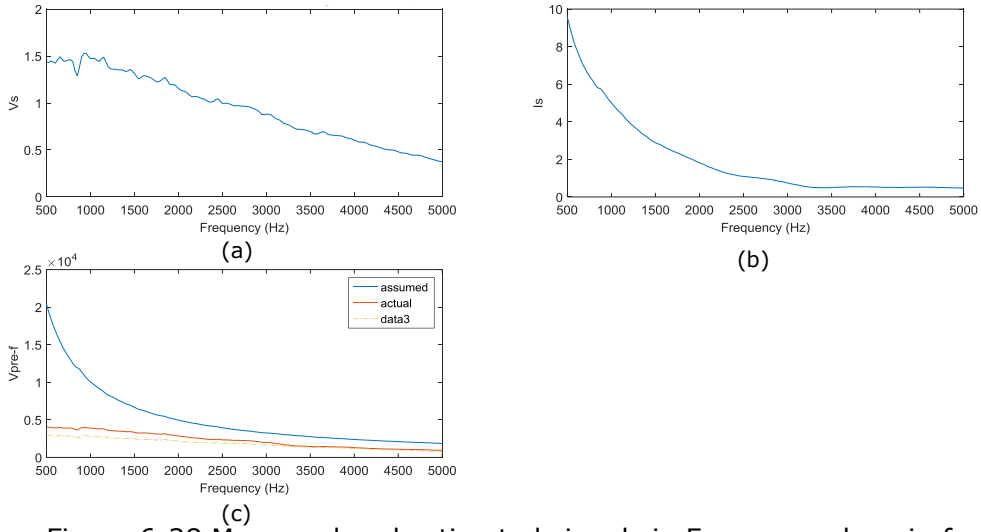


Figure 6-28 Measured and estimated signals in Frequency domain for SEFLT (a) Vs (b) Is (d) assumed, measured and estimated voltage at F50

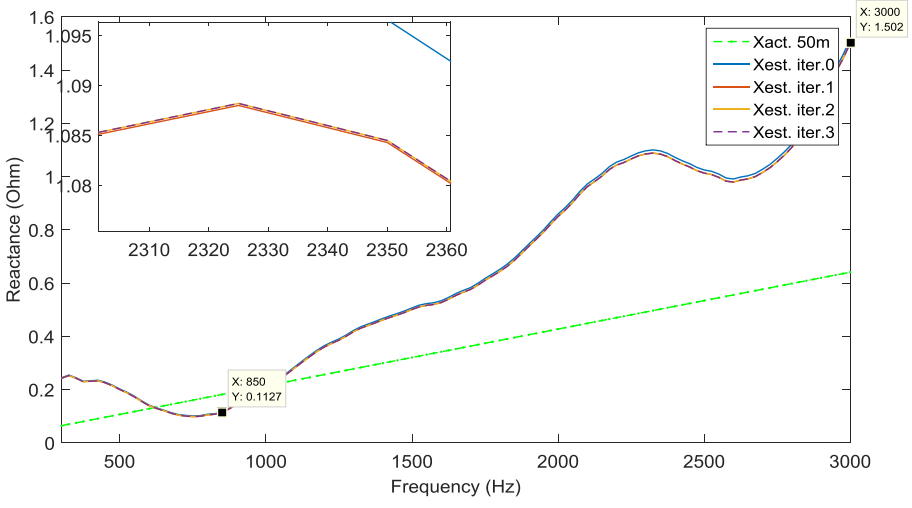
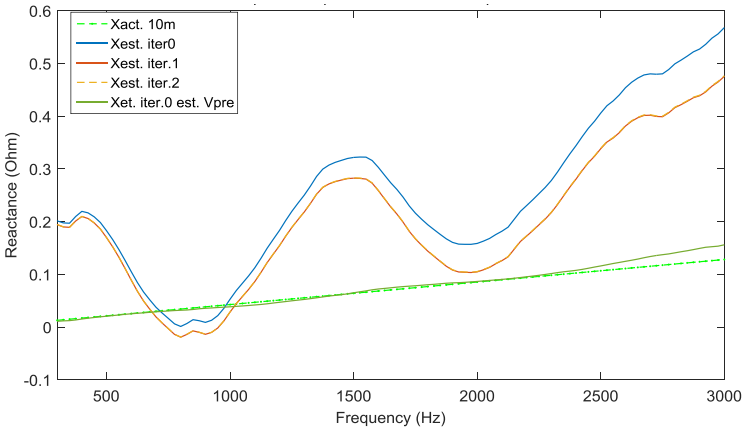
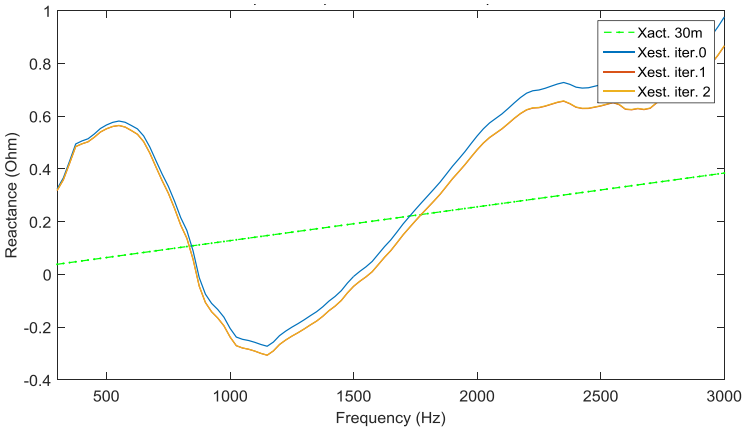


Figure 6-29 Estimated reactance for fault of 1.45Ω imposed at 50m

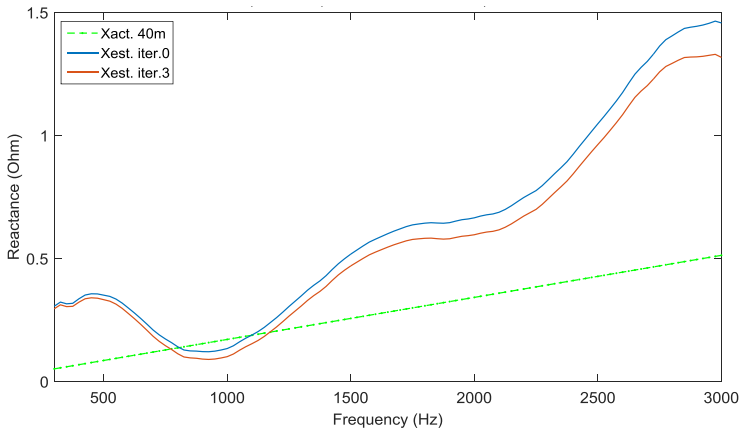
Further fault tests were carried out to prove that the iterative algorithm of (3.7) and (3.8) described in chapter 3 (simulated results) cannot be applied to the experimental measurements directly. Figure 6-30 summarises the estimated reactance for three other possible fault test locations in the experimental rig. The tested locations are F10, F30 (fault on end of tap1) and F40 respectively. All the tests are performed with R_f = 1.45 Ω. The results in Figure 6-29 and Figure 6-30 shows that the suggested approach has a potential error when it is applied to the experimental system. Therefore, a solution is required to overcome this issue which will be discussed in the next section.



(a)



(b)



(c)

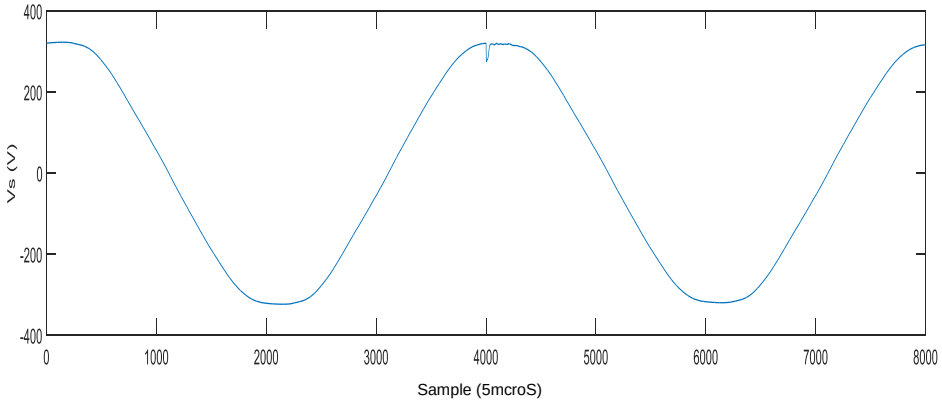
Figure 6-30 Estimated Reactance (a) F10 (b) F30 on Tap1 (c) F40

There are a few reasons for the significant error seen in these results. One of the main reasons is that the contactor used in the experimental system imposes a different transient when the fault occurs. The contactor has capacitance, and contactor bounce when it is closed, whereas in simulation the fault is imposed with a clear, single step and a step shape is assumed when reconstructing $V_{pre\text{-}f}$. Also, the system noise is larger which adds more error to the estimated reactance. Therefore, a solution is required to overcome these problems which will be discussed in the next section.

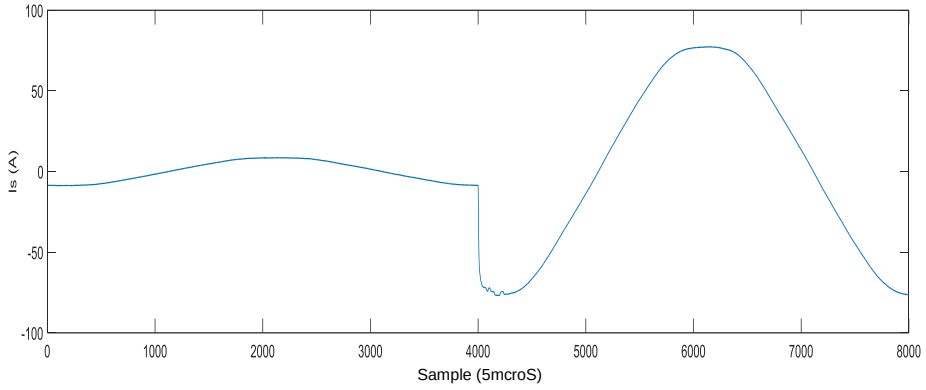
6.4.2 SEFLT using estimated fault voltage

In this section, an approach is developed to minimize the error in the single-ended approach. Therefore, changes are required in the analysis method and assumptions made at the fault location. A sample of the captured source end voltage and current as well as the assumed fault voltage for F10 are shown in Figure 6-31. The fault voltage ($V_{pre\text{-}f}$) during the fault is assumed zero. It is this assumption that leads to an adverse effect on the estimated reactance as the influence of the contactor imposed ripple on the fault

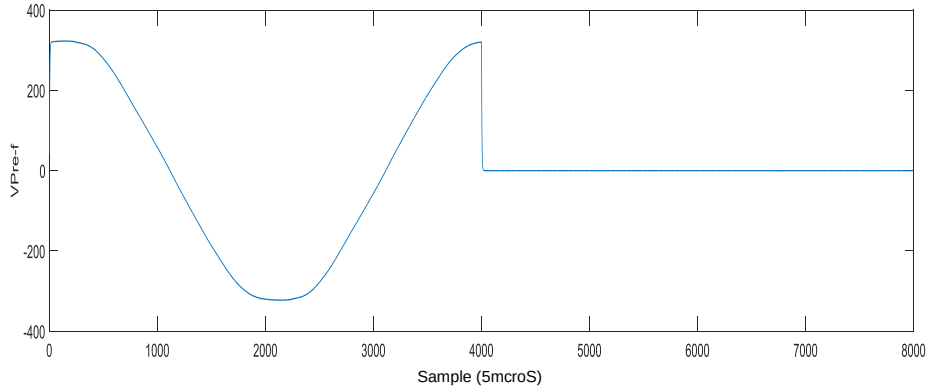
voltage is ignored. Therefore, the fault voltage during the fault time will be estimated and included in the V_{pre-f} signals.



(a)



(b)



(c)

Figure 6-31 measured and assumed signal for F10 (a) captured V_s, (b) captured I_s, (c) Assumed V_{pre-f}

These three signals are used to create an initial estimate of R_f utilizing the real part of (3.6). This estimate of R_f is then used to estimate the voltage at the fault location by applying the voltage divider rule (6.2) as the fault is assumed to be at the midline for the initial calculation as shown in Figure 6-32. A new fault distance is estimated using the measured signals at the source end as well as the estimated voltage at the fault location. This new distance is used to update Z_x in (6.2) in order to calculate a new $V_{pre\text{-}f}$ and then a new distance using (3.7). This iteration is repeated until the tolerance between two consecutive iteration converge to pre-set tolerance (such as 0.5m). The flow chart in Figure 6-33 shows the amended SEFLT to estimate the fault location which is slightly different from the flow chart used for the simulation work, as shown by the shaded blocks.

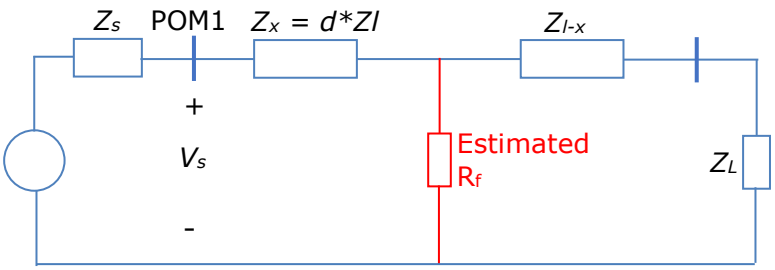


Figure 6-32 Assumed circuit during fault

$$V_{pre-f} = V_s * \frac{R_f}{d*Z_l + R_f} \tag{6.2}$$

Where R_f is the estimated fault resistance, Zx is the impedance between the fault location and POM1 whereas Vs is the voltage measured at the POM1.

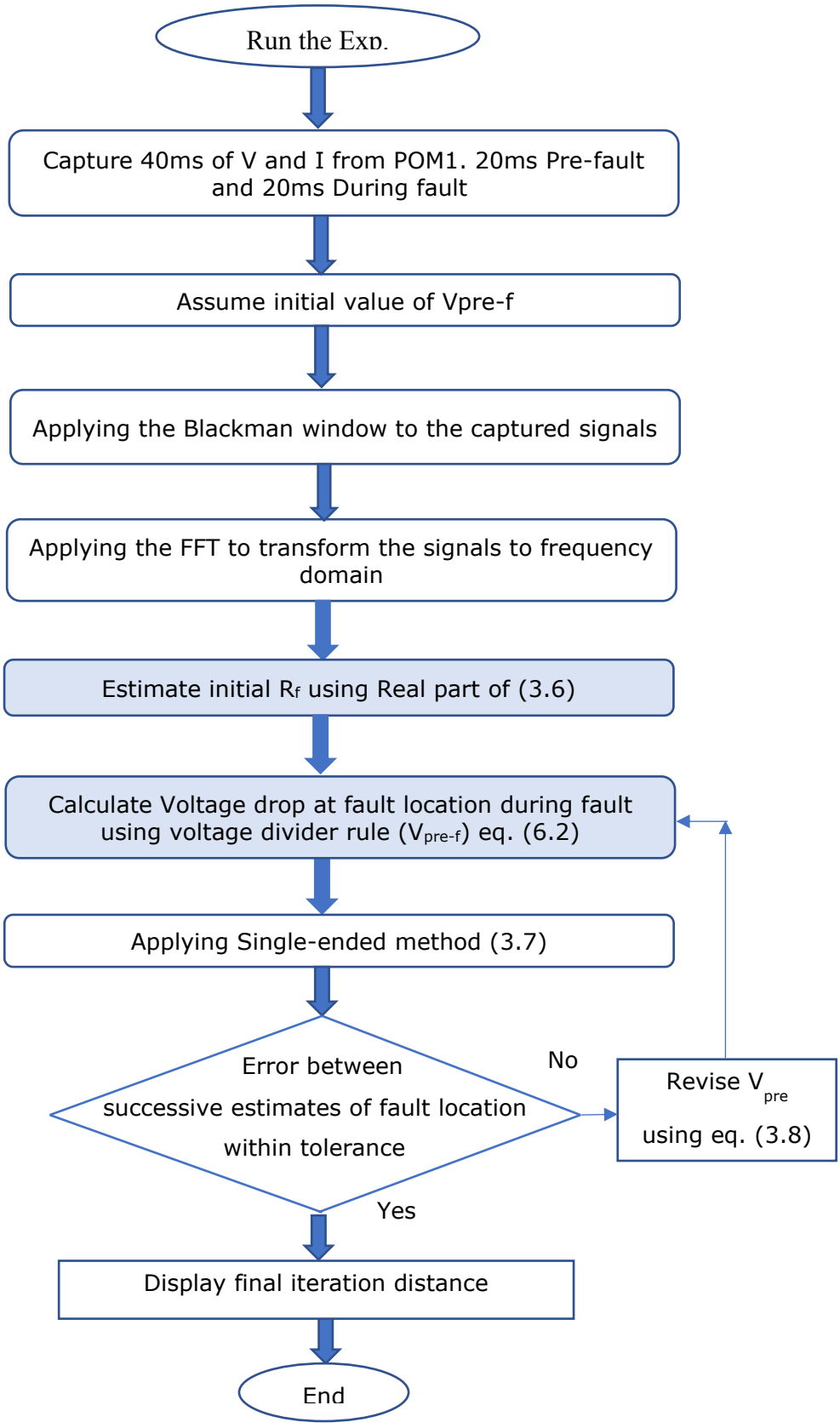


Figure 6-33 Single-ended method procedure

The proposed method in Figure 6-33 has been validated by examining different fault scenarios. The first scenario is to impose a line-neutral fault at four different possible locations in the experimental rig. Starting with a fault imposed close to the source terminal with a fault resistance (R_f) of 1.45Ω, the captured data as well as the assumed voltage at the fault location ($V_{pre\text{-}f}$) are shown in Figure 6-34. Two cycles of the measured voltage and current are given in Figure 6-34 (a) and (b), while (c) shows the initial assumed voltage at the fault point as well as the estimated voltage. Figure 6-34 (d) is the zoomed window of the estimated $V_{pre\text{-}f}$ plotted against the actual $V_{pre\text{-}f}$ measured from the test Rig. The assumed $V_{pre\text{-}f}$ in addition to the captured source end values are transferred to the frequency domain using the FFT method as presented in Figure 6-35.

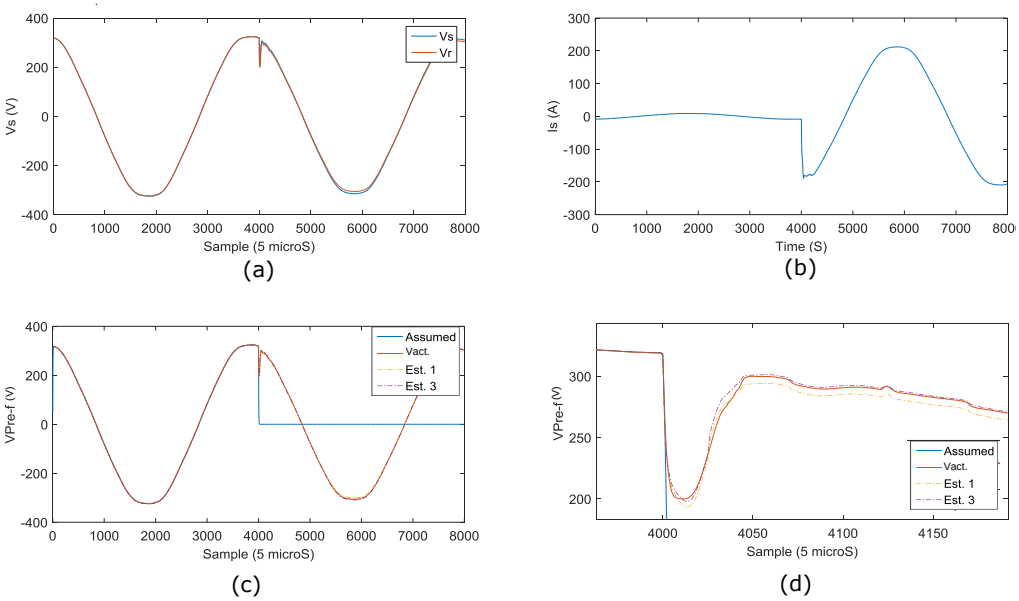


Figure 6-34 Captured, assumed and estimated signals for modified SEFLT (a) source voltage (b) source current (c) actual, assumed and estimated fault voltage at 10m (d) Zoomed window of estimated and assumed fault voltage

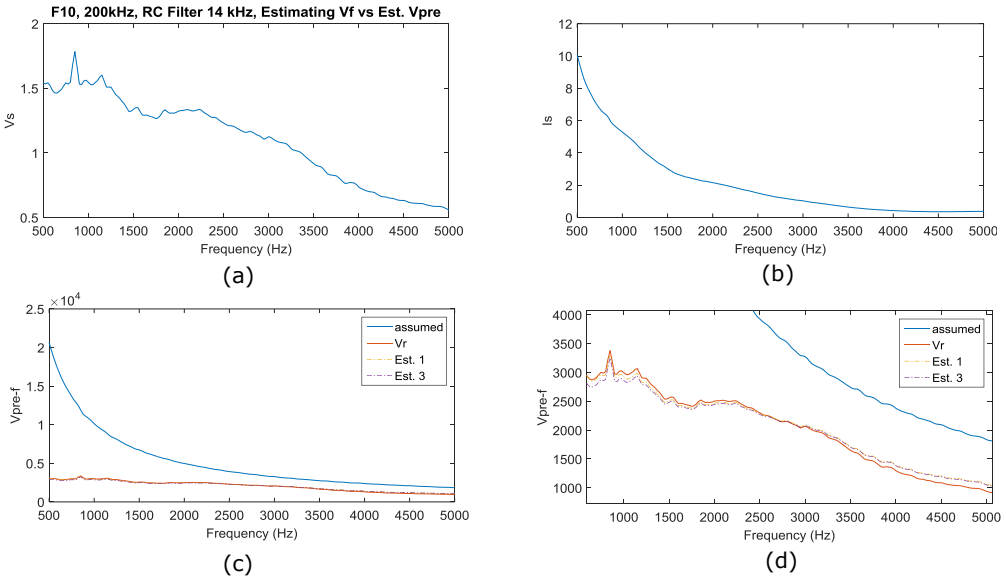


Figure 6-35 Frequency domain of the data presented in the previous figure

The estimated $V_{pre\text{-}f}$ is close to the actual measured voltage as shown in Figure 6-34 (d). The estimated $V_{pre\text{-}f}$ is used to estimate the revised fault distance which in turn is used to update the next estimate of $V_{pre\text{-}f}$ in the voltage divider equation. This iteration is repeated until the difference between two successive iterations is within the pre-set tolerance, for example ($d_{n+1} - d_n < 0.5m$). Figure 6-34(c) and (d) shows the updated $V_{pre\text{-}f}$ of the final iteration when the distance converges.

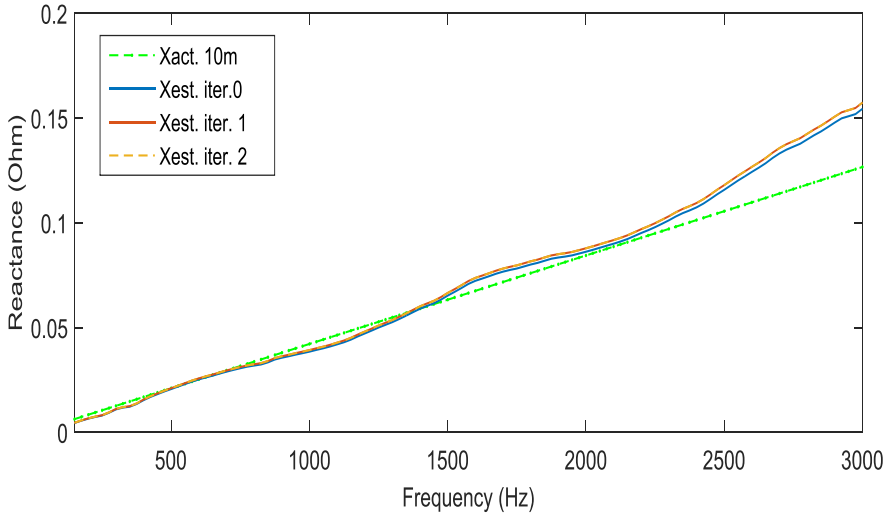
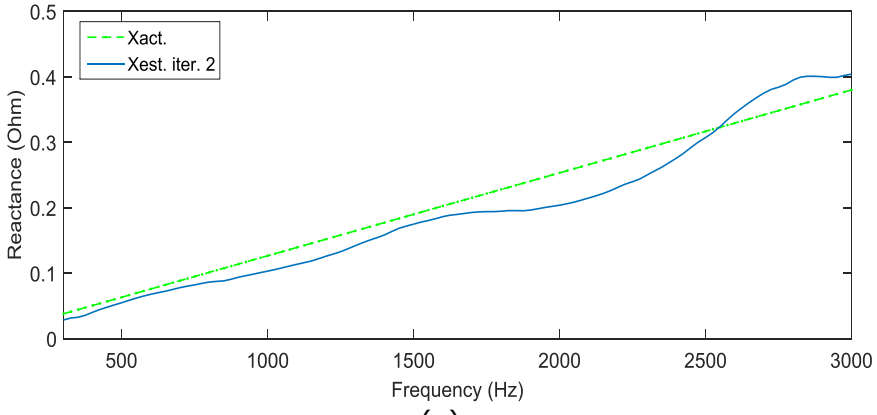


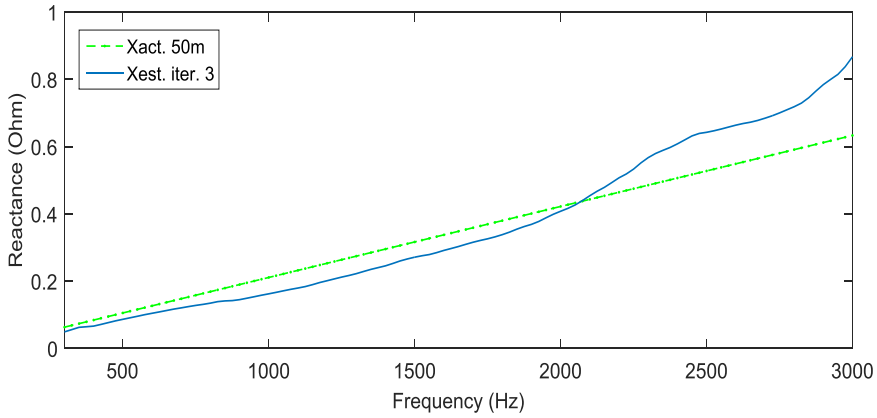
Figure 6-36 Estimated reactance for F10

The estimated reactance to the fault location is presented in Figure 6-36. The estimated reactance (orange dotted line) shows some fluctuation around the actual reactance (green dashed line) to the fault location, but it is a significant improvement over the original estimate presented in Figure 6-30(a). The estimated distance based on the average of the distance calculated from dividing the estimated reactance by the line's per-metre reactance gives a better accuracy with an error within 8%. Moreover, only 2 iterations are needed to converge to the final estimated value presented in Figure 6-36.

Using the same approach, the estimated reactances for the other possible fault locations throughout the experimental setup are summarised in Figure 6-37. The estimation for fault F30 (30m from POM1 on Tapped line 1) is shown in Figure 6-37(a). The algorithm converges to the final estimation plotted as a solid blue line in only two iterations. Although some fluctuation is presented in the estimate, the estimated distance is still within a reasonable accuracy of 10% error. Moreover, the final plot in Figure 6-37(b) shows the estimated reactance for F50 and is much improved compared to Figure 6-30(b). It is obvious that the error increases in the higher frequency range. However, the average fault distance calculated by dividing the estimated reactance by the per-metre line reactance shows an acceptable error of 8.5% based on average of error over 3kHz range.



(a)



(b)

Figure 6-37 Estimated reactance versus actual (a) F30 on Tap1 (b) F50 on Received load terminal

The aforementioned reactance estimation and fault distance calculation were performed with R_f = 1.45Ω. In the following section, the fault resistance is increased in order to investigate the SEFLT with higher fault resistances. Beginning with a fault imposed at the load terminal with fault resistance of 4.5Ω, the captured data as well as the assumed voltage at the fault location ($V_{pre\text{-}f}$) are shown in Figure 6-38. Two measured cycles of source end voltage and current are given in Figure 6-38 (a) and (b), while (c) shows the initial assumed voltage at the fault point as well as the actual and estimated one. Figure 6-38 (d) is the zoomed window of the estimated $V_{pre\text{-}f}$ plotted against the actual $V_{pre\text{-}f}$ measured from the test rig. The assumed $V_{pre\text{-}f}$ in addition to the captured source end values are transferred to the frequency domain using FFT method as presented in Figure 6-39. These three signals are used to estimate the initial value for R_f utilizing the real part of (3.7). This R_f is then used to estimate $V_{pre\text{-}f}$ applying the voltage divider rule (assuming the fault is at the midline for initial calculation).

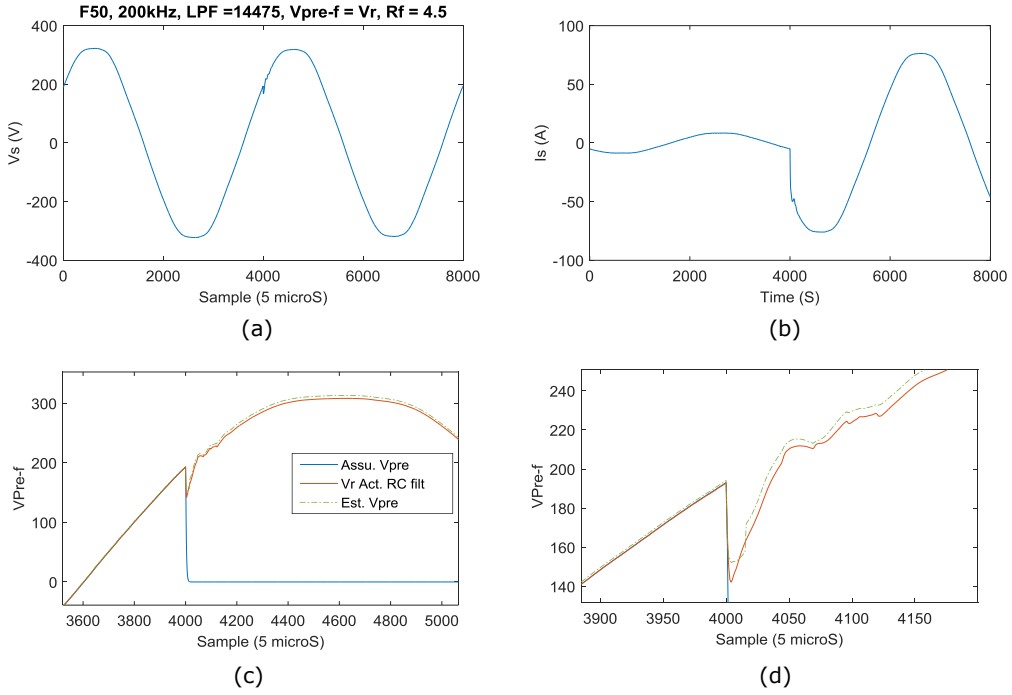


Figure 6-38 Captured and estimated signals for fault at receiving end (F50) (a) source voltage (b) source current (c) assumed and estimated fault voltage (d) Zoomed window of estimated and assumed fault voltage

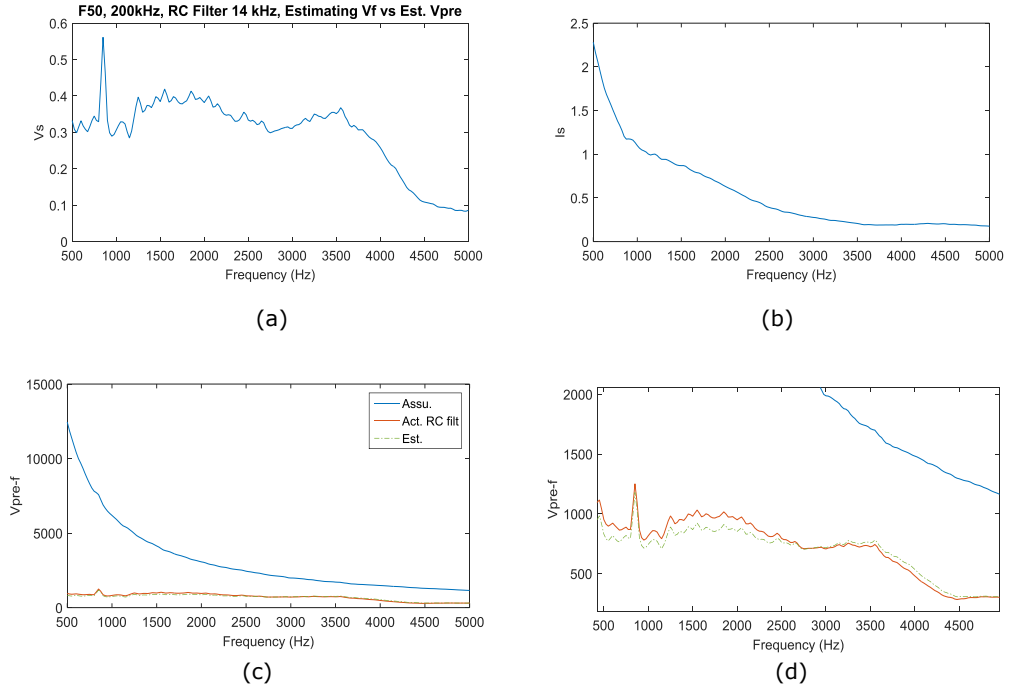


Figure 6-39 Captured, assumed and estimated data in the frequency domain for F50 (a) source voltage (b) source current (c) assumed and estimated fault voltage (d) Zoomed window of estimated and assumed fault voltage

The estimated $V_{pre\text{-}f}$ is very close to the actual measured voltage as shown in Figure 6-39(d). The estimated $V_{pre\text{-}f}$ is used to estimate the new fault distance which in turn is used to update $V_{pre\text{-}f}$ in the voltage divider equation. This iteration is repeated until the error between two successive iterations is within the pre-set tolerance.

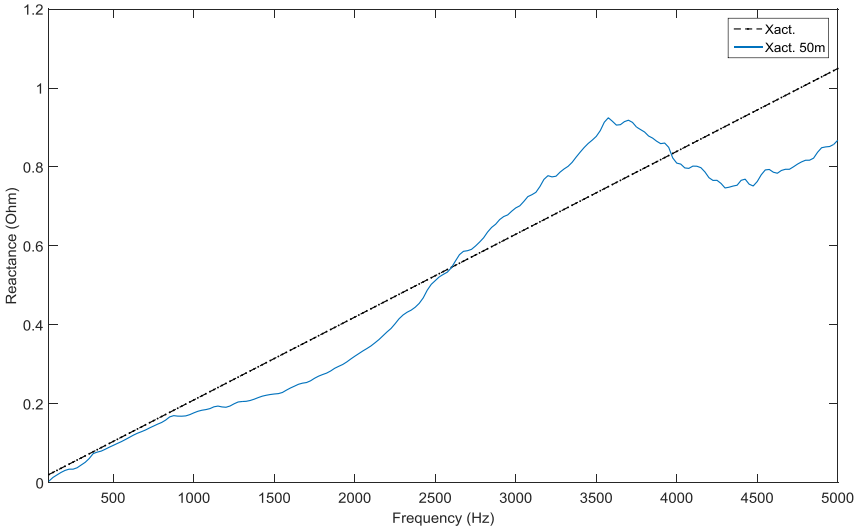
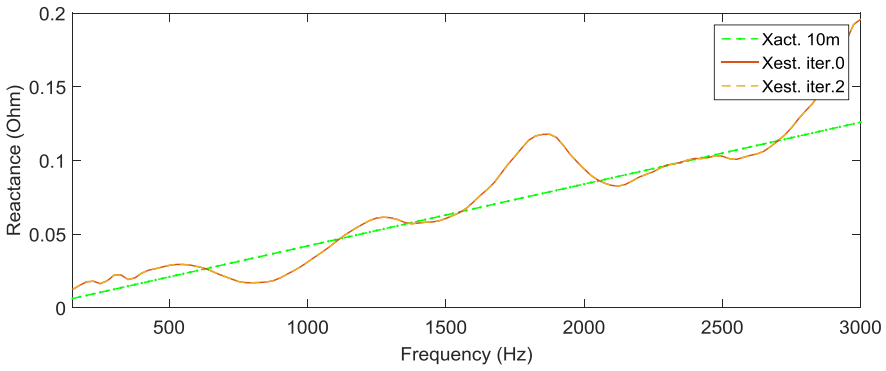


Figure 6-40 Estimated reactance versus the actual reactance to the fault location F50

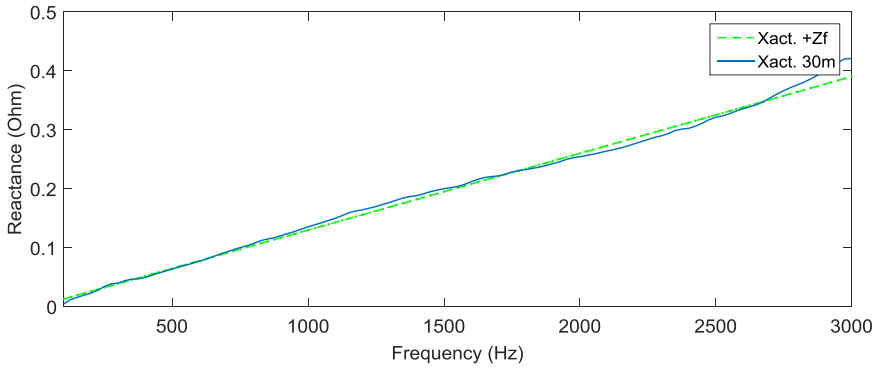
The estimated reactance to the fault location is presented in Figure 6-40. The estimated reactance (blue solid line) shows some fluctuation around the actual reactance (black dashed line) to the fault location. However, the estimated distance based on the average of the distance calculated from dividing the estimated reactance by the line's per-metre reactance gives a reliable accuracy with an error within 10%. Moreover, only 3 iterations are needed to converge to the final estimated value presented in Figure 6-40.

Using the same method, the estimated reactance for the other possible fault locations in the experimental setup are summarised in Figure 6-41. The estimation for fault F10 (10m from POM1) is shown in Figure 6-41(a). Two iterations only are needed for the algorithm to converge to the final

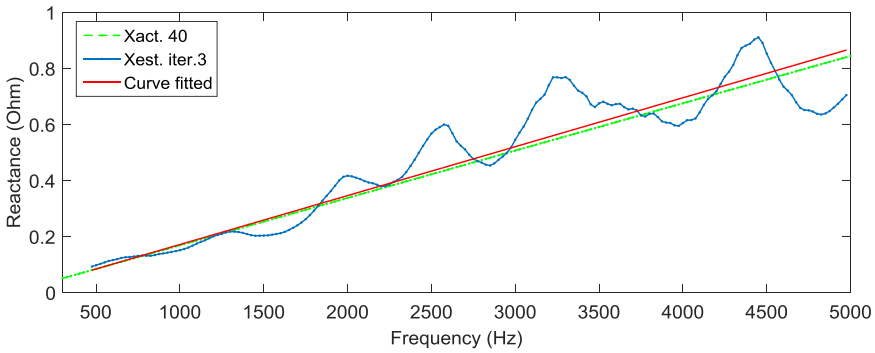
estimation given in the dashed orange line. Although some high fluctuation is seen in the estimate, the estimated distance still has a reasonable accuracy of 10% error. Moreover, Figure 6-41 (b) shows the estimation for the fault on Tapped line 1 (F30). It is obvious, the estimate is very close to the actual value with an error of 2%. The final plot in Figure 6-41 (c) shows the estimated reactance for F40. There is an obvious estimate fluctuation around the actual reactance to the fault location (green dashed line). Therefore, a linear least square curve fitting is used to fit the estimated reactance in order to compare it easier with the actual value. The curve fitted solid red line shows a high estimation accuracy compared to the actual value. The calculated percentage error is 3%.



(a)



(b)



(c)

Figure 6-41 Estimated reactance (a) F10 on main line, (b) F30 on Tap1 (c) F40 on mainline

Finally, a summary of the fault distance estimated, and the percentage error calculated are presented in Table 6-5. The table involves the calculation for fault with R_f = 1.45Ω and 4.5Ω for four possible fault locations in the experiment system. These results are very acceptable for fault location accuracy compared to the original SEFLT where the error reached more than 100%.

Table 6-5 Summary of distance estimation and error calculation

Act. Fault distance (m)	**R_f = 1.45Ω**		**R_f = 4.5Ω**	
	Est. distance (m)	**Error (%)**	**Est. distance (m)**	**Error (%)**
10	14	8.0	15	5.0
30 (on Tap1)	35	10.0	31	2.0
40	43.1	7.2	41.5	3
50	54.25	8.5	53.5	7.0

6.4.3 Factors affecting the single-ended method

The experimental investigation has shown that the estimated reactance using the single-ended method has more estimation error (up to 12% in some cases) compared to the simulated studies where the maximum error was 5%. A few reasons can explain the causes of the accuracy reduction. Firstly, the experimental measurements have more source noise which can be seen in Figure 6-42 and cause some fluctuation in the estimated results.

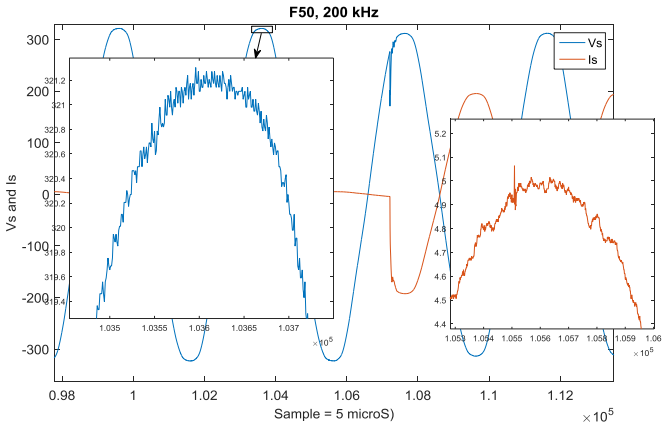
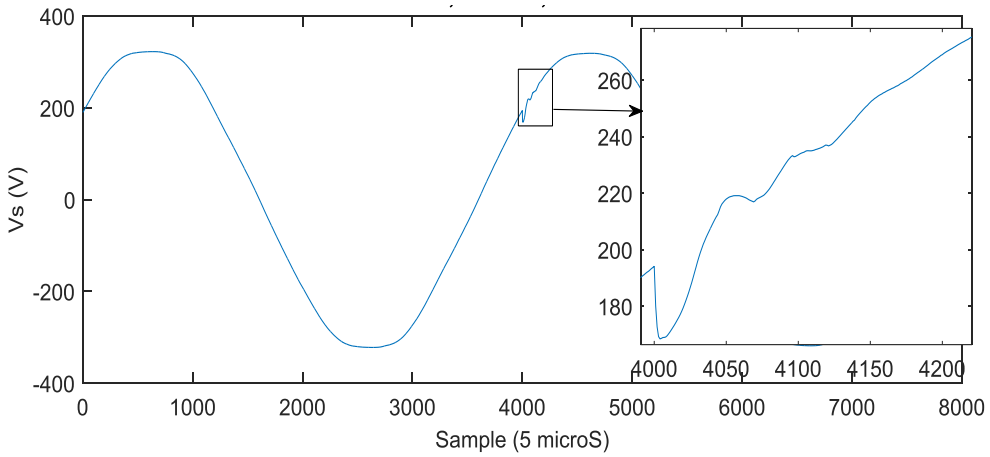
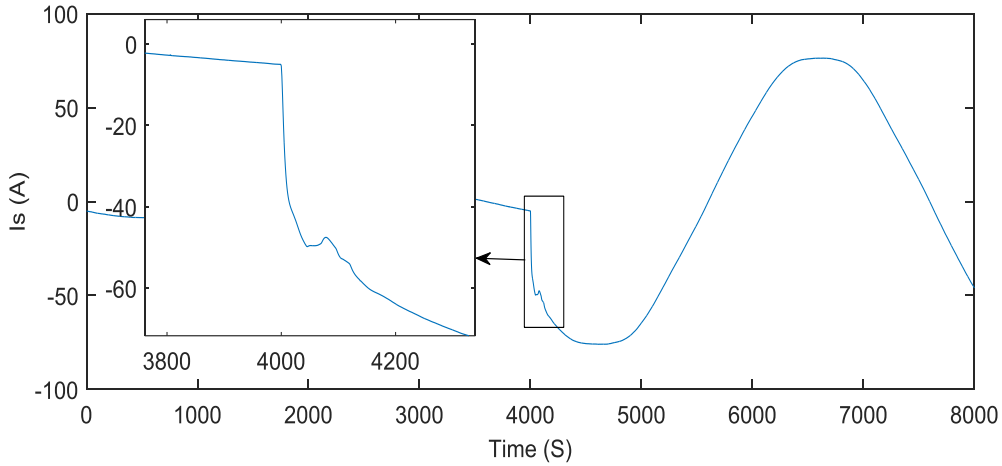


Figure 6-42 Time domain noise in the captured source end V and I

Secondly, repeated inspection and analysis of the captured signals showed that the mechanical contactor imposes some large undesirable transients after energizing the contactor coil to impose the fault due to capacitance discharge. The zoomed part of Figure 6-43 shows this contactor transient fluctuation which increases the error significantly if its characteristic has not been incorporated into the estimated fault voltage ($V_{pre\text{-}f}$) whereas the original s-ended method assumes a single sharp transient for the fault. However, this has led to the modification of the original SEFLT so that it can now be used in more realistic situations.



(a)



(b)

Figure 6-43 captured data (a) Vs (b) Is

Thirdly, the data acquisition filtering and sampling process might cause part of the error. The anti-aliasing first order low pass filter used for the measured voltage and current causes a slight error due to the tolerance of the capacitor and resistor used to form the RC filter. Figure 6-44 shows how different filter parameters change slightly the shape of the capture signal. This is important as the filters used to process the voltage and the current may have slightly different characteristics due to component tolerance, and can therefore introduce errors if they are assumed to be identical.

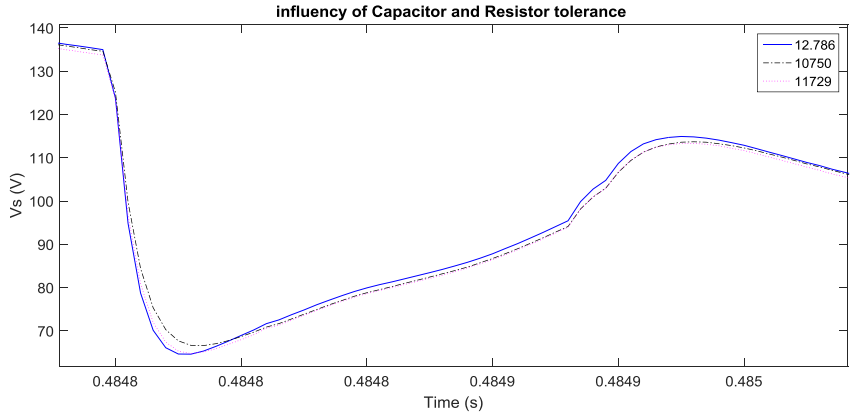
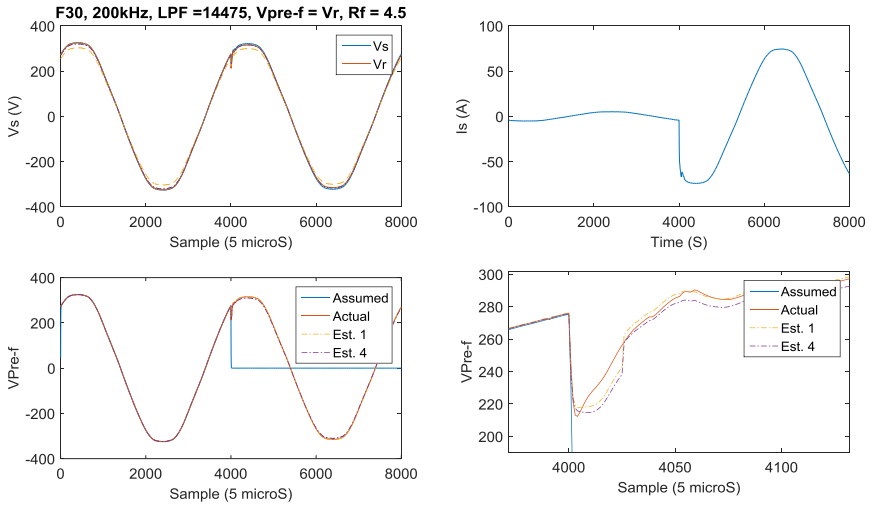
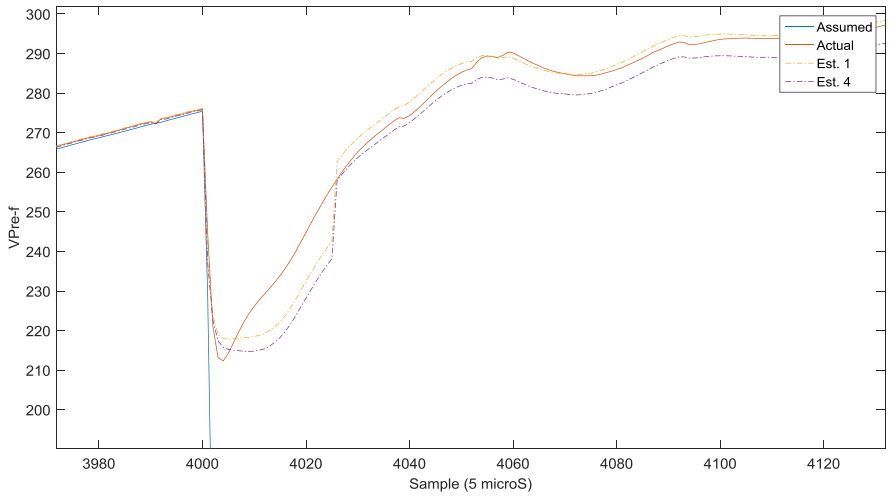


Figure 6-44 Influence of the R and C parameter tolerance on the filter cut-off frequency

Finally, the estimation of fault transient plays a vital role in the accuracy of the estimated reactance. The 20-25 μs from the moment of the fault imposition is very difficult to estimate accurately compared to the pre-fault and post-fault voltage. Therefore, any overestimation or underestimation of this 20-25μs period will lead to over or underestimated reactance as will be explained in the example below. Figure 6-45(a) shows the captured voltage and current from the source end and the assumed voltage to estimate the fault resistance.



(a)



(b)

Figure 6-45 (a) The captured source end Vs and Is, and V_{pre_f}

For fault at the end of tap1(b) The zoomed window of the estimated V_{pre_f} shows first and final iteration

Figure 6-45(b) shows a zoomed window of the estimated V_{pre_f}. This zoomed window shows the assumed voltage and the estimated voltage at the first and fourth iteration when the estimation loop converges to the final set tolerance. The frequency domain is shown in Figure 6-46. Finally, the estimated reactance is shown in Figure 6-47. The first 20μs of the transient is not correctly estimated (less than the actual transient magnitude) as shown in Figure 6-45(b), and this results in the estimated reactance being overestimated.

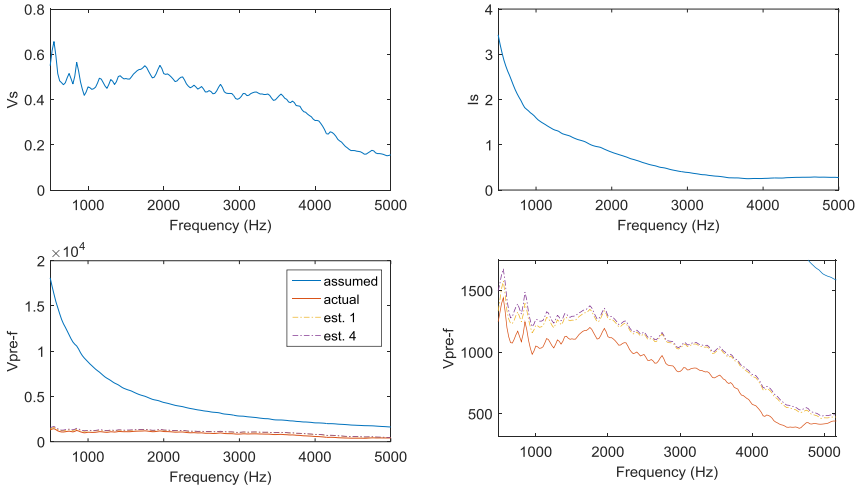


Figure 6-46 The frequency domain of Vs, Is and V_{pre_f}

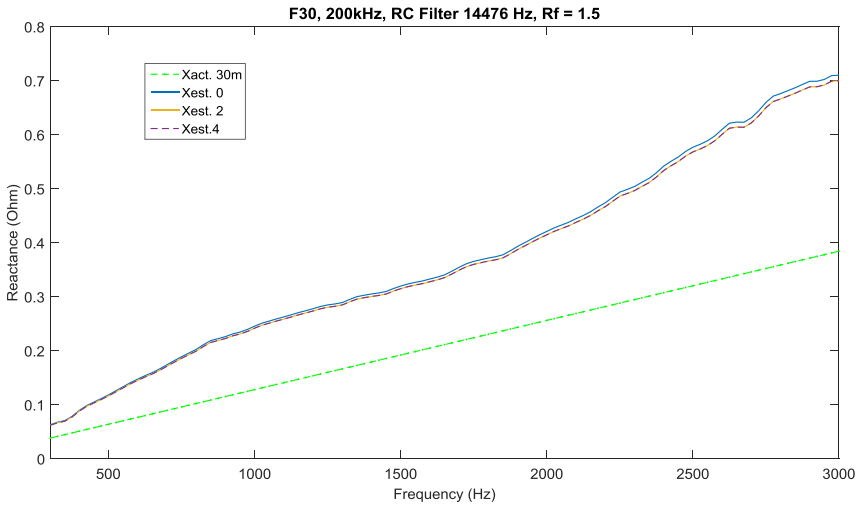


Figure 6-47 Estimated reactance versus actual reactance

6.5 Demonstration of combining DEFLT and SEFLT

The experimental validation of the combined SEFLT and d-DEFLT in order to locate the fault on the multi-tapped line will be presented in this section. A fault is imposed with R_f = 1.45Ω on the terminal of tapped line 1 (equivalent to 30m from the source) is initially used to validate the proposed technique of chapter 5.5. The modified SEFLT is used to estimate the reactance to the fault location, whereas the DEFLT is used to estimate the faulted tap. The summary of the reactance estimation is presented in Figure 6-48 and is compared to the calibrated line values. The red dashed line is the calibrated reactance to the tapping position while the blue dashed line is the calibration value to the end of the tapped line 1, i.e. the fault location. The solid lines are the estimated reactances; the blue is the SEFLT estimation which shows the distance is around the end of tapped line 1 while the purple line is the DEFLT estimation which shows the fault is around 20m. Combining the two estimates shows that the fault actually happened on the tapped line, not on the mainline. The SEFLT average calculated error over the 300-3000 Hz range is 4.2%.

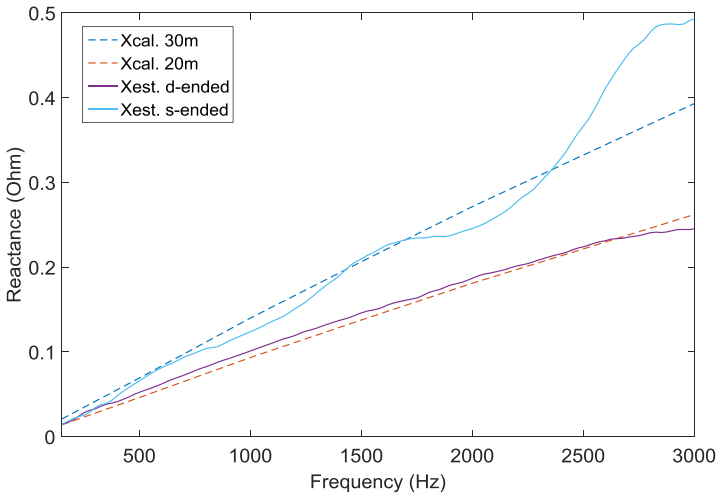


Figure 6-48 Reactance estimated using s-ended and d-ended methods for fault at Tap1 terminal

Another fault test is imposed on the terminal of tapped line 2 with the same fault resistance. The reactances estimated (solid lines) are compared to the calibrated line value (dashed lines) as shown in Figure 6-49. In the same manner, the SEFLT estimated the reactance to the fault location (solid blue line). There are two possible paths using this estimation. Therefore, the DEFLT estimated (solid red line) that the fault path is on the tapped line. The estimation error is 2.75% in the estimated distance using the SEFLT, while the DEFLT showed 2.48%.

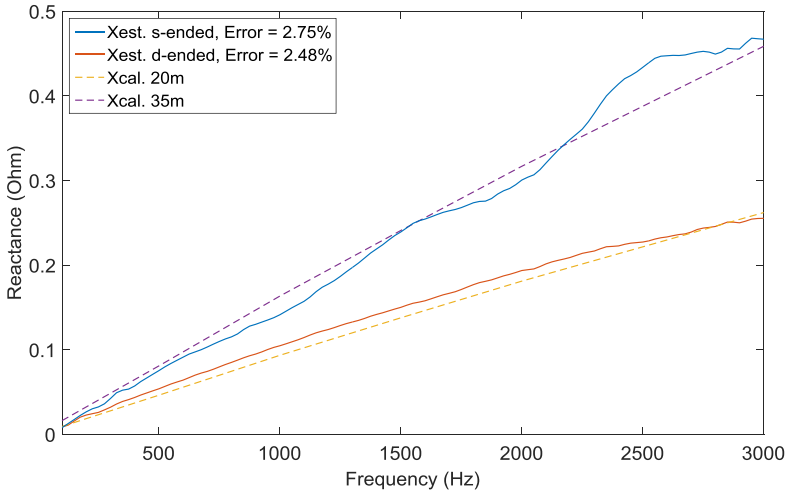


Figure 6-49 Reactance estimated using s-ended and d-ended methods for fault at Tap2 terminal (F35)

A summary of the distance and percentage error as well as the decision on the location of the fault is presented in Table 6-6 for L-N fault using Rf = 1.45Ω. The fault location decision is being made based on both the SEFLT and DEFLT estimation. If both techniques showed the close distance, i.e. the fault is on the main line. On the other hand, the fault will be on the tapped line if the estimated distance is not close as shown in row two of Table 6-6 when the fault was imposed on the end of tapped line 1.

Table 6-6 Percent error calculation for L-N faults

Actual Fault distance (m)	Estimated distance (m) using SEFLT	Error (%)	Estimated distance (m) using DEFLT	Decision on the fault location
10	14	8	9.9	On Main line
30	35	10	20.1	On Tap Line 1
40	43.1	7.2	38.75	On Main line
50	54.25	8.5	50.1	On Main line

Finally, both fault tests and the summary in Table 6-7 have identified that the combining DEFLT and SEFLT present a proper technique in order to estimate different faults on a multi-tapped distribution line using only the measurements from the two ends of the main line.

6.6 The influence of DG on the fault location methods

The influence of the inverter-based DG on the DEFLT and the SEFLT will be experimentally demonstrated in this section. A GenDrive (bidirectional power converter) [92] is utilised in order to represent an inverter-based DG. The Gendrive is an AC/DC/AC converter with a basic structure shown in Figure 6-50. This Gendrive converts the supply side AC power to DC and then back to a controlled AC power. The Gendrive is connected 20m from supply end (POM1) of the experimental rig as shown in Figure 6-51. The connection point is equivalent to the point where the two tapped lines are connected. The Gendrive is controlled using LABVIEW software. The Gendrive is supplied from the main grid Bus 1 and it puts power onto the experimental grid (Bus 2). The technical data of the GenDrive TW3-10 is presented in Table 6-7.

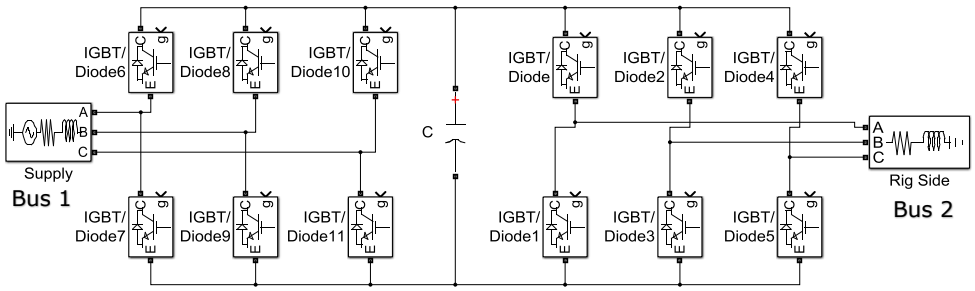


Figure 6-50 Basic structure of an AC/DC/AC converter

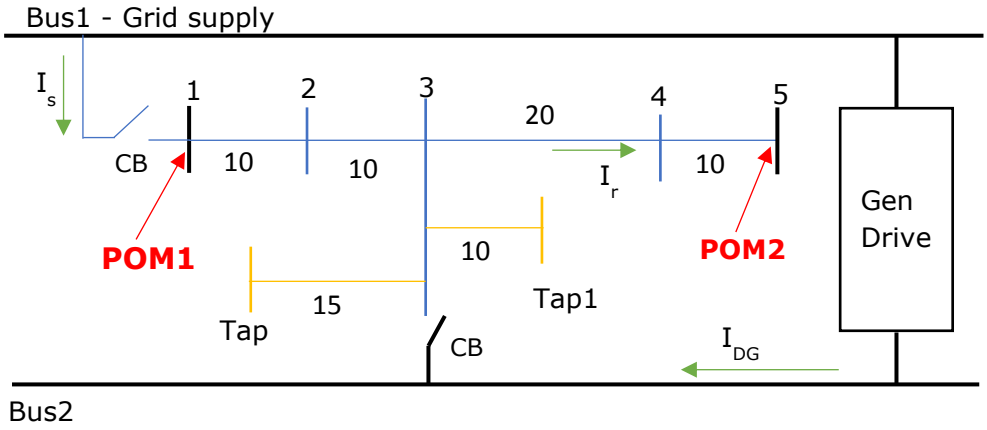


Figure 6-51 Fault rig schematic diagram with GenDrive connection

Table 6-7 Technical Data of GenDrive TW3-10

Output (AC)	
Rated power	12 kW @ 415 V
Line voltage	380 – 480 V
Phase current	16 A
Max power factor (cosφ)	1.0
Frequency	50Hz
Grid connection	3-phase
Input (AC)	
Max voltage (rms)	560 V
Max phase current (rms)	21 A
Max frequency	300 Hz
Min turbine cut-in voltage (rms)	50 V
Generator power factor	Optimised for lowest losses

6.6.1 DG influence on the DEFLT

The DG effects on the DEFLT will be explored in this section. The system uses a L-N fault with R_f = 4.5Ω and has a load set at 37Ω. The supplied power by the DG is varied between 1kW - 3kW in order to investigate the influence of the effect of the magnitude of the DG power. The data measurements, filtering, and processing are similar to those used in previous sections. The first fault test is imposed 10m from the sending end. The reactances estimated (solid blue lines) for two DG power are presented in Figure 6-52. It is obvious there is a small influence from the supplied DG rating on the accuracy of the estimated reactance using the measurements from the sending end and receiving end of the main cable. Note that there is a high divergence between the estimation and the actual reactance (green dashed lines) at a frequency range higher than 2500 Hz. The SNR of the measurement is lower in this frequency range. Comparing this estimate to Figure 6-14 for the case in the DG shows there is only large error caused by the DG at frequencies higher than 2.5 kHz.

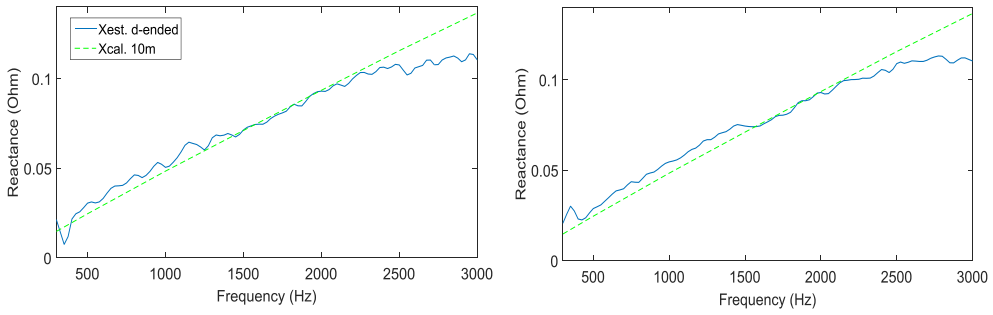
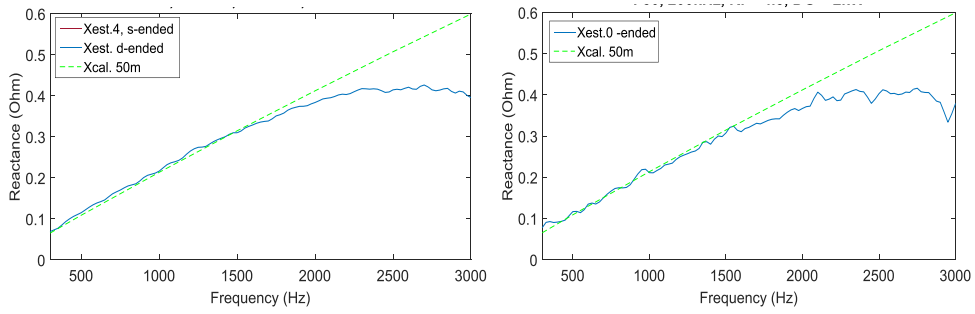


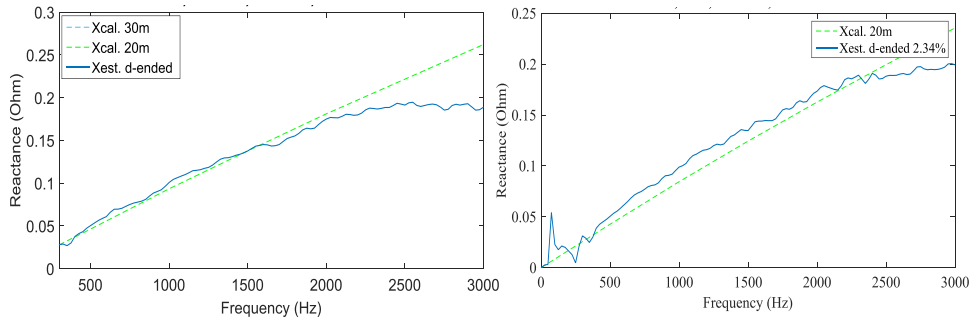
Figure 6-52 Reactance estimated using d-ended method with the presence of the DG (a) DG = 1kW (b) DG = 2kW

Another fault test is imposed on the receiving end terminal, with the same system conditions. The reactances are estimated (solid blue lines) with three different power levels and compared to the actual reactances and are in Figure 6-53. Once more, the estimation shows a close match with the calibrated cable reactance in the frequency range less than 2500Hz and the estimation diverges in the higher frequency range. The final test is performed for a fault on the tapping line, 20m from sending end. Similarly, the estimated reactance (blue solid line) plotted against the calibrated reactance (green dashed line) are shown in Figure 6-54. Initial observation shows a similar behaviour where the estimation diverges after 2500Hz. However, the lower range presents a high estimation accuracy, which is utilized to estimate the final fault distance by comparing it to the per-metre calibrated reactance.



(a) (b)

Figure 6-53 Reactance estimated using d-ended method with the presence of the DG for fault 50m from s-end (a) DG = 1kW (b) DG = 2kW



(a) (b)

Figure 6-54 Reactance estimated using d-ended method with the presence of the DG for fault 20m from s-end (a) DG = 1kW (b) DG = 2kW

A summary of the estimated fault distance for the three DG supplied power levels and different fault conditions are presented in Table 6-8, Table 6-9 and Table 6-10. Table 6-8 and Table 6-9 are for Line-Neutral (L-N) faults using two fault resistances 1.45 Ω and 4.5 Ω respectively. The third Table is for a Line-Line fault using R_f = 4.5Ω to keep the fault current within the transducer rating. The majority of the estimation error is lower than 6% of the total cable length. The power supply from the DG increased from 1kW to 3kW, and was found to have caused a limited effect on the estimated distance. This is because the 3kW will supply a steady power for 67% of the system loads while during the fault the increased current is supplied from the primary source. Furthermore, the GenDrive control loop limits the supplied current during any abnormal state to the rated value in order to protect the electronic components.

Table 6-8 L-N faults with R_f = 1.45Ω and three DG ratings and without DG

Act. Dist. (m)	**GenDrive = 0kW**		**GenDrive = 1kW**		**GenDrive = 2kW**		**GenDrive =3kW**	
	Est. dist. (m)	Error (%)	Est. dist. (m)	Error (%)	Est. dist. (m)	Error (%)	Est. dist. (m)	Erro r (%)
10	9.36	-1.28	13.0	5.96	12.9	5.86	15.25	10.5
20	20.3	0.6	22.33	4.65	22.95	5.95	22.17	4.34
40	38.75	-2.5	40.16	3.25	42.12	4.25	38.5	-1.5
50	50.1	0.2	48.88	-2.23	48.85	-2.3	48.93	-2.1

Table 6-9 L-N faults with R_f = 4.5Ω and three DG ratings and without DG

Act. Dist. (m)	**GenDrive = 0kW**		**GenDrive = 1kW**		**GenDrive = 2kW**		**GenDrive = 3kW**	
	Est. dist. (m)	Error (%)	Est. dist. (m)	Error (%)	Est. dist. (m)	Error (%)	Est. dist. (m)	Error (%)
10	9	-2.0	12.24	4.48	11.86	3.92	12.43	4.86
20	19.23	-1.5	22.6	5.2	21.17	2.34	23.3	6.6
40	38.0	-4.0	38.36	-3.33	38.92	-3.1	38.85	-2.3
50	48.05	-3.9	48.86	-3.07	47.46	-5.7	48.36	-3.2

Table 6-10 L-L faults with R_f = 4.5Ω and three DG ratings

Act. Dist. (m)	GenDrive = 1kW		GenDrive = 2kW		GenDrive = 3kW	
	Est. dist. (m)	Error (%)	Est. dist. (m)	Error (%)	Est. dist. (m)	Error (%)
10	12.75	5.74	13.6	7.15	12.5	5.01
20	22.7	5.33	22.6	5.2	22.6	5.2
40	38.5	-3.0	38.9	-2.22	38.82	-2.3
50	47.17	-5.7	48.67	-2.67	48.05	-3.9

The reactance at frequencies higher than 2.5kHz in most of the cases presented above starts to diverge significantly from the calibrated reactance. Therefore, the supplied current by the DG has been captured, converted to frequency domain, and then compared to the source end current. The frequency analysis of the supplied DG current showed that the DG current to the fault current increased with frequency as shown in Figure 6-55 for two the fault tests and if this ignored, it will cause error. This pattern is repeated with most of the analysed supplied current by the DG (GenDrive). The DG current becomes close or larger than the main source current at frequencies higher than 2.5kHz which causes the estimated reactance to diverge.

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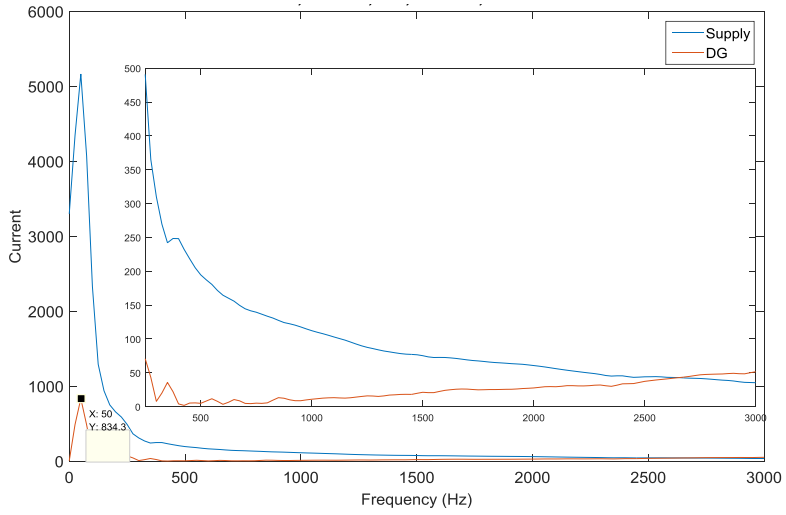
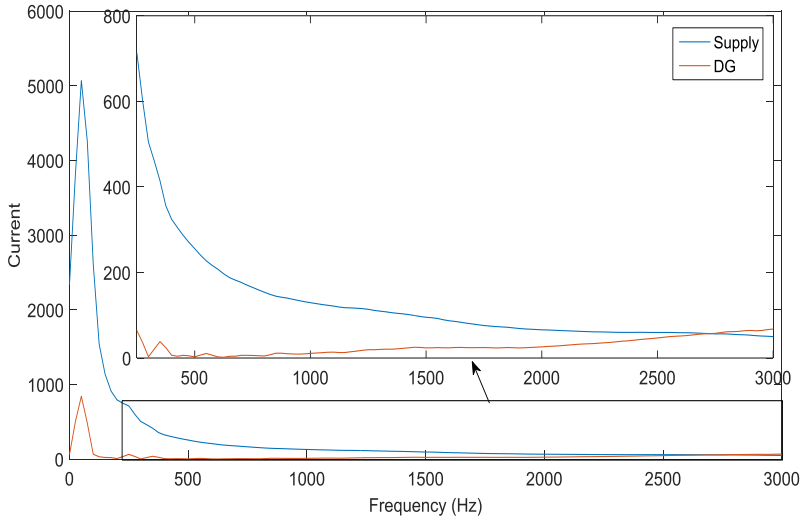


(a)

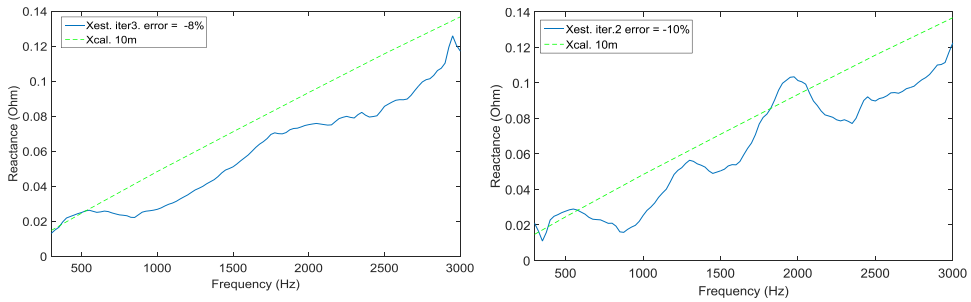


(b)

Figure 6-55 Comparison of supply to DG current at frequency domain (a) L-L fault at 50m (b) L-L fault at 10m

6.6.2 The influence of the DG on the SEFLT

The investigation of the impact of the inverter based DG on the s-ended fault location method will be carried out in this subsection. Similar fault scenarios to the previous section are used in order to identify the influence of the inverter-based DG on the accuracy of the s-ended fault location method. Initially, a L-N fault is imposed separately at three different fault locations throughout the rig, with Rf = 4.5Ω and various supplied power from the DG (GenDrive).



(a) (b)

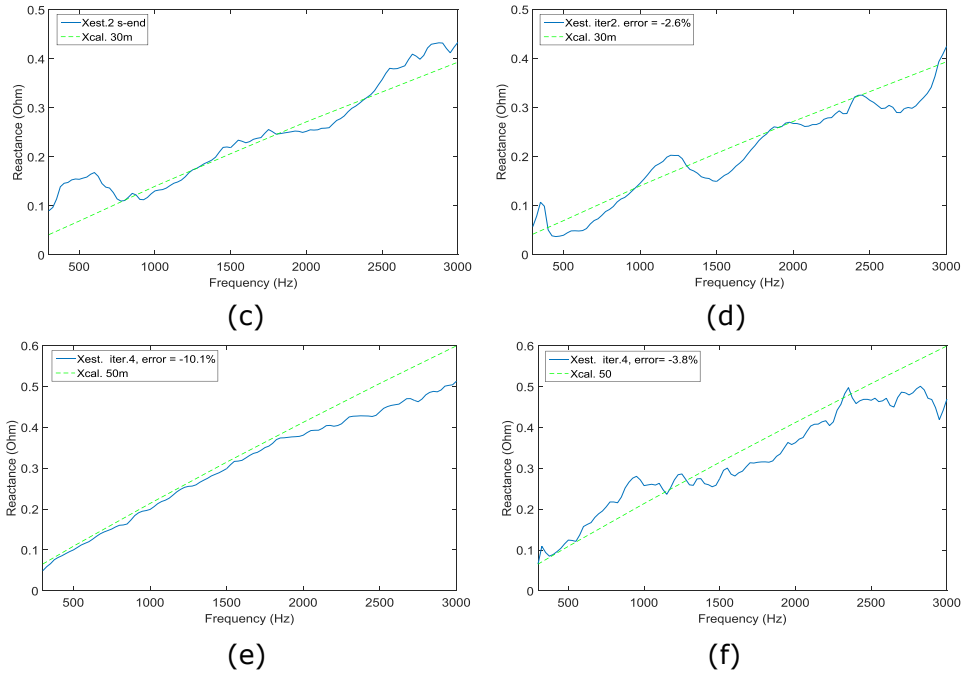


Figure 6-56 Reactance estimated using SEFLT (a) F10 with DG=1kW, (b) F10 with DG =2kW, (c) F30 (tap1) with DG=1kW, (d) F30 (tap1) with DG=2kW, (e) F50with DG=1kW (f) F50with DG=2kW

A summary of the reactances estimated is presented in Figure 6-56, with the estimated distance and computed percentage error given in Table 6-11. Figure 6-56 (a and b) is the reactance estimated for a fault 10m away from s-end. It took less than three iterations to converge to the final estimated reactance given in dashed purple line for the DG supplying 1kW and the solid blue line for the DG supplying 2kW. In the same Figure, graph (c and d) show results for a fault 30m from sending end on the end of tapped line 1 whereas (e and f) are for s fault 50m from sending end on the receiving end. The observation of the graphs shows there is a slight influence imposed by the supplied DG power level. In most of the cases, there is also a bigger effect at frequencies higher than 2.5kHz. The distance estimation and the resultant percentage error from the final iteration are summarised in Table 6-11. It is important to mention that the percentage error for each location is an average of three or four fault tests at the same location with different fault inception angles. Nevertheless, the calculated accuracy in this table

shows that the majority of the estimation error is less than 6% except for three fault tests; in total, the error is 10% or less. Close observation shows that the DG slightly influences the SEFLT even when the DG supplied 67% of the steady-state load. Moreover, there is a limited error change with successive increases in the magnitude of the supplied power by the DG from 1kW to 3kW. As has been mentioned, the DG control loop controls the DG supplied current during the fault, and it limits the fault transient in order to protect the electronic components. Similarly, the frequency analysis of the supplied DG current showed that the DG current to the fault current increased with frequency as shown in Figure 6-55 and if this ignored, it will cause error. The DG current becomes close or larger than the main source current at frequencies higher than 2.5kHz which causes the estimated reactance to diverge.

Table 6-11 Estimated distance and percentage error for L-N fault, with R_f = 4.5Ω and three DG supply ratings

Act. Dist. (m)	**GenDrive = 1kW**		**GenDrive = 2kW**		**GenDrive = 3kW**	
	Est. dist. (m)	Error (%)	Est. dist. (m)	Error (%)	Est. dist. (m)	Error (%)
10	6	-8	-5	-10	-7.75	-5.7
30	32.5	5.0	28.7	-2.6	32.5	5.0
40	38.28	-3.44	38.1	-3.84	40.95	1.95
50	45.0	-10.1	48.1	-3.8	47.55	4.9

Another L-N fault test with same DG scenario but with lower fault resistance (R_f = 1.45Ω) was performed. The distance estimation and the percentage error is summarised in Table 6-12. The results presented show the same behaviour with a maximum error of less than 10%. A final test was performed with a L-L fault, with R_f = 4.5Ω. The summary of the calculated distance and percentage error is presented in Table 6-13. Once more, the DG shows a limited impact on the estimated distance accuracy, with maximum error of 12%. The analysis in Section 6.4 has shown that the

influence of DG on the SEFLT is low, and the accuracy in the presence of DG is comparable to that without DG as presented in Table 6-5.

Table 6-12 Estimated distance and percentage error for L-N fault, with R_f = 1.45Ω and two DG supply ratings

Act. Dist. (m)	**GenDrive = 0kW**		**GenDrive = 2kW**		**GenDrive = 3kW**	
	Est. dist. (m)	Error (%)	Est. dist. (m)	Error (%)	Est. dist. (m)	Error (%)
10	14	8.0	6	8.0	4.75	10.56
30	35	10.0	31.95	3.91	35	9.54
35			37.22	4.45	33.1	-3.83
40	43.1	7.2	35	-10.0	36.75	-6.5
50	54.25	8.5	43.75	-12.5	44.75	-10.5

Table 6-13 Estimated distance and percentage error for L-L fault, with Rf = 4.5Ω and three DG supply ratings

Act. Dist. (m)	**GenDrive = 1kW**		**GenDrive = 2kW**		**GenDrive = 3kW**	
	Est. dist. (m)	Error (%)	Est. dist. (m)	Error (%)	Est. dist. (m)	Error (%)
10	14.7	9.4	15.25	10.5	15.35	10.7
30	35.8	11.6	36.15	12.33	34.55	9.1
35	38.37	6.75	39.75	9.5	39.4	7.85
40	36.7	-6.6	37.4	-5.22	38.1	-3.73
50	45.5	-11	48	-4.0	36.55	-6.89

Together, these results provide a valuable insight into the application of DG in IPS/Microgrid and its effect on fault location. These results suggested a limited influence from the inverter-based DG on the accuracy of the proposed SEFLT when the supplied DG current is not included in the estimation algorithm. Therefore, the inverter-based current contribution can be neglected especially when it is difficult access to its measurements.

6.7 Summary

The DEFLT that utilises the fault generated transient has been experimentally investigated in this chapter. The experiment outcomes demonstrated a high accuracy of the d-ended fault location technique. Moreover, it also validated the inability of the technique to locate the faults on tapped lines. However, it demonstrated the ability to locate the faulted tapped line in order to be disconnected. Furthermore, the results showed that tapped loads have a small negative effect on the estimated reactance and consequently, the estimated fault distance. The magnitude of this error is less than 5% when the tapped-load is four times bigger than the receiving end load. However, a double-ended with compensation technique was developed showed promising results, and the error was reduced by 4% without any extra measurement from the tapped load. The tapped load current is estimated from the source end current using the current divider rule.

The approximated DEFLT using only the source end voltage and current as well as the receiving end voltage has been tested. The results showed an excellent estimation accuracy and a very close match to the original DEFLT that also includes the receiving end current. The error only increased by less than 1%. Therefore, this approach represents good value in economic terms due to the reduction in the required measurements.

In the second part of this chapter, the experimental demonstration of the SEFLT is discussed. The experimental results showed that the SEFLT implemented on the simulated results is not realistic as in the experimental system the fault is not imposed as an ideal step change. Therefore, a

solution was developed in order to overcome this issue by estimating the voltage at the fault location during the fault in order to incorporate the influence or true fault transient into the voltage at the fault location. This amended methodology significantly reduced the error caused by the contactor. However, it was found there is some inconsistency in the estimated reactance due to one main factor, which is the first 25μs of the estimated voltage after the fault is imposed. This showed inaccuracy in the estimation (maximum error could exceed 25%), which caused the inconsistency in the estimated reactance to the fault location.

In the third part, the combined SEFLT and DEFLT is investigated. The experimental results demonstrated the theory of using the SEFLT to estimate the distance to the fault whilst the DEFLT is used to discriminate between the possible fault location (i.e. either the fault on the tapped line or on the main line)

Finally, the investigation of the impact of inverter-based DG on the DEFLT and SEFLT was performed. A GenDrive was used to represent the DG, and was connected to the main cable, 20m from the source end, which is the location of the two tapped lines. Both methods were tested with different supplied power levels as well as two fault resistances (1.45Ω and 4.5Ω) and with L-N and L-L faults. The tests demonstrated a small influence from the DG on both methods considering the DG supplied 67% of the system load. The majority of the calculated error for the d-ended method was less than 6% of the total cable length except for a few cases in which the error reached 10%. On the other hand, the SEFLT presented a lower accuracy with the majority of the error less than 9% (with some reaching 12%). There is a

small difference between the estimation accuracy with the DG in the system and the results without the DG in the system. This demonstrates a limited influence from the DG supply at non-fundamental frequencies as the current control loop limits the supplied current during the fault condition in order to protect the electronic equipment in the inverter.

Chapter 7 - Conclusion and Future Work

7.1 INTRODUCTION

In this work, a comprehensive investigation of impedance-based fault location techniques based on estimation at frequencies higher than the fundamental frequency is performed. Therefore, the conclusions resulting from the work will be presented along with the future recommendations.

The work presented aimed to examine thoroughly the application of impedance-based fault location methods (SEFLT and DEFLT), based on the generated fault transients, on a realistic and more complex IPS/Microgrid utilising a minimum number of measurements. Previously, the techniques had only been evaluated through simulation. Therefore, an experimental IPS/Microgrid has been set up, similar to those in marine vessels. The system is composed of 50m of main cable subdivided into four sections. Two tapped lines are connected to the end of the second section. The investigations are divided into fault location using measurement at two ends; fault location using measurement at only one end. The following conclusions have been made:

7.1.1 Conclusions for the DEFLT

The DEFLT was investigated using a simulation approach, with experimental validation. Both approaches showed that the DEFLT is a reliable method to find different fault locations under different fault types (hard step transient and bouncing transient) with different fault impedances, different tapped loads and receiving end loads. The simulation showed a high accuracy except when the source end impedance is high enough and comparable with the receiving load (the ratio of Z_s/Z_r is higher than 30%) or the tapped load is

four times or more higher than the receiving end load with high source impedance. A compensative DEFLT is proposed to overcome this issue, and the method offered a proper compensation under different conditions. One limitation is encountered which is the DEFLT is not capable of locating faults on tapped lines, although it has the ability to locate the faulted tapped line in order to disconnect it or locate the fault using another method.

Further investigation of the accuracy of the DEFLT under the presence of inverter-based DG is performed. The simulation which is validated by the experimental results showed a minimal influence on the accuracy of the estimated fault distance (error within 4m for 50m cable length) when the DG supplied 67% of the system load. The simulation of a larger scale IPS/Microgrid showed a similar accuracy.

7.1.2 Conclusions for the SEFLT

The investigation of the SEFLT is performed in the second part of this work in order to overcome some limitations and reduce the required measurements to only one end. An iterative approach is used by assuming a step fault voltage transient during the fault situation in order to minimise the error between the assumed voltage at the fault location and the actual voltage at the fault location. The simulations show very good results with an error around 3m for the system cable. However, the experiment work showed that the technique has a very low accuracy. This is because the actual fault is different from an ideal step change, especially when created by a bouncing contactor. Therefore, a method was proposed to address this issue by better estimating the fault voltage from an itrative circuit analysis. This approach enhanced the accuracy and minimised the error potentially to

within 12% of the total cable length compared to at least 60% using the assumed hard step transient. The algorithm process usually takes only a few iterations to converge to the final result within 20ms after the fault occurs. The method is potentially affected by tapped loads (comparable to the receiving load) between the POM and the fault location. Thus, a SEFLT with tapped load compensation was proposed. The simulation showed good results with error within 4m of the system cable.

In a similar approach to the DEFLT, the influence of the inverter-based DG on the SEFLT was investigated. An inverter-based DG was simulated and moved to different positions within the system, with different power levels for a comprehensive study. The simulation results showed a minimal adverse impact on the accuracy of the investigated technique. The accuracy is only affected by a maximum of 3% when the DG supplies 50% of the system load. This has been validated by the experimental outcomes for smaller rating system.

7.1.3 Contribution to knowledge

This section summarises the contributions had been made in this work.

1. Proposing a new DEFLT with tapped load compensation as validated in chapter 4.5 and 6.3.5.
2. Proposing an enhancement to the DEFLT using only three measurements and ignoring the receiving end current as demonstrated in chapter 4.4 and chapter 6.3.3.
3. Proposing a new modification to the SEFLT to address the issue of estimation error caused by a non pure fault transient (i.e. fault step contains some bounce or ripple) as demonstrated in chapter 6.4.2.

4. Proposing a new combined method of SEFLT and DEFLT in order to locate faults on a multi tapped system using only measurements from two ends, which is validated in chapter 5.5 and chapter 6.5.
5. Proposing a modified SEFLT with tapped and receiving end load compensation when Rf is Large, section 5.3
6. Proposing a SEFLT with approximate of multiple tapped loads compensation which achieves a simple solution to the exact technique when the number of tapped load are more than four, as presented in seciton 5.2.2.
7. Investigating the influence of the inverter-based DG on the DEFLT as validated in chapter 4.6 and chapter 6.6.1.
8. Describing the inlfuence of the inverter-based DG on the SEFLT as verified in chapter 6.6.2.

7.2 Future Recommendations

The investigated and proposed single-ended and double-ended techniques were demonstrated using a computer simulation as well as an experimental test on a low voltage tapped IPS. The methods now need to be further investigated using a bigger system.

7.2.1 Further suggested investigation

Further investigation that focuses on the application of the studied impedance-based fault location techniques in larger scale system such as a real distribution system with a higher voltage level and distributed line parameters. Moreover, large-scale systems have the effect of the line capacitance, which is important to investigate its effect on the proposed methods. A system that also has power electronic loads in order to

investigate the effect of the electronic switching noise on the accuracy of the techniques should be examined.

7.2.2 Impact of a synchronous Generator

Many IPS and distribution systems have a standby synchronous generator in order to be used either in emergency conditions or under overload conditions. Therefore, the influence of a second synchronous supply on the proposed fault location technique is required. A large supplied power and fault transient under abnormal conditions from the synchronous generator can be achieved because of the generator large moment of the inertia as compared to power electronic based resources such as PV and wind. A few studies have found that a second synchronous supply can has a big adverse impact on the traditional impedance based fault location technique [65, 57, 64, 60, 63, 93, 94, 95]. Thus, investigating the impact of the current contribution from the synchronous DG on the proposed technique is required.

8.1 References

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APPENDIX A - IDEAL DG

The circled zone shows the difference with the realistic DG model presented in Figure 4-20. The Ideal DG utilises an ideal control voltage source (in the red circle) while the real DG use inverter-based components (DC supply and electronic Switches)

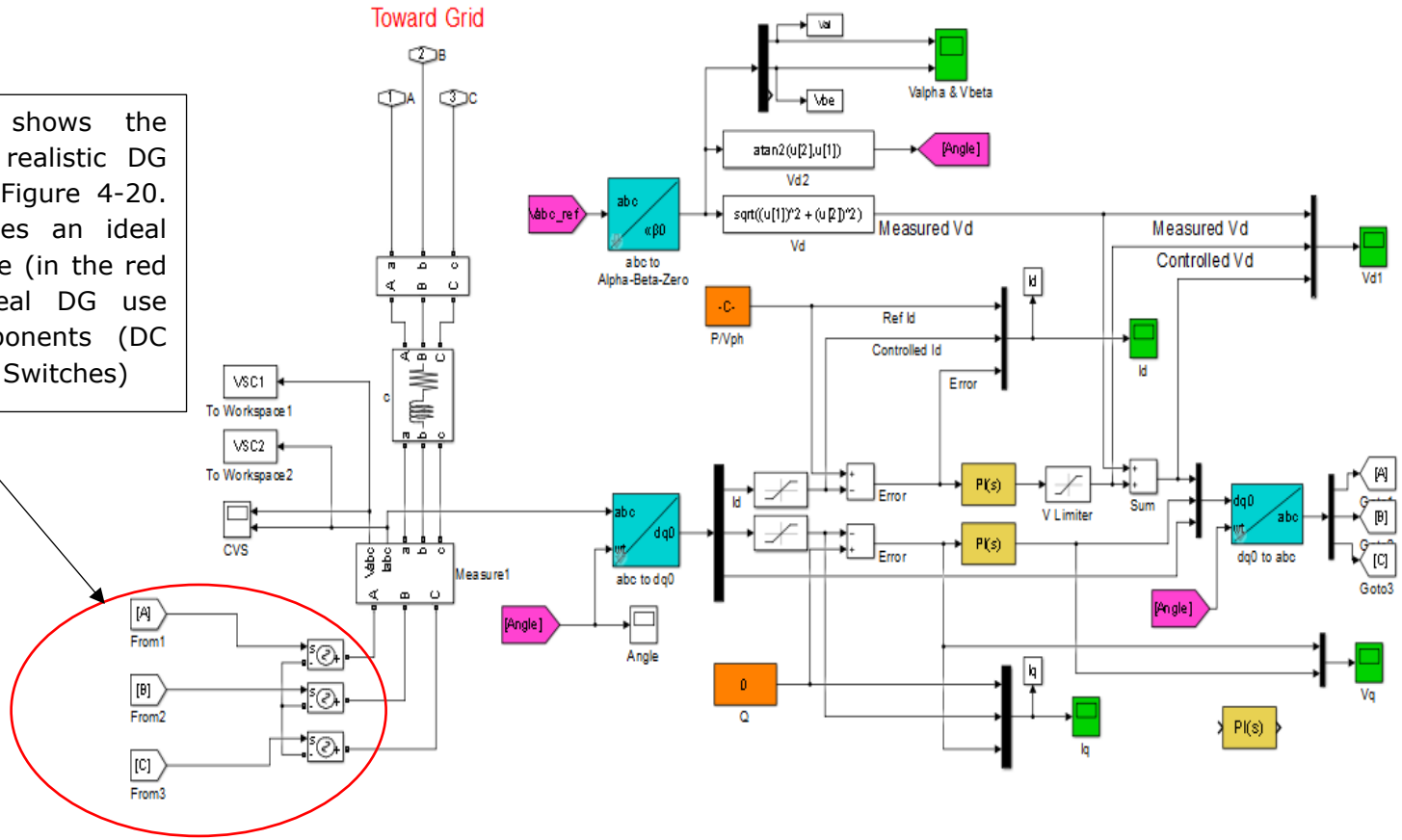

Figure A-1 Ideal DG Model