

A Sub $k_B T/q$ Semimetal Nanowire Field Effect Transistor

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The key challenges for nanoelectronics technologies is to identify designs that work on molecular length scales, provide reduced power consumption relative to classical field effect transistors (FETs), and that can be readily integrated at low cost. To this end, a FET is introduced that relies on quantum effects arising for semimetals patterned with critical dimensions below 5 nm, that intrinsically has lower power requirements due to its better than a ‘Boltzmann tyranny’ limited subthreshold swing (SS) relative to classical field effect devices, eliminates the need to form heterojunctions, and mitigates against the requirement for abrupt doping profiles in the formation of nanowire tunnel FETs. This is achieved through using a nanowire comprised of a single semimetal material while providing the equivalent of a heterojunction structure based on shape engineering to avail of the quantum confinement induced semimetal-to-semiconductor transition. *Ab initio* calculations combined with a non-equilibrium Green’s function formalism for charge transport reveals tunneling behavior in the OFF state and a resonant conduction mechanism for the ON state. A common limitation to TFET designs is related to a low current in the ON state. A discussion relating the semimetal FET (SM-TFET) design to overcoming this limitation while providing less than 60 meV/dec SS at room temperature is provided.

Increasing manufacturing costs and a lessening cadence for improved performance with new technology nodes is leading to a critical point in the manufacture of advanced nanoelectronics¹. For some time, device scaling has failed to provide increased switching speeds for transistors leading to circuit architectures that rely on increasing the level of parallel processing rather than increasing the amount of processing achievable by a single processor. As transistors are manufactured with 10 nm and 7 nm critical dimensions, source-drain tunneling makes it increasingly difficult to turn devices OFF resulting in higher power considerations for modern circuits manufactured with billions of transistors. Just as increased gate tunneling lead to the introduction of ‘high κ ’ dielectrics, continued scaling is leading to the introduction of multi-gate transistor architectures and a search for devices that can overcome the ‘Boltzmann tyranny’ that is inherent in classical field effect transistor (FET) operation.

The subthreshold swing (SS) is a measure of the electrostatic gate control over the drain-source current (I_{DS}) in a metal-oxide-semiconductor FET (MOSFET). The gate is used to lower the electrostatic barrier between drain and source, the amount of charge carriers able to surmount this barrier is related to the Fermi-Dirac distribution in the source region which for normal operating temperatures can be approximated as a Maxwell-Boltzmann distribution. For fixed temperature, the current I_{DS} varies exponentially with the gate voltage below the threshold for the transition to the ON-state. For a classical field effect transistor, the thermal emission of carriers over the barrier leads to a theoretical lower limit of approximately 60 mV/decade

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at room temperature for the SS. This is equivalent to stating that an order of magnitude change of I_{DS} in the subthreshold region requires approximately a 60 mV change in gate voltage. This thermal lower limit gives rise to the description ‘Boltzmann’s tyranny’ resulting from both Fermi-Dirac statistics and the density of states (DoS) for the charge carriers.

To overcome the thermally limited SS in classical FETs, transistors relying on band-to-band tunneling (BTBT) or tunnel FETs (TFETs) have been introduced^{2,3}. These devices rely on tunneling across a band gap by carriers in the valence/conduction band edge in the source to a conduction/valence band edge in the drain. Since the carriers are modulated by a gate voltage that brings the tunneling carriers in or out of resonance, the Boltzmann limit does not apply and SS values of 30 to 50 mV/decade have been predicted⁴. To fabricate a TFET structure, it is often desirable to introduce heterojunctions to improve performance^{5,6}. However, constructing nanoscale TFETs using heterojunctions and abrupt doping profiles to define both source and drain can cause large device-to-device variations.

Here a semimetal nanowire field effect transistor (SM-TFET) with lower than the thermal limit for the SS is proposed and advantages related to fabrication and improved transistor properties within the scheme are highlighted. For demonstrating the concept, an α -tin nanowire is used as a prototype. It has been shown that the α -tin phase in thin films can be stabilized⁷⁻¹¹. Furthermore, for α -tin nanowires with diameters below approximately 5 nm, a semimetal-to-semiconductor transition leads to a band gap of >100 meV; the energy of the band gap increases rapidly with reduced nanowire cross section¹². Based on the semimetal-to-semiconductor transition, it was shown by *ab initio* electronic structure and charge transport calculations that within a single nanowire -with a region wider than the critical dimension for the transition adjoining a narrow section of the wire with cross section dimensions below the critical dimension- that a semimetal-semiconductor junction in a monomaterial can be formed and will behave as a Schottky barrier. It was further demonstrated that using this behavior in a semimetal nanowire, that a Schottky barrier transistor can be designed¹². In the current context, the concept of a monomaterial Schottky barrier diode is applied to demonstrate that properties of nanowire FETs can be significantly enhanced using this concept, but requires altering the architecture with respect to the Schottky barrier transistor¹².

For a ‘zero gap’ bulk semimetal such as α -tin, quantum confinement leads to an induced energy gap in a two-dimensional (film) or one-dimensional (nanowire) between the conduction and valence band edges at the Γ -point in the Brillouin zone. The value of the induced gap is controlled by varying the film thickness or cross sectional area of a semimetal nanowire. The proposal for the SM-TFET is to construct a structure with a semimetal (tin) source adjoining a narrower section of the nanowire, the latter is used to create both an intrinsic semiconducting region as the channel and n -type doped region acting as the drain. A gate-all-around geometry is introduced to achieve electrostatic gating of the channel region to control tunneling in the sub-threshold region. As will be shown in contrast to conventional TFET architectures, the ON current is not limited by tunneling.

The electronic structure computations are performed using density functional theory (DFT). The local-density approximation (LDA) is used for the exchange-correlation potential¹³. A numerical atomic orbital basis set for the tin and dopant atoms are defined using optimized orbitals with three orbitals per atomic level, or ‘triple-zeta’ quality¹⁴. Note that the underestimation of the band gap typical of approximate exchange-correlation functionals used for practical DFT calculations implies that the actual quantum confinement effect occurs at larger nanowire diameters than predicted by the DFT/LDA calculations¹⁵; for example, the band gap predicted for a 1 nm circular Sn nanowire is expected to occur at approximately 3 nm diameters. The

atomistic structure of the SM-TFET is allowed to relax by minimizing the energy with respect to atom positions until the maximum force component per atoms is less than 0.01 eV/Å. The unit-cell along the transport axis of the device are periodic for the energy minimization and the transverse cell dimensions are chosen large enough to neglect the interaction between neighboring nanowires arising from periodic boundary conditions. The effect of *n*-type antimony (Sb) doping in the drain region of the narrow tin nanowire section are evaluated for doping concentrations of $N_{D1} = 2.5 \times 10^{20} \text{ cm}^{-3}$ and $N_{D2} = 8 \times 10^{20} \text{ cm}^{-3}$. The electronic band structure of the doped Sn nanowire with a 1 nm diameter is compared to an intrinsic Sn nanowire with the same diameter in Fig. 1. Dopant atoms are introduced onto substitutional sites. The curvature of the first energy subband in the conduction band is similar in Figs. 1(a) and 1(b) for the intrinsic and lower doping, respectively, while there is slight increase in Fig. 1(c) for the curvature at higher doping. This corresponds to almost equal electron effective mass for the intrinsic and lower doped nanowires of $m_{e,\text{intrinsic}} = 0.089m_0$ and $m_{e,ND1} = 0.093 m_0$, respectively, and a slightly higher effective mass of $m_{e,ND2} = 0.109 m_0$ at the higher doping concentration. The doped regions are used to define the drain and for the analysis of the SM-TFET, both doping concentrations are considered.

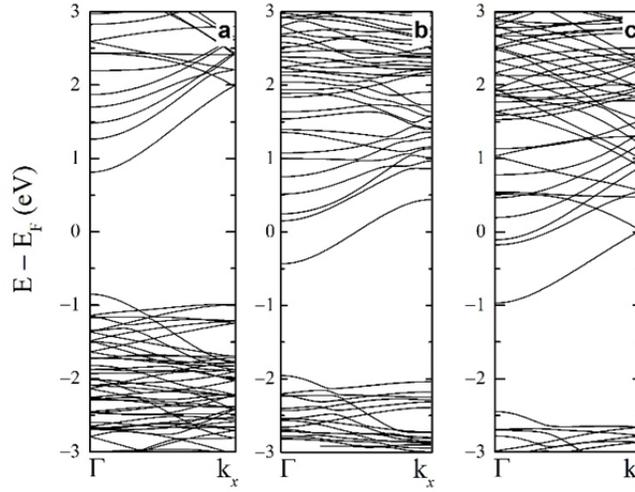


FIG. 1. Band structure of (a) intrinsic, (b) *n*-type with doping concentration of $N_{D1} = 2.5 \times 10^{20} \text{ cm}^{-3}$, and (c) *n*-type with doping concentration of $N_{D2} = 8 \times 10^{20} \text{ cm}^{-3}$ for a 1 nm-diameter tin nanowire with a [110] crystallographic orientation. The zero of energy is taken to be the Fermi energy.

The proposed SM-TFET architecture is shown in Fig. 2. The figure illustrates the atomistic structure of a nanowire with a thicker, approximately square, region of cross sectional area $4.5 \text{ nm} \times 4.5 \text{ nm}$ forming the source, and the narrower, approximately circular cross sectional area, with a diameter of 1 nm extending from the wider source region. A physical gate length of 3 nm is shown as the cylindrical equipotential surface wrapped around the channel. There are 1 nm extensions on either side of the gated channel region. The oxide isolating the gate electrode from the channel is treated only through electrostatic coupling, the gate dielectric coupling is chosen to be described by a 1 nm-thick hafnium oxide with a dielectric constant of $\kappa_{\text{HfO}_2} \sim 25$.

The resulting electronic structure as shown in fig. 2(b) is such that an electron tunneling from the Fermi level of the source, or the ‘valence band edge’ of the semimetallic region, must tunnel across the channel region to the conduction band in the drain region and hence constitutes a BTBT mechanism. However, with the application of negative gate bias and at 0.3 V

drain-source bias, there remains an approximately 5 nm long tunneling path and current is strongly suppressed in the OFF state; see fig. 3(a).

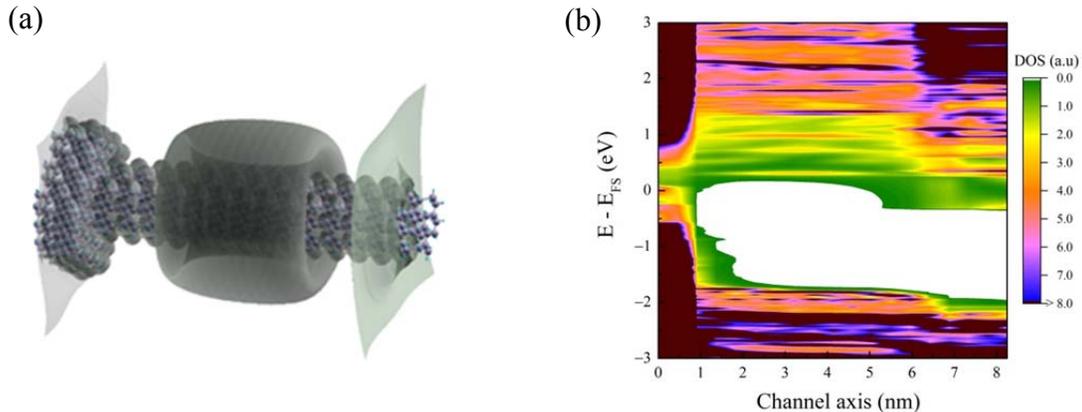


FIG. 2. (a) Atomic scale illustration of the proposed SM-TFET structure. All surface dangling bonds are passivated by bonding to hydrogen. (b) The local density of states (LDoS) for the nanowire device in (a). The semimetallic source region is on the left and the zero of energy is taken to be the Fermi level at zero drain-source voltage (V_{DS}) and zero gate voltage (V_{GS}). The central region in white indicates the band gap for the intrinsic channel, and the region in the right of LDoS diagram indicates the n-type doped drain region also with the band gap indicated in white. Note the formation of MIGS in the lower left and upper right regions in the channel band gap at the source/drain interfaces.

To investigate device operation as drain-source and gate voltage biases are applied, the electron transmission at a given bias point is calculated self-consistently using the DFT/LDA Hamiltonian with self-energies describing ‘semi-infinite’ drain and source electrodes within the method of the non-equilibrium Green’s function (NEGF)¹⁶. The 5 nm channel region is sufficiently large to eliminate coupling between the source and drain, enabling the source/drain regions to be extended as (semi-infinite) ‘ideal’ electrodes. The electrode conditions are achieved by holding the source and drain regions at thermal equilibrium described by Fermi-Dirac distributions at $T=300\text{K}$, but driven away from equilibrium with respect to each other by the chemical potential difference $\mu_{DS} = qV_{DS}$.

The local density of state (LDoS) across the SM-TFET is plotted in Fig. 3 as a function of energy and position at a fixed drain-source voltage of $V_{DS}=+0.3\text{ V}$ and for $V_{GS}=-0.12\text{ V}$ (OFF); $V_{GS}=0$ (subthreshold region); and $V_{GS}=+0.12\text{ V}$ (ON). At $V_{GS}=-0.12\text{ V}$, the potential profile across the channel leads to the formation of a sharply defined state above the potential barrier. This state can as a first approximation be thought of as an energy level in a triangular barrier formed between the source/channel barrier, the ‘linear’ voltage drop due to application of V_{DS} across the channel, and the heavily doped drain. In the OFF state, the tunneling current dominates. As the gate voltage is increased to turn the device ON, the energy level formed in the channel lowers in energy as the potential in the channel lowers and extends further into the channel becoming resonant with occupied states in the source; a side by side comparison between the LDoS in fig. 3 and the energy resolved currents shown in fig. 4 is shown in the Supplementary Material. As the state extends further into the channel at higher gate voltages, it hybridizes with the states in the source (see Fig. 3 (b) and (c) in particular). At sufficiently large gate voltages the channel is effectively in inversion as the state lowers and the source/channel barrier lowers; see fig. 3 (c). In the ON state, higher states formed in the channel begin to couple to thermally excited states in the source and the energy-resolved current is broadened. The voltage barrier as the source ‘collapses’ and electrons near in energy to the source Fermi level can flow

across the channel region without tunneling. Hence in the ON state the current becomes a combination of tunneling and ‘over the barrier’ transport resulting in a sharp current increase defeating the Boltzmann tyranny limit. The sharply peaked density of states associated with the formation of channel states overcomes the usual assumptions leading to the thermal limit, thereby allowing for a $SS < 60$ meV/dec.

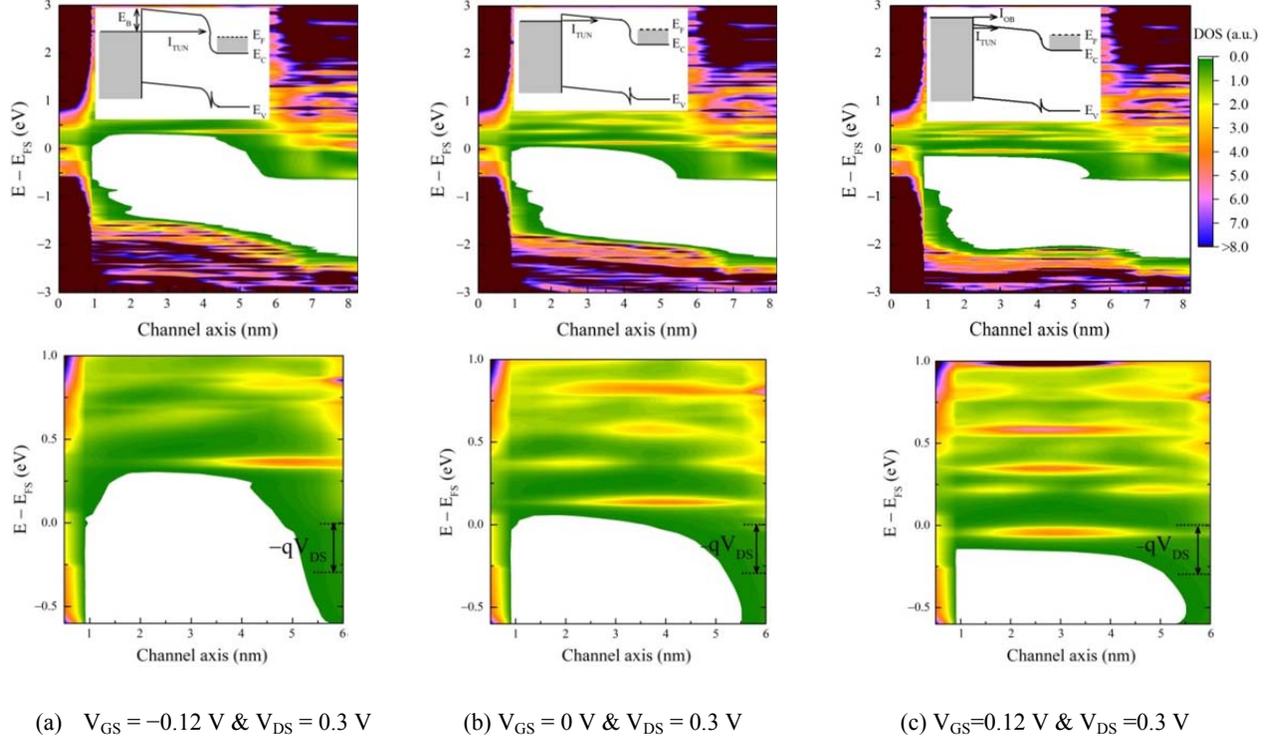


FIG. 3. Energy resolved local density (LDoS) with $V_{DS}=0.3$ V and varying V_{GS} for the device with drain doping N_{D1} . (a) OFF-state: $V_{GS} = -0.12$ V (b) Sub-threshold region: $V_{GS} = 0$ V (c) ON-state: $V_{GS} = 0.12$ V. Similar profiles have been observed with drain doping N_{D2} . Voltages referenced to the source. A schematic illustration of the band diagram is provided as an inset at each bias point. Bottom row is an enlarged view of the LDoS for energies near the source Fermi level.

To reinforce the analysis accompanying Fig. 3, the currents from drain to source are decomposed into two components. The first component is the fraction of electrons tunneling across the channel, *i.e.* for electrons that flow from the source-to-drain but that are lower in energy than the energy barrier E_B at the source-channel interface. The tunneling current from these electrons is defined as $I_{TUN} = \int_{-\infty}^{E_B} i(E)dE$ where $i(E)$ is the energy resolved current. The second component accounts for electrons emitted from the source with energies greater than E_B or ‘over the barrier’ (OB), their associated current is defined as $I_{OB} = \int_{E_B}^{\infty} i(E)dE$. Energy resolved current profiles for the bias-dependent contribution of each of the current components are shown in Fig. 4. For the OFF-state given by $V_{GS} = -0.12$ V, all electrons tunneling from the source are ‘under the barrier’ and the only current transport is BTBT. As the gate voltage increases to $V_{GS} = 0$, the energy barrier decreases leading to a higher ON-current dominated by BTBT, and as well significant contributions of the current is from the ‘over the barrier’ components associated with the thermal distribution in the source and the sharply peaked density of states in the channel.

Finally as the gate voltage is increased further to $V_{GS} = +0.12$ V, the majority of the current is due to the ‘over the barrier’ component, but nonetheless the BTBT component remains significant.

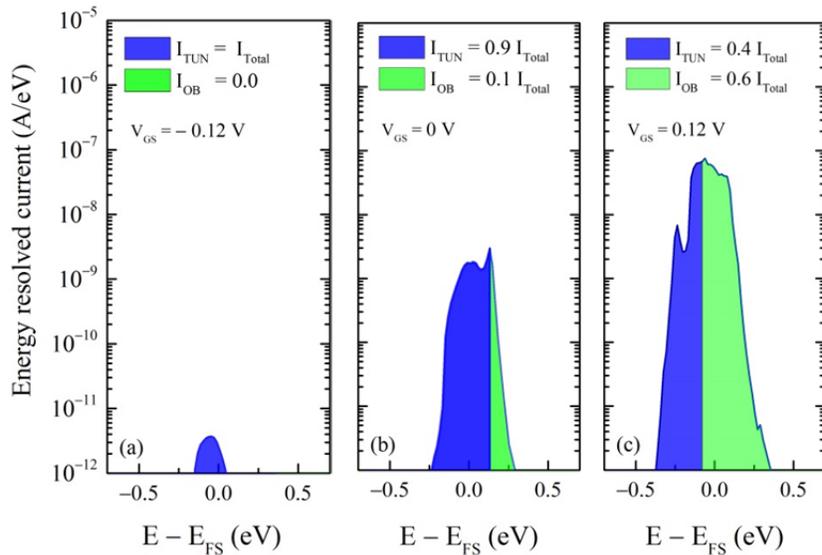


FIG. 4. Energy-resolved current profiles at (a) $V_{GS} = -0.12$ V, (b) $V_{GS} = 0$ V, and (c) $V_{GS} = +0.12$ V. All currents obtained at $V_{DS} = +0.3$ V. The contribution of the tunneling current (area shaded in blue; dark grey in b/w) and over the barrier transport (area shaded in green; light grey in b/w) are shown. Note the position of the potential barrier for $V_{GS} = -0.12$ V is above the source Fermi level but ‘collapses’ as the gate voltage is increased. The barrier collapse implies the surface dipole at the source-channel interface can be compensated with increasing gate voltage.

The current-voltage characteristic for the TFET at fixed V_{DS} and varying V_{GS} is shown in fig. 5. Subthreshold swings of 39 mV/dec and 28 mV/dec are predicted with N_{D1} and N_{D2} doping concentrations in the drain, respectively, at room temperature. Thus the tunneling current below threshold dominates and a value for the SS below the theoretical limit of a classical FET is achievable with the design. That is in itself of interest, however other designs offer similar theoretical behavior. However, there are key distinctions between the SM-TFET and previous TFET proposals. The SM-TFET is comprised of a single nanowire that has been thinned in one region, and high performance is achieved without requiring hetero-epitaxy. The fact that the source-channel junction is achieved by shape engineering to generate a Schottky barrier implies no dopant diffusion occurs at the source-channel junction, helping to define a sharp tunneling region. The proposed structure for the SM-TFET provides remarkably higher on-state current in comparison to state-of-the-art TFET designs due to the ‘barrier collapse’ and the significant contribution of resonant current^{6, 17-19} arising from states formed in the channel yielding a sharp peak in the density of states as the device turns ON. For the drain doping concentration N_{D1} and N_{D2} , the ON-state at $V_{DS} = +0.3$ V and $V_{GS} = 0.32$ V are $3.1 \text{ A}/\mu\text{m}^2$ and $7.7 \text{ A}/\mu\text{m}^2$, respectively.

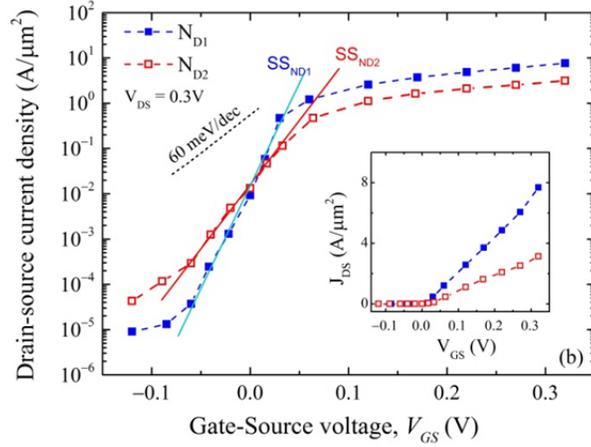


FIG. 5. I_{DS} versus V_{GS} characteristics of the SM-TFET for two doping profiles at $V_{DS} = 0.3$ V. A sub-threshold slope lower than the ‘Boltzmann tyranny’ limit has been achieved at both drain doping concentrations. The inset shows the same plot in linear scale.

It has previously been shown that using heterojunctions in TFET devices improves the device performance^{6,20,21}; however, constructing TFETs with heterojunctions on nanoscale lengths imposes critical challenges from a device fabrication point of view. Clearly fabrication of the semimetal device poses different challenges in terms of changing the diameter of a nanowire in selected regions and doping of semimetals. Nonetheless, the proposed SM-TFET is constructed from a single material yet is able to introduce a heterojunction at the source-channel junction. Applying the gate electric field modifies the channel band structure allowing for a sharply peak DoS allowing for a much more rapid increase in channel current with gate voltage than associated with conventional FETs.

In summary, a SM-TFET with a heterojunction structure is proposed with a *monomaterial* design. NEGF simulations reveal that the proposed SM-TFET architecture provides a remarkably high ON-current due a combination of resonant transport and due to the energy barrier collapse at the source, an effect not seen in semiconductor heterojunctions; see the discussion in Supplementary Material. The barrier collapse and the sharp density of states arising from the resonant state forming in the channel from the drain enables a sharply increasing transmission in the sub-threshold region, and the advantage over conventional TFETs of ‘over the barrier’ transport in the ON-state. The current-voltage characteristics for the SM-TFET indicate that subthreshold slopes lower than the thermal limit for conventional MOSFETs can be achieved with gate lengths of 3 nm and source to drain distance of 5 nm.

SUPPLEMENTARY MATERIAL

See the Supplementary Material where details are provided for the electron transmission for different gate voltages and drain doping concentrations; background information on the calculation of electronic current within the NEGF approach; definition of the subthreshold slope; Mulliken population analysis in the channel region under different gating conditions and the effect on the interfacial dipole at the Schottky barrier; a side by side comparison of the LDoS in the device to the energy resolved current.

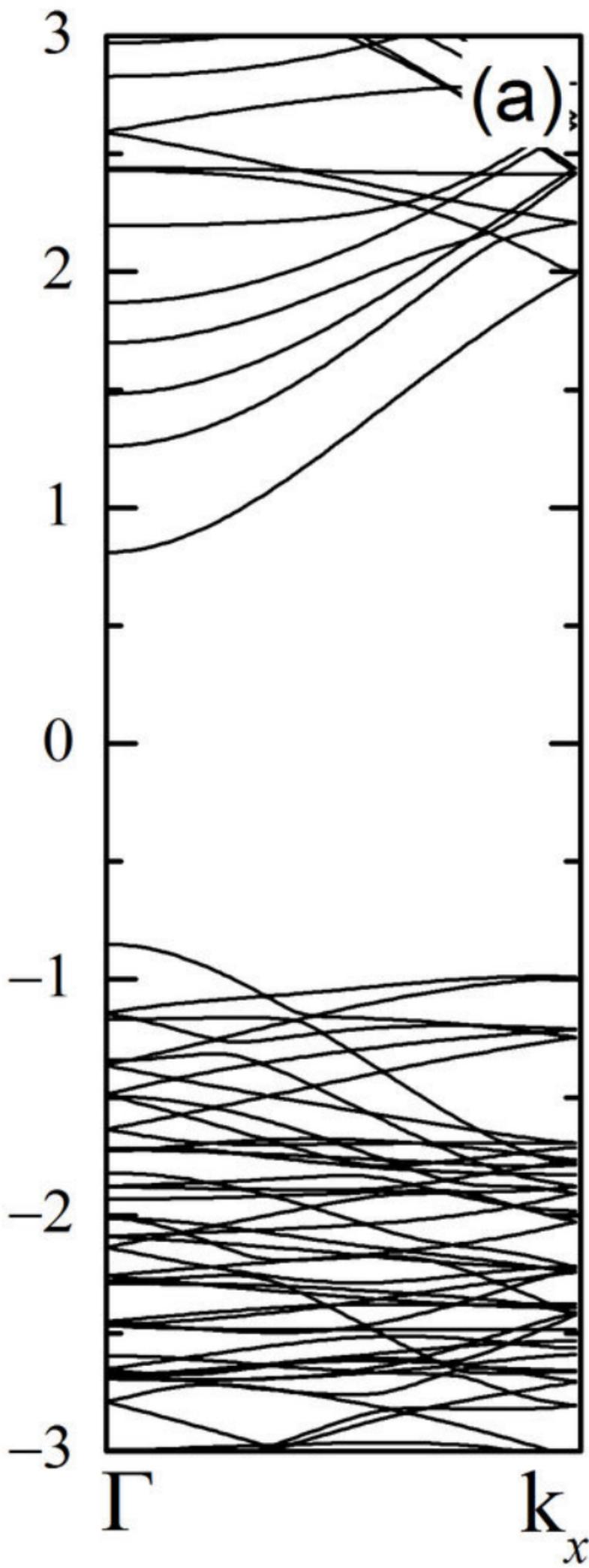
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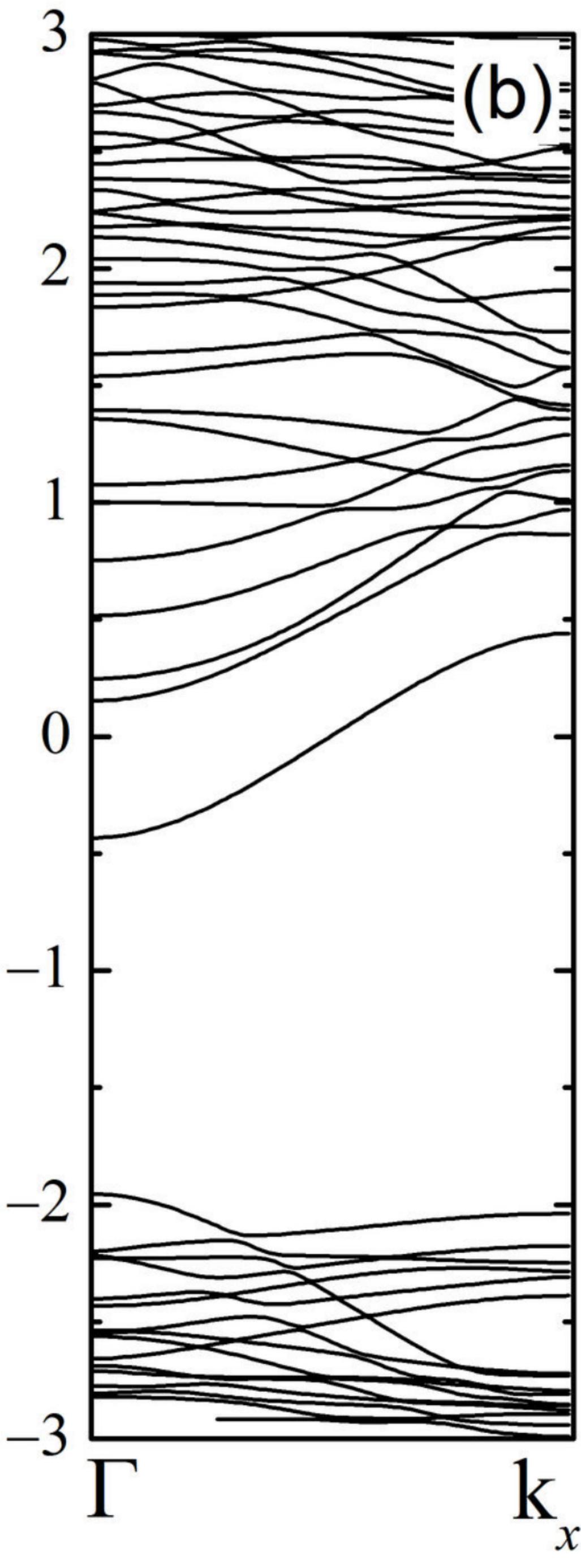
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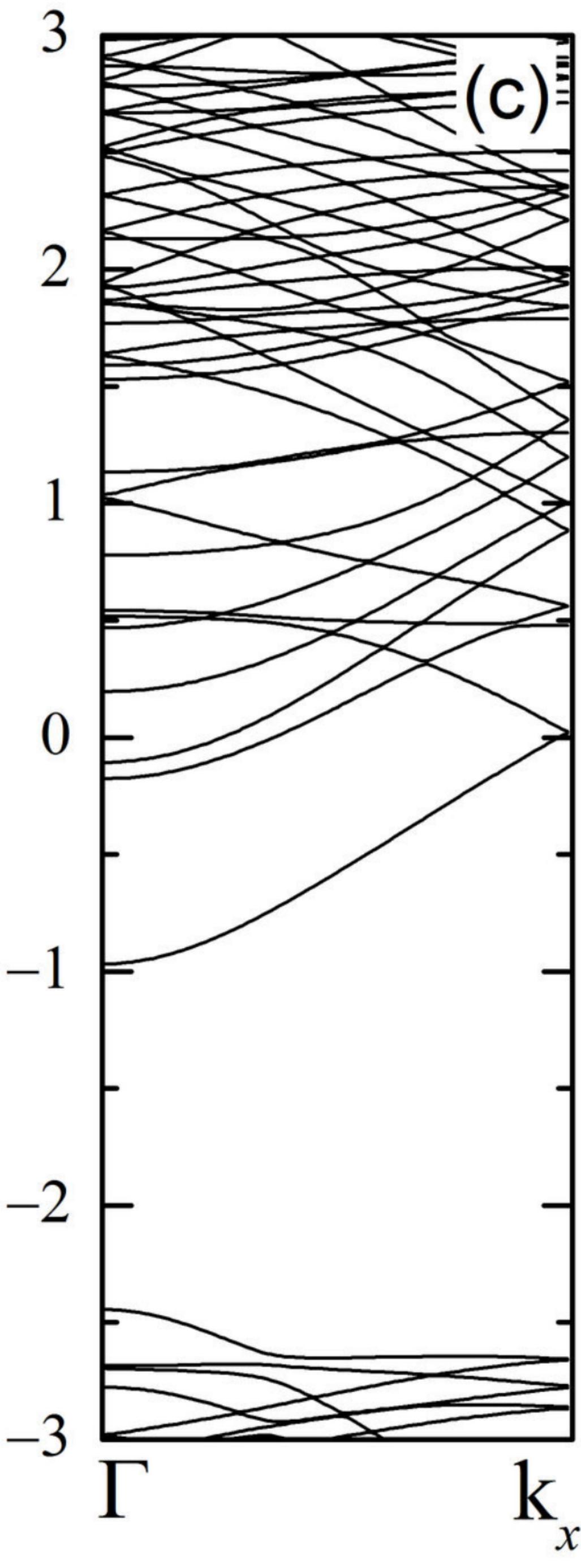
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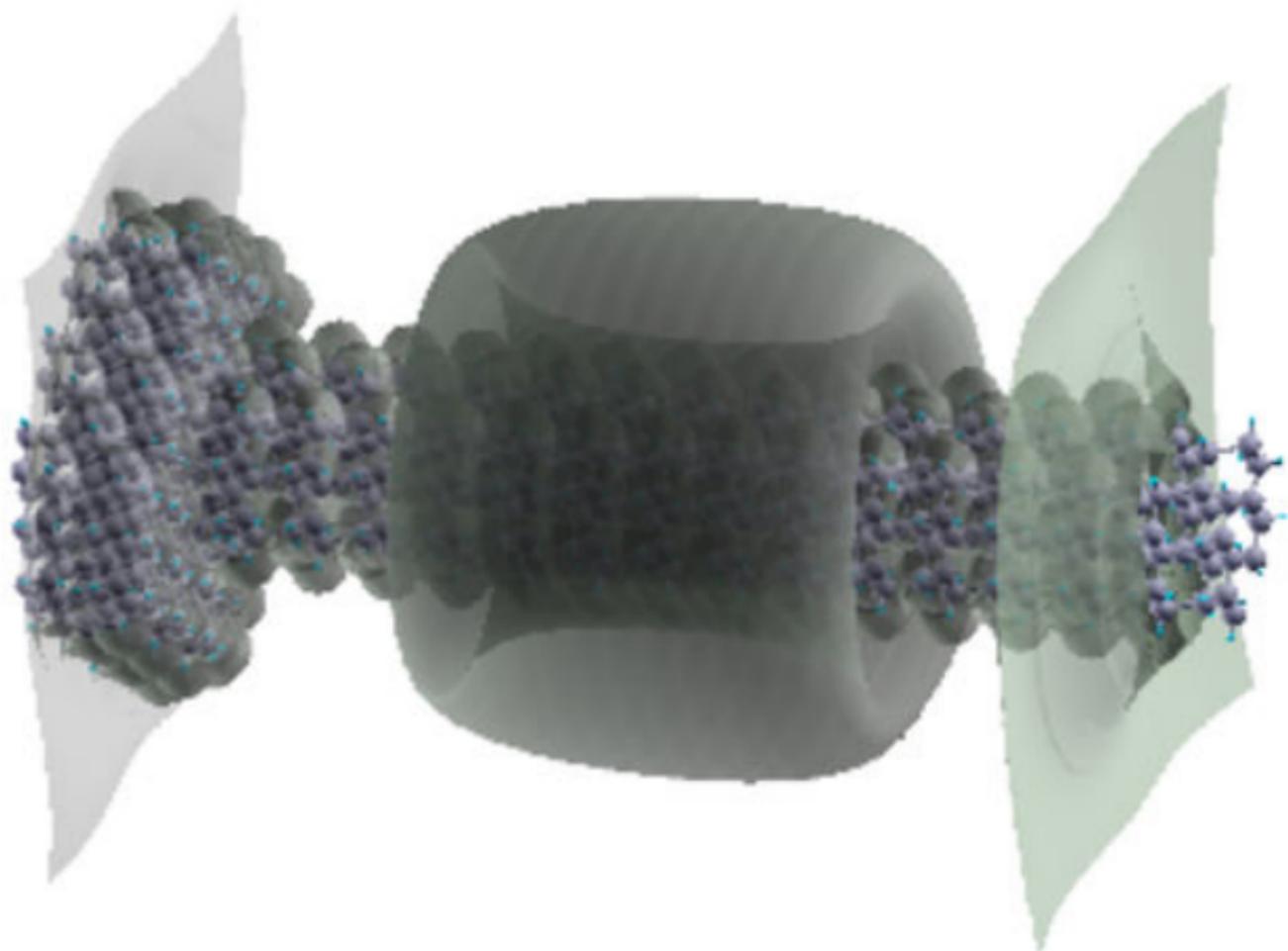
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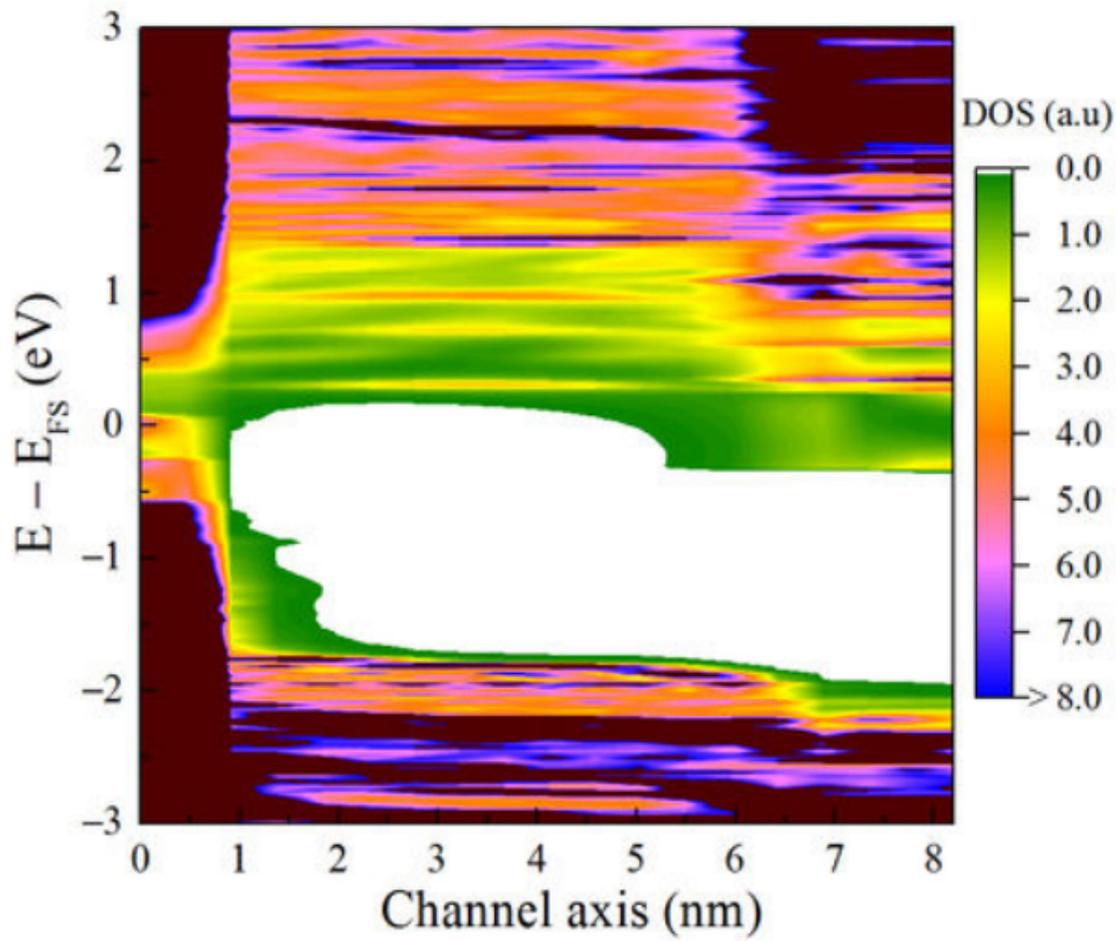
$E - E_F$ (eV)

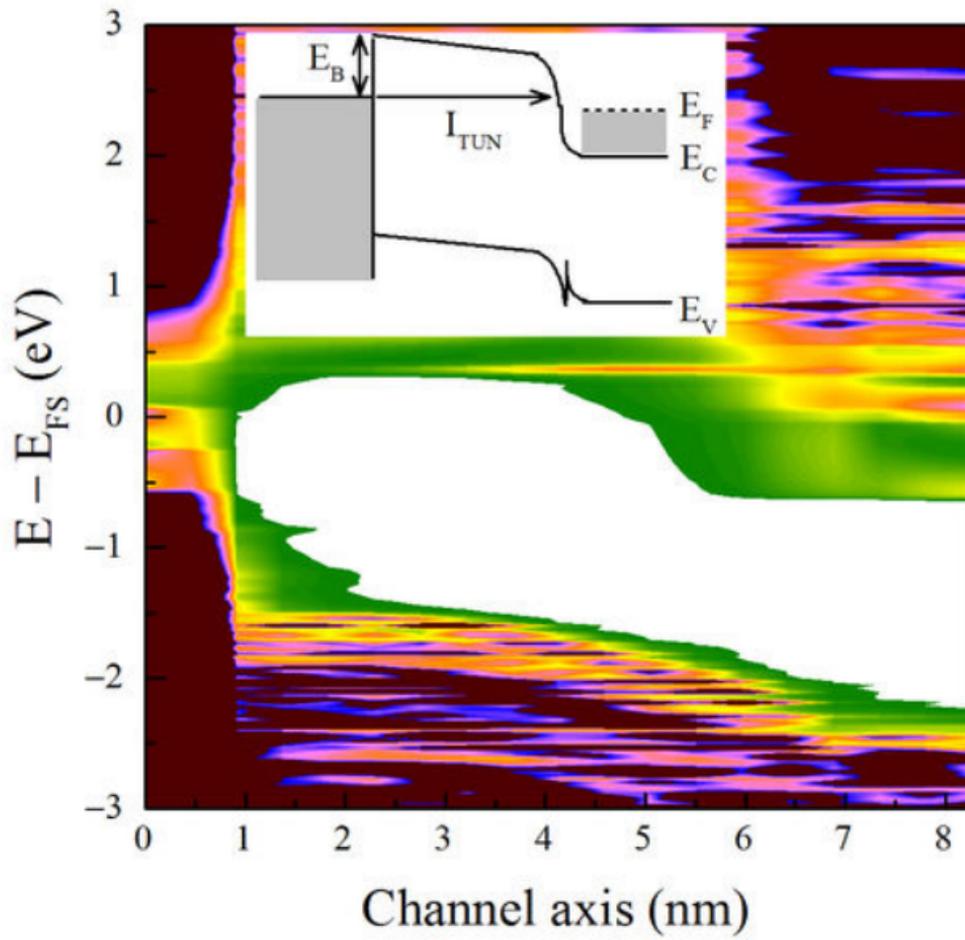


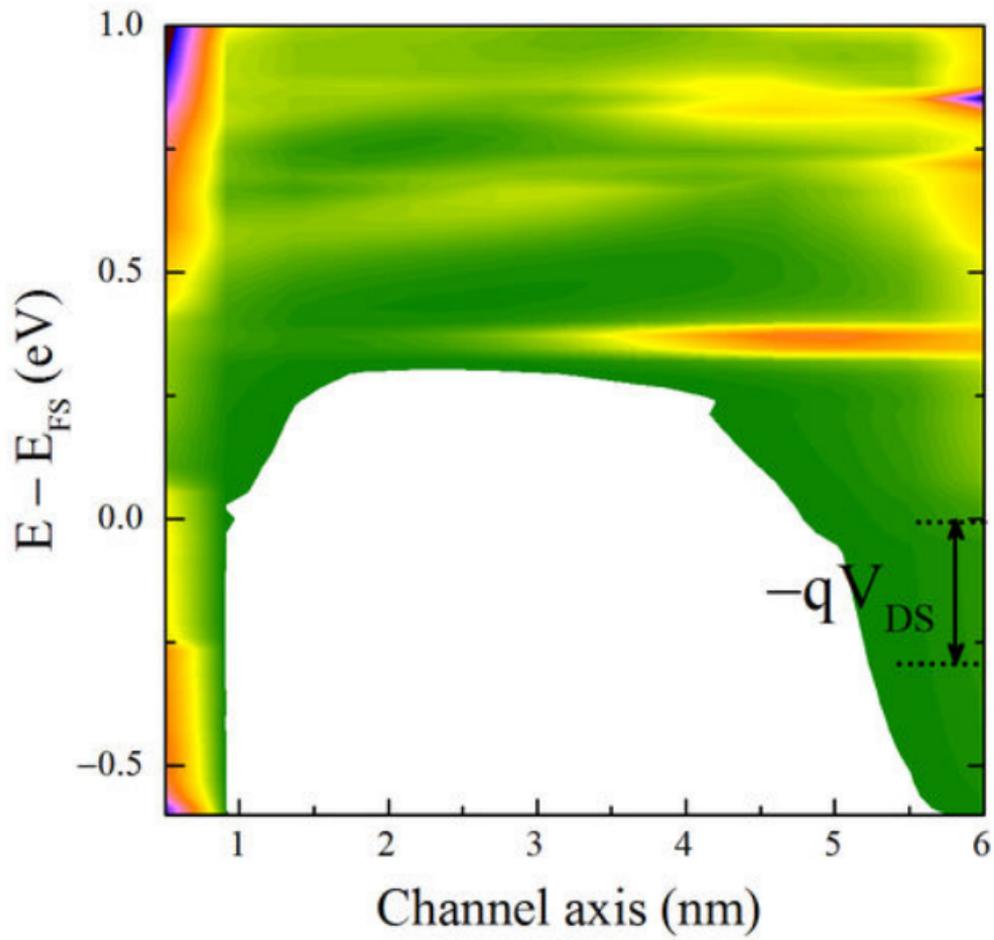


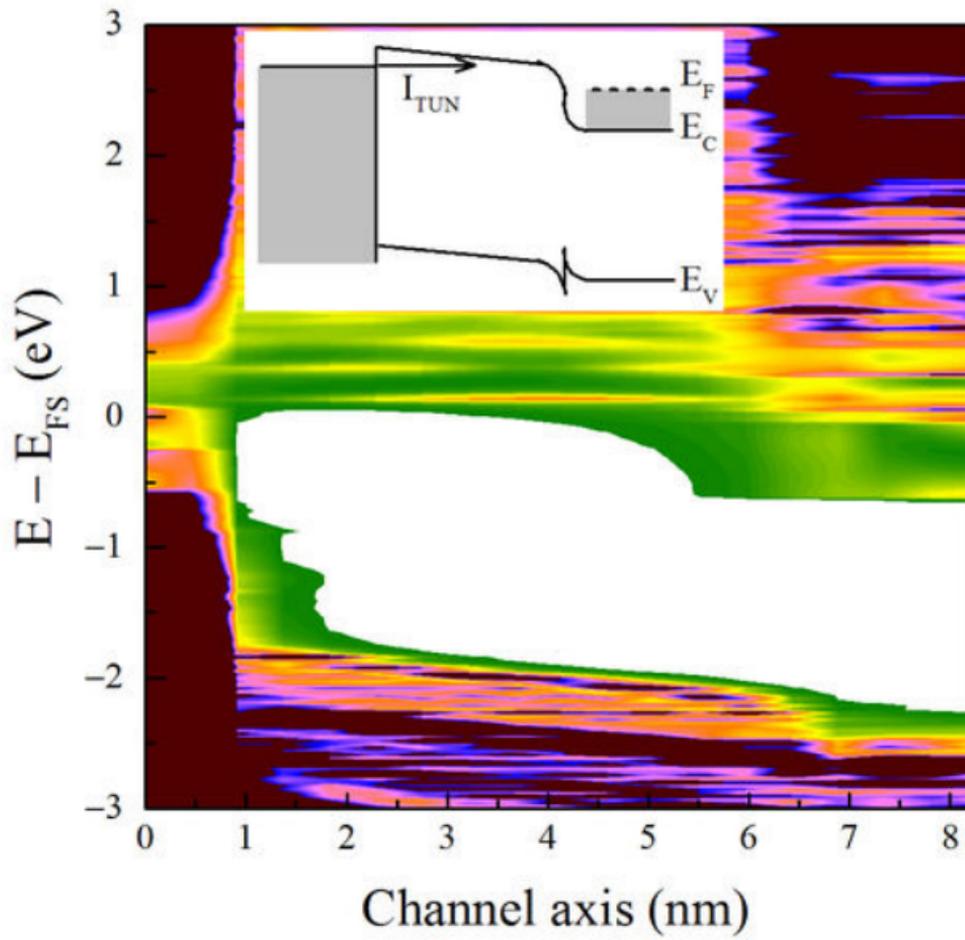


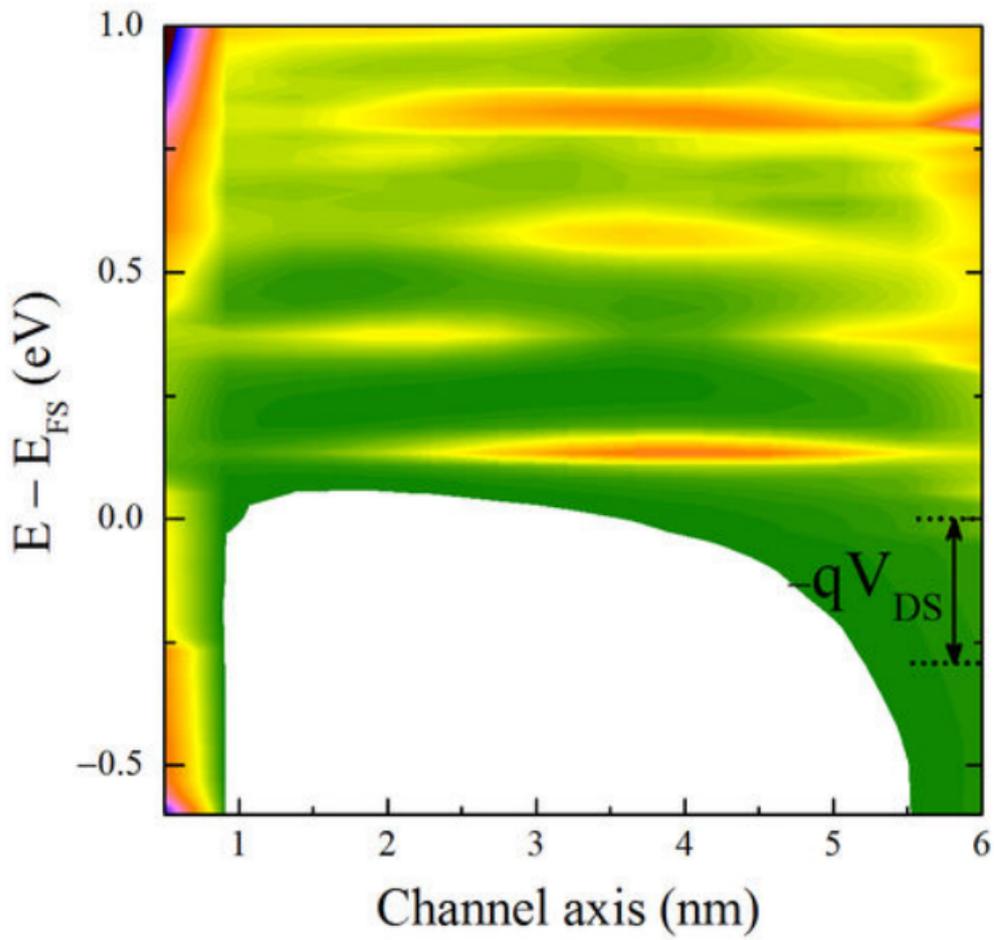


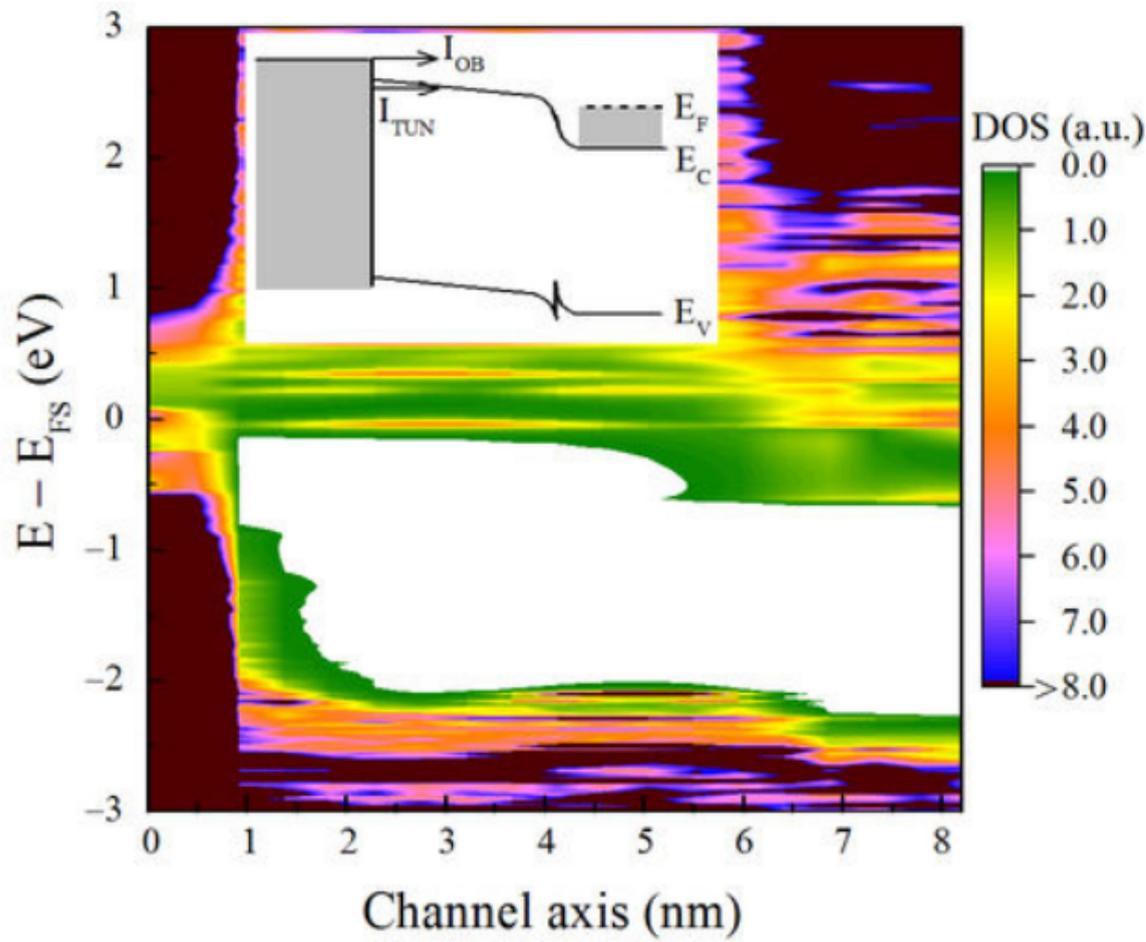


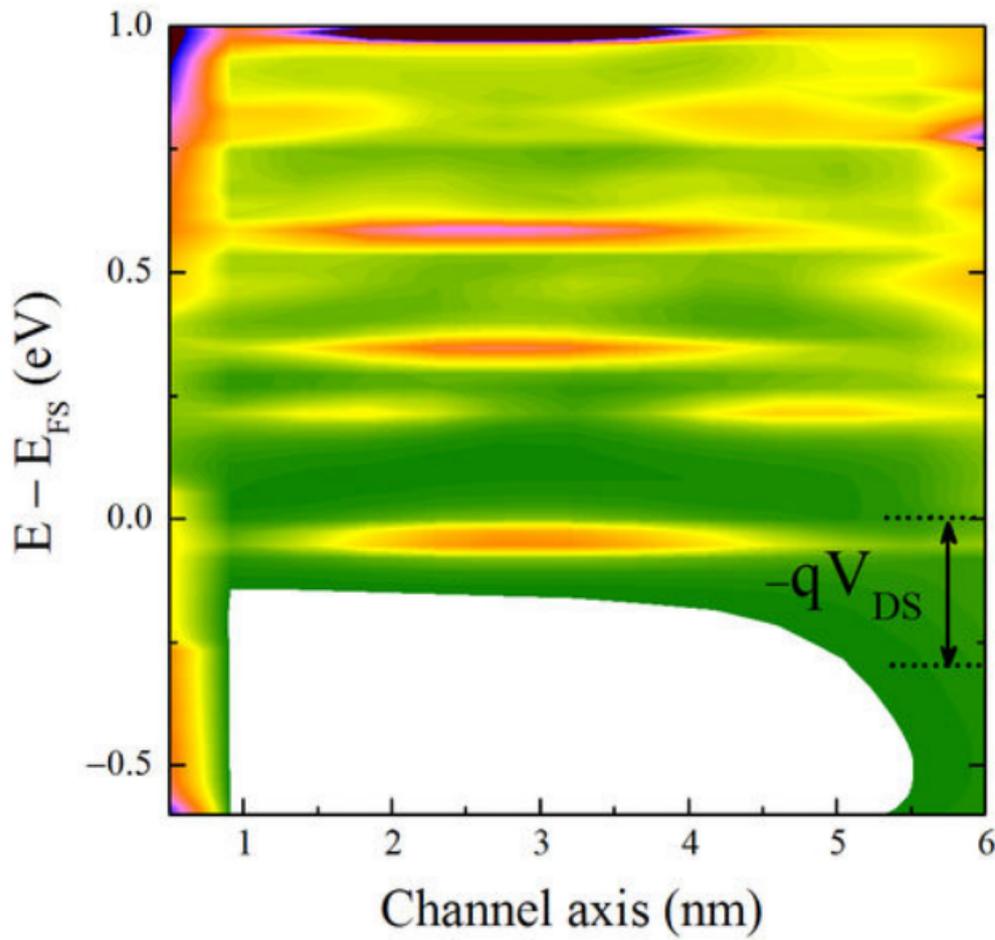




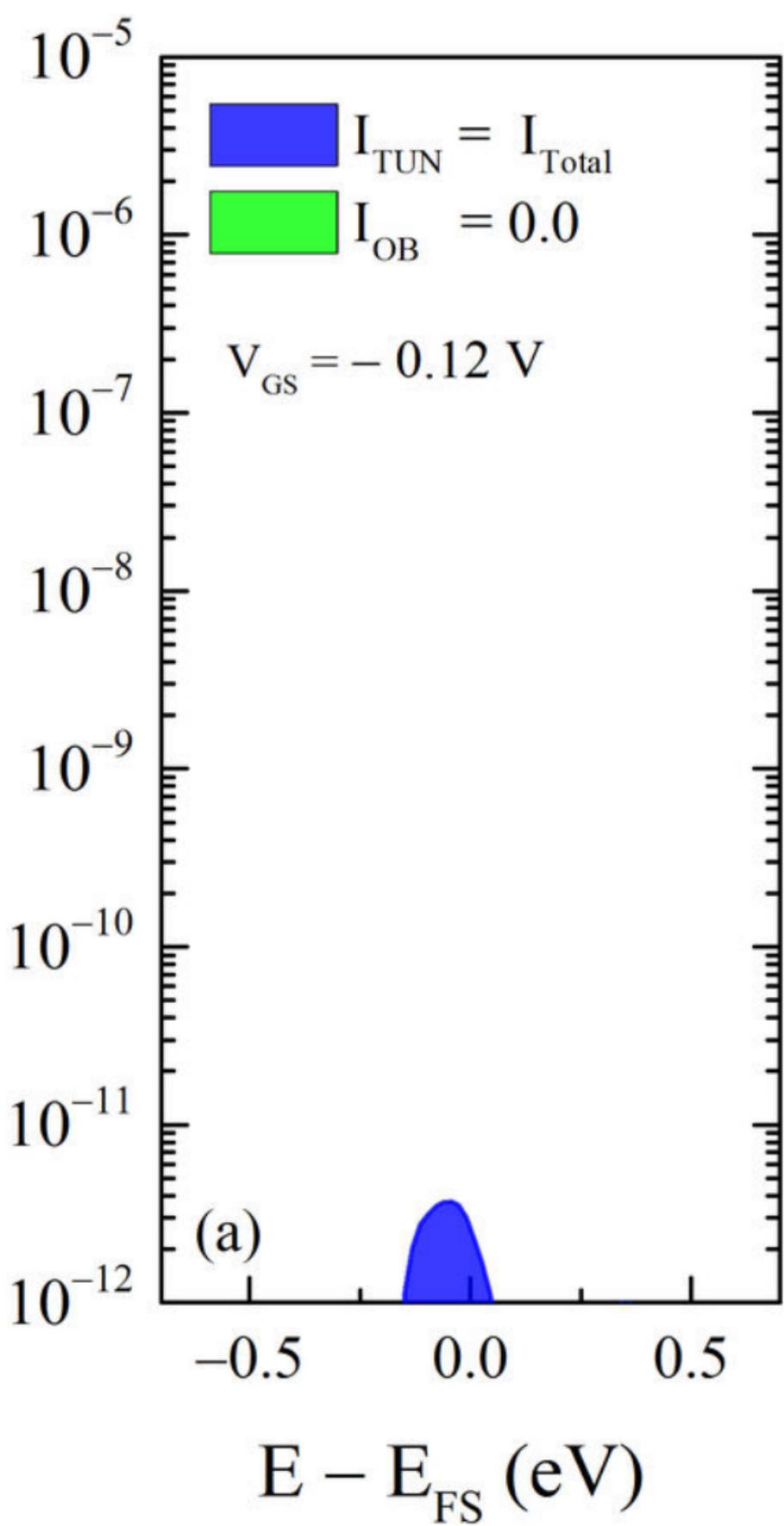


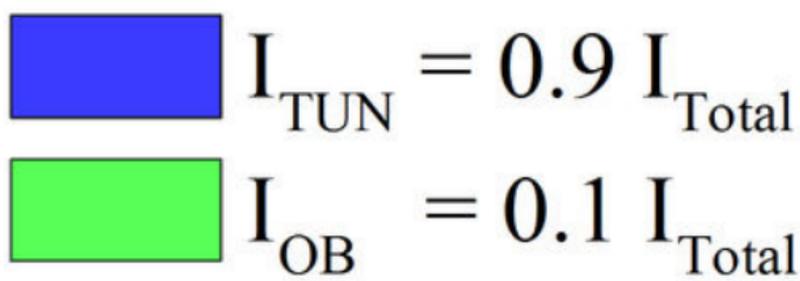






Energy resolved current (A/eV)



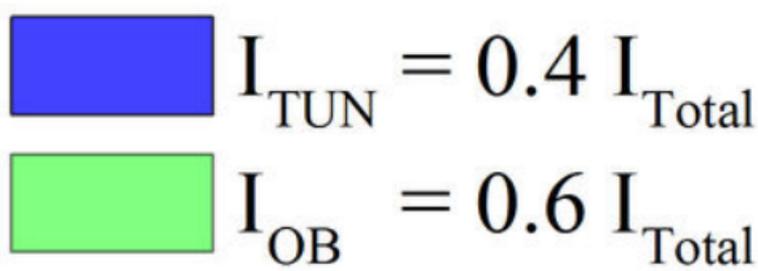


$$V_{\text{GS}} = 0 \text{ V}$$

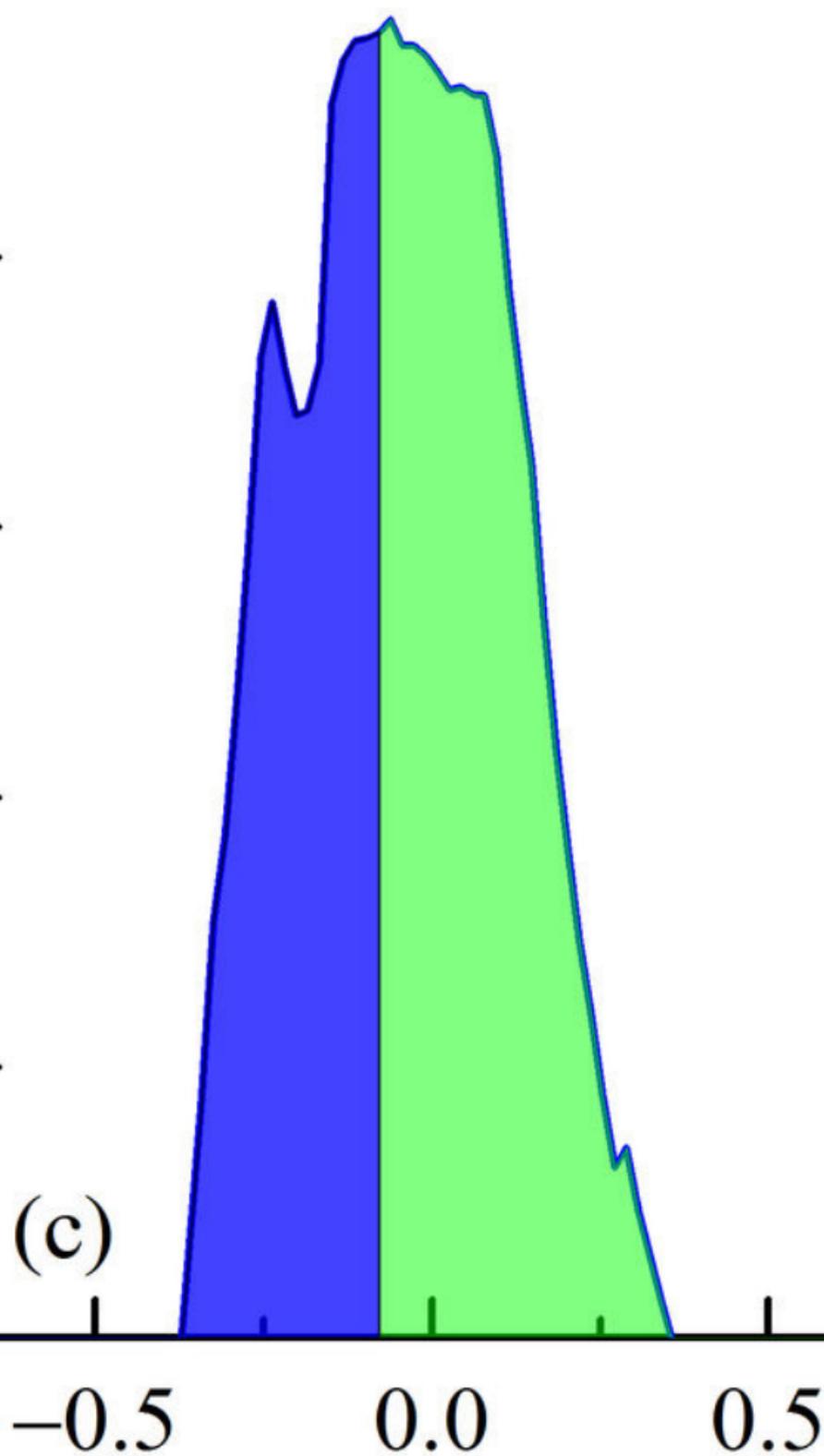
(b)

-0.5 0.0 0.5

$E - E_{\text{FS}} \text{ (eV)}$



$V_{\text{GS}} = 0.12 \text{ V}$



(c)

$E - E_{\text{FS}} \text{ (eV)}$

