An investigation of MMC based DC-DC converter for HVDC grids

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Abstract

The interconnection of multiple offshore renewable energy sources to form a network and maximise their availability requires a method for controlling the transportation of bulk electrical energy. For the distances considered, and as a result of the capacitive nature of HVAC cables, HVDC is the most likely technology for meeting these bulk transport requirements.

This research investigates the development of an MMC based Dual Active Bridge (DAB) for interfacing two different parts of a HVDC network. Computational tools are developed in order to design and evaluate such a power electronics structure as well as to support the design process of the transformer required for scaling and matching voltages between the two parts of the network. Linear control techniques are applied to control the converter to operate at the required average capacitor voltage level and power transmission. Simulation results, supported by experimental data from a low voltage MMC prototype are presented to validate the approaches.

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Chapter 1

Introduction

1.1 Background of the outline of the research project

1.1.1 Brief introduction to the human energy problem

The epic challenge of the 21st century is filling the gap between energy supply and the demand with clean, reliable and inexpensive energy[1]. Among various forms of energy sources, electrical energy is an important factor in economic development. Conventional ways of producing electricity are fossil fuel plants and nuclear fission plants. However these two sources are becoming insufficient in the new century.

In the last century, world energy was mainly based on fossil fuels, such as oil, coal and natural gas. It is also reported that the sources of fossil fuel are being found at an increasing speed[2]. So the contemporary situation of wide application of fossil fuel will not change fundamentally in the near future. However, it is widely accepted that:

- 1. Fossil fuel is not a sustainable source of energy and supplies will be exhausted.
- 2. It produces greenhouse gas in the burning process.

The history of using nuclear fission plant to generate electricity is about

50 years[3]. The power generated by fission plants contributes to 7% of the global power generation and about 35% in the European electricity market[3]. The consequences of widespread exploitation of nuclear fission plant is the high radioactive waste, which is not possible to dispose except by temporary storage, in the expectation that a future technology will be able to dispose of it in a safe way. In addition, although nuclear accidents are rare, the impact of accidents on large regions and local residents are severe, long-term and profound.

Since conventional energy sources have the problems of unsustainability and negative environmental impact, the energy problem is not a problem that can be solved once for all. So it is worthwhile to invest in different sources of energy to increase the quantity of the energy production, though these sources might not change the entire structure of the energy production on a fundamental base. It is widely believed that a large amount of energy sources are contained in remote offshore regions, such as offshore wind energy, offshore oil and gas. There have been successful commercial projects of offshore wind generation. The bulk power generated offshore can be delivered to onshore customers or used to support other offshore loads such as gas and oil rigs[4]. It can be predicted that future offshore electric networks will be deployed and the energy produced will take a reasonable proportion in the European energy production.

1.1.2 Brief introduction to offshore HVDC networks

It has been accepted that in long distance bulk power transmission, High Voltage Direct Current Transmission systems (HVDC) has higher capacity and this will be discussed in Chapter 2. Because of the following reasons, complex HVDC systems need to be constructed.

- 1. Multiple electric energy sources such as offshore wind turbines and loads such as offshore oil rigs will be exploited. These sources and loads locate in different sites, so it is not practical to connect the sources and the loads with a point-to-point transmission system.
- 2. It is safer to construct multiple sources and loads to a network. If one fault occurs at one of the sources, the fault point will be disconnected. The load will be supported by the other sources. If one fault occurs at

one of the loads, the fault will be disconnected to prevent the effect of the fault influencing the other loads or the sources.

It is normally less costly to integrate multiple wind farms and transmit the power collectively via a single HVDC system. However different HVDC systems are generally not constructed as a final bounded system. They are normally started with a small scale system and extended to the final scale. However, offshore HVDC interconnectors are required to integrate different HVDC systems, forming regional HVDC networks.

1.2 **Project objectives**

The main aim of this PhD project is to research possible approaches to the development of DC-DC converters that will facilitate the deployment of future HVDC networks. Amongst the different topics regarding HVDC, this thesis focuses on the implementation of the integration of symmetric and bipolar offshore HVDC systems. The objectives are listed as follows:

- 1. Investigate the requirements for DC-DC converters applied in future HVDC networks.
- 2. Propose a feasible and reliable topology that meets the requirements of the DC/DC converter in offshore HVDC grids.
- 3. Design transformers that are feasible to be applied in the DC/DC converter
- 4. Derive mathematical models of the converter to develop computational design tools and design controllers.
- 5. Develop a control methodology to operate the DC-DC converter at the required power level and capacitor voltage level with circulating current harmonic suppression.

1.3 Thesis structure and content

The thesis is organised into 6 chapters.

In Chapter 2 the background of the thesis is discussed in detail. It discusses the offshore wind energy, the developments of offshore grids in European North Sea, HVDC systems and a proposed HVDC offshore network to locate the application of the high voltage DC/DC converter in this thesis.

In Chapter 3 the various structures of DC-DC converters are compared to decide the topology of the converter station Cd-E1. Topologies of converters such as Dual Active Bridge (DAB) and basic DC-DC circuit, distributed transformer based and multiwinding transformer based DABs are compared to propose a suitable topology. Different multilevel power electronic converters, such as cascaded H-bridge, diode clamped and Modular Multilevel Converter (Modular Multilevel Converter (MMC)) are compared to derive an appropriate converter arrangement for the DAB.

In Chapter 4 the analysis and design of a high voltage transformer with optimisation and dynamic equations of MMC are presented to derive the algorithms, which are used to develop computational tools to design the system and design the controllers for the MMC. The analysis and results of the design are also presented.

In Chapter 5 the control of the MMC and the DAB are discussed based on the parameters designed previously.

Chapter 6 presents the conclusions of the project and summarise the further work of the thesis.

Chapter 2

High voltage direct current transmission (HVDC) Offshore Grid

2.1 Introduction

This chapter presents a brief literature review about the background topics in this thesis. In Section 2.2 the future development of offshore wind energy in UK is discussed. An introduction to HVDC and contemporary offshore HVDC configurations is given in Section 2.3. A conceptual offshore HVDC network proposed by Cigré is discussed in Section 2.4, where the requirement for an offshore high voltage DC/DC converter is found.

2.2 Future European Energy Infrastructure

Europe's energy infrastructure is the central nervous system of European economy[4]. It consists of electricity generation, natural gas and oil. Wind energy as a source of clean and renewable energy plays an important part in electricity generation. This section first introduces current state of UK wind energy. Then offshore grids in the north sea are discussed.

2.2.1 UK wind energy

Wind has been proven a clean and renewable source of energy. Wind is essentially the movement of air flow caused by uneven solar heating of the atmosphere. Kinetic energy or motion energy stored in wind flow is converted into mechanical power and supplies an electric generator via a wind turbine. Compared with burning fossil fuels, the process of wind generation produces no greenhouse gas emission and causes no effect on the environment.

The UK is considered to be one of the best locations for wind power[5] in Europe. There is a growing percentage of UK wind energy as shown in Figure 2.1. Wind farms provided 9.3% of Britain's total electricity supply in 2014, up from 7.8% in 2013[6] and this percentage rose to 11% in 2015[7].



Figure 2.1: UK's wind farm generation in total electricity generation

Onshore wind vs offshore wind

Onshore wind energy already plays an important role in UK renewable electricity because it is one of the most cost-effective and mature of all renewable technologies. It is reported that generating electricity from onshore wind turbines typically costs around 7–9p per kWh, which is around half the cost of offshore wind and a quarter of the costs of solar photovoltaic panels[8]. Onshore wind generation is around 50% more expensive than fossil fuel generation(generating electricity from gas power plants currently costs between 4.1 and 7.5 p/kWh), but its price is expected to fall in the coming years.[8]

Although offshore wind energy sources are currently one of the most expensive energy technologies, offshore wind farms are advantageous for three main reasons:

1. Offshore wind is faster than onshore wind. The mean wind speed on the sea is faster about 25% than onshore wind[9]. Also, according to Equation 2.1, the power density of the wind flow is determined by the wind speed.

$$\frac{dP_{wind}}{dA} = \frac{1}{2}\rho V^3 \tag{2.1}$$

 P_{wind} is the of the wind flow, A is the sectional area of wind flow, ρ is the density of air and V is the wind speed. Therefore 25% higher wind speed implies the offshore wind power density is almost twice the onshore one. From Table 2.1[10] it is shown that the mean capacity of offshore wind turbines is 3.48MW while the capacity of onshore wind turbines is 1.64MW.

- 2. Offshore wind breezes faster in the afternoon, which meets the peakelectricity-demand time. Because solar radiation heats the land faster than water in the morning, in the afternoon the temperature of land is higher than the surface of water. As the land warms up, it heats the air by conduction. Warm air above land is less dense than cold air above water, so the pressure of cold air is higher than warm air. It causes the offshore airflow to onshore near ground. The circulation of air flow is shown in Figure 2.2. Offshore wind turbines take advantage of this phenomenon to operate at high wind speed at the peak-electricitydemand time.
- 3. Offshore wind farms can be constructed close to the power-hungryareas close to coasts. Good onshore wind sites are normally located in remote areas far from cities. Therefore long transmission lines are needed to bring the electricity from wind farms to customers. Offshore wind farms can be constructed in the coastal water near the city. The largest offshore wind farm, London Array, is located 20km off the Kent coast and supplies London with a power of 650MW.



Figure 2.2: Lake-Land breeze

Table 2.1: Operational figures of onshore and offshore wind farm

	number of turbines	capacity(MW)
Onshore	$5,\!227$	8,578
Offshore	1,465	5,098

UK offshore wind technology has developed with government's support for more than 17 years[11]. Active programmes are driving improvements in yields, reduction of cost and an acceleration in deployment[12]. Therefore it is positive to expect that UK offshore wind energy will have another round of expansion. More projects will be constructed and existing wind farms will be expanded.

2.2.2 Offshore grid in the North Sea

Offshore grid in the North Sea and connection to Northern and Central Europe is one of the priority corridors in future European energy integration according to European Commission[4]. The term North Sea Offshore Grid (NSCOGI) was proposed to interconnect national electricity grids in North-

west Europe and offshore wind projects[13]. The offshore grid is beneficial in terms of renewable energy integration for the following two main reasons:

- 1. The increase in the reliability of the grid. In a single point-to-point transmission system, if a fault occurs in the transmission line or the generator, the supply to the customer will not be guaranteed. In a system with multiple supplies, if one of the transmission systems fails, the supply to the customer can still be supported by the other generators from the rest of the transmission systems.
- 2. The reduces in the cost of cable[14]. Instead of connecting every offshore wind farm to onshore via transmission line directly, it is normally economical and beneficial to connect the wind farms that are close together with each other and connect onshore with a single transmission line.
- 3. The reduces in the variability of offshore wind farms[15]. The power output of wind farms depend on the wind, which has large variation in speed. By connecting numerous wind farms from different regions to form a grid, the variation of power output from the grid would be reduced.

The development of such an offshore grid is going to start with the interconnection of the offshore wind farms to shore. Offshore wind farms can be integrated in two ways[15].

- 1. Wind farm hubs: Offshore wind farms can be connected at a site close to each other and the joint connection is connected to shore with one transmission line.
- 2. Tee in connection: An offshore wind farm or hub can be connected to an existing HVDC transmission line or interconnection.

2.3 High Voltage Direct Current (HVDC) Transmission

High Voltage Direct Current Transmission is a bulk electrical power transmission system using Direct Current in contrast with Alternative Current. The choice between the two has been debated since the 19^{th} century. Since HVDC is used in offshore power transmission and will play an important part in offshore network, this section will discuss the advantages of HVDC in offshore applications.

2.3.1 DC vs AC transmission

The first commercial electricity network was built in September 1882 by Thomas Edison at the Pearl Street station using 110V DC voltage for bulb lighting[16]. The commercial success created an increasing demand for electric power consumption. A great problem was that the power was difficult to deliver to customers far from the generations because of the high power loss in the transmission lines. In modern power transmission systems the voltages are shifted to a high level to reduce the current and therefore the loss in the transmission lines. Also, there were industrial demand for higher voltage rather than 110V used for bulb. During this period the technology did not exist to scale DC voltages.

The problem of long distance electrical power transmission was solved by AC transmission systems after the introduction of the transformer. Since transformers made it practical to scale to high voltages for transmission over long distances, AC became dominant in power transmission system[17].

With the development of modern power electronics, AC/DC conversion and DC voltage scaling is achievable. The advantages of HVDC transmission compared to HVAC transmissions are as follows:

- 1. Requires less conductor per unit distance. This is because direct current transmission does not need three phases and there is no skin effect in DC transmission lines.
- 2. Only real power is transmitted. AC transmission lines delivers apparent power while DC transmission lines only transfer real power.
- 3. No cable charging current. Capacitance exists between transmission cables. In long distance cables, especially in underwater applications where the capacitance per unit distance is large. An AC system often requires additional current to charge and discharge the cable. However in a DC system the cable is only charged once when system is initialised and during transients.

As a result, it is normally more economical and efficient to construct HVDC for long distance high power transmission lines. A comparison between a thyristor based HVDC system and an HVAC system is shown in Figure 2.3[18].



Figure 2.3: Cost of AC vs DC transmission systems against distance

Compared with the AC transmission system, the initial cost of an HVDC DC/AC converter station is higher than an AC transformer station. But the cost of the converter station does not rise with the distance. Because the cost for HVDC transmission line is lower than that for HVAC as discussed before, the total cost without considering the loss for HVDC increases slower than HVAC. As a result, a break point exists beyond which the total cost for an HVDC system is the most economical.

The break point is the distance that HVDC transmission becomes equally expensive to HVAC. The distance is dependent on several factors of the HVDC system, such as the technology utilised in construction, local policy, labour price and the transmission medium.

2.3.2 HVDC configurations

HVDC grids can be developed with monopole or bipolar configurations of HVDC transmission systems. The configurations are discussed in details as follows.

1. Asymmetric monopole with earth return is shown in Figure 2.4[19]. The two converter stations are connected with a single conductor. The current flows from the converter station with higher voltage to the one with lower voltage through the conductor and back to the high voltage one through the earth. The advantage of this configuration is that it requires less conductors. However, in offshore applications it is often unacceptable. This is because the ground current flow is not directional and restricted in the space, it causes negative impact on the environment and other human activities. Firstly, the underwater electrodes ionise the sea water and change the local marine chemistry. Secondly, the electromagnetic field that is generated by the current and leaks to the space affects the navigation systems of ships and aircraft. Therefore this configuration is not considered feasible in offshore applications.



Figure 2.4: Asymmetric monopole configuration with earth return

2. Asymmetric monopole with metallic return is developed from the asymmetric monopole with earth return by adding a metallic return conductor as shown in Figure 2.5[19]. This configuration is a feasible substitution of the earth return because it eliminates the problems of marine chemistry and electromagnetic field interference. As the terminal converters are connected to the ground of metallic return conductor, the voltage potential of the return conductor is much lower. Therefore the insulation design for the return conductor is not needed to meet the full requirement of the high voltage one. In addition, this configuration can be built for further expansion to bipolar transmission system.



Figure 2.5: Asymmetric monopole configuration with metallic return

3. Symmetric monopole is widely used in VSC (Voltage Source Converter) HVDC systems (although in LCC (Line commutated converter) HVDC some applications can still be found such as the NorNed interconnection [20]). In this configuration, the terminal converters are connected to two cables with half the HVDC link voltage but opposite polarity as shown in Figure 2.6[19]. There are different ways to provide the ground reference such as connecting the mid-point of DC link capacitors and there is no earth current under normal operating conditions. Although both conductors carry power, under normal operational conditions they do not operate independently, whist under fault conditions the unfaulted conductor is able to operate as an asymmetric monopole with earth return at a reduced power rating.



Figure 2.6: Symmetric monopole configuration

4. **Bipolar** can be extended from asymmetric monopole configurations. A typical topology of the configuration with earth return is shown in Figure 2.7[19]. Compared with monopole systems, bipolar systems are able to transfer double the power. Although the voltage level of the conductors are the similar but with opposite polarity, they are able to operate independently with different power rating. A metallic conductor with low voltage level can be added to connect the two grounds from different terminal converter stations to expand to a promising configuration in further offshore HVDC networks.



Figure 2.7: Bipolar configuration

2.3.3 Interfacing Symmetric monopole configuration with Bipolar configuration

The future HVDC grid will be most likely to face the problem of interfacing grids with variant voltage levels[19]. Based on previous discussion, further offshore HVDC networks would be a mix of symmetric monopole and bipolar configurations. Therefore, interfacing two HVDC grids with different configurations would be an inevitable requirement.

A topology for interfacing the metallic return bipolar configuration with a symmetric monopole configuration is shown in Figure 2.8[19]. Asymmetric monopole configurations can be connected to bipolar system directly because bipolar systems are developed from the extension of single asymmetric systems. This topology has problems when interfacing symmetric monopole because the monopole side requires balanced DC current while the bipo-

lar side does not. If the DC current in the conductors are unbalanced, the monopole side is not able to adjust the current. In this case, there will be a ground current between the mid-points of each system through the earth, which will cause the same problems in monopole configuration with earth return as discussed earlier. Therefore, a symmetric monopole system cannot be connected to a bipolar system directly and a DC/DC converter is required as an interface.



Figure 2.8: An interface betteen bipolar and monopole HVDC configurations

2.4 A proposed HVDC offshore network (Cigré benchmark)

Meshed HVDC grids have recently gained interest from academic communities and industry. In order to organise the discussion among the groups and facilitate to compare the results of the research of HVDC networks on the same basis, Cigré (Fr: Conseil International des Grands Réseaux Électriques, En: International Council on Large Electric Systems) proposed a VSC based DC grid as shown in Figure 2.9[21]. The complete system is composed of :

- 2 onshore AC systems
 - System A (A0 and A1)
 - System B (B0, B1, B2 and B3)
- 4 offshore AC systems
 - System C (C1 and C2)

- System D (D1)
- System E (E1)
- System F (F1)
- 2 DC nodes without connections to AC
 - B4
 - B5
- 3 VSC HVDC systems
 - DCS1 (A1 and C1)
 - DCS2 (B2, B3 and B5, F1 and E1)
 - DCS3 (A1, C2, D1, E1, B1, B4 and B2)



Figure 2.9: The Cigré B4 DC grid test system

The DC Grid Test System (DCGTS) consists of three grids, which are DCS1, DCS2 and DCS3. DCS1 and DCS2 are symmetric monopole systems while DCS3 is a bipolar system. DCS1 is not integrated to other systems, while DCS2 is interfaced to DCS3 at Cd-E1 with a DC/DC converter station. All of the three HVDC systems are based on VSC technology and can operate independently. The operational frame for the HVDC systems has an upper limit of 1.05pu and a lower limit of 0.95pu. Table 2.2 shows the different voltages of the sub-systems (AC onshore systems, AC offshore systems, HVDC symmetric monopole systems and HVDC bipolar systems) and Table 2.3 shows the power rating of each AC bus. Onshore AC busses are called "Ba", offshore AC busses "Bo", symmetric monopole DC busses "Bm", bipole DC busses "Bb", monopole AC-DC converter stations "Cm", bipole AC-DC converter stations "Cb" and DC-DC converter stations "Cd".

Table 2.2: The voltages of the different sub-systems in 2.9

System	Voltage (kV)
AC onshore	380
AC offshore	145
DC sym. monopole	± 200
DC bipolar	± 400

Table 2.3: The Power of AC buses (-: generation, +: load)

Bus	Bus type	Power (MW)
Ba-A0	Slack Bus	-
Ba-A1	PQ	-1000
Ba-B0	Slack Bus	-
Ba-B1	PQ	1200
Ba-B2	PQ	1300
Ba-B3	PQ	900
Bo-C1	PQ	-500
Bo-C2	PQ	-500
Bo-D1	PQ	-1000
Bo-E1	PQ	100
Bo-F1	PQ	-500

In the DCGTS, there are two DC/DC converters, which are Cd-E1 and Cd-B1. The main purpose of Cd-B1 is to control the power flow and block the fault in the DCS3 system. The functionalities of Cd-E1 are listed as follows.

- 1. To interfacing HVDC grids with different configurations. Firstly, the voltage level of DCS3 (400kV) is double that of a monopole system (200kV). Secondly, as is discussed in the previous section, there are problems to interface monopole symmetric systems with bipolar systems directly. Therefore a DC/DC converter station is required to interface the two different configurations.
- 2. To disconnect DCS2 and DCS3. It is highly costly to construct a DC breaker to block HVDC fault[22][23][24], so the DC/DC converter should function as a breaker in case there is a need to disconnect the grids. It is also mentioned in Cd-E1 is able to disconnect DCS2 from DCS3 if required in normal operation[21].
- 3. For power flow control. The requirements of power flow control for Cd-E1 is listed as follows:
 - Power rating: 1000MW
 - Operation mode setpoint: 300MW

Therefore Cd-E1 is supposed to be designed with a rated power of 2000MW while the power transmitted should be controlled at 300MW.

As is discussed in the previous section, interfacing bipolar and monopole HVDC configurations is an important problem in offshore HVDC grids and the DC/DC converter Cd-E1 is a solution to this problem. Because the research of fault block capability of Cd-E1 is dependent on the MMC converter and much research has been done in this area, the design and the power flow control of Cd-E1 is the main interest of this thesis.

2.5 Conclusions

This chapter first introduced the benefits of offshore wind farm and the growing trend of application. Then current offshore HVDC transmission systems discussed plays an important role in long distance offshore power transmission and offshore wind farm integration. After that future offshore HVDC grid and the Cigré B4 The DC Grid Test System (DCGTS) is introduced. As the conclusion to this chapter, the need for an DC/DC converter to interface different HVDC configurations as shown in Figure 2.9 is summarised, in which the converter station is labelled Cd-E1. In order to find a proper topology to meet the requirement for Cd-E1, different converter topologies will be investigated and compared in the next chapter.

Chapter 3

Topologies for DC/DC converters for Cd-E1 in Cigré benchmark system

3.1 Introduction

In the consideration of the functionalities of Cd-E1 in the Cigré benchmark as discussed in the previous chapter, a general structure of Cd-E1 is given in Figure 3.1. It consists of two unity ratio DC/DC converter stations, which are serial-connected at the bipolar side and parallel-connected at the monopole side and are able to operate independently. This general structure is chosen for Cd-E1 for the following reasons:

- 1. The two ports of the bipolar side can be operated as an asymmetric mode and the monopole side is symmetric.
- 2. The power flow can be managed by controlling the power flow of each DC/DC converter.
- 3. The fault at one of the ports of the bipolar side can be blocked by disconnecting the DC/DC converter at that port.

This chapter will aim to find out a proper topology of DC/DC converter for the upper and lower converter. It will start with the discussion of galvanic



Figure 3.1: General structure of Cd-E1. The upper and lower converters are serial-connected at the bipolar side and parallel-connected at the monopole side

isolation and structures of basic DC/DC converters to determine the design requirements for the DC/DC converters. Then Dual Active Bridge (DAB) based topology will be discussed to draw a conclusion that the centralised transformer based DAB is suitable. Since the topology of DAB is comprised of power electronic converters (DC/AC converters) and transformers, different topologies of transformers and DC/AC converters will then be discussed to draw a conclusion that a DAB with MMC based DC/AC converters on both sides and a centralised transformer in the middle is a suitable topology for the DC/DC converters of Cd-E1.

3.2 Brief discussion of galvanic isolation

Galvanic isolation is a principle of isolating functional sections of electrical systems to prevent current flow; no direct conduction path is permitted[25]. In power electronic converters it is normally implemented with a transformer, through which energy is transmitted via magnetic field rather than direct current path. The unwanted current path is then prevented. However, intro-
ducing transformers into the topology will greatly increase the cost and the complexity of the system, so it is necessary to discuss if it is compulsory to use transformers.



Figure 3.2: A topology of DC/DC converter without galvanic isolation.

Assume there is no galvanic isolation in either upper or lower converter station of Figure 3.1, then one possible topology of DC/DC converter for the upper or lower converter is shown in Figure 3.2, which consists of two DC/AC converters A and B and limb inductances L_1 and L_2 . Assuming that $V_{DC1} > V_{DC2}$, there are two possible closed current paths from V_{DC1} to V_{DC2} as follows:

- QB1 is on: $+V_{DC_1} \longrightarrow i_{C_{A1}} \longrightarrow GND \longrightarrow Ground current \longrightarrow i_{C_{B1}} \longrightarrow +V_{DC_2} \longrightarrow Current Path 1 \longrightarrow +V_{DC_1}$
- QB3 is on: $+V_{DC_1} \longrightarrow i_{C_{A1}} \longrightarrow GND \longrightarrow Ground current \longrightarrow i_{C_{B1}} \longrightarrow +V_{DC_2} \longrightarrow Current Path 2 \longrightarrow +V_{DC_1}$

It is obvious that the current paths always exists between $+V_{DC1}$ and $+V_{DC2}$ if converter B is modulated, which prevent the entire converter from operating normally. Therefore, galvanic isolation is a compulsory requirement for the design of DC/DC converters for the upper and lower converters of Cd-E1.

3.3 Topologies of DC/DC converters

3.3.1 Topologies of basic DC/DC converters

Basic DC/DC converters without a transformer applied in the circuit include the Buck converter, Fly-back converter, Boost converter and the others based on those such as two valve converter and Cùk converter. They are sufficient for some applications such as DC motor drives. However, due to the following reasons, the simple DC/DC converters cannot be applied in Cd-E1.

- 1. In these topologies one single semiconductor switch is connected to DC voltage source, which is the HVDC port if the topologies are applied. However one single or very small number of semiconductor devices cannot be applied at HVDC voltage and power levels of Cd-E1 ($\pm 400kV, 1000MW$) because of the low voltage and power rating of single devices.
- 2. These topologies are not able to extend to increase the rated voltage level and power level. Due to the fact that no single switching device can operate at HVDC voltage level, it is often practical to scale up a basic topology by connecting multiple switching devices in series or adding repetitive structures to increase the operating voltage and power level of the entire converter. More details about ways of scaling up a topology will be discussed in the next subsection but in preliminary, the basic topologies of DC/DC converters are not scalable.
- 3. Galvanic isolation is not provided. There are possible current paths between the input and output ports of the topologies.
- 4. These topologies do not have the bidirectional power flow capability.

Therefore, although basic DC/DC topologies are simple and has been proved reliable in many applications, they are not suitable for use as the topology of Cd-E1. It is also noted that besides the required functionalities and galvanic isolation, scalability is also an inevitable requirement.

3.3.2 DAB based topologies of DC/DC converters

According to the previous discussions, the upper and lower converters of converter station Cd-E1 in Cigré benchmark, which are also DC/DC converters, should have the following functionalities:

- 1. Unity voltage transfer ratio
- 2. Power flow control
- 3. To disconnect from one side to the other
- 4. Galvanic isolation
- 5. Scalability
- 6. Bidirectional power flow capability



Figure 3.3: General topology of (DAB) with transformer in the middle

A general topology of DAB is shown in Figure 3.3 will be considered. It consists of two DC/AC converters at the primary and secondary sides and a transformer in the middle, which acts as DC/AC/AC/DC. This topology was proposed in the early 1990s[26][27][28][29][30] but because of high semiconductor losses the applications were limited. With the development of modern magnetic material and power electronic switches, this topology became feasible for eliminating bulky and heavy LF transformers from power conversion systems[31][32][33]. The reasons for choosing DAB as the general topology of the DC/DC converters in Cd-E1 is shown as follows:

1. Galvanic isolation is provided. There is no direct current path from the bipolar side to the monopole side because the energy is transmitted by the transformer in the form of a magnetic field.

- 2. A mechanical breaker can be applied in the middle to disconnect the two ports.
- 3. Power flow control control is feasible. There are multiple control strategies to implement the power flow controller for DAB, which are discussed in [33]
- 4. Scalability is flexible. It will be discussed later that the DAB topology can be scaled up to cope with high voltage and high power applications.
- 5. Bidirectional power flow capability. The power flow can be controlled to both directions.

3.4 Scalability of DAB

A topology of single DAB will be scaled up to operate at HVDC applications. So the scalability of the topologies of DABs will be discussed in this section to find out a suitable topology of DAB. Depending on the structure of the transformer used in the DAB, there are three main types of DABs and will be discussed as follows.

3.4.1 Scalability of a distributed transformer based DAB

The DAB topology shown in Figure 3.4[34] can be cascaded connected to increase the voltage rating or power rating. The idea is from the project UNIFLEX in the University of Nottingham[34][35]. The scaled up structure of DC/DC converter is shown in Figure 3.5.

It is also possible to scale up a DAB with distributed transformers but with different connection on both sides. For example, an input-series-outputparallel topology is applied in [36] to achieve a high voltage transfer ratio. The advantages of this way of scaling up are as follows:

- 1. Each DAB module can be operated and controlled independently.
- 2. The frequency of AC voltage of the transformer can be increased to reduce the size, thereby the size of the entire system.



MF transformer

Figure 3.4: Dual Active Bridge DC/DC Converter with Medium Frequency Isolation



Figure 3.5: Scale up the DAB with disbtibuted transformer

There are two problems of this topology if scaling to the rated voltage of symmetric monopole HVDC system or each port of the bipolar HVDC system (400 kV):

Redundant transformer insulation

Consider the converters at the top and bottom of the topology shown in Figure 3.5, although the operating voltage at both sides of the transformer is much lower than the HVDC voltage, the phase voltages have a high DC voltage offset. Therefore the insulation design requirements of the transformer should meet the voltage offset. For example, the V_{DC_1} and V_{DC_2} are both 400kV and each DAB (the topology is the same as Figure 3.4) contributes 1kV. The voltage of the primary side and secondary side of the MF

transformer are shown as Equation 3.1.

$$v_{AC_1} = v_{AV_2} = 2\sin(\omega t)kV$$
 (3.1)

But the voltage potential of the ports of the transformer as shown in Figure 3.5 are shown as Equation 3.2, Equation 3.3, Equation 3.4 and Equation 3.5. It is obvious that although the operating voltage of each transformer is 2kV, the insulation design requirement for the transformer is 399kV

$$v_{a_1} = 399 + \sin(\omega t)kV$$
 (3.2)

$$v_{b_1} = 399 - \sin(\omega t)kV \tag{3.3}$$

$$v_{c_1} = 399 + \sin(\omega t)kV \tag{3.4}$$

$$v_{d_1} = 399 - \sin(\omega t)kV$$
 (3.5)

As a result, it would be a waste of insulation deployment and would take much space to install on an offshore platform.

Low fault robustness under DAB fault operation mode

Consider DC voltage distributed on both sides and a transformer ratio for each DAB is 1. If a short circuit fault occurred at the secondary side of DAB_1 , Then the DC voltage of from DAB_2 to DAB_N at the secondary side increases. As a result the primary side converters will not operate normally.

3.4.2 Scalability of a multi-winding transformer based DAB

Multi-winding transformers are adopted in many power electronic systems for transferring energy between multiple ports[37]. The idea of multi-winding transformer based DAB is from [38][39][40], where a structure of multiwinding medium frequency transformer isolation unit is applied as shown in Figure 3.6[38]. The AC sides of multiple DC/AC converters are coupled by the multi-winding transformer in the middle. The ports at one side can



Figure 3.6: A structure of multi-winding medium frequency transformer isolation unit



Figure 3.7: Scale up a DAB with a multiwinding transformer

be connected in serial to operate as one port to achieve a high voltage rating as shown in [41] are illustrated in Figure 3.7.

The main problem of this topology is the low reliability of the transformer. Consider a short circuit fault occurred on one of the coils. The short circuit current in that coil would increase the flux in the core of that coil to saturation. Then the transformer would fail. The probability of fault would be much higher if scaled up to HVDC voltage level. In order to scale up to 400kV, a large number of coils should be applied. Consider the probability of a fault in each port is p_0 , the number of coils is n, then the probability of a fault in one of the coils is $p = 1 - (1 - p_0)^n$. Because p_0 is smaller than 1, as n increases, p would increase and tend to 1. Therefore this topology works if the number of ports is small but is not reliable when scaled up with a large number of coils.

3.4.3 Scalability of a centralised transformer based DAB

Another approach to achieving a DC to DC conversion is the "front-to-front" connection of two AC/DC Voltage Source Converters (Voltage Sourced Converter (VSC)) forming an internal AC-link[42] and the topology was proposed in [43] as shown in Figure 3.8.



Figure 3.8: Front-to-front connection of two DC/AC VSCs for the DC/DC converters of Cd-E1.

Consider the case where the power electronic converter is scalable. The topology can be then scaled up by replacing the intermediate transformer with a high voltage, high power transformer and expanding the converter as shown in Figure 3.9.



Figure 3.9: Scale up a DAB with centralised transformer

Compared with the previous two methods, a centralised transformer would be more feasible. This is because:

- 1. Two-port high voltage and high power transformer is less challenging than multi-port in manufacturing.
- 2. A transformer with a single port on both sides is more reliable than the one with multiple ports.
- 3. Redundant insulation is not required.

Therefore, a centralised transformer based DC/DC topology (Front-to-Front topology) could be considered for the Cd-E1 converter station. However, the Cd-E1 has two ports at the bipolar side and single port at the monopole side. In the next section the structure of Cd-E1 will be discussed.

3.5 Discussion of topologies of the power electronic converters in the High voltage High power DAB

This section will compare different topologies of power electronics converters to find the suitable one for the DABs of DC/DC converters of Cd-E1.

3.5.1 Serial connected IGBT converters

H-bridge DC/AC converter can be scaled up by using multiple switching devices connected in series. Assuming N device are deployed in every phase and each device operates at voltage E, then theoretically the converter is able to operate at a DC link voltage of NE/2.

1. A Large number of redundant devices are required to increase the reliability. The redundant devices must be incorporated to increase the reliability by using more serial-connected devices (assuming it fails short circuit mode) and more parallel-connected devices (assuming it fails open circuit mode).



Figure 3.10: Serial connected IGBT DC/AC converter based DAB

- 2. High technical requirements to switch multiple semiconductors at the same time. During switching devices connected in series share different voltages and those connected in parallel share different current due to variations in switching speed. A device failure is possible to occur in the devices that share voltage or current higher than the rated values.
- 3. High switching loss. Conventional two level VSC requires large number of semiconductor devices to be connected in series in each valve. For high voltage operation they require high switching frequency which leads to high conversion losses [44].
- 4. Poor power quality. Due to the 2-level modulation technique, the amplitudes of PWM pulses of the DC/AC converters at each side are $\frac{V_{DC_A}}{2}$ and $\frac{V_{DC_B}}{2}$. So the amplitude of Pulse Width Modulation (PWM) harmonic is very high and the output power quality would be very poor.

Compared with the conventional serial-connected-IGBT VSC, multilevel converter like Neutral Point Clamped converter (NPC), Flying capacitor converter, cascaded H-Bridge converter (CHB) and MMC achieve better performance[44]. Because it is accepted that CHB requires large number of separate DC sources for power transmission[45], it will not be discussed further here.

3.5.2 The Neutral Point Clamped converter (NPC)

A typical single phase 5-level diode clamped circuit based DAB is shown in Figure 3.11. The gate drive logic signal for Q'_n is the inverse of Q_n . The relationship between gate drive logic signal for Q_n and output phase voltage is shown in Table 3.1.



Figure 3.11: NPC based DAB

Table 3.1: The relationship between gate drive logic signal for Q_n and output phase voltage (1 is on and 0 is off).

$Q_1 Q_2 Q_3 Q_4$	V_{AO}
1111	+2E
0111	+E
0011	0
0001	-E
0000	-2E

This topology can be scaled up by increasing the number of IGBTs and diodes in each arm. However, the disadvantages are as follows:

- 1. Excessive clamping diodes are required when the number of levels is high. It can be calculated that an M-level inverter leg requires M-1 storage capacitors, 2(M-1) switches and (M-1)(M-2) clamped diodes[46].
- 2. It is difficult to control the real power flow for balancing the neutral point potential [47].

3.5.3 Flying capacitor converter



Figure 3.12: Flying capacitor DC/AC multilevel converter based DAB

A typical single phase 5-level flying capacitor circuit based SST is shown Figure 3.12. The relationship between the gate drive logic signals for each switch and output voltage is shown in Table 3.2.

The disadvantage of this topology are:

1. Flying capacitor converter with more than 3 levels requires large number of clamping capacitors, which rate at different voltage level[48].

$Q_1 Q_2 Q_3 Q_4$	V_{out}	$Q_1 Q_2 Q_3 Q_4$	Vout
1111	+2E	0111	0
1110	+E	0110	+E
1101	+E	0101	0
1100	0	0100	-E
1011	+E	0011	0
1010	0	0010	-E
1001	0	0001	-E
1000	-E	0000	-2E

Table 3.2: The relationship between gate drive logic signal for Q_n and output phase voltage (1 is on and 0 is off).

2. Practical Applications of flying capacitor converters have shown the difficulty of maintaining the voltage balance of the DC link capacitors as the number of voltage level increases[48].

3.5.4 Modular Multilevel Converter (MMC)

The MMC was proposed in 2003 by Marquardt for high voltage applications [49]. The MMC-DAB is described in Figure 3.13 and the structure of each sub-module is half-bridge as described in Figure 3.14. The potential capabilities are as follows:

- 1. Scalable to different voltage level. The rated DC link voltage can be shifted by increasing the average number of inserted sub-modules.
- 2. Balanced voltage distribution. If the submodules in each arm are well balanced by the rotating algorithm, each submodule shares the same voltage[50].
- 3. Easy to add redundancy. Extra numbers of sub-modules can be added to each arm without changing the structure of the rest of the circuit.
- 4. High reliability.
 - (a) Failure bypass. If failures occur in one or more than one submodules, once the failures are detected those sub-modules can be bypassed by the capacitor balancing algorithm and also be bypassed physically.



Figure 3.13: Single phase MMC based DAB

- (b) Asynchonous switching among sub-modules. During switching, the highest voltage the IGBTs in each sub-module blocks is the capacitor's voltage, which is designed to be at a safe value.
- 5. Low requirement for cable-side filter. The circulating currents are smooth and can be controlled by the converter[51]. Therefore there is no need to deploy DC link capacitors or filters for the converter.

Since the applications of CHB, NPC and flying capacitor are limited by the disadvantages as discussed in this section, the MMC is the most suitable topology for Ultra High Voltage (UHV) and Very High Voltage (VHV) applications, which would be considered as the chosen topology for the DAB of the Cd-E1.



Figure 3.14: The structure of each submodule of the MMC

3.6 Conclusions

This chapter discussed the choices of the structure of Cd-E1, the topology of the transformer and converter. The analysis of the topologies are summarised in the following steps:

- 1. The topology of the DC/DC converters of Cd-E1 is DAB-based structure.
- 2. Centralised transformer based structure is chosen to be applied in Cd-E1.
- 3. MMC is chosen as the power electronic converters of the DABs in Cd-E1.

Therefore, an MMC based DAB would be chosen as the topology for the DC/DC converters of Cd-E1 and it is shown in Figure 3.15. The number of phases and the design of the transformer and MMC will be discussed in chapter 4.



Figure 3.15: The chosen topology of the converter station Cd-E1 in Cigré benchmark

Chapter 4

Design of MMC based DC/DC converter for Cd-E1

4.1 Introduction

As it was discussed in the previous chapters, an MMC-based DAB is chosen to be the structure of the Cd-E1 DC/DC converter. In order to calculate the parameters for Cd-E1, which will be used to design the controllers, an analysis of the transformer and the MMC should be considered. This chapter will start with the analysis of the transformer with a design procedure and optimisation of the geometric design to minimise the transformer loss. After that, the dynamic modelling and steady-state Fourier analysis are discussed to design the parameters of MMC.

4.2 Analysis and design of the Transformer

The structure of an DAB such as the number of phases and some parameters such as operating frequency are decided in the design of the transformer. The design requirement for the transformer are listed as follows:

1. Peak input and output voltages of the windings are both 400kV (unity ratio).

- 2. Peak power transmission is 500MW
- 3. Single phase windings
- 4. Sinsoidal winding currents and voltages

This section will introduce the methodology of transformer design and design the transformers of the DC/DC converters in Cd-E1. The procedure and optimisation for geometric design are shown in Figure 4.1. The design procedure will start with selection of the shape of core and the design of winding, which are decided by the rated current and voltage. The next step is the design of the core. Optimisation of geometric design of the winding and the core will also be discussed.

4.2.1 The Analysis of Winding

There are several issues in winding design, which are listed as follows:

- 1. The Core Sectional Area (CSA) of primary and secondary winding conductors
- 2. The shape of the winding conductor
- 3. The structure of the windings
- 4. Insulation requirements

The sectional area of the conductor A_{con} is calculated by Equation 4.1.

$$A_{con} = \frac{i_{max}}{J_{max}} \tag{4.1}$$

, where i_{max} is the peak current of the windings and J_{max} is peak current density in the windings. J_{max} is consided to be between $10A/mm^2$ and $15A/mm^2$ according to the requirement of using an Oil Natural Air Natural (ONAN) transformer cooling system[52]. A typical structure of an ONAN system is shown in Figure 4.2 which is redrawn from [53]. The insulation liquid (conventional insulation liquid is mineral oil but there are modern



Figure 4.1: The flow chart of transformer design procedure



Figure 4.2: Oil-immersed transformer cooling system¹

products for alternatives) is circulated from the tank, through the coils to the radiator.

The insulation liquid has two functions:

- 1. Dielectric insulation
- 2. Extract the heat generated by the core and coil

The total nubmer of turns, N_{turns} , is calculated by Equation 4.2,

$$N_{turns} = \frac{v_{AC}}{v_{pt}} \tag{4.2}$$

where:

 $v_{AC}\,$ The peak voltage of the input or output voltage of the transformer

¹This figure is redrawn from [53]

 v_{pt} The induced voltage of each turn

Because the dielectric breakdown voltage of normal insulation fluid is 30kV/mm[54], the required distance between two conductors d_{ins} is calculated by Equation 4.3,

$$d_{ins} = \frac{v_{ins}}{30kV/mm} \tag{4.3}$$

where v_{ins} is the required breakdown voltage for the insulation medium.

Conductors are covered by insulation paper. Because the electric field in the paper should be lower than 1.6kV/mm [55] and the paper layer should not be too thick which influences the cooling efficiency, the distance between consecutive turns (voltage per-turn) is considered to be 0.3mm[56] and the corresponded v_{pt} is 300V.



Figure 4.4: Round conductor

The shape of the winding conductor in a power transformer is usually rectangular to reach a relatively high space utilisation efficiency [57]. Rectangular space can not be filled with a cylinder conductor as shown in Figure 4.3 because of the geometric characteristics. Therefore conductor strands covered with insulation paper as shown in Figure 4.4 are widely used for the single strands in power transformer.

The conductor should be divided into multiple strands due to manufacturing requirements and skin effects. Skin effect is the tendency of an AC current to become distributed within the conductor cross section such that the current density is the largest near the surface of the conductor. This effect causes the effective resistance to increase with frequency. Skin effect depth is defined as the distance from the surface that the current density decreases exponentially to 1/e and is calculated by Equation 4.4, where δ is the skin depth, ω is the angular speed, μ is the permeability of the conductor materiel and σ is the conductivity of the material. Either the thickness or the height of the rectangular conductor should not exceed twice the skin effect depth. In addition, the geometric parameter such as the A_{core} , thickness and height are also restricted by manufacturing[58].

$$\delta = \sqrt{\frac{2}{\omega\mu\sigma}} \tag{4.4}$$

The arrangement of windings

A typical structure for the windings is shown in Figure 4.5. The primary and secondary coils are separated by insulating barriers and cooling ducts[59]. The high voltage coil is placed in the inner and the low voltage coil is placed in the outer of the winding window. This is because it needs less copper. There are a higher number of turns in the high voltage windings and the length of outer coil winding is longer. If the high voltage coil is placed as outer coil, it will definitely cost more copper.

The layout of windings

Disc winding layout shown in Figure 4.7 will be considered as the structure of the winding. It involves a single strand or multiple strands of insulated conductors in a series of parallel discs of horizontal orientation. The discs are connected at either the inside or the outside as a crossover point. The distance between discs depends on the highest voltage difference between the



Figure 4.5: A structure of shell form transformer



Figure 4.6: A conductor strand with insulation $lapping^2$

turns in the discs. For example, if there are 10 turns in each disc and the voltage per-turn is 300V, the breakdown voltage of the insulation paper is 1.2kV/mm the distance between consecutive discs is $2 \times 300 \times 10 \div 1200 = 5mm$.

In addition to the insulation issues discussed above, the distance between primary and second windings d_{ps} is calculated by Equation 4.5.

$$d_{ps} = \frac{\max(v_p(t) - v_s(t))}{30kV/mm}$$
(4.5)

 $v_p(t)$ is the voltage of primary winding, $v_s(t)$ is the voltage of secondary winding, 30kV/mm is the breakdown voltage of the insulation liquid.

The distance between a winding and the core d_c is calculated by Equation 4.6.

$$d_c = \frac{\max(v_p(t))}{30kV/mm} \tag{4.6}$$

²Captured from [57]



Figure 4.7: Basic disc winding layout

v(t) is the voltage of the winding which should be insulated from the core. Because this is an unity ratio isolation transformer, $d_{ps} = 2d_c$.

The total number of turns of each winding is calculated by $ceiling(v_{peak}/v_{pt})$. v_{peak} is the peak votlage of the winding and v_{pt} is the voltage between two consecutive turns.

4.2.2 The analysis of the Core

The core of a medium frequency power transformer consists of ferrite or silicon steel laminations provide the magnetic path. The CSA should be large enough to avoid flux saturation. The saturated flux of ferrite core is around 0.5T and in practical the peak flux density is normally designed at 0.3T. Silicon steel is around $1.5T \sim 2.0T[60]$. According to the Equation 4.7[61], A_{core} is inversely proportional to the peak flux density. So the size of core would be quite large if a ferrite core is applied. Therefore in high voltage high power transformers silicon steel is more widely used.

$$A_{core}(f) = \frac{v_p}{k_f n_p f B_m} \tag{4.7}$$

where:



Figure 4.8: The structure of the core

- v_p The peak value of the high voltage side
- n_p the number of turns at the high votlage side
- k_f The waveform factor
- B_m The peak flux density

The latter analysis will consider the CSA as a function of operating frequency f. In order to minimise the total length of conductors, the central core is considered to be a cylinder and the radius r_{core} is calculated by Equation 4.8.

$$r_{core}(f) = \sqrt{\frac{A_{core}(f)}{\pi}}$$
(4.8)

3-phase transformer vs single phase transformer

It is widely accepted that the size of a 3 phase transformer is normally smaller than a single phase one, because there is flux cancellation in the magnetic path. However, since in practical very large transformers are difficult to be transported to the site, 3 phase arrangements are made from three single phase transformers. So in terms of the topology of DAB, a single phase transformer will be applied in the DABs of Cd-E1.

4.2.3 Optimum design with cost function

Efficiency and weight are the main important factors in transformer design. The idea of optimisation is a three-step procedure shown as following.

- 1. Define a cost function $p_{loss}(a, b, p, f)$, where
 - a The ratio between the width and the height of the conductor
 - \boldsymbol{b} the rational ratio between the number of turns per-disk and the number of disks
 - f Operating frequency
 - p The apparent power
- 2. Describe the cost function p_{loss} with the variables.
- 3. Find the minima of the cost function with a numerical approach written in a Mathmatica script. Design the transformer with the parameters set $\{a, b, p, f\}$

Hysteresis loss, P_{hys} , and eddy current loss, P_{eddy} , in the core and copper loss, P_{copper} , in the transformer windings are the main source of transformer loss. The calculations are derived from Equation 4.9 [62] 4.10[63] to Equation 4.11.

$$P_{hys} = \rho_{core} V_{core} K_h f^{\alpha} B_m{}^{\beta} (W)$$
(4.9)

$$P_{eddy} = \rho_{core} V_{core} K_e (f B_M)^2 (W)$$
(4.10)

$$P_{copper} = l_{con} \frac{\rho_{Cu}}{A_{con}} (W)$$
(4.11)

where

- ρ_{core} The density of the core
- ρ_{Cu} The resistivity of copper

- K_h Hysteresis constant
- K_e Eddy current constant
- V_{core} The volume of the core
 - α Index of frequency
- B_M Peak flux density
 - $\beta\,$ Core loss exponent
- l_{con} The length of the conductors
- A_{con} The sectional area of the conductor

 l_{con} and V_{core} are functions of width/height ratio of the conductor section, width/height ratio of the core section and the rated apparent power p and are calculated by Equations from Equation 4.12 to Equation 4.15



Figure 4.9: The coil of the transformer

$$w_{con}(a,p) = \sqrt{A_{con}(p)a} \tag{4.12}$$

$$h_{con}(a,p) = \sqrt{\frac{A_{con}(p)}{a}} \tag{4.13}$$

$$n_{turns}(b) = ceiling(\sqrt{\frac{N_{turns}}{b}})$$
(4.14)

$$n_{disks}(b) = ceiling(\frac{N_{turns}}{n_{turns}(b)})$$
(4.15)

where:

 w_{con} Width of the conductor

 h_{con} Height of the conductor

 n_{turns} Number of turns per disk

 n_{disks} Number of disks

- a width/height ratio of the conductor
- b width/height ratio of the core section

 N_{turns} Total number of turns of each winding as defined by Equation 4.2.

 A_{con} The sectional area of the conductor

The height of coil h_{coil} can be calculated by Equation 4.16.

$$h_{coil} = n_{disks} h_{con} \tag{4.16}$$

Then the size of the window shown in Figure 4.8 are calculated by Equation 4.17 and Equation 4.18.

$$w_w = 2(n_{turns} \times w_{con} + 4d_c + r_{core}) \tag{4.17}$$

$$h_w = 2d_c + n_{disks} \times h_{con} \tag{4.18}$$

The radius of the inner coil r_{coil_1} and outer coil r_{coil_2} are calculated by Equation 4.19 and Equation 4.20.

$$r_{coil_1} = r_{core} + d_c + \frac{w_{con}}{2} \tag{4.19}$$

$$r_{coil_2} = r_{core} + d_c + w_{con} + 2d_c + \frac{w_{con}}{2} = r_{core} + 3d_c + \frac{3w_{con}}{2}$$
 (4.20)

The total length of the conductors consists of outer coil conductor and inner coil conductor. It is defined by Equation 4.21.

$$l_{con} = l_{con_1} + l_{con_2} \tag{4.21}$$

where

$$l_{con_1} = 2\pi \left(r_{core} + d_c + \frac{w_{con}n_{turns}}{2}\right) N_{turns}$$

$$(4.22)$$

$$l_{con_2} = 2\pi (r_{core} + 3d_c + \frac{3w_{con}n_{turns}}{2})N_{turns}$$
(4.23)

Substitute Equation 4.22 and 4.23 to Equation 4.21, the total length of the conductor is calculated from Equation 4.24.

$$l_{con} = 2\pi N_{turns} (r_{core} + d_c + \frac{w_{con} n_{turns}}{2} + r_{core} + 3d_c + \frac{3w_{con} n_{turns}}{2})$$
(4.24)
= $4\pi N_{turns} (r_{core} + 2d_c + w_{con} n_{turns})$



Figure 4.10: The core and related parameters

The parameters related to the design of the core are shown in Figure 4.10, where

 h_w The height of the transformer window

- w_w The width of the transformer window
- r_{core} The radius of the central cyclinder of the core
- t_{core} The thickness of the core

Because the core is symmetric, the flux through the central cyclinder is twice the flux of the other parts of the core. So the CSA of the other parts is $A_{core}/2$. The thickness of the core t_{core} can be calculated by Equation 4.25.

$$t_{core} = \frac{A_{core}}{2 \times 2r_{core}} = \frac{\pi r_{core}}{4} \tag{4.25}$$

The length of the magnetic path l_m is calculated by

$$l_m = 2 \times (2h_w + 2t_{core} + 2w_w + 2r_{core}) = 2(2h_w + 2w_w + 2r_{core} + \frac{\pi}{2}r_{core})$$
(4.26)

So the volume of the core V_{core} is calculated by Equation 4.27.

$$V_{core} = l_m \frac{A_{core}}{2}$$

$$= 2 \times \frac{A_{core}}{2} \times (2h_w + 2t_{core} + 2w_w + 2r_{core})$$

$$= A_{core} (2h_w + 2w_w + 2r_{core} + \frac{\pi}{2}r_{core})$$

$$(4.27)$$

The P_{core} and P_{copper} can be calculated by Equation 4.28 and 4.29.

$$P_{core} = (K_c f_\alpha B_m^\beta + K_e (f B_m)^2) \rho_{core} V_{core}$$
(4.28)

$$P_{copper} = \frac{\rho_{Cu} \times l_{con}}{A_{con}} \tag{4.29}$$

The core loss and copper loss described by Equation 4.28, 4.29, 4.27 and 4.24 can be expressed as functions of a, b, p, f, where

- a The ratio between the width and the height of the conductor
- $b\,$ The rational ratio between the number of turns per-disk and the number of disks

- p The transmitted apparent power
- f The operating frequency

In addition, the magnetising inductance L_m is calculated by Equation 4.30 [60]

$$L_m = \frac{n_{pr} n_{se} \mu A_{core}}{l_m} \tag{4.30}$$

where

- L_m The magnetising inductance
- n_{pr} The number of turns of the Primary winding
- n_{se} The number of turns of the secondary winding item[μ] The permeability of the core material
- l_m The length of the magnetising path

A computational script based on the equations and written in Mathematica is used to find the minima. The code is attached in Appendix A.

4.3 The Design of the Transformer of the DC/DC converters in Cd-E1

The design of the transformer should be investigated to decide the leakage inductance of the transformer and the optimum operating frequency. This is because:

- 1. The leakage inductance acts as the line-inductance between the two converters. In the discussion of control in the next chapter, the value influences the transient behaviour of the entire system.
- 2. There are complicated trade-offs between the copper loss and core loss, the total loss and the weight. If the operating frequency is low, the size of core will be larger so the length of the conductor will be longer, which

means the copper loss increases. On the other hand, if the operating frequency is high, the core will be smaller[64] but the core loss will be higher because according to Equation 4.9 and 4.10.

As it was discussed in the previous chapter, the design procedure of transformer is a iterative process of calculation and validation. However since it is not possible for the author to implement the transformer and transformer design is not the main topic of the thesis, the validation will only be processed in MagNet Finite Element Analysis (FEA) Tool and the values of power factor and leakage inductance of the feasible design will be applied.

The basic design parameters of the single phase transformers are listed in Table 4.1. Some variables are defined in Table 4.2 and will be applied in this section. The parameters about primary and secondary conductors are not distinguished because in this application the currents and voltages at both sides are the same.

Variables	Value	Description
v_{pr}	400kV	Primary side voltage amplitude
v_{se}	400kV	Secondary side voltage amplitude
P	500 MW	Rated power
η	99.0%	Expected efficiency
j_{peak}	$10A/mm^2$	peak current density
k_{f}	4.44	waveform factor (sinusoid waveform is 4.44)
B_m	1.2T	Peak flux density
k_i	0.0056186	Hysteresis loss factor
k_e	0.000139186	Eddy current loss factor
α	1.336	Index of frequency in hysteresis loss calculation
β	1.915	Index of peak flux density in hysisteresis loss calculation

Table 4.1: Basic parameters of each transformer

 v_{pr} and v_{se} are considered close to the peak value of DC link cables. P is the rated power of each HVDC port. The peak current density is decided by the cooling system as listed in [52]. k_i , k_e , α and β are the loss-related parameters of Non-Oriented Electrical Steel M-47 defined in MagNet library. In order to achieve the optimum efficiency, there are basically two design challenges:

1. Maximise the efficiency. Since the power rating of this transformer is 500MW, only 0.1% of loss would result in 500kW heat dissipation.

Table 4.2: New variables defined

Name	Description
A_{con}	Sectional area of conductors
a	Width/Height of wires
b	Width/Height of transformer core window
m	Number of disks the inner winding consists of
n_{disks}	Number of turns of each disks
n _{turns}	Total number of turns of each winding
A_{core}	Core sectional area

Therefore achievement of the maximum efficiency is the primary target of the design. Figure 4.11 is generated by the Mathematica script and it shows the maximum efficiency the design can achieve at different frequency. It is obvious that an optimum efficiency point exists. In high frequency region the efficiency drops because the core loss increases with the frequencies. In low frequency region the efficiency is also higher because the core sectional area has to be designed to be large to avoid flux saturation, as the result of which the total length of the conductors increases, thereby increases the copper loss. With the numerical approach the optimum operating frequency where the transformer achieves the highest efficiency is 250Hz.

- 2. Minimise the size of core. This converter station will be likely to be installed on an offshore platform, so there are constraints about the size and weight of transformer. An impractical design of size and weight would cause problems in installation. Since the weight of the transformer core would dominate the overall weight of converter station, it would be beneficial to have the transformer as light as possible. Similar with the calculation of efficiency, the calculation of weight with geometric design and frequency can only be processed with a numerical approach. Basically the size of core reduces at high operating frequency as shown in Figure 4.12. It is also shown that as the operating frequency increases, the weight difference between the design with the minimum weight and the design with the maximum efficiency decreases.
- 3. Minimise the leakage inductance. The leakage inductance constrains the maximum power transmitted by the converter, because it acts as a reactive power load inside the converter. It is influenced by the geometric design of the core window and the space between the coils and core. In this thesis the Infolytica MagNet FEA tool is used

to analyse the leakage inductance.



Efficiency of Transformer (Magnetic and copper loss considered) efficiency(%)

Figure 4.11: The maxmima efficiency of the transformer at different operating frequencies drawn in Mathematica

Therefore, it can be found that the optimum operating frequency is 252Hz. But there are two different geometric designs listed in Table 4.3, where Design 1 has the maximum efficiency at 252Hz while Design 2 has the lowest weight.

4.3.1 FEA analysis of the designs in Infolytica MagNet

A 2-D FEA analysis in Infolytica MagNet will be applied to choose one of the two designs because of the following two reasons:

1. Validate the feasibility of the designs. In the simulations the primary side of each transformer is connected to a AC current source with a frequency of 252Hz, while the secondary side is connected with a resistive load of 160Ω , so that there is only real power at the secondary side. Therefore the power factor of the transformer can be easily calculated by $pf = \frac{v_p}{v_s}$. The power factor of the transformers will be compared to find out the feasible design.



Figure 4.12: The maximum weight of the transformer at different frequencies drawn in Mathematica

	Design 1	Design 2
Efficiency (%)	99.56	99.51
Weight (tons)	18.3	13.4
Thickness of Wire (mm)	4.6	2.0
Width of Wire (mm)	54.4	122.5
Number of disks	667	667
Turns per disk	2	2
Magnetising Inductance L_m	175.3H	238.6H

Table 4.3: The efficiency and weight at 252Hz with different geometric design

2. Calculate the leakage inductance. Because the transformer will be modelled as Figure 4.13, The leakage impedance of the transformer R_p , L_p , L_M , L_s and R_s will be calculated and will be used in the control design in the next chapter.

The analysis is proceeded in the following procedure:

- 1. Draw the 2-D model of the transformer
- 2. Set the electrical connections of the transformer
- 3. Solve the model by Infolytica FEA tools

In the second step, the electrical connections of the transformer is shown in Figure 4.14. Although it is not logical to connect the coil to a current source



Figure 4.13: The transformer model in Electrical circuit



Figure 4.14: Electrical connections of the transformer

directly in a electrical circuit simulation software, in Infolytica MagNet the current of a coil can be set to a fixed function in this model.

FEA analysis of the Design 1 (With maxmimum efficiency)

The geometric parameters of the Design 1 are shown in Table 4.4. The

The heigth of the conductors	h_{con}	54.2mm
The width of the conductors	w_{con}	4.6mm
The height of the transformer window	h_w	4710mm
The width of the transformer window	w_w	270.2mm
The radius of the central cyclinder of the core	r_{core}	261mm
The distance between the core and the coils	d_c	13.3mm
The distance between coils	$2d_c$	26.6mm
The number of disks of each winding	n_{disks}	667
The number of turns per disk	n_{turns}	2

Table 4.4: Geometric parameters of the transformer design 1

distribution of peak flux density is shown in Figure 4.15. It is obvious that in the main magnetic path the peak flux density does not exceed 2T, which is the limit of the material. Therefore this design is acceptable.


Figure 4.15: FEA analysis of flux density distributation of the design with maximum efficiency $% \left({{{\mathbf{F}}_{\mathrm{s}}}^{\mathrm{T}}} \right)$



Figure 4.16: The current of the both sides of the transformer in Design 1

In the FEA analysis, the current of the primary winding is set to be $2500 \sin(2\pi \times 252t)$. The power factor angle θ is calculated by Equation 4.31

$$\cos(\theta) = \frac{P}{S} \tag{4.31}$$

where

- θ The power factor angle
- P The real power transmitted by the transformer
- S The apparent power input to the transformer

In order to calculate the real power P and the apparent power S in Equation 4.31, the secondary winding is connected to a resistive load so that there is only real power consumed in the secondary side load. Because the currents of the primary and secondary winding are both sinusoidal as shown in Figure 4.16.

The input apparent power is calculated by Equation 4.32

$$S_{in} = I_{pr} V_{pr} \tag{4.32}$$

where

- S_{in} The input apparent power
- $I_{pr}\;$ The RMS value of the input current, which is the current of the primary winding

 V_{pr} The RMS value of the voltage of the input port, which is the voltage of the primary winding

In the Electrical connection arrangement in Infolytica MagNet, the secondary winding is connected to a resistive load. Therefore the transmitted real power is calculated by Equation 4.33.

$$P_{out} = I_{se} V_{pr} \tag{4.33}$$

where

- P_{out} The output real power
 - I_{se} The RMS value of the output current, which is the current of the secondary winding
 - V_{se} The RMS value of the output voltage, which is the voltage of the load voltage

It can also be noted from Figure 4.16 that the waveforms of the primary and secondary windings are the same $(I_{pr} = I_{se})$, then the power factor $\cos(\theta)$ can be calculated by Equation 4.34.

$$\cos(\theta) = \frac{P_{out}}{S_{in}}$$

$$= \frac{V_{se}I_{se}}{V_{pr}I_{pr}}$$

$$= \frac{V_{se}}{V_{pr}}$$

$$= 0.925$$
(4.34)

In p.u. system, the system (voltage source - transformer - load) can be described by a equivalent circuit shown in Figure 4.17. The power factor of $X_L + R$ is 0.925. So the value of the reactance X_L is calculated by Equation 4.35 and this value will be used in the control design in Chapter 5.

$$X_{Lpu} = \tan(\arccos(\cos(\theta))) = 20\%$$
(4.35)



Figure 4.17: The equivalent circuit of the transformer in pu system

FEA analysis of the Design 2 (With minimum weight)

The Design 2 is developed from Design 1 with slight modifications to the geometric design. The geometeric parameters are listed in Table 4.5.

The heigth of the conductors	h_{con}	2mm
The width of the conductors	w_{con}	122mm
The height of the transformer window	h_w	2990 <i>mm</i>
The width of the transformer window	w_w	543mm
The radius of the central cyclinder of the core	r_{core}	261mm
The distance between the core and the coils	d_c	13.3mm
The distance between coils	$2d_c$	26.6mm
The number of disks of each winding	n_{disks}	667
The number of turns per disk	n_{turns}	2

Table 4.5: Geometric parameters of the transformer design 2

The FEA is preceded by the same way for Design 1. A 252Hz sinusoidal current is injected to the primary winding and the output current is the same as the input current as shown in Figure 4.18.

The main problem of this design is the that the flux density exceeds the saturated value in the main magnetic path as shown in Figure 4.19. This is because there is leakage flux through the coils. In theoretical analysis, the copper is to be considered as ideal conductor, where there is no magnetic field inside. However in FEA analysis, the copper is not considered as ideal conductor. So there is flux leakage through the coils. As a result of that, the leakage inductance is high.



Figure 4.18: Currents of both sides of the transformer in Design 2

The conclusion of the design of the transformer

Therefore the Design 1 the chosen as the most suitable design of the transformers applied in the DC/DC converters of Cd-E1.

4.4 The Analysis and Design of the MMC in the DC/DC converters of Cd-E1

The MMC is the DC/AC converter in the DC/DC converters of Cd-E1. In order to:

- 1. Develop a computational tool to design the MMC converters
- 2. Derive a linear time invariant model to design the controllers

This section will start with an introduction to the principle of the MMC. Then a dynamic model based on Ordinary Differential Equation (ODE) theory, Harmonic State Space (HSS) model based on the steady-state analysis and a Linear Time Invariant System (LTI) derived from regular perturbation theory will be discussed. Finally in this section a computational tool based in MATLAB will be developed to proceed the design.



Figure 4.19: FEA analysis of the flux density distributation of teh design with minimum weight

4.4.1 The structure and principle of MMC

A half-bridge single phase MMC DC/AC converter with a half-bridge in each submodule is shown in Figure 4.20. The operating algorithms are summarised in Figure 4.21.

The converter includes four functional modules. Since the control will be the topic of Chapter 5, the other functional modules are listed in the following.

Submodule operations

The operating signals are sent to each submodule to be inserted/bypassed. For half bridge submodules, a submodule can be inserted by switching on Q_1 and bypassed by switching on Q_2 . The summary of switching states of a submodule is shown in Table 4.6 [65].



Figure 4.20: The structure of MMC with one phase and single bridge sub-modules

Table 4.6: The summary of switching states of a cell

Q_1	Q_2	V_{sm}	Current direction	Power path	Capacitor States
on	off	V_{cu} or V_{cl}	$i_{sm} > 0$	D_1	Charging
on	off	V_{cu} or V_{cl}	$i_{sm} < 0$	Q_1	Discharging
off	on	0	$i_{sm} > 0$	Q_2	unchanged
off	on	0	$i_{sm} < 0$	D_2	unchanged



Figure 4.21: The operating algorithms of the MMC

Capacitor voltage balancing

Capacitor Voltage Balancing (CVB) is one of the important challenges for MMCs[66]. The capacitor voltages of the individual SMs must be monitored and equalised[67]. A simple method of CVB is proposed in [65] which requires no external reference voltages for the cell capacitor. A balancing method which is able to control the capacitor voltage of each individual submodule is proposed in [68]. Several balancing methods with reduced switching frequency were proposed in [69]. A predictive control strategy based capacitor voltage balancing method is presented in [70].



Figure 4.22: Block diagram of the CVB

According to the structure of the algorithm shown in Figure 4.21, the function of the algorithm is described in Figure 4.22. Therefore the requirements of the algorithm are as follows:

- 1. Fast sorting
- 2. No extra switching events

The algorithm of the CVB for one of the arms is shown in Figure 4.23 and the code of the algorithm is in Appendix B.

Nearest level modulation (NLM)

Many PWM techniques can be adopted for MMC such as Sinusoidal Pulse-Width Modulation (SPWM)[71][72]. However in large multilevel converter it could be a problem to apply a carrier wave for each output level since the phase displacement needed should be very little so that the requirement for the accuracy of the carrier wave generation is quite high[73]. A Nearest Level Modulation (NLM) technique is presented in [73] which applies no triangle



Figure 4.23: The flowchart of the CVB

carrier by directly computing the switching states and duty cycles for each phase of the converter. Therefore the NLM technique is applied in the MMCs of the Cd-E1 converter.

In general terms, the required pulse width can be described by Equation 4.36 [74].

$$W_{dutycycle} = \frac{1}{\Delta t} \int_{t_i}^{t+\Delta t} M \cos(\omega_0 t) dt$$
(4.36)

where

- $W_{dutycycle}$ The required pulse width
 - Δt The sampling period time
 - t_i The i_{th} sampling period

So the NLM for the upper and lower arm can be described by an operator $\mathcal{M}_{T_s}(d_i)$ defined in Equation 4.37.

$$\mathcal{M}_{T_s}(d_i) := \begin{cases} floor(d_i) & \text{if } d_i > d_{i-1} \text{and } 0 \le t < frac(d)T_s \\ & \text{if } d_i < d_{i-1} \text{and } frac(d)T_s \le t < Ts \\ ceiling(d_i) & \text{if } d_i > d_{i-1} \text{and } frac(d)T_s \le t < Ts \\ & \text{if } d_i < d_{i-1} \text{and } 0 \le t < frac(d)T_s \end{cases}$$
(4.37)

where:

 d_i The i^{th} required pulse width in percentage

 $floor(d_i)$ Returns the greatest integer which is less than d_i

 $ceiling(d_i)$ Returns the least integer which is greater than d_i

- $frac(d_i)$ Returns the fractional part of d_i
 - T_s The sampling period

4.4.2 The Dynamic model of the single phase MMC based on ODE theories

Dynamic model of the single phase MMC in Figure 4.20 is a precise mathematical approximation of the real model based on ODE theories. This model will be used to

- 1. Compute the transient behaviour of the MMC
- 2. Derive the HSS model to design the computation tool for MMC design
- 3. Derive the LTI model for the controller designs

A convenient phasor model of MMC with circulating current suppression control is proposed in [75]. However it deals with steady-state modelling and neglects all the dynamics [76]. In [76] it mentioned an dynamic model but it neglect the output current in the dynamic equations. An approximate model of three phase MMC presented in [77]. But it is modelled in three phase and it is not possible to derive a single phase model from it. Also, the conmutational results of the transient behaviour of the model does not fit the waveform of the simulation. A detailed model in [78] modelled the submodules without averaging the voltage of the capacitors. But this is based on replacing the capacitor with a constant voltage source serial connected with a resister. The results could be similar but the dynamical equations are different. Therefore it is not possible to derive a correct LTI model from it. A complicated ODE-based dynamic model is presented in [79], which is able to compute the dynamic behaviour. But the influence of the modulation reference signal is not explicit in the equation. So an LTI model cannot be able to be derived from it. Therefore, a simple but precise dynamic model should be developed.

In order to simplify the analysis, some assumptions should be made. These assumptions are as follows:

- 1. Only the fundamental component is considered in the PWM reference.
- 2. All the voltages of the submodule in the upper or lower arm are identical.
- 3. Losses are modelled by the inclusion of a serial arm resistance.

The state variables of the system are defined in Table 4.7.

Table 4.7: The state variables defined in the system

i_u	The current in the upper arm
i_l	The current in the lower arm
v_{cu}	The identical voltage of the capacitors in the upper arm
v_{cl}	The identical voltage of the capacitors in the lower arm

The modulation reference signal for the upper and lower arm are defined in Table 4.8.

Mathematical modelling

The dynamic model based on the state variable $[i_u, i_l, v_{cu}, v_{cl}]^T$ is Equation 4.38, Equation 4.39, Equation 4.40 and Equation 4.41. The detailed computation is in Appendix D.

$$\frac{di_{u}}{dt} = -\frac{1}{2} \left(\frac{R_{p}}{L_{p}} + \frac{2R_{load} + R_{p}}{2L_{load} + L_{p}} \right) i_{u} \\
+ \frac{1}{2} \left(\frac{2R_{load} + R_{p}}{2L_{load} + L_{p}} - \frac{R_{p}}{L_{p}} \right) i_{l} \\
- \frac{1}{2} \left(\frac{n_{u}(t)}{L_{p}} + \frac{n_{u}(t)}{2L_{load} + L_{p}} \right) v_{cu} \\
- \frac{1}{2} \left(\frac{n_{l}(t)}{L_{p}} - \frac{n_{l}(t)}{2L_{load} + L_{p}} \right) v_{cl} \\
+ \frac{1}{2} \left(\frac{V_{DC}}{L_{p}} + \frac{2}{2L_{load} + L_{p}} v_{load} \right)$$
(4.38)

Table 4.8: The modulation reference signals

n_u	The modulation reference signal for the upper arm
n_l	The modulation reference signal for the lower arm

$$\frac{di_{l}}{dt} = \frac{1}{2} \left(\frac{2R_{load} + R_{p}}{2L_{load} + L_{p}} - \frac{R_{p}}{L_{p}} \right) i_{u}
- \frac{1}{2} \left(\frac{R_{p}}{L_{p}} + \frac{2R_{load} + R_{p}}{2L_{load} + L_{p}} \right) i_{l}
- \frac{1}{2} \left(\frac{n_{u}(t)}{L_{p}} - \frac{n_{u}(t)}{2L_{load} + L_{p}} \right) v_{cu}
- \frac{1}{2} \left(\frac{n_{l}(t)}{L_{p}} + \frac{n_{l}(t)}{2L_{load} + L_{p}} \right) v_{cl}
+ \frac{1}{2} \left(\frac{V_{DC}}{L_{p}} - \frac{2}{2L_{load} + L_{p}} v_{load} \right)
\frac{dv_{cu}}{dt} = \frac{n_{u}(t)}{NC} i_{u}$$
(4.40)

$$\frac{dv_{cl}}{dt} = \frac{n_l(t)}{NC}i_l \tag{4.41}$$

Since the circulating current i_{cir} , output current i_{ac} and the average voltage of the capacitors in the MMC arm v_c are the outputs of the system, it would be helpful to transform the state variables $[i_u, i_l, v_{cu}, v_{cl}]^T$ to the new set of state variables $[i_{com}, i_{diff}, v_{com}, v_{diff}]^T$ defined by Equation 4.42, Equation 4.43, Equation 4.44 and Equation 4.45.

$$i_{com} := \frac{1}{2}(i_u + i_l) \tag{4.42}$$

$$i_{diff} := \frac{1}{2}(i_u - i_l) \tag{4.43}$$

$$v_{com} := \frac{1}{2}(v_{cu} + v_{cl}) \tag{4.44}$$

$$v_{diff} := := \frac{1}{2}(v_{cl} - v_{cu}) \tag{4.45}$$

where:

- i_{com} Common component of currents of upper and lower arm
- i_{diff} Differential component of the currents of upper and lower arm
- $v_{com}\,$ Common component of the identical voltages of capacitors of the upper and lower arm

 $v_{diff}\,$ Differential component of the identical voltages of capacitors of the upper and lower arm

The common and differential component of $n_u(t)$ and $n_l(t)$ are defined by Equation 4.46 and 4.47.

$$n_{com}(t) := \frac{1}{2}(n_u(t) + n_l(t)) \tag{4.46}$$

$$n_{diff}(t) := \frac{1}{2}(n_l(t) - n_u(t)) \tag{4.47}$$

where:

- $n_{com}(t)\,$ Common component of the modulation reference signals of the upper and lower arm
- $n_{diff}(t)$ Differential component of the modulation reference signals of the upper and lower arm

Then the dynamic model based on the new state variables $[i_{com}, i_{diff}, v_{com}, v_{diff}]^T$ is Equation 4.48 and the detailed computation is in Appendix D.

$$\frac{d}{dt} \begin{pmatrix} i_{com} \\ i_{diff} \\ v_{com} \\ v_{diff} \end{pmatrix} = \begin{pmatrix} -\frac{R_p}{L_p} & 0 & -\frac{n_{com}(t)}{L_p} & -\frac{n_{diff}(t)}{L_p} \\ 0 & -\frac{2R_{load} + R_p}{2L_{load} + L_p} & \frac{n_{diff}(t)}{2L_{load} + L_p} & \frac{n_{com}(t)}{2L_{load} + L_p} \\ \frac{n_{com}(t)}{NC} & -\frac{n_{diff}(t)}{NC} & 0 & 0 \\ \frac{n_{diff}(t)}{NC} & -\frac{n_{com}(t)}{NC} & 0 & 0 \end{pmatrix} + \begin{pmatrix} \frac{V_{DC}}{2L_p} \\ -\frac{v_{load}}{2L_{load} + L_p} \\ 0 \end{pmatrix}$$

$$(4.48)$$

Validation of the dynamic model with simulation and experimental rig

Since it was fortunate that in PEMC Group lab there was a three phase MMC DC/AC inverter, which was built for another project, it would be practical to validate the dynamic model Equation 4.48 with both a simulation model and the experimental rig.

The structure of the experimental rig is shown in Figure 4.24 and the parameters are shown in Table 4.9. The rig was a three phase inverter with a star-connected load. Each phase consists of 4 submodules in the upper and lower arm.

R_p	2.7Ω	ω	$100\pi rad/s$
L_p	2mH	n_{com}	2
R_{load}	57.6Ω	n_{diff}	$1.44\cos(\omega t)$
L _{load}	9mH	V_{DC}	300V
NC	$1200\mu F$	v_{load}	0
f_{sw}	1kHz		

Table 4.9: The parameters of the experimental rig

Since in practical situations, there are voltage drops across the semiconductors, the waveforms of a low voltage multilevel converter are normally distort, a PLECS simulation model is built to validate the dynamic model as shown in Figure 4.24.

The waveforms of the state variables of the dynamic model are calculated by Mathematica with a numerical computational algorithm. The Mathematica codes for the computation are presented in Appendix D. In addition, the results of the simulation and the experiment are imported in to the script and plotted.

The captured waveforms of the state variables and the waveforms of the simulations are shown in Figure 4.26, Figure 4.27, 4.28 and 4.29.

It is obvious that the difference between the waveforms of the dynamic model and the simulation model and the difference between the waveforms of i_{diff} and v_{diff} of the dynamic model, simulation results and the experimental rig are small. It implies that the dynamic model precisely describes the simulation model. However, the differences between the i_{com} and v_{com} of the dynamic model and experimental rig is larger. This is because noise is



Figure 4.24: The structure of the experimental rig







Figure 4.26: The waveforms of i_{com}



Figure 4.27: The waveforms of i_{diff}



Figure 4.28: The waveforms of v_{com}



Figure 4.29: The waveforms of v_{diff}

introduced into the converter, which is caused by that the semiconductors are not ideal in the experimental rig.

4.4.3 The Harmonic State Space (HSS) Model the single phase MMC

Although the dynamic model Equation 4.48 describes the transient behaviour of the single phase MMC converter on a precise base, it is a general Linear Time Varying System (LTV) ODE. For any initial value problem this equation does not have a explicit analytical solution. A general averaging method of LTV systems is presented in [80], which is based on describing function method. Several LTI-based methods, such as state-space averaging (SSAV) and DQ domain (DQ) are feasible in control design but not enough to analyse the complex behaviour of LTV systems[81].

The requirements for the model that is used to design the parameters are summarised as follows:

- 1. Estimate the steady state behaviour
- 2. Be used to compute the parameters according to some design requirements

A Harmonic State Space (HSS) modelling method based on harmonic domain was proposed in [82]. This method was applied to analyse the harmonic intersections of three phase MMC[83] and the experimental result showed that the estimated waveform of the steady state is different but with very small error. Because the design requirements for the MMC converter are normally explicitly related to the state variable $[i_{com}, i_{diff}, v_{com}, v_{diff}]^T$. For example,

- The output AC current i_{AC} is $2i_{diff}$
- The average voltage of the voltages of the capacitors is the DC component of the v_{com}
- The ripple voltage os the capacitors is the magnitude of v_{diff}

In order to derive an impedance of MMC, a HSS modelling method for Equation 4.48 should be applied based on the dynamic model described by Equation 4.48.

Some assumptions are made to simplify the modelling:

- 1. The assumptions that are made for the dynamic model
- 2. The n_{diff} is periodic and the n_{syn} is constant
- 3. Only the fundamental components of i_{diff} is considered.

Analysis of stability

Because the HSS model is used to analyse the steady state of the dynamic model, the stability of the system should be investigated to ensure the existance of the steady state. In linear time invariant (LTI) systems the stability problem can be easily investigated by eigen value method. But for LTV systems this method is not available. Some stability problems of power electronic converters have been investigated in the Harmonic Domain in [81]. However, instead of a global picture, it only discusses the instability phenomena in the high frequency region and there should be no coupling in the system.

Actually the term **stability** is defined in [84] and the Lyapunov direct method can be used to show that the dynamic system is asymptomatically stable. A Lyapunov function F_L based on the space spanned by $[i_{com}i_{diff}v_{com}v_{diff}]^T$ is defined by Equation 4.49.

$$F_L(t) := \frac{1}{2}L_p i_{com}^2 + \frac{1}{2}(L_p + 2L_{load})i_{diff}^2 + \frac{1}{2}CNv_{com}^2 + \frac{1}{2}CNv_{diff}^2 \quad (4.49)$$

If $\frac{dF_L}{dt} < 0$, then the system is asymptomatically stable.

$$\frac{dF_L}{dt} = L_p i_{com} \frac{di_{com}}{dt} + (L_p + 2L_{load}) i_{diff} \frac{di_{diff}}{dt} + CNv_{com} \frac{dv_{com}}{dt} + CNv_{diff} \frac{dv_{diff}}{dt}$$
(4.50)



Figure 4.30: Phase plot of (i_{com}, i_{diff})

Substitute Equation 4.48 to Equation 4.50, it yields:

$$\frac{dF_L}{dt} = i_{com} \left(-R_p i_{com} - n_{com}(t) v_{com} - n_{diff}(t) v_{diff} + \frac{V_{DC}}{2} \right) \\
i_{diff} \left(-(2R_{load} + R_p) i_d iff + n_{diff}(t) v_{com} + n_{com}(t) v_{diff} - v_{load}) \\
+ v_{com} \left(n_{com}(t) i_{com} - n_{diff}(t) i_{diff} \right) + v_{diff} \left(n_{diff}(t) i_{com} - n_{com}(t) i_{diff} \right) \\
= -R_p i_{com}^2 - \left(2R_{load} + R_p \right) i_{diff}^2 + \frac{1}{2} V_{DC} i_{com} - v_{load} i_{diff} \\
= -R_p \left(i_{com} - \left(\frac{V_{DC}}{4R_p} \right) \right)^2 - \left(2R_{load} + R_p \right) \left(i_{diff} - \frac{v_{load}(t)}{2 \left(2R_{load} + R_p \right)} \right)^2 \\
+ \left(\frac{V_{DC}^2}{16R_p} + \frac{v_{load}(t)^2}{4 \left(2R_{load} + R_p \right)} \right)$$
(4.51)

Equation 4.51 implies a limit cycle in the phase plot as shown in Figure 4.30 by letting $\frac{dF_L}{dt} = 0$. The orbit is not a ellipse because $v_{load}(t)$ is a periodic function of time and the average value is 0. The shape of the orbit can be more complicated depending on the actual waveform of i_{com} and i_{diff} but it is still a closed bounded curve.

It is easy to show that this orbit is an attractor because:

- 1. if the state (i_{com}, i_{diff}) locates outside the area surrounded by the orbit, then $\frac{dF_L}{dt} < 0$. So the state will fall towards the origin
- 2. if the state (i_{com}, i_{diff}) locates inside the area surrounded by the orbit,

then $\frac{dF_L}{dt} > 0$. So the state will diverge.

3. if the state (i_{com}, i_{diff}) locates on the the orbit, then $\frac{dF_L}{dt} = 0$. So the state will travel along the orbit.

The state variable (i_{com}, i_{diff}) will converge to an orbit, which ensures $\frac{dF_L}{dt} = 0$. So the energy stored in the converter will converge to a bounded constant value or function. Therefore the system is asymptomatically stable.

The summary of the conclusions are as follows:

- 1. There is a limit cycle for the state variables (i_{com}, i_{diff}) and it is an attractor[85].
- 2. The dynamic system is globally asymptomatically stable.

The steady state behaviour

The previous analysis showed that the steady state behaviour of the MMC is stable and the state variable (i_{com}, i_{diff}) will form an stable closed orbit, however,

- 1. It does not show the orbits of v_{com} and v_{diff} .
- 2. It does not show that the steady state solution would be periodic.

Since the steady state solution of the dynamic system should be described by Fourier series to apply HSS modelling, it should be proved that the steady state solution of the dynamic system is periodic.

The dynamic model can be generalised by Equation 4.52,

$$\frac{d\mathbf{x}(t)}{dt} = \mathbf{A}(t)\mathbf{x}(t) + \mathbf{B}(t)$$
(4.52)

where

$$\mathbf{A}(t) = \begin{pmatrix} -\frac{R_p}{L_p} & 0 & -\frac{n_{com}(t)}{L_p} & -\frac{n_{diff}(t)}{L_p} \\ 0 & -\frac{2R_{load} + R_p}{2L_{load} + L_p} & \frac{n_{diff}(t)}{2L_{load} + L_p} & \frac{n_{com}(t)}{2L_{load} + L_p} \\ \frac{n_{com}(t)}{NC} & -\frac{n_{diff}(t)}{NC} & 0 & 0 \\ \frac{n_{diff}(t)}{NC} & -\frac{n_{com}(t)}{NC} & 0 & 0 \end{pmatrix}$$
(4.53)

$$\mathbf{B}(t) = \begin{pmatrix} \frac{V_{DC}}{2l_P} \\ -\frac{v_{load}}{2L_{load} + L_p} \\ 0 \\ 0 \end{pmatrix}$$
(4.54)

and

$$\mathbf{x} = \begin{pmatrix} i_{com} \\ i_{diff} \\ v_{com} \\ v_{diff} \end{pmatrix}$$
(4.55)

Since both $\mathbf{A}(t)$ and $\mathbf{B}(t)$ are periodic of period T, it was shown in [86] that the system has a unique periodic solution of period T. Therefore, the steady state solution of the dynamic model can be described by Fourier series with the fundamental frequency 1/T.

The HSS modelling

Because the steady state $[i_{com}i_{diff}v_{com}v_{diff}]^T$ of the system are considered to be periodic of period T, they can be expressed by a Fourier Series as shown in Equations 4.56.

$$i_{com} = \sum_{n=-\infty}^{\infty} i_{com_n} e^{jn\omega t}$$

$$i_{diff} = \sum_{n=-\infty}^{\infty} i_{diff_n} e^{jn\omega t}$$

$$v_{com} = \sum_{n=-\infty}^{\infty} v_{ccom_n} e^{jn\omega t}$$

$$v_{diff} = \sum_{n=-\infty}^{\infty} v_{cdiff_n} e^{jn\omega t}$$
(4.56)

where i_{com_n} , i_{diff_n} , v_{com_n} and $v_{diff_n} \in \mathbb{C}$ and $i_{com_{-n}} = i^*_{com_n}$, $i_{diff_{-n}} = i^*_{diff_n}$, $v_{com_{-n}} = v^*_{ccom_n}$, $v_{diff_{-n}} = v^*_{cdiff_n}$.

Because only the fundamental component of the output AC current is considered and the phase of i_{diff} is considered as the reference, i_{diff} can be described by Equation 4.57.

$$i_{diff} = i_{diff_1} \left(e^{j\omega t} + e^{-j\omega t} \right) \tag{4.57}$$

Then the load voltage v_{load} is described by Equation 4.58.

$$v_{load}(t) := |v_{load}| \cos(\omega t + \theta) = \frac{V_{load}}{2} e^{jn\omega t} + \frac{V_{load}^*}{2} e^{-jn\omega t}$$
(4.58)

where $V_{load} \in \mathbb{C}$ is the complex vector of the load voltage.

The modulation reference signals $n_{com}(t)$ and $n_{diff}(t)$ are calculated by Equation 4.59

$$n_{com}(t) = \frac{V_{DC}}{2V_{level}} \tag{4.59}$$

$$n_{diff}(t) = \frac{v_{AC}(t)}{V_{level}}$$

$$= \frac{V_{AC}e^{j\omega t} + V_{AC}^*e^{-j\omega t}}{2V_{level}}$$
(4.60)

where

- v_{AC} The output AC voltage v_{AC} as shown in Figure 4.20.
- $V_{AC}\,$ The complex vector of the output AC voltage.
- $V_{level}\,$ The level voltage of the output AC voltage

Substitute Equation 4.56 to Equation 4.48 and simplify, it yields Equation 4.61.

$$\sum_{n=-\infty}^{\infty} (jn\omega L_p + R_p)i_{com_n} = \begin{cases} -\frac{V_{DC}}{2V_{level}}v_{com_0} - \frac{V_{AC}}{2V_{level}}v_{diff_1} - \frac{V_{AC}^*}{2V_{level}}v_{diff_{-1}} + \\ \frac{V_{DC}}{2} & n = 0 \\ -\frac{V_{DC}}{2V_{level}}\sum_{n=-\infty}^{\infty}v_{ccom_n} - \frac{V_{AC}}{2V_{level}}\sum_{n=-\infty}^{\infty}v_{diff_{n+1}} \\ -\frac{V_{AC}^*}{2V_{level}}\sum_{n=-\infty}^{\infty}v_{diff_{n-1}} & n \neq 0 \end{cases}$$

$$(4.61)$$

$$\sum_{n=-\infty}^{\infty} jn\omega CNv_{com_n} e^{jn\omega t} = \frac{V_{DC}}{2V_{level}} \sum_{n=-\infty}^{\infty} i_{com_n} e^{jn\omega t} - \left(\frac{V_{AC}}{2vV_{level}} i_{diff_1} + \frac{V_{AC}^*}{2V_{level}} i_{diff_1}\right) - \frac{V_{AC}}{2V_{level}} i_{diff_1} e^{2j\omega t} - \frac{V_{AC}^*}{2V_{level}} i_{diff_1} e^{-2j\omega t} \quad (4.62)$$

$$\sum_{n=-\infty}^{\infty} jn\omega CNv_{diff_n} e^{jn\omega t} = \frac{V_{AC}}{2V_{level}} \sum_{n=-\infty}^{\infty} i_{com_{n-1}} e^{jn\omega t} + \frac{V_{AC}^*}{2V_{level}} \sum_{n=-\infty}^{\infty} i_{com_{n+1}} e^{jn\omega t} - \frac{V_{DC}}{2V_{level}} i_{diff_1} e^{jn\omega t} - \frac{V_{DC}}{2V_{level}} i_{diff_1} e^{-j\omega t} \quad (4.63)$$

In summary, when n = 0,

$$i_{com_0} = \frac{2\Re(V_{AC}i_{diff_1})}{V_{DC}}$$

$$v_{com_0} = V_{level} - \frac{2\Re(V_{AC}v_{diff_1})}{V_{DC}} - \frac{2R_p V_{level}i_{com_0}}{V_{DC}}$$

$$v_{diff_0} = -\frac{2\Re(V_{AC}v_{com_1}^*)}{V_{DC}}$$
(4.64)

When $n = \pm 1$,

$$i_{com_n} = -\frac{1}{jn\omega L_p + R_p} \left(\frac{V_{DC}}{2V_{level}} v_{com_n} + \frac{V_{AC}}{2V_{level}} v_{diff_{n+1}} + \frac{V_{AC}^*}{2V_{level}} v_{diff_{n-1}} \right)$$

$$v_{com_n} = -j \frac{V_{DC}}{2\omega CNV_{level}} i_{com_n}$$

$$v_{diff_n} = \frac{1}{j\omega CN} \left(\frac{V_{AC}}{2V_{level}} i_{com_{n-1}} - \frac{V_{DC}}{2V_{level}} i_{diff_n} + \frac{V_{AC}^*}{2nV_{level}} i_{com_{n+1}} \right)$$

$$(4.65)$$

When $n = \pm 2$

$$i_{com_{n}} = \frac{1}{jn\omega L_{p} + R_{p}} \left(-\frac{V_{DC}}{2V_{level}} v_{com_{n}} - \frac{V_{AC}}{2V_{level}} v_{diff_{n+1}} - \frac{V_{AC}^{*}}{2V_{level}} v_{diff_{n-1}} \right)$$

$$v_{com_{n}} = \frac{1}{jn\omega CN} \left(\frac{V_{DC}}{2V_{level}} i_{com_{n}} - \frac{V_{AC}}{2V_{level}} i_{diff_{n-1}} - \frac{V_{AC}^{*}}{2V_{level}} i_{diff_{n+1}} \right)$$

$$v_{diff_{n}} = \frac{1}{jn\omega CN} \left(\frac{V_{AC}}{2V_{level}} i_{com_{n-1}} + \frac{V_{AC}^{*}}{2V_{level}} i_{com_{n+1}} \right)$$
(4.66)

When n =others,



Figure 4.31: The flowchart of the computational tool

$$i_{com_n} = \frac{1}{jn\omega L_p + R_p} \left(-\frac{V_{DC}}{2V_{level}} v_{com_n} - \frac{V_{AC}}{2V_{level}} v_{diff_{n+1}} - \frac{V_{AC}^*}{2V_{level}} v_{diff_{n-1}} \right)$$

$$v_{com_n} = \frac{1}{jn\omega CN} \left(\frac{V_{DC}}{2V_{level}} i_{com_n} \right)$$

$$v_{diff_n} = \frac{1}{jn\omega CN} \left(\frac{V_{AC}}{2V_{level}} i_{diff_{n-1}} + \frac{V_{AC}^*}{2V_{level}} i_{diff_{n+1}} \right)$$

$$(4.67)$$

Equation 4.64, 4.65, 4.66 and 4.67 are the state space equations of the HSS model. Based on that, a computational tool can be developed to design the parameters of the MMC. The flowchart of the algorithm is shown in Figure 4.31 and the MATLAB code of the computational tool is in Appendix F.

According to [87], the iteration is stable if and only if Equation 4.68 is sat-

isfied.

$$\max\left(\frac{1}{|j\omega L_p + R_p|} \left(\left| \frac{V_{DC}}{2V_{level}} \right| + \left| \frac{V_{AC}}{2V_{level}} \right| \right) + \left| \frac{V_{AC}^*}{2V_{level}} \right| \right), \frac{1}{|j\omega CN|} \left(\left| \frac{V_{AC}}{2V_{level}} \right| + \left| \frac{V_{AC}^*}{2V_{level}} \right| \right) \right)$$

$$< 1$$

$$(4.68)$$

In order to design the parameters L_p , CN, some assumptions should be made as follows to develop an computational algorithm:

- 1. Only the $|v_{diff_1}|$ is considered to calculate the amplitude of $v_{diff}(t)$.
- 2. The required amplitudes of i_{com_2} and v_{diff_1} are given.

The the modified HSS model are described by Equations 4.69, 4.70, 4.71 and 4.72.

In summary, when n=0 ,

$$L_{p} = \left| \frac{V_{DC}v_{com_{2}} + V_{AC}v_{diff_{3}} + V_{AC}^{*}v_{diff_{1}}}{4j\omega V_{level}i_{com_{2}}} + \frac{R_{p}}{2j\omega} \right|$$

$$CN = \left| \frac{V_{AC}i_{com_{0}} + V_{AC}^{*}i_{com_{2}} - V_{DC}i_{diff_{1}}}{2j\omega V_{level}v_{diff_{1}}} \right|$$

$$i_{com_{0}} = \frac{2\Re(V_{AC}i_{diff_{1}})}{V_{DC}}$$

$$v_{com_{0}} = V_{level} - \frac{2\Re(V_{AC}v_{diff_{1}})}{V_{DC}} - \frac{2R_{p}V_{level}i_{com_{0}}}{V_{DC}}$$

$$v_{diff_{0}} = -\frac{2\Re(V_{AC}v_{com_{1}})}{V_{DC}}$$
(4.69)

When $n = \pm 1$,

$$i_{com_n} = -\frac{1}{jn\omega L_p + R_p} \left(\frac{V_{DC}}{2V_{level}} v_{com_n} + \frac{V_{AC}}{2V_{level}} v_{diff_{n+1}} + \frac{V_{AC}^*}{2V_{level}} v_{diff_{n-1}} \right)$$

$$v_{com_n} = -j \frac{V_{DC}}{2\omega CN V_{level}} i_{com_n}$$

$$(4.70)$$

When $n = \pm 2$

$$v_{com_n} = \frac{1}{jn\omega CN} \left(\frac{V_{DC}}{2V_{level}} i_{com_n} - \frac{V_{AC}}{2V_{level}} i_{diff_{n-1}} - \frac{V_{AC}^*}{2V_{level}} i_{diff_{n+1}} \right)$$

$$v_{diff_n} = \frac{1}{jn\omega CN} \left(\frac{V_{AC}}{2V_{level}} i_{com_{n-1}} + \frac{V_{AC}^*}{2V_{level}} i_{com_{n+1}} \right)$$

$$(4.71)$$

When n =others,

$$i_{com_n} = \frac{1}{jn\omega L_p + R_p} \left(-\frac{V_{DC}}{2V_{level}} v_{com_n} - \frac{V_{AC}}{2V_{level}} v_{diff_{n+1}} - \frac{V_{AC}^*}{2V_{level}} v_{diff_{n-1}} \right)$$

$$v_{com_n} = \frac{1}{jn\omega CN} \left(\frac{V_{DC}}{2V_{level}} i_{com_n} \right)$$

$$v_{diff_n} = \frac{1}{jn\omega CN} \left(\frac{V_{AC}}{2V_{level}} i_{diff_{n-1}} + \frac{V_{AC}^*}{2V_{level}} i_{diff_{n+1}} \right)$$

$$(4.72)$$

The flowchart of the design algorithm is shown in Figure 4.32.

Similarly, the convergence of the iteration is dependent on Equation 4.73 according to [87].

$$\max\left(\frac{|V_{DC}| + |V_{AC}|}{|4j\omega V_{level} i_{com_2}|}, \left|\frac{V_{AC}}{2j\omega V_{level} v_{diff_1}}\right|\right) < 1$$

$$(4.73)$$

So the design procedure is:

- 1. Calculate the L_p , CN using the script described by flowchart 4.32 according to the required v_{diff_1} and i_{com_2} .
- 2. Validate the design with the script descirbed by flowchart 4.31.

The main problem of this design is that both algorithms should be convergent. Otherwise, if the step 1 is not convergent, L_p and CN cannot be calculated; if the step 2 is not convergent, the results of the design cannot be validated.



Figure 4.32: The flowchart of the MMC design algorithm

Validation of the HSS model based design algorithm

A case study based on the simulation model shown in Figure 4.25 is proceeded to validate the design procedure. Since

- The MMC converters used in Cd-E1 are not 50Hz
- The algorithms are not convergent at 50Hz

The operating frequency in the case study is changed to 150Hz. The process of the validation is

- 1. Calculate i_{diff} at 150Hz with the same $v_{ac}(t)$.
- 2. Calculate L_p and CN based on the i_{diff} and 150Hz
- 3. Run the simulation model with the operating frequency 150Hz.
- 4. Compare the waveforms of the HSS model and the simulation

The parameters of the simulation model are shown in Table 4.10.

i_{com_2}	$20\% i_{ac}$	ω	$300\pi rad/s$
v_{diff_1}	2V	n_{com}	2
R_{load}	57.6Ω	n_{diff}	$1.44\cos(\omega t)$
L_{load}	9mH	V_{DC}	300V
NC	$1200\mu F$	v_{load}	0
f_{sw}	1kHz		

Table 4.10: The parameters of the simulation model

The comparisons of the waveforms are shown in Figure 4.33, 4.34 and 4.35. Because of the approximation that are made to proceed the analysis, there are errors between the results of HSS model and simulation. Therefore the calculated L_p and CN sometimes should be adjusted to suppress the ripple of arm current and capacitor voltages. The 2^{nd} harmonic of i_{com} of the simulation model is higher than the HSS model, so it is necessary to increase the value of L_p in practise to suppress the ripple. Also, i_{com} control will also be applied to suppress the ripple. It is obvious that there is a small difference between amplitudes of the ripple voltages of the HSS model and the simulation, which is caused by neglecting the high order harmonic components of v_{diff} .



Figure 4.33: The comparisons between the waveforms of i_{com} of the HSS model and the simulation model



Figure 4.34: The comparisons between the waveforms of v_{com} of the HSS model and the simulation model



Figure 4.35: The comparisons between the waveforms of v_{diff} of the HSS model and the simulation model

variables	nominal value and perturbation
v_{com}	$V_{com} + \delta v_{com}$
v_{diff}	$V_{diff} + \delta v_{diff}$
i_{com}	$I_{com} + \delta i_{com}$
i_{diff}	$I_{diff} + \delta i_{diff}$
n_{com}	$N_{com} - \delta n_{com}$
n_{diff}	$0 + \delta n_{diff}$
v_{load}	$0 + \delta v_{load}$

Table 4.11: Perturbation of each state variables and modulation reference signals

4.4.4 The Linearsied time-invariant (LTI) model of the single phase MMC

In order to apply linear control theory to design the controllers, a linearised model should be developed based on the dynamic model Equation 4.48. According to [60], the perturbation method is applied to obtain a LTI model and the goal of the linearisation is to obtain an ODE in the form of Equation 4.74.

$$\frac{d\mathbf{x}}{dt} = \mathbf{A}\mathbf{x} + \mathbf{B}\mathbf{u} + \mathbf{d} \tag{4.74}$$

where,

- A,B are constant matrices.
- **x** is the state variable vector.
- **u** is the input vector.
- **d** is the disturbance vector.

The perturbations of the state variables and modulation references signals are listed in Table 4.11.

Substituting the variables in Table 4.11 into Equation 4.48, the dynamic equations for the nominal value of $[I_{com}, I_{diff}, V_{com}, V_{diff}]^T$ is shown as Equation 4.75. It can be easily shown that the vector $[I_{com}, I_{diff}, V_{com}, V_{diff}]^T$ con-

verges to $[0, 0, \frac{V_{DC}}{2N_{com}}, 0]^T$. The perturbation of the vector $[\delta i_{com}, \delta i_{diff}, \delta v_{com}, \delta v_{diff}]^T$ is shown as Equation 4.76, which will be used to design the controllers in Chapter 5.

$$\frac{d}{dt} \begin{pmatrix} I_{com} \\ I_{diff} \\ V_{com} \\ V_{diff} \end{pmatrix} = \begin{pmatrix} -\frac{R_p}{L_p} & 0 & -\frac{N_{com}}{L_p} & 0 \\ 0 & -\frac{R_p + 2R_{load}}{L_p + 2L_{load}} & 0 & -\frac{N_{com}}{L_p + 2L_{load}} \\ \frac{N_{com}}{NC} & 0 & 0 & 0 \\ 0 & \frac{N_{com}}{NC} & 0 & 0 \end{pmatrix} \begin{pmatrix} I_{com} \\ I_{diff} \\ V_{com} \\ V_{diff} \end{pmatrix} + \begin{pmatrix} \frac{V_{DC}}{2L_p} \\ 0 \\ 0 \\ 0 \end{pmatrix}$$

$$(4.75)$$

$$\frac{d}{dt} \begin{pmatrix} \delta i_{com} \\ \delta i_{diff} \\ \delta v_{com} \\ \delta v_{diff} \end{pmatrix} = \begin{pmatrix} -\frac{R_p}{L_p} & 0 & -\frac{N_{com}}{L_p} & 0 \\ 0 & -\frac{R_p + 2R_{load}}{L_p + 2L_{load}} & 0 & \frac{N_{com}}{L_p + L_{load}} \\ \frac{N_{com}}{CN} & 0 & 0 & 0 \\ 0 & -\frac{N_{com}}{CN} & 0 & 0 \end{pmatrix} \begin{pmatrix} \delta i_{diff} \\ \delta v_{com} \\ \delta v_{diff} \end{pmatrix} + \left(\frac{\frac{V_{DC}}{2L_p N_{com}}}{\frac{V_{DC}}{(L_p + 2L_{load}) N_{com}}} \\ 0 & 0 \\ 0 & 0 \end{pmatrix} \begin{pmatrix} \delta n_{com} \\ \delta n_{diff} \end{pmatrix} + \left(\frac{0}{-\frac{\delta v_{load}}{2L_{load} + L_p}} \\ 0 \\ 0 \end{pmatrix} \\ \end{pmatrix} \right) \tag{4.76}$$

4.5 Calculation of the parameters of the Transformers and the MMCs

Since it is not practical to build 400kV switching model of MMCs, so as the entire Cd-E1 in PLECS, a simulation model with reduced power and voltage level (16kV, 20MW) but with the same current level (The DC current is 1000A, AC current is 2500A) will be built. In order to implement the entire simulation model of Cd-E1, the parameters required to built a simulation model are listed as follows,

- The leakage and magnetising inductance of the transformers
- The arm inductance of the MMCs
- The product of the size of each capacitor and the number of submodules

The parameters of the transformers

The leakage inductance and mutual inductance are the parameters that should be calculated. The reactive power transmitted by the transformer is calculated by Equation 4.77

$$Q = S \times \sin(\arccos(pf)) \tag{4.77}$$

The the leakage inductance is calculated by

$$L_{leak} = \frac{Q}{\omega I_{RMS}^2} \tag{4.78}$$

So the required parameters of the transformers in Cd-E1 are calculated and listed in Table 4.12.

The parameters of the transformers in the simulation model are scaled down from the Table 4.12 and are shown in Table 4.13.
Power transmitted	540MVA
Peak input voltage	400kV
Peak output voltage	400kV
Magnetising inductance	175.3H
Power factor	0.925
Leakage inductance	41.5mH
Turn ratio	1
Operating frequency	252Hz

Table 4.12: The parameters of the transformer of Cd-E1

Table 4.13: The parameters of the transformer of the simulation model

Power transmitted	21.6MVA
Peak input voltage	16kV
Peak output voltage	16kV
Magnetising inductance	7.02H
Power factor	0.925
Leakage inductance	1.7mH
Turn ratio	1
Operating frequency	252Hz

Basic parameters of	1-phase MMC	Design Requirem	ents
Name	Value	Name	Value
VDC (kV)	16	icom2 (A)	1
√load (kV)	15.5000	vripple (∨)	60
Frequency (Hz)	252		
AC (A)	2500		
_load (mH)	1.7000		Design
vlevel (V)	2000	Lp and CN	
		Name	Value
		Lp (mH)	2.3536
Select the Model		CN (mF)	21.5116
Select the Model	Simulation	CN (mF)	21.5110

Figure 4.36: The MATLAB application of the MMC designer

The parameters of the MMCs

According to the algorithm described by flow chart 4.32, a MATLAB application is developed to calculate the L_p and CN. The application is shown in Figure 4.36.

For the simulation model, it can be seen from Figure 4.36 that L_p is 0.98mH and CN is 21.2mF. If there are 10 submodules at the upper and lower arm, the size of the capacitors is 2mF

4.6 Conclusions

This chapter discussed the design procedure of a transformer and methods of analysis and modelling the half bridge MMC. The different modelling methods are summarised as follows:

- 1. LTV model is used to analyse the transient time response with numerical methods and derive the other two models.
- 2. Fourier Analysis is used to develop computational tools to design the converter or estimate the steady state response efficiently.

3. LTI model from perturbation linearisation is used as a nominal system for controller design.

The design of the transformer and the MMC are conducted in this chapter. This includes determing the operating frequency and calculating the power factor and the leakage inductance of the transformer, arm inductor and the size of the capacitors of the MMCs. The parameters designed in this chapter will be used to design the controller, which will be discussed in the chapter 5.

Chapter 5

The design of the controllers for the DC/DC converters and the MMCs

This chapter will discuss the design of the controllers in the DC/DC converters of Cd-E1. For the MMC converters, the objectives of the controllers that should be designed are as follows:

- 1. Control the average value of v_{com} .
- 2. Suppress the harmonics of i_{com} .

For the DAB, only a power flow controller should be implemented.

This chapter will start with the control of i_{com} and v_{com} . After that the phased-shift controller for DAB power flow control will be discussed. Then the simulation of the entire system will be presented.

5.1 Control of i_{com} and v_{com} of MMCs

In order to make the MMCs operate properly, the capacitor voltages must be controlled at a given voltage reference level[88]. The block diagrams that will be applied are shown in Figure 5.1.



Figure 5.1: Block diagram of the control scheme of v_{com} and i_{com}

The voltage control can be separated into two loops:

- The average voltage controller generates the reference signal i_{com}^* regarding the error between the reference signal v_{com}^* and v_{com} . The controller is designed that the average value of v_{com} traces the v_{com}^* .
- The current control controller generates the modulation reference signal n_{com} regarding the error between the reference signal i^*_{com} and i_{com} . The controller is designed that the harmonics of i_{com} is suppressed.

5.1.1 The design of i_{com} controller

According to Equation 4.76, the linear time invariant dynamic equation of $[i_{com}, v_{com}]^T$ which is used to design the controller is shown as Equation 5.1.

$$\frac{d}{dt} \begin{pmatrix} i_{com} \\ v_{com} \end{pmatrix} = \begin{pmatrix} -\frac{R_p}{L_p} & -\frac{N_{com}}{L_p} \\ \frac{N_{com}}{CN} & 0 \end{pmatrix} \begin{pmatrix} i_{com} \\ v_{com} \end{pmatrix} + \begin{pmatrix} \frac{V_{DC}}{2L_pN_{com}} \\ 0 \end{pmatrix} n_{com}$$
(5.1)

According to [89] and assuming R_p is negligible, the differential equation for i_{com} can be simplified to Equation 5.2 and the transfer function is shown as equation 5.3, where the term $\frac{N_{com}}{sL_p}v_{com}(t)$ is treated as a disturbance. The transfer function from n_{com} to i_{com} is $G_{c_{i_{com}}}(s)$ defined in Equation 5.4.

$$\frac{d}{dt}i_{com} = \frac{V_{DC}}{2L_p N_{com}} n_{com} - \frac{N_{com}}{L_p} v_{com}$$
(5.2)

$$i_{com}(s) = \frac{V_{DC}}{2sL_p N_{com}} \left(n_{com}(s) - \frac{2N_{com}^2}{V_{DC}} v_{com}(s) \right)$$
(5.3)



Figure 5.2: Block diagram fo the control of MMC

$$G_{c_{i_{com}}}(s) := \frac{V_{DC}}{2sL_pN_{com}}$$
(5.4)

The block diagram of the control scheme of the MMC is shown in Figure 5.3. The inner current control loop is described by Figure 5.3.

where

- d_i is the plant input disturbance
- The current controller can be implemented by any control algorithm. But a discrete linear controller will be applied because it is effective and simple to implement.
- i_{com}^* is the reference of i_{com} .
- The current sensor samples i_{com} and digitalise the signal.
- $G_{c_{icom}}$ is the transfer function defined in Equation 5.4.

The parameters that are used in the design of the controller are listed in Table 5.1.

So the continuous transfer function from n_{com} to $i_{com} G_{c_{i_{com}}}(s)$ is calculated by Equation 5.5 and the discrete transfer function $G_{d_{i_{com}}}(z)$ is Equation 5.6.

$$G_{c_{i_{com}}}(s) = \frac{1 \times 10^6}{s}$$
(5.5)



Figure 5.3: The block diagram of the control loop of i^*_{com}

Table 5.1: The parameters that is used in the design of the controller

Parameters	Value
L_p	2mH
Sampling frequency	60kHz
V_{DC}	16kV
N_{com}	4

$$G_{d_{i_{com}}}(z) = \frac{16.67}{z-1} \tag{5.6}$$

According to [90], the sensitivity transfer function $S_{d_{i_{com}}}(z)$ and complementary sensitivity transfer function $T_{d_{i_{com}}}(z)$ are defined by Equation 5.7.

$$S_{d_{icom}} = \left(1 + G_{d_{icom}} K_{d_{icom}}\right)^{-1}$$

$$T_{d_{icom}} = S_{d_{icom}} G_{d_{icom}} K_{d_{icom}}$$
(5.7)

where $K_{d_{i_{com}}}(z)$ is the discrete transfer function of the current controller that should be designed.

The objectives of the controller are listed as follows,

- Good reference tracking. i_{com} should track the reference i_{com}^* . According to [90], $\sup\left(\left|T_{d_{i_{com}}}(j\omega)\right|\right) \approx 1$.
- Disturbance attenuation $\sup (|S_{d_{i_{com}}}(j\omega)|)$ should be made small [90]. For MMC converters the main harmonic component that should be suppressed is the 2^{nd} order harmonic[91].
- $K_{d_{i_{com}}}(z)$ should stabilise $G_{d_{i_{com}}}(z)$.

According to the following reasons,

- 1. The slope in the high frequency region of the bode plot of $S_{d_{i_{com}}}(z)$ is 20dB/Dec to avoid stability problem[90].
- 2. The crossover frequency of $S_{d_{i_{com}}}(z)$ should be lower than $f_{sw}/2$, where f_{sw} is the sampling frequency.

 $K_{d_{i_{com}}}(z)$ is designed to be Equation 5.8 by using MATLAB SISOTOOL. $S_{d_{i_{com}}}(z)$ is Equation 5.9 and the bode plot of $S_{d_{i_{com}}}(z)$ is shown in Figure 5.4. The magnitudes of each frequency in Figure 5.4 implies the suppression of the harmonic of that frequency[90]. The magnitude of $S_{d_{i_{com}}}(z)$ at 2^{nd} harmonic is -22dB, which leads to a suppression to 7.9% calculated by Equation

$$K_{d_{i_{com}}}(z) = 0.04 \frac{z - 0.99}{z - 1}$$
(5.8)

$$S_{d_{i_{com}}}(z) = \frac{(z-1)^2}{(z-0.3435)(z-0.9898)}$$
(5.9)

$$10 \frac{\left|S_{d_{v_{com}}}\right|_{f=504Hz}}{20} = 7.9\% \tag{5.10}$$

The transfer function $T_{d_{i_{com}}}(z)$ is calculated by Equation 5.11.

$$T_{d_{i_{com}}}(z) = \frac{0.66667(z - 0.99)}{(z - 0.3435)(z - 0.9898)}$$
(5.11)



Figure 5.4: Bode plot of $S_{d_{i_{com}}}(z)$



Figure 5.5: Block diagram of the control loop of \overline{v}_{com}

It is obvious that all the zeros and poles locate in the region |z| < 1, so the current control loop is stable. Also, $T_{d_{i_{com}}}(z)$ is used in the design of average voltage controller.

The design of \overline{v}_{com} controller

Since the average value of v_{com} , which is denoted by \overline{v}_{com} , should be controller at a reference value, a controller for the control of \overline{v}_{com} should be designed.

According to Equation 5.1, the transfer function $G_{d_{v_{com}}}(z)$ from $i^*_{com}(z)$ to $v_{com}(s)$ is calculated by 5.12.

$$G_{d_{v_{com}}}(z) = \mathcal{Z}\left(\frac{N_{com}}{sCN}\right) T_{d_{i_{com}}}(z) = \mathcal{Z}\left(\frac{181.8}{s}\right) T_{d_{i_{com}}}(z)$$

$$= \frac{0.003}{z-1} \frac{0.66667(z-0.99)}{(z-0.3434)(z-0.9898)}$$
(5.12)

The block diagram of the control loop of v_{com} is shown in Figure 5.5.

The transfer function of v_{com} controller is denoted by $K_{d_{v_{com}}}$. The sensitivity transfer function $S_{d_{v_{com}}}$ and the complementary transfer function $T_{d_{v_{com}}}$ of v_{com} control loop are defined by Equation 5.13.

$$S_{d_{v_{com}}} = \left(1 + K_{d_{v_{com}}}G_{d_{v_{com}}}\right)^{-1}$$

$$T_{d_{v_{com}}} = S_{d_{v_{com}}}K_{d_{v_{com}}}G_{d_{v_{com}}}$$
(5.13)

In order to extract \overline{v}_{com} , a filter is placed at the feedback loop.Because the largest harmonic component is the 2^{nd} harmonic, \overline{v}_{com} can be extracted by

Equation 5.14, which cancels the 2^{nd} harmonic.

$$\overline{v}_{com} = \frac{1}{2} \left(v_{com}(t) + v_{com}(t + \frac{T}{4}) \right)$$
(5.14)

Where T is the period of the operating frequency of the MMC. In order to delay the v_{com} with $\frac{T}{4}$, which is 1ms, a high order memory can be applied to delay the signal. Because the sampling frequency is 60kHz and the frequency of 2^{nd} harmonic of v_{com} is 504Hz, the order of the memory is calculated by Equation 5.15.

$$Ceiling\left(\frac{60e3}{504\times2}\right) = 60\tag{5.15}$$

So the transfer function of the filter is Equation 5.16.

$$H_{d_{v_{com}}}(z) = 1 - z^{-60} \tag{5.16}$$

Because this filter delays the signal by 1ms, the time response should be slower than the delay. According to [90], the bandwidth of the $T_{d_{v_{com}}}$ should be lower than 39.7Hz.

From MATLAB SISOTOOL, $K_{d_{v_{com}}}$ is designed to be Equation 5.17.

$$K_{d_{v_{com}}} = 0.6 \frac{z - 0.995}{z - 1} \tag{5.17}$$

The transfer function of $T_{d_{v_{com}}}$ is Equation 5.18 and the bode plot is shown in Figure 5.6

$$T_{d_{v_{com}}}(z) = 0.0012 \frac{(z - 0.995)(z - 0.99)}{(z - 0.3453)(z^2 - 1.998z + 0.9982)}$$
(5.18)

Because the $|T_{d_{v_{com}}}(j\omega)|$ achieves 5.58*dB* at 29.6*Hz*, the system will have an overshoot. According to [90], a filter can be placed as shown in Figure 5.5



Figure 5.6: Bode plot of $T_{d_{v_{com}}}$

with a bandwidth lower than 29.6Hz to reduce the overshoot. The transfer function of the filter $F_{d_{v_{com}}}$ is equation

$$F_{d_{v_{com}}}(z) = \frac{0.001665}{z - 0.9983} \tag{5.19}$$

The results of the simulation of MMC control

In order to validate the design of the controllers, a simulation model is built to compare the waveforms of i_{com} and v_{com} with the time response calculated by MATLAB.

The topology of the simulation model is shown in Figure 5.8. Both of the MMCs are modulated with sinusoidal modulation reference signal as shown in Figure 5.7. n_{diff_2} is 50° lagging n_{diff_1} .

The simulation results and the calculated waveform of i_{com} and v_{com} are shown in Figure 5.9 and Figure 5.10. It is obvious that the simulation results is the same as the calculated waveform except for the ripples caused by the IGBT switchings.



Figure 5.7: The modulation reference signals for the primary and secondary side.



Figure 5.8: The simulation model used to validate the design of the controllers



Figure 5.9: The reference signal of i_{com} and the waveform of i_{com}



Figure 5.10: The reference signal and the waveform of v_{com}



Figure 5.11: The block diagram of the DC/DC converter in Cd-E1

5.1.2 Control of Power flow of the DC/DC converters of Cd-E1

Because v_{com} and i_{com} are controlled at a constant value, the energy stored in the MMCs is also constant. According to Equation 4.64, there is a DC component in i_{com} , which forms the DC current if there is real power flow.

The plant of the power flow control loop can be described by Figure 5.11. The modulation reference signal generator generates two sinusoidal signals with θ phase shift. If there is power flow between the two ports of the DC/DC converter, constant i_{DC_1} and i_{DC_2} are formed. So the power flow controller generates the phase shift angle, θ , to control the output current, i_{DC_2} , at the reference value.

Calculation of the transfer function from θ to i_{dc_2}

The block diagram of each of the DC/DC converter is shown in Figure 5.11. The first step to design the power controller is to calculate the transfer function from the phase shift angle, θ , to the output current, i_{dc_2} .

According to the ODE of the MMC converter Equation 4.48, the differential equation of v_{com} is Equation 5.20. Therefore the term $\frac{n_{diff}(t)}{CN}i_{diff}$ is considered as a disturbance to the system.



Figure 5.12: Block diagram of the plant of the power flow control loop of DC/DC converter

$$\frac{dv_{com}}{dt} = \frac{n_{com}(t)}{CN}i_{com} - \frac{n_{diff}(t)}{CN}i_{diff}$$
(5.20)

Therefore the block diagram for the plant of the power control loop of the DC/DC converter is shown in Figure 5.12,

where $M(\cdot)$ is an operator defined by Equation 5.21, which is calculated in Appendix and d_i is the disturbance caused by $i_{diff}n_{diff}$.

$$M(\cdot) := M(\cdot) = \frac{V_{AC}^2}{\omega(L_{leak} + 2L_p)V_{DC}}$$
(5.21)

The transfer function from d_i to i_{com} is denoted by $G_{d_{\theta}}(z)$ can be easily calculated by Equation 5.22 because all the other transfer functions are given.

$$G_{d_{d_i}}(z) = \frac{0.001212z^2 - 0.002406z + 0.001194}{z^4 - 3.333z^3 + 4.008z^2 - 2.016z + 0.3412}$$
(5.22)

A comparison between the calculated step response by MATLAB and the simulated waveform by PLECS are shown in Figure 5.13.

In the plot, the input signal is the $\theta(t)$ and the output waveform is the i_{dc_2} . The red waveform is calculated by MATLAB using the transfer function Equation 5.22 and the blue waveform is generated by PLECS simulation model as shown in Figure 5.8. It is obvious that the step response of the



Figure 5.13: The step response of the power flow control loop

transfer function Equation 5.22 is close to the simulation results. Therefore Equation 5.22 can be used as the transfer function of the plant to design the power flow controller.

The design of the power flow controller

Although the power rating of the Cd-E1 is 1000MW, the operating point is 300MW. So the rated power for each DC/DC converter is 150MW and the operating point is 150MW.Since the DC link voltage of both sides of the DC/DC converter is 400kV, the rated output current and the output current at the operating point can be easily calculated to be 1250A and 375A, respectively.

Similarly, denote $K_{d_{po}}(z)$ as the transfer function of the power flow controller, the sensitivity transfer function $S_{d_{po}}(z)$ and the complementary sensitivity transfer function $T_{d_{po}}(z)$ are defined by Equation 5.23.

$$S_{d_{po}}(z) = \left(1 + K_{d_{po}}G_{d_{po}}\right)^{-1} T_{d_{po}}(z) = S_{d_{po}}K_{d_{po}}G_{d_{po}}$$
(5.23)

Since i_{com} is regulated by the current controller $K_{d_{i_{com}}}(z)$, the harmonic introduced by the power flow control loop are suppressed by the controller.



Figure 5.14: The Bode plot of $S_{d_{po}}(z)$

According to Figure 5.4, the magnitude at 504Hz is -22dB. So the magnitude of $S_{d_{po}}(z)$ at 504 should be 0dB. From MATLAB SISOTOOL, the transfer function of $K_{d_{po}}(z)$ is designed to be Equation 5.24. The bode plot of $S_{d_{po}}(z)$ is shown in Figure 5.14.

$$K_{d_{po}}(z) = 0.0137 \frac{z - 0.996}{z - 1} \tag{5.24}$$

From Figure 5.14 it is obvious that the magnitude at 506Hz is positive, therefore the power flow control loop introduces no harmonics, of which the frequency is higher than 506Hz.

However there are slight differences between the time response of $T_{d_{po}}(z)$ of the MATLAB calculation and the PLECS simulation as shown in Figure 5.15. This is because in the design of $K_{d_{po}}(z)$ the nonlinear operator $M(\cdot)$ is approximated by Equation 5.25. The error between θ and $\sin(\theta)$ increases with θ .

$$M(\theta) = \frac{V_{AC}^2}{\omega(L_{leak} + 2L_p)V_{DC}}\sin(\theta)$$

$$M(\theta) = \frac{V_{AC}^2}{\omega(L_{leak} + 2L_p)V_{DC}}(\theta)$$
(5.25)



Figure 5.15: The step response of the T_{d_θ} calculated by MATLAB and PLECS simulation



Figure 5.16: The block diagram of the power flow control loop of the DC/DC converter

In order to validate the effect of the nonlinear operator, a MATLAB simulink model is built as shown in Figure 5.16. In this model a nonlinear operator $sin(\cdot)$ is used to convert θ to $sin(\theta)$. The results of the simulink simulation is the same as PLECS simulation as shown in Figure 5.17.

5.2 The simulation of Cd-E1

In order to validate the control design in Cd-E1, a simulation model of the entire system is built. The general structure of the simulation model of Cd-E1 is shown in Figure 5.18. The entire simulation of the Cd-E1 is shown in Figure 5.19.



Figure 5.17: The step response of the calculation of the MATLAB and the simulation of the PLECS $\,$



Figure 5.18: The general structure of the Cd-E1 simulation model



Figure 5.19: The simulation model of Cd-E1 $\,$



Figure 5.20: The output current of the DC/DC_u and DC/DC_l

5.2.1 The simulation results of the DC output current control loop

The waveforms of the output DC currents are shown in Figure 5.20 and Figure 5.21. It is obvious that the output currents of DC/DC_u and DC/DC_l are tracking the reference signals and the ripples are suppressed to lower than 10%. However, there are ripples at specific time points such as t = 0.5s, t = 0.95s. This is because of the events happened in MMCs that are listed in Figure 5.22.

where,

- t = 0.65s, v_{com}^* of MMC_{ll} shifts from 2000V to 2350V.
- t = 0.95s, v_{com}^* of MMC_{ul} changes shifts from 2000V to 2350V
- t = 1.15s, v_{com}^* of MMC_{lr} changes from 2500V to 2000V.
- t = 1.25s, v_{com}^* of MMC_{ur} changes from 2500V to 2000V

The AC currents of the primary and secondary sides of the transformers are shown in Figure 5.23 and Figure 5.24. The detailed waveforms are shown in



Figure 5.21: The output current of the DC/DC_l



Figure 5.22: The events happened in the MMCs



Figure 5.23: The AC currents of the primary and secondary sides of the transformer in DC/DC_u

Figure 5.25 and Figure 5.26. It can be seen that the AC current is stable although the amplitude is not constant. This is because the phase shift control loop does not regulate the AC current directly.

5.2.2 The results of the simulation of the MMC control

The waveforms of the v_{com} of each MMCs in Cd-E1 are shown in Figure 5.27 and Figure 5.28. From the figures it can be seen that:

- 1. v_{com} in each MMC tracks the references with a delay. This implies that the control design is successful.
- 2. There are fluctuations in specific time points. This is because of disturbances caused by the events mentioned in Figure 5.22.
- 3. There are damping oscillation at the beginning of the simulation. This is because that at the starting point of the simulation, PLECS set all the semiconductors to 'OFF'. The arm inductors are charged by the DC voltage sources. As the result, an initial current is generated in every arm. When the balancing algorithm begins to operate, the capacitors in the submodules, the arm inductors and the arm resistances form a



Figure 5.24: The AC currents of the primary and secondary sides of the transformer in DC/DC_l



Figure 5.25: The detailed AC currents of the primary and secondary sides of the transformer in DC/DC_u



Figure 5.26: The detailed AC currents of the primary and secondary sides of the transformer in DC/DC_u

resonant circuit. Therefore at the beginning of the simulation there is a damping oscillation caused by PLECS.

The waveforms of i_{com} of each MMC in Cd-E1 are shown in Figure 5.29 and Figure 5.30. It can be seen that the i_{com} of each MMC tracks the reference. Similarly,

- 1. There are fluctuations caused by the events shown in Figure 5.22.
- 2. There are damping oscillations at the beginning of the simulation caused by PLECS.

5.3 Conclusions

In this chapter the power controller and the MMC controllers are designed according to the linear control theory and listed as follows.

• DC current controller



Figure 5.27: The v_{com} of each MMC in DC/DC_u



Figure 5.28: The v_{com} of each MMC in DC/DC_l







Figure 5.30: The i_{com} of each MMC in DC/DC_l

- i_{com} controller with harmonic suppression
- average v_{com} controller

Chapter 6

Conclusions

6.1 Summary

It is believed that the ocean contains tremendous potential resources that can be utilised by humans. Advanced technologies make it convenient and efficient to convert between other forms of energy such as motion kermic energy and electricity and transmit bulk power over long distances. It is obvious that in future marine development offshore electric power networks will play an important role in terms of:

- Driving motors and other equipment
- Delivering power from offshore generators to onshore customers

This thesis has investigated the current situation of the developments of offshore energy and resource. It is the current trend that in the near future offshore networks with different configurations will coexist. Therefore a high power high voltage DC-DC converter will be required to integrate multiple HVDC networks and this thesis has focused on such a DC-DC converter for interfacing symmetric and bipolar HVDC configurations.

In order to conduct the design of the DC-DC converter. This thesis presented a comprehensive review of the current topologies of DC-DC converters and DC-AC converters. As the result a structure based on MMC and DAB is considered to be the suitable topology. Although power transformers have been widely and commercially used, a single phase high power unity ratio power transformer which is used for isolation in a DAB and operating at medium frequency (252Hz) has never been designed. This thesis reviewed the technology of power transformer design and implemented a MagNet simulation model to validate the feasibility of the proposed DC-DC converter transformer.

In terms of the design, although a significant amount of research effort been conducted, the dynamic equations of the single phase half bridge MMC (SPHB-MMC), which is the basic topology of the MMC, have not been explicitly derived. This thesis derived the dynamic equations of the SPHB-MMC according to conventional ODE theory and subsequently modified them through a transformation in order to set them to a form more suitable for control design. Based on the modified state space LTV equation, this thesis derived an iterative method to design the parameters and a nominal linear system for control design.

Based on the derived LTV model, a LTV model is developed, which is used to design the controllers for the average capacitor coltages and the suppression of the harmonics of the circulating currents of the MMCs and the power flow of each DC/DC converter. This thesis applied the conventional phase shift control methodology for DAB.

6.2 Contributions of the thesis

The research work presented in this thesis is aimed to contribute to the knowledge on high power DC-DC converters and the verification of control methodologies that would be suitable for operating such a converter as an HVDC interconnector. The main contributions of the thesis are summarised as follows:

- 1. Based on a comprehensive review of the modern technologies of DC-DC conversion and the modern topologies of multilevel converters that are used in HVDC systems, a novel topology of DC-DC converter is derived, which is specific for integration of symmetric and bipolar HVDC systems.
- 2. Following a review of conventional technology of power transformer engineering, a novel isolation power transformer is designed, which is

specific for the application of the HVDC DC-DC converter discussed in this thesis.

3. This thesis proposes a novel transformation of state space dynamic differential equation of single phase MMC, which extracts the common and differential components of the upper and lower arm current and capacitors voltages. Based on this transformation, the theory of differential equations and stability, the linear time-variant state-space model, steady state frequency response and nominal linearised models are derived. These models are used in continuous time-domain simulation, parameter design and control design.

6.3 Further work

The thesis focused on the topology of the HVDC interconnector between bipolar configuration and symmetric configuration and the control methodology to operate. There are topics and problems that can be conducted as further work and are listed as following:

- 1. Investigation of cable fault operation mode. There is recent research about cable fault operation stating that by alternating a small number of half bridge submodules to full bridge submodules, the MMC is possible to absorb the fault current with the capacitors. For Cd-E1, faults can occur from both sides of the converter and both MMCs operate at different modes (one is inverter mode and the other one is rectifier mode).
- 2. Circulating current ripple suppression. It can be seen from the waveforms in Chapter 6 that there is about 10% current ripple in the circulating current. It would be useful to investigate approaches to suppress the ripple.
- 3. The control of the power flow control. Phase shift control is a simple but effective approach to control the power flow. But it does not control the real power and reactive power. So the AC current at both sides of the transformer is large. It would be useful to investigate other control techniques such as dq control to suppress the reactive power flow so as to reduce the amplitudes of the AC currents

Appendix A

The Mathmatica code for the 400KV, 500MW Single Phase Isolation Transformer Design and Optimisation

 $vps = 400 \ 10^{3};$ $ips[power_]:=2power/vps/0.999;$ jps = 10; $Awire[power_]:=ips[power]/jps;$ kf = 4.44; Bm = 1.5; $rhos[power_]:=\frac{16.78 \ 10^{-6}}{A}/.A \rightarrow Awire[power];$

vPerTurn = 300;

NTurns = Ceiling[vps/vPerTurn];

 $\begin{aligned} &\text{ACore[freq_]}:=\frac{1.2v\text{PerTurn}}{\text{kfBmfreq}}10^6;\\ &\text{WidthCore[freq_]}:=\sqrt{\text{ACore[freq]}};\\ &\text{RCore[freq_]}:=\sqrt{\text{ACore[freq]}/\pi}; \end{aligned}$

dcore = vps/30000; dps = 2vps/30000; dwire = vPerTurn/30000;

kh = 0.0056186; $\alpha = 1.33634;$ $\beta = 1.91524;$ ke = 0.000139186; s = 1;

$$\label{eq:widthWire} \begin{split} & \text{WidthWire}[\mathbf{a}_{-},\mathbf{p}_{-}] := \sqrt{\text{Awire}[p]a}; \\ & \text{HeigthWire}[\mathbf{a}_{-},\mathbf{p}_{-}] := \sqrt{\text{Awire}[p]/a}; \\ & \text{TurnsPerDisk}[\mathbf{b}_{-}] := \sqrt{\text{NTurns}/b} //\text{Ceiling}; \\ & \text{NDisks}[\mathbf{b}_{-}] := \text{NTurns}/\text{TurnsPerDisk}[b] //\text{Ceiling}; \\ & \text{WidthWindow}[\mathbf{a}_{-},\mathbf{b}_{-},\mathbf{p}_{-}] := 2(\text{TurnsPerDisk}[b] \text{WidthWire}[a,p] + 2\text{dcore}); \\ & \text{HeightWindow}[\mathbf{a}_{-},\mathbf{b}_{-},\mathbf{p}_{-}] := 2\text{dcore} + \text{NDisks}[b] \text{HeigthWire}[a,p] + 1.2\text{NTurns}; \\ & \text{LengthWire}[\mathbf{a}_{-},\mathbf{b}_{-},\mathbf{p}_{-},\mathbf{f}_{-}] := 4\pi \text{NTurns}(2\text{dcore} + \text{TurnsPerDisk}[b] \text{WidthWire}[a,p] + \text{RCore}[f]); \end{split}$$

VCore[a_, b_, p_, freq_]:=2ACore[freq]HeightWindow[a, b, p]+ 2 (2WidthWindow[a, b, p] + (2 + $\frac{\pi}{2}$) RCore[freq]) $\frac{1}{2}$ ACore[freq]; WeightCore[a_, b_, p_, freq_]:=VCore[a, b, p, freq] 7.84 10⁻⁶; $\begin{aligned} &\text{ResistanceWire}[a_{-}, b_{-}, p_{-}, f_{-}] := \text{LengthWire}[a, b, p, f] 16.78 \ 10^{-6} / \text{Awire}[p]; \\ &\text{Pfe}[\text{freq}_{-}] := \text{khfreq}^{\alpha} \text{Bm}^{\beta} + \text{ke}(s\text{freqBm})^{2}; \\ &\text{CoreLoss}[a_{-}, b_{-}, p_{-}, \text{freq}_{-}] := \text{WeightCore}[a, b, p, \text{freq}] \text{Pfe}[\text{freq}]; \\ &\text{CopperLoss}[a_{-}, b_{-}, p_{-}, f_{-}] := \frac{1}{2} \text{ips}[p]^{2} \text{ResistanceWire}[a, b, p, f]; \\ &\text{EfficiencyTransformer}[a_{-}, b_{-}, p_{-}, \text{freq}_{-}] := (1 - (\text{CopperLoss}[a, b, p, \text{freq}] + \text{CoreLoss}[a, b, p, \text{freq}])/p) \\ &\text{EfficiencyDesign}[f_{-}] := \text{NMaximize} [\{\text{EfficiencyTransformer}[a, b, 500 \ 10^{6}, f], 2/120 < a < 60, 1/\text{NTerms} < b < 10^{6}, f], 2/120 < a < 60, 1/\text{NTerms} < b < 10^{6}, f], 2/120 < a < 60, 1/\text{NTerms} < b < 10^{6}, f], 2/120 < a < 60, 1/\text{NTerms} < b < 10^{6}, f], 2/120 < a < 60, 1/\text{NTerms} < b < 10^{6}, f], 2/120 < a < 60, 1/\text{NTerms} < b < 10^{6}, f], 2/120 < a < 60, 1/\text{NTerms} < b < 10^{6}, f], 2/120 < a < 60, 1/\text{NTerms} < b < 10^{6}, f], 2/120 < a < 60, 1/\text{NTerms} < b < 10^{6}, f], 2/120 < a < 60, 1/\text{NTerms} < b < 10^{6}, f], 2/120 < a < 60, 1/\text{NTerms} < b < 10^{6}, f], 2/120 < a < 60, 1/\text{NTerms} < b < 10^{6}, f], 2/120 < a < 60, 1/\text{NTerms} < b < 10^{6}, f], 2/120 < a < 60, 1/\text{NTerms} < b < 10^{6}, f], 2/120 < a < 60, 1/\text{NTerms} < b < 10^{6}, f], 2/120 < a < 60, 1/\text{NTerms} < b < 10^{6}, f], 2/120 < a < 60, 1/\text{NTerms} < b < 10^{6}, f], 2/120 < a < 60, 1/\text{NTerms} < b < 10^{6}, f], 2/120 < a < 60, 1/\text{NTerms} < b < 10^{6}, f], 2/120 < a < 60, 1/\text{NTerms} < b < 10^{6}, f], 2/120 < a < 60, 1/\text{NTerms} < b < 10^{6}, f], 2/120 < a < 60, 1/\text{NTerms} < b < 10^{6}, f], 2/120 < a < 60, 1/\text{NTerms} < b < 10^{6}, f], 2/120 < a < 60, 1/\text{NTerms} < b < 10^{6}, f], 2/120 < a < 60, 1/\text{NTerms} < b < 10^{6}, f], 2/120 < a < 60, 1/\text{NTerms} < b < 10^{6}, f], 2/120 < a < 60, 1/\text{NTerms} < b < 10^{6}, f], 2/120 < a < 60, 1/\text{NTerms} < b < 10^{6}, f], 2/120 < a < 60, 1/\text{NTerms} < b < 10^{6}, f], 2/120 < a < 60, 1/\text{NTerms} < b < 10^{6}, f], 2/120 < a < 60, 1/\text{NTerms} < b < 10^{6},$

```
 \begin{aligned} & \text{EfficiencyTable} = \text{Table}[\{f, \text{EfficiencyDesignValue}[f]\}, \{f, 25, 500, 5\}]; \\ & \text{EfficiencyDesignInt} = \text{Interpolation}[\text{EfficiencyTable}]; \end{aligned}
```

Plot and Analysis

NTurns

NDisks[b]/.WeightCoreOpt[252][[2]]

NDisks[b]/.EfficiencyDesign[252][[2]]

RCore[252]

ACore[252]

 \mathbf{dcore}

WidthWire $[a, 500 \ 10^6]$ /.WeightCoreOpt[252][[2]]

 ${\rm HeighWire}\left[a, 500\ 10^6\right]/.{\rm WeightCoreOpt}[252][[2]]$

 $\label{eq:widthWindow} [a, b, 500 \ 10^6] \, / . \\ \mbox{WeightCoreOpt} [252] [[2]]$

 ${\rm HeightWindow}\left[a,b,500\ 10^{6}\right]/.{\rm WeightCoreOpt}[252][[2]]$

WidthWire $[a, 500 \ 10^6]$ /.EfficiencyDesign[252][[2]]

HeighWire $[a, 500 \ 10^6]$ /.EfficiencyDesign[252][[2]]

WidthWindow $[a, b, 500 \ 10^6]$ /.EfficiencyDesign[252][[2]]

EfficiencyDesign[252][[2]]

HeightWindow $[a, b, 500 \ 10^6]$ /.EfficiencyDesign[252][[2]]

 $(CopperLoss [a, b, 500 \ 10^{6}, 252] / EfficiencyDesign[252][[2]]) / 2500^{2}2$

EfficiencyTransformer $[a, b, 500 \ 10^6, 252]$ /.WeightCoreOpt[252][[2]]
$\begin{aligned} &\operatorname{Plot}[\{\operatorname{WeightCoreOpt}[f][[1]],\operatorname{WeightCoreDesign}[f]\}, \{f, 25, 700\},\operatorname{AxesOrigin} \to \{0, 0\},\operatorname{GridLines}\\ &\operatorname{AxesLabel} \to \{\text{``f (Hz)'', ``Weight (kg)''}\},\operatorname{PlotLabel} \to \text{``Weight of the Core'',}\\ &\operatorname{PlotLegends} \to \{\text{``The Lowest Weight of Core'', ``Weight of Core at maximum efficiency''}\}] \end{aligned}$

 $\begin{aligned} & \text{Plot}[\text{EfficiencyDesign}[f][[1]], \{f, 25, 700\}, \text{AxesOrigin} \rightarrow \{0, 99.4\}, \text{AxesLabel} \rightarrow \{\text{``f}(\text{Hz})\text{''}, \text{``efficiency} \text{ of Transformer''}\} \end{aligned}$

WidthWire $[a, 500 \ 10^6]$ /.EfficiencyDesign[252][[2]]

HeighWire $[a, 500 \ 10^6]$ /.EfficiencyDesign[252][[2]]

NDisks[b]/.EfficiencyDesign[252][[2]]

 $EfficiencyTable = Table[\{f, EfficiencyDesignValue[f]\}, \{f, 25, 500, 5\}];$

EfficiencyDesignInt = Interpolation[EfficiencyTable]

 $Plot[EfficiencyDesignInt[f], \{f, 25, 500\}]$

 $\label{eq:non-static-static} \texttt{NMaximize}[\{\texttt{EfficiencyDesignInt}[f], 25 < f < 500\}, \{f\}]$

HeighWire $[a, 500 \ 10^6]$ /.EfficiencyDesign[150][[2]]

 ${\rm WidthWire}\left[a,500~10^6\right]/.{\rm EfficiencyDesign}[150][[2]]$

WeightCoreDesign[252]

WeightCoreOpt[252]

RCore[252]

Appendix B

The C Code for the capacitor voltage balancing in PLECS C Script

B.1 Code declaration

#include <stdlib.h>
#define TRUE 1
#define FALSE 0

typedef int bool;
typedef struct mmcSubmodules{
 int nth;
 double vol;
}submodule;

typedef struct mmcLimb{
 struct mmcLimb *prev;
 struct mmcLimb *next;
 submodule cell;
}cellsList;

int nsubs,nExtSwitchForBalance; bool initComp = FALSE;

```
int modulationIndex [2];
double current;
cellsList *pCellsList, *idleList, *busyList;
cellsList *pUpdate, *pOutput;
void limbInitialise(int);
void limbDelete();
cellsList *removeCell(cellsList*);
void insertCellFromLeft(cellsList*, cellsList*);
void insertCellFromRight(cellsList*,cellsList*);
void insertCellToListDec(cellsList*,cellsList*);
void insertCellToListInc(cellsList*,cellsList*);
void listExchangePositiveCurrent(int);
void listExchangeNegativeCurrent(int);
cellsList* selectCellFromListHighestVol(cellsList*);
cellsList* selectCellFromListLowestVol(cellsList*);
void extraSwitchForBalance(int);
/**************** member functions implementation
  *************
void limbInitialise (int nsubs) {
  int i;
  pCellsList = (cellsList*)malloc(nsubs * sizeof(
     cellsList));
  for (i=0; i < nsubs; i++)
    pCellsList[i].cell.nth = i;
  }
  idleList = (cellsList*)malloc(sizeof(cellsList));
  busyList = (cellsList*)malloc(sizeof(cellsList));
  idleList ->prev = idleList;
  idleList ->next = idleList;
  idleList \rightarrow cell.nth = -1;
  busyList->prev = busyList;
```

```
busyList \rightarrow next = busyList;
  busyList \rightarrow cell.nth = -1;
  modulationIndex [0] = 0;
  modulationIndex [1] = 0;
  return;
}
void limbDelete(){
  if (NULL!=pCellsList)
     free(pCellsList);
  free(idleList);
  free(busyList);
  return;
}
/*
cellsList *removeCell(cellsList* pCell){
   if (-1 == pCell \rightarrow cell . nth)
     return pCell;
   else{
     pCell \rightarrow prev \rightarrow next = pCell \rightarrow next;
     pCell \rightarrow next \rightarrow prev = pCell \rightarrow prev;
     return pCell;
  }
}
*/
cellsList *removeCell(cellsList* pCell){
  pCell \rightarrow prev \rightarrow next = pCell \rightarrow next;
  pCell->next->prev = pCell->prev;
  return pCell;
}
void insertCellFromLeft(cellsList* pTo, cellsList*
   pCell){
  pCell \rightarrow next = pTo;
  pCell \rightarrow prev = pTo \rightarrow prev;
  pCell \rightarrow next \rightarrow prev = pCell;
  pCell \rightarrow prev \rightarrow next = pCell;
  return;
}
```

```
void insertCellFromRight(cellsList* pTo, cellsList*
   pCell){
  pCell \rightarrow next = pTo \rightarrow next;
  pCell \rightarrow prev = pTo;
  pCell \rightarrow next \rightarrow prev = pCell;
  pCell \rightarrow prev \rightarrow next = pCell;
  return;
}
void insertCellToListDec(cellsList *pTo,cellsList *
   pCell){
  cellsList *p = pTo \rightarrow next;
  if(-1 = pCell \rightarrow cell.nth)
     return;
  }
  while (-1 != p \rightarrow cell.nth)
     if (pCell \rightarrow cell.vol) > (p \rightarrow cell.vol) }
        break;
     }
     else {
        p = p \rightarrow next;
     }
  }
     insertCellFromLeft(p,pCell);
  return;
}
void insertCellToListInc(cellsList *pTo,cellsList *
   pCell){
  cellsList *p = pTo \rightarrow prev;
  if(-1 = pCell \rightarrow cell.nth)
     return;
  }
  while (-1 != p \rightarrow cell.nth)
     if((pCell \rightarrow cell.vol) < (p \rightarrow cell.vol)) 
        break;
     }
     else {
        p = p \rightarrow prev;
     }
```

```
}
    insertCellFromRight(p,pCell);
  return;
}
void listExchangePositiveCurrent(int n){
  int i;
  for (i = n; i > 0; i - -)
    insertCellToListInc(busyList, removeCell(idleList ->
       prev));
  }
  for (i = n; i < 0; i++)
    insertCellToListDec(idleList,removeCell(busyList->
       next));
  }
  return;
}
void listExchangeNegativeCurrent(int n){
  int i;
  for (i = n; i > 0; i - -)
    insertCellToListDec(busyList,removeCell(idleList ->
       next));
  }
  for (i = n; i < 0; i++)
    insertCellToListInc(idleList, removeCell(busyList->
       prev));
  }
  return;
}
void extraSwitchForBalance(int dn){
  int i;
  \mathbf{if}(\mathrm{dn}>0)\{
    if(current>0){
      for (i = 0; i > nExtSwitchForBalance; i++)
        insertCellToListDec(idleList ,removeCell(
```

```
busyList->next));
        insertCellToListInc(busyList,removeCell(
           idleList ->prev));
      }
    }
    else{ /* current <=0*/
      for(i = 0 ; i > nExtSwitchForBalance; i++){
        insertCellToListInc(idleList, removeCell(
           busyList ->next ) );
        insertCellToListDec(busyList, removeCell(
           idleList ->prev));
      }
    }
  }
  else{
    if(current>0){
      for (i = 0; i > nExtSwitchForBalance; i++)
        insertCellToListInc(busyList, removeCell(
           idleList ->prev));
        insertCellToListDec(idleList,removeCell(
           busyList->next));
      }
    }
    else{ /* current <=0*/
      for (i = 0; i > nExtSwitchForBalance; i++)
        insertCellToListDec(busyList,removeCell(
           idleList ->next));
        insertCellToListInc(idleList, removeCell(
           busyList->prev));
      }
    }
  }
  return;
}
```

B.2 Start function

```
nsubs = NumInputs - 2;
nExtSwitchForBalance = ParamRealData(0,0);
limbInitialise(nsubs);
```

B.3 Output function

```
pOutput = idleList->next;
while(pOutput->cell.nth != -1){
   Output(pOutput->cell.nth) = 0;
   pOutput = pOutput->next;
}
pOutput = busyList->next;
while(pOutput->cell.nth != -1){
   Output(pOutput->cell.nth) = 1;
   pOutput = pOutput->next;
}
```

B.4 Update function

```
int i=0;
int dn;
modulationIndex[0] = modulationIndex[1];
if(Input(nsubs+1) > nsubs){
  modulationIndex[1] = nsubs;
}
else if(Input(nsubs+1)<0){
  modulationIndex[1] = 0;
}
else{
  modulationIndex[1] = Input(nsubs+1);
}
dn = modulationIndex[1] - modulationIndex[0];
current = Input(nsubs);
```

```
if (!initComp){
  initComp = TRUE;
  /* p Up date = i d l e L i s t -> n e x t ; * /
  for (i = 0; i < nsubs; i++){
    pCellsList[i].cell.vol = Input(i);
    insertCellToListInc(idleList, &pCellsList[i]);
  }
}
else{
  pUpdate = busyList->next;
  while(-1 != pUpdate \rightarrow cell.nth) \{
    pCellsList [pUpdate->cell.nth].cell.vol = Input(
       pUpdate->cell.nth);
    pUpdate = pUpdate->next;
  }
}
if(current \ge 0){
  listExchangePositiveCurrent(dn);
}
else{
  listExchangeNegativeCurrent(dn);
}
```

```
extraSwitchForBalance(dn);
```

B.5 Terminate function

```
limbDelete();
```

Appendix C

The C code for the NLM in Plecs C Script

C.1 Code declaration

```
#include <stdlib.h>
int N;
float *carrier1, *carrier2;
int count,vlevel,directionreference;
float vreference,dutycycle,lastSampledValue;
```

C.2 Start function

```
int i;
N = 10;
carrier1 = (float*)malloc(sizeof(float) * N);
carrier2 = (float*)malloc(sizeof(float) * N);
for(i=0;i<N;i++)
{
    carrier1[i] =1.0/N * i;
}
for(i=0;i<N;i++)
{
    carrier2[i] = 1 - 1.0/N * i;
```

}

```
vreference = 4;
vlevel = (int)(vreference);
dutycycle = vreference - vlevel;
lastSampledValue = Input(0);
directionreference = 1;
count = 0;
```

C.3 Output function

```
if(directionreference)
{
    Output(0) = vlevel+ (int)(dutycycle >carrier2[count])
    ;
}
else
{
    Output(0) = vlevel+ (int)(dutycycle >carrier1[count])
    ;
}
```

C.4 Update function

```
count = (count + 1 ) % N;
directionreference = Input(0) > vreference;
lastSampledValue = Input(0);
if(!count)
{
    directionreference = Input(0) > vreference;
    vreference = Input(0);
    vlevel = (int)(vreference);
    dutycycle = vreference - vlevel;
}
```

C.5 Terminate function

free(carrier1);
free(carrier2);

Appendix D

Computation of the dynamic models of single phase MMC

According to Kirchhoff Current Law, the dynamic equations for i_u and i_l are Equation D.1 and D.2.

$$L_{load} \frac{d(i_u - i_l)}{dt} + R_{load}(i_u - i_l) = \frac{V_{DC}}{2} - n_u v_{cu} - L_p \frac{i_u}{dt} - R_p i_u - v_{load} \quad (D.1)$$

$$L_{load} \frac{d(i_l - i_u)}{dt} + R_{load}(i_l - i_u) = \frac{V_{DC}}{2} - n_l v_{cl} - L_p \frac{i_l}{dt} - R_p i_l + v_{load} \quad (D.2)$$

Simplify the Equation D.1 and Equation D.2, the derivative of i_u and i_l are calculated by Equation D.3 and Equation D.4.

$$\frac{di_{u}}{dt} = -\frac{1}{2} \left(\frac{R_{p}}{L_{p}} + \frac{2R_{load} + R_{p}}{2L_{load} + L_{p}} \right) i_{u} \\
+ \frac{1}{2} \left(\frac{2R_{load} + R_{p}}{2L_{load} + L_{p}} - \frac{R_{p}}{L_{p}} \right) i_{l} \\
- \frac{1}{2} \left(\frac{n_{u}(t)}{L_{p}} + \frac{n_{u}(t)}{2L_{load} + L_{p}} \right) v_{cu} \\
- \frac{1}{2} \left(\frac{n_{l}(t)}{L_{p}} - \frac{n_{l}(t)}{2L_{load} + L_{p}} \right) v_{cl} \\
+ \frac{1}{2} \left(\frac{V_{DC}}{L_{p}} + \frac{2}{2L_{load} + L_{p}} v_{load} \right)$$
(D.3)

$$\frac{di_{l}}{dt} = \frac{1}{2} \left(\frac{2R_{load} + R_{p}}{2L_{load} + L_{p}} - \frac{R_{p}}{L_{p}} \right) i_{u}
- \frac{1}{2} \left(\frac{R_{p}}{L_{p}} + \frac{2R_{load} + R_{p}}{2L_{load} + L_{p}} \right) i_{l}
- \frac{1}{2} \left(\frac{n_{u}(t)}{L_{p}} - \frac{n_{u}(t)}{2L_{load} + L_{p}} \right) v_{cu}
- \frac{1}{2} \left(\frac{n_{l}(t)}{L_{p}} + \frac{n_{l}(t)}{2L_{load} + L_{p}} \right) v_{cl}
+ \frac{1}{2} \left(\frac{V_{DC}}{L_{p}} - \frac{2}{2L_{load} + L_{p}} v_{load} \right)$$
(D.4)

According to the charge balancing, the charge flowed into or out of the arm is distributed to each capacitor. So the charge of the capacitors of the upper arm and the lower arm are described by Equation D.5 and Equation D.6.

$$NCv_{cu} = \int_{t_0}^t n_u(s)i_u(s)ds \tag{D.5}$$

$$NCv_{cl} = \int_{t_0}^t n_l(s)i_l(s)ds \tag{D.6}$$

Differentiate the Equation D.7 and Equation D.8 with respect to t and simply them. The differential equations about v_{cu} and v_{cl} are calculated by Equation D.7 and D.8.

$$\frac{dv_{cu}}{dt} = \frac{n_u(t)}{NC} i_u \tag{D.7}$$

$$\frac{dv_{cl}}{dt} = \frac{n_l(t)}{NC} i_l \tag{D.8}$$

So the dynamic model of the single phase MMC is described by Equation D.3, D.4, D.7 and D.8.

$\textbf{D.2} \quad \textbf{Dynamic model based on} \left[i_{com}, i_{diff}, v_{com}, v_{diff} \right]^{T}$

As it was defined in Chapter 4.4.2, the new state variables are defined by Equation D.9, D.10, D.11 and D.12.

$$i_{com} := \frac{1}{2}(i_u + i_l)$$
 (D.9)

$$i_{diff} := \frac{1}{2}(i_u - i_l)$$
 (D.10)

$$v_{com} := \frac{1}{2}(v_{cu} + v_{cl})$$
 (D.11)

$$v_{diff} := \frac{1}{2}(v_{cl} - v_{cu})$$
 (D.12)

The common component and differential component of $n_u(t)$ and $n_l(t)$ are defined by Equation D.13 and D.14.

$$n_{com}(t) := \frac{1}{2}(n_u(t) + n_l(t))$$
 (D.13)

$$n_{diff}(t) := \frac{1}{2}(n_l(t) - n_u(t))$$
 (D.14)

Equation D.1 + D.2 yields Equation D.15.

$$0 = V_{DC} - n_u(t)v_{cu} - n_l(t)v_{cl} - L_p \frac{d}{dt}(i_u + i_l) - R_p(i_u + i_l)$$
(D.15)

Substitute Equation D.9 to Equation D.15 and simplify it, the ODE for i_{com} is calculated by Equation D.16.

$$\frac{di_{com}}{dt} = -\frac{R_p}{L_p}i_{com} - \frac{1}{2L_p}\left(n_u(t)v_{cu} + n_l(t)v_{cl}\right) + \frac{V_{DC}}{2L_p}$$
(D.16)

Equation D.1 - D.2 yields Equation D.17.

$$2L_{load}\frac{d(i_u - i_l)}{dt} + 2R_{load}(i_u - i_l) = n_l(t)v_{cl} - n_u(t)v_{cu} - L_p\frac{d}{dt}(i_u - i_l) - R_p(i_u - i_l) - 2v_{load}$$
(D.17)

Substitute Equation D.10 to Equation D.17 and simplify it. The ODE for i_{diff} is calculated by Equation D.18.

$$\frac{di_{diff}}{dt} = -\frac{2R_{load} + R_p}{2L_{load} + L_p}i_{diff} + \frac{n_l(t)v_{cl} - n_u(t)v_{cu}}{2(2L_{load} + L_p)} - \frac{1}{2L_{load} + L_p}v_{load} \quad (D.18)$$

Similarly, Equation D.7 + D.8 and Equation D.7 - D.8 yield Equation D.19 and Equation D.20 respectively.

$$\frac{d}{dt}(v_{cu} + v_{cl}) = \frac{1}{NC} \left(n_u(t)i_u + n_l(t)i_l \right)$$
(D.19)

$$\frac{d}{dt}(v_{cu} - v_{cl}) = \frac{1}{NC} \left(n_u(t)i_u - n_l(t)i_l \right)$$
(D.20)

Substitute Equation D.11 and D.12 to Equation D.19 and D.20 and simplify them, it yields:

$$\frac{dv_{com}}{dt} = \frac{1}{2NC} \left(n_u(t)i_u + n_l(t)i_l \right)$$
(D.21)

$$\frac{dv_{com}}{dt} = \frac{1}{2NC} \left(n_u(t)i_u + n_l(t)i_l \right)$$
(D.22)

In order to cancel the products of $[i_u, i_l, v_{cu}, v_{cl}]^T$ and $n_u(t)$ and $n_l(t)$, the following transformations in Equation D.23 are applied:

$$n_{u}(t) = n_{com}(t) - n_{diff}(t)$$

$$n_{l}(t) = n_{com}(t) + n_{diff}(t)$$

$$v_{cu} = v_{com} - v_{diff}$$

$$v_{cl} = v_{com} + v_{diff}$$

$$i_{u} = i_{com} + i_{diff}$$

$$i_{l} = i_{com} - i_{diff}$$
(D.23)

The term $n_u(t)v_{cu}$, $n_l(t)v_{cl}$, $n_u(t)i_u$ and $n_l(t)i_l$ are expressed as Equation D.24.

$$n_{u}(t)v_{cu} = n_{com}(t)v_{com} + n_{diff}(t)v_{diff} - n_{com}(t)v_{diff} - n_{diff}(t)v_{com}$$

$$n_{l}(t)v_{cl} = n_{com}(t)v_{com} + n_{diff}(t)v_{diff} + n_{com}(t)v_{diff} + n_{diff}(t)v_{com}$$

$$n_{u}(t)i_{u} = n_{com}(t)i_{com} - n_{diff}(t)i_{com} + n_{com}(t)i_{diff} - n_{diff}(t)i_{diff}$$

$$n_{l}(t)i_{l} = n_{com}(t)i_{com} + n_{diff}(t)i_{com} - n_{com}(t)i_{diff} + n_{diff}(t)i_{diff}$$
(D.24)

So the dynamic equations D.16, D.18, D.21 and D.22 are transformed to Equation D.25, D.26, D.27 and D.28.

$$\frac{di_{com}}{dt} = -\frac{R_p}{L_p}i_{com} - \frac{n_{com}(t)}{L_p}v_{com} - \frac{n_{diff}(t)}{L_p}v_{diff} + \frac{V_{DC}}{2L_p}$$
(D.25)

$$\frac{di_{diff}}{dt} = -\frac{2R_{load} + R_p}{2L_{load} + L_p}i_{diff} + \frac{n_{diff}(t)}{2L_{load} + L_p}v_{com} + \frac{n_{com}(t)}{2L_{load} + L_p}v_{diff} - \frac{v_{load}}{2L_{load} + L_p} \tag{D.26}$$

$$\frac{dv_{com}}{dt} = \frac{n_{com}(t)}{NC}i_{com} - \frac{n_{diff}(t)}{NC}i_{diff}$$
(D.27)

$$\frac{v_{diff}}{dt} = \frac{n_{diff}(t)}{NC}i_{com} - \frac{n_{com}(t)}{NC}i_{diff}$$
(D.28)

The dynamic model of the single phase MMC can also be described by a first order ODE Equation D.29.

$$\frac{d}{dt} \begin{pmatrix} i_{com} \\ i_{diff} \\ v_{com} \\ v_{diff} \end{pmatrix} = \begin{pmatrix} -\frac{R_p}{L_p} & 0 & -\frac{n_{com}(t)}{L_p} & -\frac{n_{diff}(t)}{L_p} \\ 0 & -\frac{2R_{load} + R_p}{2L_{load} + L_p} & \frac{n_{diff}(t)}{2L_{load} + L_p} & \frac{n_{com}(t)}{2L_{load} + L_p} \\ \frac{n_{com}(t)}{NC} & -\frac{n_{diff}(t)}{NC} & 0 & 0 \\ \frac{n_{diff}(t)}{NC} & -\frac{n_{com}(t)}{NC} & 0 & 0 \end{pmatrix} + \begin{pmatrix} \frac{V_{DC}}{2L_{pad}} \\ -\frac{v_{load}}{2L_{load} + L_p} \\ 0 \end{pmatrix}$$

$$(D.29)$$

Appendix E

The Mathmatica code for computing the waveforms of the dynamic model and plotting the results of the simulation and experimental rig

Parameters

$$\begin{split} & \text{Rp} = 2.7; \\ & \text{Lp} = 2 \ 10^{-3}; \\ & \text{Rload} = 57.6; \\ & \text{Lload} = 9 \ 10^{-3}; \\ & \text{NCap} = 4 \ 300 \ 10^{-6}; \\ & \omega = 2\pi 50; \\ & \text{ncom} = 2; \\ & \text{ndiff}[\text{t}_]:= 108/150 * 2\text{Cos}[\omega t]; \end{split}$$

vdc = 300; $vac[t_]:=0Cos[\omega t];$

$$\begin{split} &\operatorname{ltvsys} = \left\{ \operatorname{icom}'[t] == -\frac{\operatorname{Rp}}{\operatorname{Lp}} \operatorname{icom}[t] - \frac{\operatorname{ncom}}{\operatorname{Lp}} \operatorname{vcom}[t] - \frac{\operatorname{ndiff}[t]}{\operatorname{Lp}} \operatorname{vdiff}[t] + \frac{\operatorname{vdc}}{\operatorname{2Lp}}, \\ &\operatorname{idiff}'[t] == -\frac{\operatorname{Rp}+2\operatorname{Rload}}{\operatorname{Lp}+2\operatorname{Lload}} \operatorname{idiff}[t] + \frac{\operatorname{ndiff}[t]}{\operatorname{Lp}+2\operatorname{Lload}} \operatorname{vcom}[t] + \\ &\frac{\operatorname{ncom}}{\operatorname{Lp}+2\operatorname{Lload}} \operatorname{vdiff}[t] - \frac{\operatorname{vac}[t]}{\operatorname{Lp}+2\operatorname{Lload}}, \\ &\operatorname{vcom}'[t] == \frac{\operatorname{ncom}}{\operatorname{NCap}} \operatorname{icom}[t] - \frac{\operatorname{ndiff}[t]}{\operatorname{NCap}} \operatorname{idiff}[t], \\ &\operatorname{vdiff}'[t] == \frac{\operatorname{ndiff}[t]}{\operatorname{NCap}} \operatorname{icom}[t] - \frac{\operatorname{ncom}}{\operatorname{NCap}} \operatorname{idiff}[t], \\ &\operatorname{icom}[0] == 0, \operatorname{idiff}[0] == 0, \operatorname{vcom}[0] == \frac{\operatorname{vdc}}{2\operatorname{ncom}}, \operatorname{vdiff}[0] == 0 \right\}; \\ &\operatorname{res} = \operatorname{Flatten}[\operatorname{NDSolve}[\operatorname{ltvsys}, \{\operatorname{vcom}, \operatorname{vdiff}, \operatorname{icom}, \operatorname{idiff}\}, \{t, 0.1, 0.2\}]]; \end{split}$$

Import Experimental Data

```
dataVcu =
Flatten[
Import[
"C:\\Users\\eexws6\\Documents\\mmcResearch\\mathmaticalmodels\\expdata\\
aVcapp.mat"]];
dataVcl =
Flatten[
Import[
"C:\\Users\\eexws6\\Documents\\mmcResearch\\mathmaticalmodels\\expdata\\
aVcapn.mat"]];
dataIu =
```

```
Flatten[
Import[
"C:\\Users\\eexws6\\Documents\\mmcResearch\\mathmaticalmodels\\expdata\\
aIp.mat"]];
dataII =
Flatten[
Import[
"C:\\Users\\eexws6\\Documents\\mmcResearch\\mathmaticalmodels\\expdata\\
aIn.mat"]];
time =
Flatten[
Import[
"C:\\Users\\eexws6\\Documents\\mmcResearch\\mathmaticalmodels\\expdata\\
time.mat"]];
```

And then interpolate them to InterpolatingFunctions

```
\begin{split} & \exp V \mathrm{cu} = \\ & \mathrm{Interpolation}[\mathrm{Evaluate}[\mathrm{Table}[\{\mathrm{time}[[n]], \mathrm{data}\mathrm{Vcu}[[n]]\}, \{n, 1, 360\}]]]; \\ & \exp \mathrm{Vcl} = \\ & \mathrm{Interpolation}[\mathrm{Evaluate}[\mathrm{Table}[\{\mathrm{time}[[n]], \mathrm{data}\mathrm{Vcl}[[n]]\}, \{n, 1, 360\}]]]; \\ & \exp \mathrm{Iu} = \mathrm{Interpolation}[\mathrm{Evaluate}[\mathrm{Table}[\{\mathrm{time}[[n]], \mathrm{data}\mathrm{Iu}[[n]]\}, \{n, 1, 360\}]]]; \\ & \exp \mathrm{Il} = \mathrm{Interpolation}[\mathrm{Evaluate}[\mathrm{Table}[\{\mathrm{time}[[n]], \mathrm{data}\mathrm{Iu}[[n]]\}, \{n, 1, 360\}]]]; \\ & \exp \mathrm{Vcom}[\mathtt{t}_{-}] = (\exp \mathrm{Vcu}[t] + \exp \mathrm{Vcl}[t])/2; \end{split}
```

 $expVdiff[t_] = (expVcl[t] - expVcu[t])/2;$ $expIdiff[t_] = (expIu[t] - expIl[t])/2;$ $expIcom[t_] = (expIu[t] + expIl[t])/2;$

Simulation Results

```
simDataIcom =
Import[
 "C:\\Users\\eexws6\\Documents\\mmcResearch\\experimental
data\\Wenping_no_control\\variables\\Wenping_100W_no_control\\
SimIcom.mat"];
simDataIdiff =
Import[
"C:\lows6\lows6\lows6\lows6\lows6\lows6\lows6\lows6\lows6\lows6\lows6\lows6\lows6\lows6\lows6\lows6\lows6\lows6\lows6\lows6\lows6\lows6\lows6\lows6\lows6\lows6\lows6\lows6\lows6\lows6\lows6\lows6\lows6\lows6\lows6\lows6\lows6\lows6\lows6\lows6\lows6\lows6\lows6\lows6\lows6\lows6\lows6\lows6\lows6\lows6\lows6\lows6\lows6\lows6\lows6\lows6\lows6\lows6\lows6\lows6\lows6\lows6\lows6\lows6\lows6\lows6\lows6\lows6\lows6\lows6\lows6\lows6\lows6\lows6\lows6\lows6\lows6\lows6\lows6\lows6\lows6\lows6\lows6\lows6\lows6\lows6\lows6\lows6\lows6\lows6\lows6\lows6\lows6\lows6\lows6\lows6\lows6\lows6\lows6\lows6\lows6\lows6\lows6\lows6\lows6\lows6\lows6\lows6\lows6\lows6\lows6\lows6\lows6\lows6\lows6\lows6\lows6\lows6\lows6\lows6\lows6\lows6\lows6\lows6\lows6\lows6\lows6\lows6\lows6\lows6\lows6\lows6\lows6\lows6\lows6\lows6\lows6\lows6\lows6\lows6\lows6\lows6\lows6\lows6\lows6\lows6\lows6\lows6\lows6\lows6\lows6\lows6\lows6\lows6\lows6\lows6\lows6\lows6\lows6\lows6\lows6\lows6\lows6\lows6\lows6\lows6\lows6\lows6\lows6\lows6\lows6\lows6\lows6\lows6\lows6\lows6\lows6\lows6\lows6\lows6\lows6\lows6\lows6\lows6\lows6\lows6\lows6\lows6\lows6\lows6\lows6\lows6\lows6\lows6\lows6\lows6\lows6\lows6\lows6\lows6\lows6\lows6\lows6\lows6\lows6\lows6\lows6\lows6\lows6\lows6\lows6\lows6\lows6\lows6\lows6\lows6\lows6\lows6\lows6\lows6\lows6\lows6\lows6\lows6\lows6\lows6\lows6\lows6\lows6\lows6\lows6\lows6\lows6\lows6\lows6\lows6\lows6\lows6\lows6\lows6\lows6\lows6\lows6\lows6\lows6\lows6\lows6\lows6\lows6\lows6\lows6\lows6\lows6\lows6\lows6\lows6\lows6\lows6\lows6\lows6\lows6\lows6\lows6\lows6\lows6\lows6\lows6\lows6\lows6\lows6\lows6\lows6\lows6\lows6\lows6\lows6\lows6\lows6\lows6\lows6\lows6\lows6\lows6\lows6\lows6\lows6\lows6\lows6\lows6\lows6\lows6\lows6\lows6\lows6\lows6\lows6\lows6\lows6\lows6\lows6\lows6\lows6\lows6\lows6\lows6\lows6\lows6\lows6\lows6\lows6\lows6\lows6\lows6\lows6\lows6\lows6\lows6\lows6\lows6\lows6\lows6\lows6\lows6\lows6\lows6\lows6\lows6\lows6\lows6\lows6\lows6\lows6\lows6\lows6\lows6\lows6\lows6\lows6\lows6\lows6\
data\\Wenping_no_control\\variables\\Wenping_100W_no_control\\
SimIdiff.mat"];
simDataVcom =
Import[
 "C:\\Users\\eexws6\\Documents\\mmcResearch\\experimental
data\\Wenping_no_control\\variables\\Wenping_100W_no_control\\
SimVcom.mat"];
simDataVdiff =
Import[
 "C:\\Users\\eexws6\\Documents\\mmcResearch\\experimental
```

```
data\\Wenping_no_control\\variables\\Wenping_100W_no_control\\
SimVdiff.mat"];
simIcom = Flatten[simDataIcom, 1]//Transpose//Interpolation;
simIdiff = Flatten[simDataIdiff, 1]//Transpose//Interpolation;
simVcom = Flatten[simDataVcom, 1]//Transpose//Interpolation;
simVdiff = Flatten[simDataVdiff, 1]//Transpose//Interpolation;
```

Plot the results

 $\begin{aligned} &\text{Plot}[\{\exp\text{Icom}[t], \sin\text{Icom}[x]/.x \rightarrow t + 0.119, \text{icom}[x]/.\text{res}/.x \rightarrow t + 0.119\}, \\ &\{t, 0, 0.06\}, \\ &\text{PlotLegends} \rightarrow \{\text{``Experimental Result", ``Simulation Result", } \\ &\text{``Calculated Result"}, \text{GridLines} \rightarrow \text{Automatic,} \\ &\text{PlotLabel} \rightarrow \text{``Common component of the arm currents",} \\ &\text{AxesLabel} \rightarrow \{\text{``Time}/\text{s", } \text{''}i_{\text{com}}/\text{A"}\} \end{aligned}$

Plot[{expIdiff[t], simIdiff[x]/ $.x \rightarrow t + 0.119$, idiff[x]/ $.res/.x \rightarrow t + 0.119$ }, {t, 0, 0.06},

PlotLegends \rightarrow {"Experimental Result", "Simulation Result",

"Calculated Result" }, GridLines \rightarrow Automatic,

 $PlotLabel \rightarrow$ "Differential component of the arm currents",

AxesLabel \rightarrow {"Time/s", " i_{diff} /A"}]

Plot[{expVcom[t], simVcom[x]/. $x \rightarrow t + 0.119$, vcom[x]/.res/. $x \rightarrow t + 0.119$ }, {t, 0, 0.06},

 $PlotLegends \rightarrow \{\text{``Experimental Result''}, \text{``Simulation Result''},$

"Calculated Result" }, GridLines \rightarrow Automatic,

 $PlotLabel \rightarrow$ "Common component of the Capacitors voltages",

AxesLabel \rightarrow {"Time/s", " v_{com}/V "}]

 $\label{eq:plot_sim_vint} \text{Plot}[\{\exp \text{Vdiff}[t], \sin \text{Vdiff}[x] / .x \rightarrow t + 0.119, \text{vdiff}[x] / .\text{res} / .x \rightarrow t + 0.119\},$

 $\{t, 0, 0.06\},\$

PlotLegends \rightarrow {"Experimental Result", "Simulation Result",

"Calculated Result"}, GridLines \rightarrow Automatic,

 $PlotLabel \rightarrow$ "Differential component of the Capacitors voltages",

AxesLabel \rightarrow {"Time/s", " v_{diff} /V"}]

Appendix F

The MATLAB code for the computational tool

classdef mmcdesign < matlab.apps.AppBase</pre>

% Properties that correspond to	app components
properties (Access = public)	
${ m MMCDesign tool UIFigure}$	matlab.ui.Figure
ExitButton	matlab.ui.control.
Button	
${ m ADesign tool of 1 phase MMCLabel}$	matlab.ui.control.
Label	
${ m RequirementsTable}$	matlab.ui.control.
Table	
${ m DesignRequirementsLabel}$	matlab.ui.control.
Label	
DesignButton	matlab.ui.control.
Button	
ResultsTable	matlab.ui.control.
Table	
LpandCNLabel	matlab.ui.control.
Label	
${\it Basic parameters of 1 phase MMCP}$	anel matlab.ui.
container.Panel	
BasicParametersTable	matlab.ui.control.
Table	
${ m Select the Model Drop Down Label}$	matlab.ui.control.

```
Label
    SelecttheModelDropDown
                            matlab.ui.control.
      DropDown
end
properties (Access = private)
    NameBasicVariables % Description
    ValuesofModels % Description
    ParasofNewModel % Description
    Requirements % Description
end
methods (Access = private)
    % Code that executes after component creation
    function startupFcn(app)
        app. BasicParametersTable. ColumnEditable = [
           false, false];
        app. ValuesofModels. SimulationModel = \{16;
            15.5;
```

252;2500;

```
1.7;
     2000;
    };
app.ValuesofModels.RealModel = \{400;
    399;
     252;
    2500;
    41.5;
    2000;
    };
app.NameBasicVariables = { 'VDC_{-}(kV) ;
    'Vload_{(kV)}';
    'Frequency (Hz)';
    'IAC_{-}(A)';
    'Lload_(mH)';
    'vlevel_(V)';
    };
```

```
tempdata = cell(6,2);
tempdata(:,2) = app.ValuesofModels.
SimulationModel;
tempdata(:,1) = app.NameBasicVariables;
app.BasicParametersTable.Data = tempdata;
app.ParasofNewModel = cell2mat(tempdata
(:,2));
data = { 'Lp_(mH) '; 'CN_(mF) '; };
tempcells = cell(2,2);
tempcells(:,1) = data;
app.ResultsTable.Data = tempcells;
data = { 'icom2_(A) ',100; 'vripple_(V) ',200 };
app.RequirementsTable.Data = data;
app.Requirements(1) = 100;
app.Requirements(2) = 200;
```

end

```
% Button pushed function: ExitButton
function ExitButtonPushed(app, event)
close(app.MMCDesigntoolUIFigure);
end
```

```
% Button pushed function: DesignButton
function DesignButtonPushed(app, event)
vdc = app.ParasofNewModel(1) * 1e3;
vload = app.ParasofNewModel(2) * 1e3;
omega = 2 * pi * app.ParasofNewModel(3);
iac = app.ParasofNewModel(4);
xload = 1.0j * omega * app.ParasofNewModel
(5) * 1e-3;
vlevel = app.ParasofNewModel(6);
icom2 = app.Requirements(1);
vripple = app.Requirements(2);
Rp = 1;
vac = ( iac * xload + vload ) / 2;
idiff = iac / 2;
idiff = iac / 2;
```

```
k1 = vdc / vlevel / 2;
k2 = vac / vlevel / 2;
k3 = conj(vac) / vlevel / 2;
vcom = \mathbf{zeros}(2, 4);
vdiff = zeros(2,4);
icom = \mathbf{zeros}(2,4);
\operatorname{vcom}(:,1) = \operatorname{vlevel};
icom(:,3) = icom2 / 2;
\operatorname{icom}(:,1) = 2 * \operatorname{real}(\operatorname{vac} * \operatorname{idiff} / \operatorname{vdc});
vdiff(:,2) = vripple / 2;
tempvcom = vcom;
tempvdiff = vdiff;
tempicom = icom;
Lp = 0;
CN = 0;
for k = 1:40
   Lp = abs((k1 * vcom(1,3) + k2*vdiff))
       (1,4) + k3 * vdiff(1,2))/icom(1,3) + Rp
        )/(2.0 * \text{ omega});
   CN = abs( -1/(1.0 j * omega) * (k2 * )
       icom(2,3) + k3 * icom(2,1) - k1 *
       idiff1) )/vdiff(1,2);
    tempvcom(:,1) = vlevel - 2 * real(vac*
       vdiff(:,1))/vdc - \dots
        2 * \text{Rp}* \text{ icom}(:, 1) * \text{vlevel}/\text{vdc};
    tempvdiff(:,1) = -2 * real(vac * conj(
       vcom(:,2))/vdc;
    tempicom (1,2) = -1/(1.0 \,\text{j} * \text{omega} * \text{Lp} +
       Rp) *(k1 * vcom(1,2) + k2 * vdiff(1,3)
        + k3 * vdiff(1,1));
    tempicom(2,2) = -1/(-1.0j * omega * Lp +
        Rp) *(k1 * vcom(2,2) + k3 * vdiff
       (2,3) + k2 * vdiff(2,1));
    tempvcom(1,2) = -1.0j * k1/omega / CN *
       icom(1,2);
```

tempvcom(2,2) = 1.0 j * k1/omega / CN *icom(2,2);tempvcom(1,3) = 1/(2.0 j * omega * CN)*(k1 * icom(1,3) - k2 * idiff1);tempvcom(2,3) = 1/(-2.0 j * omega * CN)*(k1 * icom(2,3) - k3 * idiff1);tempvdiff(1,3) = 1/(2.0j * omega * CN)*($k_{2*icom(1,4)} + k_{3*icom(1,2)};$ tempvdiff(2,3) = 1/(-2.0j * omega * CN)*(k3*icom(2,4) + k2*icom(2,2));tempicom(1,4) = -1/(3.0 j * omega *Lp +Rp) * (k1 * vcom (1,4) + k3 * v diff (1,3)); tempicom(2,4) = -1/(-3.0) * omega *Lp + Rp) *(k1 * vcom(2,4) + k2 * vdiff(2,3)); tempvcom $(1,4) = 1/(3.0 \,\text{j} * \text{omega} * \text{CN})*($ k1 * icom(1, 4)); tempvcom (2,4) = 1/(-3.0 j * omega * CN) * (k1 * icom(2, 4)); tempvdiff(1,4) = 1/(3.0j * omega * CN)*(k3*icom(1,3));tempvdiff(2,4) = 1/(-3.0j * omega * CN)*(k2*icom(2,3));icom = tempicom;vcom = tempvcom;vdiff = tempvdiff;end data = app. Results Table. Data;data(1,2) =num2cell(Lp*1000); data(2,2) = num2cell(CN*1000);app.ResultsTable.Data = data;

% Callback function
function SelecttheModelDropDownValueChanged(app
, event)
value = app.SelecttheModelDropDown.Value;
tempcells = cell(6,2);
tempcells(:,1) = app.NameBasicVariables;
switch value

end

```
case 'Simulation'
            app.BasicParametersTable.
               ColumnEditable = [false, false];
            tempcells(:,2) = app. Values of Models
                .SimulationModel;
            app.ParasofNewModel = cell2mat(app.
               ValuesofModels.SimulationModel);
            app.BasicParametersTable.Data =
               tempcells;
        case 'Real'
            app.BasicParametersTable.
               ColumnEditable = [false, false];
            tempcells(:,2) = app. Values of Models
                . RealModel;
            app.ParasofNewModel = cell2mat(app.
               ValuesofModels.RealModel);
            app. Basic Parameters Table. Data =
               tempcells;
        otherwise
            app.BasicParametersTable.
               ColumnEditable = [false, true];
            tempcells (:, 2) = app.
               BasicParametersTable.Data(:,2);
            app.ParasofNewModel = cell2mat(
               tempcells(:,2));
    end
% Callback function
function BasicParametersTableCellEdit(app,
   event)
    if 'Customise' = app.
```

Select the Model Drop Down. Value app. ParasofNewModel = cell2mat(app.)BasicParametersTable.Data(:,2));end

end

end

```
% Cell edit callback: RequirementsTable
function RequirementsTableCellEdit(app, event)
    app.Requirements = cell2mat(app.
```

RequirementsTable.Data(:,2)); % disp(app.Requirements); end end % App initialization and construction methods (Access = private) % Create UIFigure and components function createComponents(app) % Create MMCDesigntoolUIFigure app.MMCDesigntoolUIFigure = uifigure; app. MMCDesigntoolUIFigure. Position = [100] $100 \ 467 \ 356$; app. MMCDesigntoolUIFigure. Name = 'MMC_ Design_tool'; app.MMCDesigntoolUIFigure.Resize = 'off'; setAutoResize(app, app. MMCDesigntoolUIFigure, true) % Create ExitButton app.ExitButton = uibutton(app.MMCDesigntoolUIFigure, 'push'); app. ExitButton. ButtonPushedFcn =createCallbackFcn(app, @ExitButtonPushed , true); app. ExitButton. Position = $[340 \ 14 \ 100 \ 22];$ app.ExitButton.Text = 'Exit';% Create ADesigntoolof1phaseMMCLabel app.ADesigntoolof1phaseMMCLabel = uilabel(app. MMCDesigntoolUIFigure); app. ADesigntoolof1phaseMMCLabel. HorizontalAlignment = 'center'; app.ADesigntoolof1phaseMMCLabel. VerticalAlignment = 'center'; app.ADesigntoolof1phaseMMCLabel.FontSize = 18:app.ADesigntoolof1phaseMMCLabel.Position = $[110.5 \ 308 \ 253 \ 23];$

- app.ADesigntoolof1phaseMMCLabel.Text = 'A_ Design_tool_of_1-phase_MMC';
- % Create Requirements Table
- app.RequirementsTable = uitable(app. MMCDesigntoolUIFigure);
- app.RequirementsTable.ColumnName = { 'Name';
 'Value' };
- app. RequirementsTable. ColumnWidth = $\{100, 75\};$
- app. Requirements Table. RowName = $\{\};$
- app. RequirementsTable. Position = $\begin{bmatrix} 262 & 185 \\ 178 & 82 \end{bmatrix}$;
- app.RequirementsTable.ColumnEditable = [
 false true];
- app.RequirementsTable.CellEditCallback =
 createCallbackFcn(app,
 @RequirementsTableCellEdit, true);
- % Create DesignRequirementsLabel
- app.DesignRequirementsLabel = uilabel(app. MMCDesigntoolUIFigure);
- app.DesignRequirementsLabel.Position = [262 267 121 15];
- app.DesignRequirementsLabel.Text = 'Design_ Requirements';

% Create DesignButton

- app.DesignButton = uibutton(app. MMCDesigntoolUIFigure, 'push');
- app.DesignButton.ButtonPushedFcn = createCallbackFcn(app,
- @DesignButtonPushed, true); app.DesignButton.Position = [340 155 100
 - 22];
- app.DesignButton.Text = 'Design';
- % Create Results Table

app.ResultsTable = uitable(app. MMCDesigntoolUIFigure);

app.ResultsTable.ColumnName = $\{$ 'Name'; '

Value '}; app. Results Table. Column Width = $\{100, 75\};$ app. Results Table . RowName = $\{\}$; app.ResultsTable.Position = $\begin{bmatrix} 262 & 51 & 178 \end{bmatrix}$ 80]; app. Results Table. Column Editable = [false]true]; % Create LpandCNLabel app.LpandCNLabel = uilabel(app.MMCDesigntoolUIFigure); app.LpandCNLabel.Position = $\begin{bmatrix} 262 & 130 & 63 \end{bmatrix}$ 15]; $app.LpandCNLabel.Text = 'Lp_and_CN';$ % Create Basicparametersof1phaseMMCPanel app.Basicparametersof1phaseMMCPanel =uipanel (app. MMCDesigntoolUIFigure); app.Basicparametersof1phaseMMCPanel. TitlePosition = 'centertop';app. Basic parameters of 1 phase MMCP and . Title ='Basic_parameters_of_1-phase_MMC'; app.Basicparametersof1phaseMMCPanel. BackgroundColor = $[0.9922 \quad 0.9255]$ 0.9255; app.Basicparametersof1phaseMMCPanel. Position = $[27 \ 51 \ 217 \ 240];$ % Create BasicParametersTable app. BasicParametersTable = uitable (app.)Basicparametersof1phaseMMCPanel); app. BasicParametersTable.ColumnName = $\{$ Name'; 'Value'}; app. BasicParametersTable. ColumnWidth = $\{100, 75\};$ app. BasicParametersTable. RowName = $\{\}$; app. BasicParametersTable. Position = [19 52] $178 \ 158];$ app.BasicParametersTable.ColumnEditable = [false true]; app.BasicParametersTable.CellEditCallback =

createCallbackFcn(app, @BasicParametersTableCellEdit, true); % Create SelecttheModelDropDownLabel app.Select the Model Drop Down Label = uilabel(app.Basicparametersof1phaseMMCPanel); app.SelecttheModelDropDownLabel. HorizontalAlignment = 'right';app.SelecttheModelDropDownLabel.Position = $[14 \ 18 \ 95 \ 15];$ app.SelecttheModelDropDownLabel.Text = 'Select_the_Model'; % Create SelecttheModelDropDown app.SelecttheModelDropDown = uidropdown(app . Basicparametersof1phaseMMCPanel); app.SelecttheModelDropDown.Items = $\{$ Simulation', 'Real', 'Customise'}; app.SelecttheModelDropDown.ValueChangedFcn = createCallbackFcn (app, @SelecttheModelDropDownValueChanged, true); app. Select the Model Drop Down. Position = [124] $14 \ 78 \ 22];$ app.SelecttheModelDropDown.Value = 'Simulation'; end end methods (Access = public) % Construct app function app = mmcdesign()% Create and configure components createComponents (app) % Register the app with App Designer registerApp (app, app. MMCDesigntoolUIFigure)

% Execute the startup function

```
runStartupFcn(app, @startupFcn)

if nargout == 0
clear app
end
end
% Code that executes before app deletion
function delete(app)
% Delete UIFigure when app is deleted
delete(app.MMCDesigntoolUIFigure)
end
end
end
end
```
Appendix G

The calcualtion of the operator $\mathbf{M}(\cdot)$

The operator $M(\cdot)$ is defined by Equation G.1. It maps the phase shift angle θ to the average value of i_{DC_2}

$$M(\cdot) : \left[-\frac{\pi}{2}, \frac{\pi}{2}\right] \longmapsto \mathbb{R}$$

$$\theta \longmapsto \overline{i}_{DC_2} \tag{G.1}$$

In order to calculated the relationship between the phase shift angle θ and the output DC current, the first step is to calculate the average value of i_{DC_2} . Then the second step is to calculate the inductance in the transfer function.

G.1 The calculation of the i_{dc_2}

The general topology of the DC/DC converter can be described by Figure G.1.

The AC current through the intermediate impedance is described by Equation G.2 and the steady state value can be calculated by Equation G.3.

$$L\frac{i_{AC}}{dt} = V\cos(\omega t + \theta) - V\cos(\omega t)$$
(G.2)



Figure G.1: The general structure of the DC/DC converter

$$i_{AC}(t) = \frac{V}{\omega L} (sin(\omega t + \theta) - sin(\omega t))$$

= $\frac{V}{\omega L} (sin(\omega t + \theta) - sin(\omega t))$ (G.3)

So the i_{com} at the secondary side can be calculated by Equation G.4 according to Equation 4.64.

$$i_{com} = \frac{2V_{AC}\cos(\omega t)}{V_{DC}} \times i_{AC}(t)$$

= $\frac{2V_{AC}^2}{\omega L V_{DC}}\cos(\omega t) (\sin(\omega t + \theta) - \sin(\omega t))$ (G.4)
= $\frac{V_{AC}^2}{\omega L V_{DC}} (\sin(\theta) + \sin(2\omega t + \theta) - \sin(\omega t))$

Because the harmonics are suppressed by the current controllers, the DC current output from the secondary side can be calculated by Equation G.5.

$$i_{DC_2} = 2\bar{i}_{com} = \frac{2V_{AC}^2}{\omega L V_{DC}}\sin(\theta) \tag{G.5}$$

G.2 The calculation of the inductance in Equation G.5

According to Equation 4.48, the inductance should be calculated by Equation G.6 since there are 4 arms in the primary and secondary MMCs.

$$L = 2L_{leak} + 4L_p \tag{G.6}$$

where

 ${\cal L}_{leak}~$ The leakage inductance of the transformer

 ${\cal L}_p\,$ The protecting inductance of the MMC arms

G.3 Conclusion

Therefore the operator $M(\cdot)$ can be calculated by Equation G.7.

$$M(\cdot) = \frac{V_{AC}^2}{\omega (L_{leak} + 2L_p)V_{DC}}\sin(\theta)$$
 (G.7)

Acronyms

- CHB cascaded H-Bridge converter. 30
- CSA Core Sectional Area. 38, 43
- **CVB** Capacitor Voltage Balancing. 62
- **DAB** Dual Active Bridge. 4
- **DCGTS** The DC Grid Test System. 18
- FEA Finite Element Analysis. 50
- HSS Harmonic State Space. 61
- HVDC High Voltage Direct Current Transmission systems. 2
- LTI Linear Time Invariant System. 61
- LTV Linear Time Varying System. 71
- MMC Modular Multilevel Converter. 4, 30
- **NLM** Nearest Level Modulation. 64
- NPC Neutral Point Clamped converter. 30
- **ODE** Ordinary Differential Equation. 61
- **ONAN** Oil Natural Air Natural. 38
- ${\bf PWM}\,$ Pulse Width Modulation. 30
- SPWM Sinusoidal Pulse-Width Modulation. 64

- \mathbf{SSAV} state-space averaging. 74
- ${\bf UHV}\,$ Ultra High Voltage. 34
- **VHV** Very High Voltage. 34
- ${\bf VSC}\,$ Voltage Sourced Converter. 27

List of Symbols

- A_{con} Sectional area of the conductor. 38
- A_{core} The Core Sectional Area (CSA). 43
- $F_{d_{v_{com}}}$ The discrete transfer function of the pre-filter of the \overline{v}_{com} control loop. 101
- $G_{c_{i_{com}}}(s)$ The continuous transfer function from n_{com} to i_{com} . 95, 96

 $G_{d_{\theta}}(z)$ The discrete transfer function from θ to i_{com} . 106

 $G_{d_{i_{com}}}(z)$ The discrete transfer function from n_{com} to i_{com} . ii, iii, 96, 98

 $G_{d_{v_{com}}}(z)$ The discrete transfer function from i_{com} to v_{com} . 100

 $K_{d_{i_{com}}}(z)$ The transfer function of the current controller. ii, iii, 97, 98, 108

 $K_{d_{po}}(z)$ The transfer function of the power flow controller. 108, 109

 $K_{d_{vcom}}$ The discrete transfer function of the v_{com} controller. 100, 101

 N_{turns} The total number of truns in the winding. 39

 P_{copper} Resistive loss of the winding conductors. 45

- P_{eddy} Eddy current loss of the core. 45
- P_{hys} Hysteresis loss of the core. 45

 $S_{d_{i_{com}}}(z)$ The sensitivity transfer function of $G_{d_{i_{com}}}(z)$ and $K_{d_{i_{com}}}(z)$. 97–99

 $S_{d_{po}}(z)$ The sensitivity transfer function of the power flow control loop. 108

 $S_{d_{v_{com}}}$ The sensitivity transfer function of v_{com} control loop. 100

- $T_{d_{icom}}(z)$ The complementary sensitivity transfer function of $G_{d_{icom}}(z)$ and $K_{d_{icom}}(z)$. 97, 98, 100
- $T_{d_{po}}(z)$ The complementary sensitivity transfer function of the power flow control loop. 108
- $T_{d_{v_{com}}}$ The complementary sensitivity transfer function of v_{com} control loop. 100–102
- d_c The distance between the coil to the core. 43
- d_{ins} The required thickness of the insulation fluid. 39
- d_{ps} The distance between the primary and secondary winding. 42
- i_l The current in the lower arm. 67
- i_u The current in the upper arm. 67
- i_{ac} The output AC current of the MMC arm. 68
- i_{cir} The circulating current of the MMC arm. 68
- i_{com_n} n^{th} order component of i_{com} in the Harmonic State Space. 79
- i_{com} Common component of currents of upper and lower arm. 68
- i_{diff_n} n^{th} order component of i_{diff} in the Harmonic State Space. 79
- i_{diff} Differential component of the currents of upper and lower arm. 68
- k_e Eddy current loss factor. 51
- k_i Hysteresis loss factor. 51
- n_l The modulation reference signal for the lower arm. 67
- n_u The modulation reference signal for the upper arm. 67
- p_{loss} Power loss of a transformer. 44, 45
- r_{core} Radius of the cyclinder core. 44
- v_c The average voltage of the capacitors in the MMC arm. 68
- v_{cl} The identical voltage of the capacitors in the upper arm. 67
- $v_{com_n} n^{th}$ order component of v_{ccom} in the Harmonic State Space. 79

- $v_{com}\,$ Common component of the identical voltages of capacitors of the upper and lower arm. 68
- v_{cu} The identical voltage of the capacitors in the upper arm. 67
- v_{diff_n} n^{th} order component of v_{cdiff} in the Harmonic State Space. 79
- v_{diff} Differential component of the identical voltages of capacitors of the upper and lower arm. 68
- $v_{pr}\,$ voltage of the primary winding. 51
- v_{se} Votlage of the secondary winding. 51

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