Electric Power Components and Systems, 00:000–000, 2012

0731-356X / 12 $12.00 + .00

A Variable Current-Limit Control Scheme for a Bi-directional Converter used in Ultracapacitor Applications

Behzad Ahmadi[1], Farhad Barati[2], Charif Karimi[3]

[1] Power Electronics, Machines and Control Group, Faculty of Engineering, University of Nottingham, Nottingham, U.K.

[2] Energy Department, Materials & Energy Research Center, Tehran, Iran.

[3] SUPELEC, Department of Power & Energy Systems, Supelec,Gif-sur-Yvette, France.

In ultracapacitor applications, generally, a bi-directional converter is connected to a DC bus and is designed to compensate rapid load variations on the bus. During transient phases, overloaded DC bus can push the converter out of its operating limits. For providing the necessary power, converters should be put in parallel, while each converter is limited into its optimal operating range. In a boost converter this operating limit can be related to the inductor current and UC voltage. In this study, a variable current-limit is proposed for inductor current which then determines the operating range of the boost converter. This method will provide stability of the converter during overload transients. An experimental setup consisting of a bi-directional converter, a controllable load/source and an ultracapacitor is presented, to validate the proposed method. Several scenarii are applied to analyse the performance of the system in overloaded phases and theoretical and experimental results are presented.

Manuscript received in final form on xx, xxx.

behzad.ahmadi@nottingham.ac.uk

1 Introduction

DC. micro grids are present in most of modern electrical systems. Embedded electrical networks in electric vehicles [1], power management in residential/industrial applicaions [2], [3] and renewable energy networks are only few examples of these grids, in which key elements for energy management are bi-directional DC-DC converters. An important role of bi-directional converters, in this regard, is to stabilize the voltage of various DC buses in these networks. So often, several high dynamic loads are fed by a DC bus. These loads could be connected in different laps of time and might make abrupt variations of injected or absorbed currents into or out of the DC bus. Usually, an ultracapacitor (UC) module is connected to the DC bus via a bi-directional converter to provide voltage stability of this DC bus, in transients. Design of high efficient converters and studying their dynamic behaviour, are important issues in this domain [4].

A new trend in energy management of low voltage micro grids, is to use UC modules and associated bi-directional converters, to regulate bus voltage [5], [6]. A simplified configuration of this strategy in a DC micro grid, is shown in Fig. 1. In this configuration, the bi-directional converter controls the voltage of the DC bus while other converters and loads are connected to the bus in current control mode. In [7] the energy source is a substation rectifier and a bi-directional converter coupled with UC unit is used to compensate the line voltage at weak points. In the case of [6], the energy source is a fuel cell which can only provide the mean power to the load. Thed UC module and its dedicated converter are designed to maintain the fuel cell current slope and its maximum value within the safe operating range. These studies, however, consider that UC converter operates within its boundary

limits.

In these applications, UCs are considered to be used in 2:1 voltage range, which means 75 % of stored energy can be retrieved [8]. Since boost converters suffer from limited gain in high power applications, reduced input voltage (i.e. low UC voltage) becomes problematic for maintaining bus voltage in higher powers and transient overloads. The analysis of the UC converter, at boundary conditions is investigated in this paper and an optimal solution is presented.

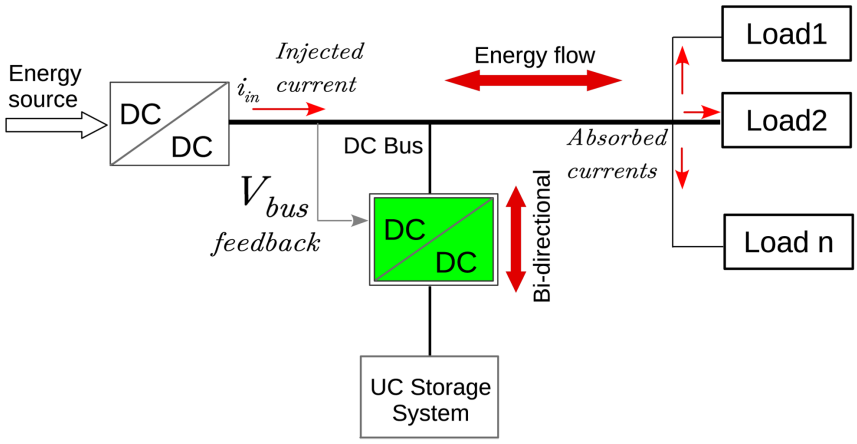


Figure 1. A simplified structure of a DC micro-grid. Input converter injects current into DC bus on one side and several loads absorb/inject currents on the other side. Bi-directional converter connected to the UC unit, maintains the voltage stability of the DC bus.

In fact, operating range (in other words, duty cycle) of the bi-directional boost converter, should be limited before reaching its maximum gain point, to maintain the stability of the bus voltage (this point will be addressed in details in Sec 2). Maximum gain of a boost converter depends on its input power [9]. Input power is the product of UC voltage and input inductor current, then both of these factors

will, independently, affect the maximum gain of the converter. Increasing inductor current has a negative effect on gain and efficiency [10] and in [11] implementation options for inductor current limiter, based on synergic control, are presented. A mixed analogue/digital technique is presented in [12] for controlling maximum inductor current in boost converters. Operating limits of a boost converter in discontinuous operating mode is investigated in [13] and a law for limiting the duty cycle is obtained. This limit, however, depends on inductance of the converter and switching frequency.

In this paper, the proposed solution for limiting the duty cycle depends on the input voltage (UC voltage) which is monitored in real time by the control system. This method is proposed to maintain the stability of the converter, in short transient overloads, while exploiting the maximum range of the duty cycle. This will also provide a solution for parallel implementation of boost converters [14], [15]: Each converter can operate up to its stable operating range.

In section 2, steady state analyses alongside with experimental verifications are considered for determining operating limits of a bi-directional converter. Based on these results, a suitable controller structure will be proposed in section 3. Dynamic behaviour of the system is investigated in 4 and experimental verification of the controller is presented in section 5.

2 Boost converter analysis: Limits of operation

2.1 Theoretical basis

Structure of bi-directional buck/boost converter, used in this experiment is shown in Fig. 2-a. An ultracapacitor module (UC) is connected to the input inductor and

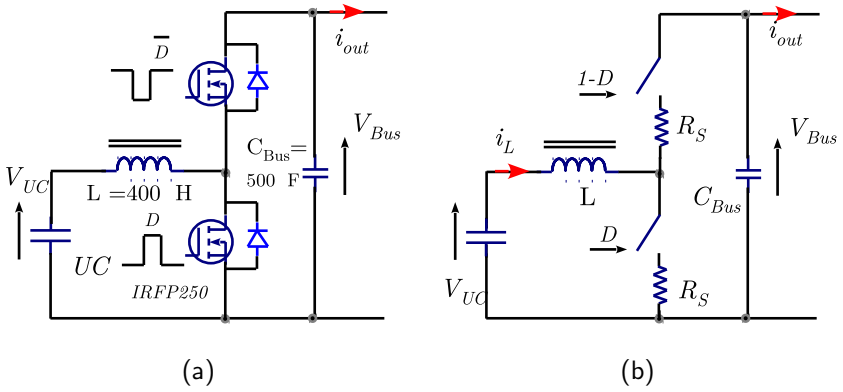


Figure 2. a) Structure of the bi-directional converter. b) Simplified model for analysing boost converter behaviour in bi-directional mode.

other end of the converter is connected to a 48 V DC bus with 500 μF capacitance. In *forward* operating mode (boost), power flow is from the UC to the bus and both i_{out} and i_L take positive values. In *reverse* operating mode (buck), these currents take negative values and flow from the bus to UC.

Simplified model of the bi-directional converter, used in this paper, is shown in Fig.2-b. In this section, analyses are performed for steady state operating points. For this analysis, demanded current on the DC bus, i_{out}, is independent from v_{Bus} and is determined by the load, meaning that loads are not necessarily supposed to represent simple resistive behaviour.

Losses in the converter are represented by two series resistances with identical values. This configuration is selected due to symmetrical structure of bi-directional converter: gate signals are provided in a complementary way and current passes through a switch while its gate signal is in high state and channel of the MOSFET is conducting (except from the dead time between two gate signals). More

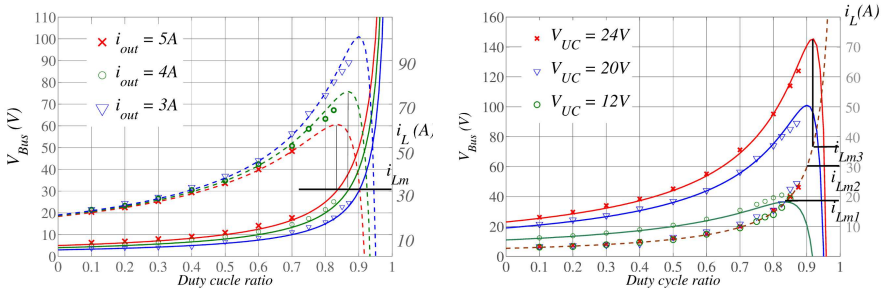
complicated loss models, are already presented [16] [17], which consider different resistances for representing losses in converter, however, analysis in this section will show that the precision of the considered model (Fig.2-b) would be sufficient for the purpose of targeted applications.

In steady state, governing equations of the converter, can be obtained by writing average voltage of the inductor and average current of the capacitor over a switching cycle. These average values should be zero in steady state, therefore, one can obtain equations (1). In this equation, $\bar{i}_L$ and $\bar{i}_{out}$, are average inductor and output currents on a switching period respectively and D represents the duty cycle ratio of the converter.

$$V_{bus} = \frac{V_{uc} - \bar{i}_L R_s}{1 - D} \qquad (1)$$
$$\bar{i}_{out} = \bar{i}_L \cdot (1 - D)$$

It is worthwhile to mention that, as the converter is bi-directional, we only have to deal with continuous operating mode; unlike the uni-directional boost where the converter can also move to discontinuous operating zone. This is due to the fact that $\bar{i}_{out}$ and $\bar{i}_L$ can take negative values and the model is then valid for both *forward* and *reverse* modes of operation.

For a given output current, $\bar{i}_{out}$, and ultracapacitor voltage, V_{uc}, maximum bus voltage can be obtained by writing $\partial V_{bus}/\partial D = 0$. This maximum voltage gain then corresponds to a duty cycle ratio, named D_m, and consequently to a specific inductor current, $\bar{i}_{Lm}$, given by (2).



(a) (b)

Figure 3. Calculation and experimental results: Bus voltage and inductor current for different values of Duty cycle. a) Constant ultracapacitor voltage ($V_{uc} = 20\ V$), different output current levels b) Constant output current level ($i_{out} = 3\ A$), various ultracapacitor voltages.

$$D_m = 1 - 2\frac{\bar{i}_{out}R_s}{V_{uc}}, \quad \bar{i}_{Lm} = \frac{V_{uc}}{2R_s} \tag{2}$$

These limits of operating range should be imposed to maintain the stability of boost converter. If the duty cycle ratio goes beyond D_m, the stability of controller could no more be guaranteed. In fact, in order to increase the bus voltage, controller always increases D, while beyond D_m bus voltage will decrease.

It can be noticed that this limit can be imposed by limiting $\bar{i}_L$ and on the other hand, model indicates that, for a given converter, this limit value depends only on ultracapacitor voltage. Fig. 3-a shows that this current limit is independent of $\bar{i}_{out}$ and Fig. 3-b shows that it will change by variation of ultracapacitor voltage. It can then be suggested that in *forward* mode, the controller should also have access to V_{uc} and be able to impose adequate limits on inductor current.

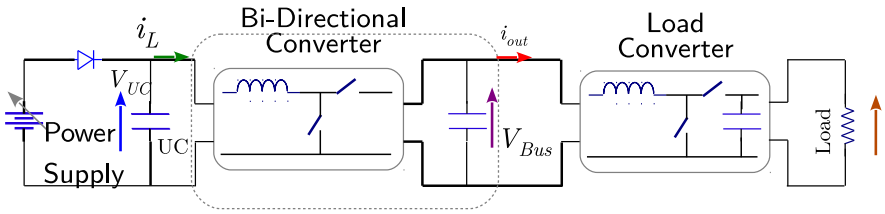


Figure 4. Experimental setup: imposing constant output current on DC bus, measurements are made in a constant duty cycle ratio.

In *reverse* mode, the described model is still valid, however, behaviour of the converter is different. DC bus is considered as the energy source and injects current into the bi-directional converter. Converter will charge the ultracapacitor, which is at a lower voltage level, and attempts to regulate the voltage of the DC bus. As in this situation converter operates in step-down mode, no maximum gain could then be imagined.

Constraints, in this mode, are mainly determined by ultracapacitor characteristics such as maximum voltage and over current and not by stable operating range of the converter.

2.2 Experimental verification

In order to verify the validity of the model (Fig. 2-b), an experimental setup is developed (Fig. 7) and is explained in more details in Sec. 5.1. In this section, bi-directional converter is connected between ultracapacitor and bus capacitor and controller provides gate pulses with constant duty cycle ratios for this converter. A power supply is connected to the ultracapacitor to maintain its voltage constant and as shown in Fig. 4-a, current i_{out} is absorbed from the bus.

Two series of measurements are performed: first by keeping constant $V_{uc} = cte$, and measuring $\bar{i}_L$ and V_{Bus} for different D and $\bar{i}_{out}$; second with maintaining constant $\bar{i}_{out}$ and measuring same quantities for various D and V_{uc}.

To prevent overheating of components and changes in characteristics of the converter, output current is maintained at the specified level for a tiny period of time (1.25 s). As this sequence is adjusted by DSP controller, signals rise and fall precisely at same instants. This repeatability of measurement sequences permits performing average over several measurements to obtain a more reliable result.

Measurement results are shown in Fig. 3. First series of measurements ($V_{uc} = 20\ V$ different values of $\bar{i}_{out}$), are shown in Fig. 3-a. Value of R_s is selected in a way that V_{Bus} curve fits with experimental measurements. It can be observed that, once R_s is identified by fitting a V_{Bus} curve in a given value of $\bar{i}_{out}$, other V_{Bus} curves corresponding to various values of output current, will coincide with measurements. In this test, $R_s = 0.33\ \Omega$, is fitted with $V_{Bus} = 20V$ and $\bar{i}_{out} = 3A$, voltage curve.

Second series of measurements ($\bar{i}_{out} = 3\ A$ different values of V_{uc}), are shown in Fig. 3-b. For the same value of $R_s = 0.33\ \Omega$, experimental curves show a good agreement with the model. It can be observed that for $V_{uc} = 12V$, V_{Bus} is underestimated, while for $V_{uc} = 24V$, V_{Bus} is slightly overestimated by the model. This observation suggests that the considered boost model (Fig. 2-b) is valid for a limited range of ultracapacitor voltages. Although this limited validity, this model can be used for ultracapacitor applications. V_{uc} is usually varied from its nominal voltage to 50% of this value and identification of R_s could be performed at the middle point of this voltage range (i.e. $V_{uc} = 75\% V_{uc-nominal}$).

Within the operating range of the converter, experimental results are close to the-

oretical calculations. This validates the proposed limit (Eq. 2) on inductor current, for ultracapacitor applications.

3 Structure of the Current limiter

Structure of the controller, proposed for bi-directional converter, is shown in Fig. 5. It consists of two loops with PI controllers, an inner current loop, named *i-loop*, getting its feedback from inductor current and an outer voltage loop, named *v-loop*, with a feedback from bus voltage. Kf_i and Kf_v are coefficients of measurements and A/D conversion for current and voltage loops, respectively. K_{pwm} is the gain of PWM in the experimental setup.

Output of the *v-loop* controller acts as a reference for the inductor current, then a hard limit is imposed on this output to limit the reference current smaller than $V_{uc}/2R_s$, according to (2). This function should be implemented by reading V_{uc} and calculating the appropriate limit, $\bar{i}_{Lm}$, at the beginning of each switching cycle. An appropriate anti-windup scheme is also implemented into the controller and is explained in Sec. 4.2.

Two points should be studied in more details: First, is to verify whether the *i-loop* controller is sufficiently precise to control the inductor current and then impose the desired limit on this current (Sec. 4). Second point is to show if the variable limit, which depends on measured V_{uc}, can guarantee the stability of the converter in practical implementation (Sec. 5).

From two parts of equation (1), one can obtain:

$$V_{Bus}.\bar{i}_{out} = V_{uc}.\bar{i}_L - \bar{i}_L^2.R_s \tag{3}$$

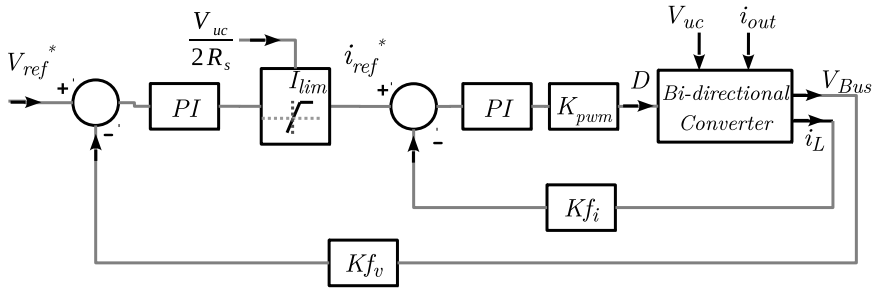


Figure 5. Two-loop structure, with inner current loop, considered for controlling the bi-directional converter.

In *forward* mode, considering input and output powers as $P_{in} = V_{uc}.\bar{i}_L$ and $P_{out} = V_{Bus}.\bar{i}_{out}$, Efficiency of the converter, $\eta_f = P_{out}/P_{in}$ can be written as:

$$\eta_f = 1 - \frac{\bar{i}_L \cdot R_s}{V_{uc}} \tag{4}$$

In *reverse* mode, Equation (1) is still valid, however, since both $\bar{i}_L$ and $\bar{i}_{out}$ takes negative values, Equation (3) is written as: $V_{Bus}.|\bar{i}_{out}| = V_{uc}.|\bar{i}_L| + \bar{i}_L^2.R_s$. Input and output powers should now be considered as $P_{in} = V_{Bus}.|\bar{i}_{out}|$ and $P_{out} = V_{uc}.|\bar{i}_L|$,which gives the efficiency of the converter in *reverse* mode, η_r, as:

$$\eta_r = 1 - \frac{|\bar{i}_L| \cdot R_s}{V_{uc} + |\bar{i}_L| \cdot R_s} \tag{5}$$

For the *reverse* mode, no limit is imposed on the converter due to stability issues and the inductor current can be obtained by:

$$\bar{i}_L = \frac{-V_{uc} + \sqrt{{V_{uc}}^2 + 4R_s V_{Bus} \cdot |\bar{i}_{out}|}}{2R_s} \tag{6}$$

while in *forward* mode, the maximum inductor current is limited to $V_{uc}/2R_s$ (Eq. (2)) by the controller. Before reaching to this limiting point, by solving equation (3) for $\bar{i}_L$, inductor current can be calculated as:

$$\bar{i}_L = \frac{V_{uc} - \sqrt{{V_{uc}}^2 - 4R_s V_{Bus} \cdot \bar{i}_{out}}}{2R_s} \tag{7}$$

Equation (4) suggests that efficiency of the converter decreases linearly by $\bar{i}_L$ and when $\bar{i}_L = i_{Lm}$, reaches to $\eta_f = 1/2$. Further increase in output current, $\bar{i}_{out}$, after this point will result in bus voltage drop, but efficiency of the converter, $\eta_f = (V_{Bus} \cdot \bar{i}_{out})/(V_{uc} \cdot i_{Lm})$ will remain at 50 %. In other words, limiting the inductor current will limit further drop of the converter's efficiency. It should be noticed that this limit considers stability of the controller, but proper thermal design of the converter is necessary to tolerate 50 % loss of input power.

4 Analysis & design of the controller

4.1 Boost converter dynamics

The model presented in Fig. 2-b is considered to analyse dynamic behaviour of the converter. State-space average model of this structure can be written as (8), with inductor current $\bar{i}_L$ and bus voltage v_{Bus} considered as state variables, output current $\bar{i}_{out}$ and ultracapacitor voltage v_{uc} as input parameters. R_s is the identified series resistance in steady state. In these analyses, $\bar{i}_{out}$ is determined by the load and no direct dependency on v_{Bus} is considered for this current. It should also be mentioned that, v_{uc} is determined by the ideal capacitor equation: $v_{uc} = V_{uc0} + 1/C_{uc} \int i_{uc} \cdot dt$.

$$\frac{d}{dt}\begin{pmatrix} \bar{i}_L \\ \\ v_{Bus} \end{pmatrix} = \begin{pmatrix} -\frac{R_s}{L} & -\frac{1-D}{L} \\ \\ \frac{1-D}{C_{Bus}} & 0 \end{pmatrix} \cdot \begin{pmatrix} \bar{i}_L \\ \\ v_{Bus} \end{pmatrix} + \begin{pmatrix} \frac{1}{L} & 0 \\ \\ 0 & -\frac{1}{C_{Bus}} \end{pmatrix} \cdot \begin{pmatrix} v_{uc} \\ \\ \bar{i}_{out} \end{pmatrix} \quad (8)$$

Analysis is performed by finding numerical solutions of Ordinary Differential Equations (ODE)(8) by a numerical solver (ode45 in Matlab ®).

Calculations for PI controller are performed according to Equation (9); with $y_I(n)$ output of the integrator and $y(n)$ output of the PI controller. e(n) is the error between reference signal and feedback signal at each switching cycle, K_i and K_p are integrator and proportional coefficients, respectively. This program is the basis for analyses in the following sections.

$$y_I(n) = y_I(n-1) + \frac{K_i}{f_{sw}} \cdot e(n) \quad (9)$$
$$y(n) = y_I(n) + K_p \cdot e(n)$$

4.2 Dynamics of the controller in transient saturated zone

In this section, behaviour of the controller in an overloaded transient is investigated. As indicated in sec. (2), theoretically, maximum inductor current is determined by Equation (2). A current limiter, therefore, is implemented in the controller (Fig. 5) to guarantee this current limit.

The scenario implemented for the calculations in this section is shown on Fig. 6: Bus voltage is established at 48 V, output current then will go through an overload

interval before settling at its final value. In this transient interval, inductor current will reach its maximal value and i^*_{ref} will be limited to prevent further increase of the inductor current, $\bar{i}_L$. In this interval, *v-loop* controller will be simply written as (10) to prevent windup effect of the integrator. Latest value of the integrator, before saturation, will be saved into the controller. This value will then be set as initial value of the integrator, y(n-1), when controller moves out from the saturated zone. This is equivalent of restoring the same value of i^*_{ref} after saturated transient, as before this interval.

$$y(n) = (K_p + \frac{K_i}{f_{sw}}) \cdot e(n) \tag{10}$$

Fig. 6-a shows the calculated behaviour of the system: $\bar{i}_{out}$ reaches 9 A in transient mode before settling to 5 A in steady state. Inductor current is limited to 80% of its theoretical limit, which is equivalent to limit the efficiency of the converter to 60%. This safety factor is selected, first to provide a further margin from the instability point and second due to considerations on thermal design of the converter in practical situation.

This transient overload test is then applied to two specific cases: different overload currents and different $d\bar{i}_{out}/dt$ (Fig. 6-b) different overload currents and same $d\bar{i}_{out}/dt$ (Fig. 6-c)

Fig. 6-b compares two overloaded transient phases with different current slope rates. First is 0.5-9.5 A with 450 A/s rising/falling rates and second is 0.5-15.5 A with 750 A/s rising/falling rates. Since the controller dynamic is the same for two cases, bus voltage overshoot after saturation transient, is more important in the

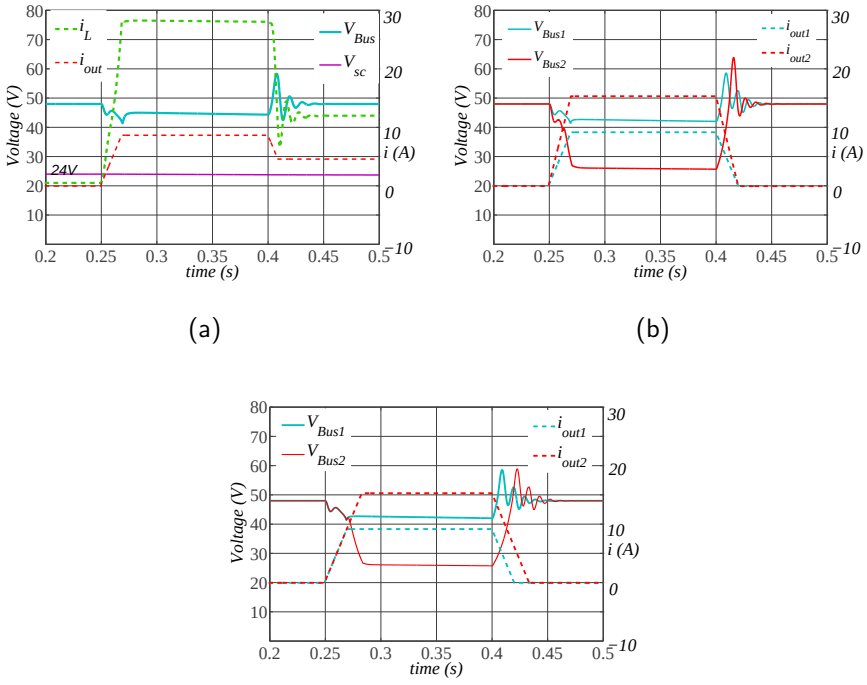


Figure 6. Simulation results: *i-loop*: $K_p = 1$, $K_i = 500$, *v-loop*: $K_p = 1$, $K_i = 2800$ a) Behaviour of controller in saturated transient. Ultra capacitor voltage variation is very small b) Overload transients with different $d\bar{i}_{out}/dt$ c) Overload transients with the same $d\bar{i}_{out}/dt$.

case with higher $d\bar{i}_{out}/dt$. This effect is due to intrinsic limit of the controller, where effect of high dynamic loads is more complicated to manage.

The proposed controller structure, however, provides an interesting feature for transient overloads with same dynamics $d\bar{i}_{out}/dt$. In Fig. 6-c, two current ramps with same slopes, $d\bar{i}_{out}/dt = 450\ A/s$, but different magnitudes: 0.5-9.5 A and 0.5-15.5 A, are compared. In the case of 15.5 A ramp, bus voltage drop is more important in overloaded interval. However, it can be noticed that the bus voltage overshoot remains unchanged comparing to the smaller load ramp of 9.5 A. As mentioned in Sec. 3, limiting the inductor current is equivalent to limiting the lowest efficiency of the converter. In these circumstances, for a given ultracapacitor voltage, maximum input power is already fixed and maximum output power is then determined, regardless of amplitude of output current. In other words, in saturated transient, converter is run in constant input and output power modes, determined by ultracapacitor voltage. For this structure of controller, design should then be performed on the basis of estimated dynamics of overloads rather than their amplitudes.

5 Experimental validation

5.1 Experimental setup

The developed experimental setup is shown in Fig. 7-a. In this setup, the main bi-directional converter is connected between ultracapacitor and bus capacitor. Second bi-directional converter, named *load converter*, is connected to the bus capacitor to absorb/inject the desired current from/into this bus (i.e. $\bar{i}_{out}$). Both converters

have the same structures, as shown in Fig. 2-a.

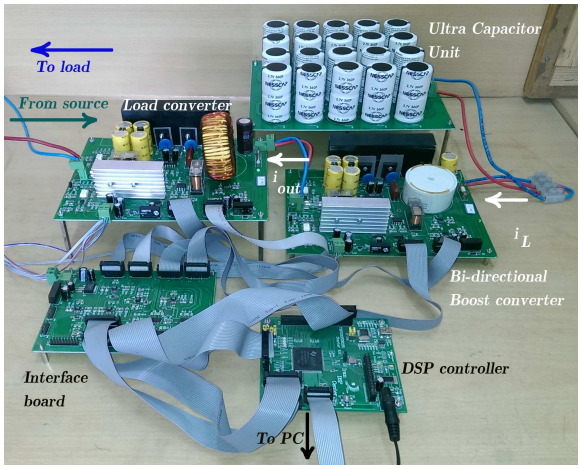
Due to practical constraints in the laboratory, a reduced scale system been developed for experimental verifications. Characteristics of this setup, are summerized in table 1. Although this method is represented for general DC micro-grid applications, due to the constraints in our laboratory, we reduced the scale of the system. In fact, the behaviour of the controller and the proposed technique is not affected by this scale change.

	Inductance	Nominal V_{in}	Nominal V_{out}	Switching freq.
bi-directional	400 μH	24 V	48 V	20 kHz
load conv.	2 mH	48 V	nc	20 kHz
Ultracapacitor unit				
Individual cell cap.	Number of cells	Total cap.	Nominal voltage	
360 F	20	18 F	24 V	

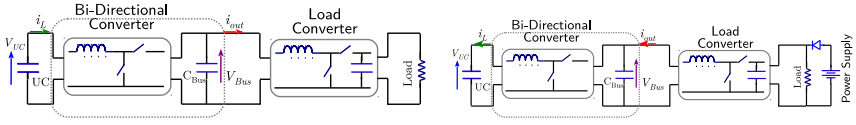
Table 1. Some values in the experimental setup

Controller is based on a floating point DSP board (Texas Instruments TMS320F28335) which is connected to converters via an interface board.

For the main bi-directional converter, the proposed control algorithm (Fig. 5) is implemented in the DSP using forward Euler digitization method [18]. Inductor current is constantly monitored and while its value is smaller than the limit, Equation (2), calculation unit applies the Equation (9) as the PI controller. In the current limiting control mode, as described in section 4.2, equation (10) is applied to the



(a)



(b) (c)

Figure 7. a) Experimental setup b) Forward operating mode b) Reverse operating mode

controller.

Voltages (UC voltage and DC bus voltage) and current feedbacks are provided by 8-bit A/D converters in synchronized sampling mode. The acquisition rate is one sample per switching cycle.

Two different configurations are then used in these tests: in *forward* operating mode, the *load converter* is connected to a 600 W resistive load (Fig. 7-b) and in *reverse* mode a 60 V DC source is connected to the *load converter* for injecting current into the bus (Fig. 7-c). The *load converter* is run in current mode controls $\bar{i}_{out}$; $d\bar{i}_{out}/dt$ can then be easily set by writing an appropriate program in the DSP controller.

5.2 Performance of the controller

Controller's coefficients are shown in Table. 2. These coefficients are obtained empirically once the setup is mounted, by making a trade-off between reducing noise effects and increasing speed of the controller. It can be noticed that the experimental PI coefficients are smaller than the simulation case. In fact, in the simulations, switching noises and their effect on the control system are not considered and, consequently, the system can have a higher dynamic in the absence of the noises. However, the ratios between *v-loop* and *i-loop* coefficients are consistent and the *v-loop* needs to have a higher K_i coefficient in both cases.

Response of the system to a pulse of $\bar{i}_{out}$ is investigated in the following tests: In all cases, ultracapacitor is initially charged to 24 V and bus voltage is established at 48 V. $\bar{i}_{out}$ is then undergoes a pulse variation according to Table 3.

i-loop	*v-loop*	feedback	K_{pwm}
$K_p = 0.5$	$K_p = 0.8$	$K_{fi} = 90$	1875^{-1}
$K_i = 100$	$K_i = 600$	$K_{fv} = 14$	-

Table 2. Coefficients of the controller in the experimental setup

Fig. 8-a and d, show the performance of the controller in *forward* and *reverse* modes respectively.

A comparison of measured inductor current with calculated one is shown in Fig. 8-b & 8-e. Calculated current is obtained from Equation (7) using the identified $R_s = 0.33\ \Omega$. Calculated current is close to measured one, specially in the case of *reverse* operating mode. Although R_s is identified for *forward* mode, this result shows that for *reverse* mode it can be valid as well. Theoretical and measured efficiencies of

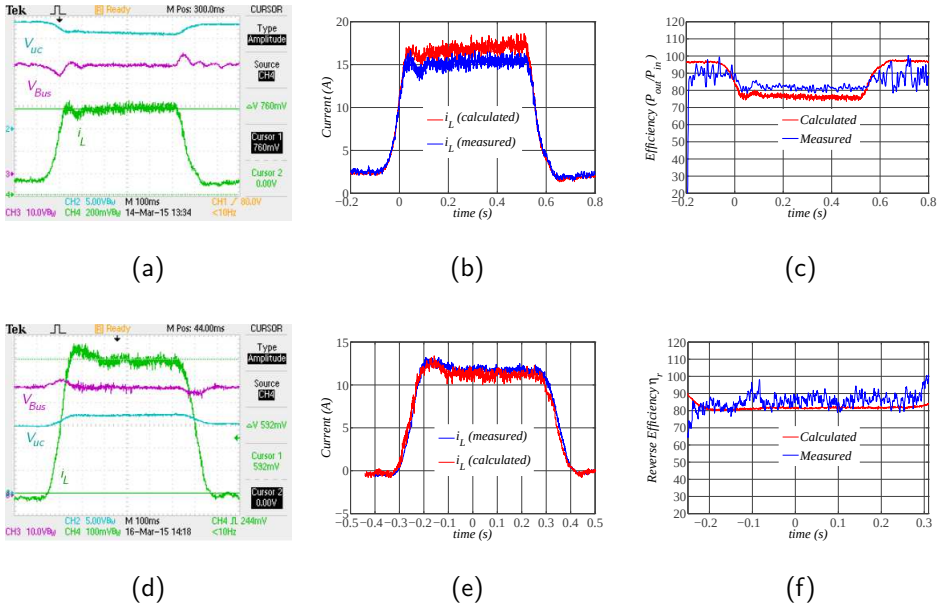


Figure 8. Experimental and calculation results: Performance of the controller in non saturated zone. Forward mode: a) Bus Voltage b) Calculated and measured inductor current c) efficiency of the converter. Same quantities in reverse mode: d,e and f. Resolution of the current probe in all measurements is 50 mV/A

the converter are shown in Fig. 8-c & f. One can observe that measurements are close to calculations. In *reverse* mode, as the converter runs as step-down one, its efficiency is higher than *forward* mode.

At the beginning and the end of measured interval, some non-relevant data can be observed (specially in reverse efficiency measurement). This is due to the resolution of current measurement in this zone: In fact, resolution of the current probe in all measurements is 50 mV/A. When current levels fall, to about 2 A, relative precision of the measured current (i.e. $\Delta I/I$) is poor and measured date are not reliable in this zone. This measured current is then multiplied by voltage to obtain power and efficiency, consequently, some noisy data appear in this zone.

	$\bar{i}_{out}$ initial/ final	$\bar{i}_{out}$ step time	$\bar{i}_{out}$ step value	d$\bar{i}_{out}$/dt rising/ falling	Converter mode	limit on $\bar{i}_{out}$
fig8-a	1 A	500 ms	5.5 A	55 A/s	forw.	no
fig8-d	0A	500 ms	-5 A	55 A/s	rev.	no
fig9-a	1 A	400 ms	8 A	50 A/s	forw.	yes
fig9-b	1 A	400 ms	10.5 A	50 A/s	forw.	yes

Table 3. Different scenarios applied on $\bar{i}_{out}$

5.3 Saturated transient

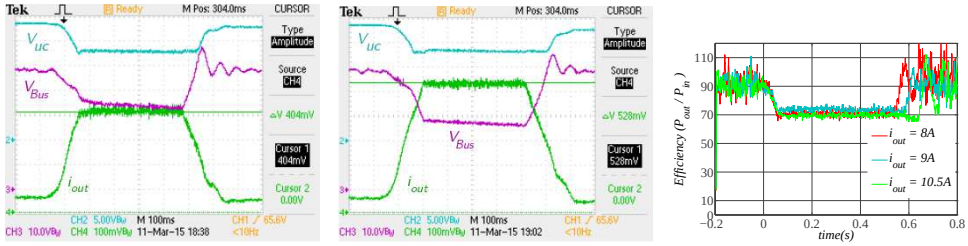
In this test, controller is pushed into the saturated zone for a tiny slice of time (400 ms), see Table 3. Inductor current reaches its maximal value and bus voltage drops to a lower voltage (Fig 9-a & b) during this transient.

Voltage overshoots and settling times, when bus voltage is restored to its nominal value, are shown in Table 4. Settling times are calculated from the point where $\bar{i}_L$ becomes smaller than i_{Lm}, (controller moves out from saturation zone) to the point where bus voltage remains within 5% of its nominal value. This test confirms the fact that by using the proposed controller, overshoot and settling time after short overload transients are independent from the magnitude of overload current and, as described earlier, depend on $d\bar{i}_{out}/dt$

Same effect can be observed on measured efficiency, in Fig. 9-c. In these tests limit value of inductor current is set to 80% of its theoretical value, i_{Lm}, due to thermal considerations and minimum efficiency of the converter should then be limited to 60% (according to Eq. 4) in saturated zone. However, the efficiency is rather limited to 70 % in three tests. In fact, identification of R_s is performed

	test1	test2	test3
i_{out} Maximum value (A)	8	9	10.5
Overshoot ($\Delta V_{Bus}/V_{Bus}$)	20.8%	20%	18.3%
Settling time (ms)	108	109	110

Table 4. Behaviour of the controller for three pulses with same di/dt: Bus voltage overshoot and settling time.



(a) (b) (c)

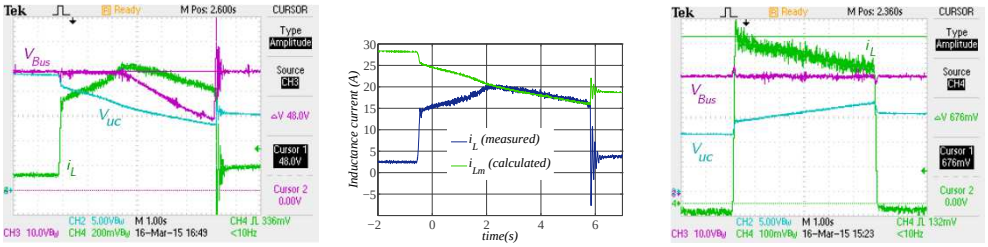
Figure 9. Overload transients with same $d\bar{i}_{out}/dt = 50\ A/s$ a) $\bar{i}_{out} = 8\ A$ b) $\bar{i}_{out} = 10.5\ A$ c) Measured efficiency of the converter is practically limited to 70 % in all cases. Resolution of the current probe in all measurements is 50 mV/A

within normal operating range of the converter and outside this range identified R_s is overestimated. In other words, when the inductor current is limited by controller, losses are smaller than those predicted from steady state measurement.

5.4 Ultracapacitor voltage and variation of current limit

In order to focus on operation of the current limit unit and its dependency on V_{uc}, ultracapacitor, initially charged to 24 V, is discharged with a constant current. During 6 s, a constant output current, $i_{out} = 5.4A$, is absorbed from the bus. Fig. 10-a shows that while the ultracapacitor discharges, inductor current, $\bar{i}_L$, is

increased to provide the necessary output power; when $\bar{i}_L$ reaches its limit value, i_{Lm}, bus voltage can be no more maintained at 48 V. Fig. 10-b compares the measured inductor current with the limit value of the current, which is set into the digital controller. One can notice that *i-loop* operates properly and inductor current follows the reference (current limit in this case).



(a) (b) (c)

Figure 10. a) Current absorbed from bus, UC is discharging b) inductor current: Calculated i_{Lm} & measured $\bar{i}_L$ c) Current is injected into the bus, UC is charging. Identification of UC parameters: C = 16.5 F, $R_{uc} = 0.18\Omega$

In *reverse* mode, a constant current of 5 A is injected into the bus during 5 s (i.e. $i_{out} = -5A$). In this sequence, $\bar{i}_L$ is injected into the ultracapacitor and no limit is imposed on this current. Fig. 10-c shows a charging sequence in which Inductor current, decreased from 14 A to 10.7 A while UC is charged gradually. Capacitance of the ultracapacitor is identified from: $V_{uc} = V_{uc0} + \frac{1}{C_{uc}} \int i_L \cdot dt + i_L \cdot R_{uc}$, with R_{uc}, total series resistance considered for UC module (identified values: $C_{uc} = 16.5\ F$, $R_{uc} = 0.18\ \Omega$).

6 Conclusion

In this paper, a control technique for managing short transient overloads in a bi-directional converter, connected between an ultracapacitor unit and a DC bus, is presented. In this method a variable current-limit is applied on the inductor current of boost converter. It is demonstrated that, this limit value depends on the ultracapacitor voltage. This control technique, allows to use the maximum operating range of a bi-directional converter in *forward* mode. Governing equations for this current-limit is obtained by characterizing boost converter in steady state operating points. This control technique provides same behaviours for short overloads of the same di/dt, regardless of the value of the overload current. An experimental setup consisting of a 360 W bi-directional DC/DC converter with a controller unit, based on a DSP, and an ultracapacitor unit is developed. The rate of the change of current, di/dt, on DC bus is then precisely set and behaviour of the controller is evaluated practically, in both cases of *forward* and *reverse* energy flow. In *forward* operating mode, minimum efficiency of the converter is limited to 70 %, by application of current-limit control. This method is useful in DC grids where several loads are connected and short overload transients could affect the performance of the system.

References

[1] M. Ortuzar, J. Moreno, and J. Dixon, "Ultracapacitor-Based Auxiliary Energy System for an Electric Vehicle: Implementation and Evaluation," *IEEE Transactions on Industrial Electronics*, vol. 54, no. 4, pp. 2147–2156, Aug. 2007.

[2] S. Zhou, Z. Wu, J. Li, and X.-p. Zhang, "Real-time Energy Control Approach for Smart Home Energy Management System," *Electric Power Components and Systems*, vol. 42, no. 3-4, pp. 315–326, Mar. 2014.

[3] M. Farhadi and O. A. Mohammed, "Real-Time Operation and Harmonic Analysis of Isolated and Non-Isolated Hybrid DC Microgrid," *IEEE Transactions on Industry Applications*, vol. 50, no. 4, pp. 2900–2909, Jul. 2014.

[4] D. Segaran, D. Holmes, and B. McGrath, "Enhanced Load Step Response for a Bidirectional DC-DC Converter," *IEEE Transactions on Power Electronics*, vol. 28, no. 1, pp. 371–379, Jan. 2013.

[5] F. Barati, Dan Li, and R. A. Dougal, "Voltage regulation in medium voltage DC systems," in *Electric Ship Technologies Symposium (ESTS 2013)*. Arlington, VA, USA: IEEE, Apr. 2013, pp. 372–378.

[6] P. Thounthong, S. Ral, and B. Davat, "Control strategy of fuel cell/supercapacitors hybrid power sources for electric vehicle," *Journal of Power Sources*, vol. 158, no. 1, pp. 806–814, Jul. 2006.

[7] A. Rufer, D. Hotellier, and P. Barrade, "A supercapacitor-based energy storage substation for voltage compensation in weak transportation networks," *IEEE Transactions on Power Delivery*, vol. 19, no. 2, pp. 629–636, 2004.

[8] J. Cao and A. Emadi, "A New Battery/UltraCapacitor Hybrid Energy Storage System for Electric, Hybrid, and Plug-In Hybrid Electric Vehicles," *IEEE Transactions on Power Electronics*, vol. 27, no. 1, pp. 122–132, Jan. 2012.

[9] G. Walker and P. Sernia, "Cascaded DC-DC converter connection of photovoltaic modules," *IEEE Transactions on Power Electronics*, vol. 19, no. 4, pp. 1130–1139, 2004.

[10] R.-Y. Duan and J.-D. Lee, "High-efficiency bidirectional DC-DC converter with coupled inductor," *IET Power Electronics*, vol. 5, no. 1, pp. 115–123, Jan. 2012.

[11] E. Santi, A. Monti, D. Li, K. Proddutur, and R. Dougal, "Synergetic control for DC-DC boost converter: implementation options," *IEEE Transactions on Industry Applications*, vol. 39, no. 6, pp. 1803–1813, Nov. 2003.

[12] S. O'Driscoll and D. Grant, "Combining peak current mode control with average current mode control using digitally assisted analog," in *2014 Twenty-Ninth Annual IEEE Applied Power Electronics Conference and Exposition (APEC)*, Mar. 2014, pp. 76–88.

[13] M. Gotfryd, "Output voltage and power limits in boost power factor corrector operating in discontinuous inductor current mode," *IEEE Transactions on Power Electronics*, vol. 15, no. 1, pp. 51–57, Jan. 2000.

[14] F. Barati and B. Ahmadi, "Current sharing in non-coupled interleaved bi-directional boost converters for supercapacitor applications." IEEE, Jun. 2015, pp. 1–5.

[15] H. Renaudineau, A. Houari, A. Shahin, J.-P. Martin, S. Pierfederici, F. Meibody-Tabar, and B. Gerardin, "Efficiency Optimization Through Current-Sharing for Paralleled DC-DC Boost Converters With Parameter Estimation," *IEEE Transactions on Power Electronics*, vol. 29, no. 2, pp. 759–767, Feb. 2014.

[16] B. Bryant and M. Kazimierczuk, "Voltage-Loop Power-Stage Transfer Functions With MOSFET Delay for Boost PWM Converter Operating in CCM," *IEEE Transactions on Industrial Electronics*, vol. 54, no. 1, pp. 347–353, Feb. 2007.

[17] A. Lidozzi, L. Solero, A. Di Napoli, and F. Crescimbini, "Synergetic control for ultracapacitors based high dynamic converters," in *Twentieth Annual IEEE Applied Power Electronics Conference and Exposition, 2005. APEC 2005*, vol. 3, Mar. 2005, pp. 1976–1982 Vol. 3.

[18] Simone Buso and Paolo Mattavelli, *Digital Control in Power Electronics*, 1st ed. Morgan & Claypool, 2006.