Limits, Stability and Disturbance Rejection Analysis of Voltage Control Loop Strategies for Grid Forming Converters in DC and AC Microgrids with High Penetration of Constant Power Loads

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Keywords

≪Control methods for electrical systems≫, ≪Microgrid≫, ≪Non-linear control≫, ≪Power quality≫.

Abstract

This paper extensively analyzes the operation limits, system stability and disturbance rejection capability of the voltage control loops used in master-slave AC and DC Microgrids (MGs). Two different control schemes are studied analytically, simulated and experimentally tested, focusing on Constant Power Loads (CPL). Additionally, the use of the virtual capacitance (VC) as a tool for response enhancement is introduced. The study pursues the proper selection of the controllers gains and minimization of capacitance values by considering the dynamic behavior.

Introduction

The increasing concern about environmental issues and concepts as renewable energies, distributed generation and self-consumption have led to the necessity of alternatives to the conventional power grid. Moreover, the fast development of power semiconductor devices and digital control systems have made power electronic converters (PECs) the most suitable interface for both generation, energy storage and dimmable loads. Due to the high penetration of renewable generation operating under a maximum power point tracking (MPPT) scheme, one of the adopted voltage control methods in these converter dominated MGs is based on the Master-Slave strategy. This approach requires a grid forming converter controlling the voltage magnitude (and the frequency in the case of AC MGs) [1, 2, 3]. Other alternatives, as droop-based on multiple slack control have been also proposed [4, 5]. Unlike the conventional grid, these kind of MGs are defined as weak. They have a low inertia that should be compensated by a stiff voltage control, and a low line X/R ratio that couples active power and voltage magnitude. Moreover,

the high presence of tightly regulated CPL contribute negatively to that low inertia, in contrast to the self-regulating effect given by conventional loads as Constant Impedance Loads (CIL). In addition, the disturbance rejection response of the voltage control schemes usually implemented in PECs depends on the type of load disturbance, becoming in some cases non-linear and load-state-dependent.

The challenges imposed by CPLs and the non-linearity and stability issues related with the voltage control schemes based on voltage feedback and PI controllers, have been already addressed in the literature [6, 7, 8, 9, 10]. Nonetheless, the dynamics, stability limitations and selection of both the passive elements and the controller parameters for a slack control under CPL have been poorly discussed. Some alternative feedback control topologies have been proposed based on the capacitor energy storage capability as an approach to linearize the relation between the voltage and the power at the DC link [11, 12, 13, 14]. However, those techniques have not been further exploited for grid forming converter applications, existing few examples in the literature focused on the analysis of the dynamic performance.

This paper analyzes the dynamic behavior of the voltage control loop used in grid forming voltage source converters (VSCs) integrated in AC and DC MGs. Due to its wide acceptance in converter control applications, a cascaded voltage-current control scheme is used in this study. Both the conventional voltage feedback control, referred as Direct Voltage Control (DVC) in this document, and the control based on squared voltage, referred as Quadratic Voltage Control (QVC), will be addressed, considering CPLs as the main disturbance. Taking advantage of the cascaded control premises, the inner control loop dynamics will be neglected. Thus, the analysis becomes valid for different applications such as AC slack, DC slack or DC link control. An analytical study on the conventional voltage control schemes is perform based on system linearization methods and validated through simulations and experimentally. In addition, the use of virtual capacitance (VC) is introduced as a tool for disturbance rejection enhancement as well as to experimentally forecast the effect of resizing the capacitance in existing systems. The study will deal with operation limits, the system stability and the disturbance rejection of the voltage control, leading not only to the proper selection of the control scheme and control parameters, but also to the sizing of the passive elements of the converter.

Problem Definition and System Modeling

In most of the MG applications requiring a voltage regulation, the system plant to be controlled consists of a capacitor whose voltage derivative is proportional to its current. Thus, the control is performed by a closed loop cascaded controller consisting of an inner current control loop and an outer voltage control loop. Assuming the current control loop is fast enough, its dynamics can be neglected. Thus, the voltage control can be assumed as a voltage regulator, which input is the error, ε, between the voltage reference, V^*, and the measured voltage, $\tilde{V}$, while the control action is the current, I, entering the system plant. Considering the existence of disturbance loads, the system plant is defined by (1), where $V_{(t)}$ is the capacitor voltage, $I_{(t)}$ is the control action of the voltage control loop, and $I_{d(t)}$ is the load disturbance. According to (1), the controller can be tuned using LTI system properties.

$$\frac{dV_{(t)}}{dt} = \frac{1}{C}(I_{(t)} - I_{d(t)}) \qquad (1)$$

$$\frac{dV_{(t)}}{dt} = \frac{1}{C}\left(I_{(t)} - \underbrace{\left(I_{L(t)} + \frac{P_{L(t)}}{V_{(t)}} + G_{L(t)}V_{(t)}\right)}_{I_{d(t)}}\right) \qquad (2)$$

Nevertheless, Constant Current Loads (CCL) are rarely found in power systems. More and more electrical appliances and industrial equipment behaves as CPLs, presenting a tight control of load power, or as CILs. Thus, the system in (1) must be reformulated as the non-linear system in (2), where I_L, P_L and G_L are the current, power and conductance disturbances drawn by CCLs, CPLs, and CILs respectively. Negative values of P_L and I_L are considered as generation. Fig. 1(a) shows the single line representation of the defined non-linear system. The behavior of the different loads existing in a MG are illustrated in Fig. 1(b). The non-linearities due to CPL and CIL will affect the voltage regulation design and performance. Moreover, unlike CILs, it is well known that CPLs are prone to compromise the system stability. In the literature, several attempts have been carried out for obtaining a linear approximation by defining a neg-

ative impedance [8, 9, 4]. In this paper, the effect of non-linear loads is approached by the linearization of the close loop system.

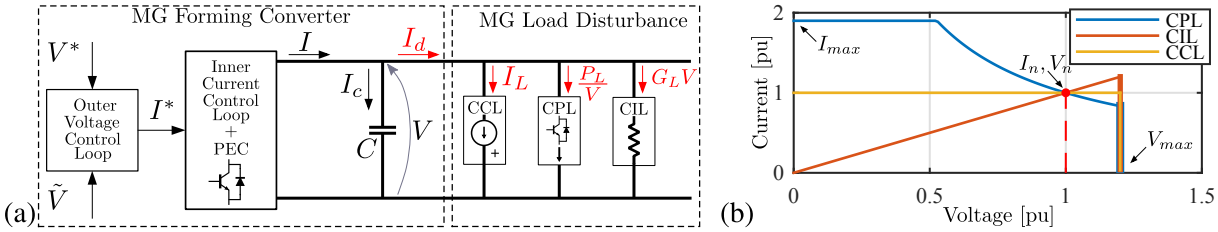


Fig. 1: (a) Simplified single line representation of the grid forming converter and load disturbance in a DC or AC MG. (b) Voltage-Current curves of the different types of loads in MGs.

The Voltage Controller: Control Topologies, Analytical Models and Analysis

The voltage controller models are analyzed in this section using linearized models. Two control schemes are considered, the direct voltage control (DVC) and the quadratic voltage control (QVC).

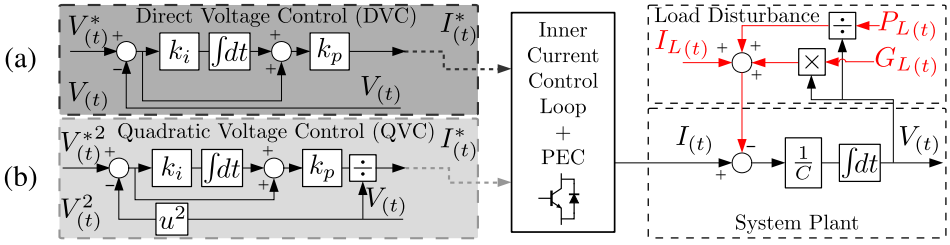


Fig. 2: Voltage control schemes for the different types of loads in MGs. (a) DVC; (b) QVC.

The Direct Voltage Controller (DVC)

The DVC control scheme is shown in Fig. 2(a). A PI regulator in the standard form has been selected for the analysis, defined by (3), where I^* is the control action, V^* the voltage reference, V the actual voltage, and k_p and k_i are the proportional and integral PI gains respectively. In this paper, the effect of the sensors is neglected. This controller is based on the linear relationship between the voltage and the current at the capacitor. Despite its apparent simplicity, achieving good dynamic behavior is not straightforward, as already reported in the literature [11]. This is due to the fact that even the reference tracking capability for the voltage control is linear, as shown in (4), the voltage reaction to both CPL and CIL disturbances is not.

$$I^*_{(t)} = k_p(V^*_{(t)} - V_{(t)}) + k_p k_i \int (V^*_{(t)} - V_{(t)})dt \qquad (3)$$

$$\frac{V_{(s)}}{V^*_{(s)}} = \frac{k_p s + k_p k_i}{s^2 C + s k_p + k_i k_p} \qquad (4)$$

The Quadratic Voltage Controller (QVC)

An alternative to the DVC has been proposed in the literature referred as fast-acting DC link voltage controller and energy based controller, in the context of applications for the DC link control of DC/DC/AC and AC/DC/AC converters [11, 12, 13, 14]. Nonetheless, its application can be generalized to any cascaded-based voltage control such as grid forming converters in both DC and AC MGs. The control scheme is shown in Fig. 2(b) and the controller differential equation is given by (5).

$$I^*_{(t)} = \frac{k_p({V^*_{(t)}}^2 - V^2_{(t)}) + k_p k_i \int ({V^*_{(t)}}^2 - V^2_{(t)})dt}{V_{(t)}} \qquad (5)$$

$$V_{(t)}\frac{dV_{(t)}}{dt} = \frac{1}{C}P_{c(t)} \Rightarrow \frac{dV^2_{(t)}}{dt} = \frac{2}{C}P_{c(t)} \qquad (6)$$

The control is based on the linear relation between the power flowing into the capacitor, $P_{c(t)}$, and the voltage module squared, $V^2_{(t)}$, as stated in (6). In [11, 13], its design is realized by exploiting the relation between voltage variations and the energy stored in the capacitor, W_c. However, the tuning method used

in those papers is oriented to the regulation of the DC link of an AFE exposed to the steady state disturbances produced by AC grid unbalances. Here, we include a general approach based on disturbance rejection analysis, considering a meaningful comparison between DVC and QVC dynamic response.

One of the main advantages of QVC, concerning the disturbance rejection and stability analysis, is that the relation between $V_{(t)}^2$ and $P_{L(t)}$ becomes linear, unlike in the case of DVC. This fact facilitates the delimitation of the stable region. However, the controlled variable is still $V_{(t)}$ and, considering other kind of disturbances that may be present in the grid, as CIL, the system performance should be evaluated according to the $V_{(t)}$ dynamics. For that reason the system linearization is also needed. Leaving the disturbances aside, unlike in the DVC, the relation between V and V^* is non-linear, (5). The linearized approximation of the reference tracking transfer function is proposed in (7), where V_0^* and V_0 are the voltage reference and the actual voltage at the equilibrium point, respectively. Assuming $V_0 = V_0^*$, the transfer function is approximated by (8).

$$\frac{V_{(s)}}{V_{(s)}^*} \approx \frac{s2k_pV_0^* + 2k_pk_iV_0^*}{s^2CV_0 + s2k_pV_0 + 2k_pk_iV_0} \quad (7) \qquad \frac{V_{(s)}}{V_{(s)}^*} \approx \frac{s2k_p + 2k_pk_i}{s^2C + s2k_p + 2k_pk_i} \quad (8)$$

Among the controllers tuning techniques available for linear systems, an analytical approach has been selected, aimed at simplifying the selection of PI regulator parameters [5]. The close loop system can be simplified as a second order system with natural frequency ω_n and damping factor ξ. Equations (4) and (8), can be expressed as (9), and assuming linearity, the system poles, ω_n and ξ, will be the same for disturbance rejection transfer functions. Thus, the PI regulator gains for DVC and QVC are tunned according to (10) and (11) respectively, leading to a similar bandwidth.

$$\frac{V_{(s)}}{V_{(s)}^*} = \frac{2\xi\omega_n s + \omega_n^2}{s^2 + 2\xi\omega_n s + \omega_n^2} \quad (9) \qquad k_p = 2\xi\omega_n C;\ k_i = \frac{\omega_n^2 C}{k_p} \quad (10) \qquad k_p = \xi\omega_n C;\ k_i = \frac{\omega_n^2 C}{2k_p} \quad (11)$$

According to cascaded control theory, the bandwidth of the inner loop is assumed to be at least one decade higher than ω_n. The damping factor, ξ, can be selected as a trade-off between overshoot and settling time. For this paper the parameters shown in Table I have been selected.

The main requirement of a grid forming converter is a stiff voltage control under disturbances. To analyze the effect of the type of load in the disturbance rejection capability, the $\frac{\Delta V_{(s)}}{\Delta P_{L(s)}}$ disturbance rejection transfer function for DVC and QVC have been obtained by linearization and are shown in (12) and (13) respectively. In these equations, the equilibrium point is defined by $x_0 = [V_0^*, V_0, P_{L0}, G_{L0}]$ for DVC and $x_0 = [V_0^*, V_0, P_{L0}, G_{L0}]$ for QVC. V_0^* and V_0 are the voltage reference and the steady state voltage at the equilibrium point. P_{L0} and G_{L0} are the load in terms of power associated to CPLs and the load in terms of conductance given by CILs at the equilibrium point respectively. An operation close to the equilibrium point is assumed, considering $V_0 = V_0^*$.

$$\frac{\Delta V_{(s)}}{\Delta P_{L(s)}} \approx \frac{-sV_0}{s^2V_0^2C + sk_pV_0^2 - P_{L0} + G_{L0}V_0^2 + k_ik_pV_0^2} \quad (12) \qquad \frac{\Delta V_{(s)}}{\Delta P_{L(s)}} \approx \frac{-s}{s^2V_0C + s2k_pV_0 + I_{L0} + 2G_{L0}V_0 + 2k_ik_pV_0} \quad (13)$$

To verify the linearized models, the response of $\frac{\Delta V_{(s)}}{\Delta P_{L(s)}}$ is compared in Fig. 3 with the simulation of the non-linear system, using Matlab/Simulink, for both DVC and QVC.

The error between the actual response and the linear approximation validates the linear models near the equilibrium point. However, when the load level at the equilibrium point is not considered, the linear model considerably deviates from the actual response as the system deviates from the equilibrium point. To analyze the effect of the load level at the equlibrium point, the root-contour of the DVC for P_{L0} and G_{L0} , (14) and (15), and the root-contour of QVC for I_{L0} and G_{L0}, (16) and (17), have been obtained.

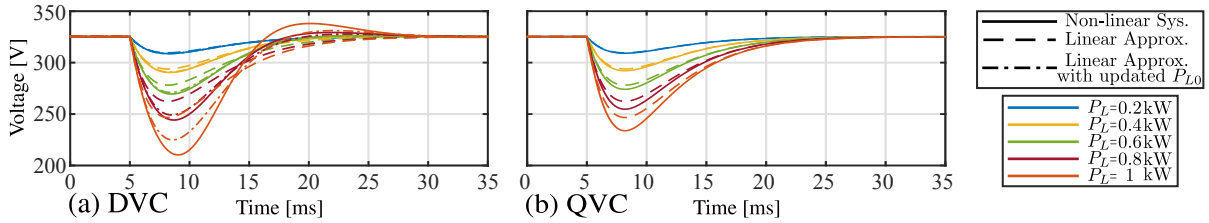


Fig. 3: Non-linear simulated response compared with the linear approximation of $\frac{\Delta V_{(s)}}{\Delta P_{L(s)}}$ under increasing active power steps. (a) DVC; (b) QVC. Results using the data in Table I.

$$DVC\ root\ contour\ P_{L0} \rightarrow 1 + P_{L0}G_{(s)}H_{(s)} \approx 1 + P_{L0}\frac{-s}{s^2V_0^2C + sk_pV_0^2 + G_{L0}V_0^2 + k_ik_pV_0^2} \quad (14)$$

$$DVC\ root\ contour\ G_{L0} \rightarrow 1 + G_{L0}G_{(s)}H_{(s)} \approx 1 + G_{L0}\frac{V_0^2 s}{s^2V_0^2C + sk_pV_0^2 - P_{L0} + k_ik_pV_0^2} \quad (15)$$

$$QVC\ root\ contour\ I_{L0} \rightarrow 1 + I_{L0}G_{(s)}H_{(s)} \approx 1 + I_{L0}\frac{s}{s^2V_0C + s2k_pV_0 + 2G_{L0}V_0 + 2k_ik_pV_0} \quad (16)$$

$$QVC\ root\ contour\ G_{L0} \rightarrow 1 + G_{L0}G_{(s)}H_{(s)} \approx 1 + G_{L0}\frac{2V_0 s}{s^2V_0C + s2k_pV_0 + I_{L0} + 2k_ik_pV_0} \quad (17)$$

It is worth noting that the response of DVC is non-linear and depends on the load level, P_{L0} and G_{L0}, thus conditioning the system behavior and the accuracy of the linear approximation. Moreover, load dependent poles lead to system instability as shown in Fig. 4(a), where the root-contour plot for P_{L0} is represented. On the other hand, negative values of P_{L0}, i.e. power generation, can affect positively to the voltage damping.

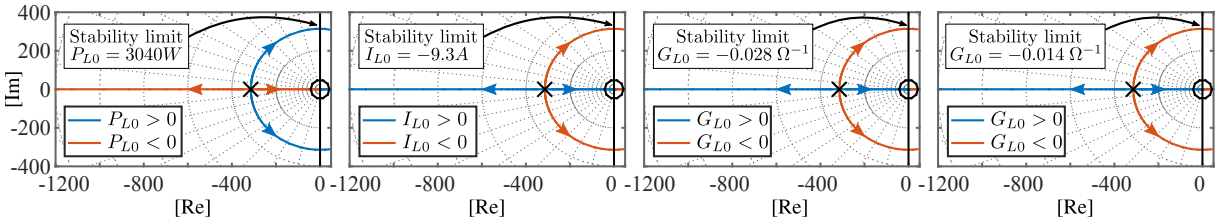


Fig. 4: Root-contour for DVC and QVC depending on P_{L0}, I_{L0} and G_{L0}. (a) parameter P_{L0} in DVC; (b) parameter I_{L0} in QVC; (c) parameter G_{L0} in DVC; (d) parameter G_{L0} in QVC.

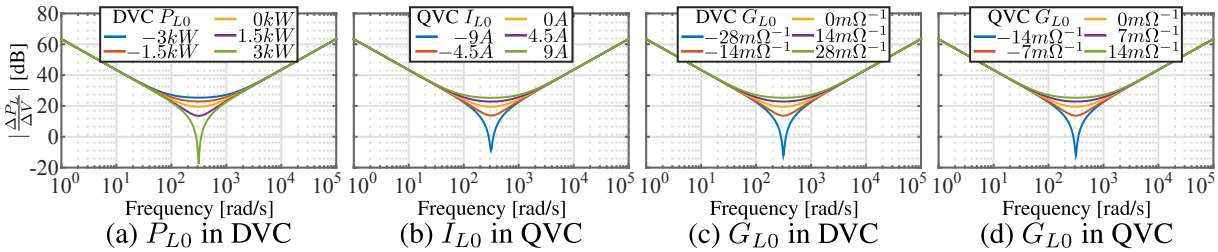
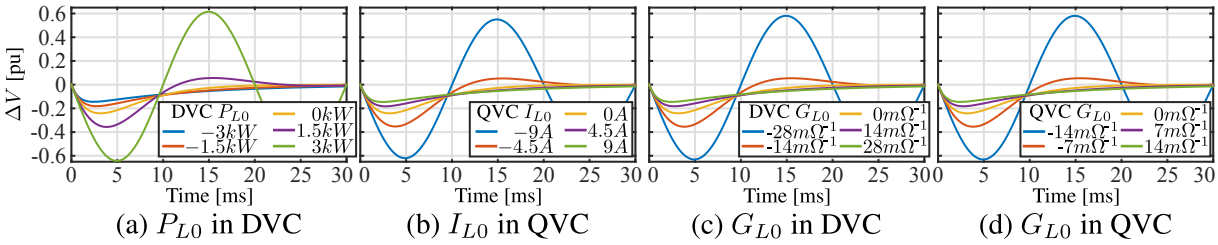


Fig. 5: Dynamic stiffness evaluation depending on P_{L0}, I_{L0} and G_{L0}. (a) Influence of P_{L0} in DVC; (b) Influence of I_{L0} in QVC; (c) Influence of G_{L0} in DVC; (d) Influence of G_{L0} in QVC.

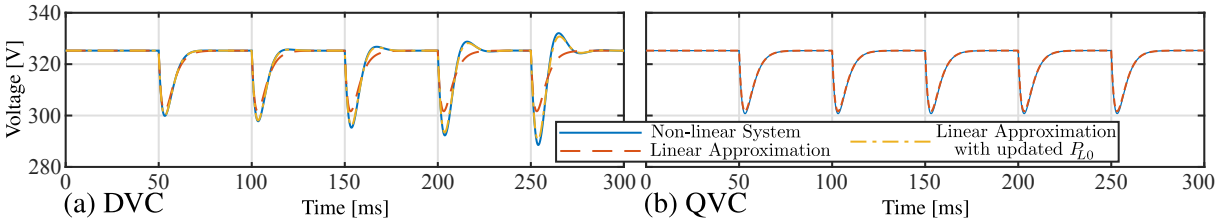
In the case of QVC, the term P_{L0} does not even appear in the equation, which is one of the main advantages of this method over the widely used DVC. It is worth to point out that such an advantage has not been reported yet in the literature. Nonetheless, a dependency on CCLs appears represented by the load level at the equilibrium point I_{L0}. Although positive load currents, $I_{L0} \geq 0$, does not present sta-



(a) P_{L0} in DVC (b) I_{L0} in QVC (c) G_{L0} in DVC (d) G_{L0} in QVC

Fig. 6: Step response under a CPL step disturbance of 1kW. (a) Influence of P_{L0} in DVC; (b) Influence of I_{L0} in QVC; (c) Influence of G_{L0} in DVC; (d) Influence of G_{L0} in QVC.

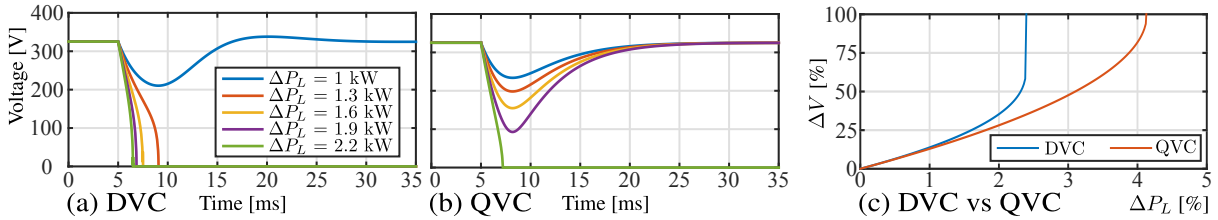
bility problems, a potential issue appears when $I_{L0} \leq 0$, i.e. when constant current generation (CCG) is injected into the grid. The root-contour of the QVC system as a function of I_{L0} is shown in Fig. 4(b). G_{L0} appears in both methods and has a positive impact in the system damping of both DVC and QVC as shown in Fig 4(c) and 4(d). However, if $G_{L0} < 0$, i.e., when some equipment in the grid behaves as a negative resistor, like a generator operating in voltage/current droop mode, the system response can be worsen until instability. The impact of P_{L0}, I_{L0} and G_{L0} on the dynamic stiffness, defined as the inverse of the disturbance rejection, and step response of DVC and QVC are shown in Fig 5 and 6. It is worth to point out that the higher is the dynamic stiffness the better is the disturbance rejection capabilities. The effect of P_{L0} in the time domain response is illustrated in Fig. 7, where the behaviour of DVC and QVC methods are compared under CPL increasing steps. Unlike in the QVC, for the same load step, the response in the DVC method is altered for the worse at higher load levels.



(a) DVC (b) QVC

Fig. 7: Disturbance response under increasing CPL. Load is increased by steps of 300W every 50ms. Dashed lines show the linear approximations. (a) DVC; (b) QVC. Results using the data in Table I.

The voltage level also represents a potential cause of instability as it deviates from the equilibrium point. The voltage collapse for both controllers is represented in Fig. 8 for a CPL disturbance. As it is shown, the QVC is not only independent of the CPL load level at the equilibrium point, P_{L0}, but also withstands higher CPL step disturbance before it collapses. This demonstrates that the QVC can withstand higher CPL variations than the DVC method under the same conditions, as shown in Fig. 8(c), which is a clear advantage of the former controller.

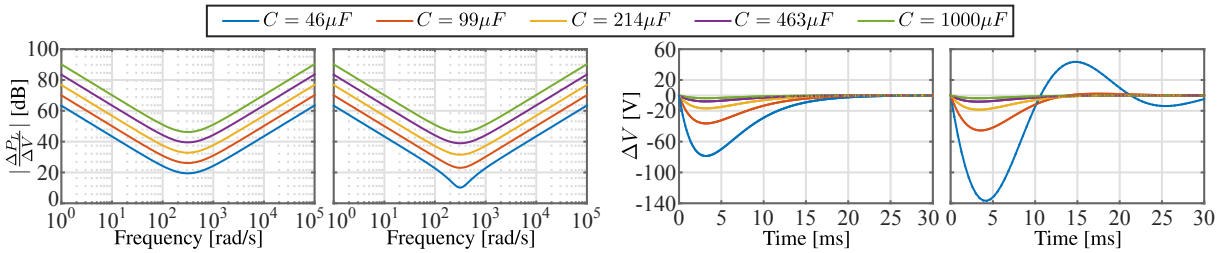


(a) DVC (b) QVC (c) DVC vs QVC

Fig. 8: Voltage collapse for the DVC and QVC methods under CPL steps. (a) DVC performance for an initial $P_{L0} = 0$; (b) QVC performance; (c) DVC and QVC maximum voltage deviation as a function of the CPL step shown in percentage. Results using the data in Table I.

Effect of system Capacitor and the Virtual Capacitance concept

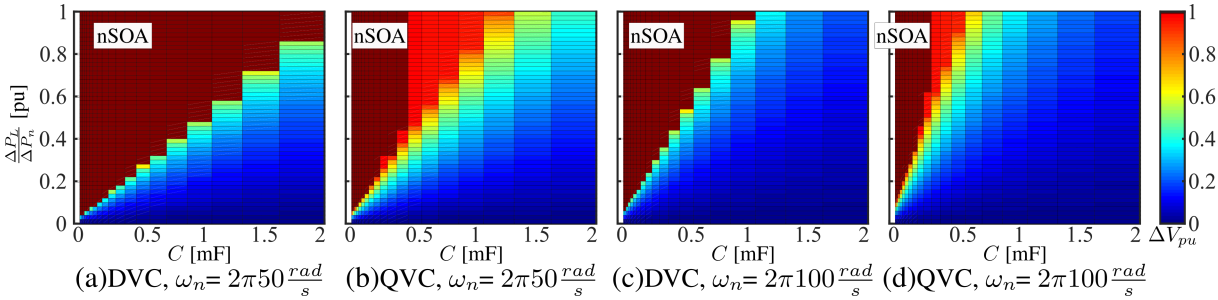
The capacitor and controller bandwidth take an important role in the system behavior. While the bandwidth is limited by the inner control loop, the size of the capacitor depends on the application. In DC voltage control applications, such as those found in DC links, the capacitor is usually sized according to the expected oscillations caused by stationary power fluctuations, which in some cases leads to oversizing [13]. Regarding AC grid forming converters, the capacitor is often determined by the filtering requirements of switching frequency harmonics, leading to small capacitor values. It is obvious that increasing the capacitor size while maintaining ω_n and ξ, will lead to an improved disturbance rejection without compromising the system stability. Fig. 9 shows the dynamic stiffness in the frequency domain and the time domain 1kW step response of the disturbance rejection transfer function $\frac{\Delta V_{(s)}}{\Delta P_{L(s)}}$ for different capacitor values using DVC and QVC. The QVC and DVC performance is the same if $P_{L0} = 0W$.



(a) DVC/QVC $P_{L0} = 0W$ (b) DVC $P_{L0} = 2kW$ (c) DVC/QVC $P_{L0} = 0W$ (d) DVC $P_{L0} = 2kW$

Fig. 9: Evaluation of the capacitor size effect in the disturbance rejection capabilities. (a) QVC dynamic stiffness, $\frac{\Delta P_{L(s)}}{\Delta V_{(s)}}$, for different capacitor values; (b) step response for the transfer function $\frac{\Delta V_{(s)}}{\Delta P_{L(s)}}$.

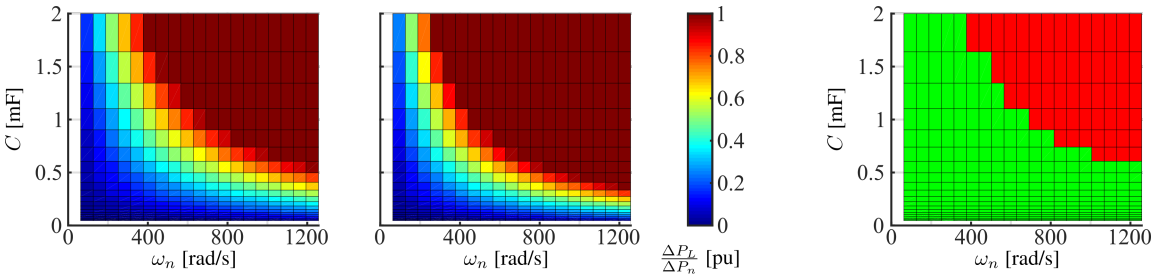
As expected, the disturbance rejection is improved as the capacitor increases. The size of the capacitor has a direct influence on the maximum disturbance the system can withstand. To compare the performance of both control techniques, the maximum voltage deviation under CPL disturbance has been obtained by non-linear simulation in Simulink as a function of the capacitor size, C, and the power step disturbance, $\frac{\Delta P_L}{P_n}$, with $P_n = 50kW$. The results comparing both methods for two different bandwidth, ω_n, are shown in Fig. 10, where $\Delta V_{pu} = 1$ represents the system voltage collapse. As a main conclusion, the QVC extends the region of operation, allowing a better disturbance rejection and avoiding voltage collapse with lower capacitor values compared with the DVC method.



(a)DVC, $\omega_n = 2\pi 50 \frac{rad}{s}$ (b)QVC, $\omega_n = 2\pi 50 \frac{rad}{s}$ (c)DVC, $\omega_n = 2\pi 100 \frac{rad}{s}$ (d)QVC, $\omega_n = 2\pi 100 \frac{rad}{s}$

Fig. 10: Maximum voltage deviation depending on the CPL step disturbance and the capacitor value. Data for two different controller bandwidth values is given. (a) DVC, ω_n=2π50rad/s; (b) QVC, ω_n=2π50rad/s; (c) DVC, ω_n=2π100rad/s; (d) QVC, ω_n=2π100rad/s. Dark red is considered as the non-Safe Operating Area (nSOA).

As shown, the voltage control bandwidth plays also an important role in the maximum voltage deviation. As an example of its effect, Fig. 11 shows the maximum supported CPL step, $\frac{\Delta P_L}{P_n}$ with $P_n = 50kW$, as a function of the capacitor size, C, and the controller bandwidth, ω_n, for a maximum voltage deviation of 0.65pu. Fig. 11(c) shows the combinations for which the QVC offers a better performance (represented in green) in the particular data shown in 11(a) and (b). The cases in red represent an operation similar in both DVC and QVC. In this case, the DVC does not offer a better performance than the QVC for any.



(a) DVC $\Delta V \geq 0.65pu$ (b) QVC $\Delta V \geq 0.65pu$ (c) QVC vs DVC

Fig. 11: Maximum CPL step disturbance for a maximum voltage deviation of 0.65 pu, depending on the capacitor value and the voltage control bandwidth, ω_n. (a) DVC; (b) QVC; (c) DVC.

Unlike the controller parameters, the modification of the hardware of the system is more restricted. Other techniques for voltage control disturbance rejection enhancement have been proposed in the past, mainly based on load decoupling through measurements, observers or estimators [15]. A simpler alternative is presented in Fig. 12, where $D_{(t)} = C_v \frac{d}{dt}$. Using a pseudo-derivative feedback control, it is possible to add a virtual capacitance C_v which ideally will be added to the passive capacitance C, improving the disturbance rejection. The DVC and QVC regulators are now defined by (18) and (19) respectively.

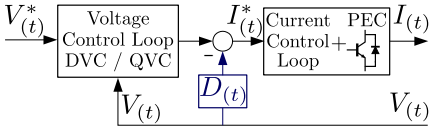


Fig. 12: Modified Voltage control scheme using PDF structure and C_v.

$$I^*_{(t)} = k_p(V^*_{(t)} - V_{(t)}) + k_i \int (V^*_{(t)} - V_{(t)})dt - C_v \frac{dV_{(t)}}{dt} \tag{18}$$

$$I^*_{(t)} = \frac{k_p({V^*_{(t)}}^2 - V^2_{(t)}) + k_i \int ({V^*_{(t)}}^2 - V^2_{(t)})dt}{V_{(t)}} - C_v \frac{dV_{(t)}}{dt} \tag{19}$$

Thus, assuming an ideal derivative and ideal sensors, the transfer functions for DVC and QVC, as well as the PI parameters, k_p and k_i, can be modified by substituting the parameter C for $C + C_v$. It is worth noting that the virtual capacitance does not only allow to improve the dynamic stiffness but can also be used to emulate low capacitance systems by applying a negative value, i.e. $C_v < 0$.

Experimental Results

The control models presented in this paper have been tested experimentally under 2 different scenarios, covering the application of voltage control in both DC and AC grids. The experimental results have been obtained using the Triphase power modules PM15F42C and PM90F60C. The experimental parameters are included in Table I.

Table I: System parameters used for voltage control analysis

System Parameters	Simulation and Analytical	Experimental Setup	
		DC MG	AC MG
Voltage reference V^*	325 V	680 V_{DC}	230 $V_{AC_{rms}}$
Nominal Frequency	-	DC	50 Hz
Nominal Active Power P	50 kW	11 kW	90 kW
Capacitor C	46 μF	1000 μF	46 μF
Switching frequency f_{sw}	8 kHz	8 kHz	8/16 kHz
Current control loop bandwidth	2π500 rad/s	2π500 rad/s	2π500 rad/s
Voltage control loop ω_n / ξ	2π50 rad/s / 1	2π5 rad/s / 1	2π50 rad/s / 1

Fig. 13 illustrates the simplified scheme of the experimental setups. For the DC voltage control, a D-Statcom with a battery energy storage system (BESS) has been used (PM15F42C). The DC link voltage is controlled by a DC/DC forming converter fed by a battery, while a DC/AC 3-phase grid tied converter operates as a DC CPL. In order to test the AC voltage control, the PM90F60C 3-ph converter has been

used as the AC grid forming converter while the D-Statcom with BESS (PM15F42C) plays the role of an AC CPL. An additional 56 Ω resistive load, R_L, has been included in the MG. The AC control has been implemented in the *dq* synchronous reference frame applying the QVC and DVC to both *d* and *q* axis.

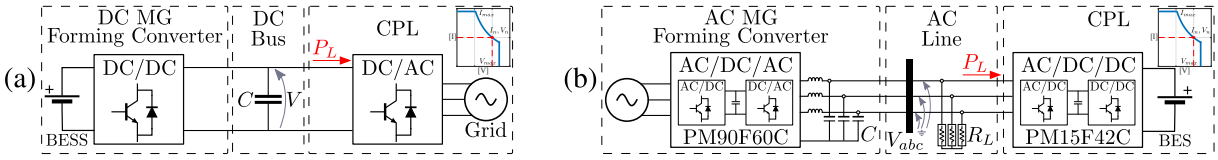


Fig. 13: Experimental setup. (a) DC MG; (b) AC MG.

Fig. 14(a) shows the response of both DVC and QVC under increasing CPL steps for several capacitor values in the DC MG setup. Due to the experimental setup limitations, the capacitor have been resized using virtual capacitance (Fig. 12), being the physical capacitor value 1000 μF. In order to better illustrate the effect, the voltage regulator bandwidth has been set to 5Hz.

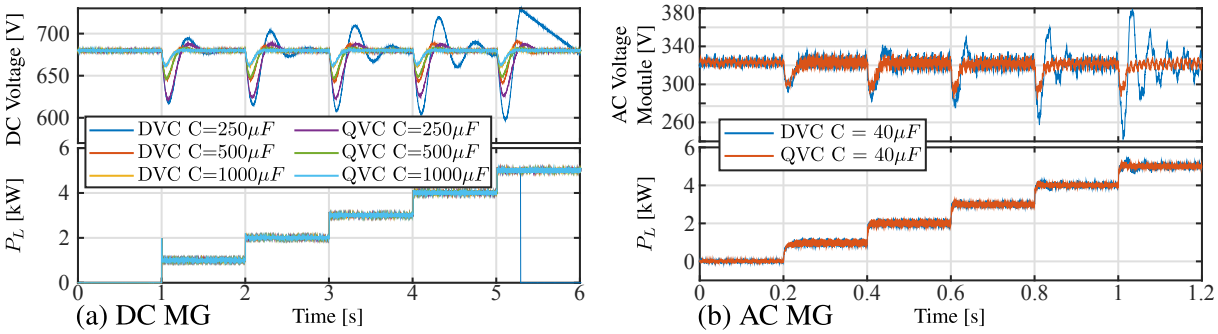


Fig. 14: Experimental Results. DVC and QVC are compared under multistep P_L. (a) DC grid forming converter performance for different capacitor values. (b) AC grid forming converter performance.

Fig. 14(b) shows the performance comparison between DVC and QVC in the AC 3-ph MG with an increasing CPL. The instantaneous voltage magnitude is represented. As expected from simulations, the DVC dependency on the load level makes its response to be worsen with increased CPL. It is worth noting that the local resistive load provides an improved damping, allowing to move the stability limit from $P_{L0} \simeq 3$ kW to $P_{L0} \simeq 6$ kW. The performance of virtual capacitance control applied to AC is shown in Fig. 15 comparing the step response of DVC and QVC. The improved response of the QVC with respect to the DVC should be highlighted, specially when low capacitance values are used.

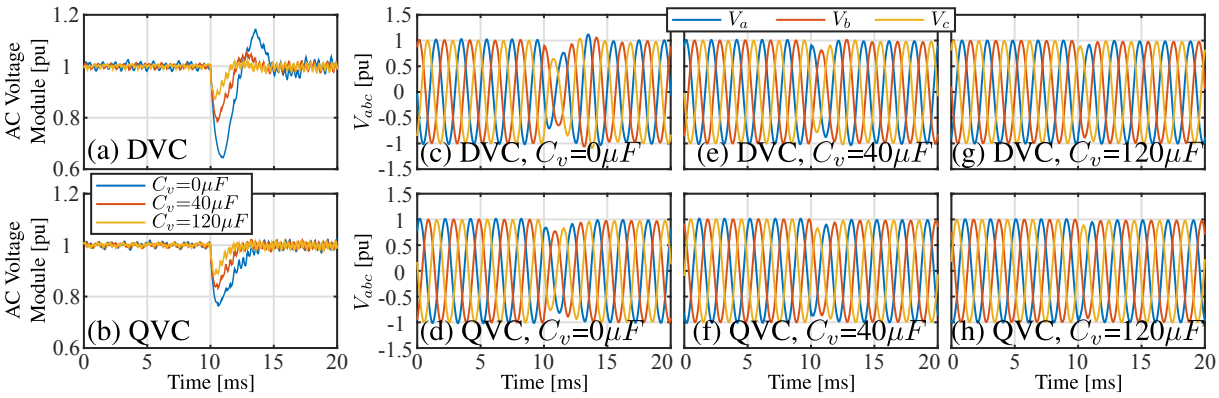


Fig. 15: AC Experimental Setup. DVC and QVC responses using virtual capacitance. Step of $P_L = 2.5$ kW at $t = 0.1$ s. (a) DVC voltage module for different C_v values; (b) QVC voltage module for different C_v values; (c) DVC phase voltages for $C_v = 0\mu F$; (d) QVC phase voltages for $C_v = 0\mu F$; (e) DVC phase voltages for $C_v = 40\mu F$; (f) QVC phase voltages for $C_v = 40\mu F$; (g) DVC phase voltages for $C_v = 120\mu F$; (h) QVC phase voltages for $C_v = 120\mu F$.

Conclusions

The paper extensively analyzes the voltage control in master-slave AC/DC microgrids with high penetration of CPLs. DVC and QVC have been compared outlining their benefits and drawbacks. The QVC has proved to be a promising alternative under CPL presence. Additionally, the use of the virtual capacitance as a tool for response enhancement has been introduced. The system linearization enables the stability and dynamic analysis for the proper selection of passive elements. The conducted study analyzes the voltage control schemes under a controlled environment valid as a starting point for simplifying the proper selection of the controller scheme, gains and the minimization of capacitance values, establishing the basics for the development of a simple procedure that takes the dynamic behavior into consideration.

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