A multiphase interleaved boost converter with coupled inductor for fuel cell APU applications

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Abstract

The growing demands for electrical capacity on future more electric aircraft (MEA) has led the engine-based generators to increase in size. Many manufacturers and researchers have a strong interest in developing fuel cells for aerospace applications due to their advantage of high efficiency and their use as a medium for clean energy resources. A particular interest is in using fuel cells within the Auxiliary Power Unit (APU) - a function that is currently provided by an additional gas turbine in most aircraft. Their integration into aircraft systems is not straightforward. A particular challenge, which this thesis addresses, is the provision of a suitable power conversion system which is able to interface the fuel cell to the aircraft electrical system - taking account of the complex electrical characteristics of the fuel cell and the demanding requirements of the aircraft electrical network.

The interleaved boost converter with coupled inductors (IBCI) is one of the many converters that is promising for fuel cell applications because it has low input current ripple and a high step-up voltage gain. It comprises a current doubler circuit, voltage doubler rectifier, coupled inductor and active clamp. The proposed converter is an extended version of the single phase to multiphase IBCI converter using interleaving techniques. The input stage of the converter is a coupled inductor which connected to a half-bridge configuration and an active clamp. The output side is a voltage doubler rectifier. A detailed analysis of the converter and associated modelling are presented. The design and construction of a prototype converter is presented with a particular focus on ensuring operability of the converter over the entire fuel cell characteristic range as well as achieving high efficiency at nominal load. A laboratory-scale (1/10) prototype of a nominal full-scale converter was built to verify the feasibility of the proposed converter topology. Good agreement between the experimental results and the simulation results has been demonstrated, which validates the converter design, modelling, and effectiveness of the efficiency evaluation approximations.

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List of Terms

- APU auxiliary power unit
- $AFC\,$ alkaline fuel cell
- $^{\circ}C\,$ degree Celsius
- $CCM\,$ continuous current mode
- $CO\,$ carbon monoxide
- C_{CL} clamp capacitor
- $\mathcal{C}_o\,$ output capacitor
- ${\cal CO}_2\,$ carbon dioxide
- $CO_3^{2-}\,$ carbonate ion
- $CH_4\,$ methane

D - duty cycle

- $DCM\,$ discontinuous current mode
- $DMFC\,$ direct methanol fuel cell
- E energy
- $e^-\,$ electron ion
- $ECS\,$ Environmental Control System
- ESR equivalent series resistance
- $FC\,$ fuel Cell
- f_{sw} switching frequency
- ${\cal H}^+\,$ hydrogen ion
- $HT-PEM\,$ high temperature polymer electrolyte membrane
- ${\cal I}_i\,$ input converter current
- i_L energy transfer inductance current
- $i_{Lm}\,$ magnetising inductance current

 ${\cal I}_N\,$ - base current

- I_o output converter current
- $j_{\boldsymbol{x}}\,$ normalised current
- K Kelvin temperature
- ${\cal K}_i\,$ normalised current ripple amplitude
- $kHz\,$ kilohertz
- kg kilogram
- $km\,$ kilometre
- $kVA\,$ kilovolt-amperes
- $kW\,$ kilowatt
- $L_{crit}\,$ critical inductance between DCM and CCM operating modes
- ${\cal L}_m\,$ magnetising inductance
- ${\cal L}\,$ energy transfer inductance
- ${\cal L}_{LK}\,$ leakage energy inductance
- $MCFC\,$ molten carbonate fuel cell
- ${\cal M}(D)\,$ voltage conversion ratio
- $MEA\,$ More Electric Aircraft
- n number of winding turns ratio
- N number of interleaving channels
- n_p number of primary turns
- n_p number of secondary turns
- No_x nitrogen oxides
- OH^- hydroxide
- $PBI\,$ polybenzimidazole
- ${\cal P}_N\,$ base power
- ${\cal Q}\,$ charge in capacitance
- ${\cal R}\,$ resistance load
- R_L series resistance

- $r_{i(Lm)}$ relative magnetising current ripple
- r_{CL} relative clamp capacitor voltage ripple
- $r_{Co}\,$ relative output capacitor voltage ripple
- ${\cal S}\,$ power device
- SO_x sulphur oxides
- $SOFC\,$ solid oxide fuel cell
- PAFC phosphoric acid fuel cell
- PEM polymer electrolyte membrane or proton exchange membrane
- RH relative humidity
- $T_{H\,}\,$ absolute temperature of the inlet gas
- $T_{C\,}\,$ absolute temperature of the outlet gas
- T_s switching period
- $T_{cell}\,$ fuel cell temperature
- $U_{\min}\,$ minimum voltage
- U_{max} maximum voltage
- V_{dc} direct current voltage
- $V_{\!A}\,$ three level voltage
- V_{CL} clamp voltage
- V_i input converter voltage
- $V_{N}\,$ base voltage
- $V_o\,$ output converter voltage
- V_x normalised voltage
- VSCF variable speed constant frequency
- WAI Wing Anti Icing
- X_L base impedance
- ZVS zero voltage switching
- Π_x normalised power
- $\vartheta\,$ phase shift angle

 $\alpha\,$ - dead angle

 $\beta\,$ - pulse duration

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Chapter 1

Introduction

1.1 More Electric Aircraft

Nowadays, the aircraft industry has grown rapidly both in the civil and military sectors, and the general trend for commercial aircraft has increased in size. For example, some of the current commercial aircrafts weigh over 30,000 kg with a generation power system of 1500 kVA and the aircraft is capable of long-haul flights up to 16,000 km[12].

In a conventional aircraft, the power needed for the subsystems utilises a combination of mechanical, electrical, hydraulic and pneumatic power sources and actuators [13]. The aircraft's main engine dispatches power to all these power systems through different methods. For example:

- The aircraft engine drives a shaft to generate mechanical power which is then supplied to lubrication pumps, fuel pumps, hydraulic pumps and electrical generators.
- Pneumatic power systems use compressed air to drive turbine motors for starting the engine and to supply the Wing Anti Icing (WAI) system and the Environmental Control System (ECS) which provides air, thermal control and cabin

pressurisation.

• Electrical power and hydraulic power subsystems are supplied throughout the aircraft for driving actuation systems such as flight control actuators, landing gear brakes, lights and commercial loads.

With the constant increase in the demand of electrical capacity, the system has become complicated and limited by the capability of the engine technology. In addition, several researches and statistics have shown that when electric generators are either driven by gas turbine auxiliary power unit (APU) or by the aircraft main propulsion system, the global in-flight efficiency is low, in the order of 30-40% whereas on the ground, the average fuel efficiency of the turbine APU generally drops to less than 20% with the main engines off. In addition, it produces undesirable noise and nitrogen oxides (NO_x) emission [14].

With the rise of environmental concerns and limitation of conventional engines, the trend in aircraft systems has moved onto the concept of "More Electric Aircraft - MEA" which is based on the idea of an increased use of electric power to drive aircraft subsystems. A comparison between conventional aircraft subsystems and more electric aircraft subsystems is shown in figure 1.1.

The concept of MEA is not a completely new idea, it has been introduced since World War II. However, during that period electric power generation capabilities and advanced power conversion technologies were still limited, so that the conventional aircraft architecture remained the favourite choice. Recently, the maturity of power electronics and machines technology has enabled the development of fault tolerant electric machines and electromechanical actuators and fuel cells which have renewed the interest in the MEA [15]. The modern aircraft electrical power systems require lower engine power with higher efficiency, improving fuel economy and performance.



Figure 1.1: Comparison between conventional aircraft systems and more electric aircraft systems (Source: How the More Electric Aircraft is influencing a More Electric Engine and More [1]).

The use of more electric systems integrated into the aircraft has broadened the research activities with a focus on the exploitation of the concept of MEA. The following are some of the research fields related to MEA:

- Electromechanical actuators (EMAs) for flight surface control [16].
- Electrically driven fuel pumps, oil system, and other engine accessories [15].
- Starter generators coupled through a gearbox or embedded within the engine.
- Converters for power conditioning, management and quality [17].
- Dynamic behaviour of aircraft power systems [18].
- Variable speed constant frequency (VSCF) power systems [19].
- Electrical generation for More Electric Aircraft (Auxiliary power unit APU) using solid oxide fuel cells and polymer electrolyte membrane fuel cells [17, 20].

The focus of this project is on the area of using fuel cells for aircraft auxiliary power unit (APU).

1.2 Auxiliary Power Unit

An auxiliary power unit (APU) is a small jet engine that provides energy for aircraft systems other than propulsion [21]. The alternator it drives generally produces 115 volts alternating current (AC) at 400 Hz, to run the electrical systems of the aircraft. The advantage of running high frequency (400 Hz) alternators rather than 50/60 Hz is that the system requires smaller transformers. Hence, much smaller and lighter transformers can be used which reduce the weight of the aircraft. However, there is a trade-off to this, which are higher losses and lower efficiency.

In most commercial aircraft, the APU is usually situated at the very rear of the aircraft just below the tail. The main purpose of the APU is to start the main engines. The main aircraft engines require much higher torque and power than a starter battery can generate to start-up, so the battery system starts the smaller APU engine which generates high pressure bleed air to start the main engines.



Figure 1.2: Photo of auxiliary power unit (APU).

The APU provides cabin air and electric power before starting the engines. Once the main engines are started, the APU will provide its secondary functions [21].

- Providing an emergency source of power in case of engine failure.
- Providing a source of bleed air for starting the aircraft engine mid-flight in an emergency.
- Providing power to air conditioning packs in the event that the aircraft requires takeoff with the engine bleed turned off.

During the flight, normally the APU system will be off but it will be turned on in the event of engine failure to provide secondary functions as described above.

1.3 Fuel Cells for Aerospace Applications

Although fuel cells have been used in many applications for several decades such as transportation, distribution power generation, residential power and portable power [2], the main focus of this project will be the use of fuel cells for aerospace application. Fuel cell technology started to be taken into consideration by the aerospace industry in 1950. General Electric and the US Air Force were the first two organisations that began development of fuel cells for aerospace applications [22, 23]. High power density is the most attractive feature of fuel cells in comparison to batteries because weight and size are very critical and important in aerospace applications. Fuel cells produce higher energy per equivalent unit of weight than batteries. A 5,000 psi tank of hydrogen and fuel cell can produce up to 600 watt-hours per kilogram which is 8-14 times higher than the power density of current batteries [24]. The first fuel cell for spacecraft was used in the Apollo missions in 1960 (1.3) [22]. It provided both electricity and drinking water for the astronauts on their journey to the moon and had an electrical power rating of 1.5 kW.


Figure 1.3: (a) Photo of Apollo13. (b) Diagram shows the internal module of Apollo13 (Source:13 Things that saved APOLLO 13 [2]).

Later, in 1970, International Fuel Cells developed a more powerful alkaline fuel cell for NASA's space shuttle orbiter [25]. It had 10 times more power than the previous fuel cells in a similar size. However, this was achieved using a high cost platinum catalyst. It was only used in NASA spacecrafts. The intense research and development at NASAs Glenn Research Center led to several new types of fuel cells which will be discussed later [23]. In 2004, Boeing started to develop a small airplane that uses fuel cells for airplane propulsion (Figure 1.4) to demonstrate the capabilities of fuel cell technology. According to [25], Boeing has prioritised the technology research for fuel efficiency, emission and noise. Miguel A. Herman, leader of the Boeing team stated that fuel cells are very attractive power units which he believes will be used in future aircraft to replace auxiliary power units. Fuel cell power units would reduce noise and the emissions produced. They also have higher efficiency. Hence, less fuel is used which would benefit the customers and environment. He explained: 'Fuel cells convert fuel directly into electricity and heat. They are environment-friendly as there is no combustion occurring in the process. In addition, the output product from the



fuel cell contains water which could be used on board. This reduces the amount of airplane carrying on a long-haul flight and reduces the fuel consumption' [26].

Figure 1.4: Innovative fuel-cell powered airplane from Boeing (Source: Boeing tests first hydrogen powered plane [3]).

Many manufacturers and others have a strong interest in developing fuel cells for aerospace applications. The main advantages of fuel cells are efficiency and reduced emissions. Fuel cells use an electrochemical process which directly converts fuel and oxidant into electricity. Their operating efficiency is considered very high, up to 60%, and is higher than any combustion engine. This can lead to a significantly reduced fuel consumption. In addition, fuel cells do not produce gaseous emissions and are therefore environment-friendly. However, fuel cells have also some peculiar disadvantages: they are not able to supply the peak power demanded by aircraft systems and they have very slow response [27] because of the natural electrochemical reactions on which the power generation principle is based. As a result of the slow reaction time of the fuel cells, an additional battery is needed to form a hybrid power generator and to supply the load during fast transient operation conditions. In addition, the output voltage of the fuel cell is not generally high enough for aerospace applications and requires an additional power conversion stage to boost it to the desired DC voltage level. The primary concern of this study is the development of the power conditioning for fuel cell based APU systems. A block diagram is depicted in figure 1.5.



Figure 1.5: A block diagram of fuel cell APU power system.

Oxygen and hydrogen are supplied to the fuel cells to generate an unregulated voltage ranging from 20 Vdc to 115 Vdc with current levels between 0 A to 600 A. However, the power generated from the fuel cell stacks is not suitable for the electrical load in the aircraft system at this point. Hence, a two stage power conversion unit is needed: a DC/DC boost converter and a voltage source inverter. Since the DC voltage generated by fuel cell stacks is low, a considerably high voltage conversion ratio boost converter is required to step-up the input voltage to the desired voltage level of 650 Vdc. Then, a three phase voltage source inverter converts the dc voltage from the previous stage to an AC voltage source of 230 Vac RMS. At this stage, the power is suitable to supply the aircraft electrical loads. Moreover, the fuel cell APU power system incorporates an auxiliary energy storage device (ultracapacitor or battery) for sudden load changes or start-up.

1.4 Objectives of the Research Project

This PhD research project is aimed at designing a suitable high step-up voltage gain and high current boost converter for a fuel cell-equipped auxiliary power unit (APU) based on reference fuel cell characteristics. The characteristics and project specifications are discussed later in this thesis. The proposed converter is expected to operate at high power with the low voltage and high current input. MOSFET technology with 20 kHz switching frequency is used to demonstrate the proposed converter. The main requirements for the converter are:

- Conversion of a wide DC input voltage (20-100V) to the desired output voltage (650V) within the tolerance range of 4.5% peak to peak voltage ripple to meet the aircraft electric power standards (MIL-STD-704F) [28].
- High average input current (600A) and input current ripple less than 4% peak to peak to enhance the life cycle of the fuel cells [29].
- Maximum power of 38.1 kW at full load and 20 kW at normal operation (light load). A full detailed specification of the fuel cell characteristics is given in Chapter 2.
- Capability of operating within the fuel cell characteristics over all the operating conditions.
- Efficiency must be as high as possible.

However, to avoid unnecessary cost and to be suitable for a laboratory test, a scaled version prototype rated for of 3.81 kW (10 times reduced from maximum power) has been constructed. All the requirements above remain the same except the average input current is dropped by 10 times (60 A).

The work done as part of the research project and described in this thesis seeks to achieve the following objectives:

- To research the fuel cell characteristics and operating conditions in order to define the input voltage range and maximum load power of the converter.
- To investigate existing high step-up boost converters and explore appropriate converter circuit modifications that can be potentially employed in fuel cell applications.
- To analyse and design the proposed high step-up converter to fulfil the project specifications.
- To derive a dynamic model of the proposed high step-up converter through nonlinear averaged modelling and linearised small signal modelling so that transfer functions can be obtained.
- To analyse the available degrees of freedom in the converter and their impacts on the converter performance so that the converter can be properly designed.
- To propose a loss estimation tool to predict the efficiency variation with different degrees of freedom, parameters and operating points so that the converter can be optimised to achieve high efficiency.
- To construct a laboratory-scale prototype of the proposed converter to validate simulation results and verify the efficiency.

1.5 Thesis Structure and Content

The thesis is structured as follows.

Chapter 2 introduces the general concept of fuel cell technology, with a focus on polymer electrolyte membrane (PEM) fuel cells. The advantages and disadvantages of existing topologies for fuel cell application are provided. In addition, the main components of a fuel cell are described. This information provides the characteristics of a voltage-current curve (often referred to as the polarisation curve) which is later used to set the operation constraints of the step-up DC-DC converter. Furthermore, a literature review of the previous research work on power converters is discussed especially in high step-up topologies.

Chapter 3 presents the operating principles of the single phase interleaved boost converter with coupled inductor. The converter is based on circuit modification of an existing high step-up converter. Two options of output configuration are discussed. The concept of a normalised unit system is introduced which will be used throughout the thesis. In addition, a detailed analysis of the steady state operation of the converter is given.

Chapter 4 presents the proposed converter (multiphase interleaved boost converter with coupled inductor). The advantages and disadvantages of the proposed converter are discussed. Furthermore, the steady state of the converter is analysed. Dynamic modelling using averaged and linearised models is undertaken. In addition, a duty cycle to output voltage transfer function is derived.

Chapter 5 introduces the design process for the converter parameters especially on the three main degrees of freedom. The impact of these parameters on the semiconductor device and passive component stresses are discussed. A tool for loss estimation is developed in MATLAB software to optimise the converter parameters, starting from the analytical steady state model of the converter. The semiconductor and passive component power loss modelling used in the MATLAB software is described. A PLECS software simulation is used to validate the analysis and design. The results of the final design of the converter are presented. The full power converter and laboratory-scale prototype scaling process is discussed.

Chapter 6 presents the design of the laboratory-scale prototype of the converter and the methodology followed in the construction process for software and hardware. There are two main circuits: Half-bridge clamp and voltage doubler circuit, and they are both presented in detail. In addition, the magnetic component (coupled inductor) and passive component selection and design are discussed. The measurement circuits for the voltages and currents are also given.

Chapter 7 presents the final experimental results obtained from the converter. These results are the compared with theoretical expectations. Experimental waveforms such as input current, input voltage, output current, output voltage, clamp capacitor voltages are shown and compared with the simulation results. The performance of the controller is discussed. In addition evaluation of the converter efficiency is also verified experimentally.

Chapter 8 concludes the work undertaken in this thesis. Some suggestions are included for the future work.

Chapter 2

Literature Review

2.1 Introduction

To properly design a step-up converter for fuel cell APU applications, a clear understanding of the fuel cell operation is needed. In this thesis, a reference fuel cell with maximum power output of 38.1 kW is selected as a case study and its output characteristics are used to define the input voltage range and maximum load power of the converter. The fuel cell characteristics and specifications are discussed in this chapter. Moreover, several high step-up boost converters that might be suitable for fuel cell applications are presented along with a discussion of the advantages and disadvantages of each topology.

2.2 Fuel Cell Overview

A fuel cell is an electrical device converting hydrogen, or hydrogen-containing fuels, directly into electrical energy. A fuel cell is different from a battery in that the fuel is continually supplied in the form of hydrogen and oxygen gas flows [30]. It produces electrical energy by the process of reverse electrolysis as illustrated by figure 2.1. The process starts when hydrogen is fed to the input "Anode" side where the catalyst causes the hydrogen atoms to release their electrons and become H^+ ions (protons):

$$2H_2 \to 4H^+ + 4e^- \tag{2.1}$$

The e⁻ electrons are then supplied to the outside electrical circuit before they reach the cathode side. There, the oxygen is supplied and combines with the electrons and hydrogen ions diffusing through the membrane to form water and a reaction that releases energy in the form of heat:

$$4H^+ O_2 \rightarrow 2H_2O + \text{energy(heat)}$$
 (2.2)



Figure 2.1: Fuel cell operation diagram (Source: New Energy and Fuel, 2016 [4]).

The water produced is removed from the cell to prevent any water flooding which will degrade the performance. In addition, any unused hydrogen and oxygen are exhausted from the cell anode and cathode outlets, respectively. The reaction is a continuous process within the cell and each cell produces an output voltage of around 0.7 V. In general, to obtain the desired amount of electrical power, several individual cells are connected in a series to form a fuel cell stack. Increasing the number of cells in the stack increases the voltage, while increasing the surface area of the cells increases the current.

Fuel cells offer many advantages over combustion engines and batteries. However, there are various advantages, which strongly depend on the fuel cell type, and this leads to different applications (Figure 2.2).



Figure 2.2: Chart to summarise main advantages of fuel cells for different types and applications (Source: Fuel cell system explained [6]).

• Efficiency: Fuel cells are not subject to the thermal bottleneck resulting from the second law of thermodynamics. The second Law states that no heat engine can use all the heat produced by a fuel to do work (although all mechanical work can be converted into heat) due to "thermal bottleneck" that strictly limits the efficiency of processes [6]. A combustion engine (or heat engine) needs to first convert chemical potential energy into heat and then mechanical work. During the mechanical work, several losses occur such as friction, mechanical losses, and leakages. The optimum (or "Carnot") thermodynamic efficiency of a heat engine is given by:

Carnot efficiency
$$(\eta) = 1 - \frac{T_C}{T_H}$$
 (2.3)

where:

 T_H = absolute temperature of the inlet(hot)gas (in °K). T_C = absolute temperature of the outlet(cold)gas (in °K).

The equation implies that the higher the temperature of the hot inlet gas entering the engine and the lower the temperature of the cold outlet gas after the expansion, the higher the Carnot efficiency. In theory, the hot gas temperature can be increased in order to achieve higher efficiency but the outlet temperature cannot be decreased lower than ambient temperature. However, the maximum upper temperature is limited by the engine material. In addition, in the internal combustion engine, the inlet temperature is the operating temperature of the engine, which is very much lower than the ignition temperature. Since fuel cells directly convert chemical energy into electrical energy, they are not affected by the thermal bottleneck and the efficiency of the fuel cells is significantly higher. The efficiency characteristics of fuel cells compared with other electric power generating systems are shown in figure 2.3.



Figure 2.3: Efficiency comparison of power generating systems (Source: Performance evaluation of fuel cell [5]).

- Low emissions: Fuel cells are electrochemical reactions which are considered as the cleanest fuel consuming energy with nearly zero emissions. The by-products of fuel cell reaction depend on the fuel used as its source. For example, a fuel cell vehicle produces only water if it is fed by compressed hydrogen, some CO, CO_2 and CH_4 if it is fed by ethanol and additional SO_2 if it is fed by gasoline. Fuel cell operation does not produce any undesirable products that contribute to the green house effect such as carbon monoxide CO or nitrogen oxides NO_x [31]. However, it is also worth noting that currently in the production of hydrogen as a fuel for fuel cells, there are CO_2 emissions involved in the process.
- **Good load-following**: Fuel cells have good electrical response to load change (good load-following characteristics) [25]. Fuel cells are like batteries that react chemically and instantly to generate variable amounts of electrical power

depending on the requirements of the load it is powering. However, fuel cell systems, are made of predominantly mechanical devices (e.g. valves) that have their own response time to change in load. For example, fuel cell systems using hydrogen as the source exhibit excellent overall response while those using a reformer can be sluggish if steam reforming techniques are used. In addition, the load-following capability of the fuel cell depends on its operating range. When the fuel cell is dominated by ohmic losses (no hysteresis), the cell voltage response in this range is up to 1-10 Hz. During the operating range where changes in cell voltage are dominated by activation losses, the dynamic response appears at lower frequencies (> 0.1 Hz) due to sluggish response in the voltage range near open circuit voltage [32].

• Low operating temperature: Fuel cell systems are suitable for automotive applications and aerospace applications due to their low operating temperatures (typically less than 100 °C)[25]. Fuel cells require little warm up time and high temperature hazards are reduced. However, the medium grade waste heat is harder to expel (especially in hot climates) so larger cooling systems are required and the electrochemical reaction could be slower than at high temperatures.

2.2.1 Fuel cell types

Fuel cells are commonly classified by the kind of electrolyte being used. There are six main classes of fuel cell that are viable systems for the present and near future [33]. These include alkaline fuel cell (AFC), proton exchange membrane fuel cell (PEMFC), direct methanol fuel cell (DMFC), phosphoric acid fuel cell (PAFC), molten carbonate fuel cell (MCFC) and solid oxide fuel cell (SOFC). A summary of the main features of each type of fuel cell is shown in table 2.1. In this study, the author will focus only on PEMFC, as the reference fuel cell for the project is PEM type.

Fuel Cell Type	Mobile Ion	Operating Temperature	Applications
Alkaline (AFC)	OH-	50-200 °C	Spacecraft e.g. Apollo, shuttle
Proton exchange membrane (PEMFC)	H+	30-100 °C	Transportation applications and low power stationary stations
Direct methanol (DMFC)	H^+	20-90 °C	Portable applications e.g. mobilephone, laptop
Phosphoric acid (PAFC)	H^+	220 °C	Large power stationary stations (200kW)
Molten carbonate (MCFC)	CO_3^{2-}	650 °C	Medium to large power stationary stations up to MW capacity
Solid oxide (SOFC)	O_2^-	500-1000 °C	Suitable for all sizes of power stationary stations (2kW to multi MW)

Table 2.1: Summary of different types of fuel cell

2.2.2 Proton exchange membrane (PEM) fuel cell specifications

Proton exchange membrane (PEM) fuel cell is also known as Polymer electrolyte membrane. The main parts of a fuel cell are illustrated in figure 2.4. The membrane-electrode assembly consists of polymer membrane, electrodes and gas diffusion layers.

The key part of the PEMFC is the proton conducting polymer membrane which is used as the electrolyte. The basic material used for the membrane is polyethylene which has been modified to extend its durability and chemical resistance. In the current market of PEMFC, the membrane is made of sulfonated fluoroethylene [34]. The main properties of these polymer membranes are high chemical resistance, capability of absorbing a lot of water and strong bonds (can be made into very thin film) [33]. Each of the electrodes comprises a layer of catalyst particles and attaches to either the membrane or the gas diffusion layer. The gas diffusion layer is made of a porous and electrically conductive layer such as carbon cloth. It provides two functions: first, it allows the reactants to diffuse into and out of the membrane-electrode assembly; second, it provides electric contact between the electrode and bipolar plate. The bipolar plates also contribute to many functions such as distribution of the reactant gas, conduction of electrical current from cell to cell, heat removal from the active area and prevention of reactant gases from leaking. The final parts are the end plates which are the input and output supplies of the fuel cell.



Figure 2.4: Internal parts of a PEM fuel cell (Source: Fuel cell store [7]).

Proton exchange membrane (PEM) fuel cells can be classified into two different types based on temperature performance: high temperature and low temperature PEM fuel cells. The temperature can influence the overall performance of a PEM fuel cell. There are several literature studies on how the temperature affects the fuel cell stack [35, 36]. For example, Yan et al.[36] studied the effect of temperature on performance



at different gas humidification temperatures, by using Gore PRIMEA 57.

Figure 2.5: Effect of cell temperature on the cell performance at humidification temperature of 50 °C (Source: PEM Fuel Cell Testing and Diagnosis [8]).

Figure 2.5 shows the fuel cell performance at different temperatures with a humidification temperature of 50 °C. As the temperature is increased from 30 to 50 °C, the fuel cell performance is increased. This can be explained by the enhanced electrode kinetic and increased membrane conductivity. However, a further increase in temperature from 50 to 70 °C causes the fuel cell to reduce in performance. This is because increases in temperature will cause the water inside membranes and electrodes to evaporate quickly, which reduces the kinetic performance of the fuel cell. Although increasing the temperature enhances the electrode kinetics and increases membrane conductivity, too much increase in temperature has negative impact on fuel cell performance. Therefore, this type of PEM is classified as a low temperature fuel cell.

Recently, the advance of technology led to a new type of membrane electrode assembly called Polybenzimidazole (PBI) membrane. This type of fuel cell is classified as HT-PEM fuel cell which normally has a temperature range of 120-200 °C [8]. The proton conductivity of a PBI membrane does not rely on its water content so it is operated without extra humidification (0% RH). Hence, the fuel cell performance increases with increasing temperature without having water dehydration and cell membrane issues as shown in figure 2.6. The maximum power density of the fuel cell increases linearly with temperature, which indicates suitability for high-temperature operation.



Figure 2.6: Effect of cell temperature on the cell performance of the HT-PEM fuel cell at ambient back-pressure, 0% RH, and different temperatures (Source: PEM Fuel Cell Testing and Diagnosis [8]).

The reference fuel cell under study is categorised as a HT-PEM fuel cell, with better performance at high temperature. During the start-up region, the fuel cell is controlled to draw a constant current of 600A to warm-up the fuel cell stack. This will reduce the start-up time and increase the performance of the fuel cell. In the steady-state region, after the fuel cell has been warmed-up, the piecewise-linear approximated current versus voltage characteristic is shown in figure 2.7 and the power versus voltage characteristic is shown in figure 2.8.



Figure 2.7: Current versus voltage characteristic of the reference fuel cell.



Figure 2.8: Power versus voltage characteristic of the reference fuel cell.

The graphs have been extrapolated from the fuel cell specifications, and are a qualitative reference to identify the required operation limits and constraints needed to design the power converter. The converter will operate between U_{min} and U_{max} as shown in curve A. This operating region is the most important region and the design of the converter will be oriented to the achievement of the highest efficiency in this operating area. However, there are other points that need to be taken into account as shown below.

• Accepting a certain variability in curve (A), due to fuel cell life cycle (caused, for instance, by current ripple at the output side), fuel compositions between hydrogen and oxygen, relative humidity (RH) and pressure etc. All these factors can affect the polarization curves of the fuel cell. For example, an increase in the fuel cell operating pressure can affect the reversible thermodynamic potential, such as the open circuit voltage, the exchange current densities of the electrode reactions, the membrane conductivity and the mass transfer properties. Overall, the fuel cell performance is enhanced as the fuel cell pressure increases as illustrated in figure 2.9.



Figure 2.9: Polarization curves of nafion $^{\textcircled{R}}$ -212 membrane-based PEM fuel cell at different back-pressure (Source: PEM Fuel Cell Testing and Diagnosis [8]).

However, pressurisation of the PEM fuel cell system can cause gas permeation (e.g. hydrogen and oxygen crossover), water management issues, increased cost, size and weight [8].

In addition, relative humidity (RH) has a large effect on the overall performance of a fuel cell. It significantly influences the reactant gas partial pressure and the electrode kinetics in a PEM fuel cell. Figure 2.10 shows the fuel cell performance at 120 °C and ambient back-pressure with different inlet RHs. It is clearly seen that the performance of the stack decreases dramatically with decreasing RHs. Conventional PEM fuel cells are typically operated near saturation (above 80% RH) to achieve high performance because the proton conductivity of the membranes depends on their water content [8].



Figure 2.10: Polarization curves of nafion $^{\textcircled{R}}$ -212 membrane-based PEM fuel cell at different relative humidity (Source: PEM Fuel Cell Testing and Diagnosis [8]).

• During the start-up period, the reference fuel cell will draw a 600A current from the stack to self-heat-up the stack itself. The start-up time is extremely critical as it limits the maximum generated power and the time needed to reach this maximum. This is the reason why the reference fuel cell draws large current at start-up, so that warm-up can be fast and start-up time can be minimised, for fast activation. However, if the maximum current of 600A cannot be drawn

from the stack, the fuel cell will operate but the start-up time will increase due to the longer time needed to reach maximum power, as depicted in figure 2.5.



Figure 2.11: Power versus time characteristic of the reference fuel cell.

To summarise the information discussed above, a converter design area can be defined based on the reference fuel cell characteristic curve as shown in figure 2.12. This can be classified into two regions: start-up and steady state.

Start-up region is a region where the fuel cell stack is controlled to draw a maximum current of 600A to warm-up the fuel cell. As a result, the start-up time reduces, the time to reach maximum power reduces and the efficiency of fuel cell increases. However, the information available from reference fuel cell, is not enough to clearly understand the start-up operation, and in particular to understand the dynamic voltagecurrent trajectories during the initial warm-up transient. In addition, there are other factors such as temperature, pressure, and relative humidity (RHs) that could affect the operating point. Hence, a conservative approach is required in the definition of the operating area used for the design of the power converter. As a worst case scenario, that covers all the possible start-up curves, it is assumed that during start-up the converter has to be able to operate at any points under the steady state curve with a low power boundary of 1 kW as a minimum operating point. The area has been highlighted in blue in figure 2.12.

Steady-state region is a region where the stack has been warmed-up and operates in its nominal condition. In this region, the curve has a linear behaviour. The voltage across the fuel cell stack ranges from 63.5 V to 88 V and power from 8800 W to 38100 W. However, a safety margin of $\pm 5\%$ is added to account for the several factors such as temperature, pressure and relative humidity, that could affect the polarization curves.



Figure 2.12: Design area (power versus voltage characteristic of reference fuel cell).

Table 2.2: Summary of reference fuel cell operation: generated current (Iin) and power (Power) as a function of fuel cell voltage (Vin). Vout is the expected output voltage of the DC-DC conversion stage

	Vin (V)	Iin (A)	Vout (V)	Iout (A)	Load (Ω)	Power (W)
	20.00	600.00	650.00	18.46	35.21	12000.00
	30.00	600.00	650.00	27.69	23.47	18000.00
Start-up	40.00	600.00	650.00	36.92	17.60	24000.00
load	50.00	600.00	650.00	46.15	14.08	30000.00
	60.00	600.00	650.00	55.38	11.74	36000.00
Full load	63.50	600.00	650.00	58.62	11.09	38100.00
	65.00	569.38	650.00	56.94	11.42	37009.96
	70.00	467.34	650.00	50.33	12.91	32714.08
Nominal	75.00	365.30	650.00	42.15	15.42	27397.80
load	80.00	263.26	650.00	32.40	20.06	21061.12
	85.00	161.22	650.00	21.08	30.83	13704.04
	88.00	100.00	650.00	13.54	48.01	8800.00
	90.00	96.85	650.00	13.41	48.47	8716.14
Light load	95.00	76.61	650.00	11.20	58.05	7278.05
	100.00	53.73	650.00	8.27	78.64	5372.60

2.2.3 DC/DC converter requirements

According to previous section, the reference fuel cell characteristics and specifications are summarised. This information is necessary to specify the requirements for the DC/DC converter. The main requirements for the converter are listed below and are summarised in table 2.3:

• Conversion of a wide DC input voltage (20-100V) to the desired output voltage (650V) within the tolerance range of 4.5% peak to peak voltage ripple to meet

the aircraft electric power standards (MIL-STD-704F)[28].

- High average input current (600A) and input current ripple less than 4% peak to peak to enhance the life cycle of the fuel cells [29].
- Maximum power of 38.1kW at full load and 20kW at normal operation (nominal load).
- Capability of operating within the fuel cell characteristics over all the operating conditions.
- Efficiency must be as high as possible.

	Vin	Iin	Power	Voltage	Iin	Vout
	(V)	(A)	(W)	gain	ripple (A)	ripple (V)
	20.00	600.00	12000.00	32.50	24.00	29.25
Stant up	30.00	600.00	18000.00	21.67	24.00	29.25
Start-up	40.00	600.00	24000.00	16.25	24.00	29.25
load	50.00	600.00	30000.00	13.00	24.00	29.25
	60.00	600.00	36000.00	10.83	24.00	29.25
Full load	63.50	600.00	38100.00	10.24	24.00	29.25
Nominal load	65.00	569.38	37009.96	10.00	22.78	29.25
	70.00	467.34	32714.08	9.29	18.69	29.25
	75.00	365.30	27397.80	8.67	14.61	29.25
	80.00	263.26	21061.12	8.13	10.53	29.25
	85.00	161.22	13704.04	7.65	6.45	29.25
	88.00	100.00	8800.00	7.39	4.00	29.25
	90.00	96.85	8716.14	7.22	3.87	29.25
Light load	95.00	76.61	7278.05	6.84	3.06	29.25
	100.00	53.73	5372.60	6.50	2.15	29.25

Table 2.3: Summary of converter requirements at different operating points (Full power)

However, to avoid unnecessary cost and to be suitable for laboratory test, a scaled version prototype rated for of 3.8kW (10 times reduced from maximum power) has been constructed. All the requirements above remain the same except the average input current is dropped by 10 times. Hence, the input current ripple is scaled by a factor of 10.

Table 2.4: Summary of converter requirements at different operating points (Proto-type for laboratory test - Reduced power)

	Vin	Iin	Power	Voltage	Iin	Vout
	(V)	(A)	(W)	gain	ripple (A)	ripple (V)
	20.00	60.00	1200.00	32.50	2.40	29.25
Stant	30.00	60.00	1800.00	21.67	2.40	29.25
Start-up	40.00	60.00	2400.00	16.25	2.40	29.25
load	50.00	60.00	3000.00	13.00	2.40	29.25
	60.00	60.00	3600.00	10.83	2.40	29.25
Full load	63.50	60.00	3810.00	10.24	2.40	29.25
Nominal load	65.00	56.94	3701.00	10.00	2.28	29.25
	70.00	46.73	3271.41	9.29	1.87	29.25
	75.00	36.53	2739.78	8.67	1.46	29.25
	80.00	26.33	2106.11	8.13	1.05	29.25
	85.00	16.12	1370.40	7.65	0.65	29.25
	88.00	10.00	880.00	7.39	0.40	29.25
	90.00	9.69	871.61	7.22	0.39	29.25
Light load	95.00	7.66	727.81	6.84	0.31	29.25
	100.00	5.37	537.26	6.50	0.22	29.25

2.3 High Step-Up Converters

The final goal of this study is to identify and design the suitable high step-up DC-DC converter for the fuel cell APU power system as described in figure 1.5. The electrical characteristics of the fuel cell under study have been given in the previous section, showing that fuel cells are not an ideal electrical power source, but have their own peculiar characteristic. A typical fuel cell stack has a wide input voltage range, depending on the load current, temperature and other factors related to environment of the fuel cell stacks. Therefore, a dedicated DC-DC converter stage needs to be capable of operating under different input voltages and wide load range. The main requirements of the converter are to provide the conversion of a DC input voltage (20-115 V) to the desired dc output voltage (650 V) and to limit the input peak to peak input current ripple to less than 4% and output peak to peak voltage ripple to 4.5%. According to [29], input current ripple higher than 4% can result in thermal issues in the fuel cell stacks and reduce the lifetime of the fuel cells. The output voltage ripple is limited to 4.5% to meet the United States aircraft electrical power standards MIL-STD-704F which defines a standardised power interface between an aircraft and its equipment.

In this section, several DC-DC converter topologies that are applicable to fuel cells are examined. Each topology has its own features and performance. Hence, it is important to choose the correct converter that provides the following functions; input current ripple control, wide input voltage operation without an additional start-up circuit, high conversion ratio with low input voltage and high current stress, a solution to leakage energy in order to respect the operation constraints and ability to fully utilise the fuel cell energy and maximise the efficiency.

The simplest and most common DC-DC converter is the boost converter which is capable of producing an output DC voltage higher than the input DC voltage. The circuit schematic is shown in figure 2.13.



Figure 2.13: Circuit diagram of boost converter.

The converter consists of an inductor, a power switch (MOSFET or IGBT), diode and capacitor. The key principle of the boost converter operation is the tendency of an inductor to resist changes in current. There are two main operation states of the converter. First, when the switch is closed, the inductor current increases and the inductor stores energy. When the switch is opened, the diode conducts, the current in the inductor decreases, and energy is transferred to the output capacitor and the load. The voltage conversion ratio M(D) of the boost converter can be found by applying the volt-second balance to the inductor over a switching cycle.

$$M(D) = \frac{V_o}{V_i} = \frac{1}{1 - D}$$
(2.4)

The above equation shows that the output voltage is controlled by the duty cycle and ideally infinity conversion ratio can be achieved $(D \rightarrow 1, M(D) \rightarrow \infty)$. However, in a practical boost converter, there are losses associated with inductor, diode and switch[37]. These losses can be properly modelled as an equivalent series resistance (ESR) to the passive components. Therefore, a more realistic voltage conversion ratio for boost converter can be written as:

$$M(D) = \frac{V_o}{V_i} = \frac{1}{1 - D} \cdot \frac{1}{\left(1 + \frac{R_L}{(1 - D)^2 R}\right)}$$
(2.5)

where R_L represents series resistance (ESR) and R is load. The voltage conversion ratio at different ESR to load conditions is plotted in figure 2.14.



Figure 2.14: Voltage conversion ratio at different ESR to load conditions.

In practice, the maximum conversion ratio of a boost converter is limited by the parasitic elements and when the boost converter operates at high step up, the efficiency is reduced and the voltage gain characteristic becomes highly non-linear, as shown in figure 2.14. The main advantages of this topology are the simple structure and low voltage stress across the switching device. However, since it is operated under hard switching, the output diode experiences reverse recovery, which worsens as the gain of the converter increases. Although the boost converter has the ability to control input current, the main issue of this converter is the maximum conversion ratio. In practice, it is lower than 6 due to the parasitic elements. This is far from the required voltage gain of 32.5. In order to operate at high voltage gain, several modifications to the traditional boost converter have been proposed. The following are some of the most common techniques that can increase the conversion ratio of the boost converter:

- Series [38] and cascade DC-DC converters [39, 40].
- Voltage multiplier [41, 42] and Voltage lift cells [43, 44, 45].
- Coupled inductor converters [46, 47, 48].
- Integration of DC-DC converters [49, 50, 51].
- Voltage-fed full-bridge converter and Current-fed full-bridge converter [52].

2.3.1 Series and cascade DC-DC converters

Series DC-DC boost converters

The basic arrangement for the series connection of converters is the three level converter (as shown in figure 2.15) [38]. It has twice the components of a standard boost converter and is equivalent to the connection of two boost converters one on top of the other, to form a voltage divider. The voltage at the mid point of the two capacitors is equal to $V_o/2$ if both capacitors have the same capacitance C_{o1} and C_{o2} .



Figure 2.15: Circuit diagram of the three level boost converter.

The operating principle of a three level boost converter is the same as the boost converter. In the boost converter, when the transistor is on, the inductor stores energy from the source and releases the energy to the output capacitor and load during the off phase. However, in a three level converter, the switching cycle is extended to $2T_s$. During $0 < t < T_s$, only the upper switching device (S_1) is on for a fraction of the period equal to the duty cycle D whereas the lower switching device (S_2) is off for the whole switching period. However, during $T_s < t < 2T_s$, the lower switching device (S_2) is on for a fraction of the period equal to the duty cycle D while the upper switching device (S_1) is off.

The voltage conversion ratio M(D) can be separated into two cases depending on the input voltage compared to the output voltage.

$$M(D) = \begin{cases} \frac{2}{(1-D)}, & for V_i < V_o/2 \\ \\ \frac{2}{(2-D)}, & for V_i > V_o/2 \end{cases}$$
(2.6)

Compared to a conventional boost converter, this topology can double the voltage gain and halve the voltage stress across the power devices so that low voltage devices can be employed to reduce conduction losses. The switching losses are reduced and the EMI noise is suppressed due to the lower dv/dt stress. However, the number of semiconductor switches is twice and the power devices operate under hard switching. Hence, the output diode reverse-recovery problem is still present.

Cascade DC-DC boost converter

The use of cascaded topology (as shown in 2.16) is an effective way to improve the voltage gain since the gain of each converter stage is multiplied resulting in a large global voltage step-up gain [39].



Figure 2.16: Circuit diagram of cascade boost converter.

The voltage conversion ratio of the cascade boost converter is equal to

$$M(D) = \frac{1}{1 - D_1} \cdot \frac{1}{1 - D_2} \cdot \cdot \cdot \frac{1}{1 - D_n}$$
(2.7)

However, the larger number of power switches, magnetic cores and control circuits increases the cost of these topologies. The power devices operate under hard switching and the diode reverse-recovery problem still exists. Moreover, the stability of the cascade structure is an issue due to the higher equivalent order of the transfer functions, that require a more careful control design.

Quadratic DC-DC boost converter

Quadratic DC-DC converters (as shown in figure 2.17) can reduce the cost by sharing common switches [41]. Although the switching components are reduced, the multiple power processing reduces the topology efficiency. This situation is exacerbated by high current stresses on the first power stage and the high voltage stresses on the last stage. The output diode reverse-recovery problem is still present.



Figure 2.17: Circuit diagram of a quadratic converter.

The voltage conversion ratio of a quadratic boost converter is given by

$$M(D) = \frac{1}{(1 - D_1)^2} \tag{2.8}$$

Summary: Series, cascade and quadratic DC-DC boost converters are able to provide extra boost factor to the traditional boost converter. However, in practice the parasitic components limit the conversion ratio below the desired voltage gain. Although, a multiple cascade configuration of boost converters can achieve very high voltage gain, the converter operates at high duty cycle and hard switching which significantly reduces the efficiency of the boost converter. Another issue is the stability of the cascade structure due to the higher equivalent order of the transfer functions.

2.3.2 Voltage multiplier

Voltage multiplier bridges [42] (as illustrated in figure 2.18(a-c)) are derived from the Cockcroft-Walton voltage multiplier for high-voltage generators [53]. The capacitors in the bridge are charged at twice input voltage and the output voltage is the sum of the voltages of the capacitors. Thus, by adding a voltage multiplication technique to the conventional boost converter, a very high voltage gain can be achieved depending on the number of voltage multiplier cells. However, these could lead to increased circuit cost and the introduction of a large amount of diode losses, degrading efficiency. In addition, this approach also experiences periodical shorting of part of the capacitors by the switch, which increases substantially the switch current stress and applies additional load on the input source.

The voltage conversion ratio of a voltage multiplier boost converter is given by

$$M(D) = \begin{cases} \frac{(n+1)-D}{(1-D)}, & n \text{ is an even integer} \\ \\ \frac{n+D}{(1-D)}, & n \text{ is an odd integer} \end{cases}$$
(2.9)

where n is the number of voltage multiplier cells.



Figure 2.18: Circuit diagram of a voltage multiplier cell. (a) General converter diagram. (b) Multiplier cell type 1. (c) Multiplier cell type 2.

Summary: Voltage multipliers are an interesting technique that can be applied to any boost converter to provide additional voltage gain. The extra boost factor depends on the number of voltage multiplier cells. However, periodical shorting of part of the capacitors by the switch is an issue. Moreover, the voltage multiplier cell has relatively poor voltage regulation and current capability which makes it suitable for a low output current and high resistance load because the output voltage rapidly drops off as load current increases. Therefore, combining a voltage multiplier cell with a conventional boost converter is not suitable for wide input voltage applications and high output voltage because output load resistance is varied and the output load current is high.

2.3.3 Coupled inductor converter

A simpler way to achieve voltage gain is to employ the turns ratio of a magnetic component, such as a transformer. If no isolation is required, the coupled inductor is used to provide high voltage gain as illustrated in figure 2.19 (a) [46].



Figure 2.19: Circuit diagram of (a) coupled inductor boost converter. (b) coupled inductor boost converter with voltage clamping. (c) coupled inductor boost converter with snubber circuit.

The coupled inductor has two windings. The primary winding serves as the filter inductor. The second winding operates as a voltage source in series to the power branch. The voltage gain can be extended by proper choices of the turns ratio of the coupled inductor. However, the main disadvantage of this topology is the effect of the leakage of the coupled inductor which could interact with switch and diode capacitances and cause ringing with consequent increase in voltage stress across the semiconductors, and EMI issues. In addition, the ringing spike on voltage and current waveforms may affect the controller of the converter and degrade the converter efficiency. Therefore, to protect the power switch, a higher voltage rating device with high $R_{ds(on)}$ is required. In addition, active clamps can be used to reduce the regenerative voltage as shown in figure 2.19 (b) or a snubber circuit can also be adopted to deplete the leakage energy as shown in figure 2.19 (c). However, additional circuitry means more losses and degradation of the conversion efficiency.

The voltage conversion ratio of the coupled inductor boost converter shown in (a) is given by

$$M(D) = \frac{1+nD}{(1-D)}$$
(2.10)

where n is the secondary to primary turn ratio (n_s/n_p) .

Summary: Although the coupled inductor boost converter with active clamp has an input inductor, the input current is not continuous which makes it unsuitable for fuel cell application as the ripple current is more than 4%. This ripple current will affect the fuel cell performance. In addition, the winding turns ratio will be relatively high in order to achieve the desired voltage gain which results in high leakage inductance. This could cause the ringing in the switch. Moreover, it is not suitable for high power and high input current because the size of the magnetic components is significant as there is no current sharing capability.

2.3.4 Integration of DC-DC converters

Integration of DC-DC converters is where a combination of different topologies are integrated together to extend the voltage gain. The most common integrated DC-DC converter is the Flyback-Boost converter which is derived by combining a conventional boost converter with a flyback converter. The inductor of the boost converter and the transformer of the flyback converter are integrated into a coupled inductor. The two converters share the same common switch. The circuit diagram is shown in figure 2.20.



Figure 2.20: Circuit diagram of flyback boost converter.

The voltage conversion ratio of a Flyback-Boost converter is given by

$$M(D) = \frac{1+nD}{(1-D)}$$
(2.11)

where n is the secondary to primary turn ratio (n_s/n_p) .

However, the Flyback-Boost converter experiences the same issues as the coupled inductor boost converter, in particular the parasitic oscillations caused by the leakage inductance of the coupled inductor. Another problem is related with the output power sharing between the two sub-converters that has an impact on the overall efficiency. The analysis in [49] reveals that when the secondary to primary turn ratio is large, the output voltage of flyback boost converter will be higher than the output
voltage of boost converter. Consequently, the output diode of the flyback converter section requires higher power handling capability, causing more losses. On the other hand, with a low turns ratio, the output diode of the boost converter will have more losses, reducing the efficiency of the converter. Therefore, maximum efficiency can be achieved when the two converters share the same output power.

Another example using integration of DC-DC converters is the Flyback-Boost converter with active clamp and voltage multiplier [54] which has an operating principle similar to the Flyback-Boost converter discussed above, except for the addition of galvanic isolation. In addition, the presence of an active clamp solves the leakage ringing issue, reduces EMI and losses and the voltage stresses across the semiconductor devices. Zero-voltage switching turn-on of the main switch can also be achieved by taking advantage of the short resonant interval associated with the the charge and discharge of switch output capacitance during dead times of the switches. Moreover, the voltage multiplier provides additional voltage gain to the converter.



Figure 2.21: Circuit diagram of a Flyback-Boost converter with active clamp and voltage multiplier.

The voltage conversion ratio of the Flyback-Boost converter with active clamp and voltage multiplier is given by

$$M(D) = \frac{n}{(1-D)}$$
(2.12)

where n is the secondary to primary turn ratio (n_s/n_p) .

Summary: Integration of DC-DC boost converters is a good technique to extend the voltage gain. It can use a combination of any converters such as flyback boost converter, forward boost converter, and coupled inductor boost converter with voltage multiplier cells. This provides an option to select the right converter that meets the specifications of the application. The characteristics of the overall converter depend on the converters that are used in combination.

2.3.5 Voltage-fed full-bridge converter and Current-fed fullbridge converter

The full-bridge boost converter is one of the most frequently implemented circuit configurations when a high step-up ratio and electrical isolation are required [55]. It uses a high frequency transformer to boost the input voltage to any desired output voltage level. The current stress in the semiconductor devices is half of the input current which is suitable in high power applications where it can reduce the number of parallel transistors. Furthermore, the transformer magnetising current can be both positive and negative and the flux in the core exploits the entire magnetic characteristic. Therefore, the core is optimally used, minimising the chance of core saturation .

The full-bridge converter can be classified into two types; voltage-fed and current-fed full-bridge converter.

Voltage-fed full-bridge converter The schematic of the voltage-fed full-bridge converter is shown in figure 2.22.



Figure 2.22: Circuit diagram of voltage-fed full-bridge converter.

The voltage conversion ratio of full-bridge converter shown is given by

$$M(D) = 2nD \tag{2.13}$$

where n is the turns ratio of secondary winding to primary winding $(n_s/n_p \text{ and duty} cycle D \text{ is limited to less than 0.5.}$

A disadvantage of the voltage-fed full-bridge converter is that in high voltage application the voltage stress across the output inductor is large. Hence, the size and cost of the inductor increases whereas the current-fed full-bridge converter does not require an output filter. In addition, the energy stored in the transformer leakage inductance can cause ringing across the switches.

Summary: The voltage-fed full-bridge converter is one of the most common converters to achieve high step-up, however, it is not suitable for fuel cell applications because the input current is discontinuous and it has no input current control option. Hence, the input current ripple cannot be controlled and instantaneous changes in current could affect the fuel cell performance and reduce the fuel cell stack lifetime. In addition, the duty cycle is limited to 0.5 which increases the transformer turns ratio for high step-up applications and as a consequence the leakage inductance is high and there are problems related to the leakage energy.

Current-fed full-bridge converter

In the current-fed full-bridge converter (as depicted in figure 2.23), an additional inductor is added to the input side. The input current can be smoothed and controlled through the input inductor which is a desirable feature for some applications such as those employing fuel cells. In addition, the nature of the current-fed full-bridge is a boost converter. It can boost input voltage without a step-up transformer whereas in the voltage-fed full-bridge converter, the input voltage is first reduced before the transformer boosts it up. Therefore, the transformer turns ratio in the current-fed full-bridge converter.



Figure 2.23: Circuit diagram of current-fed full-bridge converter.

The voltage conversion ratio of a current-fed full-bridge converter is given by

$$M(D) = \frac{n}{2(1-D)}$$
(2.14)

where n is the turns ratio of secondary winding to primary winding $(n_s/n_p \text{ and duty} cycle D \text{ is limited to higher than 0.5.}$

The disadvantage of the current-fed full-bridge converter is that start-up at low output voltage is critical, and a dedicated start-up circuit is required to prevent in-rush current during start-up from zero output [56]. Moreover, the switches experience high voltage stress so additional circuitry such as an active clamp must be added to limit stresses. In [57], an active clamp is added to the current-fed full-bridge converter

to alleviate the voltage ringing across the bridge switches by enabling zero-voltage switching.

Summary: The current-fed full-bridge converter with an active clamp is an interesting topology for fuel cell applications. It provides input current control, high voltage conversion ratio and a solution to the leakage energy. However, using this converter for the wide input voltage range is not suitable as it requires a dedicated start-up circuit when operating at low input voltage which increases the complexity and cost of the converter.

Table 2.5: Summary of the high step-up converters

Topology	Gain	Continuous current	Isolation	Reverse recovery	Soft- switching	Remark
				problem		
Traditional boost converter	Low	1	×	1	×	Not enough voltage gain
Series boost converter [38]	Low	1	×	1	×	Not enough voltage gain
Cascade boost converter [39]	Low	1	×	1	×	Not enough voltage gain
Quadratic boost converter [40]	Low	1	×	1	×	Not enough voltage gain
Voltage multiplier cell [41, 42]	High	1	×	1	×	Poor voltage regulation
Coupled inductor boost converter[46]	High	×	×	1	×	Output power sharing
Coupled inductor boost converter with voltage clamp [47]	High	×	×	×	1	Suitable for low current
Flyback boost converter [49]	High	1	×	1	×	Suitable for low current
Flyback boost converter with active clamp & voltage multiplier cell [54]	High	1	1	×	1	Good candidate
Voltage-fed full-bridge converter [55]	High	×	1	1	×	Duty cycle limit to 0.5
Current-fed full-bridge converter [56]	High	1	1	√	×	Requires start-up circuit

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2.4 Conclusions

In this chapter, a literature review of fuel cell technologies, especially considering proton exchange membrane fuel cells, was presented. The characteristics of the fuel cell selected as a case study were discussed as this information is necessary for designing the converter. The required design boundaries of the converter based on power versus input voltage, derived from the V-I characteristic curve of the fuel cell characteristics, were shown. In addition, several DC-DC converter topologies were reviewed which can be divided into five categories; series and cascade DC-DC converters, voltage multiplier cells, coupled inductor converters, integration of DC-DC converters, voltage-fed full-bridge converters and current-fed full-bridge converters. Series and cascade DC-DC converters are the most basic technique to extend the voltage gain of the boost converter, however the parasitic elements limit the output voltage below the desired voltage gain. In addition, there are several disadvantages such as hard switching, the diode reverse recovery problem and stability of the cascade structure. Adding a voltage multiplier cell to the boost converter can increase voltage gain depending on the number of voltage multiplier cells added. However the resulting arrangement has poor voltage regulation and current capability which makes it suitable for low output current and high resistance loads. The coupled inductor boost converter employs the turns ratio of a magnetic component to achieve high voltage gain. However the input current is discontinuous which is not suitable for fuel cell applications. The voltage-fed full-bridge converter also experiences the same issues as the coupled inductor version where the input current is discontinuous. The current-fed full-bridge converter requires a dedicated start-up circuit when operated at low input voltage which increases the complexity and cost of the converter. Integrated DC-DC converters are a combination of different topologies integrated together to extend the voltage gain so the characteristics of the converter depend on the combination. The flyback boost converter with active clamp and voltage multiplier cell is a good candidate for fuel cell applications. It has characteristics of continuous current, high voltage gain and is soft-switching. In the next chapter, an integrated DC-DC converter called the interleaved boost converter with coupled inductor and active clamp is presented.

Chapter 3

Single Phase - Interleaved Boost Converter with Coupled Inductors (IBCI)

In the previous chapter, several high step-up converter topologies were discussed, however they were unable to meet all the requirements of the fuel cell for aircraft application. Integrated DC-DC converters which are the combination of different topologies, integrated together to extend the voltage gain, could be a good candidate depending on the combination. In this chapter, the integrated DC-DC converter called an "interleaved boost converter with coupled inductors and active clamp (IBCI)" is introduced which combines a current doubler circuit, voltage doubler rectifier, coupled inductor and active clamp circuit. It is presented in [9] and the circuit configuration is shown in 3.1. The input side is the interleaved current doubler circuit which provides continuous current and input current control ability thanks to the interleaved operation cancelling the input current ripple. The output side is a voltage doubler rectifier. The output configuration is versatile and can be modified into a full-bridge rectifier. The proposed converter utilises the coupled inductor to provide additional voltage gain. Therefore, the IBCI converter is suitable for fuel cell and PV applications. In this chapter, the advantages and disadvantages of the IBCI converter will be discussed. Following that, converter operation at different operating modes is described, along with the soft-switching conditions. A steady state anlysis of the single phase IBCI converter which was proposed by [9] is given.



Figure 3.1: Circuit diagram and equivalent circuit of the proposed converter by [9] -Interleaved boost converter with coupled inductors (with voltage doubler rectifier).

3.1 Advantages and Disadvantages of the Converter

Advantages:

• The input current is evenly distributed and the current ripple is minimised by the interleaved operation. It divides the input current into two channels. Each channel is phase shifted by 180 degrees. The input current consists of two components; the secondary current reflected at the primary side and the magnetising current. The first component of current ripple is cancelled by the coupled inductor as the components are equal and opposite due to the phase shift. The second component of current depends on the duty cycle. Complete magnetising current cancellation can be achieved when the duty cycle is 0.5 for two-phase interleaved operation.

- Since it is a current-fed converter, it is possible to control the input current from the fuel cell. The input current is continuous, thus extending the fuel cell lifetime and increasing fuel cell performance.
- By introducing the active clamp scheme, zero-voltage switching (ZVS) softswitching operation is achieved for the primary switches and the auxiliary switches during turn-on within a given duty cycle range.
- A wide duty cycle operation range is possible, removing the need for an additional start-up circuit compared with the classic current-fed full-bridge converter (It can be operated above and below 50%).
- It is galvanically isolated which provides safety protection to the load. In addition, it has strong noise and interference blocking capability.

Disadvantages:

- The converter design is quite complex especially with regard to the coupled inductor winding ratio as this has the most impact on the component current and voltage stress, and on the efficiency of the converter.
- Energy transfer of the converter depends on the leakage inductance of the coupled inductor which requires accurate design.
- The control design is complex due to the high order system transfer function (Third-order system).
- The ZVS performance is limited and depends on the operation modes (CCM and DCM) and operating duty cycle which will be discussed in section 3.3.3.

3.2 Output Rectifier Configuration

At the output side there are two possible configurations to connect the coupled inductors with the load: full-bridge rectifier and voltage doubler rectifier. The full-bridge configuration gives an output voltage level that is the same as the voltage level in the coupled inductor while the voltage doubler rectifier doubles the coupled inductor voltage. Hence, twice the voltage gain can be achieved with a doubler rectifier. In this thesis, a voltage doubler rectifier will be selected as the output rectifier, as high voltage gain is desired.

3.2.1 Full-bridge rectifier configuration

The full-bridge rectifier configuration is represented in figure 3.2. Four diodes are required. When V_{AL} is positive (V_{AL} is the voltage across two coupled inductors and leakage inductor), diodes D_2 and D_3 are forward biased and the current charges the output capacitor C_o . When V_{AL} is negative, diodes D_2 and D_3 are reverse biased and do not conduct while D_1 and D_4 are forward biased and charge the output capacitor C_o .

3.2.2 Voltage doubler rectifier configuration

The voltage doubler rectifier is depicted in figure 3.3. Only two diodes are required. When V_{AL} is positive, diode D_2 is forward biased and charges the output capacitor C_{o2} . When V_{AL} goes negative, diode D_2 is reverse biased and does not conduct while diode D_1 is forward biased and charges the output capacitor C_{o1} . The capacitors are connected in series. Hence, the output voltage is twice the output capacitor voltage. The waveforms are shown in figure 3.3 (d).



Figure 3.2: Full-bridge rectifier configuration with current and voltage waveforms. (a) Circuit diagram. (b) Model when diode D_1 , D_3 on and diode D_2 , D_4 off. (c) Model when diode D_1 , D_3 off and diode D_2 , D_4 on.



Figure 3.3: Voltage doubler rectifier configuration with current and voltage waveforms. (a) Circuit diagram. (b) Model when diode D_1 on and diode D_2 off. (c) Model when diode D_1 off and diode D_2 on.

3.3 Converter Operation

To fully understand the converter operation, the analysis is divided into two operating modes: continuous conduction mode (CCM) and discontinuous conduction mode (DCM). In the CCM mode, the current through the energy transfer inductance (L) never goes to zero in a switching cycle, whilst in DCM the current in the energy transfer inductor reaches zero in the switching cycle. Moreover, in this converter the operating principle is also greatly affected by the duty cycle, in particular a different analysis must be provided for duty cycles above or below 0.5.

To analyse the steady-state operation several assumptions are made during one switching period T_s :

- The main switches S_1 and S_2 and auxiliary switches S_3 and S_4 are operated under dual asymmetrical pulse width-modulation with no deadtime. The duty cycle is defined based on the operating cycle of the main switches S_1 and S_2 .
- All the power MOSFET and diodes are ideal devices.
- The transistor parasitic capacitances and diode capacitances are zero.
- Passive components are linear, time-invariant and frequency-independent.
- The output impedance of the input voltage source V_i is zero.
- The magnetising inductances L_{m1} and L_{m2} are symmetrical $(L_{m1} = L_{m2} = L_m)$.
- The coupled inductor is modelled as a magnetising inductance L_m , an ideal transformer with a turns ratio of $n = n_p/n_s$, and a leakage inductance L.
- The ripple components of the magnetising inductor current I_{Lm} are considerably lower than the average magnetising current.
- The ripple components of the clamp capacitor voltage V_{Cl} and output capacitor voltage V_{Co} are negligible.

• The capacitance of the clamp capacitors C_{CL1} and C_{CL2} and output capacitors C_{o1} and C_{o2} are symmetrical ($C_{CL1} = C_{CL2} = C_{CL}$ and $C_{o1} = C_{o2} = C_o$). Since the ripple components of the clamp capacitor ($\Delta V_{CL1}=0$ and $\Delta V_{CL2}=0$) and output capacitor voltage ($\Delta V_{Co1}=0$ and $\Delta V_{Co2}=0$) are negligible, the clamp capacitor voltage for V_{CL1} and V_{CL2} and output capacitor voltage V_{Co1} and V_{Co2} are identical ($V_{CL1} = V_{CL2} = V_{CL}$ and $V_{Co1} = V_{Co2} = V_{Co}$).

3.3.1 Discontinuous conduction mode

Discontinuous conduction mode (DCM) is the operating mode where the current in the energy transfer inductance L reaches zero during one switching cycle. The value of energy transfer inductor in discontinuous current mode is below the minimum inductance L_{crit} needed to operate in continuous conduction mode. Hence, DCM generally occurs for light load operating condition.

$$L_{DCM} < L_{CCM}$$

The value of L_{crit} can be used to define the boundary between DCM and CCM operating mode.

$$L = \begin{cases} L < L_{crit}, & for DCM \\ \\ L > L_{crit}, & for CCM \end{cases}$$
(3.1)

where

$$L_{crit} = \frac{R_o F^2 |2D - 1|}{4f_{sw}}$$
(3.2)

 R_o is the output resistance Ω .

F is equal to 1 for full-bridge rectifier and 0.5 for voltage doubler rectifier.

D is duty cycle.

 f_{sw} is switching frequency Hz.

The energy stored in the inductor is proportional to the square of the current flowing through it $(E=\frac{1}{2}LI^2)$. At the same power level of the converter, the peak inductor current is higher in DCM operation compared to the CCM operation.

The operation in DCM can be further divided into two regions; duty cycle above 0.5 and duty cycle below 0.5.



3.3.1.1 DCM when duty cycle > 0.5



Figure 3.4: (a)-(f) Operation intervals at DCM >0.5. (g) Theoretical waveforms at the primary(input) side. (h) Theoretical waveforms at the secondary(output) side.

Interval 1 $[t_0 - t_1]$

At t_0 , the main switches S_1 and S_2 are already turned on and the auxiliary switches S_3 and S_4 are turned off. The voltage applied to the primary windings of the inductors is equal to V_i and the total secondary voltage across the two windings series connected with opposite polarity is zero. The diodes at the output side are reverse biased. Hence, there is no current flowing into the secondary windings. The magnetising currents I_{Lm1} and I_{Lm2} are linearly increasing:

$$i_{Lm1}(t) = i_{Lm1}(t_0) + \frac{V_i}{L_m}(t - t_0)$$
(3.3)

$$i_{Lm2}(t) = i_{Lm2}(t_0) + \frac{V_i}{L_m}(t - t_0)$$
(3.4)

Since both the output diodes D_1 and D_2 are reverse biased, the energy transfer inductor current i_L is zero. Thus, the current through the main switches i_{S1} and i_{S2} is the same as the magnetising current i_{Lm1} and i_{Lm2} , respectively during this interval.

Interval 2 $[t_1 - t_2]$

At $t=t_1$, the main switch S_2 is now turned off, causing the diode in antiparallel to the auxiliary switch S_4 to conduct. The current flows from source to drain which discharges the power device output capacitance and flows through the antiparallel diode. Hence, the auxiliary switch is zero-voltage switching (ZVS) turn-on which reduces the switching losses. The voltage across the first inductor is equal to input voltage V_i and the voltage across the second inductor is equal to input voltage minus the clamp capacitor voltage V_i - V_{CL} . Hence, the voltage across the two coupling inductors at the rectifier side is equal to:

$$V_A = \frac{V_i - (V_i - V_{CL})}{n}$$
$$V_A = \frac{V_{CL}}{n}$$
(3.5)

where

The clamp capacitor voltage is equal to that of a standard boost converter
$$V_{CL} = \frac{V_i}{1-D}.$$

Under this condition, the diode D_2 conducts and the current through the energy transfer inductance L increases linearly as:

$$i_L(t) = \frac{V_{CL} - nV_{Co}}{nL}(t - t_1)$$
(3.6)

The magnetising inductance current i_{Lm1} is continuously increasing while the magnetising inductance current i_{Lm2} decreases as the voltage applied to the magnetising inductor L_{m2} is equal to the difference between input voltage and clamp capacitor voltage $(V_i - V_{CL}/n)$.

$$i_{Lm1}(t) = i_{Lm1}(t_1) + \frac{V_i}{L_m}(t - t_1)$$
(3.7)

$$i_{Lm2}(t) = i_{Lm2}(t_1) + \frac{V_i - V_{CL}}{L_m}(t - t_1)$$
(3.8)

The main switch current i_{S1} linearly increases and is equal to the difference between the energy transfer inductor current reflected back to the primary side of coupled inductor and the magnetising current. The auxiliary switch current i_{S4} is equal to the difference between the energy transfer inductor current reflected back to the primary side of coupled inductor and the magnetising current.

$$i_{S1}(t) = i_{Lm1}(t) + \frac{i_L(t)}{n}$$
(3.9)

$$i_{S4}(t) = i_{Lm2}(t) - \frac{i_L(t)}{n}$$
(3.10)

Interval 3 $[t_2 - t_3]$

At $t=t_2$, before the S_2 is turned on, the negative current forces the anti-parallel diode across S_2 to conduct. Thus, the power device output capacitance is discharged and the switch is zero-voltage switching (ZVS) turn-on. The total voltage across the two series connected coupled inductors V_A is now cancelled again and the energy transfer inductor current is linearly decreasing because the voltage difference between two terminal points is equal to $-V_{Co2}$. Hence, the energy transfer inductor current can be written as:

$$i_L(t) = i_L(t_2) - \frac{V_{Co}}{L}(t - t_2)$$
(3.11)

The main switch current i_{S1} linearly decreases while the main switch current i_{S2} linearly increases as follows:

$$i_{S1}(t) = i_{Lm1}(t) + \frac{i_L(t)}{n}$$
(3.12)

$$i_{S2}(t) = i_{Lm2}(t) - \frac{i_L(t)}{n}$$
(3.13)

This interval ends when the energy transfer inductor current decreases to zero. In addition, both magnetising inductance currents i_{Lm1} and i_{Lm2} still increase and decrease respectively.

Interval 4 $[t_3 - t_4]$

In this interval the converter behaves as in interval 1. The main switches S_1 and S_2 remain on and the auxiliary switches S_3 and S_4 are opened. The energy transfer inductor current remains at zero. Both magnetising currents increase linearly under the applied input voltage.

Interval 5 $[t_4 - t_5]$

At $t=t_4$, the main switch S_1 is now turned off and the diode in antiparallel to the auxiliary switch S_3 conducts so the current discharges the power device output capacitance resulting in zero-voltage switching turn-on. The magnetising current i_{Lm2} continues to rise, while the magnetising current i_{Lm1} starts to fall:

$$i_{Lm1}(t) = i_{Lm1}(t_4) + \frac{V_i - V_{CL}}{L_m}(t - t_4)$$
(3.14)

$$i_{Lm2}(t) = i_{Lm2}(t_4) + \frac{V_i}{L_m}(t - t_4)$$
(3.15)

During this interval, the voltage across the two coupling inductors series connected at the rectifier side is equal to $-V_{CL}/n$. The diode D_1 is forward biased and conducts. The energy transfer inductor current linearly decreases as follows:

$$i_L(t) = \frac{nV_{Co} - V_{CL}}{nL}(t - t_4)$$
(3.16)

The main switch current i_{S2} increases while the auxiliary switch S_3 current decreases as follows:

$$i_{S2}(t) = i_{Lm2}(t) - \frac{i_L(t)}{n}$$
(3.17)

$$i_{S3}(t) = i_{Lm1}(t) + \frac{i_L(t)}{n}$$
(3.18)

Interval 6 $[t_5 - t_6]$

At $t=t_5$, the main switch S_1 has zero-voltage switching turn-on by the negative current that forces the antiparallel diode to conduct. The voltage across the two coupled inductors series connected at the secondary side is equal to zero so the current in energy transfer inductor decreases.

$$i_L(t) = i_L(t_5) + \frac{V_{Co}}{L}(t - t_5)$$
(3.19)

Both magnetising currents increase linearly with the applied input voltage. This interval ends when $t=t_6$, the energy transfer inductor current i_L reaches zero, causing the diode D_2 to be reverse biased. The currents in the main switches S_1 and S_2 are expressed as:

$$i_{S1}(t) = i_{Lm1}(t) + \frac{i_L(t)}{n}$$
(3.20)

$$i_{S2}(t) = i_{Lm2}(t) - \frac{i_L(t)}{n}$$
(3.21)

This operating interval ends when the energy transfer inductor current increases until it reaches zero. This also completes the switching cycle and starts next switching cycle in interval 1.

3.3.1.2 DCM when duty cycle < 0.5

In DCM when the duty cycle is less than 0.5, different operation occurs and the operating intervals and theoretical waveforms are shown in figure 3.5. The waveforms are similar to the previous operating mode (DCM when duty cycle is larger than 0.5). The main difference between these two operating modes is that when the total voltage of the two series connected coupled inductors at the output rectifier side is zero, the auxiliary switches S_3 and S_4 are now both turned on as shown in figure 3.7 (a), (c), (d) and (f) while both the main switches S_1 and S_2 are turned on as in the previous operating mode. Therefore, the auxiliary switches S_3 and S_4 are turned on as in the forevious operating mode. Therefore, the auxiliary switches is negative and flows from source to drain so the output capacitance is discharged. However, the

main switches S_1 and S_2 are operated in hard-switching. In addition, the current in the main switches S_1 and S_2 are both positive.





Figure 3.5: (a)-(f) Operation intervals at DCM <0.5. (g) Theoretical waveforms at the primary(input) side. (h) Theoretical waveforms at the secondary(output) side.

3.3.2 Continuous conduction mode

In this operating mode, the current passing through the energy transfer inductor is always greater than zero during a switching cycle. The operating intervals and waveforms are depicted in figure 3.6 and 3.7. Also the CCM can be divided into two different conditions, based on the duty cycle: duty cycle greater than 0.5 and duty cycle lower than 0.5.

3.3.2.1 CCM when duty cycle > 0.5

Interval 1 $[t_0 - t_1]$

At t_0 , the main switches S_1 and S_2 are already turned on and the auxiliary switches S_3 and S_4 are turned off. The voltage applied to the primary windings of the inductors is equal to V_i and the secondary voltage across the two series connected windings is zero. The magnetising current i_{Lm} is linearly increasing:

$$i_{Lm1}(t) = i_{Lm1}(t_0) + \frac{V_i}{L_m}(t - t_0)$$
(3.22)

$$i_{Lm2}(t) = i_{Lm2}(t_0) + \frac{V_i}{L_m}(t - t_0)$$
(3.23)

The output diode D_1 conducts and the total voltage across the two coupled inductors series connected at the rectifier side is equal to zero as the two voltage contributions cancel each other. The current flowing through the energy transfer inductor increases as follows:

$$i_L(t) = i_L(t_0) + \frac{V_{Co}}{L}(t - t_0)$$
(3.24)









Primary Side Waveforms





Figure 3.6: (a)-(f) Operation intervals in CCM >0.5. (g) Theoretical waveforms at the primary(input) side. (h) Theoretical waveforms at the secondary(output) side.

The current passing through S_1 is equal to the sum of the magnetising current and the current reflected back from the energy transfer inductor into the primary side of the coupled inductor, while the current flowing through S_2 is the difference between the magnetising current and the current reflected back from the energy transfer inductor into the primary side of the coupled inductor.

$$i_{S1}(t) = i_{Lm1}(t) + \frac{i_L(t)}{n}$$
(3.25)

$$i_{S2}(t) = i_{Lm2}(t) - \frac{i_L(t)}{n}$$
(3.26)

Interval 2 $[t_1 - t_2]$

At $t=t_1$, the main switch S_2 is now turned off, causing the diode in antiparallel to the auxiliary switch S_4 to conduct. In addition, zero-voltage switching turn-on (ZVS) can be obtained, reducing switching losses. Then, the auxiliary switch S_4 is turned on. The voltage across the first inductor is equal to input voltage V_i and the voltage across the second inductor is equal to input voltage minus the clamp capacitor voltage V_i-V_{CL} . Hence, the voltage across the two coupled inductors series connected at the rectifier side is equal to:

$$V_A = \frac{V_i - (V_i - V_{CL})}{n}$$
$$V_A = \frac{V_{CL}}{n}$$
(3.27)

The diode D_1 is still conducting and the energy transfer inductance L current increases linearly until it reaches zero and ends this interval:

$$i_L(t) = i_L(t_1) + \frac{V_{CL} + nV_{Co}}{nL}(t - t_1)$$
(3.28)

The magnetising inductance current i_{Lm1} continues to rise while the magnetising inductance current i_{Lm2} reaches its peak at t_1 and then starts to decrease as follows:

$$i_{Lm1}(t) = i_{Lm1}(t_1) + \frac{V_i}{L_m}(t - t_1)$$
(3.29)

$$i_{Lm2}(t) = i_{Lm2}(t_1) + \frac{V_i - V_{CL}}{L_m}(t - t_1)$$
(3.30)

The current flowing through the main switch S_1 continues to rise while the main switch S_2 is off and current passes through the auxiliary switch S_4 instead.

$$i_{S1}(t) = i_{Lm1}(t) + \frac{i_L(t)}{n}$$
(3.31)

$$i_{S4}(t) = i_{Lm2}(t) - \frac{i_L(t)}{n}$$
(3.32)

Interval 3 $[t_2 - t_3]$

At $t=t_2$, the current in the energy transfer inductance reaches zero, all the switches maintain the same state as in the previous interval. However, the diode D_1 stops conducting and the diode D_2 starts conducting. The energy transfer inductor current continues to increase as follows:

$$i_L(t) = \frac{V_{CL} - nV_{Co}}{nL}(t - t_2)$$
(3.33)

The magnetising inductance currents in both i_{Lm1} and i_{Lm2} , main switch current i_{S1} and auxiliary switch i_{S4} continue to rise at the same rate as in the previous interval.

Interval 4 $[t_3 - t_4]$

At $t=t_3$, before the S_2 is turned on, the negative current forces the antiparallel diode across S_2 to conduct which gives the switch zero-voltage switching turn-on (ZVS).

The voltage across the series connection of the two coupled inductors V_A cancels again in this interval and the energy transfer inductor current is linearly decreased because the voltage across the inductor is equal to $-V_{Co}$. Hence, the energy transfer inductor current is:

$$i_L(t) = i_L(t_3) - \frac{V_{Co}}{L}(t - t_3)$$
(3.34)

*Remark the slope of the energy transfer inductor current during interval 1 and interval 4 is the same but in the opposite direction.

The magnetising current in L_{m1} continues to rise while magnetising current in L_{m2} starts to increase again.

$$i_{Lm1}(t) = i_{Lm1}(t_3) + \frac{V_i}{L_m}(t - t_3)$$
(3.35)

$$i_{Lm2}(t) = i_{Lm2}(t_3) + \frac{V_i}{L_m}(t - t_3)$$
(3.36)

The current through the main switch S_1 begins to drop while the one through the main switch S_2 starts to increase.

$$i_{S1}(t) = i_{Lm1}(t) + \frac{i_L(t)}{n}$$
(3.37)

$$i_{S2}(t) = i_{Lm2}(t) - \frac{i_L(t)}{n}$$
(3.38)

Interval 5 $[t_4 - t_5]$

At $t=t_4$, the main switch S_1 is now turned off and the diode in antiparallel to the auxiliary switch S_3 conducts, resulting in zero-voltage switching turn-on. The magnetising current i_{Lm2} continues to rise, while the magnetising current i_{Lm1} starts to decrease:

$$i_{Lm1}(t) = i_{Lm1}(t_4) + \frac{V_i - V_{CL}}{L_m}(t - t_4)$$
(3.39)

$$i_{Lm2}(t) = i_{Lm2}(t_4) + \frac{V_i}{L_m}(t - t_4)$$
(3.40)

The energy transfer inductor current continues to drop as in the previous interval (4), at the same rate as in interval (2).

$$i_L(t) = i_L(t_4) - \frac{V_{CL} + nV_{Co}}{nL}(t - t_4)$$
(3.41)

The main switch current S_1 stops to flow and is flowing into auxiliary switch S_3 while the main switch current S_2 continues to increase.

$$i_{S2}(t) = i_{Lm2}(t) - \frac{i_L(t)}{n}$$
(3.42)

$$i_{S3}(t) = i_{Lm1}(t) + \frac{i_L(t)}{n}$$
(3.43)

This interval ends when energy transfer inductance current i_L drops to zero.

Interval 6 $[t_5 - t_5]$

In this interval, all the states of the switches remain the same as in the previous interval. However, diode D_1 now becomes reverse biased and stops to conduct while diode D_2 starts to conduct. The energy transfer inductor current continues to decrease as follows:

$$i_L(t) = i_L(t_5) - \frac{V_{CL} - nV_{Co}}{nL}(t - t_5)$$
(3.44)

The magnetising inductance currents i_{Lm1} and i_{Lm2} and the switch currents i_{S2} and i_{S3} continue change with the same trend as in the previous interval.

3.3.2.2 CCM when duty cycle < 0.5

In CCM when duty cycle is less than 0.5, the operating intervals and the theoretical waveforms are shown in figure 3.7. The waveforms and operating intervals are similar to discontinuous conduction mode when duty cycle is larger than 0.5. The main difference between these two operating conditions is that when the sum of the two coupled inductors voltages at the output rectifier side is zero, the auxiliary switches S_3 and S_4 are now both turned on as shown in figure 3.7 (a) and (d) and both the main switches S_1 and S_2 are turned on like in the previous operating mode. Therefore, the auxiliary switches S_3 and S_4 are turned on with zero-voltage switching. The current is negative and discharges the power device output capacitance. The main switches S_1 and S_2 are operated in hard-switching. The current is positive and flows from drain to source.





Figure 3.7: (a)-(f) Operation intervals in CCM <0.5. (g) Theoretical waveforms at the primary(input) side. (h) Theoretical waveforms at the secondary(output) side.

3.3.3 Soft-switching condition

There are two types of switching in power devices, hard-switching and soft-switching. Consider for instance the turn-on commutation with inductive load. The difference between hard and soft-switching is that during hard-switching turn-on, a voltage equal to at least the input voltage is supplied to the power device and the current is flowing from drain to source, resulting in high turn-on losses as shown in figure 3.8. On the other hand, soft-switching turn-on can be achieved if the current flows from source to drain. In this case, the current discharges the power device output capacitance (C_{oss}) before turning the device on. Hence, the turn-on loss is eliminated.



Figure 3.8: Diagram and waveforms of hard turn of a MOSFET with inductive load (Source: Zero-voltage switching full-bridge converter:operation, FOM, and guidelines for MOSFET selection [10]).

In soft-switching, initially the parasitic diode is conducting and when the power device turns-on, the current commutates to the channel. Figure 3.9 shows the difference between hard-switching and soft-switching. In soft-switching, during the switch turnon transition, the drain source voltage reaches zero before the gate voltage starts to rise (turn-on). Thus, there is almost zero overlap between voltage and current, and minimum loss.



Figure 3.9: Drain to source voltage and current of MOSFET waveforms for (a) hardswitching waveforms. (b) soft-switching waveforms (zero-voltage switching turn-on) (Source:Zero-voltage switching full-bridge converter: operation, FOM, and guidelines for MOSFET selection).

As mentioned previously when discussing the converter operation, the interleaved coupled inductor boost converter can be operated in soft-switching (zero-voltage switching) turn-on. The power device turn-on transitions occur at zero voltage under certain conditions. However, the soft-switching operation is limited and dependent on the sign of the current flowing in the devices. Soft-switching can be achieved if the switch current is enough to charge/discharge the switch output capacitances. The analysis can be separated into two cases corresponding to $D \leq 0.5$ and D > 0.5.

A: When duty cycle $D \le 0.5$

Two possible soft-switching commutations occur in this case, as shown in figure 3.10. The commutation between main switch S_1 and auxiliary switch S_3 occurs at angle $\theta = \theta_2$ for CCM and θ_1 for DCM operation.



Figure 3.10: Waveforms (a) CCM operation with $D \le 0.5$. (b) DCM operation with $D \le 0.5$.

The current through the switch S_1 is given by:

$$i_{S1} = \begin{cases} = i_{S1}(\theta_2) = I_{Lm(peak)} + \frac{I_2}{n}, & for CCM operation \\ = i_{S1}(\theta_1) = I_{Lm(peak)} + \frac{I_1}{n}, & for DCM operation \end{cases}$$
(3.45)

where $I_{Lm(peak)}$ represents the magnetising current peak value. It is equal to average magnetising current plus half of the ripple current $(I_{Lm(peak)} = \overline{i}_{Lm} + (\Delta i_{Lm}/2))$.

Since both the terms of equation 3.45 are positive in both CCM and DCM mode, the current flows from source to drain to discharge the power device output capacitance.

The voltage across the device is zero during the turn-on. Hence, zero-voltage switching turn-on can be achieved for the auxiliary switch S_3 in the entire load range.

2. The commutation between the auxiliary switch S_3 and main switch S_1 occurs during interval $\theta = 0$ for both CCM and DCM operation. The current through switch S_3 is given by:

$$i_{S3} \begin{cases} = i_{S3}(0) = I_{Lm(trough)} - \frac{|I_o|}{n}, & for CCM operation \\ = i_{S3}(0) = I_{Lm(trough)}, & for DCM operation \end{cases}$$
(3.46)

where $I_{Lm(trough)}$ is the magnetising current trough value. It is equal to average magnetising current minus half of the ripple current $(I_{Lm(trough)} = \overline{i}_{Lm} - (\Delta i_{Lm}/2))$.

The value of equation 3.46 needs to be negative in order to achieve zero-voltage switching turn-on. Hence, in CCM at low output power levels, the current in the main switch (S_1) is positive, losing zero-voltage switching turn-on. The current flows from drain to source, the power device output capacitance does not discharge so the drain to source voltage across device still exists. Whereas in DCM operation the switch always operates in hard-switching as the current is always positive in the assumption of small ripple in the magnetising inductor current.
B: When duty cycle D > 0.5



Figure 3.11: Waveforms (a) CCM operation with D > 0.5. (b) DCM operation with D > 0.5.

1. Two possible soft-switching commutations occur during this interval as shown in figure 3.11. The commutation between the main switch S_1 and the auxiliary switch S_3 occurs at angle $\theta = \pi$ for both CCM and DCM operation.

The current flows through switch S_1 is given by

$$i_{S1} \begin{cases} = i_{S1}(\pi) = I_{Lm(peak)} + \frac{|I_o|}{n}, & for CCM operation \\ = i_{S1}(\pi) = I_{Lm(peak)}, & for DCM operation \end{cases}$$
(3.47)

Since both the terms of equation 3.47 are positive in both CCM and DCM mode, the current flows from source to drain to discharge the power device output capacitance. The voltage across the device is zero during the turn-on. Hence, zero-voltage switching turn-on is guaranteed for the auxiliary switch S_3 in the entire load range.

2. The commutation between the auxiliary switch S_3 and the main switch S_1 occurs during interval $\theta = \theta_5$ for CCM operation and θ_4 for DCM operation. The current through switch S_3 is given by:

$$i_{S3} \begin{cases} = i_{S3}(\theta_5) = I_{Lm(trough)} - \frac{|I_2|}{n}, & \text{for } CCM \text{ operation} \\ \\ = i_{S3}(\theta_4) = I_{Lm(trough)} - \frac{|I_1|}{n}, & \text{for } DCM \text{ operation} \end{cases}$$
(3.48)

The value of equation 3.48 needs to be negative in order to achieve zero-voltage switching turn-on of the main switch. The current during this period coincides with the clamp capacitor current i_{CL} which has a zero average value at steady state. As the value of i_{sw} is monotonically decreasing in the interval $0 \leq \theta \leq \theta_2$ the value at the end is opposite sign with respect to its initial value. Hence, in this case, the value of i_{sw} is always negative and the main switch S_1 is always operated under zerovoltage switching turn-on. This does not apply to case a when duty cycle ≤ 0.5 because current i_{sw} does not monotonically decrease during the auxiliary switch (S_3) conduction interval as the value of the energy transfer inductance current i_L changes sign in the interval $[\theta_2,\pi]$ for CCM operation and in the interval $[\theta_1,\theta_2]$ for DCM operation.

In conclusion, zero-voltage switching turn-on can be achieved across all the load range for auxiliary switch S_3 both when duty cycle $D \leq 0.5$ and D > 0.5. Also, the main switch S_1 is always operated in zero-voltage switching turn-on if duty cycle D > 0.5 while for duty cycle $D \leq 0.5$ it is operated in soft-switching turn-on only if equation 3.46 gives a negative commutation current. Therefore, this suggests that the converter operation should be shifted toward the range where duty cycle D > 0.5as much as possible in order to achieve zero-voltage switching turn-on of both the switches. However, there is a trade-off in doing this as this choice will increase the voltage and current stress on the components, and increase the maximum operating duty cycle, with potential impact on conduction loss.

3.4 Normalised Unit System

In this thesis, the circuit analysis is carried out by appropriate scaling of all the variables, normalised with respect to a defined base quantity. In addition, the time variable is re-scaled to dimensionless units. Each quantity is therefore expressed in a normalised unit system (or per unit system) when it is divided by the base quantity.

The followings are the advantages of using a normalised unit system when analysing a power converter:

- It gives a set of relations linking voltage, current, power and impedance of the system that are not dependent on the specific ratings of the converter. This is useful when we want to compare two or more different systems that may not be designed for the same ratings.
- In a large system such as power generation, transmission, and distribution system where the system is complex, the normalised unit system can simplify the entire system into a simpler form. This will give a clearer concept of the system.
- It is ideal when we want to simulate the system and analyse the possible outputs under different conditions.
- The basic circuit laws are still valid when analysing the circuit using a normalised unit system.
- The normalised unit quantities are the same on either side of a transformer. If we normalise an impedance to the base on one side of the transformer, and then refer this normalised unit to the other side, both sides will have the same normalised unit and in the normalised unit system the turns ratio of the transformer is unity and it can be removed from the circuit.

There are some minor disadvantages in using a normalised unit system. For example, some equations in the non-normalised circuit are modified when scaled into the normalised one and care must be taken for factors such as $\sqrt{3}$ or 3 that could be

removed or added to the system. In addition, some circuit components are modified and become more abstract. For instance, in the normalised unit system sometimes phase shifts whose effect is clearly evident in the non-normalised circuit, are hidden by the normalisation.

In this chapter, the circuit analysis is carried out by selecting the base value of voltage and impedance. The base voltage is chosen as the output rectifier voltage (V_B) and the base impedance is the energy transfer inductance (L) in figure 3.1. Other base quantities like current and power are derived by applying the basic laws of electrical circuits. In addition, the normalised unit impedance remains unchanged when referred to one side of a coupled inductor or to the other. The turns ratio of the coupled inductor becomes unity. Thus, in circuit analysis the coupled inductor can be eliminated.

The base and normalised quantities used in the circuit analysis are summarised as follows:

Base voltage:	$V_N = V_B$
Base impedance:	$X_L = 2\pi f_{sw} L$
Base current:	$I_N = \frac{V_N}{X_L}$
Base power:	$P_N = \frac{{V_N}^2}{X_L}$
Normalised current:	$j_x = \frac{i_x}{I_N}$
$Normalised \ voltage:$	$u_x = \frac{v_x}{V_N}$
Normalised power:	$\Pi_x = \frac{p_x}{P_N}$

Remark: The lower case letters are time varying variables, while the upper case letters are constant variables.

3.5 Steady State Analysis of the 1 Phase IBCI Converter

In this section, the steady state analysis is focused on the energy transfer from source to load through the energy transfer inductance. This is so the converter voltage gain can be derived as proposed by [9]. Since the input side has a coupled inductor, the analysis is carried out based on the normalised unit system. In the normalised system, the impedance remains unchanged when referred to one side of coupled inductor or to the other. The turns ratio of the coupled inductor becomes unity. Thus, the analysis can be simplified as the coupled inductor is eliminated.

The interleaved boost with coupled inductors converter can be studied by referring to the simplified equivalent circuit depicted in figure 3.12 (b). The three level voltage source $v_A(\theta)$ (where $\theta = 2\pi f_{sw}t$ and f_{sw} is a switching frequency) is the sum of the two series connected coupled inductor voltages in opposite polarity at the rectifier side. The energy transfer inductance L determines the power flowing from the source to the load. The output rectifier reflects the output voltage $v_B(\theta)$, generating an AC waveform in phase with the energy transfer inductor current.



Figure 3.12: (a) Circuit diagram at rectifier side. (b) Simplified equivalent model.

As discussed in the previous sections, the waveforms used for analysis can be divided into four different cases: CCM when duty cycle above 0.5, CCM when duty cycle less 0.5, DCM when duty cycle above 0.5 and DCM when duty cycle less 0.5. All the main waveforms corresponding to the different modes are shown in figure 3.13. Several angle notations are introduced; φ is phase shift angle, β is pulse duration and α is dead angle.



Figure 3.13: Converter waveforms. (a) CCM operation when D > 0.5. (b) CCM operation when $D \le 0.5$. (c) DCM Operation when D > 0.5. (d) DCM operation when $D \le 0.5$.

Applying volt-second balance across each coupled inductor magnetising inductance, the average voltage across each inductor in steady state must be zero.

$$\overline{V_L} = \frac{1}{L} \int_0^T V_L dt = 0$$
$$V_i DT = (nV_A - V_i)(1 - D)T$$

Hence, the amplitude V_A of the three level voltage v_A is related to the input voltage V_i by the following equation:

$$V_A = \frac{V_i}{n(1-D)} \tag{3.49}$$

where $n = \frac{n_p}{n_s}$ is the turns ratio of each coupled inductor and n_p is the primary number of turns and n_s is the secondary number of turns. For example, from figure 3.13 (b) during interval $0 \le \theta \le \theta_2$, the main switch S_1 and the auxiliary switch S_4 are turned on. The coupled inductor primary voltages are V_i and $V_i - V_{CL}$, respectively, so the voltage $v_A(\theta)$ which is the sum of two coupled inductors at the rectifier side is equal to $(1/n)(V_i-(V_i-V_{CL})) = V_{CL}/n$. The clamp capacitor voltage V_{CL} can be calculated using the volt-balance across the magnetising inductors, leading to $V_{CL} = V_i/(1-D)$.

The positive (as well as negative) pulse duration β in $v_A(\theta)$ is also a function of the duty cycle, according to the following relations, that can be easily derived by inspecting the waveform depicted in figure 3.13.

$$\beta = \begin{cases} 2\pi D, & for D \le 0.5\\ 2\pi (1-D), & for D > 0.5 \end{cases}$$
(3.50)

Since both the voltages $v_A(\theta)$ and $v_B(\theta)$ are known, the energy transfer inductor current i_L can be determined by integrating $v_A(\theta) - v_B(\theta)$ as shown in figure 3.13. The steady state analysis is divided in two operating modes: CCM and DCM.

CCM operation 3.5.1

The current through the energy transfer inductor, which determines the amount of power transferred to the load, can be determined by exploiting the half-wave symmetry of the waveform, i.e. by imposing the condition $J_3 = -J_0$. A complete period of the current is shown in figure 3.13(a) and 3.13(b).

-Phase shift angle (φ) :

As shown in figure 3.13 (a) and (b), there is a phase shift angle between voltages $v_{A(\theta)}$ and $v_{B(\theta)}$. This can be calculated based on the constraint that the average voltage across inductor V_L must be zero. Hence, applying the volt-second balance to the energy transfer inductance L during half-wave symmetry interval ($0 \le \theta \le \pi$), we obtain:

$$(-V_A - V_B)\left(\frac{\varphi}{\omega}\right) + (V_A - V_B)\left(\frac{\beta - \varphi}{\omega}\right) - (V_B)\left(\frac{\pi - \beta}{\omega}\right) = 0$$

Re-arranging the equation above, the phase shift angle is equal to:

$$\varphi = \frac{\pi}{2} \left(\frac{\beta}{\pi} - \frac{1}{U_A} \right) \tag{3.51}$$

where U_A is the normalised voltage of V_A .

Substituting β and U_A from equation 3.50 and 3.49 respectively, we obtain:

$$\varphi = \begin{cases} \frac{\pi}{2} \left(2D - \frac{1-D}{k} \right), & for D \le 0.5 \\ \\ \frac{\pi}{2} (1-D) \left(2 - \frac{1}{k} \right), & for D > 0.5 \end{cases}$$
(3.52)

where k has been defined as $k = (U_i/n)$ and U_i is the normalised voltage of V_i .

-Initial current value (J_0) :

This refers to the energy transfer inductor current of the simplified circuit (figure 3.12 (b)) at the start of the cycle as shown in figure 3.13. By imposing the condition $J_3 = -J_0$ and the inductor voltage is proportional to the rate of change of current flowing through the inductor (A detailed derivation can be found in Appendix A):

$$2I_{L0} + \frac{2V_B \cdot \theta_1}{2\pi f_{sw}L} + \frac{V_A \cdot \theta_2}{2\pi f_{sw}L} - \frac{V_B \cdot \theta_3}{2\pi f_{sw}L} = 0$$
(3.53)

Thus, the initial current J_0 is

$$J_0 = \frac{\pi}{2} (1 + U_A) \left(\frac{1}{U_A} - \frac{\beta}{\pi} \right)$$
(3.54)

Substituting β and U_A from equation 3.50 and 3.49 respectively, we obtain:

$$J_{0} = \begin{cases} \frac{\pi}{2} \left(1 + \frac{k}{1 - D}\right) \left(\frac{1 - D}{k} - 2D\right), & for D \le 0.5 \\ \\ \frac{\pi}{2} \left(\frac{1}{k} - 2\right) \left(1 + k - D\right), & for D > 0.5 \end{cases}$$
(3.55)

-Peak current value (J_2) :

The peak energy transfer inductor current can be calculated the same way as initial current:

$$(U_A - 1) = \frac{J_2 - \theta}{\beta - \varphi}, \qquad \qquad for \ \varphi \le \theta \le \beta$$

Thus, the peak current J_2 is

$$J_{2} = \frac{\pi}{2}(U_{A} - 1)\left(\frac{1}{U_{A}} + \frac{\beta}{\pi}\right)$$
(3.56)

Substituting β and U_A from equation 3.50 and 3.49 respectively, we obtain:

$$J_{2} = \begin{cases} \frac{\pi}{2} (\frac{k}{1-D} - 1) \left(\frac{1-D}{k} + 2D \right), & for D \le 0.5 \\ \\ \frac{\pi}{2} \left(\frac{1}{k} + 2 \right) (-1 + k + D), & for D > 0.5 \end{cases}$$
(3.57)

-Normalised power (Π):

The normalised power transferred from source to load can be calculated by the product of the output rectifier voltage $v_B(\theta)$ and the energy transfer inductor current $i_L(\theta)$ during one switching cycle.

$$\Pi_{CCM} = v_B(\theta) \cdot i_L(\theta) = \frac{1}{\pi} \int_0^{\pi} \left| j_L(\theta) \right| d\theta$$
$$= U_A \frac{\pi}{4} \left[\frac{\beta}{\pi} \left(2 - \frac{\beta}{\pi} \right) - \frac{1}{U_A^2} \right]$$
(3.58)

Substituting β and U_A from equation 3.50 and 3.49 respectively, we obtain:

$$\Pi_{CCM} = \pi k \left(D - \frac{1-D}{4k^2} \right)$$
(3.59)

This normalised power equation during CCM operation holds for any duty cycle D. The maximum power transfer can be found when the pulse duration is maximum. i.e. for $\beta = \pi$ and is equal to:

$$\Pi_{max} = \frac{\pi}{4} \left(U_A - \frac{1}{U_A} \right) \tag{3.60}$$

Note that power is actually transferred only if the condition $U_A > 1$ is met, which means k > (1-D). In addition, discontinuous current mode operation is entered anytime

the phase shift angle φ becomes zero. Using equation 3.51, the CCM/DCM boundary condition is given in normalised terms by:

$$U_{Alim} = \frac{\pi}{\beta} \tag{3.61}$$

Substituting β and U_A from equation 3.50 and 3.49 respectively, we obtain:

$$k_{lim} = \begin{cases} \frac{1-D}{2D}, & for D \le 0.5 \\ \\ \frac{1}{2}, & for D > 0.5 \end{cases}$$
(3.62)

3.5.2 DCM operation

When the converter operates in DCM, the main waveforms are shown in figure 3.13(c) and figure 3.13(d). In this case, there are only two parameters needed to define the energy transfer inductor current waveform: peak value J_1 and dead angle α .

-Peak current value (J_1) :

The peak energy transfer inductor current J_1 similarly to the CCM case:

$$V_L = L \frac{di}{dt}$$

$$(U_A - 1) = \frac{J_1}{\beta} \quad , \qquad \qquad for \ 0 \le \theta \le \beta$$

Thus, peak current J_1 is

$$J_1 = (U_A - 1)\beta \tag{3.63}$$

Substituting β and U_A from equation 3.50 and 3.49 respectively, we obtain:

$$J_{1} = \begin{cases} 2\pi D\left(\frac{k}{1-D} - 1\right), & for D \leq 0.5\\ \\ 2\pi (1-D)\left(\frac{k}{1-D} - 1\right), & for D > 0.5 \end{cases}$$
(3.64)

-Dead angle (α):

The dead angle is a duration time where the energy transfer inductor current i_L and the rectifier output v_B remain zero during the DCM operation. This also causes the rectifier output to become a three level equivalent voltage source unlike CCM operation where the rectifier output is a square wave.

$$\alpha = \pi - U_A \beta \tag{3.65}$$

Substituting β and U_A from equation 3.50 and 3.49 respectively, we obtain:

$$\alpha = \begin{cases} \pi \left(1 - \frac{2kD}{1 - D} \right), & for D \le 0.5 \\ \\ \pi \left(1 - 2k \right), & for D > 0.5 \end{cases}$$
(3.66)

Normalised power:

The normalised power transferred from the source to load during DCM operation can be calculated the same way as in CCM:

$$\Pi_{DCM} = v_B(\theta) \cdot i_L(\theta) = \frac{1}{\pi} \int_0^{\pi-\alpha} \left| j_L(\theta) \right| d\theta$$
$$= \frac{1}{2\pi} U_A(U_A - 1)\beta^2$$
(3.67)

In this case, the normalised power equation needs to consider the two cases of D \leq 0.5 and D>0.5. Using the appropriate expression for β we obtain:

$$\Pi_{DCM} = \begin{cases} 2\pi \frac{D^2 k}{1 - D} \left(\frac{k}{1 - D} - 1 \right), & for D \le 0.5 \\ \\ 2\pi k \left(k - 1 + D \right), & for D > 0.5 \end{cases}$$
(3.68)

The normalised power at the DCM/CCM boundary is found using equation 3.62 and 3.68, which gives:

$$\Pi_{lim} = \frac{\pi}{2} \left| 2D - 1 \right| \tag{3.69}$$

3.5.3 Voltage conversion ratio

The voltage conversion ratio M of the interleaved boost converter with coupled inductors can be derived by recalling $\mathbf{k} = (U_i/\mathbf{n})$ which is the normalised voltage of the input voltage divided by winding turns ratio.

$$M = \frac{V_o}{V_i} = \frac{U_o}{U_i} = \frac{2}{kn} = \frac{2M'}{n}$$
(3.70)

where $M' = \frac{1}{k}$ and the parameter $\in \{0.5, 1\}$. Considering the case of a resistive load, the normalised power can be expressed as a function of the normalised load resistance $\rho_o = R_o/X_L$.

$$\Pi = \frac{V_o^2 X_L}{R_o V_B^2} = \frac{4}{\rho_o}$$
(3.71)

Using normalised power transferred to the load for CCM, DCM and normalised power as a function of the load resistance, equation 3.59, equation 3.68 and equation 3.71, respectively. The voltage gain in CCM and DCM operation can be found as (a detailed derivation can be found in Appendix B):

-CCM operation:

$$M'_{CCM} = \frac{8}{\pi \rho_o (1-D)} \left(-1 + \sqrt{1 + \frac{D(1-D)\pi^2 \rho_o^2}{16}} \right)$$
(3.72)

-DCM operation for $D \le 0.5$:

$$M'_{DCM,D\leq 0.5} = \frac{\pi\rho_o D^2}{4(1-D)} \left(-1 + \sqrt{1 + \frac{8}{\pi\rho_o D^2}}\right)$$
(3.73)

-DCM operation for D>0.5:

$$M'_{DCM,D>0.5} = 4\pi\rho_o(1-D)\left(-1 + \sqrt{1 + \frac{8}{\pi\rho_o(1-D)^2}}\right)$$
(3.74)

In addition, the normalised load resistance at the DCM/CCM boundary can be derived by using the normalised power at the DCM/CCM boundary (equation 3.69) and the normalised power as a function of the load resistance (equation 3.71).

$$\rho_{olim} = \frac{8}{\pi |2D - 1|} \tag{3.75}$$

A plot of the voltage gain M' as a function of the converter duty cycle at different values of the normalised load resistance is shown in figure 3.14. The DCM/CCM boundary line as defined by equation 3.62, is also shown. In addition it is worth noting that there is a no operation region which is defined by the condition 3.60. If the voltage U_A is <1, the power transfer becomes negative. Hence, there is no power transfer from source to load.

$$k > 1-D \qquad \Rightarrow \qquad M' < \frac{1}{1-D}$$
 (3.76)



Figure 3.14: voltage gain M' as a function of the duty cycle D for different normalised load resistances.

Note: In this steady state analysis, the magnetising inductance has no effect on the power transfered from source to load. Moreover, the analysis is carried out in the normalised unit system which has advantages of simplying the coupled inductor in the circuit. In this case, the normalised base voltage, current and impedance are selected on the secondary side of the coupled inductor. When this is referred to the primary side, both sides will have the same normalised unit system. Hence, the coupled inductor can be removed from the analysis.

3.6 Conclusions

In this chapter, an interleaved boost converter with coupled inductors (IBCI) was introduced. The IBCI converter features input current controllability, high conversion ratio, low current ripple, and galvanic isolation which makes it suitable for power conditioning for a fuel cell based APU system. The IBCI converter utilises the coupled inductor to achieve high voltage gain. This inductor could cause a problem related to the leakage inductance but however, using an active clamp, the leakage energy is recycled. In addition, the converter does not require a start-up circuit even though the input voltage is very low. Both CCM and DCM operating modes of the converter were discussed, along with the soft-switching conditions. Finally, the detailed steady state analysis for a single phase was presented.

Chapter 4

Proposed converter: Multiphase Interleaved Boost Converter with Coupled Inductors

The IBCI converter discussed so far can be defined as a single phase converter. The same concept can be extended to multiphase such as 2 phase, 3 phase, and N phase versions as shown in figure 4.1 to provide additional benefits over a single phase version such as higher voltage gain, lower input current ripple, smaller coupled inductor size and higher efficiency. Since the specifications of the reference fuel cell are high input current of 600A and low input voltage of 20V while the output is high voltage of 650V, the single phase IBCI converter will require very low coupled inductor winding ratio which results in higher current stress in the devices. As analysed earlier in the converter operation (Section 3.3), the current flowing in the switch during the on-state is the sum of the magnetising current and current at the secondary side of the coupled inductor being reflected back to the primary side. This current is inversely proportional to the coupled inductor turns ratio. To overcome the aforementioned limitations, a multiphase IBCI converter is proposed. The extra phases have advantages and disadvantages as follows:



Figure 4.1: A multiphase interleaved boost converter with coupled inductors circuit diagram.

Advantages:

• **Provides additional gain**, the additional phase can extend the voltage gain. In a multiphase IBCI converter, the power transfer from source to load is the multiplication of the number of phases. As a result, the coupled inductor winding ratio can be bigger.

- Reduces the input current ripple, adding additional phases has the same feature as the interleaving technique. Each extra phase helps to reduce the total input current ripple.
- Reduces the current stress, as mentioned earlier, the current through the input side (coupled inductor, MOSFET and clamp capacitor) can be categorised into two components; magnetising current (i_{Lm}) and secondary current reflected as the primary current i_r . The magnetising current in each channel is reduced by the number of phases $(i_{Lm}=I_i/(2^*N))$ (where N is the number of phase). i.e. for a two phase IBCI converter, if the input current is 10A, the magnetising current in each channel is 10/(4) = 2.5A. The secondary current reflected in the primary side is inversely proportional to the coupled inductor winding ratio. This current is equal to the energy transfer inductance divided by $i_r = i_L/n$. Since, the coupled inductor winding ratio in the multiphase IBCI converter is bigger, the reflected current is reduced. Therefore, both currents are reduced, the total current stress in the coupled inductor, MOSFET and clamp capacitor is lower in the multiphase IBCI.
- Reduces the coupled inductor size, the size of the coupled inductor is reduced. The input current is distributed to each phase of the multiphase IBCI converter so the input current of each coupled inductor is minimised, resulting in the reduction of magnetic flux of the coupled inductor. Thus, a smaller magnetic core can be used. In addition, the coupled inductor size can be further minimised as the coupled inductor winding ratio is larger in a multiphase IBCI converter.
- Increases efficiency, the conduction loss is a function of square of current multiplied by the on-state resistance of the MOSFETs $(I^2R_{ds(on)})$. As mentioned above, the input current is divided by the number of phases so the conduction loss is reduced.

Disadvantages:

- Increases cost and complexity of the converter, the number of components such as inductors, diodes, capacitors and MOSFETs is increased as well as cost and complexity of the converter.
- Unbalance current between each phase, in practice, the magnetising inductance and leakage inductance of each phase is difficult to control during manufacture. The difference in inductances will cause an unbalanced current between each phase. This could cause problems such as over-current and exceed the component ratings.

4.1 Steady State Analysis of the Multiphase IBCI

The analysis of the multiphase IBCI converter is similar to the single phase one, the total energy flowing to the load is the sum of the contributions of each phase. By using the steady state analysis of the single phase IBCI converter, a new voltage gain for a multiphase IBCI converter can be derived.

For example, a 2 phase interleaved boost converter with coupled inductors.

Referring to the equations from the previous chapter, the normalised power transferred from source to load is shown in equation 3.71. It is easy to demonstrate that the normalised power transferred to the load in a 2 phase converter is twice the power transferred in a single phase one. This remains true for the N phase interleaved boost converter with coupled inductors where the normalised power transferred to the load is N times the value of the single phase one.

CCM operation

The normalised power transferred from source to load for CCM operation is given below, which is twice the power transferred for a single phase IBCI converter.

$$\Pi_{CCM} = 2\pi k \left(D - \frac{1-D}{4k^2} \right) \tag{4.1}$$

Considering the case of a resistive load, the normalised power can be expressed as a function of the normalised load resistance $\rho_o = R_o/X_L$.

$$\Pi_{CCM} = \frac{V_o^2 X_L}{R_o V_B^2} = \frac{4}{\rho_o}$$
(4.2)

Since, both equation 4.1 and equation 4.2 are the normalised power transferred from source to load, the normalised voltage gain for CCM operation can be found as,

$$\frac{4}{\rho_o} = 2\pi k \left(D - \frac{(1-D)}{4k^2} \right)$$
$$4k^2 \pi D \rho_o - (1-D)\pi \rho_o - 8k = 0$$

Divided k^2 ,

$$4\pi D\rho_o - (1 - D)\pi \rho_o \frac{1}{k^2} - \frac{8}{k} = 0$$

Since, M' is equal to (1/k),

$$M'^{2}(1 - D)\pi\rho_{o} + 8M' - 4\pi D\rho_{o} = 0$$

Solving the quadratic equation, the voltage gain can be found as,

$$M'_{CCM} = \frac{2}{\pi \rho_o (1-D)} \left(-2 + \sqrt{4 + D(1-D)\pi^2 \rho_o^2} \right)$$
(4.3)

DCM operation

The normalised power transferred from the source to load during DCM operation can be calculated the same way as in CCM:

$$\Pi_{DCM} = v_B(\theta) \cdot i_L(\theta) = \frac{1}{\pi} \int_0^{\pi-\alpha} \left| j_L(\theta) \right| d\theta$$
$$= \frac{1}{\pi} U_A(U_A - 1)\beta^2$$
(4.4)

In this case, the normalised power equation needs to consider the two cases of $D \le 0.5$ and D>0.5. Using the appropriate expression for β (equation 3.50) we obtain:

$$\Pi_{DCM} = \begin{cases} 4\pi \frac{D^2 k}{1 - D} \left(\frac{k}{1 - D} - 1 \right), & for D \le 0.5 \\ \\ 4\pi k \left(k - 1 + D \right), & for D > 0.5 \end{cases}$$
(4.5)

Therefore, using the above equation 4.2 and equation 4.5 the voltage gain of 2 phase IBCI converter can be divided into two cases; duty cycle $D \leq 0.5$ and D > 0.5.

When $D \leq 0.5$, the normalised power transferred from source to load during this region is equal to, 2.2 0

$$\Pi_{DCM,D\leq 0.5} = \frac{4\pi D^2 k^2}{(1-D)^2} - \frac{4\pi D^2 k}{(1-D)}$$
(4.6)

0

The normalised voltage gain for DCM operation when $D \leq 0.5$ can be found as,

$$\frac{4}{\rho_o} = \frac{4\pi D^2 k^2}{(1-D)^2} - \frac{4\pi D^2 k}{(1-D)}$$
$$\pi D^2 k^2 \rho_o - \pi D^2 (1-D) k \rho_o - (1-D)^2 = 0$$

Divided by k^2 ,

$$\frac{1}{k^2}(1 - D)^2 + \frac{1}{k}\pi D^2(1 - D)\rho_o - \pi D^2\rho_o = 0$$

Since, M' is equal to (1/k),

$$M'^{2}(1 - D)^{2} + M'\pi D^{2}(1 - D)\rho_{o} - \pi D^{2}\rho_{o} = 0$$

Solving the quadratic equation, the voltage gain can be found as,

$$M'_{DCM,D\leq 0.5} = \frac{\pi D^2 \rho_o}{2(1-D)} \left(-1 + \sqrt{1 + \frac{4}{\pi D^2 \rho_o}} \right)$$
(4.7)

When D > 0.5, the normalised power transferred from source to load during this region is equal to,

$$\Pi_{DCM,D>0.5} = 4\pi k^2 - 4\pi k(1 - D) \tag{4.8}$$

The normalised voltage gain for DCM operation when D > 0.5 can be found as,

$$\frac{4}{\rho_o} = 4\pi k^2 - 4\pi k(1 - D)$$
$$\pi k^2 \rho_o + \pi k(1 - D)\rho_o + 1 = 0$$

Divided by k^2 ,

$$\pi \rho_o + \pi \frac{1}{k} (1 - D) \rho_o + \frac{1}{k^2} = 0$$

Since, M' is equal to (1/k),

$$M'^{2} + M'\pi(1 - D)\rho_{o} - \pi\rho_{o} = 0$$

Solving quadratic equation, the voltage gain can be found as,

$$M'_{DCM,D>0.5} = \frac{\pi(1-D)\rho_o}{2} \left(-1 + \sqrt{1 + \frac{4}{\pi\rho_o(1-D)^2}}\right)$$
(4.9)

Summary:

The voltage gain for 2 phase IBCI converter in both CCM and DCM operations can be summarised by the following equations. In addition, an N phase IBCI converter can be found by using the same derivation as 2 phase IBCI converter since the total energy flowing to the load is the sum of the contributions of each phase.

2 phase IBCI converter voltage gain:

$$M' = \begin{cases} = \frac{2}{\pi \rho_o (1-D)} \left(-2 + \sqrt{4 + D(1-D)\pi^2 \rho_o^2} \right), & \text{for CCM operation} \\ = \frac{\pi D^2 \rho_o}{2(1-D)} \left(-1 + \sqrt{1 + \frac{4}{\pi D^2 \rho_o}} \right), & \text{for DCM operation} D \le 0.5 \\ = \frac{\pi (1-D)\rho_o}{2} \left(-1 + \sqrt{1 + \frac{4}{\pi \rho_o (1-D)^2}} \right), & \text{for DCM operation} D > 0.5 \\ \end{cases}$$
(4.10)

N phase IBCI converter voltage gain:

$$M' = \begin{cases} = \frac{2}{N\pi\rho_o(1-D)} \left(-4 + \sqrt{16 + D(1-D)N^2\pi^2\rho_o^2} \right), & \text{for } CCM \text{ operation} \\ = \frac{N\pi D^2\rho_o}{4(1-D)} \left(-1 + \sqrt{1 + \frac{8}{N\pi D^2\rho_o}} \right), & \text{for } DCM \text{ operation} D \le 0.5 \\ = \frac{N\pi(1-D)\rho_o}{4} \left(-1 + \sqrt{1 + \frac{8}{N\pi\rho_o(1-D)^2}} \right), & \text{for } DCM \text{ operation} D > 0.5 \end{cases}$$

$$(4.11)$$

	Single Phase	2 Phase	N Phase
Π_{CCM}	$\pi k \left(D - \frac{1-D}{4k^2} \right)$	$2\pi \mathbf{k} \left(D - \frac{1-D}{4k^2} \right)$	$N\pi k\left(D-rac{1-D}{4k^2} ight)$
$\Pi_{DCM,D \leq 0.5}$	$2\pi \frac{D^2 k}{1-D} \left(\frac{k}{1-D} - 1\right)$	$4\pi \frac{D^2k}{1-D} \left(\frac{k}{1-D} - 1\right)$	$2N\pi \frac{D^2k}{1-D} \left(\frac{k}{1-D} - 1\right)$
$\Pi_{DCM,D>0.5}$	$2\pi k(k-1+D)$	$4\pi k(k-1+D)$	$2N\pi k(k-1+D)$
M_{CCM}^{\prime}	$rac{8}{\pi ho_o(1-D)}$.	$rac{2}{\pi ho_o(1-D)}$.	$rac{2}{N\pi ho_o(1-D)}$.
	$\left(-1 + \sqrt{1 + \frac{D(1-D)\pi^2 \rho_o^2}{16}}\right)$	$\left(-2+\sqrt{4+D(1-D)\pi^2\rho_o^2}\right)$	$\left(-4 + \sqrt{16 + D(1-D)N^2\pi^2\rho_o^2}\right)$
$M'_{DCM,D\leq 0.5}$	$\frac{\pi\rho_o D^2}{4(1-D)} \left(-1 + \sqrt{1 + \frac{8}{\pi\rho_o D^2}} \right)$	$\frac{\pi D^2 \rho_o}{2(1-D)} \left(-1 + \sqrt{1 + \frac{4}{\pi D^2 \rho_o}} \right)$	$\frac{N\pi D^2 \rho_o}{4(1-D)} \left(-1 + \sqrt{1 + \frac{8}{N\pi D^2 \rho_o}}\right)$
$M'_{DCM,D>0.5}$	$4\pi ho_o(1-{ m D})$.	$rac{\pi(1-D) ho_o}{2}$.	$rac{N\pi(1-D) ho_o}{4}$.
	$\left(-1+\sqrt{1+\frac{8}{\pi\rho_o(1-D)^2}}\right)$	$\left(-1+\sqrt{1+\frac{4}{\pi\rho_o(1-D)^2}}\right)$	$\left(-1+\sqrt{1+\frac{8}{N\pi\rho_o(1-D)^2}}\right)$

Table 4.1: Summary of the normalised power transferred from source to load and voltage gain at different operating points for single phase, 2 phase and N phase IBCI converter

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4.2 Dynamic Modelling of the Converter

Power converters are typically highly non-linear systems. Converters normally require a control circuit to regulate the DC output voltage against the variation in the load and input voltage, and also to account for component aging and variations with temperature. Several control theories can be applied to study the behaviour of dynamic systems. One of the most common approaches used in power converter systems is linear control theory. The reason for that is the simplicity of the theory and the varied choice of control design tools (Nyquist, Bode, Root Locus etc.). However, in order to apply this theory, non-linear power converter models need to be averaged and linearised. The final result is a linear circuit or model that is relatively simple and provides good intuitive insight into the dynamic behaviour of the converter. In addition, it can be used to derive the various transfer functions representing the relations between inputs, outputs, and state variables. A dynamic model of the single phase IBCI converter [9] will be shown first, then an extended version of the multiphase IBCI converter will be derived.

4.2.1 Non-linear averaged model

In deriving dynamic models of power converters, the average values of switching voltages and currents are sufficient to evaluate the dynamic behaviour of the converter up to a fraction of the switching frequency. The most popular averaging methods for power converters are: state space averaging method and circuit averaging method. The state space averaging method uses state variables to describe the equivalent linear circuits by differential equations. Different states of transistors and diodes on-off are determined and combined into the state space model. Differently, the circuit averaging method is a circuit based approach based on averaging the instantaneous values into average values and re-arranging the original circuit into a new circuit. The two methods lead to similar results, and the choice of one or the other is normally dependent on the specific converter and on the complexity of the resulting model. In

this thesis, the circuit averaging technique has been selected as a method of analysis.

4.2.1.1 Single phase IBCI converter

By applying the time averaging technique, the non-linear averaged model of the proposed converter is shown in figure 4.2. This model is valid for both CCM and DCM operations.

To derive the non-linear averaged model, several assumptions have been made:

- The energy transfer inductance L is negligible. Although it determines the power transfer between $v_A(\theta)$ and $v_B(\theta)$, it is likely to have little effect on the converter dynamic behaviour, at least at low frequency, because the energy stored in L is much lower than the magnetising inductance L_m energy. In addition, the reactance of an inductor is directly proportional to the frequency $X_L = (\omega L)$. It has a large value when frequency is high whereas at low frequency or close to zero (DC), the inductor reactance is close to zero and can be approximated as a short circuit.
- Clamp capacitors C_{CL} and output capacitors C_1 and C_2 dominate the low frequency converter dynamic behaviour. As capacitors have impedance that is inversely proportional to frequency $X_c=1/(\omega C)$, their effect dominates at low frequency.
- The interleaved operation of the two boost phases is neglected at low frequency. It might have measurable effects on the high frequency region of the converter dynamic response, but those are not taken into account in this analysis.



Figure 4.2: Non-linear averaged model of the single phase IBCI converter.

At the input side, the voltage source \overline{v}_i is connected to the input current source \overline{i}_i . However, the input current generator is multiplied by a factor 2, to account for the fact that a single phase of the converter has two half sections in interleaved operation. From an average perspective, the two interleaved sections operate in parallel. For the same reason, only one clamp capacitor is shown, corresponding to half of the converter, since the dynamics of the clamp capacitor of the other section are the same. As a result, the input stage model is a combination of a boost converter with the addition of a current generator \overline{i}_r that accounts for the energy transfer inductor current \overline{i}_L that is reflected on the primary side of the coupled inductor during the on phase of the auxiliary switch S_3 . This current must be analysed considering two different cases, CCM and DCM.

-CCM operation:



Figure 4.3: Energy transfer inductor waveforms. (a) CCM operation with D >0.5. (b) CCM operation with D <0.5.

According to figure 4.3 (a) and (b), the switch on-time interval of the auxiliary switch S_4 is $[0,\theta_2]$ and $[0,\pi] \cup [\theta_4,2\pi]$, respectively. However, in the latter case, the inductor current waveform i_L during the interval $[\theta_2,\pi]$ is equal to $[\theta_4,2\pi]$ but in the opposite direction. Hence, it cancels and only interval $[0,\theta_2]$ needs to be considered for both cases. The average energy transfer inductor current i_L reflected on the primary side of the coupled inductor can be calculated based on equation 3.55 and equation 3.57.

$$\bar{i}_{r}^{CCM} = \frac{I_N}{n} \frac{1}{2\pi} \int_0^{\theta_2} j_L(\theta) d\theta$$
$$= \frac{I_N \pi}{8n} \left(2\frac{\beta}{\pi} - \frac{\beta^2}{\pi^2} - \frac{1}{\overline{U}_A^2} \right)$$
(4.12)

Substituting β and U_A from equation 3.50 and 3.49 respectively, we obtain:

$$\bar{i}_r^{CCM} = \frac{\pi}{4nX_L} \bar{v}_o \left[D(1-D) - \left(\frac{n\bar{v}_o}{4\bar{v}_{CL}}\right)^2 \right]$$
(4.13)

-DCM operation:



Figure 4.4: Energy transfer inductor waveforms. (a) DCM operation with D >0.5. (b) DCM operation with D <0.5.

Considering figure 4.4 (a) and (b), the switch on-time interval of the auxiliary switch S_4 is $[0,\theta_1]$ and $[0,\pi] \cup [\theta_3,2\pi]$, respectively. However, in the latter case, the inductor current waveform i_L during the interval $[\theta_1,\pi]$ is equal to $[\theta_3,2\pi]$ but in the opposite direction. Thus, it cancels and only interval $[0,\theta_1]$ needs to be considered. The average energy transfer inductor current i_L reflected on the primary side of the coupled inductor can be calculated based on equation 3.64.

$$\bar{i}_r^{DCM} = \frac{I_N}{n} \frac{1}{2\pi} \int_0^{\theta_1} j_L(\theta) d\theta$$
$$\bar{i}_r^{DCM} = \frac{I_N}{4n\pi} \left(\overline{U}_A - 1 \right) \beta^2$$
(4.14)

Substituting β and U_A from equation 3.50 and 3.49 respectively, we obtain:

$$= \begin{cases} \frac{1}{2nX_L} \left(\frac{\overline{v}_{CL}}{n} - \frac{\overline{v}_o}{2}\right) D, & for D \le 0.5 \\ \\ \frac{1}{2nX_L} \left(\frac{\overline{v}_{CL}}{n} - \frac{\overline{v}_o}{2}\right) (1 - D), & for D > 0.5 \end{cases}$$

$$(4.15)$$

Comparing equation 4.12 and equation 4.14 with the normalised power expressions equation 3.59 and equation 3.68, valid in steady state, the average energy transfer inductor current i_L reflected on the primary side of the coupled inductor can be expressed as:

$$\overline{i}_r = \frac{I_N \Pi}{2n \overline{U}_A} = \frac{\overline{p}_o}{2\overline{v}_i} (1 - D) = \overline{i}_m (1 - D)$$
(4.16)

This matches with the model in figure 4.2. The average clamp capacitor current is zero in steady state. At the output rectifier side, the current generator \bar{i}_f represents the energy transfer from the source to the load. This current can be calculated considering that, in steady state, it is equal to the load current \bar{i}_o .

$$\bar{i}_f = \bar{i}_o = \Pi \frac{P_N}{\bar{v}_o} = \frac{\Pi I_N}{2} \tag{4.17}$$

The relationship between i_r and i_f can be derived by using equation 4.16 and equation 4.17:

$$\bar{i}_f = 2 \frac{\bar{v}_{CL}}{\bar{v}_o} \ \bar{i}_r = 2 \frac{\bar{v}_{CL}}{\bar{v}_o} f(\bar{v}_o, \ \bar{v}_{CL}, \ D) = g(\bar{v}_o, \ \bar{v}_{CL}, \ D)$$
(4.18)

This concludes the first stage of the dynamic modelling. The averaged equivalent circuit will now be linearised to complete the analysis.

4.2.1.2 Multiphase IBCI converter

The non-linear averaged model of the multiphase IBCI converter is shown in figure 4.5. The differences between the single phase version and the multiphase version are the magnetising current at input side and the energy transfer current i_f at the output side. The input current is now divided into N phases so the magnetising current is equal to $(i_m = i_i/2N)$. The energy transfer current is now proportional to the number of phases N.



Figure 4.5: Non-linear averaged model of the proposed converter.

In the multiphase IBCI converter, the power transfer from source to load is the multiplication of the number of phases (N). Therefore, the normalised power transfer to load for a multiphase IBCI converter can be derived from the single phase IBCI equation 3.59 and equation 3.68 and expressed as:

$$\Pi = \begin{cases} U_A \frac{\pi N}{4} \left[\frac{\beta}{\pi} \left(2 - \frac{\beta}{\pi} \right) - \frac{1}{U_A^2} \right], & \text{for CCM operation} \\ \\ U_A \frac{\pi N}{4} \left[\frac{\beta}{\pi} \left(2 - \frac{\beta}{\pi} \right) - \frac{1}{U_A^2} \right], & \text{for DCM operation} \end{cases}$$
(4.19)

Comparing equation 4.12 and equation 4.14 with the normalised power expressions equation 4.19, valid in steady state, the average energy transfer inductor current i_L reflected on the primary side of the coupled inductor can be expressed as:

$$\bar{i}_r = \frac{I_N \Pi}{2nN\overline{U}_A} = \frac{\overline{p}_o}{2N\overline{v}_i}(1 - D) = \frac{\overline{i}_m(1 - D)}{N}$$
(4.20)

The output current in a multiphase IBCI converter is equal to the sum of the number of energy transfer currents from source to load. Thus, at steady state the current generator $\overline{i_f}$ that represents this current can be given by:

$$\bar{i}_f = \frac{\bar{i}_o}{N} = \Pi \frac{P_N}{N\bar{v}_o} = \frac{\Pi I_N}{2N}$$
(4.21)

Comparing equation 4.20 and equation 4.22, the relation between two currents i_f and i_r can be derived:

$$\bar{i}_f = 2 \frac{\bar{v}_{CL}}{\bar{v}_o} \ \bar{i}_r = 2 \frac{\bar{v}_{CL}}{\bar{v}_o} f(\bar{v}_o, \bar{v}_{CL}, D) = g(\bar{v}_o, \bar{v}_{CL}, D)$$
(4.22)

Note: It can be noticed that the relationship between these two currents is the same whether in single phase IBCI converter or multiphase IBCI converter.

4.2.2 Linearised small signal model

In this section, the averaged small signal linear time-invariant model of the converter is developed for both CCM and DCM operation. In the previous section, the ideal switching network of the converter in steady state has been modelled into an averaged switch circuit, representing the converter only with passive components and ideal dependent current and voltage sources. The currents, voltages, and duty cycle are now perturbed about the DC operating point. As a consequence, the DC dependent sources in the model are replaced by large signal time-varying dependent sources which contain both a DC and a small AC component. If the magnitudes of the small-signal components are small enough, the model can be linearised by neglecting the terms containing products of AC components, finally leading to a linear model. This circuit model contains both the small signal AC model and the steady state DC model. Hence, normal circuit techniques such as the superposition principle and Kirchhoff's laws can be used to calculate the small signal transfer functions of the converter.

4.2.2.1 Single phase IBCI converter

A linearised small signal model is derived from the non-linear averaged model in figure 4.2 by considering small perturbations about the operating point and neglecting the products of perturbation signals. It is usually denoted the small perturbation as a litter with a $\hat{}$ caret (or a hat) on top of it. The final linearised small signal model is shown in figure 4.6 and is valid for both CCM and DCM. However, the parameters g_r , g_f , h_r , h_f , r_c , and r_o depend on the operating mode (CCM or DCM).



Figure 4.6: Linearised small signal model of the single phase IBCI converter.

The analysis is divided into two operating modes: CCM and DCM.

CCM:

In the linearised small signal model, the small perturbation, around a given operating point, of the energy transfer inductor current reflected on the primary side of the coupled inductor i_r in CCM can be written as (neglecting the products of perturbation signals):

$$\hat{i}_{r}^{CCM} = \frac{\partial f}{\partial \overline{v}_{o}} \bigg|_{OP} \left. \hat{v}_{o} + \frac{\partial f}{\partial \overline{v}_{CL}} \right|_{OP} \left. \hat{v}_{CL} + \frac{\partial f}{\partial D} \right|_{OP} \left. \hat{d} \right.$$

Substituting the function f with equation 4.13, we obtain:

$$= \left(\frac{\pi d(1-D)}{4nX_L} - \frac{3n\pi \overline{v}_o^2}{64X_L \overline{v}_{CL}^2}\right) \hat{v}_o + \frac{n\pi \overline{v}_o^3}{32X_L \overline{v}_{CL}^3} \hat{v}_{CL} + \frac{\pi (1-2D)\overline{v}_o}{4nX_L} \hat{d} \qquad (4.23)$$

$$= g_r \hat{v}_o + \frac{1}{r_c} \hat{v}_{CL} + h_r \hat{d}$$
(4.24)

On the rectifier side, the current generator i_f that represents the energy transfer towards the load can be written as:

$$\hat{i}_{f}^{CCM} = \frac{\partial g}{\partial \overline{v}_{o}} \bigg|_{OP} \left. \hat{v}_{o} + \frac{\partial g}{\partial \overline{v}_{CL}} \right|_{OP} \left. \hat{v}_{CL} + \frac{\partial g}{\partial D} \right|_{OP} \left. \hat{d} \right.$$

Substituting the function g with equation 4.18, we obtain:

$$= -\frac{n\pi\bar{v}_o}{16X_L\bar{v}_{CL}} \hat{v}_o + \left(\frac{\pi D(1-D)}{2nX_L} + \frac{n\pi\bar{v}_o^2}{32X_L\bar{v}_{CL}^2}\right) \hat{v}_{CL} + \frac{\pi(1-2D)\bar{v}_{CL}}{2nX_L} \hat{d} \quad (4.25)$$
$$= -\frac{1}{r_o}\hat{v}_o + g_f\hat{v}_{CL} + h_f\hat{d} \quad (4.26)$$

DCM:

In the linearised small signal model, the small perturbation, around a given operating point, of the energy transfer inductor current reflected on the primary side of the coupled inductor i_r in DCM can be written as (neglecting the products of perturbation signals):

$$\hat{i}_{r}^{DCM} = \frac{\partial f}{\partial \overline{v}_{o}} \bigg|_{OP} \hat{v}_{o} + \frac{\partial f}{\partial \overline{v}_{CL}} \bigg|_{OP} \hat{v}_{CL} + \frac{\partial f}{\partial D} \bigg|_{OP} \hat{d}$$

Substituting the function f with equation 4.15, we obtain:

$$= \begin{cases} -\frac{D}{4nX_L}\hat{v}_o + \frac{D}{2n^2X_L}\hat{v}_{CL} + \left(\frac{\overline{v}_{CL}}{2n^2X_L} - \frac{\overline{v}_o}{4nX_L}\right)\hat{d}, & \text{for } D \le 0.5 \\ \\ -\frac{(1-D)}{4nX_L}\hat{v}_o + \frac{(1-D)}{2n^2X_L}\hat{v}_{CL} + \left(-\frac{\overline{v}_{CL}}{2n^2X_L} + \frac{\overline{v}_o}{4nX_L}\right)\hat{d}, & \text{for } D > 0.5 \end{cases}$$

$$= g_r\hat{v}_o + \frac{1}{r_c}\hat{v}_{CL} + h_r\hat{d}$$

$$(4.28)$$

On the rectifier side, the current generator i_f that represents the energy transfer toward the load can be described as:

$$\hat{i}_{f}^{DCM} = \frac{\partial g}{\partial \overline{v}_{o}} \bigg|_{OP} \hat{v}_{o} + \frac{\partial g}{\partial \overline{v}_{CL}} \bigg|_{OP} \hat{v}_{CL} + \frac{\partial g}{\partial D} \bigg|_{OP} \hat{d}$$

Substituting the function g with equation 4.18, we obtain:

$$= \begin{cases} -\frac{D\overline{v}_{CL}^{2}}{n^{2}X_{L}\overline{v}_{o}}\hat{v}_{o} + \left(\frac{2D\overline{v}_{CL}}{n^{2}X_{L}\overline{v}_{o}} - \frac{D}{2nX_{L}}\right)\hat{v}_{CL} + \left(\frac{\overline{v}_{CL}^{2}}{n^{2}X_{L}\overline{v}_{o}} - \frac{\overline{v}_{CL}}{2nX_{L}}\right)\hat{d}, & \text{for } D \leq 0.5 \\ -\frac{(1-D)\overline{v}_{CL}^{2}}{n^{2}X_{L}\overline{v}_{o}}\hat{v}_{o} + \left(\frac{2(1-D)\overline{v}_{CL}}{n^{2}X_{L}\overline{v}_{o}} - \frac{(1-D)}{2nX_{L}}\right)\hat{v}_{CL} \\ + \left(-\frac{\overline{v}_{CL}^{2}}{n^{2}X_{L}\overline{v}_{o}} + \frac{\overline{v}_{CL}}{2nX_{L}}\right)\hat{d}, & \text{for } D > 0.5 \end{cases}$$

$$(4.29)$$

$$= -\frac{1}{r_o}\hat{v}_o + g_f\hat{v}_{CL} + h_f\hat{d}$$
(4.30)

All the parameters in the small signal model in figure 4.6 have been derived, and the transfer functions of interest can now be found. For example, the duty cycle to output voltage transfer function $G_{vd}(s)$. This transfer function reflects the effect of duty cycle changes to the output voltage which is essential in voltage mode control and important for describing the voltage loop for current mode control.

$$G_{vd}(s) = \frac{\hat{V}_o(s)}{\hat{D}(s)} = K \frac{1 + a_1 s + a_2 s^2}{1 + b_1 s + b_2 s^2 + b_3 s^3}$$
(4.31)
where the coefficients K, a_1 , a_2 , b_1 , b_2 , and b_3 are $(L_e = L_m/(1 - D)^2$ and $C_o = C_1C_2/(C_1 + C_2))$

$$K = h_f(r_o / / R_o) \left(1 + \frac{V_{CL}g_f}{h_f(1 - D)} \right)$$

$$a_1 = \frac{L_e}{1 + \frac{V_{CL}g_f}{h_f(1 - D)}} \left(\frac{1}{r_C} - \frac{g_f}{h_f} (I_m + h_r) \right)$$

$$a_2 = \frac{L_e C_{CL}}{1 + \frac{V_{CL}g_f}{h_f(1 - D)}}$$

$$b_1 = L_e \left(\frac{1}{r_C} + g_f g_r(r_o / / R_o) \right) + (r_o / / R_o) C_o$$

$$b_2 = L_e \left(C_{CL} + \frac{r_o / / R_o}{r_C} C_o \right)$$

$$b_3 = L_e C_{CL} (r_o / / R_o) C_o$$

To verify the derived small signal model of the single phase IBCI converter, a bode plot of duty cycle to output transfer function is plotted in figure 4.7 and is compared to the frequency response obtained by applying perturbations to a dynamic model in PLECS. The result shows good agreement between the PLECS simulation model and the approximated model. There is a slight difference in terms of phase response which could occur due to the more complicated model in PLECS. The PLECS model includes the ripple in all the passive components and the non-ideal switching behaviour of the active components - which are not included in the approximate model.



Figure 4.7: Bode plot for duty cycle to output voltage transfer function of a single phase IBCI converter at full load condition (switching frequency of 20kHz, coupled inductor winding ratio of 0.33, and energy transfer inductance of 15uH).

4.2.2.2 Multiphase IBCI converter

A linearised small signal model for multiphase IBCI is shown in figure 4.8.



Figure 4.8: Linearised small signal model of the multiphase IBCI converter.

The parameters g_r , g_f , h_r , h_f , r_c , and r_o remain the same as for the single phase IBCI converter. However, this is slightly changed in the linearised small signal model. The magnetising current is lower as it is divided by the number of phases (N) while the current source that represents the energy transfer current is multiplied by a factor N. Thus, the transfer function of interest can now be derived based on figure 4.8. An example of duty cycle to output voltage transfer function $G_{vd}(s)$ is given by,

$$G_{vd}(s) = \frac{\hat{V}_o(s)}{\hat{D}(s)} = K \frac{1 + c_1 s + c_2 s^2}{1 + d_1 s + d_2 s^2 + d_3 s^3}$$
(4.32)

where the coefficients k, c_1, c_2, d_1, d_2 , and d_3 are $(L_e = L_m/(1 - D)^2, C_o = C_1 C_2/(C_1 + C_2)$ and $R_e = (NR_o + r_o)/(r_o R_o))$

$$K = Nh_f R_e \left(1 + \frac{V_{CL}g_f}{Nh_f(1-D)} \right)$$
$$c_1 = \frac{L_e}{1 + \frac{V_{CL}g_f}{Nh_f(1-D)}} \left(\frac{1}{r_C} - \frac{g_f}{h_f}(I_m + h_r) \right)$$
$$c_2 = \frac{L_e C_{CL}}{1 + \frac{V_{CL}g_f}{Nh_f(1-D)}}$$

$$d_1 = NL_e \left(\frac{1}{r_C} + g_f g_r R_e \right) + R_e C_o$$
$$d_2 = NL_e \left(C_{CL} + \frac{R_e C_o}{r_C} \right)$$
$$d_3 = NL_e C_{CL} R_e C_o$$

4.3 Conclusions

The single phase IBCI converter can be extended to a multiphase IBCI converter by using the interleaving technique. Each additional phase is connected in parallel and the gate signal is phase shift by $2\pi/N$. An extended version multiphase IBCI converter, provides additional voltage gain, reduces the input current ripple, reduces the current stress and increases the overall converter efficiency. Finally, the dynamic modelling of the converter using circuit averaging and linearisation techniques was described. This procedure is important as the resulting transfer functions will be required for designing a control circuit to regulate the DC output voltage against variations in the load current and input voltage. However, it should be noted that closed-loop design of the converter has not been implemented and is left for further work. The converter design and component selection will be discussed in the next chapter.

Chapter 5

Converter Design

In this chapter, the design of the multiphase IBCI converter including the selection of the main components and parameters is discussed. This chapter starts with an introduction to the available degrees of freedom as observed from the previous steady state analysis. The proposed converter voltage gain depends on three main variables that affect the converter operation and performance; energy transfer inductance L, turns ratio of the coupled inductors n and switching frequency f_{sw} . The impact of these variables on the converter operation and the complex links between each of the parameters will be discussed. To avoid any unforeseen problems (such as high current and voltage stress on the components), these variables are chosen and optimised to guarantee operability of the converter over the entire fuel cell characteristic from startup load to light load (as discussed in chapter 2). Additionally, the converter efficiency is maximised at the nominal load condition where the converter mostly operates. Moreover, the converter needs to meet the requirements of input current ripple at 4% and output voltage ripple at 4.5% to suit the fuel cell application and satisfy the aircraft electrical power standards. To verify the final design of the multiphase IBCI converter, the PLECS simulation software in conjunction with MATLAB is used.

MATLAB software provides a powerful computing framework for handling calculations. Matlab code can be written to perform specific tasks such as matrix manipulations, creating functions, implementation of algorithms, and plotting data and figures. To guarantee operability of the converter over the entire fuel cell characteristic, MATLAB codes are written to generate the waveforms associated with all the main components and to determine the converter operating points. Moreover, to optimise the converter efficiency, the losses of each component are simulated through a sweep analysis across all operating points. This is to verify the functionality of the proposed design.

PLECS simulation software offers a high-speed simulation of power electronics systems. The proposed converter is modelled using both ideal characteristics and practical characteristics based on the device manufacturer's datasheets. Hence, the detailed analysis of the converter can be accomplished to study the behaviour of each of the components in the converter, while the losses can be accurately predicted. As a result, the converter total predicted efficiency can be determined. In addition, the simulation software is used to analyse the input/output dynamic response of the converter. This can be compared to the small signal analysis model that has been derived in the previous chapter.

Thus, using a combination of MATLAB and PLECS, the final proposed converter design can be verified.

5.1 Available Degrees of Freedom

Before starting the design of the converter, the impact of the available degrees of freedom must be understood so that the converter performance can be optimised; whether in terms of the operating region, passive component stress, zero-voltage switching turn-on boundary or efficiency. After taking these degrees of freedom into consideration, the design will be carried out in order to meet the fuel cell operating constraints while achieving high conversion efficiency at the nominal load.

50 n=1/2=0.5 n=1/3=0.33 45 n=1/4=0.25 n=1/5=0.2 DCM n=1/6=0.167 40 35 **Voltage gain (M) NO OPERATION** 15 DCM 10 CCM 0 0.3 0.1 0.2 0.5 0.6 0.7 0.8 0.9 0.4 1 0 Duty-cycle (D)

5.1.1 Impact of the coupled inductor turns ratio

Figure 5.1: Voltage gain M as a function of the duty cycle for different coupled inductor turns ratio with switching frequency of 20kHz, energy transfer inductance of 70uH and load resistance of 63.5Ω .

Figure 5.1 shows the voltage gain as a function of duty cycle. The coloured lines represent the voltage gain for different values of the coupled inductor turns ratio, from 0.5 to 0.167 (where *n* represents primary turns n_p to secondary turns n_s). As shown in the figure, when decreasing the turns ratio the voltage gain rises and the operating point moves upward toward the DCM region both when the duty cycle is larger and smaller than 0.5. The advantage of operating at lower turns ratio is that the converter operates at lower duty cycle. Thus, the voltage stress of each component is minimised, which means the size of passive components such as the inductor and capacitor can be reduced to save cost. However, operating at low coupled inductor turns ratio significantly increases the conduction losses and reduces the efficiency of the converter due to the current from the secondary side of the coupled inductor that reflects back into the primary. The conduction loss is directly proportional to the square of the RMS current through the power device. This aspect will be explained in more detail later in this chapter. In addition, operating in DCM, the main switch will lose zero-voltage switching turn-on when the duty cycle less than 0.5.

5.1.2 Impact of energy transfer inductance



Figure 5.2: Normalised voltage gain M' as a function of duty cycle for different energy transfer inductance values with switching frequency of 50kHz and load resistance of 63.5Ω .

The energy transfer inductance L can be referred to the leakage inductance of the coupled inductor. From figure 5.2, it can be clearly seen that increasing the energy transfer inductance reduces the normalised voltage gain of the converter and the operating point moves toward the CCM region. In addition, in order to maintain the same voltage gain, the converter needs to operate at higher duty cycle which

will increase losses, voltage and current stress on the components and the size of the coupled inductor. Moreover, with large values of energy transfer inductance the zero-voltage switching of the main switches is more likely to be maintained for a wider range, with the operation mainly in CCM.

5.1.3 Impact of switching frequency



Figure 5.3: Normalised voltage gain M' as a function of duty-cycle for different switching frequencies with energy transfer inductance of 70uH and normalised load resistance of 63.5Ω .

Figure 5.3 shows the normalised voltage gain as a function of duty cycle. The coloured lines represent the normalised voltage gain for different switching frequency values from 10kHz to 50kHz. The figure indicates that increasing the switching frequency can reduce the normalised voltage gain and therefore shift the operating point downward to the CCM region. Furthermore, to stabilise the voltage gain, the operating point

has a higher duty cycle which would increase the switching losses and put additional voltage and current stress on the components. Conduction and switching losses are directly proportional to the duty cycle and switching frequency, respectively. The obvious advantage of increasing switching frequency is to reduce the size of passive components such as the coupled inductor and clamp capacitor. While the values of inductor and capacitor are inversely proportional to switching frequency, given the ripple current and voltage remains the same, the overall size of converter can be smaller. Although increasing the switching frequency would generally increase the switching loss, the operation remains largely in CCM. This is highly desirable in terms of maximising the soft-switching region.

The table below summarises the impact of reducing the coupled inductor turns ratio, energy transfer inductance and switching frequency on the converter characteristics:

Table 5.1: Summary the impact of reducing coupled inductor turns ratio, energy transfer inductance and switching frequency on the operation of the converter

	Turns ratio	Energy transfer	Switching frequency
	(n)	inductance (L)	(f_{sw})
Operating duty cycle	Higher	Higher	Higher
Operating region	toward CCM	toward CCM	toward CCM
Voltage stress	1	1	1
Current stress	1	1	1
Conduction losses	1	1	1
Switching losses	\uparrow	1	1
Efficiency	\downarrow	\downarrow	\downarrow
Size of components	\downarrow	\downarrow	\downarrow
ZVS condition	↑	†	†

where \uparrow indicates "increase" and \downarrow indicates "decrease"

Another factor that greatly affects the converter performance and overall efficiency is the number of phases of the interleaved boost converter with coupled inductors. The number of phases does not only affect the voltage gain of the converter, but also affects the operating points, current ripple cancellation, current stress of the components and the losses.

One of the features of the proposed design is the interleaving technique where the input current ripples of the different phases cancel each other by controlling the gate signal phase shifts to $2\pi/N$ where N is the number of interleaved channels. A single phase interleaved boost converter with a coupled inductor utilises a two channel interleaving technique which means that with a duty cycle of 0.5 the input current ripple can be perfectly cancelled as shown in figure 5.4. The relative current ripple r_i is the magnetising inductor ripple current divided by the average magnetising current, which can be found by:

$$r_i = \frac{\Delta i_{Lm}}{\bar{i}_{Lm}} = \left(1 - \frac{m}{ND}\right) \left(\frac{1 + m - ND}{1 - D}\right)$$
(5.1)

where N is number of interleaved channels, $m = \text{floor}(N^*D)$ is the floored value of N^*D and D is the duty cycle.

Plotting this equation for different numbers of interleaved channels, gives the results shown below.



Figure 5.4: Normalised current ripple amplitude versus duty cycle at different numbers of interleaved channels: (Left) Even number N=2,4,6 and 8. (Right) Odd number N=3,5,7 and 9.

Furthermore, the interleaved structure helps to reduce the conduction loss as the total conduction loss is directly proportional to the square of the RMS current. In the conventional boost converter with an interleaving structure of two parallel channels, the total conduction loss is reduced by a factor of 2. However, it does not provide significant reduction in conduction loss as in the case of the interleaved boost converter. This is due to the fact that IBCI converter inherits the secondary current that is reflected back to the primary side (reverse current) and that current is a function of the turns ratio. In the IBCI converter, there are two currents; magnetising current and reverse current. To see this clearly, both individual currents and the sum of the two currents of a single phase IBCI converter and a two phase IBCI converter are plotted below. The same parameters are applied for both cases.



Figure 5.5: Converter waveforms for single phase IBCI converter at full load operating point. (Top) Magnetising current. (Middle) Reverse current. (Bottom) Total current.

Figure 5.5 shows the peak magnetising current is 302A, reverse current is 655A and sum of the current is 957A (RMS current is 499A). The total current of channel 1 and channel 2 is equal to the input current of 600A. In addition, the secondary current that is reflected to the primary side dominates the magnetising current. If the coupled inductor winding ratio becomes smaller, the reverse current will further dominate the magnetising current. This will be discussed later in this chapter.



Figure 5.6: Converter waveforms for two phase IBCI converter at full load operating point. (Top) Magnetising current. (Middle) Reverse current. (Bottom) Total current. (The current shown in figure is only one phase as another phase is the same).

Figure 5.6 shows the peak magnetising current is 150A, reverse current is 333A and sum of the currents is 483A (RMS current is 251A). Comparing the single phase and two phase IBCI converter, the RMS of the total current in each channel is 499A and 251A, respectively. The conduction loss is a function of $I^2R_{ds(on)}$, so the conduction loss in the multiphase IBCI converter can be reduced by factor of nearly 2 for the same MOSFET device. Therefore, the overall converter efficiency is increased. Moreover, in the multiphase IBCI converter, the current is distributed through a larger number of channels. Hence, the total current flow though the coupled inductor is reduced. As a result, the size of the inductor can be minimised. However, there are the trade-offs to using extra phases due to the increased number of switching devices and inductors. This will increase the cost of converter.

A multiphase IBCI converter is selected as the principal design for this thesis. The design is chosen mainly due to the extra voltage gain, flexibility of the input current control in each channel, and the current ripple cancellation characteristics corresponding to six equivalent interleaved channels. Thus, with six channels, the overall input current ripple can be limited to less than 20% of the original ripple in each of the magnetising inductors over a wide range of duty cycle from 0.15 to 0.85 which will benefit the fuel cell application. Moreover, the maximum output current from the fuel cell is 600A during start-up. With a 1 phase converter, this means that each channel of the converter has a 300A DC current component, not including the current flowing from the secondary side of each coupled inductor that is reflected back to the primary side. This reverse current depends on the coupled inductor turns ratio and energy transfer inductance current which could easily be 1-3 times the DC component in each channel. To handle this high current stress, a large number of MOSFET devices must be connected in parallel to reduce the stress. However, this could cause the effects of threshold voltage and transconductance (gain) mismatch on current and switching energy balance [58]. Hence, to avoid these problems and provide the current control flexibility in each channel, a 3-phase converter is selected. The current distribution in each channel is reduced to 100A plus the current reflected from secondary side which reduces the number of MOSFETs per channel used. Furthermore, the input current ripple cancellation can be achieved over a wide range of duty cycle for this design. Although the number of phases can be higher, especially for a high input current application because it can minimise the size of coupled inductor, current stress and increase efficiency; doing so would increase the cost, add complexity to the control circuitry, and may create additional problems associated with imbalance current between each phase. As stated above, the 3 phase IBCI converter is selected as the principal design to demonstrate the concept of the multiphase IBCI converter. It reduces the magnetising current in each channel to 1/6 of the input current so only two parallel MOSFETs are required. The size of inductor, current stress, converter losses are significantly reduced - thus avoiding higher cost, complex control circuitry and any problems related to the imbalance current.

5.2 Selection of the Converter Parameters

From the discussion in the previous sessions, it can be noted that there are several possible ways to select the value for the three degrees of freedom, depending on the design constraints and requirements. Also, considering the complex links between each of the parameters and the operating conditions of the converter, a direct choice is not recommended. This could create unforeseen problems if these parameters are not carefully chosen, such as increases in current stress, conduction loss, and reduced efficiency.

In this work, the three degrees of freedom are selected to ensure operability of the converter over the entire fuel cell characteristics from start-up to light load while maximising the efficiency at the nominal load condition. This is because the converter only operates at start-up load for a short period of time, and would operate mostly at nominal load condition. When the fuel cell stacks are warmed up, the output voltage from the fuel cell is higher until the converter is operating at nominal load. In order to achieve the design, several MATLAB codes are written to perform the following tasks.

- Plotting all the voltage and current waveforms of the main components (coupled inductor, MOSFETs, clamp capacitor, diode rectifier, output capacitor, and load). The converter parameters can be easily changed to study the impact of these parameters.
- Plotting the converter operating points over all the input voltage range. This simulates the converter operating conditions such as duty cycle, voltage gain, continuous current mode (CCM) or discontinuous current mode (DCM), power and load.
- Calculating average and RMS values of voltage and current for each component. This information is useful in selecting components to meet the component ratings.

- Calculating the losses in the main components based on power loss modelling in each component (which will be explained later in this chapter). This includes core loss and copper loss in the inductor, conduction loss and switching loss in the MOSFETs, conduction loss and reverse recovery loss in the diode, and capacitor power loss. This information is used to optimise the converter parameters to achieve the desired efficiency.
- Sweeping the above analyses over all the input voltage range from the fuel cell. This is to guarantee operability of the converter over the entire fuel cell characteristic and to obtain the data from the analysis across all operating points.
- Using the MATLAB codes to sweep over all the input voltage range with different three degrees of freedom (coupled inductor winding ratio, switching frequency and energy transfer inductance) to determine the best combination of parameters that is able to operate across all the fuel cell characteristic while achieving high efficiency at nominal load.

Following the initial analysis, the other parameters such as magnetising inductance, clamp capacitance and output capacitance are selected to meet the power stress and application requirements of 4% input current ripple and 4.5% output voltage ripple. Finally, the components are selected based on the stress at maximum power plus a safety margin.

All the parameters related to the loss analysis are shown in table 5.2. These are taken from the components manufacturer's datasheet. (The component selection process is discussed in Chapter 6 which includes components for both the full scale example and the small scale lab prototype).

	Parameters	Symbol	Val	ues
MOSFET	On resistance	R_{DS}	19	$m\Omega$
IXFN160N30T	Turn-on time	t_{on}	112	nS
	Turn-off time	t_{off}	113	nS
Diode	Forward voltage drop	V_F	1.75	V
DSEI30A	Peak reverse recovery current	I_{RM}	16	A
	Reverse recovery time	t_{rr}	40	nS
Clamp capcitor	Equivalent series resistance	R_{ESR}	0.1	$m\Omega$
KEMET R75IR4470				
Output capacitor EEUED2G470	Equivalent series resistance	R_{ESR}	0.04	Ω

Table 5.2: Summary of related parameters used in the loss analysis

5.2.1 Wide sweep over the three degrees of freedom

The first step is to sweep over a wide range of the three degrees of freedom (coupled inductor turns ratio, energy transfer inductance and switching frequency).

The summary of the conditions used in the MATLAB analysis is shown below:

- Coupled inductor turns ratio n ranges from 0.5 (1/2) to 0.1 (1/10). The lower bound is 0.5 (1/2) which is the minimum winding ratio to utilise the coupled inductor. As discussed earlier, the smaller the coupled inductor winding ratio is, the lower the efficiency will be. Hence, the upper boundary is set to 0.1 (1/10) to keep the efficiency at reasonable values (above 50 % at full load).
- Switching frequency f_{sw} ranges from 20 to 200 kHz. The minimum frequency is selected from the control design perspective. The switching frequency indicates the crossover frequency of the loop gain and converter response. In the

approximate average model, there is a phase delay which is caused by the PWM process. For this reason, the models derived using the averaging technique can be usually considered valid for $f < f_{sw}/3$ [59]. Hence, to avoid slow response of the converter, a minimum frequency of 20 kHz is chosen for the preliminary design. Although MOSFET devices can operate at higher frequency over 200 kHz, this increases the switching loss significantly. Hence, the maximum frequency at this stage is limited at 200 kHz for preliminary design. If the efficiency is within an acceptable range, further increases in switching frequency could be adjusted later in the final design.

- Energy transfer inductance L ranges from 1 to 50 uH. Energy transfer inductance in the IBCI converter is the source of leakage inductance in the coupled inductor. In practice, there is leakage inductance in the coupled inductor, approximately 1% of the magnetising inductance. As the upper boundary of leakage inductance is chosen at 50 uH, the magnetising inductance would be around 5 mH in order to avoid an oversized coupled inductor. In addition, low magnetising inductance will cause the input current ripple to increase so the minimum magnetising inductance is limited to 0.1 mH. Hence, the energy transfer inductance is chosen at 1 uH to be the lower boundary of the analysis.
- The maximum duty cycle of the converter should not exceed 0.9. This is to ensure that the voltage stress across MOSFET is lower than the voltage rating of the MOSFET device. Operating at higher duty cycle results in high voltage stress on the power devices as the voltage stress is a function of duty cycle $(V_{stress} = \frac{1}{1-D}).$
- Efficiency includes losses in the power devices, capacitors and diodes (excluding the inductor in this analysis because it is impossible to approximate losses for a wide operating range as they depend on many other factors such as maximum flux density, type of core, material, and size of wires, that are not available at an early stage of the design).
- Assuming the magnetising inductance is infinite $(L_m \to \infty)$ so the magnetising inductor ripple current can be neglected $(\Delta i_{Lm} = 0)$.



Figure 5.7: Efficiency versus input voltage for different values of the degrees of freedom.



Figure 5.8: Zoom in plot of the efficiency versus input voltage for different values of the degrees of freedom.

Table 5.3: Converter efficiency over all the input voltages for different values of the degrees of freedom

			Input voltage (V)								
n	f_{sw}		20	30	40	50	60	70	80	90	100
0.50	10000	1.00	94.42	95.74	96.39	96.79	97.05	97.25	98.34	98.57	98.64
0.21	10000	1.00	93.65	94.78	94.30	91.89	86.07	81.99	77.25	79.61	78.56
0.21	10000	13.25	93.63	94.77	94.58	93.22	91.38	90.69	91.72	93.32	93.31
0.21	10000	25.50	93.60	94.75	94.79	93.78	92.55	92.15	93.39	94.78	94.85
0.21	57500	1.00	91.54	93.33	92.12	89.99	86.49	84.80	82.81	80.31	75.03
0.21	105000	1.00	89.34	91.83	89.92	87.94	84.99	83.63	81.13	76.41	68.89
0.21	152500	1.00	87.03	90.29	87.72	85.84	83.14	81.89	78.83	72.47	63.24
0.21	200000	1.00	84.63	88.71	85.51	83.71	81.17	79.97	76.37	68.66	58.00
0.14	10000	1.00	92.47	89.28	72.73	39.85	13.77	5.34	14.38	34.49	39.09
0.14	10000	13.25	92.46	90.31	84.60	78.29	72.72	71.00	75.25	81.41	82.86
0.14	10000	25.50	92.46	90.89	86.96	82.85	79.14	78.04	81.61	86.27	87.37
0.14	10000	37.75	92.45	91.30	88.21	85.04	82.14	81.31	84.55	88.50	89.44
0.14	10000	50.00	92.44	91.61	89.03	86.40	83.97	83.31	86.32	89.85	90.69
0.14	57500	1.00	91.09	87.24	77.44	65.14	54.58	50.92	51.38	51.33	44.04
0.14	57500	13.25	90.87	89.98	87.63	85.40	83.31	82.68	84.13	84.68	82.85
0.14	105000	1.00	89.68	85.15	77.02	67.66	59.45	56.43	53.81	47.37	35.12
0.14	152500	1.00	88.24	83.02	75.71	67.57	60.34	57.55	52.82	42.13	26.28
0.14	200000	1.00	86.78	80.89	74.05	66.59	59.87	57.18	50.78	36.77	17.97
0.10	10000	25.50	88.88	80.57	71.52	63.86	57.30	55.50	63.64	73.84	76.84
0.10	10000	37.75	89.19	82.54	75.52	69.47	64.23	62.83	69.80	78.30	80.80
0.10	10000	50.00	89.44	83.83	77.99	72.89	68.44	67.27	73.53	81.00	83.19
0.10	57500	13.25	87.76	82.94	78.08	73.76	69.92	68.81	72.26	74.79	72.89
0.10	57500	25.50	86.92	85.55	82.42	79.57	76.81	76.22	79.10	81.10	79.79
0.10	105000	1.00	83.63	68.11	48.85	33.24	20.25	15.85	17.04	12.77	0.00
0.10	105000	13.25	84.03	82.97	79.30	76.19	73.42	72.51	73.82	73.18	69.09
0.10	152500	1.00	81.45	67.51	51.04	37.43	25.98	21.87	18.85	7.25	0.00
0.10	152500	13.25	82.18	79.34	76.48	72.62	68.42	67.86	73.21	70.59	64.98
0.10	200000	1.00	79.27	66.29	51.39	38.89	28.27	24.28	18.11	0.93	0.00

Remark: n is coupled inductor winding ratio, f_{sw} is switching frequency (Hz) and L is energy transfer inductance (uH)

Coupled inductor winding ratio

As observed from the figure 5.8 and table 5.3, it is clear that the winding turns ratio is the parameter with the highest impact on the efficiency of the converter. When the winding ratio reduces, the efficiency significantly drops. A huge fall in converter efficiency can be found moving between winding turns ratio 0.5 to 0.1. The reason behind this is due to the current at the secondary side of the coupled inductor being reflected back to the primary side. Recalling equation 3.25, the current flowing in the switch during the on state is given as:

$$i_s = i_{Lm} + \frac{i_L}{n} \tag{5.2}$$

From the equation above, the switch current is inversely proportional to the coupled inductor turns ratio, and when the turns ratio is reduced, the current flowing into the switch is increased. Hence, the larger current generates more losses and reduces the overall efficiency. In order to achieve high efficiency, the turns ratio needs to be as large as possible.

Switching frequency

As expected, the result in the table shows that as the switching frequency increases, the efficiency reduces. The switching loss is directly proportional to the switching frequency.

Energy transfer inductance

As observed from the figures and table, increasing energy transfer inductance will increase the converter efficiency. The energy transfer inductance current is inversely proportional to the inductance. The energy transfer inductance derived in chapter 3 is based on the normalised units. Recalling the normalised current, base current and base impedance quantities,

$$i_x = \frac{j_x \cdot FV_o}{2\pi f_{sw}L} \tag{5.3}$$

This current is reflected back to the primary side and flows through the switch as mentioned earlier. Hence, as the energy transfer inductance increases, the current flowing through the MOSFET is reduced, resulting in the increase of overall converter efficiency.

In conclusion, the analysis confirms the impact of the coupled inductor winding ratio, switching frequency and energy transfer inductance on overall efficiency. There are many possible combinations of the three degrees of freedom, each of them have complex links between each others which combine to produce different converter efficiency trends. For example; at n = 0.21, $f_{sw} = 57.5 \text{ kHz}$, and L = 1 uH, the efficiency drops as the input voltage is increased from 30-100V. However, this trend does not apply to other combinations. At n = 0.14, $f_{sw} = 10 \text{ kHz}$, and L = 50 uH, the efficiency reduces as the input voltage increases, however, the efficiency starts to rise again when the input voltage is over 70V. The reason behind this is because different combinations give different operating conditions, varying from CCM to DCM operation and low to high duty cycle.

5.2.2 Selecting the 1st degree of freedom: coupled inductor turns ratio

As observed from the previous qualitative result, the coupled inductor turns ratio needs to be as large as possible to achieve high efficiency. In this section, more details about the choice of the coupled inductor turns ratio will be investigated by varying the winding ratio and selecting the switching frequency while fixing the energy transfer inductance value. The summary of the conditions used in the MATLAB simulation is shown below:

- Coupled inductor winding ratio n ranges from 0.5(1/2) to 0.2(1/5).
- Switching frequency f_{sw} is fixed to 10 kHz. When operating at high turns ratio, the switching frequency is limit to low frequency because the operating points shift toward high duty cycle. The limitation is when both winding ratio and switching frequency are high, the duty cycle could exceed 1. Therefore the switching frequency needs to be lower in order to shift the duty cycle toward low duty cycle. In this analysis, the switching frequency is selected at 10 kHz.
- Energy transfer inductance is fixed to 1 *u*H because the energy transfer inductance has the same impact on converter duty cycle as the turns ratio. When operating at high energy transfer inductance, the operating points are shifted toward high duty cycle. If both energy transfer inductance and turns ratio are high, the duty cycle could exceed 1 which is again impossible. Therefore the energy transfer inductance is selected to be a low value in order to ensure that the duty cycle remains below 1.
- The maximum duty cycle of the converter should not exceed 0.9.
- Efficiency includes losses in the power devices, capacitors and diodes excluding inductor losses.
- Assuming the magnetising inductance is infinite $(L_m \to \infty)$ so the magnetising inductor ripple current can be neglected $(\Delta i_{Lm} = 0)$.



The result from the MATLAB simulation is shown in figure 5.9.

Figure 5.9: Efficiency versus input voltage for different values of the coupled inductor turns ratio.

Table 5.4: Converter efficiency over all the input voltage for different values of coupled inductor winding ratio

			Input voltage (V)								
n	fsw	L	20	30	40	50	60	70	80	90	100
0.50	10000	1.00	94.42	95.74	96.39	96.79	97.05	97.64	98.34	98.57	98.64
0.40	10000	1.00	94.37	95.62	96.24	96.62	96.86	97.13	97.70	98.03	97.98
0.33	10000	1.00	94.25	95.46	96.06	96.42	96.08	96.12	96.66	95.94	96.68
0.29	10000	1.00	94.09	95.27	95.85	95.70	94.76	94.17	94.13	94.06	91.75
0.25	10000	1.00	93.91	95.07	95.64	94.55	92.44	90.11	88.40	88.22	86.27
0.22	10000	1.00	93.72	94.85	94.65	92.72	88.17	82.56	80.24	81.84	80.55
0.20	10000	1.00	93.51	94.63	93.45	89.72	80.61	72.18	70.95	74.97	74.43

As shown in the figure, when the coupled inductor turns ratio decreases, the efficiency starts to drop dramatically. This figure confirms the finding from the previous analysis. The reason why the efficiency drops, is mainly due to the secondary side current reflected back to the primary side, which causes more conduction losses. The maximum current stress is plotted in figure 5.10. As the turns ratio is decreased, the RMS current stress of the main switch is increased. The RMS current at winding ratio 0.2 is almost triple the value of that at winding ratio 0.5, which means that the conduction losses in the device are increased by a factor of around 9.



Figure 5.10: The RMS current stress in the main switch versus input voltage for different values of coupled inductor turns ratio.

The analysis suggests that the winding ratio of 0.5 gives the best efficiency over the wide input voltage range. However, it limits the choices of switching frequency and energy transfer inductance if operable duty cycle is to be achieved. As mentioned earlier, the maximum operating duty cycle is set to 0.9. This is to ensure that the voltage across the MOSFET device does not exceed the device voltage rating. Further analysis is carried out to find other possible values of switching frequency and energy

transfer inductance that, when combined, will not exceed the maximum operating duty cycle of 0.9.

This result shows that at winding ratio of 0.5,

- The maximum switching frequency is 17.5 kHz with energy transfer inductance of 1 uH. The energy transfer inductance is at the lower boundary, which could cause a problem with input current ripple as the value of magnetising inductance is small.
- The maximum energy transfer inductance is $1.5 \ u$ H with switching frequency at 10 kHz. The switching frequency is at the lower boundary, which means the crossover frequency of the loop gain is low. Another issue is the size of the magnetic components, switching at low frequency will increase the magnetic core size.

As a result, the winding ratio is slightly decreased to 0.4 to increase the choices of switching frequency and energy transfer inductance while reducing the converter efficiency slightly.

5.2.3 Selecting 2nd and 3rd degrees of freedom: the energy transfer inductance and switching frequency

In this section, both the energy transfer inductance and switching frequency will be analysed to find the best value that gives highest efficiency at nominal load conditions. The efficiency versus input voltage is calculated analytically over different values of energy transfer inductance and switching frequency while keeping the coupled inductor turns ratio constant. The summary of the conditions used in the MATLAB analysis is shown below:

- Energy transfer inductance L ranges from 1 to 50 uH and Switching frequency f_{sw} ranges from 10 to 100 kHz.
- Coupled inductor turns ratio n is selected to 0.4 from previous analysis.
- The maximum duty cycle of the converter should not exceed 0.9.
- Efficiency includes losses in the power devices, capacitors and diodes, but excludes any inductor losses.
- Assuming the magnetising inductance is infinite $(L_m \to \infty)$ so the magnetising inductor ripple current can be neglected $(\Delta i_{Lm} = 0)$.

The result from analysis is depicted in figure 5.11.



Figure 5.11: Efficiency versus input voltage for different values of the energy transfer inductance and switching frequency.

Table 5.5: Converter efficiency over all the input voltage for different values of energy transfer inductance and switching frequency

			Input voltage (V)								
n	fsw		20	30	40	50	60	70	80	90	100
0.40	10000	1.00	94.37	95.62	96.24	96.62	96.86	97.13	97.70	98.03	97.98
0.40	10000	2.50	94.35	95.61	96.24	96.61	96.86	97.14	97.71	98.29	98.33
0.40	10000	4.00	94.33	95.60	96.23	96.61	96.86	97.16	97.72	98.30	98.34
0.40	15000	1.00	93.97	95.35	96.04	96.45	96.73	96.90	97.45	97.77	97.67
0.40	15000	2.50	93.93	95.33	96.03	96.44	96.72	96.92	97.48	98.02	98.02
0.40	20000	1.00	93.56	95.08	95.83	96.28	96.58	96.66	97.21	97.74	97.36
0.40	20000	2.50	93.48	95.04	95.81	96.27	96.58	96.69	97.24	97.76	97.70
0.40	25000	1.00	93.15	94.80	95.62	96.11	96.44	96.43	96.96	97.46	97.35
0.40	30000	1.00	92.73	94.52	95.41	95.94	96.30	96.19	96.72	97.19	97.03
0.40	35000	1.00	92.30	94.24	95.20	95.77	96.15	95.96	96.47	96.91	96.71
0.40	40000	1.00	91.86	93.96	94.99	95.60	96.00	95.72	96.23	96.64	96.39
0.40	45000	1.00	91.42	93.67	94.77	95.42	95.86	95.49	95.98	96.37	96.07
0.40	50000	1.00	90.97	93.38	94.55	95.25	95.71	95.25	95.74	96.10	95.76

Energy transfer inductance

As shown in the figure above, there is little difference in efficiency when the value of the energy transfer inductor is varied. However, it can be noticed that as the inductance increases, the efficiency increases. This follows the result in the first analysis (wide sweep) as the energy transfer inductance is inversely proportional to the inductor current as derived in equation 4.3. Hence, the secondary current reflected back into the primary side during the switch turn-on is reduced, so the total current flowing through the switch is also decreased as shown in equation 4.2; which ultimately reduces the conduction loss. The disadvantage is that the operating duty cycle is shifted toward 1 which increases the voltage stress of the components. These effects have a small impact on the efficiency when the winding ratio is large.

However, if the winding ratio becomes small, the energy transfer inductor will have greater impact on efficiency. The following figure shows the efficiency versus input voltage for different values of energy transfer inductance at low turns ratio.



Figure 5.12: Efficiency versus input voltage for different values of the energy transfer inductance at low turns ratio.

The result shows the same trend as high winding ratio but with greater impact on the converter efficiency. This is due to the fact that the total current flowing through switch is inversely proportional to the winding ratio. Thus, total current flowing through switch becomes larger as the energy transfer inductance is reduced resulting in increasing conduction loss, which in turn, reduce the overall converter efficiency.

Switching frequency

The result from the analysis shows that as the switching frequency increases, the efficiency drops, as expected. This is due to loss associated with switching, or switching loss. The faster the device is switched, more switching losses are generated. However, the conduction loss also reduced as the switching frequency is increased. This is because the energy transfer inductance current is inversely proportional to the switching frequency. When the switching frequency increases, the total current flowing through switch is reduced, resulting in the reduction of conduction loss. At higher winding ratio the switching loss will dominate the conduction loss while at lower winding ratio the conduction loss will dominate the switching loss. This is due to the impact of winding ratio to the total current flowing through the device.

In the final design, the three main degrees of freedom in the converter design have been investigated, and values selected to guarantee operation over the wide range of input voltage and power from the fuel cell while maintaining high efficiency at nominal load. A winding ratio of 0.4, an energy transfer inductance of 2.5 uH and a switching frequency of 20 kHz are chosen. While the combination does not achieve the highest efficiency, 0.5% efficiency drop compared to that switching at 10 kHz, it is an acceptable trade-off to reduce the size of the magnetic components and simplify the control while maintaining the energy transfer inductance as high as possible. The operating points of the converter as a function of the duty cycle are plotted in figure 5.13.



Figure 5.13: Voltage gain as a function of duty cycle for different values of load resistance.

As observed from the figure 5.13, most of the operating points are in the DCM region and the duty cycle ranges from 0.33 (light load) to 0.86 (start-up). Although the converter operates mostly in the DCM region where the main switch loses its softswitching, the converter still maintains high efficiency. The reason behind this is the low switching frequency of 20kHz and high current so the generated switching loss is considerably lower than the conduction loss. The results from loss analysis (Chapter 7) show that at start-up to full load conditions, the conduction loss in the components dominates the switching loss. Hence, in this case operating in CCM operation mode, where there is a wider soft-switching region, has little benefit on the converter efficiency. However if the converter is operated at higher frequency > 200kHz, the switching loss would be significant and could dominate the conduction loss. Then, the converter should be designed to operate in the CCM region in order to utilise zero-voltage switching turn-on.

Table 5.6: Summary of the converter main operating points								
Operating Point	Duty cycle D	Load resistance $\boldsymbol{R}(\Omega)$						
Upper boundary startup load	0.8585	35.21						
Lower boundary startup load	0.8472	422.50						
Full load	0.5238	11.09						
20kW power load	0.3971	20.07						
Light load	0.3314	48.01						

The summary of the operating points is shown in table 5.6.

5.3 Selection of the Other Parameters

There are other important parameters in the converter such as the magnetising inductance L_m , clamp capacitor C_{CL} and output capacitor C_o . They must be designed to meet the converter specifications as summarised in table 5.7. In the previous analysis, the magnetising inductance is assumed to be infinite so the magnetising current ripple is neglected. This is because the coupled inductor is modelled as magnetising inductance and ideal transformer. The magnetising inductance does not affect the amount of power transferred to the load or the operating point of the converter. However, it affects the input current ripple as well as the total current flowing through power devices. Therefore, the magnetising inductance needs to be designed to accommodate the input current ripple requirement.

Table 5.7: Summary of converter specifications								
Parameter	\mathbf{Symbol}	Value						
Minimum input voltage	$V_{i(min)}$	20 V						
Maximum input voltage	$V_{i(max)}$	100 V						
Output voltage	V_o	650 V						
Output power	P_o	5.5-38.1 kW						
Magnetising indutance relative current ripple	$r_{i(Lm)}$	0.04						
Clamp capacitors relative voltage ripple	r_{CL}	0.2						
Output capacitors relative voltage ripple	r_{Co}	0.045						

Remark: relative ripple is defined as peak-to-peak ripple value divided by average value.

5.3.1 Selection of the magnetising inductance

The magnetising inductance is an important parameter which controls the input current ripple of the converter. It is essential to limit the peak-to-peak ripple to less than 4% of the input current, a characteristic needed to improve the fuel cell performance and increase lifetime of the fuel cell stacks. Assuming 100% efficiency (input power equals output power), the average magnetising current can be found by:

$$i_{Lm} = \frac{P_o}{2NV_i} \tag{5.4}$$

where N is the number of phases of the multiphase converter.

The peak-to-peak ripple of the input current can be calculated by the voltage across the inductor (V=Ldi/dt):

$$\Delta i_{Lm} = \frac{V_i}{f_{sw}L_m} D \tag{5.5}$$

The relative current ripple is:

$$r_{i(Lm)} = \frac{2NV_i^2}{P_o f_{sw} L_m} D \tag{5.6}$$

The converter benefits from interleaving which reduces the resulting input current ripple. Therefore, combining 5.6 and 5.1, the magnetising inductance is given by:

$$L_m = \frac{2NV_i^2 D\left(1 - \frac{m}{2ND}\right) \left(\frac{1 + m - 2ND}{(1 - D)}\right)}{P_o f_{sw} r_{i(Lm)}}$$
(5.7)

where $m = \text{floor} (2^*N^*D)$ is to floor value of (N^*D) .

Plotting equation 5.7 for all the operating points of the converter leads to the result shown in figure 5.14.



Figure 5.14: Required magnetising inductance versus input voltage to limit peak-topeak input current ripple to less than 4%.

Although the minimum magnetising inductance to limit peak-to-peak input current ripple to be less than 4% for all the operating input voltages is $3.72 \ m$ H, it occurs

when the output power from the fuel cell stacks is at minimum (high voltage and low current - light load). This operating point is less important and rarely occurs because the fuel cell has fallen into the light load region and its V-I characteristic is non-linear. Therefore, the magnetising inductance at nominal load 20 kW is selected at 0.75 mH as it is the operating point where the converter mainly operates (after the fuel cell temperature is stabilised). Although, at full load, the fuel cell reaches the maximum power and maximum current, the required magnetising inductance is low because it benefits from the interleaving technique. Moreover, figure 5.14, shows that there are 4 operating points where the input current has perfect current cancellation, regardless of any magnetising inductance value.

5.3.2 Selection of the clamp capacitor

The clamp capacitor is used to reclaim the leakage energy from the coupled inductor leakage inductance. The clamp capacitor is designed to have no more than 20% voltage ripple over all the input voltage range.

The clamp capacitor current is given by the following equation:

$$i_{CL} = \left(i_{Lm(peak)} + \frac{i_L}{n}\right) \Big|_{S_{3(on)}}$$
(5.8)

The total charge variation in the clamp capacitor can be found as:

$$Q = CV_o \tag{5.9}$$

$$\Delta Q = \mathcal{C} \Delta V_o \tag{5.10}$$

where

 ΔQ is the changing in capacitor's charge C.

 ΔV_o is the output voltage ripple V.

The clamp capacitor current is designed at the full load, an operating point where the converter is operated at full power and maximum input current. The required capacitance at this point is the highest compared to other operating points as the clamp capacitor value is directly proportional to the current. Hence, the total charge variation in the clamp capacitor is also highest at full load. Based on the selected values for the three main degrees of freedom, this point is in DCM with duty cycle higher than 0.5. The clamp capacitor current is plotted below.



Figure 5.15: Converter waveforms for magnetising inductance current, energy transfer inductance current, and clamp capacitor current during one switching cycle.

As observed from figure 5.15, the magnetising current reaches its peak and starts to decrease linearly when the switch S_3 is on. The clamp capacitor current has a decreasing piecewise linear behaviour and the average current in steady state is zero. The clamp capacitor current zero crossing happens when the switch is conducting. Therefore, the charge delivered to the clamp capacitor is equal to the highlighted area which can be easily calculated as:

$$\Delta \mathbf{Q} = \frac{1}{2} \cdot I_{Lm(peak)} \cdot \mathbf{t} = \mathbf{C} \Delta \mathbf{V}$$
(5.11)

× 2

Thus, the clamp capacitor is equal to (The derivation can be found in Appendix C.1):

$$C_{CL} = \frac{(1-D)}{2r_{CL}V_i} \cdot \frac{\left(\frac{P_o}{2NV_i} + \frac{V_iD}{2L_m f_{sw}}\right)^2}{\frac{V_iD}{L_m f_{sw}(1-D)} + \frac{V_i}{n^2 f_{sw}(1-D)} - \frac{FV_o}{nf_{sw}L}}$$
(5.12)
Thus, the clamp capacitor is 50 uF.

5.3.3 Selection of the output capacitor

The output capacitor can be calculated using the same principle as the clamp capacitor. The output voltage ripple must be below 4.5% to meet the aircraft power quality specification (MIL-STD-704F). The output capacitor current can be derived from figure 5.16 which is the output side of the converter (voltage doubler rectifier).

Applying the Kirchhoff current law, the capacitor current can be calculated by:

$$i_{Co1} = i_D - i_o$$
 (5.13)



Figure 5.16: Voltage doubler rectifier circuit.

The output capacitor is designed at the same operating point (full load) as clamp capacitor. At full load, the total charge variation in the clamp capacitor is highest. Thus, the required capacitance to control the output voltage ripple needs to be calculated at the full load condition. The converter waveforms for this condition are plotted in figure 5.17. It is in DCM mode and duty cycle over 0.5.



Figure 5.17: Converter waveforms for energy transfer inductance current, diode current, and output capacitor current during one switching cycle.

The average capacitor current in steady state is zero. Hence, the charge variation is equal to the highlighted area under the curve of the capacitor current which is given by:

$$\Delta \mathbf{Q} = \frac{1}{2} \cdot (I_1 - I_o) \cdot \mathbf{t} = \mathbf{C} \Delta \mathbf{V}$$
(5.14)

The required capacitance for a given relative voltage ripple can be found by (The derivation can be found in Appendix C.2):

$$C_{o} = \frac{V_{i}}{2r_{co}FV_{o}^{2}} \cdot \frac{(\frac{V_{i}}{nf_{sw}L} - \frac{(1-D)FV_{o}}{f_{sw}L} - \frac{V_{o}}{R_{o}})^{2}}{\left(\frac{V_{i}}{L} - \frac{n(1-D)FV_{o}}{L}\right)}$$
(5.15)

Thus, the output capacitor is 40 uF.

A summary of the final converter parameters is reported in table 5.8.

Operating point	Symbol	Value	
Coupled inductor turns ratio	n	0.4(16/40)	
Energy transfer inductance	L	2.5	uH
Switching frequency	f_{sw}	20	kHz
Magnetising inductance	L_m	0.75	mH
Clamp capacitor	C_{CL}	50	uF
Output capacitor	C_o	40	uF

Table 5.8: Summary of converter parameters

5.4 Scaling Design for Laboratory Prototype

For a laboratory implementation, a scaled-down version has been proposed due to limitations in cost, size and safety issues related with the full power system. At full power, the output from the fuel cell stacks is in the range of 20V-100V, 600A and 38.1kW peak power. In the prototype discussed in the following chapter, voltages are the same as the full power scheme but current is scaled-down by a factor 10. However, this scaling must be done carefully to behave like the full power version in terms of characteristics such as converter operating points and efficiency.

As discussed earlier regarding the converter characteristics, there are three degrees of freedom that mainly affect the converter operation. When the power is reduced by a factor of 10, using the same final values of the three degrees of freedom all the operating points would be shifted, as the normalised load resistance drops 10 times as shown in figure 5.18.



Figure 5.18: Voltage gain versus duty cycle for different normalised load resistance values at scaled-down laboratory prototype power 3.8kW (start-up load, full load, light load and nominal load 2kW).

Comparing figure 5.18 to figure 5.13, it can be clearly seen that the load resistance curves are shifted to the left which means that the operating duty cycle at the same voltage gain is lower. Therefore, in order to keep the same converter characteristics, one of the three degrees of freedom needs to increase by a factor of 10. Increasing the coupled inductor turns ratio will increase significantly current stress whereas increasing switching frequency generates more switching loss. Increasing these two parameters will make the scaled prototype an unrealistic representation of the actual version in term of efficiency. Therefore, increasing the energy transfer inductance by a factor 10 is the best scaling option.

Moreover, the efficiency of the scaled version needs to match the full power version as close as possible by choosing components that generate approximately the same ratio of losses at full power and adjusting other parameters such as magnetising inductance, clamp capacitance and output capacitance to match the same ratio of voltage and current stress (components selection will be discussed in Chapter 6).

5.5 Component Power Losses Modelling

In this section, component loss modelling are discussed. These power loss models are used in the analysis to optimise the converter parameters. The modelling is divided into two categories; active and passive components.

5.5.1 Active components

The active components are the controlled semiconductors and diodes. Power loss modelling for the MOSFET devices and diodes are presented in the following sections:

5.5.1.1 MOSFET losses

Power losses in a MOSFET device can be classified into two components; conduction losses (P_{cond}) and switching losses (P_{sw}) .

Conduction losses

MOSFET conduction loss can be simply modelled as an ideal switch connected to a resistor as shown in figure 5.19.



Figure 5.19: Equivalent circuit of MOSFET.

The instantaneous conduction loss can be calculated as the dissipated power in the resistor.

$$P_{cond}(t) = V_{DS}(t) \cdot i_D(t) \tag{5.16}$$

where

 V_{DS} is the drain to source voltage which can be calculated by $(V_{DS} = R_{DS} \cdot i_D)$ V. i_D is the drain to source current A.

The average conduction loss is given by,

$$P_{cond,avg} = \frac{1}{T} \int_0^T P_{cond}(t) dt$$
$$= \frac{1}{T} \int_0^T R_{DS} \cdot i^2_D(t) dt$$
$$= R_{DS} \cdot i^2_{D,RMS}$$
(5.17)

where $i_{D,RMS}$ is root mean square value of the drain to source current A.

The value of R_{DS} can be calculated by $R_{DS} = V_{DS}/i_D$ using information provided in the device manufacturer's datasheet as depicted below in figure 5.20.



Figure 5.20: Typical output characteristics of MOSFET IXFN73N30.

In addition, the effect of junction temperature T_j to the value of R_{DS} needs to be taken into account so the conduction loss is more accurate. It is assumed that the junction temperature is 100 °C where the value of R_{DS} is approximately 1.65 times higher than the nominal value of R_{DS} .



Figure 5.21: Temperature dependence of drain to source resistance of MOSFET IXFN73N30.

Switching losses

Switching loss occurs when the device is transitioning from off-state to on-state and vice-versa. The voltage and current waveforms during these transitions are depicted in figure 5.22. The highlighted areas represent the switching losses.



Figure 5.22: Voltage and current waveforms: (Left) During turn-on transition. (Right) During turn-off transition.

The turn-on energy losses (E_{on}) is given by

$$E_{on} = \int_0^{t_{on}} V_{DS}(t) \cdot i_{D,on}(t) \, \mathrm{d}t$$

$$=\frac{V_{DS,on} \cdot i_{D,on} \cdot t_{on}}{2} \tag{5.18}$$

where

 t_{on} is the turn-on time of the MOSFET S.

 $i_{D,on}$ is the turn-on drain current A.

The turn-off energy losses (E_{off}) can be similarly calculated by

$$E_{off} = \int_0^{t_{off}} V_{DS}(t) \cdot i_{D,off}(t) \, \mathrm{d}t$$

$$=\frac{V_{DS,off} \cdot i_{D,off} \cdot t_{off}}{2} \tag{5.19}$$

where

 t_{off} is the turn-off time of the MOSFET S.

 $i_{D,off}$ is the turn-off drain current A.

Hence, the total switching losses can be calculated by the sum of the turn-on energy losses and turn-off energy losses multiplied by the switching frequency.

$$P_{sw} = (E_{on} + E_{off}) \cdot f_{sw} \tag{5.20}$$

The value of t_{on} and t_{off} can be found from the device manufacturer's datasheet.

5.5.1.2 Diode losses

Power losses in the diode is divided into two components; conduction losses and reverse recovery loss.

Conduction losses

Conduction losses are the average dissipated power in the diode during forward-biased operation. The power loss model for diode can be represented as a switch, voltage source, and resistor as shown in figure 5.23.



Figure 5.23: Equivalent circuit of diode.

The average conduction loss is given by,

$$P_{cond,avg} = \frac{1}{T} \int_{0}^{T} P_{cond}(t) dt$$

= $\frac{1}{T} \int_{0}^{T} (V_{T0} \cdot i_F(t) + R_F \cdot i^2_F(t)) dt$
= $V_{T0} \cdot i_{F,avg} + R_F \cdot i^2_{F,RMS}$ (5.21)

where

 V_{T0} is the forward voltage drop across diode V.

 $i_{F,avg}$ is the average diode current A.

 $i_{F,RMS}$ is the RMS value of diode current A.

 R_F is the resistance of diode Ω .

The values of V_{T0} and R_F can be found in the manufacturer's datasheet as shown below.



Figure 5.24: Forward current versus voltage drop of Diode DSEI30.

Reverse recovery loss

When the diode is transitioning from the conducting state to the blocking state, a stored charge must be dissipated before the diode will enter the blocking state. Hence, the current is temporarily flows in the reverse direction for a short period of time called the reverse recovery time. There are losses generated in this period which are the reverse recovery losses (or switching off losses). Figure 5.25 illustrates the voltage and current waveforms during reverse recovery.



Figure 5.25: Voltage and current waveforms during reverse recovery time.

The reverse recovery energy losses E_{rr} can be calculated by,

$$E_{rr} = \int_0^{t_{rr}} V_F(t) \cdot i_{RM}(t) dt$$
$$= \frac{V_R \cdot i_{RM} \cdot t_{rr}}{2}$$
(5.22)

where

 V_R is reverse voltage of diode V.

 i_{RM} is peak reverse recovery current A.

 t_{rr} is reverse recovery time S, which can be found from the device manufacturere's datasheet.

The reverse recovery losses of diode can be calculated

$$P_{rr} = E_{rr} \cdot f_{sw} \tag{5.23}$$

The value of i_{RM} is given by the component manufacturer's datasheet.

5.5.2 Passive components modelling

In this section, the models of passive components for the coupled inductor and capacitor are presented. These models can be used to predict the power losses occurring in each of the passive components which is information required in designing the converter. The coupled inductor can be designed and optimised to achieve lower power losses. However, the capacitor cannot be optimised, it is selected from the preferred capacitance values.

5.5.2.1 Coupled inductor losses

In the IBCI converter, the coupled inductor is used. In the magnetic core, the flux is confined in the magnetic path which results in low leakage flux and low eddy current losses in the wires. However, using the magnetic core can generate additional losses associated with magnetic material known as magnetic core losses. The coupled inductor power losses can be divided into two types; the core loss and copper loss.

Core losses The magnetic core losses can be found from datasheet of the core material [60]. In this converter, a METGLAS amorphous alloy 2605SA1 material is used for the coupled inductor core.

The power core losses can be calculated by

$$P_{core} = 6.5 \cdot f_{sw}^{1.51} \cdot B^{1.74} \cdot M_{core} \tag{5.24}$$

Where

 f_{sw} is switching frequency kHz. B is magnetic flux of the core T. M_{core} is mass of the core kg.

The value of M_{core} can be found from datasheet. It depends on size of the core.

Copper losses

The copper loss is the heat produced by the current in the conductors of the coupled inductor windings. Two resistance values are important; DC resistance (R_{dc}) and AC resistance (R_{ac}) . The DC resistance is a function of the cross-sectional area of the wire. The AC resistance depends on the eddy current effect. The equivalent circuit of the coupled inductor is depicted in figure 5.26 where L is the inductance (magnetising and leakage inductances) and C_L is the inductor self-capacitance.



Figure 5.26: Voltage and current waveforms during reverse recovery time.

The copper losses can be calculated by

$$P_{copper} = i_L^2 \cdot R_{dc} + i_{L,RMS}^2 \cdot R_{ac} \tag{5.25}$$

The value of R_{dc} and R_{ac} can be found from the datasheet. It depends on the cross-sectional area, length and resistivity of the conductor.

Therefore, the total losses of the coupled inductor are given by

$$P_{tot} = P_{core} + P_{copper} \tag{5.26}$$

5.5.2.2 Capacitor losses

The capacitor can be modelled by including an equivalent series resistance (R_{ESR}) and series equivalent inductance (R_{ESL}) . These values are usually given by the datasheet. However, the series equivalent inductance is significant only at relatively high frequencies. The simplified equivalent circuit of a capacitor is depicted in figure 5.27.



Figure 5.27: Equivalent circuit of capacitor.

The capacitor power loss can be calculated by

$$= R_{ESR} \cdot i^2_{C,RMS} \tag{5.27}$$

where $i_{C,RMS}$ is the RMS value of capacitor current A.

5.6 Conclusions

In this chapter, the impact of the three main degrees of freedom on the converter characteristics was discussed. In addition, the selection of the main converter parameters based on converter efficiency and fuel cell specifications was optimised. A MATLAB model was used as a tool to approximate the converter efficiency across the whole operating range, by evaluating the analytical expressions of voltages and currents. Moreover, the relationship between the full power converter and the reduced power prototype was examined. Finally, the power losses modelling in each component was explained. In the next chapter, the laboratory-scale of the proposed converter is introduced.

Chapter 6

Experimental Converter Hardware

6.1 Introduction

In order to verify the feasibility of the converter topology proposed in Chapter 4 and to validate the design process presented in Chapter 5, an IBCI converter has been built. The IBCI converter rig is a scaled-down prototype of the 3 phase IBCI designed in Chapter 5. This chapter will present all of the design process for the IBCI converter rig including the passive components.

6.2 Converter Prototype Overview

An overview of the converter hardware and a photograph of the IBCI converter rig setup are shown in figure 6.1 and figure 6.2. The key components of the test rig are listed in Table 6.1. The main components of the converter are 3-single phase IBCI converters, coupled inductors, energy transfer inductors (originally planned to be additional inductors but eventually integrated in the coupled inductor), diode bridge rectifier, safety trip board. A PC is used as the human-machine interface.



Figure 6.1: Diagram of the converter.



Figure 6.2: Photograph of the experimental rig.

Name	Specification	Quantity
DSP	TMS320C6713	1
FPGA	ProASIC3 A3P1000	1
Coupled inductor	1uH/10A	6
MOSFET	IXFN73N30	12
Diode	DSEI30A	6
Clamp Capacitor	$10 \mathrm{uF} / 250 \mathrm{V}$	24
Output Capacitor	ED2G470 (40uF/400V)	2
Voltage transducer	LEM LV 25-P	7
Current transducer	LEM LA 55-P	6

Table 6.1: List of key components

Design considerations for the choice of each of the main components will be discussed in sections 6.2-6.7. The size and weight of the prototype rig have not been considered because this will increase the overall cost of the converter. To minimise size and weight of passive components, the converter needs to operate at higher frequency which results in increasing the switching losses. Thereby, the converter efficiency is reduced. In order to increase efficiency and operate at higher frequency, alternative power devices such as SiC MOSFETs could be used with additional cost.

The input voltage DC power supply is a TDK-Lambda GEN 80-187.5 [61] which is able to supply voltage 0-80V at a current of 0-187.5A. This PSU with wide range of voltage and current allows the rig to be tested at various operating points according to fuel cell voltage-current characteristics. To verify the converter operation, a few sample operating points along the power versus fuel cell voltage curves are selected. The single phase IBCI consists of two coupled inductors and two half-bridge cells. Each cell comprises two IXFN73N30P MOSFETs[62], active clamp capacitor [63], voltage sensor LV-25P [64] and current transducer LA-55P [65] mounted together with 2 gate drive circuits on a printed circuit board(PCB). The voltage sensor is used for controlling the output voltage level while the current sensor is used for safety protection. The voltage doubler rectifier is composed of 6 DSEI30-10A [66] diodes and output capacitor.

The control platform used in this rig is a field programmable gate array (Actel ProA-SIC3 FPGA) to generate the switching signals and a digital signal processor (Texas Instruments TMS320C6713 DSP) to implement the control strategies and modulation. The output voltage measurement is required for the voltage control loop.

6.3 Half-Bridge Converter Design

The half-bridge circuit is referred to the 4 MOSFET devices and clamp capacitors in the IBCI converter (as shown in figure 6.3). This circuit board includes fiber optic receivers, dead-time circuits, gate driver circuits, MOSFETs, voltage transducer and current transducer. The diagram of the half-bridge converter board is shown in figure 6.4. A photograph of the current doubler circuit and active clamp is shown in 6.5. It consists of 2 printed circuit boards: gate driver board and power module board.



Figure 6.3: Diagram of single phase IBCI converter.



Figure 6.4: Diagram of half-bridge converter board.



Figure 6.5: Photograph of half-bridge converter board.

The control signal from the FPGA is sent to the half-bridge board through the fiber optic cable. The advantages of using fiber optics are good noise immunity (noise caused by electromagnetic interference), fast transmission (large capacity to carry high speed signals over long distance between control platform and power circuit) and safety.

The signals are received by the Avago Technologies HFBR-1521 receivers and are later transmitted to an analogue dead-time circuit. This circuit is to ensure there is enough time between two MOSFETs turn-on and turn-off to prevent shoot-through or cross-conduction current that could lead to a short in the bridge. Figure 6.6 shows the circuit diagram. The dead time circuit is made of a diode connected in parallel with the resistor of an RC circuit. This allows the RC circuit to generate a time delay in the rising edge of the PWM, due to the charge time constant of the capacitor. In the experiment, a potentiometer is used to adjust dead time of the PWM signal.



Figure 6.6: Diagram of dead time and PWM enable circuit.

From figure 6.6, the output signal from the RC circuit is compared with 5V constant signal using a Schmitt trigger buffer (SN74LVC1G17) with an input threshold voltage (2.65-3.33V). The output signal is then sent to a NOR gate (MC74VHC1G03). This is to provide the safety protection to the circuit to disable PWM signal in case the trip signal is triggered. The output NOR gate is connected to a 5V supply via a pull-up resistor($R=270\Omega$) because the optocoupler (HCPL-3120) requires an input current around 7-16mA. A single gate without a pull-up resistor will usually have low output current which is not enough to drive the optocoupler gate. Therefore, a NOR gate with open collector output and a pull-up resistor are used. This configuration will ensure there is enough current to drive the optocoupler gate.

The signal is then sent to the gate driver circuit shown in figure 6.7 The gate drive circuit consists of an HCPL-3120 high speed optocoupler, a gate resistance (R_G) , two Zener diodes $(D_{Z1} \text{ and } D_{Z2})$ and a gate-source resistance (R_{GS}) .



Figure 6.7: Diagram of gate drive circuit.

The HCPL-3120 gate drive optocoupler is specifically designed for gate drive applications with a peak voltage and current supplied make it ideally suited for driving MOSFETs. It is capable of driving a 2A peak current into the MOSFET gate. An isolated DC-DC converter (NMH0515S) is used to power the optocoupler with \pm 15V from a 5V power supply and it provides electrical isolation to the gate drive circuit.

The gate resistance (R_G) determines the current which will drive the gate of the MOSFET. A small R_G will cause fast turn-on and turn-off time since the gate peak current increases and therefore it reduces the switching losses. However, too small resistance could affect the voltage stress on the MOSFET due to the resonance from the stray inductance in the circuit and the intrinsic capacitance in the MOSFET. To

select gate resistance, there are two requirements that needs to be satisfied.

First, dv/dt capability

In the MOSFET manufacturer's datasheet, there is a limitation of the maximum rate of rise of drain to source voltage allowed. If the value is exceeded then the voltage across the gate source terminals may become higher than the threshold voltage of the MOSFET, resulting in the device going into current conduction mode [67]. The dv/dt capability is set by,

$$\frac{dv}{dt} = \frac{V_{TH}}{R_G C_{GD}} \tag{6.1}$$

where

 V_{TH} is the threshold voltage V.

 C_{GD} is the gate to drain capacitance F.

Both of these values can be found from the device manufacturer's datasheet.

Hence, the minimum gate resistance to satisfy this limitation is

$$R_G(min) \ge \frac{V_{TH}}{\frac{dv}{dt} \cdot C_{GD}}$$
(6.2)

In this case, the minimum gate resistance is 1.21Ω .

Second, I_{OL} peak specification

The HCPL-3120 gate drive optocoupler has the limitation of maximum output current (I_{OL}) defined by the voltage supplied [68].

$$I_{OL} = \frac{(V_{CC} - V_{EE} - V_{OL})}{R_G}$$
(6.3)

where

 V_{CC} and V_{EE} are the positive and negative supply voltage V. V_{OL} is the output voltage V.

Thus, the minimum gate resistance to satisfy this can be found by,

$$R_{G(min)} \ge \frac{(V_{CC} - V_{EE} - V_{OL})}{I_{OL}}$$
 (6.4)

In this case, the minimum gate resistance is $11.2 \ \Omega$

A suitable value of gate resistance to satisfy both requirements 30 Ω is selected for the prototype rig.

To prevent MOSFET gate overvoltage, two 15V back to back Zener diodes are connected between the gate and source. These diodes prevent the gate voltage rising higher than the maximum rated gate voltage of ± 20 V. In addition, a 20k Ω resistor for R_{GE} is added across the gate-source connection of the MOSFET for safety protection. It is to keep the gate-source voltage of the MOSFET low even if the gate signal is floating, preventing undesired turn-on.

Regarding MOSFET selection in the rig, the same scaled down power loss (and therefore the same efficiency) of the full power version converter is selected. As discussed in the previous chapter, the constructed prototype is a reduced power version of the full power converter, scaled by a factor 10. All the converter characteristics and efficiency of the reduced power are designed to behave like the full power converter. In the full power system, the maximum voltage stress and current stress of upper and lower switches of half-bridge converter are plotted over the input voltage as shown in figure 6.8 and figure 6.9. The maximum voltage stress and current stress are 141V and 300A, respectively. There is no single MOSFET that can handle this current stress. Therefore, a parallel configuration of MOSFETs is required. Three parallel connected MOSFETs IXFN160N30T with Vds of 300V, Ids of 132A and Rds(on) of 19m Ω have been selected as the power devices for the full power converter. The reason to choose a 3 parallel MOSFETs is because it is the minimum number of parallel devices that can withstand the maximum current stress of 300A (2 parallel devices, the current rating is 2*132=264A which is lower than the maximum current stress).



Figure 6.8: Voltage and current stress over input voltage of the lower MOSFET. (Top left) voltage stress. (Top right) voltage stress in rms. (Bottom left) current stress. (Bottom right) current stress in rms.



Figure 6.9: Voltage and current stress as a function of input voltage of the upper MOSFET. (Top left) Voltage stress. (Top right) RMS voltage stress. (Bottom left) Current stress. (Bottom right) RMS current stress.

At reduced power, the maximum voltage stress remains the same at 141V and current stress is reduced by 10 times 30A. In order to select MOSFET that matches with full power losses, the on resistance for reduced power needs to satisfy the following condition;

The conduction losses in the full power system are higher than the reduced power system by a factor of 10,

$$P_{con,full} = 10P_{con,reduce}$$

Recalling equation 4.17, the conduction losses of MOSFET device is given by,

$$i_{RMS,full}^2 \cdot R_{DS,full} = 10 (i_{RMS,reduce}^2 \cdot R_{DS,reduce})$$

In the full power example, 3 MOSFETs are connected in parallel so the current is reduced by a factor of 3 and the total conduction loss is the sum of three MOSFETs.

In addition, the current in the small scale prototype is 10 times lower than the full power one $(i_{RMS,full} = 10i_{RMS,reduce})$.

Thus, the above equation can be rewritten as,

$$3 \cdot (\frac{10i_{RMS,reduce}}{3})^2 \cdot R_{DS,full} = 10(i_{RMS,reduce}^2 \cdot R_{DS,reduce})$$

$$R_{DS,reduce} = 3.33 R_{DS,full} \tag{6.5}$$

Therefore, the on resistance for the small scale prototype needs to be 3 times higher than at full scale which is 57 $m\Omega$.

In addition, the turn-on time and turn-off time of the MOSFET for the small scale prototype needs to satisfy the following condition.

The switching losses in the full scale system are higher than the small scale system by a factor of 10,

$$P_{sw,full} = 10P_{sw,reduce}$$

Recalling equation 4.20, the switching losses of a MOSFET device are given by

$$V_{full} \cdot i_{full} \cdot (t_{on,full} + t_{off,full}) \cdot f_{sw} = 10 \ V_{reduce} \cdot i_{reduce} \cdot (t_{on,reduce} + t_{off,reduce}) \cdot f_{sw}$$

The full power voltage is the same as the reduce power voltage and the full power current is 10 times higher than the reduced power current. Therefore,

$$(t_{on,full} + t_{off,full}) = (t_{on,reduce} + t_{off,reduce})$$
(6.6)

The total turn-on time and turn-off time of device used in the full scale example needs to be the same as the device used in the small scale circuit.

Therefore, the closest MOSFET device that meets the above requirements is IXFN73N30P with Vds of 300V, Ids of 73A, and Rds(on) of $45m\Omega$ is selected for the experimental

rig. Although the on resistance of the reduced power MOSFET is lower than 57 $m\Omega$, the turn-on time and turn-off time is higher. The higher switching losses will compensate the reduction in conduction losses. The power losses of the power devices in the full power converter and reduced power prototype as a function of the input voltage are plotted in figure 6.10, where the losses in the reduced scale prototype are multiplied by a factor of 10 for better visualisation. As observed in figure, the prototype rig has similar device losses compared to the full power converter. The maximum difference is 76W which is less than 0.2% of the nominal power. Therefore, using MOSFET IXFN73N30P in the reduced power prototype rig provides the same scaled down power losses to the full power version.



Figure 6.10: Comparison of the device loss in the full load converter and in the reduced power prototype, multiplied by 10.

The summary of selected MOSFET parameters is shown in the table below:

1 1 01					
		Full power		Reduced power	
	Symbol	IXFN160N30	TC	IXFN73N3	0P
Drain source voltage	V_{DS}	300	V	300	V
Continuos drain current	I_D	132	А	73	А
On resistance	$R_{DS(on)}$	19 m	nΩ	45	$\mathrm{m}\Omega$
Rise time	t_r	112	nS	110	nS
Fall time	t_{f}	113	nS	150	nS

Table 6.2: Summary of selected MOSFET parameters in full power converter and reduced power prototype

6.4 Thermal Design

A heatsink is used to dissipate heat in the power semi-conductor devices by ensuring that the junction temperature is kept within its rated specification. To properly design the heatsink, the average power losses in the power devices are calculated at the worst case scenario full load power. The average power loss in the lower and upper devices in each half-bridge are $P_{av}=13.48$ W and 2.62W respectively. The average power loss can be used to determine the required thermal resistance of the heatsink. The simplest model of an heatsink is shown in figure 6.11 with the reference thermal impedances provided by the datasheet (Table 6.3). In the design, the ambient temperature (T_a) is assumed to be $T_a = 30$ °C and the maximum allowed junction temperature (T_j) is $T_j = 100$ °C.

Table 6.3: Thermal impedance of IXFN73N30P

	Typical (K/W)	Max (K/W)
$R_{th(J-C)}$	0.05	0.24
$R_{th(C-H)}$	0.05	0.24



Figure 6.11: Diagram of heatsink.

The design of the heatsink has been based on the worst case scenario at full load power. In those conditions, the temperature at heat sink (T_s) and ambient (θ_H) can be calculated by:

$$T_{s} = T_{j} - (P_{av} \ge (R_{th(J-C)} + R_{th(C-H)}))$$
(6.7)

Hence, heat sink temperature at worst case scenario is $T_s = 93.21$ °C for lower MOS-FET and 98.56 °C for upper MOSFET. The thermal resistance of the heatsink needs to satisfy:

$$R_{th(H)} < \left(\frac{T_s - T_a}{P_{av}}\right) < 4.47 \text{ K/W}$$
 (6.8)

Hence, the thermal resistance of the heatsink $(R_{th(H)})$ needs to be less than 4.47 K/W in order to keep the junction temperature lower than 100°C. An available offthe-shelf heatsink with size matching half-bridge converter PCB and with thermal resistance lower than 4.47 K/W is the Fisher Electronik SK508 100SA, with thermal resistance of 1.75 K/W. This is clearly overrated for the experimental rig, but it has been selected to keep a large thermal safety margin. This can be made smaller in a practical converter where size optimisation is a key design parameter.

6.5 Voltage Doubler Rectifier

At the secondary side of the 3 phase IBCI converter, 6 fast recovery diodes are used for the voltage doubler rectifier. The input is connected to the transfer power inductor and output is connected to the two output capacitors. One of the capacitors will store in one half cycle, while the other is charged in the opposite half cycle. Hence, the total output voltage across these two capacitors is twice the input voltage. The circuit diagram is shown in figure 6.12.



Figure 6.12: Diagram of voltage doubler rectifier.

To select the proper diode, the voltage and current stresses in the diode have been plotted in 6.13. The maximum voltage stress and current stress are 650V and 80A, respectively.



Figure 6.13: Voltage and current stress as a function of the input voltage of the output diode rectifier. (Top left) Voltage stress. (Top right) RMS voltage stress. (Bottom left) Current stress. (Bottom right) RMS current stress.

Thus, a fast recovery diode IXYS DSEI30-12A with repetitive reverse voltage of 1.2kV and forward current of 30A is selected for both full power converter and reduced power prototype. However, in full scale 3 diodes are connected in parallel to share the current whereas in reduced scale a single connection is enough to sustain the current stress.

The summary of selected diode parameters is shown in the table below:

 Table 6.4: Summary of selected diode parameters in full power converter and reduced

 power prototype

	Symbol	DSEI30-12A
Repetitive reverse voltage	V_{rrm}	1200 V
Forward current	I_f	30 A
Forward voltage drop	V_F	2.5 V
Reverse recover time	t_{rr}	40 nS

6.6 Magnetic Components Design

Firstly, the coupled inductor is one of the core components in this converter. A coupled inductor behaves like a transformer in the sense that it increases or decreases the output voltage with respect to the input voltage based on the turns ratio. However, there are several differences that distinguish between them. First, a transformer transfers the energy from the primary winding to secondary winding ideally with no energy stored, while the coupled inductor has an air-gap and stores the energy in the core flux.

Secondly, in a transformer the changing current creates the magnetic flux which induces the secondary voltage (emf). This causes the current to flow in secondary windings and creates an opposite flux due to the opposite polarity of primary and secondary windings. Hence, the net flux in ideal transformer sum up to be zero. However, in coupled inductor both primary and secondary is conducting at the same time. Mutual coupling of the coupled inductor is present and the fluxes generated by the windings are the same polarity. Hence the total next flux is added up (energy stored).

When designing the transformer, the coupling between the windings need to be as

good as possible to minimise the leakage inductance which affects the power transfer and causes ringing effects at a high frequency. However, in our case, the leakage inductance is an important parameter as it determines the energy transfer in the converter. Hence, the value of leakage inductance in the coupled inductors of the IBCI should ideally be controlled to achieve the required energy transfer.

In the prototype of the converter rig, an amorphous magnetic core is used as it offers smaller, lighter and more energy efficient designs due to its superior magnetic characteristics: high resistivity, high saturation induction, and low core loss. The amorphous metal cores can operate up to a flux saturation level of 1.56 Tesla while the typical ferrite core can only operate at 0.3-0.5 Tesla [69]. Hence, it is suitable for high frequency application. To select the appropriate core frequently involves a trial-and-error type of calculation and a simplified method of selecting the magnetic core is introduced. The inductor energy handling capability is related to magnetic core area product (A_P) which is product of available core window area (W_A) and effective core cross-sectional area (A_C) . In designing the coupled inductor, the total energy (E_t) is an important parameter as it has to be designed to accommodate both the primary energy (E_1) and secondary energy (E_2) .

The total energy E_t can be found by,

$$E_t = E_1 + E_2 (6.9)$$

The energy handling capability of the coupled inductor can be calculated by (The derivation can be found in Appendix D),

$$A_P = \frac{2E_t}{K_u BJ} \tag{6.10}$$

where

 K_u is the window utilisation factor.

B is the magnetic field T.

J is the current density A/cm^2 .

Therefore, using the above equation, a suitable amorphous core METGLAS (R)Alloy 2605SA1 POWERLITE C core size AMCC32 is used.

The following list summarises the main parameters of the amorphous AMCC32 core:

- Core sectional area: $A_c = 3.2 \ cm^2$.
- Window area: $W_a = 8.4 \ cm^2$.
- Mass: m = 0.46 Kg.
- Electrical Resistivity: $\rho = 137 \ \mu\Omega cm$.



Figure 6.14: Magnetic circuit of inductor [11].

According to figure 6.14, the magnetic circuit can be derived as:

$$ni = \Phi(\Re_c + \Re_q) \tag{6.11}$$

where n is the turns ratio of the winding.

i is the inductor current A.

 Φ is the magnetic flux Wb.

 \Re_c is the reluctance of the core ${\rm H}^{-1}.$

 \Re_g is the reluctance of the gap $\mathrm{H}^{-1}.$

Given the peak of the inductor current I_{max} , it is desired to operate the core flux density at the peak of flux saturation B_{sat} . Hence, the value of B_{max} is chosen to be less than the worst case scenario of the saturation flux density of the material core. Rearranging the above equation by substituting the Faraday's law of induction, magnetic flux Φ is defined as B·A where B is the magnetic field and A is the area perpendicular to the magnetic field.

$$B_{max} = \frac{I_{Lm,max}L_m}{N_1 A_e} \tag{6.12}$$

In order to properly design the inductor, the worst case operating scenario of the converter needs to be defined.



Figure 6.15: Graph of product of the maximum magnetising current and magnetising inductance as a function of the input voltage.

Figure 6.15 represents the product of the value of $I_{Lm,max}$ and L_m over different operating duty cycle of the converter. The maximum inductor current $(I_{Lm,max})$ is

the peak current which is equal to the average inductor current and half of the peak to peak ripple current $(\overline{I_{Lm}} + \frac{\Delta I_{Lm}}{2})$. The magnetising inductance L_m is equal to 0.75mH as designed in chapter 5 to minimise the input current ripple to less than 4% over all the operating points. As shown in figure 6.15, the worst case scenario occurs at full load condition where the product of $I_{Lm,max}$ and L_m is equal to $3.9 \cdot 10^{-4} A \cdot H$. The maximum magnetic flux of the inductor core is set to 1T to avoid the saturation of the core. Therefore, the turns ratio of the primary winding is:

$$N_1 = \frac{I_{Lm,max}L_m}{B_{max}A_e} = 16 \text{ turns}$$
(6.13)

Substituting equation 6.11 with Faraday's law $v(t)=n\frac{d\Phi(t)}{dt}$, the magnetising inductance can be derived as:

$$L_m = \frac{N_1^2}{\Re_c + \Re_q} \tag{6.14}$$

The reluctance of the magnetic core is given by $(\Re = \frac{l_{core}}{\mu_0 \mu_r A_c})$. The magnetising inductance equation can then be given as:

$$L_m = N_1^2 \cdot \left(\frac{l_{core}}{\mu_0 \mu_r A_c} + \frac{l_{gap}}{\mu_0 A_c}\right)$$
(6.15)

where

l is the magnetic path length cm.

 μ_r is the permeability of the magnetic material H·m⁻¹.

 μ_0 is the permeability of air $4\pi 10^{-7}$ H·m⁻¹.

 A_c is the cross-section of the core cm^2 .

The reluctance of the air gap is significantly higher than that of the core even when the air gap is small $\left(\frac{l_{core}}{\mu_0\mu_rA_c}\gg\frac{l_{gap}}{\mu_0A_c}\right)$. The reason for this is that the magnetic material has relatively high permeability so the reluctance of the core can be neglected. Hence,
the total reluctance of the circuit depends mainly on the air gap rather than on the core.

$$L_m = N_1^2 \cdot \frac{l_{gap}}{\mu_0 A_c}$$

Re-arranging the above equation, the length of the air gap can be calculated by:

$$l_{gap} = \frac{N_1^2 \mu_0 A_c}{L_m} = 0.23 \ cm \tag{6.16}$$

Therefore, length of the air gap is 2.3 mm.

Wire selection for primary and secondary windings:

The current density (J) of the wire is the electric current per unit area of crosssection. Selecting low value of J will require larger cross-sectional area of copper for a given current. Hence, it requires large size of winding window of the inductor core. However, increasing the value of J increases the copper loss. In general, the value of current density (J) is selected in between 200-500 A/cm^2 . In the design J of 500 A/cm^2 is chosen. The required useful cross-sectional area of the winding is calculated by:

$$a = \frac{I_{rms}}{J} \tag{6.17}$$

The voltage and current stress of the coupled inductor as a function of the input voltage is plotted in figure 6.16. The maximum RMS current stress in the reduced power prototype is 114.5/10 = 14.5 A at primary winding and 5.8 A at secondary winding. Hence, the cross-sectional area for primary winding is 0.029 cm^2 and secondary winding is 0.011 cm^2 .



Figure 6.16: Current stress of the coupled inductor as a function of the input voltage. (Top left) current stress. (Top right) RMS current stress.

At higher frequency, there is a concentration of current near the wire surface which is due to the skin effect. This is the result of magnetic flux lines that generate Eddy currents in the magnet wire and oppose the applied magnetic field. Skin effect causes the effective resistance of the conductor to increase at higher frequencies where the skin depth is smaller. Hence, it reduces the effective cross-section of the conductor.

skin effect
$$\delta = \sqrt{\frac{\rho_{cu}}{\pi\mu_0\mu_r f_{sw}}} = \frac{6.5}{\sqrt{f_{sw}}} = 0.046 \ cm$$
 (6.18)

where ρ_{cu} is resistivity of copper 1.68 \cdot 10⁻⁸ Ωm at 100 °c. Therefore, the skin effect at 20 kHz frequency is $4.6 \cdot 10^{-2} cm$

By taking skin depth into account, the minimum diameter of the winding can be calculated by

δ

$$a = \frac{D^2 \pi}{4} - \frac{(D - 2 \cdot \delta)^2 \pi}{4}$$
$$D = \frac{a + \delta^2}{\delta}$$
(6.19)

The minimum diameter of the primary winding is 0.48 cm and secondary winding is 0.22 cm. A copper wire size AWG4 and AWG11 can be used for primary winding and secondary winding, respectively. However, the AWG4 wire is thick and difficult to wound into the C core so 4 parallel AWG11 (0.25 cm) wires are used instead for the primary winding and a single AWG11 is used for the secondary winding.

Finally, it must be verified if the windings will fit into the window area of the inductor core. According to the amorphous AMCC32 core, the window area is equal to 8.4 cm^2 .

$$A_w > n_1 a_1 + n_2 a_2 > 5.47 \ cm^2 \tag{6.20}$$

The total winding usage area is 5.47 cm^2 which is less than the window area of the core so the design perfectly fits.

Several winding configurations have been considered experimentally, in order to achieve the desired value of leakage inductance. If the value of leakage inductance is too low, an additional inductor is required in series to the coupled inductor, increasing complexity of the converter. On the other hand, if the leakage inductance is too high, techniques to minimise leakage inductance can be used, such as changing the winding ratio of primary/secondary windings or interleaved winding of primary/secondary windings. At the first attempt, the most common winding configuration has been used in which the primary winding is wound on one leg and secondary winding is wound on the other leg of the core as shown in figure 6.17. The leakage inductance in this case is 52uH which is higher than the desired values of 25uH. In this winding configuration, the distance between two windings is large which results in high leakage inductance.



Figure 6.17: Windings sequence of the inductor core at the first attempt.

The second and final winding configuration is depicted in figure 6.18. The secondary winding is wound on top of the primary winding for better coupling and reduced leak-age inductance. This winding configuration provided the closest leakage inductance to the desired value, with no need for the investigation of other winding arrangements.

Summary of the coupled inductor characteristics:

- Primary turns ratio: $n_1 = 16$
- Primary copper size: AWG15*4 (in parallel) = 5.8 mm
- Secondary turns ratio: $n_2 = 40$
- Secondary copper size: AWG15 = 1.45 mm
- Magnetising inductance: $L_m = 750 \ \mu H$
- Length of the air gap: $L_{gap} = 2.3 \ mm$



Figure 6.18: Final windings sequence of the inductor core.

The final magnetic components were measured using a LCR bridge analyser (PSM1735 NumetirQ). The measurements are summarised in table 6.5.

	$L_{m,pri} (\mu H)$	$L_{lk,pri}$ (μH)	$L_{m,sec}$ (μH)	$L_{lk,sec}$ (μH)	n	L (μH)
Inductor 1	592.50	1.59	3720.06	10.41	0.40	22.01
Inductor 2	622.41	1.89	3912.34	12.50	0.40	22.91
Inductor 3	640.26	1.79	4025.13	11.56	0.40	25.80
Inductor 4	630.71	2.22	3957.32	14.24	0.40	20.00
Inductor 5	630.87	1.68	3950.17	11.25	0.40	22.10
Inductor 6	651.61	1.63	4085.47	10.94	0.40	22.19

Table 6.5: The measurements of the coupled inductors

where

 $L_{m,pri}$ is the primary indutance μH .

 $L_{lk,pri}$ is the primary leakage indutance μH .

 $L_{m,sec}$ is the primary indutance μH .

 $L_{lk,sec}$ is the secondary leakage indutance μH .

n is the coupled inductor turns ratio.

L is the leakage inductance of the two coupled inductors μH .

6.7 Capacitors Selection

There are two main capacitors in the experimental rig: active clamp capacitor and output capacitor. To select the proper capacitor, the RMS current and the maximum voltage rating need to be calculated.

6.7.1 Active clamp capacitor

The active clamp capacitor is used to recirculate the leakage energy of the coupled inductor and this capacitor is fitted in the PCB board of the half-bridge converter. A film capacitor is selected due to the small equivalent series resistance (ESR) and small equivalent series inductance (ESL), and current handling capability.

The main advantage of film capacitor is low parasitic inductance and low ohmic losses. The internal structure of a film capacitor is layers of dielectric and metal-film electrodes which are directly connected to two terminals (wire leads). This structure keeps the current paths very short and behaves like a large number of individual capacitors connected in parallel which reduces the internal ohmic losses and gives low parasitic inductance.

Therefore, it is suitable for applications such as high surge currents (clamp and snubber), AC power, and high frequency applications. When selecting the capacitor, the main consideration is the RMS current and the maximum voltage rating. The voltage stress and current stress are plotted in figure 6.19. The maximum voltage stress is 141.1V and maximum RMS current is 7.04A. Thus, the KEMET R75IR4470AA50J film capacitor 4.7 uF with voltage rating of 250V are chosen.



Figure 6.19: Voltage and current stress of the clamp capacitor as a function of the input voltage. (Top left) Maximum voltage stress. (Top right) RMS voltage stress. (Botoom left) Maximum current stress (Bottom right) RMS current stress.

6.7.2 Output capacitor

The output capacitor is designed to minimise the peak-to-peak output voltage ripple to less than 4.5% to meet the aircraft standards (MIL-STD-704F). The designed value is 40 uF. The selected output capacitor employs a conductive polymer aluminium electrolytic capacitor. This type of capacitor offers very cost effective, large capacitance per volume, high temperature resistance and high ripple current capability. There are some disadvantages of using this type such as frequency response and leakage current. The equivalent series resistance (ESR) of the capacitor rises with frequency which limits its frequency response typically well below 100 kHz. The voltage and current stress of the output capacitor is plotted in figure 6.20 The maximum voltage stress is 328.2V and the maximum RMS current is 3.5A.

Thus, the capacitor used in this rig is PANASONIC ELECTRONIC COMPONENTS EEUED2G470 capacitor, $47 \ uF$ with rated voltage of 400V.



Figure 6.20: Voltage and current stress of the one of the output capacitors as a function of the input voltage. (Top left) Voltage stress. (Top right) RMS voltage stress. (Bottom left) Current stress (Bottom right) RMS current stress.

6.8 Measurement

In this section, the voltage and current measurement techniques used in the converter are briefly presented. The input coupled inductor current, clamp capacitor voltage and output load voltage are measured for feedback control and fault protection of the IBCI. The LEM LA 55-P and LV 25-P are used for the current and voltage measurement. These two transducers are Hall effect closed loop transducers which have excellent accuracy, good linearity and a wide frequency bandwidth up to 200kHz[65].

6.8.1 Current measurement

To ensure safe operation of the converter, a current transducer, LA 55-P, is used to measure the input inductor current of each coupled inductor to monitor current entering in each interleaved channel. The maximum value of the coupled inductor current allowed for the IBCI is determined by the DSP program. In the event of the current exceeding the safety limit, the DSP automatically disables the switching signals. In addition, this current measurement could be used to add an inner current controller in the converter control architecture.



Figure 6.21: Diagram of current transducer.

In order to use current transducer LA 55-P properly, there are two parameters that need to be designed: number of turns of the primary side and resistor R_M . According to LA 55-P datasheet [65], the measuring range is -70A to 70A and the nominal RMS value of the primary current is 16A. The output from the current transducer has the best accuracy when it operates around the nominal ampere-turn condition. According to 6.16, the maximum current is 300/10=30A, therefore 2 turns are used for the primary side, as shown in figure 6.21. The conversion ratio of the transducer is 1:1000, therefore the secondary current $I_S = 2I_P/1000 = 0.060$ A.

The output signal V_M needs to be smaller than 5V to avoid the saturation of the A/D

conversion of the FPGA board. Hence, the value R_M can be calculated by:

$$V_S = I_S R_M < 5V$$

$$\Rightarrow R_M < \frac{5V}{I_{S(max)}} < 83.33 \ \Omega \tag{6.21}$$

- 7 7

A resistor of 70 Ω is selected for R_{M} .

6.8.2 Voltage measurement

To ensure safe operation of the converter and control purposes, a voltage transducer, LV 25-P, is used to measure the clamp capacitor for hardware trip protection and output voltage of the converter for controlling the desired voltage level.

The Hall effect voltage transducer LV 25-P is used to measure voltage across clamp capacitor and output load. The concept of voltage transducer is similar to current transducer where the measured voltage is converted into current as shown in figure 6.22 where input voltage VP is the voltage to be measured. I_P is the primary current passing though the resistor R_P . I_S is the secondary current and $I_S = 2.5 I_P[64]$. Both R_P and R_M resistors need to be selected properly in order to allow the correct operation of the transducer.



Figure 6.22: Diagram of voltage transducer.

The procedure to select the two resistors for the output voltage transducer is as follows:

Step1: The value of R_P

According to the LV25-P datasheet, the recommended value of I_P is -14mA to 14mA [64]. Hence, to ensure that the value of I_P is in this range, the value of R_P can be selected by:

$$\frac{1.2V_{P(max)}}{R_P} < 14\text{mA}$$

$$\Rightarrow R_P > \frac{1.2V_{P(max)}}{14mA} > 64.3 \text{ k}\Omega \tag{6.22}$$

Where $V_{P(max)}$ is the maximum value of V_P . In this case, it is set to 780V where a 20% safety margin is added.

Hence, a resistor RP 70 k Ω is selected.

Step2: the value of R_M

Like in the current transducer design, the value of R_M is chosen so that the output voltage V_M is smaller than the saturation in the A/D conversion stage 5V. Since, $I_S = 2.5I_P$:

$$I_{M(max)} R_M = 2.5 \ge \frac{1.2V_{P(max)}}{R_P} \ge R_M < 5V$$
$$\Rightarrow R_M < \frac{5 \cdot R_P}{2.5 \cdot 1.2 \cdot V_{P(max)}} < 155.56 \ \Omega \tag{6.23}$$

Hence, a resistor R_M 150 Ω is chosen.

6.9 Control Platform

The control platform for the rig employs a field programmable gate array board (Actel ProASICS A3P1000), digital signal processor (TMS320C6713 DSP) and a Host Port Interface (HPI) daughter card. A photograph of the hardware is shown in 6.23. Figure 6.24 shows the overview block diagram of the control platform.



Figure 6.23: Photograph of the control platform.

The FPGA board used in the converter was originally developed by the PEMC group of the University of Nottingham. The FPGA contains Analogue to Digital(A/D) conversion (up to 10 channels), Input/Output transmission ports (up to 12 ports), data buffers for the data transmission between FPGA and other devices and hardware comparators for over-current or over-voltage protections.

The DSP used in this rig is a Texas Instruments TMS320C6713. It is operating at 225MHz and delivers up to 1350million instruction per second which is suitable for complex calculations. The DSP C6713 DSK is the development platform for the DSP with USB host interfaces for external peripherals and HPI.

The HPI daughter card provides an interface to the Host port interface on the DSP board. It allows a bi-directional data transfer between the host PC and the DSP via serial, parallel or USB access without interrupting the central processor unit.

The overview of the control platform of the converter rig is shown in 6.24.



Figure 6.24: Overview of the control platform.

The measurement signals from the transducers are fed into 14 bit ADCs on the FPGA board which transform the analogue signals into the digital signals and store the converted data into the DSP memory. Then the signals are processed through the DSP board to implement the control strategies, carrier based modulation and switching states selection. The control strategy is written in C language using Code Composer studio. The DSP starts the calculation process upon receiving an interrupt signal from the FPGA corresponding to interrupt frequency of 20kHz. When the DSP finishes the calculation process, the data of the switching state is sent to the FPGA to generate the PWM signal. This will be later sent to the gate drive circuit.

6.10 Conclusions

In this chapter, the hardware design and component selection of the prototype converter has been presented including gate driver, power module, coupled inductors, and capacitors. In addition, the control platform and measurement techniques used in the converter rig have been discussed. Next, the experimental results are presented.

Chapter 7

Experimental results

7.1 Introduction

In this chapter, the experimental results for the converter prototype are presented and compared with the simulation results to validate the proposed converter design and operation. A 3.8 kW prototype (1:10 scaling) of the full-powered converter was built based on the optimal design procedure. The aim of the design was to guarantee operability of the converter over the entire fuel cell characteristic, at the same time ensuring high efficiency at nominal load. The estimated power losses and efficiency of the converter from the simulation are compared to measurements from the prototype rig to confirm the effectiveness of the design procedure and verify the power loss calculation presented in chapter 5.

7.2 Experimental Setup

The experimental setup is shown in figure 7.1. An input voltage DC power supply TDK-Lambda GEN80-187.5 was connected to the to the converter and the output

was connected to a load resistance ranging from 100-470 Ω . The results were collected using a LeCroy wavesurfer 454 500MHZ oscilloscope. LeCroy current probes (CP100 and CP150) were used to measure input inductor current, transfer energy inductance current and output load current to make sure the converter operation is correct. TESTEC SI-51 differential probes were used to measure the clamp capacitor voltage, coupled inductor voltage and output load voltage to verify the converter operation and the voltage doubler rectifier operation.



Figure 7.1: Diagram of the prototype rig setup.

7.3 Experimental Results

All the results obtained from the converter prototype were compared with the PLECS simulation software. The experiment was carried out under open-loop control with a fixed duty cycle calculated from the converter operating curves. The converter proto-type needs to be able to operate under all the conditions of the fuel cell characteristics. Hence, some sample points along the power versus fuel cell stack voltage curves of the fuel cell were selected and tested. The resulting waveforms at start-up load, full load and nominal load of 2kW are presented. Moreover, the converter efficiency at selected points was measured and compared to the analytical power loss calculation.

• Start-up load is a load in which the fuel cell starts to operate. The maximum current is drawn to warm-up the fuel stacks.

The details of the start-up load are as follows:

- Input voltage V_i is 20V.

- Duty cycle D is 0.865.
- Load resistance R_o is 348.8 Ω .
- Voltage conversion ratio (M_D) is 32.5.
- Operating mode is discontinuous current mode.
- Full load is a load corresponding to the maximum power the fuel cell can supply.

The details of the full load condition are as follows:

- Input voltage V_i is 63.5V.
- Duty cycle D is 0.57.
- Load resistance R_o is 113.62 Ω .
- Voltage conversion ratio (M_D) is 10.236.
- Operating mode is discontinuous current mode.
- Nominal load 2kW is the load at which the fuel cell operates at in normal operation (after the fuel cell is warmed-up).

The details of the nominal load are as follows:

- Input voltage V_i is 80V.
- Duty cycle D is 0.418.
- Load resistance R_o is 214.8 Ω .
- Voltage conversion ratio (M_D) is 8.125.
- Operating mode is discontinuous current mode.

7.3.1 Input current

The input current from the voltage supply was measured to validate the design and ensure the input current ripple is lower than 4%. This is an important requirement for fuel cell applications as high input ripple will affect the fuel cell performance and life expectancy. The waveforms obtained from the experimental rig and PLECS simulation (simulation model is shown in Appendix F) were plotted below as well as the calculation of the current ripple percentage.

Start-up load



Figure 7.2: Experimental and simulation results of the input current at start-up load.

Table 7.1: Comparison between experimental and simulation results of input current ripple at start-up load

	Experimental	Simulation
Input current ripple (A)	0.81	0.31
% Input current ripple	1.24	0.48

Full load



Figure 7.3: Experimental and simulation results of the input current at full load.

Table 7.2: Comparison between experimental and simulation results of input current ripple at full load

	Experimental	Simulation
Input current ripple (A)	1.12	0.51
% Input current ripple	1.81	0.83

Nominal load



Figure 7.4: Experimental and simulation results of the input current at nominal load.

Table 7.3: Comparison between experimental and simulation results of input current ripple at nominal load

	Experimental	Simulation
Input current ripple (A)	0.75	0.54
% Input current ripple	2.79	2.03

The experimental and simulation results show good agreement. The experimental input current ripple is slightly higher than the simulation due to the magnetising inductance, current unbalance, and noise. In practice, it is impossible to wind all the coupled inductors to have the same values of magnetising inductance. The current ripple in each interleaving channel is not equal. Hence, the ripple cancellation cannot be achieved as effectively in the simulation. All the results meet the requirement of 4% input current ripple. The highest input ripple current is 2.79% which occurs at nominal load as expected.

7.3.2 Output load voltage and current

The experimental and simulation results of the output load voltage at different output loads are plotted below. The converter needs to boost the input voltage to the desired output voltage level of 650V. Moreover, the zoom in of the output voltage waveform are illustrated to confirm the converter meets the aircraft standard of 4.5% output voltage ripple.

Start-up load



Figure 7.5: Experimental and simulation results of the load voltage at start-up load.



Figure 7.6: Zoom in experimental and simulation results of the load voltage at startup load.

Table 7.4: Comparison between experimental and simulation results of output load voltage and current at start-up load

	Experimental	Simulation
Load voltage ripple (V)	4.2	2.51
% Load voltage ripple	0.65	0.39

Full load



Figure 7.7: Experimental and simulation results of the load voltage at full load.



Figure 7.8: Zoom in experimental and simulation results of the load voltage at full load.

 Table 7.5: Comparison between experimental and simulation results of output load

 voltage at full load

	Experimental	Simulation
Load voltage ripple (V)	6.02	2.72
% Load voltage ripple	0.92	0.42

Nominal load



Figure 7.9: Experimental and simulation results of the load voltage at nominal load.



Figure 7.10: Zoom in experimental and simulation results of the load voltage at nominal load.

 Table 7.6: Comparison between experimental and simulation results of output load

 voltage at nominal load

	Experimental	Simulation
Load voltage ripple (V)	10.80	4.94
% Load voltage ripple	1.66	0.76

The results show good correlation between the experimental waveforms and the PLECS simulation waveforms which validates the converter operation and the modelling in PLECS. The percentage of output voltage ripple is slightly higher in the experimental rig than in simulation due to the noise caused by the parasitic elements. The maximum voltage ripple is 1.66% which is lower than 4.5%. Hence, the converter meets the output voltage ripple specification of the aircraft standards.

7.3.3 Clamp capacitor voltage

In order to verify the converter operation, the clamp capacitor voltage was measured. This capacitor voltage is related to the input voltage by the relation $(V_{CL}=V_i/(1-D))$. The clamp capacitor waveforms at start-up load, full load and nominal load are plotted below. The experimental results show good agreement with the simulation waveforms. The slight discrepancy is due to the switching noise.

Start-up load



Figure 7.11: Experimental and simulation results of the clamp capacitor voltage at start-up load.





Figure 7.12: Experimental and simulation results of the clamp capacitor voltage at full load.

Nominal load



Figure 7.13: Experimental and simulation results of the clamp capacitor voltage at nominal load.

7.3.4 Three level voltage

The sum of two coupled inductor voltages at the secondary winding is a three level voltage V_A which represents the input source to the voltage doubler rectifier. The voltage in this stage should equal to half of the output voltage which is 325 V. The results of all three phases are plotted below at different operating loads. The results show good agreement between the experimental results and simulation results. The voltage in each phase is 325 V as expected. However, there is high ringing around zero. This is caused by the parasitic inductance and leakage inductance together with the parasitic capacitance of the MOSFET device which forms an LC circuit [70]. During the experiments, the gate signal was measured and it had no oscillation. However, the ringing happened at the drain to source voltage and is due to the stray inductance in the switches and PCB. This is because the PCB design wasn't optimised properly which could cause a high stray inductance to exist between the drain and source terminals. Hence, when the MOSFET device is switching, the oscillation occurs. A few small film capacitors were soldered in parallel to the drain to source terminal of the MOSFET devices to minimise the ringing.

Start-up load



Figure 7.14: Experimental results of the three level voltage at start-up load.



Figure 7.15: Simulation results of the three level voltage at start-up load.

Full load



Figure 7.16: Experimental results of the three level voltage at full load.



Figure 7.17: Simulation results of the three level voltage at full load.

Nominal load



Figure 7.18: Experimental results of the three level voltage at nominal load.



Figure 7.19: Simulation results of the three level voltage at nominal load.

7.3.5 Energy transfer inductance current

The energy transfer inductance is one of the main components in the converter which determines the energy transfer from source to load. The energy transfer inductance is the leakage inductance of the coupled inductor. The output waveforms of energy transfer inductance current are plotted at different operating loads.

Start-up load



Figure 7.20: Experimental results of the energy transfer inductance current at startup load.



Figure 7.21: Simulation results of the energy transfer inductance current at start-up load.

Full load



Figure 7.22: Experimental results of the energy transfer inductance current at full load.



Figure 7.23: Simulation results of the energy transfer inductance current at full load.

Nominal load



Figure 7.24: Experimental results of the energy transfer inductance currente at nominal load.



Figure 7.25: Simulation results of the energy transfer inductance current at nominal load.

Overall the experimental waveforms match the PLECS simulation waveforms. However, there is a slight difference between them due to the unbalanced current between each phase. The total leakage inductance in each phase is not exactly 25uH as designed. The results in all three operating points showed that the 2^{nd} phase current had a lower current than other phases which corresponded to the inductance of the energy transfer inductor. As measured in Chapter 6, the 2^{nd} phase energy transfer inductor has lower inductance than the other phases.

7.3.6 Converter efficiency and Loss estimation

This section presents the efficiency of prototype rig at different operating points on the power versus input voltage fuel cell characteristic. The converter efficiency at 6 different operating points along the fuel cell characteristic curve was measured as shown in figure 7.26. The power supply that is used in the experiment can supply a maximum voltage of 80V, hence, the converter was tested up to this point. Moreover, at light load operation, the fuel cell I-V characteristic curve is non-linear and the converter is rarely operated in this region.

The details of each point are summarised in the table 7.7.



Figure 7.26: Power versus fuel cell stacks voltage at reduced power.

	Vin (V)	Iin (A)	Vout (V)	Iout (A)	Load (W)	Power (W)
	20.00	60.00	650.00	1.85	352.08	1200.00
Start-up	49.00	60.00	650.00	4.52	143.71	2940.00
	34.50	60.00	650.00	3.18	204.11	2070.00
Full load	63.50	60.00	650.00	5.86	110.89	3810.00
Nominal load	71.75	43.16	650.00	4.76	136.42	3096.95
	80.80	24.75	650.00	3.08	211.25	2000.00

Table 7.7: Details of selected operating points are used in experiment

The results are compared to the analytical calculations of the converter efficiency based on the power loss modelling in each component that was discussed in Chapter 5. The converter power losses can be divided into two categories; active component power losses and passive component power losses. There are two active components that are used in the IBCI converter; First, MOSFET devices are used in the halfbridge circuit. There are two sources of power losses generated by a MOSFET device which are conduction losses and switching losses. Second, the diode is used in the voltage doubler rectifier to provide a conversion of AC input voltage to DC output voltage. The diode produces two power losses; conduction losses and reverse recovery losses. There are two passive components in IBCI converter which are the coupled inductor and capacitors. The coupled inductor is used to control input current and provide the step-up ability. Core losses and copper losses are generated in the coupled inductor during operation. There are two main capacitors used in the converter which are the active clamp capacitor and output capacitor. The power losses of a capacitor are due to the equivalent series resistance (ESR). All the parameters that related to the power loss calculation are summarised in table 7.8.

Table 7.8: Summary of related parameters used in the loss analysis in reduced power converter

	Parameters		Values	
MOSFET	On resistance	R_{DS}	45	$m\Omega$
IXFN73N30T	Turn-on time	t_{on}	110	nS
	Turn-off time	t_{off}	150	nS
Diode	Forward voltage drop	V_F	1.75	V
DSEI30A	Peak reverse recovery current	I_{RM}	16	A
	Reverse recovery time	t_{rr}	40	nS
Clamp capcitor	Equivalent series resistance	R_{ESR}	0.1	$m\Omega$
KEMET R75IR4470				
Output capacitor	Equivalent series resistance	R_{ESR}	0.04	Ω
EEUED2G470				
Coupled inductor	Copper resistance(AWG 15)	R_{copper}	0.01 (Ω	2/m)

The analytical calculations were performed in MATLAB over all the operating range of the fuel cell characteristics. The results were verified by PLECS simulation at some specific operating points to confirm the calculations. The PLECS simulation can calculate the losses based on the device manufacturer's datasheet at the specific conditions. For example, the on resistance in a MOSFET varies with the operating voltage and current, gate to source voltage, and temperature. The results at start-up load (1.2 kW), full load (3.81 kW) and nominal load (2 kW) will be discussed.

Start-up load



Figure 7.27: Bar chart of all components power losses at start-up load based on analytical calculation.

Figure 7.27 shows the calculated results of all the active and passive components at the start-up load. As shown in the figure, it is clearly seen that the power losses occurring with this load are dominated by the coupled inductor losses. This is because the converter operates at its maximum current to warm-up the fuel cell. The conduction losses on the lower leg MOSFET are also affected by the high current and high duty cycle. The total current flowing through the lower devices is the summation of the input current and the secondary current reflected at the primary side. The upper leg MOSFET has much lower conduction losses because it operates at a lower duty cycle (1-D) than the lower leg MOSFET. Moreover, both the upper and lower MOSFETs benefit from the zero-voltage switching turn-on which reduces the switching losses. The power losses in the output capacitors are a film type capacitors are insignificant. Although the output capacitors have higher equivalent series resistance, the output converter is
high voltage and low current. Thus, the ESR losses in the output capacitors are low.



Figure 7.28: Pie chart of total losses in each component and efficiency of the converter at start-up load.

The total power losses of the converter at start-up load are 168.53W. The losses in each component and the efficiency of the converter are summarised in figure 7.28. The analytical evaluations of the converter efficiency is 85.96%.

Full load



Figure 7.29: Bar chart of active components power losses at full load based on analytical calculation.

Figure 7.29, illustrates the calculated results of all the active components and passive components at full load. The converter operates at the maximum power and maximum input current. The power losses in the coupled inductor dominate the power losses in the other components. This is due to the core losses which are directly proportional to the input current. The power losses in the lower leg MOSFET are much higher than in the upper leg MOSFET because the current that flows through the lower devices is the summation of the input current and the secondary current reflected at the primary side. Both the upper and lower leg MOSFETs are turned on at zero votlage which reduces the switching losses. The power losses in output capacitors and clamp capacitors are relatively small compared to the total power of the converter.



Figure 7.30: Pie chart of total losses in each component and efficiency of the converter at full load.

The total power losses of the converter at full load are 237.74W. The losses in each component and the efficiency of the converter are summarised in figure 7.30. The estimated converter efficiency from the analytical calculations is 93.76%.



Nominal load

Figure 7.31: Bar chart of active components power losses at nominal load based on analytical calculation.

Figure 7.29, presents the calculated results of all the active components and passive components at the nominal load. The coupled inductor power losses are no longer dominant. It is because the input current is reduced linearly from maximum input current after the fuel cells reach full load power. Hence, the input current at nominal load is lower than at the start-up load and full load. At nominal load, the switching loss in the lower leg MOSFET dominates the conduction losses because the MOSFET has lost the zero-voltage switching turn-on. The output current is low so the total current flowing through the MOSFET device during turn on is positive. Hence, the current is flowing from drain to source and the output capacitance of the MOSFET does not discharge before device turn-on. The upper leg MOSFET switching losses are low due to soft-switching turn-on. The power losses in the output capacitors and clamp capacitors are relatively small compared to the power of the converter.



Figure 7.32: Pie chart of total losses in each component and efficiency of the converter at nominal load.

The total power losses of the converter at the nominal load are 97.29W. The losses in each component and the efficiency of the converter are summarised in figure 7.30. The approximate converter efficiency from the analytical calculations is 95.14%.

In the experiment, a precision power analyser (KinetiQ PPA2530 0.04% accuracy) was connected to the input and output of the converter rig to measure the input power and output power. The input current measurement is additionally connected to the external current shunt as the measured current exceeds the current ratings of the power analyser. The input voltage was adjusted in accordance with the output voltage to achieve desired output voltage. The converter was tested at different points along the fuel cell characteristic curve to validate the reliability of the power loss estimation. The details of selected operating points are shown earlier in table 7.7. The analytical approximations of the converter efficiency are shown in table 7.9 and the experimental converter efficiency at different input voltages are shown in table 7.10.

Table 7.9: Analytical approximation of the converter efficiency and power losses at different input voltages

Input voltage (V)	20	34.5	49	63.5	71.75	80.8
Output power (W)	1200	2070	2940	3810	3097	2000
Lower MOSFETs conduction losses	37.26	44.93	48.74	61.45	35.52	14.59
Lower MOSFETs on losses	0.00	0.00	0.00	0.00	5.34	2.92
Lower MOSFETs off losses	13.45	13.32	13.35	13.32	30.61	22.42
Total lower MOSFETs power losses	52.16	60.36	64.41	77.44	71.42	39.13
Upper MOSFETs conduction losses	1.75	3.60	4.58	7.61	7.46	4.70
Upper MOSFETs on losses	0.00	0.00	0.00	0.00	7.26	22.42
Upper MOSFETs off losses	13.45	13.32	13.35	13.32	30.11	3.96
Total upper MOSFETS power losses	16.65	19.03	20.25	23.60	12.02	5.77
Diodes conduction losses	1.48	2.55	3.06	4.69	3.78	2.42
Diode reverse recovery losses	0.16	0.28	0.33	0.51	0.41	0.26
Total diodes power losses	9.82	16.94	20.38	31.18	25.13	16.10
Total active components losses	78.63	96.33	105.04	132.23	108.57	60.99
Coupled inductors core losses	79.16	89.29	92.93	98.52	64.73	34.59
Coupled inductors wire losses	6.12	6.33	6.43	6.60	3.65	1.56
Total coupled inductors power losses	85.27	95.62	99.36	105.12	68.38	36.16
Clamp capacitors ESR losses	0.00	0.00	0.00	0.00	0.00	0.00
Output capacitors ESR losses	0.51	0.55	0.46	0.40	0.28	0.14
Total passive components losses	85.79	96.17	99.82	105.52	68.66	36.30
Total power losses	164.42	192.50	204.86	237.75	177.23	97.29
Converter efficiency	86.30	90.70	93.03	93.76	94.28	95.14

Input voltage (V)	20	34.5	49	63.5	71.75	80
Output power (W)	1182.90	2033.60	2941.10	3666.90	2542.20	1941.40
Input power measurement						
1	1362.2	2238.7	3186.6	3932.9	2726.1	2086.6
2	1362.60	2238.50	3185.90	3932.40	2726.50	2085.90
3	1362.30	2239.10	3186.50	3933.10	2725.90	2086.30
4	1359.80	2238.60	3186.20	3932.90	2726.20	2086.90
5	1363.10	2239.00	3186.90	3932.70	2726.30	2086.40
Average Output power	1362.00	2238.78	3186.42	3932.80	2726.20	2086.42
Practical efficiency	86.85	90.84	92.30	93.24	93.25	93.05
Approximated efficency	86.30	90.70	93.03	93.76	94.28	95.14

Table 7.10: Practical converter efficiency at different input voltages

The 7.10 shows the practical converter efficiency at different input voltages. The output power was measured 5 times and then the values were averaged to ensure the precision of the measurement. The output power from the power analyser was obtained to calculate the efficiency. There is a slight difference in output power from the analytical approximation because the exact output load resistance can not be obtained according to the fuel cell characteristics (Power vs Input voltage curve). Several fixed value of load resistors were used in the experiment to match the required power according to the fuel cell characteristics.

The results from the analytical calculations and experiments are plotted below (converter efficiency versus input voltage).



Figure 7.33: Converter efficiency at different input voltages.

As observed in figure 7.33, the analytical calculation shows a very good approximation of the converter efficiency at start-up load to full load (20V-63.5V). At nominal load, the approximated efficiency derived from analytical calculations is higher than the experimental efficiency. This is due to the equivalent series resistance within MOSFETs and passive components. In addition, at nominal load when the duty cycle is less than 0.5 and with DCM operation, the lower leg MOSFET loses its soft switching turn-on. The current flow in the device is from drain to source so output capacitance in the device does not discharge before switching on. Hence, it operates in hard switching. The switching losses in lower leg MOSFET are now an important factor in the overall converter efficiency. In the experiments, the output power is slightly different from the analytical calculations. This affects the input current as well as the turn-on switching current. Hence, the experimental switching losses are different from the estimated values. The maximum experimental efficiency occurs at the full load(63.5V) 93.27% which is slightly lower than approximated efficiency 93.39% At nominal load (63.5-80V), the converter efficiency remains at 93% level. Therefore, after the fuel cells are warmed-up and stabilised, the converter will operate at approximately 93% efficiency. Although at the start-up load, the converter can only achieve 86%, it is a region that is less significant because the reference fuel cells take 30 seconds from the start-up load to reach the full load.

7.4 Conclusions

In this chapter, experimental results have been presented and compared with the simulation results from PLECS. The output waveforms from the prototype rig for different components showed good correlation to the results obtained from PLECS simulation. This validated the accuracy of the modelling. The three level voltage which is the voltage across two coupled inductors was successfully achieved. In addition, the output voltage was twice that of the three level voltage which confirmed the voltage doubler rectifier operation. Moreover, both the input current ripple and the output voltage ripple had met the input/output ripple requirements. Finally, the experiment rig was able to operate over all the testing points which confirmed the operability over the entire fuel cell characteristics.

The analytical calculation of the converter efficiency was presented. The results showed good agreement to the experimental efficiency, confirming the effectiveness of the design procedure. The converter rig achieved the maximum efficiency 93.28% at full load whereas at nominal load the converter operates at around 93% efficiency. The converter efficiency could be improved by increasing the number of interleaved phases to reduce the current flowing in each device. Furthermore, increasing the coupled inductor core size can reduce the core loss as the magnetic flux in the core is reduced.

Chapter 8

Conclusions and Future Work

8.1 Conclusions

The thesis presents research on a multiphase DC/DC power converter topology for a fuel cell-based auxiliary power unit (APU) system to be used on future more electric aircraft (MEA). The thesis takes into consideration a reference fuel cell used within industry, including its V-I characteristics among other properties, to identify the required operational limitations and constraints necessary for the design of the power converter. Fuel cell applications dictate a fundamental requirement on the input current ripple. The ripple is required to be less than 4% (peak-to-peak) of the input current in order to enhance the fuel cell performance, and significantly increase its lifetime. In addition, the output voltage ripple must also meet the specification for aircraft electric power characteristics (MIL-STD-704F) which serve as a sort of inspiration for this thesis. An appropriate scaling has to be applied to the standards for a high voltage aircraft application which implies that the output voltage ripple has to be less than 4.5% (29.25 peak-to-peak ripple at 650V nominal). Most importantly, the converter has to be operable across the entire fuel cell characteristics.

In this particular application, the very high step-up ratio boost converter must take an input at the lowest fuel cell voltage (20V), and convert it to the desired output at 650V – implying boosting with voltage gain of 32.5. This is the first challenge. Another constraint comes from the maximum input current which is very high at 600A because the fuel cell needs high current to warm-up during its operational start-up.

Conventional boost converters, despite their popularity and simple structure, do not suit the application. Although the conventional boost converter has theoretically infinite voltage gain, in practice, parasitic losses would limit the maximum voltage gain to about 6, leaving a wide margin that needs to be bridged.

There are several techniques that can increase the boost factor such as voltage multiplier cells and coupled inductors. Voltage multiplier cells can increase the boost factor by an amount depending on the number of voltage multiplier cells being used. However, the resulting arrangement has poor voltage regulation and poor current capability which is not suited for high current applications.

The coupled inductor boost converter employs a high turns ratio magnetic component to achieve high voltage gain, but the input current is typically discontinuous making this topology unsuitable for fuel cell applications. Integration of different topologies of DC-DC converters is needed to extend the voltage gain, while also maintaining all required specifications set forth by the application. The characteristics of such an integrated converter topology vary depending on the combination used and the design parameters.

The proposed converter topology is a type of integrated DC-DC converter which combines a current doubler circuit, voltage doubler rectifier, coupled inductor and active clamp. It is called an interleaved boost converter with coupled inductor, or IBCI. The main advantages of this topology include input current ripple cancellation, continuous input current, zero-voltage switching (turn-on) and galvanic isolation. The thesis focuses on a multiphase IBCI converter, an extended version of the single phase IBCI converter by implementing interleaving techniques. The extra phases provide additional gain, increase the overall efficiency, reduce the input current ripple and minimise the size of the passive components – making this an excellent choice for fuel cell-based APU applications.

The IBCI converter was analysed through a series of operating mode identification steps and steady-state analyses for both the single phase IBCI converter and the multiphase IBCI converter. The single component with most significant influence has been identified as the energy transfer inductance (leakage inductance) which is responsible for the delivery of energy being transferred from source to load. In the multiphase IBCI converter, the energy transfer is multiplied by the number of phases, which enables extra voltage gain. Dynamic models, based on a non-linear averaged model and a linearised small signal model, for both single phase and multiphase IBCI, were developed that can be used to derive transfer functions for closed-loop control design (closed-loop control design itself is left as further work). Furthermore, the degrees of freedom in the design were discussed, their ranges examined and their impacts analysed. The design freedoms typically influence the converter efficiency and its operating conditions such as CCM/DCM and soft-switching.

A power loss model for each of the main components was investigated so that analytical calculations can be carried out to approximate the converter efficiency at different operating points. Parameters were optimised during the design process to ensure high efficiency at nominal load. A laboratory-scale prototype converter rated at 3.81 kW was constructed as a proof-of-concept. The prototype, 1/10 scale of the actual converter, provided results that validate the analysis and simulation of the preliminary design.

Testing was performed under open-loop control. Several operating conditions were tested to ensure functionality of the converter across the entire fuel cell characteristic. The prototype achieved both the input current ripple and output voltage ripple requirements, recorded at nominal load as 2.79% and 1.66% respectively. Moreover, the testing at nominal load showed a near "exact" approximation from the start-up load to full load with only 1% discrepancy between the actual data and simulated

results. The prototype converter was able to achieve a maximum efficiency of 93.39% at full load and approximately 93% on average over all the nominal loads. The lowest efficiency was recorded at 86% at the start-up load. Fortunately, this condition will only be met for a few seconds during start-up in the actual application.

8.2 Future Work

The thesis has proven the practicality of the multiphase interleaved boost converter with coupled inductor concept. However, there is still room for improvement and additional research on the following aspects;

- Imbalance current between each phase of the IBCI converter. The results from the experimental rig showed a slight imbalance in current measurement in each phase due to the leakage inductances in each coupled inductor not being sufficiently equally matched. This can be improved by implementing closed-loop current control to distribute the current evenly in each phase.
- The converter efficiency can be further improved by optimising the coupled inductor. During the design process, optimisation was not prioritised on the coupled inductor, because effort was directed at matching the value of leakage inductance to be as close as possible to the required inductance. For future improvement, the coupled inductor can be optimised by increasing the core size, which will reduce the flux density within the magnetic path, resulting in the reduction of core loss.
- Testing the converter with the actual fuel cell will confirm the operability and practicality of the converter over the entire fuel cell characteristic. Although the prototype showed a proof-of-concept, being operable from the start-up load to nominal load conditions, there might be other unforeseen problems that may arise only when the actual fuel cells are being used as the source.

- Constructing a voltage source inverter to convert the DC voltage from the IBCI converter to an AC voltage source, so the entirety of the fuel cell based APU systems can be realised.
- Designing and implementing full closed-loop control from the small signal model.

8.3 Publications

The research reported in this thesis has contributed to the following international conference publications:

- Poster presentation: S. C. Lai, A. Costabeber, J. Clare, P. Wheeler, (2017), "An interleaved boost converter with coupled inductor for fuel cell equipped emergency auxiliary power unit (APU) system" More Electric Aircraft (MEA) conference 2017, Bordeaux, France.
- Pending paper: "An interleaved boost converter with coupled inductor for fuel cell equipped emergency auxiliary power unit (APU) system" at PEMD 2018 (The 9th International Conference on Power Electronics, Machines and Drives).

Appendix A

Normalised unit transformation and current in each interval

The base and normalised quantities used in the circuit analysis are summarised as follows:

Base voltage:	$V_N = V_B$
Base impedance:	$X_L = 2\pi f_{sw} L$
Base current:	$I_N = \frac{V_N}{X_L}$
Base power:	$P_N = \frac{{V_N}^2}{X_L}$
Normalised current:	$j_x = \frac{i_x}{I_N}$
$Normalised \ voltage:$	$u_x = \frac{v_x}{V_N}$
Normalised power:	$\Pi_x = \frac{p_x}{P_N}$

A.1 Continuous current mode (CCM)

Initial current J_0

The current through the energy transfer inductor, which determines the amount of power transferred to the load, can be determined by exploiting the half-wave symmetry of the waveform, i.e. by imposing the condition $J_3 = -J_0$. A complete period of the current is shown in figure A.1(a) and A.1(b).



Figure A.1: Converter waveforms (a) CCM operation when D> ~0.5 (b) CCM operation when D ≤ 0.5

This refers to the energy transfer inductor current at the start of the cycle as shown in figure A.1. The inductor voltage is proportional to the rate of change of current flowing through the inductor:

Time interval 1
$$(0 \le t \le \theta_1)$$
: $i_{L1(t)} = I_{L0} + \frac{V_A + V_B}{2\pi f_{sw}L} \cdot \theta_1$ (A.1)

Time interval 2
$$(\theta_1 \le t \le \theta_2)$$
: $i_{L2(t)} = I_{L1} + \frac{V_A - V_B}{2\pi f_{sw}L} \cdot (\theta_2 - \theta_1)$ (A.2)

Time interval 3 (
$$\theta_2 \le t \le \pi$$
): $i_{L3(t)} = I_{L2} + \frac{0 - V_B}{2\pi f_{sw}L} \cdot (\pi - \theta_2)$ (A.3)

Since the waveform has half-wave symmetry, the current at I_3 is equal to $-I_0$. Hence, re-arranging the above equation we got,

$$2I_{L0} + \frac{2V_B \cdot \theta_1}{2\pi f_{sw}L} + \frac{V_A \cdot \theta_2}{2\pi f_{sw}L} - \frac{V_B \cdot \pi}{2\pi f_{sw}L} = 0$$
(A.4)

Substitute time variables $\theta_1 = \varphi$ and $\theta_2 = \beta$, we had

$$2I_{L0} + \frac{2V_B \cdot \varphi}{2\pi f_{sw}L} + \frac{V_A \cdot \beta}{2\pi f_{sw}L} - \frac{V_B \cdot \pi}{2\pi f_{sw}L} = 0 \tag{A.5}$$

Transforming A.5 into the normalised unit system;

Step 1: Changing variable V_B to base voltage V_N ,

$$2I_{L0} + \frac{2V_N \cdot \varphi}{2\pi f_{sw}L} + \frac{V_A \cdot \beta}{2\pi f_{sw}L} - \frac{V_N \cdot \pi}{2\pi f_{sw}L} = 0$$
(A.6)

Step 2: Substituting the equation with normalised voltage $u_x = \frac{v_x}{V_N}$,

$$2I_{L0} + \frac{2V_N \cdot \varphi}{2\pi f_{sw}L} + \frac{U_A \cdot V_N \beta}{2\pi f_{sw}L} - \frac{V_N \cdot \pi}{2\pi f_{sw}L} = 0$$
(A.7)

Step 3: Changing variable $\frac{V_N}{X_L}$ (where base impedance $X_L = 2\pi f_{sw}L$) to base current I_N ,

$$2I_{L0} + 2I_N\varphi + U_A I_N\beta - I_N\pi = 0 \tag{A.8}$$

Step 4: Substituting the equation with normalised current $j_x = \frac{i_x}{I_N}$, we got

$$2J_0 + 2\varphi + U_A\beta - \pi = 0 \tag{A.9}$$

Re-arranging A.9 and substituting φ , the initial current can be found as

$$J_0 = \frac{\pi}{2} (1 + U_A) \left(\frac{1}{U_A} - \frac{\beta}{\pi} \right)$$
 (A.10)

Peak current J_2

The peak energy transfer inductor current can be calculated the same way as the initial current:

From equation A.3, the peak current can be found since $J_3 = -J_0$ and J_0 has been derived above.

$$I_{L3} = -I_{L0} = I_{L2} + \frac{0 - V_B}{2\pi f_{sw}L} \cdot (\pi - \beta)$$
(A.11)

Transforming A.11 into the normalised unit system;

Step 1: Changing variable V_B to base voltage V_N ,

$$-I_{L0} = I_{L2} + \frac{0 - V_N}{2\pi f_{sw}L} \cdot (\pi - \beta)$$
(A.12)

Step 3: Changing variable $\frac{V_N}{X_L}$ (where base impedance $X_L = 2\pi f_{sw}L$) to base current I_N ,

$$-I_{L0} = I_{L2} - I_N(\pi - \beta)$$
 (A.13)

Step 4: Substituting the equation with normalised current $j_x = \frac{i_x}{I_N}$, we got

$$-J_{L0} = J_{L2} - (\pi - \beta) \tag{A.14}$$

Re-arranging A.14 and substituting J_0 from equation A.10, the initial current can be found as

$$J_{2} = \frac{\pi}{2}(U_{A} - 1)\left(\frac{1}{U_{A}} + \frac{\beta}{\pi}\right)$$
(A.15)

A.2 Discontinuous current mode (DCM)

-Peak current value (J_1) :

The peak energy transfer inductor current J_1 similarly to the CCM case.



Figure A.2: Converter waveforms (a) DCM operation when D> ~0.5 (b) DCM operation when D $\leq ~0.5$

Time interval 1
$$(0 \le t \le \theta_1)$$
: $i_{L1(t)} = 0 + \frac{V_A - V_B}{2\pi f_{sw}L} \cdot \theta_1$ (A.16)

Time interval 2
$$(\theta_1 \le t \le \theta_2)$$
: $i_{L2(t)} = I_{L1} + \frac{0 - V_B}{2\pi f_{sw}L} \cdot (\theta_2 - \theta_1)$ (A.17)

From equation A.17, the peak current J_1 can be found since $\theta_1 = \beta$,

$$I_{L1} = \frac{V_A - V_B}{2\pi f_{sw}L} \cdot \beta \tag{A.18}$$

Transforming A.18 into the normalised unit system;

Step 1: Changing variable V_B to base voltage V_N ,

$$I_{L1} = \frac{V_A \beta}{2\pi f_{sw} L} - \frac{V_N \beta}{2\pi f_{sw} L} \tag{A.19}$$

Step 2: Substituting the equation with normalised voltage $u_x = \frac{v_x}{V_N}$,

$$I_{L1} = \frac{U_A V_N \beta}{2\pi f_{sw} L} - \frac{V_N \beta}{2\pi f_{sw} L} \tag{A.20}$$

Step 3: Changing variable $\frac{V_N}{X_L}$ (where base impedance $X_L = 2\pi f_{sw}L$) to base current I_N ,

$$I_{L1} = U_A I_N \beta - I_N \beta \tag{A.21}$$

Step 4: Substituting the equation with normalised current $j_x = \frac{i_x}{I_N}$, we got

$$J_1 = (U_A - 1)\beta \tag{A.22}$$

Appendix B

Voltage gain for IBCI converter

The voltage gain for a single phase IBCI can be derived by,

CCM operation

The normalised power transferred from source to load as a function of the load resistance is given by,

$$\Pi = \frac{4}{\rho_o} \tag{B.1}$$

The normalised power transferred from source to load for CCM operation is equal to,

$$\Pi_{CCM} = \pi k \left(D - \frac{(1-D)}{4k^2} \right)$$

Hence, the normalised voltage gain for CCM operation can be found as,

$$\frac{4}{\rho_o} = \pi k \left(D - \frac{(1-D)}{4k^2} \right)$$
$$16k^2 \pi D \rho_o - (1-D)\pi \rho_o - 16k = 0$$

Divided k^2 ,

$$16\pi D\rho_o - (1 - D)\pi \rho_o \frac{1}{k^2} - 16\frac{1}{k} = 0$$

Since, M' is equal to (1/k),

$$M^{2}(1 - D)\pi\rho_{o} + 16M^{2} - 16\pi D\rho_{o} = 0$$

Solving quadratic equation, the voltage gain can be found as,

$$M'_{CCM} = \frac{8}{\pi \rho_o (1-D)} \left(-1 + \sqrt{1 + \frac{D(1-D)\pi^2 \rho_o^2}{16}} \right)$$
(B.2)

DCM operation

The power transferred from source to load during DCM operation can be divided into 2 regions; $D \leq 0.5$ and D > 0.5.

When $D \leq 0.5$, the normalised power transferred from source to load during this region is equal to,

$$\Pi_{DCM,D<0.5} = 2\pi k^2 - 2\pi k(1 - D) \tag{B.3}$$

The normalised voltage gain for DCM operation when $D \leq 0.5$ can be found as,

$$\frac{4}{\rho_o} = 2\pi k^2 - 2\pi k (1 - D)$$
$$-\pi k^2 \rho_o + \pi k (1 - D) \rho_o + 2 = 0$$

Divided by k^2 ,

$$-\pi\rho_o + \pi \frac{1}{k}(1 - D)\rho_o + 2\frac{1}{k^2} = 0$$

Since M' is equal to (1/k),

$$2M'^{2} + M'\pi(1 - D)\rho_{o} - \pi\rho_{o} = 0$$

Solving the quadratic equation, the voltage gain can be found as,

$$M'_{DCM,D\leq 0.5} = \frac{\pi\rho_o D^2}{4(1-D)} \left(-1 + \sqrt{1 + \frac{8}{\pi\rho_o D^2}}\right)$$
(B.4)

When D > 0.5, the normalised power transferred from source to load during this region is equal to,

$$\Pi_{DCM,D>0.5} = \frac{2\pi D^2 k^2}{(1-D)^2} - \frac{2\pi D^2 k}{(1-D)}$$
(B.5)

The normalised voltage gain for DCM operation when $D \leq 0.5$ can be found as,

$$\frac{4}{\rho_o} = \frac{2\pi D^2 k^2}{(1-D)^2} - \frac{2\pi D^2 k}{(1-D)}$$
$$\pi D^2 k^2 \rho_o - \pi D^2 (1-D) k \rho_o - 2(1-D)^2 = 0$$

Divided by k^2 ,

$$2\frac{1}{k^2}(1 - D)^2 + \frac{1}{k}\pi D^2(1 - D)\rho_o - \pi D^2\rho_o = 0$$

Since, M' is equal to (1/k),

$$2M'^2(1 - D)^2 + M'\pi D^2(1 - D)\rho_o - \pi D^2\rho_o = 0$$

Solving quadratic equation, the voltage gain can be found as,

$$M'_{DCM,D>0.5} = 4\pi\rho_o(1-D)\left(-1 + \sqrt{1 + \frac{8}{\pi\rho_o(1-D)^2}}\right)$$
(B.6)

Summary:

-CCM operation:

$$M'_{CCM} = \frac{8}{\pi \rho_o (1-D)} \left(-1 + \sqrt{1 + \frac{D(1-D)\pi^2 \rho_o^2}{16}} \right)$$
(B.7)

-DCM operation for D \leq 0.5:

$$M'_{DCM,D\leq 0.5} = \frac{\pi\rho_o D^2}{4(1-D)} \left(-1 + \sqrt{1 + \frac{8}{\pi\rho_o D^2}}\right)$$
(B.8)

-DCM operation for D>0.5:

$$M'_{DCM,D>0.5} = 4\pi\rho_o(1-D)\left(-1 + \sqrt{1 + \frac{8}{\pi\rho_o(1-D)^2}}\right)$$
(B.9)

Appendix C

Clamp capacitor and output capacitor selection

C.1 Clamp capacitor

The clamp capacitor current is given by the following equation,

$$i_{CL} = \left(i_{Lm(peak)} + \frac{i_L}{n}\right) \Big|_{S_{3(on)}}$$
(C.1)

where

 i_L is the energy transfer inductance current, during when the auxiliary switch is on, this can be calculated by

$$i_L = \frac{V_i}{n f_{sw} L} - \frac{(1-D)FV_o}{f_{sw} L}$$
(C.2)

 $i_{Lm(peak)}$ is the peak magnetising current, this can be calculated by,

$$i_{Lm(peak)} = \frac{V_i}{n^2 f_{sw}(1-D)} - \frac{FV_o}{n f_{sw}L}$$
 (C.3)

The clamp capacitor can be found as,

$$Q = CV_o \tag{C.4}$$

$$\Delta Q = C \Delta V_o \tag{C.5}$$

where

 ΔQ is the changing in capacitor's charge

 ΔV_o is the output voltage ripple

The clamp capacitor current is designed at the full load, this point is in DCM with duty cycle higher than 0.5. The clamp capacitor current is plotted below.



Figure C.1: Converter waveforms for magnetising inductance current, energy transfer inductance current, and clamp capacitor current during one switching cycle.

As observed from figure C.1, the magnetising current reaches its peak and starts to decrease linearly when the switch S_3 is on. The clamp capacitor current has a decreasing piecewise linear behaviour and the average current in steady state is zero. The clamp capacitor current zero crossing happens when the switch is conducting. Therefore, the charge delivered to the clamp capacitor is equal to the highlighted area which can be easily calculated as;



Figure C.2: Area under clamp capacitor current curve.

$$Area \ \Delta Q = \int_{\frac{P_o}{2NV_i} + \frac{V_i D}{2L_m f_{sw}}}^0 0 - \left(\frac{y - \frac{P_o}{2NV_i} - \frac{V_i D}{2L_m f_{sw}}}{-\frac{V_i D}{L_m f_{sw}(1 - D)} - \frac{V_i}{n^2 f_{sw}(1 - D)} + \frac{FV_o}{n f_{sw} L}}\right) \ \mathrm{d}y$$

$$= \frac{\frac{y^2}{2} - \frac{P_o}{2NV_i}y - \frac{V_iD}{2L_m f_{sw}}y}{\frac{V_iD}{L_m f_{sw}(1-D)} + \frac{V_i}{n^2 f_{sw}(1-D)} - \frac{FV_o}{nf_{sw}L}} \Big|_{\frac{P_o}{2NV_i} + \frac{V_iD}{2L_m f_{sw}}}^{0}$$

$$= 0 - \frac{\frac{(\frac{P_o}{2NV_i} + \frac{V_iD}{2L_mf_{sw}})^2}{2} - \frac{P_o}{2NV_i}(\frac{P_o}{2NV_i} + \frac{V_iD}{2L_mf_{sw}}) - \frac{V_iD}{2L_mf_{sw}}(\frac{P_o}{2NV_i} + \frac{V_iD}{2L_mf_{sw}})}{\frac{V_iD}{L_mf_{sw}(1-D)} + \frac{V_i}{n^2f_{sw}(1-D)} - \frac{FV_o}{nf_{sw}L}}$$

$$=\frac{\frac{1}{2}\cdot\left(\frac{P_o}{2NV_i}+\frac{V_iD}{2L_mf_{sw}}\right)^2}{\frac{V_iD}{L_mf_{sw}(1-D)}+\frac{V_i}{n^2f_{sw}(1-D)}-\frac{FV_o}{nf_{sw}L}}$$

(C.6)

Thus, the clamp capacitor is equal to,

$$C_{CL} = \frac{(1-D)}{2r_{CL}V_i} \cdot \frac{\left(\frac{P_o}{2NV_i} + \frac{V_iD}{2L_m f_{sw}}\right)^2}{\frac{V_iD}{L_m f_{sw}(1-D)} + \frac{V_i}{n^2 f_{sw}(1-D)} - \frac{FV_o}{nf_{sw}L}}$$
(C.7)

C.2 Output capacitor

The output capacitor current can be derived from figure C.3 which is the output side of the converter (voltage doubler rectifier).

When applying the Kirchhoff current law, the capacitor current can be calculated by,



$$i_{Co1} = i_D - i_o \tag{C.8}$$

Figure C.3: Voltage doubler rectifier circuit.

The converter waveforms at full load condition are plotted in figure C.4. It is in DCM mode and duty cycle over 0.5.



Figure C.4: Converter waveforms for energy transfer inductance current, diode current, and output capacitor current during one switching cycle.

The average capacitor current in steady state is zero. Hence, the charge variation is equal to the highlighted area under the curve of the capacitor current which is given by,

$$\Delta Q = C \Delta V \tag{C.9}$$

The capacitor current is shown in figure C.5 under the curve in the highlighted area.



Figure C.5: Area under output capacitor current curve.

Highlighted area can be calculated by using integration,

Area
$$\Delta Q = \int_{I_1-I_0}^0 \frac{y+I_0}{I_1} \beta - \left(\frac{y+I_0}{I_1}(\beta-\pi+\alpha)+\pi-\alpha\right) dy$$

$$= \frac{y^2}{2I_1} \beta + \frac{yI_0}{I_1} \beta - \frac{y^2}{2I_1}(\beta-\pi+\alpha) - \frac{yI_0}{I_1}(\beta-\pi+\alpha) - \pi y + \alpha y \Big|_{I_1-I_0}^0$$

$$= \frac{-(I_1-I_0)^2 \beta - 2(I_1-I_0)I_0 \beta + (I_1-I_0)^2 (\beta-\pi+\alpha) + 2(I_1-I_0)I_0 (\beta-\pi+\alpha)}{2I_1}$$

$$+ \frac{2(I_1-I_0)I_1 \pi - 2(I_1-I_0)I_1 \alpha}{2I_1}$$

$$= \frac{I_1^2 (\pi-\alpha) - 2(I_1-I_0)(\pi-\alpha) + I_0^2 (\pi-\alpha)}{2I_1}$$

(C.10)

Recalling I_1 , I_o and $(\pi - \beta)$,

$$I_1 = \frac{V_i}{nf_{sw}L} - \frac{(1-D)FV_o}{f_{sw}L}$$

 $I_o = \frac{V_o}{R_o}$

$$(\pi - \beta) = \frac{V_i}{n f_{sw} F V_o}$$

Therefore, the value of output capacitor can be found by,

$$C_{o} = \frac{V_{i}}{2r_{co}FV_{o}^{2}} \cdot \frac{\left(\frac{V_{i}}{nf_{sw}L} - \frac{(1-D)FV_{o}}{f_{sw}L} - \frac{V_{o}}{R_{o}}\right)^{2}}{\left(\frac{V_{i}}{L} - \frac{n(1-D)FV_{o}}{L}\right)}$$
(C.11)

Appendix D

Coupled inductor area product

To select an appropriate core frequently involves a trial-and-error type of calculation, here a simplified method of selecting the magnetic core is introduced. The inductor energy handling capability is related to the magnetic core area product (A_P) which is the product of available core window area (W_A) and effective core cross-sectional area (A_C) . In designing the coupled inductor, the total energy (E_t) is an important parameter as it has to be designed to accommodate both the primary energy (E_1) and secondary energy (E_2) .

The total energy can be found by,

$$E_t = E_i + E_o \tag{D.1}$$

The primary turns ratio can be expressed using Faraday's law,

$$N_1 = \frac{I_{Lm}L_m}{B_{max}A_C} \tag{D.2}$$

The winding area of a coupled inductor is fully utilized when,

$$K_u W_A = n_1 a_1 + n_2 a_2 \tag{D.3}$$

where

 a_1 and a_2 are the cross-sectional area for primary winding and secondary winding

 (cm^2) , respectively.

 K_u is the window utilisation factor

The cross-sectional area of winding is given by,

$$a = \frac{I}{J} \tag{D.4}$$

where

J is the current density A/cm^2 .

From equation D.3 and D.4, the winding area of a coupled inductor can be rewritten by, (L)

$$K_u W_A = n_1 \left(\frac{I_1}{J}\right) + n_2 \left(\frac{I_2}{J}\right) \tag{D.5}$$

Substituing in equation D.2,

$$K_u W_A = \frac{I_{Lm1}^2 L_{m1}}{BA_C J} + \frac{I_{Lm2}^2 L_{m2}}{BA_C J}$$
(D.6)

Since the energy of the inductor is given by,

$$E = \frac{LI^2}{2} \tag{D.7}$$

Thus, the energy handling capability of the coupled inductor can be calculated by,

$$A_P = \frac{2E_t}{K_u BJ} \tag{D.8}$$

Appendix E

Coding for MATLAB

E.1 MATLAB Codes for IBCI converter

E.1.1 Plot all waveforms in IBCI converter

% Plot all waveforms in 3 phase IBCI converter function [Vx,Vy,Ix,Iy] = VIwaveFormVin(Vin,n,Fsw,Llk,Lin)

```
Vout = 650;

G = Vout/Vin;

% Calculating Power if Vin;= 63.5

power = 600*Vin;

elseif Vin;= 88

power = ((-20.408*Vin)+1895.904)*Vin;

else

power = (-0.053*Vin<sup>2</sup> + 5.758*Vin + 7.926)*Vin;

end

R = (Vout^2)/power;
```

% Find operating points

$$\begin{split} [d,g,r] &= outputR(R,n,Fsw,Llk);\\ iNan &= find(isnan(g));\\ g(iNan) &= [];\\ d(iNan) &= [];\\ r(iNan) &= []; \end{split}$$

D = interp1(g,d,G);region = interp1(g,r,G,'nearest');

D G region power R

%Find voltage and current in each component

[Vx,Vy] = VwaveFormLin(D,G,region,n,Fsw,Llk);
[Vx2,Vy2] = VwaveFormMos1(D,G,region,n,Fsw,Llk);
[Vx3,Vy3] = VwaveFormMos2(D,G,region,n,Fsw,Llk);
[Vx5,Vy5] = VwaveFormD1(D,G,region,n,Fsw,Llk);
[Vx6,Vy6] = VwaveFormD2(D,G,region,n,Fsw,Llk);

[Ix,Iy] = IwaveFormIlin(D,G,region,power,n,Fsw,Llk,Lin);
[Ix2,Iy2] = IwaveFormImos1(D,G,region,power,n,Fsw,Llk,Lin);
[Ix3,Iy3] = IwaveFormImos2(D,G,region,power,n,Fsw,Llk,Lin);
[Ix4,Iy4] = IwaveFormIcl(D,G,region,power,n,Fsw,Llk,Lin);
[Ix5,Iy5] = IwaveFormId1(D,G,region,n,Fsw,Llk);
[Ix6,Iy6] = IwaveFormId2(D,G,region,n,Fsw,Llk);
[Ix7,Iy7] = IwaveFormIcout(D,G,region,power,n,Fsw,Llk);
[Ix8,Iy8] = IwaveFormIlk(D,G,region,n,Fsw,Llk);
%Figure waveforms figure subplot(8,2,1); plot(Vx,Vy); xlim([0 max(Vx)]); title('Input inductor voltage waveform');

subplot(8,2,2); plot(Ix,Iy); xlim([0 max(Ix)]); title('Input inductor current waveform');

subplot(8,2,3); plot(Vx2,Vy2); xlim([0 max(Vx2)]); title('Device1 voltage waveform');

```
subplot(8,2,4);
plot(Ix2,Iy2);
xlim([0 max(Ix2)]);;
title('Device1 current waveform');
```

```
subplot(8,2,5);
plot(Vx3,Vy3);
xlim([0 max(Vx3)]);
title('Device2 voltage waveform');
```

subplot(8,2,6); plot(Ix3,Iy3); xlim([0 max(Ix3)]); title('Device2 current waveform');

subplot(8,2,7);
plot(Vx5,Vy5);

xlim([0 max(Vx5)]); title('Diode1 voltage waveform');

```
subplot(8,2,8);
plot(Ix5,Iy5);
xlim([0 max(Ix5)]);
title('Diode1 current waveform');
```

subplot(8,2,9); plot(Vx6,Vy6); xlim([0 max(Vx6)]);

```
title('Diode2 voltage waveform');
subplot(8,2,10);
plot(Ix6,Iy6);
xlim([0 max(Ix6)]);
title('Diode2 current waveform');
```

```
subplot(8,2,11);
plot(Ix4,Iy4);
xlim([0 max(Ix4)]);
title('Clamp current waveform');
```

```
subplot(8,2,12);
plot(Ix7,Iy7);
xlim([0 max(Ix7)]);
title('Output capacitor current waveform');
```

```
subplot(8,2,13);
plot (Ix8,Iy8);
xlim([0 max(Ix8)]);
title('Leakage current waveform');
```

RMS (Vx2,Vy2); RMS (Ix2,Iy2); RMS (Ix3,Iy3); end

E.1.2 Plot inductor waveforms

Coupled inductor voltage

 $\label{eq:constraint} \begin{array}{l} \mbox{function [Vx,Vy] = VwaveFormLin(D,G,region,n,Fsw,Llk) } \\ \mbox{\%Coupled inductor voltage} \end{array}$

Vout = 650;F = 0.5;

w=2*pi*Fsw; k = 2*n/G; cm = region; % 0: ccm % 1: dcm1 % 2: dcm2 alpha = []; beta = []; Vmax = []; Vx = []; Vy = []; Vy = []; Vmax = Vout/G;duty= 2*pi*(1-D); Vx = [0; duty; duty+.00001; 2*pi];Vy = [-Vmax; -Vmax; Vmax; Vmax];end

Coupled inductor current

function [Ix,Iy] = IwaveFormIlin(D,G,region,power,n,Fsw,Llk,Lin) %Coupled inductor current

Vout = 650;F = 0.5;w=2*pi*Fsw;Llk=Llk; Lin=Lin; k = 2*n/G;cm = region;% 0: ccm % 1: dcm1 % 2: dcm2 Vin = Vout/G;normFactor = Vout*F/(w*Llk);Iin = power/Vin; $duty = 2^* pi^*(D);$ j0 = [];j1 = [];j2 = [];i0 = [];i1 = [];i2 = [];i3 = [];i4 = [];

```
alpha = [];

beta = [];

Ix = [];

Iy = [];

i0 = (-(Vin/Lin)*(D*1/Fsw)/2)-(Iin/6);

i1 = ((Vin/Lin)*(D*1/Fsw)/2)-(Iin/6);

Iy = [abs(i1); abs(i0); abs(i1)];

Ix = [0; duty; 2*pi];

end
```

E.1.3 Lower leg MOSFET waveforms

Lower leg MOSFET voltage

function [Vx,Vy] = VwaveFormMos1(D,G,region,n,Fsw,Llk) %Lower leg MOSFET voltage

Vout = 650; F = 0.5; w=2*pi*Fsw; k = 2*n/G; cm = region; % 0: ccm % 1: dcm1 % 2: dcm2 normFactor = Vout*F/(w*Llk); j2 = [];alpha = []; beta = []; Vmax = [];

Vx = [];Vy = [];

Vmax = (Vout/G)/(1-D); duty = 2*pi*(D);

Vx = [0; duty; duty+.00001; 2*pi];Vy = [0; 0; Vmax; Vmax];end

Lower leg MOSFET current

function [Ix,Iy] = IwaveFormImos1(D,G,region,power,n,Fsw,Llk,Lin) %Lower leg MOSFET current

```
Vout = 650;

F = 0.5;

w=2*pi*Fsw;

Lin = Lin;

k = 2*n/G;

cm = region;

% 0: ccm

% 1: dcm1

% 2: dcm2

Vin = Vout/G;

normFactor = Vout*F/(w*Llk);

Iin= power/Vin;
```

$$\begin{split} j0 &= []; \\ j1 &= []; \\ j2 &= []; \\ i0 &= []; \\ i1 &= []; \\ i2 &= []; \\ i3 &= []; \\ i4 &= []; \\ alpha &= []; \\ beta &= []; \\ duty &= 2*pi*(1-D); \\ Ix &= []; \\ Iy &= []; \end{split}$$

%Check condition CCM/DCM operation if $D \le 0.5$ j0 = pi/2* (1+k/(1-D)) * ((1-D)/k - 2*D); j1 = 2*pi*D * (k/(1-D)-1); j2 = pi/2 * (k/(1-D) - 1) * ((1-D)/k + 2*D); beta = 2*pi*D;

$$\label{eq:cm} \begin{split} & if(cm == 0) \\ & alpha = pi/2^* \; (2^*D \; - \; (1\text{-}D)/k); \\ & else \\ & alpha = pi^*(1\text{-}(2^*k^*D/(1\text{-}D))); \\ & end \end{split}$$

else

j0 = pi/2 * (1/k-2) * (1+k-D); j1 = 2*pi * (1-D) * (k/(1-D)-1);j2 = pi/2 * (1/k + 2) * (-1+k+D);

```
beta = 2*pi*(1-D);
if cm == 0
alpha = pi/2 * (1-D) * (2 - 1/k);
else
alpha = pi * (1-2*k);
end
end
if cm == 0
if D>0.5
i0 = (-j2*n*normFactor) + (Iin/6) - ((Vin/Lin)*(D*1/Fsw)/2);
i1 = (i0*n*normFactor) + (Iin/6) - ((Vin/Lin)*(D*1/Fsw/2)) +
((Vin/Lin)^{*}(D^{*}1/Fsw)^{*}(pi-beta)/(2^{*}pi^{*}D));
i2 = (Iin/6) - ((Vin/Lin)*(D*1/Fsw/2)) + ((Vin/Lin)*(D*1/Fsw)*(pi-beta)/(2*pi*D)) + ((Vin/Lin)*(D*1/Fsw)*(D*1/Fsw)*(D*1/Fsw)*(D*1/Fsw)*(D*1/Fsw)*(D*1/Fsw)*(D*1/Fsw)*(D*1/Fsw)*(D*1/Fsw)*(D*1/Fsw)*(D*1/Fsw)*(D*1/Fsw)*(D*1/Fsw)*(D*1/Fsw)*(D*1/Fsw)*(D*1/Fsw)*(D*1/Fsw)*(D*1/Fsw)*(D*1/Fsw)*(D*1/Fsw)*(D*1/Fsw)*(D*1/Fsw)*(D*1/Fsw)*(D*1/Fsw)*(D*1/Fsw)*(D*1/Fsw)*(D*1/Fsw)*(D*1/Fsw)*(D*1/Fsw)*(D*1/Fsw)*(D*1/Fsw)*(D*1/Fsw)*(D*1/Fsw)*(D*1/Fsw)*(D*1/Fsw)*(D*1/Fsw)*(D*1/Fsw)*(D*1/Fsw)*(D*1/Fsw)*(D*1/Fsw)*(D*1/Fsw)*(D*1/Fsw)*(D*1/Fsw)*(D*1/Fsw)*(D*1/Fsw)*(D*1/Fsw)*(D*1/Fsw)*(D*1/Fsw)*(D*1/Fsw)*(D*1/Fsw)*(D*1/Fsw)*(D*1/Fsw)*(D*1/Fsw)*(D*1/Fsw)*(D*1/Fsw)*(D*1/Fsw)*(D*1/Fsw)*(D*1/Fsw)*(D*1/Fsw)*(D*1/Fsw)*(D*1/Fsw)*(D*1/Fsw)*(D*1/Fsw)*(D*1/Fsw)*(D*1/Fsw)*(D*1/Fsw)*(D*1/Fsw)*(D*1/Fsw)*(D*1/Fsw)*(D*1/Fsw)*(D*1/Fsw)*(D*1/Fsw)*(D*1/Fsw)*(D*1/Fsw)*(D*1/Fsw)*(D*1/Fsw)*(D*1/Fsw)*(D*1/Fsw)*(D*1/Fsw)*(D*1/Fsw)*(D*1/Fsw)*(D*1/Fsw)*(D*1/Fsw)*(D*1/Fsw)*(D*1/Fsw)*(D*1/Fsw)*(D*1/Fsw)*(D*1/Fsw)*(D*1/Fsw)*(D*1/Fsw)*(D*1/Fsw)*(D*1/Fsw)*(D*1/Fsw)*(D*1/Fsw)*(D*1/Fsw)*(D*1/Fsw)*(D*1/Fsw)*(D*1/Fsw)*(D*1/Fsw)*(D*1/Fsw)*(D*1/Fsw)*(D*1/Fsw)*(D*1/Fsw)*(D*1/Fsw)*(D*1/Fsw)*(D*1/Fsw)*(D*1/Fsw)*(D*1/Fsw)*(D*1/Fsw)*(D*1/Fsw)*(D*1/Fsw)*(D*1/Fsw)*(D*1/Fsw)*(D*1/Fsw)*(D*1/Fsw)*(D*1/Fsw)*(D*1/Fsw)*(D*1/Fsw)*(D*1/Fsw)*(D*1/Fsw)*(D*1/Fsw)*(D*1/Fsw)*(D*1/Fsw)*(D*1/Fsw)*(D*1/Fsw)*(D*1/Fsw)*(
((Vin/Lin)^*(D^*1/Fsw)^*(alpha)/(2^*pi^*D));
i3 = (j2*n*normFactor) + (Iin/6) - ((Vin/Lin)*(D*1/Fsw/2)) +
((Vin/Lin)^{*}(D^{*}1/Fsw)^{*}(pi)/(2^{*}pi^{*}D));
i4 = (-j0*n*normFactor) + (Iin/6) + ((Vin/Lin)*(D*1/Fsw)/2);
I_{V} = [i0; i1; i2; i3; i4; 0; 0];
Ix = [0; pi-beta; pi-beta+alpha; pi; 2*pi-duty; 2*pi-duty+0.01; 2*pi];
else
i0 = (j0*n*normFactor) + (Iin/6) - ((Vin/Lin)*(D*1/Fsw)/2);
i1 = ((Iin/6) - ((Vin/Lin)*(D*1/Fsw/2))) + ((Vin/Lin)*(D*1/Fsw)*alpha/(2*pi*D));
i2 = (-j2*n*normFactor) - (Iin/6) - ((Vin/Lin)*(D*1/Fsw)/2);
Iy = [i0; i1; -i2; 0; 0];
Ix = [0; alpha; 2*pi*D; 2*pi*D+0.01; 2*pi];
```

```
end
else
```

if Dgeq0.5

$$\begin{aligned} & \text{duty} = 2^* \text{pi}^*(\text{D}); \\ & \text{i0} = (-j1^* \text{normFactor}^*\text{n}) - (-(\text{Iin}/6) + ((\text{Vin}/\text{Lin})^*(\text{D}^*1/\text{Fsw}/2))); \\ & \text{i1} = ((\text{Iin}/6) - ((\text{Vin}/\text{Lin})^*(\text{D}^*1/\text{Fsw}/2))) + ((\text{Vin}/\text{Lin})^*(\text{D}^*1/\text{Fsw})^*(\text{pi-beta-alpha})/\text{duty}); \\ & \text{i2} = ((\text{Iin}/6) - ((\text{Vin}/\text{Lin})^*(\text{D}^*1/\text{Fsw}/2))) + ((\text{Vin}/\text{Lin})^*(\text{D}^*1/\text{Fsw})^*(\text{pi-beta})/\text{duty}); \\ & \text{i3} = ((\text{Iin}/6) - ((\text{Vin}/\text{Lin})^*(\text{D}^*1/\text{Fsw}/2))) + ((\text{Vin}/\text{Lin})^*(\text{D}^*1/\text{Fsw})^*(\text{pi})/\text{duty}) + (j1^* \text{normFactor}^*\text{n}); \\ & \text{i4} = ((\text{Iin}/6) - ((\text{Vin}/\text{Lin})^*(\text{D}^*1/\text{Fsw}/2))) + ((\text{Vin}/\text{Lin})^*(\text{D}^*1/\text{Fsw})^*((2^*\text{pi-beta-alpha})/\text{duty})); \\ & \text{i5} = ((\text{Vin}/\text{Lin})^*(\text{D}^*1/\text{Fsw}/2) + (\text{Iin}/6); \end{aligned}$$

$$\begin{split} Iy &= [i0; i1; i2; i3; i4; i5;0; 0]; \\ Ix &= [0; pi-beta-alpha; pi-beta; pi; 2*pi-beta-alpha; 2*pi-beta; 2*pi-beta+0.01; 2*pi]; \end{split}$$

```
else

duty = 2*pi*(D);

i0 = (Iin/6)-((Vin/Lin)*(D*1/Fsw)/2);

i1 = (Iin/6)+((Vin/Lin)*(D*1/Fsw)/2)+(j1*normFactor*n);

Iy = [i0; i1; 0; 0];

Ix = [0; duty; duty+0.01; 2*pi];

end

end

end
```

E.1.4 Upper leg MOSFET waveforms

Upper leg MOSFET voltage function [Vx,Vy] = VwaveFormMos2(D,G,region,n,Fsw,Llk) %upper leg MOSFET voltage

Vout = 650; F = 0.5; w=2*pi*Fsw; k = 2*n/G; cm = region; % 0: ccm % 1: dcm1 % 2: dcm2

normFactor = Vout*F/(w*Llk);

j0 = []; j1 = []; j2 = []; alpha = []; beta = []; Vmax = []; Vx = [];Vy = [];

Vmax = (Vout/G)/(1-D);duty= 2*pi*(D);

Vx = [0; duty; duty+.00001; 2*pi];Vy = [Vmax; Vmax; 0; 0];end

Upper leg MOSFET current

function [Ix,Iy] = IwaveFormImos2(D,G,region,power,n,Fsw,Llk,Lin) %Upper leg MOSFET current

Vout = 650;F = 0.5;

w=2*pi*Fsw;k = 2*n/G;cm = region;% 0: ccm % 1: dcm1 % 2: dcm2 Vin = Vout/G;normFactor = Vout*F/(w*Llk);Iin = power/Vin;j0 = [];j1 = [];j2 = [];i0 = [];i1 = [];i2 = [];i3 = [];i4 = [];alpha = [];beta = []; $duty = 2^* pi^*(D);$ Ix = [];Iy = [];if $D \le 0.5$ j0 = pi/2* (1+k/(1-D)) * ((1-D)/k - 2*D); j1 = 2*pi*D * (k/(1-D)-1);j2 = pi/2 * (k/(1-D) - 1) * ((1-D)/k + 2*D);beta = 2*pi*D;if(cm == 0)

```
alpha = pi/2^* (2^*D - (1-D)/k);
 else
alpha = pi^*(1-(2^*k^*D/(1-D)));
end
else
j0 = pi/2 * (1/k-2) * (1+k-D);
j1 = 2*pi * (1-D) * (k/(1-D)-1);
j2 = pi/2 * (1/k + 2) * (-1+k+D);
beta = 2*pi*(1-D);
if cm == 0
 alpha = pi/2 * (1-D) * (2 - 1/k);
 else
 alpha = pi * (1-2*k);
 end
 end
if cm == 0
if D \ge 0.5
i0 = (j0*n*normFactor) - (Iin/6) - ((Vin/Lin)*(D*1/Fsw)/2);
i1 = (-(Vin/Lin)^*(D^*1/Fsw)/2) - (Iin/6) + ((2^*pi-beta+alpha-duty)/2) - (Iin/6) + 
(2*pi*(1-D))*(Vin/Lin)*(D*1/Fsw));
i2 = (-i2*n*normFactor) + (((Iin/6)-((Vin/Lin)*(D*1/Fsw)/2)));
Iy = [0; 0; i0; i1; -i2];
Ix = [0; \text{ duty}; \text{ duty}+0.01; 2*\text{pi-beta+alpha}; 2*\text{pi}];
```

else

 $\begin{aligned} &((Vin/Lin)^*(D^*1/Fsw)^*(pi-beta+alpha)/(2^*pi^*(1-D)));\\ &i3=(j2^*n^*normFactor)-((((Iin/6)+((Vin/Lin)^*(D^*1/Fsw)/2)))+\\ &((Vin/Lin)^*(D^*1/Fsw)^*(pi)/(2^*pi^*(1-D)));\\ &i4=(-j0^*n^*normFactor)-(Iin/6)+((Vin/Lin)^*(D^*1/Fsw)/2); \end{aligned}$

```
\begin{split} Iy &= [0;\,0;\,i0;\,i1;\,i2;\,i3;\,i4];\\ Ix &= [0;\,duty;\,duty{+}0.01;\,pi;\,pi{+}alpha;\,2^{*}pi{-}(pi{-}beta);\,2^{*}pi];\\ end \end{split}
```

else

if $D \ge 0.5$ i0 = (-(Vin/Lin)*(D*1/Fsw)/2)-(Iin/6); i1 = ((Vin/Lin)*(D*1/Fsw)/2)-(Iin/6)+(j1*normFactor*n);

```
\begin{split} &Iy = [0; 0; i0; i1]; \\ &Ix = [0; duty; duty+0.01; 2*pi]; \\ &else \\ &i0 = (Iin/6) + ((Vin/Lin)*(D*1/Fsw)/2) + (j1*normFactor*n); \\ &i1 = (-(Vin/Lin)*(D*1/Fsw)/2) - (Iin/6) + ((pi-alpha-duty)/(2*pi*(1-D))*(Vin/Lin)*(D*1/Fsw)); \\ &i2 = i1 + ((alpha)/(2*pi*(1-D))*(Vin/Lin)*(D*1/Fsw)); \\ &i3 = (j1*normFactor*n) + ((-(Vin/Lin)*(D*1/Fsw)/2) - (Iin/6) + ((pi)/(2*pi*(1-D))*(Vin/Lin)*(D*1/Fsw))); \\ &i4 = ((Vin/Lin)*(D*1/Fsw)/2) - (Iin/6); \end{split}
```

```
\begin{split} Iy &= [0; \ 0; \ -i0; \ i1; \ i2; \ i3; \ i4; \ i4]; \\ Ix &= [0; \ duty; \ duty + 0.01; \ pi-alpha; \ pi; \ pi+beta; \ 2*pi-alpha; \ 2*pi]; \\ end \\ end \\ end \end{split}
```

E.1.5 Clamp capacitor waveforms

Clamp capacitor current

```
Vout = 650;
F = 0.5;
w=2*pi*f;
\operatorname{Lin} = \operatorname{Lin};
k = 2*n/G;
cm = region;
% 0: ccm
% 1: dcm1
% 2: dcm2
Vin = Vout/G;
normFactor = Vout*F/(w*Llk);
Iin= power/Vin;
j0 = [];
j1 = [];
j2 = [];
i0 = [];
i1 = [];
i2 = [];
i3 = [];
i4 = [];
alpha = [];
beta = [];
duty = 2^* pi^*(D);
Ix = [];
```

$$Iy = [];$$

if D leq 0.5
$$j0 = pi/2* (1+k/(1-D)) * ((1-D)/k - 2*D);$$

$$j1 = 2*pi*D * (k/(1-D)-1);$$

$$j2 = pi/2 * (k/(1-D) - 1) * ((1-D)/k + 2*D);$$

beta = 2*pi*D;

$$\label{eq:cm} \begin{split} & if(cm == 0) \\ & alpha = pi/2^* \; (2^*D \; - \; (1\text{-}D)/k); \\ & else \\ & alpha = pi^*(1\text{-}(2^*k^*D/(1\text{-}D))); \\ & end \end{split}$$

else

$$\begin{split} j0 &= pi/2 * (1/k-2) * (1+k-D); \\ j1 &= 2*pi * (1-D) * (k/(1-D)-1); \\ j2 &= pi/2 * (1/k+2) * (-1+k+D); \\ beta &= 2*pi*(1-D); \end{split}$$

if cm == 0 alpha = pi/2 * (1-D) * (2 - 1/k); else alpha = pi * (1-2*k);end

 end

if cm == 0

if D ${\geq}0.5$

 $i1 = (-(Vin/Lin)^{*}(D^{*}1/f)/2) - (Iin/6) + ((2^{*}pi-beta+alpha-duty)/(2^{*}pi^{*}(1-D))^{*}(Vin/Lin)^{*}(D^{*}1/f));$ $i2 = (j2^{*}n^{*}normFactor) - ((Iin/6) - ((Vin/Lin)^{*}(D^{*}1/f)/2));$

Iy = [0; 0; -i0; i1 ; i2];Ix = [0; duty; duty+0.0001; 2*pi-beta+alpha; 2*pi];

else

$$\begin{split} &\text{i0} = (-j2^*n^*\text{normFactor}) - (((\text{Iin}/6) + ((\text{Vin}/\text{Lin})^*(\text{D}^*1/f)/2))); \\ &\text{i1} = (j0^*n^*\text{normFactor}) - ((((\text{Iin}/6) + ((\text{Vin}/\text{Lin})^*(\text{D}^*1/f)/2))) + ((\text{Vin}/\text{Lin})^*(\text{D}^*1/f)^*(\text{pi-beta})/(2^*\text{pi}^*(1\text{-D}))); \\ &\text{i2} = -((((\text{Iin}/6) + ((\text{Vin}/\text{Lin})^*(\text{D}^*1/f)/2))) + (((\text{Vin}/\text{Lin})^*(\text{D}^*1/f)^*(\text{pi-beta} + \text{alpha})/(2^*\text{pi}^*(1\text{-D}))); \\ &\text{i3} = (j2^*n^*\text{normFactor}) - ((((\text{Iin}/6) + ((\text{Vin}/\text{Lin})^*(\text{D}^*1/f)/2))) + (((\text{Vin}/\text{Lin})^*(\text{D}^*1/f)^*(\text{pi})/(2^*\text{pi}^*(1\text{-D}))); \\ &\text{i4} = (-j0^*n^*\text{normFactor}) - (((\text{Iin}/6) + (((\text{Vin}/\text{Lin})^*(\text{D}^*1/f)/2)); \\ \end{split}$$

Iy = [0; 0; -i0; -i1; -i2; -i3; -i4];Ix = [0; duty; duty+0.0001; pi; pi+alpha; 2*pi-(pi-beta); 2*pi];

end

else

if D ${\geq}0.5$

$$\begin{split} &i0 = (-(Vin/Lin)^*(D^*1/f)/2) - (Iin/6); \\ &i1 = ((Vin/Lin)^*(D^*1/f)/2) - (Iin/6) + (j1^*normFactor^*n); \end{split}$$

$$Iy = [0; 0; -i0; -i1];$$

Ix = [0; duty; duty+0.0001; 2*pi];

else

$$\begin{split} &i0 = (Iin/6) + ((Vin/Lin)^*(D^*1/f)/2) + (j1^*normFactor^*n); \\ &i1 = (-(Vin/Lin)^*(D^*1/f)/2) - (Iin/6) + ((pi-alpha-duty)/(2^*pi^*(1-D))^*(Vin/Lin)^*(D^*1/f)); \\ &i2 = i1 + ((alpha)/(2^*pi^*(1-D))^*(Vin/Lin)^*(D^*1/f)); \\ &i3 = (j1^*normFactor^*n) + ((-(Vin/Lin)^*(D^*1/f)/2) - (Iin/6) + ((pi)/(2^*pi^*(1-D))^*(Vin/Lin)^*(D^*1/f))); \end{split}$$

$$\begin{split} Iy &= [0; \ 0; \ i0; \ -i1; \ -i2; \ -i3; \ 0; \ 0]; \\ Ix &= [0; \ duty; \ duty + 0.00001; \ pi-alpha; \ pi; \ pi+beta; \ 2^*pi-alpha; \ 2^*pi]; \end{split}$$

end end end

E.1.6 Diode waveforms

Diode voltage

function [Vx,Vy] = VwaveFormD1(D,G,region,n,Fsw,Llk) %Diode voltage

Vout = 650; F = 0.5; w=2*pi*Fsw; k = 2*n/G; cm = region; % 0: ccm % 1: dcm1 % 2: dcm2

normFactor = Vout*F/(w*Llk);

j0 = [];

j1 = [];j2 = [];alpha = [];beta = [];Vmax = [];Vx = [];Vy = [];if D = 0.5 $j0 = pi/2^* (1+k/(1-D)) * ((1-D)/k - 2^*D);$ j1 = 2*pi*D * (k/(1-D)-1);j2 = pi/2 * (k/(1-D) - 1) * ((1-D)/k + 2*D);beta = 2*pi*D; if(cm == 0) $alpha = pi/2^* (2^*D - (1-D)/k);$ else $alpha = pi^*(1-(2^*k^*D/(1-D)));$ end else j0 = pi/2 * (1/k-2) * (1+k-D);j1 = 2*pi * (1-D) * (k/(1-D)-1);j2 = pi/2 * (1/k + 2) * (-1+k+D);beta = 2*pi*(1-D);if cm == 0

alpha = pi/2 * (1-D) * (2 - 1/k);else alpha = pi * (1-2*k);end

 ${\rm end}$

Vmax = (Vout/G)/(1-D);duty= 2*pi*(D);

if cm == 0

Vx = [0; pi-beta+alpha; pi-beta+alpha+0.0001; pi-beta+alpha+duty; pi-beta+alpha+duty+0.0001; 2*pi];Vy = [0; 0; -Vout; -Vout; 0; 0];

else

if $D \ge 0.5$

Vy = [0; 0; -Vout/2; -Vout/2; -Vout; -Vout; -Vout/2; -Vout/2; 0; 0]; Vx = [0; pi-beta-alpha; pi-beta-alpha+0.0001 ; pi-beta; pi-beta+0.0001; 2*pi-betaalpha; 2*pi-beta-alpha+0.0001; 2*pi-beta; 2*pi-beta+0.0001; 2*pi];

else

 $\begin{array}{l} Vy = [-Vout; -Vout; -Vout/2; -Vout/2; 0; 0; -Vout/2; -Vout/2; -Vout]; \\ Vx = [0; pi-alpha; pi-alpha+0.0001; pi; pi+0.0001; 2*pi-alpha; 2*pi-alpha+0.0001; 2*pi-0.0001; 2*pi]; \\ end \\ end \\ end \\ \end{array}$

Diode current

function [Ix,Iy] = IwaveFormId1(D,G,region,n,Fsw,Llk) % Diode current Vout = 650; F = 0.5; w=2*pi*Fsw; k = 2*n/G; cm = region; % 0: ccm % 1: dcm1 % 2: dcm2

normFactor = Vout*F/(w*Llk);

j0 = [];j1 = [];j2 = [];alpha = [];beta = [];Ix = [];Iy = [];if $D \le 0.5$ $j0 = pi/2^* (1+k/(1-D)) * ((1-D)/k - 2^*D);$ j1 = 2*pi*D * (k/(1-D)-1);j2 = pi/2 * (k/(1-D) - 1) * ((1-D)/k + 2*D);beta = 2*pi*D; if(cm == 0) $alpha = pi/2^* (2^*D - (1-D)/k);$ else $alpha = pi^*(1-(2^*k^*D/(1-D)));$ end

else

$$\begin{split} j0 &= pi/2 * (1/k-2) * (1+k-D); \\ j1 &= 2*pi * (1-D) * (k/(1-D)-1); \\ j2 &= pi/2 * (1/k+2) * (-1+k+D); \\ beta &= 2*pi*(1-D); \end{split}$$

if cm == 0 alpha = pi/2 * (1-D) * (2 - 1/k); else alpha = pi * (1-2*k);end

end

if cm == 0

Iy = [j2; -j0; 0; 0; 0; 0; j2];

Ix = [0; pi-beta; pi-beta+alpha; pi; 2*pi-beta; 2*pi-beta+alpha; 2*pi];

else

if D ≥ 0.5

Iy = [j1; 0; 0; 0; 0; 0; j1];Ix = [0; pi-beta-alpha; pi-beta; pi; 2*pi-beta-alpha; 2*pi-beta; 2*pi];

else

Iy = [0; 0; 0; 0; j1; 0; 0];Ix = [0; beta; pi-alpha; pi; pi+beta; 2*pi-alpha; 2*pi]; end end
$$\label{eq:Iy} \begin{split} Iy = Iy.*normFactor; \\ end \end{split}$$

E.1.7 Output capacitor waveforms

```
Output capacitor voltage
```

 $\label{eq:constraint} \begin{array}{l} \mbox{function} ~[~Vx,Vy~] = VwaveFormCapacitor(D,G,region,power,n,Fsw,Llk,Cin~) \\ \% Output ~capacitor~voltage \end{array}$

c = Cin;Vout = 650;F = 0.5;w=2*pi*Fsw;k = 2*n/G;cm = region;% 0: ccm % 1: dcm1 % 2: dcm2 Iout=power/Vout; normFactor = Vout*F/(w*Llk);j0 = [];j1 = [];j2 = [];alpha = [];beta = [];Ix = [];Iy = [];if D ≤ 0.5 $j0 = pi/2^* (1+k/(1-D))^* ((1-D)/k - 2^*D);$
$$\begin{split} j1 &= 2^* pi^* D * (k/(1\text{-}D)\text{-}1); \\ j2 &= pi/2 * (k/(1\text{-}D) \text{-} 1) * ((1\text{-}D)/k + 2^*D); \\ beta &= 2^* pi^* D; \end{split}$$

$$\label{eq:cm} \begin{split} & if(cm == 0) \\ & alpha = pi/2* \; (2*D - (1-D)/k); \\ & else \\ & alpha = pi*(1-(2*k*D/(1-D))); \\ & end \\ & else \end{split}$$

j0 = pi/2 * (1/k-2) * (1+k-D); j1 = 2*pi * (1-D) * (k/(1-D)-1); j2 = pi/2 * (1/k + 2) * (-1+k+D);beta = 2*pi*(1-D);

if cm == 0 alpha = pi/2 * (1-D) * (2 - 1/k);else alpha = pi * (1-2*k);end end

if cm == 0

$$\begin{split} Iy &= [j2; -j0; 0; 0; 0; 0; j2]; \\ Ix &= [0; pi-beta; pi-beta+alpha; pi; 2*pi-beta; 2*pi-beta+alpha; 2*pi]; \\ else \end{split}$$

if $D \ge 0.5$ Iy = [j1; 0; 0; 0; 0; 0; j1]; Ix = [0; pi-beta-alpha; pi-beta; pi; 2*pi-beta-alpha; 2*pi-beta; 2*pi]; else
$$\begin{split} Iy &= [0; \ 0; \ 0; \ 0; \ j1; \ 0; \ 0]; \\ Ix &= [0; \ beta; \ pi-alpha; \ pi; \ pi+beta; \ 2^*pi-alpha; \ 2^*pi]; \\ end \end{split}$$

 ${\rm end}$

$$\begin{split} Iy &= Iy.*normFactor;\\ [Ix,Iy] &= shifting(Ix,Iy,0);\\ [Ix2,Iy2] &= shifting(Ix,Iy,2*pi/3);\\ [Ix3,Iy3] &= shifting(Ix,Iy,4*pi/3); \end{split}$$

```
Ix = Ix';

Iy = Iy';

Ixu = union(Ix,Ix2);

Ixu = union(Ixu,Ix3);

sort(Ixu);
```

```
Iy1 = interp1(Ix,Iy,Ixu);

Iy2 = interp1(Ix2,Iy2,Ixu);

Iy3 = interp1(Ix3,Iy3,Ixu);
```

$$\begin{split} & Ix = Ixu; \\ & Iy = Iy1 + Iy2 + Iy3 \text{-Iout}; \end{split}$$

Vx=Ix; Vy=(650/2)+((Iy/10/c)*(D*1/Fsw)/2); end

Output capacitor current

 $\label{eq:function} \ensuremath{\left[\ Ix,Iy \ \right] = IwaveFormIcout(\ D,G,region,power,n,Fsw,Llk \)} % Output \ capacitor \ current$

Vout = 650;F = 0.5; w=2*pi*Fsw; k = 2*n/G; cm = region; % 0: ccm % 1: dcm1 % 2: dcm2 Iout=power/Vout;

normFactor = Vout*F/(w*Llk); j0 = [];j1 = [];j2 = [];alpha = [];beta = [];Ix = [];Iy = [];if $D \le 0.5$ $j0 = pi/2^* (1+k/(1-D)) * ((1-D)/k - 2^*D);$ j1 = 2*pi*D * (k/(1-D)-1);j2 = pi/2 * (k/(1-D) - 1) * ((1-D)/k + 2*D);beta = 2*pi*D; if(cm == 0) $alpha = pi/2^* (2^*D - (1-D)/k);$ else $alpha = pi^*(1-(2^*k^*D/(1-D)));$ end else j0 = pi/2 * (1/k-2) * (1+k-D);

j1 = 2*pi * (1-D) * (k/(1-D)-1);

```
j2 = pi/2 * (1/k + 2) * (-1+k+D);
beta = 2*pi*(1-D);
if cm == 0
alpha = pi/2 * (1-D) * (2 - 1/k);
else
alpha = pi * (1-2*k);
end
end
if cm == 0
Iy = [j2; -j0; 0; 0; 0; 0; j2];
Ix = [0; pi-beta; pi-beta+alpha; pi; 2*pi-beta; 2*pi-beta+alpha; 2*pi];
else
if D \ge 0.5
Iy = [j1; 0; 0; 0; 0; 0; j1];
Ix = [0; pi-beta-alpha; pi-beta; pi; 2*pi-beta-alpha; 2*pi-beta; 2*pi];
else
Iy = [0; 0; 0; 0; j1; 0; 0];
Ix = [0; beta; pi-alpha; pi; pi+beta; 2*pi-alpha; 2*pi];
end
```

end

$$\begin{split} Iy &= Iy.*normFactor;\\ [Ix,Iy] &= shifting(Ix,Iy,0);\\ [Ix2,Iy2] &= shifting(Ix,Iy,2*pi/3);\\ [Ix3,Iy3] &= shifting(Ix,Iy,4*pi/3); \end{split}$$

Ix = Ix';Iy = Iy';

Ixu = union(Ix,Ix2); Ixu = union(Ixu,Ix3); sort(Ixu);

$$\begin{split} Iy1 &= interp1(Ix,Iy,Ixu);\\ Iy2 &= interp1(Ix2,Iy2,Ixu);\\ Iy3 &= interp1(Ix3,Iy3,Ixu); \end{split}$$

Ix= Ixu; Iy= Iy1+Iy2+Iy3-Iout;

 end

E.1.8 Plot all boundary

```
Fsw=20e3;

Llk=2.5e-6;

D=0:1e-6:1;

F=0.5;

w=2*pi*Fsw;

n=2.5*2;

%No operation

NO=n*1/(1 D);
```

NO=n*1./(1-D); figure(1) plot(D,NO,'r','linewidth',2); axis([0, 1, 0, 45]); xlabel('ylabel('hold on grid on

text(0.15, 27.5, '

```
%Dcm for D<0.5
d1=0:1e-4:0.5;
DCM1= n*(2*d1)./(1-d1);
plot(d1,DCM1,'r','linewidth',2);
text(0.12,2.5,'
```

line([0.5 1],[10 10],'linewidth',2,'color','r');

%Dcm for D>0.5 d2=0.5:1e-4:1; DCM2= n*2; plot(d2,DCM2,'r','linewidth',0.1); text(0.85,17.5,'

```
%Plot R at full load 63.5V
r1=11.089/(w*Llk);
```

```
%find duty cycle intersect between ccm/dcm D>0.5
dintersect1= (0.5+1/(3*F^2*r1*pi));
%find duty cycle intersect between ccm/dcm D<0.5
dintersect2= (0.5-1/(3*F^2*r1*pi));
```

```
ddcm1= 0:1e-4:dintersect2;
ddcm2= dintersect1:1e-4:1;
dccm= dintersect2:1e-4:dintersect1;
ddcm1 = [ddcm1 dintersect2];
dccm = [dccm dintersect1];
```

```
%m' at ccm region

mfullccm = n*(4./(6*pi*F^2*r1*(1-dccm))).*(-1+sqrt(1+9*dccm.*(1-dccm).*pi.^2*F.^4*r1.^2));

%m' at dcm region d<0.5

mfulldcm1 = n*((3*pi*F^2*r1*ddcm1.^2)./(1-ddcm1)).*

(-1+sqrt(1+(2./(3*pi*F^2*r1*ddcm1.^2))));
```

%m' at dcm region d>0.5

 $mfulldcm2 = n^{*}(3^{*}pi^{*}F^{2}r1^{*}(1-ddcm2)).^{*}(-1+sqrt(1+(2./(3^{*}pi^{*}F^{2}r1^{*}(1-ddcm2).^{2}))));$

 $d = [ddcm1 \ dccm \ ddcm2]; m = [mfulldcm1 \ mfullccm \ mfulldcm2]; p3=plot (d,m,'b','linewidth',1); text(0.5,8.5,'text(0.5238,10.236,'X','Fontsize',10);$

r1=35.208/(w*Llk);

dintersect1= $(0.5+1/(3*F^2*r1*pi))$; dintersect2= $(0.5-1/(3*F^2*r1*pi))$;

ddcm1 = 0:1e-4:dintersect2; ddcm2 = dintersect1:1e-4:1; dccm = dintersect2:1e-4:dintersect1; ddcm1 = [ddcm1 dintersect2]; dccm = [dccm dintersect1];

$$\begin{split} & mfullccm = n^*(4./(6^*pi^*F^2^*r1^*(1\text{-}dccm))).^*(-1 + \text{sqrt}(1 + 9^*dccm.^*(1\text{-}dccm).^*pi.^2^*F.^4^*r1.^2)); \\ & mfulldcm1 = n^*((3^*pi^*F^2^*r1^*ddcm1.^2)./(1\text{-}ddcm1)).^*(-1 + \text{sqrt}(1 + (2./(3^*pi^*F^2^*r1^*(1\text{-}ddcm2).^2)))); \\ & (3^*pi^*F^2^*r1^*ddcm1.^2)))); \\ & mfulldcm2 = n^*(3^*pi^*F^2^*r1^*(1\text{-}ddcm2)).^*(-1 + \text{sqrt}(1 + (2./(3^*pi^*F^2^*r1^*(1\text{-}ddcm2).^2)))); \end{split}$$

 $d = [ddcm1 \ dccm \ ddcm2]; m = [mfulldcm1 \ mfullccm \ mfulldcm2]; p1 = plot \ (d,m,'r','linewidth',1);$

text(0.8,31,'o @ start up','Fontsize',10); text(0.858,32.5,'X','Fontsize',10);

r1 = 422.5/(w*Llk);

dintersect1= $(0.5+1/(3*F^2*r1*pi))$; dintersect2= $(0.5-1/(3*F^2*r1*pi))$;

ddcm1 = 0:1e-4:dintersect2; ddcm2 = dintersect1:1e-4:1; dccm = dintersect2:1e-4:dintersect1; ddcm1 = [ddcm1 dintersect2]; dccm = [dccm dintersect1];

$$\begin{split} & m fullccm = n^*(4./(6^*pi^*F^2^*r1^*(1\text{-}dccm))).^*(-1 + \text{sqrt}(1 + 9^*dccm.^*(1\text{-}dccm).^*pi.^2^*F.^4^*r1.^2)); \\ & m fulldcm1 = n^*((3^*pi^*F^2^*r1^*ddcm1.^2)./(1\text{-}ddcm1)).^*(-1 + \text{sqrt}(1 + (2./(3^*pi^*F^2^*r1^*(1\text{-}ddcm2).^2)))); \\ & (3^*pi^*F^2^*r1^*ddcm1.^2)))); \\ & m fulldcm2 = n^*(3^*pi^*F^2^*r1^*(1\text{-}ddcm2)).^*(-1 + \text{sqrt}(1 + (2./(3^*pi^*F^2^*r1^*(1\text{-}ddcm2).^2)))); \end{split}$$

d = [ddcm1 dccm ddcm2]; m = [mfulldcm1 mfullccm mfulldcm2]; p2=plot (d,m,'Color',[1]); p2=plot (d,m,

0.4 0],'linewidth',1);

text(0.8,31,' @ start up','Fontsize',10); text(0.8472,32.5,'X','Fontsize',10); line([0.8472 0.8585], [32.5 32.5],'LineWidth',1.5);

r1=20.067/(w*Llk);

dintersect1= $(0.5+1/(3*F^2*r1*pi))$; dintersect2= $(0.5-1/(3*F^2*r1*pi))$;

ddcm1 = 0:1e-4:dintersect2; ddcm2 = dintersect1:1e-4:1; dccm = dintersect2:1e-4:dintersect1; ddcm1 = [ddcm1 dintersect2]; dccm = [dccm dintersect1];

$$\begin{split} m fullccm &= n^*(4./(6^*pi^*F^2^*r1^*(1\text{-}dccm))).^*(-1 + \text{sqrt}(1 + 9^*dccm.^*(1\text{-}dccm).^*pi.^2^*F.^4^*r1.^2)); \\ m fulldcm1 &= n^*((3^*pi^*F^2^*r1^*ddcm1.^2)./(1\text{-}ddcm1)).^*(-1 + \text{sqrt}(1 + (2./(3^*pi^*F^2^*r1^*ddcm1.^2)))); \\ (3^*pi^*F^2^*r1^*ddcm1.^2)))); \\ m fulldcm2 &= n^*(3^*pi^*F^2^*r1^*(1\text{-}ddcm2)).^*(-1 + \text{sqrt}(1 + (2./(3^*pi^*F^2^*r1^*(1\text{-}ddcm2).^2)))); \end{split}$$

d = [ddcm1 dccm ddcm2]; m = [mfulldcm1 mfullccm mfulldcm2]; p4=plot (d,m,'m','linewidth',1);

text(0.26,12,' @ light load','Fontsize',10); text(0.3314,7.386,'X','Fontsize',10);

r1=20.067/(w*Llk);

dintersect1= $(0.5+1/(3*F^2*r1*pi))$; dintersect2= $(0.5-1/(3*F^2*r1*pi))$;

ddcm1 = 0:1e-4:dintersect2; ddcm2 = dintersect1:1e-4:1; dccm = dintersect2:1e-4:dintersect1; ddcm1 = [ddcm1 dintersect2]; dccm = [dccm dintersect1];

$$\begin{split} & mfullccm = n^*(4./(6^*pi^*F^2^*r1^*(1\text{-}dccm))).^*(-1 + \text{sqrt}(1 + 9^*dccm.^*(1\text{-}dccm).^*pi.^2^*F.^4^*r1.^2)); \\ & mfulldcm1 = n^*((3^*pi^*F^2^*r1^*ddcm1.^2)./(1\text{-}ddcm1)).^*(-1 + \text{sqrt}(1 + (2./(3^*pi^*F^2^*r1^*(1\text{-}ddcm2).^2)))); \\ & (3^*pi^*F^2^*r1^*ddcm1.^2)))); \\ & mfulldcm2 = n^*(3^*pi^*F^2^*r1^*(1\text{-}ddcm2)).^*(-1 + \text{sqrt}(1 + (2./(3^*pi^*F^2^*r1^*(1\text{-}ddcm2).^2)))); \end{split}$$

 $d = [ddcm1 \ dccm \ ddcm2]; m = [mfulldcm1 \ mfullccm \ mfulldcm2]; p5 = plot \ (d,m,'g','linewidth',1);$

text(0.35,6,' @ 20kw','Fontsize',10); text(0.3971,8.125,'X','Fontsize',10); line([0.5238 0.3314], [10.236 7.386],'LineWidth',1.5);

legend([p1 p2 p3 p4 p5],' @ upper boundary startup load','@ lower boundary startup load',' @ full load','@ light load',' @ 20kW power load','Location','northwest');

Loss analysis

```
%Loss analysis
clc
clear all
Vin = [20:0.5:100];
```

```
load('possible.mat','temp');
temp =[2.5 20e3 25e-6];
eff=[];
temp2=[];
```

```
Lin=7.5e-4;
```

```
for j = [1:size(temp,1)]

n(j)=temp(j,1);

Fsw(j)=temp(j,2);

Llk(j)=temp(j,3);

end
```

```
for j = [1:size(temp,1)]
for i = [1:length(Vin)]
if Vin(i)_i = 63.5
power(i) = 600^*Vin(i)/10;
elseif Vin(i)_i = 88
power(i) = ((-20.408^*Vin(i))+1895.904)^*Vin(i)/10;
else
power(i) = (-0.053^*Vin(i)^2 + 5.758^*Vin(i) + 7.926)^*Vin(i)/10;
end
```

```
\begin{split} & [PconDevice1(i), PswDevice1(i), PconDevice2(i), PswDevice2(i), TotallossDevice1(i), \\ & TotallossDevice2(i)] = Devicelossreduce(Vin(i), n(j), Fsw(j), Llk(j), Lin); \\ & [Pcon(i), Prec(i), PtotalDi(i)] = Diodelossreduce(Vin(i), n(j), Fsw(j), Llk(j)); \\ & [Pdi(i), PtotalCap(i)] = Capacitorlossreduce(Vin(i), n(j), Fsw(j), Llk(j), Lin); \\ & [Pcoreloss(i), Pcopperloss(i), Totalinductorloss(i)] = Inductorlossreduce (Vin(i), n(j), Fsw(j), Llk(j), Lin); \\ & [Pdi2(i), Ptotalcapout(i)] = outputcapacitorlossreduce (Vin(i), n(j), Fsw(j), Llk(j), Lin); \\ & [Pdi2(i), Ptotalcapout(i)] = outputcapacitorlossreduce (Vin(i), n(j), Fsw(j), Llk(j), Lin); \\ & Ptotalloss(i) = Ptotalcapout(i) + PtotalCap(i) + PtotalDi(i) + TotallossDevice2(i) + \\ & TotallossDevice1(i) + Totalinductorloss(i); \end{split}
```

```
temp2(:,end+1) = (power(i)-Ptotalloss(i))/power(i)*100;
end
eff(end+1,:) = temp2;
temp2=[];
end
save('efficiency.mat','eff');
for i = [1:size(temp,1)]
temp2(i,1,:) = roundn(1/temp(i,1,:),-2);
end
for j = [1:size(temp)]
temp2(j,2,:) = temp(j,2,:);
end
for k = [1:size(temp)]
temp2(k,3,:) = temp(k,3,:);
end
figure
text = cell(1);
for \mathbf{k} = [1:\text{size}(\text{eff},1)]
```

plot (Vin,eff(k,:),'Color',[rand rand rand]);

```
xlabel('Input voltage (V)','Fontsize', 11);
ylabel('bfEfficiency (%)','Fontsize', 11);
textk=num2str(temp2(k,:));
legend(num2str(temp(k,:)))
hold on
end
```

axis([20,100,0,100]);

E.1.9 Device loss

function [PconDevice1,PswDevice1,PconDevice2,PswDevice2,TotallossDevice1,TotallossDevice2] = Devicelossreduce(Vin,n,Fsw,Llk,Lin) %Loss analysis

%Input components mosfet IXFB132N50P3 %Vds=500V Ids=132A

```
Rds = 45e-3;
ton = 110e-9;
toff = 150e-9;
Nchannel= 1;
Lin=Lin;
w = 2*pi*Fsw;
Vout = 650;
G = Vout/Vin;
k = 2*n/G;
if Vinj= 63.5
power = 600*Vin/10;
elseif Vinj= 88
```

```
power = ((-20.408*Vin)+1895.904)*Vin/10;
else
power = (-0.053*Vin^2 + 5.758*Vin + 7.926)*Vin/10; end
```

```
R = (Vout^2)/power;
```

```
\begin{split} [d,g,r] &= outputR(R,n,Fsw,Llk);\\ iNan &= find(isnan(g));\\ g(iNan) &= [];\\ d(iNan) &= [];\\ r(iNan) &= []; \end{split}
```

```
iDuplicate = find(diff(g)==0);
g(iDuplicate) = [];
d(iDuplicate) = [];
r(iDuplicate) = [];
```

```
D = interp1(g,d,G);
region = interp1(g,r,G,'nearest');
```

 $\% {\rm Loss}$ calculation

[Ix1,Iy1] = IwaveFormImos1(D,G,region,power,n,Fsw,Llk,Lin); [Ix2,Iy2] = IwaveFormImos2(D,G,region,power,n,Fsw,Llk,Lin);

```
step= 0:1e-4:2*pi;
[Ix1,Iy1]=shifting(Ix1,Iy1,0);
[Ix2,Iy2]=shifting(Ix2,Iy2,0);
Iy1rms = interp1(Ix1,Iy1,step);
Iy2rms = interp1(Ix2,Iy2,step);
Iy1rms= RMS(step,Iy1rms);
Iy2rms= RMS(step,Iy2rms);
```

Iy1rms = Iy1rms/Nchannel; Iy2rms = Iy2rms/Nchannel; PconDevice1 = (Iy1rms.²)*Rds; PconDevice2 = (Iy2rms.²)*Rds;

%calculate switching loss cm=region;

[Vx3,Vy3] = VwaveFormMos1(D,G,region,n,Fsw,Llk);
[Vx4,Vy4] = VwaveFormMos2(D,G,region,n,Fsw,Llk);
[Ix3,Iy3] = IwaveFormImos1(D,G,region,power,n,Fsw,Llk,Lin);
[Ix4,Iy4] = IwaveFormImos2(D,G,region,power,n,Fsw,Llk,Lin);

```
Iy3=Iy3/Nchannel;
Iy4=Iy4/Nchannel;
if cm == 0
if D_{\dot{c}}=0.5
IonDevice1= Iy3(1);
IoffDevice1= Iy3(5);
IonDevice2= Iy4(3);
IoffDevice2= Iy4(5);
else
IonDevice1= Iy3(1);
IoffDevice1= Iy3(3);
IonDevice2= Iy4(3);
IonDevice2= Iy4(3);
IoffDevice2= Iy4(7);
```

end else

if $D_{\xi}=0.5$ IonDevice1= Iy3(1); IoffDevice1= Iy3(6);

IonDevice2 = Iy4(3);IoffDevice2 = Iy4(4);

else

IonDevice1= Iy3(1); IoffDevice1= Iy3(2);

IonDevice2 = Iy4(4);IoffDevice2 = Iy4(8);

 ${\rm end}$

end

VonDevice1= max(Vy3); VoffDevice1= max(Vy3); VonDevice2= max(Vy4); VoffDevice2= max(Vy4);

```
if IonDevice1;0
IonDevice1 = IonDevice1;
else
IonDevice1 = 0;
end
if IoffDevice1;0
IffDevice1 = IoffDevice1;
else
```
```
IoffDevice1 = 0;
end
if IonDevice2;0
IonDevice2 = IonDevice2;
else
IonDevice2 = 0;
end
if IoffDevice2;0
IoffDevice2 = IoffDevice2;
else
IoffDevice2 = abs(IoffDevice2);
end
VonDevice1 = \max(Vy3);
VoffDevice1 = \max(Vy3);
VonDevice2= \max(Vy4);
VoffDevice2= \max(Vy4);
PonDevice1 = (ton*VonDevice1*IonDevice1*Fsw)/2;
PonDevice2 = (ton*VonDevice2*IonDevice2*Fsw)/2;
PoffDevice1 = (toff*VoffDevice1*IoffDevice1*Fsw)/2;
PoffDevice2 = (toff*VoffDevice2*IoffDevice2*Fsw)/2;
PswDevice1= PonDevice1+PoffDevice1;
PswDevice2= PonDevice2+PoffDevice2;
TotallossDevice1 = (PconDevice1 + PswDevice1)*6*Nchannel;
TotallossDevice2 = (PconDevice2 + PswDevice2)*6*Nchannel;
```

E.1.10 Inductor losses

```
function [Pcoreloss, Pcopperloss, Totalloss] = Inductorlossreduce(Vin,n,Fsw,Llk,Lin
)
%Inductor loss calculation
wcore = 0.454;
rcopper = 10*0.99e-3;
w = 2*pi*Fsw;
Vout = 650;
G = Vout/Vin;
k = 2*n/G;
if Vin_i = 63.5
power = 600*Vin/10;
elseif Vin_i = 88
power = ((-20.408*Vin)+1895.904)*Vin/10;
else
power = (-0.053*Vin^2 + 5.758*Vin + 7.926)*Vin/10;
end
R = (Vout^2)/power;
[d,g,r] = outputR(R,n,Fsw,Llk);
iNan = find(isnan(g));
g(iNan) = [];
d(iNan) = [];
r(iNan) = [];
iDuplicate = find(diff(g) == 0);
g(iDuplicate) = [];
d(iDuplicate) = [];
```

r(iDuplicate) = [];

D = interp1(g,d,G);region = interp1(g,r,G,'nearest');

[Ix,Iy]=IwaveFormIlinreduce(D,G,region,power,n,Fsw,Llk,Lin); Iymax= abs(max(Iy)); Iyrms = RMS(Ix,Iy);

Bac= (Iymax*1.5e-4)/(16*3.2e-4); B=Bac/2;

Pcoreloss= 6.5*((Fsw/1000)^1.51)*(B^1.74)*wcore; Pcopperloss= Iyrms^2*rcopper; Totalloss = (Pcoreloss+Pcopperloss)*6;

E.1.11 Output capacitor losses

function [Pdi,Ptotal] = Outputcapacitorlossreduce(Vin,n,Fsw,Llk,Lin)
%Loss analysis

%Input components PMC1405350 %Vdc400 Vrms275 Vpeak600 Cap35Uf Ipeak600 Irms34,5 ESR2,2

Esr = 0.04;Nchannel=1;

w=2*pi*Fsw; Vout = 650; G = Vout/Vin;k = 2*n/G;

```
if Vin_i = 63.5
power = 600*Vin/10;
elseif Vin_i = 88
power = ((-20.408*Vin)+1895.904)*Vin/10;
else
power = (-0.053*Vin^2 + 5.758*Vin + 7.926)*Vin/10;
end
R = (Vout^2)/power;
[d,g,r] = outputR(R,n,Fsw,Llk);
iNan = find(isnan(g));
g(iNan) = [];
d(iNan) = [];
r(iNan) = [];
iDuplicate = find(diff(g) == 0);
g(iDuplicate) = [];
d(iDuplicate) = [];
r(iDuplicate) = [];
D = interp1(g,d,G);
region = interp1(g,r,G,'nearest');
[Ix2,Iy2] = IwaveFormIcoutreduce(D,G,region,power,n,Fsw,Llk);
```

```
step= 0:1e-4:2*pi;

[Ix2,Iy2]=shifting(Ix2,Iy2,0);

Iy2rms = interp1(Ix2,Iy2,step);

Iy2rms= RMS(step,Iy2rms);

Iy2rms = Iy2rms/Nchannel;

Pdi = (Iy2rms.^2)*Esr;
```

```
Ptotal = Pdi^{*}2;
end
```

E.1.12 Clamp capacitor losses

function [Pdi,Ptotal] = Capacitorlossreduce(Vin,n,Fsw,Llk,Lin)

Esr = 0.1e-3; Nchannel= 8; w=2*pi*Fsw;Vout = 650; G = Vout/Vin; k = 2*n/G;if Vinj= 63.5 power = 600*Vin/10; elseif Vinj= 88 power = ((-20.408*Vin)+1895.904)*Vin/10; else power = (-0.053*Vin^2 + 5.758*Vin + 7.926)*Vin/10; end $R = (Vout^2)/power;$ [d,g,r] = outputR(R,n,Fsw,Llk);

[d,g,r] = outputk(R,n,Fsw,Lik), iNan = find(isnan(g)); g(iNan)=[]; d(iNan)=[];r(iNan)=[];

iDuplicate = find(diff(g) = = 0);

```
g(iDuplicate) = [];

d(iDuplicate) = [];

r(iDuplicate) = [];
```

```
D = interp1(g,d,G);
region = interp1(g,r,G,'nearest');
```

[Ix2,Iy2] = IwaveFormImos2reduce(D,G,region,power,n,Fsw,Llk,Lin);

```
step= 0:1e-4:2*pi;

[Ix2,Iy2]=shifting(Ix2,Iy2,0);

Iy2rms = interp1(Ix2,Iy2,step);

Iy2rms= RMS(step,Iy2rms);

Iy2rms = Iy2rms/Nchannel;

Pdi = (Iy2rms.^2)*Esr;

Ptotal = Pdi*6*Nchannel;

end
```

Appendix F

Simulation schematics



Figure F.1: Simulation schematic of a 3-phase interleaved boost converter with coupled inductor and clamp capacitor



Figure F.2: Simulation schematic of a PWM generator



Figure F.3: Simulation schematic of a H-bridge converter

Appendix G

Experimental results of the converter input and output power



Figure G.1: Converter efficiency at start-up load 1.182kW (Top) Input power (Bottom) output power

APPENDIX G. EXPERIMENTAL RESULTS OF THE CONVERTER INPUT AND OUTPUT POWER



Figure G.2: Converter efficiency at start-up load 2.033kW (Top) Input power (Bottom) Output power



Figure G.3: Converter efficiency at start-up load 2.941kW (Top) Input power (Bottom) Output power

	rrenge 2007 PH3 Solat units ces current frequency	America Augusta 3.9278k 63.499 61.864 0.0000	bendervätte barr W V A Hz	
<u>N</u> N	4L			PPA2530 Precision Power Analyzer Kinet
C.K)	Vrange 355' PH3 bota watts ratioge ratioge ratioge current frequency	Process and sectors 3.66662k 649.99 5.6411 0.00000	W W V A Hz	

Figure G.4: Converter efficiency at full load 3.667kW (Top) Input power (Bottom) Output power

APPENDIX G. EXPERIMENTAL RESULTS OF THE CONVERTER INPUT AND OUTPUT POWER



Figure G.5: Converter efficiency at nominal load 2.542kW (Top) Input power (Bottom) Output power



Figure G.6: Converter efficiency at nominal load 1.941kW (Top) Input power (Bottom) Output power

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