NON-VOLATILE FPGA ARCHITECTURE USING RESISTIVE SWITCHING DEVICES

PATRICK HO WAN CHUAN

B.ENG (HONS) M.SC

DISSERTATION SUBMITTED IN PARTIAL FULFILLMENT OF THE REQUIREMENTS FOR THE DEGREE OF DOCTOR OF PHILOSOPHY (PhD) IN ELECTRICAL & ELECTRONIC ENGINEERING FROM THE UNIVERSITY OF NOTTINGHAM MALAYSIA CAMPUS

ABSTRACT

This dissertation reports the research work that was conducted to propose a non-volatile architecture for FPGA using resistive switching devices. This is achieved by designing a Configurable Memristive Logic Block (CMLB). The CMLB comprises of memristive logic cells (MLC) interconnected to each other using memristive switch matrices. In the MLC, novel memristive D flip-flop (MDFF), 6-bit non-volatile look-up table (NVLUT), and CMOS-based multiplexers are used. Other than the MDFF, a non-volatile D-latch (NVDL) was also designed. The MDFF and the NVDL are proposed to replace CMOS-based D flip-flops and D-latches to improve energy consumption. The CMLB shows a reduction of 8.6% of device area and 1.094 times lesser critical path delay against the SRAM-based FPGA architecture. Against similar CMOS-based circuits, the MDFF provides switching speed of 1.08 times faster; the NVLUT reduces power consumption by 6.25nW and improves device area by 128 transistors; while the memristive logic cells reduce overall device area by 60.416μm^2. The NVLUT is constructed using novel 2TG1M memory cells, which has the fastest switching times of 12.14ns, compared to other similar memristive memory cells. This is due to the usage of transmission gates which improves voltage transfer from input to the memristor. The novel 2TG1M memory cell also has lower energy consumption than the CMOS-based 6T SRAM cell. The memristive-based switch matrices that interconnects the MLCs together comprises of novel 7T1M SRAM cells, which has the lowest energy-delay-area-

product value of 1.61 among other memristive SRAM cells. Two memristive logic gates (MLG) were also designed (OR and AND), that introduces non-volatility into conventional logic gates. All the above circuits and design simulations were performed on an enhanced SPICE memristor model, which was improved from a previously published memristor model. The previously published memristor model was fault to not be in good agreement with memristor theory and the physical model of memristors. Therefore, the enhanced SPICE memristor model provides a memristor model which is in good agreement with the memristor theory and the physical model of memristors, which is used throughout this research work.

ACKNOWLEDGEMENT

Thank you to my supervisor Dr. T. Nandha Kumar and co-supervisor Prof. Haider Abbas F. Almurib for giving constant guidance and supervision on the direction of my research.

I would also like to express my gratitude towards my PhD colleagues, Firas O. Hatem and Nemat Al-Hassan for their teamwork and dedication to complete projects together.

My family, loved ones, especially Ming Teng, and my godmother have been the greatest source of determination and motivation to complete this research, as well as friends that have also given their tremendous support.

I would also like to thank God almighty for His blessings upon me for me to complete my PhD.

LIST OF PUBLICATIONS

List of published works in journals:

1. P. W. C. Ho, H. A. F. Almurib, and T. Nandha Kumar, "Configurable Memristive Logic Block for Memristive-based FPGA Architectures" in *INTEGRATION, the VLSI journal, – re-submitted with minor revision.*

2. P. W. C. Ho, F. O. Hatem, H. A. F. Almurib, and T. N. Kumar, "Comparison between Pt/TiO2/Pt and Pt/TaOX/TaOY/Pt based bipolar resistive switching devices," *IOP Journal of Semiconductors*, vol. 37, no. 6, p. 064001, 2016.

3. F. O. Hatem, P. W. C. Ho, H. A. F. Almurib, and T. N. Kumar, "Modeling of Bipolar Resistive Switching of Nonlinear MISM Memristor" in *IOP Semiconductor Science and Technology,* vol. 30, no. 11, pp. 115009, 2015. (journal highlight article)

4. P. W. C. Ho, H. A. F. Almurib, and T. Nandha Kumar, "Novel Memristive SRAM with 7 transistors and 1 memristor" in *IOP Journal of Semiconductors*. (article confirmed for publication, volume and issue number not yet assigned)

List of published works in conferences:

1. P. W. C. Ho, H. A. F. Almurib, and T. Nandha Kumar, "One-bit Non-Volatile Memory Cell Using Memristor and Transmission Gates," in *IEEE International Conference on Electronic Design*, 2014, pp. 244 – 248. (Presented in 2014, Penang, Malaysia)

2. P. W. C. Ho, F. O. Hatem, H. A. F. Almurib, and T. N. Kumar, "Comparison on TiO_2 and TaO_2 Based Bipolar Resistive Switching Devices," in *IEEE International Conference on Electronic Design*, 2014, pp. 249 – 254.
   (Presented in 2014, Penang, Malaysia)
3. P. W. C. Ho, N. H. El-Hassan, T. N. Kumar, and H. A. F. Almurib, "PCM and Memristor Based Nanocrossbars," in *IEEE International Conference on Nanotechnology (NANO 2015)*, 2015, pp. 456 – 459.
   (Presented in 2015, Rome, Italy)

4. P. W. C. Ho, F. O. Hatem, H. A. F. Almurib, and T. N. Kumar, "Enhanced SPICE Memristor Model with Dynamic Ground," in *IEEE International Circuits and Systems Symposium (ICSyS)*, 2015, pp. 130 – 132.
   (Presented in 2015, Langkawi Island, Malaysia)

5. P. W. C. Ho, H. A. F. Almurib, and T. Nandha Kumar, "Non-volatile D-latch for sequential logic circuits using memristors" in *IEEE Region 10 Conference, TENCON* 2015, 2015, pp. 1 – 4.
   (Presented in 2015, Macau)

List of published works submitted to journals for possible publication:

1. P. W. C. Ho, H. A. F. Almurib, and T. Nandha Kumar, "Non-volatile look-up table using memristive memory cells" in *IET Circuits, Devices & Systems – re-submission after addressing of reviewer comments.*
   (Currently awaiting reviewer response)

2. P. W. C. Ho, H. K. Hoi, H. A. F. Almurib, and T. Nandha Kumar, "Memristive Logic Gates in Combinational Circuits" – *pending submission to journal*.

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1. INTRODUCTION

INTRODUCTION

1.1 Background

Field-Programmable Gate Arrays (FPGA) has become increasingly popular compared to Application Specific Integrated Circuits (ASIC) due to their configurability, programmability and versatility. With the reduction of gate-length in the CMOS process technology, FPGA chips are smaller in size relative to ASIC chips and the rising cost of ASIC is at a higher rate than that for FPGA chips [1]. Current Static Random Access Memory (SRAM) FPGAs have fast switching speeds but are volatile. Furthermore, SRAM cells require 6 transistors to store one-bit logic. These factors contribute to larger device area and an increased routing path length, which eventually leads to higher power consumption and longer critical path delays. Although FPGAs are fully programmable, all programmed information are only kept temporarily due to the volatility of SRAM cells. Thus, programmed information is lost when power supply to the FPGA is disrupted and hence, requires re-programming of the FPGA.

The volatility of SRAM cells and the increased demands for density and speed in electronic devices has driven an increase in the amount of research and in the number of electronic applications being proposed for migration to using non-volatile

memory devices. Such applications have adopted memristors in their designs [2]–[4], while other applications that uses memristors include memristor oscillators [5], memristor-based chaotic circuits [6] and memristor-based adaptive coupling [7]. By using memristors in these electronic applications, these applications have benefitted from reductions of switching delay, power consumption, and device area. Similarly, FPGA applications would also benefit from adopting memristor-based architectures [8]. Using memristor-based FPGA architectures also allow the programmed information to be retained in the FPGAs even if the power supply is interrupted.

The current FPGA market is dominated by SRAM-based architectures [9]. However the SRAM based FGPA architecture is volatile; hence programmed information will be lost in the event of power interruption causing the design in the FPGA to malfunction. Therefore, to address this issue and improve the performance of the FPGA operation in terms of increasing speed, reducing area and reducing power dissipation, the main objective of the research work presented in this dissertation is to propose a novel non-volatile Configurable Memristive Logic Block (CMLB) that can be used in a non-volatile FPGA architecture.

1.2 Problem statement

Due to the numerous memristor models available in the literature review, a single memristor model has to be selected for use throughout the entire research if a novel memristor model is not designed. The selection of the memristor model from the literature is based on the flexibility of the memristor model which allows researchers to adapt the memristor model to different simulation environments.

In the FPGA, there are many CMOS-based memory cells and circuits which are volatile. The objective of this research is to produce a non-volatile FPGA architecture which is based on non-volatile memory cells and circuits. Therefore, novel non-volatile memory cells and circuits are to be designed using memristors. Comparison of these designed non-volatile memory cells and circuits are then compared against similar works in the literature review for verification and justification of selection to be used in the non-volatile FPGA. The following section explains novel memory cells and circuits that must be designed to produce the non-volatile FPGA architecture, as well as the summary of the aims of this research.

1.3 Aims of the research

To achieve the objective of designing a non-volatile FPGA architecture using resistive switching devices, the aim of the research works is to produce a non-volatile configurable logic block. Configurable logic blocks contain various types of electronic and electrical components. For the configurable non-volatile configurable logic block to be novel, the following categories of circuits must also be designed in novelty:

(i) non-volatile memory cell

(ii) non-volatile combinational logic circuit

(iii) non-volatile sequential logic circuit

To produce the above circuits, a single simulation model needs to be identified to be used throughout this research. This is performed by conducting a literature review on the existing SPICE models of resistive switching devices. The SPICE model that is used in this research is obtained by developing an enhanced SPICE memristor model, which was adopted and improved from one of the SPICE models available in the literature. This SPICE model was then used throughout this research to simulate every circuit that are presented in this dissertation, including the simulation of the circuits from the literature and other sources, to ensure simulations are performed on a similar simulation environment and that the results are unbiased.

All the experiments presented in this dissertation are all conducted in SPICE simulation environment. All circuit designs and experiments presented in this dissertation are performed on the LTspice 4.2 software, which is the latest version of the LTspice at the time of the start of this research work. The 32nm transistor gate-length process technology SPICE model is adopted from Predictive Technology Model [10], hence V_{DD} in all simulations are set to 1.0V based on the transistor technology. The aims of this research are summarized in figure 1, where each block in the diagram is a circuit that needs to be designed using the same memristor model and simulation parameters as described.

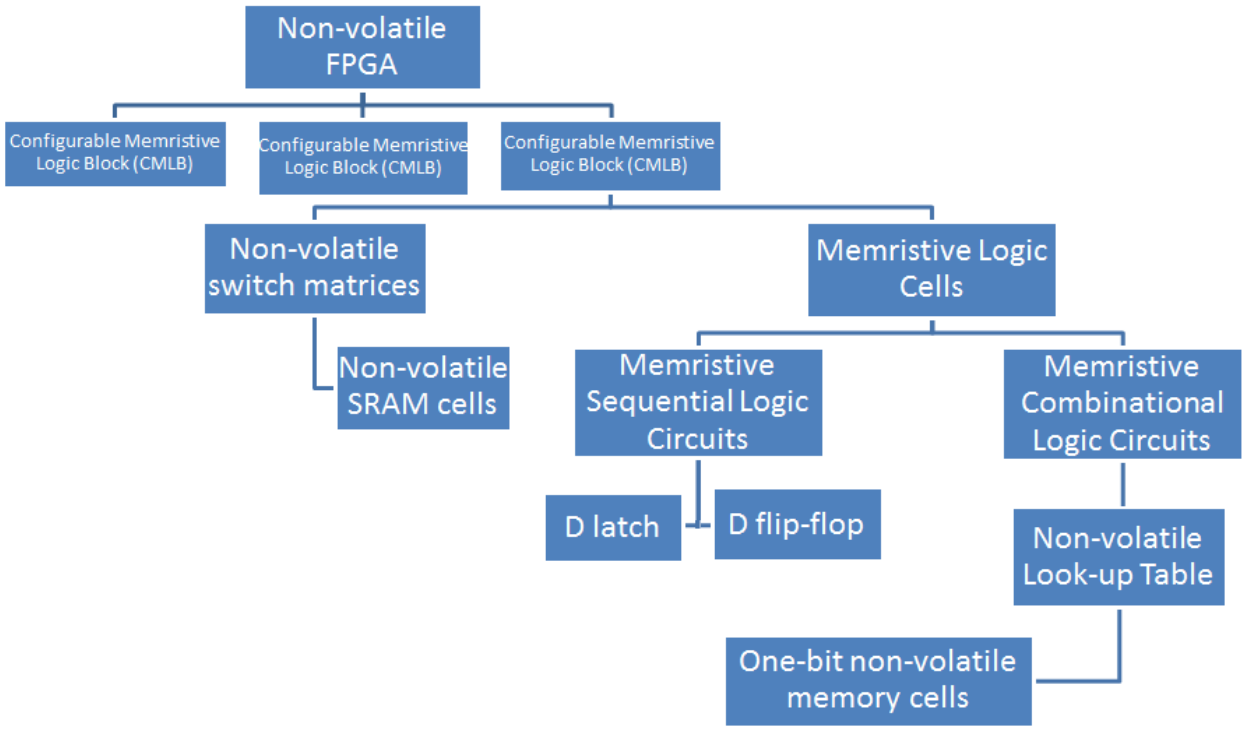

Figure 1. Summary of the aims of research.

1.4 Thesis outline

The literature review to the research work presented in this dissertation is described in chapter 2. The preliminaries include the types of FPGA architectures available in the literature and an overview of the CMOS-based FPGA architecture. The preliminaries also include the different types of non-volatile memory devices, and a brief background on the development of memristors. This chapter also explains the development of memristor modelling and SPICE memristor models. How previous researches have tried to improve on the FPGA architecture by using non-volatile memory devices are explained in this chapter. Further literature review is conducted on memristive sequential and combinational logic circuit, as well as previously proposed improvements on switch matrices. The research work that was conducted to provide a detailed comparison between TiO_2 and TaO_2 memristive devices is presented in this chapter also. This chapter concludes by explaining the electrical and physical factors that differentiate memristors.

Chapter 3 presents an enhanced SPICE memristor model is presented that is based on a previous SPICE memristor model that was found to be working differently from the theories of the memristor.

Chapter 4 presents two types of memristive sequential logic circuits, D-latch and D flip-flop, as well as their simulation results and analysis. Other memristive sequential logic circuits from the literature are also analysed and compared against the memristive sequential logic circuits.

In chapter 5, the research findings on combinational logic circuits are divided into two sections. The first section shows the construction of a non-volatile look-up table using a novel one-bit non-volatile memory cell that was designed using memristors and transmission gates. The memory cell was compared against other similar memory cells available in the literature. In the second section of chapter 5, two novel memristive logic gates are proposed (OR and AND). The analysis and simulation results are presented in this chapter. Additionally, a method to improve a previously published memristive logic circuit in the literature is also discussed and explained.

Chapter 6 introduces and discusses the general switch blocks and crossbar arrays. The arrangement of memristors in a crossbar array is also discussed in this chapter. A research was conducted to compare and analyse crossbars of memristor and phase-change memory cells. Upon these results, a memristive memory cell is designed to create a memristive switch matrix, which is presented in this chapter. Simulation experiments were conducted on this switch matrix memristive memory cell along with other similar memory cells found in the literature.

Subsequently, chapter 7 introduces the configurable memristive logic block (CMLB) that encapsulates all the research work presented in the previous chapters. The CMLB is a network of memristive logic cells (MLC), interconnected to each other using memristive switch matrices. The MLC comprises of the non-volatile look-up table and the memristive D flip-flop. The CMLB is then proposed to be used in a memristive-based FPGA architecture. This chapter also presents the simulation results and analysis of the MLC and CMLB using various FPGA test designs.

Chapter 8 provides the conclusion to this dissertation and the researches that has been conducted and presented. This chapter also discusses all the possible future researches that stems from this dissertation.

2. LITERATURE REVIEW

LITERATURE REVIEW

2.1 Field-programmable Gate Arrays (FPGA)

Field-programmable Gate Arrays (FPGA) are integrated circuits containing various types of resource blocks that are programmable and configurable to any manner desired by the programmer. Examples of resources that are built in FPGAs are built-in memory, clock generators, I/O interfaces, multipliers, arithmetic units, Digital Signal Processor (DSP), and logic blocks. Hardware description language (HDL) is used to program these resources to however a user wishes it to behave. The common SRAM-based FPGA architecture (figure 2) consists of logic blocks (LB) and control blocks (CB) interconnected to one another by switch blocks (SB).

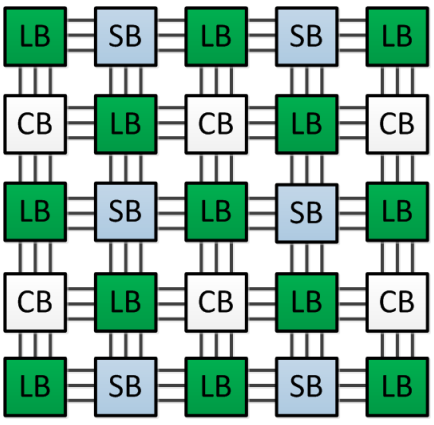

Figure 2. General FPGA architecture where logic blocks (LB) are interconnected with control blocks (CB) and switch blocks (SB).

Switch blocks contain switch matrices, where each switch matrix is a network of routing channels interconnected to one another via pass-transistors. Switch matrices complete the connections between blocks in an FPGA.

Logic blocks are the basic building block for memory storages in an FPGA. They are meant to provide an avenue for users to program logical functions, utilize built-in functions and modules, such as memory blocks, counters, and registers; or perform arithmetic functions. LBs can also be programmed to function as combinational logic circuits or sequential logic circuits in synchronous or asynchronous manner. Programmable logic blocks are also known as configurable logic blocks (CLB) whereas non-programmable logic blocks are called hard-wired logic blocks.

LBs are usually constructed from several logic cells (also known as configurable logic blocks (CLB), slice, or adaptive logic modules (ALM)), interconnected by programmable switch matrices, multiplexers and other logic components [11]. Multiple logic cells can be connected to each other to execute complexed logic functions. Each logic cell generally consists of look-up tables (LUT), multiplexers, full-adders, and D flip-flops. Logic cells are also called as Configurable Logic Blocks (CLB) [12], slice [13], Logic Elements [14] or Adaptive Logic Modules (ALM) [15], depending on the FPGA manufacturer.

In general, an LUT consists of memory cells which are addressed by the LUT inputs. A decoder is used to decode the LUT inputs to select and enable specific memory cells for programming or reading, and the output of the LUT is the logic

information stored in the accessed memory cell. The LUT functions as a programmable combinational logic circuit, where the LUT address inputs are analogous to the combinational logic circuit input, while the output of the combinational logic circuit is the logic information stored in the memory cell with the address that corresponds to the LUT input. Thus, LUTs are usually used to execute complex Boolean algebra functions.

Control blocks govern the operating functions of logic blocks and switch blocks. To perform this, CBs contain memory elements to store user-programmed information and use sequential logic circuits to channel appropriate control signals. These control signals configure the operation of the pass-transistors in the switch matrices and the functions of the LBs by enabling or disabling transistors, switches, multiplexers, and memory cells in the LBs and SBs. There are various types of control blocks in an FPGA to control different sections or resources of the FPGA. Some examples are clock control block [16], memory controller block [17], communication or Transceiver Reconfiguration Controller [18], and I/O control block [19], [20].

FPGAs are mainly used when designing or testing integrated circuits (IC) and electronic applications because FPGAs are easily programmable which gives short programming and testing times. This shortens debugging and verification processes. Conversely, Application Specific Integrated Circuits (ASIC) are non-programmable and does not allow flexibility in its applications. ASICs also take a longer time from designing stage to fabrication, and are expensive for low volume production.

The major concern for FPGAs is the high cost per chip and large device area required to manufacture a programmable integrated circuit. Furthermore, the amount of power consumption is higher in FPGAs than ASICs due to the various resources built into an FPGA chip to accommodate its programmable functionality. However, due to the emergence of 20nm and 16nm process technologies, FPGA devices are becoming smaller [21]–[23]. Moreover, various articles have also shown that the decreasing costs of FPGA could also lead to the possibility of FPGA replacing ASIC for medium to high volume production in the near future [1], [24], [25].

2.2 Types of FPGA

FPGAs are manufactured by semiconductor companies such as Altera (now Intel), Xilinx, Lattice Semiconductor, Microsemi, and QuickLogic. These manufacturing companies can be divided based on the switching technology used in the FPGA: Static Random-Access Memory (SRAM), antifuse or flash.

Out of the three types of switching technology, antifuse FPGAs have the densest structure but are not re-programmable [26]. Between SRAM and flash, where both are re-programmable, SRAM switching is faster than flash devices. However, flash switching technology consumes lower power consumption and has higher security. Moreover, flash devices are non-volatile, which enables logic information to be retained even after power is disconnected from the device. On the

other hand, SRAM-based FPGAs are usually manufactured with the same type of Complementary Metal–Oxide–Semiconductor (CMOS) technology with the rest of the integrated circuit chip, thus additional manufacturing processes are not required and the cost of fabricating SRAM-based FPGAs is reduced. This is the main reason for SRAM-based FPGAs dominating the FPGA market [9]. Therefore, the SRAM-based FPGA has been selected as the benchmark for comparison in this research work.

One of the disadvantages of SRAM-based FPGAs is the large SRAM devices which reduces the density of FPGA chips, compared to antifuse and flash devices [26]. Although SRAM devices are highly re-programmable, SRAM devices are volatile and lose logic information whenever power supply to the device is disrupted. Despite these disadvantages, SRAM-based FPGAs are widely used in various fields and are also reported to be used for security-related applications [27]. Due to the high demand for SRAM-based FPGAs, researchers have proposed several methods to improve or reduce the disadvantages of SRAM-based FPGAs [28]–[30].

A study was conducted on various architectures of SRAM cells used in FPGAs [28]. The purpose of the study was to propose a 9T SRAM cell with high data stability and low power consumption, but suffers from large device area and volatility. A novel FPGA architecture that uses controllable-polarity transistors was designed [29], which forms the basic building blocks of ultrafine grain cells. These ultrafine grain cells function as computational or logic cells and offers an improvement on the routing imbalance in traditional FPGA architecture [31], as well as reductions in delay and device area. Evolvable processing array-based FPGA

architecture constructed using Dynamic Partial Reconfiguration (DPR) was proposed [30]. This architecture applies evolvable processing array which features protection mechanism against permanent and transient faults, and improve processing quality.

Although these methods to improve SRAM-based FPGA show reliable results, they still use CMOS process technologies and researchers were motivated in breaking away from conventional CMOS devices. This give birth to resistive switching devices and subsequently, FPGA architectures have been proposed and designed using resistive switching devices, or non-volatile memory (NVM) devices, such phase-change memory cells [32], spintronic devices [33], and magnetoresistive memories [34].

2.3 Non-volatile memory (NVM) devices

Resistive switching devices or non-volatile memory (NVM) devices became a sought-after technology due to its relatively faster switching speed, higher endurance cycles, and smaller device area per component [35]. Researchers have also managed to fabricate flexible NVM devices [36]–[38]. Most of all, NVM devices are becoming increasingly popular due to their non-volatility properties, as well as multi-level storage capabilities [39]–[41]. NVM devices are also known as resistive switching devices because NVM devices use different resistance levels to indicate different logic information. The common context is to assign logic ‘0’ to the high

resistance state (HRS) and logic '1' to the low resistance state (LRS) of the NVM device. So far, the non-volatile memories that have been developed are:

(i) Phase-Change Memory (PCM) [42]

(ii) Ferroelectric Random-Access Memory (FeRAM) [43]

(iii) magnetoresistive memory (MRAM) [44]

(iv) Memristors

2.3.1 Phase-Change Memory (PCM) cells

PCM cells switch between resistance states by manipulating the phase of chalcogenide materials. Amorphous state of the chalcogenide material is highly-resistive (logic '0'), while crystalline state is of lower resistance (logic '1'). The phase change is attained by heating or cooling. Rapid cooling of chalcogenide causes the material to turn into amorphous state (HRS), while heating it below its melting point causes the chalcogenide to crystallize (LRS) [45]. The rate of cooling or heating is controlled by manipulating magnitude of input current and pulse width.

2.3.2 FeRAM devices

FeRAM devices use ferroelectric materials where an application of electric field across the device causes polarization in the form of small shifts in the atomic

dipoles. The atomic dipoles have the tendency to align themselves according to the electric field. Thus, the change in the distribution of electric charges in the ferroelectric material causes a change in resistance. The polarization would remain after electric field is removed and ferroelectric materials usually have only two stable polarized states, resulting in two different resistance states [46].

2.3.3 MRAM devices

In MRAM devices, the switching of resistance states in the material is induced by an application of magnetic fields. The device structure contains two magnetized layers sandwiched between two metal electrodes. One of it is a fixed magnetized layer, while another is a freely polarizable magnetized layer. The resistance state of MRAM devices are manipulated by controlling the magnetic orientation of the free layer using magnetic fields. Thus, the resistance of the MRAM devices is dependent on the polarization of the free layer in comparison to the polarization of the fixed layer [44]. If the polarization of the layers is parallel to each other, the device is in low resistance (LRS), and if they are not parallel, the device is in high resistance (HRS).

2.4 Memristor

The memristor was first theorized in 1971 by Prof. Leon Chua [47]. The four electrical quantities that relate the three fundamental passive circuit elements are voltage (V), current (I), charge (q) and flux (φ). Voltage is the rate of change of flux, while current is the rate of charge flow. Resistance is related by voltage and current, capacitance is related by voltage and charge, and inductance is related by current and flux. The only remaining relationship is between charge and flux. Thus, the fourth passive circuit element, known as memristor, was proposed to complete the network of relationships between the four fundamental electrical quantities (figure 3).

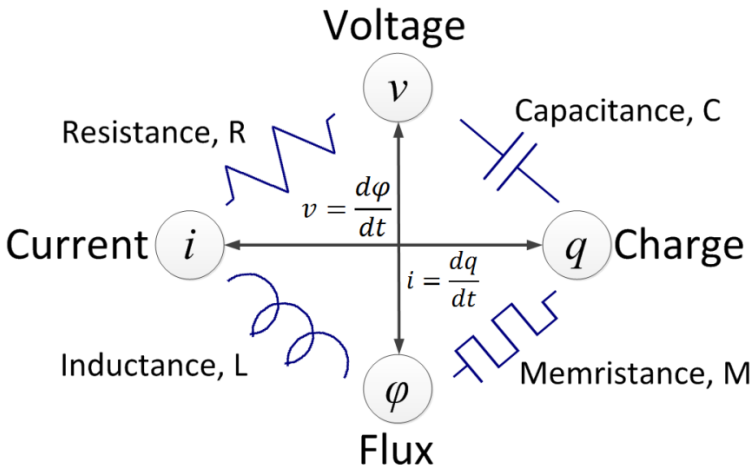

Figure 3. The relationship between the four fundamental electric quantities.

In 2002, a physical non-volatile memory device was developed by manipulating the resistance of bulk layer of the device, called as Resistive Random-Access Memory (ReRAM) using colossal magnetoresistance (CMR) materials [48].

CMR materials are usually manganite perovskites and the electrical resistance is manipulated using magnetic fields [49]. The ReRAM device has a two-terminal device with a bulk layer sandwiched between two metal electrodes. A bias potential is applied across the terminals which alters the physical composition of the bulk layer. The physical changes that occur cause a change in the resistance of the bulk layer and of the device. When no potential bias is applied, the bulk layer does not alter its physical composition due to the lack of energy required for physical changes to occur, thus leaving the device in its latest resistance state. This is the non-volatile characteristics of the ReRAM device. With the development of the CMR-ReRAM device, researchers have found a more convenient way to manipulate resistance by using electrical fields instead of magnetic fields [50].

In 2005, TiO_2 thin films were grown by atomic-layer deposition using platinum (Pt) as top and bottom electrodes, and titanium oxide (TiO_2) as bulk layer [51]. The electrodes are metals, which are conductive while the bulk layer of TiO_2 is highly resistive that makes it similar to an insulator layer. This structure mimics a Metal-Insulator-Metal (MIM) structure and the behaviour of this device is in good agreement with the memristor theory [47]. Around the same time, copper oxide (CuO_2) was used as the bulk layer to fabricate a device with MIM structure that also exhibits similar resistive switching behaviour [52]. This shows that MIM structures in general are able to exhibit resistance switching abilities. The resistance states of memristors (LRS and HRS) are also commonly known as memristance.

Since then, researchers have shown that other metal oxides could also be used as the bulk material to fabricate nanoscale memristive devices, such as zinc oxide (ZnO) [53], zirconium oxide (ZrO_2) [54], nickel oxide (NiO) [55], hafnium oxide (HfO) [56], niobium oxide (Nb_2O_5) [57], and vanadium oxide (VO_2) [58], tantalum oxide (TaO_2) [59], zinc tin oxide [60], bismuth ferrite ($BiFeO_3$) [61], and aluminium oxide (Al_2O_3) [62]. Resistive switching behaviour was also observed when semi-metal oxides are used as the bulk layer (silicon oxide (SiO_2) [63]). Some chalcogenides have also exhibited memristive properties such as germanium selenide (Ge_2Se_3) [64] and copper sulphide (Cu_2S) [65]. ReRAM and resistance-switching devices are also commonly coined as memristors [66] because the physical structure of MIM devices are similar to ReRAM devices. Moreover, functional behaviour of the ReRAM devices are in good agreement with a memristor [67]. Some authors may also abbreviate ReRAM as RRAM [68]–[70].

2.4.1 Advantages of memristor against other NVM devices

The introduction of RRAM devices (or memristors) has significantly attracted more attention than PCM devices because RRAM devices have better switching speeds than PCM. The writing time of RRAM devices is less than 20ns, while PCM devices require at least 100ns for writing time [53], [71]. PCM devices also use large amounts of heat energy during switching which significantly degrades endurance performances [71].

In comparison to MRAM devices, the physical structure of MRAM is larger than a typical RRAM device, where RRAM devices can be fabricated in a nano crossbar array structure [72]. The read time of FeRAM devices (100 ns) is much slower than Dynamic Random-Access Memory (DRAM) devices (40 to 70 ns) [43], which is a common memory device used in computers. It is also reported that are interface issues between Si and the ferroelectric material when fabricating FeRAM devices with current CMOS process technologies [73].

Between PCM, MRAM, FeRAM and memristors, memristors requires the least manufacturing steps to fabricate [74]. In addition, memristors are developed with simple fabrication processes and has high-density structure [75], as well as high compatibility with current CMOS process technologies [50]. Therefore, there are more research and developments in RRAM devices (memristors) than PCM, MRAM and FeRAM devices.

2.4.2 Types of memristors

Among the memristive devices that have been developed, TaO_2 is considered as one of the prospective resistive switching material due to its existence in only two stable phases (TaO_2 and Ta_2O_5) [76] which gives better control over the stability of the high and low resistance states. The TaO_2 and Ta_2O_5 layers in the TaO_2 memristor give rise to a Metal-Insulator-Semiconductor-Metal (MISM) structure. In addition, the fabricated TaO_2 memristors have exhibited better resistance switching

characteristics than TiO_2 memristors, in terms of switching speed (5 times faster), endurance (10^8 times more switching cycles) [77], and retention of at least 10 years backed by experimental results [78]. Due to these statistics, a detailed comparison between fabricated TaO_2 and TiO_2 memristive devices was conducted as part of this research to understand the requirements and factors to fabricate better performing memristive devices. TiO_2 memristors are selected as the benchmark for this comparison because the study and fabrication of TiO_2 memristors has been the most extensive among the different types of memristors available in the literature. The detailed comparison between TiO_2 and TaO_2 memristors is further discussed in sections 2.14 to 2.18 of this dissertation [79][80].

2.4.3 Applications of memristors

The objectives of using memristors in circuits are either to: (i) improve electrical and physical performance or (ii) introduce non-volatile function. To introduce non-volatile functions, the pioneer applications of memristors were proposals to replace flash memory [81] and DRAM to improve memory performance [82]. Subsequently, memristors are then used to improve electrical and electronic circuits, such as memory cells [83], filters [3] and amplifiers [84], by reducing device area. Other applications of memristors that were found in the literature include neuromorphic circuits [4], Van der Pol Oscillator [85], pH sensors [2], and crossbar arrays [86], which are commonly used in FPGA architectures. These

applications take advantage of the resistance switching behaviour of memristors to improve overall switching speed and energy.

2.5 The development of memristor models

Although there were heavy developments on RRAM devices, none have managed to relate it to the memristor that was proposed by Prof. Chua [47]. After many years since Prof. Chua's proposal of the memristor, the breakthrough came in 2005 where resistive switching mechanism was exhibited in TiO_2 thin films [51]. The article however did not directly relate the switching mechanism of the TiO_2 thin films to memristive behaviour. In 2008, a nano-crossbar array with MIM structure that shows similar behaviour to memristors was proposed and fabricated using TiO_2 as the bulk layer [87]. The hysteresis loop in the current-voltage curve and a current-voltage relationship that characterizes the current-voltage behaviour of memristor was subsequently presented [88]. A physical model based on the doping of TiO_2 in the bulk layer was also proposed for the basis of resistive switching mechanism.

According to the physical model proposed in [88], oxygen vacancies act as n-type dopant in TiO_2. Doping of TiO_2 with oxygen vacancies would cause the highly resistive TiO_2 layer to become less resistive. The asymmetric distribution of oxygen vacancies during doping process causes the TiO_2 layer to have regions of different resistances. The highly-doped region is less resistive, while the lowly-doped region

is more resistive. The drifting of oxygen vacancies from the region of highly-doped TiO_2 towards the oxygen-deficient region causes the overall resistance of TiO_2 to decrease [89], [90].

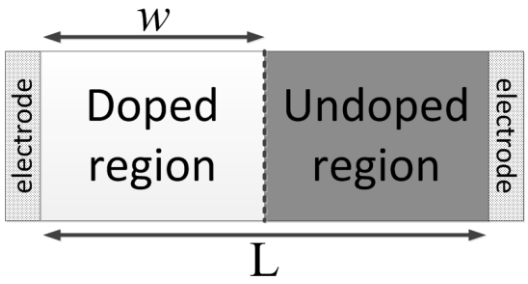

Figure 4. Barrier width in the bulk layer of MIM memristive devices.

Using the above explanation, the physical model presented in [88] have assumed that the bulk layer is divided into two regions of high and low resistance. This is illustrated in figure 4, where *w* represents the thickness of low resistance doped region of the bulk layer (also known as barrier width) and *L* is the total length of the bulk layer. The barrier width is modelled to sweep along the bulk length when voltage is applied, ranging from 0 to *L*. The drifting of oxygen vacancies and movement of barrier width along the bulk length are proposed to be linearly [88], and the rate of change of barrier width is defined as:

$$\frac{dw(t)}{dt} = \frac{\mu R_{ON}}{L} i(t) f(t) \quad (1)$$

where *i(t)* is the amount of current passing through the device and *f(t)* is a window function with respect to time. For the relationship between barrier width *x(t) = w(t)/L* and resistance, the state equation is also proposed by [88]:

$$R(t) = R_{ON}x(t) + R_{OFF}\big(1 - x(t)\big) \quad (2)$$

x represents the thickness of low resistance doped region of bulk layer (w) over the total thickness of bulk layer (L), giving $x = w/L$ and x ranges from 0 to 1. R_{ON} is the resistance of the device when it is in its LRS and R_{OFF} is the resistance of the device when it is in its HRS.

Equations (1) and (2) assume that: (i) the bulk layer does not have any other titanium oxide phases other than TiO_2 and Ti_4O_7, (ii) the device could be in any state of intermediate resistance, where the resistivity of the bulk can be between LRS and HRS, (iii) the drifting of oxygen vacancies or barrier width along the bulk length is linear and (iv) the resistance of the bulk layer is defined by the resistance of the highly and lowly doped regions of the bulk layer.

These assumptions have caused many researchers to propose other nonlinear simulation models [91]–[95] that contradict the linearity of this model. These other theories and simulation models also aim to reduce the assumptions of equations (1) and (2). Biolek [91] was the first published memristor model based on the physical memristor device [87]. However, the memristor model is very close to linear behaviour and does not allow flexibility in changing switching parameters. The most accurate memristor model is the Batas & Fiedler memristor model [92] due to the usage of magnetic flux controlled memristor model and it meet the requirements for simulations of multi memristor circuits. Other than that, the Batas & Fiedler model also allows other researchers to easily modify switching speed and boundary conditions in their SPICE model. Therefore, Batas & Fiedler has been selected for further improvement and used in this research work. Furthermore, the switching

mechanism in memristive devices has been proven to involve the formation and collapse of conducting channels, instead of the manipulation of barrier width in the bulk layer [96].

Another type of resistive switching process incorporates the tunnelling probability factor (TPF) between the semiconductor and the metal layers, which is based heavily on Schottky barrier modulation and tunnelling, where the majority charge carrier is electrons. Resistive switching behaviour based on Schottky barrier modulation differs from the conducting channel theories, but these switching behaviour have also been proven to be correct [97]–[99] and the memristor modelling for these type of switching process for MISM memristor devices has also been proposed [100]. However, at the time of this research, the conducting channel theory was used for memristor modelling due to the lack of MISM memristor models and memristor models that are based on the modulation of Schottky barrier.

2.6 Window functions

The drifting of oxygen vacancies is proposed to be nonlinear in physical devices due to the region of high and low resistance not being easily distinguishable in the bulk layer [101]. The electric field along the bulk layer is also nonlinear due to the asymmetric distribution of oxygen vacancies in the bulk layer, which further justifies the theories of nonlinear drift in the bulk layer [102]. Furthermore, the drift velocity of charge carriers is strongly affected by the varying resistance along the bulk layer [103]. This causes the drift velocity of the charge carriers to change non-uniformly as they approach or leave electrodes. It is also postulated that the change in drift velocity near the electrodes may also be due to the charge carriers moving into another medium of different charge density and resistivity. The nonlinear models have displayed simulation results which are closer in agreement to the physical memristive devices [101], [104], [105]. Therefore, the change of drift velocities of charge carriers when it approaches the boundaries is concluded to be nonlinear.

Several window functions, $f(x)$ were proposed to model the nonlinear change of the mobility of charge carriers when approaching electrode-bulk layer boundaries. The window functions proposed are summarized in table 1, arranged in chronological order.

Table 1. Proposed window functions for the behaviour of charge carriers approaching electrode boundaries.

Author(s)	Window function, *f(x)*
Strukov et. al. [88]	$f(x) = x(L - w)/L^2$
Joglekar et. al. [102]	$f(x) = 1 - (2x - 1)^{2p}$
Biolek et. al. [91]	$f(x) = 1 - (x - stp(-i))^{2p}$
Prodromakis et. al. [106]	$f(x) = 1 - [(x - 0.5)^2 + 0.75]^p$
Kvatinsky et. al. [107]	$f_{on}(x) = exp\left[-exp\left(-\frac{x - a_{on}}{p}\right)\right]$ $f_{off}(x) = exp\left[-exp\left(\frac{x - a_{off}}{p}\right)\right]$

The first window function to simulate the rate of change of charge carriers was proposed in [88]. The window function was improved by introducing a parameter *p* for generalization of nonlinear behaviour [102]. A larger value of *p* would cause the behaviour to be highly nonlinear, while a value of 1 would give a linear behaviour. However, both of these two window functions cause the barrier width to be stuck at the boundaries because these two window functions give the rate of change of barrier width ($\frac{dw(t)}{dt}$) a value of zero at the boundaries. Thus, the barrier width of the device cannot be adjusted further and *x* remains stuck at 0 or 1. For example, if *w* is at L, meaning *x* is at 1,

$$f(x) = 1(L - L) / L^2 = 0 \text{ (Strukov window function)} \quad (3)$$

$$f(x) = 1 - [2(1) - 1]^{2p} = 0 \text{ (Joglekar window function for any value of } p) \quad (4)$$

Substituting either of these values into equation (1) would result in a zero rate of change of barrier width. This causes the barrier width to be permanently stuck at 1 in this example.

In order to avoid the simulation of x being stuck at 0 or 1, a window function was proposed to be dependent of current [91], where:

$$stp(i) = \begin{cases} 1, & for\ i \geq 0 \\ 0, & for\ i < 0 \end{cases} \tag{5}$$

The addition of the *stp* function allows *f(x)* value to be non-zero, even though x is at 0 or 1. For example, if both p *a*nd x are 1, and current is positive ($i \geq 0$), *stp(-i)* equals to 0. This causes $f(x) = 1 - (1 - 0)^2 = 0$. But if a bias of opposing polarity is the applied, or current is negative ($i < 0$), *stp(-i)* equals to 1 and $f(x) = 1 - (1 - 1)^2 = 1$. This result in a non-zero rate of change of barrier width at the boundaries and the simulation of x does not stuck at 0 or 1.

Although the window function from [91] has solved the stuck-at issues and has parameter p for curve-fittings, it lacks scalability. A new window function that improves scalability giving a range of f_{max} where $0 \leq f_{\max}(x) \leq 1$ was proposed by [106]. The simulation of the barrier width does not stuck at 0 or 1, but it is still mathematically possible for x to be stuck at 0 or 1 with certain input parameters. Thus, the window functions for memristors can still be further improved.

2.7 Simmons tunnelling current density equation

Before the memristance state equation (1) was proposed, a tunnelling current density equation, known as the Simmons tunnelling current density equation, for an insulator layer sandwiched between two metals was proposed by J. G. Simmons [108] but was unused in previous simulation models. The advantages of this equation are: (i) it includes the behaviour of current that is dependent on the lengths of the insulator layer in MIM structures and (ii) applicable for a various range of voltages applied across the MIM structure. At hitherto, the most detailed expression relating the current and voltage behaviour for a generalized MIM structure is the Simmons tunnelling current density equation.

Currently, no physical devices correlate to equation 1 or any of the window functions in table 1. On the other hand, two publications have suggested close relations between physical memristive devices and Simmons tunnelling current density equation [63], [109]. Due to the window functions hitherto do not fit the Simmons tunnelling current density equation, a window function which correlates to the Simmons equation was proposed by [107]. The Kvatinsky window function fits Simmons equation but it lacks scalability and does not guarantee symmetrical behaviour. This means that according to their window function and depending on parameters, the rate of change of drift velocity of charge carriers moving towards one electrode may be different from towards the opposite electrode. They also introduced two more fitting parameters in the form of a_{on} and a_{off}, used to fit the model to the Simmons equation.

The Simmons tunnelling current density is given as:

$$J = \int_0^{E_m} D(E_x)\xi dE_x \tag{6}$$

where ζ is defined as:

$$\xi = \frac{4\pi qm^2}{h^3}\int_0^{\infty}[f(E) - f(E + eV)]dE_r \tag{7}$$

and $D(E_x)$ is a function of the probability of an electron being able to overcome the potential barrier posed by the insulating layer and penetrate through from one electrode to another. $f(E)$ and $f(E+eV)$ is the Fermi-Dirac functions for electrons following and against the potential barrier respectively, while dE_r is the integral with respect to the effective electron direction. The Simmons tunnel equation is the most accurate due to its consideration of distribution and drifting of electrons in both directions. However, the probability function $D(E_x)$ is ambiguous and difficult to obtain. Thus, further research is still needed for the modelling of the general memristive switching behaviour in MIM devices.

2.8 Memristor modelling for MIM devices

Various SPICE memristor models and various window functions have been published to simulate memristive behaviour of MIM devices [91]–[95] according to the memristor theory [47] and behaviour of physical memristor devices [88]. These memristor models are widely used in simulating various electronic applications due to the absence of memristor component in current Electronic Design Automation (EDA) software. The SPICE memristor models [91]–[95] are based on Bipolar Resistance Switching (BRS) mechanism similar to the characteristics exhibited by physical memristors, which conforms to the memristor theory [47] and behaviour of physical memristor devices [88].

Among the SPICE memristor models, it was observed that there is room for improvement in the Batas & Fiedler model [92]. This memristor model is versatile because it can accommodate a variety of window functions. At the time of writing, this memristor model is being cited by at least 156 other publications, which justifies its popularity and suitability in electronic applications. Thus, chapter 3 of this dissertation explains the research work that has been conducted to improve on the Batas & Fiedler SPICE memristor model. This SPICE memristor model is then used throughout the remainder of this research work [110].

In this SPICE memristor model, noise was not included into the simulation model because noise can be random and is also dependent on the application that uses the memristor. Furthermore, all the MIM memristor models that are available in

the literature review do not include noise into the SPICE memristor models. This is because noise in memristor has not yet been fully researched. Experimental data on the effect of noise on memristance switching behaviour is also not available in the literature. However, the effect of noise in memristor model is important and could be included into future researches.

The SPICE memristor models found the literature are based on MIM devices [91]–[95] that switch memristance states by forming and collapsing conducting channels in the bulk layer. However, a more accurate MIM memristor model based on the modulation of Schottky barrier is in development and has been placed for future research.

2.9 Memristor modelling for MISM devices

For MISM memristive devices, the tunnelling current density for insulator layers thinner than 5nm is given as [111]:

$$J = A^{*}T^{2}exp\left(-\alpha_T d\sqrt{q\phi_T}\right)exp\left(\frac{-q\phi_B}{kT}\right)\left[\exp\left(\frac{qV}{\eta kT}\right)-1\right] \quad (8)$$

This equation involves the thermionic-emission for Schottky barrier and includes a tunnelling probability term, $exp\left(-\alpha_T d\sqrt{q\phi_T}\right)$. A^{*} is Richardson constant, q is electron charge, V is voltage applied, T is temperature, k is Boltzmann constant, ϕ_T is the effective barrier height, d is insulator layer thickness and α_T is the base transport factor term. α_T approaches 1 if the effective mass in the insulator is equals to the free electron mass. The Schottky barrier height ϕ_B term exists in the tunnelling current density equation due to the movement of charge carriers between metal and semiconductor through a very thin insulator layer mimics that of a Schottky-barrier diode. Ideality factor, η is close to the value of 1 when the amount of doping in the insulator layer is small, and becomes a larger value when doping increases. Using this equation, a simulation model has been developed and it matches the characteristics displayed by physical TaO_2 devices [112].

Increasing the thickness of Ta_2O_5 layer decreases the amount of current flow through the device in both LRS and HRS [113], which is also shown in equation 8 that current density J is inversely proportional to insulator layer thickness d. Therefore, the equation 8 is in good agreement with the results from experiments of physical MISM memristive devices.

2.10 Development of FPGA architectures

Current FPGA architectures use CMOS-based memory cells and logic circuits as the fundamental building blocks. In memristive-based based FPGA architectures, these memory cells and logic circuits are replaced with memristive-based memory cells and logic circuits. Alternatively, memristive-based memory cells and logic circuits can also be constructed using a novel memristor cell. For example, PCM cells were used to construct a switch matrix that is used in FPGA architectures [32], spintronic devices were used to design a non-volatile LUT for FPGA [33] and magnetoresistive memories were used to design switch matrices and sequential logic circuits [34]. There are also memristive-based FPGA architectures that have been previously proposed by other researchers [114]–[119].

A Generic Memristive Structure (GMS) was proposed and used to design a multiplexer and memory structure [114], while a memory cell was proposed to create a configurable logic block and memristors are used to replace interconnect elements [117]. Similarly, an NVSRAM was also used to create memristive-based logic, control and switch blocks [116]. The mrFPGA proposed in [115] created a generic memristive-based placement of logic and switch blocks, as well as memristive interconnects. Memristors were also used to design 3-D memristive-based FPGA architectures as a method to increase density and decrease routing delay [118], [119].

Apart from using PCM cells [32] spintronic devices [33] and MRAM [34], FPGA architectures can also be built using memristors [114]–[119]. These memristor-based FPGA architecture designs have shown improvements against the SRAM-based FPGA architecture. The Generic Memristive Structure (GMS) for non-volatile FPGAs [114] presented GMS-based multiplexer and GMS-based memory for implementation in the non-volatile FPGA. The article has clearly explained the programming and reading processes of the memristors. The GMS for non-volatile FPGA reduces device area by 7% and shortened critical path delay by 58%. However, power consumption of the GMS for non-volatile FPGA requires additional research. The mrFPGA was proposed in response to other works on FPGAs that uses emerging resistive switching technologies [115]. The mrFPGA is based heavily on memristor routing structure that showed vast improvements with reduction of 5.18 times of device area, 2.28 times of delay, and 1.63 times lesser power consumption. However, in the mrFPGA architecture, the memristive switch blocks circuit design with complete read/write control circuit is not presented.

The RRAM-based FPGA have proposed an NVSRAM to be used in the architecture [116]. However, the RRAM-based FPGA uses more device area (26%) than SRAM FPGA. A Hybrid CMOS-Memristor based FPGA Architecture [117] was discussed in detailed about device area and power reduction against SRAM FPGA. This architecture uses memristive crossbar, but has been reported to have high leakage current [120]. An FPGA based on Integration of CMOS and RRAM [118] provided comprehensive qualitative analysis for device area, power consumption, and critical path delay for its architecture with various benchmark circuits used in its analysis and the results are compared against SRAM FPGA. The

article also proposed several memristive memory cells for use in the FPGA architecture [118]. However, this design uses 1T1R structures which consume more voltage than SRAM cells. This is due to NMOS pass-transistors not being able to effectively pass voltages.

The Non-volatile 3D stacking RRAM-based FPGA showed promising results with 62.7% reduction of device area and 34% less delay [119]. However, the 3D stacking FPGA is placed for future research, as the simulation resources available for this research work allows for 2D simulations only.

For this research work, a novel configurable memristive logic block (CMLB) is constructed and proposed to replace current configurable logic blocks, as presented in chapter 7 of this dissertation. The CMLB comprises of novel memristive logic cells (MLC) interconnected with one another using non-volatile switch matrices, which are built using novel 7T1M SRAM cells. The MLC comprises of a non-volatile look-up table (NVLUT), multiplexer, and memristive D flip-flop (MDFF). Therefore, the development of the MDFF, NVLUT, and non-volatile switch matrix requires further literature review into previous works that are related to memristive sequential logic circuits, memristive combinational logic circuits, and memristive crossbars.

2.11 Sequential logic circuits

Although CMOS sequential logic circuits have fast switching times, they are volatile. Therefore, novel memristive sequential logic circuits (MSLC) are proposed and are presented in chapter 4 of this dissertation, which are able to store logic information without power supply.

In this research, only the D-latch and D flip-flop are considered and the CMOS D-latch and D flip-flop are shown in figures 5(a) and 5(b) respectively. These two circuits are the most frequently used sequential logic circuits in FPGAs. However, the improvement on other types of latches and flip-flops has been placed for future research, such as SR NOR latch, SR NAND latch, JK latch, T flip-flop, and JK flip-flop.

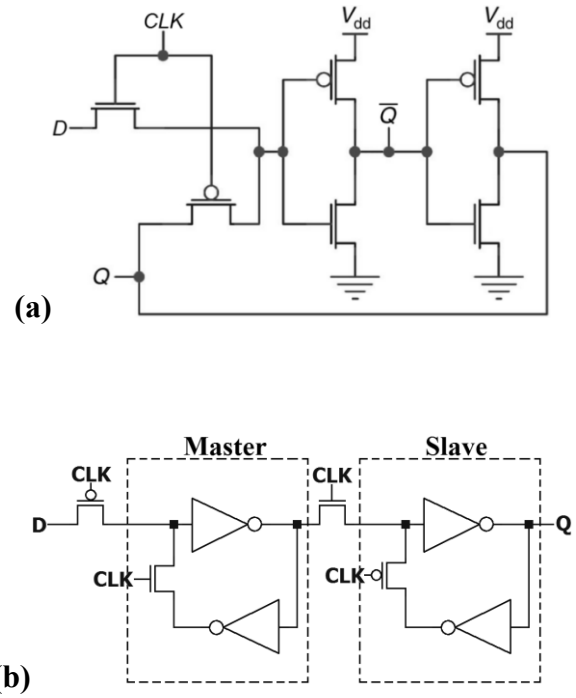

Figure 5. CMOS sequential logic circuits. (a) CMOS D-latch (b) CMOS D flip-flop

Previously published memristive sequential logic circuits have been simulated and tested to be working correctly but faced several issues. The Zero-Sleep-Leakage Flip-Flop Circuit [121] reduces switching power up to 97% but the circuit uses 26 transistors, 2.17 times more transistors than the CMOS flip-flop (12 transistors). This requires at least twice the amount of device area to fabricate the Zero-Sleep-Leakage Flip-Flop Circuit. The 8T2R Nonvolatile Latch [122] has the smallest device area among memristor-based latch circuits with only 8 transistors per latch. However, the terminals of the memristors RL and RR are connected to the same bit-lines, BL (bit-line) and BLB (bit-line bar) of the circuit respectively. Hence, the potential difference across the memristors is very small and the speed of resistance switching in the memristors is reduced. The memristor-based latch circuit proposed in [123] showed promising results, but uses three switches per latch, which may require complex programming of the latch circuit, as well as large device area.

Although these proposed circuits meet their objectives to function as non-volatile sequential circuits, there are several aspects which these circuits can be improved on, which are: (i) device area, (ii) resistive switching delay, and (iii) simpler programming of the latch circuit.

2.12 Combinational logic circuits

Current LUTs are constructed with flash RAM and these CMOS memory cells consume an average of 26.5fJ when accessed for writing or reading and the switching delay is 5.6ns (simulation results from section 5.5 of this dissertation). The major issue with these memory cells is that they are volatile and lose logic information when power is removed from the LUT. To overcome this, non-volatile one-bit memory cells were designed and proposed as a replacement for the CMOS memory cells that are used in LUTs [124]–[126]. This ensures that the logic information is retained after power loss. By retaining logic information, the LUT does not require programming to retain its intended behaviour and thus, avoids restoring time. Storing non-volatile logic information also reduces power consumption.

Several one-bit non-volatile memory cells are found in the literature which are suitable to be used in the LUT to create a non-volatile look-up table [124]–[126]. The 1 transistor 1 memristor (1T1M) memory cell is one of the smallest memristive one-bit memory cell using only two components in its design [124]. Although the 1T1M memory cell was designed to have one of its memristor terminal grounded which requires a bipolar voltage source to create voltage levels larger and smaller than 0V, it is noticed that dynamic ground method of voltage supply for the 1T1M memory cell is also possible, where a unipolar voltage source is inverted to create a complementary voltage source at the other end of the memory cell. However, it is also researched that the 1T1M memory cell uses an NMOS pass-transistor would

consume a fraction of the input voltage, thus leaving lesser amounts of voltage for the memristor, which slows the resistive switching process in the memristor.

Likewise, the 2 ambipolar transistors 1 memristor (2A1M) [125] memory cell uses one pass-transistor and one ambipolar transistor at each end of the memristor. This results in the input signal travelling through four other components apart from the memristor, which results in larger amounts of voltage loss. This means that the switching time is slower than the 1T1M memory cell.

The 3 transistors 2 memristors (3T2M) [126] memory cells does not invert the input voltage to create a complementary voltage as the reference at the opposite end of the memristor. Instead, the 3T2M memory cell uses $V_{DD}/2$ and $V_{DD}/4$ references. The use of $V_{DD}/2$ and $V_{DD}/4$ voltage references in the 3T2M memory cell requires more circuitry which results in larger device area and higher energy consumption.

Therefore, it is noticed that although the 1T1M, 2A1M and 3T2M memristive memory cells have efficient read and write processes, the disadvantage is the reduced potential difference across the memristor, which decreases switching speed and increased energy consumption, as well as a larger device area usage. The 2TG1M memory cell [83] have addressed these issues by using transmission gates, which increases the amount of potential difference dropped across the memristor and thus, improving switching speed and reducing energy consumption.

The multiplexers in logic cells are made up of logic gates, which may be improved by using Memristive Ratioed Logic (MRL) [127]–[131]. These MRL circuits were proposed to replace CMOS logic gates, where memristors are used to fully replace transistors. MRL circuits have shown that they have the capability to replace CMOS logic gates. The MRL circuits have exhibited excellent improvements against CMOS logic gates in terms of device area and energy consumption. However, it is hypothesised that the output logic is heavily dependent on the connection of input supply to the MRL circuit. This hypothesis is investigated in chapter 5.7 of this dissertation.

2.13 Crossbar topology

Another advantage of memristors is the ability to fabricate it into a crossbar topology. The memristive crossbar topology is an array of memristors, made up of two layers of parallel metal wires arranged perpendicularly on top of each other. The programmable interconnects (figure 6) are then placed at the intersection of these metal wires.

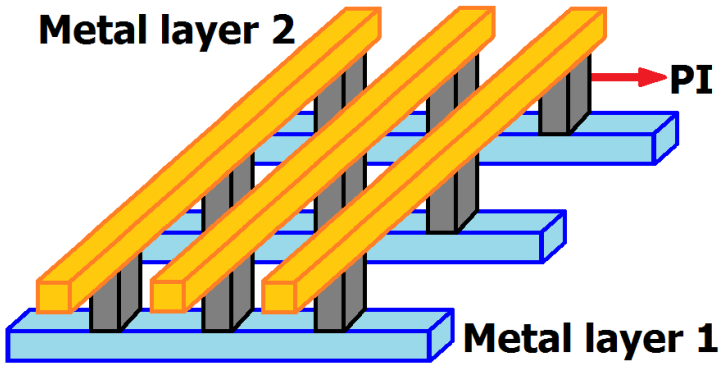

Figure 6. Structure of a crossbar array with programmable interconnects (PI) or vias connecting the intersections between metal layer 1 and metal layer 2.

Recently, there are several research publications that propose the use of memristors in crossbar arrays [132]. Memristive crossbars are generally constructed by fabricating memristors at the interconnections between the metal wires. The general structure of a memristive crossbar is shown in figure 7. It can also be observed from this diagram that the width of a memristor is as wide as the metal layer width, which is smaller than a transistor by at least 2 times.

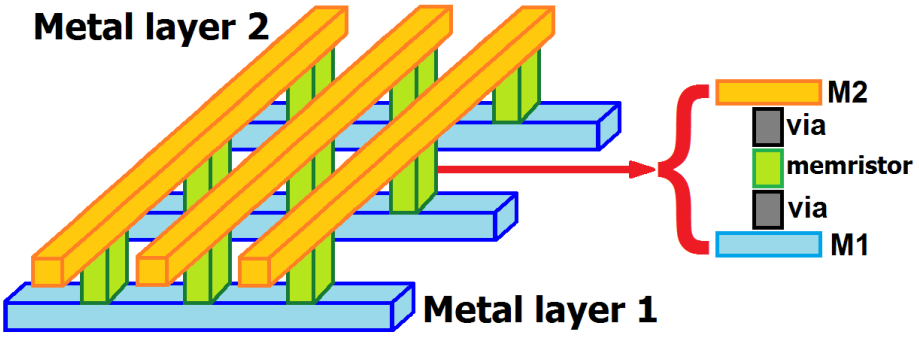

Figure 7. Structure of memristive crossbar where memristors are fabricated in the vias between metal layers.

However, there are also research works that highlights the issue of leakage current in memristive crossbars [133]. This is due to the parallel paths that currents can flow through when reading one memory cell in the crossbar (figure 8). Due to this, a research proposed using PCM cells in the crossbar array would improve the leakage current issue in crossbar arrays [134]. Therefore, simulation experiments were also conducted to perform a comparison of the leakage current in memristive crossbar and PCM cells crossbar [135].

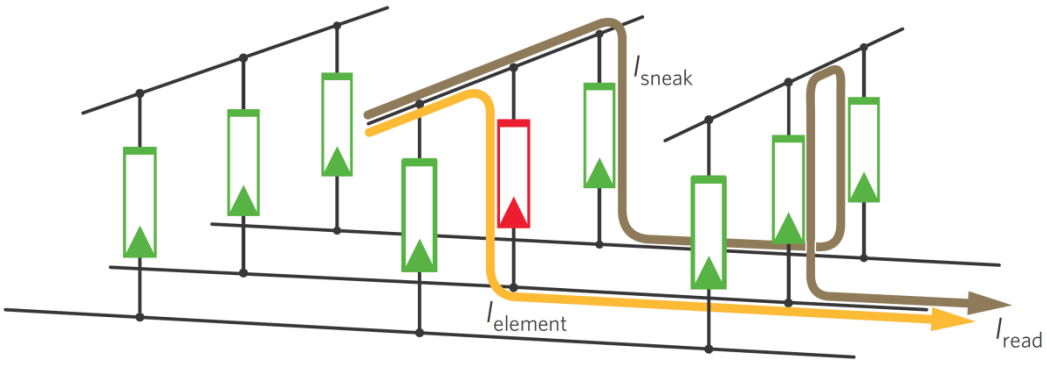

Figure 8. Leakage current (also known as sneak current) issue in crossbar array [133]**.**

Due to the issues of leakage current in crossbar arrays, researchers have proposed memristive SRAM cells which are suitable to replace the volatile CMOS 6T SRAM cells as the logic storage of the switch matrix [136]–[139]. This converts the volatile switch matrix into a non-volatile switch matrix, where the configuration of the switch matrix will be lost in the event of power interruption.

Among the memristive SRAM cells in the literature [136]–[139], the 4T2M cell [136] uses the least device area, but has high energy consumption due to current constantly flowing through two memristors when in operation. Similarly, the 7T2R cell [137] also has current constantly flowing through two memristors in series, which also causes high energy consumption. Energy consumption and switching delay are improved in the NVPG cell [138] by adding pass-transistors to control the current through the memristors. However, this comes at the cost of larger device area. The rSRAM cell [139] uses the largest device area due to 10 transistors and 4 memristors used per rSRAM cell. This amounts to unfavourable ratio of logic information per device area.

2.14 General device structure of TiO_2 and TaO_2 memristors

The physical structures of TiO_2 and TaO_2 memristors are shown in figures 9(a) and 9(b) respectively. TiO_2 memristors have a substrate of TiO_{2-X} bulk layer sandwiched between two Pt electrodes, resembling Metal-Insulator-Metal (MIM) structures [67]. In contrast, TaO_2 memristors have two layers in the substrate, as compared to the TiO_2 memristors containing only one layer (TiO_{2-X} bulk layer) in the substrate. The TaO_2 memristor has a layer of insulator Ta_2O_{5-X} fabricated above a semiconductor TaO_{2-X} bulk layer. The top Pt electrode is directly deposited over the Ta_2O_{5-X} layer [140]. Therefore, TaO_2 memristors resemble Metal-Insulator-Semiconductor-Metal (MISM) structures.

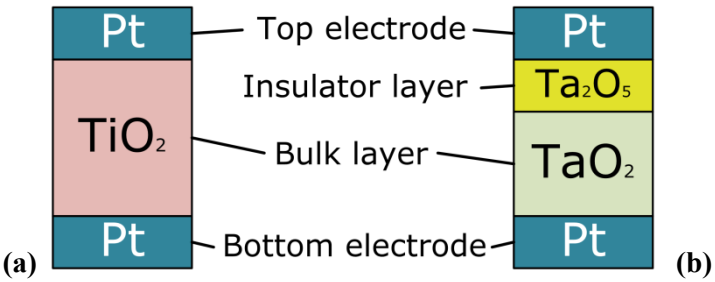

Figure 9. Typical construction of memristive devices. (a) Titanium oxide memristor with TiO_2 bulk layer. (b) Tantalum oxide memristor with TaO_2 bulk layer and Ta_2O_5 insulator layer.

The purpose of the insulator Ta_2O_5 layer in the substrate of TaO_2 memristors is to convert the device into a bipolar resistive switching device because TaO_2 MIM structures exhibit unipolar resistive switching [141], [142]. The difference between unipolar and bipolar resistive switching is explained further in section 2.16 of this dissertation. On the other hand, Ta_2O_5 MIM structures are not suitable for bipolar

resistive switching owing to the highly resistive Ta_2O_5 layer forming a very high Schottky barrier with the metallic Pt electrodes. Thus, a large reverse bias may be required to overcome the high Schottky barrier. Consequently, very large amounts of energy are needed to perform resistive switching in Ta_2O_5 MIM structures.

In the Ta_2O_5/TaO_2 MISM structure, the TaO_2 layer functions as an oxygen vacancy supply layer whereas Ta_2O_5 functions as an oxygen vacancy accumulation layer [143]. Although the fabrication of TaO_2 memristive devices require an additional layer of Ta_2O_5, it serves as an advantage because the variation of the thickness of the insulator layer in the substrate provides an easier manipulation of resistance ratio between R_{OFF} and R_{ON} [113].

By using the Ta_2O_5/TaO_2 MISM structure instead of an MIM structure, and by selecting each of these layers to have the desired resistance levels and ratio, the Ta_2O_5/TaO_2 structure has two additional two factors that can be manipulated: programming current and device stability [113]. The MISM memristor structure reduces the LRS current by maintaining a medium resistance during the switching between LRS and HRS [113]. The low-current operated devices (<100 μA) are necessary for better Random-Access Memory (RAM) applications [76].

Despite having different device structures and bulk layer materials, both TiO_2 (MIM) and TaO_2 (MISM) memristors exhibit similar resistive switching behaviour. This is evident by the fact that both devices are able to switch between high and low resistance states and the switching of resistance states depends on the direction of current, demonstrating similar bipolar switching behaviours.

2.15 Electroformation of NVM devices

Post-fabricated MIM structures may not be able to exhibit resistive switching behaviour because insulator bulk layers are highly resistive in normal operating conditions. To form a device capable of conducting current, electroformation is performed, which is an irreversible one-time process that forms a device capable of conducting current. This is usually done by applying an electrical potential large enough to cause physical changes to the device and form conducting channels through the bulk layer, which reduces the resistance of the bulk layer. It is essential for MIM structures to undergo electroformation in order to exhibit memristive behaviour [144], [145].

The magnitude of electroforming voltage is usually much larger than the switching voltage magnitude required for subsequent resistance switching to take place [146]. The electroforming voltage magnitude also usually exceeds the breakdown potential of the device, causing a build-up or depletion of oxygen ions at the electrodes, depending on the polarity of electroforming voltage. Subsequent physical switching mechanisms take place around these erupted regions, where conducting channels are formed and collapse near these regions [147].

During electroformation, the potential bias applied at the electrodes energizes the oxygen ions of negative charge to drift to the electrode that is applied with a more positive voltage. Oxygen ions combine to form oxygen gas molecules. The oxygen gas molecules are trapped in the interface between the electrode and bulk

layer. Gas pressure builds up as more oxygen gas molecules are formed. This eventually causes an eruption through the top electrode and a permanent physical deformation occurs in the memristive device [148].

Although there is permanent physical change to the device during electroformation, subsequent resistance switching after electroformation is not affected by the physical damage. This is due to the subsequent conducting channels that are responsible for the conduction of current are being formed and collapsed near the electroformed conducting channels [149], [150]. Thus, no further deformations or physical changes at other regions are required [150]. The theories that were proposed to explain electroformation in MIM devices are:

(i) Gibbs free energy of formation

(ii) Dearnaley theory

2.15.1 Gibbs free energy of formation

According to the Gibbs free energy of formation [146], the electroforming voltage is given by:

$$V_F \cong \Delta G_{MX} x F \tag{9}$$

where ΔG_{MX} is the Gibbs free energy of formation of the bulk layer material and F is Faraday's constant. The proposed theory by Greene et al. states that the electroforming voltage is independent of bulk layer thickness [146], giving equation (1). According the equation, the amount of voltage required to electroform a device is proportional to the Gibbs free energy of formation of the bulk layer material. This theory can be used to compare two devices of similar physical dimensions but different bulk layer material. The Gibbs free energy of formation of metal oxides commonly used in the bulk layer of MIM resistive switching devices is shown in table 2 [151].

Table 2. Gibbs free energy of the formation of metal oxides used in MIM resistive switching devices.

Metal Oxide	Gibbs free energy of formation, $\Delta_f G°$ (kJ/mol)
Hafnium oxide (HfO)	-1088.2
Zirconium oxide (ZrO_2)	-1042.8
Titanium oxide (TiO_2)	-888.8
Silicon oxide (SiO_2)	-856.4
Vanadium oxide (VO_2)	-446.4
Nickel oxide (NiO)	-211.7
Tantalum oxide (TaO_2)	-209.0
Copper oxide (Cu_2O)	-149.0

From table 2, it is observed that the Gibbs free energy of formation of TaO_2 and Cu_2O are among the lowest whereas HfO and TiO_2 are among the highest. Between TaO_2 and Cu_2O, TaO_2 is more widely used over Cu_2O due to its more stable resistance states as seen in the current-cycle and resistance-cycle graphs of TaO_2 and Cu_2O memristive devices [52], [78], [152]. An example of resistance-cycle for TaO_2 and Cu_2O memristive devices is shown in figures 10(a) and 10(b) respectively. Other researchers have also shown that the smaller difference of the Gibbs free energy of formation between TaO_2 and Ta_2O_5 phases produces more stable resistive switching behaviour [76].

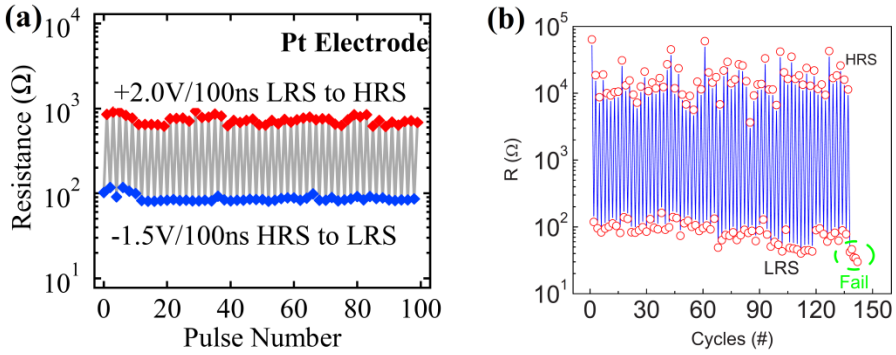

Figure 10. Resistive switching in memristive devices of (a) TaO_2 and (b) Cu_2O

Although memristors with bulk layers of high Gibbs free energy of formation may also exhibit resistive switching behaviour, these devices require an additional one-time electroformation step. This is reflected by TiO_2 devices requiring an electroformation process that requires a large electroforming potential before TiO_2 devices can exhibit resistive switching behaviour [148]. As TiO_2 devices mimics an MIM structure, many publications have reported that other MIM structures of different materials also require an electroforming step to exhibit memristive behaviour [153], [154].

In contrary, TaO_2 devices with similar physical dimensions as TiO_2 devices would require ~4.5 times less energy for the electroforming process because the Gibbs free energy of formation of TaO_2 is ~4.5 times smaller than the Gibbs free energy of formation of TiO_2. Moreover, if the Gibbs free energy of formation is very small, it is postulated that the electroforming voltage is less than or equal to the switching voltage of the memristive device. The damage to the device is insignificant and the electroformation process could be part of the first switching cycle. This avoids the need of a large voltage for a separate electroforming process. This was reported in a TaO_2 memristor where no additional electroformation step was required [155]. It was also observed that the voltage of the first switching cycle is lesser than the voltage of the subsequent switching cycles [155].

Research also shows that the electroforming voltages of physical TiO_2 and TaO_2 devices are proportional to bulk layer thickness [141], [156]. This may be in contradiction to Greene's theory. Thus, it is reinstated that Greene's theory is applicable only if the devices in comparison are of the same physical dimensions. For comparing devices that have different physical dimensions but similar bulk layer material, the Dearnaley theory would be more appropriate [157].

2.15.2 Dearnaley theory

Dearnaley et al. proposed that the electroforming voltage is proportional to insulator thickness in MIM devices [157]. The electric field applied during electroforming, E_F is the amount of voltage supplied per insulator thickness:

$$E_F = {}^{V}/_{L} \tag{10}$$

where V is the voltage applied across the device and L is the thickness of the substrate of the device.

Voltage connected to the electrodes is applied across the entire bulk layer surface. Owing to the insulator-metal interface not being completely smooth, there is a possibility that some regions in the bulk layer are thinner than the intended length of the bulk layer. Since electric field is inversely proportional to insulator thickness (equation 2), the electric field is larger at the regions of thinner bulk layer. At these high electric field regions, electroformation is more likely to occur and thus forms a conducting channel at these regions. The Dearnaley theory also explains why conducting channels in TiO_2 and TaO_2 devices are not spanned across the entire bulk layer [158].

Bulk layers or insulators thicker than 1 μm cannot be electroformed due to insufficient electroforming electric field applied across the bulk layer [67], [146], whereas devices thinner than 10 nm may suffer from permanent dielectric breakdown due to the high electric field [159] or due to large amounts of current flow [160], [161]. Thus, current compliance methods are used to avoid a permanent

breakdown or excess physical damage during the electroformation of devices with bulk layer thinner than 10nm [162].

2.15.3 Preventing electroformation in memristive devices

To exhibit resistive switching behaviour in TiO_2 devices without electroformation, two methods were proposed: (i) thinning bulk layer to a few nanometres thick while using current compliance methods [148], and (ii) depositing bulk layer by reactive sputtering in oxygen rich ambient [163], because electroformation of metal-oxide memristors has been shown to be assisted by oxygen vacancies [164]. Reducing device size also decreases the physical damages caused by oxygen gas eruption because smaller devices increases the rate of release of oxygen molecules out of the device [148].

To prevent electroformation in TaO_2 devices, the top electrode Pt is proposed to be replaced with Ta [77]. Although a different electrode is used, the device still behaves with similar memristive properties [155]. Using magnetron sputtering method, TaO_2 devices still exhibit memristive behaviour without electroformation [143]. This shows that TaO_2 devices can exhibit memristive behaviour without the need for an additional electroformation process.

2.16 Resistive switching mechanism

After fabrication, and performing electroformation if necessary, memristive devices can undergo resistive switching cycles. The resistive switching mechanism is dependent on whether the device is of MIM or MISM type of structure. There are also two types of resistive switching mechanisms; unipolar resistive switching (URS) and bipolar resistive switching (BRS) mechanisms, which can either occur in MIM or MISM type of structure.

2.16.1 Unipolar Resistive Switching (URS)

In URS devices, the switching operation is selected by controlling voltage magnitude and length. URS switching does not depend on the polarity of the applied voltage, as shown in figure 11 [165].

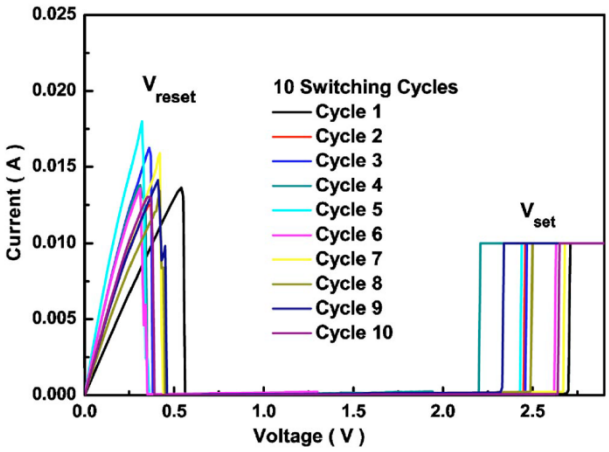

Figure 11. Unipolar Resistance Switching observed in ZrO_2 resistive switching device [165].

URS switching operation depends on the amount of energy supplied to the ions in the bulk layer. Thus, it is independent of the direction of energy flow, but dependent on the magnitude of energy supplied, which is proportional to the magnitude of applied voltage and the duration of applied voltage [166]. However, URS devices did not gain as much attention due to BRS devices having faster switching speeds and requiring lower switching energies [53][67]. Furthermore, URS devices are not in agreement with the theory of memristors [47], which states that switching of memristive devices require opposing polarities of voltage.

2.16.2 Bipolar Resistive Switching (BRS)

The BRS mechanism is a switching mechanism that requires opposing voltage polarities for different switching operations (turning ON or OFF). BRS can be further differentiated into two types; (i) clockwise BRS (figure 12), where positive polarity turns device OFF, and (ii) counter-clockwise BRS (figure 13), where positive polarity turns device ON. The voltage polarities for device switching operations (clockwise BRS or counter-clockwise BRS) are interchangeable depending on its fabrication process [167].

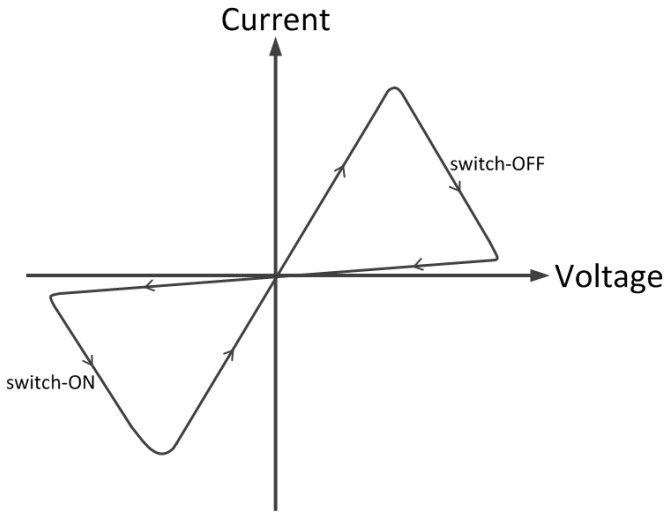

Figure 12. Current-Voltage curve for clockwise bipolar resistance switching.

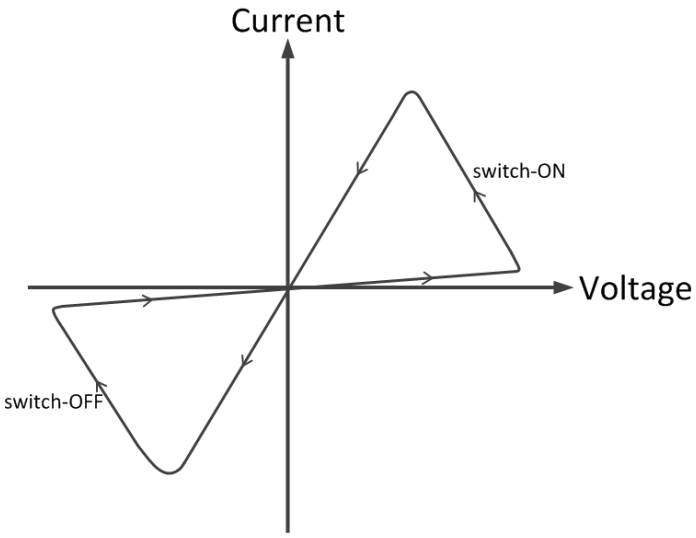

Figure 13. Current-Voltage curve for counter-clockwise bipolar resistance switching.

The BRS of TiO_2 memristive devices resembles that of other MIM memristive devices [168]. Thus, the general BRS mechanism of MIM memristive devices can be explained by studying the switching mechanism of TiO_2 memristive devices. Similarly, the BRS mechanism of MISM memristive devices can be explained by studying the switching mechanism of TaO_2 memristive devices.

During fabrication of memristive devices with metal oxide bulk layers, oxygen ions are injected into the bulk layer as a doping process. This process is uneven and the distribution of oxygen ions (and vacancies) are asymmetrical in the bulk layer [169], [170]. This contributes to the memristive properties of the device. The defect states induced by oxygen vacancies act as n-type dopant in TiO_2 and the highly resistive TiO_2 layer becomes more conductive. The asymmetric distribution of oxygen vacancies also causes the TiO_2 layer to have regions of high and low resistances. The highly-doped region is less resistive, while the lowly-doped region is more resistive. Due to the asymmetric doping of bulk layer, only one of the electrodes dominates the switching mechanism. The formation and collapsing of conducting channels takes place nearer to one of the electrodes that dominates the switching cycles [51]. The electrode that is nearer to the higher resistive region of the bulk layer is the electrode that dominates the switching cycles. The region where switching cycles take place in the bulk layer or the electrode that dominates the switching cycles is determined during fabrication [113], [167].

2.16.3 MIM memristive device switching mechanism

The switching mechanism in TiO_2 devices involves the dislocation of the charged species, ions or vacancies, of the metal-oxide towards or away from an electrode. This process either forms or collapses conducting channels [171].

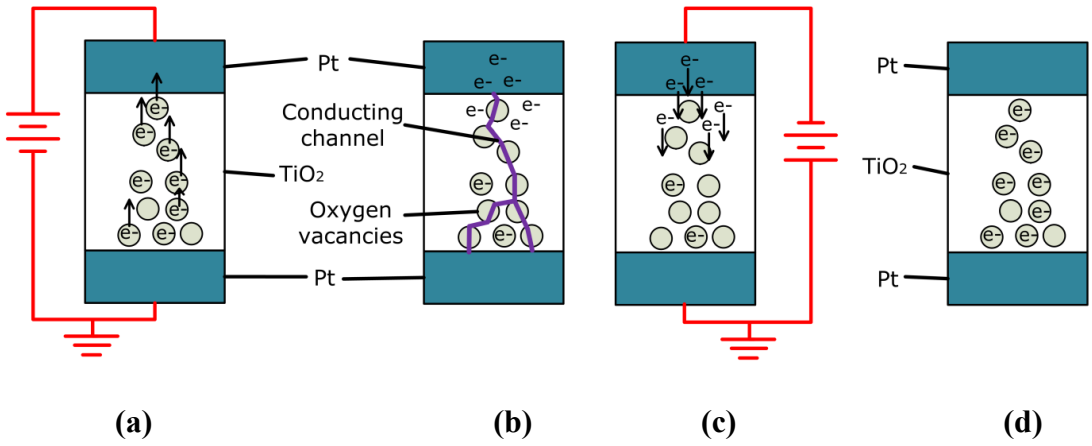

Figure 14. Switching mechanism of TiO_2 devices. (a) Positive bias is applied at the top electrode to switch the device ON, pulling electrons away from the bulk layer, causing an increased number of oxygen vacancies in the bulk layer. (b) The oxygen vacancies in the bulk layer create a conducting path for current to tunnel through the device and device is in low resistance state. (c) Negative bias is applied at the top electrode to switch the device OFF, repelling electrons towards the bulk layer and recombination occurs, thus (d) collapsing the conducing channel. The device switches to high resistance state.

Positive-charge oxygen vacancies are migrated in the bulk layer during switching (figure 14(a)). The drifting of oxygen vacancies from the region of highly-doped TiO_2 towards the oxygen-deficient region forms areas of lower resistances in the lowly-doped region of the bulk layer [89], [90]. These areas of lower resistances then combines to form a chain of low resistance regions, which forms a filament-like structure that protrudes the entire bulk layer and creates the conducting channels (figure 14(b)). The formation of the conducting channel is localized and do not take place throughout the entire cross-section of the bulk layer [158]. The conducting channel consists of Ti_4O_7 phase [154], which is less resistive than the non-doped regions of the bulk layer, which are mainly composed of TiO_2 phase [171]. Thus, the memristive device is in LRS.

The application of an opposing voltage causes the opposite movements of oxygen vacancies. This transforms the Ti_4O_7 phase in the conducting channel into other Ti–O phases, mainly TiO_2 phase (figure 14(c)). TiO_2 phase is highly-resistive and the conducting channel can no longer conduct current. The collapse of the conducting channel eliminates the current conduction path from the bulk layer, so large amounts of current cannot tunnel through the device (figure 14(d)). Thus, the bulk layer is now highly resistive and the memristive device is in HRS.

2.16.4 MISM memristive device switching mechanism

In TaO_2 devices, the resistive switching mechanism is assisted by a very thin insulating layer of highly resistive Ta_2O_5 phase fabricated between the top electrode and bulk layer [77], [78], [141]. The insulating layer of Ta_2O_5 consists of Ta_2O_5 and a very small percentage of TaO_2 phase.

To switch the device to its LRS, a negative bias is applied at the top electrode and the bottom electrode is grounded. The negative bias at the top electrode repels negative charged oxygen ions away from the top electrode (figure 15(a)). This causes Ta_2O_5 molecules to be reduced to TaO [172] and Ta [173] molecules by releasing oxygen ions from the Ta_2O_5 molecules. The oxygen ions then drift from the Ta_2O_5 layer towards the TaO_2 bulk layer. After a number of TaO and Ta molecules align in the Ta_2O_5 layer to form a conducting channel that is TaO and Ta-rich, large

amounts of current can tunnel through the insulating layer. This switches the device into LRS (figure 15(b)).

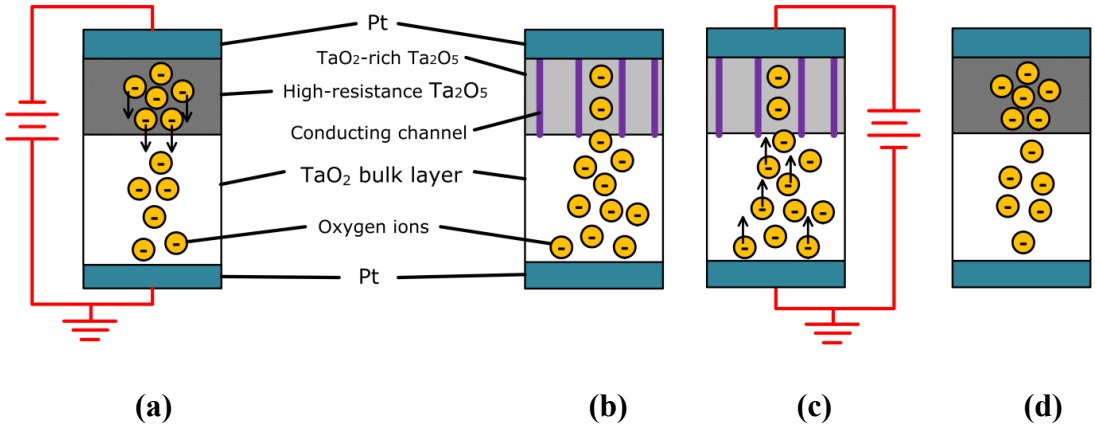

Figure 15. Switching mechanism of TaO_2 devices. (a) A negative bias is applied on the top electrode to switch the device ON, repelling negatively charged oxygen ions away from the Ta_2O_5 layer towards the TaO_2 layer. (b) Ta_2O_5 phase is reduced to TaO and Ta. After low-resistance TaO and Ta phases align, it forms conducting channels in the Ta_2O_5 layer. (c) Positive bias is applied on the top electrode to switch the device OFF, attracting oxygen ions towards the Ta_2O_5 layer. (d) The oxygen ions oxidize TaO and Ta phases to become Ta_2O_5 phases, and cause the collapse of conducting channels.

To switch the TaO_2 device to HRS, a positive bias is applied at the top electrode while the bottom electrode remains grounded. This attracts negatively charged oxygen ions from the TaO_2 bulk layer towards the top electrode and migrates into the Ta_2O_5 layer (figure 15(c)). As the oxygen ions accumulate in the Ta_2O_5 insulating layer, oxidation takes place and TaO and Ta molecules are oxidized into Ta_2O_5 molecules. The number of Ta_2O_5 molecules in the conducting channel increases and the resistance of the conducting channel increases. The conducting channel collapse when a number of Ta_2O_5 molecules disconnect the conducting

channel. This prevents current from flowing through the bulk layer and Ta_2O_5 layer, thus the device is in the HRS (figure 15(d)).

2.16.5 Comparison between MIM and MISM switching mechanisms

The switching mechanisms of TiO_2 and TaO_2 devices can be used to represent the general switching mechanisms of MIM and MISM devices respectively. The similarity between MIM and MISM devices is that redox reactions are performed on metal oxides when switching between resistance states. A redox reaction is a chemical reaction where one of the reactant undergoes oxidation while another reactant undergoes reduction. The resistivity is different for different phases of a metal oxide. Thus, by performing oxidation and reduction in memristive devices which switches the phases of the metal oxide in the bulk layer, the resistivity of the bulk layer is altered.

The difference between the two types of switching mechanisms of MIM and MISM devices is the manner of the formation of the conducting channels. In MIM devices, the conducting channel spans the entire length of the bulk layer of the device, protruding from one electrode to the other. As for MISM devices, the conducting channels are formed only in the insulator layer of the substrate. The low resistivity of the semiconductor bulk layer in MISM devices does not require a conducting channel to conduct.

2.17 Evaluation of TiO_2 and TaO_2 memristive devices

The electrical performance of memristive devices are evaluated based on switching speed, switching energy, resistance ratio, retention, and endurance.

2.17.1 Switching speed

The mobility of charged species through the switching layer is dependent on the material type and the forming field across that layer [174]. The mobility of the charged species in both TiO_2 and TaO_2 devices is the oxygen vacancies. The oxygen vacancies mobility, μ in TiO_2 is $1x10^{-10}$ $cm^2/V.s$ [88] and in TaO_2 is $5.46x10^{-10}$ $cm^2/V.s$ [175]. Assuming that temperature, voltage applied, electric field, and device dimensions are the same between TiO_2 and TaO_2 memristive devices, it is deduced that the migration of mobile charged species in TaO_2 is about 5 times faster than that in TiO_2 due to the vacancy mobility in TaO_2 is about 5 times faster than that in TiO_2. This also means that the time taken to form a conducting channel in TaO_2 devices is about 5 times faster than that in TiO_2 devices. Thus, it is postulated that the average switching speed of TaO_2 devices is about 5 times faster than that of TiO_2 devices.

2.17.2 Switching energy

The amount of electric field applied and charge carrier mobility are considered when estimating the energy consumed during the switching cycles in the devices. The drift velocity of charge carriers, v_d is given as:

$$v_d = \mu E_L \tag{11}$$

where E_L is the amount of electric field along the length of the bulk layer, and μ is the mobility of the charged species that is responsible for switching process.

In order to maintain similar switching speeds (fixed drift velocity of charge carriers) the required application of electric field across the length of the bulk layer is inversely proportional to the charge carrier mobility in the bulk material. Assuming TiO_2 and TaO_2 devices of similar physical dimensions, it is postulated that the switching energy of TiO_2 devices is larger than that of TaO_2 devices to obtain similar switching speeds based on the oxygen vacancy mobility, μ, in TiO_2 is slower than that in TaO_2.

2.17.3 Resistance ratio

A large resistance ratio is preferable for NVM devices [176] to ensure that the resistance states are further apart to increase the number of switching cycles before the resistance states of LRS and HRS intersect on another. When LRS and HRS

intersects, where the resistances are almost similar or resistance ratio becomes unity, then the device is assumed to cease from behaving as an NVM device as it can no longer perform resistive switching cycles. Large resistance ratio also reduces error when obtaining logic information from memristors.

To evaluate resistance ratio of memristors, the resistance of a memristor is first studied. Since the electrodes and substrate in TiO_2 and TaO_2 devices are in series to each other, the instantaneous resistance (memristance) of memristive devices is the summation of the resistance of each layer (electrodes and substrate). The resistance of the electrodes is always constant because it does not take place in the switching mechanism and is usually made of a metallic element. Thus, memristance is dependent on the resistance of the device substrate, which in turn depends on the history of charge flow through the memristor [88], i.e. HRS or LRS.

The resistance ratios (R_{OFF}/R_{ON}) of TiO_2 devices ranges from 500 to 10^5 [163], [169], [51], [177], [178], while the switching resistance ratios of TaO_2 devices ranges from 10^1 to 10^6 [59], [78], [155]. It is estimated that the average resistance ratio of future fabricated TaO_2 devices may be higher than that of TiO_2 devices due to the resistance ratios of TaO_2 devices reaching 10^6, while TiO_2 devices reaching up to only 10^5 of resistance ratios. However, further experiments are needed to prove this.

In order for memristive devices to be able to replace physical memory devices, it needs to be able to consistently switch between resistance states. Although slight deviation from its resistance state is allowed, a stable OFF/ON ratio is required. In

both devices, the HRS varies much more than the LRS, where an example of resistance switching is shown in figure 16. The HRS is formed by collapsing conducting channels, which is not a consistent process because the amount of charge carriers needed to collapse a conducting channel may vary during each switching. In the LRS, the conducting channel effectively shorts the device, so the only resistance along the device is the resistances of the electrodes, which is constant [179], [180]. The smaller the difference Most of the TiO_2 and TaO_2 devices have exhibited an almost consistent OFF/ON resistance ratio [78],[181]. Therefore, both TiO_2 and TaO_2 devices are two of the suitable candidates of memristive devices to replace physical memory devices in terms of stable resistive states.

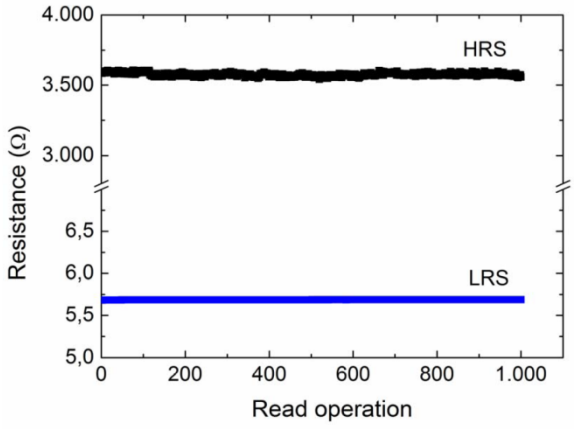

Figure 16. Resistance switching of memristive devices [179]**, showing that the LRS is more consistent than the HRS.**

2.17.4 Retention

Retention is the ability of memory and memristive devices to retain logic information without power supply, measured by the amount of time that the memory is still retrievable. The retention time of a memristive device may also be defined as the time taken for the device to deteriorate from its resistance state (HRS or LRS) by a certain amount of percentage, *R%*. The threshold for percentage of change, *R%* can be determined by researchers or manufacturers. Smaller values of *R%* yield better quality of retention in exchange for shorter retention period. Conversely, larger values of *R%* results in a longer retention period but yields a device with poor retention quality.

The retention time of memory devices at room temperature or normal operating conditions is estimated using extrapolation of the Arrhenius plot, which have also been used by other publications [182]–[184]. The Arrhenius equation defines the rate constant τ of a chemical reaction as:

$$\tau = Ae^{-E_a/kT} \tag{12}$$

where E_a is the activation energy of the reaction. A is a pre-exponential factor or frequency factor that depends on the frequency of collision between molecules, while the rate constant τ is the frequency of a successful reaction between reactants. Taking the natural logarithm, equation 12 becomes:

$$\ln \tau = -\frac{E_A}{k}\left(\frac{1}{T}\right) + \ln A \tag{13}$$

This method uses temperature-accelerated degradation of memristive devices and the percentage of change of resistance or conductivity, ΔR is observed. The device is degraded past $R\%$ at a specific constant temperature T. These temperature-accelerated degradations are usually performed at temperatures much higher than room temperature or normal operating conditions, in the range between 150 °C to 250 °C [182]–[184]. From the temperature-accelerated degradation experiment performed at temperature T, a graph of ΔR is plotted against time and the gradient is the rate constant τ for temperature T (figure 17).

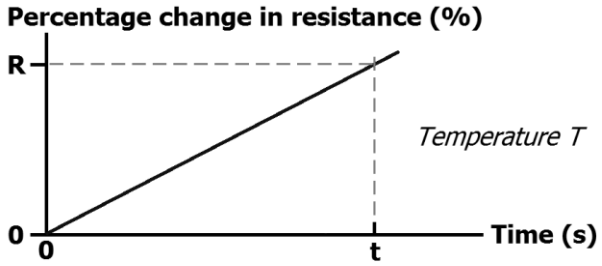

Figure 17. Temperature-accelerated degradation plot of percentage change in resistance against time at temperature T.

A similar procedure is repeated to obtain rate constants at different temperatures. The Arrhenius plot is drawn with $ln(\tau)$ plotted against T^{-1} (figure 18). The graph is then extrapolated to obtain the rate constant at room temperature or at a desired operating condition.

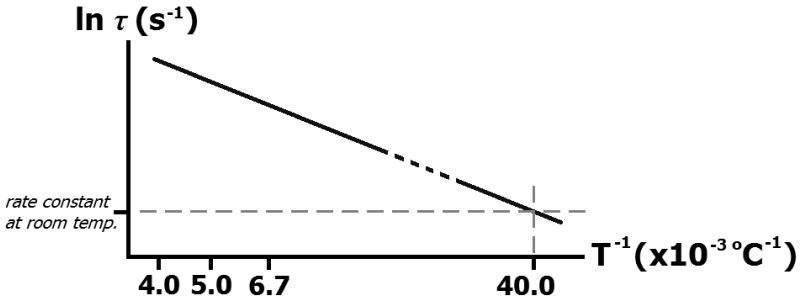

Figure 18. Arrhenius plot to find rate constant of at room temperature. 40.0 x10^{-3} °C^{-1} corresponds to a room temperature of 25 °C, while 4.0, 5.0 and 6.7 (x10^{-3}) °C^{-1} corresponds to the temperature-accelerated degradation performed at 250 °C, 200 °C, and 150 °C respectively.

This approach was used to obtain the retention time for TaO_2 devices operating between 25°C and 85°C, which is of over 10 years [78]. This retention time meets the standards of manufacturers of memory devices [182]. At the time of writing, the retention of TiO_2 devices has not yet been obtained using extrapolation of Arrhenius plot. There were reports stating that TiO_2 devices have retention time as long as 10 years but there are no experimental data or method that could provide sufficient evidence to support this statement. Although different fabrication methods and/or slightly different electrodes were tried, experiment data could still not provide sufficient evidence for retention of 10 years [185]–[188]. Due to the lack of robust methods in obtaining the retention period of TiO_2 devices, it cannot be concluded yet that TiO_2 devices have the retention ability of 10 years.

2.17.5 Endurance

The endurance of memristive devices is measured by the number of resistance switching cycles that can be successfully performed until the resistance ratio converges towards unity (intersection of HRS and LRS), or when the resistance ratio becomes less than a required amount. The minimum resistance ratio is determined by the application that uses the memristive device. The method to test device endurance is by switching the device continuously until it fails to meet any of the endurance criteria above.

Recent publications have shown that TaO_2 devices (10^{10} cycles [143]) have better endurance than TiO_2 devices (10^4 cycles [189]). It was also shown that after 10^4 cycles, the resistance states of TiO_2 converges and no longer exhibit memristive properties [77], while endurance of TaO_2 devices can reach up to 10^{12} cycles via increasing device size [113]. Increasing device size improves endurance due to the larger space available to produce more conducting channels. In larger devices, if for any reasons a conducting channel fails to reconnect while turning-ON, then there is a possibility that the turning-ON voltage is able to electroform a new conducting channel at other parts of the bulk layer that does not already have a conducting channel. Thus, ensuring another switching cycle can occur.

For memristive devices with similar physical device size, TaO_2 devices exhibit better endurance than TiO_2 devices due to the existence of multiple stable Magnéli phases in the titanium oxide (Ti-O) series [190], whereas the tantalum oxide (Ta-O)

series has only two stable Magnéli phases [191]. The phase diagrams of Ti-O and Ta-O are shown in figures 19 and 20 respectively. Magnéli phases of oxides appear when crystallographic shear occurs that changes the stoichiometry of the cation (metal) but still maintaining the coordination requirements of the cation. The homologous series of metal-oxide phases are made up of Magnéli phases of metal-oxides [192].

Due to the unstable Ti_4O_7 phase and multiple Magnéli phases in the Ti–O series, the doping of TiO_2 results in the formation of oxide phases other than Ti_4O_7 [154]. After a number of switching cycles, the redox reaction that takes place in the bulk layer forms Ti–O phases other than TiO_2 and Ti_4O_7. The other phases of Ti–O are also in thermal equilibrium with TiO_2 and Ti_4O_7, which increases the reluctance of the other phases to react. With the increase of other higher resistive phases in the bulk layer, the device is unable to switch back to its initial R_{ON} and R_{OFF} states. This means that the TiO_2 device has reached its endurance limit.

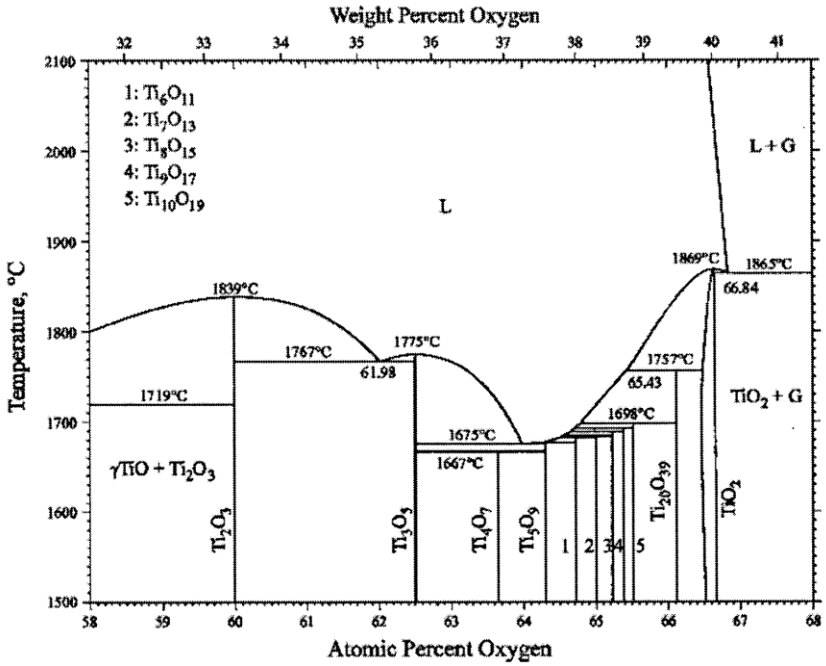

Figure 19. Ti-O phase diagram [190].

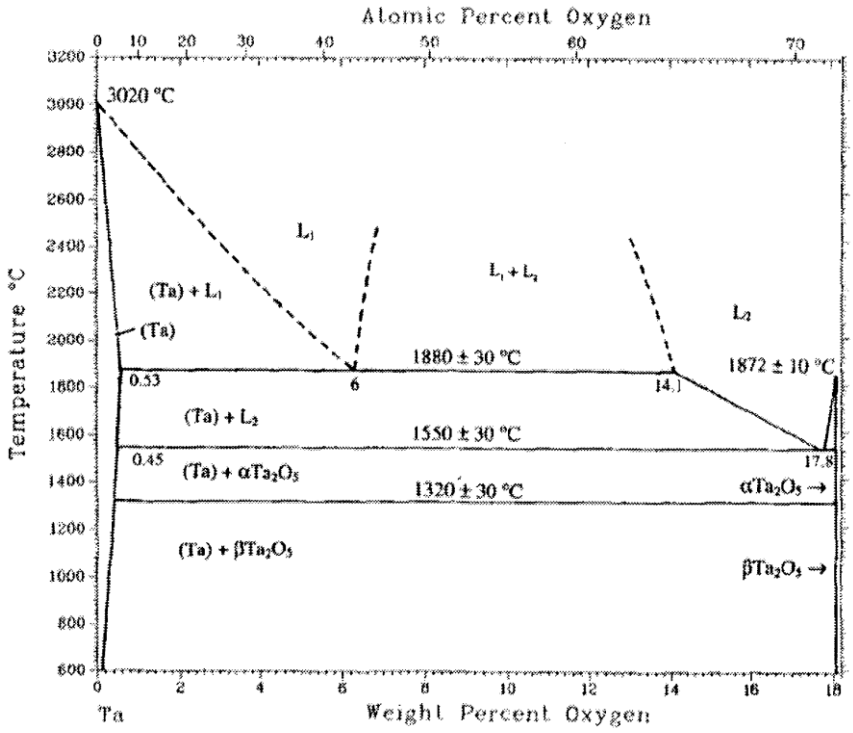

Figure 20. Ta-O phase diagram [191].

For TaO_2 devices, the Magnéli series consist of only two stable phases: TaO_2 and Ta_2O_5. This means that every chemical reaction in the bulk layer only involves these two Ta–O phases. This improves device endurance because the redox reaction that occurs in TaO_2 is only between two phases of Ta–O. Therefore, it is concluded that TaO_2 devices have better endurance than TiO_2 devices due to the lesser number of stable Magnéli phases in the Ta–O series.

Apart from using materials with lesser number of stable Magnéli phases, endurance of resistive switching devices can also be improved by regulating the electroformation process [142]. By minimizing the electroforming process, physical damages are minimized. This reduces the probability of a conducting channel failing to form or collapse, which eventually increases the number of resistive switching cycles that can be performed in the device and improves endurance of the memristive device.

2.18 Physical factors of memristive devices

Resistance ratio, retention and endurance are factors of reliability of memristive devices, which are affected by the physical factors of memristive devices. Apart from resistance ratio, retention and endurance, physical factors also affect resistive switching behaviour. The physical factors that affect the behaviour of memristive devices are: thickness of bulk layer, device size, and electrode material.

2.18.1 Thickness of bulk layer

Thick bulk layers in MIM memristive devices prevents conducting channels from being formed due to the large amount of electric field required to breakdown the thick bulk layer. This is shown by the decrease in probability for formation of a conducting channel with an increase in bulk layer thickness [181]. The range of bulk layer that consistently exhibits memristive behaviour is below 500nm [193], while bulk layers thinner than 50nm [154], [194] or even 10nm [195] also has memristive properties. Switching voltages are observed to be independent with varying bulk layer thickness [146]. This is due to the forming and deforming of conducting channel occurs only at localized areas, which is a small region inside the bulk layer. Majority of the applied potential difference is dropped across the switching region, which are almost constant in size and independent of bulk layer thickness. Thus, the switching bias remains fairly constant with varying bulk layer thickness [154], [156].

The resistivity of the HRS of MIM memristive devices increases with the thickness of bulk layer due to the charge carriers needing to drift through a greater distance along the device [51]. There are no conducting channels in the HRS of the device, thus the greater the distance, the higher the resistivity of the bulk layer. Conversely, the resistivity of LRS remains fairly constant because the device is fundamentally shorted in the LRS.

In TaO_2 devices, the substrate is composed of two layers, the bulk layer with majority of TaO_2 phase and insulator layer with majority of Ta_2O_5 phase. Because there are two layers with different phases of Ta–O, two types of comparison are performed: (i) devices with same layer ratio but different substrate thickness, and (ii) devices with different layer ratios.

2.18.1(a) TaO_2 devices with similar layer ratio

It was observed that the trend among TaO_2 devices with different substrate thickness but constant thickness ratio between TaO_2 and Ta_2O_5 layers is similar to that of TiO_2 devices and the switching bias is fairly constant for constant layer ratio between layers [196]. The reason for this trend is due to the similar switching characteristics between HRS and LRS given the same R_{OFF}/R_{ON} ratio of the memristive device.

2.18.1(b) TaO_2 devices with different layer ratio

For TaO_2 devices with different layer ratios [141], there are two types of comparison: (i) varying TaO_2 bulk layer thickness with constant Ta_2O_5 insulator layer, and (ii) varying Ta_2O_5 layer thickness with constant TaO_2 bulk layer.

Varying TaO_2 layer thickness (fixed Ta_2O_5 layer thickness) does not change the amount of current flow in the LRS due to the device being shorted in LRS. In the HRS, it is observed that the current flow is lesser in the device with thicker TaO_2 layer (10^{-8}A compared to 10^{-6}A), because a longer device increases overall device resistance. Due to switching regions located inside the Ta_2O_5 insulator layer, thus varying TaO_2 layer does not affect the switching-ON bias (-1.5V) because the electric field is applied across the switching region located in the Ta_2O_5 insulator layer. However, the switching-OFF bias is larger with thicker TaO_2 layer due to the longer distance the oxygen ions need to travel through the thicker TaO_2 layer towards the Ta_2O_5 layer to collapse the conducting channels. Therefore, a larger switching-OFF bias is required to collapse the conducting channel, and it is concluded that varying TaO_2 layer affects the HRS but not the LRS of the device [141].

Varying Ta_2O_5 layer thickness (fixed TaO_2 layer thickness) changes the current flow in the LRS and HRS of the device. Increasing the thickness of Ta_2O_5 layer decreases the amount of current flow through the device in both LRS and HRS, due to increased resistivity of the Ta_2O_5 layer [113]. Another observation is that both switching-ON and switching-OFF biases remain fairly constant with different Ta_2O_5

thickness. Switching-ON bias is constant due to the switching regions, located in the Ta_2O_5 insulator layer, are usually fairly constant in size regardless of the thickness of the Ta_2O_5 layer. Since TaO_2 bulk layer has fixed thickness, the distance between the switching regions in the Ta_2O_5 layer to the opposite end of the TaO_2 layer is constant. Therefore, the switching-ON and switching-OFF biases are constant with varying Ta_2O_5 layer thickness [141].

2.18.2 Device size of memristive devices

The device size of memristors is defined by the cross-section area of electrodes. For the parameters used in this research work, the device size of the memristors is 32nm x 32nm. According to Ohm's law, resistance of a conductor is inversely proportional to cross-section area of the conductor. Increasing memristive device size would decrease R_{OFF} only. In the HRS of the devices, there are no conducting channels, thus electric field is applied across the entire cross-section of the bulk layer. Thus, R_{OFF} decreases with increasing device size.

Increasing device size of memristive devices does not linearly decrease R_{ON} of TiO_2 and TaO_2 devices [113]. When a memristive device is in LRS, it forms a thin conducting channel with a diameter much smaller than the electrode cross-section area. The conducting channels do not span across the entire electrode [197]. This observation was also reported for other memristive devices with similar device structures [60][198]. Increasing device size does not necessarily mean that the

conducting channels increase in size. However, it increases the probability of more conducting channels being formed [154], but not all conducting channels are switched on when the memristive device is switched ON. Thus, since larger devices do not guarantee an increase in conductivity, then it might be a waste to fabricate larger devices for the sole purpose of increasing conductivity.

2.18.3 Band gaps

Comparing band gaps of TiO_2 and TaO_2/Ta_2O_5, publications have reported that wider band gaps leads to lower switching currents, which are advantageous for resistive switching [193]. The band gap of TaO_2 is 4.0 – 4.2 eV [199], Ta_2O_5 is 3.9 – 5.3 eV [200], [201], and TiO_2 is 3.0 – 3.2 eV [193], [202]. Therefore, this adds weight to the choice of TaO_2 memristive devices over TiO_2 memristive devices.

2.18.4 Electrode material selection

Electrodes do not place in the switching process, but electrode elements affect the manner chemical reactions takes place in the bulk layer [203]. Thus, for the same type of bulk layer material, it is possible to fabricate a URS or BRS device based on the electrode material used. For example, a $Ag/TiO_2/Ag$ device shows URS mechanism [204], while $Pt/TiO_2/Pt$ device shows BRS mechanism [51].

For TiO_2 devices, one of the electrode is usually Pt, and the other electrode may be replaced with other materials that still allow bipolar resistive switching to take place, such as: silver, Ag [202], aluminium, Al [205], and tungsten, W [206]. For TaO_2 devices, other electrode materials that allow bipolar resistive switching to take place are such as: Al [207], copper, Cu [59], nickel, Ni [208], and W [209].

Electrode material selection is vital to enable resistive switching to take place in a device. Resistive switching cannot take place in a device if both top and bottom electrodes create ohmic contacts with the bulk layer [210]. Resistive switching can only take place when at least one of the electrodes creates a Schottky barrier with the bulk layer. This also explains why certain electrode materials can be used to fabricate memristive devices with different bulk layer materials, such as tungsten, W is used as the electrode material to fabricate memristive devices with bulk layers of TiO_2 [206], TaO_2 [209], silicon oxide, SiO_2 [211], or hafnium oxide, HfO_2 [212].

Among the electrodes used to fabricate memristive devices, a common trend could not be found and the effect on the performance of the devices varies, albeit several similarities in the electrode elements that can be used to fabricate TiO_2 and TaO_2 devices. Hence, the trend in electrode material selection is placed for future research.

In summary, the physical factors of memristive devices (bulk layer thickness, device size, and electrode material) affect the electrical properties of memristive devices (electroformation, switching voltage, resistance ratio, retention, endurance, and type of switching). Due to the various physical factors and electrical properties

affecting memristive devices, there have been extensive researches conducted to further understand the relationships between the various physical factors and various electrical properties. It is therefore understood that the role of memristors in its application would most likely determine the fabrication process to ensure that the electrical properties of the memristors conform to its intended resistive switching behaviour in the application.

3. MEMRISTOR MODELLING

MEMRISTOR MODELLING

3.1 Batas & Fiedler memristor model

The Batas & Fiedler memristor model has shown flexibility by being able to adapt to a variety of window functions [92]. However, a fault has been found in the Batas & Fiedler memristor model and the following sections explain the fault, as well as the proposed memristor model [110]. In general, bidirectional current flow can be created in two ways:

(i) fixed ground

(ii) dynamic ground

3.1.1 Fixed ground bidirectional current

In the fixed ground method, one terminal of the memristor is permanently grounded while biasing potential is applied at the other terminal of the memristor. As shown in figure 21, terminal B of the memristor is connected permanently to ground (fixed ground) while a voltage supply is applied at terminal A. The voltage supply at A can be either a square wave or sinusoidal, but regardless of the waveform the

voltage supply at A must have alternating polarity to ensure bidirectional current flow through the memristor.

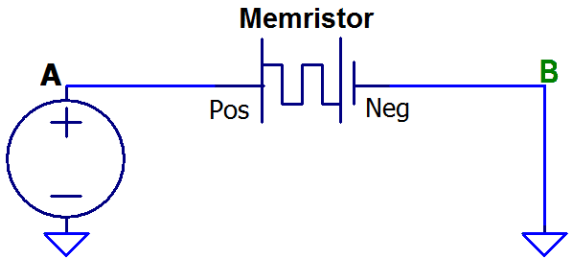

Figure 21. Memristor connected using fixed ground method.

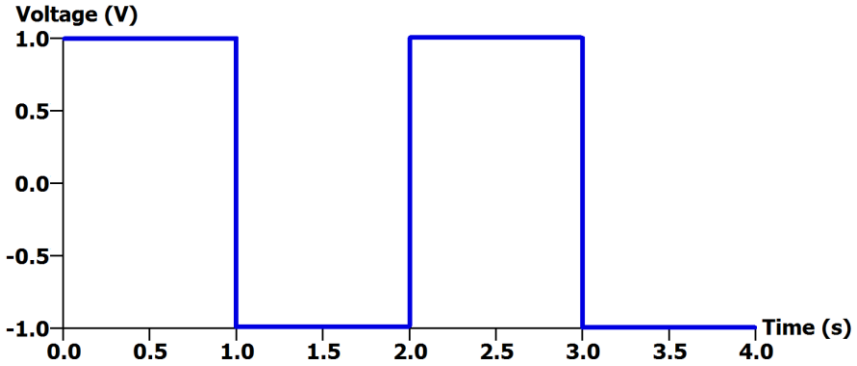

Figure 22. Voltage input at A for the circuit in figure 21.

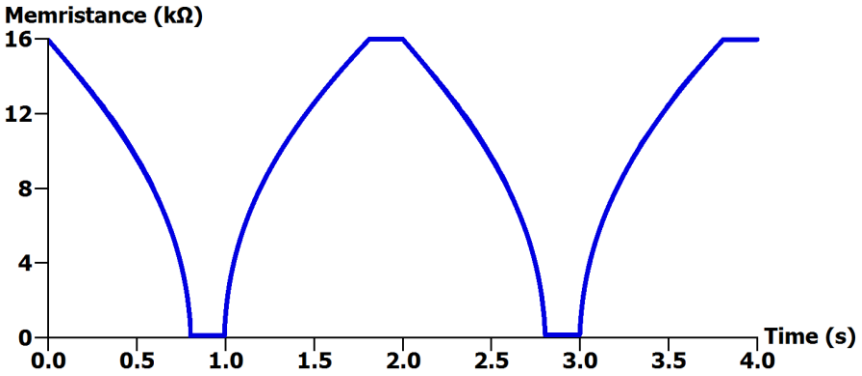

Figure 23. Memristive behaviour exhibited by the Batas & Fiedler memristor model using fixed ground method.

Figure 22 shows the voltage applied at A. Current is directed into (1V from 0ns until 200ns) and drawn out (–1V from 200ns to 400ns) from the memristor at the terminal A alternatively, which creates a bidirectional current flow through the memristor. The memristive behaviour exhibited by the Batas & Fiedler model is shown in figure 23, where the memristance of switches between 100Ω (LRS) and 16kΩ (HRS). Therefore, the characteristics of the Batas & Fiedler model memristor model using fixed ground connection are similar to the mathematical theory of memristors [47] and the physical model of the memristor [88].

3.1.2 Dynamic ground bidirectional current

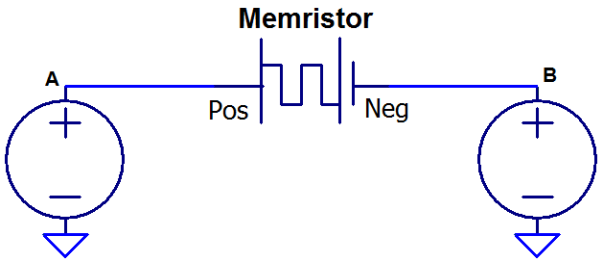

Figure 24. Memristor connected using dynamic ground method.

In the dynamic ground method, none of the terminals are permanently grounded. Bidirectional current flow with dynamic ground is created by connecting both memristor terminals to two independent voltage sources as shown in figure 24. The direction of current flowing through the memristor depends on the polarity of the potential difference across the memristor terminals. For instance, if the biasing at A is +V and B is at 0V, current flows from A to B. Conversely, if the biasing at B is

+V and A is at 0V, current flows from B to A. Thus, dynamic ground method does not impose restrictions on grounding on a specific terminal. Such a memristor model has been described by the mathematical theory [47] and physical model of memristors [88].

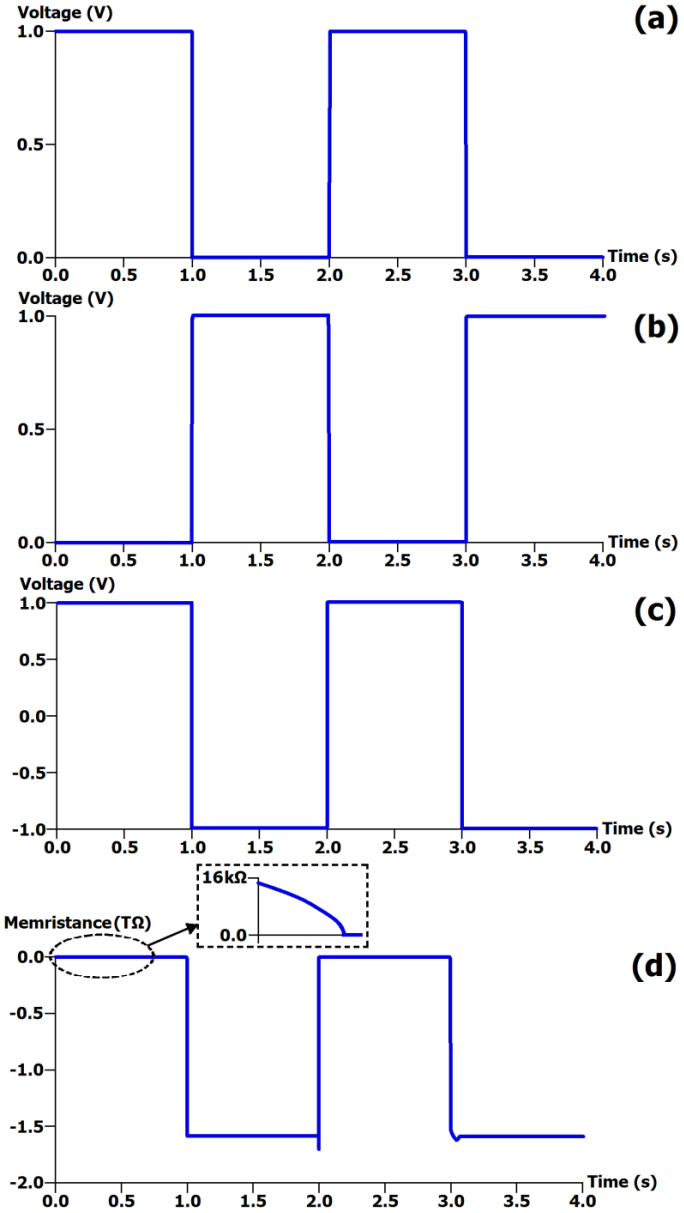

Figure 25. Simulation results of the memristor connected using dynamic ground method. (a) Voltage input of V_A. (b) Voltage input of V_B. (c) Potential difference across memristor. (d) Memristive behaviour exhibited by the Batas & Fiedler memristor model using dynamic ground.

The behaviour of the Batas & Fiedler memristor model is subjected to the dynamic ground method by applying potentials V_A and V_B as shown in figures 25(a) and 25(b) respectively. The potential V_A and V_B are complementary to each other, where if one is at 1V then the other is at 0V, and vice versa. This results in the potential difference across the memristor as shown in figure 25(c), which is exactly similar to the potential difference across the memristor with fixed ground bidirectional current. The resulting memristive behaviour exhibited is shown in figure 25(d).

It is observed that the R_{OFF} of the memristor increases to the range of Tera-Ohms in contrast to the memristor modelling parameters that set R_{OFF} to 16kΩ. Thus, the Batas & Fiedler memristor model fails to behave correctly when dynamic ground bidirectional current is used and hence, it is not in good agreement with the mathematical theory [47] and physical model of memristors [88].

3.1.3 Fault in the Batas & Fiedler memristor model

The Batas & Fiedler memristor model consists of two sub-circuits (figure 26). For ease of explanation, the sub-circuits are named as Voltage-Input Circuit (VIC) and Memristance Function Circuit (MFC). The VIC functions to connect the memristor to external circuitry. Apart from receiving input voltage, the VIC also has a voltage-dependent variable voltage source (*Ememristor*) that acts as a variable resistance that represents the memristance of a memristor. Meanwhile, the MFC

simulates the behaviour of the memristance by using a current source to simulate the current flow through the memristor.

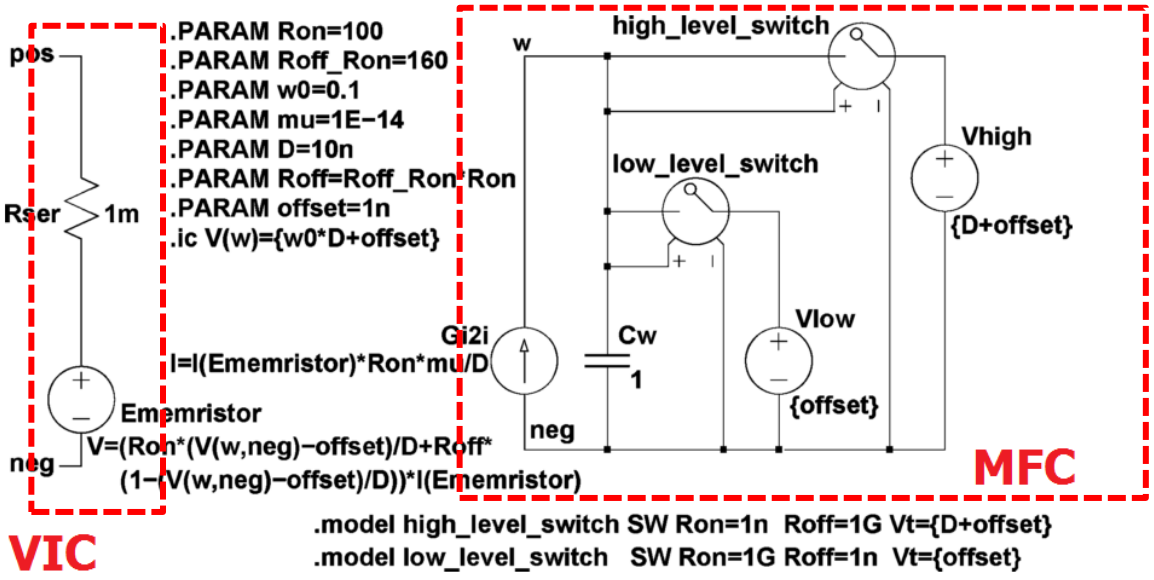

Figure 26. Batas & Fiedler memristor model [92].

In the MFC, the current source is proportional to the amount and dependent on the direction of current flowing through the VIC. Thus, the larger the voltage in the VIC, the higher the amount of current supplied by the current source in the MFC. Similarly, an opposing polarity of voltage applied at the VIC also changes the polarity of the current source in the MFC. The memristance behaviour (*Ememristor*) is inversely proportional to the potential difference between nodes *w* and *neg* in the MFC. Thus, whenever voltage is applied at the VIC, the current source in the MFC causes a change in the potential difference between nodes *w* and *neg* in the MFC, which in turn changes the amount of current flow in the VIC by changing (*Ememristor*), which then affects the current source in the MFC. Eventually and

gradually, memristance switches in a nonlinear manner to either LRS or HRS depending on the polarity of the applied voltage at VIC. The MFC has voltage-controlled switches that provide boundary conditions and a capacitor to behave as the component that remembers the history of charge flow.

The VIC has two nodes (*pos* and *neg)* to establish connections to an external circuit. The ground node in MFC is the *neg* node, which is also connected to the VIC. This forces the *neg* pin of the memristor to be constantly connected to an external ground (fixed ground) in order to obtain the correct functionality of the memristor. When a positive bias in a dynamic grounding method is applied at *neg* node, the charging and discharging of the capacitor and switches inside the MFC fails to conform to correct circuit behaviour. Therefore, this causes the memristance of the memristor to increase to the range of Tera-Ohms (Fig. 25(d)). Hence, the Batas & Fiedler memristor model fails to exhibit the correct memristive behaviour if the *neg* node is connected to a non-zero voltage source.

3.2 Enhanced SPICE Memristor Model with Dynamic Ground

To address this issue in the Batas & Fiedler memristor model, the *neg* node connection between MFC and VIC in the memristor model is separated and an enhanced memristor model with dynamic ground features was published [110]. The schematic of the enhanced SPICE memristor model with dynamic ground is shown in figure 27 and the netlist for the memristor model is attached in appendix A.

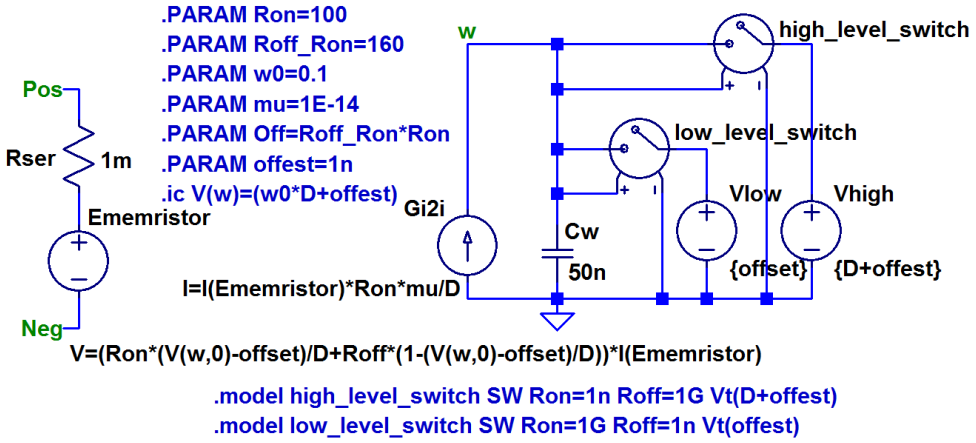

Figure 27. Schematic circuit of enhanced SPICE memristor model with dynamic ground.

In the enhanced SPICE memristor model with dynamic ground model, the *neg* node of the VIC is connected to the external pin of the memristor, while the *neg* node in the MFC is separately grounded. When the *neg* terminal of the memristor is connected to a non-zero voltage source, the circuit behaviour of the MFC is not affected due to the independent grounding of MFC. Thus, when the proposed memristor model is subjected to dynamic grounding, it is able to admit bidirectional

current flow through it and allows the MFC to function correctly regardless of the type of biasing of the memristor.

To verify the proposed memristor model, the memristor is subjected to bidirectional current flow with both types of biasing; fixed and dynamic ground. This is performed by applying voltage inputs similar to that in figures 22 and 25. The memristance of the proposed memristor model obtained for both types of bidirectional current flow is shown in figure 28. It can be observed that the proposed memristor model exhibits correct memristive switching behaviour for the respective applied voltage in either fixed or dynamic ground method of biasing.

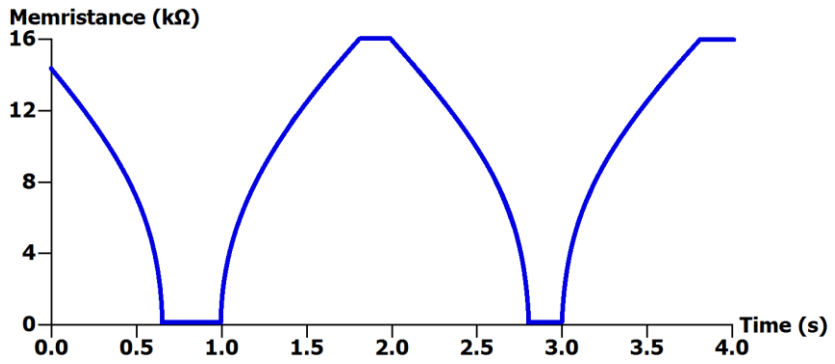

Figure 28. Memristive behaviour exhibited by the proposed memristor model using fixed and dynamic ground method of input biasing.

Furthermore in recent memristive devices, memristive switching times are less than 50ns. Due to this, the proposed memristor model was also improvised to simulate switching in nanoseconds. This was done by changing the capacitance in MFC from 1F in the original circuit to 50nF in the proposed memristor model.

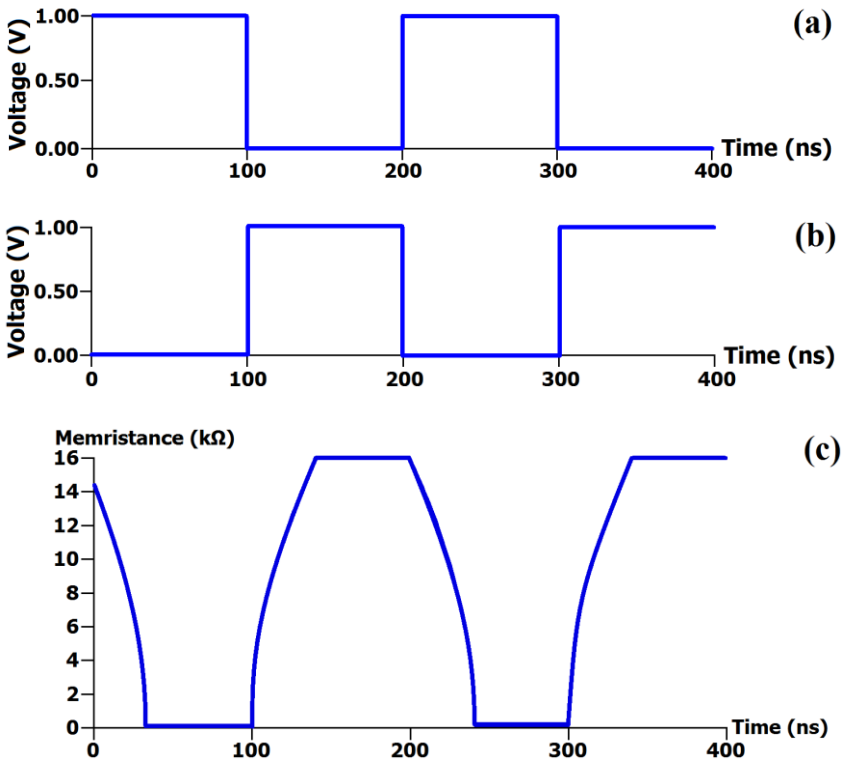

Figure 29. Simulation of the enhanced SPICE memristor model with nanoseconds switching. (a) Voltage input of V_A. (b) Voltage input of V_B. (c) Memristive behaviour exhibited by the SPICE memristor model.

The final memristor model is subjected to similar voltage input magnitude but at higher frequencies, as shown in figures 29(a) and 29(b), and the resulting memristance behaviour is shown in figure 29(c), where R_{OFF} is 16kΩ and R_{ON} is 100Ω. This summarizes that the proposed memristor model is able to perform at high frequency for nanoseconds switching behaviour with both types of grounding methods, fixed and ground.

In summary, the published enhanced SPICE memristor model with dynamic ground [110] was shown to exhibit memristive behaviour close agreement to physical and theoretical characteristics of memristors. Therefore, this SPICE

memristor model is used to simulate memristors for the remainder of the research work that are documented in this dissertation, unless stated otherwise.

4. SEQUENTIAL LOGIC CIRCUITS

SEQUENTIAL LOGIC CIRCUITS

4.1 Non-volatile memristive D-latch (NVDL)

To overcome the volatility of CMOS-based D-latch and to improve power consumption, a non-volatile memristive D-latch (NVDL) was proposed and published [213]. The NVDL also benefits against CMOS sequential logic circuits with the addition of non-volatile memory storage. The non-volatility of memristors allows the sequential logic circuit to be independent of input supply when retrieving logic information that was previously programmed into the latch circuit.

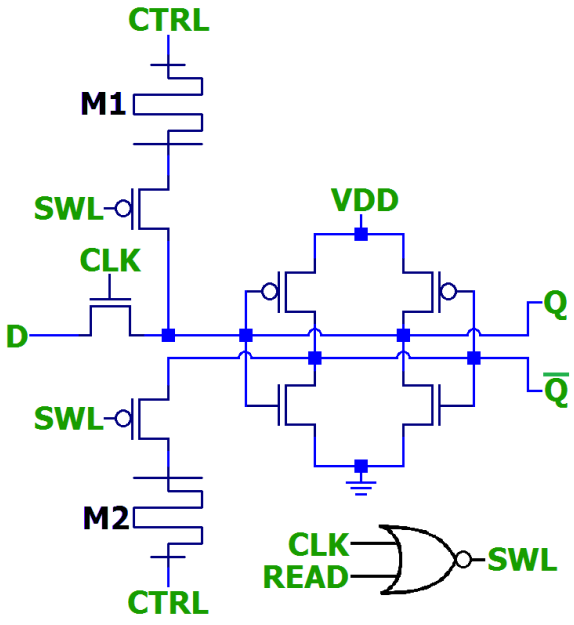

Figure 30. Schematic circuit of the non-volatile memristive D-latch (NVDL)

The schematic circuit of the NVDL is shown in figure 30 and the netlist is attached in appendix B. The NVDL uses 11 transistors (including 4 transistors in the logic NOR gate) and 2 memristors, which is 1.83 times more device area than the CMOS D-latch. The function of the logic NOR gate is to ensure that the NVDL is selected for either writing (CLK) or reading ($READ$) processes. The non-volatility of the NVDL is implemented by incorporating memristors into the circuit design. Thus, logic information of the latch is stored in the form of memristance. The functionality of the NVDL is divided into four parts: (i) latch circuit, (ii) retention of logic information, (iii) resistive switching, and (iv) steady-state operation.

4.1.1 Latch function of NVDL

A latch is defined as a circuit where its output changes whenever its input changes, provided that the circuit is enabled by a clock signal. The NVDL functions with D and CLK as inputs to the circuit while Q and $\bar{Q}$ are the outputs, where Q and $\bar{Q}$ are complementary to each other. D is charged to V_{DD} to input logic '1' and grounded to 0V to input logic '0'. An NMOS pass-transistor with its gate connected to CLK separates input D from output Q, and acts as the circuit-enable switch.

If CLK is low, a high impedance channel exists in this NMOS pass-transistor. Thus, any changes in input D do not affect output Q when CLK is low and Q remains unchanged. When CLK is high, the pass-transistor has a low impedance conducting channel between input D and output Q, and the voltage at D is transmitted to Q.

Therefore, whenever CLK is high, output Q changes instantaneously towards any changes in input D. Thus, the NVDL functions as a latch.

4.1.2 Retention of logic in NVDL

For temporary logic information storage, an inverter loop consisting of two CMOS inverters connected back-to-back is used. Output Q is fed into a CMOS inverter to produce a complementary output $\bar{Q}$. At the same time, another CMOS inverter is connected to $\bar{Q}$ and the output of this CMOS inverter is connected to Q. This ensures that the complementary logic between Q and $\bar{Q}$ is retained for as long as the power supply to the CMOS inverters is uninterrupted. Q and $\bar{Q}$ are also not changeable when CLK is low.

4.1.3 Resistive switching in NVDL

Memristors are also used as logic information storage which can be programmed and read. SWL controls the access of memristors for programming or reading and is the result of $READ$ or CLK. Whenever CLK is high, SWL is activated and creates low impedance conducting channels between Q and memristor M1, and between $\bar{Q}$ and memristor M2. $CTRL$ is connected to the negative terminals of both memristors and is a constant voltage supply. $CTRL$ should be between the voltage

levels of V_{DD} (1.0V) and 0V to allow bidirectional current flow through the memristors and is set to 0.6V for the NVDL in this research. $CTRL$ set to 0.6V also ensures the switching speed to switch the memristors to LRS or HRS is almost similar. If Q (or $\bar{Q}$) is at V_{DD}, the voltage at the positive terminal of memristor M1 (or M2) is larger, thus current flows into the positive terminal of memristor M1 (or M2) and the memristance decreases to its LRS. Conversely, if Q (or $\bar{Q}$) is at 0V, the voltage at the negative terminal of memristor M1 (or M2) is larger, thus current flows out of the positive terminal of memristor M1 (or M2) and the memristance increases to its HRS. Since memristors M1 and M2 are connected to Q and $\bar{Q}$ respectively, their memristance states are always complementary to each other due to Q and $\bar{Q}$ are complementary of each other.

When CLK is low, outputs Q and $\bar{Q}$ are disconnected from memristors M1 and M2 because SWL creates a high impedance channel in the pass-transistors between outputs Q and $\bar{Q}$ and memristors M1 and M2 respectively. Thus, memristors are only programmed when CLK is high.

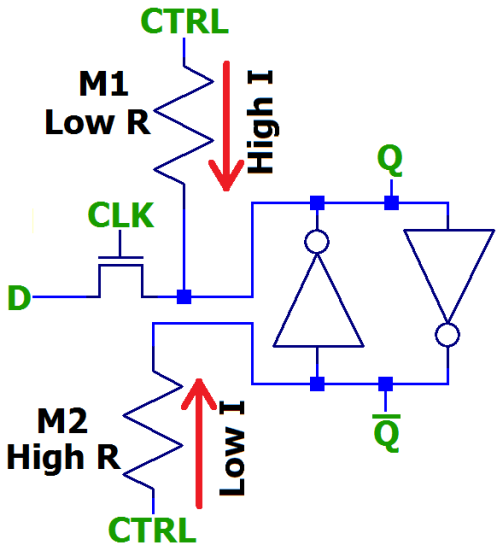

Figure 31. Equivalent circuit when restoring logic information in the NVDL

To read from the memristors and restore logic information into the inverter loop, $READ$ signal is triggered and $CTRL$ is set to V_{DD}. Current flows with different amounts from $CTRL$, through the SWL pass-transistors, and into memristors M1 and M2. The path where the memristor is in LRS provides a path of lower resistance and current flow is higher. For example (as shown in figure 31), if Q was latched to logic '1' (Q was at V_{DD}) memristor M1 would have been programmed to LRS, and the voltage drop across memristor M1 is about $0.2V_{CTRL}$ and the remaining $0.8V_{CTRL}$ is dropped at Q when reading the memristor. These values are obtained from simulation results. This causes the inverter loop to output 0V at $\bar{Q}$, and eventually the complement CMOS inverter pulls-up Q to V_{DD}. In the meantime, memristor M2 is at HRS and the voltage drop across it is $0.8V_{CTRL}$ and the remaining $0.2V_{CTRL}$ is dropped at $\bar{Q}$. This causes the CMOS inverter to output V_{DD} at Q. Conversely, if Q was latched to logic '0' (Q was at 0V), memristor M1 is switched to HRS with a potential difference of $0.8V_{CTRL}$ across memristor M1 and only $0.2V_{CTRL}$ is dropped at Q, thus $\bar{Q}$ outputs V_{DD} and Q is grounded to 0V.

4.1.4 Steady-state operation of NVDL

Without $READ$ or CLK signals, SWL is grounded to 0V and the SWL pass-transistors are in high impedance. Memristors M1 and M2 preserve their memristance states because they are disconnected from Q and $\bar{Q}$. When the pass-transistors are in high impedance, current cannot flow through the memristors between the outputs (Q or $\bar{Q}$) and $CTRL$. Thus, memristance states are retained. This ensures that the NVDL do not lose logic information while in operation. The high impedance channels also ensure that the resistance parallel to output Q and $\bar{Q}$ is high. The output impedance parallel to output load is 3.72TΩ. The summary of the operation of the proposed NVDL is summarized in table 3, where X refers to 'don't care' logic state.

Table 3. Summary of the operation of NVDL

CLK	**READ**	**D**	**Q**	**$\bar{Q}$**
0	0	X	Last Q	Last $\bar{Q}$
0	1	X	Last Q	Last $\bar{Q}$
1	X	0	0	1
1	X	1	1	0

4.2 Memristive D flip-flop (MDFF)

Similarly, a Memristive D Flip-Flop (MDFF) has been designed and proposed to replace CMOS-based D flip-flops to introduce non-volatile characteristics into sequential logic circuits, as well as to improve power consumption. The schematic circuit for the MDFF is shown in figure 32 and the netlist is attached in appendix C. The MDFF has a master and slave relationship between two sets of CMOS inverter loops that satisfies the definition of a flip-flop circuit.

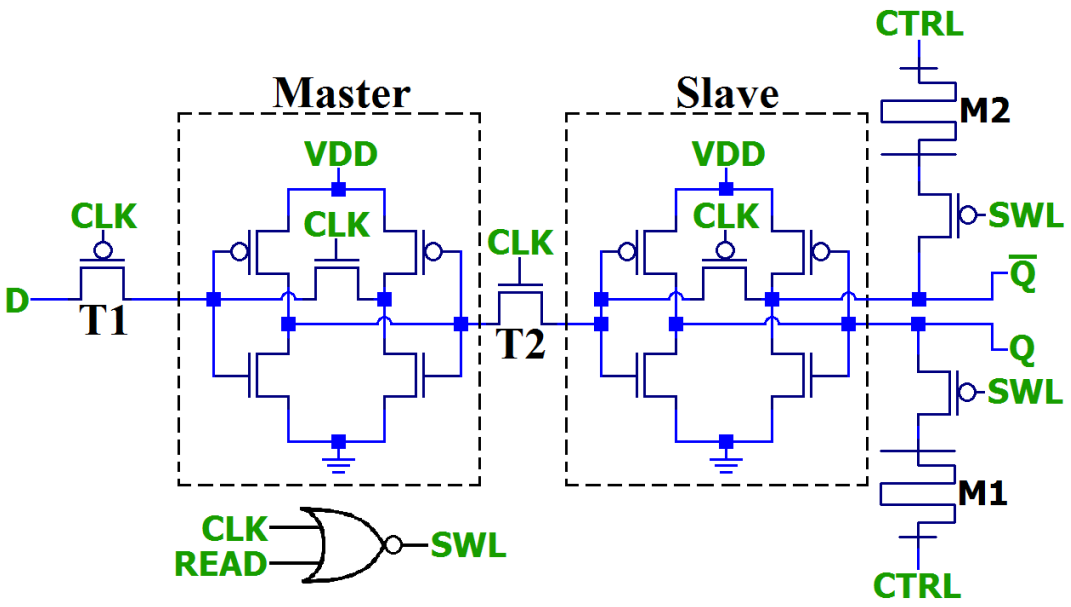

Figure 32. Schematic circuit of the Memristive D Flip-Flop (MDFF)

When clock is low, the master latches onto the input from *D* and the master and slave are disconnected by a high-impedance transistor T2. The addition of a pass-transistor between the CMOS inverters in both master and slave is to prevent

short-circuiting between the CMOS inverters. This was not evident in the NVDL, and thus was not inserted in the NVDL circuit.

When the clock toggles high, any changes at input D do not affect the voltage levels in the master due to T1 being turned off. Thus, the logic bit has been latched in the master. While the clock is high, the master and the slave are connected via transistor T2. The CMOS inverters in the master are connected to ensure a stable voltage and the slave latches onto the logic bit from master. The CMOS inverter in the slave inverts the logic bit from the output of master to produce output Q. At the same time when the clock is high, memristors M1 and M2 are programmed to the appropriate memristance states. The switching of memristance states of M1 and M2 depends on the voltage at Q and $\bar{Q}$. If Q or $\bar{Q}$ is at logic '1' (V_{DD} = 1V), current flows from Q or $\bar{Q}$ to $CTRL$ ($CTRL$ = 0.6V). Consequently, M1 or M2 is switched to its LRS. Conversely, if Q or $\bar{Q}$ is at logic '0' (0V), current flows from $CTRL$, and M1 or M2 is switched to its HRS.

When clock returns to low, T2 disconnects the slave from the master and any changes in input D can only be transmitted to the output Q at the next rising edge of the clock. Simultaneously, output Q carries the logic bit from the slave for as long as power supply to the MDFF is uninterrupted. At this time also, any change in input D is immediately reflected in the master.

If power supply to the memristive sequential logic circuits is interrupted, logic information can be restored by reading from the memristors. When the read process is initiated, the SWL transistors are turned on and the $CTRL$ channels V_{DD} for 5ns

through the memristors. The current through the memristor with LRS is larger than the current through the memristor with HRS. This causes the voltage dropped at the invertor loop that is connected to the LRS memristor to output 0V, due to the higher amount of voltage at the input terminal of the inverter. Likewise, the complementary inverter outputs V_{DD} and logic information is restored in the slave.

4.3 Simulation results of memristive sequential logic circuits (MSLC)

Simulation of the NVDL and MDFF is shown in figures 33 and 34 respectively. V_{DD} is set to 1.0V (due to the 32nm CMOS process technology), thus 0.6V connected to the CMOS inverter input is sufficient for the CMOS inverter to be able to output 0V. As such, $CTRL$ is set to 1.0V to perform read process to ensure that the CMOS inverter is able to produce the appropriate output when retrieving logic information from the memristors. $CTRL$ is set to 0.6V during normal operation to ensure that the potential at the negative terminal of the memristors is between the potential of logic '1' (V_{DD}) and logic '0' (0V), as well as to ensure a more symmetrical resistance switching between HRS and LRS.

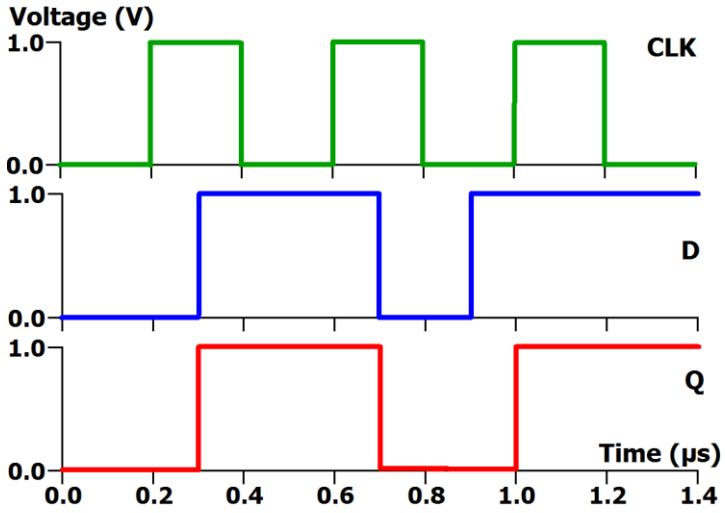

Figure 33. Simulation of the NVDL

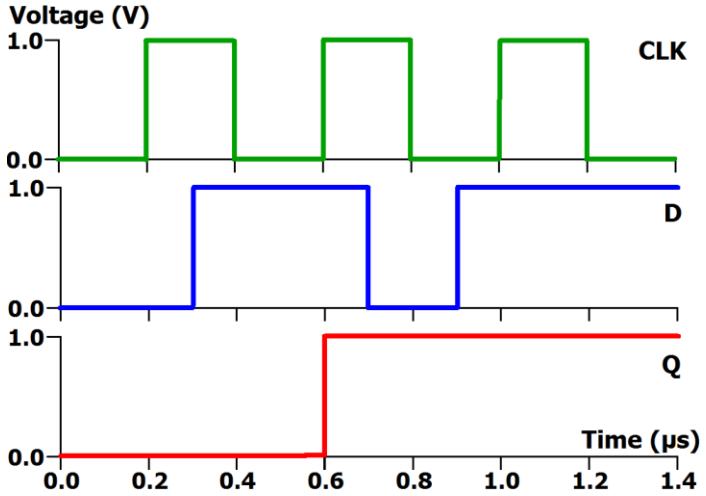

Figure 34. Simulation of the MDFF

Figure 33 shows that output Q of the NVDL changes instantaneously with input D whenever CLK is high. This proves that the NVDL functions as a latch. For the MDFF (figure 34), output Q only changes at the rising-edge of CLK. Between 0.2µs to 0.4µs, output Q remains the same although there is a change in input D at 0.3µs. Therefore, this proves that the MDFF functions as a flip-flop.

4.3.1 Time measurements

The output delay is the time taken for the output Q to change and switch voltage levels between 1V and 0V. It is measured from the time when the input of the sequential logic circuit is changed until the time when output Q reaches a stable voltage. The output delay of NVDL, MDFF, and CMOS D-latch and D flip-flop is shown in figures 35 and 36, and also summarized in table 4. The output delay for the NVDL to switch to logic '0' (0V) is shorter than that for MDFF because the NVDL only needs to collapse the conducting channels in one memristor. Conversely, the MDFF needs to switch two memristors at the same time; one memristor to HRS and another memristor to LRS. This also explains the output delay for MDFF is similar between output '0' and '1'.

Table 4. Output delays of sequential logic circuits

Sequential logic circuit	Output delay for logic '0' (ns)	Output delay for logic '1' (ns)
NVDL	0.030	0.270
MDFF	0.194	0.196
CMOS D-latch	0.190	0.160
CMOS D flip-flop	0.186	0.190

Although the NVDL exhibits a wide range of output delay, the output delay is 0.15ns, which is faster than the average output delay of the CMOS-based D-latch. However, the average output delay for the MDFF is longer than the CMOS-based D

flip-flop due to the larger number of transistors used in the circuit, which reduces current flow to output nodes.

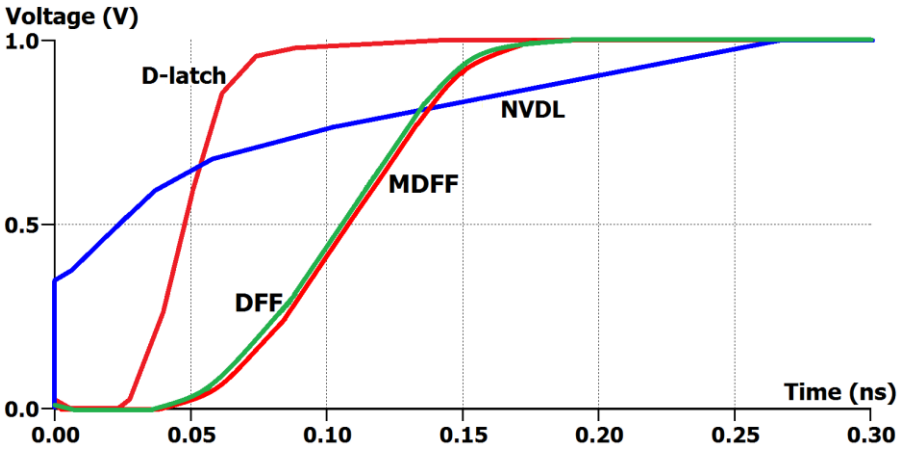

Figure 35. Output '1' delay of sequential logic circuits

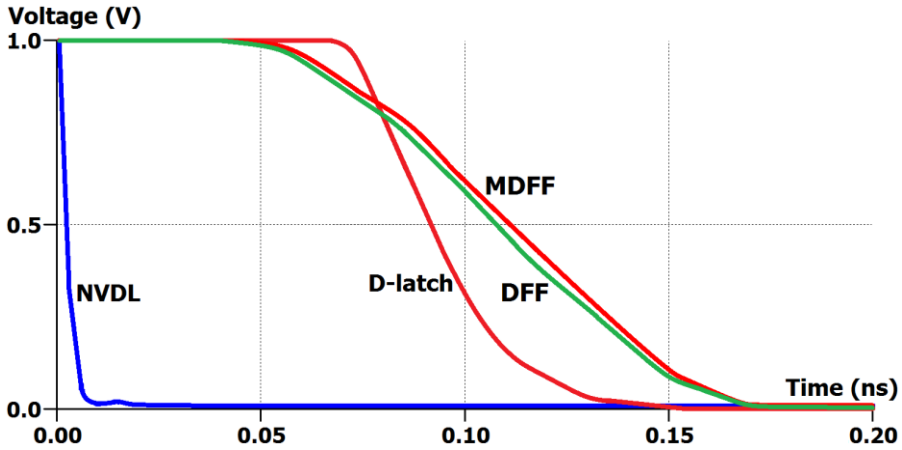

Figure 36. Output '0' delay of sequential logic circuits

Although it takes a very short time for input D to be transmitted to output Q, the memristors require an average of 143.93ns and 146.07ns to complete resistance switching in the NVDL and MDFF respectively. The resistive switching graphs are

shown in figures 37 and 38, and are applicable for both memristors for both cases of Q and $\bar{Q}$ at V_{DD} and 0V because the memristors are in reciprocal to each other, thus their resistance switching is identical. For example, the switching of M1 to HRS ($\bar{Q}$ at 0V) is similar to the switching of M2 to HRS (Q at 0V).

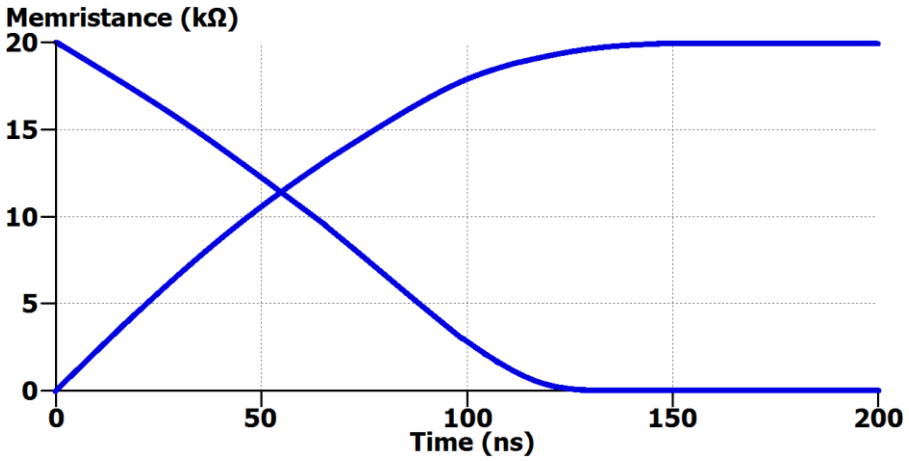

Figure 37. Resistive switching delay in the memristors of NVDL

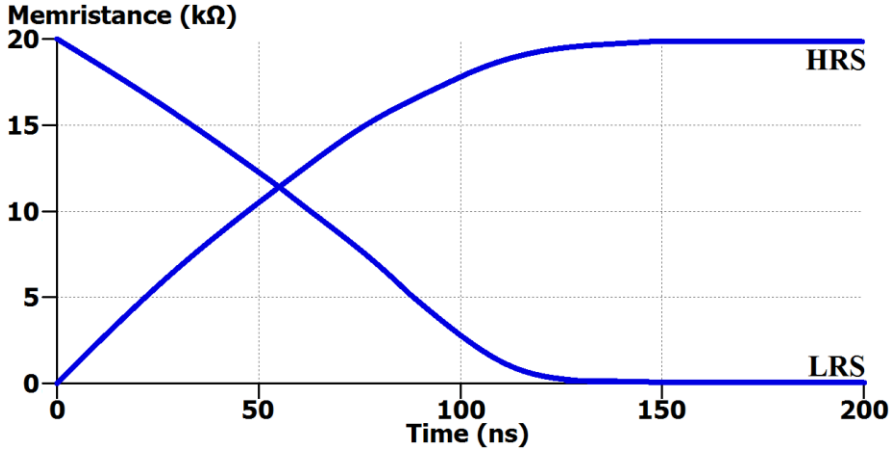

Figure 38. Resistive switching delay in the memristors of MDFF

The memristance switching simulation results show that the switching speed of NVDL is an average of 1.68 times faster than the 8T2R Nonvolatile Latch that takes between 225ns and 258ns to switch memristance states [122]. Switching speed of the MDFF is an average of 1.66 times faster than the memristor-based non-volatile latch circuit (243.16ns) [123]. However, the Zero-Sleep-Leakage Flip-Flop Circuit exhibited fastest switching speed of 100ns using the results published in [121].

4.3.2 Energy measurement and non-volatile features

Energy consumption of a circuit is measured by adding the energy consumed by each component in the circuit. Energy consumed by the CMOS D-latch to output '0' is 18.11fJ and 17.69fJ to output '1'. Energy consumed by the NVDL to output '0' is 0.44fJ and 2.78fJ to output '1'. For retrieving logic information from the memristors, the NVDL requires 8.07fJ and 8.01fJ to output logic '0' and '1' respectively, giving an average of 8.04fJ to retrieve logic information from the NVDL. This is compared to 18.11fJ and 17.69fJ required by the CMOS D-latch circuit to translate its input D to output Q, giving an average of 17.90fJ. This means that the average energy consumed by the CMOS D-latch to read logic information is 1.5 times more than the energy required by the NVDL to restore logic information. The reason for the low energy consumption of NVDL is the usage of memristance, instead of re-application of input power supply from input D. Thus, the overall energy consumption by the proposed NVDL is lower than the CMOS D-latch.

When operating at 5MHz, the power consumption of the NVDL is 626.20nW, which is relatively very high due to large amounts of current and programming the memristors at high frequency. However, when the non-volatile features of the NVDL is exercised as shown in figure 39, the average power consumption of the NVDL is reduced to 198.12fW, while the constant power consumption of the CMOS D-latch to operate at 5MHz or to retain logic information is 199.10pW. Thus, it is summarised that the NVDL ensures lower power consumption if the non-volatile feature is utilised by disconnecting the power supply to the NVDL, and only re-connected if logic information from the NVDL is required.

The average energy consumed by MDFF to output logic '0' and '1' is 1.464fJ and 0.008fJ respectively. To retrieve logic information from the memristors in the MDFF, an average energy consumption of 21.320fJ is required. Comparing this value against the NVDL that has similar structures to write and read the memristors, the energy consumption is higher due to the larger number of components in the MDFF than the NVDL. At clock frequency of 5MHz, the power consumption for the operation of MDFF is 58.06nW, giving average energy consumption of 11.612fJ per clock cycle. If the non-volatile feature is exercised (figure 39), the average operation of MDFF consumes only 37.16pW, whereas the constant power consumption of the CMOS D flip-flop to operate at 5MHz or to retain logic information is 16.80nW.

This shows that the non-volatile characteristics of the MDFF improve energy and power consumption. Similarly, the MDFF is advantageous over the CMOS D flip-flop only if the non-volatile features of the MDFF is fully utilised.

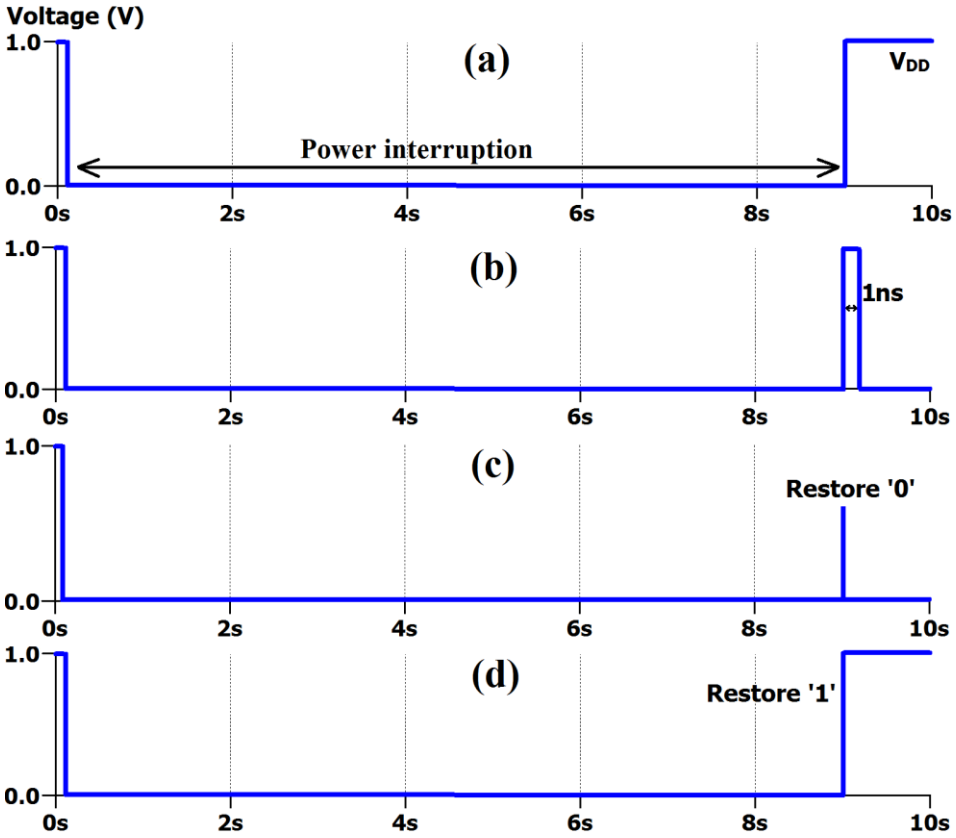

Figure 39. Restoration of logic information in the NVDL and MDFF circuits. (a) V_{DD} supply to the circuit. (b) Read signal, which is turned on for 1ns to retrieve logic information from the memristors. (c) Output Q when restoring logic '0'. (d) Output Q when restoring logic '1'.

The non-volatility of the NVDL and MDFF are shown in figure 39, where power supply V_{DD} is turned off from 0.06 s onwards, and turned on again from 9s onwards (figure 39(a)). Both simulation results are similar due to the similar structure of programming and restoring of logic information into and from the memristor respectively. According to simulation, it takes about 8s for the volatile inverter loop and CMOS D-latch to fully discharge and lose logic information. Thus at 9s, *READ* signal is triggered for 1 ns to restore logic information (figure 39(b)), long enough to draw sufficient current to switch the logic at output *Q*, as well as short enough to maintain memristance states [214].

During the read process, CLK signal is not activated, which shows that the restoring of logic information does not require the input signal D. When restoring logic '0', output Q rises to give a spike in voltage, but it does not reach V_{DD} and immediately falls to 0V (figure 39(c)). The rise and fall of this spike takes 13.94 ns. The reason for the spike when restoring logic '0' is due to $\bar{Q}$ discharged to 0V when power supply is disconnected and thus, it turns on the CMOS inverter that would momentarily channel V_{DD} into output Q when V_{DD} is reconnected to the circuit. After 13.94 ns, the current through the memristors restore the outputs Q and $\bar{Q}$ to logic '0' and '1' respectively. When restoring logic '1', output Q takes 16.54ns to be pulled-up to V_{DD} (figure 39(d)).

4.3.3 Device area

Device area of the proposed NVDL is improved against memristive-based latch circuits by a total of 13 transistors, whereas the memristor-based non-volatile latch circuit [123] uses an operational-amplifier in its design which would significantly increase device area. Furthermore, the NVDL does not require switches, which eases programming and reading of the NVDL, when compared to the memristor-based latch circuit proposed in [123]. Although the 8T2R Nonvolatile Latch [122] uses only 8 transistors in its design which amounts to 1.625 times of lesser device components, the energy consumption is 10^2fJ, which is about 12.5 times more than the proposed NVDL.

The MDFF uses 18 transistors, which is less than that compared to the Zero-Sleep-Leakage Flip-Flop Circuit which uses about 26 transistors [121]. However, both the MDFF and NVDL have larger device area than the CMOS D flip-flop and D-latch respectively by 2 transistors per circuit.

4.3.4 Summary of memristive sequential logic circuits (MSLC)

The proposed NVDL and MDFF circuits show non-volatile characteristics in the event of power interruption. Programming and restoring operations of both NVDL and MDFF were also demonstrated. Although the steady-states of NVDL and MDFF consume more energy than the CMOS circuits, the non-volatile nature of NVDL and MDFF allows the circuits to store logic information without power, thus reducing average power consumption.

In summary, two memristive sequential logic circuits (NVDL and MDFF) have been published which show improvements against the CMOS and other memristive D-latch and D flip-flops, in terms of switching speed and energy consumption. Therefore, the NVDL and MDFF are used wherever sequential logic circuits are required in the remainder of this research work, unless stated otherwise. The NVDL and MDFF are also used to replace CMOS sequential logic circuits.

5. COMBINATIONAL LOGIC CIRCUITS

COMBINATIONAL LOGIC CIRCUITS

5.1 2TG1M memory cell

Current CMOS-based LUTs use flash RAM as the memory cells, which volatile. Therefore, to build a non-volatile look-up table (NVLUT), a two transmission gate one memristor (2TG1M) memory cell (figure 40) was proposed and published [83]. The motivation for using transmission gates (figure 41) is due to conventional pass-transistors not being able to effectively pass high and low logic levels. The netlists of the 2TG1M memory cell and the transmission gate are attached in appendix D and E respectively.

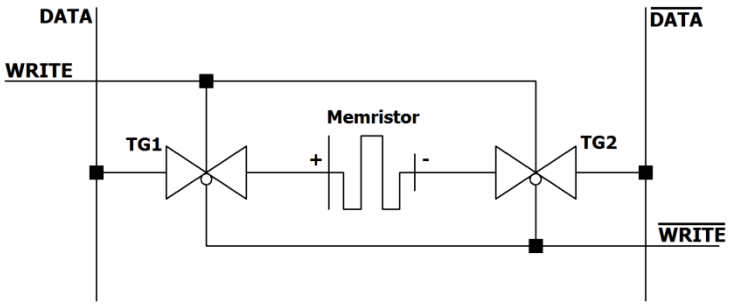

Figure 40. Schematic circuit of the two transmission gate one memristor (2TG1M) memory cell.

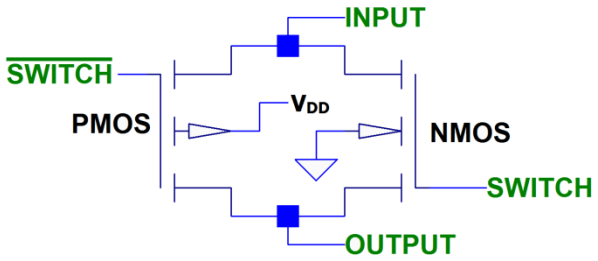

Figure 41. Schematic diagram of the CMOS transmission gate.

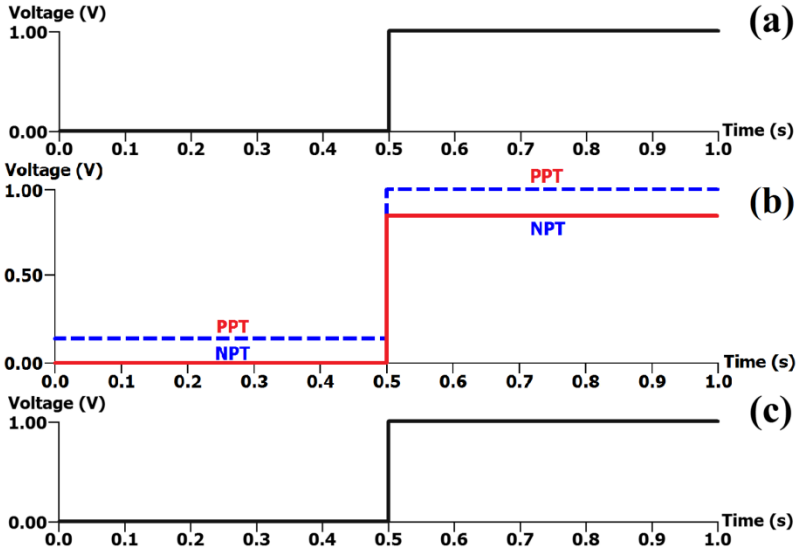

Figure 42. Simulation of pass transistors and transmission gate (a) Input voltage (b) NMOS and PMOS pass transistor output (c) Transmission gate output.

When both NMOS and PMOS pass-transistors are subjected to identical input signals (figure 42(a)), it is shown that NMOS pass-transistors are ineffective in passing high-logic levels, but can fully pass low-logic levels. Conversely, PMOS pass-transistors can pass high-logic levels, but is ineffective in passing low-logic levels. These outputs are shown in figure 42(b).

The usage of transmission gates ensure that both high and low logic levels are passed through the transistors effectively without any noticeable voltage dropped across the transmission gate. Simulation results of the transmission gate show that the output of the transmission gate is similar to its input (figure 42(c)).

The 2TG1M memory cell is controlled by two data lines, which are the complement of one another ($DATA$ and $\overline{DATA}$), and a write line $WRITE$, where $\overline{WRITE}$ is the complement. The data lines serve to write the memory cell with either a '0' or '1' by applying 0V or V_{DD} respectively to $DATA$. $WRITE$ is active high and is used to select the respective memory cell to be written. The proposed memory cell has two operations: (i) Write operation, and (ii) Read operation.

5.1.1 Write operation of 2TG1M memory cell

Data line $DATA$ is either charged to V_{DD} or ground, 0V. The purpose of the inversion of $DATA$ to create complementary $\overline{DATA}$ is to ensure that the magnitude of potential difference across the memristor whenever the memristor is selected for write operation is always V_{DD}. The data lines are connected to opposite ends of the memristor, where $DATA$ is connected to the positive terminal of the memristor through a transmission gate, while $\overline{DATA}$ is connected to the negative terminal of the memristor through another identical transmission gate.

To write a 2TG1M memory cell, the memory cell is selected by activating its respective write line. V_{DD} is applied to $WRITE$ and the high voltage in the write line creates a low impedance channel in the NMOS of the transmission gates, while $\overline{WRITE}$ is connected to the gate terminal of the PMOS of the transmission gates. This also creates a low impedance channel in the PMOS of the transmission gates. Therefore, the transmission gates connect $DATA$ and $\overline{DATA}$ to the memristor. If $DATA$ is charged to V_{DD} then $\overline{DATA}$ is grounded to 0V, and vice versa. Thus, this applies a potential difference magnitude of V_{DD} across the memristor.

When $DATA$ is charged to V_{DD}, the memristor is switched to its LRS due to current flowing from the positive terminal of the memristor to the negative terminal of the memristor. Current flows in this direction due to the more positive voltage at $DATA$. Thus, the 2TG1M memory cell is programmed with logic '1' when the memristor switches to its LRS.

To write logic '0' into the 2TG1M memory cell, $DATA$ is grounded and $\overline{DATA}$ is charged to V_{DD}. This causes a reverse potential difference across the memristor. The voltage at the negative terminal is larger than at the positive terminal and current flows through the memristor from the negative to the positive terminals. The memristor switches to its HRS and the 2TG1M memory cell is programmed with logic '0'.

5.1.2 Read operation of 2TG1M memory cell

To read the 2TG1M memory cell, a very short write pulse is signalled, enabling current to flow through the memristor. This very short pulse of write signal must be less than 5 ns in order to preserve the state of the memristor [214]. For the read operation, a sense-amplifier is used in this research work to detect and amplify the current drawn from the memristor. $DATA$ and $\overline{DATA}$ create a constant potential difference of 1V between the memristor terminals whenever the cell is selected. Thus, the amount of current drawn from the memristor is inversely proportional to the resistance of the memristor. A large current drawn from the memristor would signify a logic of '1' (LRS), while a small current drawn from the memristor would signify a logic of '0' (HRS). Since the direction of current is insignificant to the read operation, neither $DATA$ nor $\overline{DATA}$ needs to be pre-charged to V_{DD}. Hence, the read operation can work with either $DATA$ or $\overline{DATA}$ at V_{DD}.

5.2 Simulation results of 2TG1M memory cell

The 2TG1M memory cell was compared against the conventional volatile one-bit six transistor SRAM memory cell [215] and against the popular 1T1M memristive memory cell [124].

5.2.1 Comparison against one-bit SRAM memory cell

The simulation of the memristance of the memristor in the memory cells when writing logic '0' and '1' is shown in figure 43, where figure 43(a) is the $WRITE$ signal and figure 43(b) is the input $DATA$ connected to the 2TG1M memory cell.

Switching delay is measured by the time taken for the memristor in the 2TG1M memory cell to switch resistance states, starting from when $WRITE$ is active high. The switching delay of the 2TG1M memory cell is 4.01 ns to write logic '0' and 4.64 ns to write logic '1' (figure 43(c)), while switching delays of an SRAM memory cell is 86ps to write logic '0' and 74ps to write logic '1' (figure 43(d)). Thus, the SRAM memory cell has faster switching speed than the 2TG1M memory cell.

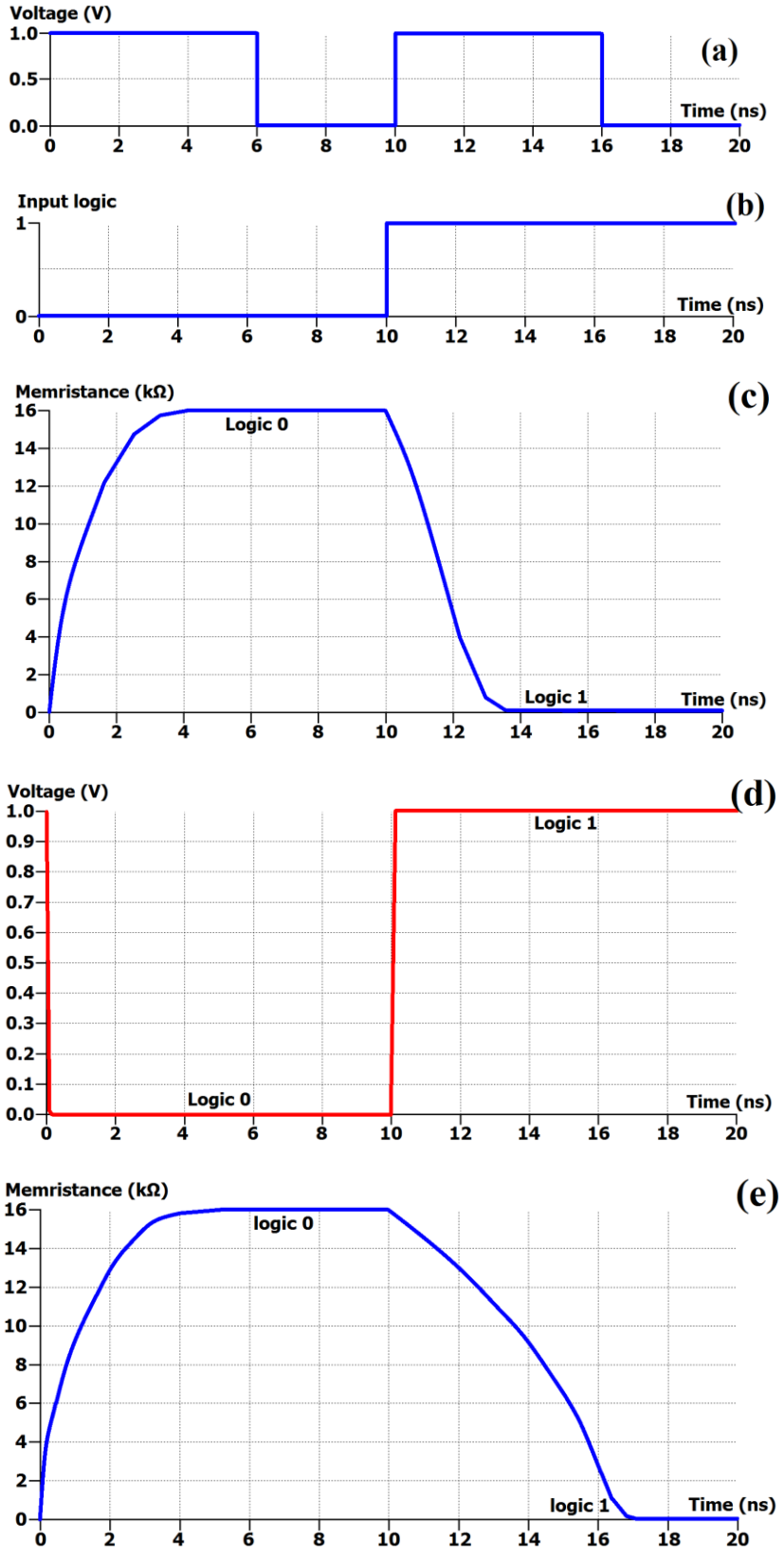

Figure 43. Simulation results of memristive memory cells (a) WRITE signal (b) Input logic to be written into memory cell (c) Memristance of memristor in the proposed 2TG1M memory cell (d) Output of SRAM memory cell (e) Memristance of memristor in the 1T1M memory cell.

However, to retain logic information, voltage must be constantly supplied to the SRAM memory cell due to its volatile characteristics. The constant supply of electric energy to retain logic information in SRAM memory cells means that energy requirements would be much higher for retention of logic information in the long-term. In oppose to this, the non-volatility of the 2TG1M memory cell ensures that logic information can be retained without power supply. This means that energy is only required by the 2TG1M memory cell during resistance switching, which is 1.88fJ to write logic '0' and 916.28fJ to write logic '1'. Energy consumption is measured by accumulating the amount of energy consumed by each component in the 2TG1M memory cell during switching process. Once switching is completed where memristances become stable, the 2TG1M memory cell will be able to retain its memristive state for as long as 10 years [216]. This means that for at least 10 years, the only time that energy is required by the 2TG1M memory cell is during write and read processes, regardless of the retention period.

The switching energy requirements of SRAM memory cell is much lower than the proposed memory cell, which is 0.54fJ to write logic '0' and 0.61fJ to write logic '1'. As an estimation, if an SRAM memory cell is supplied with power for one second to retain data for one second, the energy requirements are 73.034pJ to retain a logic '0' and 12.433nJ to retain a logic '1', as shown in figure 44. By extrapolation, retaining logic information in an SRAM memory cell for 1 hour would require about 262.92nJ for logic '0' and 44.76μJ for logic '1'.

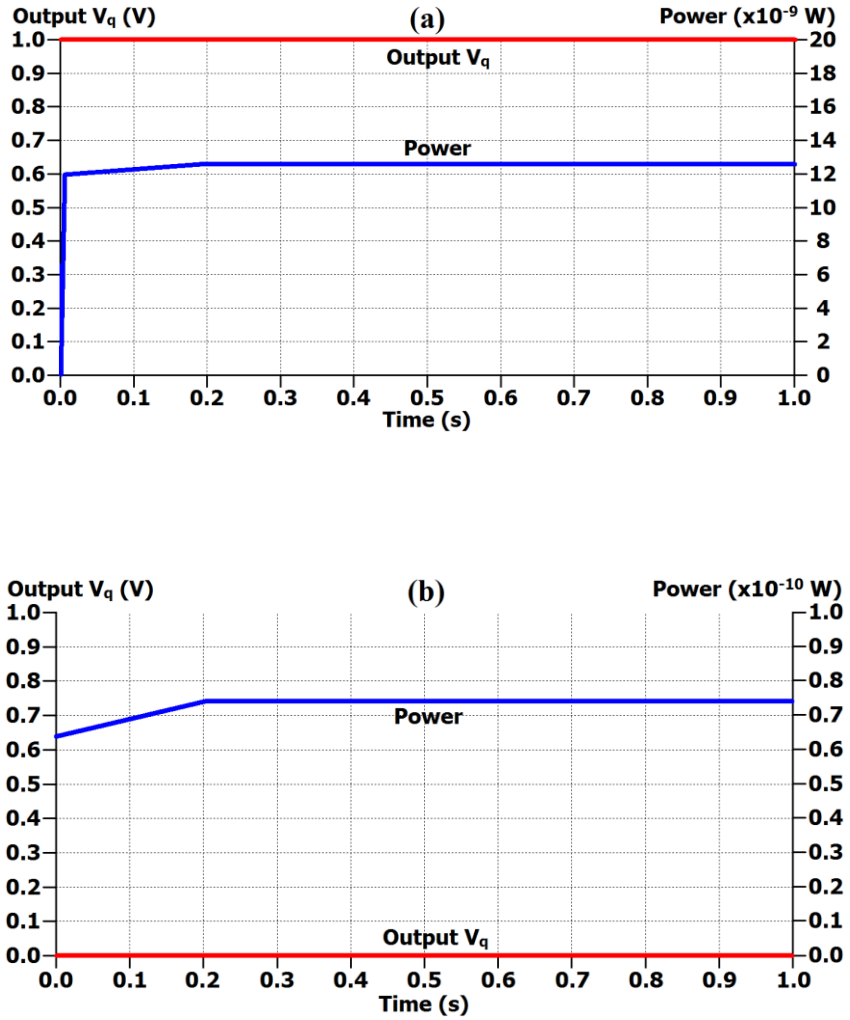

Figure 44. Energy dissipation for 1s in a one-bit SRAM memory cell when retaining: (a) logic '1' and (b) logic '0'

The energy cost would be 3.92J to retain logic '1' and 0.023J to retain logic '0' if the SRAM memory cell is continuously used for 10 years, which is about $4x10^{12}$ times the energy required by the 2TG1M memory cell for the same duration. This clearly shows that the switching speed of SRAM is offset by its high energy cost. Conversely, the reduction of energy consumption of the 2TG1M memory cell is proportional to retention period, despite switching 55 times slower than the SRAM memory cell.

5.2.2 Comparison against 1T1M memory cell

In the design of a 1T1M memory cell [124], an NMOS pass-transistor is used as the gate control of the memory cell, while the other end is usually grounded. A voltage is applied at the gate of the pass-transistor to control the input to the positive terminal of the memristor. If V_{DD} is applied at the gate of the NMOS pass-transistor, a low impedance conducting channel is created and the input voltage is applied to the pass-transistor and memristor in series. Due to a voltage drop across the pass-transistor, the voltage applied across the memristor, V_{MEM}, is lesser than the input voltage. V_{MEM} is equivalent to:

$$V_{MEM} = V_{CC} - V_{PT} \tag{14}$$

where V_{PT} is the voltage drop across the pass-transistor and V_{MEM} is the net potential difference applied across the memristor. In comparison to the 2TG1M memory cell, there is no voltage loss across the transmission gates. Thus, the net potential difference across the memristor in the 2TG1M memory cell equals to the input voltage of the memory cell, where:

$$V_{MEM} = V_{DD} - 0 = V_{DD} \tag{15}$$

The increased amount of potential difference across the memristor increases switching speed of the 2TG1M memory cell. The 2TG1M memory cell exhibits an average of 1.5 times faster switching speed than the 1T1M memory cell. The difference in switching speed is illustrated in figures 45 and 46. Simulation results

for energy requirements and the switching delays of the 2TG1M, SRAM and 1T1M memory cells are summarized in tables 5 and 6 for logic ‘1’ and ‘0’ respectively.

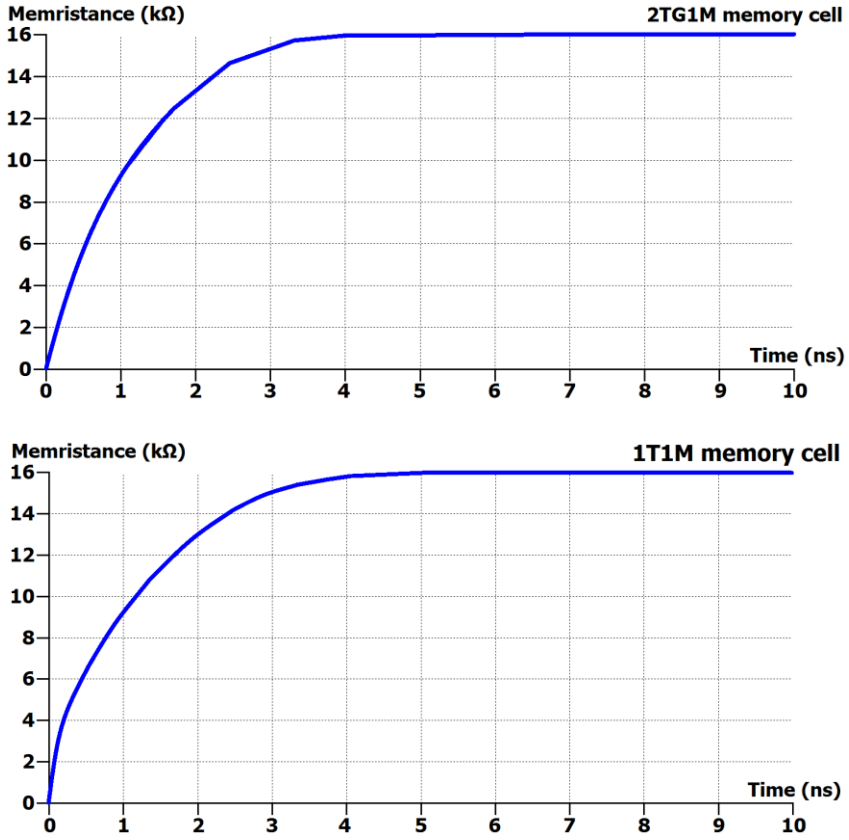

Figure 45. Simulations results of the proposed 2TG1M (4.64 ns) and the 1T1M (7.56 ns) memory cells when writing logic ‘1’.

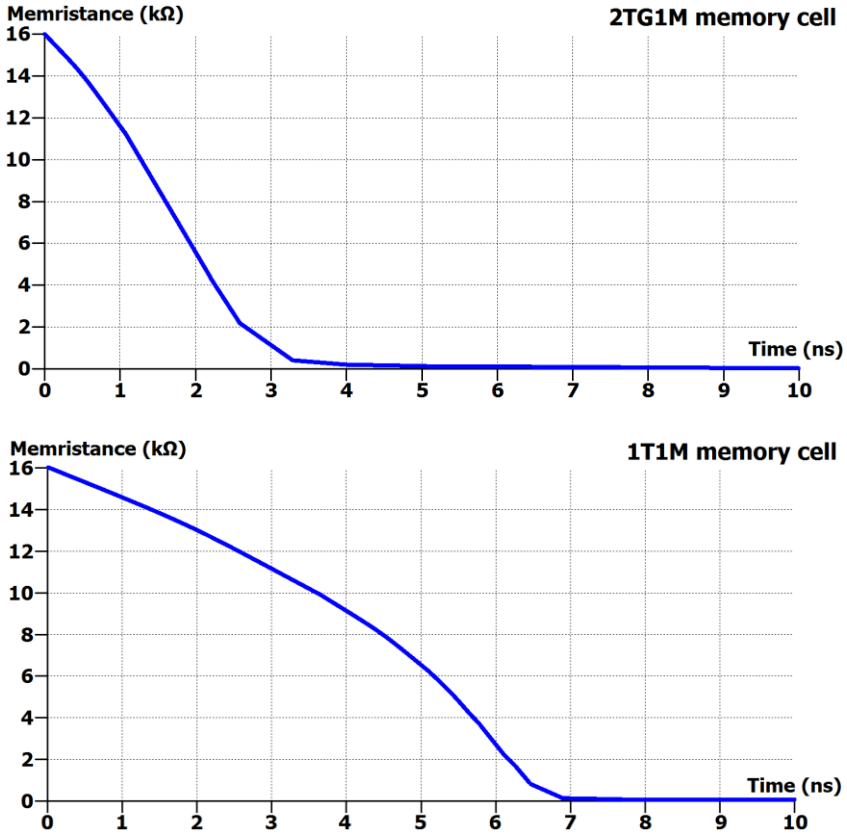

Figure 46. Simulations results of the proposed 2TG1M (4.01 ns) and the 1T1M (6.05 ns) memory cells when writing logic '0'.

Table 5. Comparison of switching delay and energy costs for writing logic '1'

Memory cell	Energy cost (fJ)	Switching delay (ns)
2TG1M	916.28	4.640
SRAM	0.61	0.074
1T1M	111.21×10^3	7.560

Table 6. Comparison of switching delay and energy costs for writing logic '0'

Memory cell	Energy cost (fJ)	Switching delay (ns)
2TG1M	1.88	4.010
SRAM	0.54	0.086
1T1M	930.31	6.050

5.3 Non-volatile Look-up Table (NVLUT)

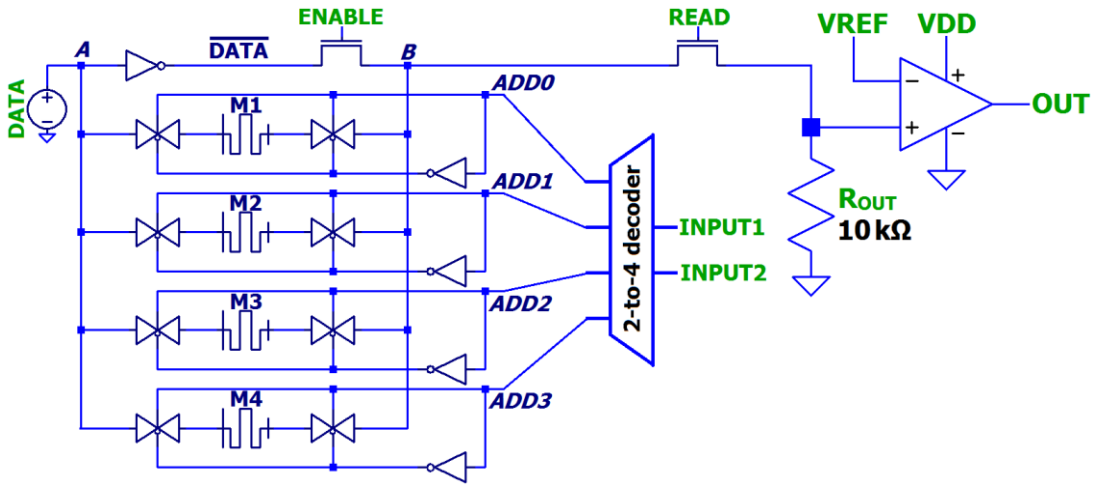

Figure 47. 2-bit input NVLUT constructed with four 2TG1M memory cells.

A 2-bit input Non-volatile Look-Up Table (NVLUT) is constructed using four 2TG1M memory cells that share $DATA$ and $\overline{DATA}$ inputs (figure 47) Instead of a one-bit $WRITE$ line, the array of 2TG1M memory cells are indexed using a 2-bit $INPUT$ that also act as the input signals of the NVLUT. $INPUT1$ and $INPUT2$ are decoded using a 2-to-4 decoder to select one of the four address lines (*ADD0* – *ADD3*).

At any time, the decoder charges only one of the address lines to V_{DD}, with its respective complementary address line discharged to 0V by a CMOS inverter. In the meantime, all other address lines are discharged to 0V with their respective complementary address lines inverted to V_{DD}. The inverters for each address line create their respective complementary to ensure that the PMOS gate in the transmission gates is grounded if the respective address is selected, or charged to

V_{DD} if the address line is not selected. Thus, only one of the 2TG1M memory cells in the NVLUT is accessed for writing or reading at any time.

5.3.1 Operation of NVLUT

During the writing phase, $DATA$ drives node A and the CMOS inverter *INV* forms $\overline{DATA}$ at node B. $ENABLE$ is charged to V_{DD} to connect $\overline{DATA}$ to the memory cells. The potential difference across the memristor of a memory cell is equal to the potential difference between A and B, where the magnitude is always V_{DD}. When a cell is to be written with logic '1', $DATA$ is charged to V_{DD} and $\overline{DATA}$ is at 0V. Thus, *INV* provides a path to ground via the NMOS in the inverter and current flows from $DATA$ to $\overline{DATA}$. Whereas when a cell is to be written with logic '0', $DATA$ is grounded to 0V ($\overline{DATA}$ is charged to V_{DD}). Thus, $DATA$ provides the ground for current to flow from the inverter *INV*.

$ENABLE$ is used to enable or disable writing processes in the array of memory cells. If $ENABLE$ is grounded, the pass-transistor is driven into cut-off mode, thus current path from or to the inverter *INV* is blocked. Thus, no matter what the voltage input at $DATA$ is, current cannot flow through any memristor and the memristances of the memristors does not change. Therefore, the logic information of the memory cells in the array is retained whenever $ENABLE$ is grounded, as shown in figure 48, from 150ns to 200ns.

To read a memory cell in the array, $INPUT1$ and $INPUT2$ are pre-charged to select the respective memory cell. $READ$ is then charged to V_{DD} and $ENABLE$ is grounded to initiate the reading process. The memristor and R_{out} creates a potential difference at the non-inverting input of the operational amplifier (op-amp). This potential is compared against a reference voltage, which is set to 0.5V. Thus, *OUT* is pulled-up to V_{DD} if memristance is at LRS and *OUT* is pulled-down to 0V if memristance is at HRS. Figure 48 shows the entire simulation of the programming process of the memory cells in the 2-bit NVLUT. The read circuit is not shown due to the flexibility in executing the read process, which is similar to the read process of CMOS-based LUTs.

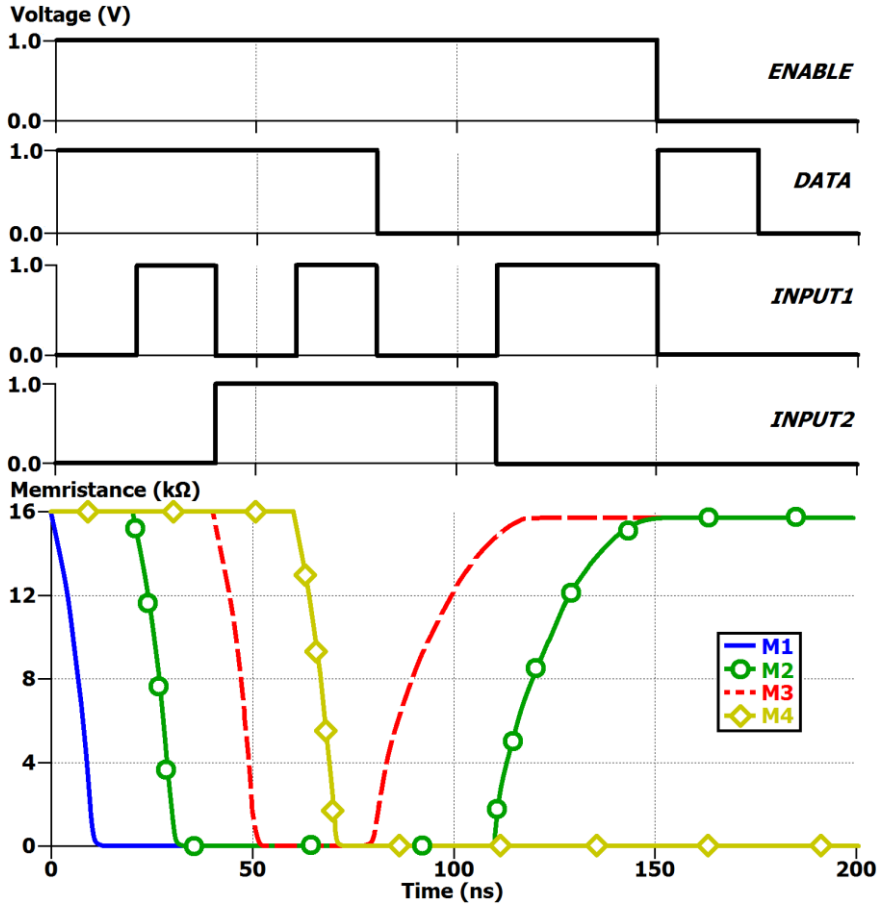

Figure 48. Simulation of the 2-bit NVLUT of 2TG1M memory cells.

5.3.2 Application of Boolean algebra into NVLUT

The following Boolean algebra is applied into the 6-bit input NVLUT:

$$X = (AB + CD) \cdot (E + F) \tag{20}$$

with 6 inputs ($A - F$) is programmed into the NVLUT. An extract of the truth table is shown in table 7. The memory cell of address '101100' (M45) is programmed with logic '0' ($(1 \cdot 0 + 1 \cdot 1) \cdot (0 + 0) = 0$), and the memory cell of address '101101' (M46) is programmed with logic '1' ($(1 \cdot 0 + 1 \cdot 1) \cdot (0 + 1) = 1$). This is executed by setting *INPUT 1-6* with '101101' and charging *DATA* to V_{DD}. Memory cell M46 is accessed and current flows from *DATA* to the positive terminal of the memristor in memory cell M46. The memristance switches to LRS and memory cell M46 is programmed with logic '1'. Hence, when the inputs of the NVLUT are '101101', memory cell M46 is read and the output of the NVLUT is logic '1'. Likewise, setting INPUT 1-6 to '101100' and discharging DATA to 0V programs memory cell M45 to logic '0'.

Table 7. An extract of the truth table for X = (AB + CD) · (E + F)

A	B	C	D	E	F	X
0	0	0	0	0	0	0
0	0	0	0	0	1	0
0	0	0	0	1	1	0
0	1	1	1	0	0	0
0	1	1	1	1	0	1
1	0	0	0	0	0	0
1	0	1	1	0	0	0
1	0	1	1	0	1	1
1	1	0	0	0	0	0
1	1	1	1	1	1	1

5.3.3 *Expansion of NVLUT*

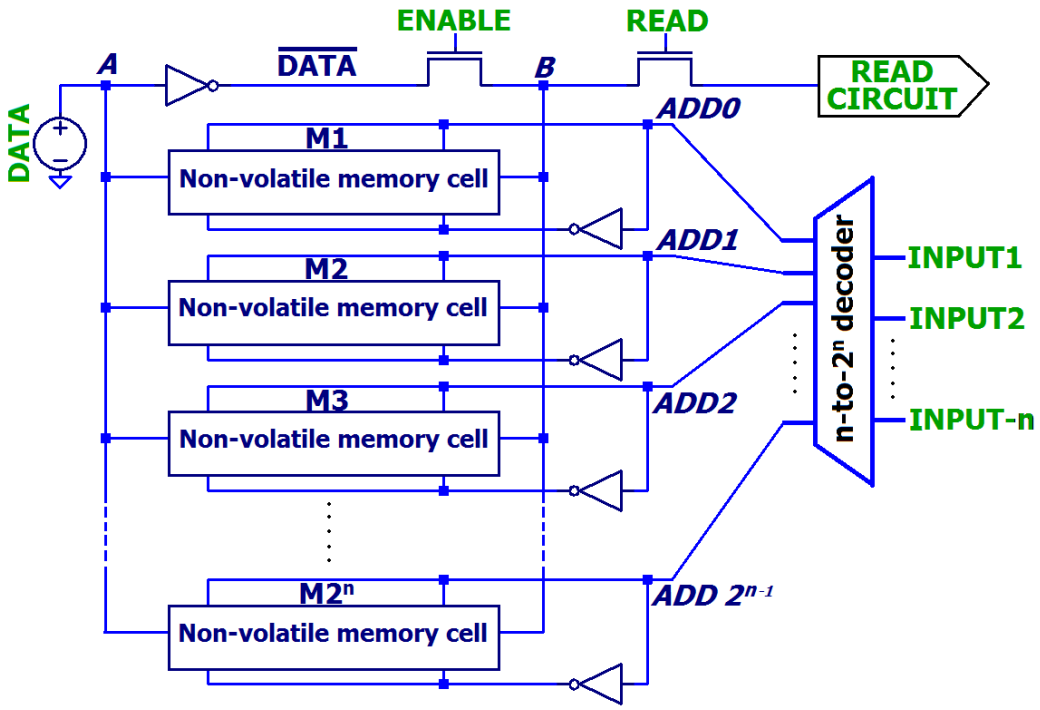

Figure 49. n-bit input NVLUT constructed with non-volatile one-bit memory cells

Using a similar structure to that shown in figure 47, the 2-bit input NVLUT is expanded to 3-, 4-, 5- and 6-bit input NVLUTs. The general n-bit NVLUT is shown in figure 49, while the netlist for the 6-bit input NVLUTs is attached in appendix G. The NVLUTs can also function as an array of memory cells, by using input lines as the address word and the memory cells as the array memory. Using similar configuration to the 2-bit input NVLUT, the structure can be expanded to become 8-, 16-, 32- and 64-bit array of memory cells.

5.4 Analysis of NVLUT using different memristive memory cells

For selection of non-volatile memory cells to be used in the general n-bit NVLUT, memristive one-bit memory cells in the literature that are suitable to be used in an array [83], [124]–[126] are simulated and compared, in terms of switching energy requirements, device area, switching speed, and flexibility of application. The comparison is based on the following aspects: (i) switching energy, (ii) device area, and (iii) switching speed.

In each of the memristive one-bit memory cells that are being analysed [83], [124]–[126], a reference voltage is placed at the opposite end of a memristor. The magnitude of input voltage is either larger or smaller than the reference voltage, but of the same polarity. This creates a bidirectional current through the memristor using a single unipolar voltage source.

5.4.1 Switching energy consumption

Energy consumption is observed starting from the moment the memory cell is selected for writing or reading until the time when the memristor completely switches resistance states or when the logic information is fully switched. Energy consumption of every component used in the design of the memory cells are taken into consideration when determining the amount of energy consumed by the memory

cell during switching. The simulation of the average energy consumption of the memory cells are summarized in table 8. The reason for the similar energy consumption for writing logic '0' and '1' is due to the similar potential difference applied across the memristor when writing logic '0' and '1' in the 2TG1M memory cell. For other memory cells, the net potential difference across the memristor is different due to different structure of memory cell and different components used. Thus, the energy consumption for write operation in other memory cells is different between writing logic '0' and '1'.

Table 8. Average energy consumption of memristive memory cells.

Memory cell	Write Operation (J)	
	Logic '0'	Logic '1'
2TG1M [83]	1.66×10^{-12}	1.66×10^{-12}
1T1M [124]	350.60×10^{-12}	1.67×10^{-12}
2A1M [125]	1.23×10^{-12}	2.83×10^{-12}
3T2M [126]	0.67×10^{-12}	1.82×10^{-12}
6T SRAM	0.42×10^{-12}	0.57×10^{-12}

Compared to the 1T1M memory cell [124], the 2TG1M memory cell uses lesser energy because the transmission gate allows a complete pull-up or pull-down of input voltage. There is a voltage dropped across pass transistors, which are also used in the other memristive memory cells. This causes energy wastage through the pass transistors. It is also shown that the 2A1M memory cell [125] have higher energy consumption than the 2TG1M memory cell due to the usage of two pass transistors in series with the memristor in the 2A1M memory cell, which causes two times more voltage drop across the pass transistors and reduced voltage drop across

the memristor. This causes larger energy losses, and results in a poor ratio of energy conversion.

Relying on $V_{DD}/2$ and $V_{DD}/4$ voltage references in the 3T2M memory cell [126], the voltage lost across the pass transistors is lower in the 3T2M memory cell than the 2TG1M and 2A1M memory cells. Consequently, power consumption of the pass transistors in the 3T2M memory cells is lesser. Thus, the overall energy consumption when switching the 3T2M memory cell would be lower than both the 2TG1M and 2A1M memory cells. 1T1M memory cells have the highest energy consumption due to the largest fraction of input voltage dropped across the pass-transistor in the cell.

Although the 6T SRAM has lower switching energy requirements per writing cycle, the SRAM memory cell requires constant voltage supply to ensure logic information is not lost. Through simulations, the energy required to operate and retain logic information in an SRAM memory cell for 1 second is 12.433nJ for logic '1' and 73.034pJ for logic '0'. By extrapolating, SRAM memory cells will require 3.92J to retain logic '1' and 0.023J to retain logic '0' to retain logic information for 10 years. Conversely, the 2TG1M memory cell requires only 1.66pJ to write logic '0' or '1' because memristors has the ability to retain logic information for 10 years [216]. This means the SRAM requires an average of 1.19×10^{12} times more energy to retain logic information for 10 years.

5.4.2 Device area of NVLUT

Device area can be calculated by the number of transistors used per memory cell. The size of one transistor is f^2, where f is the half-pitched length of transistors. Memristors are fabricated in the via between metal layers in a semiconductor device fabrication [72], hence the memristor device area can be neglected compared to transistor size. Ambipolar transistors show a great potential in offering flexibility of designing transistor logic circuits, but the width of ambipolar transistors is 175nm [217], which are larger than transistors. Thus, the device area of the 2A1M memory cell is approximately at least $4f^2$.

The 3T2M memory cell requires $V_{DD}/2$ and $V_{DD}/4$ references, which would require more circuit components. The gate control also requires an OR-gate, which uses an additional of at least 4 transistors, making the 3T2M memory cell requiring a total of 7 transistors. This amounts to larger device area required per memory cell (at least $7f^2$).

The 1T1M memory cell has the smallest device area among compared memristive memory cells, due to the design requiring only one transistor and one memristor and the device area is f^2. The disadvantage of the 1T1M memory cell is that writing logic '0' requires a negative potential (-1V) if the other of the memory cell is connected to ground. This reduces the flexibility of designing using 1T1M memory cell. Moreover, digital information is transmitted between 0V and V_{DD}.

Thus, more circuit components may be required to incorporate the 1T1M memory cell into digital circuits.

The proposed 2TG1M memory cell requires a device area of $6f^2$ due to the usage of two PMOS transistors, where each PMOS transistor ($2f^2$) is twice the width of each NMOS transistor to ensure that the pull-up and pull-down of both NMOS and PMOS are equal. The device area utilized by each unit of memristive memory cell is summarized in table 9.

Table 9. Summary of device area utilized by each unit of the memristive memory cell.

Memory cell	Device area per memristive memory cell
2TG1M [83]	$6f^2$
1T1M [124]	f^2
2A1M [125]	$4f^2$
3T2M [126]	$7f^2$
6T SRAM	$8f^2$

5.4.3 Switching speed of memory cells in NVLUT

The memristor is the main memory storage element and the major factor in determining the switching delay of a memristive memory cell is proportional to the speed of resistance switching process in the memristor. The speed of charge carriers tunnelling through the bulk layer of memristors is proportional to the magnitude of the voltage between the terminals of the memristor [218]. Thus, the switching speed

is proportional to the effective magnitude of voltage across the memristor in a memristive memory cell, which may be lesser than the voltage applied at the input or the voltage supplied to the memristive memory cell.

Switching speed is defined that the switching speed of a memristive memory cell is equivalent to the amount of time for a memristor to completely switch resistance states. This is determined by measuring the time when the memory cell is enabled for writing process until the time when the memristor has completely switched resistance states or has reached the memristance levels as defined in the memristor model. The required writing time of the memory cells studied in this research are summarized in table 10 and graphically compared in figure 50.

Table 10. Writing time of memristive memory cells.

Memory cell	Write time (ns)	
	Logic '0'	Logic '1'
2TG1M [83]	14.67	12.14
1T1M [124]	18.86	27.22
2A1M [125]	47.13	56.00
3T2M [126]	44.17	102.12
6T SRAM	0.05	0.10

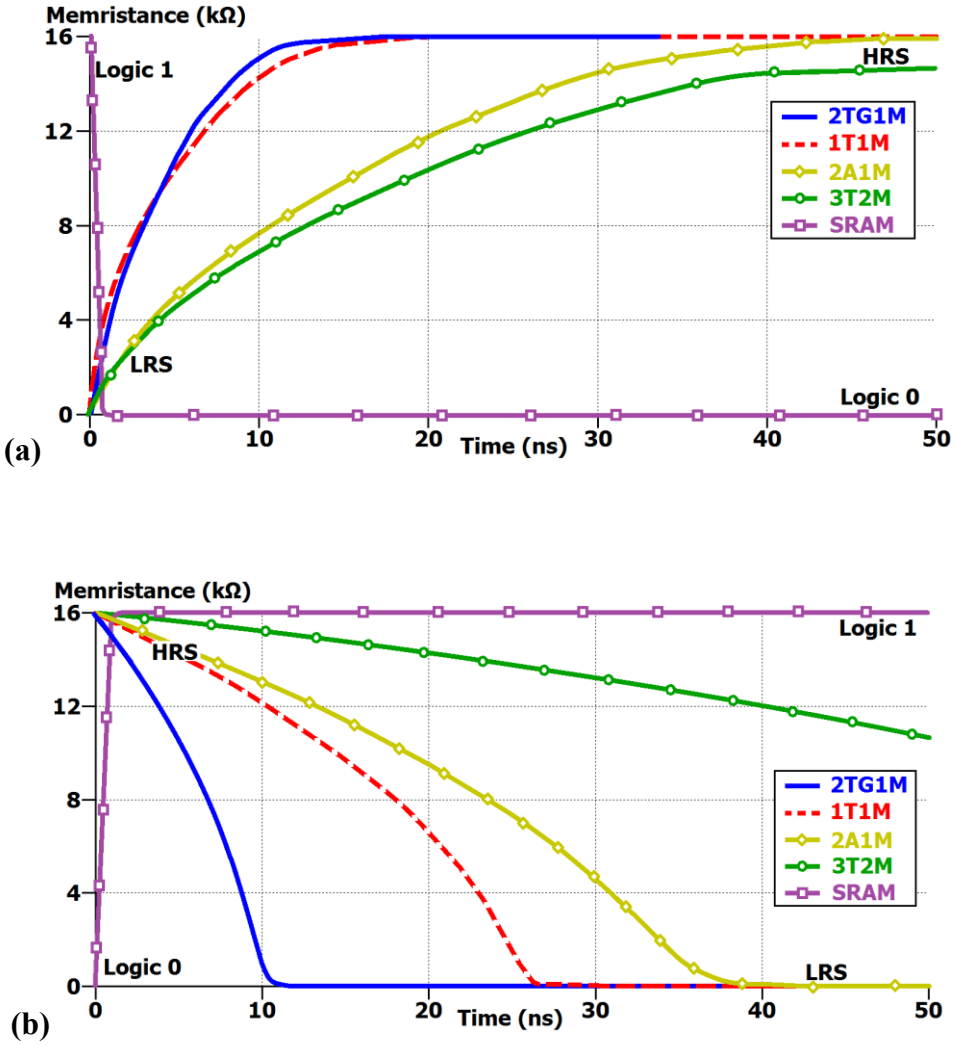

Figure 50. Switching delay of NVLUT using different memristive memory cells when storing (a) logic '0' and (b) logic '1'. The graph for SRAM uses an arbitrary scale to represent switching between logic '0' and '1'.

The 3T2M memory cell uses $V_{DD}/4$ as a voltage reference during writing operation of the memory cell [126]. Effectively, the potential difference across the memristor in the 3T2M memory cell would be $V_{DD} - V_{PT} - V_{DD}/4$, where V_{PT} is the voltage loss across a pass transistor. With V_{DD} of 1V, V_{PT} is 0.2V and $V_{DD}/4$ is 0.25V. This gives an effective potential difference of 0.55V applied across the memristor. A substantial amount of voltage is lost through other components of the

memory cell and causes the very slow switching operation of the 3T2M memory cell.

The 2A1M memory cell also has a lesser magnitude of potential difference applied across the memristor compared to the 2TG1M memory cell. This is due to the voltage lost across two pass-transistors that are in series with the memristor. The potential difference across the memristor is $V_{DD} - 2(V_{PT})$, which roughly equals to 0.6V. The assumption is that there is no voltage loss across the ambipolar transistors. The slightly larger potential difference across the memristor in the 2A1M memory cell gives faster switching speed than the 3T2M memory cell. Similarly, the magnitude of the potential difference across the memristor in the 1T1M memory cell is $V_{DD} - V_{PT}$, which roughly equals to 0.8V. Thus, the switching speed of the 1T1M memory cell is faster than the 2A1M and 3T2M memory cells.

The switching speed of the 2TG1M memory cell is the highest and the contributing factor to this advantage is the large magnitude of potential difference applied across the memristor. The ratio of the potential difference across memristor to input voltage is 100%, due to the pass transistors fully transmitting input voltage to output voltage almost without any significant loss of voltage across it. Therefore, with the components used in every memory cell under comparison are identical, the switching speed of the 2TG1M memory cell is be the fastest.

5.4.4 Energy-Delay-Area product comparison of NVLUTs

The memristive one-bit memory cells do not excel in every performance criteria that they are being evaluated on (energy, device area, and switching speed). For example, the 1T1M memory cell uses the least device area per cell, but suffers from high energy consumption. Similarly, the 2TG1M has the fastest switching speed and lowest energy consumption, but suffers from a large device area. Thus, a single performance index is required to estimate the overall performance of the memristive memory cells.

Energy-Delay-Area Product (EDAP) is used as the performance index, which is the product of energy consumption, switching delay, and device area of a memory cell. The value of EDAP is inversely proportional to the overall performance of the memory cell. The EDAP results are as follows in table 11, which shows that the 2TG1M memory cell has the lowest EDAP value. This summarizes that the 2TG1M has the superior overall performance among memristive memory cells.

Table 11. Summary of results of energy, delay, and device area, and values of Energy-Delay-Area Product for the memristive memory cells.

Memory cell	Energy (fJ)		Delay (ns)		Device area	EDAP (fJ-ns)
	Logic '0'	Logic '1'	Logic '0'	Logic '1'		
2TG1M [83]	1.66	1.66	14.67	12.14	$6f^2$	2944.53
1T1M [124]	350.60	1.67	18.86	27.22	f^2	300578.69
2A1M [125]	1.23	2.83	47.13	56.00	$4f^2$	36748.28
3T2M [126]	0.67	1.82	44.17	102.12	$7f^2$	38501.92

5.5 Comparison against SRAM-based LUT

An LUT of SRAM memory cells is also constructed with similar structure to that in figure 51 for 2-, 3-, 4-, 5- and 6-bit input LUTs. The NVLUT, constructed with 2TG1M memristive memory cells and the SRAM LUT are compared in terms of switching delay, energy requirements and device area. The comparison is performed for one complete cycle of write and read processes for logic '0' and '1'. The transistor sizing and LTspice version is the same for both types of LUTs.

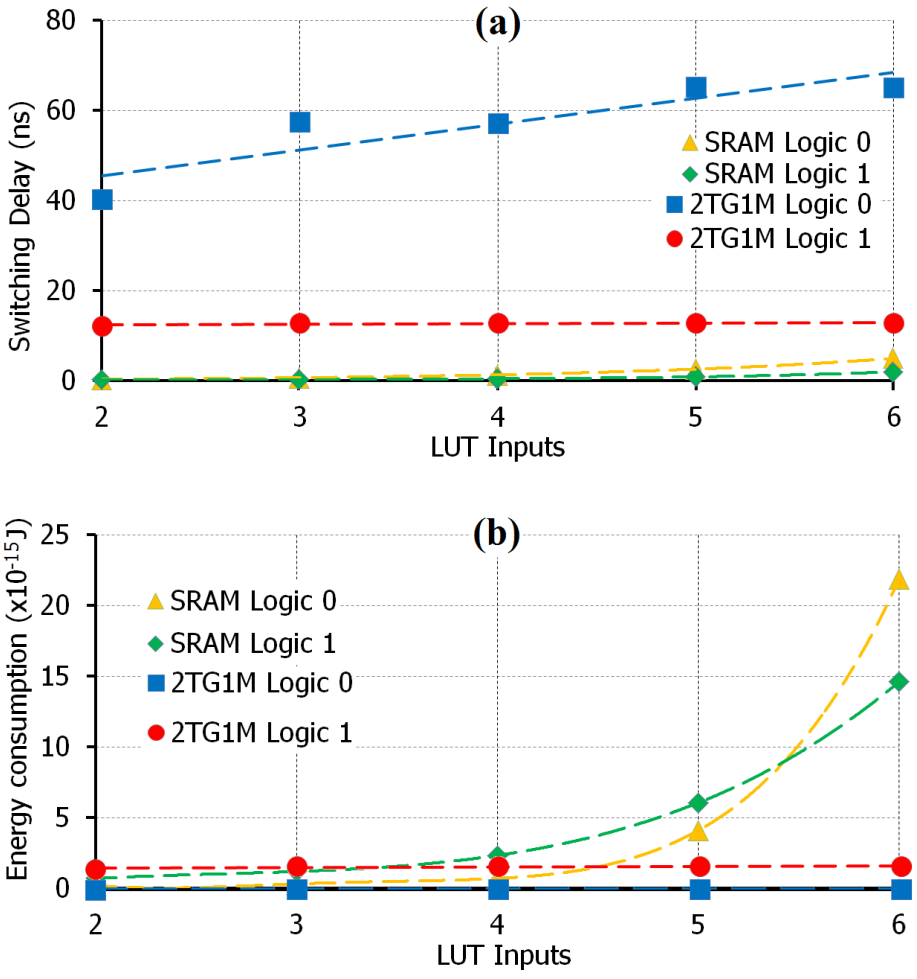

Figure 51. (a) Switching delay and (b) energy consumption of 6-bit input NVLUT of 2TG1M memory cells and LUT of SRAM memory cells.

The average switching delay (average of write and read) and energy requirements are shown in figures 51(a) and 51(b) respectively. The results show that the performance of the proposed NVLUT is more linear against the number of input bits than the SRAM LUT. Table 12 also shows that the 6-bit input NVLUT has very consistent switching times and energy requirements among its memory cells compared to a 6-bit input LUT of SRAM cells. This is attributed to the identically repeated memory cells used in the proposed NVLUT. The almost identical memristors used in each 2TG1M memory cell ensures a reduction of fluctuations of write and read delays between memory cells in the proposed NVLUT, even with a larger number of memory cells in the NVLUT. Therefore, based on simulation results, an array of 2TG1M memory cells would result in a more consistent performance even at larger number of memory cells in the NVLUT.

Table 12. Writing time and energy requirements of memory cells in a 6-bit input NVLUT of 2TG1M memory cells and LUT of SRAM memory cells.

Address	Writing time (ns)				Energy requirements ($x10^{-12}$ J)			
	2TG1M		SRAM		2TG1M		SRAM	
	Logic '0'	Logic '1'	Logic '0'	Logic '1'	Logic '0'	Logic '1'	Logic '0'	Logic '1'
0	65.13	12.79	4.63	2.52	0.0087	1.6205	0.0267	0.0190
31	65.13	12.79	5.63	2.23	0.0087	1.6205	0.0172	0.0124
32	65.13	12.79	4.62	2.40	0.0087	1.6205	0.0265	0.0190
63	65.13	12.79	5.60	1.07	0.0087	1.6205	0.0172	0.0081

The read-out delay of the NVLUT using 2TG1M memory cells is a minimum of 1.0ns to draw current into the read circuit through the memristor, whereas for the

LUT using SRAM cells, the read-out delay is an average of 3.6ns. This is based on the same type of read-out circuit.

CMOS-based LUTs are constructed with flash RAM and these memory cells consume an average of 26.50fJ and the switching delay is 5.60ns, while the complete operation of the CMOS-based LUT (read, write, and steady-state) consumes an average of 66.05nW. Using the 6-bit input NVLUT reduces power consumption by an average of 6.25nW for its complete operation, but writing speed is an average of 33.33ns slower than the SRAM-based LUT. However, the read-out delay for the NVLUT is faster by 4.95ns, because of the capacitive loading of the SRAM cells in the SRAM-based LUT which slows charging and discharging of output, while the NVLUT read-out is obtain through a voltage pulse of 5ns through the memristor. The read operation is at maximum of 5ns to prevent memristance change [219], [220]. The path delay through a 6-bit input NVLUT is the time between addressing the NVLUT to obtaining the logic information from the NVLUT, which is 0.321ns.

The 6-bit input NVLUT requires a total of 256 transistors. Each 2TG1M memory cell uses 4 transistors (2 NMOS and 2 PMOS), and the 6-to-64 decoder requires a total of 396 transistors (198 NMOS and 198 PMOS). On the other hand, the 6-bit input LUT of SRAM cells uses 384 transistors, where each SRAM cell uses 6 transistors of 4 NMOS and 2 PMOS, while the 6-to-64 decoder remains the same. Therefore, the 6-bit input NVLUT reduces device area by 128 transistors against the 6-bit input SRAM LUT.

5.6 Switching time against transistor width

From simulation experiments of the proposed NVLUT, it is observed that the switching time is inversely proportional to transistor size. Smaller transistor widths mean that the transistor allows lesser electric current flowing through its channel. Since electric current is usually proportional to the potential difference across a resistive component, channelling more current towards a memristor results in faster switching speeds. Figure 52 shows the switching speed is inversely proportional to transistor sizing used in the 2TG1M memory cell in the proposed NVLUT, where the width of PMOS is twice the width of NMOS transistors.

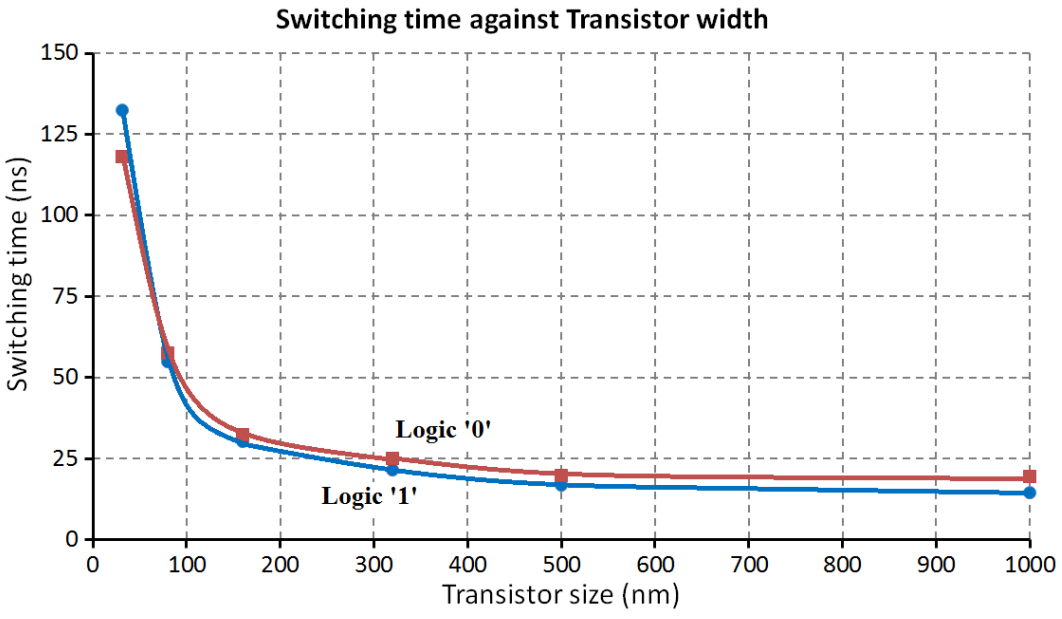

Figure 52. **Switching time of writing logic '0' and '1' against NMOS transistor widths (PMOS width is twice of NMOS width).**

5.7 Memristive Ratioed Logic (MRL)

Memristive Ratioed Logic (MRL) circuits [127]–[131] were proposed to replace CMOS-based logic gates. However, it was hypothesized that these MRL circuits would not be able to function properly due to the resistive switching delay in the memristors that would cause a delay in the propagation of logic signals when used in a combinational logic circuit. To prove this, the MRL circuits are used in a combinational circuit with the Boolean algebra (16). The CMOS-based logic gates circuit for this Boolean algebra is shown in figure 53.

$$X = AB + CD \tag{16}$$

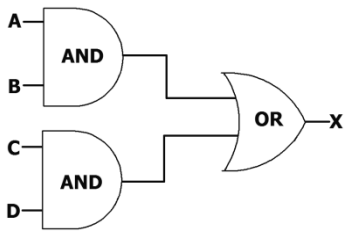

Figure 53. Boolean algebra X = AB + CD realized using CMOS logic gates.

Several designs of MRL circuits have been proposed but the structure, function and operation are very much similar to each other [127]–[131]. Since the operation and function of the MRL circuits are almost identical, using only one design for research would suffice and the MRL circuit proposed in [128] is used in the simulation experiments.

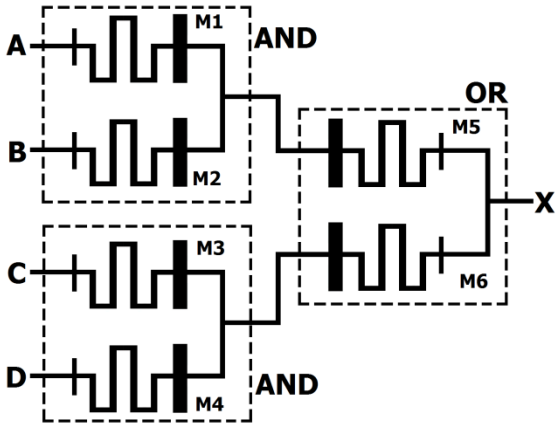

Figure 54. Schematic circuit for the MRL circuit implementing the Boolean algebra (16) X = AB + CD.

Figure 54 shows the schematic circuit for the MRL circuit implementing the Boolean algebra (16). Figure 55 shows the simulation results, which confirms that the MRL circuit shows slight deviation and delay in its output. If the signal frequency is higher than 20MHz (period slower than 50ns), then the MRL combinational circuits will not function properly. This is due to the insufficient path delay for signals to propagate from one MRL to the next cascading MRL. The insufficient amount of time of the application of the input signals does not allow the memristors to fully switch states at higher frequencies.

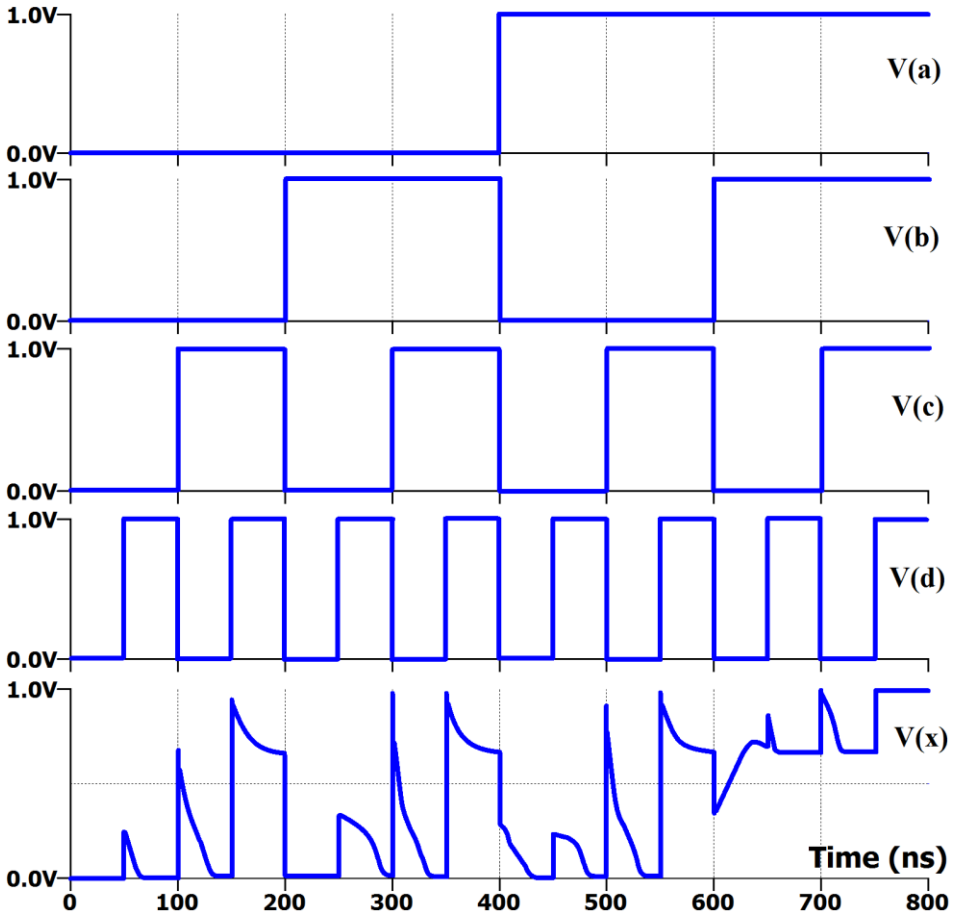

Figure 55. Simulation of the MRL circuit in figure 54.

For example, when input ABCD changes from "0001" to "0010" (at 100ns of the simulation in figure 55) memristors M3 and M4 changes from LRS and HRS to HRS and LRS respectively. This results in the overall resistance in the circuit changes, which then results in the output voltage changing from 0.6V to 0V, which is seen from 100ns to 135ns. Although the correct output of 0V is observed, the output delay of 35ns is not desirable.

As such, the MRL combinational circuits are added with buffers to increase the delay in propagation from one MRL to the next cascading MRL, shown in figure 56. The buffered MRL combinational circuit is found to behave accordingly to different

signal frequencies (figure 57). Adding buffers allow the delay to be shortened. The correct output of 0V when changing inputs ABCD from “0001” to “0010” is also observed with a shorter delay of 10ns (100ns to 110ns, figure 57).

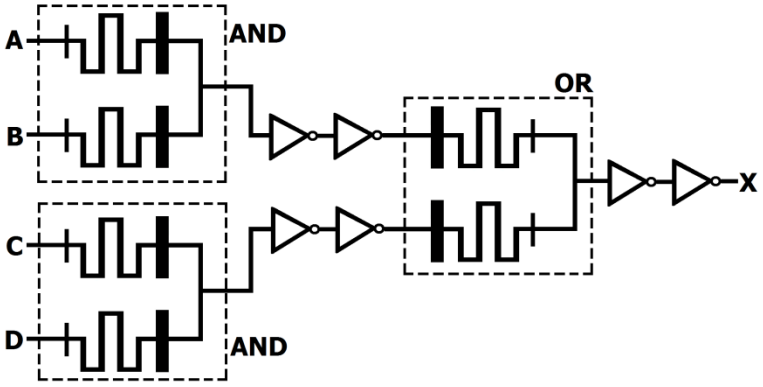

Figure 56. Improved MRL circuit by inserting buffers.

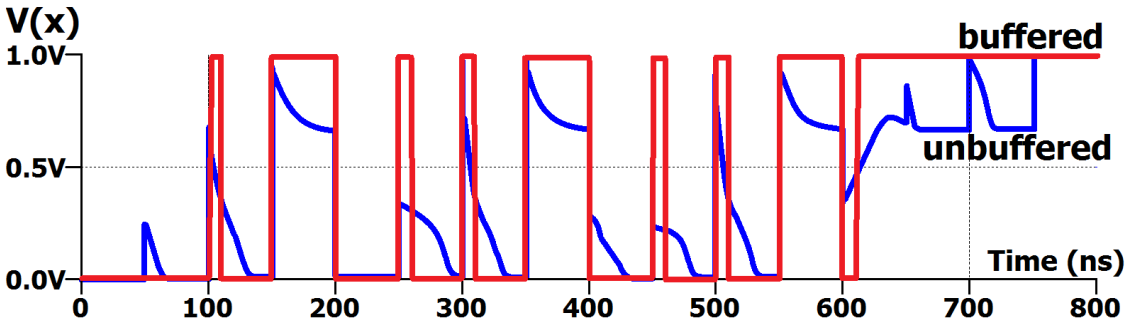

Figure 57. Simulation of the improved MRL circuit with buffers.

Although the addition of buffers in the MRL combinational circuit allow it to work at different signal frequencies, the MRL combinational circuits are still volatile and does store or retrieve logic information. This is because the power supply of the output of MRL depends on the input voltage supply to the MRL. Removing the input

thus removes the output. If input voltage supply is interrupted, the exact same input must be re-connected for the previous output to be retrieved. Otherwise, there is no other way to retrieve the previous information, which makes MRL a volatile device. Therefore, it is concluded that the MRL circuit is not a non-volatile logic gate although it uses memristors.

The following section introduces the Memristive Logic Gates which can function both as logic gates and as non-volatile memory devices. The proposed design makes full use of the non-volatility of memristors and logic gates that uses lesser energy consumption.

5.8 Memristive Logic Gate (MLG)

The Memristive Logic Gate (MLG) has been submitted for possible publication. Two MLGs are proposed: OR-MLG (figure 58) and AND-MLG (figure 59), which functions as OR and AND logic gates respectively. The MLG has two input (A and B) and one output (V_o) terminals, where $\bar{A}$ and $\bar{B}$ are the complementary of A and B respectively. The MLG is designed with three operating modes: (i) program, (ii) read, and (iii) steady-state. Logic information is written into the MLG during the programming mode, where input signals are applied to the logic gate and the MLG is write-enabled. Logic information is retrieved from the memristors during the reading mode. If at any time power supply to the MLG is interrupted during the output mode, the MLG can retrieve logic information by performing the reading mode without re-programming of the memristors. Steady-state mode is the default mode if the MLG is neither in programming or reading modes, where the output of the MLG is constantly provided to external circuitry by a pair of CMOS inverters.

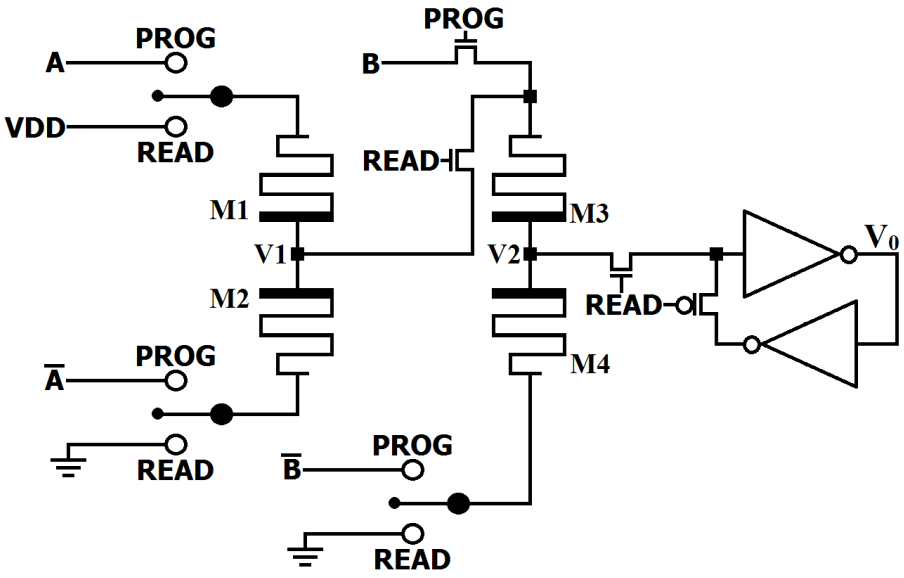

Figure 58. Schematic circuit of the OR-MLG.

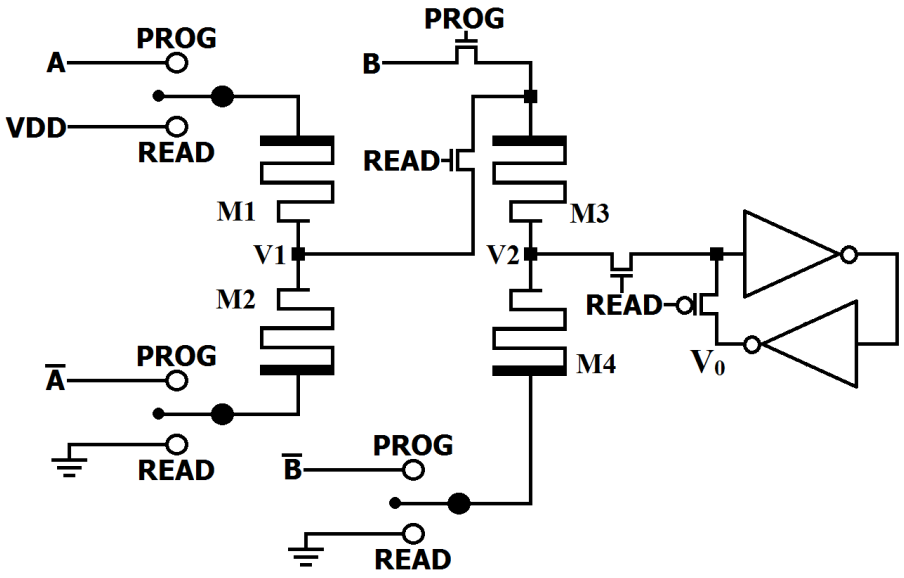

Figure 59. Schematic circuit of the AND-MLG.

5.8.1 Programming mode of MLG

For both types of MLG, programming mode is actuated by charging *PROG* to V_{DD}. This allows current flow between A and $\bar{A}$, as well as between B and $\bar{B}$. The current flow between the complementary inputs functions to alter memristances of two memristor pairs: M1 and M2, programmed by input A; and M3 and M4, programmed by input B. In each memristor pair, the memristors are connected in series in opposite directions, thus each memristor behaves reciprocally against the other memristor in a memristor pair. If M1 is in R_{OFF}, then M2 is in R_{ON}, and vice versa. Similarly, if M3 is in R_{OFF}, then M4 is in R_{ON}, and vice versa. The purpose of reciprocal memristances in a memristor pair is to create a varying potential difference at nodes V_1 and V_2.

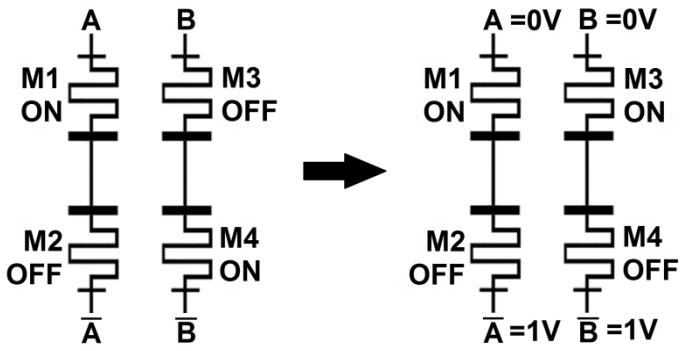

Figure 60. An example of a case of programming OR-MLG.

An example of programming of the OR-MLG is shown in figure 60. Before programming, memristors M1 and M4 are initialized to R_{ON} while M2 and M3 are initialized to R_{OFF}. Inputs A and B are then set to 0V and programming is actuated. Memristors M3 and M4 are switched to R_{ON} and R_{OFF} respectively. Memristors M1 and M2 remain in their current states due to the direction of current from $\bar{A}$ to A which would also program M1 and M2 to R_{ON} and R_{OFF} respectively. The behaviour of the memristors to produce the truth tables of the OR-MLG and AND-MLG is further explained in section 5.8.2, which also explains the reading mode of the MLG.

Table 13. The four typical cases of programming in the MLG.

Initial state of memristors before switching				State of memristor after applying 0V to inputs A and B				Time needed for output change (ns)	Switching delay of memristors (ns)	Ener consum (pJ
M1	M2	M3	M4	M1	M2	M3	M4			
R_{ON}	R_{OFF}	R_{ON}	R_{OFF}	R_{ON}	R_{OFF}	R_{ON}	R_{OFF}	0.00	0.00	0.0
R_{OFF}	R_{ON}	R_{OFF}	R_{ON}	R_{ON}	R_{OFF}	R_{ON}	R_{OFF}	26.42	45.00	17.1
R_{ON}	R_{OFF}	R_{OFF}	R_{ON}	R_{ON}	R_{OFF}	R_{ON}	R_{OFF}	25.93	45.00	17.0
R_{OFF}	R_{ON}	R_{ON}	R_{OFF}	R_{ON}	R_{OFF}	R_{ON}	R_{OFF}	25.93	45.00	17.0

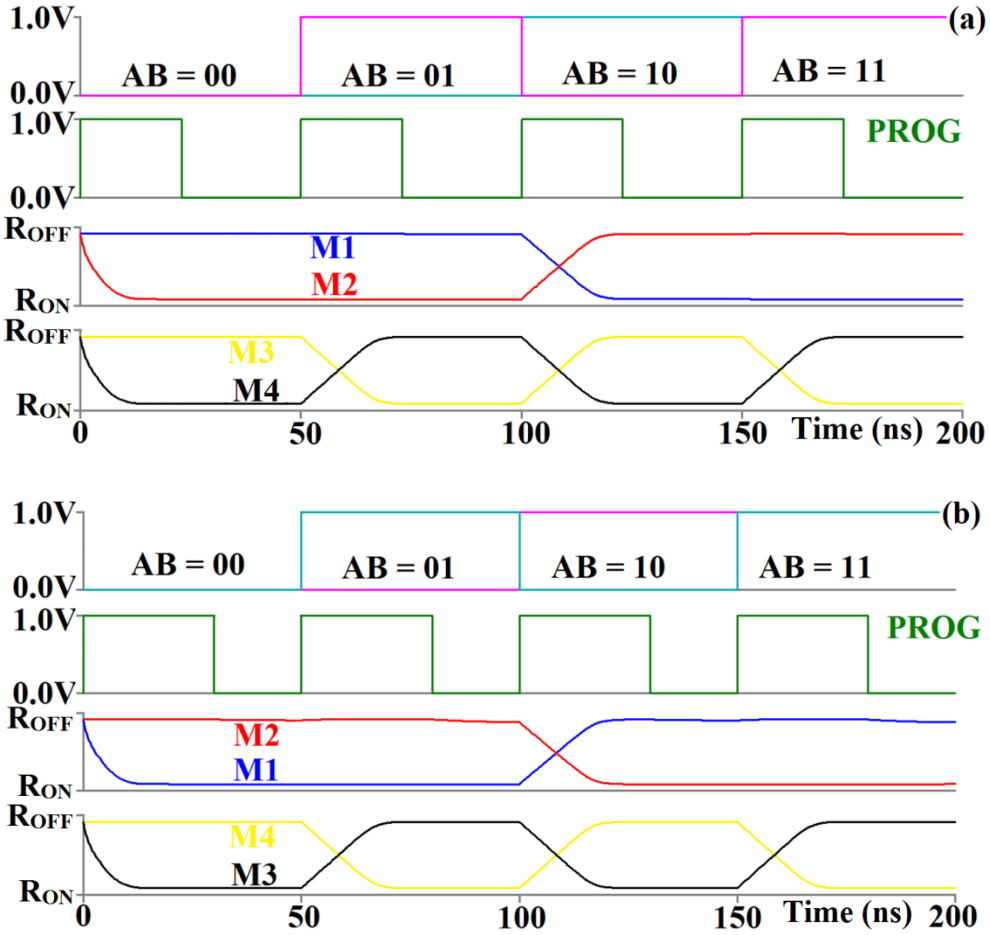

Figure 61. Simulation of the programming of (a) OR-MLG and (b) AND-MLG.

The programming of OR-MLG and AND-MLG is summarised in table 13, where 0V is applied at inputs *A* and *B* when programming the MLGs. The simulation of programming of the MLGs is shown in figures 61(a) and 61(b) respectively. The time needed for output change, switching delay of memristors and energy consumption of the two memristor pairs depend on the initial and final memristance states, regardless of the combination of inputs. Thus in table 13, the cases for other input combinations (A = 0V and B = 1V, A = 1V and B = 0V, and A = 1V and B = 1V) are not added to the table because the results of the other input combinations are similar to the cases that are already shown in table 13.

The average time needed for an output change is 25.93ns if memristance switching is required. Otherwise if memristance switching is not required, the output voltage level remains the same and there is no output delay. To fully switch the memristors to their R_{ON} or R_{OFF} states, an average delay of 45ns is required, while the energy required to switch memristance states is an average of 17.07pJ. Table 13 also shows that if two pairs of memristors require switching, the amount of delay and energy required does not differ much if only one pair of memristor requires switching. This shows that the two memristor pairs are independent of each other. Therefore, it is postulated that if the number of inputs are increased, as well as the number of memristor pairs, the amount of delay and energy consumption would not vary significantly from the results of the two-input MLGs.

5.8.2 Reading mode of MLG

The function of reading mode is to retrieve programmed information from the memristors and translate it to the output node of the MLG. For both OR and AND-MLGs, reading mode is activated by applying a short pulse to *READ*, lasting about 1ns, which is sufficient for the output inverter to sense the voltage at node V_2. This in accordance to the simulation environment conducted in this research. At the same time, the memristors are undisturbed by the short reading pulse [221]. Activating *READ* channels V_{DD} to the four memristors, M1 – M4. During reading mode, the output inverters are separated by the PMOS, which is active low. This is to ensure

that the voltage at V_o does not interfere with the voltage at V_2 during read mode by preventing short-circuit between V_o and V_2.

The voltage at node V_2, which is used to translate to the output of the MLG, can be calculated using circuit theories. To develop the equations for the equivalent read circuit, the memristors are replaced with resistors that represent instantaneous memristances and the circuit becomes that in figure 62. Resistance of transistors are as low as 10Ω when in conduction, which is 10 times smaller than the R_{ON} of the memristors used in the simulation. Thus, it is safely assumed that the removal of transistors from the equivalent circuit to do not affect the circuit equations and simplifies the circuit equations.

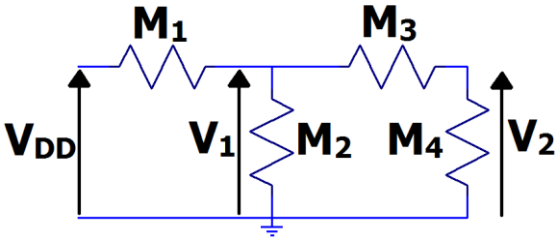

Figure 62. Equivalent circuit of the MLG during reading mode.

The voltage at node V_1 is defined by:

$$V1 = Vdd\left(\frac{M2||(M3+M4)}{M1+M2||(M3+M4)}\right) \quad (17)$$

Hence, V_2 equals to:

$$V2 = V1\left(\frac{M4}{M3+M4}\right) \quad (18)$$

Using equations (17) and (18), the programming and reading of the MLGs are summarised in table 14, where V_o is the output of MLG. For the OR-MLG, when V_2 is close to 0V, the inverter outputs V_{DD} and the potential at V_o is V_{DD}. Conversely, if V_2 is close to V_{DD}, the inverter outputs 0V and the potential at V_o is 0V.

Table 14. Summary of programming of memristors and the output from reading mode for OR-MLG and AND-MLG.

MLG	Inputs		Memristances (Ω)		V_2 (V)	V_o (V)
	A	B	M1 : M2	M3 : M4		
OR	0	0	100 : 16000	100 : 16000	0.981558	0
	0	1	100 : 16000	16000 : 100	0.006135	1
	1	0	16000 : 100	100 : 16000	0.006135	1
	1	1	16000 : 100	16000 : 100	0.000038	1
AND	0	0	16000 : 100	16000 : 100	0.000038	0
	0	1	16000 : 100	100 : 16000	0.006135	0
	1	0	100 : 16000	16000 : 100	0.006135	0
	1	1	100 : 16000	100 : 16000	0.981558	1

As for the AND-MLG, when V_2 is closer to 0V, the double inverter outputs 0V at V_o. Similarly, if V_2 is closer to V_{DD}, the potential at V_o is V_{DD}. For example, when inputs *A* and *B* connected to the AND-MLG are '1' and '0' respectively, the voltage at V_1 is 0.9877 of V_{DD} and thus, the voltage at *V2* is 0.006135V. Since this magnitude of voltage is smaller than $V_{DD}/2$ (0.5V), the first inverter outputs V_{DD} and hence after the second inverter, the output V_o is 0V.

5.8.3 Steady-state mode of MLG

The steady-state mode is the default mode of the MLGs and is actuated when neither *PROG* nor *READ* is triggered. The output of the MLG is V_o and is kept in steady-state by the inverter loop. The inverter loop ensures that the MLG output is retained for as long as power supply to the inverter loop is undisturbed. This means that the output of MLG is independent of the presence of input supply. Once the MLG is programmed, the inputs can be disconnected from their respective input power sources and this provides more design flexibility. This is unlike the Memristive Ratioed Logic (MRL) circuits [128], whereby the output is only available for as long as the MRL inputs are connected to appropriate voltage levels. For example, if the inputs are supposed to be logic '1', the inputs must constantly be connected to V_{DD} to ensure a constant output of V_{DD}.

Moreover, the MLG is dependent on only one voltage source, which is to supply voltage to the inverter loop, regardless of the number of inputs of the MLG. Thus, if the MLG is expanded to increase the number of inputs, the steady-state remains dependent on only one voltage source.

If power supply to the MLG is disturbed during steady-state mode, the output of the MLG can be refreshed by performing the reading mode on the MLG. Re-programming is not necessary because the memristance of the memristors is unchanged throughout reading and steady-state modes. This feature is not available in previous memristive logic gates, where if the input supply is disconnected, then

the only method to retrieve information is by reconnecting input voltages. If input voltages cannot be reconnected, then information is permanently lost.

The MLG solves this issue by ensuring the stored information is saved in the form of memristances which can be retained for up to 10 years [216] and also ensures that the memristors are not affected during the steady-state mode of the MLG.

5.8.4 Expansion of the 2-bit input MLG

The proposed MLGs can be expanded to include more number of inputs by repeating the memristor pairs. The general structure of an OR-MLG being expanded to *n*-number of inputs is shown in figure 63. Although the expanded OR-MLG can be simulated to show correct functional behaviour, a general equation for the potential difference produced at the n^{th} set of memristor could not be derived due to the complexity of the equivalent resistive circuit when expanded to *n*-number of inputs.

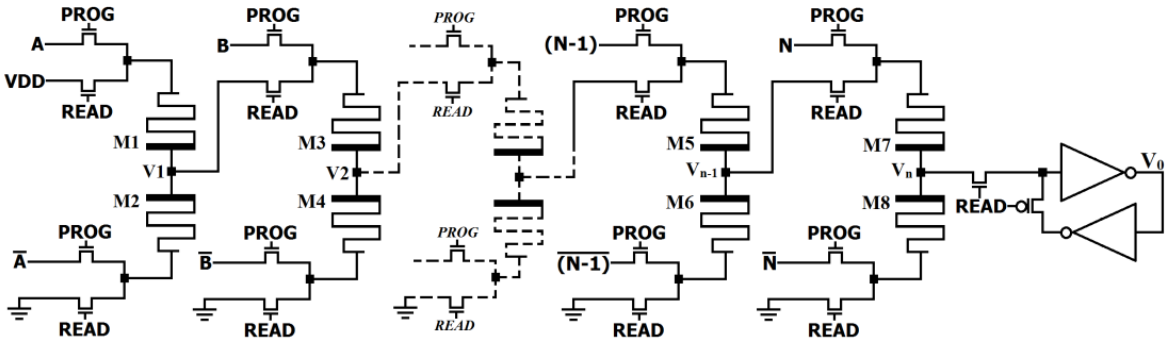

Figure 63. Expanded OR-MLG to *n*-number of inputs.

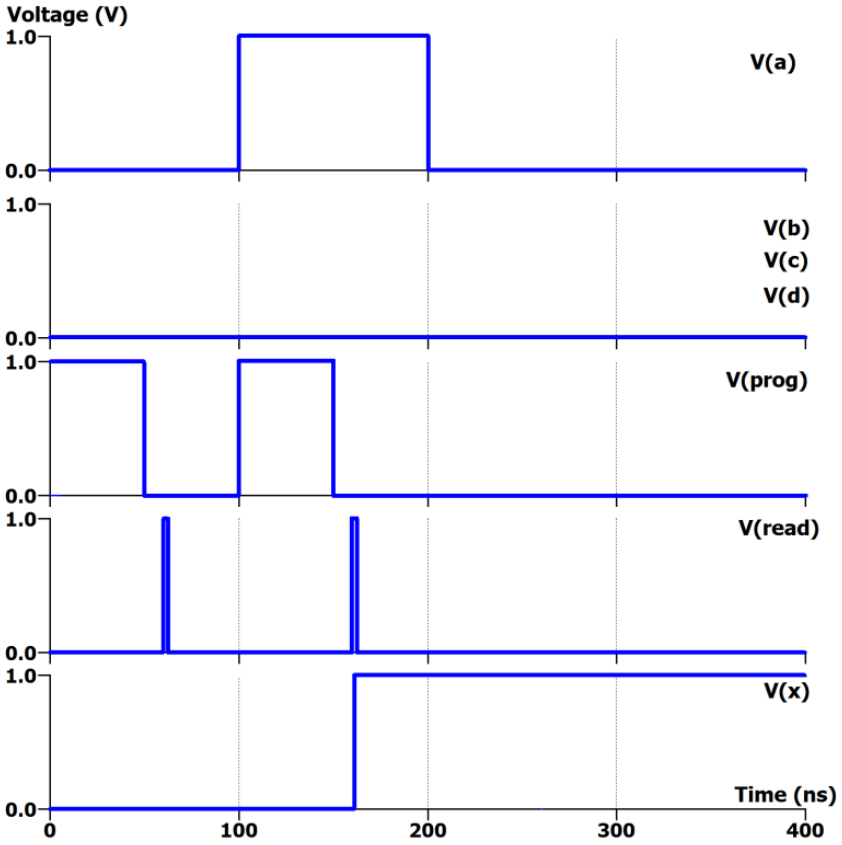

Figure 64. Simulation results of a 4-bit input OR-MLG.

A 4-bit input OR-MLG is simulated and simulation results are shown in figure 64. In the graphs, V(a), V(b), V(c), and V(d) are the input voltages at input pins A, B, C, and D respectively, where V_{DD} is 1V, representing logic '1', and 0V represents

logic ‘0’. V(prog) and V(read) is used to initiate programming and reading modes respectively in the MLGs. The MLGs operate in their steady-state mode when neither V(prog) or V(read) is charged to V_{DD}.

From the simulation results, the n-input OR-MLG shows that the output of MLG is independent of the presence of the input supplies, where the voltage of input A is discharged to 0V, but the output of the OR-MLG remains at 1V (logic ‘1’). This is unlike the MRL and CMOS logic circuits. Therefore, the MLG is dependent on only one voltage source, which is to supply voltage to the inverter loop, regardless of the number of inputs of the MLG. Thus, the energy consumption during steady-state remains dependent on only one voltage source even if the MLG is expanded to increase the number of inputs; hence this reduces the amount of energy consumed by the MLGs, when compared to the MRL and CMOS logic circuits.

5.9 Simulation results of MLG and MRL combinational circuits

The proposed MLG devices are used in a combinational circuit that realizes the Boolean algebra $X = AB + CD$ (19), with its equivalent CMOS circuit previously shown in figure 53. The equivalent MLG schematic for this combinational circuit is shown in figure 65.

$$X = AB + CD \tag{19}$$

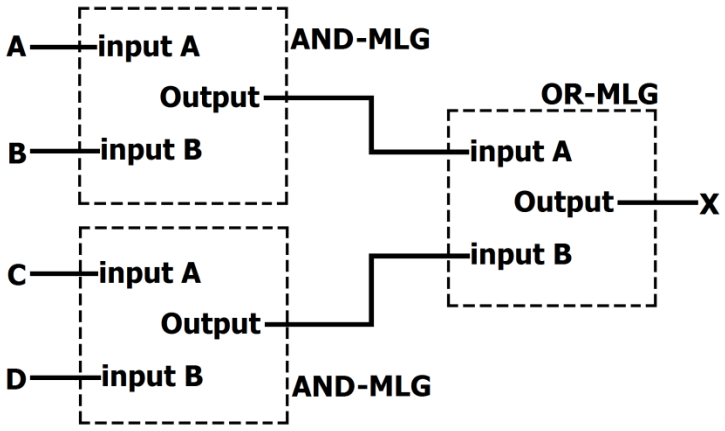

Figure 65. Boolean algebra X = AB + CD realized using MLG.

The double inverters at the output of each MLG ensure that the input supply to the next MLG is at V_{DD} or 0V. Moreover, the output logic is still independent of inputs A – D and the output logic requires only one power source to retain logic information in the CMOS inverters of the OR-MLG. The simulation results are shown in figure 66. In the graphs, V(a), V(b), V(c), and V(d) are the voltages at

input pins A, B, C, and D respectively, and V(x) is the output of the combinational circuit.

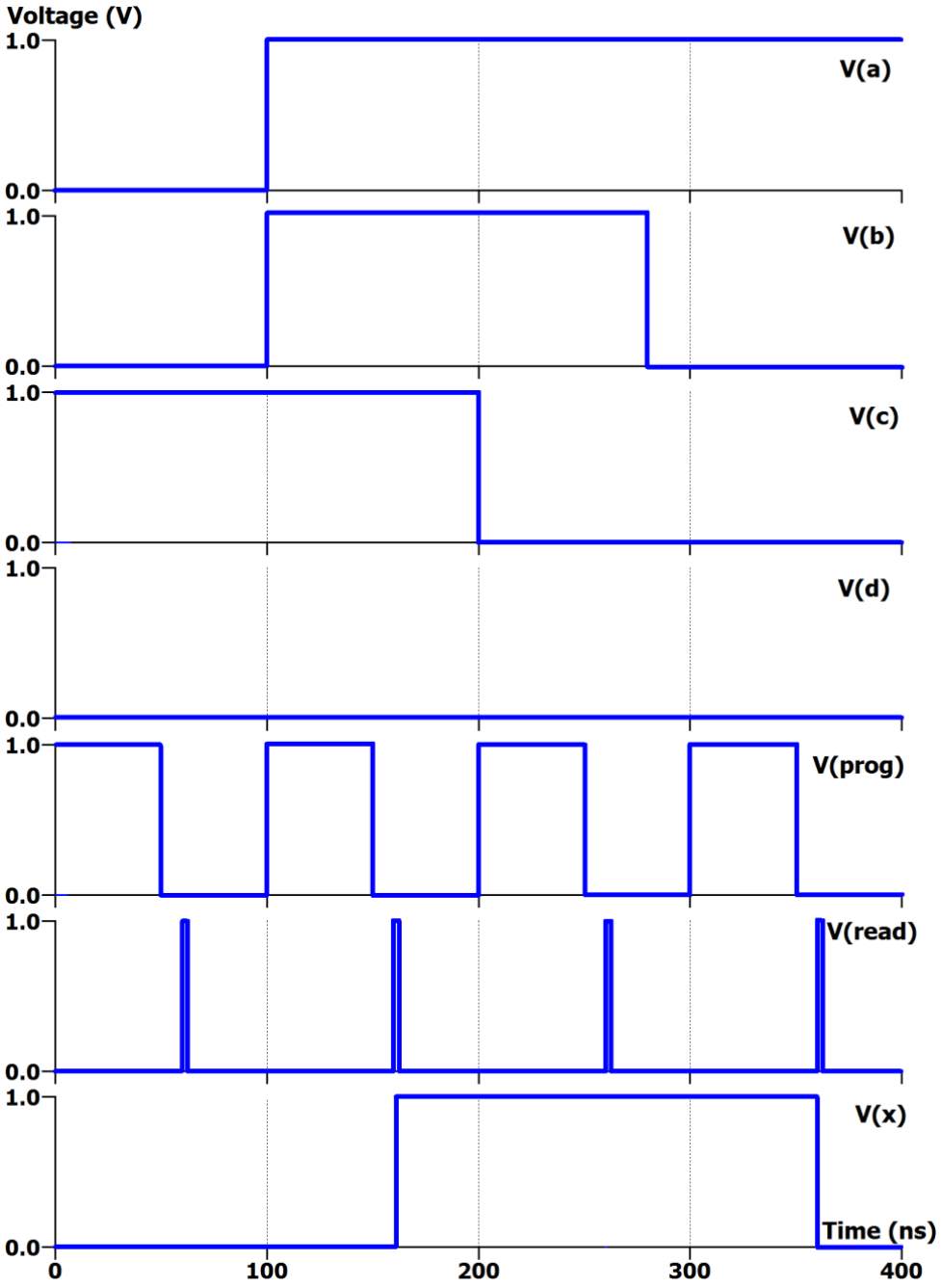

Figure 66. Simulation results of the circuit in figure 64.

5.9.1 Energy consumption of MLG combinational circuit

The average energy consumption to hold an output at steady-state (when memristance switching is not performed) for 45ns in the MRL combinational circuit is 1.496pJ (33.24μW), where all of the combinations of inputs are taken into account, from "0000" to "1111". The amount of energy consumption is based on a period of 45ns, which is the longest amount of time taken to switch memristance states in the MLG combinational circuit. The energy consumption for memristance switching in the MLG combinational circuit is at most 17.07pJ, while the energy consumed during steady-state for 45ns is 1.312pJ (29.16μW). Thus, the rate of energy consumption of the proposed MLG circuit during steady-state is about 1.14 times lesser than the equivalent MRL.

However, the energy consumption for memristance switching (1.892pJ) is about 1.28 times higher compared to the 4-input MRL combinational circuit, which requires 1.474pJ in average per memristance switching cycle. Although the average consumption of MLG circuit is higher per memristance switching, it is noted that the majority of the operation of the MLG and MRL circuits is in its steady-state. Therefore, at a frequency of 5MHz switching, the energy consumption per clock cycle is 6.626pJ and 6.412pJ for MLG and MRL circuits respectively. At 20MHz, the energy consumption per clock cycle is 1.640pJ and 2.038pJ respectively.

The MLG circuit improves energy consumption by isolating the CMOS inverter loop from the memristors that allows the MLG to power its output during

steady-state without depending on input power supply. This drastically reduces energy consumption. Since majority of the MLG operation is during its steady-state mode, the energy consumption is independent to an increase of inputs of the MLG combinational circuit. Furthermore, as shown in the programming mode of the MLG circuit (section 5.8.1), the amount of energy consumption and switching delay is independent on the number of memristor pairs that undergo memristance switching.

In contrary, the energy consumption of MRL combinational circuits is proportional to the number of inputs because the operation of the MRL combinational circuits is powered by the consistent supply of input voltages. Therefore, it is postulated that the MLG combinational circuits is a better option in handling combinational circuits in terms of energy consumption and non-volatility.

5.9.2 Output delay of MLG combinational circuit

The output delay is the measurement of time taken for the MRL and MLG combinational circuits to exhibit proper output voltage levels when addressed. For the MLG circuit, it is measured from the time when *READ* is triggered until the time when V(x) completes the switch between logic levels. For the MRL circuit, output delay is measured from the time when input connected to the MRL circuit is changed until the time when V(x) completes switching between logic levels. Simulation results show that the output delay for V(x) in the MLG to switch between logic levels is an average of 70.26ps, which is about 500 times faster than when simulating

the same Boolean algebra with the unbuffered MRL combinational circuit (average of 34.21ns) [128]. The average output delay of the buffered MRL combinational circuit is 114.82ps, which is faster than the unbuffered MRL but is still 1.63 times slower than the MLG.

During programming, both MRL and MLG combinational circuits require an average of 45ns to complete memristance switching. The output voltage takes some time for it to become stable while memristance switching is taking place. The programming to output delay is measured by the amount of time needed for node V_x or V_2 to reach a steady voltage level above 0.95V for logic '1' or 0.05V for logic '0' during memristance switching. Simulation results show that it takes an average of 31.66ns for output to be stable during programming in the MRL circuits, which is 1.22 times slower than the MLG circuit (25.93ns). Although the MRL combinational circuit has buffers to decrease the delay of stabilising of output, the MLG circuit does not use buffers. Thus, the programming to output delay in the MLG combinational circuit is still faster than that in the MRL combinational circuit.

5.9.3 Comparison against CMOS combinational circuit

The MLG combinational circuit is compared against a CMOS logic gate combinational circuit that realizes the same Boolean algebra. The time needed for output change in the CMOS combinational circuit is 100.127fs, which is about 700 times faster than the proposed MLG combinational circuit. However, the CMOS

combinational circuit consumed an average of 54.664nW of energy for the 400ns simulation as performed by the MLG combinational circuit, which is 25% more energy consumed than the proposed MLG combinational circuit (43.535nW). This is due to the CMOS combinational circuit uses input power to maintain output logic, which similar to the MRL circuits. Therefore, the CMOS combinational circuit also consumes more energy than the MLG combinational circuit.

In summary, a non-volatile one-bit memory cell (2TG1M) has been published which shows better overall performance against other similar one-bit memristive memory cells and against the CMOS memory cell. Using the 2TG1M memory cell, an NVLUT was proposed, which reduces device area by at least 128 transistors against the CMOS 6-bit input LUT. This chapter also discusses the proposal of an improved MRL combinational circuit using buffers, as well as two proposed MLG combinational circuits.

6. SWITCH BLOCK

SWITCH BLOCK

6.1 Switch block and switch matrix

A switch block is a network of interconnections between routing channels that links one resource block (logic block, switch block, control block, I/O block, etc.) to another in an FPGA architecture. Switch blocks contain a number of switch matrices, where the number of switch matrices in a switch block depends on the number of routing channels that passes through the switch block. Each switch matrix interconnects routing channels to at least three other routing channels (figure 67). The interconnections between two routing channels are completed via pass-transistors, which are controlled by SRAM cells in the SRAM-based FPGA architecture.

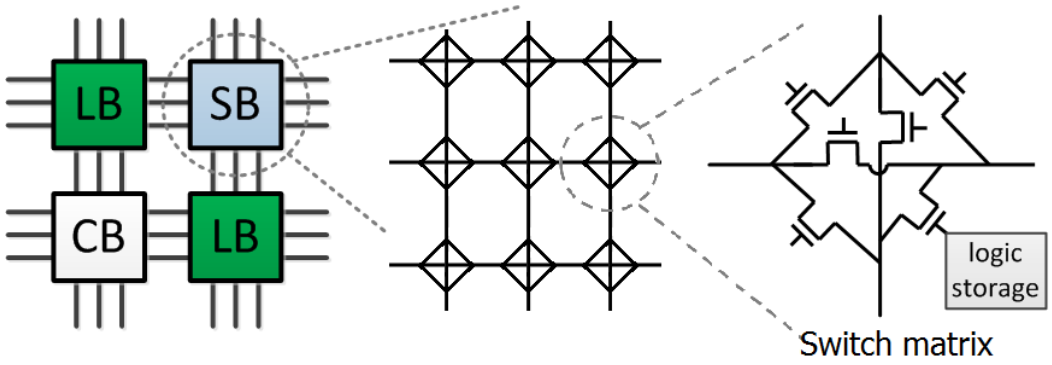

Figure 67. General structure of a switch matrix in a switch block.

6.2 7T1M SRAM cell

A 7 transistor 1 memristor (7T1M) SRAM cell was published that provides an overall reduction of switching delay, reduced energy consumption, and smaller device area against other similar memristive SRAM cells in the literature [222]. The schematic of the published 7T1M SRAM cell is shown in figure 68 and the netlist is attached in appendix H.

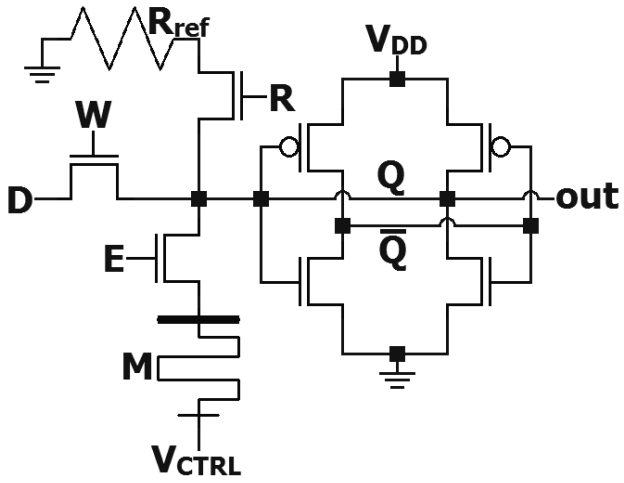

Figure 68. Schematic circuit of the 7T1M SRAM cell.

Different from the CMOS 6T SRAM cell, the 7T1M SRAM cell uses an additional one transistor and one memristor in the design, but more importantly it exhibits non-volatility features. In the 7T1M SRAM cell, the V_{CTRL} is set to V_{DD} and $V_{DD}/2$ when performing read and write operations respectively, while W and R are

used to select the write and read operations respectively. During write processes, E is activated in order to ensure the flow of current through the memristor during both writing logic '1' and '0' operations.

6.2.1 Write operation of 7T1M SRAM cell

When programming the 7T1M SRAM cell, V_{CTRL} is set to 0.5V to ensure that current can flow through the memristor in either direction and W is charged to V_{DD} to create a low-impedance channel in the NMOS pass-transistors that connects Q to the voltage from input signal D. At the same time, R is connected to ground that turns the transistor into high-impedance and disconnects the cell from resistor R_{ref}. To disable write operation, W is connected to ground to disconnect the cell from the input signal D.

To write logic '1' D is charged to V_{DD} and current flows from positive terminal of the memristor to the negative terminal due to potential at the positive terminal of the memristor (1.0V) is higher than at the negative terminal (0.5V), thus switching the memristor to LRS. On the other hand, to write logic '0', D is grounded (0V) and the memristance is switched to HRS due to current flowing from the negative terminal of the memristor to the positive terminal, where the potential at the negative terminal of the memristor (0.5V) is higher than at the positive terminal (0V). Also, during write operation Q is connected to the voltage from input signal D. Thus, Q is

charged to V_{DD} when the cell is programmed to logic ‘1’ or grounded (0V) when the cell is programmed to logic ‘0’.

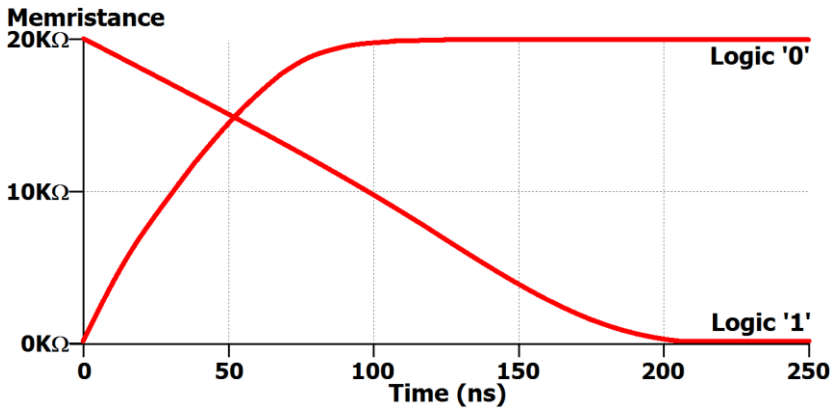

Figure 69. Simulation of the write process of the 7T1M SRAM cell.

Simulation of the proposed 7T1M SRAM cell shows that the writing delay is 208.35ns for logic ‘1’ and 144.07ns for logic ‘0’ (figure 69) , giving an average delay of 176.21ns. The difference in the writing delay between logic ‘1’ and ‘0’ is due to the asymmetric resistive switching behavior of memristors, where switching from HRS to LRS requires a longer time due to the higher electric field required to breakdown the bulk layer and form a conducting channel [177]. When switching to logic ‘0’ (from LRS to HRS), the memristance increases with time. Thus, it is observed that the rate of change of memristance with time (gradient of memristance-time graph) decreases as the memristor approaches HRS, where current flow in the memristor decreases, which slows the change of memristance. Conversely, when switching to logic ‘1’ (from HRS to LRS), the memristance change is constant with time due to the large resistance presented by the initial HRS of the memristor.

Consequently, the energy consumption for writing logic '1' is higher (0.958pJ) than for writing logic '0' (0.363pJ), giving an average energy requirement of 0.683pJ per writing cycle. The energy consumption for writing logic '1' is higher due to switching the memristor from its HRS to its LRS which requires a larger electric field and takes a longer time, thus energy consumption to switch to logic '1' is higher.

6.2.2 Read operation of 7T1M SRAM cell

For the read operation of the proposed 7T1M SRAM cell, R and E are charged to V_{DD} to create a low-impedance channel in the NMOS pass-transistors to connect the memristor and R_{ref} to the cell. At the same time, W is connected to ground that turns the transistor into high-impedance and disconnects the cell from the input signal D. Thus, the voltage across the R_{ref} provides the logic stored in the cell, which is dependent on the resistance of the memristor. It should also be noted that during the read operation, the state of the memristor is unaltered.

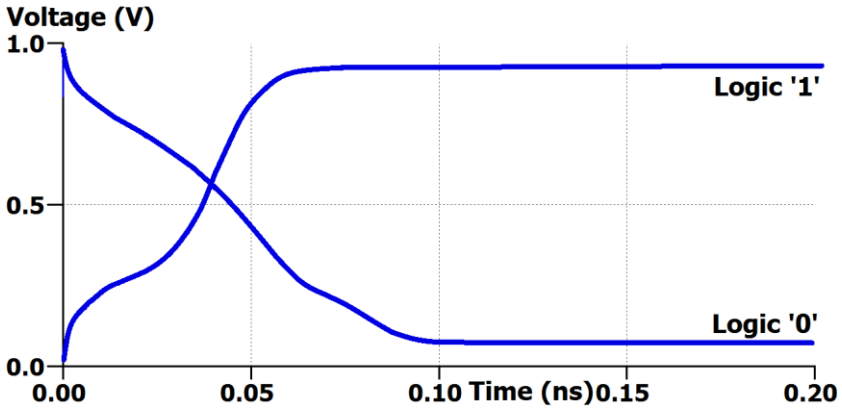

Figure 70. Simulation of the read process of the 7T1M SRAM cell.

The simulation results of the read operation are shown in figure 70, where the proposed cell requires 104ps to read logic '1' and 146ps to read logic '0'. The reading of logic '0' is slower than reading logic '1' due to the lesser amount of current flowing through the high memristance when reading logic '0'. The amount of current when reading logic '0' and '1' is 10.49μA (HRS) and 13.48μA (LRS) respectively. Thus, the delay in reading logic '0' is higher due to lesser current flow into node Q.

6.2.3 Non-volatile feature of 7T1M SRAM cell

In the proposed 7T1M SRAM cell, similar to the CMOS 6T SRAM cell, inverters connected back-to-back forming a loop is used for retaining the logic information of the cell as long as V_{DD} is available. However, should there be an interruption of V_{DD}, unlike in the CMOS 6T SRAM cell, the proposed 7T1M SRAM cell retrieves the logic information using the memristor and restores logic

information into the inverter loop. This is achieved by performing a read operation with W being turned off while transistors E and R are turned on. A short pulse of 1ns of V_{DD} is applied at V_{CTRL} during the read operation. Figure 71(a) shows the equivalent resistive circuit when read process is performed on the 7T1M SRAM cell. Figure 71(b) shows the switching of Q and $\bar{Q}$ between logic levels.

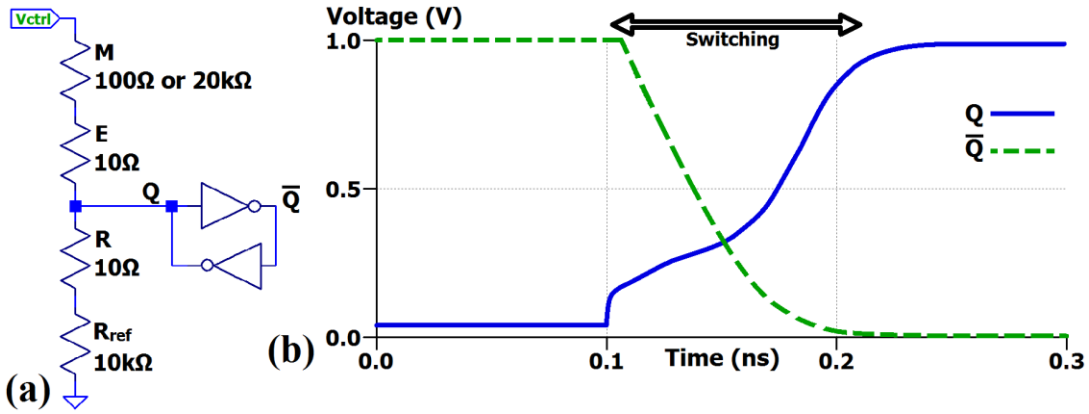

Figure 71. Equivalent circuit of the 7T1M SRAM cell during reading and (b) the simulation of the inverter loop between Q and $\bar{Q}$.

The non-volatility characteristic of the 7T1M SRAM cell is initiated by turning off the power supply V_{DD} for at least 0.5s to ensure parasitic capacitances of the transistors are fully discharged. Since the CMOS inverters have been discharged due to interruption in V_{DD}, they offer high impedance. Thus, when the CMOS inverters are in parallel, their effect on the equivalent resistance is negligible. R connects the cell to a fixed reference resistor R_{ref} forming a series connections with transistors E and R, and resistor R_{ref}. The resistance of transistors E and R is 10Ω. This creates a potential divider between R_{ref} and the memristor. V_{CTRL} is then charged to V_{DD} for 1ns to bring Q and $\bar{Q}$ to their appropriate voltage levels.

Considering that the stored logic level is low (‘0’) before the power interruption, then the memristor is in its HRS (20kΩ) state. This causes the initial voltage at Q to be about 1/3 of V_{CTRL}. Hence, $\bar{Q}$ is charged to V_{DD} by the CMOS inverter and subsequently Q is discharged to 0V.

On the other hand, if the stored logic level is high (‘1’) before the power interruption, then the memristor is in its LRS (100Ω) state. Thus causing the initial voltage at Q is about 0.98 of V_{CTRL} due to resistance of memristor and transistor E (total of 110 Ω) smaller than the resistance of R_{ref} and transistor R (10.01kΩ). $\bar{Q}$ is discharged to 0V and subsequently Q is charged to V_{DD}, similar to that shown in figure 70(b). The simulation of the non-volatility of the proposed 7T1M SRAM cell is summarized in figure 72.

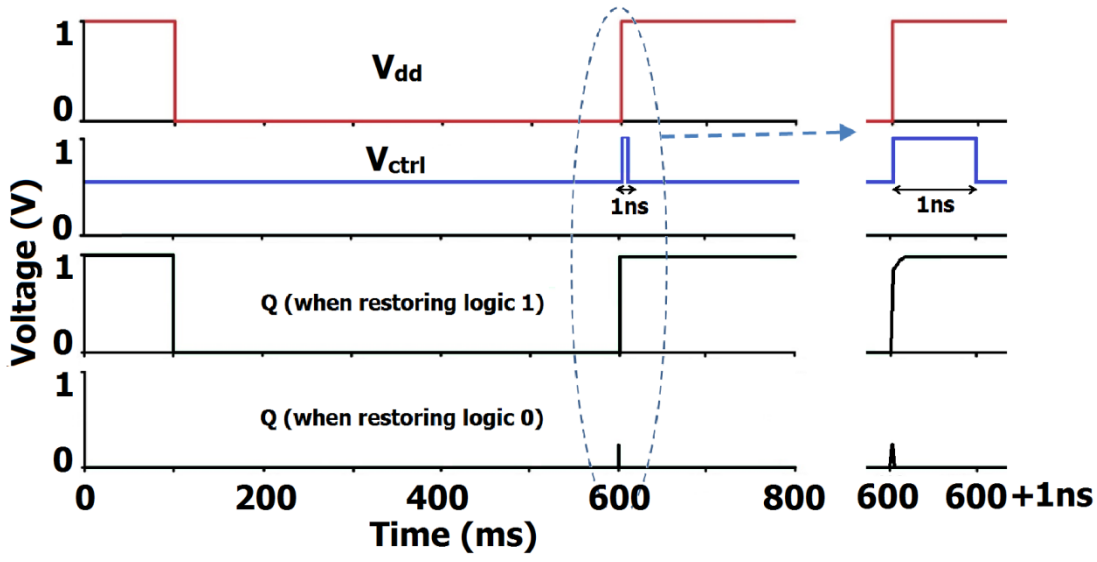

Figure 72. Demonstration of the non-volatile properties of the proposed memristive SRAM cell.

6.3 Comparison of memristive SRAM cells

Simulation is performed on the memristive SRAM cells from literature [136]–[139] and the 7T1M SRAM cell. In order to provide a fair comparison, all the memristive SRAM cells are simulated using similar device parameters. Table 15 summarizes the performance of the memristive SRAM cells. Switching delay is the average of the delay of writing logic '0' and '1', defined by the amount of time taken to completely switch memristance states. Power consumption is the rate of energy consumption by a memristive SRAM cell throughout switching process and retention of logic. The amount of device area used by the memristive SRAM cells is measured in terms of λ^2, where λ is equivalent to the length of the minimum feature size (transistor gate length). For this research work, λ is 32nm.

Energy-Delay-Area-Product (EDAP) is used to determine the optimum memristive SRAM cell. The EDAP value is the product of switching delay, power consumption and device area used by a memristive SRAM cell. Using the EDAP allows a single quantity for comparison because none of the memristive SRAM cells are superior in every performance aspect. For example, the 7T1M SRAM cell has the least power consumption, but uses more device area than the 4T2M cell [136]. Therefore, a smaller EDAP value represents a better overall performance of the memristive SRAM cell among the three performance aspects.

Table 15. Summary of the memristive SRAM cells and their EDAP value.

Memristive SRAM cell	Switching delay (ns)	Power consumption (µW)	Area (λ^2)	EDAP (10^4 ns-µW-λ^2)
Proposed 7T1M	176.21	2.9665	308	1.61
4T2M [136]	156.56	32.645	176	9.00
7T2R [137]	132.91	28.648	352	13.40
NVPG [138]	135.32	3.5126	396	1.88
rSRAM [139]	186.66	5.3514	440	4.40

The 4T2M cell [136] uses only four transistors and two memristors, which is the least number of components among the memristive SRAM cells in the literature. However, the two memristors are connected to the cell power supply, V_{DD}, thus whenever the cell is in use, current constantly flows from V_{DD} through both memristors. This increases the amount of energy dissipated across the two memristors, and increases the value of EDAP of the 4T2M cell. The usage of the 7T2R cell [137] also causes current to constantly flow through two memristors. Moreover, the memristors are reciprocal to each other, meaning when one is in LRS, the other is in HRS. This causes the current to consistently flow through a high resistive memristor in the memristive SRAM cell, which increases energy consumption and increases the value of EDAP of the 7T2R cell.

The NVPG cell [138] has lower energy consumption due to two pass-transistors that are used to control the access of two memristors. This ensures that during the normal usage of the cell, the pass-transistors are switched off and becomes high-impedance. Thus, current do not pass through the memristors.

However, by using two pass-transistors and two memristors, as compared to the 7T1M SRAM cell, the amount of device area used is increased which increases the EDAP value of the NVPG cell.

The switching speed of a memristor is proportional to the amount of current flowing through a memristor. The large number of transistors used in the rSRAM cell [139] increases overall cell resistance, which reduces current flow in the rSRAM cell. The lesser amount of current in the rSRAM cell decreases switching speed and increases switching time delay in the rSRAM cell. Therefore, the large device area and long switching delay increases the EDAP value of the rSRAM value.

The 7T1M SRAM cell uses the least number of memristors per cell, which decreases device area. Also, the amount of voltage applied across the memristor in the 7T1M SRAM cell is less than V_{DD}, which is equivalent to $V_{DD}/2$. This is due to the usage of V_{CTRL}, set to $V_{DD}/2$ during programming. These two factors contribute to lesser amounts of current passing through large resistances of memristors in the 7T1M SRAM cell, which improves energy consumption. However, this contributes to the longer switching delay in the 7T1M SRAM cell than in the 4T2M, 7T2R, and NVPG SRAM cells, whereby the amount of current supplied to the memristors of the 7T1M SRAM cell is relatively lesser.

Combining the performance criteria of switching delay, power consumption, and device area, the 7T1M SRAM cell has an overall EDAP value of 1.61, which is the lowest among the memristive SRAM cells.

6.4 Application of 7T1M SRAM cell in a switch matrix

The CMOS SRAM-based switch matrix is improved by replacing CMOS 6T SRAM cells with 7T1M SRAM cells (figure 73). The output *Q* of the 7T1M SRAM cell is connected to the gate terminal of pass-transistors in the switch matrix to create a memristive-based non-volatile switch matrix. This circuit is simulated with a routing channel RC_{IN} transmitting signals to another routing channel RC_{OUT}.

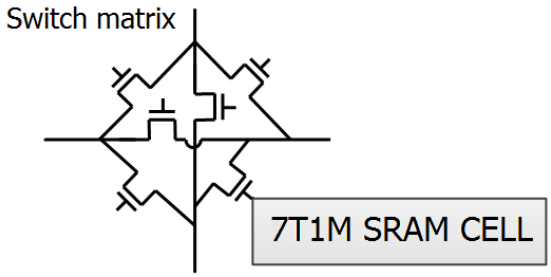

Figure 73. Output *Q* of 7T1M SRAM cell connected to a pass-transistor in a switch matrix.

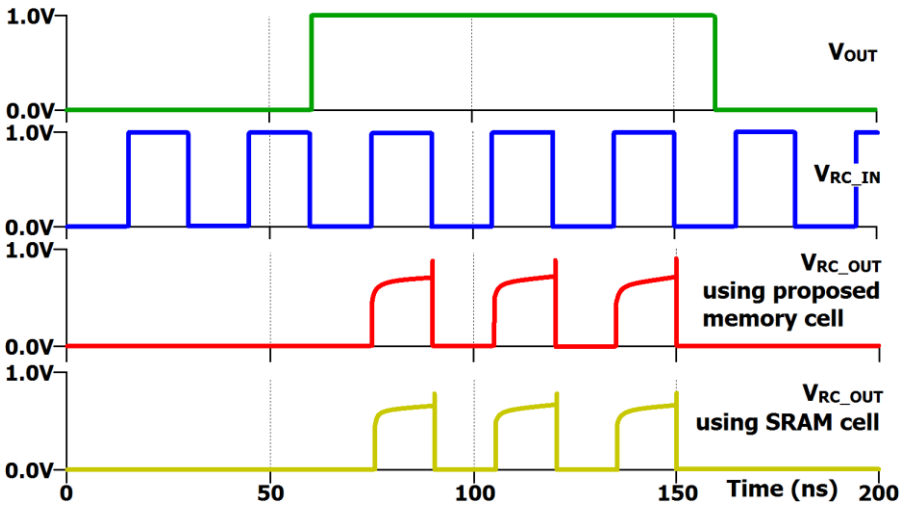

Figure 74. Switch matrix pass-transistor controlled by the memristive switch matrix of 7T1M SRAM cells and CMOS SRAM-based switch matrix.

The simulation of the control of the switch matrix is shown in figure 74 where RC_{IN} is the input to the routing channel and RC_{OUT} is the output of the routing channel. This simulation is conducted with 7T1M SRAM cells and CMOS 6T SRAM cells in the switch matrix. V_{OUT} is the output from the cell that controls the gate-terminal of the switch matrix pass-transistor. V_{OUT} of 0V turns off the pass-transistor and RC_{OUT} is disconnected from RC_{IN} (as shown from 0ns to 60ns, and from 160ns to 200ns in figure 74). Likewise, if V_{OUT} is 1V, RC_{IN} is transmitted to RC_{OUT} (as shown from 60ns to 160ns in figure 74).

Since the simulation results of RC_{OUT} of both types of switch matrices are similar to each other in terms of the amount of delay taken by RC_{OUT} to reach appropriate voltage levels, as well as the stable voltage level reached by RC_{OUT}, it is concluded that the memristive-based switch matrix is able to replace the CMOS SRAM-based switch matrix in terms of electrical performance.

7. MEMRISTIVE-BASED FPGA ARCHITECTURE

MEMRISTIVE-BASED FPGA ARCHITECTURE

7.1 Memristive Logic Cell (MLC) and Configurable Memristive Logic Block (CMLB)

A memristive logic cell (MLC) is designed with the schematic block diagram in figure 75. The MLC comprises of an NVLUT, two CMOS-based multiplexers, and an MDFF. The NVLUT may also act as an array of memory cells. Multiplexer *f* performs the selection switch between NVLUTs, while multiplexer *control* selects or de-selects the MDFF. MDFF is used if the MLC is programmed to function as a sequential logic circuit, asynchronous or synchronous. Conversely, the MDFF is not used if the MLC is programmed to function as a combinational logic circuit or if it does not require clock cycles.

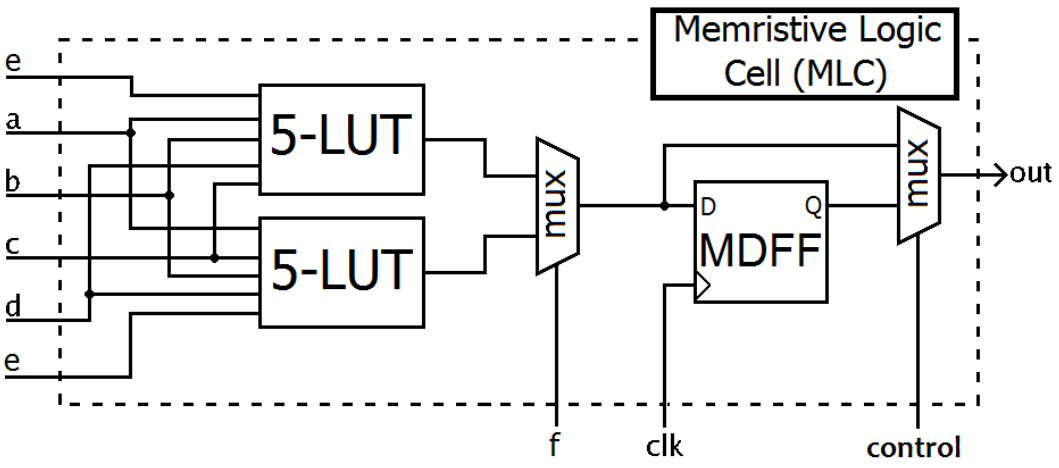

Figure 75. Memristive logic cell (MLC).

To construct the MLC, CMOS-based LUT is replaced with the 6-bit NVLUT and the D flip-flop is replaced with a memristive D flip-flop. The NVLUT can also be programmed to function between 2 to 6 input LUTs. Current FPGA logic cells are used to function as two 5-input LUTs, three 4-input LUTs, four 3-input LUTs, or five 2-input LUTs. Similarly, the 6-input NVLUT can also be used to function as two 5-input NVLUTs by assigning *INPUT6* of the NVLUT as the control bit to select one of the two 5-input NVLUTs. *f* in figure 75 is connected to a multiplexer which selects the output from one of the two 5-input NVLUTs. This separates the 64 memory cells into two sections of 32 memory cells, separated by logic '0' and '1' of *INPUT6*. The remaining 5 address lines (*a* – *e* in figure 75) are used as the 5-bit inputs to address one section of the 32 memory cells. Using this similar method, the 6-input NVLUT can also be further used as three 4-input NVLUTs, four 3-input NVLUTs, or five 2-input NVLUTs.

Several MLCs are then interconnected using switch matrices to form a configurable memristive logic block (CMLB), as shown in figure 76. The switch matrices function to route the output of an MLC to the input of another MLC, or vice versa. The switch matrices can also connect outputs of several MLCs to form a larger output. In the proposed CMLB, four switch matrices are used as the routing switches.

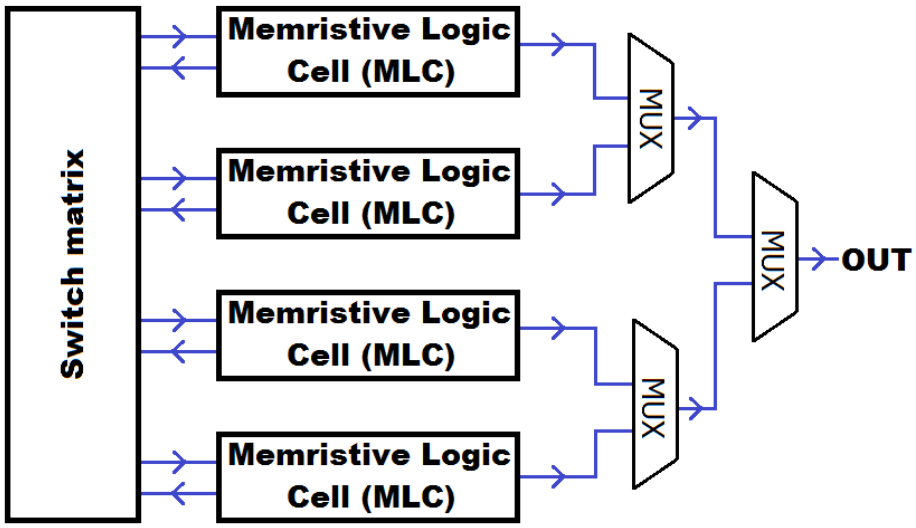

Figure 76. Block diagram of configurable memristive logic block (CMLB).

7.2 Evaluation of MLC and CMLB

The CMLB is evaluated by comparing: (i) the amount of device area used, (ii) average power consumed, and (iii) critical path delay. Due to various FPGAs being manufactured by various companies, the device area and power consumption of different test designs in different FPGA family would be different. Thus, the comparison performed in this article is based on only one type of FPGA family, Virtex-5. The test designs used in the simulations to validate and evaluate the CMLB are obtained from [223].

To measure the three performance criteria, the amount of resources used by each test design are obtained by synthesizing the test designs using an Electronic Design Automation (EDA) software for FPGAs. The test designs are synthesized

using Xilinx ISE 10.1 to obtain the breakdown of the resources utilized by each test design. Each of the logic blocks are then replaced with CMLBs and the device area and power consumed by the test design in the memristor-based environment is evaluated, where the amount of device area and power consumed by the test design is the summative consumption of each of the CMLB used in each test design. The critical path delay is obtained by measuring the accumulative delay in the critical path of each test design. To ensure that a fair comparison between the CMLB and the SRAM-based logic block (SLB), the design and structure of the SLB follows that of the CMLB but uses SRAM cells and CMOS circuits instead of memristive cells and circuits.

7.2.1 Resource utilization of test designs

The amount of resources used by each test design depends on the minimization of logic computation performed by an FPGA EDA software. Xilinx ISE was chosen due to the denser packing of logic resources compared to other similar logic synthesizing software, which minimizes the amount of resources required by each test design [224].

In the MLC, the 6-bit NVLUT reduces a total of 128 transistors from the CMOS 6-bit LUT, but the use of MDFF requires additional 6 transistors compared to the CMOS D flip-flop. Overall, the MLC experiences a reduction of 122 transistors. The amount of device area per 6-bit input NVLUT is 196.608μm^2 while the SRAM-

based LUT uses 262.144μm^2. This is an improvement of 65.536 μm^2 in device area per each 6-bit input LUT. Therefore after subtracting the additional device area for the MDFF, the total device area reduction by the MLC is 60.416μm^2.

Each switch matrix consists of six pass-transistors, and each pass-transistor is controlled by an individual SRAM cell, which amounts to 6 SRAM cells. Hence, each SRAM cell is replaced with a 7T1M SRAM cell. The 7T1M SRAM cell uses one transistor more than the SRAM cell. This results in an addition of six transistors for six 7T1M SRAM cells per switch matrix, which amounts to an addition of 3.072μm^2 of device area. In each CMLB, four switch matrices are used, which results in an addition of 12.288μm^2 of device area per CMLB.

In overall, the CMLB has four MLCs and four switch matrices. Four MLCs reduces device area by 241.664μm^2 but the four switch matrices increases 12.288μm^2 of device area. Therefore, the total reduction of device area by one CMLB is 229.376μm^2. The estimated total device area of one CMLB is 950.272μm^2 while one SLB is 1179.648μm^2.

Table 16. Comparison of FPGA architecture performance based on one set of CMLB and one switch matrix.

Logic Block	Device area (μm^2)	Power (nW)
SRAM-based	1179.648	116.647
Memristor-based	950.272	74.343

Based on four sets of 6-bit input LUT logic cell and four switch matrices, overall utilization of FPGA device area is reduced when using the CMLB (table 16). Although memristive flip-flops and switch blocks use more device area than their respective SRAM-based blocks, this is compensated by the large reduction of device area by the NVLUT. Since the utilization of these logic blocks is based on the amount of resources required by a design, a more accurate comparison of device area is evaluated by the number of logic blocks used by each test design.

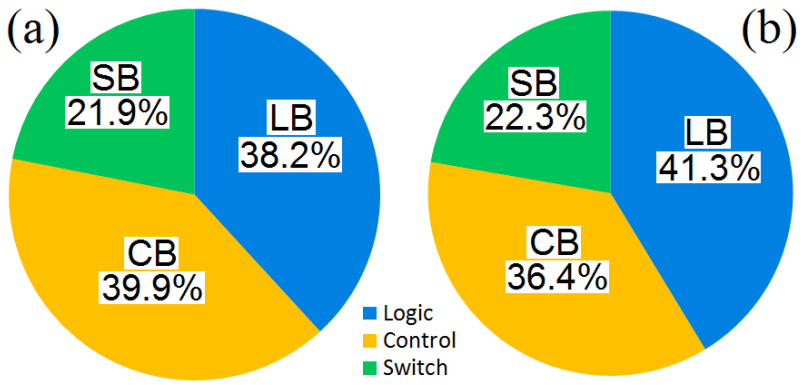

Figure 77. Resource utilization by device area of the test designs in (a) memristive-based and (b) SRAM-based FPGA architectures.

Figure 77 shows the average proportion of the type of FPGA blocks utilized by the test designs in SRAM and memristor-based FPGA architectures. Due to the designs usually utilizes a large number of logic blocks compared to other types of FPGA blocks, this result in an overall device area reduction when using memristor-based architecture compared to the SRAM-based architecture. The device area utilized by the test designs in both types of FPGA architecture is summarized in table 16.

7.2.2 Power consumption of test designs

The power consumption measurement of the CMLB is performed by running all the functions (programming and reading) of the CMLB in all of the modes (synchronous and asynchronous). The power consumption of the CMLB is measured by summing the amount of energy consumed by each component in the CMLB over a pre-determined number of clock cycles, and then dividing it by the amount of time equivalent to the clock periods.

Since the proposed CMLB is for use in a memristive-based FPGA architecture, it is beneficial to take advantage of the non-volatile characteristics of the memristive circuits and memory cells. Thus, the clock feeding the MDFFs of the MLCs are turned off until a read process of the MDFF is activated. The average power consumption of the CMLB is 74.343nW, compared to the SLB that has an average power consumption of 116.647nW (table 16).

7.2.3 Critical path delay in logic cell

Due to the different type of resources used in the SRAM-based and memristor-based FPGA architectures, the distance of critical path changes. However for this research, the structure and design of both the CMLB and SLB are the same, thus the critical path of the test designs is assumed to pass through the same type and same

amount of resources in both types of FPGA architecture. Figure 78 shows the typical critical path in a logic cell, both CMLB and SLB. The critical path delay through a logic cell in the CMLB is 5.81ns, while in the SLB is 5.86ns. This is measured by the amount of time taken for the output to reach a stable voltage level after a change in inputs to the logic cell is applied.

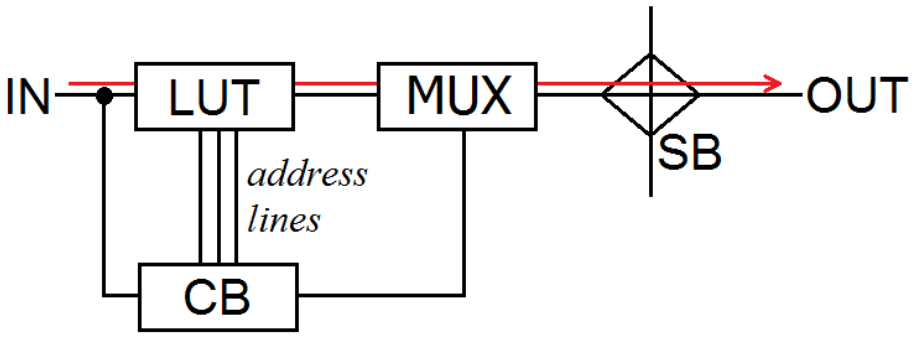

Figure 78. Typical critical path through a logic cell.

7.3 Comparison against other memristive-based FPGA architectures in the literature

Table 17 shows the comparison of memristive FPGA architectures in the literature benchmarked against the SRAM-based FPGA architecture. Value of more than 1 denotes improvement while value of less than 1 denotes deterioration against the SRAM-based FPGA architecture.

Table 17. Comparison of memristive FPGA architectures in the literature against SRAM-based FPGA architecture (number of times improved against the SRAM-based FPGA architecture).

FPGA architecture	Process technology	Device area	Path delay	Power
CMLB (this research)	32nm	1.09	1.09	0.93
GMS [114]	45nm	1.07	1.58	1.69
mrFPGA [115]	45nm	5.18	2.28	1.63
RRAM-based FPGA [116]	22nm	0.74	0.83	1.50
Hybrid CMOS-Memristor [117]	22nm	1.40	N/A	N/A
CMOS-RRAM Integration [118]	32nm	6.00	1.10	1.23
3D-stacking [119]	32/45nm	1.63	1.34	N/A

The evaluation of the CMLB using test designs is summarized in tables 18 and 19. The evaluation shows that the CMLB improves device area requirements by an average of 8.6%, while power consumption is increased by 7.1%. The power consumption evaluation does not take into account the retention of logic information

in the CMLB by removing power supply. This experiment was not performed because the removal of power supply and retention of logic information in the CMLB can last at least 10 years [187]. Thus, power reduction is dependent on the length of time of logic retention and this does provide a fair comparison against the SRAM-based FPGA architecture. Henceforth, it is postulated that the power consumption of this proposed CMLB will be lesser than the SRAM-based FPGA architecture if the non-volatile feature of the memristors are considered. Critical path delay is reduced by 1.094 times due to the smaller device area used by the CMLB which also decreases routing channel lengths.

Table 18. Comparison of device area used by each design in terms of µm^2.

Test design	SRAM-based 32nm device area	Memristor-based 32nm device area	Device area improvement	
			Percentage (%)	Ratio (SRAM/memristive)
s298	6661.364	6237.696	6.4	1.0679
s349	5735.082	5555.536	3.1	1.0323
s382	10942.954	10324.480	5.7	1.0599
s400	10942.954	10324.480	5.7	1.0599
s444	15401.990	14455.808	6.1	1.0655
s510	17434.518	15940.848	8.6	1.0937
s641	35755.976	32721.536	8.5	1.0927
s713	33862.832	31026.416	8.4	1.0914
s820	44219.460	40514.560	8.4	1.0914
s1196	53068.894	48908.240	7.8	1.0851
s1423	66107.720	61438.384	7.1	1.0760
s1488	63889.104	58779.776	8.0	1.0869
s5378	144289.476	133240.144	7.7	1.0829
s9234	128309.782	118193.280	7.9	1.0856
s15850	888418.344	800669.312	9.9	1.1096
s35932	3112490.634	2813016.704	9.6	1.1065
S38584	3122078.676	2810518.448	10.0	1.1109
Average			**8.6%**	**1.09 times**

Table 19. Comparison of power consumption and critical path delay of each design.

Test design	Power consumption (μW)		Improvement (%)	Critical delay (ns)		Improvement (times)
	SRAM-based	Memristor		SRAM-based	Memristor	
s298	2.206	2.567	-16.4	2.830	2.462	1.149
s349	2.714	3.113	-14.7	3.577	3.114	1.149
s382	3.708	4.339	-17.0	3.324	2.815	1.181
s400	3.708	4.339	-17.0	3.324	2.815	1.181
s444	4.833	5.578	-15.4	3.324	2.815	1.181
s510	4.469	4.846	-8.4	3.916	3.283	1.193
s641	13.862	13.846	0.1	7.244	7.166	1.011
s713	13.415	13.393	0.2	7.498	7.257	1.033
s820	11.331	12.253	-8.1	5.542	5.357	1.035
s1196	13.442	14.991	-11.5	10.107	9.521	1.062
s1423	19.169	22.016	-14.8	7.503	7.291	1.029
s1488	15.375	17.031	-10.8	5.551	5.701	0.974
s5378	52.001	54.787	-5.4	8.874	7.708	1.151
s9234	42.396	45.085	-6.3	5.233	4.498	1.164
s15850	428.930	393.473	8.3	10.583	9.894	1.070
s35932	1683.024	1549.361	7.9	4.603	4.736	0.972
S38584	1450.245	1328.524	8.4	7.731	7.248	1.067
Average			**-7.1%**			**1.094 times**

The CMLB is made up of four switch matrices and four MLCs, which consists of a novel NVLUT and a memristive D flip-flop (MDFF) that was designed to replace CMOS D flip-flops. The usage of the 7T1M SRAM cell converts switch matrices to non-volatile memristive switch blocks. The memristive switch block and memristive sequential circuit uses larger device area than their CMOS counterparts by 1.17 times and 1.63 times respectively, but logic cells are used in abundance in the SRAM-based FPGAs and have a reduction of device area by 1.23 times when MLCs are used instead of CMOS-based logic cells. Although the logic blocks are used with different proportions in different designs, the test designs show that the CMLB uses an overall average of 8.6% lesser device area than the SRAM-based

FPGA. Due to the reduction in device area which shortens routing channels, as well as the reduction in transition delay when using memristive blocks, the overall critical path delay was reduced by 1.094 times.

In summary, the SRAM-based logic blocks (SLB) in SRAM-based FPGA architectures are proposed to be replaced with the presented CMLB. A memristor-based FPGA architecture is designed by replacing CMOS-based components such as flip-flops, switch matrix and LUTs with memristive D flip-flop, non-volatile LUT, and memristive switch block that are used in the CMLB. The CMLB presented in this article is proposed to only replace Configurable Logic Blocks in the CMOS-based FPGA architectures. However, it is also noticed that these memristive components and circuits can also be used to build other types of FPGA blocks (such as control blocks). Thus, it is postulated that these memristive components and circuits are also suitable to be used to design a memristor-based FPGA architecture in a future research work.

7.4 Memristive and PCM cells crossbar

Another advantage of memristors is the ability of fabrication of memristive crossbar topology, where memristors are fabricated in the programmable interconnects between metal layers. SRAM-based FPGA architectures frequently use nanocrossbar architectures to reduce device area and increase density.

The crossbar architecture used in this research work is a 2x2 array of four memory cells arranged as shown in figure 79. The four memory cells M0 – M3 can be addressed using a 2-bit input that also represents the address of the memory cells. The 2-bit inputs used to address one of the four memory cells is decoded by using a 2-to-4 demultiplexer.

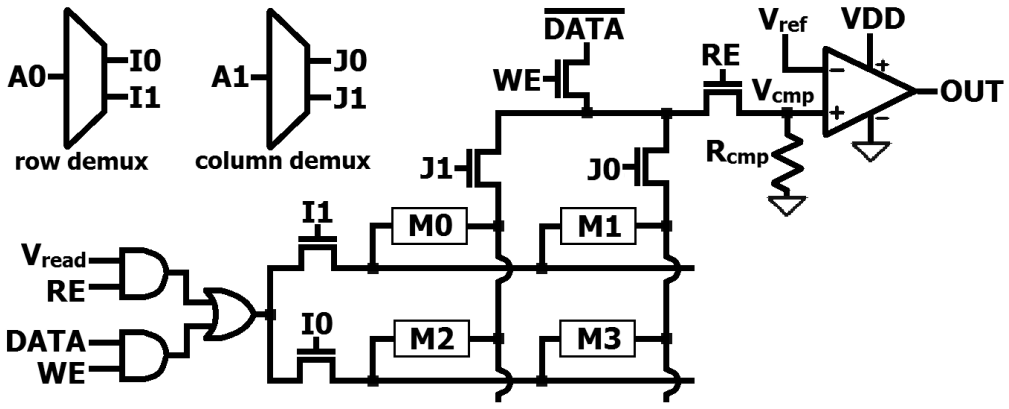

Figure 79. Schematic diagram of the crossbar architecture used in this research.

The write and read operations of the crossbar are activated by triggering WE (write enable) and RE (read enable) respectively. $DATA$ and $\overline{DATA}$ (complementary of $DATA$) are used for programming the memory cells with appropriate logic information. At the row section, a decoder is used to gate the input for write and read processes. WE connects $DATA$ to the memory cells if write is performed, and RE connects V_{READ} to the memory cells if read is performed.

Since each of the memory cells is controlled by one row and one column pass-transistors, both the respective pass-transistors must be enabled to access the respective memory cells in the crossbar. The least number of selector inputs for the decoder is $\log_2 N$ for N number of rows or columns. Since there are 2 rows and 2 columns for a 2x2 array, this gives $\log_2 2 = 1$. Therefore, one input is required for each of the row (A_0) and column (A_1) decoders. The row and column pass-transistors that are to be enabled are selected using two 1-to-2 decoders, one for row and one for column.

This crossbar architecture, as well as the write and read circuitry, are used for both types of memory cells; memristor and PCM. The memory cells M0 – M3 of the general 2x2 crossbar array are then substituted with memristors and PCM cells as shown in figures 80(a) and 80(b) respectively.

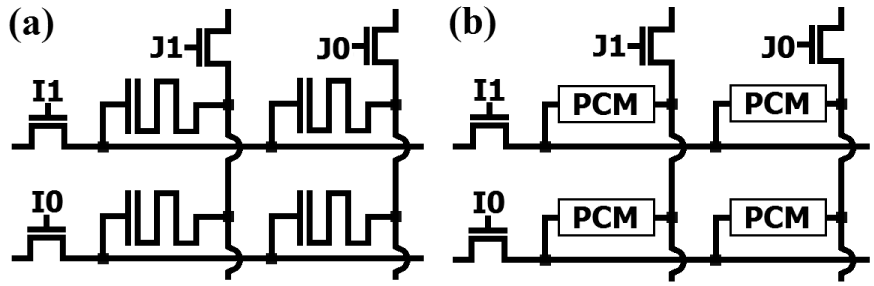

Figure 80. Crossbar memory cells replaced with (a) memristors and (b) PCM cells.

7.4.1 Write operation of crossbar

To write a memory cell, write enable (WE) allows current flow between $DATA$ and $\overline{DATA}$ through the selected memory cell. $DATA$ is connected to the row section of the array and $\overline{DATA}$ is connected to the column section of the array. The direction of current through the selected memory cell depends on the potential difference between $DATA$ and $\overline{DATA}$. Due to the difference of the magnitude of voltage required to program memristors and PCM, there is a slight modification to the write circuitry to compensate for this difference as shown in figure 81.

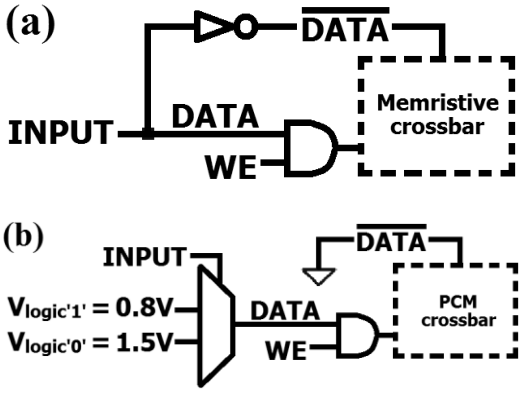

Figure 81. Write circuit of (a) memristor crossbar and (b) PCM cells crossbar.

The difference between programming logic ‘0’ and ‘1’ into memristors is the direction of current through the memristor. The magnitude of voltage for programming logic ‘0’ and ‘1’ is the same, which is 1V for the simulation in this research work. Thus, $DATA$ and $\overline{DATA}$ is designed to complement each other in the memristive crossbar write circuit to ensure a programming magnitude of 1V is always applied to the memristors. If $INPUT$ is 1V, then $DATA$ is 1V and $\overline{DATA}$ is 0V, and the selected memristor is programmed with logic ‘1’ due to current flowing into the positive terminal of the memristors in the crossbar. Conversely, if $INPUT$ is 0V, then $DATA$ is 0V and $\overline{DATA}$ is 1V, and the selected memristor is programmed with logic ‘0’ due to current flowing in the opposite direction, out of the positive terminal of the memristor.

In the PCM crossbar, the programming voltage and time for logic ‘1’ and ‘0’ is different. Thus, $\overline{DATA}$ is permanently grounded (0V) and $DATA$ is connected to a selector in the write circuit of the PCM crossbar. The selector decides the appropriate programming voltage to be applied to $DATA$ depending on the required input logic. 0.8V is applied to $DATA$ for 200ns if logic ‘1’ is to be written into the PCM, while 1.5V is applied for 10ns to $DATA$ if logic ‘0’ is to be written. The difference in voltage and input time is due to the different switching mechanisms between the amorphous and crystalline states of the PCM cells [45].

7.4.2 Read operation of crossbar

The read circuitry for memristive and PCM cells crossbar is the same, where a comparator amplifier is used. RE is charged to V_{DD} to enable current flow from V_{READ}, through the memory cell and into the read circuitry. V_{READ} is set to 0.5V in this research work. V_{REF} is channelled into the inverting input of the amplifier as reference voltage.

For memristive crossbar, V_{REF} is connected to a 0.25V supply and R_{CMP} is 200Ω, which is the mid-resistance between the high memristance (20kΩ) and low memristance (100Ω) states of the memristor. For PCM cells crossbar, V_{REF} is connected to a 0.2V supply and R_{CMP} is 50kΩ, which is the mid-resistance between high (200kΩ) and low (30kΩ) resistances of the average physical PCM devices. For both types of crossbar, the value of R_{CMP} is not taken as the mid-point between the values of HRS and LRS, due to the consideration of the presence of untargeted memory cells which provides a path of parallel resistance. Figure 82 shows the difference in the read circuitry parameters for the memristor (figure 82(a)) and PCM cells crossbars (figure 82(b)).

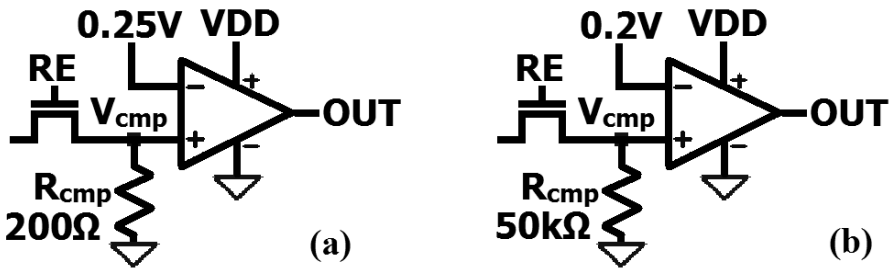

Figure 82. Read circuitry for (a) memristive crossbar and (b) PCM cells crossbar

The read operation for both types of crossbar is similar, by using a comparator amplifier that compares the potential differences at V_{CMP} and V_{REF} with respect to ground. The memristor and PCM memory cells are in series with R_{CMP}, dividing the potential between V_{READ} and ground at V_{CMP}. The equivalent resistive circuit during read operation is shown in figure 83. Resistance of transistors is 10Ω when turned on, which is 10 times and 3000 times smaller than the R_{ON} of memristors and PCM cells respectively. Thus, it can be reasonably omitted from the equivalent resistive circuit. The non-inverting input of the amplifier receives the potential difference across R_{CMP} (equivalent to V_{CMP}), while the inverting input of the amplifier is connected to V_{REF} that act as the reference voltage.

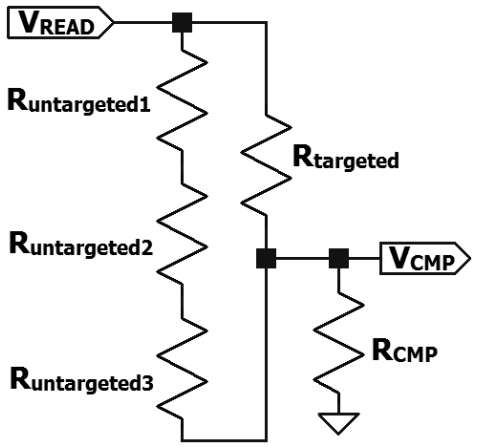

Figure 83. Equivalent circuit when reading the crossbar, where $R_{targeted}$ and $R_{untargeted}$ represent the resistance of the memory cells which are targeted and untargeted respectively.

While reading, leakage current passes through three untargeted memory cells to reach the same destination as the targeted current (figure 8 in chapter 2.13). Hence, there are also three untargeted resistances in the equivalent read circuit in figure 83. Table 20 summarizes the cases of reading the targeted memory cell for

different cases of untargeted memory cells (only worst case scenarios of the untargeted memory cells are listed in table 20).

Table 20. Voltage formed at node V_{CMP} for different cases of reading memristive and PCM cells crossbar.

Memristive crossbar			**PCM cells crossbar**		
Targeted memory cell	**Untargeted memory cells**	**V_{CMP}**	**Targeted memory cell**	**Untargeted memory cells**	**V_{CMP}**
Logic '0' R_{OFF} (20kΩ)	All R_{ON}	0.40V	Logic '0' R_{OFF} (200kΩ)	All R_{ON}	0.45V
	All R_{OFF}	0.01V		All R_{OFF}	0.25V
Logic '1' R_{ON} (100Ω)	All R_{ON}	0.73V	Logic '1' R_{ON} (30kΩ)	All R_{ON}	0.69V
	All R_{OFF}	0.67V		All R_{OFF}	0.64V

From the results, it was shown that the resistance of the memory cell is lower than R_{CMP} if the memory cell contains logic '1'. This is due to the specifically chosen values of R_{CMP} for the read operations. A larger portion of V_{READ} (more than 0.5 of V_{READ}) is dropped across R_{CMP}. Thus, the magnitude of V_{CMP} is larger than V_{REF} and OUT obtains the positive input voltage of the amplifier, which is V_{DD} (logic '1'). Conversely, a memory cell with logic '0', where the resistance of the memory cell is higher than R_{CMP}, results in V_{CMP} lower than V_{REF}. Thus, OUT obtains the negative input voltage of the amplifier, which is connected to ground, 0V (logic '0').

7.4.3 Simulation results of memristive and PCM cells crossbar

To evaluate the performance metrics of both PCM and memristive crossbars, programming and reading (both logic '0' and '1') are performed separately on each of the four memory cells. Two types of worst case scenarios were adopted for each experiment. The methods of initialisation to create the worst case scenarios are:

(i) All other memory cells are initiated to a different logic than the programmed logic.

(ii) All other memory cells are initiated to the same logic as the programmed logic.

For the first type of worst case scenario, all other memory cells are initialised to logic '0' if the targeted memory cell is tested with logic '1'. Similarly, all other memory cells are initialised to logic '1' if the targeted memory cell is tested with logic '0'. For the second type of worst case scenario, all other memory cells are initialised to logic '1' if the targeted memory cell is tested with logic '1'. Likewise, all other memory cells are initialised to logic '0' if the targeted memory cell is tested with logic '0'.

Simulation is performed on the crossbar array by writing to a targeted memory cell in the array, and then reading from the same memory cell, with both types of worst case scenarios used for programming and reading. This experiment is then repeated on the other memory cells. Simulation results are compiled and used to analyse programming and reading delay, programming and reading energy, and

leakage energy. The values of each performance criteria are measured from writing and reading each of the four memory cells. For each performance criteria, the results are averaged to estimate the general behaviour of a memory cell in the crossbar.

Figure 84 shows the programming delay of memristive and PCM cells crossbar, while figure 85 shows the reading delay of the crossbars. Energy leakage dissipated by the crossbar is obtained by measuring the power consumption of all the unselected cells in the crossbar and is summarized in figure 86.

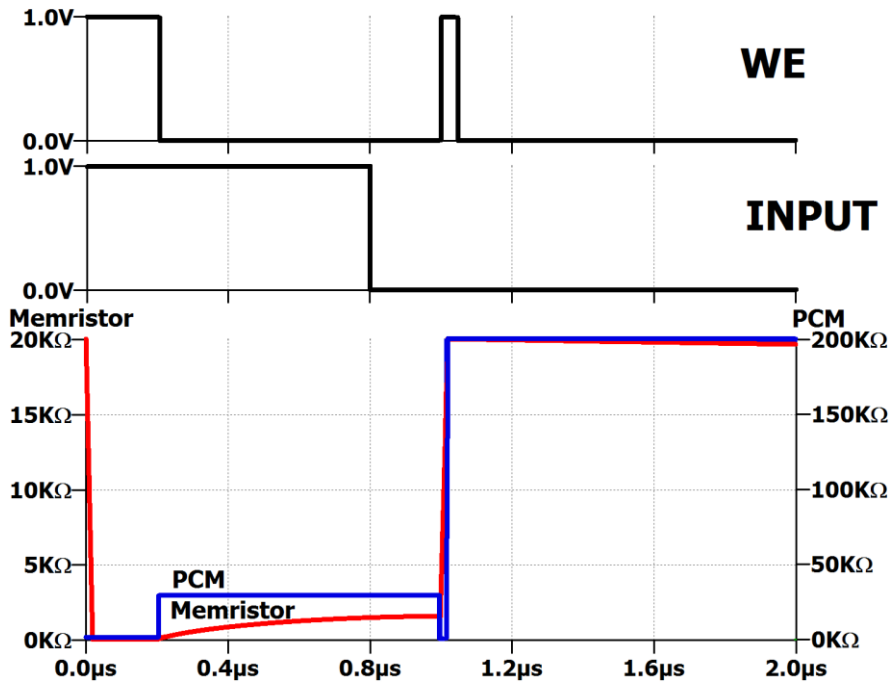

Figure 84. Average programming delay of memristive and PCM cells crossbar

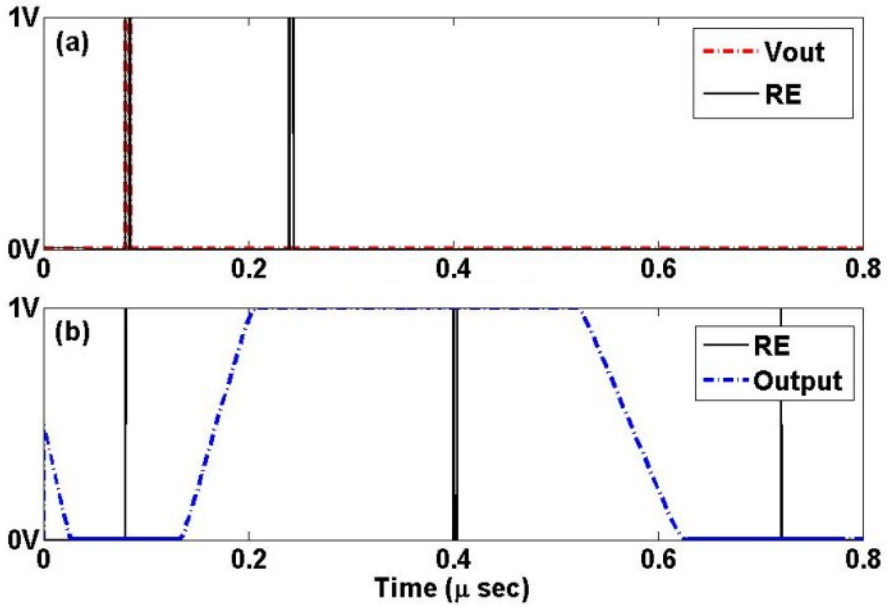

Figure 85. Average read delay of memristive and PCM cells crossbar

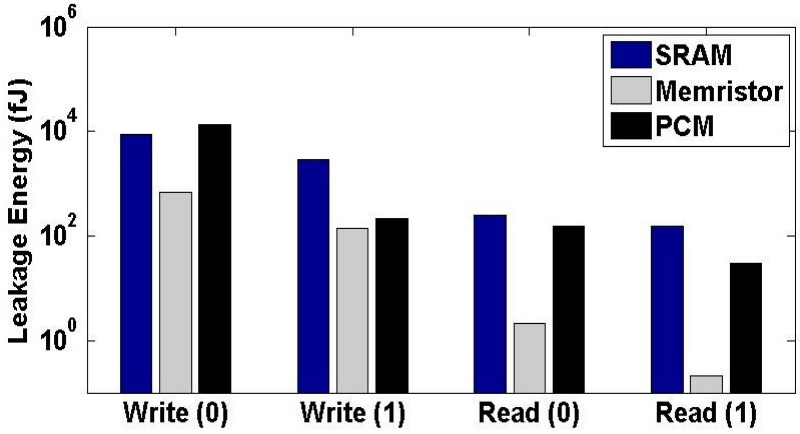

Figure 86. Leakage Energy in SRAM, Memristive, and PCM crossbars

7.4.4 Delay of memristive and PCM cells crossbar

From the simulation results, it was found that the programming delay for both memristive and PCM cells crossbars is worse than the SRAM crossbar by 2 and 3 orders of magnitude respectively. The longer write delay in both memristive and PCM crossbars are contributed by the programming processes that require charge displacement and physical change of material in memristors and PCM cells.

Due to these programming processes which are more complicated than switching the SRAM cell, current needs to be channelled through memristors and voltage needs to be applied across PCM cells for a certain amount of time. As a result, the writing delay in both memristive and PCM crossbars are prolonged. Contrarily, SRAM cells are switched by application of a voltage at the gate terminals of NMOS and PMOS transistors to either create or collapse an inversion layer between the collector and emitter terminals. The inversion layer is a very thin layer and hence, switching of SRAM cells takes shorter time than memristors and PCM cells [225].

Read delay is the amount of time taken for the output to become stable at its appropriate voltage level after a targeted memory cell has been addressed for reading. The read delay of the memristive crossbar is about 3 orders of magnitude faster than the reading process of SRAM crossbar while PCM crossbar is about 1.5 orders of magnitude faster than the SRAM crossbar. The reason for the longer read delay of SRAM cells is the SRAM cells have high parasitic capacitance due to the

larger amount of transistors used to build an SRAM cell, compared to NVM cells. Thus, it takes a longer time to charge or discharge output load in the SRAM crossbar.

Between memristive and PCM crossbar, the read delay for memristors is shorter due to the lower resistance of memristors when compared to the PCM cells. Thus, the amount of current flow into the read circuitry would be higher for the same amount of V_{READ} applied to the crossbar. V_{READ} is maintained the same magnitude for memristor and PCM crossbars so that the amount of leakage current and energy for the crossbars are produced by the same amount of power supply. This is to ensure a uniform comparison between memristor and PCM crossbars.

7.4.5 Energy consumption of memristive and PCM cells crossbar

Programming energy is the amount of energy consumed by the crossbar to complete the switching of a targeted memory cell. The programming energy of memristive and PCM crossbars were found to be 3 and 5 orders of magnitude higher than the programming energy of SRAM crossbars, while reading energy is 2 and 3 orders of magnitude higher respectively. The reason for the high programming energy is due to the switching mechanisms of memristors and PCM cells, which requires the application of voltage and current for a longer duration than to switch an SRAM cell. Thus, this increases the amount of energy supplied to the crossbar and increases programming energy.

Leakage energy is the amount of energy that is wasted by untargeted memory cells while accessing the targeted memory cell. From simulation results, both PCM and memristive crossbars showed more than 3 orders of magnitude of improvement compared to the SRAM crossbar. The reason being the overall resistance levels of memristors and PCM cells are lower than that of SRAM cells. The high impedance of SRAM cells causes larger amounts of voltage dropped across the SRAM cells, which increases energy dissipated across the SRAM cells. Between PCM cells and memristors, PCM cells have the higher resistance range, thus, the energy consumption for reading and writing for PCM crossbar is the larger than that for memristive crossbar. Moreover, the longer programming and reading delays of PCM cells also contribute to higher energy consumption in the PCM crossbar.

7.4.6 Summary of the comparison of memristive and PCM cells crossbar

Table 21. Summary of simulation results performed on crossbar arrays of memristor, PCM, and SRAM.

Average	Memristor	PCM	SRAM
Programming Delay (ns)	27.06	200	0.101
Read Delay (ns)	0.346821	636.826	391.926
Programming Energy (pJ)	1.752	126.73	0.00227
Read Energy (fJ)	23.1125	1369	0.7099
R_{ON} (Ω)	100	30 k	<10
R_{OFF}(Ω)	20 k	200 k	>10 M
Size	f^2	$4f^2$	$6f^2$

The summary of the simulation results are shown in table 21. Programming delay is the amount of time taken by the memory cells in the crossbar to complete switching from one logic state to another.

Although both memristor and PCM crossbars show high programming and leakage energy as compared to the SRAM crossbar, researchers are still widely using NVM crossbars for non-volatile applications and have placed them as emerging technologies. This is due to the advantage of the non-volatile ability to retrieve information, whereas the SRAM crossbar requires re-programming to retrieve information. Thus, it is postulated that the long-term benefits of using NVM-based crossbars would overcome the short-term disadvantages of NVM-based crossbars (high energy consumption and long switching delays) against the SRAM-based crossbar. Due to the high number of applications using crossbars, the long-term usage of NVM-based crossbars has been placed for future research.

Between memristive and PCM crossbars, the memristive crossbar showed superior performance compared to PCM in many aspects, except that PCM cells offer higher resistance range. Thus, it is summarized that PCM cells crossbar provides a better option for multilevel switching crossbar due to its higher resistance range, while memristive crossbar is more suited for bi-level switching crossbar due to its lower leakage current and energy. Alternatively, the non-volatile crossbar with two-input LUT memristor-based memory block can be used [220], which eliminates leakage current.

8. CONCLUSION

CONCLUSION

8.1 Conclusion

In this dissertation, a probable memristive-based FPGA architecture was proposed by replacing logic, control, and switch blocks with CMLB, and memristive control and switch blocks. To complete this project, a comprehensive literature review was conducted on the different types of FPGA and the mechanisms of various resistive switching devices available in the literature. Due to limited resources, all the experiments conducted for this research work are purely simulation. It was realized that simulation experiments could not cover all of the electrical and physical characteristics and behaviour of resistive switching devices, such as retention and endurance, as well as electrode material selection.

For simulation-based experiments, a SPICE memristor model is required. Although a SPICE memristor model was published, it was based on the physical characteristics published in the literature at the time of publishing. It is understood that there could be new developments on the behaviour of memristors which will require updated SPICE memristor models in the future.

Using the published SPICE memristor model, the following memristive circuits and memory cells have been published:

(i) 2TG1M memory cell and 7T1M SRAM cell (non-volatile memories)

(ii) NVDL and MDFF (memristive sequential logic circuits)

(iii) NVLUT and MLG (memristive combinational logic circuits)

The 2TG1M memory cell was shown to have the fastest switching speeds among other published non-volatile memristive memory cells. This is due to the usage of transmission gates which allows near-lossless transfer of voltage from its input to output pins. The device area of the 2TG1M memory cell is smaller than all other memory cells in comparison, except for 1T1M memory cell, which is smaller than the 2TG1M memory cell. This is compensated by the 2TG1M memory cell being able to be written with a unipolar voltage source, instead of a bipolar input voltage.

The 7T1M SRAM cell was shown to have the lowest power consumption among memristive SRAM cells at 2.9665μW. The 7T1M SRAM cell also operates with an average switching speed of 176.21ns. The drawback of the 7T1M SRAM cell is that it uses less current to switch the memristor, which increases switching delay. The Energy-Delay-Area Product (EDAP) value of 1.61 is the lowest among similar memristive SRAM cells in the literature. Therefore, the proposed 7T1M SRAM cell has the best overall electric performance and device characteristics among other similar memristive SRAM cells in the literature.

The NVLUT designed using 2TG1M memory cells operates with the fastest switching speed (at most 8 times faster) among LUTs using other published memristive memory cells. The NVLUT also reduces device area by 128 transistors per each 6-bit input LUT. Another type of combinational logic circuit was also proposed, in the form of MLGs. Two MLGs were proposed, AND-MLG and OR-MLG. In this research work also, an improved version of the MRL was presented with simulation results to support findings.

The NVDL and MDFF were shown to have better energy consumption over their CMOS equivalents, albeit with larger device area. However, in an FPGA architecture, the amount of device area used by the logic blocks far exceeds that of the CMOS sequential logic circuits. Thus, the percentage of device area reduced by using the NVLUT compensates for the additional device area that is used by the NVDL and MDFF.

In conclusion, A memristor-based FPGA architecture replaces SRAM-based FPGA blocks (control, switch and logic) with novel memristor-based blocks. In this article, the SRAM-based logic blocks (SLB) are replaced with the novel CMLB, which is also proposed and presented in this article along with the structure and functionality.

The proposed CMLB is made up of four switch matrices and four MLSs, which consists of a novel NVLUT and a memristive D flip-flop (MDFF), which was designed to improve CMOS D flip-flops. The usage of the 7T1M SRAM cell converts switch matrices to non-volatile (memristive switch block). The memristive

switch block (1.17 times) and memristive sequential circuit (1.63 times) uses larger device area than their CMOS counterparts, but logic cells are used in abundance in the SRAM-based FPGAs which have a reduction of device area by 1.23 times when MLSs are used instead.

The logic blocks are used with different proportions in different FPGA designs, thus the FPGA test designs show that the CMLB uses an overall average of 8.6% lesser device area than the SRAM-based FPGA. Due to the reduction in device area which shortens routing channels, as well as the reduction in transition delay when using memristive blocks, the overall critical path delay was reduced by 1.094 times. It is also postulated that the power consumption of the CMLB is lower than that of the SRAM-based FPGA architecture if non-volatile feature is fully utilized by the CMLB. However, if non-volatile feature is not utilized power consumption of the CMLB increases by 7.1%.

8.2 Future research

Although the effect of electrode material selection on resistive switching mechanisms was studied, a common trend was not found due to the lack of experiments conducted on a series of electrode materials on the same type of bulk layer. For example, various different materials, such as Al, W, Ti, and Ta, can be selected as the electrode for the TiO_2 bulk layer memristor.

The designing of memristive latches and flip-flops other than D-type would also benefit the semiconductor industry, because it provides design and layout flexibility when there is a larger range of sequential logic circuits to choose from.

A larger scale of the memristive-based FPGA architecture that includes more CMLBs, switch matrices and various types of control blocks, as well as I/O blocks needs to be experimented on, whether it is in the form of simulation of physical experiments. This is due to the proposal of a full-extent memristive-based FPGA architecture requires thorough research on the total power supply required and the total amount of device area needed for fabrication of the FPGA chip.

The implementation of the proposed CMLB into a physical FPGA chip is possible by adjusting current CMOS fabrication process to fabricate an MIM device in the vias between metal layers [54]. This would allow further verification of the

research work that has been conducted in this thesis. For this, collaboration with semiconductor companies would provide the opportunity to implement this research work onto a physical FPGA chip, which was however not possible at the time of research.

In the future, the 3D-stacking FPGA could solve a lot of routing delay and device area issues. Therefore, this dissertation postulates that it would be beneficial for researchers to use the CMLB proposed in this article to be used in a memristive-based 3D-stacking FPGA architecture.

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BIBLIOGRAPHY

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APPENDIX

Appendix A: Netlist for enhanced SPICE memristor model with dynamic ground (MEMRISTOR.lib)

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.SUBCKT memristor Pos Neg PARAMS:
+ Ron=100 Roff_on=200 w0=0.5 uv=1e-14
+ D=10n Roff=Roff_on*Ron offset=1n p=5


.IC V(w)={w0*D+offset}


Rser Pos ser 1m
Emem ser Neg
+ value={(Ron*(V(w)-offset)/D+Roff*(1-(V(w)-offset)/D))*I(Emem)}


Gw 0 w value={(I(Emem)*Ron*uv/D)*f((V(w)-offset)/D,I(Emem),p)}
* value={(I(Emem)*Ron*uv/D)}
*+ value={(I(Emem)*Ron*uv/D)*f((V(w)-offset)/D,I(Emem),p)}
Shigh w n1 w 0 highSW
Slow w n2 w 0 lowSW
Vhigh n1 0 DC {D+offset}
Vlow n2 0 DC {offset}
Cw w 0 10n


.FUNC f(x,i,p)={1-(x-stp(-i))**(2*p)}
.MODEL highSW SW(Ron=1n Roff=1G Vt={D+offset})
.MODEL lowSW SW(Ron=1G Roff=1n Vt={offset})
.ENDS memristor
```

Appendix B: Netlist for Non-volatile D-Latch (NVDL.lib)

```
.SUBCKT NVDL VDD D CLK READ CTRL Q Q_ PARAMS:
+ PL=32n PW=2u NL=32n NW=1u


M1 D CLK Q 0 NMOS_32n L=NL W=NW
M2 VDD Q_ Q VDD PMOS_32n L=PL W=PW
M3 0 Q_ Q 0 NMOS_32n L=NL W=NW
M4 VDD Q Q_ VDD PMOS_32n L=PL W=PW
M5 0 Q Q_ 0 NMOS_32n L=NL W=NW
M6 Q_ SWL N001 VDD PMOS_32n L=PL W=PW
M7 N002 SWL Q VDD PMOS_32n L=PL W=PW


XU1 N002 CTRL memristor
XU2 N001 CTRL memristor


A1 CLK READ 0 0 0 SWL 0 0 OR


.LIB MEMRISTOR.lib
.LIB PTM_MOS.lib
.ENDS NVDL
```

Appendix C: Netlist for Memristive D Flip-flop (MDFF.lib)

```
.SUBCKT MDFF VDD D CLK READ CTRL Q Q_ PARAMS:
+ PL=32n PW=2u NL=32n NW=1u


M1 Q SWL N006 VDD PMOS_32n L=PL W=PW
M2 Q_ SWL N005 VDD PMOS_32n L=PL W=PW
M3 N003 CLK N001 0 NMOS_32n L=NL W=NW
M4 VDD N001 N002 VDD PMOS_32n L=PL W=PW
M5 0 N001 N002 0 NMOS_32n L=NL W=NW
M6 VDD N002 N003 VDD PMOS_32n L=PL W=PW
M7 0 N002 N003 0 NMOS_32n L=NL W=NW
M8 Q_ CLK N004 VDD PMOS_32n L=PL W=PW
M9 VDD N004 Q VDD PMOS_32n L=PL W=PW
M10 0 N004 Q 0 NMOS_32n L=NL W=NW
M11 VDD Q Q_ VDD PMOS_32n L=PL W=PW
M12 0 Q Q_ 0 NMOS_32n L=NL W=NW


M§T1 N001 CLK D VDD PMOS_32n L=PL W=PW
M§T2 N002 CLK N004 0 NMOS_32n L=NL W=NW


A1 CLK READ 0 0 0 SWL 0 0 OR


XU1 N006 CTRL memristor
XU2 N005 CTRL memristor


.LIB MEMRISTOR.lib
.LIB PTM_MOS.lib
.ENDS MDFF
```

Appendix D: Netlist for 2TG1M memory cell (2TG1M.lib)

```
.SUBCKT 2TG1M D D_ W W_


XTG1 D N001 W W_ T_GATE
XMemristor N001 N002 memristor
XTG2 N002 D_ W W_ T_GATE


.LIB MEMRISTOR.lib
.LIB T_GATE.lib
.ENDS 2TG1M
```

Appendix E: Netlist for Transmission Gate (T_GATE.lib)

```
.SUBCKT T_GATE IN OUT GATE1 GATE2 VSS PARAMS:
+ PL=32n PW=2u NL=32n NW=1u


M1 IN GATE1 OUT 0 NMOS_32n L=NL W=NW
M2 OUT GATE2 IN VSS PMOS_32n L=PL W=PW


.LIB PTM_MOS.lib
.ENDS T_GATE
```

Appendix F: Netlist for CMOS inverter (INVERTER.lib)

```
.SUBCKT INVERTER IN OUT PARAMS:
+ PL=32n PW=64n NL=32n NW=32n


Vdd VDD 0 DC 1
M1 OUT IN VDD VDD PMOS_32n L=PL W=PW
M2 OUT IN 0 0 NMOS_32n L=NL W=NW


.LIB PTM_MOS.lib
.ENDS INVERTER
```

Appendix G: Netlist for 6-bit Non-Volatile Look-Up Table (NVLUT.lib)

```
.SUBCKT NVLUT DATA EN RD ADD1 ADD2 ADD3 ADD4 ADD5 ADD6 VCC OUT


XUB1 ADD1 WRITE1_ INVERTER
XUB2 ADD2 WRITE2_ INVERTER
XUB3 ADD3 WRITE3_ INVERTER
XUB4 ADD4 WRITE4_ INVERTER
XUB5 ADD5 WRITE5_ INVERTER
XUB6 ADD6 WRITE6_ INVERTER
XUB7 WRITE1_ WRITE1 INVERTER
XUB8 WRITE2_ WRITE2 INVERTER
XUB9 WRITE3_ WRITE3 INVERTER
XUB10 WRITE4_ WRITE4 INVERTER
XUB11 WRITE5_ WRITE5 INVERTER
XUB12 WRITE6_ WRITE6 INVERTER


XUA0 DATA N001 INVERTER
XUA1 ADD1 N004 INVERTER
XUA2 ADD2 N005 INVERTER
XUA3 ADD3 N006 INVERTER
XUA4 ADD4 N007 INVERTER
XUA5 ADD5 N008 INVERTER
XUA6 ADD6 N009 INVERTER
XUA7 ADD7 N010 INVERTER
XUA8 ADD8 N011 INVERTER
XUA9 ADD9 N012 INVERTER
XUA10 ADD10 N013 INVERTER
XUA11 ADD11 N014 INVERTER
XUA12 ADD12 N015 INVERTER
XUA13 ADD13 N016 INVERTER
XUA14 ADD14 N017 INVERTER
XUA15 ADD15 N018 INVERTER
XUA16 ADD16 N019 INVERTER
XUA17 ADD17 N020 INVERTER
XUA18 ADD18 N021 INVERTER
XUA19 ADD19 N022 INVERTER
XUA20 ADD20 N023 INVERTER
XUA21 ADD21 N024 INVERTER
XUA22 ADD22 N025 INVERTER
XUA23 ADD23 N026 INVERTER
XUA24 ADD24 N027 INVERTER
XUA25 ADD25 N028 INVERTER
XUA26 ADD26 N029 INVERTER
XUA27 ADD27 N030 INVERTER
XUA28 ADD28 N031 INVERTER
XUA29 ADD29 N032 INVERTER
XUA30 ADD30 N033 INVERTER
XUA31 ADD31 N034 INVERTER
XUA32 ADD32 N035 INVERTER
XUA33 ADD33 N036 INVERTER
XUA34 ADD34 N037 INVERTER
XUA35 ADD35 N038 INVERTER
XUA36 ADD36 N039 INVERTER
XUA37 ADD37 N040 INVERTER
XUA38 ADD38 N041 INVERTER
XUA39 ADD39 N042 INVERTER
XUA40 ADD40 N043 INVERTER
XUA41 ADD41 N044 INVERTER
XUA42 ADD42 N045 INVERTER
```

```
XUA43 ADD43 N046 INVERTER
XUA44 ADD44 N047 INVERTER
XUA45 ADD45 N048 INVERTER
XUA46 ADD46 N049 INVERTER
XUA47 ADD47 N050 INVERTER
XUA48 ADD48 N051 INVERTER
XUA49 ADD49 N052 INVERTER
XUA50 ADD50 N053 INVERTER
XUA51 ADD51 N054 INVERTER
XUA52 ADD52 N055 INVERTER
XUA53 ADD53 N056 INVERTER
XUA54 ADD54 N057 INVERTER
XUA55 ADD55 N058 INVERTER
XUA56 ADD56 N059 INVERTER
XUA57 ADD57 N060 INVERTER
XUA58 ADD58 N061 INVERTER
XUA59 ADD59 N062 INVERTER
XUA60 ADD60 N063 INVERTER
XUA61 ADD61 N064 INVERTER
XUA62 ADD62 N065 INVERTER
XUA63 ADD63 N066 INVERTER
XUA64 ADD64 N067 INVERTER


XUA65 EN EN_ INVERTER
XUA66 RD RD_ INVERTER
XU65 N001 N002 EN EN_ T_GATE
XU67 N002 N003 RD RD_ T_GATE


XU1 DATA N002 ADD1 N004 2TG1M
XU2 DATA N002 ADD2 N005 2TG1M
XU3 DATA N002 ADD3 N006 2TG1M
XU4 DATA N002 ADD4 N007 2TG1M
XU5 DATA N002 ADD5 N008 2TG1M
XU6 DATA N002 ADD6 N009 2TG1M
XU7 DATA N002 ADD7 N010 2TG1M
XU8 DATA N002 ADD8 N011 2TG1M
XU9 DATA N002 ADD9 N012 2TG1M
XU10 DATA N002 ADD10 N013 2TG1M
XU11 DATA N002 ADD11 N014 2TG1M
XU12 DATA N002 ADD12 N015 2TG1M
XU13 DATA N002 ADD13 N016 2TG1M
XU14 DATA N002 ADD14 N017 2TG1M
XU15 DATA N002 ADD15 N018 2TG1M
XU16 DATA N002 ADD16 N019 2TG1M
XU17 DATA N002 ADD17 N020 2TG1M
XU18 DATA N002 ADD18 N021 2TG1M
XU19 DATA N002 ADD19 N022 2TG1M
XU20 DATA N002 ADD20 N023 2TG1M
XU21 DATA N002 ADD21 N024 2TG1M
XU22 DATA N002 ADD22 N025 2TG1M
XU23 DATA N002 ADD23 N026 2TG1M
XU24 DATA N002 ADD24 N027 2TG1M
XU25 DATA N002 ADD25 N028 2TG1M
XU26 DATA N002 ADD26 N029 2TG1M
XU27 DATA N002 ADD27 N030 2TG1M
XU28 DATA N002 ADD28 N031 2TG1M
XU29 DATA N002 ADD29 N032 2TG1M
XU30 DATA N002 ADD30 N033 2TG1M
XU31 DATA N002 ADD31 N034 2TG1M
XU32 DATA N002 ADD32 N035 2TG1M
XU33 DATA N002 ADD33 N036 2TG1M
XU34 DATA N002 ADD34 N037 2TG1M
XU35 DATA N002 ADD35 N038 2TG1M
XU36 DATA N002 ADD36 N039 2TG1M
XU37 DATA N002 ADD37 N040 2TG1M
XU38 DATA N002 ADD38 N041 2TG1M
```

```
XU39 DATA N002 ADD39 N042 2TG1M
XU40 DATA N002 ADD40 N043 2TG1M
XU41 DATA N002 ADD41 N044 2TG1M
XU42 DATA N002 ADD42 N045 2TG1M
XU43 DATA N002 ADD43 N046 2TG1M
XU44 DATA N002 ADD44 N047 2TG1M
XU45 DATA N002 ADD45 N048 2TG1M
XU46 DATA N002 ADD46 N049 2TG1M
XU47 DATA N002 ADD47 N050 2TG1M
XU48 DATA N002 ADD48 N051 2TG1M
XU49 DATA N002 ADD49 N052 2TG1M
XU50 DATA N002 ADD50 N053 2TG1M
XU51 DATA N002 ADD51 N054 2TG1M
XU52 DATA N002 ADD52 N055 2TG1M
XU53 DATA N002 ADD53 N056 2TG1M
XU54 DATA N002 ADD54 N057 2TG1M
XU55 DATA N002 ADD55 N058 2TG1M
XU56 DATA N002 ADD56 N059 2TG1M
XU57 DATA N002 ADD57 N060 2TG1M
XU58 DATA N002 ADD58 N061 2TG1M
XU59 DATA N002 ADD59 N062 2TG1M
XU60 DATA N002 ADD60 N063 2TG1M
XU61 DATA N002 ADD61 N064 2TG1M
XU62 DATA N002 ADD62 N065 2TG1M
XU63 DATA N002 ADD63 N066 2TG1M
XU64 DATA N002 ADD64 N067 2TG1M


XUZ1 WRITE1_ WRITE2_ ADD1 WRITE1 WRITE2_ ADD2 GATE1 WRITE2 WRITE1_ ADD3
WRITE2 WRITE1
+ ADD4 0 74HC08
XUZ2 WRITE1_ WRITE2_ ADD5 WRITE1 WRITE2_ ADD6 GATE2 WRITE2 WRITE1_ ADD7
WRITE2 WRITE1
+ ADD8 0 74HC08
XUZ3 WRITE1_ WRITE2_ ADD9 WRITE1 WRITE2_ ADD10 GATE3 WRITE2 WRITE1_ ADD11
WRITE2
+ WRITE1 ADD12 0 74HC08
XUZ4 WRITE1_ WRITE2_ ADD13 WRITE1 WRITE2_ ADD14 GATE4 WRITE2 WRITE1_ ADD15
WRITE2
+ WRITE1 ADD16 0 74HC08
XUY1 WRITE3_ WRITE4_ GATE1 WRITE3 WRITE4_ GATE2 GATEX1 WRITE4 WRITE3_ GATE3
WRITE4
+ WRITE3 GATE4 0 74HC08
XUZ5 WRITE1_ WRITE2_ ADD17 WRITE1 WRITE2_ ADD18 GATE5 WRITE2 WRITE1_ ADD19
WRITE2
+ WRITE1 ADD20 0 74HC08
XUZ6 WRITE1_ WRITE2_ ADD21 WRITE1 WRITE2_ ADD22 GATE6 WRITE2 WRITE1_ ADD23
WRITE2
+ WRITE1 ADD24 0 74HC08
XUZ7 WRITE1_ WRITE2_ ADD25 WRITE1 WRITE2_ ADD26 GATE7 WRITE2 WRITE1_ ADD27
WRITE2
+ WRITE1 ADD28 0 74HC08
XUZ8 WRITE1_ WRITE2_ ADD29 WRITE1 WRITE2_ ADD30 GATE8 WRITE2 WRITE1_ ADD31
WRITE2
+ WRITE1 ADD32 0 74HC08
XUZ9 WRITE1_ WRITE2_ ADD33 WRITE1 WRITE2_ ADD34 GATE9 WRITE2 WRITE1_ ADD35
WRITE2
+ WRITE1 ADD36 0 74HC08
XUZ10 WRITE1_ WRITE2_ ADD37 WRITE1 WRITE2_ ADD38 GATE10 WRITE2 WRITE1_ ADD39
WRITE2
+ WRITE1 ADD40 0 74HC08
XUZ11 WRITE1_ WRITE2_ ADD41 WRITE1 WRITE2_ ADD42 GATE11 WRITE2 WRITE1_ ADD43
WRITE2
+ WRITE1 ADD44 0 74HC08
XUZ12 WRITE1_ WRITE2_ ADD45 WRITE1 WRITE2_ ADD46 GATE12 WRITE2 WRITE1_ ADD47
WRITE2
+ WRITE1 ADD48 0 74HC08
```

```
XUZ13 WRITE1_ WRITE2_ ADD49 WRITE1 WRITE2_ ADD50 GATE13 WRITE2 WRITE1_ ADD51
WRITE2
+ WRITE1 ADD52 0 74HC08
XUZ14 WRITE1_ WRITE2_ ADD53 WRITE1 WRITE2_ ADD54 GATE14 WRITE2 WRITE1_ ADD55
WRITE2
+ WRITE1 ADD56 0 74HC08
XUZ15 WRITE1_ WRITE2_ ADD57 WRITE1 WRITE2_ ADD58 GATE15 WRITE2 WRITE1_ ADD59
WRITE2
+ WRITE1 ADD60 0 74HC08
XUZ16 WRITE1_ WRITE2_ ADD61 WRITE1 WRITE2_ ADD62 GATE16 WRITE2 WRITE1_ ADD63
WRITE2
+ WRITE1 ADD64 0 74HC08
XUY2 WRITE3_ WRITE4_ GATE5 WRITE3 WRITE4_ GATE6 GATEX2 WRITE4 WRITE3_ GATE7
WRITE4
+ WRITE3 GATE8 0 74HC08
XUY3 WRITE3_ WRITE4_ GATE9 WRITE3 WRITE4_ GATE10 GATEX3 WRITE4 WRITE3_ GATE11
WRITE4
+ WRITE3 GATE12 0 74HC08
XUY4 WRITE3_ WRITE4_ GATE13 WRITE3 WRITE4_ GATE14 GATEX4 WRITE4 WRITE3_
GATE15 WRITE4
+ WRITE3 GATE16 0 74HC08
XUX1 WRITE5_ WRITE6_ GATEX1 WRITE5 WRITE6_ GATEX2 VCC WRITE6 WRITE5_ GATEX3
WRITE6
+ WRITE5 GATEX4 0 74HC08


XU66 N003 VDD2 VDD1 0 OUT level.2 Avol=1Meg GBW=100G Slew=100G ilimit=25m
rail=0
+ Vos=0 phimargin=45 en=0 enk=0 in=0 ink=0 Rin=500Meg
R1 N003 0 10k
VDD2 VDD2 0 0.5
VDD1 VDD1 0 1.0


.LIB MEMRISTOR.lib
.LIB T_GATE.lib
.LIB INVERTER.lib
.LIB PTM_MOS.lib
.LIB 74HC08.lib
.LIB 2TG1M.lib
.LIB UniversalOpamps2.sub
.ENDS NVLUT
```

Appendix H: Netlist for 7T1M SRAM cell (7T1M.lib)

```
.SUBCKT 7T1M D RD EN Q Q_ VDD PARAMS:
+ PL=32n PW=2u NL=32n NW=1u RR=10k


M1 0 Q_ Q 0 NMOS_32n L=NL W=NW
M2 VDD Q_ Q VDD PMOS_32n L=PL W=PW
M3 0 Q Q_ 0 NMOS_32n L=NL W=NW
M4 VDD Q Q_ VDD PMOS_32n L=PL W=PW
M6 D WORD Q 0 NMOS_32n L=NL W=NW
M5 Q RD N001 0 NMOS_32n L=NL W=NW
M7 N002 EN Q 0 NMOS_32n L=NL W=NW


XM N002 CTRL memristor
Rref 0 N001 RR


.LIB PTM_MOS.lib
.LIB MEMRISTOR.lib
.ENDS 7T1M
```