In-service Estimation of State of Health of Power Modules

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Abstract

The in-service reliability of power electronics modules during their normal operation in their work environment is a major concern for application developers. Failure mechanisms act on power modules limiting their lifetime and leading to unpredictable interruptions of power converter operation. That reduces the availability of power converters and can have large financial and safety implications in applications such as in wind turbines and railway traction. Therefore, many attempts are made to use Physics-of-Failure models to estimate the lifetime of power modules while in service utilizing the rainflow counting algorithm. However, large uncertainty in the lifetime estimate given by Physics-of-Failure methods limits the usefulness of that estimate and cannot help improving the availability of power converters. Condition Monitoring on the other hand provides information about the current health state of power modules based on online measurements of failure indicators that can be obtained from the power modules. This information can be used to inform the prognostics stage to provide an estimate of lifetime based on PoF models and online measurements in a Fusion-based approach such that uncertainty in the resulting lifetime estimate can be reduced.

In this thesis, the main emphasis is to use online measurement data of failure indicators that can be obtained during the normal operation of power modules to infer the health status of the power module. Failure indicators such as the on-state voltage and junction temperature are estimated or measured online from the power converter. They are indicative of the two dominant failure mechanisms of power modules which are wire-bond lift-off and solder fatigue. Therefore, different simultaneous failure mechanisms can be discriminated. However, in order to infer the health information from the online measurement and discriminate between failure mechanisms, the measurement noise and the effects of operating conditions should be removed from the measurement. The approach proposed in this thesis is based on combining online measurements with pre-determined models of the power

module in its original state. Comparing the online measurements with the models reveals the deviation of the power module from its original state. To achieve this, Kalman filter is used to estimate junction temperature based on a noisy estimate from a thermo-sensitive electrical parameter. In addition, measurement circuits are developed to realize the online measurements during normal operation of power modules.

The health information inferred from the online measurement of failure indicators can be used in the future to estimate the remaining useful lifetime of the power modules and to inform the Physics-of-Failure models in a fusion framework in order to reduce the uncertainty in the lifetime estimates.

Acknowledgment

I am grateful to all people who helped me to complete this work. My parents who I could not have achieved my PhD without their support. Special thanks to my supervisor Prof. Mark Johnson who gave me the opportunity to pursue this PhD and who has been very kind an ultimately supportive during all the stages of this work. Many thanks to all the people from within the research group and outside whom I worked with and who helped me throughout my PhD.

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Chapter 1 Introduction

1.1 Introduction

This chapter introduces power electronics modules and their role in the applications of power generation and transmission. The assembly and the packaging of power modules are introduced detailing the structure of the module. Failure mechanisms of power modules are discussed explaining their effect on the reliability and availability of power converters. Then, the role of prognostics and health management is discussed as a means to enable preventive maintenance, which improves availability, reduces maintenance costs and systems downtime.

1.2 Introduction to Power Electronics

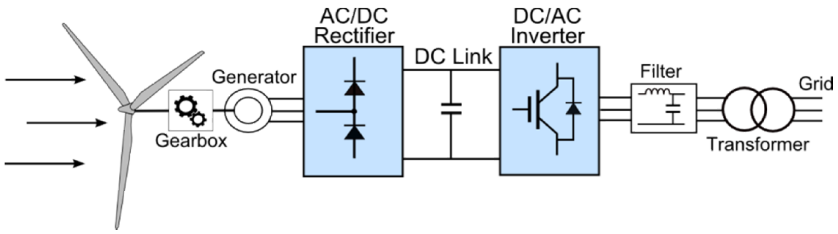
1.2.1 Power Electronics Applications

Reliance on electrical energy has been increasing rapidly over the recent years as a more economic and environment friendly source of energy. The production of energy from renewable sources has increased rapidly over the past years. World consumption of energy produced from renewable sources such as wind, solar, tidal and hydro power for power generation grew by 16.3% of the overall energy consumption in 2013[1]. This figure is increasing each year with the constructions of new onshore and offshore wind farms all over the world [2]. A study at Stanford University stated that renewable energy can provide all world needs of energy [3]. This will result in greater electrical loads which will be sourced from generating stations which are remote from loads such as offshore wind farms.

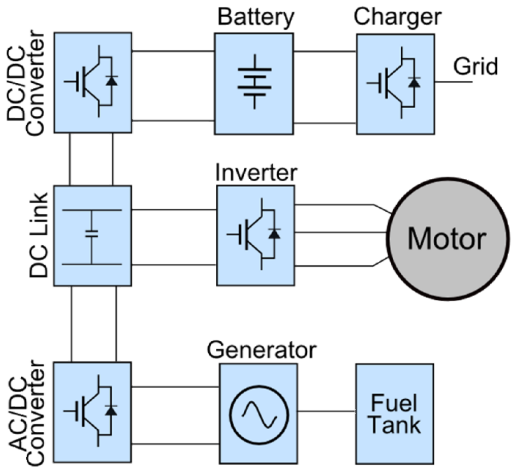
As a consequence of this rapid evolution in electrification and the hunt for efficient power transmission and distribution, power electronics comes to the fore. Power electronics is the tool for electrical power conditioning in transmission, distribution and consumption. It facilitates the control of voltage, current, phase and frequency of electrical power at different levels in the transmission and distribution systems, starting from generating stations (e.g

wind farms and solar farms) through transmission networks and ending in the distribution and consumption end-points.

Power electronics is being used in a variety of applications such as industrial, residential, aerospace, transportation and utility power application such as power supplies, lighting, motor drives, Electric and Hybrid Electric Vehicles EVs/HEVs. As an example, Figure 1.1(a) shows a typical structure of a power electronics system of a wind power turbine. Wind power is converted using a generator into electrical power which can be of variable voltage and variable frequency. This AC power is usually converted then into a DC power using an AC/DC rectifier which is connected using a DC link to a DC/AC converter that allows interfacing the wind turbine with the power grid.



(a)



(b)

Figure 1.1 (a) A typical structure of a power electronics system of a wind power turbine (b) A typical structure of a power electronics system of a Plug-in Hybrid Electric Vehicle (HEV).

Another example of a Plug-in HEV power electronics system is shown in Figure 1.1 (b). The energy is stored in a battery. A DC/DC converter boost up the voltage level in order to supply the DC link which distributes the energy to the inverter unit. The inverter then drives the electric motor by converting the DC power into AC power with variable voltage/frequency which allows controlling the speed of the motor. The electrical system is assisted by a combustion engine which is used to drive the motor and charge the battery using the generator.

Power electronics systems consist of active (semiconductor switches) and passive (resistors, capacitors, inductors) components which are combined together to accomplish the desired functionality of the power converter. Among these components, power semiconductors are the electrical switches that control the flow of current (commutation) in the converter. Power semiconductors are produced in different types such as BJTs, MOSFETs, IGBTs … which have different voltage and current rating and switching speeds. Power semiconductor devices are assembled in modular packages in order to improve their current and voltage capabilities and to facilitate their use and connection to the outer circuit in the power converter.

1.2.2 Power Electronic Modules Packaging and Assembly

Power electronics modules come in multiple packages with different configuration, voltage and current rating. Single switch, dual switch, chopper, and half-bridge are some common configurations of power modules. Figure 1.2 shows two different types of IGBT power modules, a single IGBT switch module is shown to the right and a half-bridge module is shown to the left.

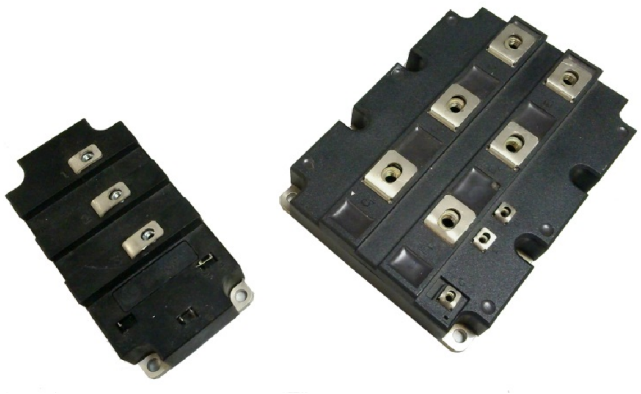


Figure 1.2 Power electronics modules. (Left) Half-bridge module (Right) Single switch module

The assembly of an IGBT power module is shown in Figure 1.3. Multiple IGBT/Diode chips are combined on a substrate tile. One or more substrate tile can be used within the package. The substrate tile is usually made of ceramic with a Direct-Bonded Copper (DBC) to the upper and lower faces. A solder layer is used to attach the semiconductor chips to the top copper of the substrate tile. This solder provides the mechanical attachment of the chip to the substrate. In addition it provides the electrical connection between the collector which constitutes the backside of the chip and the copper trace on the substrate. The substrate tile in its turn is attached to the baseplate using another solder layer providing mechanical attachment. The baseplate is normally made of Copper (Cu) or Aluminum Silicon-Carbide (AlSiC). Aluminium wires provide electrical connection between the chip surface and the copper of the substrate tile. This assembly is ultimately encapsulated with a silicone gel and a plastic casing for improved electrical isolation.

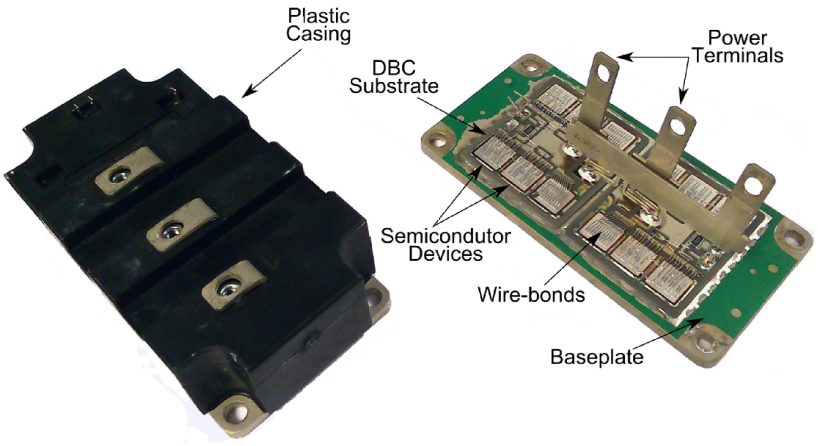


Figure 1.3 The assembly of an IGBT power module

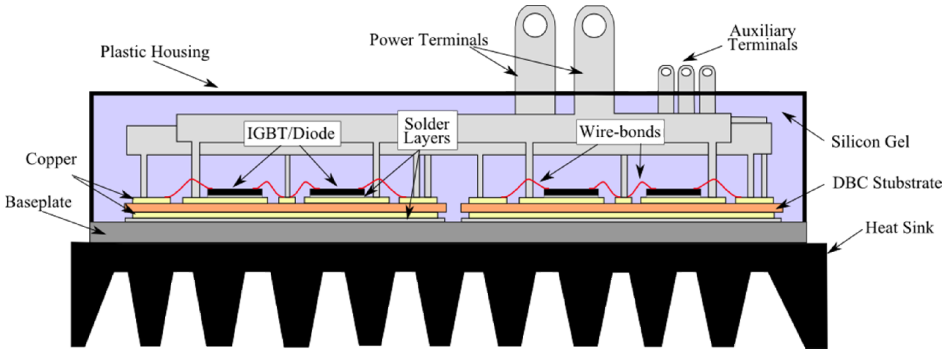


Figure 1.4 The multilayer structure of a power module

This stack of materials constitutes the multi-layered structure of power modules which is shown in Figure 1.4. It provides the heat removal path within the power module. Power semiconductors dissipate electrical energy in the form of heat during their normal operation which causes the temperature of the power modules to increase. This heat propagates through the multilayer structure from the chip toward the baseplate and the heatsink which removes the heat from the power module to the surrounding environment.

The use of different materials in the multilayer structure raises concerns about the reliability and lifetime of power modules since different materials have different coefficients of thermal expansion (CTEs) which can lead to mechanical failures at different sites in the structure (interconnects and solder layers) under thermal cycling. In addition, the semiconductor devices themselves can suffer from thermal and electrical overstressing which in turn can result in the failure of semiconductor chips. The next section details some

of the main reliability considerations for power modules and the resulting failures that might occur.

1.3 Failures and Reliability of Power Modules Packaging

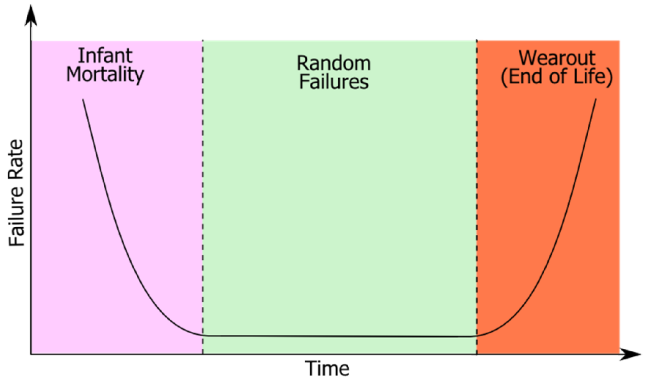


Figure 1.5 The bathtub curve describes the lifetime of the power modules

The lifetime of a power module can be described by the bathtub curve shown in Figure 1.5. The infant mortality stage signifies the early life stage of a power module. In this stage some failures related to the fabrication process may appear. Most of these failures can be detected by qualification testing of the devices during the manufacturing process. Devices that fail the testing are excluded so that the failure rate of the power modules goes down to enter the Random Failures stage. During this period, most of the failures are caused by external factors. Malfunctioning of other components can result in electrical and thermal overstressing which might end up in device failure. For example, the failure of DC capacitors or a lightning strike can result in a voltage surge that exceeds the breakdown voltage of the semiconductor and consequently the chip fails due to overvoltage stressing. Another example is a failure in the load which can result in a short circuit current to pass through the device causing an excess power dissipation and overheating and the chip can fail by burn-out. These types of failure are unpredictable and hence the name “random failures”. Some of these failures can be avoided by protection circuits applied by the gate drive (e.g. short circuit protection). Then the module enters the wearout stage where failures related to mechanical fatigue starts to appear as a result of the cyclic thermo-mechanical stressing. The appearance of these failures signifies the end of power module lifetime.

From the above, failures of power modules can be categorized into chip-related failures and package-related failures. Chip-related failures are mainly induced by thermal or electrical overstressing of the semiconductor chip whereas package-related failures are induced by aging and mechanical fatigue. However, package failures can accelerate or lead to chip-related failure as a secondary mechanism [4].

1.3.1Chip-related Failure Mechanisms

Typically, the gate oxide region is the most vulnerable site in the IGBT device. The failure of the gate oxide is driven mainly by two degradation mechanisms: Time-Dependent Dielectric Breakdown (TDDB) and Hot-Carrier Injection (HCI). TDDB are induced by charges accumulation in the silicon-oxide (SiO_2) interface under normal operation condition. These accumulated charges causes electrical isolation properties of the oxide layer to deteriorate overtime [5]. This leads to the formation of a conductive channel through the oxide which eventually results in gate dielectric breakdown.

Similarly, HCI happens under elevated operating temperature when the electrons gain sufficient energy to jump from the silicon into the gate oxide. Those injected electrons can accelerate the TDDB leading to dielectric breakdown. However, due to the relatively large thickness of the gate oxide of IGBTs devices the degradation of gate oxide dielectric is not considered as a dominant failure mechanism in comparison with the package-related failures [6].

1.3.2Package-related Failure Mechanisms

Cyclic thermal loading of power modules results from the dissipated power in the semiconductor devices. Since the multi-layered structure is made of different materials which have different coefficients of thermal expansion (CTEs), this mismatch in CTEs causes different elongations and contractions between different materials. As an example of the variation in CTEs of material, typical materials used in power modules and their CTEs are listed in Table 1.1 [4]. This leads to the development of mechanical stresses at the interfaces between those materials. These stresses are most significant at two sites within the power module packaging: wire-bonds and solder layers.

Therefore, wire-bond lift-off and solder fatigue are the two dominant failure mechanisms of the power modules.

Table 1.1 Materials used in power modules packaging and their CTEs [4]

Material	CTE (ppm/^{o}C)*
Aluminium (Al)	22
Silicon (Si)	3
Aluminium Nitride (AlN)	4
Copper (Cu)	17
Aluminium Silicon-Carbide (AlSiC)	8

*ppm/^{o}C: part-per-million (10^{-6}) per ^{o}C

1.3.2.1Wire-bond Interconnects

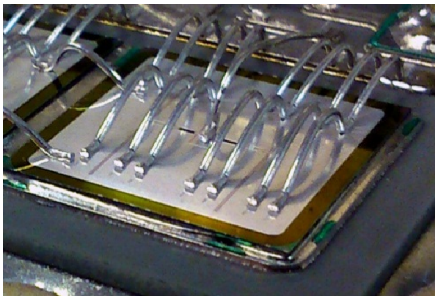


Figure 1.6 A photograph of the wire-bonds on a semiconductor chip

Wire-bonds provide the electrical connection between the metallization on the top surface of the chip and the copper traces on the substrate tile. Aluminium wires are typically used in power modules. Essentially, the wire-bonds on the active area of the chip are the most susceptible to fail due to mechanical fatigue since they are subject to the highest temperature swing, whereas the wire-bonds on the copper traces are less vulnerable as they experience lower temperature swings. In addition, CTE mismatch between aluminium and copper is lower than it is between aluminium and silicon as can be seen in Table 1.1.

Under mechanical stressing, cracks are initiated at the boundaries of the bonded area of the wire. At these boundaries the highest level of stress develops since the expansion of the wire is restricted at the edges of the bond pad [7]. Hence, cracks propagate from the edges towards the centre of the

bonded area through the pad between the wire and the metallization or through the body of the wire which is usually aluminium wire as can be seen clearly in Figure 1.7. Wire heel is another site where cracks can initiate and propagate through the body of the wire. However, failure at this site is rarely observed in the modules manufactured with recent bonding technologies [4].

When cracks reach the centre of the bond from both sides the wire-bond lift-off and the electrical connection between the wire and the chip is lost. This causes the current to be redistributed through the other attached wires such that remaining wires conduct more current and get hotter. This result in higher temperature swings at the remaining attached wires which accelerates the failure of the remaining wire-bonds. The loss of the electrical contact between the wire and the chip results in an increment of the electrical resistance of the power module.

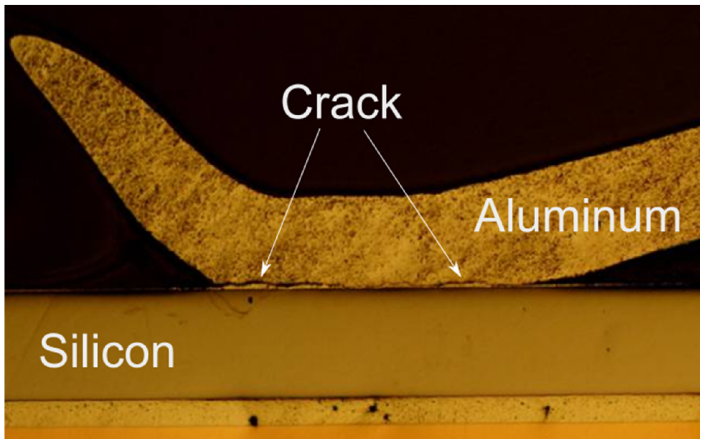


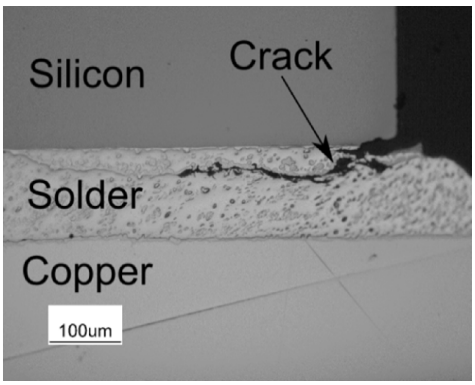
Figure 1.7 A metallurgical cross-sectioning image shows the cracking at the bonded pad between the silicon chip and the aluminium wire.

1.3.2.2Solder layer degradation

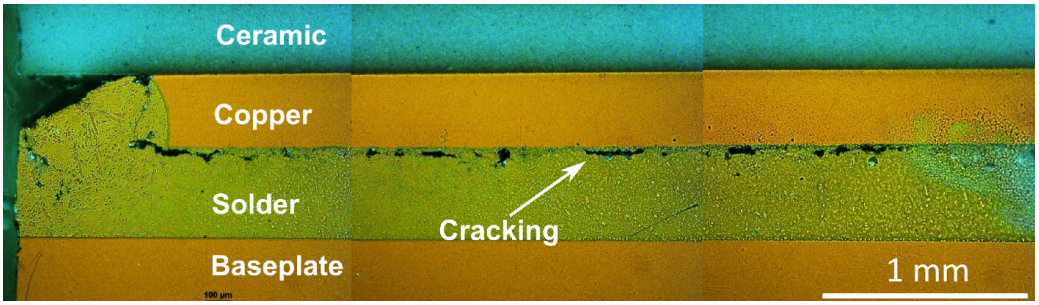
In a similar way to the failure of wire-bonds, the CTEs mismatch between the solder and the copper and between the solder and the silicon results in mechanical stresses under cyclic thermal loading at the die-attach layer and the substrate mount-down solder. These mechanical stresses are maximum at the corners of the solder layers due to the restricted elongation [8]. Therefore, cracks typically start initiating at the corners and propagate towards the center of solder layers. In addition, there will be voids which may

residue from the manufacturing process. Those voids constitute high mechanical stress locations where cracks can initiate and propagate. Hence, the voids can expand under thermal cycling and congregate together forming larger voids [9]. An example of the die-attach layer cracking is shown in Figure 1.8 (b)

As solder layers constitute a part of the heat conduction path, cracking and voiding of the solder layers obstruct the flow of heat through the multi-layered structure to the heatsink. This diminishes the local thermal flux and increases the thermal resistance of the package which consequently increases the temperature of the power module. This temperature increment accelerates the thermally driven mechanical fatigue process resulting in positive feedback of the degradation process. In addition, localized heating and hot spotting resulting from voiding and cracking at the die-attach layer can end up in chip burn-out due to over temperature.



(a)



(b)

Figure 1.8 A cross-sectioning image shows the cracking at (a) the die-attach layer (b) the substrate solder layer

1.3.3Summary

In brief, failures related to the aging of the packaging dominate the reliability of the power modules. As a result of packaging failure, power modules eventually fail by over temperature (due to solder fatigue) or by the loss of electrical connection (due to wire-bond lift-off). The failure of power modules disrupts the operation of the related power converters resulting in interruptions of service which can lead to consequential economic and social losses.

The attainment of high availability is essential in some applications such as space, offshore wind turbines and transportation since system downtime and/or failure may incur significant financial expenses. Moreover, maintaining the power converter can be difficult in some applications. For example, off-shore wind turbines are inaccessible during some times of the year due to weather conditions. Therefore, achieving high reliability of power modules in the design, manufacturing and in-service is very important to improve the availability of power converters.

1.4**Traditional Handbook Methods for Reliability Assessment**

Reliability assessment has, for a long time, been based on the traditional method of constant failure rate models. Mean-Time- To-Failure (MTTF) is the most common measure of reliability. It is a measure of the time (years, hours …) that an item can operate before the first maintenance is required. It is expressed as the inverse of the failure rate λ. The failure rate is normally expressed in FIT (Failure-In-Time) which is equivalent to ($1x10^{-9}$ h^{-1}) where (h^{-1}) is (1/hour).

In order to calculate the MTTF for a specific component the failure rate λ needs to be determined. Failure rate λ can be determined from reliability handbooks. Multiple handbooks are available and they define different reliability standards. Some available reliability handbooks are: Siemens SN29500 for telecommunication applications, FIDES for aeronautical and military applications, SAE for automotive and Mil-Hdbk-217 for military applications. Failure rate models defined in those handbooks are identified from data of failed components returned from operation field. Therefore, those

models are classified according to the work environment (e.g. military, aerospace, …) the components were returned from.

After the failure rate λ is determined, component reliability *R(t)* and Mean-Time-To-Failure (MTTF) can be calculated as follows:

$$MTTF = {}^{1}/_{\lambda} \quad \textbf{(1.1)}$$

$$R(t) = e^{-\lambda t} \quad \textbf{(1.2)}$$

1.4.1Limitations of Handbook Methods

Traditional failure rate models suffer many limitations. These models are identified and classified for specific work environments where different loading conditions are applied to the components. That is because the lifetime of a component depends on its work environment and it usage profile. In other words, failure rate models have types of stresses and loading profiles implicitly defined and the user of these models has no access or control over these conditions. This can lead to a lack of confidence in the resulting lifetime estimates given by the failure rate models. Even if models from similar environment are used, significant differences may appear between lifetime estimates which increases level of uncertainty [10]. This is because component lifetime is affected by many factors that are not considered by failure rate models such as maintenance procedures, differences in material properties and geometric design.

In order to classify failure rate models according to work environment, handbooks of reliability are produced. These handbooks are updated on a rate of 6 years [11] to compensate for the changes in factors affecting reliability estimates. However, even with updated models the results can be inaccurate as new designs and technologies are being assessed by models which were identified using data collected from old items produced using old designs and technologies.

Hence, the credibility of reliability handbooks are questioned by many researchers [10-12] and the lack of an alternative solution for reliability estimation methods is identified. The need for alternative methods for reliability estimation that can make use of loading profiles, design and material

properties to assess reliability has been addressed, in addition to the need for reliability assessment while components are in field operation which can support maintenance procedures and improve system availability.

1.5 Improving Availability of Power Converters by Predictive Maintenance

The availability of a system is defined as the probability of the system functioning properly without failures at any point in time. Availability of a system is related to its reliability and maintainability. This relationship can be defined mathematically by the expression:

$$A = \frac{MTTF}{MTTF + MTTR} \tag{1.3}$$

where A is the availability, the Mean-Time-To-Failure (MTTF) defines system reliability as mentioned earlier. The Mean-Time-To-Repair (MTTR) is the time needed to maintain the system by eliminating the failure and returning it back to operation and it defines system maintainability. The higher maintainability the system has the shorter time it takes to be repaired. From this expression it can be seen that the availability of a system can be improved by increasing system reliability and decreasing its downtime by increasing its maintainability. Higher maintainability, and consequently higher availability, can be achieved by two ways: Redundancy and Predictive Maintenance.

1.5.1 The Concept of Redundancy

Typically, system availability depends on the availability of the subsystems constituting it. In order for a system to achieve its proposed functionality all subsystems should be operational. This is normally expressed by series connected subsystems as it is depicted in Figure 1.9(a). The failure of any subsystem (X or Y) prevents the overall system from performing its functionality and consequently results in the failure of the overall system. For the series connected subsystems, the overall availability is expressed as the product of the individual availabilities of the constituting subsystems (X and Y):

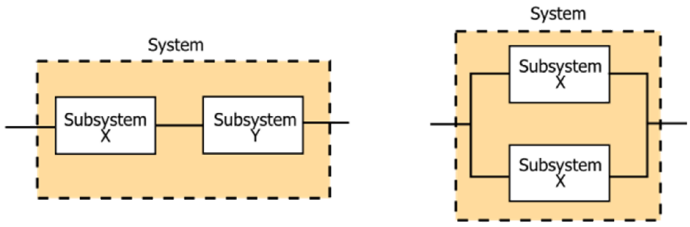
$$A = \prod_{i=1}^{n} A_i \qquad \textbf{(1.4)}$$

where A is the availability of the overall system and A_i is the availability of the subsystems constituting it. According to this equation, a subsystem with low availability can reduce the overall availability of the whole system.

Therefore, in order to improve the availability of the overall system, a redundant subsystem of the low availability subsystem (X) is added in parallel as shown in Figure 1.9(b) . For two parallel connected subsystems, the overall availability is expressed as:

$$A = 1 - (1 - A_X)^2 \qquad \textbf{(1.5)}$$

This expression shows that the availability can be significantly increased by duplicating subsystems of low availability. This is the definition of redundancy concept which is used in availability-critical applications to increase power system availability.



(a) **(b)**

Figure 1.9 (a) Series connection of subsystems (b) Parallel connection of subsystems

However, redundancy suffers drawbacks related to increased cost and weight. In addition, it comes as a remedial solution after system failure so it does not achieve any protection against failure. On the other hand, scheduled maintenance can improve availability and protect systems from unpredicted failures through periodic check-ups and replacement of critical components.

1.5.2 Predictive Maintenance

Maintenance can be classified as corrective and preventive. Corrective maintenance is the unscheduled remedial procedures that are carried out as a consequence of failure. It is performed to eliminate the failure and return the

system back into operation. Preventive maintenance, on the other hand, is a scheduled periodic maintenance that is carried out to ensure high system availability by performing periodical inspections and replacement of consumable parts in order to prevent catastrophic failures.

Costs associated with maintenance procedures make the achievement of high system availability an expensive task. There is a trade-off between achieving high system availability and cost of maintenance. This trade-off is explained in Figure 1.10. Increasing reliance on corrective maintenance reduces system availability due to the long downtime that may result from catastrophic failures which adds up to the maintenance costs and consequently increases the overall cost. Long system downtime can results from the lack of logistics, site inaccessibility or the unavailability of maintenance labour. On the opposite side, increasing the frequency of the preventive maintenance procedures can achieve higher system availability and reduces the corrective maintenance procedures required, but can at the same time increase the cost of maintaining the system.

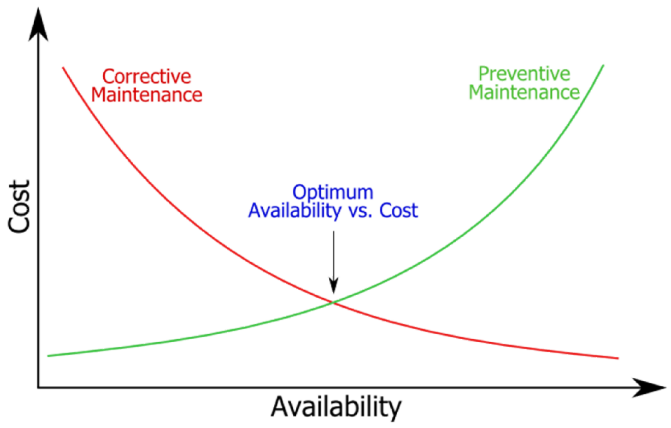


Figure 1.10 The trade-off between availability and cost of maintenance

Therefore, a compromise between availability and cost can be achieved by an efficient combination between corrective and preventive maintenance. This can be achieved by predictive maintenance which is based on the evidence of need. That means maintenance procedures can be performed only when required by monitoring the critical components and assessing the severity of degradation and failures within them. Consequently, corrective

maintenance and preventive maintenance procedures can be reduced which reduces maintenance cost keeping system availability at high levels. In order to enable that, prognostics and health monitoring techniques and condition monitoring techniques need to be implemented.

1.6 **Motivation**

Some recent studies focused on reliability quantification of power converters components by the examination of statistical samples [13-16]. It has been concluded in those studies that power semiconductor modules and DC capacitors are the most fragile components in power converters. However, the ranking of the most delicate component in a power converter differs according to many factors such as mission profiles, operating environment and the manufacturing technologies.

In addition, some reports stated that power converters have the highest failure rate in electrical energy generating systems. For example, in the "Wind Energy Report in Germany 2008" [17] power converters are stated as the highest failure rate component in wind turbines. Similar observations are found in photovoltaic systems. For example, in a study of a utility-scale photovoltaic plant in the US [18] it is noticed from maintenance data that the power inverter has recorded the highest failure rate and it was responsible of the highest unscheduled maintenance events which consequently contributed to the major amount of maintenance cost.

In order to improve availability of power converters, multiple studies have advised to put more effort into condition/health monitoring for power electronics [6, 13, 19-21]. Prognostics and condition/health monitoring provides diagnostic information about impending failures which allows maintenance staff to take scheduled maintenance actions and prevent catastrophic failures. It can provide an estimate of the criticality level of failure which can support the decision process regarding the required actions. It enables efficient maintenance to be carried out having a previous knowledge about failure site and faulty components which improves maintainability.

Multiple approaches to prognostics are available. Physics-of-Failure (PoF) based methods are based on lifetime models obtained from principal

understanding of the failure mechanisms. These model-based methods rely on the mission profile to estimate the lifetime. Canaries, on the other hand, are another approach for prognostics. A hardware device called canary similar to the monitored device with a pre-calibrated lifetime can give an early indication of an imminent failure of the monitored device. Data-based approach to prognostics is based on the measurement of failure indicators under predefined conditions. Trends in the measured failure indicators can then be used to give lifetime estimates.

Condition/Health monitoring methods are based on the evaluation of reliability indictors that can be monitored in-service during the normal operation of power converters. It helps detecting emerging failures and preventing their development into catastrophic failures which ensures safe operation of power converters. It can reduce cost of maintaining the system by reducing scheduled maintenance procedures and enabling the reliance on preventive maintenance.

In addition, analysing the health monitoring data allows better understanding of the relationship between usage profiles and dominant failure mechanisms which can inform the design process to optimize design for reliability [22]. Condition/Health monitoring enables estimation of the remaining useful life of power modules based on the online measurement data without the need for a previous knowledge of the loading profiles. A lifetime estimate can be produced under any arbitrary loading profile.

Some of the challenges of real-time health monitoring of power modules can be identified. Firstly, achieve the online measurement of the failure indicators which show indications of failure using external measurements since sensors are difficult to be embedded inside the device packaging and require special consideration. In addition, measurement noise is an important issue which results in distortion of the online measurements and hinders the changes related to failures. Secondly, junction temperature of power devices is a very important parameter that drives degradation processes in power modules. Obtaining an accurate measurement of junction temperature has been a challenge due to infeasibility of sensor mounting and inaccessibility

to the measurement location. Thirdly, extract failure signatures from the online measurements by removing the effects of operating conditions. Lastly, distinguish between effects of different failures on failure indicators where different failures can leave similar effect on failure indicators and it is important for the diagnosis to separate between the failures.

Therefore, in order to enable an efficient real-time health monitoring of the power modules, measurable failure indicators should be identified. The measurement of these failure indicators should be achieved online without interruption of the normal operation of power converters. Care should be taken to the accuracy of the online measurement as changes due to power module degradation can be small. Then, proper processing of the measurement data is required to extract information about the health state and remove masking effects of operating conditions. Hence, clear indications of degraded state of power modules can be identified.

1.7 **Structure of the thesis**

Chapter 2 introduces the state-of-the-art of the prognostics and health monitoring for power modules. In this chapter, Physics-of-Failure based methods, canaries, data-based methods and model-data fusion based methods are reviewed. Then condition monitoring for the two dominant failure mechanisms (solder fatigue and wire-bond lift-off) are presented.

Chapter 3 is a background about the available methods to estimate junction temperature in power modules. Thermal modelling methods and measurement methods of junction temperature are presented. Thermo-sensitive electrical parameters TSEPs are reviewed and methods to achieve online measurements of TSEPs are presented.

The proposed method for health monitoring of IGBT power modules is presented in Chapter 4. In this chapter, a background of Kalman filter is presented which is used to estimate junction temperature. Then, the theory of analytical redundancy which is the method used to extract health information from online measurements is presented.

In Chapter 5, the experimental investigation of two electrical parameters (on-state voltage $V_{CE(ON)}$ and gate threshold voltage V_{th}) is presented where temperature and failure correlation to these two parameters is investigated. The circuits required to achieve the online measurement of these two parameters are presented in Chapter 6 where the effect of noise on the measurement and on the estimate of junction temperature obtained from these two TSEPs is investigated.

Chapter 7 investigates by simulation and experiment the application of Kalman filter to estimate junction temperature of IGBT power modules. Modelling of the thermal path of power modules is presented in addition to the power loss modelling and electrical modelling. The improvement in accuracy of the junction temperature estimate given by Kalman filter compared to the estimate given by TSEP is demonstrated by simulation and experiment.

The application of analytical redundancy to extract health information from online measurements by the use of pre-defined models of the power module in its original state is demonstrated in Chapter 8. A power cycling test is performed to activate the failure mechanisms of the power module. The results of the proposed real-time method are compared with the results of the power cycling test. Finally, conclusions and scope for future work is presented in Chapter 9.

Chapter 2 Review of Condition Monitoring, Prognostics and Health Management of Power Electronics

2.1 Introduction

A thorough review of the different approaches to lifetime estimation and health monitoring for power electronics modules are presented in this chapter. The Physics-of-Failure (PoF) methods and the data-based methods are discussed. Condition monitoring of power converters proposed for online health monitoring is then presented.

2.2 Approaches of Prognostics and Lifetime Estimation

2.2.1 Canaries

The concept of canaries is derived from the coal mining industry. Canary birds were used in coal mines in the past as an indicator of hazardous gas leakage to alarm workers to evacuate the site. That is because the canary birds are more vulnerable to gases than humans. Hence, the death of a canary is an early indicator of an impending failure or hazard.

Goodman et al [23] introduced the concept of a "prognostic cell" that is co-located with the host circuit to provide an early warning of failure. The prognostic cell fails before the actual circuit so that it predicts circuit failure. This "prognostic cell" has become commonly known as a "Canary" since the same concept of a canary bird applies. It is integrated on the same board/package and therefore it is subject to the same loading and environmental conditions. The lifetime of a canary device can be calibrated to be shorter than the monitored device so that it fails earlier and provides an advance warning of an ongoing failure. Hence, a maintenance procedure can be carried out to prevent unpredicted failure.

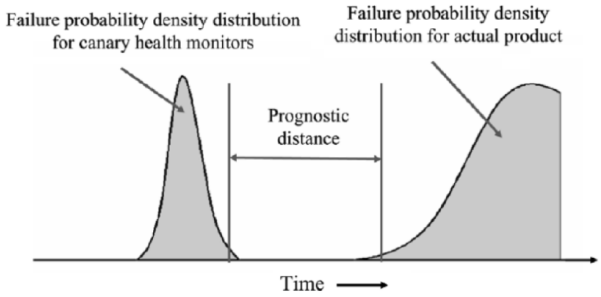


Figure 2.1 The working principle of canaries [23].

Figure 2.1 describes the working principle of canaries. The failure probability of a canary is higher than the failure probability of the actual component at the End-of-Life stage of the component. The prognostic distance is the time between the canary failure and the failure of the monitored device. This time allows maintenance procedures to be completed to replace the component. Multiple canaries can have their lifetime distributed along the time vector providing multiple indications during different lifetime stages.

Many studies demonstrate the use of canaries for electronics components [23-25] and some canaries have been commercialized [26]. An example of canaries for Surface-Mount-Device (SMD) resistors is shown in Figure 2.2 where the narrow soldering pad fails before the standard soldering pad. This helps indicate the impending failure of the standard resistor at an early stage. However, there are still many challenges obstructing their application on a wider scale [25].

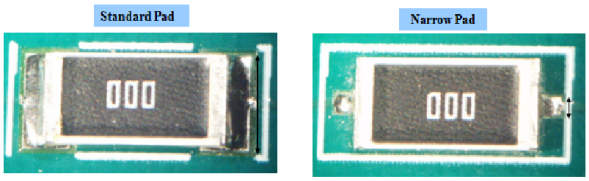


Figure 2.2 An example of Canaries . (a) Actual Resistor with standard soldering pad (b) A Canary Resistor with a narrow soldering pad [24]

2.2.2Physics-of-Failure Approach

The first appearance of the term of Physics-of-Failure (PoF) goes back to 1961 when Rome Air Development Center (RADC) initiated the “Physics-of-Failure” program to enhance the knowledge of failure mechanisms and

physical and chemical process driving the failure of electronic components [27].

Physics-of-Failure (PoF) approach is proposed as an alternative to the traditional handbook methods to overcome their drawbacks. PoF models describe the physical process of a failure mechanism. They focus mainly on the wear-out mechanisms resulting from component aging. Physics-of-Failure approach is proposed to make use of the available knowledge of material properties, geometries, environmental and operational stresses to produce an estimate of component lifetime. Unlike traditional methods, it can assist the design and manufacturing process and allow optimizing design parameters for improved lifetime.

One of the first attempts was made by James Black [28] in 1967 who introduced a PoF model to describe the electromigration of aluminium interconnects which was a limiting factor for integrated circuits reliability. Many other PoF models started to be developed afterwards for other failure mechanisms for integrated circuits such as Hot carriers [29] and Time-dependent dielectric breakdown [30]. Package-level failure mechanisms started to be considered by the Physics-of-Failure approach after its success on the chip-level. Multiple PoF Models based on cyclic fatigue and fracture mechanics are proposed [31].

Some of the advantages of PoF can be stated as the ability to incorporate reliability prediction within the design process since it gives the possibility to assess the use of new materials and new design parameters on product lifetime. It can be used during the design stage to optimize the product lifetime for certain application environment by mitigating the root-cause of failures. For example, a specific design structure of the module can be simulated under a specific loading profile and developing stresses can be calculated which allows estimating the lifetime of that module.

However, PoF approach is still an immature field and suffers many drawbacks. In addition, failures may emerge simultaneously and can be mutually affected by each other leading to accelerated degradation [32, 33]. This phenomenon is not yet addressed by PoF approach. Moreover, PoF

models are determined for specific ranges of loading and environmental conditions, therefore getting lifetime predictions for a product under multiple working conditions can be a time consuming process. In addition, the uncertainty of the lifetime estimates given by the PoF models may be large. That can arise from uncertainties in the manufacturing process which emerge from the spread of the geometrical parameters and the material properties.

Recent work in the field of Physics-of-Failure started to focus on the real-time implementation of PoF models in order to enable more efficient and more accurate reliability prediction. Since component lifetime is driven mainly by its loading and environmental conditions, the real-time implementation of PoF approach allows use the actual loading and stresses to estimate component lifetime.

A typical implementation of PoF-based lifetime estimation is shown in Figure 2.3. This method is proposed by CALCE group [34]. It starts by conducting a Failure Mode, Mechanism and Effect Analysis (FMMEA) to identify potential failure mechanisms of a specific component under certain conditions. It is followed by a virtual reliability assessment which identifies the dominant mechanisms and the required environmental (temperature, humidity, vibration, …) and operational (currents, voltages, …) variables for in-situ monitoring. The monitored loading profiles are analysed and transferred into a feature form applicable to PoF models. The analysis and features depend on the parameter being monitoring (temperature, vibration,…) , the failure mechanism and the model being used.

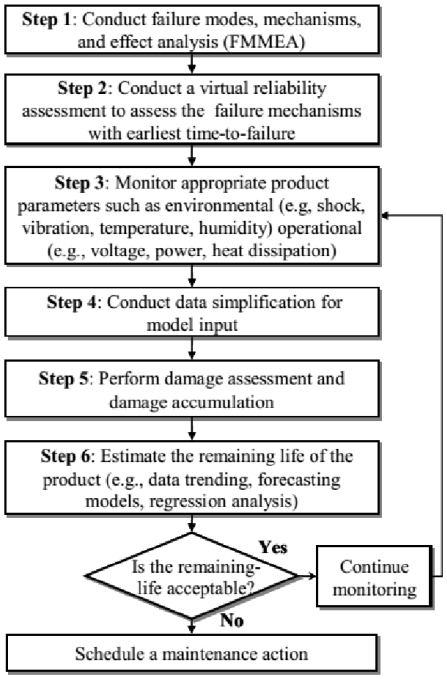


Figure 2.3 The Life Consumption Monitoring method proposed by CALCE [34].

To enable real-time implementation of PoF, a set of tools are needed to achieve the monitoring of loading profiles, analysis and extraction of the features required by the PoF model.

2.2.2.1Failure Mode, Mechanism and Effect Analysis (FMMEA)

Failure Mode, Mechanism, and Effect Analysis (FMMEA) is a procedure proposed to identify potential failure mechanisms and models for all failure modes and to prioritize failure mechanisms [35]. It evaluates potential failures and their effects on operational parameters and suggests potential actions to mitigate their emergence [36]. It documents the failure mechanisms and their physical models in order to enable their use during design and manufacturing process. FMMEA identifies critical loading and environmental parameters that need to be controlled in order to mitigate emerging failures.

2.2.2.2Data Reduction and Cycle Counting Methods

The operational and environmental variables which drive failure mechanisms need to be monitored in-situ and recorded over an extended period of time. This long data record implies difficulties related to data storage and subsequent analysis of this data which can be limited by the computing resources. Loading profile data is typically inapplicable to PoF models in its

raw format and requires pre-processing to extract the required features that can be applied to PoF models.

Many algorithms were investigated by researchers and compared for their accuracy, efficiency of data size reduction and applicability for PoF-based prognostics. For cycle based PoF models, Dowling [37] compared six cycle counting methods. He explains that rainflow algorithm and Rang-Pair counting algorithm give the most reasonable results as they produced more accurate results compared to other counting algorithms.

The Rainflow algorithm is demonstrated by Musallam [38] for cyclic thermal loading of IGBT power modules where the time data of temperature profile is transformed into mean T_m and range ΔT features in order to be applied to a Coffin-Manson type PoF model. Ordered Overall Range (OOR) algorithm is explained by Ramakrishnan [39]. Similar to the Rainflow algorithm, it transforms the irregular loading profile into a regular sequence of peaks and valleys eliminating loading features which have negligible effect on component damage while preserving the features that contribute to the damage. Another similar method called the Hayes method for data simplification is explained by Fan [40].

2.2.2.3Lifetime Models

Lifetime models for cycling fatigue can be categorized into two types [31]: thermal fatigue models and fracture mechanics based models. Thermal fatigue models originate from Coffin-Manson relationship which correlates lifetime expressed as a number of cycles to failure N_f to the cyclic strain loading [41]:

$$\frac{\Delta\varepsilon}{2} = \left(\frac{\sigma_f - \sigma_0}{E}\right)\left(2N_f\right)^b + \varepsilon_f\left(2N_f\right)^c \qquad \textbf{(2.1)}$$

where $\Delta\varepsilon$ is the strain amplitude, σ_f and ε_f are fatigue constants, E is the Young's modulus, σ_0 is the mean hydrostatic stress, b is Basquin constant and c is the Coffin-Manson constant. Many simplified versions of this relationship were proposed (e.g. Engelmaier [42] and Held et al [43]).

Fracture mechanics based models on the other hand, focus on modelling the crack growth process in ductile materials. The most common model of crack propagation is the Paris' Law which correlates crack growth rate with stress intensity factor:

$$\frac{da}{dN} = C(\Delta K_\varepsilon)^n \qquad \textbf{(2.2)}$$

where a is the crack length, N is number of cycles to failure, ΔK_ε is the stress intensity range, C and n are material constants.

These lifetime models can be identified using accelerated aging tests [42, 43]. The input to these lifetime models is the applied stress parameters (e.g. $\Delta\varepsilon$, ΔK_ε, ...) which are extracted by the cycle counting algorithm. They produce a lifetime estimate related to the applied stress profile. However, loading profiles can be irregular and applied stresses can vary overtime, and therefore a damage model is required to accumulate damage caused by different stress levels.

2.2.2.4 Fatigue Cumulative Damage Models

The most common cumulative fatigue damage model is the Linear Damage Model proposed by Miner in 1945 [44]. The damage is expressed as a linear summation of the cycle ratio where each cycle ratio corresponds to an individual loading range. The Linear Damage Model can be expressed by:

$$D = \sum r_i = \sum {}^{n_i}/_{N_{fi}} \qquad \textbf{(2.3)}$$

where D is the total damage, r_i is the cycle ratio, n_i is the applied cycles N_{fi} is the cycles to failure under the ith loading range. When $D=1$ the component is considered to be failed.

Other models for cumulative damage have been proposed such as nonlinear damage curve, energy-based, crack growth and others. An extensive review of the cumulative damage rules is presented by Fatemi [44].

2.2.2.5Examples of Real-time PoF-based PHM for Power Modules

Recently, there have been attempts to use PoF models to estimate lifetime of power modules in their work environment by the online

implementation of PoF methods which can enable a more accurate estimation of lifetime. Musallam et al [45] proposed a real-time PoF approach for IGBT power modules. First, the loading temperature profile is calculated using a reduced-order thermal model. Then, the temperature profile is analysed using the rainflow counting algorithm to extract the temperature swings ΔT and mean temperature T_m. These features are translated into mechanical stress using a response surface model obtained from a FEA simulation [46]. The calculated mechanical stress forms the input to a Coffin-Manson type lifetime model which is used with the Linear Damage accumulation rule to calculate life consumption of wire-bonds and solder joints. Figure 2.4 describes a block diagram of the proposed implementation.

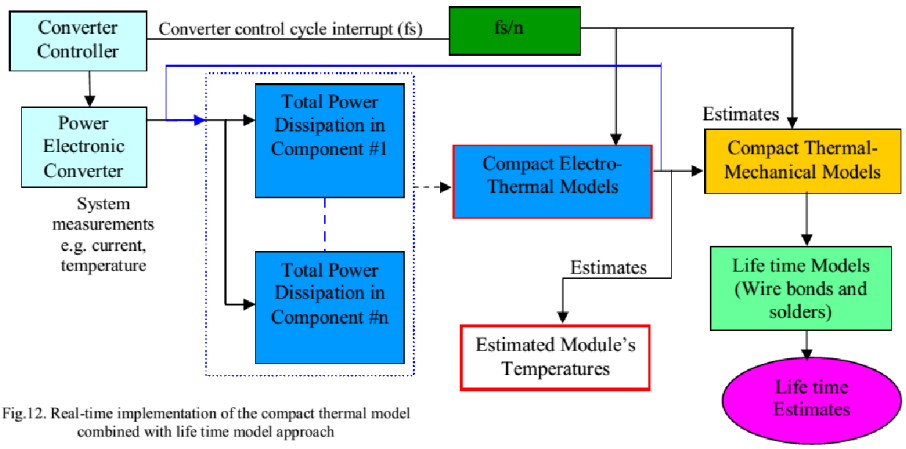


Figure 2.4 Real-time implementation of thermal model with lifetime PoF model [45]

Similar approaches are proposed by other researchers such as in [47] where temperature loading profile is estimated using a thermo-sensitive electrical parameter and the Rainflow counting algorithm is modified so that output features are applicable to a lifetime model proposed by Bayerer [48]. The use of Rainflow algorithm and Coffin-Manson type lifetime models is also demonstrated by Hui [49] and Bohllander et al [50] for wind turbine applications.

2.2.3Data-based Methods

Data-based methods essentially use in-situ measurements of failure precursors to produce lifetime estimates. Failure precursors are measureable parameters that are correlated to failures. Measurements data changes its

statistical characteristics over time as a result of degradation. Therefore, detecting trends in the data overtime allow detecting impending failures and estimating time to failure [51].

On-state voltage $V_{CE(ON)}$, threshold voltage $V_{GE(th)}$, leakage current I_{CES} and junction temperature T_J are all failure precursors of semiconductor devices [52]. Each parameter can be affected by one or more failure mechanism. For example, the on-state voltage $V_{CE(ON)}$ of IGBT devices can be affected by wire-bond failures and solder fatigue. In addition, some of these parameters can be affected by loading conditions which masks the effect of failures. Therefore, it is common to do the measurement of failure indicator under controlled conditions in order to isolate the effects of loading from the effects of failures.

In data-based methods, lifetime estimates are purely calculated from the data. Black-box non-physical models are used to learn the time behaviour of the historical data. These models are then used to make predictions of future evolution of the failure precursors and therefore a lifetime estimate can be produced. In order to do that, a threshold value is defined for the failure precursor to indicate component end-of-life [53]. At the moment when the value of the failure precursor exceeds the defined threshold value a failure is declared. Threshold value can be defined based on previous knowledge and experience. However, defining the failure threshold is still a common problem [54].

2.2.3.1Advantages and Disadvantages of Data-based PHM

Unlike PoF methods, data-based methods do not require previous knowledge of the physical process of failure, material properties and design parameters. They can give lifetime estimate based only on in-situ measurements which can produce an up-to-date lifetime estimate. They can be applied in cases where competing failures emerge simultaneously. Multiple failure mechanisms can be monitored where each precursor is related to a specific mechanism. However, some failure precursors can be affected by more than one failure which may require advanced algorithms to isolate the effect of simultaneous failure mechanisms.

On the opposite side, the disadvantages of data-based methods include: the need for training data which is required to determine the correlation between the data and the corresponding failure mechanisms. Sufficient data is required to define an empirical model to be used for lifetime estimation. Data-based methods require defining a failure threshold which is yet an open research problem. Lifetime estimates produced by data-based methods depend on the quality of the training data. If data suffers inaccuracies, lifetime estimates can be inaccurate. Failure indicators are correlated to operating conditions, therefore if operating conditions are changed the algorithm must be re-trained [55]. Moreover, data-based methods are accurate at the component end-of-life where the trends in failure precursors become clearer. Whereas it is less accurate during the useful life period of the component where no indication of wear-out may be noticed in the monitored data.

2.2.3.2Examples of Data-based PHM for Power Modules

Many demonstrations are available for data-based PHM for power modules. Patil [56] demonstrated a prognostic framework for IGBT devices which is shown in Figure 2.5. The on-state voltage $V_{CE(ON)}$ is used as a failure indicator for in-situ monitoring. A healthy data of $V_{CE(ON)}$ is used as training data to determine failure threshold value. The deviation of $V_{CE(ON)}$ from its healthy value during the aging test is estimated using the Mahalanobis Distance (MD) which measures the deviation of statistical data points from the center of the healthy data cluster. In order to isolate the effect of loading conditions, the measurement of $V_{CE(ON)}$ are made at a constant current and a constant temperature. The prognostic step is carried out based on Particle Filtering algorithm to predict the future time evolution of $V_{CE(ON)}$.

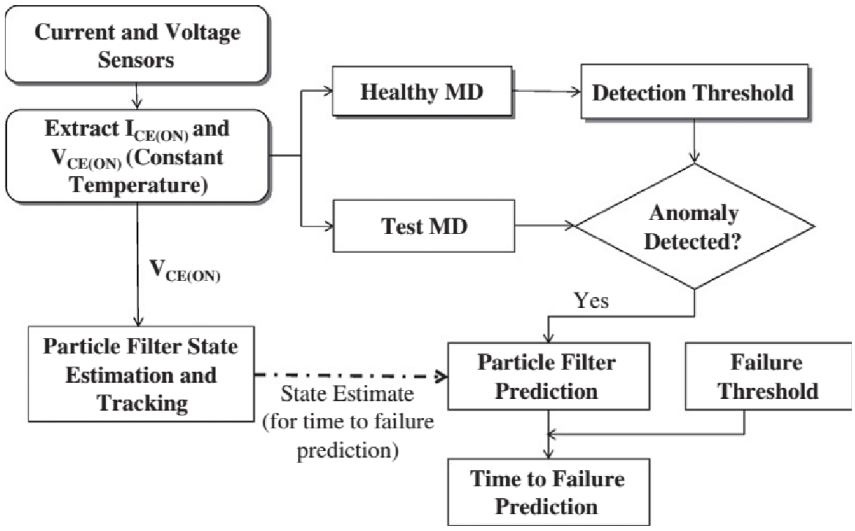


Figure 2.5 Prognostic framework of IGBT devices [56]

A similar framework is shown Figure 2.6. This framework is used in [57-59] to estimate the Remaining Useful Life (RUL) of IGBTs and MOSFETS. Different failure precursors are used such as current tail, threshold voltage and on-resistance. Oukaour et al [60] monitored $V_{CE(ON)}$ and T_J as failure precursors and constructed two classes of training data using the monitored variables. One class describes healthy IGBTs and another class describes aged IGBTs. Figure 2.7 shows the training data of the two classes and the discrimination boundary between aged and healthy data.

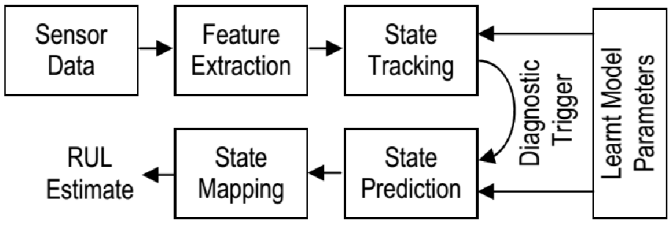


Figure 2.6 Prognostic framework of IGBT devices [57]

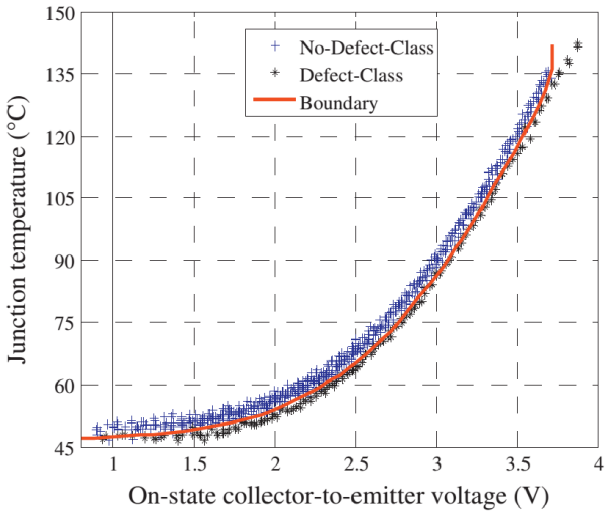


Figure 2.7 Healthy and aged data of $V_{CE(ON)}$ and T_J of IGBTs [60]

2.2.4Data-Model Fusion Methods

Recently, there has been increasing interest in Data-Model fusion techniques for PHM [51]. Fusion methods combine the benefits of both data-based and PoF-based methods and overcome some of their disadvantages. They make use of all available information of the power module such as failure precursors, loading profiles, failure models, material and geometrical information in order to provide more accurate lifetime estimate and reduce uncertainty boundaries. The field of information fusion has been recently recognized as an open research field [61].

Principally, data/knowledge fusion techniques can be applied at different levels of the PHM architecture. Roemer et al [62] defines three levels where fusion can be applied in a PHM framework as shown in Figure 2.8. Sensor fusion is the lowest level of fusion where outputs of multiple sensors are combined to improve the accuracy of extracted features of failures. The second level is features fusion where features extracted from the data of different sensors can be combined. The highest level is knowledge fusion where multiple lifetime estimates given from multiple methods such as PoF-based and data-based can be combined together.

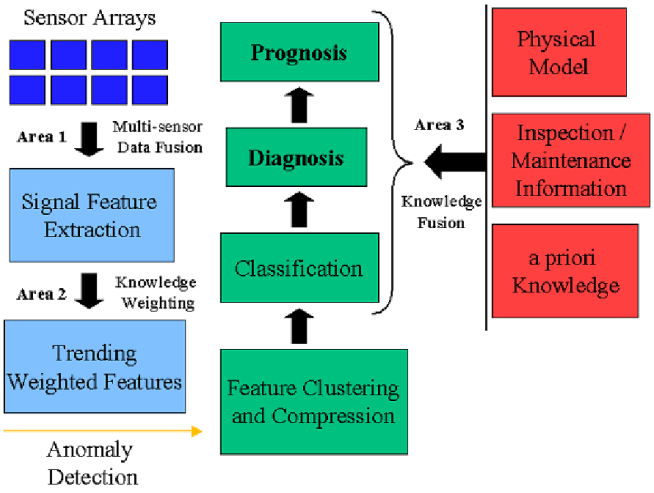


Figure 2.8 Fusion Application areas [62]

2.2.4.3Examples of Fusion PHM for Power Modules

Figure 2.9 shows a fusion PHM framework proposed by CALCE group [63]. Failure precursors are monitored in-situ and compared with a healthy baseline data in order to detect any trends in failure indicators. At the moment when failure threshold is exceeded an alarm is triggered indicating an imminent failure. Parameters which exhibit trends are identified and isolated in order to apply the prognostic step and calculate RUL. Those parameters can be related to different failure mechanisms, and therefore the appropriate PoF models can be chosen accordingly. The next step is to use the historical data of loading profiles to get a PoF- based RUL estimate utilizing the identified failure models. Finally, a knowledge fusion technique is used to aggregate the two RUL estimates.

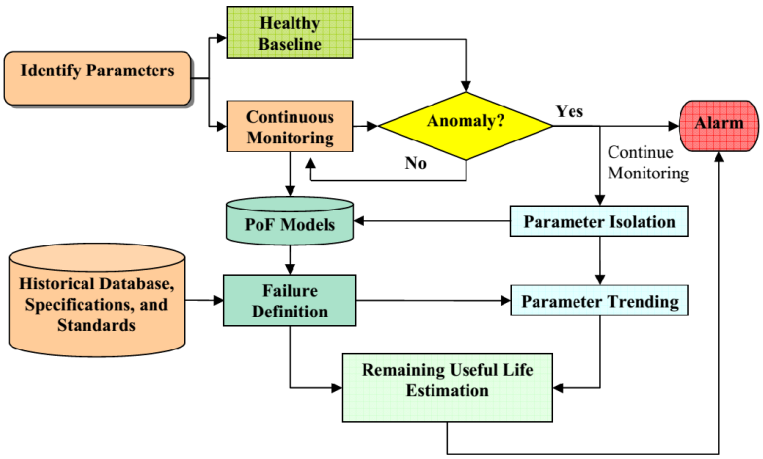


Figure 2.9 Fusion PHM methods proposed by CALCE [63]

Multiple techniques are tested in literature for knowledge fusion. Dempster-Shafer [64] and, fuzzy fusion and Transferable Belief Model [65] are all methods of knowledge fusion.

Guangfan [66] demonstrated the use of the Transferable Belief Model for the fusion of two RUL estimates given by two different prognostic algorithms. The targeted failure mechanism is solder joints fatigue under thermal loading. It is explained that the output of the fusion stage achieved higher accuracy in predicting the end-of-life of the component and the uncertainty of the resulting estimate is reduced. Similar results are observed by Goebel [67] who demonstrated the use of Dempster-Shafer method to aggregate RUL estimates given by a data-based and a PoF-based methods for crack propagation.

2.3 Condition Monitoring of IGBT Power modules

Condition monitoring provides a continuous monitoring and assessment of power module reliability in their work environment. It relies on real-time measurements to detect any deviation from healthy characteristics during normal operating conditions such that a maintenance action can be taken [6]. It ensures protection and safe operation of power converters.

Unlike lifetime estimation methods, condition monitoring methods are not intended in principle to give lifetime estimate of the monitored component. They focus on extracting the features of the failures from the real-time

measurements during the normal operation of power converters such that the loading conditions are isolated from the features of the failures. Condition monitoring methods can inform the prognostics stage by indicating ongoing failures and triggering the prognostics algorithm. In this section, methods of condition monitoring proposed for power modules are presented.

2.3.1Monitoring of Solder Fatigue

Dawei et al [68] proposed a method to detect solder fatigue in power modules. The proposed method is shown in Figure 2.10. It is based on thermal and power loss models to estimate the change in the thermal resistance of the heat flow path due to solder fatigue. The change in the thermal resistance is estimated by comparing an online estimate of the power loss to the original power loss model. Power loss is estimated online using a thermal model and measurements of baseplate and ambient temperature. The difference between the estimated and the original baseline power loss is then used in an iterative algorithm to calculate the change in R_{th}.

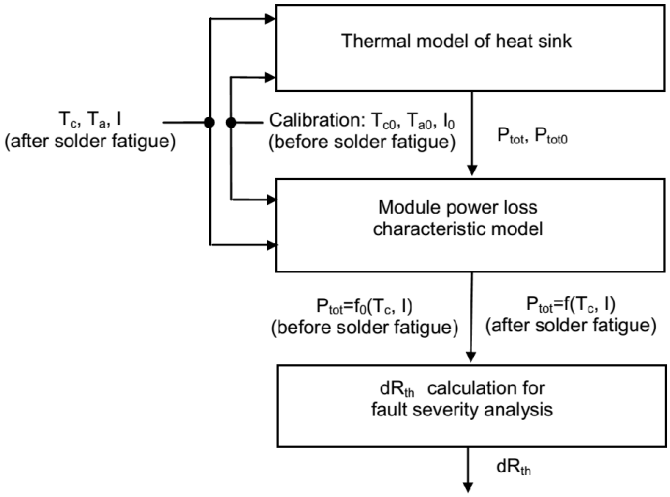


Figure 2.10 condition monitoring method proposed by Dawei [68].

In another work, Dawei et al [69] demonstrated the use of the output harmonics of the inverter in order to detect the degradation of solder layers. It is explained that the amplitude of the harmonics is correlated to the temperature and therefore the change in temperature due to solder fatigue can be detected. This method implements a two loop control strategy. The inner loop is used to excite specific harmonics in the output whereas an outer loop is

used to suppress the excited harmonics. The control signal of the outer loop is used as indicator of solder fatigue. This method is shown in Figure 2.11.

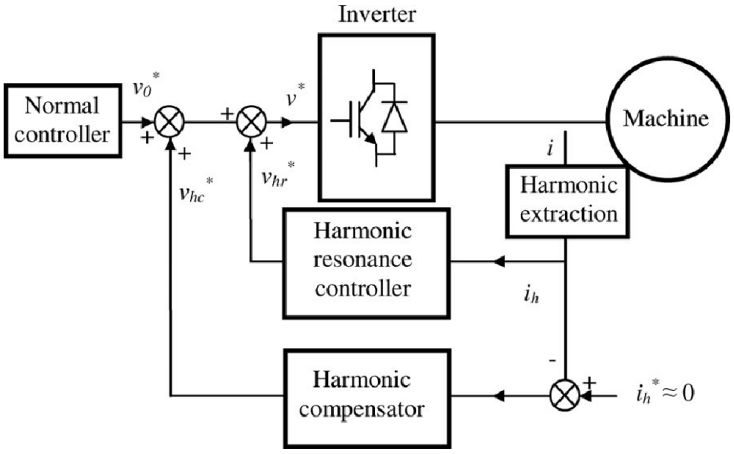


Figure 2.11 Controller Structure for harmonic resonance and compensation [69]

The algorithm of Principal Component Analysis (PCA) is demonstrated by Anderson et al [70] for the detection of solder fatigue in IGBT. In this method, the on-state voltage $V_{CE(ON)}$, the current I_C and the case temperature T_C are monitored and used to extract a vector of features. Extracted features are then compared with a pre-determined healthy features and the difference between the two indicates the deviation from the healthy state of the thermal path. This is explained in Figure 2.12.

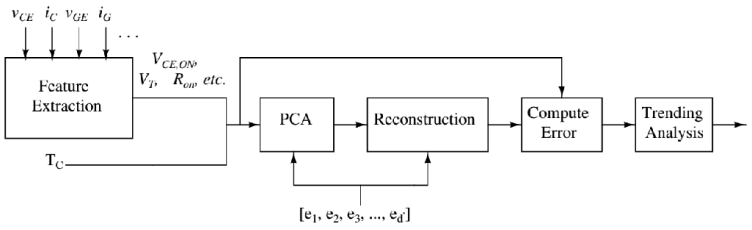


Figure 2.12 Condition Monitoring algorithm for IGBTs based on Principle Component Analysis [70].

Musallam [71] used a model estimate of junction temperature T_J of the IGBT for the purpose of solder fatigue detection. The model estimate is compared with a measurement of the junction temperature T_J obtained using an infrared camera. The model represents the healthy state of the thermal path and

so the difference between measurement and model estimate is used to assess the change in thermal resistance due to solder fatigue.

2.3.2Monitoring of Wire-bonds

A measurement system is proposed by Ji et al [72] to monitor the health state of wire-bonds in IGBT modules. The system shown in Figure 2.13 is proposed for traction applications. It works during the idle periods of normal operation. That is when the power converter is at rest and is not supplying energy to the motor. The system utilizes a relay network which is used to connect the tested IGBT to two current sources. A high current source is used for heating the IGBT and a low current source is used to measure the collector-emitter voltage V_{ce}. The on-state voltage $V_{CE(ON)}$ is measured and used to test the state of wire bonds. The measured $V_{CE(ON)}$ is compared with a healthy baseline of the forward characteristic $V_F=f(I,T_J)$ and the difference indicate a failure in the wire-bonds.

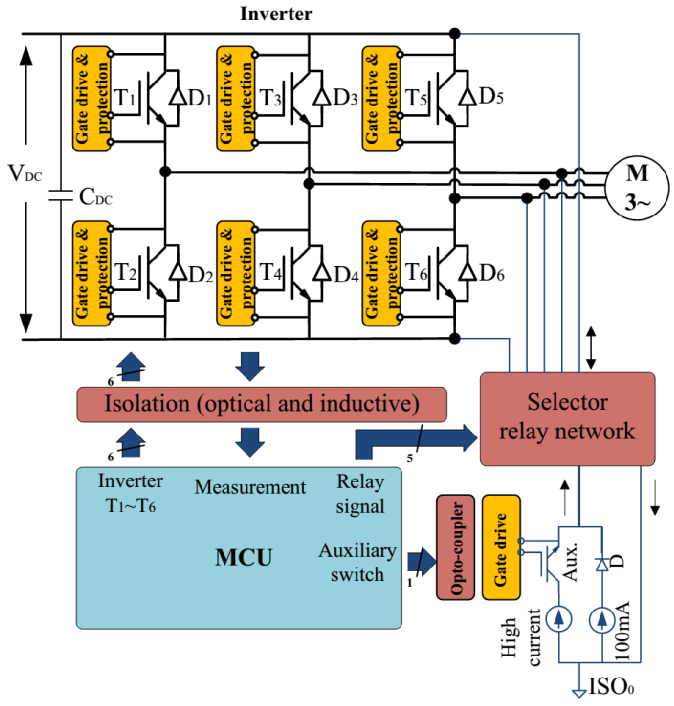


Figure 2.13 In-situ health monitoring system for power converter [72].

Lehmann et al [73] proposed a method for the detection of wire-bond lift-offs during normal operation of power modules. The method is shown in Figure 2.14. This method requires modification of the packaging. Additional sensing wires are bonded to the emitter contact on the chip. These additional

wire-bonds are connected to a resistor to increase current path impedance preventing high current from flowing through those wires. At the moment when wire-bonds are lost, the voltage difference between sense contact (S) and emitter contact (E) changes, indicating a wire-bond failure.

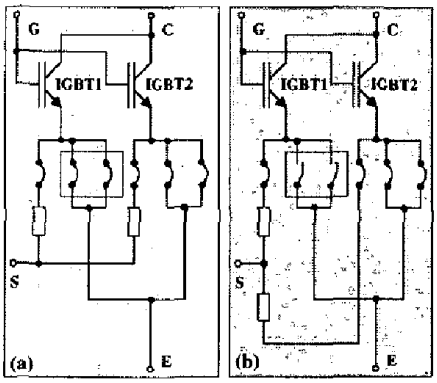


Figure 2.14 Lift-off detection method proposed by Lehmann [73]. (a) Circuit with no life-off (b) Circuit with Lift-off

2.4**Discussion**

The diverse applications of power electronics make reliability assessment of power modules a difficult task since reliability is dependent on the mission profile. Therefore, in-service PHM can be an efficient solution to provide an accurate assessment of the reliability of power modules in their actual applications. As a consequence, there is a drive towards the in-service application of prognostics and health management methods to monitor the reliability of power modules in the work environment. In addition, condition monitoring for power modules is gaining more interest from researchers. This is due to the need to achieve higher availability of the assets that use power converters and reduce the cost of maintaining those assets.

To date, most of the work on PHM of power modules described in the literature is demonstrated in a controlled environment (e.g. temperature and current) whereas in a real work environment such parameters vary continuously with many factors related to the loading demand and to the surrounding environment (e.g. current and ambient temperature). Therefore, many difficulties still face the practical application of in-service PHM.

Therefore, there is a need to establish practical methods to obtain online measurements of essential parameters (e.g. junction temperature and on-state voltage) that are used by the PHM approach. This problem was indicated as a limiting factor for the development of efficient PHM for power electronics [6]. For the data-based methods, care should be taken to achieve high accuracy measurements, which preserves the health information contained in the measurement. That is in addition to the need to eliminate the noise in the measurement and isolate the effects of loading conditions from the effects of failures. It is important as well to distinguish between competing failure mechanisms which can emerge simultaneously in the power module such as solder fatigue and wire-bond lift-off. That is because the dominant mechanism which leads to power module failure is dependent on the application and the mission profile.

It can be stated that junction temperature of power modules is an essential parameter since it drives the mechanical fatigue processes loading to the wear-out of the module. In addition, junction temperature has an effect over all the electrical parameters such as the on-state voltage $V_{CE(ON)}$ which can be used as failure indicators. Therefore, the knowledge of junction temperature is essential to extract the features of failures from the measurement of failure indicators. However, since junction temperature cannot be directly measured it has to be estimated.

Finally, the combination of models and measurement data can provide more information about the monitored power module. The incorporation of more information can lead to more accurate estimation of lifetime and more accurate estimation of degradation level. This is the working principle of the Data-Model fusion method discussed earlier. Based on that, the method proposed in this thesis integrates online measurement data and pre-calibrated models in order to infer health information and degradation levels. In addition, Kalman filter which is used in this thesis to estimate junction temperature can be viewed as a fusion method that incorporates measurement data and a pre-calibrated model to improve the accuracy of the junction temperature estimate. This reduces measurement noise and updates the model estimate by

measurements from the real system providing an estimate which is more accurate than each technique individually.

2.5**Summary**

In this chapter, the state-of-art approaches for prognostics and health monitoring of power modules were presented. The recent developments in the in-service PoF-based and Data-based methods were presented as well as Data-Model fusion methods. Condition monitoring for power modules were reviewed. Next chapter reviews the methods to estimate and measure junction temperature in power electronics modules.

Chapter 3 Background to Real-time Junction Temperature Estimation

3.1 Introduction

This chapter presents a background about the thermal modelling of IGBT power modules and available methods to measure junction temperature. Models used to represent the thermal path in power modules are presented. Obtaining junction temperature using integrated sensors, model-based methods and thermo-sensitive electrical parameters TSEPs are discussed. Then, online measurement methods for obtaining TSEPs for junction temperature estimation are considered.

3.2 Heat Conduction and Thermal Modelling in Power Semiconductor Modules

Heat transfer can take place by three different mechanisms: conduction, convection and radiation. Heat conduction is the transmission of energy in solid materials from high temperature side to low temperature side. This process is governed by Fourier's law of heat conduction. Convection, on the other hand, is the heat transfer between solids and adjacent fluids (e.g. air, water, oil, …). It has two forms: forced and natural. Forced convection is when the fluid motion is induced by external sources (e.g. fan, pump, …) whereas natural convection is when no external factor is affecting the fluid motion. Convection is roughly governed by Newton's law of cooling. At last, radiation is the heat transfer by electromagnetic radiation through vacuum and it is governed by Stefan-Boltzmann law of thermal radiation [74].

It is common in the field of power electronics to assume that the heat transfer happens only by conduction inside the power module [75]. For example, if the flow rate of the coolant at the convective interface of the heatsink is constant, the heat transfer will only be affected by the solid conductive materials. Therefore, convection and radiation can be neglected when the thermal stack of an IGBT power module is considered for modelling.

3.2.1 Heat Conduction Equation

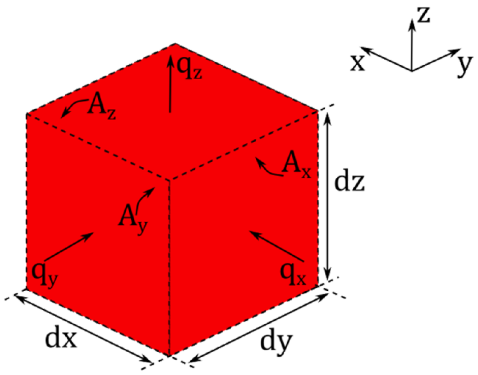


Figure 3.1 An element of homogeneous isotropic material of volume *dV*

Heat conduction equation is the differential equation whose solution gives the temperature distribution in a given medium over time. It can be derived from Fourier's law of heat conduction and the energy conservation principle. Considering the volumetric element of a homogeneous isotropic material of density ρ (kg/m^3) as shown in Figure 3.1, the element volume is $dV=dx.dy.dz$ and its mass is $dm=\rho.dV$, the heat conduction equation in a 3-dimentional space is given as:

$$\alpha\left(\frac{\partial^2 T}{\partial x^2}+\frac{\partial^2 T}{\partial y^2}+\frac{\partial^2 T}{\partial z^2}\right)=\frac{\partial T}{\partial t} \qquad \textbf{(3.1)}$$

where $\alpha=k/\rho c_p$ is called thermal diffusivity and it represents the ratio of the thermal conductivity k (W.m^{-1}.^{o}C^{-1}) to the specific heat capacity c_p (J.kg^{-1}.^{o}C^{-1}).

In order to simplify the solution of the thermal problem the heat spreading can be neglected by assuming surfaces of constant temperature (isotherms) in the direction of x such that the temperature of a single point is representative of the isotherm temperature. This is a common assumption in order to simplify heat transfer problems in power electronics modules [75]. Therefore, (3.1) can be simplified to a one-dimensional heat transfer equation:

$$\alpha\frac{\partial^2 T}{\partial x^2}=\frac{\partial T}{\partial t} \qquad \textbf{(3.2)}$$

The solution of this equation gives the temperature distribution along the one-dimensional x-axis overtime. The following section shows available solutions of this equation.

3.2.2 Solution of Heat Conduction Equation

Solutions for heat conduction problem in power electronics were proposed since the appearance of power semiconductors in the 1950s [76]. Mortenson [77] in 1957 showed analytically that the step response of the heat flow path of a power semiconductor device can be represented by an infinite summation of exponential terms. He assumed a one-dimensional rectangular heat flow path with a finite length and expressed the step response of the heat flow path by the following formula:

$$T_J(t) = T_a + PR_{th}\left(1 - \frac{8}{\pi}\sum_{n=1,3,\dots}^{\infty}\frac{e^{-t/\tau_n}}{n^2}\right) \qquad \textbf{(3.3)}$$

where T_a is the ambient temperature, P is the power dissipation, R_{th} is the thermal resistance of the heat flow path and τ_n is the time constant of the nth term.

This simplified solution was questioned by many researchers who have tried proposing more accurate solutions of the heat conduction problem. Zommer [78] for example, explained a different solution for a multi-layer structure of power semiconductor packages by solving the diffusion equation for all layers simultaneously with boundary conditions coupling adjacent layers. In another work, David [79] considered the heat spreading effect on the response of the heat flow path. He assumed a constant spreading angle of 45^o from the power dissipating element and derived an analytical solution for the resulting problem.

Analytical solutions of the heat diffusion equation can get very complicated for real world problems where packages are made of complex multi-layer structures and non-homogenous material. Therefore, to avoid the complexity of analytical solution of heat diffusion equation, Finite Element Analysis (FEA) simulation packages can be used to numerically solve heat diffusion equation. In addition, the use of an electrical equivalent to the

thermal problem is another solution to find the temperature using techniques of circuit analysis. This analogy eliminates the need to solve the heat diffusion equation and provides a computationally efficient method to model the thermal response of the heat flow path in power semiconductor packages.

3.2.3 Cauer Network Equivalent

Fourier's law has an analogy with Ohm's law which governs the current conduction in a conductive material. This analogy allows transforming the heat conduction problem into an electrical network which can be solved using a circuit simulator such as SPICE. This allows incorporation of the thermal model of the semiconductor package within the electrical simulator so that electro-thermal simulation can be achieved. Ohm's law can be expressed in the following form:

$$\vec{J} = -\sigma\left(\vec{\imath}\frac{dE}{dx} + \vec{\jmath}\frac{dE}{dy} + \vec{k}\frac{dE}{dz}\right) \quad \textbf{(3.4)}$$

where J is the current density (A.m^{-2}), σ is the conductivity and E is the electric field. The similarity between Ohm's and Fourier laws encourages the comparison between the differential equation in (3.2) and the differential equation that governs an electrical transmission line which can be expressed by the following differential equation assuming zero inductance and zero conductance:

$$\frac{\partial^2 u}{\partial x^2} = CR\frac{\partial u}{\partial t} \quad \textbf{(3.5)}$$

where du/dt (V) is the voltage gradient in the x direction, C is the distributed capacitance per meter (F/m), R is the distributed resistance per meter (Ω/m). The similarity between (3.2) and (3.5) suggests that the solutions of the two differential equations are similar. This analogy was first stated by Newell [80] who represented the heat conduction path by a uniform electrical transmission line using basic RC circuits blocks.

Therefore, the heat conduction path can be modelled by an electrical transmission line as shown in Figure 3.2. In this electrical equivalent model, the electrical resistances R_i and the electrical capacitances C_i represent the thermal resistances and the thermal capacitances of the heat conduction path.

This model is commonly called a Cauer network or ladder network. The analogy between electrical and thermal terms is detailed in Table 3.1.

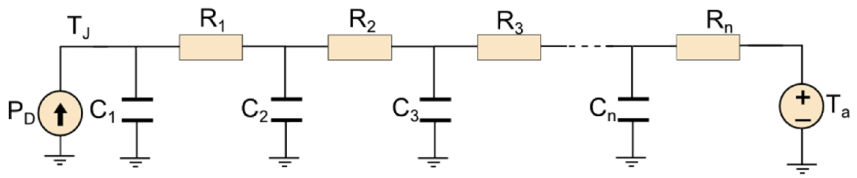


Figure 3.2 Cauer Model of thermal impedance

Table 3.1Electrical Analogy of Thermal Systems

Electrical		Thermal	
Current Density (A/m^2)	J	Heat Flux (W/m^2)	q
Current (Amp)	$I = JA$	Heat Flow Rate (Watt)	$P = qA$
Resistance (V/A)	$R_e = {}^{l}/_{\sigma A}$	Resistance ($^oC/W$)	$R_{th} = {}^{l}/_{\lambda A}$
Voltage (V)	$\Delta V = RI$	Temperature (^oC)	$\Delta T = R_{th}P$
Capacitance (As/V)	$C = {}^{\varepsilon A}/_{l}$	Capacitance ($Ws/^oC$)	$C_{th} = c\rho lA$
σ (S/m) is the electrical conductivity of the material **ε** (A.s/V.m)is the permittivity of the dielectric material **c** (J/kg.^{o}C) is the specific heat of the material **ρ** (kg/m^3) is the density of the material			

Newell [80] defined the thermal step response as being equivalent to the transfer function of the transmission line which relates the input voltage (temperature) to the input current (thermal power). This step response function (or thermal impedance function) describes temperature rise relative to a chosen reference temperature and it is realized by the continued fraction expansion:

$$Z_{th}(s) = \frac{\Delta T_J(s)}{P_D(s)} = \cfrac{1}{sC_1 + \cfrac{1}{R_1 + \cfrac{1}{sC_2 + \cdots + \cfrac{1}{R_n}}}} \qquad \textbf{(3.6)}$$

The Cauer network equivalent model has two advantages. It preserves the physical meaning of thermal resistance and thermal capacitances where the internal circuit nodes can theoretically be correlated to internal locations within the modelled heat conduction path. This is explained by the fact that a current pulse applied to the input of a Cauer network charges up the capacitors in sequence since they are all referenced to a common ground. This behaviour is in physical correlation with the heat diffusion phenomenon in solid structures where heat propagates from one isotherm to the next in the direction of decreasing temperature. Therefore, a Cauer network is considered a physical model of the thermal diffusion path.

The other advantage is that the Cauer network allows the power semiconductor package and the heatsink to be modelled separately and then combined to obtain an extended thermal model which describes the thermal path from junction-to-ambient [81].

However, one major disadvantage of the Cauer network model is the parameterization of the network which can be a difficult process and it suffers inaccuracies due to the heat spreading effect. Cauer network parameterization can be done following the procedure presented by Newell [80] where the values of thermal resistances R_θ and time constants τ_θ of the thermal path layers can be determined from material properties and geometrical information of the structure:

$$\tau_\theta = \frac{\pi}{4}\frac{\rho c}{k} l^2 = \frac{\pi}{4} R_\theta C_\theta, \qquad R_\theta = \frac{1}{A}\left(\frac{\pi}{4}\frac{\tau_\theta}{k\rho c}\right)^{1/2} \qquad \textbf{(3.7)}$$

where ρ (Kg/mm^3) is the material density, c (W.s/Kg.^{o}C) is the material specific heat, k (W/mm.^{o}C) is the thermal conductivity, l (mm) is the thickness of the layer and A (mm^2) is the cross sectional area. Formula (3.7) assumes a rectangular structure and ignores the effect of heat spreading which reduces the accuracy of the resulting model for many geometries where heat spreading is significant by design.

To take heat spreading into account, Newell [80] suggested a correcting factor to be used when parameterizing the network. This was later investigated by Masana [82, 83] who proposed in two consecutive works a "Variable Angle Method (VAM)" to calculate thermal resistances R_θ and thermal capacitances C_θ.

However, material and geometric information may not be available for the users of power semiconductor packages and they are usually not provided in datasheets. Therefore, other methods are proposed to determine the parameters of the Cauer model from experimental measurements of the transient thermal impedance.

Szekely [84] proposed a method which starts from the thermal impedance measurement to work out by deconvolution a "time-constant spectrum" which is principally the impulse response of the thermal diffusion path. The "time-constant spectrum" describes the time constants of the thermal path and their corresponding thermal resistances. A Foster network (described in Section 3.2.4) is then obtained by discretizing the "time-constant spectrum" then circuit transformation techniques [85] are used to obtain the parameters of the Cauer network.

Bagnoli [86, 87] introduced a similar method called "Transient Resistance Analysis by Induced Transients (TRAIT)" to identify the Cauer network parameters. The thermal impedance measurement is analysed into a set of time constants τ_i and their corresponding thermal resistances R_i using an algorithm called "Blomer-Pade method" which operates on exponential decay curves, similar to the thermal impedance curves. After R_i and τ_i are obtained a continued fraction expansion procedure is performed to calculate the Cauer network components values.

Skibinski [88] introduced a method based on utilizing Recursive Least Squares (RLS) and "Time Decoupled Theory" to extract the parameters of the Cauer model from experimental data. Due to the nature of power semiconductor packages, thermal time constants tend to be widely scattered over time axis resulting in slow and fast modes of the thermal system. Therefore, a dedicated excitation signal is designed to identify the slow modes

and the fast modes of the system separately in a two-steps procedure based on the principles of system identification theory. Two separate models are identified and then combined to form the final Cauer network model.

From the above, it can be concluded that the parameterization of a Cauer network is not a straightforward process. Therefore, there is a tendency to use a behavioural model which can help to avoid the complications of identifying a physical model. A behavioural model is an acceptable solution in cases where the interest is limited to the knowledge of the temperature at a specific location in the thermal path regardless of the internal temperature distribution along that path. This can be achieved by a black-box model that describes the step response of the thermal conduction path. This model can be obtained from experimental measurement of thermal impedance and is commonly called a Foster network equivalent model.

3.2.4 Foster Network Equivalent

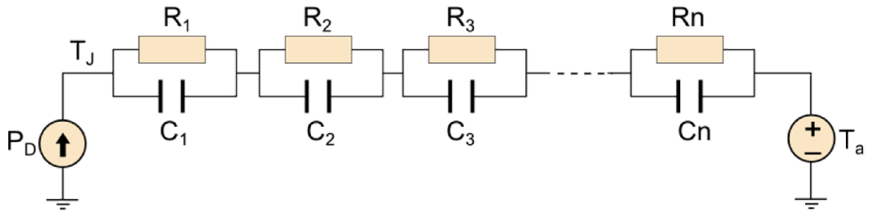


Figure 3.3 Foster Model of Thermal Impedance

In 1959, Strickland [89] demonstrated the possibility of using a Foster network as an electrical equivalent to describe the thermal impedance of power semiconductor package. Foster network shown in Figure 3.3 is a series connection of RC pairs. The step response of a Foster network can be described mathematically by a sum of exponential terms. The time step response of the electrical equivalent network shown in Figure 3.3 is expressed by:

$$Z_{\theta ja}(t) = \sum_{i=1}^{n} R_i(1 - e^{t/\tau_i}) \qquad \textbf{(3.8)}$$

where R_i is the thermal resistance of the ith term, τ_i is the time constant of ith term and n is the number of terms.

In contrast to a Cauer network, a Foster network is considered as a black-box model and has no physical correlation to the thermal diffusion path because all capacitors in Foster network start charging instantaneously in response to a power pulse applied at the input. This results in the development of an instantaneous voltage at the internal circuit nodes. And since voltage is analogous to temperature as described earlier, this means that the temperature of the internal nodes changes instantaneously in response to a power pulse. This disagrees with the physical process of heat diffusion. Therefore, the Foster network is considered to be a behavioural model that can be used to describe the step response of a thermal conduction path at a specific location relative to a reference temperature. And hence, Foster network can represent the thermal response of any thermal path regardless of its geometry.

In addition to its physical insignificance, the Foster network model describes the "temperature rise" from a constant reference temperature (e.g. case temperature or ambient temperature). Therefore if the reference temperature is variable with time, the model becomes invalid. Moreover, a Foster network model cannot be partitioned and combined as is the case with Cauer model. Instead, a characterization of the complete setup of the power semiconductor package and its heat sink should be done to generate a Foster model.

An important advantage of the Foster model is the decoupled nature of its RC components which simplifies its numerical solution and allows computationally efficient thermal models to be obtained directly from experimental measurement of thermal impedance. This can be seen by the Laplace transformation of (3.8) which shows that the thermal impedance can be expressed by a partial fraction expansion:

$$Z_{th}(s) = \frac{\frac{1}{C_1}}{s + \frac{1}{R_1 C_1}} + \frac{\frac{1}{C_2}}{s + \frac{1}{R_2 C_2}} + \cdots + \frac{\frac{1}{C_n}}{s + \frac{1}{R_n C_n}} \qquad \textbf{(3.9)}$$

For the purpose of this work, the time behaviour of the junction temperature of an IGBT power module is required regardless of the internal temperature distribution in the thermal stack of the power module. Therefore, a

Foster network equivalent is considered to model the thermal response of the IGBT power module.

3.2.5Summary

This section reviewed the heat conduction problem in power electronics modules and the available solutions for the heat conduction equation. The Cauer network is a physical model of the heat conduction path but parameterizing the model is problematic. On the other hand, the Foster network is a behavioural model and has no physical significance, but its parameterization is easier and therefore it will be adopted in the thermal modelling reported in this thesis.

3.3**Methods of Measurement and Estimation of Temperature in IGBT Power Modules**

3.3.1Integrated Sensors

One way to obtain an online measurement of IGBT temperature is via integrated sensors. Two types of sensors are typically integrated into power modules, Negative Temperature Coefficient (NTC) resistors and on-chip diodes. While NTC resistors shown in Figure 3.4 are mounted on the DBC substrate and return the baseplate temperature with a time constant in the range of few seconds [90], on-chip diodes are integrated within the IGBT chip itself as shown in Figure 3.5 and return the local chip temperature with a time constant of about 1ms [91]. Both types require special consideration during the design of the package and manufacturing process to ensure electrical isolation from high voltage copper traces on the substrate and require separate copper traces and external pins which might increase manufacturing cost and give rise to new reliability issues.

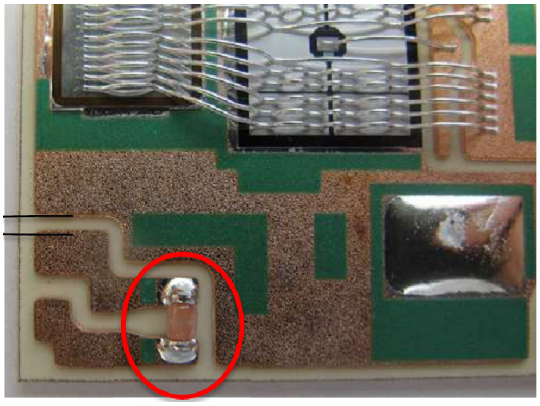


Figure 3.4 NTC integrated sensor for SKiM IGBT modules [90]

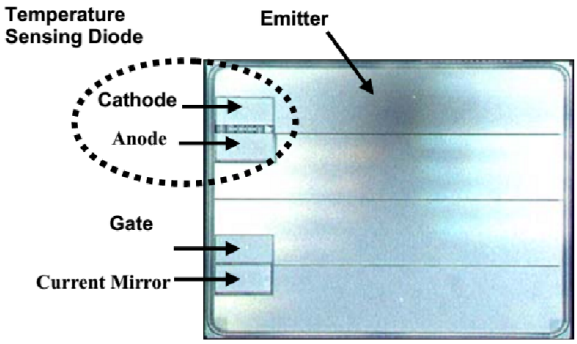


Figure 3.5 Integrated diode in the polysilicon of an IGBT chip for temperature sensing [92]

Normally, NTC integrated sensors provide the temperature of the baseplate at the location it is mounted. A thermal RC network can then be used to calculate the junction temperature of the semiconductor chip [93]. However, integrated sensors return the local temperature at a specific location on the substrate. Therefore, they might not be affected by thermal degradation caused by solder fatigue at die-attach layer and substrate solder layer which can increase chip temperature. And conequently, depending on the location of the integrated sensor, an increment of temperature may not be seen by the NTC sensor.

Many manufacturers are now considering adding integrated thermal sensors into their recent designs of IGBT modules, such as Infineon [91], Semikron [90], Mitsubishi [92]. However, the cost of those new technologies can be a limiting factor to be widly considered in some applications. Therefore, alternative methods can be used such as model-based estimates which can provide juntion temperature information.

3.3.2Model-based Estimate

In the absence of a direct measurement of IGBT junction temperature, thermal models can provide a simple and efficient way to obtain junction temperature information for IGBT modules. The electrical equivalent model of the thermal conduction path can be used to estimate junction temperature in real-time [94]. However, even with accurate pre-characterisation of the junction-to-case thermal impedance Z_{thjc}, large uncertainties in the thermal interfacing and heat sink variations reduce the accuracy and applicability of those models [95]. Therefore, thermal characterization of the complete thermal path, which can be obtained by measuring junction-to-ambient thermal impedance Z_{thja}, is often needed to achieve more accurate models. Furthermore, these models are generally defined under known boundary condition of a constant ambient temperature and heat transfer coefficient. Any variations in the ambient temperature, fan speed or flow rate result in a variation in the heat transfer coefficient and consequently varies the thermal resistance of the heat sink [96] which may result in errors in the estimated temperature.

One solution for this issue is a multi-model approach which considers the effect of variable cooling on the thermal impedance by generating multiple models for multiple cooling rates [97]. This procedure complicates the modelling process and still cannot cope with degradation of the thermal path. The increment of thermal resistance due to thermal path degradation by solder fatigue cannot be detected by the multi-model approach. And hence, temperature estimates will not be affected by thermal degradation on the longterm.

Solder degradation resulting from power modules aging reduces model validity over time since thermal resistance increases with gradual degradation of the thermal path [98]. Therefore, adaptive thermal models were proposed to quantify the change in the thermal resistance and update model parameters accordingly. Huifeng [99] presented a method to update the parameters of the Foster network by calculating the change in the thermal resistance resulting from aging effects. A measurement of T_J is obtained periodically by measuring

threshold voltage V_{th} which is a thermo-sensitive electrical parameter. The change in the thermal resistance is then calculated as:

$$R_{i(aged)} = R_i(1 + \frac{T_{j(measured)} - T_{j(estimated)}}{PR_{total}}) \quad \textbf{(3.10)}$$

where P is the power dissipation, R_{total} is the original total thermal resistance and R_i is the current value of thermal resistance before the update. However, this method requires modification of gate drive to allow the functionality of extending the turn-on time of the IGBT to allow the measurement of threshold voltage V_{th} to be made, a feature which is undesirable in practical applications.

Ze[100] proposed a different method based on the "Effective Heat Propagation Path (EHPP)" by observing temperature nonuniformity at the baseplate using thermocouples. It is argued that the temperature distribution at the case changes with solder fatigue at internal layers as a result of a change in the heat-spreading effect. A correlation between this change in the nonuniformity and the heat-spreading angle can be made and used to update the parameters of the Foster network. This method is shown in Figure 3.6.

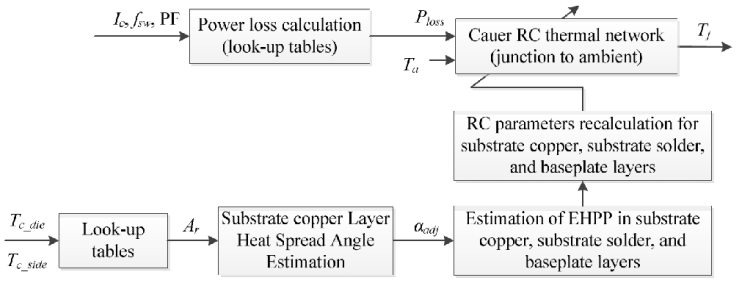


Figure 3.6 The adaptive thermal model proposed by Ze[100]

This method is intrusive and requires temperature sensors positioned on the baseplate to detect the change of temperature nonuniformity and therefore it is highly sensitive to the locations of those sensors. In addition, the number of required sensors can be large for high power multi-chip modules in order to cover the whole area beneath the module.

3.3.3Thermo-Sensitive Electrical Parameters (TSEPs)

Thermo-Sensitive Electrical Parameters are parameters which characterize the electrical performance of an IGBT such as on-state voltage $V_{CE(ON)}$, gate threshold voltage V_{th}, gate resistance R_G, turn-on and turn-off

timing. Those parameters show variations with chip temperature. Therefore, they allow the semiconductor chip itself to be used as a temperature sensor. And consequently, they can provide up-to-date information about the real temperature of the IGBT chip.

TSEPs have been used for thermal characterization of power modules for a long time. Forward voltage drop of IGBTs, diodes and some other devices has a linear correlation with chip temperature at low current which encouraged its use as a means to measure the thermal impedance of power modules. Other parameters such as threshold voltage V_{th} and on-resistance R_{ON} are used for the same purpose [101].

The use of TSEPs to measure junction temperature during the normal operation of power converters has been limited due to many difficulties, specifically:

- Low sensitivity of those TSEPs to T_J which is of an order of mV/^oC
- TSEPs dependency on operating conditions of power converters which complicates resolving T_J information (e.g. $V_{CE(ON)}$ varies with current)
- The lack of a flexible data acquisition platform that achieves the measurement on the power converter and sends it through the isolation barrier to the processing endpoint.
- The noisy working environment of power converters which is characterized by high voltage, high current, and electromagnetic fields make an accurate online measurement of TSEPs a challenging task.
- Measurement inaccuracies can originate from the high common-mode noise, switching and modulation signals and the EMI of the working environment.

Those factors can increase measurement errors and consequently affect the accuracy of the resolved T_J [102]. Moreover, some TSEPs are affected by the progressive degradation of power modules. For example, on-state voltage

$V_{CE(ON)}$ which is a TSEP is affected by wire-bond lift-off. This can lead to large errors in the resolved T_J from $V_{CE(ON)}$ when wire-bonds are lifted.

Multiple studies have investigated TSEPs in details [103, 104]. Avenas et al [105] investigated multiple electrical parameters for the purpose of estimating junction temperature. He compared $V_{CE(ON)}$ at high current, $V_{CE(ON)}$ at low current, threshold voltage V_{th}, gate-emitter voltage V_{ge}, saturation current I_{sat}, and switching times. He concluded that $V_{CE(ON)}$ at low current is the most suitable TSEP due to its linearity and high sensitivity while its feasibility for online measurement is limited. Whereas switching times and $V_{CE(ON)}$ at high current have better online measurability on the expense of lower sensitivity. Kuhn [106] studied turn-on delay time t_{don}, turn-off time t_{off} and di/dt. He found that t_{don} and t_{off} are better in terms of linearity and current dependency than di/dt which makes them better candidates for online measurement of T_J.

A linear correlation of the TSEP with temperature is desirable as it means a constant sensitivity to temperature and makes translating the TSEP measurement into T_J easier. On the other hand, a nonlinear relationship to temperature can result in a variable sensitivity of the TSEP to temperature where the sensitivity can be lower for some operating points compared to others. It can even go to zero at some points as it is the case with $V_{CE(ON)}$.

3.3.4 Summary

This section looked at available methods for obtaining junction temperature of an IGBT power module. Among the reviewed methods, the approach of Thermo-Sensitive Electrical Parameters (TSEPs) is of interest for the purpose of this work. That is because they use the semiconductor chip itself as a sensor and hence they provide up-to-date information about the current state of the IGBT chip in terms of temperature and health state (wire-bonds and thermal stack state). This information is a requirement for achieving a real-time health monitoring of the IGBT modules. Therefore, the next section will look at the methods of the online measurement of TSEPs.

3.4 Online Measurement Methods of Thermo-Sensitive Electrical Parameters TSEPs

3.4.1 On-state Voltage $V_{CE(ON)}$

Multiple techniques are proposed to measure forward voltage drop during normal operation of power converters at low and high current to estimate junction temperature. Rashed et al [107] proposed a modified control strategy to enable the measurement of V_{CE} at low current. The normal operation of the power converter is interrupted for few switching cycles to allow injecting a calibrated low current (100mA) through the required IGBT and acquiring the measurement of V_{CE}. This measurement is averaged and translated into junction temperature using a pre-calibrated relationship $T_J=f(V_{CE})$. The interruption of switching cycles distorts the sinusoidal output current. However, as stated by Rashed [107] this approach is proposed only for lab testing and is not suitable for power converters in field operation.

The measurement of $V_{CE(ON)}$ at high current can be made using the desaturation circuit. It is essentially used in gate drives to achieve protection against short circuit events. This circuit checks the value of $V_{CE(ON)}$ during the on-state of the IGBT and trips the gate drive when the measured $V_{CE(ON)}$ is higher than a pre-defined value. This is achieved using the desaturation diode which blocks the high voltage when the IGBT is off whereas it opens when the IGBT is conducting to allow measuring $V_{CE(ON)}$. However, the measured voltage is the sum of $V_{CE(ON)}$ and the forward voltage drop of the desaturation diode.

To eliminate diode forward voltage drop from the measured voltage Ghimire [108] proposed a modification to the desaturation circuit. The modified circuit is shown in Figure 3.7. The voltage drop of the desaturation diode D1 is subtracted from the measured voltage using a diode D2 identical to the desaturation voltage D1. Both diodes are contained in a single package which reduces differences between their voltage drops due to temperature and fabrication variability. Therefore it can be assumed that the forward voltage drops of the diodes are similar ($V_{D1}=V_{D2}$). The diodes D1 and D2 are connected in series and biased using a current source I_B. Therefore, the output

voltage of the circuit when the IGBT is ON is $V_{CE}=2V_b-V_a$ where $V_{CE}=V_b-V_{D1}$ and $V_a=V_{D1}+V_b$ assuming $V_{D1}=V_{D2}$.Whereas when IGBT is blocking the diode D1 blocks the high voltage.

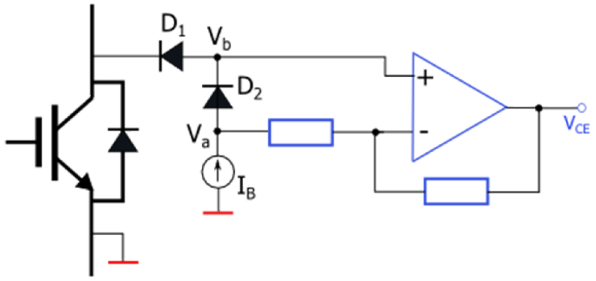
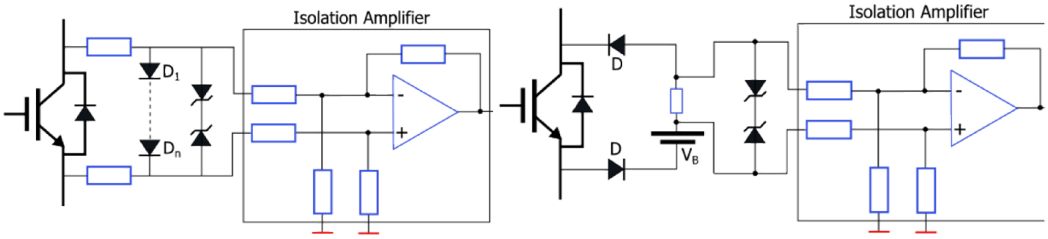


Figure 3.7 The modified desaturation circuit to enable the measurement of V_{CE} [108]

Kim [109] proposed two solutions to measure V_{CE} for medium and high DC voltage applications. Figure 3.8(a) shows the circuit for medium voltages. When the IGBT is blocking the diodes D_1 to D_n are forward biased clipping the input voltage to the amplifier hence the output voltage is $V_o=n*V_D$. An additional clipping stage uses zener diodes for protection against fast voltage transients. Whereas when the IGBT is conducting $V_o=V_{CE}$. For high voltages, the conduction current of the diodes D_1-D_n becomes too high. Therefore, the circuit in Figure 3.8(b) is used. In this circuit, when the IGBT is conducting $V_o=(V_B-2V_D)-V_{CE(ON)}$ while D blocks high DC voltage when the IGBT is OFF. And in this case the circuit becomes similar to the desaturation circuit explained earlier as it is required to remove the voltage drop of the diode D and the biasing voltage source V_B from the measured voltage V_o.



(a)For medium V_{CE} (0-600)V (b) For high V_{CE} (600-2000)V

Figure 3.8 V_{CE} online measurement circuits proposed by Kim[109]

3.4.2 Gate Threshold Voltage V_{th}

Because of its relatively high sensitivity, linear correlation to temperature and independence of current, threshold voltage V_{th} can provide a simple and accurate sensor for junction temperature. However, these good temperature characteristics of V_{th} come at the expense of measurement ease. The fast switching characteristic of power semiconductors prevents the accurate sampling of the dynamic V_{ge} signal when V_{ge}=V_{th} using common Sample-and-Hold circuits. Therefore, it is difficult to achieve online measurement of V_{th}.

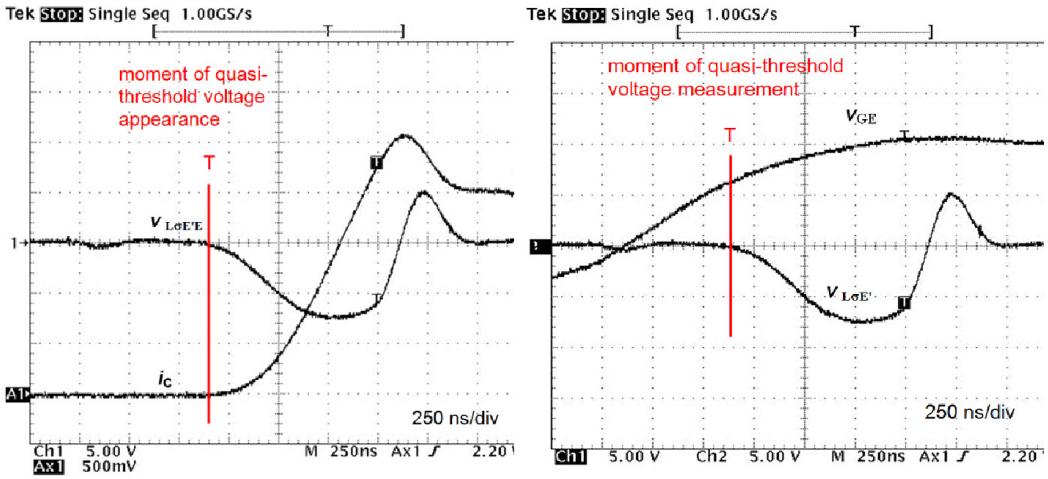
In order to overcome this problem, Chen [110] proposed a method to measure V_{th} in real-time using the turn-on delay time. A large gate resistor is switched in during the measurement interval to slow down the turn-on switching of a MOSFET device. The turn-on delay time t_{don} between the rise of V_{GE} and the rise of current is measured using a digital counter. The normal gate resistor is switched back by the end of the measurement cycle. Threshold voltage V_{th} is then calculated from the measured t_{don} using the formula:

$$V_{th} = V_{GG}\left(1 - e^{\frac{t_{don}}{R_g C_{iss}}}\right) \qquad \textbf{(3.11)}$$

where V_{GG} is the gate driving voltage, R_g is the gate resistance and C_{iss} is the input capacitance of the MOSFET device. Junction temperature can then be resolved from the calculated V_{th}. The measurement of t_{don} is made periodically every specific number of switching cycles. That is to minimize the disturbances to converter operation where the power loss during the measurement cycle is larger due to the larger gate resistance used during the measurement cycle.

Bahun et al [111] proposed a different method which enables the measurement of V_{th} without disturbing the switching cycles of the power converter. The proposed method utilizes a high speed analogue comparator and a DSP to sample V_{th}. The parasitic inductance between Kelvin emitter and the main emitter terminals of the power module is used to trigger the sampling of V_{th}. A voltage proportional to di/dt develops across this parasitic inductance during current rise. The gate-emitter voltage V_{ge} at that instant is assumed to be

equal to the threshold voltage V_{th}. This is described in Figure 3.9 . It is stated by Bahun et al [111], that the online measurement of V_{th} is found to be higher than the lab measured value but all the characteristic of linearity to temperature and independence of loading current are preserved. With proper calibration of the measured V_{th} with junction temperature T_J an estimate of T_J can be produced.



(a) Collector current i_c and parasitic inductance voltage.

(b) Parasitic inductance voltage and IGBT gate voltage V_{ge}. T indicates the moment of V_{th} sampling

Figure 3.9 operating waveforms showing V_{th} measurement method [111]

3.4.3 Switching Waveforms

The switching waveforms of i_c, v_{ge} and v_{ce} of the IGBT during turn-on and turn-off are correlated to temperature. This correlation allows using parameters of the switching waveforms to measure junction temperature T_J. Sundaramoorthy et al [112] demonstrated the use of Miller Plateau of the V_{ge} waveform during IGBT turn-off to measure junction temperature. Figure 3.10 explains the measurement method of Miller Plateau. The time difference between Trigger 1 and Trigger 2 is measured using a digital counter. A measurement circuit is developed to realize this measurement. This time difference is used as a TSEP to measure junction temperature. The change in the width of the Miller Plateau is caused by the lifetime of minority carriers which increases with temperature [113] which slows down the turn-off process and creates a current tail which is a common characteristic of IGBT devices.

Nonetheless, it is explained by Sundaramoorthy et al [112] that the width of Miller Plateau is also affected by current and DC link voltage which complicates the calibration process and consequently complicates the resolution of T_J. Another difficulty is the accurate measurement of the time difference between the two triggers, typically to the accuracy of 1ns/count.

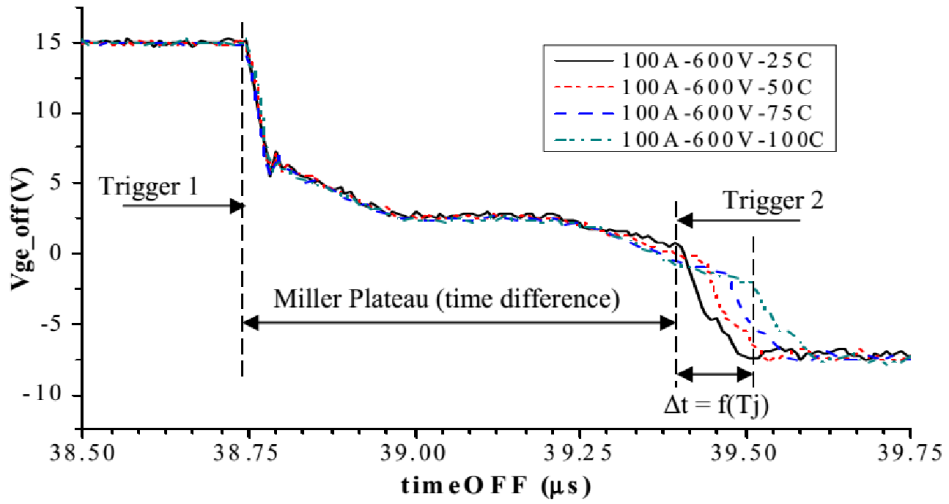


Figure 3.10 the difference in Miller Plateau wifth of V_{ge} during IGBT turn-off at different temperatures [112]

In another work, Sundaramoorthy et al [114] demonstrated the use of the maximum di/dt as TSEP. This value can be measured using the parasitic inductance between the main emitter and the kelvin emitter in a power module. This voltage is proportional to the di/dt where the peak value of this voltage can determine the maximum di/dt. The correlation of the di/dt with temperature is shown in Figure 3.11. A measurement circuit is proposed by Sundaramoorthy to enable the real-time measurement of $(di/dt)_{max}$.

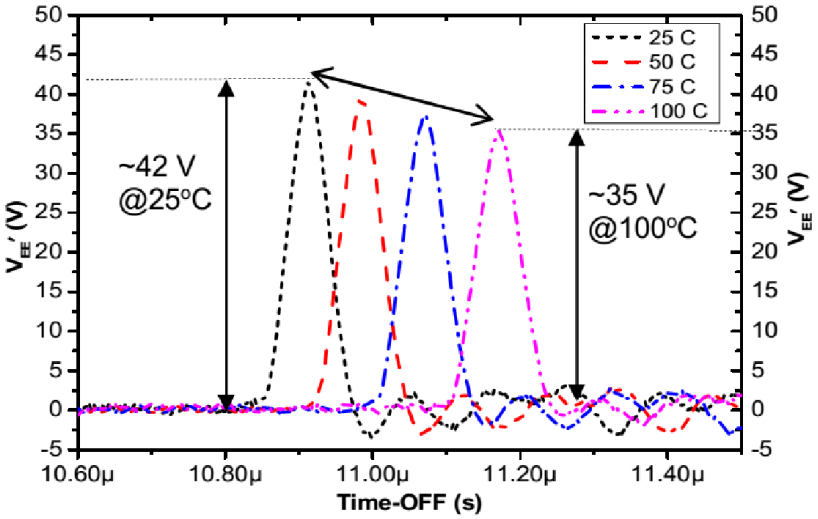


Figure 3.11 The change of the maximum of di/dt measured across the parasitic inductance of IGBT module at multiple temperature[114]

Bryant et al [115] investigated the correlation of dv/dt of the collector-emitter voltage V_{ce} during the IGBT turn-off to temperature. He found that the sensitivity can be very small (~0.5ns/°C) which makes it difficult for dv/dt to be used as a TSEP. But in another work [116], he demonstrates that the effect of dv/dt on the output harmonics is correlated to temperature and consequently the output harmonics can be used to measure junction temperature.

3.4.4 Internal Gate Resistance R_{Gint}

The internal gate resistance R_{Gint} of the IGBT chip which emerges from the device gate structure (oxide, polysilicon, …) increases with temperature. It is inversely proportional to mobility carriers which decrease with temperature. R_{Gint} is a part of the gate circuit of the IGBT through which the gate capacitance charges and discharges. Brekel [117] proposed a method to enable the measurement of R_{Gint} during power converter normal operation. The method is based on a modified substrate design for IGBT packaging. This is explained in Figure 3.12. An additional bond wire (F1-F2) is made on the chip to allow a constant current (I_0) to pass through R_{gint} and enable V_{GINT} measurement. This voltage drop V_{GINT} is proportional to R_{Gint} which in turn is proportional to T_J and hence the junction temperature can be measured.

However, the requirement for a special substrate design limits the applicability of this method and reliability concerns about the additional wire-

bonds need to be addressed as the lift-off of those wire-bonds will obstruct the measurement of V_{GINT} at the end-of-life period of the power module.

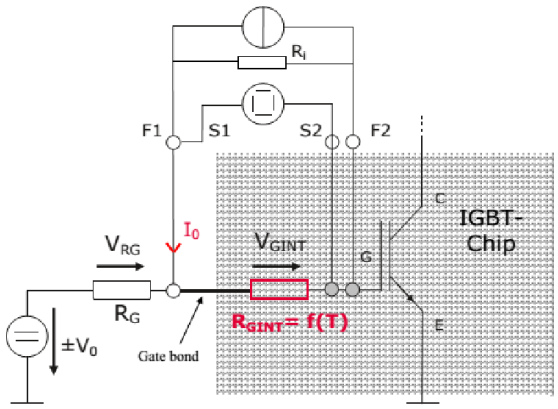


Figure 3.12 Principle circuit for R_{GINT} measurement with additional substrate contacts [117]

Another approach is proposed by Denk [118] who demonstrated the measurement of junction temperature by examining the effect of R_{Gint} on the frequency response of the RLC gate resonance circuit shown in Figure 3.13. The response amplitude of the RLC circuit at the resonance frequency changes with R_{Gi} and thus varies with temperature. A modified gate drive is proposed to superimpose a high frequency excitation signal on the negative gate voltage when IGBT is off. The response of the circuit is measured across the external gate resistance and the amplitude of the measured voltage is used as a TSEP.

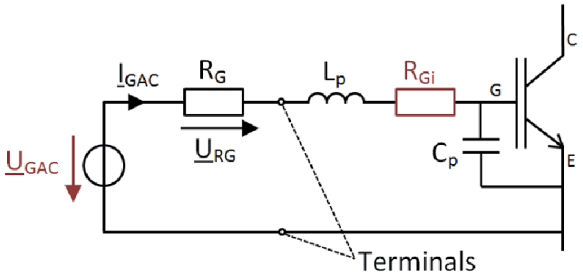


Figure 3.13 AC equivalent circuit of the IGBT driver and power module [118]

Baker et al [119] demonstrated a different method to measure junction temperature using R_{Gint}. When a positive voltage is applied to the gate during IGBT turn-on, the gate capacitance C_{ge} starts charging through the external gate resistance R_{gext} and the internal gate resistance R_{gint} as shown in Figure 3.14 (a). During the region when $V_{ge} \leq V_{th}$, the gate voltage V_{ge} is

influenced by the variation of R_{gint} with temperature. Therefore, V_{ge} voltage during this period can be used to estimate junction temperature. Baker developed a measurement circuit that integrates V_{ge} during the turn-on delay time as shown in Figure 3.14 (b) and used the voltage integral as a TSEP to estimate T_J.

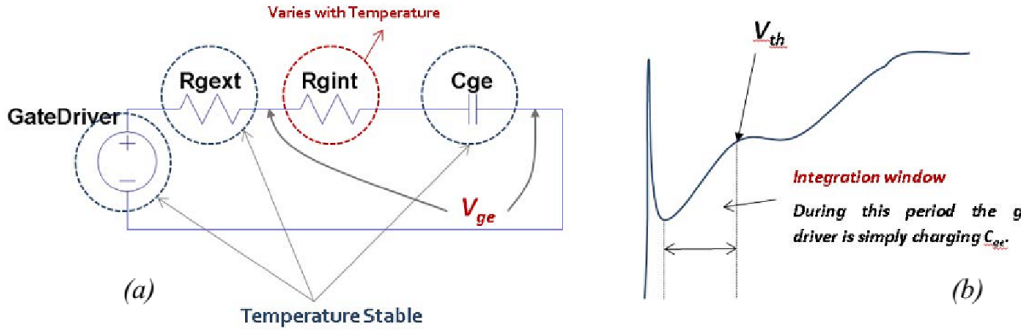


Figure 3.14 (a) Gate drive RC circuit. (b) Region of integrated gate voltage to produce measurement voltage [119].

3.4.5 Summary

This section reviewed the state-of-the-art online measurement methods of TSEPs. The importance of accuracy should be stressed when developing such circuits since the sensitivity of the measured parameters to temperature are generally small. It is important as well to be aware of the dependencies of the candidate TSEP on loading conditions and degradation mechanisms such that effects of those factors are considered when inferring temperature and health information from measured TSEPs.

An essential problem with the online measurement of thermo-sensitive electrical parameters during converter operation is measurement noise which can degrade the accuracy of the measurement. Therefore, after the online measurement is made, it is very important to improve the accuracy of the resolved T_J and eliminate the noise inherited from the measurement. This can be achieved through many algorithms. A good candidate to solve this problem is the algorithm of the Kalman Filter which is explained in the next chapter.

3.5**Summary**

This chapter introduced the required theory for the thermal conduction problem in IGBT power modules. Modelling methods for the thermal

conduction path were presented. These will be used later for constructing the electro-thermal model of the IGBT module. Methods to obtain an online measurement or estimate of junction temperature were reviewed. Among them, the approach of thermos-sensitive electrical parameters (TSEPs) seems to be suitable for real-time health monitoring as explained earlier. Therefore, the methods proposed in literature to acquire online measurement of TSEPs were reviewed.

Chapter 4 Proposed Online Health Monitoring Framework for IGBT Power Module

4.1 Introduction

The previous chapter reviewed the state-of-the-art the common methods of obtaining junction temperature of power modules. This chapter introduces the proposed health monitoring framework for in-service assessment of the heath state of IGBT power modules. The framework is presented first and the multiple functionalities in the framework are discussed, then the theoretical background of the methods employed are presented.

4.2 A Framework for In-service Health Monitoring of IGBT Power Modules

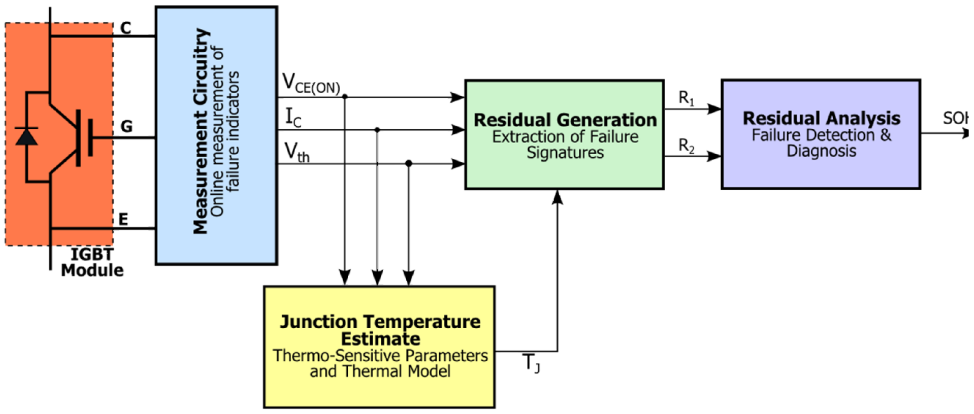


Figure 4.1 The proposed health monitoring framework

Figure 4.1 shows a block diagram of the proposed health monitoring framework of IGBT power modules. This framework includes multiple functionalities which operate together in order to come out with an assessment of the health state of the IGBT module. This framework operates independently from the topology of the power converter and does not interfere with the control strategy or with the normal operation of the power converter. It provides an online health assessment of the wire-bonded interconnects and the thermal path within power modules as they degrade overtime due to aging.

In order to provide a health assessment of a the power module, a set of functions must be implemented in order to detect deviations of the module characteristics from its original state and whether that deviation is caused by wire-bond lift-off or by solder fatigue. Thus, discrimination between these two failure mechanisms can be achieved. The different functional blocks in Figure 4.1 can be described as follows:

Measurement Circuitry: this is a dedicated hardware circuit which is connected to the IGBT power module and provides an online measurement of electrical parameters such as the on-state voltage $V_{CE(ON)}$, gate threshold voltage V_{th} and loading current I_L during normal operation of the power converter. These parameters are used by the framework to estimate junction temperature and to extract health state information.

Junction Temperature Estimate: this block provides information about the junction temperature T_J of the monitored IGBT module. Junction temperature is an essential operating parameter which has an effect on all electrical parameters that can be used as health indicators. It is also considered as a health indicator of the thermal path. This block allows a real-time estimate of T_J to be obtained using measured data of a TSEP and Kalman filter algorithm. More details about the Kalman filter are presented later in this chapter.

Residual Generation: after all the required information of health indicators and TSEPs are acquired, they are processed to eliminate the effects of noise and operating conditions such as loading current and temperature. This is achieved using reference models of the module in its original state. The output of this stage is a set of residuals which reveal the deviation of the power module from its original healthy state, thus, providing a mean to detect solder fatigue and wire-bond lift-off. This process is detailed later in this chapter.

Residual Analysis: after the residuals are generated they are analysed statistically in order to detect any deviation which is indicative of an ongoing degradation. The output of this stage gives indications of solder fatigue and wire-bond lift-off failures.

4.3 A Background of Kalman Filter

For the purpose of obtaining a real-time estimate of junction temperature of the IGBT module, Kalman filter algorithm is used. The Kalman filter is a state-estimator which estimates the states of a linear system assuming a known input vector , a measurement vector are available. Therefore, in this application, Kalman filter is a model-based approach that uses a thermal model of the heat conduction path to process a T_J measurement signal provided from the online measurement of a TSEP. Kalman filter helps improving the accuracy of the T_J estimate by eliminating the noise from the online measurement. The adaptive property of Kalman filter, which is based on a predict-correct mechanism allows consistent and accurate estimates of junction temperature to be obtained in the presence of time-varying factors such as module aging due to solder fatigue and varying cooling conditions.

4.3.1 Introduction to the Least-Squares Estimation

Gauss in 1795 was the first to propose a solution for the problem of estimating the coefficients of a system of equations from a noisy measurement [120]. The least-squares method is concerned with estimating system parameters that minimizes the “error” between estimates and measurements. This error is characterized by the sum of errors squared. Later on, Kolmogorov in 1941 and Wiener in 1942 proposed an optimization approach based on a cost function of the mean errors squared to find system parameters [121]. The work of Wiener-Kolmogorov formed the foundation for Kalman who applied the theory of state-space variables to Wiener-Kolmogorov optimal filtering.

The mathematical formulation of the optimal filtering problem proposed by Kalman led to a nonlinear differential equation. Kalman and Bucy recognized that this equation is a Reccati difference equation which has a recursive numerical solution. This solution can easily be implemented on a digital computer to find the optimal set of parameters which minimizes the cost function.

4.3.2Bayesian Background of Kalman Filtering

Consider two random dependent variables X and Y which can be described by probability density functions (pdf) and whose dependence can be described by a linear relationship:

$$\mathbf{y} = \mathbf{H}\mathbf{x} + v \tag{4.1}$$

where $\boldsymbol{y}$ and $\boldsymbol{x}$ are vectors representing individual values of the random variables X and Y, v is a stochastic process which represents the measurement noise and $\boldsymbol{H}$ is the measurement matrix.

Suppose that $\boldsymbol{x}$ is an immeasurable variable whereas $\boldsymbol{y}$, which is correlated to $\boldsymbol{x}$, can be measured but that measurement is corrupted by noise v as described in (4.1). The aim is to infer information about the variable $\boldsymbol{x}$ given the noisy measurement of $\boldsymbol{y}$. Estimation can be described by the procedure of inferring information about the random variable X from information given by another random variable Y with the aid of a conditional density function [122]. The probability density function of $\boldsymbol{x}$ conditional on a given $\boldsymbol{y}$, referred to as $p(x|y)$, summarizes all the information about X that is given by the knowledge that $Y=\boldsymbol{y}$.

Assuming that the probability density function $p(x)$ summarizes the knowledge about X before $Y=\boldsymbol{y}$ is given, then the conditional probability $p(x|y)$ tells how the knowledge about X has changed after knowing that $Y=\boldsymbol{y}$. This is called the Bayesian update process. It can be described by Bayes' rule which expresses the conditional probability function:

$$p(x \mid y) = \frac{p(y \mid x)p(x)}{p(y)} \tag{4.2}$$

The density function $p(x|y)$ is termed the *a posteriori* density function which represents the knowledge of $\boldsymbol{x}$ *after* the information $Y=\boldsymbol{y}$ is used, whereas $p(x)$ is termed the *a priori* density function which represents the knowledge of $\boldsymbol{x}$ *before* the information $Y=\boldsymbol{y}$ is used. $p(y|x)$ is often termed the *likelihood* (probability that the new information takes on the value $Y=y$ given that $X=x$) and $p(y)$ is often termed the *evidence* (probability that the new information takes on the value $Y=y$) and it acts as a normalization factor in (4.2).

Since $p(x|y)$ sums up all the information about X given that $Y=\boldsymbol{y}$, the *a posteriori* density function $p(x|y)$ is all that is required to generate an estimate $\hat{\boldsymbol{x}}$ of the random variable X from a measurement $\boldsymbol{y}$. In addition, a criterion should define what a best estimate or an *optimal* estimate $\hat{\boldsymbol{x}}$ is. This can be defined according to a cost function that measures optimality. By applying this cost function to the *a posteriori* $p(x|y)$ the estimate $\hat{\boldsymbol{x}}$ can be calculated.

Multiple cost functions are proposed. However, according to the least-squares method stated by Gauss, the most probable value $\hat{\boldsymbol{x}}$ of the *a posteriori* $p(x|y)$ is considered as the best estimate [121]. This is determined by minimizing the Mean-Squared Error which can be expressed by the following cost function:

$$\mathbf{J} = \frac{1}{2}(\mathbf{y} - \mathbf{H}\hat{\mathbf{x}})^T (\mathbf{y} - \mathbf{H}\hat{\mathbf{x}}) \qquad \textbf{(4.3)}$$

where the error is defined as the difference between the true measurement $\boldsymbol{y}$ and the estimated value of $\boldsymbol{y}$ from the estimate $\hat{\boldsymbol{x}}$. In this way, the estimate incorporates all available information given about the random variable X and the measurement $\boldsymbol{y}$. This estimate is represented by the *a posteriori* probability $p(x|y)$ which is given by (4.2).

Bayesian filtering in general is concerned with the determination of the *a posteriori* $p(x|y)$ regardless of the types of probability density function. The Kalman Filter is a special case of Bayesian filtering when the Linear-Quadratic-Gaussian (LQG) assumptions are made which is defined as follows:

- The relationship between X and Y is linear.
- The random variables X and Y are Gaussian.
- The cost function is a quadratic function of the estimation error.

Therefore, the Kalman filter is a state-estimator that calculates the mean and the covariance of a Gaussian *a posteriori* $p(x|y)$ density function. This is done by minimizing the mean-squares of estimation error described in the quadratic cost function in (4.3).

Multiple derivations have been proposed for Kalman filter equations. It was derived originally by Kalman [123] using the orthogonality principle.

Later on, Kailath [124] derived the equations using the so-called innovations approach. Ho and Lee [125] formulated the Kalman filter from a Bayesian probability perspective. They showed that Kalman filter is a special case of the Bayesian Filtering when the assumptions of LQG are made.

4.3.3 Derivation of Kalman Filter

Consider a vector $\boldsymbol{y}_k$ which represents the measurements available at discrete time instants $\boldsymbol{t}_k$ as $\{y_1, y_2, \ldots, y_k\}$ where $k=1,2,\ldots,n$ is an index and n is the number of measurements. This measurement $\boldsymbol{y}_k$ is correlated with a vector $\boldsymbol{x}_k$ which represents the states of a linear time-invariant dynamic system. This correlation can be described by a state-space representation which describes the system dynamics:

$$\mathbf{x}_{k+1} = \mathbf{F}\mathbf{x}_k + \mathbf{G}w_k \tag{4.4}$$

$$\mathbf{y}_k = \mathbf{H}\mathbf{x}_k + v_k \tag{4.5}$$

where $\boldsymbol{F}$ and $\boldsymbol{H}$ are called the state transition matrix and the measurement matrix respectively whereas $\boldsymbol{G}$ is the process noise gain matrix. The process noise w_k and the measurement noise v_k are assumed to be zero-mean white, Gaussian and independent random sequences and uncorrelated with system states $\boldsymbol{x}_k$. Since the system is linear and w_k and v_k are Gaussian, this results in $p(x_k)$ and $p(y_k)$ being Gaussian density functions. These assumptions are expressed as follows:

$$E(v_k) = 0 \qquad E(w_k) = 0 \tag{4.6}$$

$$Cov(v_k) = R \qquad Cov(w_k) = Q \tag{4.7}$$

$$Cov(\mathbf{x}_k, v_k) = 0 \qquad Cov(\mathbf{x}_k, w_k) = 0 \tag{4.8}$$

$$Cov(w_k, v_k) = 0 \tag{4.9}$$

where $E(.)$ is the mean value and $Cov(.)$ is the covariance. The aim is to determine the most probable value $\hat{\boldsymbol{x}}_k$ that maximizes the *a posteriori* density function $p(\boldsymbol{x}_k|\boldsymbol{y}_k)$ given by Bayes' rule:

$$p(\mathbf{x}_k \mid \mathbf{y}_k) = \frac{p(\mathbf{y}_k \mid \mathbf{x}_k)\, p(\mathbf{x}_k \mid \mathbf{y}_{k-1})}{p(\mathbf{y}_k \mid \mathbf{y}_{k-1})} \tag{4.10}$$

where $p(\boldsymbol{x}_k|\boldsymbol{y}_k)$ is Gaussian since the joint probability density function of two Gaussian variables is Gaussian. Therefore, this estimate is called the Maximum

A Posteriori (MAP) estimate of $\boldsymbol{x}_k$ and it can be given by the mode or the mean value of $p(\boldsymbol{x}_k|\boldsymbol{y}_k)$ as can be seen in Figure 4.2.

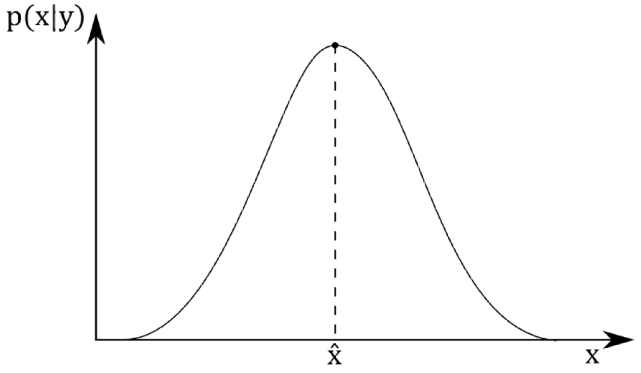


Figure 4.2 Maximum A Posteriori Estimate for Gaussian conditional probability density function p(x|y)

All the terms on the right hand side of (4.10) are Gaussian and can be expressed by their mean *E(.)* and covariance *Cov(.)*. The denominator $p(\boldsymbol{y}_k|\boldsymbol{y}_{k-1})$ is a normalization factor and therefore it can be ignored from the following derivation.

At this point it is important to discriminate between the time step (or the time-update) which is referred to by the subscript k and the Bayesian update (or measurement-update) which is referred to by the superscripts (+) and (-). At every time instant k there are *a priori* (-) estimate, *before* the measurement $\boldsymbol{y}_k$ is used, and *a posteriori* (+) estimate *after* the measurement $\boldsymbol{y}_k$ is used. The aim is to determine the mean $\hat{\boldsymbol{x}}_k^+$ and the covariance $\boldsymbol{P}_k^+$ of the *a posteriori* $p(\boldsymbol{x}_k|\boldsymbol{y}_k)$ as well as the mean $\hat{\boldsymbol{x}}_k^-$ and the covariance $\boldsymbol{P}_k^-$ of the *a priori* $p(\boldsymbol{x}_k|\boldsymbol{y}_{k-1})$. This can be expressed as:

$$E[\mathbf{x}_k \mid \mathbf{y}_k] = \hat{\mathbf{x}}_k^+ \qquad Cov(\mathbf{x}_k \mid \mathbf{y}_k) = \mathbf{P}_k^+ \tag{4.11}$$

$$E[\mathbf{x}_k \mid \mathbf{y}_{k-1}] = \hat{\mathbf{x}}_k^- \qquad Cov(\mathbf{x}_k \mid \mathbf{y}_{k-1}) = \mathbf{P}_k^- \tag{4.12}$$

The mean and covariance of the likelihood $p(\boldsymbol{y}_k|\boldsymbol{x}_k)$ can be determined from (4.5):

$$\hat{\mathbf{y}}_k = E[\mathbf{y}_k \mid \mathbf{x}_k] = \mathbf{H}\hat{\mathbf{x}}_k^- \qquad Cov(\mathbf{y}_k \mid \mathbf{x}_k) = \mathbf{R} \tag{4.13}$$

where $\boldsymbol{R}$ is the covariance of the measurement noise v according to (4.7). From (4.4) the mean and covariance for the *a priori* $p(\boldsymbol{x}_k|\boldsymbol{y}_{k-1})$ can be expressed:

$$\hat{\mathbf{x}}_k^- = E[\mathbf{x}_k \mid \mathbf{y}_{k-1}] = \mathbf{F}\hat{\mathbf{x}}_{k-1}^+$$
$$\mathbf{P}_k^- = Cov(\mathbf{x}_k \mid \mathbf{y}_{k-1}) = \mathbf{F}\mathbf{P}_{k-1}^+\mathbf{F}^T + \mathbf{G}\mathbf{Q}\mathbf{G}^T \quad \textbf{(4.14)}$$

Notice that $\boldsymbol{P}_k^-$ can be viewed in two ways: as the covariance matrix of the conditional probability $p(\boldsymbol{x}_k|\boldsymbol{y}_{k-1})$, and as the error covariance matrix where the estimate error is defined as:

$$\mathbf{e}_k = \mathbf{x}_k - \hat{\mathbf{x}}_k^- \quad \textbf{(4.15)}$$

and therefore:

$$\begin{aligned}\mathbf{P}_k^- &= Cov(\mathbf{x}_k \mid \mathbf{y}_{k-1}) \\ &= E\left[\left(\mathbf{x}_k - \hat{\mathbf{x}}_k^-\right)^T\left(\mathbf{x}_k - \hat{\mathbf{x}}_k^-\right)\right] \\ &= E\left[\mathbf{e}_k^T\mathbf{e}_k \mid \mathbf{y}_{k-1}\right] \\ &= Cov(\mathbf{e}_k \mid \mathbf{y}_{k-1})\end{aligned} \quad \textbf{(4.16)}$$

where $\hat{\boldsymbol{x}}_k^-$ is the mean value of $p(\boldsymbol{x}_k|\boldsymbol{y}_{k-1})$ as stated in (4.12). This defines the *a priori* error. In a similar way the *a posteriori* error is defined where the error covariance matrix $\boldsymbol{P}_k^+$ is the covariance matrix of the conditional probability $p(\boldsymbol{x}_k|\boldsymbol{y}_k)$.

Considering that all pdfs in (4.10) are expressed as Gaussian functions, using (4.14) and (4.13) the *a posteriori* density function in (4.10) which represents the measurement update of the Kalman Filter can be written as a Gaussian pdf:

$$p(\mathbf{x}_k \mid \mathbf{y}_k) = \frac{1}{(2\pi)^{n/2}\left|\mathbf{R}\right|^{1/2}\left|\mathbf{P}_k^-\right|^{1/2}}\exp\left(-\frac{1}{2}\left(\mathbf{y}_k - \mathbf{H}\mathbf{x}_k^-\right)^T\mathbf{R}^{-1}\left(\mathbf{y}_k - \mathbf{H}\mathbf{x}_k^-\right) - \frac{1}{2}\left(\mathbf{x}_k - \hat{\mathbf{x}}_k^-\right)^T\mathbf{P}_{k+1}^{-1}\left(\mathbf{x}_k - \hat{\mathbf{x}}_k^-\right)\right) \quad \textbf{(4.17)}$$

The maximum of the function $p(\boldsymbol{x}_k|\boldsymbol{y}_k)$ as expressed in (4.17) happens when its derivative in respect to $\boldsymbol{x}_k$ equals to zero. To simplify the algebraic manipulation, the derivative of the logarithm of $p(\boldsymbol{x}_k|\boldsymbol{y}_k)$ can be considered:

$$\frac{\partial}{\partial \mathbf{x}_k}\log p(\mathbf{x}_k \mid \mathbf{y}_k) = 0 \quad \textbf{(4.18)}$$

Solving this equation for $\hat{\boldsymbol{x}}_k$ gives the *a posteriori* estimate of the Kalman filter:

$$\hat{\mathbf{x}}_k^+ = \hat{\mathbf{x}}_k^- + \mathbf{K}_k\left[\mathbf{y}_k - \mathbf{H}\hat{\mathbf{x}}_k^-\right] \quad \textbf{(4.19)}$$

where the Kalman filter gain matrix $\boldsymbol{K}_k$ is determined by:

$$\mathbf{K}_k = \mathbf{P}_k^- \mathbf{H}^T \left[\mathbf{H} \mathbf{P}_k^- \mathbf{H}^T + \mathbf{R} \right]^{-1} \quad \textbf{(4.20)}$$

substituting (4.19) in (4.15) and using (4.5) the error can be written as:

$$\mathbf{e}_k = \left[\mathbf{I} - \mathbf{K}_k \mathbf{H} \right] \left(\mathbf{x}_k - \hat{\mathbf{x}}_k^+ \right) - \mathbf{K}_k v_k \quad \textbf{(4.21)}$$

The *a posteriori* error covariance is then determined by:

$$\mathbf{P}_k^+ = \left[\mathbf{I} - \mathbf{K}_k \mathbf{H} \right] \mathbf{P}_k^- \quad \textbf{(4.22)}$$

So, the mean value $\hat{\boldsymbol{x}}_k^+$ and the covariance $\boldsymbol{P}_k^+$ of the *a posteriori* density function $p(\boldsymbol{x}_k|\boldsymbol{y}_k)$ is calculated in (4.19) and (4.22) where $\hat{\boldsymbol{x}}_k^+$ represents the *optimal* estimate given bythe Kalman Filter of the system state vector $\boldsymbol{x}_k$ whereas $\boldsymbol{P}_k^+$ represents the covariance of the estimation error. This estimate $\hat{\boldsymbol{x}}_k^+$ which is given by the Maximum A Posteriori (MAP) cost function is the same as the Least-Squares Estimate under the Gaussian assumption made earlier [122].

4.3.4 Practical Implementation of Kalman Filter

The Kalman filter is implemented as a recursive algorithm which consists of a set of steps that can be summarized from the equations derived in the previous section as follows:

1. Given the initial state $\boldsymbol{x}_0$ and initial covariance $\boldsymbol{P}_0$ compute the *a priori* estimate

   $$\hat{\mathbf{x}}_k^- = \mathbf{F} \hat{\mathbf{x}}_{k-1}^+ + \mathbf{G} w_k$$

   $$\mathbf{P}_k^- = \mathbf{F} \mathbf{P}_{k-1}^+ \mathbf{F}^T + \mathbf{G} \mathbf{Q} \mathbf{G}^T$$

2. Compute the Kalman gain matrix

   $$\mathbf{K}_k = \mathbf{P}_k^- \mathbf{H}^T \left[\mathbf{H} \mathbf{P}_k^- \mathbf{H}^T + \mathbf{R} \right]^{-1}$$

3. Compute the *a posteriori* estimate given the measurement $\boldsymbol{y}_k$

   $$\hat{\mathbf{x}}_k^+ = \hat{\mathbf{x}}_k^- + \mathbf{K}_k \left[\mathbf{y}_k - \mathbf{H} \hat{\mathbf{x}}_k^- \right]$$

4. Compute the *a posteriori* covariance matrix

   $$\mathbf{P}_k^+ = \left[\mathbf{I} - \mathbf{K}_k \mathbf{H} \right] \mathbf{P}_k^-$$

Those steps can be calssified into: a time update and a measurement update. This can be depicted as shown in Figure 4.3. The time update relies on the state-space model to give predictions of the state $\boldsymbol{x}_k$ for $k=k_1$ where k_1 is some arbitrary time instant where the last *a posteriori* $\hat{\mathbf{x}}_k^+$ is available. The measurement update come into action when a measurement $\boldsymbol{y}_k$ becomes available at $k=k_2$ where $k_2>k_1$. When the measurement $\boldsymbol{y}_k$ is not available, the algorithm can run continuously unchanged with the exception that the measurement sensitivity matrix $\boldsymbol{H=0}$. And hence, $\mathbf{P}_k^+ = \mathbf{P}_k^-$ and $\hat{\mathbf{x}}_k^+ = \hat{\mathbf{x}}_k^-$.

As the Kalman Filter is a recursive algorithm, it is initialized with some initial conditions $\boldsymbol{x}_0$ and $\boldsymbol{P}_0$ then the algorithm starts converging into a solution after a few time steps. The convergence of the algorithm is independent of the initial conditions [120], that is regardless of what value the initial state $\boldsymbol{x}_0$ and the initial covariance $\boldsymbol{P}_0$ are, the algorithm will always converge to the same solution. Therefore, $\boldsymbol{x}_0$ and $\boldsymbol{P}_0$ can be set to any arbitrary values ensuring that $\boldsymbol{P}_0$ is a symmetric positive definite matrix. A common choice is to set $\boldsymbol{P}_0=\boldsymbol{I}$ where $\boldsymbol{I}$ is the identity matrix which is symmetric positive definite.

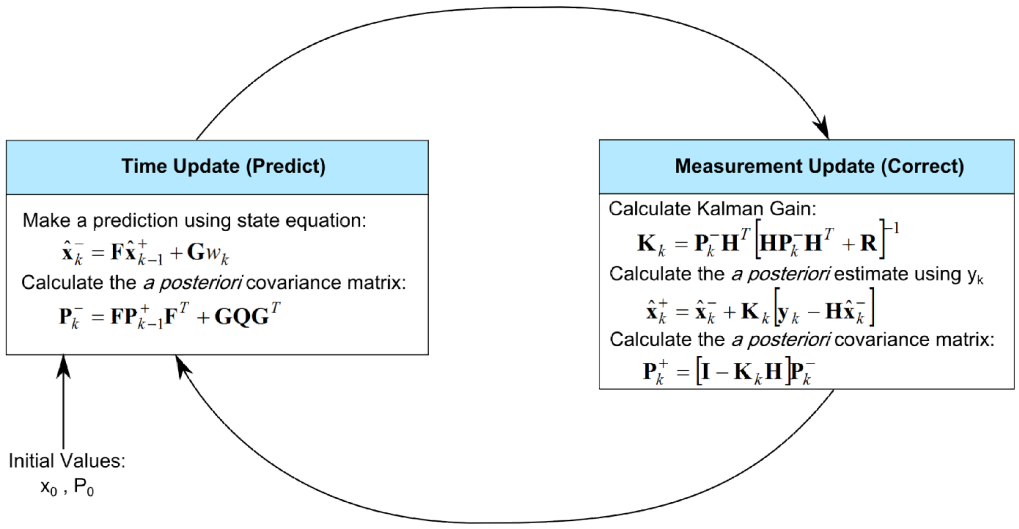


Figure 4.3 The Recursive algorithm of Kalman Filter is divided into Time Update and Measurement Update steps

Covariance Matrices $\boldsymbol{R}$ and $\boldsymbol{Q}$ of measurement and process noise are supposed to be known parameters of the Kalman filter. Covariance matrix $\boldsymbol{R}$ of the measurement noise can be determined practically either from the sensor noise specification or by experimental observation. A set of time measurement

can be recorded and processed off-line to estimate the variance of the measurement data using some software packages such as MATLAB.

Determination of process noise covariance matrix $\boldsymbol{Q}$ is more difficult as this noise is internal to the process and cannot be observed externally. However, $\boldsymbol{Q}$ represents the uncertainty of the process model and it influences the Kalman gain Matrix $\boldsymbol{K}_k$ through the error covariance $\boldsymbol{P}_k^-$ as can be seen from (4.20). This means that a larger value of $\boldsymbol{Q}$ which means large uncertainty in the process model would result in larger $\boldsymbol{K_k}$ and consequently more influence is given to the measurement according to (4.19). However, that would result in a noisier estimate since the measurement noise is given more influence on the estimate.

Therefore, the matrix $\boldsymbol{Q}$ can be considered as a tuning parameter that can be determined by observing the noise level in the resulting estimate. It can be tuned to give more weight to the measurement on the expense of the model. It can be chosen such that more weight is given to the measurement without the estimate becoming very noisy. In fact, it is the ratio of $\boldsymbol{R}$ to $\boldsymbol{Q}$ which is important. If the two parameters are changed such that their ratio is constant, the performance of the Kalman Filter would not change.

4.3.5 Summary

The algorithm of the Kalman filter has been presented in this section. In this work the Kalman filter is used to estimate junction temperature of the IGBT module in real-time. A thermal model of the heat conduction path and a measurement of thermo-sensitive electrical parameter are combined to obtain estimates of junction temperature. However, other solutions may be available to estimate junction temperature which were reviewed in the previous chapter. The next section presents the analytical redundancy method of generating residuals. Residuals are the means used in this work to monitor the health state of the IGBT module.

4.4A Background of the Analytical Redundancy for Health Monitoring

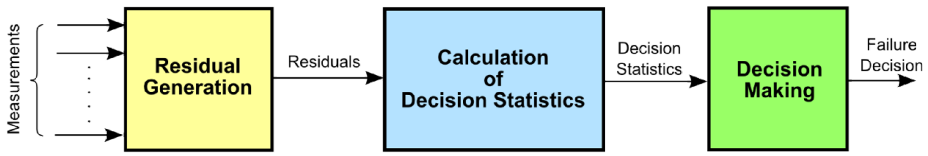


Figure 4.4 Residual-Based Health Monitoring

The analytical redundancy approach [126, 127] consists of two steps: residual generation and decision making as illustrated in Figure 4.4. The first step is Residual Generation where measurement data are processed by means of reference models in order to separate the effects of degradation from the effects of operating conditions. Normally, system degradation information contained in the measurement data is mixed with the effects of operating conditions such as current and temperature. Therefore, it is necessary to remove these effects from the measurement data.

Residuals are defined as quantities that represent the discrepancy between measured variables and their expected values given for the healthy baseline state. The expected values are obtained from a reference model that represents the power module in its original state. The second step is Residuals Evaluation where generated residuals are evaluated to reveal any deviation from their original value. This evaluation normally involves statistical testing because a residual is a non-deterministic signal. Therefore, it is more convenient to detect changes in its statistical distribution. According to the result of the statistical analysis stage a decision can be made about the health state of the power module.

The residual generator is designed according to the modelled system. For a static system, the residual generator is a reformulation of the input-output relationship. Whereas for a dynamic system the residual generator can be obtained using a range of different methods [128], for example: parity equations, diagnostic observers, and Kalman Filters. In this work, residual generation for the static system representing the device on-state voltage is investigated as a means to deal with wire-bond failures whereas the Kalman

Filter is used as a residual generator to monitor the health state of the thermal path in a power module.

4.4.1 Modelling of Degradation Effects

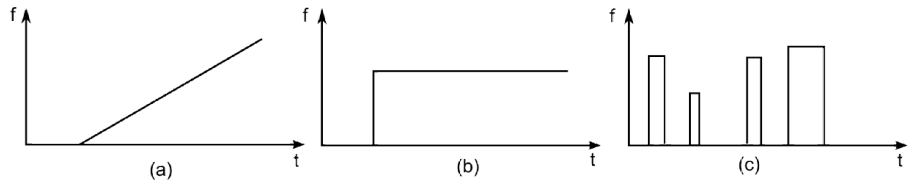


Figure 4.5 The time behaviour of the change in a physical process. (a) incipient (b) abrupt (c) intermittent

The effects of degradation in power modules should first be studied in order to build an understanding on how the change in residuals will change under degraded conditions. Changes affecting physical processes can be classified in terms of their time behaviour as [127]: abrupt (stepwise), incipient (drift-like) and intermittent. Those types are illustrated in Figure 4.5.

Two failure mechanisms of power modules are considered, wire-bond lift-offs and solder fatigue. In the case of wire-bond lift-off the mechanical fatigue process which drives the failure of the wire-bonds is a progressive process. However, the effect of a wire-bond failure on the electrical forward characteristic of the IGBT is abrupt. The on-state voltage $V_{CE(ON)}$ changes in an abrupt (step-wise) behaviour when wire-bonds are lifted. In the case of solder fatigue, the change in the thermal resistance resulting from solder fatigue is a progressive or incipient (drift-like) change.

This degradation, which can be observed at the output of the physical process, can be described as additive or multiplicative [127] depending on whether it acts external or internal to the process. These two types are explained in Figure 4.6 where f_i and f_o are additive changes at the input and the output of the process respectively and are therefore external to the system. Additive faults represent sensors failure at the input and at the output and they appear as offsets in the measurement. Multiplicative faults f_m are internal to the process and they appear as a change in the physical parameters of the system. Additive faults represent effects such as sensor failure at the input and at the

output and appear as offsets in the measurement. Multiplicative faults are internal to the physical process and they appear as a change in the physical parameters of the process.

In power modules, degradation of the thermal path due to solder fatigue can be considered as a multiplicative change to the heat conduction process as it changes the parameters of the thermal path. On the other hand, wire-bond lift-off can be considered as additive or multiplicative. This is explained in the next section.

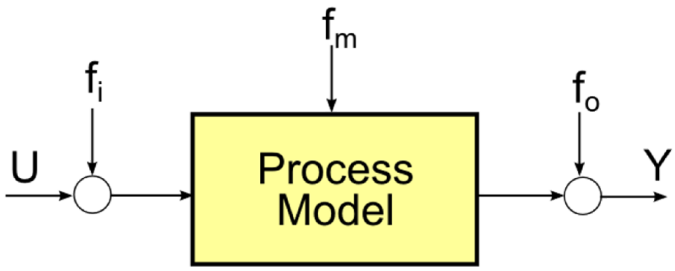


Figure 4.6 Faults acting of a physical process can be additive (sensor faults) or multiplicative (parameters change)

4.4.2Generating Residual for Wire-bonds Monitoring

Wire-bond failures result in an increment in the electrical resistance of the IGBT module. This increases the on-state voltage $V_{CE(ON)}$ and is described by the forward characteristic. The forward characteristic of an IGBT module is a static nonlinear relationship between device current I_C, on-state voltage $V_{CE(ON)}$ and junction temperature T_J assuming that gate-emitter voltage V_{GE} is constant. This kind of static nonlinear relationship can be represented by a polynomial:

$$V_{CE(ON)}(T_J, I_C) = a_0 + a_1 T_J + a_2 {T_J}^2 + \cdots + a_k {T_J}^k + b_1 I_C + b_2 {I_C}^2 + \cdots + b_j {I_C}^j + c_1 T_J I_C + \cdots + c_l {T_J}^l {I_C}^m \quad \textbf{(4.23)}$$

In a matrix form this can be represented by:

$$V_{CE(ON)} = \boldsymbol{AT} + \boldsymbol{BI} + \boldsymbol{CG} \quad \textbf{(4.24)}$$

where $\boldsymbol{A} = [a_0\ a_1 \dots\ a_k], \boldsymbol{B} = [b_1\ b_2 \dots\ b_j], \boldsymbol{C} = [c_1 c_2 \dots c_l], \boldsymbol{T^T} = [1\ T_J\ {T_J}^2 \dots {T_J}^k], \boldsymbol{I^T} = [I_C\ {I_C}^2 \dots {I_C}^j], \boldsymbol{G^T} = [T_J I_C\ T_J {I_C}^2\ {T_J}^2 I_C \dots {T_J}^l {I_C}^m]$

By further simplification:

$$V_{CE(ON)} = \boldsymbol{\Theta^T \Psi} \quad \textbf{(4.25)}$$

where $\boldsymbol{\Theta} = [\boldsymbol{A}\ \boldsymbol{B}\ \boldsymbol{C}], \boldsymbol{\Psi} = [\boldsymbol{T}\ \boldsymbol{I}\ \boldsymbol{G}]$

If the forward characteristic of the power module changes due to a wire-bond lift-off, this change can be represented as a multiplicative failure that affects the coefficients matrix $\boldsymbol{\Theta}$ of the polynomial (4.25) by an amount $\boldsymbol{\Delta\Theta}$ such that:

$$V_{CE(ON)} = (\boldsymbol{\Theta} + \boldsymbol{\Delta\Theta})^{\boldsymbol{T}} \boldsymbol{\Psi} \quad \textbf{(4.26)}$$

And therefore:

$$V_{CE(ON)} = \boldsymbol{\Theta^T \Psi} + \boldsymbol{\Delta\Theta^T \Psi} \quad \textbf{(4.27)}$$

where $\boldsymbol{\Delta\Theta} = [\boldsymbol{\Delta A}\ \boldsymbol{\Delta B}\ \boldsymbol{\Delta C}]$. Therefore, it can be seen that the effect of wire-bond lift-offs on the on-state voltage which is a multiplicative in nature, can be represented as additive to the output of the undegraded forward characteristic.

Defining the residual *r* as the difference between the actual (measured) system output $V_{CE(ON)}$ and estimated output $\hat{V}_{CE(ON)}$:

$$r = V_{CE(ON)} - \hat{V}_{CE(ON)} \quad \textbf{(4.28)}$$

This residual r according to (4.28) is affected by the parametric change $\boldsymbol{\Delta\Theta}$ of the forward characteristic in (4.27). Therefore, the residual *r* has the value of zero under the normal state when the forward characteristic of the IGBT module matches the original forward characteristic represented by the model in (4.23). Any change in *r* is then correlated to a change in the forward characteristic and hence the wire-bonds failures.

4.4.3Generating the Residual for Thermal Degradation Monitoring

It was explained earlier that the heat conduction path in a power module can be represented by an electrical equivalent Foster network. This

Foster network can be expressed by the following discrete state-space representation:

$$\begin{aligned} x_k &= \mathrm{F}x_{k-1} + \mathrm{L}u_k \\ y_k &= \mathrm{H}x_k + \mathrm{J}u_k \end{aligned} \quad \textbf{(4.29)}$$

where ***F***, ***L***, ***H*** and ***J*** are the system parameters under the original health state. Assuming ***ΔF***, ***ΔL***, ***ΔH***, and ***ΔJ*** are the changes in system parameters resulting from solder fatigue, this state-space model can be extended to accommodate the change in system parameters. In addition, process and measurement noise terms w_k and v_k can be added to the model along with the disturbance term d_k and an additive fault term q_k that represents output sensor faults. The model becomes:

$$\begin{aligned} x_k &= (F + \Delta F)x_{k-1} + (L + \Delta L)u_k + d_k + w_k \\ y_k &= (H + \Delta H)x_k + (J + \Delta J)u_k + q_k + v_k \end{aligned} \quad \textbf{(4.30)}$$

This state-space model which represents the thermal system of a power module can be used to derive a Kalman filter, as explained earlier in this chapter. Using the Kalman filter, the state estimate $\hat{x}_k$ and the estimated output $\hat{y}_k$ are given by the following expression assuming that the feedforward matrix ***J=0*** for simplification:

$$\hat{x}_k = F\hat{x}_{k-1} + K[y_k - \hat{y}_k] \quad \textbf{(4.31)}$$

$$\hat{y}_k = H\hat{x}_{k-1} \quad \textbf{(4.32)}$$

where K is the Kalman Gain Matrix. Defining the state estimate error e_k as the difference between the true state vector x_k and the estimated state vector $\hat{x}_k$. And defining the residual r_k as the difference between the measured output y_k and the estimated output $\hat{y}_k$:

$$e_k = x_k - \hat{x}_k \quad \textbf{(4.33)}$$

$$r_k = y_k - H\hat{x}_k^- \quad \textbf{(4.34)}$$

Using (4.30) and (4.31), the state estimation error e_k can be derived as:

$$e_k = [(F + \Delta F) - K(H + \Delta H)]e_{k-1} + (L + \Delta L)u_k + d_k + w_k + Kv_k + Kq_k \quad \textbf{(4.35)}$$

And the residual r_k can then be written in terms of e_k as:

$$r_k = (H + \Delta H)e_k + q_k + v_k \quad \textbf{(4.36)}$$

This expression shows that the residual r_k is driven by the state estimation error e_k in (4.35). Consequently this residual is affected by the change in system parameters $\Delta \boldsymbol{F}$, $\Delta \boldsymbol{L}$, $\Delta \boldsymbol{H}$ in addition to the disturbances d_k, noise terms w_k and v_k and sensor faults q_k.

Therefore, in the ideal case where no modelling errors are present, no disturbances are acting on the system and no faults in the sensor or in the physical process are present, the residual r_k ideally has a mean value of zero. However, in practice these conditions do not hold since modelling errors are unavoidable and external disturbance can affect the thermal system which leads to the residual r_k having an initial non-zero value in the healthy state.

4.4.4Statistical Evaluation for Residual Change Detection

In order to detect changes in the residuals which are caused by the degradation of the power module a statistical evaluation of the residuals is required. Residuals are non-deterministic signals. Therefore, an evaluation of the statistical distribution should be done to detect the deviation of the residuals from their original healthy state.

The required statistics for the evaluation depend on the shape of the statistical distribution of the residual. For example, in the case of a Gaussian distribution, the mean value and the variance are sufficient statistics to describe the Gaussian distribution. According to [129] it is more convenient to consider the normalized residual for statistical evaluation:

$$r_{nk} = (HP_k^- H^T + R)^{1/2} \times r_k \quad \textbf{(4.37)}$$

where the term $(\boldsymbol{HP}_k^-\boldsymbol{H}^T+\boldsymbol{R})^{1/2}$ is the standard deviation of the residual. Therefore, in the normal healthy state the mean value of the residual μ_r can be expressed as:

$$\mu_r = E[r_{nk}] \quad \textbf{(4.38)}$$

The deviation of the mean statistics is indicative of a change in the actual system from its healthy state. The change in this statistic can be represented as:

$$\Delta\mu_r = E[r(t) - \mu_r] \quad \textbf{(4.39)}$$

This deviation is depicted in Figure 4.7 where $p_n(r)$ is the statistical distribution of the residual in the normal state whereas $p_f(r)$ is the distribution of the residual in the degraded state. The shift in the mean value of the distribution is $\Delta\mu_r$.

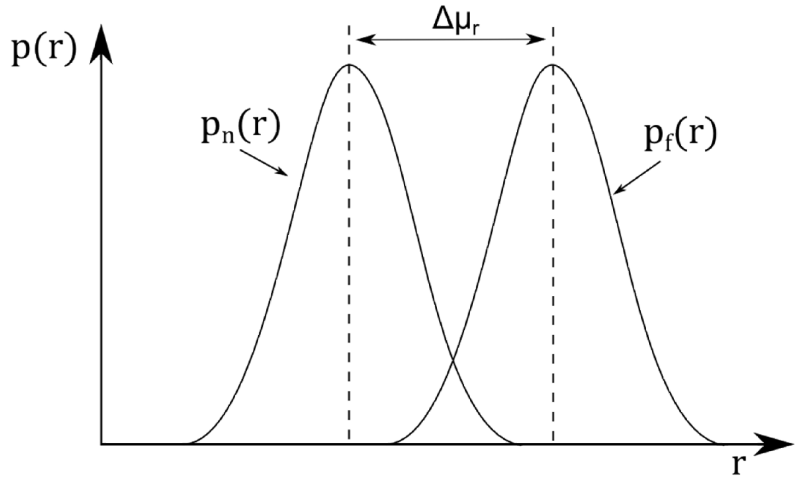


Figure 4.7 The change in the statistical properties of residual signal due to system degradation

4.4.5Summary

The concept of analytical redundancy is used in this work as a mean to get an assessment of the health state of the power module. This is practically achieved using a set of reference models of the monitored processes or parameters. Measurement data of the monitored parameters (T_J and $V_{CE(ON)}$) are compared to the expected values of the same parameters given by the reference models to generate residuals. The change in the residuals is indicative of a change in the actual power module. Different residuals are used to monitor different mechanisms such as wire-bond liftoff and solder fatigue.

4.5**Summary**

This chapter introduced the proposed framework for the health monitoring of IGBT power modules. A background of the algorithms used in this framework is presented. Kalman filter is used to estimate the junction temperature T_J of the power module. Then, analytical redundancy is discussed

and the generating residuals to monitor the changes in the power modules are explained.

Chapter 5 Experimental Investigation of On-state Voltage $V_{CE(ON)}$ and Threshold Voltage V_{th}

5.1 Introduction

This chapter studies by experiment the dependencies of two electrical parameters of an IGBT in order to evaluate their use as failure indicators and as thermo-sensitive electrical parameters. Among the various electrical parameters of the IGBT, the on-state voltage $V_{CE(ON)}$ and the threshold voltage V_{th} are chosen to be characterized with temperature variation and with packaging degradation. These two parameters are chosen due to their dependency on temperature and packaging wear-out. Those reasons are explained in the following sections.

5.2 Experimental Test Setup

A Sony-Tektornix 371A High Power Curve Tracer shown in Figure 5.1 is used to help investigate the characteristics of the on-state voltage $V_{CE(ON)}$ and threshold voltage V_{th} of the IGBT. The curve tracer is a test equipment used to characterise semiconductor devices (IGBT, BJT, Diodes, …). Among multiple uses, it can be used to measure the forward characteristic of an IGBT as well as the transfer characteristic. The IGBT module can be mounted on a temperature controlled hotplate such that variations of those characteristics with temperature can be measured.

Figure 5.1 Sony 371A High Power Curve Tracer used for IGBT Characterization

5.3 On-state Voltage $V_{CE(ON)}$

5.3.1 Temperature dependency

The behaviour of $V_{CE(ON)}$ can be described by the forward characteristic of the IGBT which is dependent on temperature, current I_C and gate voltage V_{GE}. A curve tracer is used to obtain the forward characteristic of the IGBT at multiple temperatures. The IGBT module is mounted on a temperature controlled hotplate and the temperature of the IGBT chip is assumed to be similar to the hotplate temperature. This is acceptable since the curve tracer applies short pulses of current which minimizes power dissipation. Therefore, the temperature change during the measurement cycle is negligible.

Figure 5.2 shows the forward characteristic of a 1.2kV/400A IGBT module at a constant V_{GE}=15V and multiple temperatures. It is clear that the temperature coefficient of $V_{CE(ON)}$ is a function of current, where at low currents $V_{CE(ON)}$ has a negative temperature coefficient and at high currents it has a positive temperature coefficient. The point where temperature coefficient changes sign is the inflection point and here $V_{CE(ON)}$ becomes independent of temperature. For the module under test, the negative temperature coefficient of $V_{CE(ON)}$ below inflection point is found to have a maximum value of 1.23mV/^{o}C at 8A which decreases in magnitude towards the inflection point.

Above that point temperature coefficient becomes positive and increases with current to reach 2.68mV/°C at 180A.

The variable temperature coefficient of $V_{CE(ON)}$ can be better seen in Figure 5.3. Here the $V_{CE(ON)}$ is plotted as a function of temperature at multiple current values. The approximate linear correlation of $V_{CE(ON)}$ to temperature is clear at all current values. The slope (i.e. temperature coeffcient) of the lines is dependent on current value. This dependence makes the joint function $V_{CE}=f(I_C,T_J)$ a nonlinear function assuming V_{GE} is constant.

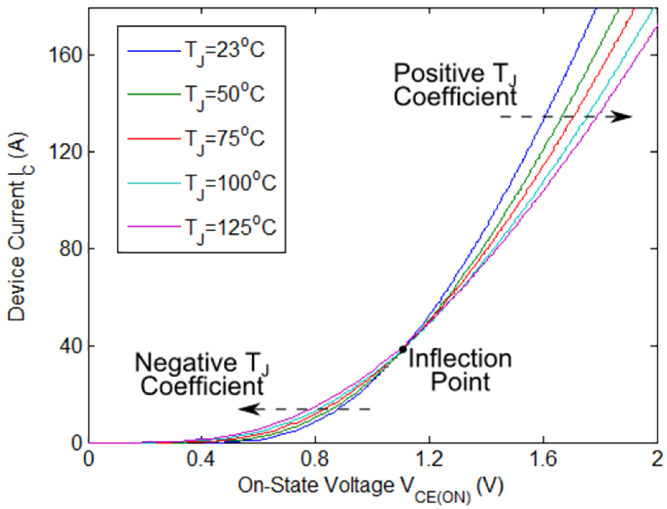


Figure 5.2 I-V characteristic of a 1.2kV/400A IGBT power module at multiple temperatures shows temperature dependency of the on-state voltage $V_{CE(ON)}$.

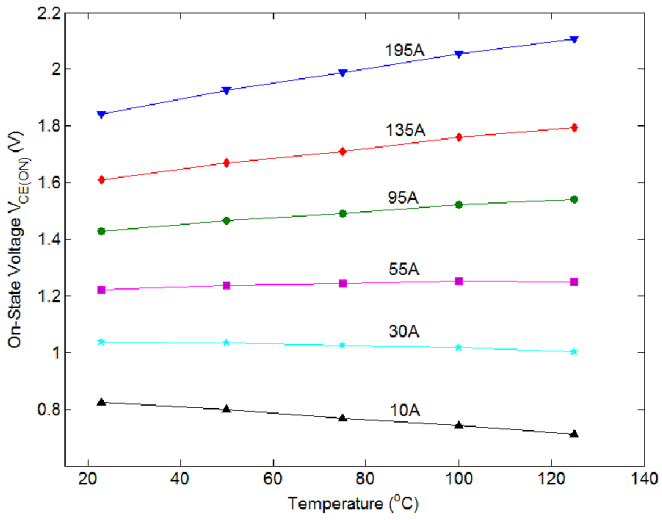


Figure 5.3 On-state voltage as a function of temperature T_J at multiple currents shows correlation of temperature sensitivity to current.

This nonlinear correlation between on-state voltage $V_{CE(ON)}$, current I_C and junction temperature T_J can be explained by considering the IGBT structure shown in Figure 5.4. The IGBT can be considered as a PiN Diode in series with a MOSFET. The collector-emitter voltage drop V_{CE} of the IGBT during forward conduction can be described as the sum of the forward voltage drop of the PiN diode and the forward voltage drop of the MOSFET structure. Baliga [76] expressed the collector-emitter voltage drop of the IGBT during ON state as a function of gate voltage V_G and device current I_C using the following formula:

$$V_{CE(ON)} = \frac{2kT}{q}\ln\left(\frac{I_C d}{2qWZD_a n_i F\left(d/L_a\right)}\right) + \frac{I_C L_{CH}}{\mu_{ns} C_{OX} Z(V_G - V_T)} \qquad \textbf{(5.1)}$$

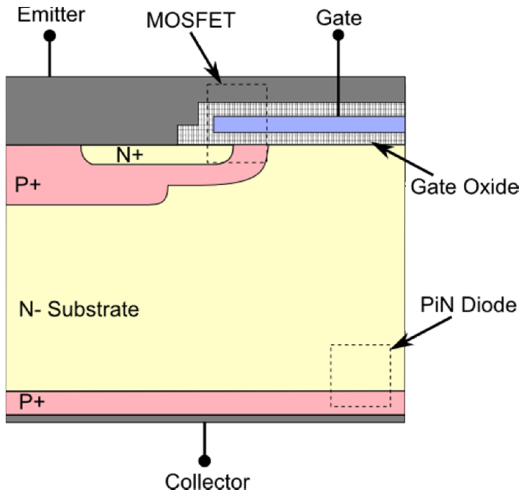


Figure 5.4 IGBT device structure can be viewed as PiN diode in series with MOSFET

The first term represents the PiN diode forward voltage drop while the second term represents the MOSFET forward voltage drop. Two parameters in this formula are temperature dependent. The intrinsic carrier concentration n_i in the first term and the minority carriers μ_{ns} in the second term. These two parameters have contradicting temperature coefficients and their net effect results in the characteristic shown in Figure 5.2. The region above the inflection point is dominated by the MOSFET effect whereas the channel carrier mobility μ_{ns} decreases with increased temperature causing higher electrical resistance and higher voltage drop. The region below the inflection point is dominated by the diode effect where the intrinsic carrier concentration

n_i increases with temperature. At the inflection point the two effects cancel each other and $V_{CE(ON)}$ of the IGBT becomes independent of temperature.

5.3.2Dependency on Packaging Degradation

To investigate the effect of wire-bond failures on $V_{CE(ON)}$, a single chip IGBT module is used for testing. The tested IGBT module has 8 wire-bonds connecting the emitter contact on the chip to the copper tracers on the substrate. The wire-bond lift-offs are emulated by cutting off the wires manually. The forward I-V characteristic of the IGBT is recorded using a curve tracer after each wire cut. Figure 5.5 shows the result of this test. It can be seen that $V_{CE(ON)}$ increases with wire-bond failures as a result of electrical resistance increment. This is similar to the correlation of $V_{CE(ON)}$ to junction temperature T_J which can be seen in Figure 5.2. This similarity in the effect of temperature and wire-bond failures masks the effect of wire-bond failures. It cannot be determined whether the increment in $V_{CE(ON)}$ is a result of temperature increment or a wire-bond failure (an increment in electrical resistance). Therefore, if $V_{CE(ON)}$ is used as a sensor to measure T_J, wire-bond failures will mask T_J information contained in $V_{CE(ON)}$ and result in an erroneous measurement of junction temperature T_J.

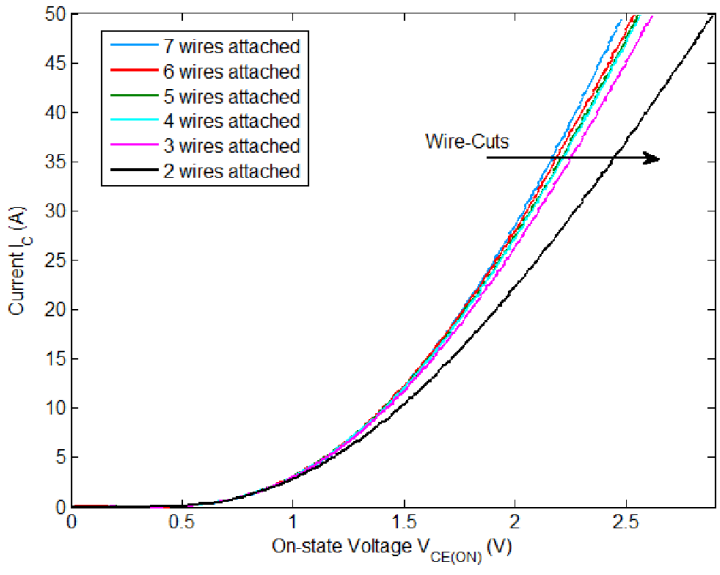


Figure 5.5 I-V characteristic of a single chip IGBT module shows correlation of $V_{CE(ON)}$ to wire-bond failures

On the other hand, the correlation of $V_{CE(ON)}$ to wire-bond failures is advantageous since it provides a mean to detect wire-bonds failures. But in order to enable this detection, the effect of junction temperature T_J on the measurement of $V_{CE(ON)}$ should be removed from the measured value of $V_{CE(ON)}$ so that information regarding the health state of wire-bonds can be isolated from the temperature effect. This implies the necessity to obtain information about junction temperature T_J from another source which is not correlated to wire-bond failures.

Among the reviewed TSEPs presented in Section 3.3.3, threshold voltage V_{th} is chosen as a TSEP to resolve junction temperature T_J information because of its good temperature correlation characteristics and its independence of wire-bond failures.

5.4 **Threshold Voltage V_{th}**

Threshold voltage is the minimum gate-emitter voltage V_{GE} required to form an inversion layer in the P^+ substrate layer below the gate oxide (SiO_2) in the MOSFET region of the IGBT structure as shown in Figure 5.6.The inversion layer is the conducting channel which allows the current to pass from collector to emitter. When a positive voltage V_{GE} is applied at the gate the negative charges in the substrate are attracted towards the gate forming a depletion layer. When $V_{GE}<V_{th}$ the amount of charges are not sufficient to form that conductive channel. As the V_{GE} increases more negative charges congregate in the depletion region at the interface between the oxide and the silicon. When $V_{GE}=V_{th}$ the concentration of negative charges becomes sufficient to form a conductive channel that allows the collector current to pass to the emitter.

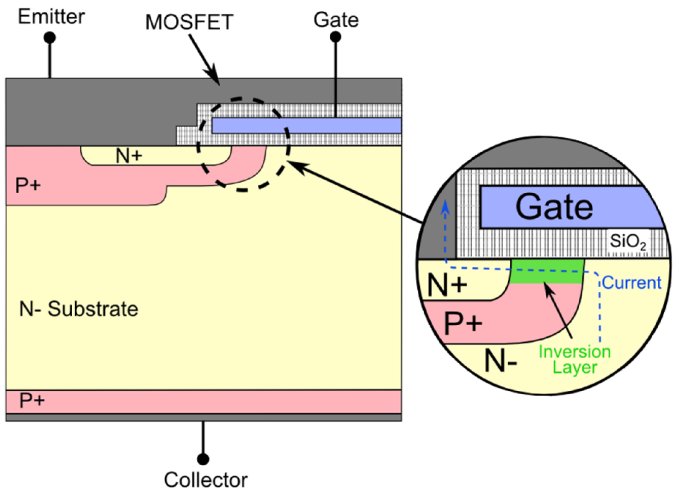


Figure 5.6 Formation of the inversion layer at the interface between Silicon and gate oxide SiO_2 causing collector current to flow

Threshold voltage can be defined from the transfer characteristic of the IGBT which describes the variations of device current I_C with gate-emitter voltage V_{ge}. Threshold voltage is defined as the x-intercept of the tangent of the transfer characteristic [130] as is explained in Figure 5.7.

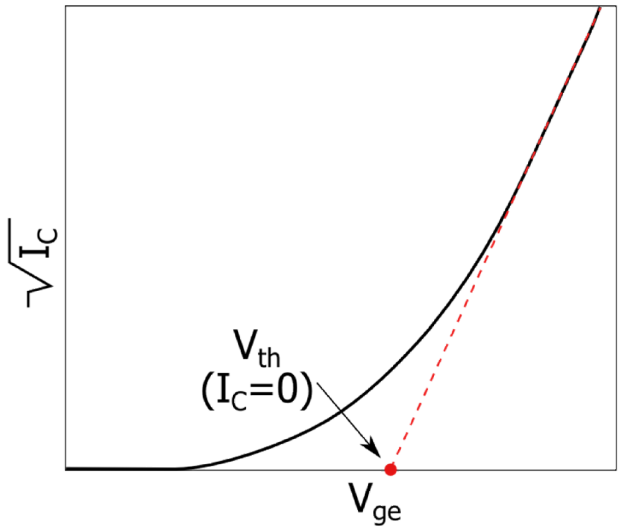


Figure 5.7 The extrapolation method to measure threshold voltage V_{th} from the transfer characteristic

5.4.1Temperature Dependency

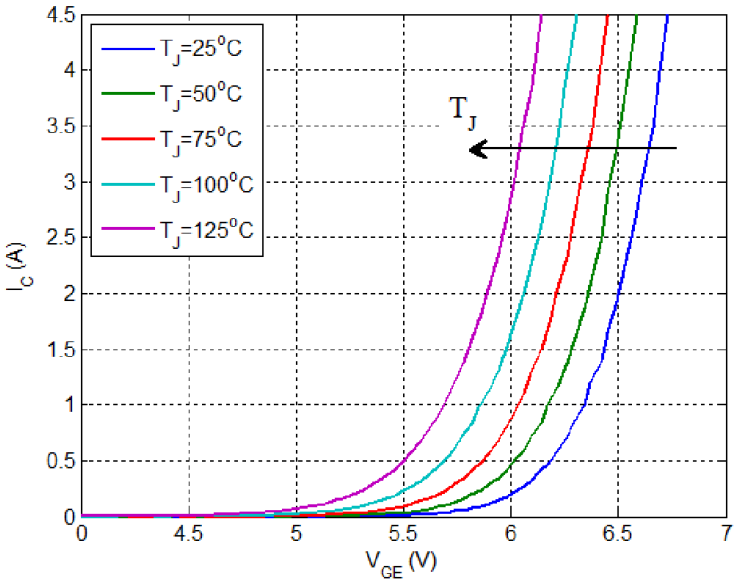


Figure 5.8 IGBT transfer characteristic at multiple temperatures shows correlation of threshold voltage to temperature

Variations of transfer chracteritic with temperature allows the threshold voltage V_{th} to be characterized as a function of temperature. For this purpose, an IGBT module is mounted on a temperature controlled hot plate and the transfer characteristic is obtained at muliple temperatures using a curve tracer. Figure 5.8 shows the linear region of the transfer characteristic at multiple temperartures. As can be seen the current starts flowing at lower gate-emitter voltage V_{ge} as temperature increases. That is, gate-emitter voltage V_{ge} has a negative temperature coefficient in the linear region. Threshold voltage V_{th} can be extracted from this data using the extrapolation method explained in the previous section. Figure 5.9 shows the extracted threshold voltage as a function of temperature. It is clear that V_{th} is linearly dependent on temperature with a slope of -6mV/^{o}C for the specific IGBT under test.

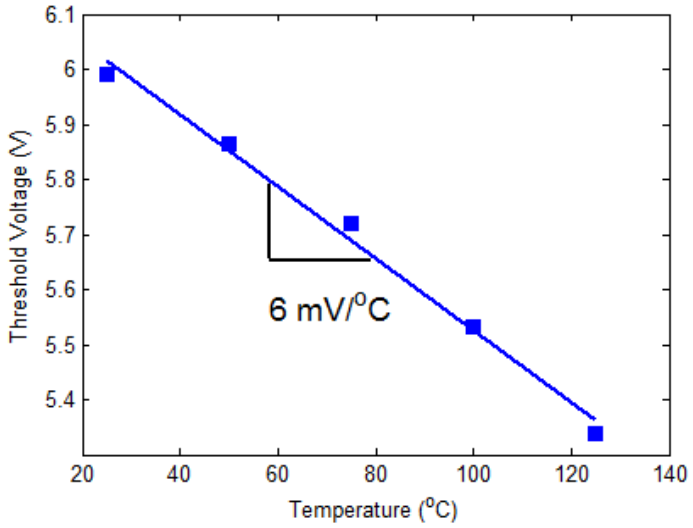


Figure 5.9 Correlation of Threshold voltage V_{th} to temperature as measured from the transfer characteristic

The effect of temperature on threshold voltage can be explained by considering the following formula which describes threshold voltage V_{th} as a function of gate structure parameters [113]:

$$V_{th} = V_{FB} + 2\Psi_B + \frac{\sqrt{2\varepsilon_S q N_A (2\Psi_B - V_{BS})}}{C_{OX}} \qquad \textbf{(5.2)}$$

where V_{FB} is the flatband voltage which is the voltage across the gate oxide at the flatband condition [113]. ψ_B is the Fermi potential, ε_s is the dielectric constant of the silicon, q is the elementary charge, N_A is the doping concentration, C_{OX} is the oxide capacitance, and V_{BS} is the voltage across the substrate region of the MOS-structure. Most of the parameters in Equation (5.2) are independent of temperature except from Fermi potential ψ_B which can be described by the following expression [113]:

$$\Psi_B = \frac{kT}{q} \ln\left(\frac{N_A}{n_i}\right) \qquad \textbf{(5.3)}$$

The intrinsic carrier concentration n_i is positively correlated to temperature so that the bulk potential (which is the potential difference between the intrinsic and Fermi level of the semiconductor [113]) decreases with increasing temperature and hence, threshold voltage V_{th} has a negative correlation to temperature. Taking the derivative of Equation (5.2) in respect to

temperature gives the variation of threshold voltage to temperature which can be expressed by the formula assuming V_{BS}=0:

$$\frac{dV_T}{dT} = \frac{d\Psi_B}{dT}\left[\frac{1}{C_{OX}}\sqrt{\frac{\varepsilon_S q N_A}{\Psi_B}} + 2\right] \qquad \textbf{(5.4)}$$

This expression reveals an important fact about temperature sensitivity of V_{th}. It shows that oxide capacitance C_{OX} and doping concentration N_A controls temperature sensitivity of V_{th}. Those parameters can vary during fabrication process. Therefore, the sensitivity of threshold voltage to junction temperature T_J can vary between IGBTs from manufacturers or even within samples from the same production lot due to the variability in the fabrication process. Therefore, if V_{th} is used as a sensor of junction temperature, it is important to do a calibration for each individual IGBT module with temperature. According to [105] this temperature sensitivity of V_{th} can range between -2mV/^{o}C to -10mV/^{o}C for IGBT devices.

In addition to temperature correlation of V_{th}, it can be seen from Equation (5.2) that V_{th} is correlated to substrate bias voltage V_{BS}. This voltage is related to the collector-emitter voltage V_{CE} applied across the IGBT. Therefore, it is necessary to examine the correlation of threshold V_{th} to collector-emitter voltage varaitions.

5.4.2 Collector-Emitter Voltage Dependency

From Equation (5.2) the change in threshold voltage ΔV_{th} due to a change in V_{BS} can be derived. Considering threshold voltage V_{th} at zero bias voltage ($V_{BS} = 0$) and at a non-zero bias voltage ($V_{BS} \neq 0$) the difference can be expressed by [113]:

$$\begin{aligned}\Delta V_{th} &= V_{th}(V_{BS}) - V_{th}(V_{BS} = 0) \\ &= \frac{\sqrt{2\varepsilon_S q N_A}}{C_{OX}}\left(\sqrt{2\Psi_B - V_{BS}} - \sqrt{2\Psi_B}\right)\end{aligned} \qquad \textbf{(5.5)}$$

This expression suggests that threshold voltage V_{th} has a negative correlation to V_{BS}. Considering the IGBT structure shown in Figure 5.6, this negative correlation can be described by the fact that an inversion layer is formed as a result of the voltage difference between gate oxide and the

substrate region. Applying a positive voltage (V_{BS}>0) at the substrate implies less gate voltage to create the inversion layer and hence a smaller threshold voltage. In order to verify that, the transfer characteristic is measured at multiple collector-emitter voltages V_{CE} applied across the IGBT at room temperature. The test setup for this measurement is described in Appendix A.

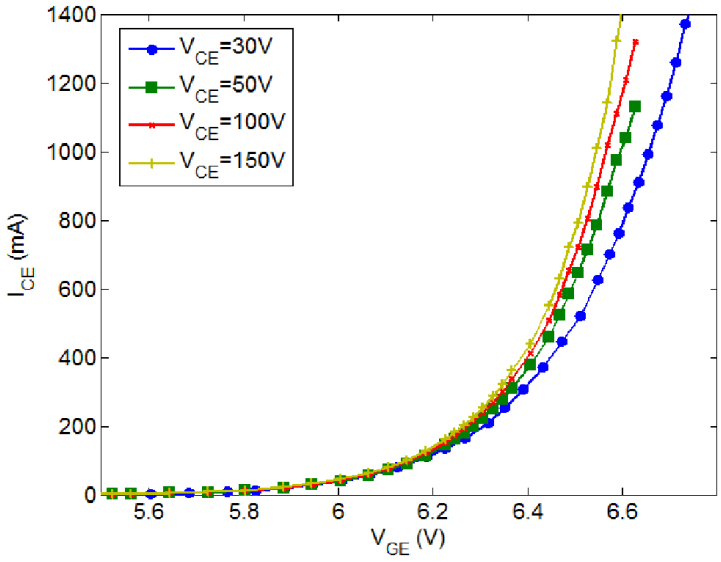


Figure 5.10 IGBT transfer characteristic at multiple collector emitter voltages V_{CE} shows correlation of threshold voltage to V_{CE}

Figure 5.10 shows the measured transfer characteristic at multiple V_{CE}. It can be seen that for a constant current I_{CE} the gate-emitter voltage V_{GE} is lower for higher V_{CE}. By using the extrapolation method described earlier, it can be seen that the x-intercept of the tangent which represents V_{th} decreases with increasing V_{CE}. This is in agreement with Equation (5.5).

This correlation of V_{th} to collector-emitter voltage V_{CE} should be considered during the calibration of V_{th} with temperature if DC link voltage varies largely in the power converter. However, in many power converters the ripple in DC link voltage is small and the effect it has on V_{th} can be considered negligible. Therefore, it is sufficient to calibrate V_{th} with temperature at a constant DC link voltage.

5.4.3 Dependency on Packaging Degradation

The effect of wire-bond failures on V_{th} is investigated by Zhou et al [131]. He showed by experiment that V_{ge} signal has no correlation to wire-bond failures during IGBT turn-on. An observable change can be seen only after a complete failure of the IGBT chip when all emitter wire-bonds are lifted off. This is described in Figure 5.11.

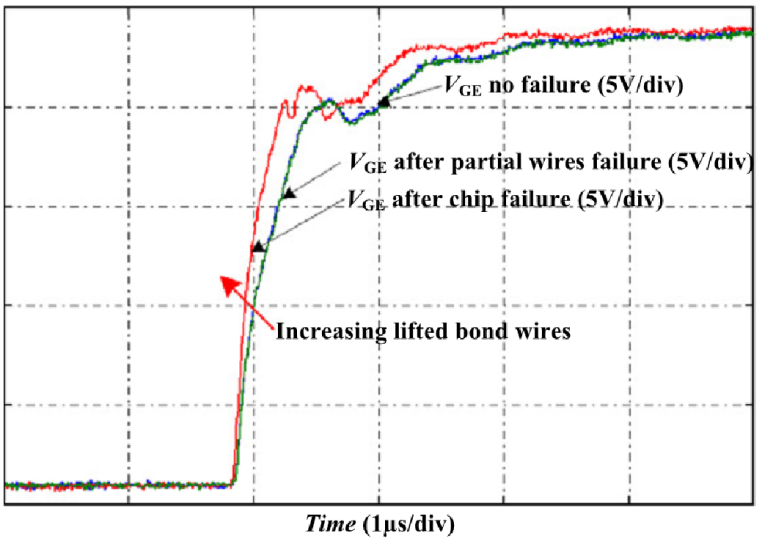


Figure 5.11 Gate-emitter voltage V_{ge} at IGBT turn-on shows no correlation to wire-bond failures. Only a complete chip failure results in a change of V_{ge} [131]

This result suggests that V_{th} can provide a consistent measurement of junction temperature T_J over the lifetime of the IGBT power module. Wire-bond failures will not affect the information of T_J resolved from V_{th} as it is the case with $V_{CE(ON)}$.

5.5 Discussion on the Effect of Measurement Noise on the Resolved T_J

The linear correlation to temperature of V_{th} is an advantage in the presence of measurement noise compared to the nonlinear correlation of $V_{CE(ON)}$ w.r.t current. This makes V_{th} a better TSEP if compared with $V_{CE(ON)}$. This can be explained by noting that the sensitivity of V_{th} to temperature is found to be -6mV/^{o}C. For example, if the measurement noise for V_{th} is 20mV peak-to-peak that accounts for 3.33^{o}C peak-to-peak noise in the resolved T_J.

Whereas for $V_{CE(ON)}$, the nonlinear correlation between T_J and I_L has a nonlinear effect on the resulting noise in the resolved T_J. For example, it was found that at 8A the sensitivity of $V_{CE(ON)}$ to T_J is 1.23mV/^oC whereas it is 2.68mV/^oC at 180A. For a 20mV peak-to-peak noise in $V_{CE(ON)}$ the output noise on the resolved T_J is 16.26^oC peak-to-peak at 8A whereas it is 7.46^oC peak-to-peak at 180A.

In other words, the signal-to-noise ratio (SNR) of the resolved T_J will vary with the current I_L if $V_{CE(ON)}$ is used as a TSEP due to the variable sensitivity of $V_{CE(ON)}$ to temperature T_J. This effect can be imagined as if noise is passing through an amplifier with a current dependent gain, so that noise characteristic changes as the current changes. At the inflection point and its neighbourhood (Figure 5.2), the resolved T_J becomes un-informative of the true T_J as sensitivity becomes very small in that region and goes down to zero at the inflection point. Therefore, the measurement signal of T_J becomes intermittent if current level varies over a wide range and therefore passes through the inflexion point as is typical in an inverter as an example. This does not apply to the threshold voltage V_{th} since it has a linear correlation to T_J and it is independent of I_C. Therefore, V_{th} can be considered as a better sensor for T_J than $V_{CE(ON)}$.

5.6 Comparison of $V_{CE(ON)}$ and V_{th} for T_J measurement and Health Monitoring

A comparison between on-state voltage $V_{CE(ON)}$ and threshold voltage V_{th} can be made according to the above. The aim of this comparison is to investigate the feasibility of using a combination of the two parameters for the heath monitoring of IGBT power modules such that discrimination between multiple failure mechanisms can be enabled. The two dominant failure mechanisms of wire-bond lift-off and solder fatigue can arise simultaneously in a power module and they give rise to different effects on $V_{CE(ON)}$ and V_{th} as described previously. Therefore, it is believed that proper combination of these two parameters can enable failure diagnosis.

A comparison between $V_{CE(ON)}$ and V_{th} is summarized in Table 5.1. In terms of temperature, it can be seen that threshold voltage V_{th} is a better sensor

for T_J than $V_{CE(ON)}$ since it has higher sensitivity and linear correlation to temperature and it is independent of loading current. In addition, it is insensitive to wire-bond failures which preserve the consistency of T_J estimate.

In terms of packaging degradation, both parameters $V_{CE(ON)}$ and V_{th} can be affected by solder fatigue due to their correlation to T_J. That is because solder fatigue degrades the thermal path and increases thermal resistance which results in an increment in T_J and consequently affect all TSEPs. On the other hand, $V_{CE(ON)}$ is affected by wire-bond lift-offs, and therefore it can be used as a sensor to examine the health state of the wire-bonds.

As a conclusion, it can be seen that $V_{CE(ON)}$ and V_{th} can provide useful information about temperature and health state of IGBT power modules. Through a proper combination of $V_{CE(ON)}$ and V_{th} data, the detection and discrimination of wire-bond failures and thermal degradation can be enabled. In order to obtain the data for $V_{CE(ON)}$ and V_{th} during normal operation of power converter, measurement circuits are required to enable online measurements. The following chapter discusses the development of the required measurement circuits.

Table 5.1 Comparison between $V_{CE(ON)}$ and V_{th} for T_J Estimate and Health Monitoring

		On-state Voltage $V_{CE(ON)}$	Threshold Voltage V_{th}
Temperature	Sensitivity	<3mV/^{o}C	6mV/^{o}C
	Linearity	Nonlinear	Linear
Operating Conditions	Current	✔	✘
	V_{CE}	✘	✔
Failure mechanisms	Wire-bond lift-off	✔	✘
	Solder fatigue	✔	✔

5.7**Summary**

This chapter focused on two thermos-sensitive electrical parameters TSEPs, the on-state voltage $V_{CE(ON)}$ and threshold voltage V_{th}. An extensive study on their correlation to temperature dependency, operating condition and failure mechanism has been presented based on theory and experiment. The dependence of these two parameters on temperature and wear-out mechanisms allows them to be used for health monitoring and junction temperature estimation.

Chapter 6 Online Measurement of On-State Voltage $V_{CE(ON)}$ and Threshold Voltage V_{th}

6.1 Introduction

In the previous chapter, the on-state voltage $V_{CE(ON)}$ and the threshold voltage V_{th} are investigated for their dependencies on temperature, operating conditions and packaging failures. This chapter achieves the online measurement of these two parameters during normal operation of power converter/inverter. Required measurement circuits are explained and tested experimentally. Then the online measurements are used to resolve junction temperature T_J information. The effect of measurement noise on the resolved T_J is investigated as well.

6.2 On-state Voltage $V_{CE(ON)}$ Measurement Circuit

6.2.1 Circuit Design

Online measurement of the on-state voltage $V_{CE(ON)}$ during the normal operation of power converters is challenging. The voltage across the IGBT device has a wide dynamic range (between DC link voltage and on-state voltage) and must be measured with millivolts accuracy. Precise timing, synchronized to the device switching instants, is required in order to capture a consistent representation of $V_{CE(ON)}$. In addition, electrical isolation is required between power converter and the data processing end-point. Therefore, a dedicated measurement circuit is developed to meet these requirements. Figure 6.1 shows a simplified schematic of the measurement circuit. A detailed schematic can be found in Appendix B.

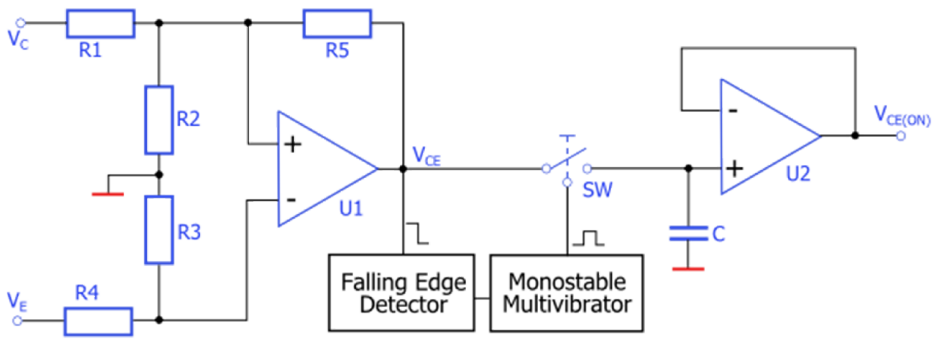


Figure 6.1 A Simplified Schematic of the Online Measurement Circuit of $V_{CE(ON)}$

The voltage dividers at the input of the op-amp U1 scale down the input voltage to acceptable values of the op-amp. For additional protection, ESD diodes internal to the U1 op-amp are used to protect the inputs of the op-amp from voltage spikes higher than its input range. The differential amplifier U1 is used to capture the collector-emitter voltage V_{CE} across the IGBT device. The amplifier output which represents V_{CE} signal goes into a timing circuit which includes a falling-edge detector and a monostable multivibrator. The function of this timing circuit is to generate the sampling signal in synchronous with the switching signal. The falling edge detector detects the IGBT turn-on by the falling edge of V_{CE}. This in turn triggers the monostable multivibrator to generate a pulse with a controllable width and a controllable delay time from the falling edge of V_{CE}. A sample and hold (S/H) circuit picks up a sample of V_{CE} 100us after the falling edge of the transient in V_{CE}, so giving enough time for this value to stabilize. This time can be tuned by choosing the appropriate components values of the timing circuit. This time should be larger than the minimum acquisition time of the used sample and hold circuit. Every switching cycle a single sample is captured and held until the next switching cycle. The sampled $V_{CE(ON)}$ signal is send through a capacitive isolator which provides the electrical isolation between the high voltage side of the power converter and the low voltage side of the PC-based data processing end-point. Further information on electrical isolation and its practical achievement is found in Appendix B. The circuit realization is shown in Figure 6.2.

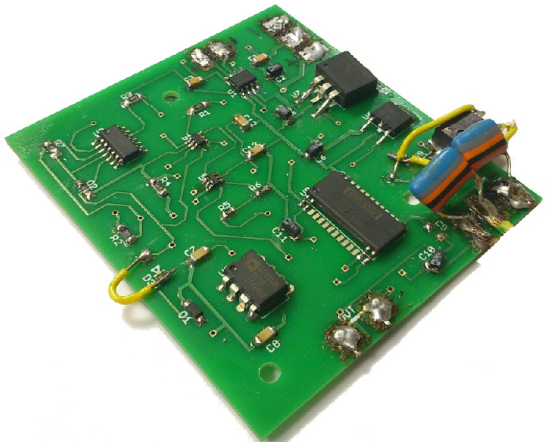


Figure 6.2 The Realization of the Online Measurement Circuit of $V_{CE(ON)}$

6.2.2 Circuit Testing

The circuit is connected across the collector and emitter terminals of an IGBT module in a double pulse test. Figure 6.3 explains the operation of the measurement circuit in a realistic switching cycle. The sampling signal (S/H) can be seen with a width of 100us and it is triggered after 10us delay time from the V_{CE} falling edge. The $V_{CE(ON)}$ sample is captured at the falling edge of the S/H signal. The knowledge of the current value at that instant is important for the translation of $V_{CE(ON)}$ measurement to junction temperature measurement. Therefore, current value is captured by the data acquisition system using a hall-effect sensor.

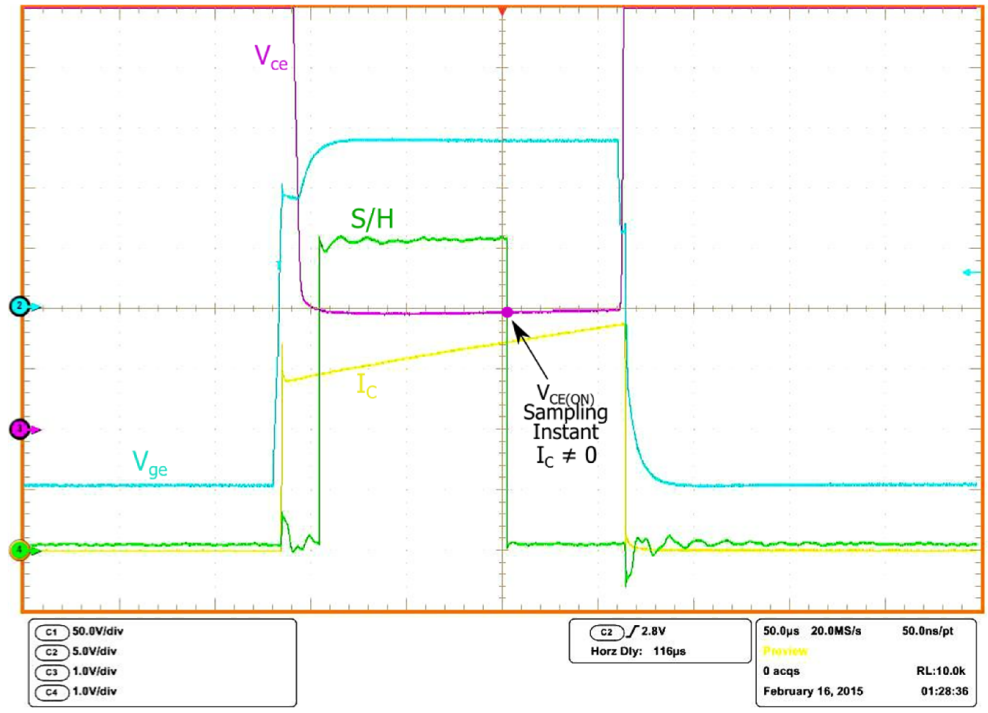


Figure 6.3 Measurement circuit operational waveforms of current I_C, gate-emitter voltage V_{ge}, collector-emitter voltage V_{CE} and sampling signal S/H used to capture $V_{CE(ON)}$

A calibration is required to obtain the input-output relationship of the circuit which allows translating the circuit output into the true input voltage. This is achieved by inputing a known voltage signal using a signal generator and measuring the output of the circuit. The input-output plot is shown in Figure 6.4 where a linear relationship with a slope of 1 and an offset of 5mV is observed.

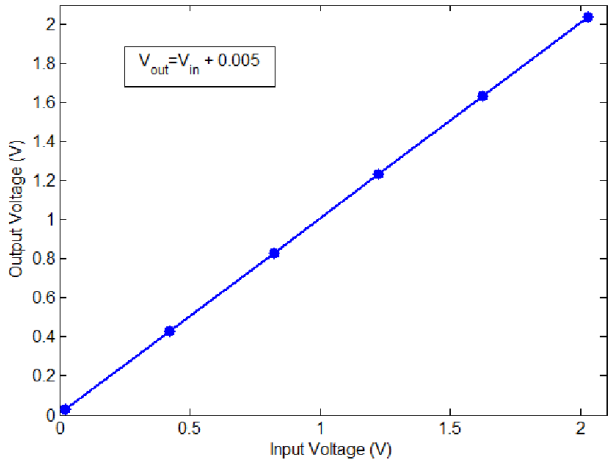


Figure 6.4 Input-Output relationship of the $V_{CE(ON)}$ measurement circuit shows a slope of 1 and an offset of 5mV

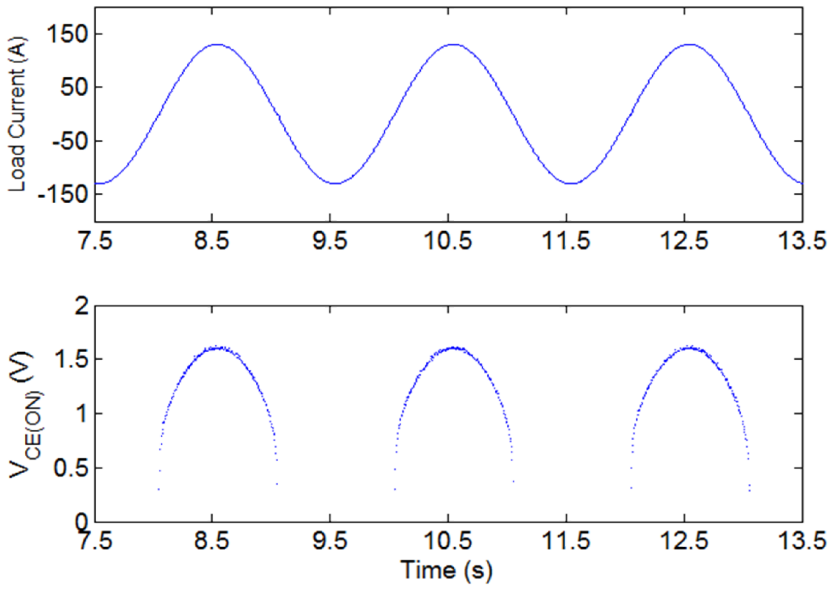


Figure 6.5 Online measurement of load current and $V_{CE(ON)}$ during inverter operation. $V_{CE(ON)}$ is measured using the proposed circuit.

In order to test the measurement circuit in a real application, the circuit is connected to the collector and emitter terminals of the high side IGBT of a half-bridge module. Figure 6.5 shows the experimental online measurement of the loading current and the corresponding $V_{CE(ON)}$ measurement obtained using the proposed measurement circuit. It can be seen that the $V_{CE(ON)}$ measurement signal follows the sinusoidal loading current and the high frequency component which originates from the switching frequency is removed ending up with the envelop of V_{CE} signal. Since $V_{CE(ON)}$ is a TSEP, the data shown in Figure 6.5 enables the junction temperature T_J to be resolved online using the data of $V_{CE(ON)}$.

6.2.3 Resolving Junction Temperature T_J from $V_{CE(ON)}$ Measurement

A look-up table is used to learn the forward characteristic of the IGBT shown in Figure 5.2 as a function $T_J=f(V_{CE(ON)},I_C)$. This function is used to resolve junction temperature T_J from the measurement of $V_{CE(ON)}$ and loading current. The look-up table is realized in MATLAB using the curve fitting tool *"cftool"* and the Linear Interpolation Method. The look-up table is shown in Figure 6.6. Other methods can be used to learn this relationship such as polynomials and neural networks.

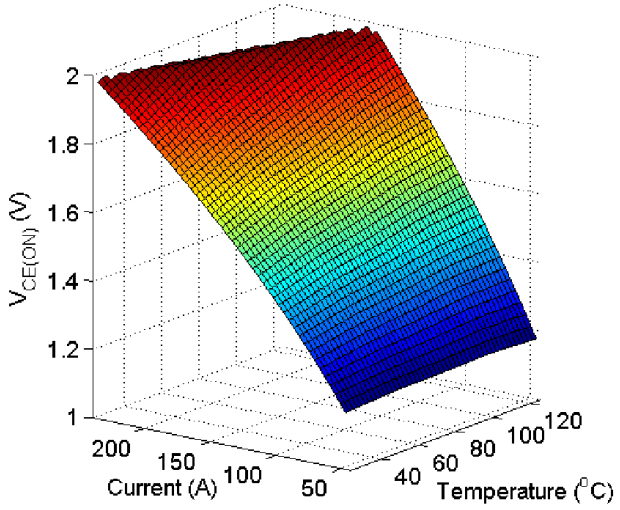


Figure 6.6 Look-up table used to resolve junction temperature T_J from measurement of current and on-state voltage $V_{CE(ON)}$

Figure 6.7 shows the measurement of T_J resolved from $V_{CE(ON)}$ and compared to the IR camera measurement along with the corresponding sinusoidal loading current and on-state voltage. Compared to IR camera measurement, T_J measurement signal exposes intermittency which happens when the current changes direction in the inverter. It should be noted that T_J measurement is available only when the current value goes above certain limit, in this case about 80A. This comes as a result of the inflection point where sensitivity of $V_{CE(ON)}$ to T_J becomes zero as described previously in Section 5.3.1. Around the inflection point the sensitivity is very low such that measurement noise dominates any useful information of T_J. Therefore, this limit can be determined experimentally by observing noise level in the resolved T_J.

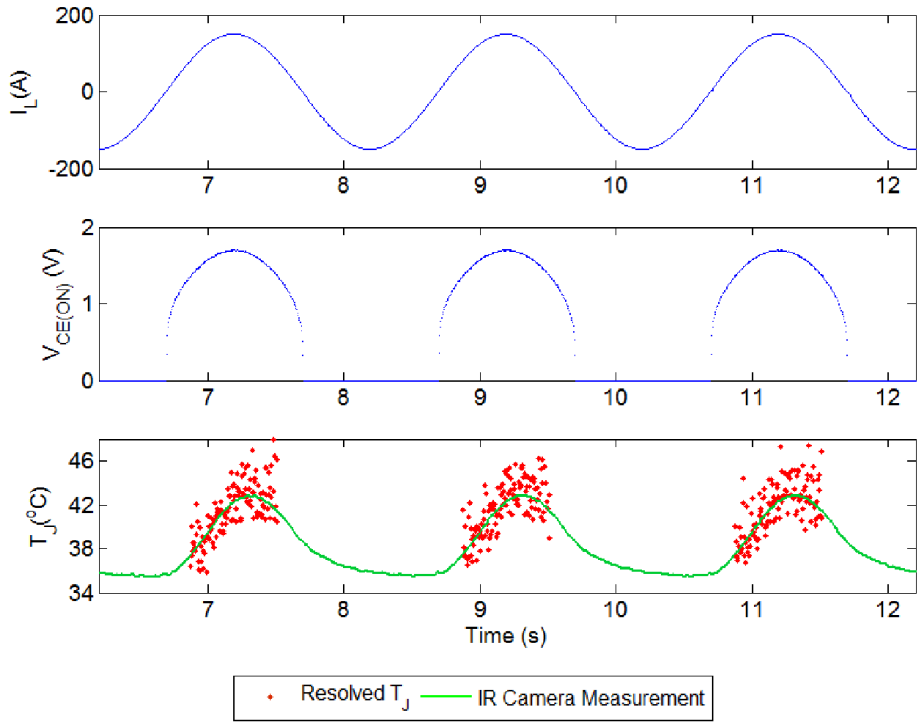


Figure 6.7 Online measurements of load current I_L, $V_{CE(ON)}$ and T_J measurement compared to IR camera measurement.

6.2.4 Noise Levels in the Measurement of $V_{CE(ON)}$ and the Resolved T_J

The resolved junction temperature T_J in Figure 6.7 shows a large spread compared to the IR camera measurement. This noise is inherited from measurement noise of $V_{CE(ON)}$. In order to measure the level of noise in $V_{CE(ON)}$, the experimentally collected data of $V_{CE(ON)}$ shown in Figure 6.7 is post-processed offline using a high-pass digital filter such that the low frequency component of the modulation sinusoid signal is removed. Only the high frequency noise remains after the high-pass filter is applied. The data sampling frequency used to collect the data is 200Hz.

Figure 6.8 shows the histogram of the measurement noise of $V_{CE(ON)}$. As can be seen, the noise data is Gaussian with a zero mean and a variance σ^2 of 10. That is 95% of the noise data lies between $\pm 2\sigma$ which is ±6.32mV. When $V_{CE(ON)}$ measurement translates into T_J this noise accounts to a spread in T_J with variable spread due to variable sensitivity of $V_{CE(ON)}$ as explained earlier in Section 5.5. The load current is sinusoid of amplitude of 150A. At a load current I_L=150A the sensitivity is 2.08mV/°C which accounts to a minimum

spread of ±3.04°C. At a load current I_L=80A the sensitivity is 0.832mV/°C which accounts to a maximum spread of ±7.59°C. This is confirmed by the histogram of the noise in the resolved T_J which is shown in Figure 6.9. The variance σ^2 for this data is 3.89 which mean that 95% of the noise lies between ±3.94°C.

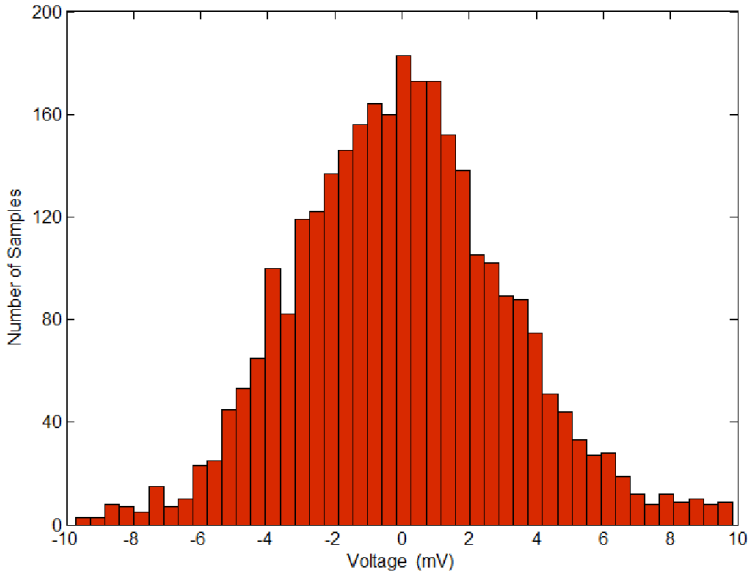


Figure 6.8 Histogram of the Measurement Noise of $V_{CE(ON)}$.

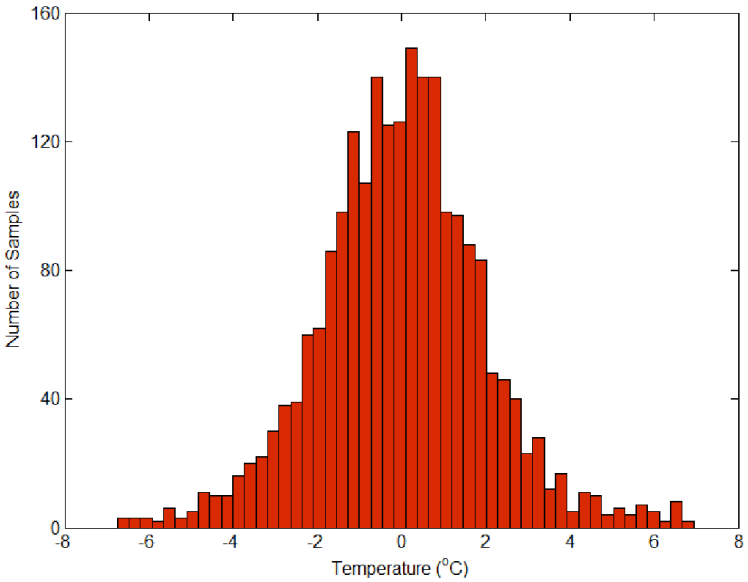


Figure 6.9 Histogram of the Noise in the Resolved T_J.

6.3 **Threshold Voltage V_{th} Measurement Circuit**

6.3.1 Circuit Design

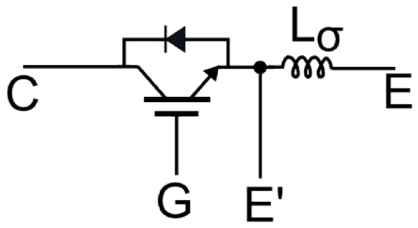


Figure 6.10 The packaging parasitic inductance L_σ between kelvin emitter E' and main emitter E

The method presented by Bahun [111] for online measurement of V_{th} is used to develop the measurement circuit. His work was presented in Section 3.4.2. The method is based on sampling gate-emitter voltage V_{ge} utilizing the di/dt event across the packaging parasitic inductance L_σ during IGBT turn-on. Figure 6.10 shows the packaging parasitic inductance L_σ used for this purpose which is present between Kelvin emitter (E') and main emitter (E) of the IGBT module. This parasitic inductance develops a voltage $V_{E'E}$ proportional to di/dt according to the following formula:

$$V_{E'E} = L_\sigma \times {di}/{dt} \qquad \textbf{(6.1)}$$

Figure 6.11 shows $V_{E'E}$ which can be measured between Kelvin emitter and main emitter along with the corresponding device current during IGBT turn-on. The sampling signal of V_{th} can be generated from $V_{E'E}$. Voltage $V_{E'E}$ is compared with a pre-calibrated reference voltage using a high speed comparator such that comparator output is triggered at the very beginning of $V_{E'E}$ development. This sampling signal informs a sample and hold circuit to capture the value of V_{ge} at the very beginning of current rise. The captured value of V_{ge} at that instant represents V_{th}. However, it is stated by Bahun [111] that the measured V_{th} using this method is higher than the true V_{th} value measured by other means (such as curve tracer). Therefore, the name "Quasi-Threshold Voltage" is used by Bahun [111] to refer to the measured V_{th}. No reasons are stated for this difference.

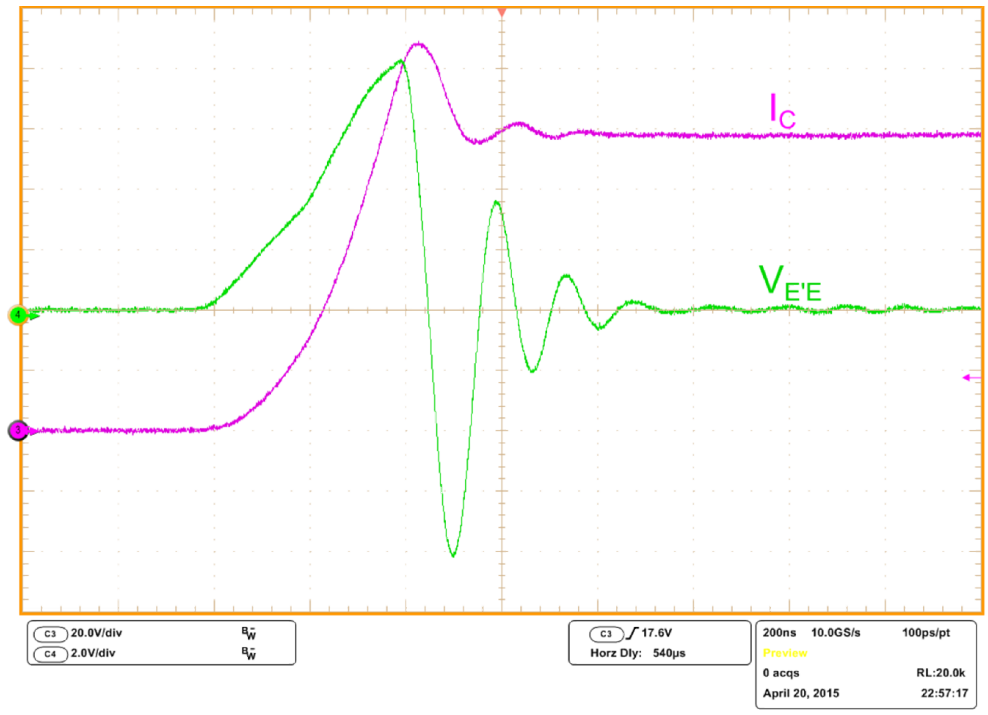


Figure 6.11 IGBT Device Current I_C and the $V_{E'E}$ Voltage Measured Across the Parasitic Inductance L_σ During IGBT Turn-on.

A simplified schematic of the proposed circuit is shown in Figure 6.12. A detailed schematic can be found in Appendix B. The voltage divider stage scales down the gate-emitter voltage V_{ge} using the resistors R1-R4. The capacitors C1-C4 are used to compensate for the parasitic capacitance of the resistors and to improve the frequency response of the voltage divider which prevents distortion of V_{ge} signal. An instrumentation amplifier U1 is then used to capture the differential voltage V_{ge}. The obtained V_{ge} signal goes into a track and hold circuit which is consisted of an analogue switch SW, a holding capacitor C5 and a buffer U4. The analogue switch SW has a response time of 5ns. The fast response of the switch SW is essential since V_{th} is captured during the dynamic transition of V_{ge} where V_{th} appears for a very small fraction of time. The high speed comparator U3 generates the triggering signal for the switch SW.

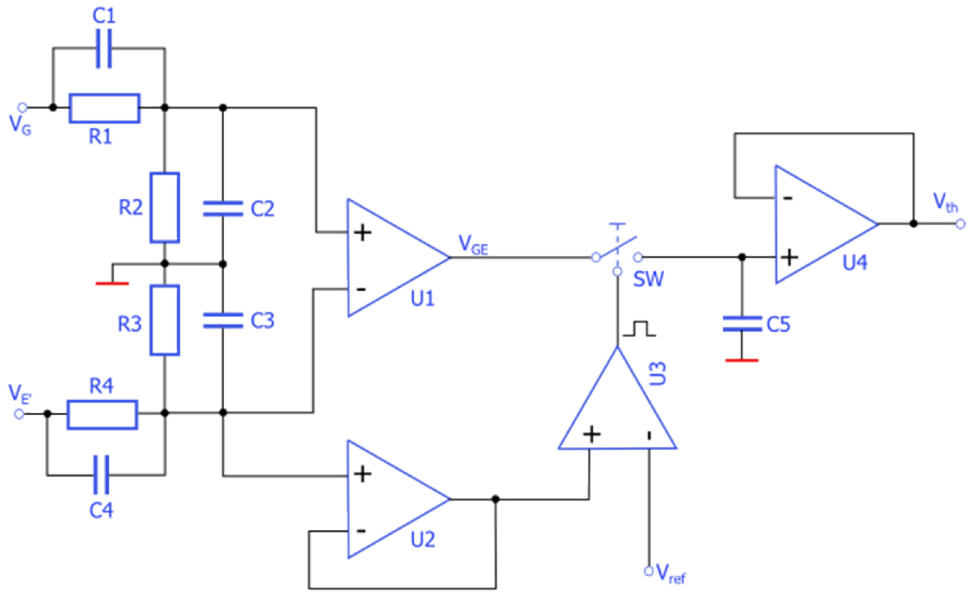


Figure 6.12 A Simplified schematic of V_{th} online measurement circuit

The circuit operates in two modes: track mode and hold mode. Before current rise (I_C=0), the switch SW is normally closed allowing the voltage of the capacitor C5 to track V_{GE}. Therefore, the output of U4 follows V_{ge} during the track mode. At the very beginning of current rise, the voltage $V_{E'E}$ starts to develop as it is proportional to di/dt. This voltage is captured by the buffer U2 and compared by U3 to a pre-defined voltage V_{ref}. When $V_{E'E}$>V_{ref} the high speed comparator U3 triggers the switch SW to open and stops tracking V_{ge}. At this point the voltage of the capacitor C5 represents the threshold voltage V_{th}. Hence, the output of U4 equals V_{th} in the hold mode.

Similar to $V_{CE(ON)}$ measurement circuit, an electrical isolation is required to interface V_{th} measurement circuit with the PC-based data acquisition system. This is implemented as described previously using a capacitive isolator. The realization of the circuit is shown in Figure 6.13.

6.3.2 Circuit Testing

In order to test circuit operation, a double pulse test is used. The operating waveforms are shown in Figure 6.14. The signal V_{th_sample} represents the output of the measurement circuit. It can be seen that V_{th_sample} signal tracks V_{ge} when (I_C=0) until the moment when current I_C starts rising. At that moment, the voltage $V_{E'E}$ develops and triggers the track and hold circuit to

stop tracking V_{ge} and holds its value at that instant. The held V_{th_sample} is then send through the isolation barrier and sampled by an ADC at the data acquisition system.

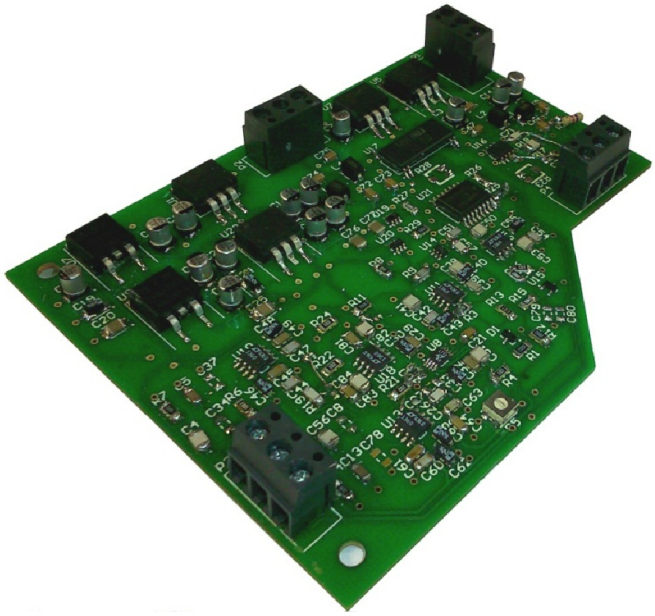


Figure 6.13 Realization of V_{th} online measurement circuit.

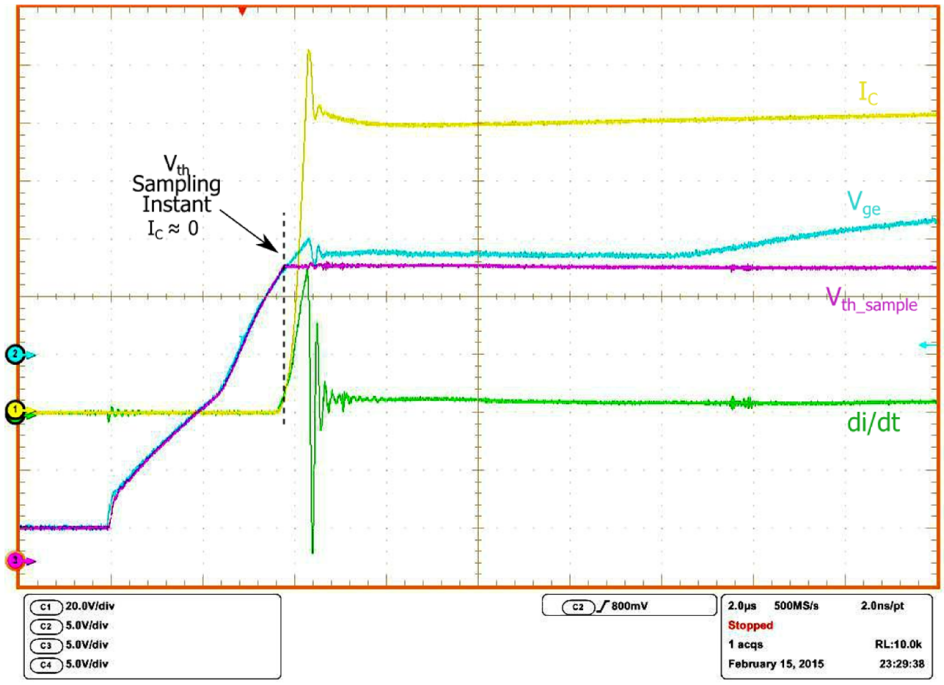


Figure 6.14 Measurement circuit operating waveforms. Current I_C, gate-emitter voltage V_{ge}, di/dt voltage used to sample V_{th} and the sampled threshold voltage V_{th_sample}.

It is very important to choose the components of the measurement circuit such that the response time of the circuit is minimized. This time is composed of the op-amps propagation delays and the response time of the analogue switch SW. The response time should be minimal in order to minimize the measurement error since the value of V_{th} is sampled from a dynamic signal V_{ge}. A slow response time can miss the moment when V_{th} should be captured.

The input-output calibration of V_{th} measurement circuit can be done using a signal generator where a known input voltage is given at the circuit input and the output voltage is measured. This calibration is required to translate the output voltage back to its true V_{th} value. This calibration is shown in Figure 6.15.

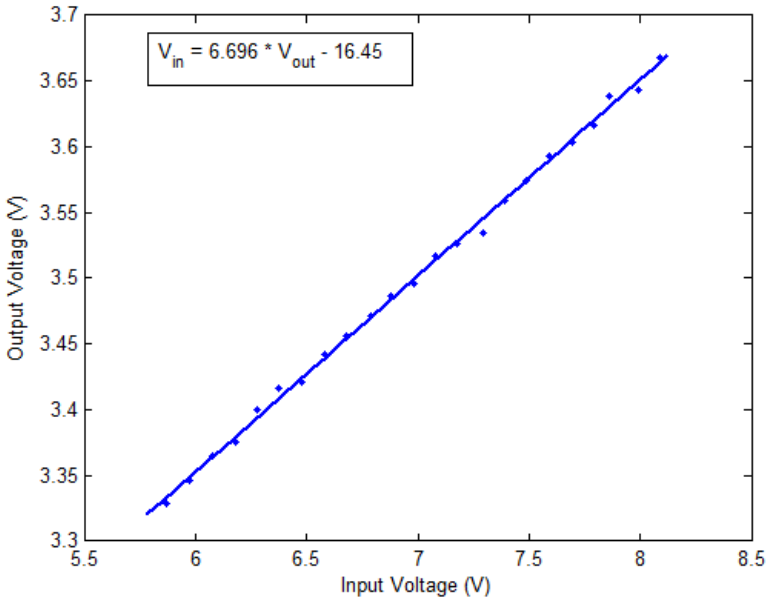


Figure 6.15 Input-Output relationship of V_{th} measurement circuit.

6.3.3 Effect of Gate Resistance on the Measured V_{th}

The measurement of V_{th} obtained from the proposed circuit seems to be higher than that measured by the curve tracer which agrees with the finding stated by Bahun [111]. The reason of this offset is thought to be a result of the dv/dt rate of the V_{ge} signal and the response time of the measurement circuit. This is investigated by obtaining the measurement of V_{th} using the measurement circuit at multiple switching speeds. The gate resistance R_G at the

gate drive is changed to achieve different switching speeds. Table 6.1 shows the measured V_{th} at room temperature using multiple R_G. An increment in V_{th} can be seen as R_G decreases. A lower R_G means faster switching of the IGBT (i.e. higher dv/dt of V_{ge}). Faster switching results in higher value of the measured V_{th}. That means the sampling point position is changing relative to V_{ge} waveform resulting in a higher value of V_{th}.

Table 6.1 Measured V_{th} at multiple gate resistances R_G at room temperature. VDC=100V, IC=100A

Gate Resistance R_G	Measured V_{th}
33R	7.664V
15R	7.948V
4.7R	8.491V

6.3.4 Resolving Junction Temperature T_J from V_{th} Measurement

In order to resolve junction temperature T_J of the IGBT from the measurement of V_{th}, a calibration of V_{th} against temperature is required. This calibration is done using a modified double pulse tester described in Appendix A. V_{th} is measured at multiple temperatures using the measurement circuit. 50 readings of V_{th} are recorded and averaged to eliminate noise effect. Since the current I_C is not exactly zero at the moment when V_{th} is sampled, the calibration is done at multiple current values to examine the effect of the current on the measured value of V_{th}. Figure 6.16 shows the calibration curve for V_{th} against temperature. All testing is done at a DC link voltage V_{DC}=100V and a gate resistance of R_G=20Ω. A linear relationship between temperature and V_{th} can be seen with a slope of -6.09mV/^{o}C. The effect of different current values is negligible on the measurement of V_{th}. This result is in good agreement with the calibration done previously in Chapter 4 using a curve tracer. The linearity and the sensitivity of 6mV/^{o}C are preserved.

In order to test the measurement circuit in a real application, it is connected to the full-bridge inverter presented in Appendix A. Figure 6.17 shows the online measurement of loading current I_L, threshold voltage V_{th} and the resolved junction temperature T_J. The large spread in T_J measurement is

because of the noisy measurement of V_{th} which is used as a sensor for T_J. V_{th} data is converted into T_J data using the calibration relationship show in Figure 6.16. The noise in V_{th} originates mainly from the working principle of the measurement circuit where V_{th} is captured from V_{ge} during its dynamic transition which increases variability in the captured value. In addition, noise in the triggering signal can affect the integrity of V_{th} measurement since false triggering leads to capturing value of V_{ge} at the wrong moment. Noise from the power converter working environment is also additive to the measurement signal. All these factors increase noise level in measured V_{th} and consequently in T_J measurement.

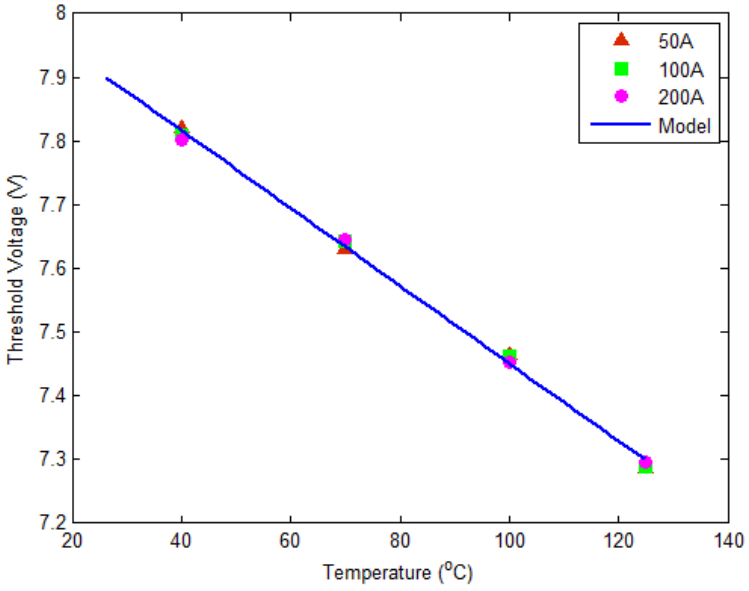


Figure 6.16 Temperature Calibration of V_{th} Measured using the Proposed Circuit.

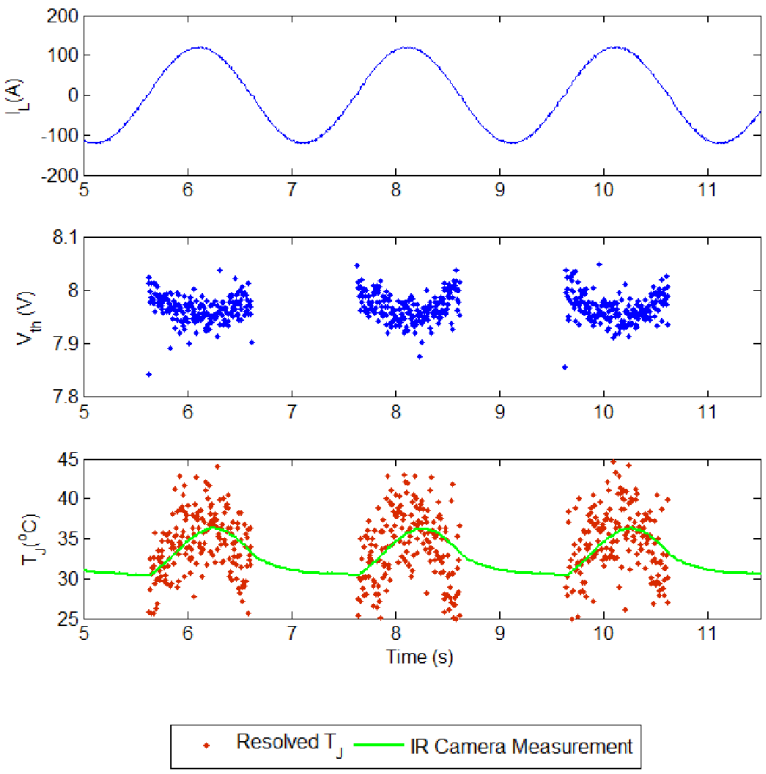


Figure 6.17 Temperature calibration of V_{th} measured using the proposed circuit.

6.3.5 Noise Levels in the Measurement of V_{th} and the Resolved T_J

Similar to $V_{CE(ON)}$ measurement, an offline post-processing is done on the measurement of V_{th} to measure the noise levels. The experimental measurement data of V_{th} is processed using a high-pass filter to extract the measurement noise. The data is collected using a sampling frequency of 200Hz.

The histogram of the measurement noise of V_{th} is shown in Figure 6.18. The noise has a Gaussian distribution with a zero mean and a variance σ^2 of 36. That is 95% of the noise is within a range of ±38mV. This accounts for a spread in the resolved T_J of ±6.23°C where the sensitivity is 6.09mV/°C. Figure 6.19 shows the histogram for the noise of the resolved T_J from V_{th} measurement. This shows a variance σ^2 of 14.72 which means that 95% of the noise in the resolved T_J lies between ±7.67°C which is close to the previously calculated range.

6.4 Discussion

Measurement noise levels in V_{th} (±38mV) are higher than that for $V_{CE(ON)}$ (±6.32mV). This is expected since V_{th} is a dynamic parameter and is more difficult to measure than $V_{CE(ON)}$ which is a static parameter. In other words, $V_{CE(ON)}$ is measured after the IGBT is turned on and the value of collector-emitter voltage V_{CE} is settled to a constant value which is the saturation voltage $V_{CE(ON)}$, whereas V_{th} is measured during the turn-on dynamic transition of gate-emitter voltage V_{ge}. The value of V_{ge} during this dynamic transition does not settle to a constant value.

It should be mentioned as well that in the V_{th} measurement circuit (Figure 6.12) the voltage reference V_{ref} used by comparator U3 to trigger the track and hold circuit can have an effect on the sampling point position. Noise levels in the circuit can prevent setting the reference voltage below a certain level which can result in an additional delay in the sampling process. In addition, noise on the voltage reference V_{ref} can result in false triggering of the sampling circuit which results in a larger spread in the measured V_{th}.

Comparing the noise in T_J resolved from $V_{CE(ON)}$ and that resolved from V_{th}, it can be seen that this noise is lower when $V_{CE(ON)}$ is used as a sensor with a spread of ±3.94^{o}C compared to a spread of ±7.67^{o}C when V_{th} is used as a sensor. However, the spread obtained with $V_{CE(ON)}$ is dependent on current and can become too large if the current becomes lower. Therefore, it is difficult to get a conclusive accurate estimate of the spread in T_J resolved from $V_{CE(ON)}$ since it is current dependent. This does not apply to V_{th} which is independent of current and therefore a conclusive estimate of noise level in the resolved T_J can be obtained.

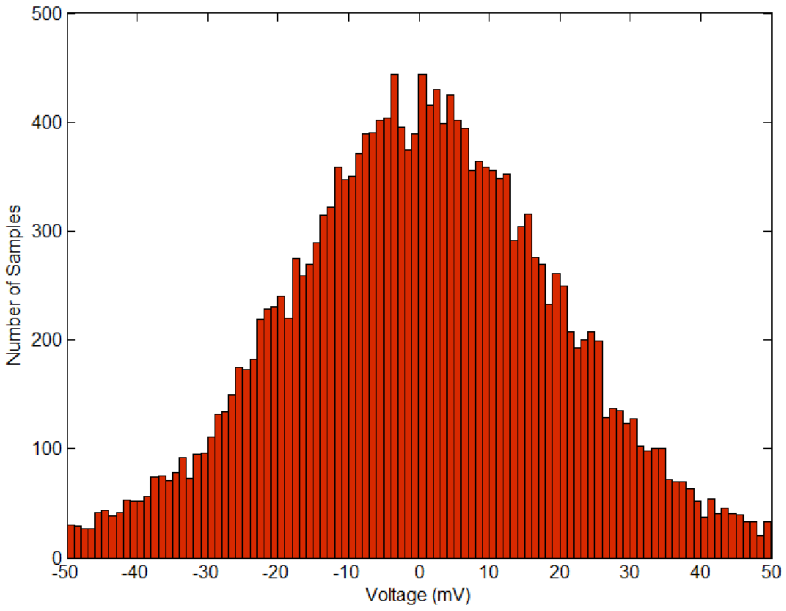


Figure 6.18 Histogram of the measurement noise of V_{th}

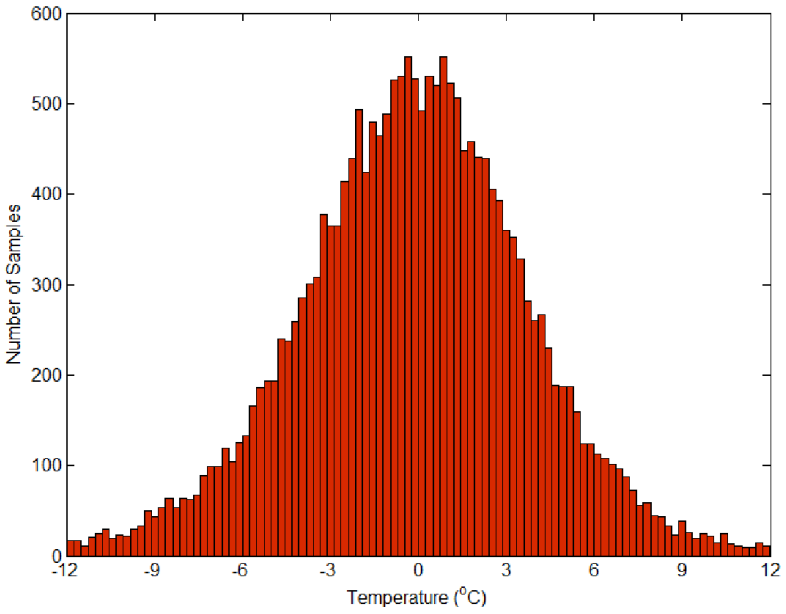


Figure 6.19 Histogram of the Noise in T_J Resolved from V_{th}

6.5 Summary

The online measurement of the thermo-sensitive electrical parameter $V_{CE(ON)}$ and V_{th} are presented in this chapter. Measurement circuits to allow the online measurement of these two parameters during power converter/inverter normal operation are developed and tested experimentally using a double pulse

tester and a full-bridge inverter. It is explained that the online measurement of these two parameters can be resolved into T_J measurement using appropriate calibration relationships.

The effect of measurement noise on the resolved T_J from both parameters is examined. It is concluded that V_{th} can be a better sensor for T_J compared to $V_{CE(ON)}$ because of its linear correlation to temperature and its independence from loading current even though the noise levels in the resolved T_J from V_{th} can be higher. However, in order to deal with the noise problem and achieve an improved accuracy from the TSEPs measurement which is important for accurate health monitoring, the next chapter explores through simulation and experiment the application of Kalman Filter to estimate junction temperature T_J.

Chapter 7 Simulation and Experimental Validation of Kalman Filter Algorithm for Real-time Junction Temperature Estimation

7.1 Introduction

The previous chapter explained the effect of measurement noise of the TSEPs on the resolved T_J. Measurement noise is typical in any power converter/inverter because of the harsh working environment. An accurate estimate of T_J is very important for health monitoring of power modules as it is a key failure indicator. Therefore, this chapter explores by simulation and experiment the application of Kalman Filter algorithm to improve the accuracy of the resolved T_J from a TSEP in order to be used later for health monitoring.

The following sections detail the development of the electro-thermal model and model parameterization using experimental data. Then the Kalman filter algorithm is applied and simulation results are presented. Finally, simulation results are confirmed by experimental results.

7.2 Development of the Electro-Thermal Model of IGBT Power Module

A MATLAB/Simulink model is developed to help study and develop the Kalman Filter algorithm for estimation of the junction temperature of IGBT power modules. The model describes the electro-thermal behaviour of an IGBT power module and it provides the possibility of simulating the on-state voltage $V_{CE(ON)}$ and threshold voltage V_{th} as thermo-sensitive electrical parameters (TSEPs).

Figure 7.1 shows a high level abstraction of the proposed electro-thermal model of the IGBT module. Each block contains many sub-blocks which will be detailed in the following sections. This model describes the electro-thermal behaviour of the IGBT module during the conductive state of the IGBTs as well as the conductive state of the freewheeling diodes in the power module. This model is a behavioural model constructed using common modelling techniques of power electronics such as Foster network for thermal

models and look-up tables for power dissipation and electrical models. Thermal modelling techniques were presented earlier in Chapter 3.

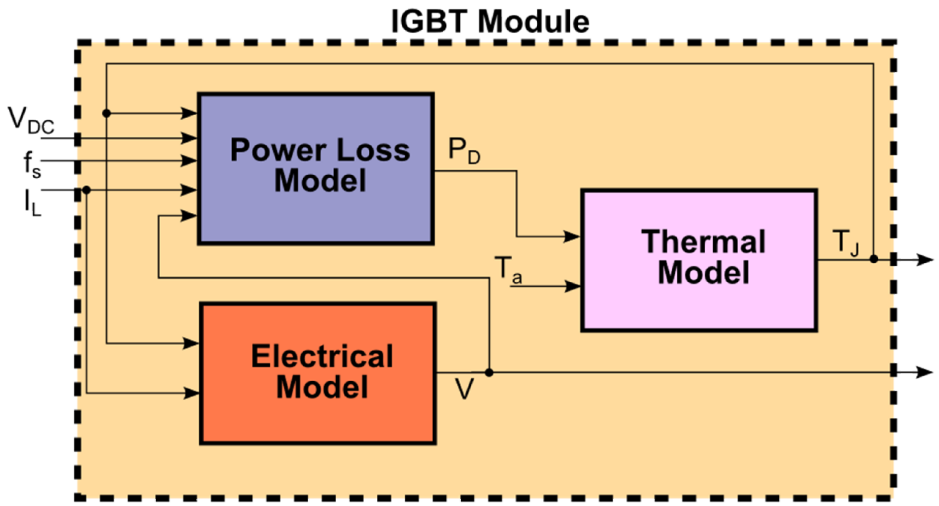


Figure 7.1 The electro-thermal model of an IGBT power module

The physics of the semiconductor devices are not used in the modelling process and therefore, the electrical switching characteristics are not modelled. However, switching losses during IGBT turn-on and turn-off plus diode reverse recovery are accounted for in the modelling.

The power loss model in Figure 7.1 contains two power loss models, one for the IGBT and another for the freewheeling diode. Therefore, the output of the power loss block is considered as a vector of two components $P_D=[P_{IGBT}, P_{DIODE}]$. The power loss model calculates the power dissipation resulting from conduction losses and switching losses utilizing loading current I_L, forward voltage V, junction temperature T_J, switching frequency f_s and the DC link voltage V_{DC} which is assumed to be constant.

Similarly, the thermal model in Figure 7.1 contains thermal models of the IGBT and freewheeling diode and its output T_J is a vector of two components representing the junction temperatures of the IGBT and the freewheeling diode $T_J=[T_{IGBT},T_{DIODE}]$. The thermal model is a behavioural model which describes the heat conduction path from junction to ambient. It captures the effects of self-heating of IGBT and diode and cross-coupling between them. It receives the power dissipation P_D and the ambient

temperature T_a as inputs and gives the junction temperature T_J asthe output. The junction temperature T_J is fed-back to the electrical model and the power loss model.

The electrical model consists of two electrical models, one for the IGBT and one for the diode. The output of this block is the forward voltage drop $V_{CE(ON)}$ of the IGBT and V_F of the diode where $V=[V_{CE(ON)},V_F]$. The electrical model describes the forward characteristic and its variation with temperature. It takes current I_L and junction temperature T_J as inputs and produces on-state voltage of the IGBT $V_{CE(ON)}$ and the forward voltage of the diode V_F.

7.2.1Thermal Model

7.2.1.1Thermal Description of the Power Module

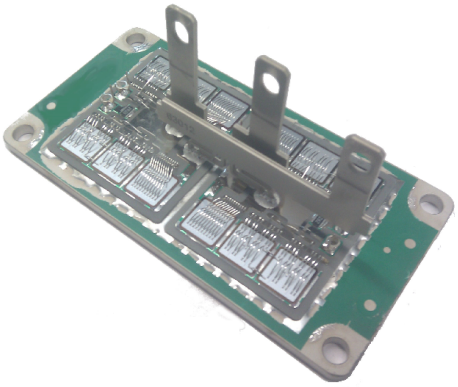
Typically in a power module multiple semiconductor chips are placed adjacent to each other and more than one substrate tile can be soldered to one baseplate in order to increase current capability of the module. Figure 7.2(a) shows the half-bridge module used in this work and which is considered for the modelling process. In this module, two substrate tiles are mounted on one baseplate. Each substrate tile has 4 IGBTs and 2 anti-parallel Diodes. Figure 7.2(b) shows the layout of this module and the location of the IGBT and diode chips on each substrate tile.

From a thermal perspective, adjacent semiconductor chips and adjacent substrate tiles have mutual or cross-coupling thermal effect. The heating of the IGBT chips on one substrate increases the temperature of the adjacent diode chips on the same substrate and vice-versa. Similarly, adjacent substrates sharing a common baseplate have a mutual thermal effect between each other and consequently the temperature rise on one substrate can thermally affect the chips on the adjacent substrate.

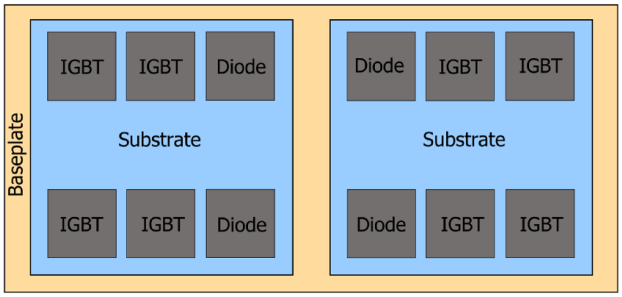
In this work, only one substrate of the half-bridge module is considered in the model. The other side can be considered a copy of it. Therefore, only the cross-coupling between diodes and IGBTs on the same substrate is considered whereas cross-coupling between substrates is neglected. Hence, the full

thermal description of one side of the IGBT module can be represented by four thermal impedances:

- Self-heating of the IGBT devices
- Self-heating of the freewheeling diode devices
- Cross-coupling between IGBT and diode
- Cross-coupling between diode and IGBT



(a)



(b)

Figure 7.2 (a) The IGBT power module used for modelling (b) The layout of the power module has two adjacent substrates on a common baseplate. Adjacent IGBT and Diode chips have a mutual heating effect

The complete thermal model of one-side of the half-bridge IGBT module is shown in Figure 7.3. The junction temperature of the IGBT devices T_{J_IGBT} is the summation of the IGBT temperature rise due to its self-heating and the temperature rise due to the Diode-IGBT cross-coupling. Similarly, the junction temperature of the freewheeling diodes T_{J_DIODE} is the summation of the diode self-heating and IGBT-Diode cross-coupling. All four thermal models (IGBT self-heating, Diode self-heating, IGBT-Diode cross-coupling,

Diode-IGBT cross-coupling) are described by Foster network models. The parameters of these thermal models are determined from experimental measurement by curve fitting.

7.2.1.2 Experimental Measurement of the Thermal Impedance

Experimental measurement of the step response of the heat conduction path is required for the parameterization of the Foster network. This measurement can be realized using a thermos-sensitive electrical parameter that can be used to measure the junction temperature of the semiconductor chip. On-state voltage $V_{CE(ON)}$ of the IGBT and forward voltage V_F of the diode are commonly used as TSEPs for thermal characterization of the heat conduction path.

A schematic of the thermal characterization setup is shown in Figure 7.4. Two current sources are used in the experiment. A high current source I_H for the purpose of heating and a low current source I_L for the purpose of measuring the voltage drop across the DUT which can be an IGBT or a diode. The low current source I_L provides a current on the level of milliamps to minimize the self-heating of the DUT during measurement. The power semiconductor package is mounted on a heatsink (cold plate) to remove the heat dissipated and to ensure the DUT reaches thermal equilibrium. The two current sources and the voltage measurement can be connected in any arrangement allowing the measurement and heating to be done on any combination such that self-heating and cross-coupling thermal impedances of IGBT or diode can be determined. The experimental setup is shown in Figure 7.5.

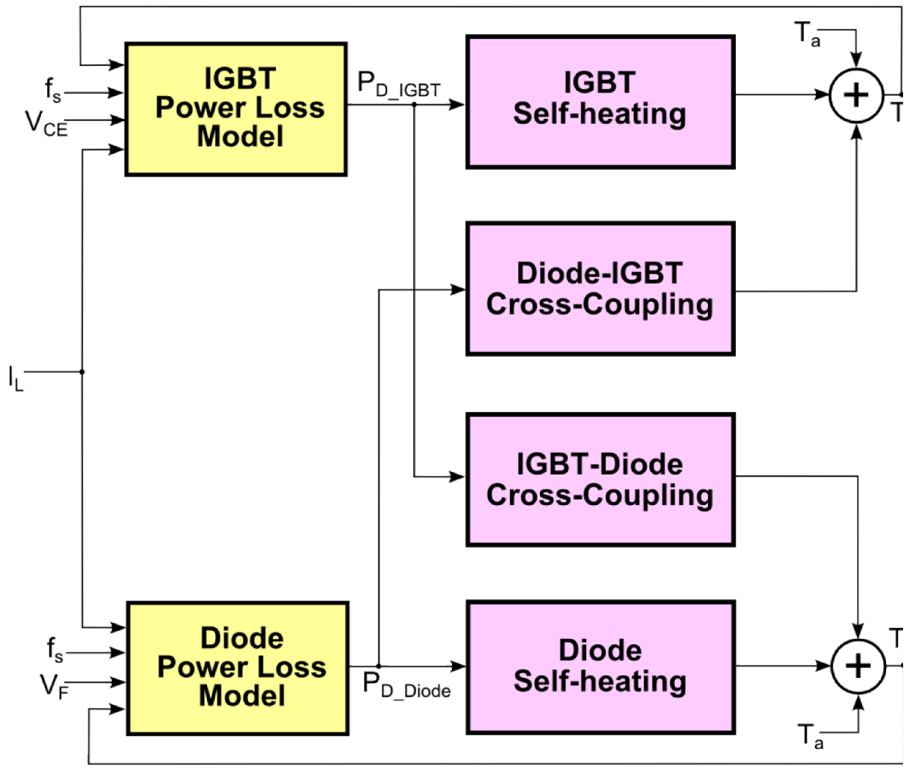


Figure 7.3 The full thermal model of IGBT power module. Power loss model inform thermal models of self-heating and cross-coupling of IGBT and Diode

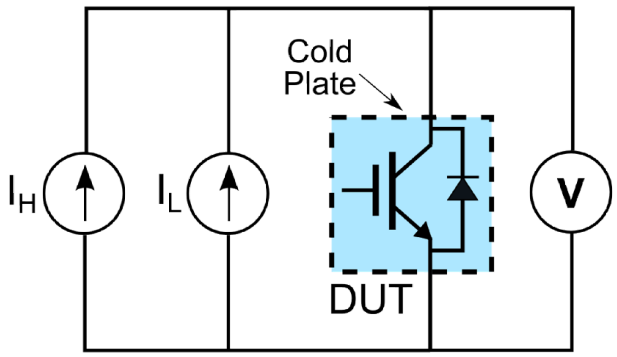


Figure 7.4 A Schematic for the Power Module Thermal Characterization Setup

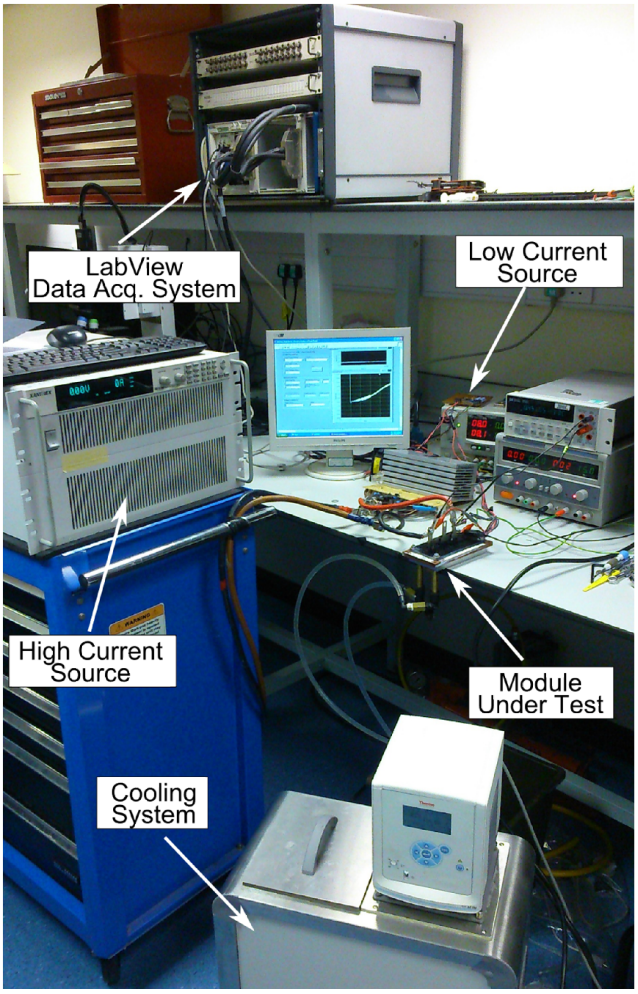


Figure 7.5 The Experimental Setup of the Thermal Characterization

The experiment for thermal characterization starts from the thermal equilibrium state of the power module at the coolant temperature. Then the high current source applies a heating current I_H which generates a step power input to the thermal system of the DUT and the temperature of the module starts to rise. During heating, the system reaches a second thermal equilibrium state and the high current source is switched off. The DUT starts cooling down. During this time the low current source I_L generates a voltage drop across the DUT which is continuously measured until thermal equilibrium is attained at the cold-plate temperature.

A calibration of the voltage with temperature is required in order to reconstruct the junction temperature measurement from the voltage measurement. This calibration can be done in a temperature controlled environment. The experimental setup to obtain the calibration curve is shown

in Figure 7.6. The calibration curves for the IGBT and the diode, measured at a current of 40mA, are shown in Figure 7.7. Table 7.1 shows the parameters used for the thermal characterization test of the IGBT and the freewheeling diodes of the tested power module.

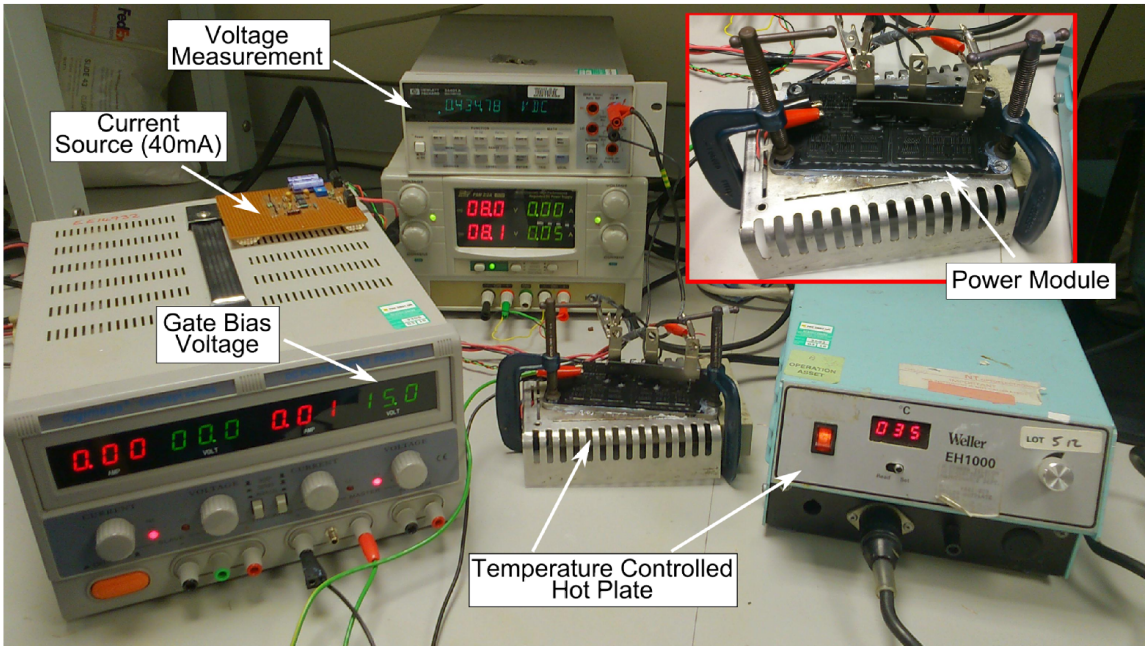


Figure 7.6 Experimental setup to obtain calibration curve $T_J=f(V_{CE})$

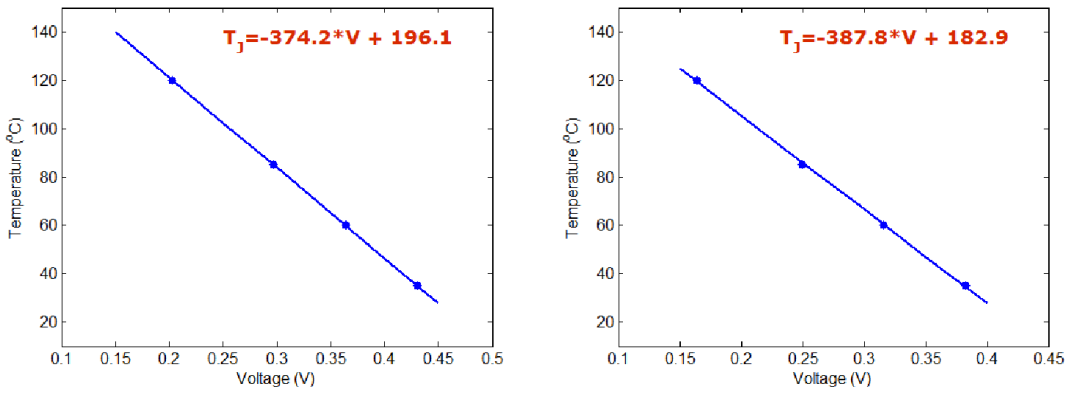


Figure 7.7 Calibration of Voltage with Temperature at 40mA for (a) IGBT (b) Diode

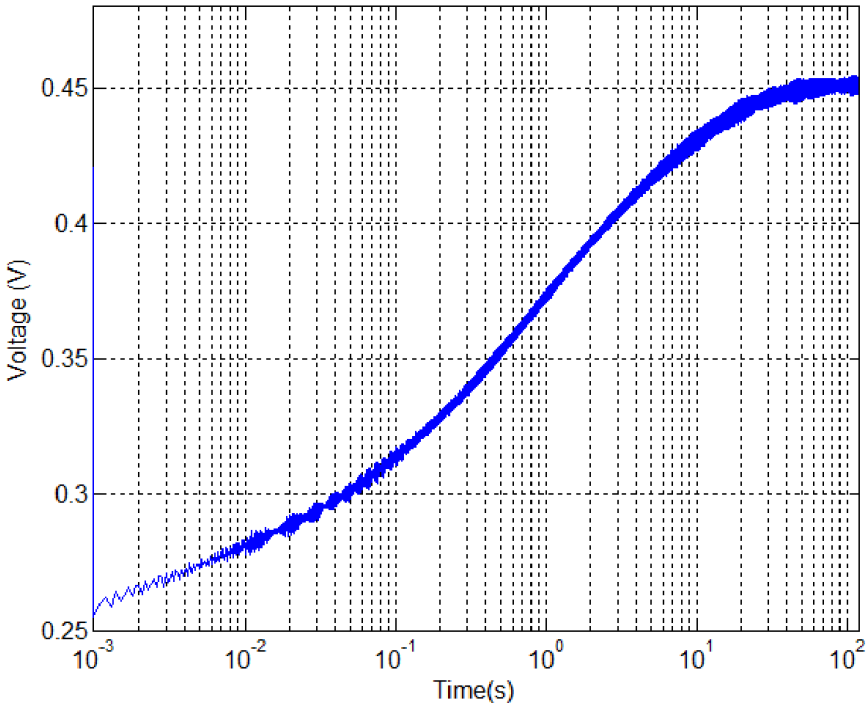


Figure 7.8 The raw voltage measurement data of the IGBT during cool-down transition

Table 7.1 Test parameters for thermal characterization of IGBT power module

	Current (A)	Voltage (V)	P_D (W)	Max. T_J (^oC)	Heating time (s)	Cooling Time (s)	Water Temp.(^oC)	Gate Bias Voltage (V)
IGBT	300	2.48	744	100	120	120	25	15
Diode	300	1.79	537	105	120	120	25	-15

Because of the module structure, shown in Figure 7.2, all calibration and thermal transient measurement are done across the four IGBT chips in parallel. The same applies for the two freewheeling diodes in parallel. The measurement process is repeated 10 times and averaged to reduce measurement noise. The raw data of the voltage measurement for the IGBT is shown in Figure 7.8. The data is plotted on a logarithmic time scale to reveal

the detail of the response across a wide range of time. Similar data can be obtained for the freewheeling diodes.

The raw voltage data shown in Figure 7.8 is resampled using a logarithmic time vector for the purpose of determining the Foster network model. Since the thermal system takes a relatively long time to approach steady-state and the dominant dynamics of the thermal system have short time constants, the logarithmic time vector allows the behaviour of the fast dynamics of the thermal system to be captured. The logarithmic-spaced time vector t_{ln} is generated as:

$$t_{ln} = e^{x} \tag{7.1}$$

where $ln(min(t))<x<ln(max(t))$ and $t \neq 0$ and t is the linear time vector.

The junction temperature is reconstructed from the voltage measurement using the calibration curve $T_J=f(V_{CE})$ in Figure 7.7. The ambient (coolant) temperature T_a is subtracted from the temperature data. The data is then inverted to obtain the heating curve which is assumed to be equivalent to the cooling curve [132]. The inversion is achieved by multiply all data points by (-1) and adding the $max(T_J)$ before inversion. The resulting temperature difference ΔT is then normalized by the power dissipation P_D to obtain the junction-to-ambient thermal impedance $Z_{\theta ja}$ of the heat conduction path:

$$Z_{\theta ja} = \frac{\Delta T}{P_D} \tag{7.2}$$

The resulting thermal impedance of the IGBT self-heating is shown in Figure 7.9. In the same way, the thermal impedances of Diode self-heating and cross-coupling are obtained.

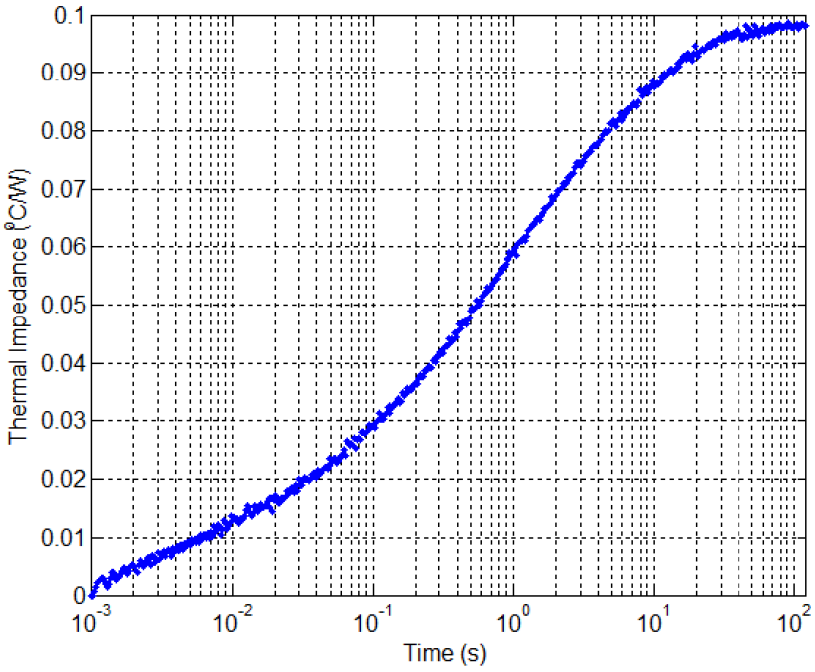


Figure 7.9 Measurement Data of the Junction-to-ambient Thermal Impedance Z_{0ja} of IGBT Self-Heating

7.2.1.3Parameterization of the Thermal Model

The values of the RC components of the Foster model in (3.8) can be identified from the experimental measurement of thermal impedance by curve fitting. A parameter identification process is carried out using the least squares algorithm in MATLAB. The function "*lsqnonlin*" is used to fit a Foster network model represented in (3.9) to the experimental data of the thermal impedance. The fitting residual produced by the fitting algorithm is used to determine the order of the model; the residual decreases with increased model order and converges to a constant value after a model order of 5 for the self-heating thermal impedances. Therefore the models of the self-heating impedances of the IGBT and freewheeling diode are chosen to be 5th order. Figure 7.10 shows the measured IGBT and diode self-heating impedances and the response of the fitted 5th order models. The fitting parameters are listed in Table 7.2.

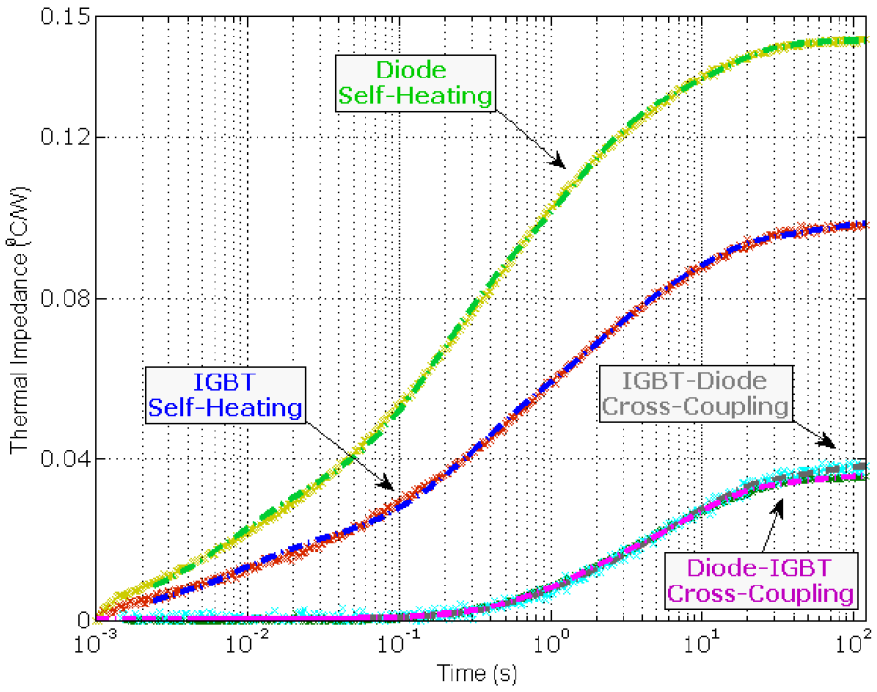


Figure 7.10 Measurements of Self-heating and Cross-Coupling Thermal Impedances compared to the response of fitted models

Similarly, the IGBT-Diode and Diode-IGBT cross-coupling impedances can be described by a Foster model as stated by Whitehead [133]. A 4th order model is found to give an acceptable matching with the measured cross-coupling impedance. Figure 7.10 also shows the measured IGBT-Diode and Diode-IGBT cross-coupling impedances and the response of the fitted 4th order models. The fitting parameters are also listed in Table 7.2.

According to [13], the parameters of a transfer function of a Foster network should satisfy a set of conditions: 1) its poles and zeros should lie on the real negative axis. 2) Poles and zeros must alternate on the real axis. 3) The nearest singularity to the origin must be a pole and the nearest singularity to infinity must be a zero. 4) The residues should be real and positive. Those conditions should be satisfied by the curve fitting algorithm during the identification process in order to generate positive values for RC parameters. Dissatisfying those conditions can result in imaginary values or negative values of RC parameters. This can affect the accuracy of the resulting model. In addition, some circuit simulators do not accept negative values for RC

components which prevents simulating the model.Those conditions can be satisfied by the self-heating impedance which results in positive values of RC components as can be seen in Table 7.2.

Table 7.2 Idenitfied parameter of Foster networks

		Term No.				
		1	2	3	4	5
IGBT Self-Heating	R	0.0165	0.0269	0.0233	0.0263	0.0068
	C	0.4764	8.745	57.731	249.10	8946.87
Diode Self-Heating	R	0.02508	0.04975	0.04613	0.02100	0.00212
	C	0.2680	3.1400	28.760	492.08	12852.6
DIODE-IGBT Cross-Coupling	R	-0.00342	0.01253	0.0225	0.0043	-
	C	-95.45	73.791	312.63	9217.84	-
IGBT-DIODE Cross-Coupling	R	-0.00309	0.00963	0.02557	0.00664	-
	C	-89.41	81.70	260.06	6885.89	-

However, in the case of cross-coupling thermal impedance those conditions cannot be satisfied because of the thermal propagation time which exhibit itself as an internal delay of the system. This thermal propagation time can be seen in Figure 7.10 at the beginning of the response and it can be estimated in this case by about 0.1s. Violation of the previous conditions results in negative values for the RC parameters which are seen in Table 7.2. This is acceptable since the Foster network is a behavioural model of the thermal system and its parameters have no physical significance.

7.2.2Power loss Model

7.2.2.4IGBT Power Loss

The total power dissipation in IGBT devices consists of conduction loss and switching losses. The conduction loss results from the ohmic resistance of the semiconductor device. The conduction loss P_{c_IGBT} is calculated by the multiplication of the loading current I_L and the on-state voltage of the IGBT $V_{CE(ON)}$:

$$P_{c\_IGBT} = V_{CE(ON)} \times I_L \quad \textbf{(7.3)}$$

where the on-state voltage $V_{CE(ON)}$ is obtained from the electrical model of the IGBT presented later in Section 7.2.3.

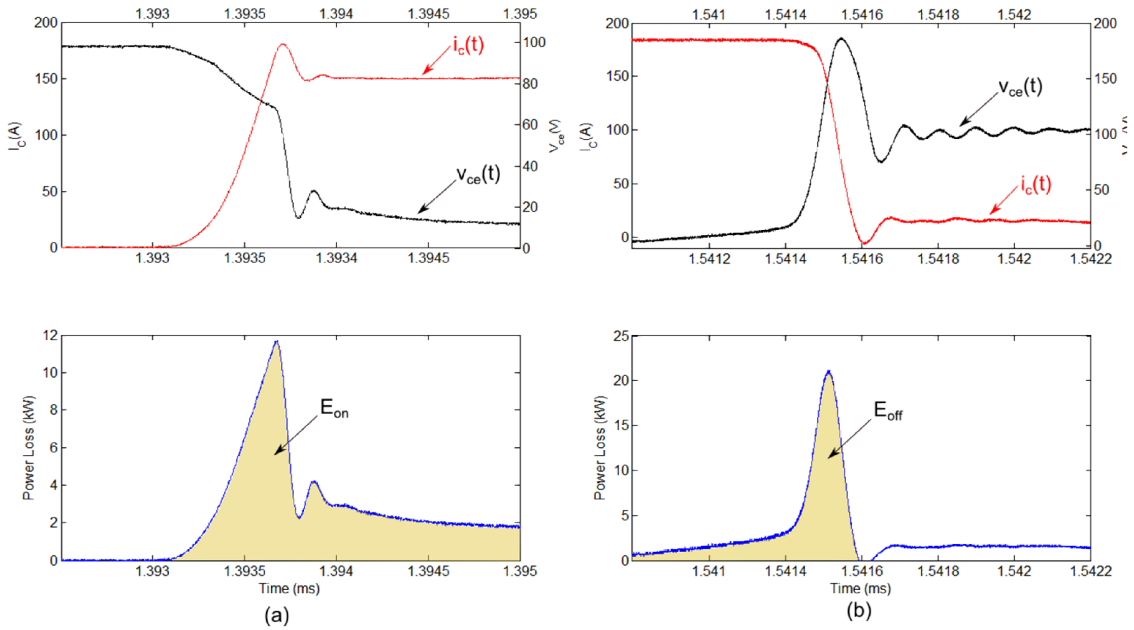


Figure 7.11 Current i_c and voltage v_{ce} switching waveforms used to calculate switching losses of the IGBT (a) turn-on loss (b) turn-off loss

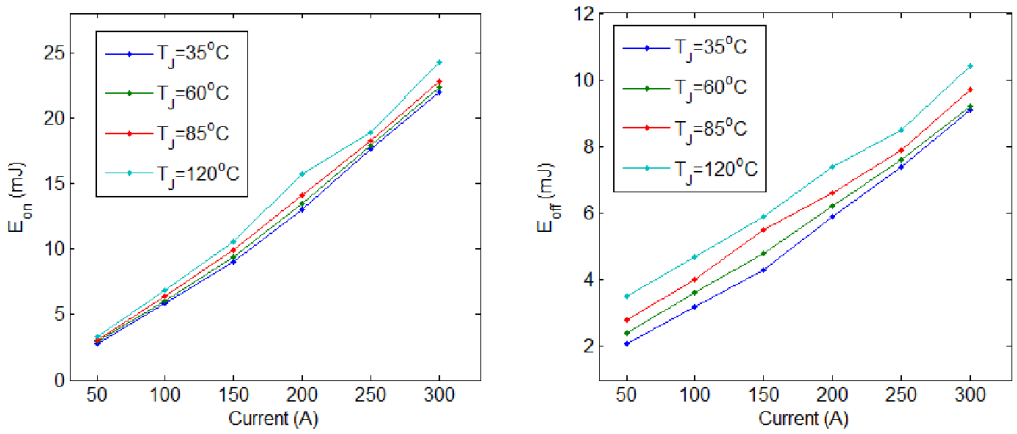
Switching losses result from the dynamic electrical characteristics of the IGBT during turn-on and turn-off events. Figure 7.11 shows typical switching waveforms of an IGBT device obtained experimentally with test conditions of V_{GE}=15V, R_G=10R and V_{DC}=100V. Figure 7.11(a) shows the current $i_c(t)$ and collector-emitter voltage $v_{ce}(t)$ waveforms of the IGBT during turn-on whereas Figure 7.11(b) shows the waveforms during turn-off.

Switching energies at turn-on E_{on} and turn-off E_{off} can be calculated by integrating the power dissipation which is the product of current waveform $i_c(t)$ and collector-emitter voltage waveform $v_{ce}(t)$ as shown in Figure 7.11. The switching energies are calculated as follows:

$$E_{on} = \int_{t1}^{t2} i_c(t) \times v_{ce}(t)dt \quad \textbf{(7.4)}$$

$$E_{off} = \int_{t3}^{t4} i_c(t) \times v_{ce}(t)dt \quad \textbf{(7.5)}$$

These energies are calculated at multiple currents and multiple temperatures by obtaining the switching waveforms of the IGBT experimentally using a double pulse test. The resulting values are tabulated to build look-up tables which constitute the model for switching losses calculation. Look-up tables are shown in Figure 7.12.



(a) (b)

Figure 7.12 Switching Loss energies at multiple temperature (a) turn-on loss energy (b) turn-off loss energy

The switching loss P_{sw} can be considered as an average power loss and it is calculated from the turn-on and turn-off energies E_{on} and E_{off} multiplied by the switching frequency f_s [134]:

$$P_{sw} = \left(E_{on} + E_{off}\right) \times f_s \tag{7.6}$$

Finally, the total power loss of the IGBT P_{IGBT} is the summation of switching loss P_{SW} and the conduction loss P_{c_IGBT}. The power loss model of the IGBT is shown in Figure 7.13.

$$P_{IGBT} = P_{c\_IGBT} + P_{sw} \tag{7.7}$$

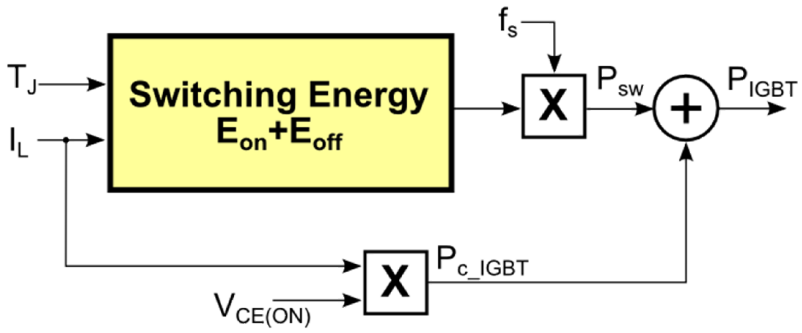


Figure 7.13 The IGBT power loss calculation block digram shows switching loss P_{SW} and condution loss P_{c_IGBT}

7.2.2.5Diode Power Loss

The power dissipation of the freewheeling diode P_{DIODE} consists of conduction loss and reverse recovery loss. The conduction loss is characterized by the forward characteristic of the diode and therefore it can be calculated as:

$$P_{c\_DIODE} = V_F \times I_L \tag{7.8}$$

where V_F and I_L are the forward voltage and the conduction current of the diode.

The reverse recovery behaviour of the diode happens when the diode turns from conducting state into blocking state. This behaviour is caused by the internal stored charge of the diode that has to be removed, resulting in reverse current flow through the diode. It is during this negative current phase where the reverse recovery loss is dissipated. Figure 7.14(a) shows typical current $i_f(t)$ and voltage $v_f(t)$ waveforms across the diode during reverse recovery event.

The reverse recovery energy E_{rr} is the time integral of reverse recovery power loss obtained by multiplying current $i_f(t)$ and voltage $v_f(t)$ waveforms as shown in Figure 7.14(b). Reverse recovery energy E_{rr} can be calculated as follows:

$$E_{rr} = \int_{t1}^{t2} i_f(t) \times v_f(t) dt \tag{7.9}$$

Current $i_f(t)$ and voltage $v_f(t)$ waveforms are obtained experimentally using a double pulse test at multiple currents and multiple temperatures.

Reverse recovery energy E_{rr} is calculated as in (7.5(7.9). The data is used to build a look-up table to enable the calculation of diode power loss in the simulation. Figure 7.15 shows the look-up table for the reverse recovery energy of the freewheeling diode.

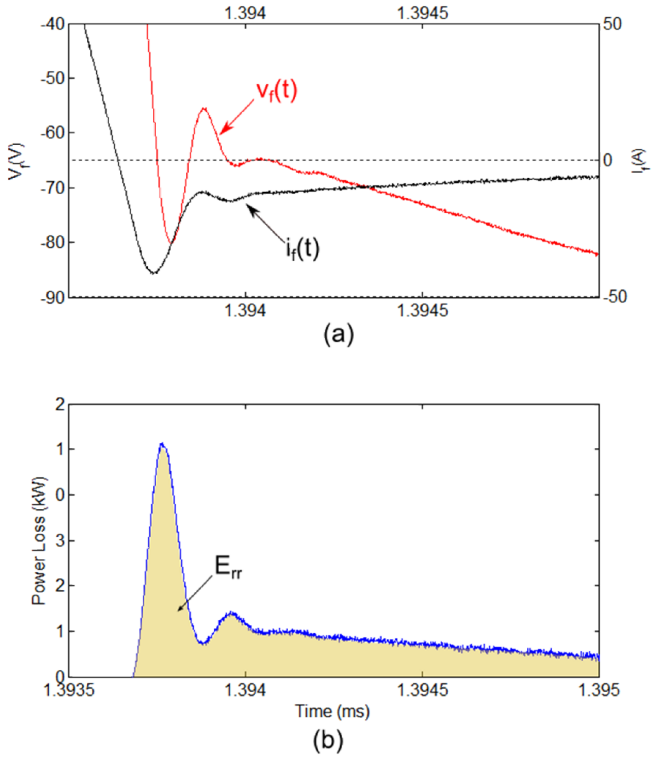


Figure 7.14 Reverse Recovery Loss of Diode (a) reverse recovery diode waveforms (b) reverse recovery power loss

The average reverse recovery power loss P_{rr} can be calculated by multiplying the reverse recovery energy E_{rr} by the switching frequency f_s:

$$P_{rr} = E_{rr} \times f_s \tag{7.10}$$

Consequently, the total power loss of the diode P_{DIODE} is the sum of conduction loss P_{c_DIODE} and the reverse recovery loss P_{rr}:

$$P_{DIODE} = P_{c\_DIODE} + P_{rr} \tag{7.11}$$

The power loss calculation model of the freewheeling diode is detailed in Figure 7.16.

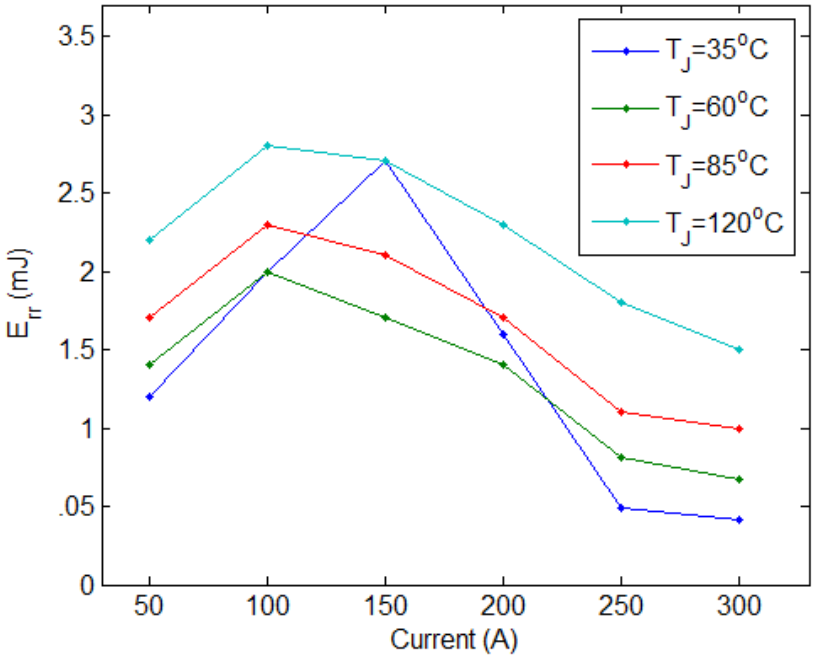


Figure 7.15 Diode Reverse Recovery Energy as a function of current at multiple temperatures

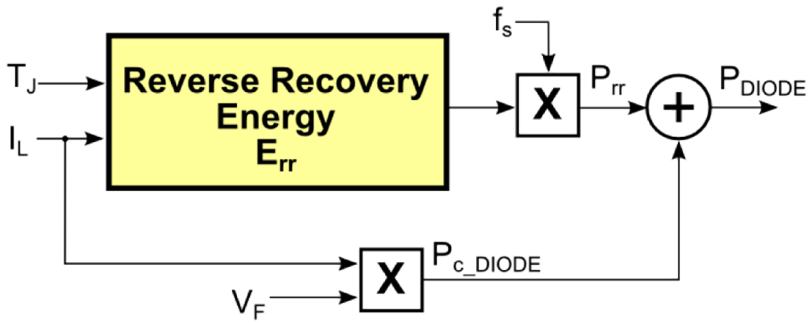


Figure 7.16 The Diode power loss calculation block digram shows reverse recovery loss P_{rr} and condution loss P_{c_DIODE}

7.2.3Electrical Model

7.2.3.6IGBT Electrical Model

The electrical model is required to simulate the behaviour of the forward I-V characteristic of the IGBT and to obtain the forward voltage drop. The forward I-V characteristic is obtained experimentally using a curve tracer at multiple temperatures and used to generate a look-up table $V_{CE(ON)}=f(I_L,T_{J\_IGBT})$ which represents the electrical model. The electrical

model receives loading current I_L and junction temperature T_{J_IGBT} as inputs and gives the on-state voltage $V_{CE(ON)}$ as an output. This voltage is used for the power loss calculation as described in Section 7.2.2 and as a TSEP to estimate the junction temperature T_{J_IGBT}. The look-up table for the I-V characteristic of the IGBT is shown in Figure 7.17.

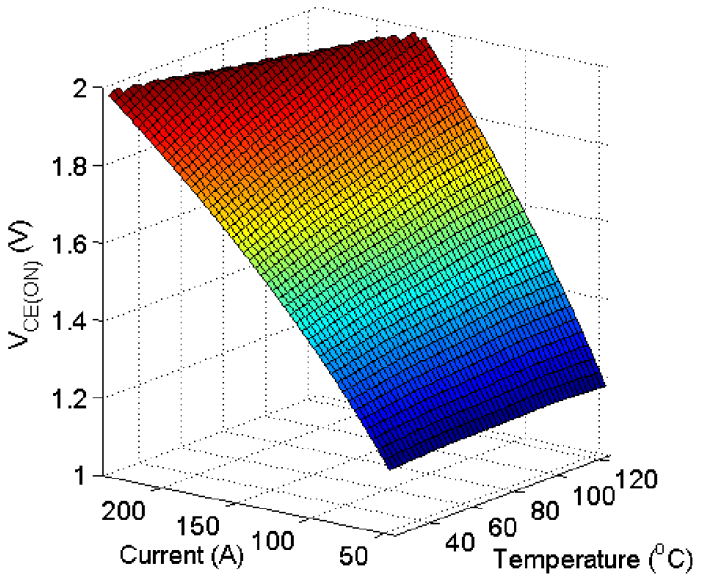


Figure 7.17 Electrical model of the IGBT. $V_{CE(ON)}$ is a function of currrent and temperature

7.2.3.7Diode Electrical Model

In a similar way, the electrical model of the diode is obtained from the experimental measurement of its forward characteristic using a curve tracer at multiple temperatures. A look-up table $V_F=f(I_L,T_{J\_DIODE})$ is generated from experimental data. The output of the electrical model is the forward voltage drop V_F which is used for the diode power loss calculation. The look-up table representing the electrical model of the diode is shown in Figure 7.18.

7.2.4 Modelling TSEP Measurement Noise

In order to simulate the effect of measurement noise on $V_{CE(ON)}$ and V_{th} a white noise model is used. White noise is defined as a random sequence of independent identically distributed random variables [135]. It has a constant and flat power spectral density which indicates that all frequencies receive

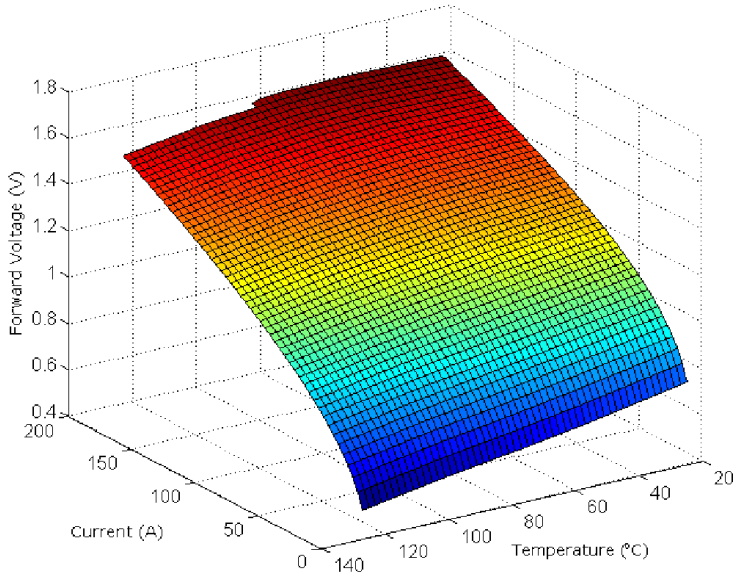


Figure 7.18 Electrical model of the Diode. V_F is a function of currrent and temperature

equal weights. Normally, white noise has a zero mean and a variance σ^2 which can be chosen.

The on-state voltage $V_{CE(ON)}$ is the output of the electrical model of the IGBT. This signal can represent the measurement of this variable in the real application. Therefore, in order to simulate measurement noise, a white noise is superimposed on the $V_{CE(ON)}$ signal to generate the signal V_{CE_mea} which is assumed to be the measurement of $V_{CE(ON)}$. In order to resolve junction temperature information from V_{CE_mea}, a look-up table $T_J=f(V_{CE(ON)}, I_L)$ is used. This look-up table can be generated from the forward characteristic of the IGBT. It receives V_{CE_mea} and current I_L as inputs and gives T_{J_VCE} as output. This is shown in Figure 7.19.

To avoid confusion, it worth distinguishing between the output of the look-up table $T_J=f(V_{CE}, I_L)$ which is T_{J_VCE} which represents the resolved T_J from V_{CE_mea} signal, and the true junction temperature T_J which is the output of the thermal model.

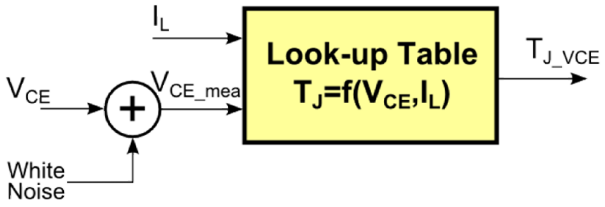


Figure 7.19 White noise is added to $V_{CE(ON)}$ to simulate measurement noise. Measurement signal V_{CE_mea} is used to obtain junction temperature T_{J_VCE} using a look-up table

In the case of V_{th}, the white noise can be added directly to the signal T_J which is the output of the thermal model to create a new signal that represents the resolved T_J from V_{th}. That is because V_{th} is linearly correlated with T_J with a fixed sensitivity (-6mV/^{o}C). The reason for this is made clear earlier in Section 4.5

7.2.5Simulation results

The complete block diagram of the electro-thermal model of the IGBT module is shown in Figure 7.20. The model is implemented in SIMULINK. It receives the loading current signal I_L, switching frequency f_s, and the ambient temperature T_a as inputs. DC link voltage V_{DC} is assumed constant. Model outputs are the IGBT on-state voltage $V_{CE(ON)}$, the diode forward voltage drop V_F, IGBT power loss P_{D_IGBT}, diode power loss P_{D_Diode}, diode junction temperature T_{J_DIODE} and the IGBT junction temperature T_{J_IGBT}.

This model represents the electro-thermal behaviour of a power module regardless of the external circuit topology. It can simulate the electro-thermal behaviour based on the loading current I_L waveform.

To test the model, a sinusoid current input is used to simulate electro-thermal behaviour of the IGBT module in an inverter. A sinusoidal current with amplitude of 150A and frequency 2Hz is applied as an input. The ambient temperature is set fixed to 30^{o}C and the switching frequency is set to 1kHz. Figure 7.21 shows the IGBT and diode voltage forward drops with the corresponding current signal. Figure 7.22 shows IGBT and diode power losses and the corresponding junction temperatures of the IGBT and freewheeling diode. The noise amplitude on the $V_{CE(ON)}$ measurement is set to 10mV. The

simulated measurement signal of $V_{CE(ON)}$ and the resolved T_{J_VCE} is shown in Figure 7.23.

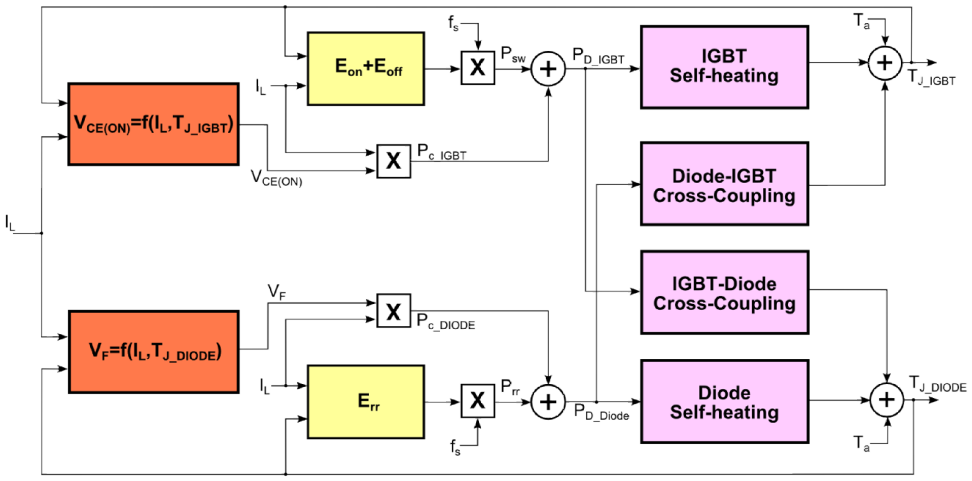


Figure 7.20 A detailed block diagram of the thermo-electrical model of the IGBT module

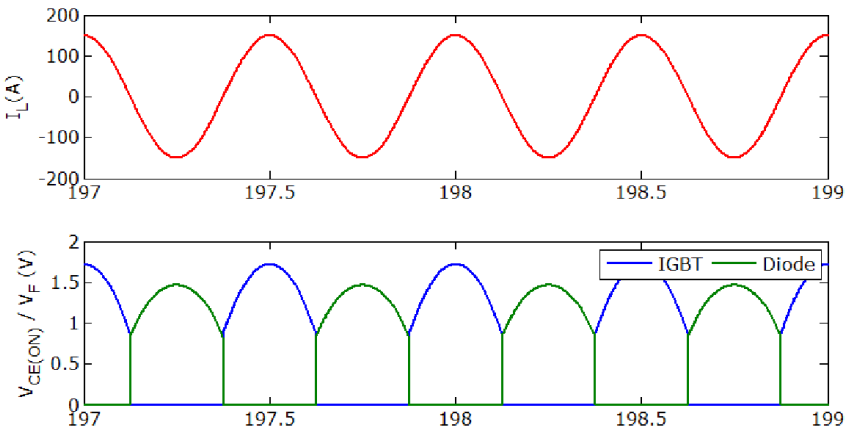


Figure 7.21 Simulated current and forward voltages of the IGBT and the freewheeling diode

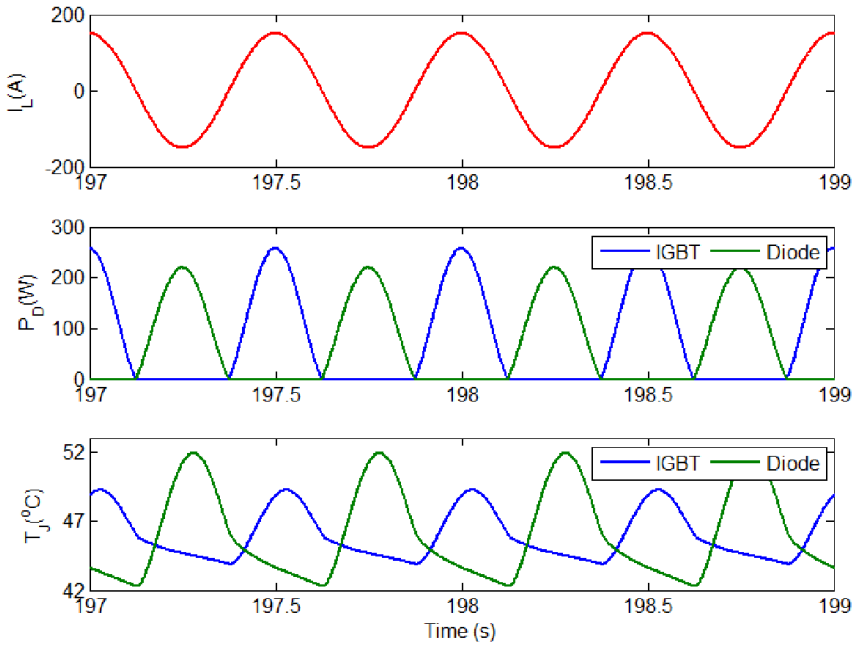


Figure 7.22 Simulated current I_L, IGBT and Diode power dissipation P_D and Junction temperature T_J.

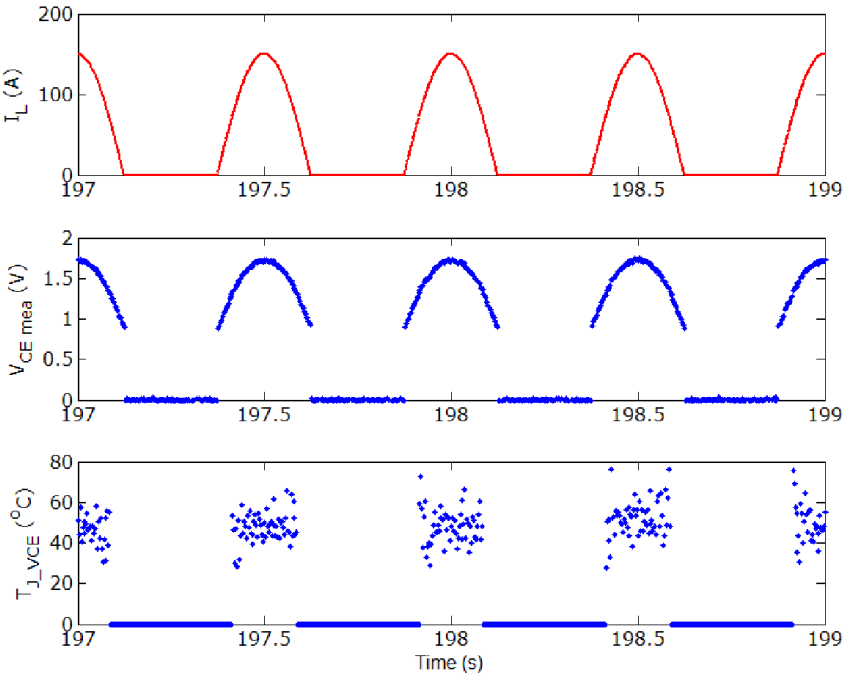


Figure 7.23 Simulated current IL, V_{CE} meaurement V_{CE_mea}, and junction temperature measurement T_{J_VCE}

7.3 Application of Kalman Filter for Junction Temperature Estimation

7.3.1 Developing the State-Space Model of the Thermal Path of the IGBT Module

In order to derive the state space representation required for the implementation of Kalman Filter the model of the thermal path of the IGBT module represented by the Foster equivalent network is employed. This model describes the junction-to-ambient thermal impedance $Z_{\theta ja}(t)$ which is defined as the step response of the thermal path.

The partial fraction expansion form presented earlier in 3.2.4 can be easily transferred into a state-space representation of the parallel form with a diagonal system matrix, where the poles p_i form the elements of the main diagonal while the residues k_i form the elements of the input matrix [136]. The resulting state-space representation for an n element Foster network is:

$$\dot{\mathbf{x}}(t) = \mathbf{A}\mathbf{x}(t) + \mathbf{B}\mathbf{u}(t) \qquad (state\ equation)$$

$$T_J(t) = \mathbf{C}\mathbf{x}(t) + \mathbf{D}\mathbf{u}(t) \qquad (output\ equation)$$

$$\mathbf{A} = \begin{bmatrix} \frac{1}{R_1C_1} & 0 & 0 & \cdots & 0 \\ 0 & \frac{1}{R_2C_2} & 0 & \cdots & 0 \\ 0 & 0 & \frac{1}{R_3C_3} & \cdots & 0 \\ \vdots & \vdots & \vdots & \ddots & \vdots \\ 0 & 0 & 0 & \cdots & \frac{1}{R_nC_n} \end{bmatrix} \quad \mathbf{B} = \begin{bmatrix} \frac{1}{C_1} & 0 \\ \frac{1}{C_2} & 0 \\ \frac{1}{C_3} & 0 \\ \vdots & \vdots \\ \frac{1}{C_n} & 0 \end{bmatrix} \qquad \textbf{(7.12)}$$

$$\mathbf{C} = \begin{bmatrix} 1 & 1 & 1 & \cdots & 1 \end{bmatrix} \quad \mathbf{D} = \begin{bmatrix} 0 & 1 \end{bmatrix}$$

where $\boldsymbol{A_{n\times n}}$ is the system matrix, $\boldsymbol{B_{n\times 2}}$ is the input matrix, $\boldsymbol{C_{1\times n}}$ is the output matrix and $\boldsymbol{D_{1\times 2}}$ is the feed-forward matrix. The state vector $\boldsymbol{x(t)}$ represents the differential temperatures across the RC elements, $\boldsymbol{u(t)=[}P_D(t), T_a\boldsymbol{]}$ is the system input vector, where $P_D(t)$ is the power dissipation and T_a is the ambient temperature. The output equation gives the junction temperature $T_J(t)$ which is the total sum of system states and the constant ambient temperature. According to [94] the ambient temperature can be considered

additive to the output when the variations in the ambient temperature are slow in comparison to the slowest dynamics in the thermal system.

7.3.2 The Addition of the Diode Cross-coupling effect

Since the cross-coupling effect of the diode can be modelled by a Foster network as discussed earlier in Chapter 3, the state-space model in (7.12) is suitable to represent both the self-heating and cross-coupling thermal impedances individually. However, a single model which combines the two effects (self-heating and cross-coupling) is required for the Kalman Filter derivation. Therefore, an extended model that represents both impedances can be constructed by combining a state-space model of order n for the self-heating impedance with a model of order m for the cross-coupling impedance. This results in a model that describes the thermal behavior of the IGBT chips on one substrate tile. A similar modeling procedure can be used to construct a model for the diode chips if required following the same procedure. The complete state-space model description for IGBT junction temperature becomes:

$$\begin{bmatrix} \dot{x}_{s1} \\ \vdots \\ \dot{x}_{sn} \\ \dot{x}_{c1} \\ \vdots \\ \dot{x}_{cm} \end{bmatrix} = \begin{bmatrix} p_{s1} & 0 & 0 & 0 & \cdots & 0 \\ 0 & \ddots & 0 & \vdots & \cdots & 0 \\ \vdots & 0 & p_{sn} & 0 & \vdots & 0 \\ 0 & \vdots & 0 & p_{c1} & 0 & \vdots \\ 0 & \cdots & \vdots & 0 & \ddots & 0 \\ 0 & \cdots & 0 & 0 & \cdots & p_{cm} \end{bmatrix} \begin{bmatrix} x_{s1} \\ \vdots \\ x_{sn} \\ x_{c1} \\ \vdots \\ x_{cm} \end{bmatrix} + \begin{bmatrix} k_{s1} & 0 & 0 \\ \vdots & \vdots & \vdots \\ k_{s1} & 0 & 0 \\ 0 & k_{s1} & 0 \\ \vdots & \vdots & \vdots \\ 0 & k_{s1} & 0 \end{bmatrix} \begin{bmatrix} P_{IGBT} \\ P_{DIODE} \\ T_a \end{bmatrix} \quad \textbf{(7.13)}$$

$$T_J = \begin{bmatrix} 1 & 1 & 1 & \cdots & 1 \end{bmatrix} \begin{bmatrix} x_{s1} \\ \vdots \\ x_{sn} \\ x_{c1} \\ \vdots \\ x_{cm} \end{bmatrix} + \begin{bmatrix} 0 & 0 & 1 \end{bmatrix} \begin{bmatrix} P_{IGBT} \\ P_{DIODE} \\ T_a \end{bmatrix} \quad \textbf{(7.14)}$$

where $x_{s1},\ldots,x_{sn}$ are the states of the self-heating impedance, $p_{s1},\ldots,\ p_{sn}$ and $k_{s1},\ldots,k_{sn}$ are the poles and residues of the self-heating impedance respectively. Similarly, $x_{c1},\ldots,x_{cm}$ are the states of the cross-coupling impedance whereas $p_{c1},\ldots,p_{cm}$ and $k_{c1},\ldots\ ,k_{cm}$ are the poles and residues of the self-heating impedance respectively. T_J is the IGBT junction temperature. T_a is the ambient temperature, P_{IGBT} and P_{Diode} are the power dissipation of the IGBT and diode respectively.

7.3.3 Identification of Kalman Filter Matrices

Derivation of the Kalman Filter was presented in Chapter 3 where the steps of the algorithm implementation were described. Here, the values of the matrices required for the implementation are determined. Since the Kalman filter is implemented on a digital computer, the discrete version of the Kalman filter should be used. Therefore, the state-space model in (7.13) should be transformed into a discrete state-space model of the form:

$$\mathbf{x}_k = \mathbf{F}\mathbf{x}_{k-1} + \mathbf{L}\mathbf{u}_k + \mathbf{G}w_k \tag{7.15}$$

$$T_{Jk} = \mathbf{H}\mathbf{x}_k + \mathbf{J}\mathbf{u}_k + v_k \tag{7.16}$$

The components of matrices ***F*** and ***L*** of the discretized model in (7.15) can be obtained from the continuous time values of ***R***s and ***C***s of the Foster network in (7.13) that were identified in Section 7.2.1. The model that was identified is of 5th order for the self-heating model and a 4rd order for the cross-coupling model. Therefore, the model in (7.13) has a total of 9 states. Consequently, the dimensions of matrix ***F*** are 9x9, matrix ***L*** is 9x3, matrix ***G*** is 9x1, matrix ***H*** is 1x9 and ***J*** is 1x3. The discretization step is performed using a zero-order hold on the inputs and a sample time t_s=1kHz. The command "*c2d*" in MATLAB is used to obtain the discretized state-space model. The resulting parameters are listed in Table 7.3.

Table 7.3 Parameters of the Discrete State-Space Thermal Model

Term Num.	p	k
s1	0.880542792586113	0.001971043922329
s2	0.995758053888483	1.141083503998116e-04
s3	0.999256854971480	1.731527916451451e-05
s4	0.999256854971480	4.01414565837939e-06
s5	0.999983563233294	1.11770013601867e-07
c1	0.996941327834298	-1.04606588067007e-05
c2	0.998919037322463	1.35444623495441e-05
c3	0.999857847022312	3.19844199797550e-06
c4	0.999974771182193	1.08483916572435e-07

where the terms s1 to s5 represent the parameters of the self-heating whereas terms c1 to c4 represent the parameters of the cross-coupling. Matrices $\boldsymbol{H}$ and $\boldsymbol{J}$ do not change and they remain as shown in (7.14). The values of the covariance matrices $\boldsymbol{Q}$ and $\boldsymbol{R}$ were determined by tuning : $\boldsymbol{R}$=0.1 and $\boldsymbol{Q}$=0.0001*$\boldsymbol{I}$ where $\boldsymbol{I}$ is 9x9 identity matrix.

7.3.4 Simulation Results

The algorithm of the Kalman Filter is coded in the C programming language. The code for the Kalman filter algorithm can be found in Appendix C. As can be seen in Figure 7.24, the electro-thermal model of the IGBT module provides the signals required for the Kalman filter. The inputs to the Kalman Filter are the power dissipation $\boldsymbol{P_D}$ of the IGBT and the diode in addition to the ambient temperature T_a which forms the input vector $\boldsymbol{u(t)=[P_D(t),\ T_a]}$. The noisy T_J measurement signal is represented by the signal T_{J_VCE} which is obtained from $V_{CE(ON)}$ signal as described earlier.

The on-state voltage $V_{CE(ON)}$ is chosen to be the TSEP in the simulation as it is a worse example of a TSEP than the threshold voltage V_{th} (nonlinearity and low sensitivity properties as compared to V_{th}). This was described in Chapter 4.

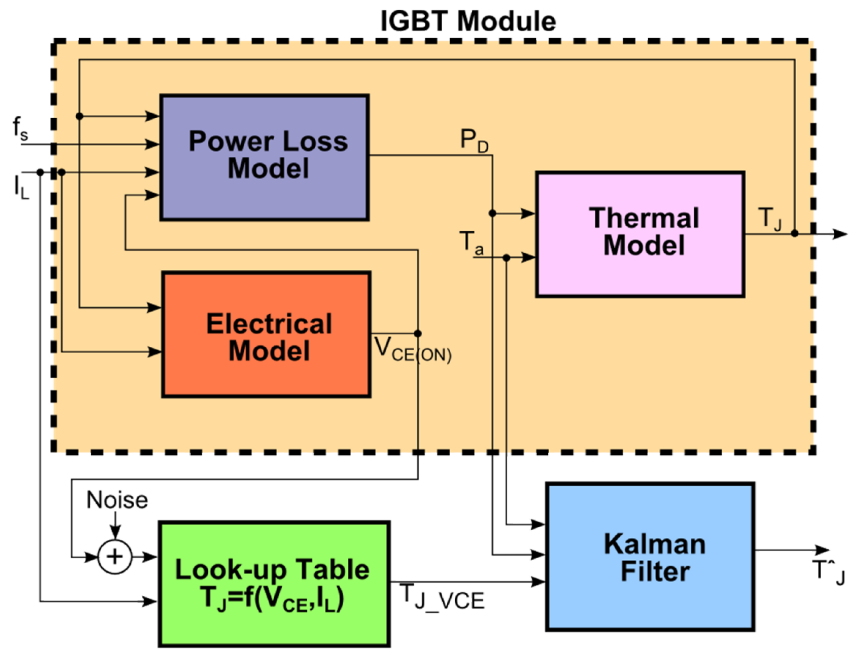


Figure 7.24 The electro-thermal model of the IGBT module with the look-up table for the TSEP and Kalman Filter

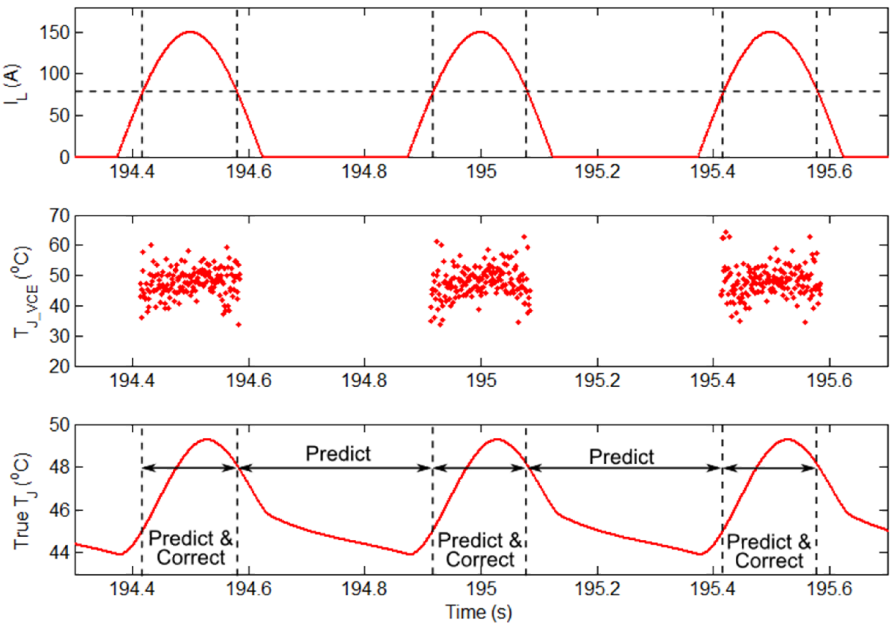


Figure 7.25 Availability of the Resolved T_{J_VCE} and the Corresponeding Steps of Kalman Filter

The availability of the estimate T_{J_VCE} is limited to when I_L>80A during half of the inverter modulation period. This threshold should be higher than the inflection point which happens at I_L=40A. It can be determined by examining noise level in the signal T_{J_VCE}. That limits the implementation of the correction step, which uses the T_{J_VCE} estimate, to the period when I_L>80A. This is shown in Figure 7.25. The filter estimates junction temperature T_J relying on the model in the prediction step for the rest of the modulation period.

Similarly, the T_J resolved from the threshold voltage V_{th} is intermittent. However, that intermittency is related only to the switching of the IGBT. As long as the IGBT is switching, a resolved T_J can be obtained from V_{th} regardless of the current value. Intermittency still applies when current is commutated away from the IGBT dies.

A sinusoidal input current of amplitude 150A and frequency 2Hz is used in this simulation. Figure 7.26 shows the true T_J which is the thermal model output, the T_{J_VCE} resolved from $V_{CE(ON)}$ noisy measurement and the estimated junction temperature T_{J_est} produced by Kalman filter. Figure 7.27 shows a magnified overlay of the three signals together. It can be seen that the estimated junction temperature T_{J_est} given by Kalman Filter is in good agreement with the true T_J. Compared to T_{J_VCE} resolved directly from $V_{CE(ON)}$, a large improvement is achieved by using the Kalman Filter on the resolved T_{J_VCE} produced by the thermos-sensitive parameter $V_{CE(ON)}$. It is clear in Figure 7.27 that the noise and the intermittency are eliminated in the estimate of T_J.

Similar results can be obtained when the threshold voltage V_{th} is used as a TSEP to give a resolved T_J instead of $V_{CE(ON)}$. However, as explained earlier $V_{CE(ON)}$ is chosen due to its nonlinear characteristic which makes it less well suited to resolve T_J. As a conclusion, regardless of the TSEP used to resolve T_J, Kalman filter provides an accurate estimate of the true T_J of an IGBT module. The same applies for the junction temperature of the freewheeling diode, where the forward voltage can be used to resolve its junction temperature and the Kalman filter can again be applied.

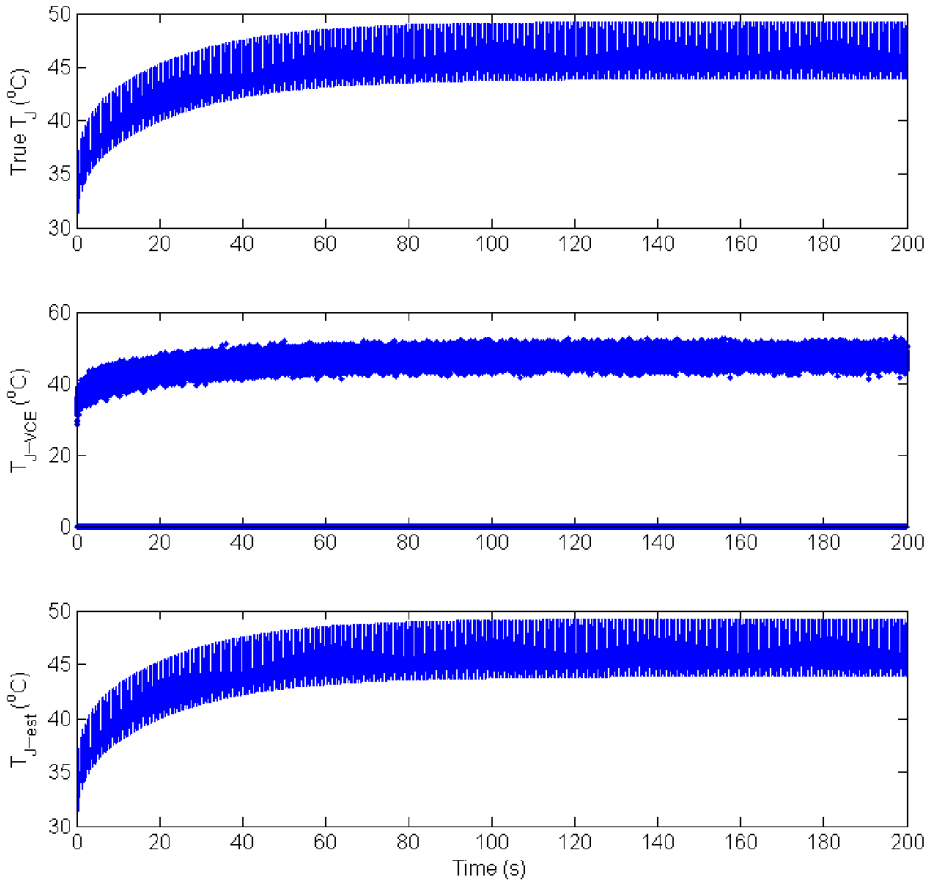


Figure 7.26 Kalman Estimate of T_J compared to True T_J and $V_{CE(ON)}$ estimate T_{J_VCE}

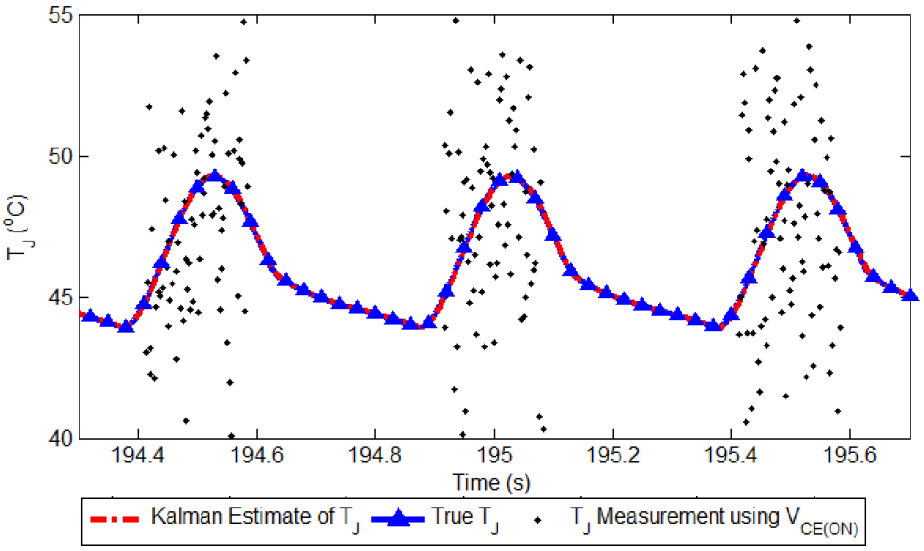


Figure 7.27 Kalman Estimate of T_J compared to True T_J and $V_{CE(ON)}$ estimate T_{J_VCE}

7.4 Experimental Verification of Kalman Filter for Real-time Estimate of Junction Temperature

For the experimental verification of the Kalman Filter algorithm, a full-bridge inverter is used. The top IGBT of one half-bridge module is monitored using the IR camera where the maximum temperature in the module is chosen for comparison as explained earlier in Section 1.1.1.1A.3. The Kalman filter algorithm is implemented on the dSPACE system and a block diagram for the practical implementation is illustrated in Figure 7.28. The loading current I_L and the on-state voltage $V_{CE(ON)}$ are measured on the inverter by the dSPACE system. A look-up table is used to resolve T_J information from the measured $V_{CE(ON)}$. This resolved T_J is fed into Kalman Filter along with the power dissipation of the IGBT P_{IGBT} and the diode P_{DIODE}. The estimated junction temperature $\hat{T}_J$ is fed-back to the power loss model. The construction of this model was explained in Chapter 5.

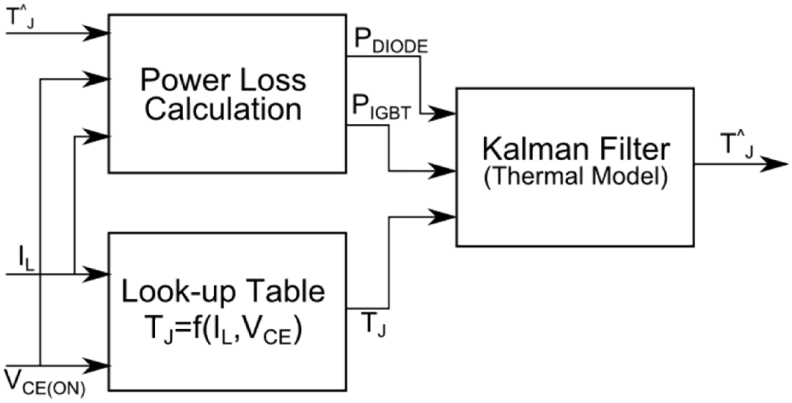


Figure 7.28 A Block Diagram of the Practical Implementation of Kalman Filter

The TSEP used for verification is the on-state voltage $V_{CE(ON)}$. That is because it has temperature correlation properties which are worse than those for threshold voltage V_{th} and it therefore serves as a more demanding test case for validation. In addition, the current dependent noise behaviour of the resolved T_J can make it more difficult to achieve good performance by using the Kalman filter since the algorithm assumes known noise characteristics (white Gaussian zero-mean with known variance σ^2). Therefore, the variable noise characteristic of the resolved T_J can be a difficulty to achieve a good performance by the algorithm.

It is true that the noise in T_J resolved from V_{th} is higher than that resolved from $V_{CE(ON)}$, but for the Kalman Filter this is not an issue as long as the filter can be tuned to compensate for the higher noise levels. Moreover, the availability of $V_{CE(ON)}$ measurement is limited to I_L>80A for reasons explained earlier. Therefore, $V_{CE(ON)}$ provides less data compared to V_{th}.

For these reasons, $V_{CE(ON)}$ is a more challenging TSEP than V_{th} and therefore it is chosen to validate the algorithm. However, threshold voltage V_{th} can also be used to provide the information of T_J instead of $V_{CE(ON)}$ by replacing the look-up table $T_J=f(V_{CE(ON)},I_L)$ with the appropriate calibration relationship $T_J=f(V_{th})$. No modification of the Kalman filter or the power loss model is required.

7.4.1 Verification of the Real-time Estimate of Junction Temperature

Figure 7.29a shows the experimental measurement of loading current, T_J estimate given by the Kalman filter, IR camera measurement and T_J resolved from $V_{CE(ON)}$ along with the error, which is represented by the difference between the Kalman filter estimate and the IR camera measurement. It is evident that the estimate of T_J given by the Kalman filter tracks the IR camera measurement accurately during both heating and cooling regimes with a maximum error of 5.3%.

The difference between the IR camera measurement and the Kalman filter estimate of T_J can be attributed to many factors. First, the IR camera measures the temperature at the top surface of the IGBT whereas $V_{CE(ON)}$ indicates the temperature at the intrinsic body region buried inside the IGBT. Second, the presence of the wire-bonds on the top of the chip prevents the IR camera from obtaining the maximum temperature due to the shading effect and the measured temperature could therefore be lower than reality [137]. In addition, calibration of the look-up table is done under isothermal conditions while in practice there are temperature gradients across the module. Since $V_{CE(ON)}$ is measured across the power terminals, the measurement includes the voltage drop across the packaging resistance which is affected by temperature gradients. This results in a mismatch with the calibration. On the other hand, the difference between the IR camera and T_J estimate in the cooling regime,

which shows a maximum of 1.5 ºC, is justified by the fact that no $V_{CE(ON)}$ data is available for T_J measurement and the correction step of the Kalman filter is not carried out. As a result, the estimate in this regime is fully dependent on the thermal model. The difference is then linked to errors inherited from the modelling process.

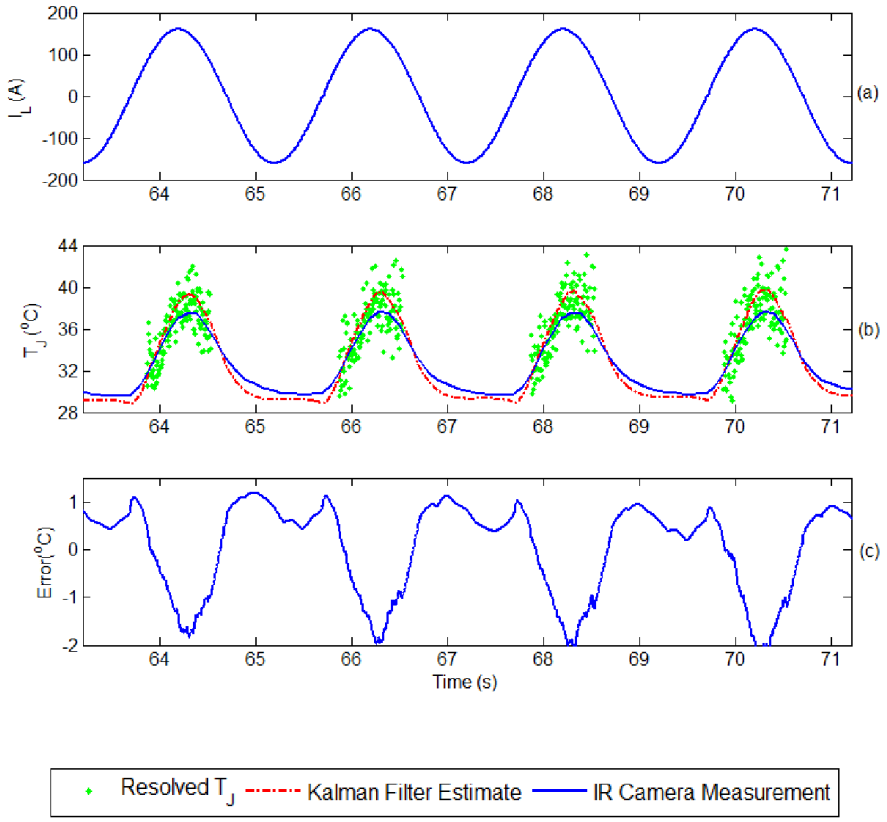


Figure 7.29 (a) Sinusoid Loading Current 150A/0.5Hz (b) Kalman estimate of junction temperate compared to IR camera measurement and T_J resolved from $V_{CE(ON)}$. (c) The difference between IR camera measurement and T_J estimate

Compared to the T_J measurement, the estimate is noise free and continuity of the signal is preserved. To evaluate the improvement in the T_J estimate over the T_J measurement, the Mean Absolute Error (MAE) and Standard deviation (σ) of the error is examined. Those statistics are calculated as follows:

$$MEA = \frac{1}{n}\sum_{i=1}^{n}|e_i|, \qquad \sigma = \sqrt{\frac{1}{n}\sum_{i=1}^{n}(e_i - \bar{e})^2} \qquad \textbf{(7.17)}$$

where n is the number of data points and $\bar{e}$ is the error mean. The errors e of the T_J estimate and the resolved T_J are acquired by subtracting the T_J estimate and the T_J measurement from the IR camera measurement. Table 7.4 shows the statistics of the two error signals. It is evident that the accuracy of T_J estimate has improved compared to T_J measurement obtained by $V_{CE(ON)}$ with 53% less mean absolute error and 30% less spread.

Table 7.4

error statistics of T_J measurement and T_J estimate

	Mean Absolute Error (^oC)	Standard Deviation(^oC)
T_J resolved by $V_{CE(ON)}$	1.40	2.06
T_J estimate	0.74	0.62

7.4.2Variable Operating Conditions

In many applications, the modulation frequency can change for example in with wind turbines and motor speed controllers. The modulation frequency and amplitude both affect the junction temperature profile. To demonstrate the consistency of the T_J estimate under variable operating conditions, the load current is varied in the inverter. Figure 7.30 shows the T_J estimate response at the instant when the modulation frequency changes from 0.5 Hz to 1 Hz with constant amplitude 150 A. The agreement of the T_J estimate with the IR camera measurements is maintained. It is seen that the ripple ΔT in T_J is reduced when the frequency is increased whereas the mean temperature T_m is nearly constant in agreement with the IR camera measurement as can be seen in Table 7.5. This is to be expected since the frequency response of the thermal system replicates a low-pass filter.

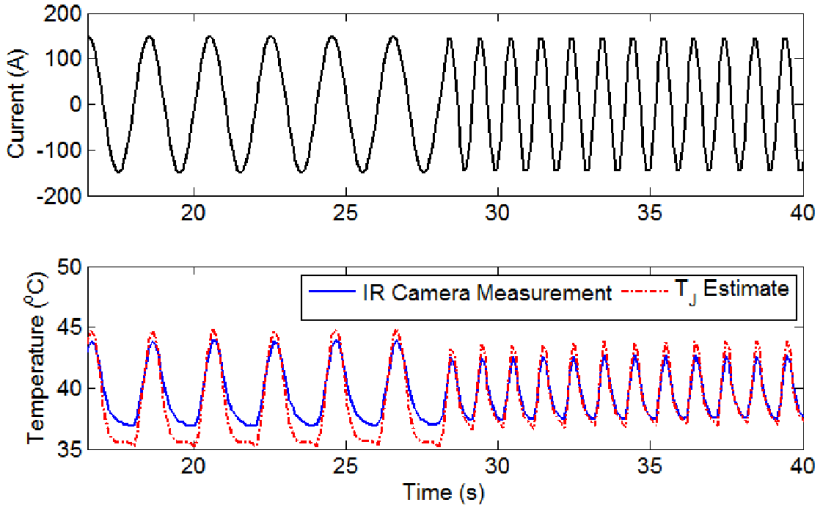


Figure 7.30 IR camera measurement and T_J Estimate when modulation frequency is changed from 0.5Hz to 1Hz as can be seen in the load current.

Table 7.5

T_J profile parameters for IR camera and T_J estimate under a change in modulation frequency

	0.5Hz		1Hz	
	IR Camera	T_J Estimate	IR Camera	T_J Estimate
Tm	40.43	40.13	40.1	40.47
ΔT	6.9	9.2	4.96	6.79

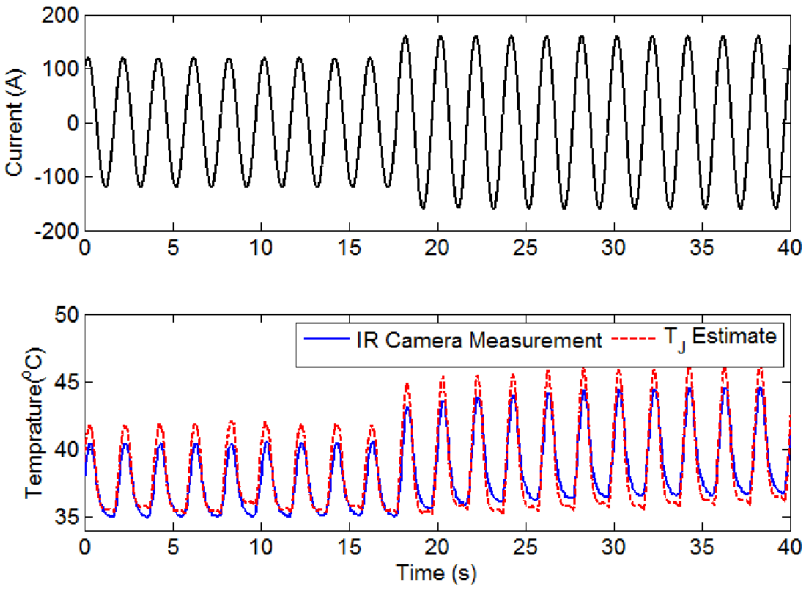


Figure 7.31 IR camera measurement and T_J Estimate when current amplitude is changed from 120A to 160A as can be seen in the load current.

Table 7.6

T_J profile parameters for IR camera and T_J estimate under a change in current amplitude

	120A		160A	
	IR Camera	T_J Estimate	IR Camera	T_J Estimate
Tm	37.68	38.55	40.51	41.01
ΔT	5.49	6.65	7.89	10.29

Figure 7.31 shows T_J estimate when current amplitude is increased from 120A to 160A with a modulation frequency of 0.5Hz. An increase in the mean temperature and the ripple is evident in Table 7.6 for both IR measurement and T_J estimate.

7.4.3Unstable Boundary Conditions

Variations in the heat transfer coefficient at the thermal boundary conditions can result from deviations of coolant flow rate. This changes the thermal resistance of the thermal path and affects junction temperature. For the examination of this effect on the T_J estimate, the water flow in the heat sink is

changed during inverter operation. The water flow is reduced which increases the thermal resistance of the heat sink [96]. Figure 7.32(a) shows the T_J estimate compared to the IR camera measurement. Figure 7.32(b) shows T_J resolved from $V_{CE(ON)}$ compared to the IR camera measurement and Figure 7.32(c) shows the baseplate temperature T_C when the water flow is changed after reaching thermal equilibrium. The baseplate temperature T_C is measured with a thermocouple fixed to the back side of the baseplate facing the coolant. The water pump is stopped for 84s where upon the peak junction temperature increases from 42°C to 58°C and the baseplate temperature increases from 32°C to 43°C. After 84s, the water flow is returned back to its original level and T_J goes down back to 43°C after 52s in good agreement with IR camera measurement whereas T_C falls back to 32°C .

The difference between the IR camera measurements and the T_J estimate is shown in Figure 7.32(d). During the transient state a gradual increase in error margins and slight shift in the mean value can clearly be seen. However, regardless of the growing error, which remains within 3.6% in this case, the adaptive property of Kalman filter preserves estimate consistency and robustness by the predict-correct mechanism. The T_J measurement derived from $V_{CE(ON)}$ is utilized to update the T_J estimate and keep it in track with the true value obtained from the IR camera.

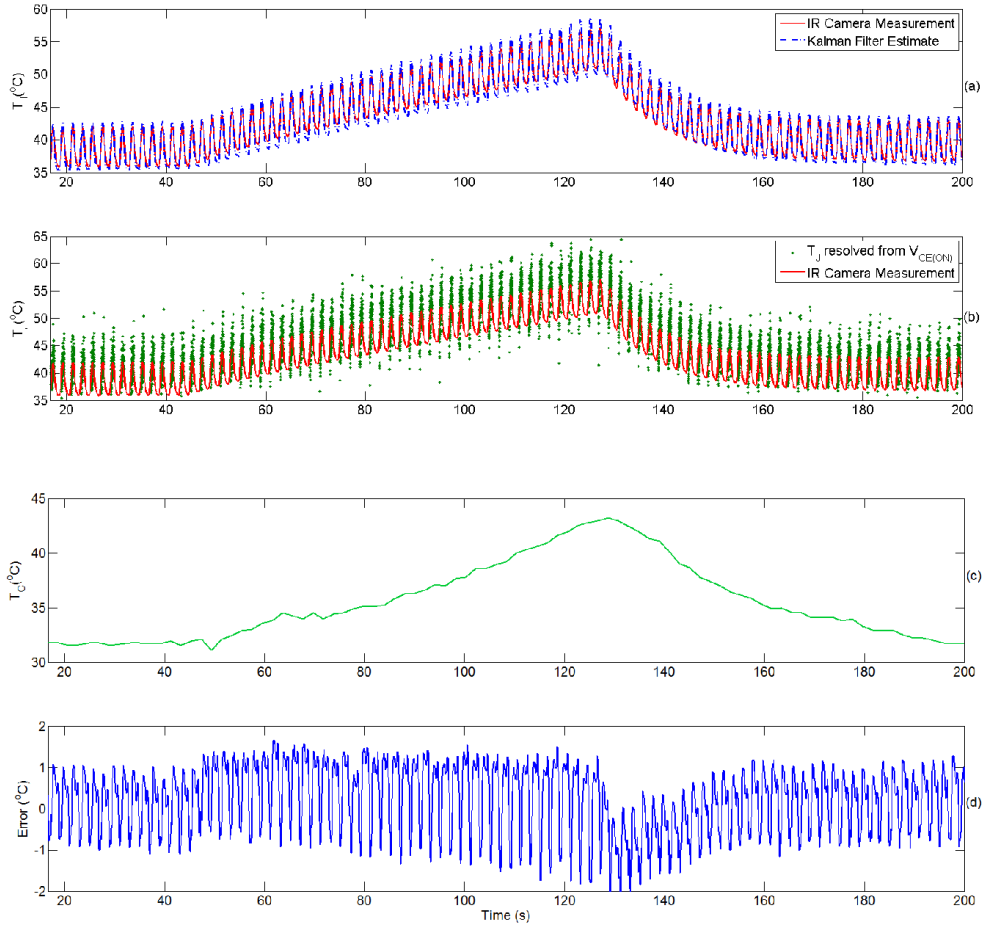


Figure 7.32 (a) IR camera measurement compared to T_J estimate over the duration of water flow change (b) IR camera measurement compared to T_J resolved from $V_{CE(ON)}$ (c) the corresponding baseplate temperature T_C (d) the difference between IR camera measurement and T_J estimate.

7.5 Discussion

An accurate estimate of junction temperature T_J is obtained from an online measurement of the on-state voltage $V_{CE(ON)}$, measured at high current during normal operation of power converter. $V_{CE(ON)}$ is used as a thermo-sensitive electrical parameter (TSEP) to get a measurement of T_J. A Kalman filter is then applied to the resulting T_J measurement to reduce noise and eliminate the effects of intermittency of the $V_{CE(ON)}$ measurement by constraining the measurement signal to a thermal model in a predict-correct manner. The mechanism of Bayesian updating of *a priori* knowledge from a thermal model by *a posteriori* knowledge given by a measurement allows the accuracy of the T_J information to be improved.

Excellent matching is achieved between the T_J estimate and the IR camera measurement under different loading and cooling conditions, demonstrating the ability of the method to adapt to variations in the operating conditions of the power converter. An improved accuracy is obtained by using the Kalman filter compared to T_J measurement resolved from $V_{CE(ON)}$ alone. The method presented is suitable for real-time estimation of T_J with no modification of the control strategy of the power converter. This method can be easily implemented on a gate drive if the appropriate measurement circuit of the TSEP is integrated within it. Therefore, T_J information can be used to inform the control system and the health management of the power converter allowing more effective usage of the power modules from both electrical and reliability perspectives.

7.6 Summary

This chapter detailed the development of the electro-thermal model of a power module in the MATLAB/SIMULINK environment. This model is used to investigate the applicability of the Kalman Filter algorithm to estimate the junction temperature of the IGBT. Simulation results showed that an improved accuracy can be achieved by Kalman Filter to estimate junction temperature T_J compared to the measurement of T_J resolved from a noisy measurement of a TSEP such as $V_{CE(ON)}$ or V_{th}.

Those results are confirmed by experimental results by implementing the Kalman Filter algorithm on a full-bridge inverter test setup. The algorithm is vaildated for variable operating conditions and variable cooling conditions. Experimental results show an improved accuracy is achieved by using the proposed algorithm under all conditions.

The next chapter continues the development of Kalman filter algorithm to explain the use of the residual produced by the Kalman filter as a means to monitor the thermal degradation of the power module. It is demonstrated that the online measurements of the $V_{CE(ON)}$ and V_{th} along with the estimate of T_J can be combined in a residual based health monitoring to detect and estimate packaging degradation (wire-bond and solder fatigue) of the power module in real-time.

Chapter 8 Experimental Validation of Analytical Redundancy for IGBT Health Assessment

8.1 Introduction

In this chapter, the health assessment of IGBT power modules using the principle of analytical redundancy is validated. The background to this method was presented in Chapter 4. In order to validate this method, a power cycling test is carried out to activate the two dominant failure mechanisms of wire-bond lift-offs and solder fatigue. At prescribed intervals during the power cycling test, an inverter is installed to allow evaluation of the cycled module under normal operating conditions and collect the online measurements. The residuals are analysed to reveal changes in their statistical behaviour which is indicative of module degradation.

8.2 Experimental Procedure

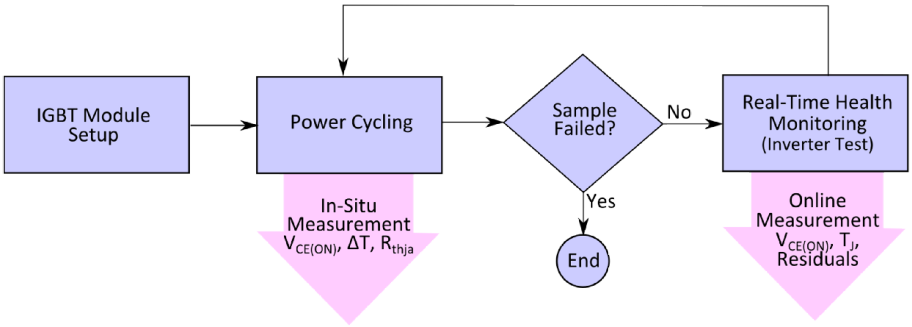


Figure 8.1 The experimental procedure for validating analytical redundancy.

Figure 8.1 explains the experimental procedure of validating the proposed health monitoring of power modules using analytical redundancy. The IGBT module sample is setup on the test equipment and the power cycling test is started. The power cycling test is interrupted from time to time to connect the inverter test rig in order to allow the collection of online measurements from the cycled module under normal operating conditions. In the inverter test rig, the residuals are generated from the online measurements using the health monitoring framework described earlier. Then, the power

cycling test is continued and the procedure is repeated until the IGBT module is deemed to have reached end of life.

The measurements of on-state voltage $V_{CE(ON)}$, temperature swing ΔT_J, and junction-to-ambient thermal resistance R_{thja} are made by the power cycling equipment during the power cycling test. Similarly, the measurement of $V_{CE(ON)}$,V_{th} and current I_L are made on the inverter test rig in addition to the estimate of T_J obtained using the real-time health monitoring framework. This allows the indications given by the proposed health monitoring of a degraded IGBT module during normal operation to be compared with the indications given by the power cycling test with controlled, pre-determined and known conditions.

8.2.1 Power Cycling Test

The power cycling test was performed using a "MentorGraphics" Power Tester 1500A [138] as shown in Figure 8.2. The IGBT module subjected to cycling is an off-the-shelf half bridge 1.2kV/200A shown in Figure 8.3. The module was mounted on a cold plate with a 25µm thick Kapton film used as an interfacing material between the cold plate and the baseplate. The purpose of the Kapton film was to increase the case-to-ambient thermal resistance in order to achieve a temperature swing at the substrate-case interface and so accelerate the degradation of the substrate mount-down solder layer compared to other failure mechanisms.

The module was set up for power cycling in the configuration shown in Figure 8.4. The tested module contains 4 IGBT devices. Each side (High and Low) has 2 IGBTs connected in parallel. The low side IGBTs were biased with a gate-emitter voltage V_{GE}=15V such that the cycling current I_C as well as the measurement current I_M were shared between the two IGBTs in parallel. The connection of the module on the power cycling equipment is shown in Figure 8.5. The collector-emitter voltage V_{CE} is a global measurement across the two parallel IGBTs and therefore, it represents an "average" measurement of the two IGBTs. The gate and emitter terminals of the high side of the module are shorted together during the cycling such that no current flows through them.

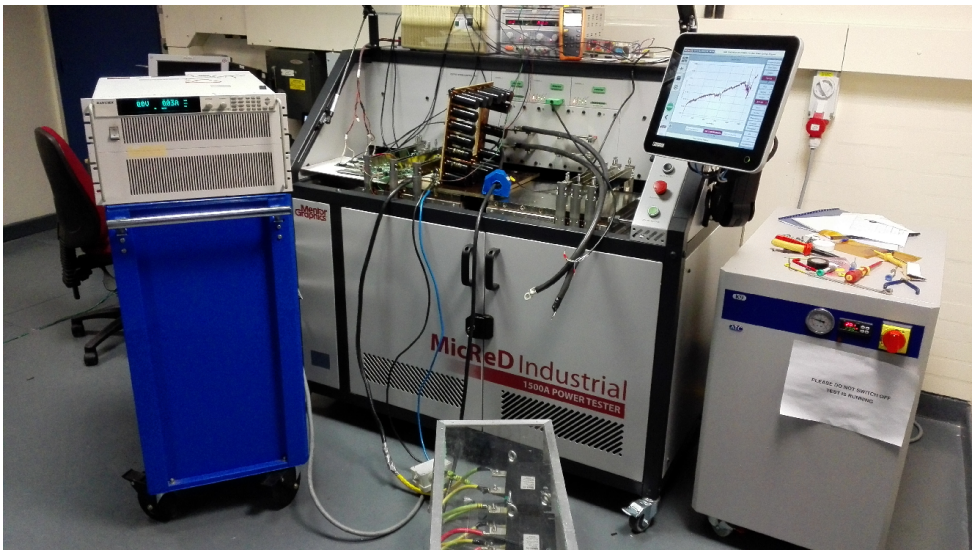


Figure 8.2 Mentor Graphics Power Tester 1500A used for Power Cycling Test with the inverter setup installed

Figure 8.3 An off-the-shelf 1.2kV/200A IGBT power module used for power cycling and validation of analytical redundancy.

The module junction temperature T_J was estimated using the collector-emitter voltage drop V_{CE} as a thermo-sensitive electrical parameter. A calibration curve $T_J=f(V_{CE})$ at a constant measurement current of I_M=200mA was used to calculate junction temperature T_J. Since the V_{CE} value is a global measurement across the low side, the junction temperature T_J is a global temperature which is a representative temperature of the two IGBTs rather than

an estimate of the actual temperature of any individual IGBT. An actual measurement of the temperature at the substrate was obtained via a thermocouple fixed to the substrate.

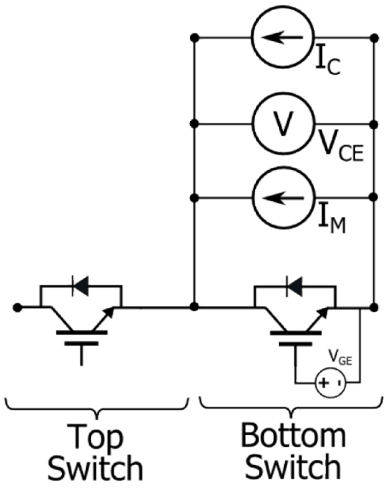


Figure 8.4 The low side is biased with a Voltage $V_{GE.}$ Cycling Current I_C and Measurement Current I_M pass through the low side and V_{CE} measurement is made across the low side.

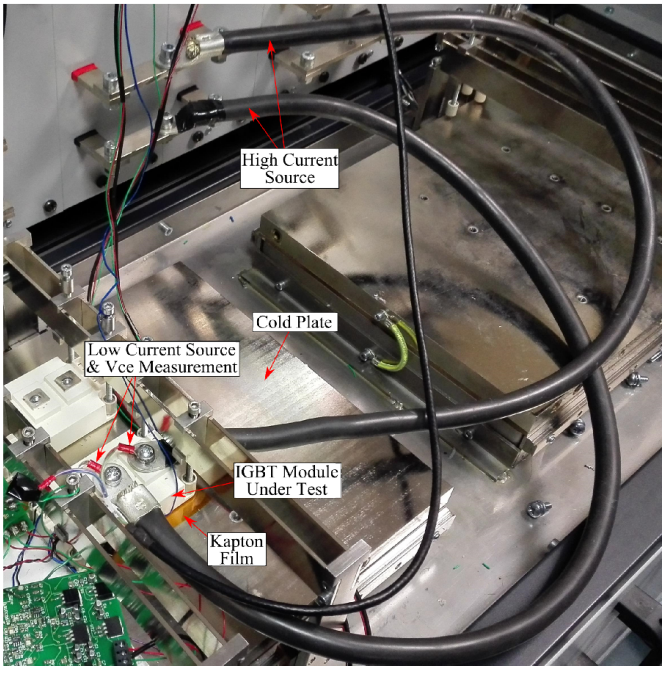


Figure 8.5 Connection of High and Low Current sources of the power cycling equipment

The cycling current I_C is fixed at 170A which gives a temperature swing at the junction ΔT_J=120 K with T_{Jmax}=140°C and T_{Jmin}=20°C as estimated from V_{CE}. The water temperature was maintained at 20°C. The

heating time and cooling time were fixed at 65s and 70s respectively. This achieved a ΔT of about 70K at the substrate with T_{max}=90°C and T_{min}=20°C. The test started with an initial power dissipation P_D=344W.

Transient thermal impedance measurements were made at a fixed interval of 1000 cycles during the cycling. This measurement was made with the module in situ without disturbing the physical mounting of the module. A heating current of 150A was used for the thermal transient measurement which produced a power dissipation step of 360W. The junction temperature T_J was calculated using the common method $T_J=f(V_{CE})$ where V_{CE} at low current is used as thermo-sensitive parameter.

8.2.2Inverter Test Setup

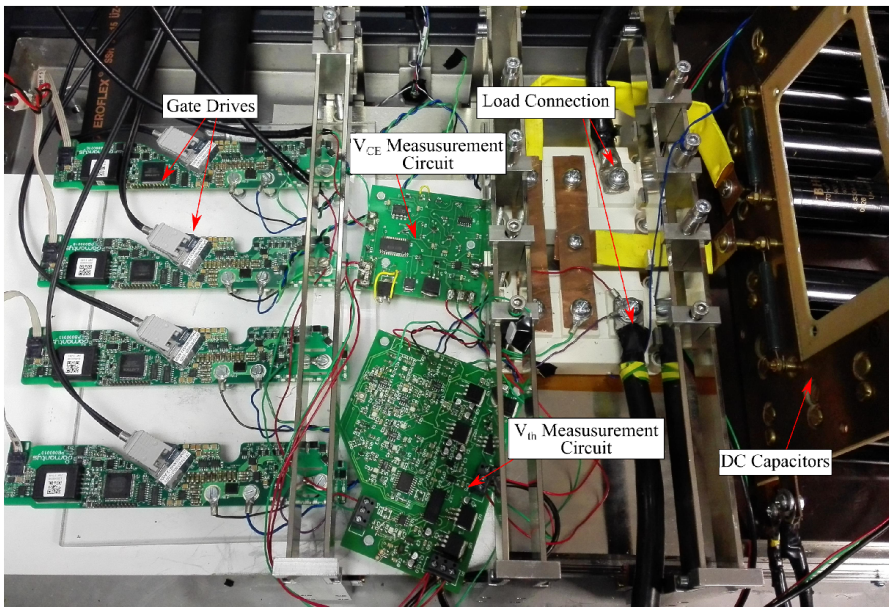


Figure 8.6 Inverter setup on the power cycling equipment

For the testing of the proposed health monitoring framework, an inverter is installed on the same power cycling equipment, as shown in Figure 8.6. The inverter can easily be connected and disconnected such that power cycling test can be carried out without dismounting the tested module from the power cycling equipment. This is important since dismounting the module can alter the junction-to-ambient thermal path and consequently the junction-to-ambient thermal impedance. This will invalidate the calibrated thermal model and hide any changes in thermal resistance that might result

from solder fatigue. In this way, the consistency of the thermal path from the chip to the ambient is ensured.

This inverter setup is the same setup used to validate the junction temperature estimation method explained earlier. More details of the inverter are provided in Appendix A.

8.3 Results

8.3.1 Power Cycling Test Results

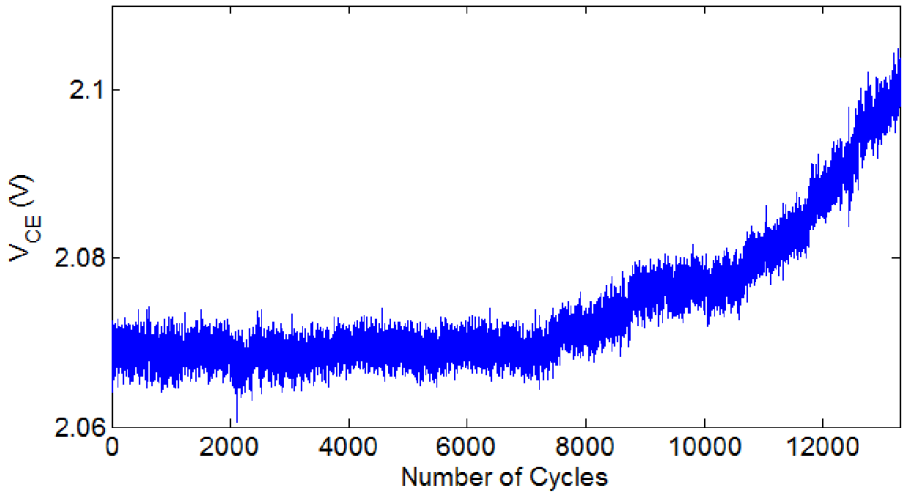


Figure 8.7 On-state voltage $V_{CE(ON)}$ of the IGBT measured by the power cycling equipment.

The power cycling test was terminated after 13350 cycles by which time the total junction-to-ambient thermal resistance R_{thja} had increased by 15% from its original value. Figure 8.7 shows the collector-emitter voltage V_{CE} measured during the power cycling test. This measurement is obtained at a constant current value of 170A which was used for power cycling. A gradual increase in V_{CE} can be observed after 7,000 cycles but note the absence of the step-changes that are typically associated with wire bond lift. This increment is therefore associated with the increment in the junction temperature T_J and no wire-bond lift-offs are observed.

Figure 8.8 (a) shows the junction temperature swing ΔT_J measured by the power cycling equipment. It can be seen that ΔT_J starts at 125°C and increases slightly from the beginning of the test until about 7,000 cycles where

it starts to increase more rapidly up to 145°C by the end of the test. This observed increment agrees with the change in junction-to-ambient thermal resistance R_{thja}, which is measured every 1000 cycles up to 9100 cycles and every 500 cycles afterwards as shown in Figure 8.8 (b). the cooling water temperature is controlled to remain constant at 20°C over the duration of the test.

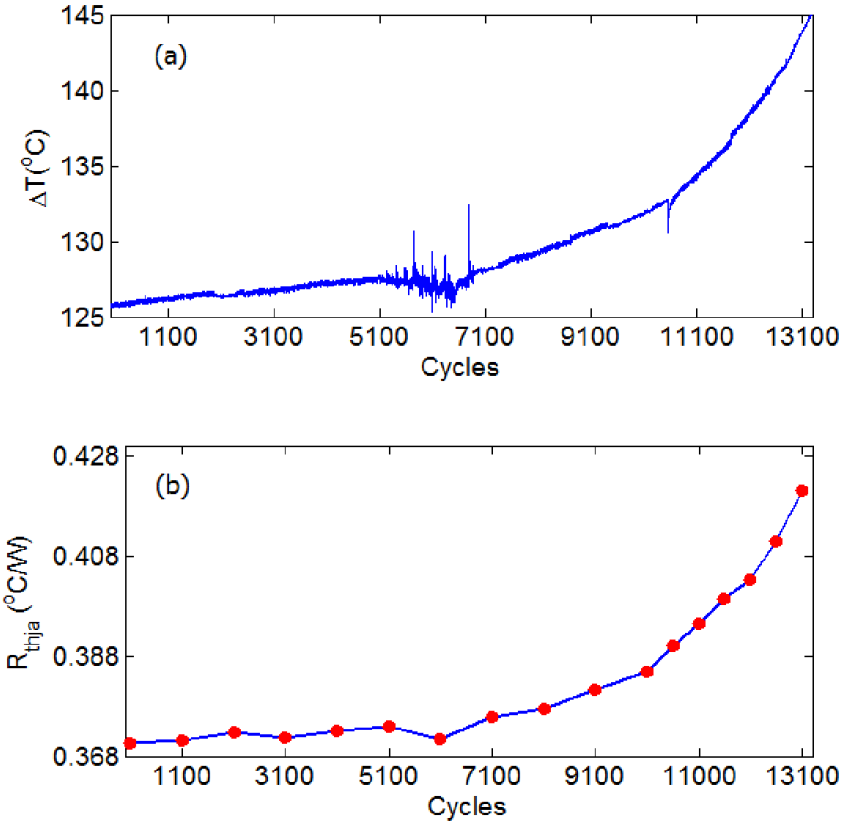


Figure 8.8 (a) Temperature Swing and (b) Junction-to-ambient Thermal Resistance R_{thja} during the power cycling test measured by power cycling equipment.

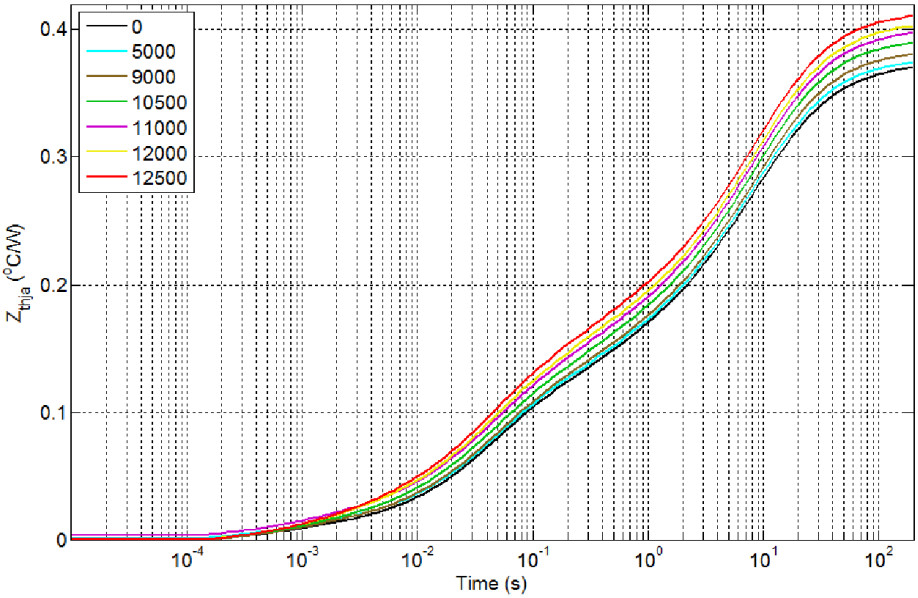


Figure 8.9 The thermal transient measurement at different cycles as measured during the power cycling test.

The transient thermal impedance is shown in Figure 8.9. It can be seen that Z_{thja} increases as the number of cycles progresses. This increment is related to the degradation in the thermal path as a result of solder fatigue. In order confirm that, Scanning Acoustic Microscopy is performed on the cycled module after the power cycling test is terminated.

8.3.2Scanning Acoustic Microscopy

Scanning Acoustic Microscopy (SAM) characterization was carried out using PVA TePla AM300. Scanning acoustic microscopy is a non-destructive technique to image the internal features of a specimen and can detect delamination and voids of sub-micron thickness. C-mode scanning (interface scan) was conducted with a 35MHz transducer to provide planar view on several focused depths corresponding to specific internal layers. This creates 2D greyscale images from the reflected ultrasonic echoes, in which discontinuities show different brightness from the intact area.

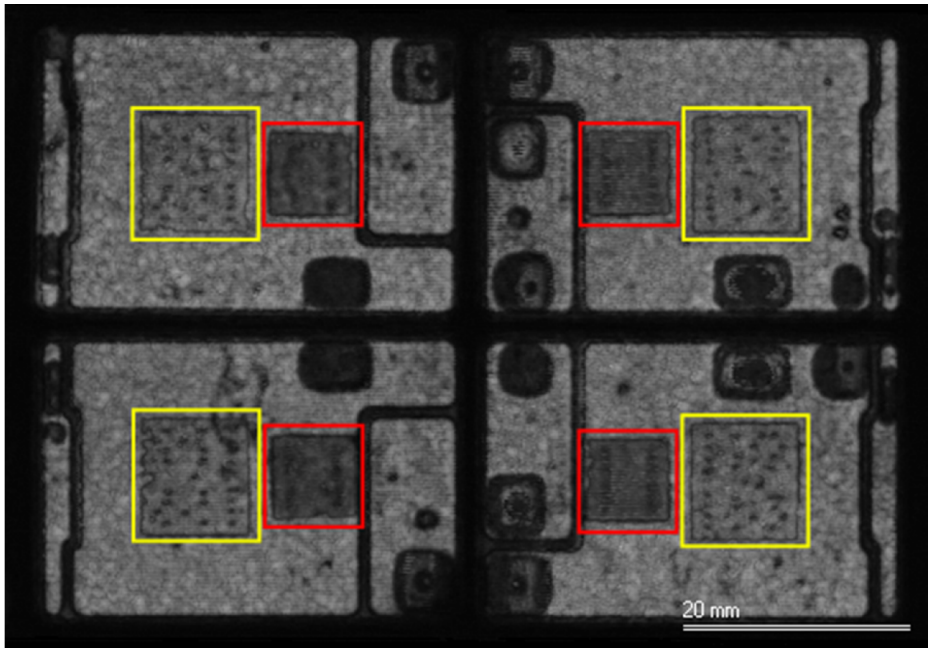


Figure 8.10 SAM image of the tested IGBT power module in its original condition before cycling. Four IGBTs (Yellow) can be seen with four free-wheeling diodes (Red).

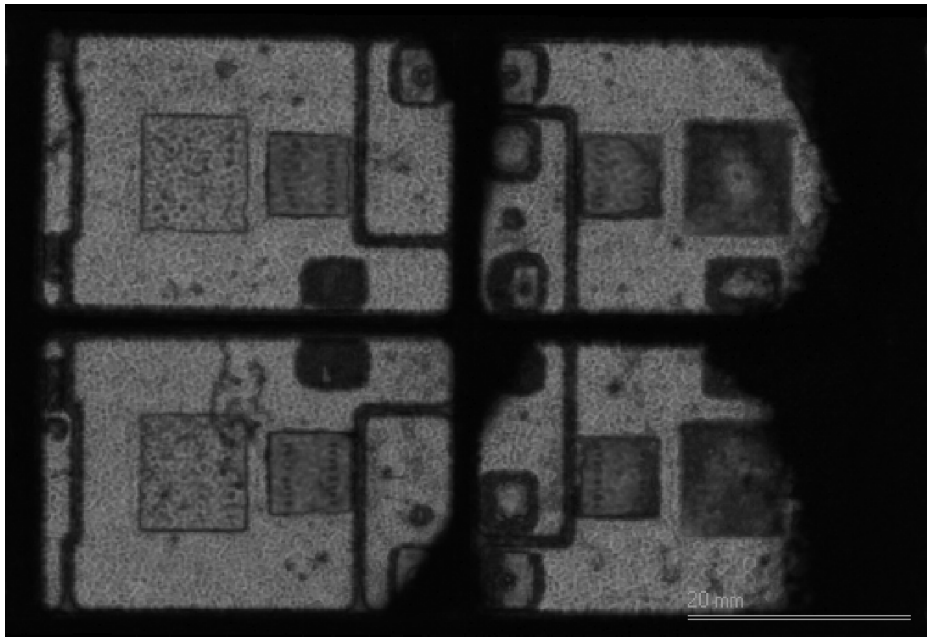


Figure 8.11 SAM image of the cycled IGBT power module after13500 cycles.

SAM characterization of the tested IGBT module is made before and after the power cycling test. Figure 8.10 shows the SAM image of the module in its original state before power cycling whereas Figure 8.11 shows the SAM image of the module after 13500 cycles. It can be seen from these images that cracking of the solder layer happens at the die-attach layer and the substrate

mount-down solder layer. This can be seen mainly on the substrate for the lower switch of the half-bridge module as it is this switch which was cycled. However, slight degradation at the substrate solder layer can also be observed at the corners of the upper switch adjacent to the cycled side of the module.

Cracking propagates from the corners of the substrate solder towards the centre of the module. The same happens for the die-attach layer where the cracks propagate from the corners of that layer towards the centre of the chip. The most significant cracking happens at the IGBT chips as they are the chips which are cycled whereas less cracking is observed at the die-attach layer of diodes.

Cracking of the substrate solder and the die-attach solder obstructs the heat flow from the IGBT devices towards the heatsink, resulting in an increased thermal resistance and an increased junction temperature T_J. The SAM observations are thus well-correlated with the observed trends in ΔT_J and R_{thja} presented earlier.

8.3.3Real-time Health Monitoring Results

The power cycling test was stopped at different intervals to allow the inverter test setup to be installed and the health monitoring framework to be operated. A sinusoidal current with a peak of 150A, a DC-link voltage of 100V and a switching frequency of 3kHz are used to operate the inverter which drives an inductive load of about 300µH. A dSPACE system is used for control and monitoring of the load current I_L, $V_{CE(ON)}$ and V_{th}. The Kalman filter algorithm for junction temperature estimation is also implemented on the dSAPCE system.

8.3.3.1Junction Temperature Estimate

Figure 8.12 shows the real-time junction temperature estimate T_J obtained by the Kalman filter algorithm during the normal operation of the inverter. The T_J data shown is obtained at multiple stages of the power cycling test. As the number of cycles increases, so the estimated junction temperature increases, in good agreement with the power cycling test results presented earlier. This demonstrates the ability of the junction temperature estimation algorithm to adapt to changes in the thermal path caused by aging effects.

It should be mentioned here that the cooling water temperature was maintained constant at 20°C for all of the observed results, thus preventing the variations in this parameter from disturbing the results of the estimated junction temperature. However, in a real-life application, this factor may not be maintained constant, and the T_J estimate would change accordingly, making it difficult to detect degradation of the thermal path by observing variations in T_J estimate. For this reason, the residual rather than T_J is used to detect degradation of the thermal path.

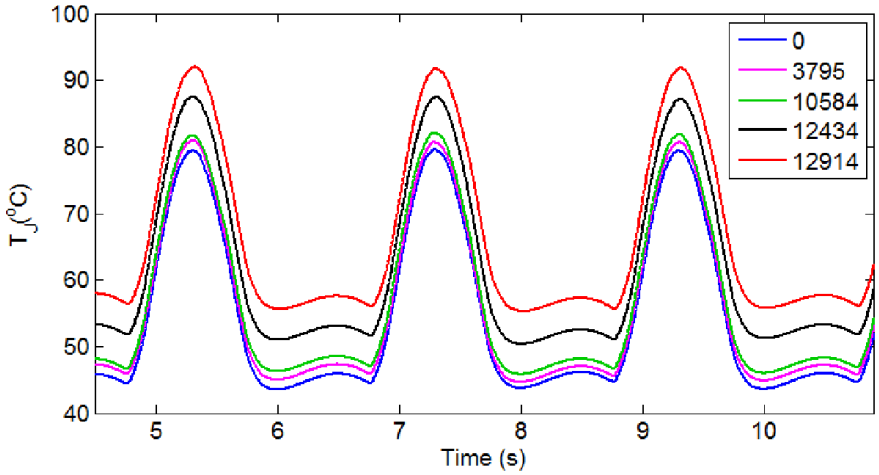


Figure 8.12 Real-time Junction temperature estimate given by Kalman Filter at multiple stages of the power cycling test. Power cycling is paused and the inverter is operated.

8.3.3.2Residuals

As detailed earlier, the residual represents the deviation between the measurement of T_J given by V_{th} and the estimate given by the Kalman filter. The residual signal is shown in Figure 8.13. This signal is non-deterministic and therefore, it is more convenient to look at its statistical distribution. Figure 8.14 shows the probability density function (PDF) of the residual. It can be seen that as the number of cycles progresses the distribution of the residual shifts to the right, revealing a change in the mean value of the residual. Figure 8.15 shows the mean value of the residual as function of number of cycles. Ideally, the value of the residual should start at zero, indicating a perfect match between the thermal model and the true thermal path. However, in practise this may not be the case because of the modelling errors that result during the original identification of the thermal model.

The residual mean follows a trend similar to the trend in R_{thja} shown earlier in Figure 8.8. After 11300 cycles the residual shows a significant jump which shows good agreement with the observed increment in V_{CE} and R_{thja} obtained during power cycling and which are indicative of the end-of-life period of the module. No significant change was seen on the residual produced by $V_{CE(ON)}$ and as no wire lifts are observed, this is to be expected. This is shown in the next section.

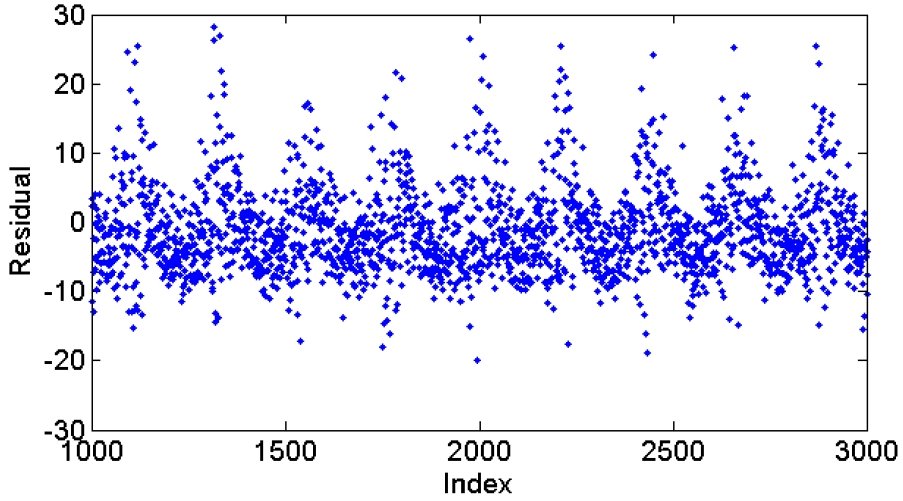


Figure 8.13 The raw signal of the generated residual

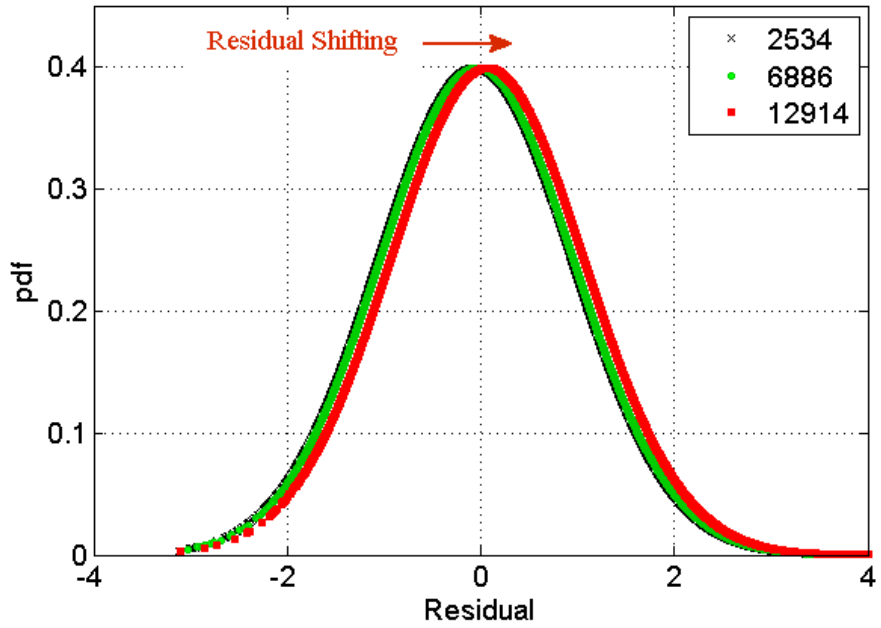


Figure 8.14 The statistical distribution (PDF) of the residual changes as number of cycles progresses indicating a change in the thermal path.

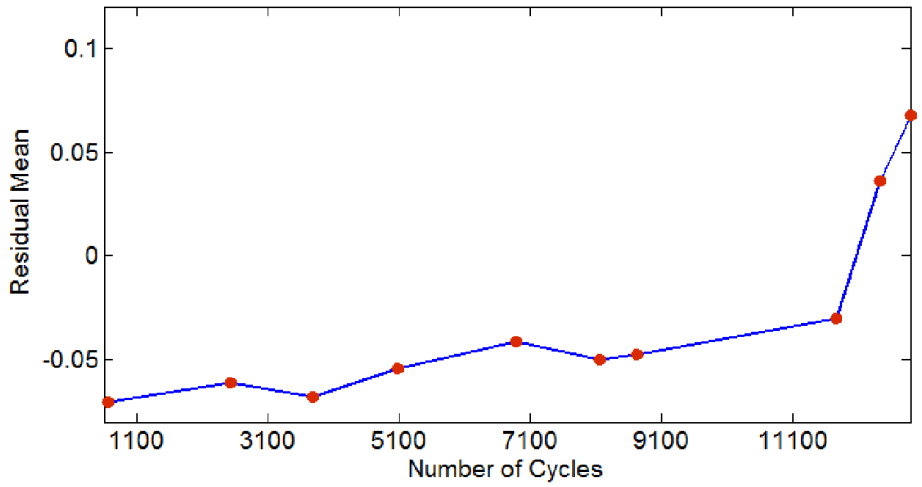


Figure 8.15 Mean of the Residual of T_J given by V_{th} as a function of number of cycles.

8.3.4Wire-bond Cut-off Test Results

Since the power cycling test activated only the solder fatigue mechanism in the cycled module and no wire-bond lift-off was observed, another test was required to validate the ability of the proposed framework to detect the failures of wire-bonds. However, since power cycling test is time consuming, an intentional wire-bond cutting is carried out. For this test, the power module was uncovered as shown in Figure 8.16 in order to allow access to the wire-bonds. After the module was uncovered, it was installed in the inverter test rig and the online measurements were recorded for the module in its original state (all wire-bonds connected). Then, the wire-bonds were cut-off one at a time while the inverter is shutdown. The online measurement was recorded after each wire-bond cut-off. The cuts were made on the wires connecting the IGBT and the diode chips as depicted in Figure 8.16. The cuts were made in sequence starting from one side of the chip and moving on one by one to the other side of the chip. Each chip has 8 wire-bonds such that a total of 16 wire-bonds on both chips are available.

Figure 8.17 shows the online measurement of the loading current I_L and the on-state voltage $V_{CE(ON)}$ at the original state and after each wire-bond cut-off. Figure 8.18 shows a magnified version of the $V_{CE(ON)}$ signal. It can be seen that as the wire-bonds are cut-off the $V_{CE(ON)}$ is increasing. That is because of

the increment in the electrical resistance of the IGBT module as the number of attached wire-bonds is reduced. Two significant jumps can be identified after the 4th cut and after the 8th cut. The 4th cut puts half of the chip out of operation whereas the 8th cut put the complete chip out of operation. The other chip in parallel is still connected after the 8th cut and all its wire-bonds are attached. It was noticed that the $V_{CE(ON)}$ measurement circuit was saturated after the 8th resulting in a distortion of the measurement signal as can be seen in Figure 8.18.

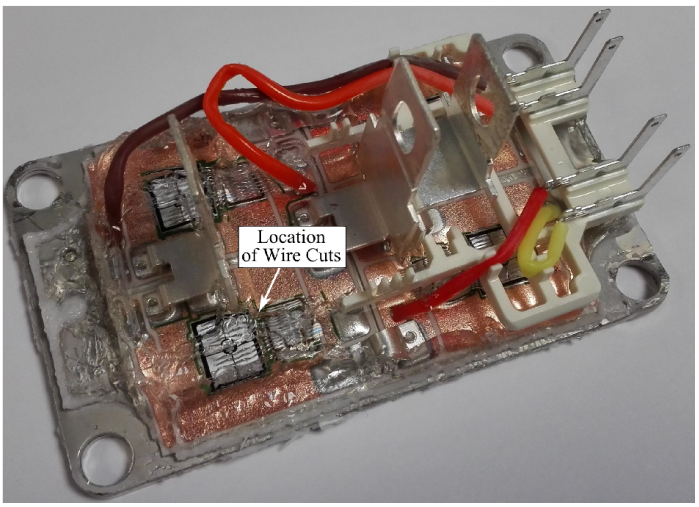


Figure 8.16 Uncovered IGBT power module used for the wire-bond cut-off test

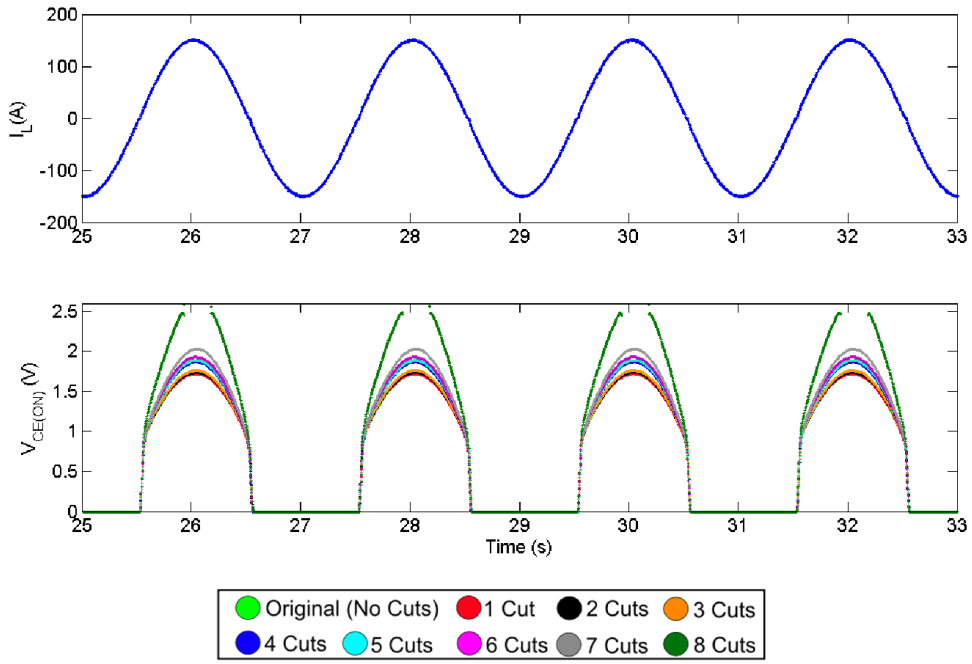


Figure 8.17 Raw Current I_L and $V_{CE(ON)}$ measurements at each wire-bond cut-off

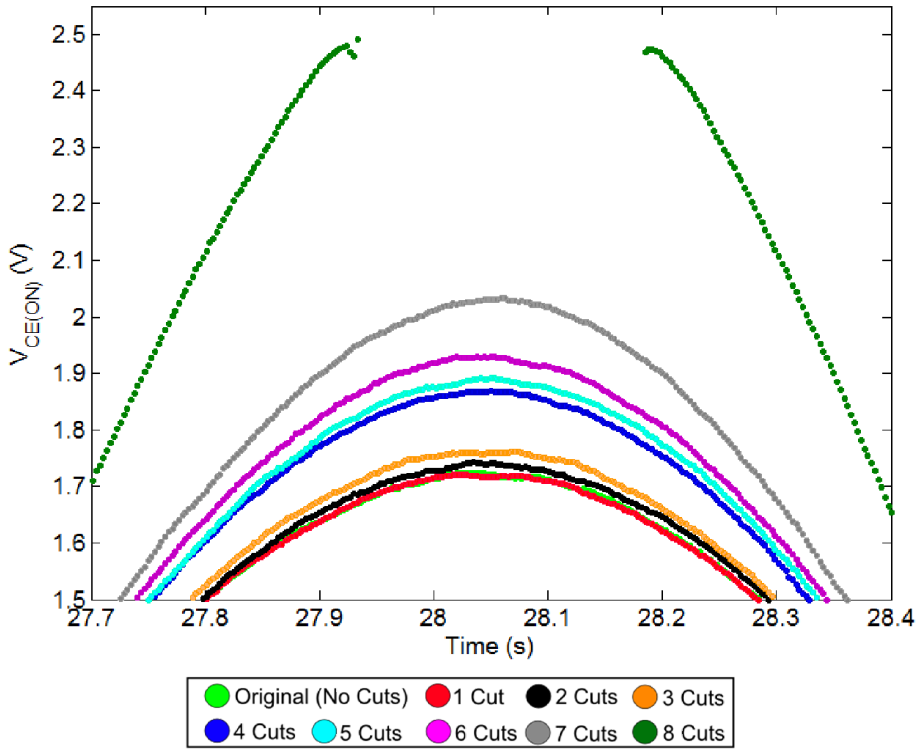


Figure 8.18 Raw $V_{CE(ON)}$ measurement at each wire-bond cut-off

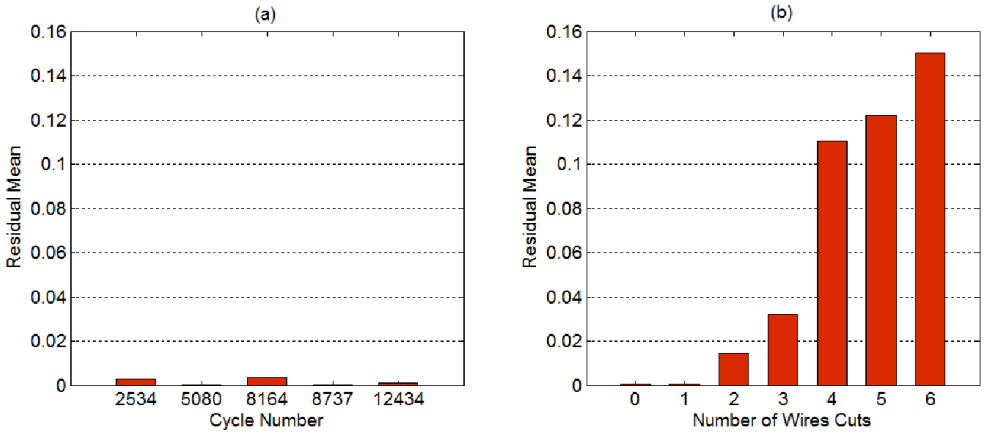


Figure 8.19 Mean value of the residual produced by $V_{CE(ON)}$ for (a) power cycling test (b) wire-bond cut-off test

Figure 8.19 shows the change in the mean value of the residual signal produced by the $V_{CE(ON)}$. It can be seen that the change in the mean value of the residual during the power cycling test shown in Figure 8.19 (a) is negligible compared to the change resulting from the loss of the wire-bonds shown in Figure 8.19 (b). The change Figure 8.19 (a) is a result of the noise. In Figure 8.19 (b) no obvious change can be seen after the 1st cut, however, a clear indication can be seen after the 2nd cut and afterwards. The change caused

by the loss of the 2nd wire-bond is larger than the variability caused by the noise. A significant change can be seen after the 4th cut when half of the IGBT chip is disconnected. From this data, it can be seen that the residual gives a quantitative estimate of the level of degradation in the wire-bonds within the module.

An increment in the junction temperature T_J was observed during the test as the wire-bonds were progressively cut. This is an expected result of the increment in the $V_{CE(ON)}$ which increases the conduction power loss of the module, in addition to the reduced active area of the module (two chips) which carries the load current.

8.4 Summary

This chapter presented the experimental results for validating the proposed health monitoring framework. A power cycling test was performed to activate the failure mechanisms in an IGBT power module. The power cycling test was interrupted at different intervals to allow operating the inverter and acquire the online measurements which is used by the health monitoring framework. Solder fatigue was activated by the power cycling test and the residual produced by the health monitoring framework showed indications of degraded thermal path which is confirmed by the measurement of R_{thja} and by SAM imaging.

No wire-bond lift-offs were noticed during the power cycling test, therefore an intentional wire-bond cut-offs were carried on a new module in order to examine the ability of the health monitoring framework to detect wire-bond failures. The results of the test showed a shift in the mean value of the residual proportional to the number of wire-bond failed giving a quantitative estimate of the level of degradation of the wire-bonds.

Chapter 9 Conclusion and Future Work

9.1 Conclusion

This thesis presented a methodology for monitoring the degradation of power modules in-service. The proposed methodology relies on online measurements of failure indicators to allow the detection of the two dominant failure mechanisms (solder fatigue and wire-bond lift-offs) while they are operating under normal in-circuit conditions.

In this work, the hardware required to collect online measurement of the failure indicators on the power converter has been developed. This hardware allows measurements of the on-state voltage $V_{CE(ON)}$ and the gate threshold voltage V_{th} to be obtained from the IGBT and transmitted through a capacitive isolation channel to a dSPACE digital system which is used for data processing. The gate threshold voltage V_{th} is used to estimate the junction temperature T_J utilizing the Kalman filter algorithm for improved accuracy. It is shown that the Kalman filter reduces the effect of measurement noise on the estimate of T_J and consequently enhances the detectability of the drift in T_J due to solder fatigue. On the other hand, $V_{CE(ON)}$ is an indicator of wire-bond failures and therefore it is measured online and used to monitor wire-bond lift-offs.

However, since the measurement of $V_{CE(ON)}$ and the estimate of T_J are obtained while the power converter is operating under normal conditions, these measurements are affected by the loading conditions (e.g. loading current) and the work environment (e.g. ambient temperature). Hence, the aging effects on the measured parameters are masked by these factors. Therefore, it is necessary to eliminate the effects of loading and environmental conditions from the online measurements such that drifts in the measurement resulting from module aging can be distinguished. To achieve this, a model-based approached has been proposed which seeks to identify deviations from models of the monitored power module in its original state.

An electrical model represents the I-V characteristic of the IGBT module under healthy conditions. Similarly, an RC equivalent network of thermal path represents the thermal conduction path under healthy conditions. The online measurements obtained from the power converter represent the current state of the power module. Comparing the online measurements with the model estimates of the failure indicators $V_{CE(ON)}$ and T_J produces residuals. These residuals are only sensitive to the drifts in the failure indicators from their healthy values. In this way, solder fatigue and wire-bond lift-offs were detected and distinguished using these residuals.

Experimental validation of the proposed methodology was performed by power cycling tests and by wire-bonds cut-off. The change in the residual that monitors the thermal path showed matching with the change in R_{thja} obtained during a power cycling test, revealing degradation in the thermal path. Similarly, the residual which monitors the wire-bonds showed a clear indication of failed wire-bonds as the wire-bonds are cut.

The results presented in this work establish the possibility of detecting and quantitatively estimating the level of degradation in the thermal path and the wire-bonds of IGBT power modules while they are in normal operation. It shows that the measurement of failure indicators such as $V_{CE(ON)}$ and T_J can be used to infer information about the packaging health state of the power module. It proves that it is possible to distinguish between solder fatigue and wire-bond lift-off by a proper choice of the measured parameters and by the combination of more than one failure indicator. The results have also demonstrated that an accurate estimate of junction temperature T_J is essential for efficient health monitoring since all electrical parameters are influenced by the temperature.

In conclusion, enabling online measurements of failure indicators and TSEPs, for example on a gate drive unit, can facilitate the monitoring and estimation of the level of degradation in power modules without the need to disrupt the operation of power converters. In this way, predictive maintenance can be enabled such that power modules can be monitored and replaced when they reach their end of life stage before they fail in an unpredictable manner,

thus improving converter availability and avoiding further damage and increased maintenance costs. This consequently saves effort and time required by periodical maintenance. In addition, it improves system protection of unpredicted failures that might result from degraded power modules.

9.2 Future Work

The results of this work provide an incentive to investigate new algorithms for health monitoring of power modules using model-based approach. However, there are many other approaches for data processing that can reveal drifts in online measurements such as Principle Component Analysis (PCA) which is a data-based method. Comparing these different approaches for health monitoring in terms of detectability, computing efficiency and robustness is desirable to determine the most appropriate algorithms for IGBT health monitoring.

Estimated drifts in failure indicators resulting from aging effect can be used to inform lifetime estimating algorithms. Typically, Physics-of-Failures (PoF) approaches are used to provide an estimate for the lifetime of the power modules for certain failure mechanisms. However, large uncertainties in the resulting lifetime estimates is a major concern for this kind of approach. This uncertainty can be reduced by introducing updated information of the current level of degradation in the power module which can be obtained from health monitoring algorithms, for example using model-based lifetime estimates. In this way, a more accurate Remaining Useful Lifetime (RUL) estimate can be obtained.

Since solder fatigue can happen at different locations in the thermal stack (die-attach and substrate solder layers), it is believed that the location of the cracking can be identified by examining the change in the dynamics of the junction temperature. The response of the thermal system can change according to the location of the cracking such that cracking at the die-attach layer affects the fast dynamics (short time constants) of the thermal response whereas the cracking at the substrate solder layer affects the slower dynamics (long time constants) of the thermal response. Consequently, cracking leaves different effects on the response of the thermal system according to the

location of the defects. However, an appropriate excitation input signal must be used to excite all the poles (time constants) of the thermal system in order to detect the location of cracking in the thermal stack. This requires a thorough investigation of the effect of cracking location on the dynamics of the thermal system and identification of appropriate ways to inject the excitation signal.

The main implementation platform for the health monitoring algorithm is the gate drive unit. None of the available gate drives implement the measurement hardware required for the online measurement of TSEPs and failure indicators. This integration requires the provision of a data transmission channel which allows the measured parameters to be extracted by a higher level controller. Therefore, it is essential to develop gate drives which integrate the required measurement circuitry and computing resources for data transmission and processing. In addition, the topology of the platform that implements the health monitoring functionality needs to be investigated. As the measurement data needs processing, this step can be implemented locally on the gate drive itself, then identified indications of degradation, rather than raw data, can be issued to the centralized control unit. Another approach can be achieved by transmitting the measurement data to a centralized control unit which receives the measurement data from the gate drive and performs the required processing. Different topologies can have different requirements of computing recourses and data transmission rates. This in turn has an effect on the cost of the gate drive units. Hence, a thorough investigation is required.

In this work, multiple thermos-sensitive electrical parameters TSEPs were reviewed which can be used to estimate junction temperature T_J. There are many research papers that explain the online measurement methods for these TSEPs. However, none of these researches consider the effect of measurement noise present in the measurement of each of these TSEPs. This noise has a negative effect on the accuracy of T_J estimate which consequently affects the health monitoring functionality. Therefore, it is important to compare all the available TSEPs from an online measurement point of view and investigate the effect of noise on each parameter.

Finally, wide band gap devices are gaining more attention. Therefore, this work should be extended by investigating potential thermos-sensitive electrical parameters and failure indicators of Silicon-Carbide (SiC) and Gallium-Nitride (GaN) devices and propose proper hardware circuitry to achieve the online measurements of the failure indicators. This also requires studying the failure mechanism of the SiC and GaN devices and the correlation between the identified failure indicators and the observed failures. Understanding these correlations constitutes the first step in interpreting the outcomes of any health monitoring approach.

Appendix A Test Setups

A.1 Double Pulse Tester

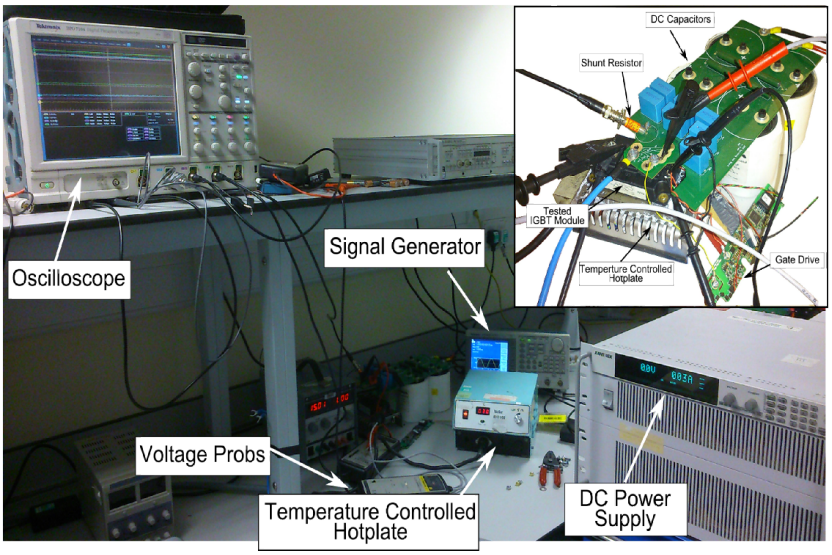
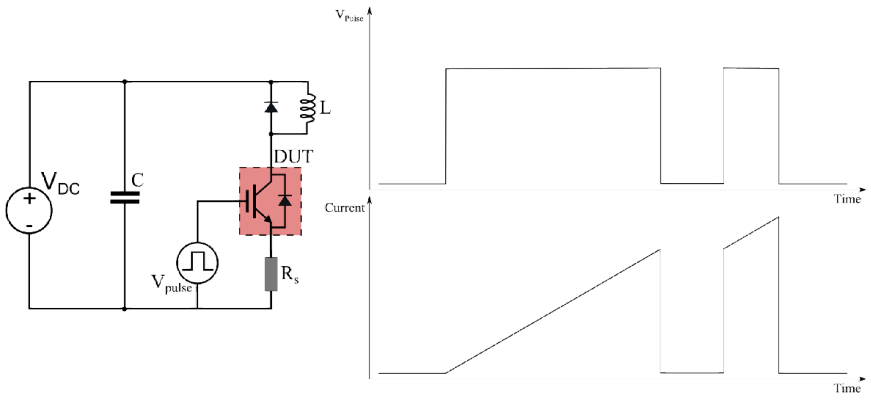


Figure A.1 Double Pulse Tester used to get the dynamic characteristics of IGBT



(a) **(b)**

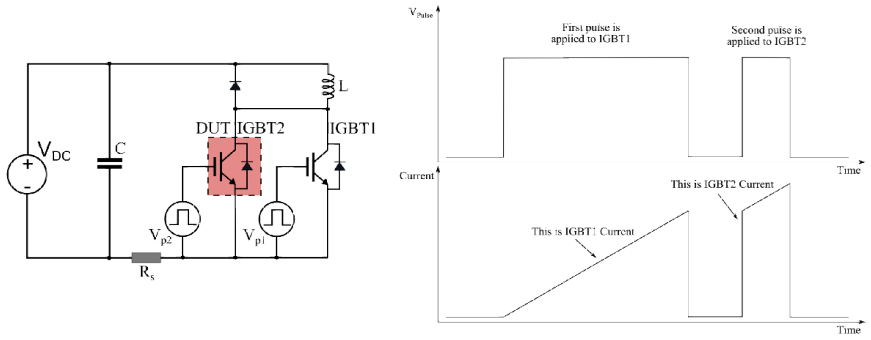
Figure A.2 (a) Schematic of the Double Pulse Tester. (b) The double pulse signal applied to IGBT gate and the corresponding current waveform

The Double Pulse tester is a setup that allows obtaining the dynamic switching characteristics of an IGBT during turn-on and turn-off transients. The test setup is shown in Figure A.1 and the schematic of the setup is shown in Figure A.2 (a). A signal generator V_{Pulse} is used to apply a double pulse gate signal to an IGBT. A DC power supply provides the required input voltage V_{DC} which is maintained at a constant level with the

help of the capacitor bank C. A shunt resistor R_s provides a mean to measure the current passing through the IGBT device. The inductor L constitutes the inductive load.

The first pulse is applied to the IGBT allowing the loading current to build up to the required level. The IGBT is then switched off and the current is commutated from the IGBT to circulate through the load L and the diode. Therefore, the load current does not reduce to zero as it is the case with the IGBT device current. The second pule is then applied to the IGBT and the current is commutated again through the load and the IGBT. This is depicted in Figure A.2 (b). It is during the second pulse where the switching characteristics of the IGBT are observed. If the IGBT is mounted on a temperature controlled hotplate, the variations of the switching characteristics with temperature can be observed.

A slight modification to the typical double pulse setup is used for the characterization of the IGBT with temperature. This modification is shown in Figure A.3 (a). An additional IGBT is connected in parallel with the tested IGBT (DUT). In this modified setup, the first pulse V_{P1} is applied to the gate of the IGBT1 to allow the load current to build up to the required level, whereas the second pulse V_{P2} is applied to the IGBT2 (DUT) which is the tested IGBT as shown in Figure A.3 (b). The reason for this modification is to avoid the self-heating effect of the tested IGBT during the first pulse caused by current passage. The self-heating can increase the temperature of the IGBT chip which is supposed to be constant and controlled by the hotplate. This modification allows preventing the first pulse from disturbing the controlled temperature of the tested IGBT (DUT) and consequently allows consistent calibration for IGBT characteristics with temperature.



(a) **(b)**

Figure A.3 (a) The modified Double Pulse Setup. (b) and the corresponding gating and current waveform

A.2 Full-bridge Inverter Setup

The test setup is shown in Figure A.4. The system utilizes two 1.2kV/400A half bridge IGBT power modules. The modules are uncovered and sprayed in black to allow thermal imaging with an infrared camera for verification. This is shown in Figure A.5. The modules are fixed on a copper water cooled heat sink and are connected to an inductive load of 300uH. A current transducer is used to measure the load current. The load current is controlled by a PI current controller which, along with the Kalman filter and PWM generator, is implemented on a dSPACE system. A schematic of the full-bridge inverter is shown in Figure A.6.

The dSPACE digital system includes a 16-channel Digital Waveform Output Board for generating pulse pattern signals with a resolution of 25ns and an output frequency up to 2MHz. Also included in the dSPACE system a 5-channels Analogue-to-Digital A/D Converter Board with 16-bit resolution and a selectable input voltage range of (±5V, ±10V). The sample time is resolution dependant where at 16-bit resolution it is 5us accounting for a maximum sampling frequency of 200kHz at 16-bit.

A unipolar switching scheme is used to generate a 1 kHz PWM switching signals taking into consideration the blanking time t_B required to prevent short circuiting of upper and lower devices of the same phase [134]. The blanking time is set to t_B=4us. The experimental measurement

of output voltage and output current of for an input DC voltage V_{DC}=100V and a reference modulation signal 120A/0.5Hz are shown in Figure A.7.

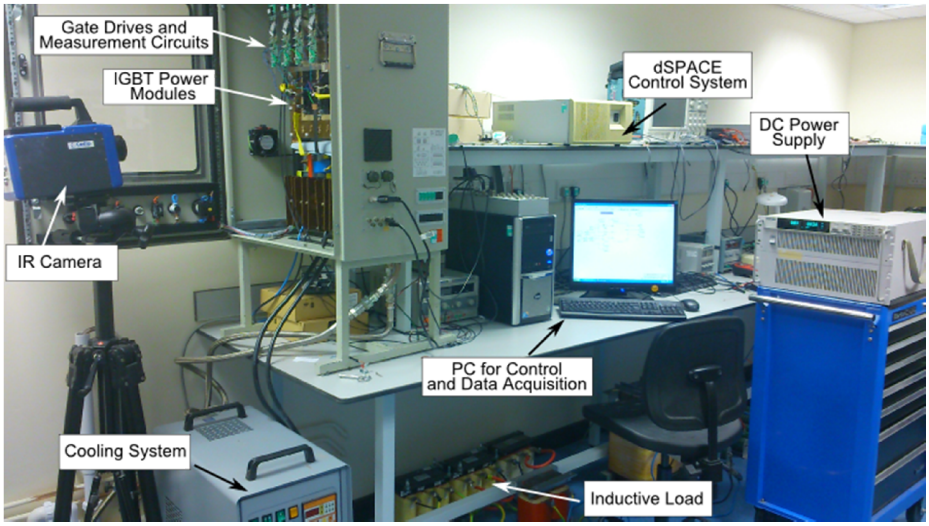


Figure A.4 A Photograph of The Full-bridge Inverter Test Setup

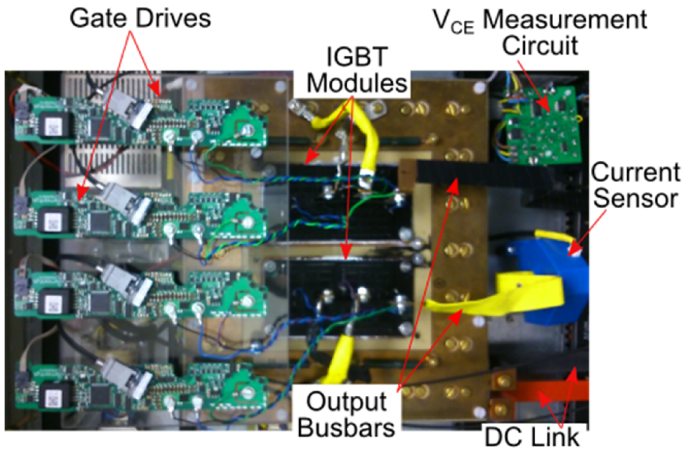


Figure A.5 A Photograph of The Full-bridge Inverter Test Setup

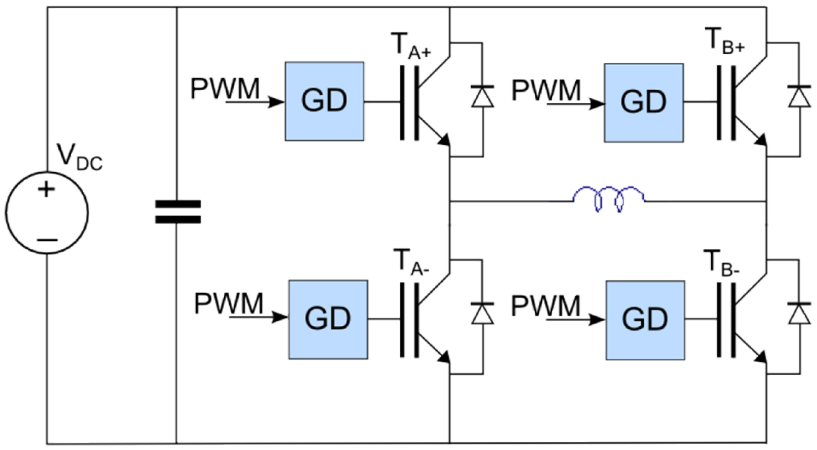


Figure A.6 A Schematic of the Full-bridge Inverter Test Setup

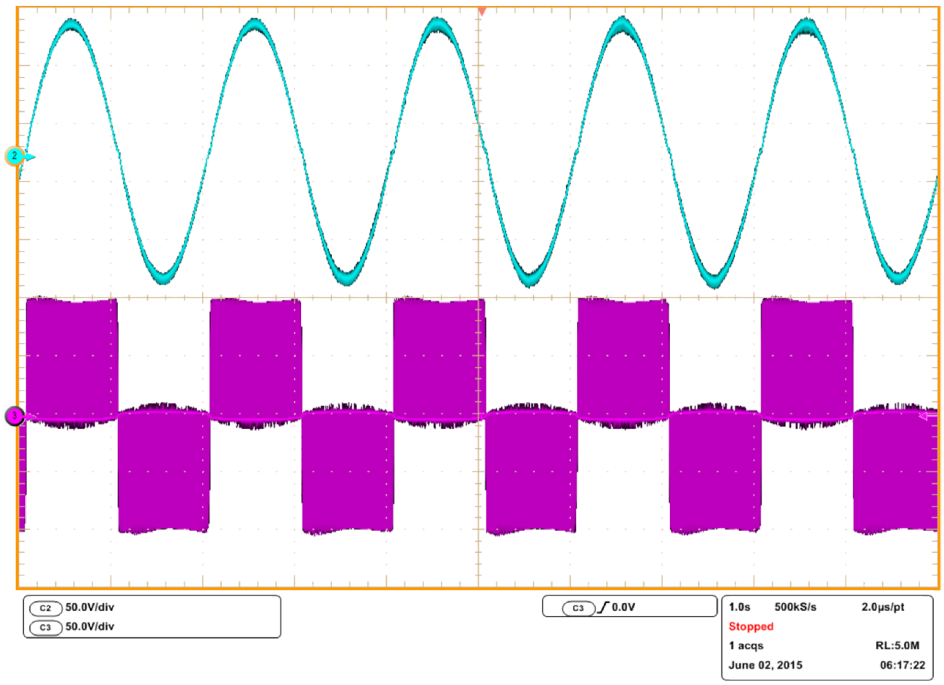


Figure A.7 Experimental Measurement of Inverter Output Current (Blue) and Output Voltage. (Pink). Current Modulation Signal is 120A/0.5Hz. V_{DC}=100V

A.3 Infrared Camera Measurement

An infrared camera with an accuracy of ±1°C and a sampling frequency of 50Hz is used to measure the temperature at the top surface of the IGBTs during inverter operation. This requires the IGBT modules to be uncovered and painted in matt black in order to increase the surface emissivity to 1 which allows more accurate measurement of the surface

temperature. The emissivity controls the infrared energy emitted by the monitored object. This infrared energy is used by the infrared camera to calculate the object temperature.

A thermal image of an IGBT module during inverter operation is shown in Figure A.8. Four IGBT devices and two freewheeling diodes can be seen. The thermal image shows temperature distribution across the surface of the IGBT module. A data logging software allows recording the time data of the surface temperature at any location on the surface.

A single temperature should be chosen among the multiple locations on the IGBT chips to be used for experimental verification of junction temperature estimate. Therefore, it is necessary to understand the representative temperature given by the used TSEP such as $V_{CE(ON)}$ or V_{th} in order to choose the right location of the thermal image to compare with. In [139] it is stated that the temperature measured by the voltage drop V_{CE} represents a weighted average across the chip surface temperatures where the weighting vector is proportional to the current density such that areas on the chip with the highest current density and highest temperature dominate the measurement of V_{CE}. Similarly, in [140] it is reported that the voltage drop across multiple paralleled IGBTs operating at different temperatures is a temperature weighted average with the hottest chip being the most influential.

Therefore, the maximum temperature among the monitored IGBTs is selected for comparison. The maximum temperature on each chip is found by examining the temperature profile across the chip diagonal and then the maximum temperature among the chips is chosen for validation.

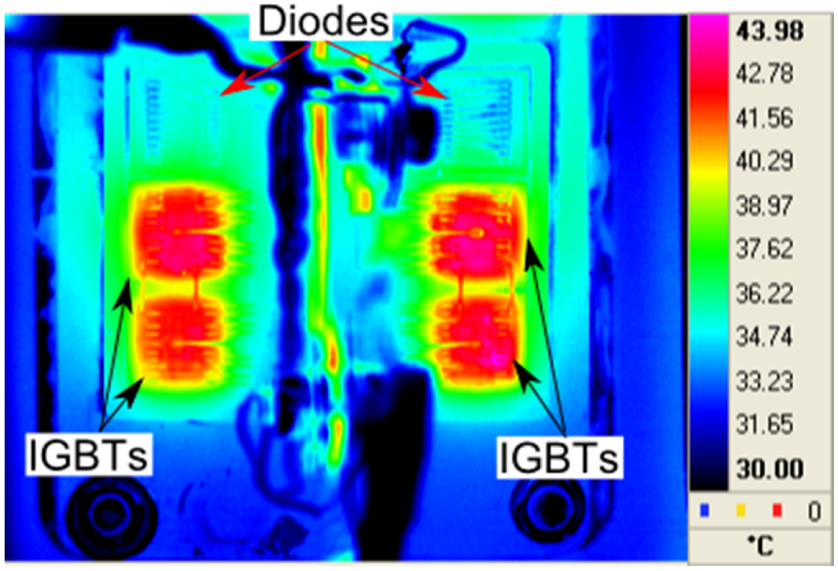


Figure A.8 A Thermal Image of the IGBT Module during Inverter Operation

Appendix B Measurement Circuits

B.1 Achieving Floating Measurements by Electrical Isolation

Achieving electrical isolation between measurement circuits mounted on the power converter/inverter and the PC-based data acquisition system (dSPACE) is essential to achieve accuracy of measurement and safety of user. This isolation is required because the signals measured on the power converter/inverter is non-ground-referenced or floating singals. That is the voltages on the power converter/inverter are not referenced to the "earth" ground. Instead, they are referenced to a common point which can be elevated at hundreds of volts from "earth" ground whereas the data acquisition end is strictly grounded to "earth" potential. This is illustrated in Figure B.1(a).

In such situation, the voltage difference between signal source (power converter) and signal destination (dSPACE) results in current loop to form and develop voltage drops at reference points that can range from microvolts up to hundreds of millivolts [141]. These voltages depend on the amount of current flowing and results in erroneous measurements. In addition, the current flowing through the signal return path can cause heating which can result in the signal return path to fail in an open circuit.

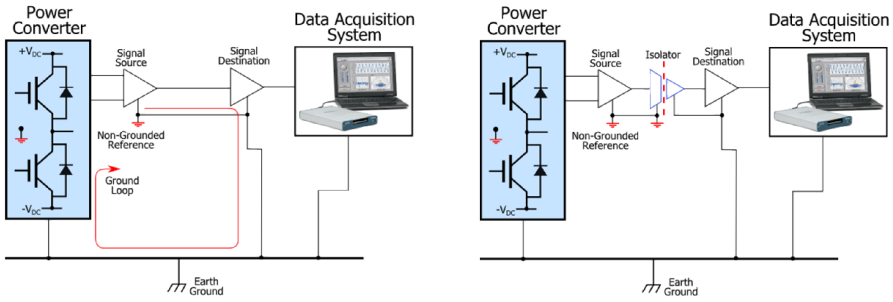


Figure B.1 (a) Current Loops can form between "Non-Ground Reference" and "Earth Ground". (b) Electrical Isolation breaks current loops andensures accuracy of measurement

In order to avoid that, an electrical isolation (optical, capacitive, galvanic) is required. This isolation provides seperate return path for the

signal in each side of the isolator. The signal is transmitted from non-ground-referenced side to the the "earth" grounded side through the isolator which breaks the current loop. This is illustrated in Figure B.1 (b). This isolation is achieved in practice using the Isolation Amplifier IC "ISO122" which provides a capacitive isolation barrier with an isolation voltage of 1.5kV.

B.2 Schematic of VCE(ON) Measurement Circuit

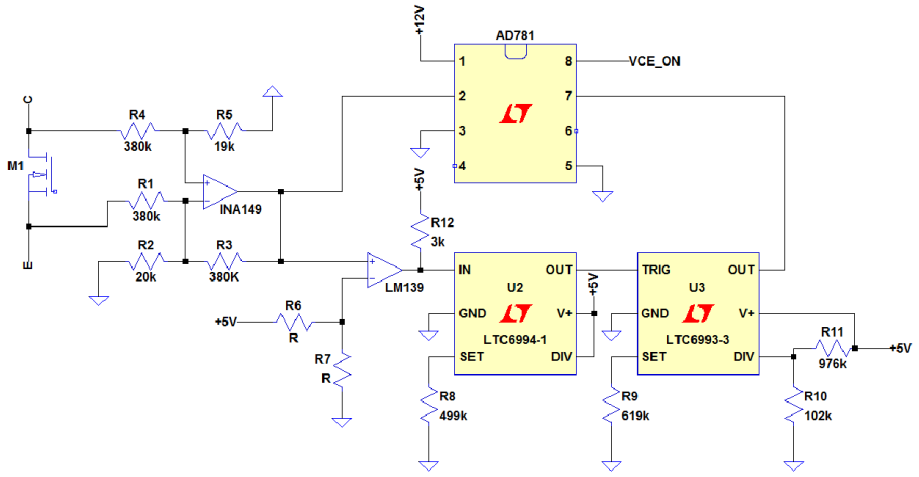


Figure B.2 Schematic of VCE(ON) measurement circuit

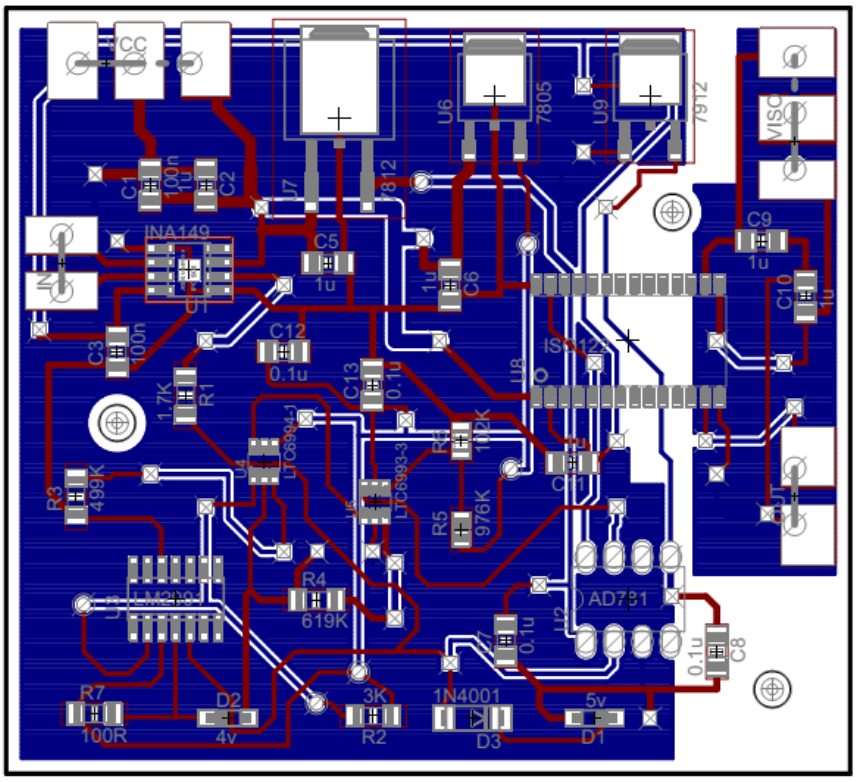


Figure B.3 Printed circuit board layout of VCE(ON) measurement circuit

B.3 Schematic of Vth Measurement Circuit

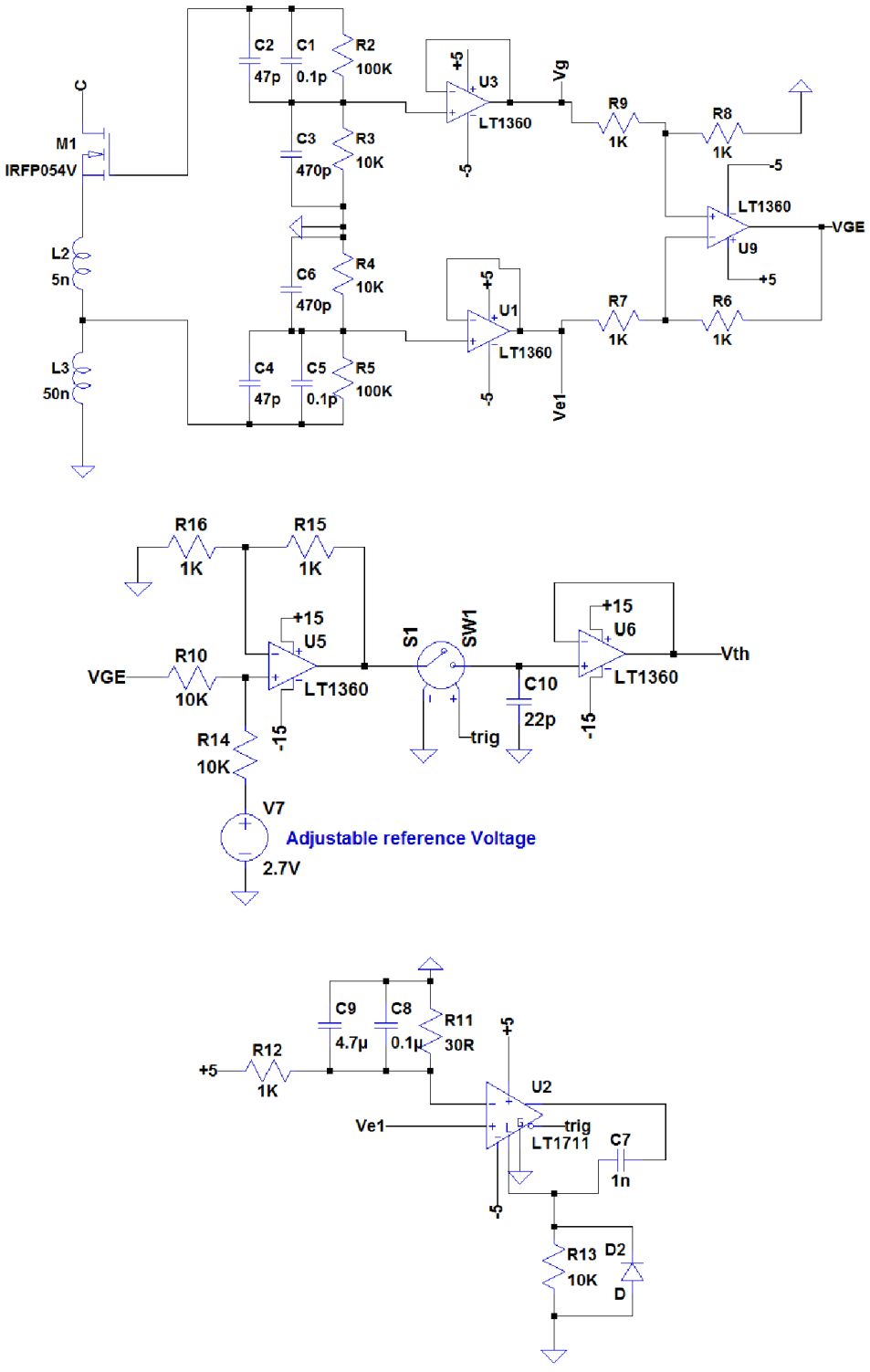


Figure B.4 Schematic of Vth Measurement Circuit

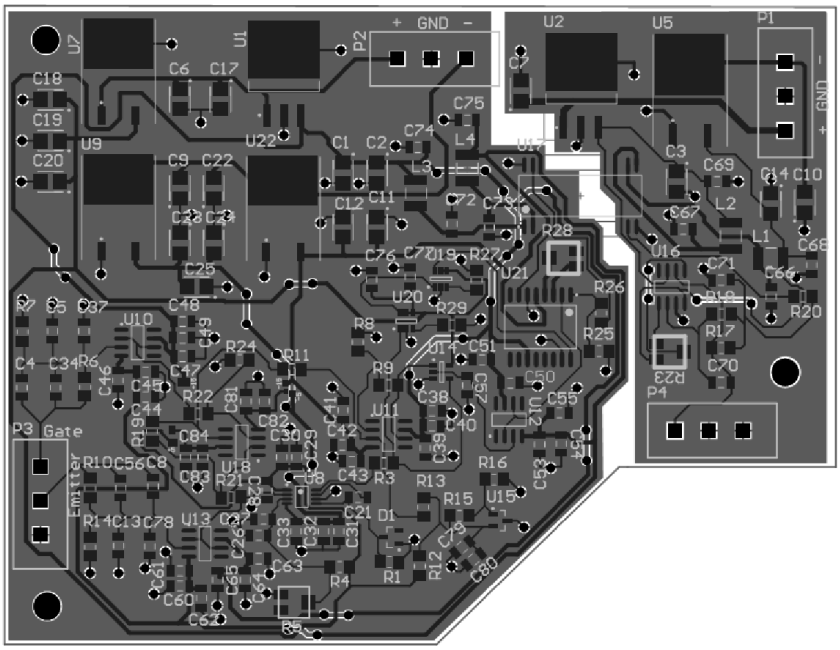


Figure B.5 Printed circuit board layout of Vth measurement circuit

Appendix C Code of the Kalman Filter

```
#define S_FUNCTION_NAME recursive_kalman_cross_coupling
#define S_FUNCTION_LEVEL 2

#include "simstruc.h"
#include "math.h"

#define U(element) (*uPtrs[element])  /* Pointer to Input
Port0 */
#define yv U(3)
#define N 7 //Model Order


static real_T A[N][N]={ {0.859773582982013,0,0,0,0,0,0} ,
                        {0,0.996432379136060,0,0,0,0,0} ,
                        {0,0,0.999616873411743,0,0,0,0} ,
                        {0,0,0,0.999962200714411,0,0,0},
                        {0,0,0,0,0.998966040903071,0,0},
                        {0,0,0,0,0,0.999143712371519,0},
                        {0,0,0,0,0,0,0.999951601534326}
                      };


static real_T B[N][3]={ {0.001989336565724 ,      0,      0}
,
                        {0.000113497059941 ,      0,      0}
,
                        {0.000011897720251 ,      0,      0}
,
                        {0.000002399954641 ,      0,      0}
,
                        {0 ,-0.025599362021296*1e-4,      0}
,
                        {0 , 0.154984090150479*1e-4,      0}
,
                        {0 , 0.033722270781426*1e-4,      0}
                      };


static real_T C[N]={1, 1, 1, 1, 1, 1, 1};

static real_T D[3]={0, 0, 1};

real_T K[N]=NULL;
real_T Xp[N] = NULL;

real_T Pp[N][N]=NULL;

real_T Pc[N][N]=NULL;

real_T Q[N][N]={{ 0.00000001,0,0,0,0,0,0} ,
                { 0,0.00000001,0,0,0,0,0} ,
                { 0,0,0.00000001,0,0,0,0} ,
                { 0,0,0,0.00000001,0,0,0} ,
                { 0,0,0,0,0.00000001,0,0} ,
                { 0,0,0,0,0,0.00000001,0} ,
```

```
                { 0,0,0,0,0,0,0.00000001}
                };

real_T G[N][N]={{ 1,0,0,0,0,0,0} ,
                { 0,1,0,0,0,0,0} ,
                { 0,0,1,0,0,0,0} ,
                { 0,0,0,1,0,0,0} ,
                { 0,0,0,0,1,0,0} ,
                { 0,0,0,0,0,1,0} ,
                { 0,0,0,0,0,0,1} ,
                };

real_T ye = 0.0;
real_T errcov = 0.0;
real_T err_norm=0.0;

real_T R=0.5;


void Multiplication(real_T A[N][N], real_T B[N][N], real_T
C[N][N]);
real_T Determinant(real_T A[4][4]);
void Transpose(real_T A[4][4],real_T C[4][4]);
void Cholesky_decompos(real_T A[4][4], real_T C[4][4]);
void Trangular_Inverse(real_T A[4][4], real_T C[4][4]);
void Inverse(real_T A[4][4], real_T C[4][4]);

/*====================*
 * S-function methods *
 *====================*/

/* Function: mdlInitializeSizes
================================================
 * Abstract:
 *    The sizes information is used by Simulink to determine
the S-function
 *    block's characteristics (number of inputs, outputs,
states, etc.).
 */
static void mdlInitializeSizes(SimStruct *S)
{
    ssSetNumSFcnParams(S, 0);  /* Number of expected
parameters */
    if (ssGetNumSFcnParams(S) != ssGetSFcnParamsCount(S)) {
        return; /* Parameter mismatch will be reported by
Simulink */
    }

    ssSetNumContStates(S, 0);
    ssSetNumDiscStates(S, N);

    if (!ssSetNumInputPorts(S, 1)) return;
    ssSetInputPortWidth(S, 0, 4);
    ssSetInputPortDirectFeedThrough(S, 0, 1);

    if (!ssSetNumOutputPorts(S, 2)) return;
    ssSetOutputPortWidth(S, 0, 2);
    ssSetOutputPortWidth(S, 1, 9);
```

```
    ssSetNumSampleTimes(S, 1);
    ssSetNumRWork(S, 0);
    ssSetNumIWork(S, 0);
    ssSetNumPWork(S, 0);
    ssSetNumModes(S, 0);
    ssSetNumNonsampledZCs(S, 0);
    ssSetSimStateCompliance(S, USE_DEFAULT_SIM_STATE);

    /* Take care when specifying exception free code - see
sfuntmpl_doc.c */
    ssSetOptions(S, SS_OPTION_EXCEPTION_FREE_CODE);
}



/* Function: mdlInitializeSampleTimes
=========================================
 * Abstract:
 *    Specify the sample time as 1.0
 */
static void mdlInitializeSampleTimes(SimStruct *S)
{
    ssSetSampleTime(S, 0, 0.001);
    ssSetOffsetTime(S, 0, 0.0);
    ssSetModelReferenceSampleTimeDefaultInheritance(S);
}

#define MDL_INITIALIZE_CONDITIONS
/* Function: mdlInitializeConditions
========================================
 * Abstract:
 *    Initialize both discrete states to one.
 */
static void mdlInitializeConditions(SimStruct *S)
{
    real_T *x0 = ssGetRealDiscStates(S);
    int_T  i;

    for (i=0;i<N;i++) {
        *x0++=0;
    }

    for (i=0;i<N;i++)
        Xp[i]=0;

    for (i=0;i<N;i++)
        K[i]=0;
}



static void mdlOutputs(SimStruct *S, int_T tid)
{
    real_T *y1    = ssGetOutputPortRealSignal(S,0);
    real_T *y2    = ssGetOutputPortRealSignal(S,1);
    real_T *x     = ssGetRealDiscStates(S);
    InputRealPtrsType uPtrs =
ssGetInputPortRealSignalPtrs(S,0);
```

```
    UNUSED_ARG(tid); /* not used in single tasking mode */

    y1[0]=ye;
    y1[1]=err_norm;

    y2[0]=x[0];
    y2[1]=x[1];
    y2[2]=x[2];
    y2[3]=x[3];
    y2[4]=x[4];
    y2[5]=x[5];
    y2[6]=x[6];

}


#define MDL_UPDATE
static void mdlUpdate(SimStruct *S, int_T tid)
{
    int i,j,a;
    real_T err=0.0;
    real_T temp1[N]=NULL;
    real_T temp3[N][N]=NULL;
    real_T temp2=0;

    real_T            *xc       = ssGetRealDiscStates(S);
    InputRealPtrsType uPtrs    =
ssGetInputPortRealSignalPtrs(S,0);

    UNUSED_ARG(tid); /* not used in single tasking mode */


ye=C[0]*Xp[0]+C[1]*Xp[1]+C[2]*Xp[2]+C[3]*Xp[3]+C[4]*Xp[4]+C[
5]*Xp[5]+C[6]*Xp[6]+D[0]*U(0)+D[1]*U(1)+D[2]*U(2);

    //K(k)=Pp(k)*C'*[C*Pp(k)*C'+R]^-1
    for(i=0;i<N;i++)
        for(j=0;j<N;j++)
            temp1[i]=temp1[i]+Pp[i][j]*C[j];
    for(i=0;i<N;i++)
        temp2=temp2+C[i]*temp1[i];

    //temp2=[C*Pp(k)*C']+R which is the error covariance
    temp2=temp2+R;

    for(i=0;i<N;i++)
        K[i]=temp1[i]/temp2;

    //e(k)=y(k)-yp(k)
    err=yv-ye;

    //error covariance
    errcov=temp2;

    //Normalized error
    err_norm=err*sqrt(1/temp2);
```

```
    //Parameter a determines availability of data a=1
(Available) a=0 (not Available)
    if(yv>0)
        a=1;
    else
        a=0;

    //Xc(k)=Xp(k)+a*K*e(k)
    for (i=0;i<N;i++)
        xc[i]= Xp[i]+a*K[i]*err;

    //Xp(k+1)=A*Xc(k)+B*U(k)
    for (i=0;i<N;i++)

Xp[i]=A[i][0]*xc[0]+A[i][1]*xc[1]+A[i][2]*xc[2]+A[i][3]*xc[3
]+A[i][4]*xc[4]+A[i][5]*xc[5]+A[i][6]*xc[6]+B[i][0]*U(0)+B[i
][1]*U(1)+B[i][2]*U(2);

    //Pc(k)=[I-K(k)*C]Pp(k)
    for (i=0;i<N;i++)
        for (j=0;j<N;j++)
            if (i==j)
                temp3[i][j]=1-K[i]*C[j];
            else
                temp3[i][j]=-K[i]*C[j];

    Multiplication(temp3,Pp,Pc);

    //Pp(k+1)=A*Pc(k)*A'+G*Q*G'
    Multiplication(Pc,A,temp3);
    Multiplication(A,temp3,Pp);
    for (i=0;i<N;i++)
        for (j=0;j<N;j++)
            Pp[i][j]=Pp[i][j]+Q[i][j];

    }


static void mdlTerminate(SimStruct *S)
{
    UNUSED_ARG(S); /* unused input argument */
}

#ifdef  MATLAB_MEX_FILE    /* Is this file being compiled as
a MEX-file? */
#include "simulink.c"      /* MEX-file interface mechanism
*/
#else
#include "cg_sfun.h"       /* Code generation registration
function */
#endif
```

References

[1] BP Statistical Review of World Energy 2014, 2014.

[2] Wind in Power: 2013 European Statistics, 2014.

[3] M.A.D. Mark Z. Jacobson, A Path to Sustainable Energy by 2030, Scientific American, 5 (2009) 58-65.

[4] M. Ciappa, Selected failure mechanisms of modern power modules, Microelectronics Reliability, 42 (2002) 653-667.

[5] P.W. Kalgren, M. Baybutt, A. Ginart, C. Minnella, M.J. Roemer, T. Dabney, Application of Prognostic Health Management in Digital Electronic Systems, Aerospace Conference, 2007 IEEE2007, pp. 1-9.

[6] S. Yang, D. Xiang, A. Bryant, P. Mawby, L. Ran, P. Tavner, Condition Monitoring for Device Reliability in Power Electronic Converters: A Review, IEEE Transactions on Power Electronics, 25 (2010) 2734-2752.

[7] S. Ramminger, P. Türkes, G. Wachutka, Crack mechanism in wire bonding joints, Microelectronics Reliability, 38 (1998) 1301-1305.

[8] H. Ye, M. Lin, C. Basaran, Failure modes and FEM analysis of power electronic packaging, Finite Elements in Analysis and Design, 38 (2002) 601-612.

[9] D.C. Katsis, J.D. van Wyk, Void-induced thermal impedance in power semiconductor modules: some transient temperature effects, IEEE Transactions on Industry Applications, 39 (2003) 1239-1246.

[10] MIL-HDBK-217F, 1991.

[11] J.B. Bowles, A survey of reliability-prediction procedures for microelectronic devices, Reliability, IEEE Transactions on, 41 (1992) 2-12.

[12] M.J. Cushing, D.E. Mortin, T.J. Stadterman, A. Malhotra, Comparison of electronics-reliability assessment approaches, Reliability, IEEE Transactions on, 42 (1993) 542-546.

[13] Y. Shaoyong, A. Bryant, P. Mawby, X. Dawei, R. Li, P. Tavner, An Industry-Based Survey of Reliability in Power Electronic Converters, IEEE Transactions on Industry Applications, 47 (2011) 1441-1451.

[14] S.F. P. Lyding, B. Hahn, P. Tavner, Reliability of the Electrical Parts of Wind Energy Systems - a statistical evaluation of practical experiences, EPE Wind Energy Chapter Symposium 2010, EPE Stafford, UK, 2010.

[15] E. Wolfgang, Examples for Failures in Power Electronics Systems, ECPE Tutorial ”Reliability of Power Electronic Systems”2007.

[16] F.W. Fuchs, Some diagnosis methods for voltage source inverters in variable speed drives with induction machines - a survey, Industrial Electronics Society, 2003. IECON '03. The 29th Annual Conference of the IEEE2003, pp. 1378-1385 Vol.1372.

[17] M.D. S. Faulstich, B. Hahn, K. Knorr, and K. Rohrig, Windenergy Report Germany 2008, 2008.

[18] L.M. Moore, H.N. Post, Five years of operating experience at a large, utility-scale photovoltaic generating plant, Progress in Photovoltaics: Research and Applications, 16 (2008) 249-259.

[19] S. Yantao, W. Bingsen, Survey on Reliability of Power Electronic Systems, Power Electronics, IEEE Transactions on, 28 (2013) 591-604.

[20] P.J. Tavnet, G.J.W. Van Bussel, F. Spinato, Machine and Converter Reliabilities in Wind Turbines, Power Electronics, Machines and Drives, 2006. The 3rd IET International Conference on2006, pp. 127-130.

[21] J. Guenther, M. Rothe, J. Hefer, A. Middendorf, K. Lang, Condition monitoring system adapted for photovoltaic power converter, Environment and Electrical Engineering (EEEIC), 2011 10th International Conference on2011, pp. 1-4.

[22] W. Huai, M. Ke, F. Blaabjerg, Design for reliability of power electronic systems, IECON 2012 - 38th Annual Conference on IEEE Industrial Electronics Society2012, pp. 33-44.

[23] D.L. Goodman, Prognostic methodology for deep submicron semiconductor failure modes, Components and Packaging Technologies, IEEE Transactions on, 24 (2001) 109-111.

[24] P. Chauhan, S. Mathew, M. Osterman, M. Pecht, <italic> In Situ</italic> Interconnect Failure Prediction Using Canaries, Device and Materials Reliability, IEEE Transactions on, 14 (2014) 826-832.

[25] R.D. Abhijit Dasgupta, Michael Azarian, Michael Osterman, Sony Mathew, and Michael Pecht, The Use of “Canaries” for Adaptive Health Management of Electronic Systems, The Second International Conference on Adaptive and Self-Adaptive Systems and Applications2010, pp. 176-183.

[26] N.M. Vichare, M.G. Pecht, Prognostics and health management of electronics, Components and Packaging Technologies, IEEE Transactions on, 29 (2006) 222-229.

[27] G.H. Ebel, Reliability physics in electronics: a historical view, Reliability, IEEE Transactions on, 47 (1998) SP379-SP389.

[28] J.R. Black, Mass Transport of Aluminum by Momentum Exchange with Conducting Electrons, Reliability Physics Symposium, 1967. Sixth Annual1967, pp. 148-159.

[29] E. Takeda, N. Suzuki, An empirical model for device degradation due to hot-carrier injection, Electron Device Letters, IEEE, 4 (1983) 111-113.

[30] C. Hu, A lucky-electron model of hot-electron emission, International Electron Devices Meeting Technical Digest, (1979) 22–25.

[31] L. YANG, A Damage-Based Time-Domain Wear-Out Model For Wire Bond Interconnects In Power Electronic Module, The University of Nottingham2013.

[32] B.J.B. White M., Microelectronics Reliability: Physics-of-Failure Based Modeling and Lifetime Evaluation, NASA2008.

[33] J. Evans, M.J. Cushing, P. Lall, R. Bauernschub, A physics-of-failure (POF) approach to addressing device reliability in accelerated testing of MCMs, Multi-Chip Module Conference, 1995. MCMC-95, Proceedings., 1995 IEEE1995, pp. 14-25.

[34] M. Pecht, B. Tuchband, N. Vichare, Y. Qu Jian, Prognostics and Health Monitoring of Electronics, Thermal, Mechanical and Multi-Physics Simulation Experiments in Microelectronics and Micro-Systems, 2007. EuroSime 2007. International Conference on2007, pp. 1-8.

[35] S. Mathew, D. Das, R. Rossenberger, M. Pecht, Failure mechanisms based prognostics, Prognostics and Health Management, 2008. PHM 2008. International Conference on2008, pp. 1-6.

[36] J.B. Bowles, Fundamentals of Failure Modes and Effects Analysis, Tutorial Notes Annual Reliability and Maintainability Symposium2003.

[37] N.E. DOWLING, FATIGUE FAILURE PREDICTIONS FOR COMPLICATED STRESS-STRAIN HISTORIES.

[38] M. Musallam, C.M. Johnson, Y. Chunyan, C. Bailey, M. Mermet-Guyennet, Real-time life consumption power modules prognosis using on-line rainflow algorithm in metro applications, Energy Conversion Congress and Exposition (ECCE), 2010 IEEE2010, pp. 970-977.

[39] A. Ramakrishnan, M.G. Pecht, A life consumption monitoring methodology for electronic systems, Components and Packaging Technologies, IEEE Transactions on, 26 (2003) 625-634.

[40] L. Fan, M. Pecht, D. Lau, N. Gang, The research and application of the method of life consumption monitoring based on physics of failure, Electronic Packaging Technology & High Density Packaging (ICEPT-HDP), 2010 11th International Conference on2010, pp. 1027-1033.

[41] A. Dasgupta, Failure mechanism models for cyclic fatigue, Reliability, IEEE Transactions on, 42 (1993) 548-555.

[42] W. Engelmaier, Fatigue Life of Leadless Chip Carrier Solder Joints During Power Cycling, Components, Hybrids, and Manufacturing Technology, IEEE Transactions on, 6 (1983) 232-237.

[43] M. Held, P. Jacob, G. Nicoletti, P. Scacco, M.H. Poech, Fast power cycling test of IGBT modules in traction application, Proceedings of International Conference on Power Electronics and Drive Systems1997, pp. 425-430 vol.421.

[44] A. Fatemi, L. Yang, Cumulative fatigue damage and life prediction theories: a survey of the state of the art for homogeneous materials, International Journal of Fatigue, 20 (1998) 9-34.

[45] M. Musallam, C.M. Johnson, Y. Chunyan, L. Hua, C. Bailey, In-service life consumption estimation in power modules, Power Electronics and Motion Control Conference, 2008. EPE-PEMC 2008. 13th2008, pp. 76-83.

[46] C.Y. Yin, H. Lu, M. Musallam, C. Bailey, C.M. Johnson, In-service reliability assessment of solder interconnect in power electronics modules, Prognostics and Health Management Conference, 2010. PHM '10.2010, pp. 1-5.

[47] D. Wagenitz, A. Hambrecht, S. Dieckerhoff, Lifetime Evaluation of IGBT Power Modules Applying a Nonlinear Saturation Voltage Observer, Integrated Power Electronics Systems (CIPS), 2012 7th International Conference on2012, pp. 1-5.

[48] R. Bayerer, T. Herrmann, T. Licht, J. Lutz, M. Feller, Model for Power Cycling lifetime of IGBT Modules Â¿ various factors influencing lifetime, Integrated Power Systems (CIPS), 2008 5th International Conference on, (2008) 1-6.

[49] H. Hui, P.A. Mawby, A Lifetime Estimation Technique for Voltage Source Inverters, IEEE Transactions on Power Electronics, 28 (2013) 4113-4119.

[50] M.S. Bohllander, J. ; Lutz, J. ; Pettertei, A., Extraction of Power Cycles in Offshore Wind Power Applications, PCIM Europe 2011, Nuremburg, Germany.

[51] M. Pecht, R. Jaai, A prognostics and health management roadmap for information and electronics-rich systems, Microelectronics Reliability, 50 (2010) 317-323.

[52] N. Patil, D. Das, Y. Chunyan, L. Hua, C. Bailey, M. Pecht, A fusion approach to IGBT power module prognostics, Thermal, Mechanical and Multi-Physics simulation and Experiments in Microelectronics and Microsystems, 2009. EuroSimE 2009. 10th International Conference on2009, pp. 1-5.

[53] X.-S. Si, W. Wang, C.-H. Hu, D.-H. Zhou, Remaining useful life estimation – A review on the statistical data driven approaches, European Journal of Operational Research, 213 (2011) 1-14.

[54] N.D. Singpurwalla, The Hazard Potential, Journal of the American Statistical Association, 101 (2006) 1705-1717.

[55] G. Jie, N. Vichare, T. Tracy, M. Pecht, Prognostics Implementation Methods for Electronics, Reliability and Maintainability Symposium, 2007. RAMS '07. Annual2007, pp. 101-106.

[56] N. Patil, D. Das, M. Pecht, A prognostic approach for non-punch through and field stop IGBTs, Microelectronics Reliability, 52 (2012) 482-488.

[57] B. Saha, J.R. Celaya, P.F. Wysocki, K.F. Goebel, Towards prognostics for electronics components, Aerospace conference, 2009 IEEE2009, pp. 1-7.

[58] S. Saha, J.R. Celaya, V. Vashchenko, S. Mahiuddin, K.F. Goebel, Accelerated aging with electrical overstress and prognostics for power MOSFETs, Energytech, 2011 IEEE2011, pp. 1-6.

[59] J.R. Celaya, A. Saxena, S. Saha, K. Goebel, Prognostics of Power MOSFETs under Thermal Stress Accelerated Aging using Data-Driven and Model-Based Methodologies, Annual Conference of the Prognostics and Health Management Society2011.

[60] A. Oukaour, B. Tala-Ighil, B. Pouderoux, M. Tounsi, M. Bouarroudj-Berkani, S. Lefebvre, B. Boudart, Ageing defect detection on IGBT power modules by artificial training methods based on pattern recognition, Microelectronics Reliability, 51 (2011) 386-391.

[61] K. Goebel, P. Bonissone, Prognostic information fusion for constant load systems, Information Fusion, 2005 8th International Conference on2005, pp. 9 pp.

[62] M.J. Roemer, G.J. Kacprzynski, R.F. Orsagh, Assessment of data and knowledge fusion strategies for prognostics and health management, Aerospace Conference, 2001, IEEE Proceedings.2001, pp. 2979-2988 vol.2976.

[63] C. Shunfeng, M. Pecht, A fusion prognostics method for remaining useful life prediction of electronic products, Automation Science and Engineering, 2009. CASE 2009. IEEE International Conference on2009, pp. 102-107.

[64] P. Smets, What is Dempster-Shafer's model?, Advances in the Dempster-Shafer theory of evidence, John Wiley & Sons, New York, NY, USA, 1994 pp. 5 - 34.

[65] P. Smets, R. Kennes, The transferable belief model, Artificial Intelligence, 66 (1994) 191-234.

[66] Z. Guangfan, K. Chiman, R. Xu, N. Vichare, M. Pecht, An Enhanced Prognostic Model for Intermittent Failures in Digital Electronics, Aerospace Conference, 2007 IEEE2007, pp. 1-8.

[67] K. Goebel, N. Eklund, P. Bonanni, PROGNOSTIC FUSION FOR UNCERTAINTY REDUCTION, 2007.

[68] X. Dawei, R. Li, P. Tavner, A. Bryant, Y. Shaoyong, P. Mawby, Monitoring Solder Fatigue in a Power Module Using Case-Above-Ambient Temperature Rise, IEEE Transactions on Industry Applications, 47 (2011) 2578-2591.

[69] X. Dawei, L. Ran, P. Tavner, Y. Shaoyong, A. Bryant, P. Mawby, Condition Monitoring Power Module Solder Fatigue Using Inverter Harmonic Identification, IEEE Transactions on Power Electronics, 27 (2012) 235-247.

[70] J.M. Anderson, R.W. Cox, On-line condition monitoring for MOSFET and IGBT switches in digitally controlled drives, Energy Conversion Congress and Exposition (ECCE), 2011 IEEE2011, pp. 3920-3927.

[71] M. Musallam, C.M. Johnson, Monitoring through-life thermal path degradation using real time thermal models, Power Electronics Specialists Conference, 2008. PESC 2008. IEEE2008, pp. 738-743.

[72] B. Ji, V. Pickert, B. Zahawi, M. Zhang, In-situ bond wire health monitoring circuit for IGBT power modules, Power Electronics, Machines and Drives (PEMD 2012), 6th IET International Conference on2012, pp. 1-6.

[73] J. Lehmann, M. Netzel, R. Herzer, S. Pawel, Method for electrical detection of bond wire lift-off for power semiconductors, Power Semiconductor Devices and ICs, 2003. Proceedings. ISPSD '03. 2003 IEEE 15th International Symposium on2003, pp. 333-336.

[74] M.N. Özışık, Basic Heat Transfer, McGraw-Hill1977.

[75] U. Drofenik, J.W. Kolar, Teaching thermal design of power electronic systems with web-based interactive educational software, Applied Power Electronics Conference and Exposition, 2003. APEC '03. Eighteenth Annual IEEE2003, pp. 1029-1036 vol.1022.

[76] B.J. Baliga, Power Semiconductor Devices, Wadsworth Publishing Co Inc1995.

[77] K.E. Mortenson, Transistor Junction Temperature as a Function of Time, Proceedings of the IRE, 45 (1957) 504-513.

[78] N. Zommer, D.L. Feucht, Analytical thermal response of a multiple-layer device under the semi-infinite approximation, Electron Devices, IEEE Transactions on, 25 (1978) 441-448.

[79] R. David, Computerized Thermal Analysis of Hybrid Circuits, Parts, Hybrids, and Packaging, IEEE Transactions on, 13 (1977) 283-290.

[80] W.E. Newell, Transient Thermal Analysis of Solid-State Power Devices--Making a Dreaded Process Easy, IEEE Transactions on Industry Applications, IA-12 (1976) 405-420.

[81] P. Nance, M. Marz, Thermal Modeling of Power-electronic Systems, in: Infineon (Ed.) Infineon Technologies Application Note 05/20002000.

[82] F.N. Masana, A closed form solution of junction to substrate thermal resistance in semiconductor chips, Components, Packaging, and Manufacturing Technology, Part A, IEEE Transactions on, 19 (1996) 539-545.

[83] F.N. Masana, A new approach to the dynamic thermal modelling of semiconductor packages, Microelectronics Reliability, 41 (2001) 901-912.

[84] V. Székely, T. Van Bien, Fine structure of heat flow path in semiconductor devices: A measurement and identification method, Solid-State Electronics, 31 (1988) 1363-1368.

[85] F.F. Kuo, Network analysis and synthesis, John Wiley & Sons Australia, Limited1966.

[86] P.E. Bagnoli, C.E. Casarosa, M. Ciampi, E. Dallago, Thermal resistance analysis by induced transient (TRAIT) method for power electronic devices thermal characterization. I. Fundamentals and theory, Power Electronics, IEEE Transactions on, 13 (1998) 1208-1219.

[87] P.E. Bagnoli, C.E. Casarosa, E. Dallago, M. Nardoni, Thermal resistance analysis by induced transient (TRAIT) method for power electronic devices thermal characterization. II. Practice and experiments, Power Electronics, IEEE Transactions on, 13 (1998) 1220-1228.

[88] G.L. Skibinski, W.A. Sethares, Thermal parameter estimation using recursive identification, Power Electronics, IEEE Transactions on, 6 (1991) 228-239.

[89] P.R. Strickland, The Thermal Equivalent Circuit of a Transistor, IBM Journal of Research and Development, 3 (1959) 35-45.

[90] A. Zanin, SKiM IGBT Modules in: Semikron (Ed.) Technical Explanations2013.

[91] D. Domes, U. Schwarzer, IGBT-Module integrated Current and Temperature Sense Features based on Sigma-Delta Converter, PCIM Europe, Nuremberg, Germany, 2009.

[92] E.R.M. John F. Donlon, Takashi Igarashi, Mitsuhara Tabata, Takahiro Inoue, High Performance Intelligent Power Modules Using CSTBT Chips with Integrated Temperature Sensor, Power Electronics Technology Conference 20032003.

[93] P.-L. Doumergue, Using NTC Temperature Sensors Integrated into Power Modules - APT0406, 2004.

[94] M. Musallam, C.M. Johnson, Real-Time Compact Thermal Models for Health Management of Power Electronics, IEEE Transactions on Power Electronics, 25 (2010) 1416-1425.

[95] R. Schnell, M. Bayer, S. Geissmann, Thermal design and temperature ratings of IGBT modules, in: ABB (Ed.) Application Note 5SYA 2093-002013.

[96] O. Karim, J.C. Crebier, C. Gillot, C. Schaeffer, B. Mallet, E. Gimet, Heat transfer coefficient for water cooled heat sink: application for standard power modules cooling at high temperature, Power Electronics Specialists Conference, 2001. PESC. 2001 IEEE 32nd Annual2001, pp. 1938-1943 vol. 1934.

[97] G.C. James, V. Pickert, M. Cade, A thermal model for a multichip device with changing cooling conditions, Power Electronics, Machines and Drives, 2008. PEMD 2008. 4th IET Conference on2008, pp. 310-314.

[98] A.J. Yerman, J.F. Burgess, R.O. Carlson, C.A. Neugebauer, Hot Spots Caused by Voids and Cracks in the Chip Mountdown Medium in Power Semiconductor Packaging, IEEE Transactions on Components, Hybrids, and Manufacturing Technology, 6 (1983) 473-479.

[99] C. Huifeng, J. Bing, V. Pickert, C. Wenping, Real-Time Temperature Estimation for Power MOSFETs Considering Thermal Aging Effects, Device and Materials Reliability, IEEE Transactions on, 14 (2014) 220-228.

[100] W. Ze, Q. Wei, T. Bo, Q. Liyan, An effective heat propagation path-based online adaptive thermal model for IGBT modules, Applied Power Electronics Conference and Exposition (APEC), 2014 Twenty-Ninth Annual IEEE2014, pp. 513-518.

[101] Z. Jakopovic, Z. Bencic, F. Kolonic, Important properties of transient thermal impedance for MOS-gated power semiconductors, Industrial Electronics, 1999. ISIE '99. Proceedings of the IEEE International Symposium on1999, pp. 574-578 vol.572.

[102] N. Baker, M. Liserre, L. Dupont, Y. Avenas, Junction temperature measurements via thermo-sensitive electrical parameters and their application to condition monitoring and active thermal control of power converters, 39th Annual Conference of the IEEE Industrial Electronics Society, IECON 20132013, pp. 942-948.

[103] L. Dupont, Y. Avenas, P. Jeannin, Comparison of junction temperature evaluations in a power IGBT module using an IR camera and three thermo-sensitive electrical parameters, Applied Power Electronics Conference and Exposition (APEC), 2012 Twenty-Seventh Annual IEEE2012, pp. 182-189.

[104] N. Baker, M. Liserre, L. Dupont, Y. Avenas, Improved Reliability of Power Modules: A Review of Online Junction Temperature Measurement Methods, Industrial Electronics Magazine, IEEE, 8 (2014) 17-27.

[105] Y. Avenas, L. Dupont, Z. Khatir, Temperature Measurement of Power Semiconductor Devices by Thermo-Sensitive Electrical Parameters: A Review, IEEE Transactions on Power Electronics, 27 (2012) 3081-3092.

[106] H. Kuhn, A. Mertens, On-line junction temperature measurement of IGBTs based on temperature sensitive electrical parameters, Power Electronics and Applications, 2009. EPE '09. 13th European Conference on2009, pp. 1-10.

[107] A. Rashed, F. Forest, J.J. Huselstein, T. Martire, P. Enrici, On-line [T<inf>J</inf>, V<inf>ce</inf>] monitoring of IGBTs stressed by fast power cycling tests, Power Electronics and Applications (EPE), 2013 15th European Conference on2013, pp. 1-9.

[108] P. Ghimire, K.B. Pedersen, A.R.d. Vega, B. Rannestad, S. Munk-Nielsen, P.B. Thogersen, A real time measurement of junction temperature variation in high power IGBT modules for wind power converter application, Integrated Power Systems (CIPS), 2014 8th International Conference on2014, pp. 1-6.

[109] K. Yong-Seok, S. Seung-Ki, On-line estimation of IGBT junction temperature using on-state voltage drop, Industry Applications

Conference, 1998. Thirty-Third IAS Annual Meeting. The 1998 IEEE1998, pp. 853-859 vol.852.

[110] H. Chen, V. Pickert, D.J. Atkinson, L.S. Pritchard, On-line Monitoring of the MOSFET Device Junction Temperature by Computation of the Threshold Voltage, Power Electronics, Machines and Drives, 2006. The 3rd IET International Conference on2006, pp. 440-444.

[111] I.Č. Bahun, Neven; Jakopović, ŽEljko, Real-Time Measurement of IGBTs Operating Temperature, Automatika: Journal for Control, Measurement, Electronics, 52 (2011) 295–305.

[112] V. Sundaramoorthy, E. Bianda, R. Bloch, I. Nistor, G. Knapp, A. Heinemann, Online estimation of IGBT junction temperature (Tj) using gate-emitter voltage (Vge) at turn-off, 15th European Conference on Power Electronics and Applications (EPE)2013, pp. 1-10.

[113] S.M. Sze, K.K. Ng, Physics of Semiconductor Devices, Wiley2006.

[114] V.K. Sundaramoorthy, E. Bianda, R. Bloch, F. Zurfluh, Simultaneous online estimation of junction temperature and current of IGBTs using emitter-auxiliary emitter parasitic inductance, PCIM Europe 2014; International Exhibition and Conference for Power Electronics, Intelligent Motion, Renewable Energy and Energy Management; Proceedings of2014, pp. 1-8.

[115] A. Bryant, Y. Shaoyong, P. Mawby, X. Dawei, L. Ran, P. Tavner, P.R. Palmer, Investigation Into IGBT dV/dt During Turn-Off and Its Temperature Dependence, Power Electronics, IEEE Transactions on, 26 (2011) 3019-3031.

[116] X. Dawei, Y. Shaoyong, R. Li, P. Tavner, A. Bryant, P. Mawby, Change of terminal characteristics of a Voltage-source-inverter (VSI) due to semiconductor device degradation, Power Electronics and Applications, 2009. EPE '09. 13th European Conference on2009, pp. 1-10.

[117] W. Brekel, T. Duetemeyer, G. Puk, O. Schilling, Time Resolved In Situ TvjMeasurements of 6.5kV IGBTs during Inverter Operation, PCIM Europe2009.

[118] M.-M.B. Marco Denk, An IGBT Driver Concept with Integrated Real-Time Junction Temperature Measurement, PCIM Europe, Nuremberg, Germany, 2014.

[119] N. Baker, S. Munk-Nielsen, M. Liserre, F. Iannuzzo, Online junction temperature measurement via internal gate resistance during turn-on, Power Electronics and Applications (EPE'14-ECCE Europe), 2014 16th European Conference on2014, pp. 1-10.

[120] M.S. Grewal, A.P. Andrews, Kalman Filtering: Theory and Practice Using MATLAB, Wiley2011.

[121] H.W. Sorenson, Least-squares estimation: from Gauss to Kalman, Spectrum, IEEE, 7 (1970) 63-68.

[122] B.D.O. Anderson, J.B. Moore, Optimal Filtering, Dover Publications2012.

[123] R.E. Kalman, A New Approach to Linear Filtering and Prediction Problems, Journal of Fluids Engineering, 82 (1960) 35-45.

[124] T. Kailath, The innovations approach to detection and estimation theory, Proceedings of the IEEE, 58 (1970) 680-695.

[125] Y.C. Ho, R. Lee, A Bayesian approach to problems in stochastic estimation and control, Automatic Control, IEEE Transactions on, 9 (1964) 333-339.

[126] E. Chow, A.S. Willsky, Analytical redundancy and the design of robust failure detection systems, Automatic Control, IEEE Transactions on, 29 (1984) 603-614.

[127] R. Isermann, Supervision, fault-detection and fault-diagnosis methods — An introduction, Control Engineering Practice, 5 (1997) 639-652.

[128] J.Gertler, Analytical redundancy methods in fault detection and isolation - survey and synthesis, IFAC Fault Detection, Supervision and Safety for Technical Processes, Baden-Baden, Germany, 1991, pp. 9-21.

[129] R.K. Mehra, J. Peschon, An innovations approach to fault detection and diagnosis in dynamic systems, Automatica, 7 (1971) 637-640.

[130] B.J. Baliga, Temperature behavior of insulated gate transistor characteristics, Solid-State Electronics, 28 (1985) 289-297.

[131] L. Zhou, S. Zhou, M. Xu, Investigation of gate voltage oscillations in an IGBT module after partial bond wires lift-off, Microelectronics Reliability, 53 (2013) 282-287.

[132] J.W. Sofia, Fundamentals of Thermal Resistance Measurement, Analysis Tech1995.

[133] M.J. Whitehead, C.M. Johnson, Determination of Thermal Cross-Coupling Effects in Multi-Device Power Electronic Modules, The 3rd IET International Conference on Power Electronics, Machines and Drives.2006, pp. 261-265.

[134] N. Mohan, T.M. Undeland, W.P. Robbins, Power electronics: converters, applications, and design, John Wiley & Sons2003.

[135] J.D. Cryer, K.S. Chan, Time Series Analysis: With Applications in R, Springer2008.

[136] N.S. Nise, Control Systems Engineering, John Wiley & Sons, Incorporated2011.

[137] T. Bruckner, S. Bernet, Estimation and Measurement of Junction Temperatures in a Three-Level Voltage Source Converter, Power Electronics, IEEE Transactions on, 22 (2007) 3-12.

[138] MentorGraphics, Power Tester 1500A.

[139] R. Schmidt, U. Scheuermann, Using the chip as a temperature sensor- The influence of steep lateral temperature gradients on the Vce(T)-measurement, EPE '09. 13th European Conference on Power Electronics and Applications, 2009.2009, pp. 1-9.

[140] E. Farjah, R. Perret, Application and analysis of thermosensitive parameters in the case of hybrid power modules, Industry Applications Society Annual Meeting, 1994., Conference Record of the 1994 IEEE1994, pp. 1284-1289 vol.1282.

[141] Tektronix, Fundamentals of Floating Measurements and Isolated Input Oscilloscopes, 2005.