Advanced packaging and integration solutions for enhanced performance power convertors

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Abstract

The design of novel solutions for packaging and integration of power semiconductor devices to deliver switches with advanced performance and reliability is very important aspect of power electronics technology evolution. The advancement of technology in this area is committed to bring significant improvements in the design and implementation of power converters particularly in the enhancement of efficiency, higher power density and better cooling system as compared to the state-of-the-art solutions.

A power module is a combination of either multiple semiconductor or discrete devices which are connected to form an electrical circuit of certain structure. They are mainly constructed with a stack of four main parts *(power semiconductor devices, insulating substrate with circuit conductor, baseplate, and interconnecting material encapsulated in a plastic case)* and each of these parts is of a different material. Some of the interfaces within the module are prone to failure with thermal cycling such as wire-bond, solder die attach and substrate. Therefore reducing the number of interfaces in the assembly will greatly reduce the thermal resistance from the junction to ambient and yields noticeable increase of performance.

Moreover, using solid posts as opposed to wires to connect the surface of vertical power components enable a significant improvement in power density as compared with standard modules based on wire bond technology. Additionally, the replacement of wires with such posts drastically reduces the

distributed parasitic inductance, together with double-sided cooling of the devices, results in an increase of performance and reliability of the components and assemblies.

In this work, 70um thick Infineon technology power devices which are rated at 600V/200A were used for the assembly of a Bi-directional switch based converter and discussing the challenges and tradeoffs related to selecting processes and materials. Encapsulation is also one of the important factors in making of power module to protect the power chip and the interconnections from moisture, chemicals, dust, gases, and so on. Here, insulation process was carried out for a given prototype using silicone gel; however, it is worth to note the existing challenge on insulating a very small gap between the sandwich layers of the prototype as compared with the standard planar power module structure. A basic partial discharge test was also taken to demonstrate the performance of the insulation.

This research has presented an advanced modular integration approach for power device packaging demonstrating the progress beyond the state of the art in power system assembly by proposing a solution which significantly improves electromagnetic and thermomechanical performance of the power module. In particular, fully bond wireless, double sided cooling and layout symmetry are key aspects. The proposed approach is transferable to many topologies having extra benefit of restricting the impact of single device or switch failure on the general system accessibility.

Acknowledgements

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To my dearest Mother and my wife

Behind every successful man, there is a strong, wise, and hardworking woman!

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Abbreviations

ABC	Active brazed copper
A/D	Analogue to digital
AC	Alternating current
AMB	Active metal brazed
BDS	Bi-directional switch
CAE	Computer aided engineering
CCS	Code Composer Studio
CFD	Computational fluid dynamics
CMC	Copper molybdenum copper
CTE	Coefficient of thermal expansion
CWC	Copper tungsten copper
DAI	Dimple array interconnection
DBC	Direct bond copper
DC	Direct current
DSP	Digital signal processor
EMI	Electromagnetic interference
FDM	Finite difference method
FEM	Finite element method
FPGA	Field programmable gate array
GTO	Gate turn-off thyristor
HC	Hard commutation
HPI	Host port interface
HTV	High temperature vulcanising
IGBT	Insulated gate bipolar transistor
IGCT	Integrated gate commutated thyristor

IMC	Intermetallic component
IPC	Industry association for printed circuit
IR	International rectifier
MOSFET	Metal oxide synchronise field effect transistor
MPa	Mega Pascal
NC	Natural commutation
NPT	Non-Punch through
PC	Personal computer
PCB	Printed circuit board
ppm	Point per million
PT	Punch through
PTH	Plated through hole
TPM	Transfer-molded-Power-Module
RTV	Room temperature vulcanising
SW	Switch
SMD	Surface mount device
TIM	Thermal interface material
USB	Universal serial bus

Nomenclature

Ag	Silver	Mo	Molybdenum
Al	Aluminium	NiP	Nickel phosphorous
AlN	Aluminium nitride	Pd	Lead
Al_2O_3	Aluminium oxide	Si	Silicon
AlSiC	Aluminium silicon carbide	SiC	Silicon carbide
Au	Gold	Si_3N_4	Silicon nitride
^0C	Degree centigrade	Sn	Tin
Cu	Copper	SnAgCu	Tin silver copper
GaN	Gallium nitride		

α	Fatigue ductility exponent	μ	Magnetic permeability
ε	Strain accumulation, Emissivity of the object	ρ	density of the material
$\Delta\varepsilon_{cr}$	creep strain accumulation per thermal cycle	σ	Electrical conductivity, Equivalent stress, Boltzmann constant ($5.6703x10^{-8}$ W/m^2k^4)
θ_{max}	maximum input displacement angle	ω_{in}	Input frequency
Ω	ohm	Φ	heat flux

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Chapter 1:
Introduction

1.1. Power electronics packaging

Power electronics is an enabling technology in the application of solid-state electronics that achieves conversion of electric power from one form to another, using a combination of high-power semiconductor devices and passive components. It also refers to a subject of research in electrical engineering which deals with design, control, computation, advance packaging and integration solutions. The general task of power electronics is to process and control the power conversion from an electrical source to an electrical load in a highly efficient, highly reliable and cost-effective way [1].

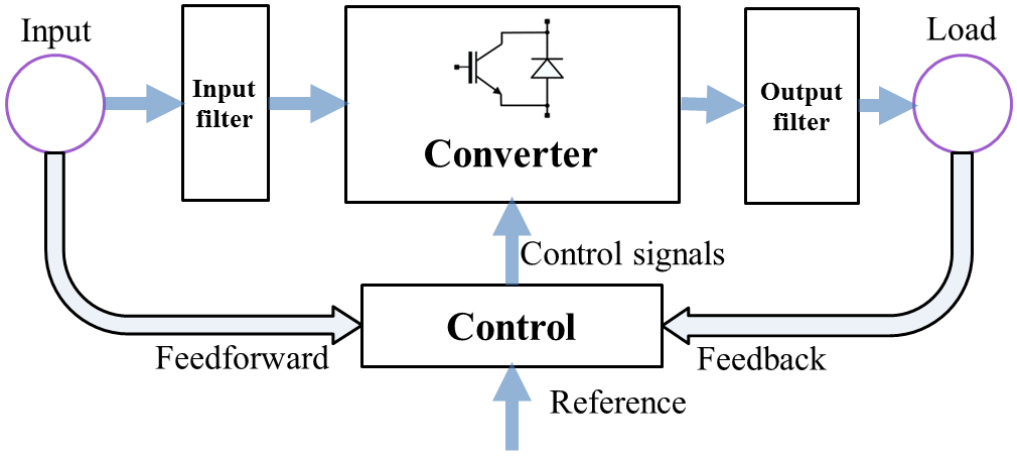


Fig.1.1 Scheme of principle of a power converter system

Looking into the generic power electronic converter block diagram of Fig.1.1, the whole system is a combination of active components, passive components, and control unit. The active components are the power semiconductor components that turn on and off the power flow within the converter. The passive components are transformers, filters, inductors and capacitors which temporarily store energy within the system. Different magnetic, dielectric and insulation materials are used depending on the operating of switching frequency, voltage, cooling method and level of integration. Considering power density, smaller passive component can be achieved using high switching frequency operation. However, the power losses associated with such high switching frequencies can prohibit semiconductor devices from delivering the required performance. Control unit can be either analogue or digital electronics circuits containing converter signals, processors, and sensors to control the energy transfer within the converter in a way that the output signals follow the computed reference signal.

Power devices used in power converters such as THYRISTORs, Gate Turn-Off thyristors (GTOs), Bipolar Junction Transistors (BJT), Insulated Gate Bipolar Transistors (IGBTs), Metal-Oxide Semiconductor Field-Effect Transistors (MOSFETs) and Diodes are strategically very important in terms of increased power capability, ease of control and cost. The development of such power devices provides a direct link between integrated circuits and power converters construction. This relationship has led to power device development with regard to the structure, design, size reduction, and manufacturing.

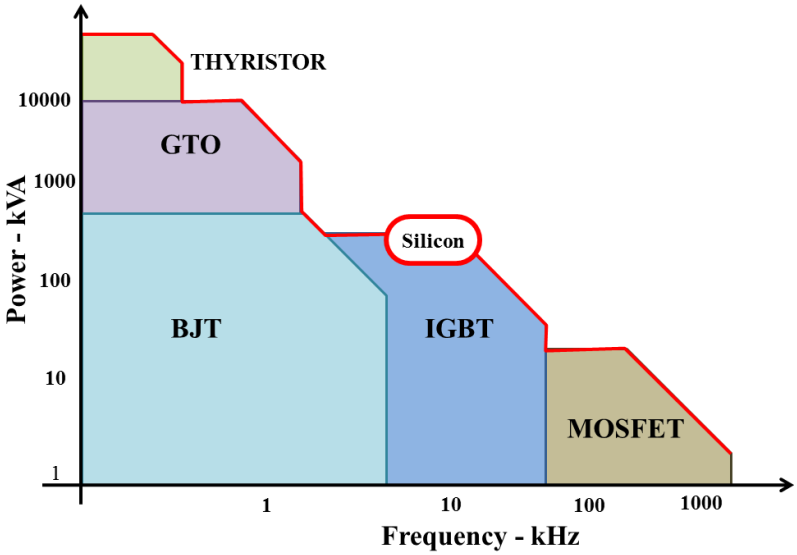


Fig.1.2. Trends to power semiconductor device capabilities [2].

Looking from the trend in Fig.1.2, thyristors are basically three-junction pn-pn devices rated at 5 - 7KV which are commonly used in adjustable AC (alternative circuit) rectifier circuits, especially in high power converters higher than 10MVA. However their frequency capability is less than 1 kHz. Conversely, GTOs are basically thyristor-type devices that can be turned on by positive gate current pulse. Unlike the thyristors, they can be turned off by applying negative gate current pulse. They are available up to 10MVA and 3KV ratings operating at 1 kHz. BJTs are current controlled devices where the base current is supplied continuously to keep them switched on. They are available in power ratings of 500kVA and voltage rating up to 1.4KV which can operate at switching frequency range of few hundred hertz to 10 kHz. MOSFETs are voltage controlled unipolar devices having high switching frequency capability up to 1GHz. They have relatively low power handling capabilities rated at around 10kVA and 1KV voltage rating. IGBTs are voltage controlled bipolar devices constructed with integration of power MOSFET and BJT devices in monolithic form to make use of the advantages of both power devices. Hence, they can operate at a frequency higher than BJT and rated at

higher power than MOSFET. IGBTs are available in the range of 2 – 3.3KV voltage ratings [1].

Over the last twenty years, industrial and research efforts in the field of power electronics have been making progress toward high-frequency operation, which results in great improvement in converter performance, miniaturization in size and weight. Progress in semiconductor technology aims to yield higher power ratings, and higher switching frequencies for a given device size. Fig.1.2 illustrates the summary of the power device capabilities and a qualitative comparison observation is depicted in Table 1.1. The development trends for power semiconductor device have been focused on increasing current and voltage levels to reduce the number of devices needed, increasing operational temperature to reduce the demands on the cooling system, enhancing reliability and reducing losses, while reducing size, and weight. Taking these into account, the trend in Fig.1.2 is indicating that silicon based power devices continue to utilize their performance for decades. However in [3], the wide bandgap devices based on silicon carbide (SiC) and gallium nitride (GaN) could operate at high frequency and high temperature having much smaller size for the same relative voltage and current handling capability compared with silicon (Si) device.

Table 1.1 power semiconductor device capabilities comparison

Device	**Power capability**	**Switching frequency**
Thyristor	High	Slow
GTO /IGCT	High	Slow
BJT	Medium	Medium
IGBT	Medium	Medium
MOSFET	Low	Fast

The increased development of such technology with advanced features has strongly covered a variety of new products and has driven the power electronics technology towards the high power density design and integration. However, these trends inevitably lead to an increase in power and heat flux densities generated by the active devices. As from the development in power capability of semiconductor devices illustrated in Fig.1.3 [4], the chip power density was typically about 40 W/cm² in the early 2000's, and now frequently reaches > 150 W/cm2.

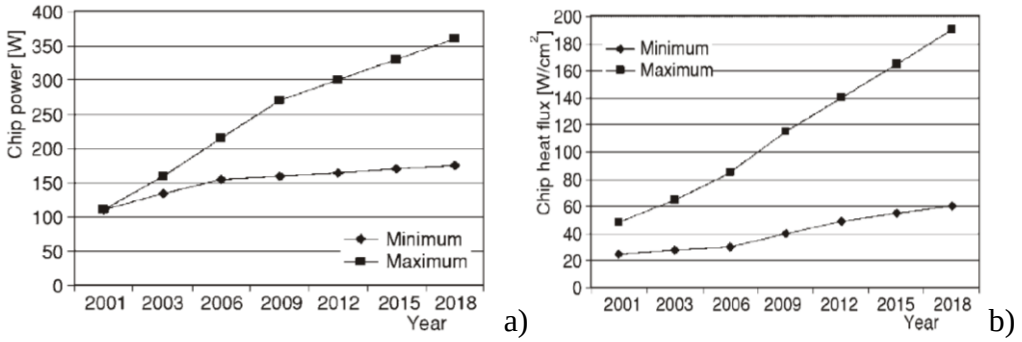


Fig.1.3 Trend to power capability of semiconductor device; power, a) and heat flux, b)

These high levels of heat flux density raise concerns about the thermal management of the power converters, which is critical to their reliability and lifetime. A rough estimate has been indicated in [4] that high temperature is responsible for about 55% of the failures occurring in electronic components, while 6%, 19%, and 20% of these failures originate from dust, humidity, and vibration, respectively.

Eventually, such result will keep pushing the limits of existing control, packaging and thermal management technology. This means that in a given power system, the enhancement of the switching performance of semiconductor devices, makes the controlling and reducing of losses in the power module become drastically important. For this reason, power conversion

technology will more urgently demand the solutions to the challenges of reducing the packaging parasitic inductance as well as efficient dissipation of heat and better structural design.

A power electronic module is a multi-layered structure with different materials in intimate contact with each other. The detailed description is fully discussed in Chapter 2. The heat removal ability of the package is limited by the total thermal impedance involved in the packaging structure. The cooling procedure of the device must be carefully analysed to minimize the thermal resistance of the module, taking into account that the materials involved have different electrical and thermo-mechanical properties. The electrical circuit behaviour of power semiconductor devices is greatly dependent on packaging design. A good packaging assembly should provide not only electrical isolation from semiconductor devices to the supporting baseplate but also better thermal performance to limit the rise in junction temperature.

Hence, electrical and thermal interaction has become so great in this case that no longer will there be a separation between both design functions. The development of power electronic packaging depends on the development of power device integration and the corresponding interconnections which its operation involves a multitude of interactions, such as electric, magnetic, mechanical and thermal. Therefore, it is clear that the design of a power electronic circuit must not to be considered solely as an electrical design.

Generally power electronic packaging technology involves integrating of power semiconductor devices, power integrated circuits, sensors and protection circuits for the wide range of power electronics applications, such as inverters

for motor drives and converters for power processing equipment. Such technology has been developed gradually over the last two decades, with incremental improvements in performance and reliability. However, the requirements for lower cost, small size, light weight and more reliable power modules couldn't stop. For this reason, integration in power electronics is getting rather complex and challenging due to some technical hitches of materials and processing methods used in fabrication, high electrical density levels and insulation requirements [5].

In order to preserve the reliability of the power devices, it is of critical importance to keep their temperature below their maximum operating temperature, which is a junction temperature typically located between 125°C and 175°C for a silicon chip. Above this temperature, the chip might become unstable and eventually fail [6]. Moreover, it is important to limit the evolution of thermo-mechanical stresses and strain induced by mismatches of coefficient of thermal expansion (CTE) between neighbouring layered materials due to the temperature change created inside the power module.

1.2. Motivation and objectives of the project

The high switching frequency and high current generates electromagnetic fields that affect the other components in the power system, creating considerable electrical interference [7]. Such interference is called electromagnetic interference (EMI) which is one of the most challenging problems in power electronics circuits. In order to minimise EMI, components must be carefully placed and contained by shielding so that EMI will have a minimal effect on the rest of the system.

This means that all paths and electrical interconnections must be kept as close as possible to further reduce the circulating loop for the parasitic components and integrate the paths in a fashion where the generated fields will cancel out one another. Fig.1.4 is the current power module where its construction is going to be discussed in the next chapter. In simple term, power semiconductor devices in such modules still use long and thin wires for electrical interconnections. Parasitic inductances associated with this long wire interconnection technology combined with short switching times severely limit the electrical performance of the device and whole converter. This inductance combined with large di/dt values causes voltage overshoot across switching devices *(due to the voltage created by the parasitic inductance, V=L*di/dt),* electromagnetic interference (EMI) and switching energy loss. Wire bonds are also prone to detaching from the semiconductor chip due to electrical and thermal fatigue (Coefficient of thermal expansion, CTE, mismatches) which significantly affects converter reliability.

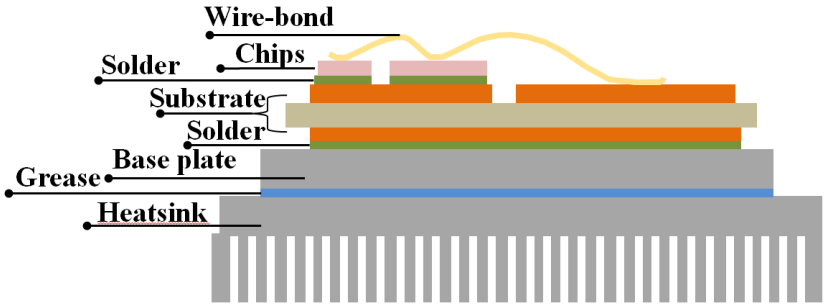


Fig.1.4 power module construction layout; wire bond interconnect

Greater attention is also being placed on thermal management's role in the module's packaging design and interconnection due to miniaturization and power increase. Fig.1.4 shows the current standard power module construction configuration consisting of power devices along with electrical and thermal interconnection layout. With the current technology for power module, almost

all of the heat has to be extracted through the solder layer that connects the chips to the substrate as illustrated in Fig.1.4 due to higher thermal resistances of the wire bonds as compared to the solder layer attached to the chip and substrate.

In searching for solutions to overcome these limitations, new and emerging technologies are introduced. Unlike wire bonds interconnection depicted in Fig.1.4, the development of power bump technology allows for innovative interconnection by stacking the power devices one on top of the other. The interconnection between the chip and substrate in power bump technology is made through a conductive power bump that is placed directly on the chip surface. The bumped chip is then flipped over and placed face down, with the bumps connecting to either the substrate directly or onto another chip. By doing so, the electrical performance can be greatly improved with the intimate contact of the interconnections. However, the closeness of the heat generating chips still causes hotspots within the power module. Therefore, removal of generated heat from the chip within the module is an important factor to the effort of establishing long-term reliability for a given power device. Currently, a power module with double sided cooling system is not commercially available in the existing market.

Advanced design and construction is nothing but impractical, if it cannot be manufactured. Therefore, in plain terms, the design has to be checked if it can be manufactured cost effectively with the existing materials and technology. As from previous experience, the proposed design can be constructed easily

with less manufacturing steps and materials usage as compared to the traditional wire-bond power module.

To ensure the reliability of the power module, this research deals with the concept, design and implementation of highly integrated bi-directional switch based matrix converter. In particular, a structural numerical characterisation of the selected bi-directional switch model in terms of thermo-mechanical and electromagnetic behaviour including constructing the module and experimental verification. The main original contributions are listed as follows:

- A novel approach to the design and interconnections of bi-directional switch that provides reduction of parasitic inductance and space exploitation.
- Considerable reduction of the thermal resistance by reducing the number of interfaces and constituent materials due to the design arrangement and construction based on theoretical interpretation. Converter with double-sided cooling capability and high power density figure as compared to conventional power modules.
- The proof of concept experimental demonstration of a prototype. In addition, this study identifies that the copper-molybdenum-copper or copper-tungsten-copper, CMC/CWC composite brick bumps can more effectively reduce the extent of mismatch of coefficient of thermal expansions (CTEs) between the bumps, Si chips and DBC substrates.

1.3. Thesis outline

Chapter 2 discusses the detail construction of conventional IGBT power modules. The section also clearly states the interconnection materials and devices used to construct a complete power module together with the interconnection methods such as wire bonding, surface die attachment, and encapsulation.

Chapter 3 presents the state-of-the-art of electronic power module technology in general and the current practice related to the electrical, thermal, and electromagnetic performance. The theory behind the insulation and reliability of power converter are also discussed in this chapter. Finally the chapter illustrates the advanced power module and its advantages by discussing different types of power packaging technologies.

Chapter 4 discusses about the power devices used in power module construction and their application using circuit assembly showing the detail circuit description and the switching operation of the selected prototype. The power losses and cooling capability of selected power devices and circuits are also discussed in the chapter.

Chapter 5 is the main body of the work and explains the detail design characterisation of bi-directional switch constructed with a flip chip technology in particular. The details include characterising the selected interconnection materials with thermo-mechanical, electro-magnetic performance and reliability. It also presents the development of the power module and a detailed manufacturing process along with the design of the water cooling system.

Chapter 6 introduces the general setup of the experimental procedure and its external circuit configurations such as power and gate drive circuit PCB board. The experimental results are also presented in this chapter.

Chapter 7 finalises and concludes the project by presenting some recommendations and assumptions that have been taken through the course of the project. The contributions and other related work have also been stated in this chapter.

Chapter 2:
Standard Power Module Construction

This chapter focuses on the detailed construction of the traditional wire bond power module. Packaging of power semiconductor devices refers to the assembly of one or several discrete chips providing electrical interconnection and as well as with external circuit thermal paths for removing heat from the chip, mechanical support and protection from external environmental factors such as dust and humidity. The detailed construction of the power module is summarised below and depicted in Fig.2.1 which lists the basic flow of the manufacturing process.

The standard power electronics modules are constructed with multi-layer structure consisting of different materials able to provide electrical interconnection, good thermal conduction, and mechanical support. The representative construction flow chart shown in Fig.2.1 illustrates the details of manufacturing process with the chronological order starting from interconnection layout, device and material selection to the final manufacturing stage called insulation.

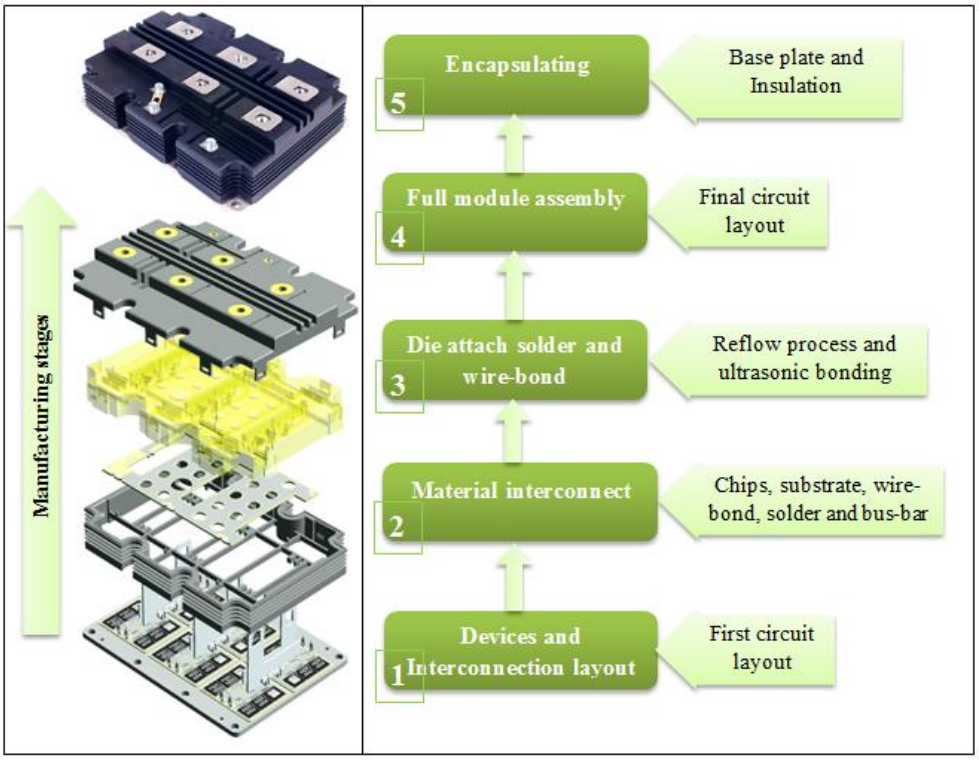


Fig.2.1 flow chart of the basic construction of a power module

2.1. Interconnection layout and power devices

The combination of a controllable switch with anti-parallel freewheeling diode as depicted in Fig.2.2 is the basic building block of a board variety of power converter topologies feeding an inductive load. As indicated in Fig.2.2, the collector and emitter (C and E) terminals of the Insulated gate bipolar transistor (IGBT) are connected with the cathode and anode (K and A) of the diode, respectively; the gate terminal (G) is used to control the active switch status, or ON/OFF.

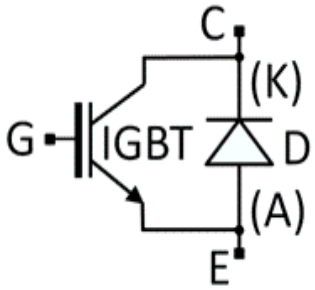


Fig.2.2 Circuit schematic of IGBT and anti-parallel freewheeling diode

In order to carry out a general description of traditional bond-wire power electronics packaging approach though-out this chapter, a reference is made to a specific type of components such as IGBTs and P-i-N power diodes which are the most wide spread power devices covering a broad range of application requirements.

Table 2.1 Comparative performance of NPT and PT IGBT [8]

Feature	NPT	PT
Cost Effectiveness	Less expensive process	More expensive
Paralleling	Simple paralleling	Care needs to be taken for paralleling
Turn off loss	Less temperature sensitive	More temperature sensitive
Thermal stability	More stable	Less stable

Mainly two types of IGBT devices and P-i-N diode for freewheeling are used to construct the power module. These IGBTs are punch through (PT) and Non-Punch through (NPT) type devices. From the general comparison stated in Table 2.1, NPT type IGBTs is more preferable than PT type due to the advantages over the temperature, cost, device paralleling and it is known to be widely used in making the power modules [9]. The PT IGBTs cannot be easily paralleled for two main reasons that inhibit current sharing. Firstly, due to the on-state current unbalance caused by V_{ce_sat}. Secondly, due to the current unbalance at turn-on and turn-off period caused by the switching time difference of the parallel connected devices. PT IGBTs are less stable due to the occurrence of thermal runaway at a lower junction temperature. They are

more sensitive to temperature variation than NPT due to low lifetime, thin drift region and large number of minority carrier.

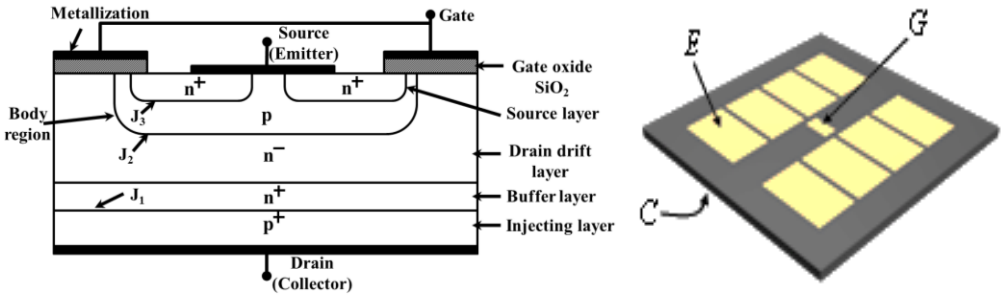


Fig.2.3 Vertical cross section and 3D structure of IGBT (C, G, and E indicate collector, gate and emitter respectively).

The structural view is a very important factor in the discussion of interconnection technology in terms of the limitation on size, track width, length, spacing and so on. Different manufacturers use different design layout. Fig.2.3 and 2.4 show 3D structural views of PT-IGBT and diode respectively along with their vertical cross section view. The n^+ buffer layer between the p^+ drain contact and the n^- drift layer in the IGBT structural view is not essential for the operation of the IGBT. IGBTs with buffer layer termed as PT whereas without buffer layer are termed as NPT IGBTs. In its operation, when a positive voltage applied across emitter to gate terminals is reached at or above threshold voltage, enough electrons are drawn towards the gate to form a conductive channel across the body region allowing current to flow from collector to emitter.

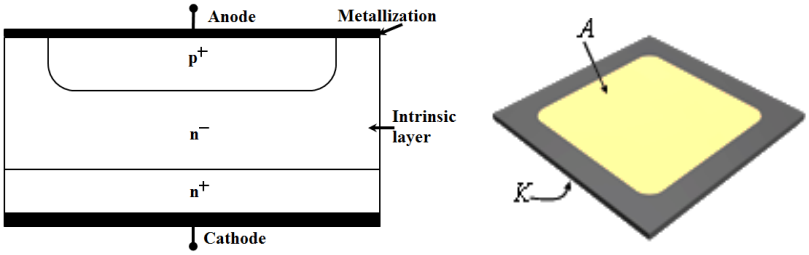


Fig.2.4 Vertical cross section and 3D structure of P-i-N power diode (A and K indicate anode and cathode respectively).

The structural cross section of P-i-N diode shown in Fig.2.4 [1] is a silicon semiconductor device constructed with two heavily doped regions (P^+ and n^+ substrates) separated by lightly doped intrinsic material of finite area and thickness. By varying this intrinsic layer and diode area different geometrics of P-i-N diode could be constructed. The thicker intrinsic layer diode would have a higher breakdown voltage and on the other hand, the thinner diode would have faster switching speed. P-i-N diodes are also characterised by parameter called carrier lifetime, which increases with the thickness of the intrinsic region. The main drawback of the lifetime carrier mechanism is the relatively slow response of the P-i-N diode to the switching command where switching time ranges from fractions of a microsecond to a few microseconds. A method of controlling and improving the lifetime characteristics of a P-i-N diode and switching speed is needed. A variety of techniques have been employed to control lifetime, such as gold and platinum diffusion and electron and proton irradiation [10]. Therefore, the choice of the structure and design refers to the required application.

In both cases (IGBT and diode), the device surface shown in the light-coloured areas consists of a metallisation layer onto which the interconnections need to be implemented. These vertical devices [11] are rated at 3.3KV with solderable top and bottom metallization treated with a combination of aluminium (Al), titanium (Ti), nickel (Ni), silicon (Si) and silver (Ag) available from ABB Switzerland and their detail dimensions of each device are listed in Table 2.2.

Table 2.2 Mechanical data of the devices

Parameter	IGBT	DIODE
Chip dimension	13.5mm x 13.5mm	13.6mm x 13.6mm
Chip thickness	0.514mm	0.385mm
Top metallization thickness	Al-Si = 0.004mm	Al-Si = 0.005mm
Bottom metallization thickness	Ti/Ni/Ag = 0.00106mm	Al/Ti/Ni/Ag = 0.0012mm

Aluminium metallization is the most widely used for interconnection providing low resistivity, ease of deposition, excellent adhesion to dielectrics and does not contaminate silicon. Al inter-diffuses into Si to form aluminium spikes causing shorting to substrate silicon. Adding 1% of silicon to aluminium to form (Si-Al) alloy instead of pure aluminium prevents aluminium silicon inter-diffusion causing junction spike. Die for solder attachment requires appropriate backside metallization. For Sn based solder alloys, a composite Ti/Ni/Ag metallization is common. The Ti provides adhesion to the Si, Ni is a solderable metal, and Ag prevents oxidation of the nickel [12].

2.2. Components involved in power module assembly

The manufacturing process in standard power module cover wide range of materials which can be broken down into the following sections: insulators, conductors, wires, adhesive, gap filler, and interconnect solder which all behave differently under various environmental, electrical and thermal conditions.

2.2.1. Substrates

The main purpose of the substrate is to interconnect the electrical circuit through the top copper layer and perform a good thermal conductivity via ceramic layer while providing high voltage isolation. Three types of substrates

are commonly employed for power modules such as aluminium oxide (Al_2O_3), aluminium nitride (AlN), and silicon nitride (Si_3N_4) substrates. These substrates are coated with copper layer by one of the following methods: copper thick film technology using screen printing, copper on ceramic by electro-less plating, direct copper bonding through eutectic oxide bonding, and active metal braising. Fig.2.5 (a) shows the photographs of top and bottom side of a DBC substrate. In such structure copper layer provides the ability to carry high current and ceramic tile provides high voltage insulation.

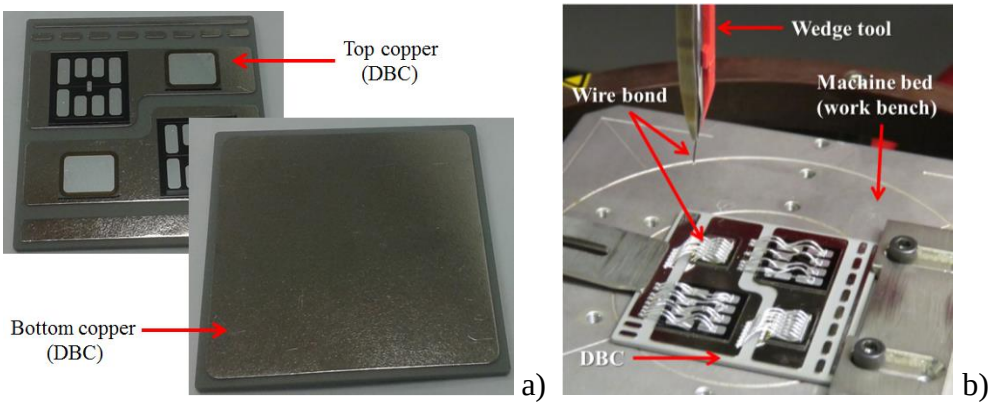


Fig.2.5 Direct bonded copper substrate; a) two IGBTs and two diodes backside soldered on a substrate and interconnected using ultrasonic wire bond, b)

As from mechanical properties listed in Table 2.3, AlN has the highest thermal conductivity which makes it better of removing heat from the device attached to it. However, Si_3N_4 takes the priority to be selected when it comes to the thermal expansion and fracture toughness. This is because the CTE of Si_3N_4 is closer to the silicon (*where CTE of Si = 3 ppm/^0C*) and it has high resistance to brittle fracture during thermal cycle.

Table 2.3 Properties of materials of ceramic substrates

Properties	**Al_2O_3**	**AlN**	**Si_3N_4**
Thermal conductivity (W/mK)	35	174	50
Fracture toughness (MPa.$m^{1/2}$)	3.3	2.7	6
CTE (ppm/^{0}C)	8.4	4.5	3.3
Young modulus(MPa)	375	330	310
Cost	Low	Medium	High

2.2.2. Solder paste

Solder paste is a form of alloy or unalloyed metal paste used to solder two close fitting parts creating a soldered joint when heated in a certain temperature profile. Standard solder paste includes tin, lead, silver, lead-free, copper or nickel is used to perform soldering. A eutectic tin-lead solder is commonly used in most surface mount soldering process, however, such alloys which contain lead have been banned due to worldwide health and safety regulations. Therefore, tin-silver (Sn-3.5Ag) is a preferable solder in a flux-less reflow soldering process [13].

2.2.3. Wire bond

Wire bonding is a process in which wires are connected onto a chip and substrate using very fine diameter wire as shown in Fig.2.5 (b). Such wires are usually made of aluminium, copper, silver or gold and have good electrical characteristics. As from Table 2.4, copper and gold have better thermal conductivity with lower electrical conductivity. Such value will result in quick and partial heat conduction along the wire providing good current carrying capability for a given wire diameter.

Table 2.4 Properties of materials for making wire bonds

Properties	Copper	Aluminium	Gold
Thermal conductivity (W/mK)	398	237	317
Electrical Conductivity (10^{-8} Ωm @ 20^0C)	1.7	2.7	2.2
CTE (ppm/^{0}C)	16.5	23.5	14.2
Melting point (^{0}C)	1083	660	1063
Cost	Medium	Low	High

The interaction between the wire bond and the device top surface is of course related to the device metallisation layer construction which commonly treated with Al, copper (Cu) or gold (Au). If the device metallisation layer is treated with copper for instance, copper wire shows better reliability due to its mechanical properties of having less thermal expansion, better electrical conductivity and an alternative technology with better cost saving compared with gold wire bonding that is commonly used in integrated circuits.

2.2.4. Bus bar

Bus bars are electrically conducting materials usually made of copper and used to obtain the desired degree of interconnection in power module construction. These bars are properly designed such that the desired internal interconnections are extracted for external circuit and be able to achieve the lowest possible module inductance.

2.2.5. Base plate

Base plates are heat conductive material typically made of Copper, Aluminium Silicon carbide or Copper composite materials serves as mechanical support. They also provide an effective thermal pathway to the cooling system (e.g. heat sink or cold plate) by conducting or spreading the heat while electrically isolated from all internal heat generating devices.

2.2.6. Silicone gel, adhesive and thermal grease

Silicone gel with a combination of hard epoxy is widely used. Silicone gel protects the circuit interconnection from environmental contamination. In the silicone and epoxy filled power module, the epoxy adhesive is used for holding the terminals tightly providing efficient heat transmission with high voltage isolation capability. Thermal greases are used to enhance heat transfer across the interfaces where the highly lubricating base oil used in some types effectively fills the microscopic air gaps between coupling surfaces.

2.3. Die attach soldering and wire-bonding

As far as interconnection is concerned, the same or analogous structure can be found with small differences at either the gate or emitter pads depending on the manufacturer, but relatively independent of the voltage class and of the particular technology (e.g., punch-through vs. non-punch-through IGBTs). For a given current rating, implementation of an elementary switch in standard bond-wire technology results in the assembly of Fig.2.6. The components are soldered backside, which is, collector and cathode terminals of the IGBT and diode, respectively, onto a proper landing area of metallization layer [14]. This metallization layer is soldered on top of a ceramic substrate using flux-less solder in between, which provides the thermal interface towards a mounting and cooling support.

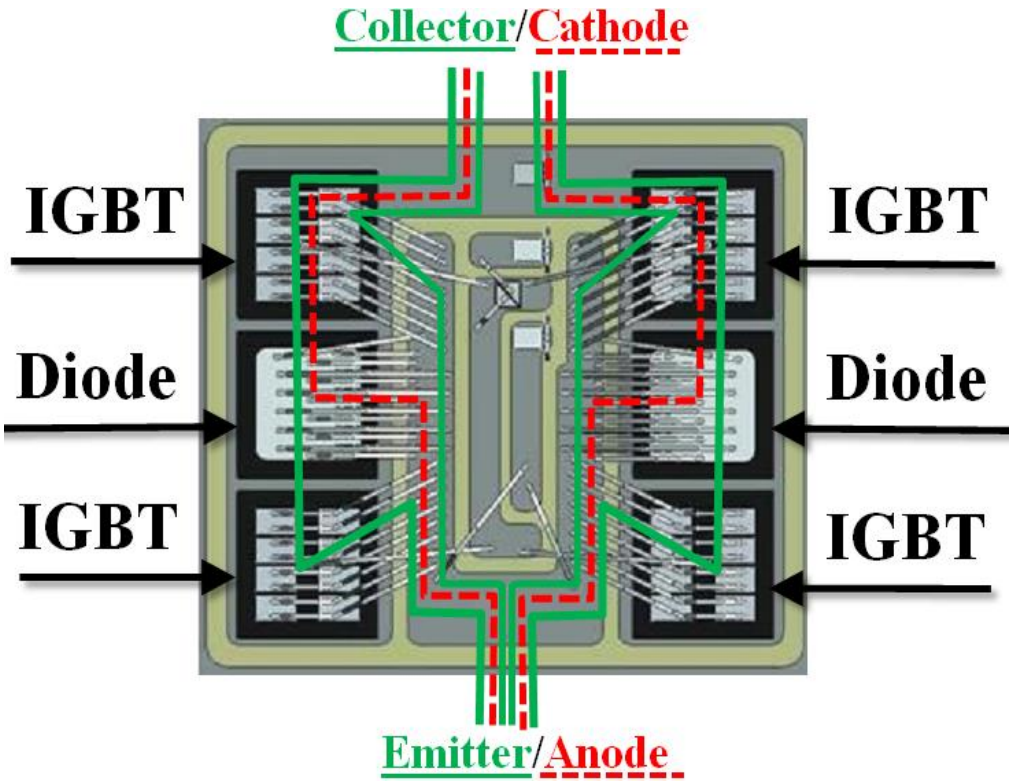


Fig.2.6 Top-view of bond-wire technology IGBT-Diode DBC substrate.

After the solder attachment is finished, the interconnection inside the module will be done using wire bonding. An ultrasonic bonding machine and aluminium wires are involved in this process. During bonding, the wedge presses the wire against the metal termination pad, and ultrasonic energy is applied to the wedge and creates an interconnection between chip to chip or chip to substrate on a properly patterned metallization layer. To increase the current carrying capacity, the wires are paralleled several fold. Wire diameter used in this process is ranging from 150-500µm. As from the current path shown in Fig.2.6, the bold green lines are referring to the IGBTs interconnection paths which start from collector down to emitter leg. The red dotted lines are for the diode interconnection paths start from cathode to anode. The figure also shows asymmetry of current paths.

2.4. Full module assembly

Connecting several IGBTs and diodes in parallel is a common feature in power module construction and results in a possibility of current de-rating that needs to be applied due to the different power dissipation levels that the components experience. In most cases, a given number of elementary switches are connected in parallel to form a power module with desired current ratings. However it is a technical challenge task to ensure proper current sharing between the parallel connected devices due to differences in device parameters (e.g. V_{cesat} and V_{th}) which are technology dependent. An example is given in Fig.2.7 a) that includes a total of 6 DBCs (the power module is rated at 3.3kV-1200A and its dimensions are 19cm x 14cm x 3.8 cm), mounted onto a base plate, which provides a common thermal and mechanical interface towards a cooling device.

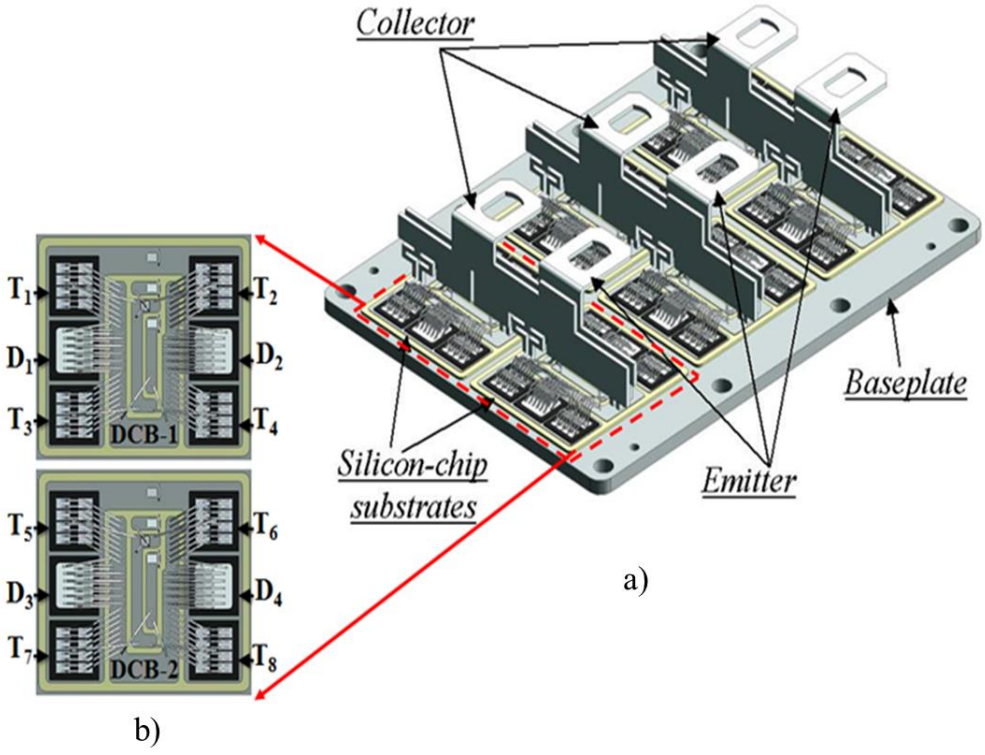


Fig.2.7 Overall view of a full module a); top view of IGBT-Diode DBC substrate, b)

The internal structure depicted in Fig.2.7 (a), contains three elementary phases according to the distribution of the emitter-anode and collector-cathode power terminals. Each elementary phase includes eight IGBTs (T_{1-8}) and four free-wheeling diodes (D_{1-4}), electrically interconnected as shown in Fig.2.7 (a) and the corresponding schematic is shown in Fig.2.8. Such devices are equally shared between two direct copper bonded substrates (DBC1 and DBC2 in Fig.2.7 (b)). The DBC substrates are soldered on a common AlSiC base plate. Metal-bars, also visible in Fig.2.7 (a) [15]. The DBCs are connected pair-wise by means of metals bars, while the interconnection between pairs must be implemented by the user. For instance, a one leg operational inverter can be implemented using two modules of the kind depicted in Fig.2.7 (a).

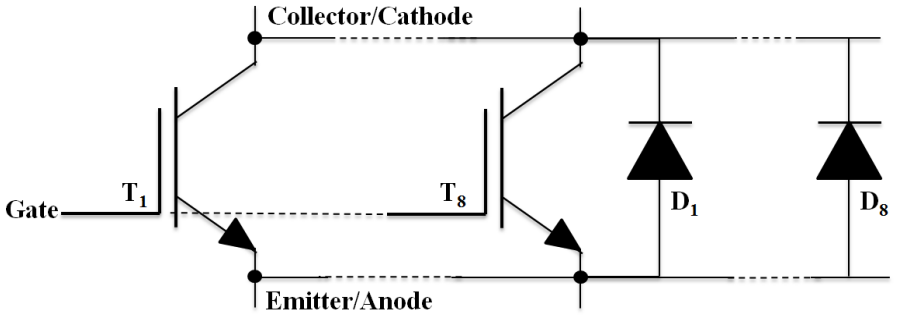


Fig.2.8 Schematic of single elementary phase

2.5. Encapsulating and cooling system

In order to maintain power electronic devices at a reasonable temperature during operation, it is necessary to implement some form of cooling method which can cope with high heat dissipation. The base plate of the power module can be used as first stage cooler. The base plate in Fig.2.7 (a) is a thick layer of metal used for mechanical support as well as spreading and conducting of heat towards the cooling system. The module is attached to this heat spreader using solder (or a thermally conductive adhesive).

Once the interconnection process is finished, a coating of a special polymer onto the heavy wire-bond and the copper bus-bars is applied to enhance the power cycling capability. The module assembly is then enclosed in a plastic housing. Afterwards, the whole assembly is immersed in a soft encapsulant, typically silicone gel, in order to provide the dielectric strength along the surfaces of the substrate, between the bus-bars and between any other parts of the module subject to high electric fields. Degassing process is done using vacuum to ensure the absence of air bubbles (void) in the entire module to decrease the partial discharge that may occur [16], [17].

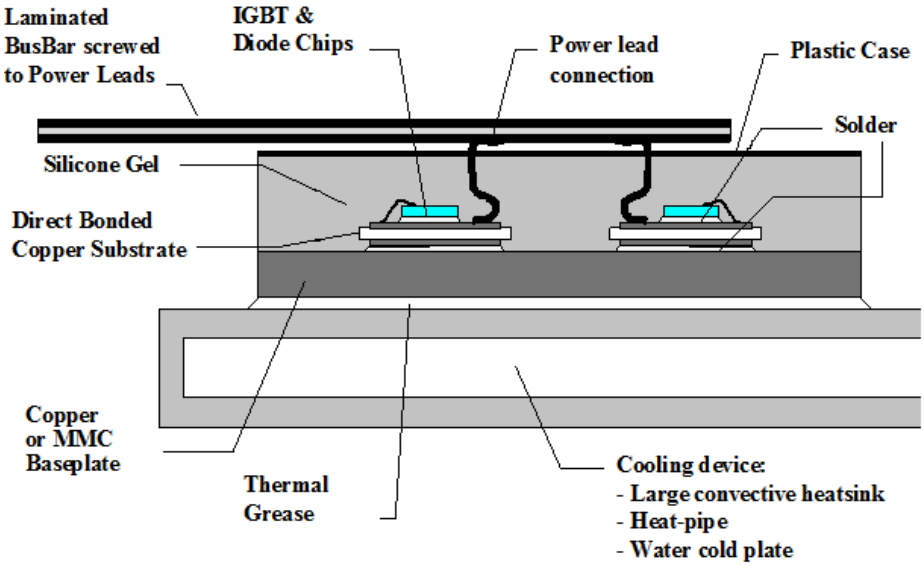


Fig.2.9 Cross section of standard power module

An epoxy layer may then added over the top of the entire dielectric system to implement extra protection from environmental factors such as moisture, dust and other contaminants as well as providing mechanical strength for the entire module. Finally, plastic mould covers are screwed or glued to cover the surface. Fig.2.9 shows the cross-sectional view of the finished IGBT power module which consists of the possible subassemblies mounted on a heat sink or

cooling device [18] where thermal grease is used between the IGBT power module and cooling device to avoid any air gaps that contribute to worse of the thermal transfer impedance.

2.6. Summary

A detail construction of the traditional wire-bond based power module is clearly introduced in this chapter. The process still holds the same procedure in case of industrial manufacturing and is more uniform and standardised. This allows manufacturing high volumes and special high power modules with same high quality level and experience in technology. The next chapter will focus on the design of power electronics packaging module in general in terms of thermal, mechanical, electromagnetic and electrical isolation.

Chapter 3:
Power Electronics Packaging Technology

In this chapter, the state-of-the-art of electronics power module technology is discussed. The chapter starts with the current practice of constructing power electronic packages in relation to electro-thermal, thermo-mechanical, and electromagnetic performance, along with electrical isolation and reliability of the power module. Then the discussion focuses on a historical background of power electronics packaging development.

3.1. Electromagnetic performance

When considering a power switch as an ideal switch, that means the switch can handle unlimited current and blocks unlimited voltage. The voltage drop across the switch and the leakage current through the switch are considered to be zero. This assumption helps to analyse a power circuit at low frequency however for practical considerations real power switches need to be analysed in terms of two main issues such as: power losses and EMI [7]. During switching transients, there are significant switching losses associated with dv/dt and di/dt. These phenomena depend on several issues where characteristics of power

switches, control signals, gate drives, stray parameters and operating points of the system need to be analysed.

Parasitic inductance is one of the stray parameters which are the major problem with power modules, particularly in high switching frequency applications. The parasitic inductance of device interconnection can cause an over voltage across the switching device and increase the losses. Many approaches have been investigated to reduce the parasitic inductance in power modules utilizing a complex mechanical construction. In power module, switching OFF the semiconductor devices (e.g. IGBT) results a current change which causes an over voltage spike by the change in the parasitic inductance created by the current commutation loop [1]. The wider the loop the higher is the parasitic inductance.

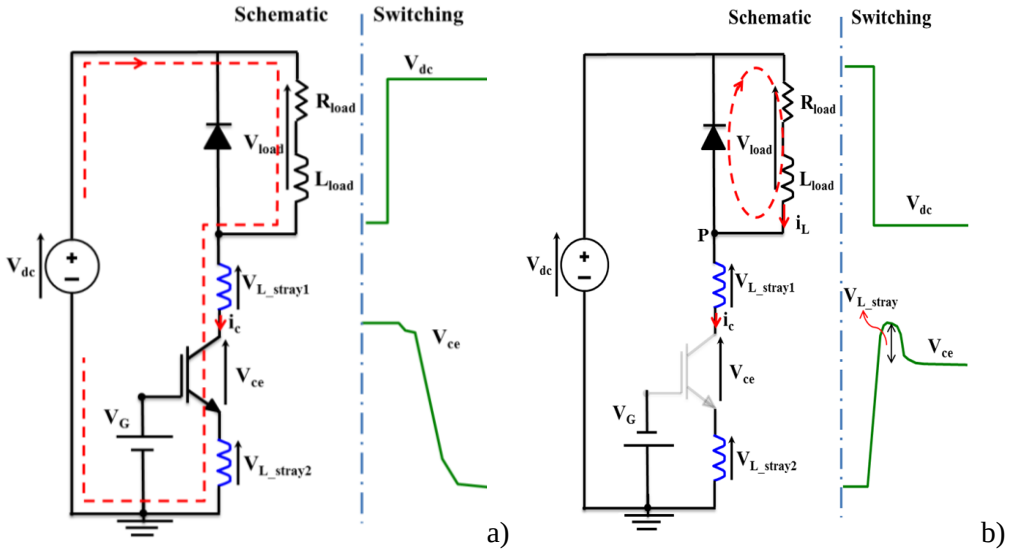


Fig.3.1 Schematic diagram of chopper circuit; a) current loop when the switch is ON; b) current loop when the switch is OFF

Parasitic inductance exists, for example, from the IGBT chip collector and emitter to their terminal connections, no matter what kind of packaging technique is used. The parasitic inductance stores energy whenever the current

flows through the interconnections inside the module when the IGBT is ON (Fig.3.1(a)). When it turns OFF, the energy is released directly as a voltage spike if there is no external snubber circuit in the current loop (Fig.3.1(b)). This spike is a function of total stray inductance (L_{Stray}) and di/dt rate. Reduction of stray inductances is an important factor in the design and layout of semiconductor device packages and power stages with both high switching frequency and power handling requirements.

$$V_{CE(peak)} = V_{CE} + L_{stray}\frac{dI}{dt} \quad \text{(Eq.3.1)}$$

Where, V_{CE} - collector-emitter voltage
dI/dt - rate of change of current
L_{stray}. – total stray inductance,

Referring to the common rule for an inductor, the current cannot change instantaneously. So, when the transistor is instantly turned off, there is still current flowing through the load inductor and as well as the equivalent stray inductances and it takes a while for the current to stop flowing. What will happen here is that the voltage would build up until all the stored inductive energy has been returned to the electrical energy. In case of the load inductor, the current will have a path to flow through the forward biased diode unlike for the equivalent stray inductance as depicted in Fig.3.1 (b). Conventionally, currents are flowing downward but the electrons are flowing upward. Therefore, with all negative electrons leaving from the point "P", Fig.3.1 (b), it ended up with a very high voltage spike across the transistor. If the voltage spike is high enough from the rated value of the device, then it runs the risk of destroying the device and neighbouring circuit. Therefore, minimising the equivalent parasitic inductance is an important issue to be able to increase the

lifetime of a power module. In general term the cumulative stray inductance of a power module can be classified into three categories, as follows:

- Inductance due to DBC substrate pattern;
- Inductance due to bonding wires;
- Inductance due to terminals;

The substrate inductance is the smallest among the three. The inductance in the bonding wires depends on the length. Usually, the length of wire is minimized and hence the induced inductance is not a big concern. The terminal conductors have a relatively large dimension, thus the largest inductance exists in this part as shown in Table 3.1 [19].

Table 3.1 Summary of the stray inductance of IGBT power module [19]

	Bond wire	**Emitter conductor trace**	**Collector conductor trace**	**Terminal connections**
Stray inductance (nH)	10 - 15	5 – 7	4 – 5	30 – 40

As from the discussion above, high di/dt may create significant overvoltage in power converters due to the parasitic inductance of the current commutation loop. Decreasing di/dt and dv/dt can decrease the inductive voltage and capacitive current of the stray parameters but this will create an increase to the switching time which increases the losses. Therefore, a compromise solution needs to be considered between the losses and EMI to determine the switching time. One can optimize the gate driver parameters to get an optimum solution. For example, using relatively small gate resistance enables fast switching, low switching delay times and low switching losses whereas large gate resistor enables the direct opposite scenario.

In this particular work however, an alternative solution is chosen using a better interconnection layout and configuration in order to reduce the parasitic inductance of the power module and Chapter 5 demonstrates the dramatic reduction of parasitic inductance in a particular power module.

3.2. Thermomechanical performance

To understand and optimize the operating mechanisms of power semiconductor power modules, analysing thermo-mechanical behaviour is one of the major interests in power packaging technology. In power module, the operation of a semiconductor device is sensitive to junction temperature. This means that if the junction temperature of the semiconductor device exceeds the functional limit, then the device will not be able to operate properly as expected. This depends on the amount of power dissipation and the thermal resistance between the junction and the package surface along with some unnoticeable area of pre damaged chip which results in heating up of power module. Besides, the environmental and operational loads add severe thermo-mechanical stresses on the devices. The coefficient of thermal expansion (CTE) mismatch between different layers coupled with the thermal cycling can cause weakening of the die attach solder and cracking of the silicon chip [6].

3.2.1. Thermal behaviour

Temperature is an important parameter that must be controlled in power electronics to ensure long term reliability of the power module. Heat generation occurs primarily within the volume of semiconductor pellets (active area of the device) which will in turn increase the components' temperature.

For safe functioning of these components, manufacturer specifies allowable temperature and if the component temperature exceeds these limits then the component will fail. For this reason, heat generated inside the power module must be transferred to the surface of the package and dissipated from the package to ambient by any available cooling strategies. The theory says that when there is a temperature difference between one physical body and its surroundings or another body, heat is transferred from the hot body to a cold one until a state of equilibrium is established.

The mechanisms of heat transfer depend on the media involved and are usually called modes of heat transfer. The three modes are **conduction**, **convection** and **radiation**. When a temperature gradient exists within a continuous, non-moving medium, heat is transferred through the medium via the conduction mode. When a surface is in contact with fluid, or gas, at a different temperature then the convection mode is occurred. Radiation heat transfer mode occurs when two surfaces exchange energy in the form of electromagnetic energy emitted by the surface at different temperature [20]. In general terms, the process of heat transfer in a power electronics module can be categorized into three stages;

- Transfer within the component package,
- Transfer from the package to heat spreader or heat sink, and
- Transfer from the spreader to the ambient environment.

Heat transfer theory is well established in the literature and there are many engineering problems that require the analysis of a heat transfer. Analytical solutions of heat transfer laws and governing equations can only be obtained by simplifying assumptions for the geometry, material properties and boundary

conditions. For this reason, a basic differential equation and concept of the numerical formulation of heat transfer are introduced prior to the use of 3D finite element simulation software.

3.2.1.1. Conduction

The general 3D equation of the conductive heat transfer in a continuous medium can be derived by the principle of the heat energy conservation over an arbitrary closed system as shown in Eq.3.2.

$$\vec{\nabla}.\left(k\vec{\nabla}T\right) + q = \rho C_p \frac{\partial T}{\partial t} \quad \text{(Eq.3.2)}$$

$$\vec{\nabla}^2 T - \frac{\rho C_p}{k}\frac{\partial T}{\partial t} = -\frac{1}{k}q \quad \text{(Eq.3.3)}$$

Where, q –volumetric heat generation
c_p –specific heat capacity
k –thermal conductivity of the material
ρ -density of the material

This equation can be simplified to the following two equations for one - dimensional heat flow [21] assuming the solid materials are homogeneous and isotropic with no heat generation. The thermal conductivity of the materials is also considered to be constant everywhere and not depending on location and temperature.

$$\vec{\nabla}^2 T = \frac{\rho C_p}{k}\frac{\partial T}{\partial t} \quad \text{(Eq. 3.4)}$$

$$\vec{\nabla}^2 T = 0 \quad \text{(Eq. 3.5)}$$

The right side of Eq.3.4 represents the rate of increase in internal energy inside the control volume per unit volume under transient condition. Eq.3.5 is a one dimensional Cartesian heat equation which refers to second order differential equation under steady state condition. Eq.3.5 can be rewritten so that the dT/dx could be formulated as in Eq.3.6 and inserted into Eq.3.7 of the Fourier's law

of heat conduction for one-dimensional steady state heat transfer equation in a solid structure and Cartesian coordinate form.

$\vec{\nabla}^2 T = 0$ *: integrate both sides*

$T(x) = C_1 x + C_2$ *: Boundary conditions, T(0) = T1 and T(L) = T2*

$T(x) = \frac{T_2 - T_1}{L} x + T_1$ *: solve equation T(x) and differentiate both sides*

$$\frac{dT(x)}{dx} = \frac{T_2 - T_1}{L} \qquad \text{(Eq.3.6)}$$

As from Fourier's law of heat conduction equation, the magnitude of the heat flux is directly proportional to the gradient of temperature field. However, the gradient of the temperature is negative due to the fact that the direction of the heat is in the direction of decreasing temperature.

$$\phi = \left.\frac{P}{A}\right|_x = -k_x \frac{\partial T}{\partial x} \qquad \text{(Eq.3.7)}$$

Where, P – power (the product of heat flux (ϕ) and area (A))

If the material is assumed to be an isotropic material where thermal conductivity is constant at any given point regardless of direction, the resulting heat flow is only in one direction as shown in Fig.3.2.Therefore, using the formulated dT/dx obtained by the heat equation, the governing Fourier's law of heat conduction equation in Eq.3.7 is:

$$\frac{P}{A} = -k \frac{T2 - T1}{L}, \qquad \text{(Eq. 3.8)}$$

Eq.3.7 can also be written as

$$P = \frac{T2 - T1}{\left(\frac{L}{kA}\right)} \qquad \text{(Eq. 3.9)}$$

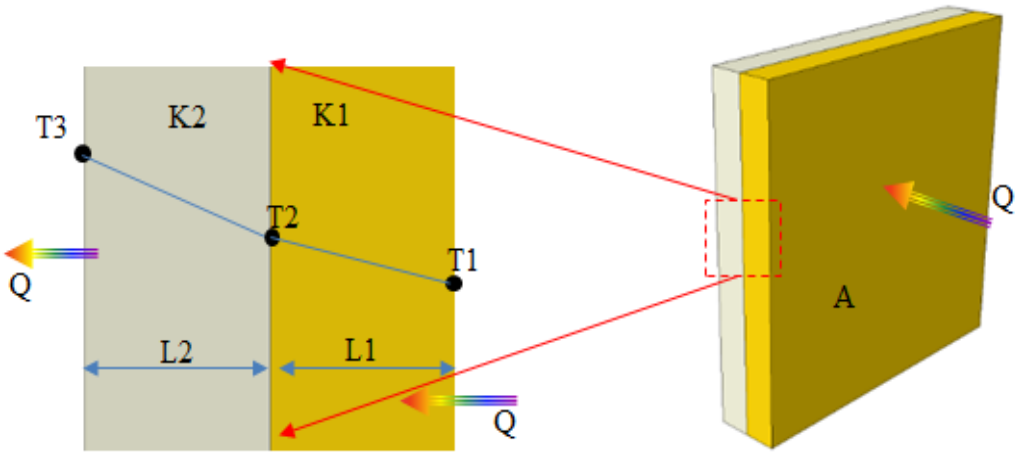


Fig.3.2 Temperature distribution for conduction across a plane

Comparing Eq.3.9 with Ohm's law for an electrical current (I), in Eq.3.10, resulting from a potential difference, V across the resistor, R shows analogous characteristic to the thermal components as depicted in Table 3.2.

$$I = \frac{V2-V1}{R} \qquad \text{(Eq. 3.10)}$$

Table 3.2 Electrical analogy of thermal components

Thermal			**Electrical**		
Variable	**Symbol**	**Unit**	**Variable**	**Symbol**	**Unit**
Power loss	P	W	**Current**	I	A
Temperature	ΔT	K	**Voltage**	U	V
Heat	q	J	**Electrical charge**	Q	As
Thermal resistance	R_{th}	K/W	**Electrical resistance**	R	Ω
Thermal capacitance	C_{th}	J/K	**Electrical capacitance**	C	F
Thermal conductivity	k	W/mK	**Electrical conductivity**	σ	1/Ωm

The thermal conductivity of a material is an important factor to the heat transfer in a given power module. The corresponding values for the materials involved in making power module are illustrated in Table 3.3.

Table 3.3 Thermal conductivity of materials used in power module

Material	Thermal conductivity (W/mK)
Aluminium	237
Aluminium nitride	174
Aluminium oxide	35
Copper	398
Gallium nitride	130
Molybdenum	138
Silicon	146
Silicon carbide	120
Silicon nitride	50
Solder (Tin - silver)	55
Tungsten	174

3.2.1.2. Convection

The transfer of energy from one region to another due to microscopic motion in a fluid added to energy transfer by conduction is heat transfer by convection. Such transfer is categorised in two different mode; forced convection where the fluid motion is caused by an external agency and natural convection where the fluid motion occurs due to density variation caused by temperature differences. Eq.3.11 is the convection process equation which is described by the Newton's law of cooling.

$$\frac{P}{A} = h(T_w - T_f) \qquad \text{(Eq. 3.11)}$$

Where, P – power
A – surface area of the heat source
h – convection heat transfer coefficient of a material
Tw – surface temperature
Tf – fluid temperature

Fig.3.3 shows the basic heat transfer by convection setup using a chip installed onto the PCB substrate where the arrows pointing outward from the chip

indicate the heat flux (power per area) and the arrows above the chip and substrate is a cooling medium (air).

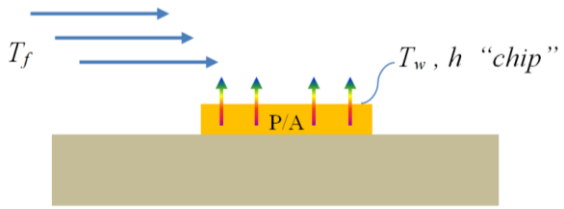


Fig.3.3 Convection heat transfer from a hot semiconductor device

Heat transfer coefficient, *h*, is a very complex and difficult number which depends on the all the variables influencing convection such as surface geometry, nature of fluid motion, properties like viscosity, thermal conductivity and density of the given material. All these influence the value of heat transfer coefficient and it is technically known as an experimentally determined parameter. Typical values of heat transfer coefficient are given in Table 3.4.

Table 3.4 Heat transfer coefficient of different cooling system

Description	**Heat transfer coefficient (W/m^2K)**
Natural convection (air)	3 – 25
Forced convection (air)	10 – 200
Forced convection (water)	50 – 10,000
Condensing steam	5,000 – 50,000
Boiling water	3,000 – 100,000

3.2.1.3. Radiation

All physical matter emits thermal radiation in the form of electromagnetic waves because of vibrational and rotational movements of the molecules and atoms which make up the matter either solid, liquid or gas. In radiation, no material medium required for energy transfer to occur and the rate of emission

increases with temperature level. The maximum possible heat emission from an ideal radiating surface is given by the Stefan-Boltzmann law.

$$\frac{P}{A} = \sigma\varepsilon(T_w^4 - T_f^4) \qquad \text{(Eq.3.12)}$$

Where, P - power
A - surface area of the heat source
T_w - surface temperature
T_f - fluid temperature
σ - Boltzmann constant ($5.6703x10^{-8}$ W/m^2k^4)
ε - emissivity of the object.

Heat transfer by radiation is potentially present everywhere. Commonly, the radiation is a major heat transfer mechanism in space application but is generally negligible in forced convection systems [20]. Moreover, among these three modes of heat transfer, conduction plays the most part within heat transfer of the power module.

3.2.1.4. Thermal impedance of power module

Heat transfer at the component level is significantly influenced by the type of package involved. This heat is usually conducted from the heat source out through the body of the part via the interconnection layers as illustrated in Fig.3.4. Since the thickness of each layer is much less than the cross section (width × length), the heat transfer is assumed to be dominantly taking place vertically downwards as shown by the arrows in Fig.3.4. The thermal path is influenced by the thermal resistance of the package which depends on the type of heat spreader, the degree of contact between layers, and the spreading of the heat inside the power module. Looking from the basic chip on board structure in Fig.3.4, the cross section of the heat source interface is chosen equal to the active area of the component (A) and the spreading angle of the heat-wave (α), is chosen to be 45 degrees with respect to the normal to the surface.

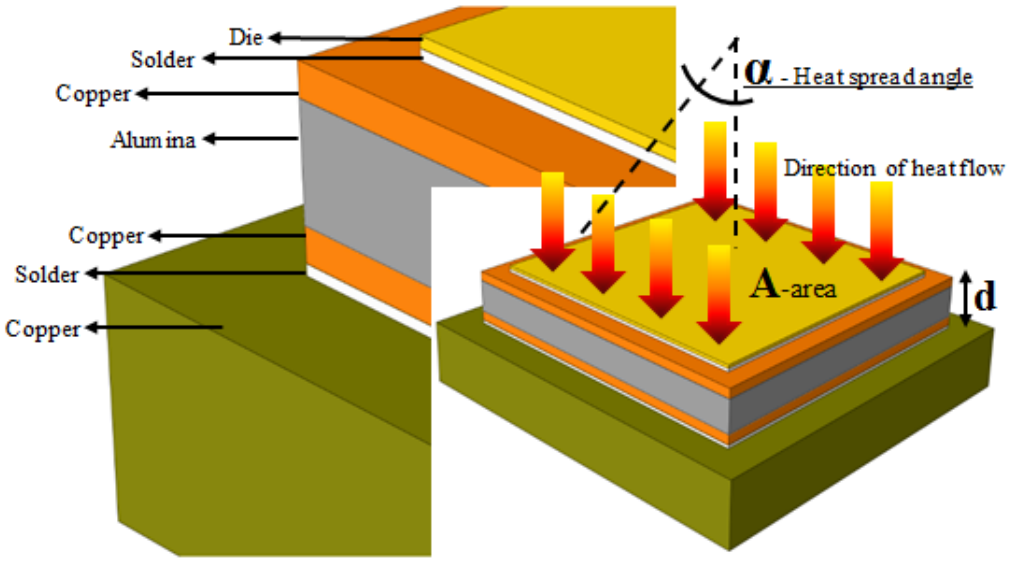


Fig.3.4 Basic chip on board layout

This is a valid approximation as long as the boundary conditions at the bottom of the device do not influence heat conduction. However, due to the very high ratio between the lateral and vertical dimension of the chips, the value of α does not affect significantly the resulting thermal model. Moreover, and as from Fig.3.5, minimum spacing of X_{min} (Eq.3.13) between the chips needs to be kept to avoid thermal cross-coupling effect when using more than one chip mounted next to each other [24].

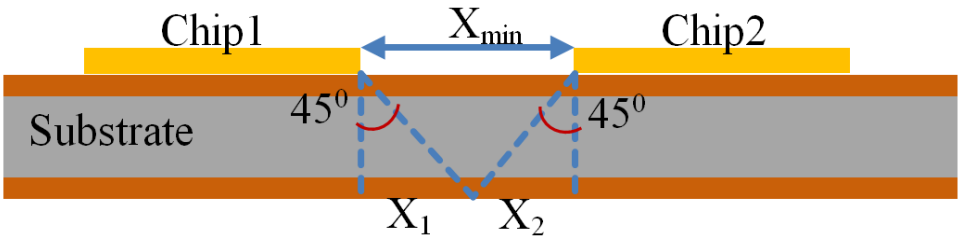


Fig.3.5 Direction of heat flow of basic chip on board layout

$$X_{min} = X_1 + X_2 = 2X_1; \text{ where } X_1 = X_2 \quad \text{(Eq.3.13)}$$

The long term reliability of power electronic devices is strongly linked to device operating temperatures and amplitude of thermal cycles that the components are subjected to. Thermal management and effective cooling of the power electronic devices is thus of critical importance when designing power

modules. Power module manufacturers have responded to this requirement by minimising the thermal resistance of the path from die to case. A common method of characterising thermal performance of packaged device is with the so called thermal resistance. In order to realise the required low thermal resistance of a power module, one has to look for the shortest heat path or avoiding unnecessary interface and combine intimate thermal contact at the surfaces with thermal interface materials which provide high thermal conductivity. Therefore, it is really important to understand the static and dynamic thermal characteristics of power modules on which IGBTs are mounted, especially regarding the junction temperature.

Static properties of a basic power module

Thermal resistance of any thermal joint at a steady state condition is directly proportional to the interface thickness and inversely proportional to the thermal conductivity of the interface material as well as to the area of the heat transfer.

$$R_{th} = \frac{d}{kA} = \frac{T2-T1}{P} \qquad \text{(Eq.3.14)}$$

Where, R_{th} *- thermal resistance*
d - thickness of the interface
A - cross-section of the die (active area)
k - thermal conductivity of the interface.

Dynamic properties of a basic power module

The thermal behaviour of a power module changes when dynamic phenomenon is considered. This behaviour can be described in terms of thermal capacity, C_{th}, which is directly proportional to the relevant volume, to the density of the material and to a proportional constant factor of the specific heat capacity as depicted in Eq.3.15.

$$C_{th} = c\rho dV \qquad \text{(Eq.3.15)}$$

Where, C_{th} - thermal capacitance
c - specific heat capacity of the material
ρ - density of the material
dV - volume.

The RC thermal networks are more popular to use for thermal analysis. They are easy to integrate into existing circuit simulator to both electrical and thermal characteristics of circuits. The RC thermal model is flexible and can be used to describe 1D, 2D and 3D problems. It can be built through the discretisation of the thermal conduction equation by either finite difference or finite element method [22]. In order to construct RC network for a given power module, it is necessary to understand the detail stacked structure in case of Cauer network or a transient temperature response curve for the Foster network.

Cauer Network

For example, each layer of the heat flow path shown in Fig.3.4 can be interpreted by two basic thermal resistances and one thermal capacitance as shown in Fig.3.6. Combining the basic thermal circuit as in Fig.3.7 results a Cauer network for the structures stacked one on top of the other as shown in Fig.3.4.

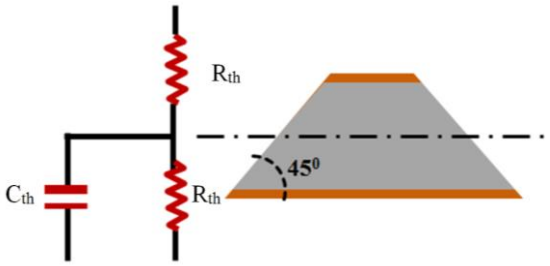


Fig.3.6 RC thermal model for a single layer

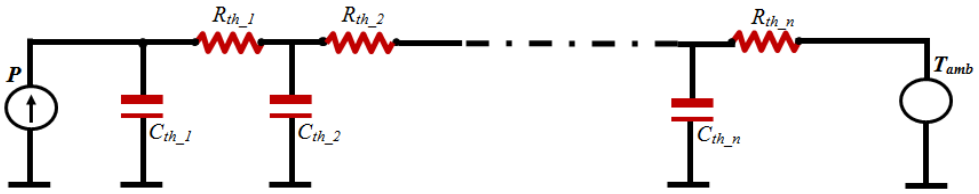


Fig.3.7 Grounded capacitor RC thermal model of a power module (Cauer Network)

Note needs to be taken that it is not a simple task to construct a Cauer network for a 3D structure. It normally requires greater computational power along with a long series of equations which need to be solved at each time step.

Cauer network derives from the fundamental heat transfer physics where every node in the network is connected to thermal ground through a capacitor. This means that there is at least a chance that experimental data from various points within the physical system can be correlated with specific individual nodes of the network model. As we go along to the heat transfer path, from junction to ambient, physical locations can be correlated with specific nodes [23].

Foster Network

The equivalent Foster network illustrated in Fig.3.8 can be used for proper calculation of the whole given thermal system. However the nodes between RC elements of the circuit do not refer to specific geometric points of the thermal system. Therefore with this network a physical interpretation of partial thermal areas within the heat flow path is not possible. The reasonable physical description of partial thermal resistances gives the equivalent Cauer network depicted as in Fig.3.7.

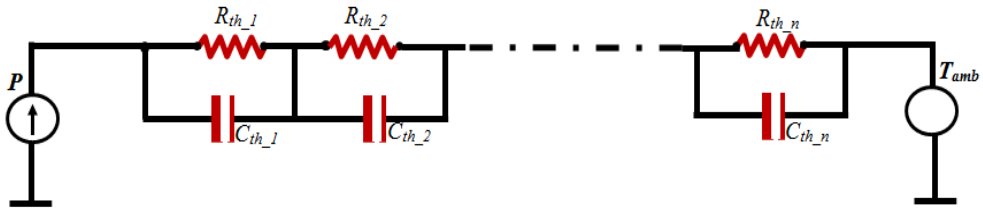


Fig.3.8 Ungrounded capacitor RC thermal model of a power module (Foster Network)

The thermal impedance from the power device junction to the ambient is determined by the particular package configuration. The junction-to-ambient thermal impedance function, $Z_{th,JA,}$ is usually described using equation (Eq.3.16), which represents the equivalent Foster network.

$$Z_{th,JA} = \frac{\Delta T(t)}{P} = \sum_{i=1}^{N} R_{thi} * \left(1 - e^{-\frac{t}{R_{thi}C_{thi}}}\right) \quad \text{(Eq.3.16)}$$

Where, P *-power loss*
$\Delta T(t)$ *-temperature gradient at a given time t.*
R_{thi} and C_{thi} *-thermal resistance and capacitance of the network.*
N *-number of RC terms in the network*

As it is mentioned above, thermal resistance of each level of a power module through the heat path contributes to the total thermal resistance limiting thermal performance of the system and affecting its life time by increasing the device junction temperature. The maximum allowable junction temperature is one of the key factors that limit the power dissipation capability of a semiconductor device which is defined by the manufacturer. The typical equation used to evaluate this temperature is shown in Eq.3.17 where ΔT is the equivalent thermal impedance multiplied by the power loss extracted from Eq.3.16.

$$T_j = T_{amb} + \Delta T$$

$$T_j = T_{amb} + \int_1^n P.Z_{th}dz \quad \text{(Eq.3.17)}$$

Where, T_j *-junction temperature*
ΔT *-temperature gradient*
T_{amb} *-ambient temperature*

The power cycling curves for the PrimePACK™ IGBT module type FF450R12ME4 tested by Infineon is shown in Fig.3.9. As evidence, the higher

the maximum junction temperature, the higher is the stress to the device which results in a reduced number of cycles [24].

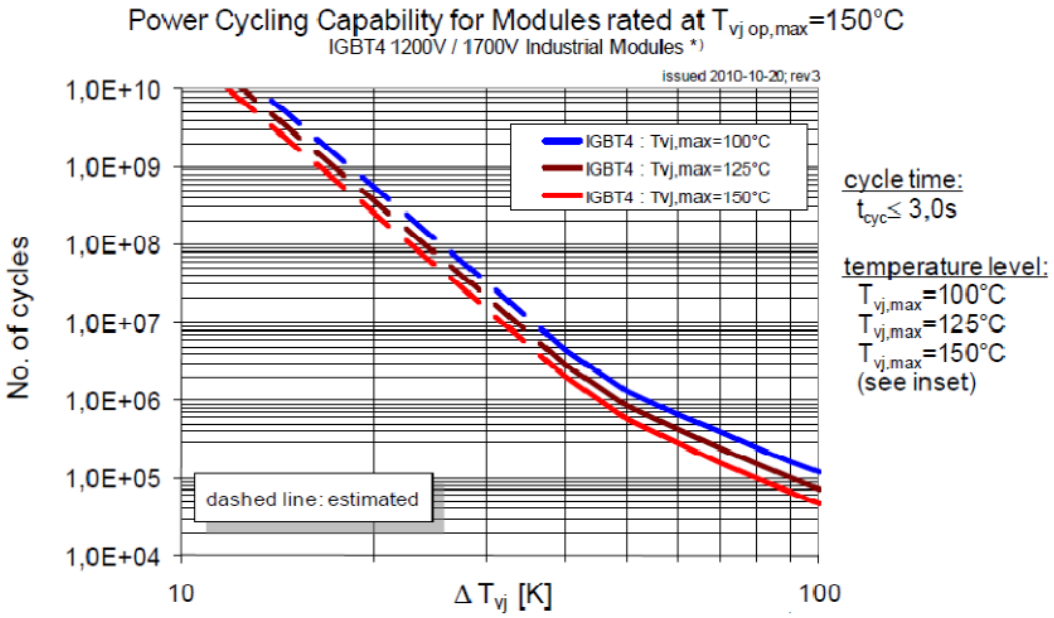


Fig.3.9 Power cycling capability for the module FF450R12ME4 [24]

Therefore, expected lifetime of the power module decreases with the increase of the junction temperature. The lifetime and the increase in junction temperature are limited mainly by the packaging technologies, like wire bonding and soldering. Hence, long term reliability consideration requires that junction temperature should be maintained at low level.

The need for more accurate and fast prediction of thermal performance of power modules in the design stage has led to an increasing demand on thermal modelling using numerical methods. Due to the complex nature of the thermal issue, commercial numerical analysis for finite element method and computational dynamics have been widely used and have shown their strength in practical thermal analysis. Numerical approaches like Finite Element Method (FEM) [25] and Finite Difference Method (FDM) [26] are useful in representing the details characterisation of the power electronics packaging

module. Abaqus, Ansys, Solidwork and Comsol are the commonly used and commercially available software. Here in this project, Abaqus 6.12-3 and its graphic user interface CAE is used.

3.2.2. Mechanical behaviour

The reliability of the power electronics modules rely on the consistencies of the interconnection and joining process utilized in their assembly. These joining technologies might not realise electrical performance requirements, but must be capable of offering strong resistance to the thermo-mechanical stresses caused by operating environments. When it comes to the high temperature and frequency operation, the CTE mismatch and the various temperature gradients within material layers are responsible of the stresses strain accumulation experienced by the materials and packaging.

There are several fundamental terms that are known as the material constraints. Starting with the definition given by Hooke's law, stress and strain are related to each other by a material constant. The stress in Eq.3.18 is directly proportional to the strain with some proportional constant, k. This proportional constant k is called the modulus of elasticity E or young's modulus and is equal to the slope of the stress-strain curve starting from origin up until point *P* as shown in Fig.3.10.

$$\sigma = k\varepsilon = E\varepsilon \qquad \text{(Eq.3.18)}$$

Where, σ - *equivalent stress,*
ε - *strain accumulation*
k - *proportionality constant (E, young modulus)*

Referring to Fig.3.10, it can be observed that the stress-strain curve starts at the lower left as a straight line. This is because the stress increases in a manner

directly proportional to the strain. The highest point attained before the line begins to curve is called the proportional limit, which is the maximum point at which extension remains proportional to load [27]. The yield strength at 0.2% offset is obtained by drawing through the point where 0.002 of strain is maintained at the same slope as the initial portion of the stress-strain curve. This 0.2% offset of yield strain is an arbitrary point which is considered by standard organization called ASTM (American Society for Testing and Materials) as an optimum value and small enough to ensure the accuracy of the yield point for most metals.

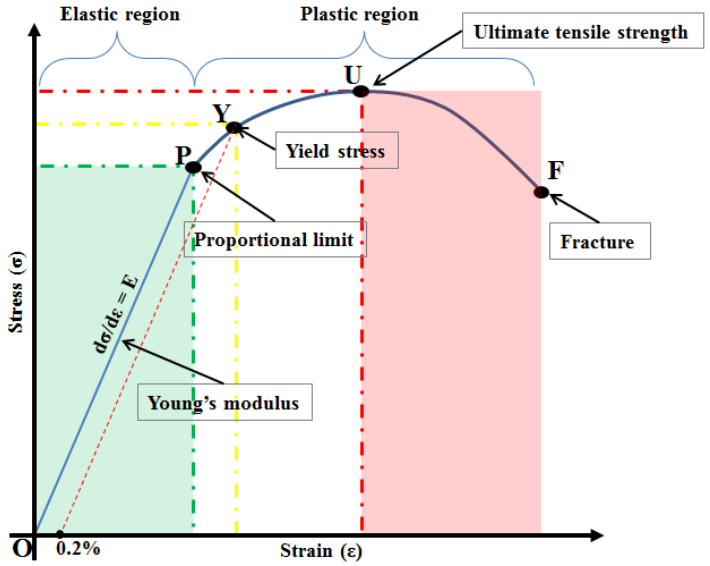


Fig.3.10 Fundamental stress - strain curve of a material

The point of intersection of the new line and stress- strain curve is known to be a yield stress of a material and is usually considered to be the failure stress. Past this point, the proportional relationship between load and extension begins to increase more rapidly than load which produces a curve and reaches to ultimate tensile strength where a fracture starts to build up. It is at this stage where the sample eventually starts to fail. This nonlinearity is usually associated with stress induced in the sample. At any point within the sample,

there are stresses acting in different directions. These stresses are called principal stresses acting in x, y, and z directions. The equivalent stress of these principal stresses is known to be Von Mises stress which is then compared to the yield stress of the material. If the Von Mises stress exceeds the yield stress, then the material is considered to be at the failure condition. Different materials and their interconnection process have different stress-strain behaviour from which the failure and reliability issues can be altered.

Table 3.5 Mechanical properties of selected materials [27][28]

Material	CTE (ppm/C)	Young's modulus (Gpa)
Aluminium	23.5	75
Aluminium nitride	4.5	330
Aluminium oxide	8.4	375
Copper	16.5	117
Gallium nitride	3.17	181
Molybdenum	4.8	317
Silicon	3	146
Silicon carbide	4	450
Silicon nitride	3.3	310
Solder	21.5	50
Tungsten	4.5	400

Table 3.5 shows the possible materials involved in power module and their mechanical properties at room temperature. Depending on thermal expansion behaviour and stiffness, different materials behave differently when exposed to heat and vibration. Materials with high modulus (stiffness) contribute low expansion coefficient. Thus, the value of CTE needs to be seriously chosen so that very high mismatch between two materials could be avoided when joining. Several reliability issues relating to material and joining processes can limit power module performance and long life.

These include creep deformation and fatigue cracking of solder joints, cracking and lift-off of wire bonds, and delaminating and cracking of substrates [29]. Both single and double sided cooled power electronics modules are constructed with number of layers having different material properties. Special efforts need to be considered to the material selection and geometrical shape of different interconnection techniques in the design for improving the thermo-mechanical reliability of a given power module.

For example, thermo-mechanical fatigue lifetimes of soft solder joints, such as Sn-3.5Ag solder joints can be described with prediction models based on plastic strain development, creep strain development and inelastic energy density per thermal cycle [30]–[32]. Such models can be implemented using FE simulation environment.

In most FE simulation, the mechanical property of the (Tin-silver) Sn3.5Ag solder joints was described by the Anand viscoplastic model, and the simulated creep strains include both the creep and plastic deformation developments in the solder joints subjected to thermal cycling. From the point of view of structural reliability, the reliability of the solder joints can be assessed with the creep strain range, accumulation and energy density. For example, the lifetime model of (Tin-silver-copper) SnAgCu solder joints based on the creep strain accumulation can be evaluated using the Coffin-Manson law equation where the higher the creep strain the shorter the lifetime of the power module is [32]:

$$N_f^{\alpha} \Delta\varepsilon_{cr} = C \qquad \text{(Eq.3.19)}$$

Where, N_f *-experimental fatigue lifetime in thermal cycles,*
α *-fatigue ductility exponent*
$\Delta\varepsilon_{cr}$ *-creep strain accumulation per thermal cycle,*
C *-fatigue ductility coefficient*

3.3. Insulation

The other feature that affects high voltage systems is the need to provide sufficient insulation between components inside the power module. Air is a relatively good insulator but its insulating properties are affected by the levels of humidity, dust and other contaminants which can lead to unnecessary parasitic components and interferences. Sufficient clearance must be allowed between components at different voltage levels so that high voltage short circuit cannot occur under worst case conditions.

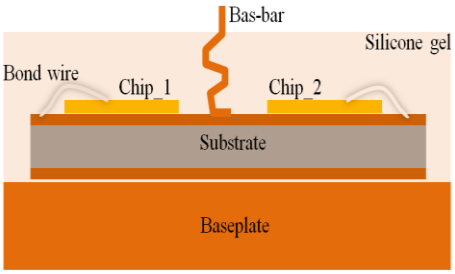


Fig.3.11 Cross-section view of a single sided power module

The internal structure illustrated in Fig.3.11 can be constructed with multiple semiconductor chips connected in parallel to achieve large-current switching. A ceramic material such as AlN, Al_2O_3, or Si_3N_4 used as substrate material based on preferable material characteristics such as thermal conductivity, CTE, and mechanical strength as depicted in Table 3.6. Finally, silicone gel is used as insulation sealing material inside fully encapsulated plastic case of the power module.

Table 3.6 Properties of insulation materials

Insulation material	Breakdown field (kV/mm)	Thermal conductivity (W/mk)	Coefficient of thermal expansion (ppm/k)
Aluminium nitride	17	174	4.5
Aluminium oxide	16.7	35	8.4
Silicon nitride	15	50	3.3
Silicone gel	16.73		

The requirement for voltage survival of dielectric strength is an average electric field of 10kV/mm, which is an extremely severe voltage from an insulation point of view. To suppress partial discharge under the presence of these higher electric fields at the edge of electrode patterns, there is a need for advanced manufacturing-process and insulation design technologies. The very appropriate solution to satisfying the above insulation characteristics is to eliminate voids in the silicone gel and in ceramic substrate, due to thermal and mechanical stresses related to power cycling [33].

3.4. Reliability

The low-cost manufacturability and rapid adaptability to different device and module designs make the wire bond technology widely used in power electronics packaging technology. However, such technique involves a number of reliability performance issues due to package-related failure modes such as solder joint degradation, wire bond lift off, wire bond heel and vertical cracking and substrate delaminating. These failures are very well-known reliability issues mainly caused by fatigue and creep process. Fatigue is a progressive structural damage due to repeated oscillating stress below the yield stress of the material whereas; creep is a time dependent deformation behaviour that occurs when a material is subjected to a constant load at high temperature [34].

3.4.1. Solder joint degradation

Within the power electronic module, solder joints serve as mechanical and electrical connection between the die and the package, therefore, their electrical stability is one of the most important reliability considerations. The repeated heating and cooling of power module cause thermo-mechanical fatigue in the

solder joint. When fracture occurs or spreads through the solder interconnection, the thermal path between the active device and the rest of the package is interrupted leading to resistance/impedance rise. This thermal resistance value is often used as a parameter to determine the remaining life time of the solder joint interconnection, also, an increased thermal resistance will shorten the life of the power module. The fracture spread through the solder joint, shown in Fig.3.12, an optical micrograph [29], was due to the course of thermal cycling forming cracks at the edge and propagating towards the centre.

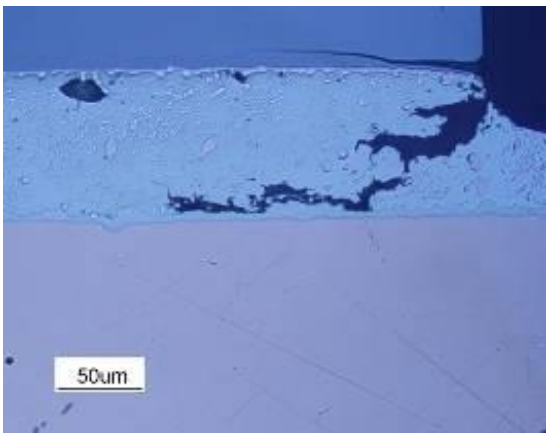
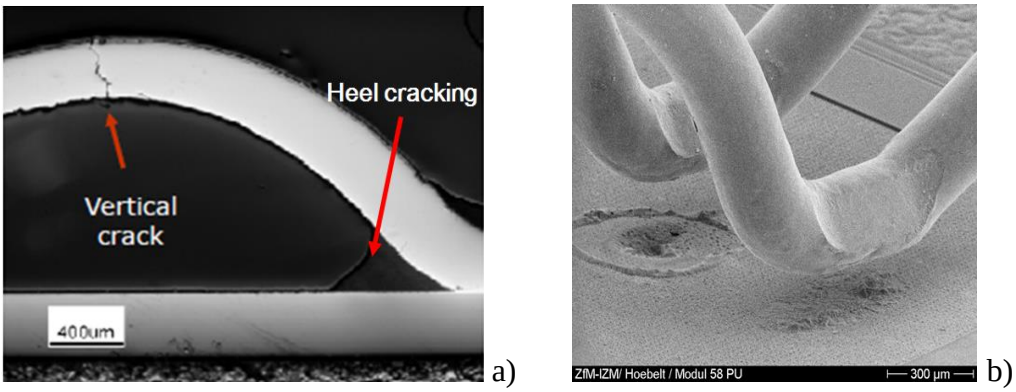


Fig.3.12 Effect of thermal cycling on crack propagation [35]

3.4.2. Wire bond lift off and bond heel cracking

The wire bond quality is controlled by a number of parameters: temperature, ultrasonic power, time, and bond quality directly influences reliability. Although wire bonding is the current technology with high production capability, it is clear that at high switching frequency, the thin and long loop of wire results significant parasitic inductance which often restricts the thermal and electrical performance of the power module. There is also a substantial mismatch in CTE between the wires and silicon device onto which they are bonded. As a result thermo-mechanical strains are generated at the bond interface and residual stress from the ultrasonic bonding adds to the build-up of

strain during thermal cycling. Such effect will either generate bond wire heel cracking, cracking across the wire loop or lift-off from the interface as shown in Fig.3.13 [36].

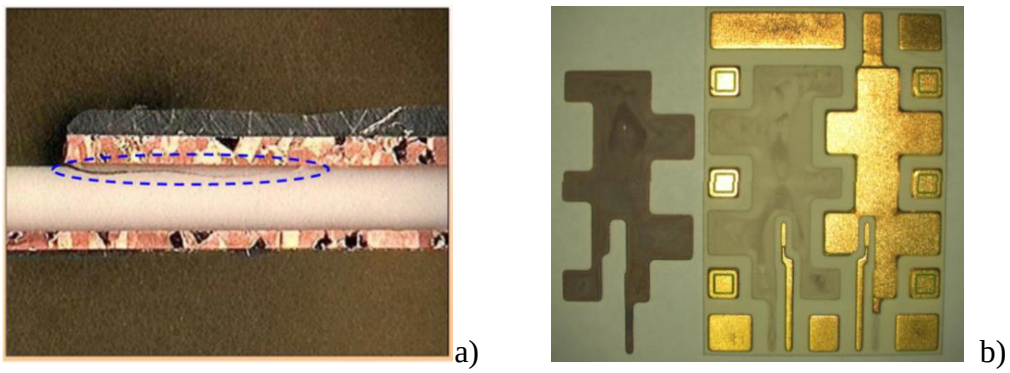


a) b)

Fig.3.13 Micrograph of wire loop and heel crack, a) and wire bond lift off, b)

3.4.3. Ceramic substrate cracking and delamination

In substrates, fracture toughness refers to a property which describes the ability of a material containing a crack to resist further fracture. CTE mismatch is the major factor in the delamination of the copper away from the ceramic and it is common in high fracture toughness ceramics. Fracture like conchoidal (see dotted lines on Fig.3.14 (a)) can also occur through the ceramic and is common in low fracture toughness ceramics. Fig.3.14(a) and (b) show the conchoidal type fracture through ceramic and delamination of copper associated with DBC and AMB ceramics [37]. All these drawbacks have major effect on the long term reliability of power module.



a) b)

Fig.3.14 Concoidal Fracture of ceramic substrate and delamination [37]

3.5. Advanced power module technology

Downsizing and system integration in power electronics are mainly driven by applications with very challenging space restrictions, such as automotive, renewable energy, aerospace, railway system, wind turbine, commercial and industrial applications. For the past twenty years, power electronic packaging technology with enhancement of high power density, high efficiency and better technology solutions aiming at very high performance were developed. Such technology involves material and power device upgrading, structural improvement and different interconnection techniques.

3.5.1. Wire and Ribbon bond interconnects

The two most accepted wire bond process are ball (wire) bonding and wedge bonding. Both of these processes use ultrasonic energy to create an intermetallic interface bond, between the wire and the die pad or the substrate. Although wire bonding is normally faster and is used in a variety of bonding applications, ribbon bonding (a form of wedge bonding) is gaining momentum in high frequency and applications [38]. Ribbon is a flexible conductive metal foil that is ultrasonically bonded to the surface of a die and terminals from a package.

Since one of the demands in the performance of power electronics is reduction of parasitic inductance, ribbon bond is often specified an interest instead of wire bonds. This is because of the larger surface area of ribbon bond as compared to the round wire. Fig.3.15 shows an aluminium ribbon bond on a chip. Ribbon bonds are preferred because a typical one has two or three times less inductance than a wire bond [39]. They also allow interconnection with a

large cross-sectional area that serves to replace multiple wires to be bonded. In comparison with bond-wire, the larger cross-section area of ribbon enables it to possess lower electrical resistance and thus carries larger current.

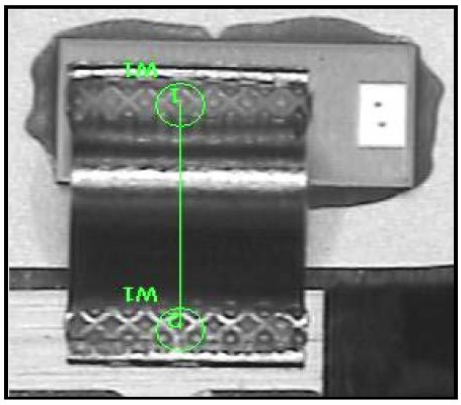


Fig.3.15 Al ribbon on a chip

However, ribbon bond simply fails in the comparison to a traditional wire bond on different levels. It is not as fast as wire bond during manufacturing as the components get smaller. Furthermore, due to their flatness, ribbon bonds lack the flexibility of bond wires have to be bent or configured in complex angular interconnection pattern [38]. The main concern focuses on the bondpad metalization on the chip. Several problem areas can converge to these three:

- Ultrasonic power and bond force increase with increasing bond crossection
- Power deivices are becoming thinner
- Damage can be invisible but causes long term failure

3.5.2. Solder bump interconnects

Avoiding the use of wire bonding process is a suitable solution to overcome the existing drawbacks and increase efficiency of the power module. Several bond wireless techniques have been explored in the industry for many years. For example, there has been an active effort in 3D packaging techniques aimed at

integration of the entire module and driver circuits in a compact stacked structure where a chip scale IGBT package is presented which uses solder joints to interconnect power chips [40]. The cross section of the package structure is illustrated in Fig.3.16. The package design and process have been optimised to gain better electrical performance and achieved higher reliability as compared to the wire bond modules.

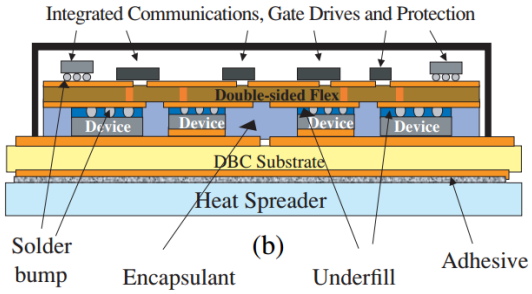


Fig.3.16 Structural view of the solder bump type power module

Whereas here in [41], dimple array interconnection (DAI) technique is presented which establishes electrical interconnections on the power devices using solder bumps formed between the device electrodes and arrays of dimples pre-formed on a metal sheets capable of carrying large current for packaging power devices. The main target of this technique focused on its dimpled metal interconnects which are convex valleys on metal sheet extended from one side to enable easy forming of joints with underlying solderable device through solder layer as shown in Fig.3.17.

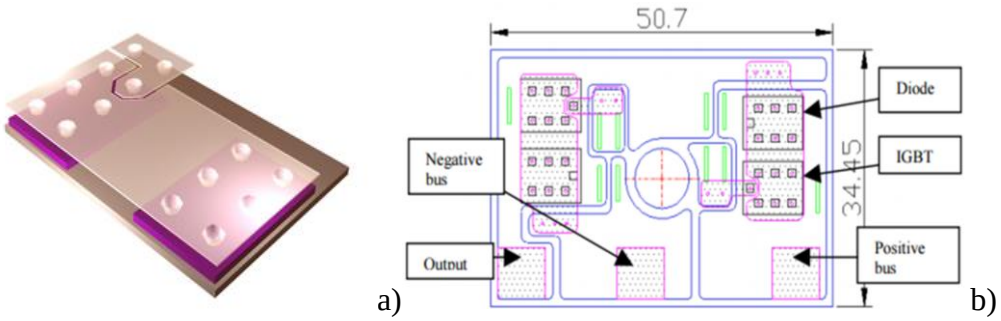


Fig.3.17 Dimple array interconnection model, a) and DAI circuit layout, b)

The benefit is its simplicity as compared to the above solder joint technique and other power packaging technology like flip chip. The DAI solder joints are also more reliable than flip chip solder joints under power cycling conditions. However, the symmetrical current commutation loop is challenging due to the copper trace on top of the silicon devices and the loop is still longer. For example, looking at the half-bridge model [42], the loop from collector (positive bus) to load (output) and emitter (negative bus) to load are not symmetrical. Such asymmetrical structure makes current sharing more difficult to predict during switching. It also requires additional tooling to fabricate and handle the dimpled copper plates. Besides, further optimisation is quite limited due to the behaviour of the technique (design) structure.

3.5.3. Metal post interconnects, stacked device and flip chip

Reliable metal posts interconnected parallel plate structure power module based on the use of direct bonding copper posts was designed and presented as depicted in Fig.3.18 [43]. Such power module approach requires less expensive equipment and has the potential to produce modules having superior electrical, thermal and mechanical performance.

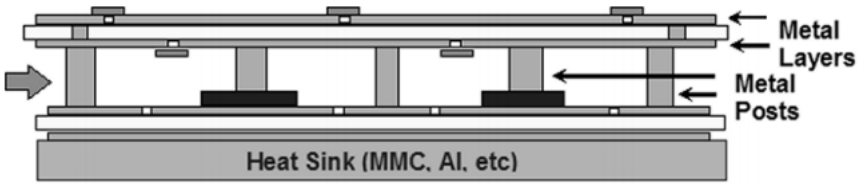


Fig.3.18 Cross section of metal post type power module structure

A thermo-mechanical modelling of the metal post interconnect did show that the post joints are susceptible to failure under thermal and power cycling conditions. Therefore, a solder or metal post with a lower CTE and high temperature creep resistance is preferred for better reliability [44]. International

rectifier researchers [45] presented samples of high current power IGBT packages with copper clip directly soldered onto top emitter electrode as shown in Fig.3.19 which can offer double sided cooling capability. The approach exhibits significant reduction of on-state voltage drop and enhanced reliability.

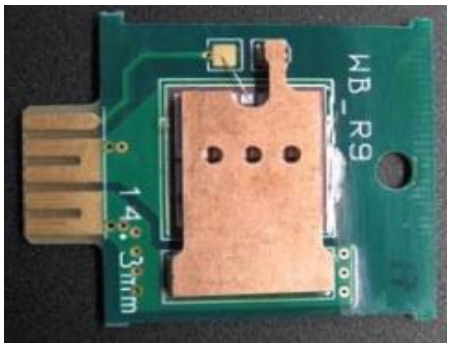


Fig.3.19 Top view of IR planar IGBT package in Cu-clip

Mitsubishi also developed a copper lead bonded Transfer-molded-Power-Module (TPM) [46]. The cross section view of the module is shown in Fig.3.20. Copper leads are soldered directly on top of all switch dies. Both IR's and Mitsubishi's interconnection components reduce the package parasitic resistance dramatically but the approach still used a wire bond interconnect for the control pad. In both cases, the modules are non-electrically isolated and a ceramic slice needs to be inserted between power module and the cooling system. This implies that thermal grease layers are needed to each ceramic insulator and will add thermal resistance to the thermal path.

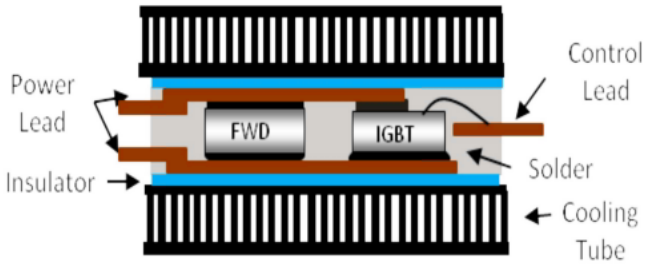


Fig.3.20 Schematic cross section view of packaging component stack

So in place of the conventional wire bond and the above listed technologies, the first interconnect approach developed in power electronics packaging uses copper posts to construct a parallel structure with double sided cooling capability in 1999 [47]. The interconnection has been demonstrated not only to obtain dramatic improvement in the thermal and electromagnetic performance but also allows advance integration scheme, such as stacked devices and flip-chip, for optimization of a basic power switch topology. However, further investigation of reliability and manufacturability of such technology is still in demand for wider acceptance and generalization. In recent years, a bond-wire-less advanced integration approach has been demonstrated for vertical power devices [48], [49].

Fig.3.21 Bump technology based elementary power module

The idea is based on the use of conductive power bumps to connect the surface of vertical power devices which deliver a reduced stray inductance, higher integration levels and double-sided cooling capability. Fig.3.21 illustrates the first generation of integrated converters which was developed by PEARL-ALSTOM based on the stated approach. As from Fig.3.21, the devices are sandwiched between two ceramic substrates with properly patterned

metallization layers where connections to the bottom substrate are made using solder joints whereas to the top substrate by conductive surface bumps.

Continuation of work initiated by [50] comes up with the idea of integrating semiconductor power module in an alternative 3D integration scheme. Compared to the first integration structure [48], one lateral dimension is kept the same, the other one is halved and the vertical is doubled as shown in Fig.3.22. Hence, for the same power density alternative space exploitation is obtained. This approach is however used extra copper layer in order to create the middle interconnection point.

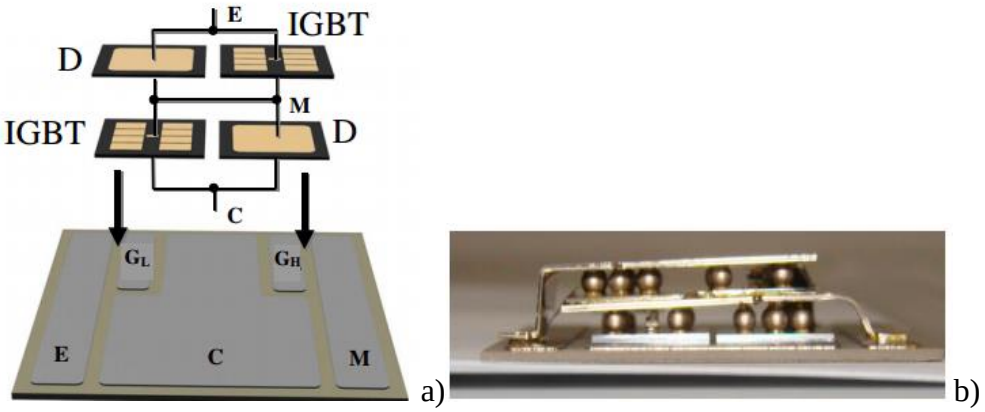


Fig.3.22 Surface bump technology approach, a) side view of the prototype, b)

Another packaging structure [51] was presented with a 200A/1200V phase leg power module for liquid cooled, Fig.3.23, sandwiching power semiconductor switches between two symmetric substrates but using die attach solder layer.

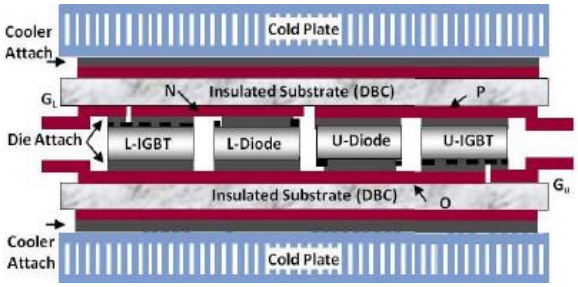


Fig. 3.23 Planar bond structure

As from the study carried out and presented in [31], the thermo-mechanical reliability of an IGBT module constructed with Cu cylinder bumps and soldering technology have been investigated and identified that the solder joints used to bond the bumps as thermo-mechanically weak points.

3.5.4. Progress beyond state-of-the-art

Traditional power modules discussed in chapter 2 are realized by bonding one or several substrates on a baseplate made of e.g. Cu or AlSiC. The modules have to be screwed on a cold-plate in which the non-bonded, mechanically detachable contact plane requires a thermal interface material for acceptable thermal properties or heat transfer. But even with the best available thermal interface materials (TIMs), this contact plane causes a considerable contribution to the total thermal resistance between chip and coolant. So, modules with a directly cooled system as in Fig.3.24 can avoid the disadvantages of a TIM layer and contribute a dramatically reduced thermal resistance.

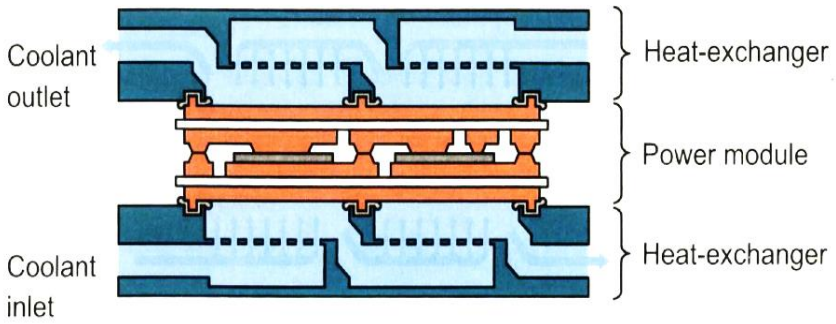


Fig.3.24 A cross-section of double side cooled power module model [52]

Cu posts on direct bond copper substrates using a double etching process were presented [52] and the posts were created to make contact on the top side of power devices for assembling a sandwich structure power module with low parasitic inductances. The approach in Fig.3.24 illustrates an integrated inverter

consists of three power modules, clamped between two heat exchangers permitting double side cooling of the embedded dies whilst controlling the mechanical stresses in the entire module.

In response to the weakness of the solder joint, a novel packaging technology (SKiN Technology) [53] presented using silver sinter joint offers a very high power density figure and demonstrates a remarkable reliability performance mainly using wide band semiconductor device (e.g. SiC). The technology uses sintered flexible foil to replace bond wires and currently is not designed for flip-chip type configuration where all chips are mounted in a planar form.

Our previous preliminary study [54]–[56] used Cu brick and Cu hollow cylinder bumps to develop highly integrated bi-directional switch and half bridge switch modules, and obtained dramatic improvements in the thermal and electromagnetic performance. A comprehensive FE modelling approach to optimize the thermo-mechanical performance of the stacked bi-directional power switch assembly is also presented in [57] .

To develop more reliable integrated power electronics modules, it is very important to consider the coupling between electrical, thermo-mechanical and electrical isolation effects along with comprehensive characterization of the materials and their interconnections.

3.6. Summary

In this chapter, the important factors in designing and constructing power electronic converters were outlined. The discussions were particularly focussed on thermal, mechanical, and electro-magnetic behaviour of power electronics

packaging in terms of reliability including the electrical insulation within the package. The main drawbacks of the traditional power module were identified; particularly the long and thin aluminium or copper wire bond based power converter design practice does not optimize thermal and electromagnetic issues. The main point of this breakdown is to show that a typical silicon based power electronic converter constructed with power bump (posts) using flip chip/stacking up technology can deliver high density figure, better performance, and dramatically reduced parasitic inductance while enabling double sided cooling capability. Currently, double side bond wireless interconnection is still on the area of preliminary research and fabrication process. In addition, when it is coming to the high frequencies and high temperature, it is quite obvious that the silicon based devices (IGBTs) are not preferable as compared to the wide band semi-conductor device like silicon carbide (SiC). Therefore, a low temperature joining technology based on sintering of silver powder has emerged in the power electronics industry for the future wide band gap power devices. However, the study show that the proposed method is transferrable and has enough potential to improve electrical, thermal and mechanical performances further by optimising the issues stated in this chapter. In Chapter 4, a theory that deals with the advance integration approaches of 3D flip chip/stacking power electronics packaging concept will be discussed along with the selection of specific case study.

Chapter 4:
Basic switch topologies of power electronic converter and device circuit interactions

This chapter focused on the selection of the power devices and application along with the interaction between the semiconductor device packaging and its cooling system. The detail switching pattern of power device and circuit operations are also presented including the power losses and cooling capability of a given power module. The chapter has also pre-informed the selected case study that would be continued in the next chapter in detail.

4.1. Device, application and switches

An ideal switch should have an infinite blocking voltage capability, very small switching times, no parasitic inductance or capacitance, and no on-state resistance. The switch should require minimal energy to change its state from ON to OFF or vice-versa. However, solid-state transistors approximate an ideal switch to a good degree up to several kHz [1]. They have enabled power switch-mode type circuits to be widely implemented for many applications. The principal requirement of a switching device used in a switch-mode type circuit is that it has fast enough switching times for operation at a desired

frequency. For several years and nowadays, modern power semiconductor devices, like MOSFETs, IGBTs, and diodes have made converters suitable in many applications due to their reduced cost, ease of control, and increased power capabilities [58], [59]. These have also opened up a host of new converter topologies for power electronics applications. Therefore, knowing the detail characteristics of available power devices is vitally important factor to understand the feasibility of any new topologies and applications. In this particular work, consideration is taken place on two semiconductor devices such as:

Diodes: ON and OFF states controlled by the power circuit

IGBTs: ON and OFF state by control signals

4.1.1. Power Diode

The power diode is perhaps the simplest switching device among all the semiconductor power devices. Its electrical circuit symbol and steady state I-V characteristic are shown in Fig.4.1. From the I-V characteristic, one notices that when the diode is forward biased, it starts to conduct and the current flows through the device with only a small forward voltage which is in the range of (0.6-1V).

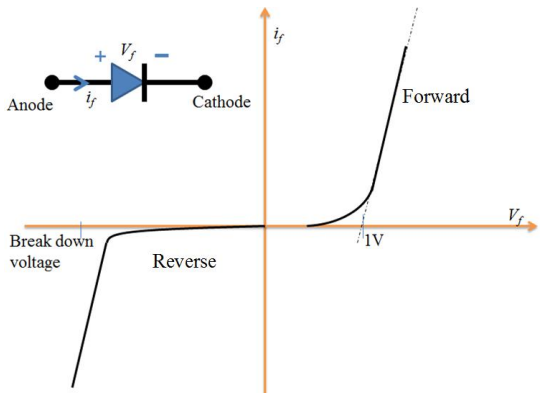


Fig.4.1. V-I characteristics of a pn-junction diode. The circuit symbol is also shown with the anode and cathode designation

When the diode is reverse biased, it doesn't conduct and a negligibly small amount of leakage current flows through the device until the reverse break down voltage is reached. Once the applied voltage is over this limit, the current will increase rapidly to a very high value. In normal operation, the reverse bias voltage should not reach the breakdown rating of the device [60]. Depending on the application requirements, various types of diodes are available in the market such as schottky diodes, fast recovery diodes, and line frequency diodes.

4.1.2. Reverse recovery of diode

The time interval, t_{rr}, shown in Fig.4.2 is often termed as reverse recovery time. It is a time required for the current to reach a specified reverse current after instantaneous switching from a specified diode forward current. In simple term, when a given circuit commutates a diode, the stored charge, Q_{rr}, which represents the area under the current-time curve during t_{rr}, must be completely extracted or neutralized before the diode is said to be OFF. The time it takes for this to happen is defined as reverse recovery time. This recovery time is composed of two distinct intervals which are the time required for the reverse current to reach its negative peak value and the time required for the negative peak value to reach zero labelled as t_1 and t_2 respectively [60].

In most power electronic circuit design, the reverse recovery current waveform shown in Fig.4.2 is an important characteristic. One of the features of particular interest in such waveform is the sharpness of the fall of the diode reverse current during diode turn off time.

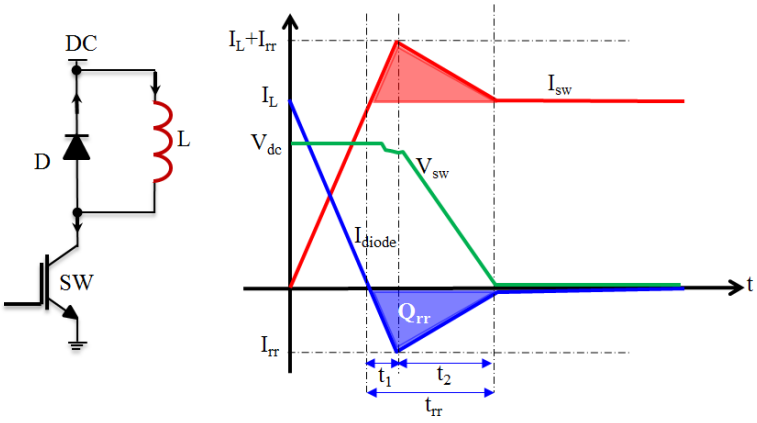


Fig.4.2 Effect of reverse recovery current on switch current

Reverse recovery in diodes introduce small losses in the diode but larger losses in the IGBT that can be seen in Fig.4.4. Such losses are influenced by the two reverse recovery parameters $\boldsymbol{I_{rr}}$ and $\boldsymbol{t_{rr}}$. Here, it should also be noted that a diode with a long reverse recovery time is similar to a diode with a large parasitic capacitance and a diode with long forward recovery time is similar to a diode with large parasitic inductance. From the packaging and system design perspective, the use of fast recovery diodes and lower turn-on resistance transistors improve switching and conduction losses [61].

4.1.3. Controllable switch

The insulated gate bipolar transistor, which was introduced in the early 1980s, has become a promising device because of its superior characteristics [62]. Typical forward I-V characteristic of an IGBT and its electrical symbol are shown in Fig.4.3. The steady state forward I-V characteristic of the IGBT consists of number of curves, each of which corresponds to a different gate-emitter voltage. Keeping the gate-emitter voltage fixed, the collector-emitter current is measured as a function of collector emitter voltage as illustrated in Fig.4.3.

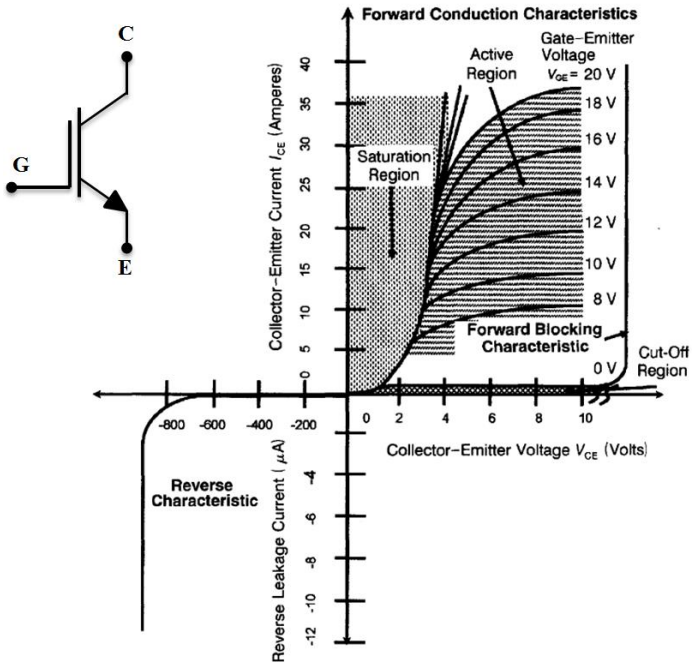


Fig.4.3 Output I-V characteristics of IGBT [62]

The IGBT is in the OFF state if the gate emitter voltage is below the threshold voltage such that no current will flow and it operates as an open circuit. But, when it is ON, current can flow in the direction of the arrow and makes the circuit closed. In general, an ideal controllable IGBT switch has four main characteristics. Firstly, it blocks arbitrarily large forward and reverse voltages with zero current flow when OFF. Secondly, it conducts arbitrarily large currents with zero voltage drop when ON. Thirdly, it switches from ON to OFF or vice versa instantaneously when triggered. Fourthly, it requires very small power from control source to trigger the switch.

The diode clamped inductive load circuit shown in Fig.4.2 is a circuit commonly encountered in power electronics. Fig.4.4 is a realistic IGBT switching waveform considering the characteristics of diode recovery and stray inductance.

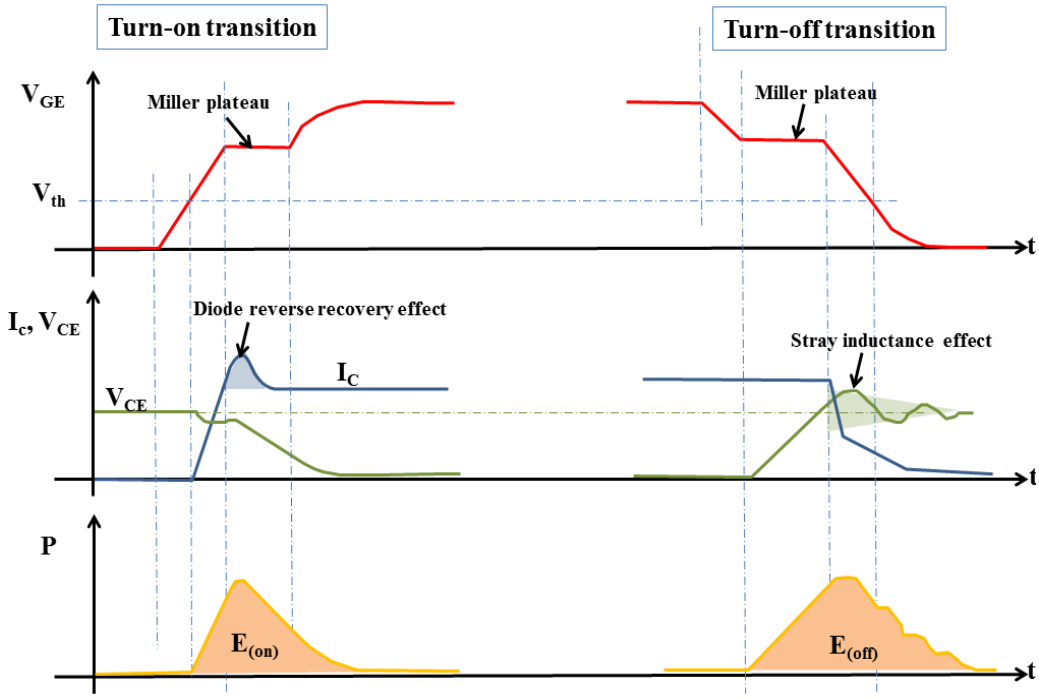


Fig.4.4 Switching behaviour of semiconductor device, in this instance an IGBT.

Turn-On transition

Referring to the schematic in Fig.4.2, when the gate voltage is applied across the gate-emitter terminals of the switch, the gate-emitter voltage rises up from zero to threshold voltage (Vth) as shown in Fig.4.4. Beyond Vth, the gate-emitter voltage continues to rise and the collector current begins to increase linearly whereas the diode current decreases. Once the forward diode current goes to zero, the current in the switch (SW) will be a combination of inductor current and reverse recovery current (see Fig.4.4 shown by the hump). With the falling of collector-emitter voltage, the gate bias current charges the gate-collector capacitance and the gate voltage remains constant and this stage is called Miller effect. When the base bias current needed for charging becomes smaller than the bias supply current then the gate voltage starts to rise again while the collector current is constant and the collector-emitter voltage falling to zero.

Turn-Off transition

When the gate-emitter voltage is switched OFF, the gate-emitter voltage starts decreasing in a linear fashion. Once the gate-emitter voltage gets below the threshold voltage, the collector-emitter voltage starts to increase linearly and the collector current remains constant since the clamp diode is OFF. Subsequently collector-emitter voltage increases and most of the gate discharge current is used up for the gate-collector capacitance, hence the gate-voltage remains constant. When the collector-emitter voltage reaches the DC input voltage, the clamp diode starts conducting and the current through the IGBT falls down linearly[62] .

4.2. Application

A direct power conversion technology that generates variable magnitude and frequency output voltage is used in the course of this study. The topology is called matrix converter and it has attracted the power electronics industry during recent years[63]–[65].

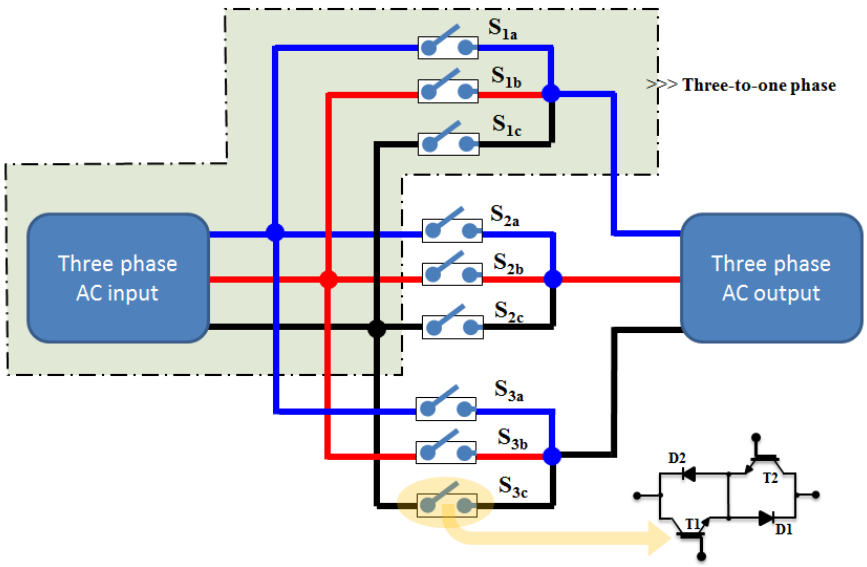


Fig.4.5 Three-to-three phase matrix converter structure

It also plays a great role in an industrial AC drives, marine, military and aerospace applications. However the maximum voltage transfer ratio factor that can be achieved with Matrix converter is limited to 0.866. Three-to-one phase matrix converter is chosen as it is an important topology which could be used to feed a single phase AC facilities in utility grid or distributed power system [66]. However, its structure can be considered as part of three-to-three matrix converter. Fig. 4.5 illustrates the schematic of the three-to-three matrix converter which contains nine bi-directional switches.

4.2.1. Bi-directional switch

Bi-directional switch is one of the major challenges for the power stage design of a three-phase to three-phase matrix converter. Matrix converter topologies require nine bi-directional switches capable of blocking voltages of both polarity and conducting current in both directions. Even though the research activity on the design and fabrication of a true bi-directional switch keep going both in academia and power semiconductor industry, suitable bi-directional switches are still not widely available as a single module that fulfils the requirement. Hence, discrete devices are configured to construct a bi-directional switch. There are four types of bi-directional switch topologies used for the matrix converter [65][64].

- Diode Bridge
- Common Emitter
- Common Collector
- Anti-parallel Reverse Blocking IGBT

However, the most commonly used bi-directional switch topologies are common collector and common emitter type switches. Only the bi-directional

switch cells that are constructed using the IGBTs are shown in this section, but other devices such as MOSFETs, SiC or GaN can also be used for the same topology.

4.2.2. Common emitter bi-directional switch

The common emitter bi-directional switch arrangement consists of two diodes and two IGBT switches that are connected in an anti-parallel form, as shown in Fig.4.6. The anti-parallel diodes provide reverse voltage blocking capability and the two IGBTs enable the independent control of the current direction. Such topology requires only two devices to conduct current at any instant; hence the conduction losses are smaller [63]. One possible disadvantage is the requirement for two gate drive circuits to operate the IGBTs. Due to its common emitter arrangement, each bidirectional switch requires an isolated power supply in order to ensure a correct operation and, hence, a total of nine isolated power supplies are needed to build a three-to-three matrix converter.

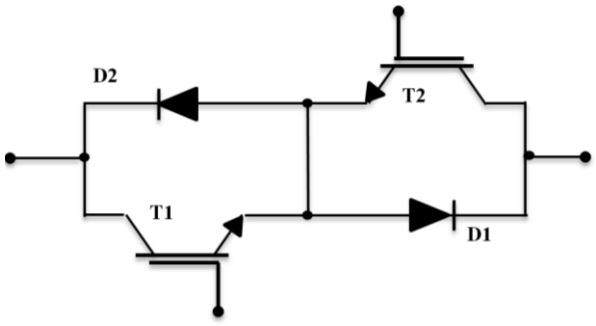


Fig.4.6 Schematic of common emitter bi-directional switch

4.2.1. Common collector bi-directional switch

The common collector bi-directional switch arrangement, shown in Fig.4.7 (a), is a topology that has the same conduction losses as the common emitter configuration due to the identical number of discrete devices. A commonly known advantage of this method is that only 6 isolated power supplies are

required to supply the gate drive signals as shown in Fig.4.7 (b) labelled with six shaded colours that shared the same gate drive. However, this advantage is only applicable where the inductance between the devices sharing the same gate drive is low. The common emitter configuration however, allows a common point (emitter) on each bidirectional switch which shares the same gate drive.

The inductance between such devices limits the power level that can be reached by the matrix converter design using six isolated power supplies and operation with such supplies is generally not viable. Therefore, the common emitter topology is generally preferred for high power application to build the matrix converter bi-directional switch [67].

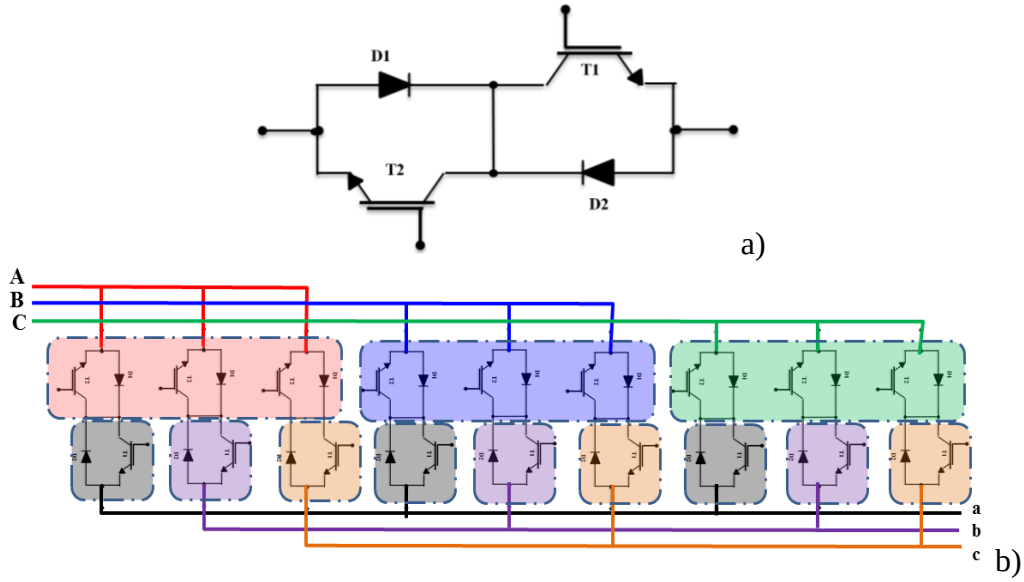


Fig.4.7 Schematic of common collector bi-directional switch, a) and its three-to-three matrix converter configuration, b)

4.3. Geometry definition and critical interconnections

The geometrical circuit construction and structural view are of particular interest for the discussion about 3D power packaging interconnection technology. The construction of power module involves several interfaces like copper tracks, ceramic layers, solders, semiconductor and passive devices.

The critical interconnections need to be carefully considered when designing the construction of the power module. From a mechanical point of view, such critical interconnections would be solder joints' thermo-mechanical fatigue and brittle materials' (ceramic and chips) fracture as it is discussed in Chapter 3. The module characteristic lifetime and reliability with respect to the critical parts and interconnections need to be evaluated based on the materials and loading distributions. Thermal and mechanical properties could be gathered from bibliographical searches, for all the materials with respect to their operating conditions, thermal and mechanical properties.

The locations of semiconductor device interconnection pads and their bonding layer properties are also important feature for the interconnection technology.
In addition to some common requirements like good electrical or magnetic performance, less processing or manufacturing cost and high reliability, different electronic devices have their own special requirements for packaging and assembly techniques. For example experience shows that during packaging process, centre gate IGBTs are more challengeable than the corner gate due to the fact that the position of the gate being at the corner is free from the surrounding emitter contact.

4.4. Power losses and cooling of a power module

Cooling of power modules is required in the first instance to prevent permanent damage of the silicon devices as they will fail if operated above 125°C [68]. High temperatures result in a degradation of electrical performance which could potentially lead to thermal runaway as the losses within the module increase with temperature.

Such losses are commonly involved with the conduction and switching losses of the power devices and the parasitic elements of the interconnection within the power module. Parameters which influence the total device power loss in a semiconductor device are junction temperature, turn-on resistance, voltage, current, and switching frequency as shown in Fig. 4.8.

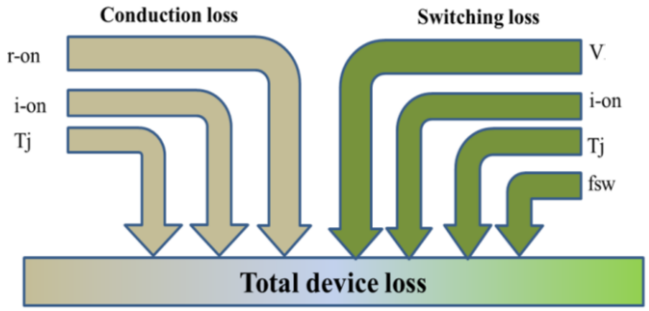


Fig.4.8 Electro-thermal parameters contributing to the power loss of the device

4.4.1. Conduction power losses

In general terms, when a semiconductor device is operating at ON-state condition, there will be a conduction loss due to its on-state resistance, current flowing through and the voltage across it (*emitter-collector, IGBT and anode-cathode, diode*) [69].

This is given by:

$$P_{con(IGBT)} = (V_{ceo} + i_c r_c) i_c \quad \text{(Eq.4.1)}$$

$$P_{con(diode)} = (V_{do} + i_d r_d) i_d \quad \text{(Eq.4.2)}$$

Where V_{ceo} - *on-state zero current emitter-collector voltage*
V_{do} - *on-state zero current diode forward voltage*
r_c - *collector-emitter on-state resistance*
r_d - *diode on-state resistance*
i_c - *collector/switch current*
i_d - *diode current*

4.4.2. General switching power loss

The other form of power loss is a switching loss created by the device switching transition behaviour, from the ON-state to the OFF-state or vice versa as depicted in Fig.4.8. As it is stated in section 4.1 of this chapter, when a semiconductor device is turned on, ideally the voltage would drop to zero and the current would reach its set level, determined by the load. However, in practice, the voltage never drops to zero and whenever the device is turned ON or OFF the current flowing through does not change instantaneously, instead rises or falls in a given time. Such behaviour of the power devices result in switching losses which is mainly caused by stray inductance [1][69]. *E*(*on*) represents the turn on energy loss and *E*(*off*) the turn off energy loss. So, the total amount of energy lost during a switching cycle is,

$$E_{tot} = E_{on} + E_{off} \quad \text{(Eq.4.3)}$$

$$P_{tot(igbt)} = \frac{1}{T}E_{on} + \frac{1}{T}E_{off} \quad \text{(Eq.4.4)}$$

$$P_{tot(diode)} = \frac{1}{T}E_{on} \quad \text{(Eq.4.5)}$$

where

E_{on}	*-on-state energy loss*
E_{off}	*-off-state energy loss*
E_{tot}	*-total energy loss*
P_{tot}	*-total power*
T	*-time preriod*

As from the relationship between energy and power, the total power loss is the product of the energy lost and switching frequency (f_{sw}).

$$P_{tot(igbt)} = (E_{on} + E_{off})f_{sw} \quad \text{(Eq.4.6)}$$

$$P_{tot(diode)} = E_{on}f_{sw} \quad \text{(Eq.4.7)}$$

These total power losses are combination of conduction and switching losses from which the switching loss can be extracted for both IGBT and diode.

$$P_{tot(igbt)} = P_{con(igbt)} + P_{sw(igbt)} \quad \text{(Eq.4.8)}$$

$$P_{tot(diode)} = P_{con(diode)} + P_{sw(diode)} \quad \text{(Eq.4.9)}$$

4.4.3. Switching power loss in matrix converter

To determine the switching losses in each stage of the three-level-output-stage matrix converter, it is important to understand the commutation mechanism between the switches.

Current commutation between switches in matrix converters is more difficult to achieve than in conventional voltage source inverters since there are no inherent freewheeling paths. The commutation has to be actively controlled at all times with respect to two fundamental rules. These can be visualised by considering just the two switches undergoing commutation on one output line of a matrix converter as illustrated in Fig. 4.9.

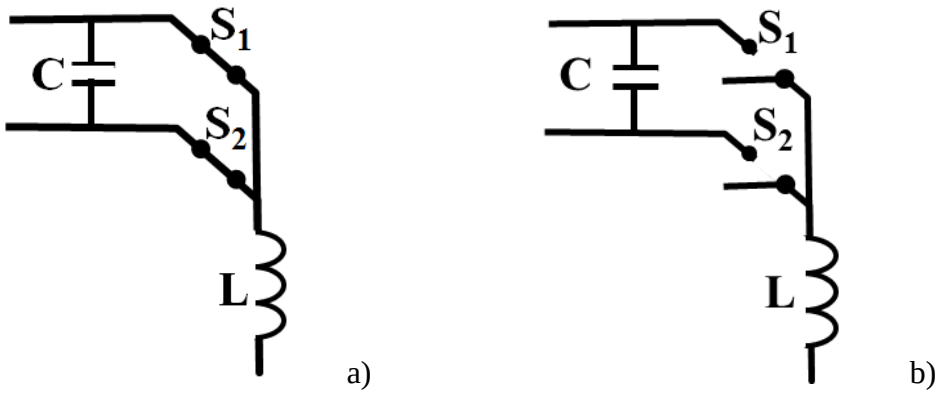


Fig.4.9. Matrix converter commutation fundamental rules: a) avoid short circuits of capacitive input lines; b) avoid open circuits of inductive output lines.

As in Fig.4.9 (a), no two or more bidirectional switches on the same output line can be turned ON at the same time, as this would lead to a line-to-line short circuit. The bidirectional switches for each output phase should not all be turned OFF at any point in time, as shown in Fig.4.9 (b). This would result in the absence of a path for the inductive load current which causes large

overvoltage. These two conditions cause a conflict since semiconductor devices cannot be switched instantaneously due to propagation delays and finite switching times. Fig4.10 illustrates the three-to-one phase matrix converter containing three bi-directional switches.

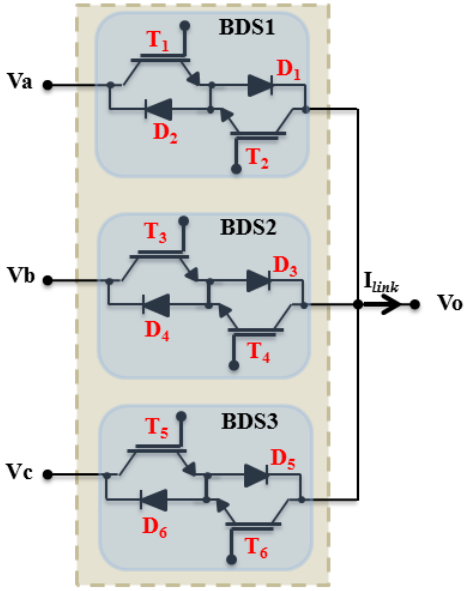


Fig.4.10. Schematic diagram of three-to-one bi-directional switch matrix converter

Different commutation methods are used in academia and industrial application [1] but for this particular experimental test a method based on knowledge of the input voltage polarity between commutating switches is used. Fig.4.11 clearly illustrates the detail logic state diagram of four step voltage based commutation. The concept of this strategy is to form a free-wheeling path in each bidirectional switch cell involved in commutation. The commutation process begins by identifying the 'free-wheeling' device in each bidirectional switch (BDS) cell based on the relative magnitudes of the input voltages.

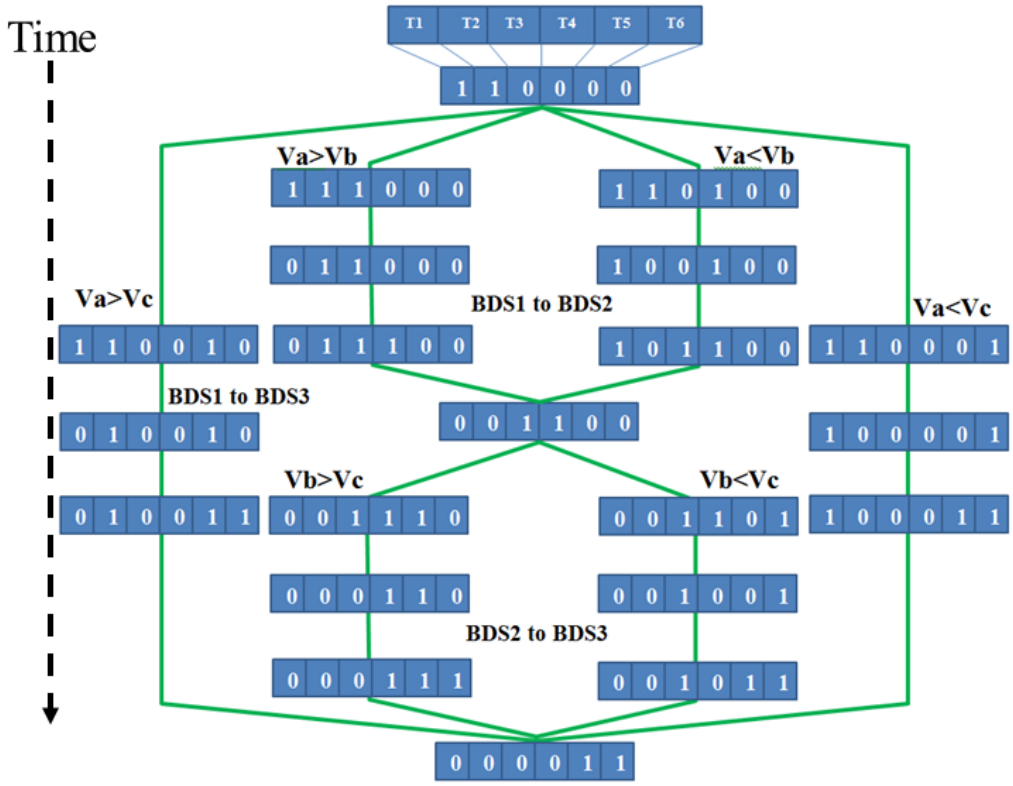


Fig.4.11. Logic state diagram for three-to-one phase four step commutation strategy

The commutation scheme is set to generate a constant output voltage, by properly changing the required gate pattern at all times. In such topology, current commutations take place not between device pairs in the same BDS, but within device pairs in different phases and switches, conducting current in the same direction. So, for instance, in the case of Fig.4.12 and 4.13, current commutations would be between the pairs T1-D1 and T3-D3 (BDS1 to BDS2), T1-D1 and T5-D5 (BDS1 to BDS3), T3-D3 and T5-D5 (BDS2 to BDS3) during the positive half wave of the input voltage; between the pairs T2-D2 and T4-D4 (BDS1 to BDS2), T4-D4 and T6-F6 (BDS2 to BDS3), T2-D2 and T6-D6 (BDS1 to BDS3) during the negative half-wave. The commutation sequence for the case where Vab >0 is also presented in the state diagram and schematic illustrated as in Fig.4.12 and 4.13 respectively holding two overlaps and one dead time switching transition.

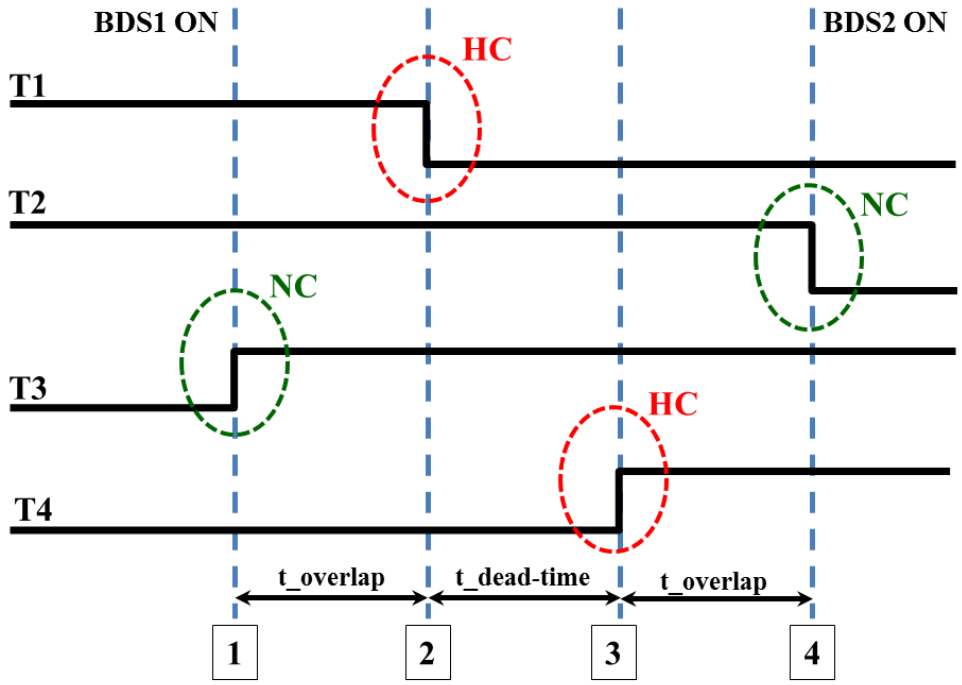


Fig.4.12. Timing diagram four step voltage based commutation (Va>Vb) where HC refers to hard commutation and NC is natural commutation

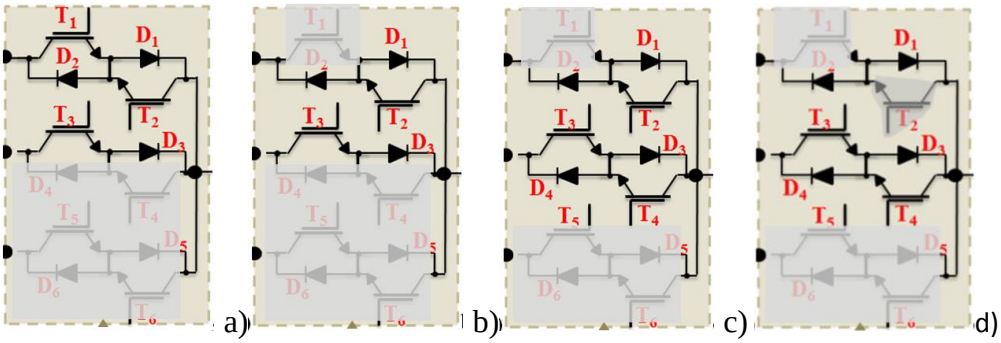


Fig.4.13. Voltage based commutation from BDS1 to BDS2

Referring to schematic and timing diagram shown in Fig.4.10, Fig.4.12 and Fig.4.13, if I_{link} is positive, the commutation will occur at point 2 results a hard turn-OFF in T1(BDS1) and a soft turn-ON "natural commutation (NC)" in T3 (BDS2). Conversely, if I_{link} is negative, commutation will happen at point 3 results a hard turn-ON in T4 (BDS2) and soft turn-OFF in T2 (BDS1). Table 4.1 summarizes the switching energy losses involved in the commutations between BDS1 and BDS2 for different commutating current polarities and the relative magnitudes of Va and Vb.

Table 4.1 the switching energy loss for current commutation between two bi-directional switches (BDS1 and BDS2)

	$\mathbf{I_{link} > 0}$		$\mathbf{I_{link} < 0}$	
	BDS1>>BDS2	BDS2>>BDS1	BDS1>>BDS2	BDS2>>BDS1
Va > Vb	T1 >> E-OFF T3 >> zero (NC)	T1 >> E-ON T3 >> zero (NC)	T2 >> zero (NC) T4 >> E-ON	T2 >> zero (NC) T4 >> E-OFF
Va < Vb	T1 >> zero (NC) T3 >> E-ON	T1 >> zero (NC) T3 >> E-OFF	T2 >> E-OFF T4 >> zero (NC)	T2 >> E-ON T4 >> zero (NC)

The natural commutation are not completely lossless however the energy loss involved in soft switching is at least an order of magnitude less than for the hard switching, only the energy losses due to hard switching in matrix converter topology are considered in most literatures [70]. The switching energy loss is linearized into a form that is directly proportional to the blocking voltage and conducting current during the switching event [71].

$$E_{sw} = E_{swr} \times \frac{|v| \times |i|}{V_R \times I_R} \qquad \text{(Eq.4.10)}$$

where

E_{swr}	*-rated switching energy loss*
V_R	*-reference voltage*
I_R	*-reference current*
v and i	*-commutation voltage and current*

The reference voltage and current are parameters provided by the datasheet of a particular switching device (IGBT or diode). In the event of hard commutation, E_{swr} is an ON state energy loss while "v" is the voltage across the switch right before the commutation and "i" is the current flowing through the switch right after the commutation. Conversely, E_{swr} is E_{off} during hard turn OFF commutation where "v" is the voltage across the switch right after commutation and "i" is the current flowing through the switch right before the commutation. Therefore, once the energy is extracted properly using Eq.4.10

the average switching power loss can be estimated using Eq.4.6 and 4.8 under a given time interval.

4.4.4. Junction temperature

The on-state resistance of a device is temperature dependent; hence the device conduction losses are also temperature dependent. Since junction temperature is dependent on the total device power losses, a mechanism to extract the power losses using the device physics by interacting with the thermal properties of the switching device, cooling system and the external load conditions is needed. This clearly shows that electro-thermal simulation framework is essential to be able to simulate the coupled electro-thermal system and provide a suitable thermal model [72]. This means that a thermal model is required which can produce a profile of the device junction temperature, using a device power loss profile. In order to create a suitable thermal model the packaging structure which is going to be modelled must be understood. Once the packaging structure is well known, the thermal performance of a given power module can then be easily extracted. For example, it can be measured by the maximum temperature rise in the chip at a given power dissipation level, with a fixed cooling device temperature. The lower the chip temperature, the better the module performance will be. As the thermal resistance from the junction of the chip to the cooling device is reduced, higher power densities can be achieved for the same temperature rise or for the same power density, a lower junction temperature can be attained [6].

4.4.5. Cooling a power module

As from the discussion in Chapter 2, the existing power modules are constructed by bonding the chip, copper layers, substrate and the base plate together. The whole module is then mounted on a heat sink using thermal grease or a thermal pad. The thermal greases used by the industry today that can stand high temperatures and have very low conductivities on the order of 0.3 to 4W/mK. As a result of this small thermal conductivity, the thermal grease contributes an increase to the total thermal resistance between the junction and the cooling device. Therefore it is essential to minimise this resistance by increasing the thermal conductivity of the thermal grease. However, either thermal grease or pads with high thermal conductivity are not available in the market. Therefore, avoiding such interface will be the best solution while decreasing the overall thermal resistance of the power module. Such design could also be constructed with double sided cooling system as it is discussed in Chapter 3 where the cooling system is targeting the hot spot without any baseplate and heat sink attached to the module.

4.5. Converter topology case study

This study typically focuses on discrete semiconductor devices such as IGBT and Diode chips based converter using flip chip technology. The technique benefits from the space exploitation and high power density figures while having double sided cooling capability. The interconnection method is chosen to be fully bond-wire-less using a power bump technology where conducting metal bricks or cylinders are kept between the top and bottom chip using solder joint. Mainly, it includes comprehensive characterisation of the selected circuit design interconnection in terms of thermo-mechanical, electro-magnetic, and

insulation behaviour. Generally, the study covers comprehensive discussion on the application, modularity, manufacturability, electrical functionality, and performance of the selected power module.

4.5.1. Functionality and performance

From previous work [56], an innovative vertical integration scheme for three-to-one phase bi-direction switch has been presented where the proposed approach enhance power density, reduce stray inductance, while enabling double-sided cooling with all devices backside kept in contact with the principal cooling surface. The results recorded from the preliminary test clearly showed the correct electrical functionality of the prototype. However, the approach was not totally bond-wire-less where the gate signals were interconnected with aluminium wire bonds. The other main issue here is that the loop inductance was also not symmetrical along each current commutation path which can result in improper current distribution. For example, looking from Fig.4.14 and the possible current commutation loop, the parasitic inductance created during commutation from BDS1 to BDS2 is smaller than that of from BDS1 to BDS3.

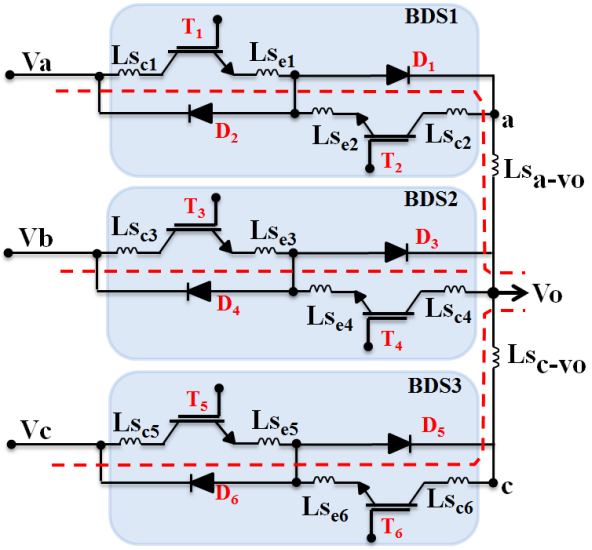


Fig.4.14 parasitic inductances of three-to-one phase matrix converter

Ls_e and Ls_c refer to emitter and collector side of stray inductances. $Ls_{a\text{-}vo}$ and $Ls_{c\text{-}vo}$ are the stray inductances between point 'a' and 'c' towards the output due to the external interconnect. Therefore, such prototype can be optimised by properly design the substrate and interconnection materials to construct three separate bi-directional switches. Unlike in the previous work, all three bi-directional switches were built as single module placed one next to the other. However, in the optimised version each bi-directional switch is placed in the symmetrical order so that the impedance mismatch would reduce. By doing so, it is possible to minimise the loop inductance while distributing uniformly along the current commutation path as clearly depicted in Fig.4.15; except the fact that the package looks bigger than the previous one. However, unused spaces can be used as space exploitation for the gate drivers and other passive components.

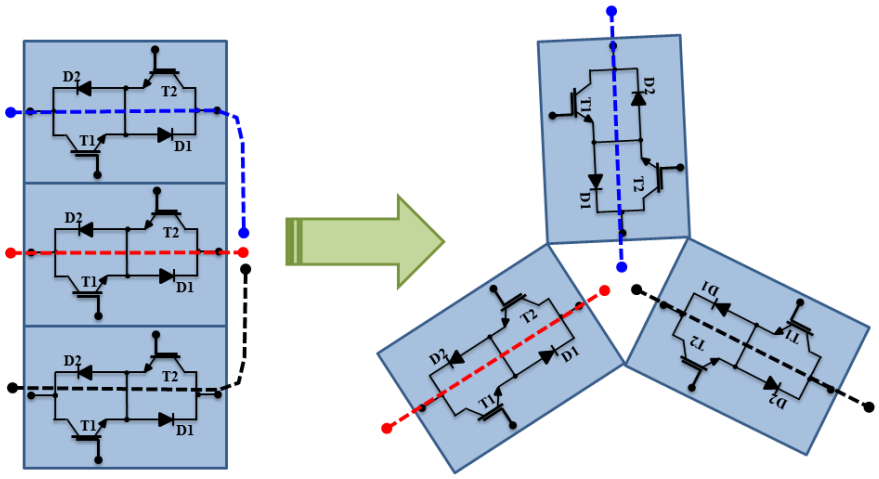


Fig.4.15 The proposed layout concept of three-to-one phase matrix converter

4.5.2. Modularity

The use of modular construction of power electronics during manufacturing certifies a large and complex unit to be broken down into small and often repetitive subassemblies that can be manufactured efficiently [29]. This clearly

makes the power module simple to repair because mostly the failure appears on the subassembly rather than the whole module. In power electronics, modularization is present only in the form of power modules, where a number of semiconductor dies connected according to the most common topologies (e.g. half-bridge or bi-directional switch) are placed in a single package. As evident from Fig.4.16, failure of a single chip implies the need to replace and dispose of the whole module, with a major disproportion between the cause and effect. This means that it is clearly understood the cost of a single chip with the cost of the whole module resulting in non-negligible long term running costs of the power system. Moreover, the impact of a single chip failure is even more significant in the case of passive components, gate drivers, sensors, and logic circuits being co-packaged with in the same module.

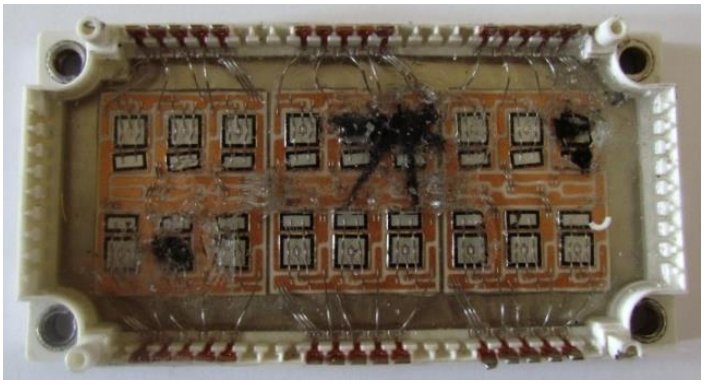


Fig.4.16 Matrix converter power module

To overcome such limitations and drawbacks, here in this study, an alternative module integration approach is hunted. Apart from the high power density performance and reliability demand of a power module, low installation and maintenance cost, good scalability and flexibility are the major factors making the power module one of the key technologies for the future generation.

4.6. Summary

In this chapter, an approach to improve the construction of three-to-one matrix converter was introduced. In Section 4.1 different basic circuit configuration of power electronic converters were discussed down to their construction on the basis of the functions they operate. The detailed introduction of the proposed case study was presented. The means to combine the methods with integration technologies into a design process (*whose introduction is pointed out in the case study)* to be able to implement them in actual workbench will be presented in Chapter 5. This chapter presents an approach that will be used as a foundation for improving the construction of power electronic module, something that will be described in the chapters that follow.

Chapter 5:
Highly Integrated Bi-directional Switch and Matrix Converter Design

This chapter includes four main sections discussing the development of the bi-directional switch based matrix converter. The first section focussed on the switch design specification and selection of materials and performance in terms of thermo-mechanical and electromagnetic behaviour using numerical simulation. In the second section, the construction of the bi-directional switches assembly with a detailed description of the manufacturing process. In the third section, detailed and general insulation process for the encapsulation of the switch assembly is discussed including the dispensing of the silicone gel and degassing the air to eliminate any void. A partial discharge test has been also carried out for five samples. The last section, the reliability characterisation of the constructed switch assembly subjected to thermal cycling testing and the assembly of the three-to-one matrix converter is described. It includes the installation of three bi-directional switch assemblies onto an integrated double sided cooler. It also includes a basic computational fluid dynamic analysis to assess the thermal performance of the assembled matrix converter.

5.1. Bi-directional Switch design specification

The stacked assembly of substrate-chip-bump-chip-substrate has been designed to implement a bi-directional switch constructed with 70 μm thin IGBTs and diodes in which their front metallization has been treated with a NiP/Pd finish to be solderable. The devices used for this design are shown in Fig.5.1. The dimension of both IGBTs and diodes are 10×9.5×0.07 mm and 9.5×5.5×0.07 mm respectively which are kindly provided by the Infineon Technologies as free samples rated at 600V/200A [Appendix 1].

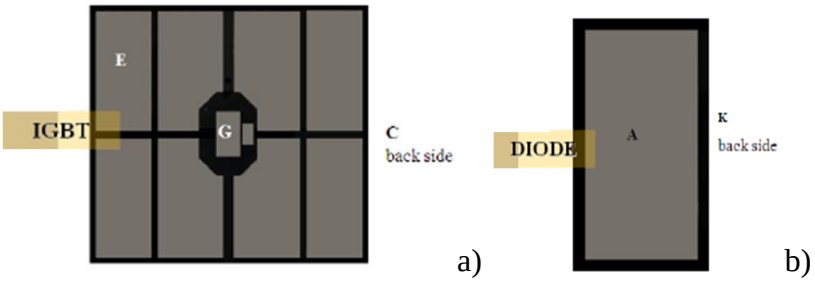


Fig.5.1 Photographs of 70μm thin: IGBT, a); and Diode, b)

Selection of substrate

Three types of substrates commonly used in power electronics have been considered and compared in [73] and the detail thermo-mechanical simulation results are listed in Table 5.1. The modelling and simulation have been carried out using commercially available finite element analysis (FEA) software called Abaqus 6.12-3 and its graphic user interface CAE (Computer Aided Engineering). The first one consists of 0.4mm thick Al_2O_3 tile sandwiched by 0.3mm thick direct bonded copper (DBC) on both sides, and this is the cheapest substrate of all. The second one is 0.3mm thick active brazed copper (ABC) on both sides of 1mm thick AlN tile. It is more expensive than the Al_2O_3-based substrate, but offers much better thermal performance. The third one is 0.3mm thick active ABC on both sides of 0.3mm thick Si_3N_4 tile. This is

the most expensive substrate, and the Si_3N_4 tile has excellent mechanical strength.

For all the three types of substrates, a layer of about 5um thick electroless NiP finish commonly existing in commercially available substrates was also included to cover all surfaces of the Cu parts on both sides of ceramic substrates to prevent corrosion and wear. Table 5.1 and [73], three different types of bumps were used to design the sandwich structure of the prototype. 2 mm diameter and 3mm long Solid cylinder, 2 mm diameter and 3mm long cylinder with 0.5mm diameter hole, and 2mm × 3mm × 3mm solid brick. Here for all cases the assembly was first subjected to a predefined temperature profile to simulate the stress and strain development. At this stage, all the solder joints were deactivated so that strain/stress did not develop up until solidification of the molten solder occurred. The power losses of IGBTs and diodes were then taken from [74] as heating source, while heat boundary conditions was applied to both top and bottom cooling surfaces of the assembly. T_{Jmax} is the maximum temperature of the chip, S_{max0}, S_{max1}, ε_{max0}, ε_{max1} are the maximum von Mises stress and maximum creep strain in the solder joints of the as-reflowed assembly and after one mission profile respectively. As can be seen from Table 5.1, the thickest AlN-based substrate has the best thermal performance among the three types of substrates, with a reduction of about 10K and 20K in the highest junction temperature of the hottest IGBT chip during the mission profile when compared to the Si_3N_4 and Al_2O_3-based substrates, respectively.

Table 5.1 Comparison of the highest junction temperatures of chips and the maximum von Mises stress, creep strain and creep strain accumulation in the solder joints

Simulation case (bump type)		$T_{J,max}$ **(K)**	S_{max0} **(MPa)**	S_{max1} **(MPa)**	ε_{max0} **(%)**	ε_{max1} **(%)**	$\Delta\varepsilon_{max}= \varepsilon_{max1}-\varepsilon_{max0}$ **(%)**
A	$Cu/Al_2O_3/Cu$ (solid cylinder)	415.0	42.9	40.6	5.34	7.61	2.27
B	$Cu/Si_3N_4/Cu$ (solid cylinder)	405.3	42.9	40.3	5.70	7.52	1.82
C	Cu/AlN/Cu (solid cylinder)	393.0	42.9	40.9	5.82	8.51	2.79
D	Cu/AlN/Cu (Hollow cylinder)	393.4	42.8	40.5	4.94	7.24	2.30
E	Cu/AlN/Cu (solid bricks)	391.8	42.2	40.1	5.43	7.59	2.16

It should be pointed out that according to the one-dimensional analysis of thermal resistance, the thinnest Si_3N_4-based substrate should transfer the heat more effectively than the thickest AlN-based substrate. This is because that the thermal conductivity of AlN is just 2.5 times greater than the Si_3N_4, but the thickness of the AlN tile is 3.3 times bigger than that of the Si_3N_4 tile. The maximum residual stresses in the solder joints after both the reflow process and the mission profile are basically similar to each other for the three types of substrates. However, the maximum creep strain accumulation in the solder joint in the assembly with the thinnest Si_3N_4-based substrate is the lowest. This result may be associated with the fact that the thinnest Si_3N_4-based substrate is relatively flexible and could absorb a certain amount of deformation energy during the mission profile. Finally, comparing the results for the simulation cases C to E in Table 5.1, it can be seen that the effect of the three bump shapes on the thermal performance of the chips is negligible. However, hollow and brick bumps can slightly reduce the maximum residual stresses, and clearly reduce the creep strain accumulation ($\Delta\varepsilon_{max}$) in the solder joints after the mission profile.

AlN based DBC Substrate

Fig.5.2 and Fig.5.3 are corresponding to the AlN based substrate model which have been designed and sent to manufacturer in order to build the required bi-directional switches.

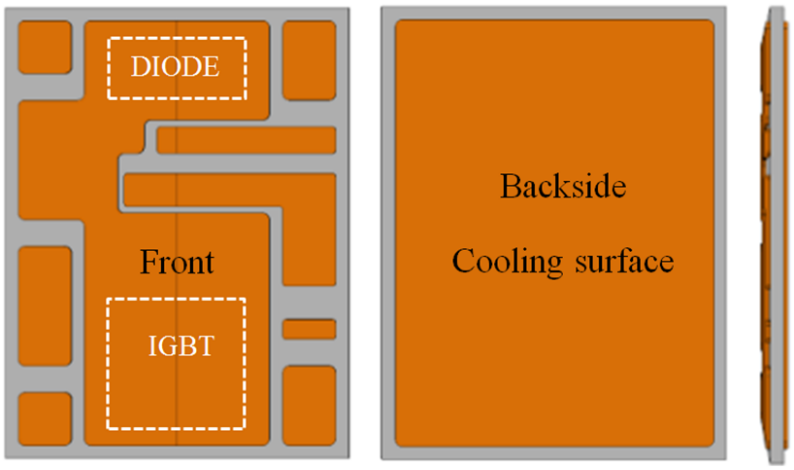


Fig.5.2 Top substrate of bi-directional switch

Here, both the top and bottom substrates are DBC substrate consisting of 1 mm thick AlN sandwiched by 0.3 mm thick copper on both sides. According to [75], 0.3 mm copper layers and 1mm thick AlN ceramic substrate are both a good compromise between the needs for the current carrying capability, better thermal conductivity and substrate reliability.

Looking from the design structure in Fig.5.3, the front surface of the substrate is the surface where both the IGBT and diode soldered backside (Collector, IGBT and Cathode, Diode) while providing terminals for gate and emitter interconnection located at one side (dotted line - A) and collector on the other side (dotted line – B) of the same substrate. The backside of both substrates can be used as a primary cooling contact surfaces to achieve double-sided cooling capability.

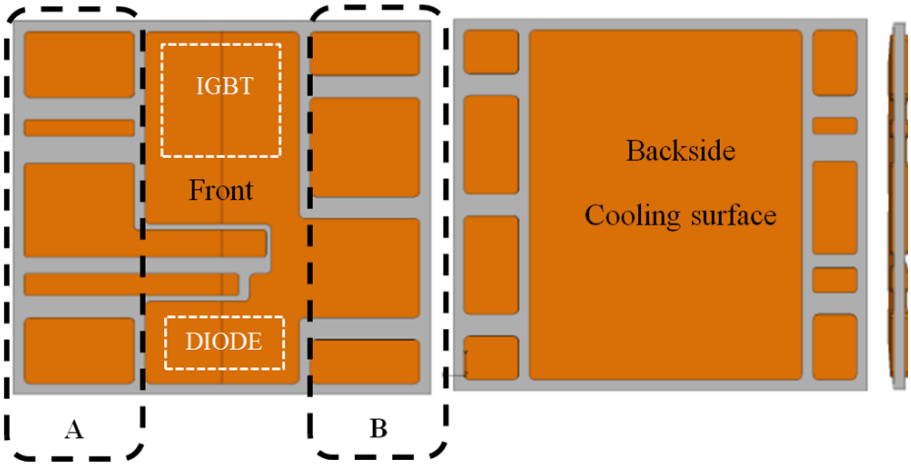


Fig.5.3 Bottom substrate of bi-directional switch

Interconnecting bumps

Fig.5.4 shows another results of numerical steady-state thermal simulations for different packaging schemes [76]. In Fig.5.4 (a), silicon chip dissipating 100 W and being effectively cooled only via the backside (representative of standard bond-wire technology) whereas in (b), effect of having surface interconnections connected to a cooling surface (i.e., heat exchange boundary conditions on top of bumps, representative of 2D integration approaches).

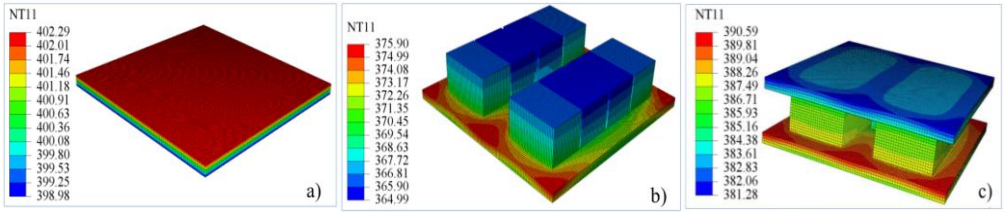


Fig.5.4 Results of steady-state thermal simulations for various packaging options: a), single silicon chip cooled via backside; b), effect of using surface bump interconnections connected to a cooling surface; c), effect of device stacking [76]

Fig.5.4 (c) shows the effect of having two devices, both dissipating power 100W and 70W, each with its backside cooled and topside interconnected by means of solid bumps of 2mm thick copper bricks (representative of the approach presented here). Here, the chip dimensions are 10 x 10 x 0.5 mm; the initial temperature is 300K in all cases; the boundary conditions on the bottom

emulate the presence of heat conduction, while the heat-transfer coefficient on the surface is set to render natural convection as depicted in Table 5.2.

Table 5.2 Heat transfer boundary condition

Case	Boundary conditions (heat transfer coefficient - W cm^{-2} K^{-1})		
	Top	Middle	Bottom
A	0.01	-	0.5
B	0.01	-	0.5
C	0.5	0.01	0.5

These results clearly show that surface bumps can be effectively used for partial heat-removal via the surface and that the arrangement considered in this work, c), further to improving stray inductance and space exploitation, still improves thermal performance as compared with standard single-sided cooling, a). A temperature difference of 12^0 K can have a huge beneficial impact in terms of reliability and lifetime, as these typically foresee an exponential dependence on temperature and the amplitude of thermal cycles.

Bi-directional switch characterisation

In addition to the above discussion and due to the reduced thickness of semiconductor devices (e.g. 70µm thick) that can offer not only superior electrical but also thermal performance as compared with thicker one [45]. It is important to understand that the effects of different interconnect geometries, sizes, materials and shapes should return optimum reliability [57]. In this work, detail thermo-mechanical analyses of different interconnection bumps are presented as shown in Fig.5.5. To improve the mechanical stiffness of the structure and reduce the mechanical stress of the chips, fixing of the upper substrate to the lower one does not only rely on the bumps on top of the silicon dies, but also on additional bigger ones, placed directly between the two substrates.

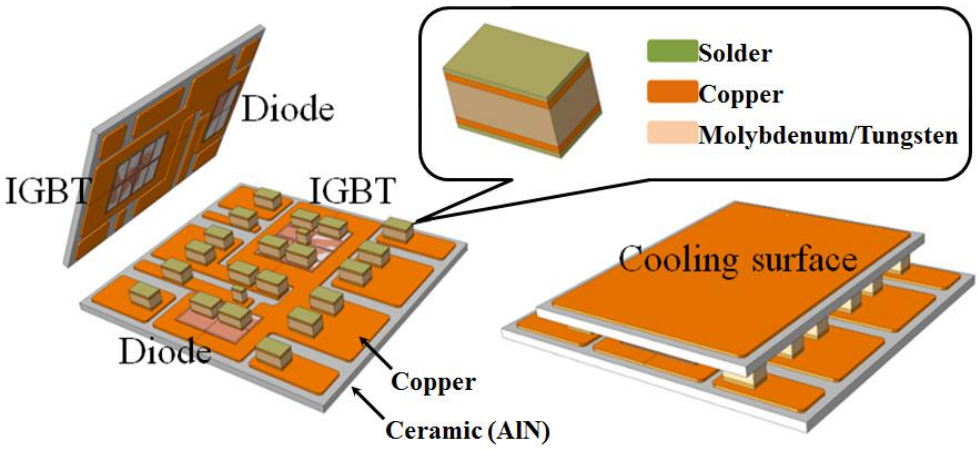


Fig.5.5 Stacked assembly of substrate-chip-bump-chip-substrate for a bi-directional switch

For these, five types of bumps consisting of pure copper, copper-molybdenum-copper (CMC) or copper-tungsten-copper (CWC) composite as shown in Fig.5.5 have been considered to investigate the effects of bump shapes and selection of materials on the thermal performance and the thermo-mechanical reliability of the stacked assemblies.

As from Fig.5.6, the bumps A are used to provide the electrical interconnects between the IGBTs and the opposite diodes. The bumps B are used to provide the electrical interconnects between the IGBTs and the opposite substrates.

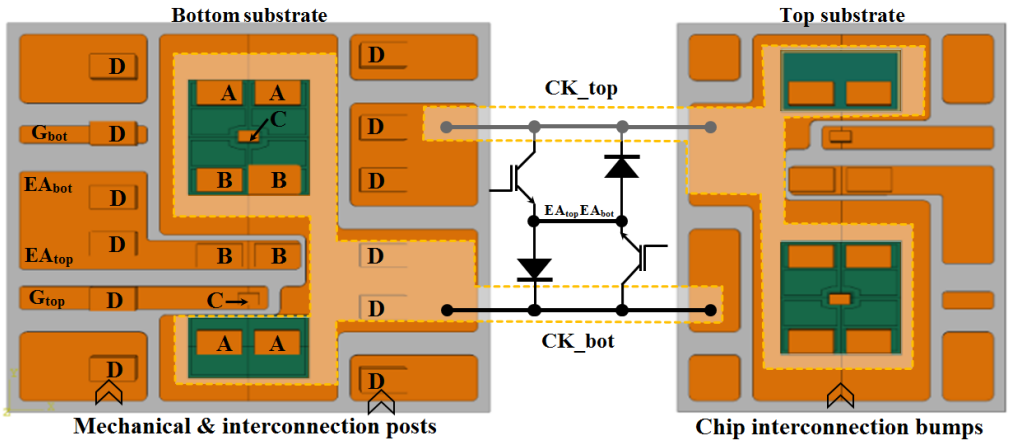


Fig.5.6 Schematic of Bi-directional switch and the corresponding structural view; where CK and EA refer to collector-cathode and emitter-anode of the IGBTs and diodes respectively and G is for gate

The bumps C are used to connect the gate signals of the IGBTs from the opposite substrates. In addition, the bumps D are used to achieve all inputs, outputs and signals of the switch to be terminated on one substrate, and provide additional mechanical support to the assembly.

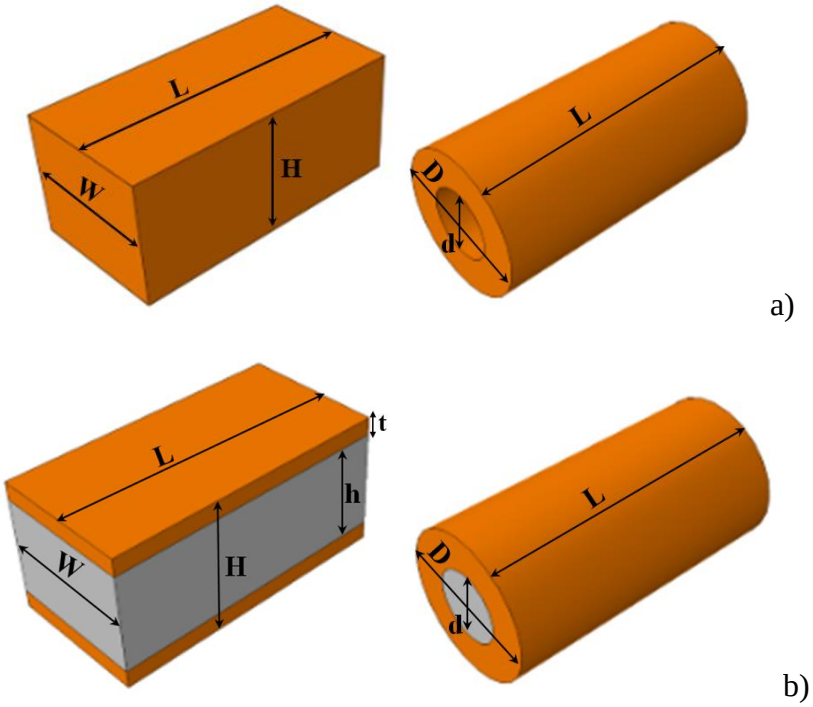


Fig.5.7 Bump interconnects; Copper only, a) CMC or CWC, b)

In Fig.5.7, *L* is length, *t* is thickness, *W* is width, whereas *H (h) and D (d)* are corresponding to the height and diameter of outer and inner side of the brick and cylinder respectively. Furthermore, several ratios of *diameter* for the Cu hollow cylinder bump, the CMC and CWC composite cylinder have also been taken into account. The dimensions of the bumps A, B, C and D shown in Fig.5.6 for all the considerations of bump shapes and selection of materials are listed in Table 5.3. These dimensions have been selected to ensure both sufficient insulating distance between the electrodes of the IGBTs and diodes in the prototype and relative convenience for assembling.

Table 5.3 Types and dimension of bump shapes along with selection of materials for the design of the stacked substrate-chip-bump-chip-substrate assembly

Bump material		***LxWxH (LxD)***			
	Design case	**Bump_A**	**Bump_B**	**Bump_D**	**Bump_C Gate**
Copper brick	Cu-Brick	3.5x2x1.5	3.5x2.1x1.7	3.5x2x1.7	1.6x0.9x1.7
Cu cylinder d = 0.25mm	CuC25	3x1.8	3x2.1	3x2.1	1.5x2.1 d = 0.25
Cu cylinder d = 0.50mm	CuC50	3x1.8	3x2.1	3x2.1	1.5x2.1 d = 0.25
Cu cylinder d = 0.75mm	CuC75	3x1.8	3x2.1	3x2.1	1.5x2.1 d = 0.25
Cu-Moly-Cu brick h/t = 0.1258mm	C**M13**C	3.5x2x1.5	3.5x2.1x1.7	3.5x2x1.7	1.6x0.9x1.7
Cu-**Moly**-Cu cylinder d = 0.25mm	C**M25**C	3x1.8	3x2.1	3x2.1	1.5x2.1 d = 0.25
Cu-**Moly**-Cu cylinder d = 0.50mm	C**M50**C	3x1.8	3x2.1	3x2.1	1.5x2.1 d = 0.25
Cu-**Moly**-Cu cylinder d = 0.75mm	C**M75**C	3x1.8	3x2.1	3x2.1	1.5x2.1 d = 0.25
Cu-Tungsten-Cu brick h/t = 0.1258mm	C**W13**C	3.5x2x1.5	3.5x2.1x1.7	3.5x2x1.7	1.6x0.9x1.7
Cu-**Tungsten**-Cu cylinder d = 0.25mm	C**W25**C	3x1.8	3x2.1	3x2.1	1.5x2.1 d = 0.25
Cu-**Tungsten**-Cu cylinder d = 0.50mm	C**W50**C	3x1.8	3x2.1	3x2.1	1.5x2.1 d = 0.25
Cu-**Tungsten**-Cu cylinder d = 0.75mm	C**W75**C	3x1.8	3x2.1	3x2.1	1.5x2.1 d = 0.25

For example, commercially available or custom prepared Cu bars, tubes and plates can be used to cut or machine into Cu cylinders, Cu hollow cylinders and Cu brick bumps, respectively.

The Cu/Mo rods can be formed using metal wire drawing technology, and then cut into Cu/Mo composite cylinder bumps. The CMC plates can be produced using combined rolling and diffusion bonding process, and then stamped into the CMC composite brick bumps [5]. However the CWC composite material is currently not available in the manufacturing process and it is in the area of research therefore in this work the model is simulated only for the sake of comparison.

Interconnecting solder

Lead free Sn-3.5Ag solder joints were used for all IGBTs and diodes attachments including bump interconnects which therefore eliminate the need for standard wire bond packaging technology. In the design, 0.1 mm in thickness of Sn-3.5Ag solder joint was chosen for attaching the IGBTs, diodes and bumps onto the substrates. It should be pointed out that the shapes of the solder joints shown in Fig.5.5 are ideal approximations for subsequent FE modelling and simulation, and those of the real reflowed solder joints might differ as this depends on how the solder is pasted onto the sample.

5.1.1 Thermo-mechanical modelling analysis

Advanced thermo-mechanical finite element (FE) modelling and simulations were carried out to spot the weak points in the assembly and investigate the effects of substrates and bumps on the thermal performance of the chip, maximum residual mechanical stress and creep strain developments in the solder joint. The effects of the bump shapes and materials on the maximum

junction temperature in the silicon chips and on the thermo-mechanical reliability of the Sn-3.5Ag solder joints and DBC substrates have been considered. Regarding the possibility of thermo-mechanical failure of the solder joints, the maximum creep strain accumulation is adopted for qualitative comparison with the simulated creep strain fields for the different design cases [31], [32], and [30]. It should be noted that these criteria are only regarded as indicators of the sequence and location of possible crack initiation, and are viewed as sufficient to provide insight and guidance for subsequent thermo-mechanical design and optimization. A more accurate prediction of the thermo-mechanical lifetime of the assembly would require a finer numerical model and a full description of the stress-strain behaviour and response of all the materials in the assembly under the relevant thermal history.

5.1.1.1. Discretization of the assembly

Fig.5.8 presents three representative meshing systems consisting C3D8 linear brick elements and DC3D6 linear triangular prism elements to discretize the design cases Cu**75** and CMC and CW**75**C. In all cases, the largest element is 1×1×0.45 mm, and the smallest element is 0.5×0.25×0.025 mm. In all the design cases listed in Table 5.3, the elements used in the critical domains all have the same dimensions. For example, the sizes of the brick elements used to discretize the critical solder joints whose maximum von Mises stress and creep strain accumulation will be used to assess the thermo-mechanical reliability are all 0.5×0.25×0.025 mm in size. This is necessary because longer computing times would be required if meshing size-independent solutions were implemented for the present three-dimensional model with a much finer

meshing system used. Therefore, relatively coarse meshing systems with the same size of elements (in the critical domains for all the design cases) have been employed to achieve an acceptable computing time. The smallest element is 0.5×0.25×0.025 mm.

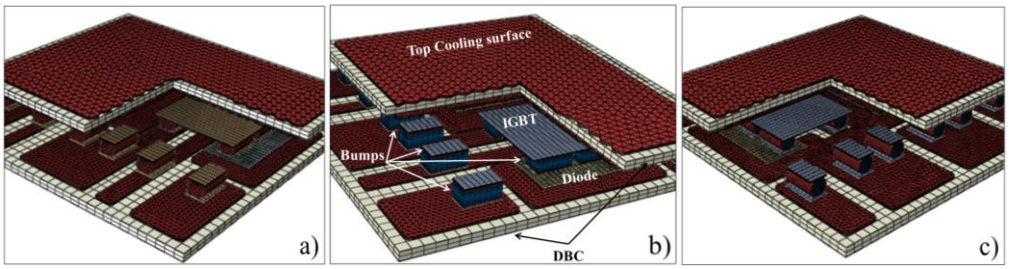


Fig.5.8 Meshing for solid and hollow bumps assembly

In addition, S4 shell elements of 0.5×0.5 mm or 0.5×0.25 mm in size were also used to discretize the NiP finish on the surfaces of the substrates and the Al metallization on both sides of the chips. This is because there is a layer of ~5 μm thick electroless NiP finish existing on all surfaces of the Cu metallization on both sides of the commercially available AlN-based DBC substrates. There were also 3.2μm/500nm/300nm thick AlSiCu/NiP/Pd metallization on the top side, and 1μm/300nm/300nm thick AlTi/Ni/Ag metallization on the back side of all the as-received IGBTs and diodes. They were assumed as a layer of 3.2 μm thick Al on the top side and a layer of 1 μm thick Al on the back side of the chips in the present model. This is justified and based on the fact that most of the NiP/Pd and Ni/Ag layers react with liquid Sn-3.5Ag solder to form intermetallic compounds (IMCs) embedded within the matrix of the solder during the reflow process [77][78], and such IMCs have been neglected. It is important to point out here that a more accurate three-dimensional model to analyse the thermo-mechanical performance of the stacked assembly should include the IMCs formed at the solder/contact metallization interfaces and their subsequent evolution during any thermal history. But, it is still an intimidating

task to solve such a three-dimensional thermo-mechanical problem because the IMCs are extremely thin when compared to other materials and parts in the model, and would require extremely fine elements to discretize them. Therefore, the formation and growth of the IMCs in this model have been ignored.

5.1.1.2. Properties of materials

The materials involved in a power module such as insulators, conductors and semiconductors behave differently under various environmental, electrical and thermal conditions. In this bi-directional switch eight different materials were implemented such as Si, Cu, Mo, W, Al, AlN, NiP and Sn-3.5Ag and their thermal and mechanical properties for the thermo-mechanical simulation are listed in Table 5.4 - Table 5.6. All the mechanical and thermal properties for the Cu, Al and Sn-3.5Ag were taken from Refs [31] and [79].

Table 5.4 Thermo-mechanical properties

	Si	**Mo**	**W**	**AlN**	**NiP**	**Sn-3.5Ag**
Thermal conductivity (W/K.m)	146	138	174	175	5	55
Specific heat (J/kg.^{0}C)	750	250	132	740	540	200
Density (kg/cm^3)	2.33	10.22	19.3	3.3	8.1	7.36
CTE (10^{-6}/K)	2.5	4.8	4.5	4.6	16.4	21.5
Young's modulus (GPa)	130	317	400	331	60	40
Poisson ratio	0.22	0.32	0.28	0.22	0.33	0.4

Table 5.5 Elastic constants and Chaboche's parameters of copper

T	**CTE**	**E**	**v**	**R_0**	**Q**	**b**	**C**	**Γ**
[K]	[$10^{-6}K^{-1}$]	[GPa]	[-]	[MPa]	[MPa]	[-]	[GPa]	[-]
218.15	17	133	0.36	33.7	196	40	93.31	1200
295.15	17.3	130.9	0.36	25	170	40	93.31	1431
473.15	19	98	0.36	5	110	40	93.31	2000
673.15	20	70	0.36	4	50	40	93.31	2700

Table 5.6 Elastic constants and Chaboche's parameters pure Aluminium

T	CTE	E	v	R_0	Q	b	C	γ
[K]	[$10^{-6}K^{-1}$]	[GPa]	[-]	[MPa]	[MPa]	[-]	[GPa]	[-]
218.15	23.5	74	0.34	15	50	45	110	3
295.15	24	66.8	0.34	10	40	45	100	3
473.15	25	50	0.34	7	10	45	40	3
673.15	28	30	0.34	4	5	45	10	3

Chaboche's plastic model was used to describe the mechanical properties of the Cu and Al, and Anand's creep model [Appendix 4] was used to characterise the mechanical properties of the Sn-3.5Ag solder alloy at varying temperatures. Anand model is a unified plastic-creep constitutive relation with one internal variable. This model is available in some commercial FEM software and one of these is in ABAQUS user defined subroutine. In real applications, the stacked assembly will be filled with a soft dielectric encapsulant and integrated with a double-sided water-based cooler. These have been ignored because silicone gel, which is commonly used as encapsulating gel, has extremely low thermal conductivity and Young's modulus compared to the other components and parts in the assembly. Therefore, the effect of ignoring the encapsulant on the simulation results to be used for the optimization of the thermo-mechanical design considered to be negligible.

5.1.1.3. Loading and boundary conditions

The power loss of the IGBTs and diodes as shown in Fig.5.9 were taken as uniform heating sources to simulate the thermal performance of the assembly during realistic traction mission profile [49] whereas Fig.5.10 is a single cycle of a -55 to 155 thermal cycle typically used for reliability evaluation. This is somehow different from the actual distribution of heating source in the devices as discussed in Chapter 4, but can offer a relatively simple way to assess the thermal performance of the different design cases as listed in Table 5.3.

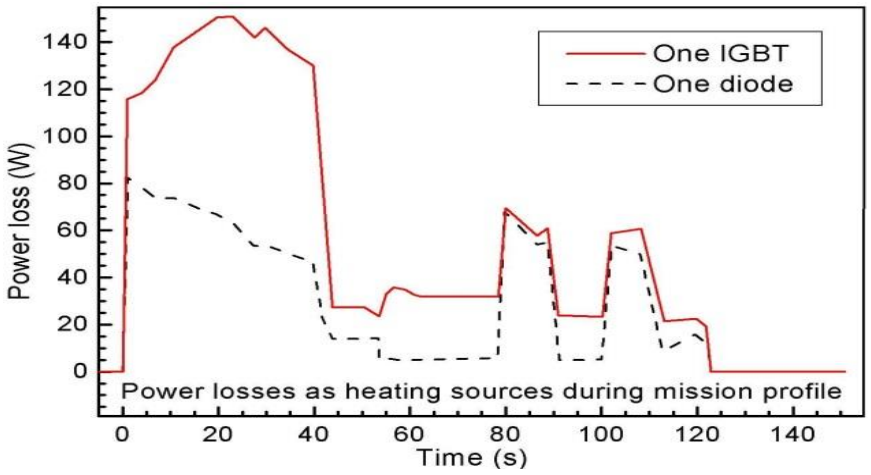


Fig.5.9 Power losses of one IGBT and one diode during a mission profile

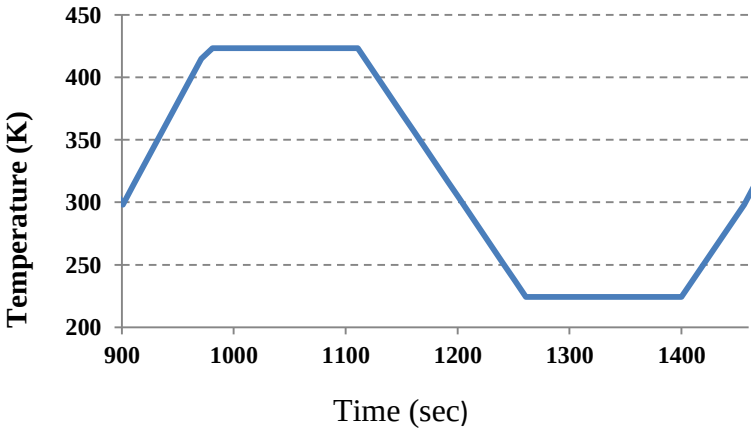


Fig.5.10 Temperature profile of one thermal cycle

The heat exchange boundary condition as described in Fig.5.11 were applied to both the top and bottom cooling surfaces of the assembly, where the heat exchange coefficient of 5000W.m^{-2}k^{-1} is typical for a water-based cooler in power electronics [29].

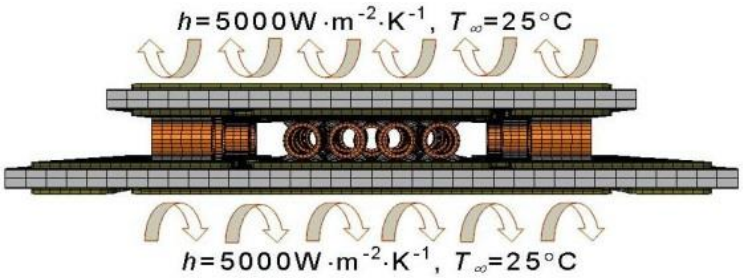


Fig.5.11 Boundary condition of heat exchange applied in the thermal simulation

The assembly was first subjected to a predefined temperature profile to

simulate the stress and strain developments during a single step reflow soldering process. During soldering step, the corresponding solder joints were deactivated without the development of stress and strain when they were in the form of either solder paste or molten solder.

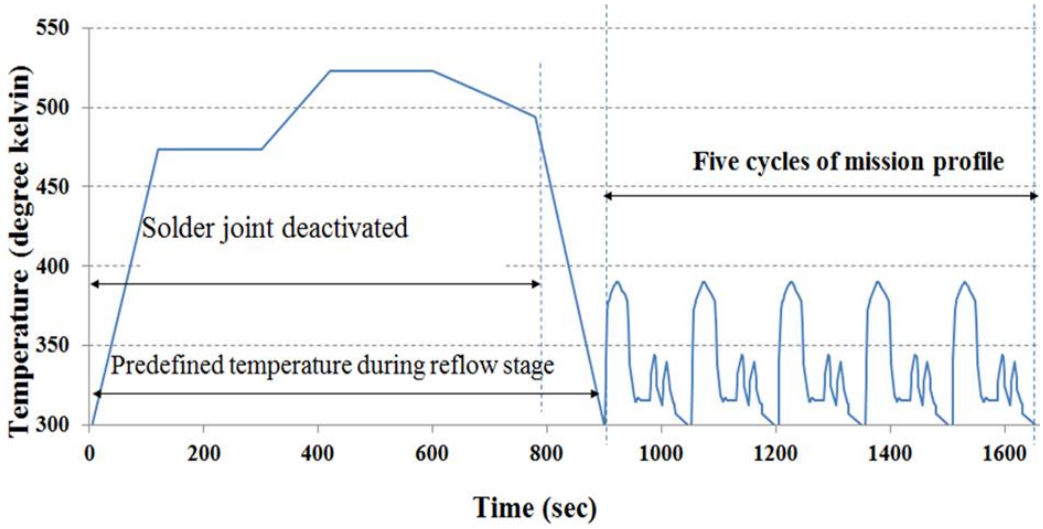


Fig.5.12 Thermal history of predefined temperature of a single reflow process followed by five cycles of mission profile

They were activated when they solidified from the molten solder. Both the solder paste and the solid solder joints are molten at the melting point of 221 ºC, and the solidification of the molten solder occurs at a super-cooling temperature of 192 ºC for Sn-3.5Ag solder alloys.

Then the thermo-mechanical response of the assembly associated with 5 cycles of a realistic mission profile and 5 cycles of thermal cycling between -55 ºC and +150 ºC, as shown in Fig.5.12 and 5.13, were further simulated independently. The temperature field obtained from the thermal simulation was used as inputs to simulate further stress and strain development in the assembly during the mission profile. For the thermal cycling, a predefined uniform temperature field in the entire assembly (following the temperature profile) was directly applied to simulate further stress and strain developments. Thermal

cycling between -55 ºC and +150 ºC has been selected because the reliability of the assembly samples for the design cases CuC25 and CM13C-Brick had been experimentally tested under this thermal cycling condition.

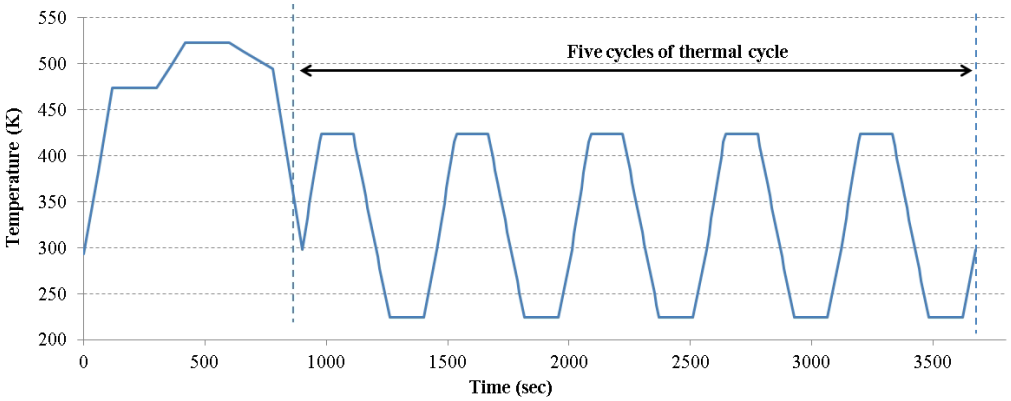


Fig.5.13 Thermal history of predefined temperature of a single reflow process followed by five thermal cycles

For the above thermo-mechanical simulations, all the parts in the assembly (for all the design cases) have been assumed to have a zero stress and strain state at the beginning of the soldering step, and the model is referred to as full model.

5.1.1.4. Simulation cases and results

All the 12 design cases listed in Table 5.7 have been simulated and subjected to the two types of thermal history associated with the mission profile and thermal cycling (as shown in Figs. 5 and 6). In total 45 simulation cases have been executed on a PC computer with Intel[R] Core[TM] i3-2100 CPU @ 3.10 GHz processor and 16 GB RAM. The running times were 50 to 60 hours for each case therefore, due to space and time only the brick bumps were simulated in case of thermal cycling.

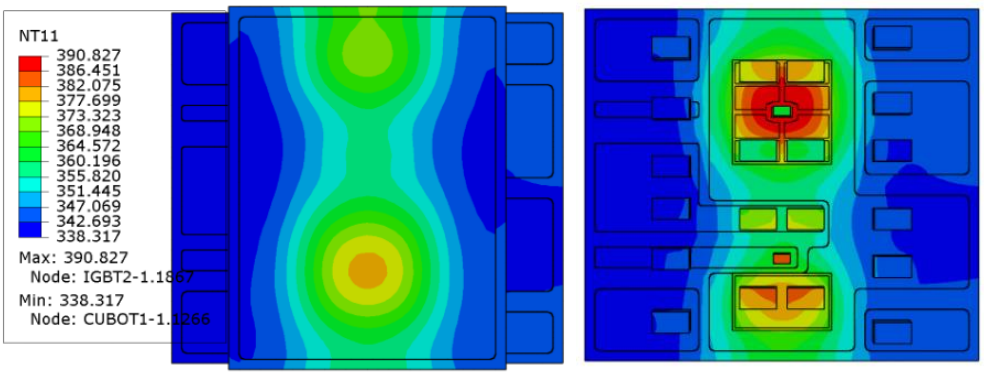
Table 5.7 Lists of chosen simulation cases

	Mission profile			Thermal cycling		
Design case	Temp	Maximum Von-Mises	Maximum Creep strain	Temp	Maximum Von-Mises	Maximum Creep strain
Cu-Brick	✓	✓	✓	✓	✓	✓
CuC25	✓	✓	✓			
CuC50	✓	✓	✓			
CuC75	✓	✓	✓			
CM13C-Brick	✓	✓	✓	✓	✓	✓
CM25C	✓	✓	✓			
CM50C	✓	✓	✓			
CM75C	✓	✓	✓			
CW13C-Brick	✓	✓	✓	✓	✓	✓
CW25C	✓	✓	✓			
CW50C	✓	✓	✓			
CW75C	✓	✓	✓			

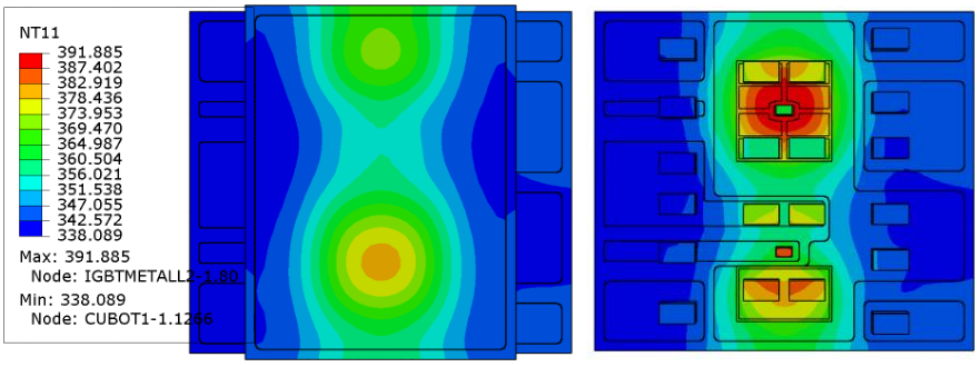
5.1.1.5. Thermal performance

Fig.5.14 presents the simulated temperature distribution field for the design case Cu-Brick, CM13C and CW13C bricks at 23.01 s during the mission profile, where in the open view, right side of each figure, the top substrate of the assembly is removed for better observation. For all design cases listed in Table 5.7, the maximum temperature can be observed on the IGBT attached to the top DBC substrate, during the mission profile. At any instantaneous time the maximum temperature on the IGBT and diode attached on the bottom DBC substrate is 0.1 ºC to 0.2 ºC lower than the corresponding devices attached on the top substrate. This is readily understood because the cooling surface (area) of the top substrate is slightly smaller than the bottom substrate while the bumps used (for joining) are similar in size and material. The thermal contour in Fig.5.14 and detailed result in Fig.5.16 compare the evolution of the simulated maximum temperature in the assembly for all the 12 design cases listed in Table 5.3 during one cycle of the mission profile. For all the design

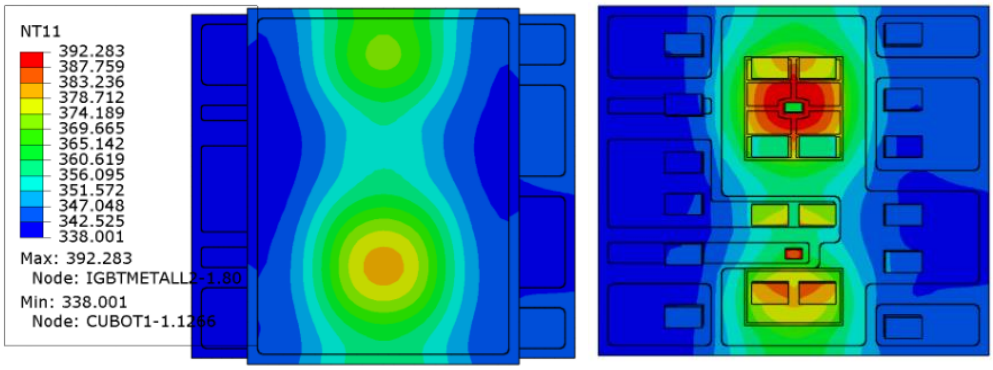
cases, the highest maximum temperature is observed at 23.01 sec during the mission profile.



a) Cu-Brick bump type model



b) CW13C-Brick bump type model



c) CM13C-Brick bump type model

Fig.5.14 Simulated temperature field at 23.01 sec during one cycle of temperature mission profile for three design cases

Compared with copper hollow cylinder bumps (CuC25) which will be used as a reference, the Cu-brick bumps can reduce the highest maximum temperature in the assembly by 2.423 ºK. This can be attributed to the fact that, in addition to the slight difference in size as shown in Fig.5.15 (b), the average thickness of the Sn-3.5Ag solder joints used to join the cylinder bumps is thicker than the average thickness of the Sn3.5Ag solder joints used to join the brick bumps.

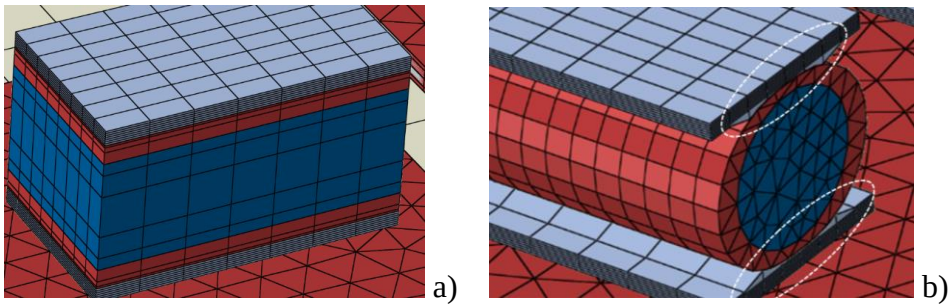


Fig.5.15 CMC bump model with solder on top and bottom; a) brick; and b) cylinder

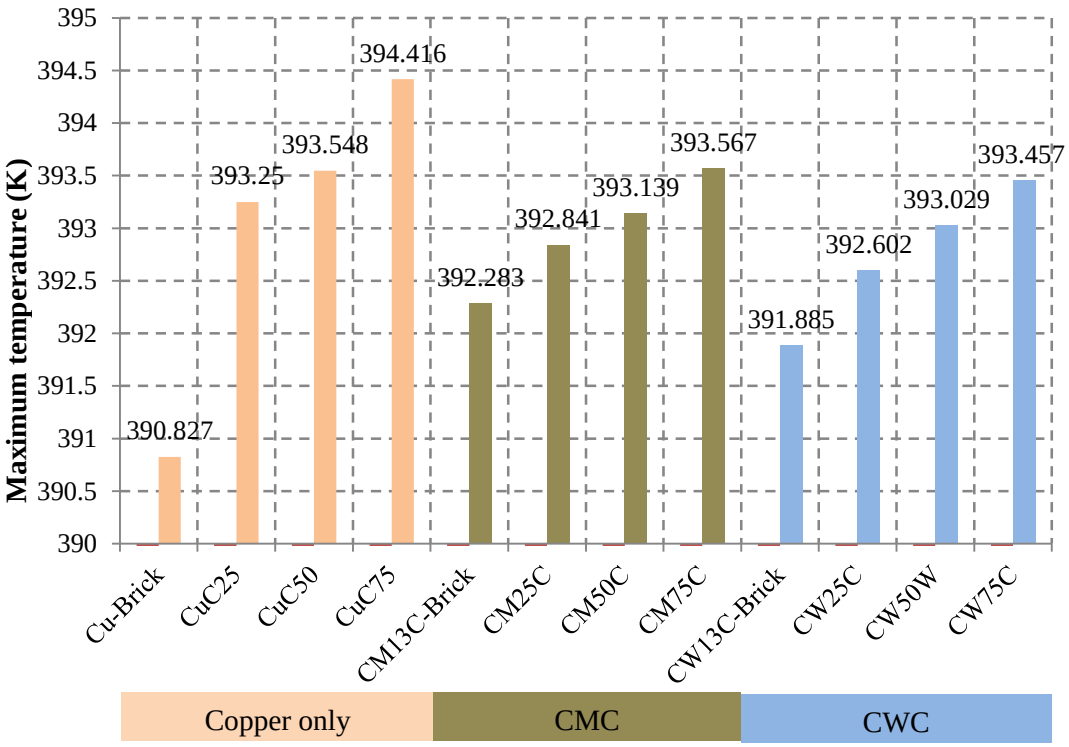


Fig.5.16 Maximum simulated temperature distribution results for all design cases

In comparison with the Cu-brick bump result in Fig.5.16, the Cu hollow cylinder bumps (CuC25, CuC50, and CuC75) with different wall thicknesses

increase the highest maximum temperature in the assembly by 2.4 ºK to 3.6 ºK. This again can be easily understood because the air gap in the hollow bumps reduces the cross-sectional area for heat transfer. In agreement, the CMC composite cylinder bumps (CM25C, CM50C, and CM75C) also increase the highest maximum temperature in the assembly by 1.5 ºK to 2.7 ºK when compared to the Cu-Brick bumps. The CWC composite cylinder bumps (CW25C, CW50C, and CW75C) also increase the highest maximum temperature in the assembly by 1.1 ºK to 2.6 ºK when compared to the Cu-Brick bumps. However, the highest maximum temperatures in the assembly with the CM13C-Brick bumps are higher than those of the Cu-Brick and CW13C-Brick bumps which can be ascribed to the Mo in the bumps which has a lower thermal conductivity than copper and tungsten.

5.1.1.6. Thermo-mechanical stresses and strains Performance

The simulation results between the design cases of Cu-Brick, CM13C-Brick and CW13C-Brick are compared for the, maximum von-Mises stress, distribution of creep strain accumulation, and maximum Max-principal stress. The maximum von Mises stress and creep strain accumulations are at the corners of the solder layer in contact with the emitter metallization of the IGBT, which are the most critical areas of failure.

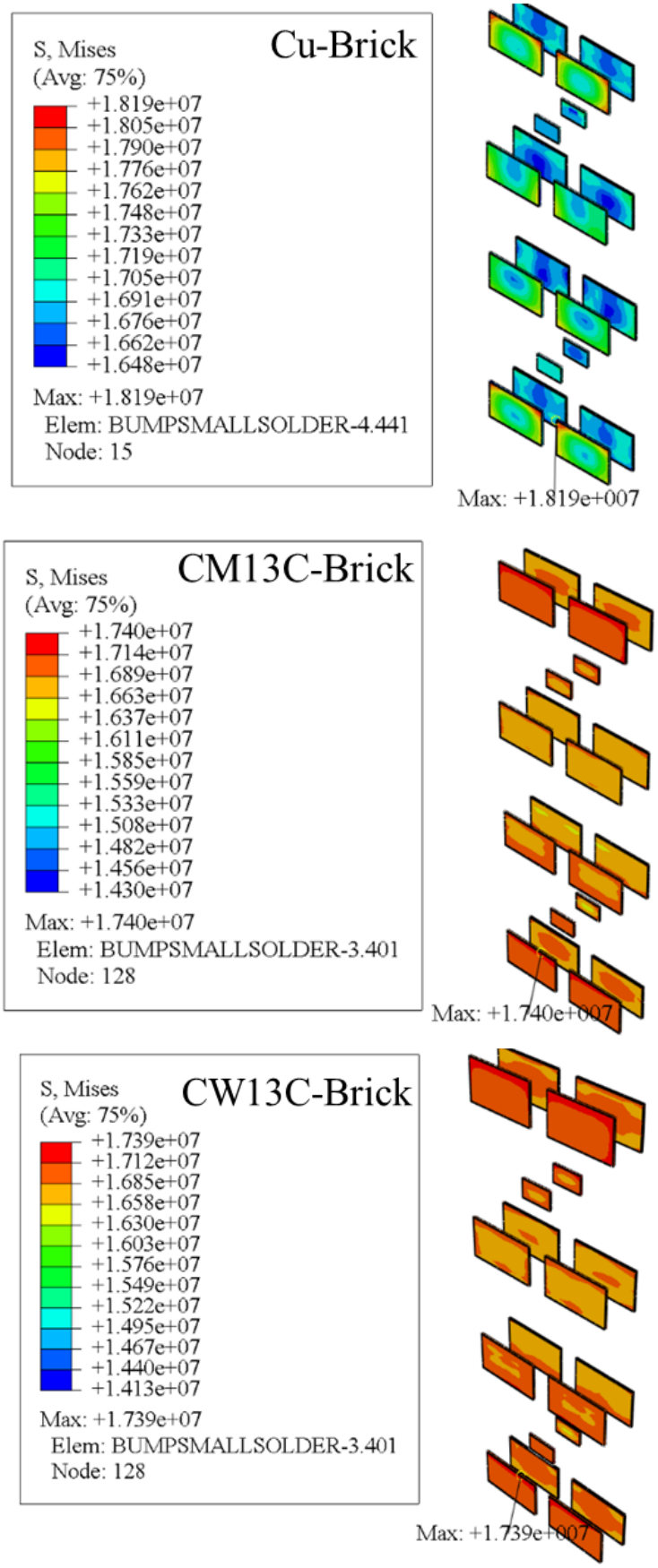


Fig.5.17 Simulated distribution of Von Mises stresses in the solder joints for bump interconnection after 5 cycles of mission profile for three design cases

Such a result can be attributed to the mismatch of thermal expansion between the Sn-3.5Ag solder and the Si chips. Furthermore, it is also related to the joining area or the shapes and size of the bumps. This can be seen from the representative simulated results of the assembly with Cu-Brick, CM13C-Brick and CW13C-Brick bumps as shown in Fig.5.17 and 5.18 respectively.

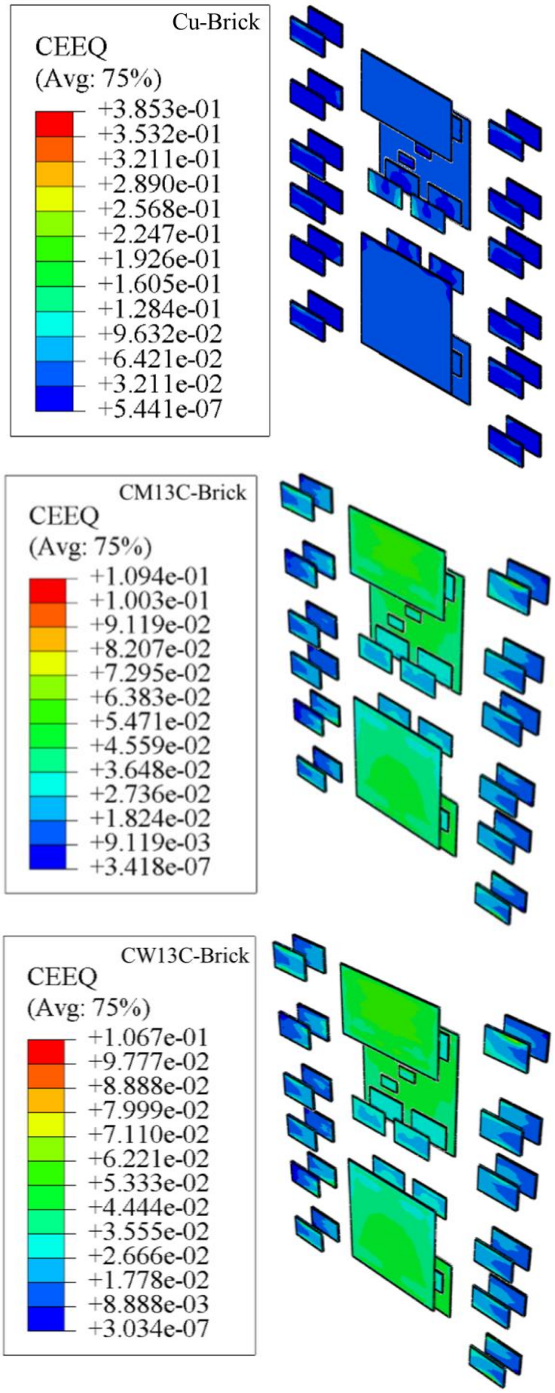


Fig.5.18 Simulated distributions of creep strain accumulation in all solder joints after 5 cycles of mission profile for three design cases

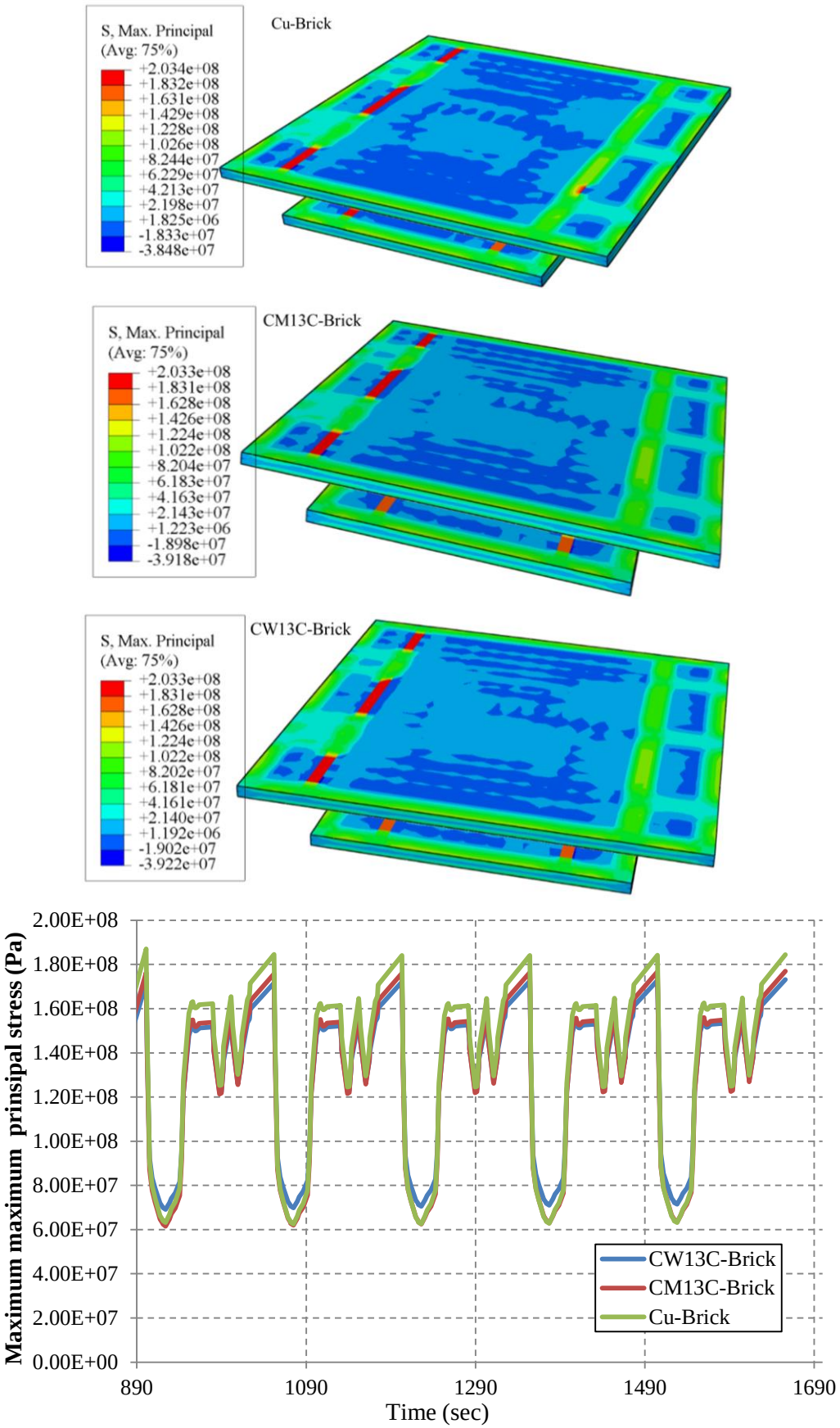


Fig.5.19 Distribution of the maximum principal stress (pa) in the AlN tiles of the DBC substrates in three design cases after 5 cycles of mission profile (3D contour and data)

As from the result for the maximum principal stresses in the AlN substrate tiles of the DBC substrate depicted in Fig.5.19, the results also clearly show that the stress and strain developments in the materials are controlled by the mismatch of coefficients of thermal expansion between the materials and the accumulations of plastic and/or creep strains in the copper and solder alloy. Different amounts of mismatches in the coefficient of thermal expansion between the materials in the different design cases dominate the relative sizes of the stress and strain development in the DBC substrates. The AlN substrate tiles of the DBC substrates, where both CM13C-Brick and CW13C-Brick type bumps were used in the construction of the switch can slightly reduce the maximum principal stress when compared to the Cu-Brick type switch. One needs to consider that these small differences between each case are only an indication for five cycles of both profiles. However, as evident form the strain curve in Fig.5.23, the higher the cycling profile is, the wider the differences will be.

5.1.1.7. Mission profile and thermal cycling influence

The assemblies have been subjected to relatively high temperatures for longer durations during the 5 thermal cycles than that of the mission profile. High temperatures at longer duration would of course promote creep strain accumulation that leads to the release of more stress. Therefore, the results of mission profile and thermal cycling have significant different effects on the stress and/or strain development in the whole assembly.

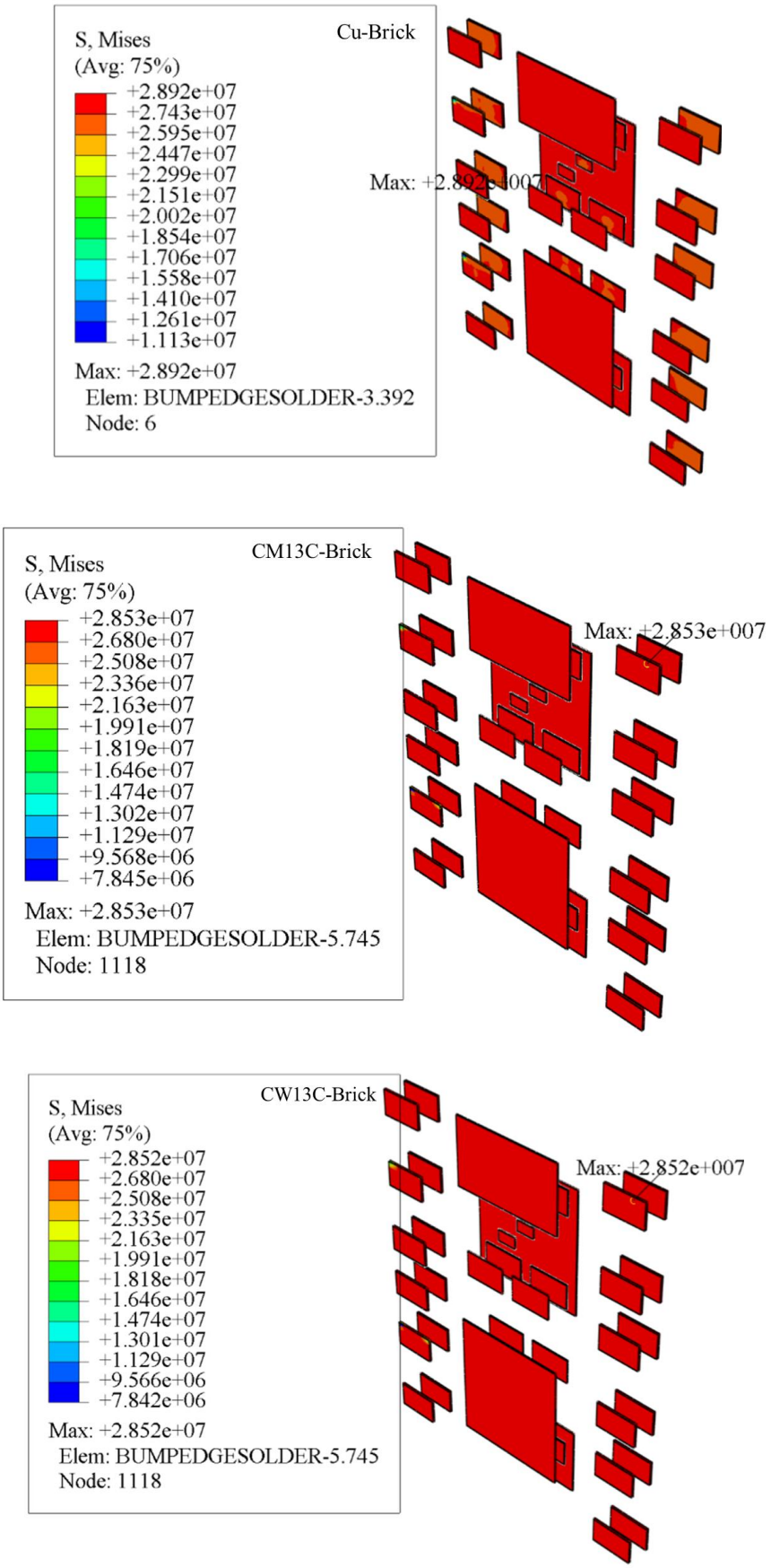


Fig.5.20 Simulated distribution of Von Mises stresses in the solder joints after 5 cycles of thermal cycling for three design cases

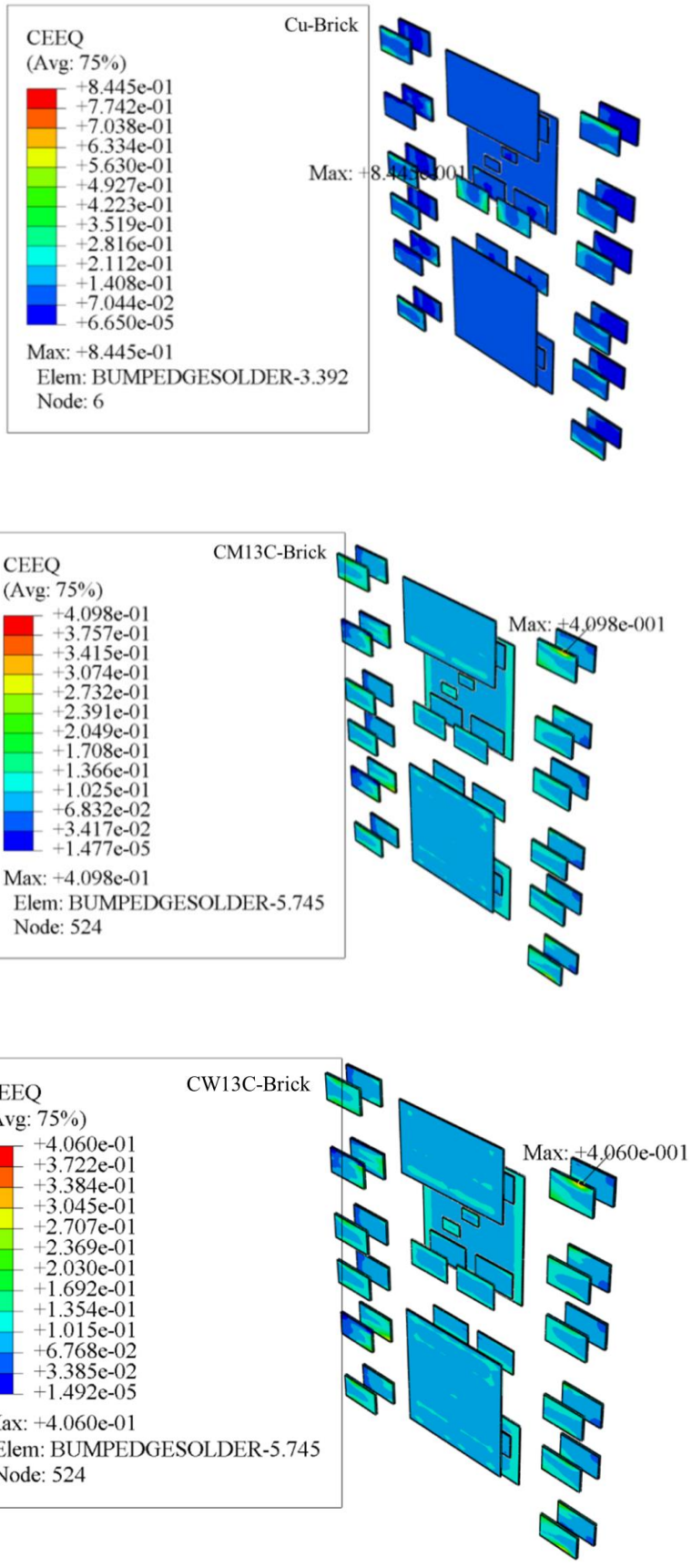


Fig.5.21 Simulated distributions of creep strain accumulation in the solder joints after 5 cycles of thermal cycling for three design cases

For all design cases listed in Table 5.3, the relevant maximum stresses and strain in different parts have been observed at the corners and edges of the interfaces between the different materials, irrespective of the mission profile or thermal cycling. As from Fig.5.17 and 5.18, the maximum von Mises stresses and creep strain accumulations occur in the solder joints between the bumps and IGBTs during mission profile. However, during thermal cycling they occur in the solder joints between bumps and DBC substrates as shown in Fig.5.20 and Fig.5.21.

This can be explained to the relatively high temperatures in the solder joints (between bumps and silicon chips) when compared to those in the solder joints (between bumps and DBC substrates) during mission profile and thermal cycling. The solder joints with the maximum creep strain accumulations are in general identified as the thermo-mechanically weak spot [30]. Therefore, care must be taken when the results of thermal cycling are used to predict the failure and life times of the assembly during realistic mission profile.

5.1.1.8. Effects of bump shapes and materials

Fig.5.22 and 5.23 compare the simulated von-Mises stress and creep strain in all solder joints for die attachment and bump interconnection between the assemblies with four different types of bumps for the three design cases. In comparison with the Cu-Brick type bumps, using relatively compliant Cu hollow cylinder bumps (design cases CuC25, CuC50 and CuC75) can reduce the maximum von Mises stresses and creep strain accumulations in all the solder joints to some extent during the mission profile.

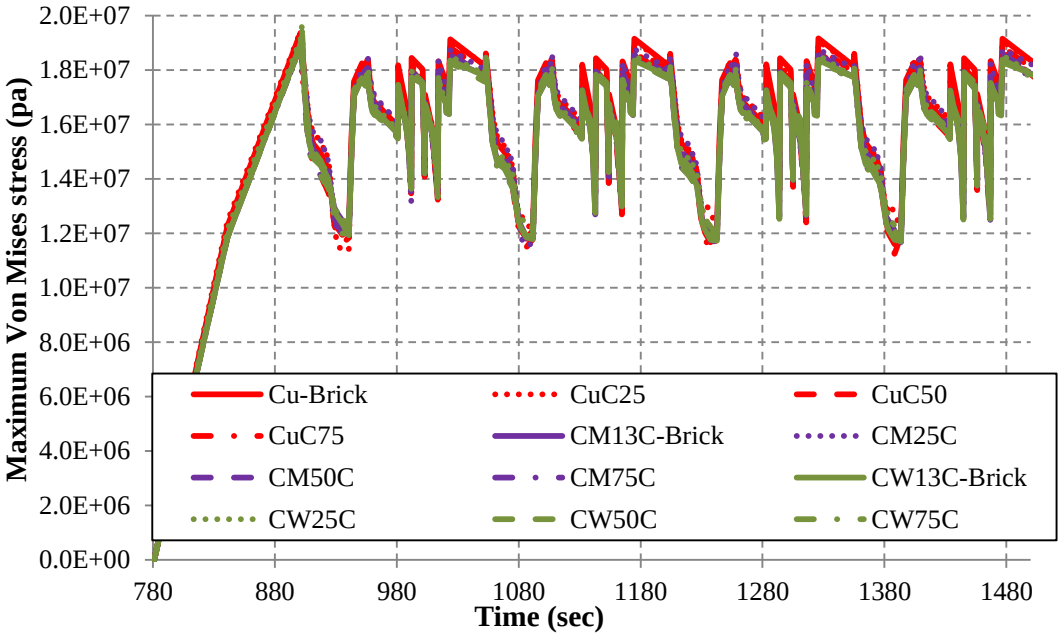


Fig.5.22 evolution of maximum von Mises stress in the solder joints in all design cases

It is noted also that the maximum residual stress in the solder joints for the bump interconnects decrease with decreasing the wall thickness of the bumps.

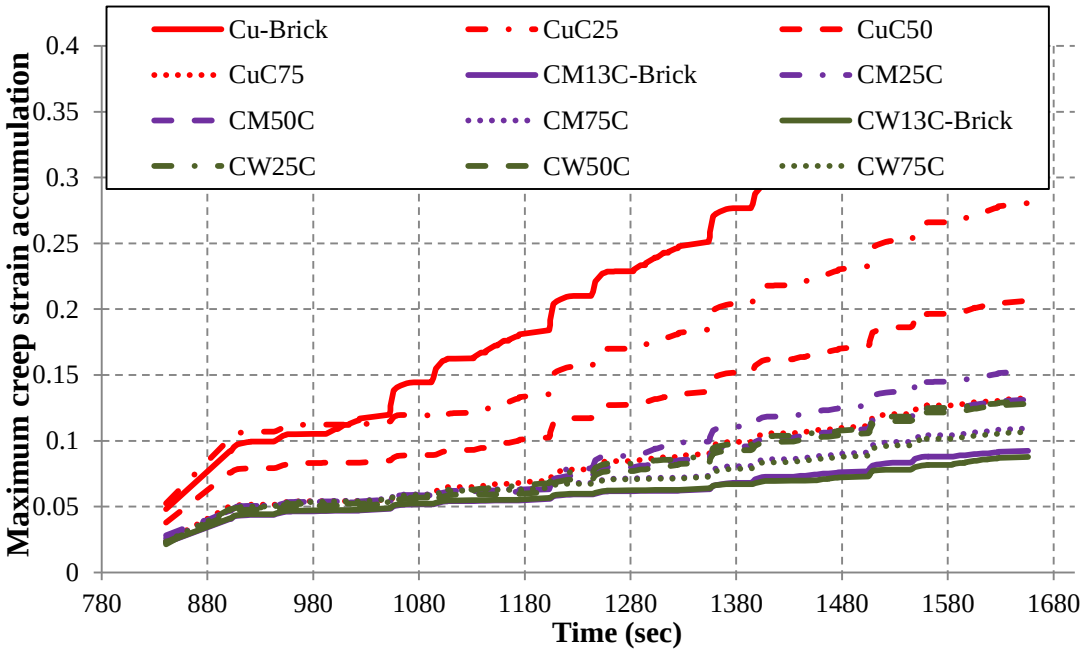


Fig.5.23 Evolution of maximum creep strain accumulations in the solder joints in all the design cases of mission profile

However, in comparison with the CMC and CWC Brick type bumps, using relatively compliant cylinder bumps (design cases CM25C/CW25C, CM50C/CW50C and CM75C/CW75C) can increase the maximum von Mises

stresses and creep strain accumulations in all the solder joints to some extent during the mission profile.

In case of hollow cylindrical bumps, this is readily understood that because bumps with thinner walls can be the bumps to be more compliant. As a result, the more compliant bumps can withstand more elastic deformation, and the solder joints and silicon chips need relatively low stress development against the CTE mismatch and different deformations. Whereas in CMC/CWC type bumps, the thicker the copper part is less effective in reducing the existence of CTE mismatch between the bumps, silicon chips and DBC substrate.

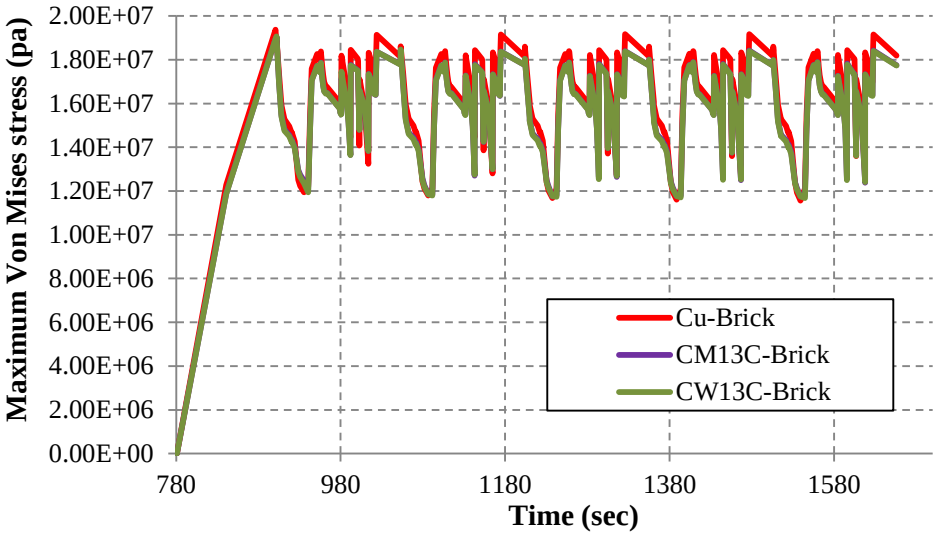


Fig.5.24 Comparison of the evolutions of maximum von Mises stress in the solder joints for the three design cases; a) five cycles of mission profile;b) five thermal cycles

The comparison between three main brick bumps using two different thermal histories are illustrated in Fig.5.24 and Fig.5.25. The simulated result for maximum von Mises stress and maximum creep strain in all solder joints respectively in both cases. More effectively, using the CM13C and CW13C composite brick bumps, the maximum von Mises stresses and creep strains in all solder joints can be reduced when compared with those using all copper based and CMC/CWC cylindrical bumps during both the mission profile and the thermal cycling.

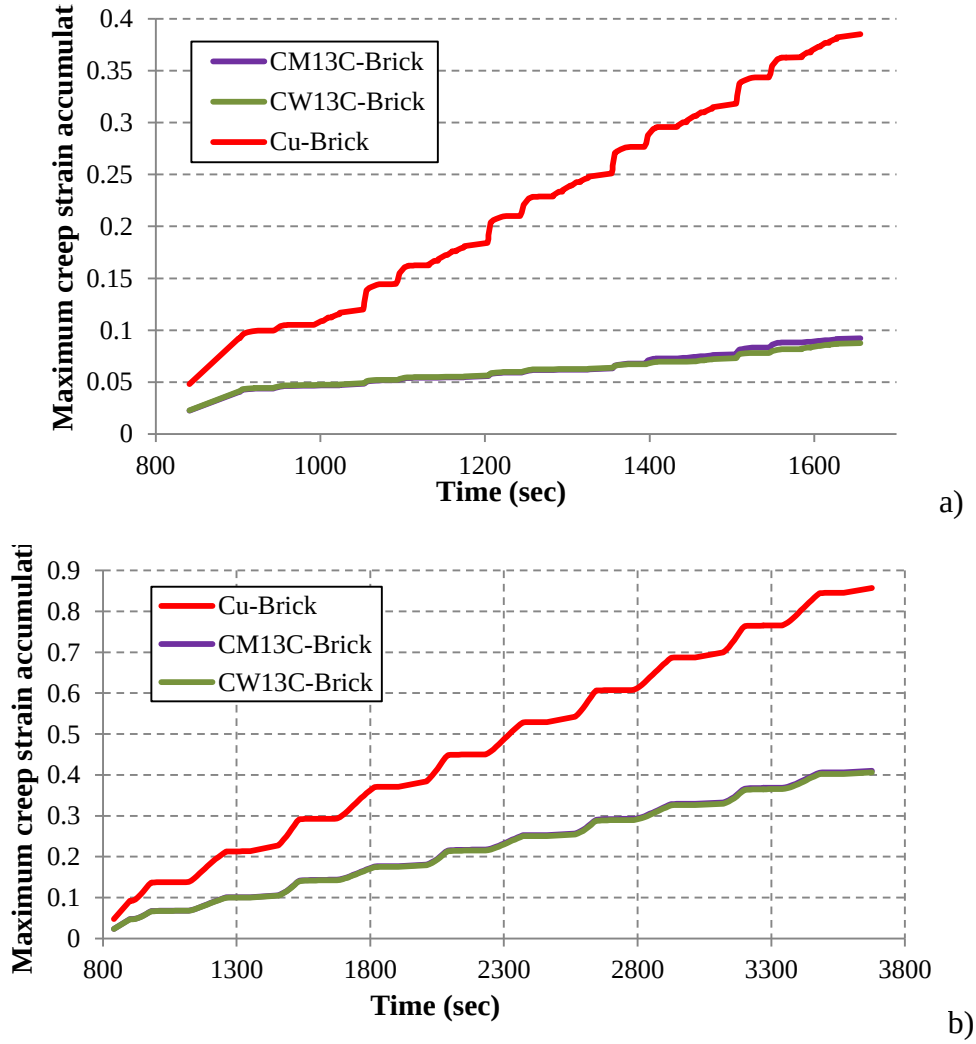


Fig.5.25 Comparison of the evolutions of maximum creep strain accumulations in the solder joints for the three design cases; a) five cycles of mission profile; and b) five thermal cycles

The relevant maximum stresses in the AlN tiles of the DBC substrates are also slightly lower than or similar to those using the CMC/CWC composite cylinder bumps. Therefore, the results from the thermomechanical simulation and thermal cycling experiment verify that the selection of CMC brick bumps in the stacked assembly can significantly improve the thermomechanical reliability of both solder joints and DBC substrates when compared with solid and hollow copper cylinders.

5.1.2 Electromagnetic modelling of bi-directional switch

Modelling electromagnetic interactions for interconnect has become an issue of great interest for integrated circuit design in recent years. The use of double-sided cooling power modules is noticeably interesting due to their inherent thermal capabilities. Apart from this interesting heat transfer solution as described in the thermal characterisation section of this work, the double-sided technology and related interconnection techniques allow a great reduction of stray inductances but, at the same time, increase capacitive couplings which are not the main targets of this work. The design of such power modules must therefore account for electromagnetic characterization.

In a conventional power module described in Chapter 2, the IGBTs and diodes are placed next to each other interconnected by thin and long aluminium wires. Such interconnection suffers with the parasitic inductances and results poor electromagnetic performance. Therefore, removal of wire bonding, for instance, as well as the compactness of the module dramatically reduces the overall stray inductance. For high performance power circuit packaging and integration, there are many cases where accurate estimates of the coupling inductances of complicated three dimensional structures are important for

determining the performance and functionality of the converter. The process of inductive interaction between conductors carrying currents can be decomposed into three different factors (Ampere's law, Faraday's law and potential difference across the conductor) which take place simultaneously [80] [81]. The representative figure for these three effects is depicted in Fig.5.26. In the case of loop 1, current flowing through the conductor and time varying electric field create magnetic field. This relationship between current density, the electric field and the resulting magnetic field density is known as Ampere's law (Eq.5.1).

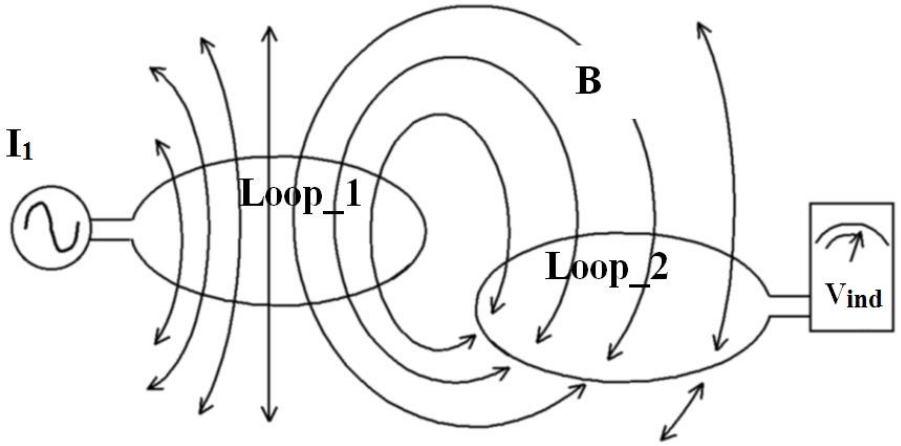


Fig.5.26 Magnetic field created by current carrying conductor in loop 1 and induced voltage in loop 2

$$\vec{\nabla} \times \vec{B} = \mu\vec{j} + \mu\varepsilon\frac{d\vec{E}}{dt} \qquad \text{(Eq.5.1)}$$

$$\oint_{edges(S)} \vec{B} \,.\, d\vec{l} = \mu \int_S \left(\vec{j} + \varepsilon\frac{d\vec{E}}{dt}\right).d\vec{S} \qquad \text{(Eq.5.2)}$$

Where μ - *Magnetic permeability*
ε - *Electric permittivity*
B - *Magnetic field density*

The first term on the right hand side of Eq. 5.1 represents the contribution of the current density to the magnetic field on the left hand side. The curl operator on the left hand side causes the resulting magnetic field to be enveloped around the existing current flow patterns as shown in Fig.5.26. The integral form,

which can be derived from (Eq.5.1) via Stokes' Law, is as in Eq.5.2. The second term ($\varepsilon \frac{d\vec{E}}{dt}$) in the right side of Eq.5.2 is referred to the displacement current density. Such current has a dimension of a current density and represents the alternating current flowing between two conductors due to their capacitive coupling. However this current considered to be negligible since the magnetic field created by the currents flowing within the conductors is far more than the magnetic field created by the displacement current (*i.e.* $\mu >> \mu.\varepsilon$).

As from loop 2, the varying magnetic fields created by the Ampere's law create induced electric fields in the loop (Eq.5.3). Such phenomenon is called Faraday's law. These induced electric fields exert forces upon the electrons in the conductors and causes voltage drops from which the resistance, self and mutual inductance could be extracted.

$$\vec{\nabla} \times \vec{E} = -\frac{\partial B}{\partial t} \qquad \text{(Eq.5.3)}$$

$$V_{ind} = -\oint \vec{E}_{ind} . d\vec{l} \qquad \text{(Eq.5.4)}$$

Where E *-Magnetic field intensity*
E_{ind} *-Induced electric field*
V_{ind} *-Induced voltage*

In recent years much effort has been devoted to the fast and accurate computation of interconnect models directly from Maxwell's equations. The aim of parasitic interconnects extraction for a set of conductors is to determine the relation between the currents and the voltages at the terminals of the conductors. Several integral equation-based approaches have been used to drive the parasitic associated with a given package or interconnect structure.

Building a power module and verifying the proposed concept through the entire module is extremely expensive and time consuming. Therefore, this

process has been simplified using computer aided program called FASTHENRY which computes the parasitic elements taking magneto-quasi-static assumption where the displacement current is negligible everywhere, and discretises the problem into a mesh of conductors each carrying current with uniform distribution [82]. The model shown in Fig.5.28 uses a copper conducting material being set at an electrical conductivity of 59600 S/mm. As from the model, the path through the chips, solder paste and copper bumps considered as two 10×10×2mm filaments cubes connected as a block. Two blocks are designed to form a bi-directional switch between two properly designed copper layers.

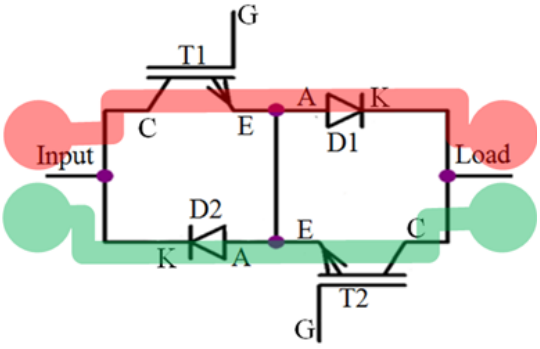


Fig.5.27 Schematic and measuring path of bi-directional switch

Two simulations as in Fig.5.28 and 5.29 were carried out to compare the influence of the bump interconnection using the same dimension. Fig.5.28 shows the layout corresponding to the bi-directional switch model with bump interconnection. One bump is used to extract the current commutation loop inductance and resistance where the bump refers to one IGBT and diode as shown in the schematic diagram (see the coloured paths in Fig.5.27). The two dots in Fig.5.28 represent the input and load position where the loop extraction is taken place.

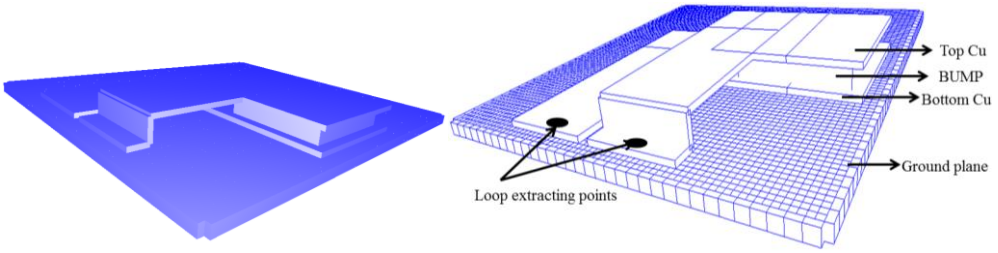


Fig.5.28 FastHenry model for bi-directional switch with bump

The input data is set to specify every conductor model as a sequence of rectilinear segments connected between nodes.

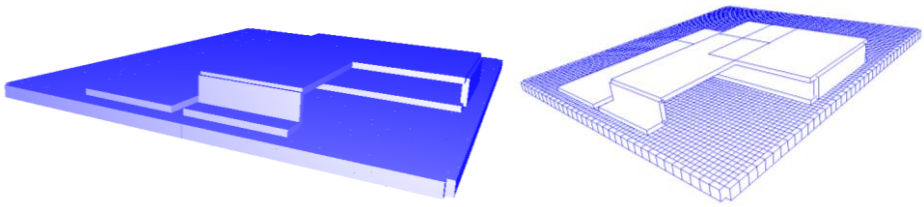


Fig.5.29 FastHenry model for bi-directional switch without bump

In both simulations, the copper layers are designed and assumed to be the paths where the current commutation flows through DBC, chips and bumps. This is done using number of filaments for the interconnection between the top and bottom substrate. As from the FASTHENRY software the ground plane is used for return current path where one of the loop extraction points short circuited to the ground plane.

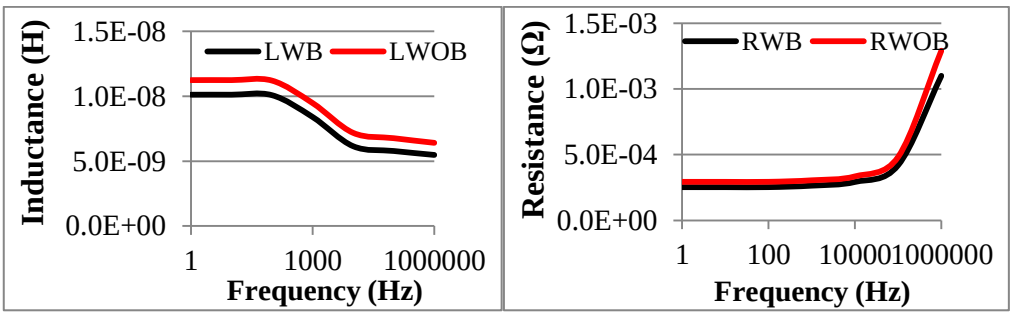


Fig.5.30 Extracted loop inductance and resistance of the proposed switch at wide range of frequencies using FASTHENRY (WB-with bump, WOB-without bump)

Measurement are extracted on a single path (Fig.5.27) while the rest of the paths (one bump connection) excluded so that it doesn't contribute to the

measuring path considering one IGBT and diode are not conducting. The results in the Fig.5.30 have been recorded in the form of complex number R+jL where R is resistance in ohms and L is inductance in Henry. It can be clearly seen from the result, both inductance and resistance values are reduced with the bump interconnection.

This can be attributed by the fact that the bump interconnection used more parallel filaments to connect the top copper layer to the bottom one. Therefore, in this particular simulation result, electro-magnetic characterisation of the assembly indicated very satisfactory values of equivalent stray inductance of around 6 nH. However, as in Chapter 5, the current commutation loop inductance for the conventional power module is 20-22nH.

5.2. Switch assembly

A stacked assembly concept of substrate-chip-bump-chip-substrate for the common emitter bi-directional switch has been constructed with the AlN-based substrate based on the latest generation Infineon Technologies 70um thin IGBTs and diodes, rated at 200A/600V. As from Fig.5.1, the IGBT die contains one gate pad at the centre surrounded by 8 emitter metallisation pads on top and a collector covers the whole surface at the backside whereas the diode is built with anode on top and cathode at the backside.

5.2.1. Chips, Substrates, and interconnection layout

The front sides of both the top and bottom DBC substrates shown in Fig.5.31 are used for attaching one IGBT and one diode and providing terminals for gate and emitter of the IGBT attached on the opposite substrate. The backsides of both substrates can be in contact with the primary cooling surfaces for achieving double-sided cooling.

The sizes of the top and bottom substrates are 26×34×1mm and 38×34×1mm of AlN ceramics with 0.3mm thick copper on both sides respectively. The bumps are used to provide all inputs, outputs and gate interconnects of the switch to be terminated on one substrate, and establish a strong mechanical support to the assembly. All the bonding and interconnects are soldered with Sn-3.5Ag solder alloy and 62Sn3.6Pb2Ag solder paste to eliminate the use of standard bond-wire packaging technology.

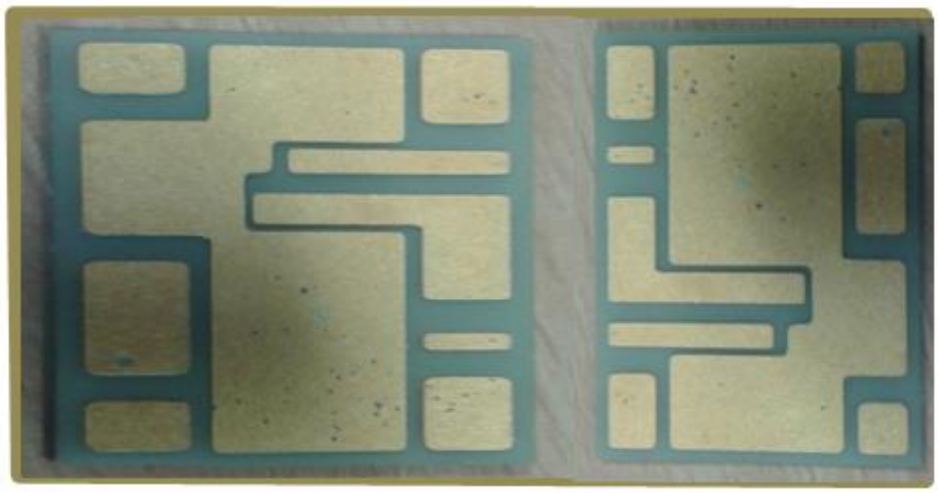


Fig.5.31 Bottom and top substrate layout for bi-directional switch

5.2.2. Switch prototype development

The constructing of assembly is very challenging and a number of things need to be considered before starting to solder the chips onto the substrate. The step is critical because it involves soldering and direct handling of the semiconductor devices like IGBTs and diodes. Fixtures (jigs, Appendix 3) are designed in accordance to the shape and position of the chips to facilitate the process by holding the chips and bumps not move around during soldering in conventional reflow oven. The soldering steps were taken into account that the first temperature of soldering process must not be higher than the second step. The soldering process inside the reflow oven was taken place using three

heating steps with three different time settings. Once the oven is preheated at a given temperature for some time, the module has to be heated up with a temperature higher than the preheating temperature. Then finally need to give some time to cool down.

5.2.3. Soldering process

Two direct bonded copper substrates as in Fig.5.31 were used to manufacture the bidirectional switch prototype. In this particular prototype, soldering process has been taken place at three different locations such as:

- At the chip and the ceramic substrate,
- At the interface between chips and the power bumps, and
- At the bumps and ceramic substrate

Two different solder joints have been processed in a single prototype of bi-directional switch using two different soldering alloys with two melting temperatures been employed. Indeed, the chip-to-substrate joint processed first which should not be able to melt when the chip-to-bumps joint is processed.

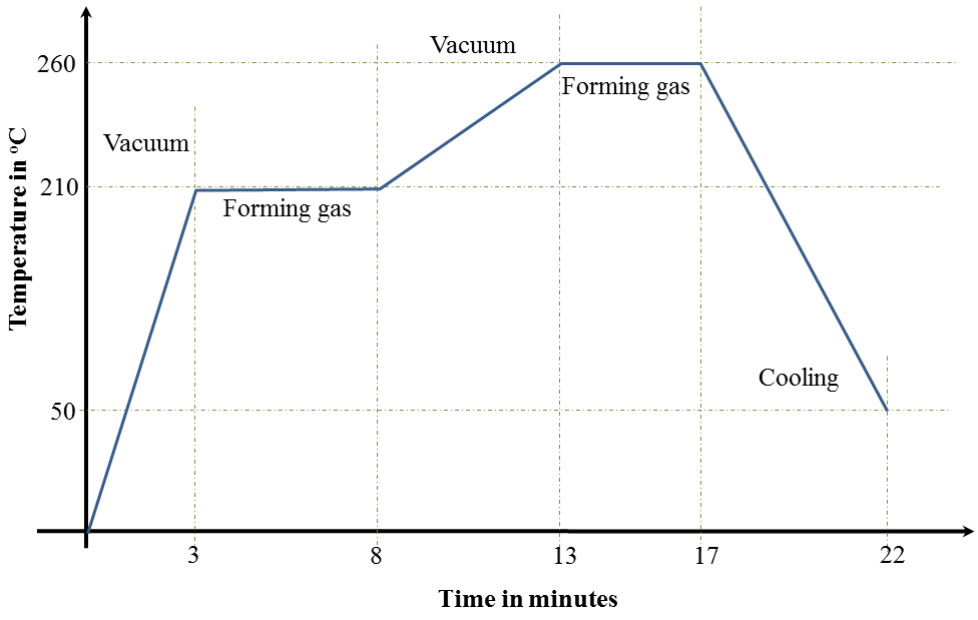


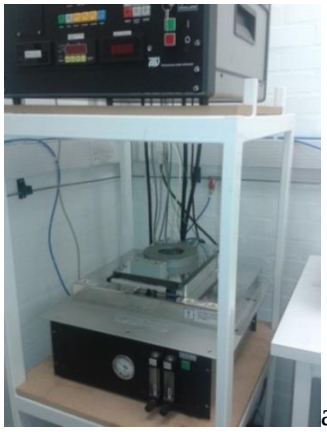
Fig.5.32 Temperature profile representative of the reflow process

Solder pastes: These types of solder paste consist in a mixture between the alloy, as a powder and organics that provides mechanical carriage to the paste, and a flux, which cleans the surfaces to be soldered and enhances their wettability toward the soldering alloy.

Solder preforms: These are thin foils of the soldering alloy without any additives applied onto the surfaces to be soldered.

5.2.3.1. First step – Die attach solder

The solder used to bond the chips onto the substrate is solder preform Sn3.5Ag and 96.4Sn3.6Ag solder paste is used for bump interconnections. The first step soldering process is taken as in Fig.5.32 reflow profile. First the transistor and diode chips are soldered underside (Collector and cathode) onto a direct bonded copper substrate with a 100µm thick Sn-3.5Ag pre-form foil that is employed in a flux-less reflow soldering process. Fig.5.33 (a) is the flux-less reflow soldering process set up that includes vacuum oven, vacuum pump and control unit. The reflow process is programmed such that the sample passes through five consecutive steps using forming gas in conjunction with vacuum down to pressure level of 5mbar. The first step is to set the preheating temperature to 210 ^{o}C for 3 minutes while vacuum is turned ON. Here vacuum is used which sufficiently prevents oxidation through low residual gas pressure and partially removes oxides and prevent trapped gas bubbles (voids) within the solder joint. Then the forming gas is turned ON for 5 minutes and at this stage the vacuum is switched OFF. This gas penetrates all surface layers and scrubs, cleans, and prepares the surfaces for soldering reflow without the use of flux.


a)


b)

Fig.5.33 Flux less reflow oven, a) High temperature oven, b)

The same procedure is followed for 5 minutes of vacuum at the ramp increase of temperature to 260 ^{o}C and 4 minutes of forming gas at constant temperature of 260 ^{o}C. Finally, the sample is set to cool down for 5 minutes.

5.2.3.2. Second step – soldering bumps

At this instant, the substrate is moved to the next step where the bumps are placed onto the chips and mechanical supports using 96.4Sn3.6Ag solder paste. Two types of bumps are used for the interconnection such as copper cylinder and copper-molybdenum-copper. The detail dimensions and sizes are clearly illustrated in the beginning of this Chapter. The 96.4Sn3.6Ag solder paste has sufficient tension to hold the components in place, but care should be taken not to knock the substrate at this stage otherwise the components may move or fall off. In this case the masks will help to hold and be soldered within a few minutes of being placed. Then the sample is placed into the high temperature oven, Fig.5.33 (b), while the temperature is set to 260 ^{o}C and an external timer is used to set the heating time for 5minutes. Fig.5.34 shows the dies and interconnection bumps properly soldered on to the given DBC substrates.

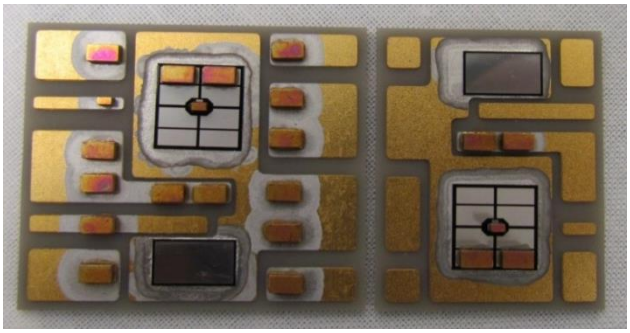


Fig.5.34 Bottom and top substrate of the bi-directional switch with bump interconnection

5.2.3.3. Third step - sandwich

This is the final stage where the two substrates are sandwiched together and soldered using 96.4Sn3.6Ag solder paste. First the wider (bottom) substrate is placed into the properly designed mask where the gate resistor and all interconnections are going to be soldered. Then the top substrate is carefully sandwiched on top of the soldered bumps of the bottom substrate using 96.4Sn3.6Ag solder paste in between. The mask is designed for taking care of position of the substrate when sandwiched so that no short circuit could be created.

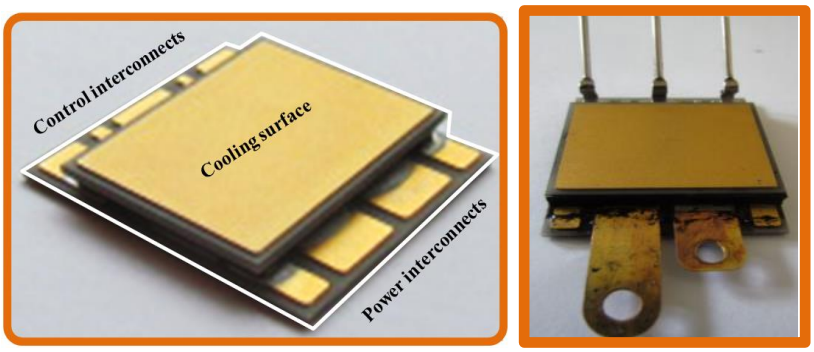


Fig.5.35 Bi-directional switch prototype

Two properly designed and cut connectors are placed on the bottom substrate of the two middle flat copper layers with 96.4Sn3.6Ag solder as shown in Fig.5.35. Finally three pins for two gates and one common emitter leg are placed through the pin holder.

Once all the interconnection and substrate placed, the final sample is inserted in to the high temperature oven at 250 ^{o}C for 5 minutes.

Table 5.8 Types of material used in the prototype

Material	Function
AlN-DBC	Substrate
96.4Sn3.6Ag	Solder paste
Sn-3.5Ag	Solder Preform foil
Cylindrical copper bumps	Vertical interconnects
Cu-Mo-Cu bumps	Vertical interconnects
IGBTs and Diodes	Switches
10Ω SMD resistor (1206 footprint)	Gate resistor

Fig.5.35 shows the final bond wire-less bi-directional switch prototype where the power and control signals are separated for minimising unusual signal interaction. The packaging materials used are listed in Table 5.8. Two prototypes of those different bump types (cylindrical copper bump and CMC) were built and the reliability performance of each model is compared.

5.3. Insulation and partial discharge

5.3.1. Insulation

Moisture induced corrosion has an activation energy of about 1eV for silicon chips. This means that for every 9^{0}C, the rate of reaction will double and it greatly affects the service lifetime of the power module [5]. In order to protect the power device encapsulant material is dispensed into the module, which can completely shield the chips and interconnections from influences of its surroundings, such as humidity, dust, chemical, and mechanical damage. IPC-HDBK-830 is the industry standard guideline for design, selection application of conformal coatings.

The guideline is actually for surface-mount products but many of the discussion are also applicable to use on power module. Selection of the encapsulation material is discussed in detail in [5] and some of the criteria are listed below.

- High purity for direct contact with semiconductor chip
- Good thermal properties
- High electrical isolation
- Manufacturing and environmental friendliness
- Cost effectiveness and etc.

Mostly Silicone gel is preferred from several classes of coatings such as Silicone, Silicon-nitride, Acrylic, Polyurethane, and Epoxy. Since silicone gels are very resilient (able to recover from deformation), they can absorb thermo-mechanical stress better than any other materials. They are ideal for the encapsulation of electrical systems such as electronic assemblies due to their outstanding features like high purity, high and low temperature performance, low toxicity and thermal endurance. Their physical and technical properties remain unchanged between -50 °C to +200 °C, even after several thousand hours in service. In short, most silicone gels are usually more durable than the devices or assemblies that they encapsulate [83][84].

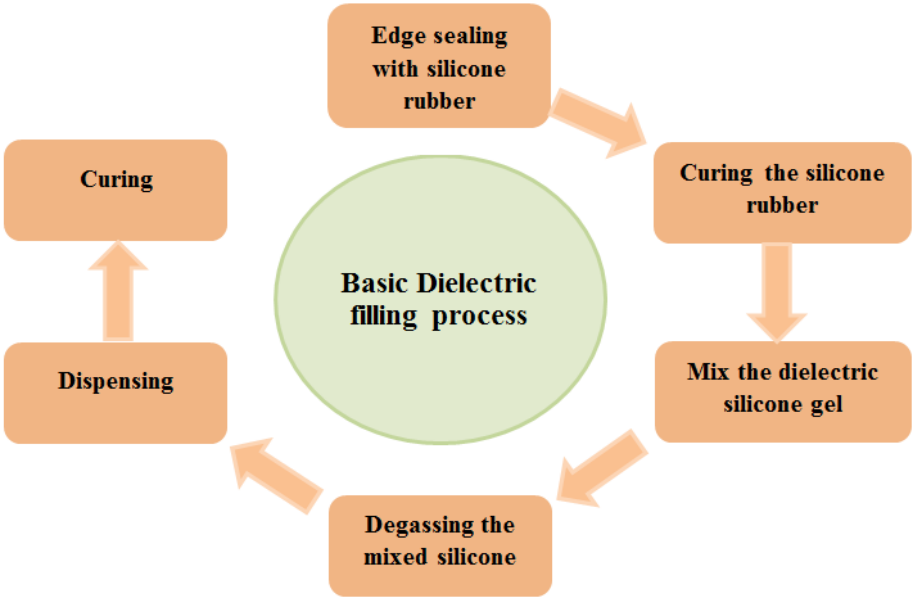


Fig.5.36 Silicone dielectric filling process

Fig.5.36 is the general process of filling silicone dielectric in a power module. Two types of silicone were used in this process; thick silicone gel to seal the edges of the sample and a dielectric silicone gel for filling. The process needs some preparation before dispensing the gel into the given sample. The sample has to be either sealed with some sort of paste/glue or make a mould so that the sample could be filled. The first method is chosen for this work as it is easier and faster.

In order to create the borders with silicone glue, attention is paid to the cleanliness of the sample surfaces. Therefore, the sample has been cleaned using "LOCTITE, 7063" high solvent power cleaner to remove grease, lubrication fluid or unnecessary dirt when handling the sample Once the sample is cleaned, then three edges of the sample are properly and carefully covered using SEMICOSIL-987 silicone glue and analogue liquid dispenser so that the dielectric can be dispensed through the remaining side as shown in Fig.5.37.

Such type of glue has thixotropic behaviour which means that the glue can be returned to semisolid state when it is shaken. This behaviour helps to build a layer of glue one on top of the other to cover up the edges without penetrating into the sample. The sealing area was kept free of any openings which may result in a leakage when dispensing the silicone dielectric gel of very low viscosity. The sample is then cured inside the oven heated at the temperature of 100^0C for about an hour. The glue can also stand for about 17KV/mm.

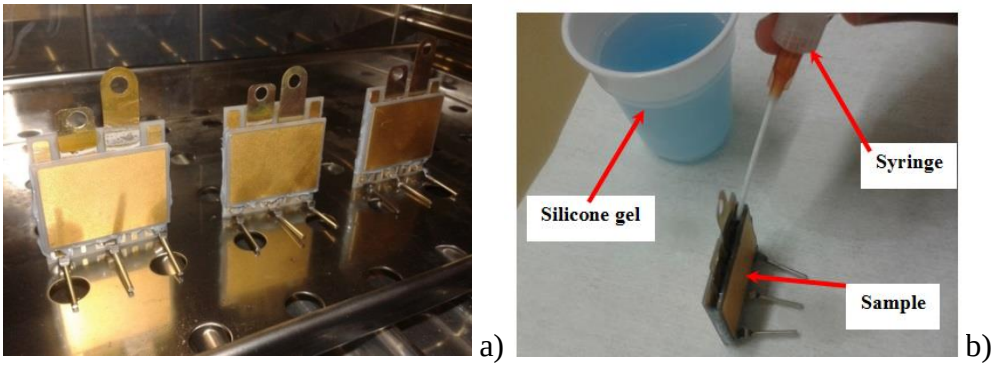


Fig.5.37 Sample sealed with silicone glue at three of its edges and ready for curing

There are several types of curing mechanisms involved in the field of silicone sealant such as high temperature vulcanising (HTV) and room temperature vulcanising (RTV). In both mechanisms, silicone rubber is made either from two component systems or one. RTV cures at room temperature to form a flexible strong bond to the substrate and HTV cures at elevated temperature. When using HTV, the sample is placed at high temperature for curing which makes it faster as compared to the RTV. However, if the sample has some fluxes around the solder joints, for example in this particular sample (Fig.5.37), it is difficult to guaranty that air is not trapped under the fluxes due to the change in temperature. Therefore, in this particular experiment a 2-part, RTV-2 silicone rubber (component A and B of WACKER SilGel 612) [Appendix 2], and 1:1 ratio mix silicone gel is used for dielectric dispensing that vulcanises at

the room temperature. Component B of WACKER SilGel® 612 contains the platinum catalyst (causes a fast chemical reaction to occur without permanent change in the reaction) whereas component A contains cross-linker. Cross-linking is a chemical reaction between two polymer (group of molecules) chains. This means that the platinum catalyst may cause gelling of the component containing the cross-linker which joins the two components together and cannot slide away from each other when they are stretched [85]. Here a stirrer is used for handling the platinum containing component and cross-linker to be thoroughly mixed. During mixing of the two components, some air bubbles were observed and a vacuum oven at room temperature is used to eliminate those air bubbles with 200mbar pressure at a room temperature until the bubbles are disappeared.

When using dispensable products, factors such as pump equipment, mating surfaces, tolerance stack up, and physical application of the material have to be considered. There are many options for dispensing equipment, ranging from manual syringes, to high volume automated dispensing systems. The choice of the proper equipment will depend on several factors, including volume, labour/equipment cost, precision requirements, and material type to be dispensed [86]. For this experiment a manual syringe is used for simplicity and it is assumed that certain factors might affect the quality and throughput of the material. These factors may include needle height, dispensing pattern and speed, needle diameter, substrate surface finish etc. Fig.5.37 (b) shows how the silicone gel is manually inserted using a syringe. The sample was filled with silicone gel up to 2/3 of the volume of the sample in order to protect the surrounding from leakage when the vacuum pump is in operation. However

during dispensing, it is clear that small bubbles or voids may form inside the sample, which represents in-homogeneities on the gel filling normally closer to the edges of the interconnection region such as die, solder, bump and substrate.

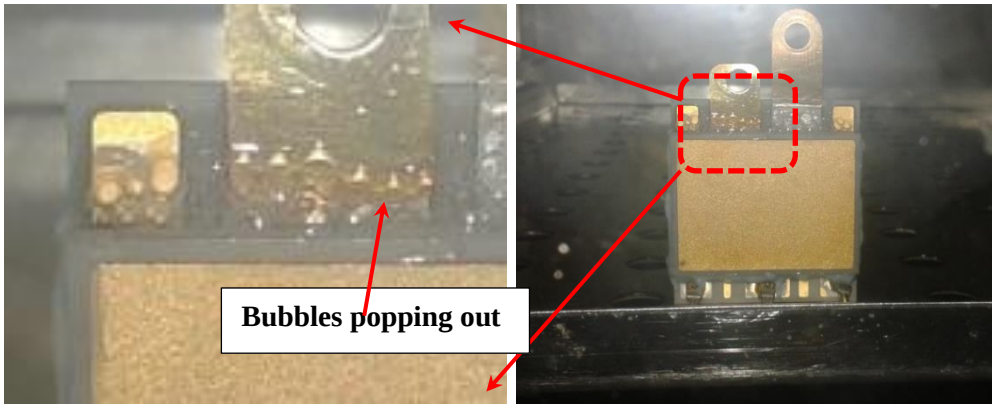


Fig.5.38 degassing process in the vacuum oven

The sample is subjected to a vacuum in a vacuum drying oven as depicted in Fig.5.38. The conditions were 20°C and 10mBar pressure, applied for one hour. Repetitive action is applied in visual inspection with the vacuum being interrupted when bubbles popped out from the sample as clearly shown in the zoomed-in view of Fig.5.38 and been removed by enabling the air out. Thanks to their good self-healing properties, it can be touch up and repair the silicone gel without pre-treatment by applying more of the liquid silicone gel to the already cured gel surface. Here care need to be taken of using the vacuum for a long time as the silicone might change its characteristics and solidify. The whole process from dispensing the silicone gel, through the treatment in the vacuum drying oven must be completed within one hour to prevent uncontrolled partial curing of the gel.

5.3.2. Partial discharges test

Partial discharges are small electrical sparks that occur within the insulation of medium and high voltage electrical power module. Each discrete discharge is

the result of an electrical breakdown of an air pocket within the insulation. These discharges erode insulation and eventually result in insulation failure.

The portable AC high voltage partial discharge tester (PHENIX – Technologies) was first calibrated at 200p Coulomb (23dB) for each sample throughout the test. The system is equipped with advanced digital metering, and control along with protection devices which are easy to use and provide safety operating system. The test was carried out with (100-600) V/50Hz ac voltage connected across collector legs while the gates of the two IGBTs were shorted and hence the switches remain turned OFF allowing no current to flow through either of IGBTs or freewheeling diodes as depicted in Fig.5.39.

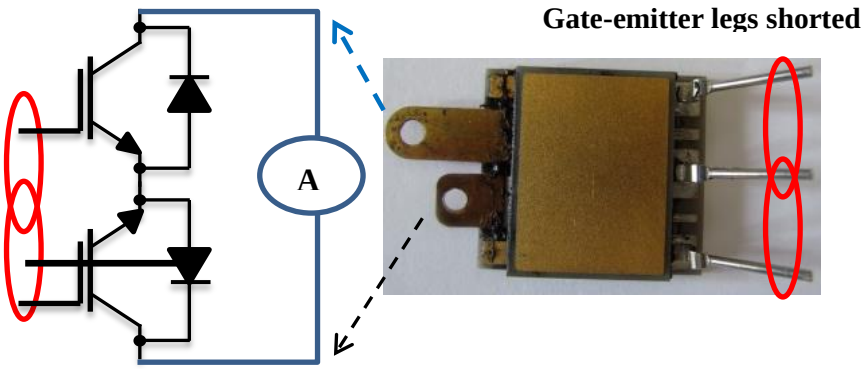


Fig.5.39 Schematic of the experimental setup

The maximum voltage used is 600V which is the nominal rated voltage of the devices. Fig.5.40 illustrates the partial discharge test setup under AC voltage. During calibration and testing the sample was inserted into the container filled with FC-72 Fluorinert electronic liquid which has high dielectric strength up to 35000 volts across a 0.254 cm gap. Then the partial discharge of the silicone gel is measured using partial discharge (PD) control unit and partial discharge meter. Five samples were tested and the corresponding results are shown in Fig.5.40.

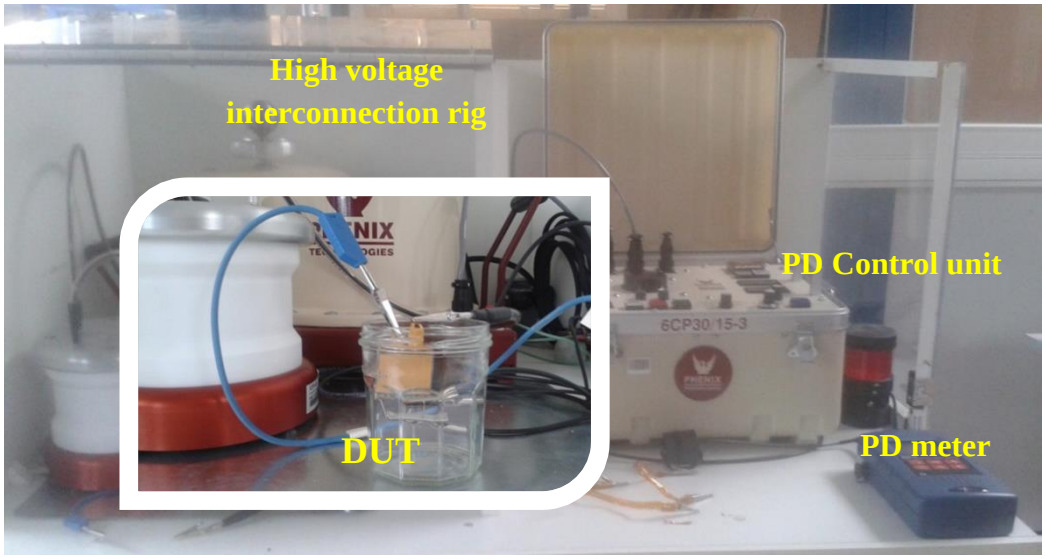


Fig.5.40 Partial discharge experimental setup

As from the test result shown in Fig.5.41, the sample has totally no partial discharge up until 500V. And this is somehow a promising result if the device is meant to be operated below the rated voltage. Past this voltage however, the partial discharge increased rapidly even though it is in few mili-amps. This experiment verifies that the silicone gel filled in the sample is less affected by the voids.

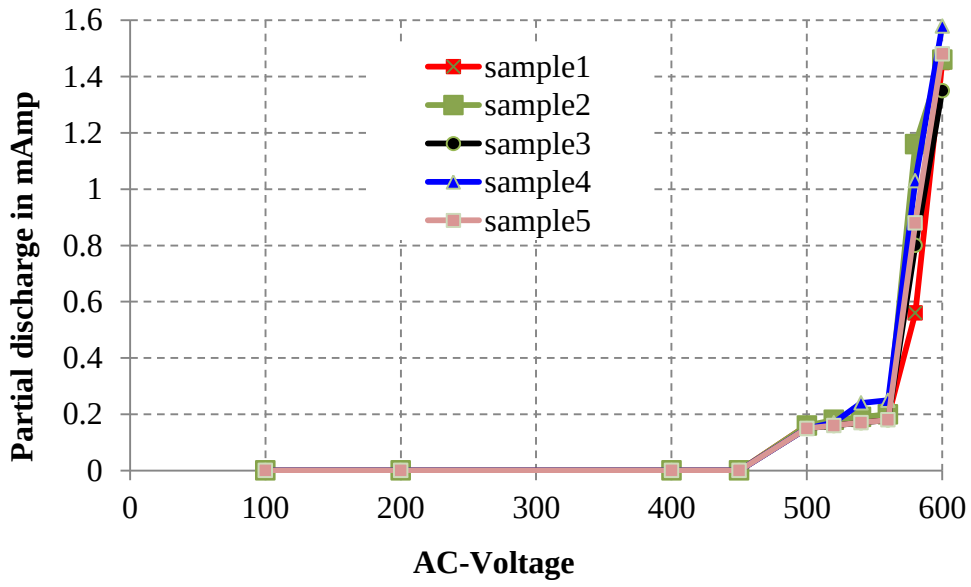


Fig.5.41 Partial discharge test results

5.4. Reliability characterisation

Defining the failure criteria is the necessary approach to describe the lifetime of a power module. For example, it has been stated in [87] that the failure in bus-bars is defined when 50% of the area of the solder has delaminated. Whereas for the chip and the substrate, solder failure is defined when 20% of the solder area has delaminated. The failure criterion for the wire bond is when a 90% reduction in shear strength is observed. It should be noted that power modules are usually filled with silicone gel and epoxy resin and as the temperature changes they expand and contract to push the top of the case up and down. This movement causes cyclic deformation and damage to the solder joints. Based on the findings in [73] and discussion in Chapter 5, the simulation results for such novel bump interconnection scheme indicate that the mechanical stress at the solder layer interface between bump-substrate and bump-chips were very critical and severe.

However, the most relevant stress level was recorded at the die attach interface of both the top and bottom dies. This most critical and weakest spot causes a change in on-state resistance. In an experiment, such resistance is detectable with an accurate highly resolved measurement of the device on-state characteristic. Therefore, a testing method was established based on continuous monitoring of the IGBT and Diode on-state voltage under fixed bias conditions and during passive thermal cycling. For the switches of Fig.5.35, preliminary reliability tests for technology validation have been carried out.

Two switches made of copper hollow cylinder and CM13C bumps were placed in a controllable thermal chamber and a four point electrical interconnection

scheme with copper terminals was implemented to isolate the influence of cables or terminals on the measurement and hence minimize the potential of intermetallic voltage drop as shown in Fig.5.42. A K-type thermocouple was connected on the top substrate to monitor the temperature.

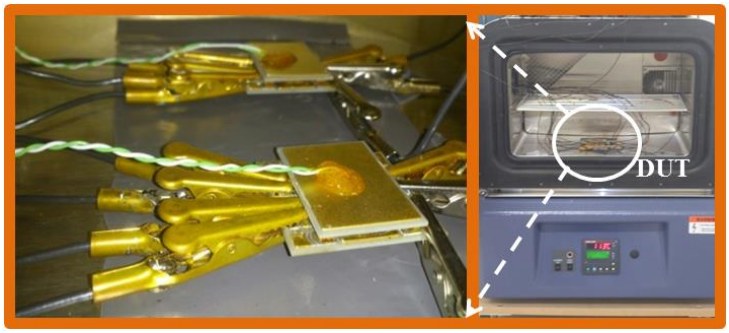


Fig.5.42 Detail of interconnection in the thermal chamber for the reliability tests

Here, to reduce testing time the harshest temperature cycle was applied, shown in Fig.5.43 which corresponds to a ΔT=210 K, from -55 to +150 ºC.

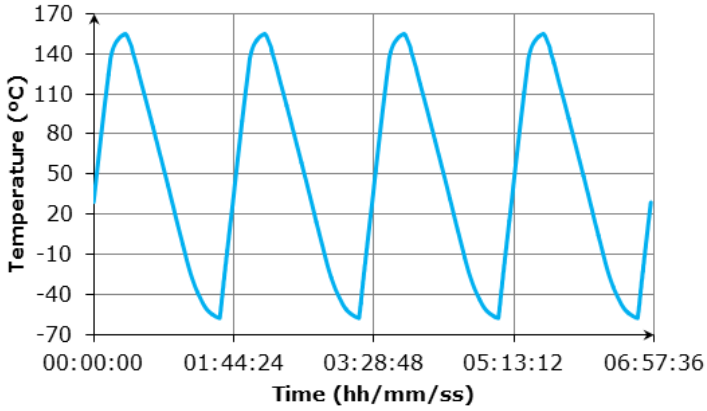


Fig.5.43 Passive thermal cycling for preliminary reliability validation

In these particular tests, the variation of the IGBT on-state voltage for a fixed on-state current and temperature was used as the monitor of interconnects degradation [88]. The two main factors contribute to the rapid increase of on-state voltage in the end-of-life period are degradation of the solder layer underneath chip and bumps and peeling-off of the copper tracks from the ceramic. The number of cycles at which these effects become detrimental

depends on the type and quality of the materials involved in the assembly. For example the quality of the solder joint in the die attach is one of them where the voids are dependent on the soldering process used.

Fig.5.44 is captured with X-ray camera for two different solder joint beneath one of the diodes in the assembly. These two samples were built such that a solder is first soldered onto the substrate without die inside conventional high temperature oven then the diode is placed on top to be soldered using reflow oven. The second one was soldered inside the high temperature oven while the solder was attached to the die. As it can be clearly seen, a single step method is more vulnerable than the second step having a lot more and bigger voids.

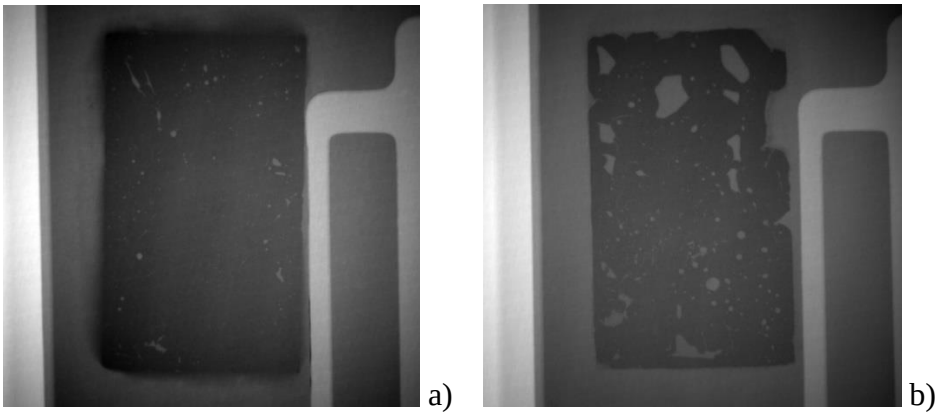


Fig.5.44 Solder die attach; two step solder joint, a) and one step solder joint, b)

Initially, the failure criterion was set at 10% variation of the on-state resistance. As from the test results summarized in Fig.5.45, a 10% increase in V_IGBT was captured after around 265 thermal cycles for the sample CM13C and around 100 cycles for the cylindrical hollow bump. As stated earlier, a 10% increase in V_IGBT can be used as an indicator of the failure of the solder joints in the conductive path, due to the formation of rapid growth of fatigue cracks. For standard power modules, extrapolation for lifetime estimation based on Coffin-Manson law would give roughly at least a factor 2 increase for

reduction of 10K in the ΔT (at least over common temperature ranges). In this case, for a more realistic operational ΔT of -55 to +25^{0}C (70K, e.g. avionics), the lifetime estimate would be 280 times higher, that is around 74,200 cycles. Fig.5.45 shows that end-of-life behaviour is characterised just like in the case of conventional bond-wire interconnections by a step increase of on-state resistance [89]. Therefore, as from the result in Fig.5.45, CM13C bump can reduce creep accumulation in the solder joint for connecting the bumps, hence improving long term reliability of the switch.

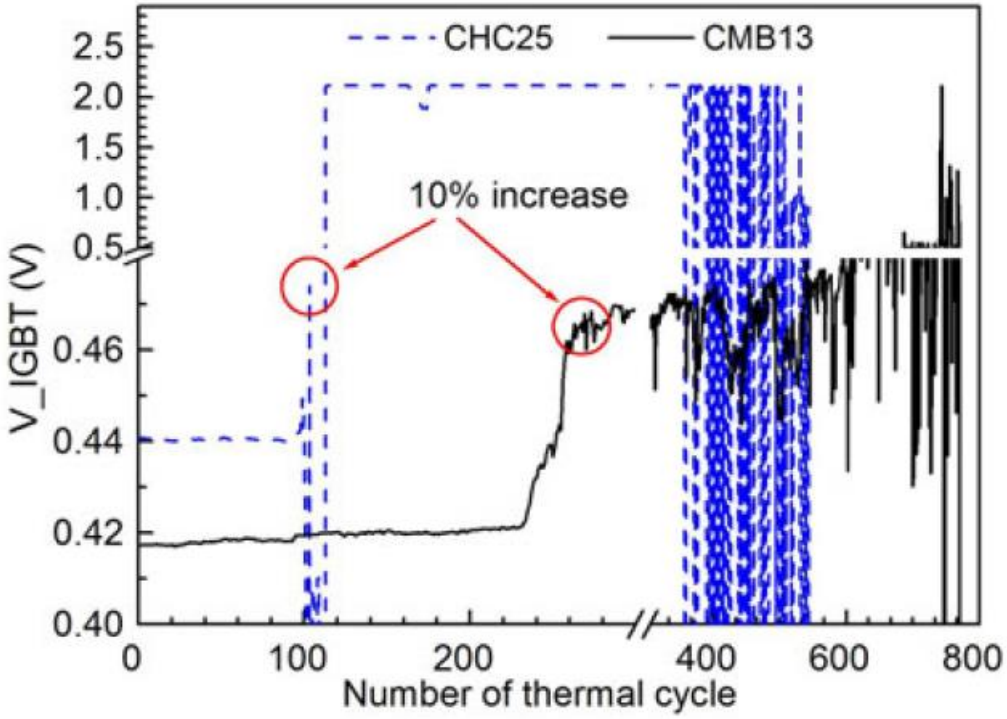


Fig.5.45 Experimental results of lifetime estimate with the proposed methodology on the CMC and copper hollow cylinder bump switch [57]

According to the past publications on wire-bonded modules, it indicates that the most suitable monitor of end of life may be a differential analysis of the change in resistance over number of cycles, since a noticeable change of slope is visible when entering the end of life region.

Without entering to the details of the failure analysis, it is finally worth noting that the failed switch exhibited evidence of the copper layer partially peeling off from the top substrate, of the kind visible in Fig.5.46, this believed to have contributed to the observed end-of-life behaviour and the eventual switch failure.

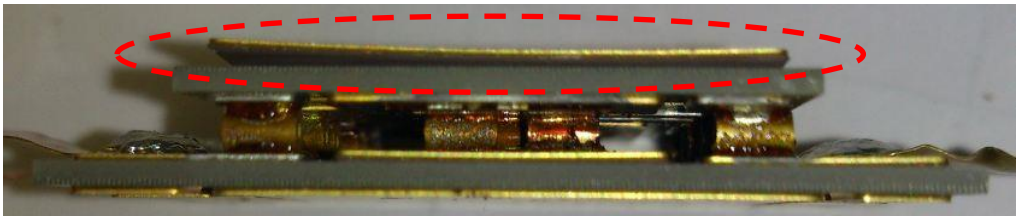


Fig.5.46 Detail of DBC track peeling-off after thermal cycling

5.5. Matrix converter assembly and cooling system

Referring to the schematic diagram of 3-to-3 matrix converter shown in Fig.4.10, at least three switches as per Fig.5.34 are required to build, a three-to-one phase matrix converter. The proposed module is constructed with three bi-directional switches in which three inputs (three holes located equilaterally, Fig.5.47) are interconnected symmetrically with copper bars through three embedded input capacitors (small rectangular grey block between three L-shape copper bars). A common output terminal (load side) and three input terminals (input side) are designed to be connected only by means of bolts and screws (no soldering) as shown in Fig.5.47. The load at the centre is electrically isolated from the three inputs. This is done using three rectangular blocks of copper which are placed on each phase to allow gap between the load and phases (Fig.5.48). As from Fig.5.48, properly shaped interconnect enables to enclose phase-to-phase high-frequency filtering capacitors (here, a total of 2.2 uF ceramic capacitance is introduced between the phases; the value can be easily increased by stacking the capacitors one on top of the other.

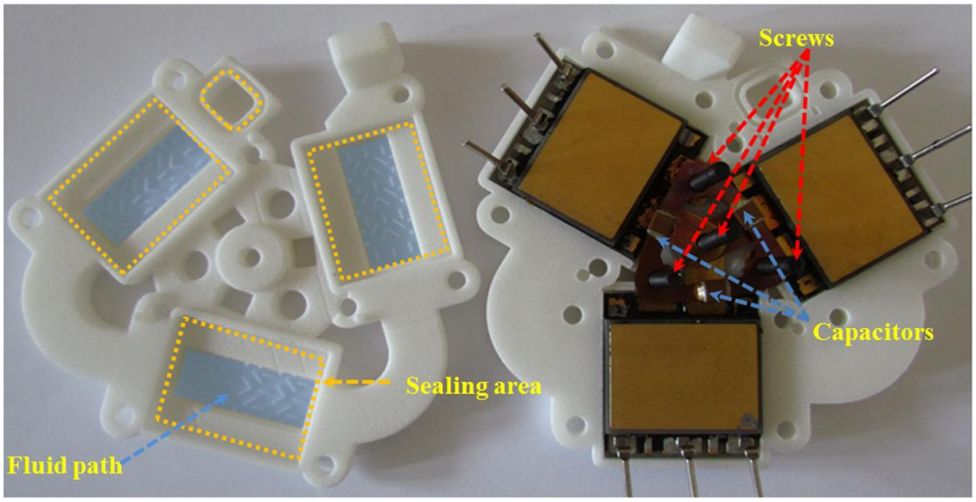


Fig.5.47 Internal view of the assembly and the interconnection setup

Here the power and gate signals are also planned to be separated in such a way that the interconnection located at either side of the assembly. Each bi-directional switch is cooled directly through the substrate unlikely the single sided module discussed in Chapter 2 has a base plate beneath the substrate.

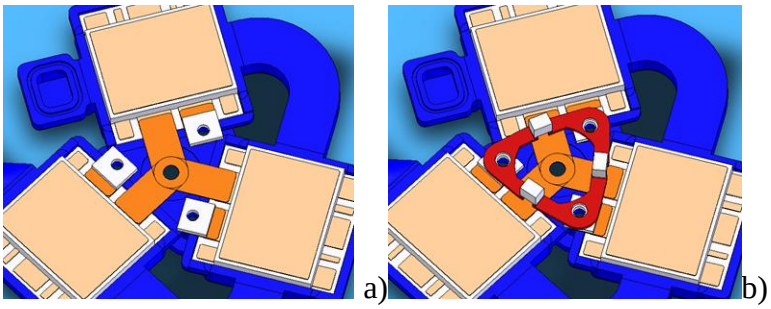


Fig.5.48 gap between load and phase, a) input filter interconnects module, b)

Avoiding this baseplate will further reduce the thermal resistances of the module. Moreover, the switches are enclosed within a forced liquid based cooler that can cool top and bottom side of the switch. The module design is fully symmetrical, so that each switch sees identical electro-magnetic and electro-thermal conditions.

The power module is enclosed with polyamide 12 (LS-PA12GF), a very well-known plastic material with excellent strength and stiffness. It is made of two parts which cover the bottom and top surfaces of the three bi-directional

switches along with holding all interconnections parts together. First, both plastics were thoroughly cleaned to ensure that satisfactory adhesion to the plastics is achieved and sprayed with a flexible transparent silicone resin conformal coating which is designed for the protection of environmental conditions (e.g. water resists). Then the plastics were left for a day to allow the solvent system to fully evaporate and cure at a room temperature. Once the plastics fully dried, a silicone rubber sealant is used around the edges, dotted lines shown in Fig.5.47, to seal the three bi-directional switches.

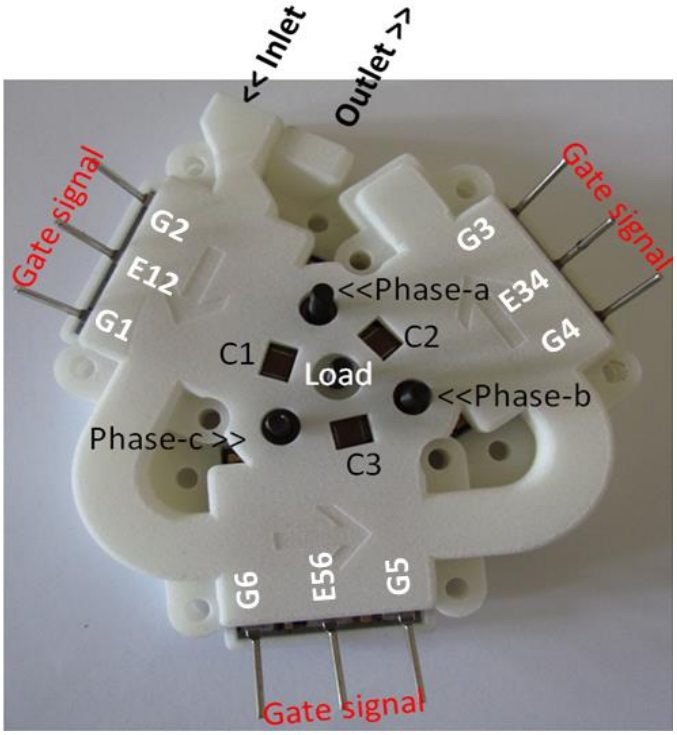


Fig.5.49 Three phase to single phase Matrix converter assembly with water cooler; where G1-G6 are six IGBT gate connections and E12, E34 and E56 are common emitter connections for each bi-directional switch

Finally, the module is firmly fixed with nine other screws and left to dry for a day. Fig.5.49 shows the closed module: the power and gate signals are completely separated and the top-side of the enclosure (the cooler) can be used to mount gate drivers and additional filter elements and control to deliver a self-contained unit.

The water cooling system flow path inside the power module is designed to directly target to the hot spot (light blue area) shown in Fig.5.47 where the power devices are located. The flow of liquid will start from the inlet and goes to the top surface of each three switches; and once it passes the third switch it turns down and flows via the bottom side of each switch to get to the outlet. Although this initial cooler design with a single inlet and outlet, cannot guarantee exactly symmetrical thermal conditions for the switches, 3D simulations carried out with established industrial computational fluid dynamic design tools (ANSYS Fluent), delivered an indication that the temperature gradient would be low enough to make it a viable easier solution for initial testing. In the simulations, the liquid flow rate is defined as inlet boundary condition with initial liquid temperature set at 300 K.

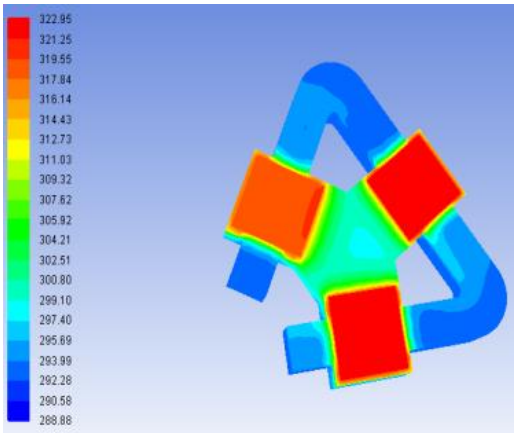


Fig.5.50 Heat transfer temperature contour (in degree Kelvin)

At the outlet, the external gauge pressure is set to zero. Thermal properties of the materials involved in the model have been assigned to evaluate the heat conduction through all solid bodies due to the fluid flow. For this simulation, a heat transfer coefficient of 5W/m^{2}K was used for each wall which is exposed to the air considered as a free convection. An evenly distributed heat flux of 10,000W/m^2 is used for top surface of each three silicon block. Here the silicon

blocks are assumed to be three bidirectional switches. A velocity of 0.08m/s (a flow rate of 0.3litre/minute) is used to the inlet while the outlet is fixed at zero pressure. This flow rate corresponds to the realistic heat transfer value between 500 - 5000 W/m^2k. Fig.5.50 shows the resulting temperature distribution. Although the cooler design is not fully symmetrical, this initial study ensured that the asymmetry is negligible under realistic operational conditions and the cooler design can easily be optimized.

5.6. Summary

Selection and switch design specification for power electronics packaging have been discussed with a detailed section to the material characterisation and cooling system of a power module. The construction of the bi-directional switch assembly is discussed with a detailed manufacturing process. The chapter also introduced the basic reliability characterisation of the switch which verifies that selection of the CMC/CWC bump type switch can significantly improve the thermo-mechanical reliability of solder joint. The detail insulation process of bi-directional switch is performed and five samples were prepared and the corresponding partial discharge experiments were carried out. Partial discharge test have shown somehow reasonable result that confirms the efficiency of the filling of silicone gel. However, a proper test procedure and equipment need to be used in order to conclude the performance of the filing of silicone gel.

Chapter 6:
System level demonstration

In this chapter, the functionality and performance of the proposed three-to-one matrix converter that is constructed with three bi-directional switches is presented. The chapter starts from the development of the test setup and show the experimental test results.

6.1. Matrix converter test setup development

Matrix converter is a direct AC-AC power converter which belongs to the group of the direct frequency converters. As it does not use any large inductors or dc link electrolytic capacitors it offers potential for higher power density and higher operating temperatures. In its simplest specification it consists of 9 bidirectional switches, which can connect any output phase to any input phase as shown in Fig.4.13. By a suitable modulation the matrix converter produces a three-phase output voltage system with an adjustable frequency and amplitude, whereby the maximum voltage transfer ratio factor is limited to 0.86 [67].

Fig.6.1 shows the general experimental test circuit schematic of a bi-directional switch based three-to-one phase matrix-converter containing the popular snubber configuration along with control platform. The fully assembled

module was subjected to some preliminary functional tests. As proper filtering is not the main target to this project, the type of input filter developed in this work is the conventional first order LC filter assuming a low inductance value coming from the 3-phase AC supply (variac).

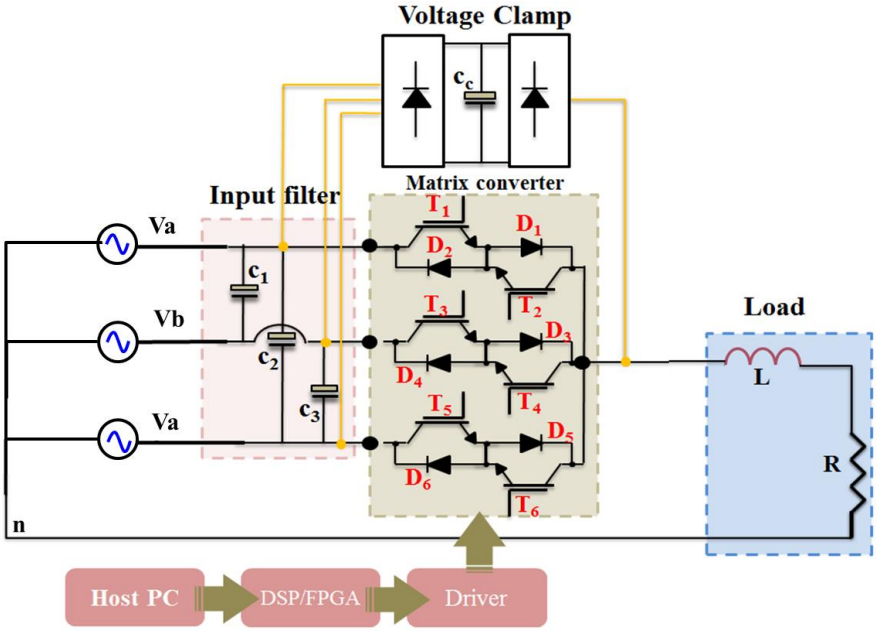


Fig.6.1 Schematic of experimental setup

Here note to be taken from Chapter 5 is that the high frequency input filtering capacitors (C1, C2 and C3) are already embedded into the matrix converter. The value of the input capacitor is chosen and calculated by considering two requirements where the choice of the reactive power at the supply frequency is minimized and the voltage drop across the inductor at a rated current is minimized in order to provide the possible highest voltage transfer ratio.

$$C_{fil} = \frac{P_{out} \times \tan(\theta_{max})}{3V_{in}^2 \omega_{in}} \qquad \text{(Eq.6.1)}$$

Where P_{out} - *output power*
V_{in} - *input voltage*
ω_{in} - *input frequency*
θ_{max} - *maximum input displacement angle*

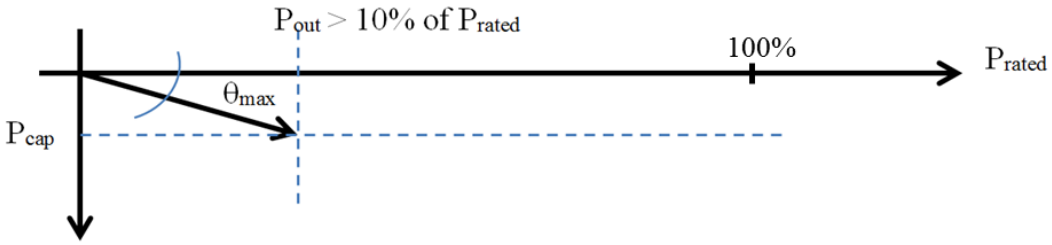


Fig.6.2 Required performance at the rated power of matrix converter

The detailed consideration taken to evaluate the capacitor value are listed in Table 6.1 which were planned to test the functionality of the matrix converter. As from Fig.6.2 and stated in Eq.6.1 [90], the required capacitance was calculated considering the output power is greater than 10% of the rated power and the power factor, $\cos(\theta_{max})$, is greater than or equal to 0.95.

Table 6.1 Matrix converter testing parametres

Parameter	**Value**
Input voltage	100V
Output voltage	85V
Output current	10A
Capacirors connection	Delta
Input frequency	50Hz
Capacitor calculated	~2uF

6.1.1. Power and measurement board

Fig.6.3 shows the assembled hardware and test setup, corresponding to the circuit schematic depicted in Fig.6.1. In the initial set-up, a dedicated test board was built, which accommodates passives and interface with the control platform; also, the gate drivers were connected to the switch terminals still using additional connectors to enable more easily a thorough characterization of the converter performance. A four layer printed circuit board (PCB) for the implementation of the power plane is designed along with measurement

circuits. The input and output terminals of the power converter were built directly on the PCB so that connection can be made using bolts and nuts. The power module is cooled through the water cooling system where the inlet and outlet are firmly fitted with 8mm plastic tubes.

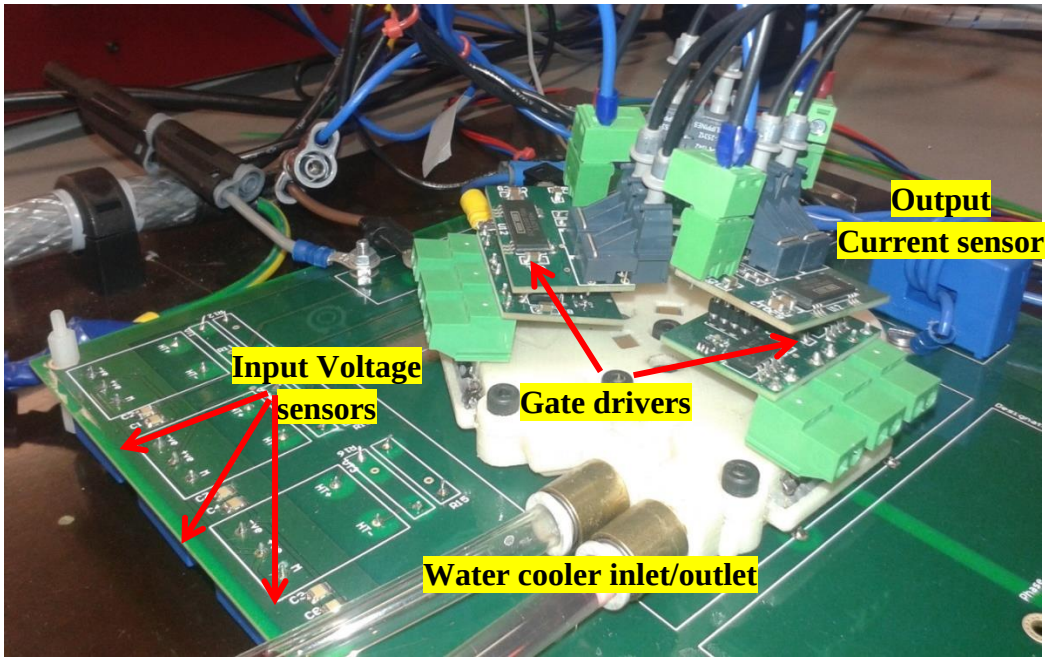


Fig.6.3 Experimental test setup

The input data required by the control platform is supplied from the measurement circuits though the voltage and current sensors. The data includes three input voltages, one output current and a clamp capacitor voltage. All instantaneous voltages are measured using commercially available voltage transducers (LV25-P model) and the output current is monitored using a LAH-25-NP model transducer to ensure that the converter does not operate over the maximum current level. The maximum value of current allowed in the output of the converter is set in the digital signal processor (DSP) program. Using this fixed output current value the DSP will protect the matrix converter and automatically switched off the system in the event of overcurrent condition.

6.1.2. Gate drive circuit

The signals provided by the DSP through field programmable gate array (FGPA) are not capable of switching the power devices and for this reason a suitable gate drive needs to be built. Three gate drivers were designed for the functionality of the converter and have been placed on top of the three-to-one phase matrix converter assembly as shown in Fig.6.3. The corresponding single channel gate driver schematic is shown in Fig.6.4 where the same configuration is used for the other two. These drivers have two main purposes where one is to provide isolation between the control and power circuit and the other is to give the power to drive the switching devices (IGBTs).

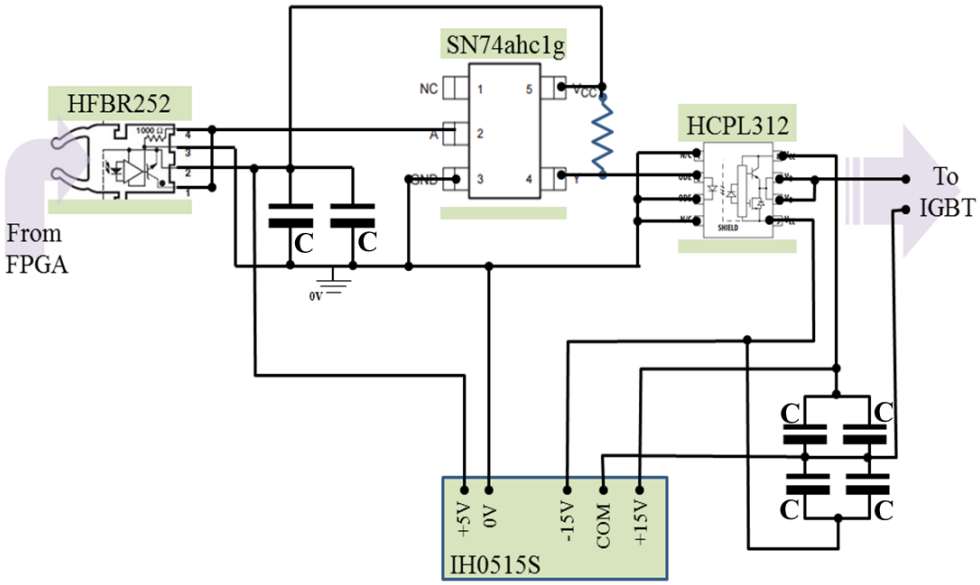


Fig.6.4 Schematic of gate drive for a single channel

The gate driver provides +15V and -15V between gate and emitter legs of the IGBTs to switch the device ON and OFF when the digital signal is high and low respectively. This is done through an isolation chip called HCPL-3120-300E IGBT gate drive optocoupler. The ground of the 5V control signal supply and the local signal references is isolated using a dc to dc converter which generate isolated +/-5V and +/-15V from a 5V power supply.

6.1.3. Protection circuit

Due to the lack of an inherent freewheeling path for circulating the inductive load current, the converter needs to be switched off whenever a fault occurred. Therefore, a suitable protection method was implemented to the converter. The proposed protection method known as voltage clamp circuit shown in Fig.6.5. It is the most common protection solution which is used to protect the bi-directional switches from damaging due to over-voltages in the event of commutation failure. The clamp circuit configuration generally consists of two rectifier bridge circuits using six fast-recovery diodes with a clamp capacitor and resistor connected in parallel [67]. In this test however, six input diodes and two output diodes are used as it clearly shown in Fig.6.5.

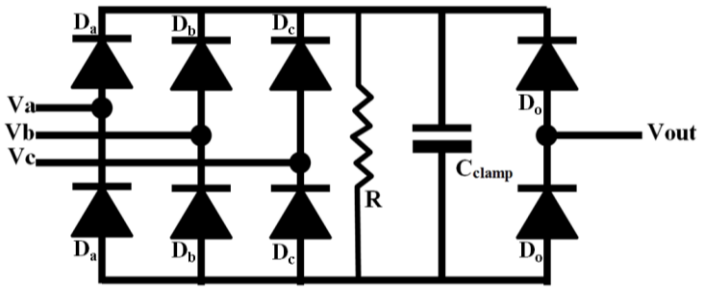


Fig.6.5 Voltage clamp circuit for overvoltage protection

The clamp capacitor C_{clamp} takes the commutation energy and stores it, whereas the dumping resistor discharges the energy stored in the clamp capacitor. The main task of the clamp circuit is to de-energize the load without damaging the power switches.

$$C_{clamp} = \frac{\frac{3}{4} I_{lim}^2 \times (L_l)}{V_{cmax}^2 - V_{cinit}^2} \qquad \text{(Eq.6.2)}$$

Where I_{lim} *- overcurrent protection level,*
L_l *-total motor leakage inductance,*
C_{clamp} *-clamp capacitor,*
V_{cmax} *-maximum admissible overvoltage and*
V_{cinit} *.clamp voltage before the fault condition*

The value of the clamp capacitor can be estimated using the Eq.6.2, taken from the comprehensive analysis for the design of the clamp circuit for matrix converters in induction motor applications, which is described in [90]. This value is chosen so that the increase in clamp voltage in the worst condition does not lead to the device voltage beyond its maximum rating.

6.1.4. Control platform

A four - step voltage based commutation scheme described in Chapter 4 is employed as a commutation control using 32-bit TMS320C6713 digital signal processor (DSP) board, a general purpose field programmable gate array (FPGA) based matrix converter interface card, and daughter card *(Fig.6.6)*. The DSP is used to perform all necessary calculations needed for the converter modulation and control. Whereas the FPGA board, designed by the Power Electronics Machines and Control group of the University of Nottingham handle all logic tasks such as four step commutation, analogue to digital (A/D) conversion.

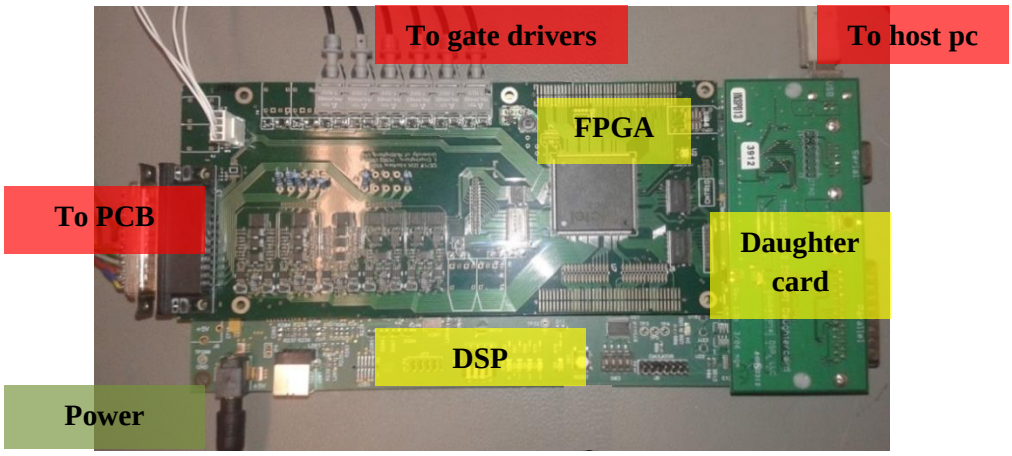


Fig.6.6 General Control board

A daughter card allows serial, parallel and universal serial bus (USB) access to the C6713DSK's host port interface (HPI) which can be used to permit a PC host so that the DSP operation can be controlled.

The values of the required output voltage and frequency are set in the DSP by using the Matlab interface through daughter card. This interface is directly linked to the DSP program so that one can either read values from variables used or write on them. The values of each of the variables used in the DSP program are monitored in a window displayed in the Matlab environment. This interface is also used to load the program into the DSP without the need of the Code Composer Studio (CCS) software which was used mainly to develop and implement the modulation technique and controller.

6.2. Functionality of the prototype

To validate the functionality and performance of the proposed matrix converter, the prototype was tested at a realistic power in the laboratory. The test conditions were very conservative to avoid unnecessary failures. The output voltage was set to be DC, but a purely resistive-inductive RL load was used, without any filter capacitors, which explains the load voltage and current waveforms.

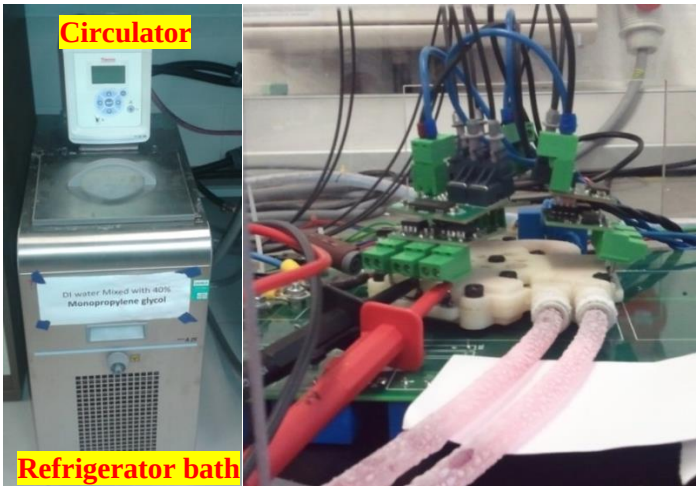


Fig.6.7 Hardware and test set-up for preliminary functional test operating at -15^{0}C

The switching frequency was set to 10 KHz. The cooling liquid temperature was set in the range of -15 to 20 ºC and a 40% less toxic propylene glycol was

used for corrosion and frost protection. Fig.6.7 illustrates the photographs of the water cooling system (SC100/A25 - Series refrigerated/heated bath circulator) and the converter operating at -15^{0}C of water cooling temperature.

6.2.1. Experimental results

The input supply as in Fig.6.8, is provided by a three phase variac. LeCroy differential probes were placed across RL load, converter input, and a single bi-directional switch. Then the corresponding results were observed using LeCroy oscilloscope and power analyzer.

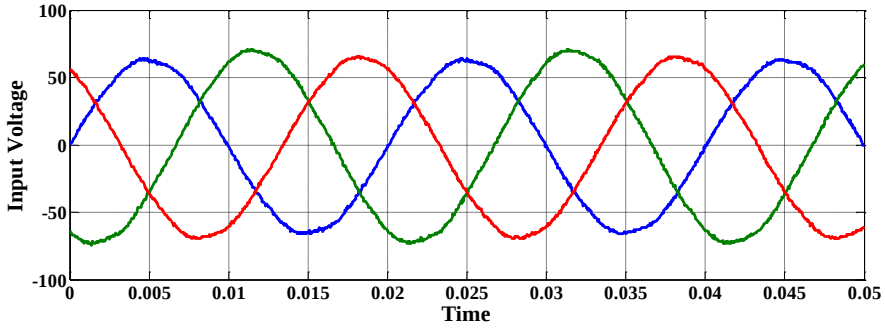


Fig.6.8 Converter's three phase input voltage (50-3phase)

The representative experimental results shown in Fig.6.9 are typical matrix converter waveforms: from bottom to top, gate-drive signals (C2, 20V/div), load output current (C3, 2A/div) and load output voltage (C1, 50V/div).

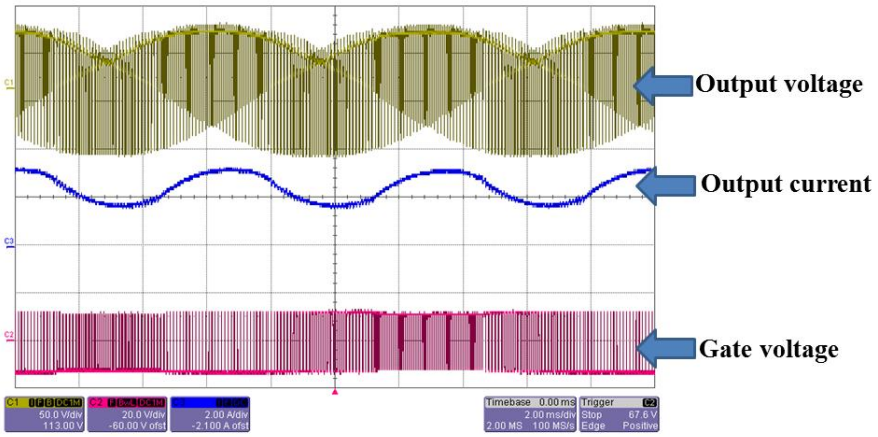


Fig.6.9 Representative Preliminary test waveforms for modular matrix converter.

Fig.6.10 proposes a zoomed-in view of the waveforms, with the addition of the voltage drop measured across one of the bi-directional switches (C4): as can be seen the switching waveform is free from overshoots of any sort, indicating a significantly contained value of the overall switch parasitic inductance.

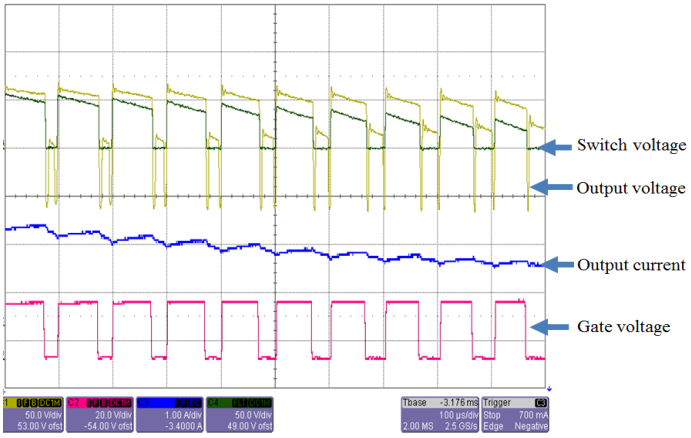


Fig.6.10 Detailed test waveforms including voltage across the bi-directional switch.

Electro-magnetic analysis discussed in Chapter 5 indicated a value of just a few nH for each current conduction path in a switch at a frequency of 10 kHz. It is worth to mention that this experimental test is not a lifetime test, but rather an evaluation of the prototype performance in order to gain an optimized three-to-one matrix phase converter design.

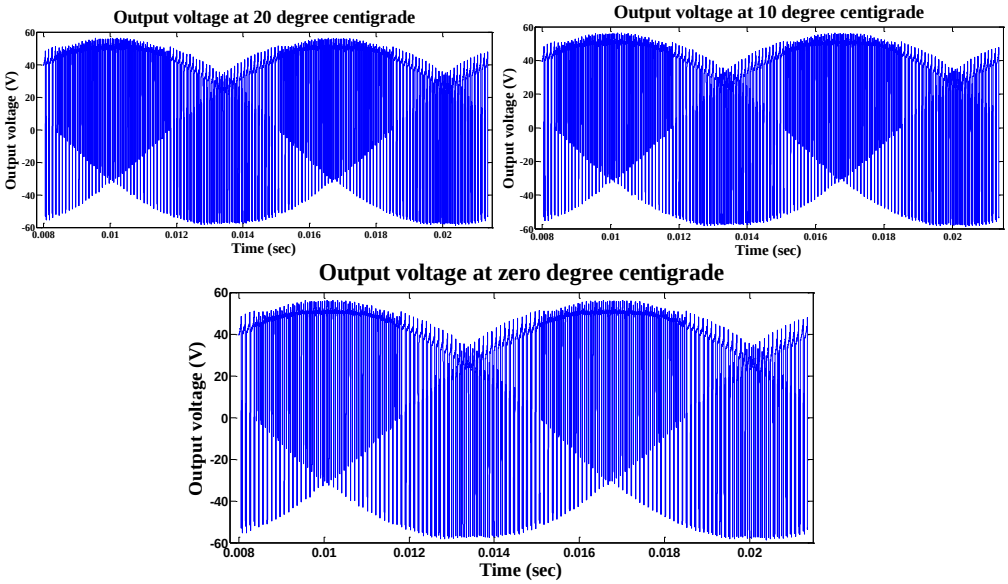


Fig.6.11 Test waveforms measured operating at positive cooling fluid temperatures.

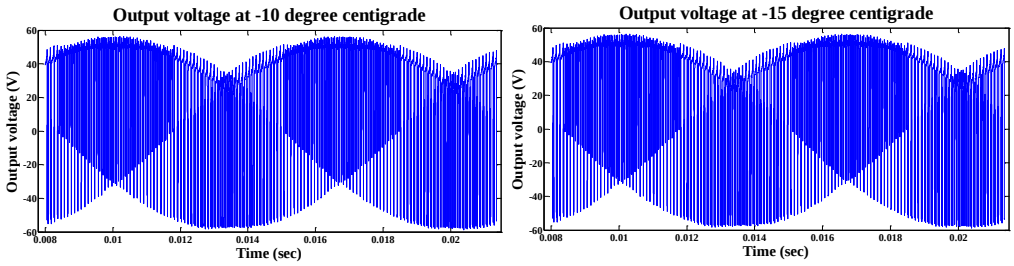


Fig.6.12 Test waveforms measured operating at negative cooling fluid temperatures.

The wave forms in Fig.6.11 and 12 show the output voltages measured while operating at different cooling liquid temperatures with 60V/3ϕ input voltage. As from the results the module has shown no indications of failure or difference and remains active over the entire temperature range (-15^0C to $+20^0$C). The indication is that such module can be further implemented over a wide and harsh temperature range.

Table 6.2 Functional test conditions

	Parameter	**Value**
Vin (three phase)	Input supply voltage	60V and 100V
f_{in}	Input line frequency	50Hz
C_{in}	Input capacitance	6.6uF
R_{out}	Load resistance	(6.4 - 57.6)Ω
L_{out}	Load inductance	10mH
V_{out} (single phase)	Output voltage	85V
f_{out}	Output frequency	0Hz
I_{out}	Output current	(8.9 – 1.5)A
f_{sw}	Switching frequency	10KHz
Module	Volume	~82.7cm3

The converter is also tested at 100V/3ϕ input (Fig.6.13) with various load resistances as shown in Table 6.2. The test was carried out on each five load resistances (6.4Ω, 9.6Ω, 19.2Ω, 28.8Ω, 57.6Ω) while each were connected in series with 10mH of load inductance.

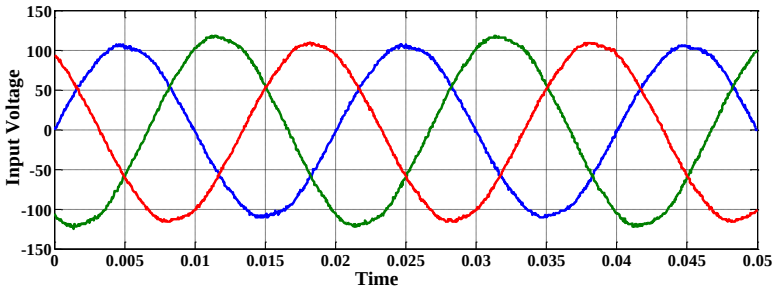


Fig.6.13 Converter's three phase input voltage (100V 3-phase)

Fig.6.14 – Fig.6.18 are the representative experimental results for the DC output voltage, a voltage across single bi-directional switch, and output current when the converter was operating at 100V/50Hz and load resistance of 6.4Ω .

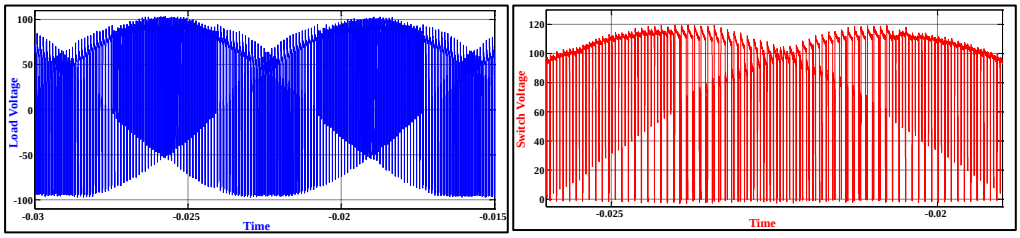


Fig.6.14. Measured single phase load voltage and voltage across BDS switch

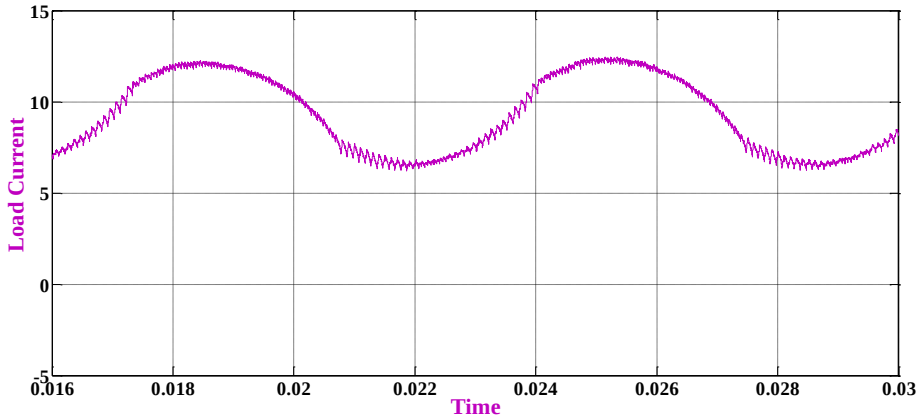


Fig.6.15 Measured single phase output current

The efficiency of a converter defined as (power out/power in), is an important measure of its performance especially when heat and life time are concerns. A power analizer is used to detect the measurement of the three input and single output voltage and current. The load resistance was varied while the three phase input voltage is fixed to 100V.

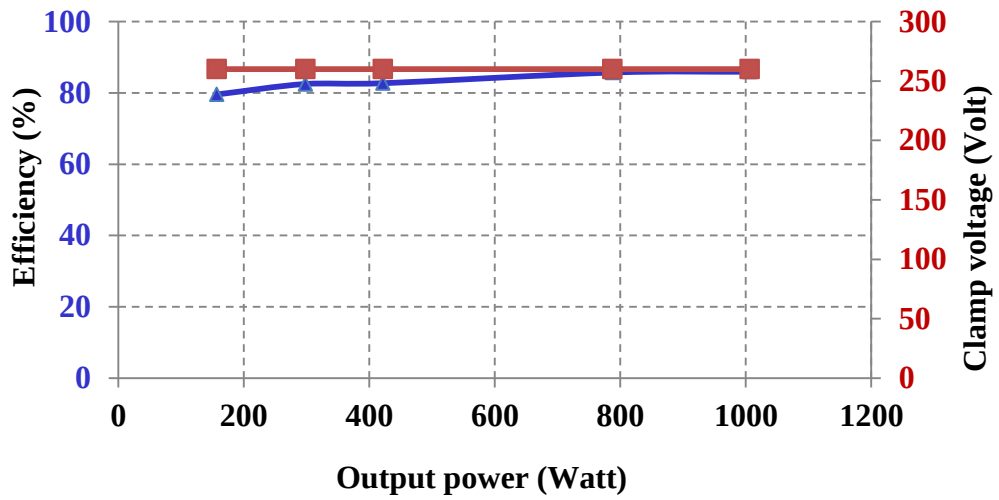


Fig.6.16 Effeciency of the 3-to-1 matrix converter prototype against its output power

Here, the prototype was tested in an open loop configuration and for this reason the voltage across the clamp capacitor was inspected and recorded 260V using a multimeter at all times. As from the graph in Fig.6.16, the power efficiency of the converter is maintained above 80% at different output power. Fig.6.17 and 6.18 are the extracted measured results of the efficiency of the converter as functions of load current and resistance respectively while the temperature of the cooling system is set to 25^0 centigrade.

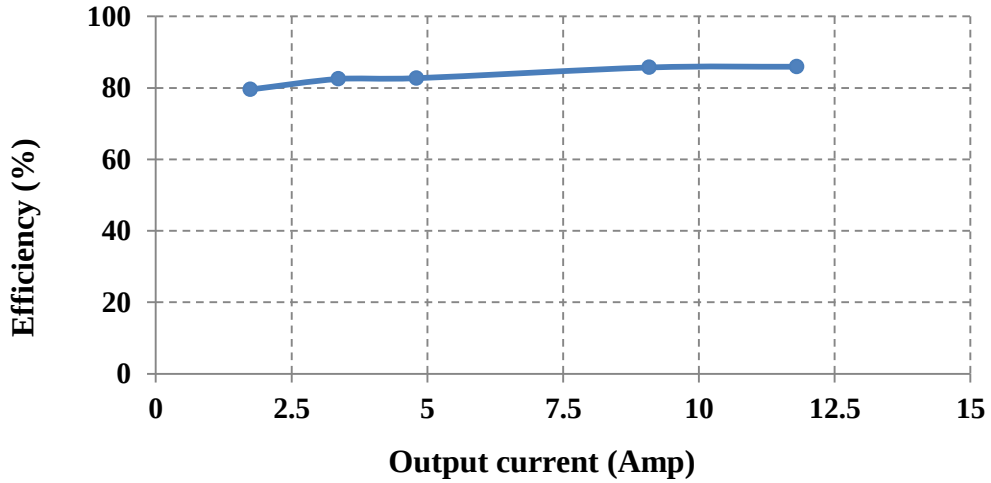


Fig.6.17 Effeciency of the 3-to-1 matrix converter prototype against its output current

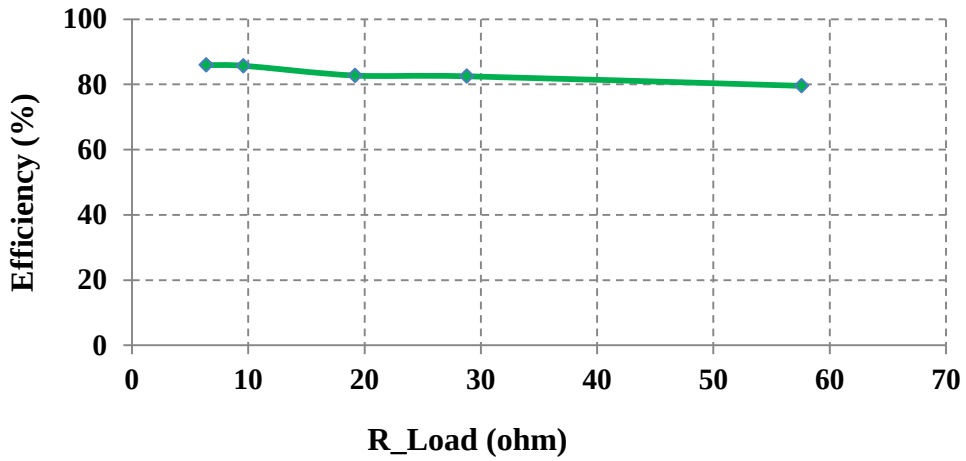


Fig.6.18 Effeciency of the 3-to-1 matrix converter prototype against load resistance

6.3. Summary

This chapter presented the functionality and performance of the modular integration of a three-to-one phase matrix converter. According to the result on the output current, a fluctuation has been recorded due to the input filter and control strategy, but in this particular work the intention was mainly concentrated at integrating the devices in a single assembly or package to adopt thermo-mechanical and electromagnetic performance. And for this reason, the test was carried out using an open loop system in order to show the dramatic reduction of parasitic inductance and functionality of the assembly while providing double-sided cooling capability.

Chapter 7:
Conclusion and Future work

7.1. Conclusion

This work has presented an advanced integration approach for power switches, demonstrating the correct electrical functionality of a three-to-one phase Matrix converter. Construction of the conventional wire-bond based power module has been critically discussed and compared. The main limitations of the traditional power module were identified on the basis of a detailed discussion of current practice; particularly the long and thin aluminium or copper wire bond based power converter design can only be improved partially when it comes to the thermal and electromagnetic issues.

Different circuit configurations were discussed prior to the selection of the proposed case study. In Chapter 5, comprehensive numerical study was carried out on a highly integrated bidirectional power switch constructed with the proposed stacked substrate–chip–bump–chip–substrate assembly. Based on the results obtained from simulations and subsequent experimental evaluation for reliability, this thesis has addressed the relative outcomes to improve the design even further. Thermomechanical simulation reveals that solder joints at the corners of the bumps in contact with the emitter can be critical. Twelve design

cases were considered; Cu brick bumps have the best thermal performance, and Cu hollow cylinder bumps with the thinnest thickness have the worst thermal performance. The CMC/CWC composite brick bumps showing optimized thermomechanical reliability of the assembly have thermal performance between the Cu brick bumps and the Cu hollow cylinder bumps, with only a maximum temperature of 1.5 K higher than in the case of Cu brick bumps. During both the mission profile and thermal cycling, the relevant maximum stress and creep strain developments reflecting the thermomechanical reliability of the Sn-3.5Ag solder joints and DBC substrates have similar order of magnitude when comparing the different bumps in the assembly. However, during mission profile, there were maximum von Mises stresses and creep strain accumulations in solder joints between bumps and IGBTs. Whereas during thermal cycling, maximum von Mises stresses and creep strain accumulations were recorded in solder joints that join bumps on DBC substrates.

The thermomechanical reliability of DBC substrates is dominated by the maximum-principal stress development within the AlN tiles. The results from the accelerated thermal cycling experiment verifies that selection of the CMC/CWC composite brick bumps in the stacked substrate–chip–bump–chip–substrate assembly can significantly improve the thermomechanical reliability of both the solder joints and the DBC substrates when compared to Cu cylinder bumps and Cu hollow cylinder bumps.

Basic insulation process was also performed. Five samples were prepared and subjected to partial discharge test. During the course of insulation, some factors

like dispensing pattern, speed, needle diameter, and substrate surface finish were assumed to have negligible effect on this particular prototype in terms of performance and reliability. Preliminary partial discharge test have shown reasonably good results that confirms the efficiency of the filling of silicone gel. Although the result gives some indication, this work needs to have further study and proper dielectric filling and test procedure to be able to confirm the definite insulation performance of the prototype.

Three bi-directional switches were constructed to build a modular integration of three-to-one phase matrix converter. The aim was to progress beyond the state of the art in power system assembly by proposing a solution which significantly improves the electromagnetic and electro-thermal performance of the semiconductor switches, as a result of both an original switch design and assembly process and system-level integration of the switches in the converter. The experimental results show an interesting advancement of the state of the art, which is represented by the recently proposed stacked package concepts based on the power bump interconnections, in particular by ensuring the switching waveforms free from overshoots of any sort indicating a significantly contained value of overall parasitic inductance. More importantly, the proposed approach is transferable to a number of topologies and has the additional important benefit of limiting the impact of single device/switch failure on the overall system availability. The solution can be of interest to all applications in which weight and volume reduction are highly favoured, such as aerospace, automotive, traction.

7.2. Future work and transfer of technology to other power switch architecture

Although the experimental validation of the prototype in Chapter 5 and 6 were successful, there are several subjects to be studied in this particular area of work. At the moment the approach and prototype work best when comparing the overall performance in terms of interconnection and material selection to the conventional wire-bond power module. However there are many open issues that must be solved before the definite performance and lifetime of the power module can be estimated.

One of the issues is the mechanism and order in which the boundary conditions occur in related to the power losses and thermal profiles. At the moment the present power loss profile does not take in to account the current commutation of the Matrix converter as stated in Chapter 4. The proper study of the power loss needs to be taken for the particular devices used in the prototype. Thermal management is also another aspect to this work where the current water cooling system and an alternative temperature measuring reference point could be further optimized and designed respectively so that the thermal model would describe the behaviour from the chip to the ambient.

To increase the level of confidence for the determination of the number of cycles to failure in particular for the thermomechanical fatigue test, repetition of experimental test to the most selected interconnects structure models would be of an interest. The current experiment procedure only considered one set of experiment to Cu cylinder and CMC brick type bump construction. In addition, apart from the unavailability of product in current technology trend, the CWC

brick type bumps could also provide better performance as compared to the CMC brick type bumps.

The final module electrical experiment was done using an open loop system and basic filters in order to show the functionality of the prototype. However, operating at a closed loop and properly designed filters are the scope of the future work to realise the performance of the converter. As from the related work presented below, the proposed work is fully transferable to other types of converters (e.g. half-bridge, full-bridge, multi-level, and photovoltaic converters) and wide band gap power devices (e.g. SiC and GaN).

7.2.1. Highly integrated design of a half-bridge switch

This is an advanced, application-driven integration approach of a half-bridge power switch. In particular, in trying to optimize the switching and thermal performance of the half-bridge switch, the assembly is designed to construct with double-etched Si3N4 (silicon-nitride) substrates, which also make use of filled via extending through the tracks to create a very low-inductive structure with a ground plane.

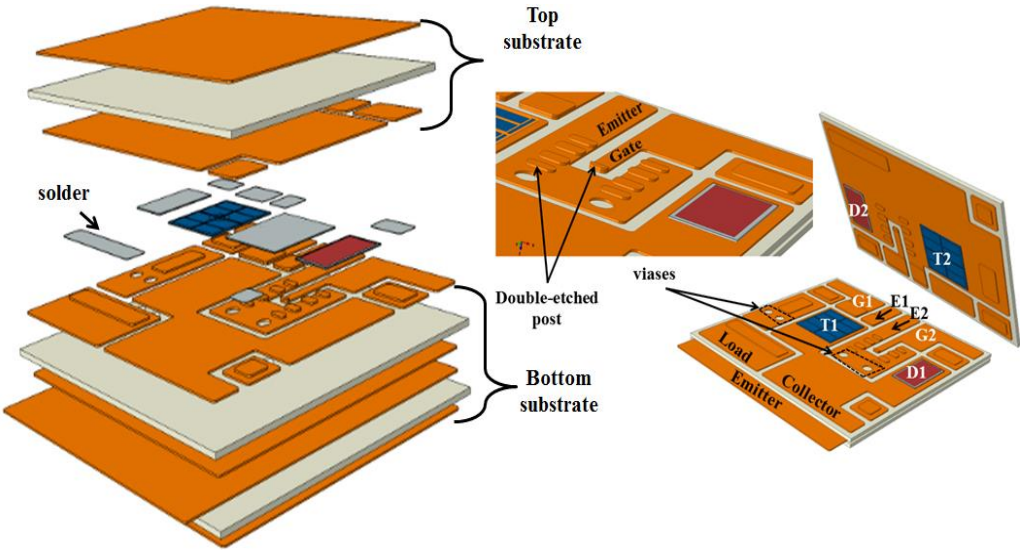


Fig.7.1 Building structure of the half-bridge switch

The optimization of the half-bridge switch layout (i.e., positioning of IGBTs and diodes) is being investigated and has given enhanced characteristics, both in terms of parasitic inductance and thermal performance. As from the layout in Fig.7.1, the switch is implemented in an innovative sandwich type assembly where each IGBTs and diodes are soldered backside onto the substrate. Such arrangement offers a minimum interconnection loop between T1 and D2, and between T2 and D1 as compared with [55].

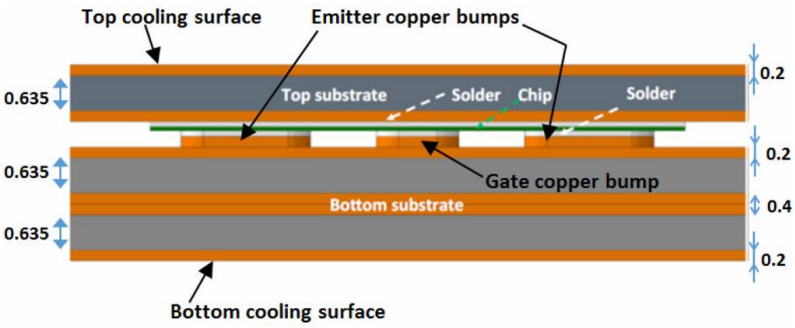


Fig.7.2 Detail of of vertical section at the IGBT side of the half-bridge switch model

To connect the chips top metallization to the substrates, double-etching of the tracks is used, which creates interconnection posts of suitable dimensions even for the gate contact. This solution enables to use a single solder layer between device metallization and copper post, also allowing for a very compact and thin assembly. A cross-sectional view of the proposed assembly, with the top substrate connected onto the bottom one, is shown in Fig.7.2, with a detail of component dimensions (all dimensions are in mm).

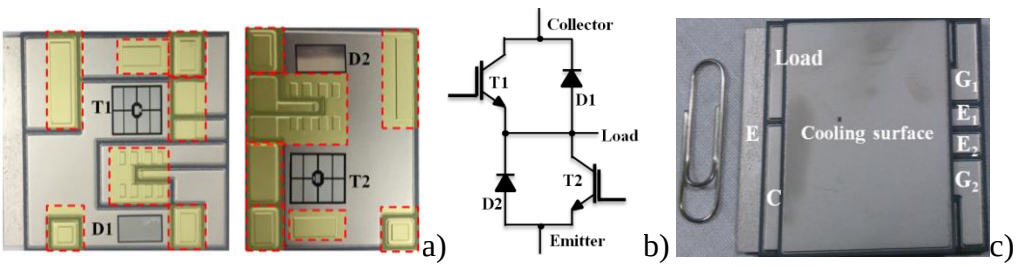


Fig.7.3 Open view with detail of the double-etched posts (shaded areas) a), schematic diagram b), and fully integrated half-bridge switch

The power and drive loops are also clearly separated as shown in Fig.7.3. So, external power line connections have been designed following similar idea applied to the switch in order to still minimise the overall parasitic inductance.

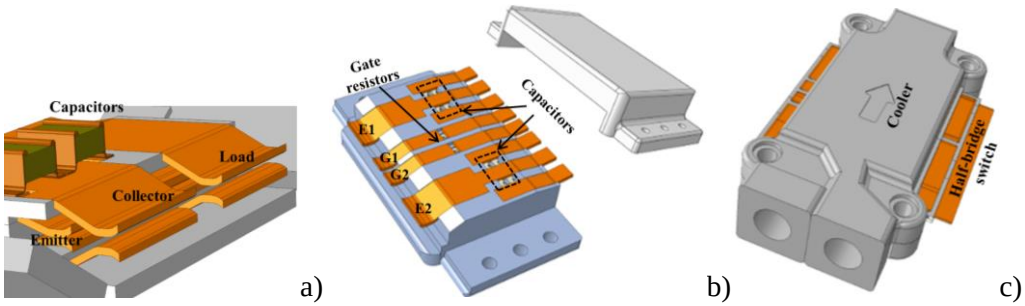


Fig.7.4 details of proposed switch; Source and load connector, a) gate side connector, b) cooler attached to both sides of the switch, c)

In both connectors, folded metal clips are used to ensure good electrical and mechanical contacts with the gate, emitter, collector, and load pads of the switch. Both connectors are also designed to embed small high frequency capacitors and gate resistors. The concept is illustrated in Fig.7.3.

The prototype containing the switch packed with cooler and connectors are shown in Fig.7.4. Plugged PCBs can be plugged into each connector sides for electrical functionality of the prototype.

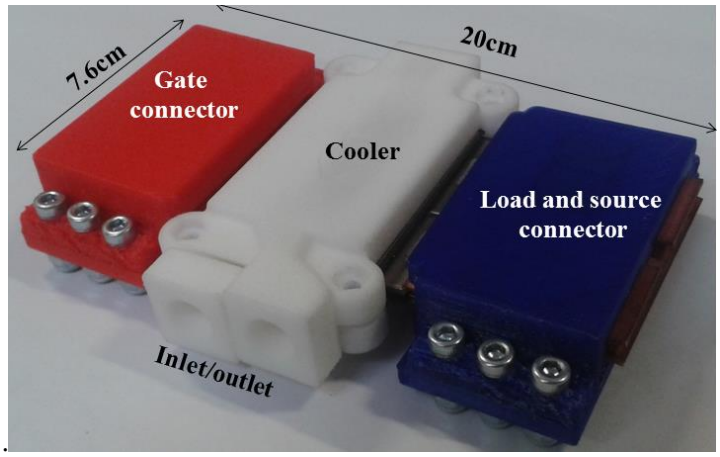


Fig.7.5 A photograph of the prototype with cooler and connectors inserted to the switch at the gate and power side

7.2.2. Advanced PCB Embedment Technology Integration

As from the discussion in Chapter 2, the standard commercial power modules are typically constructed with vertical transistors (MOSFETs, IGBTs) and diodes with their backside soldered onto patterned DBC or AMB ceramic substrates and their top metallization interconnected by heavy aluminium wire-bonds. Although the traditional power module assembling is a well-established, it is relatively expensive and exhibits a number of well-known electro-magnetic performance and reliability limitations. Its assembly technology is also not easily transferable to upcoming technology such as, wide-band-gap device (SiC, GaN), and low power applications. PCB embedment is becoming a promising technology to embed multiple chips and passive components using plated-through-hole (PTH) and micro-via interconnection techniques. Such technique can deliver lower parasitic effect, higher power density, higher switching frequency operation and overall improved performance.

Consumer electronics is one of the applications in power electronics which greatly benefit from the integration of power switching devices. Most of the current AC/DC wall adapters are constructed with volume consuming passive components such as transformer and filters operating at low frequency. However, operating at much higher frequency allows for much smaller passive components while handling the same power. In this particular work, a flyback based converter was designed on a PCB with six layers of 70μm thin primary and secondary copper windings. These layers are separated with 85μm thin embedded component packaging (ECP)-core dielectric material along with another 800μm ECP-core in the middle for chip embedment as shown in Fig.7.6.

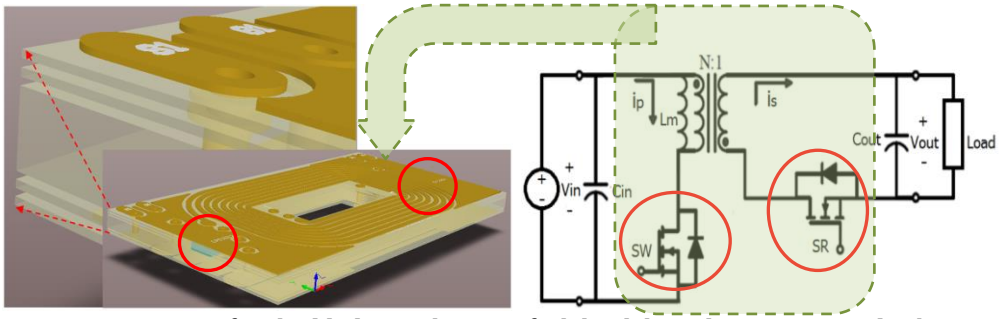


Fig.7.6 Structure of embedded PCB layout of Flyback based converter and schematic

Such position will ensure a symmetrical distribution of the copper layers in the circuit board to be able to decrease any bow or twist effect (warping) during manufacturing process. The present work is motivated by the need for computationally efficient thermal analysis of EPC's GaN *(Efficient Power Conversion Company)* based electronic devices (Fig.7.7), which are characterized by high frequency and power densities associated with high junction temperatures.

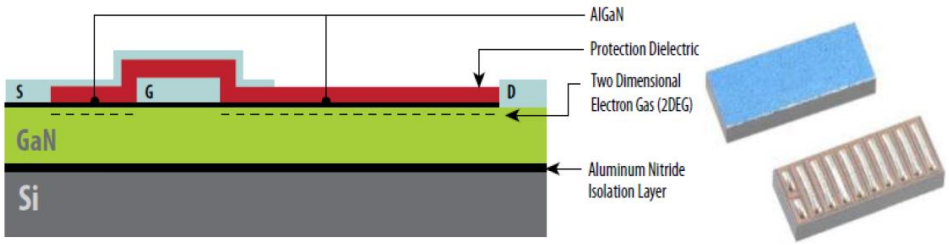


Fig.7.7 Lateral structure of EPC's GaN device

The winding and track interconnections are made of 0.8mm diameter plated though-hole (PTH) together with four 100µm diameter micro-vias depicted as in Fig.7.8. The very small form factor present in GaN devices lead to high junction temperatures and serious reliability concerns where these devices often have a very small heat source area corresponding to the length and width of each pad. Therefore, the design of using thermal micro-vias (Fig.7.8) having direct contact to both sides of the GaN chip is important in partially removing the heat from the device.

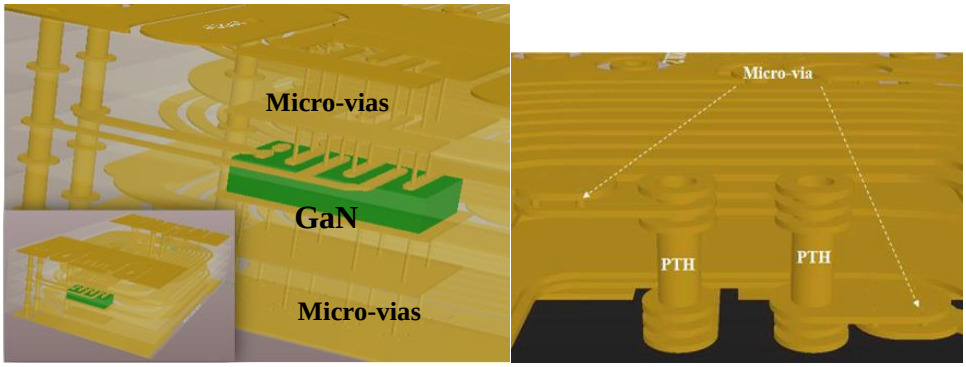


Fig.7.8 Micro-vias and PTH in the structure of embedded PCB layout

Numerical steady state thermal simulation result shown in Fig.7.9, illustrates that putting micro-vias on top and bottom sides of the GaN device along with thermal copper plate embedded in between offer partial reduction of junction temperature of the device as compared with no vias connected at the same boundary condition and loading.

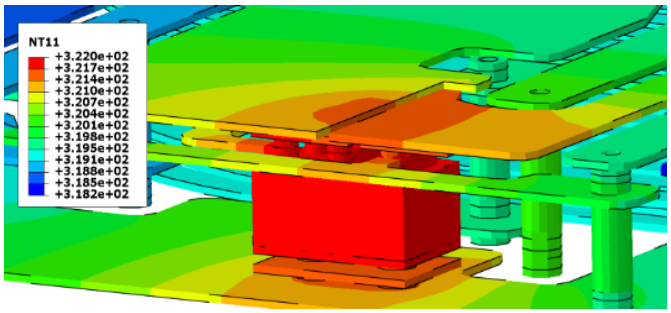


Fig.7.9 Temperature distribution for thermal micro-vias on both sides of the chip

Recently in [91], such innovative embedded die package has been developed by AT&S (ECP process) having no wire bonding to reduce the stray inductance and space exploitation as shown in Fig.7.10.

Fig.7.10 650V GaN on Silicon HEMT AT&S ECP Embedded Power Die Package [91]

Paper contributions to the project and related work

Journals

Adane. K. Solomon, A. Castellazzi, R. Sikuriat, and P. Wheeler. Member-ieee, "Modular Integration of a Matrix Converter," in *Transactions on IEEJ Industry Applications vol. 1, No. 1, 2016*.

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Appendix-1

70µm IGBT and Diode Datasheet

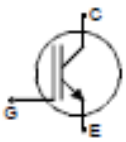
SIGC100T60R3

IGBT^3 Chip

FEATURES:
- 600V Trench & Field Stop technology
- low $V_{CE(sat)}$
- low turn-off losses
- short tail current
- positive temperature coefficient
- easy paralleling

This chip is used for:
- power module

Applications:
- drives



Chip Type	V_{CE}	I_{Cn}	Die Size	Package	Ordering Code
SIGC100T60R3	600V	200A	9.73 x 10.23 mm^2	sawn on foil	Q67050-A4345-A101

MECHANICAL PARAMETER:

Raster size	9.73 x 10.23	mm^2
Emitter pad size	(4.256 x 1.938) x 4 (4.256 x 2.356) x 4	
Gate pad size	1.615 x 0.817	
Area total / active	99.5 / 80.1	mm^2
Thickness	70	µm
Wafer size	150	mm
Flat position	90	deg
Max. possible chips per wafer	121 pcs	
Passivation frontside	Photoimide	
Emitter metallization	3200 nm AlSiCu	
Collector metallization	1400 nm Ni Ag –system suitable for epoxy and soft solder die bonding	
Die bond	electrically conductive glue or solder	
Wire bond	Al, <500µm	
Reject ink dot size	Ø 0.65mm ; max 1.2mm	
Recommended storage environment	store in original container, in dry nitrogen, < 6 month at an ambient temperature of 23°C	

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SIGC100T60R3

MAXIMUM RATINGS:

Parameter		Symbol	Value	Unit
Collector-emitter voltage, T_j= 25 °C		V_{CE}	600	V
DC collector current, limited by T_{jmax}		I_C	1)	A
Pulsed collector current, t_p limited by T_{jmax}		I_{Cpuls}	600	A
Gate emitter voltage		V_{GE}	±20	V
Operating junction and storage temperature		T_j, T_{stg}	-40 ... +175	°C
SC data, V_{GE} = 15V, V_{CC} = 360V	TVJ = 150°C	tp	6	µs
	TVJ = 25°C		8	

1) depending on thermal properties of assembly

STATIC CHARACTERISTICS (tested on chip), T_j=25 °C, unless otherwise specified

Parameter	Symbol	Conditions	Value			Unit
			min.	typ.	max.	
Collector-emitter breakdown voltage	$V_{(BR)CES}$	V_{GE}=0V , I_C= 4mA	600			V
Collector-emitter saturation voltage	$V_{CE(sat)}$	V_{GE}=15V, I_C=200A	1.05	1.45	1.85	
Gate-emitter threshold voltage	$V_{GE(th)}$	I_C=3200µA , V_{GE}=V_{CE}	5.0	5.8	6.5	
Zero gate voltage collector current	I_{CES}	V_{CE}=600V , V_{GE}=0V			10.1	µA
Gate-emitter leakage current	I_{GES}	V_{CE}=0V , V_{GE}=20V			–	nA
Integrated gate resistor	R_{Gint}			2		Ω

ELECTRICAL CHARACTERISTICS (verified by design/characterization):

Parameter	Symbol	Conditions	Value			Unit
			min.	typ.	max.	
Input capacitance	C_{iss}	V_{CE}=25V, V_{GE}=0V, f=1MHz		12335		pF
Output capacitance	C_{oss}			769		
Reverse transfer capacitance	C_{rss}			366		

SWITCHING CHARACTERISTICS (verified by design/characterization), Inductive load

Parameter	Symbol	Conditions	Value 2)			Unit
			min.	typ.	max.	
Turn-on delay time	$t_{d(on)}$	T_j=125°C, V_{CC}=300V, I_C=200A, V_{GE}=-15/15V, R_G= 2Ω		145		ns
Rise time	t_r			30		
Turn-off delay time	$t_{d(off)}$			340		
Fall time	t_f			60		

2) values also influenced by parasitic L- and C- in measurement and package.

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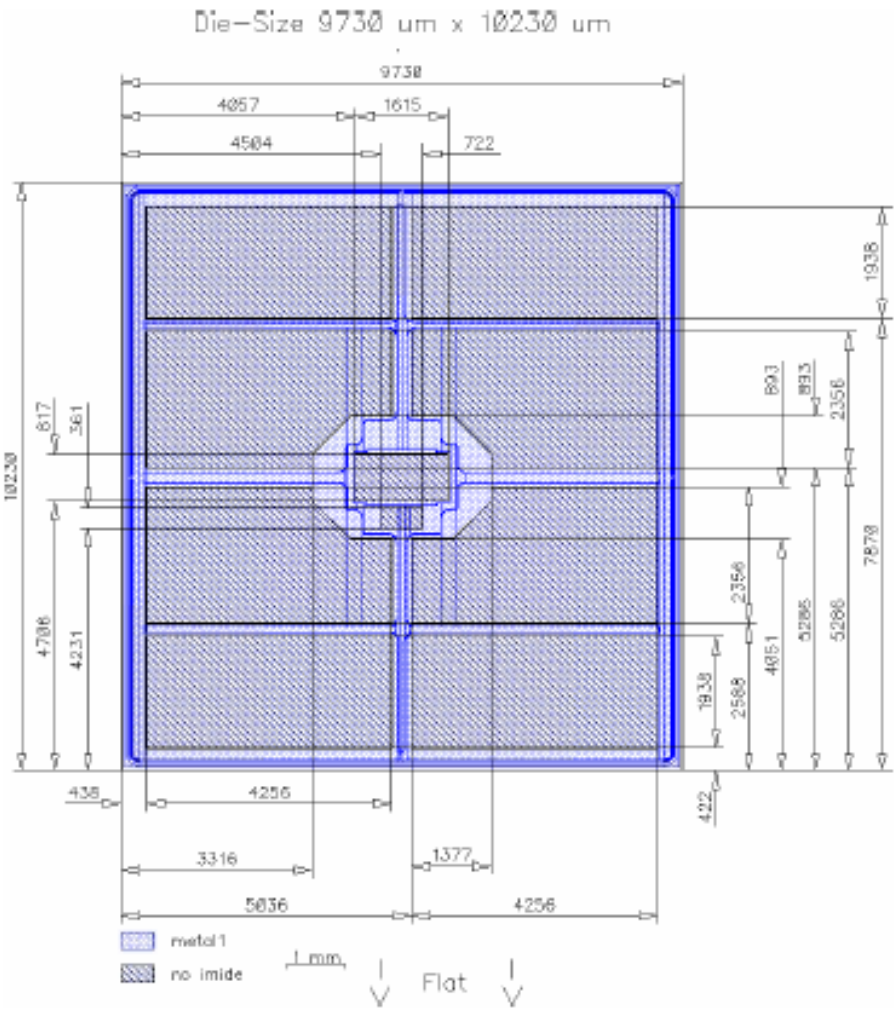
SIGC100T60R3

CHIP DRAWING:



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Infineon technologies

SIDC50D60C6

Fast switching diode chip in EMCON 3 -Technology

FEATURES:
- 600V EMCON 3 technology 70 µm chip
- soft, fast switching
- low reverse recovery charge
- small temperature coefficient

This chip is used for:
- power module

Applications:
- drives

Chip Type	V_R	I_F	Die Size	Package	Ordering Code
SIDC50D60C6	600V	200A	9.2 x 5.44 mm²	sawn on foil	Q67050-A4356-A101

MECHANICAL PARAMETER:

Raster size	9.2 x 5.44	mm²
Area total / active	50.05 / 44.47	
Anode pad size	8.52 x 4.74	
Thickness	70	µm
Wafer size	150	mm
Flat position	180	deg
Max. possible chips per wafer	282 pcs	
Passivation frontside	Photoimide	
Anode metallization	3200 nm AlSiCu	
Cathode metallization	Ni Ag –system suitable for epoxy and soft solder die bonding	
Die bond	electrically conductive glue or solder	
Wire bond	Al, ≤500µm	
Reject ink dot size	∅ 0.65mm; max 1.2mm	
Recommended storage environment	store in original container, in dry nitrogen, < 6 month at an ambient temperature of 23°C	

Infineon technologies

SIDC50D60C6

Maximum Ratings

Parameter	Symbol	Condition	Value	Unit
Repetitive peak reverse voltage	V_{RRM}		600	V
Continuous forward current limited by T_{jmax}	I_F		1)	A
Single pulse forward current (depending on wire bond configuration)	I_{FSM}	t_P = 10 ms sinusoidal	tbd	
Maximum repetitive forward current limited by T_{jmax}	I_{FRM}		600	
Operating junction and storage temperature	T_j , T_{stg}		-40...+175	°C

1) depending on thermal properties of assembly

Static Electrical Characteristics **(tested on chip)**, T_j=25 °C, unless otherwise specified

Parameter	Symbol	Conditions		Value			Unit
				min.	Typ.	max.	
Reverse leakage current	I_R	V_R= 600V	T_j=25°C			1250	µA
Cathode-Anode breakdown Voltage	V_{BR}	I_R=0.25mA	T_j=25°C	600			V
Forward voltage drop	V_F	I_F=200A	T_j=25°C	1.2	1.6	1.9	V

Dynamic Electrical Characteristics (verified by design/characterization), inductive load

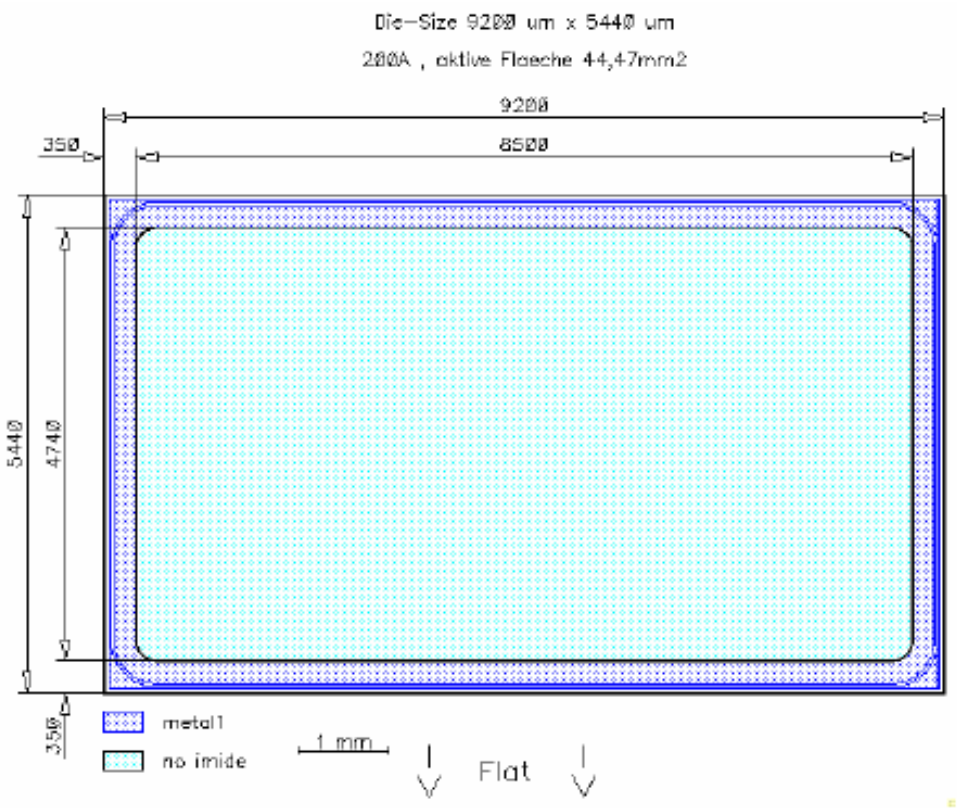
T_j = 25 °C, unless otherwise specified

Parameter	Symbol	Conditions		Value 2)			Unit
				min.	Typ.	max.	
Reverse recovery time	t_{rr1}	I_F=200A, dI/dt=tbdA/µs, V_R=300V	T_j = 25 °C		tbd		ns
	t_{rr2}		T_j = 125 °C		tbd		
Peak recovery current	I_{RRM1}	I_F=200A, dI/dt=tbdA/µs, V_R=300V	T_j = 25 °C		tbd		A
	I_{RRM2}		T_j = 125 °C		tbd		
Reverse recovery charge	Q_{rr1}	I_F=200A, dI/dt=tbdA/µs, V_R=300V	T_j=25°C		tbd		µC
	Q_{rr2}		T_j=125°C		tbd		
Peak rate of fall of reverse recovery current	di_{rr1}/dt	I_F=200A, dI/dt=tbdA/µs, V_R=300V	T_j=25°C		tbd		A/µs
	di_{rr2}/dt		T_j=125°C		tbd		
Softness	S1	I_F=200A, dI/dt=tbdA/µs, V_R=300V	T_j=25°C		tbd		1
	S2		T_j=125°C		tbd		

2) values also influenced by parasitic L- and C- in measurement and package.

SIDC50D60C6

CHIP DRAWING:



Appendix-2

Insulating silicone gel

RTV-2 Siliconkautschuk / RTV-2 Silicone Rubber | Wacker Silicone

swiss-composite.ch
suter-kunststoffe ag

WACKER SilGel® 612

Kennzeichen

WACKER SilGel® 612 ist ein gießbarer, bei Raumtemperatur vulkanisierbarer, additionsvernetzender Zweikomponenten-Siliconkautschuk.

WACKER SilGel® 612 vulkanisiert nicht zu einem Silicongummi im herkömmlichen Sinn, sondern ergibt ein weiches, gelartiges Vulkanisat.

Merkmale

- sehr dünnflüssig
- sehr niedrige Härte (Silicon-Gel)
- glasklares Vulkanisat
- ausgeprägte Eigenklebrigkeit
- exzellente mechanische Dämpfungseigenschaften

Characteristics

WACKER SilGel® 612 is a pourable, addition-curing two-component silicone rubber that cures at room temperature.

WACKER SilGel® 612 cures to a very soft, gel-like vulcanizate.

Features

- Very low viscosity
- Very low hardness (silicone gel)
- Crystal-clear vulcanizate
- Pronounced tackiness
- Excellent mechanical damping properties

Anwendung

- Verguß von elektronischen Bauteilen in der KFZ- und Leistungselektronik (für Anwendungen, bei denen ein geringer Ionengehalt gefordert wird, empfehlen wir SEMICOSIL® 912)
- Verguß von Solarzellen
- Einbettung von Glasfasern
- Herstellung von Dämpfungselementen
- Abdichtung von Reinraumfiltern

Applications

- Encapsulation of electronic components for the automotive and power electronics industries. (If low ion content is required, we recommend SEMICOSIL® 912.)
- Encapsulation of solar cells
- Embedding of optical fibres
- Production of shock absorbers
- Sealing of clean-room filters

Eigenschaften / Product data

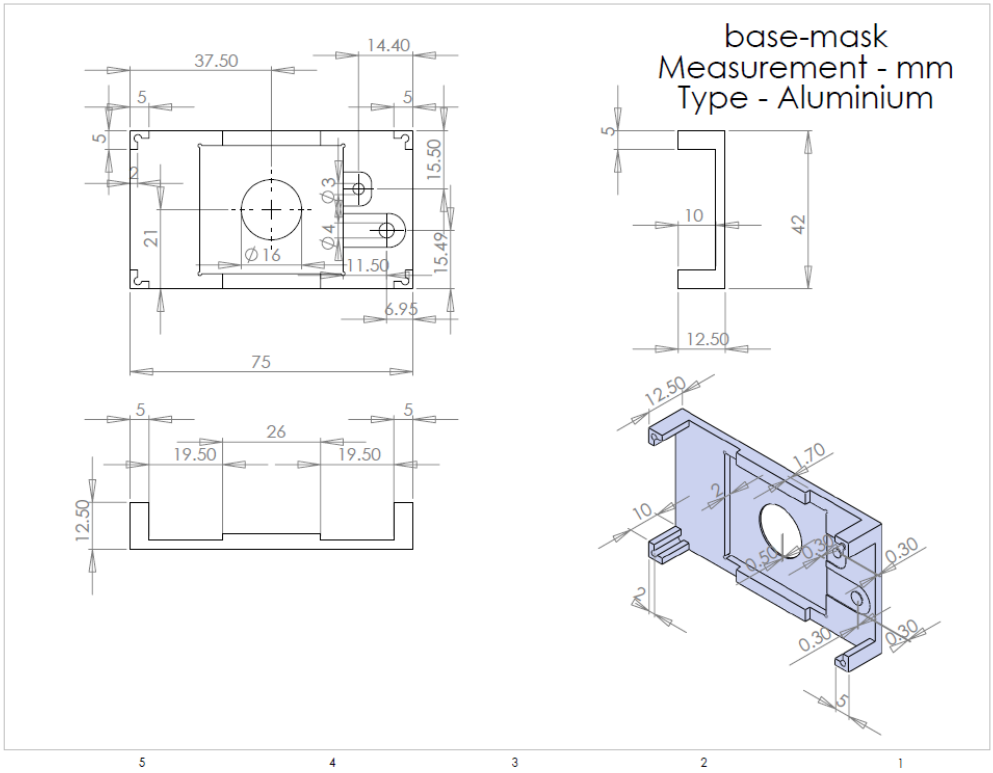
Unvulkanisiert / Uncured

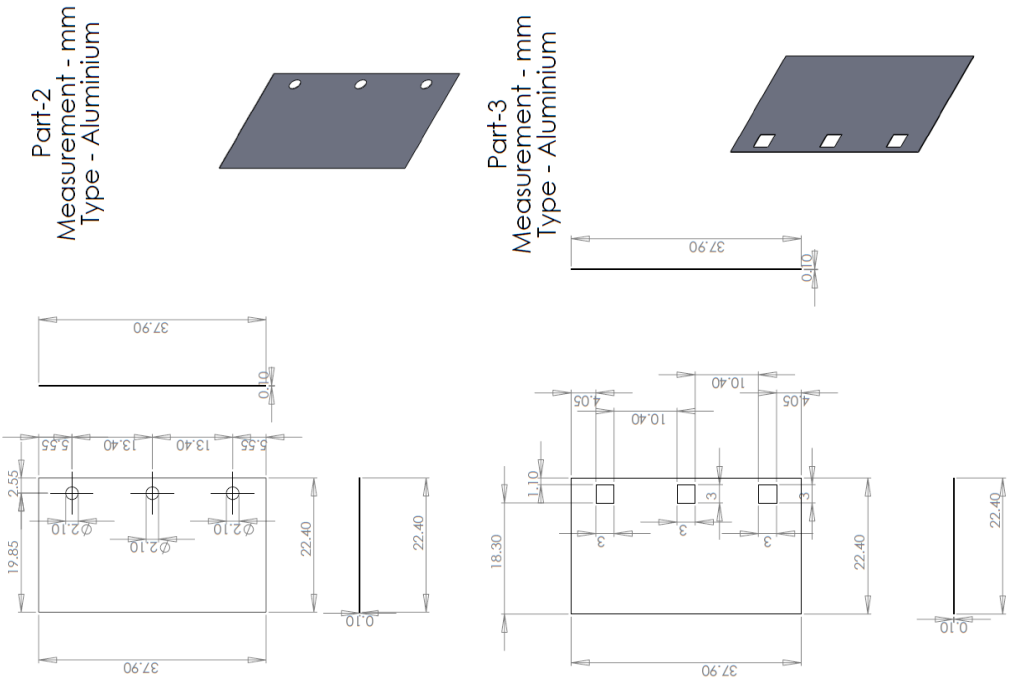
Komponente Component			A	B
Aussehen Appearance			transparent	transparent
Viskosität bei 23 °C Viscosity at 23 °C	Brookfield	[mPa s]	1.000	1.000
Dichte bei 23 °C Density at 23 °C		[g/cm³]	0.97	0.97
Brechungsindex Refractive index		[n_D^{25}]	1.4026	1.4031

Diese Angaben stellen Richtwerte dar und sind nicht zur Erstellung von Spezifikationen bestimmt.
These figures are intended as a guide and should not be used in preparing specifications.

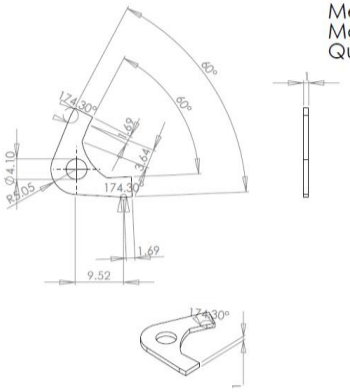
Appendix-3

Masks for soldering

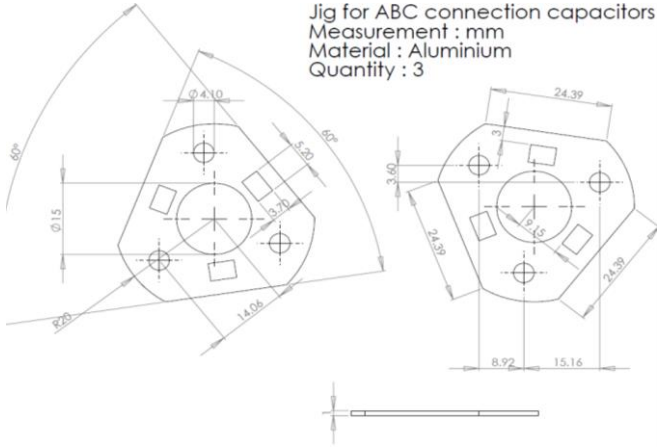




ABC rail1
Measurement : mm
Material : Copper
Quantity : 50

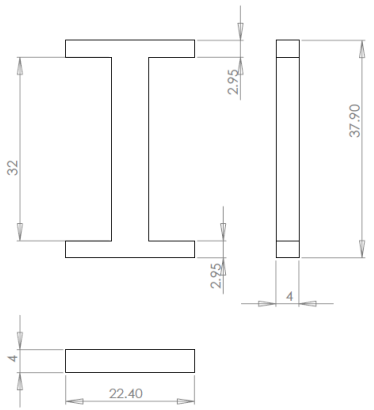


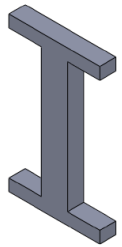
Jig for ABC connection capacitors
Measurement : mm
Material : Aluminium
Quantity : 3

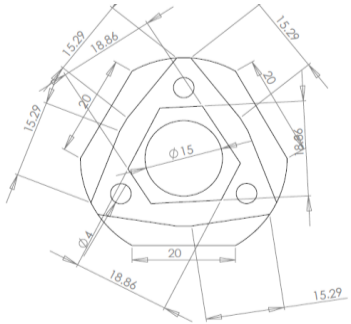


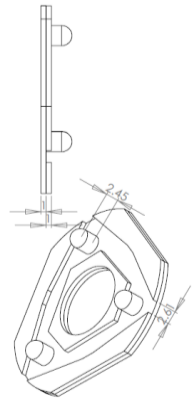
Part-4
Measurement - mm
Type - Aluminium

1mm and 4mm Thickness









jig_for_ABC_connection21

Appendix-4

Anand model ABAQUS subroutine

```
      SUBROUTINE SDVINI(STATEV,COORDS,NSTATV,NCRDS,NOEL,NPT,1 LAYER,KSPT)
C
      INCLUDE 'ABA_PARAM.INC'
C
      DIMENSION STATEV(NSTATV),COORDS(NCRDS)
C
     STATEV(1)=0.0
C
     RETURN
     END
C
     SUBROUTINE CREEP(DECRA,DESWA,STATEV,SERD,EC,ESW,P,QTILD,1
TEMP,DTEMP,PREDEF,DPRED,TIME, DTIME, CMNAME, LEXIMP,LEND,2
COORDS,NSTATV,NOEL,NPT,LAYER,KSPT,KSTEP,KINC)
C
     INCLUDE 'ABA_PARAM.INC'
C
     CHARACTER*80 CMNAME
C
     DIMENSION DECRA(5),DESWA(5),STATEV(*),PREDEF(*),DPRED(*), 1
TIME(2),COORDS(*),EC(2),ESW(2)
C
C     DEFINE CONSTANTS - Initialising variables for four different types of solder
C
C     96.5Sn3.5Ag
C     A=1.63E6 Q/R=14100 KK=1.61 M=0.13 SPAR=11.99E6
C     N=0.017 H0=58700E6 ALPHA=2.09 s0=7.72E6
C
C     So =   (MPa) Initial value of deformation resistance
C    Q/R = (1/kelvin) Acivation energy /Boltzmann's constant (universal gas constant:energy/volume;energy/volume
            Temp)
C      A      = (1/sec) Pre-Exponential factor
C     kk      = (dimensionless) Multiplier of stress (epsilon)
C     m       = (dimensionless) Strain rate sensitivity of stress
C     h0      = (MPa) Hardening/softening constant
C    spar     = (MPa) Coeff. for Deformation resistance saturation value
C     n       = (dimensionless) Strain rate sensitivity of saturation (Deformation resistance value
C    alpha    = (dimensionless) Strain rate sensitivity of hardening or softening
C
C
     A=1.63E6
     Q=14100
     XK=1.61
     XM=0.13
     XSPAR=11.99E3
     XN=0.017
     H0=58700E3
     ALPHA=2.09
     S0=7.72E3
C
     STATT=S0+STATEV(1)
     PKK=XK*QTILD/STATT
     TKK=Q/TEMP
     TT1=SINH(PKK)
     TEM=A*(TT1)**(1.0/XM)*EXP(-TKK)
     DECRA(1)=TEM*DTIME
     XSTAR=XSPAR*(TEM*EXP(TKK)/A)**XN
     TEM1=1-STATT/XSTAR
     ABSTE=ABS(TEM1)
     TEM2=(H0*ABSTE**ALPHA*TEM1/ABSTE)*DECRA(1)
     STATEV(1)=STATEV(1)+TEM2
     IF(LEXIMP.EQ.1) THEN
      DECRA(5)=XK*DECRA(1)*COSH(PKK)/(XM*STATT*TT1)
     END IF
C
     RETURN
     END
```