High Performance Active Filtering Solutions for Modern Aircraft Power Network

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Abstract

In the past 2 decades the increasing intensive use of non-linear loads has resulted in a substantial reduction of power quality in electric power systems. Current harmonics produced by non-linear loads, such as power electronic converters and electrical drives cause a number of problems in power distribution networks. In more recent years this problem has affected also smaller distribution grids like for example in aircrafts, due to the so called "more electric aircraft" trend, consisting in the replacement of most of hydraulic/pneumatic actuators with electronically controlled electromechanical devices. Electrically powered actuation is becoming more attractive due to technology advances in bespoke equipment among which electrical motors, magnetic materials, electronic control circuits and power devices. Power electronics converters are required to control electrical power and are necessary for example for actuator motor drives and to convert variable frequency (360-800Hz) in the next generation of civil aircraft to a constant frequency supply bus for various loads or to a DC supply bus. Although the presence of electrically powered equipment is desirable for weight and fuel cost reduction, the increase of electrical systems on board, and above all the presence of power electronic subsystems, brings severe challenges to aircraft power system distribution interns of power quality.

The aim of this research project is to investigate Shunt Active Filter (SAF) solutions to improve the quality of power of on-board grids. In particular advanced control strategies will be studied in order to enhance the SAFs' operation in maintaining high power quality in these particular power networks. Anyway, only harmonics compensation will be addressed, as considered SAF are not intended to alleviate other power quality potential issues such as current

unbalance between phases, reactive power compensation. This research project presents the specific application of a wide-band current control method based on Iterative Learning Control (ILC) for aircraft power networks, and introduces enhanced design strategies to increase compensation accuracy and improve the robustness of the SAF control system by using a P-type ILC controller. Due to the fact that a variable supply frequency (360Hz – 800Hz) is adopted in the power networks of newly released aircrafts, this research project presents a close investigation of the P-type ILC current controlled SAF system in such application (together with the standard fixed 400Hz supply), and hence identifies suitable modifications for the SAF system control to provide an effective and accurate current harmonic cancellation during the supply frequency variation.

Considering both simulation and experimental results, it can be concluded that the proposed SAF control proved to be very effective for accurate reduction of current harmonics on aircraft power grids with both fixed and variable supply frequency, using ordinary equipment and reasonable switching frequency and also ensuring good dynamics in transient conditions.

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Chapter 1 Introduction

In recent years, due to the "More Electric Aircraft (MEA)" paradigm, most hydraulic/pneumatic actuators are planned to be replaced by electronically controlled electromechanical devices. [1-3] Although the MEA paradigm can provide significant benefits in terms of actuation accuracy, flexibility, system dependability, energy efficiency and overall lifecycle, it also involves the intensive use of power converter systems; they have a non-linear behavior producing more intense current harmonics in the power system of the aircraft. These current harmonics can cause a number of problems in the power distribution equipments, such as the transmission losses, false tripping of circuit breakers or blowing of fuses, discrepancies in metering and interference to telecommunication system. [4-6] The power quality reduction can actually threaten the instruments precision, energy efficiency and most importantly the aircraft safety. Hence the importance of providing compensation system to reduce the current harmonics associated with non-linear loads should never be underestimated, which pushes the research field to find effective solutions.

For the harmonic cancellation on power networks, passive filters have been used historically, because of its simplicity and reliability. [7] Recently, due to the development in modern power electronic technologies, the research focus has gradually shifted from passive filters to active ones.[8-10] In this project, one of the most popular active filters structure, the Shunt Active Filter (SAF), will be studied and investigated for the aircraft power network application. Its superior ability for harmonics current cancellation and its feasibility and use in modern aircrafts will be demonstrated.

In a SAF system, the key issue to address for providing an accurate current harmonic cancellation is the implementation of a fast and stable current control loop. This subject will be carefully analyzed with in this study, where a control strategy called Iterative Learning Control (ILC) is investigated to be applied in the SAF system for overall improved performance. In order to provide a very accurate current harmonic cancellation, this work will focus on the adaptation and optimization of existing ILC technology for active power filtering in aircraft network.

Due to lower maintenance cost and higher reliability, the Variable Frequency Generator (VFG) becomes a popular direction in today's aircraft industry (see Section 1.1.2). However, one of the main drawbacks of the use of VFG is that, since its supply frequency varies proportionally to the engine rotor speed, this results in a variation in the current harmonics frequencies, indicating an increasing challenge for current harmonics cancellation. [4] Hence, in this study, suitable modifications and optimization of the basic ILC strategy are investigated in order to develop a novel SAF control system producing an accurate current harmonic cancellation for the VFG application.

This chapter firstly presents a background overview of the harmonic distortion problem, highlighting the importance and challenges of current harmonics cancellation in aircrafts power system, followed by the contribution of this research, the project objectives and the thesis plan.

1.1 Background overview

1.1.1 Power quality issues caused by the current harmonics

As it is well known, current harmonics are generally caused by the presence of non-linear loads supplied by AC grid. Typical examples of non-linear loads are fluorescent lamps, rectifiers, inverters, adjustable speed drives, switching power supplies etc. Current harmonics caused by these non-linear loads result in several problems for the overall power system [8].

One major problem associated with the grid harmonic distortion is the power losses. Current harmonics cause higher transmission losses, determining an increased cost per kW of power transmitted. In some cases, the harmonic power caused by the current harmonics can significantly increase the operating temperatures of generators and transformers and degrade the insulation material of their windings. The worst case is that such heating will make the insulation fail, as a result, the device in the power system would be damaged by a flashover. Moreover, the current harmonics can cause voltage distortion and overvoltage, which may affect electronic equipments in the power grid[6, 11].

In addition, the current harmonics in the transmission line can cause interference with communication circuits nearby and with eventual sensitive loads in the power system. In addition, in the control systems, the current zero-crossing detection is very sensitive to current harmonics; therefore control systems may not work properly under current harmonic distortion. In general we can say that current harmonics are menaces for the sensitive devices, such as medical devices, computers, and control systems. [12][16]

Together with current harmonics, grid resonance is another key issue that needs

to be addressed. Power factor correction capacitors coupled with line inductance as reactors can produce resonant frequencies when used in a predominantly inductive transmission system. If the resonant frequency coincides with the frequency of the current harmonic in the transmission line, a significant voltage distortion and over voltage will appear which can results in line faults.[12, 13]

Given the disadvantages mentioned above, current harmonics cancellation has been seriously considered in both research and industrial fields during recent years, above all considering the continuous increase of power electronics installations. Regulations and recommendations trying to limit this phenomenon have been also put in place. Currently, there are mainly three standards dealing with the current harmonics and power quality:

- IEEE 1159-1995: IEEE Recommended Practices for Monitoring Electrical Power Quality;[14]
- IEEE 519-1992: IEEE Recommended Practices and Requirements for Harmonic Control in Electrical Power Systems (standard applied in the USA), BC IEC 61000-3-4 (standard applied in the UK);[15, 16]
- TEC 1000 (1991-1995): Electromagnetic compatibility (EMC) .[13]

1.1.2 Harmonics in aircrafts power systems

Nowadays, due to the revolution of aircraft power generation and the MEA paradigm pushing for more and more use of non-linear loads in the aircraft power system, the research on current harmonics cancellation becomes more significant and the power quality requirements become stricter.

Most part of electrical power in an aircraft power system, excluding the backup one, is fed by the aircraft engines. During the flight period, the turbofans of the engines need to vary their speeds and the most popular solution for maintaining a supply frequency of 400Hz is to use the IDG power generating form.[4]

The concept of an IDG system is shown in fig.1.1. The key component in the IDG is the Constant Speed Drive (CSD).[17, 18] The CSD effectively acts as an automatic gearbox and can maintain the generator shaft speed at a constant rpm, which means the output AC power can be set with a fixed frequency of 400Hz.[18]

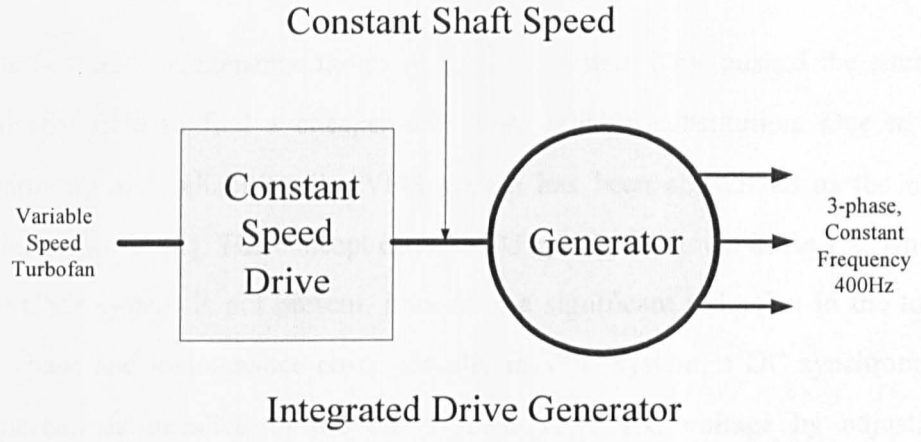


Figure 1. 1: Concept of Integrated Drive Generator (IDG)

The constant supply frequency on-board makes possible the use of standard solutions for the current harmonic filter in the IDG power system; even if the higher frequency, compared to terrestrial grids, introduce challenge on the control bandwidth in case of SAF use. Targets of harmonic compensation in IDG power systems are: [19, 20]

- Power quality (THD<10%);
- Simple structure and reliable filter system;
- Fast response to the load variation (for example, switching between zero load, half load and full load).

Although the IDG has been widely adopted for providing power with constant supply frequency in the aircraft system, it is not the best solution under the economical point of view.[4]

- The complexity and extreme operating conditions of the CSD make the IDG system expensive and become the most delicate part of the IDG system;
- The high level of maintenance required by the CSD in terms of frequent oil level change and oil cleanliness requirement make the cost of IDG systems a considerable issue.[21]

The cost and maintenance issues of the IDG system have pushed the aircraft industry field to find a cheaper and more reliable substitution. Due to its simplicity and reliability, the VFG system has been considered as the best solution so far [4]. The concept of the VFG system is shown in fig.1.2, where the CSD system is not present, indicating a significant reduction in the total purchase and maintenance costs. Usually in VFG system, a DC synchronous generator is installed to provide a fixed 115V AC voltage by adjusting excitation current.

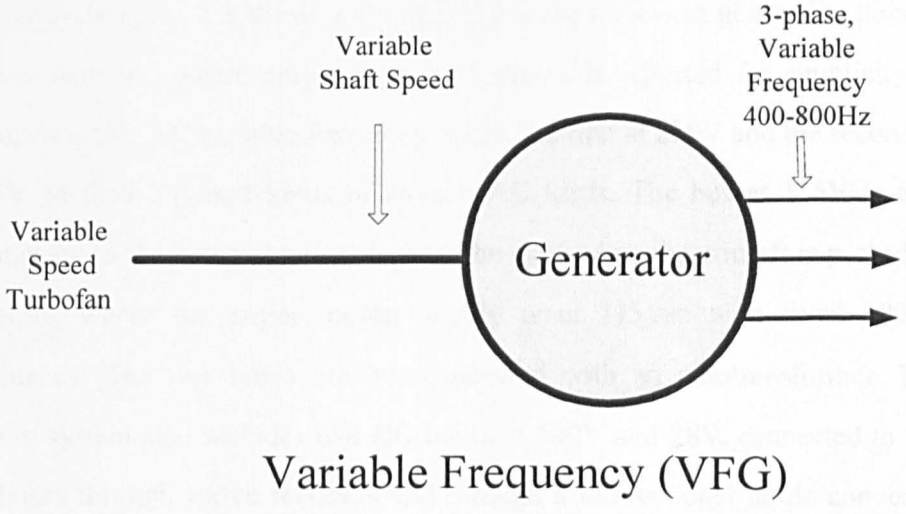


Figure 1. 2: The concept of the Variable Frequency Generator (VFG)

However, the application of the VFG leads to a variable supply frequency aircraft power network, results a stricter requirement of the power quality in the power system. In a typical VFG powered commercial aircraft, the supply frequency varies between 400Hz to 800Hz with a variation speed less than 100Hz per second.[5, 22, 23] This wide band variable supply frequency can cause a series of problems, among which affecting frequency sensitive aircraft loads in many important aircraft sub-systems.[24, 25] In order to solve this problem, more sensors and more complex diagnostic and control systems are needed for certain aircraft loads. However, as discussed in Section 1.1.1, the current harmonics can affect the overall performances of the sensors and control systems. This means, the more sensors and control systems are installed in the VFG power system; the stricter should be the requirement of power quality in the power system. Therefore, in practice, the recommendation for a current harmonic filter in a VFG power system is to ensure high power quality (THD<8%) during supply frequency variation from 400Hz to 800Hz and at each steady state operating point.[26]

On the other hand, aircraft power distribution systems contain many non-linear loads which can produce harmonic distortions. As an example of the aircraft power system, fig. 1.3 shows a simplified scheme for a next generation aircraft power network, where only one aircraft engine is reported for simplicity. It comprises two AC variable frequency buses, the first at 230V and the second at 115V, to feed different kinds of aircraft AC loads. The bus at 115V is also connected to the external power input to be used when the aircraft is parked in airports, where the airport power supply is at 115Vac with fixed 400Hz frequency. The two buses are interconnected with an autotransformer. The power system also includes two DC buses at 540V and 28V, connected to the ac buses through active rectifiers and through a bidirectional dc-dc converter between them.[4]

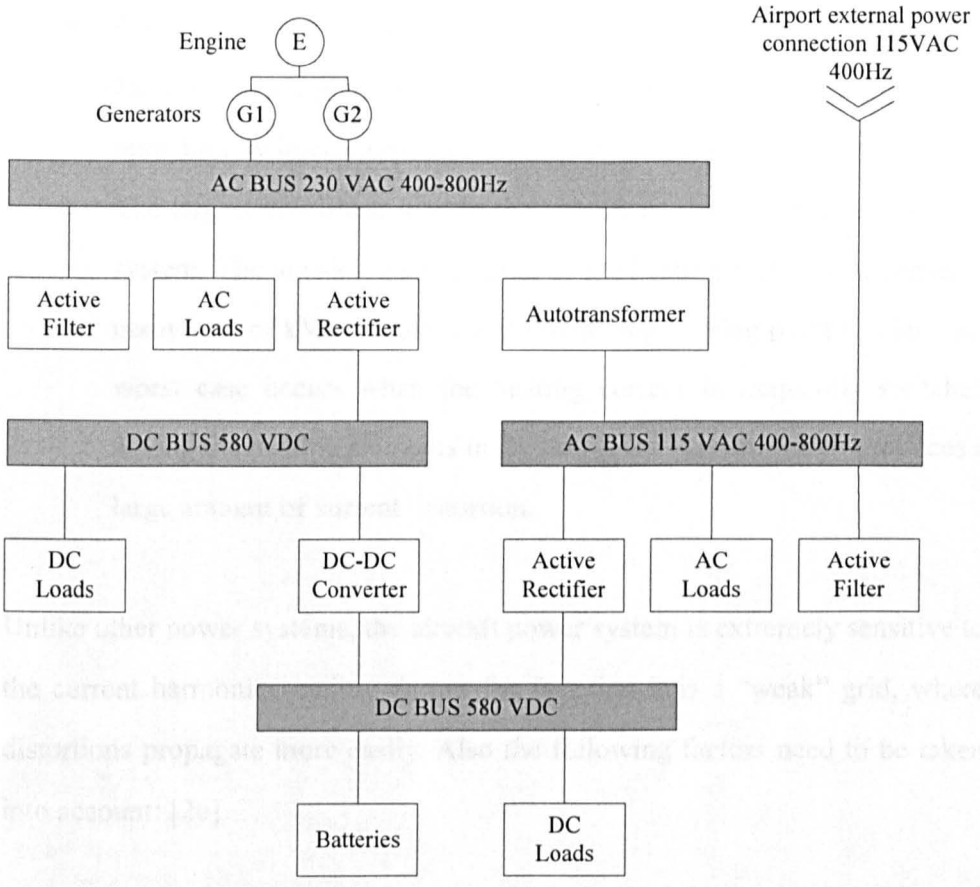


Figure 1. 3: Simplified example of electric aircraft power network.

Although the presence of electrically powered equipment is desirable for weight and fuel cost reduction, the increase of electrical systems on board, and above all the presence of power electronic subsystems, brings more non-linear loads producing current harmonics in aircraft power system. Typical non-linear loads including power electronic systems in modern aircraft power systems can mainly be summarized as follows. [27-29]

- Active rectifiers used to convert the 115VAC to 28VDC power, to supply devices such as navigation system, control systems and DC motors;
- AC/AC converters used to convert the 115VAC to 26VAC power and convert the 400-800Hz supply frequency to a certain frequency in some cases;

- Contactors used to switch power at various levels within the system. Many of them are placed in the primary power distribution system and may directly inject current distortions to the supply;
- The largest non-linear load in the aircraft power system is the heating system. The anti-icing sub-system in the heating system can consume many tens of kVAs. From the electrical engineering point of view, the worst case occurs when the heating current is frequently switched among the heating elements in the anti-icing system, which produces a large amount of current distortion.

Unlike other power systems, the aircraft power system is extremely sensitive to the current harmonics mainly due to the fact that it is a "weak" grid, where distortions propagate more easily. Also the following factors need to be taken into account: [20]

- Many electrical and electronic devices in the aircraft power system are particularly sensitive to distortion, which can directly affect the behavior of sensors, like for example in the heating system and primary avionics system;
- The current harmonics can also undermine the safe functioning of power devices in the aircraft power system, where some of them are usually used for continuous operation during the flight period, such as fuel booster pumps, flight instrument gyroscopes and etc. As discussed in Section 1.1.1, the current harmonics can reduce the lifecycle or even damage the power devices indicating the possibility of an accident. [28]

Therefore, for safety purposes, overall lifecycle and energy efficiency, there are strict requirements for the aircraft power quality, like for example, standard

DO-160E applied in the Boeing: 787B3-0147 and Airbus: AMD-24 .[30] Table 1.1 shows the specifications included in the standard DO-160E, where $i_{fundamental}$ represents the fundamental current and h represents the order of harmonic. It also needs to be mentioned that the DO-160E has a sticker limitation for the odd triple current harmonics than the non triple ones, in order to limit the unbalance of the supply current.

Table 1. 1: DO-160E current harmonics limitation

Harmonic Order (up to 40^{th} harmonic)	Limitation
3^{rd}, 5^{th}, 7^{th}	0.02 $i_{fundamental}$
Odd Triple Harmonics (h= 9, 15, 21,…39)	i_h=0.1 $i_{fundamental}$/h
11^{th}	0.1 $i_{fundamental}$
13^{th}	0.08 $i_{fundamental}$
Odd Non Triple Harmonics 17^{th}, 19^{th}	0.04 $i_{fundamental}$
Odd Non Triple Harmonics 23^{th}, 25^{th}	0.03 $i_{fundamental}$
Odd Non Triple Harmonics 29^{th}, 31^{th}, 35^{th}, 37^{th}	i_h=0.3$i_{fundamental}$/h
Even harmonics 2^{nd}, 4^{th}	i_h=0.01 $i_{fundamental}$/h
Even Harmonics >4^{th} (h=6,8,10,...40)	i_h=0.0025 $i_{fundamental}$

1.1.3 Challenges of current harmonics cancellation in aircraft power systems

Conventional current harmonics cancellation methods adopt passive filters. Along with the development of the aircraft power generation technology, this traditional approach appears inadequate, for the reasons that can be summarized as follows.

- Weight: Compared with active filtering solutions, the passive filter has heavier weight. The typical weight for a 4kW 400Hz passive filter is around 2kg, and a typical small commercial aircraft (20 passengers) requires at least 20 passive filters in its power network , which means the passive filter group has a total weight of at least 40kg;[31]
- Fixed operation frequency: Passive filters are designed as tuned band-pass filter with band-pass frequency determined by the harmonic components to attenuate harmonic components.

These disadvantages limit the application of the passive filtering solutions in modern aircraft power systems. As presented in Section 1.1.2, due to the simplification introduced in power generation, reduction in cost and improvement in reliability, the VFG are gradually taking over the IDG in commercial aircraft power system. As the name suggested, both VFG can operate in a variable fundamental frequency (generally from 400Hz to 800Hz), which is beyond the ability of current harmonics cancellation for conventional passive filter due to its fixed operation frequency. Therefore, the aircraft industry requires a suitable replacement of passive filters, providing an accurate current harmonics cancellation for the variable frequency power system.[7][24]

Research on active filters and in particular on SAF, has lasted for more than ten years.[32] The SAF is essentially a controlled current source, which theoretically injects a controlled current into the power system, containing all the harmonics to be compensated, but in phase opposition. Therefore, if such injection is ideal, the selected current harmonics in the power system can be perfectly cancelled. The key objectives to achieve accurate current harmonic cancellation for the SAF are:

- Accurate determination of the currents that the SAF should inject into the power system;
- Accurate current control loop for the SAF.[13]

Many control strategies have been investigated in literature but only few have proved capability of providing an accurate current control for the SAF in the VFG power systems. This is because, by using a VFG, the frequencies of the current harmonics proportionally vary with the fundamental supply frequency. The frequency variation increases the difficulties of accurately determining and tracking the demand current and increase the compensation challenge which is already strong given the high frequency of the harmonics.

1.2 Contribution of thesis

This thesis focuses on the current harmonics cancellation in aircraft grids for both IDG and VFG power systems by using a SAF. Based on the ILC theory, this thesis develops and proposes solutions for the application of SAF on board of modern aircraft systems. The SAF control strategy is also optimized for improvement in both control efficiency and accuracy. The original contributions of this thesis can be mainly summarized as follows.

- Mathematical verification of the feasibility of using the P-type ILC controller in cascade control systems like the voltage-current one needed for SAF control;
- Design and implementation of a P-type ILC controlled SAF system, providing a very accurate current harmonic cancellation for the aircraft IDG power systems (400Hz) or other power systems with fixed fundamental frequency;

- Optimization of the P-type ILC controller by improving its robustness, dynamic response and error-decay speed;
- Design and implementation of a P-type ILC controlled SAF system, providing an accurate current harmonic cancellation for aircraft VFG power systems in the range 400-800Hz;
- Design and implementation of the SAF prototype (with Marco Degano). Using the experimental data to prove that the prototype is able to successfully compensate the current harmonics in fixed (400Hz) or the linear variable (400-800Hz) supply frequency power network

In addition, the optimized P-type ILC controlled SAF system presented in the thesis, can not only be applied to aircraft power systems with supply frequency of 400Hz, but also be utilized in standard industrial applications with supply frequency of 50/60Hz. The optimized P-type ILC strategy can be also applied in many other control systems which have cascade control structure and repetitive reference signal, providing similar excellent performance.

1.3 Project objectives

1. Background research and literature review about existing SAF control strategies for various different applications particularly investigating the Iterative learning control as a possible solution

2. Implementation of a new control strategy for SAF installed in an aircraft IDG power system based on the ILC theory for its simplicity and performance. However, the cascade control structure of the SAF control loop does not fit well within the fundamental requirements for P-type ILC controller applications. Hence a mathematical robustness

analysis is conducted to verify the feasibility of applying P-type ILC controller in a cascade control system.

3. Investigate P-type ILC controller optimizations, in order to improve the robustness, dynamic response and error-decay speed (the reciprocal of the number of repetitions that ILC needed to converge the average absolute tracking error in a repetition to 1% of the initial average absolute tracking error) of the SAF control system.

4. Investigation of P-type ILC controlled SAF system and its application in aircraft VFG systems. In this case, the SAF control system must provide an accurate current harmonic cancellation with a fundamental frequency varying between 400Hz to 800Hz with a max frequency variation speed of about 200Hz/s.

5. Design and get ready an experimental prototype to verify the performance of the SAF system with the designed control strategies.

1.4 Thesis plan

Focusing on the objectives set out in previous section, this thesis is organized as follows:

Chapter 2 presents a literature review on SAF systems including their operation and the reference current derivation methods. This chapter will then focuses on the existing current control strategies for SAF and summarize their respective advantages and disadvantages. In the end, the motivations for applying P-type ILC for the SAF current control loop will be explained and commented.

Chapter 3 introduces the design procedure for the SAF system, where the SAF control loop will be designed in the traditional d-q rotating frame. A standard control strategy, based on Proportional plus resonant (P+resonant) controllers, will be designed. Its performance in the SAF control system will be demonstrated with simulation tests

Chapter 4 introduces the principle of the P-type ILC and its standard design method. In this chapter, the mathematical robustness analysis of the P-type ILC controller against system disturbances will also be investigated to prove its application feasibility in a cascade control system. Based on this analysis, few improvement techniques are proposed at the end of this chapter.

Chapter 5 presents suitable solution for applying the P-type ILC controller in the SAF current control loop, based on the mathematical derivation presented in the previous chapter. The improvement techniques proposed in Chapter 4 are verified by simulation test at the end of this chapter.

Chapter 6 presents a structure modification of the SAF system control, to simplify the application of the P-type ILC control strategy and to make implementation practical for an experimental verification. Then based on the mathematical analysis and simulation verification presented in Chapter 4 and 5, several standard and novel improvement methods for the P-type ILC controller will be presented, to significantly improve its robustness, dynamic response and error-decay speed.

Chapter 7 introduces the proposed control loop structure for the SAF in the VFG power system. The optimized P-type ILC controller designed in previous chapters will be implemented in this SAF application, to provide an accurate current harmonic cancellation during the supply frequency variation.

Chapter 8 experimentally verifies the SAF system with the control strategies proposed in Chapter 6 and 7. The experimental results will be analyzed against the simulation ones to validate the high performance of the designed SAF systems in both fixed and variable fundamental frequency power systems.

Chapter 9 summarizes the conclusions and contribution of this work. Directions for further work will also be included.

Chapter 2 Harmonic distortion and shunt active filter solutions

2.1 Introduction

The research focus of this thesis is to design, optimize and implement an active filtering solution for the current harmonics mitigation in modern aircrafts power systems; hence this chapter will present a literature review on active power filters and in particular the Shunt Active Filter (SAF) system, and its control strategies.

The first part of this chapter will present the general operation of SAF systems. The major parts of a typical SAF system, i.e. the control loop and the current harmonics derivation methods, will be introduced.[10][12] Since the performance of an SAF system greatly depends on its current control strategy, the second part of this chapter focuses on a literature review investigating existing current control strategies for SAF system studied and published in the past years, whose advantages and disadvantages in IDG (fixed supply frequency) and VFG (variable supply frequency) aircraft power systems will be analyzed, compared and discussed. Finally, a brief introduction of the Iterative Learning Control (ILC) theory will be given。 Advantages and drawbacks of applying the ILC strategy for fixed or variable supply frequency SAF in aircraft power system will be presented and discussed.

2.2 Introduction of the SAF system

Active filter systems have been designed, improved and commercialized in the last three decades.[33-35] With the enormous advances made in the past years on DSP digital control implementation and semiconductor power devices, active filter more and more represent a preferable solution to traditional passive filtering systems for grid harmonics mitigation. Many structures have been designed and proposed in the scientific literature among which there are the most widely studied:

- Shunt Active Filter (SAF), connected at the Point of Common Coupling (PCC) in paralleled with the grid. Namely aiming to compensate for current harmonics;[32]
- Series active filter, connected in series at the PCC, used for voltage harmonics mitigation;[36-38]
- Shunt or series hybrid active filters, they are used in conjunction with passive filters for a more effective compensation.[11]

SAF are the most studied and the most used practically, therefore this work will focus on them. Also researches show the SAF system has been applied in the IDG power systems with decent performances. [20][24] The basic operation theory of a SAF system will be presented in this section.

Figure 2.1 shows a three phase SAF connected in a power system. The SAF system is installed in parallel with the non-linear load. The SAF is expected to compensate the current harmonics ($\{i_h\}$) produced by the non-linear load to leave the only fundamental current at the PCC. Ideally, the SAF system can inject a current (i_f) with the same amplitude but reverse direction as the current harmonics ($\{i_h\}$), in such a way that the current harmonics in the power system

can be ideally perfectly cancelled leaving the non-linear load drawing only the fundamental current ($i_s=i_1$) from the supply. Through the concept of SAF system, it can be found that, the SAF system also can be used to compensate the unbalance behavior of power network by injecting as suitable current into the power network; however, in this research, the objective power network is assumed to be balanced. Hence the two key points of the SAF system control strategy can be summarized as follows.

- Accurate determination of the current harmonics $\{i_h\}$;
- Accurate control of the SAF system output current i_f to track $\{i_h\}$.[39]

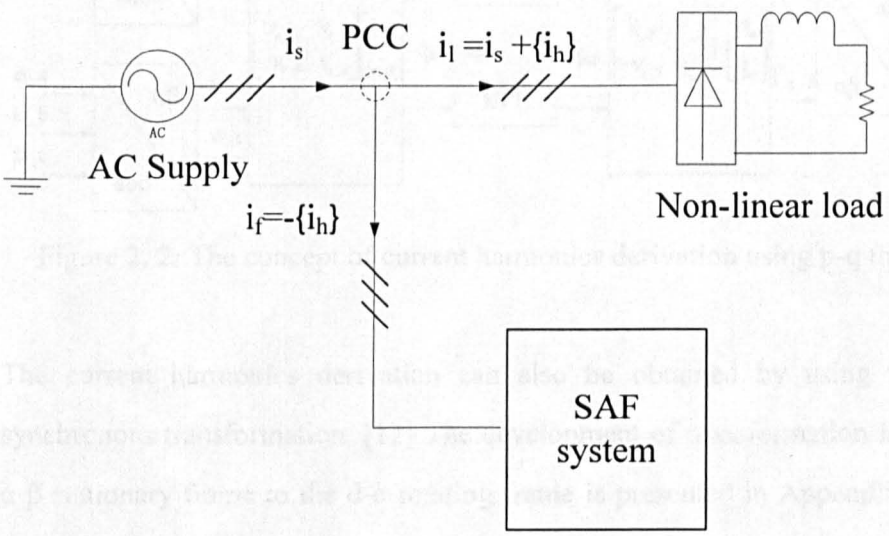


Figure 2. 1: The concept of SAF operation

2.2.1 Current harmonics derivation methods

Many current harmonic detection methods have been proposed in scientific literature with distinct characteristics valid for different kinds of applications. The most commonly used method is based on the instantaneous reactive power theory (p-q theory) firstly proposed by Akagi in [40]. As shown in fig. 2.2, both

supply voltage and supply current are measured to calculate the active power p and reactive power q in the αβ reference frame. It is assumed that the measured supply voltage does not contain any voltage distortions, therefore, if the supply current contains harmonic components, the p and q will contain both AC and DC components, where the AC components represent the harmonic power. A high-pass filter is used to allow the selection of the AC components while rejecting the DC components. Then the AC components of active and reactive power can be used to calculate the current harmonics, using the inverse αβ transformation.

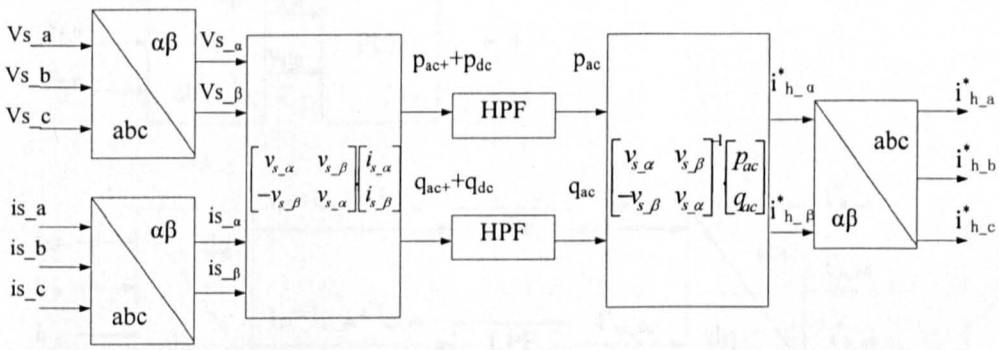


Figure 2. 2: The concept of current harmonics derivation using p-q theory

The current harmonics derivation can also be obtained by using the d-q synchronous transformation. [12] The development of transformation from the α-β stationary frame to the d-q rotating frame is presented in Appendix A. As presented in fig.2.3 (the figure only shows the derivation of one positive sequence (5^{th}) current harmonic and one negative sequence (7^{th}) current harmonic as an example), the instant angle θ of the supply voltage can be determined by using α-β transformation and a Phase Lock Loop (PLL). Under the assumptions where the supply voltage and supply current are in phase, and the supply voltage distortion is zero, once obtained θ though the supply voltage, the components in the measured load currents can be converted into DC components by using d-q transformation synchronous with each of the

harmonics i.e. 5θ for the 5th harmonic component, 7θ for the 7th harmonic component, etc. Therefore on each of these synchronous frames, the DC signal will represent the relative harmonic, but there will be also the presence of AC signals due to the multiple reference frame system interaction. By using low-pass filters, the DC components representing the current harmonics in the load current can be isolated. Hence the current harmonics can be determined by converting the AC components from the d-q rotating frame back to the a-b-c stationary frame using the corresponding PLL reference angle.[41]

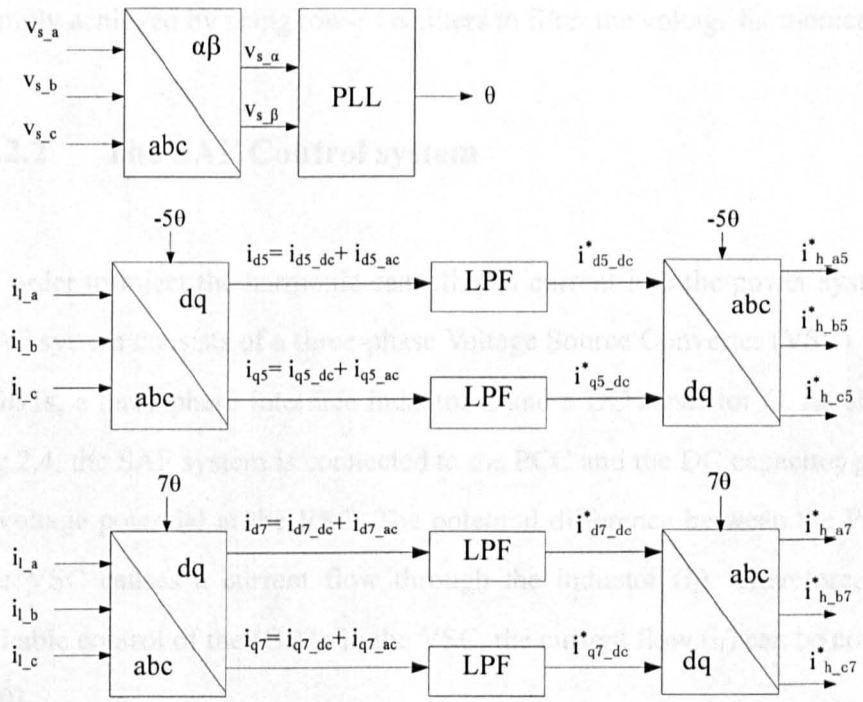


Figure 2. 3: Diagram of the multiple current harmonics synchronous frame system

As discussed above, both current harmonic derivation methods require rather complex computations. More importantly, the second current harmonic derivation method requires a precise determination of the instant angle θ, i.e., the effectiveness of the strategy relies on the correct design of the PLL system. A different method for current harmonics derivation will be adopted in this

work, due to its simplicity and accuracy in an isolated power system. It is explained in Chapter 6. However, it needs to be mentioned that, all these current harmonics derivation methods presented above, require a measurement of the supply voltage. This means the supply voltage harmonics can affect the accuracy of the determination of current harmonics. By using the first derivation method as an example, if the supply contains voltage harmonics, the current harmonic components may be converted into DC terms after the p-q calculation (see fig. 2.2), which means the current harmonics cannot be isolated by using the high-pass filters. The compensation strategy of this problem is simply achieved by using low-pass filters to filter the voltage harmonics.

2.2.2 The SAF Control system

In order to inject the harmonic cancellation current into the power system, the SAF system consists of a three-phase Voltage Source Converter (VSC) with six IGBTs, a three-phase interface inductor L and a DC capacitor C. As shown in fig.2.4, the SAF system is connected to the PCC and the DC capacitor provides a voltage potential at the VSC. The potential difference between the PCC and the VSC causes a current flow through the inductor (i_f). Therefore, with a suitable control of the IGBTs in the VSC, the current flow (i_f) can be controlled. [20]

As shown in fig.2.4, the SAF control system actually has two functions: 1) Maintaining a constant voltage in the DC capacitor, to provide a voltage potential for the VSC; 2) Controlling the switching signals of IGBTs for the current flow (i_f) control. In order to provide these two functions, the SAF system is designed to be in a cascade structure with an outer DC voltage control loop and an inner current control loop. The outer voltage control loop takes the measured DC voltage of the capacitor (V_{dc}) as the input and produces

a demand current (i_{dc}^*) to maintain the demand V_{dc}. The inner current control loop then produces a demand voltage (v_f) for the VSC to provide correctly controlled current flow (i_f) to cancel the current harmonics and maintain the DC voltage of the capacitor. Finally, the demand voltage is converted to the switching signals of the IGBTs by using a Pulse Width Modulator (PWM). [42]

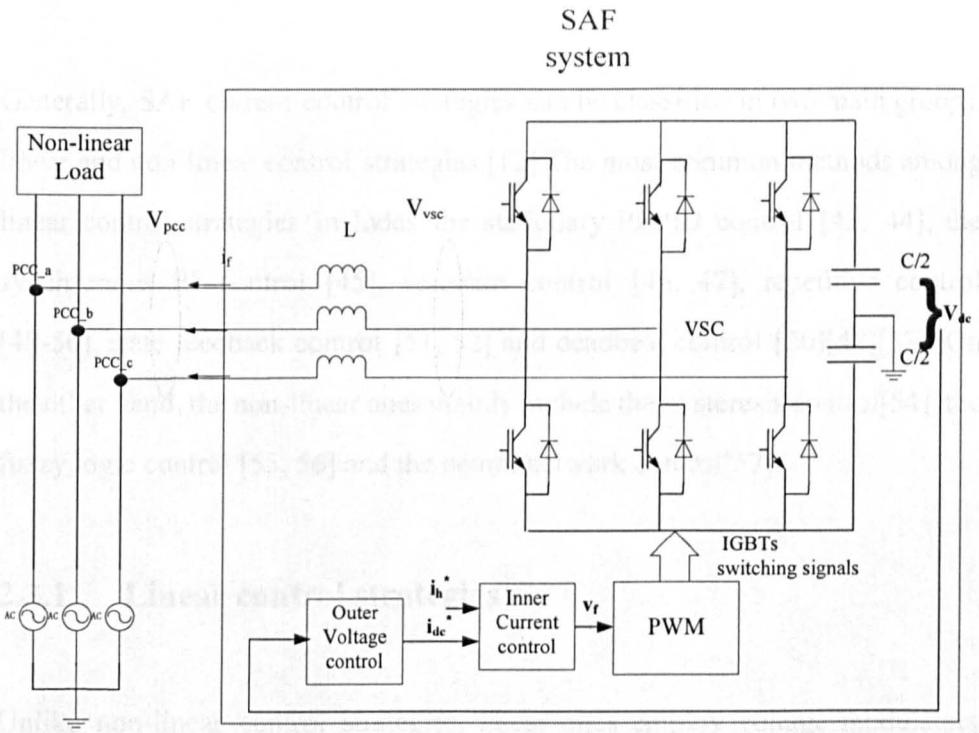


Figure 2. 4: Structure of the SAF system

In the SAF system, a simple PI controller can be adopted for the outer control loop as the V_{dc} is a constant DC value. However, the inner current control loop requires an accurate tracking of multiple frequency current reference to provide an effective current harmonics cancellation, which is the key control issue of the SAF system. [13]

2.3 Current control strategies

Due to the importance of the current control strategy in a SAF system, a literature review about the existing current control methods will be presented in this section, whose associated advantages and disadvantages will also be analyzed and compared.

Generally, SAF current control strategies can be classified in two main groups: linear and non-linear control strategies.[12] The most common methods among linear control strategies includes the stationary PI/PID control [43, 44], the synchronous PI control [45], resonant control [46, 47], repetitive control [48-50], state feedback control [51, 52] and deadbeat control [20][48][53]. On the other hand, the non-linear ones mainly include the hysteresis control[54], the fuzzy logic control [55, 56] and the neural network control[57].

2.3.1 Linear control strategies

Unlike non-linear control strategies, linear ones employ voltage modulators such as sinusoidal PWM [58] and space-vector modulation[59], which normally use a constant switching frequency.

2.3.1.1 Stationary PI/PID control

The stationary PI/PID control strategy uses three PI/PID controllers, one for each phase, to compensate the current tracking error under the interference between three phases. If a stationary $\alpha\beta$ reference frame is used instead, and the zero-sequence component can be neglected, then only two PI/PID controllers are need. The advantages of this control strategy are: 1) the simplest structure

and easiest to be implemented; 2) the design procedure of the PI/PID controller is simple. [43, 44]

The largest disadvantage of such control strategy derives from its reduced ability of accurate tracking of the current reference. Since the current reference in this application is a periodical signal containing high harmonic frequencies rather than a constant value, PI/PID controllers cannot avoid an inherent steady state tracking error, more evident at higher frequency due to the limited achievable closed loop bandwidth of the PI/PID controlled inner control loop.

2.3.1.2 Synchronous PI/PID control

Since PI/PID controllers can provide theoretically zero steady state tracking error for a constant reference signal, the disadvantage of the stationary control strategy can be partially compensated by using an reference frame synchronous with the fundamental.

The structure of the synchronous PI/PID control is shown in fig.2.5. As discussed in Section 2.2.1, if the supply voltage and supply current are in phase, given the instantaneous supply rotating angle θ, the d-q transformation can convert the fundamental component of an AC current reference to a corresponding constant value, which allows the PI/PID controller to provide an accurate current tracking for fundamental control. [45]

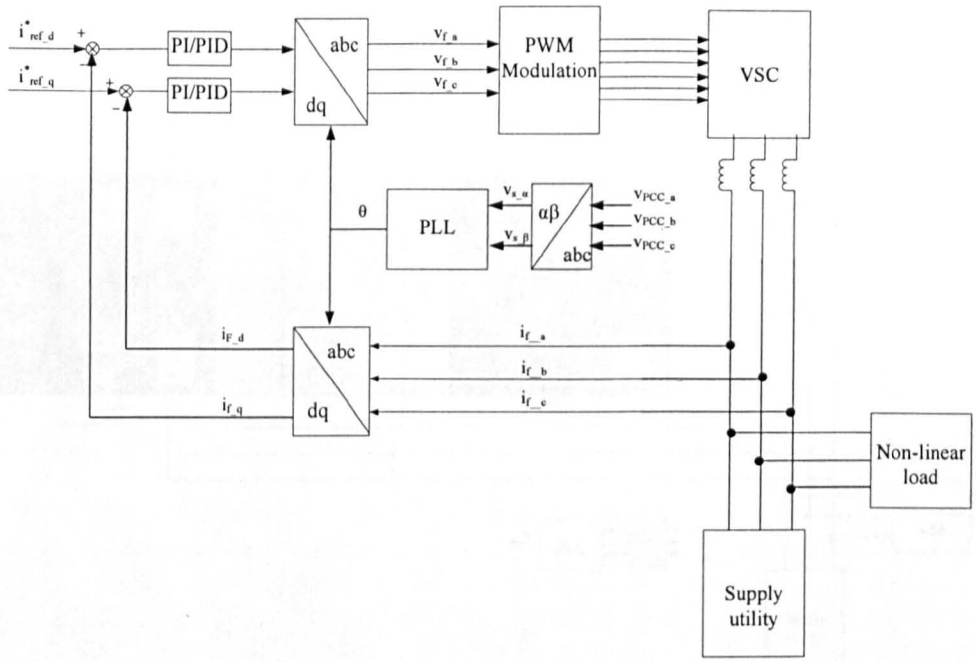


Figure 2. 5: Structure of the synchronous PI/PID control system

However such control strategy results insufficient for the current harmonics cancellation as it only converts the fundamental component to a corresponding DC value, all harmonics are converted to different harmonic frequency therefore their control is still affected by tracking error due to bandwidth limitations, above all for higher order harmonics.

2.3.1.3 Multiple synchronous reference frame PI/PID control

As discussed in Section 2.2.1, if the supply current and supply voltage are in phase, each current harmonic can be converted into a DC component by using different synchronous reference frames rotating at the corresponding harmonics angles. Hence, by using two PI controllers for each of the frames (as shown on fig. 2.6), the steady state tracking error can be significantly reduced even for higher order harmonics.[60]

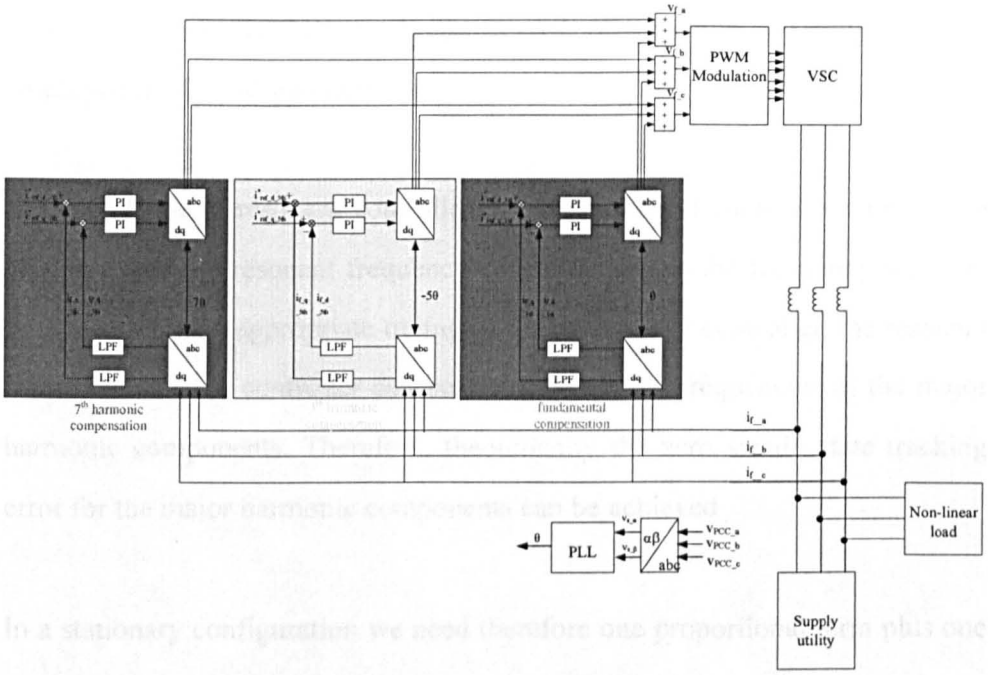


Figure 2. 6: Structure of the multiple synchronous reference frame PI/PID control system

Although this control strategy can provide an accurate reference tracking, it still has some drawbacks: 1) Interactions among the reference frames introduce relevant errors; 2) Increased complexity of the system with increased computational power requested.

2.3.1.4 Stationary and synchronous Proportional plus resonant (P+resonant) control

Research shows the synchronous P+resonant control strategy is a preferable approach for SAF current control [46]. The structure of this control strategy is similar to the one presented in fig.2.5, in the synchronous case where the PI/PID controllers are replaced by the P+resonant controllers. The characteristic of the P+resonant controller guarantees a more accurate current tracking over the standard PI/PID implementation. In the stationary case, three

P+resonant controllers are used, one of each phase while two controllers are employed in αβ configuration.

In general, the P+resonant controller is a narrow-band controller with a high gain at a specific resonant frequency corresponding to the frequency we want to control. With a appropriate tuning of the P+resonant controller, the resonant frequencies of the controller can be set to match the frequencies of the major harmonic components. Therefore, theoretically the zero steady state tracking error for the major harmonic components can be achieved.

In a stationary configuration we need therefore one proportional term plus one resonant term for each harmonic to be controlled. Using a synchronous frame can help to reduce the number of resonant terms for the P+resonant controller. As presented in Appendix A, both positive and negative sequence harmonics will appear as one harmonic in the d-q rotating frame. For example, 5^{th} and 7^{th} harmonic components will appear as the 6^{th} in a synchronous frame with the fundamental. Hence, only one resonant term is required to control two harmonic components.

Inevitably, the synchronous P+resonant control strategy also has its own disadvantages including:

- Only the major current harmonics in the current reference can be accurately tracked unless using a very complex controller structure;
- Appropriate tuning of the resonant frequencies controller is challenging, therefore increasing the design difficulty of the P+resonant controller;
- The resonant frequencies for the P+resonant controller are usually fixed, indicating its unsuitability for the VFG power system.

Due to the high performance of the resonant control presented in [46, 47], this control strategy will be further investigated in more details in Chapter 3.

2.3.1.5 Deadbeat control

Deadbeat control is a linear control strategy based on the system modal. More detail and its use in SAF current control application is described in [48, 53]. Compared with the P+resonant control strategy, this control strategy offers a similar current reference tracking performance in a wide frequency range rather than only at resonant frequencies [46].

The basic scheme of a digital deadbeat control strategy is represented in fig.2.7, where the operation of the controller consists of two major parts including predicting the current reference for the next sampling period ($i(k+1)^*_{ref}$) and using the predictive control law based on the discrete system model (which is the mathematical equation representing the relationship between VSC voltage $v(k)_f$, supply voltage $v(k)_{PCC}$, SAF current in current sampling period $i(k)_f$ and current reference for next sampling period $i(k+1)^*_{ref}$) to calculate the demand voltage of the VSC in current sampling period and then fed to a Space Vector Modulation (SVM). With a correct prediction of the current reference for the next sampling period, the demand voltage of the VSC can be determined to eliminate the tracking error in the current sampling period.

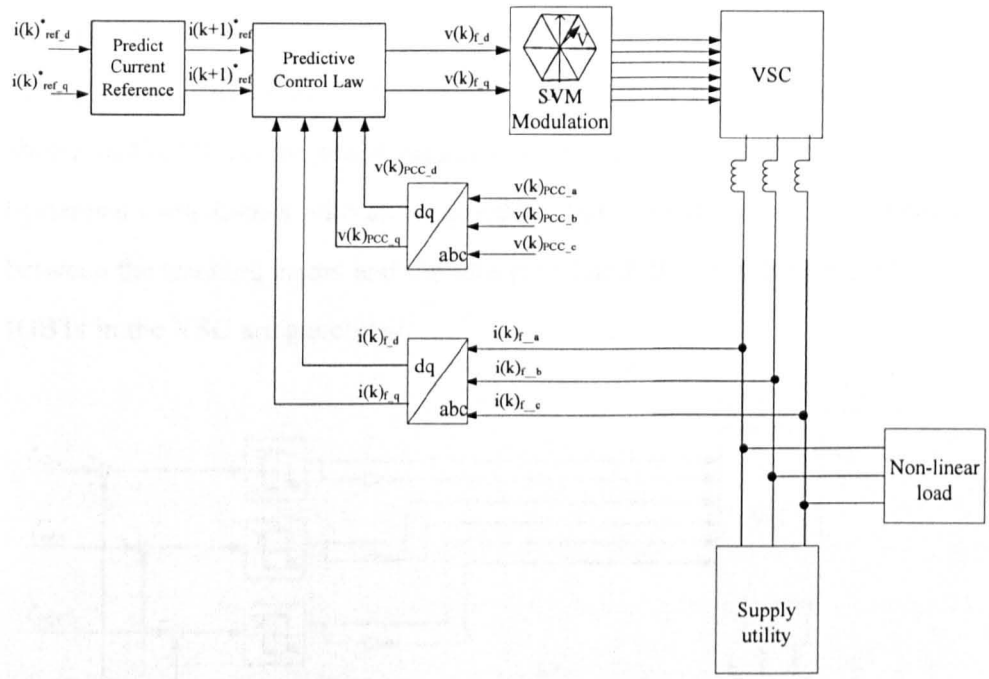


Figure 2. 7: Structure of the current loop in digital deadbeat control system

Being the deadbeat controller a model-based controller, its control performance is very sensitive to variations of the system parameter. Therefore, the accuracy of the system parameters determination is essential for the deadbeat controller design.

2.3.2 Non-linear control strategies

As mentioned earlier non-linear control approaches directly generate the switching signals for the switching devices in the VSC without PWM or SVM modulators.[61] Hence, one of the biggest benefits of using non-linear control strategies derives from its excellent control responses and its design independent on the system modal.[62, 63] However some implementation difficulties in practical systems can sometime prevent their use. In this section only hysteresis control will be introduced.

The hysteresis control strategy is the simplest and fastest non-linear control

strategy, whose application feasibility in the SAF current control system has been proved in literature [54]. The basic structure of the hysteresis control is shown in fig.2.8. As the name suggests, the hysteresis controllers are naturally hysteresis comparators with an assigned tolerance band. From the comparison between the tracking errors and the tolerance band, the switching signals of the IGBTs in the VSC are generated.

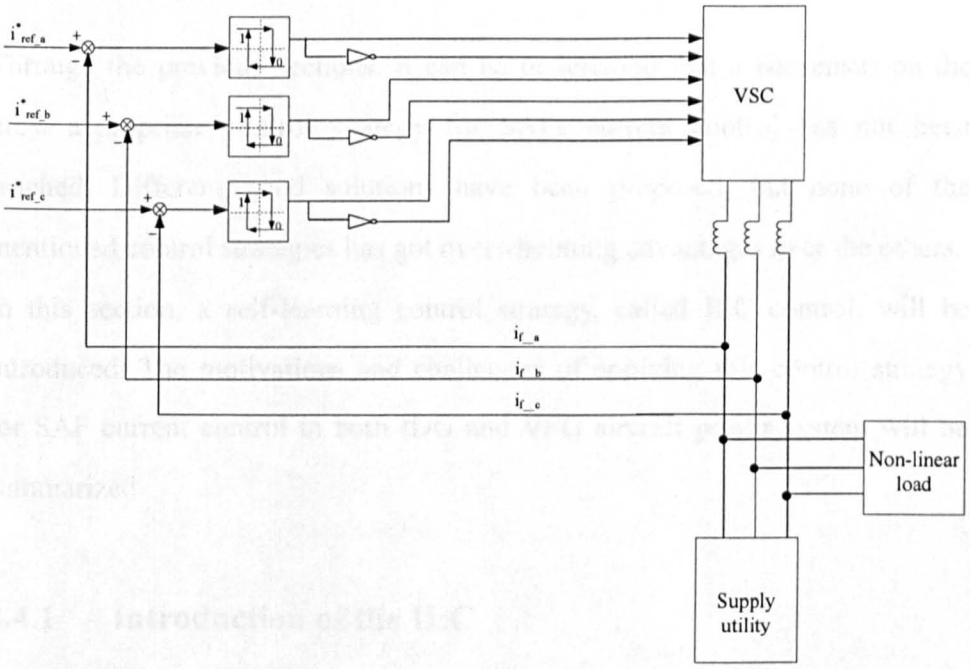


Figure 2. 8: The structure of the current loop in hysteresis control system

Due to the simplicity of the hysteresis control strategy, the SAF current control can be implemented also using analogue circuitry, where only one analog comparator and one logic gate are required for each phase, to compensate the tracking error under the interference between phases in 3-wires system. Hence the sampling and processing delay can be avoided and a very fast dynamic response can be achieved.

The main problem of the hysteresis controller derives from the fact that it produces a varying switching frequency for the VSC, which greatly depends on

its tolerance band, i.e., a smaller tolerance band results in a larger peak switching frequency, whereas a larger tolerance band leads to a larger tracking error. A compromise solution is needed in this case.

2.4 ILC current controlled SAF system in the aircraft power system

Through the previous sections, it can be understood that a consensus on the most appropriate control strategy for SAFs current control has not been reached. Different good solutions have been proposed, but none of the mentioned control strategies has got overwhelming advantages over the others. In this section, a self-learning control strategy, called ILC control, will be introduced. The motivations and challenges of applying this control strategy for SAF current control in both IDG and VFG aircraft power system will be summarized.

2.4.1 Introduction of the ILC

The ILC is a kind of linear self-learning control approach based on the internal modeling principle. [64, 65] The procedure of learning the tracking error from the previous period (called repetition in the ILC strategy) enables the ILC controller to adjust the control signal of the current repetition for the tracking error reduction. Therefore, a zero steady state tracking error within a finite number of repetitions can be achieved for a repetitive (periodic) signal.[66]

Based on the learning rules of ILC, the ILC controllers can be classified as follows: the Proportion (P) type, the Differential (D) type and the Proportion

plus Differential (PD) type. In this study, the P-type ILC controller will be adopted due to its simplest structure and design procedure. [64]

2.4.2 Motivations and challenges for P-type ILC application

As previously discussed, the existing SAF control strategies might not be able to fulfill the requirement of providing a reliable and very accurate current harmonics cancellation for the SAF system in the modern aircraft power systems for both high bandwidth and variable frequency operation requirements. Compared with the existing control strategies, research shows the P-type ILC provide the following advantages in other control applications:

- The P-type ILC controller can provide a zero steady state tracking error when the reference signal is periodic;
- As a wide-band controller, the P-type ILC controller can provide an accurate current tracking for all frequency components (from zero to Nyquist frequency);
- Simple design procedure;
- With a tolerable mismatch of the real system parameters, the P-type ILC controller still can provide a very accurate current tracking.[67, 68]

However the requirements for harmonic filters in the IDG and VFG power systems increase the difficulties of applying the P-type ILC controller for SAF current control. The main problem can be identified with the P-type ILC controller's sensitivity to current reference variations. As discussed in Section 2.2.2, the SAF system uses a cascade control structure, where the un-periodical demand current from outer voltage control loop during transients can cause a non-periodical variation to the current reference. Whereas the aircraft power

system requires a fast dynamic response for the SAF current control, even under extreme conditions such as jump from zero to full load. The load variation will cause an instant large variation in the SAF current reference, which could cause stability issues for the P-type ILC controlled SAF system. In addition, the frequency of the current reference can also vary in the VFG system due to the variation in the supply frequency, which is beyond the capabilities of the standard ILC control strategy. In this case the standard ILC control strategy fails in tracking the current reference.

In order to provide a very accurate current harmonic cancellation by using the P-type ILC controlled SAF system in both IDG and VFG power systems, the following issues are required to be investigated:

- Feasibility of applying the P-type ILC controller in a cascade control system;
- Stability and dynamic response of the control system under large load transient;
- Accurate current tracking under variable supply frequencies.

2.5 Conclusion

In this chapter, the suitability of SAFs application in aircraft power systems is investigated; their operation theory, current reference derivation methods and control structure are also presented. Due to the importance of the current control in SAF systems, a literature review of the existing current control strategies is investigated. However, conventional control methods cannot fully satisfy the requirements of an aircraft power system. Hence, the possibility, feasibility and challenge of applying an iterative learning controlled SAF in an aircraft power network has been discussed. The solutions to the presented

problem will be addressed in following chapters.

Chapter 3 Modeling and traditional synchronous reference frame control for Shunt Active Filters

3.1 Introduction

The first objective of this chapter is to determine the system model, including both system plant equations for the current control and DC voltage control, of the Shunt Active Filter (SAF). Since traditional PI and PID controllers have proven their weakness when applied to active filter current control [46, 47], in this chapter one of the most diffuse existing current control strategies for harmonic control, Proportional plus Resonant (P+resonant) control, will be applied in the SAF current control loop. Design considerations for both current and voltage control will be also presented in this chapter.

The SAF system model with the designed synchronous P+resonant current control and PI voltage control will be validated using the simulation tool (Matlab Simulink). Based on the simulation results, current reference tracking performance and dynamic response of the P+resonant controlled SAF system will be analyzed and discussed for compensation of specifically imposed current harmonics (5^{th}, 7^{th}, 11^{th} and 13^{th}).

3.2 The SAF system model

As discussed in Section 2.3, the overall SAF system control consists of an outer DC voltage and an inner current control loops. In order to maintain a constant DC voltage (V_{dc}) across the DC capacitor in a timescale of (1/400Hz), the outer DC voltage control loop produces a demand current (i_{dc}) to the inner

current control loop as the current reference. The current control loop produces a demand output voltage (v_f) to the Voltage Source Converter (VSC) to provide a controllable current flow (i_f) between the PCC and the VSC. In order to design the control of the DC voltage (V_{dc}) and of the output phase current of the SAF (i_f) by using traditional linear control strategies, the system equations for both outer DC voltage and inner current control plants are required.

3.2.1 System equations for the current control loop in the d-q rotating frame

The per-phase equivalent circuit of the SAF system connecting to a power network is shown in fig.3.1 (red rectangle).[69] The AC voltage source V_s represents the supply phase voltage; the AC voltage source V_f represents the phase output voltage of the VSC; R_l represents a variable non-linear load; L_f and R_f represent the phase inductance and its internal resistance between the PCC and VSC; i_f represents the output phase current of the SAF system. In addition, the system is designed under the assumption that the supply voltage and the supply current are in phase, hence the presence of the supply impedance is ignored.

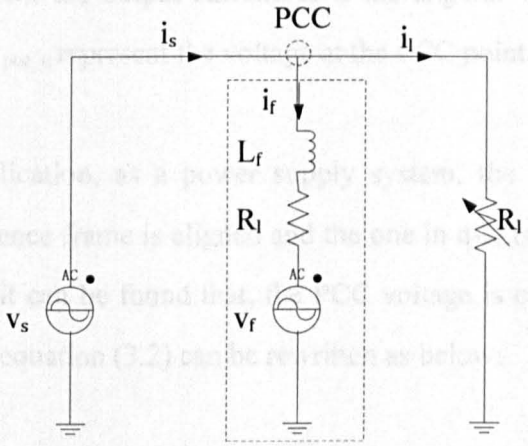


Figure 3. 1: Per-phase equivalent circuit of the SAF system

Based on this equivalent circuit, the voltage across each phase can be written down by using Kirchhoff's Law [42],

$$\begin{aligned} v_{pcc\_a} &= R_f i_{f\_a} + L_f \frac{di_{f\_a}}{dt} + v_{f\_a} \\ v_{pcc\_b} &= R_f i_{f\_b} + L_f \frac{di_{f\_b}}{dt} + v_{f\_b} \\ v_{pcc\_c} &= R_f i_{f\_c} + L_f \frac{di_{f\_c}}{dt} + v_{f\_c} \end{aligned} \tag{3.1}$$

As discussed in section 2.3.1.4, the use of a d-q rotating frame, halves the number of resonant controllers needed. Hence the current control loop of the SAF system will be designed in the d-q rotating frame. By using the coordinate transformations given in Appendix A, eq. (3.1) can be rewritten in the d-q frame synchronous with the supply frequency:

$$\begin{aligned} v_{pcc\_d} &= R_f i_{f\_d} + L_f \frac{di_{f\_d}}{dt} - \omega L_f i_{f\_q} + v_{f\_d} \\ v_{pcc\_q} &= R_f i_{f\_q} + L_f \frac{di_{f\_q}}{dt} + \omega L_f i_{f\_d} + v_{f\_q} \end{aligned} \tag{3.2}$$

Under the d-q rotating frame, v_{f_d} and v_{f_q} represent the VSC output voltage; i_{f_d} and i_{f_q} represent the output current; ω is the angular velocity of the d-q frame; v_{pcc_d} and v_{pcc_q} represent the voltage at the PCC point.

Since in this application, as a power supply system, the supply voltage in d-axis of the reference frame is aligned and the one in q-axis can be neglected. Through fig. 3.1, it can be found that, the PCC voltage is equal to the supply voltage; therefore equation (3.2) can be rewritten as below:

$$v_{pcc\_d} = R_f i_{f\_d} + L_f \frac{di_{f\_d}}{dt} - \omega L_f i_{f\_q} + v_{f\_d}$$
$$0 = R_f i_{f\_q} + L_f \frac{di_{f\_q}}{dt} + \omega L_f i_{f\_d} + v_{f\_q} \tag{3.3}$$

In order to control the current i_f, the demand voltage for the VSC has to be evaluated as:

$$v_{f\_d} = -(R_f i_{f\_d} + L_f \frac{di_{f\_d}}{dt}) + (\omega L_f i_{f\_q} + v_{pcc\_d})$$
$$v_{f\_q} = -(R_f i_{f\_q} + L_f \frac{di_{f\_q}}{dt}) - \omega L_f i_{f\_d} \tag{3.4}$$

By defining,

$$v^*_{f\_d} = R_f i_{f\_d} + L_f \frac{di_{f\_d}}{dt}$$
$$v^*_{f\_q} = R_f i_{f\_q} + L_f \frac{di_{f\_q}}{dt} \tag{3.5}$$

Substituting eq.(3.5) in to eq.(3.4), the following equation can be obtained,

$$v_{f\_d} = -v^*_{f\_d} + (\omega L_f i_{f\_q} + v_{pcc\_d})$$
$$v_{f\_q} = -v^*_{f\_q} - \omega L_f i_{f\_d} \tag{3.6}$$

Through eq. (3.6), it can be found that, the demand voltage for the VSC in both d axis and q axis contains two parts: the output signals from the current controller ($v_{f\_d}^*$ in d-axis of the reference frame and $v_{f\_q}^*$ in q-axis of the reference frame) and the compensation components ($\omega L_f i_{f\_q} + v_{pcc\_d}$ in d-axis of the reference frame and - $\omega L_f i_{f\_d}$ in q-axis of the reference frame). Considering eq. (3.5), the control plant of the SAF current control loop can be derived as follows:

$$\frac{i_{f\_d}(s)}{V^{*}_{f\_d}(s)} = \frac{i_{f\_q}(s)}{V^{*}_{f\_q}(s)} = \frac{1}{L_f s + R_f} \tag{3.7}$$

3.2.2 System equations for DC voltage control loop

In order to maintain a constant (under a timescale of 1/400Hz) regulated voltage across the DC capacitor in the VSC, the current feeding the DC capacitor has to be controlled. The equivalent circuit for the DC link is shown in fig.3.2, where, V_{dc} represents the voltage of the DC capacitor, i_{dc} represents the current flowing at the DC side of the VSC. [69]:

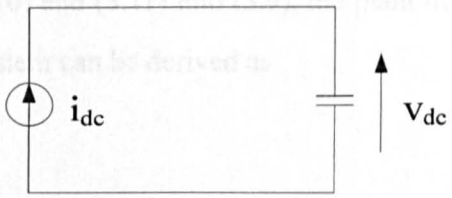


Figure 3. 2: Equivalent circuit of the DC link

Neglecting the losses of the VSC, the power drawn by the DC capacitor can be written in d-q rotating frame as follows:

$$V_{dc} i_{dc} = \frac{3}{2}(i_{f\_d} v_{pcc\_d} + i_{f\_q} v_{pcc\_q}) + i_{f\_0} v_{PCC\_0} \tag{3.8}$$

Since the d-axis of the reference frame is aligned with the PCC voltage vector, the value of v_{pcc}_q can be neglected. Hence, eq.(3.8) can be rewritten as follows:

$$V_{dc} i_{dc} = \frac{3}{2} i_{f\_d} v_{pcc\_d} \tag{3.9}$$

Through the equivalent circuit shown in fig.3.2, the relationship between v_{dc}

and i_{dc} can be obtained as,

$$i_{dc} = C\frac{dv_{dc}}{dt} \tag{3.10}$$

The PWM modulation index can be defined in this case as [39]:

$$m = \frac{2v_{pcc\_d}}{v_{dc}} \tag{3.11}$$

Substituting eq.(3.10) and (3.11) into (3.9), the plant of the DC voltage control loop in the SAF system can be derived as

$$\frac{v_{dc}(s)}{i_{f\_d}(s)} = \frac{3m}{4Cs} \tag{3.12}$$

3.2.3 The overall structure of the SAF system control

Based on the system equations derived in Section 3.2.1 and 3.2.2, the overall control structure of the SAF system can be determined as shown in fig.3.3 and controllers can be designed.

The line-to-line PCC voltages are measured and converted into the stationary α-β reference frame, to determine the instantaneous angle θ of the supply frequency (by using a PLL). This instantaneous angle θ is then used to convert the measured SAF output phase current (i_f) to the d-q frame rotating at the fundamental frequency. The current control loop in d-q rotating frame strictly follows the system equations derived in Section 3.2.1. The errors between the

demand and measured current in the d and q axis are fed into two P+resonant controllers respectively. The demand voltages ($v_{f\_d}^*$ and $v_{f\_q}^*$) produced by the P+resonant controllers are coupled with the decoupling components ($\omega L_f i_{f\_q}+v_{pcc\_d}$ and - $\omega L_f i_{f\_d}$) as presented in eq.(3.6). The coupled demand voltages in d and q axis are then converted to three phase voltages (v_{f_a}, v_{f_b} and v_{f_c}) by using a d-q to a-b-c transformation. Finally, these demand phase voltage pass through a modulating signal for the PWM to generate the switching signals of the IGBTs.

As shown in fig.3.3, in the SAF DC voltage control, the error between the demand DC voltage and the measured one is fed into a PI controller. As presented in eq.(3.2), the DC voltage (V_{dc}) depends on the current flow in the d axis (i_{f_d}). Hence the output demand current (i_{dc}^*) of the PI controller is added to the current harmonic reference in the d axis (i_{h_d}), as the fundamental current reference of the current control loop on the d axis. [47]

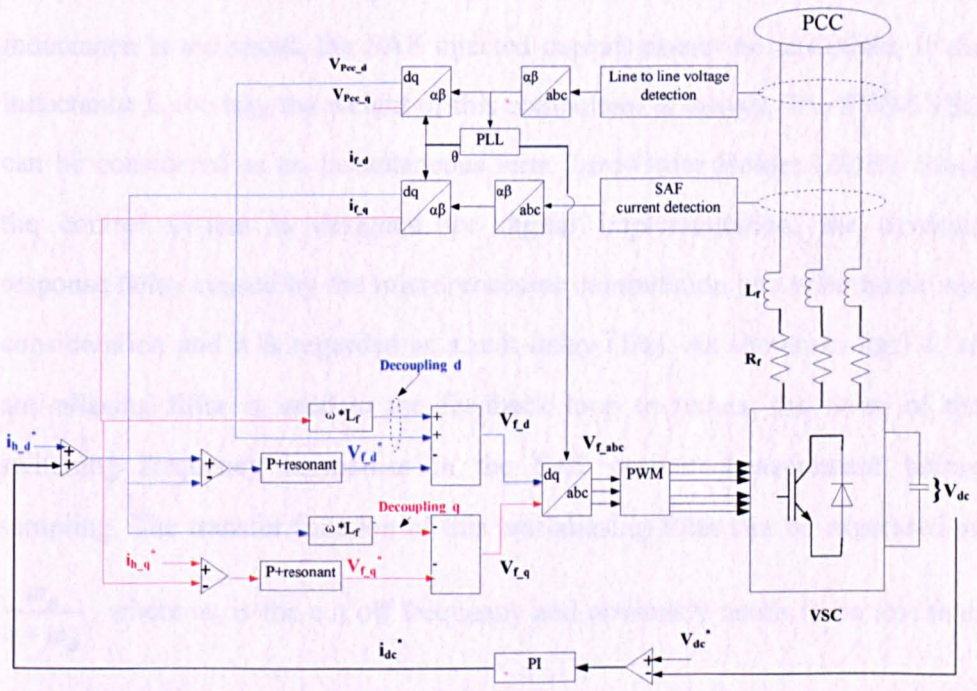


Figure 3. 3: Overall control structure of the SAF system in the d-q rotating frame

3.3 The control design

As discussed in Section 2.3.1.4, P+resonant type controllers are used in the inner current control loop, and a standard PI controller is applied in the outer voltage control loop. In this section, the design procedures and discussions about the P+resonant controllers and the PI controller will be analyzed and presented respectively.

3.3.1 The synchronous P+resonant current control

The block schematic of the SAF current control loop in the discrete domain is shown in fig.3.4.The supply impedance is usually ignored in the design (see it in Section 3.2.1). The active filter inductance (L_f) and internal resistance (R_f) used in this design are set to be 1mH and 0.15Ω respectively, with a compromise between the weight and performance of the SAF device (i.e. if the inductance is too small, the SAF injected current cannot be smoothed; if the inductance is too big, the weight of this component is heavy). The PWM VSC can be considered as an instantaneous term Zero-Order Holder (ZOH). Since the control system is designed for digital implementation, the dynamic response delay caused by the microprocessor computation has to be taken into consideration and it is regarded as a unit delay (1/z). As shown in fig.3.4, an anti-aliasing filter is used in the feedback loop to reduce the noise of the switching frequency harmonics in the SAF current measurement before sampling. The transfer function of this anti-aliasing filter can be expressed as $\frac{\omega_a}{s+\omega_a}$, where ω_a is the cut off frequency and obviously needs to be less than the Nyquist frequency. [70, 71] In this application, the sampling frequency is set to be 48000Hz to accurately describe the current and voltage measurements, while the cut off frequency of the anti-aliasing filter is chosen to be 24000Hz

($1.5x10^5$ rad/s).

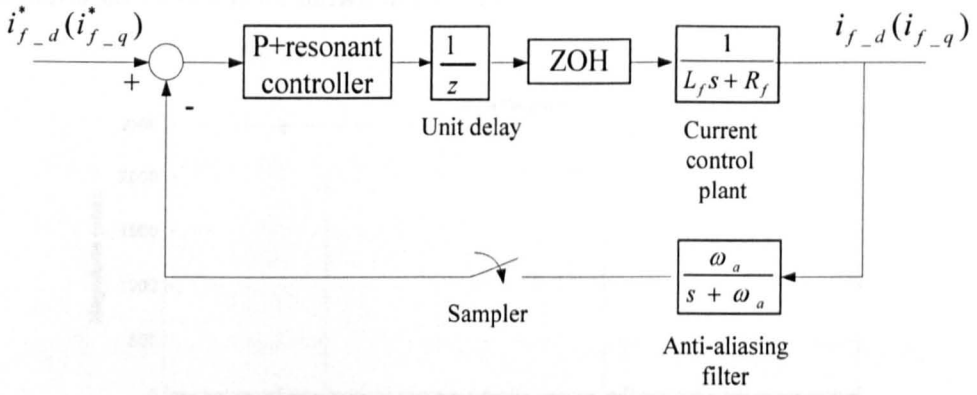


Figure 3. 4: SAF current control loop block scheme

As presented in the Section 2.4.1.3, the P+resonant controller can provide a very small steady state tracking error due to its designed high gain at the specified harmonic frequencies. In this application the current reference consists of the 5^{th}, 7^{th}, 11^{th} and 13^{th} harmonic components. As presented in Appendix A, in the d-q frame rotating at the supply frequency of 400Hz, the 5^{th} and 7^{th} harmonic components both appear as 2400Hz AC components. Similarly, the 11^{th} and 13^{th} harmonic components appear as 4800Hz AC components. Therefore, the P+resonant controller is designed to provide a high gain at 2400Hz and 4800Hz to achieve a small steady state tracking error for the 5^{th}, 7^{th}, 11^{th} and 13^{th} current harmonics. The transfer function of the P+resonant controller is hence given by [72],

$$C_{current}(s) = K_p + \frac{K_{r\_1}(\omega_1/Q_1)s}{s^2 + (\omega_1/Q_2)s + \omega_1^2} + \frac{K_{r\_2}(\omega_2/Q_2)s}{s^2 + (\omega_2/Q_2)s + \omega_2^2} \quad (3.13)$$

Where, the K_p represents the proportional gain, K_{r_1} and K_{r_2} represent the gains of each resonant term, Q_1 and Q_2 represent the quality factor of each resonant term, ω_1 and ω_2 represent the resonant frequencies. Assuming the

resonant frequencies equal the frequencies of the harmonic components, i.e. $\omega_1=2*2400\pi$ and $\omega_2=2*4800\pi$, the P+resonant controller provides high gains at 2400Hz and 4800Hz as shown in fig. 3.5.

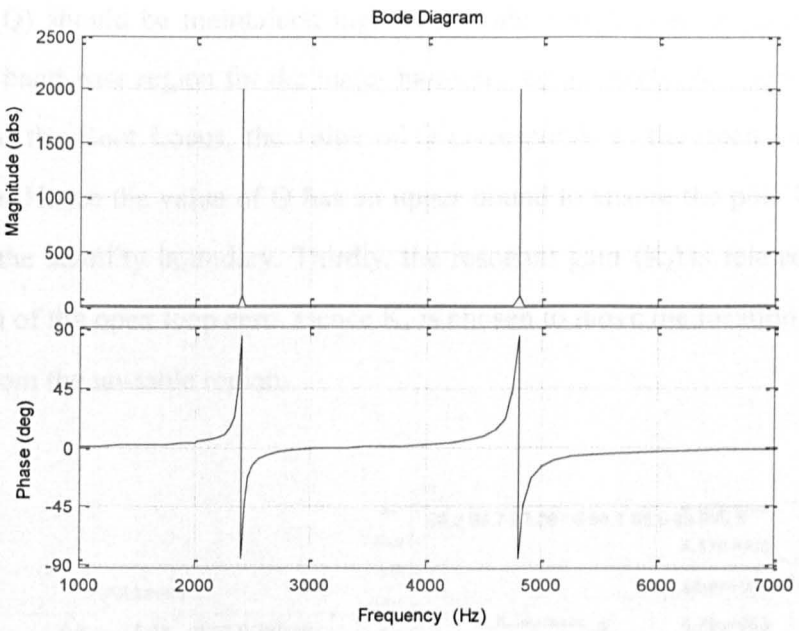


Figure 3. 5: Bode plot of the P+resonant controller with resonant frequencies of 2400Hz and 4800Hz

After the determination of the resonant frequencies, the design of the P+resonant controller still requires more considerations on the other controller parameters i.e. K_p, Q_1, Q_2, K_{r_1} and K_{r_2}. As shown in fig.3.5, the P+resonant controller can be considered as a band-pass filter. The proportional gain (K_p) determines the magnitude of the controller at all frequencies; the quality factors (Q_1 and Q_2) are related to the peak magnitudes and band-pass regions of the P+resonant controller; the resonant gains (K_{r_1} and K_{r_2}) are related the gains of the resonant frequencies. The performance of the P+resonant controller actually depends on the proper determination of these parameters. [39]

The controller parameters design methodology is presented in fig.3.6 showing

a Root Locus of the closed loop current control system of fig.3.4. Firstly, the proportional gain (K_p) will determine the location of the closed loop poles. Hence K_p has to be selected to maximize the distance between the closed loop poles and the stability boundary (the unit circle). Secondly, the value of quality factor (Q) should be maintained high to provide a high peak magnitude and narrow band-pass region for the major harmonic components. As shown in the zoom of the Root Locus, the value of Q corresponds to the open loop pole location. Hence the value of Q has an upper bound to ensure the pole location within the stability boundary. Thirdly, the resonant gain (K_r) is related to the location of the open loop zero. Hence K_r is chosen to move the location of zero away from the unstable region.

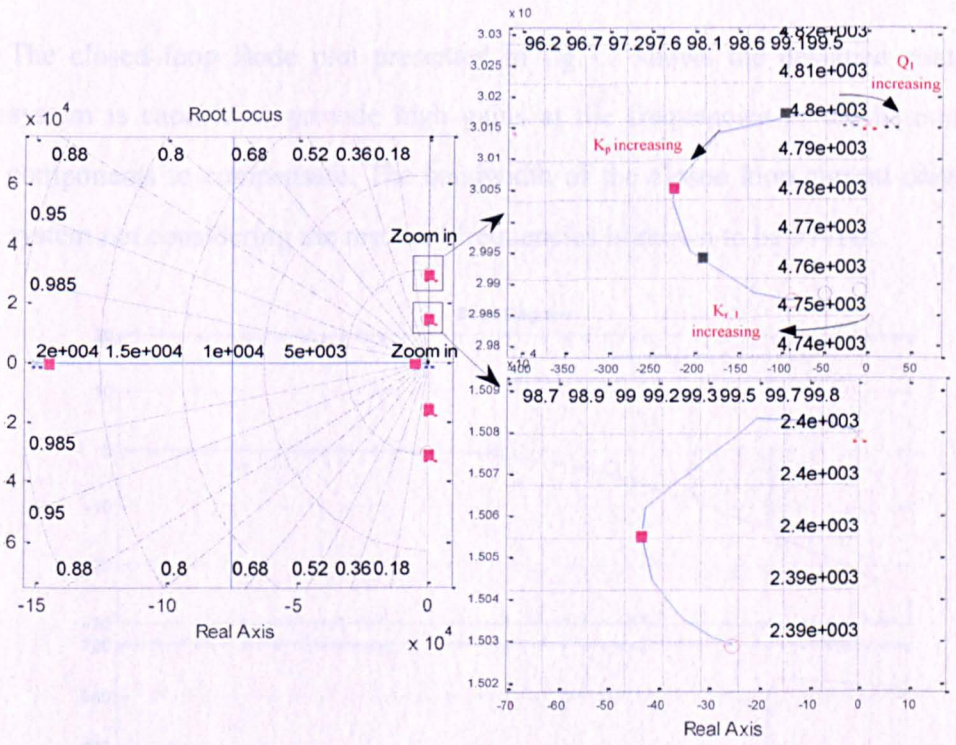


Figure 3. 6: Root Locus of the closed loop P+resonant current control

With a careful tuning and compromise choices, the parameters of the resonant controller are designed as in tab.3.1.

Table 3. 1: Parameters of the P+resonant controller

ω_1	ω_2	K_p	Q_1	Q_2	K_{r_1}	K_{r_2}
15079	30159	5	20000	2000	2000	3000

In addition, since the ratio between the sampling frequency and the current loop natural frequency is higher than 15, the designed P+resonant controller can be directly converted to the discrete domain. The transfer function of the controller in z-domain is given in eq. (3.14).

$$P_{current}(z) = \frac{5z^4 - 17.42z^3 + 24.88z^2 - 17.09z + 4.822}{z^4 - 3.52z^3 + 5.078z^2 - 3.52z + 0.9999} \tag{3.14}$$

The closed loop Bode plot presented in fig.3.7 shows the designed control system is capable to provide high gains at the frequencies of the harmonic components to compensate. The bandwidth of the closed loop current control system not considering the resonant frequencies is shown to be 917Hz.

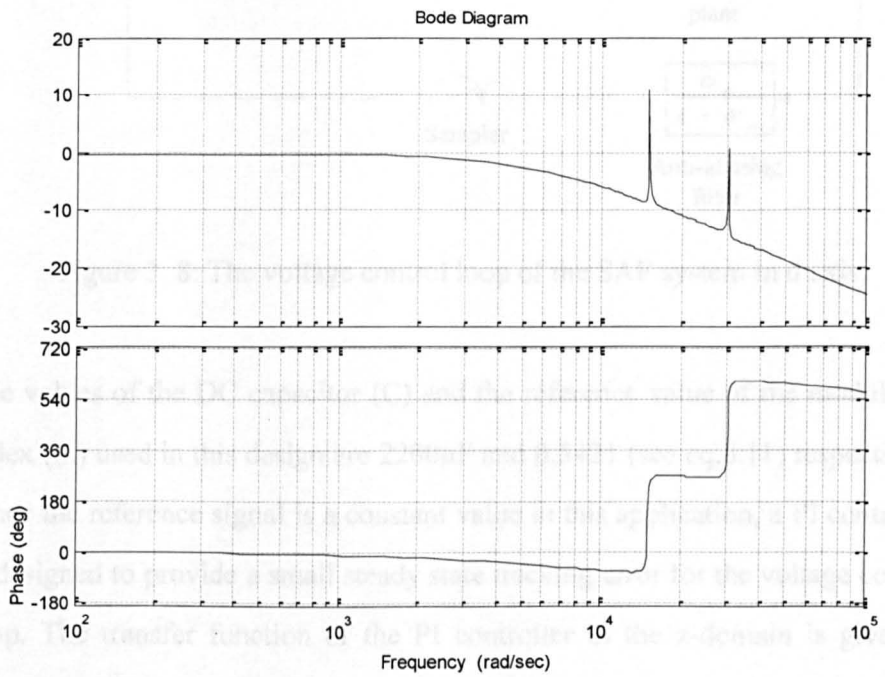


Figure 3. 7: Closed loop Bode plot of the designed current control system

3.3.2 PI control design for the DC voltage loop

As discussed in Section 3.2.3, the voltage control loop is cascaded to the current control loop on the d axis, which indicates that the dynamics of the current control loop can affect the performance of the voltage control loop. Theoretically, the voltage control loop should be designed to provide a much lower bandwidth than the current control loop (i.e. usually the closed loop bandwidth of the outer voltage control loop is 10% of the closed loop of the inner current control loop). Thus the dynamics of the current control loop can be ignored in the design of the voltage control loop. The block scheme of the SAF voltage control loop in the discrete domain is shown in fig.3.8.

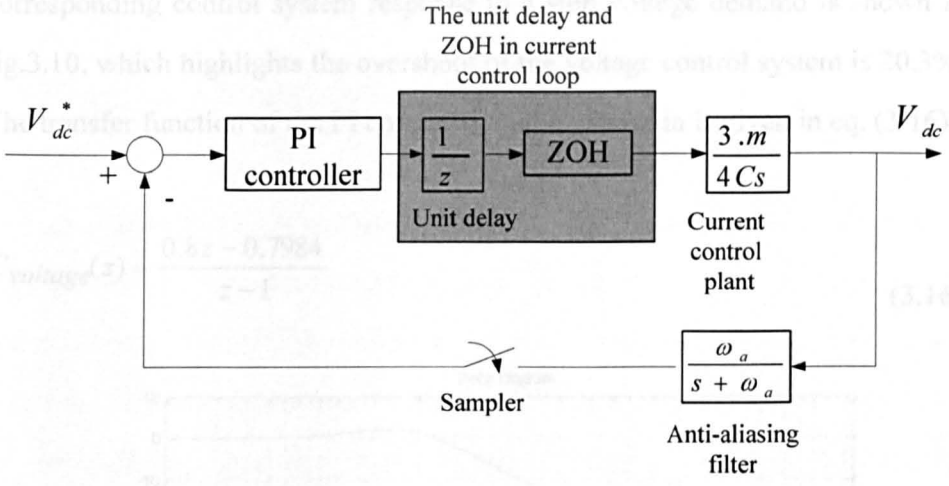


Figure 3. 8: The voltage control loop of the SAF system in d axis

The values of the DC capacitor (C) and the reference value of the modulation index (m) used in this design are 2200μF and 0.5421 (see eq.3.11) respectively. Since the reference signal is a constant value in this application, a PI controller is designed to provide a small steady state tracking error for the voltage control loop. The transfer function of the PI controller in the z-domain is given as follows,

$$P_{voltage}(z) = \frac{K_1 z + K_2}{z - 1} \tag{3.15}$$

For any PI controller design, the design specifications are needed, usually translating in values for the closed loop bandwidth and the damping factor. The upper bound of the voltage control loop bandwidth is chosen to be 10% of the one of the current control loop.[69, 73] As analyzed in the previous section, the bandwidth of the current control loop is 917Hz, which means the bandwidth of the voltage control loop should be less than 91Hz to minimize the influence of the current control loop. The damping factor is selected to be 0.7 in this design to provide a suitable damping for the control system.[71] As shown in fig.3.9, the designed closed loop control system has a bandwidth of 90Hz. The corresponding control system response to a step voltage demand is shown in fig.3.10, which highlights the overshoot of the voltage control system is 20.3%. The transfer function of the PI controller in the z-domain is given in eq. (3.16).

$$C_{voltage}(z) = \frac{0.8z - 0.7984}{z - 1} \tag{3.16}$$

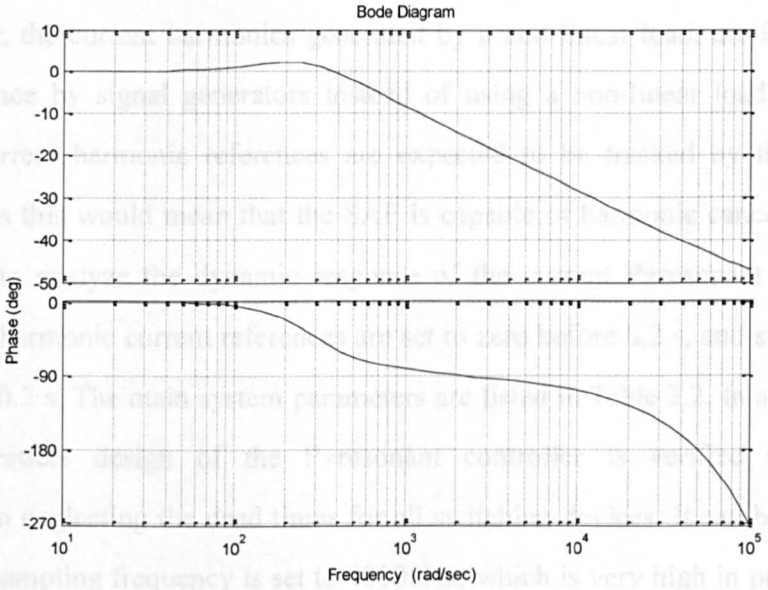


Figure 3. 9: Close loop Bode plot of the designed voltage control system

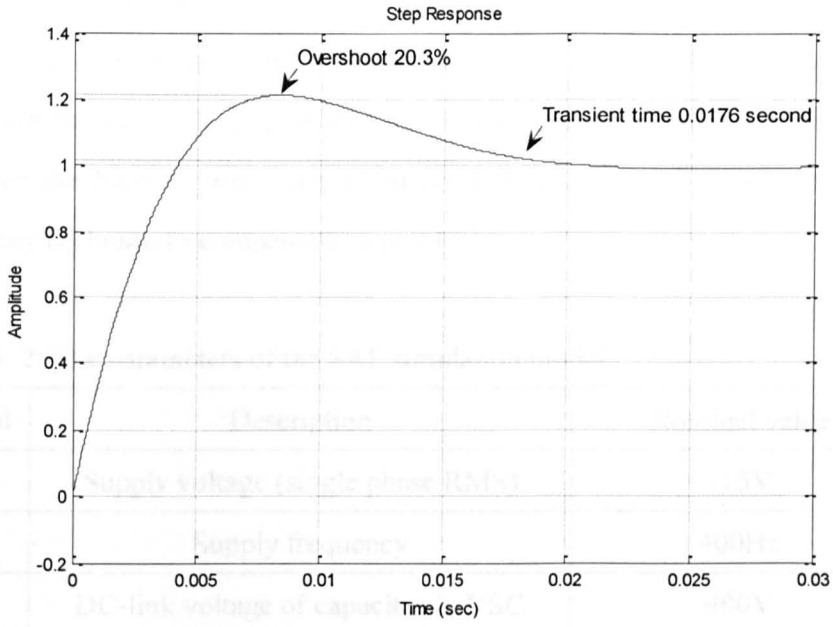


Figure 3. 10: Closed loop unit step response

3.4 Simulation model and results

The simulation software Matlab/Simulink including the Simpower Blockset is used to model the 400Hz SAF system presented in fig.3.3. In order to independently analyze the current reference tracking of the P+resonant controller, the current harmonics generated by a non-linear load, are imposed as reference by signal generators instead of using a non-linear load model. These current harmonic references are expected to be tracked by the SAF system, as this would mean that the SAF is capable of harmonic cancellation. In order to analyze the dynamic response of the current P+resonant control loop, the harmonic current references are set to zero before 0.2 s, and switched to full at 0.2 s. The main system parameters are listed in Table 3.2. In addition, the theoretical design of the P+resonant controller is verified through simulation neglecting the dead times for all switching devices. It can be found that, the sampling frequency is set to 48000Hz, which is very high in practical. It is because the closed loop gain of the current loop with the P+resonant

controller attenuate fast when it closed to the Nyquist frequency as presented in fig. 3.7 (i.e. a small sampling frequency leads to a small Nyquest frequency, and hence the closed loop gain will be too small to compensate the tracking error for the higher order current harmonics). Therefore, a large sampling frequency is chosen to compensate is problem.

Table 3. 2: The parameters of the SAF simulation model

Symbol	Description	Nominal value
V_s	Supply voltage (single phase RMS)	115V
F	Supply frequency	400Hz
V_{DC}	DC-link voltage of capacitor in VSC	400V
C_{DC}	DC capacitance	2200μ F
L_f	Filter input inductance	1mH
R_f	Filter input resistance	0.15Ω
F_s	Sampling frequency	48000Hz
F_{sw}	Switching frequency	48000Hz
I_{5th}, I_{7th}	Current reference of 5^{th} and 7^{th} harmonic	2A
I_{11th}, I_{13th}	Current reference of 11^{th} and 13^{th} harmonic	3A,1A

Two parameters are defined as follows and used for the performance evaluation of the simulation results.

- Average tracking error (ATE): sum of the absolute values of tracking errors at each sampling time in one repetition (cycle) divided by the number of samples in one repetition;
- Maximum tracking error (MTE): maximum absolute value among tracking errors at each sampling time in one repetition;

Figure 3.11 shows the DC voltage response of the SAF outer voltage control. As shown the actual DC voltage tracks its reference properly. Figure 3.12 shows the steady state current tracking of the P+resonant controlled SAF system in the d and q axis respectively. As shown, the ATE and MTE are 0.0731A and 0.2515A respectively in the d axis, and the ATE and MTE are 0.0629A and 0.2428A respectively in the q axis. The simulation results prove the capability of the P+resonant controllers, in the SAF current control loop, of providing an accurate current reference tracking in both d and q axis. The steady state tracking error shown in fig. 3.12 is caused by the small closed loop gain at the frequency of the high order current harmonics (11^{th} and 13^{th}).

Figure 3.13 shows the comparison between the actual SAF output phase current and its current reference which contains the 5^{th}, 7^{th}, 11^{th} and 13^{th} current harmonic components after the anti-aliasing filtering which attenuates the switching harmonics. It can be found, that the P+resonant controller approach can provide a good current control of the 5^{th}, 7^{th}, 11^{th} and 13^{th} current harmonics, where the ATE is 0.1217A and the MTE is 0.3183A.

Figure 3.14 shows the dynamic response of the SAF system, when a load transient (from zero load to full) appears at 0.2 s. It is clear that the dynamic performance of the P+resonant controller is satisfactory, since it take only around 0.004 s to achieve the steady state condition.

The simulation results show that, in the SAF current control system, the P+resonant controllers is capable of providing a good current tracking for the indicated harmonic references. In addition, when a load transient occurs, the proposed SAF provides a good dynamic response.

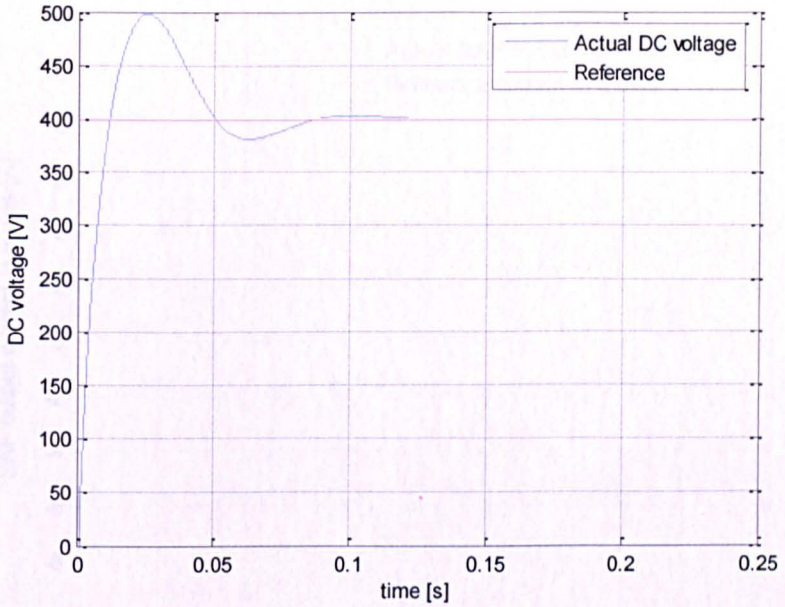


Figure 3. 11: Actual and reference SAF DC voltage

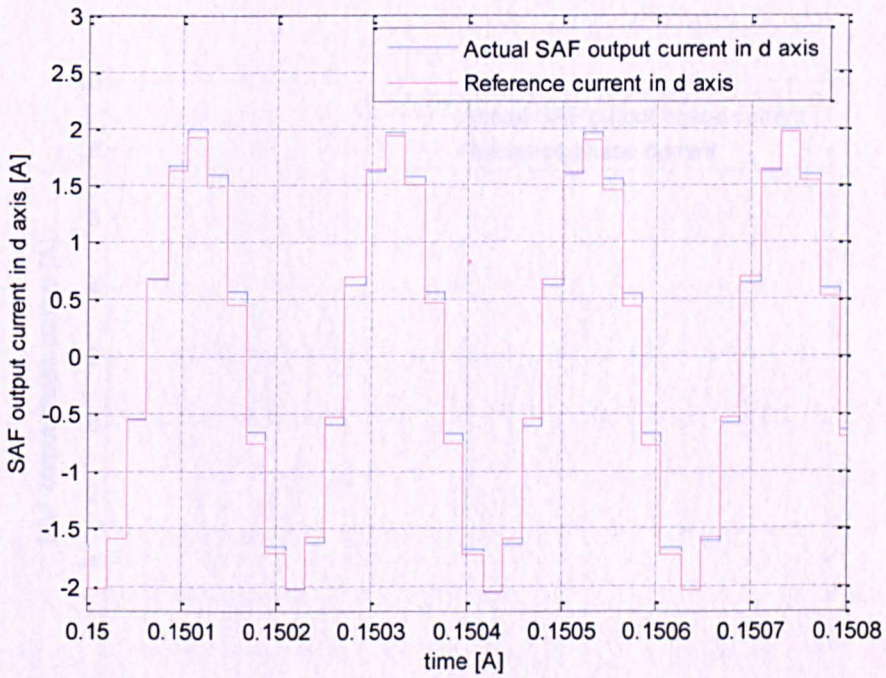


Figure 3. 12a: Actual and reference SAF output currents on the d axis.

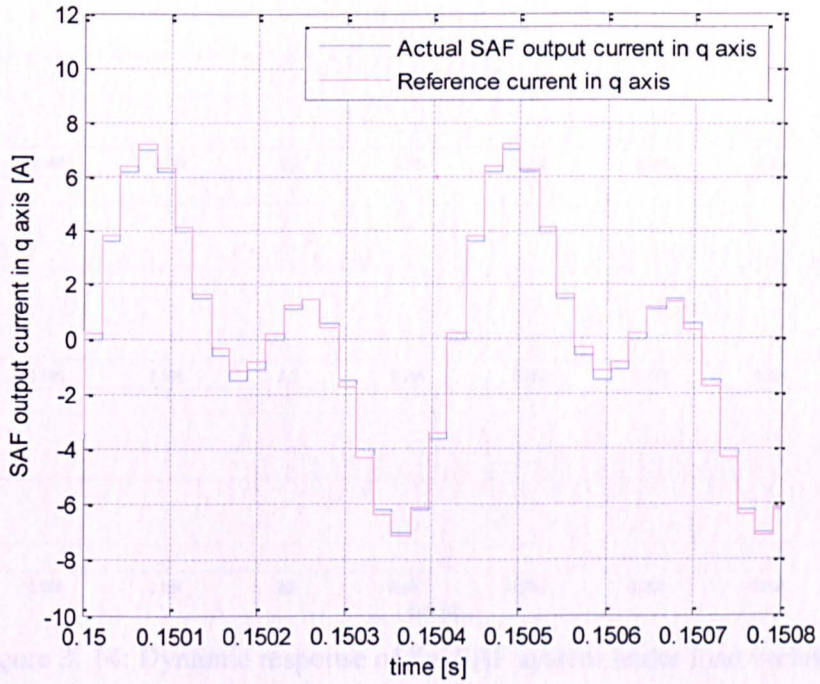


Figure 3.12b: Actual and reference SAF output currents on the q axis.

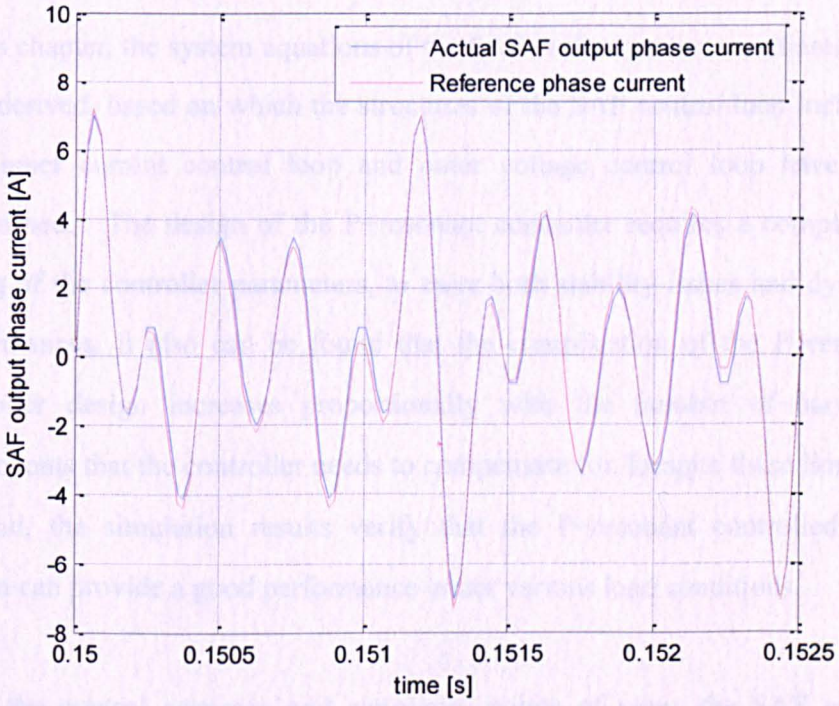


Figure 3. 13: Actual and reference SAF output currents on the q axis.

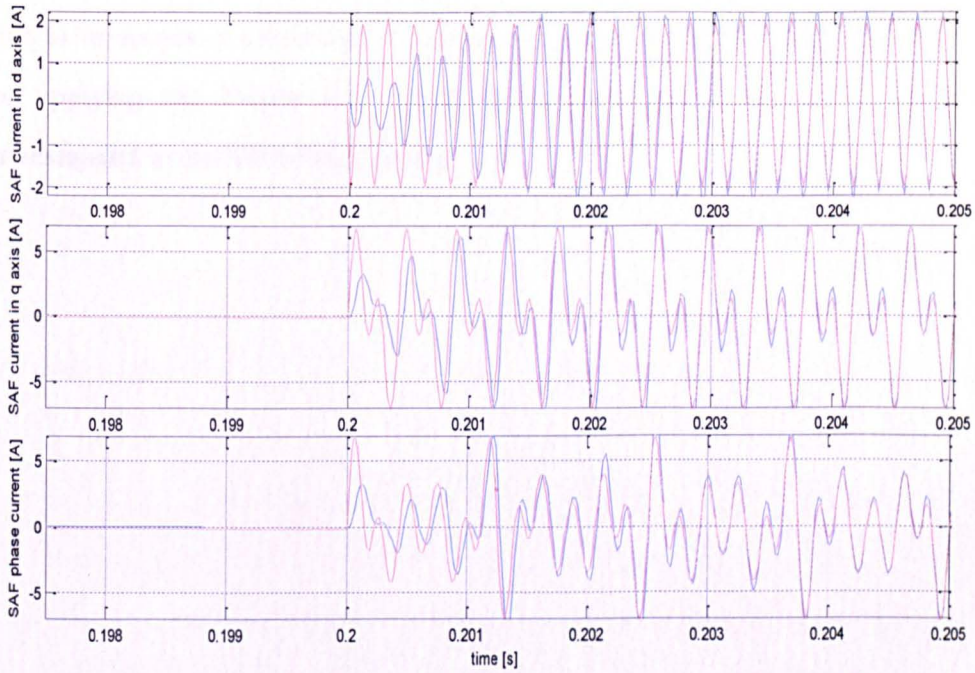


Figure 3. 14: Dynamic response of the SAF system under load variation

3.5 Conclusion

In this chapter, the system equations of the SAF in the synchronous frame have been derived, based on which the structures of the SAF control loop including both inner current control loop and outer voltage control loop have been determined. The design of the P+resonant controller requires a complicated tuning of the controller parameters, to cater both stability issues and dynamic performances. It also can be found that the complication of the P+resonant controller design increases proportionally with the number of harmonic components that the controller needs to compensate for. Despite these limits, in the end, the simulation results verify that the P+resonant controlled SAF system can provide a good performance under various load conditions.

From the control accuracy and simplicity points of view, the SAF system requires however a better current control strategy. As discussed in Chapter 2, the P-type ILC controller is a replacement to the resonant controller approach,

due to its simple structure and design procedure. The feasibility and suitability of applying the P-type ILC controller for SAF current control will be investigated in the following chapter.

Chapter 4 Introduction and robustness analysis of P-type ILC

4.1 Introduction

The previous chapter has demonstrated the small tracking error capability of the P+resonant controlled SAF system. However the design procedure of this type of controller is complex. In addition, the P+resonant controller can only compensate a limited number of harmonic components. From the control accuracy, simplicity and robustness points of view, the SAF system requires a more suitable control method rather than the P+resonant controller. Therefore, a method based on Iterative Learning Control (ILC) approach is introduced in this chapter. Compared with other types of ILC controllers, the one called Proportional (P) type ILC is selected in this research due to its simple structure and design.[65, 74]

In this chapter, the principle of the P-type ILC will be given, followed by the definition of the error decay condition, which is used to determine the learning gain of the P-type ILC controller for each specific control case.

Since the P-type ILC controlled SAF system in this project is designed for aircraft applications, it requires the control system proving a high robustness against disturbances. In addition, using the P-type ILC controller for the inner loop of cascaded control systems goes theoretically against the basic condition of ILC application, since in transient conditions the output of the outer loop representing the reference of the inner one is not a periodical waveform. Anyway, this chapter will prove, by using rigorous mathematical analysis, the

robustness of the P-type ILC system against bounded disturbances and the non-periodical reference caused by the voltage control loop. Hence the feasibility of applying the P-type ILC control for SAF system can be theoretically proved.

4.2 The principle of the P-type ILC and the error-decay condition

As presented in Chapter 2, the P-type ILC is an intelligent control structure which can be applied for the regulation of system operation under a repeated reference signal. This control method has already been applied in inverter control systems [66], robot manipulator control systems [74, 75] and other non-linear control systems [65][76-78]; in these applications the structural simplicity and operational performances of the ILC method are shown.

Fig 4.1 shows the basic concept of the P-type ILC controller in discrete domain, where e is the tracking error, u is the output control signal of the P-type ILC, y is the output signal of the control plant, y_d is the reference signal; the subscript k represents the k^{th} repetition (cycle) of the repetitive system. Through fig. 4.1, it can be seen that, the P-type ILC delays the tracking error $e_k(z)$ and control signal $u_k(z)$ for one repetition by using two memories (certain numbers of discrete delays in discrete domain) respectively, and then the P-type ILC learns the tracking error from the previous repetition $e_{k-1}(z)$ and uses a learning update algorithm to adjust the control signal $u_k(z)$ in the current repetition to reduce the tracking error.

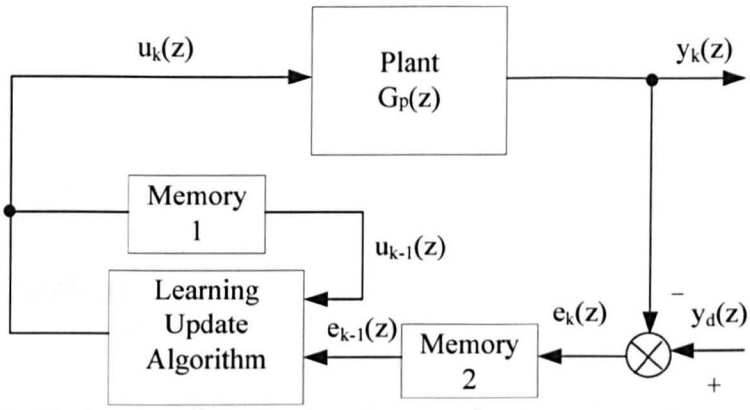


Figure 4. 1: Concept and structure of P-type ILC

In a single-input and single-output system, the P-type ILC can be used to limit the tracking error, if the system satisfies the following conditions,

A1) The reference signal is repetitive;

A2) The system variables have the same initial condition in each repetition;

A3) The offsets and noise of the output are zero;

A4) The system dynamics is invariant. [65, 66]

The form of a simple learning update algorithm used in the P-type ILC controller can be represented by,

$$u_k(z) = u_{k-1}(z) + L(z)e_{k-1}(z) \tag{4.1}$$

Where L(z) is called the learning factor of the learning update algorithm (in discrete domain). As presented in eq. (4.1), the control signal in each time step $u_k(z)$ is derived by summing the control signal in previous repetition and the tracking error in previous repetition weighted by a learning factor. Based on the structure of the P-type ILC control loop show in fig 4.1, the error $e_k(z)$ between

the actual output and the reference, and the output $y_k(z)$ of the plant are given as follows,

$$e_k(z) = y_d(z) - y_k(z) \tag{4.2}$$

$$y_k(z) = G_p(z)u_k(z) \tag{4.3}$$

Where $G_p(z)$ is the discrete domain transfer function of the plant. By combining eq. (4.1), (4.2) and (4.3), the tracking error for the k^{th} repetition can be derived as,

$$\begin{aligned} e_k &= y_d(z) - G_p(z)u_k(z) \\ &= y_d(z) - G_p(z)(u_{k-1}(z) + L(z)e_{k-1}(z)) \\ &= y_d(z) - G_p(z)u_{k-1}(z) - G_p(z)L(z)e_{k-1}(z) \end{aligned} \tag{4.4}$$

Based on eq. (4.3), eq. (4.4) can be rewritten as,

$$e_k(z) = y_d(z) - y_{k-1}(z) - G_p(z)L(z)e_{k-1}(z) \tag{4.5}$$

As presented in condition A1, the reference signal $y_d(z)$ is the same in each repetition; therefore equation (4.5) can be rewritten as:

$$\begin{aligned} e_k(z) &= e_{k-1}(z) - G_p(z)L(z)e_{k-1}(z) \\ &= (1 - G_p(z)L(z))e_{k-1}(z) \end{aligned} \tag{4.6}$$

Through eq. (4.6), it can be found that, the tracking error will decay over successive repetitions if,

$$\left|1 - G_p(e^{j\omega T_s})L(e^{j\omega T_s})\right| < 1 \qquad -\pi \le \omega T_s \le \pi \tag{4.7}$$

The eq. (4.7) is called the error-decay condition, where the T_s represents the sampling period; $\left|1-G_p(e^{j\omega T_s})L(e^{j\omega T_s})\right|$ is called error-decay factor, where T_s is the sampling frequency of the control system. $L(e^{j\omega T_s})$ is called learning factor which includes two components: learning gain and phase shift component.[79]

It can be found in eq. (4.6) that the error decay speed of the system is determined by the error-decay factor. If the error-decay factor is closer to zero, the tracking error can be decayed to a smaller value in one repetition. Therefore, the value of learning factor ($L(e^{j\omega T_s})$) can be determined by imposing fast tracking error decay (error-decay factor close to zero).

4.2.1 Determination of the learning factor based on error-decay condition

The error-decay condition in eq. (4.7) must be satisfied for all frequencies from zero to Nyquist frequency; failing this the tracking error may be amplified at certain frequency. The error-decay condition can be presented in a Nyquist diagram.

In a Nyquist diagram shown on fig.4.2, the error-decay factor $\left|1-G_p(e^{j\omega T_s})L(e^{j\omega T_s})\right|$ is the distance between the point (1, 0) to the locus of $G_p(e^{j\omega T_s})L(e^{j\omega T_s})$. And in order to satisfy the error-decay condition $\left|1-G_p(e^{j\omega T_s})L(e^{j\omega T_s})\right|<1$, the distances should be less than 1 at all frequencies. Therefore, the error-decay condition can be presented as a unit circle with central point at (1, 0) in the Nyquist diagram as shown on fig 4.2.

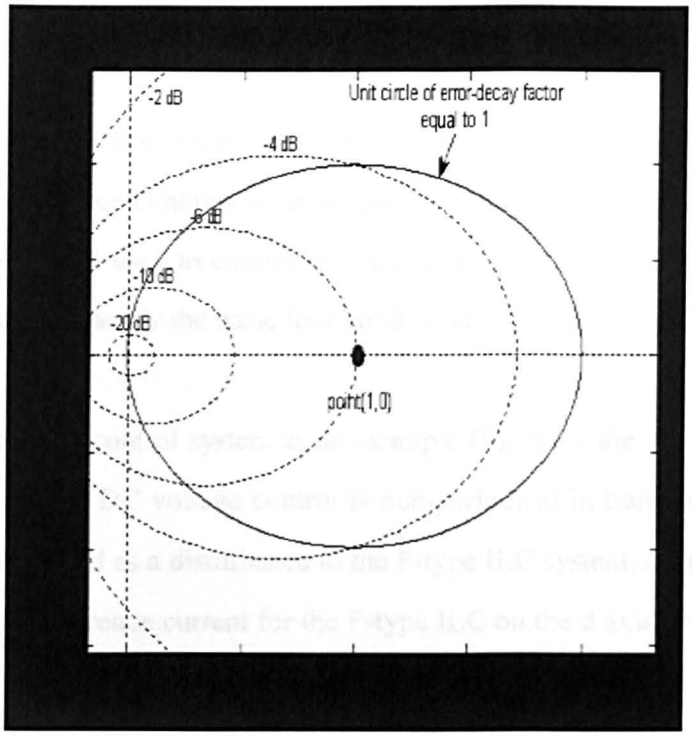


Figure 4. 2: Unit circle of error-decay condition in the Nyquist diagram of $G_p(e^{j\omega T_s})L(e^{j\omega T_s})$

Through fig.4.2, it can also be obtained that, the error-decay factor at a certain frequency ω is represented by the distance between the central point and the point on the locus of $G_p(e^{j\omega T_s})L(e^{j\omega T_s})$. Hence the learning factor $L(e^{j\omega T_s})$ is selected to ensure that the locus of $G_p(e^{j\omega T_s})L(e^{j\omega T_s})$ lies inside the unit circle to satisfies the error decay condition and to minimize the value of the error decay factor at the frequencies of interest.

4.3 Analysis of robustness against bounded disturbances

For real applications, the P-type ILC needs to be proved robust against various kinds of disturbance, such as initial offset, state and input disturbances.[80] So it is important to prove that the system is still able to minimize the tracking

error when subject to these disturbances.

The P-type ILC control hasn't been applied in literature to cascaded power control system which contains an inner and an outer control loop. In particular if the P-type ILC is used to control the inner control loop, this cascade control structure may not satisfy the basic four conditions (A1-A4) of page 59.

By using the SAF control system as an example (fig. 4.3), the demand current i_{dc}^* from the outer DC voltage control is non-periodical in transient condition and can be regarded as a disturbance to the P-type ILC system. As presented in Chapter 3, the reference current for the P-type ILC on the d axis is equal to the reference of the harmonic current plus the demand current from the DC voltage control. As a component of the reference, this demand current behaves as a non-periodic signal. The variations in power system and load transient can also cause large variations of this demand current. However through section 4.2 it can be understood that the ILC controller theoretically requires the reference to be a periodic signal, otherwise, the tracking error may not converge to a satisfactory level. Therefore, a robustness analysis is required to prove the feasibility of applying P-type ILC in cascade control structures.

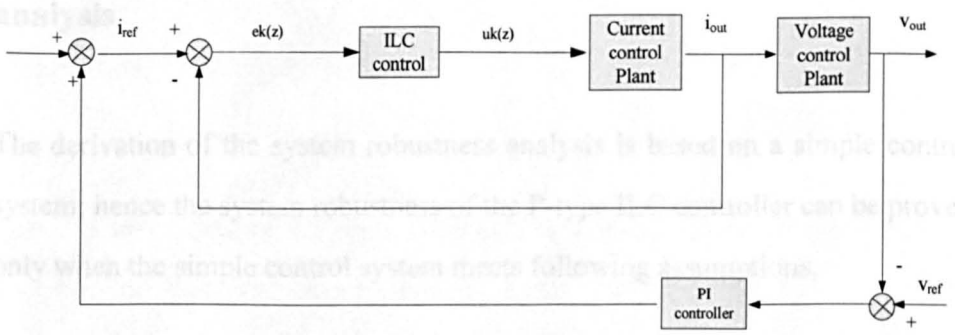


Figure 4. 3: Concept structure of the SAF control system

Authors in [80] introduce a general method for analyzing the robustness of a

P-type ILC controlled system under mismatch of the system parameters. However, the consideration of robustness under the disturbances is absent in this mathematical derivation.

Based on the method in [80], a novel system robustness analysis to input disturbances is proposed in this section. This analysis can also be used in other systems using a cascade control structure, where the inner loop is controlled by a P-type ILC system.

This system robustness analysis aims to prove that the difference between the actual control signal $u_k(t)$ (as shown on fig. 4.1) and the expected one $u_d(t)$ is still capable to converge to a low value when the system is exposed to bounded input disturbances. The expected control signal $u_d(t)$ is able to ideally control the system with a zero tracking error, hence if the difference between $u_k(t)$ and $u_d(t)$ converges to a low value after finite repetitions, then the tracking error between the actual output signal $y_k(t)$ and the reference one y_d of the control system can also converge, theoretically to a low value after finite repetitions.

4.3.1 Conditions and theorems applied in the robustness analysis

The derivation of the system robustness analysis is based on a simple control system; hence the system robustness of the P-type ILC controller can be proven only when the simple control system meets following assumptions.

B1) The control plant is a first order system and the state space equation of the control plant does not contain a feed-through matrix D;

B2) The expected control signal $u_d(t)$ which provides a zero tracking error do exists, as well as the expected state signal $x_d(t)$;

B3) All the disturbances including the state disturbance, the initial offset and the disturbance caused by the non-periodic demand current signal for DC voltage control, must be bounded;[65, 80]

In addition, the development of the robustness analysis for the P-type ILC system also requires the following two theorems.

Theorem 1: Bellman-Gronwall law

Defining u(t) and v(t) as non-negative continuous functions in the time range [0, T], there are non-negative constants M and q for which the following condition can be obtained[81],

If

$$u(t) \le M_1(q + \int_0 v(s)ds) + M_1 \int_0 u(s)ds \tag{4.8}$$

Then

$$u(t) \le M_1 q e^{M_1 t} + M_1 \int_0 e^{M_1(t-s)} v(s)ds \tag{4.9}$$

The full derivation of Bellman-Gronwall law is presented in Appendix B. Based on this theorem, a lemma can be presented as following [81].

$$u(t) \le M_1(q e^{M_1 t} + \int_0 e^{M_1(t-s)} v(s)ds) \tag{4.10}$$

Theorem 2:

We assume the state space equation of a first order control plant is expressed as below:

$$\left.\begin{aligned}\dot{x}(t) &= Ax(t) + Bu(t)\\ y(t) &= Cx(t)\end{aligned}\right\} \tag{4.11}$$

Where the following notation has been used:

A: is the system matrix;

B: is the input matrix

C: is the output matrix;

x(t): is the state vector;

u(t): is the input vector (control signal to the plant);

y(t) is the output vector.

Considering that the system is time-invariant and therefore the system matrix A, input matrix B and output matrix C have constant elements, a matrix function f( ) for A, B and g( ) for C can be written down as eq.(4.12) for the simplification of the derivation procedure:

$$\left.\begin{aligned}\dot{x}(t) &= f((x(t),u(t)))\\ y(t) &= g(x(t))\end{aligned}\right\} \tag{4.12}$$

Based on this state space equation, it is possible to derive the following relations as done in[80],

$$\|f(x_1,u) - f(x_2,u)\| \le M_2\|x_1 - x_2\| \qquad \forall x_1, x_2, u \tag{4.13}$$

$$\|f(x,u_1) - f(x,u_2)\| \le M_2\|u_1 - u_2\| \qquad \forall u_1, u_2, x \tag{4.14}$$

$$\|g(x_1) - g(x_2)\| \le M_2 \|x_1 - x_2\| \qquad \forall x_1, x_2 \tag{4.15}$$

Where M_2 is a suited non-negative constant.

4.3.2 Derivation of the robustness analysis

The derivation of the robustness analysis can be separated into four steps including,

- Defining the disturbances of the control system
- Deriving the relationship between input signal error at k+1th repetition ($\delta u_{k+1}(t)$) and input signal error at kth repetition ($\delta u_k(t)$) by using an operator Q_k;
- Determining upper bound of the operator Q_k;
- Proving the difference between the actual and expected control signal is able to converge under bounded disturbances.

Step 1 Defining the disturbances

Assuming the state and output equations of a first order control plant as the one shown in eq. (4.12), the learning update rule for P-type ILC in continuous domain can be expressed as below:

$$u_{k+1}(t) = u_k(t) + \phi(t)(y_d(t) - y_k(t)) \tag{4.16}$$

Where $\Phi(t)$ represents the learning factor in continuous domain. Defining the non-periodic demand current signal from the DC voltage loop as a disturbance $\eta(t)$ to the control system, the measured output tracking error can be written as,

$$e_k(t) = (y_d(t) + \eta_k(t)) - y_k(t) \tag{4.17}$$

Thus the real tracking error is given by,

$$y_d(t) - y_k(t) = e_k(t) - \eta_k(t) \tag{4.18}$$

Substituting eq. (4.18) into (4.16), the learning update rule can be rewritten as below:

$$u_{k+1}(t) = u_k(t) + \phi(t)(e_k(t) - \eta_k(t)) \tag{4.19}$$

Defining the state disturbance as ε. Since the state disturbance may vary with time, ε_k should be defined as a time varying function. Thus the system state and output equations (4.16) are rewritten as below:

$$\left.\begin{aligned} \dot{x}(t) &= f(x_k(t), u_k(t)) - \varepsilon_k(t, x_k(t), u_k(t)) \\ y(t) &= g(x_k(t)) \end{aligned}\right\} \tag{4.20}$$

In [13] it has been stated that the ILC control system is very sensitive to initial state offsetζ (0), which is therefore seriously considered in this section for the robustness analysis. Initial conditions of the states at k^{th} repetition can be written as,

$$x_k(0) = x_d(0) + \zeta_k(0) \tag{4.21}$$

Step 2 Relation between $\delta u_{k+1}(t)$ and $\delta u_k(t)$

In accordance with condition B2, the expected control signal, states and the output signal exist. Therefore the following equations describing the state error, output signal error and control signal error of the k^{th} repetition can be written,

$$\left.\begin{aligned}\delta x_k(t) &= x_d(t) - x_k(t)\\ \delta y_k(t) &= y_d(t) - y_k(t)\\ \delta u_k(t) &= u_d(t) - u_k(t)\end{aligned}\right\} \quad 0 \le t \le T, k \ge 0 \tag{4.22}$$

Defining following equations [13]:

$$\left.\begin{aligned} f_1(x,u) &= f(x_d(t),u_d) - f(x_d(t) - x(t), u_d(t) - u(t))\\ g_1(x) &= g(x_d(t)) - g(x_d(t) - x(t))\end{aligned}\right\} \tag{4.23}$$

And substituting eq. (4.22), (4.23) into (4.20), the state space equation of the system is rewritten as below:

$$\left.\begin{aligned}\delta\dot{x}_k(t) &= f_1(\delta x_k(t), \delta u_k(t)) - \varepsilon_k(t, \delta x_k(t), \delta u_k(t))\\ \delta y(t) &= g_1(\delta x_k(t))\end{aligned}\right\} \tag{4.24}$$

Substituting eq. (4.21) into (4.22), the error on the initial state signal $\delta x_k(0)$ can be written as,

$$\begin{aligned}\delta x_k(0) &= x_d(0) - x_k(0)\\ &= x_d(0) - (x_d(0) + \zeta_k(0))\\ &= -\zeta_k(0)\end{aligned} \tag{4.25}$$

Based on the learning update rule in eq. (4.19), and eq. (4.22), the error

$\delta u_{k+1}(t)$ can be derived as,

$$\begin{aligned}\delta u_{k+1}(t) &= u_d(t) - u_{k+1}(t) \\ &= (u_d(t) - u_k(t)) - (u_{k+1}(t) - u_k(t)) \\ &= \delta u_k(t) - (u_k(t) + \phi(t)(e_k(t) - \eta_k(t)) - u_k(t))\end{aligned} \tag{4.26}$$

Since $e_k(t) = \delta y_k(t)$, substituting eq. (4.24) into (4.26) yields,

$$\delta u_{k+1}(t) = \delta u_k(t) - (\phi(t) g_1(\delta x_k(t)) - \phi(t)\eta_k(t)) \tag{4.27}$$

Equation (4.27) can be separated into two parts, including $\delta u_k(t)$ and $\emptyset(t) g_1(\delta x_k(t)) - \emptyset(t)\eta_k(t)$. Since $\delta x_k(t)$ in the term $\emptyset(t) g_1(\delta x_k(t)) - \emptyset(t)\eta_k(t)$ can be written in function of $\delta u_k(t)$, then defining an operator Q_k [] which satisfies following equation,

$$Q_k(\delta u_k(t)) = \phi(t) g_1(\delta x_k(t)) - \phi(t)\eta_k(t) \tag{4.28}$$

Thus eq. (4.28) can be rewritten as following,

$$\delta u_{k+1}(t) = \delta u_k(t) - Q_k(\delta u_k(t)) \tag{4.29}$$

Step 3 Determining the upper bound of Q_k

In order to determine the upper bound of $Q_k(t)$, an equation describing the relationship between $\delta x_k(t)$ and $\delta u_k(t)$ should be derived. As presented in (4.24) and (4.25), the $\delta x_k(t)$ in (4.28) satisfies following equation:

$$\left.\begin{aligned}\delta\dot{x}(t) &= f_1(\delta x(t), \delta u(t)) - \varepsilon_k(t, \delta x(t), \delta u(t)) \\ x(0) &= -\zeta(0)\end{aligned}\right\} \tag{4.30}$$

Integrating eq. (4.30) yields,

$$\delta x(t) = -\zeta_k(0) + \int_0^t f_1(\delta x(s), \delta u(s))ds - \int_0^t \varepsilon_k(s, \delta x_k(s), \delta u_k(s))ds \tag{4.31}$$

Based on Theorem 2, the upper bound of $\|f_1(\delta x(s), \delta x(s))\|$ in eq. (4.31) can be estimated from the following derivation:

$$\begin{aligned}&\|f_1(\delta x(t), \delta u(t))\| \le \|f(x_d(t), u_d(t)) - f(x_d(t) - \delta x(t), u_d(t))\| + \\ &\|f(x_d(t) - \delta x(t), u_d(t)) - f(x_d(t) - \delta x(t), u_d(t) - \delta u(t))\| \\ &\le M_3 \bullet \|\delta x(t)\| + M_3 \bullet \|\delta u(t)\|\end{aligned} \tag{4.32}$$

M_3 is a non-negative constant as discussed in Theorem 2. According to condition B3, the upper bound of $\|\varepsilon_k(s, \delta x(s), \delta x(s))\|$ in eq. (4.31) can be estimated as follows:

$$\beta_k = \sup_t \|\varepsilon_k(t, x_k(t), u_k(t))\| \tag{4.33}$$

Where theβ_k is a non-negative constant. Substituting (4.32) and (4.33) into (4.31) yields,

$$\|\delta x(t)\| \le \zeta_k(0) + M_3 \int_0^t \|\delta x(s)\|ds + M_3 \int_0^t \|\delta u(s)\|ds + \beta_k T \tag{4.34}$$

Based on Bellman-Gronwall law presented in Theorem 1, eq. (4.34) can be rewritten,

$$\begin{aligned}&\|\delta x(t)\| \le M_3 (\int_0^t \|\delta x(s)\|ds + \int_0^t \|\delta u(s)\|ds) + \beta_k T + \zeta_k(0) \\ &\le M_4 (\int_0^t \|\delta u(s)\|ds + \beta_k T + \|\zeta_k(0)\|)\end{aligned} \tag{4.35}$$

Where M_4 is positive constant. Similarly the matrix function g(x) also has its

upper bound, therefore a non-negative constant c can be obtained to meet the following requirement,

$$\|g_1(x(t))\| \le c\|x(t)\| \tag{4.36}$$

Based on condition B3, the disturbance caused by the demand current (the output signal from the outer control loop) has an estimated upper bound. It can be defined as follows, where λ_k is a non-negative constant,

$$\lambda_k = \sup_l \|\eta_k(t)\| \tag{4.37}$$

Substituting eq. (4.35), (4.36) and (4.37) into (4.28) yields the upper bound of Q_k,

$$\begin{aligned} Q_k &\le (\|\phi(t)g_1(\delta x(t))\| + \|\phi(t)\eta_k(t)\|)/\|(\delta u_k(t))\| \\ &\le (\phi(t)M_4(\int_0 \|\delta u(s)\|ds + \beta_k T + \|\zeta_k(0)\|) + \|\phi(t)\eta_k(t)\|)/\|(\delta u_k(t))\| \\ &\le (\phi(t)M_4(\int_0 \|\delta u(s)\|ds + \beta_k T + \|\zeta_k(0)\| + \|\phi(t)\lambda_k\|)/\|(\delta u_k(t))\| \end{aligned} \tag{4.38}$$

Step 4 Convergence of the control signal under bounded disturbances

Equation (4.29) can be rewritten as below,

$$\begin{aligned} \|\delta u_{k+1}(t)\| &= \|(\delta u_k(t)) - Q_k(\delta u_k(t))\| \\ &= |(1-Q_k).(1-Q_{k-1})...(1-Q_0)|.\|(\delta u_0(t))\| \end{aligned} \tag{4.39}$$

In the presence of disturbances, the P-type ILC controller is still able to let the

$\delta u_k(t)$ converge to low value by satisfying the following condition:

$$\left|1-(\phi(t)M_4(\int_0\|\delta u(s)\|ds+\beta_k T+\|\zeta_k(0)\|)+\|\phi(t)\lambda_k\|)/\|(\delta u_k(t))\|\right|<1 \tag{4.40}$$

Therefore it can be summarized that, the P-type ILC controller is capable to still be effective in a control system with disturbances, even in those where the disturbance appears in the reference signal. The robustness analysis theoretically proves that the P-type ILC control not only can be applied in SAF systems, but also in other cascade control systems structures, not presenting a feed-through matrix in the state space equations.

4.3.3 Discussion on the robustness analysis

Based on the mathematical derivation in section 4.3.2, three consideration can be made, which will be adopted as theoretical guidelines and support for designing and optimizing the P-type ILC controller in the following chapters.

1) Through equation (4.40) it can be observed that, the components $\beta_k T, \|\zeta_k(0)\|$ and $\|\phi(t)\lambda_k\|$ which represent the disturbances in k^{th} repetition, can affect the converge speed of the P-type ILC system or even the stability of the control system, if they do not verify (4.40).

   The relationship in (4.39) and (4.40) facilitates the design of learning factor Φ(t), which should be chosen to make the value of $(1-Q_k)$ close to zero in k^{th} repetition. By doing this, the error of the control signal $\delta u_{k+1}(t)$ can converge fast to a small value. Therefore, as an example, if Φ(t) is determined without the consideration of the disturbances (only to make the

value of $\left|1-(\phi(t)M_4(\int_0\|\delta u(s)\|ds)\right|$ close to zero), then the values of eq.(4.40) will be deviated further away from zero due to the terms of $\beta_k T, \|\zeta_k(0)\|$ and $\|\phi(t)\lambda_k\|$, resulting in a slower error-decay speed. Under some extreme circumstances, the value of $|(1-Q_k)|$ can exceed 1 due to very large disturbances, this will compromise the system stability by amplifying the value of the error $\delta u_{k+1}(t)$.

Therefore, the robustness of the control system greatly depends on the disturbances intensity. For a suitable learning gain Φ(t), the smaller disturbances, indicates the faster error-decay speed and better system stability.

2) The demonstration of the system robustness proves that an instant high disturbance in any repetition can affect the final error-decay speed.

As presented in eq. (4.39), the error between the actual and expected control signal in the $(k+1)^{th}$ repetition ($\delta u_{k+1}(t)$)can be represented as the initial control error $\delta u_0(t)$ times the $(1-Q_k)$ factors of each previous repetition. Therefore, with the same learning gain L and initial control error, the value of $\delta u_{k+1}(t)$ only depends on the product of $(1-Q_k).(1-Q_{k-1})...(1-Q_0)$, which means the value of Q in any previous repetitions can affect the control error in the final repetition. Therefore the appearance of any instant large disturbance in a random repetition can slow down the overall error-decay speed.

Simulation results in Chapter 3 have shown that a power system load transient can cause a variation in the demand current from the voltage

control loop; this can be considered an instant large disturbance to the inner control loop and can seriously affect the error-decay speed. More importantly, such variation may cause stability problem as discussed in 1). Therefore, the P-type ILC controller should increase its dynamic response to against the instant disturbances.

3) Through eq. (4.40) it also can be noticed the smaller value of L(t) may minimize the value of the components $\phi(t)M_4(\int_0\|\delta u(s)\|ds+\beta_k T+\|\zeta_k(0)\|)$ and $\phi(t)\lambda_k$ in eq. (4.40); hence the effect caused by the instantaneous disturbances can be minimized.

As discussed in 1), if a large disturbance appears in some repetitions, then the value of $|(1-Q_k)|$ maybe large than 1 in these repetitions, which results in the P-type ILC system becoming unstable. In this situation, a smaller learning gain value may maintain the value of $|(1-Q_k)|$ below 1 by minimizing the value of components $\phi(t)M_4(\int_0\|\delta u(s)\|ds+\beta_k T+\|\zeta_k(0)\|)$ and $\phi(t)\lambda_k$, and so making the control system still able to converge during a large instantaneous disturbance.

4.4 Conclusion

In this chapter, the theoretical principle of the P-type ILC controller is presented, followed by the introduction of the error-decay condition, and by the procedure for using this error-decay condition to identify the controller learning factor.

This chapter also closely investigate the control system robustness to state and input disturbances and initial offset when P-type ILC is used as inner loop of a

cascade control structure. In particular the non-periodic behaviour of the demand current from the outer voltage control loop, generate an input disturbance to the P-type ILC control system that actually pulls the feasibility of P type ILC beyond its applicable conditions.A mathematical derivation finds the robustness conditions to be verified for the suitability of the use of P-type ILC control under bounded disturbances. Based on the robustness analysis, three considerations which can be used to optimize the P-type ILC system performance, are presented. These will be verified by the simulation results of the P-type ILC controlled SAF system in chapter 5.

Chapter 5 Direct P-type ILC system design of SAF in synchronous frame

5.1 Introduction

Chapter 4 has mathematically shown the feasibility of applying the P-type ILC controller in a cascade control system. This chapter concentrates on verifying its superiority in the SAF current control application over conventional controllers via simulation using Simulink in Matlab.

In this chapter the direct P-type ILC will be applied in the SAF system. [66] Its design procedure to obtain a fast error-decay on proposed harmonic frequencies will be also presented.

Finally, the simulation results will prove the validity of the mathematical derivations in Chapter 4. However, a close investigation by simulation demonstrates the limits of the standard direct P-type ILC approach, which will lead to in the corresponding proposed improvement solutions.

5.2 Introduction of direct P-type ILC controller

It has been shown in Chapter 4 that the demand current of the outer voltage control loop acts as a non-periodic disturbance for the P-type ILC controller. Since the P-type ILC controller takes the tracking error in previous ILC repetition to compute the current control signal, it is found that a large non-periodic variation of the demand current can cause the instability of the whole system. To overcome this problem, an extra signal corresponding to the

error is introduced as a compensation to the P-type ILC control, to help maintaining the system stability and added to the output of the control. The P-type ILC with the addition of the extra signal fed directly from the tracking error signal is called the direct P-type ILC [66].

The discrete domain block diagram of the proposed direct P-type ILC current control is shown in fig.5.1, where, y_d represents the output reference and $e_k(z)$ represents the harmonic current tracking error at the k^{th} repetition. The $e_k(z)$ is combined with the P-type ILC controller to form the control signal. As shown on fig 5.1, the P-type ILC controller consists of two memories (which are two different numbers of discrete delays) and one learning factor (L(z)). The memories are used to discrete delay the error $e_k(z)$ and control signal $u_k(z)$ for one repetition, which, together with the learning factor L(z), ensure that the structure of this P-type ILC controller is in strict accordance with its learning update rule: $u_k(z)=u_{k-1}(z)+L(z)e_{k-1}(z)$.

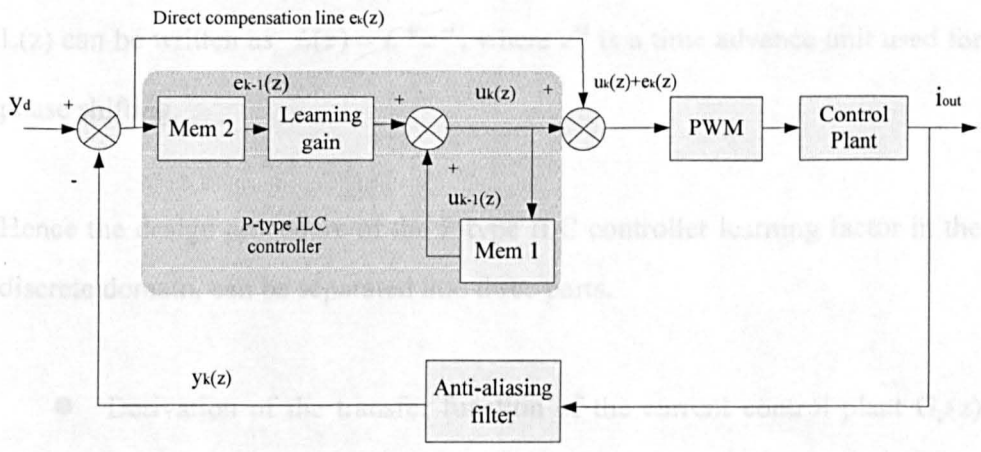


Figure 5. 1: block diagram of direct P-type ILC current control loop

Due to the simple structure of the direct P-type ILC controller, only three parameters, including the learning factor L(z), and two memories are required to be determined. Section 5.3 will introduce the design procedure for the learning factor (which consists of the learning gain and the phase shift

component, as presented in Chapter 4). Since the leaning factor contains a phase shift component, the Mem 2 shown in fig.5.1 has to compensate this phase shift properly, for the purpose of discrete delaying the error signal for a complete repetition. The determination of the numbers of discrete delays of the memories (Mem1 and Mem2) will be addressed in section 5.5.

5.3 Determination of the learning factor based on error-decay condition

As discussed in Section 4.2, the error-decay condition of the P-type ILC system, written as $\left|1-G_p(e^{j\omega T_s})L(e^{j\omega T_s})\right|<1$ can be used to identify the learning factor of the P-type ILC in the discrete domain. The learning factor contains two components, namely the learning gain (L) and the phase shift component ($e^{j\omega T}$). One of the simplest expressions of the function of the learning factor L(z) can be written as $L(z)=L*z^m$, where z^m is a time advance unit used for phase shifting.

Hence the design procedure of the P-type ILC controller learning factor in the discrete domain, can be separated into three parts.

- Derivation of the transfer function of the current control plant $G_p(z)$ seen by the P-type ILC controller;
- Determination of the phase shift component (time advance unit in this application) of the learning factor by using the bode diagram;
- Determination of the learning gain (L) of the learning factor by using the Nyquist diagram.

5.3.1 Transfer function of the current control plant seen by the P-type ILC controller

The block diagram of the current control loop in the discrete domain is presented in fig.5.2, where G(z) represents the transfer function of the control plant, and H(z) represents the transfer function of the anti-aliasing filter. A unit delay Z(z)=1/z caused by the PWM modulation and DSP computation time is also taken into account.

Through fig.5.2 it can be found that, G(z) is not equal to the control plant seen by the P-type ILC ($G_p(z)$). In order to determine the learning gain of P-type ILC controller, the transfer function of $G_p(z)$ has to be determined. In order to do so, the signal $a_k(z)$ representing the control signal from the P-type ILC controller, is defined as shown in fig.5.2.

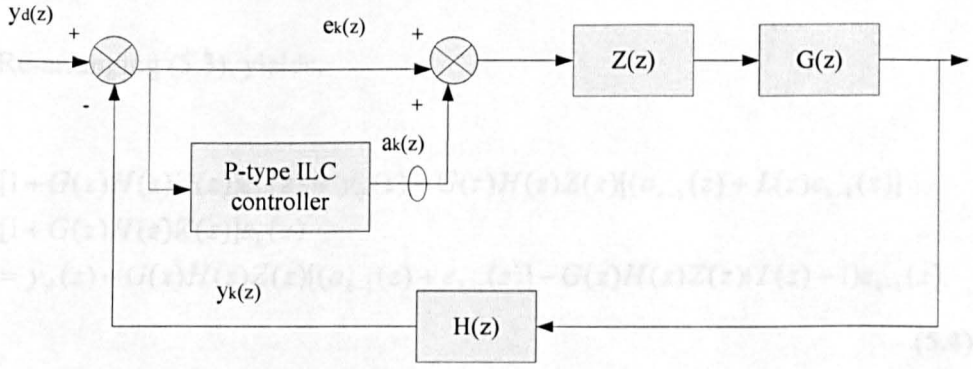


Figure 5. 2: Block diagram of direct ILC current control loop in discrete domain

Based on fig.5.2, the transfer function of the control plant $G_p(z)$ seen by the P-type ILC controller can be derived as repeated in the following procedures.

Though fig.5.2, the following equations can be defined:

$$\left.\begin{aligned} e_k(z) &= y_d(z) - y_k(z) \\ y_k(z) &= (G(z)H(z)Z(z))(a_k(z) + e_k(z)) \end{aligned}\right\} \tag{5.1}$$

Similarly as discussed in Section 4.2, in the direct P-type ILC system, the learning update rule of the P-type ILC controller can be written as,

$$a_k(z) = a_{k-1}(z) + L(z)e_{k-1}(z) \tag{5.2}$$

Based on the eq.(5.1) and (5.2), the following derivation can be obtained:

$$\begin{aligned} & e_k(z) = y_d(z) - y_k(z) \\ & = y_d(z) - G(z)H(z)Z(z)[a_k(z) + e_k(z)] \\ & = y_d(z) - G(z)H(z)Z(z)[a_{k-1}(z) + L(z)e_{k-1}(z) + e_k(z)] \\ & = y_d(z) - G(z)H(z)Z(z)[(a_{k-1}(z) + L(z)e_{k-1}(z)] - G(z)H(z)Z(z)e_k(z) \end{aligned} \tag{5.3}$$

Re-arranging (5.3), yields:

$$\begin{aligned} & [1 + G(z)H(z)Z(z)]e_k(z) = y_d(z) - G(z)H(z)Z(z)[(a_{k-1}(z) + L(z)e_{k-1}(z)] \\ & [1 + G(z)H(z)Z(z)]e_k(z) \\ & = y_d(z) - G(z)H(z)Z(z)[(a_{k-1}(z) + e_{k-1}(z)] - G(z)H(z)Z(z)(L(z) - 1)e_{k-1}(z) \end{aligned} \tag{5.4}$$

Considering (5.1), (5.4) can be rewritten as,

$$\begin{aligned} & [1 + G(z)H(z)Z(z)]e_k(z) = e_{k-1}(z) - G(z)H(z)Z(z)(L(z) - 1)e_{k-1}(z) \\ & [1 + G(z)H(z)Z(z)]e_k(z) \\ & = [1 + G(z)H(z)Z(z)]e_{k-1}(z) - G(z)H(z)Z(z)L(z)e_{k-1}(z) \end{aligned} \tag{5.5}$$

If both sides of (5.5) are divided by 1+G(z)H(z)Z(z), the following relation can

be obtained:

$$e_k(z) = (1 - L(z)\frac{G(z)H(z)Z(z)}{1+G(z)H(z)Z(z)})e_{k-1}(z) \tag{5.6}$$

Comparing (5.6) with the (4.6), the transfer function of the control plant seen by the P-type ILC controller can be written as,

$$G_p(z) = \frac{G(z)H(z)Z(z)}{1+G(z)H(z)Z(z)} \tag{5.8}$$

As shown in chapter 3, the transfer functions of blocks G and H in continuous domain are, $G(s)=1/(L_f s+R_f)$, and $H(s)=\omega_a/(s+\omega_a)$ respectively; Z(z) equals to a unit delay z^{-1}. Therefore, $G_p(z)$ can be written as:

$$G_p(z) = \frac{(\frac{z}{z-e^{-(\frac{R_f}{L_f})T_s}})(\frac{\omega_a z}{z-e^{-\omega_a T_s}})z^{-1}}{1+(\frac{z}{z-e^{-(\frac{R_f}{L_f})T_s}})(\frac{\omega_a z}{z-e^{-\omega_a T_s}})z^{-1}} \cdot \frac{L_f z - L_f e^{-(\frac{R_f}{L_f})T_s}}{L_f z - L_f e^{-(\frac{R_f}{L_f})T_s}} \tag{5.9}$$

It needs to be emphasized that, in this application the sampling time (T_s) in eq. (5.9), is chosen to be 1/48000 s. As presented in Chapter 4, the P-type ILC controller requires the reference signal to be periodic. The sampling frequency should be determined to ensure a sufficient samples number in each current harmonics reference repetition. As discussed in Chapter 3, the current reference of the SAF current control loop only contains the 5^{th} and 7^{th}, 11^{th} and 13^{th} harmonics for this design, which means that they will be transformed into two harmonic signal at frequency 2400Hz and 4800Hz in the d-q frame rotating

with fundamental frequency equal to 400Hz. With a sampling frequency of 48000Hz there are N=20 samples in each repetition of the reference current signal, which remain identical in every cycle.

5.3.2 Design of the phase shift component ($e^{j\omega T}$) using bode diagram

With the knowledge of the transfer function $G_p(z)$ seen by the P-type ILC controller, the system Nyquist diagram can be plotted by using the Matlab SISOTOOL toolbox.

As discussed in Chapter 4, the error-decay condition requires the locus of $G_p(e^{j\omega T_s})L(e^{j\omega T})$ to be located within a unit circle centered at (1, 0). However, for the Nyquist diagram of the SAF current control system as shown on fig 5.3, the locus of $G_p(e^{j\omega T_s})$ passes through the third and fourth quadrants, which means the locus of $G_p(e^{j\omega T_s})$ does not located within the unit circle. As presented in Section 4.2.1, the distance between point (1, 0) and point A on the locus of $G_p(e^{j\omega T_s})$ stands for the error-decay factor at the corresponding frequency of point A. If the distance is longer than 1, the P-type ILC controller will amplify the error at the corresponding frequency. Therefore, a phase shift component in the learning factor is required to draw the locus of $G_p(e^{j\omega T_s})$ back into the first and second quadrants, in order to satisfy the error-decay condition.

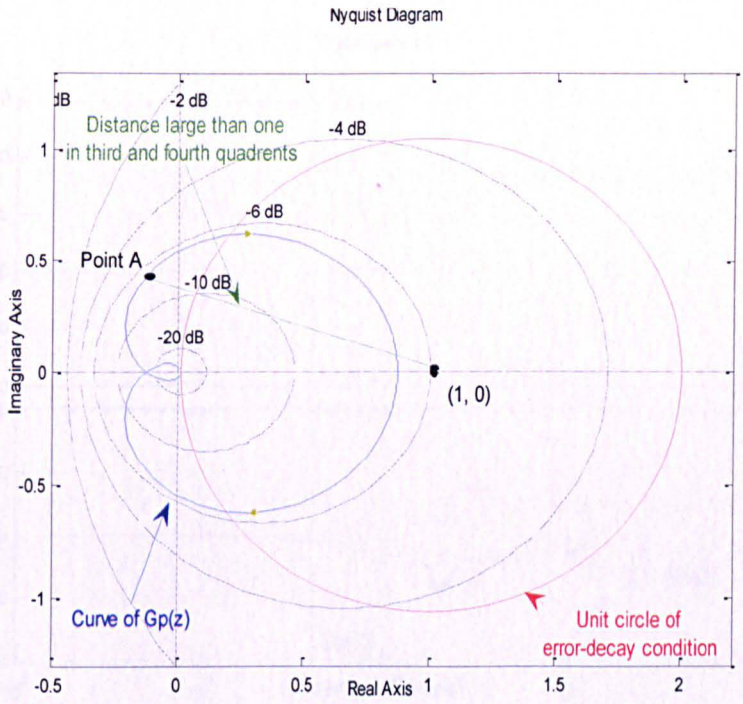


Figure 5. 3: Nyquist diagram of $G_p(z)$

In this application, the phase shift component of the P-type ILC controller ($e^{j\omega T}$), is a time-advance unit which can be written as z^m in the discrete domain, where m is an integer. Since the P-type ILC controller has a memory to delay the tracking error for one repetition (z^{-N}), where N is the number of samples in one repetition, it is possible to apply a time-advance unit in a P-type ILC controller, which will result a reduction of N to N-m.

By using this time-advance unit, the phase of $z^m G_p(z)$ from zero to Nyquist frequency can be maintained within the range of -90 degree to 90 degree, i.e., the locus of $z^m G_p(z)$ locates inside the first and second quadrants in a Nyquist diagram. The bode diagram shown in fig.5.4, presents a time-advance unit chosen as z^2, which is capable to keep the phase of $z^m G_p(z)$ within the desire range (-90 degree to 90 degree). Therefore, the phase shift component is determined as a time-advance unit z^2 for this design.

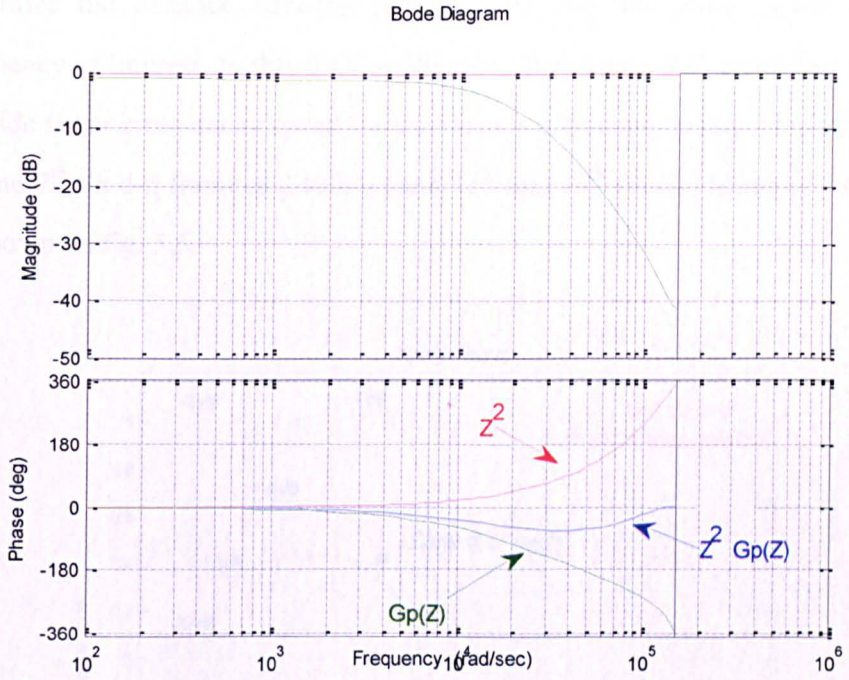


Figure 5. 4: Frequency response of z^2, $G_p(z)$ and $z^2G_p(z)$

5.3.3 Design of the learning gain (L) using the Nyquist diagram

After the phase shift component of the P-type ILC controller has been identified (as in section 5.3.2), the design task is determining the learning gain. As shown in fig.5.5, the locus of $z^2G_p(z)$ locates inside the unit circle of the error-decay condition. This means the P-type ILC controller is able to theoretically achieve zero steady state error at any frequency from zero to the Nyquist frequency. In this case, the learning gain L is used to minimize the error-decay factor and hence maximize the error-decay speed of the control system on specific frequencies.

As discussed in section 4.2.1, a smaller error-decay factor presents a faster error-decay speed. Therefore the learning gain should be determined to

minimize the distance between point (1, 0) and the point related to the frequency of interest. In this SAF application, the P-type ILC controller should provide faster error-decay speed for the harmonic frequencies to compensate i.e. 5^{th} and 7^{th} (in d-q frame at 2400Hz) and 11^{th} and 13^{th} (in d-q frame at 4800Hz) as shown on fig. 5.5.

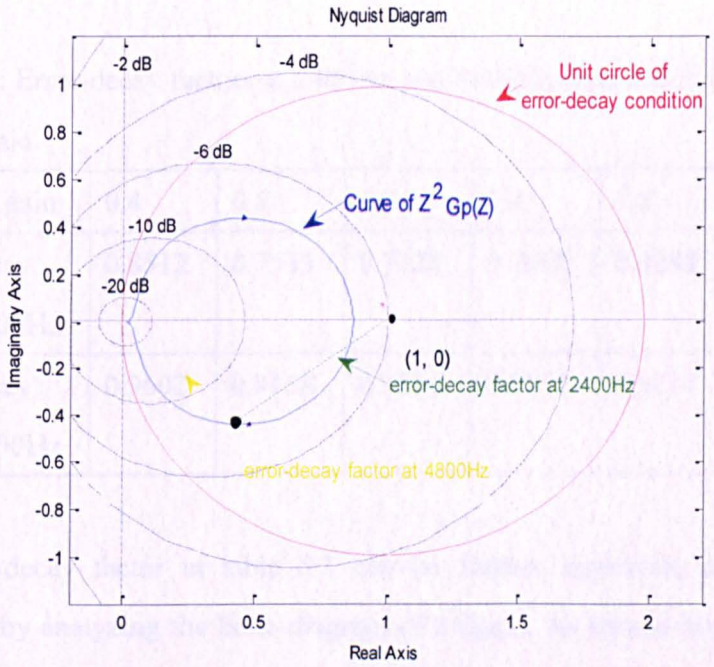


Figure 5. 5: Locus of $z^2G_p(z)$ in the Nyquist diagram.

In the Nyquist diagram, the error-decay factor at a specific frequency can be determined by eq.(5.10), where a and b are the real and imaginary values of the point on the locus of $z^2G_p(z)$ relative to that frequency.

$$d_f = \sqrt{(1-a_f)^2 + b_f^2} \tag{5.10}$$

During the tuning procedure of the learning gain, it can be found that its lower bound is 0.1, where the distance between the point (1, 0) and the point corresponding to 4800Hz is almost equal to 1. Similarly its upper bound can be

obtained equal to 2.2, when the locus of $Lz^2G_p(z)$ runs just beyond the unit circle of error-decay condition.

Table 5.1 presents the different learning gain values and their corresponding error-decay factors at 2400Hz and 4800Hz. It is clear that, the smallest error-decay factors appear when the learning gain is 1.2.

Table 5. 1: Error-decay factors at 2400Hz and 4800Hz with different values of learning gain.

Learning gain	0.4	0.8	1.2	1.4	1.8	2.0
Error-decay factor 2400Hz	0.8512	0.7533	0.7328	0.7968	0.8298	0.9001
Error-decay factor 4800Hz	0.9602	0.9158	0.9114	0.9171	0.9257	0.935

The error-decay factor in table 5.1 can be further improved, this can be explained by analyzing the bode diagram of $z^2G_p(z)$. As shown in fig 5.6, the magnitudes at 2400Hz and 4800Hz are -4.77dB and -10.9dB respectively and their phase shifts -42.4 degree and -66.2 degree. Hence with a constant learning gain, the P-type ILC controller cannot provide a small error-decay factors at both these frequencies. Therefore, smaller error-decay factors can be achieved if the magnitudes of control plant seen by the P-type ILC controller at these proposed harmonic frequencies can be increased or the phase shifts can be decreased. By doing this, the error-decay speed at those harmonic frequencies can be increased. This theory will be verified in next chapter.

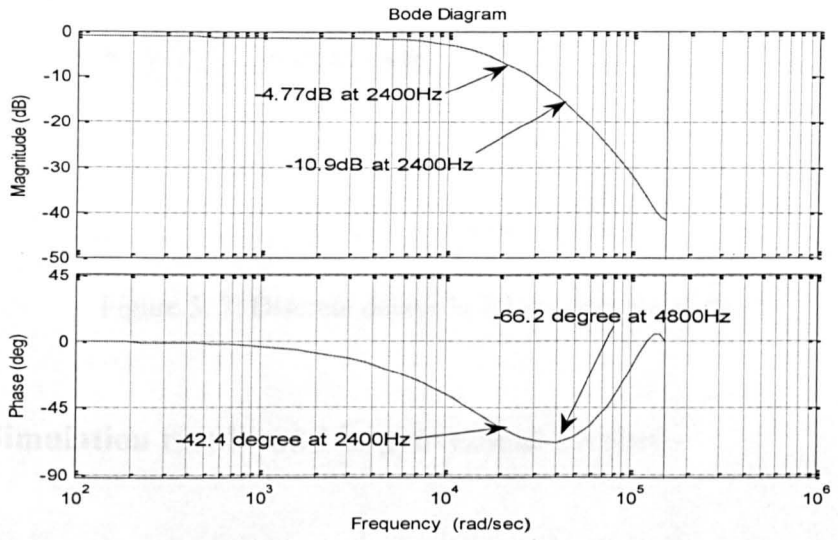


Figure 5. 6: Magnitudes and phases of $z^2G_p(z)$ at 2400Hz and 4800Hz

5.4 Determination of Memories

As discussed in section 5.2, the memories (Mem 1 and Mem2 in fig. 5.1) are actually discrete delays postponing the input error $e_k(z)$ and output control signal $u_k(z)$ of the P-type ILC controller for one repetition. Hence the number of discrete delays N should equal to the number of samples in one repetition. As discussed earlier, the harmonic reference signal composed by $5^{th}$and 7^{th} (2400Hz in d-q frame) 11^{th} and 13^{th} (4800Hz in d-q frame) harmonic components. Thus the total reference signal has a frequency in the d-q reference frame equal to2400Hz; using a sampling frequency of 48000Hz, N equals to 20.

Since the learning factor phase shift component is recognized as a time-advance unit z^m, where m equals to 2 in this application; the delay of the tracking error signal $e_k(z)$ will be z^{-N+m} and the delay for $u_k(z)$ will be z^{-N}. Therefore, the structure of the P-type ILC controller in the discrete domain can be presented as follow,

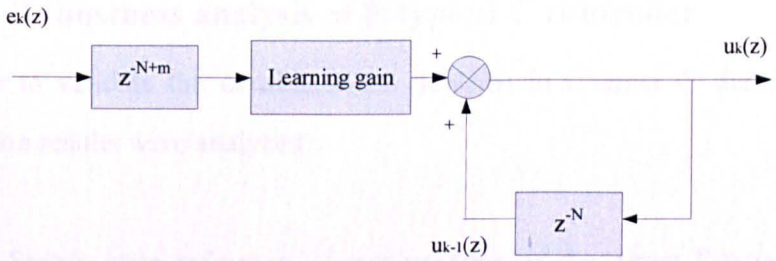


Figure 5. 7: Discrete delays in P-type ILC controller

5.5 Simulation results and improvement methods

The simulation model for the SAF system is selected identical to the one presented in Chapter 3, with the only difference that the direct P-type ILC controller designed in this chapter is used in the simulation model instead of the P+resonant controller.

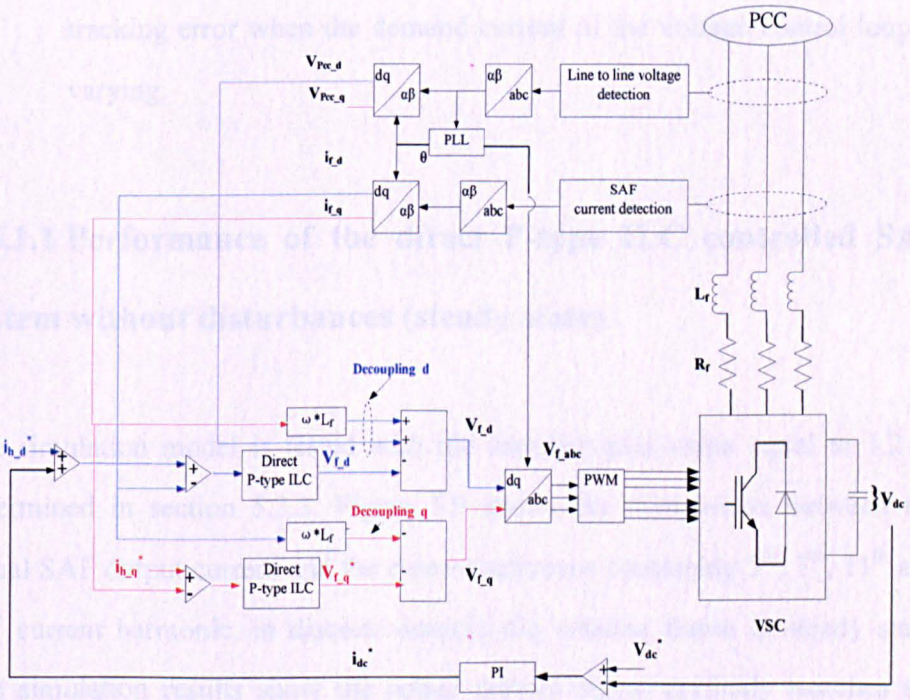


Figure 5. 8: Overall control structure of the direct P-type ILC controlled SAF system in the d-q rotating frame

5.5.1 Robustness analysis of P-type ILC controller

In order to validate the considerations describe in Chapter 4, the following simulation results were analyzed:

- Steady state reference current tracking of the direct P-type ILC, to prove the feasibility of applying the P-type ILC in cascade control systems;
- Reference current tracking, under bounded disturbances (i.e. supply voltage distortion and measurement white noise), to prove that the P-type ILC is able to maintain its correct function under certain intensity of disturbance, and that disturbances slow down the error-decay speed;
- Dynamic response of the direct P-type ILC to a power system load transient, to prove that smaller learning gain value provides a smaller tracking error when the demand current of the voltage control loop is varying.

5.5.1.1 Performance of the direct P-type ILC controlled SAF system without disturbances (steady state)

The simulation model is tested with the learning gain value equal to 1.2 as determined in section 5.3.3. Figure 5.9 shows the comparison between the actual SAF output current and the current reference containing 5^{th}, 7^{th}, 11^{th} and 13^{th} current harmonic, in discrete domain d-q rotating frame in steady state. The simulation results show the actual current signal perfectly matches the reference current with MTE equals to 0.007 and ATE equals to 0.003A for d and q reference frame.

Figure 5.10 presents the simulation results of phase a current tracking. As

shown, the actual SAF output current strictly tracks its reference signals with *MTE* equals to *0.011A*, and *ATE* equals to *0.006A*.

The simulation results in fig 5.9 and 5.10, prove the application feasibility of the P-type ILC controller in a cascade control system.

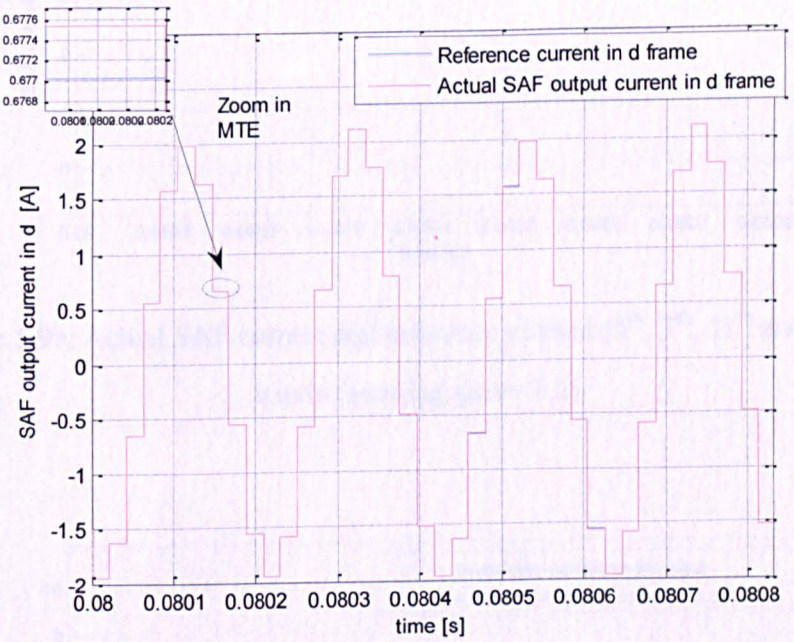


Figure 5. 9a: Actual SAF current and reference current (5^{th}, 7^{th}, 11^{th} and 13^{th}) on d axis (learning gain=1.2)

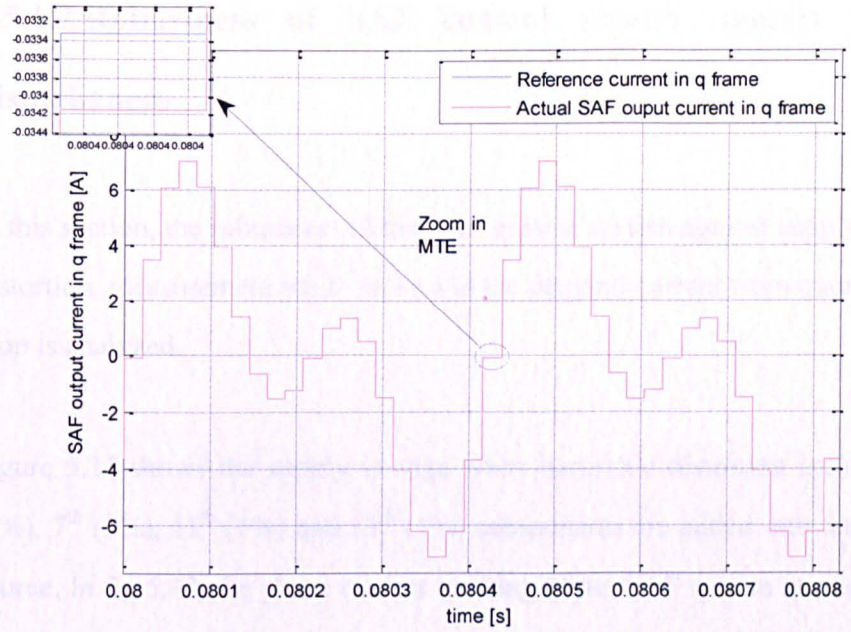


Figure 5.9b: Actual SAF current and reference current (5^{th}, 7^{th}, 11^{th} and 13^{th}) on q axis (learning gain= 1.2)

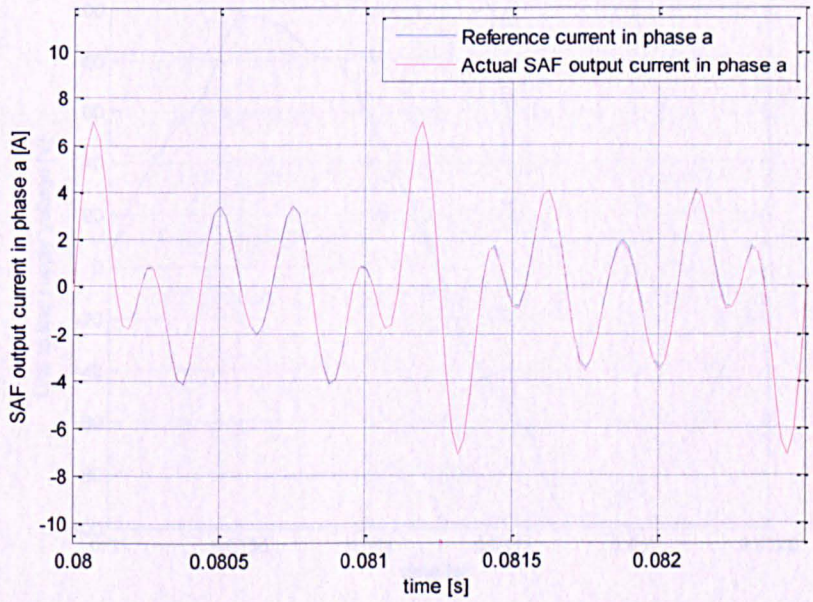


Figure 5. 10: Actual SAF current and reference current (5^{th}, 7^{th}, 11^{th} and 13^{th}) in phase a (learning gain= 1.2)

5.5.1.2 Robustness of SAF control system against several disturbances

In this section, the robustness of the SAF control system against supply voltage distortion, measurement white noise and the demand current from outer control loop is analyzed.

Figure 5.11 shows the supply voltage when harmonic distortion including 5^{th} (4%), 7^{th} (3%), 11^{th} (1%) and 13^{th} (1%) components are added into the voltage source. In fig 5.12, the phase current tracking of the SAF system at steady state is shown. It is clear that the control system is only slightly affected by the assumed distortion, with the MTE equal to 0.8233A and the ATE equal to 0.2518A.

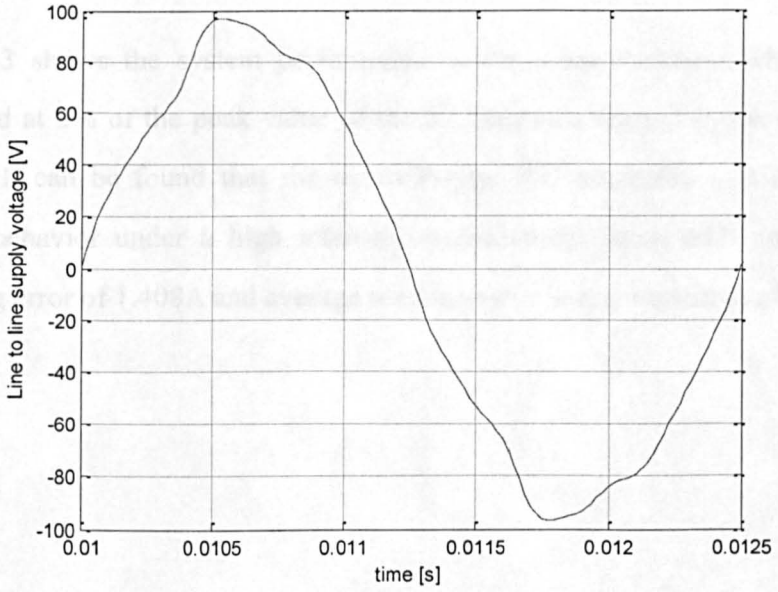


Figure 5. 11: Line to Line supply voltage with 5^{th}, 7^{th}, 11^{th} and 13^{th} harmonic distortion

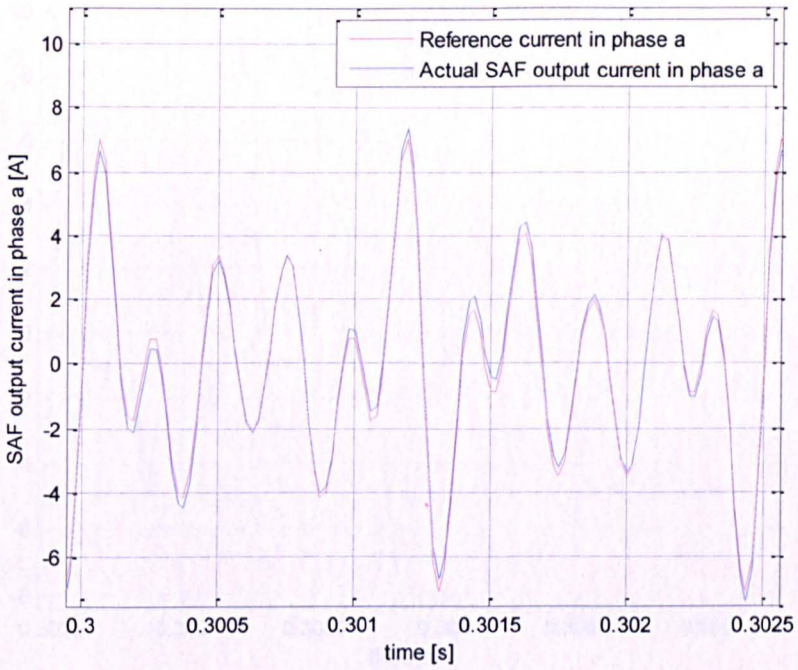


Figure 5. 12: Actual SAF current and reference current in phase a under supply voltage distortion (L= 1.2)

Fig 5.13 shows the system performance under a measurement white noise bounded at 3% of the peak value of the 5^{th} harmonic current in the reference signal. It can be found that the direct P-type ILC controller still maintains stable behavior under a high intensity measurement noise with maximum tracking error of 1.408A and average tracking error in one repetition of 0.629A.

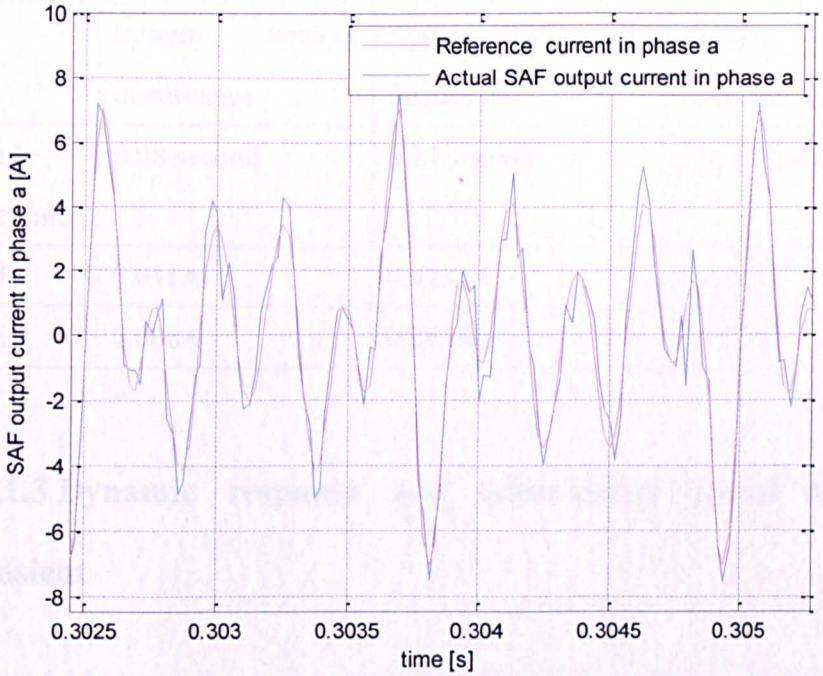


Figure 5. 13: Actual SAF current and reference current in phase a second under measurement white noise (L= 1.2)

Table 5.2 compares the simulation results obtained by the SAF system subject to disturbances, with the ones without disturbances. It can be observed that, when the P-type ILC controller operates subject to disturbance, it requires longer time to achieve steady state condition. This result matches the consideration presented in Chapter 4 stating that under bounded intensity of the disturbance, the P-type ILC controller has a slower error-decay speed.

Table 5. 2: SAF tracking capability under disturbed condition

	System without disturbance	System with supply distortion	System with measurement noise
Steady state time	0.08 second	0.27 second	0.3025second
MTE	0.011A	0.8233A	1.408A
ATE	0.006A	0.2518A	0.629A

5.5.1.3 Dynamic response and error-decay speed to load transient

Figure 5.14 shows the dynamic response of the direct P-type ILC controlled SAF system, when a load transient (for example from zero load to full) appears at 0.2 s. As shown on fig. 5.14, the direct P-type ILC controller takes about 0.01second to achieve steady state.

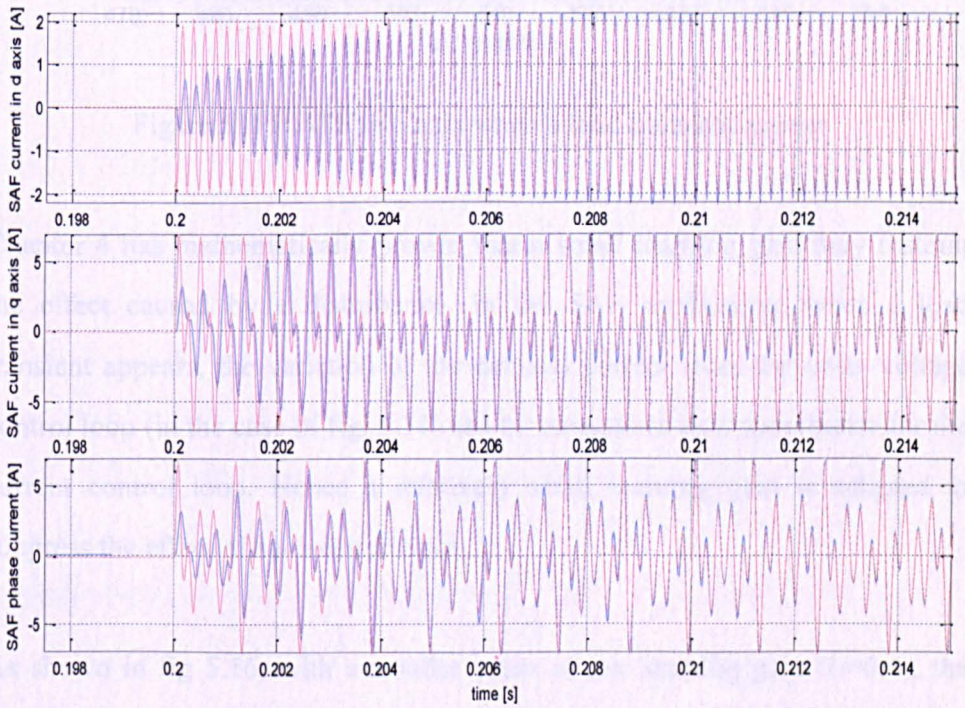


Figure 5. 14: Dynamic response of the direct P-type ILC controlled SAF system

As shown on fig. 5.15, when a load transient (from full load to zero) appears at 480th ILC repetition (0.2 s), the direct P-type ILC controller requires 70 ILC repetitions (0.0292s) to compensate the tracking error down to 0.1A. This simulation result proves that the direct P-type ILC controller is sensitive to variation in its reference.

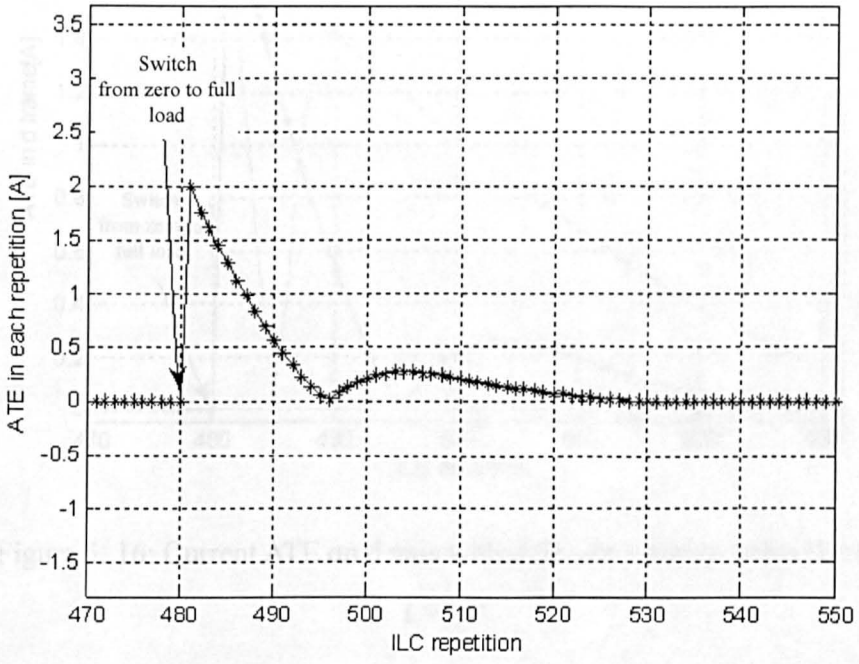


Figure 5. 15: ATE in q axis when a load transient appear

Chapter 4 has mathematically proven that a small learning gain may restrain the effect caused by a disturbance. In the SAF application, when a load transient appears, the variation of the demand current from the outer voltage control loop (in the case of fig. 5.14) can be recognized as a disturbance for the current control loop. Hence a relatively small learning gain is adopted to suppress the effect of such disturbance.

As shown in fig 5.16, with a smaller value of the learning gain (L=0.4), the ATE is significantly reduced in the first 6 repetitions. With the reduction of the demand current variation in the next repetitions, the system with larger learning

gain constant (L=1.2) gradually shows its better contribution to a faster error-decay speed.

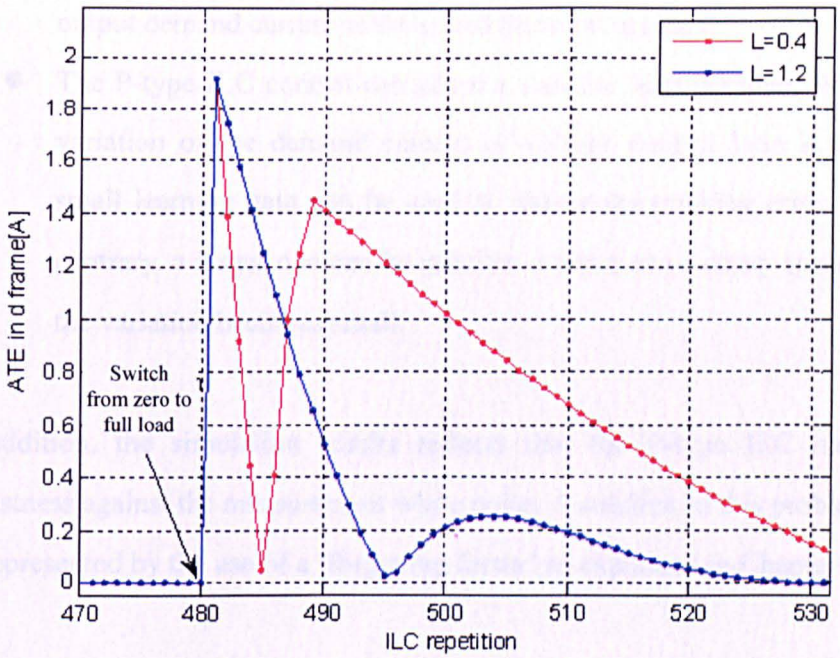


Figure 5. 16: Current ATE on d axis with different learning gains (L=1.2, L=0.8)

5.5.2 Methods to improve the P-type ILC controlled SAF system

Although the direct P-type ILC controller is able to provide almost zero steady state tracking error, it has low tolerance to variation in its current reference. This results in the controller to have poor dynamic response and slow error-decay speed during the load transient. The following methods can be indentifying to improve these limitations.

- A PI controller can be used to jointly with the P-type ILC controller to increase the closed loop bandwidth of the current control loop, thus

the dynamic response of the SAF control can be improved;

- The PI controller in the voltage control loop can be designed to give an over-damped response and therefore reduce the variation of its output demand current when a load transient appears;
- The P-type ILC control can adopt a variable learning gain. When the variation of the demand current of voltage control loop is large, a small learning gain can be used to reduce the tracking error. On the contrary, a larger one can be used for a faster error-decay speed when the variation becomes small.

In addition, the simulation results reflects that the P-type ILC has poor robustness against the measurement white noise. A solution to this problem will be represented by the use of a 'forgetting factor' as explained in Chapter 6.

5.6 Conclusion

This chapter has presented the control system structure of a SAF using a direct P-type ILC controller in the current control loop. The design procedure of the parameters of the direct P-type ILC controller including learning factor and memories is presented.

For the learning factor determination, a method based on the error-decay condition is introduced, which includes the design for both learning gain and phase shift component. During this design procedure, it has also been found that, the error-decay speed at certain frequencies can be increased by increasing the magnitudes or decreasing the phase shift of the control plant seen by the P-type ILC controller at those frequencies.

The simulation results in this chapter have also verified the correctness of the

robustness analysis performed in Chapter 4. Based on the improvement methods in section 5.5.2, a further investigation intending to optimize the P-type ILC controlled SAF system in term of dynamic response, error-decay speed and robustness will be addressed in next chapter.

Chapter 6 Optimizations of P-type ILC controlled SAF control system in fixed fundamental frequency

6.1 Introduction

Chapter 5 has presented the feasibility of applying the P-type ILC controller for the SAF current control. Although the direct P-type ILC controller can provide an accurate current tracking when applied to SAF current control, a slow dynamic response and a limited error-decay speed during a load transient cannot avoided. In addition, the direct P-type ILC controller has low tolerance to non-repetitive disturbances such as measurement white noise. Due to the limitations of a standard direct P-type ILC, in this chapter, optimizations of the P-type ILC controlled SAF system be conducted. In addition, this chapter will firstly modify the SAF system model with more consideration of the practical application.

To verify the validity and effectiveness of proposed optimization measures, theoretical analysis and simulation results will be shown.

6.2 Modifications of SAF system model

6.2.1 Implementing the diode bridge rectifier

In previous chapters, for the purpose of analyzing the reference tracking performance of the P+resonant and direct P-type ILC controller, the simulation

model used a signal generator to inject 5^{th}, 7^{th}, 11^{th} and 13^{th} current harmonics into the power network. However, such model is not much realistic. In this section, to reproduce a practical situation an inductively smoothed diode bridge rectifier is applied as the non-linear load in the power network to generate the current harmonics. Fig 6.1 shows the circuit structure of a diode bridge rectifier.

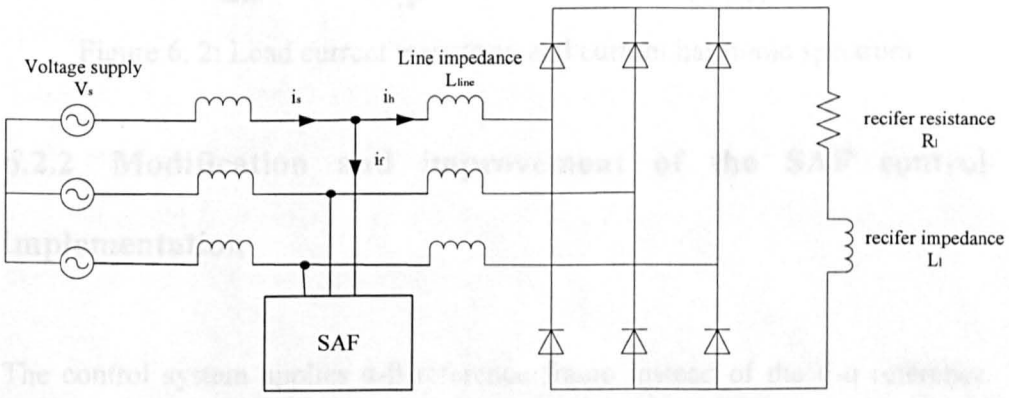


Figure 6. 1: Circuit structure of the diode bridge rectifier

Figure 6.2 shows the load current (ac-side current) with the diode bridge rectifier connected in the power network. The rectifier resistance and impendence are set to be 0.753mH and 49.2Ω respectively. The current harmonic spectrum clearly shows the presence of 5^{th}, 7^{th}, 11^{th}, 13^{th}, 17^{th} and 19^{th} current harmonics. Therefore, the SAF control system should provide an accurate current tracking at these harmonic frequencies for current harmonics cancellation.

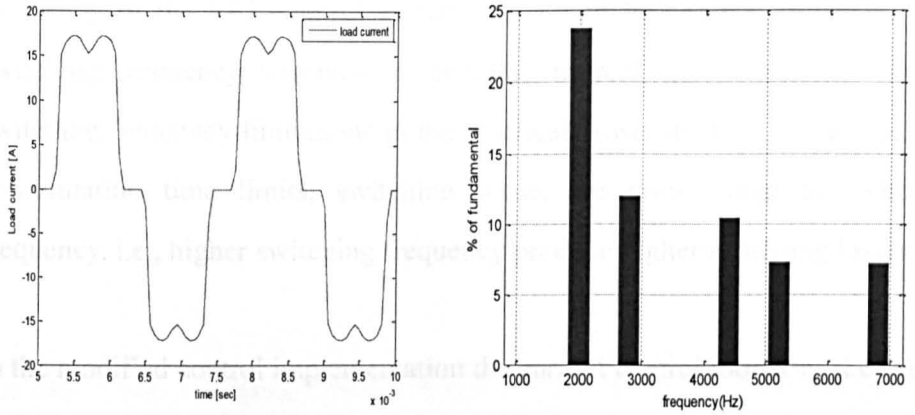


Figure 6. 2: Load current waveform and current harmonic spectrum

6.2.2 Modification and improvement of the SAF control implementation

The control system applies α-β reference frame instead of the d-q reference rotating frame. By doing so, the control system avoids conversions of the input signals from α-β frame to d-q frame, and the output signals from d-q frame to α-β frame. This means, the control system designed in α-β reference frame can reduce the computations in the DSP rather than the one designed in the d-q reference frame. With the SAF control system in the α-β reference frame, there are several modifications for the structure of the control system, which are presented in following sections.

6.2.2.1 Reference signal to the current control

In previous chapters, the current loop of the SAF control system was implemented in a standard d-q configuration and uses the load harmonic current in d-q rotating frame as the current reference. In order to accurately describe this reference harmonic current (including very high frequency signal) and the demand voltage in a discrete domain, the sampling and switching

frequency of the SAF control system was set to be 48KHz. However, such switching frequency becomes meaningless in real applications due to the switching frequency limitations in the practical power devices. In fact, besides commutation time limits, switching losses are proportional to switching frequency, i.e., higher switching frequency produce higher switching losses.

In the modified control implementation the current control loop uses the supply current (i_s) rather than SAF output current as the signal to be controlled. Therefore, for the supply current with a frequency of 400Hz, a sampling and switching frequency of 14400Hz will be adequate to represent the demand supply current in each ILC repetition for the P-type ILC current controller, giving a number of 36 samples per period.

However, the SAF control system actually controls the output current of the SAF (i_f). Thus the relationship between the tracking error of (i_f^*-i_f) and the demand and actual supply current (i_s^* and i_s) has to be determined. As discussed in chapter 3, the demand SAF output current (i_f^*) equals to the current harmonics (i_h). The actual supply current (i_s) can be recognized as a demand supply current which contains the harmonic current and the output SAF current ($i_s^*+i_h-i_f$). Therefore, the tracking error between the i_f^* and i_f can be represented by i_s and i_s^* as shown below[82],

$$i_f^* - i_f = i_h - i_f = (i_s^* + i_h - i_f) - i_s^* = i_s - i_s^* \tag{6.1}$$

6.2.2.2 System equation of voltage control loop

By using the α-β reference frame, the control plant of the voltage control loop is changed. The derivation of this control plant can be elaborated as follows.

By equaling the instantaneous power input to the instantaneous power output, we obtain,

$$V_{dc}i_{dc}^{*} = v_{f\_a}i_{f\_a} + v_{f\_b}i_{f\_b} + v_{f\_c}i_{f\_c} \tag{6.2}$$

For balanced steady-state operations that without the consideration of the load power, by neglecting the phase angle between the phase supply current and the PCC phase voltage, the following equation can be written:

$$i_{dc}^{*} = \frac{3V_{PCC}I_s}{2V_{dc}} \tag{6.3}$$

Where the V_s and I_s represent the amplitudes of the supply phase voltages and currents. The relationship between the V_s and V_{dc} for a classical carrier-modulated converter is:

$$V_{PCC} = m\frac{V_{dc}}{2} \tag{6.4}$$

Where, m is the modulation index. Substituting eq. (6.4) into (6.3), yields,

$$i_{dc}^{*} = \frac{3mI_s}{4} \tag{6.5}$$

Since the demand DC current (i_{dc}^{*}) can be determined by the equation $i_{dc}^{*} = C\frac{dV_{dc}^{*}}{dt}$. Combining this equation with eq. (6.5), the transfer function of the control plant for the voltage control loop can be written as,

$$P_{dc}(s) = \frac{V_{dc}}{I_s^*} = \frac{3m}{4Cs} \tag{6.6}$$

Through eq. (6.6), it can be found that, the controller in the voltage control loop, takes the tracking error of the DC voltage, and then produces the demand phase current amplitude (I_s^*) to compensate the tracking error.

6.2.2.3 System equation of current control loop

The modifications in the current control loop can be separated into two parts, which include the system plant model and the derivations of the current reference (i_{ref}^*).

The system plant model of the current control loop in α-β reference frame can be determined as follows. Kizkoff voltage law applied at the output circuit of the SAF can be written in α-β reference frame as,

$$\begin{aligned} v_{pcc\_\alpha} &= R_f i_{f\_\alpha} + L_f \frac{di_{f\_\alpha}}{dt} + v_{f\_\alpha} \\ v_{pcc\_\beta} &= R_f i_{f\_\beta} + L_f \frac{di_{f\_\beta}}{dt} + v_{f\_\beta} \end{aligned} \tag{6.7}$$

By defining a demand voltage v_f^* in the α-β reference frame as:

$$\begin{aligned} v_{f\_\alpha}^* &= R_f i_{f\_\alpha} + L_f \frac{di_{f\_\alpha}}{dt} \\ v_{f\_\beta}^* &= R_f i_{f\_\beta} + L_f \frac{di_{f\_\beta}}{dt} \end{aligned} \tag{6.8}$$

Equation (6.7) can be rewritten as,

$$\begin{aligned} v_{f\_\alpha} &= -v^{*}_{f\_\alpha} + v_{PCC\_\alpha} \\ v_{f\_\beta} &= -v^{*}_{f\_\beta} + v_{PCC\_\beta} \end{aligned} \tag{6.9}$$

Based on the above system equations, the cascade control loop of the SAF system in α-β reference frame can be designed as shown in fig. 6.3. The inner current control loop takes the demand current from outer voltage control loop (I_s^*) as the current reference amplitude. This is then multiplied by a sinusoidal three-phase template synchronous with the PCC voltage to generate the current reference.

The reference phase current of the current control loop can therefore be written as:

$$\begin{aligned} i^{*}_{ref\_a} &= I^{*}_{s}(\omega_s t + \varphi_s) \\ i^{*}_{ref\_b} &= I^{*}_{s}(\omega_s t + \varphi_s + 120^0) \\ i^{*}_{ref\_c} &= I^{*}_{s}(\omega_s t + \varphi_s - 120^0) \end{aligned} \tag{6.10}$$

Where I_s^* represents the demand supply current amplitude, which is the output of the voltage control loop, ω_s and φ_s are frequency and phase of the supply voltage identified with a PLL system.

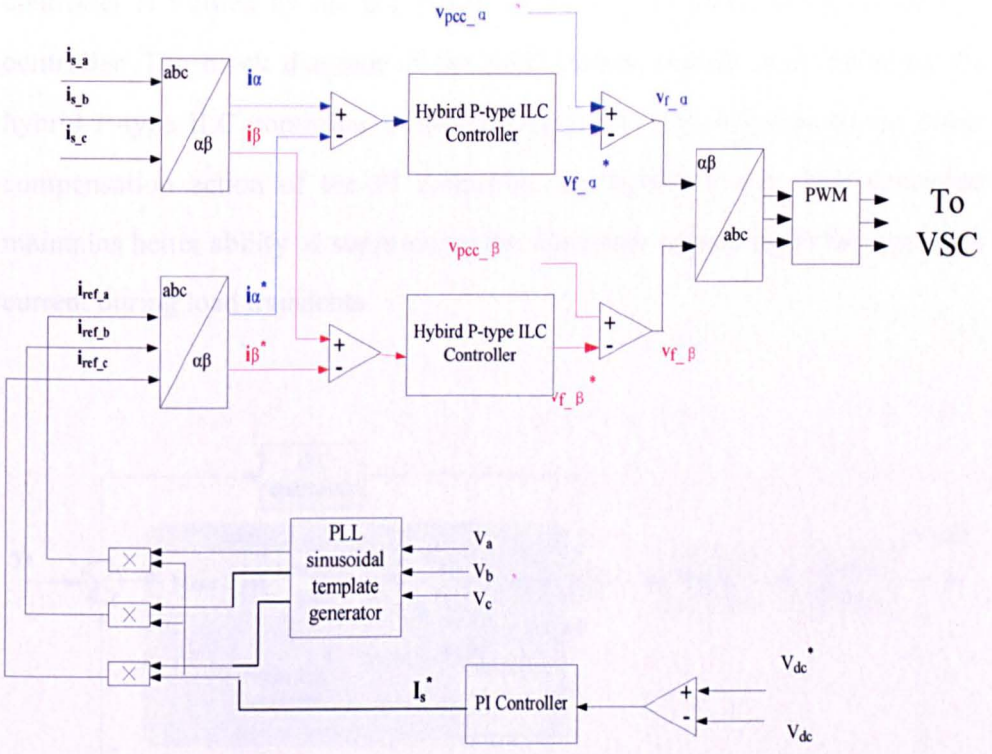


Figure 6. 3: Structure of control system in α-β frame

6.3 Hybrid P-type ILC controller for the improvement of dynamic response

The control philosophy of the P-type ILC controller is to learn the tracking error in the previous repetition and adjust the control signal to compensate the tracking error in the current repetition. This control action makes the direct P-type ILC controller very sensitive to variations in the reference signal, which determines a poor dynamic response of the P-type ILC controller during load transient, as presented in Chapter 5.

Research shows that a type of ILC control system called hybrid P-type ILC controller can provide a better dynamic response when compared with the direct P-type ILC controller [83] In this project, an hybrid P-type ILC

controller is formed by the combination of a PI controller and a P-type ILC controller. The block diagram of the SAF current control loop including the hybrid P-type ILC controller is shown in fig. 6.4. [66, 67] Due to the direct compensation action of the PI controller, the hybrid P-type ILC controller maintains better ability of suppressing the variations appearing in the reference current during load transients.

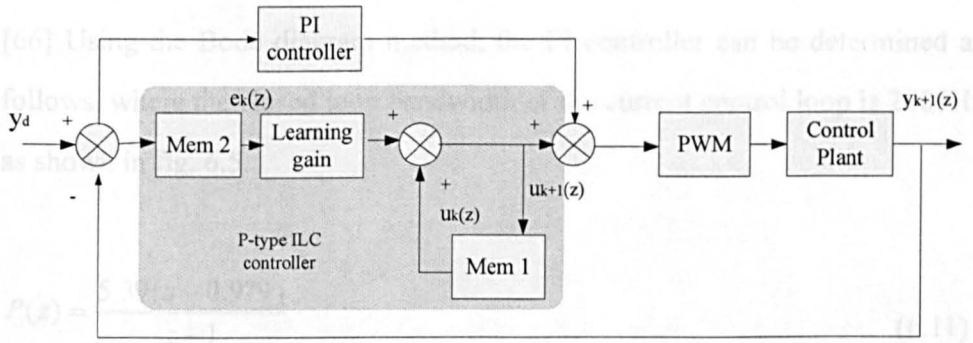


Figure 6. 4: Structure of the hybrid P-type ILC control in SAF system

This section will firstly introduce the traditional hybrid P-type ILC design procedure. For propose of increasing the error-decay speed produced by the P-type ILC controller at the process start and at any transient condition, an improved hybrid P-type ILC will be presented, together with proper design methodology.

6.3.1 Traditional design

The PI controller of the hybrid P-type ILC controller is usually designed by ignoring the P-type ILC term, and by using classical method like for example bode diagram or root locus. By knowing the transfer function of the P-type ILC control plant, the learning factor, including the learning gain (L) and the time advance unit (z^m), can be determined by the design procedures presented in Chapter 5.

In order to calculate the PI controller parameters the toolbox SISOTOOL in Matlab has been used. The parameters of the SAF have been presented in Chapter 3, while the SAF inductance L_f and internal resistance R_f are set to 1mH and 0.15Ω respectively. A unit delay (1/z) for one sampling period (1/14400 s) is also taken into account in this design to incorporate the computational delays of the digital control implementation. The PI controller is designed to compensate the high frequency harmonic components, thus the design specification of the PI controller simply is a high closed loop bandwidth. [66] Using the Bode diagram method, the PI controller can be determined as follows, where the closed loop bandwidth of the current control loop is 2085Hz as shown in fig. 6.5.

$$P(z) = \frac{5.39(z-0.979)}{z-1} \tag{6.11}$$

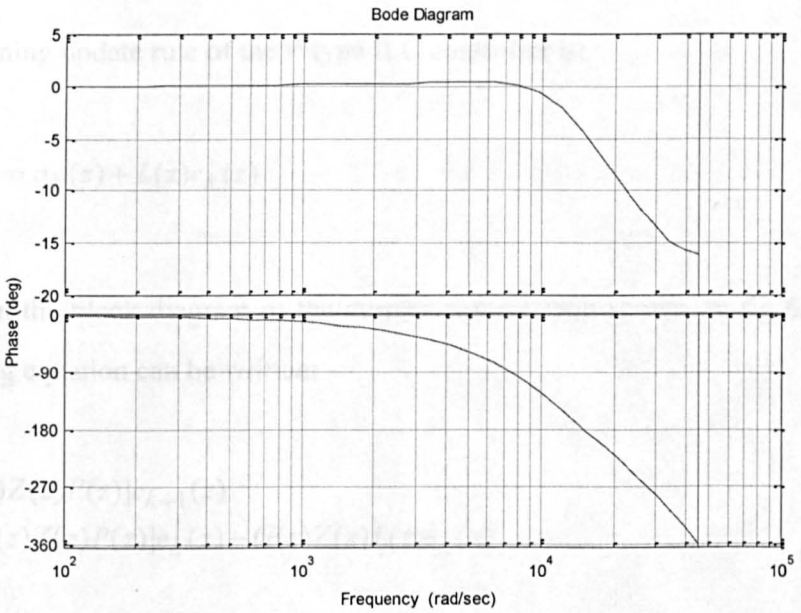


Figure 6. 5: Bode plot of the PI controller within the hybrid P-type ILC

Based on the structure of the SAF current control system shown on fig. 6.4, the block diagram of the SAF current control loop is presented on fig. 6.6, where G(z) represent the transfer function of the controlled plant in the discrete

domain. The transfer function of the PI controller is represented as P(z) in this diagram and $a_{k+1}(z)$ represents the output control signal from the P-type ILC controller. The transfer function of the control plant seen by the P-type ILC control plant can be determined by a similar derivation procedure as the one in section 5.3.1.

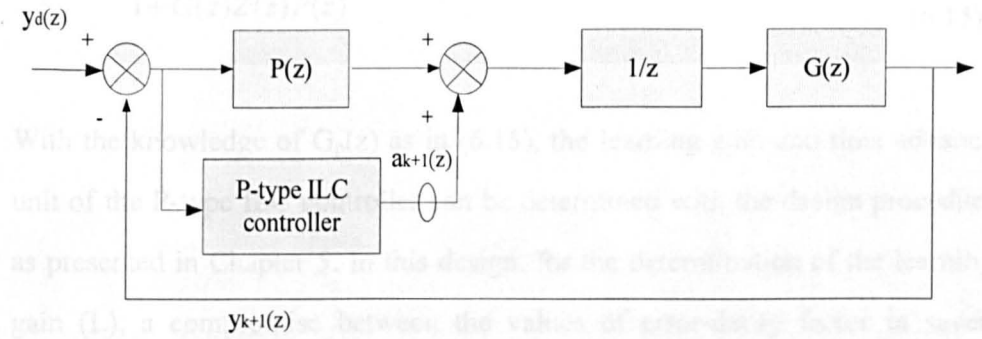


Figure 6. 6: Block diagram of SAF current control loop with hybrid P-type ILC

The learning update rule of the P-type ILC controller is:

$$a_{k+1}(z) = a_k(z) + L(z)e_k(z) \tag{6.12}$$

Based on the block diagram of the current control loop shown on fig 6.5, the following equation can be written:

$$\begin{aligned}&[1+G(z)Z(z)P(z)]e_{k+1}(z)\\&=[1+G(z)Z(z)P(z)]e_k(z)-G(z)Z(z)L(z)e_k(z)\end{aligned} \tag{6.13}$$

Hence the error in the next repetition can be written as:

$$e_{k+1}(z) = (1 - L(z)\frac{G(z)Z(z)}{1+G(z)Z(z)P(z)})e_k(z) \tag{6.14}$$

Comparing eq. (6.14) with eq. (4.7) (the equation of error-decay condition), the transfer function of the control plant seen by the P-type ILC control can be derived as [79]:

$$G_p(z) = \frac{G(z)Z(z)}{1+G(z)Z(z)P(z)} \tag{6.15}$$

With the knowledge of $G_p(z)$ as in (6.15), the learning gain and time advance unit of the P-type ILC controller can be determined with the design procedure as presented in Chapter 5. In this design, for the determination of the learning gain (L), a compromise between the values of error-decay factor in seven proposed frequencies (fundamental, 5^{th}, 7^{th}, 11^{th}, 13^{th}, 17^{th} and 19^{th} harmonic frequencies in the load current as presented in Section 6.2.1) will be required.

Figure 6.7 shows the Nyquist diagram of $L(e^{j\omega T_s})G_p(e^{j\omega T_s})$, where the learning gain is chosen to be 3.7 and the time-advance unit is set to z^2. It can be observed that, the curve of $L(e^{j\omega T_s})G_p(e^{j\omega T_s})$ lies inside the unit circle according to the method described in Chapter 5; hence as shown in fig. 6.7, the hybrid P-type ILC with the determined learning factor is capable to reduce the tracking error with the frequencies from zero to the Nyquist frequency.

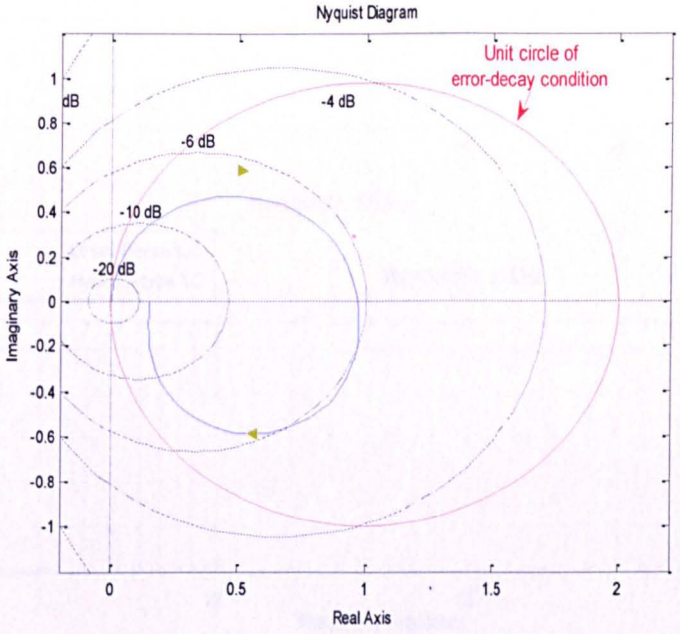


Figure 6. 7: Nyquist diagram of $3.7z^2G_p(z)$ determined by traditional method

Analyzing the closed loop bode plot shown in fig. 6.8, it can be found that, the behavior of the P-type ILC is similar to the one of the P+resonant control (see in Chapter 3); the P-type ILC provides high gains at all the frequencies of the harmonic components. As shown in fig. 6.8, without considering the harmonic frequencies, the hybrid P-type ILC controller provides a wider closed loop bandwidth than the direct one. This means the hybrid P-type ILC scheme can improve the dynamic response of the control system.

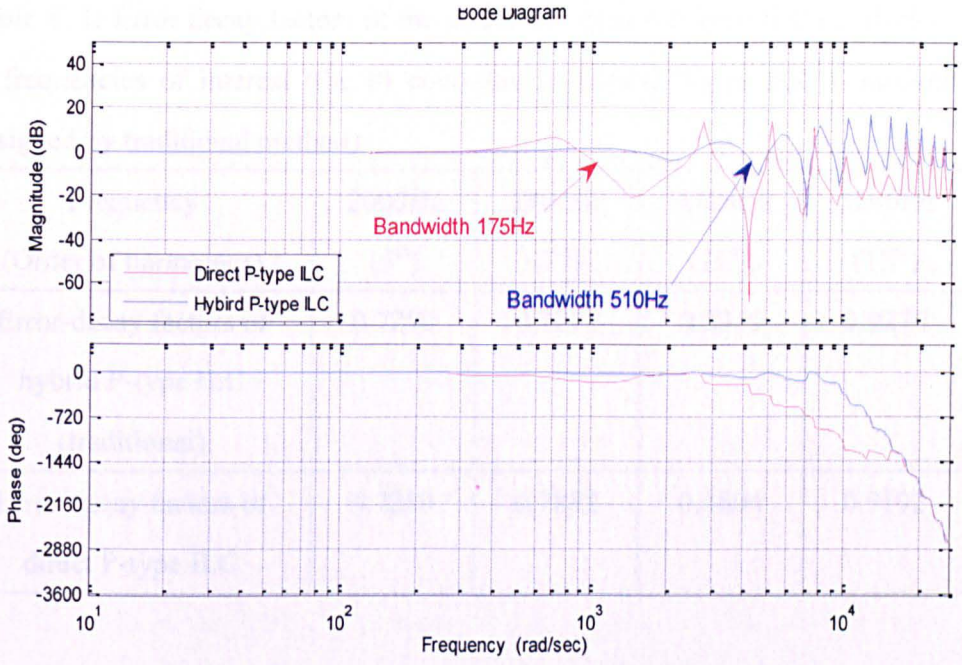


Figure 6. 8: Bode plot of the SAF current control loop with direct and hybrid P-type ILC controller (traditional design) respectively

However, from table 6.1, it can be seen that, the error-decay factors of the hybrid P-type ILC controller are larger than the direct ILC. This means the main disadvantage of such design procedure is that the error-decay factor of the P-type ILC may become relatively large since the PI controller is designed without the consideration of the effect from the P-type ILC controller. i.e., the error-decay speed of the hybrid P-type ILC controller will be limited.

Table 6. 1: Error decay factors of the direct and hybrid P-type ILC controllers at frequencies of interest (the PI controller in hybrid P-type ILC controller designed by traditional method)

Frequency (Order of harmonics)	2000Hz (5^{th})	2800Hz (7^{th})	4400Hz (11^{th})	5200Hz (13^{th})
Error-decay factors of hybrid P-type ILC (traditional)	0.7290	0.8231	0.8919	0.9279
Error-decay factors of direct P-type ILC	0.7280	0.7882	0.8804	0.9192

6.3.2 Improved design

Due to the limitation shown by the hybrid P-type ILC with traditionally designed PI, an improved design method will be hence introduced. Through eq. (6.15), it can be found that, the design choice of the PI controller (P(z)) can modify the magnitude and phase of the frequency response of the control plant seen by the P-type ILC controller ($G_p(z)$). As discussed in section 5.3.3, the P-type ILC controller has relatively slow error-decay speeds at harmonic frequencies, because the control plant $G_p(z)$ has small magnitudes and large phase shifts in the high frequency range. These factors can result in a large error-decay factor at the harmonic frequencies of interest.

Thus an optimized design of the PI controller needs to address two main issues: 1) produce a satisfying dynamic response of the SAF current control; 2) produce a magnitude increase and phase shift decrease of $G_p(z)$ at the frequencies of interest for the control, so that the error-decay factor at these frequencies can be reduced. This can be achieved through an iterative trial and error procedure. The transfer function of the PI controller chosen in this design

is presented as follows:

$$P(z) = \frac{4.1(z-0.973)}{z-1} \tag{6.16}$$

Based on the transfer function of P(z), the transfer function of $G_p(z)$ can be determined. In accordance with the design procedure and SAF data presented in section 5.3, the learning gain and phase shift components can then be determined. , which are L=3.2 and a time-advance unit z^2 respectively.

From fig. 6.9, it can be found that, including the transfer function of the PI controller the P(z) in eq. (6.16), the hybrid P-type ILC controller produces a closed loop bandwidth of 302.4Hz (not considering the harmonic frequencies). This means that the optimized design of the PI controller generates a preferable dynamic response of the overall current control system.

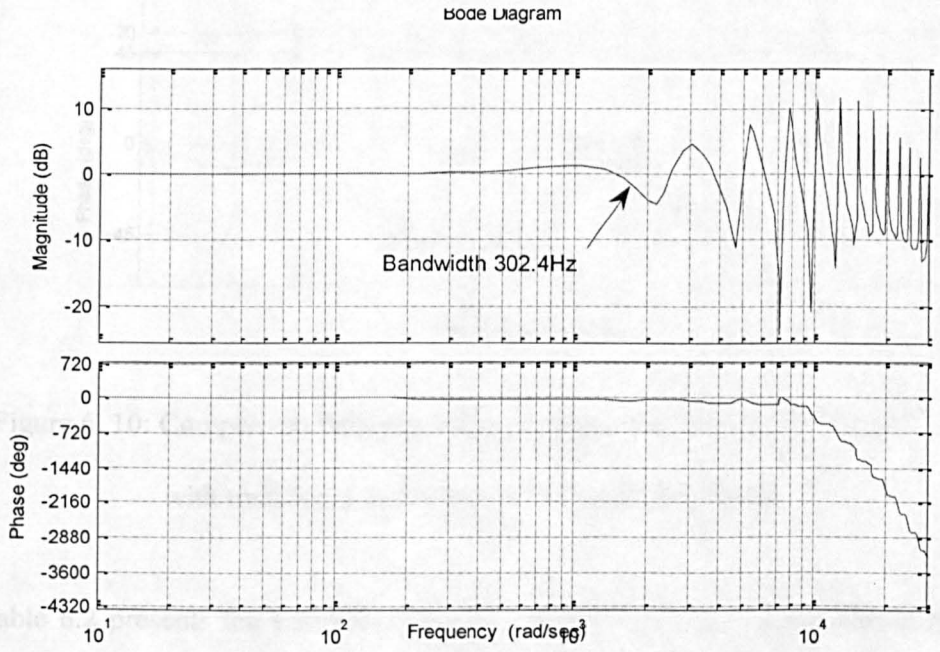


Figure 6. 9: Bode plot of the SAF current control loop with hybrid P-type ILC controller (improved design)

Figure 6.10 presents the magnitude and phase curves of $L(e^{j\omega T_s})G_p(e^{j\omega T_s})$ in both case of PI designed with traditional and improved methods. Through fig 6.10, it can be seen that, comparing the magnitude curves of $3.7z^2G_{p\_traditioanl}(z)$ and $3.2z^2G_{p\_improved}(z)$ the last one, which is designed using the improved PI has higher magnitudes at harmonic frequencies of interest (≥2000Hz). It can also be observed that, in this harmonic frequency range, the phase curve obtained by the improved method has smaller phase shift than the traditionally designed one. This means, a faster error-decay speed for the harmonic current tracking error.

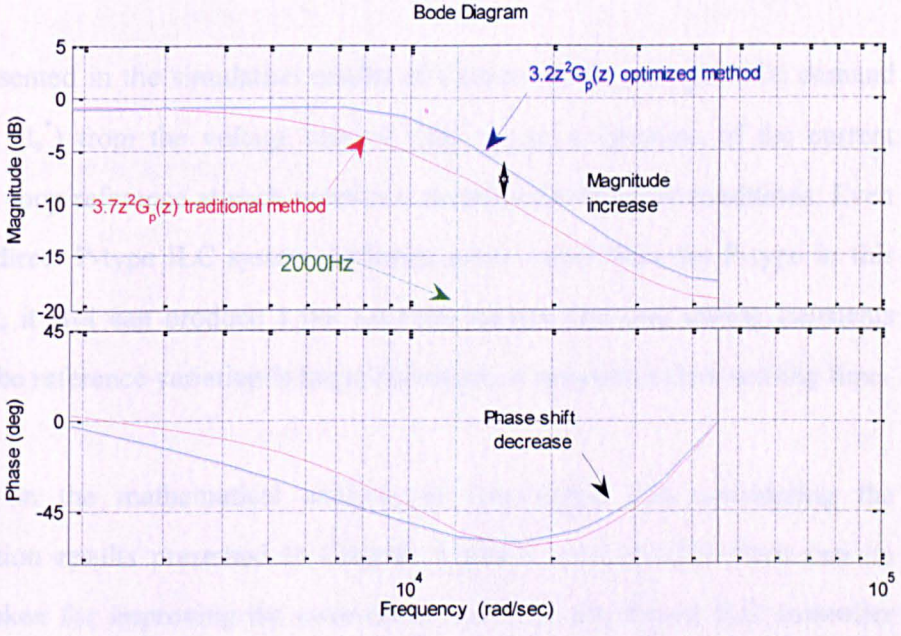


Figure 6. 10: Comparison between frequency responses of $L(e^{j\omega T_s})G_p(e^{j\omega T_s})$ with traditional and improved PI controller design

Table 6.2 presents the error-decay factors of the P-type ILC controller at the harmonic frequencies of interest using the improved design. Compared with tab.6.1, the improved design method provides smaller error-decay factor at considered harmonic frequencies.

Table 6. 2: Error decay factors of the P-type ILC controller at specific frequencies with improved PI design

Frequency	2000Hz (5^{th})	2800Hz (7^{th})	4400Hz (11^{th})	5200Hz (13^{th})
Error-decay factor of hybrid P-type ILC (novel)	0.6330	0.7468	0.7647	0.8108

6.4 Optimizations for increasing the error-decay speed during the load transient

As presented in the simulation results of Chapter 5, the non-periodic demand current (I_s^*) from the voltage control loop causes a variation of the current control loop reference at each repetition during load transient conditions. Even if the direct P-type ILC system performs much better than the P-type in this respect, it still can produce a not accurate current tracking during transients when the reference variation is large; moreover, it presents a slow settling time.

Based on the mathematical analysis of robustness, and considering the simulation results presented in Chapter 4 and 5, two specific steps can be undertaken for improving the error-decay speed of the P-type ILC controller during a large variation in the current reference. The first one simply consists in reducing the variation of the demand current from the outer voltage control loop. It needs to be mentioned that, the outer voltage control loop cannot very quickly; hence an over-damped voltage controller should be used to reduce the variation of the demand current. The second is to design a P-type ILC controller with variable learning gain to guarantee the fastest error-decay speed in initial repetitions just after a transient has happened. With these two solutions plus the optimized hybrid P-type ILC controller, the overall control

system structure can be re-drawn as shown in fig. 6.11.

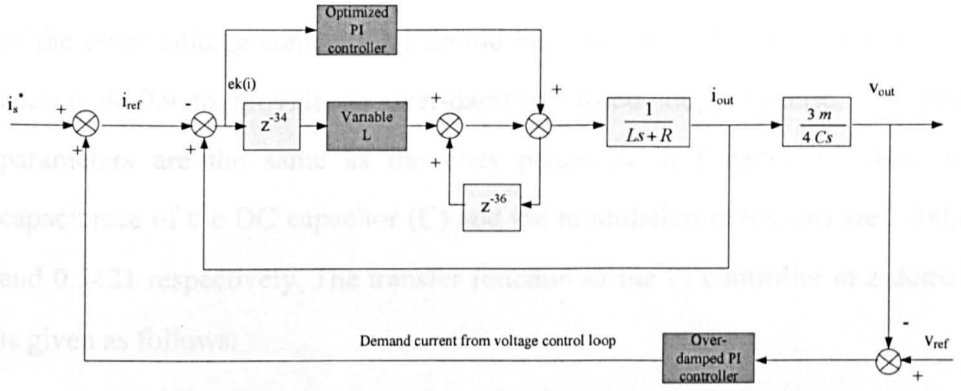


Figure 6. 11: Structure of the optimized SAF control system

6.4.1 Over-damped design of the PI controller in voltage control loop

As mentioned earlier, a larger variation of the demand current from the outer voltage control loop can reduce the error-decay speed of the P-type ILC controller. A slower dynamics of the voltage control loop is therefore desirable to counteract this trend and reduce the variation of the demand current in each repetition. On the other hand, a too slow voltage control could create stability concerns in the case of SAF load transient operative conditions. A compromised solution is represented by a PI design for the voltage control loop which produces an over-damped closed loop response rather than an under-damped one.

Given that current and voltage loops are in a cascade configuration, it is required the internal loop to have a bandwidth much faster than the external one (usually at least 10 times), this is to ensure that variation in the output of

the external loop are tracked by the internal loop and also to ensure that the two loops can be designed separately. With the consideration of the closed loop bandwidth of the inner current control loop is 302.4Hz, the demand bandwidth of the outer voltage control loop should be max 30Hz. The damping factor is chosen at 0.9 to provide an over-damped closed loop response. The plant parameters are the same as the ones presented in Chapter 3, where the capacitance of the DC capacitor (C) and the modulation index (m) are 2200μF and 0.5421 respectively. The transfer function of the PI controller in z-domain is given as follows:

$$P_{voltage\_control}(z) = \frac{0.716(z-0.998)}{z-1} \tag{6.17}$$

6.4.2 Variable learning gain

The robustness analysis in Chapter 4 and the simulation results in Chapter 5 prove that the P-type ILC control with a smaller learning gain (L) has a faster error-decay speed when a large disturbance occurs in the SAF current control loop. However, along with the reduction in the disturbance intensity, the smaller L can actually reduce the error-decay speed for the P-type ILC controller. Therefore, if the value of learning gain (L) is made variable according to the intensity of the disturbance, then the P-type ILC controller could achieve optimized error-decay speed in each different condition.

As shown in fig. 6.12, in the case that the SAF is enabled to full load at 0.1 second, the ideal solution is to set a small value of L when the variation in the current reference is large and to increase the value of L in each repetition in function of the attenuation of this reference variation, lastly reaching a final larger learning gain value when the reference variation is negligible.

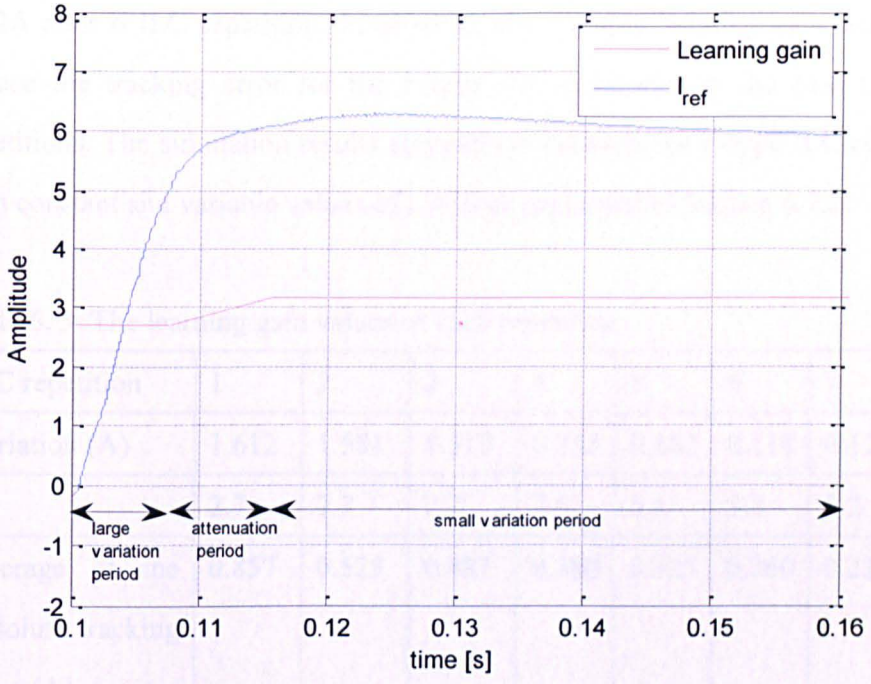


Figure 6. 12: Concept of the value of learning gain varying with the demand current at the system state-up

However, there is no deterministic relationship between the value of the learning gain (L) and the intensity of the disturbance. The approach used in this method firstly finds the most suitable value of L which can provide the faster error-decay within the first repetition. Then using the value of L generated from the previous repetition as a reference point, it derives the value of L for the next repetition using the same method; this is iterated for the subsequent repetitions till the disturbance becomes negligible.

The variable value of L is here designed for the control system with the optimized hybrid P-type ILC controller (presented in section 6.3.2) and the modified voltage control loop PI controller (presented in section 6.4.1). In tab.6.3, the second row shows the average variation of the current reference between the n^{th} and the $(n+1)^{th}$ ILC repetition; the third row shows the learning gain values of each corresponding ILC repetition determined by the proposed

method. It is clear that the variation of the current reference is decayed to 0.12A after 6 ILC repetition. Meanwhile, the variable learning gain helps to reduce the tracking error for the P-type ILC controller in the first 5 ILC repetitions. The simulation results comparison between the P-type ILC control with constant and variable values of L will be presented in Section 6.7.2.

Table 6. 3: The learning gain values of each repetition

ILC repetition	1	2	3	4	5	6	7
Variation (A)	1.612	1.581	1.517	0.753	0.383	0.118	0.124
L	2.7	2.7	2.7	2.9	3.1	3.2	3.2
Average of the absolute tracking error (A)	0.857	0.525	0.487	0.380	0.325	0.260	0.223

6.5 Using the forgetting factor α to increase system robustness against measurement noise

The forgetting factor is a variation the P-type ILC controller, which has been successfully used to improve the ILC system robustness against measurement white noise and initialization error in the robotic motions application. [75] Due to the high performance of this solution presented in [84, 85], the forgetting factor is here applied to optimize the P-type ILC controller performance in the SAF system.

Figure 6.13 presents the P-type ILC controller structure including a forgetting factor. The feedback of the control signal $u_k(z)$ is fed through a gain $(1-\alpha)$, where α is a small positive constant. A disturbance $d_k(z)$ representing the measurement noise is added to the output signal of the control plant $y_k(z)$.

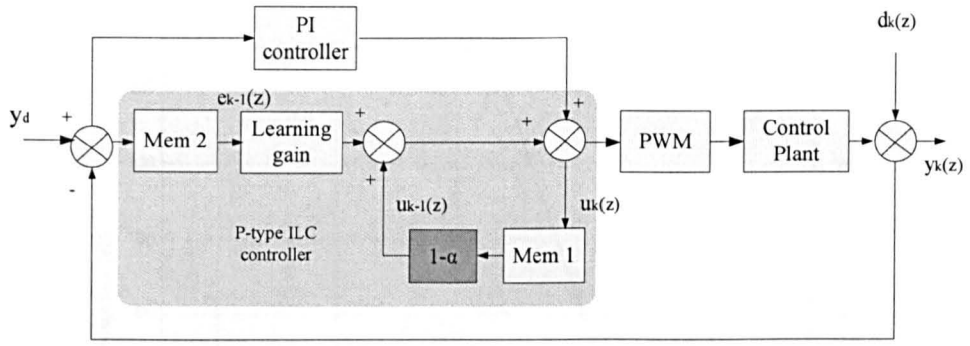


Figure 6. 13: Structure of the P-type ILC controller with forgetting factor

As shown in fig.6.13, the forgetting factor is used to reduce the value of control signal u_k and the tracking effectiveness is reduced, which means when the measurement noise causes a tracking error in one repetition, the P-type ILC controller with a forgetting factor will distract the attention of the tracking error compensation in following repetitions.

As shown in the zoom in the frequency response of the P-type ILC around the 5^{th} harmonic frequency with different forgetting factor values (fig. 6.14), the forgetting factor narrows the pass-bandwidth at the harmonic frequencies and the degree of such compensation is related to the value of α, i.e. a smaller α means more effectiveness on compensating the tracking error (higher gain). On the other hand, a larger α indicates higher steady-state tracking error (lower gain). It is found that, a value of α equals to 0.01 provides preferable pass-bandwidth and gain for the P-type ILC controller.

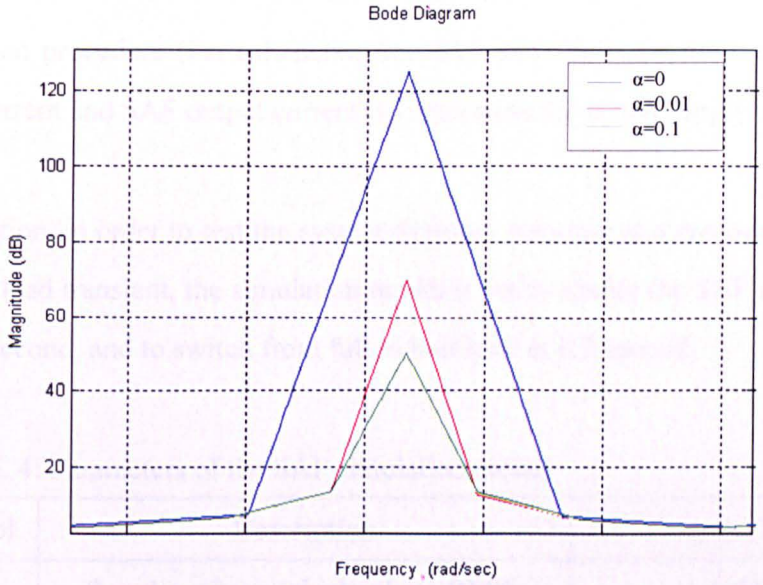


Figure 6. 14: Frequency response of the P-type ILC controller with different forgetting factors

6.6 Simulation model

The improved hybrid P-type ILC SAF control has been verified through simulation. The power network, the SAF and the proposed control system are modeled using Matlab-Simulink and the Simpower toolbox. The parameters of the simulation model are summarized in tab.6.4.

The schematic diagram reproducing the simulation model is shown in fig. 6.15. The power network of the SAF system and the electrical part of the simulation model (i.e. three phase two level VSC, three phase diode bridge rectifier) have been created by using Simpower toolbox.

The simulation model control part (described in Section 6.2.3) is implemented using Simulink discrete blocks. It is worth highlighting that, since in the experimental rig (get ready in Section 8.2.3) the measurement of the supply

current is not available, thus the simulation model follows the practical operation procedure (i.e. calculating the difference between the measured the load current and SAF output current) to determine the actual supply current.

In addition, in order to test the system dynamic response and error-decay speed during load transient, the simulation model is set to enable the SAF to full load at 0.1 second, and to switch from full to half load at 0.3 second.

Table 6. 4: Parameters of the SAF simulation model

Symbol	Description	Nominal value
V_s	Supply voltage (single phase RMS)	115V
F	Frequency of supply voltage	400Hz
V_{dc}	DC-link voltage of capacitor in VSC	400V
C_{dc}	DC capacitance	470μF
L_s	Line inductance	0.01mH
L_f	Filter input inductance	1mH
R_f	Filter input resistance	0.15Ω
L_l	Rectifier Load inductance	0.753mH
R_l	Rectifier Load resistance	49.2Ω
F_s	Sampling frequency	14400Hz
F_{sw}	Switching frequency	14400Hz

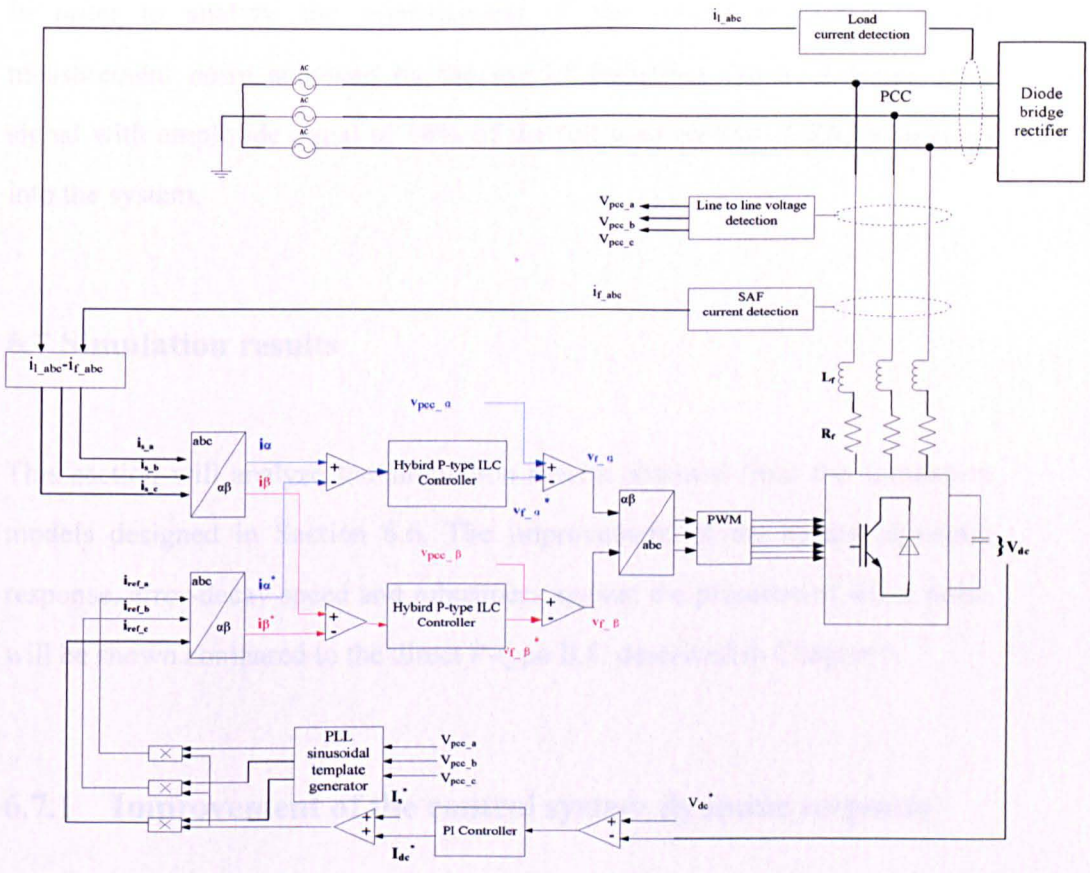


Figure 6. 15: Simulation model of the overall SAF system

The SAF control has been tested for dynamic and steady state operations defined as follows:

- Dynamic response and error-decay speed: the performance of SAF system with a direct P-type ILC controller (described in Chapter 5) is compared with the one containing the optimized hybrid P-type ILC (described in Section 6.3.2), the variable learning gain constant component (described in Section 6.4.2) and the over-damped voltage control loop (described in Section 6.4.1).
- Performance of the SAF system with optimized control in steady state condition.

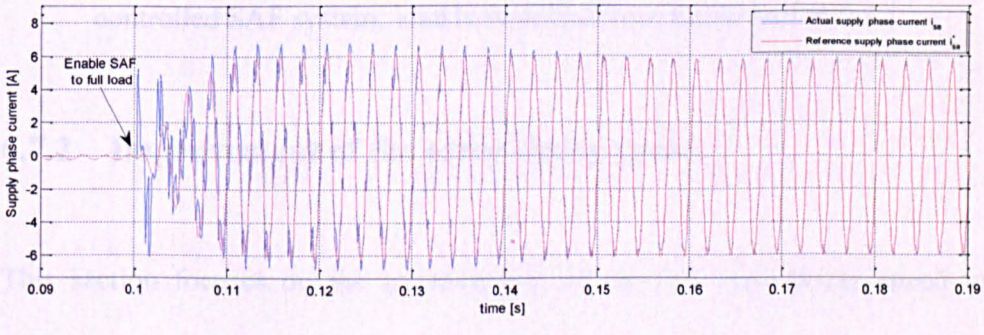
In order to analyze the improvement of the system robustness against measurement noise achieved by the use of forgetting factor, a white noise signal with amplitude equal to 10% of the full load current (5.8A) is injected into the system.

6.7 Simulation results

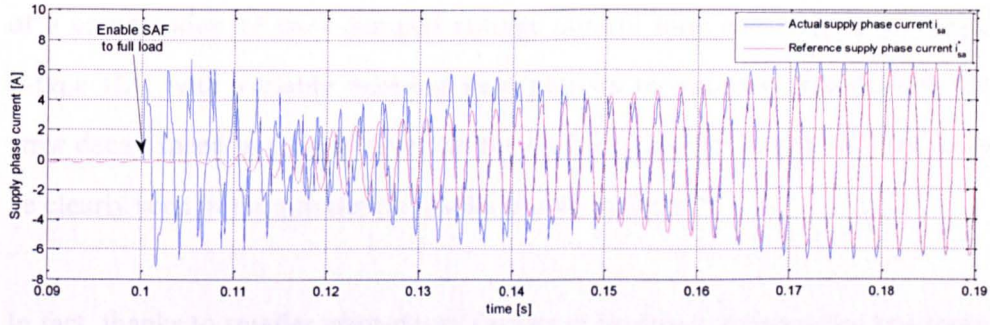
This section will analyze the simulation results obtained from the simulation models designed in Section 6.6. The improvement of the system dynamic response, error-decay speed and robustness against the presence of white noise will be shown compared to the direct P-type ILC described in Chapter 5.

6.7.1 Improvement of the control system dynamic response

Figure 6.16 presents the current reference tracking when using both direct and hybrid P-type ILC controller; the SAF system is enabled to full load at 0.1 second. Figure 6.17 presents the current reference tracking when using both direct and hybrid P-type ILC controller during a load step change from full to half load at 0.3 second. The simulation results in fig.6.16 and 6.17 shows clearly that the optimized hybrid P-type ILC can actually provide an overall better dynamic response over the direct one for the SAF current control.

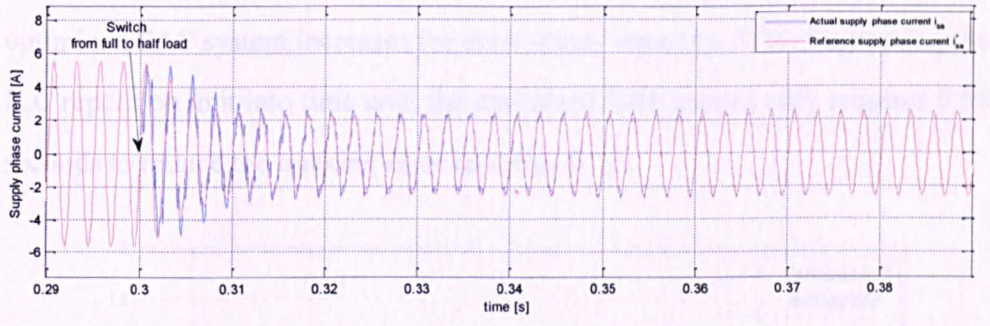


(a)

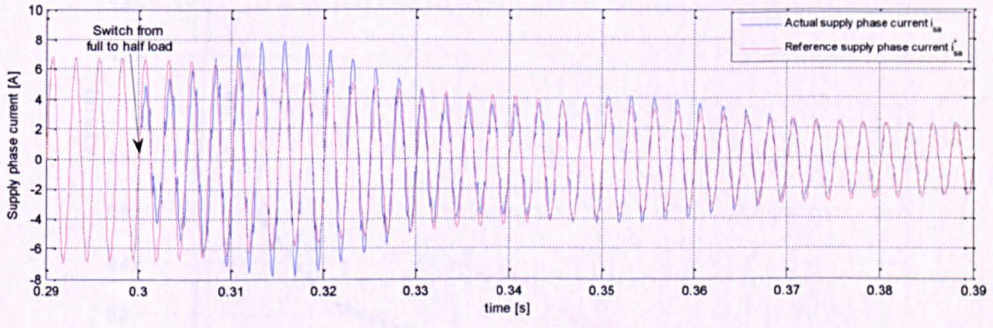


(b)

Figure 6. 16: Supply current tracking using hybird (a) and direct (b) P-type ILC controlled SAF system, SAF is enabled to full load at 0.1 s



(a)



(b)

Figure 6. 17: Supply current tracking using hybird (a) and direct (b) P-type ILC controlled SAF system; load is switched from full to half at 0.3 s

6.7.2 Improvement of the error-decay speed

This section focuses on the improvement of the ILC error-decay speed in

transient conditions. For example, when the SAF is enabled to full load, the use of a combination of over-damped voltage control loop and optimized hybrid P-type ILC with variable learning gain permits to improve significantly the error decay speed in comparison with the traditional direct P-type ILC, as it can be clearly seen in the simulation results shown in fig.6.18 .

In fact, thanks to smaller error-decay factors at harmonic frequencies and faster transients, the optimized hybrid P-type ILC controller reduces the tracking error to less than 0.1A within 20 ILC repetitions. Compared with the performance of the SAF system with standard direct P-type ILC controller, the optimized SAF system increases the error-decay speed by 57%. Converting the ILC repetition unit into time unit, the optimized SAF control only requires 0.05 seconds to reduce the tracking error less than 0.1A.

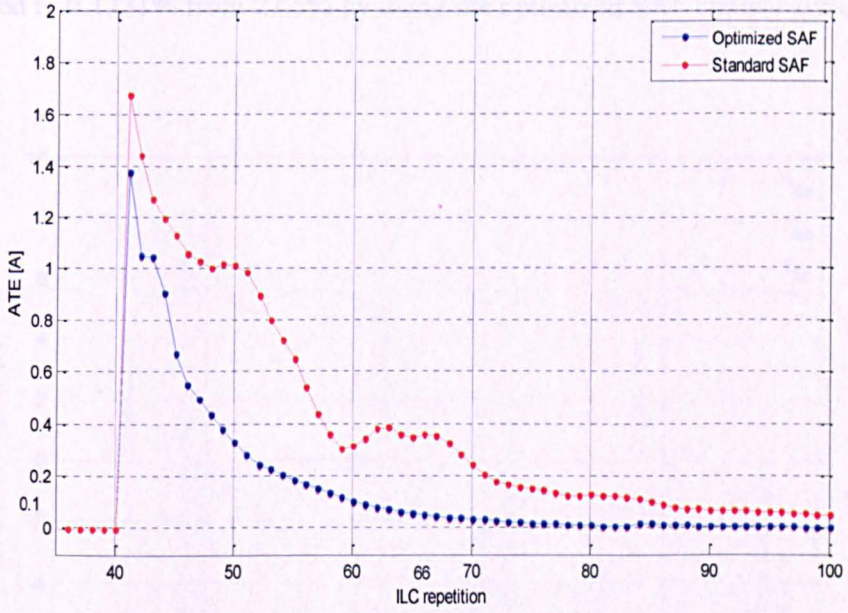


Figure 6. 18: Average supply phase current tracking error when using the standard direct P-type ILC controller and the optimized one with variable L and over-damped voltage control loop

6.7.3 Current harmonics attenuation

Figure 6.19a and 6.19b show the three phase supply current waveforms without and with the compensation of the SAF system. Similarly, figure 6.20a and 6.20b show the harmonic spectrums of the supply current under the same circumstances. As presented in fig.6.19, the optimized SAF system successfully compensates the current harmonics caused by the non-linear load. It has to be mentioned that, regularly the THD should contains the harmonics till the 40^{th}; however, in this application, the switching frequency (14400Hz) is lower than the frequency of the 40^{th} harmonic (16000Hz). Therefore, the harmonics at the switching frequency is not taken into account in the following THD calculation. The corresponding current harmonic spectrums presented in fig.6.20 shows the total harmonic distortion (THD) in the supply current is reduced to 0.1331% from 27.5% by using the optimized SAF control system.

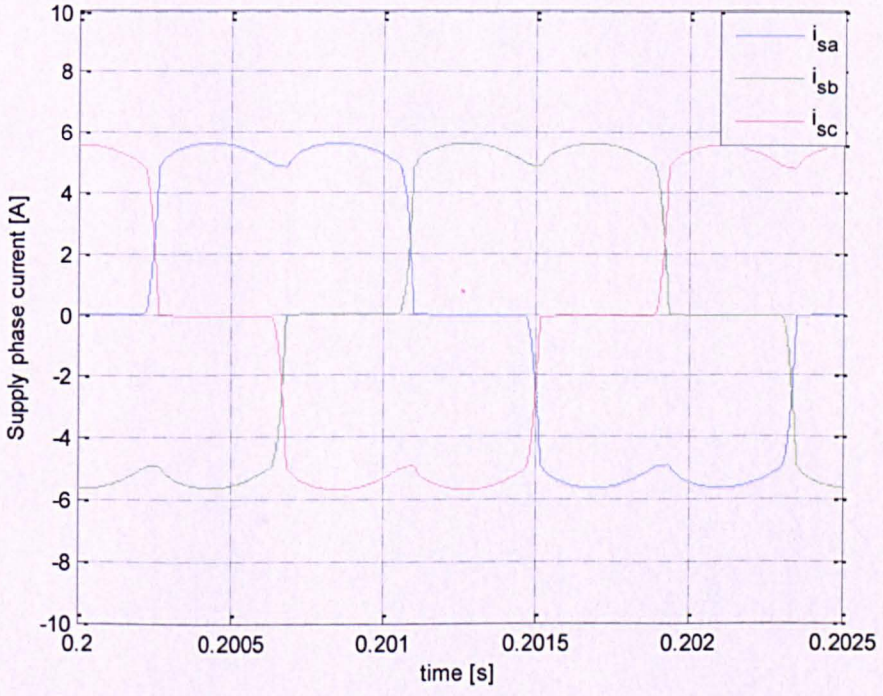


Figure 6. 19a: Supply current before compensation

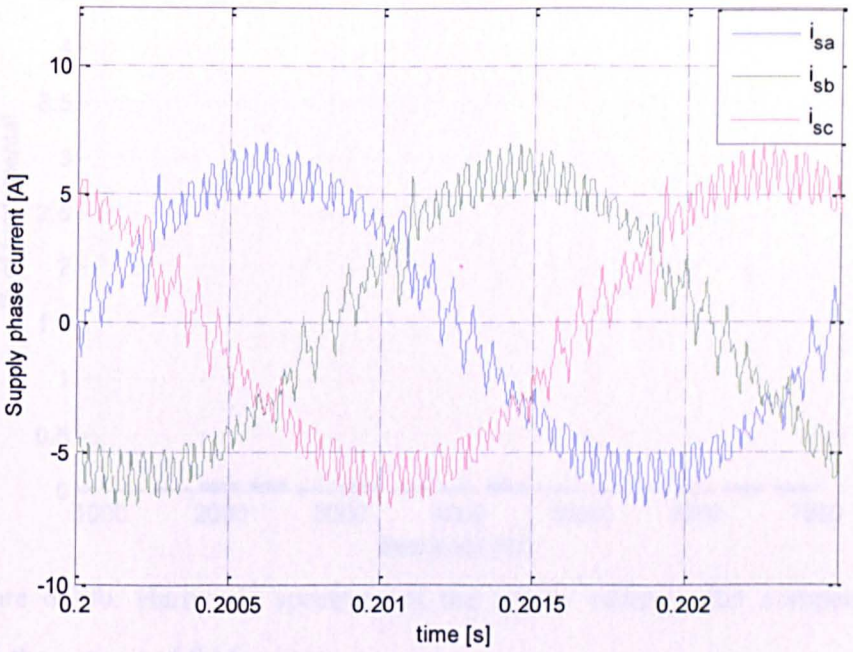


Figure 6.19b: Supply current after compensation with the optimized SAF system

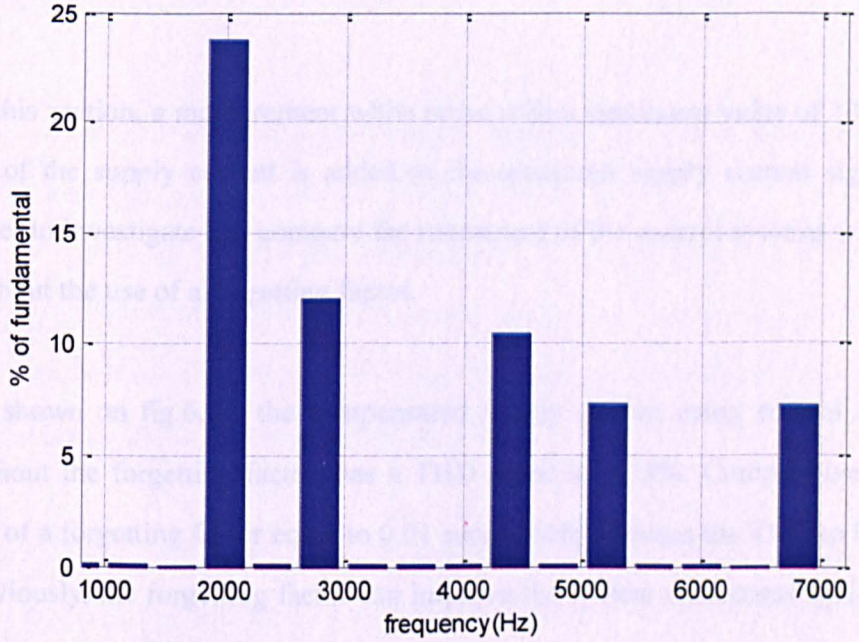


Figure 6. 20a: Harmonic spectrum of the supply current before compensation

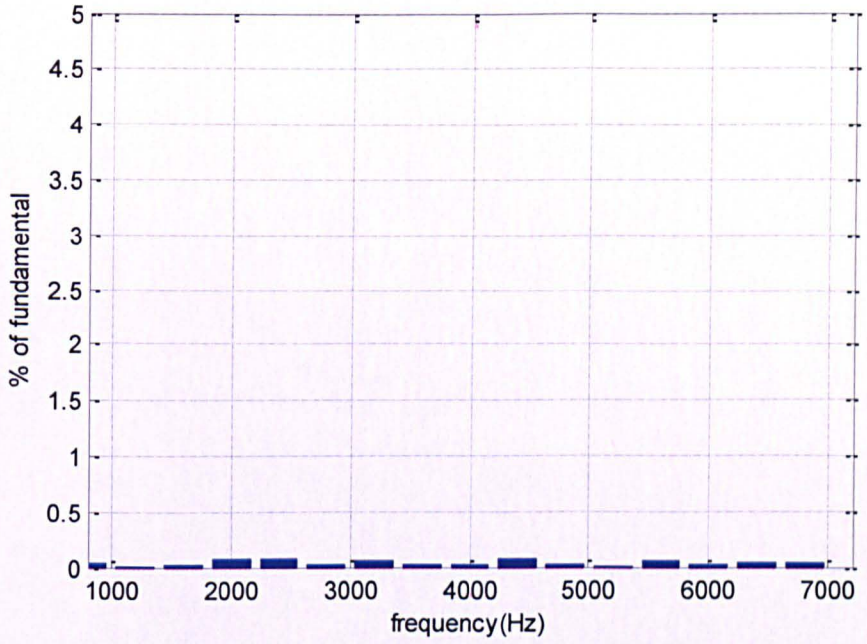


Figure 6.20b: Harmonic spectrum of the supply current after compensation with the optimized SAF system

6.7.4 Robustness of the control system against measurement noise

In this section, a measurement white noise with a maximum value of 10% (0.6 A) of the supply current is added to the measured supply current signal, in order to investigate and compare the robustness of the control systems with and without the use of a forgetting factor.

As shown on fig.6.21, the compensated supply current using control system without the forgetting factor, has a THD equal to 1.33%. Comparatively, the use of a forgetting factor equal to 0.01 successfully reduces the THD to 0.58%. Obviously, the forgetting factor can improve the system robustness against the measurement white noise.

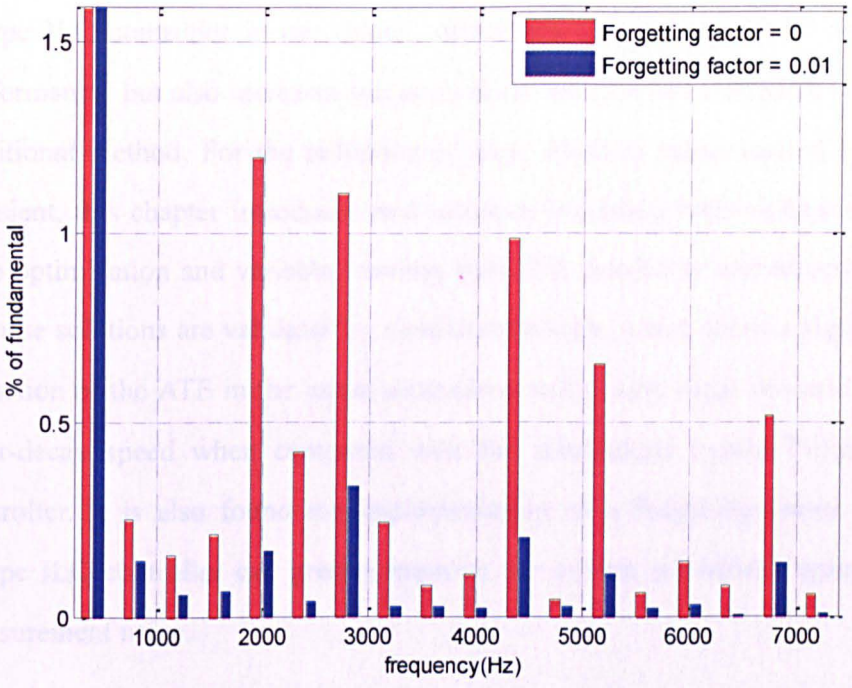


Figure 6. 21: Harmonic spectrum of the compensated supply current with SAF control system with and without forgetting factor presence of measurement noise

6.8 Conclusion

From a practical point view, this chapter modifies the SAF system introduced in the previous chapter. These modifications include the use of the demand supply current as the current reference and the implementation of the SAF control system in the α-β reference frame, which will allow reducing relevantly the impractical sampling and switching frequencies used in previous chapter still maintaining an accurate current tracking.

As mentioned in Chapter 5, the dynamic performance to load transients, the error-decay speed and the robustness against disturbances of the SAF control system requires further improvement. Hence, specific optimization to the SAF control system used in this chapter is conducted. For the improvement of the

system dynamic performance to the load transient, a novel design of hybrid P-type ILC controller is introduced, which not only improves the dynamic performance, but also increases the error-decay speed when compared with the traditional method. For the reduction of large tracking errors caused by load transient, this chapter introduces two solutions including both voltage control loop optimization and variable learning gain. The feasibility and effectiveness of these solutions are validated by simulation results, which show a significant reduction of the ATE in the initial repetitions and a fairly large increase in the error-decay speed when compared with the stand-alone hybrid P-type ILC controller. It is also found the implementation of a forgetting factor in the P-type ILC controller can greatly improve the system robustness against the measurement noise.

Finally the optimized SAF control system can provide a very accurate current tracking while compensating the current harmonics. More importantly, the proposed optimized methods are capable to improve the system performance including dynamic response, the error-decay speed and the robustness. All of the above conclusions were taken testing the improved SAF control facing a more realistic load, constituted by a diodes rectifier supplying a resistive load. However, these investigations are limited to a power system with a fixed supply frequency only. The feasibility and suitability of such SAF system's application in a variable fundamental frequency power network will be investigated in the next chapter.

Chapter 7 Hybrid P-type ILC controller applied in a variable supply frequency SAF (VSFSAF) system

7.1 Introduction

As mentioned in Chapter 1, one of the major objectives of this project is to design a SAF system for the current harmonic cancellation in an aircraft VFG system, where the supply frequency varies linearly between 400Hz to 800Hz. Such supply frequency variation will cause variation of the power system harmonic frequencies. In the worst case scenario of supply frequency at 800Hz, 5^{th} and 7^{th} harmonics get to 4Khz and 5.6KHz respectively, drastically increasing the control difficulty for the SAF system requiring very large bandwidth control. The literature review in Chapter 2 shows the inadequacy of traditional current control strategies under such circumstance.

The analysis and investigation in Chapter 6 shows the outstanding performance and high robustness of the optimized hybrid P-type ILC controlled SAF system in the case of fixed supply frequency at 400Hz. The aim of this chapter is to extend and adopt the control strategy developed for the SAF operating at fixed supply frequency to the case of variable frequency supply system for variable frequency harmonic currents compensation. The studies of this chapter will also investigate the capability of the variable supply frequency SAF (VSFSAF) system to achieve accurate current tracking as in the fixed frequency case. The key issues of such VSFSAF application can be summarized as: 1) maintaining an integer number of samples in each ILC repetition; 2) applying the ILC

principles despite possible changes in supply frequency at each repetition; 3) efficiently cancelling the current harmonics with a bounded sampling and switching frequency. In order to do so, two algorithms are introduced for the VSFSAF control in the first part of this chapter. The corresponding modifications and optimizations in the current control loop of the hybrid P-type ILC controller will be presented in the second part of this chapter, followed by the system stability analysis of both current and voltage control loops. To verify the validity and effectiveness of the proposed VSFSAF system, simulation results with analysis will be demonstrated.

7.2 VSFSAF system model

As discussed in Chapter 5, the P-type ILC controller requires an integer and constant number of samples in each reference repetition to maintain its function. [68] However, in a VSFSAF application the supply frequency various meaning that, a fixed sampling frequency cannot provide an integer constant number of samples in the current repetition. The simplest solution to this problem is to use a variable sampling and switching frequency proportional to the supply frequency.

However, if this route is chosen, the upper limit of the switching frequency imposed by the power converter used needs to be considered. In fact, by using a fixed number of samples per cycle proportionally varying sampling and switching frequency, it must be checked that the upper bound is not exceeded when the supply frequency reaches its peak value. In this application the upper bound of the supply frequency is fixed to 800Hz, and the one for the switching frequency is fixed to 16000Hz which is a reasonable value given the IGBT components used and the power rating of the considered system. By using a fixed number of samples per cycle (N), the value of N should be equal to 20,

which means the switching frequency should be 8000Hz for a 400Hz supply frequency. As a result, the Nyquist frequency is only 4000Hz when the supply frequency is 400Hz, hence at most the current control loop can only compensate the harmonic components at frequencies lower than 4000Hz (i.e. 3^{rd}, 5^{th}, 7^{th} and 9^{th} harmonics). To have a larger control bandwidth at lower supply frequency, the solution is to use a variable number of samples per cycle (N). By doing so, the sampling frequency can vary linearly at steps and oscillates around a fixed average value, while N decreases as the supply frequency increase. Thus the current control loop will still be able to compensate only up to the 9^{th} harmonic at 800Hz (supply frequency), but the control bandwidth increase as the supply frequency decreases reaching its maximum at 400Hz, which is leading to a more efficient harmonic control throughout the supply frequency variability range. This concept will be better explained in Section 7.2.1.

Figure 7.1 shows the block scheme of the VSFSAF control system with variable sampling and switching frequency and thus variable number of samples per cycle. Two algorithms are needed to achieve this in the control system.

The upper algorithm takes the measured PCC phase voltage as its input signal, and according to its frequency, produces three output signals: the discrete components trigger signal, the PWM carrier signal and the demand number of samples per cycle (N). The discrete components trigger signal is used to control the period of the discrete control loop including the zero order holders (ZOHs), current and voltage control loops. The PWM carrier signal is fed to the PWM to control its switching frequency. Thus, by varying the period of the trigger and carrier signal, a variable sampling and switching frequency can be obtained. In addition, the number of samples is fed to the hybrid P-type ILC

controllers to generate a corresponding discrete delays for the error and control signal.

For the current control loop, the measured PCC voltage is firstly passed through a PLL based algorithm, to determine a sinusoidal three-phase template with a fixed frequency in each repetition, which is then multiplied by the sum of the demand supply current amplitude and the demand current amplitude of voltage control loop to generate the current reference. Thus, with a certain sampling frequency, a current reference with integer number of samples per cycle can be provided for the current control loop hybrid P-type ILC controllers.

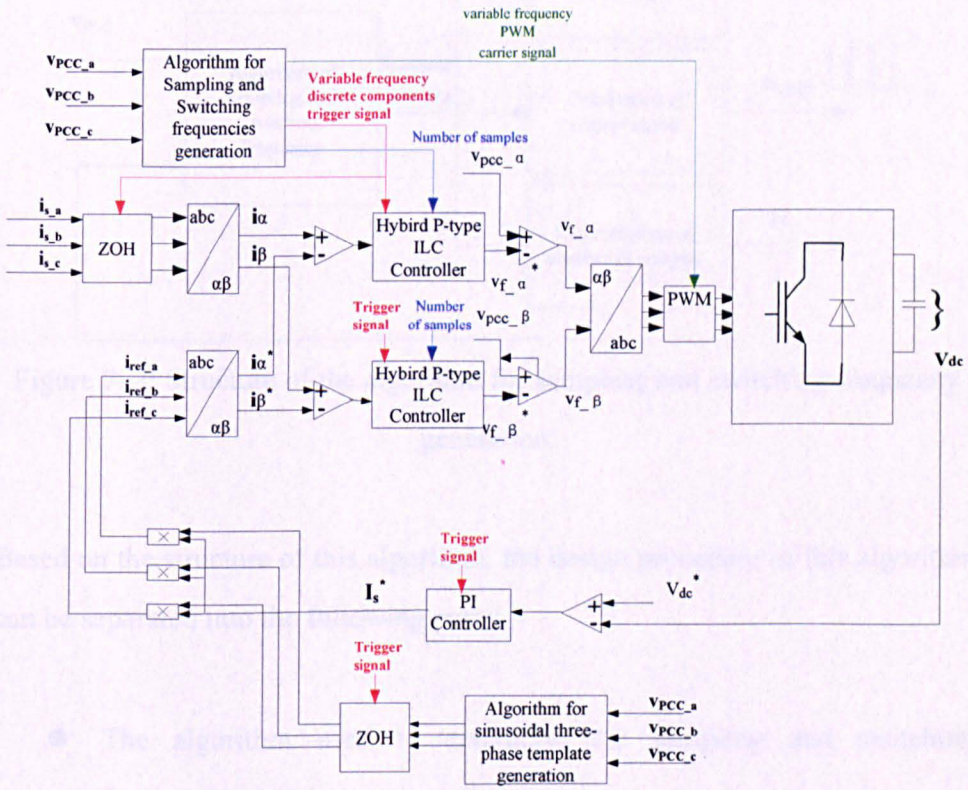


Figure 7. 1: Proposed SAF control system with variable fundamental frequency

The design procedures of both sampling and switching frequency generation algorithm and sinusoidal three-phase template generation algorithm will be introduced in the following sections.

7.2.1 Algorithm for variable sampling and switching frequency and variable number of sample generation

The basic structure of this algorithm is shown in fig.7.2, where it uses the measured PCC phase voltage ($v_{pcc\_a.}$ $v_{pcc\_b.}$ $v_{pcc\_c.}$) and the feedback demand number of samples per cycle (N) to calculate the sampling and switching frequency ($f_{sampling}$ & $f_{switching}$). Then the corresponding waveforms of the discrete components trigger ($s_{trigger}$), PWM carrier signal ($s_{carrier}$) and the demand number of samples (N) can be determined.

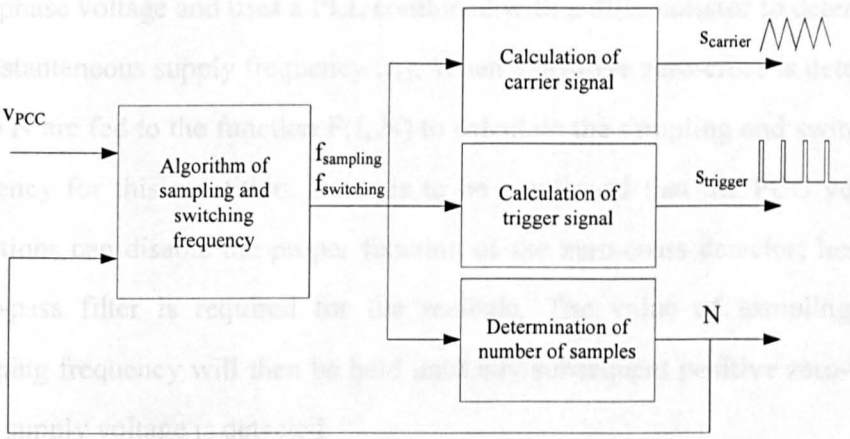


Figure 7. 2: Structure of the algorithm for sampling and switching frequency generation

Based on the structure of this algorithm, the design procedure of this algorithm can be separated into the following parts:

- The algorithm used to determine the sampling and switching frequency;
- The determination of the number of samples per cycle keeping into account of the switching frequency limitation;
- The determination of the waveforms of both the trigger and carrier signal.

7.2.1.1 Determination of the sampling and switching frequency

The method used to determine the sampling and switching frequency to provide an integer value of N in each repetition can be explained as follows. Since the supply frequency can be constantly varied, the method calculates a suitable sampling and switching frequency at the beginning of each cycle to provide an integer number of samples only once for each repetition. Figure 7.3 presents the concept of this step varying sampling and switching frequency generation. This method continuously detects the positive zero-cross of the PCC phase voltage and uses a PLL combined with a differentiator to determine the instantaneous supply frequency (f_s). When a positive zero-cross is detected, f_s and N are fed to the function $F(f_s,N)$ to calculate the sampling and switching frequency for this repetition. It needs to be mentioned that the PCC voltage distortions can disable the proper function of the zero-cross detector; hence a lower-pass filter is required for the realistic. The value of sampling and switching frequency will then be held until any subsequent positive zero-cross in the supply voltage is detected.

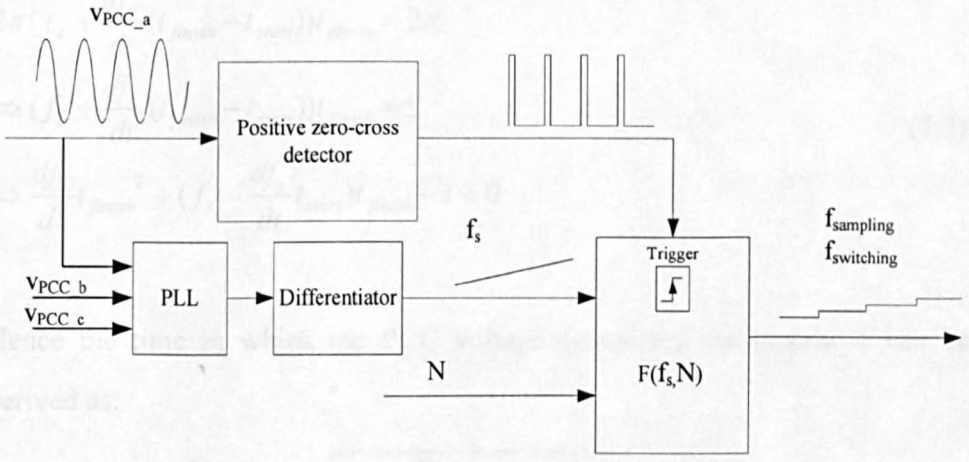


Figure 7. 3: Block diagram of the sampling and switching frequency generation algorithm

The function $F(f_s,N)$ predicts the period of the current repetition at the beginning of this repetition. Given the repetition period and the demand N, the corresponding sampling and switching frequency can be determined. Supposing the supply frequency varies linearly with time, considering the instantaneous supply frequency at the beginning of the proposed repetition (t_{start}) as f_s, the waveform of the PCC voltage can be written as,

$$v_{PCC\_a} = V_{PCC} \sin(2\pi(f_s + \frac{df_s}{dt}(t - t_{start}))t) \tag{7.1}$$

Supposing the PCC voltage completes the cycle at t_{finish}, eq.(7.1) can be rewritten as follows,

$$v_{PCC\_a} = V_{PCC} \sin(2\pi(f_s + \frac{df_s}{dt}(t_{finish} - t_{start}))t_{finish}) = 0 \tag{7.2}$$

Since the interval from t_{start} to t_{finsih} can be considered as the full cycle of the PCC voltage, the eq.(7.2) becomes:

$$\begin{aligned} & 2\pi(f_s + \frac{df_s}{dt}(t_{finish} - t_{start}))t_{finish} = 2\pi \\ \Rightarrow & (f_s + \frac{df_s}{dt}(t_{finish} - t_{start}))t_{finish} = 1 \\ \Rightarrow & \frac{df_s}{dt} t_{finish}^{\ 2} + (f_s - \frac{df_s}{dt} t_{start}) t_{finish} - 1 = 0 \end{aligned} \tag{7.3}$$

Hence the time in which the PCC voltage completes the repetition can be derived as:

$$t_{finish} = \frac{-(f_s - \frac{df_s}{dt} t_{start}) + \sqrt{(f_s - \frac{df_s}{dt} t_{start})^2 + 4 \cdot \frac{df_s}{dt}}}{2\frac{df_s}{dt}} \tag{7.4}$$

Therefore, the period (T) of the repetition can be determined by the following equation,

$$T = t_{finish} - t_{start} = \frac{-(f_s - \frac{df_s}{dt} t_{start}) + \sqrt{(f_s - \frac{df_s}{dt} t_{start})^2 + 4 \cdot \frac{df_s}{dt}}}{2\frac{df_s}{dt}} - t_{start} \qquad (7.5)$$

Given the demand number of samples per cycle (N) in the repetition, the sampling and switching frequency can be determined as,

$$f_{sampling} = f_{switching} = N(\frac{1}{T}) \qquad (7.6)$$

7.2.1.2 Determination of the number of samples per cycle (N)

As discussed in Section 7.2, due to the limitation of the switching frequency, a variable number of samples per cycle can lead to the use of a higher sampling frequency than in the fixed one, during the supply frequency variation. Thus the current control loop can compensate harmonic components up to a higher frequency when the supply frequency is low.

The determination method of the number of samples per cycle in each repetition can be graphically explained by fig.7.4. Assuming the supply frequency linearly increases from 400Hz and the initial number of samples (N) is 34, by using a step varying sampling and switching frequency as shown in Section 7.2.1.1, the switching frequency will increase with the supply frequency. Starting from a fixed switching frequency $f_{switching}$=14.4Khz, when the switching frequency excesses its upper limit of 16KHz, the number of samples per cycle (N) will be reduced to 32, and hence the sampling and switching frequency is reduced instantly. N will be maintained at 32 until the

switching frequency exceed its upper limit again. This procedure will be repeated until the supply frequency stops varying. It needs to be mentioned that, in fig 7.4 the lower limit of the $f_{switching}$ is indicated as constant for simplicity. In reality (fig. 7.15) it varies according with N and f_s, since the sampling frequency should equal to the number of sample times the supply frequency. The Matlab code written to implement this method is presented in Appendix C.

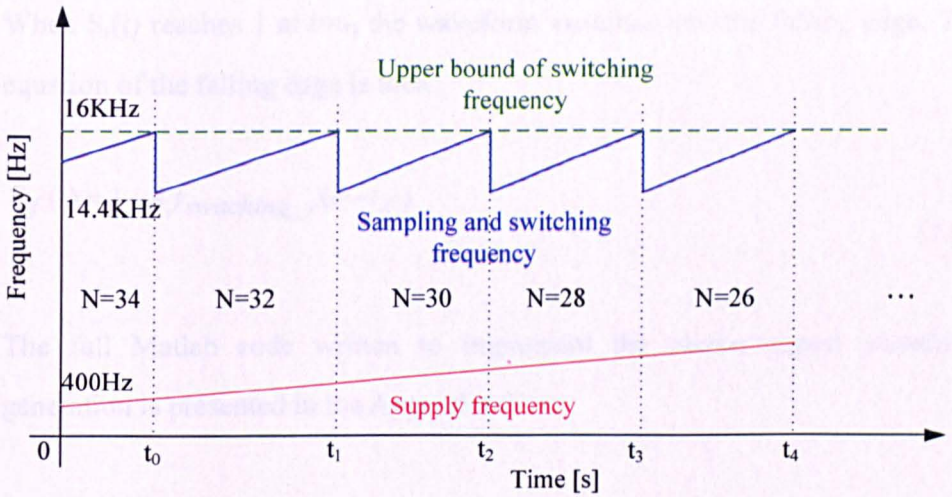


Figure 7. 4: Concept of variable number of samples per cycle.

7.2.1.3 Generation of the discrete components trigger and PWM carrier signal

Given the sampling and switching frequency in a repetition, the waveforms of the discrete components trigger signal and PWM carrier signals of the VSFSAF control can be determined. The discrete component trigger signal is a pulse wave with a period of $1/f_{sampling}$. This pulse wave can be produced by detecting the positive zero-crossing of a sinusoidal signal with a frequency equals to the demand sampling frequency.

The carrier signal for the PWM modulator is a unit triangle wave with a period

of 1/ $f_{switching}$. By defining the rising and falling edge of the triangle wave as S_r and S_f, and by assuming the carrier signal starts with the rising edge at t_r, where $S_r(t_r)$=-1, since the slope of the rising edge is $4f_{swiching}$, the equation of S_r versus time is:

$$S_r(t) = -1 + 4f_{switching\_i}(t - t_r) \tag{7.7}$$

When $S_r(t)$ reaches 1 at t=t_f, the waveform switches into the falling edge. The equation of the falling edge is then,

$$S_f(t) = 1 - 4f_{switching\_i}(t - t_f) \tag{7.8}$$

The full Matlab code written to implement the carrier signal waveform generation is presented in the Appendix C.

7.2.2 Algorithm for sinusoidal template generation

As discussed in Section 7.2, the VSFSAF control loop uses a PLL based algorithm to generate a three-phase sinusoidal template. This sinusoidal template is multiplied by the sum of the demand supply current amplitude and the demand current amplitude produced by the voltage control loop, which acts as the reference of the current control loop. This section will introduce the algorithm of generating this sinusoidal template, followed by the optimization of this algorithm with the more practical considerations.

7.2.2.1 The standard algorithm

The analysis in Chapter 6 shows that the sinusoidal template should be

synchronous with the PCC voltage. Hence with a fixed supply frequency, it can be determined by using a standard PLL sinusoidal template generator. However, in a VSFSAF system, due to the supply frequency variation, the signal produced by the PLL sinusoidal template generator is a chirp signal. Taking the samples of this chirp template signal with a certain sampling frequency (presented in section 7.3.1), a current reference variation between the corresponding time step in the nearby repetitions can appear. Although the optimized hybrid P-type ILC controller can provide a highly robust performance against such variation, the avoidance of reference variation is still a primary consideration in P-type ILC application.

In order to produce a sinusoidal template instead of a chirp one, the algorithm uses a same method as introduced in Section 7.2.1.1, to predict the period (T) of the PCC voltage (eq. (7.5)). As shown in fig.7.5, the sinusoidal template determined by this algorithm is synchronous with the phase PCC voltage.

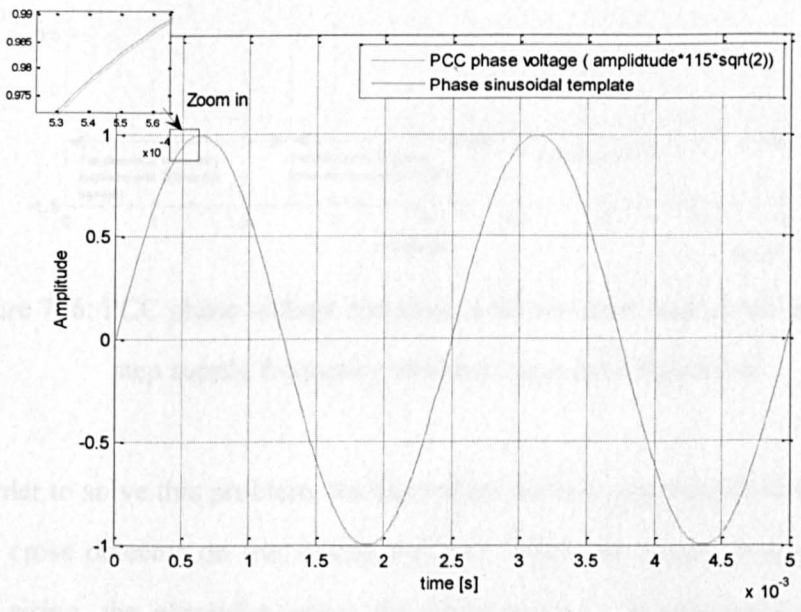


Figure 7. 5 Comparison between the sinusoidal template and the PCC phase voltage

7.2.2.2 Algorithm improvement

Practically, the supply frequency depends on the rotation speed of the generators driven by the aircraft engines, meaning that a non-linear supply frequency variation is possible. As discussed, the algorithm for sinusoidal template generation is based on a prediction of the PCC voltage period. Therefore, a permanent phase shift between the generated sinusoidal template and the PCC voltage will appear when there is a mismatch between the actual and predict period of the PCC voltage. Simulation results in fig.7.6 shows such phase shift in the case of a frequency step change.

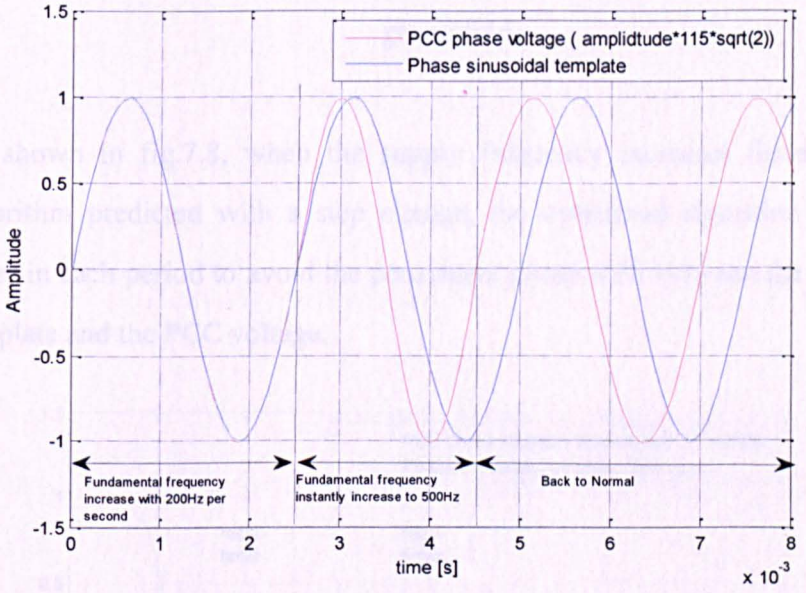


Figure 7. 6: PCC phase voltage and sinusoidal template with an un-predictable step supply frequency variation (standard algorithm)

In order to solve this problem, the algorithm has been augmented using a rising zero cross detector on the supply voltage. When the supply voltage crosses zero rising, the algorithm resets the timer to zero. As discussed in Section 7.2.1.1, the zero cross detector in this application is very sensitive to the PCC voltage distortion, a low-pass filter is required in the real application. Thus the

permanent phase shift can be avoided. The block diagram of this algorithm is drawn in fig.7.7.

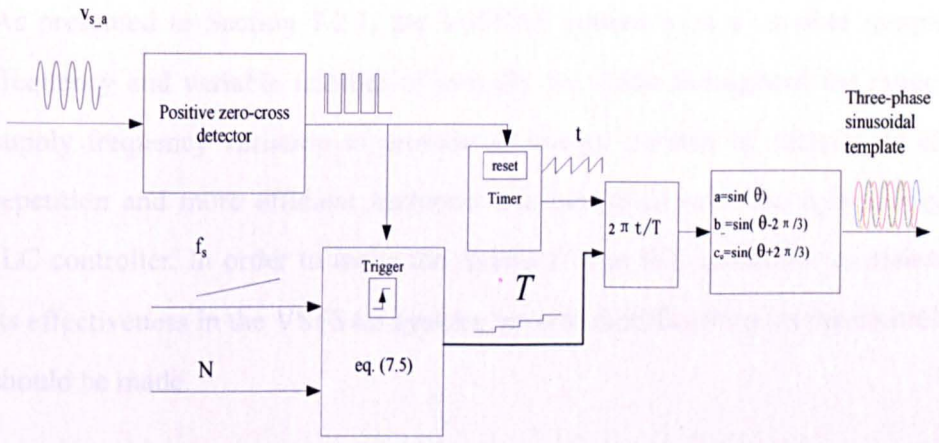


Figure 7. 7: Block diagram of the algorithm for the sinusoidal template generation

As shown in fig.7.8, when the supply frequency increases faster than the algorithm predicted with a step change, the optimized algorithm resets the timer in each period to avoid the permanent phase shift between the sinusoidal template and the PCC voltage.

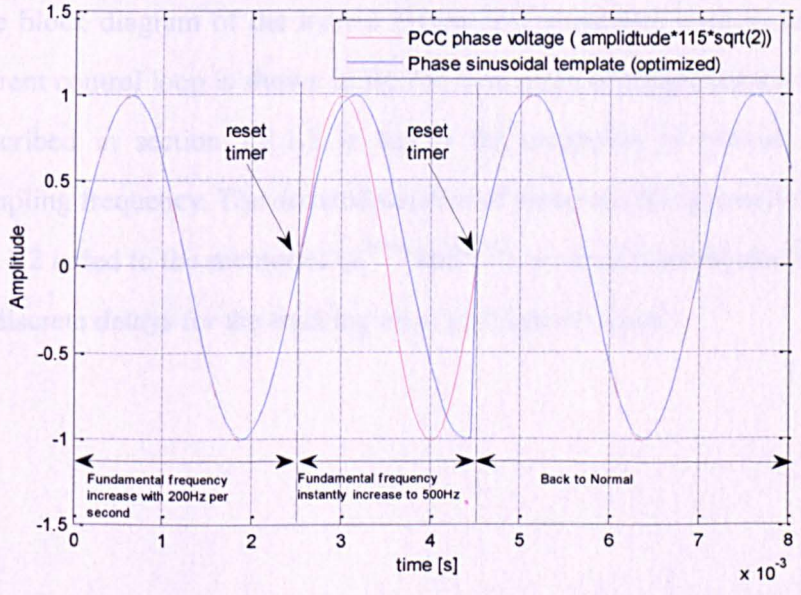


Figure 7. 8: PCC phase voltage and sinusoidal template with an un-predictable step supply frequency variation (optimized algorithm)

7.3 VSFSAF control loop design

As presented in Section 7.2.1, the VSFSAF system uses a variable sampling frequency and variable number of samples per cycle throughout the range of supply frequency variation to provide an integer number of samples in each repetition and more efficient harmonic compensation with the hybrid P-type ILC controller. In order to make the hybrid P-type ILC controller to maintain its effectiveness in the VSFSAF system, several modifications on the controller should be made.

In addition, since the hybrid P-type ILC control in the current control loop and the PI controller in the voltage control loop should operate with a variable sampling frequency, the stability of these controllers within the variation range of sampling frequency has to be investigated.

7.3.1 Modifications of the hybrid P-type ILC controller

The block diagram of the hybrid P-type ILC controller used in the VSFSAF current control loop is shown in fig.7.9. The discrete components trigger signal described in section 7.2.1.3 is fed to the controller to provide a variable sampling frequency. The demand number of samples (N) determined in section 7.2.1.2 is fed to the memories (z^{-N+m} and z^{-N}), to determine the demand number of discrete delays for the tracking error and control signal.

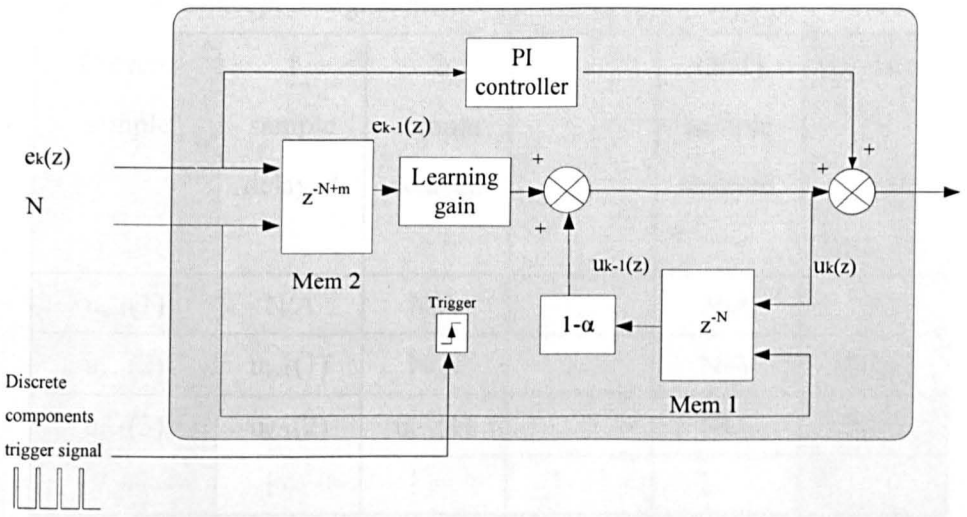


Figure 7. 9: Block diagram of the hybrid P-type ILC controller for VSFSAF

It is clear in fig.7.9 that the variable number of samples leads to a variable number of discrete delays for the memories (Mem1 and Mem2). A specifically developed software control routine will be used to delay the error and control signal of the demand sampling periods according with the current value of N.

Let's consider the generation of the discrete delay z^{-N} (for Mem 1) as an example. At the beginning of each sampling period, the routine not only updates the last sample of the control loop of the signal $u_{k-1}(z)$, but also takes a new sample from the control signal $u_k(z)$. The sequence of the stored N samples for the whole cycle ($u_{k-1}(z)$) is then updated at every sample time as shown in tab.7.1. Thus the sample updated to the control loop for each time is delayed for N sampling periods, which is a full repetition as requested.

Table 7. 1: Concept of signal memory in the hybrid P-type ILC controller

Current sample	1 sample delayed	2 sample delayed	…	(N-1) sample delayed	Updates (N sample delayed)
$u_{k-1}(1)$	N/A	N/A	…	N/A	N/A
$u_{k-1}(2)$	$u_{k-1}(1)$	N/A	…	N/A	N/A
$u_{k-1}(3)$	$u_{k-1}(2)$	$u_{k-1}(1)$	…	N/A	N/A
⋮	⋮	⋮	⋮	⋮	⋮
$u_{k-1}(N)$	$u_{k-1}(N-1)$	$u_{k-1}(N-2)$	…	$u_{k-1}(1)$	N/A
$u_k(1)$	$u_{k-1}(N-1)$	$u_{k-1}(N-2)$	…	$u_{k-1}(2)$	$u_{k-1}(1)$
$u_k(2)$	$u_{k-1}(N)$	$u_{k-1}(N-1)$	…	$u_{k-1}(3)$	$u_{k-1}(2)$

However, in the case that the number of samples per cycle N changes, the previously stored samples in the routine presented above will not match the new requirement, saying N_1 value in the current repetition. Due to this problem, the routine uses a linear interpolation to convert the stored N samples into N_1 samples, when a variation of the number of samples per cycle is detected. This linear interpolation function is implemented as follows.[86]

Figure.7.10 shows that the i^{th} time step in the scale of N_1 samples can be approximately regarded as x_i^{th} time step in the scale of N samples, by using the function shown below:

$$x_i = i\frac{N}{N_1} \qquad 1 \le i \le N_1 \tag{7.9}$$

As in general x_i is not integer, the two adjacent integer time steps in the scale of N samples, name x_a and x_b, can be determined by using the function named 'fix'

in the Matlab software, as shown below:

$$x_a = fix(x_i)$$
$$x_b = fix(x_i) + 1 \tag{7.10}$$

The corresponding sample values at time steps x_a and x_b are defined as y_a and y_b. As shown in fig.7.10, the point (x_i, y_i) representing the sampling value (y_i) at i^{th} time step in a scale of N_1 samples, can be considered as an interpretation point on the linear line between points (x_a, y_a) and (x_b, y_b),. Therefore, the sampling value (y_i) can be determined by following equation,

$$y_i = y_a + (x_i - x_a)\frac{(y_b - y_a)}{(x_b - x_a)} \tag{7.11}$$

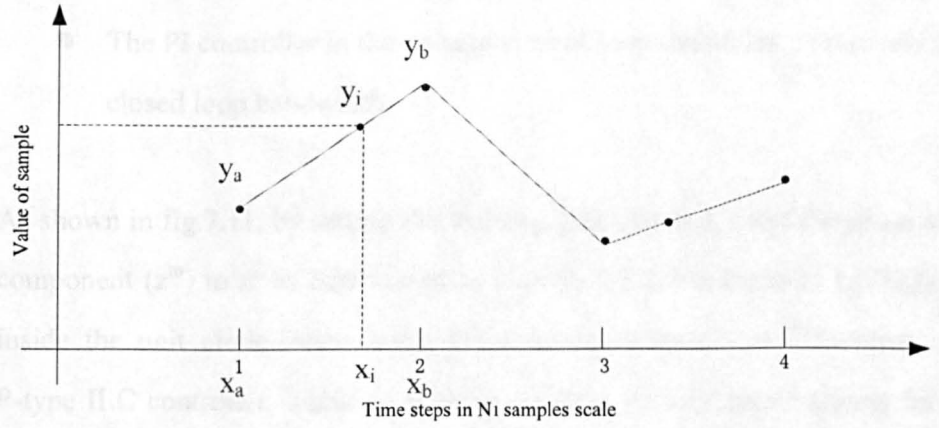


Figure 7. 10: Concept of the linear interpolation method

The full routine codes for this implementation within the hybrid P-type ILC controller, which includes the linear interpolation function is presented in Appendix C.

7.3.2 System stability analysis under a variable sampling frequency

In this application, the upper limit of the sampling frequency is set to be 16000Hz with a starting point of 14400Hz for the 400Hz supply frequency. In accordance with the algorithm presented in Section 7.2.1.2, the sampling frequency can vary from 14400Hz to 16000Hz. Therefore, it is worthwhile to investigate stability issues of the hybrid P-type ILC based the current control loop and the PI based voltage control loop designed in Chapter 6, under such sampling frequency variation. The stability analysis consists in the following checks:

- The P-type ILC controller inside the hybrid P-type ILC controller satisfy the error-decay condition;
- The PI controller in the voltage control loop maintains a relatively low closed loop bandwidth.

As shown in fig.7.11, by setting the learning gain (L) to 3.2 and the phase shift component (z^m) to z^2 as determined in Section 6.3.2, the locus of $Lz^mG_p(z)$ is inside the unit circle determining the error-decay condition. Therefore, the P-type ILC controller is able to provide an accurate reference tracking for all frequency components (from zero to Nyquist frequency), during the sampling frequency variation.

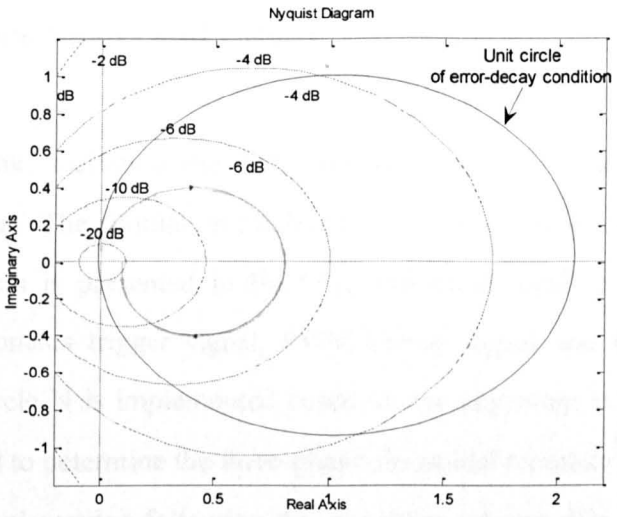


Figure 7. 11: Nyquist diagram of $3.2z^2G_p(z)$ used to verify the error-decay condition (sampling frequency varying from 14400Hz to 16000Hz)

In accordance with the voltage PI controller determined in the Chapter 6, i.e., $P_{voltage\_control}(z) = \frac{0.716(z-0.998)}{z-1}$, the maximum closed loop bandwidth voltage control while the sampling frequency varies should be 30Hz, which is sufficient for the PI controller to maintain its function in the voltage control loop. The corresponding closed-loop bode diagram for the PI controller is shown in fig.7.12, exhibiting a negligible variation with sampling freuqnecy.

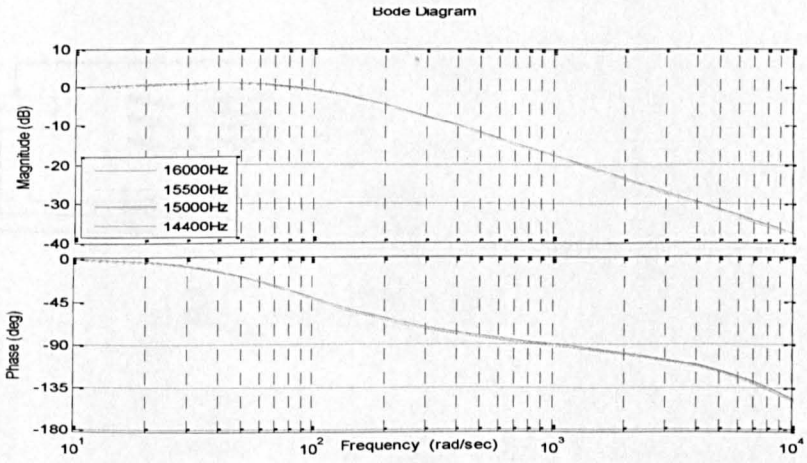


Figure 7. 12: Closed-loop bode diagram of the PI controller in the voltage control loop (sampling frequency varying from 16000Hz to 18000Hz)

7.4 Simulation model and results

Matlab/Simulink, including the Simpower Blockset, is used to model the VSFSAF system. The simulation model of the overall power network with the VSFSAF system is presented in fig.7.13. The block used to determine the discrete components trigger signal, PWM carrier signal and the number of samples per cycle N is implemented based on the algorithm in Section 7.2.1. The block used to determine the three-phase sinusoidal template for the current reference is implemented following the algorithm presented in Section 7.2.2. The hybrid P-type ILC controller is modified in accordance with the description in Section 7.3.1. Since the stability and feasibility of both current and voltage controllers have been verified, they are applied in this simulation model. The parameters of this simulation, including the line inductance, load inductance and resistance, VSFSAF inductance and resistance, the DC link capacitance and etc, maintain the same values as shown in Chapter 6.

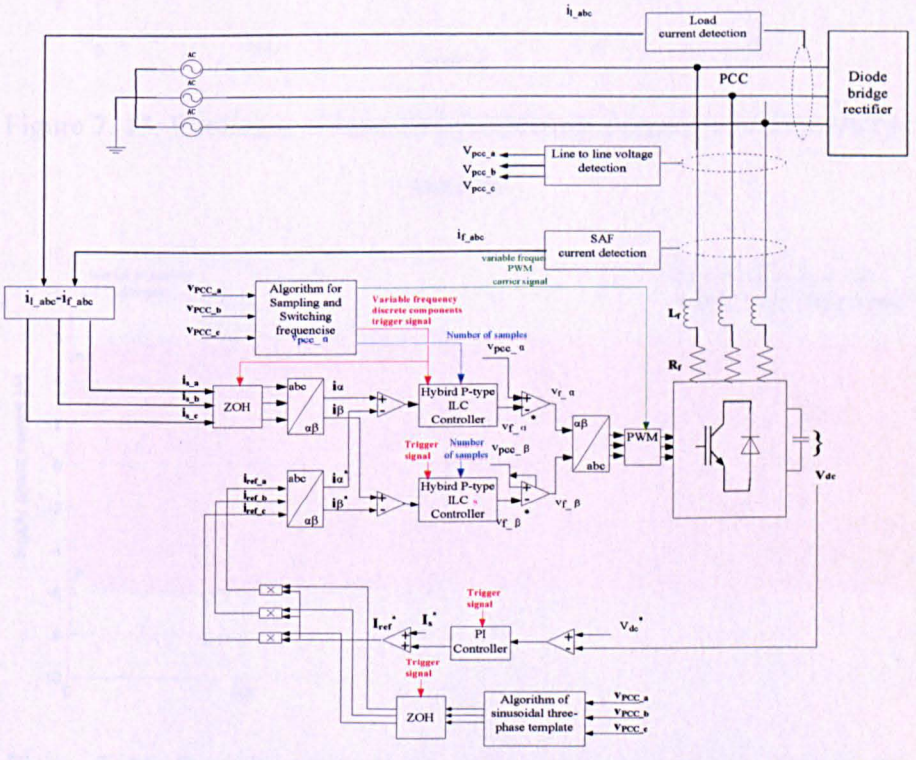


Figure 7. 13: Simulation model of the VSFSAF system

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shows the overall current reference tracking of the VSFSAF system. Considering the waveform of the number of samples shown in fig. 7.15 against the current reference tracking performance shown in fig. 7.16, it can be noticed that a current transient appears at each point of number of samples variation. Figure 7.17 shows a zoom of one of those transient (N=36 to N=34). It can be observed that the hybrid P-type ILC controller requires a few repetitions to compensate the tracking errors caused by the variation of number of samples. After this short transient, the current tracking provides an excellent harmonic compensation.

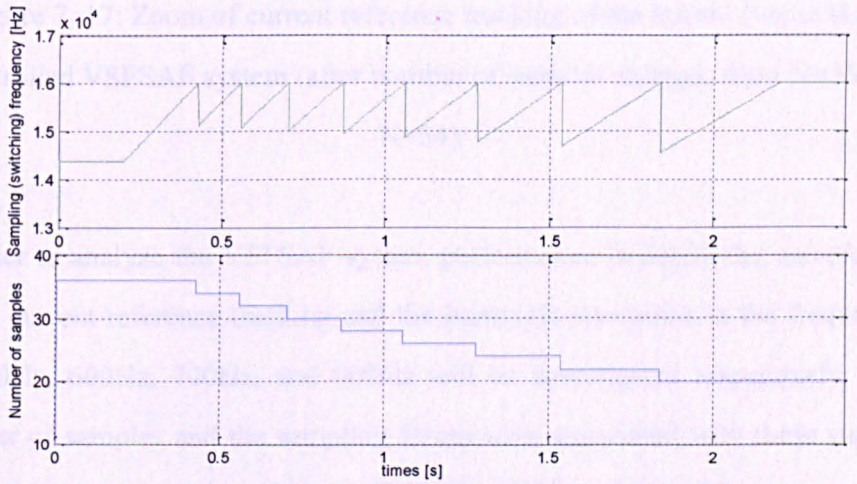

Figure 7. 15: Evolution of sampling (switching) frequency and number of samples

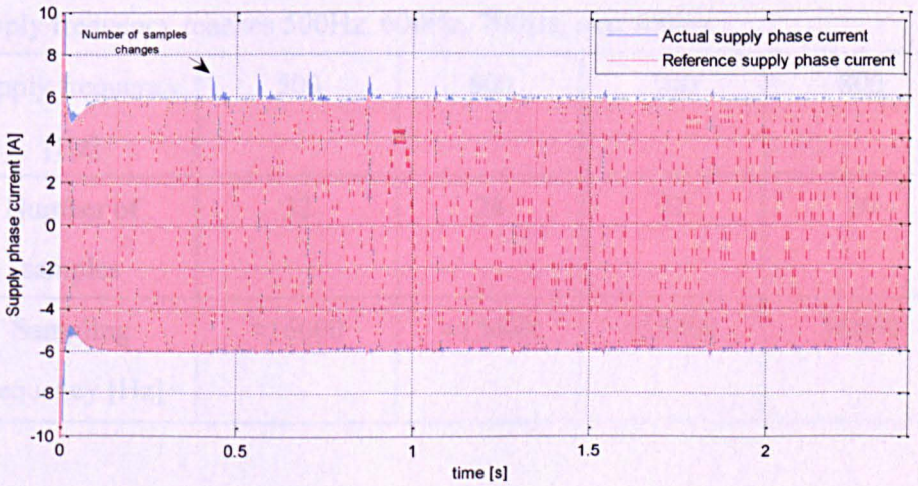

Figure 7. 16: Overall current reference tracking of the hybrid P-type ILC

controlled VSFSAF system

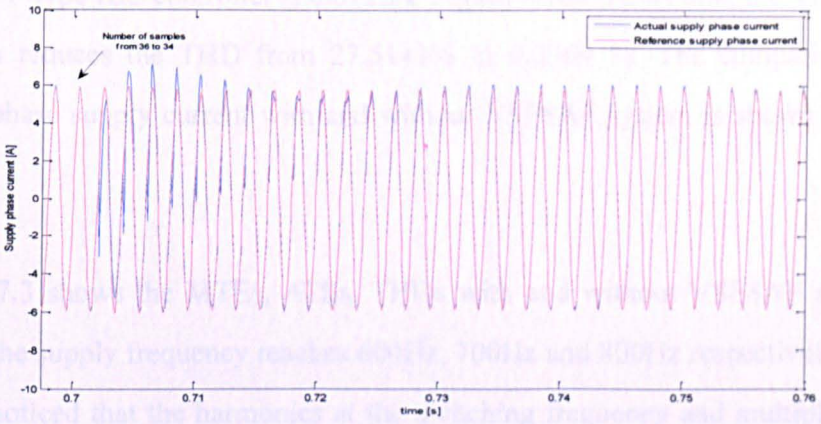

Figure 7. 17: Zoom of current reference tracking of the hybrid P-type ILC controlled VSFSAF system (after number of samples changes from N=36 to N=34)

In order to analyze the VSFSAF system performance in detail, the waveforms of the current reference tracking and the harmonic spectrums at the frequency of 500Hz, 600Hz, 700Hz, and 800Hz will be investigated respectively. The number of samples and the sampling frequencies associated with these supply frequencies are determined through fig.7.16 and shown in tab.7.2.

Table 7. 2: the time, number of samples and the sampling frequency when the supply frequency reaches 500Hz, 600Hz, 700Hz, and 800Hz

Supply frequency [Hz]	500	600	700	800
Number of samples	32	26	22	20
Sampling frequency [Hz]	≈16000	≈15600	≈15400	16000

As shown in fig.7.18a, the Maximum Tracking Error (MTE) is 0.0739A at the

supply frequency of 500Hz. Whereas the average tracking error (ATE) for the hybrid P-type ILC controller is 0.0122A. Figure 7.18b shows that, the VSFSAF system reduces the THD from 27.5141% to 0.2369 %. The comparison of three-phase supply current with and without VSFSAF system is shown in fig. 7.18c.

Table 7.3 shows the MTEs, ATEs, THDs with and without VSFSAF system when the supply frequency reaches 600Hz, 700Hz and 800Hz respectively. It is to be noticed that the harmonics at the switching frequency and multiples are not taken into account in the THD calculation as discussed in Section 6.7.3. The corresponding waveforms of the current reference tracking, the harmonic spectra and the waveforms of three-phase supply current are shown in fig.7.19 - 7.21 respectively. The simulations results verify the feasibility and suitability of the use of hybrid P-type ILC controllers in the VSFSAF current control loop. It is proved that the hybrid P-type ILC controller can provide an accurate reference tracking during the supply frequency variation.

Table 7. 3: Values of MTEs, ATEs and THDs at 600Hz, 700Hz, and 800Hz.

Supply frequency [Hz]	600	700	800
MTE [A]	0.0921	0.0831	0.1008
ATE [A]	0.0136	0.0105	0.0451
THD % (without VSFSAF)	28.9710	28.7525	30.7542
THD % (with VSFSAF)	0.3821	0.4783	0.5593

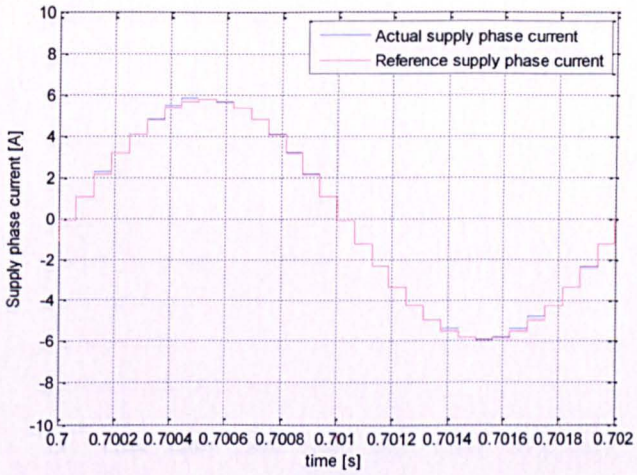

Figure 7. 18a: Current reference tracking of the VSFSAF current control loop (supply frequency 500Hz)

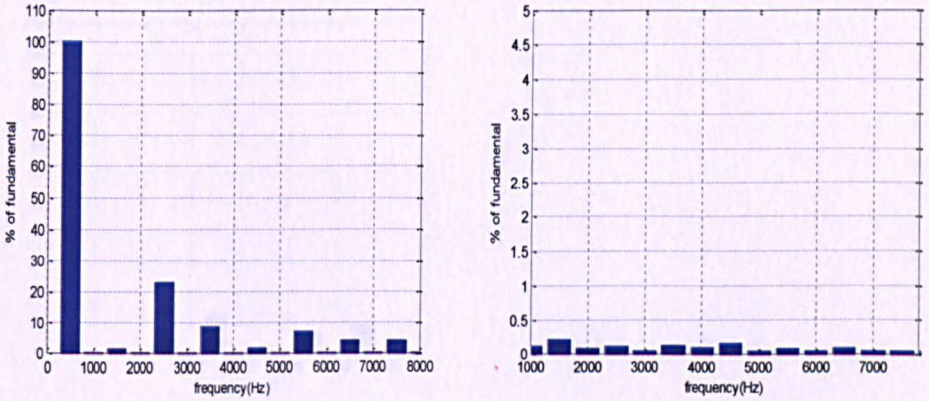

Figure 7.18b: Harmonic spectrums with and without VSFSAF system (supply frequency 500Hz)

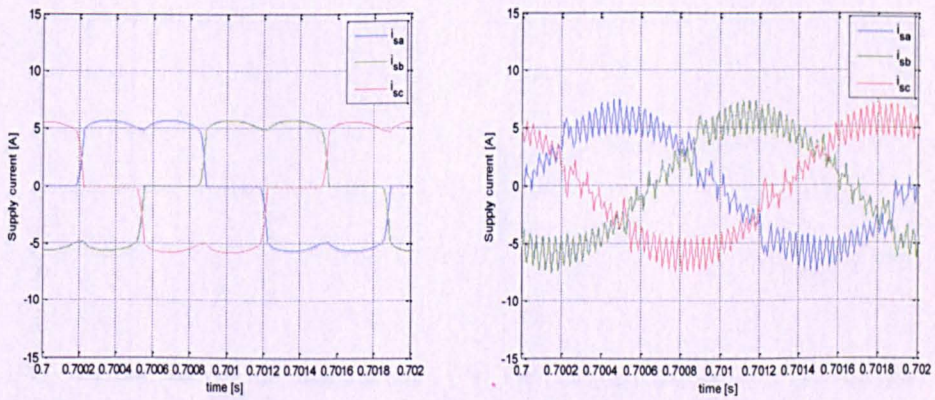

Figure 7.18c: Waveforms of three-phase supply current with and without VSFSAF system (supply frequency 500Hz)

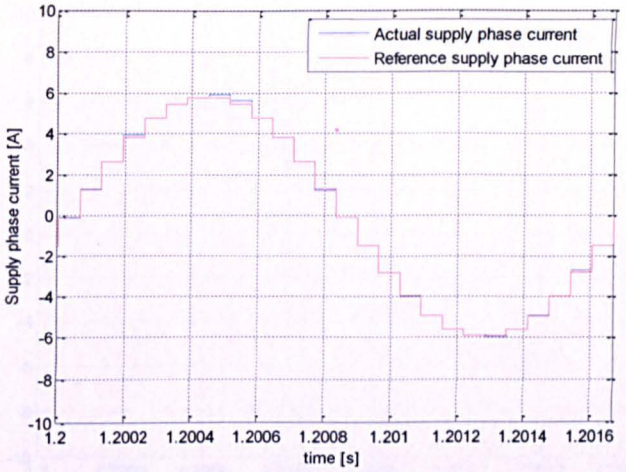

Figure 7. 19a: Current reference tracking of the VSFSAF current control loop (supply frequency 600Hz)

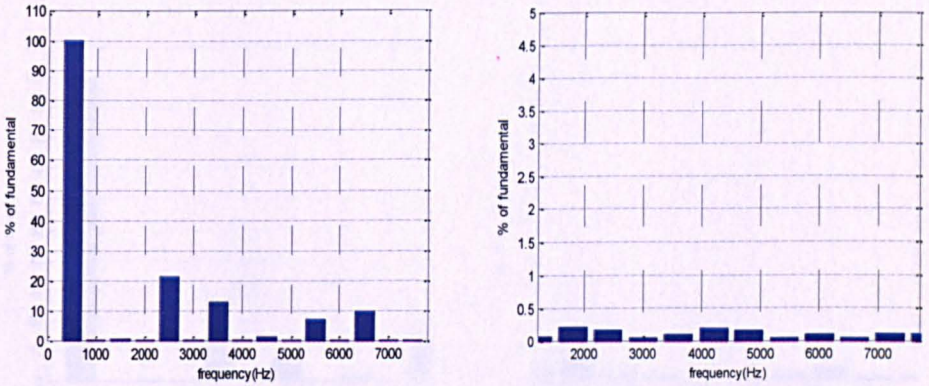

Figure 7.19b: Harmonic spectrums with and without VSFSAF system (supply frequency 600Hz)

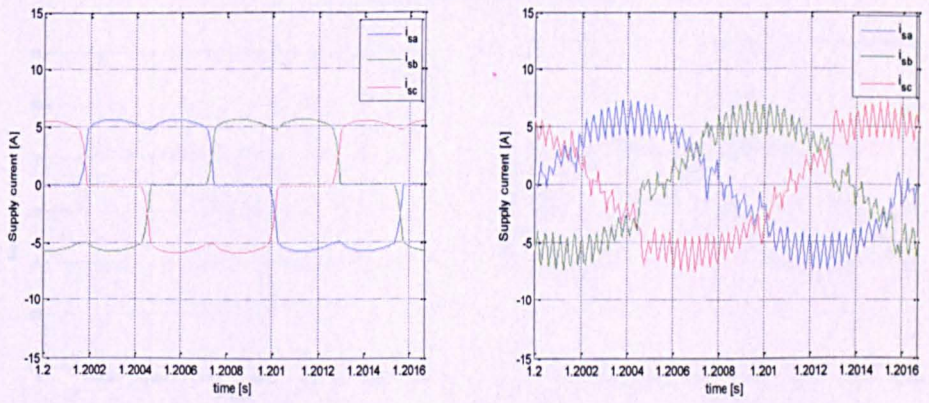

Figure 7.19c: Waveforms of three-phase supply current with and without VSFSAF system (supply frequency 600Hz)

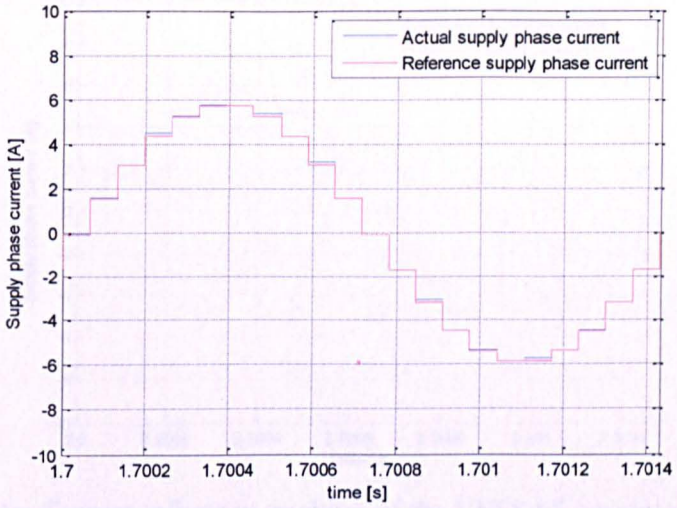

Figure 7. 20a: Current reference tracking of the VSFSAF current control loop (supply frequency 700Hz)

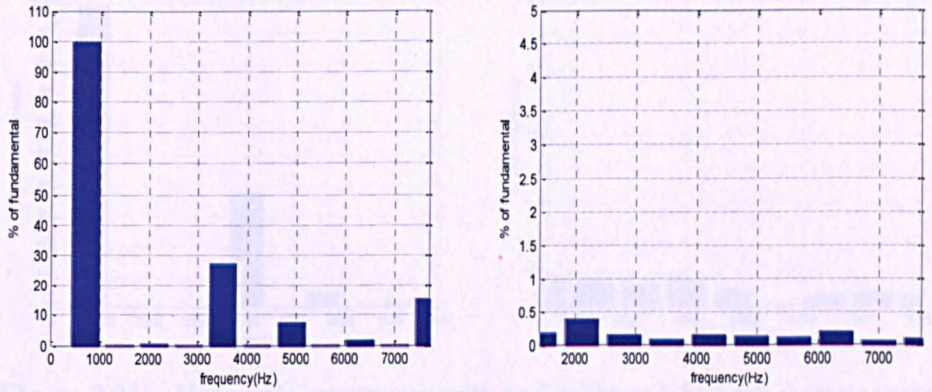

Figure 7.20b: Harmonic spectrums with and without VSFSAF system (supply frequency 700Hz)

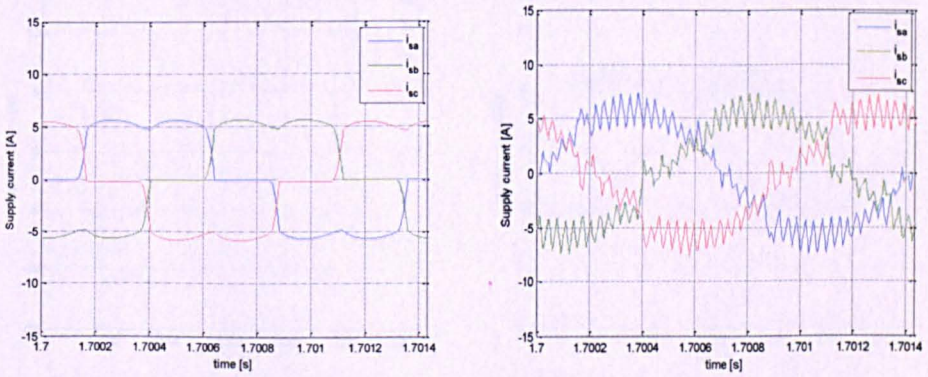

Figure 7.20c: Waveforms of three-phase supply current with and without VSFSAF system (supply frequency 700Hz)

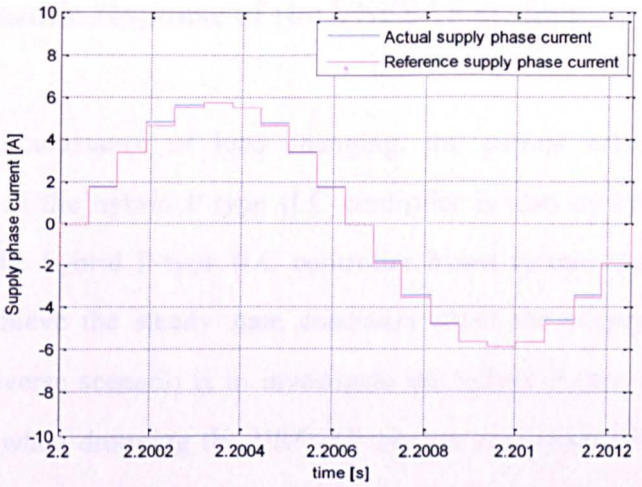

Figure 7. 21a: Current reference tracking of the VSFSAF current control loop (supply frequency 800Hz)

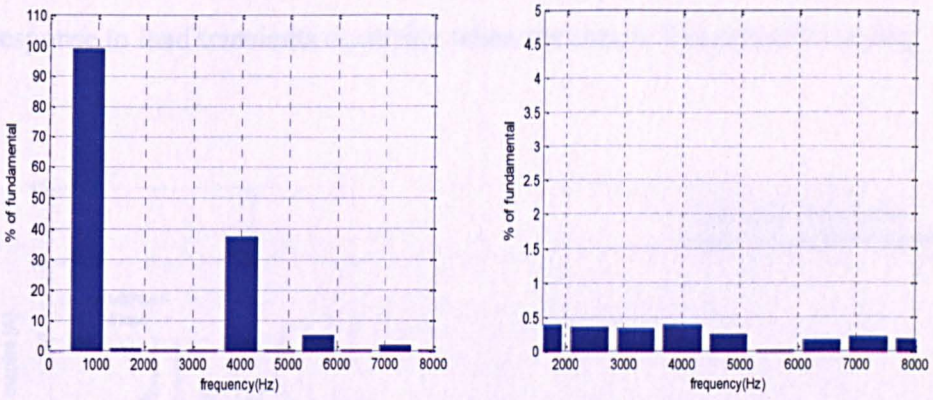

Figure 7.21b: Harmonic spectrums with and without VSFSAF system (supply frequency 800Hz)

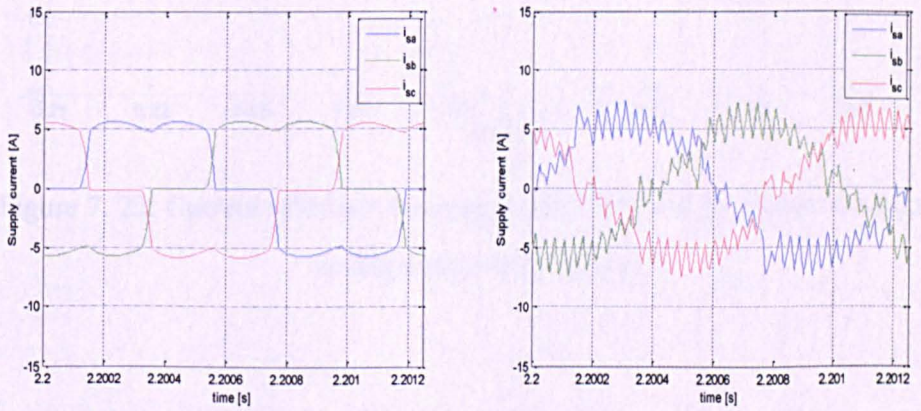

Figure 7.21c: Waveforms of three-phase supply current with and without VSFSAF system (supply frequency 800Hz)

7.4.2 Dynamic response of the VSFSAF system

Under the circumstance of load changing, the current reference tracking performance of the hybrid P-type ILC controller is also investigated. Figure 7.22 shows the hybrid P-type ILC controller based system takes about 0.05 second to achieve the steady state condition when the supply frequency is varying. A reverse scenario is to investigate the hybrid P-type ILC controller performance when dropping the VSFSAF system load from full to half load. Simulation results in fig.7.23 show that the controller takes about 0.04 second to achieve the steady state condition. There simulation results show that the hybrid P-type ILC controlled VSFSAF system can provide a decent dynamic response to load transients occurring when the supply frequency is varying.

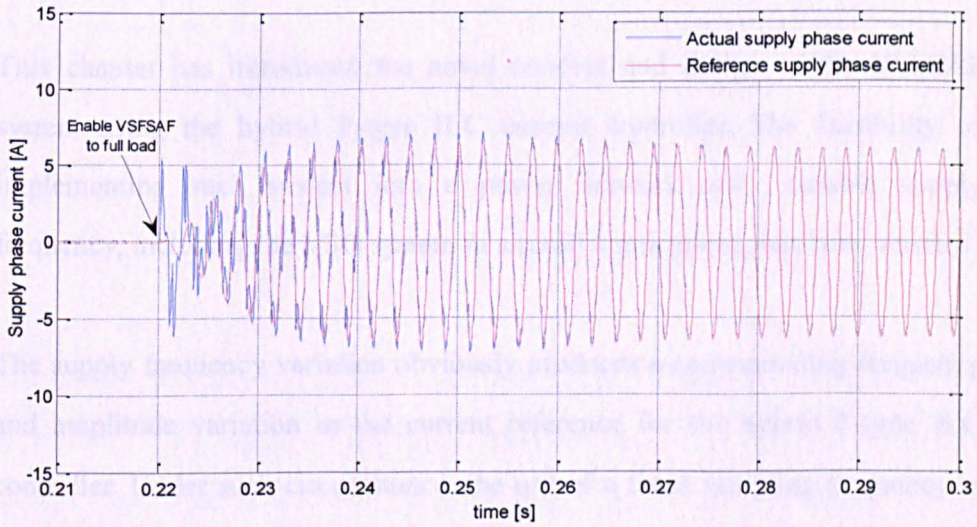

Figure 7. 22: Current reference tracking when the VSFSAF system is enabled to full load at 0.22 second

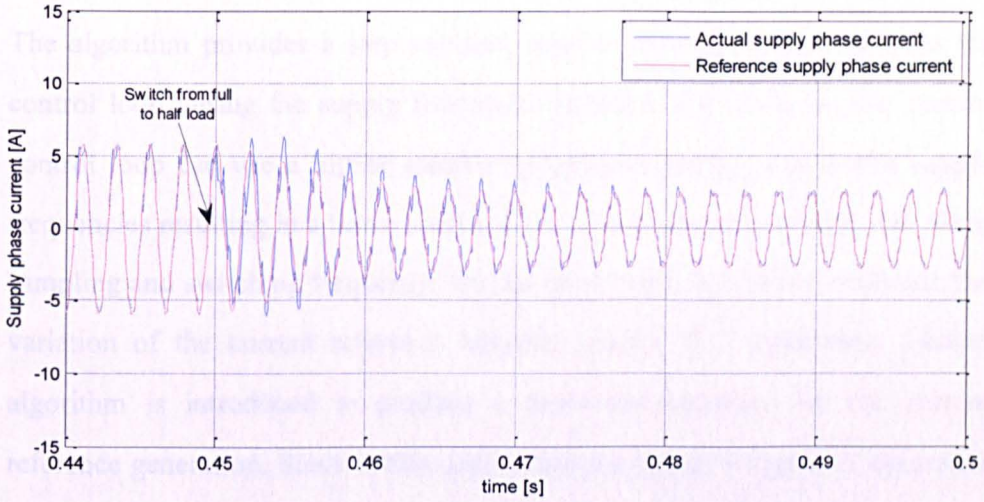

Figure 7. 23: Current reference tracking when the VSFSAF system switches from full to half load at 0.45 second

7.5 Conclusion

This chapter has introduced the novel concept and design of the VSFSAF system using the hybrid P-type ILC current controller. The feasibility of implementing such system into a power network with variable supply frequency, including the VSG system in aircraft applications, has been verified.

The supply frequency variation obviously produces a corresponding frequency and amplitude variation in the current reference for the hybrid P-type ILC controller. Under such circumstance, the use of a fixed sampling frequency is not a suitable solution to determine an integer number of samples per cycle of the current reference signal, which is needed to satisfy the requirement for the application of a P-type ILC controller. A novel algorithm is introduced to provide a variable sampling and switching frequency, thus an integer number of samples per cycle can be achieved for the VSFSAF control loop. To avoid the switching frequency to reach an impractical high value, but at the same time to provide a good quality harmonic compensation at low supply

frequencies, a limitation for the system switching frequency has been fixed. The algorithm provides a step variable number of samples per cycle for the control loop during the supply frequency variation. By doing so, the current control loop can use a higher number of samples per cycle at lower supply frequencies resulting in a better control over what could be achieved with fixed sampling and switching frequency. On the other hand, in order to minimize the variation of the current reference between nearby ILC repetitions, another algorithm is introduced to produce a sinusoidal template for the current reference generation. Since in this application the hybrid P-type ILC controller has to operate with a variable sampling frequency and number of samples, and the number of samples per cycle are strictly related to the discrete delays in the controller, several modifications of the hybrid P-type ILC controller was also made.

The simulation results of the hybrid P-type ILC controlled VSFSAF system shows that the hybrid P-type ILC controller can accurately track the filter current reference and hence the VSFSAF system is capable to provide an accurate current harmonics cancellation during the supply frequency variation. In addition, the simulation results also verify that the VSFSAF system can provide a good dynamic response to load transients occurring during the supply frequency variation. The simulation results therefore validate the feasibility and suitability of the proposed VSFSAF system in the variable supply frequency power network of an aircraft. Corresponding experimental verification will be discussed in the next chapter.

Chapter 8 Experimental setup and results

8.1 Introduction

As analyzed in Chapter 5 and 6, the hybrid P-type ILC controlled SAF and VSFSAF systems can theoretically provide an accurate current harmonic cancellation for both fixed and variable supply frequency power system, this achievement has been proved with extensive and detailed simulation tests . In this chapter, an experimental set-up unit for the proposed hybrid P-type ILC controlled SAF and VSFSAF systems will be described and associated experimental test results will be presented to validate the theoretical achievements. The experimental unit uses a 10kVA power converter built at the University of Nottingham.

In the first part of this chapter, the experimental setup will be introduced. In the second part, the experimental performances of the proposed hybrid P-type ILC controlled SAF and VSFSAF systems will be investigated and discussed.

8.2 Experimental rig used

The overall layout of the experimental setup is presented in fig.8.1, where a three-phase voltage supply is connected to an uncontrolled diode bridge rectifier representing the harmonic producing non-linear load. The SAF/VSFSAF system is connected to the same power network at PCC. The parameters and operational conditions of the voltage supply, diode bridge rectifier and the SAF/VSFSAF system are given in tab.8.1.

There are five main parts in the experimental rig, including the three phase voltage supply, the VSC in the SAF/ VSFSAF system, the data acquisition system, the control platform and the IGBT gate signals generation. The description of these parts will be reported in the following sections.

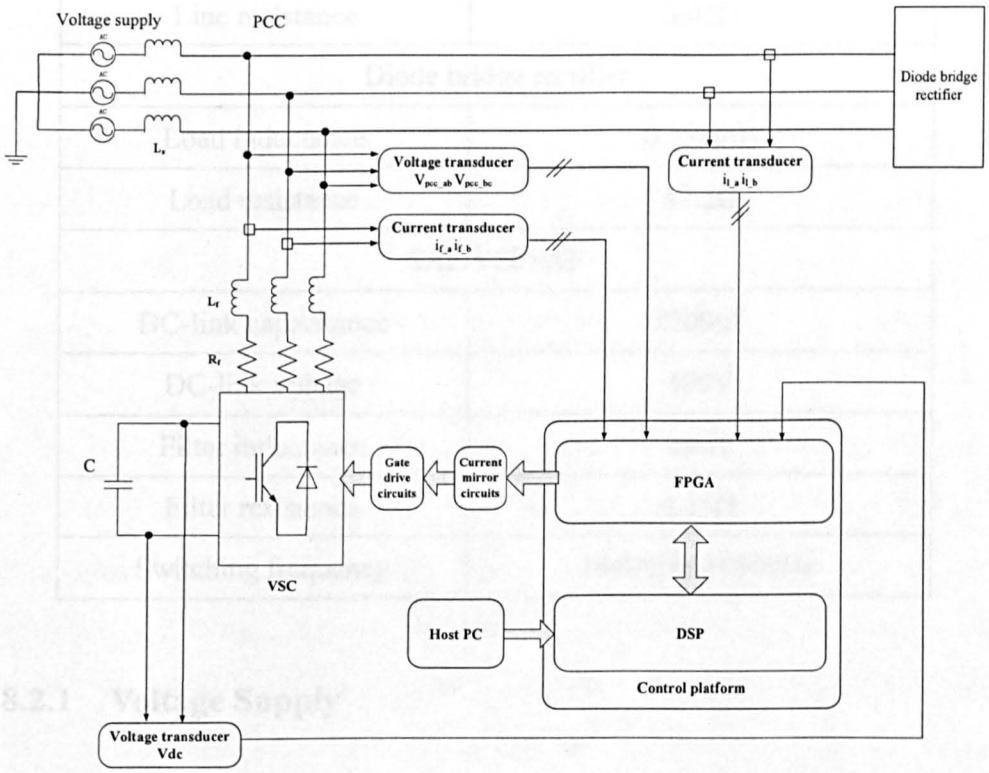

Figure 8. 1: The overall layout of the experimental rig

Table 8. 1: Experimental rig parameters and the operational conditions of the voltage supply, diode bridge rectifier and SAF/VSFSAF

Three-phase voltage supply	
Supply phase voltage	115Vrms, 400Hz-800Hz
Line inductance	0.1mH,400-800Hz
Line resistance	0.02Ω
Diode bridge rectifier	
Load inductance	0.753mH
Load resistance	47.2Ω
SAF/VSFSAF	
DC-link capacitance	2200μF
DC-link voltage	400V
Filter inductance	1mH
Filter resistance	0.15Ω
Switching frequency	14400Hz-16000Hz

8.2.1 Voltage Supply

To reproduce an aircraft power supply, in the experimental rig, a programmable AC source (Chroma 1705) is adopted as the voltage supply to the power network.[87] For the experimental tests of the hybrid P-type ILC controlled SAF system, this AC source produce a three-phase 115Vrms 400Hz voltage in the case of a fixed frequency aircraft power network and a three-phase 115Vrms 400-800Hz voltage in the case of a variable frequency aircraft power network. Since the programmable AC source is programmed by using a host computer, it supply frequency can vary linearly as described in Chapter 7.

8.2.2 The VSC of SAF/VSFSAF

A VSC rated at 10kVA is used in this experimental rig as shown in fig.8.2. The DC-link of VSC consists of two individual electrolytic capacitors. The two 4400μF capacitors are connected in series, which produce a 2200μF DC-link capacitance to the VSC. Since the rated voltage of each capacitor is 400V, the reference DC-link voltage is set to be 400V from safety operation point of view. Six 1200V 300A IGBTs constitute the power switching part; these six IGBTs are controlled by the gate signals produced by the gate drive circuit, which will be described later on in Section 8.2.5. The VSC output is connected to the 1mH coupling inductor to form the SAF/VSFSAF system.

If the VSC is connected directly to the power network with a zero DC-link voltage, a large instant current will flow though the IGBTs and DC-link capacitors, which will damage these devices. Hence, for the safety consideration, two contactors are implemented in the VSC circuit as shown in fig.8.2. During the experiment, the main contactor is disconnected initially, and the pre-charge contactor is manually connected instead to charge the capacitor, till the DC-link capacitor achieves a certain level of DC-link voltage (about 400V), which can guarantee the current flow in the VSC devices to be in the acceptable range when the main contactor is connected.

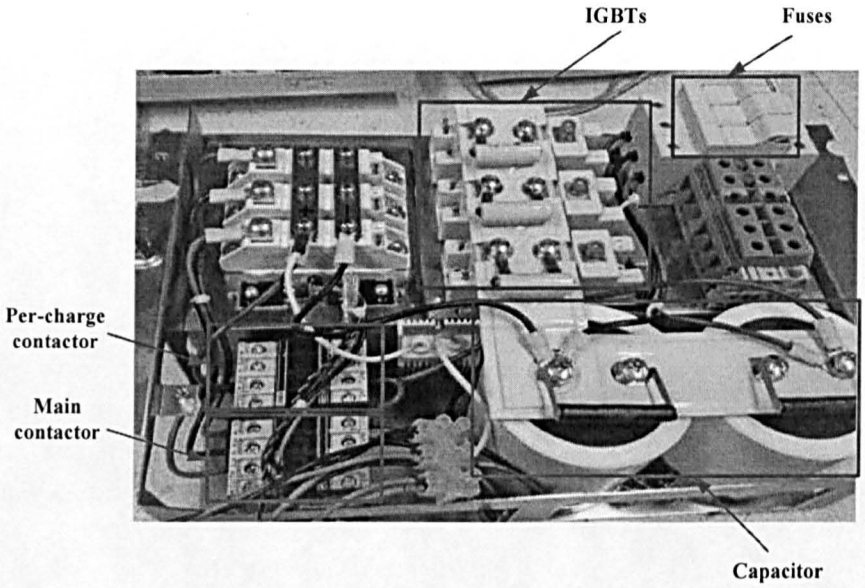

Figure 8. 2: VSC in the SAF/VSFSAF system

8.2.3 The data acquisition system

In the experimental system, the DC-link voltage, two line to line PCC voltages, two SAF output phase currents and two load phase currents need to be measured. In order to measure the required voltages, three LEM voltage transducers are installed on a dedicated board in the experimental rig together with LEM current transducers to measure the SAF output phase currents.[88] In addition, two extra current transducers are used to measure the load phase currents from the diode bridge rectifier. The data acquisition board is shown in fig. 8.3. The analogue measurement signals produced by these transducers are then fed to the analogue to digital converters (ADCs) channels in the field programmable gate array (FPGA) and encoded to digital form.

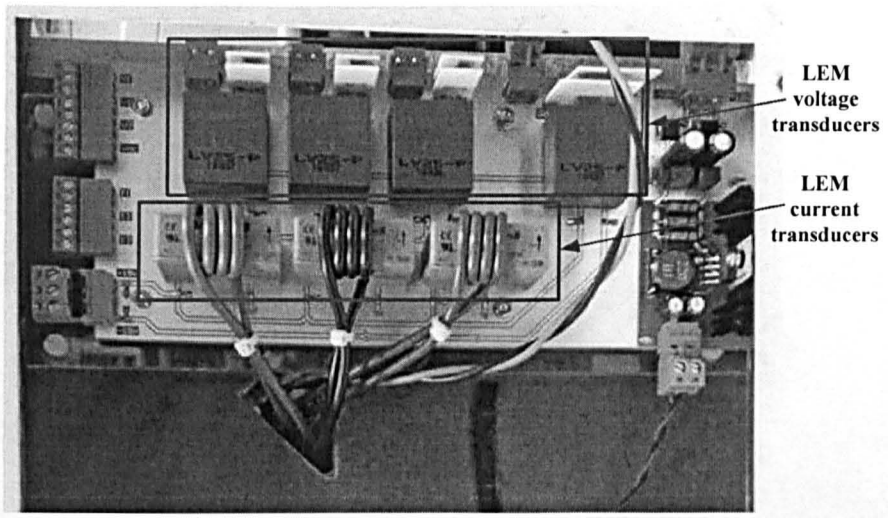

Figure 8. 3: Data acquisition board with voltage and current transducers

8.2.4 The control platform

As shown in fig.8.4, a FPGA and a digital signal processer (DSP) are used for the SAF/VSFSAF DC-link voltage control and current control; together with supervisory controls and system protections.

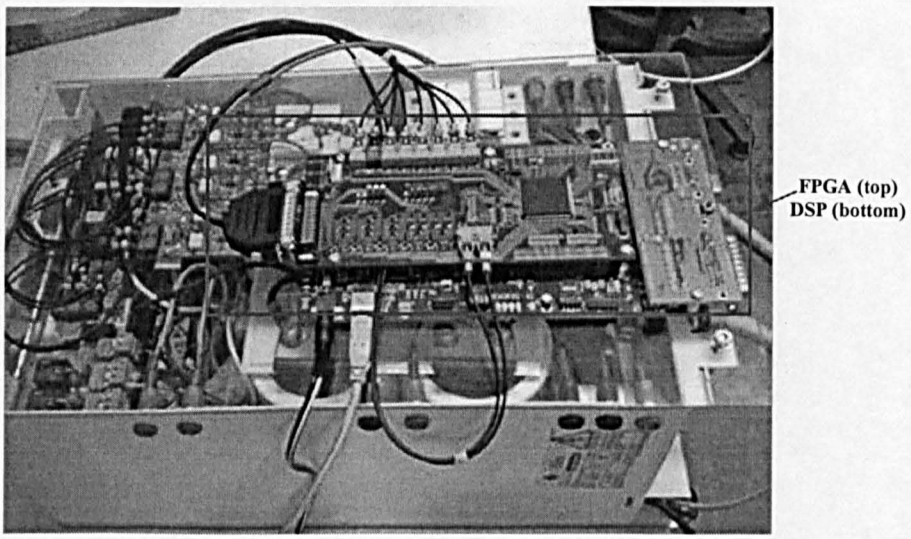

Figure 8. 4: Control platform in the experimental rig

As shown in the corresponding functional block diagram (fig.8.5), the DSP

chip, a Texas Instruments TMS320C44 is used to handle the control calculations. This DSP is a typical 32 bit floating point processor with a clock frequency of 50Mhz. It has a parallel port controller (PPC) connected to the host computer to provide a user interface. The DSP can be programmed in C language using Code Composer Studio on the host computer interfaced with the board. [89]

In the experimental rig, the DSP takes the digital measurements signals from the FPGA as its inputs, and uses the control strategies presented in Chapter 5 and 6 to work out the modulated demand voltage signals of the VSC. The DSP is also responsible for controlling the switching frequency in the FPGA, which is obtained by sending the demand time, when the interrupt occurs, to the FPGA. In the experimental rig, for the SAF test, the interrupt occurs every 69.4μs to make the switching frequency equal to 14400Hz. Similarly, for the VSFSAF application, the interrupt takes place with variable periods (62.5-69.4μs) to provide variable sampling frequencies ranging from 14400Hz to 16000Hz.

The FPGA (Actel ProASIC^{TM} A500,[90]) has two functions: 1) converting the measured currents and voltages from analog signals to digital ones, thus the data can be read by the DSP; 2) when interrupts occur in the DSP, taking the modulated demand voltage signals and the relative time to generate the correct sequence of the PWM pulse signals. The PWM pulse signals then pass through the gate drive circuit to act as the gate signals of IGBTs in the VSC.

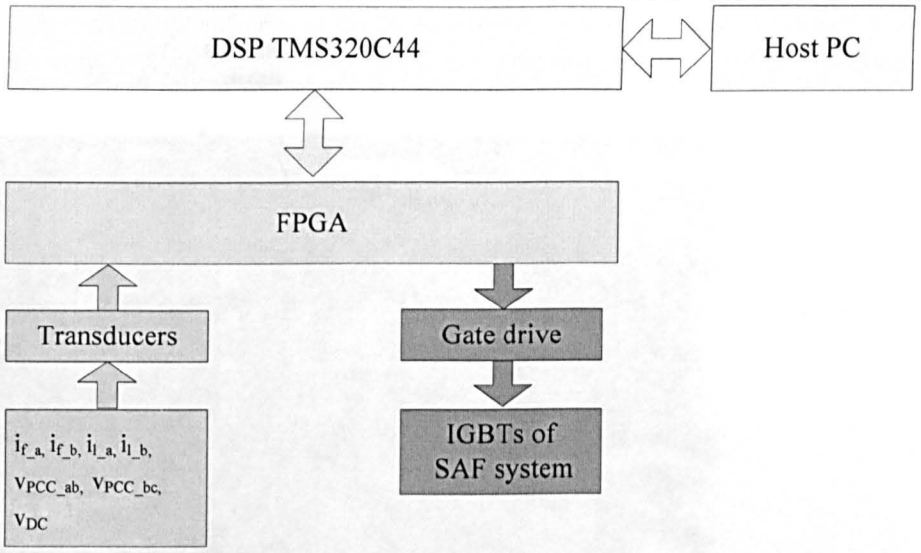

Figure 8. 5: Functional block diagram of the control platform

8.2.5 IGBTs gate signals generation

Optical fiber is used to transmit the PWM pulse signal from the FPGA to the gate drive circuit, which can greatly reduce the influence of switching noise and EMC problems. The gate drive circuits are used for PWM pulse signals amplification, producing a +15V difference between the gate and emitter of the IGBT which enables switching. As shown in fig.8.6, the outputs from the gate drive circuits are connected to the gates of the IGBTs to control the switching of the IGBTs.

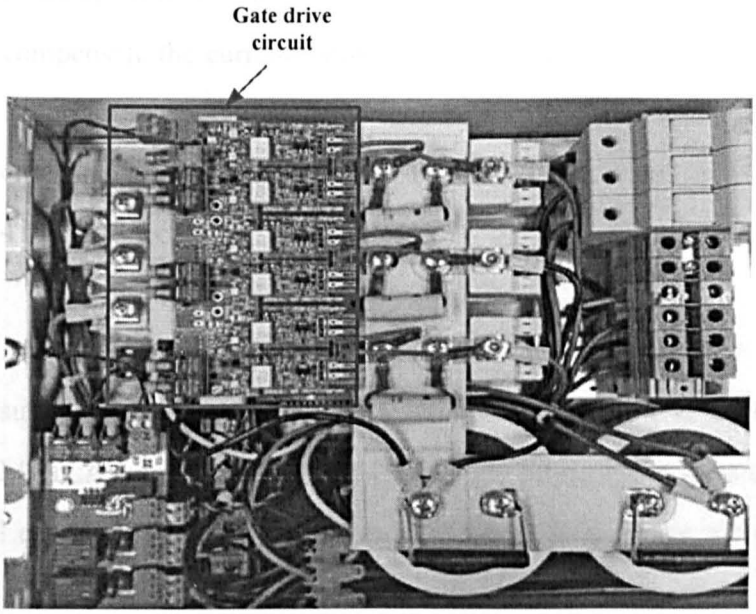

Figure 8. 6: Gate drive circuits in the experimental rig

8.3 The experimental results

For the purpose of validating the theoretical design and the simulations and verifying the current harmonic cancellation performances of the hybrid P-type ILC controlled SAF and VSFSAF systems, corresponding experimental results will be analyzed in this section. The first part of this section presents the experimental results regarding the implementation of the hybrid P-type ILC controlled SAF system. The second part of this section presents the experimental results relative to the implementation of the proposed VSFSAF to verify the performance of system under of supply frequency variation.

8.3.1 Hybrid P-type ILC controlled SAF system

The control system of the hybrid P-type ILC controlled SAF system is implemented in the DSP according to the scheme described in Chapter 6. It is

operated with a fixed sampling and switching frequency of 14400Hz to compensate the current harmonics produced by the diode bridge rectifier load. In order to meet the requirement of the IDG power system operational environment, the supply voltage and frequency are set to be 115Vrms and 400Hz respectively.

In order to investigate the performance of the proposed SAF system and obtain suitable measurements, all data are captured by the DSP and transferred to the MATLAB host interface with a sampling frequency of 14400Hz. In addition, a LeCroy oscilloscope is used to measure the PCC phase voltage and the supply current with a high sampling frequency of 50MHz.

The current reference tracking performance of the hybrid P-type ILC controller will be presented firstly, followed by the harmonic cancellation performance of the whole SAF system.

8.3.2 Performance of current reference tracking

Figure 8.7 shows the comparison between the demand supply phase current (current reference) and the actual supply phase current in both experiments and simulations. Table 8.2 presents the maximum and average tracking error (MTE and ATE) obtained from both experimental and simulation results. The mismatch between the MTE and ATE will be explained in Section 8.3.3. In general, the experimental results shows the hybrid P-type ILC controller is capable of providing an accurate current tracking.

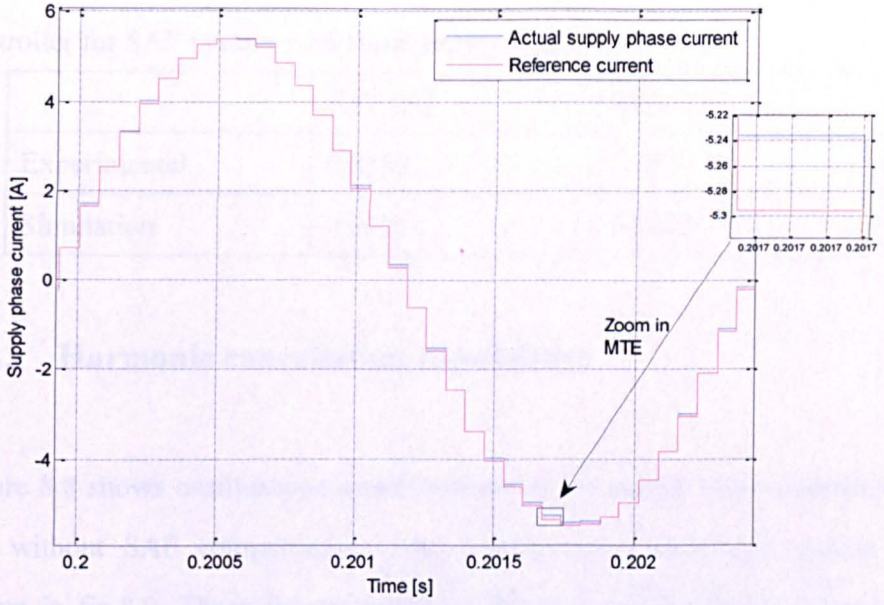

Figure 8. 7a: Current reference tracking of the hybrid P-type ILC controlled SAF system with fixed supply frequency (experimental)

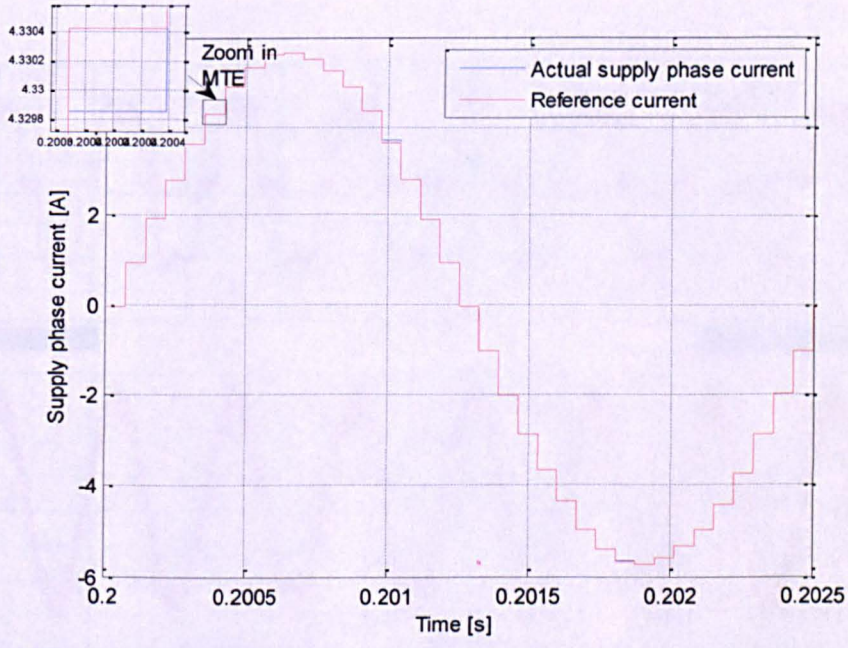

Figure 8.7b: Current reference tracking of the hybrid P-type ILC controlled SAF system with fixed supply frequency (simulation)

Table 8. 2: Current reference tracking errors of the hybrid P-type ILC controller for SAF system with fixed supply frequency

	ATE [A]	MTE [A]
Experimental	0.0193	0.0533
Simulation	0.0023	0.0092

8.3.3 Harmonic cancellation capabilities

Figure 8.8 shows oscilloscope measurements of the supply phase current with and without SAF compensation. The corresponding harmonic spectra are shown in fig.8.9. These figures highlight that the proposed SAF system can provide an effective current harmonic cancellation for the power network with fixed supply frequency. The THD of the supply phase current is reduced from 27.12% to 0.5411%.

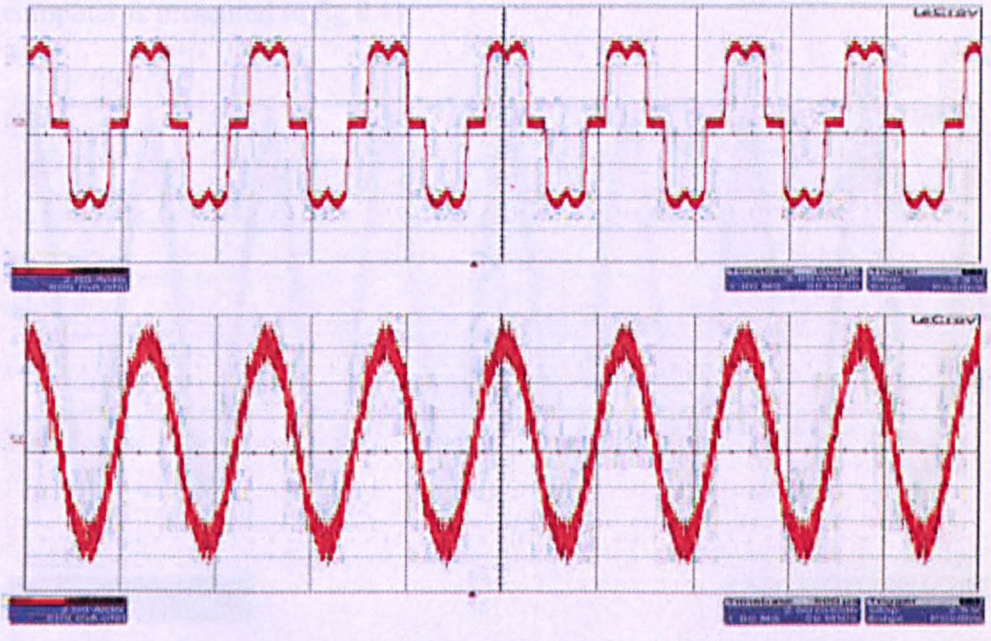

Figure 8. 8: Supply phase current without (top) and with (bottom) SAF compensation (x-axis [2ms/div] y-axis [2A/div])

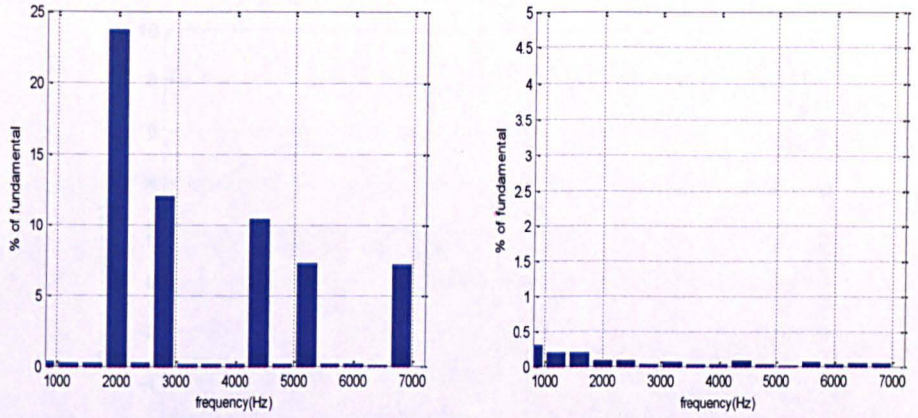

Figure 8. 9: Harmonic spectrum of the supply phase current without and with SAF compensation operated in fixed supply frequency (experimental)

Figure 8.10 shows the waveforms of PCC phase voltage (green) and the supply phase current (red) acquired by the oscilloscope. It clearly shows that, with the compensation of the SAF system, the supply phase current and the PCC phase voltage are in phase ensuring unity power factor operation. The waveform of three-phase supply current after SAF compensation measured through the host computer is presented in fig.8.11.

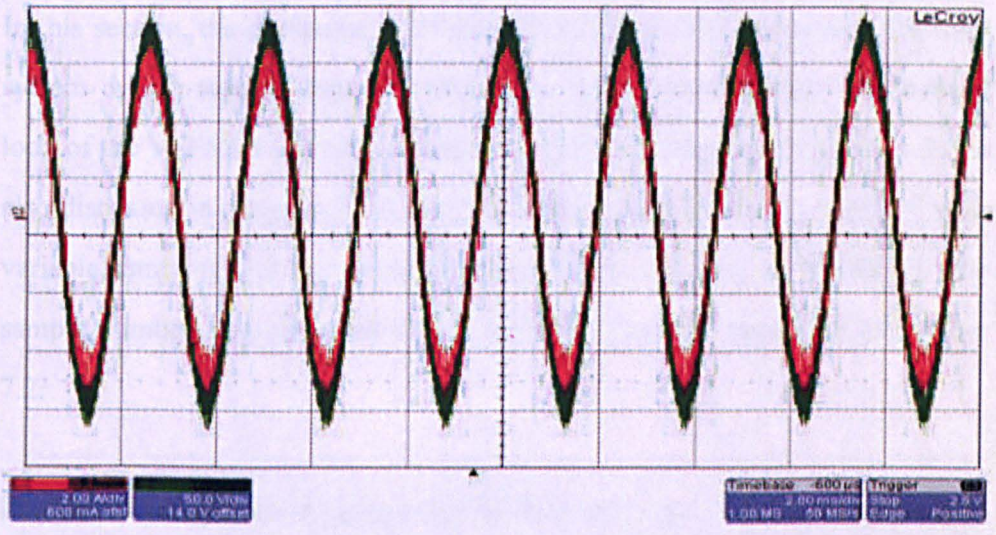

Figure 8. 10: PCC phase voltage and supply phase current e (x-axis [2ms/div] y-axis [C2 current 2A/div], [C3 voltage 50V/div])

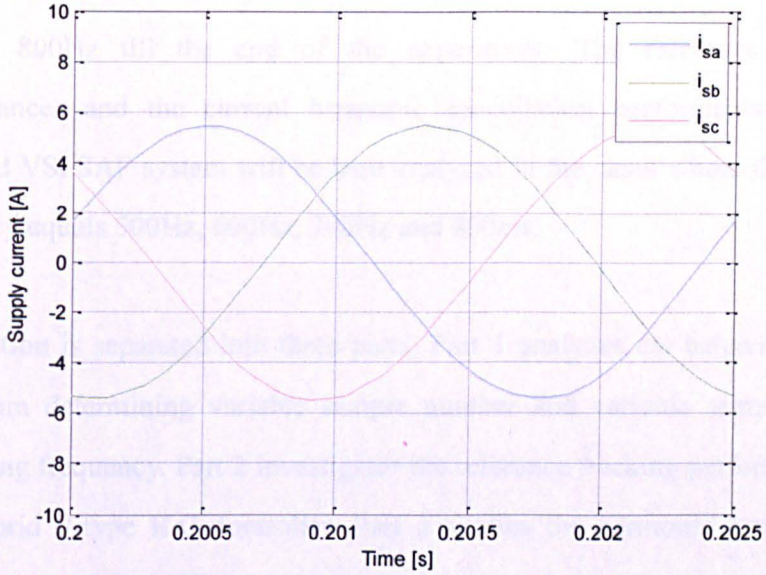

Figure 8. 11: Three-phase supply current with SAF compensation operated at 400Hz fixed supply frequency (experimental)

8.3.4 The performance of the hybrid P-type ILC controlled VSFSAF system

In this section, the performance of the hybrid P-type ILC controlled VSFSAF system during supply frequency variations will be investigated. The control loop of the VSFSAF is implemented in the DSP as described in Chapter 7. As also discussed in Chapter 7, the control loop of the VSFSAF is operated with variable sampling and switching frequency (from 14400Hz to 16000Hz). The sample number also varies according with the algorithm presented in Section 7.2.

In order to verify correct current reference tracking and harmonic cancellation performances of the proposed VSFSAF system during the supply frequency variation, the supply voltage source is programmed as discussed in Section 8.2.1. In the experimental tests, the supply frequency is maintained at 400Hz

for 1.2 second, then linearly increased to 800Hz within 4 second and then is kept at 800Hz till the end of the experiment. The reference tracking performances and the current harmonic cancellation performances of the proposed VSFSAF system will be here analyzed in the cases where the supply frequency equals 500Hz, 600Hz, 700Hz and 800Hz.

This section is separated into three parts. Part 1 analyzes the behavior of the algorithm determining variable sample number and variable sampling and switching frequency. Part 2 investigates the reference tracking performance of the hybrid P-type ILC controller. Part 3 studies the harmonic cancellation performance of the VSFSAF system.

8.3.4.1 Variable sampling (switching) frequency and variable sample number algorithm

Figure 8.12 shows the supply frequency, sampling frequency and the samples number per cycle respectively. This figure clearly shows that, the sampling (switching) frequency varies with the supply frequency; and when the sampling (switching) frequency exceed its upper bound (16000Hz), the sample number is reduced by 2 as expected. The test shows that the algorithm for sampling (switching) and sample number determinations works properly in the experimental rig.

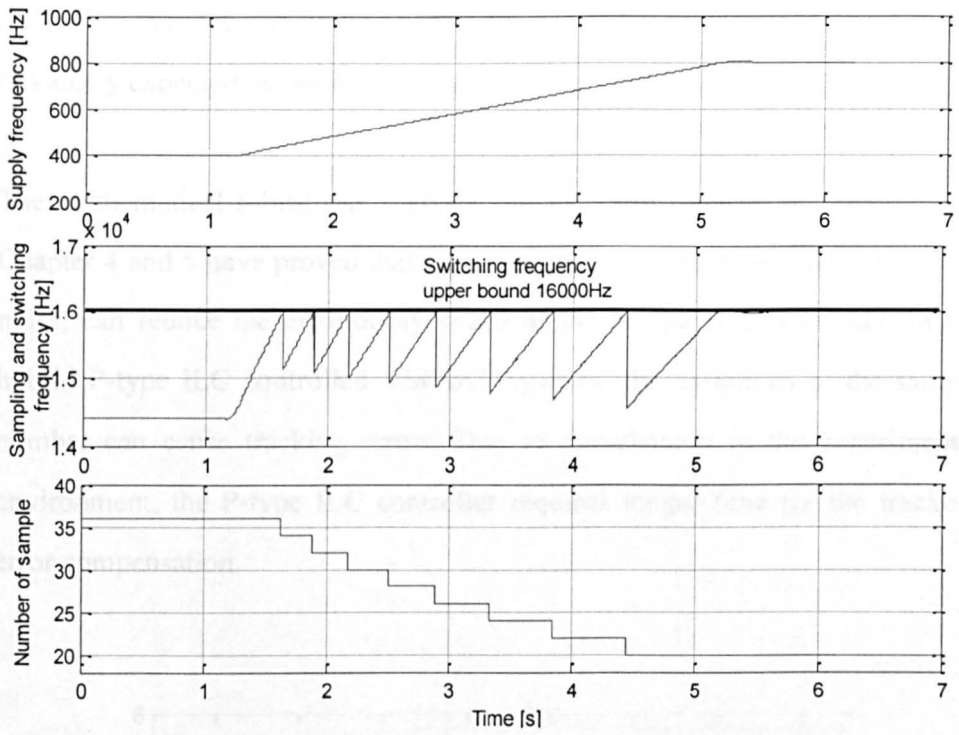

Figure 8. 12: Supply frequency, sampling (switching) frequency and the samples number (experimental)

8.3.4.2 Performance of current reference tracking

The current reference tracking performances of the hybrid P-type ILC controlled VSFSAF, when the supply frequency reaches 500Hz, 600Hz, 700Hz and 800Hz are shown in fig,8.13, 8.14, 8.15 and 8.16 respectively. The experimental results clearly show that the proposed VSFSAF system is able to provide a good current reference tracking during the supply frequency variation.

The corresponding MTE and ATE obtained from both experiment and computer simulations are presented in Tab.8.3. It is found that, although the hybrid P-type ILC controller provides a good reference tracking during the supply frequency variation, the MTEs and ATEs obtained from the experiment

are higher than the one obtained from the computer simulation. Even if this is obviously expected, it can be explained as follows.

The mathematical robustness analysis and the simulation results presented in Chapter 4 and 5 have proved that disturbances, such as the measurement white noise, can reduce the error-decay speed of the P-type ILC controller. In the hybrid P-type ILC controlled VSFSAF system, the variations of the sample number can cause tracking errors. Due to disturbances in the experimental environment, the P-type ILC controller requires longer time for the tracking error compensation.

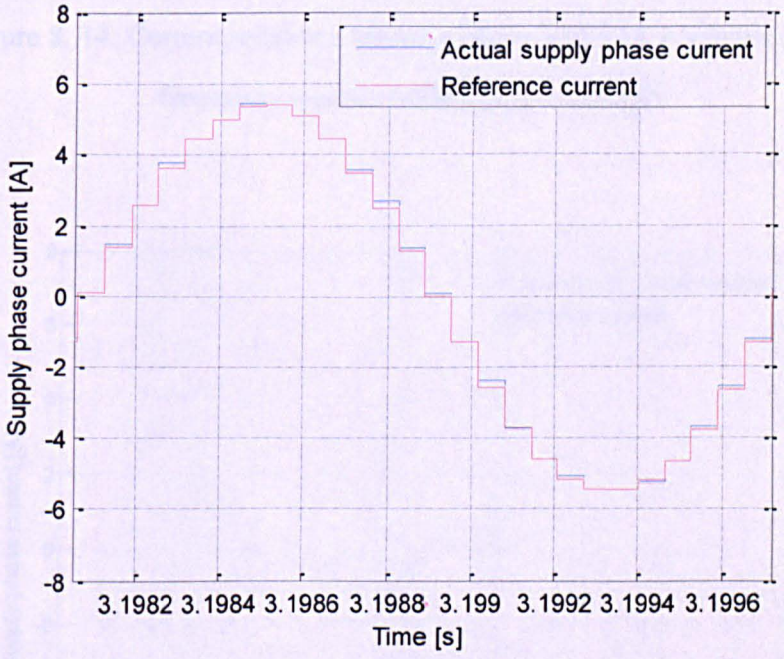

Figure 8. 13: Current reference tracking of the VSFSAF when the supply frequency reaches 500Hz (experimental)

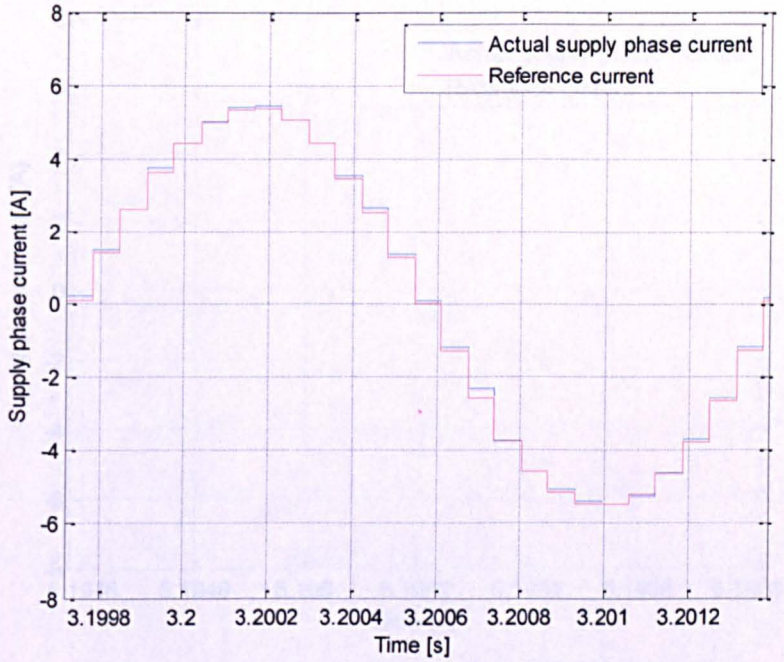

Figure 8. 14: Current reference tracking of the VSFSAF when the supply frequency reaches 600Hz (experimental)

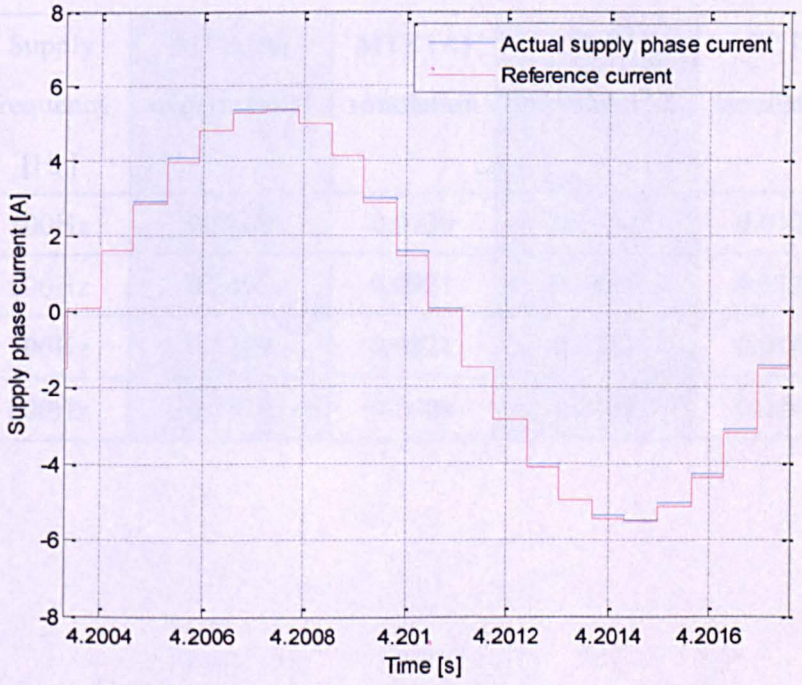

Figure 8. 15: Current reference tracking of the VSFSAF when the supply frequency reaches 700Hz (experimental)

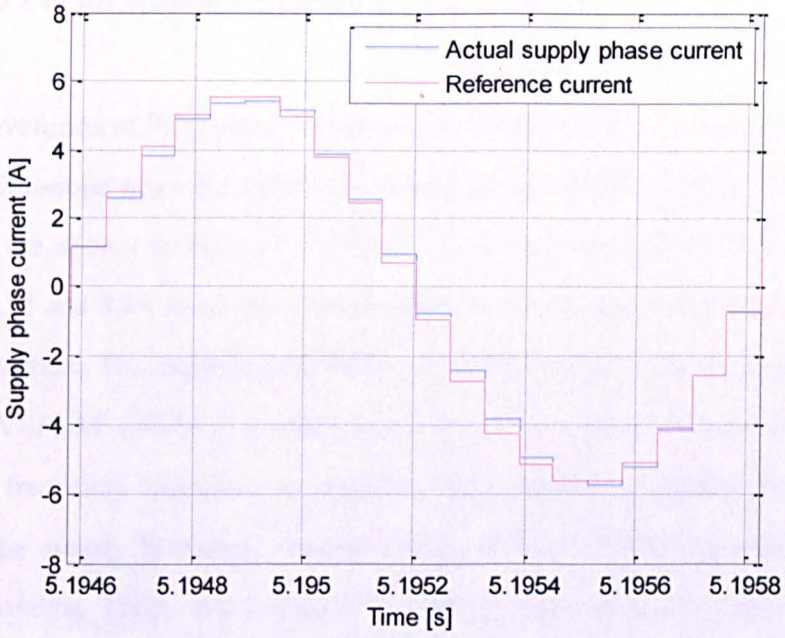

Figure 8. 16: Current reference tracking of the VSFSAF when the supply frequency reaches 800Hz (experimental)

Table 8. 3: Current reference tracking errors introduced by the hybrid P-type ILC controller for variable supply frequencies

Supply frequency [Hz]	MTE [A] experimental	MTE [A] simulation	ATE [A] experimental	ATE [A] simulation
500Hz	0.6268	0.0739	0.1314	0.0122
600Hz	0.2405	0.0921	0.0886	0.0136
700Hz	0.1289	0.0831	0.0383	0.0105
800Hz	0.3338	0.1008	0.1189	0.0451

8.3.4.3 Performance of harmonic cancellation

The waveforms of PCC phase voltage and the supply phase current acquired by the oscilloscope when the supply frequency reaches 500Hz, 600Hz, 700Hz and 800Hz are shown in fig.8.17, 8.19, 8.21 and 8.23 respectively. Figure 8.18, 8.20, 8.22 and 8.24 show the corresponding harmonic spectrums of the supply phase current. The experimental results show the supply current compensated by the VSFSAF system is synchronous with the PCC phase voltage during the supply frequency variation. In addition, the harmonic spectrums show that, when the supply frequency reaches 500Hz, 600Hz, 700Hz and 800Hz, the corresponding THDs are 0.8680%, 1.1308%, 1.3823% and 2.2317%. This indicates that the hybrid P-type ILC controlled VSFSAF system can successfully reduce the current harmonics generated by the non-linear load in the power system, during the supply frequency variation.

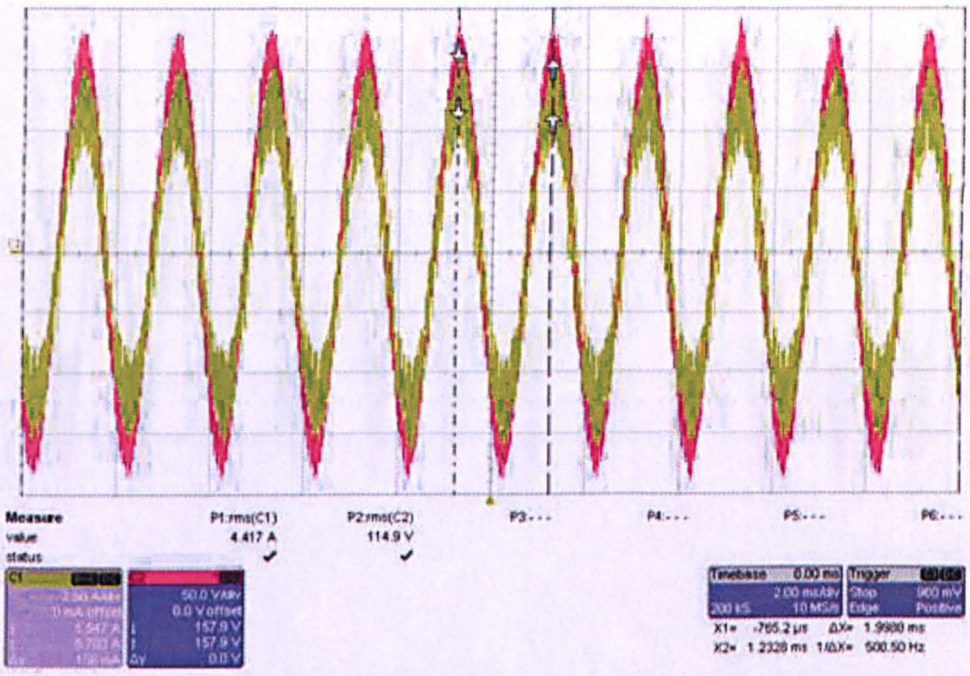

Figure 8. 17: PCC phase voltage and supply phase current acquired as the supply frequency reaches 500Hz (x-axis [2ms/div] y-axis [C1 current 2.5A/div], [C2 voltage 50V/div])

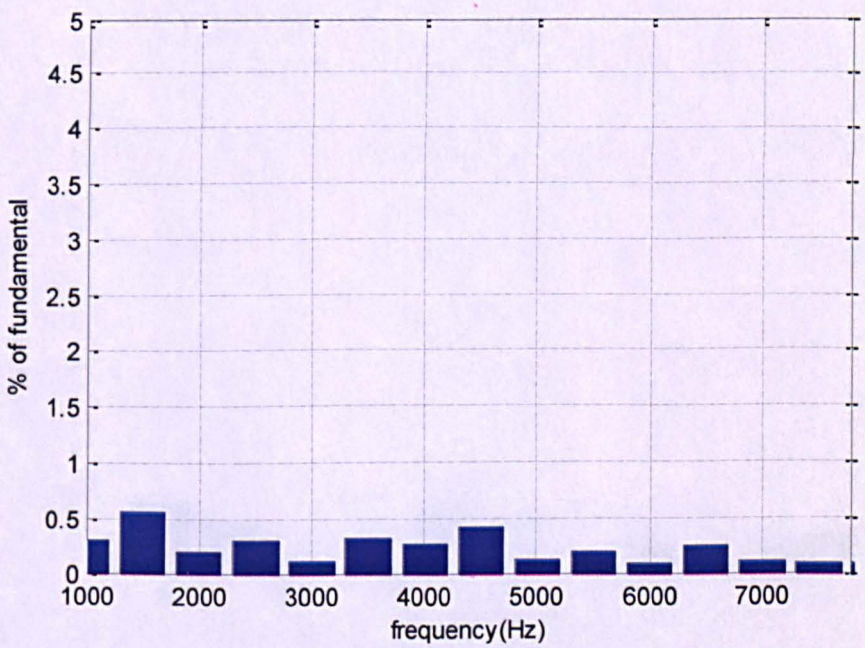

Figure 8. 18: Harmonic spectrum of the supply phase current with VSFSAF compensation at 500Hz (experimental)

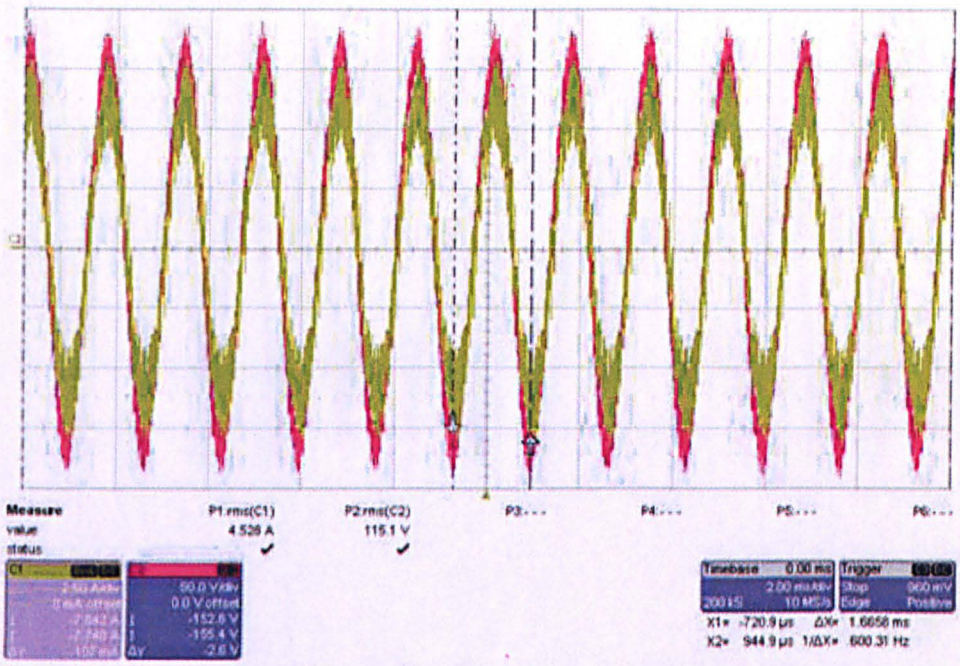

Figure 8. 19: PCC phase voltage and supply phase current acquired as the supply frequency reaches 600Hz (x-axis [2ms/div] y-axis [C1 current 2.5A/div], [C2 voltage 50V/div])

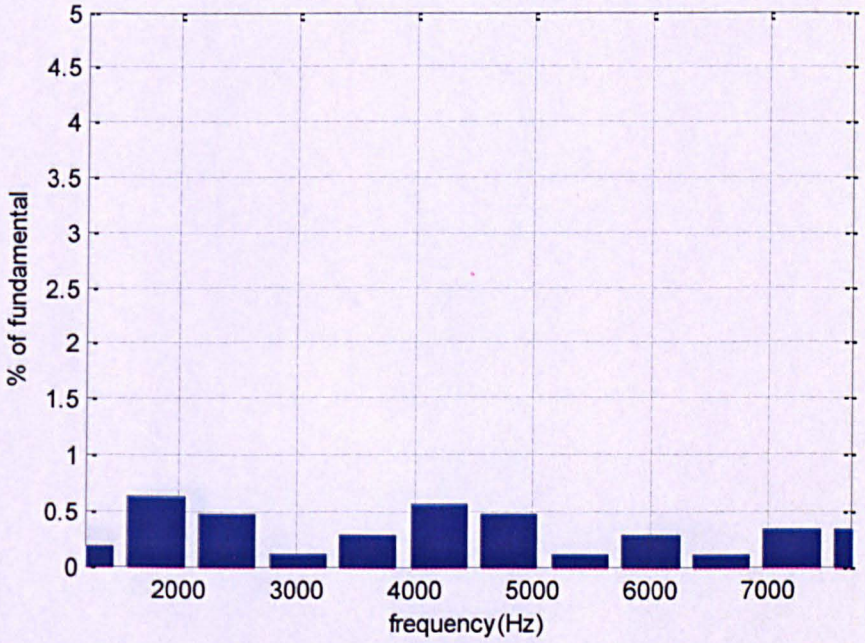

Figure 8. 20: Harmonic spectrum of the supply phase current with VSFSAF compensation at 600Hz (experimental)

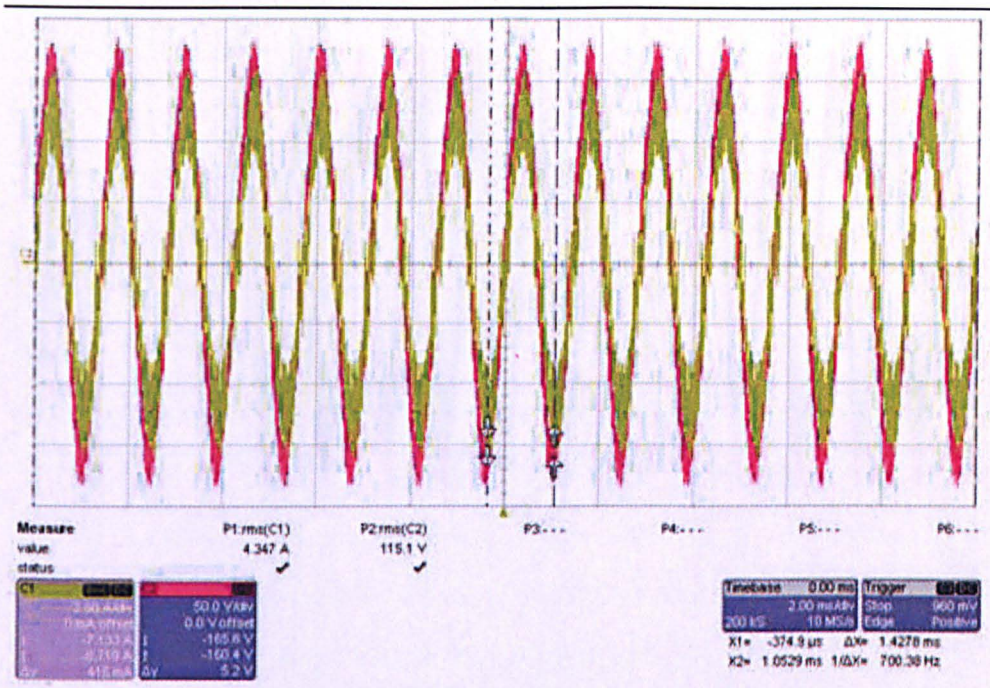

Figure 8. 21: PCC phase voltage and supply phase current acquired as the supply frequency reaches 700Hz (x-axis [2ms/div] y-axis [C1 current 2.5A/div], [C2 voltage 50V/div])

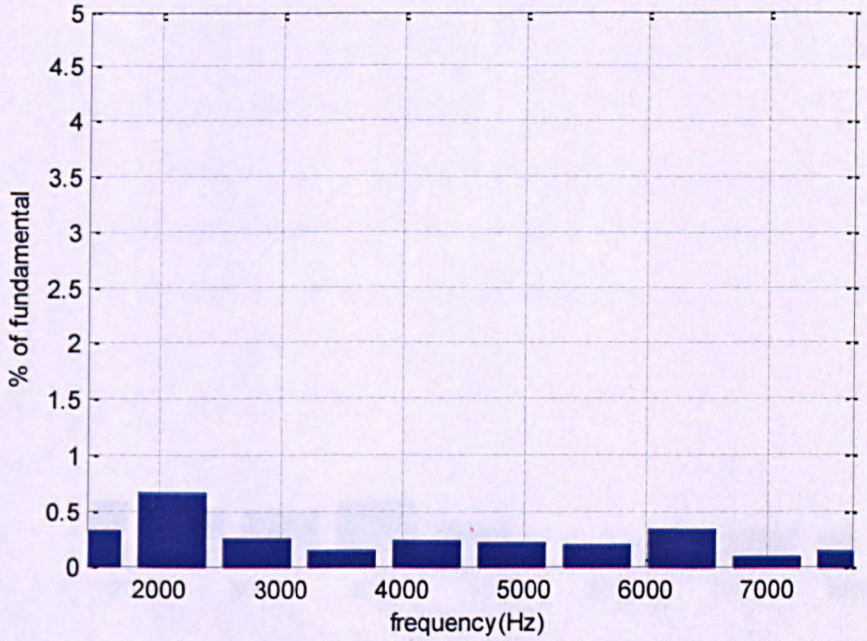

Figure 8. 22: Harmonic spectrum of the supply phase current with VSFSAF compensation at 700Hz (experimental)

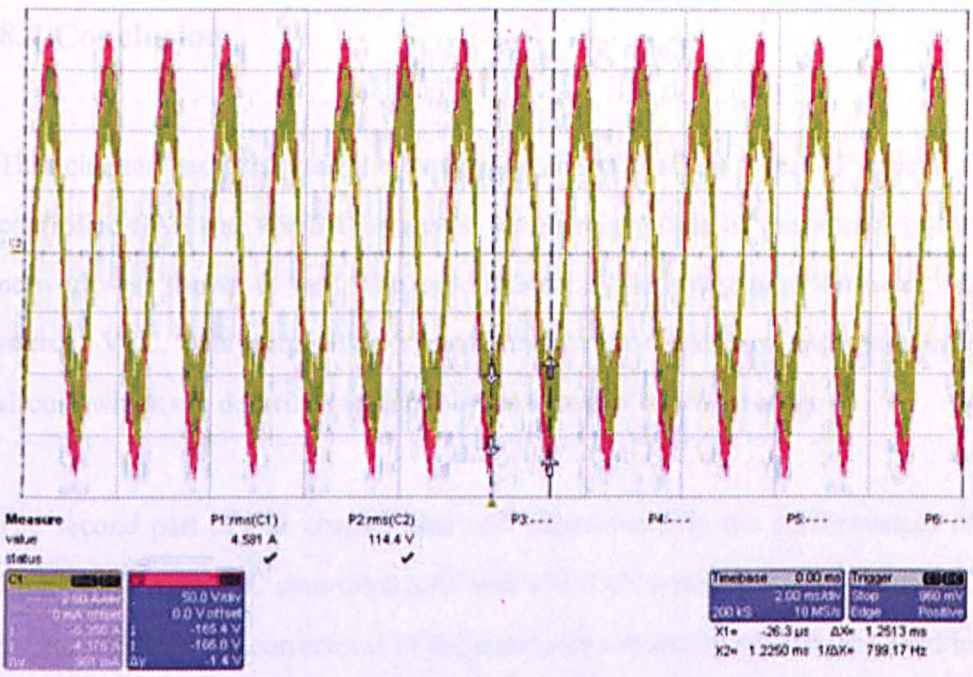

Figure 8. 23: PCC phase voltage and supply phase current acquired at the supply frequency reaches 800Hz (x-axis [2ms/div] y-axis [C1 current 2.5A/div], [C2 voltage 50V/div])

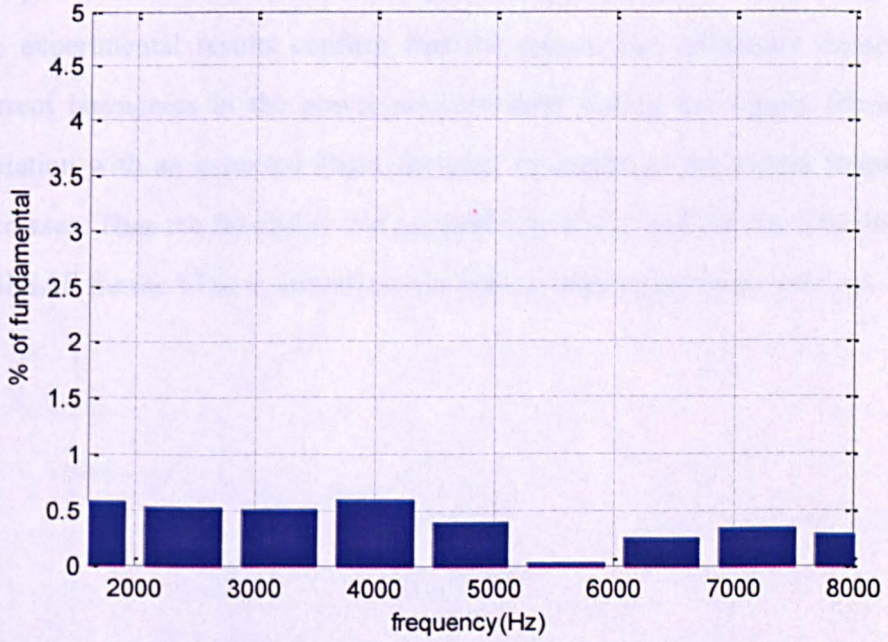

Figure 8. 24: Harmonic spectrum of the supply phase current with VSFSAF compensation at 800Hz (experimental)

8.4 Conclusion

This chapter has presented the experimental setup of the hybrid P-type ILC controlled SAF and VSFSAF systems. The configuration of the overall power network was shown as well. The experimental rig includes: programmable AC source, VSC, data acquisition system, the control platform and gate drive circuit, which are described in detail in the first part of this chapter.

The second part of this chapter analyzed experimentally the performances of the hybrid P-type ILC controlled SAF and VSFSAF systems. The experimental results validated the correctness of the computer simulation results presented in Chapter 6 and 7 and the validity of the theoretical treatment presented. The ability of providing accurate current tracking for the hybrid P-type ILC controller is therefore experimentally proven. For the power system with fixed 400Hz supply frequency, THD can be significantly reduced by the compensation of the proposed SAF system. For the proposed VSFSAF system, the experimental results confirm that the system can efficiently cancel the current harmonics in the power network even during the supply frequency variation with an expected slight decrease in quality as the supply frequency increases. Thus the feasibility and applicability of the SAF for the IDG and the VSFSAF for the VFG in aircraft power system in experimentally verified.

Chapter 9 Conclusion

Due to the large presence of distorting loads, constant-power loads, widespread devices interconnections and relatively large grid impedances, at least compared to the conventional power distribution systems, power quality issues such as harmonic pollution, voltage dips and swells and grid stability are difficult to address in an aircraft power grid. These problems will be exacerbated in the new generation aircrafts, since the fundamental frequency will become variable over a wide range. The aim of this project was therefore to investigate active filtering solutions to be installed in aircraft networks (for both fixed and variable frequency configurations) to overcome the above mentioned problems

9.1 Current control strategies for SAF

The review of the existing SAF current control strategies presented in Chapter 2, has pointed out advantages and disadvantages of each of them; only a few of these control strategies could be capable to accurately compensate the current harmonics with a wide-bandwidth control for 400Hz fixed supply frequency aircraft power networks; none of them can provide accurate current harmonics compensation in variable supply frequency power networks (400-800Hz). For example the P+resonant control presented in Chapter 3 is able to achieve a small steady state reference tracking error for specific current harmonic components with a fast dynamic response. This characteristic has been demonstrated through simulation tests. However, the design of P+resonant controller strictly requires a very careful tuning to adjust the resonant frequencies matching the specific harmonic components to regulate. This drawback limits its applicability for the SAF system with variable supply

frequency which leads to variable harmonic frequencies. Also resonant control requires a quite complex design procedure where many parameters have to be determined on the basis of system stabilities and performance. The use of an approach based on Iterative learning control (ILC) has made possible to overcome these issues.

The principles of the P-type ILC controller have been introduced in Chapter 4. ILC is a viable solution where the goal of the control is to track a repetitive (periodic) reference signal, like theoretically in the current control for an active filter. However, in the SAF cascade control structure, the reference for the inner current control loop is related with the output of the outer voltage control loop, which can cause a non-periodical variation of the reference for the inner control loop. A mathematical robustness analysis presented in Chapter 4 proved that the P-type ILC controller can still operate properly in the inner control loop with a tolerable non-periodical variation of its reference signal. The mathematical analysis also found that, if the variation of the reference signal and the amplitude of disturbances are within an acceptable range, these reference variation and disturbances will only slow down the error-decay speed of the P-type ILC controller, but not jeopardize the control action.

The simulation results presented in Chapter 5 validated 1) the correctness of the robustness analysis presented in Chapter 4; 2) the accurate wide-band harmonic compensation capability of the P-type ILC in SAF current control. The feasibility of applying the P-type ILC for SAF control in high frequency power networks was then successfully proved through theoretical analysis and corresponding simulation tests.

9.2 P-type ILC for SAFs in IDG power systems

By analyzing the simulation results of the P+resonant and direct P-type ILC controlled SAF systems presented in Chapter 3 and 5, several drawbacks of the standard P-type ILC were highlighted. Although the standard P-type ILC provides a more accurate current reference tracking than the P+resonant control and does not need a tuned controller for each harmonic (or sets of harmonics) to be regulated, it has a poor dynamic response to load transient and very limited robustness against system disturbances (measuring white noise and non-periodical transient signal from the outer voltage control loop). Based on the research of the P-type ILC principle and the corresponding robustness analysis in Chapter 4, several modifications have been investigated and applied in Chapter 6, for the purpose of improving the dynamic response, robustness and boosting the error-decay speed.

The simulation results presented in Chapter 6 show that, the proposed modifications of the P-type ILC including the traditional hybrid P-type ILC structure with a improved design procedure, the new variable learning gain concept, the over-damped voltage loop PI controller and the introduction of a forgetting factor, significantly improve the dynamic response, error-decay speed and robustness of the SAF current control loop. The experimental results (presented in Chapter 8) verified that, the optimized hybrid P-type ILC controller provides an very accurate reference tracking in the SAF control loop, and hence the corresponding SAF system provides an efficient harmonic compensation for aircraft power networks with a 400Hz fixed supply frequency.

9.3 P-type ILC for SAFs in VFG power system

As presented in Chapter 2, the adoption of the VFG in aircraft power networks can lead to several benefits; however, such choice results in variable supply frequency which increases the challenges for power quality improvement and current harmonic reduction. This research project also investigates a shunt active power filter solution based on the P-type ILC in variable supply frequency aircraft power networks using a fully digital control implementation.

In Chapter 7, two novel solutions are investigated and implemented to extend and adopt the control strategy developed for the SAF operating at fixed supply frequency to the case of variable frequency supply systems and therefore capable of variable frequency harmonic currents compensation. These solutions provide:

1) Variable sampling and switching frequency operation in the SAF system. A step change reduction/increase in number of samples per cycle when the supply frequency increases/decreases respectively. This solution will provide a sampling/switching frequency within a certain band, to avoid the use of impractical switching frequency values. It will lead to a compromise solution where the effectiveness of the compensation reduces with the increase of the supply frequency, still keeping good results at the highest frequency values.

2) A suitable interpolation routine included in the control to make sure that, despite the variable number of samples per cycle, the iterative learning control condition of a cyclic reference under a ramp supply frequency variation can be satisfied during number of samples step changes.

Simulation and experimental results presented in Chapter 6 and 8 shows that the proposed SAF system provides an accurate and effective current harmonic compensation and hence validates the feasibility and suitability of this VSFSAF solution in aircraft variable supply frequency power networks.

9.4 Further work

Even if the application of the ILC controlled Shunt active power filter for 400Hz fixed frequency aircraft power network proved to be a very successful full digital solution, a couple of issues still remains for the variable supply frequency implementation.

First of all, the small transients appearing on the simulation and experimental results in correspondence with step variations of number of samples per cycle, need to be addressed. This phenomenon is probably due to both the interaction of the interpolation routine with the control and the accuracy of the PLL used. Further investigation of this problem is required aiming to acheive a more effective reference tracking during these transient conditions.

Secondly, the system performance has been tested only for ramp supply frequency variation with a certain slope. More tests will be required to investigate needed when different profiles of the supply frequency variation, as soon as the aircraft industry will make available more information on the subject.

Finally a test of the VSFSAF inserted in a real or emulated aircraft supply grid would be interesting to validate the filter behavior in a more practical environment.

Appendix A

Fundamental and harmonic transformation to a dq frame of reference

The d-q transformation is a conversion of coordinates from the three-phase stationary coordinate system to the d-q rotating system. The transformation is a very useful tool for the analysis and modeling of a three phase electrical system. This transformation is performed in two steps. Firstly, in the case that the three-phase is in balance, a transformation from the three-phase stationary coordinate system to the two-phase (α-β stationary coordinate system, where γ is zero) then transformation from the α-β stationary coordinate system to the d-q rotating coordinate system. In three phase (three-dimensional) space, a vector $\vec{X}$ can be represented as:

$$\overrightarrow{X_{abc}} = [\overrightarrow{u_a} \quad \overrightarrow{u_b} \quad \overrightarrow{u_c}] \begin{bmatrix} \overrightarrow{X_a} \\ \overrightarrow{X_b} \\ \overrightarrow{X_c} \end{bmatrix} \tag{A.1}$$

Where $\overrightarrow{X_{abc}}$ represents a voltage or a current vector in three-phase system with its instantaneous phase values of $\overrightarrow{X_a}$, $\overrightarrow{X_b}$ and $\overrightarrow{X_c}$; $\overrightarrow{u_a}$, $\overrightarrow{u_b}$ and $\overrightarrow{u_c}$ are vectors of unit in a-axis, b-axis and c-axis respectively.

The transformation of a a-b-c vector representation to a α-β-γ orthogonal system is performed through the transformation matrix T which is defined as Equation (A.2) shows where θ is the phase angle between the two coordinate systems at the same time.

$$T = \frac{2}{3}\begin{bmatrix} \cos\theta & \cos\left(\theta - \frac{2\pi}{3}\right) & \cos\left(\theta + \frac{2\pi}{3}\right) \\ -\sin\theta & -\sin\left(\theta - \frac{2\pi}{3}\right) & -\sin\left(\theta + \frac{2\pi}{3}\right) \\ \frac{1}{2} & \frac{1}{2} & \frac{1}{2} \end{bmatrix} \quad \text{(A.2)}$$

The coefficient 2/3 is somewhat arbitrarily chosen. The commonly used value is 2/3 or $\sqrt{(2/3)}$. The main advantage of using 2/3 is that the magnitude of the two-phase voltages will be equal to that of the three-phase voltages after the transformation.

- **Transformation from a-b-c to α-β coordinate system**

In this work for both simulation and experimental implementation the PCC voltage has been considered as a reference for all the transformations. Assuming a balanced three-phase voltage system the only two line to line voltage V_{AB} and V_{BC} have been measured, from those the correspondent phase voltages V_{AN}, V_{BN}, V_{CN}, can be derived. By taking the phase angle of A-phase input voltage as the reference angle, the three input phase voltages can be described as:

$$\begin{aligned} V_{AN} &= V_x \cos \omega t \\ V_{BN} &= V_x \cos\left(\omega t - \frac{2\pi}{3}\right) \\ V_{CN} &= V_x \cos\left(\omega t + \frac{2\pi}{3}\right) \end{aligned} \quad \text{(A.3)}$$

Where V_X and ω are the voltage magnitude and angular frequency respectively. The voltage considering the representation of voltage vector $\vec{V}$ in different coordinate systems, which are three-phase system a-b-c, orthogonal two-phase stationary system α-β (γ equals to zero if phase balanced) as shown in Figure A.1.

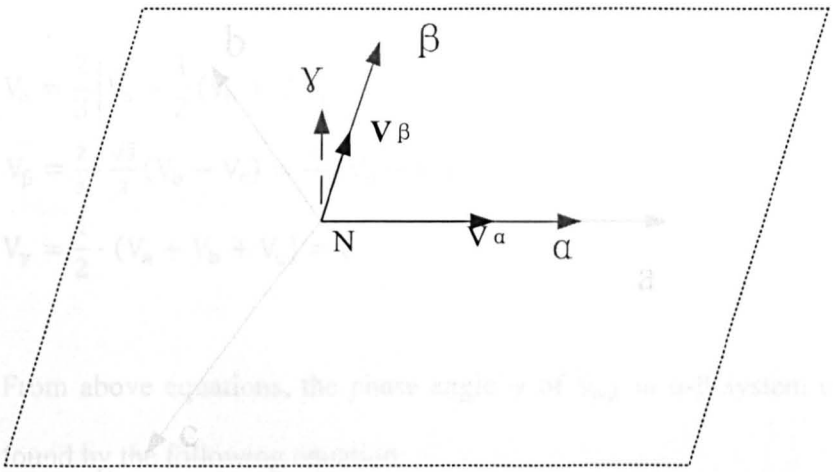

Figure A.1: Representation of voltage vector in a-b-c and α-β coordinate systems.

In this transformation it is usual to have the α-axis aligned with a-axis as shown in Figure A.1, thus the phase angle between the a-b-c and α-β coordinate systems is zero at any time: θ=ωt=0. Replacing this value to Equation (A.2), the Park's transformation matrix becomes:

$$T_{abc/\alpha\beta\gamma} = \frac{2}{3}\begin{bmatrix} \cos 0 & \cos\left(-\frac{2\pi}{3}\right) & \cos\left(\frac{2\pi}{3}\right) \\ -\sin 0 & -\sin\left(-\frac{2\pi}{3}\right) & -\sin\left(\frac{2\pi}{3}\right) \\ 1/2 & 1/2 & 1/2 \end{bmatrix} = \frac{2}{3}\begin{bmatrix} 1 & -\frac{1}{2} & -\frac{1}{2} \\ 0 & \frac{\sqrt{3}}{2} & -\frac{\sqrt{3}}{2} \\ \frac{1}{2} & \frac{1}{2} & -\frac{1}{2} \end{bmatrix} \quad \text{(A.6)}$$

The coordinates of vector $\vec{V}$ in α-β frame is $V_{\alpha\beta}$

$$\begin{bmatrix} V_\alpha \\ V_\beta \\ V_\gamma \end{bmatrix} = \frac{2}{3}\begin{bmatrix} 1 & -\frac{1}{2} & -\frac{1}{2} \\ 0 & \frac{\sqrt{3}}{2} & -\frac{\sqrt{3}}{2} \\ \frac{1}{2} & \frac{1}{2} & -\frac{1}{2} \end{bmatrix}\begin{bmatrix} V_a \\ V_b \\ V_c \end{bmatrix} \quad \text{(A.7)}$$

In a balanced three phase voltage system the coordinates of voltage vector V (or any vector in general) represented in α-β frame can be calculated as follows

$$V_\alpha = \frac{2}{3}\left[V_a - \frac{1}{2}(V_b + V_c)\right]$$
$$V_\beta = \frac{2}{3}\cdot\frac{\sqrt{3}}{2}(V_b - V_c) = \frac{\sqrt{3}}{3}(V_b - V_c) \quad (A.8)$$
$$V_\gamma = \frac{1}{2}\cdot(V_a + V_b + V_c) = 0$$

From above equations, the phase angle ψ of $\vec{V}_{\alpha\beta}$ in α-β system can be easily found by the following equation:

$$\psi = \omega t + \vartheta_0 = \arctan\left(\frac{V_\beta}{V_\alpha}\right) \quad (A.9)$$

- **Transformation from α-β to d-q coordinate system**

This transformation is to convert vectors in balanced two-phase orthogonal stationary system mentioned above (α-β system) to an orthogonal reference frame (d-q system) rotating at the mains angular frequency, ω, as presented in fig. A.2.

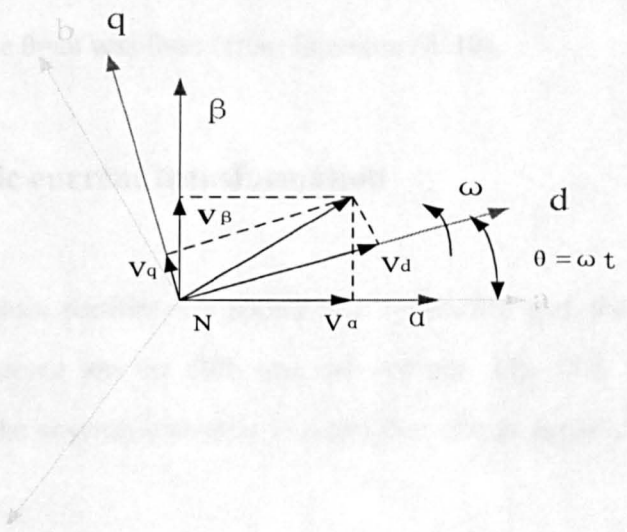

Figure A.1: Representation of voltage vector in different coordinate systems.

In this transformation the inputs are the direct axis (V_α), the quadrature axis (V_β) components of the voltage represented in α-β frame and the phase angle (θ) between the stationary and rotating frames. From Figure A.2it is possible to express the vector $\widehat{V_{dq}}$ as a function of $V_{\alpha\beta}$ as follows:

$$\widehat{V_{dq}} = \widehat{V_{\alpha\beta}} e^{-j\omega t} \tag{A.11}$$

Where:

$$\widehat{V_{dq}} = V_d + jV_q$$

$$\widehat{V_{\alpha\beta}} = V_\alpha + jV_\beta$$

$$e^{-j\omega t} = (\cos \omega t - j \sin \omega t)$$

Rearranging the Equation (A.11):

$$\begin{bmatrix} V_d \\ V_q \end{bmatrix} = \begin{bmatrix} \cos \omega t & \sin \omega t \\ -\sin \omega t & \cos \omega t \end{bmatrix} \begin{bmatrix} V_\alpha \\ V_\beta \end{bmatrix} \tag{A.12}$$

Where the angle θ=ωt was found from Equation (A.10).

- **Harmonic current transformation**

When a three-phase rectifier is supplied by a symmetric grid, the main current harmonics observed are the fifth and the seventh. The fifth is a negative sequence and the seventh harmonic is a positive one as Equation (A.13) and (A.14) shows

Fifth harmonic currents:

$$i_a = K_5 \cos(5\omega t)$$
$$i_b = K_5 \cos(5\omega t + 2\pi/3) \quad \text{(A.13)}$$
$$i_c = K_5 \cos(5\omega t - 2\pi/3)$$

Seventh harmonic currents:

$$i_a = K_7 \cos(7\omega t)$$
$$i_b = K_7 \cos(7\omega t - 2\pi/3) \quad \text{(A.14)}$$
$$i_c = K_7 \cos(7\omega t + 2\pi/3)$$

Where K_5 and K_7 are the magnitude of the fifth and seventh harmonic current respectively.

In the above condition, using the d-q reference frame transformation, synchronous with fundamental, the fifth and seventh harmonic currents both appear as sixth harmonic currents in the d-q frame of reference as the follows shows.

The fifth harmonic current:

$$i_{d5} = k[K_5 \cos(6\omega t)]$$
$$i_{q5} = k[-K_5 \sin(6\omega t)] \quad \text{(A.15)}$$

The seventh harmonic current:

$$i_{d7} = k[K_7 \cos(6\omega t)]$$
$$i_{q7} = k[-K_7 \sin(6\omega t)] \quad \text{(A.16)}$$

Where k is a constant that depends of the coefficient adopted in the transformation. The only difference between the two is the sign of q-axis current. Hence if the fundamental current component is considered as a positive sequence, the fifth and seventh harmonic currents are negative and positive sequence respectively. In general for a three phase controlled or uncontrolled front-end rectifier supplied by a symmetric set of grid voltages, harmonic currents are generated at orders: (6k±1) (k=1,2...) of the fundamental frequency. Table A.1 resume the above conclusion up to the ninetieth harmonic.

Harmonic in abc stationary frame	Sequence	Harmonic order in dq frame of reference Rotating at fundamental supply frequency
5	Negative	6 (Negative sequence)
7	Positive	6 (Positive sequence)
11	Negative	12 (Negative sequence)
13	Positive	12 (Positive sequence)
17	Negative	18 (Negative sequence)
19	Positive	18 (Positive sequence)

Table A.1: Harmonic sequences appeared in dq frame of reference

Appendix B

Bellman-Gronwall law

Assuming u(t) and v(t) are non-negative continuous equations, and there are non-negative constant values M, q to satisfies following equation,

$$u(t) \leq M(q + \int_0^t v(s)dx) + M\int_0^t u(s)ds \quad \text{(B.1)}$$

Then

$$u(t) \leq Mqe^{Mt} + M\int_0^t e^{M(t-s)}\, v(s)ds \quad \text{(B.2)}$$

Proof,

Since,

$$u(t) - M\int_0^t u(s)ds \leq M(q + \int_0^t v(s)ds)$$

Multiplying by e^{-Mt} both sides, one obtains,

$$(e^{-Mt}\int_0^t u(s)ds) \leq Mqe^{-Mt} + Me^{-Mt}\int_0^t v(s)ds) \quad \text{(B.3)}$$

Based on eq. (B.3), following equation can be obtained,

$$(e^{-Mt}\int_0^t u(s)ds)' \leq \int_0^t Mqe^{-Mt}\,d\tau + \int_0^t (Me^{-Mt}\int_0^t v(s)ds))\,d\tau \quad \text{(B.4)}$$

By changing the integration sequence of the second term in eq. (B.3), yields,

$$e^{-Mt}\int_0^t u(s)ds \leq q(1 - e^{-M\tau}) + \int_0^t (\int_s^t Me^{-Mt}\int_0^\tau v(s)d\tau)ds = q(1 -$$

$$e^{-M\tau}) + \int_0^t v(s)(e^{-Ms} - e^{-M\tau})ds \tag{B.5}$$

Thus,

$$\int_0^t u(s)ds \leq q(e^{Mt} - 1) + \int_0^t v(s)e^{M(t-s)ds} - \int_0^t v(s)ds.$$

$$q + \int_0^t v(s)ds + \int_0^t u(s)ds \leq qe^{Mt} + \int_0^t e^{M(t-s)}v(s)ds \tag{B.6}$$

By integrating eq, (B.6), eq. (B.2) can be obtained, the Bellman-Gronwall law has been proved.

Appendix C

Matlab Code for VSFSAF Implementation

- **Variable samples number per cycle**

```
function [sys,x0,str,ts]=mdlInitializeSizes

sizes = simsizes;

sizes.NumContStates  = 0;
sizes.NumDiscStates  =1;
sizes.NumOutputs     = 2;
sizes.NumInputs      = 1;
sizes.DirFeedthrough = 1;
sizes.NumSampleTimes = 1;

sys = simsizes(sizes);

x0  = 36;
str = [];
ts  = [-1 0]; % Inherited sample time


function sys = mdlUpdate(t,x,u)
    if u(1)*x(1)>16000
       sys(1,1)=x(1)-2;
    else sys(1,1)=x(1);       % reduce the samples number when
switching frequency reaches the upper limit
    end
    elseif u(1)*x(1)<14400
       sys(1,1)=x(1)+2;
    else sys(1,1)=x(1);      % increase the samples number when
switching frequency reaches the lower limit
    end


function sys = mdlOutputs(t,x,u)
   sys(1,1)=x(1);
   sys(2,1)=x(1)*u(1); % generate the samples number and switching
```

```
frequency to the simulink
```

● Switching signal generation

```
function [sys,x0,str,ts]=mdlInitializeSizes

sizes = simsizes;

sizes.NumContStates  = 0;
sizes.NumDiscStates  =2;
sizes.NumOutputs     = 1;
sizes.NumInputs      = 3;
sizes.DirFeedthrough = 1;
sizes.NumSampleTimes = 1;

sys = simsizes(sizes);

x0  = 0;
str = [];
ts  = [-1 0]; % Inherited sample time


function sys = mdlUpdate(t,x,u)
    if u(2)==1
       sys(1,1)=t;
       sys(2,1)=-1;
    elseif u(3)==1
       sys(1,1)=t;
       sys(2,1)=1;
    else sys(1,1)=x(1);
       sys(2,1)=x(2); % switches between the fallen and rising
edge
    end

function sys = mdlOutputs(t,x,u)
   sys=x(2)*(1-4*u(1)*(t-x(1))); % update the switching signal to
the simulink
```

● Discrete delays with linear interpolation

```
function [sys,x0,str,ts] = test1(t,x,u,flag)

switch flag,

  case 0,
   [sys,x0,str,ts]=mdlInitializeSizes;

  case 2,
    sys = mdlUpdate(t,x,u);

  case 3,
    sys = mdlOutputs(t,x,u);

  case 9,
    sys = [];

  otherwise
    error(['unhandled flag = ',num2str(flag)]);
end

function [sys,x0,str,ts]=mdlInitializeSizes

sizes = simsizes;

sizes.NumContStates  = 0;
sizes.NumDiscStates  =41;
sizes.NumOutputs     =1;
sizes.NumInputs      =2;
sizes.DirFeedthrough = 1;
sizes.NumSampleTimes = 1;

sys = simsizes(sizes);

x0  = 0;
str = [];
ts  = [-1 0]; % Inherited sample time


function sys = mdlUpdate(t,x,u,a)
```

```
    if x(41)==0
       sys(1,1)=u(2);
       sys(41,1)=u(1);
       a=1;
       while a<38,
           sys((a+1),1)=x(a);
           a=a+1;
       end
    elseif x(41)==u(1)
       sys(1,1)=u(2);
       sys(41,1)=u(1);
       a=1;
       while a<(u(1)-2),
           sys((a+1),1)=x(a);
           a=a+1;
       end
    elseif (x(41)~=0)&&(x(41)~=u(1))
       sys(1,1)=u(2);
       sys(41,1)=u(1);
       a=1;
       while a<(u(1)-2),
           b=a*(x(41)/u(1));
sys((a+1),1)=x(fix(b))+(b-fix(b))*(x(fix(b)+1)-x(fix(b)));
           a=a+1;
       end
    end

function sys = mdlOutputs(t,x,u)
   sys=x(u(1)-2);
```

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