The Control and Operation of the Five Level Diode Clamped Inverter

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Abstract

This thesis describes an investigation of three and five level diode clamped inverters for motor drive applications. The work was completed as a PhD project at the University of Nottingham with funding from EPSRC and Heenan Drives Ltd.

The investigation of the three level converter describes the design, development, control and operation of an 11kW prototype. Included in the design is a review of typical switching strategies employed for control of the output voltage. New improvements to the sub-harmonic pulse width modulation method are presented which allow an improved output waveform to be obtained. The problem of DC link capacitor voltage balancing (Neutral Point Control) is addressed and a novel balancing control method is presented based on the addition of a DC offset to the modulation pattern. This method is verified through mathematical analysis and experimental operation. The operational limits of the control are analysed. Improvements to the technique are presented to expand its operating limits.

The development of a prototype five level converter is then described. The design again features improvements to the sub-harmonic modulation strategy to provide enhanced output waveform generation, particularly for transient operation. The current demands on the DC link capacitors for the five level arrangement are analysed and it is concluded that the capacitors cannot be regulated by simple modifications to the output switching pattern.

A novel circuit is presented to achieve capacitor balancing within the DC link. The circuit behaviour is described and analysed. Operation is confirmed through simulation and experimental implementation. High dynamic performance is demonstrated via the use of a vector controlled induction motor. Neutral point control is successfully achieved through a similar method to that used for the three level inverter.

Having demonstrated the principle of operation of the three and five level inverters on low voltage prototypes, the thesis concludes with a review of the main considerations required to implement the configurations as medium voltage drives.

Acknowledgements

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Terms and Definitions

The following terms and definitions are used throughout this thesis.

Total Harmonic Distortion

$$THD = \frac{\sqrt{Waveform_{RMS}{}^2 - Fundamental_{RMS}{}^2}}{Fundamental_{RMS}}$$

Chapter 1

Introduction

Chapter Contents

1.1 Introduction

The history of electric machines is nearly as old as electricity itself. Once Faraday discovered how electricity and magnetism could be used to produce mechanical force the electrical machine became the most significant area of development in the industrial world. Supplies of electricity are almost completely generated via electrical machines, and other machines account for a significant percentage of the power used.

Electrical machines have always had one problem: speed control. The DC machine, given a particular supply voltage will rotate at a fixed speed. Adding resistors to the circuit to reduce the voltage reduces the motor speed, but at the expense of efficiency. Similarly, AC machines operated from a particular voltage and frequency will also rotate at a fixed speed.

In order to produce a variable speed motor drive the Ward-Leonard arrangement was commonly employed. This consists of three machines arranged as shown in figure 1.1. The first machine is an AC motor, either synchronous, or induction, which is driven direct from the main electric supply. This will run at a fixed speed, driving the rotor of a second machine. This machine is a DC generator. The field of this motor is controlled to regulate the output voltage used to feed the third machine. The third machine, also a DC machine, with a fixed field will operate at the speed set by its supply voltage and controlled by the field on the second machine.

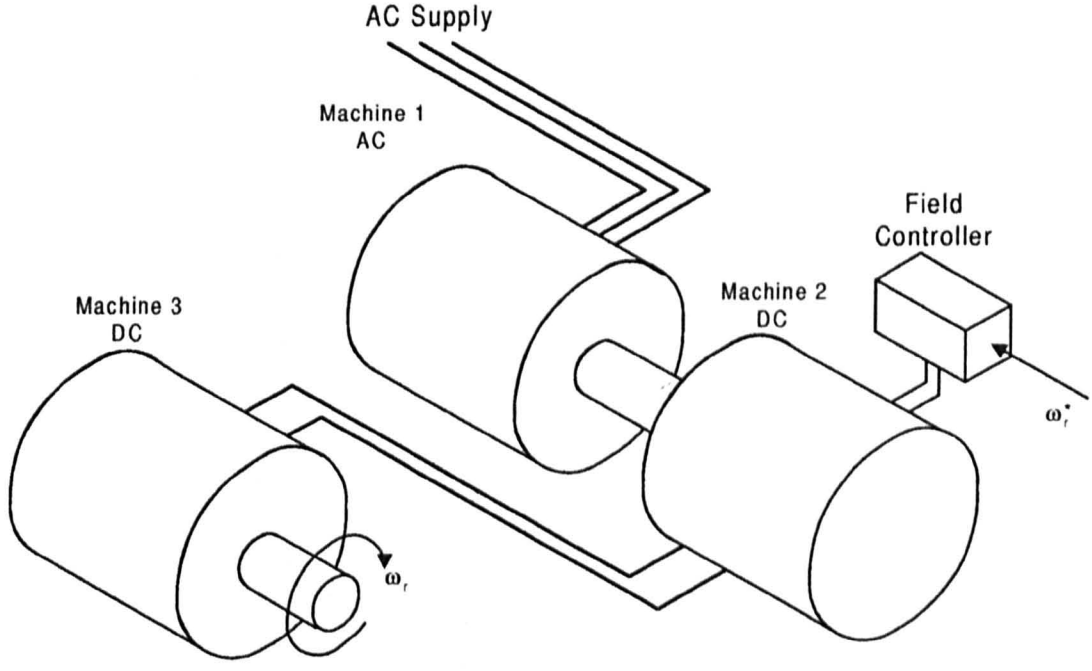

***Figure 1.1** : The Ward-Leonard arrangement*

The Ward-Leonard arrangement is reasonably efficient, and capable of operating in all four quadrants (motoring and generating in both speed directions). The use of three similarly rated machines to achieve variable speed requires a large amount of space, and is often noisy.

The development of electronics and semiconductor devices offered an alternate method of controlling motor speed. A circuit that would control the terminal voltage of the motor direct from a supply could allow the motor speed to be varied. The most significant step in motor control was the development of modern semiconductor switching devices. By switching the

voltage or current applied to the machine terminals, it is possible to directly control the speed and/or torque of the motor.

The development of the motor drive has seen a massive market expansion over the last twenty years. Motor drives cover a wide power range, from orders of watts for the speed controller in a CD player, to several megawatts for large industrial or transportation drives.

For the very low power end, single IC controllers provide all the functions required to control a small DC servomotor. In the low to medium power range (1 kW to 100 kW) the control and power separate. The supply is normally derived from the mains, with special power electronic devices capable of the voltage requirement. The control in this size of drive is becoming more and more complex, commonly utilising powerful microprocessor controllers. Motor control is now a major development on its own. Modern drives will commonly offer closed loop speed control without a requirement for a shaft encoder. At the very high power end of the market, the power electronics becomes very specialised to the particular application. Drives for this market cannot be bought 'off the shelf' as occurs at lower power levels. It is quite likely that the motor and drive will be supplied as an optimised system.

1.2 Low and Medium Power Motor Drives

There are a number of drive topologies that are commonly used for the low and medium power market. The DC motor drive market is gradually decreasing. At one time this was the only option if precise torque control was required. Developments in AC drive technology and high performance control allow an AC machine to be used in more and more of these applications. The low maintenance requirement of AC machines makes them the preferable choice provided the required performance is available.

1.2.1 DC Chopper

One of the simplest drive circuits is the DC H-Bridge chopper arrangement. This is illustrated in figure 1.2. A DC source is connected via power switches to the armature of the motor. By varying the timing of the switching, the mean voltage at the output can be defined. Since the speed of the machine is dependent on this voltage, control is achieved.

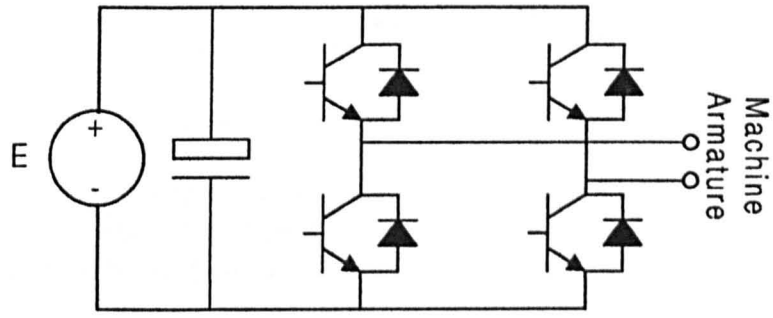

***Figure 1.2** : DC Chopper Circuit*

1.2.2 DC Controlled Rectifier

The basic chopper circuit is common for low power drives. Particularly those applications requiring accurate control such as servo drives. For higher power ranges it is usual to have a mains supply and a fully controlled thyristor bridge as shown in figure 1.3. When control is required in all for quadrants then a second anti-parallel bridge (thyristors connected in reverse polarity) can be employed.

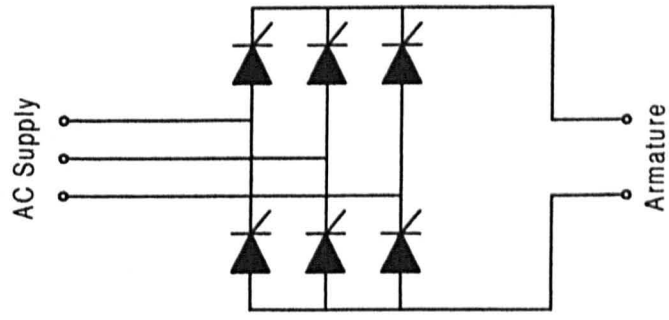

***Figure 1.3** : DC Controlled Thyristor Bridge*

The phase angle of the bridge is controlled to regulate the armature voltage. The voltage output to the armature is poor with this arrangement, but the armature inductance keeps the current, and torque, reasonably constant.

1.2.3 Conventional AC Inverter (2-Level)

The basic conventional inverter is an extension of the DC chopper circuit. Figure 1.4 shows the standard three phase example. In order to control the speed of an AC machine, both the voltage and the AC frequency must be determined. By controlling the switching of the devices, a fundamental alternating pattern can be generated at a lower frequency than the switching frequency. This process is termed pulse width modulation (PWM). The inductance of the machine filters out the majority of the switching to leave a fundamental current waveform that is sinusoidal and at the desired frequency.

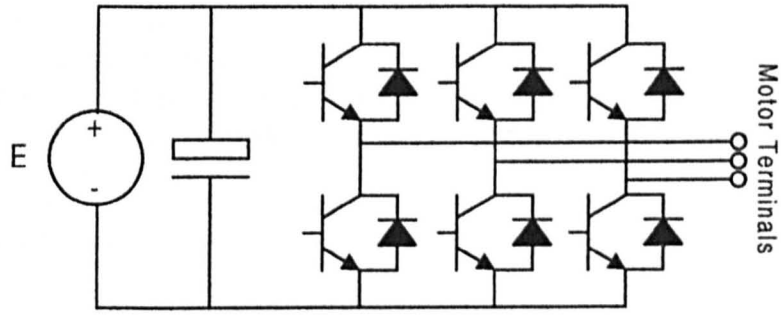

Figure 1.4 : *Conventional Inverter*

This arrangement has become one of the commonest drives, with numerous manufacturers offering competing products. These products cover the range of 1kW to 500kW, and suitable for a wide range of industrial applications (pumps, fans, lifts, small conveyors).

1.3 High Power Motor Drives

There are a number of high power motor drives currently available on the commercial market, and the range is expanding every year. Some are based on technology which has been around for a number of years, whilst others are leading research into new technology areas. Drives in this power range are used for large industrial units (mine winches, steel mills) and transportation (ship propulsion).

1.3.1 High Power Drives

The high power drive market is predominantly 1MW and upward. Machine design for these power ranges is frequently based on medium voltage supplies (3300V, 4160V) assuming direct connection. The limited voltage capability of many of the drive technologies has previously restricted the drive market. Recent developments in semiconductor technology, and the emergence of new topologies, has allowed the drive market to expand in this area. In this market the AC machine is often the preferred choice, due to inherent rugged construction and maintainability. The drives described in the following discussions assume an AC machine is used.

1.3.2 Current Source Drives

The basic diagram for a current source drive is shown in figure 1.5. The complete drive consists of a front-end supply converter, DC link choke to provide constant current and an output inverter bridge.

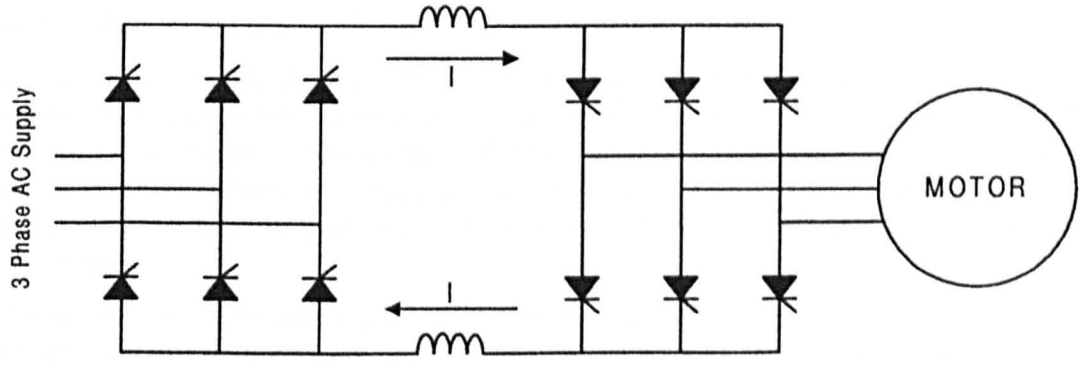

Figure 1.5 : *Generic Current Source Drive*

Depending on the type of machine the drive has to control (synchronous or induction), there are two different variations. The basic operating principle is the same for both variations. The front-end converter is a simple inductively smoothed three phase bridge. This provides constant current in the DC link choke. The output inverter chops the constant link current into the windings of the machine. The inverter is traditionally built with thyristor devices, which need commutation of the load current to allow the devices to turn-off.

With an induction motor load the bridge cannot commutate naturally, and additional circuitry is required in the output bridge to assist commutation. The altered output circuit is shown in figure 1.6. The commutation is dependent on the machine inductance and the additional capacitors. These have to be carefully matched to ensure commutation occurs. The drive design is therefore closely linked to the parameters of the motor being used. Knowledge of the motor shaft speed is required to maintain stable operation and additional force commutation circuits may be necessary to achieve operation over the full speed range.

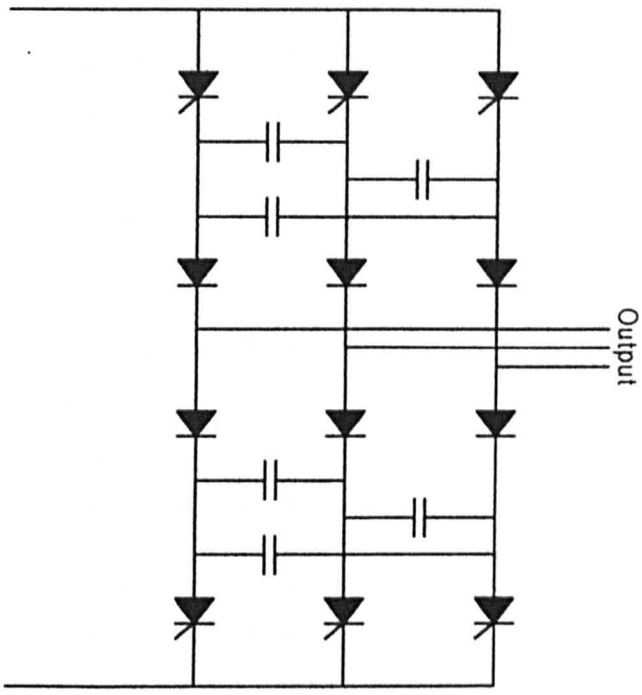

Figure 1.6 : *Current Source Inverter (CSI) for an induction motor*

With a synchronous motor the situation is slightly simplified. The back-emf of the motor provides a similar voltage pattern to that observed on the front end, and commutation will occur naturally. No additional circuitry is required, with the load naturally completing the commutation. This is commonly known as a load commutated inverter (LCI) [1].

The most significant disadvantage of this type of drive is the output phase current. The output will be quasi-squarewave, resulting in a significant level of torque ripple at the motor shaft. Voltage source inverters offering improved output currents have gradually reduced the market for current source drives. The high power capability of this type of drive has maintained its position in the market, though this is likely to diminish due to developments in other drive technologies.

This circuit does have one notable feature. Since the DC link is inductively smoothed to produce a constant current, the input bridge can be used in both the available quadrants (positive current with either positive or negative voltage). It is therefore possible to regenerate from the motor direct to the AC supply without additional circuitry being required.

1.3.3 Cycloconverter Drives

For high power, low frequency applications cycloconverters [1] have maintained their place in the market. The basic circuit for a three phase cycloconverter is shown in figure 1.7. A four quadrant thyristor bridge fed from an isolated supply generates each output phase.

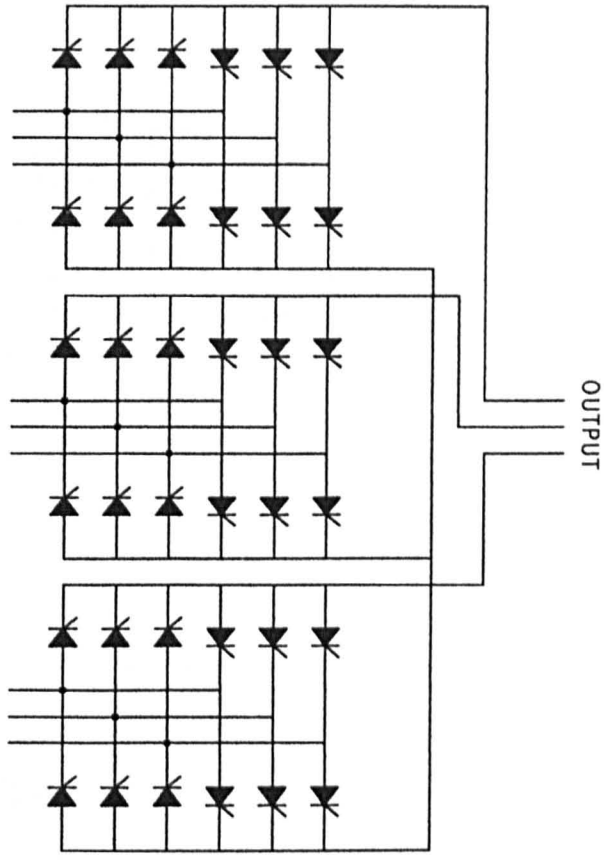

***Figure 1.7** : Cycloconverter*

Time varying the phase angle reference for each bridge allows a sinusoidal fundamental output to be generated. Figure 1.8 shows a typical output waveform for a single phase. The output frequency is limited to half the supply frequency to ensure commutation occurs.

The cycloconverter does not require DC link components, but does require isolation transformers on the input. Anti-parallel bridges are necessary to provide paths for reactive currents.

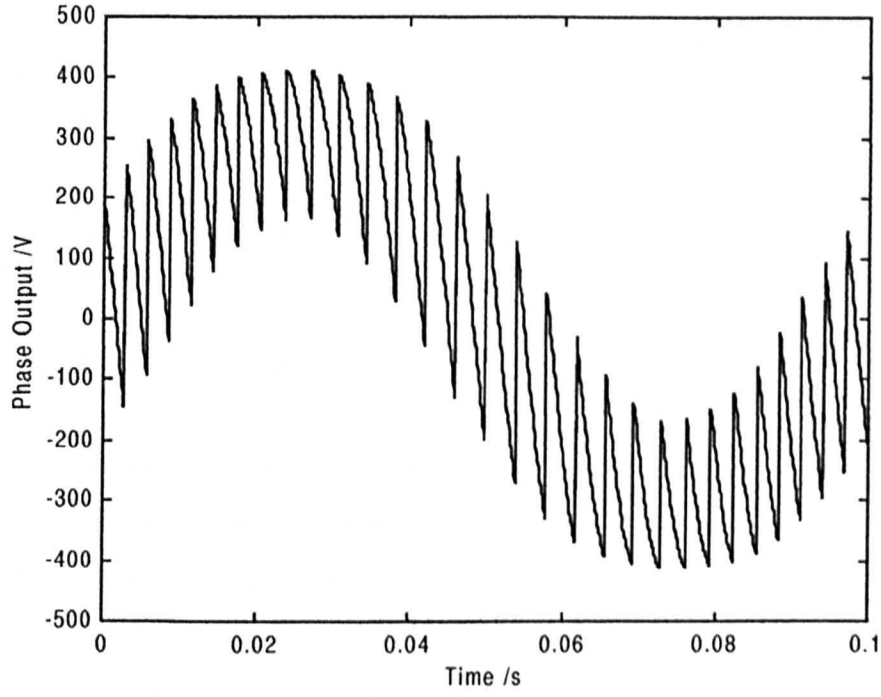

Figure 1.8 : *Cycloconverter phase output (ideal model)*

1.3.4 GTO Voltage Source Drives

The highest power conventional structure voltage source inverters are GTO based. These drives offer voltages above standard levels, into lower end of the medium voltage range, and with quite substantial current capability. Power ratings for these drives are still lower than is obtainable with current source and cycloconverters.

Snubber requirements, high gate drive loading and limited switching frequency are significant disadvantages to the use of GTOs, and the market is beginning to decrease with the expansion of IGBT device operating capabilities. This will be described further in chapter 6.

1.3.5 Multi-Level Drives

Over recent years the multi-level inverter has received increasingly more interest. A medium voltage drive can be constructed using series connection of devices without the need for simultaneous series switching. The focus of this project was to investigate the design and operation of multi-level inverters and therefore this class of drive will be described more thoroughly in subsequent chapters.

1.4 Project Motivation and Aims

The work described in the following chapters was completed as part of a PhD course at the University of Nottingham. The Engineering and Physical Sciences Research Council (EPSRC) funded this work, with industrial sponsorship via the CASE scheme from Heenan Drives Ltd.

The overall aim of the project as defined at the start of the three years was to investigate the operation of a five level diode clamped inverter. This was chosen in consultation with the industrial sponsor, who expressed an interest in the circuit as a possible area for expansion of their product range.

The major defined objectives are listed below.

- Develop an understanding of diode clamped multi-level inverter circuits
- Construct a three level prototype inverter
- Implement improved PWM on the inverter
- Develop and implement novel neutral point control
- Confirm correct operation of the prototype inverter
- Construct a five level prototype inverter
- Develop improved PWM strategy for the five level inverter
- Demonstrate operation with transformer supplied DC link levels
- Develop and implement high performance inverter control
- Develop and implement new capacitor balancing arrangement
- Demonstrate correct operation of a full five level inverter drive system

1.5 Thesis Layout

This thesis is laid out in the following structure.

Chapter one introduces the area of drives and sets out the project background.

Chapter two describes the different multi-level topologies, and general switching strategies.

Chapter three describes the construction and operation of a prototype three level inverter. Pulse width modulation and neutral point control are specifically addressed.

Chapter four describes the construction and basic operation of a prototype five level inverter. The expansion of the PWM structure for the increased number of levels is addressed.

Chapter five expands on chapter four, describing the implementation of high performance motor control and capacitor balancing on the five level inverter.

Chapter six introduces some of the issues that need to be considered in the design of a multi-level, medium voltage inverter.

Chapter seven describes the conclusions from the work.

Appendix one describes the design and construction of the control boards, and introduces the software methodology.

Appendix two details simulation and analysis work referenced within the main chapters.

Appendix three provides additional reference information.

1.6 Chapter References

[1] S. B. Dewan, G. R. Slemon, A. Straughen, "Power Semiconductor Drives", J. Wiley & Sons, 1984

Chapter 2

The Multi-Level Inverter - Topologies and General Operation

Chapter Contents

2.1 Introduction

Since the early 1980s, there has been considerable development on several new topologies for the generation of variable frequency AC through the use of modern power electronics. The conventional voltage and current source inverters have their limitations, as does the cycloconverter (discussed in chapter 1). The current waveform they generate on the load machine is often quite poor, producing significant levels of torque ripple. Given the switching limitations of the early power semiconductors, the only way to improve the operation was through changes to the inverter circuit. Various new topologies were designed which provided several benefits over the conventional arrangement. One group of these circuits became known as Multi-Level Inverters.

This chapter will start with a description of a generalised multi-level inverter. This will provide a common reference to describe the benefits obtained from this group of circuits. The three main circuit topologies under consideration, namely the H-Bridge, the flying capacitor and the diode clamped configurations will then be individually described in sections 2.3, 2.4, 2.5 respectively. Each topology has its own particular advantages and disadvantages. These will be discussed from a practical perspective.

The new circuit topologies required the development of new switching strategies, and a review is made of the common techniques. The descriptions of these in section 2.6 are focussed on the generalised structure, since the techniques are applicable to all the different circuit arrangements.

2.2 A Generalised Multi-Level Inverter

The first multi-level inverter topologies were suggested around 1980. At this time, the thyristor was the dominant power switching device, and the conventional two level inverter circuits produced poor quality output waveforms onto the machine due to the low frequency switching imposed by forced commutation. The harmonics associated with the switching increased the losses in the machine, and generated excessive torque ripple. It was not until the subsequent development of faster switching devices, and advanced PWM strategies, that the performance of the conventional voltage source inverter could be improved. As a solution to improving the output quality of thyristor drives, Nabae et al. [1] proposed one of the first multi-level topologies. The new circuit allowed a number of fixed voltage sources to be connected in series combinations at the output. This allowed an output pattern to be generated which contained a number of voltage steps, or levels. The circuits were named according to the number of voltages each individual phase could generate.

Figure 2.1 shows the circuit of a generalised multi-level inverter. The output can be connected to n different levels, formed from n-1 voltage sources. Typical output patterns are shown in figures 2.2 and 2.3. These two figures show the phase to neutral output of a three level and five level inverter. Several different circuits have been suggested which produce a similar stepped pattern at the output, and provide similar benefits. Because of the different techniques these circuits use to produce the pattern however, each circuit also has its own particular advantages and disadvantages.

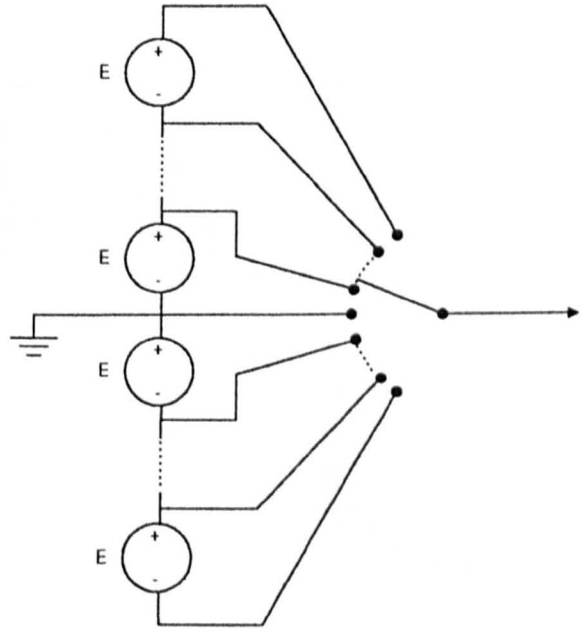

Figure 2.1: *The Generalised n-Level Converter*

Whilst the naming convention defines the number of levels in the phase voltage with respect to neutral, the phase to phase voltage will contain 2n-1 levels. For example, a three level inverter produces three output voltages in a particular phase (+E, 0, -E). The phase to phase voltage can therefore contain up to five levels (+2E, +E, 0, -E, -2E).

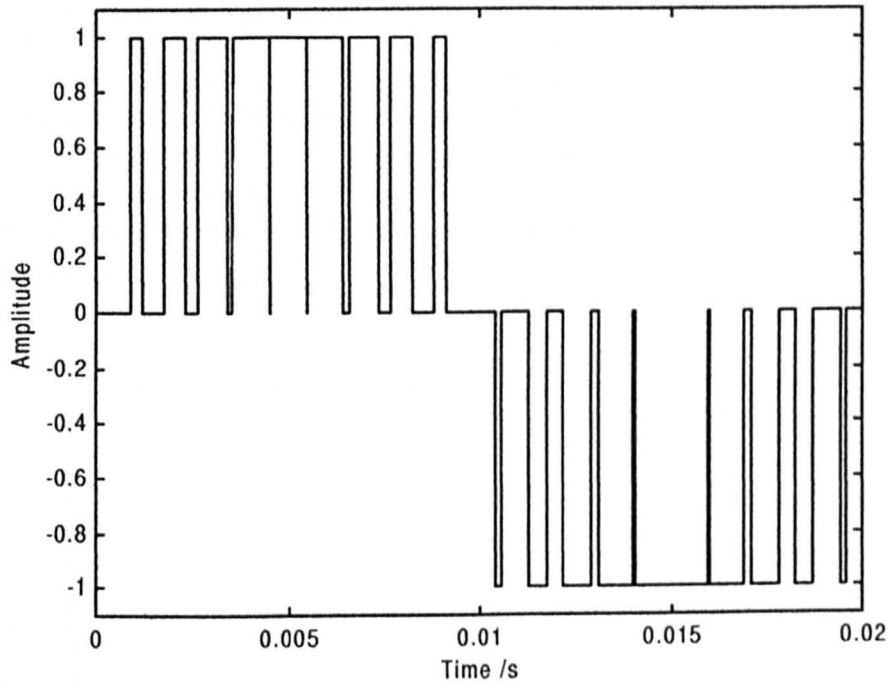

Figure 2.2: *Example Three Level Phase Output Waveform*

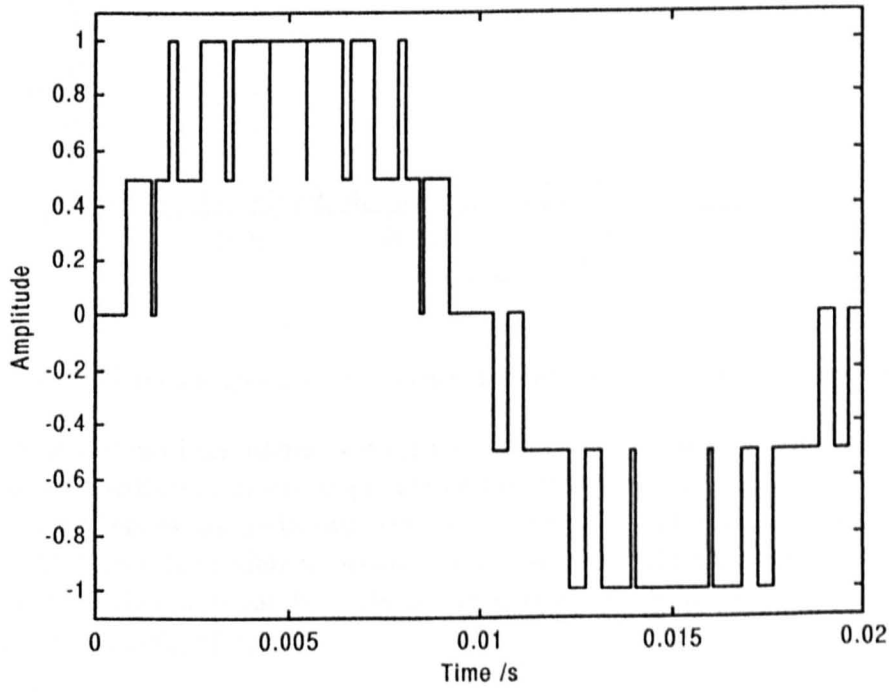

Figure 2.3: *Example Five Level Phase Output Waveform*

2.2.1 Advantages of the generalised multi-level inverter

The multi-level inverter has several advantages over conventional two level inverters. The principal advantage, the improved harmonic content, was the original impetus for the

development of these topologies. Looking at the five level waveform that was shown in figure 2.3, the sinusoidal variation is clearly visible in the pattern. The magnitude of the harmonics has been reduced, along with the associated losses and torque ripple. Simulating an ideal naturally sampled PWM strategy for a conventional inverter and a five level inverter (generation of multi-level PWM will be discussed later in the chapter) produces the harmonic spectra shown in figure 2.4. Both simulations are producing 50 Hz full modulation output from a 1kHz carrier frequency. The line to line voltage has been used so that the spectra accurately demonstrate what would occur in practice. As the simulation is ideal, there are no restrictions on the pulse width.

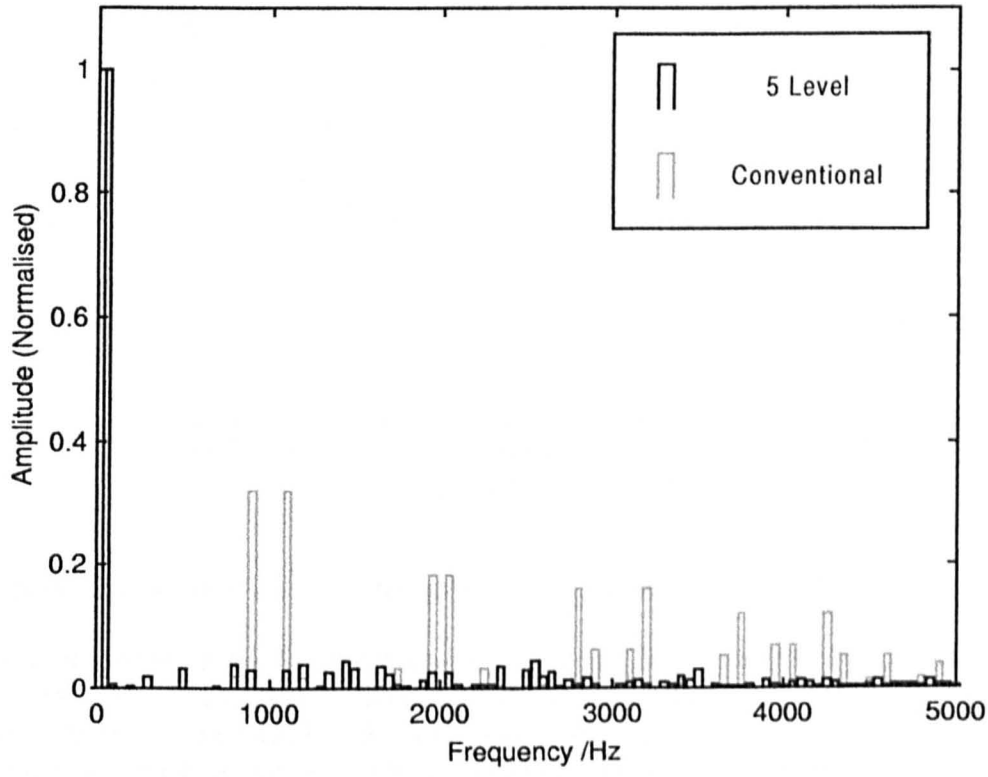

Figure 2.4 : *Harmonic spectra for two level and five level line to line voltage waveforms*

The fundamental has been normalised for the two spectra to aid the comparison. It is clear that there is a reduction in the amplitude of the switching harmonics for the multi-level inverter. If the line to line switching patterns are applied to an RL load model, defined by equation 2.1, then it is possible to obtain an estimate of the total harmonic distortion (THD) in the current. This ratio has been chosen as it is similar to the parameters of a typical induction machine (R_s, σL_s).

$$\frac{i(s)}{v(s)} = \frac{1000}{s+1000} \qquad [2.1]$$

Figure 2.5 shows plots of the current THD against switching frequency for a conventional two level, three level, and a five level inverter. The decreased THD for the multi-level inverters is clearly visible throughout the frequency range. The THD for the five level

inverter is approximately equivalent to that of a conventional inverter operating with four times the switching frequency.

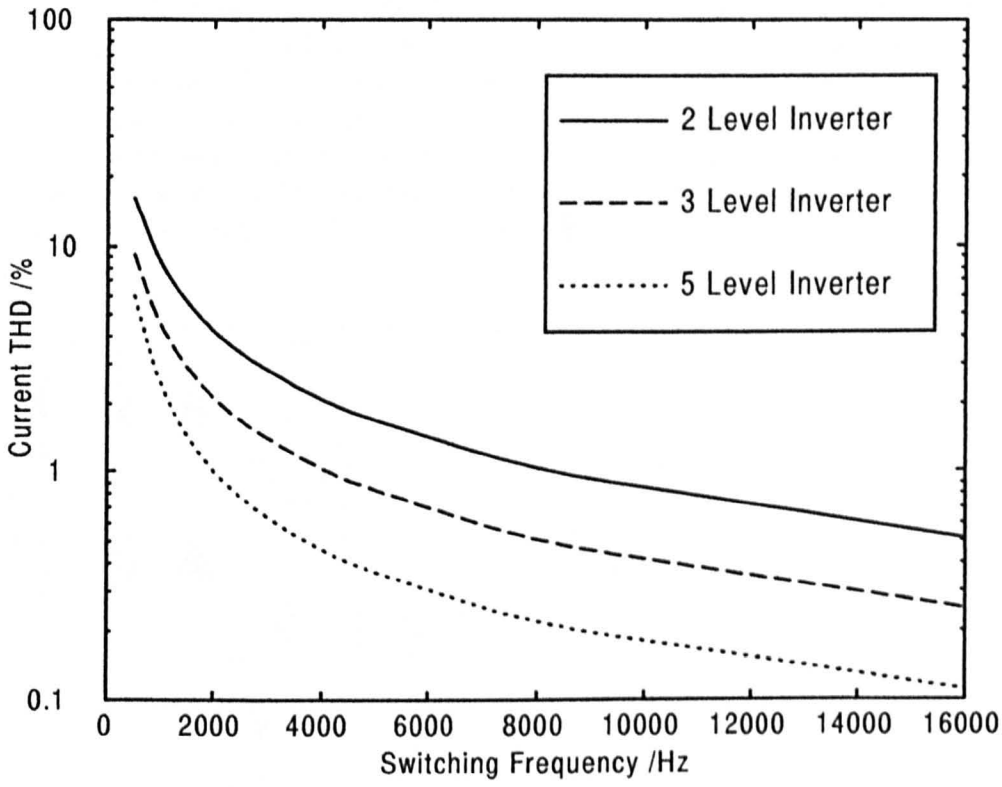

***Figure 2.5** : Graph of current THD against switching frequency for different converters*

The second advantage, and the recent driving force in the development of these topologies, is the increase in voltage capability. Each step in the output waveform is generated by switching a pair of devices in the circuit. If the devices are operating at their full safe operating limit, then the total operating voltage will be multiplied by the number of steps in the output (n-1 steps for an n level inverter). For example, a five level converter, using devices capable of blocking E volts will have a total voltage capability of 4E.

2.3 The Isolated "H Bridge" Structure

The simplest method of producing a multi-level waveform, is by the series connection of several isolated "H-bridge" chopper units or cells. Figure 2.6 shows an example of this type of circuit, in this case a five level, three phase inverter. Each cell contains a rectifier, capacitor bank, and a 'H-bridge' chopper. The H-bridge has four possible switching states, which produce three different output voltages (+E, 0, -E). When the outputs are added along the series chain of cells, the typical multi-level output is produced (i.e. with two cells in series then phase output voltages can be varied from +2E to -2E in four steps as the state of each cell is changed). The base potential of each cell is dependent on the switching states of the other cells in that particular phase. Because of this the supply to each cell has to be isolated.

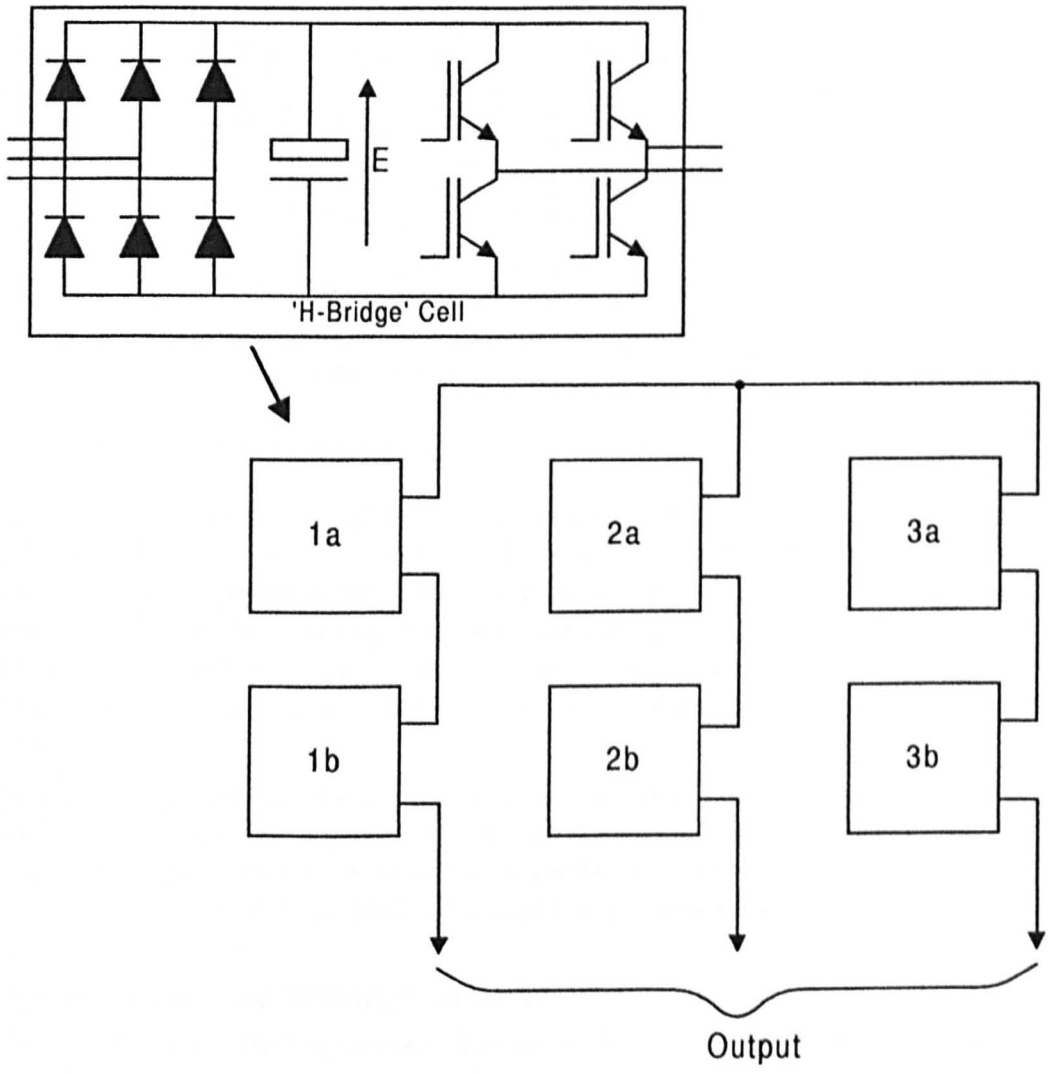

Figure 2.6 : *The isolated "H Bridge" inverter*

2.3.1 Operation of the "H-Bridge" structure

Each cell has four possible switch combinations. The resulting output will be either +E, -E, or zero (a zero output occurs from two switch combinations). When the polarity of the output voltage is the same as the phase current direction, then energy is drawn from DC link of the

cell. If the voltage and current are in opposing directions however, then energy is returned to the DC link. Reactive current drawn by the AC load will not circulate between phases as occurs in a conventional inverter circuit, since there is no conduction path between the cells. The energy associated with the reactive current appears as a power pulsation in the conducting cells. This is a particular problem when the circuit is used for static VAr compensation [3]. The size of the capacitor bank may have to be substantially increased to compensate for this.

Examining the operation of the whole phase there is some redundancy in the switching states in order to generate a particular output voltage. An example of this redundancy is shown in figure 2.7. There are six different state combinations that will produce an output of +E on a seven level inverter.

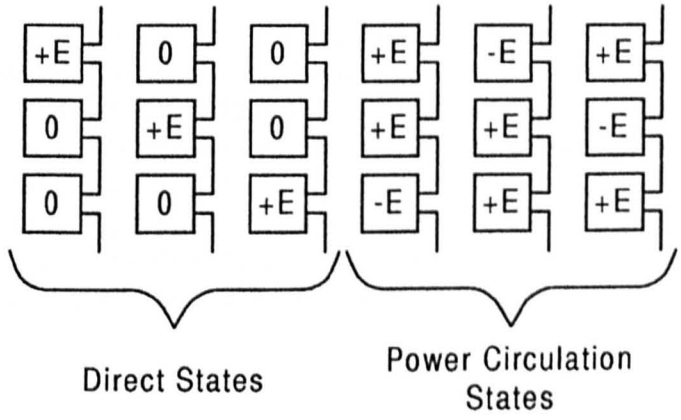

Figure 2.7 : *State redundancy for a phase output of +E on a seven level inverter*

The redundant states can be split into two categories, the "direct states" where energy is transferred directly from the cells to the load, and the "power circulation states" where energy is circulated between the cells as well as to the load. It is possible to utilise these redundant states in the switching strategy to share the power flow between the cells. This balances the losses between cells (reducing cyclic load stressing) and provides a method to redistribute any excess energy stored in the cell capacitor bank due to reactive power pulsation.

The control requirements for this topology are actually quite simple. The basic PWM strategies (described later in this chapter) can be directly applied without any specific modifications. Improvements to the operation can be achieved by selection of the redundant states as mentioned above, but this is not a requirement for basic operation.

2.3.2 Advantages of the "H Bridge" structure

This topology has several advantages. The circuit is made up of identical cell units. This simplifies the manufacturing for commercial production. The individual cell has a single standard voltage rating for all the semiconductor devices. The overall voltage rating is the product of the individual cell rating and the number of series cells. Potentially any voltage can be achieved, provided the cell isolation can be maintained for both the link power supply, and the control signals. One solution for the isolated supplies is a transformer with multiple secondary windings [2]. Each cell has a three phase input via a six pulse diode bridge. By phase shifting the different cell windings the current loading is spread through the cycle. The input current distortion factor is greatly improved, with values near unity attainable.

2.3.3 Disadvantages of the "H Bridge" structure

There are two main disadvantages to the structure. If a transformer is used to power the cells, then it becomes large and complex (the design of the transformer to achieve the correct phase shifting is not trivial). The second disadvantage is the circuit behaviour when supplying reactive power. When used for motor drive applications, there is always a reactive component drawn to magnetise the machine. When used for static VAR compensation, the reactive component is dominant, and the capacitor bank will have to be suitably large to avoid excessive voltage fluctuations. In the worst case condition, power drawn from the supply to feed the reactive current in one cell, will have to be discarded into a resistor to avoid over voltage in a different cell.

2.3.4 Discussion

This type of inverter has received interest for various applications. It is currently in commercial production in the motor drive industry, where a transformer is used to provide the multiple supplies to the cells [2]. With sufficient isolation between the cells, the final output voltage can be taken far beyond any of the conventional techniques, which has promoted interest in its use for power factor correction in HV grid systems [3]. Here the problems of obtaining the isolated supply become less significant since no real power transfer occurs. Other areas of interest have included satellite AC generation, where the isolated supplies can be obtained naturally from the solar cells [4], and AC rectification for electric trains [5].

2.4 The Flying Capacitor Structure

The second topology to be considered here is commonly known as the flying capacitor circuit. This consists of a series string of IGBTs, with connections to an arrangement of isolated charged capacitors that are used to provide the levels. One phase of a five level flying capacitor circuit is shown in figure 2.8.

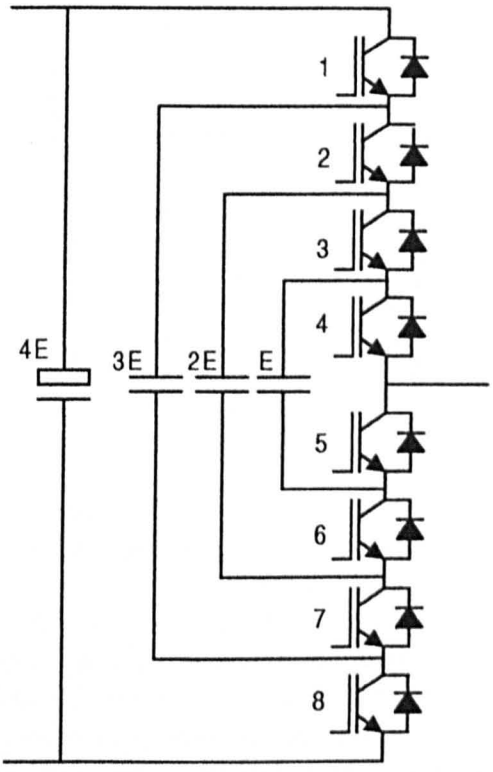

***Figure 2.8** : The Flying Capacitor Circuit*

With the main DC link capacitor bank charged to 4E, each separate phase requires additional capacitor banks charged to 3E, 2E, and E. The devices are switched in complementary pairs (1-8, 2-7, 3-6, 4-5). The load current is passed through the isolated capacitors back to the DC link. The resulting output voltage will then be the sum of the appropriate capacitor voltages. As the devices are switched the base potential of the isolated capacitors associated with the phase will change. It is from this behaviour that the name of 'the flying capacitor' is derived.

2.4.1 Operation of the flying capacitor circuit

An example conduction path is shown in figure 2.9. In this case, devices 1, 5, 6 and 7 are turned on, with the paired devices turned off. The current will flow along the same path independent of the current direction (using either the switching device or the associated anti-parallel diode). Assuming the DC link is split around an effective neutral point, then from the top of the link at +2E the current flows back through the isolated capacitor, which is pre-charged, to 3E. The resulting output voltage is then –E with respect to the neutral point. During conduction, the isolated capacitor will either charge or discharge (depending on the current direction) and deviate from the original potential. For correct operation, the voltages on the isolated capacitors have to be maintained, so the average mean current through each capacitor must be zero (in the ideal case).

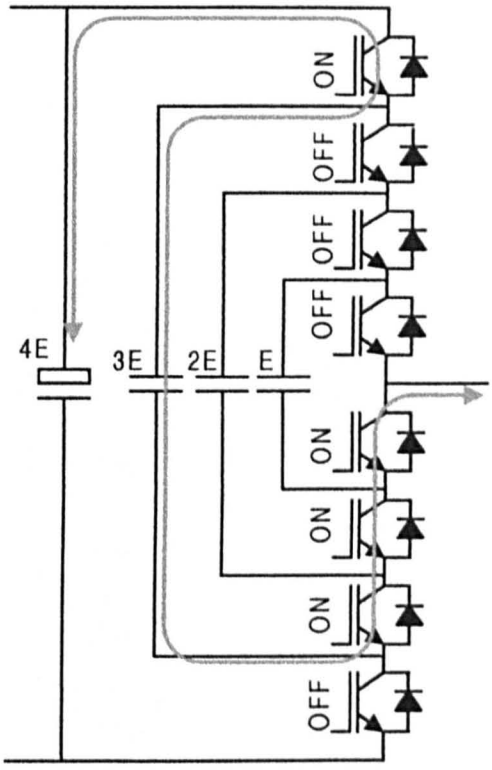

Figure 2.9 : *Example conduction path for the Flying Capacitor Circuit*

As with the isolated H-bridge, there is some redundancy in the switching states. There is more than one combination of current paths that will produce the same output voltage. For the previous example, there are two other switch combinations that will produce the same output voltage. These switch combinations are shown in figure 2.10. The different combinations change the current path through the isolated capacitors. In the two alternative states shown below it can be seen that current passes through the last capacitor (charged to E). The current direction through this capacitor differs between these two combinations. Choice between these states allows the charging of the capacitor to be controlled. Unfortunately for the other capacitors the current path cannot be reversed by the switching state, and the direction of the load current becomes the controlling condition. Certain PWM strategies also include redundant states that produce the same effective voltage at the output. Different switching strategies will be discussed later in the chapter. These states may allow further control of the capacitor voltages. The worst condition for this inverter is low frequency, high current, where the capacitors may have to provide energy for long periods before the current direction reverses, and the capacitors can be returned to their original condition.

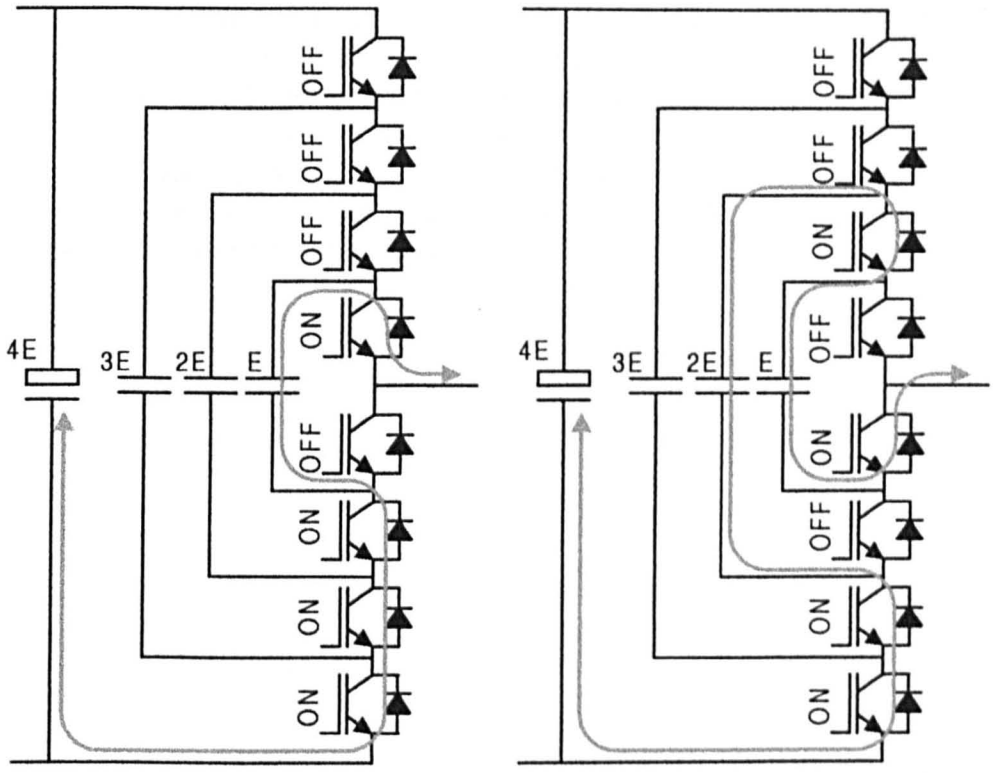

Figure 2.10 : *Examples of Alternative Conduction Paths*

2.4.2 Advantages of the flying capacitor circuit

The flying capacitor circuit provides a solution that does not need the addition of extra silicon (which will be seen later for the diode clamped circuit), but which can still offer true three phase operation. The circuit is built around one main capacitor bank that allows cancellation of the reactive current between the phases. All the devices are equally rated, and the voltages on the capacitors ensure that the sharing is correctly maintained.

2.4.3 Disadvantages of the flying capacitor circuit

The main disadvantage of the circuit is the variation of the capacitor voltages. The output waveform shape is dependent on these capacitors maintaining their defined voltages. The control implementation must include some form of feedback and closed loop regulation of the voltages. This compares to the other circuits that can operate from the basic switching strategy. Another problem that can occur is the pre-charge of the isolated capacitors. When the supply is initially applied, the main capacitor bank will charge to the full link voltage, the isolated capacitors have no path to charge through, so they will remain uncharged. This will result in an over-voltage on the outer devices. Some form of charging strategy has to be implemented to get the inverter into its start condition. The capacitor banks that are associated with each phase are often large (having to supply current for long periods without significant variation in voltage). The physical design of the phase then becomes more complex if the stray inductance is to be kept small (otherwise resonance can occur).

2.4.4 Discussion

Little research has been done on this topology, with most people taking the view that the control of the capacitor voltages through the switching strategy is too complex to be achieved

on line without excessive computational power [6]. It has been proposed by [7] that the switching pattern can be predetermined whilst still maintaining the correct voltages on the capacitors. After originally being discussed for motor drive applications though with results from a simple RL load, a more recent publication by the authors has seen a change of application to sinusoidal rectification [8]. This slightly simplifies the control since the frequency becomes fixed, and the capacitors will only have to supply current for a predetermined interval before the direction reverses.

2.5 The Diode Clamped Structure

The third multi-level circuit is the diode clamped structure. This topology closely resembles the generalised circuit shown in figure 2.1. This is the structure that has been investigated in this project, so the description that is given in this section will be limited. More specific details will be presented in subsequent chapters. Figure 2.11 and 2.12 show examples of a three level and a five level inverter phase.

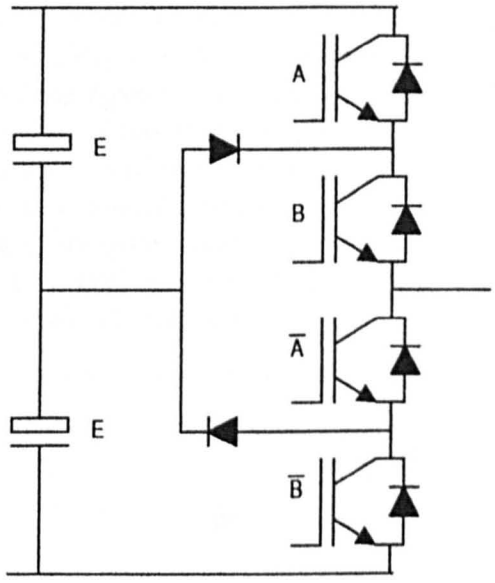

Figure 2.11 : *Three level diode clamped inverter phase*

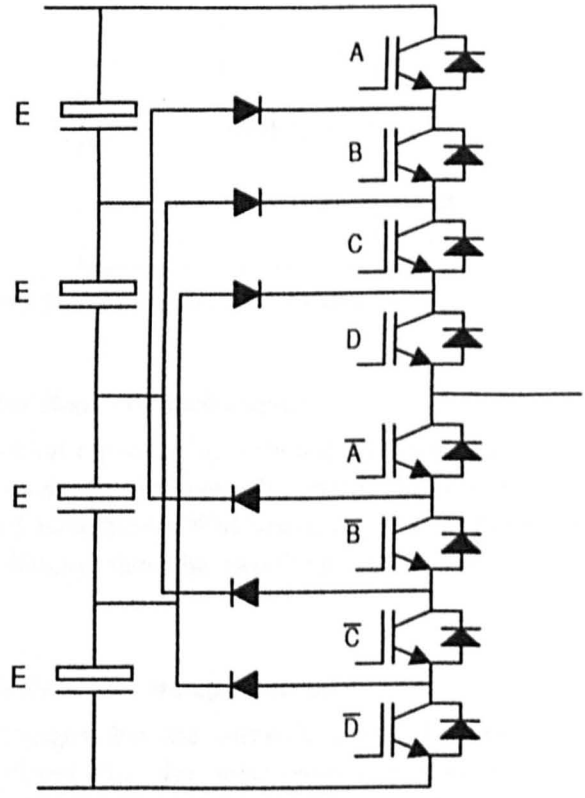

Figure 2.12 : *Five level diode clamped inverter phase*

The circuits consist of a series of IGBTs with additional diodes that provide current paths back to a split capacitor bank. Each of the capacitors are equally charged to E volts. It is these splits in the capacitor bank which provide the defined levels. By switching the load current through the particular diode paths, the general output voltage pattern can be produced.

2.5.1 Operation of the diode clamped circuit

The devices are switched in complementary pairs to direct the current either directly to the top and bottom levels, or through the additional diodes to the split capacitor bank. Figure 2.13 shows an example switching state for a three level diode clamped inverter. There are two possible current paths that depend on the current direction. These are highlighted in the figure. It is one of the features of this structure that the current paths can be quite different when the direction reverses. In this switch state, the output is connected to the effective midpoint in the link, or what is generally referred to as the 'Neutral Point'. The similarity can be quite easily seen back to the generalised circuit given earlier. Since the voltages on the various capacitors in the link define the levels, then for correct operation, the capacitors need to maintain these voltages under all conditions.

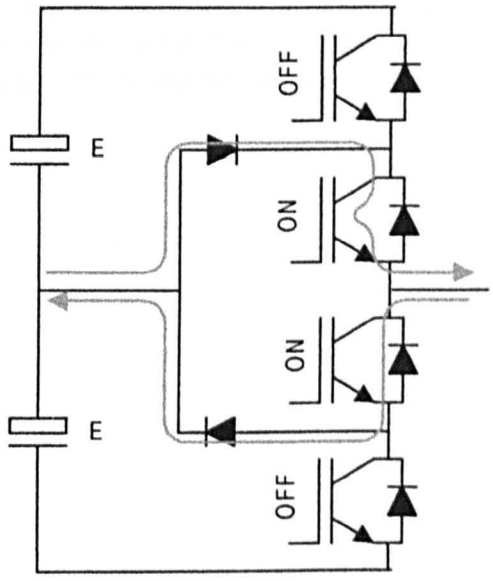

Figure 2.13 : *Example current paths in a three level inverter*

2.5.2 Advantages of the diode clamped circuit

The circuit uses one central capacitor bank for a three phase system. This allows the reactive current components to circulate between the phases. Similar to the isolated H-bridge the circuit can be controlled using basic PWM strategies. If the capacitors are fed from individual supplies to fix their voltages, then the switching pattern only needs to control the output waveform.

2.5.3 Disadvantages of the diode clamped circuit

There are two disadvantages that are normally quoted for this topology. The first is the voltage rating requirement for the interconnecting diodes. Examining the blocking conditions, then whilst the switching devices have to block 1/n-1 of the total link (for an n level inverter) then the maximum diode capability is n-2/n-1 of the total link voltage. Thus

for a five level inverter where the switches block one quarter of the link voltage, some of the interconnection diodes have to block voltages up to three quarters of the total link.

If the capacitors are not individually supplied, then equal voltage sharing is no longer guaranteed. Assuming one single supply is used to feed the total DC link, then current drawn from the intermediary nodes will have to pass through the capacitors. This will cause some of the capacitors to charge and some to discharge, producing unequal voltages. In order to achieve operation from a single supply this current must be cancelled so that the capacitors remain equally charged. As the number of levels increases, balancing the capacitor voltages becomes more and more complex.

2.5.4 Discussion

Despite the disadvantages, this circuit has seen more interest than any other topology for multi-level applications. Much work has been done on the basic three level circuit, or 'neutral point clamped inverter'. This circuit has the advantage of using interconnection diodes that match the devices for voltage rating. The balancing of the capacitors is also relatively simple, and several papers have been published specifically on this subject [9][10]. Some interest is now being shown to the five level inverter [11]. The balancing of the capacitors for real power applications requires more consideration, and the diode blocking voltage need to be addressed. These difficulties will be addressed in later chapters.

2.6 Switching Strategies for Multi-Level Inverters

The different circuit topologies all obey the rules set down for the generalised multi-level inverter. Since they all produce the same output pattern, they share the same basic switching techniques.

Various switching strategies have been suggested for multi-level converters. These have varied in complexity as the switching speed of the devices has improved. The early circuits often used fundamental switching, generating simple staircase patterns. As the switching frequency increased with the improvements in semiconductor technology, then there was a change to pulse width modulated (PWM) techniques, and the typical output began to resemble the examples shown earlier in figures 2.2 and 2.3.

Each step in the output pattern of a phase is generated by switching a complementary pair of devices in the circuit. This applies to all three topologies. By limiting the change to being a step between adjacent levels (one level up or down) the series devices are not switched simultaneously, reducing the requirement for dynamic snubbering. This is a common rule of operation for all the circuit topologies.

2.6.1 Fundamental switched modulation

Fundamental switching offers the simplest pattern, and similar to the quasi-squarewave pattern from the early conventional inverters, the harmonics are linked to the fundamental. This produces large low order harmonics (significantly 7^{th} and 11^{th}, the triple harmonics cancel between phases) due to the switching. The amplitude of these is dependent on the number of levels in the pattern that is generated. During early work on the multi-level, when the switching speed of the devices was limited, this was a common technique.

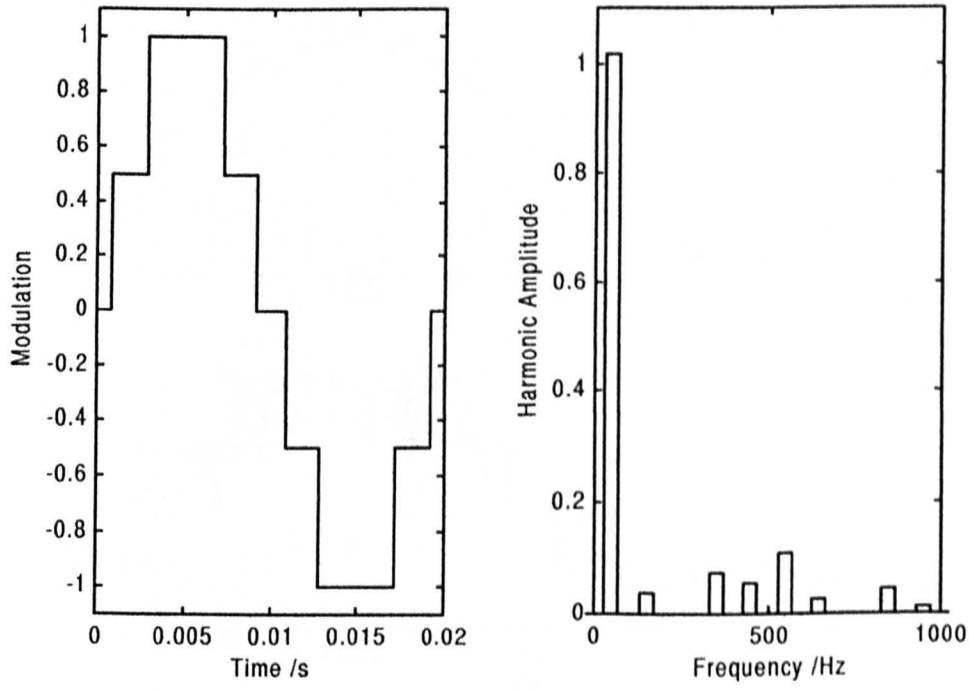

Figure 2.14 : *An example of fundamental switching with spectra*

Figure 2.14 shows an example output waveform from a five level inverter operating at 50 Hz. The fundamental shape can be clearly seen. Harmonic analysis of this waveform produces a

relatively simple spectrum. The total harmonic distortion is quite low at 18.4 %, which would suggest a good current waveform, and at this frequency this is the case. As the amplitude decreases then the number of levels used is decreased, and some of the advantage is lost. The level of harmonic distortion then increases as the low order harmonics (5^{th}, 7^{th}, 11^{th} etc) become more significant.

If the multi-level inverter is being used for sinusoidal rectification, then the output is normally near full modulation, and the frequency will be defined by the supply (be it 50 or 60 Hz). In this case, fundamental switching may well be sufficient for the application. For motor drive applications however, the output must be capable of a wide frequency operating range (down to fractions of a hertz). Due to the voltage/frequency relationship of the machine, the low frequency is combined with low amplitude, which is the worst operating condition for fundamental switching, and this leads to large distortions in the current waveform. The normal solution was to use pulse width modulation in the lower frequency range.

2.6.2 Sub-harmonic PWM

As power electronics developed, it became possible to operate at higher switching frequencies, and the use of Pulse Width Modulation became standard. Appearing first for the conventional inverter, the techniques were soon adapted for the multi-level circuits. The basic technique is often referred to as 'sub-harmonic PWM'. For a conventional inverter, this is generated by comparing a triangle wave carrier at the switching frequency, with a lower frequency modulation wave [12]. For the multi-level, the technique is expanded by having multiple carriers that form a contiguous set. The crossing of the modulation wave with the different carriers defines the switching for the various levels [13]. An example is shown in figure 2.15

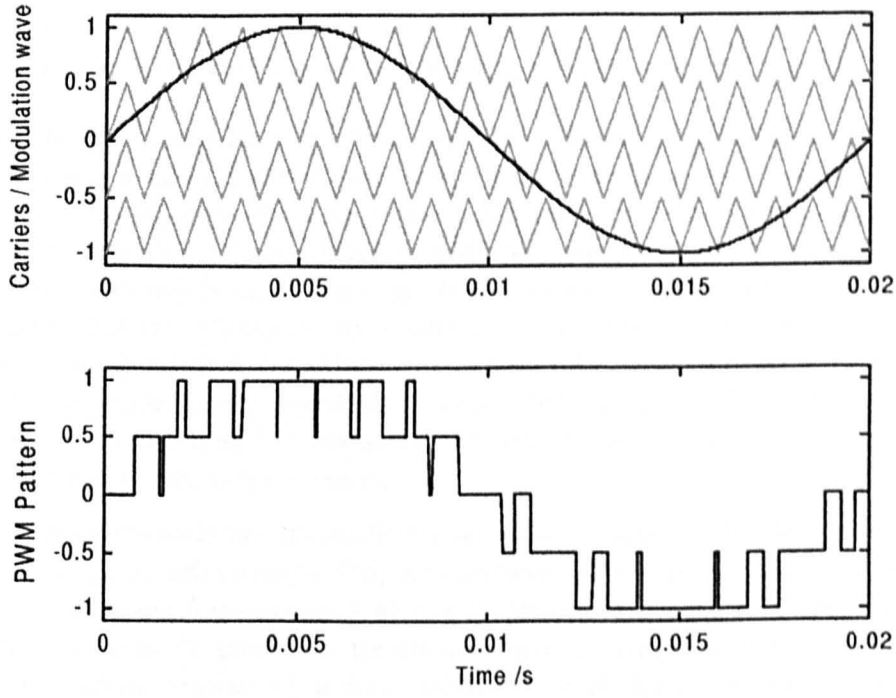

Figure 2.15 : *PWM generation via the Sub-Harmonic method*

The example represents the full modulation condition at 50 Hz. There are four carriers to define five levels, which are all in phase. This does not have to be the case, and it can be

shown that the harmonics will vary for different carrier arrangements [13]. The use of carriers with different phase shifts affects the pattern as the modulation wave passes from one carrier to another. If the system uses a sampled modulation wave, and is constrained to produce an alternating rise/fall pattern then delays can occur. Figure 2.16 shows a changeover between carriers for the two different carrier phase relationships.

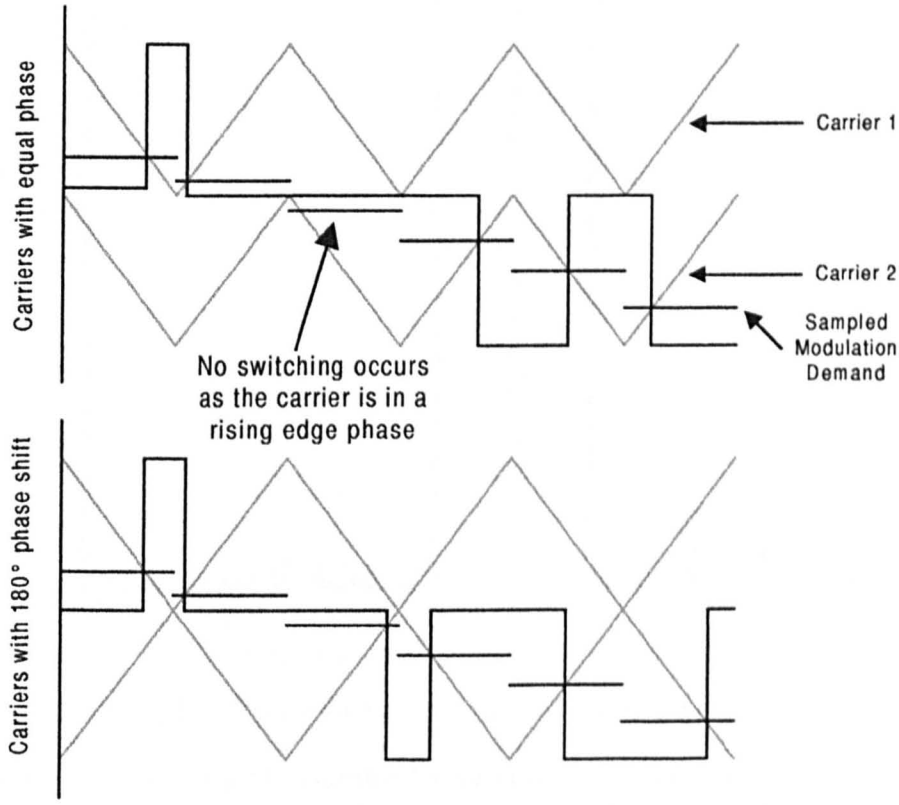

Figure 2.16 : *Carrier changeovers with different phase relationships*

Comparing the two examples, in the first case the modulation demand (the discontinuous steps since this is a sampled technique) changes to a lower carrier when the carrier phase would generate a rising edge. Since the output is already in the high state for this carrier, no switching occurs. With a different phase relationship however, when the changeover occurs the new carrier is already in the falling edge state. This allows switching to occur as normal. The difference has two effects in the pattern. The first effect is a delay that has been introduced at the changeover. This produces a notch in the output waveform, distorting the fundamental and increasing the magnitude of the low order harmonics. The second effect will be a change in the switching harmonics. The reversal of carrier will cause cancellation of certain harmonics, and increases in others.

Figure 2.17 shows the harmonic spectra for the line to line output of a five level inverter with different carrier phase relationships. This was simulated with natural (rather than sampled) PWM with a switching frequency of 1 kHz, a modulation frequency of 50 Hz, and at full modulation. Spectrum 'A' shows the harmonics when all four carriers are in phase. The switching harmonics consists of a low amplitude broad spread around the switching frequency. The switching frequency component cancels because this is the line to line spectra. With alternate carriers 180° out of phase, the pattern changes, and is shown in spectrum 'B'. In place of the broad spread of harmonics, there are several large harmonics clustered around the switching frequency.

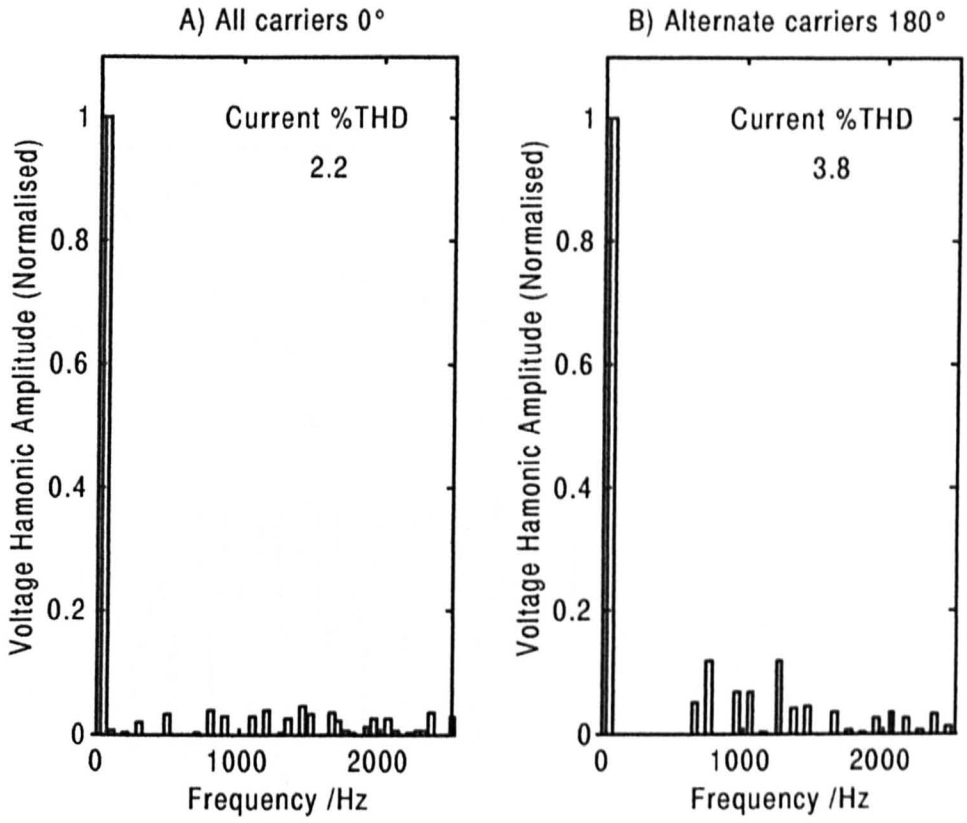

Figure 2.17 : *Line to line voltage harmonic spectra with different carrier phase relationships*

Calculating the total harmonic distortion for the current produced by the two patterns (using equation 2.1), it can be seen that there is significant difference in the values. These are quoted in the figure on the appropriate spectra. Looking at the individual phases when carrier changes are implemented does not show significant difference. When the line to line voltage is examined however it is evident that switching harmonic cancellation is reduced, resulting in the poor current THD.

2.6.3 Dipolar sub-harmonic PWM

An extension to the basic sub-harmonic PWM has been suggested [14] for three level PWM. Rather than switch between two levels during any period, the PWM can be modified to switch between three levels. This has been called dipolar PWM, with the standard technique being referred to as bipolar. Figure 2.18 shows the modified generation technique that is required for three level dipolar modulation.

The noticeable change in the technique is the changeover between the carriers and the modulation wave. In this example there are two modulation waves, and one single carrier, with the modulation waves separated by a defined distance. The crossing of the modulation waves with the carrier again generate the timings for the switching pattern. All the levels are being used in the output pattern. As the separation of the modulation waves is increased, then eventually the modulation waves will pass outside the carrier boundary. While only one of the modulation waves is within the carrier boundaries the output will only use two levels. The separation between the modulation waves defines the behaviour of the PWM and it has been shown that by setting a particular separation, then an output similar to the bipolar

technique can be generated [15]. The bipolar case can therefore be classified as a special condition of the generalised dipolar PWM.

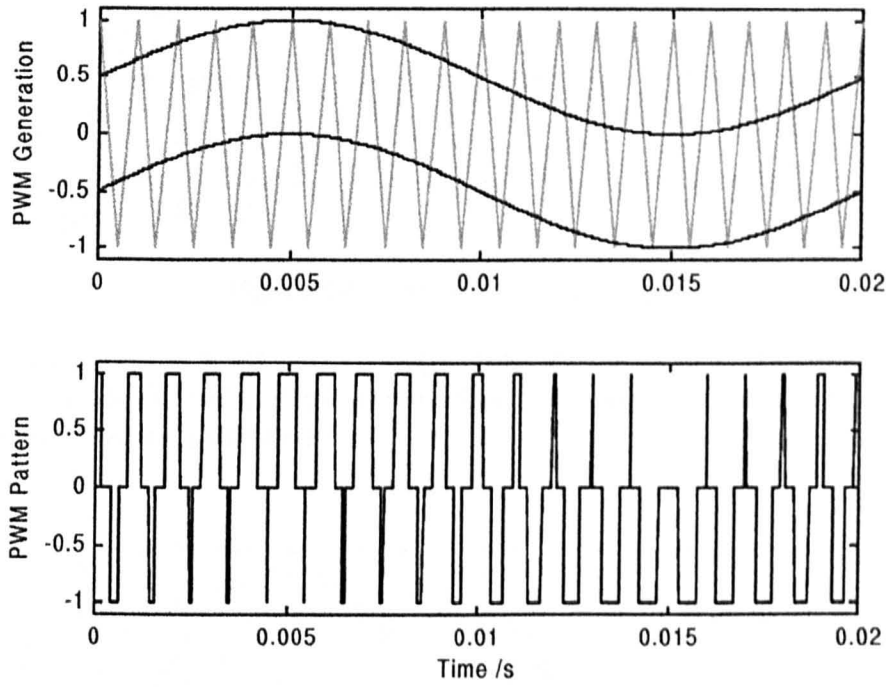

Figure 2.18 : *Dipolar Sub-Harmonic PWM*

It has been suggested [14] that under certain conditions the dipolar technique can produce improved output waveforms. One example that is quoted is low modulation depths, where the bipolar technique will go into pulse dropping. Whilst the dipolar technique is capable of generating an improved output under these conditions, it is at the expense of increasing the switching harmonics. The technique can be used for any number of levels with the appropriate number of shifted modulation waves though this can become complex.

Whilst benefits may be obtained in a few particular operating conditions, the technique produces significantly more switching events (increasing losses) and larger switching harmonics. The technique is therefore not considered practical.

2.6.3 Switching frequency optimal PWM (SFO-PWM)

The switching frequency limitation for an inverter is usually determined from the losses in the devices. This is particularly significant in the slower switching devices, where the switching losses are normally the dominant component. Switching frequency optimal control was suggested as a simple way of generating the PWM from a basic sub-harmonic technique that would minimise the switching losses. Assuming the use of bipolar modulation (for minimum switching), then for a three level inverter, one set of devices will switch during the positive half cycle, with the others switching during the negative half cycle. Under this condition, the mean switching frequency for the devices is effectively halved when compared to dipolar modulation. Since only one carrier is used at any instant in time, the switching strategy can be simplified [16]. The technique is very similar to the dipolar PWM when it

used to generate the bipolar pattern style. Figure 2.19 shows a block diagram for the technique when used for a three level inverter.

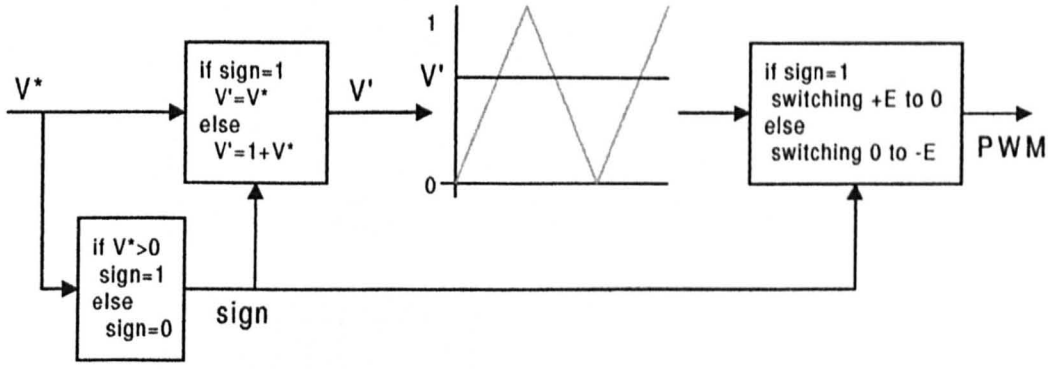

Figure 2.19 : *SFO-PWM Block Diagram*

The resulting system is based around a single carrier. As the modulation wave passes through zero there is a discontinuity. There are effectively two separate modulation waves. Figure 2.20 shows the pattern generation.

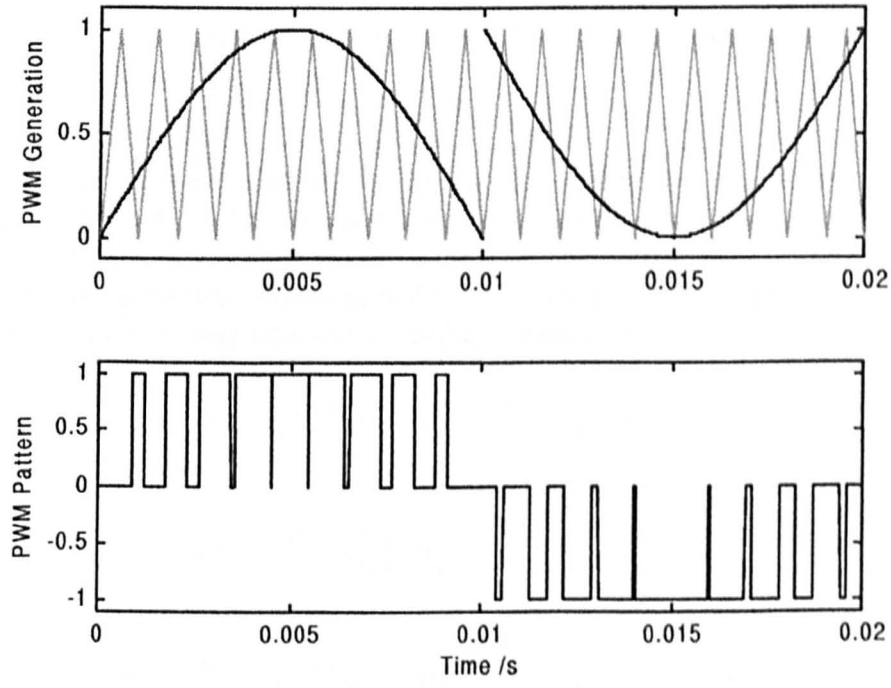

Figure 2.20 : *SFO-PWM Three Level Generation*

The technique can be applied to any number of levels in a similar fashion. Figure 2.21 shows the generation of a five level pattern. The modulation wave has been broken up into several sections, which equate the different carriers in the standard sub-harmonic technique.

This is clearly no different from the basic sub-harmonic technique. Rather than considering two separate carriers, the modulation wave steps up, and the appropriate outputs are changed. The output pattern, and harmonics are exactly the same. It may however be easier to implement in practice.

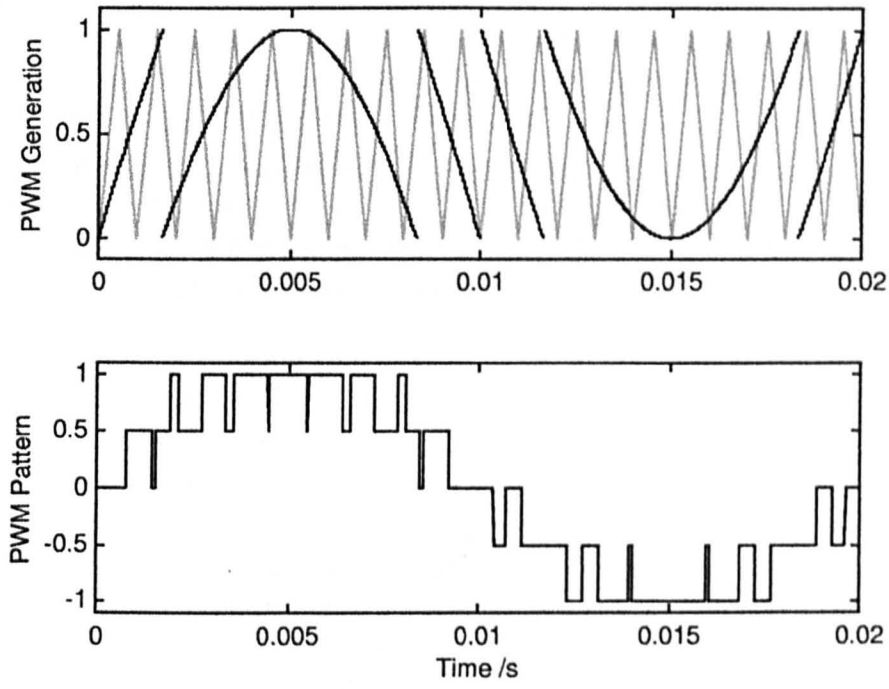

Figure 2.21 : *SFO-PWM Five Level Generation*

2.6.4 Space Vector PWM

The recent trend in PWM strategies for all types of inverters has been towards space vector modulation (SVM) [17]. The outputs of the three phases are mapped onto a two dimensional plane, with the three axes (1 per phase) 120° apart. The output can then be translated to a single rotating vector. The combinations for a three level inverter produce the map in figure 2.22. Each node in the map represents an output voltage [18].

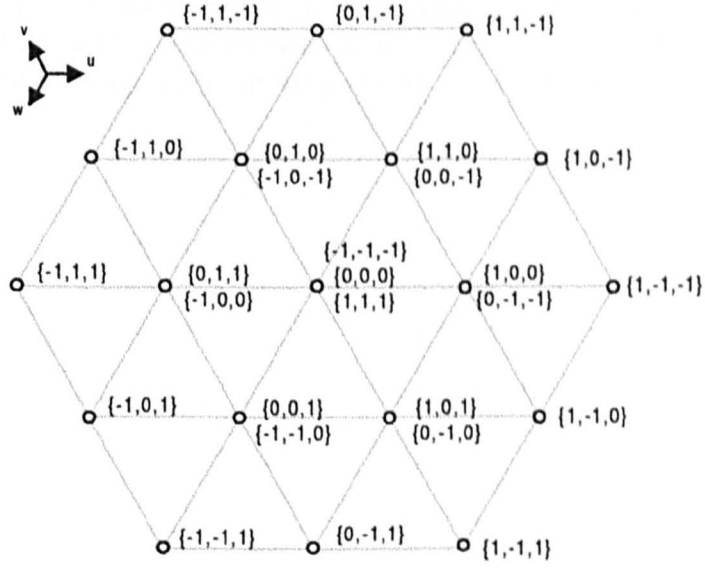

Figure 2.22 : *SVM Map for a Three Level Inverter*

In the figure it can be seen that there are 28 possible combinations which produce 19 different vectors at the output. There is redundancy in the PWM strategy, with several switch combinations producing the same output. As with the redundancy in the topologies themselves, the choice of state, whilst not affecting the load, will vary the conduction paths through the inverter, possibly affecting it's behaviour.

The map is divided into triangular sectors. A particular output vector can be generated by switching between the nodes of the sector in which the desired output lies. The switching times for the particular nodes can be calculated from the position of the vector. Figure 2.23 shows an example output vector mapped into its particular sector.

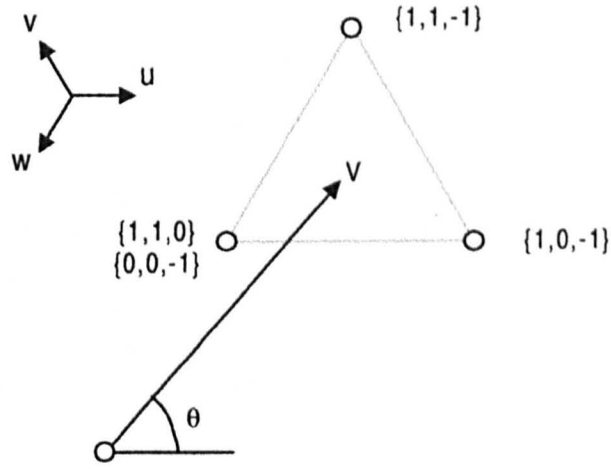

Figure 2.23 : *Output vector mapped into appropriate sector*

Following the basic rule that any phase can only switch one level at a time, then the active switch state can only change to one of the connected nodes in the map. As the vector rotates, it will eventually cross from one sector to another. When this happens, the present switch state node may not touch the sector containing the new demand vector. An example of this is shown in figure 2.24. The vector has moved between two sectors. At this changeover the switch state could potentially be at node A, which is not touching the new sector. In this case, a path needs to be found via adjacent nodes from the present switch state to one on the new sector. This problem is equivalent to the problems of carrier changeover in sub-harmonic PWM.

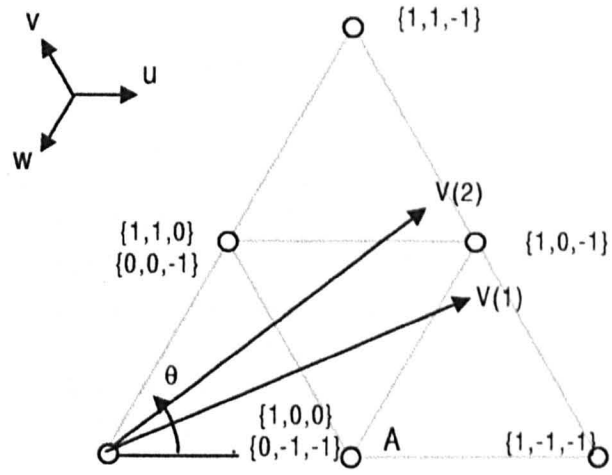

Figure 2.24 : *SVM Sector changeover*

For the conventional inverter, SVM is simple to implement, and since all six sectors touch at the zero node, there are no transient problems. Unfortunately when applied to multi-level topologies, the complexity increases. One solution that has commonly been taken is to introduce a closed loop hysteresis voltage controller [19]. By feeding back the output voltage and comparing against the desired voltage, states can be instantaneously selected to produce a mean output voltage as close to the demand as possible.

2.6.5 Discussion

From the various switching strategies that have been described, there are only three identifiably different techniques. Switching frequency optimal, and dipolar PWM are both variations on the sub-harmonic method. For the conventional inverter, space vector PWM has become the dominant strategy, since it is easy to calculate, and provides high fundamental output (equivalent to third harmonic addition in alternative techniques). For the multi-level, there is not such a great advantage. For a multi-level implementation the complexity of space vector transient conditions makes the technique more complicated than sub-harmonic techniques.

Fundamental switching has a good harmonic spectrum when a large number of levels are used, and the frequency is relatively high. It has become common to implement fundamental switching if high frequency is required, often with a changeover from basic sub-harmonic once a particular frequency is exceeded. This changeover point has increased with the switching speed of the devices.

The switching strategies that have been implemented during this project have been based on the sub-harmonic technique. Further detail to the practical implementation will be given in later chapters.

2.7 Conclusions

There are several circuits that meet the criteria defined from the generalised multi-level inverter. The three that have been presented here represent the circuits that have received research or development interest, either in academia or in industry. The choice between these circuits depends on the application for which the inverter is intended, since each has it's own particular advantages and disadvantages. Some of the circuits are easier to operate than others, with some requiring closed loop control just to achieve basic operation.

This project is primarily examining the application of multi-level inverters to motor control. In this field, the diode clamped circuit seems to offer several advantages, whilst still presenting several problems that require solutions, and it is this circuit which will be investigated further in the following chapters.

Accompanying the topologies are a range of switching strategies which range from the very basic fundamental pattern, to the modern space vector modulation. Apart from the fundamental technique, which is still the best technique when very high output frequencies are required, the techniques have little to distinguish them in terms of output quality. Selection is then mainly based on the ease of implementation.

The strategy that has been used during this project has been based on the sub-harmonic technique. This provided the simplest and quickest PWM implementation. Details of this are discussed in the later chapters, along with the refinements that have been added to improve the technique for various conditions.

2.8 Chapter References

[1] Nabae, I. Takahashi, H. Akagi, "A New Neutral-Point-Clamped PWM Inverter", IEEE Transactions on Industry Applications, Vol. 17, No. 5, Sept./Oct. 1981, pp 518-523.

[2] P. W. Hammond, "A New Approach to Enhance Power Quality for Medium Voltage AC Drives", IEEE Transactions on Industry Applications, Vol. 33, No. 1, Jan/Feb 1997.

[3] F. Z. Peng, J.-S. Lai, J. McKeever, J. VanCoevering, "A Multilevel Voltage-Source Inverter with Separate DC Sources for Static Var Generation", IEEE Conference Proceedings IAS'95, 1995, pp 2541-2548.

[4] D. Casini, M. Marchesoni, L. Puglisi, "Variable structure control system applied to multilevel power conditioning converters", Proceedings First European Space Power Conference, Madrid, Oct. 1989, pp 672-682.

[5] A. –Ch. Rufer, N. Schibli, Ch. Briguet, "A DIRECT COUPLED 4-QUADRANT MULTILEVEL CONVERTER FOR 16 2/3 TRACTION SYSTEMS", IEE Conference Proceedings PEVD'96, Nottingham UK, pp 448-453.

[6] J. –S. Lai, F. Z. Peng, "Multilevel Converters – A New Breed of Power Converters", IEEE Transactions on Industry Applications, Vol. 32, No. 3, May/June 1996, pp 509-517.

[7] P. Carrère, T. Meynard, J. P. Lavieville, "4000V-300A EIGHT LEVEL IGBT INVERTER LEG", Conference Proceedings EPE'95, Sevilla, Vol. 1, 1995, pp 106-111.

[8] N. Aouda, L. Prissé, T. Meynard, H. Foch, "A Multilevel Rectifier with Unity Power Factor and Sinusoidal Input Current for High Voltage Applications" EPE Journal. Vol. 6, No. 3-4, December 1996, pp 27-35.

[9] S. Ogasawara, H. Akagi, "Analysis of Variation of Neutral Point Potential in Neutral-Point-Clamped Voltage Source PWM Inverters", IEEE Conference Proceedings IAS'93, 1993, pp 965-970.

[10] M. Fracchia, T. Ghiara, M. Marchesoni, M. Mazzucchelli, "OPTIMISED MODULATION TECHNIQUES FOR THE GENERALISED N-LEVEL CONVERTER", IEEE Conference Proceedings PESC'92, 1992, pp 1205-1213.

[11] R. W. Menzies, P. Steimer, J. K. Steinke, "Five-Level GTO Inverters for Large Induction Motor Drives", IEEE Transactions on Industry Applications, Vol. 30, No. 4, July/Aug. 1994, pp 938-944.

[12] S. R. Bowes, M. J. Mount, "Microprocessor Control of PWM Inverters", IEE Proceedings Part B, Vol. 128, No. 6, November 1981, pp 293-305.

[13] G. Carrara, S. Gardella, M. Marchesoni, R. Salutari, G. Sciutto, "A New Multilevel PWM Method: A Theoretical Analysis", IEEE Transactions on Power Electronics, Vol. 7, No. 3, July 1992, pp 497-505.

[14] B. Velaerts, P. Mathys, E. Tatakis, G.Bingen, "A NOVEL APPROACH TO THE GENERATION AND OPTIMISATION OF THREE-LEVEL PWM WAVE FORMS", Conference Proceedings PESC'88, April 1988, pp 1255-1262.

[15] B. Velaerts, P. Mathys, G. Bingen, "NEW DEVELOPMENTS OF 3-LEVEL PWM STRATEGIES", Conference Proceedings EPE'89, Aachen, 1989, pp 411-416.

[16] J. K. Steinke, "Switching Frequency Optimal PWM Control of a Three-Level Inverter", IEEE Transactions on Power Electronics, Vol. 7, No. 3, July 1992, pp 487-496.

[17] H. W. van der Broeck, H. –C. Skudelny, G. V. Stanke, "Analysis and Realisation of a Pulsewidth Modulator Based on Voltage Space Vectors", IEEE Transactions on Industry Applications, Vol. 26, No. 1, Jan/Feb 1988, pp 142-150.

[18] R. Joetten, C. Kehl, "A FAST SPACE-VECTOR CONTROL FOR A THREE-LEVEL VOLTAGE SOURCE INVERTER", Conference Proceedings EPE'91, Firenze, Vol. 2, pp 70-75.

[19] R. Rohas, T. Ohnishi, T. Suzuki, "An Improved Voltage Vector Control Method of Neutral-Point-Clamped Inverters", IEEE Transactions on Power Electronics, Vol. 10, No. 6, Nov. 1995, pp 666-672.

Chapter 3

The Three Level Inverter - Motor Drive

Chapter Contents

3.1 Introduction

As mentioned in the previous chapter, the diode clamped configuration will be investigated as this is seen to be the topology best suited to motor drive applications. As a starting point for the eventual development of a five level inverter, the first practical objectives for the project were the construction and operation of a three level inverter. This would allow some experience to be gained on a simpler circuit, and allow basic control to be developed and implemented. This chapter will detail the work completed during these early stages.

The chapter will describe the fundamental operation of the circuit and analyse the operating modes. Once this has been established, the actual power electronic construction will be described. The later sections will describe the implementation of the switching strategy and neutral point control.

Practical operating results are presented from the constructed prototype inverter (shown in figure 3.1).

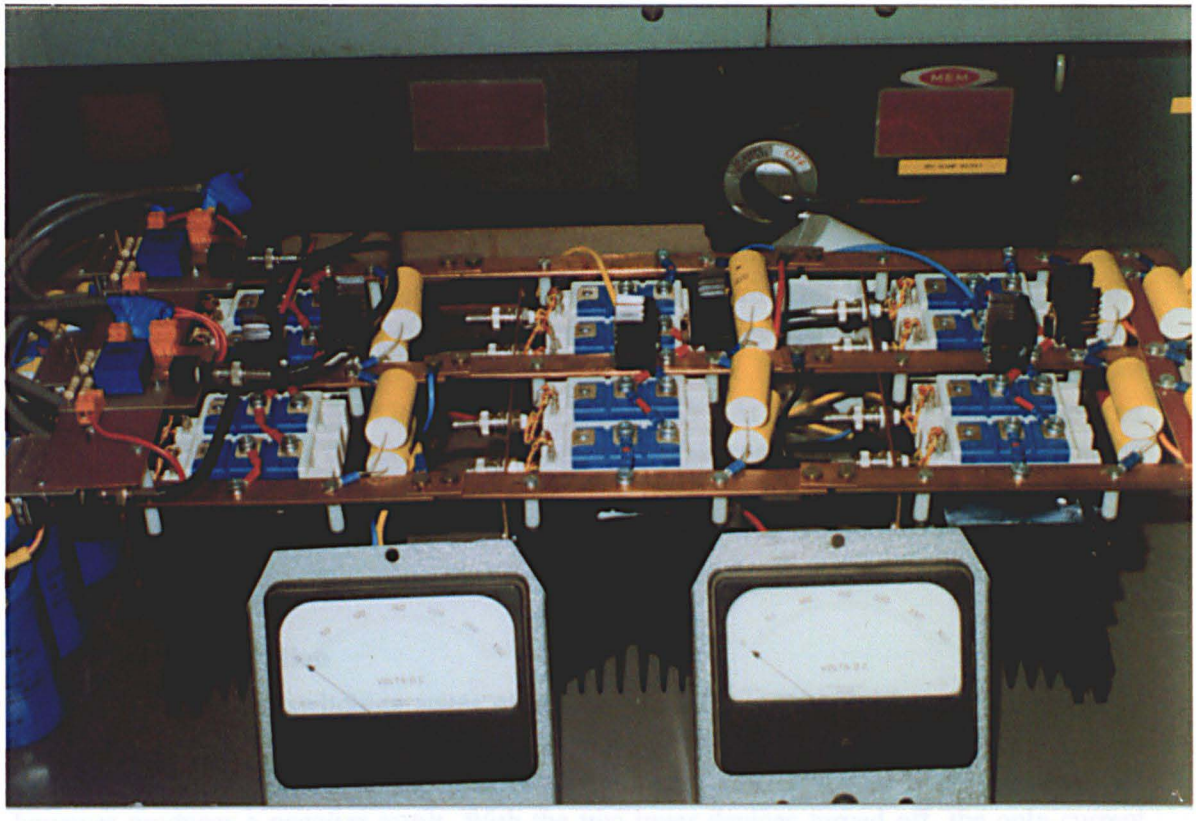

Figure 3.1 : *Prototype Three Level Inverter*

3.2 The Three Level Circuit Structure

Figure 3.2 shows the circuit diagram for a three phase, three level, diode clamped inverter.

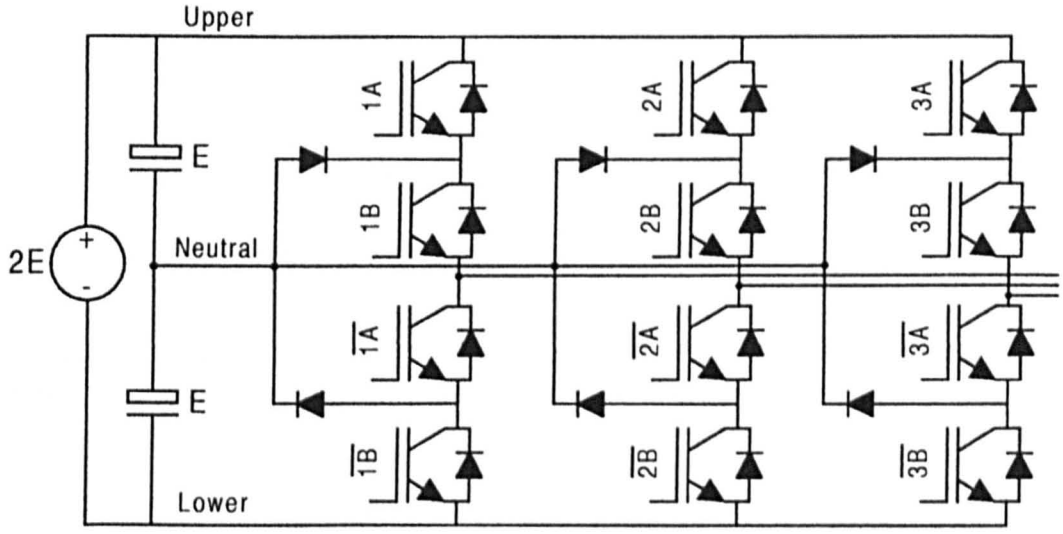

***Figure 3.2** : The Three Level Inverter*

Each phase of the circuit consists of four IGBTs with anti-parallel diodes, plus two additional power diodes. These separate diodes provide conduction paths back to the mid-point or 'Neutral Point' of the capacitor bank. In general, any type of fully controlled power switch can be used in this circuit structure. IGBTs were used during this project, and this is the symbol used as standard in the circuit diagrams. Similar to the conventional inverter, devices are switched in complementary pairs (one upper and one lower device). When an upper device ($1A$) is 'on', its paired lower device ($\overline{1A}$) is 'off'. At any instant in time two devices will be blocking, and two devices will be conducting. This ensures that the DC link cannot be shorted through the devices. Following standard convention, the output voltage is measured with respect to the Neutral Point, with the DC bus providing equal positive and negative supply rails.

3.2.1 Modes of operation

Table 3-1 defines the switching states of one phase of the inverter with respect to the gate drive signals (A, B) and the output current direction. Three of the switching states select the different output voltages, and are unaffected by the current direction. State number three however produces a peculiar result. With the two inner devices turned off, the only current paths available are through the anti-parallel diodes. If a load current is present when the output is switched to this state, then the current will flow through the anti-parallel diode of a device that should be blocking. This results in only one device being in the blocking state. This single device will be exposed to twice the normal blocking voltage. Because of this, the switching state cannot be utilised.

State	A	B	Current	Output Voltage (w.r.t. Neutral Point)
1	0	0	+	-E
	0	0	-	-E
2	0	1	+	0
	0	1	-	0
3	1	0	+	XX
	1	0	-	XX
4	1	1	+	E
	1	1	-	E

Table 3-1 : *Switching States*

The conduction paths corresponding to states one, two and four are shown in figures 3.3 to 3.5. Each figure shows the respective paths for both positive and negative load current.

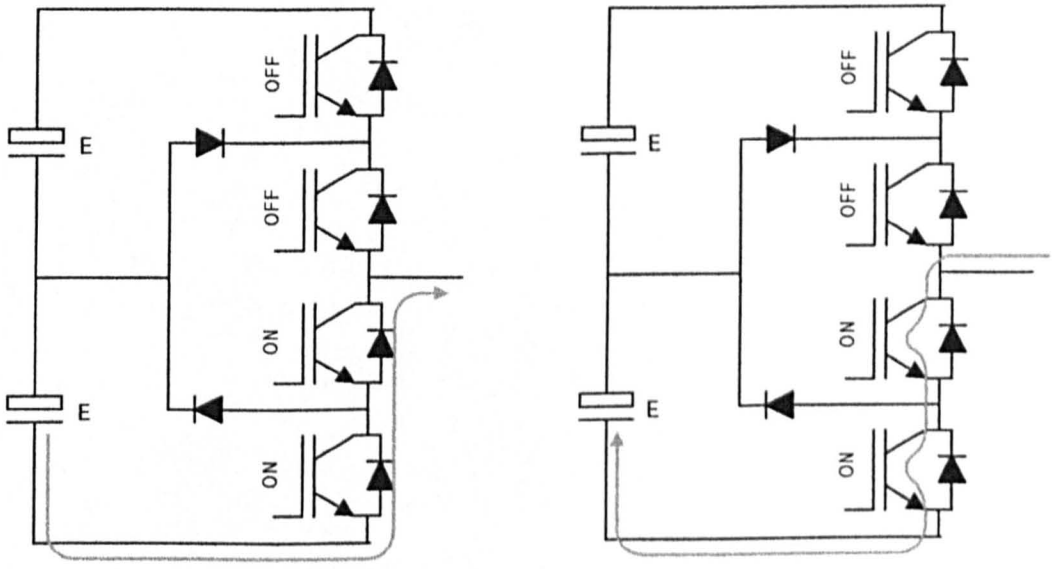

Figure 3.3 : *Conduction modes for state one*

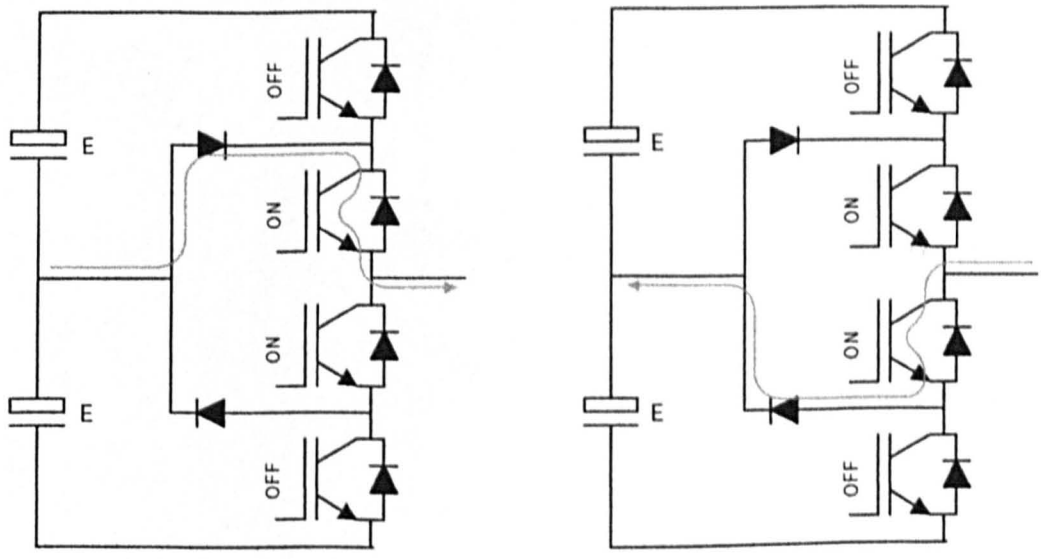

Figure 3.4 : *Conduction modes for state two*

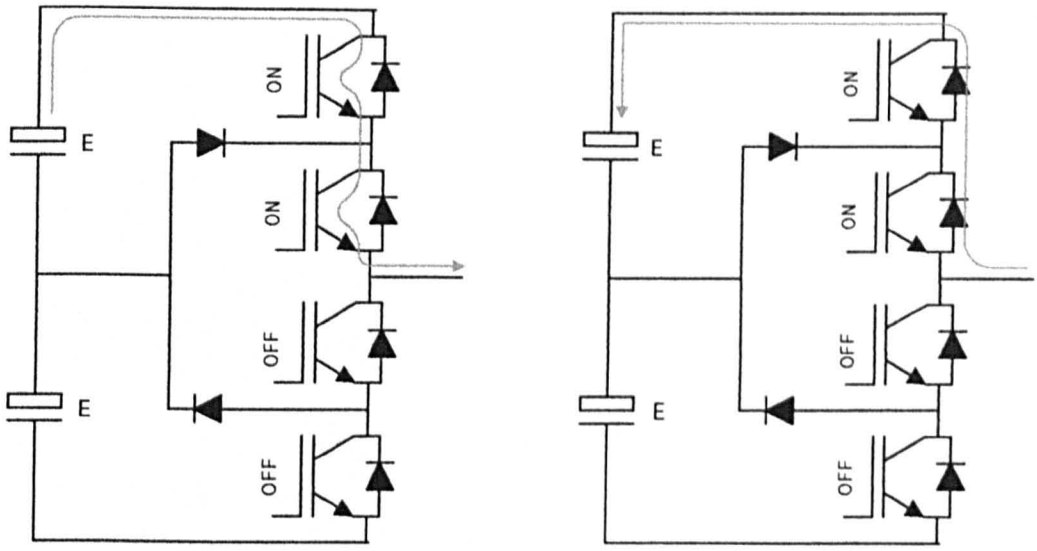

Figure 3.5 : *Conduction modes for state four*

3.2.2 Control of the inverter phase

Switching between the three permitted states described above creates the standard stepped output waveform. In chapter two it was defined that the transition on the output had to be a single level step, either between states one and two, or states two and four. By attempting to switch directly between states one and four, then there is a step of two levels, which breaks this rule. Examining the commutation process, it can be seen that both the upper devices both have to change from blocking to conduction, with the lower devices going through the reverse process. These devices are unlikely to evenly share the voltage naturally (due to variation in device parameters, circuit layout, and gate drive differences) which can result in an over-voltage on one of the devices. If this transition is produced by the switching strategy, then the addition of snubber circuits is required to ensure transient voltage sharing. Failure to do this can cause device failure.

The selection of switching state is performed by the specific PWM strategy implemented in the controller. The specific details of this will be discussed later in the chapter. By generalising the switching strategy, it is possible to examine the fundamental behaviour (independent of the particular switching strategy). From this analysis it is possible to confirm the basic operational capabilities of the circuit, namely its ability to operate as a variable voltage, variable frequency supply.

The analysis of the circuit will be based on the mathematical functions that define the time spent in a particular state at any instant of the modulation strategy. Assuming the PWM is asynchronous, then if the output is examined at a particular instant over an infinite number of cycles, then the average voltage should be the demanded value from the modulator. A probability map can also be produced from this, which gives the probability of the output being in a particular state for a given reference. Expressing the probability mathematically, the 'modulation functions' are created. These functions provide a mathematical basis for defining the proportion of time spent in a particular state. The probability is directly tied to the demanded reference, and ignores the specifics of the modulation.

Three basic rules can be defined as follows.

1) To obtain a positive output, the circuit is switched between states two and four. The mean output voltage will be given by:

$$V_{mean} = E.upper \qquad [3.1]$$

Where *upper* = modulation function ($0 < upper < 1$), being the proportion of time spent in state four.

2) To obtain a negative output, then the circuit is switched between states two and one. The mean output voltage is thus given by:

$$V_{mean} = -E.lower \qquad [3.2]$$

Where *lower* = modulation function ($0 < lower < 1$), being the proportion of time spent in state one.

3) At no instant will the state instantaneously change between one and four.

The third rule, states that the output cannot switch between states one and four, which means that state two must be used. The modulation function for the neutral state can be defined from the functions for the other states.

3.2.3 Analysis of Operation

Figure 3.6 shows the sinusoidal wave, which is the 'ideal' demanded output waveform. From this it is then possible to define the respective modulation functions for the states one and four, and hence state two. All three modulation functions are plotted in figure 3.7. This example represents the full modulation condition.

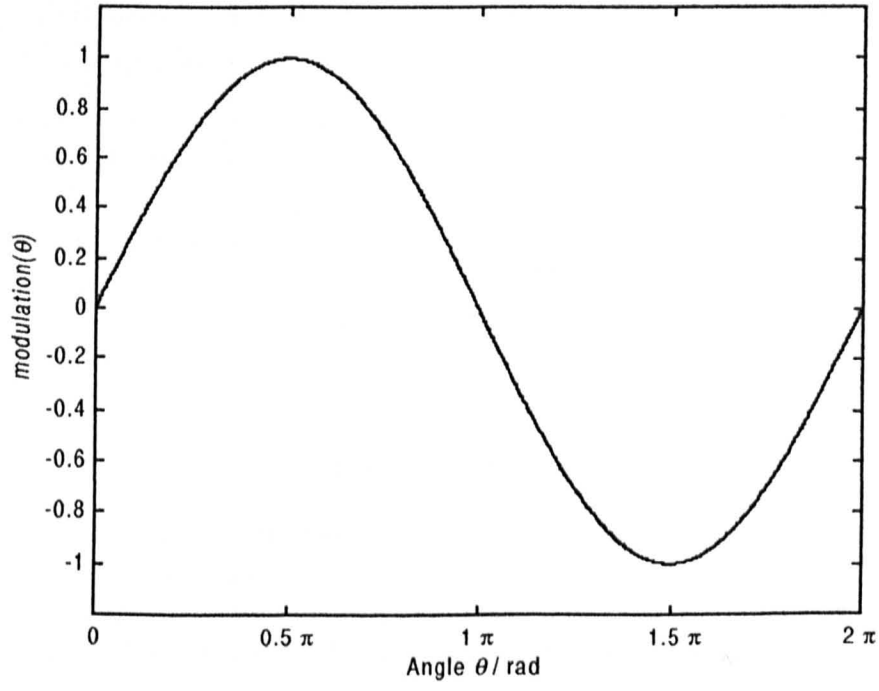

Figure 3.6 : *Sinusoidal modulation demand*

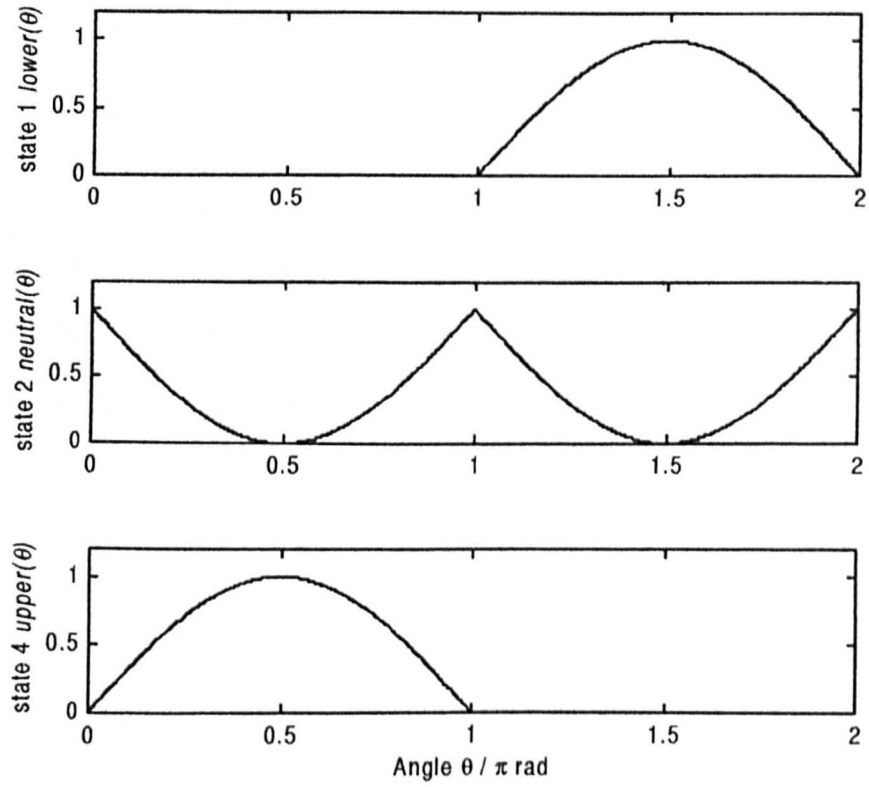

Figure 3.7 : *Modulation functions for the switching states*

Mathematically, the modulation demand can be defined as equation 3.3.

$$\begin{aligned} &Modulation(t) = A\sin(\omega t) \\ &A = \text{ Modulation Amplitude } (0 < A < 1) \end{aligned} \qquad [3.3]$$

Applying the basic rules that have been described, then the state modulation functions can then be defined by equation 3.4.

$$\begin{aligned} \text{State 4 : } upper(t) &= \begin{cases} Modulation(t) & Modulation(t) \geq 0 \\ 0 & Modulation(t) < 0 \end{cases} \\ \text{State 2 : } neutral(t) &= \begin{cases} 1 - Modulation(t) & Modulation(t) \geq 0 \\ 1 + Modulation(t) & Modulation(t) < 0 \end{cases} \\ \text{State 1 : } upper(t) &= \begin{cases} 0 & Modulation(t) \geq 0 \\ Modulation(t) & Modulation(t) < 0 \end{cases} \end{aligned} \qquad [3.4]$$

With the sinusoidal demand, the functions are repetitive, therefore it is possible to replace the ωt term by the angle θ, in the range $0 < \theta < 2\pi$. Assuming the load is linear and reactive, then the phase current can be taken as being purely sinusoidal. There will be a phase shift with respect to the voltage. An equation for the current is defined in equation 3.5.

$$\begin{aligned} &i_{load}(\theta) = \hat{I}\sin(\theta + \phi) \\ &\phi = \text{phase shift } (rad) \end{aligned} \qquad [3.5]$$

In this analysis, the modulation functions have been used to define the output voltage. The equations that define the proportion of time in each state also control the path taken by the load current. It is therefore possible to define the currents drawn from the three nodes of the capacitor bank, as the product of the load current and the respective modulation function. The three resulting equations are given below.

$$\begin{aligned} i_{upper}(\theta) &= i_{load}(\theta).upper(\theta) \\ i_{neutral}(\theta) &= i_{load}(\theta).neutral(\theta) \\ i_{lower}(\theta) &= i_{load}(\theta).lower(\theta) \end{aligned} \qquad [3.6]$$

By integrating the instantaneous current equations over the modulation cycle, the mean current can be obtained. Taking the current drawn from the neutral point as an example, then the modulation function can be defined by equation 3.7.

$$neutral(\theta) = \begin{cases} (1 - A\sin(\theta)) & 0 \le \theta < \pi \\ (1 + A\sin(\theta)) & \pi \le \theta < 2\pi \end{cases} \qquad [3.7]$$

By integrating the product of this function with equation 3.5 (the load current) then the following solution is obtained.

$$I_{neutral} = \frac{1}{2\pi}\int_0^{2\pi} i_{load}(\theta).neutral(\theta)\,d\theta \qquad [3.8]$$

$$\begin{aligned} I_{neutral} = \frac{1}{2\pi}\Bigg[&\int_0^{\pi} \hat{I}\sin(\theta+\phi).(1 - A\sin(\theta))\,d\theta \\ &+ \int_{\pi}^{2\pi} \hat{I}\sin(\theta+\phi).(1 + A\sin(\theta))\,d\theta\Bigg] \end{aligned} \qquad [3.9]$$

$$\begin{aligned} I_{neutral} = \frac{1}{2\pi}\Bigg[&\Bigg[-\hat{I}\cos(\theta+\phi) - \frac{A\hat{I}}{2}\cos(\phi)\theta + \frac{A\hat{I}}{2}\sin(2\theta+\phi)\Bigg]_{\theta=0}^{\theta=\pi} \\ &+ \Bigg[-\hat{I}cos(\theta+\phi) + \frac{A\hat{I}}{2}\cos(\phi)\theta - \frac{A\hat{I}}{2}\sin(2\theta+\phi)\Bigg]_{\theta=\pi}^{\theta=2\pi}\Bigg] \end{aligned} \qquad [3.10]$$

$$I_{neutral} = 0 \qquad [3.11]$$

The calculation shows that the neutral point current has a mean value of zero. By similar calculations, the mean current can be found for the positive (upper) node and the negative (lower) node. It should be remembered that these equations are based on a single phase of the inverter.

$$I_{upper} = \frac{1}{2\pi}\int_0^{2\pi} i_{load}(\theta).upper(\theta)\,d\theta \qquad [3.12]$$

$$I_{upper} = \frac{A\hat{I}}{4}\cos(\phi) \qquad [3.13]$$

$$I_{lower} = \frac{1}{2\pi}\int_0^{2\pi} i_{load}(\theta)lower(\theta)d\theta \qquad [3.14]$$

$$I_{lower} = -\frac{A\hat{I}}{4}\cos(\phi) \qquad [3.15]$$

These calculations can be confirmed by calculating the power flow from the DC link capacitor bank, and comparing it to the AC load power. The power flow from the capacitors can be defined by the following equations.

$$P_{DC} = E.I_{upper} - E.I_{lower} \qquad [3.16]$$

$$P_{DC} = \frac{EA\hat{I}}{2}\cos(\phi) \qquad [3.17]$$

The standard equation can be quoted for the fundamental power on the AC side, and this is given in equation 3.18.

$$P_{AC} = V_{rms} I_{rms}\cos(\phi) \qquad [3.18]$$

From equations 3.1 and 3.2, it is possible to define the AC voltage under ideal conditions.

$$V_{rms} = \frac{\hat{V}}{\sqrt{2}} \qquad [3.19]$$

$$V_{rms} = \frac{AE}{\sqrt{2}} \qquad [3.20]$$

Similarly, from equation 3.5, it is possible to define the AC current.

$$I_{rms} = \frac{\hat{I}}{\sqrt{2}} \qquad [3.21]$$

Substituting equations 3.20 and 3.21 into 3.18 gives the AC power for the inverter.

$$P_{AC} = \frac{EA\hat{I}}{2}\cos(\phi) \qquad [3.22]$$

Equations 3.17 and 3.22 for the ideal AC and DC side powers show the same result, confirming the validity of the analysis.

3.2.4 Conclusion of analysis

The objective of the analysis was to confirm the capability of the inverter as a variable voltage, variable frequency supply. The basic requirement is the ability to generate a waveform to a particular modulation demand. This was defined by equations 3.1 and 3.2, which defined the modulation. Given these definitions the converter modulation was then analysed to confirm the circuit will work as predicted.

Using modulation functions based on a generalised switching strategy, the effect of the modulation on the circuit behaviour was investigated. This technique allows prediction of the currents in the DC link. The analysis was then checked via comparison of the power flow on the AC and DC sides of the inverter.

Two significant results are obtained from the inverter. The first is that voltage can be generated from the modulation within ±E. Varying the modulation produces a sinusoidal output. The second significant result is that the neutral point current in the DC link should have a mean value of zero provided that the modulation is balanced.

The analysis has been completed for a single phase of the inverter. The analysis can be expanded for a three phase case by superposition, with the respective currents summed into the DC link.

3.3 Power Circuit Implementation

The power circuit was constructed in a modular form, with each phase being a separate block. As this was the first power construction in the project, the first phase module was constructed and tested. Further phases were constructed after basic evaluation had been completed, and operation was shown to be satisfactory.

The basic inverter was rated for operation from the standard 415V AC supply, and nominally rated at 25A peak output current.

3.3.1 Power Semiconductor Devices

Selection of the semiconductor devices was made using two main criteria. The project, being a practical evaluation, needed to operate at a reasonable power level. This desire was tempered by the limited funding available for the purchase of devices. With these criteria in mind, the following devices were selected.

IGBTs : Siemens BSM 25 GAL 120

Siemens produce a range of module packaged IGBT devices. This particular module being a 25A (continuous rating at 125°C) 1200V device. 'GAL' modules were chosen, which consist of an IGBT, with an anti-parallel diode, and an additional freewheeling diode that was not used. This module type is commonly used for resistive 'brake' chopper units in inverter drives.

Clamp diodes : Harris RUR30100

Harris produce a wide range of high speed power diodes. The 'RUR' range is described as ultrafast, exhibiting a low reverse recovery current. The diodes are available in several package styles, depending on the current and voltage rating. The diode used is rated for 30A and 1000V in a TO-220 package.

3.3.2 Circuit Layout

A photograph of the complete inverter was shown in figure 3.1. The three separate phase modules are clearly identifiable. Figure 3.8 shows a photograph of a single phase block. The four IGBT modules are mounted to the main heatsink base, with the gate connections brought out to BNC connectors mounted on a side panel. The additional clamp diodes are mounted on small floating heatsinks, positioned above the switching devices. This provided the closest connection method to minimise the path inductance. With this arrangement the diodes are not solidly mounted, and only have limited thermal dissipation capability. For the prototype this was considered to be sufficient, since long running periods were not expected. The mounting of the diodes can be seen from the photograph in figure 3.9.

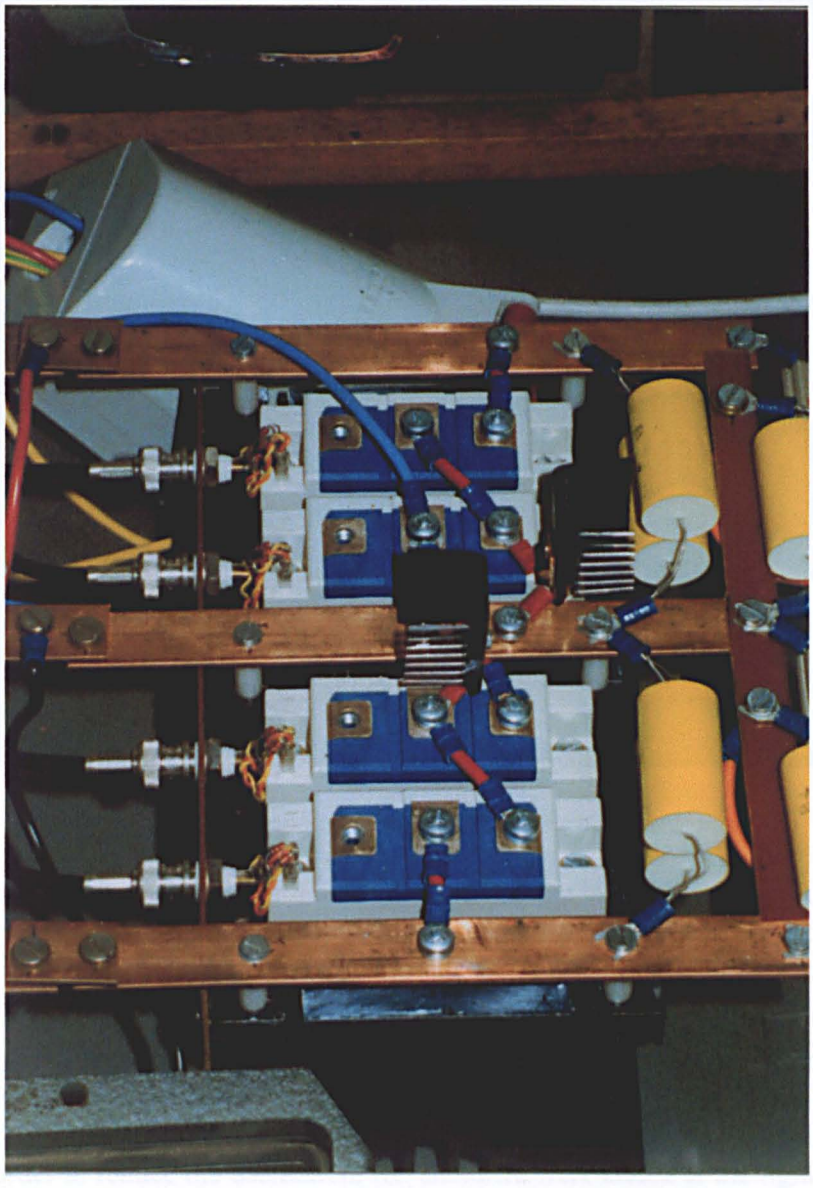

Figure 3.8: *Photograph of a phase from the inverter*

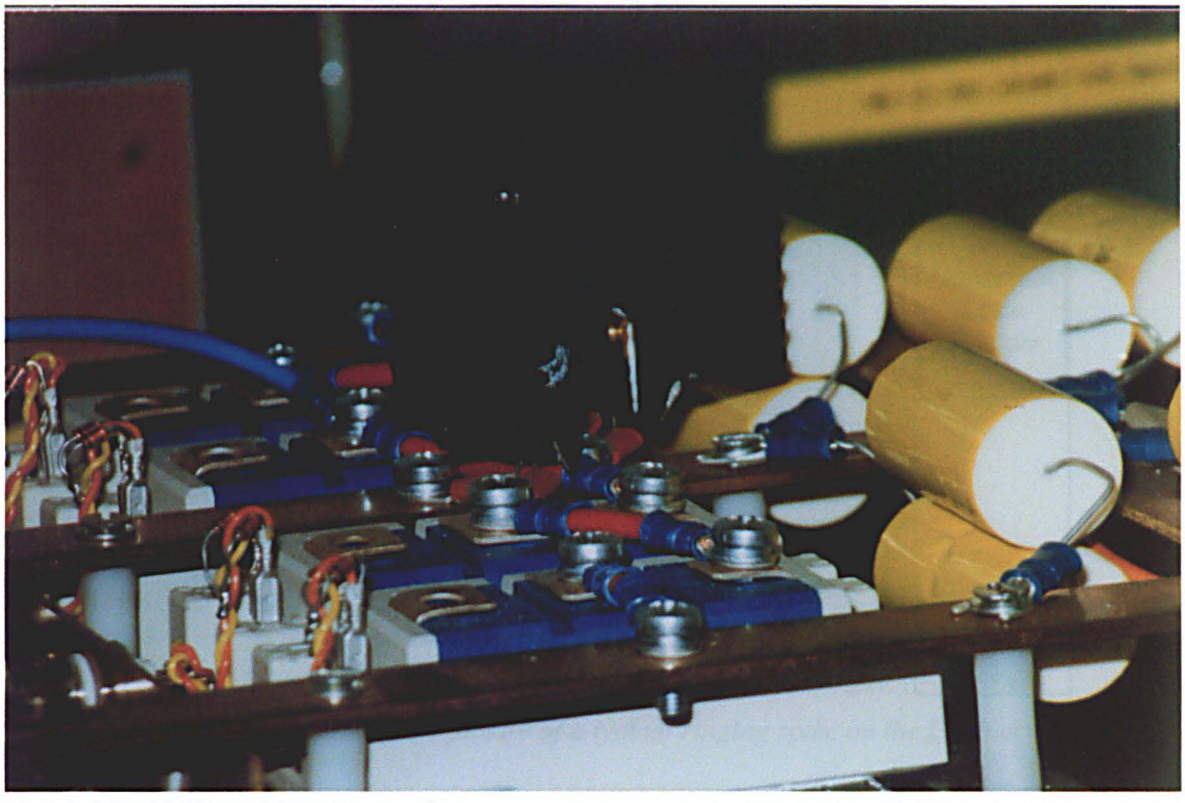

Figure 3.9: *Photograph of the clamp diodes on a phase module*

Referring to the complete inverter as shown in figure 3.1, the main electrolytic capacitor bank is located at the left hand end of the busbars, with small polyester next to each module to provide local capacitance. These capacitors provide a source for the high frequency transient currents required during switching.

The separation of the busbars creates a relatively significant inductance between these capacitors. This LC network behaves as a transmission line, and the switching transients trigger ringing oscillations. The resistance of the busbars is too small to provide significant damping. In order to reduce the oscillation, RC snubbers were added at the right hand end of the busbars to provide a termination. The resistance provides a sink for the ringing energy, and damps the oscillations. Figure 3.10 shows a ringing spike during a switching transient with the line snubbers applied. The initial voltage overshoot is approximately 60V (20V/div) with no significant ringing. This compares favourably against a commercial two level inverter with similar ratings. An equivalent result for the commercial inverter is shown in figure 3.11.

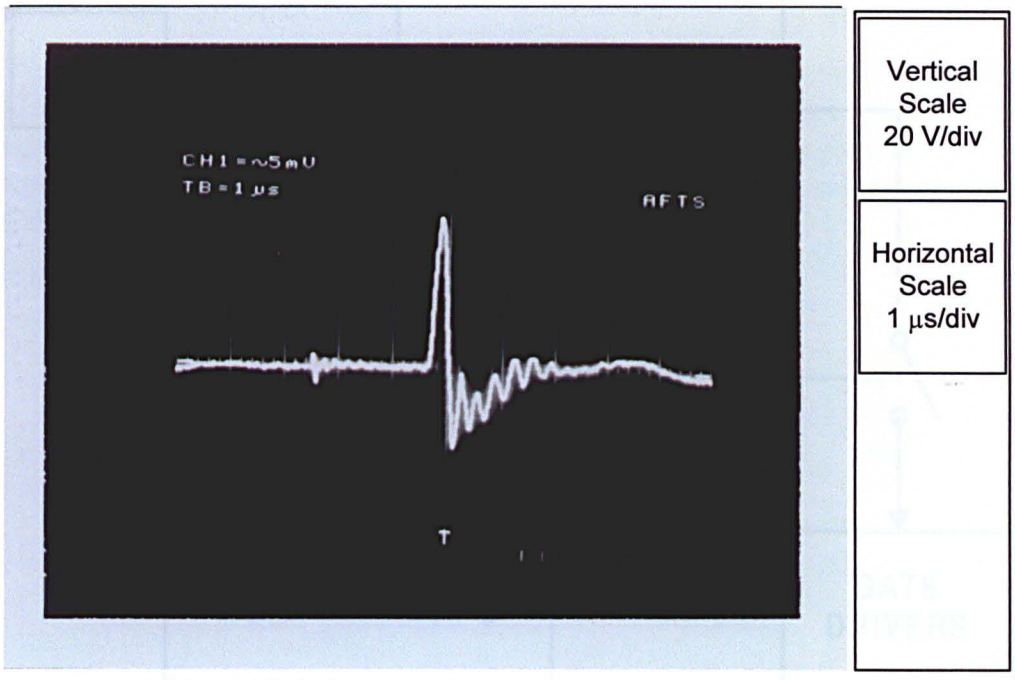

Figure 3.10: *Oscilloscope picture of a typical ringing spike on the DC bus*

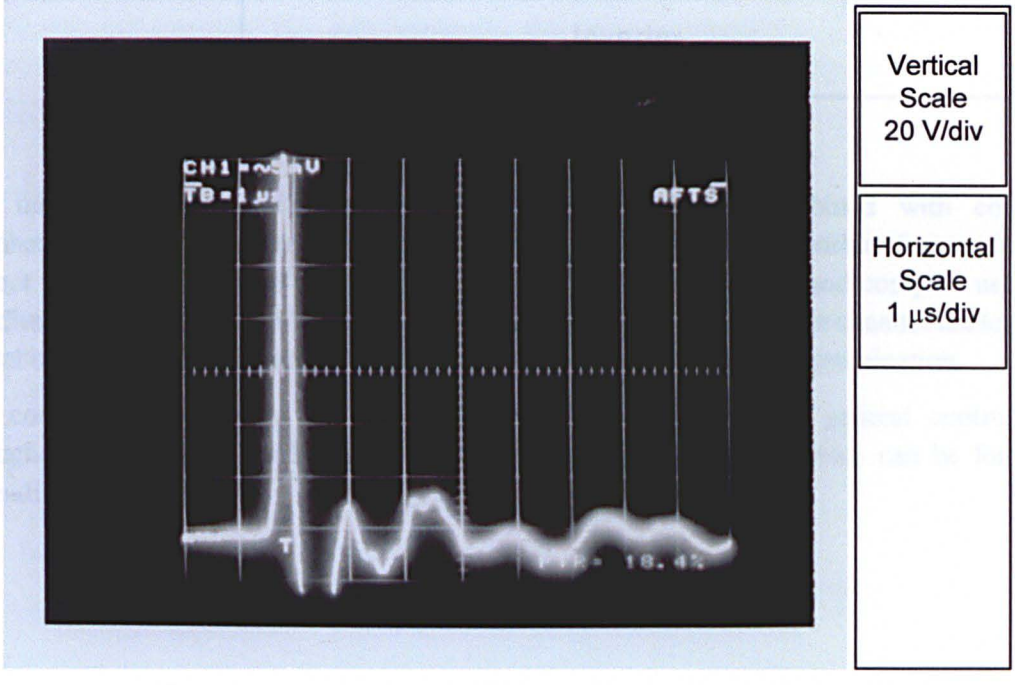

Figure 3.11 : *Oscilloscope picture of DC bus ringing on a commercial inverter*

Between the main capacitor bank and the phase modules, three hall effect current transducers are mounted around the DC bus rails. These provide measurements of the currents drawn by the inverter, and are used to provide over-current protection. Two voltage transducers are also present to provide over-voltage protection, and to provide a measurement of the neutral point potential.

The inverter control was provided from a Siemens 80C166 microcontroller, which was built into a nineteen inch rack unit along with the associated peripheral units, and protection hardware. An overview diagram is shown in figure 3.12.

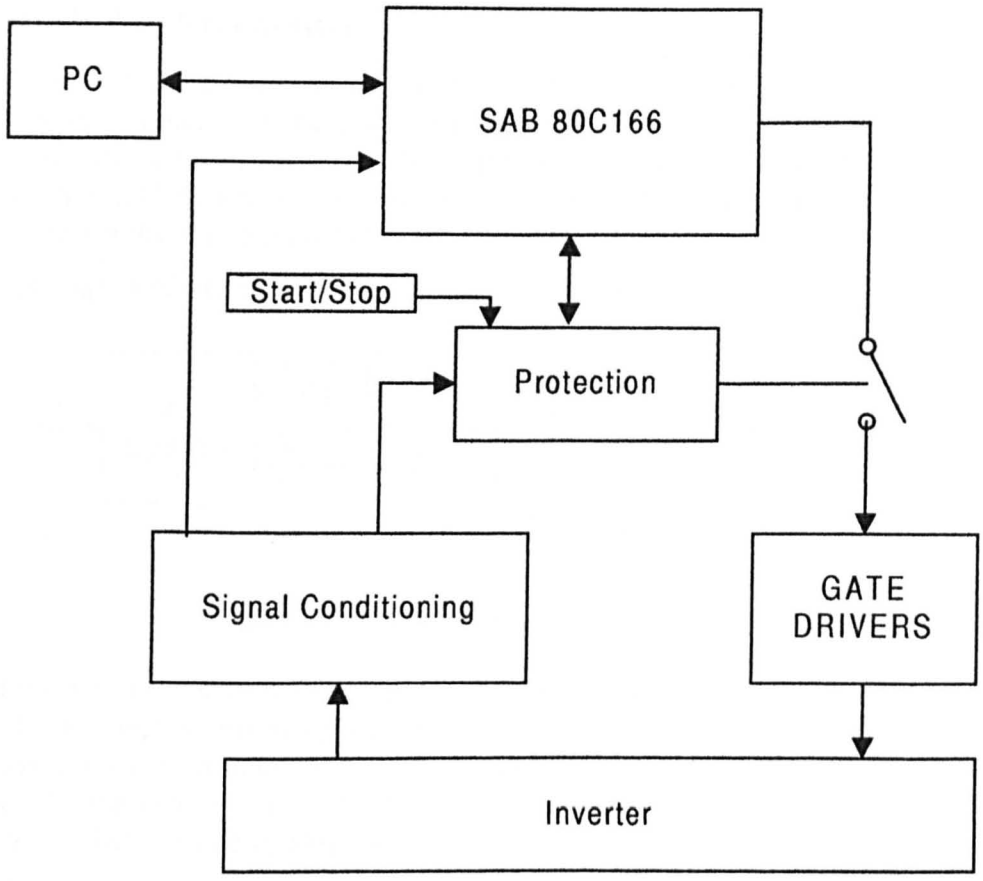

Figure 3.12 : *Overview of control hardware*

The microcontroller provides the computational operations, combined with common peripheral units typically used in industrial applications. The most important feature for this project was the "CAPCOM" module [1], which is a combined timer and compare unit that can directly produce the PWM signals. The processor also includes a ten channel analogue to digital converter, general purpose counter/timer modules, and serial communication.

The control hardware was built on a modular basis to provide a general control unit throughout the project. Further detail of the control circuits and software can be found in appendix 1.

3.4 PWM Implementation

The PWM scheme implemented on the prototype three level inverter is based on the standard sub-harmonic technique described in chapter two. A sampled modulation wave is compared against two triangular carrier waves. The upper carrier is used for the positive half cycle to generate timings for states two and four, whilst the lower carrier generates timings for states one and two during the negative half cycle.

A block diagram of the control strategy is shown in figure 3.13.

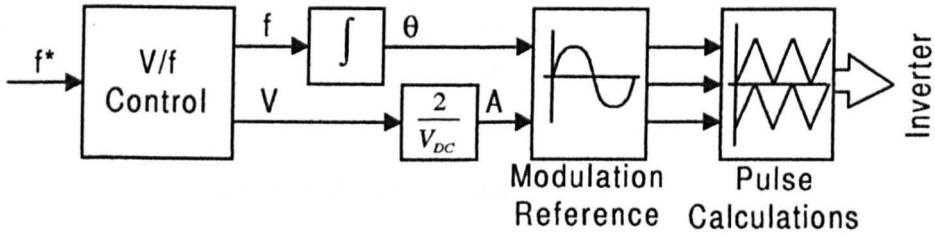

Figure 3.13 : *Block Diagram for PWM routine*

The drive is operated under basic open loop V/f control. Using the amplitude (represented by A) and angle (represented by θ) information, three references are generated from a stored modulation wave. Comparing these three values against triangle waves produces the pulse timings for the inverter. The new difficulty that arises is how the changeover between different carriers is handled. This has to be controlled to avoid stepping through more than one level.

3.4.1 Pulse Width Calculation

There are several common techniques for generating three phase references in a digital sub-harmonic PWM generation system. The simplest method is to define a common amplitude, and a single reference angle. The actual angles for the three phases are then defined as an ideal three phase set. From the angle information, values can be found from a standard modulation table. The frequency reference is then used to provide the amplitude scaling. The modulation table consists of 500 points, which represent a quarter cycle. Symmetry provides the full modulation cycle with 2000 points (scaled by 10 to give 20000 points for 0.1Hz minimum frequency). The timers are loaded with values based on a 200ns resolution, hence the ±1250 output.

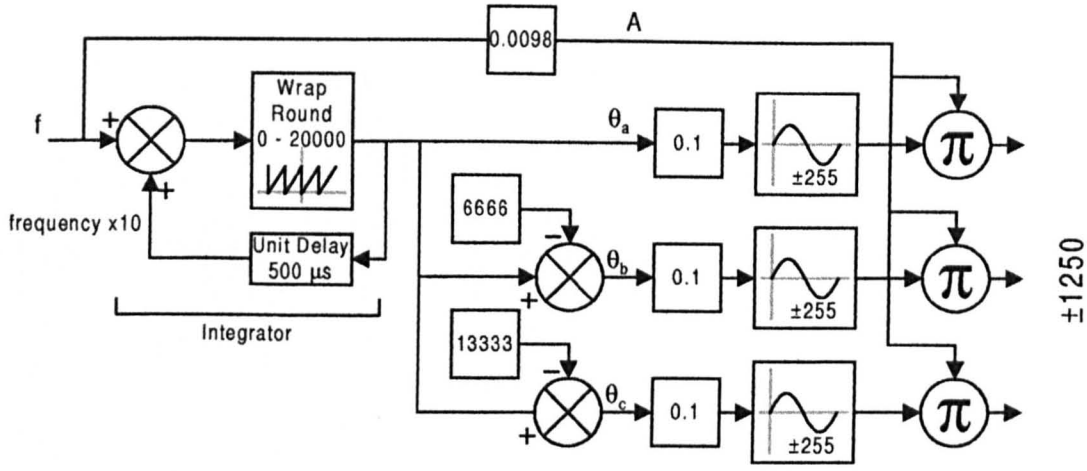

Figure 3.14 : *Block Diagram for Pulse Timing*

The microcontroller used for the implementation contains a pattern generator that will compare a loaded value with a sawtooth wave [1]. The crossovers then clock a flip-flop to produce the final pattern. During each PWM cycle the values are loaded with either rising or falling edge times before the next values are calculated. A 2 kHz cycle therefore produces a 1 kHz asymmetric pattern. Figure 3.15 shows the cycle for one PWM signal.

Each phase uses two channels of PWM, one for the upper carrier, one for the lower. The microcontroller has to generate a total of 6 channels for the full inverter. The calculation of T_{high} is simple, since it is directly proportional to the desired modulation value. The timers are then loaded with the appropriate value depending on the required edge direction (rising or falling).

Problems arise from the zero crossing in the modulation wave where the switching changes to the other carrier. At any instant one of the carriers should not be initiating switching. The conventional technique that is used to stop switching events on a conventional inverter when the modulation reaches the carrier limit is the implementation of pulse dropping.

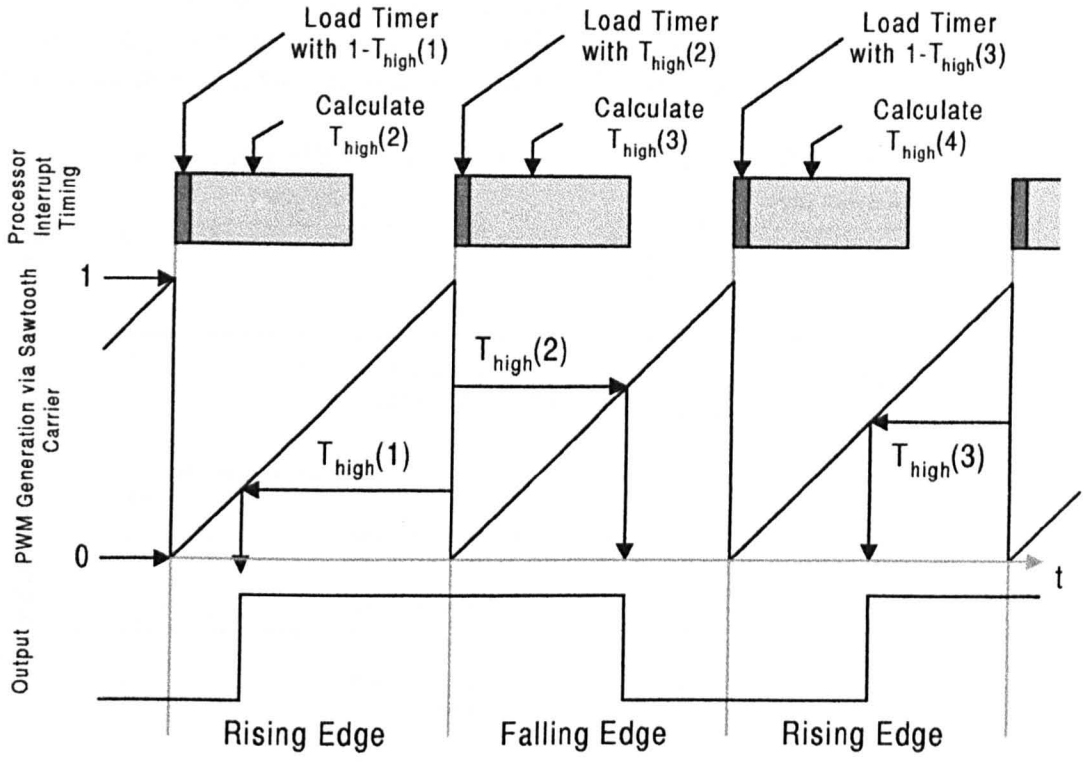

Figure 3.15 : *PWM cycle*

With the switching frequency of 1 kHz, the changeover into pulse dropping needs to be designed to avoid distortion, as well as being able to handle the carrier changeover. In order for this to be achieved the switching decision not only depends on the current edge direction and modulation value, but also the previous condition.

Table 3-2 shows the possible combinations that can occur for a particular carrier. Because pulse dropping can remove the switching edge in a particular cycle, it is possible for the next cycle to start from either state (low or high) irrespective of the new edge.

Edge Type	T_{high} value	Previous PWM state
Rising	< Minimum	High
		Low
	OK	High
		Low
	> Maximum	High
		Low
Falling	< Minimum	High
		Low
	OK	High
		Low
	> Maximum	High
		Low

Table 3-2 : *Possible switching conditions*

As the table shows, there are actually 12 different conditions that can occur. Because the calculation of the edges occurs during the previous half cycle, it is possible to reinstate a dropped edge before the start of the next half cycle. This greatly improves the entry and exit from pulse dropping. The responses to the rising edge conditions are shown in figure 3.16.

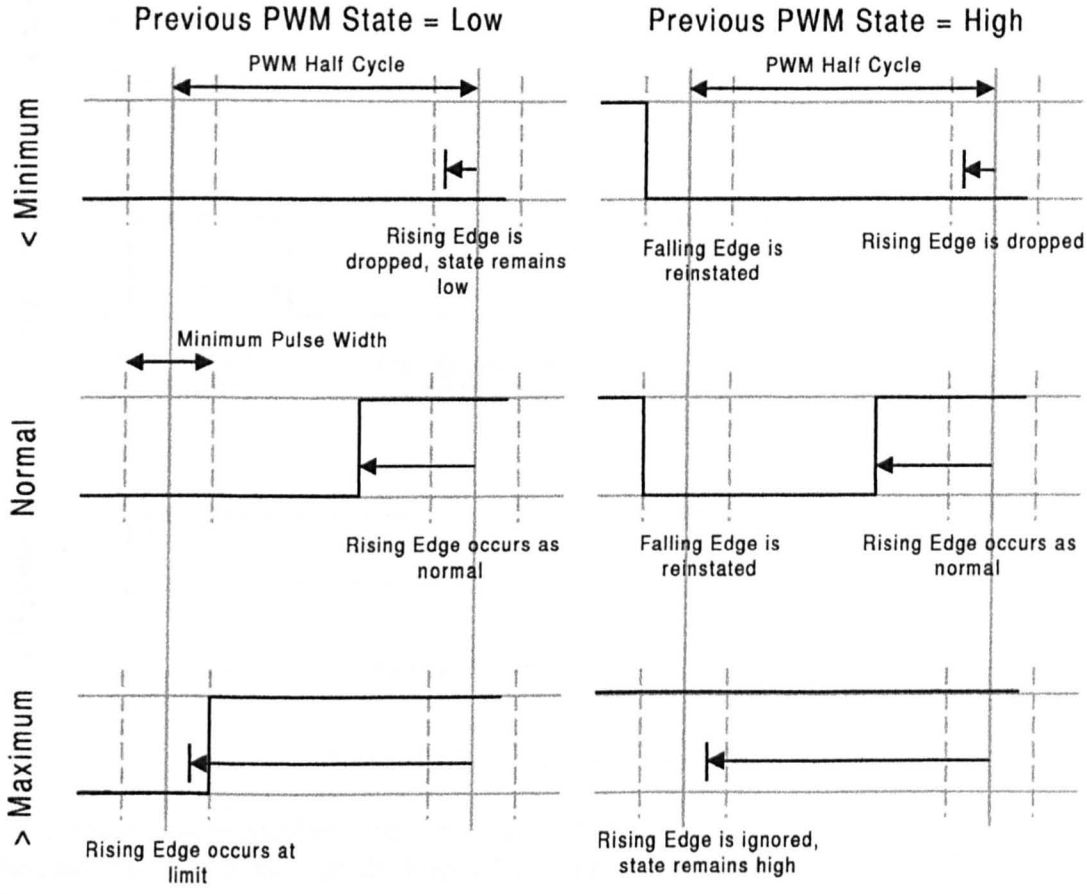

***Figure 3.16** : Rising edge conditions*

In two of the conditions (when the previous PWM state was high) a dropped falling edge has been reinstated at the switching time limit of the previous cycle. This allows the correct average voltage to be obtained over the new half period. The falling edge has a similar set of conditions, and these are shown in figure 3.17.

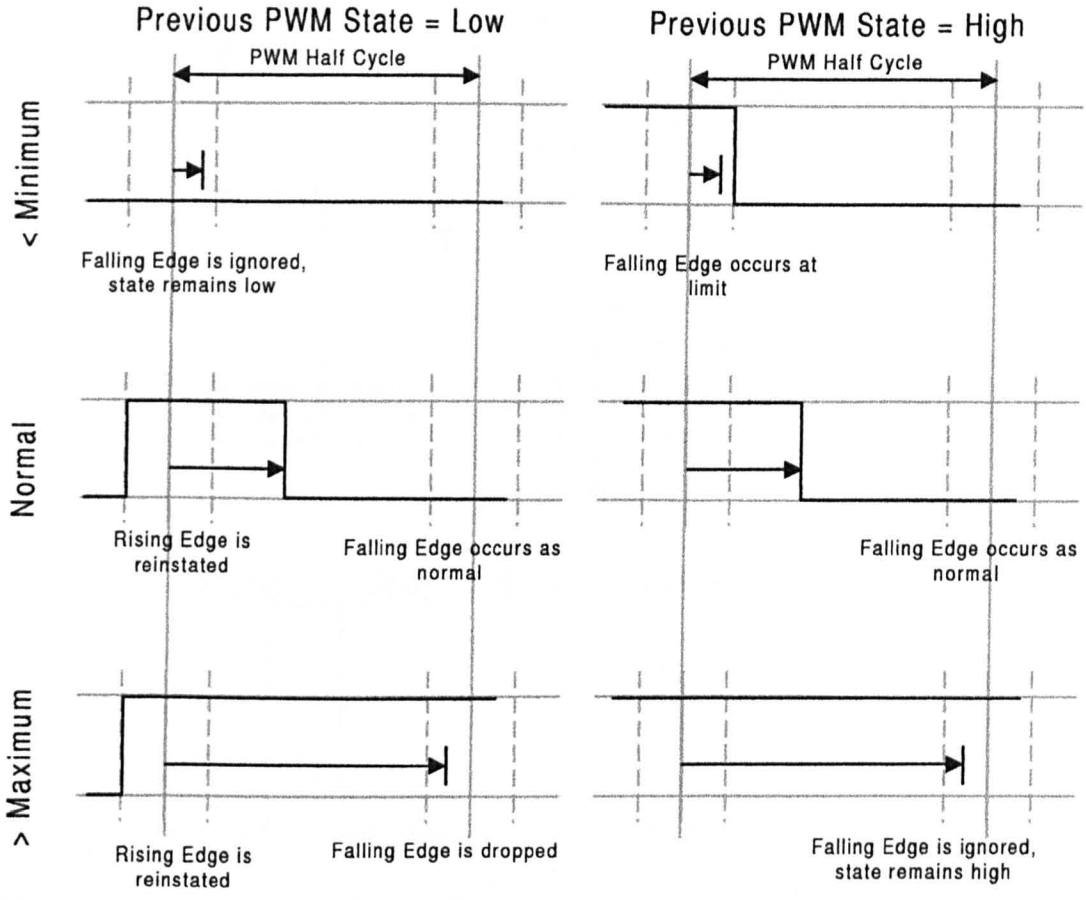

Figure 3.17 : *Falling edge conditions*

By applying these conditions to our combined carriers it can be seen that the system manages the changeover quite successfully. Figure 3.18 shows two typical changeovers. These are for the same modulation values, but with different carrier phases. The first example simply enters pulse dropping with a minimum pulse edge on the upper carrier, whilst the lower carrier completes its natural falling edge. It is in the second example that the benefit of the technique is visible. Here the modulation crosses over against the natural phase of the carriers. Without the insertion of the switching edge in period 3, the fundamental output would be distorted.

In both examples there are two separate switching points in the same half cycle. One event for each of the two devices. These will not occur at the same time unless the modulation steps from full positive to full negative within one half cycle. This would not occur with normal PWM operation, so the system is protected from simultaneous switching. If a very fast transient is required then the output pattern has to be protected from switching simultaneously. This will be addressed for the five level inverter in chapter 4.

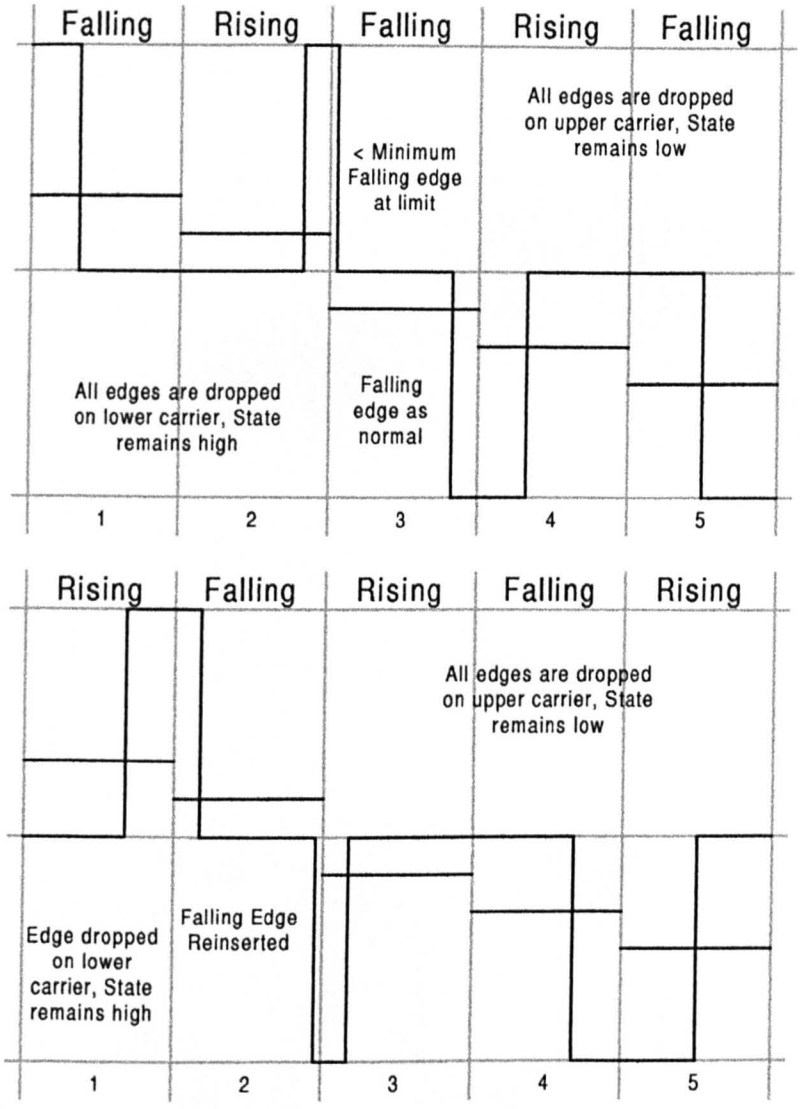

Figure 3.18 : *Carrier changeover examples*

3.4.2 Results

The basic PWM strategy was initially tested on a small 1.5kW induction motor. During these initial tests the capacitor mid-point was connected back to the supply neutral to provide voltage balance. The following figures show basic test results taken whilst commissioning the inverter operation.

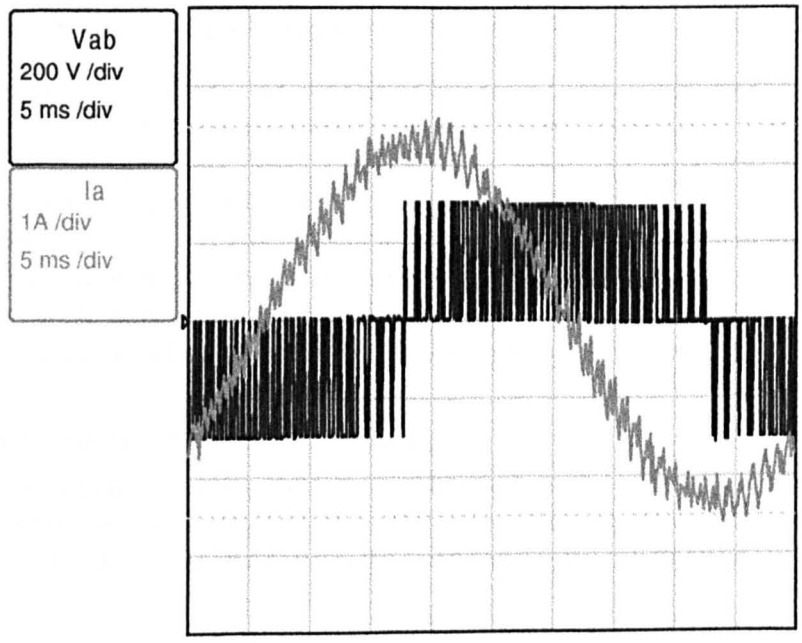

Figure 3.19 : *Line current and voltage at 20 Hz*

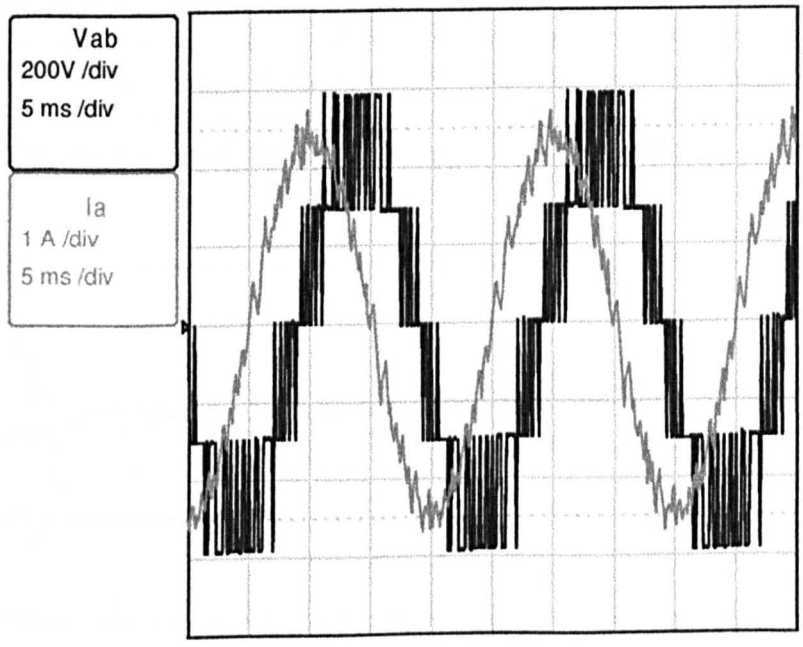

Figure 3.20 : *Line current and voltage at 50 Hz*

3.4.3 Discussion

The technique presented here produces a simple sub-harmonic PWM pattern. By using a look-up table for the modulation pattern, any predetermined shape can be used, so third harmonic can be easily added for example. Pulse dropping has been implemented, with careful control of the switching combinations. This allows simple and safe changeover between carriers.

3.5 Neutral Point Control Implementation

During the testing of the PWM, the inverter was operated with the neutral point connected back to the supply neutral. This connection forces the capacitor voltage balancing at the cost of an increase in voltage ripple. Whilst this was a necessary step to allow the PWM to be evaluated, it is not desirable. In the theoretical analysis given earlier in the chapter (Section 3.2.2, equations 3.8 to 3.11), it was shown that the mean current drawn from the midpoint by the inverter is expected to be zero, so the capacitors should remain balanced. In practice this is unlikely to be the case, and some form of regulation will be required. The first question that has to be examined is how close to the ideal analysis is the inverter?

3.5.1 Operation with the Neutral Point floating

Without any other changes to the operating conditions from the initial test of the PWM, the neutral connection was removed, and the inverter operation examined in a number of test conditions. Parallel discharge resistors on the capacitor bank provided a minimal balancing effect.

Figure 3.21 shows a conventional ramp acceleration of an induction motor up to an output frequency of 25 Hz. The upper graph shows the voltages on the upper and lower capacitors, with the output frequency shown on the lower graph. The initial conditions are not perfect, and an offset is visible in the voltages. This variation is due to the tolerance on the parallel sharing resistors. As the motor is accelerated, the steady state conditions used in the analysis do not apply, and difference between the capacitor voltages steadily increases. Once the motor reached the desired speed, the voltage difference remained constant.

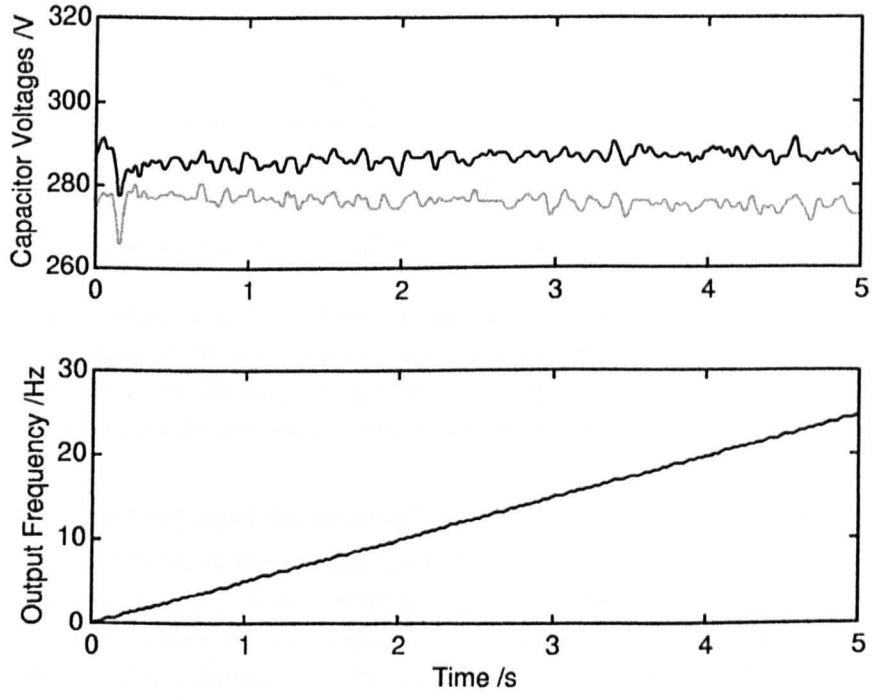

Figure 3.21 : *Neutral point variation during acceleration*

Testing showed that in one particular steady state condition the capacitor voltages diverged. This was at zero frequency, when voltage boost is applied to keep the induction machine in a

fluxed condition. There was sufficient error in the switching, or the phase currents, to generate a neutral point current and cause the capacitor voltages to diverge. The results from a deceleration test to zero speed can be seen in figure 3.22. The capacitor voltages remains reasonably stable (although with an offset) during deceleration, until zero frequency is reached. At this point the voltages begin to diverge, and this results in a protection trip due to over-voltage on one of the capacitors.

It is not surprising that the worst case condition was zero frequency. Errors in the switching that produce a voltage imbalance often cancel out over a modulation cycle, and do not produce a mean current. Errors at zero frequency will accumulate to produce the divergence in the capacitor voltages.

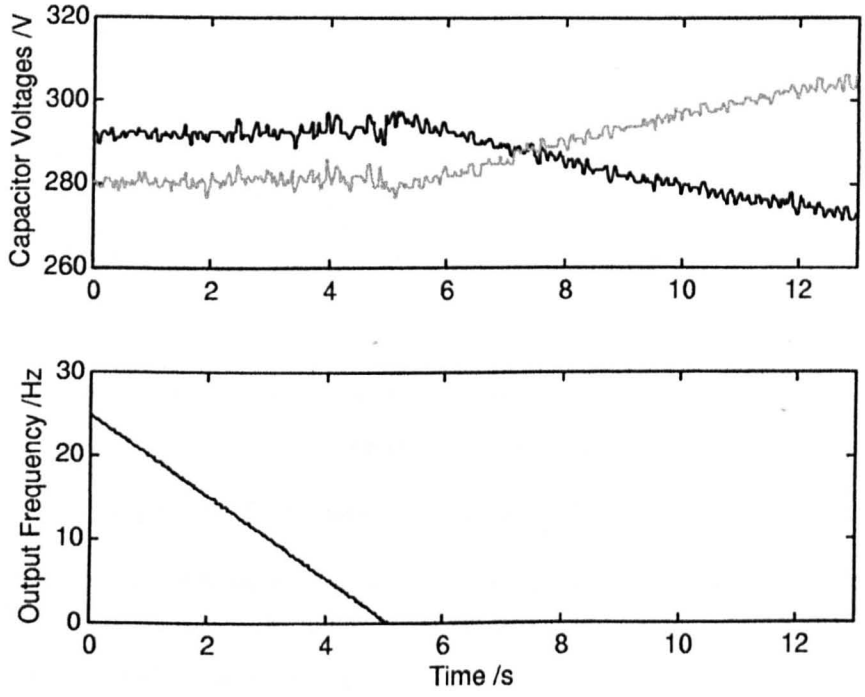

Figure 3.22 : *Deceleration to zero without neutral point control*

The tests have confirmed that if the voltages are to remain balanced, then some form of regulation is required. Several papers have suggested that regulation can be implemented through additions to the PWM strategy [2,3]. This is preferable to the addition of extra power circuitry if control can be achieved over the full operating range of the drive.

3.5.2 Theoretical analysis of the proposed Neutral Point Control technique

For space vector PWM, several authors [4,5] have demonstrated neutral point control. In the basic description of space vector techniques given in chapter two, it was stated that it is possible to obtain many of the output vectors from several different switch states. The selection of these redundant states does not impact on the output waveform, but does change the mapping of the load current through the capacitor bank. Controlled selection of the switching state is a necessary condition of operation

In the case of the sub-harmonic PWM technique that has been employed in the inverter, the modulation wave is symmetrical between the upper and lower carriers. The effect of this is to

equally share the power flow across the capacitor bank. If an offset is added equally to the three modulation waves then the symmetry will be lost. In a similar way to the redundant state selection in the space vector technique, the output is not affected if viewed phase to phase, but the current flow through the DC link will have changed. The addition of an offset to the modulating waves is shown in figure 3.23.

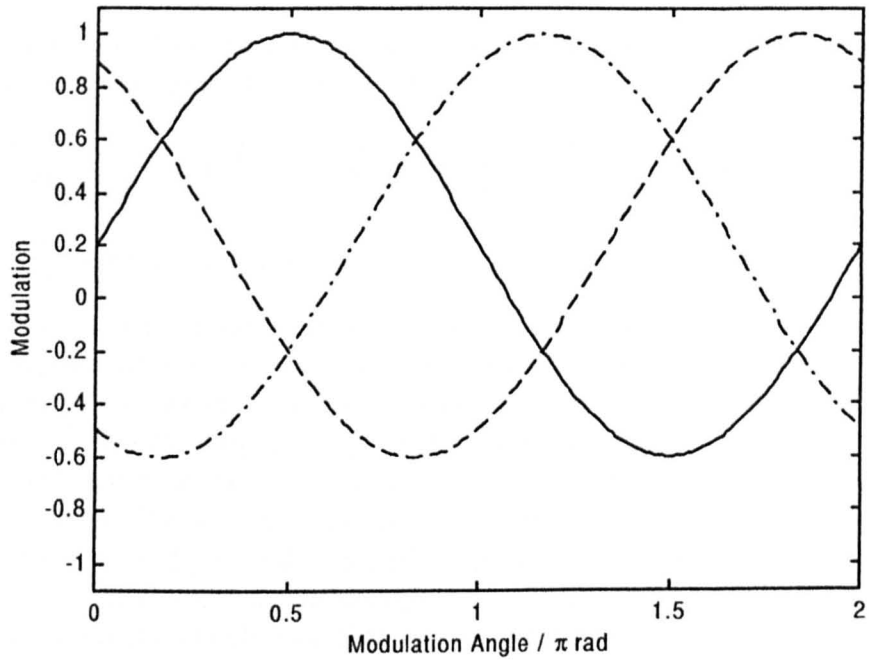

Figure 3.23 : *Modulation waves with DC component δ=0.2*

Following the same mathematical analysis technique used in section 3.2.2, new modulation functions can be defined which include the additional offset (which is given the symbol δ).

$$Modulation(\theta) = A\sin(\theta) + \delta \qquad [3.23]$$

$$neutral(\theta) = \begin{cases} 1-(A\sin(\theta)+\delta) & -\sin^{-1}\left(\frac{\delta}{A}\right) \le \theta < \pi + \sin^{-1}\left(\frac{\delta}{A}\right) \\ 1-(A\sin(\theta)+\delta) & \pi + \sin^{-1}\left(\frac{\delta}{A}\right) \le \theta < 2\pi - \sin^{-1}\left(\frac{\delta}{A}\right) \end{cases} \qquad [3.24]$$

Integrating the product of the modulation function and the phase current then derives the mean neutral point current. The offset changes the zero crossing points of the modulation wave, and thus changes the limits for the integration.

$$\overline{I_{neutral}} = \frac{1}{2\pi}\left[\int_{\alpha}^{\beta}\left(\hat{I}\sin(\theta+\phi)\right)\left(1-A\sin(\theta)-\delta\right)d\theta + \int_{\beta}^{\gamma}\left(\hat{I}\sin(\theta+\phi)\right)\left(1+A\sin(\theta)+\delta\right)d\theta\right] \qquad [3.25]$$

$$\alpha = -\sin^{-1}\left(\frac{\delta}{A}\right)$$

Where $$\beta = \pi + \sin^{-1}\left(\frac{\delta}{A}\right) \qquad [3.26]$$

$$\gamma = 2\pi - \sin^{-1}\left(\frac{\delta}{A}\right)$$

Solving this integral and substituting the limits yields equation 3.27. For simplification this will be quoted in the form of equation 3.28.

$$\overline{I_{neutral}} = -\left[A^2 \sin^{-1}\left(\frac{\delta}{A}\right) + \delta\sqrt{A^2 - \delta^2}\right]\frac{\hat{I}\cos(\phi)}{A\pi} \qquad [3.27]$$

$$\overline{I_{neutral}} = K(A,\delta)\hat{I}\cos(\phi) \qquad [3.28]$$

The function K(A,δ) becomes complex in the condition δ>A. This limit condition is the saturation point, when the offset exceeds the modulation amplitude. Once this condition has been exceeded the modulation wave no longer passes through zero. The current loading of the capacitors is now completely biased to either the upper or lower capacitor. Further increasing the offset can have no effect. At this limit both the square root and the inverse sine become complex. The only real component comes from the inverse sine which tends to π/2. This results in the real part of K(A,δ) tending to A/2. The complex nature of the equation is purely a mathematical state. Numerical calculation using a discrete time step integration (see appendix 2) produces a result equal to the real part of the algebraic solution.

Figure 3.24 shows the real part of K(A,δ) plotted against δ for the condition A=0.6. There is a clear linear region through δ=0 that extends to the saturation limits of δ=±0.6.

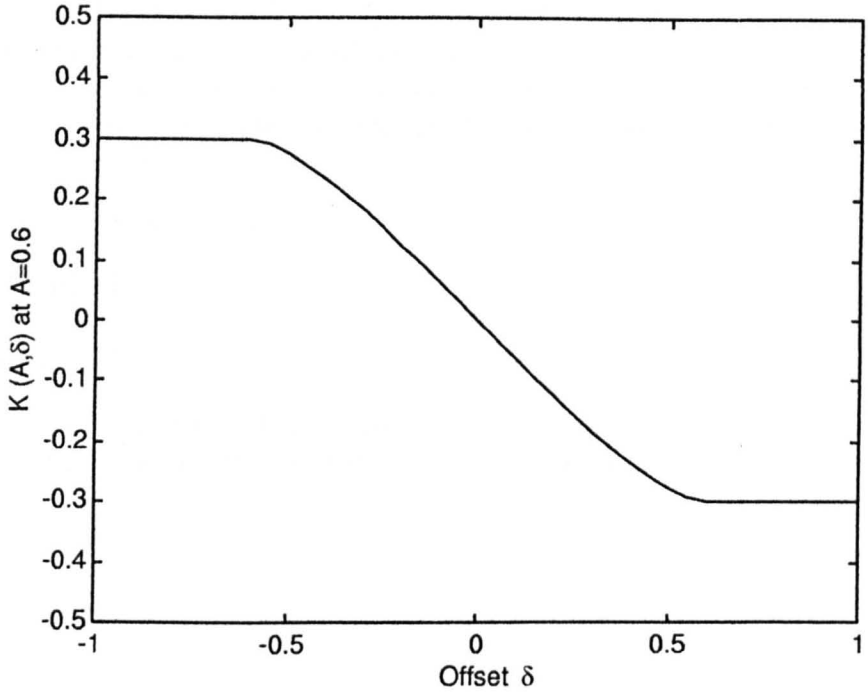

Figure 3.24 : *Plot of* $K(A,\delta)$ *against* δ *for* $A=0.6$.

The equation for K can be plotted as a three dimensional surface against the two variables δ and A. This is shown in figure 3.25. The linear region observed in figure 3.24 becomes a planar region in three dimensions.

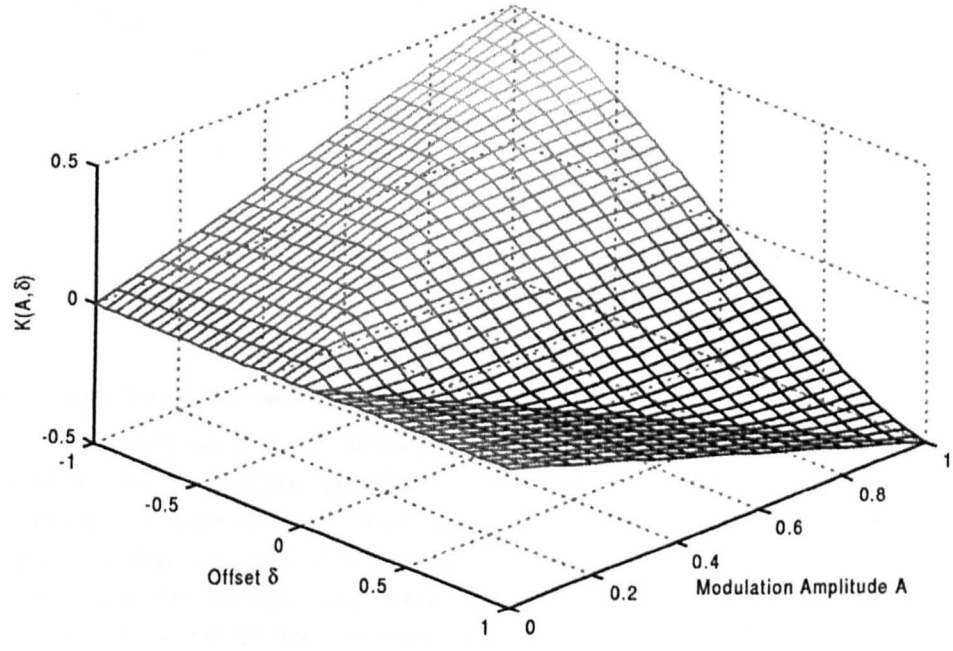

Figure 3.25 : *Surface Plot for* $K(A,\delta)$

The analysis used for the derivation of K has been based on a simple mathematical function for the modulation function. The analysis assumes that any value of offset can be added to any particular amplitude of sinusoid. In practice the modulation function is bounded (The inverter can only generate a limited amplitude) and clipping will occur if the offset is too large. If the output is to remain undistorted, then the addition of an offset is limited by the following condition.

$$-1 \leq (A\sin(\phi) + \delta) \leq 1 \qquad [3.29]$$

$$A + |\delta| \leq 1 \qquad [3.30]$$

$$|\delta| \leq 1 - A \qquad [3.31]$$

Applying this limitation condition to the surface plot, then a large area is removed from the operating range. The modified surface plot is shown in figure 3.26.

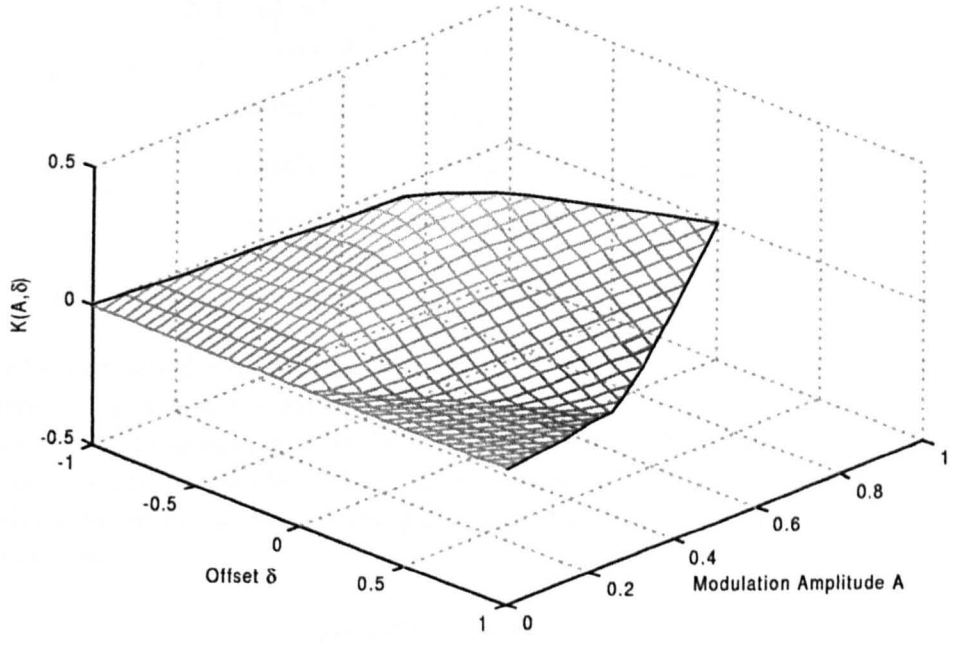

Figure 3.26 : *Surface Plot of the permitted region for* $K(A,\delta)$

3.5.3 Control Design for Neutral Point Control

In the original analysis, it was shown that the capacitor voltages should remain constant, and this was confirmed in practice apart from certain specific operating conditions. The addition of a controller is required to maintain the equal voltage operating point. This defines the control to be regulatory. From the equations, the basic operating point can be defined as $\delta=0$, since the capacitor voltages are basically stable. Following classical control design techniques, it is possible to linearise the function K about the operating point by deriving the small signal model. The small signal gain equates to the slope of the planar surface with respect to δ.

$$\frac{dK(A,\delta)}{d\delta} = -\frac{1}{A\pi}\left[2\sqrt{A^2-\delta^2}\right] \qquad [3.32]$$

$$\Delta K = \frac{dK(A,\delta)}{d\delta}_{\delta=0}\Delta\delta + K(A,\delta)_{\delta=0} \qquad [3.33]$$

$$\Delta K = -\frac{2}{\pi}\Delta\delta \qquad [3.34]$$

Equation 3.34 provides the basis for implementation of a control strategy. The mean neutral point current is proportional to the applied offset, for a given load current, and is independent of the modulation. It is limited however by the saturation conditions, and modulation wave bounds in equation 3.31. Figure 3.27 shows the adaptation of the modulation strategy to include the neutral point controller.

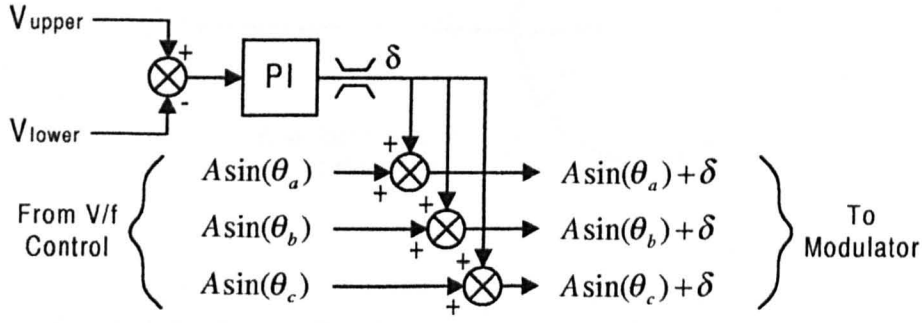

Figure 3.27 : *Block diagram for the addition of the controller to the modulation*

The effective closed loop control model is shown in figure 3.28. The two capacitors are combined to give a single integrator, with the feedback being the voltage difference. The dependence of the system gain on the load current amplitude and power factor complicates the control loop. An absolute value for the closed loop gain cannot be defined without knowledge of the motor current. The gain block of $6/\pi$ represents equation 3.34 for a three phase inverter.

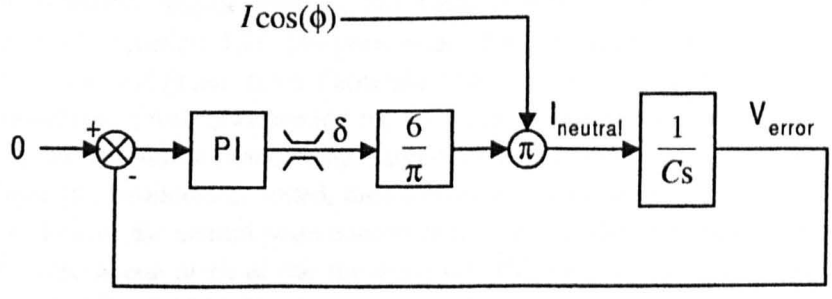

Figure 3.28 : *Control loop model*

Equation 3.28 showed that the neutral point current was dependent on the motor current. This is represented by a multiplier in the above control loop. On the three level prototype inverter, a measure of the motor current was not available to the microprocessor. By defining the operating range for the inverter, it is possible to characterise the system. Since the prototype did not employ a regenerative brake unit on the DC link, the drive was limited to motoring quadrant operation. The term in the equation, being the product of current amplitude and

power factor, relates to the neutral point current to the power flow from the inverter to the motor. If the motor current term becomes negative (as occurs in regeneration), the multiplier creates positive feedback in the control loop, making the system unstable. The control loop can be designed for motoring condition on the basis that the system gain will vary over a defined range set by the current rating of the drive (the no load, and full load operating conditions). Figure 3.29 shows the root locus for an example system.

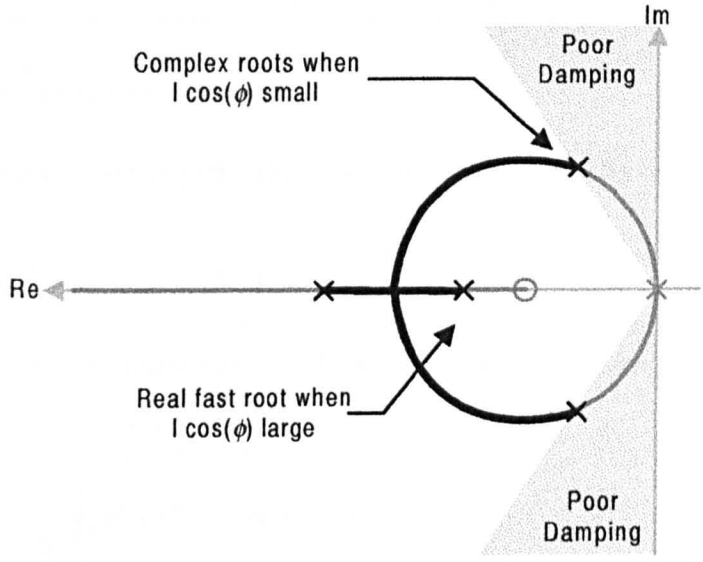

Figure 3.29 : *Control Root Locus showing an example operating range*

Design of the PI controller is fairly simple, as the plant is effectively a simple integrator. Placement of the zero will define the general order for the natural frequency. With the gain of the plant being variable, the controller gain defines the operation over a region of the root locus. The system gain should be set for stability in the no load condition. Bandwidth and damping will both improve under load.

3.5.4 Operation range improvement by third harmonic addition

The control technique cannot work in this form at full modulation due to the clipping limitations given in equation 3.31. The peak value of the modulation function can be reduced by addition of an anti-phase third harmonic. The addition of a third harmonic to the modulation function is well documented for conventional inverters, normally as a technique for increasing the maximum fundamental amplitude at the output. If the fundamental is not increased when the harmonic is added, then freedom is obtained to include an offset at full modulation and allow the neutral point controller to operate. The amplitude of third harmonic added in this case is one ninth of the fundamental. This represents the condition where the peak of the modulation will be flat. For maximum fundamental boost a value of one sixth is normally used [6].

Applying the third harmonic to the modulation pattern, and repeating the earlier analysis produces the following equation for the neutral point current.

$$\overline{I_{neutral}} = \frac{1}{2\pi}\left[\int_{\alpha}^{\beta}\left(\hat{I}\sin(\theta+\phi)\right).\left(1-A\sin(\theta)-\frac{A}{9}\sin(3\theta)-\delta\right)d\theta + \int_{\beta}^{\gamma}\left(\hat{I}\sin(\theta+\phi)\right).\left(1+A\sin(\theta)+\frac{A}{9}\sin(3\theta)+\delta\right)d\theta\right] \quad [3.35]$$

In the original analysis the integration ranges were simple to define. The mathematical definition for the new zero crossing with third harmonic added is given in equation 3.36.

$$A\sin(\theta)+\frac{A}{9}\sin(3\theta)+\delta=0 \quad [3.36]$$

Applying the standard trigonometric identities, equation 3.36 can be rearranged into cubic form.

$$-\frac{4A}{9}\sin(\theta)^3+\frac{4}{3}\sin(\theta)+\delta=0 \quad [3.37]$$

By substitution, the cubic equation can be solved, and the three roots are given below.

$$\sin(\theta)=\begin{cases}\dfrac{1}{\Pi}\left(\Pi^2+1\right)\\ -\dfrac{1}{2\Pi}\left[\left(\Pi^2+1\right)+j\sqrt{3}\left(\Pi^2-1\right)\right]\\ -\dfrac{1}{2\Pi}\left[\left(\Pi^2+1\right)-j\sqrt{3}\left(\Pi^2-1\right)\right]\end{cases} \quad [3.38]$$

$$\Pi=\sqrt[3]{\frac{9}{8}\cdot\frac{\delta}{A}+\sqrt{81\left(\frac{\delta}{A}\right)^2-64}} \quad [3.39]$$

The mathematical solutions that are derived are complicated, and a simple equation for the neutral point current cannot be easily derived.

Numerical analysis can again be performed to evaluate the operation. The result is shown as a surface plot in figure 3.30. The surface has changed only slightly, but the reduced peak modulation now allows a small δ to be added even at full modulation ($\pm 11\%$).

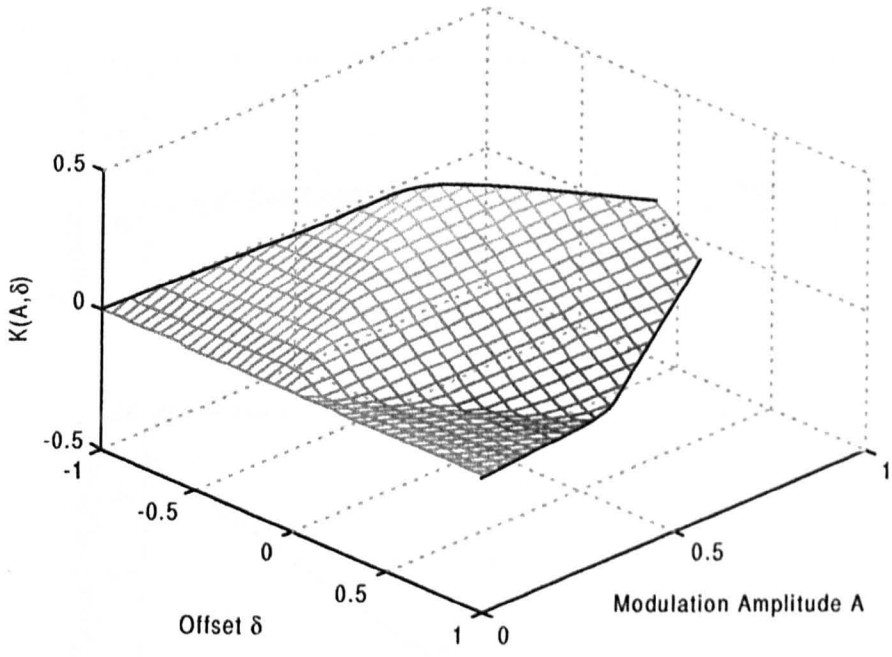

Figure 3.30 : *Surface plot when 3rd harmonic has been added*

3.5.5 Test Results for operation of neutral point control

With the neutral point control built into the open loop control strategy, its performance was evaluated through a series of tests. The first test checked operation at zero frequency (the unstable condition from figure 3.22). Figure 3.31 shows the result for the same operating test, but with the neutral point control active. It is clear from the trace that the two capacitor voltages are maintained equal.

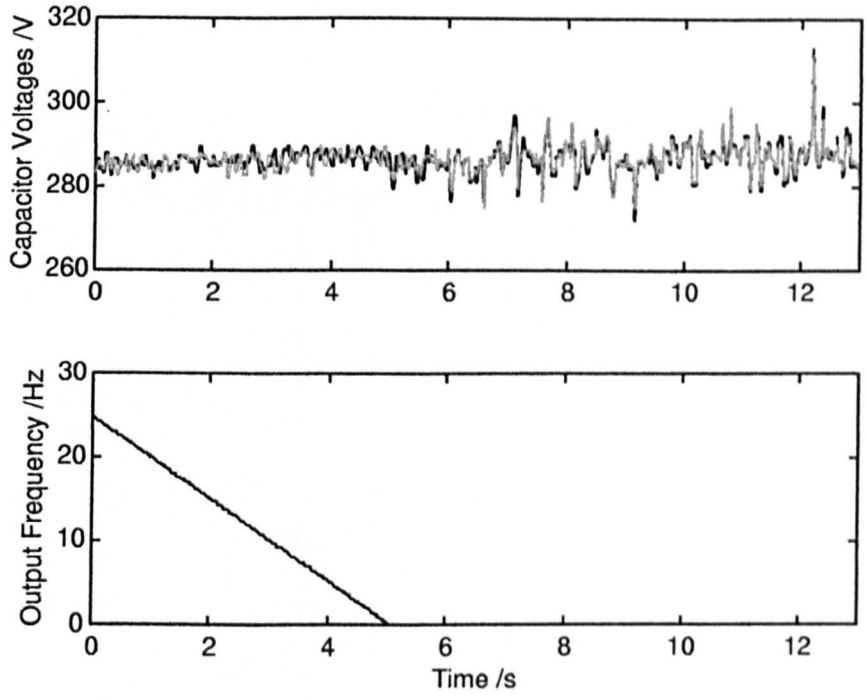

Figure 3.31 : *Deceleration to zero with neutral point control*

With the control system successfully maintaining the capacitor voltages, the control strategy was modified to allow a deliberate offset to be demanded from the controller. This is a condition that would not required in a practical converter, but does allow the step response of the control to be evaluated. Figure 3.32 shows a test cycle of the controller. From the initial balanced condition, both positive and negative offsets are demanded sequentially before the system is returned to normal. This test was performed whilst turning an induction motor at 25 Hz, with no external load torque applied.

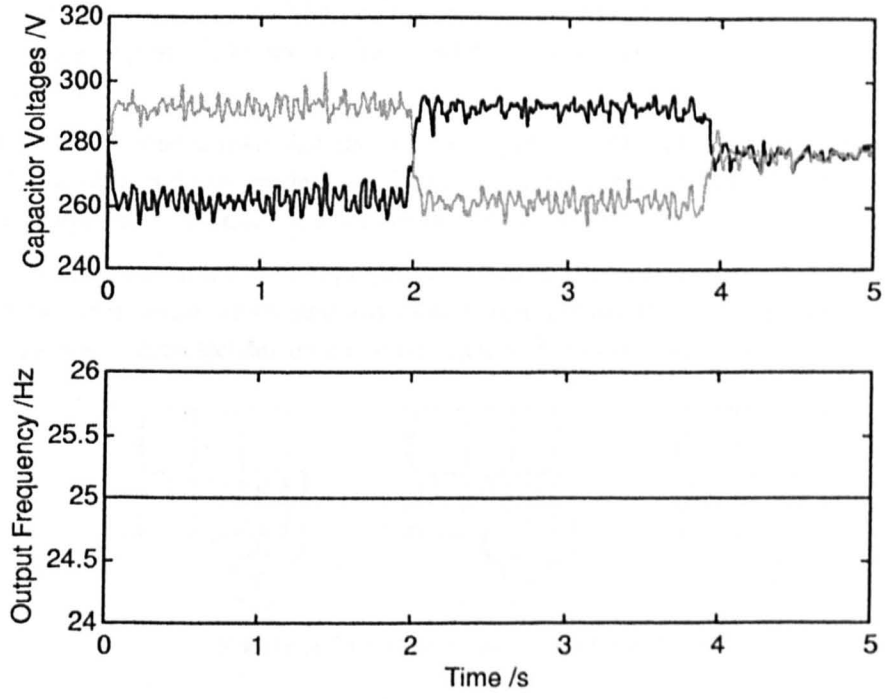

Figure 3.32 : *Offset step test for neutral point controller*

3.5.6 Comparison with Neutral Point Control based on SVM

In this chapter a technique has been presented to control the neutral point voltage using a modification to the conventional sub-harmonic PWM method. The most commonly published technique has been based on space vector modulation, so it is natural that some comparison should be made.

Neutral point control is implemented in SVM by controlling the selection of redundant switch states. The basic operation of SVM has been described in chapter two. Figure 3.33 shows an example vector, and the associated switch states.

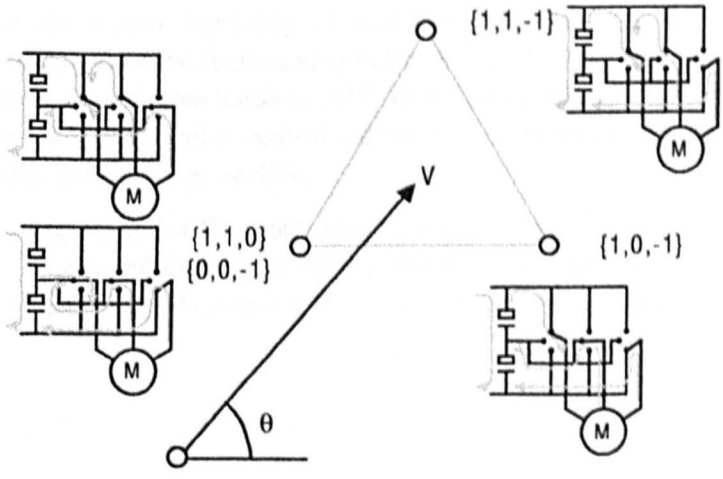

Figure 3.33 : *Redundant state effect on the neutral point*

As the figure shows, the selection of the particular redundant states influences the current drawn from the neutral point. The outer vectors do not allow any choice in the current drawn from the neutral point. The intermediate vectors do however allow the direction of current to be controlled.

In figure 3.30 it was shown that the neutral point control technique presented has limited capability at high and low modulation depths. Examining the SVM approach to neutral point control shows that it is similar limitations in these conditions.

At low modulation values, a high proportion of time is spent in the zero vector states. Since none of the zero vector states pass any current through the DC link capacitors, neutral point current cannot be effected during this time. This is shown in figure 3.34.

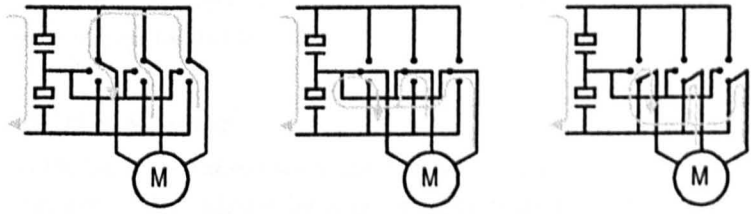

Figure 3.34 : *SVM states for the zero vector*

At high modulation values the majority of time is spent in the vectors on the edge of the vector map. Since there is only one state for these vectors, the ability to control the output current is also limited.

Knowledge of the current is a requirement in both strategies so that either the correct redundant state or offset is applied.

3.5.7 Conclusions and Discussion

A neutral point control technique has been presented, with complete mathematical analysis to describe the fundamental behaviour. The limitations of the control technique in its basic form have been given, and mitigated by the addition of simple solutions. Practical results have been provided which demonstrate the control in operation on the prototype inverter.

The addition of a third harmonic component to the modulation pattern is a standard technique used to increase the output capability of inverters. The flattening of the peaks in the modulation normally allows the fundamental to be increased. Using this technique the output magnitude can be increased from 0.866 to 0.977 of the input voltage. Using third harmonic to provide freedom for neutral point control means the fundamental output remains limited. This is addressed in the following section.

It is possible to compensate for the motor current term, giving control in both motoring and regeneration conditions, and defining a fixed operating point. This will be discussed during implementation of neutral point control on the five level inverter in chapter 5.

3.6 Extended operation range for neutral point control

It has been discussed in the previous section that neutral point control can be implemented via the addition of an offset into the modulation pattern, which was confirmed by practical results. This technique is limited for high modulation amplitudes by the limits of modulation defined in equation 3.31. This was partially overcome by the addition of a third harmonic to the modulation wave, but this left the fundamental modulation capability limited to 0.866 of the input voltage. If full power operation is to be obtained, then a third harmonic is normally added to an increased fundamental, which allows an output voltage ratio of 0.977. With an increased fundamental the neutral point controller is once again limited at full modulation.

A technique called "bus clamping" can be used to avoid non-linearities caused by pulse dropping on a conventional inverter. It also allows modulation waves to be generated that exceed the standard amplitude limits.

3.6.1 Principles of bus clamping

Looking at the modulation technique for a conventional inverter, pulse dropping is commonly used when the desired pulse widths become smaller than the minimum allowed for safe switching of the devices. This changeover introduces a step in the modulation wave from the minimum pulse limit to full modulation. In figure 3.35 the top graph shows the desired, and effective modulation waves when pulse dropping occurs. This is an extreme example for demonstration, with a large minimum pulse width. The effective line to line output is then shown in the lower graph.

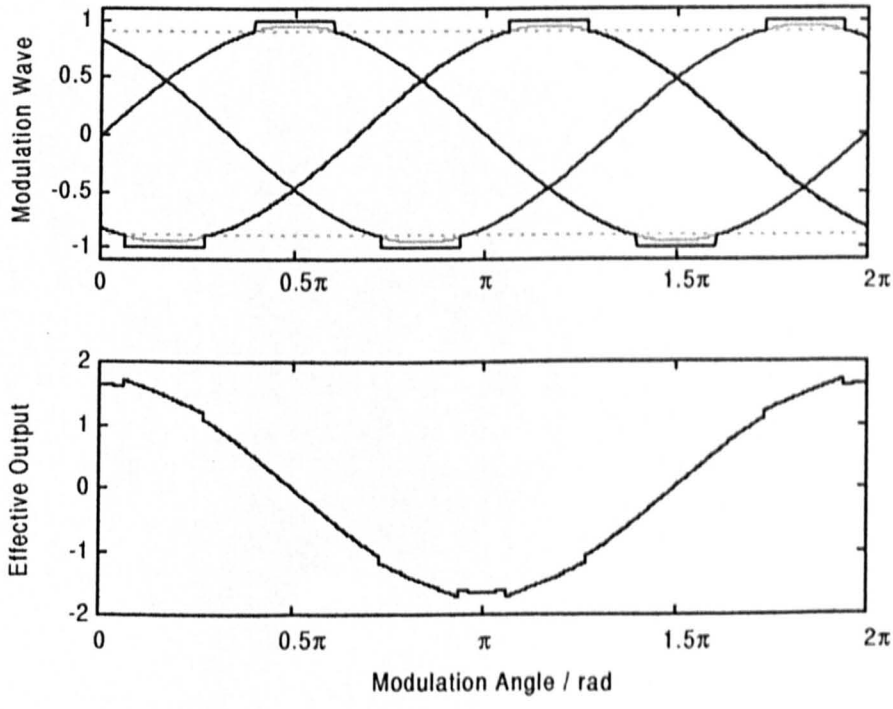

Figure 3.35 : *Effect of pulse dropping for a conventional inverter*

There is a clear distortion in the output that has been introduced by the pulse dropping. It was proposed that when pulse dropping is initiated, and the output is effectively clamped to the DC bus, then by compensating the modulation on the other phases the effective output can

remain undistorted. The modified modulation waves with compensation are shown in figure 3.36. It can be seen that the resulting line to line output pattern is now sinusoidal, and the distortion has been removed.

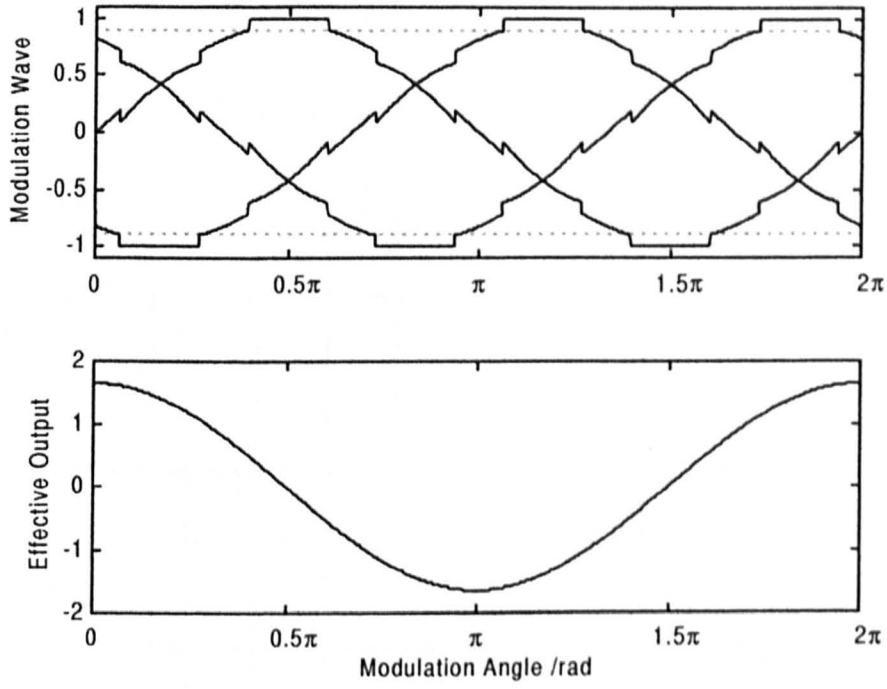

Figure 3.36 : *Bus clamping in operation*

3.6.2 Relationship of bus clamping to neutral point control

Examining the times where bus clamping has come into operation in figure 3.36, it can be seen that an offset has been added to each of the three phases. The size of the offset varies during the clamping period so that the clamped wave remains at the appropriate limit. This demonstrates that an output may be clamped to a particular level provided that it is compensated for in the other phases (so that the effective output remains the same).

The operation of the neutral point control described earlier was limited according to equation 3.31, which severely restricted the operation at high modulation amplitudes. Bus clamping allows distortion in one modulating wave provided it can be compensated for in the other phases. By applying this to the addition of an offset to the modulation wave, then when the limits are exceeded by a particular phase, the wave can be clamped. Provided that the lost voltage is compensated for in the other phases the output will be unaffected. A block diagram for this is shown in figure 3.37.

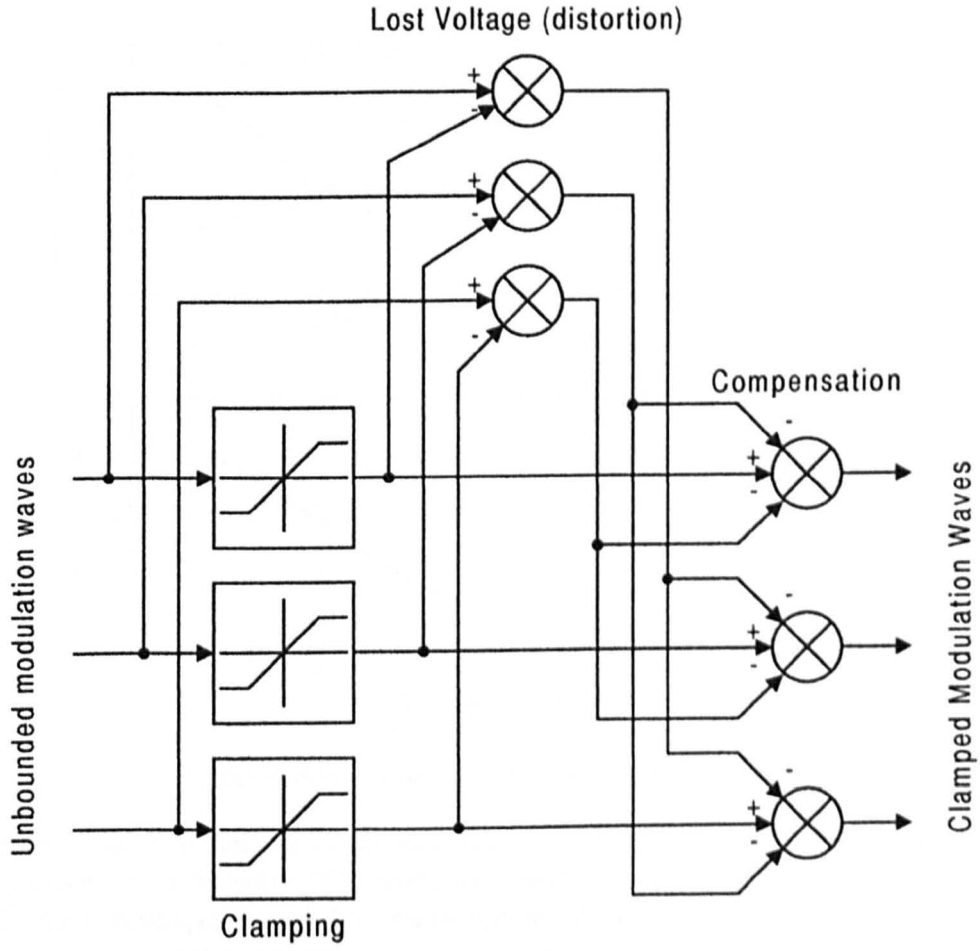

Figure 3.37 : *Clamping Block Diagram*

An example situation is shown in figure 3.38. The offset has pushed the top of the modulation pattern into clamping and the compensating component is then added to the other modulation waves. The output then remains undistorted.

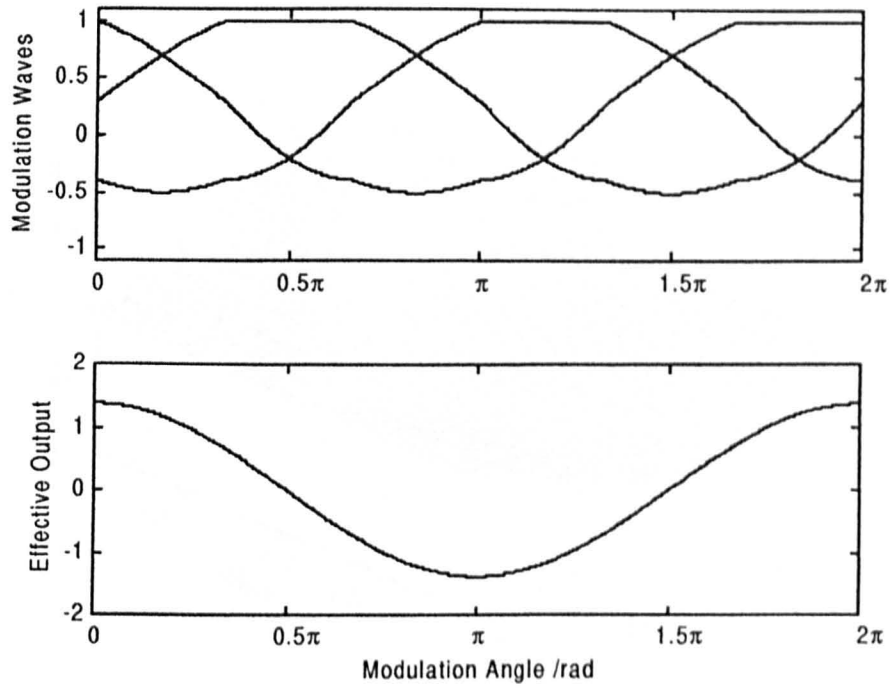

Figure 3.38 : *Neutral point control with clamping*

Examining the effect on the modulation waves, it can be seen that the offset has been modulated to avoid distortion. The modulation functions cannot be defined mathematically, so numerical techniques have to be used to find the effect on the neutral point current. Figure 3.39 shows the surface plot for the modified strategy.

With the modification applied, there is no longer a limit on the use of the surface due to the modulation limits. The shape of the new surface does introduce some limitations to the control range however. At high modulation amplitudes the surface begins to curve back on itself when the offset is increased to maximum. If the controller enters this region then instability will occur as increasing the offset actually decreases the neutral point current. The restrictions to avoid these regions are relatively small. Neutral point control can therefore be achieved even at full modulation with third harmonic injection and fundamental boosting.

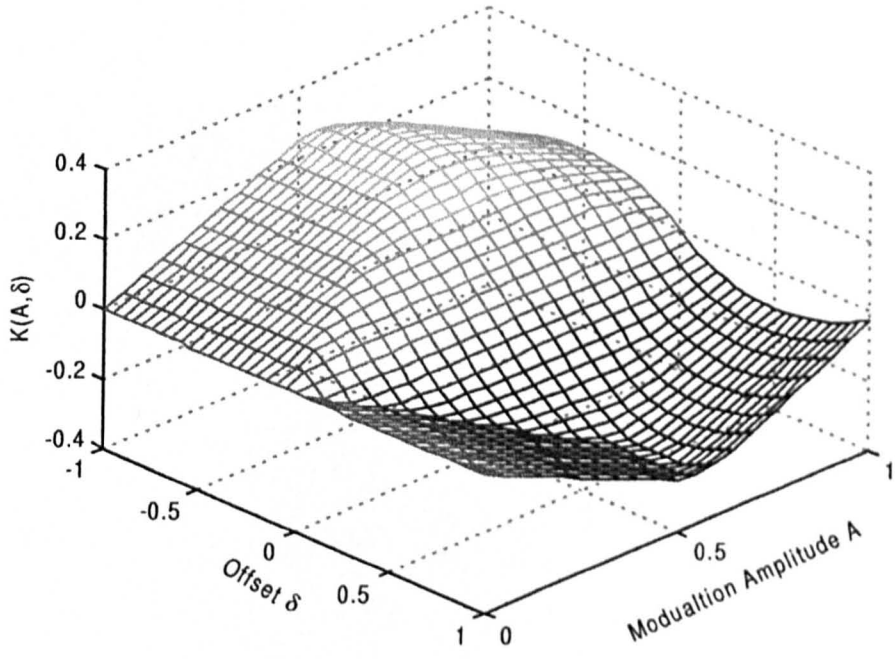

Figure 3.39 : *Surface Plot with clamping*

3.6.3 Discussion

The range extension technique described here was not implemented on the prototype three level inverter. The idea was developed during the construction of the five level prototype inverter. It has been included here for completeness since the technique is general and can be used whatever the number of levels. It has been practically implemented on the five level, and this will be presented in chapter 5.

3.7 Results from Practical Inverter

3.7.1 Test Results

The following sections show results from the operation of the 11kVA inverter driving a Mitsubishi induction motor coupled to a DC loading machine. The machine nameplate parameters are given in appendix 3. The drive was operated at 20, 30, 40 and 50 Hz both unloaded and with loading to the device current limit of 25A peak. Table 3-3 shows the basic meter results of phase voltage and line current from the tests.

Frequency /Hz	Load Condition	Phase Voltage / V_{rms}	Line Current / A_{rms}
20	No Load	108.1	6.09
	Loaded	107.8	17.74
30	No Load	132.1	6.02
	Loaded	130.0	17.60
40	No Load	170.4	6.02
	Loaded	164.9	17.50
50	No Load	207.6	6.07
	Loaded	194.5	17.62

Table 3-3 : *Results from inverter load tests*

The reduced voltages are due to the 0.866 factor in the output. This was necessary to avoid problems with the neutral point control at high modulation, as has been described in the chapter.

The following sections show the line to line output voltage and the line current captured via a digital storage scope, the no load and full load traces were taken at different times, and in some cases different timebases were used. Rather than modifying the data, the results are shown as they were recorded.

The data was post processed to produce harmonic spectra, and to calculate values for the total harmonic distortion percentage (THD). All the results are grouped according to output frequency.

3.7.2 20 Hz Output Frequency

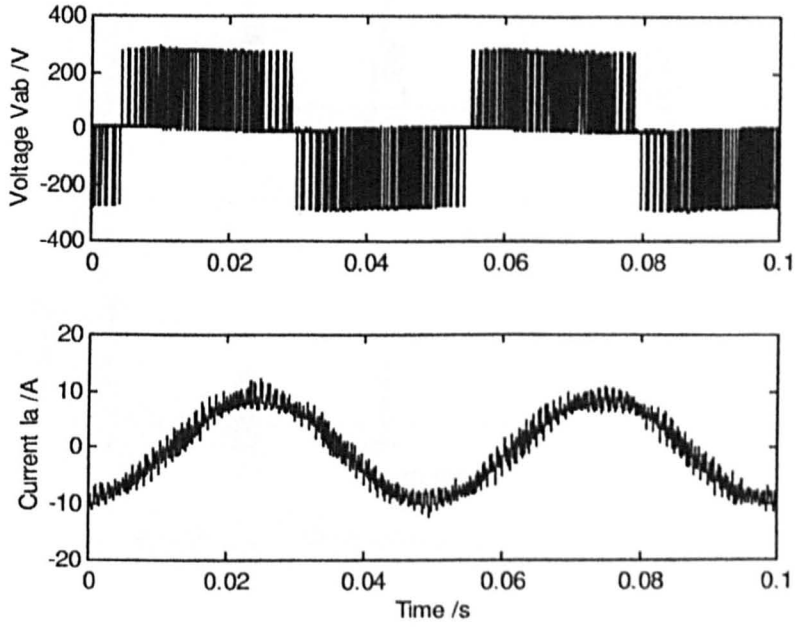

Figure 3.40 : *20 Hz No load operation*

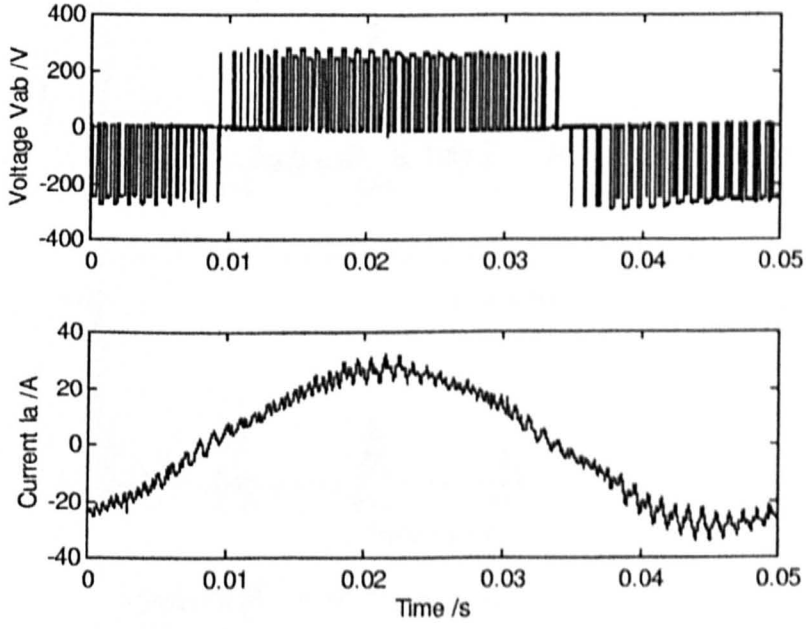

Figure 3.41 : *20 Hz Full load operation*

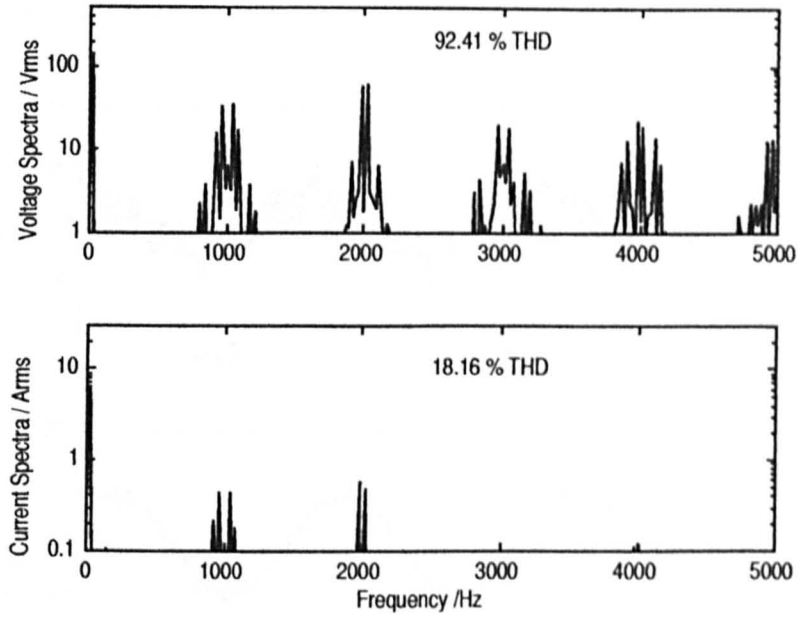

Figure 3.42 : *20 Hz Harmonics, no load operation*

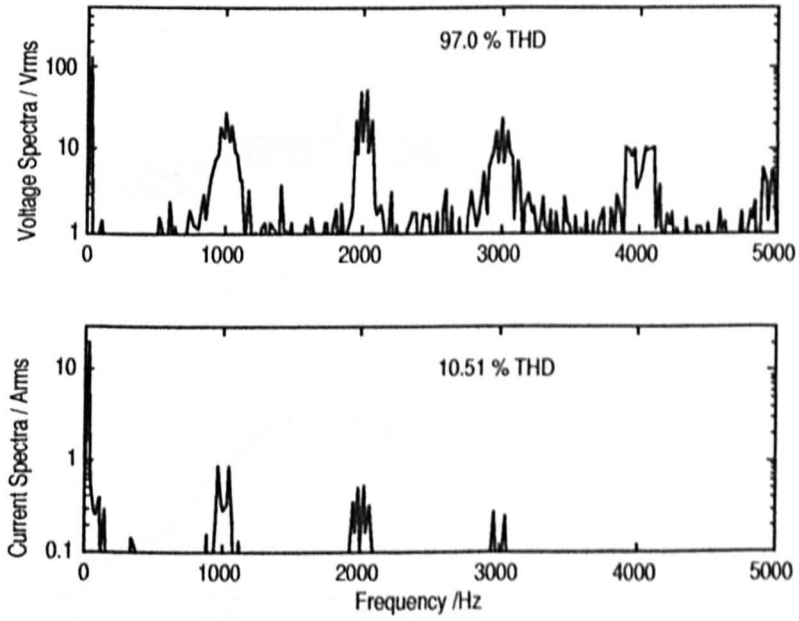

Figure 3.43 : *20 Hz Harmonics, full load condition*

3.7.3 30 Hz Output Frequency

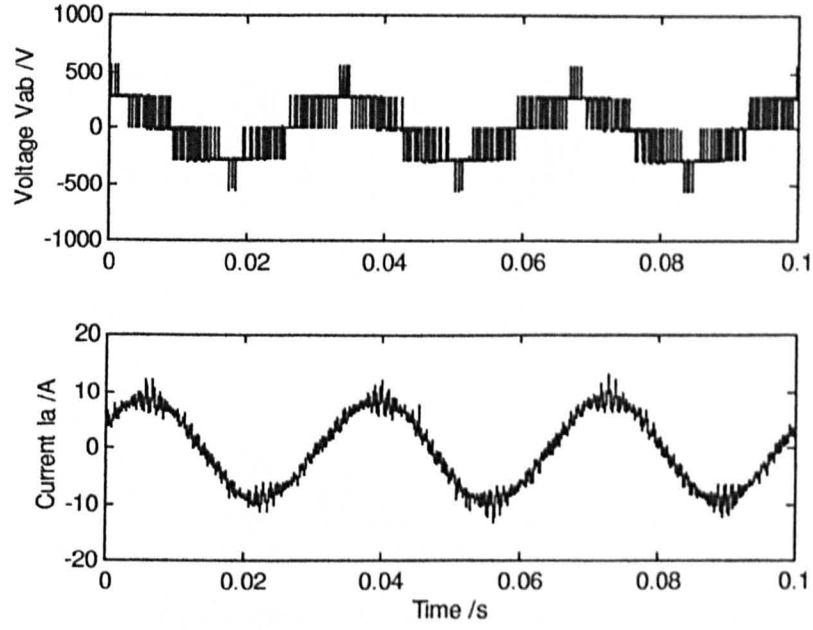

Figure 3.44 : *30 Hz No load operation*

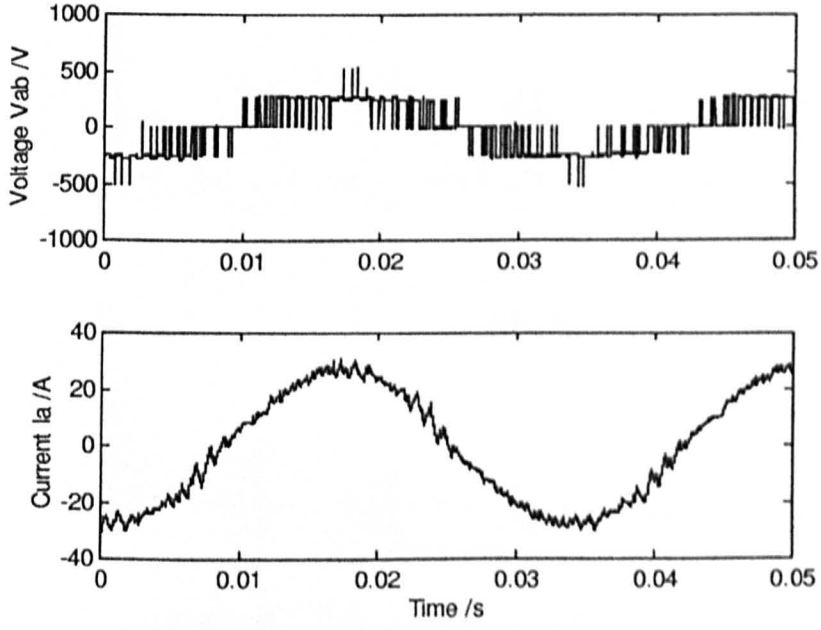

Figure 3.45 : *30 Hz Full load operation*

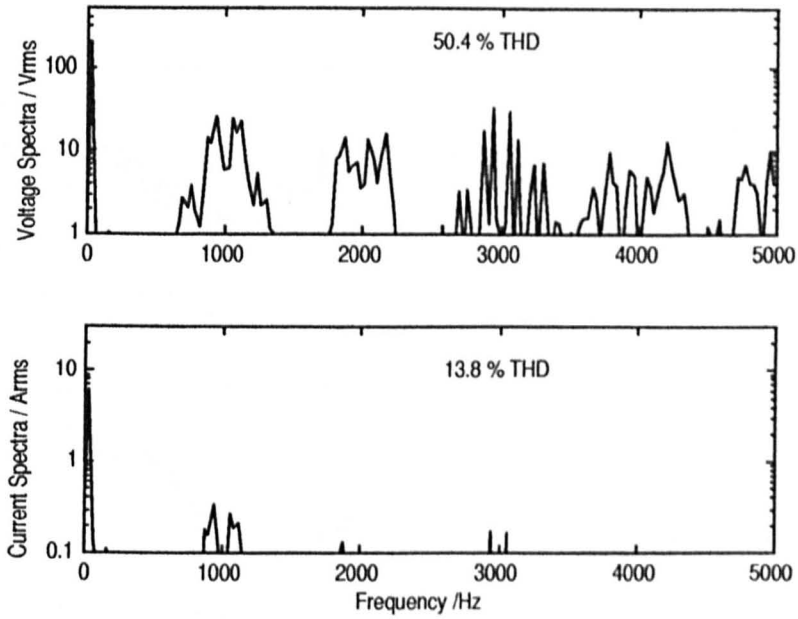

Figure 3.46 : *30 Hz Harmonics, no load condition*

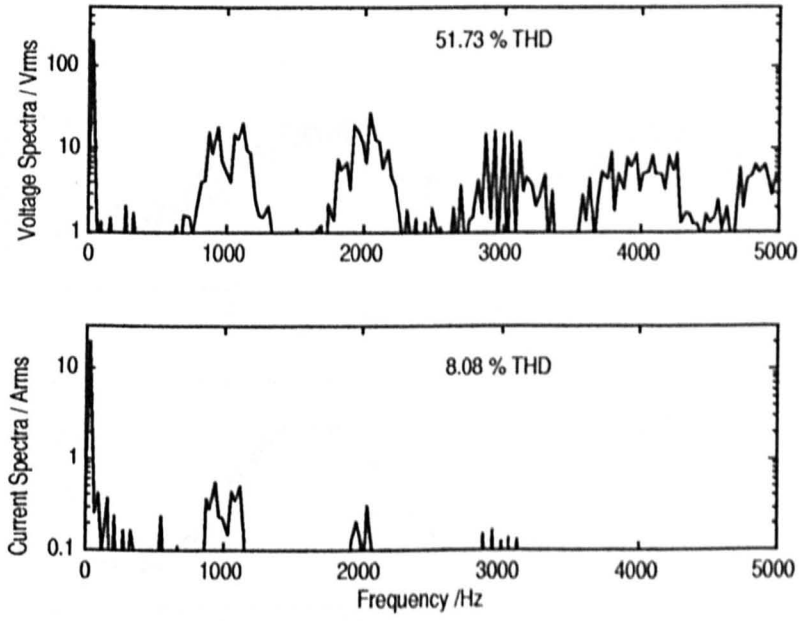

Figure 3.47 : *30 Hz Harmonics, full load condition*

3.7.4 40 Hz Output Frequency

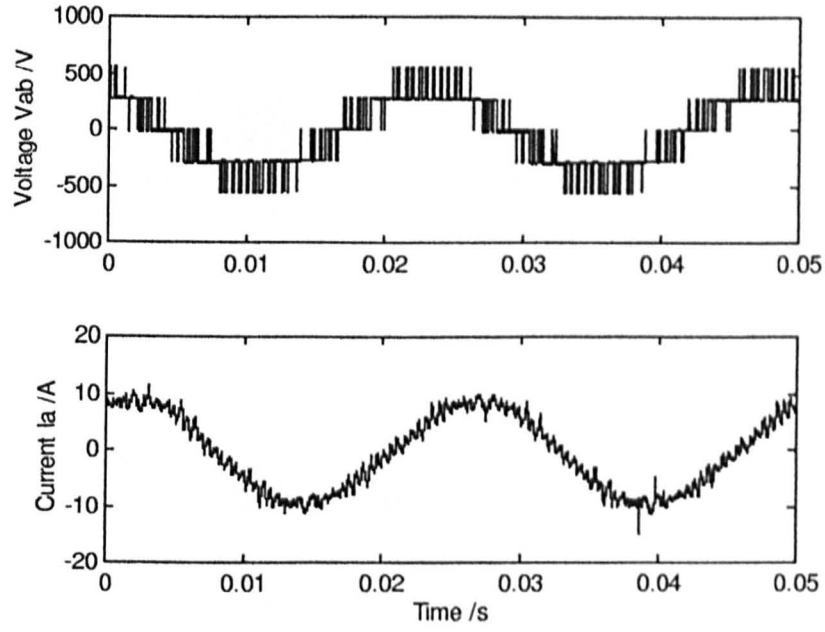

Figure 3.48 : *40 Hz No load operation*

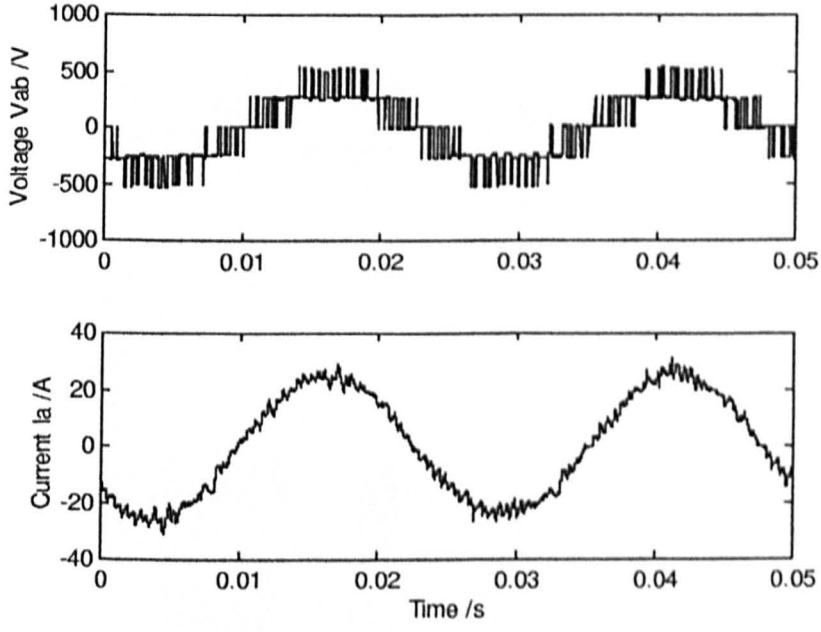

Figure 3.49 : *40 Hz Full load operation*

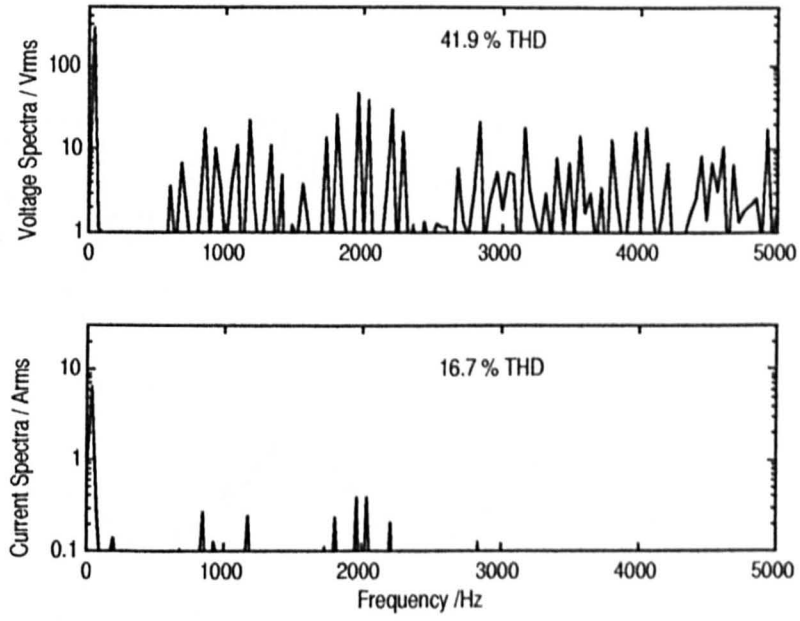

Figure 3.50 : *40 Hz Harmonics, no load condition*

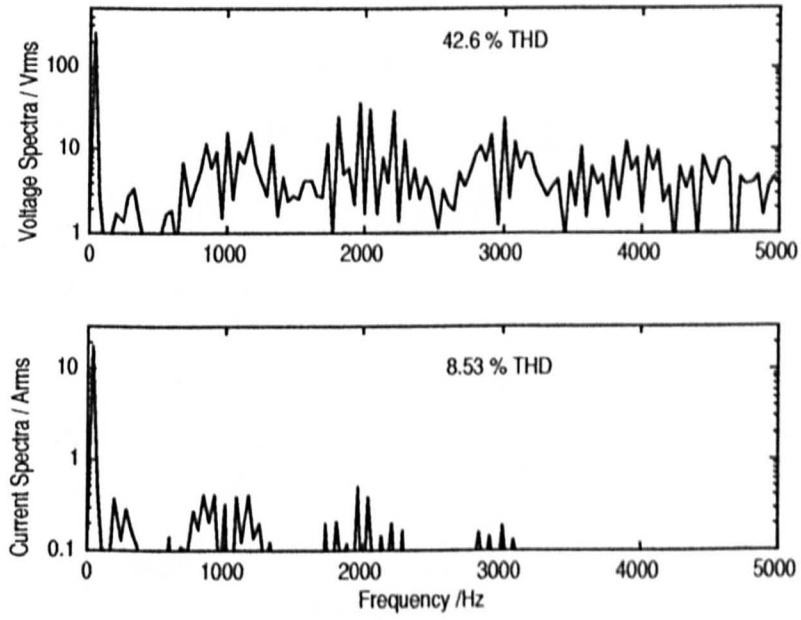

Figure 3.51 : *40 Hz Harmonics, full load operation*

3.7.5 50 Hz Output Frequency

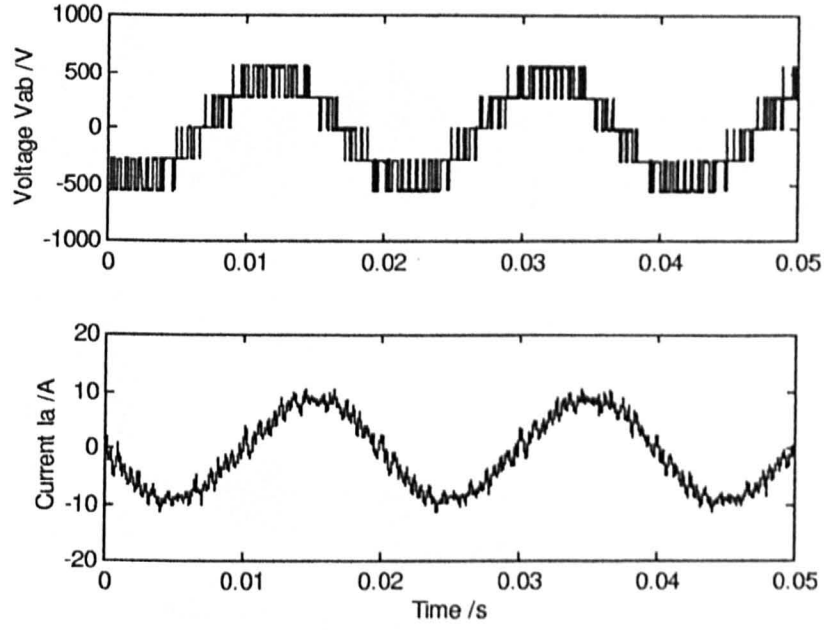

Figure 3.52 : *50 Hz No load operation*

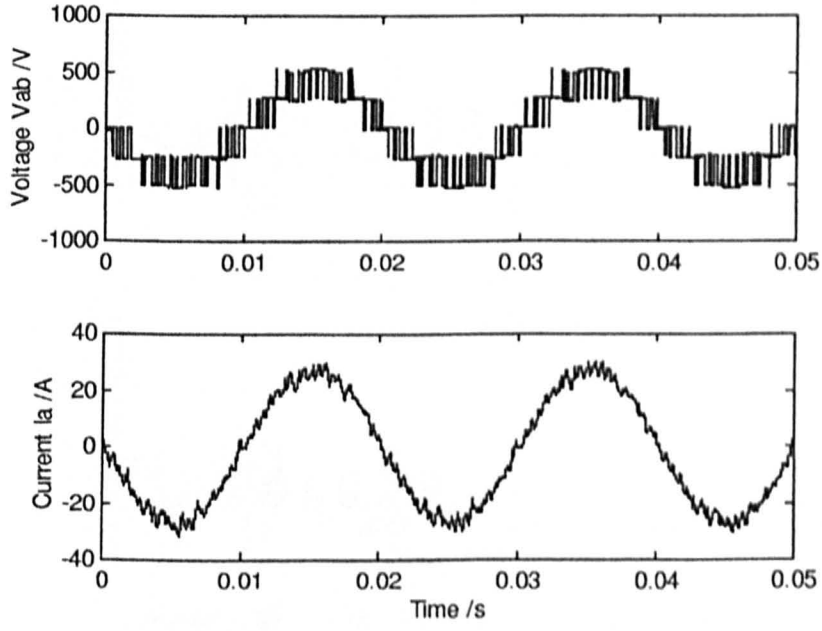

Figure 3.53 : *50 Hz Full load operation*

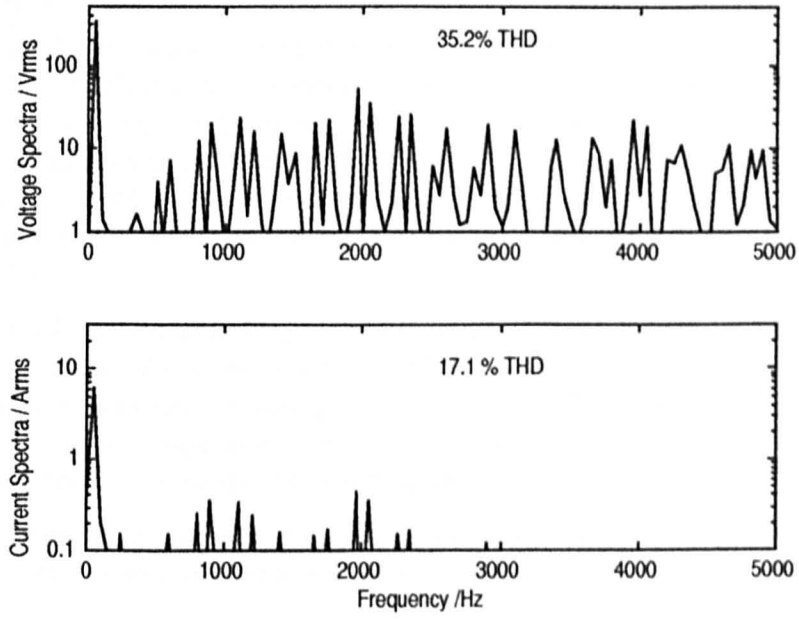

Figure 3.54 : *50 Hz Harmonics, no load condition*

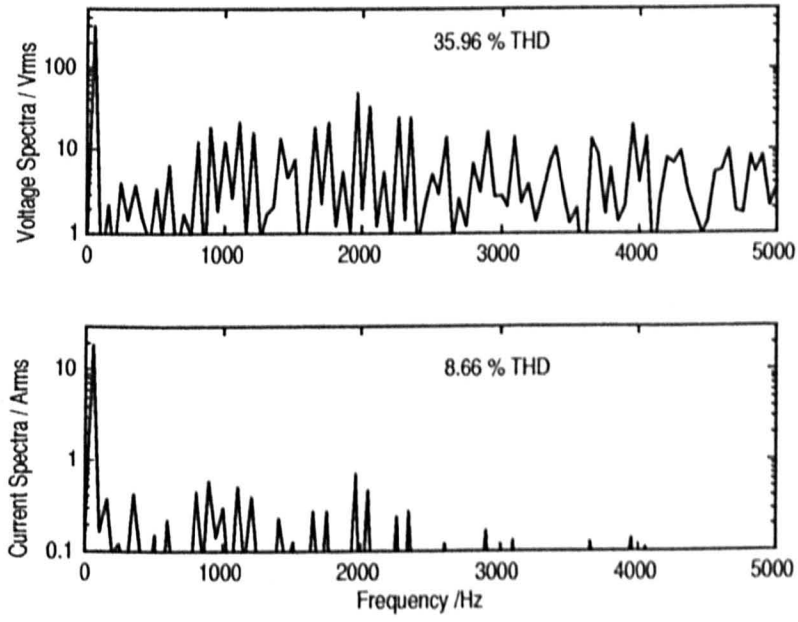

Figure 3.55 : *50 Hz Harmonics, full load condition*

3.7.6 Discussion of Results

Comparing similar results as the output frequency is increased there is the normal spreading of the switching sidebands in the spectrum of both the current and voltage. The voltage THD improves with frequency. This is reasonable as the fundamental amplitude increases, thereby reducing the relative magnitude of the harmonics. The current THD remains approximately constant however. With the current fundamental being about the same throughout the frequency range, this would indicate that whilst the harmonics move, their total effect remains the same.

Comparing results for the same frequency, there is a visible ripple in the voltage pattern when the inverter is loaded. The supply used for the inverter had a considerable inductance, which produces ripple in the capacitor voltages when the current is increased. This effect is seen in the harmonics, as the voltage THD increases whilst under load. The increase in fundamental current dominates the current spectrum and the THD decreases considerably.

The results show successful operation of the inverter through a wide steady state operating range. The neutral point control is in operation, and the capacitors are remaining balanced.

3.8 Conclusions

This chapter has presented the operation of a three level diode clamped inverter. The theoretical operation of the inverter has been discussed, and analysis completed to predict the operation. The actual construction of the first prototype inverter has been described.

Practical implementation of a PWM technique has been presented, including pulse dropping. The technique provides a stable changeover as the modulation passes between carriers.

The effects of operating without neutral point control have been presented, with practical results to show instability under certain operating conditions. As a solution to this, a basic control strategy has been suggested. Analysis has been performed to justify the proposed technique, with practical results confirming the capabilities. A technique for expanding the operating range of the control has been suggested. This will be demonstrated in chapter 5.

Full results have been presented showing the prototype operating over the full frequency range, both loaded and unloaded, within the capabilities of the open loop V/f control employed.

The construction of the three level inverter provided valuable information on the development of multi-level PWM, construction techniques, and understanding of the neutral point control requirement. This information was used in the development of the five level prototype inverter described in chapters 4 and 5.

3.9 Chapter References

[1] "80C166 Microcontroller User Manual", Siemens AC, 1990

[2] J. K. Steinke, "PWM CONTROL OF A THREE-LEVEL INVERTER – Principles and practical experience", IEE Conference Proceedings PEVD'90 , London, 1990, pp 98-103

[3] S. Ogasawara, H. Akagi, "Analysis of Variation of Neutral Point Potential in Neutral-Point-Clamped Voltage Source PWM Inverters", IEEE Conference Proceedings IAS'93, 1993, pp 965-970.

[4] A. M. Walczyna, R. J. Hill, "SPACE VECTOR PWM STRATEGY FOR 3-LEVEL INVERTERS WITH DIRECT SELF-CONTROL", Conference Proceedings EPE'93, Brighton, 1993, pp 152-157.

[5] R. Rojas, T. Ohnishi, T. Suzuki, "An Improved Voltage Vector Control Method for Neutral-Point-Clamped Inverters", IEEE Conference Proceedings PESC'94, 1994, pp 951-957.

[6] J. A. Houldsworth, D. A. Grant, "The use of harmonic distortion to increase the output voltage of a three phase inverter", IEEE Transactions on Industry Applications, Vol. 20, 1984, pp 1224-1227.

Chapter 4

The Five Level Inverter – Basic Motor Drive

Chapter Contents

4.1 Introduction

The completion of the three level inverter and its successful operation provided significant experience and knowledge regarding the practical construction of a multi-level inverter. This knowledge was then applied to the design and construction of a five level inverter, the main objective of the project. Only a limited number of papers have been published regarding the operation of a five level inverter [1]

This chapter will describe the basic construction and operation of a five level inverter prototype. This chapter concentrates primarily on the basic inverter operation assuming the levels in the DC link are supplied individually. Most of the work presented is an extension of that completed for the three level inverter in the previous chapter, and is presented in a similar format (Fundamental Analysis, Construction, PWM Strategy).

Chapter 5 will describe advanced operation of the inverter with high performance control, and capacitor balancing techniques.

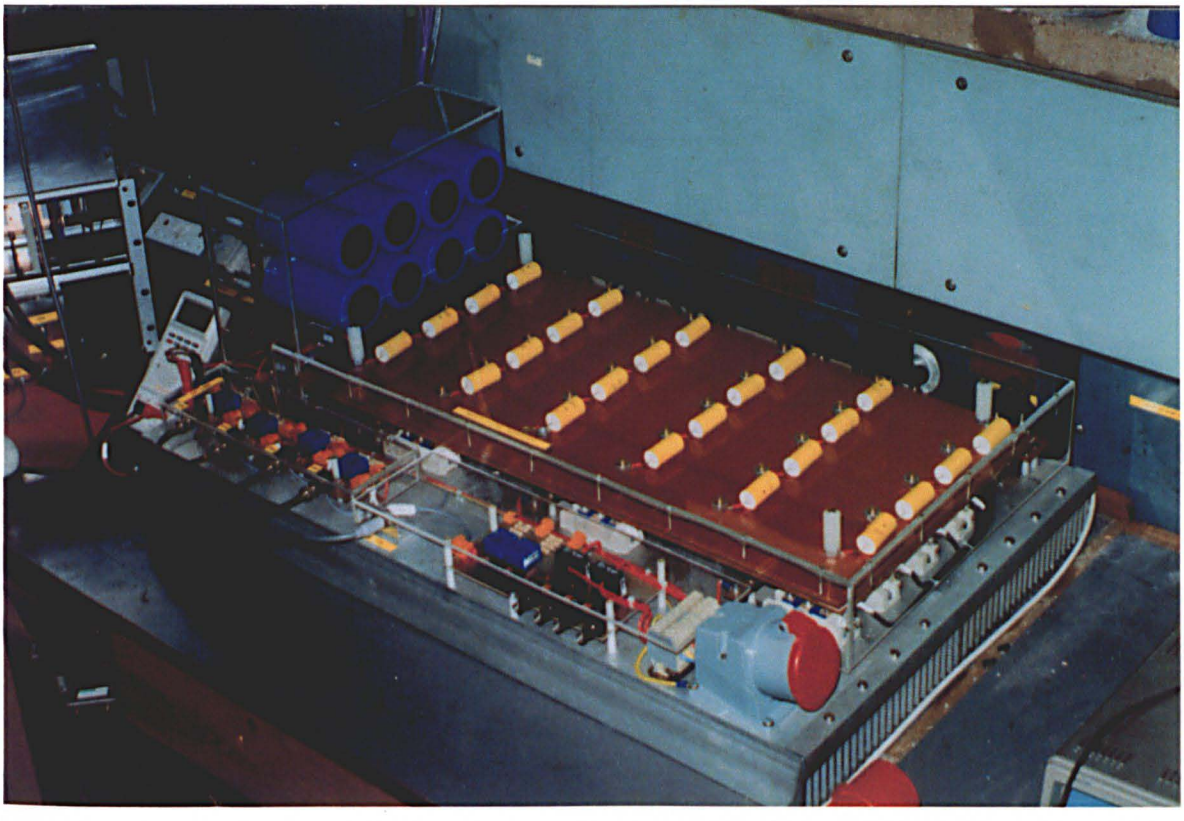

Figure 4.1 : *Five level prototype inverter*

4.2 The Five Level Circuit Structure

Figure 4.2 shows the circuit diagram for a single phase of a five level diode clamped inverter. The capacitor bank is now split into four parts, with interconnection via diodes to the IGBT string. Following the same principle as the three level inverter, the devices are switched in complementary pairs.

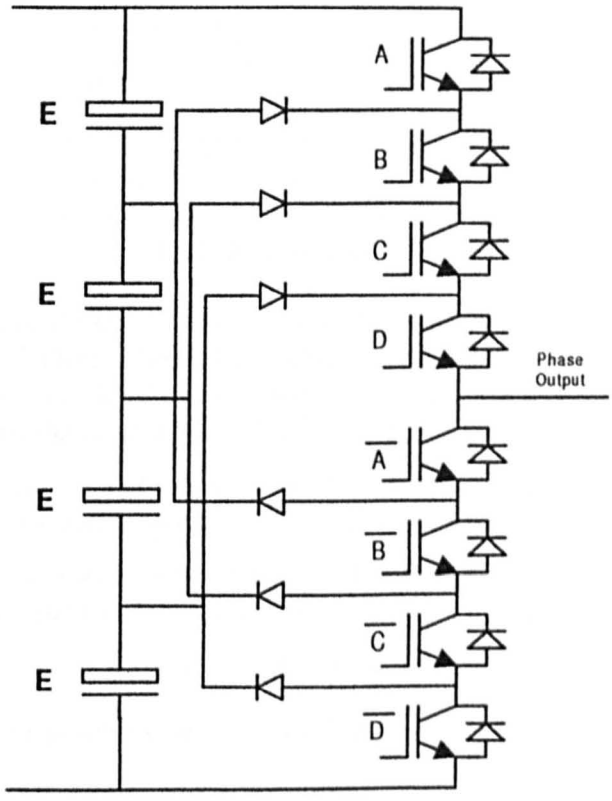

***Figure 4.2** : The Five Level Inverter*

4.2.1 Modes of operation

With four pairs of devices there are 16 theoretical switch states for each phase. The majority of these states cannot be used however, as the conduction path would result in some of the switching devices having to block more than E (as occurred in state three for the three level inverter). The blocking voltages for the interconnection diodes will be discussed later. The permitted combinations are listed in table 4-1.

State	A	B	C	D	Current	Output Voltage (w.r.t Neutral Point)
1	0	0	0	0	+	-2E
	0	0	0	0	-	-2E
2	0	0	0	1	+	-E
	0	0	0	1	-	-E
3	0	0	1	1	+	0
	0	0	1	1	-	0
4	0	1	1	1	+	+E
	0	1	1	1	-	+E
5	1	1	1	1	+	+2E
	1	1	1	1	-	+2E

Table 4-1 : *Switching States*

Switching sequentially through the five states produces the multi-level pattern. Stepping instantly past one of these states can produce transient voltage stresses (due to series switching) beyond the individual device capabilities and is therefore not permitted. For low modulation amplitudes the outer states will not normally be used.

Following a similar analysis to that used on the three level, it is possible to define modulation functions for the various states. An expanded set of rules then define the operation.

1) To obtain a positive output between +E and +2E, the circuit is switched between states four and five. The mean output voltage will be given by:

$$V_{mean} = E + E \cdot m_5 \qquad [4.1]$$

2) To obtain a positive output up to +E, the circuit is switched between states three and four.

$$V_{mean} = E \cdot m_4 \qquad [4.2]$$

3) To obtain a negative output down to –E, the circuit is switched between states two and three.

$$V_{mean} = -E \cdot m_2 \qquad [4.3]$$

4) To obtain a negative output between –E and –2E, the circuit is switched between states one and two.

$$V_{mean} = -E - E \cdot m_1 \qquad [4.4]$$

There are now five modulation functions that define the voltage at the output, and the current path through the circuit.

4.2.2 Analysis of Operation

Figure 4.3 shows the example modulation functions for a sinusoidal demand. This is the full modulation condition with all states being used. Below half modulation the outer states are not used in generating the output pattern.

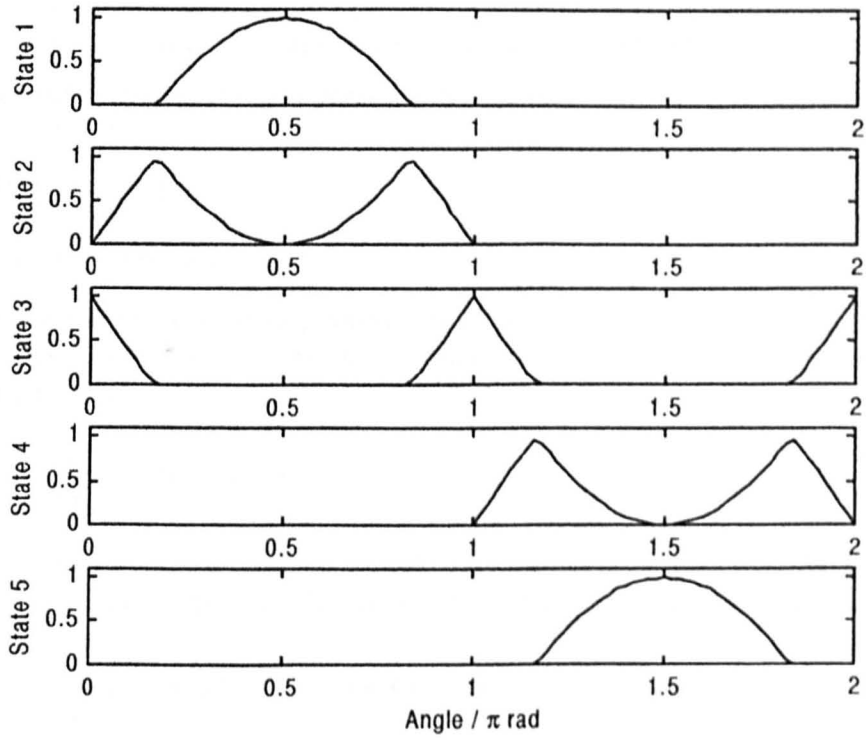

Figure 4.3 : *Modulation functions for the five level inverter*

Mathematically the modulation functions can be defined for a general modulation wave. If the modulation wave is given by M(θ) the modulation functions for the different states become those shown in equation 4.5.

$$
\begin{aligned}
m_1 &= \begin{cases} 2M(\theta)-1 & 0.5 < M(\theta) < 1.0 \\ 0 & -1 < M(\theta) < 0.5 \end{cases} \\
m_2 &= \begin{cases} 2-2M(\theta) & 0.5 < M(\theta) < 1.0 \\ 2M(\theta) & 0 < M(\theta) < 0.5 \\ 0 & -1 < M(\theta) < 0 \end{cases} \\
m_3 &= \begin{cases} 0 & 0.5 < M(\theta) < 1.0 \\ 1-2M(\theta) & 0 < M(\theta) < 0.5 \\ 1+2M(\theta) & -0.5 < M(\theta) < 0 \\ 0 & -1 < M(\theta) < -0.5 \end{cases} \\
m_4 &= \begin{cases} 0 & 0 < M(\theta) < 1 \\ -2M(\theta) & -0.5 < M(\theta) < 0 \\ 2+2M(\theta) & -1 < M(\theta) < -0.5 \end{cases} \\
m_5 &= \begin{cases} 0 & -0.5 < M(\theta) < 1.0 \\ -2M(\theta)-1 & -1 < M(\theta) < -0.5 \end{cases}
\end{aligned}
\qquad [4.5]
$$

Assuming a sinusoidal modulation, the currents drawn from the various levels can be calculated from the modulation functions by the same process as used for the three level inverter. Because of the change in operation that occurs as the amplitude increases beyond one half (when the outer states are utilised), each current is defined by two separate equations.

The sinusoidal modulation and resulting fundamental load current are defined by the equations 4.6 and 4.7.

$$M(\theta) = A\sin(\theta) \qquad [4.6]$$

$$i(\theta) = \hat{I}\sin(\theta + \phi) \qquad [4.7]$$

Following the same analysis as presented in chapter 3, the current for the top node of the capacitor bank, which will be the load current during state 1, can be calculated from the following equation.

$$\overline{I_1} = \frac{1}{2\pi}\int_0^{2\pi} m_1(\theta)\cdot i(\theta)\,d\theta \qquad [4.8]$$

For A<0.5, the state is not used, the modulation function m_1 is zero, as is the mean current. With A>0.5, the state is used, and the mean current can be calculated by equation 4.9.

$$\overline{I_1} = \frac{1}{2\pi}\int_{\alpha}^{\pi-\alpha}\left(2A\sin(\theta)-1\right)\cdot\hat{I}\sin(\theta+\phi)\,d\theta \qquad [4.9]$$

The angle α is defined as the crossover point between the modulation functions. This can be expressed as equation 4.10.

$$\alpha = \sin^{-1}\left(\frac{1}{2A}\right) \qquad [4.10]$$

The equation 4.9 can then be evaluated algebraically.

$$\overline{I_1} = \frac{\hat{I}\cos(\phi)}{4A\pi}\left[4\pi A^2 - \left(\sqrt{4A^2-1} + 4A^2\sin^{-1}\left(\frac{1}{2A}\right)\right)\right] \qquad [4.11]$$

Similar calculations can be performed for the other states yielding the following results.

$$\overline{I_1} = \begin{cases} 0 & 0 \le A \le 0.5 \\ \dfrac{\hat{I}\cos(\phi)}{4A\pi}\left[4\pi A^2 - \left(\sqrt{4A^2-1} + 4A^2\sin^{-1}\left(\dfrac{1}{2A}\right)\right)\right] & 0.5 \le A \le 1 \end{cases} \qquad [4.12]$$

$$\overline{I_2} = \begin{cases} \dfrac{A\hat{I}\cos(\phi)}{2} & 0 \le A \le 0.5 \\ \dfrac{\hat{I}\cos(\phi)}{2A\pi}\left[\sqrt{4A^2-1} + 4A^2\sin^{-1}\left(\dfrac{1}{2A}\right) - A^2\pi\right] & 0.5 \le A \le 1 \end{cases} \qquad [4.13]$$

$$\overline{I_3} = 0 \qquad [4.14]$$

$$\overline{I_4} = \begin{cases} -\dfrac{A\hat{I}\cos(\phi)}{2} & 0 \le A \le 0.5 \\ -\dfrac{\hat{I}\cos(\phi)}{2A\pi}\left[\sqrt{4A^2-1}+4A^2\sin^{-1}\left(\dfrac{1}{2A}\right)-A^2\pi\right] & 0.5 \le A \le 1 \end{cases} \quad [4.15]$$

$$\overline{I_5} = \begin{cases} 0 & 0 \le A \le 0.5 \\ -\dfrac{\hat{I}\cos(\phi)}{4A\pi}\left[4\pi A^2-\left(\sqrt{4A^2-1}+4A^2\sin^{-1}\left(\dfrac{1}{2A}\right)\right)\right] & 0.5 \le A \le 1 \end{cases} \quad [4.16]$$

Rewriting these equations then the general pattern in equation 4.17 is obtained.

$$\begin{aligned} \overline{I_1} &= K_{m1}(A)\cdot\hat{I}\cos(\phi) \\ \overline{I_2} &= K_{m2}(A)\cdot\hat{I}\cos(\phi) \\ \overline{I_3} &= K_{m3}(A)\cdot\hat{I}\cos(\phi) \\ \overline{I_4} &= K_{m4}(A)\cdot\hat{I}\cos(\phi) \\ \overline{I_5} &= K_{m5}(A)\cdot\hat{I}\cos(\phi) \end{aligned} \quad [4.17]$$

Figure 4.4 shows the current factors K_{m1} to K_{m5} plotted against the modulation amplitude A.

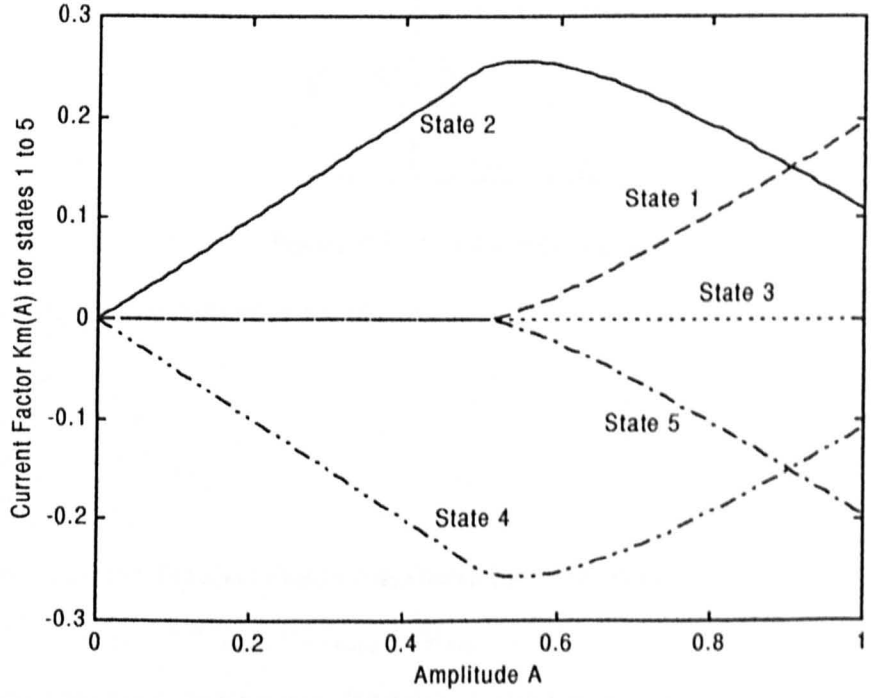

Figure 4.4 : *Plot of current factors for the level currents*

The analysis can be confirmed through the power flow. For this circuit the AC power equation is slightly different, due to the increased number of levels.

$$V_{rms} = \sqrt{2}AE \quad [4.18]$$

$$I_{rms} = \frac{\hat{I}}{\sqrt{2}} \quad [4.19]$$

$$P_{AC} = V_{rms} I_{rms} \cos(\phi) = AE\hat{I} \cos(\phi) \qquad [4.20]$$

For amplitudes A<0.5, the analysis is the same as the three level.

$$P_{DC} = E\overline{I_2} - E\overline{I_4} = EA\hat{I} \cos(\phi) \qquad [4.21]$$

Above half modulation the analysis becomes more complicated, and loop current analysis is required. Figure 4.5 shows the loop current paths from the capacitor bank.

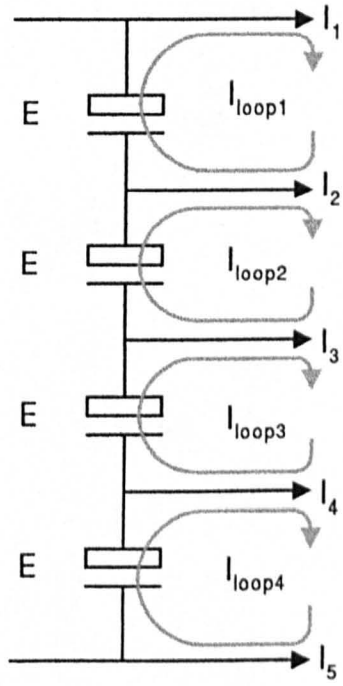

Figure 4.5 : *Loop current analysis*

The loop currents are defined in equation 4.22.

$$\begin{aligned} I_{loop1} &= I_1 \\ I_{loop2} &= I_2 + I_1 \\ I_{loop3} &= -I_4 - I_5 \\ I_{loop4} &= -I_5 \end{aligned} \qquad [4.22]$$

The power flow can then be calculated as shown by equation 4.23.

$$P_{DC} = EI_{loop1} + EI_{loop2} + EI_{loop3} + EI_{loop4} \qquad [4.23]$$

Substituting the mean currents gives the solution in equation 4.24.

$$P_{DC} = AE\hat{I} \cos(\phi) \qquad [4.24]$$

This result confirms the basis of the analysis. As with the three level inverter, the neutral point current (state 3) is zero for all modulation values. The capacitor balance around the neutral point will therefore remain constant (assuming no disturbance). The currents for states 2 and 4 are non-zero when power is transferred from the link, and will result in variation of the capacitor voltages. The circuit will not operate correctly unless some additional circuitry is added to force the voltage balance on the capacitors.

It was mentioned earlier that the switching strategy was restricted to the five listed states to avoid over-voltage on the IGBTs. Examining the blocking requirements for the diodes which provide the conduction paths back to the DC link indicates that the diodes do not all see the same voltage. Certain diodes are required to block multiples of the step voltage E. Figure 4.6 shows the blocking voltages for state five.

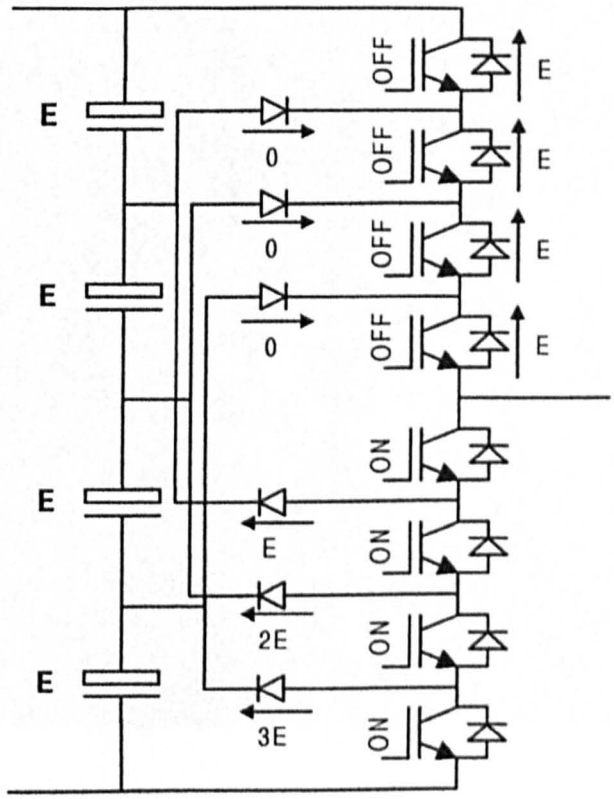

***Figure 4.6** : Example Blocking Condition*

It can be seen in the figure that the diodes have to block different voltages, with the maximum for one particular diode in this state of three times the nominal IGBT blocking voltage. This means the diode needs to be a special high voltage device, or a series combination. The practicalities of series diode operation will be discussed further in chapter 6.

4.3 Power Circuit Implementation

Figure 4.7 shows a photograph of the power electronics for the prototype five level inverter.

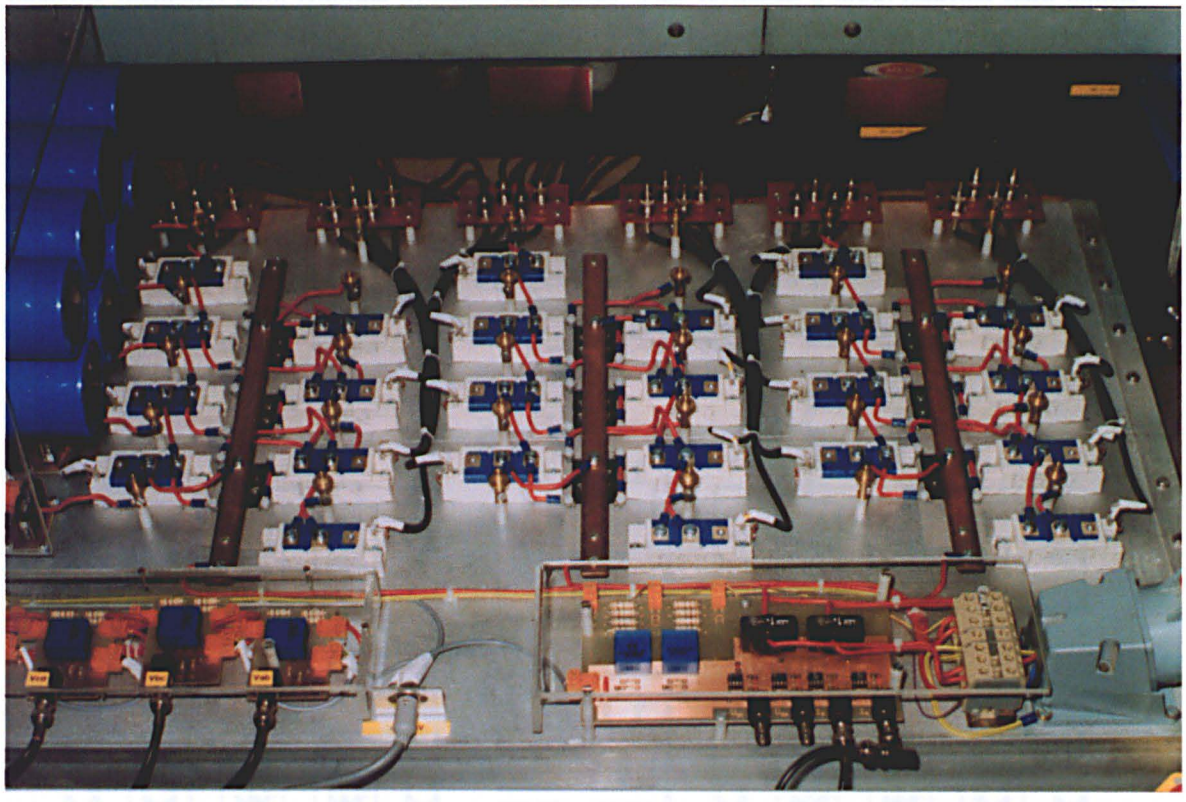

Figure 4.7 : *Photograph of Prototype Inverter*

Rather than using a modular structure, the five level inverter was built as a single unit. The construction of the three level provided the necessary experience to enable this to be done with sufficient confidence. This allowed improvement in the layout to reduce the inductance from the devices to the DC link.

4.3.1 Power Semiconductor Devices

The same IGBTs that were used in the three level inverter prototype were used again for the five level inverter prototype. The diodes used in the three level prototype were being pushed to the limit of their safe operating area, so with the construction of the five level inverter it was decided to upgrade these. Details of the alternate diodes are given below.

Clamp diodes : Harris RUR50100

The diode used is a higher rated version of that described for the three level prototype. The higher current requires a larger package size, in this case TO-240.

4.3.2 Circuit Layout

The power electronic devices are mounted on a main heatsink block (1000 mm x 600 mm). Above this there is a layered busbar system. This provides the connections back to the capacitor bank. Connection points along the sheets provide access to the voltage levels in the split capacitor bank. Polyester capacitors are connected at the distributed terminations to

increase the local capacitance and provide a low inductive path for the transient currents at switching. This structure greatly reduces the current path inductance, and avoids the ringing problems that occurred on the prototype three level inverter. The layout of the devices beneath the bus for a single phase leg is shown in figure 4.8. The diodes are mounted to the earthed heatsink insulated with silicone impregnated sheet. This provides a good thermal path whilst providing the insulation requirement to the back of the diodes (which are live).

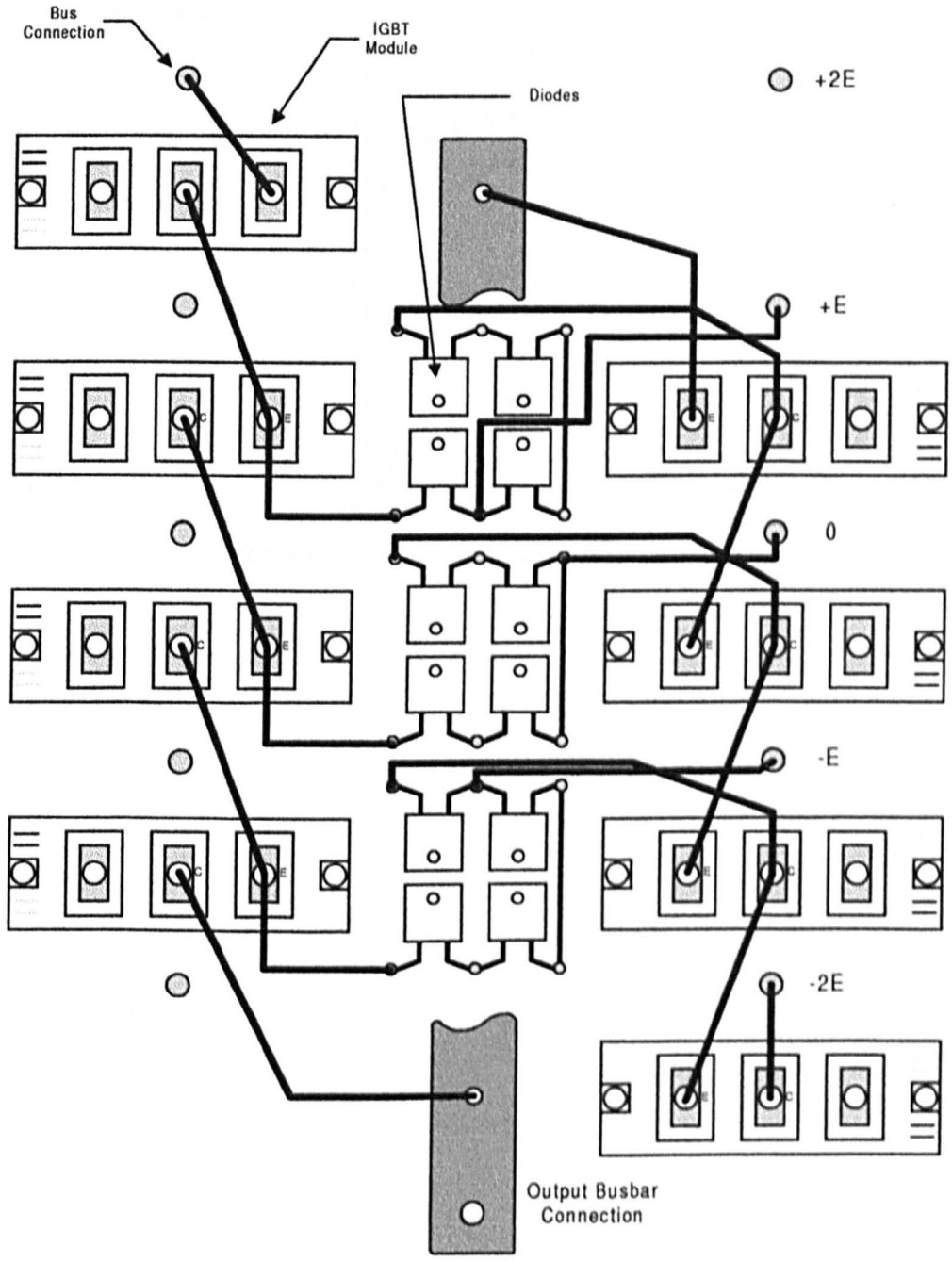

Figure 4.8 : *Layout of one phase*

Current and voltage transducers are mounted on the DC bus to provide protection and measurement. Additional transducers are also connected to the output to provide feedback of motor current and motor voltage.

The DC link was initially fed via a three phase transformer arrangement which removed the need for balancing of the capacitor voltages. The arrangement is shown in figure 4.9. This arrangement was satisfactory for testing of the PWM, but due to the high leakage inductance in the transformer, this produced too high a voltage drop in the DC link when under load.

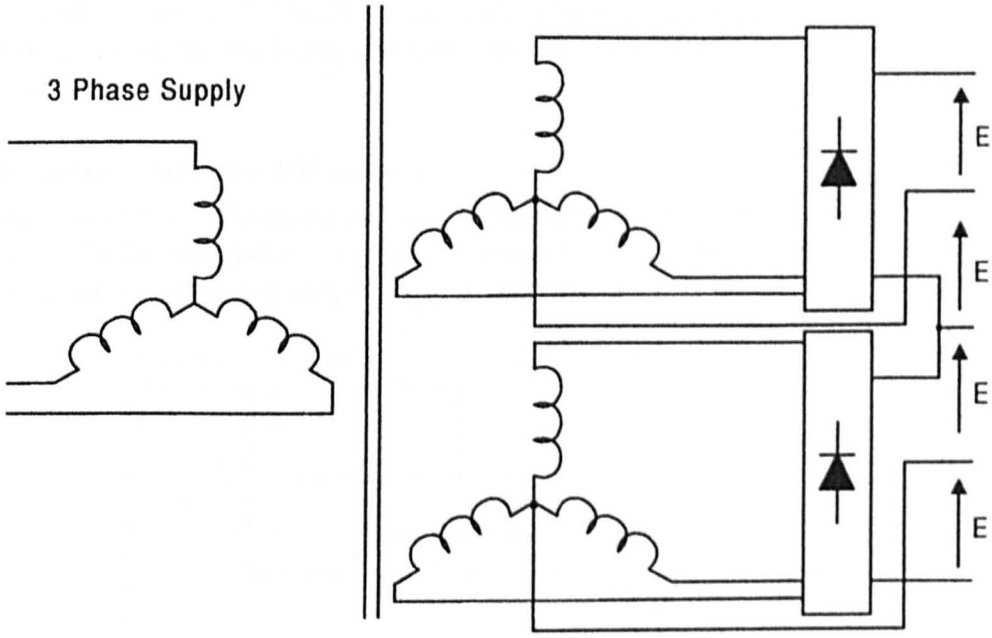

***Figure 4.9** : Transformer Supply Arrangement*

4.4 PWM Implementation

In chapter three the PWM strategy was discussed for the three level inverter. The five level technique is basically the same, but the carrier changeover method has to be expanded to handle steps between non-adjacent carriers. Generation of the PWM for the five level inverter was shown in figure 2.15. Due to the increased complexity required to drive twelve channels of PWM, reinstating previously dropped edges becomes impractical. A new approach is therefore required.

4.4.1 Carrier Adaptive PWM strategy

Without the ability to change the previous switching edge, a fixed carrier pattern will generate delays when the modulation wave passes between carriers. One solution is to modify the carrier phase to enable switching to occur. An example of this is shown in figure 4.10.

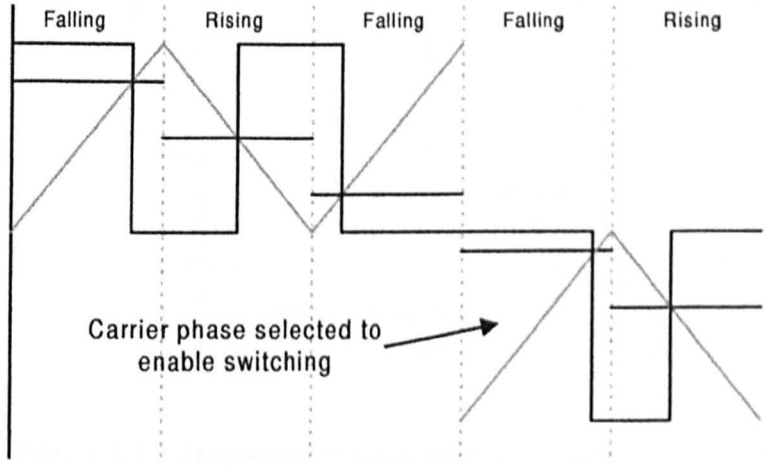

Figure 4.10 : *Carrier phase selection*

The carrier phase for each half cycle is now chosen by examining the output state at the end of the previous cycle. If the state is above the carrier, then the next half cycle will look for a falling edge. On the other hand if the state is below the carrier, then the next edge will be a rising edge. This also handles the entry and exit of pulse dropping efficiently. Once pulse dropping is entered on a rising edge for example, then the carrier phase will remain in the falling edge condition until pulse dropping is finished. This is demonstrated in figure 4.11.

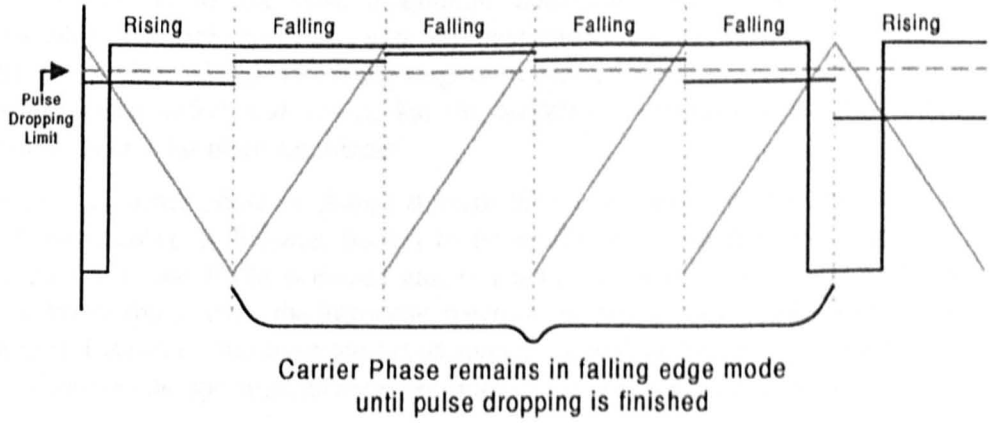

Figure 4.11 : *Pulse dropping with carrier phase selection*

If the modulation wave passes from one carrier to another non-adjacent carrier, then the technique discussed for the three level would simultaneously switch two devices. Staggering the switching edges for each carrier by inserting a minimum pulse width into the timing can solve this. Figure 4.12 shows an example transient pattern with staggered edges.

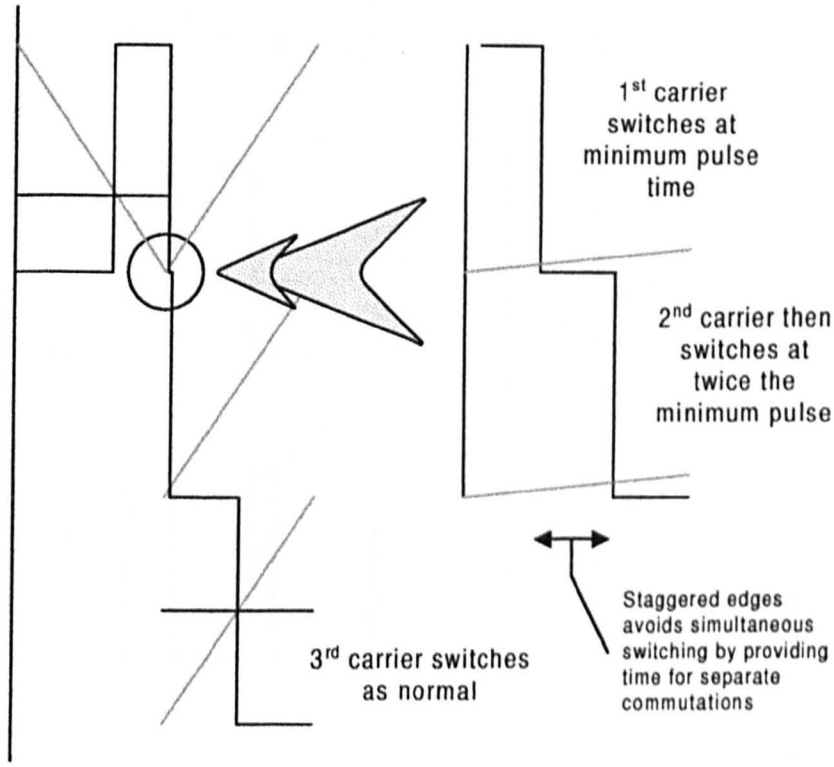

***Figure 4.12** : Staggered minimum pulse for carrier changeover*

Rapid changes in modulation of this nature may seem extreme, but with the intention to implement high performance closed loop current control, it can easily occur. As an additional benefit the technique also improves operation at higher modulation frequencies (100 – 200 Hz).

Because the carrier phases change during the modulation cycle, this has an effect on the switching harmonics. Since the carriers on different output phases are now independent, it is possible for one to produce a rising edge whilst the other is producing a falling edge. Figure 4.13 shows output for the same modulation conditions, but with different carrier phase relationships. The right hand set, with different carrier phases, produces a phase to phase pattern with a clearly larger switching amplitude. This possible increase in the phase to phase harmonics is an unfortunate effect, but the distortion in fundamental voltage that would otherwise occur is far more significant.

Allowing the carrier phase to change through the cycle means that the start and end states may differ, causing a different pattern to be produced during the next cycle. At certain operating points the PWM becomes almost chaotic in nature, with a constantly changing pattern. When this occurs, the harmonic spectrum no longer has a defined set of switching harmonics. Instead of this there are broad spreads around multiples of the carrier frequency. This is shown in the spectrum analysis provided in the operating results section.

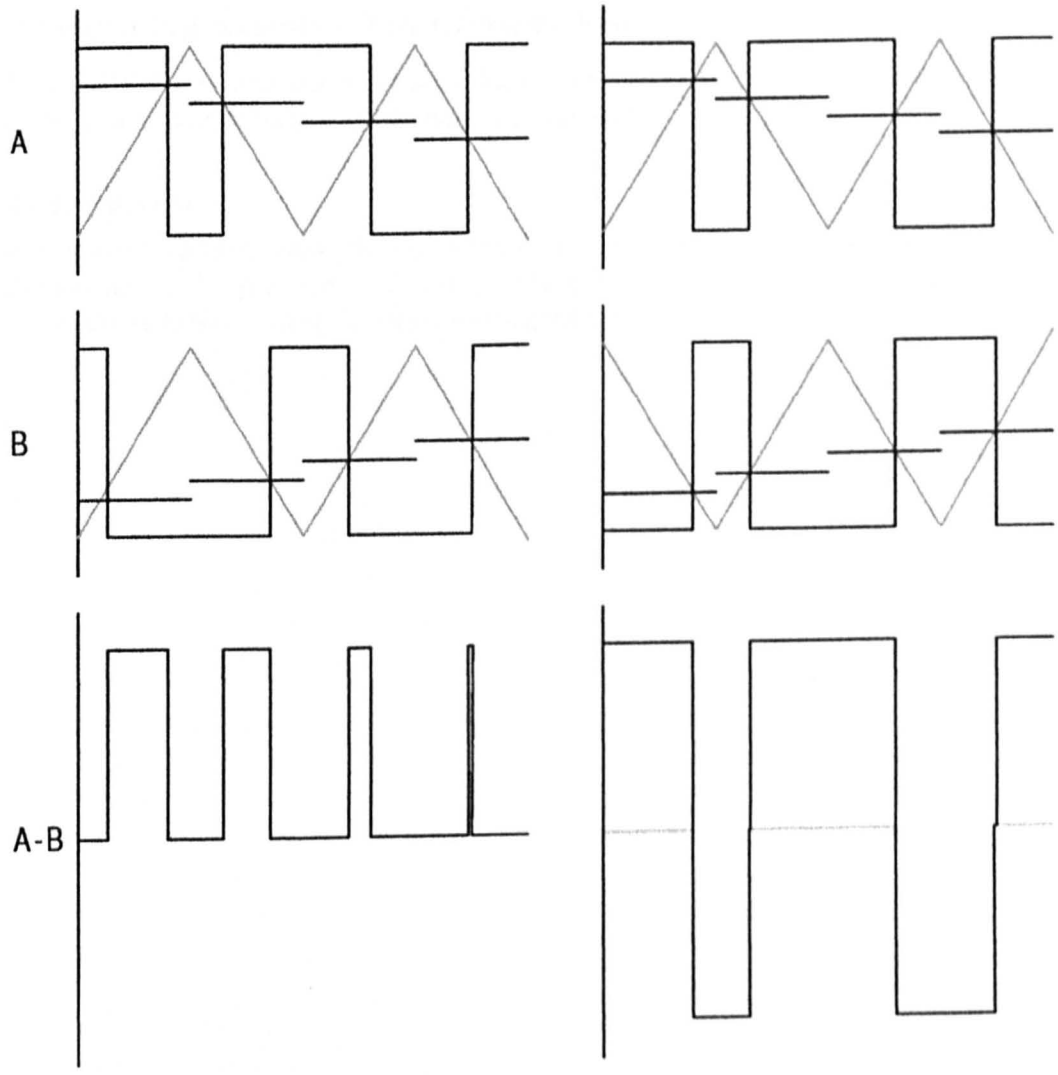

Figure 4.13 : *Effect of relative carrier phases*

4.5 Operating Results – Transformer Fed

With the PWM implemented, a set of no load results was taken with the transformer supply arrangement providing balance of the capacitor voltages.

4.5.1 Test Results

The following sections show the operation of the prototype inverter driving a Mitsubishi induction motor in open loop V/f control. These results provide harmonic information to evaluate the switching strategy implemented on the inverter.

4.5.2 10 Hz Output Frequency

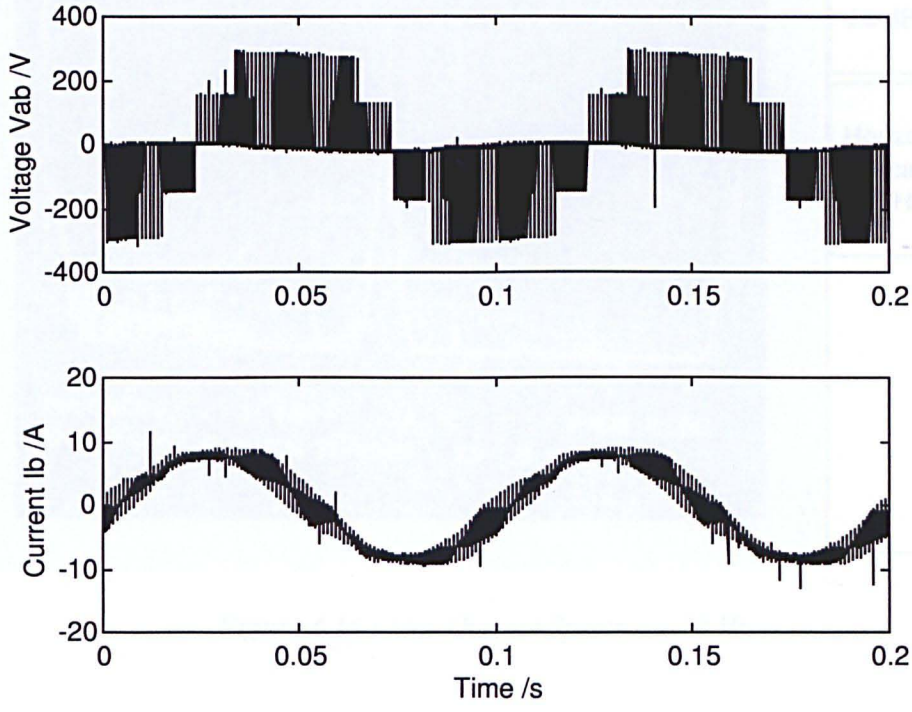

Figure 4.14 : *Operating result at 10 Hz*

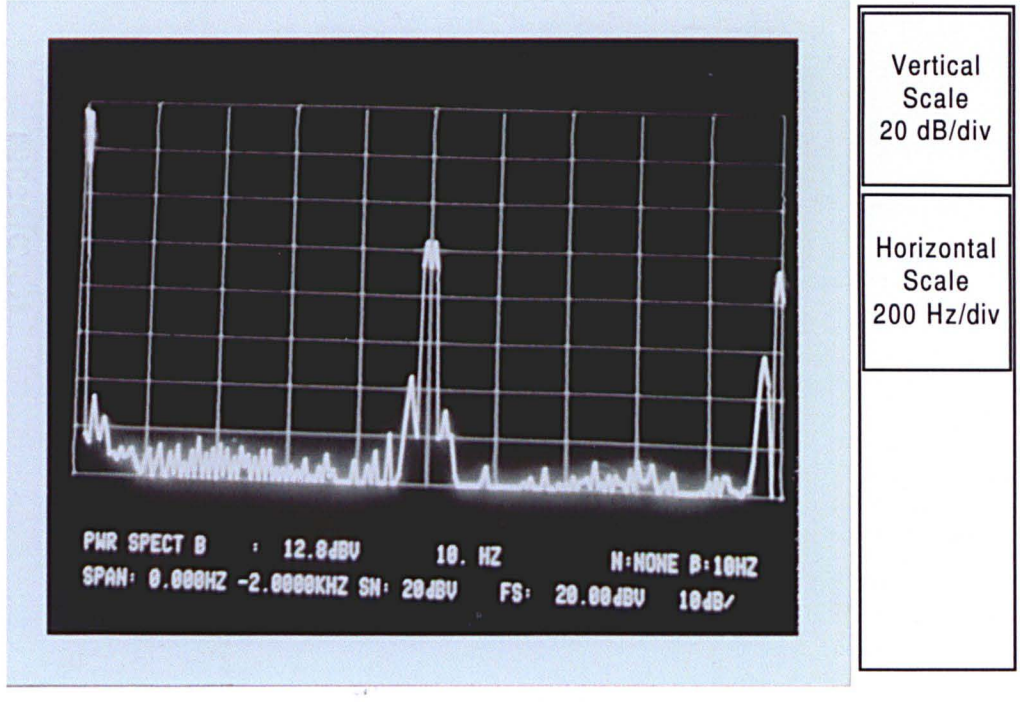

Figure 4.15 : *Phase Voltage Spectra at 10 Hz*

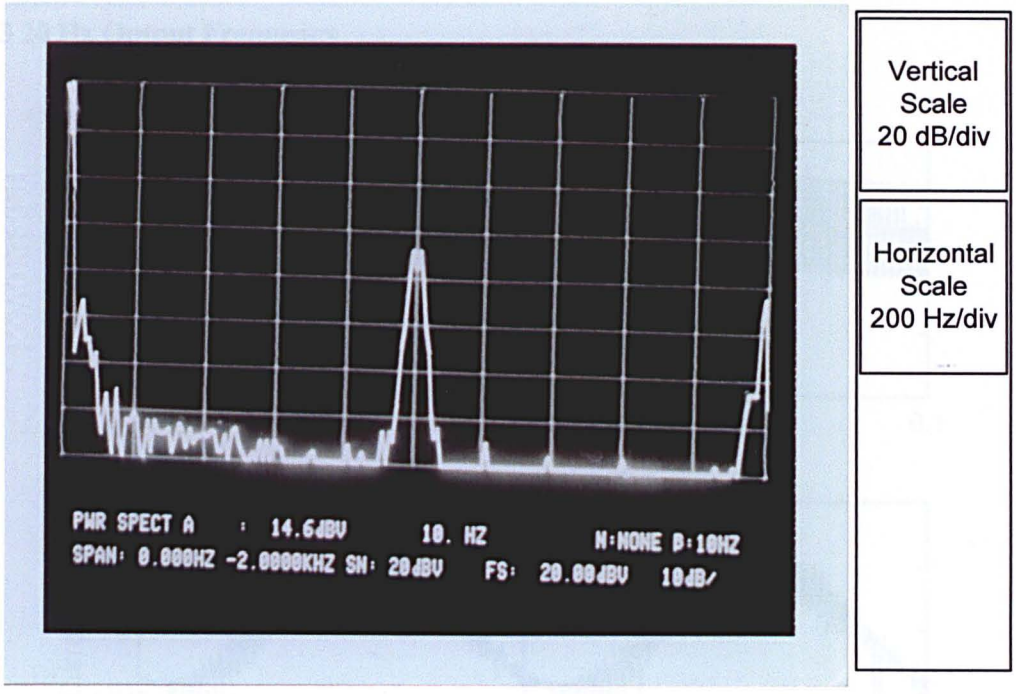

Figure 4.16 : *Line Current Spectra at 10 Hz*

4.5.3 20 Hz Output Frequency

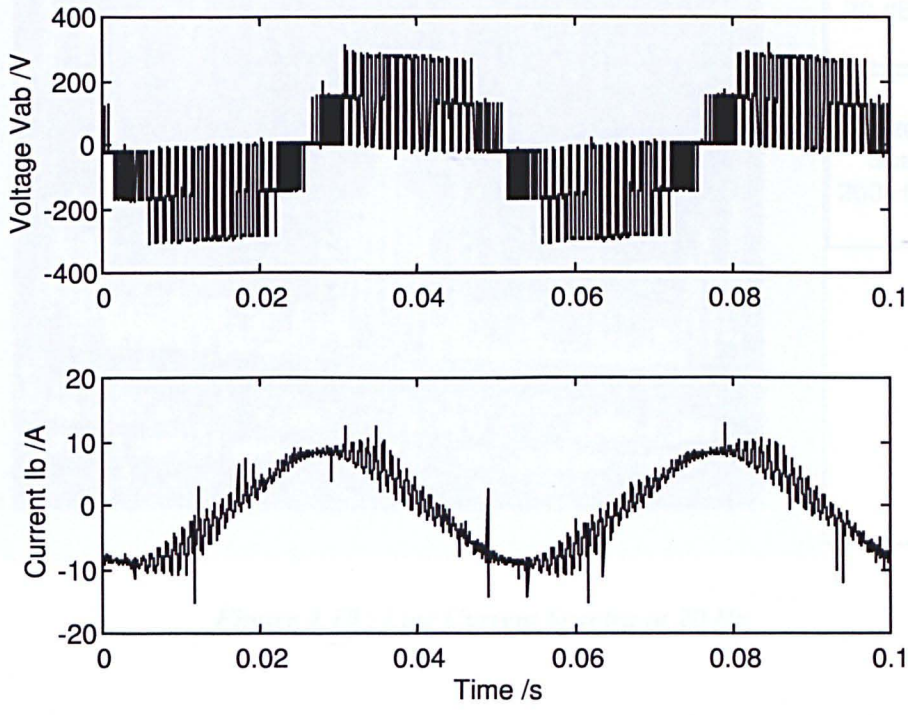

Figure 4.17 : *Operating result at 20 Hz*

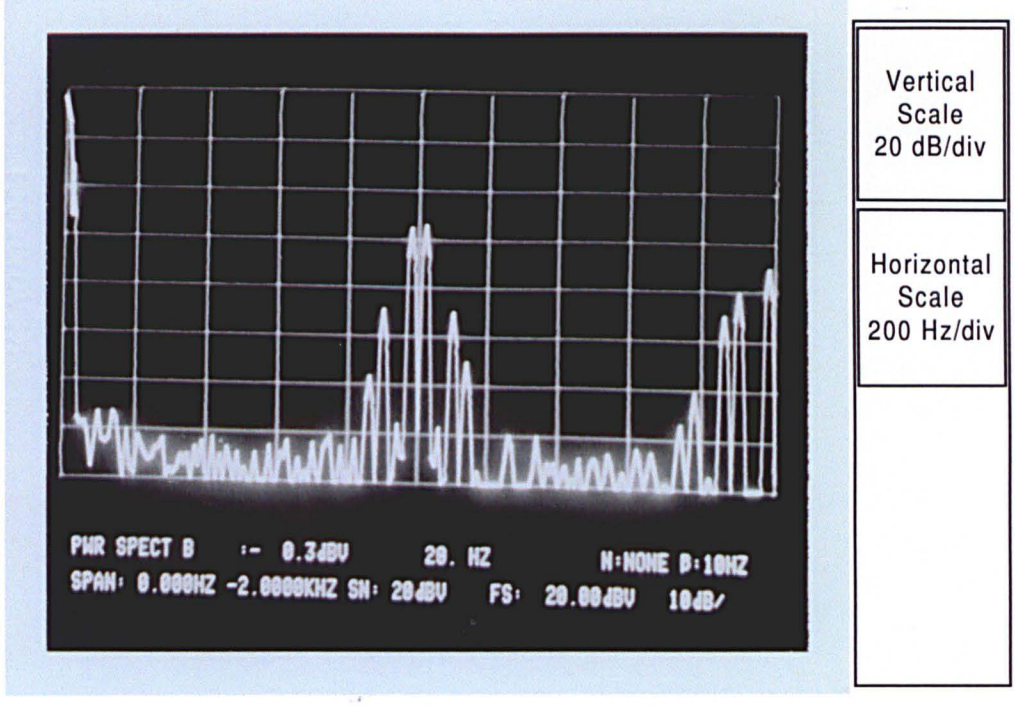

Figure 4.18 : *Phase Voltage Spectra at 20 Hz*

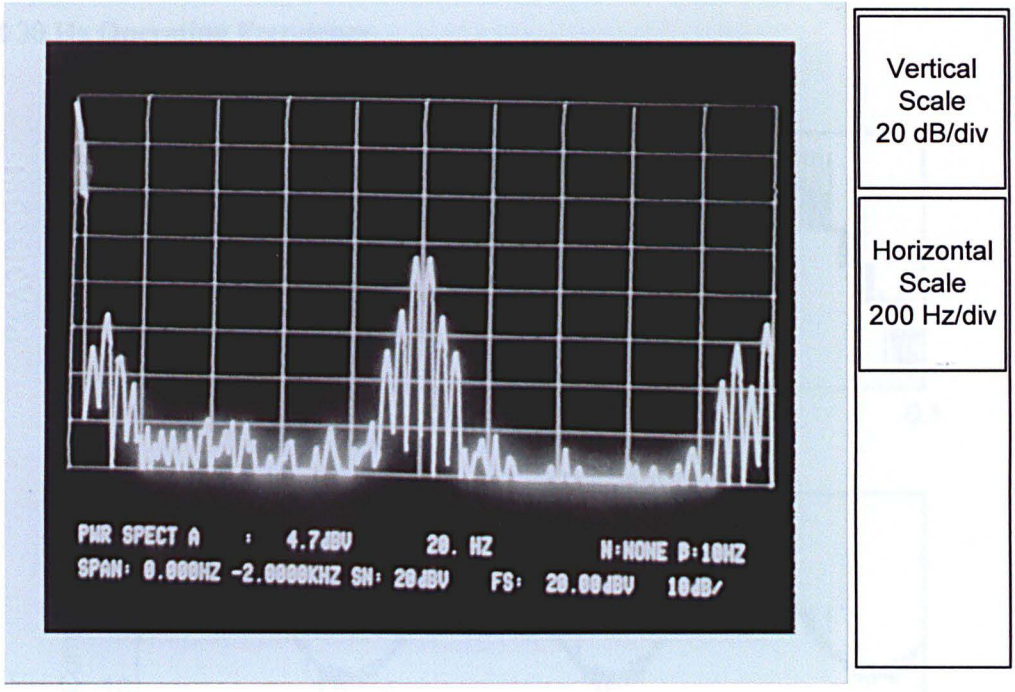

Figure 4.19 : *Line Current Spectra at 20 Hz*

4.5.4 30 Hz Operating Frequency

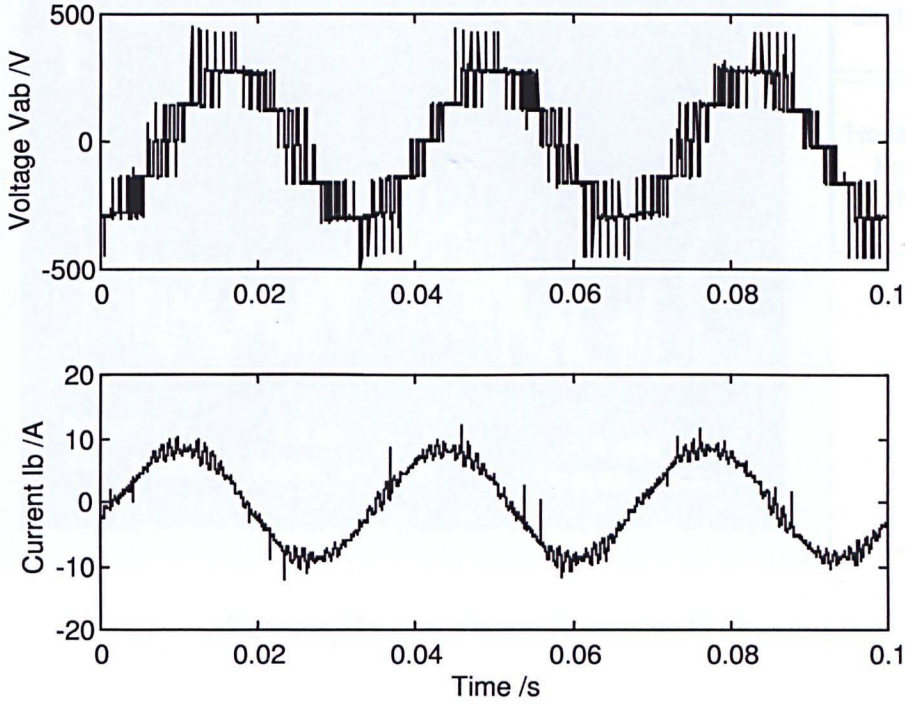

Figure 4.20 : *Operating result at 30 Hz*

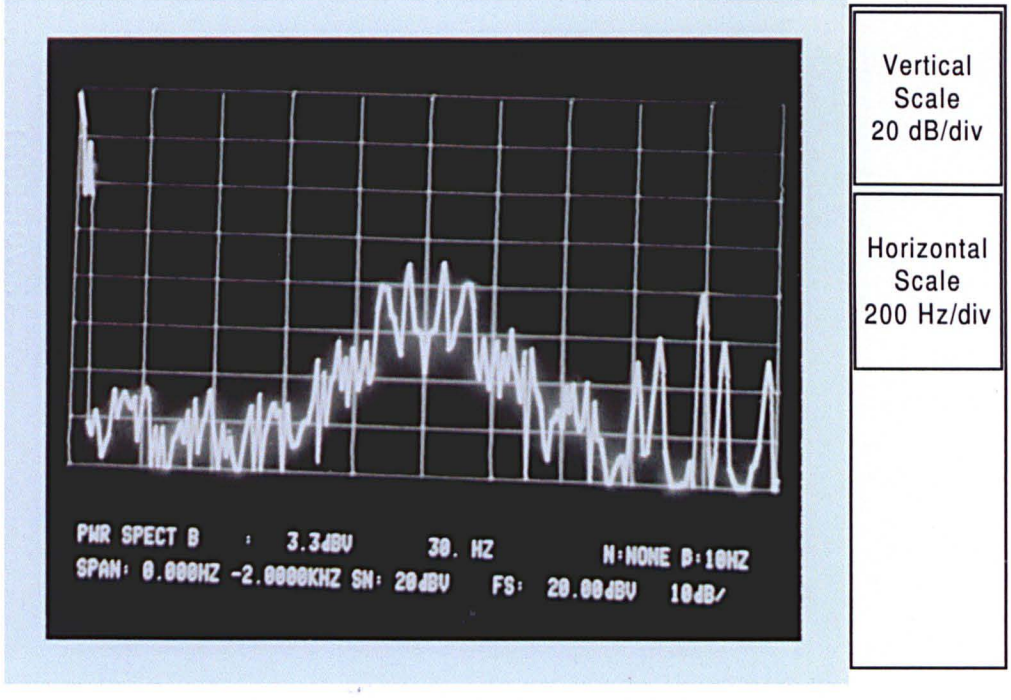

Figure 4.21 : *Phase Voltage Spectra at 30 Hz*

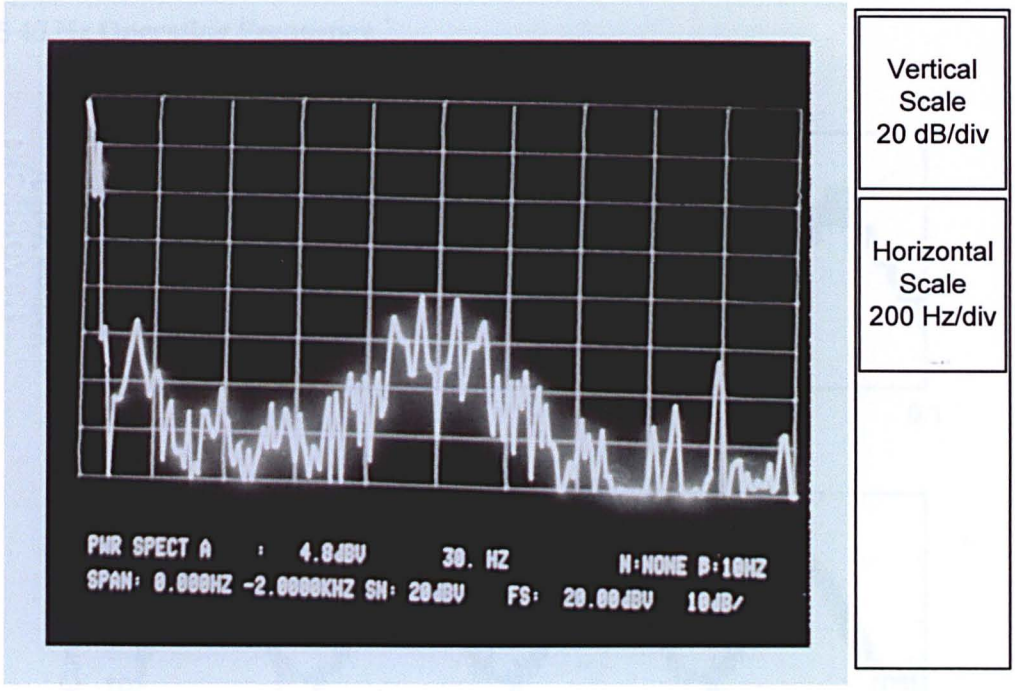

Figure 4.22 : *Line Current Spectra at 30 Hz*

4.5.5 40 Hz Operating Frequency

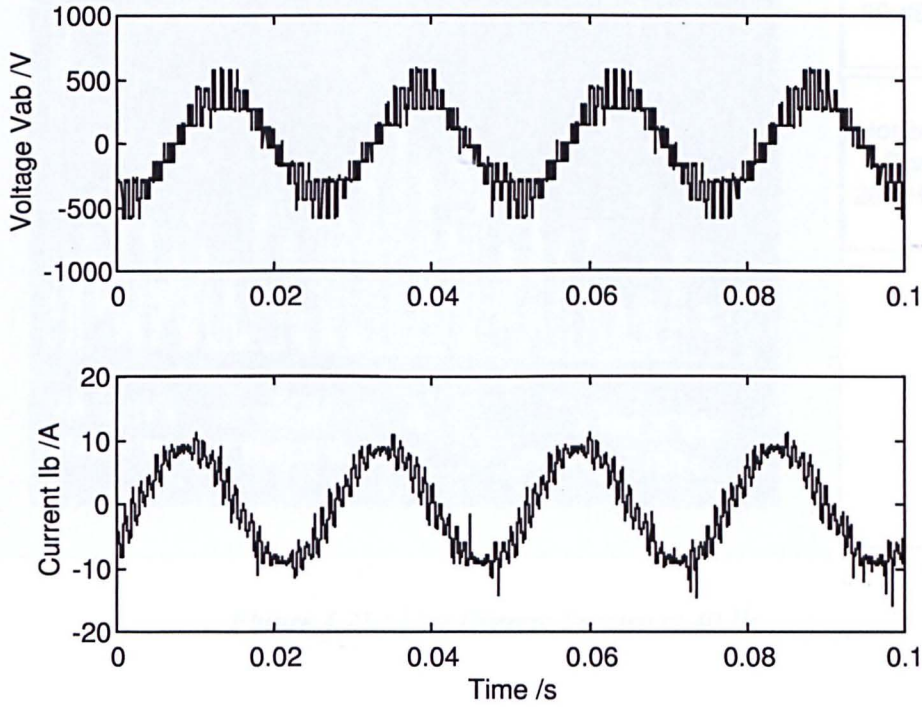

Figure 4.23 : *Operating result at 40 Hz*

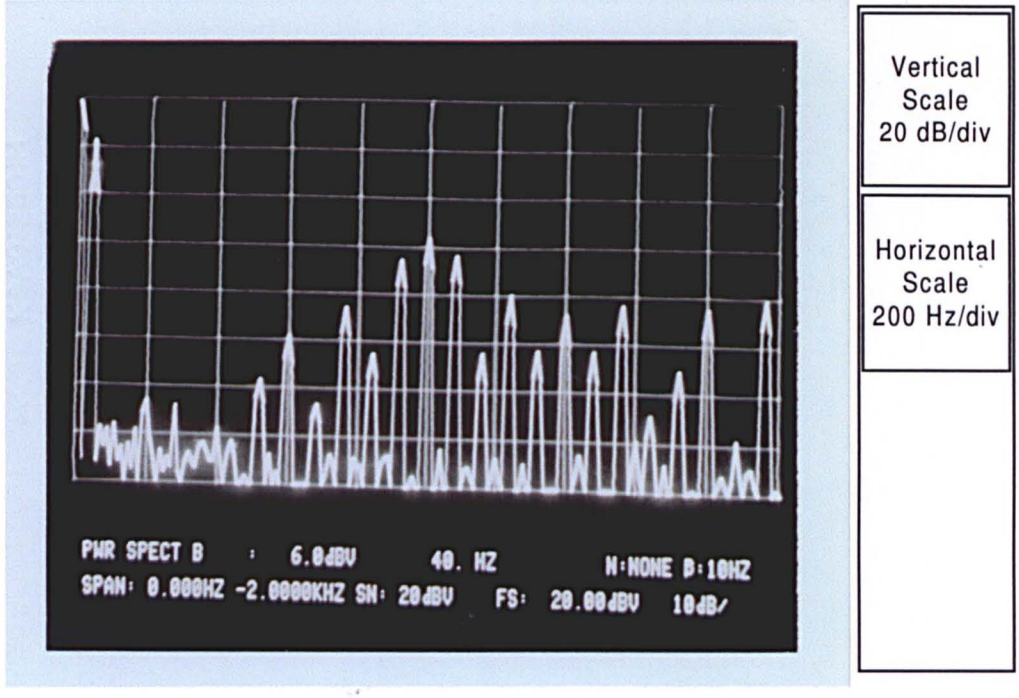

Figure 4.24 : *Phase Voltage Spectra at 40 Hz*

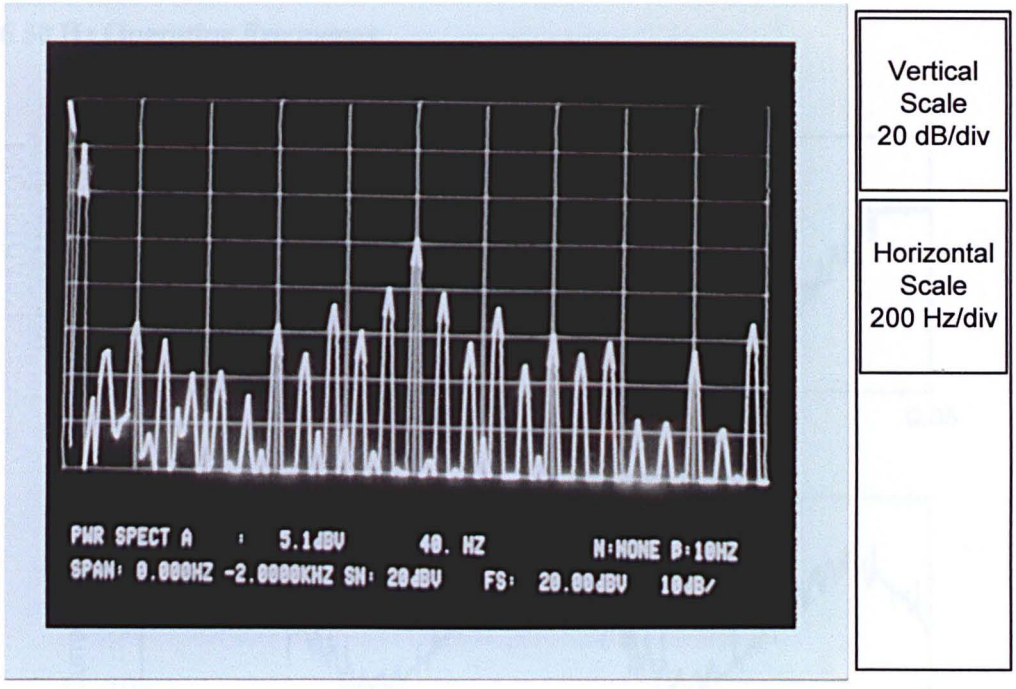

Figure 4.25 : *Line Current Spectra at 40 Hz*

4.5.6 50 Hz Operating Frequency

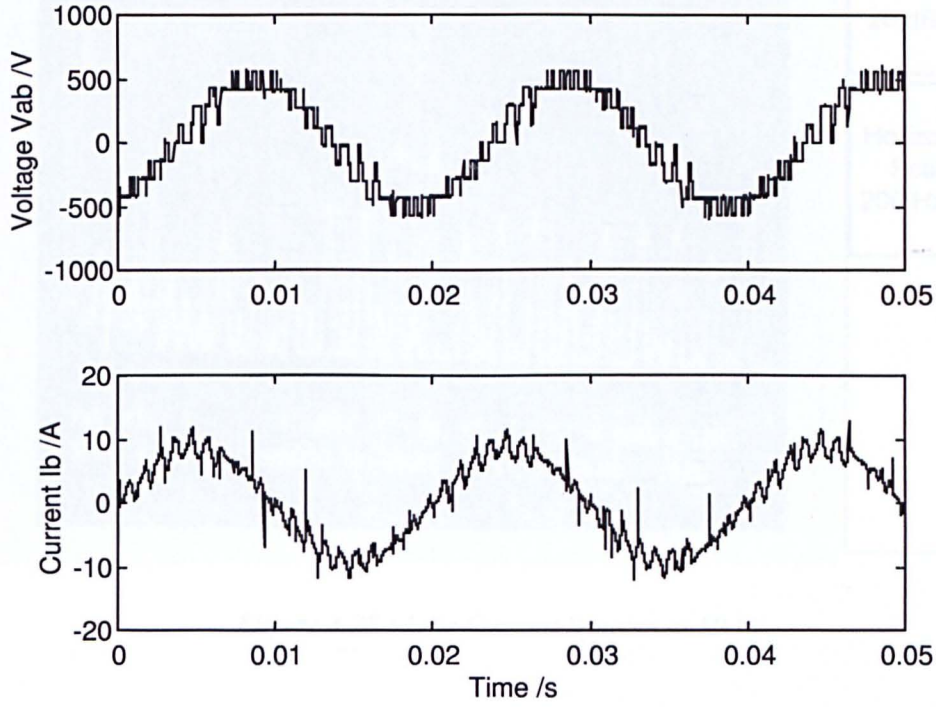

Figure 4.26 : *Operating result at 50 Hz*

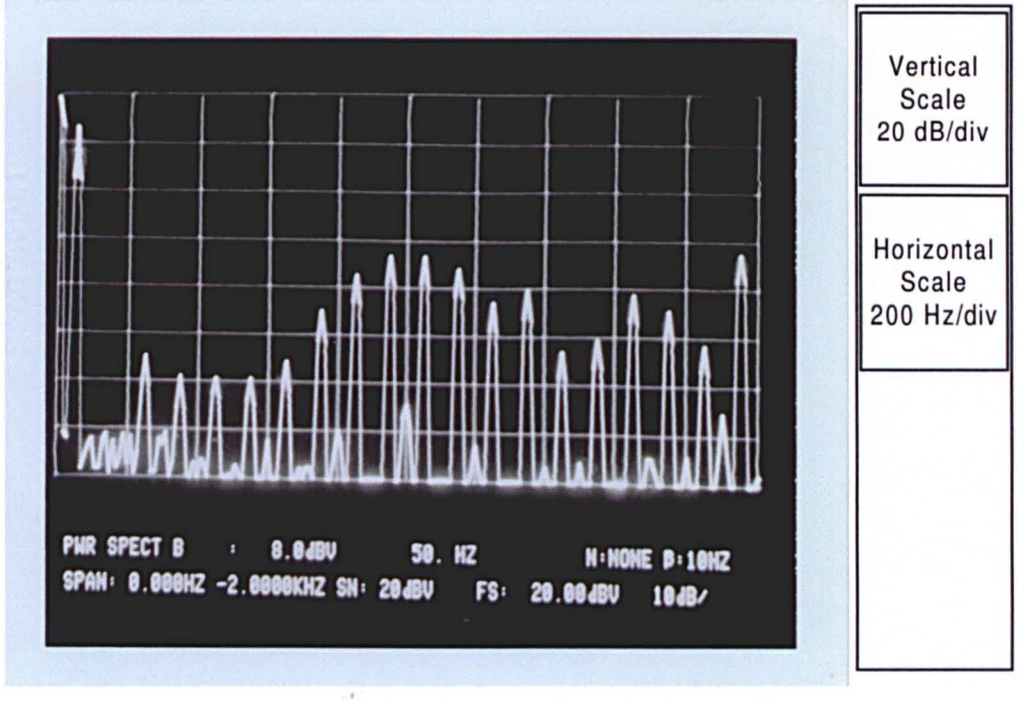

Figure 4.27 : *Phase Voltage Spectra at 50 Hz*

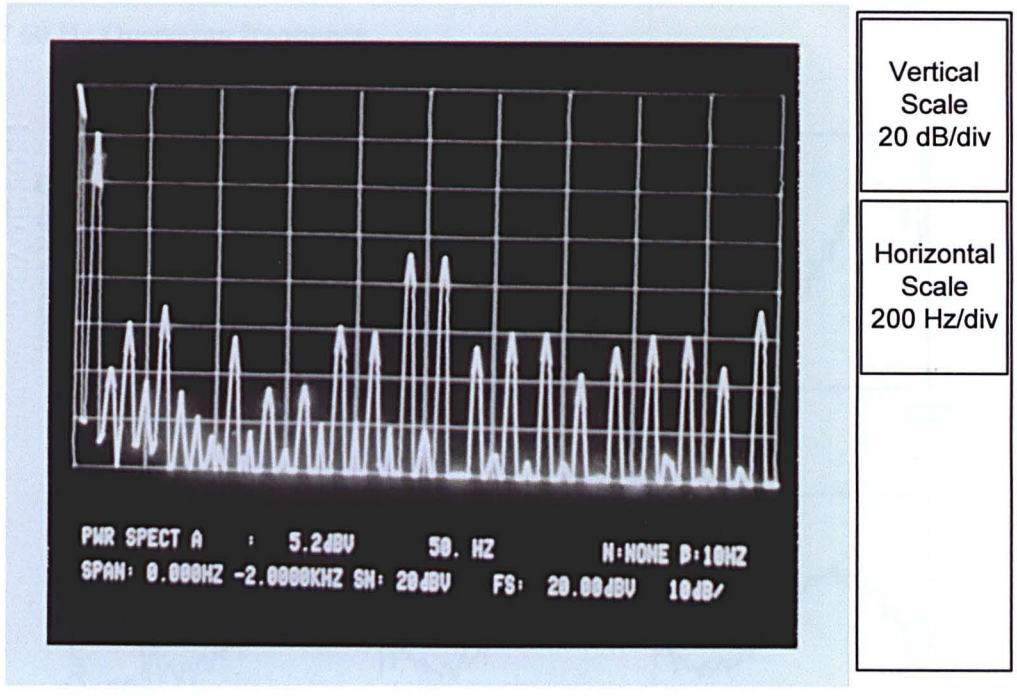

Figure 4.28 : *Line Current Spectra at 50 Hz*

4.5.7 60 Hz Operating frequency

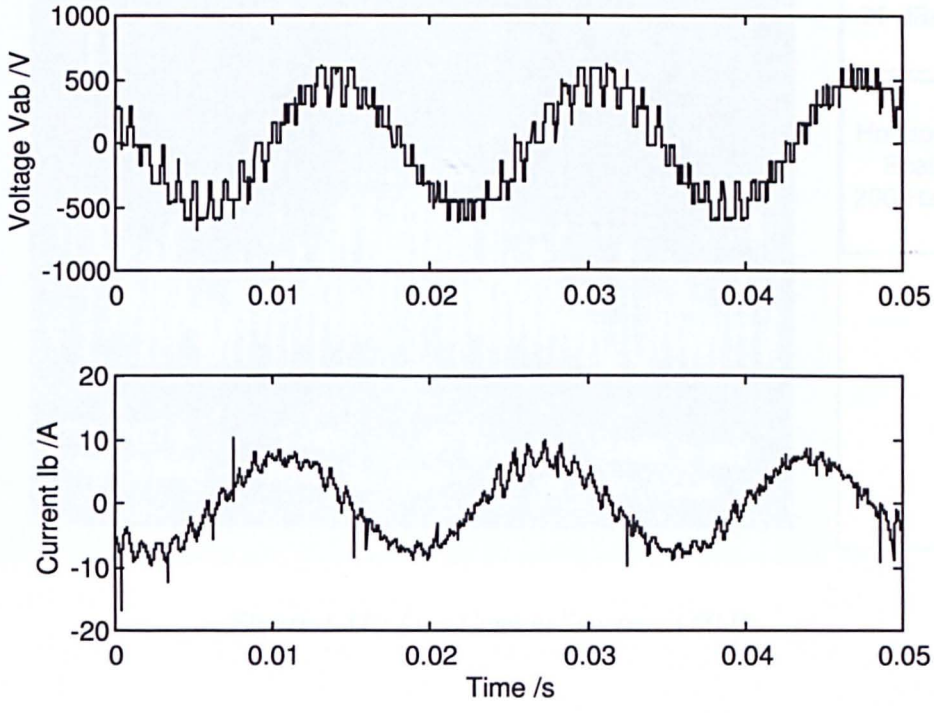

Figure 4.29 : *Operating result at 60 Hz*

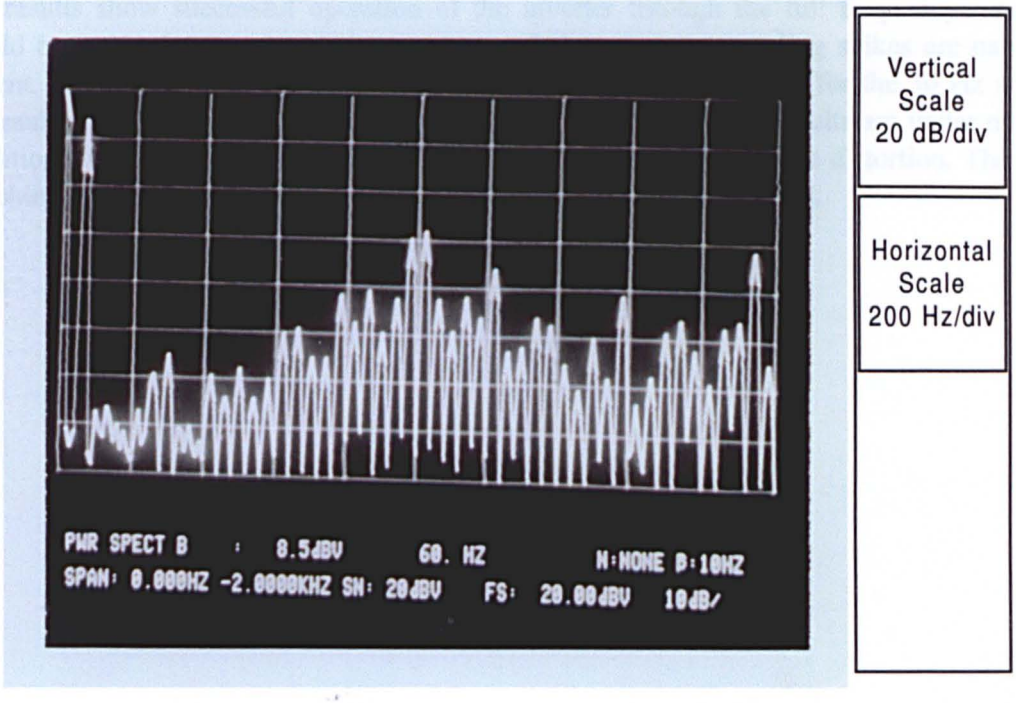

Figure 4.30 : *Phase Voltage Spectra at 60 Hz*

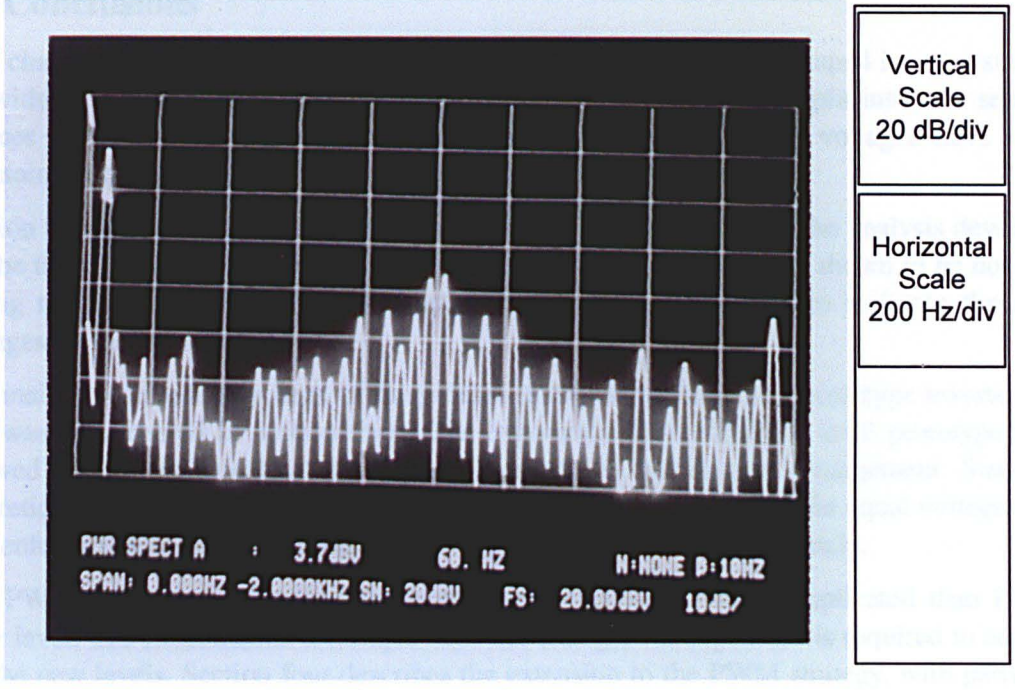

Figure 4.31 : *Line Current Spectra at 60 Hz*

4.5.8 Discussion of Results

The results show successful operation of the inverter through the full frequency range. It should be noted that traces are shown as recorded, and some sampling spikes are naturally present. The sinusoidal nature of the voltage waveform is very visible for the 50 Hz and 60 Hz results and the respective current waveforms reflect this. These results are under no load conditions, which represent the worst case condition for measuring the distortion. The peak switching harmonics in the spectra are around one tenth the fundamental.

4.6 Conclusions

This chapter has presented the operation of a basic five level diode clamped inverter suitable for within a motor drive system. The circuit uses a DC link which is split into four separate sources to provide the five levels in the output waveform. These voltages have to be maintained equal if successful operation is to be achieved.

Section two addressed the fundamental operation of the circuit. Using the analysis developed for the three level inverter, the node currents for the DC link have been shown to be non zero during real power operation. This means that a strategy is required to maintain the equal voltages on the capacitors.

The main objective at this stage of the process is the construction of a prototype inverter, and this was documented in section three. The experience from the three level prototype build allowed a better technical solution to be achieved for the physical arrangement. Since the theoretical analysis showed that the capacitor voltages would not maintain equal voltages, this was enforced by the use of a supply transformer to feed the levels separately.

The PWM requirement for the five level inverter becomes more complicated than for the three level. The fundamental technique does not change, but expansion is required to account for the new levels. Section four describes the extension to the PWM strategy, with particular attention to the level changeover and selection of the carrier for fast transients.

Results have been presented of the inverter operating at no load on the same Mitsubishi machine used during the testing of the three level (The rating of the supply transformer prevented operation at full power). Full harmonic analysis has been provided to show the effects of the carrier selection techniques.

4.7 Chapter References

[1] R. W. Menzies, P. Steimer, J. K. Steinke, "Five-Level GTO Inverters for Large Induction Motor Drives", IEEE Transactions on Industry Applications, Vol. 30, No. 4, July/Aug. 1994, pp 938-944.

Chapter 5

The Five Level Inverter – Advanced Motor Drive

Chapter Contents

5.1 Introduction

Whilst the five level inverter is fully functional when supplied by transformers in the arrangement described in the previous chapter, it is desirable to operate from a single DC link with the voltage levels derived using a series arrangement of four capacitors. A single DC link allows the use of a conventional supply arrangement (i.e. a medium voltage rectifier). If this is to be achieved, some form of balancing strategy is required to regulate the voltages on the capacitor banks. This will be discussed in this chapter. Implementation of vector control will also be discussed, which provides a basis to fully demonstrate the operation of the circuit. The implementation of the vector control was actually done in parallel with the development of the capacitor balancing techniques.

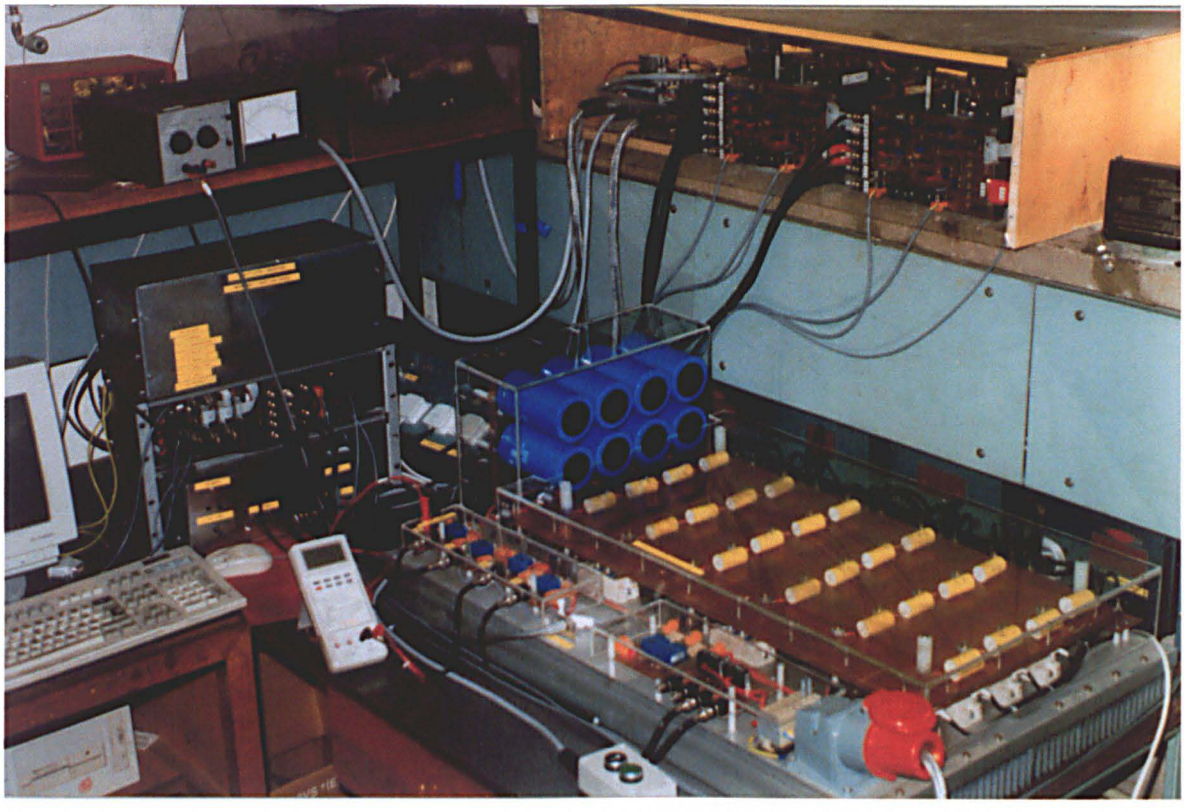

Figure 5.1 : *Complete five level inverter*

5.2 Vector Control Implementation

Over the last few years, it has nearly become an industrial standard to implement some form of high performance control on a commercial inverter. Field orientation, or "vector control" [1] provides several advantages over the conventional V/f control technique. The basis of V/f control is the steady state induction machine model. If the motor is required to rapidly change speed, then a more complicated approach has to be taken

5.2.1 Field Orientation: The basics

The induction machine, like most electromagnetic machines, produces torque by the reaction of flux and current. In order to maximise the torque generated, the field and current must be orientated perpendicularly. For a DC machine, the stator magnet (be it made of a magnetised material, or an electromagnet) provides the field, and the rotor currents react with this producing torque. The brushes and commutator enforce the quadrature relationship. Figure 5.2 shows a basic diagram of the interactions within the machine.

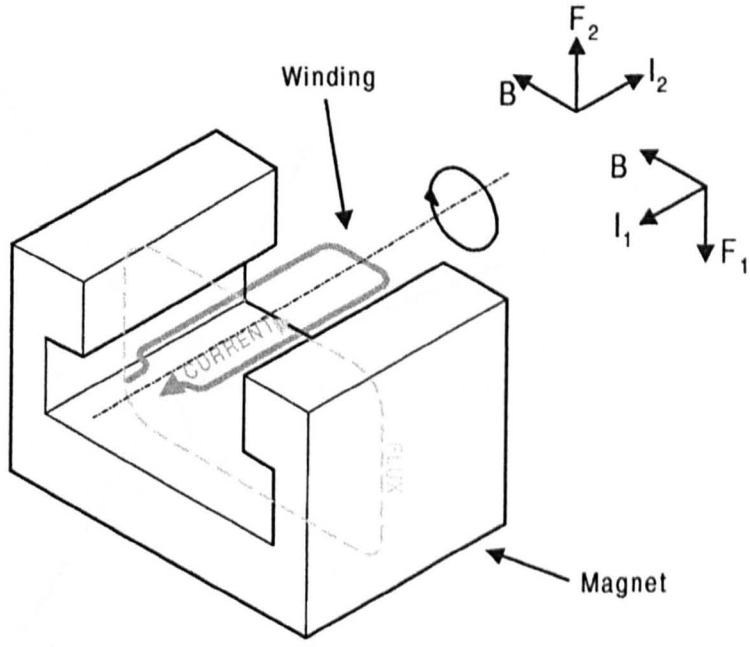

***Figure 5.2** : Diagrammatic DC Machine*

Within a constant field, B, the torque produced is directly proportional to the instantaneous current in the armature. Closed loop torque control is therefore simple to implement. The induction machine on the other hand does not benefit from this natural simplicity.

The conventional induction machine [2] can be considered to have two three phase distributed windings, one on the stator and one on the rotor. The rotor winding is effectively shorted (for a standard cage rotor machine). When a voltage is applied to the stator winding, and a current produced, a rotating magnetic field is generated in the machine. The speed at which this field rotates depends on the frequency applied, and the number of poles in the winding.

If the rotor is rotating at a different speed to the field, then a voltage will be induced in the rotor windings due to the time varying magnetic field. Since the winding is shorted, a current will flow in the rotor. The necessary conditions for torque generation are now present in the machine, being flux and current. The flux and current are inherently coupled together, since

the motor is effectively a transformer. In order to achieve high performance control, the field current and torque current have to be de-coupled. Vector control is a method of achieving this.

The basis of vector control, as the name suggests, is vector analysis of the machine. Using a two pole machine as the starting point (higher pole numbers being electrically equivalent), the three phase windings are physically located at 120° angles. Using this information to provide the directions and the instantaneous currents to provide the magnitudes, then by addition a single current vector can be defined. Figure 5.3 shows an argand diagram of the vector addition.

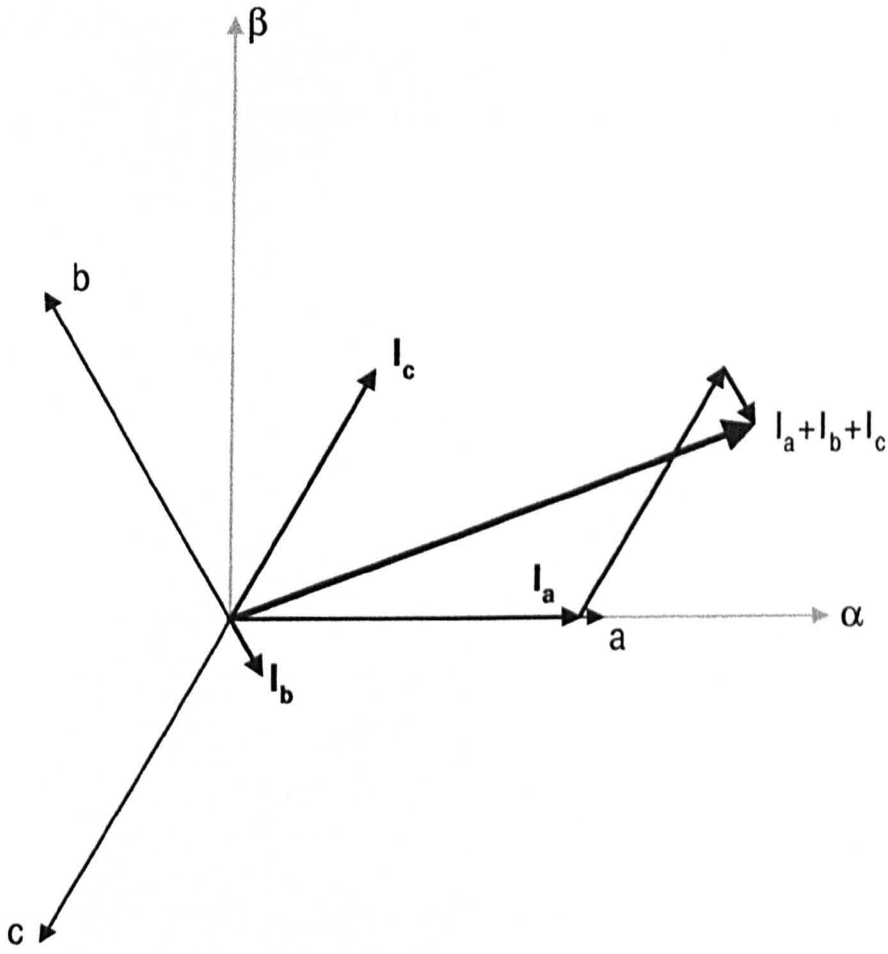

Figure 5.3 : *Argand diagram of vector addition*

Mapping the total vector on the fixed frame of reference (α,β) then the AC current equations are reduced down to two time varying equations. The three phase currents are defined as being balanced, with arbitrary phase γ.

$$\begin{pmatrix} i_a \\ i_b \\ i_c \end{pmatrix} = \sqrt{2}I \begin{pmatrix} \cos(\omega t + \gamma) \\ \cos\left(\omega t + \gamma - \frac{2\pi}{3}\right) \\ \cos\left(\omega t + \gamma - \frac{4\pi}{3}\right) \end{pmatrix} \qquad [5.1]$$

$$\begin{pmatrix} i_\alpha \\ i_\beta \end{pmatrix} = \begin{pmatrix} \cos(0) & \cos\left(\frac{2\pi}{3}\right) & \cos\left(\frac{4\pi}{3}\right) \\ \sin(0) & \sin\left(\frac{2\pi}{3}\right) & \sin\left(\frac{4\pi}{3}\right) \end{pmatrix} \begin{pmatrix} i_a \\ i_b \\ i_c \end{pmatrix} \quad [5.2]$$

$$\begin{pmatrix} i_\alpha \\ i_\beta \end{pmatrix} = \begin{pmatrix} \frac{3I}{\sqrt{2}}\cos(\omega t + \gamma) \\ \frac{3I}{\sqrt{2}}\sin(\omega t + \gamma) \end{pmatrix} \quad [5.3]$$

Equation 5.3 defines the result of the vector addition. The three currents have been combined to create one rotating vector. The key stage is to map the current vector onto a rotating frame of reference (d,q). If this frame rotates at the same frequency as the current vector, then the desired DC quantities are created.

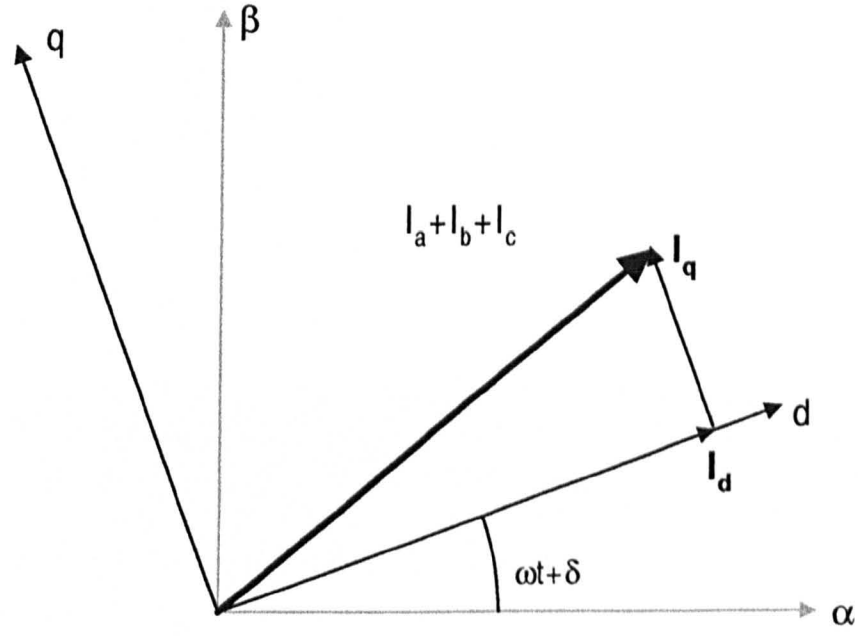

Figure 5.4 : *Mapping of the current vector onto the rotating d-q frame*

$$\begin{pmatrix} i_d \\ i_q \end{pmatrix} = \begin{pmatrix} \cos(\omega t + \delta) & \sin(\omega t + \delta) \\ -\sin(\omega t + \delta) & \cos(\omega t + \delta) \end{pmatrix} \begin{pmatrix} i_\alpha \\ i_\beta \end{pmatrix} \quad [5.4]$$

$$\begin{pmatrix} i_d \\ i_q \end{pmatrix} = \begin{pmatrix} \frac{3I}{\sqrt{2}}\cos(\gamma - \delta) \\ \frac{3I}{\sqrt{2}}\sin(\gamma - \delta) \end{pmatrix} \quad [5.5]$$

Equation 5.5 for the currents referenced in the d-q frame shows quantities that are dependent on the relative phases of the currents and the reference. There is no time variation. By analysing the induction motor in this rotating frame, a transient model can be generated which is independent of the operating frequency.

5.2.2 Indirect Rotor Flux Orientated Control

In order to apply the rotating frame analysis, a basic assumption has to be made on how to align the reference with the physical machine. The usual arrangement is to align the d-axis with the rotor flux. Current in the d-axis is assumed to be the "magnetising current", i.e. the current linked to the machine flux. The q-axis is then naturally aligned with the torque producing current.

There are two common models for machine control. Direct rotor flux orientated (DRFO), and indirect rotor flux orientated (IRFO). The simplest to implement is IRFO control. This method uses the slip equation and knowledge of the rotor speed to achieve orientation. DRFO requires some form of flux feedback from the machine.

The derivation of the actual vector control equations is not given here. There are many publications that give very through explanation [3]. The resulting stator equations are given below for the constant flux condition.

$$v_d = R_s i_d + \sigma L_s \frac{di_d}{dt} - \omega_e \sigma L_s i_q \qquad [5.6]$$

$$v_q = R_s i_q + \sigma L_s \frac{di_q}{dt} + \omega_e L_s i_d \qquad [5.7]$$

$$\omega_{sl} = \frac{1}{\tau_r i_d} i_q \qquad [5.8]$$

$$\tau_r = \frac{L_r}{R_r} \qquad [5.9]$$

These equations are quoted in their simplest forms, and with several approximations. In practice this is sufficient for implementing a basic vector control scheme. The aim of this project was not to push the boundaries of vector control. The implementation of vector control does provide an important benchmark in evaluating the converter.

The basic control implementation of these equations is shown in figure 5.5.

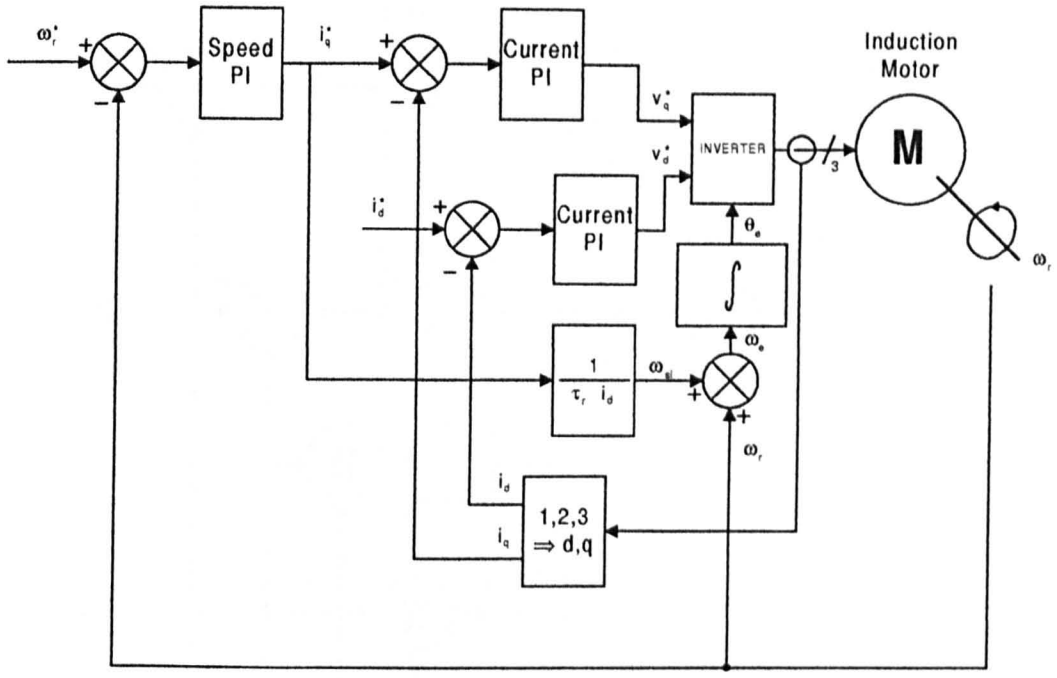

Figure 5.5 : *Vector control arrangement*

Equations 5.6 and 5.7 show three terms. Figure 5.6 shows the circuit analogy for the q-axis equation. The similarity to the standard DC machine model is clearly visible.

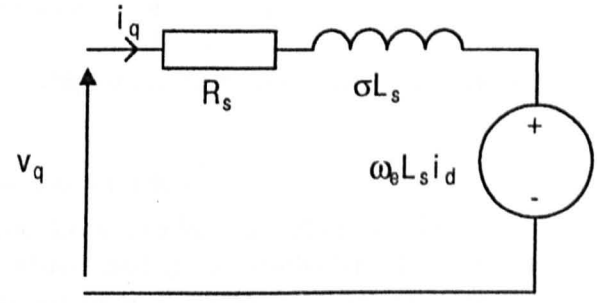

Figure 5.6 : *q-axis equivalent circuit*

Applying a PI controller can provide fast and accurate current control assuming the back emf term is constant. This assumption is not true during a speed transient. Acceleration or deceleration will insert a ramp disturbance into the control loop, which the PI controller cannot cancel. This results in a steady state error in the current control. In order to overcome this, it is conventional to add compensation terms to the outputs of the current controllers. This is shown in figure 5.7.

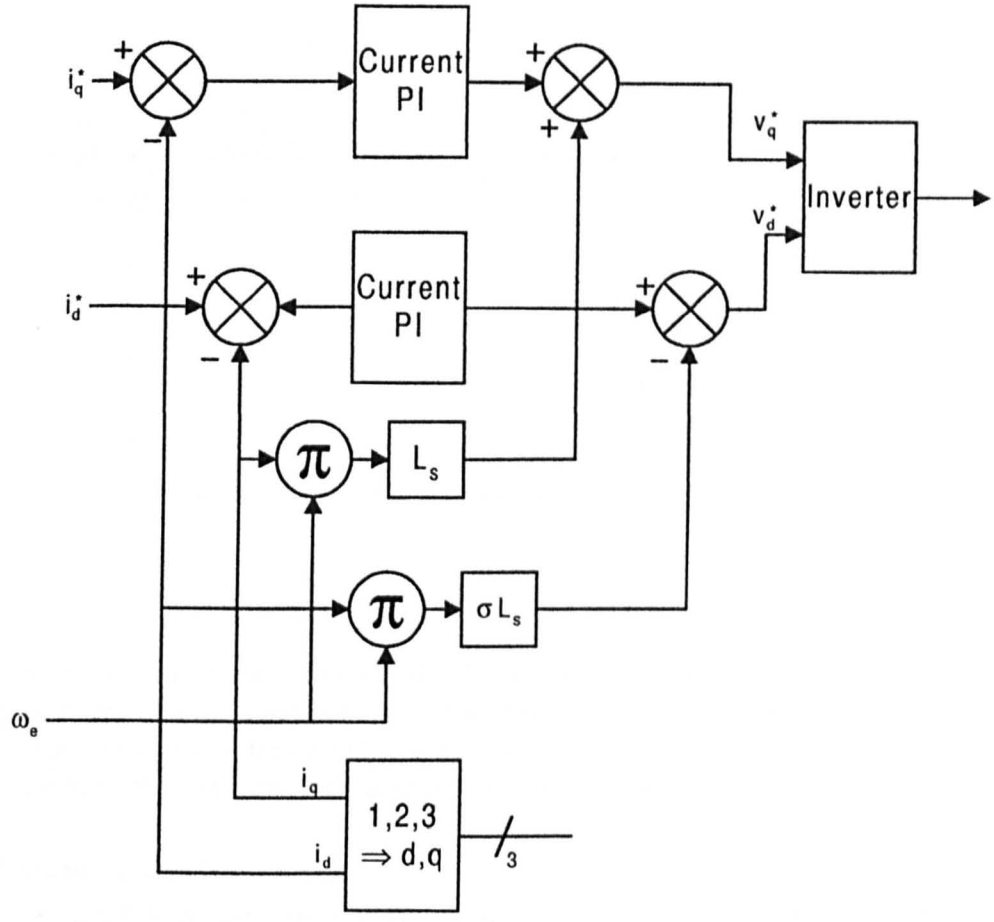

Figure 5.7 : *Addition of compensation terms*

5.2.3 Current Control Loop Design

With the compensation terms in place the design of the current controllers is reasonably straightforward. The d-axis and q-axis controllers have different actions in the control structure. Since the d-axis current is effectively the machine flux, the demand quantity is constant. The controller's job is regulatory. The q-axis current is the torque component, and needs to be changed rapidly. The controller is acting as a servo. However, since the electrical models are identical (excluding the back emf terms which are handled by the compensation), a common design can be used for both the d and q axis controllers.

The design does become more complex when the system delays are taken into account. Integrating the control into a PWM structure adds a delay in the forward path, since switching times are normally calculated during the previous cycle (or half cycle for asymmetric PWM). The current feedback will normally be filtered to remove switching frequency components and extract the fundamental. Assuming the filter response is significantly higher than the control bandwidth, the gain can be treated as a constant (and compensated for), and the only effect on the signal is a fixed time delay.

The complete control model including all the delays is shown in figure 5.8.

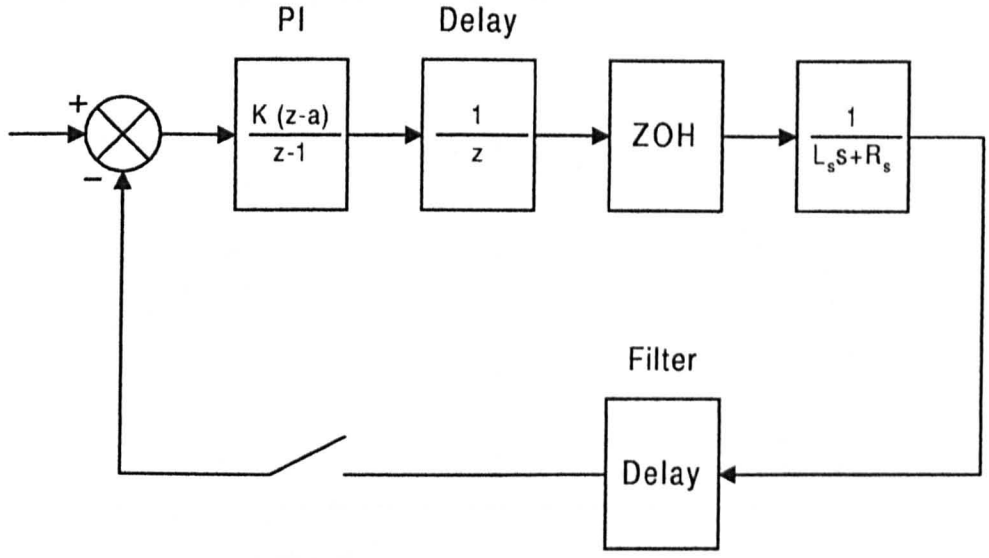

Figure 5.8 : *Current loop design model*

The current loop is commonly designed to be as fast as possible whilst achieving a sensible damping factor. It is the feedback delay that often limits the system performance, since it is represented by a zero in the closed loop system. As with all classical control designs, if the poles are faster than this zero, then an excessive overshoot will occur.

5.2.4 Speed Control Loop Design

The fast current loops are nested within the speed loop. The bandwidth of the speed loop is relatively slow, usually defined by the speed sampling period and practical requirements. The use of a digital incremental encoder limits the discretisation interval. The selection of sampling frequency has to be made as a trade-off between update frequency (hence bandwidth) and resolution. The control loop design model is shown in figure 5.9. Speed is estimated from the angle change over the previous sampling period. This does introduce a feedback delay that may become significant if the required bandwidth is too high.

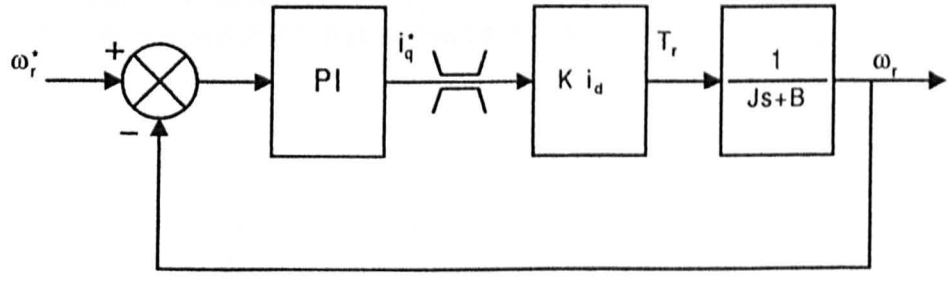

Figure 5.9 : *Speed loop design model*

5.2.5 Field Weakening

Operation beyond the normal base speed of the machine is limited by the back-emf term in the equations and the voltage limit of the inverter. If the control is to operate successfully, then some headroom in voltage has to be allowed for the current controller. Because of this it not actually possible to operate all the way to base speed. If this is to be achieved, the back-emf has to be reduced. If the d-axis current is reduced, the decrease in flux will result in the

desired change. By weakening the field, the operation range can be extended, as shown in figure 5.10.

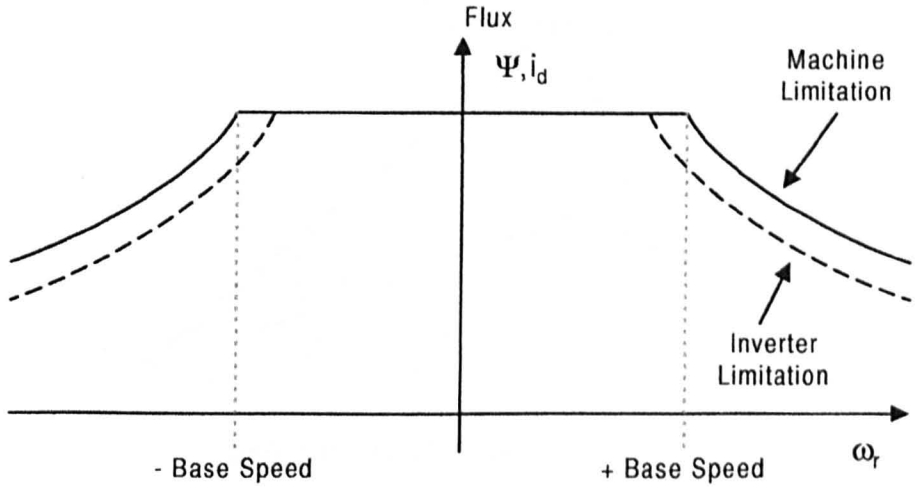

Figure 5.10 : *Field Weakening for increased speed range*

From the equations it can be seen that the torque will be reduced, and the slip will change. At the same time certain other changes occur in the machine operation. Under normal rated flux conditions for a typical induction motor, the magnetic flux path will normally be entering saturation between the slots. The machine is on the verge of non-linearity. By decreasing the flux, this saturation will be lost. This has a knock on effect on the leakage reactance. This will influence the rotor time constant, and can result in loss of orientation unless compensated for.

In the case of this work, the field weakening was purely used to allow base speed to be reached (50Hz) without loss of control due to current controller saturation.

5.2.4 Addition of Vector Control to the Five Level Inverter

The outputs from the current controllers are voltage references in the d-q axes. These need to be mapped into something more conventional for the PWM technique to generate. From the PWM description in chapter 3 section 4 it can be seen that the sinusoidal technique used is based around a reference angle, and an amplitude. The d-q quantities map out as shown in figure 5.11.

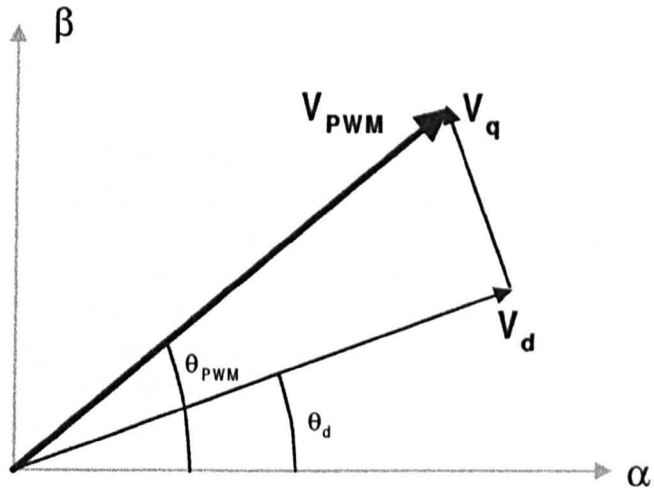

Figure 5.11 : *Resolving of voltage demands*

This is a basic trigonometric arrangement, described by the following equations.

$$\theta_{PWM} = \theta_d + \tan^{-1}\left(\frac{v_q}{v_d}\right) \qquad [5.10]$$

$$V_{PWM} = \sqrt{{v_d}^2 + {v_q}^2} \qquad [5.11]$$

Implementation of equation 5.10 is difficult, due to the on line calculation of the inverse tangent. The ratio of d to q voltages can vary over an infinite range. This does not lend itself to the simple look up table kind of approach that is preferable. An alternative approach is required. Equation 5.11 is simpler, and can be implemented with a basic look up table. An integer table can become inaccurate at small values, but this can be overcome by simple scaling techniques.

Assuming the amplitude is available, then this opens up alternatives to equation 5.10 for the calculation of the angle.

$$\theta_{PWM} = \theta_d + \sin^{-1}\left(\frac{v_q}{V_{PWM}}\right) \qquad [5.12]$$

$$\theta_{PWM} = \theta_d + \cos^{-1}\left(\frac{v_d}{V_{PWM}}\right) \qquad [5.13]$$

Inverse sine and cosine tables are simpler, since the range is bounded. Due to the limitation of using integer numbers, both these tables are inaccurate as the ratios tend to unity. For example, if the q-axis voltage is much larger than the d-axis voltage, then the inverse sine produces a less accurate result than the inverse cosine. By having access to both tables, the accuracy can be increased, but this is wasteful of the limited processor memory available. From basic trigonometry, the following equation can be derived.

$$\theta_{PWM} = \theta_d + \frac{\pi}{2} - \sin^{-1}\left(\frac{v_d}{V_{PWM}}\right) \qquad [5.14]$$

This provides the result without the need for an extra lookup table. With these alternate equations the output of the vector current controllers can be easily integrated with the PWM generation.

5.2.4 Results of Full Control Scheme

This section presents results from the operation of the inverter under vector control. Various transient tests were completed in order to demonstrate the control. The initial work was completed on a known 4kW machine to enable rapid development of the various algorithms. The motor was then changed for an 11kW machine in order to push the inverter to it's limits. The capacitor balancing techniques described later in the chapter were in operation for the full tests. In order to achieve rapid deceleration of the motor, a resistive braking unit was employed over the total DC link.

TEST 1 : Current Control

The most essential part of the control is the fast current loops. Figure 5.12 shows the step response for both controllers on the 4kW machine. The rapid response is clearly visible. These step responses were recorded individually whilst the other controller was in steady state conditions.

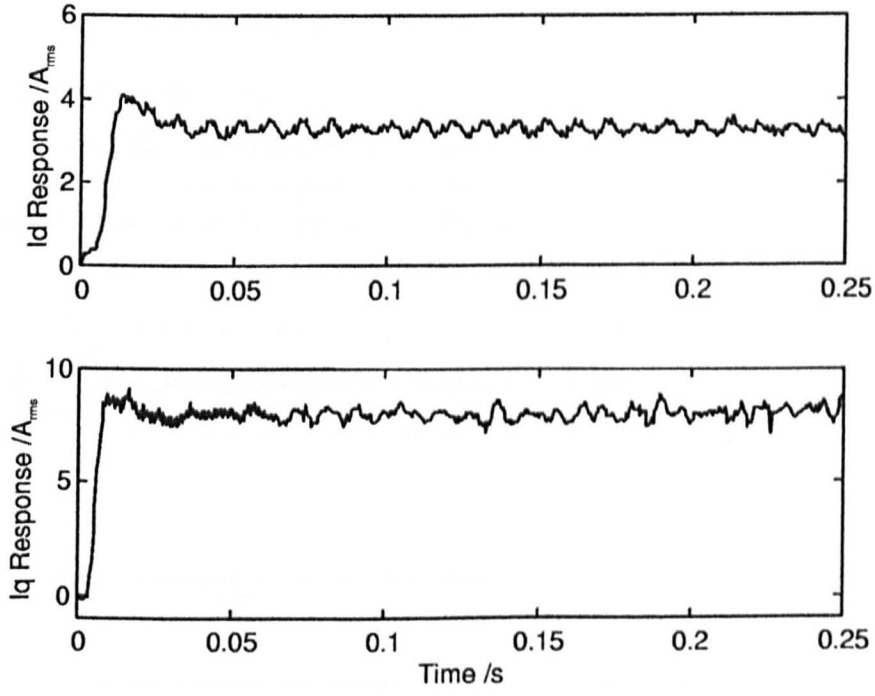

Figure 5.12 : *Independent control of dq-axis current*

TEST 2 : Speed Reversal ±30Hz

Figure 5.13 shows the motor phase current during a speed reversal of ±900rpm.

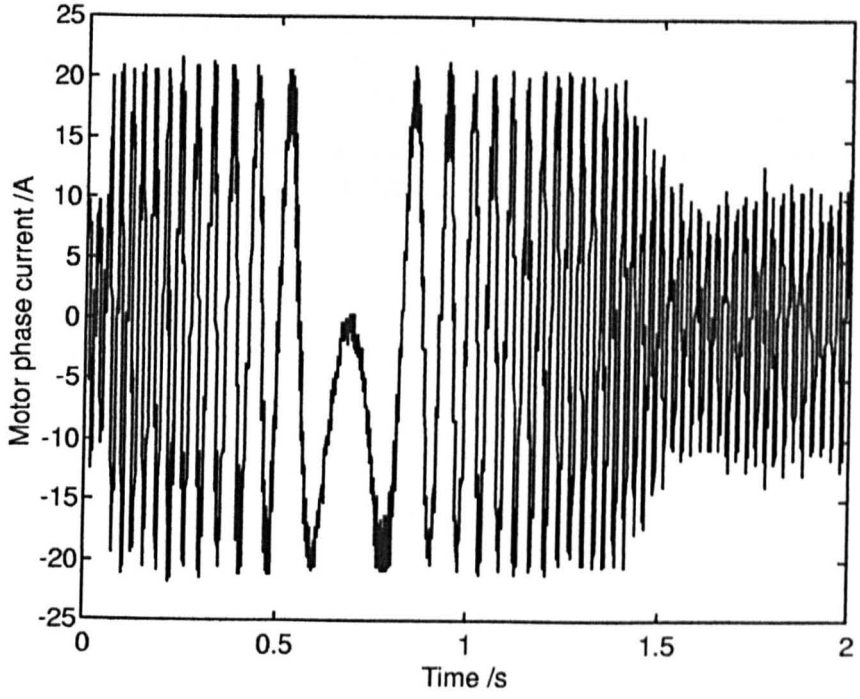

Figure 5.13 : *Motor Current During Speed Reversal*

TEST 2: Speed Reversal ±50Hz

Figure 5.14 shows the transformed motor current and motor speed during a speed reversal of ±1500rpm. In order to achieve this the control has to reduce the field at full speed, which can be seen in the d axis current (the grey trace in the figure).

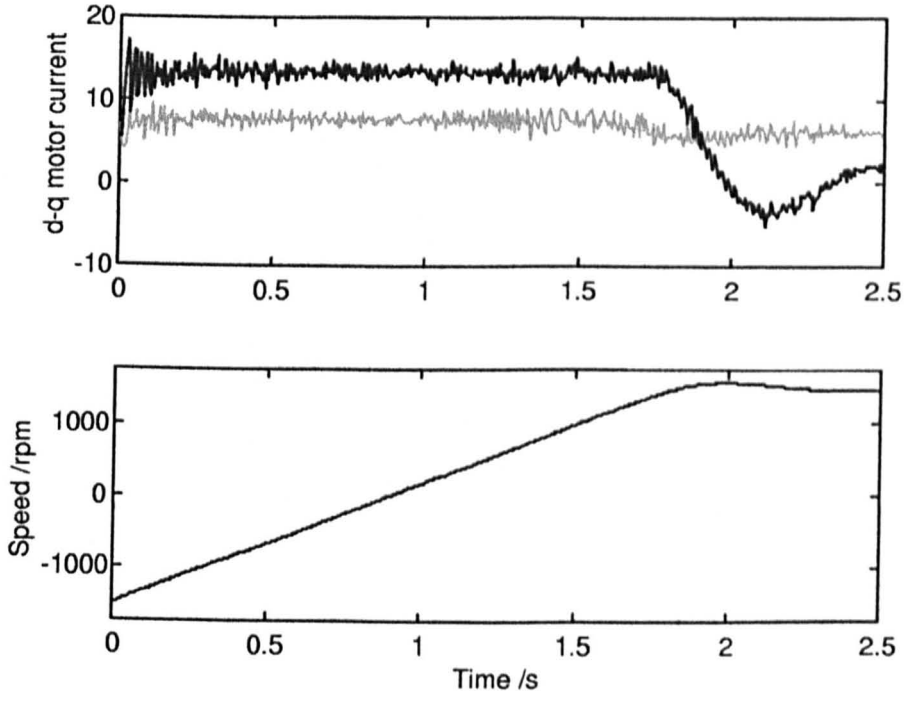

Figure 5.14 : *Speed Reversal*

5.2.5 Conclusions

This section has described the basic principles of a simple closed loop vector control scheme. Implementation of such a scheme within the control of the five level inverter has been discussed. The control has been fully tested and results presented to verify the operation.

The vector control provides an important means for evaluating the operation of the inverter and capacitor balancing techniques described in the following sections.

5.3 Techniques for Capacitor Balancing

For the three level inverter, a simple technique was introduced as 'neutral point control' which provided balance of the capacitor voltages. This task becomes more complex with an increased number of levels. In the previous chapter, the operation of the circuit was demonstrated with a transformer supplied DC link (illustrated in figure 4.9). This ensures balance of the capacitor voltages, but at the expense of the input current, since the loading will not be symmetrical. Regeneration will also cause imbalance unless each level has it's own independent brake unit.

Various techniques have been suggested for capacitor balancing, and these different approaches are described here. The analysis of these different techniques will provide justification to the approach that has been taken.

5.3.1 Independent Power Supplies

The ideal supply arrangement, if the supplies can be rated appropriately, is to use separate DC power supplies for the various levels. This has been suggested [4] as being particular suitable for battery or solar panel supplied applications. In these cases the separate supplies are inherent. The power loading of the various supplies will not be constant, and this may limit the operation in particular situations.

5.3.2 SVM Control

Space vector modulation has been suggested previously as a technique to balance the neutral point on the three level inverter. The question then arises to the ability of redundant state selection on an n-level inverter with SVM control to regulate all the capacitor voltages on an n-level inverter.

The implementation of neutral point control is reasonably simple, since the current drawn from the node is zero if modulation is balanced. For an n-level inverter this is made more complex, since the currents into the additional nodes are not naturally zero. This was shown in figure 4.4.

Figure 5.15 shows one sector of the space vector map for a five level inverter, illustrating the different switch states for a particular vector. Similar problems to those described for neutral point control are still applicable, with no choice in vector at high modulation amplitudes, and no benefit from different zero vectors at low modulation amplitudes. There are often several alternate switching states for any particular vector, which implies some control of the currents into the DC link should be possible.

It has been demonstrated [5] that for a four level inverter, the balancing could be achieved on a four level inverter provided the modulation amplitude was restricted. For high modulation amplitudes an additional circuit was required.

Selection of the switch state cannot provide balancing of the capacitor voltages for multi-level inverters with more than three levels without additional circuitry if the full operating range is to be utilised.

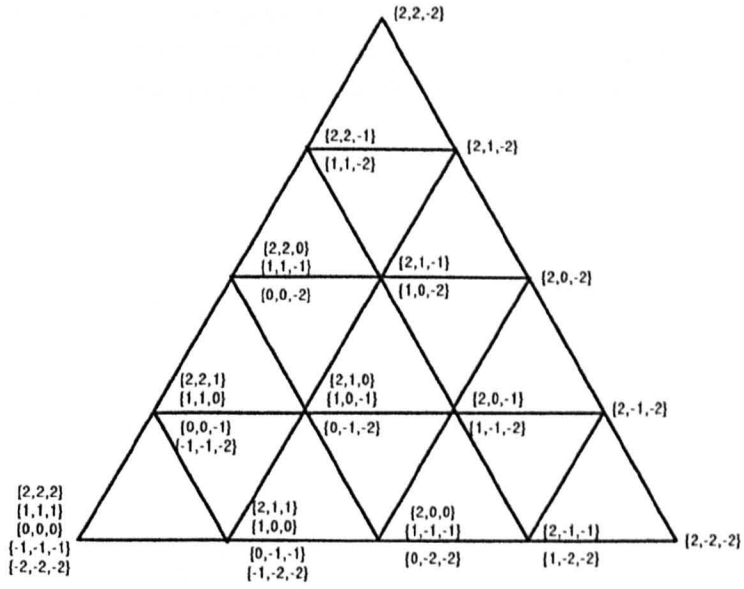

Figure 5.15 : *One sector from the SVM map for the five level inverter*

5.3.3 Back to Back Operation

It has been demonstrated that the capacitor voltages can be regulated in a back to back arrangement [6][7]. A typical arrangement for a four level inverter is shown in figure 5.16. Control for this arrangement is often based on SVM, or a hybrid sub-harmonic PWM with intelligent redundant state selection. The selection of which redundant state to employ on both the 'rectifier' and 'inverter' affects common mode voltage at the output and may induce problems with EMI from circulating earth currents. Unless sustained regeneration is required the additional cost, volume, and efficiency loss associated with the sinusoidal front end is unlikely to be popular for industrial applications.

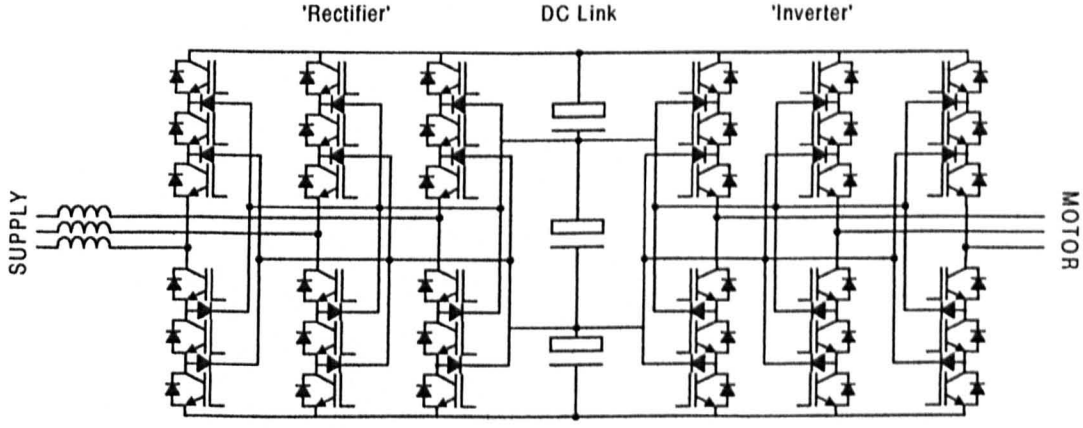

Figure 5.16 : *Back to back four level inverter*

5.3.4 Conclusions

In order for a diode clamped multi-level inverter to operate correctly, some form of balancing technique for the capacitor voltages must be implemented. For inverters with more than three levels, additional circuitry is required if a single DC link is to be employed. Assuming

sustained regeneration is not a requirement, the simplest solution is a switching regulator to inject current into the nodes of the DC link to regulate the capacitor voltages. Any switching circuit needs to provide balancing throughout the whole operating range of the inverter.

5.4 Capacitor Balancing Circuit

The review of capacitor balancing techniques in the previous section concluded that the addition of extra circuitry to the basic inverter circuit is required if operation from a single DC link is to be achieved. It has already been discussed that this is likely to be the preferred option for many applications.

This section will review the requirements for a suitable circuit, and the arrangement on the DC link. The new balancing circuit will then be discussed. Simulations will be provided (detailed in appendix 2) to confirm the design basis, along with practical operating results.

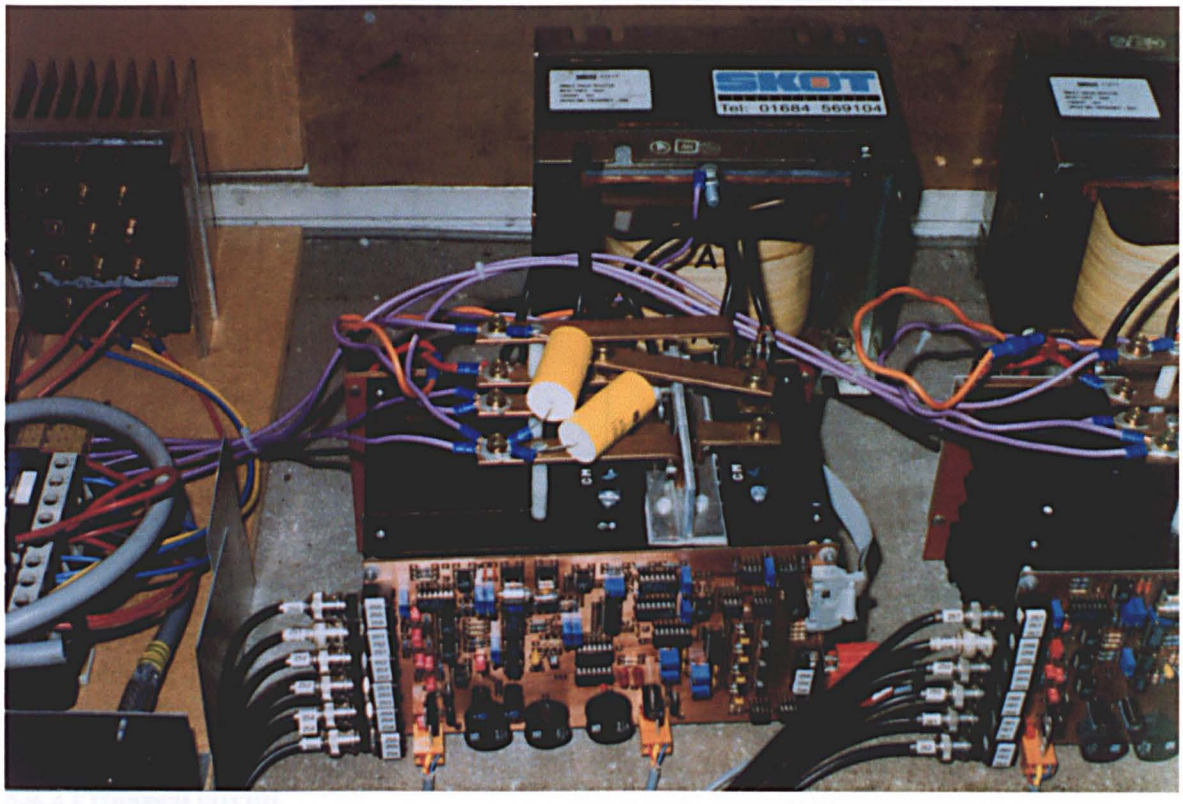

***Figure 5.17** : Photograph of Balancer Circuit*

5.4.1 Circuit Requirements

It was shown in the analysis in chapter three that variation in the voltages on the capacitor bank on the three level inverter was a direct result of current being drawn from the intermediate node (the neutral point) in the capacitor bank. Voltage balance is achieved by cancelling this current so that the voltages will remain undisturbed. Whilst this was simple to achieve on the three level (since the current cancellation could be achieved through modification of the switching pattern), the analysis in chapter four showed that a mean current is drawn from some of the intermediate nodes. This is part of the fundamental operation of the circuit in a real power application. Any additional balancing circuit will have to provide the currents predicted by equations 4.12 to 4.16 in the previous chapter.

Since the five level inverter is symmetrical about the neutral point, the problem can be split into balancing of the top two capacitors and the bottom two capacitors, as independent systems. This is shown in figure 5.18.

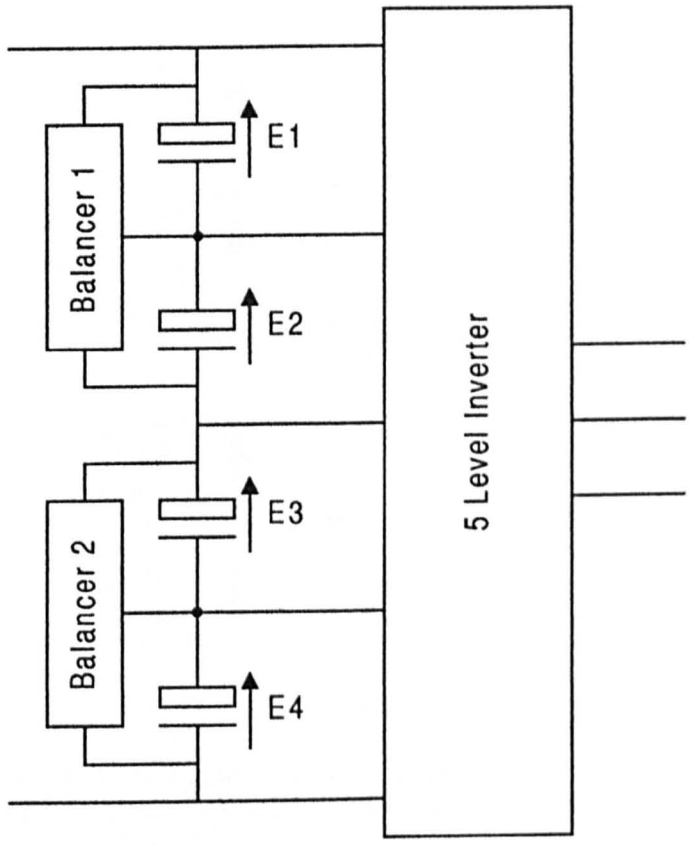

Figure 5.18 : *Balancing arrangement*

The current drawn by the inverter from the nodes was defined by equation 4.17. This can be positive or negative depending on the power factor in the AC load. The balancing circuit must be capable of handling both positive and negative current injection if operation is to be achieved with high performance four quadrant control.

5.4.2 Proposed circuit

Figure 5.19 shows the basic circuit that is proposed for the capacitor balancing. The physical circuit is identical to a phase of a three level inverter, with an inductor connected back to the centre point. Simpler circuits have been suggested for balancing in multi-level inverters [8] but these have been limited in their operational capability.

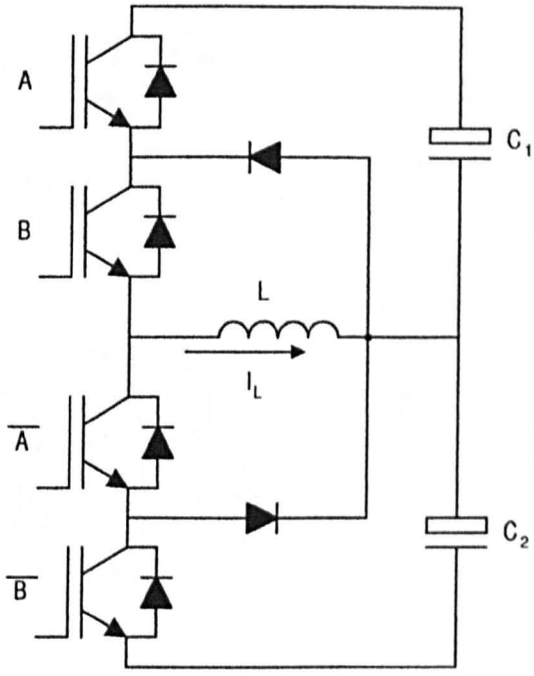

Figure 5.19 : *Balancing circuit*

An alternative drawing of the circuit is shown in figure 5.20. In this arrangement, the circuit resembles the classic 'flyback' converter. In this case the circuit is bi-directional, allowing power to be transferred in both directions.

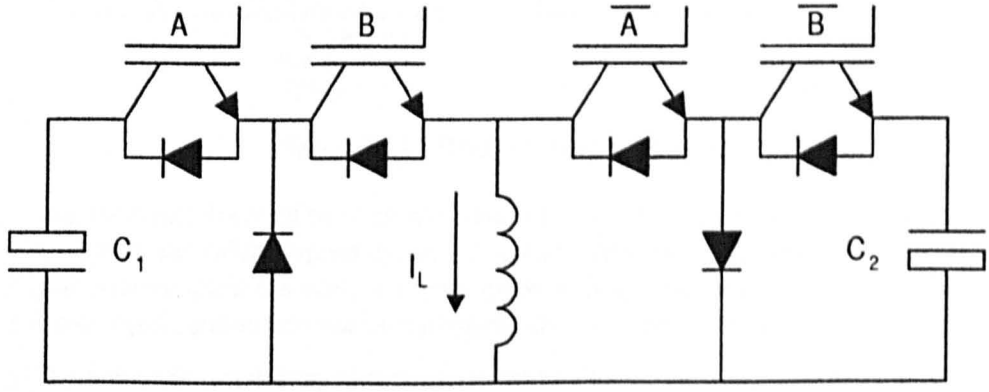

Figure 5.20 : *'Flyback' style arrangement*

5.4.3 Circuit Operation

The circuit operates by transferring energy/charge from one capacitor to the other via the inductor. The switching requirements (IGBTs switched as complementary pairs) have already been documented earlier, since the circuit is basically a single phase from a three level inverter driving an inductive load. Figure 5.21 shows the three permitted switch states with both positive and negative inductor current.

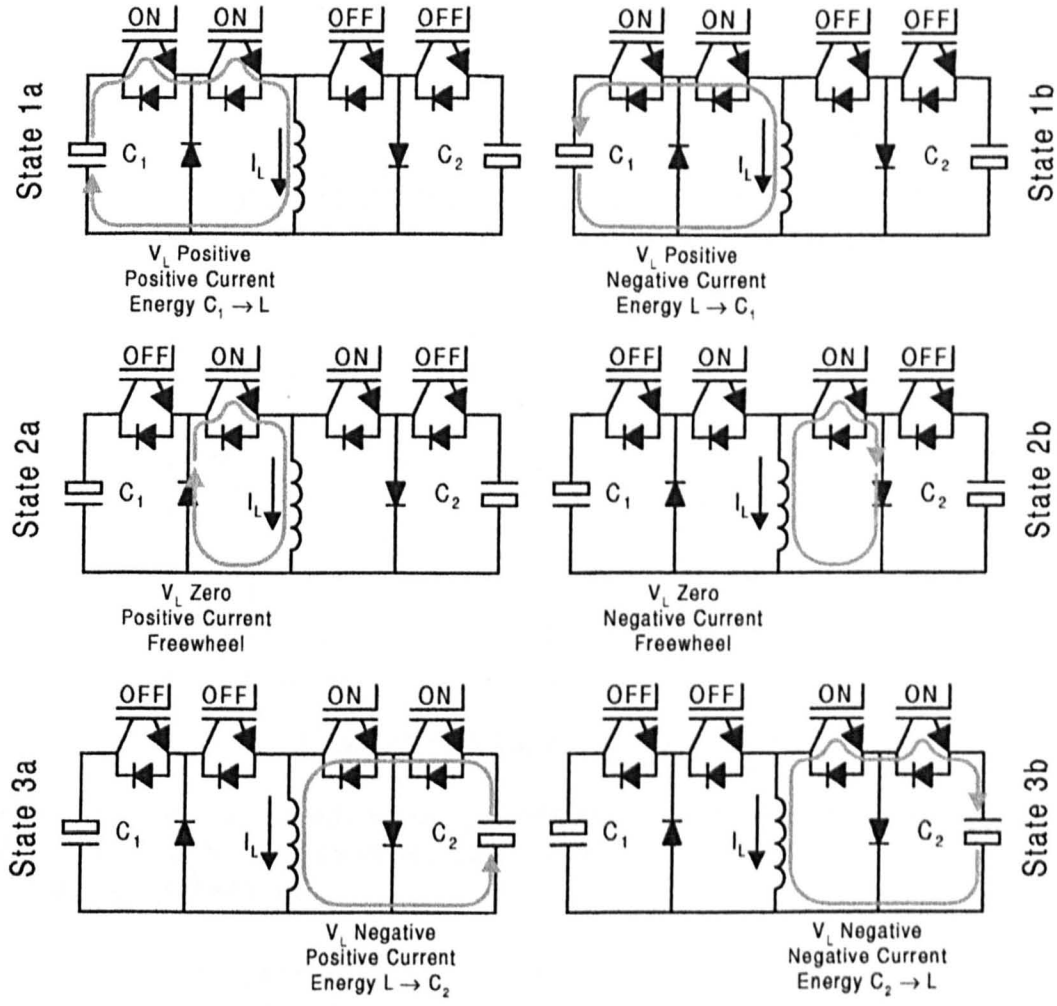

Figure 5.21 : *Balancer switching states*

By cycling back and forward through the states (1-2-3-2-1). Energy will be transferred from one capacitor to the other depending on the current direction. The time spent in state 2 is effectively wasted, since the current is just freewheeling. The state is used to complete the commutation cycle, and to prevent exceeding the device voltage rating.

The generation of the switching pattern is shown in figure 5.22. The technique used is based around a traditional triangle wave comparison technique. Two references are generated which symmetrically band the desired reference value. This is in fact an implementation of the dipolar sub-harmonic technique described in chapter two. In this case the offset between the two modulation waves is small. The reference determines the pattern duty cycle, and therefore the mean voltage on the inductor.

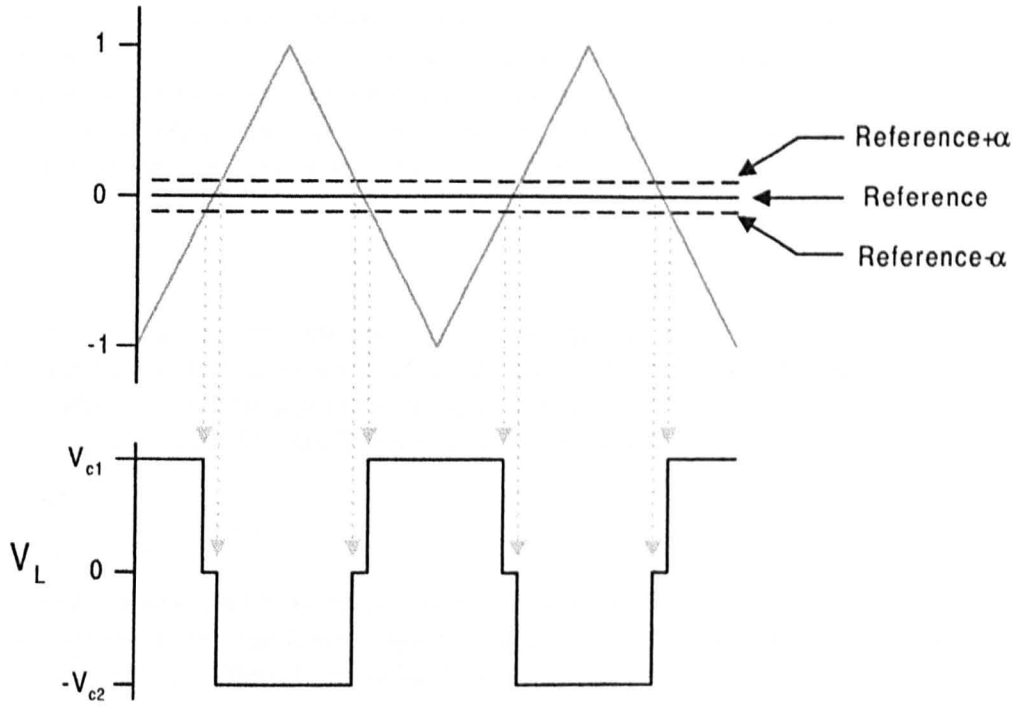

Figure 5.22 : *Balancer switching pattern*

Figure 5.23 shows an example operating condition. The mean inductor current is relatively small, with the current troughs going negative. In this condition all the states that were shown in figure 5.21 are being used.

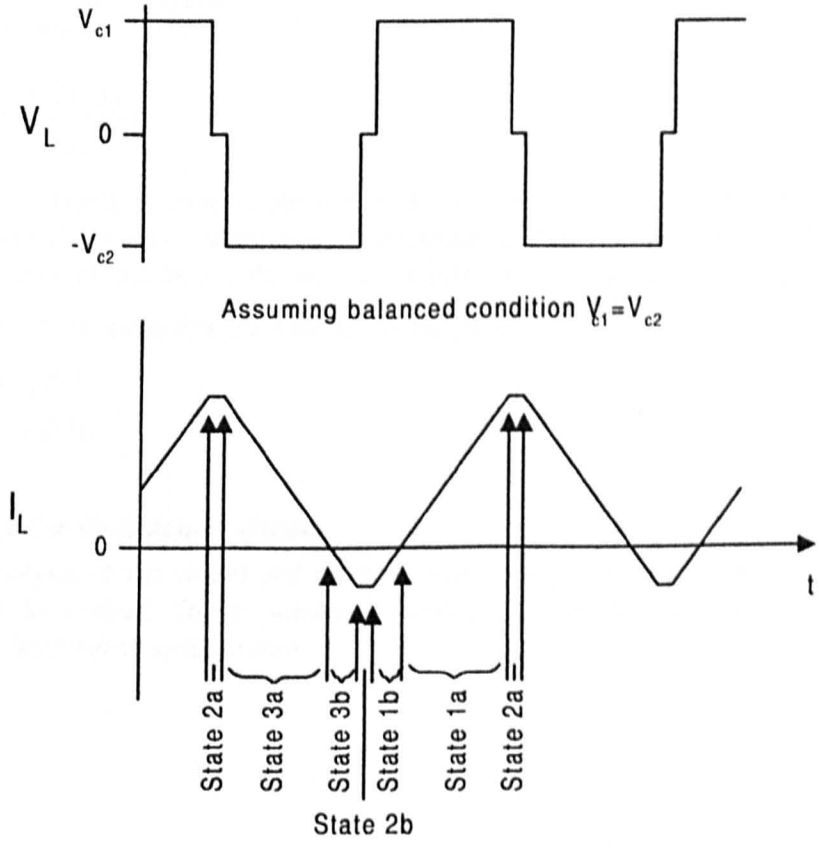

Figure 5.23 : *Balancer operation example*

In the example, the mean inductor voltage is zero, which results in a repeating current waveform with a constant mean value. The commutation period (state 2) is kept to a minimum, to maximise the current utilisation (since energy transfer between the capacitors does not occur during state two). The current ripple can be approximated to equation 5.16, with the assumption that the state 2 time is negligible.

$$\Delta I_L = \frac{V_C}{2 f_s L} \qquad [5.15]$$

This does assume the two capacitor voltages are equal at their normal operating point. The ripple current also defines the speed of response, and the maximum large signal bandwidth. If the switching is in its maximum or minimum condition, then a full period is allocated to either state one or state three. The maximum change of current will then be given by equation 5.16

$$\left.\frac{dI_L}{dt}\right|_{Maximum} = 2\Delta I_L f_s \qquad [5.16]$$

If the peak current capability is I_{max}, then the bandwidth can defined from the sinusoidal current capability. Assuming the frequency bandwidth limit is the -3dB gain point, then the sinusoidal current is defined by equation 5.17.

$$I_{sinusoidal} = \frac{I_{max}}{\sqrt{2}} \sin(2\pi f_{bw} t) \qquad [5.17]$$

By equating the maximum rate of change of current required with that defined above the large signal bandwidth limit can be derived.

$$\left.\frac{dI_L}{dt}\right|_{Maximum} = \frac{2\pi f_{bw} I_{max}}{\sqrt{2}} \qquad [5.18]$$

$$f_{bw} = \frac{\sqrt{2} f_s \Delta I_L}{I_{max} \pi} \qquad [5.19]$$

For a given switching frequency, the size of the inductor can be calculated from the desired ripple current, with a trade off against the bandwidth. In this case the switching frequency for the balancer was set the same as the inverter, at 1kHz, and a 10mH inductor used.

From the above equations this gives the following parameters.

$$\Delta I_L = 7.5A$$
$$f_{bw} = 135Hz$$

5.4.4 Control for the balancer circuit

From the analysis of the circuit and the switching strategy, an approximate Laplace block diagram can be derived. This is shown in figure 5.24. The current drawn by the inverter appears as a disturbance to the system.

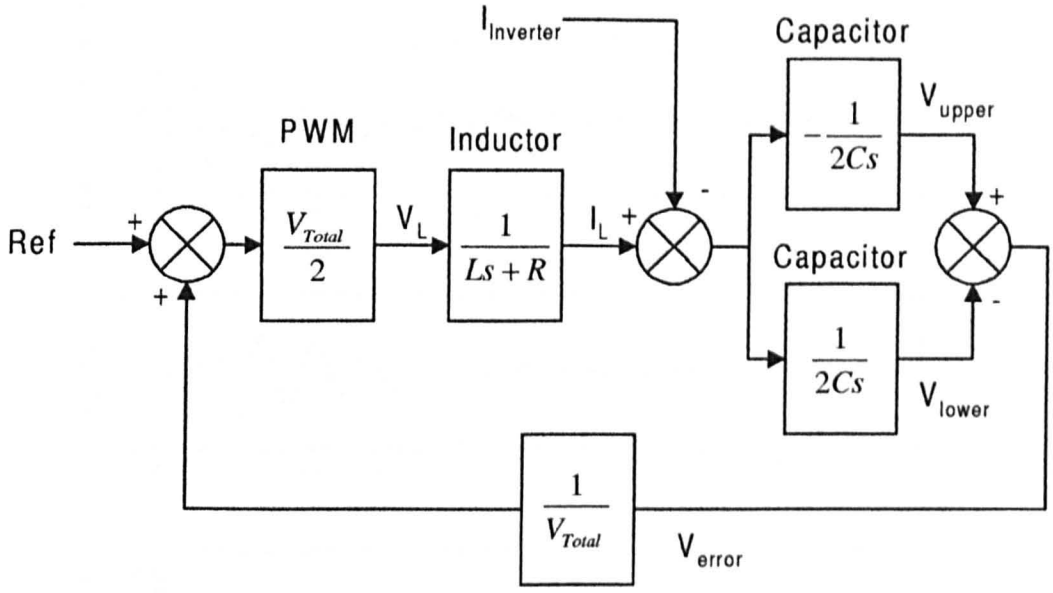

Figure 5.24 : *Balancer block diagram*

Two of the blocks contain the sum of the two capacitor voltages. It has been assumed that this remains constant, to ensure a linear system. The Laplace transfer function (ignoring the disturbance input) for the system is given in equation 5.20. In steady state, the difference between the voltages is directly proportional to the PWM reference.

$$\frac{V_{error}}{Ref} = \frac{\frac{V_{Total}}{2LC}}{s^2 + \frac{R}{L}s + \frac{1}{2LC}} \qquad [5.20]$$

The open loop system is second order, and oscillatory. Whilst the capacitors will balance, given the correct reference, the system is likely to be very poorly damped. Inserting the following values into the block diagram (which are correct for the practical system) the open loop system was simulated, and the result shown in figure 5.25. The system was started with the capacitor voltages offset to observe the settling response.

$$C = 4mF$$
$$L = 10mH \qquad [5.21]$$
$$R = 0.1\Omega$$

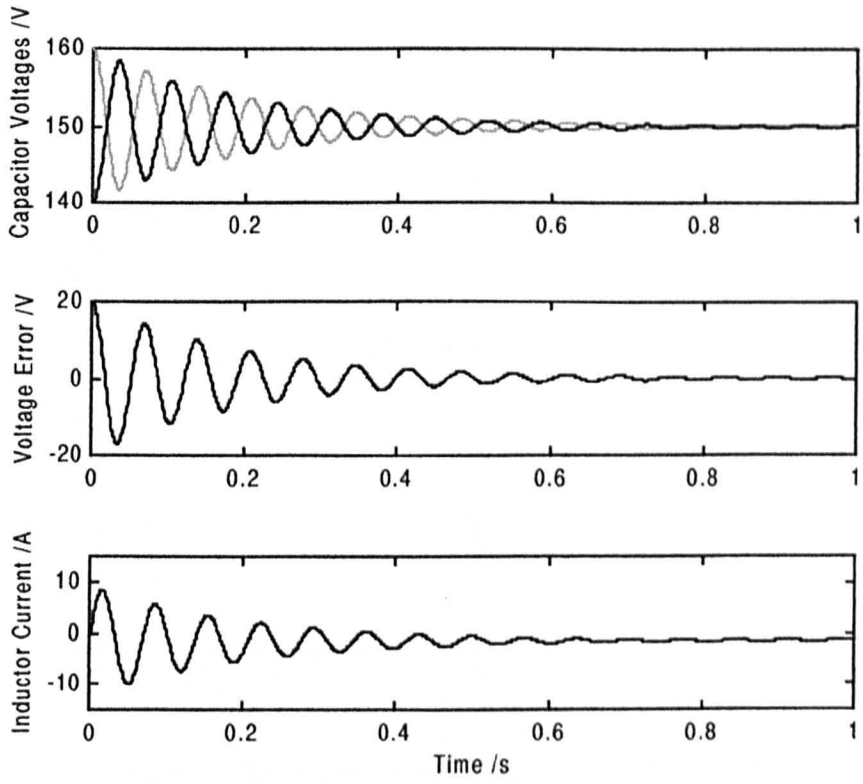

Figure 5.25 : *Open loop balancer response simulation*

In order to improve the response, a closed loop control system has to be used. The usual starting point would be to add a PI controller, and feedback the voltage error. Figure 5.26 shows the root locus with a PI controller added.

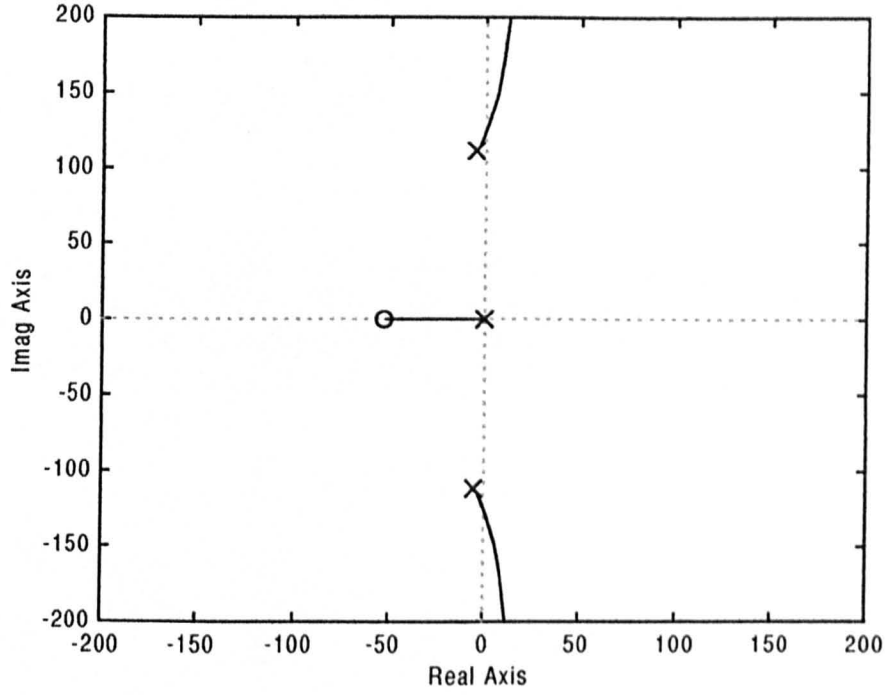

Figure 5.26 : *Control root locus with a simple PI control*

As the figure shows, the system quickly becomes unstable with the PI added. With complex plant poles it is not possible to achieve the bandwidth required. The operation needs to be changed so that the plant is not complex. This can be achieved by having a nested control system, separating the current control in the inductor from the voltage control on the capacitors. The new control structure is shown in figure 5.27.

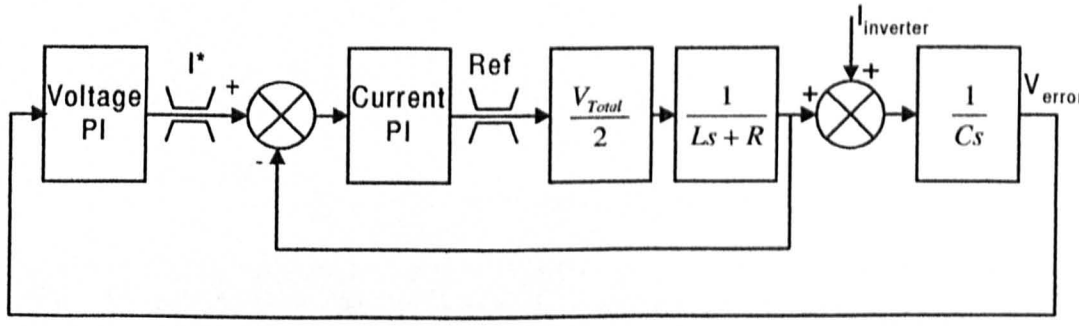

Figure 5.27 : *Nested control arrangement*

The natural feedback from the voltage error into the current loop has been ignored. Under normal operating conditions this will be negligible (i.e. the system will be balanced). With nested control, it is normal to have the inner loop operating with a significantly higher bandwidth than the outer loop.

The control design was completed giving a current loop of:

$$\omega_0 \approx 200Hz$$
$$\zeta = 0.707 \qquad [5.22]$$

This is the control bandwidth, and is beyond the circuit limitation defined given in 5.19. The closed loop control defines the small signal limit rather than the large signal behaviour defined earlier.

The voltage loop was then designed with:

$$\omega_0 \approx 50Hz$$
$$\zeta = 0.707 \qquad [5.23]$$

Whilst the inverter is running, the system will have to withstand the disturbance current drawn from the node. This is not constant, but contains many high frequency components. The disturbance rejection was examined in simulation to test the control design. Figure 5.28 shows the simulated response to a step disturbance in the current drawn from the node.

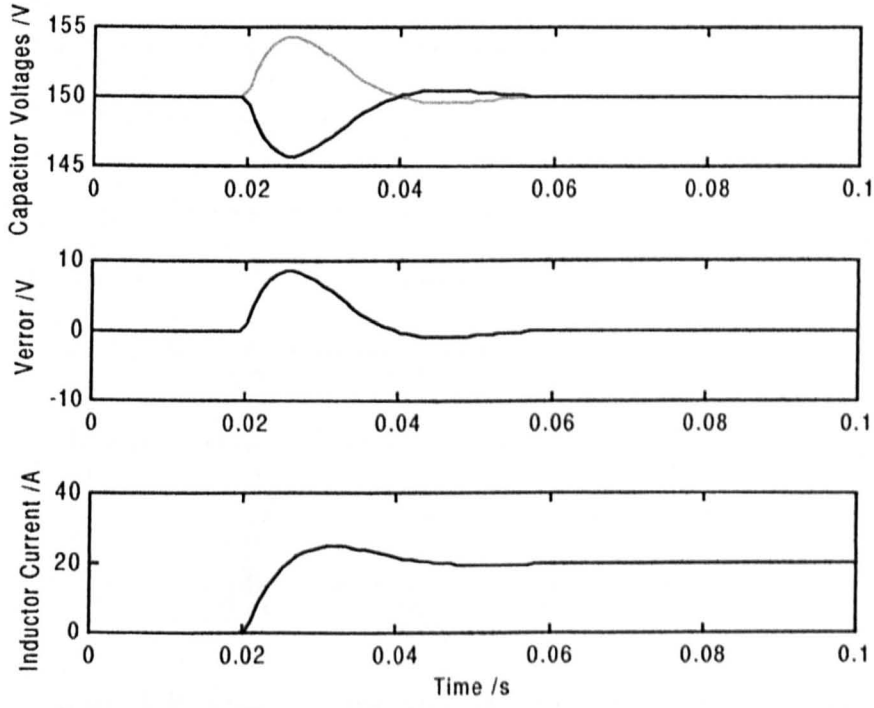

Figure 5.28 : *Simulated disturbance response*

The disturbance response is defined by the slower voltage loop. This results in quite a large variation in the capacitor voltages. The current transducers that are present on the inverter for protection purposes also provide a direct measurement of the current drawn from the node. This measurement can be fed into the control strategy as a demand on the current loop. The current drawn by the inverter can now be tracked by the high bandwidth inner loop, with the outer loop tuning the capacitor voltages. The modified control arrangement is shown in figure 5.29. A repeat of the previous simulation is shown in figure 5.30 with the current feed forward added.

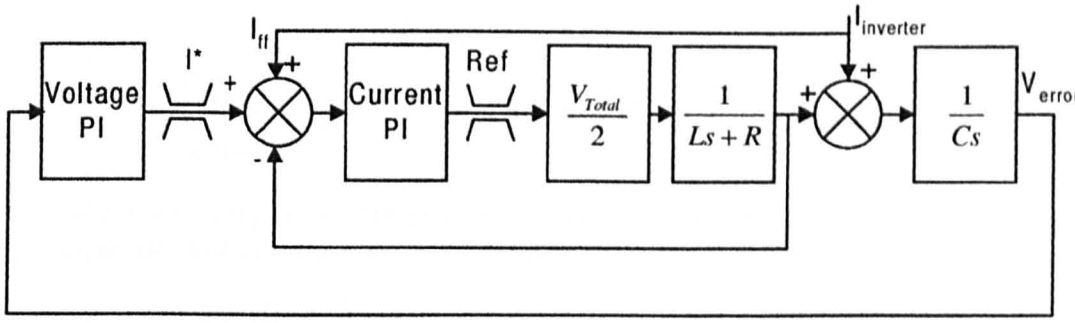

Figure 5.29 : *Control arrangement with current feed forward*

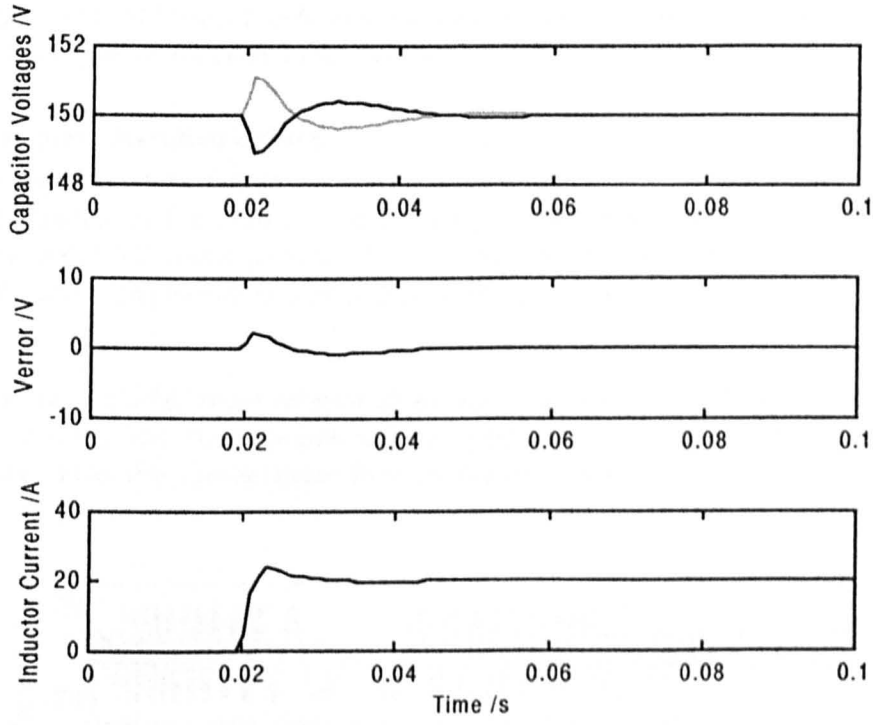

Figure 5.30 : *Simulated disturbance response with current feed forward*

The figure clearly shows the improvement that the current feed forward has produced. The voltage fluctuation is reduced by a factor of four. This is the control arrangement that is implemented in the balancer construction.

5.4.5 Implementation of balancer circuit

The microcontroller did not have sufficient pattern generation lines remaining to implement the PWM for the balancers. The control is also fairly complex, needing several analogue measurements. It was therefore decided to implement both the control and switching generation using a discrete analogue/digital system. This will be described later in appendix 1.

In the analysis of the inverter, equation 4.13 modelled the mean current drawn at the upper balancing node by each phase. The total current for the inverter is thus given by:

$$\overline{I_2} = \begin{cases} \dfrac{3A\hat{I}\cos(\phi)}{2} & 0 \le A \le 0.5 \\ \dfrac{3\hat{I}\cos(\phi)}{2A\pi}\left[\sqrt{4A^2-1}+4A^2\sin^{-1}\left(\dfrac{1}{2A}\right)-A^2\pi\right] & 0.5 \le A \le 1 \end{cases} \quad [5.24]$$

From the graph in figure 4.4, the peak current occurs as the outer carriers come into use at half amplitude. The maximum mean current is simply found by substitution.

$$\overline{I_{2\,Max}} = \frac{3\hat{I}\cos(\phi)}{4} \quad [5.25]$$

The maximum mean current that the balancer will have to supply to the node is three quarters of the peak real AC current. Allowing for current ripple on top of this value, the balancer current rating was set the same as the inverter.

5.4.6 Balancer Operation Results

The development of the balancer was concurrent with the basic vector control that has been described earlier in the chapter. The results presented below were taken with the drive operating under full vector control. This provides the best test conditions for the balancer, with full current load transients used to disturb the capacitor voltage balance.

Test 1:

The first test was a full speed reversal of the machine. Figure 5.31 shows the motor current, balancer current, and the capacitor voltage error. These are all recorded by independent transducers rather than taking signals from the control boards.

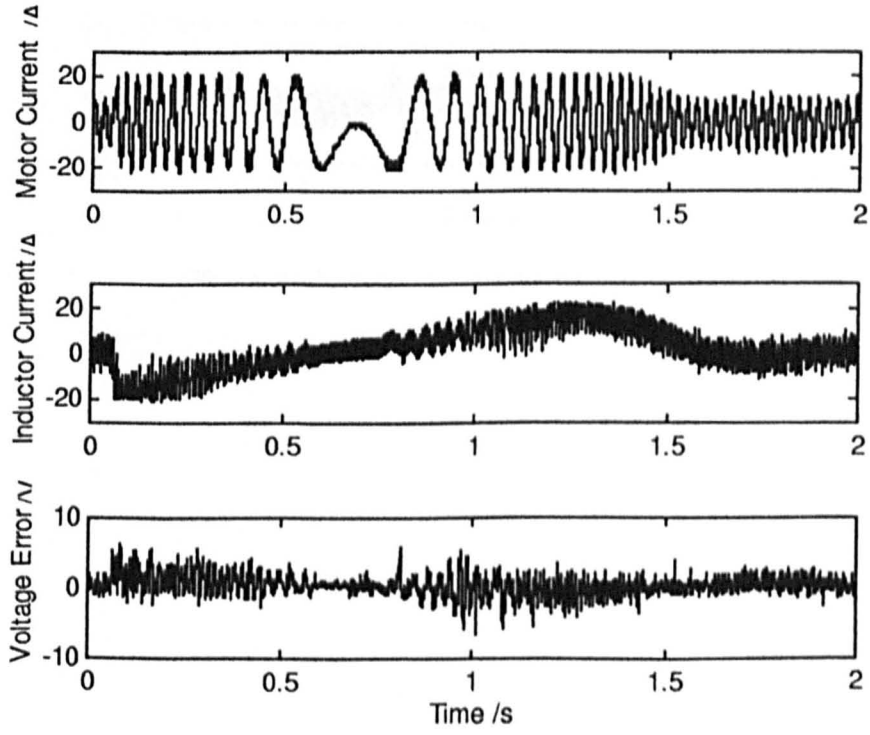

Figure 5.31 : *Balancer Test 1 – Speed Reversal*

From steady state operation with a small mean balancer current, the step speed demand causes full power regeneration. The balancer quickly absorbs this current with minimal disturbance on the capacitor voltages. The system then tracks the node current through the deceleration, and acceleration, with a reversal in the current direction, maintaining the capacitor voltages at all times.

Test 2:

The second test was to evaluate the transient response. Starting from zero speed, full torque was applied to the machine. Once the balancer current was up to rated operating conditions the torque was reversed, and the machine decelerates back to zero speed. This inserts a full current reversal into the DC link node. Figure 5.32 shows the full test result, with figure 5.33 showing a close-up of the actual current transient that occurred at torque reversal.

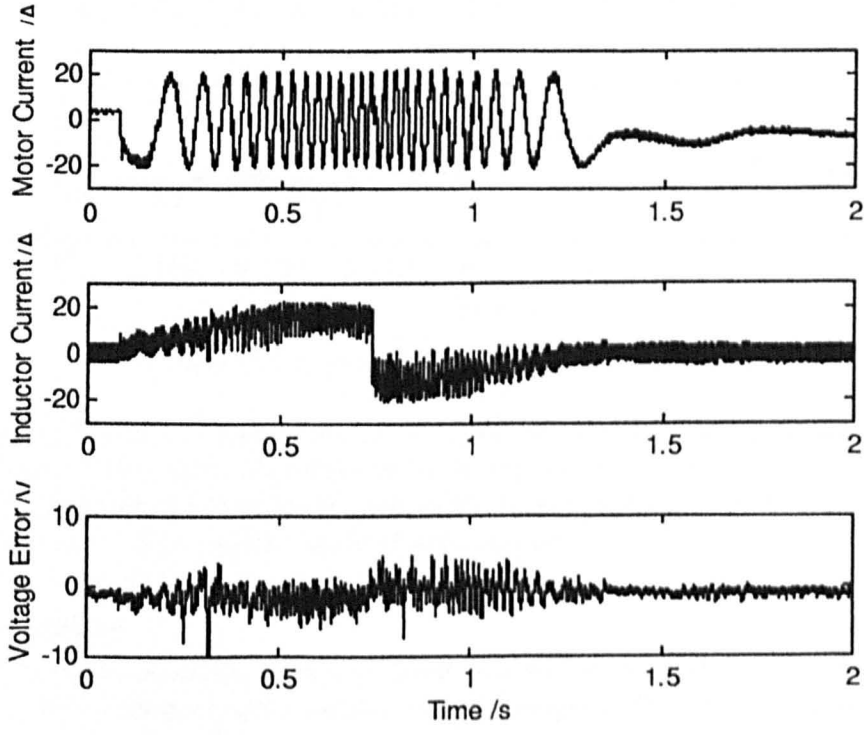

***Figure 5.32** : Balancer test 2 – Current reversal*

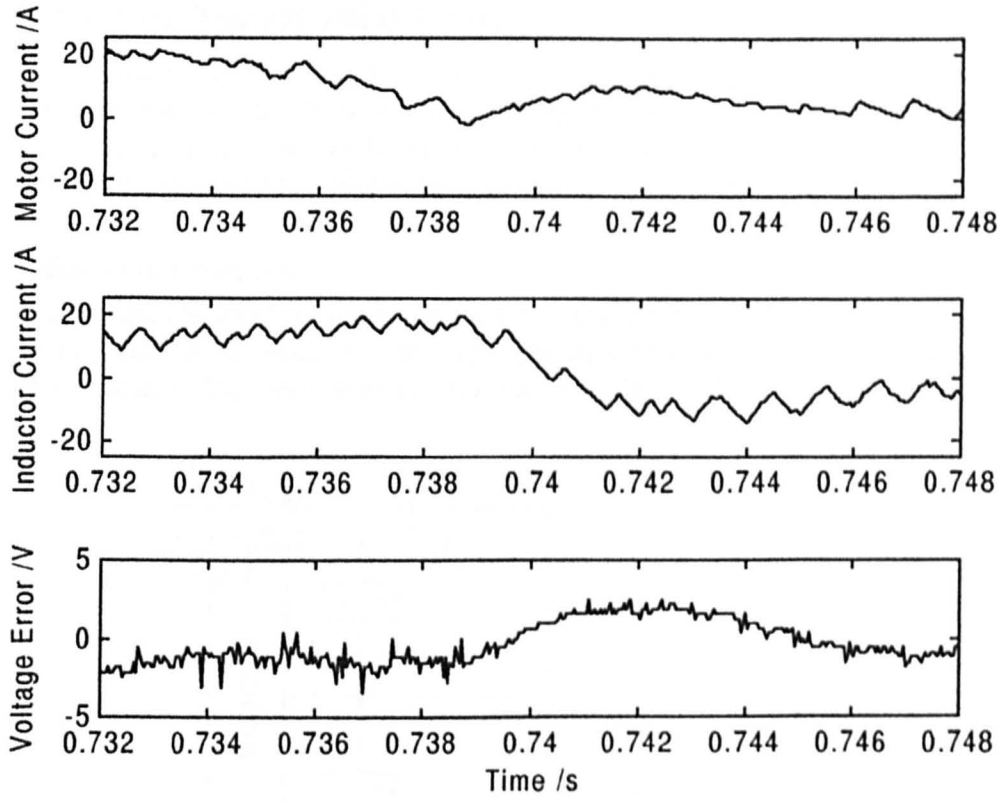

Figure 5.33 : *Inductor current response from test 2*

The balancer has clearly maintained the capacitor voltages successfully. Examination of the step response in the current control shows a time to peak of ~3.7 ms. This corresponds well to the theoretical value of 3.5 ms based on the control parameters from equation 5.22. See figure A2.4 in appendix 2 for a similar simulated step response.

5.4.7 Conclusions

A novel balancer circuit has been introduced, and the operation described. Control for the circuit has been examined and a suitable strategy designed. The balancers were constructed and put into operation on the five level prototype inverter.

Results have been presented showing the balancers in operation, and the capability to regulate the voltage throughout the operating range (in all four quadrants) has been demonstrated. Voltage regulation is maintained to within ±3%.

5.5 Advanced Neutral Point Control

The technique proposed for neutral point control in the three level inverter is equally valid in the five level inverter. The effect of adding the offset is more complicated to analyse, but it does result in a change in the neutral point current. An effect is also observed in the currents at the balancer nodes, which indirectly impacts on the neutral point.

5.5.1 Analysis of Operation

The steady state condition for the balancers from equation 5.20 is a reference of zero. This equates to equal time in states one and three. The state times also dictate the current drawn from the capacitors. The mean current flow is shown in figure 5.34.

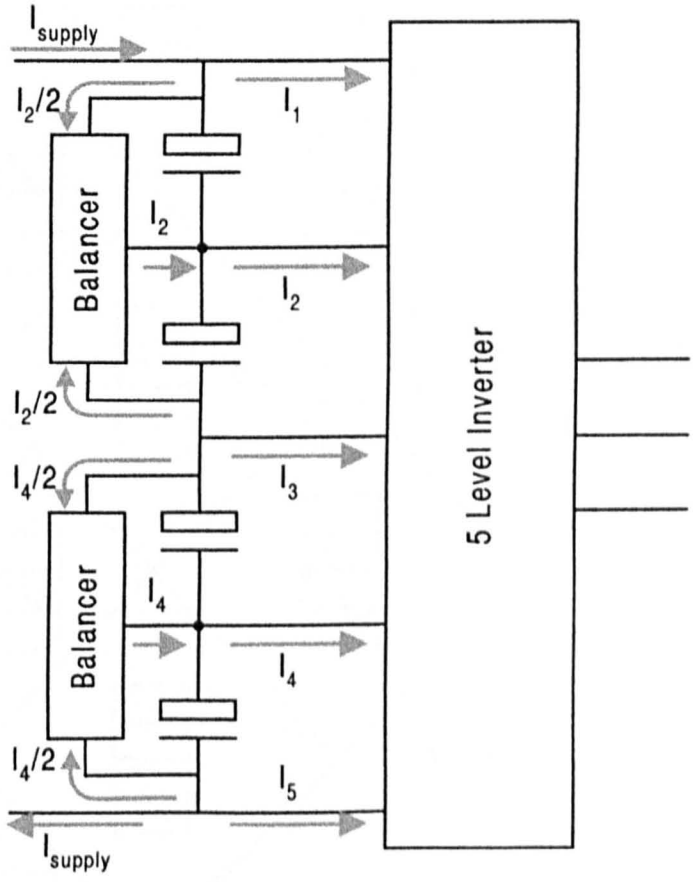

Figure 5.34 : *Node currents with balancers*

The effective neutral point current (including the influence of the balancers) is given by:

$$I_{neutral} = I_3 + \frac{I_2}{2} + \frac{I_4}{2} \qquad [5.26]$$

The analysis of the node currents for the normal operation strategy produced two expressions for each current depending on the modulation amplitude. With the offset applied, there are more boundary conditions, and more solutions for the currents. These solutions are mapped out in figure 5.35.

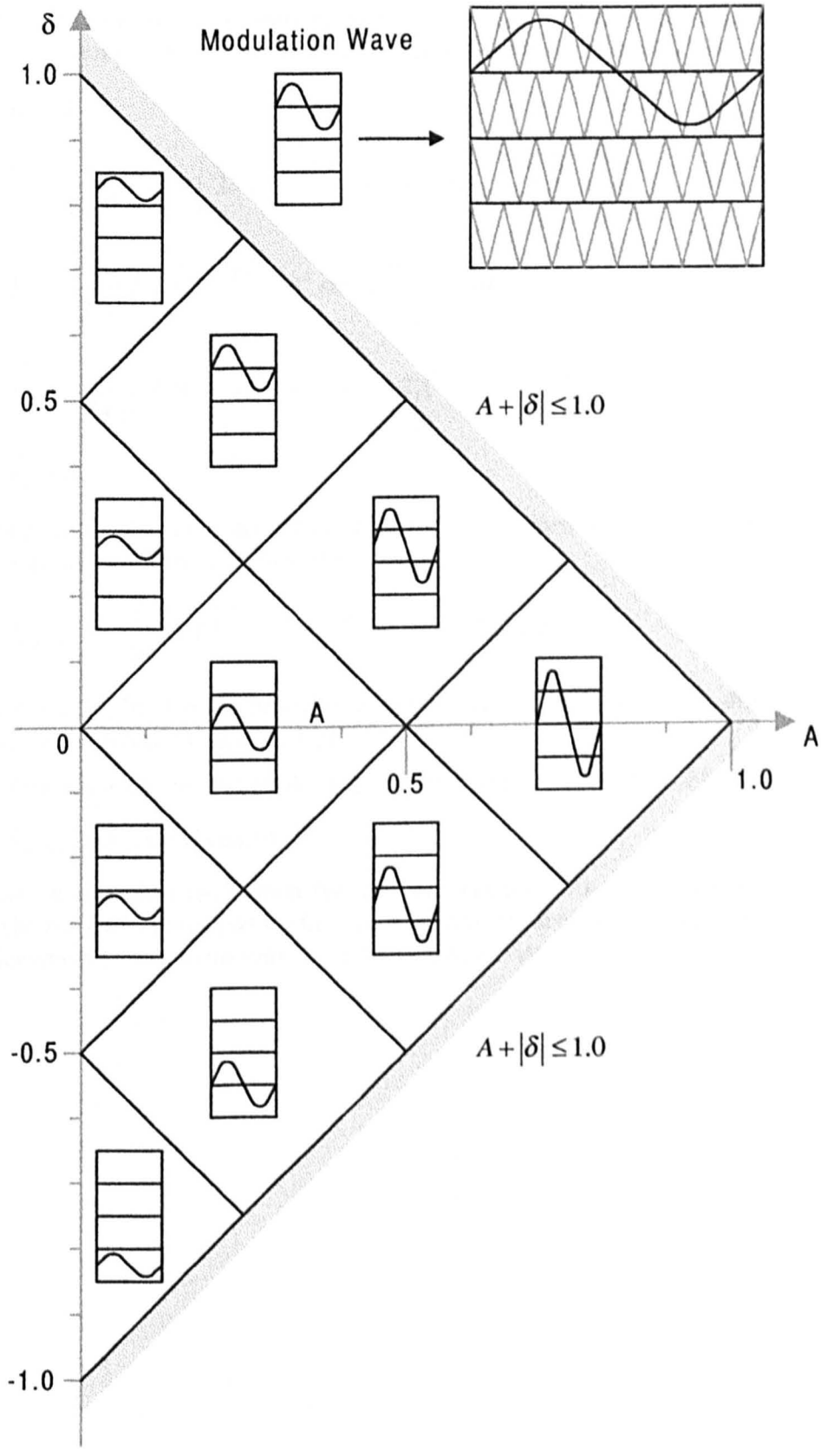

Figure 5.35 : *Modulation conditions with offset added*

There are ten different modulation conditions, each producing different equations for the five node currents. In some zones the currents can be calculated simply, an others the equations

become more complicated. Examining zone A for example, a simple set of equations can be derived for the node currents by the same technique used in previous chapters.

$$\overline{I_1} = 0 \qquad [5.27]$$

$$\overline{I_2} = \frac{1}{2\pi A}\left[A^2\pi + \left(2\delta\sqrt{A^2-\delta^2} + 2A^2\sin^{-1}\left(\frac{\delta}{A}\right)\right)\right]\hat{I}\cos(\phi) \qquad [5.28]$$

$$\overline{I_3} = -\frac{2}{\pi A}\left[\delta\sqrt{A^2-\delta^2} + A^2\sin^{-1}\left(\frac{\delta}{A}\right)\right]\hat{I}\cos(\phi) \qquad [5.29]$$

$$\overline{I_4} = -\frac{1}{2\pi A}\left[A^2\pi - \left(2\delta\sqrt{A^2-\delta^2} + 2A^2\sin^{-1}\left(\frac{\delta}{A}\right)\right)\right]\hat{I}\cos(\phi) \qquad [5.30]$$

$$\overline{I_5} = 0 \qquad [5.31]$$

Applying these solutions to the effective neutral point current defined in equation 5.26, the following result is obtained for this zone.

$$I_{neutral} = -\frac{1}{\pi A}\left[\delta\sqrt{A^2-\delta^2} + A^2\sin^{-1}\left(\frac{\delta}{A}\right)\right]\hat{I}\cos(\phi) \qquad [5.32]$$

This solution for the effective neutral point current for zone A is identical to that obtained for the three level inverter in equation 3.27.

The general equation over the whole range can be expressed in the form of equation 5.33.

$$I_{neutral} = K(A,\delta)\hat{I}\cos(\phi) \qquad [5.33]$$

Assuming a sinusoidal modulation function, the function K is shown graphically in figure 5.36. The surface has been formed from an numerical result obtained through a mathematical step simulation as used in the three level derivation (see appendix 2).

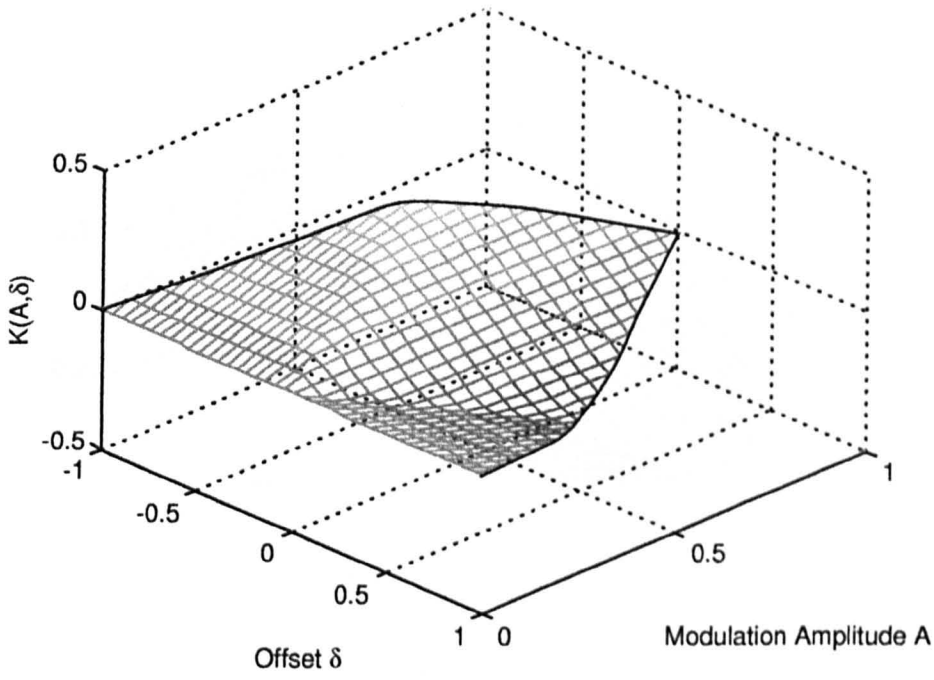

Figure 5.36 : *Surface Plot of function K(A,δ)*

The system described above, and used to calculate the surface plot, has the same limitations described for the three level inverter. The limited addition of an offset within the modulation bounds prevents operation at full modulation. This can be solved by applying the same clamping and compensation technique described in chapter three. The resulting surface plot is shown in figure 5.37.

The surface is also similar in form to that obtained for the three level inverter when the clamping technique was applied. Whilst the entire surface is technically valid, stability limitations exist at high modulation amplitudes. Figure 5.38 shows the operating curve for the full modulation condition. Within the safe operating region (avoiding control instability) an offset of up to ±0.5 can be inserted producing values for K of ±11%. For the three phase case this means that one third of the real current can be utilised to balance the neutral point.

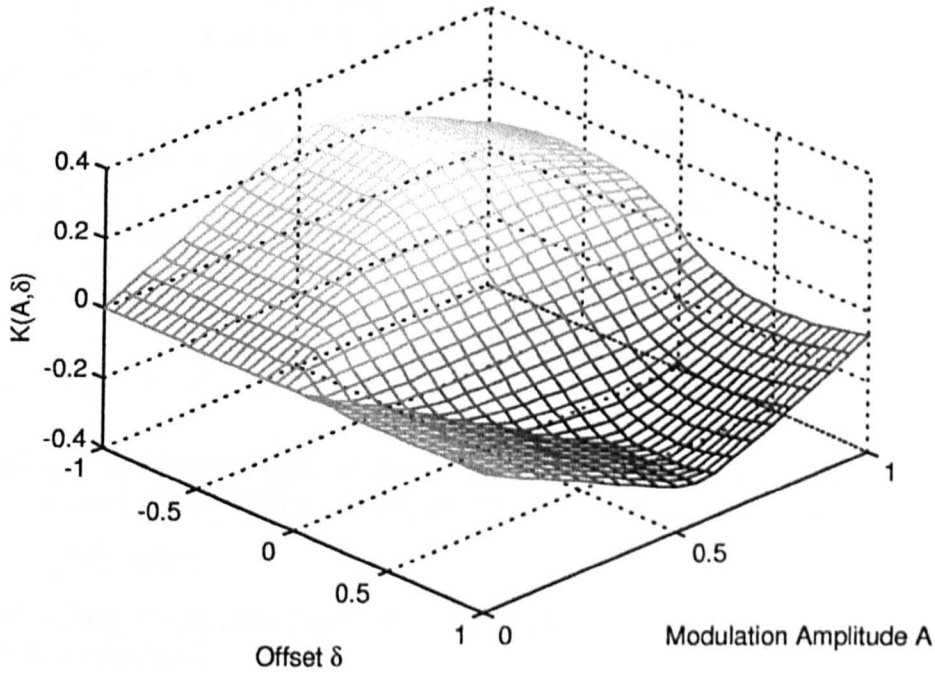

Figure 5.37 : *Surface plot with range extension applied*

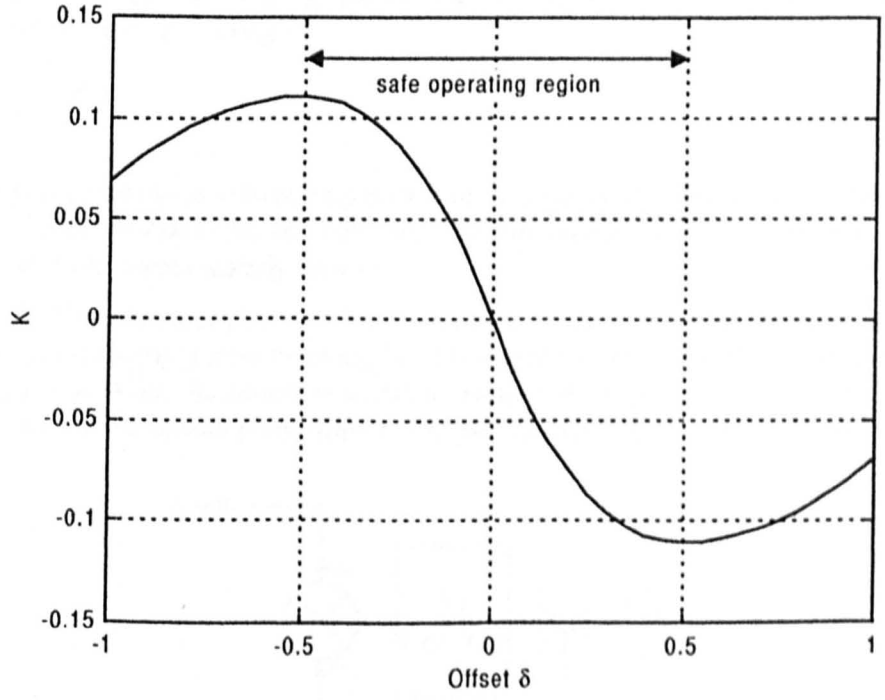

Figure 5.38 : *Operating curve for offset addition at full modulation (A=1)*

5.5.2 Current Compensation

For the three level inverter, it was assumed that the drive would be operated only in motoring mode. The design of the neutral point controller was then based around a fixed operating

range. As has been described in the previous section, the five level inverter is operating under vector control, and capable of full torque both in motoring and regeneration. Compensation of the motor current is therefore required in order for the control to maintain the capacitor voltages in all conditions.

From the earlier analysis it has been shown that the neutral point current is dependent on the amplitude, and relative phase angle of the motor current. There are several ways that the necessary values can be obtained within the software, but the technique employed is based around the power flow.

In the d-q rotating frame of reference the power flow can be calculated by the following equation.

$$P_{dq} = v_d i_d + v_q i_q \qquad [5.34]$$

It should be noted that the units of this equation are not watts. Assuming that the motor current is sinusoidal, then basic AC theory provides us with the following equation.

$$P = 3VI\cos(\phi) \qquad [5.35]$$

Simple algebraic manipulation therefore gives an equation for the load current component of the neutral point current.

$$\hat{I}\cos(\phi) = k\frac{v_d i_d + v_q i_q}{\sqrt{v_d{}^2 + v_q{}^2}} \quad \text{where k = constant} \qquad [5.36]$$

The constant k can be found by calculating back through the equations that relate the d-q variables with the real voltages.

$$k = \frac{\sqrt{2}}{3} \qquad [5.37]$$

Since the calculation of voltage amplitude and the associated square root already exists as part of the PWM structure, the equation becomes reasonably simple to implement within the vector control routines already present.

Figure 5.39 shows the controller with current compensation included. The gain compensation is shown as a simple inverse function, but this would encounter stability problems at very low current levels. When the current is within a low level dead band, the controller can have little or no effect on the neutral point current. The gain is therefore reduced for stability.

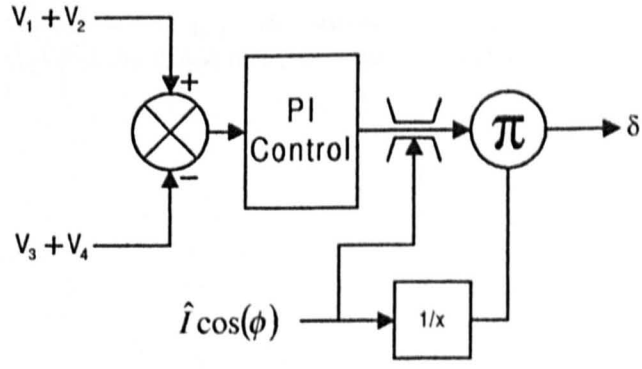

Figure 5.39 : *Controller with current compensation*

5.5.3 Results

TEST 1:

The first test is steady state operation. Figure 5.40 shows operation at 50Hz no load. This represents one of the most difficult operating conditions, since the real current component is small (most of the current is the reactive magnetising component) and the modulation index A is at maximum.

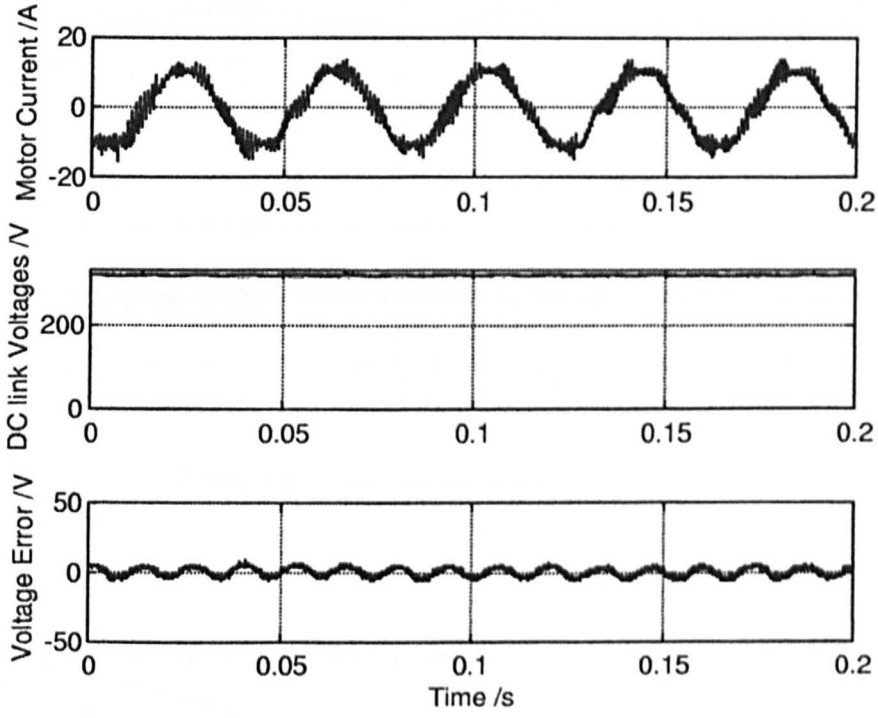

Figure 5.40 : *Steady State Operation with 580V total DC link*

TEST 2:

The second test is a speed reversal. This demonstrates the operation of the control in four quadrants, which requires accurate current compensation to correctly adjust the gain for regeneration. Figure 5.41 shows measurements taken from a ±1500rpm speed reversal under vector control. The periods of motoring and regeneration are clearly visible from the DC link voltage. The link voltage is limited by the braking chopper circuit. The regulation on the capacitor voltages is clear.

Figure 5.42 shows a data recording on the processor during a separate speed reversal. This shows the motor speed, the estimated real motor current, and the measured voltage error at the neutral point

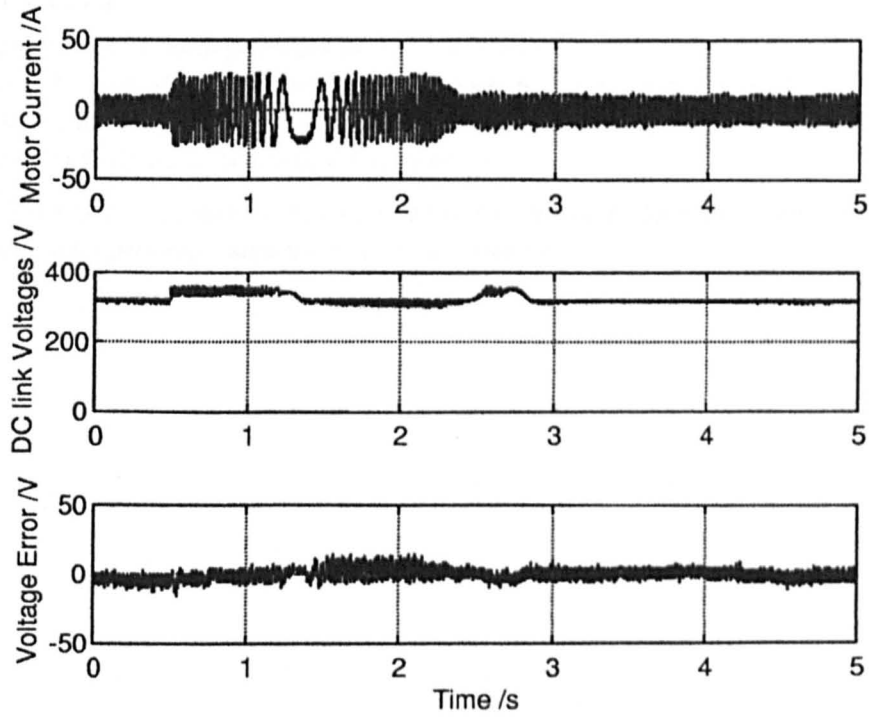

Figure 5.41 : *Operation through a speed reversal*

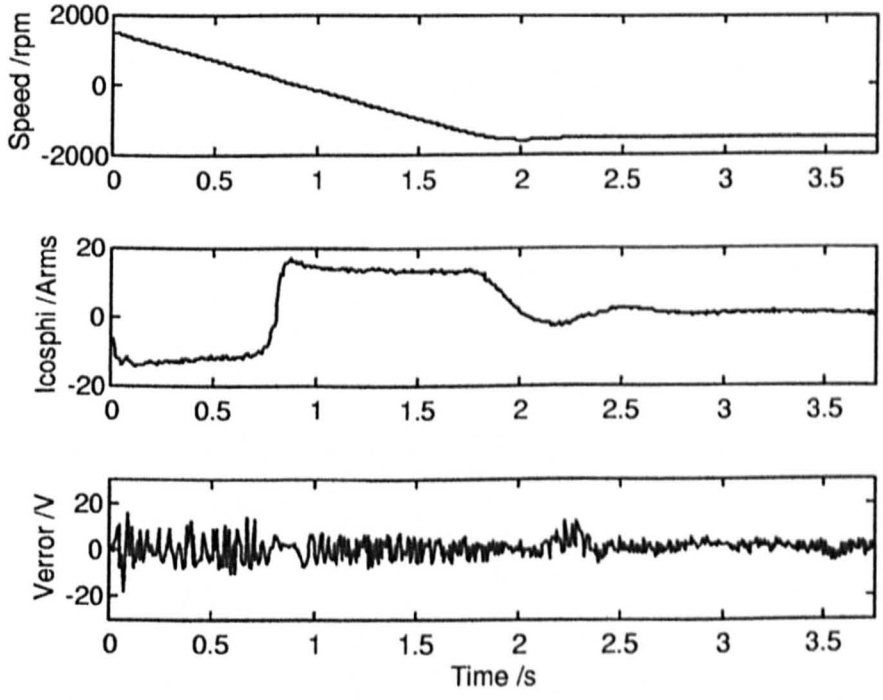

Figure 5.42 : *Speed reversal*

5.5.4 Conclusions

The application of neutral point control on a five level inverter with balancer circuits has been described. As with the three level the technique has been analysed and a control strategy produced. Current compensation has been included which has been derived from the mathematical analysis of the control technique.

Results have been included which clearly show the neutral point control operates successfully throughout the operating range and in all four quadrants.

5.6 Operating Results – Full System

5.6.1 Test Results

The following sections show results from the operation of the full five level inverter with vector control, balancers, and neutral point control. Harmonics are recorded via a spectrum analyser to achieve sufficient time averaging.

This section has been included to show the harmonic analysis when the full prototype inverter system is in operation at no load, which represents the worst case condition. The results are steady state plots of current and voltage, with the respective spectrum analysis.

The loaded capabilities of the prototype inverter have been fully demonstrated during vector controlled speed reversals.

5.6.2 10 Hz operating frequency

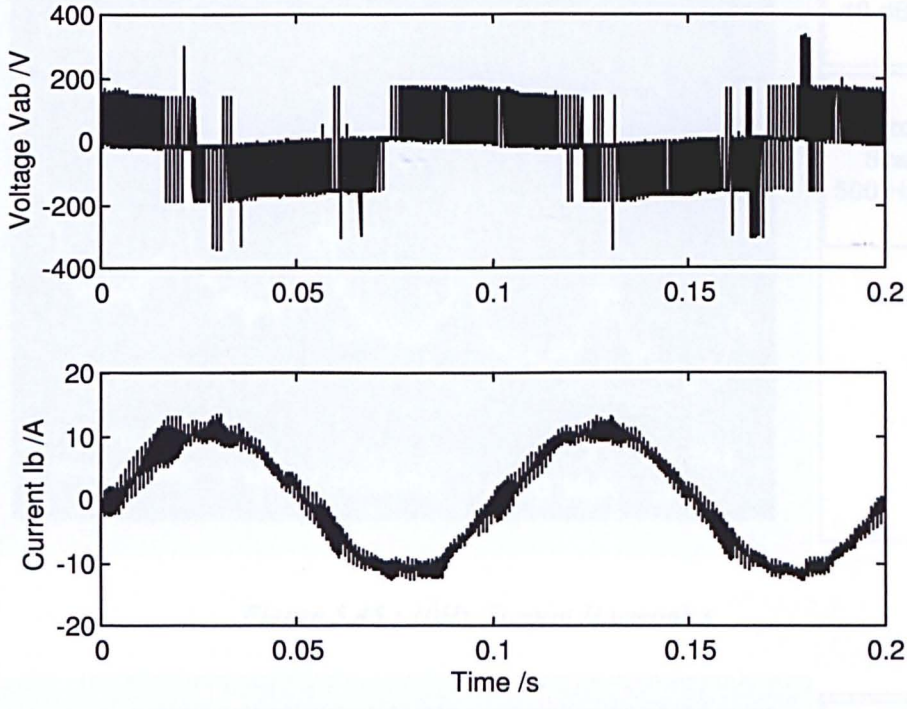

Figure 5.43 : *10 Hz Operating result*

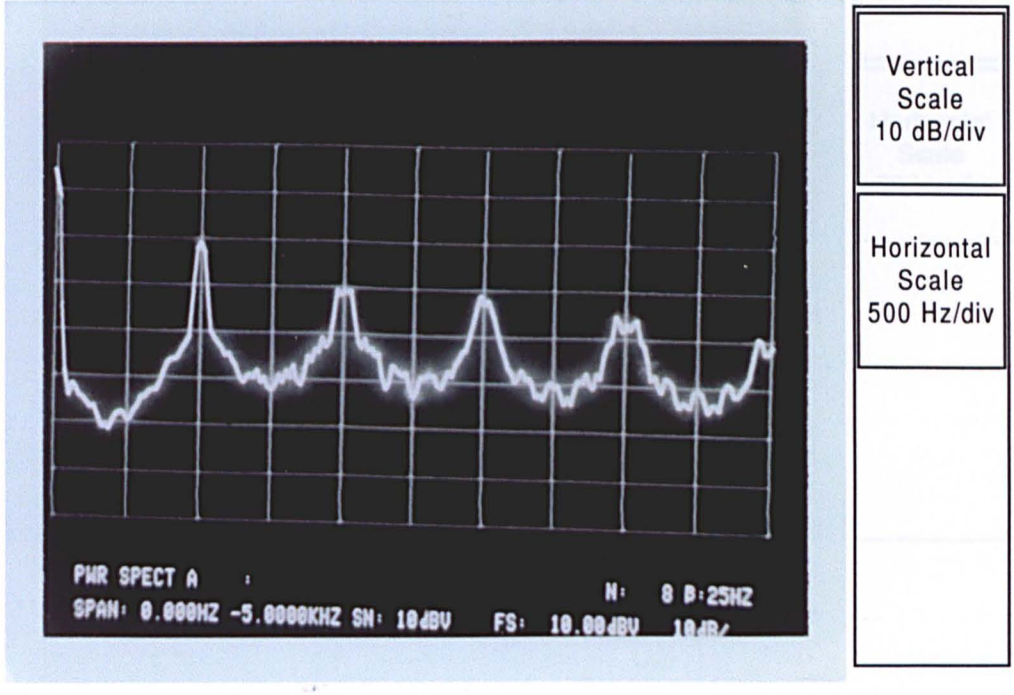

Figure 5.44 : *10Hz Voltage Harmonics*

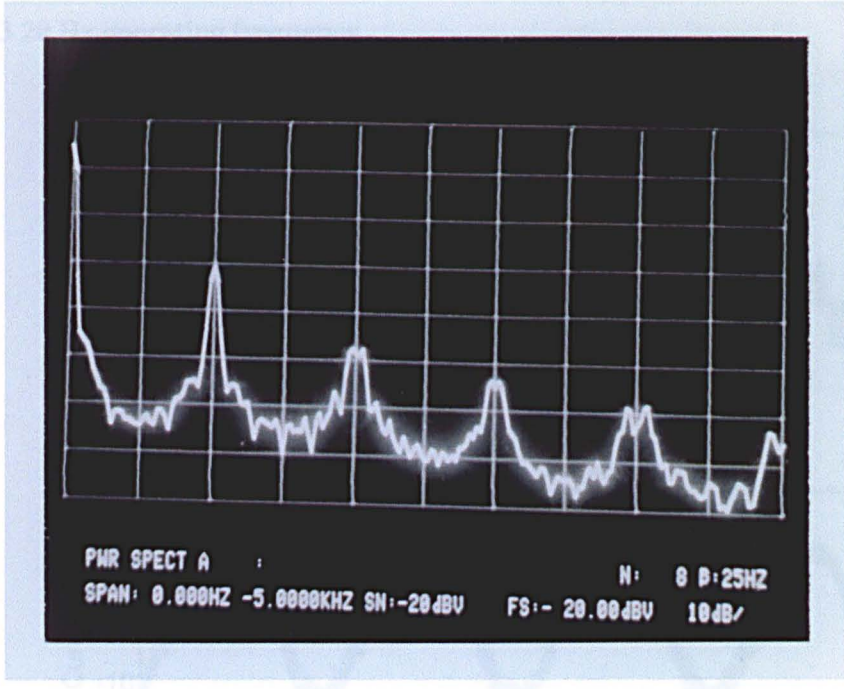

Figure 5.45 : *10Hz Current Harmonics*

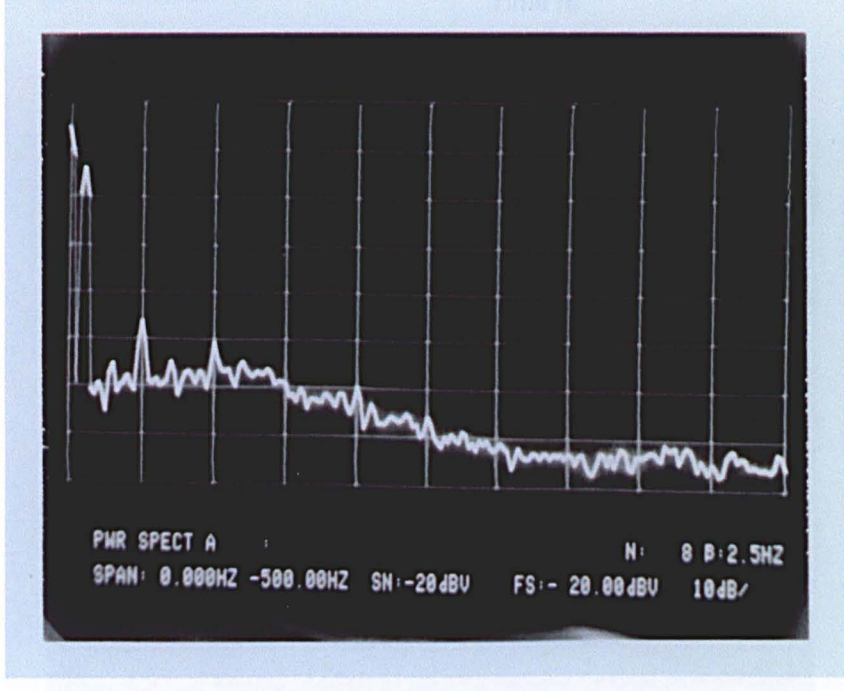

Figure 5.46 : *10Hz Low Order Current Harmonics*

5.6.3 20 Hz operating frequency

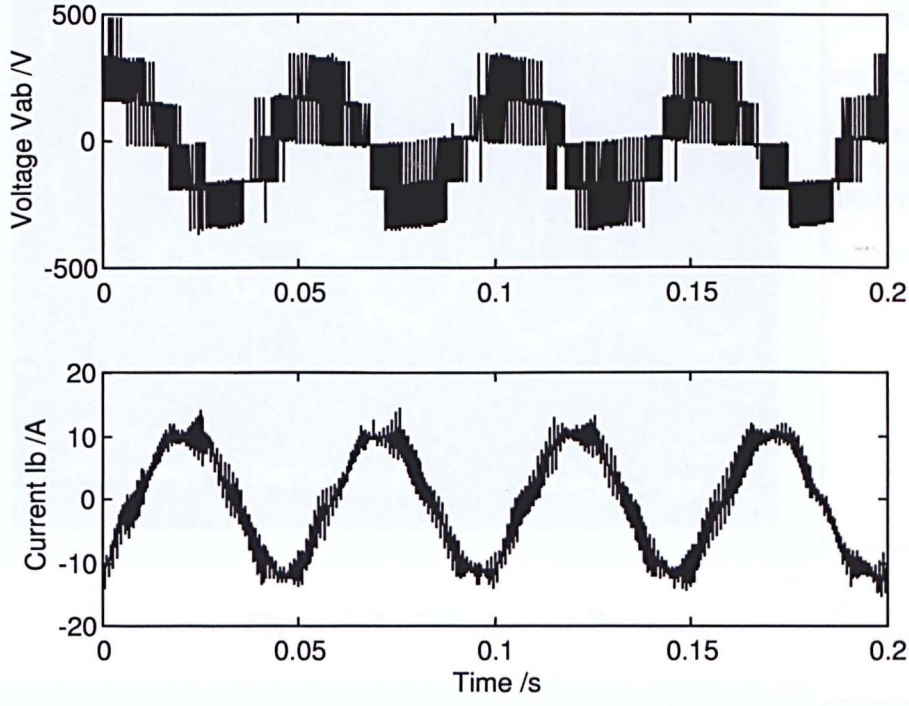

Figure 5.47 : *20Hz Operating Result*

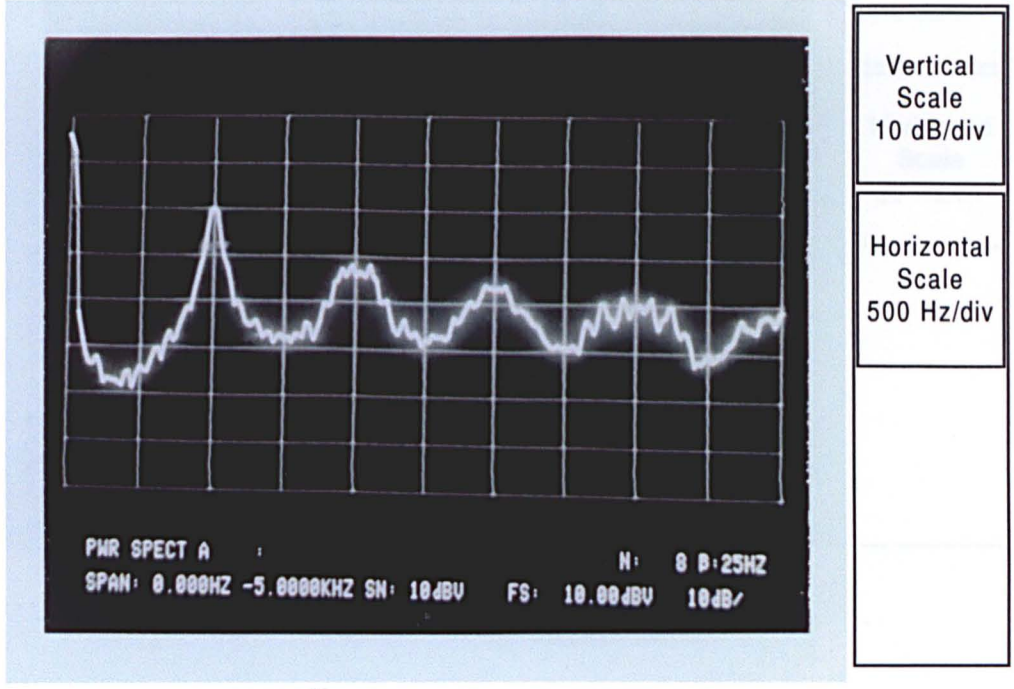

Figure 5.48 : *20Hz Voltage Harmonics*

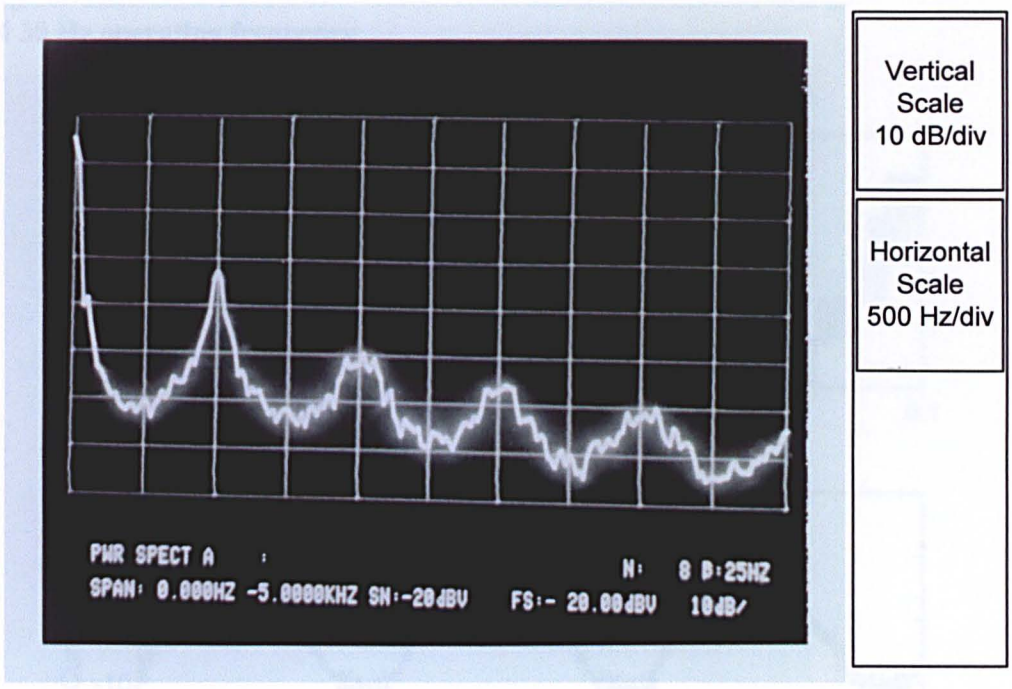

Figure 5.49 : *20Hz Current Harmonics*

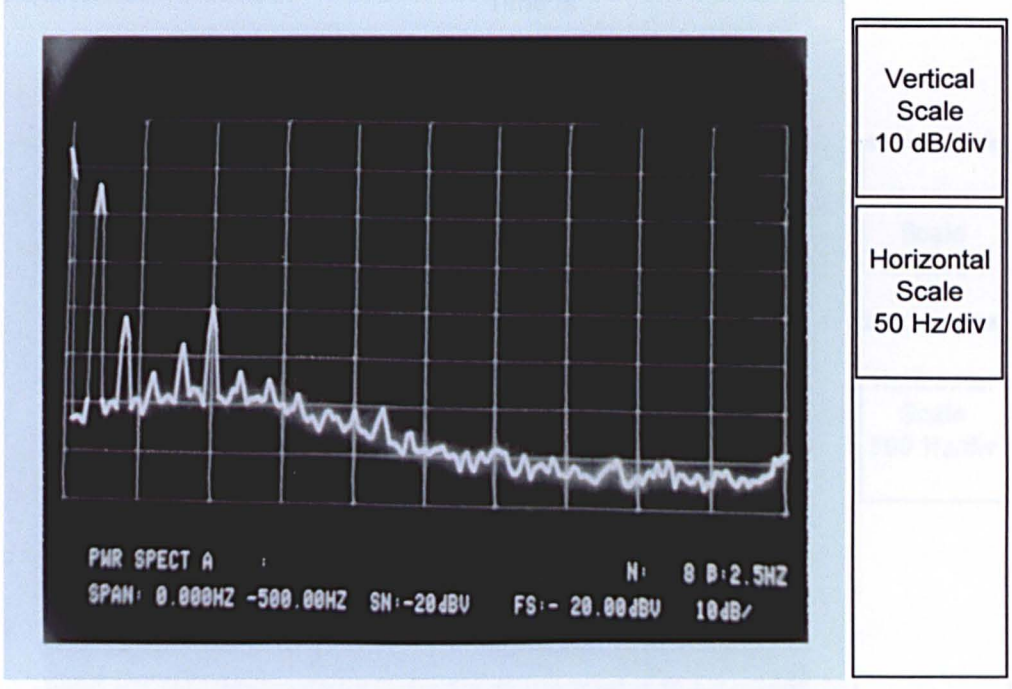

Figure 5.50 : *20Hz Low Order Current Harmonics*

5.6.4 30 Hz operating frequency

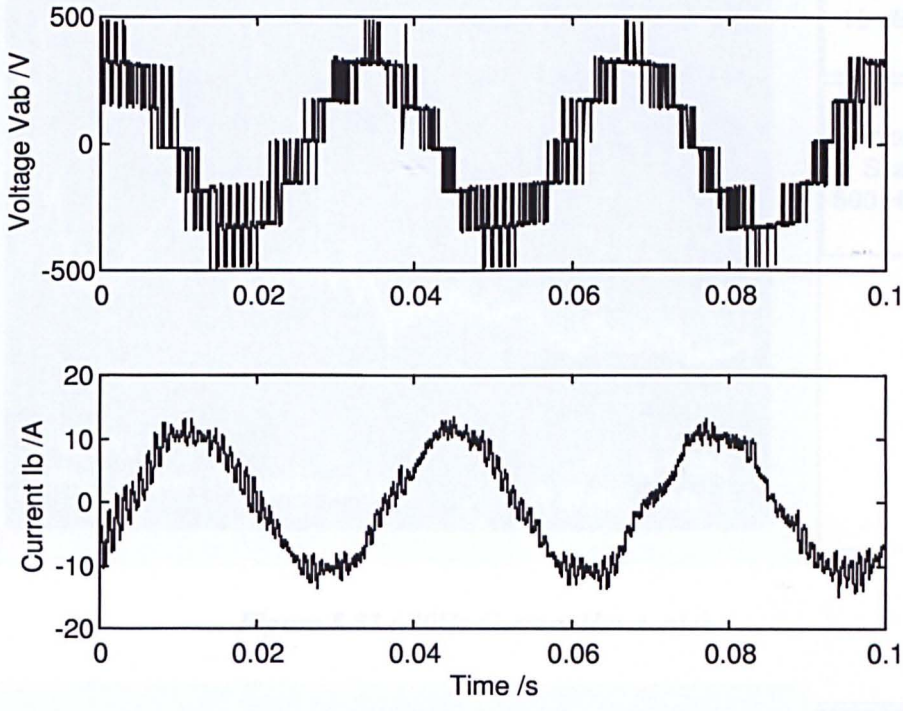

Figure 5.51 : *30Hz Operating Result*

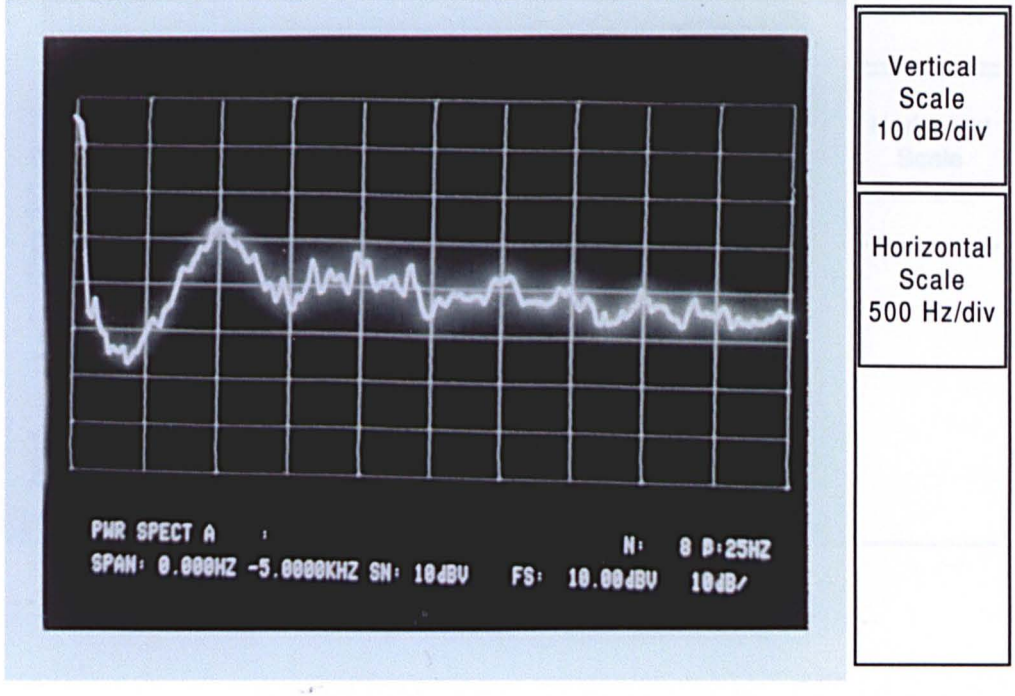

Figure 5.52 : *30Hz Voltage Harmonics*

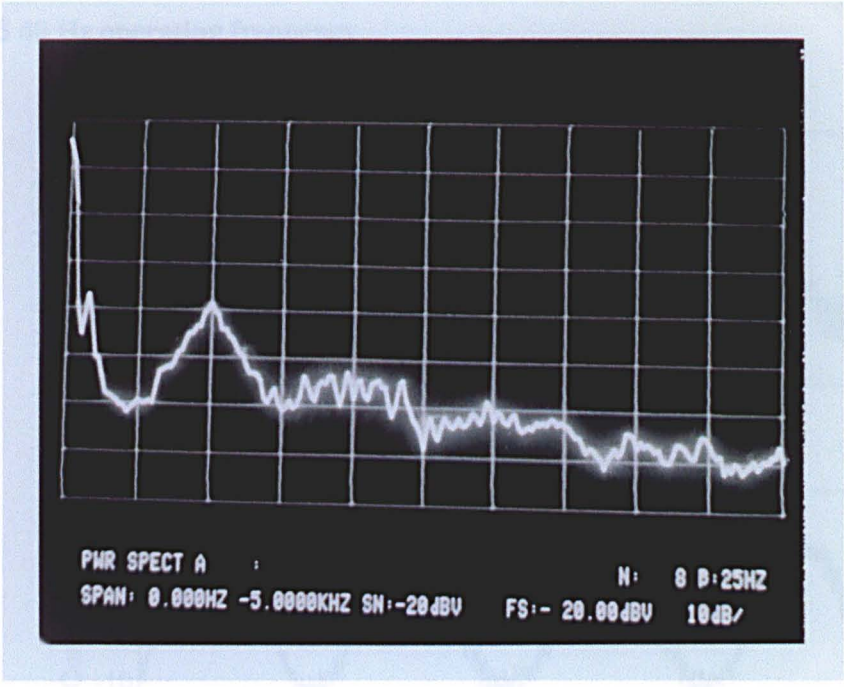

Figure 5.53 : *30Hz Current Harmonics*

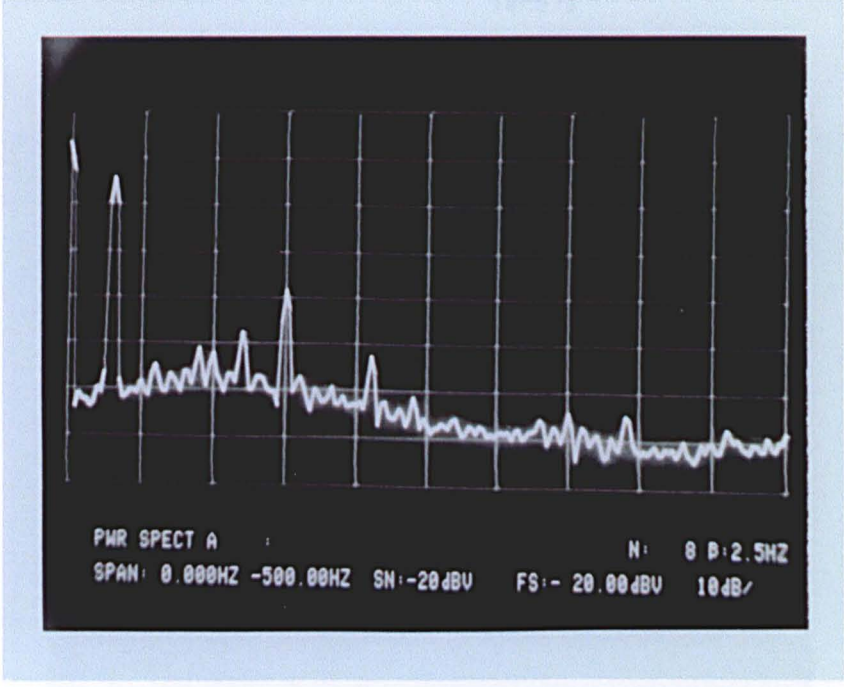

Figure 5.54 : *30Hz Low Order Current Harmonics*

5.6.5 40 Hz operating frequency

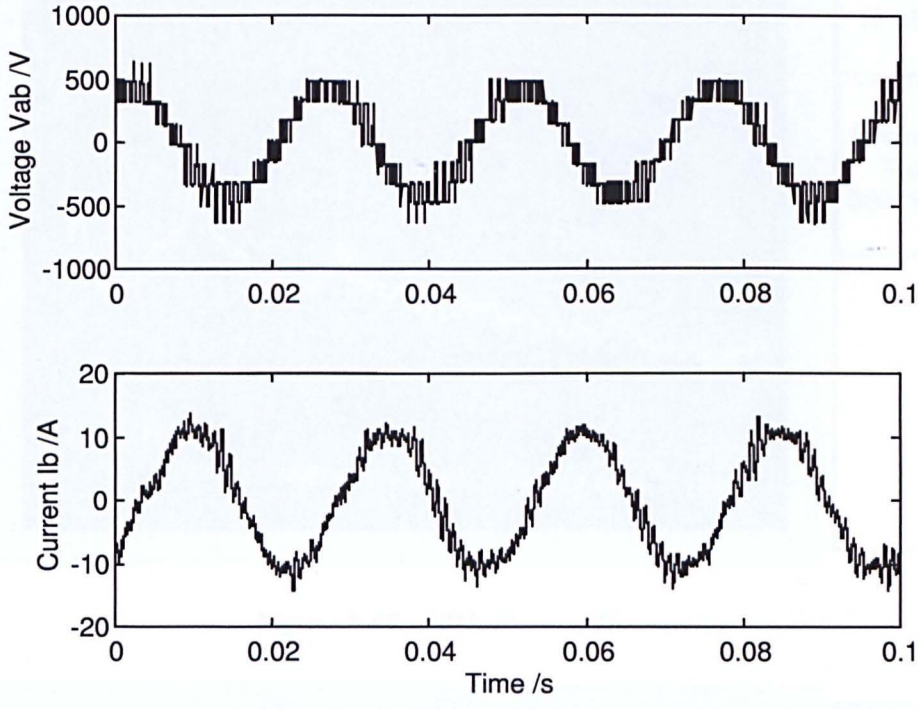

Figure 5.55 : *40Hz Operating result*

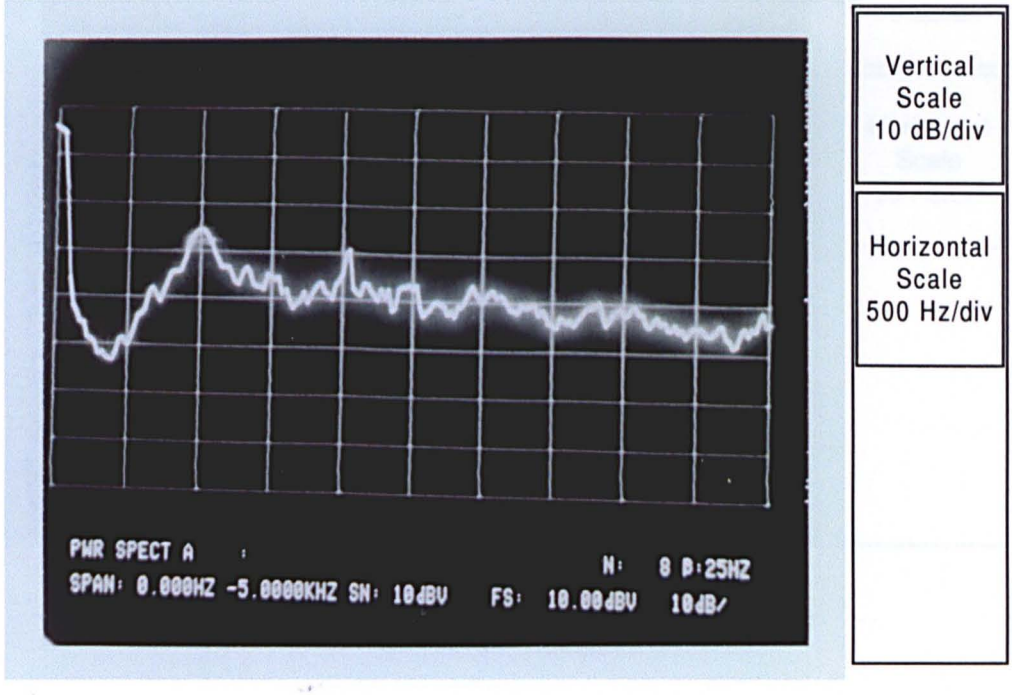

Figure 5.56 : *40Hz Voltage Harmonics*

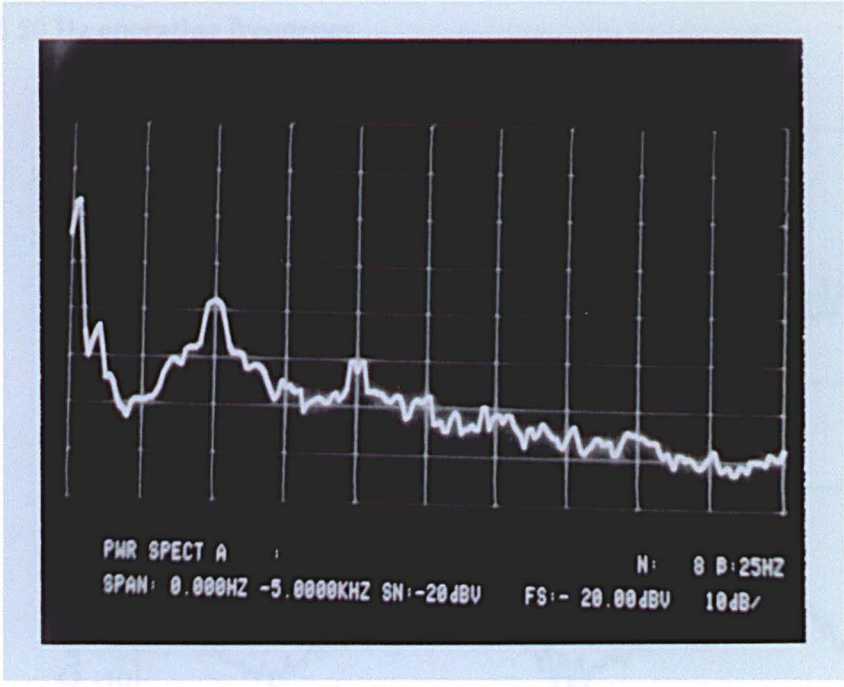

Figure 5.57 : *40Hz Current Harmonics*

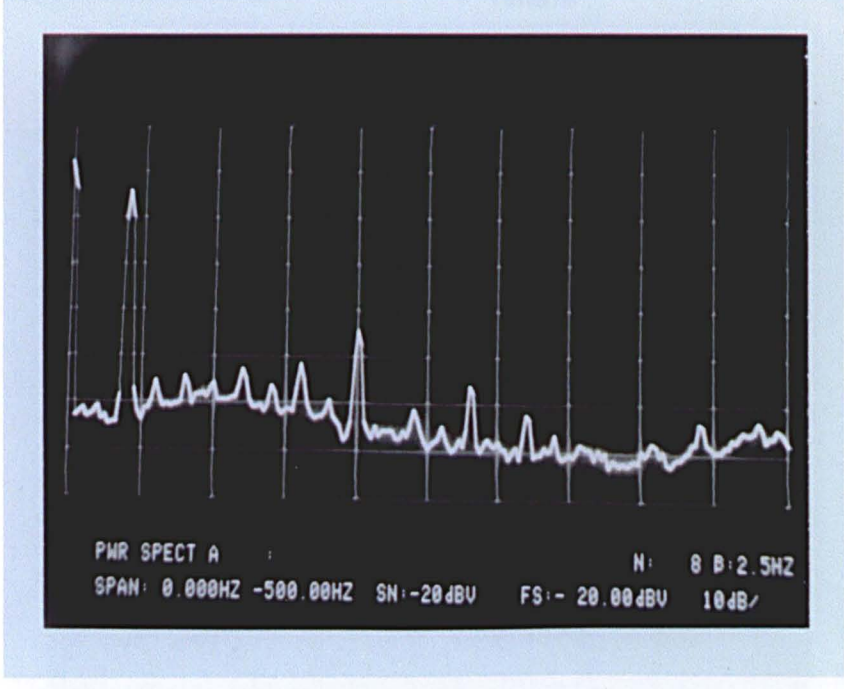

Figure 5.58 : *40Hz Low Order Current Harmonics*

5.6.6 50 Hz operating frequency

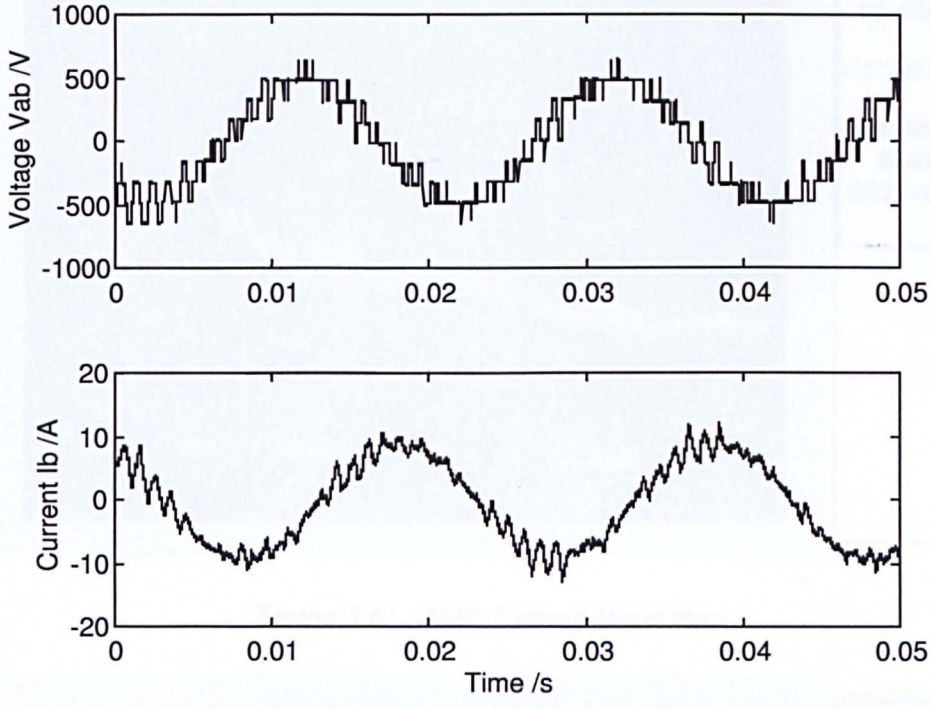

Figure 5.59 : *50 Hz Operating result*

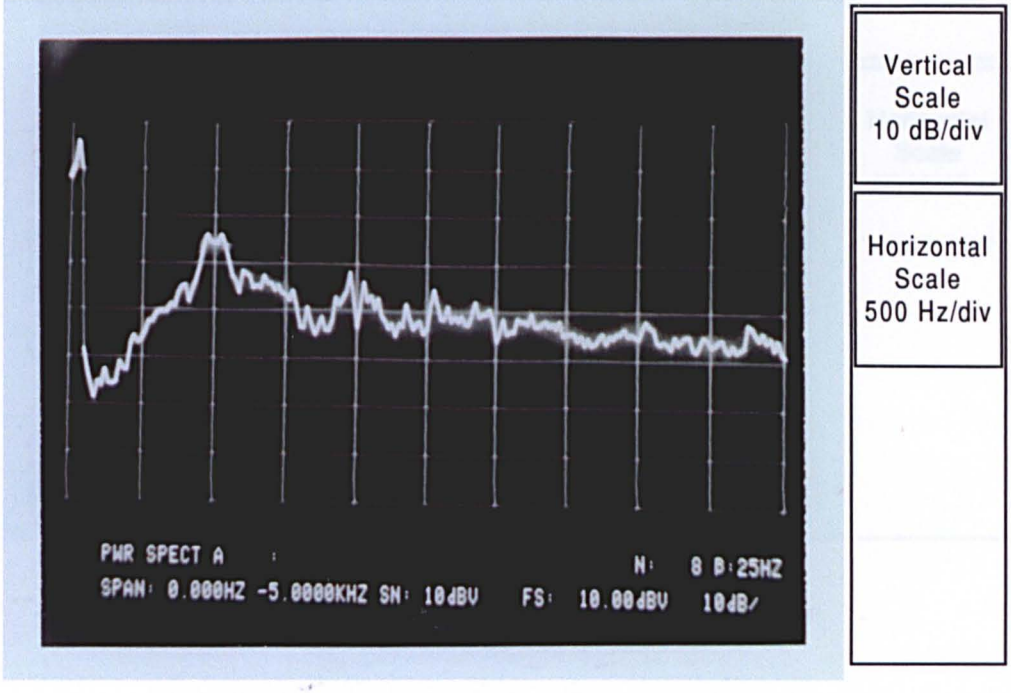

Figure 5.60 : *50Hz Voltage Harmonics*

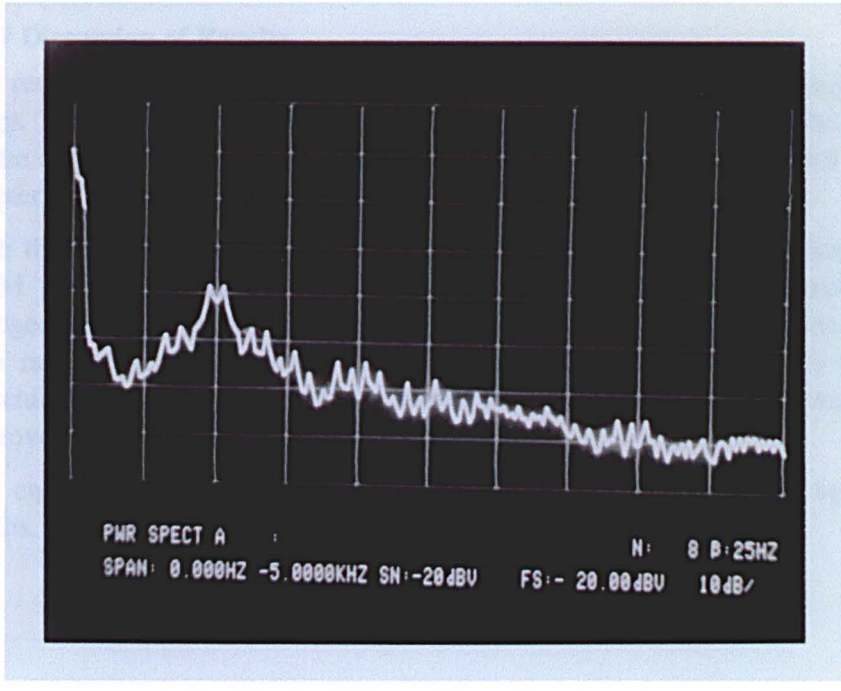

Figure 5.61 : *50Hz Current Harmonics*

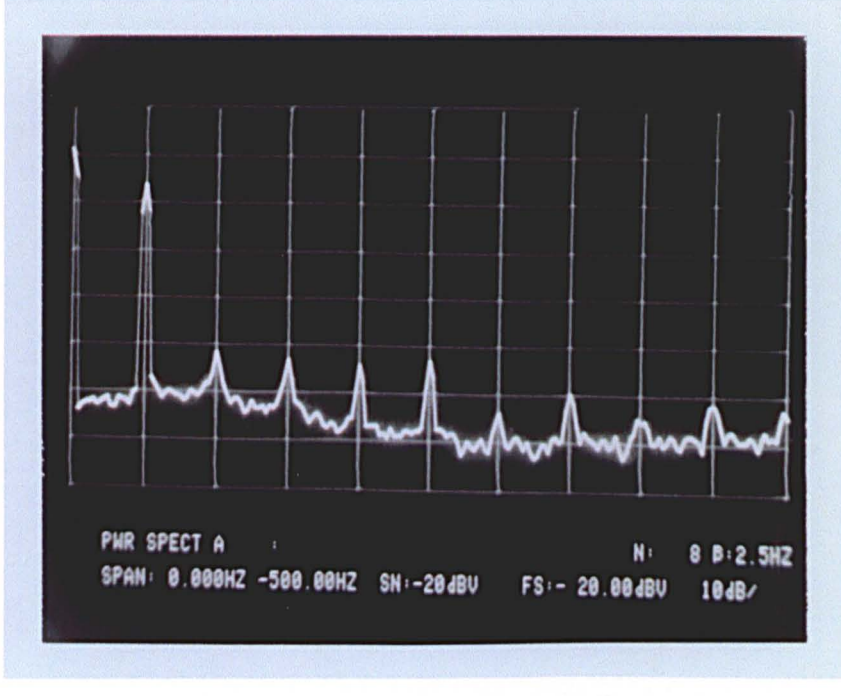

Figure 5.62 : *50Hz Low Order Current Harmonics*

5.6.7 Discussion of Results

The results once again show successful operation of the inverter throughout the frequency range. These are no load results provided to show that the effects of the advanced operation on the output waveform. These can be compared to the basic V/f control results presented in chapter 4.

With the vector control in operation, there is an increase in the transient demands on the PWM generator. This can be observed in the harmonic spectra presented. The carrier changeover events are completely independent and the PWM pattern becomes non repeating. This random behaviour, which could be described as chaotic, results in spreading of the switching harmonics. This is an incidental effect of the switching strategy that significantly improves the audible noise.

Full current capability has been demonstrated earlier in the chapter by the vector control results.

5.7 Conclusions

This chapter has described the advanced operation of an five level diode clamped inverter. Expanding on the basic operation described in chapter four, the operation of the circuit from a single DC link has been shown along with operation under a high performance four quadrant vector control scheme.

Capacitor balancing is achieved through the use of switching balancer circuits. This novel arrangement provides balancing of the upper and lower capacitor pairs. Control of the neutral point is performed by the same technique employed on the three level inverter. Range extension and current compensation have been included into the neutral point control strategy to allow the full operating range to be utilised. The balancing technique has been thoroughly tested via the vector control, placing rapid changes of current loading, and high transient conditions onto the DC link.

Operating results have been provided to show steady state operation with the full arrangement.

This work within this chapter fulfils the main project aim, demonstrating the full operation of a five level inverter.

5.8 Chapter References

[1] W. Leonhard, "Control of Electrical Drives", Springer-Verlag, 1985.

[2] M. G. Say, "The performance and design of alternating current machines", Sir Isaac Pitman & Sons Ltd, 1957.

[3] R. B. Giménez, "High Performance Sensorless Vector Control of Induction Motor Drives" PhD Thesis, University of Nottingham, 1995.

[4] D. Casini, M. Marchesoni, L. Puglisi, "Variable structure control system applied to multilevel power conditioning converters", Proceedings 1st European Space Power Conference, Madrid, Oct. 1989, pp 672-682.

[5] M. Fracchia, T. Ghiara, M. Marchesoni, M. Mazzucchelli, "OPTIMISED MODULATION TECHNIQUES FOR THE GENERALISED N-LEVEL CONVERTER", IEEE Conference Proceedings PESC'92, 1992, pp 1205-1213.

[6] J. –S. Lai, F. Z. Peng, "Multilevel Converters – A New Breed of Power Converters", IEEE Transactions on Industry Applications, Vol. 32, No. 3, May/June 1996, pp 509-517.

[7] G. Sinha, T. A. Lipo, "A Four-Level Rectifier-Inverter System for Drive Applications", IEEE Industry Applications Magazine, Vol. 4, No. 1, Jan/Feb 1998, pp 66-74.

[8] R. Rojas, T. Ohnishi, T. Suzuki, "PWM control method for a four-level inverter", IEE Proceedings Electric Power Applications, Vol. 142, No.6, November 1995, pp 390-396.

Chapter 6

Practical Considerations for a Medium Voltage Multi-Level Inverter

Chapter Contents

6.1 Introduction

The previous chapters have described the main research work completed during the project. Since the project included industrial support the aims of the project were based around a practical evaluation. There are several areas that need consideration when evaluating a design for a practical medium voltage inverter, the envisaged market for these topologies.

This chapter has been included to provide discussion of some of these areas, and to describe some of the ancillary work that was completed. The most significant part of the circuit is the power device. The IGBT was chosen for the prototypes built during the project, but this is not the only device that is suitable for these topologies. The operation of common devices will be discussed with regard to practical operation.

The use of series diodes was discussed in chapter 4 to obtain the blocking voltage requirement for the DC link connection diodes. This chapter will provide some discussion on the practicalities of this.

There are many areas that need consideration in a design of an inverter for this market, such as insulation and earthing. The basics of these areas will be discussed to provide background material.

6.2 Semiconductor Technology

The last decade has seen an explosion in power semiconductor technology, both metaphorically, or as many people working in the field will testify, often literally. At this time the invention of new devices (or variants of previous devices) seems to occur on a regular basis. No discussion on the practical considerations for a multi-level converter can be complete without mentioning the current and future options. Since IGBT devices were used throughout the project these received some evaluation work, and this is reflected in the detail included. Experience gained on the project also identified special requirements for the power diodes used in the circuit. This is an area that is sometimes neglected, but vitally important. The diodes used in a modern converter circuit are just as important technically as the switching devices.

6.2.1 The IGBT

The IGBT has become probably the "standard" power switch for many applications. It combines the ease of drive of the MOSFET with seemingly ever expanding voltage and current capability. Commercial devices are available from 600V to 3.3kV with 6.6kV expected in the near future. Current ratings vary from tens of amps to in excess of 1600A in a single module.

Figure 6.1 shows the basic equivalent circuit for an IGBT, and the typical physical construction. The construction shows the basic cell arrangement. These are then paralleled up across the wafer to provide a full IGBT chip.

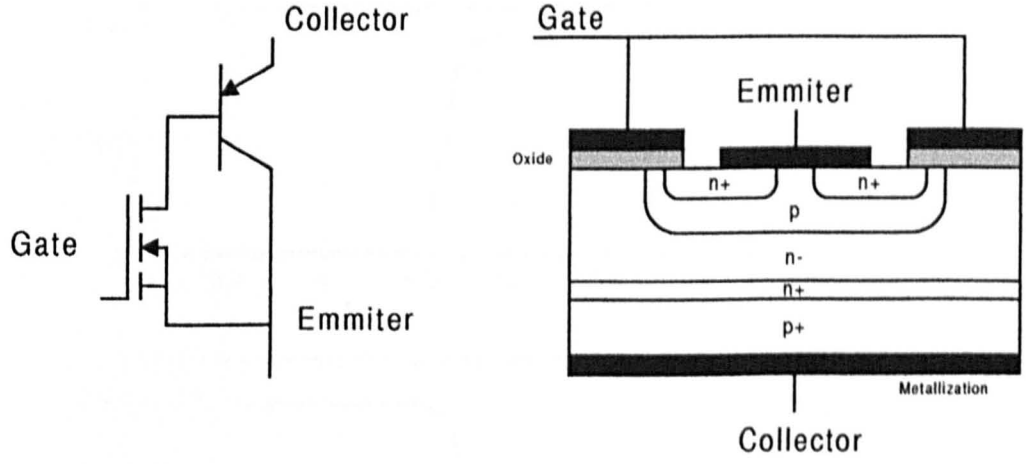

***Figure 6.1** : IGBT equivalent circuit and physical construction*

The current gain of the pnp transistor is low, and a significant component of the overall "collector" current passes through the MOSFET part of the structure. Whilst this may seem uneconomic from the equivalent circuit, it is this current sharing which provides the high switching speeds of these devices.

Typical turn-on and turn-off traces for a hard switched application are shown in figures 6.2 and 6.3. These are results taken from tests completed on a commercially available 1600V IGBT module. The test rig arrangement provided a reasonably low inductance for the circuit, hence the rather ideal voltage waveform for turn off. In practical applications it is likely that there will be some level of overshoot.

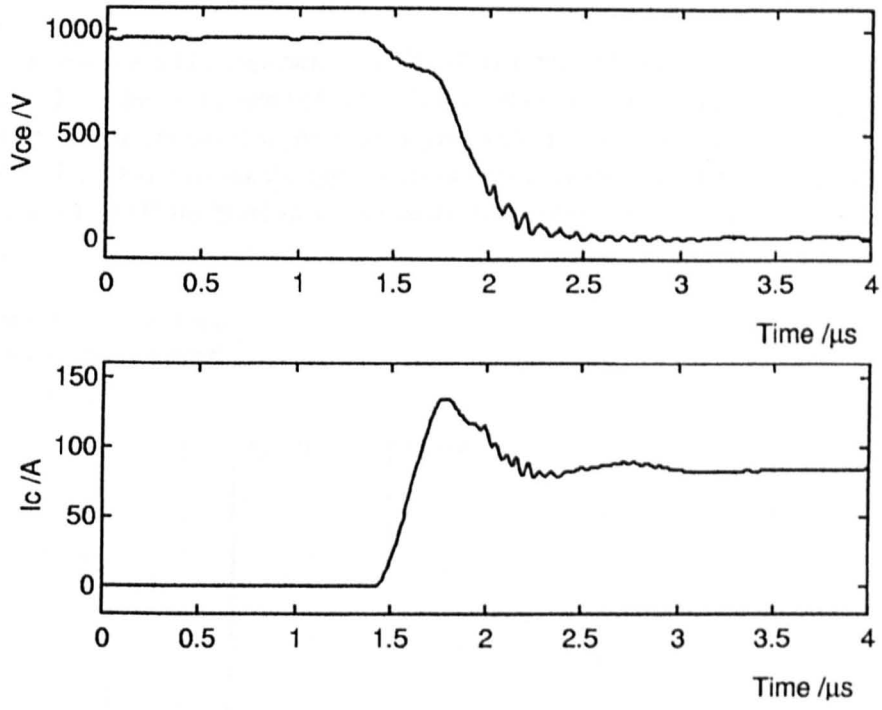

***Figure 6.1** : Typical IGBT turn-on*

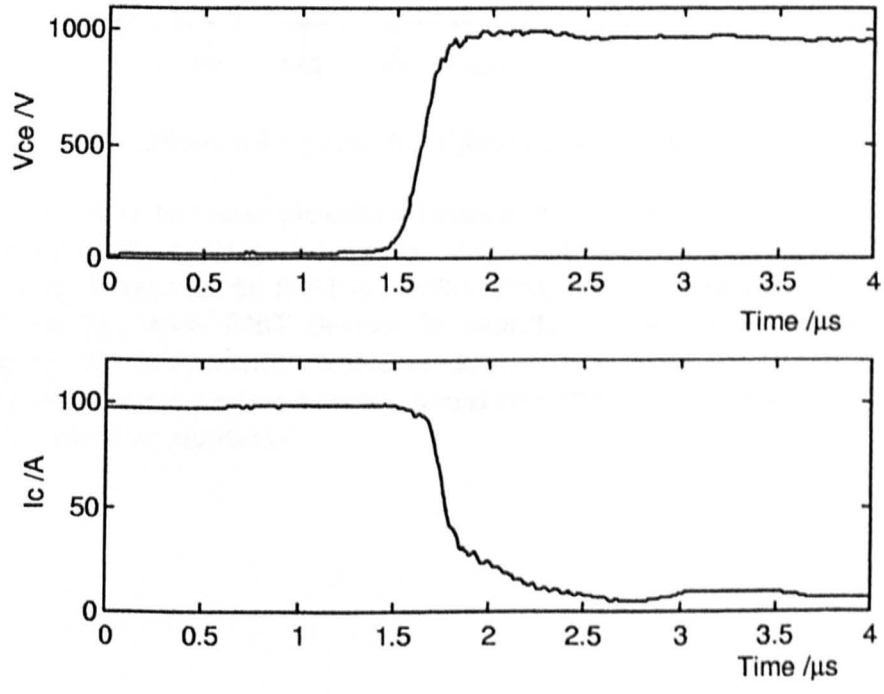

***Figure 6.2** : Typical IGBT turn-off*

One of the problems with early IGBTs was 'latch up'. The semiconductor construction includes a parasitic thyristor (p-n-p-n layers), which can turn on under high current conditions. Developments in the semiconductor design and addition of specially doped layers

have eliminated this behaviour provided the device is used with its specified safe operating area.

During normal switching operation the IGBT is saturated, and the collector emitter voltage drop is in the order of a couple of volts. The number of available carriers is dependent on the gate voltage. This means that for a given gate voltage there is a limit in the forward current capability. Figure 6.3 shows the typical set of characteristic curves for an IGBT. For a typical gate voltage of 15V, the level of de-saturation is approximately 10 times the nominal forward current.

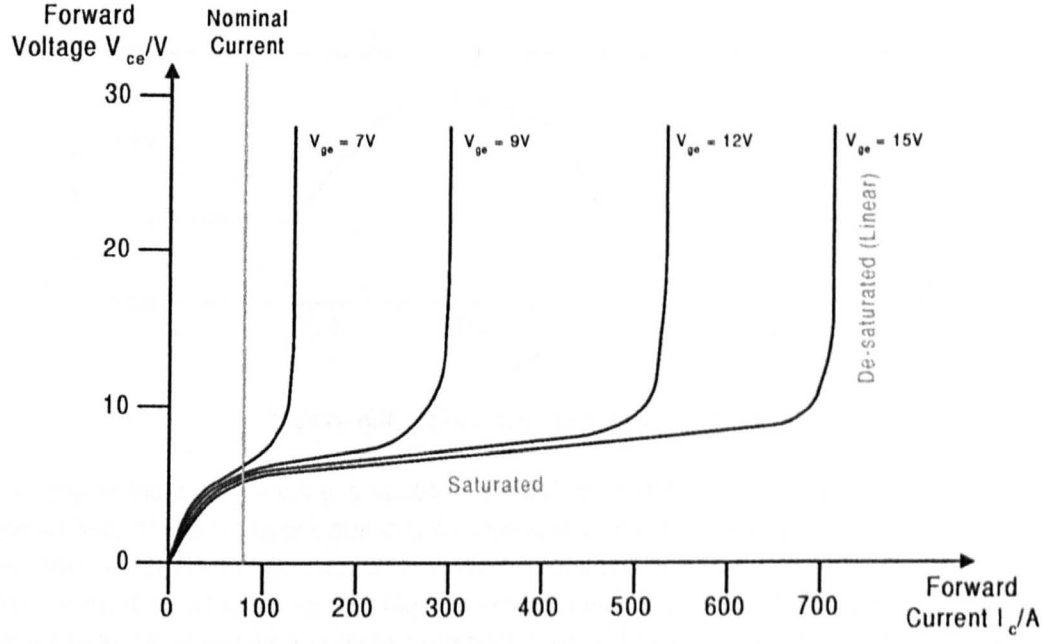

Figure 6.3 : *Typical IGBT forward voltage characteristic*

The de-saturation behaviour provides a mechanism of short circuit protection. The device will limit the current with an increase in voltage. Figure 6.4 shows a typical turn-on into a short circuit. In this case the IGBT is a 1200V/150A device. Power loss under this condition is extremely high in the IGBT. Devices are normally capable of withstanding this condition for around ten microseconds (dependent on junction thermal capacitance and operating temperature). If the device can be safely turned off within this time period then failure of the device should be avoidable [1].

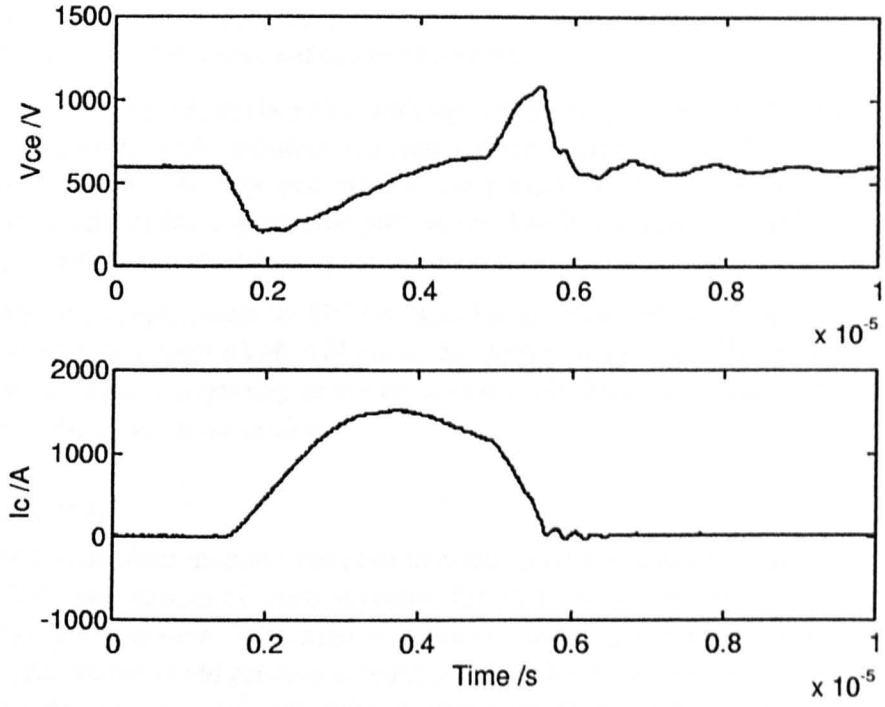

Figure 6.4 : *IGBT turn-on into a short circuit*

The requirement for placing a snubber around an IGBT is very much dependent on the application. The advantages that can be obtained through the use of a snubber circuit are a reduction in switching loss, and a decreased commutation speed. It is often the second factor that has most significance on any high power design. During turn-off any energy stored in the circuit inductance causes a voltage overshoot. The addition of a snubber may be necessary in order to protect the device during normal running conditions.

6.2.2 The GTO

The Gate Turn Off Thyristor market share has decreased over recent years. Whilst the GTO was once the favoured device for high power applications, the expansion of IGBT technology and corresponding increase in ratings has pushed the GTO out of competition for many new applications.

Figure 6.5 shows the basic four layer structure of a typical GTO. It resembles the conventional thyristor with several specific modifications to enable turn-off.

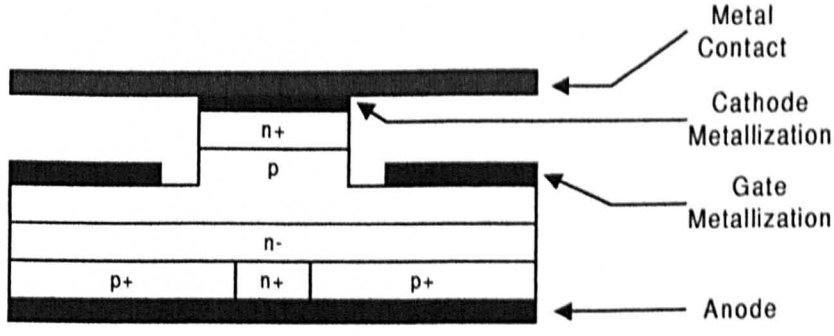

Figure 6.5 : *GTO Structure*

The GTO has a similar turn on mechanism to a conventional thyristor. A positive pulse of current is applied to the gate. As with conventional thyristors, the GTO can be triggered by a high dV/dt across the anode and cathode terminals.

The turn-off process is initiated by applying a negative gate current. The turn-off gain for a GTO is relatively small, resulting in a large current requirement (up to one third of the anode current is typical). The large gate current requirements are one of the main disadvantages for the GTO necessitating a substantial gate driver. The losses in the gate driver associated with the high current requirement are quite substantial.

Snubbers are a requirement for GTO devices for safe operation to be obtained. It has already been stated that a high dV/dt will cause the device to turn on. The presence of a turn-off snubber prevents re-triggering as the device turns off. Turn-on snubbers are often employed to reduce the losses in the device.

6.2.3 The MCT

The MOS-controlled-thyristor has been developing for a number of years. The integration of MOSFET gate structures onto thyristor for turn-on and/or turn off offers significant advantages. Combining the voltage and current ratings possible with GTO devices with a lower gate current could produce a nearly ideal device for many applications. Unfortunately the MCT has not yet realised it's full potential, with devices often having limited voltage and current capability, and in some examples, relatively difficult gating requirements.

Development in MCT technology is ongoing and recent developments in n-channel devices could see an expansion in market for this device.

6.2.4 Power Diodes

The discussion of semiconductor devices has to be incomplete without mentioning power diodes. In a circuit based on any of the above devices it is virtually impossible to escape the use of a suitable power diode. As the current, voltage and switching speeds continuously increase, then the diodes have to follow suit. In many cases the diode technology has actually fallen behind that of the switching device. This shortfall has generated an increase in the development of higher performance diodes. Figure 6.6 shows the basic semiconductor structure for a power diode.

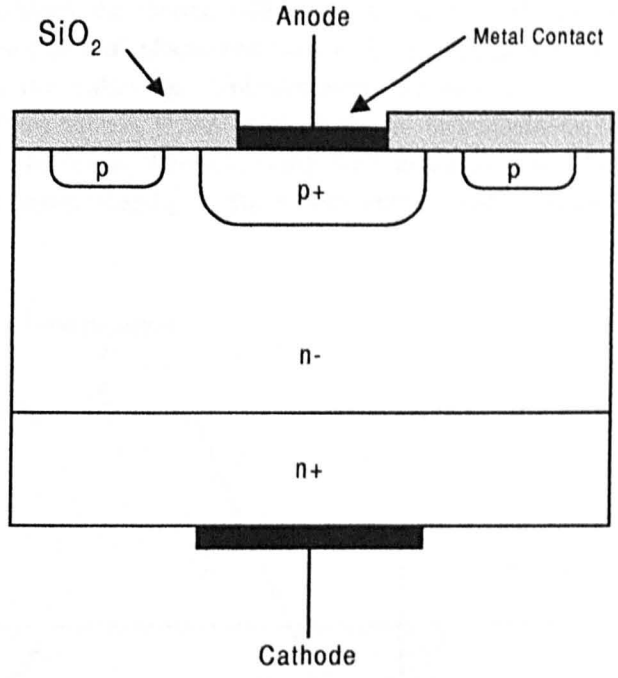

Figure 6.6 : *Diode structure*

The two main problems encountered are usually found when going from conduction to blocking. These are snap-off and dynamic avalanche. Ideal textbook descriptions will typically show a turn-off response similar to that in figure 6.7.

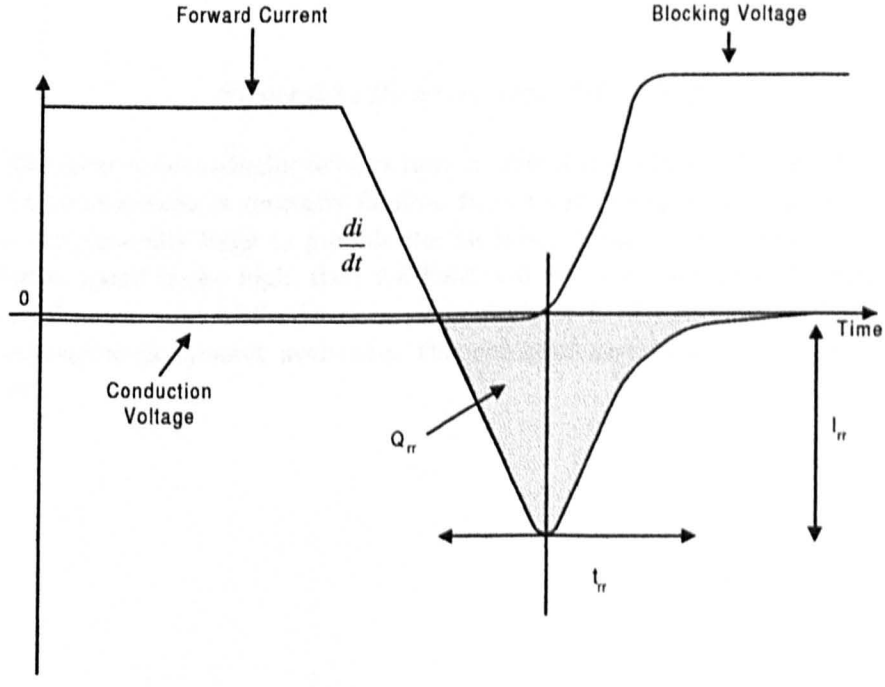

Figure 6.7 : *Ideal diode reverse recovery*

At turn off the forward current is swept out the device at a given rate. This is dependent on the associated switching device. The device can not immediately block once the forward current reaches zero due to the carriers still present in the junction. These are removed through the presence of a reverse current and natural recombination. Once the carriers have

been sufficiently reduced the device will begin to block volts and will then resemble a capacitor with an associated displacement current. A net charge will have been removed from the junction, given the value Q_{rr}. Unfortunately the recovery current does not always resemble the waveform shown. If the level of carrier recombination in the junction is too high, then snap-off can occur. This is exemplified in figure 6.8. The sudden high rate of change of current triggers ringing in the power circuit, with associated EMI and voltage stress problems.

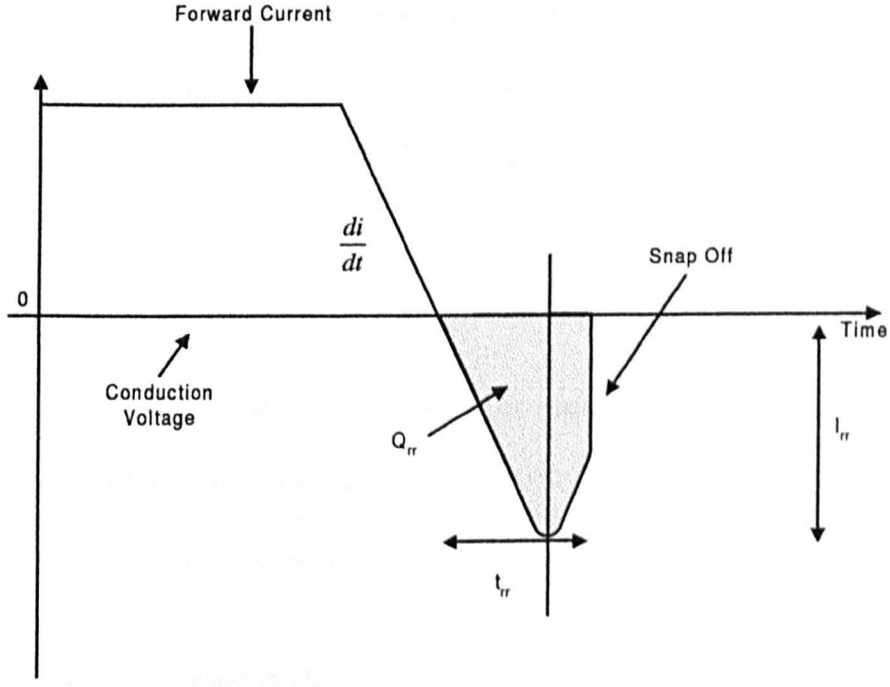

Figure 6.8 : *Diode recovery with snap-off*

Diodes like most semiconductor devices have a natural breakdown voltage where avalanche occurs. Static avalanche is generally familiar from zener diodes. In a large power diode, the junctions are generally large to provide the blocking voltage and current capability. If the commutation speed is too high, then the field will not distribute properly, causing a high electric field across part of the junction. This transient field can cause avalanche to occur. This is referred to as dynamic avalanche. This condition rapidly heats the device and failure will occur.

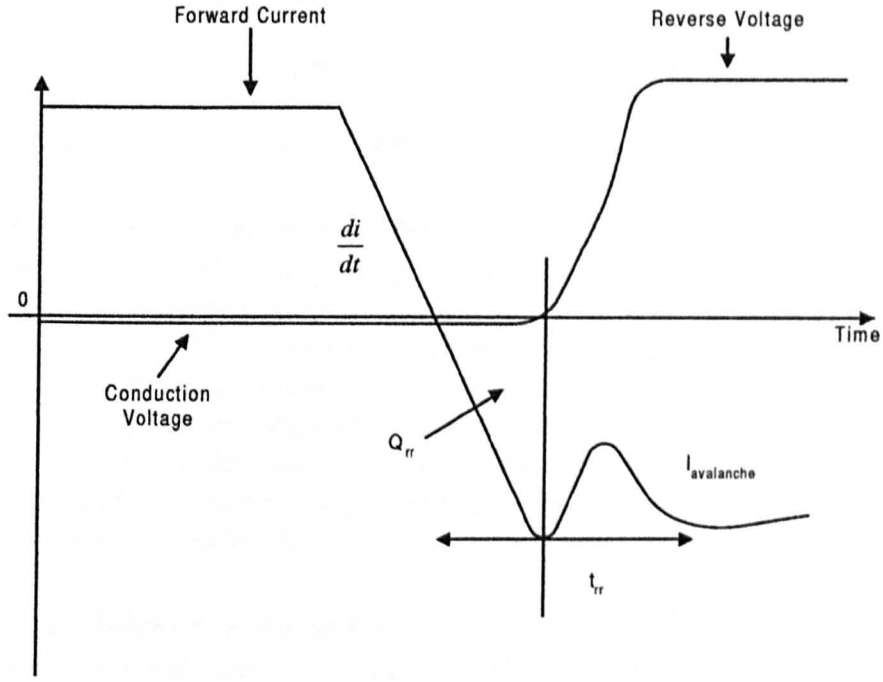

Figure 6.9 : *Diode undergoing dynamic avalanche*

Several manufacturers are now providing special diodes for high speed switching applications often using special doping techniques to control the lifetime of the carriers. Improvements to carrier lifetimes reduce Q_{rr}, thereby reducing the problems from snap-off and avalanche.

6.2.6 Conclusions on power devices

Semiconductor technology is an expanding area, with new materials and new device structures being developed. The above descriptions provide information on the significant devices that are currently available and suitable for a high power inverter. Others do exist, but these are either unsuitable for high power designs, or are variations on those described. Within a couple of years time the situation could well have changed.

Choice of power switch for a new drive will always be decided by cost, reliability, efficiency and practicality from the devices available at that particular time.

6.3 Series Device Operation (Multi-level)

The cornerstone of all the multi-level topologies is the individual switching of series connected devices to generate a number of voltage levels. This avoids the difficulties that can be encountered when simultaneously switching series devices.

6.3.1 Static Voltage Sharing for the IGBTs

Assuming switching does not occur simultaneously on series devices, there is still a requirement on the designer to ensure voltage balance. In steady state static conditions, the voltage sharing of a series string will be dominated by the leakage current of the devices. (The small forward current present when the device is in the blocking state). If the devices vary in leakage current, then sharing will not be achieved. The usual solution is to employ resistors across each of the devices, which will dominate the sharing provided the resistor current is designed to be significantly larger than the leakage current. It should be noted that this will result in some additional loss but this is not likely to be significant.

6.3.2 Voltage Sharing in Series Diodes

The diode clamped structure, when employed with more than three levels, does require that the diodes used to feed current back to the link capacitors have a blocking capability greater than the switching devices. In the case of the five level inverter that has been presented, then the diodes have to block three times the voltage of the IGBTs. This is likely to necessitate the use of series connected diodes.

The first issue has to be the choice of diode. The commutation of current into these diodes is driven by the switching devices (IGBTs in the examples), so the diode chosen has to be capable of handling the high dI/dt during switching. The diodes have to be matched to the device, and are likely to be the same class of device that are used for anti-parallel diodes.

Once the diode is selected, the sharing behaviour has to be examined. This can be separated into static and dynamic sharing. Static sharing as has already been mentioned is dependent on the leakage current, and can be simply controlled through the addition of parallel resistors.

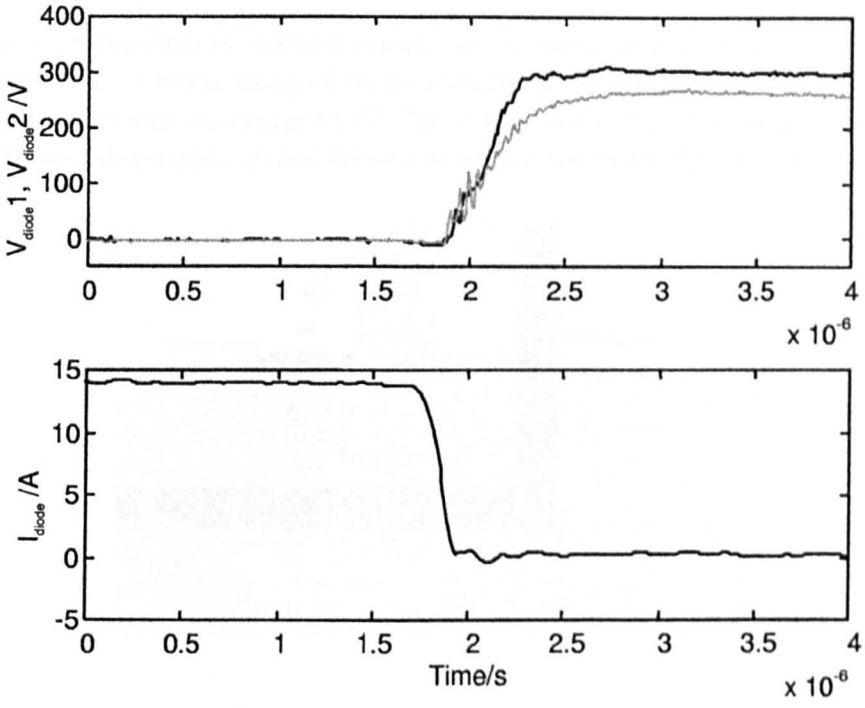

Figure 6.10 : *Transient voltage sharing in diodes*

Dynamic sharing is most significant at turn off. Variation of in reverse recovery charge (Q_{rr}) between devices will cause differences in voltage sharing. This is demonstrated in figure 6.10 which shows the voltages on two series diodes during a turn-off transient. The diodes used were classified as 'ultrafast', and exhibit a very low reverse recovery current which was not identifiable on the current trace. Differences were significant enough to cause a difference in the voltage waveforms for the two diodes.

Sharing can be improved by the addition of an RC snubber. The presence of the parallel capacitance dominates over the reverse recovery current. The sharing will therefore be defined by the tolerance in the capacitors. The resistor is required to limit the current when the diode turns on. This technique has been used on series thyristors for a number of years.

6.3.3 Conclusions

With dynamic sharing of the switching devices unnecessary on a multi-level inverter, the only real sharing problem is in the diodes used to connect back to the DC link nodes. Diode sharing can be enforced reasonably simply with the use of RC snubbers.

6.4 High Voltage Insulation Considerations

The recent development of medium voltage drives opens up a wide new field of emerging technology. As the voltage rating of the semiconductor components has increased, the system implications have increased several fold. The largest impact is in the insulation requirements. Insulation breakdown takes several forms that are exemplified in figure 6.11.

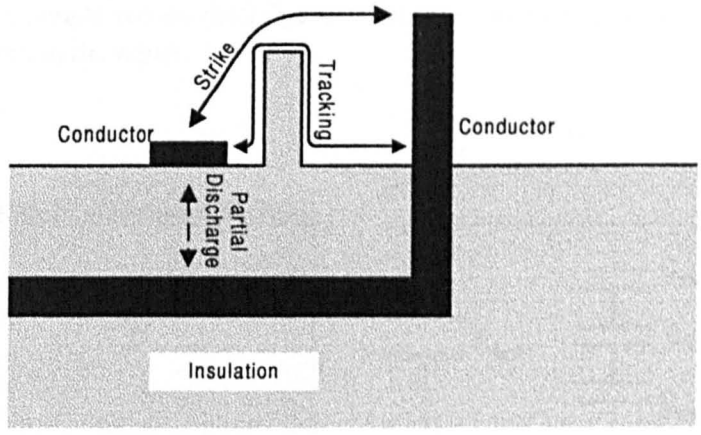

***Figure 6.11** : Insulation breakdown modes*

6.4.1 Strike

The most intuitive insulation factor is the separation of bare conductors. The static breakdown condition for dry air is 1.2kV/mm. Variations in humidity, ionisation and voltage impulse characteristics require a significantly lower design rating [2]. The arc conditions that occur during this class of breakdown causes ionisation in the air, thus the breakdown is self supporting (The voltage required to sustain the arc is significantly lower than the initial voltage).

6.4.2 Insulation Materials and Dielectric Properties

With modern chemical processing, the range of insulation materials available is impressive. The basic requirement of an insulating material is relatively simple. Withstand a high electric field strength with minimum leakage current. Dielectric materials are often used, since they provide the maximum insulation properties for a given material thickness.

Dielectric materials polarise under an electric field. The current flow associated with the polarisation produces losses in the material. In poor dielectric materials the losses cause heating which can result in deterioration of the insulation over a period of time

6.4.3 Tracking

Insulation breakdown can occur across the surface of an insulating material [2]. Contamination of the insulation medium along its surface can allow a small leakage current to flow. This leakage can result in a conductive layer being deposited onto the insulation. Arcing then occurs between the conductive areas, eventually complete failure occurs. The production of conductive areas in this way is known as tracking.

The process propagates slowly across a surface and failure can occur after a period of time.

6.4.3 Partial Discharge

Discharges occur when an electric field exceeds the breakdown voltage. Partial discharges are indirect non-sustained discharges that occur in and around insulation. The typical example usually quoted [3] is an air bubble within an insulating medium. This is shown in figure 6.12. The example can be modelled as a simple capacitive divider, and the equivalent circuit is also given in the figure.

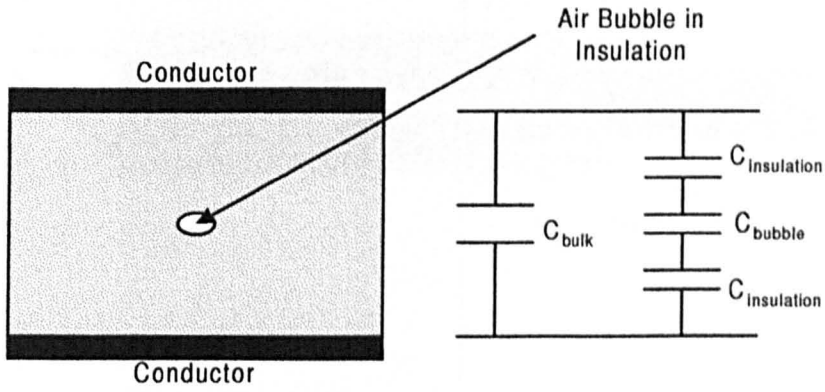

Figure 6.12 : *Air bubble in insulating medium*

The high permittivity of the insulation medium means that during a voltage transient, a high proportion of the voltage will appear cross the air bubble ($C_{insulation}$ being much larger than C_{bubble}), until breakdown occurs. This process can repeat several times through a particular transient. The breakdown will be short lived, since the energy is limited to that stored in the effective bubble capacitance. Whilst the energy dissipation of a single partial discharge is small, it is localised to a very small area. Repetitive breakdown can cause damage within the insulation causing failure after a period of time.

It is important that materials are manufactured correctly to avoid air bubbles if they are to provide the required insulation.

Another common form of partial discharge is corona occurring on the ends of machine windings set into the stator. Figure 6.13 shows a typical arrangement. During transient conditions the field distribution around the conductor as it exits the stator results in partial discharging. This is visible as corona. The effect is applicable to any conductor arrangement with air insulation.

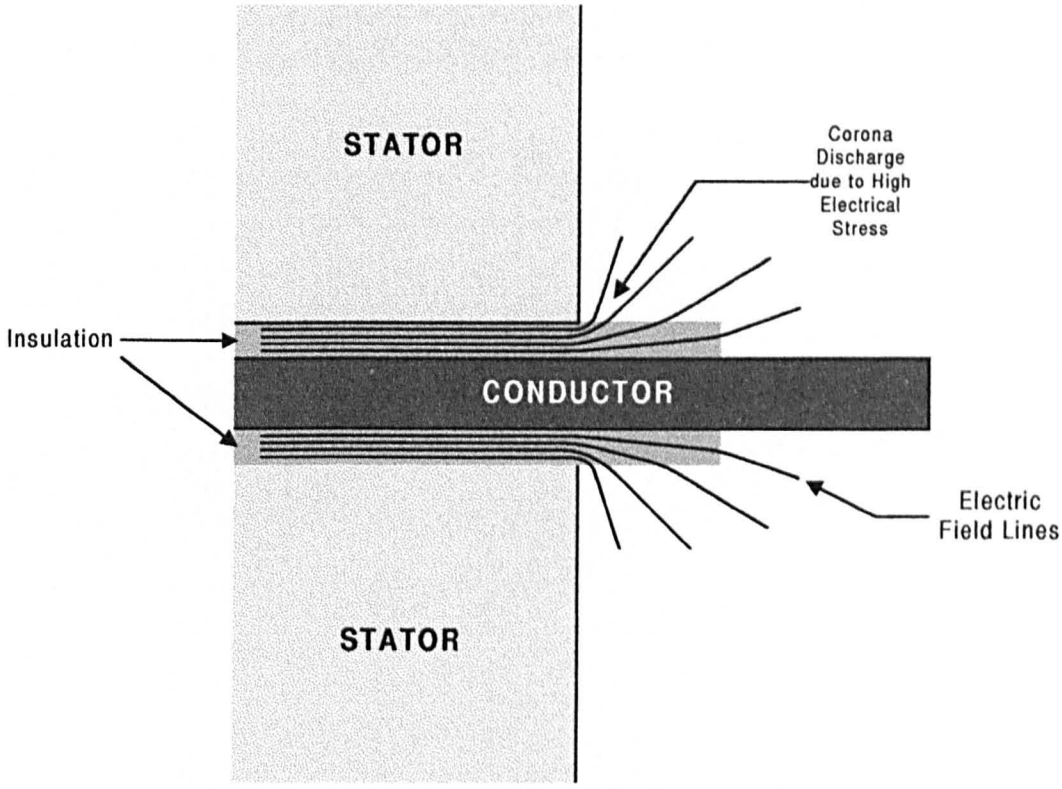

Figure 6.13 : *Corona discharge example*

6.4.4 Machine Considerations

The area of machine insulation has become topical for high power medium voltage designs as the motor drive market has expanded. Modern fast switching converters introduce fast voltage transients onto the motor windings, which needs to be addressed. The two areas of concern are the dv/dt and the overshoot [4].

Most windings can be modelled by an equivalent circuit similar to that shown in figure 6.14.

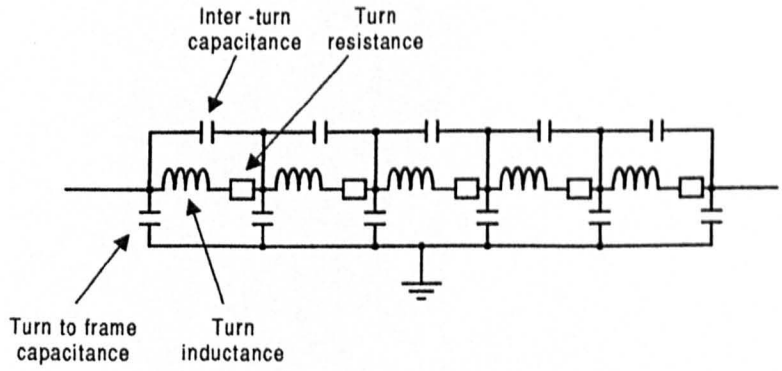

Figure 6.14 : *Winding equivalent circuit*

The basic inductive winding, with the expected series resistance is combined with a capacitor network. The distributed nature of the ground capacitance means that due to the propagation of the voltage transient is slowed, with the first turn being exposed to significantly higher voltages than might normally be expected. This can result in failure of the turn to turn insulation.

The second problem, the overshoot is a consequence of the inverter and the transmission line effects of the motor cable. The machine winding voltage can see significant overshoots that can exceed twice the switched voltage in certain conditions.

It should be noted that both these situations are partially mitigated against by the use of a multi-level inverter topology with its stepped output waveform.

6.4.5 Conclusions

Insulation issues are an essential design criterion for a medium voltage inverter drive application. Correct design of the insulation system is likely to be the single largest driving force in the practical layout of an inverter for these voltages.

6.5 Earthing and EMI

For medium voltage drives based on VSI configurations, earthing of the converter and the motor become extremely important. Failure to approach this correctly will result in currents circulating around the system, producing high levels of electromagnetic interference. Failure to design around this will produce numerous problems

6.5.1 Motor Earth Capacitance

With very few exceptions, all the different types of electrical machine are based on windings set in or around a magnetic core. Taking the stator of an induction motor as an example, the windings are arranged in slots lining the bore of a laminated steel block. The stator, which is fixed inside the casing, can normally be considered to be at earth potential. Because of this arrangement there is a distributed capacitance between the windings and the frame. See figure 6.14 in the previous section for the equivalent circuit.

6.5.2 Earth Current Generation

Any change of potential of a winding within the machine will result in a current being drawn to charge the winding to earth capacitance. The typical current path is shown in the following figure.

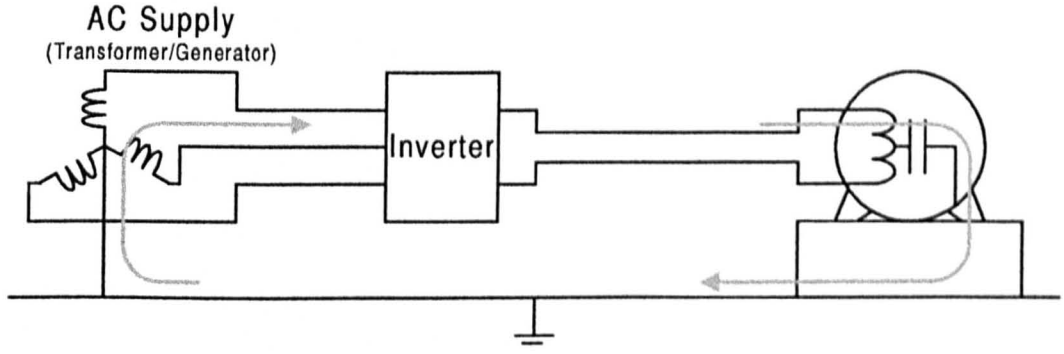

***Figure 6.15** : Earth Current*

If the capacitance to frame of the machine is distributed evenly, then provided the winding is switched symmetrically, then their should be no net current drawn through the earth path. The presence of common mode voltages however will always try to induce currents in the earth path.

This is one problem with utilising the redundant states in the switching strategy for DC link balancing (see chapter five section 5.3). Whilst the vectors {+2E, 0, -E} and {E, -E, -2E} are equivalent as far as the fundamental machine currents are concerned, there is a difference in common mode voltage. Switching between these states as part of a capacitor balancing scheme for example does impact on the earth current.

The design of a strategy to prevent earth currents is very particular to an individual application. Distances between the inverter to motor, and the zero sequence impedance of the supply all affect the behaviour of the system.

6.6 Conclusions

This chapter has provided background information to a wide range of topics that are important for the design of a practical high power inverter based on a multi-level topology. The information is not exhaustive, and does not constitute a design manual. It should provide some interest however, and sense of reality to the discussions in the previous sections.

The design of a practical multi-level inverter is not a simple task, and cannot be underestimated.

6.7 Chapter References

[1] P. W. Wheeler, C. Newton, "An investigation of the turn-off characteristics of an IGBT under short circuit conditions", Conference Proceedings EPE'97, Trontheim, Vol.4, September 1997, pp 29-33.

[2] W. Fordham Cooper, D. A. Dolby Jones, "Electrical Safety Engineering", Butterworth Heinemann, 3rd Edition, 1993.

[3] D. Hilder, "Partial-discharge measurements for insulation quality", IEE Power Journal, March 1992, pp 79-86.

[4] A. H. Bonnett, "Avaliable Insulation Systems for PWM Inverter-Fed Motors", IEEE Industry Applications Magazine, Vol. 4, No. 1, Jan/Feb 1998, pp 14-26.

Chapter 7

Conclusions

Chapter Contents

7.1 Conclusions

7.1.1 General Conclusions

Developments within the drive market has seen a steady increase in converter power rating over recent years, with interest now being given to medium voltage inverter drives. Multi-level inverter topologies are one of the options for this market. This thesis has considered the multi-level inverter both from the functional point of view, and for its suitability to this application.

The three different types of inverter that fall into the multi-level category were described in chapter 2. The advantages and disadvantages for each of the circuits were discussed and it was concluded that for motor drive applications, the diode clamped topology offered significant advantages over the H-bridge circuit (in particular the lower magnetic component requirement), and the flying capacitor arrangement (simplicity of control). However it was noted that the H Bridge system had already seen commercial exploitation, and the flying capacitor circuit had seen industrial development.

Having selected a general circuit topology for investigation, multi-level switching strategies were then considered. SVM and sub-harmonic modulation strategies were considered equally valid. The later strategy was selected, as there was little previous work reported on practically implementing the strategy with a five level inverter.

The construction of the three level diode clamped prototype was presented in chapter 3. A fully operational system was demonstrated. A modified PWM algorithm was proposed to improve the transition between the two carrier signals, and this was successfully implemented. A novel control system for maintaining neutral point control when the capacitor mid-point is not connected to the supply neutral was also proposed. The basic performance of this controller was confirmed. The chapter concluded by suggesting operating range extensions to the neutral point control, by employing 3rd harmonic addition and bus clamping within the modulation strategy. This was confirmed by mathematical analysis, and experimentally verified with the five level inverter. The three level diode clamped inverter is now commercially available from companies such as Siemens and Toshiba. The work here confirmed the maturity of this technology.

The five level inverter was considered in more detail in chapters 4 and 5. A modified version of the sub-harmonic PWM method was devised and implemented successfully on the five level inverter prototype, providing a flexible waveform generation that could move rapidly between different voltage references without breaking the switching laws. The first inverter prototype received power from individually isolated DC supplies, and the unsuitability of this arrangement was demonstrated by the large voltage regulation under load. A single DC link supply was preferable and methods for achieving DC link capacitor voltage balance were reviewed. The use of modified output switching techniques was rejected, as these techniques were only valid over a small area of the inverter's operating range. Extra circuitry was therefore required and a novel capacitor balancer circuit is presented in chapter five. Design, construction and control are all evaluated, and the performance of the final system is demonstrated over the full four quadrant range of the system, and also under severe load transient conditions (a vector controlled induction motor drive). The balancer proved extremely effective. Its power electronic design, which is effectively a fourth semiconductor leg within the inverter, coupled with its stand alone operation, make this system an industrially viable arrangement.

Chapter 5 concluded with an investigation of the neutral point control for the five level system. The techniques described for the three level inverter were successfully implemented. Again, successful operation was demonstrated, even under severe transient conditions.

Chapter 6 described some of the areas for consideration in the design of a practical inverter. Choice of power device is discussed, with practical results presented from testing of devices completed during the project. Other issues are discussed including insulation, and EMC/EMI. This chapter provides some practical background to raise some of the issues that occur in practical design.

7.1.2 Final Conclusion

The final conclusion from this work is that a working five level inverter can be built, and solutions obtained to overcome any operating difficulties. Operation has been demonstrated of a five level inverter drive, with high performance current control operating from a single DC link.

7.2 Areas for future investigation

Possible areas for future investigation on the prototype inverter rig constructed during this project are listed below.

- Operation of the five level diode clamped inverter as a sinusoidal rectifier
- Sinusoidal rectifier operation into split loads (individual loads for separate levels in the DC link)

Areas of work beyond the prototype inverter are as follows.

- Development of a working inverter at a higher operating voltage and current.

Appendix 1

Prototype Construction Information

Appendix Contents

A1.1 Introduction

This appendix provides details from the construction of the two prototype inverters investigated during the project. The main emphasis of the project was the power electronics and the control strategies that were implemented. The main chapters have described the fundamental operation, and contains much of the new work associated with the project.

The development of hardware and software for the system is predominantly based on classical design techniques and the details of this is therefore only given as an appendix. The inclusion of this information should allow the hardware to be utilised in other projects to further the work documented here.

A1.2 Microcontroller System

The control system of the prototype inverters is based around a Siemens 80C166 microcontroller [1]. The processor/controller used is supplied on a standard half height rack board. To enable connection to the board through the edge connector, and to provide a versatile system that could be easily modifiable, a backplaned rack system was designed.

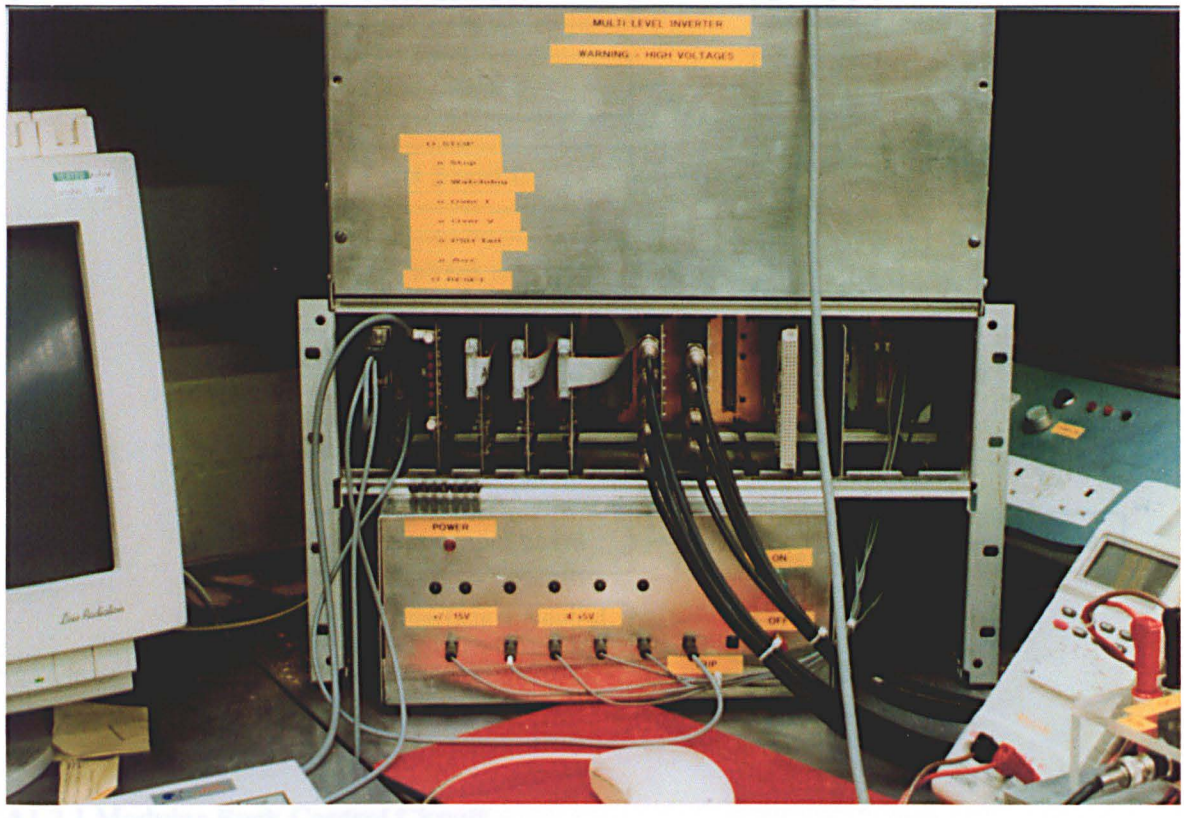

Figure A1.1 : *Photograph of Control Board Rack*

An overview of the final control board arrangement for the five level prototype inverter is shown in figure A1.2.

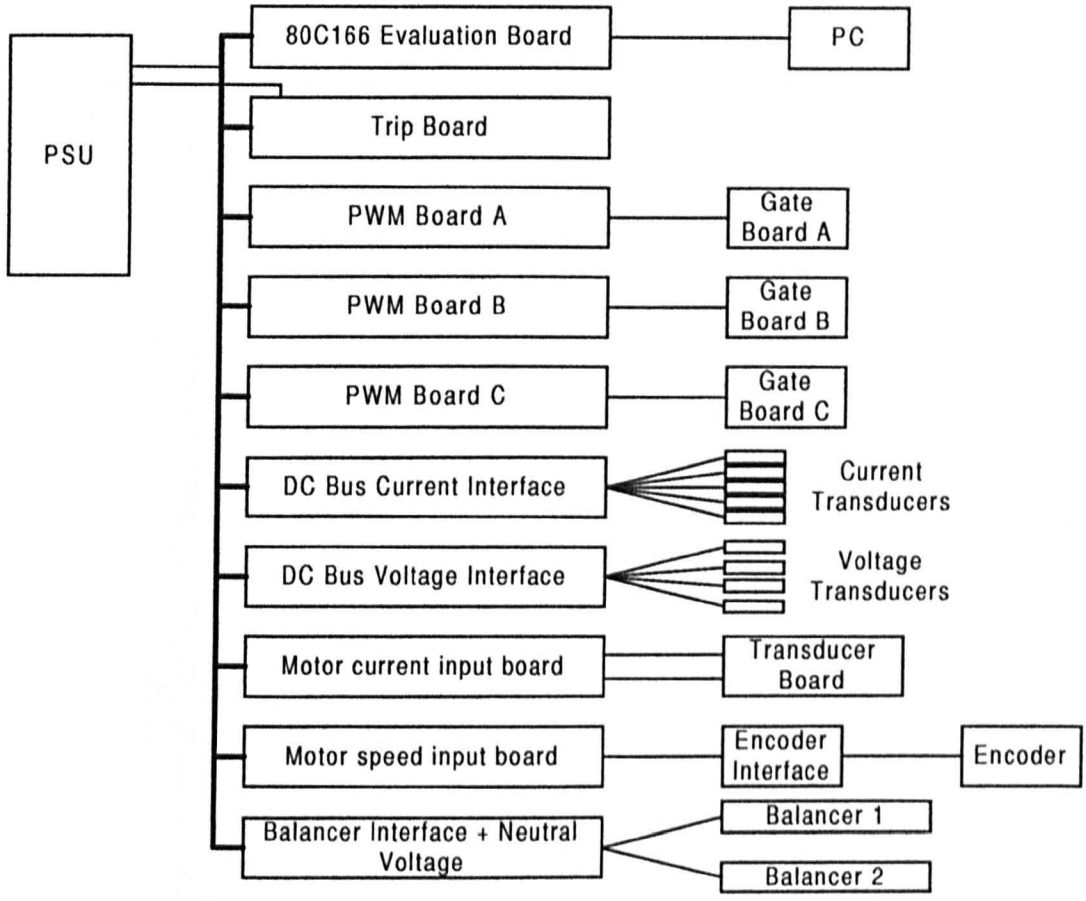

***Figure A1.2** : Control boards for the five level inverter*

A1.2.1 Modular Rack Control Circuit

The functional block diagram of the backplane rack arrangement is shown in the following figure. The emphasis in the design of the backplane was to make the arrangement as modular as possible from the start so that it could develop freely as the prototypes were designed. It was decided to mount the gate driver boards within a screened box above the control rack. Gate signals were then connected to the devices via coaxial cables.

The backplane provides connection of digital and analogue signals between boards. It also provides a common power bus, with +5V and ±15V.

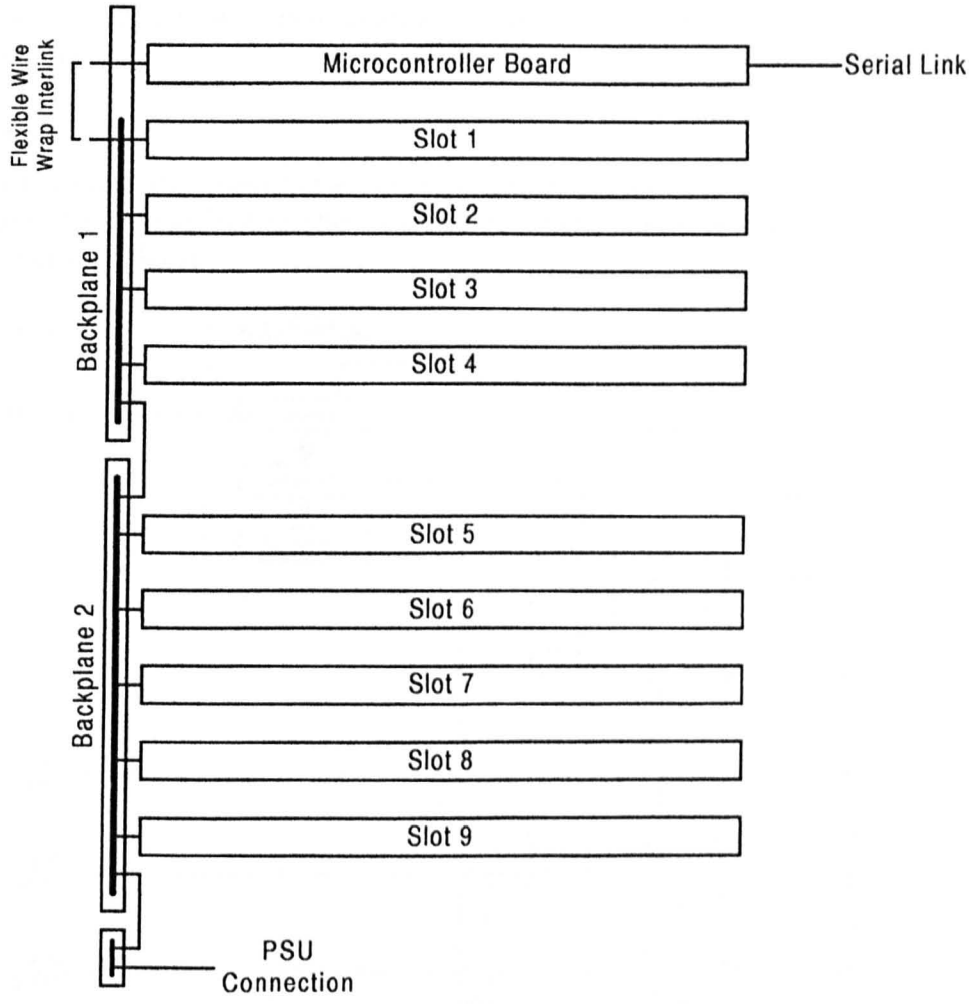

***Figure A1.3** : Backplane arrangement*

A1.2.2 Microcontroller Evaluation Board

The microcontroller board used during the project was an EVA166. This board includes the processor, clock crystal, EPROM boot memory, RAM, memory decode logic and the RS232 interface. With this arrangement, no other components, other than a power supply, and serial connection are required to get the board operational. All processor connections are brought out to a 96-way standard rack connector.

The board connects the reference for the in-built analogue to digital converter on the processor to the five volt power rail. It was found that the power rail would fluctuate quite significantly during operation, which caused errors in the analogue information captured by the processor. Modifications were made to the board to remove this link, and a precision reference was connected to provide a stable reference. The board includes a manual switch that changes the memory map location of the EPROMs and the RAM. This enables the user program to be downloaded, then executed without the use of the EPROM. In this mode the bus settings can be set for maximum processor speed(beyond the timing limits of the EPROMs).

The 80C166 microcontroller includes internal function blocks that provide many of the core functions of the control system. These include analogue to digital conversion, serial communications, counter/timing, and PWM generation. It is the in built ability of the

processor to perform the pattern generation that has led to much interest from the drives community.

A1.2.3 Trip Board

The first board in the system is the trip board. This board provides a central link point for all the protective systems built into the control. A functional block diagram of the board is shown in the following figure.

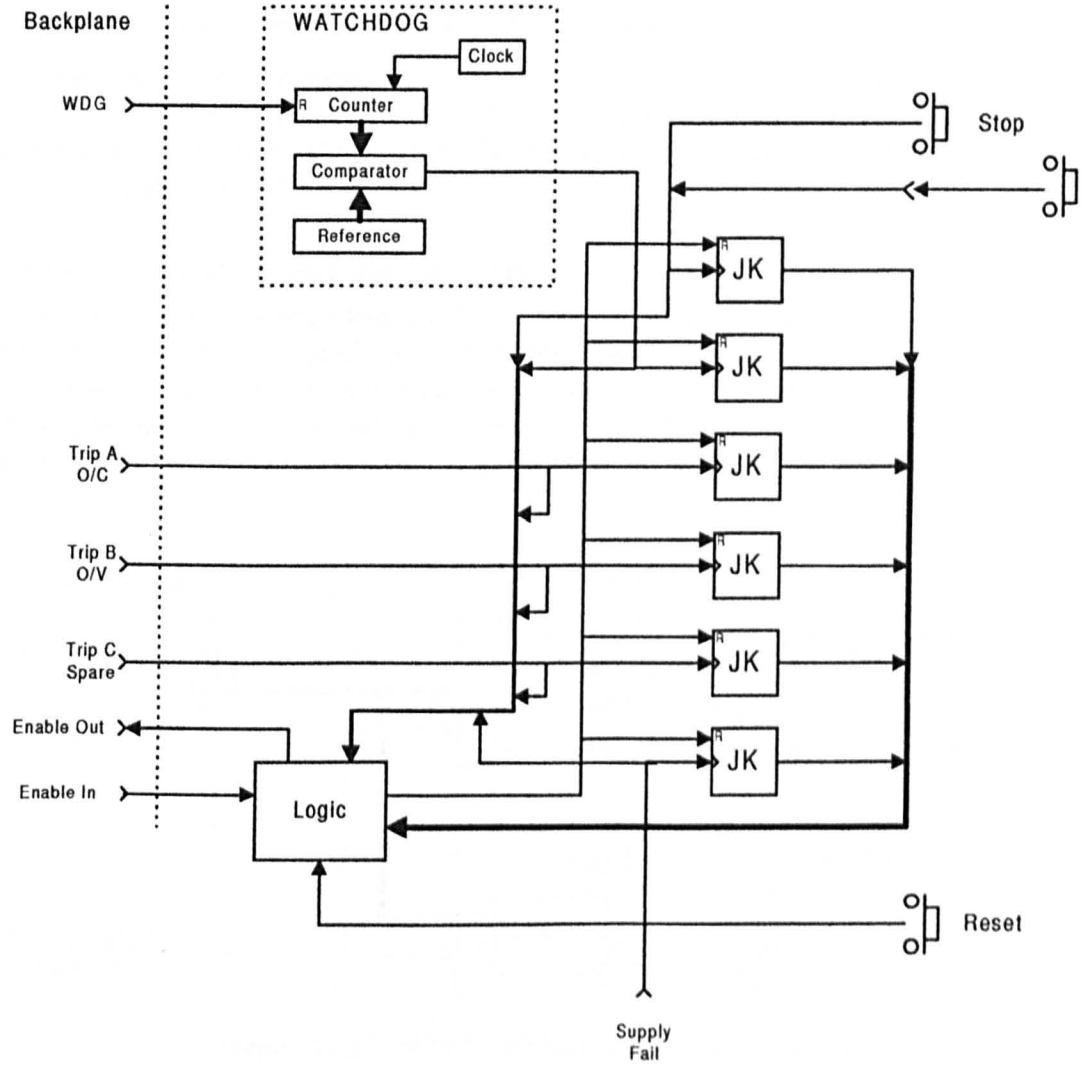

Figure A1.4 : *Trip Board Functional Block Diagram*

The main function of the board is to receive trip signals from the back plane, and latch these in the event of a trip occurring. The processor board produces an active low output enable signal (which through the use of a pull up resistor defaults into the safe state). The trip board reads this signal in, and outputs a safe enable to the PWM boards which will be disabled once a trip is registered. Indication of the particular trip is given through the LEDs mounted on the end of the board.

Resetting of the trip latches is interlocked to the incoming enable system so that a trip cannot be cleared until such time as the processor program has stopped the PWM. This ensures that the correct ramp-up procedures are observed. The trip inputs also interlock back to the reset

so that any active trip will prevent resetting. This is an important requirement since the trip latches are edge triggered, and could be reset in a fault condition without this interlock.

Two trip conditions are built into this board. The first is a simple stop button arrangement. Two buttons are present, one on the edge of the board, the other remotely mounted on a small box on the desk for easy access. The second trip on the board is a watchdog unit. Each time the processor interrupt routine is run a pulse is transmitted on a particular processor pin, which is fed to the trip board via the backplane. A timer circuit on the board measures the interval between the pulses, and if the gap is too long, indicating a software problem, the trip is activated. The trip time is variable, and set by DIP switches.

An additional trip on the board is fed by a signal from the power supply unit. This indicates power fail to the AC supply. The PSU is battery backed up, so the processor uses this signal to complete shutdown of the inverter. This provides interlock into the standard emergency stop system that shuts off the AC supply.

A1.2.4 PWM Deadtime and Opto Driver Board

Three boards were built to perform the PWM interface through to the gate driver boards. Each board would accept four signals, and provide eight outputs, arranged as complementary pairs. The board introduces timing delays between the complementary pair to avoid shoot through. These are independently configured to allow compensation for component tolerances. The block diagram for the board is shown in figure A1.5.

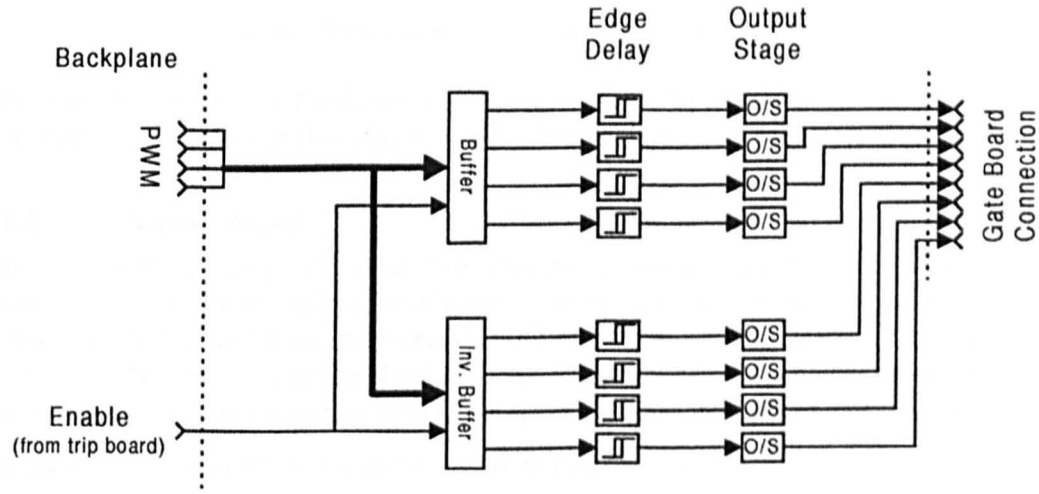

Figure A1.5 : *PWM Board Functional Block Diagram*

PWM signals are taken from the processor via the backplane. The board is capable of handling four signals, or one phase of a five level inverter. The input signals are sent to a pair of tri-state buffers. The enable signal from the trip board controls these, so that under fault conditions (when the enable signal goes false) all the outputs are turned off. The delays are introduced by simple RC circuits with bypass diodes to select the appropriate edge.

The output stage is based on the circuit shown in figure A1.6. This is a conventional current mirror circuit that provides a current drive to an opto-coupler. In this application of the circuit, the input transistor is an NPN bipolar transistor, which will turn off when the input goes open circuit. The circuit has been shown to provide a reasonable speed of response with high noise immunity. The circuit in this form is limited in its voltage operating range (nominal +5V), since thermal drift can occur due to the temperature dependence of the transistor gains.

This circuit was designed to try to provide a high noise immunity on the signals through to the gate drivers, which are mounted remotely. The resistor in the current return path from the opto-coupler is in the order of ten ohms to provide an impedance to earth to limit noise pick-up being injected back into the ground.

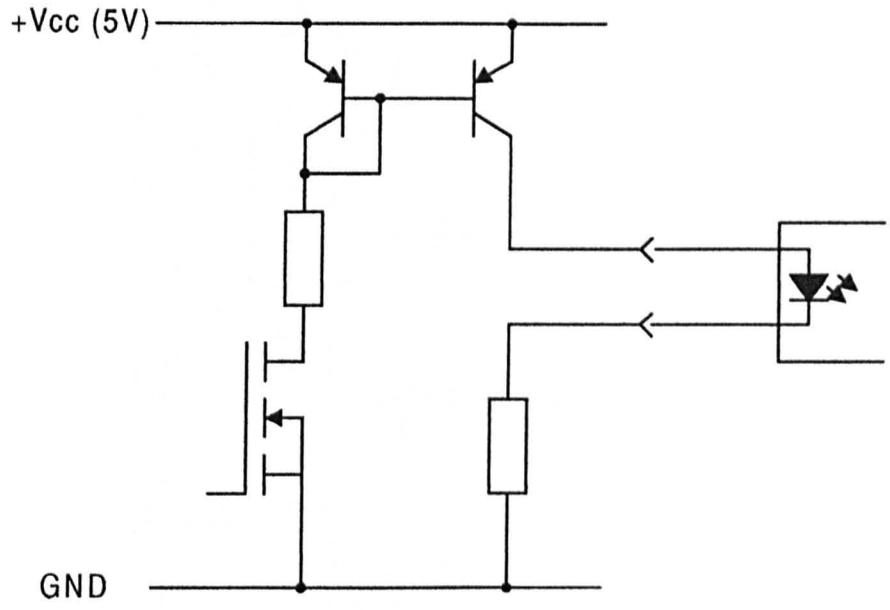

Figure A1.6 : *Generic Current Mirror Output Stage*

The board is connected through to the gate drivers via a 16-way ribbon cable with standard IDC connectors. Each signal is next to its independent return signal to avoid cross-talk.

A1.2.5 Gate Driver Board

Since each IGBT in the power circuit needs it's own driver board, for a five level inverter this means 24 boards. Hand building these boards was not an economic use of time on the project, so standard driver sub-boards were obtained from the sponsoring company. These we capable of driving the devices used without any modification or additional circuitry. The only requirement for the project was to arrange the power supply and connections to these boards.

The gate driver board block diagram is shown in figure A1.7.

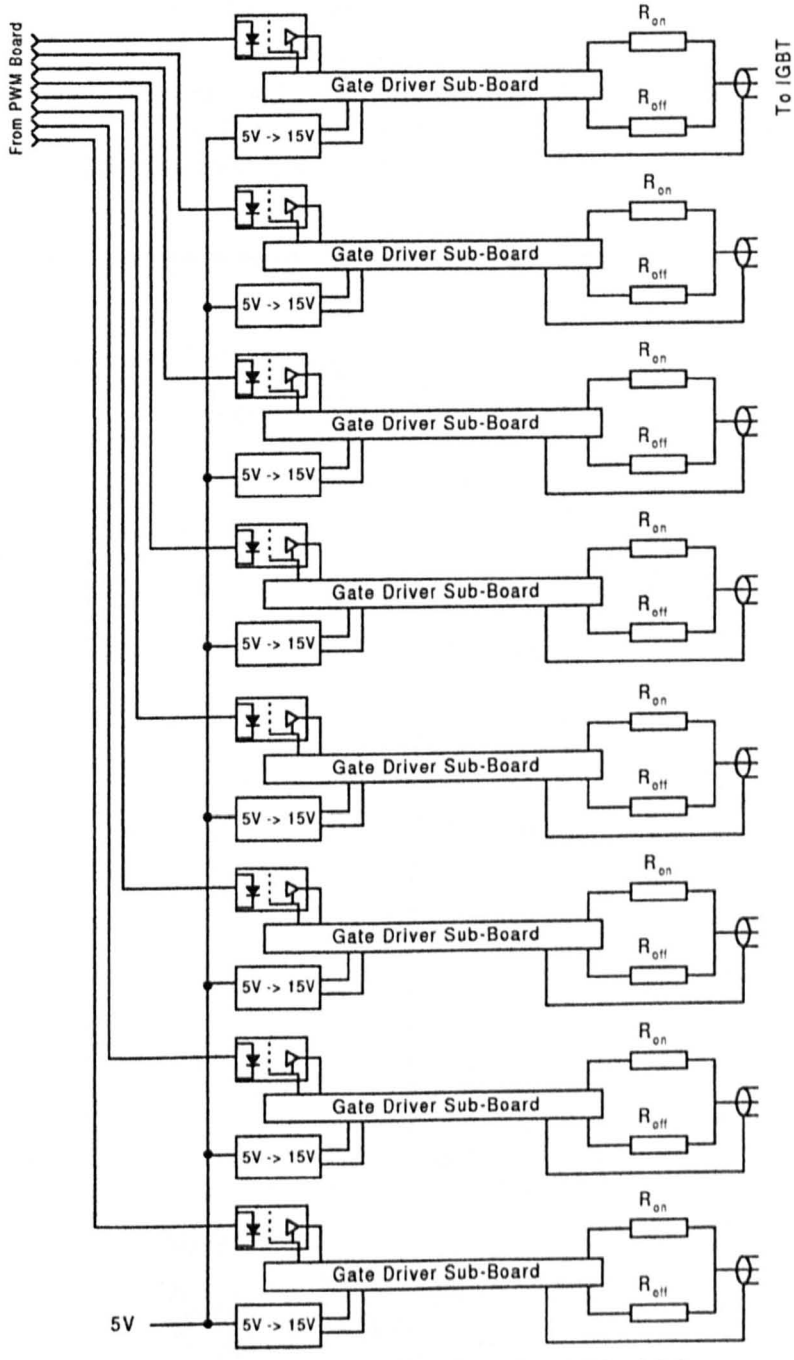

Figure A1.7 : *Gate Driver Board Functional Block Diagram*

Each gate-driver needs it's own isolated power supply. Since the prototype inverters that were developed during the project were fed from the standard 415V supply, the isolation requirement was limited to 1000V. This allowed the use of individual standard switching power supply modules (Newport NME0515D). Signal input is via high common mode immunity opto-couplers. The output of each gate driver is connected to an isolated BNC plug at the back of the board.

Three boards were used to provide the required number of gate drivers, and these were enclosed in the screened box mounted above the rack. Input signals are via a ribbon cable connected to the PWM board for the particular phase.

A1.2.6 DC Bus Current Interface Board

The DC bus current interface board provides two functions. The board accepts the input signals from up to five dc bus transducers and passes these to the backplane where they can be accessed by other boards. The board also include over-current trip protection. The block diagram for the board is shown in figure A1.8

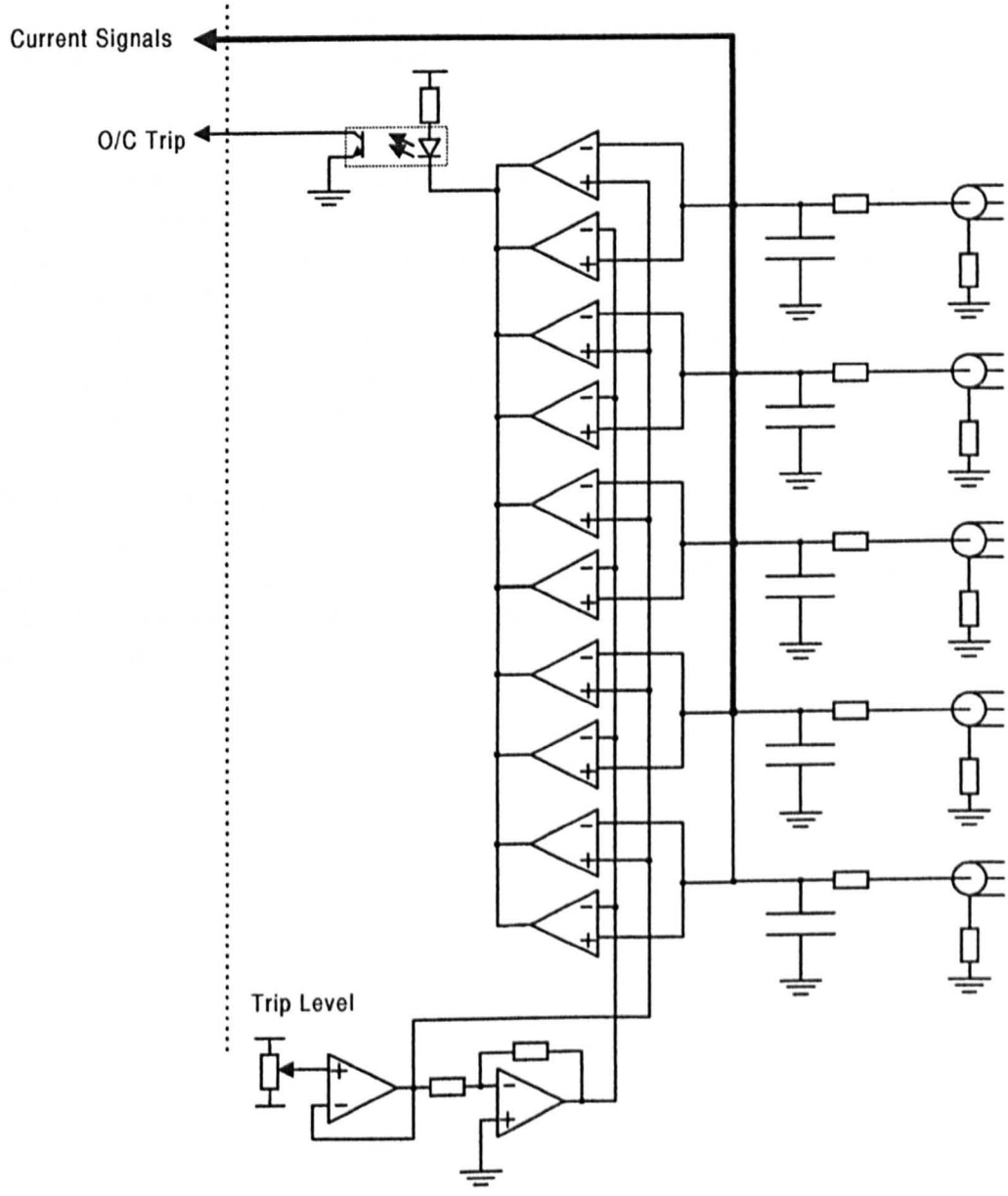

Figure A1.8 : *DC Bus current board functional block diagram*

The inputs to the board are via BNC coax connectors. Since the application is an AC drive the board is arranged to have identical positive and negative protection. The input RC is present to prevent spurious tripping, with a time constant of around 5 μs. The shield of the input BNC is connected to the board ground via a 10Ω resistor to limit circulating earth currents.

The trip detection is implemented with standard open collector comparitors operating on the ±15V supply rails. The output of these are connected together in a hard wired OR arrangement which is level shifted at the output via an opto-coupler. The trip output is passed via the backplane to the trip board.

A1.2.7 DC Bus Voltage Interface Board

A similar board to that used for input of the DC bus currents was built to monitor the DC bus voltages (the voltages on the DC link capacitors). Trip protection is simplified by only having an over-voltage fault. It common practice on a commercial drive to have the under-voltage condition as a trip. On the prototype inverters investigated during the project it is often helpful to be able to lower the DC link voltage as required, so no under-voltage protection was implemented. As the input signal was limited to being positive, the comparitors were arranged on the standard +5V rail, and therefore did not need a level shift before interfacing to trip logic.

A1.2.8 Voltage and Current Transducer Boards

Standard Boards were made up for measurement of the DC bus voltages and DC bus currents. These were simple boards that provided a mounting arrangement for the particular transducer. All the boards were fed via a daisy chain power supply.

A single board was made up for monitoring of the AC output with two current transducers and two voltage transducers. This board was added for the high performance control work that was conducted on the five level prototype.

A1.2.9 AC Current Input Board

In order for the prototype inverter to be used for vector control, an input board had to be built to take in the AC output current signals. This was one of the later boards to be built, and benefited from the experience obtained throughout the project. The functional block diagram is shown in figure A1.9.

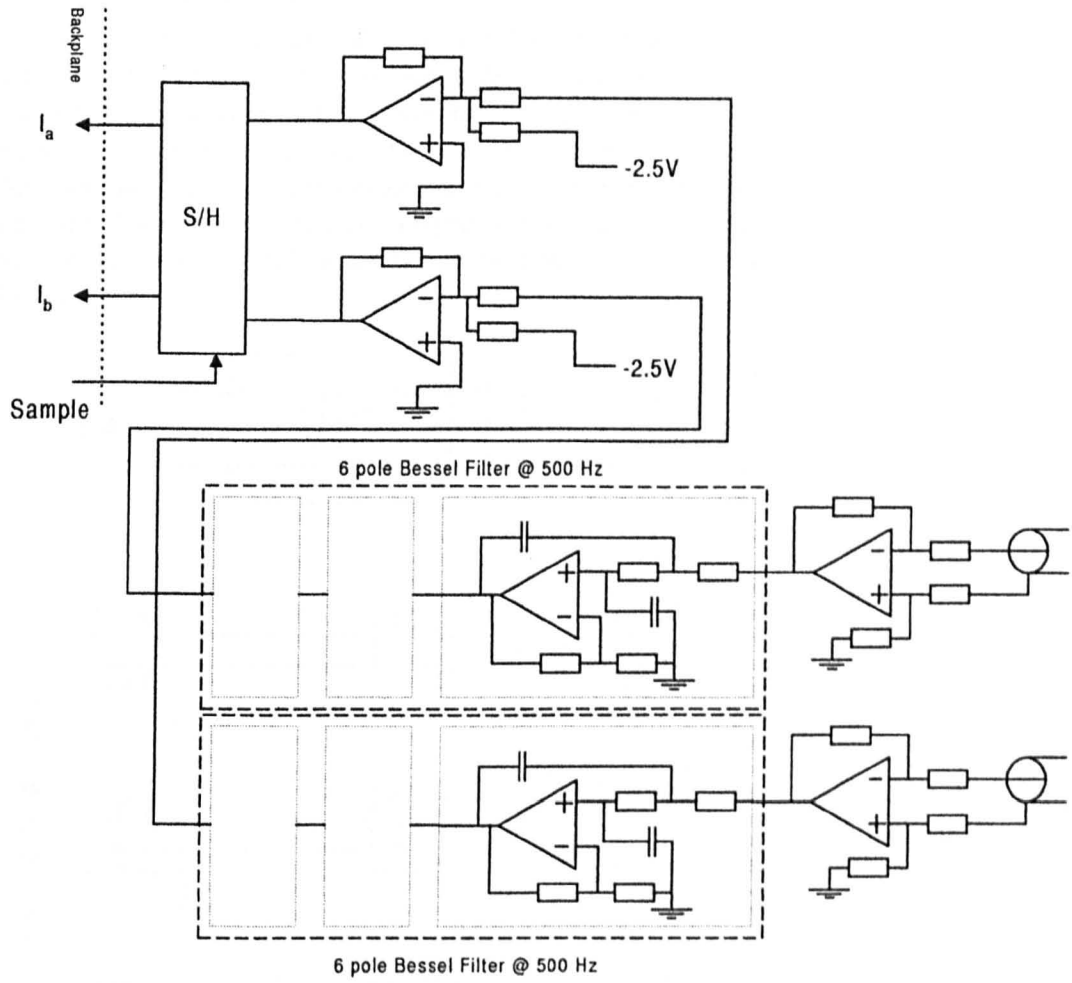

Figure A1.9 : *AC Input Board Functional Block Diagram*

The board receives input from current transducers at two BNC coax connectors. These signals are then passed through differential amplifiers. This provides the maximum de-coupling of the signals, and avoids earth loop problems. The signals are then filtered by a six pole bessel filter with a cut-off frequency of 500 Hz.

The since the inverter is operating with a switching frequency of 1 kHz, in order to achieve a high bandwidth in the current control, it is necessary to have a high pole number filter to remove switching frequency components. To maximise the response a bessel low pass filter was used since this offers approximately constant phase change throughout the pass band. The phase error in the input can be compensated for in the controller.

Once the signals have been filtered, they are offset to suit the processor analogue input, then passed to a sample and hold unit. The analogue to digital converter on the processor is limited to capturing and converting signals sequentially. With the large number of signals that needed to be converted during each cycle, it was not possible to sample all the signals within the minimum pulse width to avoid disturbance from switching. By adding a sample and hold to the individual signals, all the inputs are sampled simultaneously (triggered by a bit output from the processor) and can then be read sequentially.

A1.2.10 Speed Input Board

The motor speed is monitored by a digital incremental encoder. Incorrect isolation of the encoder can often result in corruption of the speed information. The ideal situation is to have the encoder on a independent power supply with a stage of galvanic isolation between the input signal and the processor. This was achieved by having a receiver box for the encoder that contained its own mains power supply. Here the signal was converted from differential to a current drive output as shown in figure A1.6. Interconnection from the board is via single pair twisted and screened cable. The block diagram for the interface box is shown in figure A1.10.

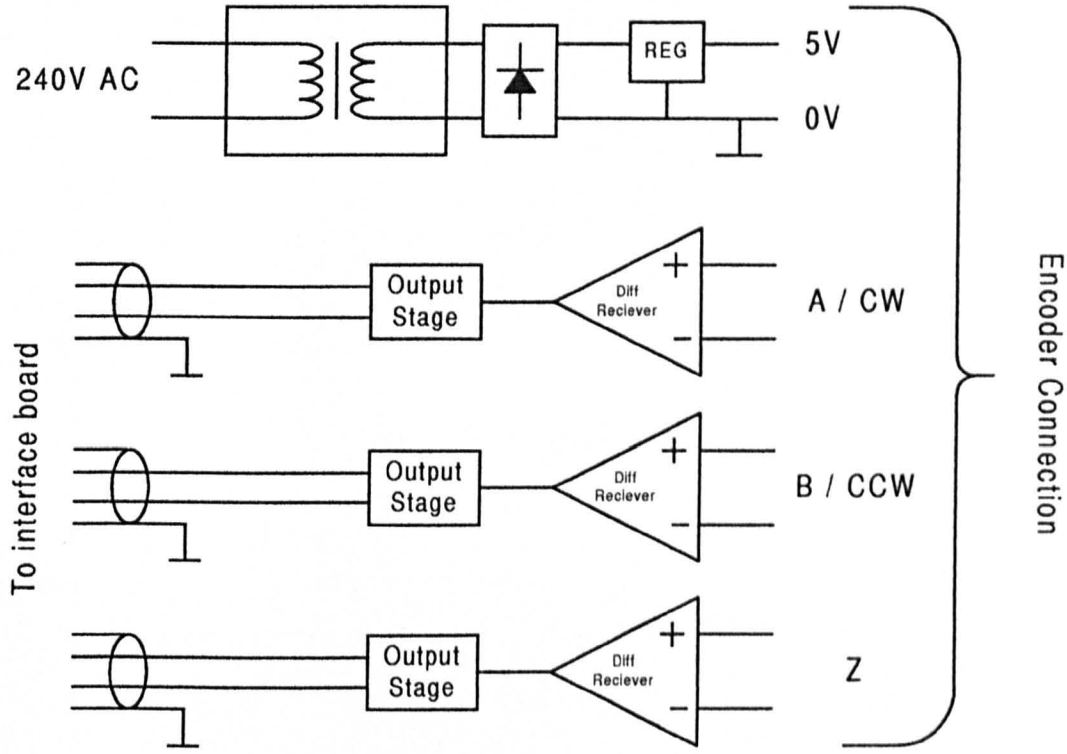

Figure A1.10 : *Encoder Interface Box*

The microcontroller includes several general purpose counter/timer blocks. Speed is measured by counting increment pulses from the encoder over a fixed sample period. The count input is software controlled to respond to either positive, negative or both edges. The direction has to be decoded and input as a up/down signal. The counter includes a reload register that can be used to provide a zero reference if position control is required. This feature was not used during the project. Two different encoders were used during the project, depending on which motor rig was in use. A 4kW as well as the standard 11kW motor rig were available. The 11kW used a standard quadrature 2500 pulse plus zero encoder. The 4kW used an encoder that produced separate signals for clockwise and counter-clockwise. Similarly the encoder produces 2500 pulses with a zero. Both encoders included differential output stages, allowing a common interface box to be used. The quadrature encoder has the advantage of producing a higher resolution when decoded and all the edges counted.

An interface board was built suitable for interfacing signals from both encoders to the processor. This is shown in figure A1.11.

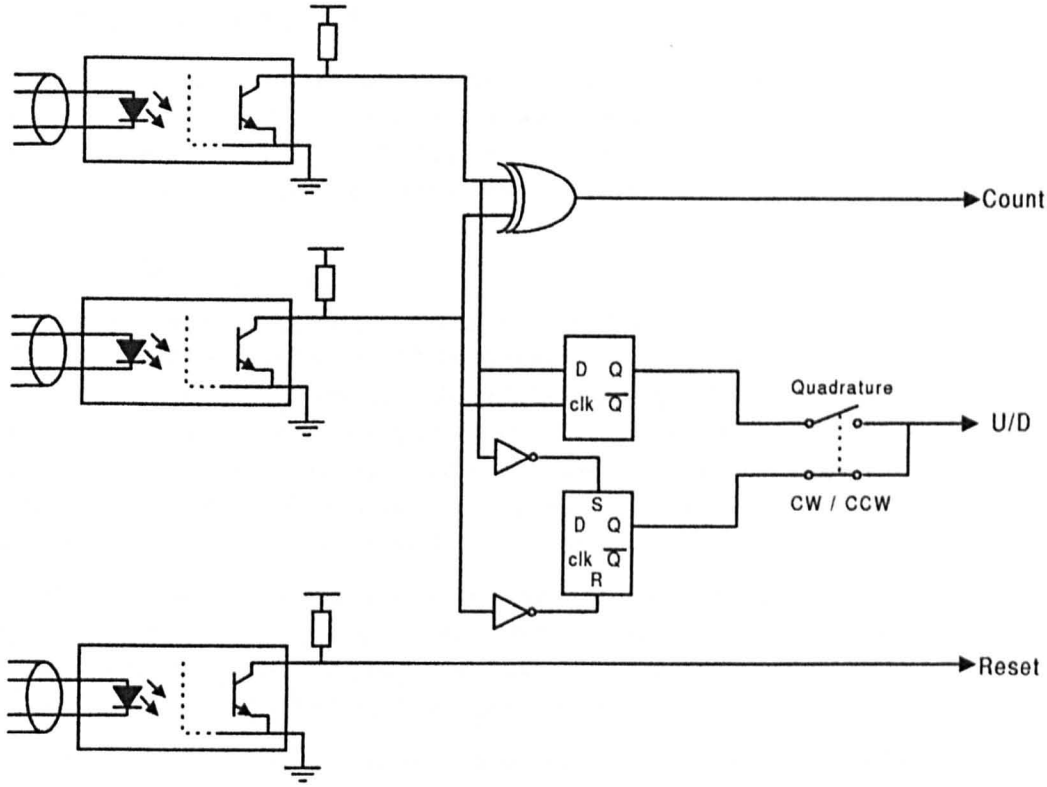

***Figure A1.11** : Speed input board block diagram*

A1.2.11 DC Link Voltage Feedback

Monitoring of DC link voltages is required in order to implement a closed loop control strategy. A board was built whilst the three level inverter prototype was being investigated. This was simply four amplifiers to scale the input obtained from the voltage interface board (section A1.2.7) and add the required offset (normally zero). The resulting signal was captured by a sample and hold unit for sampling by the processor. This board was used to implement neutral point control on the three level inverter.

A1.2.12 Balancer Interface and Neutral Point Feedback

In order to achieve voltage balancing on the DC link of the five level inverter, external switching circuits were added. This board was added to provide an interface point. With the external circuits providing balancing of the upper and lower capacitor pairs, it was not necessary to read all four capacitor voltages. The processor only needed to read the sum of the upper and lower capacitor pairs. This was done in analogue circuitry on the board, reducing the processor overhead. The circuitry for this part was a simple op-amp circuit with a sample and hold IC at the output.

Two interfacing signals were required by the balancer circuits. The first was a synchronisation pulse which locked the switching frequency to that generated by the processor. The second was an enable signal to start and stop the switching. The role of these signals will be discussed further in section A1.4. The outputs for these signals are current mirror drivers.

A1.3 Battery Backed PSU

Rather than using a standard lab PSU to power the rack, it was decided to add a battery backed unit. This would fulfil two roles. In the event of an AC power failure, the processor will detect this and turn off the IGBTs safely. Once this failure has occurred, the processor will still be running, allowing any history log to be downloaded.

A1.3.1 Circuit Design Basis

The main aim in designing the power supply was to maintain the output after a power failure. Beyond this requirement, the rest of the design was kept as simple as possible. The critical systems that needed maintaining are the processor and gate cards. These parts run from the standard +5V supply. Since the controller will trip when the power fails (an auxiliary output from the power supply to the trip board is a requirement) the ±15V rails, which are used for the analogue feedback can be left on an unsupported rail. Rectifier capacitance will maintain these rails long enough for the controller to have tripped.

Without AC power the output will be supported by a sealed lead acid battery. The battery being recharged whilst the AC power is present. Standard batteries are made for this kind of application, being suitable for long term trickle charging on a constant voltage supply. The charging current should be limited however for protection.

Interlock will be included so that the output can only be turned on when the AC power is present.

A1.3.2 Design Detail

A basic schematic for the circuit is shown in figure A1.12.

The input supply is standard 240V single phase AC. Toroidal transformers are used in the PSU to provide isolated LV supplies. One transformer feeds the ±15V output circuit, which consists of a simple capacitor smoothed rectifier and linear regulators. The second transformer feeds the battery support system. From this there are four 5V regulators.

The power supply is turned on by pressing the momentary action 'ON' button. This bypasses the input relay and energises the transformer. The internal power rails within the PSU rapidly rise to their normal operating voltage, and the two relays turn on. Turning on RL1 feeds the PSU once the 'ON' button has been released. The PSU is turned off by pressing the momentary action 'OFF' button that releases the relays, cutting the power. Turning of RL2 in this way disconnects the battery circuit.

In the event of an AC power failure the output voltage from the second transformer rectifier will begin to drop rapidly. Once this falls below the battery voltage the diodes will allow the battery to feed the output. The diodes are arranged so that the battery can be charged independantly of the output when the supply is healthy and to allow changeover without loss of output. If the AC power returns whilst the PSU is still active this will take over and begin to charge the battery again.

The 5V output regulators are simple switching regulators. These provide the regulated output voltage from the supported power rail with a high efficiency. This maximises the operating time available when running on the battery.

Supply status is passed to the trip board from a relay on the AC input.

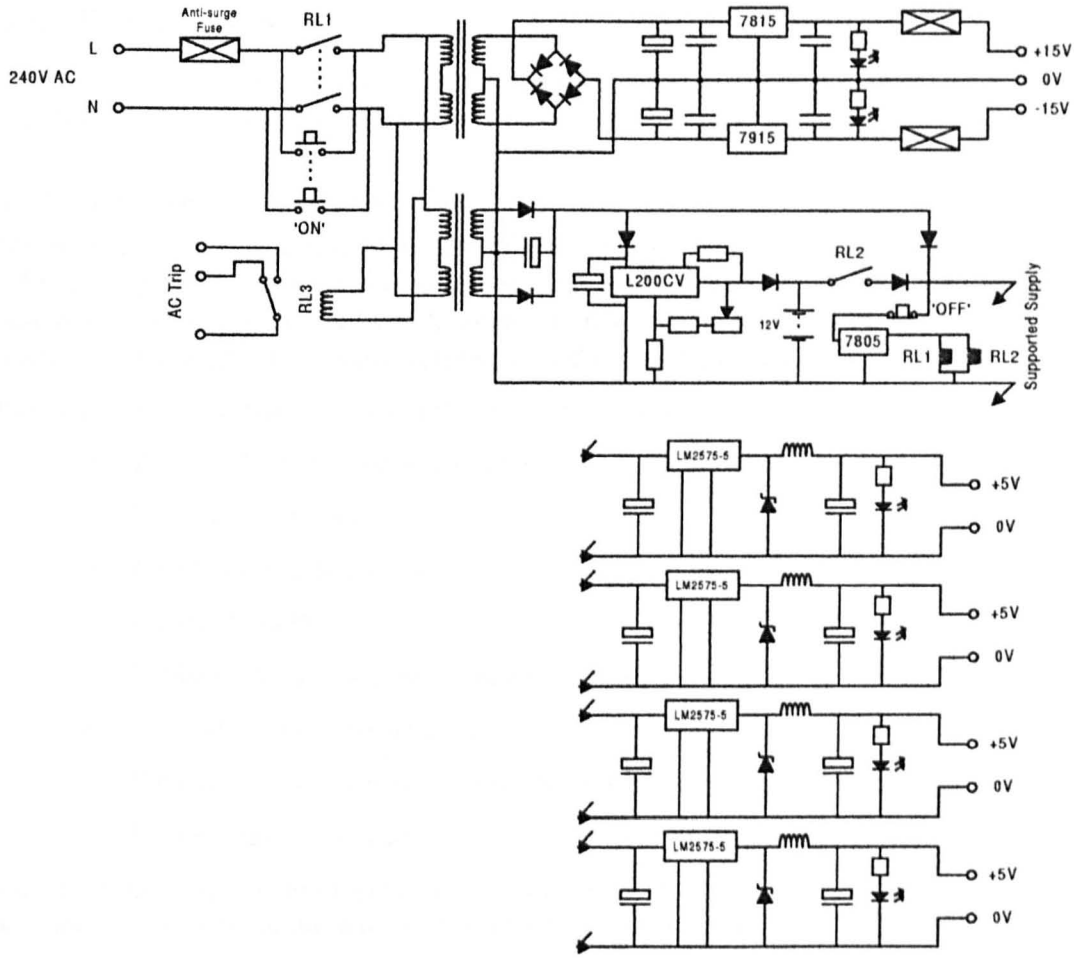

Figure A1.12 : *Battery Backed PSU*

A1.4 Balancer Units

The balancer units described in chapter 5 (see section 4) required the most complex control boards of any part of the inverter system. This section will describe the design.

A1.4.1 Balancer Operation Overview

The balancers were designed to be virtually stand alone units, just needing the minimum reference signals from the main processor rack. They were therefore designed around a standard heatsink module onto which would be mounted the power electronics and control boards. A photograph of a completed balancer is shown in figure 5.17.

The balancer control boards have to fulfil a number of roles.

1. Read in DC link voltages and currents
2. Voltage loop PI control
3. Measure inductor current
4. Current loop PI
5. Produce PWM synchronised to the processor
6. Provide voltage error protection
7. Provide current protection of the inductor
8. Produce gate drive outputs

The resulting design to meet these requirements is a combination of digital and analogue circuitry. An overview of the general arrangement is shown in figure A1.13.

The arrangement includes a special PSU box. This contains a toroidal transformer and two rectifiers with large smoothing capacitors. The two outputs are completely isolated. The balancer PSU is fed from the same supply as the battery backed control rack PSU. In the event of supply failure occurring the capacitors will maintain the balancer control board long enough for the trip signal to disable the outputs.

The analogue inputs are through connected so that the signals from the transducers can be connected to the input boards in the rack as normal.

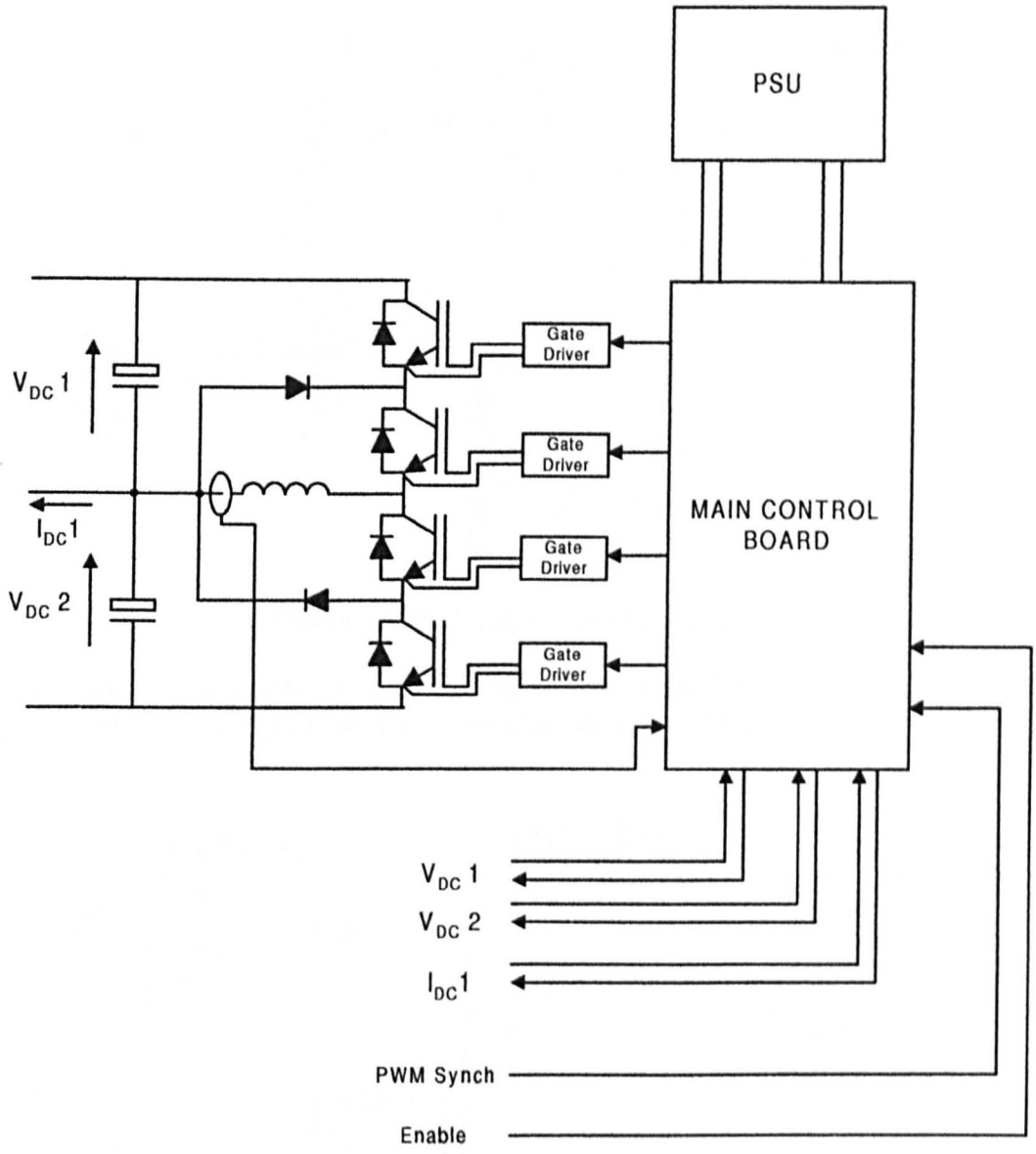

***Figure A1.13** : Balancer Arrangement*

A1.4.2 Main Control Board

The description of the control board will be split down into the basic sections. These are the voltage controller, current controller, PWM generator, Trip generation, trip integration and enable logic and the power supplies.

The voltage control is implemented via a conventional op-amp circuit. This is shown in figure A1.14. The inputs are via differential amplifiers to provide ground impedance. The feedback network for the actual PI amplifier were mounted on a DIL component header. This allows modifications to be made. Presets are often placed in series with resistors to allow signal gains to be trimmed. The points A and B provide signals to the trip circuits.

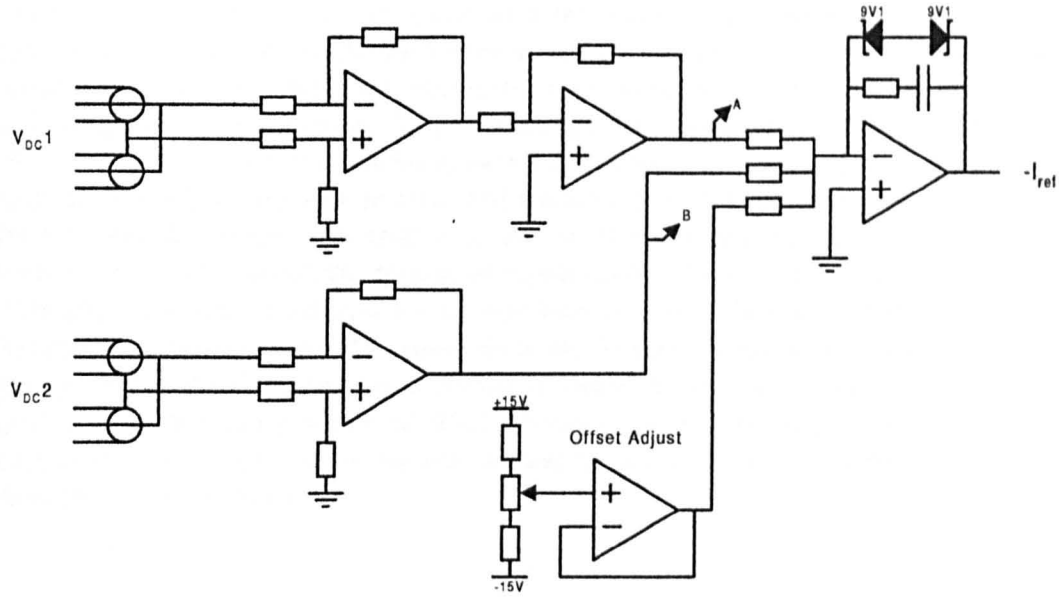

Figure A1.14 : *Voltage Controller Circuit*

A very similar arrangement is used for the current controller. Again the controller is implemented as an op-amp circuit. The circuit is shown in figure A1.15.

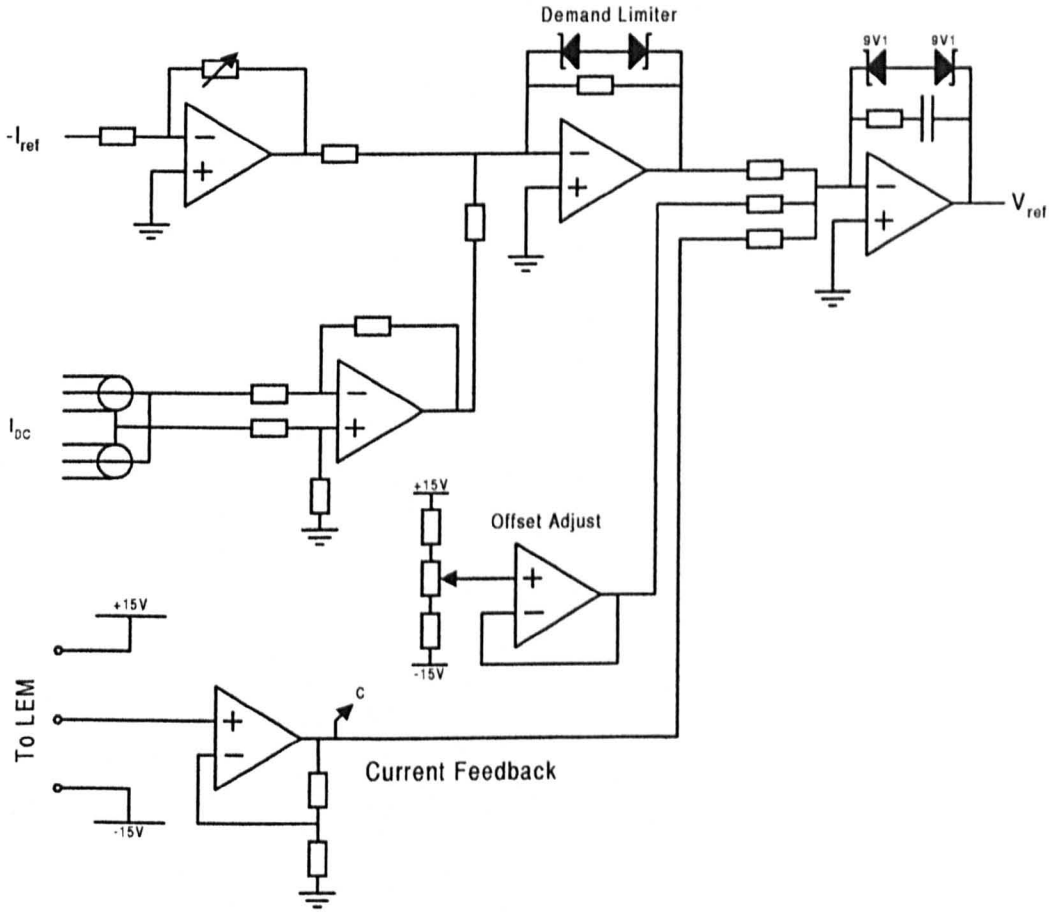

Figure A1.15 : *Current Controller Circuit*

The PWM generator is key to the operation of the circuit. The technique follows the classical generation technique by comparing references against a triangle wave. In order to keep signal sampling away from switching transients it is preferable to synchronise the balancer switching cycle to the processor. A synchronising pulse from the processor is used to toggle a JK flip-flop. This controls an analogue switch on the input of an integrator. By switching the integration reference between positive and negative references a triangle wave is produced. By trimming the integrator to saturate at the end of a half period (saturation defined by the back to back diodes across the integration capacitor) then the triangle wave will be protected from integrator drift. In this case the triangle wave is ±10V. The selection of op-amp for this integrator is important since the output skew rate is very important in this application. The circuit for the PWM generation is shown in figure A1.16. The actual pulse patterns are generated by comparing a pair of offset references against the triangle wave. The offsets control the time spent in the current circulation states for safe commutation. This was described in section 5.4.3.

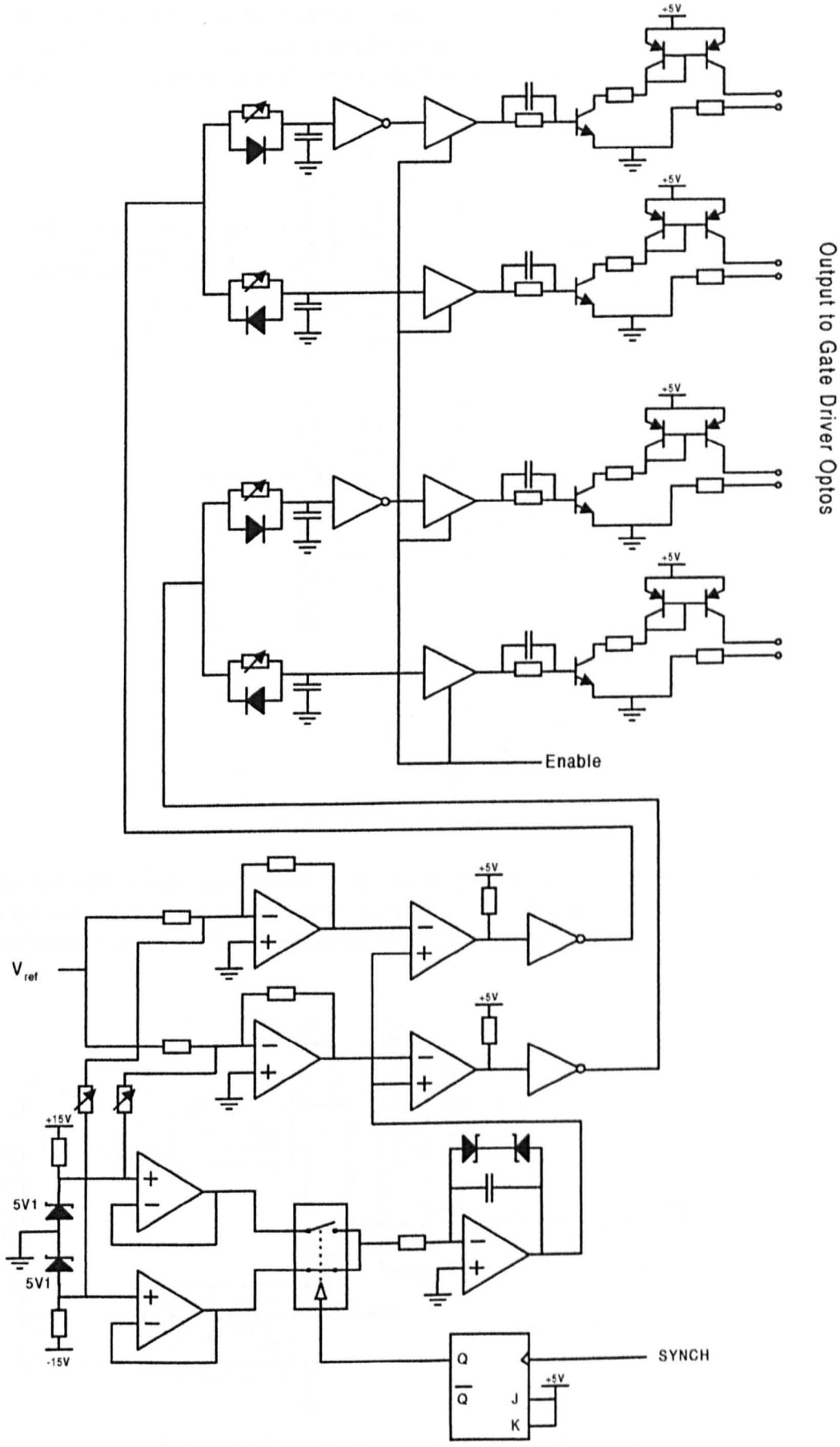

Figure A1.16 : *PWM Generation Circuit*

Protection is provided for the inductor current (point C) and the difference in voltage on the two capacitors (points A,B). These conditions produce a local trip on the balancer. The trip latches are automatically cleared at power up. The trip circuits are shown in figure A1.17.

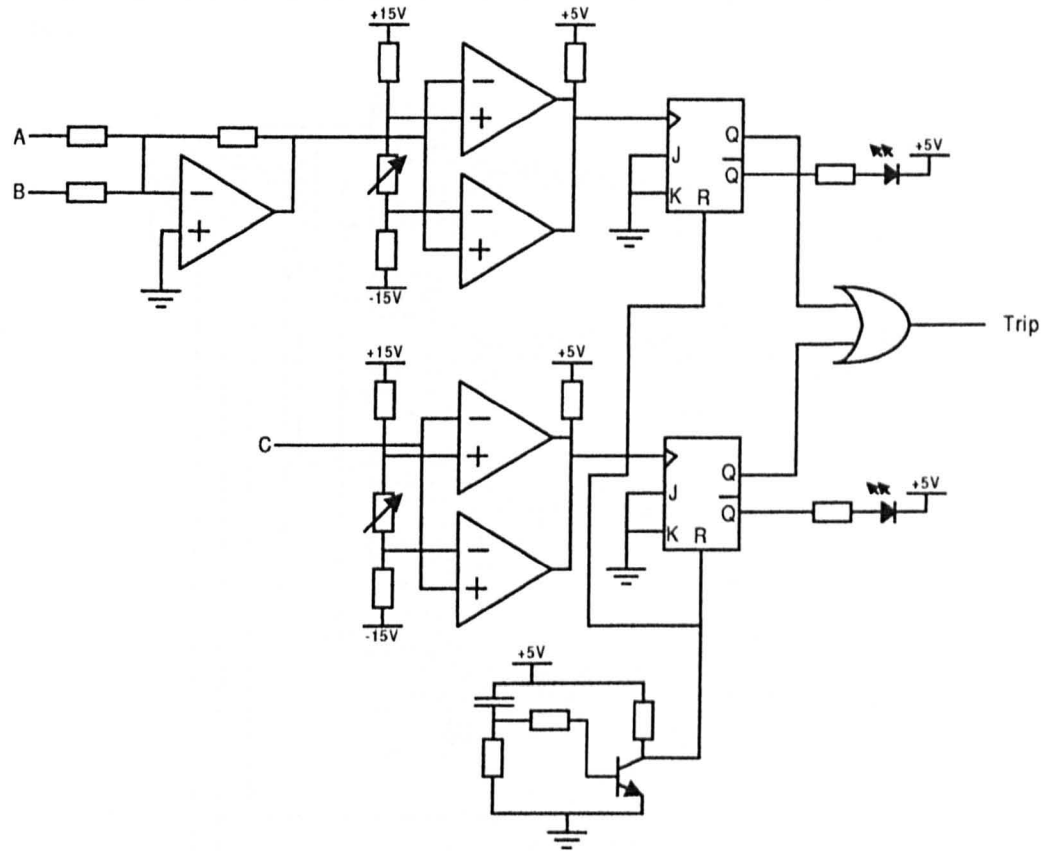

***Figure A1.17** : Protection Circuit*

The on board trips are integrated with the incoming enable signal to control the output signals to the gate drivers. To ensure correct start up the outputs are only enabled with the first synchronisation pulse. The circuit for this is shown in figure A1.18.

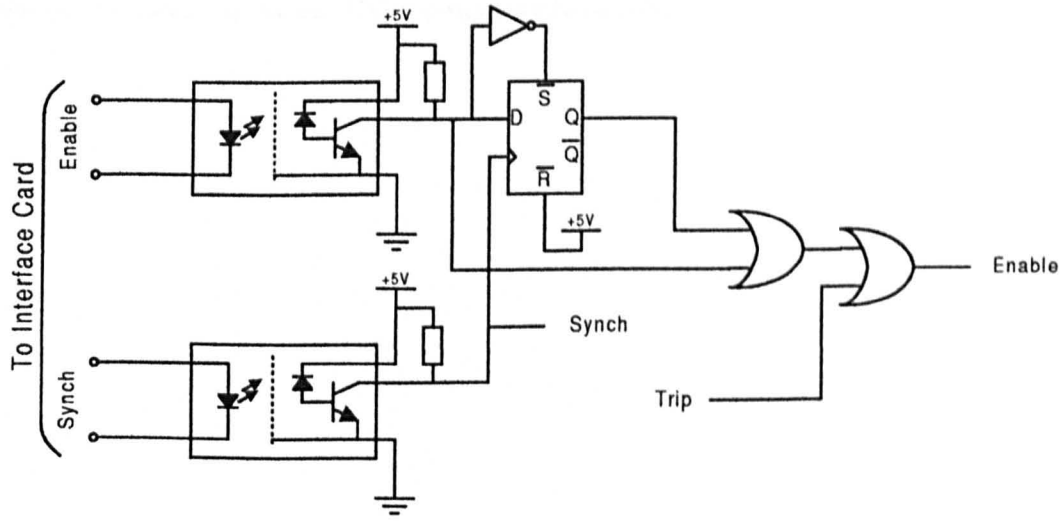

***Figure A1.18** : Trip Integration and Enable Logic Circuit*

A1.4.3 Gate Board and Current Feedback

The second board for the balancer, which is mounted on the back of the unit provides support for four gate driver boards, with their associated isolation power supplies, and a current transducer for feedback of the inductor current. A block diagram of the board is shown in figure A1.19.

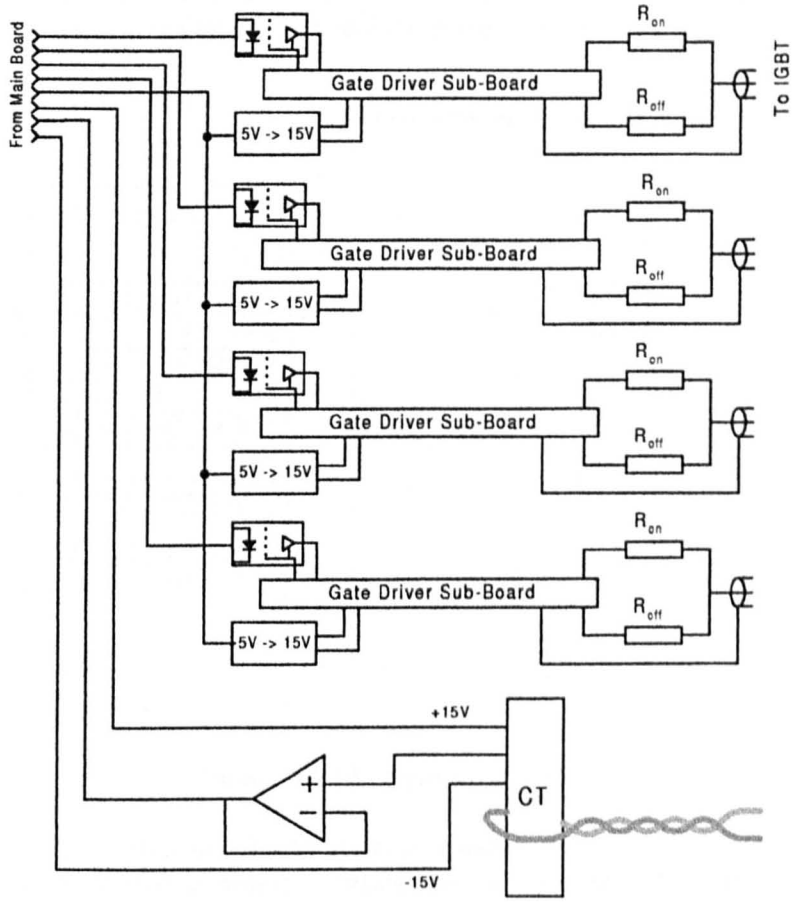

Figure A1.19 : *Gate and feedback board block diagram*

Connections to the IGBTs are made by short lengths of coaxial cable. The interconnection to the main board is via 16 way IDC terminated ribbon cable.

A1.5 Software Methodology

An overview diagram of the software is shown in figure A1.20. The software for controlling the drive is written in C and compiled for downloading to the processor. There are essential two parallel tasks in operation on the processor. As with any C program the top level task is the 'main()' function. This is the controlling level that communicates to the user via a serial link, and activates the PWM. The PWM is generated by a background function called 'PWM_routine()'. This function is executed in response to an interrupt from an internal timer.

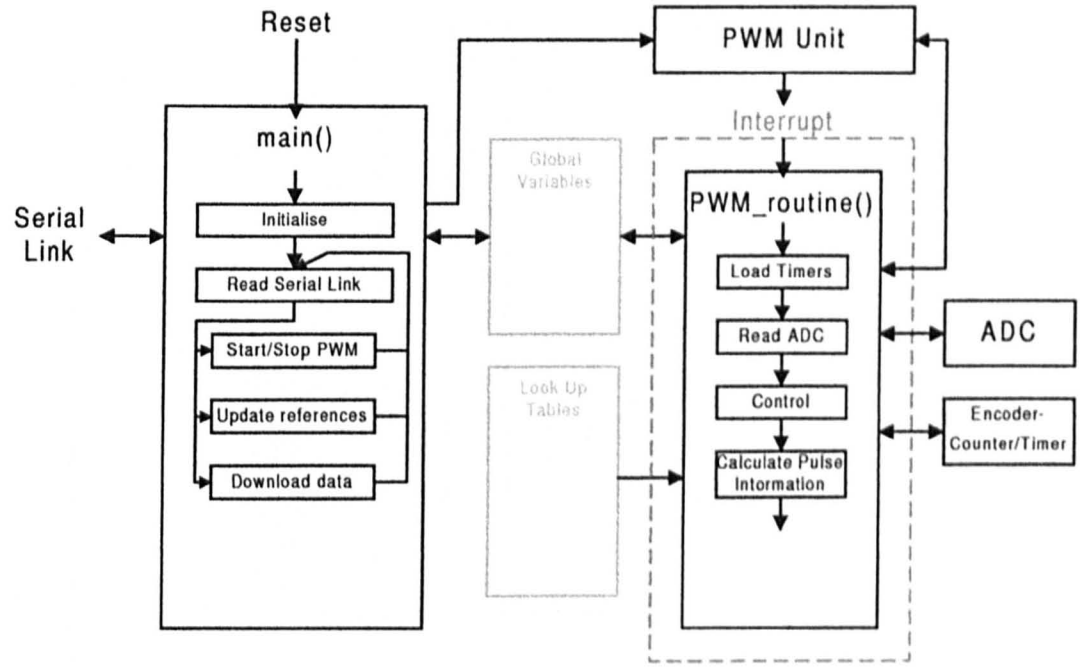

***Figure A1.20** : Software Overview*

Once the interrupt occurs this function takes control, and the execution of 'main()' is suspended. The PWM routine timing is critical, and as such takes the highest priority level. Because of this the serial communications has been left open loop. The bandwidth of the serial link was not a concern, so an open loop technique is quite satisfactory. Since the PWM routine is called in response to an interrupt it can neither accept nor return variables. Because of this it is necessary to pass all data required by the routine in the form of global variables.

All the software associated with control strategies and pulse time calculation is included within the single function. Function calls to other functions have been reduced where possible to keep execution time to a minimum.

Each time the interrupt routine is called the PWM timers are loaded with a set of values that were calculated during the previous cycle. This is the first task the routine has in order that all the timers are loaded within the minimum pulse gap (where no switching occurs). The routine can then begin the process of calculating the switching times for the next cycle.

Complex mathematical functions are generated by the use of look-up tables. The three level inverter control did not require many complex tables, so the tables were built by software routines. For the five level inverter however, where the control was more complex (including vector control) the tables were built up on the PC and included as constants in the final sotware.

A1.6 Software Listings

Software listings have been included for reference. These are the versions used on the final three level and five level prototype inverters.

A1.6.1 Software for the Three Level Inverter

```
/*-------------------------------------------------------------------------
-
-
    3 LEVEL INVERTER DRIVE PROGRAM : BASIC OPEN LOOP V/F DRIVE
-
-
    Re-route of pwm signals and fix half modulation max
-
-------------------------------------------------------------------------*/

#pragma debug
#pragma code

#include <stdio.h>
#include <math.h>
#include <reg166.h>
#include <intrins.h>

/*-------------------------- DEFINITIONS ----------------------------*/

#define PWM_HALF_PERIOD 1250   // To give 1 khz Asymmetric 2kHz LOOP
#define PI 3.141592654
#define WDGO 0
#define WDRST 1

/*------------------  BIT ACCESS DEFINITIONS ----------------------*/

sbit OUT1A=P2^0;
sbit OUT1B=P2^1;
sbit OUT1C=P2^2;
sbit OUT1D=P2^3;
sbit OUT2A=P2^4;
sbit OUT2B=P2^5;
sbit OUT2C=P2^6;
sbit OUT2D=P2^7;
sbit OUT3A=P2^8;
sbit OUT3B=P2^9;
sbit OUT3C=P2^10;
sbit OUT3D=P2^11;
sbit ENABLE=P2^12;              // ACTIVE LOW SIGNAL!!
sbit WATCHDOG=P2^13;
sbit SYNCH=P2^14;


/*---------------------- GLOBAL VARIABLES  -------------------------*/


int idata rise_fall;    // indicate rising or falling for asymmetric PWM
                          // 1 = rise, 0 = fall.

unsigned char sine_array[500];         // Sine table 0 - 90 degrees

int data_array[5][500];         // Array for storing data

int idata PWM_times[12];

int idata AD_offset[10];                // A/D Converter Offsets

int idata PWM_angle;                    // PWM reference angle
int idata fdemand;                      // Frequency Demand set by user
int idata fstep;                        // Controls actual frequency
int idata mag;                          // Controls magnetude/modulation
int idata ramp_u;                         // Controls the ramp rate
int idata ramp_d;
int idata loop;                         // Controls the control loop
int idata v_over_f;                     // V/f ratio variable 0-10

int idata slow_control;                 // time variable for slow control

int idata neutral_point_error;          // Error voltage for neutral point

int idata capture_count;                // counter for data capture
int idata capture_period;

int idata npc_output;                   // output of neutral point control

int idata parameter[50];                // parameter values
/*
```

```
                Parameter No    Value

                0               Data Capture Sample period
                1               Neutral Point Control nth multiplier
                2               """ n-1th multiplier
                3               """ divisor
                4               Neutral Point Offset Demand
                5               Neutral Point Control Active
                6               Neutral Point sample freq divider
                7               voltage boost minimum limit
                8               deceleration limiter
                9
                10              balancer test active
                11               balancer test amplitude
*/

char *channel_name[5]=
{
     "Vcap1",
     "Vcap2",
     "NPC output",
     "Frequency",
     "NULL"
};


/*------------------------  FUNCTIONS  -----------------------------*/


void set_comms(void)            /* Sets up for the front end */
{
        P3|=0x0400;
        DP3|=0x0400;
        DP3&=0xf7ff;

        P3 |= 0x0100;
        DP3 |=0x0100;
        DP3 &=0xFDFF;
        S1TIC =0x80;
        S1RIC =0x00;
        S1BG  =0x40;
        S1CON = 0x8011;
}

void configure_PWM(void)
{
        T0IC=0x77;      // level 13, group 3, interrupt enabled
        T01CON=0x0000;  // 2.5 Mhz Counter Mode
        T0REL=-PWM_HALF_PERIOD;
        T0=-PWM_HALF_PERIOD;
        P2=0x0000;
        ENABLE=1;
        WATCHDOG=WDRST; // Start in Reset State
        SYNCH=1;
        DP2=0xFFFF;     // set up outputs

        CCM0=0x5555;
        CCM1=0x5555;
        CCM2=0x5555;    // set to mode 1 compare

        CC0IE=0;        // Turn of compare interrupts
        CC1IE=0;
        CC2IE=0;
        CC3IE=0;
        CC4IE=0;
        CC5IE=0;
        CC6IE=0;
        CC7IE=0;
        CC8IE=0;
        CC9IE=0;
        CC10IE=0;
        CC11IE=0;

        mag=0;
        fstep=0;
        PWM_angle=0;

}

void initialise_parameters(void)
{
        ramp_u=200;
        ramp_d=200;
        v_over_f=10;

        parameter[0]=0;
        parameter[1]=100;
        parameter[2]=40;
        parameter[3]=20;
        parameter[4]=0;
        parameter[5]=0;
        parameter[6]=5;
        parameter[7]=2;
        parameter[8]=3;
        parameter[10]=0;
        parameter[11]=20;
}

void generate_sine_array(void)
{
    int i;
```

```
    for (i=0; i<500; i++)
sine_array[i]=255*(sin(PI*i/1000)+(sin(3*PI*i/1000)/9.0));
}

int int_sine(int angle)
{
   int quadrant;
   int relative;

   quadrant=angle/500;
   relative=angle%500;

   switch (quadrant)
   {
      case 0:
         return sine_array[relative];
      case 1:
         return sine_array[499-relative];
      case 2:
         return -sine_array[relative];
      case 3:
         return -sine_array[499-relative];
   }
   return 0;
}

void start_PWM(void)
{

   PWM_times[0]=0;
   PWM_times[1]=0;
   PWM_times[2]=0;
   PWM_times[3]=0;
   PWM_times[4]=0;
   PWM_times[5]=0;
   PWM_times[6]=0;
   PWM_times[7]=0;
   PWM_times[8]=0;
   PWM_times[9]=0;
   PWM_times[10]=0;
   PWM_times[11]=0;

   CC0=0;
   CC1=0;
   CC2=0;
   CC3=0;
   CC4=0;
   CC5=0;
   CC6=0;
   CC7=0;
   CC8=0;
   CC9=0;
   CC10=0;
   CC11=0;

   OUT1A=0;
   OUT1B=0;
   OUT1C=0;
   OUT1D=0;
   OUT2A=0;
   OUT2B=0;
   OUT2C=0;
   OUT2D=0;
   OUT3A=0;
   OUT3B=0;
   OUT3C=0;
   OUT3D=0;

   rise_fall=1;
   PWM_angle=0;
   fstep=0;              // Start at zero speed
   loop=0;
   npc_output=0;
   neutral_point_error=0;
   slow_control=parameter[6]-2;

   T0=-PWM_HALF_PERIOD;
   T0R=1;        // Start PWM timer
   ENABLE=0;
   WATCHDOG=WDGO;
   SYNCH=1;
   capture_count=0;
   capture_period=0;

}

void stop_PWM(void)
{
    T0R=0;       // Stop PWM timer
    ENABLE=1;
    WATCHDOG=WDRST;

    OUT1A=0;
    OUT1B=0;
    OUT1C=0;
    OUT1D=0;
    OUT2A=0;
    OUT2B=0;
    OUT2C=0;
    OUT2D=0;
    OUT3A=0;
    OUT3B=0;
    OUT3C=0;
    OUT3D=0;
```

```
    SYNCH=1;

}

/*-------------------------  INTERRUPT FUNCTIONS  --------------------*/

void PWM_routine(void) interrupt 0x20 using PWM_registers
{

  int mod_wave_value[3];
  int phase_angle[3];
  int times[4];
  int level;
  int voltages[2];
  int temp;


  WATCHDOG=WDRST;
  SYNCH=0;

  // load timers with values as calculated in last half cycle

  CC0=PWM_times[0];
  CC1=PWM_times[1];
  CC2=PWM_times[2];
  CC3=PWM_times[3];
  CC4=PWM_times[4];
  CC5=PWM_times[5];
  CC6=PWM_times[0];
  CC7=PWM_times[1];
  CC8=PWM_times[2];
  CC9=PWM_times[3];
  CC10=PWM_times[4];
  CC11=PWM_times[5];

  WATCHDOG=WDGO;
  SYNCH=1;

  ADCON=8;
  ADST=1;

  while(ADBSY==1)
  {
  _nop_();  //DELAY
  }
  ADCON=7;
  ADST=1;
  voltages[0]=ADDAT;
  voltages[0]&=0x03FF;
  voltages[0]=voltages[0]-AD_offset[8];

  while(ADBSY==1)
  {
  _nop_();  //DELAY
  }
  voltages[1]=ADDAT;
  voltages[1]&=0x03FF;
  voltages[1]=voltages[1]-AD_offset[7];


  if (parameter[10]>0)
  {
    parameter[10]++;

    if (parameter[10]<8000) parameter[4]=parameter[11];
    else if(parameter[10]>16000)
    {
      parameter[4]=0;
      parameter[10]=0;
    }
    else parameter[4]=-parameter[11];
  }



  // Control Stage
  slow_control++;
  if (slow_control==parameter[6])
  {
   temp=-parameter[2]*neutral_point_error;
   neutral_point_error=voltages[1]-voltages[0]-parameter[4];
   temp=parameter[1]*neutral_point_error;
   temp=temp/parameter[3];
   npc_output=npc_output+temp;
   slow_control=0;
  }

  if (npc_output>250) npc_output=250;
  if (npc_output<-250) npc_output=-250;
  if (parameter[5]!=0) npc_output=0;

  if (((fdemand>fstep)&&(fstep>=0))||((fdemand<fstep)&&(fstep<=0)))
  {
    if(loop>=ramp_u)
    {
      if(fdemand>fstep)fstep++;
      else fstep--;
      loop=0;
    }
    else
    {
      loop++;
```

```
  }
}
else if (((fdemand<fstep)&&(fstep>0))||((fdemand>fstep)&&(fstep<0)))
{
  if(loop>=ramp_d)
  {
    if (fdemand>fstep) fstep++;
    else fstep--;
    loop=0;
  }
  else
  {
    loop++;
  }
}
else
{
loop=0;
}

if (fstep>500) fstep=500;
if (fstep<-500) fstep=-500;
mag=fstep*v_over_f/51;
if (mag<0) mag=-mag;
if (mag<parameter[7]) mag=parameter[7];
if (mag>98) mag=98;

// Calculate switching times

phase_angle[0]=PWM_angle;

phase_angle[1]=PWM_angle-6666;
if (phase_angle[1]<0) phase_angle[1]=phase_angle[1]+20000;

phase_angle[2]=PWM_angle-13333;
if (phase_angle[2]<0) phase_angle[2]=phase_angle[2]+20000;

mod_wave_value[0]=(mag*int_sine(phase_angle[0]/10)/20)+npc_output;
mod_wave_value[1]=(mag*int_sine(phase_angle[1]/10)/20)+npc_output;
mod_wave_value[2]=(mag*int_sine(phase_angle[2]/10)/20)+npc_output;

// Phase 1 calculation

if (mod_wave_value[0]>-1)
{
    times[0]=mod_wave_value[0];
    times[1]=1250;
}
else if (mod_wave_value[0]<0)
{
    times[0]=0;
    times[1]=1250+mod_wave_value[0];
}


if (rise_fall==0)
{      // Falling Edge

        if (times[0]>24 && times[0]<1225 && CC0!=0)
        {
            PWM_times[0]=-PWM_HALF_PERIOD+times[0];
        }
        else if (times[0]<25 && CC0!=0 )
        {
            PWM_times[0]=-1224;
        }
        else if (times[0]<25 && CC0==0)
        {
            PWM_times[0]=0;
        }
        else if (times[0]>24 && times[0]<1225 && CC0==0)
        {
            PWM_times[0]=-PWM_HALF_PERIOD+times[0];
            CC0=-25;
        }
        else if (times[0]>1224)
        {
            PWM_times[0]=1;
        }

        if (times[1]>24 && times[1]<1225 && CC1!=0)
        {
            PWM_times[1]=-PWM_HALF_PERIOD+times[1];
        }
        else if (times[1]<25 && CC1!=0 )
        {
            PWM_times[1]=-1224;
        }
        else if (times[1]<25 && CC1==0)
        {
            PWM_times[1]=0;
        }
        else if (times[1]>24 && times[1]<1225 && CC1==0)
        {
            PWM_times[1]=-PWM_HALF_PERIOD+times[1];
            CC1=-25;
        }
        else if (times[1]>1224)
        {
            PWM_times[1]=1;
        }

}
else          // Rising Edge
```

```
{
        if (times[0]>24 && times[0]<1225 && CC0!=1)
        {
            PWM_times[0]=-times[0];
        }
        else if (times[0]>1224 && CC0!=1 )
        {
            PWM_times[0]=-1224;
        }
        else if (times[0]>1224 && CC0==1)
        {
            PWM_times[0]=1;
        }
        else if (times[0]>24 && times[0]<1225 && CC0==1)
        {
            PWM_times[0]=-times[0];
            CC0=-25;
        }
        else if (times[0]<25)
        {
            PWM_times[0]=0;
        }

        if (times[1]>24 && times[1]<1225 && CC1!=1)
        {
            PWM_times[1]=-times[1];
        }
        else if (times[1]>1224 && CC1!=1 )
        {
            PWM_times[1]=-1224;
        }
        else if (times[1]>1224 && CC1==1)
        {
            PWM_times[1]=1;
        }
        else if (times[1]>24 && times[1]<1225 && CC1==1)
        {
            PWM_times[1]=-times[1];
            CC1=-25;
        }
        else if (times[1]<25)
        {
            PWM_times[1]=0;
        }

}// END OF RISE FALL CONDITION

// END OF PHASE 1 CALCULATION

// PHASE 2 CALCULATION

if (mod_wave_value[1]>-1 )
{
    times[0]=mod_wave_value[1];
    times[1]=1250;

}
else if ( mod_wave_value[1]<0)
{
    times[0]=0;
    times[1]=1250+mod_wave_value[1];
}

if (rise_fall==0)
{       // Falling Edge

        if (times[0]>24 && times[0]<1225 && CC2!=0)
        {
            PWM_times[2]=-PWM_HALF_PERIOD+times[0];
        }
        else if (times[0]<25 && CC2!=0)
        {
            PWM_times[2]=-1224;
        }
        else if (times[0]<25 && CC2==0)
        {
            PWM_times[2]=0;
        }
        else if (times[0]>24 && times[0]<1225 && CC2==0)
        {
            PWM_times[2]=-PWM_HALF_PERIOD+times[0];
            CC2=-25;
        }
        else if (times[0]>1224)
        {
            PWM_times[2]=1;
        }

        if (times[1]>24 && times[1]<1225 && CC3!=0)
        {
            PWM_times[3]=-PWM_HALF_PERIOD+times[1];
        }
        else if (times[1]<25 && CC3!=0)
        {
            PWM_times[3]=-1224;
        }
        else if (times[1]<25 && CC3==0)
        {
            PWM_times[3]=0;
        }
        else if (times[1]>24 && times[1]<1225 && CC3==0)
        {
            PWM_times[3]=-PWM_HALF_PERIOD+times[1];
            CC3=-25;
```

```
        }
        else if (times[1]>1224)
        {
            PWM_times[3]=1;
        }


}
else          // Rising Edge
{
        if (times[0]>24 && times[0]<1225 && CC2!=1)
        {
            PWM_times[2]=-times[0];
        }
        else if (times[0]>1224 && CC2!=1)
        {
            PWM_times[2]=-1224;
        }
        else if (times[0]>1224 && CC2==1)
        {
            PWM_times[2]=1;
        }
        else if (times[0]>24 && times[0]<1225 && CC2==1)
        {
            PWM_times[2]=-times[0];
            CC2=-25;
        }
        else if (times[0]<25)
        {
            PWM_times[2]=0;
        }

        if (times[1]>24 && times[1]<1225 && CC3!=1)
        {
            PWM_times[3]=-times[1];
        }
        else if (times[1]>1224 && CC3!=1)
        {
            PWM_times[3]=-1224;
        }
        else if (times[1]>1224 && CC3==1)
        {
            PWM_times[3]=1;
        }
        else if (times[1]>24 && times[1]<1225 && CC3==1)
        {
            PWM_times[3]=-times[1];
            CC3=-25;
        }
        else if (times[1]<25)
        {
            PWM_times[3]=0;
        }
```

```
        }

}// END OF RISE FALL CONDITION

// END OF PHASE 2 CALCULATION

// PHASE 3 CALCULATION
if (mod_wave_value[2]>-1)
{

    times[0]=mod_wave_value[2];
    times[1]=1250;
}
else if (mod_wave_value[2]<0)
{
    times[0]=0;
    times[1]=1250+mod_wave_value[2];
}

if (rise_fall==0)
{       // Falling Edge

        if (times[0]>24 && times[0]<1225 && CC4!=0)
        {
            PWM_times[4]=-PWM_HALF_PERIOD+times[0];
        }
        else if (times[0]<25 && CC4!=0)
        {
            PWM_times[4]=-1224;
        }
        else if (times[0]<25 && CC4==0)
        {
            PWM_times[4]=0;
        }
        else if (times[0]>24 && times[0]<1225 && CC4==0)
        {
            PWM_times[4]=-PWM_HALF_PERIOD+times[0];
            CC4=-25;
        }
        else if (times[0]>1224)
        {
            PWM_times[4]=1;
        }

        if (times[1]>24 && times[1]<1225 && CC5!=0)
        {
            PWM_times[5]=-PWM_HALF_PERIOD+times[1];
        }
        else if (times[1]<25 && CC5!=0)
        {
            PWM_times[5]=-1224;
        }
```

```
        else if (times[1]<25 && CC5==0)
        {
            PWM_times[5]=0;
        }
        else if (times[1]>24 && times[1]<1225 && CC5==0)
        {
            PWM_times[5]=-PWM_HALF_PERIOD+times[1];
            CC5=-25;
        }
        else if (times[1]>1224)
        {
            PWM_times[5]=1;
        }

}
else          // Rising Edge
{
        if (times[0]>24 && times[0]<1225 && CC4!=1)
        {
            PWM_times[4]=-times[0];
        }
        else if (times[0]>1224 && CC4!=1)
        {
            PWM_times[4]=-1224;
        }
        else if (times[0]>1224 && CC4==1)
        {
            PWM_times[4]=1;
        }
        else if (times[0]>24 && times[0]<1225 && CC4==1)
        {
            PWM_times[4]=-times[0];
            CC4=-25;
        }
        else if (times[0]<25)
        {
            PWM_times[4]=0;
        }

        if (times[1]>24 && times[1]<1225 && CC5!=1)
        {
            PWM_times[5]=-times[1];
        }
        else if (times[1]>1224 && CC5!=1)
        {
            PWM_times[5]=-1224;
        }
        else if (times[1]>1224 && CC5==1)
        {
            PWM_times[5]=1;
        }
        else if (times[1]>24 && times[1]<1225 && CC5==1)
        {
            PWM_times[5]=-times[1];
            CC5=-25;
        }
        else if (times[1]<25)
        {
            PWM_times[5]=0;
        }


  }// END OF RISE FALL CONDITION

  // END OF PHASE 3 CALCULATION

  // Data capture

  if (capture_count<500)
  {
    if(capture_period>=parameter[0])
    {
      data_array[0][capture_count]=voltages[0];
      data_array[1][capture_count]=voltages[1];
      data_array[2][capture_count]=npc_output;
      data_array[3][capture_count]=fstep;
      capture_count++;
      capture_period=0;
    }
    else
    {
      capture_period++;
    }
  }


  PWM_angle=PWM_angle+fstep;
  if (PWM_angle>20000) PWM_angle=PWM_angle-20000;
  if (PWM_angle<0) PWM_angle=PWM_angle+20000;

  if (rise_fall==1) rise_fall=0;
  else rise_fall=1;

}


/*------------------------ MAIN PROGRAM FUNCTION --------------------*/

void main (void)
{
  char input;
  float frequency;              // The demand frequency
  float ramp_rate;
```

```
float vfpercent;
float tempf;
bit PWM_active;
char status;

int data_counter;
int channel_valid[5];
int i;
int param;



data_counter=500;

IEN=1;

SYNCH=1;
DP2=0x4000;

set_comms();

frequency=0;
PWM_active=0;
status='U';                    /* START UNINITIALISED  */

do
{
 input=_getkey();
 switch (input)
 {
     case (0x01):              /*  RETURN MODE  */
        putchar(status);
        break;

     case (0x02):              /* SET FREQUENCY DEMAND  */
        scanf("%f",&frequency);
        fdemand=frequency*10;
        capture_period=0;
        capture_count=0;
        break;

     case (0x03):              /* RETURN FREQUENCY DEMAND  */
        printf("%f",(float)fdemand/10.0);
        putchar('\0');
        break;

     case (0x04):              /* RETURN ACTUAL FREQUENCY  */
        printf("%f",(float) fstep/10.0);
        putchar('\0');
        break;

     case (0x05):              /* SET RAMP RATE */
        scanf("%f",&ramp_rate);
        ramp_u=((float) 200.0/ramp_rate);
        if(ramp_rate>(float)parameter[8])ramp_rate=(float)parameter[8];
        ramp_d=((float) 200.0/ramp_rate);
        break;


     case (0x06):              /* START MODUALTION */
        if (PWM_active!=1)
        {
         PWM_active=1;
         start_PWM();
        }
        break;

     case (0x07):              /* STOP MODULATION */
        if (PWM_active!=0)
        {
         PWM_active=0;
         stop_PWM();
        }
        break;

     case (0x08):              /* RETURN MODULATION STATE */
        if (PWM_active) putchar('Y');
        else putchar('N');
        break;

     case (0x09):              /* ADJUST V/F RATIO */
        scanf("%f",&vfpercent);
        v_over_f=vfpercent/10;
        break;

     case (0x10):              /* STEP F INCREASE */
        fdemand++;
        break;

     case (0x11):              /* STEP F DECREASE */
        fdemand--;
        break;


     case (0x20):              /* Neutral Point Error */
        printf("%f",(float) neutral_point_error);
        putchar('\0');
        break;


// AD CONVERTER SET UP  ----- OFFSETS AND CALIBRATION
```

```
case (0x30):
case (0x31):
case (0x32):
case (0x33):
case (0x34):
case (0x35):
case (0x36):
case (0x37):
case (0x38):
case (0x39):

                                /* OFFSET */
   if (status=='U')
   {
      int temp, channel;

      SYNCH=0;
      channel = input-0x30;

      _nop_();
      _nop_();

      SYNCH=1;

      ADCON=channel;
      ADST=1;
      while (ADBSY==1){};
      temp=ADDAT;
      temp&=0x03FF;
      printf("%f",(float) temp);
      putchar('\0');
      AD_offset[channel]=temp;
      break;
   }
   else
   {
      printf("0.00");
      break;
   }


case (0x40):
case (0x41):
case (0x42):
case (0x43):
case (0x44):
case (0x45):
case (0x46):
case (0x47):
case (0x48):
case (0x49):
```

```
                                /* Calibration */
   if (status=='U')
   {
      int temp, channel;

      SYNCH=0;
      channel = input-0x40;

      _nop_();
      _nop_();

      SYNCH=1;

      ADCON=channel;
      ADST=1;
      while (ADBSY==1){};
      temp=ADDAT;
      temp&=0x03FF;
      temp=temp-AD_offset[channel];
      printf("%f",(float) temp);
      putchar('\0');
      break;
   }
   else
   {
      printf("0.00");
      putchar('\0');
      break;
   }

//-------------------------------------------------------


   case (0xA0):              /* INITIATE DATA TRANSFER */
     data_counter =0;

     for(i=0; i<5; i++)
     {
       printf("%s",channel_name[i]);
       putchar('\0');
       channel_valid[i]=strcmp(channel_name[i],"NULL");
     }
     break;

   case (0xA1):              /* TRANSMIT DATA BYTE */
     if (data_counter<500)
     {
       for (i=0; i<5; i++)
       {
         if (channel_valid[i]!=0)
         {
```

```
            printf("%d",data_array[i][data_counter]);
            putchar('\0');
          }
        }
        data_counter++;
      }
      else
      {
        putchar('\0');
      }

      break;

    case (0xA2):              /* CAPTURE DATA */
      capture_period=0;
      capture_count=0;
      break;

    case (0xA3):              // Capture in progress?
      if (capture_count<500) putchar('Y');
      else putchar('N');
      break;

//-----------------------------------------------------------------------

    case (0xB0):               /* Set parameter number */
      scanf("%f",&tempf);
      param=(int)tempf;
      if (param>49) param=49;
      if (param<0) param=0;
      break;

    case (0xB1):              /* Read parameter Value */
      printf("%f",(float)parameter[param]);
      putchar('\0');
      break;

    case (0xB2):              /* Write Parameter Value */
      scanf("%f",&tempf);
      parameter[param]=(int)tempf;
      capture_period=0;
      capture_count=0;
      break;


//-----------------------------------------------------------------------
    case (0xFF):              /* INITIALISE */
      status='B';
      configure_PWM();
      generate_sine_array();
      initialise_parameters();
      putchar('I');           /* SEND INITIALISATION COMPLETE */
      break;


    }

  } while (1);
  return;
}
```

A1.6.2 Software for the Five Level Inverter

```
/*-------------------------------------------------------------------------

    5 LEVEL INVERTER DRIVE PROGRAM : Vector Drive
                                     +Neutral point control

-------------------------------------------------------------------------*/


#pragma debug
#pragma code

#include <stdio.h>
#include <math.h>
#include <reg166.h>
#include <intrins.h>
#include <arrays.c>    // Arrays defined rather than built

/*-------------------------- DEFINITIONS ----------------------------*/

#define PWM_HALF_PERIOD 1250   // To give 1 khz Asymmetric 2kHz LOOP
#define PWM_HALF_LIMIT 1249
#define PWM_FULL_PERIOD 2500

#define MIN_HALF_TIME 35        // Minimum pulse width limits
#define MAX_HALF_TIME 1215

#define PWM_RISING_OFFSET 33
#define PWM_FALLING_OFFSET 0xFB3F
#define PWM_LIMIT_L 0xFB62

#define PI 3.141592654
#define WDGO 0
#define WDRST 1

/*------------------  BIT ACCESS DEFINITIONS ----------------------*/

sbit OUT1A=P2^0;
sbit OUT1B=P2^1;
sbit OUT1C=P2^2;
sbit OUT1D=P2^3;
sbit OUT2A=P2^4;
sbit OUT2B=P2^5;
sbit OUT2C=P2^6;
sbit OUT2D=P2^7;
sbit OUT3A=P2^8;
sbit OUT3B=P2^9;
sbit OUT3C=P2^10;
sbit OUT3D=P2^11;
sbit ENABLE=P2^12;              // ACTIVE LOW SIGNAL!!
sbit WATCHDOG=P2^13;
sbit SYNCH=P2^14;
sbit TIMING=P2^15;

/*----------------------- GLOBAL VARIABLES  --------------------------*/


int data_array[5][500];         // Array for storing data

int idata PWM_times[3][4];

int idata AD_offset[10];                // A/D Converter Offsets

int idata rise_fall[3];                 // 1=rising edge, 0=falling edge

int idata level[3];                     // Ouptut level for each phase
int idata carrier[3];                   // last carrier

int idata PWM_angle;                    // PWM reference angle
int idata fdemand;                      // Frequency Demand set by user
int idata fstep;                        // Controls actual frequency
int idata ramp_u;                         // Controls the ramp rate
int idata ramp_d;
int idata loop;                         // Controls the control loop
int idata v_over_f;                     // V/f ratio variable 0-10

int idata speed_loop;
int idata old_speed;

int idata iq_demand;                     // q axis current demand
int idata iq_d;
int idata old_speed_error;
int idata old_iq_error;
int idata old_id_error;
int idata Vdc;
int idata Vqc;

int idata Va;
int idata Vb;
long idata offset;
```

```
int idata old_Verror;
int idata delta;
int idata icp;


int idata capture_count;                // counter for data capture
int idata capture_period;


int idata parameter[50];                // parameter values
/*
                Parameter No    Value

                0               Data Capture Sample period
                1               Neutral Point Control nth multiplier
                2               """ n-1th multiplier
                3               """ divisor
                4               Neutral Point Offset Demand
                5               Neutral Point Control Active
                6               Neutral Point sample freq divider
                7               voltage boost minimum limit
                8               deceleration limiter
                9
                10               q axis limiter
                11               d axis demand
*/

char *channel_name[5]=
{
     "Id",
     "Iq",
     "Verror",
     "Icosphi",
     "Speed"
};


/*------------------------  FUNCTIONS  ------------------------------*/


void set_comms(void)            /* Sets up for the front end */
{
        P3|=0x0400;
        DP3|=0x0400;
        DP3&=0xf7ff;

        P3 |= 0x0100;
        DP3 |=0x0100;
        DP3 &=0xFDFF;
        S1TIC =0x80;
        S1RIC =0x00;
        S1BG  =0x40;
        S1CON = 0x8011;
}

void configure_PWM(void)
{
        T0IC=0x77;      // level 13, group 3, interrupt enabled
        T01CON=0x0000;  // 2.5 Mhz Counter Mode
        T0REL=-PWM_HALF_PERIOD;
        T0=-PWM_HALF_PERIOD;

        P2=0x0000;
        ENABLE=1;
        WATCHDOG=WDRST; // Start in Reset State
        SYNCH=1;
        DP2=0xFFFF;     // set up outputs

        CCM0=0x5555;
        CCM1=0x5555;
        CCM2=0x5555;    // set to mode 1 compare

        CC0IE=0;        // Turn of compare interrupts
        CC1IE=0;
        CC2IE=0;
        CC3IE=0;
        CC4IE=0;
        CC5IE=0;
        CC6IE=0;
        CC7IE=0;
        CC8IE=0;
        CC9IE=0;
        CC10IE=0;
        CC11IE=0;


        fstep=0;
        PWM_angle=0;

}

void configure_speed_timer(void)
{

        T3CON=0x014B;
        DP3&=0xFFAF;
        T3R=1;
}

void initialise_parameters(void)
{
        ramp_u=200;
        ramp_d=200;
```

```
        v_over_f=10;

        parameter[0]=0;
        parameter[1]=100;
        parameter[2]=40;
        parameter[3]=20;
        parameter[4]=0;
        parameter[5]=0;
        parameter[6]=5;
        parameter[7]=2;
        parameter[8]=3;
        parameter[10]=280;
        parameter[11]=160;
}


int int_modulation(int angle)
{
   int quadrant;
   int relative;

   quadrant=angle/500;
   relative=angle%500;

   switch (quadrant)
   {
      case 0:
         return modulation_array[relative];
      case 1:
         return -modulation_array[499-relative];
      case 2:
         return -modulation_array[relative];
      case 3:
         return modulation_array[499-relative];
   }
   return 0;
}

int int_cosine(int angle)
{
   int quadrant;
   int relative;

   quadrant=angle/500;
   relative=angle%500;

   switch (quadrant)
   {
      case 0:
         return cosine_array[relative];
      case 1:
         return -cosine_array[499-relative];
      case 2:
         return -cosine_array[relative];
      case 3:
         return cosine_array[499-relative];
   }
   return 0;
}

int int_sine(int angle)
{
   int quadrant;
   int relative;

   quadrant=angle/500;
   relative=angle%500;

   switch (quadrant)
   {
      case 0:
         return cosine_array[499-relative];
      case 1:
         return cosine_array[relative];
      case 2:
         return -cosine_array[499-relative];
      case 3:
         return -cosine_array[relative];
   }
   return 0;
}


void start_PWM(void)
{
   int *capcom;

   capcom=0xFE80;


   PWM_times[0][0]=0;
   PWM_times[0][1]=0;
   PWM_times[0][2]=0;
   PWM_times[0][3]=0;
   PWM_times[1][0]=0;
   PWM_times[1][1]=0;
   PWM_times[1][2]=0;
   PWM_times[1][3]=0;
   PWM_times[2][0]=0;
   PWM_times[2][1]=0;
   PWM_times[2][2]=0;
   PWM_times[2][3]=0;
```

```
capcom[0]=0;
capcom[1]=0;
capcom[2]=0;
capcom[3]=0;
capcom[4]=0;
capcom[5]=0;
capcom[6]=0;
capcom[7]=0;
capcom[8]=0;
capcom[9]=0;
capcom[10]=0;
capcom[11]=0;

OUT1A=0;
OUT1B=0;
OUT1C=0;
OUT1D=0;
OUT2A=0;
OUT2B=0;
OUT2C=0;
OUT2D=0;
OUT3A=0;
OUT3B=0;
OUT3C=0;
OUT3D=0;

rise_fall[0]=1;
rise_fall[1]=1;
rise_fall[2]=1;

level[0]=4;
level[1]=4;
level[2]=4;

carrier[0]=3;
carrier[1]=3;
carrier[2]=3;

PWM_angle=0;
fstep=0;              // Start at zero speed
loop=0;
fdemand=0;

speed_loop=0;
old_speed=0;
old_speed_error=0;
T3=0;

Vdc=0;
Vqc=0;
   old_id_error=0;
   old_iq_error=0;

   iq_demand=0;
   iq_d=0;

   offset=0;
   old_Verror=0;
   delta=0;
   icp=0;


   T0=-PWM_HALF_PERIOD;
   T0R=1;        // Start PWM timer
   ENABLE=0;
   WATCHDOG=WDGO;
   SYNCH=1;
   capture_count=0;
   capture_period=0;

}

void stop_PWM(void)
{
    T0R=0;       // Stop PWM timer
    ENABLE=1;
    WATCHDOG=WDRST;

    OUT1A=0;
    OUT1B=0;
    OUT1C=0;
    OUT1D=0;
    OUT2A=0;
    OUT2B=0;
    OUT2C=0;
    OUT2D=0;
    OUT3A=0;
    OUT3B=0;
    OUT3C=0;
    OUT3D=0;
    SYNCH=1;

}

/*-------------------------  INTERRUPT FUNCTIONS  --------------------*/


void PWM_routine(void) interrupt 0x20 using PWM_registers
{

  int mod_wave_value[3];
```

```
int mod_clamped[3];
int mod_diff[3];
int phase_angle[3];
int theta;
int vector_e;
int times[4];
int voltages[2];
int temp;
int i;
int phase;
int new_carrier[3];
int new_level[3];
int update[3][4];
int *capcom;
int Ia,Ib,Id,Iq,Ialpha,Ibeta;
int Vd,Vq;
int error;
long Idcalc,Iqcalc,demand;
long Icosphi,ltemp;
int amplitude;
int alpha,beta;
int speed;
int id_demand;
int Verror;


WATCHDOG=WDRST;
SYNCH=0;
capcom=0xFE80;
// load timers with values as calculated in last half cycle

capcom[0]=PWM_times[0][0];
capcom[1]=PWM_times[0][1];
capcom[2]=PWM_times[0][2];
capcom[3]=PWM_times[0][3];
capcom[4]=PWM_times[1][0];
capcom[5]=PWM_times[1][1];
capcom[6]=PWM_times[1][2];
capcom[7]=PWM_times[1][3];
capcom[8]=PWM_times[2][0];
capcom[9]=PWM_times[2][1];
capcom[10]=PWM_times[2][2];
capcom[11]=PWM_times[2][3];

WATCHDOG=WDGO;
SYNCH=1;
TIMING=1;

// Insert wait period while capture occurs on the sample/hold IC's
// using dummy a/d capture

ADCON=0;
ADST=1;


if(speed_loop>=9)
{
  speed=T3;
  speed=(speed*8)/20;
  T3=0;
  speed_loop=0;

  error=fdemand-speed;          // normalised to Hz * 10

  demand=(long)iq_d+((long)40*error)-((long)38*old_speed_error);
                  // Slow overshoot control

  //demand=(long)iq_d+((long)170*error)-((long)156*old_speed_error);
                  // Fast control

  old_speed_error=error;
  temp=parameter[10]*10;

  if(demand>temp) demand=temp;
  if(demand<-temp) demand=-temp;

  //if (speed>0 && demand<0) demand=0;
  //if(speed<0 && demand>0) demand=0;

  iq_d=demand;
  iq_demand=demand/10;
  old_speed=speed;
}
else
{
  speed=old_speed;
  speed_loop++;
}

while (ADBSY==1) _nop_(); // Finish delay for sample and hold IC's

// Sample A/D for real

ADCON=0;                        // Ia
ADST=1;

_nop_();
_nop_();
_nop_();

while (ADBSY==1) _nop_();
Ia=ADDAT;
Ia&=0x03FF;
Ia=Ia-AD_offset[0];
```

```
  ADCON=1;                        // Ib
  ADST=1;

  Ialpha=(3*Ia)/2;                // 'alpha' axis current
  Ibeta=+(52*Ia)/60;              // 'a' component of 'beta' axis current

  temp=PWM_angle-(fstep*10)/4;     // create reference angle for trig functions
  if (temp<0) temp=temp+20000;
  if (temp>=20000) temp=temp-20000;
  temp=temp/10;

  Idcalc=(long)Ialpha*int_cosine(temp);   // calculate 'alpha' components to
dq
  Iqcalc=(long)-Ialpha*int_sine(temp);

  while (ADBSY==1) _nop_();          // wait for Ib conversion to occur
  Ib=ADDAT;
  Ib&=0x03FF;
  Ib=Ib-AD_offset[1];

  ADCON=4;
  ADST=1;

  Ibeta=Ibeta+((52*Ib)/30);        // Finish the 'beta' calc.

  Idcalc=(long)Idcalc+(long)Ibeta*int_sine(temp);   //  finish dq calulations
  Iqcalc=(long)Iqcalc+(long)Ibeta*int_cosine(temp);

  Id=(long)Idcalc/256;       // Rescale due to integer trig functions.
  Iq=(long)Iqcalc/256;


  // D axis current control

  if(fstep>400)            // Field Weakening
    {
      demand=(long)parameter[11]*(long)400/fstep;
      id_demand=demand;
    }
  else if (fstep<-400)
    {
      demand=(long)parameter[11]*(long)400/-fstep;
      id_demand=demand;
    }
  else
    {
      id_demand=parameter[11];
    }

  error=id_demand-Id;
```

```
demand=(long)Vdc+(10*error)-(9*old_id_error);
old_id_error=error;

if (demand>5550)  demand=5550;
if (demand<-5550) demand=-5550;

Vdc=demand;

Vd=Vdc/200;


while (ADBSY==1) _nop_();
temp=ADDAT;
temp&=0x03FF;
temp=temp-AD_offset[4];
Va=temp;
//Va=(Va*7+temp)/8;

ADCON=5;
ADST=1;

// Q axis current control

error=iq_demand-Iq;

demand=(long)Vqc+(10*error)-(9*old_iq_error);
old_iq_error=error;

if(demand>5000) demand=5000;
if(demand<-5000) demand=-5000;

Vqc=demand;
Vq=Vqc/200;


// slip calculation:

fstep=speed+((iq_demand*8)/id_demand);

// Vector Compensation

demand=((long)id_demand*(long)fstep)/984;         // Field weakening

temp=demand;

Vq=Vq+temp;                    //  Approximation to V/f


while (ADBSY==1) _nop_();
temp=ADDAT;
temp&=0x03FF;
temp=temp-AD_offset[5];
```

```
Vb=temp;
//Vb=(Vb*7+temp)/8;


//if (fstep>1000) fstep=1000;
//if (fstep<-1000) fstep=-1000;


temp=(Vd*Vd)+(Vq*Vq);

if (temp==0)
{
  theta=0;
  amplitude=0;
}
else
{
  if (temp<128)
  {
    amplitude=sqrt_array[temp*4];
    temp=(10000/amplitude)*8;
    amplitude=amplitude/8;
  }
  else
  {
    amplitude=sqrt_array[temp/16];
    temp=10000/amplitude;
  }

  if (Vd>=0) alpha=Vd;
  else alpha=-Vd;
  if (Vq>=0) beta=Vq;
  else beta=-Vq;

  if (alpha<=beta) theta=20*(arccos_array[(alpha*temp)/32]);
  else theta=20*(250-arccos_array[(beta*temp)/32]);

  if (Vd>=0)
  {
    if (Vq<0) theta=-theta;
  }
  else
  {
    if (Vq>=0) theta=10000-theta;
    else theta =-10000+theta;
  }
}

// I cos(phi) calculation

if(amplitude!=0) Icosphi=((long)Vd*Id+(long)Vq*Iq)/amplitude;
else             Icosphi=0;
```

```
temp=Icosphi;

icp=(icp*7+temp)/8;

// Neutral Point Control

if(speed_loop==0)
{
  Verror=Vb-(Va-parameter[4]);

  demand=offset+(long)5000*Verror-(long)4500*old_Verror;

  if(Icosphi<0)
    ltemp=-Icosphi*1000;
  else
    ltemp=Icosphi*1000;

  if (demand>ltemp) demand=ltemp;
  if (demand<-ltemp) demand=-ltemp;

  offset=demand;
  old_Verror=Verror;

  if (icp<5 && icp>-5)
    delta=0;
  else
    delta=offset/((long)icp*4);
}

Verror=old_Verror;

// Rotate Vector for next cycle due to frequency


PWM_angle=PWM_angle+fstep;
if (PWM_angle>=20000) PWM_angle=PWM_angle-20000;
if (PWM_angle<0) PWM_angle=PWM_angle+20000;

// Add phase angle due to vector componants

vector_e=PWM_angle+theta;

if (vector_e>=20000) vector_e=vector_e-20000;
if (vector_e<0) vector_e=vector_e+20000;

phase_angle[0]=vector_e;

phase_angle[1]=vector_e-6666;
if (phase_angle[1]<0) phase_angle[1]=phase_angle[1]+20000;

phase_angle[2]=vector_e-13333;
if (phase_angle[2]<0) phase_angle[2]=phase_angle[2]+20000;
```

```
  mod_wave_value[0]=(amplitude*int_modulation(phase_angle[0]/10)/10)+delta;
  mod_wave_value[1]=(amplitude*int_modulation(phase_angle[1]/10)/10)+delta;
  mod_wave_value[2]=(amplitude*int_modulation(phase_angle[2]/10)/10)+delta;


  // Clamping
  for (phase=0; phase<3; phase++)
  {
    if (mod_wave_value[phase]>PWM_FULL_PERIOD)
mod_clamped[phase]=PWM_FULL_PERIOD;
    else if (mod_wave_value[phase]<-PWM_FULL_PERIOD) mod_clamped[phase]=-
PWM_FULL_PERIOD;
    else mod_clamped[phase]=mod_wave_value[phase];

    mod_diff[phase]=mod_wave_value[phase]-mod_clamped[phase];
  }

  mod_wave_value[0]=mod_clamped[0]-(mod_diff[1]+mod_diff[2]);
  mod_wave_value[1]=mod_clamped[1]-(mod_diff[0]+mod_diff[2]);
  mod_wave_value[2]=mod_clamped[2]-(mod_diff[0]+mod_diff[1]);

  // PWM


  for (phase=0; phase<3; phase++)
  {

    // Separate into carriers

    if(mod_wave_value[phase]>=PWM_HALF_PERIOD)
    {
       new_carrier[phase]=0;

       times[0]=(mod_wave_value[phase]-PWM_HALF_PERIOD);
       times[1]=PWM_HALF_PERIOD;
       times[2]=PWM_HALF_PERIOD;
       times[3]=PWM_HALF_PERIOD;
    }
    else if(mod_wave_value[phase]>=0)
    {
       new_carrier[phase]=1;

       times[0]=0;
       times[1]=mod_wave_value[phase];
       times[2]=PWM_HALF_PERIOD;
       times[3]=PWM_HALF_PERIOD;
    }
    else if(mod_wave_value[phase]>=-PWM_HALF_PERIOD)
    {
       new_carrier[phase]=2;

       times[0]=0;
       times[1]=0;
       times[2]=(mod_wave_value[phase]+PWM_HALF_PERIOD);
       times[3]=PWM_HALF_PERIOD;

    }
    else
    {
       new_carrier[phase]=3;

       times[0]=0;
       times[1]=0;
       times[2]=0;
       times[3]=(mod_wave_value[phase]+PWM_FULL_PERIOD);

    }

    //select rising or falling edge with optimisation for level transition

    if (new_carrier[phase]<carrier[phase]) rise_fall[phase]=1;
    else if (new_carrier[phase]>carrier[phase]) rise_fall[phase]=0;
    else if (level[phase]==carrier[phase]) rise_fall[phase]=0;
    else rise_fall[phase]=1;



    if (rise_fall[phase]==0)    // Falling Edge Condition
    {
      new_level[phase]=0;

      for (i=0; i<4; i++)
      {
      /*
        Step through the carriers, starting at the top and working down.

      */
        if(times[i]<=MIN_HALF_TIME) // Minimum Pulse Condition
        {
          if(level[phase]==i)
          {
          /*
            Switching level is high for this carrier,  Allows a falling
            edge to occur as normal, so load timer for edge at minimum
            value, and set new level as the next one down.

          */
            PWM_times[phase][i]=PWM_LIMIT_L;
            new_level[phase]=i+1;
          }
          else if(level[phase]>i)

          {
```

```
   /*
      Switching level is either at bottom of carrier due to pulse
      dropping, or is lower, and this is a perminant off state.
      Either case, no pulse required, and level can be set to
      the next one down.
   */
      PWM_times[phase][i]=1;
      new_level[phase]=i+1;
   }
   else
   {
   /*
      Switching level is above this carrier.  This must be a multi-
      level step.  Set the width accordingly, and increment level
      to the next one down.
   */
      PWM_times[phase][i]=PWM_LIMIT_L+(i-level[phase])*MIN_HALF_TIME;
      new_level[phase]=i+1;
   }
}
else if(times[i]>=MAX_HALF_TIME)  // Maximum pulse condition
{
   if(level[phase]==i)
   {
   /*
      Switching level is just above carrier, maintain this (drop
      falling edge), and leave level.
   */
      PWM_times[phase][i]=1;
      new_level[phase]=i;
   }
   else
   {
   /*
      If level above carrier, this must be turned on
   */
      PWM_times[phase][i]=1;
   }
}
else                                  // Normal pulse condition
{
   if(level[phase]==i)
   {
   /*
      Switching level is just above carrier, complete falling edge
      as standard.
   */
      PWM_times[phase][i]=PWM_FALLING_OFFSET+times[i];
      new_level[phase]=i+1;
   }
   else
   {
      /*
         This must be the end of a multi-level step, so check against
         new minimum width (including multi-step).  Otherwise as
         normal.
      */
         temp=MIN_HALF_TIME+(i-level[phase])*MIN_HALF_TIME;
         if(times[i]<temp) PWM_times[phase][i]=PWM_FALLING_OFFSET+temp;
         else PWM_times[phase][i]=PWM_FALLING_OFFSET+times[i];
         new_level[phase]=i+1;
      }

   }

  }

}
else                  // RISING EDGE CONDITION
{
  new_level[phase]=4;

  for(i=3; i>-1; i--)
  {
  /*
     Step through the carriers starting at the bottom and working up
  */
     if(times[i]<=MIN_HALF_TIME)  // Minimum pulse condition
     {
        if(level[phase]==(i+1))
        {
        /*
           level is just below carrier, so maintain below.
        */
           PWM_times[phase][i]=1;
           new_level[phase]=i+1;
        }
        else
        {
        /*
           level must be below carrier range, so just keep off
        */
           PWM_times[phase][i]=1;

        }

     }
     else if(times[i]>=MAX_HALF_TIME)  // Maximum pulse condition
     {
        if(level[phase]==i)
        {
        /*
             Already high, so just maintain
        */
```

```
            PWM_times[phase][i]=1;
            new_level[phase]=i;
          }
          else if(level[phase]>i)
          {
          /*
               level below carrier, so switch allowing for multi-level step
          */
            PWM_times[phase][i]=PWM_LIMIT_L+(level[phase]-i)*MIN_HALF_TIME;
            new_level[phase]=i;
          }
          else
          {
          /*
            Level above carrier, so ignore
          */
            PWM_times[phase][i]=1;
            new_level[phase]=i;
          }
        }
        else
        {


          temp=MAX_HALF_TIME-(level[phase]-i)*MIN_HALF_TIME;
          if(times[i]>temp)  PWM_times[phase][i]=PWM_RISING_OFFSET-temp;
          else PWM_times[phase][i]=PWM_RISING_OFFSET-times[i];
          new_level[phase]=i;


        }

    }

  }

  carrier[phase]=new_carrier[phase];
  level[phase]=new_level[phase];

}


// Data capture

if (capture_count<500)
{
  if(capture_period>=parameter[0])
  {
    data_array[0][capture_count]=Id;
    data_array[1][capture_count]=Iq;
    data_array[2][capture_count]=Verror;
    data_array[3][capture_count]=icp;
    data_array[4][capture_count]=speed;
    capture_count++;
    capture_period=0;
  }
  else
  {
    capture_period++;
  }
}


TIMING=0;
}


/*------------------------- MAIN PROGRAM FUNCTION --------------------*/

void main (void)
{
  char input;
  float frequency;              // The demand frequency
  float ramp_rate;
  float vfpercent;
  float tempf;
  bit PWM_active;
  char status;

  int data_counter;
  int channel_valid[5];
  int i;
  int param;


  data_counter=500;

  IEN=1;

  SYNCH=1;
  DP2=0x4000;

  set_comms();

  frequency=0;
  PWM_active=0;
  status='U';                    /* START UNINITIALISED  */

  do
  {
   input=_getkey();
```

```
switch (input)
{
    case (0x01):              /*  RETURN MODE  */
       putchar(status);
       break;

    case (0x02):              /* SET FREQUENCY DEMAND  */
       scanf("%f",&frequency);
       fdemand=frequency*10;
       capture_period=0;
       capture_count=0;
       break;

    case (0x03):              /* RETURN FREQUENCY DEMAND  */
       printf("%f",(float)fdemand/10.0);
       putchar('\0');
       break;

    case (0x04):              /* RETURN ACTUAL FREQUENCY  */
       printf("%f",(float) fstep/10.0);
       putchar('\0');
       break;

    case (0x05):              /* SET RAMP RATE */
       scanf("%f",&ramp_rate);
       ramp_u=((float) 200.0/ramp_rate);
       if(ramp_rate>(float)parameter[8])ramp_rate=(float)parameter[8];
       ramp_d=((float) 200.0/ramp_rate);
       break;


    case (0x06):              /* START MODUALTION */
       if (PWM_active!=1)
       {
        PWM_active=1;
        start_PWM();
       }
       break;

    case (0x07):              /* STOP MODULATION */
       if (PWM_active!=0)
       {
        PWM_active=0;
        stop_PWM();
       }
       break;

    case (0x08):              /* RETURN MODULATION STATE */
       if (PWM_active) putchar('Y');
       else putchar('N');
       break;

    case (0x09):              /* ADJUST V/F RATIO */
       scanf("%f",&vfpercent);
       v_over_f=vfpercent/10;
       break;

    case (0x10):              /* STEP F INCREASE */
       fdemand++;
       break;

    case (0x11):              /* STEP F DECREASE */
       fdemand--;
       break;


    case (0x20):              /* Neutral Point Error */
       printf("%f",(float) Va-Vb);
       putchar('\0');
       break;


    // AD CONVERTER SET UP  ----- OFFSETS AND CALIBRATION



    case (0x30):
    case (0x31):
    case (0x32):
    case (0x33):
    case (0x34):
    case (0x35):
    case (0x36):
    case (0x37):
    case (0x38):
    case (0x39):

                                        /* OFFSET */
       if (status=='U')
       {
          int temp, channel,count;
          long sum;

          sum=0;

          for(count=0; count<1000; count++)
          {
            SYNCH=0;
            channel = input-0x30;

            _nop_();
            _nop_();
            _nop_();
            _nop_();
```

```
        SYNCH=1;

        ADCON=0;
        ADST=1;

        _nop_();

        while (ADBSY==1) _nop_();

        ADCON=channel;
        ADST=1;

        _nop_();

        while (ADBSY==1) _nop_();
        temp=ADDAT;
        temp&=0x03FF;
        sum=sum+temp;
      }

      temp=sum/1000;
      if((sum%1000)>=500) temp=temp+1;

      printf("%f",(float) temp);
      putchar('\0');
      AD_offset[channel]=temp;
      break;
   }
   else
   {
      printf("0.00");
      break;
   }



case (0x40):
case (0x41):
case (0x42):
case (0x43):
case (0x44):
case (0x45):
case (0x46):
case (0x47):
case (0x48):
case (0x49):

                                /* Calibration */
   if (status=='U')
   {
      int temp, channel, count;
      long sum;

      sum=0;

      for(count=0; count<1000; count++)
      {
        SYNCH=0;
        channel = input-0x40;

        _nop_();
        _nop_();
        _nop_();
        _nop_();

        SYNCH=1;

        ADCON=0;
        ADST=1;

        _nop_();

        while (ADBSY==1) _nop_();

        ADCON=channel;
        ADST=1;

        _nop_();

        while (ADBSY==1) _nop_();;
        temp=ADDAT;
        temp&=0x03FF;

        sum=sum+temp;
      }

      temp=sum/1000;
      if((sum%1000)>=500) temp=temp+1;

      temp=temp-AD_offset[channel];
      printf("%f",(float) temp);
      putchar('\0');
      break;
   }
   else
   {
      printf("0.00");
      putchar('\0');
      break;
   }

//-------------------------------------------------------
```

```
   case (0xA0):              /* INITIATE DATA TRANSFER */
     data_counter =0;

     for(i=0; i<5; i++)
     {
       printf("%s",channel_name[i]);
       putchar('\0');
       channel_valid[i]=strcmp(channel_name[i],"NULL");
     }
     break;

   case (0xA1):              /* TRANSMIT DATA BYTE */
     if (data_counter<500)
     {
       for (i=0; i<5; i++)
       {
         if (channel_valid[i]!=0)
         {
           printf("%d",data_array[i][data_counter]);
           putchar('\0');
         }
       }
       data_counter++;
     }
     else
     {
       putchar('\0');
     }

     break;

   case (0xA2):              /* CAPTURE DATA */
     capture_period=0;
     capture_count=0;
     break;

   case (0xA3):              // Capture in progress?
     if (capture_count<500) putchar('Y');
     else putchar('N');
     break;

//---------------------------------------------------------------------

   case (0xB0):               /* Set parameter number */
     scanf("%f",&tempf);
     param=(int)tempf;
     if (param>49) param=49;
     if (param<0) param=0;
     break;

   case (0xB1):              /* Read parameter Value */
     printf("%f",(float)parameter[param]);
     putchar('\0');
     break;

   case (0xB2):              /* Write Parameter Value */
     scanf("%f",&tempf);
     parameter[param]=(int)tempf;
     capture_period=0;
     capture_count=0;
     break;


//---------------------------------------------------------------------
   case (0xFF):              /* INITIALISE */
     status='B';
     configure_PWM();
     configure_speed_timer();
     initialise_parameters();
     putchar('I');           /* SEND INITIALISATION COMPLETE */
     break;


 }

 } while (1);
 return;
}
```

A1.7 Ancillary Components

A1.7.1 Dynamic Braking Unit

In order for rapid deceleration of the motor to occur some form of energy sink is required on the DC link to absorb the stored energy from the mechanical system. The AC supply used throughout the project was the standard 415V three phase mains. This allowed a standard commercial dynamic braking chopper to be utilised.

A1.7.2 DC link Precharge

The precharge arrangement for the DC link varied with different inverter types and conditions. For the three level inverter the supply was connected via a variac. This allowed the supply to be charged to any desired level at the users control.

For the five level inverter with an input transformer a variac was used on the primary connection to again regulate the voltage as desired. Once the balancers had been added, and full power operation was required a more conventional precharge circuit was installed. The basic arrangement is shown in figure A1.21.

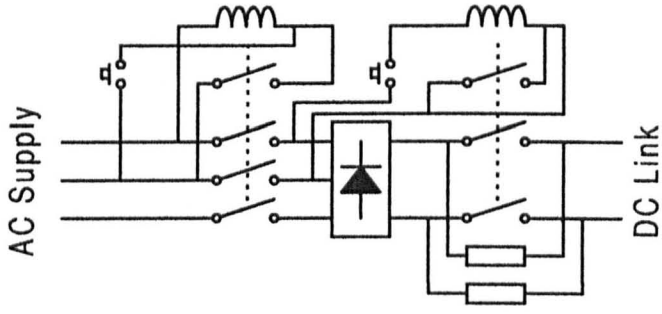

***Figure A1.21** : Precharge Circuit*

A1.8 Appendix References

[1] "80C166 Microcontroller User Manual", Siemens AC, 1990

Appendix 2

Simulations and Numerical Analysis

Appendix Contents

A2.1 Introduction

Some of the work described in the main chapters of this thesis has been backed up by simulations and numerical analysis. Whilst the main chapters concentrate on the results of any analysis work, this appendix has been included to provide a description of the analytical techniques used.

A2.2 Generation of Surface Plots

The various surface plots presented in chapters three and five were produced using MATLAB [1]. For the basic three level inverter the algebraic equation is used to calculate the points on the surface. For those surfaces that do not have simple algebraic solutions, a discrete step analysis is used.

A2.2.1 Script for plotting 3D surface

An example script for the plotting the 3D surface for the neutral point control is given below. This is the script for the five level inverter.

```
for x=1:41
  for y=1:21
   K(x,y)=real(Kn5((y-1)/20,(x-21)/20));
  end
end

for x=1:41
   X(x)=(x-21)/20;
end

for y=1:21
   Y(y)=(y-1)/20;
end

mesh(X,Y,K');
view(45,40);
grid;
xlabel ('Offset d');
ylabel('Modulation Amplitude A');
zlabel('K(A,d)');
colormap(gray);
```

The surface consists of 41 by 21 points calculated from an external function. In this case Kn5 is used, which derives the current for the five level inverter. Different surfaces are plotted by calling the appropriate function to calculate the points.

A2.2.2 Functions for calculation of points on the surface

The three level inverter produced a algebraic solution when sinusoidal modulation was used. The MATLAB script for this is relatively simple and is given below. The numerical solution does have a discontinuity at zero modulation amplitude which could generate a divide by zero error. This is prevented by a simple check before each calculation.

```
function [result]=Kn(A,d)

if A==0
   A=0.00001;

end

result=(-1/(A*pi))*((A*A*asin(d/A))+(d*sqrt(A*A-d*d)));
```

Once third harmonic injection is included it becomes simpler to use a step average to find the mean current rather than algebraic integration. The script for this situation is given below.

```
function [result]=Kn3(A,d)

for t=1:1000

  m=A*sin(t*pi/500)+(1/9)*A*sin(t*3*pi/500)+d;

  if (m>=0)
    m2=(1-m);
  else
    m2=(1+m);
  end

  in(t)=m2*sin(t*pi/500);

end

result=mean(in);
```

The solution at the particular point (amplitude A, offset d) is generated by calculating the instantaneous product of the modulation function and a sinusoidal load current. One thousand points are calculated over a modulation cycle from which the mean value is obtained. Not that the use of a sinusoidal current of unit amplitude equates to the following equation.

$$\hat{I}\cos(\phi) = 1 \qquad [A2.1]$$

A slightly more complicated function is required when clamping is employed. Modulation functions for all three phases must be generated, and clamping applied to each in order to generate the correct compensation components. Once this is done the calculation proceeds as before.

```
function [result]=Kn3(A,d)
for p=1:3
  for i=1:1000

  m(p,i)=A*sin((i*pi/500)+(2*p*pi/3))+d;

  if m(p,i)>1
   mc(p,i)=1;
  elseif m(p,i)<-1
   mc(p,i)=-1;
  else
   mc(p,i)=m(p,i);
  end

  md(p,i)=mc(p,i)-m(p,i);

  end
end

mclamp(1:1000)=mc(3,:)+md(2,:)+md(1,:);


for t=1:1000

  if (mclamp(t)>=0)
    m2=(1-mclamp(t));
  else
    m2=(1+mclamp(t));
  end

  in(t)=m2*sin(t*pi/500);

end

result=mean(in);
```

Similar functions are used to generate the points for the five level inverter. The following listing gives the script for the five level case with range extension via the clamping technique. It is assumed that the balancers are operating with the predicted effect on the neutral point (as defined by equation 5.26).

```
function [result]=Kn5(A,d)

for t=1:1000

  m=A*sin(t*pi/500)+d;

  c1=A*sin((2*pi/3)+(t*pi/500))+d;
  c2=A*sin((4*pi/3)+(t*pi/500))+d;

  if (c1>1.0)
      c1=c1-1.0;
  elseif (c1<-1.0)
      c1=c1+1.0;
  else
      c1=0;
  end;

  if (c2>1.0)
      c2=c2-1.0;
  elseif (c2<-1.0)
      c2=c2+1.0;
  else
      c2=0;
  end;

  m=m-(c1+c2);

  if (m>1.0)
      m=1.0;
  elseif (m<-1.0)
      m=-1.0;
  end;

  if (m>=0.5)
    m3=0.5*(2-2*m);
  elseif (m>=0)
    m3=(1-2*m)+0.5*(2*m);
  elseif (m>=-0.5)
    m3=(1+2*m)-0.5*(2*m);
  else
    m3=0.5*(2+2*m);
  end

  in(t)=m3*sin(t*pi/500);

end

result=mean(in);
```

A2.3 Balancer Simulations

The balancer circuit developed for the project required simulation to confirm the operation, and allow the control strategy to be developed. Since the controller was to be built in hardware, the control had to be fully checked before building commenced. SIMULINK [2] was chosen since this allowed the various parts of the circuit to be modelled.

A2.3.1 S-plane simulation

Most of the control development was completed via a simple block diagram structure. The switching was assumed to be ideal except for the dependence on the capacitor voltages. Figure A2.1 shows the top level block diagram for the simulation.

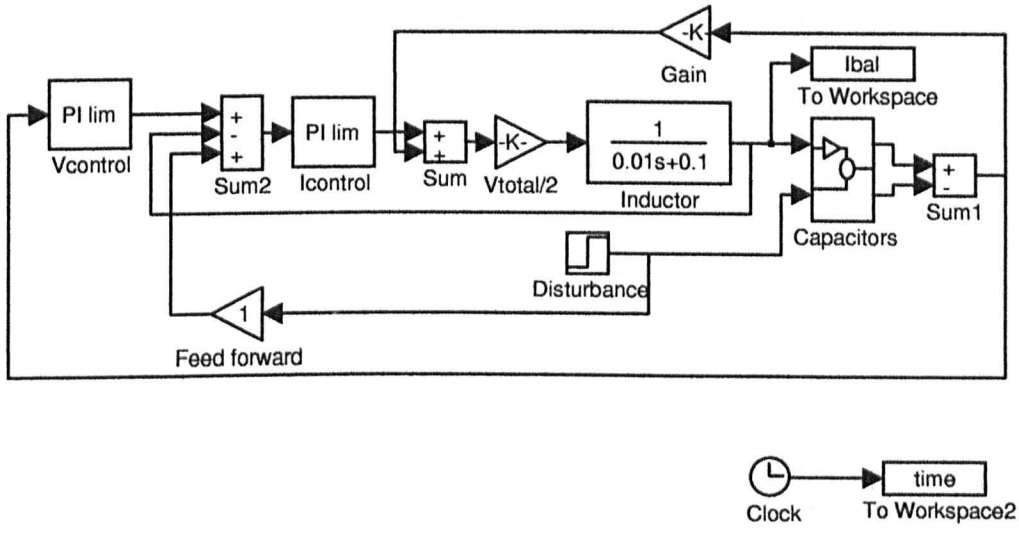

Figure A2.1 : Balancer control model

The figure shows the complete control arrangement, including feed-forward of the current drawn by the inverter, which is shown as a disturbance.

The inductor is modelled as a s plane RL block. This sets the initial condition for the current to zero. The capacitors are modelled in the sub-block shown in figure A2.2.

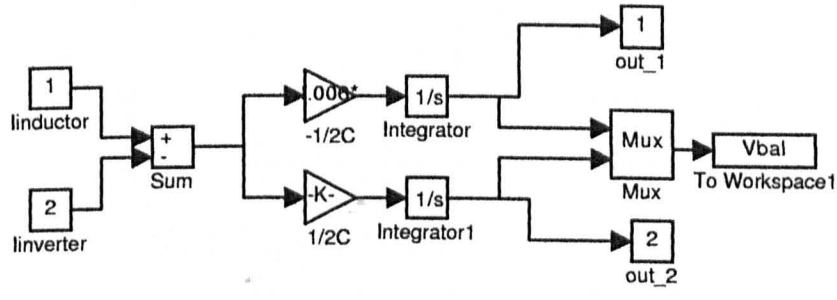

Figure A2.2 : Capacitor Model

The capacitors are modelled as ideal integrators, with the capacitance set by gains on their respective currents. This has the advantage of allowing the initial conditions of the capacitors to be defined.

This control model was used to generate the simulated responses given in chapter 5 figures 25, 28 and 29. The model was modified for the particular conditions.

A2.3.2 Simulation of switching within control model

The predicted operation of the balancer was further confirmed by inclusion of the switching strategy into the simulation, along with a more detailed node current breakdown for the circuit. This model is shown in figure A2.3.

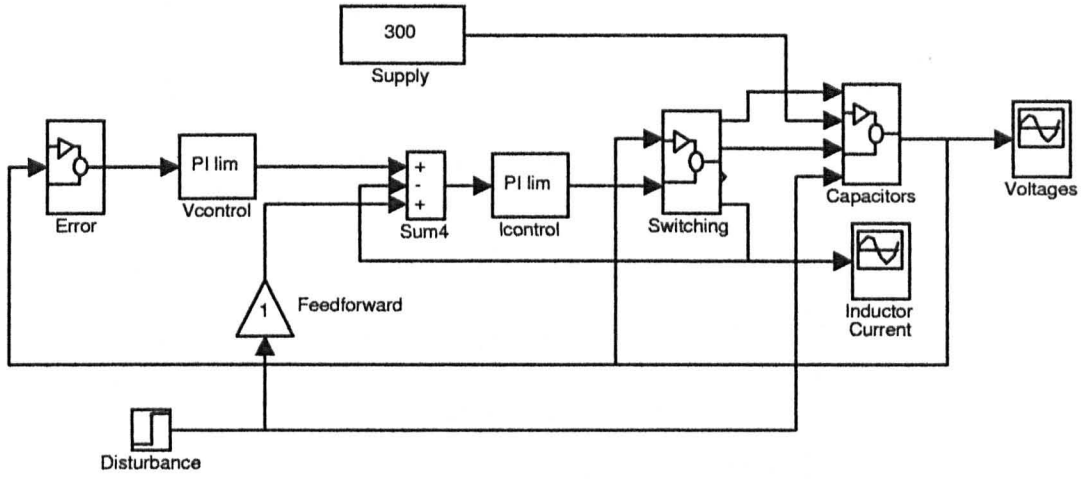

Figure A2.3 : *Model with switching included*

The inclusion of switching into the model provides some additional information on the behaviour of the circuit, but provides little additional knowledge for the control design. Figure A2.4 shows the results for a similar current disturbance between the basic ideal simulation, and the simulation with switching included. It is clear that two simulations produce very similar results..

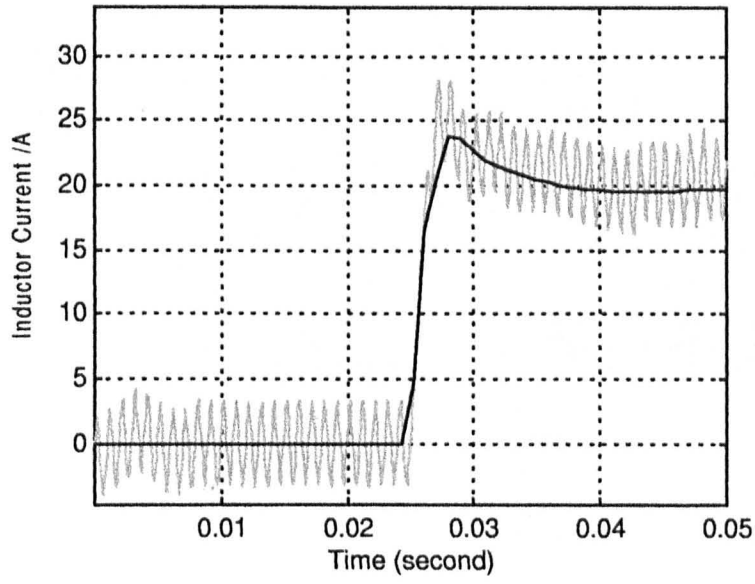

Figure A2.4 : *Simulation of current response with and without switching*

The sub-block for the switching is shown in figure A2.5. This block takes the PWM pattern generated from a function block and produces the actual voltage waveform for the inductor. The inductor is modelled as an s-plane RL as with the earlier simple model. The PWM pattern also allows the various node currents to be derived.

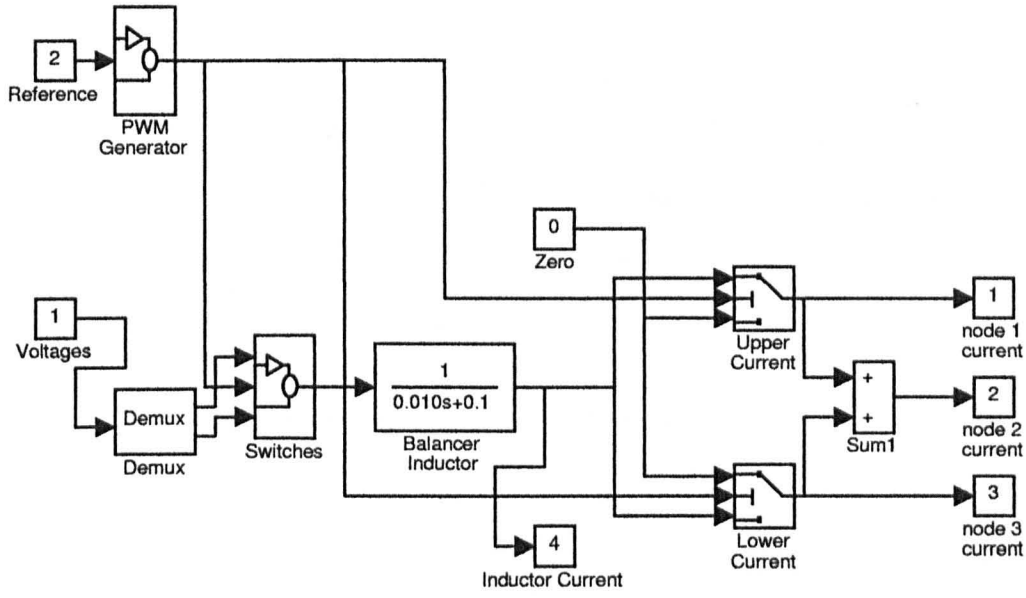

Figure A2.5 : *Switching sub-block model*

The PWM is generated by the sub-block shown in figure A2.6. This block constructs the switching pattern, including the commutation state as described in chapter 5.

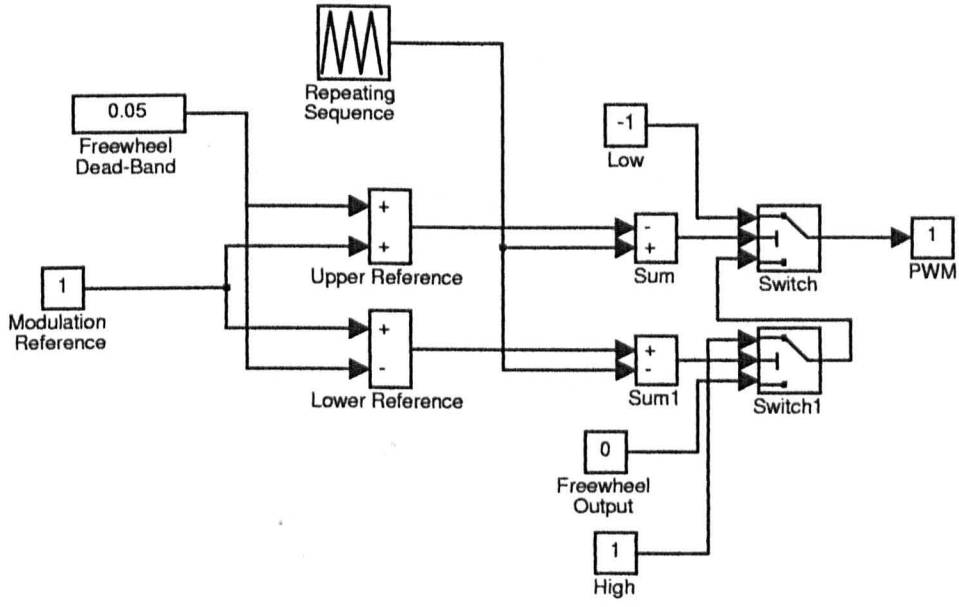

Figure A2.6 : *Balancer PWM sub-block model*

Once the node currents are derived the circuit model for the capacitors can be used to obtain the voltages. The sub-block model for this is shown in figure A2.xx. The supply for the two capacitors is also included into the model.

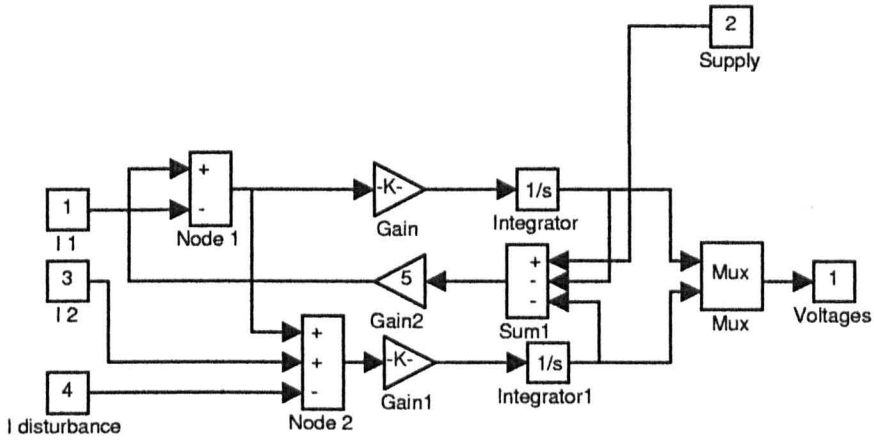

Figure A2.7 : *Circuit model for capacitors*

A2.4 References

[1] "Matlab Reference Guide", The Math Works Inc., 1992.

[2] "Simulink User's Guide", The Math Works Inc., 1992.

Appendix 3

Additional Information

Appendix Contents

A3.1 Introduction

This appendix provides reference information not available in documented form.

A3.2 Motor Information

Three motors were used on the prototype inverters during the project. The nameplate details of these are given below.

A3.2.1 Machine 1: BBC Brown Boveri 4kW Induction Motor

The second motor was used for development testing on both the three level and five level prototypes. The motor was used extensively during vector control development.

Parameter	Value	Units
Power	4	kW
Voltage	415	V
Current	8.42	A
p.f.	-	
Poles	4	
Speed	1420	rpm

***Table A3-1** : Parameters for machine 1*

This machine was used for the early vector control work, since it has been used previously in high performance control development, and the electrical parameters are accurately known. These are given in the following table.

Parameter	Value	Units
R_s	2.0	Ω
R_r	1.66	Ω
I_m	3.387	A
L_s	244	mH
σL_s	21	mH
τ_r	0.135	

***Table A3-2** : Vector control parameters for machine 1*

A3.2.2 Machine 2: Mitsubishi 11kW Induction Motor

The third motor was used for full current testing of both the three and five level inverters.

Parameter	Value	Units
Power	11	kW
Voltage	400	V
Current	21.5	A
p.f.	-	
Poles	4	
Speed	1430	rpm

***Table A3-3** : Parameters for machine 2*

Bibliography

Bibliography Contents

B1.1 Introduction

This bibliography is a collection of the reference material from the project. The numbers given here to each item is independant to that used for each of the chapter reference sections, which are subsets of these lists.

B1.2 Papers listed by first author

[1] A. I. Alolah, L. N. Hulley, W. Shepherd, "A Three-Phase Neutral Point Clamped Inverter for Motor Control", IEEE Transactions on Power Electronics, Vol. 3 No. 4, Oct. 1988, pp 399-405.

[2] F. B. Ammar, L-O Peter-Contesse, M. Pietrzak-David, B. de Fornel, "POWER-RANGE EXTENSION OF AN INDUCTION MOTOR SPEED-DRIVE BY USING A THREE-LEVEL GTO INVERTER WITH SPACE VECTOR MODULATION", Conference Proceedings EPE'93, Brighton, 1993, pp 219-223.

[3] N. Aouda, L. Prissé, T. Meynard, H. Foch, "A Multilevel Rectifier with Unity Power Factor and Sinusoidal Input Current for High Voltage Applications" EPE Journal. Vol. 6, No. 3-4, December 1996, pp 27-35.

[4] F. Bauer, H.-D. Heining, "QUICK RESPONSE SPACE VECTOR CONTROL FOR A HIGH POWER THREE LEVEL INVERTER DRIVE SYSTEM", Conference Proceedings EPE'89, Aachen, 1989, pp 417-421.

[5] H. Bächle, H. P. Bauer, T. Seger, "REQUIREMENTS ON THE CONTROL OF A THREE-LEVEL FOUR QUADRANT POWER CONVERTER IN A TRACTION APPLICATION", Conference Proceedings EPE'89, Aachen, 1989, pp 577-582.

[6] P. M. Bhagwat, V. R. Stefanovic, "Generalised Structure of a Multilevel PWM Inverter", IEEE Transactions on Industry Applications, Vol. 19, No. 6, Nov./Dec. 1983, pp 1057-1069.

[7] A. H. Bonnett, "Avaliable Insulation Systems for PWM Inverter-Fed Motors", IEEE Industry Applications Magazine, Vol. 4, No. 1, Jan/Feb 1998, pp 14-26.

[8] S. R. Bowes, M. J. Mount, "Microprocessor Control of PWM Inverters", IEE Proceedings Part B, Vol. 128, No. 6, November 1981, pp 293-305.

[9] H. W. van der Broeck, H. –C. Skudelny, G. V. Stanke, "Analysis and Realisation of a Pulsewidth Modulator Based on Voltage Space Vectors", IEEE Transactions on Industry Applications, Vol. 26, No. 1, Jan/Feb 1988, pp 142-150.

[10] A. Campagna, G. Carrara, D. Casini, R. Salutari, "A NEW GENERALISED MULTILEVEL THREE-PHASE STRUCTURE CONTROLLED BY PWM", Conference Proceedings EPE'91, Firenze, Vol. 3, 1991, pp 235-239.

[11] G. Carrara, S. Gardella, M. Marchesoni, R. Salutari, G. Sciutto, "A NEW MULTILEVEL PWM METHOD: A THEORETICAL ANALYSIS", IEEE Conference Proceedings PESC'90, June 1990, pp 363-371.

[12] G. Carrara, S. Gardella, M. Marchesoni, R. Salutari, G. Sciutto, "A New Multilevel PWM Method: A Theoretical Analysis", IEEE Transactions on Power Electronics, Vol. 7, No. 3, July 1992, pp 497-505.

[13] P. Carrère, T. Meynard, J. P. Lavieville, "4000V-300A EIGHT LEVEL IGBT INVERTER LEG", Conference Proceedings EPE'95, Sevilla, Vol. 1, 1995, pp 106-111.

[14] D. Casini, M. Marchesoni, L. Puglisi, "Sliding Mode Multilevel Control for Improved Performances in Power Conditioning Systems", IEEE Transactions on Power Electronics, Vol. 10, No. 4, July 1995, pp 453-463.

[15] D. Casini, M. Marchesoni, L. Puglisi, "Variable structure control system applied to multilevel power conditioning converters", Proceedings First European Space Power Conference, Madrid, Oct. 1989, pp 672-682.

[16] N. S. Choi, J. G. Cho, G. H. Cho, "A GENERAL CIRCUIT TOPOLOGY OF MULTILEVEL INVERTER", IEEE Conference Proceedings PESC'91, 1991, pp 96-103.

[17] P. Enjeti, R. Jakkli, "OPTIMAL POWER CONTROL STRATEGIES FOR NEUTRAL POINT CLAMPED (NPC) INVERTER TOPOLOGY", IEEE Conference Proceedings IAS'89, 1989, pp 924-930.

[18] P. N. Enjeti, R. Jakkli, "Optimal Power Control Strategies for Neutral Point Clamped (NPC) Inverter Topology", IEEE Transactions on Industry Applications, Vol. 28, No. 3, May/June 1993, pp 558-566.

[19] M. Fracchia, T. Ghiara, M. Marchesoni, M. Mazzucchelli, "OPTIMISED MODULATION TECHNIQUES FOR THE GENERALISED N-LEVEL CONVERTER", IEEE Conference Proceedings PESC'92, 1992, pp 1205-1213.

[20] P. W. Hammond, "A New Approach to Enhance Power Quality for Medium Voltage AC Drives", IEEE Transactions on Industry Applications, Vol. 33, No. 1, Jan/Feb 1997.

[21] D. Hilder, "Partial-discharge measurements for insulation quality", IEE Power Journal, March 1992, pp 79-86.

[22] C. Hochgraf, R. Lasseter, D. Divan, T. A. Lipo, "Comparison of Multilevel Inverters For Static Var Compensation", IEEE Conference Proceedings IAS'94, 1994, pp921-928.

[23] J. Holtz, S. Stadtfeld, P. Lammert, "AN ECONOMIC VERY HIGH POWER PWM INVERTER FOR INDUCTION MOTOR DRIVES", Conference Proceedings EPE'85, Bruxelles, Vol. 3. 1989, pp 75-80.

[24] J. Holtz, S. F. Salama, "MEGAWATT GTO-INVERTER WITH THREE-LEVEL PWM CONTROL AND REGENERATIVE SNUBBER CIRCUITS", IEEE Conference Proceedings PESC'88, April 1988, pp 1263-1270.

[25] J. A. Houldsworth, D. A. Grant, "The use of harmonic distortion to increase the output voltage of a three phase inverter", IEEE Transactions on Industry Applications, Vol. 20, 1984, pp 1224-1227.

[26] R. Joetten, M. Gekeler, J. Eibel, "A.C. DRIVE WITH THREE-LEVEL VOLTAGE SOURCE INVERTER AND HIGH DYNAMIC PERFORMANCE MICROPROCESSOR CONTROL", Conference Proceedings EPE'85, Bruxelles, Vol. 3, 1985, pp 1-6.

[27] R. Joetten, C. Kehl, "A FAST SPACE-VECTOR CONTROL FOR A THREE-LEVEL VOLTAGE SOURCE INVERTER", Conference Proceedings EPE'91, Firenze, Vol. 2, pp 70-75.

[28] H. L. Klaver, "CONTROL OF THE NEUTRAL POINT OF A THREE-LEVEL-INVERTER", Conference Proceedings EPE'91, Firenze, Vol. 3, 1991, pp278-281.

[29] J. –S. Lai, F. Z. Peng, "Multilevel Converters – A New Breed of Power Converters", IEEE Transactions on Industry Applications, Vol. 32, No. 3, May/June 1996, pp 509-517.

[30] H. L. Liu, G. H. Cho, "THREE-LEVEL SPACE VECTOR PWM IN LOW INDEX MODULATION AVOIDING NARROW PULSE PROBLEMS", IEEE Conference Proceedings PESC'93, 1993, pp 257-262.

[31] H. L. Liu, G. H. Cho, S. S. Park, "Optimal PWM Design for High Power Three-Level Inverter Through Comparative Studies", IEEE Transactions on Power Electronics, Vol. 10, No. 1, Jan. 1995, pp 38-47.

[32] A. Mahfouz, J. Holtz, A El-Tobshy, "DEVELOPMENT OF AN INTEGRATED HIGH VOLTAGE 3-LEVEL CONVERTER-INVERTER SYSTEM WITH SINUSOIDAL INPUT OUTPUT FOR FRRDING 3-PHASE INDUCTION MOTORS", Conference Proceedings EPE'93, Brighton, 1993, pp 134-139.

[33] M. Marchesoni, M. Mazzucchelli, S. Tenconi, "A NON CONVENTIONAL POWER CONVERTER FOR PLASMA STABALIZATION", IEEE Conference Proceedings PESC'88, April 1988, pp 122-129.

[34] M. Marchesoni, "HIGH PERFORMANCE CURRENT CONTROL TECHNIQUES FOR APPLICATIONS TO MULTILEVEL HIGH POWER VOLTAGE SOURCE INVERTERS", IEEE Conference Proceedings PESC'89, 1989, pp 672-682.

[35] M. Marchesoni, M. Mazzucchelli, S. Tenconi, "A Nonconventional Power Converter for Plasma Stabilization", IEEE Transactions on Power Electronics, Vol. 5, No. 2, April 1990, pp 212-219.

[36] M. Marchesoni, "High-Performance Current Control Techniques for Applications to Multilevel High-Power Voltage Source Inverters", IEEE Transactions on Power Electronics, Vol. 7, No. 1, Jan. 1992, pp 189-204

[37] M. Marchesoni, M. Mazzucchelli, "Multilevel Converters for High Power AC Drives: a Review", IEEE Symposium on Industrial Electronics, Budapest, 1993, pp 38-43.

[38] T. Maruyama, M. Kumano, M. Ashiya, "A NEW ASYNCHRONOUS PWM METHOD FOR A THREE-LEVEL INVERTER", IEEE Conference Proceedings PESC'91, Vol. 1, 1991, pp 366-371.

[39] R. W. Menzies, P. Steimer, J. K. Steinke, "Five-Level GTO Inverters for Large Induction Motor Drives", IEEE Transactions on Industry Applications, Vol. 30, No. 4, July/Aug. 1994, pp 938-944.

[40] A. Nabae, I. Takahashi, H. Akagi, "A New Neutral-Point-Clamped PWM Inverter", IEEE Transactions on Industry Applications, Vol. 17, No. 5, Sept./Oct. 1981, pp 518-523.

[41] S. Ogasawara, H. Akagi, "Analysis of Variation of Neutral Point Potential in Neutral-Point-Clamped Voltage Source PWM Inverters", IEEE Conference Proceedings IAS'93, 1993, pp 965-970.

[42] K. Oguchi, Y. Maki, "A Multilevel-Voltage Source Rectifier with a Three-Phase Diode Bridge Circuit as a Main Power Circuit", IEEE Conference Proceedings IAS'92, 1992, pp 695-702.

[43] K. Oguchi, Y. Maki, Y. Sunaga, "Three-Phase Multilevel Voltage Source Converters with Low Switching Frequencies and Less-Distorted Input Voltages", IEEE Conference Proceedings IAS'93, 1993, pp 870-878.

[44] K. Oguchi, Y. Maki, Y. Sunaga, "Three-Phase Multilevel-Voltage Source Converters with Low Switching Frequencies and Less Distorted Input Voltages", IEEE Transactions on Industry Applications, Vol. 30, No. 5, Sept./Oct. 1994, pp 1156-1165.

[45] F. Z. Peng, J.-S. Lai, J. McKeever, J. VanCoevering, "A Multilevel Voltage-Source Inverter with Separate DC Sources for Static Var Generation", IEEE Conference Proceedings IAS'95, 1995, pp 2541-2548.

[46] F. Z. Peng, J.-S. Lai, J. McKeever, J. VanCoevering, "A Multilevel Voltage-Source Converter System with Balanced DC Voltages", IEEE Conference Proceedings PESC'95, 1995, pp 1144-1150.

[47] E. K. H. van der Pols, J. D. L. Haesakkers, "DESIGN AND IMPLEMENTATION OF A PULSE WIDTH MODULATOR FOR A THREE-LEVEL INVERTER USING A MICROPROCESSOR AND EPLDS", Conference Proceedings EPE'93, Brighton, pp 146-151.

[48] R. Rojas, T. Ohnishi, T. Suzuki, "An Improved Voltage Vector Control Method for Neutral-Point-Clamped Inverters", IEEE Conference Proceedings PESC'94, 1994, pp 951-957.

[49] R. Rojas, T. Ohnishi, T. Suzuki, "PWM control method for a four-level inverter", IEE Proceedings Electric Power Applications, Vol. 142, No.6, November 1995, pp 390-396.

[50] R. Rohas, T. Ohnishi, T. Suzuki, "Neutral-Point-Clamped Inverter with Improved Voltage Waveform and Control Range", IEEE Transactions on Industrial Electronics, Vol. 42, No. 6, Dec. 1995, pp 587-594.

[51] R. Rohas, T. Ohnishi, T. Suzuki, "An Improved Voltage Vector Control Method of Neutral-Point-Clamped Inverters", IEEE Transactions on Power Electronics, Vol. 10, No. 6, Nov. 1995, pp 666-672.

[52] A. –Ch. Rufer, N. Schibli, Ch. Briguet, "A DIRECT COUPLED 4-QUADRANT MULTILEVEL CONVERTER FOR 16 2/3 TRACTION SYSTEMS", IEE Conference Proceedings PEVD'96, Nottingham UK, pp 448-453.

[53] T. Schütze, V. Strönisch, "LOW FLOOR TRAMS WITH IGBT-3-LEVEL INVERTER", Conference Proceedings EPE'93, Brighton, Vol. 1, 1993, pp 92-96.

[54] G. Sinha, T. A. Lipo, "A Four-Level Rectifier-Inverter System for Drive Applications", IEEE Industry Applications Magazine, Vol. 4, No. 1, Jan/Feb 1998, pp 66-74.

[55] J. K. Steinke, "CONTROL OF A NEUTRAL-POINT-CLAMPED PWM INVERTER FOR HIGH POWER AC TRACTION DRIVES", IEE Conference Proceedings PEVD'88, pp 214-217.

[56] J. K. Steinke, "CONTORL STRATEGY FOR THREE PHASE AC TRACTION DRIVE WITH THREE-LEVEL GTO PWM INVERTER", IEEE Conference Proceedings PESC'88, April 1988, pp 431-438.

[57] J. K. Steinke, "PWM CONTROL OF A THREE-LEVEL INVERTER – Principles and practical experience", IEE Conference Proceedings PEVD'90 , London, 1990, pp 98-103.

[58] J. K. Steinke, "SWITCHING FREQUENCY OPTIMAL PWM CONTROL OF A THREE-LEVEL INVERTER", Conference Proceedings EPE'89, Aachen, 1989, pp 1267-1272.

[59] J. K. Steinke, "Switching Frequency Optimal PWM Control of a Three-Level Inverter", IEEE Transactions on Power Electronics, Vol. 7, No. 3, July 1992, pp 487-496.

[60] Y. Tadros, G. Junge, S. Salama, "DESIGN ASPECTS OF HIGH POWER PWM INVERTERS WITH IGBT", Conference Proceedings EPE'91, Firenze, Vol. 2, 1991, pp 83-88.

[61] Y. Tadros, S. Salama, R. Höf, "THREE LEVEL IGBT INVERTER", IEEE Conference Proceedings PESC'92, 1992, pp 46-52.

[62] Y. Tadros, S. Salama, Th. Schütze, "Three Level IGBT Inverters for Industrial Drives and Traction Applications", EPE Journal, Vol. 4, No. 2, June 1994, pp 39-42.

[63] B. Velaerts, P. Mathys, E. Tatakis, G.Bingen, "A NOVEL APPROACH TO THE GENERATION AND OPTIMISATION OF THREE-LEVEL PWM WAVE FORMS", Conference Proceedings PESC'88, April 1988, pp 1255-1262.

[64] B. Velaerts, P. Mathys, G. Bingen, "NEW DEVELOPMENTS OF 3-LEVEL PWM STRATEGIES", Conference Proceedings EPE'89, Aachen, 1989, pp 411-416.

[65] B. Velaerts, P. Mathys, Z. F. Zendaoui, "STUDY OF 2 AND 3-LEVEL PRECALCULATED MODULATIONS", Conference Proceedings EPE'91, Firenze, Vol. 3, 1991, pp 228-234.

[66] A. M. Walczyna, R. J. Hill, "SPACE VECTOR PWM STRATEGY FOR 3-LEVEL INVERTERS WITH DIRECT SELF-CONTROL", Conference Proceedings EPE'93, Brighton, 1993, pp 152-157.

[67] P. W. Wheeler, C. Newton, "AN INVESTIGATION OF THE TURN-OFF CHARACTERISTICS OF AN IGBT UNDER SHORT CIRCUIT CONDITIONS", Conference Proceedings EPE'97, Trondheim, 1997, Vol. 4, pp 29-33.

B1.3 Books and Theses

[1] N. Mohan, T. M. Underland, W. P. Robbins, "Power Electronics: Converters, Applications and Design", John Wiley & Sons Inc, 1989

[2] S. B. Dewan, G. R. Slemon, A. Straughen, "Power Semiconductor Drives", J. Wiley & Sons, 1984

[3] M. G. Say, "The performance and design of alternating current machines", Sir Isaac Pitman & Sons Ltd, 1957.

[4] "80C166 Microcontroller User Manual", Siemens AC, 1990

[5] "Matlab Reference Guide", The Math Works Inc., 1992.

[6] "Simulink User's Guide", The Math Works Inc., 1992.

[7] W. Leonhard, "Control of Electrical Drives", Springer-Verlag, 1985.

[8] R. B. Giménez, "High Performance Sensorless Vector Control of Induction Motor Drives" PhD Thesis, University of Nottingham, 1995.

[9] W. Fordham Cooper, D. A. Dolby Jones, "Electrical Safety Engineering", Butterworth Heinemann, 3rd Edition, 1993.