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Model Predictive Control for advanced multilevel power converters in Smart-Grid applications

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"Available energy is the main object at stake in the struggle for existence and the evolution of the world."

Ludwig Boltzmann (1844-1906)

ABSTRACT

In the coming decades, electrical energy networks will gradually change from a traditional passive network into an active bidirectional one using concepts such as these associated with the smart grid.

Power electronics will play an important role in these changes. The inherent ability to control power flow and respond to highly dynamic network will be vital. Modular power electronics structures which can be reconfigured for a variety of applications promote economies of scale and technical advantages such as redundancy. The control of the energy flow through these converters has been much researched over the last 20 years.

This thesis presents novel control concepts for such a structure, focusing mainly on the control of a Cascaded H-Bridge converter, configured to function as a solid state substation. The work considers the derivation and application of Dead Beat and Model Predictive controllers for this application and scrutinises the technical advantages and potential application issues of these methodologies. Moreover an improvement to the standard Model Predictive Control algorithm that include an intrinsic modulation scheme inside the controller and named Modulated Model Predictive Control is introduced.

Detailed technical work is supported by Matlab/Simulink model based simulations and validated by experimental work on two converter platforms, considering both ideal and non-ideal electrical network conditions.

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HV	High Voltage
MV	Medium Voltage
LV	Low Voltage
DG	Distributed Generation
RES	Renewable Energy Sources
DSOs	Distribution System Operators
PV	Photovoltaic
LVRT	Low Voltage Ride Through
FACTS	Flexible AC Transmission System
STATCOM	Static Synchronous Compensator
PHEV	Plug-In Hybrid Electric Vehicles
PEV	Plug-In Electric Vehicles
HVDC	High Voltage DC
SCADA	Supervisory Control and Data Acquisition
AMI	Advanced Metering Infrastructure
ICT	Information and Communication Technologies
IGBT	Insulated Gate Bipolar Transistor
SiC	Silicon Carbide
THD	Total Harmonic Distortion
NPC	Neutral Point Clamped
FC	Flying Capacitor
CHB	Cascaded H-Bridge
M^2C	Modular Multilevel Converter
HB	H-Bridge
SST	Solid State Transformer
UNIFLEX-PM	Universal and Flexible Power Management
DSP	Digital Signal Processor
PI	Proportional Integral
PLL	Phase Locked Loop
PR	Proportional Resonant
DBC	Dead-Beat Control
MPC	Model Predictive Control
FCS-MPC	Finite Control Set Model Predictive Control
P-DTC	Predictive Direct Torque Control

PWM	Pulse Width Modulation
PSCM	Phase Shifted Carrier Modulation
LSCM	Level Shifted Carrier Modulation
SVM	Space Vector Modulation
SHE	Selective Harmonic Elimination
SVC	Space Vector Control
DCM	Distributed Commutation Modulation
M^2PC	Modulated Model Predictive Control
LPF	Low Pass Filter
SOGI	Second Order Generalized Integrator
SSLKF	Steady State Linear Kalman Filter
FPGA	Field Programmable Gate array
FIFO	First In First Out
PIR	PI+Resonant
PR	P+Resonant
FLL	Frequency Locked Loop
RMS	Root Mean Square

a	SSLKF PLL phase angle derivative
a_1	1DM voltage error between the first selected voltage vector and the voltage reference
a_2	1DM voltage error between the second selected voltage vector and the voltage reference
A	SSLKF PLL state matrix
c	SSLKF PLL output matrix
c_{ij}	Normalized modulation index correction factor of the i^{th} HB of phase p i = 1,2 , p = A,B,C
C	DC-Link capacitance
C_{eq}	Equivalent capacitance when the DAB converter dynamics is neglected
C_x	DC-Link capacitors x = 1,2,3,…
dv_{ip}	DCM normalized voltage error on port i, phase p i = 1,2,3 , p = A,B,C
D	Phase-Shift between the PWM signals on the two sides of the DAB converter
D_x	Diodes x = 1,2,3,…
D_+	One step ahead derivative approximation operator
D_-	One step behind derivative approximation operator
D_c	Centered derivative approximation operator
D_1	Fifth order derivative approximation operator
e	DC voltage error between the two sides of the DAB converter
e_{PLL}	SSLKF PLL voltage error
E_+	Normalized one step ahead derivative approximation error
E_c	Normalized centered derivative approximation error
E_1	Normalized fifth order derivative approximation error
f_s	Overall sampling frequency of the UNIFLEX-PM
$f_{sw,HB}$	HB switching frequency of the UNIFLEX-PM
$f_{sw,Q}$	Single device switching frequency of the UNIFLEX-PM
f_{sw}	Overall switching frequency of the UNIFLEX-PM converter per phase
$f_{sw}{}^{DC/DC}$	Switching frequency of the DC/DC converter
g	SSLKF PLL steady state gain
g_n	SSLKF PLL gain sequence
G_{PI}	PI controller transfer function
G_{PIR}	PIR controller transfer function
G_{PR}	PR controller transfer function
G_R	Resonant controller transfer function

G_C	Controller transfer function
G_{PLANT}	Plant transfer function
G_{ip}	MPC cost function on UNIFLEX-PM port *i*, phase *p* *i* = 1,2 , *p* = A,B,C
G_{Iip}	MPC current cost function on UNIFLEX-PM port *i*, phase *p* *i* = 1,2 , *p* = A,B,C
G_{Vip}	MPC DC-Link voltage cost function on UNIFLEX-PM port *i*, phase *p* *i* = 1,2 , *p* = A,B,C
$G_{Iip}^{(1)}$	M²PC current cost function on UNIFLEX-PM port *i*, phase *p* for the first selected vector *i* = 1,2 , *p* = A,B,C
$G_{Vip}^{(1)}$	M²PC DC-Link voltage cost function on UNIFLEX-PM port *i*, phase *p* for the first selected vector *i* = 1,2 , *p* = A,B,C
$G_{Iip}^{(2)}$	M²PC current cost function on UNIFLEX-PM port *i*, phase *p* for the second selected vector *i* = 1,2 , *p* = A,B,C
$G_{Vip}^{(2)}$	M²PC DC-Link voltage cost function on UNIFLEX-PM port *i*, phase *p* for the first second vector *i* = 1,2 , *p* = A,B,C
G_{MPC}	MPC DC- cost function
G_{M2PC}	M²PC DC- cost function
h_x	Fifth order derivative approximation coefficients *x* = 1,2,3,4,5
H_d	SOGI direct component transfer function
H_q	SOGI quadrature component transfer function
i	AC Current
i^I	Analytical expression of the first AC current derivative
$\vec{\imath}$	AC current vector on UNIFLEX-PM port 1
i_p	AC current on phase *p* *p* = *A*,*B*,*C*
i_p^*	AC current reference on phase *p* *p* = *A*,*B*,*C*
i_{ip}	AC current on UNIFLEX-PM converter port *i*, phase *p* *i* = 1,2 , *p* = *A*,*B*,*C*
$i_{ip}^{(1)}$	AC current on UNIFLEX-PM converter port *i*, phase *p* for the first vector selected by M²PC *i* = 1,2 , *p* = *A*,*B*,*C*
$i_{ip}^{(2)}$	AC current on UNIFLEX-PM converter port *i*, phase *p* for the second vector selected by M²PC *i* = 1,2 , *p* = *A*,*B*,*C*
i_{ip}^{avg}	AC average current applied by MPC on UNIFLEX-PM converter port *i*, phase *p* during one sampling interval *i* = 1,2 , *p* = *A*,*B*,*C*

i_{ip}^{*}	AC current reference on UNIFLEX-PM converter port *i*, phase *p* $i = 1,2 \quad , \quad p = A,B,C$
i_{ip}^{*avg}	AC average current reference applied by MPC on UNIFLEX-PM converter port *i*, phase *p* $i = 1,2 \quad , \quad p = A,B,C$
i_{abc}	Line currents on the three phases
$i_{\alpha\beta}$	Line currents on the three phases in static reference frame
i_{α}	AC current real component in stationary reference frame
i_{α}^{*}	Real component of the current reference in stationary reference frame
$i_{\alpha\beta}^{neg}$	Negative sequence of line currents on the three phases in stationary reference frame
$i_{\alpha\beta}^{pos}$	Positive sequence of line currents on the three phases in stationary reference frame
i_{β}	AC current imaginary component in stationary reference frame
i_{β}^{*}	Imaginary component of the current reference in stationary reference frame
I_{Cjp}	Current flowing through the equivalent DC-Link capacitor connected to the j^{th} H-Bridge of UNIFLEX-PM converter phase *p* $j = 1,2,3 \quad , \quad p = A,B,C$
$I_{C,p}$	Current flowing through the equivalent DC-Link capacitor connected to the UNIFLEX-PM converter phase *p* $p = A,B,C$
$I_{Rc,p}$	Current flowing through the equivalent DC-Link resistance connected to the UNIFLEX-PM converter phase *p* $p = A,B,C$
$I_{d,neg}$	Negative sequence / direct component of line currents on the three phases in synchronous reference frame
$I_{d,pos}$	Positive sequence / direct component of line currents on the three phases in synchronous reference frame
I_{peak}	AC current peak value
$I_{q,neg}$	Negative sequence / quadrature component of line currents on the three phases in synchronous reference frame
$I_{q,pos}$	Positive sequence / quadrature component of line currents on the three phases in synchronous reference frame
$I_{d,neg}^{*}$	Negative sequence / direct component current reference in synchronous reference frame
$I_{d,pos}^{*}$	Positive sequence / direct component current reference in synchronous reference frame
I_{d}	AC current direct component in synchronous reference frame
I_{d}^{*}	Direct component of the current reference in synchronous reference frame
I_{dq}^{neg}	Negative sequence of line currents on the three phases in synchronous reference frame
I_{dq}^{pos}	Positive sequence of line currents on the three phases in synchronous reference frame

I_p^*	Current reference amplitude on phase *p* *p* = A,B,C
$I_{q,neg}^*$	Negative sequence / quadrature component current reference in synchronous reference frame
$I_{q,pos}^*$	Positive sequence / quadrature component current reference in synchronous reference frame
I_q	AC current quadrature component in synchronous reference frame
I_q^*	Quadrature component of the current reference in synchronous reference frame
j	Complex variable
k	Discrete time variable
k_{ip}	DCM selected HB on port *i*, phase *p* *i* = 1,2 , *p* = A,B,C
k_{SOGI}	SOGI gain value
K_I	Integral gain of PI and PIR controllers
K_P	Proportional gain of PI, PIR and PR controllers
K_R	Resonance gain of PR and PIR controllers
K_{ip}	M^2PC switching time calculation constant on UNIFLEX-PM port *i*, phase *p* control *i* = 1,2 , *p* = *A*,*B*,*C*
L	AC Line inductance
$L_{leakage}$	Leakage inductance of DAB converter MF transformer
m_{ij}	Modulation index of the j^{th} HB of phase *p* before the DC-Balancing control *j* = 1,2,3 , *p* = A,B,C
$\widehat{m}_{ij}$	Modulation index of the j^{th} HB of phase *p* after the DC-Balancing control *j* = 1,2,3 , *p* = A,B,C
O	Derivative approximation order
v	Measured active power
P^*	Active power reference
P_i	Active power flowing in UNIFLEX-PM port *i* *i* = 1,2
P^{nom}	UNIFLEX-PM rated power
qv'	SOGI generated quadrature component
qv_p'	SOGI generated quadrature component on phase *p* *p* = A,B,C
Q	Measured reactive power
Q^*	Reactive power reference
Q_L	Reactive power consumed by the line inductor *L*
Q_{cov}	SSLKF PLL covariance matrix
Q_i	Reactive power flowing in UNIFLEX-PM port *i* *i* = 1,2
r	SSLKF PLL scalar output with variance

r_L	AC Line resistance
R_c	DC-Link equivalent parallel resistance
R_{LOAD}	Load resistance in UNIFLEX-PM experimental setup
R_j	DC-Link load resistance in connected to the j[th] HB j = 1,2,3
R_d	Diode on-state resistance
R_q	Active device on-state resistance
s	Laplace variable
s_p	Modulating signal on phase p p = A,B,C
$s_p{}^{i-j}$	State of the j^{th} H-Bridge of UNIFLEX-PM converter port i, phase p i = 1,2 , j = 1,2,3 , $p = A,B,C$
s_{ip}	Total state of UNIFLEX-PM converter port i, phase p i = 1,2 , $p = A,B,C$
$s_{ip}{}^{(1)}$	Total state of UNIFLEX-PM converter port i, phase p for the first vector selected by M[2]PC i = 1,2 , $p = A,B,C$
$s_{ip}{}^{(2)}$	Total state of UNIFLEX-PM converter port i, phase p for the second vector selected by M[2]PC i = 1,2 , $p = A,B,C$
S_x	Switching devices x = 1,2,3,…
$state_{ip}(j)$	State of the j[th] HB on UNIFLEX-PM converter port i, phase p i = 1,2 , j = 1,2,3 , $p = A,B,C$
t	Time
t_k	Current time instant in the discrete variable k
t_1	1DM on time of the first selected voltage vector and the voltage reference
t_2	1DM on time of between the second selected voltage vector and the voltage reference
$t_{x,ip}$	Switching time instant inside the sampling period defined by T_m of the HB defined by k_{ip} on port i, phase p i = 1,2 , $p = A,B,C$
$t_{ip}{}^{(1)}$	Switching time instant inside the sampling period of the UNIFLEX-PM converter port i, phase p for the first vector selected by M[2]PC i = 1,2 , $p = A,B,C$
$t_{ip}{}^{(2)}$	Switching time instant inside the sampling period of the UNIFLEX-PM converter port i, phase p for the second vector selected by M[2]PC i = 1,2 , $p = A,B,C$
T_s	Sampling time of the UNIFLEX-PM CHB converter
$T_s{}^{DC/DC}$	Sampling time of the DC/DC converter
T_m	Numerical representation of the sampling period
T	Analytical tangent line equation
T_+	Tangent line equation using the one step ahead derivative approximation

T_c	Tangent line equation using the centered derivative approximation
T_1	Tangent line equation using the fifth order derivative approximation
$u_{old,ip}$	Previous switching state of the HB defined by k_{ip} on port i, phase p $i = 1,2$, $p = A,B,C$
$u_{ip,ip}$	New switching state of the HB defined by k_{ip} on port i, phase p $i = 1,2$, $p = A,B,C$
$V_{DC}{}^{*}$	DC-Link voltage reference
V_{DCp}	Equivalent DC-Link voltage reference on phase p p = A,B,C
$V_{DCp}{}^{*}$	DC-Link voltage reference on phase p p = A,B,C
$V_{DC}{}^{nom}$	UNIFLEX-PM rated capacitor voltage
$V_{DCp}{}^{i-j}$	DC-Link voltage on the j^{th} H-Bridge of UNIFLEX-PM converter port i, phase p $i = 1,2$, $j = 1,2,3$, $p = A,B,C$
$V_{DCp}{}^{j}$	DC-Link voltage on the j^{th} H-Bridge of UNIFLEX-PM converter phase p when the DAB converter dynamics is neglected $j = 1,2,3$, $p = A,B,C$
$V_{DCp}{}^{(1)}$	Prediction for the UNIFLEX-PM converter phase p equivalent DC-Link voltage for the first selected vector by M^{2}PC $p = A,B,C$
$V_{DCp}{}^{(2)}$	Prediction for the UNIFLEX-PM converter phase p equivalent DC-Link voltage for the second selected vector by M^{2}PC $p = A,B,C$
$V_d{}^{neg}$	Negative sequence / direct component of supply voltages on the three phases in synchronous reference frame
$V_d{}^{pos}$	Positive sequence / direct component of supply voltages on the three phases in synchronous reference frame
$V_{dq}{}^{neg}$	Negative sequence of supply voltages on the three phases in synchronous reference frame
$V_{dq}{}^{pos}$	Positive sequence of supply voltages on the three phases in synchronous reference frame
$V_j{}^{nom}$	UNIFLEX-PM rated peak value of the AC voltage supply (line-to-line) on port i $i = 1,2$
$V_q{}^{neg}$	Negative sequence / quadrature component of supply voltages on the three phases in synchronous reference frame
$V_q{}^{pos}$	Positive sequence / quadrature component of supply voltages on the three phases in synchronous reference frame
$v_C{}^{*}$	Converter voltage reference
$v_{Cip}{}^{*}$	Converter voltage reference on port i, phase p $i = 1,2$, $p = A,B,C$
v_{Cip}	Converter voltage on port i, phase p of UNIFLEX-PM converter $i = 1,2$, $p = A,B,C$

$v_{Cip}^{(1)}$	Converter voltage on port *i*, phase *p* of UNIFLEX-PM converter for the first vector selected by M²PC *i* = 1,2 , *p* = *A*,*B*,*C*
$v_{Cip}^{(2)}$	Converter voltage on port *i*, phase *p* of UNIFLEX-PM converter for the second vector selected by M²PC *i* = 1,2 , *p* = *A*,*B*,*C*
v_{Cip}^{avg}	Average converter voltage applied by MPC to port *i*, phase *p* of UNIFLEX-PM converter in one sampling interval *i* = 1,2 , *p* = *A*,*B*,*C*
v_p'	SOGI generated direct component on phase *p* *p* = A,B,C
v_q^*	PLL input voltage quadrature component reference value
$v_{\alpha\beta}^{neg}$	Negative sequence of supply voltages on the three phases in static reference frame
$v_{\alpha\beta}^{pos}$	Positive sequence of supply voltages on the three phases in static reference frame
$V_{DC,abc}$	DC-Link voltage on the three phases
V_{DC}	Average DC-Link voltage on the three phases
V_{DCi}	DAB converter voltage on side *i* *i* = 1,2
V_L	Voltage across the leakage inductance of DAB converter MF transformer
V_i	Voltage on side *i* of the DAB MF transformer *i* = 1,2
V_n	AVM First selected voltage vector
V_{n+1}	AVM First selected voltage vector
$V_{p,rms}$	PLL input voltage rms value on phase *p* *p* = A,B,C
V_{peak}	Supply voltage peak value
V_{rms}	PLL input voltage rms value
V_s	SSLKF PLL input voltage amplitude
$v_{ABC,f}$	Filtered supply voltages on the three phases
v_{ABC}	Supply voltages on the three phases
v_C	Converter voltage
v_{Chp}	Converter voltage produced by UNIFLEX-PM converter port *i*, phase *p* *i* = 1,2 , *p* = *A*,*B*,*C*
v_{Cd}	Direct component of the converter voltage in synchronous reference frame
v_{Cq}	Quadrature component of the converter voltage in synchronous reference frame
$v_{C\alpha}$	Real component of the converter voltage in static reference frame
$v_{C\beta}$	Imaginary component of the converter voltage in static reference frame
v_H	H-Bridge voltage
v_d	Supply voltage direct component in synchronous reference frame

v_{ip}	Supply voltage connected to UNIFLEX-PM converter port *i*, phase *p* $i = 1,2$, $p = A,B,C$
v_p	Supply voltage on phase *p* p = A,B,C
v_d	Direct component of the supply voltage in synchronous reference frame
v_q	Quadrature component of the supply voltage in synchronous reference frame
v_α	Real component of the supply voltage in static reference frame
$v_{\alpha\beta}$	Supply voltages on the three phases in static reference frame
v_β	Imaginary component of the supply voltage in static reference frame
v	Supply voltage
v'	SOGI generated direct component
v_{Nij}	Normalized voltage reference on port *i*, phase *p* $i = 1,2$, $p = A,B,C$
$v_{hb,1A}$	Normalized voltage produced by the HBs that are not selected to switch on port *i*, phase *p* $i = 1,2$, $p = A,B,C$
$V_{DCp,eff}{}^{i-j}$	Effective DC-Link voltage on the j^{th} H-Bridge of UNIFLEX-PM converter port *i*, phase *p* $i = 1,2$, $j = 1,2,3$, $p = A,B,C$
$V_{DCp}{}^{i-AVG}$	Average DC-Link voltage on UNIFLEX-PM converter port *i*, phase *p* $i = 1,2$, $p = A,B,C$
$V_{DCp}{}^{i-TOT}$	Total DC-Link voltage on UNIFLEX-PM converter port *i*, phase *p* $i = 1,2$, $p = A,B,C$
$V_{DCp}{}^{TOT}$	Total DC-Link voltage on UNIFLEX-PM converter phase *p* when the dynamic of the DAB converter is neglected $p = A,B,C$
$V_{DCp,err}{}^{i-j}$	DC-Link voltage error on the j^{th} H-Bridge of UNIFLEX-PM converter port *i*, phase *p* $i = 1,2$, $j = 1,2,3$, $p = A,B,C$
V_0	Parasitic voltage applied when zero power is flowing through the HB
V_+	Parasitic voltage applied a positive power is flowing through the HB
V_-	Parasitic voltage applied a negative power is flowing through the HB
V_d	Diode voltage drop
V_q	Active device voltage drop
$\tilde{x}_{PLL}$	SSLKF PLL state vector error
$\hat{x}_{PLL}$	SSLKF PLL estimated state vector
x_{PLL}	SSLKF PLL state vector
y_{PLL}	SSLKF PLL output vector
w_I	Current cost function weighting factor
w_V	DC-Link voltage cost function weighting factor
z	Z transformation variable

α_x	Discretised plant model coefficients x = 1,2
β_x	Dead beat control model coefficients x = 1,2
γ_x	Improved dead beat control model coefficients x = 1,2
Δ_{ij}	Modulation index correction factor of the i^{th} HB of phase j i = 1,2 , j = A,B,C
θ_e	SSLKF PLL estimated phase angle
θ_m	SSLKF PLL measured phase angle
θ_p	PLL output phase angle on phase p p = A,B,C
θ_{pi}	PLL output phase angle on phase p, port i of UNIFLEX-PM converter i = 1,2 , p = A,B,C , p = A,B,C
φ_p	Current reference phase shift on phase p p = A,B,C
φ_{pi}	Current reference phase shift on phase p, port i of UNIFLEX-PM converter i = 1,2 , p = A,B,C
ω_0	Resonance angular frequency of PR and PIR controllers
ω_{ff}	PLL feed forward angular frequency compensation term
ω_r	SOGI resonance frequency
η	SSLKF zero-mean independent Gaussian white noise on the scalar output with variance r
θ	PLL output phase angle
ξ	SSLKF zero-mean independent Gaussian white noise state vector with covariance matrix Q_{cov}
τ	Integration variable
φ	Phase shift between supply voltage and AC current
ω	Supply voltage angular frequency

Chapter 1
Introduction: The present electrical grid and the future Smart-Grid

In this chapter an introduction to the proposed work is presented. Starting from the issues in the current electrical grid and proposed solutions. The concept of a Smart-Grid is defined, highlighting the importance of power electronics in its evolution.

1.1 The present electrical grid

The current electrical grid is based on a passive structure, with unidirectional power flow from large power plants to the end user. Figure 1.1 shows the classic electrical grid architecture where the power, produced in large power plants mainly from fossil fuels and nuclear, is distributed across the network using High Voltage (HV) and Medium Voltage (MV) transmission and distribution lines connected to several substations. The MV substations are connected to a Low Voltage (LV) distribution network which provides the power to the end user.

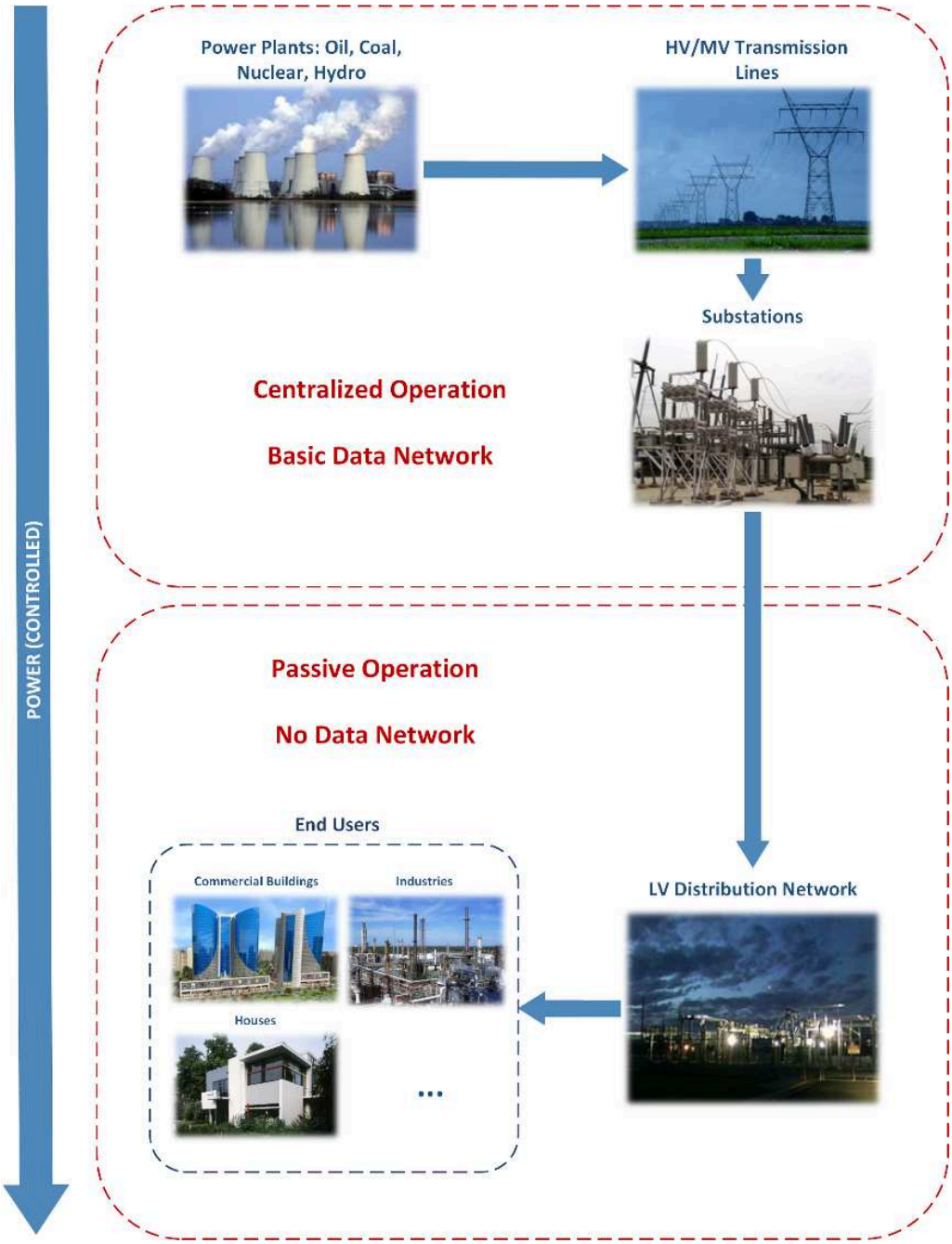


Figure 1.1 Power flow in the current electrical grid.

According to [1] the electricity grid is based on electromechanical components, such as contactors, transformers, etc., and allow unidirectional flow from the power plants and substations to distribution network. The power generation is centralised in large power plants and the distribution network is not allowed to inject power into the grid, since it has a completely passive structure. This hierarchal grid structure is subject to failure and blackouts that are difficult to locate since only few sensors are present on the grid, for protection purposes, and only at the top of the grid hierarchy. Moreover, check/test and restoration after a failure of the grid requires manual operations and cannot be completed remotely, considering the limited top level control on the activity of the grid. The energy market is typically controlled by a few operators resulting in a reduced number of customer choices.

Nowadays, with the liberalisation of the electricity market, the higher attention to green technologies, and the increasing power demand, the power system infrastructure requires changes [2]. This is partially due to the increased penetration of Distributed Generation (DG) systems into the electrical grid [2], [3]. DG technologies can be divided into Renewable Energy Sources (RES) such as solar, wind, geothermal, ocean, and non-renewable sources such as internal combustion engines, combustion turbines, combined cycle systems, micro turbines and fuel cells [3]. In the recent years the use of DG systems is increasing as a result of the many benefits that these technologies may offer in terms of infrastructure reliability [2], reduced pollution [3] and improved power quality [4].

In general, the incorporation of RES and other Distributed Generation (DG) systems presents significant advantages [2]–[4] over the traditional network, by increasing its reliability and flexibility. Since the energy is produced onsite, close to the end users, the use of DG systems may significantly reduce the congestion on the distribution and transmission lines, as well as the environmental impact of the power system infrastructure and the losses in the transmission and distribution network. Moreover, DG systems are able to provide part of the required power demands onsite, reducing the peak demand capacity required for large power plants (peak shaving). DG systems also have the potential to open the electricity production market to several Distribution System Operators (DSOs). However, several issues related with the increased use of RES and other DG have been highlighted in countries developing and implementing these

technologies [5], [6]. The traditional electrical grid shown in Figure 1.1 can be adjusted to incorporate RES and DG systems. Typically these systems are connected directly to the MV substations or to the LV distribution network, depending on the energy generation system's power rating, as shown in Figure 1.2. Unfortunately, this incorporation may result in issues which degrade the performance of the system.

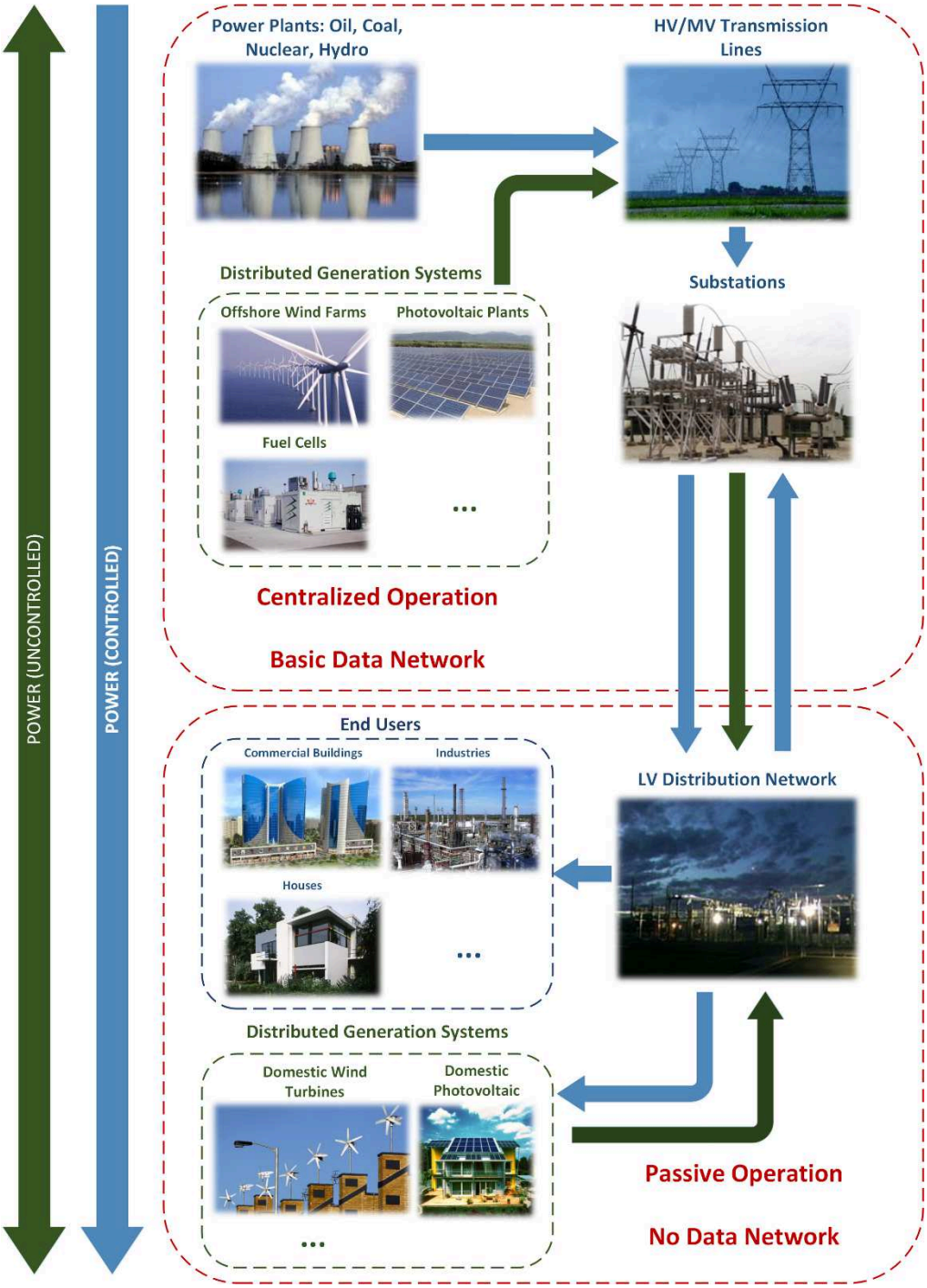


Figure 1.2 Power flow in the current electrical network with RES penetration.

When there is a high penetration of RES, or if the connection is made at a point where there is a high source impedance in the grid, the DG systems may introduce increased interruptions, voltage regulation issues, harmonic distortion, etc [4]–[6]. The case where a high penetration of Photovoltaic (PV) penetration in the German electrical grid is analysed in [6]. The German power system is well developed for the use of RES, with 25% of the electricity demand produced using RES. In particular PV plays an important role with 31GW of installed peak power (September 2012), where 70% of this represents small and medium scale systems (<30kW peak power) connected to the LV distribution network.

However, this experience with a high penetration of PV modules in the Distribution Network has highlighted issues relating to the stochastic nature of the power generation. In particular this effect may result in a reverse power flow in the Distribution Network, or from the Distribution Network to the Transmission Network, causing frequency and voltage amplitude variations and under extreme circumstances, grid instability.

Several solutions have been proposed to overcome these issues such as new interconnection requirements, lines reinforcements, transformers replacements and remote control of the PV plants [6]. In [5] the case of high penetration of wind power generation systems in Europe is analysed. As of 2004, 34GW (peak value) of wind power generation had been installed, mainly in northern Europe, resulting in a high penetration of wind power generation systems [5]. Increased interest in the installation of offshore plants has also been observed and the penetration of wind turbines in both transmission and distribution networks is expected to further increase. The main issues associated with the high penetration of wind generation are identified in [5] and include:

- Low Voltage Ride Through (LVRT) capability of high power wind farms when the voltage drops more of 20% during faults. In this case the disconnection of the wind farm might result in the violation of the Union of European Transmission System Operators security criteria.
- Power fluctuations caused by wind speed variance.
- Limitations in the installation of wind farms on lines below 100kV due to the passive structure of the distribution network.

New grid codes have been developed and are going to be applied to wind power generation systems [5]. Other studies on the potential of PV integration in the U.S. electrical grid have been carried out [7], [8]. The issues associated with the integration of DG in the electrical network are highlighted from a survey produced by DSOs in Norway in 2012 [9]. These include issues related to voltage regulation, grid instability, protection issues, and problems associated with control equipment. The DSOs are trying to overcome these issues by performing network planning aided by power flow and short-circuit analysis on the distribution network [9]. To improve the grid stability a family of devices, named Flexible AC Transmission System (FACTS), have been introduced [10], [11]. In particular Static Synchronous Compensator (STATCOM) [12] can be applied at the transmission side to ensure the best utilisation of the transmission system and improve its stability by controlling the reactive power flow through the grid at critical points [10]. However, several studies on a redesign of the electrical power grid have been carried out leading to the concept of Smart-Grid [1], [13]–[18].

1.2 The Smart Grid

In order to overcome the grid stability issues related with the DG system integration and allow the introduction of new emerging technologies, such as Plug-in Hybrid Electric Vehicles (PHEV) and Plug-in Electric Vehicles (PEV), without creating congestions in the electrical network, a redesign of the current electrical network is proposed. As part of this concept the grid will evolve from a passive structure to an active one, which allows omnidirectional power flow and presents an architecture that resembles the internet network architecture [1], [13]–[18].

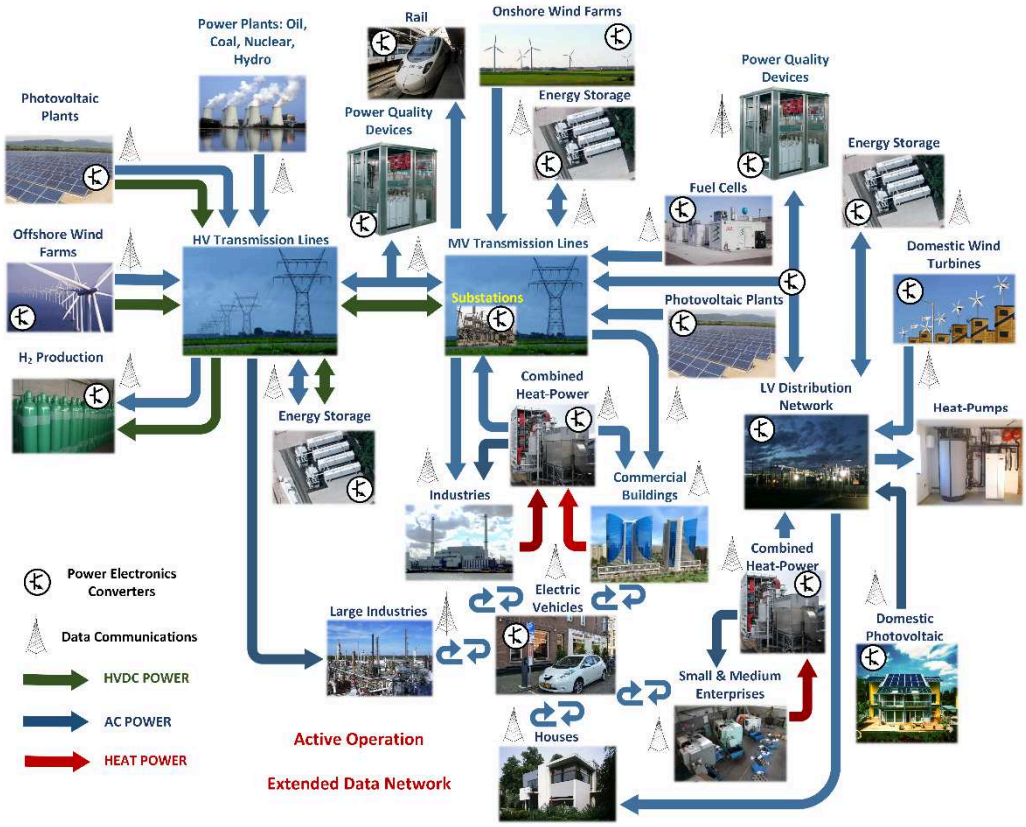


Figure 1.3 The future smart grid.

Several definitions of Smart Grid have been proposed. In [19] it is stated that "the objective of transforming the current power grid into a smart grid is to provide reliable, high quality electric power to digital societies in an environmentally friendly and sustainable way". The target of the future Smart Grid will be to achieve a high penetration of RES and DG systems, and incorporate energy storage systems, PHEV and PEV into the electrical grid whilst assuring "smart" fault detection and metering capabilities.

In order to achieve these targets, power electronic devices can replace electromechanical components into the grid to facilitate the required levels of controllability. The use of power

electronic converters will support bidirectional communication amongst the HV, MV and LV networks (via measurements, required for operation), active control of DG systems and, in general, improved grid controllability, where the network operators are able to check the status of the grid and vary the control parameters in real-time [1], [19]. Moreover, the future Smart Grid will provide a broad distribution of sensors across the network that, in conjunction with the increased controllability of the grid, will ensure Self-Monitoring and Self-Healing capabilities and an open energy market with several DSOs, giving the customers more choices [1], [19].

In conclusion, the future Smart-Grid concepts will result in the creation of a completely active network, similar to the internet in Information and Communication Technology (ICT) applications, with pervasive control and adaptability to different load conditions. As an example, when requested by the grid load conditions, the future Smart-Grid will be able to island a portion of the grid in order to improve its stability and reliability.

At the current time (2014) companies in the energy sector are working to provide efficient and reliable technologies capable of fulfil the future Smart-Grid requirements [15] and several proposals for the practical implementation of Smart-Grid technology have been considered by different countries. These projects differ depending on geographical differences [14] and, in some proposals, High Voltage DC (HVDC) transmission lines are being considered to connect remote or offshore generation sites [19] and take advantage of the peculiar RES availability of each country.

Several actions in the direction of making the grid “smarter” have already been undertaken including the use of Supervisory Control and Data Acquisition (SCADA) systems to improve the controllability of the electrical network from the top levels [17] and the use of Advanced Metering Infrastructure (AMI) to get information from the bottom level of the electrical network [20].

The definitions and concepts introduced in [1], [19] define a smart grid conceptual diagram as shown in Figure 1.3, where the power flow and data communications through the smart grid are shown. The latter is required to enable communication between any level of the electrical network and highlight recent advances in ICT and their role in future networks [21] with power electronics representing a key asset to achieve the desired controllability of the power grid [22].

Several Smart-Grid topologies have been proposed in literature. As already stated, one attractive solution is to design the future electrical grid to emulate the internet network architecture. In this case the transmission lines and the distribution network interconnect DG systems and include power electronic devices to "route the power" within the grid [18], [23]. Other topologies have also been proposed, mainly based on the interconnection of microgrids [24]–[27]. Several projects to develop smart grid technologies and applications of Smart Grid concepts between different countries are currently being undertaken [28]–[33]. As an example, the "Friends of the Supergrid" consortium is currently working on Smart Grid realisation in Europe [29]–[33].

1.3 Objectives, aims and thesis structure

The presented work aims to design, implement and evaluate predictive control techniques, in particular Dead Beat Control (DBC) and Finite Control Set Model Predictive Control (FCS-MPC), as well as Space Vector Modulation (SVM) techniques particularly suitable for high power grid connected applications utilising multilevel converters. The proposed controls and modulators are implemented and their operation validated using the 7-Level Cascaded H-Bridge (CHB) Solid State Transformer (SST) constructed during the Universal and Flexible Power Management (UNIFLEX-PM) project. The thesis is organised as it follows:

- Chapter 1: An introduction to the Smart-Grid motivations and issues is presented.
- Chapter 2: Focusing on the importance of power electronics as an enabling technology, the most common multi-level converters topologies are described and the importance of control and modulation techniques is highlighted.
- Chapter 3: Starting from the concept of a Solid State Transformer, the UNIFLEX-PM demonstrator is described in detail showing advantages and disadvantages of the proposed topology. System models are derived.
- Chapter 4: A brief description of the grid monitoring algorithms is presented starting from standard Phase Locked Loop (PLL) algorithms and proposing an improved grid monitoring system based on Steady State Linear Kalman Filter.
- Chapter 5: A literature review of control and modulation techniques for high power multi-level converter is presented. Attention has been focused on linear and predictive control techniques, such as Dead-Beat Control and Finite Control Set Model Predictive Control. Modulation methods such as carrier based Pulse Width Modulation (PWM) and Space Vector Modulation techniques are also considered.
- Chapter 6: A novel Space Vector Modulation technique, named Distributed Commutation Modulation (DCM), particularly suitable for high power Cascaded H-Bridge converters is presented. DCM can distribute the commutations equally amongst the device or actively balance the DC-Link voltage on each capacitor, depending on the application. Simulation and experimental results are shown for the proposed control and modulator in this chapter.

- Chapter 7: The implementation of DBC control on the UNIFLEX-PM demonstrator (2 port) is presented in detail focusing on the differences between the classic derivation and the proposed one. Simulation and experimental results are shown for the proposed control in this chapter.
- Chapter 8: In this chapter FCS-MPC is presented, evaluated and tested on the UNIFLEX-PM demonstrator (2 port). Starting from a FCS-MPC current control, modified for high power applications, a multi-objective FCS-MPC control is presented. Simulation and experimental results are shown for the proposed control and modulator in this chapter.
- Chapter 9: In this chapter a novel control technique, named Modulated Model Predictive Control (M^2PC), is proposed to overcome the issues of the classic FCS-MPC control derivation, including a suitable modulation technique in the MPC algorithm. Simulation and experimental results are shown for the proposed control and modulator in this chapter.
- Chapter 10: Conclusions about the proposed control and modulation techniques are drawn, considering the obtained performances and discussing future work in the area.

1.4 Chapter summary

In this chapter the current status of the electrical grid is described briefly and the concept of Smart-Grid is introduced to overcome the grid stability issues, which can arise from the high penetration of RESs into the grid. The concept of Smart-Grid is defined and the importance of power electronics in the implementation of Smart-Grid technologies is highlighted.

Finally an outline of the thesis structure, describing the contents of the next chapters, is illustrated.

Chapter 2
Introduction to multilevel converters topologies, control and modulation techniques.

This chapter presents the most relevant multilevel power converter topologies which are currently being considered for smart grid applications. An overview of the control and modulation of these converters is included.

2.1 The importance of power electronics in the future electrical grid: multilevel converters

Interest in power electronics is increasing, as is clear from the recent report from the Department for Business Innovation and Skills in the United Kingdom [22]. Power electronics represents a £135 billion global market which is growing at a rate of 10% per annum [22]. Power electronics includes several applications like power conversion systems for home appliances, transportation and industrial processing. Power electronics also represents a crucial enabling technology for the connection of RES to the electricity network and will play a critical role in improving the reliability and the stability of the future electrical power grid [22].

High power electronic converters are able to operate at HV, MV and LV. For LV applications it is possible to use the classic 2-level converter configurations based on silicon Insulated Gate Bipolar Transistors (IGBTs). For application at MV and HV two option are currently possible [34]:

- 2-level converters utilising a series connected MV silicon IGBTs or Silicon Carbide devices. In the case of SiC devices the technology is still under development.
- Multi-level converters with MV devices such as silicon IGBTs. In this case the technology is maturing.

Multilevel converters represent an attractive solution for high power applications using reliable medium power devices already available on the market [34]. Moreover, multilevel converters present several advantages with respect to the classic two-level converter in terms of output power quality and, as a consequence, filtering requirements [34]. Several topologies for multilevel converters have been proposed, with some configurations boasting bidirectional operation (with the converter allowing bidirectional power flow) and others unidirectional (with the power flowing only from one side to another of the converter) converters [34]–[37].

In Figure 2.1 the four main topologies for multilevel converters, including a schematic for each 5-level inverter (DC/AC) phase leg, are introduced. The main topologies considered are the Diode Clamped, Flying Capacitor (FC), Cascaded H-Bridge (CHB) and Modular Multilevel (M^2C) converters.

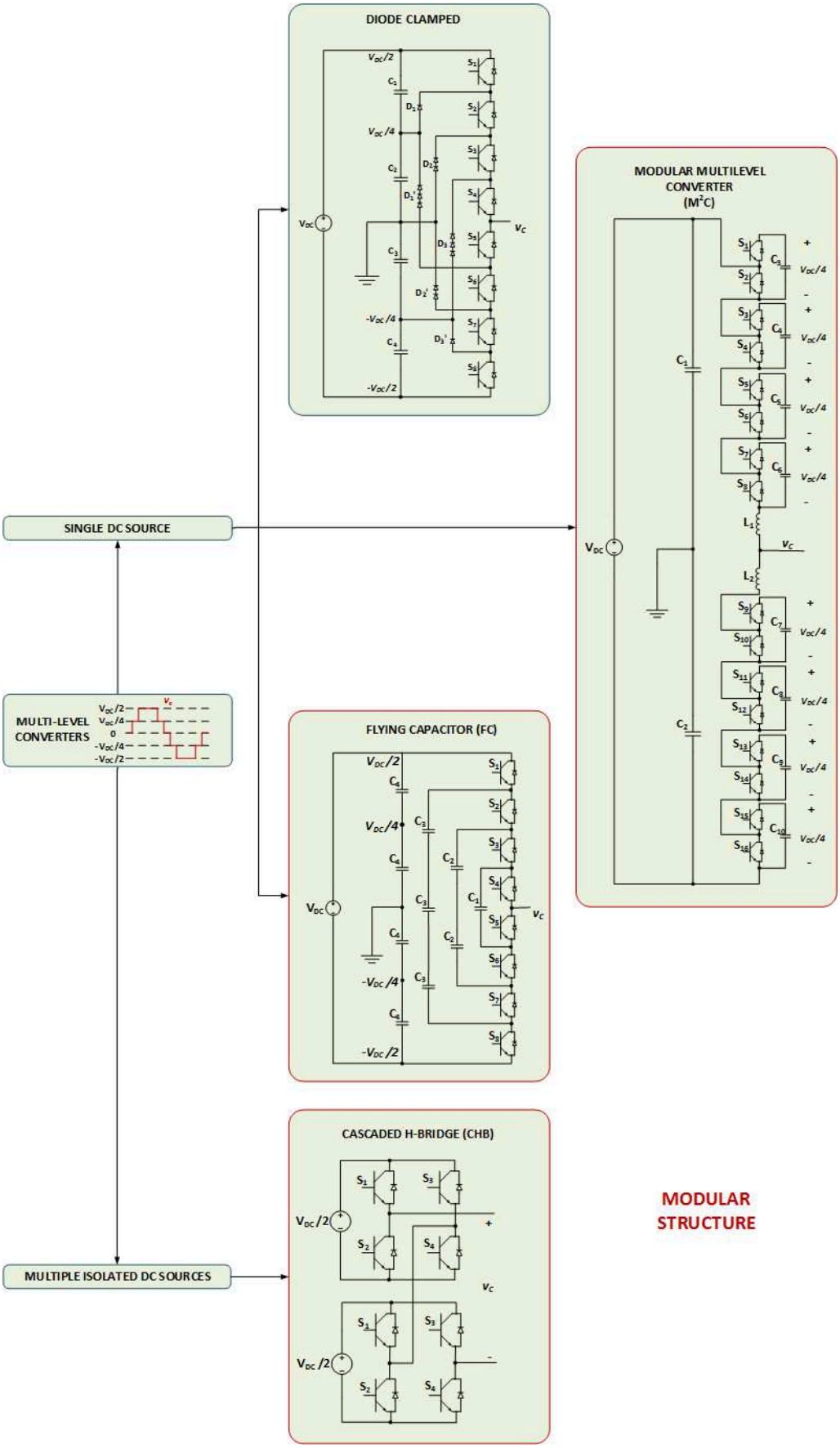


Figure 2.1 Multilevel converters topologies: schematics of 5-level inverters phase legs.

2.1.1 Diode Clamped converter

Introduced for the first time by A. Nabae, I. Takahashi and H. Akagi in 1981 [38], the Diode Clamped converter, also known as Neutral Point Clamped (NPC) in its 5-level implementation, is based on a modification of the classic 2-level converter; adding two devices per phase [34] and using diodes to clamp the voltage across the active device at a fraction of the total DC-Link voltage [35]. This concept is shown in Figure 2.2 for a 5-level single phase configuration. In this configuration five voltage levels are possible: V_{DC}, $V_{DC}/2$, 0, $-V_{DC}/2$, $-V_{DC}$, depending on the conduction state of the devices. Table 2.1 shows the allowable converter states and the obtained output voltage for each.

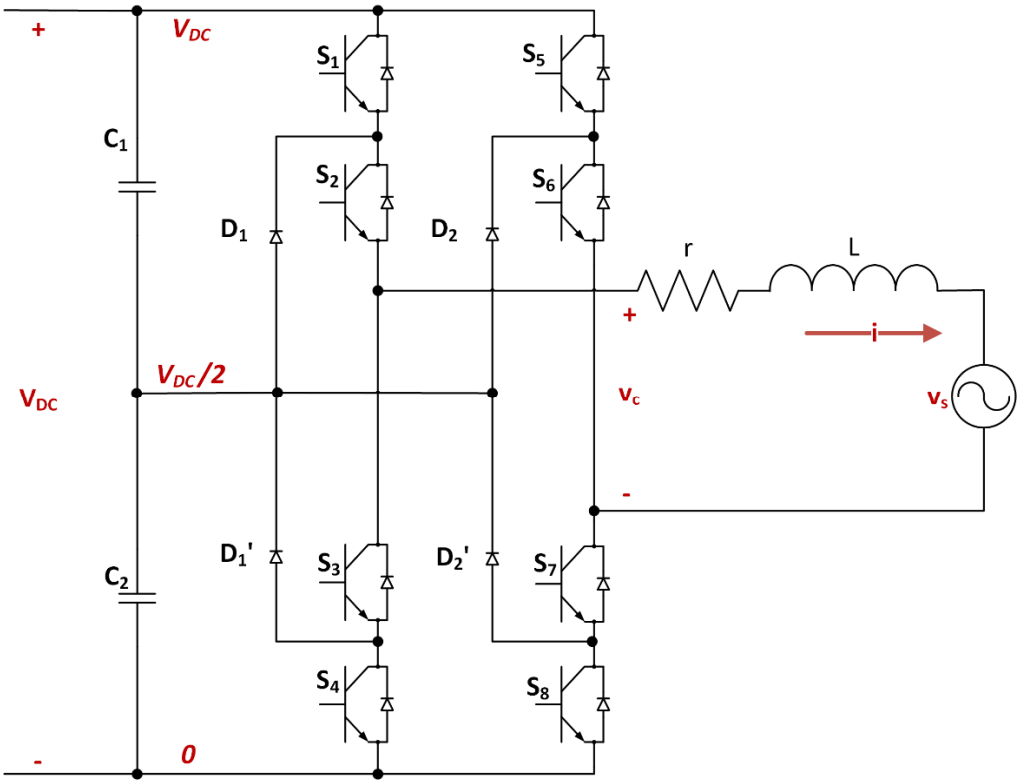


Figure 2.2 5-level, single-phase grid connected NPC converter schematic.

Clearly, the overall converter complexity increases with the number of possible converter states as shown in Table 2.2. In general an *m*-level NPC converter leg requires *(m-1)* capacitors on the DC side, *2(m-1)* active devices and *(m-1)(m-2)* diodes with same voltage rating. The resulting single-phase converter is capable of producing *(2m-1)* voltage levels [37]. Configurations with a higher number of levels are also possible, as shown in Figure 2.3 for a 9-level, single phase configuration. The voltage levels are: V_{DC}, $(3/4)V_{DC}$, $(1/2)V_{DC}$, $(1/4)V_{DC}$, 0, $-(1/4)V_{DC}$, $-(1/2)V_{DC}$, $-(3/4)V_{DC}$ and $-V_{DC}$.

Table 2.1 Possible states for a 5-level, single-phase NPC converter.

V_C	S_1	S_2	S_3	S_4	S_5	S_6	S_7	S_8
$+ V_{DC}$	1	1	0	0	0	0	1	1
$+ V_{DC}/2$	1	1	0	0	0	1	1	0
$+ V_{DC}/2$	0	1	0	1	0	0	1	1
0	1	1	0	0	1	1	0	0
0	0	1	0	1	0	1	1	0
0	0	0	1	1	0	0	1	1
$- V_{DC}/2$	0	0	1	1	0	1	1	0
$- V_{DC}/2$	0	1	0	1	1	1	0	0
$- V_{DC}$	0	0	1	1	1	1	0	0

The Diode Clamped converter provides several advantages such as high efficiency, especially when the modulation strategy implies that the devices are switched at fundamental frequency.

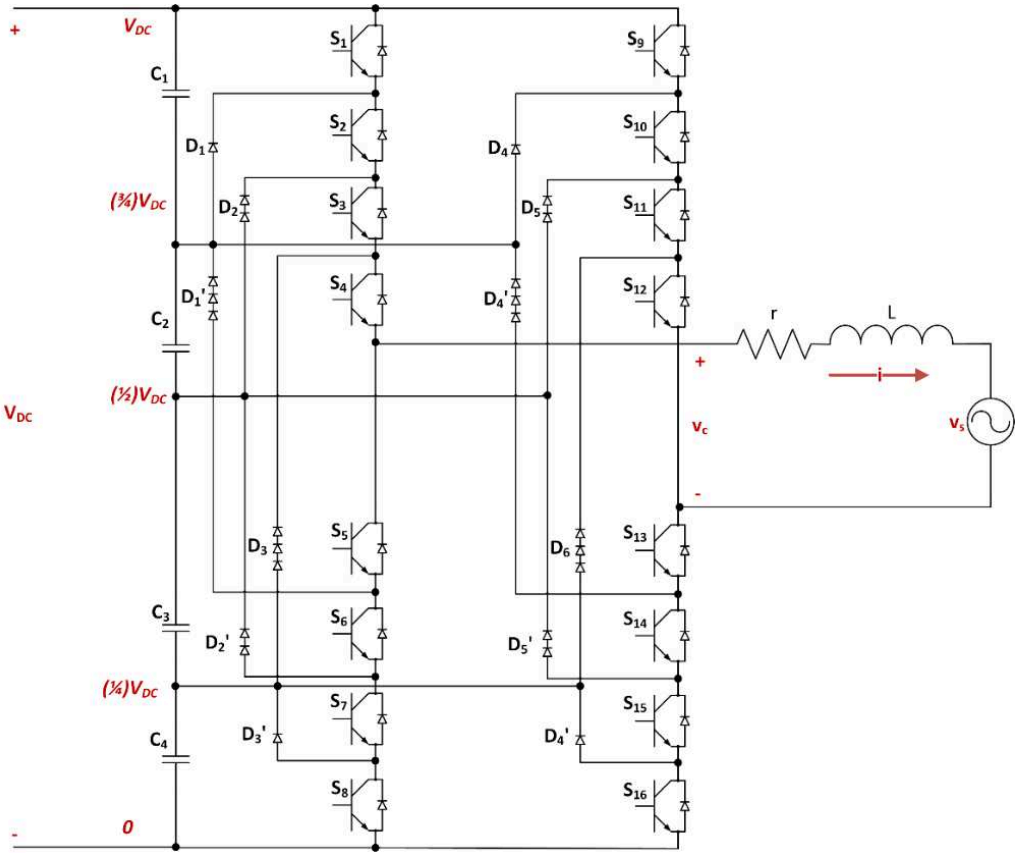


Figure 2.3 9-level, single-phase grid connected Diode Clamped converter schematic.

Table 2.2 Possible states for a 9-level, single-phase NPC converter.

V_C	S_1	S_2	S_3	S_4	S_5	S_6	S_7	S_8	S_9	S_{10}	S_{11}	S_{12}	S_{13}	S_{14}	S_{15}	S_{16}
+ V_{DC}	1	1	1	1	0	0	0	0	0	0	0	0	1	1	1	1
+(3/4) V_{DC}	0	1	1	1	1	0	0	0	0	0	0	0	1	1	1	1
+(3/4) V_{DC}	1	1	1	1	0	0	0	0	0	0	0	1	1	1	1	0
+(1/2) V_{DC}	0	0	1	1	1	1	0	0	0	0	0	0	1	1	1	1
+(1/2) V_{DC}	0	1	1	1	1	0	0	0	0	0	0	1	1	1	1	0
+(1/2) V_{DC}	1	1	1	1	0	0	0	0	0	0	1	1	1	1	0	0
+(1/4) V_{DC}	0	0	0	1	1	1	1	0	0	0	0	0	1	1	1	1
+(1/4) V_{DC}	0	0	1	1	1	1	0	0	0	0	0	1	1	1	1	0
+(1/4) V_{DC}	0	1	1	1	1	0	0	0	0	0	1	1	1	1	0	0
+(1/4) V_{DC}	1	1	1	1	0	0	0	0	0	1	1	1	1	0	0	0
0	0	0	0	0	1	1	1	1	0	0	0	0	1	1	1	1
0	0	0	0	1	1	1	1	0	0	0	0	1	1	1	1	0
0	0	0	1	1	1	1	0	0	0	0	1	1	1	1	0	0
0	0	1	1	1	1	0	0	0	0	1	1	1	1	0	0	0
0	1	1	1	1	0	0	0	0	1	1	1	1	0	0	0	0
-(1/4) V_{DC}	0	0	0	0	1	1	1	1	0	0	0	1	1	1	1	0
-(1/4) V_{DC}	0	0	0	1	1	1	1	0	0	0	1	1	1	1	0	0
-(1/4) V_{DC}	0	0	1	1	1	1	0	0	0	1	1	1	1	0	0	0
-(1/4) V_{DC}	0	1	1	1	1	0	0	0	1	1	1	1	0	0	0	0
-(1/2) V_{DC}	0	0	0	0	1	1	1	1	0	0	1	1	1	1	0	0
-(1/2) V_{DC}	0	0	0	1	1	1	1	0	0	1	1	1	1	0	0	0
-(1/2) V_{DC}	0	0	1	1	1	1	0	0	1	1	1	1	0	0	0	0
-(3/4) V_{DC}	0	0	0	0	1	1	1	1	0	1	1	1	1	0	0	0
-(3/4) V_{DC}	0	0	0	1	1	1	1	0	1	1	1	1	0	0	0	0
- V_{DC}	0	0	0	0	1	1	1	1	1	1	1	1	0	0	0	0

The voltage applied to the diodes in different parts of the circuit is variable and, as a result, in order to maintain the converter modularity, series connected diodes with the same voltage rating are used. However, the number of diodes can be reduced by using diodes with different voltage ratings. The active devices have different average conduction intervals resulting in different active devices current ratings. The capacitors on the DC bus need an appropriate voltage balancing algorithm in real applications where "natural balancing" inherent in some modulation strategies is imperfect, leading to a difference in the voltage levels [37].

However, the high number of diodes and the lack of modularity shown from the different current ratings of the active devices represent major issues when a high number of levels is required [37]. Focusing on the industrial applications the NPC converter has been successfully applied to high power AC motor drives [34], [39] and grid interfacing of RES [34], [40], [41].

2.1.2 Flying Capacitor converter

In the Flying Capacitor (FC) topology independent capacitors, instead of diodes, are used to clamp the voltage across the devices to a fraction of the total DC voltage [35] as shown in Figure 2.4 for a 5-level, single phase, converter. In this configuration five voltage levels are possible: V_{DC}, $V_{DC}/2$, 0, $-V_{DC}/2$, $-V_{DC}$, depending on the conduction state of the switching devices.

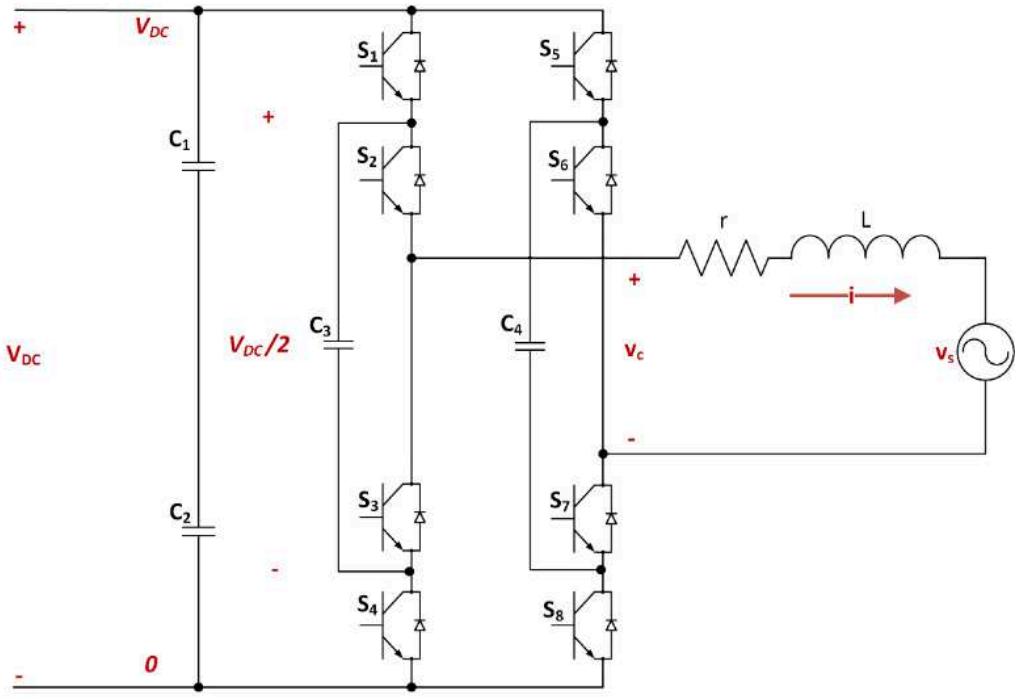


Figure 2.4 5-level, single-phase grid connected FC converter schematic.

The FC converter provides more flexibility to achieve the desired voltage output when compared to the NPC [36], as can be appreciated from Table 2.3 where the possible states of the 5-level single-phase FC converter are shown.

Table 2.3 Possible states for a 5-level, single-phase FC converter.

V_C	S_1	S_2	S_3	S_4	S_5	S_6	S_7	S_8
$+ V_{DC}$	1	1	0	0	0	0	1	1
$+ V_{DC}/2$	1	1	0	0	0	1	0	1
$+ V_{DC}/2$	1	1	0	0	1	0	1	0
$+ V_{DC}/2$	0	1	0	1	0	0	1	1
$+ V_{DC}/2$	1	0	1	0	0	0	1	1
0	1	1	0	0	1	1	0	0
0	0	1	0	1	0	1	0	1
0	1	0	1	0	1	0	1	0
0	0	0	1	1	0	0	1	1
$- V_{DC}/2$	0	1	0	1	1	1	0	0
$- V_{DC}/2$	1	0	1	0	1	1	0	0
$- V_{DC}/2$	0	0	1	1	0	1	0	1
$- V_{DC}/2$	0	0	1	1	1	0	1	0
$- V_{DC}$	0	0	1	1	1	1	0	0

Configurations with a higher number of levels are also possible as shown in Figure 2.5 for a 9-level single phase configuration. The voltage levels are: V_{DC}, $(3/4)V_{DC}$, $(1/2)V_{DC}$, $(1/4)V_{DC}$, 0, $-(1/4)V_{DC}$, $-(1/2)V_{DC}$, $-(3/4)V_{DC}$ and $-V_{DC}$. As for the NPC converter, the overall converter complexity and state redundancy increases, as shown in Table 2.4, where the possible converter states for one converter leg are shown. In general an *m*-level FC converter leg requires $(m-1)$ capacitors on the DC side plus $(m-1)(m-2)/2$ additional capacitors, $2(m-1)$ active devices. The resulting single-phase converter is able to produce $(2m-1)$ voltage levels [37]. FC converter capacitors need an appropriate capacitor voltage balancing algorithm since "natural balancing", inherent in some modulation strategies, is imperfect as a result of parameter asymmetries present in a practical realisation [37]. FC converters provide several advantages. The large capacitance may provide an additional ride through capability if a power interruption occurs. Moreover, the FC converter has a modular structure [34]. Unfortunately, when a high number of voltage levels is required, FC converters are bigger and less cost effective than other multilevel converter topologies [37]. FC converters have been applied in high-bandwidth, high switching frequency applications such as MV traction drives [34], [42].

Table 2.4 Possible states for a 9-level, single-phase FC converter leg.

V_C	S_1	S_2	S_3	S_4	S_5	S_6	S_7	S_8
V_{DC}	1	1	1	1	0	0	0	0
$(3/4)\ V_{DC}$	1	1	1	0	1	0	0	0
$(3/4)\ V_{DC}$	0	1	1	1	0	0	0	1
$(3/4)\ V_{DC}$	1	0	1	1	0	0	1	0
$(1/2)\ V_{DC}$	1	1	0	0	1	1	0	0
$(1/2)\ V_{DC}$	0	0	1	1	0	0	1	1
$(1/2)\ V_{DC}$	1	0	1	0	0	1	0	1
$(1/2)\ V_{DC}$	1	0	0	1	1	0	0	1
$(1/2)\ V_{DC}$	0	1	0	1	0	1	0	1
$(1/2)\ V_{DC}$	0	1	1	0	0	1	1	0
$(1/4)\ V_{DC}$	1	0	0	0	1	1	1	0
$(1/4)\ V_{DC}$	0	0	0	1	0	1	1	1
$(1/4)\ V_{DC}$	0	0	1	0	1	0	1	1
0	0	0	0	0	1	1	1	1

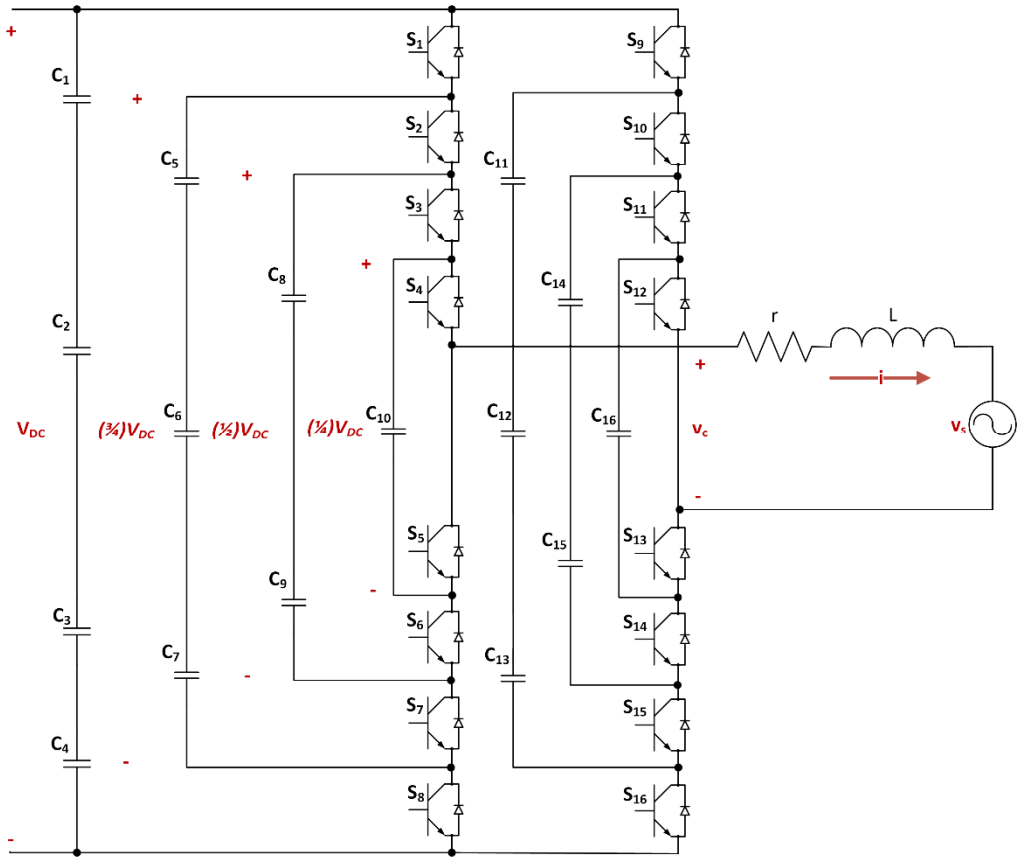


Figure 2.5 9-level, single-phase grid connected FC converter schematic.

2.1.3 Cascaded H-Bridge converter

The Cascaded H-Bridge (CHB) topology is formed from several H-Bridge (HB) cells with independent DC sources connected in series, as shown in Figure 2.6 for a 5-level single phase configuration. In Table 2.5 the allowable states of the 5-level single-phase CHB converter are shown and relate to five possible voltage levels. V_{DC}, $V_{DC}/2$, 0, $-V_{DC}/2$, $-V_{DC}$.

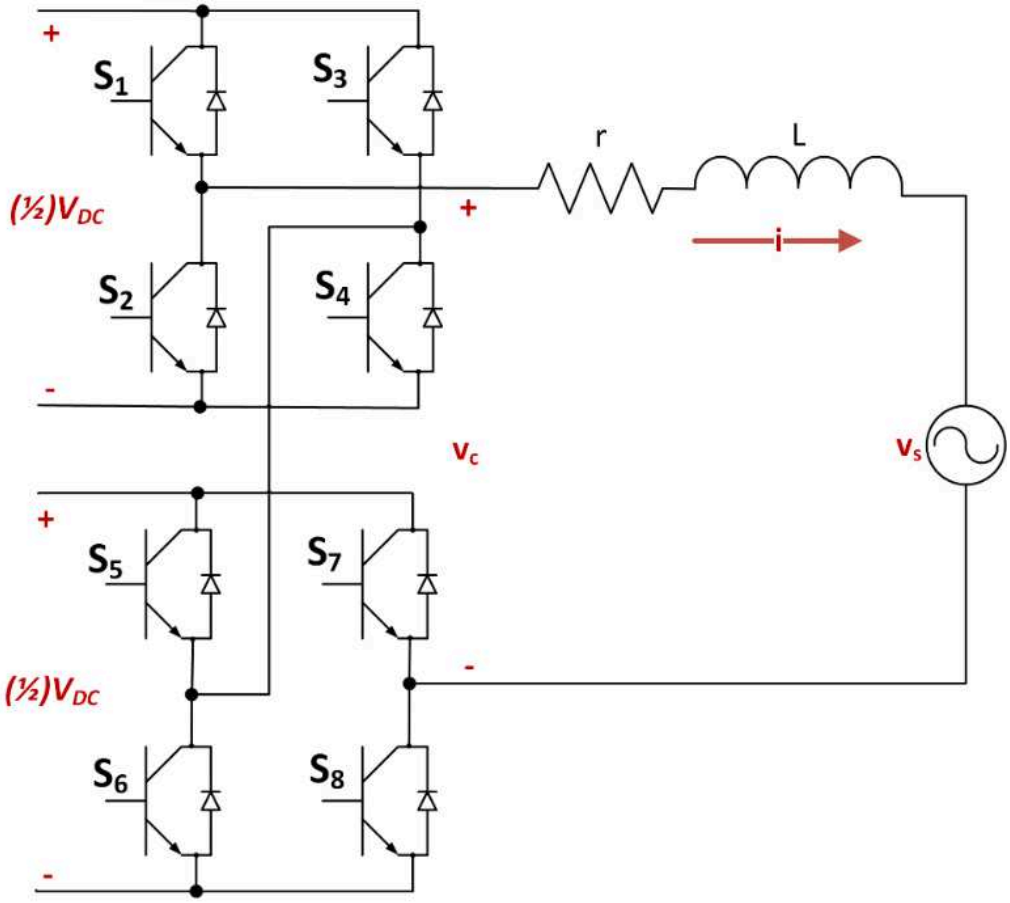


Figure 2.6 5-level, single-phase grid connected CHB converter schematic.

Configurations with a higher number of levels are also possible as shown in Figure 2.7 for a 9-level single phase configuration. The voltage levels are: V_{DC}, $(3/4)V_{DC}$, $(1/2)V_{DC}$, $(1/4)V_{DC}$, 0, $-(1/4)V_{DC}$, $-(1/2)V_{DC}$, $-(3/4)V_{DC}$ and $-V_{DC}$.

Using different notation for the single H-Bridge cell it is possible to obtain a compact notation for the CHB states. Considering Figure 2.8, the three states for the single HB are considered, *1*, *0*, *-1*, and associated with the voltage produced by the HB, respectively V_{DC}, 0, $-V_{DC}$.

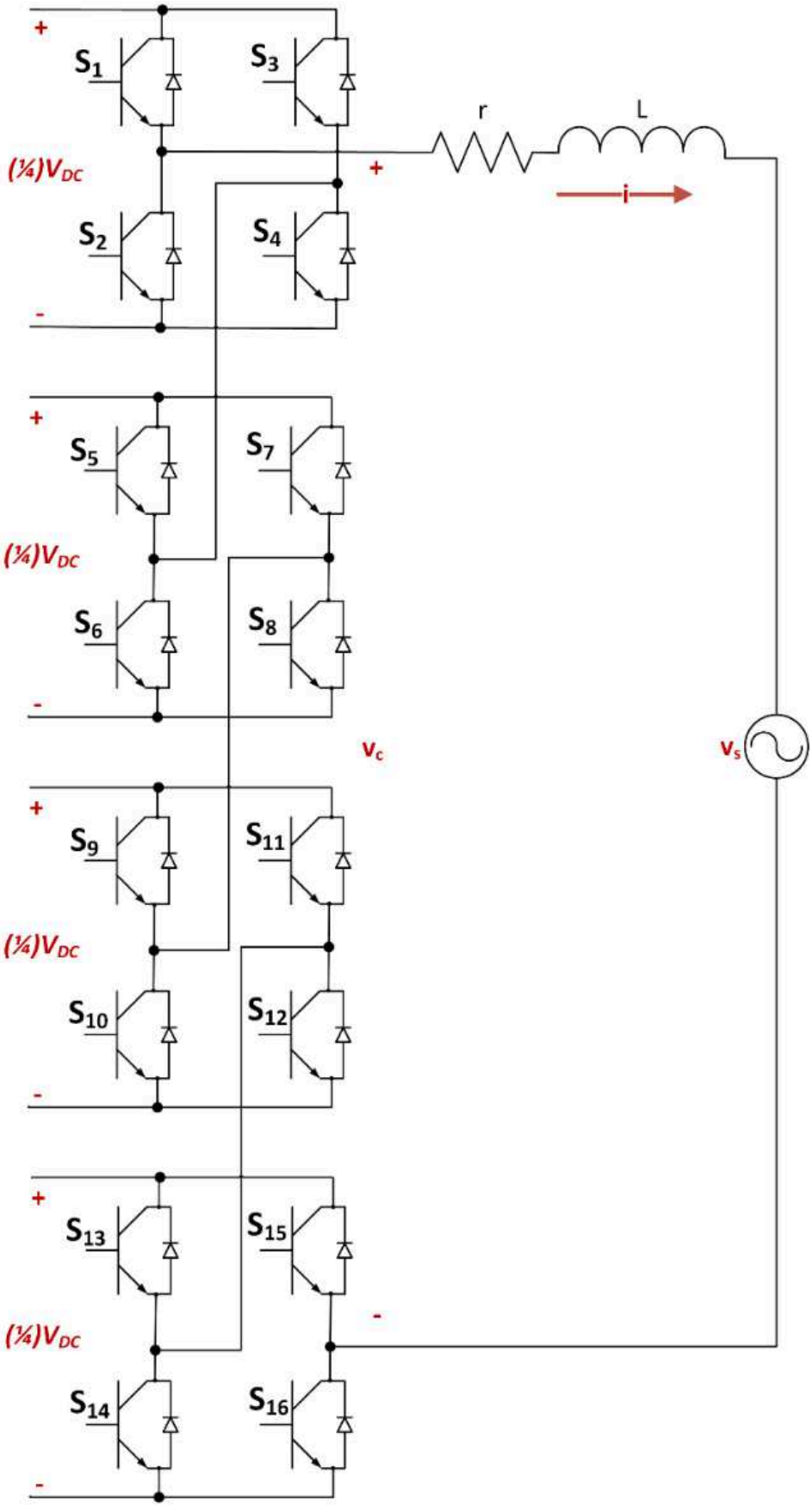


Figure 2.7 9-level, single-phase grid connected CHB converter schematic.

Table 2.5 Possible states for a5-level, single-phase CHB converter.

V_C	S_1	S_2	S_3	S_4	S_5	S_6	S_7	S_8
$+V_{DC}$	1	0	0	1	1	0	0	1
$+V_{DC}/2$	1	0	0	1	1	1	0	0
$+V_{DC}/2$	1	0	0	1	0	0	1	1
$+V_{DC}/2$	1	1	0	0	0	1	1	0
$+V_{DC}/2$	0	0	1	1	0	1	1	0
0	1	0	1	0	1	0	1	0
0	1	0	1	0	0	1	0	1
0	0	1	0	1	1	0	1	0
0	0	1	0	1	0	1	0	1
0	1	0	0	1	0	1	1	0
$-V_{DC}/2$	0	1	1	0	1	1	0	0
$-V_{DC}/2$	0	1	1	0	0	0	1	1
$-V_{DC}/2$	1	1	0	0	0	1	1	0
$-V_{DC}/2$	0	0	1	1	0	1	1	0
$-V_{DC}$	0	1	1	0	0	1	1	0

With this notation, and considering that the CHB converter produces an output voltage determined by the sum of the voltages produced from the individual HB cells [37], the composite CHB state will be equal to the sum of the single HB states.

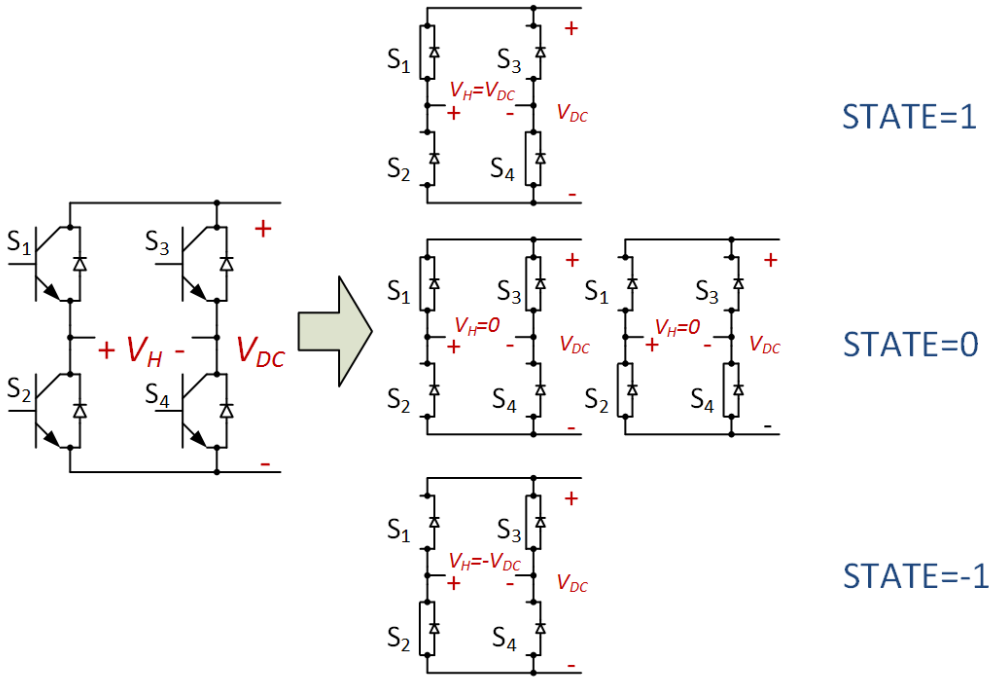


Figure 2.8 Possible switching states of a single H-Bridge.

Using this notation for the 9-level CHB shown in Figure 2.7 the states shown in Table 2.6 can be obtained. In general an *m*-level CHB converter requires *(m-1)* isolated DC sources plus *2(m-1)* active devices [37]. CHB converters avoid the need for extra clamping diodes or capacitors [37], have high modularity and require less components to achieve the same number of levels when compared to other multilevel topologies [43]. However they require isolated DC sources and the capacitors have to be rated to handle pulsating single phase power [43]. Isolated DC sources can be derived using a line frequency transformer [35] or isolated DC/DC converters [44].

The CHB converter has been commercialised for several high power (up to 31MVA) applications. These applications include active filters, reactive power compensation, PEV and PHEV, grid interfacing of photovoltaic generation, uninterruptible power supplies and magnetic resonance imaging systems [34].

Table 2.6 Possible states for a 9-level, single-phase CHB converter.

V_C	**Possible states** (HB_1, HB_2, HB_3, HB_4)
V_{DC}	(1,1,1,1)
$(3/4)\ V_{DC}$	(1,1,1,0) (1,1,0,1) (1,0,1,1) (0,1,1,1)
$(1/2)\ V_{DC}$	(1,1,0,0) (1,0,1,0) (1,0,0,1) (1,1,1,-1) (1,1,-1,1) (1,-1,1,1) (0,1,1,0) (0,1,0,1) (0,0,1,1) (-1,1,1,1)
$(1/4)\ V_{DC}$	(1,0,0,0) (1,1,0,-1) (1,-1,0,1) (1,1,-1,0) (1,-1,1,0) (1,0,1,-1) (1,0,-1,1) (0,1,0,0) (0,0,1,0) (0,0,0,1) (0,1,1,-1) (0,1,-1,1) (0,-1,1,1) (-1,1,1,0) (-1,1,0,1) (-1,0,1,1)
0	(1,-1,0,0) (1,0,-1,0) (1,0,0,-1) (1,-1,-1,1) (1,-1,1,-1) (1,1,-1,-1) (0,0,0,0) (0,1,0,-1) (0,-1,0,1) (0,1,-1,0) (0,-1,1,0) (0,0,1,-1) (0,0,-1,1) (-1,1,0,0) (-1,0,1,0) (-1,0,0,1) (-1,1,1,-1) (-1,1,-1,1) (-1,-1,1,1)
$-(1/4)\ V_{DC}$	(1,-1,-1,0) (1,-1,0,-1) (1,0,-1,-1) (0,-1,0,0) (0,0,-1,0) (0,0,0,-1) (0,-1,-1,1) (0,-1,1,-1) (0,1,-1,-1) (-1,0,0,0) (-1,1,0,-1) (-1,-1,0,1) (-1,1,-1,0) (-1,-1,1,0) (-1,0,1,-1) (-1,0,-1,1)
$-(1/2)\ V_{DC}$	(1,-1,-1,-1)(0,-1,-1,0) (0,-1,0,-1) (0,0,-1,-1)(-1,-1,0,0) (-1,0,-1,0) (-1,0,0,-1) (-1,-1,-1,1) (-1,-1,1,-1) (-1,1,-1,-1)
$-(3/4)\ V_{DC}$	(0,-1,-1,-1) (-1,-1,-1,0) (-1,-1,0,-1) (-1,0,-1,-1)
$-V_{DC}$	(-1,-1,-1-,1)

2.1.4 Modular Multilevel Converter

The Modular Multilevel Converter (M^2C) was introduced by R. Marquardt as part of a new family of multilevel converters [45]–[47]. In this topology several DC/DC modules with floating capacitors are connected in series to obtain a multilevel waveform generator [36]. In Figure 2.9 a 5-level single phase M^2C converter is shown. Each converter leg of the 5-level M^2C is composed by two arms, connected respectively to the positive and negative DC-Link terminals via a buffer inductance, *L*. Each arm is composed of two series connected half bridge cells supplied by a floating capacitor, ideally charged to $V_{DC}/2$. Gating the upper half bridge switch results in application of $V_{DC}/2$ at the cell output terminals. Alternatively, gating the bottom device bypasses the capacitor, applying 0V at the output terminals.

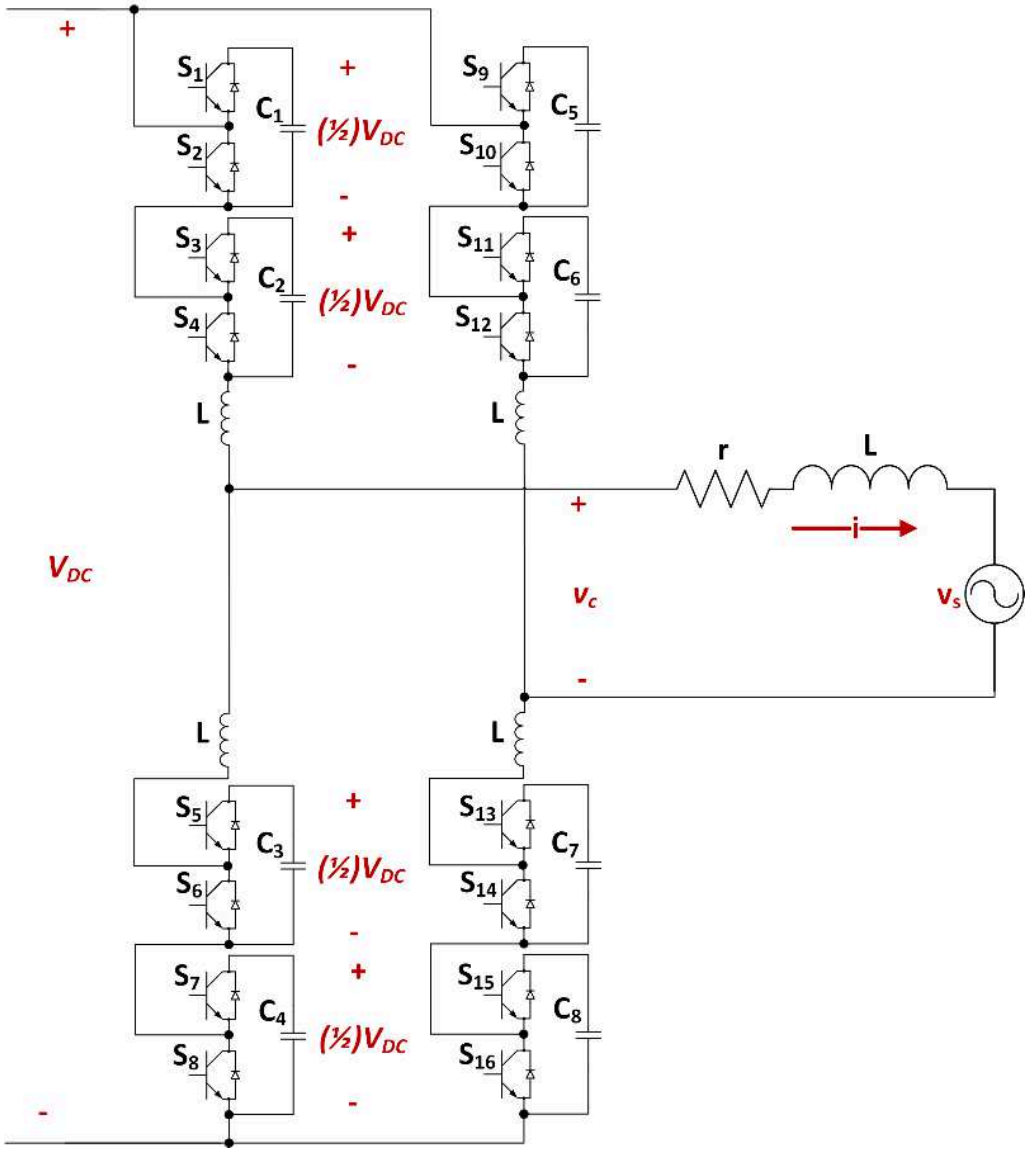


Figure 2.9 5-level, single-phase grid connected M^2C converter schematic.

Table 2.7 Possible states for a 5-level, single-phase M^2C converter leg.

V_C	S_1	S_2	S_3	S_4	S_5	S_6	S_7	S_8	S_9	S_{10}	S_{11}	S_{12}	S_{13}	S_{14}	S_{15}	S_{16}
$+V_{DC}$	0	1	0	1	1	0	1	0	1	0	1	0	0	1	0	1
$+(1/2)\,V_{DC}$	0	1	0	1	1	0	1	0	1	0	0	1	1	0	0	1
$+(1/2)\,V_{DC}$	0	1	0	1	1	0	1	0	1	0	0	1	0	1	1	0
$+(1/2)\,V_{DC}$	0	1	0	1	1	0	1	0	0	1	1	0	1	0	0	1
$+(1/2)\,V_{DC}$	0	1	0	1	1	0	1	0	0	1	1	0	0	1	1	0
$+(1/2)\,V_{DC}$	1	0	0	1	1	0	0	1	1	0	1	0	0	1	0	1
$+(1/2)\,V_{DC}$	1	0	0	1	0	1	1	0	1	0	1	0	0	1	0	1
$+(1/2)\,V_{DC}$	0	1	1	0	1	0	0	1	1	0	1	0	0	1	0	1
$+(1/2)\,V_{DC}$	0	1	1	0	0	1	1	0	1	0	1	0	0	1	0	1
0	0	1	0	1	1	0	1	0	0	1	0	1	1	0	1	0
0	1	0	1	0	0	1	0	1	1	0	1	0	0	1	0	1
0	1	0	0	1	1	0	0	1	1	0	0	1	1	0	0	1
0	1	0	0	1	1	0	0	1	1	0	0	1	0	1	1	0
0	1	0	0	1	1	0	0	1	0	1	1	0	1	0	0	1
0	1	0	0	1	1	0	0	1	0	1	1	0	0	1	1	0
0	1	0	0	1	0	1	1	0	1	0	0	1	1	0	0	1
0	1	0	0	1	0	1	1	0	1	0	0	1	0	1	1	0
0	1	0	0	1	0	1	1	0	0	1	1	0	1	0	0	1
0	1	0	0	1	0	1	1	0	0	1	1	0	0	1	1	0
0	0	1	1	0	1	0	0	1	1	0	0	1	1	0	0	1
0	0	1	1	0	1	0	0	1	1	0	0	1	0	1	1	0
0	0	1	1	0	1	0	0	1	0	1	1	0	1	0	0	1
0	0	1	1	0	1	0	0	1	0	1	1	0	0	1	1	0
0	0	1	1	0	0	1	1	0	1	0	0	1	1	0	0	1
0	0	1	1	0	0	1	1	0	1	0	0	1	0	1	1	0
0	0	1	1	0	0	1	1	0	0	1	1	0	1	0	0	1
0	0	1	1	0	0	1	1	0	0	1	1	0	0	1	1	0
$-(1/2)\,V_{DC}$	1	0	0	1	1	0	0	1	0	1	0	1	1	0	1	0
$-(1/2)\,V_{DC}$	1	0	0	1	0	1	1	0	0	1	0	1	1	0	1	0
$-(1/2)\,V_{DC}$	0	1	1	0	1	0	0	1	0	1	0	1	1	0	1	0
$-(1/2)\,V_{DC}$	0	1	1	0	0	1	1	0	0	1	0	1	1	0	1	0
$-(1/2)\,V_{DC}$	1	0	1	0	0	1	0	1	1	0	0	1	1	0	0	1
$-(1/2)\,V_{DC}$	1	0	1	0	0	1	0	1	1	0	0	1	0	1	1	0
$-(1/2)\,V_{DC}$	1	0	1	0	0	1	0	1	0	1	1	0	1	0	0	1
$-(1/2)\,V_{DC}$	1	0	1	0	0	1	0	1	0	1	1	0	0	1	1	0
$-V_{DC}$	1	0	1	0	0	1	0	1	0	1	0	1	1	0	1	0

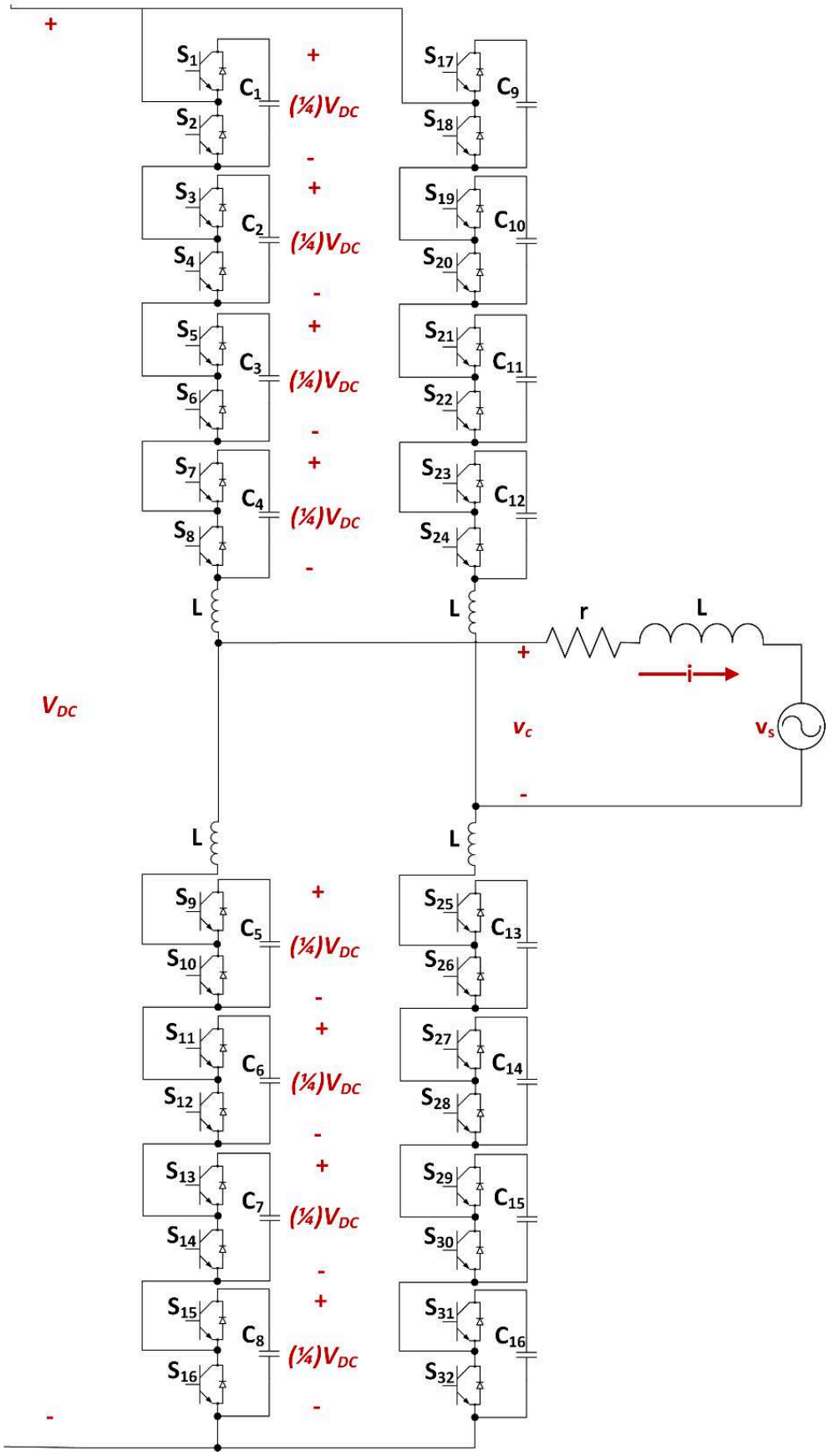


Figure 2.10 9-level, single-phase M^2C converter schematic.

The converter shown in Figure 2.9 is able to produce five possible voltage levels, respectively V_{DC}, $V_{DC}/2$, 0, $-V_{DC}/2$ and $-V_{DC}$, in accordance with Table 2.7 where the possible converter leg states, associated with the produced output voltage, are shown. The high state redundancy is mainly used to regulate the leg circulating current in order to balance the floating capacitors voltages [48]–[50]. Configurations with a higher number of levels are also possible, as shown in Figure 2.10 for a 9-level single phase configuration. The voltage levels in this case are: V_{DC}, $(3/4)V_{DC}$, $(1/2)V_{DC}$, $(1/4)V_{DC}$, 0, $-(1/4)V_{DC}$, $-(1/2)V_{DC}$, $-(3/4)V_{DC}$ and $-V_{DC}$. As a result of the high state redundancy of a M^2C, the table of the possible states for the 9 level M^2C has been omitted. In general, one leg of the M^2C converter can produce $m=(N+1)$ voltage levels where N is the number of DC/DC modules in an arm and the floating capacitors must be maintained at a voltage equal to V_{DC}/N [51].

The M^2Cs is a topology that doesn't require isolated DC sources [36], [46] and can be extended to produce a higher number of voltage levels without problems associated with capacitor voltage balancing. Furthermore, it has low conversion losses [51]. However the M^2C requires a very sophisticate control, requiring several levels of energy management. M^2Cs are a recently proposed topology that are attracting interest as a possible alternative to CHB converters in very high power applications [51], [52] and is a promising solution for Voltage Source Converter, High Voltage Direct Current (VSC-HVDC) transmission [46], [47], [53].

2.1.5 Multi-level converters for Solid State Transformer applications

In [16] a CHB converter utilising SiC devices is proposed as a Solid State Transformer (SST) for a future electrical grid as a replacement for the transformer in a medium voltage substation. SST technology provides several advantages respect to classic transformers. It uses less copper, and it's application may results in a three times size and weight reduction with respect to a classic transformer [16]. Moreover, SST allows an improved substation controllability, compared with classic transformers, by providing active control of the AC current amplitude, frequency and phase shift, resulting in an accurate active and reactive power flow control [37].

Recently a CHB converter based structure has been proposed during the Universal and Flexible Power Management (UNIFLEX-PM) project to replace the transformer in a substation, extending the concept of the SST in order to connect energy storage elements directly to the MV

substation [23]. To achieve this target, the UNIFLEX-PM demonstrator was designed with a three port structure as shown in Figure 2.11. The structure provides active and reactive power flow control across three converter ports and presents numerous advantages when compared to classical transformers in terms of power quality and voltage stability [23], [54]. Moreover the direct connection with energy storage elements may be used to support the LVRT capability of wind farms [23]. A prototype UNIFLEX-PM converter was constructed in a previous European Union project [44] and is described in detail in Chapter 3.

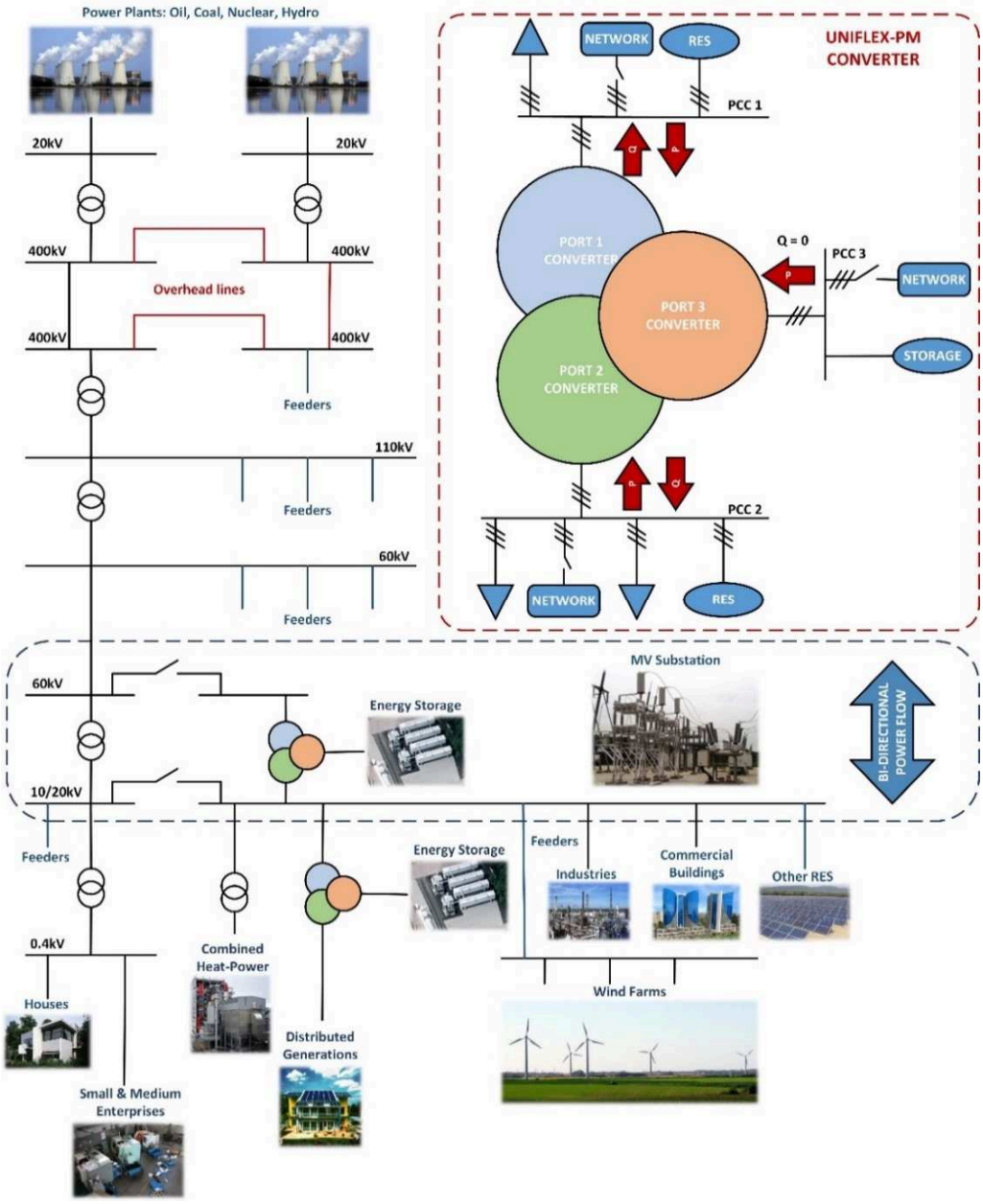


Figure 2.11 UNIFLEX-PM converter: general structure and proposed applications.

2.2 Control and modulation techniques for power converters

Power electronics converter control has attracted research interest in the recent years and several novel control techniques have been applied to different converter topologies, with the aim to improve the converter steady state and transient performances, reliability, efficiency and fault ride-trough capabilities. An overview of these techniques is given in Figure 2.12.

Improvements in microcontroller and Digital Signal Processor (DSP) technology enable the implementation of novel and more sophisticated control techniques [55] in comparison with classical linear control methods [56].

Modulation techniques have also been an active area of research over the last twenty years. In particular, when multi-level converters are considered, modulation techniques can take advantage of the increased degrees of freedom provided by the higher number of possible switching states in order to improve the converter efficiency, reliability , modularity and waveforms quality [34].

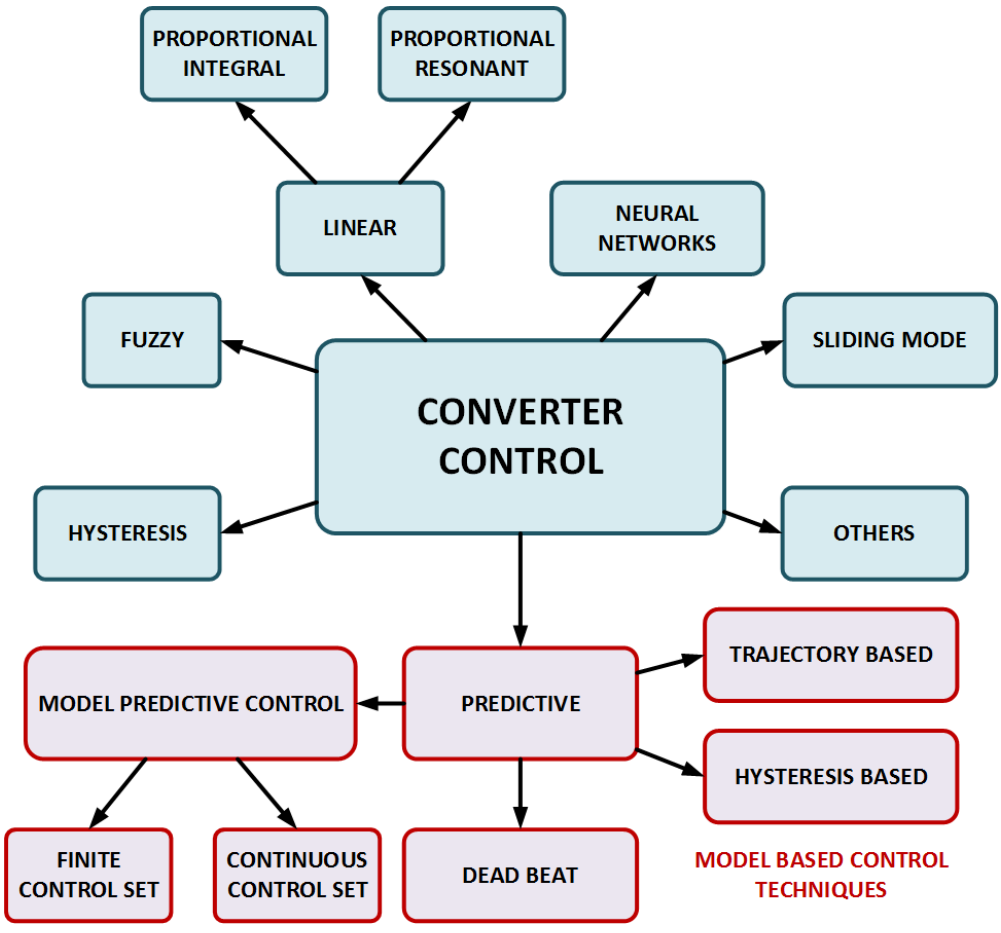


Figure 2.12 Control techniques applicable to multilevel converters.

2.2.1 Control of power converters

Classic linear control, is well established in the literature and can be implemented in natural, stationary or synchronous reference frames [56]. A general circuit for a grid connected multilevel converter is shown in Figure 2.13, and the equivalent circuits in the three possible reference frames are considered. In the case of linear control in the natural reference frame three PI error compensators are used to derive the required voltage which the converter must produce in order to obtain the desired output current. Further feed-forward corrections (utility voltage disturbances for example) or Phase-Locked-Loop (PLL) algorithms can be used to compensate current amplitude and phase errors [56]. Another option is to convert the phase currents into a rotating synchronous reference frame (direct and quadrature components or for simplicity d-q) [57], [58] obtaining two DC equivalent currents which allow currents to be controlled using two PI compensators reducing the error on the fundamental components to zero [56]. Implementation in a stationary reference frame (α-β) is also possible using variable-frequency generators to produce the reference voltages [56]. In conclusion, linear controllers based on PI compensators can produce good reference tracking performances but their dynamic response may be inferior when compared with more advanced control techniques, which can provide faster transient response [56].

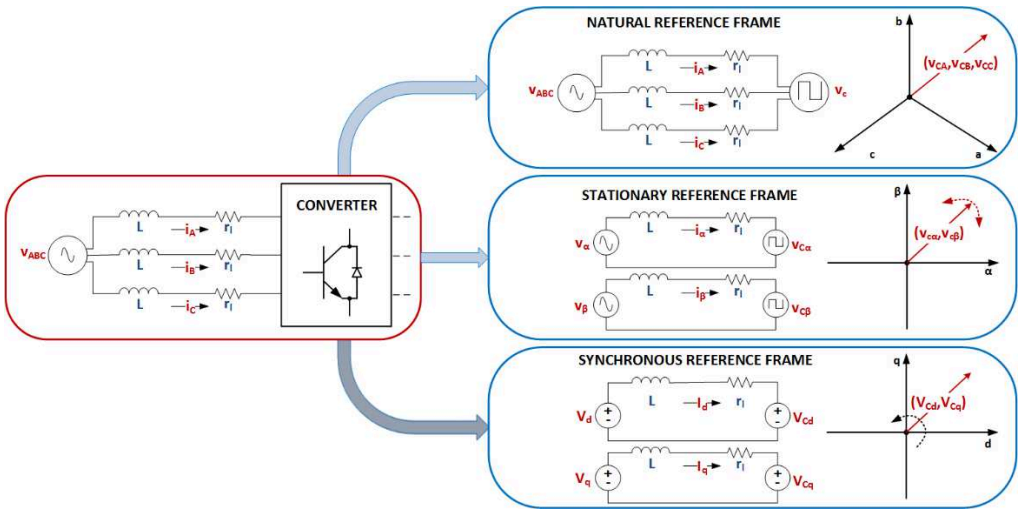


Figure 2.13 General grid connected multilevel converter structure and equivalent circuits.

Linear control using Proportional Resonant (PR) compensators has also been proposed for the control of multi-level converters in natural [59] and stationary [60] reference frames to overcome the limitation of PI controllers in term of reference tracking error and harmonic rejection [61] without using feed-forward compensations.

Hysteresis control is based on a feedback control loop using 2-level hysteresis comparators to control the phase currents to the desired references [56]. The main advantages are simplicity, robustness and good dynamic performance. However the switching frequency depends on the AC voltage and the load parameters [56]. Hysteresis control has been successfully applied to multilevel converters [62]–[66] where solutions to maintain constant the switching frequency by varying the tolerance band of the hysteresis comparator has been proposed.

More advanced control techniques such as Neural Network [67], Sliding Mode [68], Fuzzy Logic [69], [70] and Predictive [55], [71], [72] control have also been proposed in literature as potential ways to overcome the limitations of more traditional control techniques.

Predictive control techniques, and in particular Dead Beat Control (DBC) and Model Predictive Control (MPC), have attracted significant research interest [55], [71]–[98]. DBC is a well-known control technique that uses the discretised system model to calculate the optimal voltage reference value that the converter has to apply to track the desired current reference with zero error at the next sampling instant [55]. DBC control provides a faster dynamic than is possible using a discrete-time control; however DBC is very sensitive to model parameter errors and delays in the measured variables. It is also difficult to include non-linearity and other constraints in the control law [55]. DBC has been applied to current control in three-phase inverters [78], [85]–[92], rectifiers [99], back-to-back converters [93], active filters [94], power factor preregulators [95], uninterruptible power supplies [96], DC-DC converters [97] and torque control of induction machines [98].

MPC uses a discretised system model to predict the system behaviour for every possible converter state. A cost function is defined and the state that returns the minimum value of the cost function is applied during the next sampling interval [55], [72]. MPC may also consider a continuous control set; in this case a suitable modulation technique has to be included in the control system [55]. However, considering the finite number of output states of a converter, the Finite Control Set MPC (FCS-MPC) [71], [73]–[78] is usually considered because of its robustness and the absence of a modulator, resulting in a simple implementation. This is a different approach that has been successfully applied for the output current control in three-phase inverters [83], [100] and a matrix converters [80], [101], power control in active front end

rectifiers [102], [103], and torque and flux control of induction machines [98], [104]–[108]. The lack of a modulator is, unfortunately, also one of the main drawbacks of finite control set MPC because the control can choose only from a limited number of converter output voltages vectors. Furthermore, the cost function minimisation algorithm requires high computational effort [55], [71], [72]. FCS-MPC has been applied to several converter topologies and applications [77], [84], [102], [109] and more advanced schemes which include modulation techniques inside the FCS-MPC algorithm have been proposed [108], [110]–[116]. In [110]–[112] FCS-MPC current control is applied to a six-phase inverter to feed an Asymmetrical Dual Three-Phase Induction Machine while in [113], [114], [116] a Predictive Direct Power Control is applied to a three-phase voltage source converter. In [108], [115] a Predictive Direct Torque Control (P-DTC) approach is described. In all these study cases, the duty cycles are calculated by solving an optimisation problem. This approach determines the optimal control action in order to track the desired reference with minimal error. Multi-objective control can become rather complex since a solution to a multidimensional optimisation problem must be found. Linear and predictive control techniques are described in detail in Chapter 5.

2.2.2 Modulation techniques for multi-level converters

Several modulation strategies for multi-level converters have been developed for different converter topologies and applications, and those can be classified depending on the device switching frequency they produce [35], as shown in Figure 2.14.

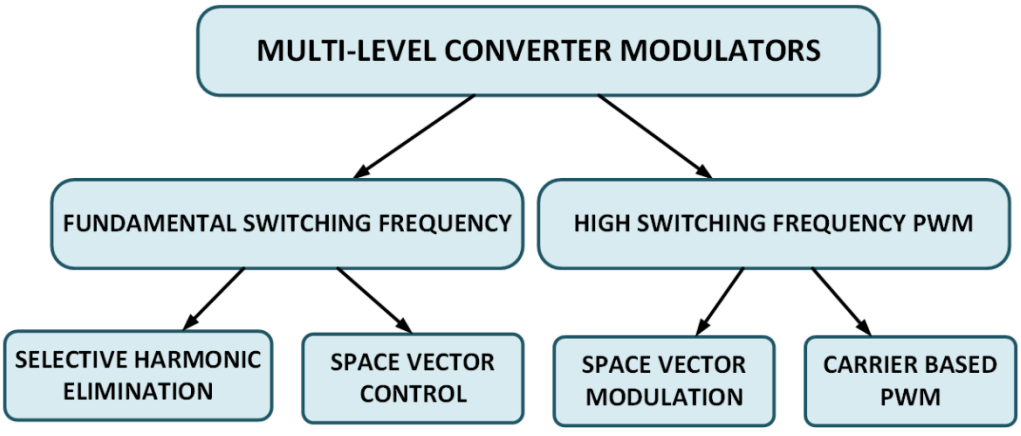


Figure 2.14 Multilevel converters modulators classification.

In particular high switching frequency techniques have several device commutations in each voltage waveform fundamental period and take advantage of Pulse Width Modulation (PWM)

applying the desired mean voltage in every switching interval. Modulation techniques operating at fundamental switching frequency perform very few device commutations in each fundamental voltage period [35]. The modulation techniques considered in this work are listed below:

- Carrier Based PWM uses several triangular carriers and one modulating signal to provide the desired voltage value. Carrier based PWM can be divided into Phase Shifted Carrier Modulation (PSCM) and Level Shifted Carrier Modulation (LSCM), depending on whether the carriers have different phase or different DC components [36], [117].
- Space Vector Modulation (SVM) considers the reference voltage as a voltage vector in the (α,β) space and uses a combination of the possible voltage vectors applicable by the converter to obtain the desired reference vector [34]. SVM provides a low THD and is easy to implement digitally [35]; however increasing the number of levels increases the modulator complexity drastically [35], [36]. Several algorithms have been proposed to reduce the modulator complexity and the computational effort of the controller [118]–[120] or to include additional targets for the SVM algorithm [121], [122].
- Selective Harmonic Elimination (SHE) uses pre-calculated switching angles to eliminate the desired harmonics reducing the converter voltage THD and the converter switching losses [34]. Even though SHE presents clear advantages in term of THD reduction at fundamental or low device switching frequency, this technique is limited to open loop or low-bandwidth applications and becomes very complex to implement for a multilevel converter with a high number of levels [34].
- Space Vector Control (SVC) considers the high number of voltage levels in a multi-level converter in order to apply the voltage vector closest to the reference vector [34], [35]. When compared to SHE, SVC provides an easy implementation for multilevel converters with an high number of voltage levels, with closed-loop control and high-bandwidth applications, reducing the converter losses [34]. However, SVC does not provide the desired mean voltage value over a sampling interval, resulting in errors, because of the absence of a PWM technique [35].

The carrier based and Space Vector modulation techniques are described in detail in Chapter 5.

2.3 Chapter summary

In this chapter the attention is focused on multilevel converter topologies that are applicable at the voltage levels considered for SSTs. Four multilevel converter topologies are analysed in detail:

- Diode Clamped converter.
- Flying Capacitor converter.
- Cascaded H-Bridge converter.
- Modular Multilevel Converter.

Between all these topologies, CHB based converters may present a viable solution for SST applications; they provide high modularity and require less components when compared to other multilevel converter topologies.

Converter control and modulation strategies are fundamental to achieve the desired power quality and converter stability. Several control techniques have been reviewed, focusing the attention on DBC and FCS-MPC, which can provide a fast transient response, high power quality and straightforward digital implementation. With the exception of FCS-MPC, a modulator is required to generate the actuating signals for the converter and several different solutions are possible. Carrier based PWM, SVM, SHE and SVC techniques have been considered and, in particular, SVM and PSCM will be described in detail in Chapter 5.

Chapter 3
The 2-Port Universal and Flexible Power Management demonstrator

The UNIFLEX-PM project [23], [44], [123]–[128] had the aim of investigating modular power conversion technologies for future electrical network applications and to experimentally verify some of these approaches via the construction and testing of a MV power converter.

The UNIFLEX-PM demonstrator has a three port structure, and presents numerous advantages over traditional electro-mechanical transformers in terms of power quality and voltage stability.

For this thesis work the UNIFLEX-PM demonstrator is configured in a two port structure, which accurately portrays the characteristics of a Solid State Substation, testing and validation of the novel control and modulation techniques, developed over the course of this work. The UNIFLEX-PM two port structure is introduced and modelled. Furthermore, its hardware realisation and the experimental setup are described in detail.

3.1 Universal and Flexible Power Management demonstrator structure

The Universal and Flexible Power Management (UNIFLEX-PM) demonstrator described in [124], [127], [128] has a three port structure based on a CHB back-to-back converter. However, in order to validate the control strategies proposed in this thesis and avoid complexities associated with multiport power flow, its two port structure is considered and described in this chapter. This structure closely resembles what is widely accepted as a likely Solid State Substation configuration.

3.1.1 Universal and Flexible Power Management demonstrator two port structure

In Figure 3.1 the overall converter structure, presented in [128], is shown. The converter presents a CHB structure, based on identical fundamental AC/AC cells, with each port comprising three AC/AC fundamental cells per phase.

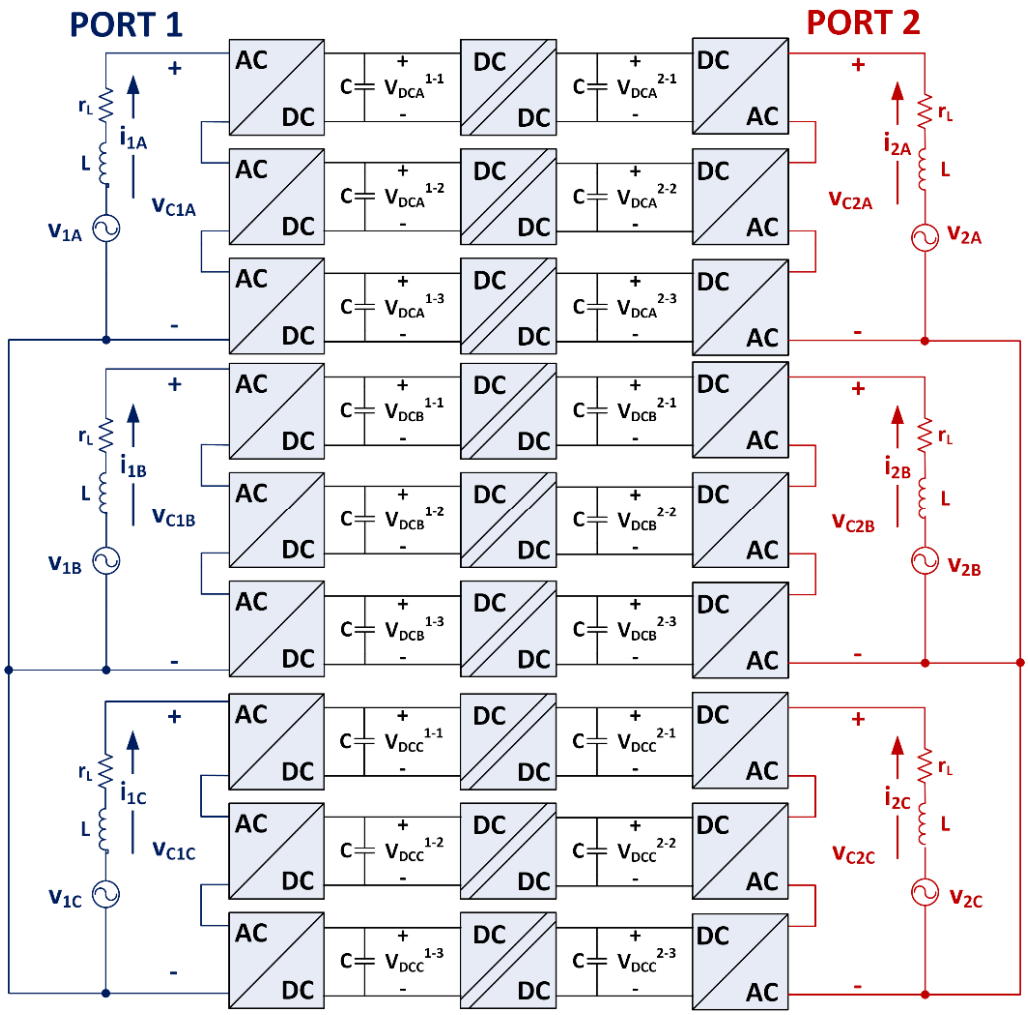


Figure 3.1 UNIFLEX-PM demonstrator two ports converter structure.

Each AC/AC cell consists of 4 H-Bridges configured in an AC/DC/DC/AC structure, with the DC/DC part of the structure providing medium frequency isolation. This isolation allows the cells to be series connected on the AC side to produce multi-level converter structures. Ports 1 and 2 can produce, respectively, 7 voltage levels (v_{C1A}, v_{C1B}, v_{C1C}, v_{C2A}, v_{C2B}, v_{C2C}) on each phase. An inductive filter L, including its winding resistance r_L, is present the phase of each port while a capacitive filter C is present on either side of each DC/DC converter. A three-phase, four-wire system is considered in order to treat the control of each phase independently. The proposed structure presents several advantages in comparison with other converter topologies:

- The CHB topology allows the use of active devices with lower voltage rating, reducing the converter losses and grid side filtering requirements, as discussed in Chapter 2.
- The use of identical AC/AC cells make the UNIFLEX-PM converter modular and, as consequence, easily expandable for higher powers and voltages.
- The structure of the AC/DC/DC/AC cell, if properly controlled, allows decoupled operation of the two ports of the converter with regards to power quality, operating frequency etc.

The nominal parameters of the UNIFLEX-PM demonstrator are shown in Table 3.1.

Table 3.1 UNIFLEX-PM converter parameters.

Name	**Description**	**Value**	**Unit**
C	DC-Link capacitor	3100	[μF]
r_L	Inductor resistance	0.5	[Ω]
L	AC filter inductance	11	[mH]
P^{nom}	Rated power	300	[kVA]
V_1^{nom}	Rated peak value of the AC supply on port 1 (line-to-line)	3300	[V]
V_2^{nom}	Rated peak value of the AC supply on port 2 (line-to-line)	3300	[V]
V_3^{nom}	Rated peak value of the AC supply on port 3 (line-to-line)	415	[V]
V_{DC}^{nom}	Rated capacitor voltage	1100	[V]
$f_{sw}^{DC/DC}$	Switching frequency of DC/DC converter	2500	[Hz]
$T_s^{DC/DC}$	Sample time of DC/DC converter	0.4	[ms]
f_{sw}	Switching frequency	5000	[Hz]
T_s	Sample time	0.2	[ms]

In Figure 3.2 the internal structure of a single AC/AC cell is shown. Each fundamental AC/AC cell comprises four HBs, two capacitors and a Medium Frequency (MF) transformer. The two outer HBs are used as part of the CHB structure on the two AC sides whilst the two inner HBs and the MF transformer form the DC/DC converter providing the necessary isolation between

the two AC connections. The DC/DC converter is a Dual Active Bridge (DAB) converter, designed to maintain the DC-Link 1 voltage equal to the DC-Link 2 voltage [129]. By controlling the converter DC link voltages (V_{DCA}^{1-1}, V_{DCA}^{1-2}, V_{DCA}^{1-3}, V_{DCB}^{1-1}, V_{DCB}^{1-2}, V_{DCB}^{1-3}, V_{DCC}^{1-1}, V_{DCC}^{1-2}, V_{DCC}^{1-3}, V_{DCA}^{2-1}, V_{DCA}^{2-2}, V_{DCA}^{2-3}, V_{DCB}^{2-1}, V_{DCB}^{2-2}, V_{DCB}^{2-3}, V_{DCC}^{2-1}, V_{DCC}^{2-2}, V_{DCC}^{2-3}) and the converter AC voltages (v_{C1A}, v_{C1B}, v_{C1C}, v_{C2A}, v_{C2B}, v_{C2C}) it is possible to control the converter AC currents (i_{1A}, i_{1B}, i_{1C}, i_{2A}, i_{2B}, i_{2C}) with an arbitrary phase shift respect to the supply voltages (v_{1A}, v_{1B}, v_{1C}, v_{2A}, v_{2B}, v_{2C}), thus achieving four quadrant power flow control.

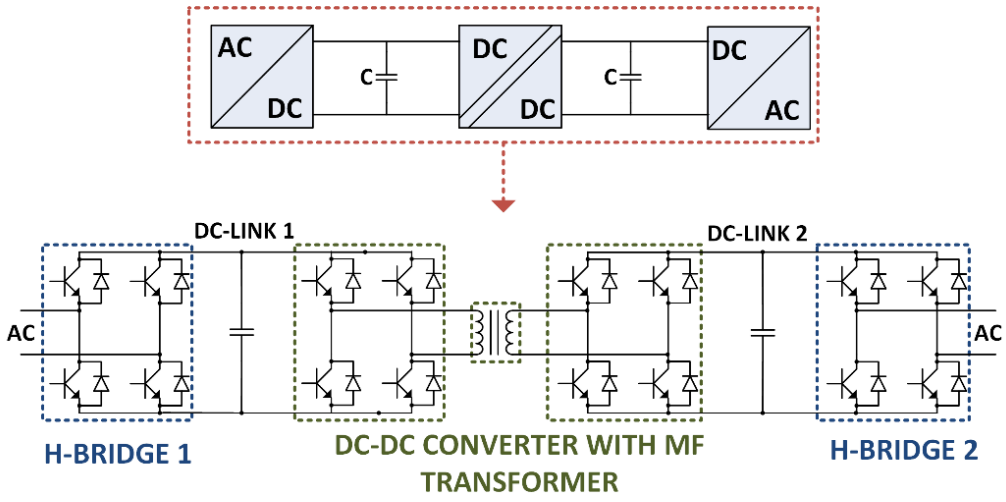


Figure 3.2 Fundamental AC/AC cell structure.

3.1.2 DC/DC converter description and control

In Figure 3.3 the DAB structure, comprising of two HBs linked on their AC side with a MF transformer, is shown. This structure can provide galvanic insulation at high frequencies, achieving a potential reduction in volume when compared to a 50Hz equipment at the same power level [129].

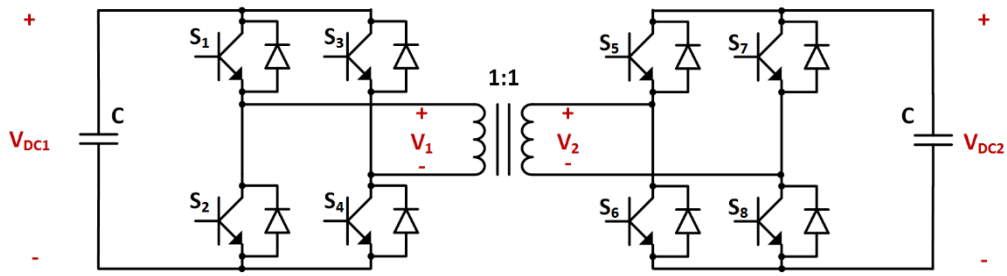


Figure 3.3 Dual Active Bridge converter schematic.

A soft switching approach is needed in order to not degrade efficiency significantly with switching losses [129], [130]. For this reason the DAB converter structure has been selected, since it is able to naturally soft switch when operated at rated power [131]. Power flow control can be achieved by regulating the voltage drop across the leakage inductance of the MF transformer, as shown in the simplified DAB equivalent circuit of Figure 3.4.

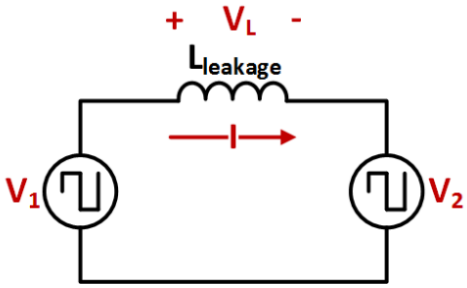


Figure 3.4 Dual Active Bridge converter equivalent circuit.

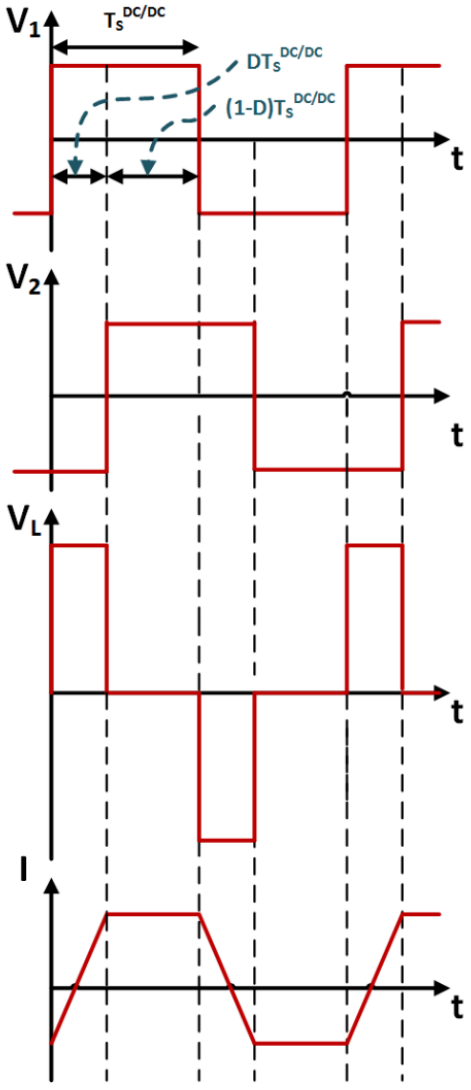


Figure 3.5 Dual Active Bridge converter produced waveforms.

The two HBs are switched in order to produce 50% duty cycle square waves; by phase shifting the square waves, V_1, V_2, with respect to each other a voltage drop on the transformer leakage inductance, $L_{leakage}$, is generated causing a current and power flow. In Figure 3.5 the two square waveforms produced by the HBs, as well as the produced voltage drop on the transformer leakage inductance and the resulting current are shown considering a MF transformer turns ratio equal to *1*.

By controlling the duty cycle *D* between the two square waveforms it is possible to control the current and power flow through the DAB converter [131], using the closed loop control scheme shown in Figure 3.6. A discretised PI controller model, a square wave generator and the DAB converter model, are necessary to design the control parameters, derived in [132] when small variations of *D* are considered. However, additional feed-forward compensation terms can be added to improve the control performances for wider variations of *D*.

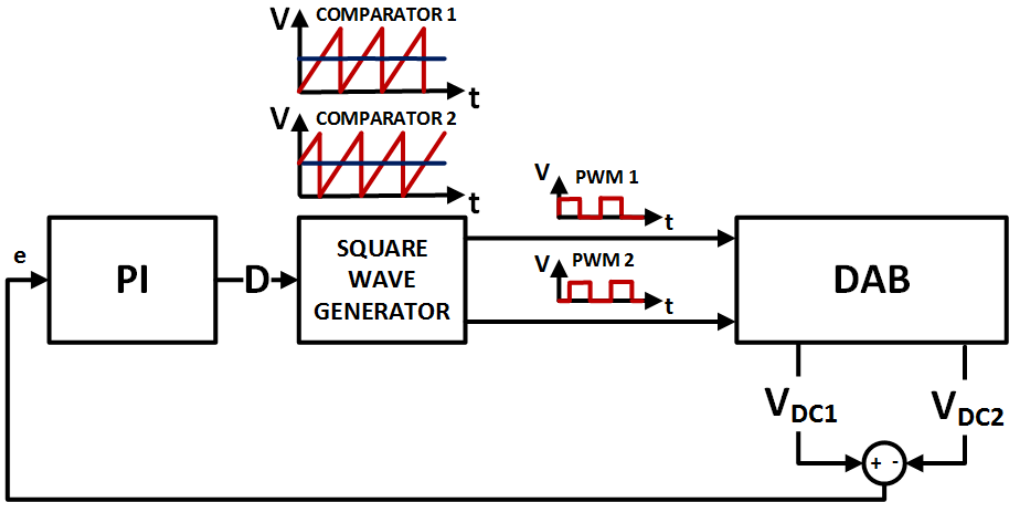


Figure 3.6 Dual Active Bridge converter control block scheme.

Using this simple control it is possible to operate each DAB converter in order to maintain equal DC-Link voltages on either side of the isolation barrier. In particular in [127], [132] it is shown that for simulation purposes it is possible to approximate the DAB converter dynamics with an equivalent capacitor *C*, equal to the capacitance on one side of the DAB converter. This is possible if the DAB control is designed to have a faster dynamic response when compared to the total DC-Link voltage control present on each CHB converter phase, making the delay introduced by the DAB negligible.

3.1.3 Universal and Flexible Power Management demonstrator two port model

The total switching model of the UNIFLEX-PM converter, shown in Figure 3.7, is obtained by approximating the DC/DC converter as a capacitor, *C*. This approximation is valid under the assumption that the DAB converter is controlled in such a way that its effect on the other control loops in the converter is negligible [123]. The model is intrinsically nonlinear since the switching state of each HB defines the produced AC voltage and DC current simultaneously.

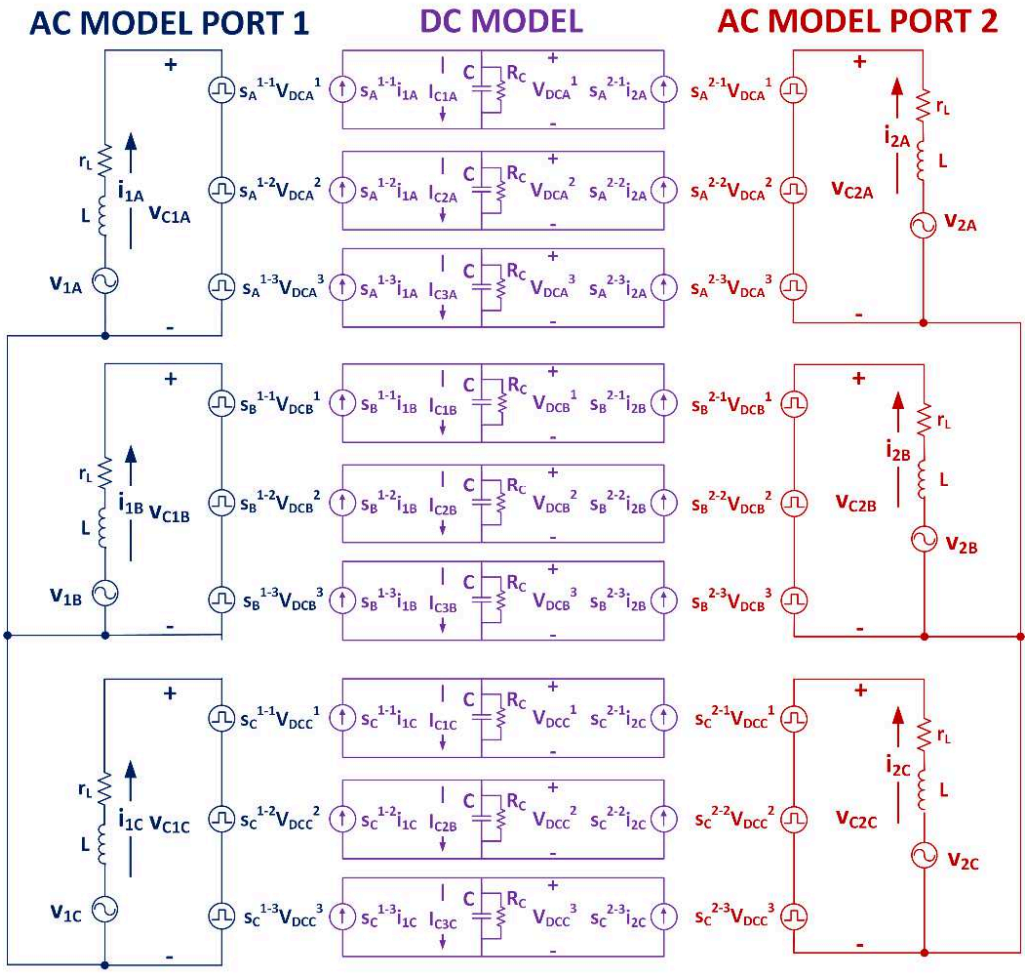


Figure 3.7 UNIFLEX-PM converter equivalent two port model.

The HBs states are defined in (3.1) according to the notation defined in section 2.1.3.

$$s_p{}^{i-j} = -1,0,1 \tag{3.1}$$

To identify each HB three indexes are used, where *p* is the phase, *i* is the port connected to the selected HB, and *j* defines which HB of the CHB is considered. As an example, the third HB of UNIFLEX-PM demonstrator port 1, phase A is defined as $s_A{}^{1\text{-}3}$.

It is important to highlight that R_C represents the losses in the DC/DC converter and DC-Link capacitors and it is variable, depending on the converter operating point. For simulation purpose a value of R_C equal to 1kΩ has been chosen. Considering the parameters of Table 3.1, when the power is equally shared between the three fundamental cells on each phase, this value results in a DC/DC converter efficiency of around 96%, which is in line with the expected efficiency of the converter.

The model is described by the following system of equations, where the state of the system is defined by the DC-Link voltage and AC currents and the HB states are defined according to the notation in (3.1).

$$\begin{cases} \dot{\imath_{1A}}(t) = \frac{1}{L}[v_{1A}(t) - v_{C1A}(t)] - \frac{r_L}{L} i_{1A}(t) \\ \dot{\imath_{1B}}(t) = \frac{1}{L}[v_{1B}(t) - v_{C1B}(t)] - \frac{r_L}{L} i_{1B}(t) \\ \dot{\imath_{1C}}(t) = \frac{1}{L}[v_{1C}(t) - v_{C1C}(t)] - \frac{r_L}{L} i_{1C}(t) \\ \dot{\imath_{2A}}(t) = \frac{1}{L}[v_{2A}(t) - v_{C2A}(t)] - \frac{r_L}{L} i_{2A}(t) \\ \dot{\imath_{2B}}(t) = \frac{1}{L}[v_{2B}(t) - v_{C2B}(t)] - \frac{r_L}{L} i_{2B}(t) \\ \dot{\imath_{2C}}(t) = \frac{1}{L}[v_{2C}(t) - v_{C2C}(t)] - \frac{r_L}{L} i_{2C}(t) \\ \dot{V_{DCA}}^1(t) = \frac{1}{C} I_{C1A}(t) - \frac{1}{R_c C} V_{DCA}{}^1(t) \\ \dot{V_{DCA}}^2(t) = \frac{1}{C} I_{C2A}(t) - \frac{1}{R_c C} V_{DCA}{}^2(t) \\ \dot{V_{DCA}}^3(t) = \frac{1}{C} I_{C3A}(t) - \frac{1}{R_c C} V_{DCA}{}^3(t) \\ \dot{V_{DCB}}^1(t) = \frac{1}{C} I_{C1B}(t) - \frac{1}{R_c C} V_{DCB}{}^1(t) \\ \dot{V_{DCB}}^2(t) = \frac{1}{C} I_{C2B}(t) - \frac{1}{R_c C} V_{DCB}{}^2(t) \\ \dot{V_{DCB}}^3(t) = \frac{1}{C} I_{C3B}(t) - \frac{1}{R_c C} V_{DCB}{}^3(t) \\ \dot{V_{DCC}}^1(t) = \frac{1}{C} I_{C1C}(t) - \frac{1}{R_c C} V_{DCC}{}^1(t) \\ \dot{V_{DCC}}^2(t) = \frac{1}{C} I_{C2C}(t) - \frac{1}{R_c C} V_{DCC}{}^2(t) \\ \dot{V_{DCC}}^3(t) = \frac{1}{C} I_{C3C}(t) - \frac{1}{R_c C} V_{DCC}{}^3(t) \end{cases} \quad (3.2)$$

In (3.2) the converter AC voltages (V_{C1A}, V_{C1B}, V_{C1C}, V_{C2A}, V_{C2B}, V_{C2C},) are defined by (3.3) while the DC-Link capacitor currents, (I_{C1A}, I_{C2A}, I_{C3A}, I_{C1B}, I_{C2B}, I_{C3B}, I_{C1C}, I_{C2C}, I_{C3C}), are defined by (3.4).

$$\begin{cases} V_{C1A}(t) = s_A{}^{1-1}(t) V_{DCA}{}^1(t) + s_A{}^{1-2}(t) V_{DCA}{}^2(t) + s_A{}^{1-3}(t)\, V_{DCA}{}^3(t) \\ V_{C1B}(t) = s_B{}^{1-1}(t) V_{DCB}{}^1(t) + s_B{}^{1-2}(t) V_{DCB}{}^2(t) + s_B{}^{1-3}(t) V_{DCB}{}^3(t) \\ V_{C1C}(t) = s_C{}^{1-1}(t)\, V_{DCC}{}^1(t) + s_C{}^{1-2}(t) V_{DCC}{}^2(t) + s_C{}^{1-3}(t)\, V_{DCC}{}^3(t) \\ V_{C2A}(t) = s_A{}^{2-1}(t) V_{DCA}{}^1(t) + s_A{}^{2-2}(t) V_{DCA}{}^2(t) + s_A{}^{2-3}(t)\, V_{DCA}{}^3(t) \\ V_{C2B}(t) = s_B{}^{2-1}(t) V_{DCB}{}^1(t) + s_B{}^{2-2}(t) V_{DCB}{}^2(t) + s_B{}^{2-3}(t) V_{DCB}{}^3(t) \\ V_{C2C}(t) = s_C{}^{2-1}(t)\, V_{DCC}{}^1(t) + s_C{}^{2-2}(t) V_{DCC}{}^2(t) + s_C{}^{2-3}(t)\, V_{DCC}{}^3(t) \end{cases} \quad (2.3)$$

$$\begin{cases} I_{C1A}(t) = {s_A}^{1-1}(t) i_{1A}(t) + {s_A}^{2-1}(t) i_{2A}(t) \\ I_{C2A}(t) = {s_A}^{1-2}(t) i_{1A}(t) + {s_A}^{2-2}(t) i_{2A}(t) \\ I_{C3A}(t) = {s_A}^{1-3}(t) i_{1A}(t) + {s_A}^{2-3}(t) i_{2A}(t) \\ I_{C1B}(t) = {s_B}^{1-1}(t) i_{1B}(t) + {s_B}^{2-1}(t) i_{2B}(t) \\ I_{C2B}(t) = {s_B}^{1-2}(t) i_{1B}(t) + {s_B}^{2-2}(t) i_{2B}(t) \\ I_{C3B}(t) = {s_B}^{1-3}(t) i_{1B}(t) + {s_B}^{2-3}(t) i_{2B}(t) \\ I_{C1C}(t) = {s_C}^{1-1}(t) i_{1C}(t) + {s_C}^{2-1}(t) i_{2C}(t) \\ I_{C2C}(t) = {s_C}^{1-2}(t) i_{1C}(t) + {s_C}^{2-2}(t) i_{2C}(t) \\ I_{C3C}(t) = {s_C}^{1-3}(t) i_{1C}(t) + {s_C}^{2-3}(t) i_{2C}(t) \end{cases} \quad (2.4)$$

The two port UNIFLEX-PM demonstrator as described from the model of Figure 3.7 does not present any particular power flow control limitations, in contrast with the three port structure. In fact in the latter case a power flow control limitation is present and related with current circulation between ports, as reported in [128], [133]. Considering the UNIFLEX-PM demonstrator two port structure, all the cells are connected between port 1 and port 2, and the active power balance of equation (3.5) is always satisfied, where P_1 and P_2 are respectively the active power flowing through Port 1 and Port 2 of the UNIFLEX-PM demonstrator.

$$P_1 + P_2 = 0 \quad (3.5)$$

However a limitation appears under real operating conditions because even a small delay introduced by the DC/DC converter affects the constraints imposed by equation (3.5) during fast dynamic active power transients (for example, a step change in the active power reference). In order to minimise this effect, the rate of change of the active power reference is limited to avoid excessive DC-Link voltage overshoot during transients.

3.2 Hardware realisation

A 300kVA hardware prototype, designed for the UNIFLEX-PM project demonstration and shown in Figure 3.8, has been constructed at the University of Nottingham. The prototype is based on the parameters shown in Table 3.1, and has been realised in order to evaluate the performance of the proposed converter topology [124]. This hardware has been used to validate the control techniques proposed in the next chapters.

Figure 3.8 UNIFLEX-PM converter experimental prototype [124].

The converter comprises of the power circuits, transducers, control circuits and low voltage auxiliary power supplies. A single UNIFLEX-PM converter cell is shown in Figure 3.9, highlighting the location of various components and the dimensions of the converter [124], [134].

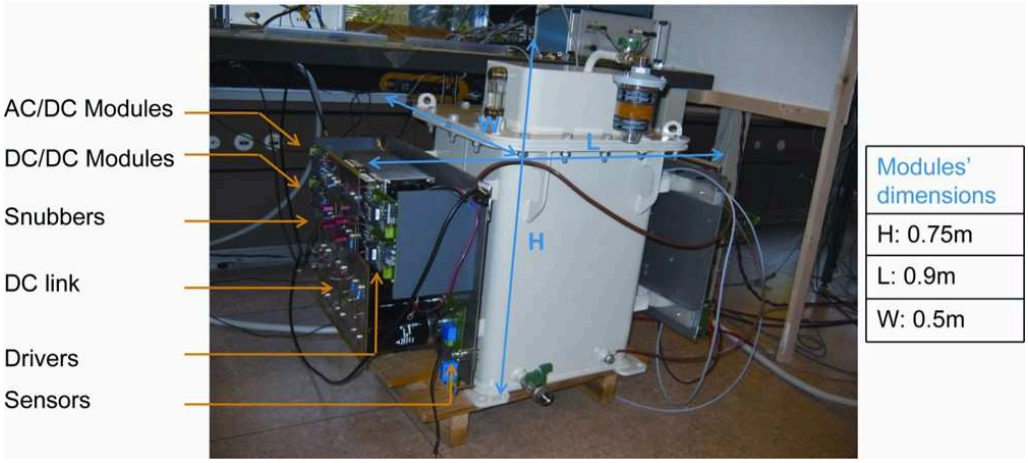


Figure 3.9 UNIFLEX-PM converter fundamental cell realization [132], [134].

The structure of the UNIFLEX-PM cell was designed by researchers at Ecole Polytechnique Federal de Lausanne (EPFL), Switzerland, aided by ABB, Secheron, Switzerland, who designed the MF transformers [132], [134].

The overall converter is described in the block diagram of Figure 3.10 where both power and signal connections are highlighted. Three main circuits are defined:

- The control circuit which implements closed-loop control and modulation.
- The power circuit which represents the high-power converter circuitry.
- The sensing and drives circuit which represents the insulated interface between power and control circuit.

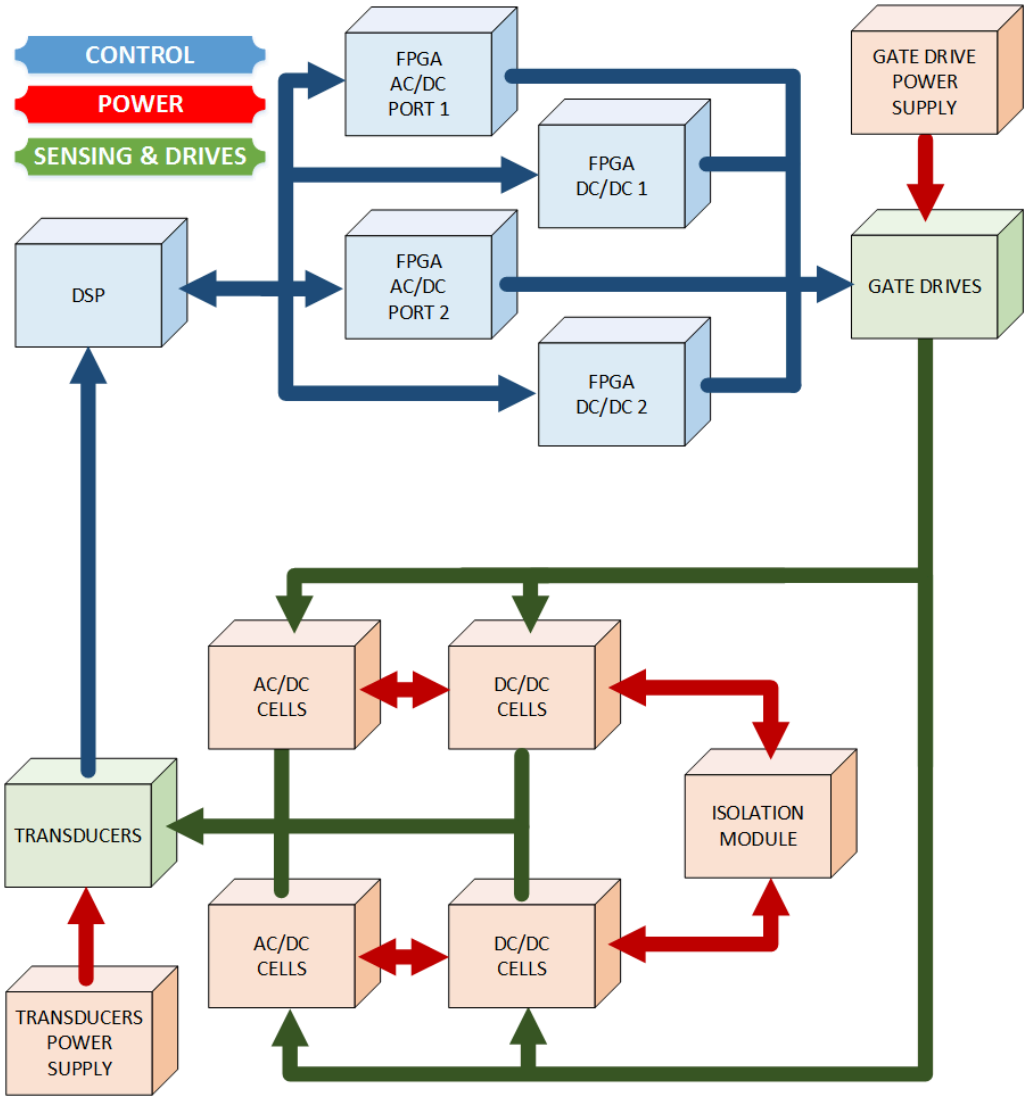


Figure 3.10 UNIFLEX-PM converter realization block diagram.

3.2.1 Control hardware

The control hardware is composed of 4 ACTEL ProASIC 3 FPGA boards, designed at the University of Nottingham, and a commercial TI6713DSK 32 bit floating point DSP board, designed by Spectrum Digital. The FPGA boards, clocked at 50MHz, also include ten Analogue to Digital conversion channels for data acquisition and protection systems. The FPGA boards registers are mapped into the DSP board memory, allowing the DSP to communicate with the FPGA boards in real time [124].

The complete control circuit realisation, implemented during the UNIFLEX-PM project, is shown in Figure 3.11 [44], [124]. Two FPGA boards (one for each converter port) are used to implement the gate drives signal generation for the AC connection while the DSP board is used to implement the closed loop control of the AC side power converter. The DSP board sends the desired demands to the appropriate FPGA card, which transform it into gating pulses which are transmitted to the gate drives via optical fibres.

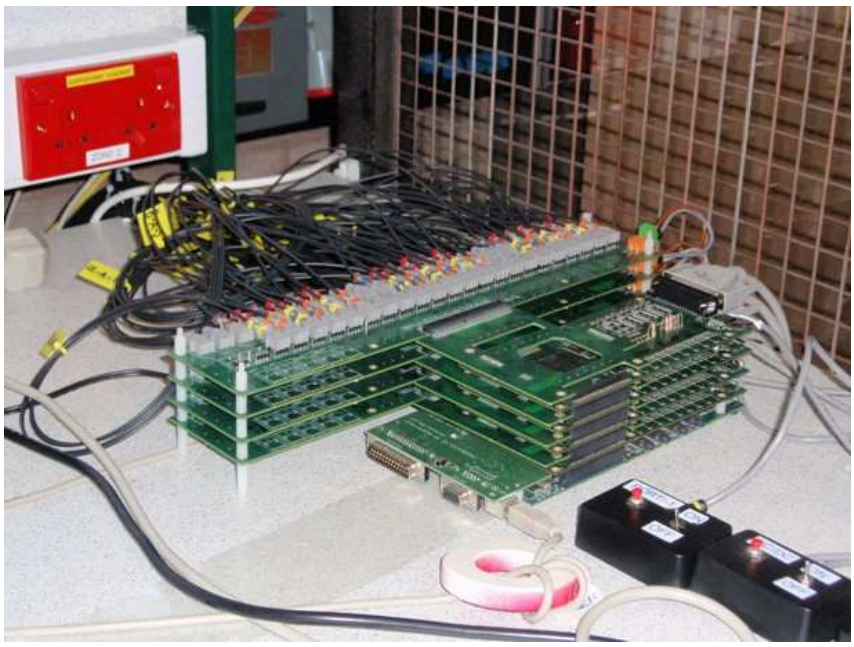


Figure 3.11 DSP/FPGA boards and fibre optic connections [124].

A further two FPGA boards implement the analogue to digital conversion of the eighteen DC-Link voltage measurements as well as the complete DAB control implementation, relieving the DSP board from the high computational effort required to implement nine further PI controllers [129]. The control and modulation of five complete DC/DC converters can be

implemented in a single FPGA [129]. The DSP board just accesses the control registers for the DC/DC converters once during boot operations, after which the DC/DC converters run independently of the DSP. The DSP, however, can still access the DC link voltage measurements which are required for modulation and the operation of safety systems.

Thirty measurements are required to operate the two port UNIFLEX-PM demonstrator: six AC voltages, six AC currents and eighteen DC-Link voltages. For the AC voltages measurements LEM LV-100-SP16E transducers are used while the DC-Link voltages measurements use LEM LV-25P transducers. The AC current measurement are achieved using Honeywell CSNS300M transducers.

2.2.2 Converter hardware

Each converter cell is realised using Dynex 1700V, 200A, IGBT modules, shown in Figure 3.12. The local capacitance of 3.1mF, on each side of the DAB converters, is realised using a combination of series and parallel electrolytic capacitors to achieve the desired current and voltage rating. Six 11mH inductors are used to provide the desired filter inductance on each converter phase. The inductance value is clearly high but is used to achieve reasonable filtering at switching frequencies suitable for the application. In a more realistic application, an increased number of cells would significantly reduce the filtering requirements.

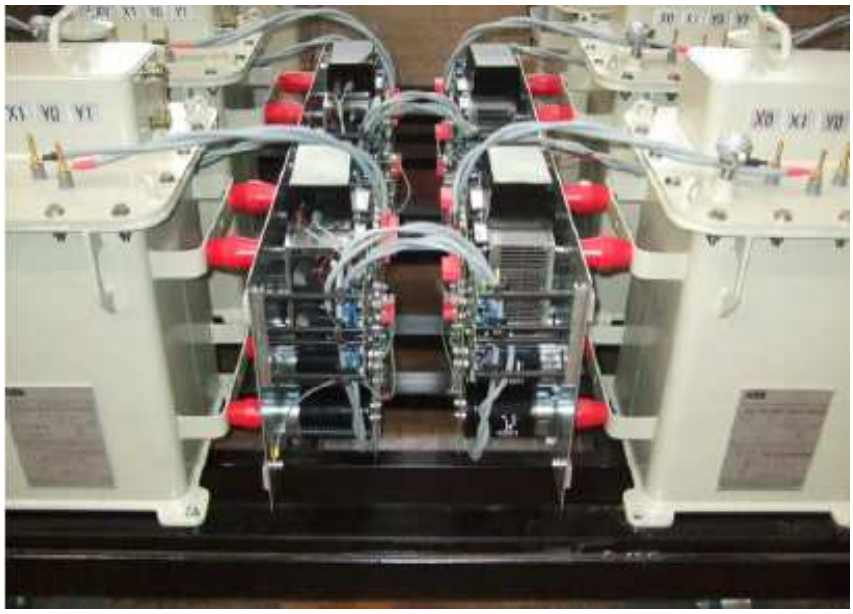


Figure 3.12 UNIFLEX-PM converter MF transformer with power electronic in place [124].

3.2.3 Experimental setup for two port low voltage testing

In Figure 3.13 the actual UNIFLEX-PM converter configuration is shown. For the SST testing only the three left hand side columns are used (bottom right cell is inactive).

Figure 3.13 Actual UNIFLEX-PM converter configuration.

Since only 415 V is grid currently available for experimental testing, during the thesis work experimental two port low voltage testing is considered while simulation results are shown considering the rated parameters of Table 3.1.

For experimental testing the simplified scheme of Figure 3.14 (unidirectional configuration) is considered to test the capability of the proposed control methodologies under different non-ideal grid conditions. This is because the programmable power supply used in the test is only able to generate (and not absorb) power.

However it is possible to achieve bidirectional power flow operation by connecting the two converter ports in parallel as shown in Figure 3.15. In this case the grid provides only the power necessary to compensate the converter losses.

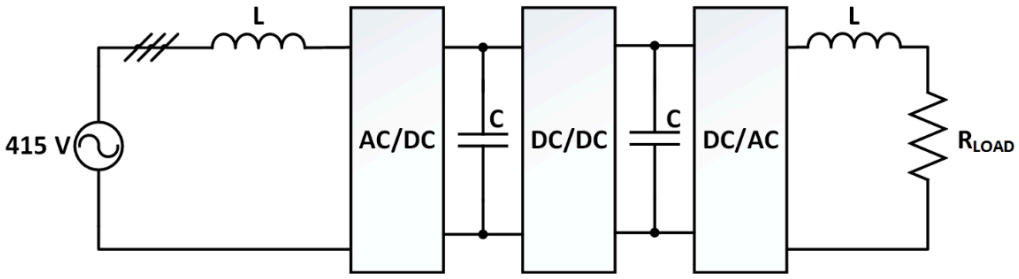


Figure 3.14 Simplified block scheme for UNIFLEX-PM converter, 2 port low voltage testing unidirectional configuration.

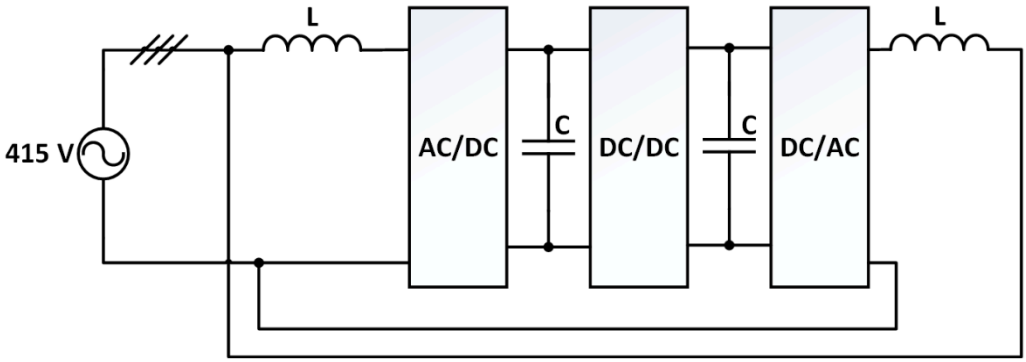


Figure 3.15 Simplified block scheme for UNIFLEX-PM converter, 2 port low voltage testing bidirectional configuration.

3.3 Chapter summary

In this chapter the converter topology used to validate the control techniques described in the following chapters has been described. In particular a 7-Level CHB converter for SST applications, proposed during the UNIFLEX-PM project is described in detail, highlighting its multi-stage structure.

A comprehensive description of the AC/DC, DC/DC and DC/AC power conversion stage is provided.

In order to provide the necessary information for the control design and validation, the equivalent switching model of the proposed converter is derived and the UNIFLEX-PM demonstrator hardware, used to experimentally validate the proposed control techniques, is analysed.

Chapter 4
Grid monitoring systems

A monitoring system is required in grid connected applications in order to derive certain characteristic about the electrical network under both normal and abnormal conditions [123]. It provides information on the phase, frequency and Root Mean Square (RMS) value of the supply voltage to the main control loops. Several methods to derive this information exist depending on the technique used to detect the supply phase. Many of these are based on supply voltage zero crossing detection, arctangent calculation or PLL algorithms [123]. The latter case presents a robust method to dynamically detect the grid voltage phase angle. When compared to the other phase detection techniques the PLL provides better disturbance and noise rejection [123] and several PLL structures have been presented in literature for grid connected applications [135]–[142].

During this work the attention is focused on the classic PLL design, using a rotating reference frame, distinguishing between three-phase and single phase structures. Moreover an improved grid monitoring system particularly suitable for digital implementation is described.

4.1 Grid monitoring system based on a three-phase Phase-Locked-Loop

In Figure 4.1 a block diagram of a three-phase PLL based grid monitoring system is shown. It includes a coordinate transformation from a natural to a rotating reference frame [57], [58], PLL algorithm, and the RMS and frequency detection systems.

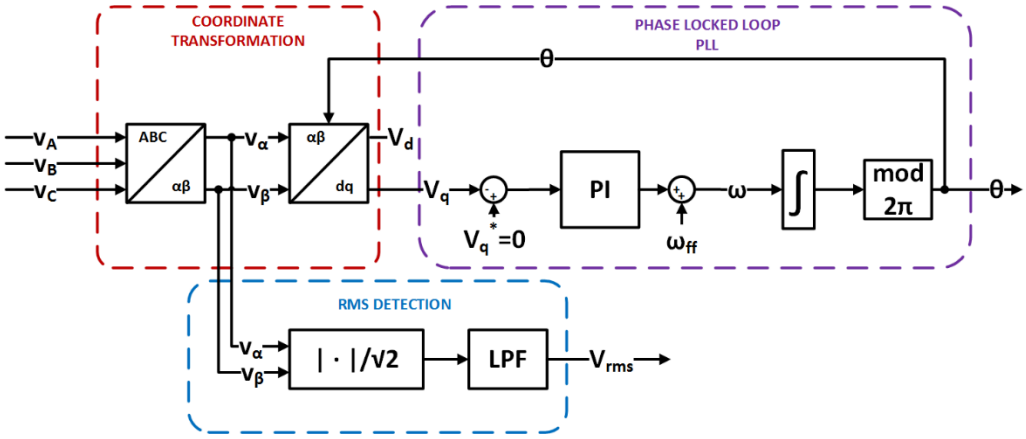


Figure 4.1 General structure of a three-phase PLL based grid monitoring system.

The PLL is based on a PI controller designed to regulate the quadrature supply voltage component, v_q, to zero in order to synchronise the *d*-axis of the synchronous reference frame to the supply voltage vector. Under these conditions the supply frequency ω is obtained which can be integrated to derive the supply voltage phase angle θ.

By using this PLL scheme it is also possible to extract the supply frequency, *f*, from ω, when appropriately scaled and filtered using a Low-Pass Filter (LPF) to eliminate high order harmonics.

The RMS voltage detection is based on the calculation of the absolute value of the voltage vector in a stationary reference frame which, when divided by $\sqrt{2}$, gives the RMS value of the supply voltage under non-distorted grid conditions. A LPF is needed to filter high order harmonics that might be present on the supply voltage measurement.

This structure provides good grid harmonics rejection. However in the case of an unbalanced grid voltage the structure of Figure 4.1 is not able to filter the negative sequence generated on the three-phase voltage system and improvements to the PLL algorithm are needed to extract the positive sequence angle [136].

Simulation results for the three phase PLL under several operating conditions are presented in Figure 4.2. The three phase PLL has been designed in order to get a fast dynamic response and to filter high order harmonics that may be present on the grid voltage. In order to satisfy this specification a phase margin of 45° and a crossover frequency of 100Hz has been chosen.

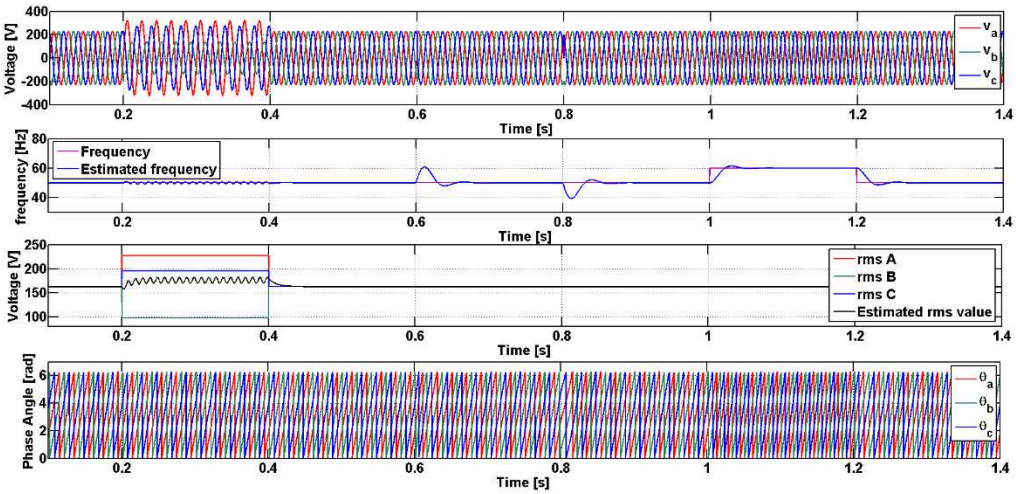


Figure 4.2 Three Phase PLL: overall response.

The three phase PLL does not respond well to voltage unbalances, as shown in Figure 4.3; the RMS value on each phase is not well estimated and distortion appears on the produced grid voltage phase angle.

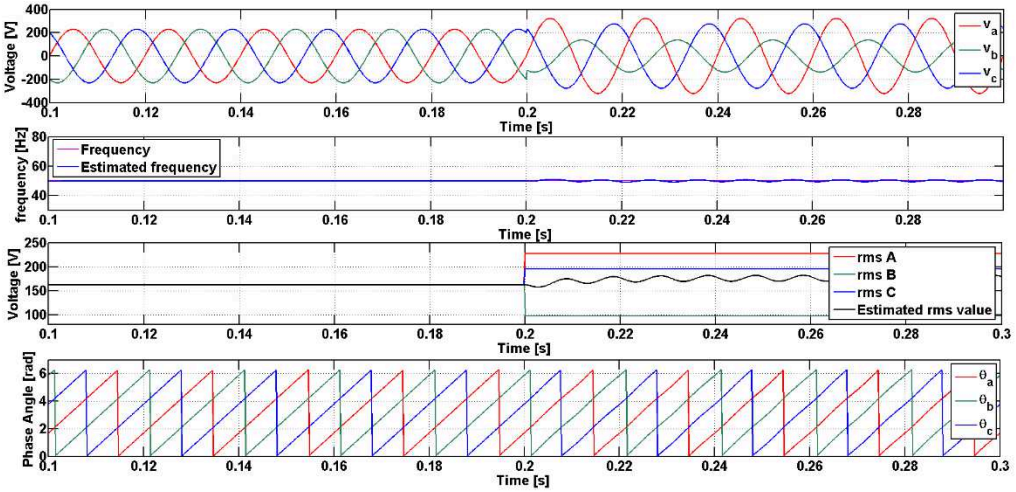


Figure 4.3 Three Phase PLL: response to voltage unbalances.

In Figure 4.4 a phase jump of 60° is considered. In this case the PLL presents a fast response and recovers in one supply cycle.

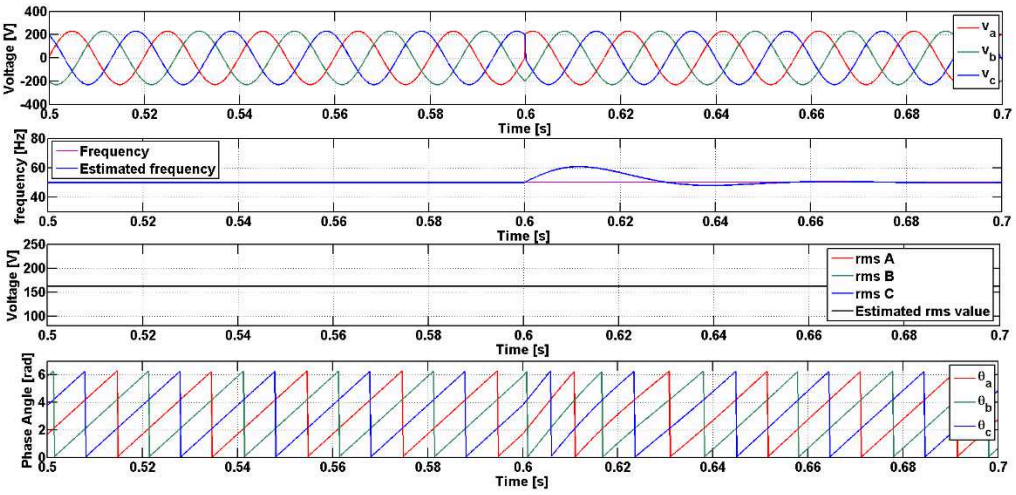


Figure 4.4 Three Phase PLL: response to phase jumps.

In Figure 4.5 a frequency variation from 50Hz to 60Hz is considered. It is clear that the three phase PLL quickly recovers with negligible frequency overshoot.

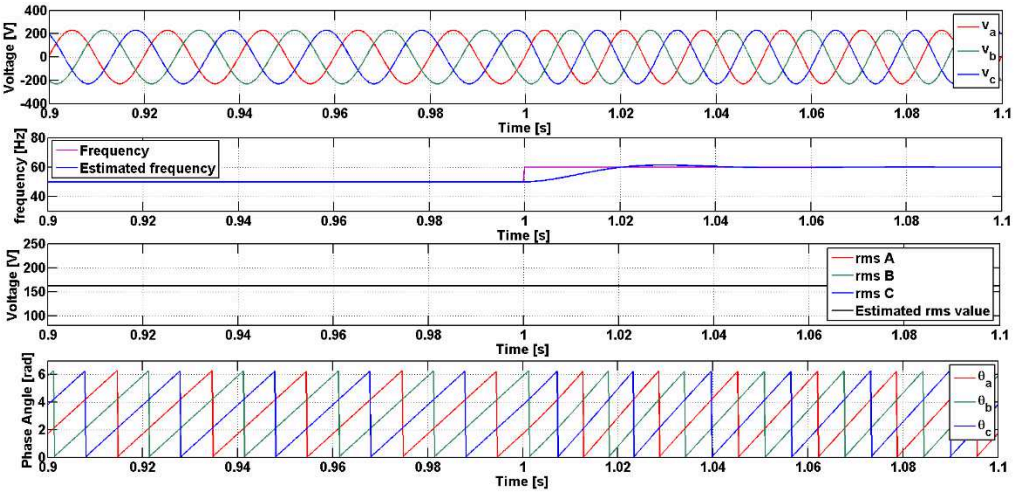


Figure 4.5 Three Phase PLL: response to frequency variations.

4.2 Grid monitoring system based on single-phase Phase-Locked-Loop

The same structure of Figure 4.1 can be used to implement a grid monitoring system based on a single-phase PLL, using an appropriate orthogonal system generator, as shown in Figure 4.6.

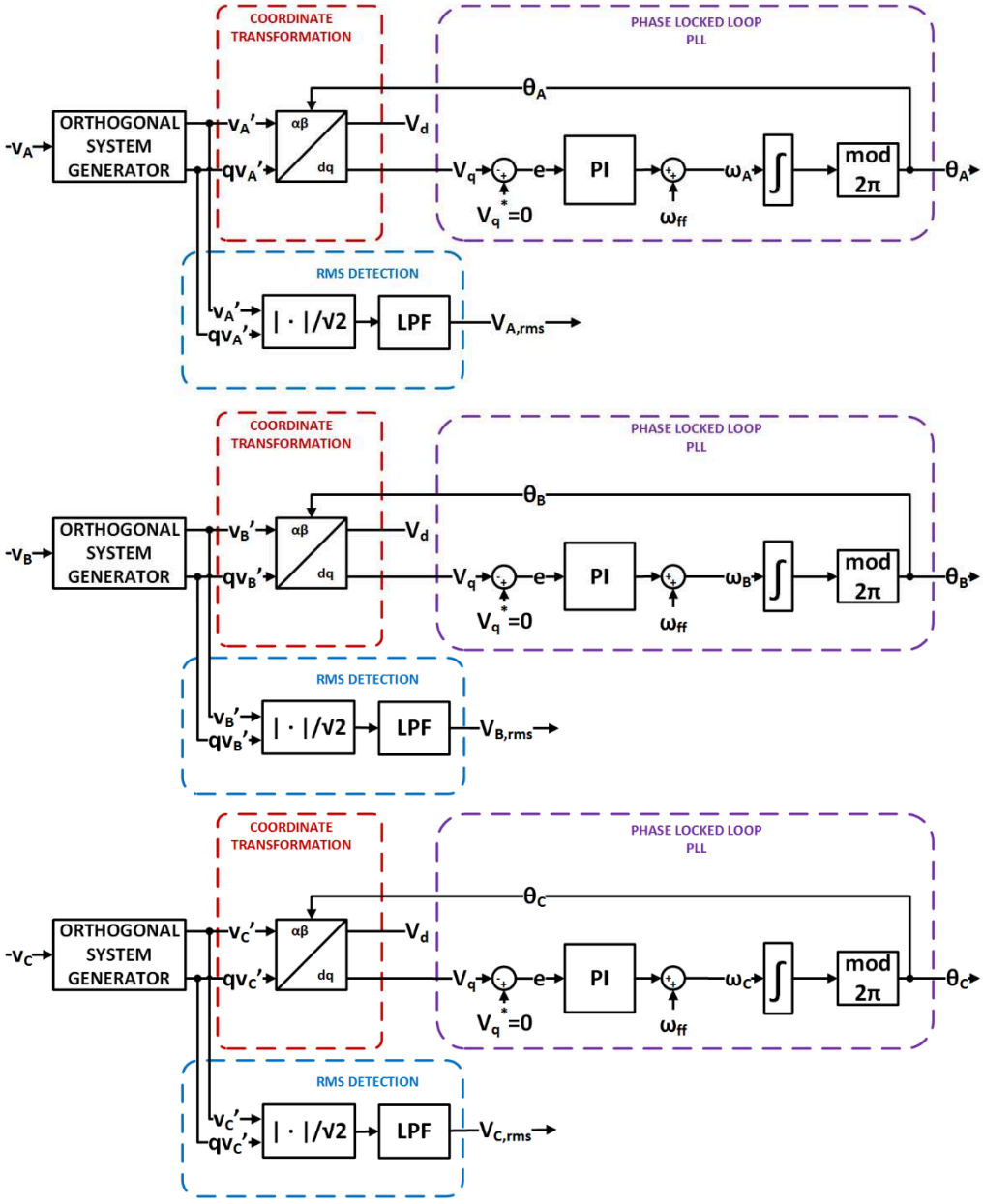


Figure 4.6 General structure of a single-phase PLL based grid monitoring system.

In this case, particular attention to the choice of the orthogonal system generator has to be made in order to reduce delay effects on the operation of the PLL. Several methods can be considered including the use of a transport delay, inverse park transform, Hilbert filter [137] etc. These options provide several disadvantages in terms of frequency dependency, nonlinearity, high complexity and poor signal filtering [139].

Another option is a Second Order Generalized Integrator (SOGI) [135], [139]. This method provides several advantages, such as high dynamic response, easy digital implementation and natural filtering of orthogonal voltages with zero delay. Moreover, it can be tuned for various characteristics, such as frequency independency or fast response to transients [123], [139]. On the other hand, the SOGI is affected by the discretisation method applied to implement it digitally and its tuning is dependent on the amplitude of the supply voltage [123], [139]. The overall PLL structure, shown in Figure 4.6, provides the same advantages as the three-phase PLL based grid monitoring system in terms of grid harmonics rejection and is able to work effectively under asymmetrical grid conditions such as voltage unbalances and short-circuits. The obvious disadvantage is the requirement of higher system complexity and computational effort [123].

In Figure 4.7 simulation results for the single phase PLL under several operating conditions are shown. The single phase PLL has been designed with the same criteria as the three phase PLL, i.e. achieve a fast dynamic response and filter high order harmonics that may be present on the grid voltage. As for the three phase PLL, the PI control parameters have been chosen in order to satisfy the specifications a phase margin of 45° and a crossover frequency of 100Hz.

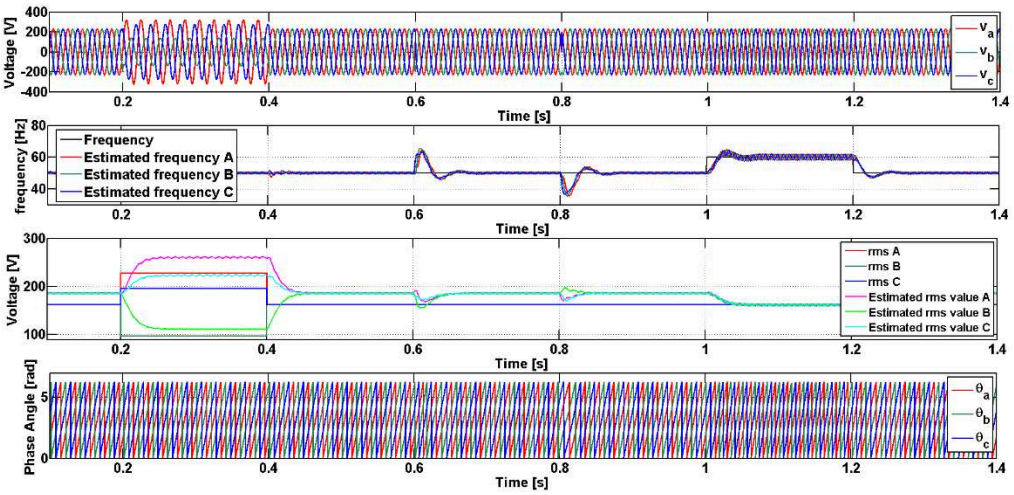


Figure 4.7 Single Phase PLL: overall response.

The single phase PLL is not affected by voltage unbalances, as shown in Figure 4.8; however, since the SOGI amplitude gain between input voltage and orthogonal components is not unity, the RMS value on each phase has a steady state error. In Figure 4.9 a phase jump of 60° is considered; in this case the PLL presents a fast response and recovers in less than half supply cycle. In Figure 4.10 a frequency variation from 50Hz to 60Hz is considered; compared with

Figure 4.5, the three single phase PLLs quickly recovers with negligible frequency overshoot but a higher frequency ripple is present, mainly related with the tuning and discretisation of the SOGIs.

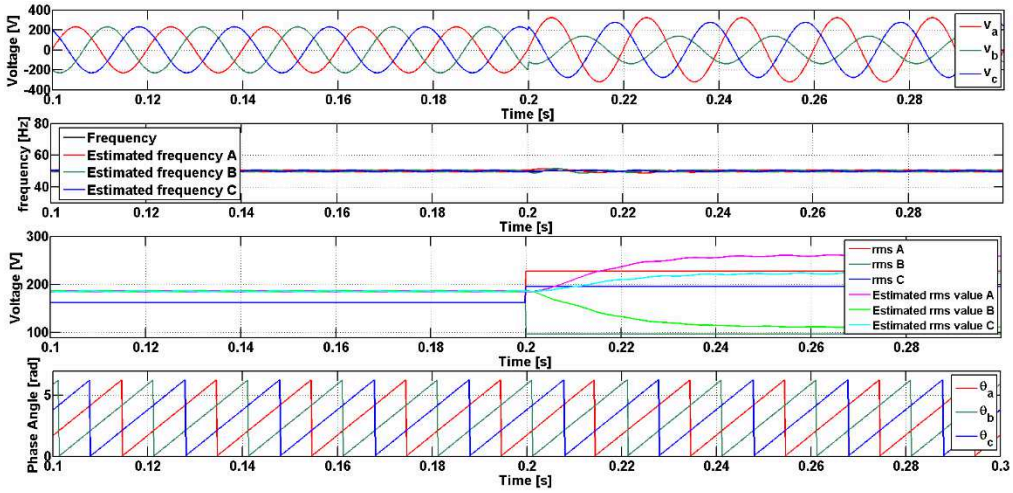


Figure 4.8 Single Phase PLL: response to voltage unbalances.

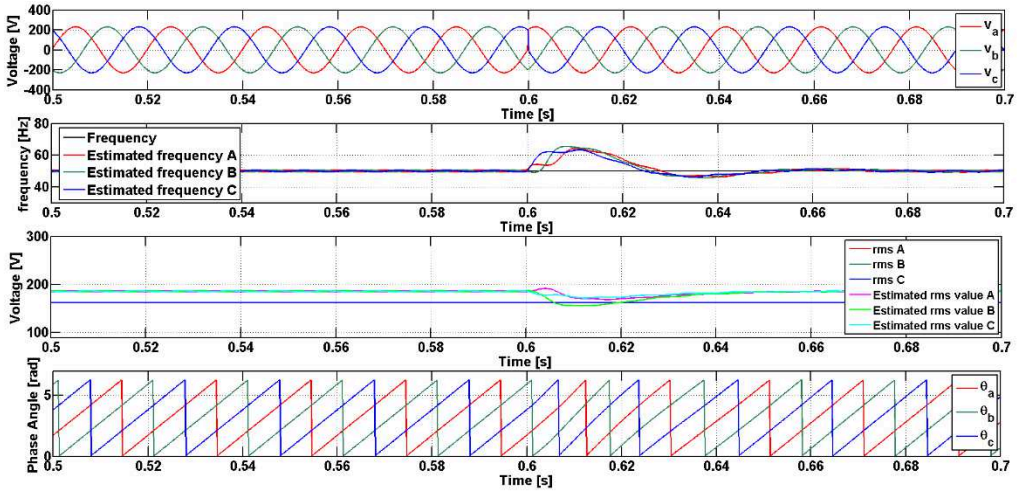


Figure 4.9 Single Phase PLL: response to phase jumps.

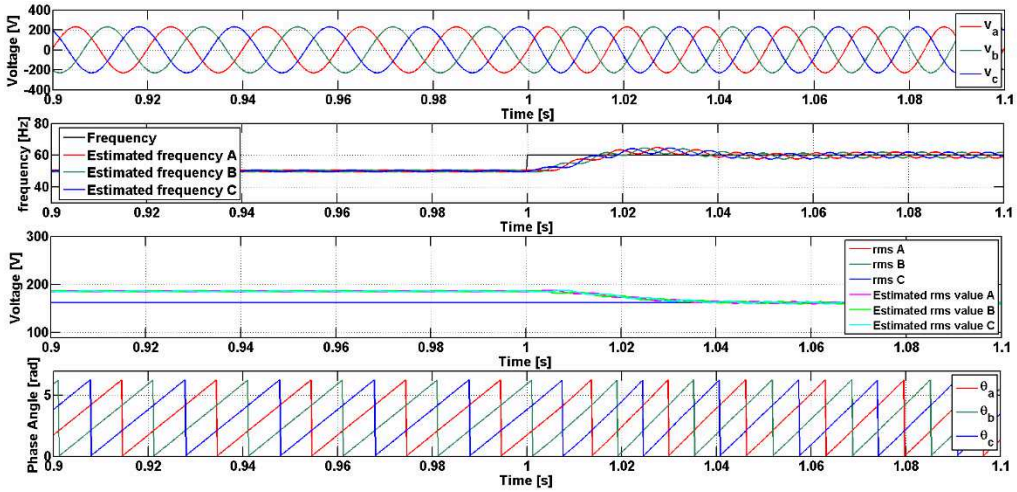


Figure 4.10 Single Phase PLL: response to frequency variations.

4.3 Advanced grid monitoring system based on single-phase Phase-Locked-Loop

Based on the issues considered in paragraphs 4.1 and 4.2, it has been decided that a grid monitoring system based on single-phase PLL would be prudent. In order to overcome the issues associated with the synchronous reference frame PLL, a new approach has been devised as shown in Figure 4.11 for phase A.

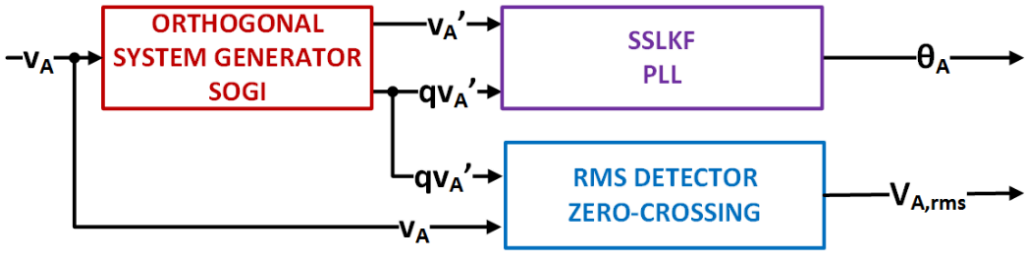


Figure 4.11 Overall proposed grid monitoring scheme on phase A.

A SOGI is implemented to realise the orthogonal system generation and a PLL based on a Steady State Linear Kalman Filter (SSLKF) is used instead of the classic dq PLL. The RMS voltage calculation is based on a zero-crossing technique in order to decouple it from the SOGI parameter tuning.

4.3.1 Orthogonal system generator based on a Second Order Generalized Integrator

The Second Order Generalized Integrator (SOGI) is based on the resonant structure shown in Figure 4.12 [139]. The obtained closed loop transfer functions between the input signal *v* and the output signal in phase, *v'*, and in quadrature, *qv'*, are shown below [139].

$$H_d(s) = \frac{v'(s)}{v(s)} = \frac{k_{SOGI}\omega_r s}{s^2 + k\omega_r s + {\omega_r}^2} \tag{4.1}$$

$$H_q(s) = \frac{qv'(s)}{v(s)} = \frac{k_{SOGI}{\omega_r}^2}{s^2 + k_{SOGI}\omega_r s + {\omega_r}^2} \tag{4.2}$$

Where ω_r is the SOGI resonant frequency, set to be equal to the grid frequency, and k_{SOGI} is the gain of the proportional controller which determines the orthogonal system generation bandwidth and, thus, its time response to variation on the input.

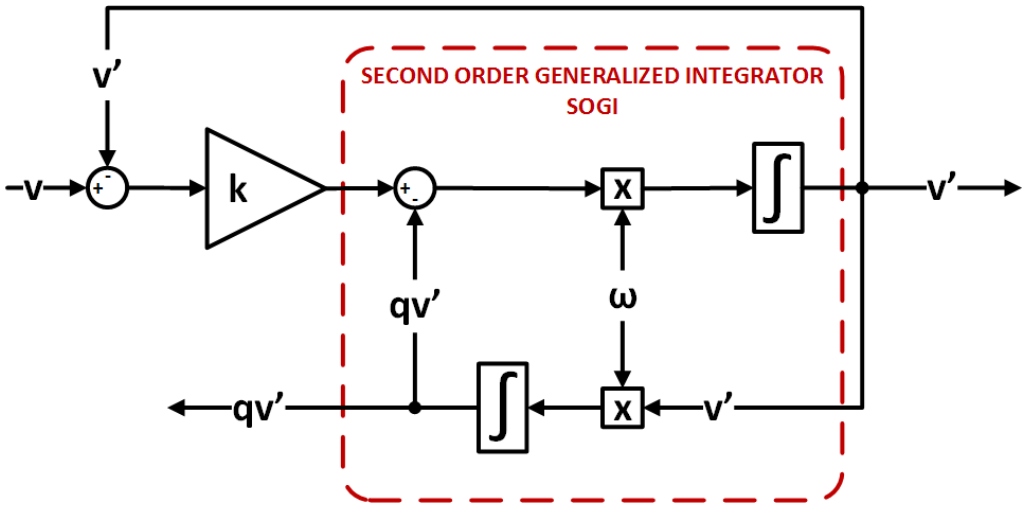


Figure 4.12 Orthogonal reference generator using SOGI.

The tuning of the proposed structure is frequency dependent if an adaptive tuning of ω is not implemented using a Frequency Locked Loop (FLL) [139], [143]. Using this method the supply voltage, *v,* is also filtered obtaining two clean waveforms, *v'* and *qv'*, in phase and quadrature with respect to the supply voltage. The filtering level is set from the value of k_{SOGI}:

- A low value of k_{SOGI} result in a narrow bandwidth which indicates heavy bandpass filtering around ω but with a slow dynamic response.
- A high value of k_{SOGI} results in a fast dynamic response but with a wide bandwidth which indicates light bandpass filtering around ω.

In order to be implemented digitally, the SOGI must be discretised. Several methods are possible such as forward and backward Euler discretisation or higher order discretisation methods [139]. During this work a backward Euler discretisation method is considered for simplicity.

4.3.2 Steady State Linear Kalman Filter PLL

The basic structure of the digital SSLKF PLL [138], [144] is shown in Figure 4.13 and is composed of three main blocks.

Starting from the supply voltage component in a stationary reference frame, v_α and v_β, the supply phase angle error can be approximated using the small signal approximation of the sine function of e_{PLL}, as follows.

$$e_{PLL} = \theta_m - \theta_e \cong \sin(\theta_m - \theta_e) = \sin(\theta_m)\cos(\theta_e) - \cos(\theta_m)\sin(\theta_e) =$$

$$= \frac{v_\beta \cos(\theta_e) - v_\alpha \sin(\theta_e)}{V_s} \tag{4.3}$$

In (4.3) θ_e is the estimated phase and V_s, θ_m are, respectively, the supply voltage amplitude and phase angle. The error is processed by the SSLKF which returns the new value of θ_m, used to calculate its sine and cosine value, and then fed back to the error calculation block. The SSLKF processes this error, generating a corrected value for θ_e. This is then used to calculate the sine and cosine values which are returned to the error calculation block.

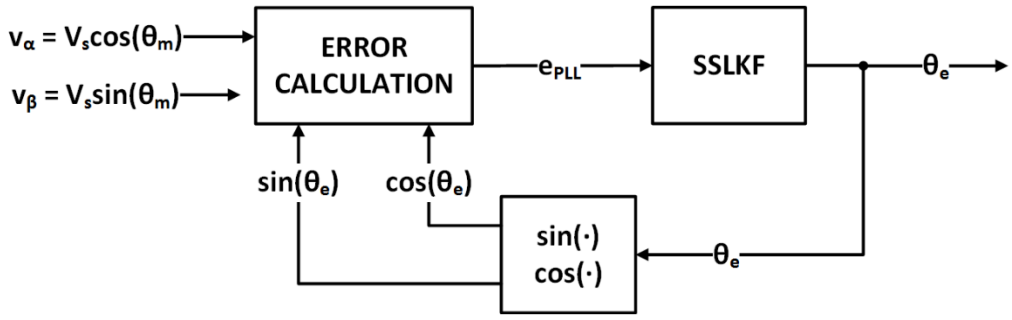


Figure 4.13 Steady State Linear Kalman Filter PLL

The Steady-State Linear Kalman Filter is designed to fit the stochastic discrete time model shown in (4.4), where:

- k is the actual sampling instant.
- T_s is the length of the sampling interval
- θ_m is the supply phase angle
- ω is the supply angular frequency
- a is the supply angular frequency derivative
- ξ is the zero-mean independent Gaussian white noise state vector with covariance matrix Q_{cov}
- η is the zero-mean independent Gaussian white noise on the scalar output with variance r.

$$\begin{cases} x_{PLL}(k) = Ax_{PLL}(k-1) + \xi(k) \\ y_{PLL}(k) = c^T x_{PLL}(k) + \eta(k) \end{cases} \quad x_{PLL} = \begin{bmatrix} \theta_m \\ \omega \\ a \end{bmatrix} \quad A = \begin{bmatrix} 1 & T_s & {T_s}^2 \\ 0 & 1 & T_s \\ 0 & 0 & 1 \end{bmatrix} \quad c = \begin{bmatrix} 1 \\ 0 \\ 0 \end{bmatrix} \tag{4.4}$$

The model of (4.4) can be estimated by using the Kalman filter algorithm. However, since the model is linear and time invariant, it is possible to approximate the Kalman filter gain sequence g_n with its limit g for k that tent to ∞, obtaining the following SSLKF which requires a lower computational effort.

$$\begin{cases} \tilde{x}_{PLL}(k) = A\hat{x}_{PLL}(k-1) \\ \hat{x}_{PLL}(k) = \tilde{x}_{PLL}(k) + g[\theta_m(k) - c^T x_{PLL}(k)] \end{cases} \tag{4.5}$$

The gain vector g depends on Q_{cov} and r and can be calculated by solving the relative Riccati equation or directly allocating the poles of SSLKF transfer function. In the second case g is calculated as demonstrated in [138]. The SSLKF PLL, compared with the traditional synchronous reference frame PLL provides a faster dynamic when frequency or phase variations are considered [138]. Moreover, since it is already designed in a discrete time system it has a straightforward digital implementation.

4.3.3 Root Mean Square detector

The voltage RMS value detection is based on the simple scheme shown in Figure 4.14. As stated in paragraph 4.3.1 the tuning of the SOGI based orthogonal system generator is critical when it is necessary to obtain unity gain between the supply voltage, *v*, and it's in phase and quadrature components, *v'*, *qv'*, especially if there is likely to be a wide range of supply voltage peak values.

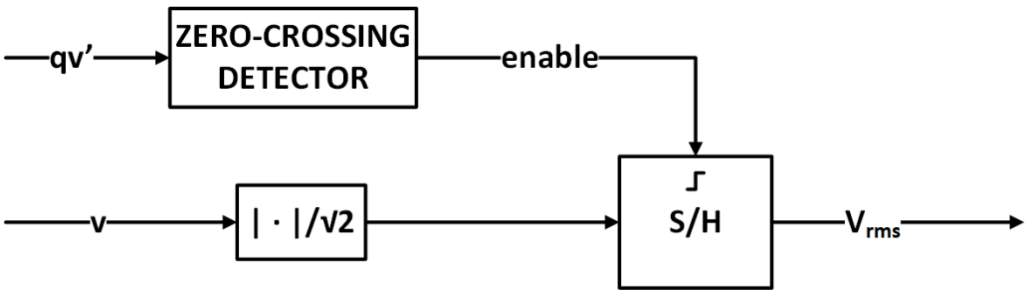


Figure 4.14 Zero-Crossing based rms detector.

However the SOGI can be tuned to maintain the phase shift between *v'* and *qv'* and have filtering performances that avoid multiple zero crossings for *v'* and *qv'*. In this case the supply voltage

RMS value can be calculated by detecting the zero-crossing of *qv'*, which corresponds to the time instant where *v* is a maximum or minimum. Then, dividing the absolute value of *v,* at the time instant when *qv'=0*, by √2, the supply voltage RMS value is obtained and held until the next zero-crossing of *qv'*. The proposed RMS detector provide an accurate measurement of the grid voltage RMS value; however, a maximum detection delay of half supply cycle has to be taken into account for the proposed system.

4.3.4 Proposed grid monitoring scheme simulation results

In Figure 4.15 simulation results for the single phase PLL under several operating conditions are shown. The SSLKF PLL has been designed with a narrower bandwidth, with respect to the single phase and three phase PLL. This bandwidth has been selected to be approximately 40Hz using the design instruction found in [138].

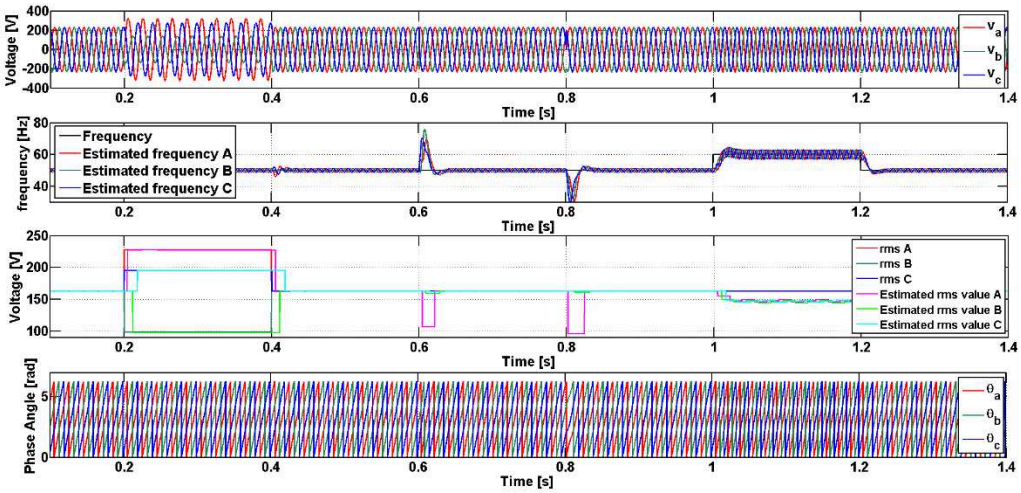


Figure 4.15 SSLKF PLL: overall response.

As for the single phase PLL, the SSLKF PLL is not affected by voltage unbalances, as shown in Figure 4.16; moreover, since the RMS value is calculated using the proposed RMS detector, the RMS value of each phase voltage is accurately estimated. In Figure 4.17 a phase jump of 60° is considered; in this case the PLL presents a fast response and recovers in less than one supply cycle. However since the RMS voltage value calculation is dependent on the phase voltage zero crossing during the SOGI transient estimation errors are present. This error does not affect the control significantly since the correct phase voltage RMS value is estimated at the next zero crossing event on the phase voltage. In Figure 4.18 a frequency variation from 50Hz to 60Hz is considered. It is clear on the produced waveforms that the three single phase PLLs quickly

recover with negligible frequency overshoot. Compared with Figure 4.5 a higher frequency ripple is present, mainly related with the tuning and discretisation of the SOGIs.

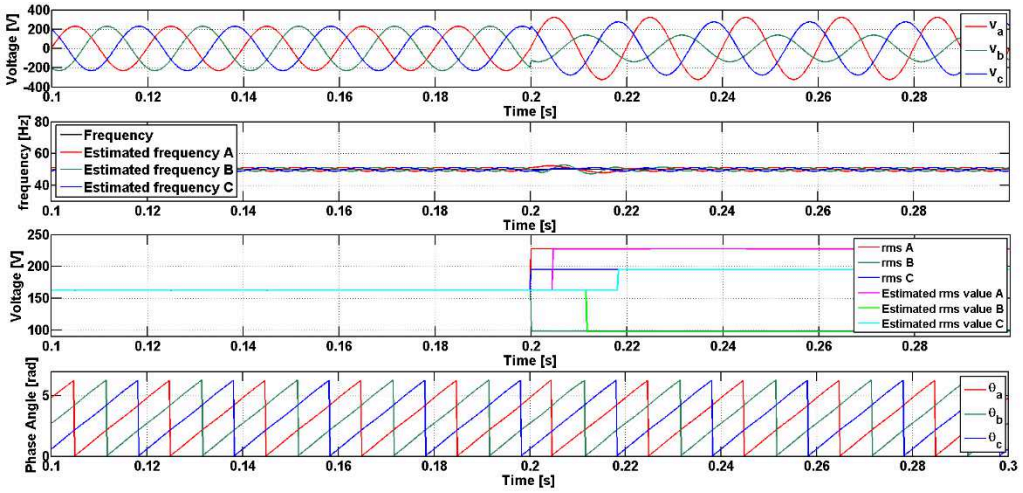


Figure 4.16 SSLKF PLL: response to voltage unbalances.

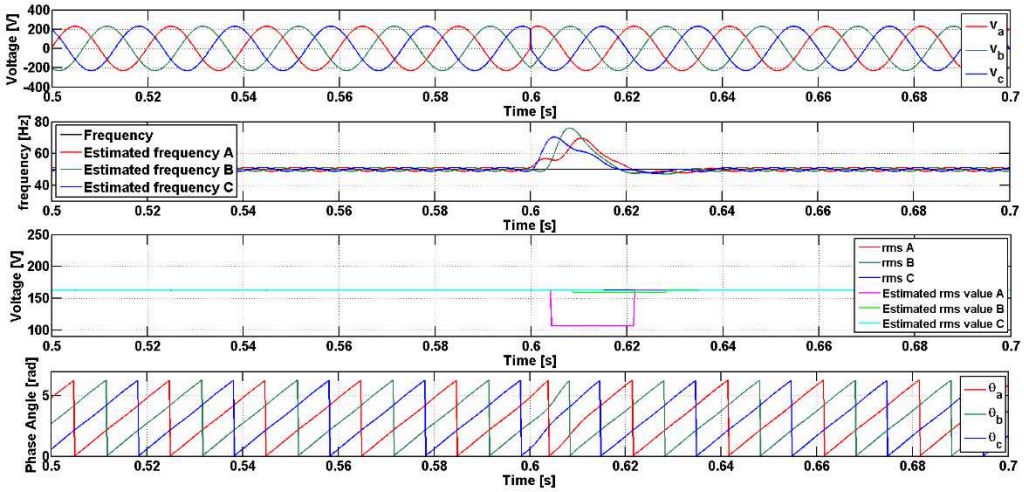


Figure 4.17 SSLKF PLL: response to phase jumps.

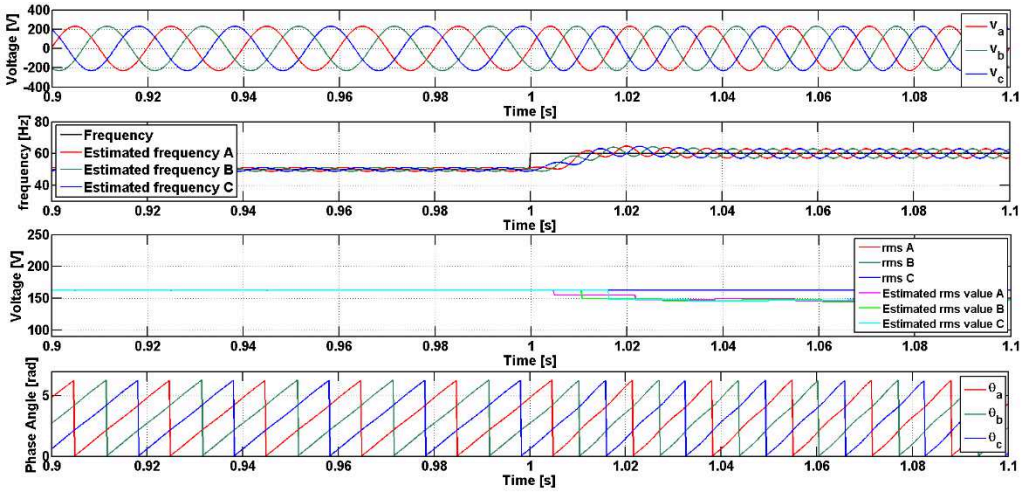


Figure 4.18 SSLKF PLL: response to frequency variations.

4.4 Chapter summary

In this chapter the grid monitoring system, necessary to achieve the desired synchronization between the AC currents and voltages waveforms, is described in detail for three possible structures:

- Classic three phase PLL.
- Classic single phase PLL.
- SSLKF single phase PLL.

In particular the latter presents a novel structure which includes three single phase PLLs based on a SOGI and a SSLKF. This structure presents benefits in terms of digital implementation and fault ride-through capabilities and will be considered in the rest of the thesis work.

Chapter 5
Control and modulation techniques for the multilevel Solid State Transformer

Several control and modulation techniques for the two port UNIFLEX-PM demonstrator, described in Chapter 3, have been proposed with the aim of providing the desired power flow with low current distortion, even during non-ideal grid conditions, whilst maintaining low losses and high converter reliability.

Four different controllers have been proposed, and are described in this chapter. In all of the cases described the converter gate drive signals are produced using a suitable modulation scheme. Four such modulation strategies, considered during the UNIFLEX-PM project, are presented in this chapter.

The aim of evaluating these control and modulation strategies is to provide a comparison framework for the novel control and modulation methods proposed in this work, and presented in later chapters.

5.1 Control techniques proposed for the multilevel solid state substation

Four different control strategies have been proposed for controlling the 2-Port SST developed during the UNIFLEX-PM project [123]:

- Synchronous reference frame control.
- Stationary reference frame control.
- Natural reference frame control.
- Predictive control.

These controllers are described in detail in the following sections for controlling the primary port of the UNIFLEX-PM demonstrator as shown in Figure 5.1. The control scheme on the secondary port is identical with the only difference that the total DC-Link voltage control is implemented only on the primary port.

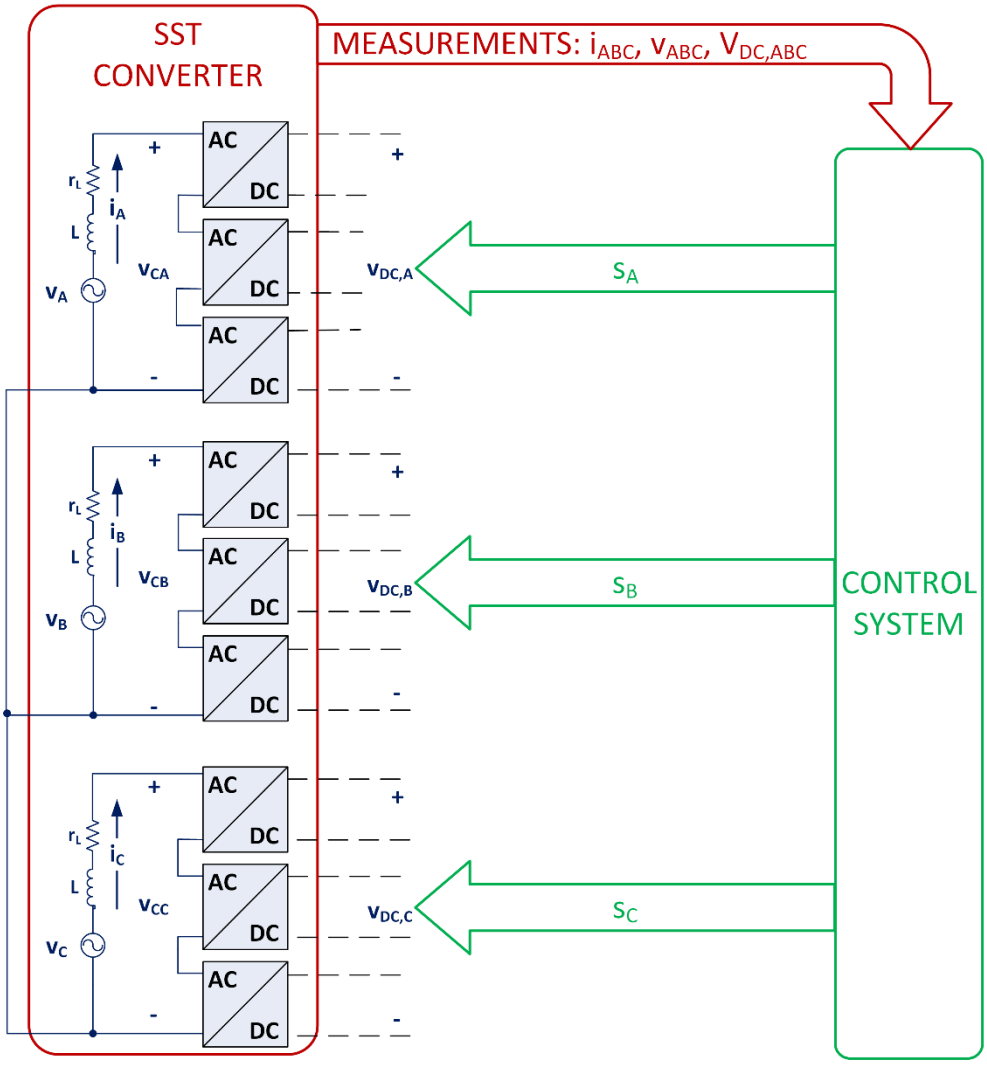


Figure 5.1 Considered SST converter circuit and general control scheme.

5.1.1 Synchronous reference frame control (dq)

A synchronous reference frame control scheme is shown in Figure 5.2 [123], [145]. In order to operate with unbalanced grid conditions the positive and negative sequences must be extracted and controlled separately using two different synchronous reference frames [146]–[148].

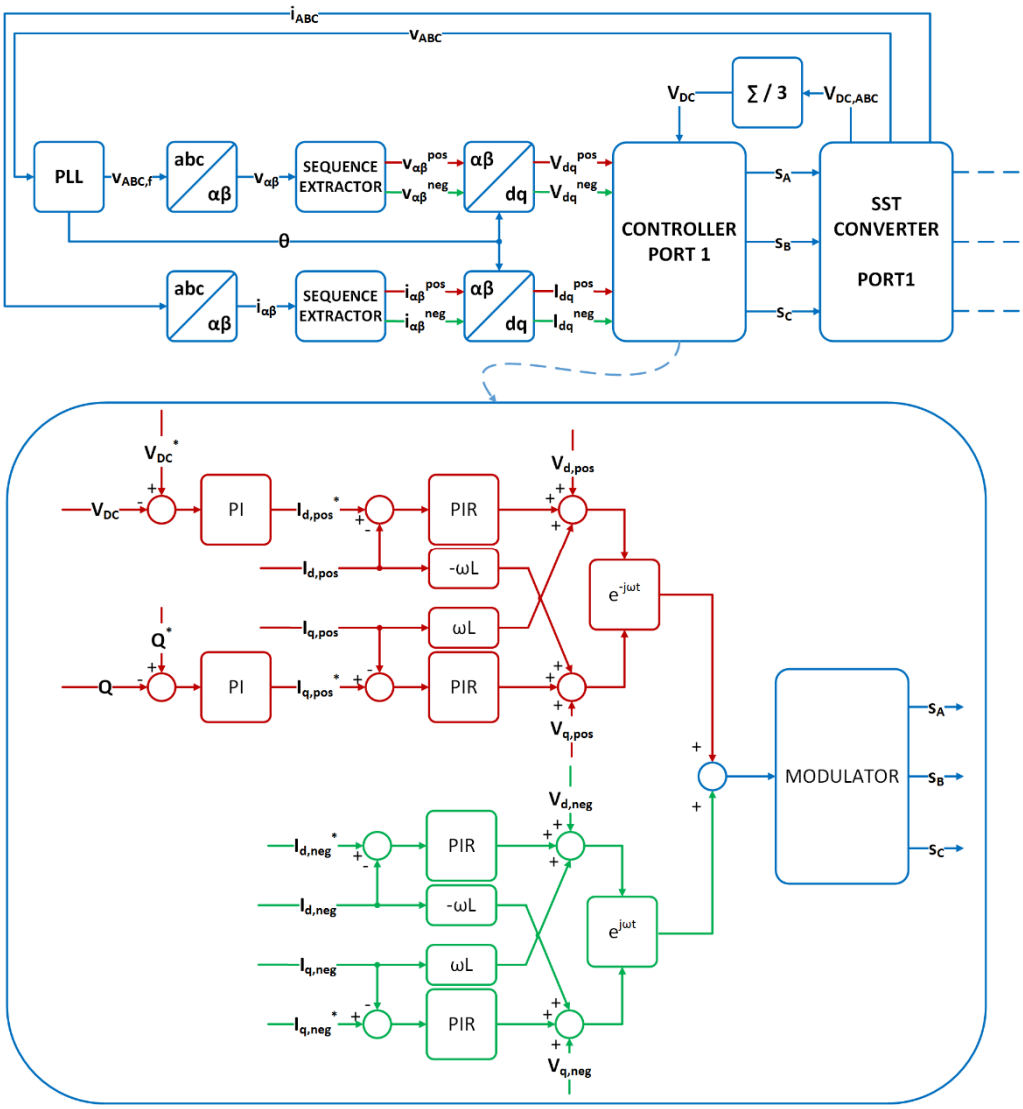


Figure 5.2 Overall control scheme of synchronous reference frame control on port 1 of the SST converter.

The positive and negative sequence components are extracted using a delay signal cancellation method, described in [149], [150]. A PLL is used to derive the grid voltage angle for the positive sequence. This is then used to generate a rotating reference frame, synchronised to the grid voltage positive sequence. In achieving this, the active power can be regulated by controlling the *d*-axis positive sequence current component while the reactive power can be regulated by controlling the *q*-axis positive sequence current component. Clearly, an advanced PLL scheme

is needed to extract only the positive sequence phase angle of the grid voltage [136], [138], [141], [142]. Four control loops are implemented to control, respectively, the *d*-axis and *q*-axis currents for both the positive and negative components. Two additional control loops are also necessary to generate the positive sequence *d*-axis and *q*-axis current references, $I_{d,pos}^*$, $I_{q,pos}^*$, in order to achieve, respectively, the desired DC-Link voltage, V_{DC}^*, and reactive power Q^*. A similar control is implemented on the secondary converter side with the only difference being that the DC-Link voltage control loop is substituted with an active power control loop. The negative sequence current references in the dq reference frame, $I_{d,neg}^*$, $I_{q,neg}^*$, are set to zero in order to provide only positive sequence (i.e. balanced) currents. The current control is implemented using four PI+Resonant (PIR) controllers [151]–[153] in order to achieve zero steady state error and suppress oscillations that may be present on the d-axis and q-axis current components for both sequences (as a result of harmonics, for example).

In general, a PIR control can be expressed as a combination of a proportional, integral and resonant control action. The transfer function of a PI controller is defined, in general, by a proportional gain, K_P, and an integral gain, K_I, as shown in (5.1).

$$G_{PI}(s) = K_P + \frac{K_I}{s} \tag{5.1}$$

The resonant term is defined by the transfer function defined in (5.2) where K_R is the resonant gain, ω_0 is the resonance frequency and Q is a quality factor that define the width of the resonance.

$$G_R(s) = \frac{sK_R}{s^2 + s(\omega_0/Q) + {\omega_0}^2} \tag{5.2}$$

The PIR controller transfer function is then defined adding (5.2) to (5.1) obtaining a parallel realisation of the PIR controller.

$$G_{PIR}(s) = G_{PI}(s) + G_R(s) = K_P + \frac{K_I}{s} + \frac{sK_R}{s^2 + s(\omega_0/Q) + {\omega_0}^2} \tag{5.3}$$

Figure 5.3 shows the Bode diagram for a PI and a PIR controller in order to demonstrate the effect of the resonant term. The PIR controller has the ability to obtain accurate current tracking and good dynamic performance even under unbalanced or distorted grid conditions [151]–[153].

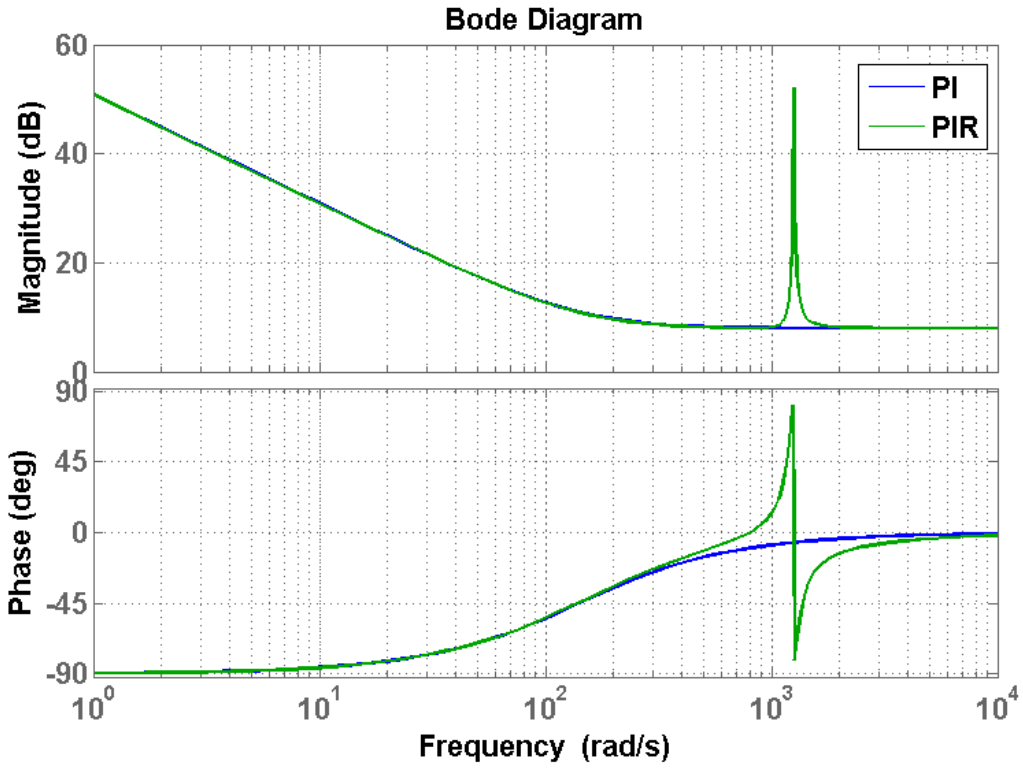


Figure 5.3 Bode Diagram of PI and PIR controller with K_P=2.5, K_I=350, K_R=500, ω_0=100Hz, Q=1000.

Simulation results for the synchronous reference frame control are shown in [123] with good current tracking under different operative conditions. It is clear from the results presented, however, that there is a coupling between the active and reactive power control which may require a more complicated control design.

5.1.2 Stationary reference frame control

Stationary reference frame control [61], [123] is an alternative to the more commonly used synchronous reference frame control schemes. A common structure for this control method is shown in Figure 5.4. In this case two control loops, utilising PI controllers, are implemented in a synchronous reference frame to indirectly regulate the active power, the DC-Link voltage and the reactive power, at the desired references P^*, V_{DC}^* and Q^*, generating respectively the desired *d*-axis current reference I_d^* and q-axis current reference I_q^*. The Active Power/DC-Link voltage control loop is supported by a feed forward term which represent the *d*-axis current necessary to obtain the desired active power P^*. However, since the feed forward term requires the online calculation of the grid voltage peak value, V_{peak}, if a disturbance is present on V_{peak}, this will cause distortion of the current references calculated in the synchronous reference frame. The

reactive power control loop is also supported by a feed forward term which represents the q-axis current necessary to obtain the desired reactive power Q^*. The feed forward compensation allow the PI regulators to manage only the necessary variation from the nominal current reference values, representing the current required to supply the converter losses for the current set point.

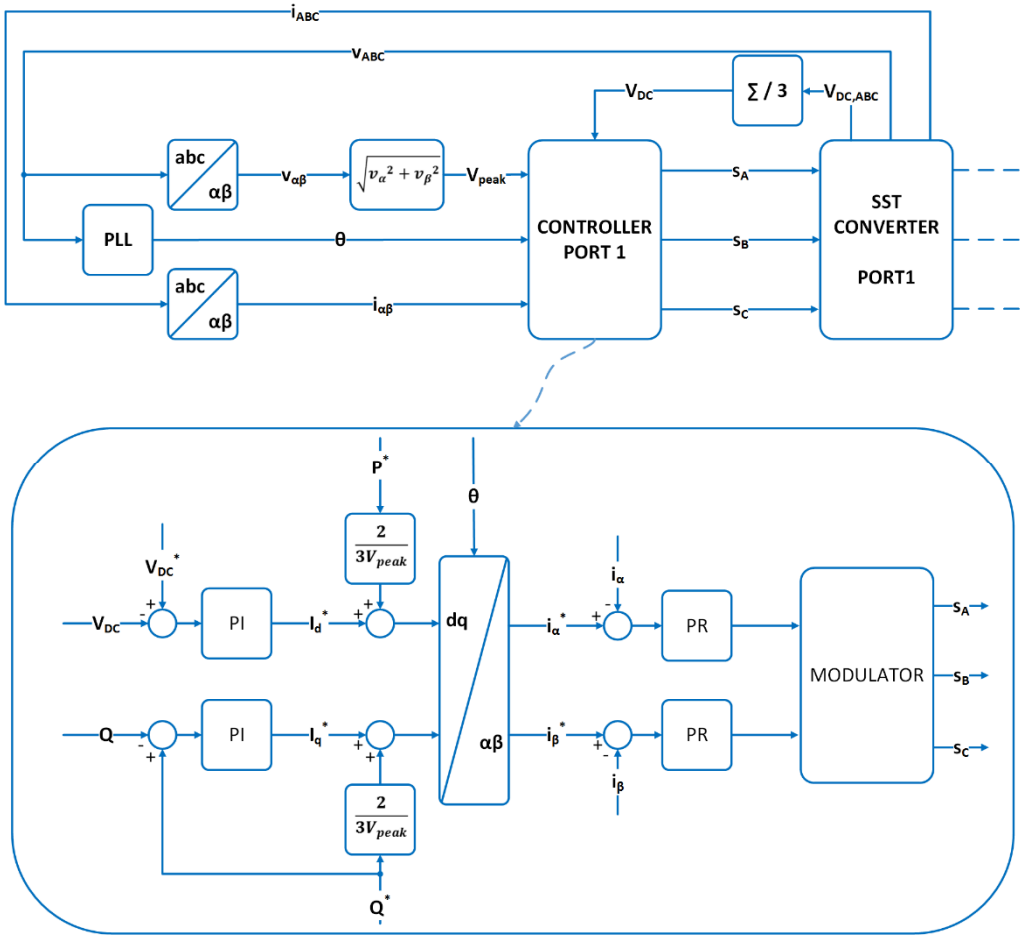


Figure 5.4 Overall control scheme of stationary reference frame control on port 1 of the SST converter.

The current control is implemented in a stationary reference frame, the dq current references, I_d^*, I_q^*, are transformed into $\alpha\beta$ coordinates, i_α^*, i_β^*, using the grid voltage phase angle, obtained from a PLL. As for the synchronous reference frame control, described in the previous section, the PLL has to be able to extract only the phase angle of the grid voltage positive sequence component and advanced PLL schemes have to be considered [136], [141], [142]. In order to control sinusoidal current references, two PR controller are implemented. PR control has good AC current tracking providing zero error at its designed frequency without voltage feed forward terms, improving reliability and operation in the presence of a distorted grid. PR controllers can be expressed in the s domain as shown in (5.4).

$$G_{PR}(s) = K_P + \frac{sK_R}{s^2 + s(\omega_0/Q) + {\omega_0}^2} \tag{5.4}$$

Simulation results are shown in [123]. Stationary reference frame control produces good current tracking. The control method is also proved to be robust in the presence of voltage amplitude variations, phase and frequency excursion and naturally suppresses AC distortion associated with DC-Link voltage ripple feed-through.

5.1.3 Natural reference frame control

Natural reference frame control [54], [123] allows independent control of each phase of the SST, allowing better management of faults and grid voltage unbalance conditions. As shown in Figure 5.5, two PI control loops are implemented in order to regulate, respectively, Active Power/DC-Link voltage and reactive power at the desired references P^*, $V_{DC}{}^*$ and Q^*.

Clearly such a control structure has been specifically designed to be applied on three-phase, four wire systems; in fact, in case of grid voltage unbalances, a zero-sequence current is generated in order to maintain the power balanced between the phases. On the other hand, in case of three wire systems it is not possible to generate a zero sequence current and natural reference frame control may cause power unbalances, or other undesirable operation, between phases when in presence of grid voltage unbalances.

The Active Power/DC-Link voltage control generates the active current reference amplitude $I_d{}^*$, with the support of a feed forward term that represents the active current amplitude necessary to obtain the desired power flow. As for stationary reference frame control, the feed forward term is calculated using the grid voltage peak value, V_{peak}, and distortion on this term may introduce a distortion in the current references calculated in the synchronous reference frame. The reactive power control loop generates the reactive current reference amplitude $I_q{}^*$. Also in this case a feed forward compensation is implemented.

Three single phase PLLs are implemented to generate the active current references and reactive current references on each phase which, when added together, constitute the desired current references on each phase, $i_a{}^*$, $i_b{}^*$, $i_c{}^*$. The use of single phase PLL is necessary to allow independent detection of the grid voltage amplitude and angle on each phase, improving the converter ride-through capabilities [54], [123].

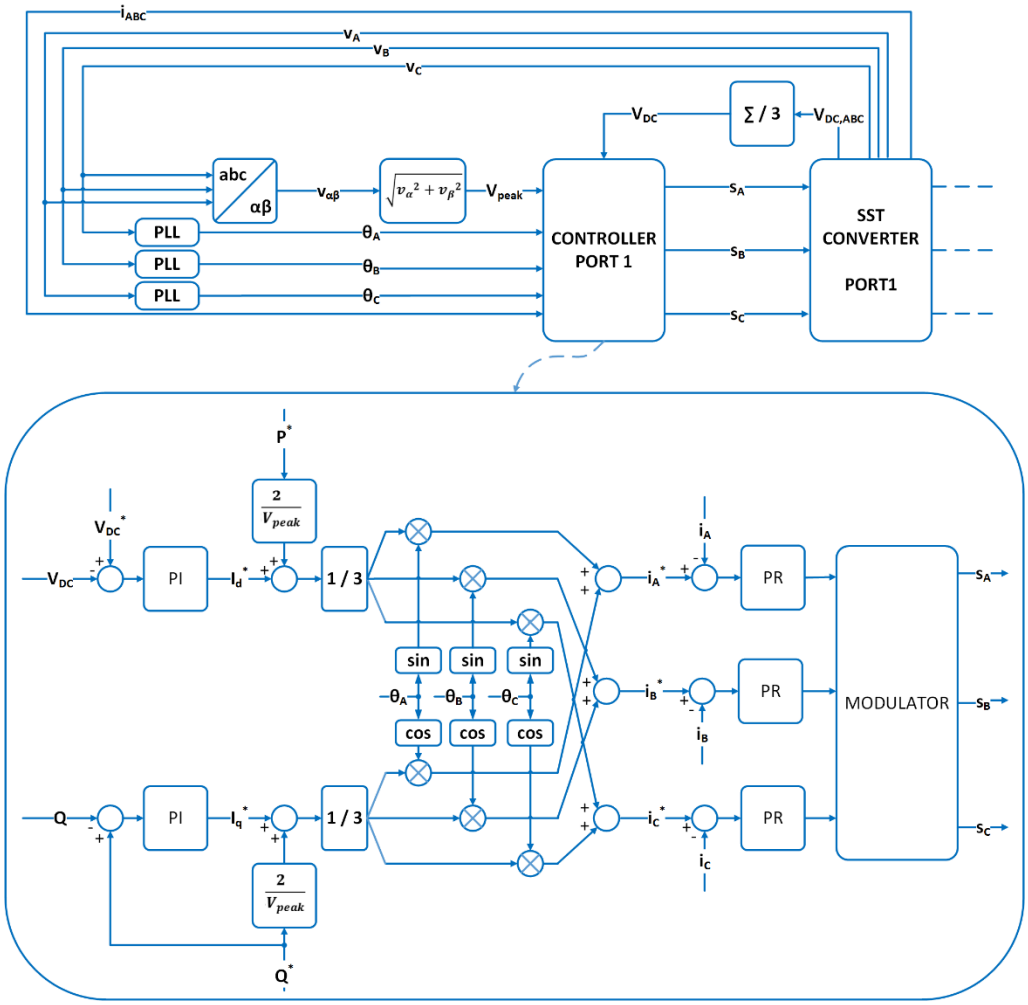


Figure 5.5 Overall control scheme of natural reference frame control on port 1 of the SST converter.

Three PR controllers are used to control the AC current. Simulation results are shown in [123] demonstrating fast power flow control capability and DC-Link voltage stability. Moreover the control maintains good performance under non ideal grid conditions such as supply voltage excursions, unbalance and phase jumps.

5.1.4 Predictive control

Amongst all the family of predictive controllers, described in Chapter 2, a Dead-Beat control scheme [54], [123], [145] for four wire three phase systems in a natural reference frame has been proposed for the SST developed during the UNIFLEX-PM project.

Similarly to the control described in the previous section, the presented method allows independent control of each phase and a zero-sequence current may be generated in order to maintain the power equally shared between the phases when a grid voltage unbalance is present,

if and only if a four wire, three phase system is considered. In the case of an unbalanced three wire system if the power is not equally shared between the phases and it may results in DC-Link voltage regulation issues.

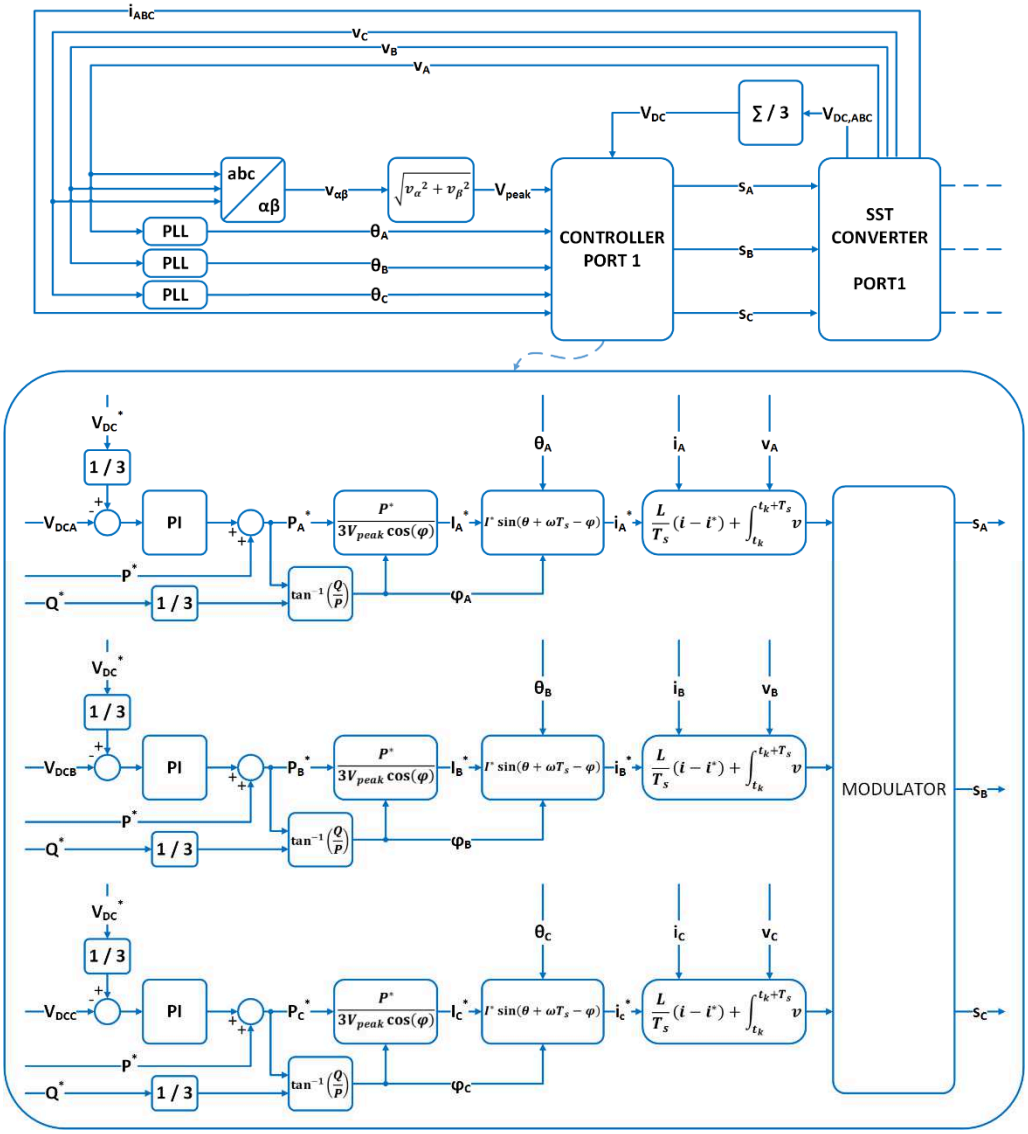


Figure 5.6 Overall control scheme of predictive (dead-beat) control on port 1 of the SST converter.

The control scheme of Figure 5.6 shows the Dead-Beat control implementation for the primary side. The control of the secondary side is identical with the exception of the outer control loop necessary to control the DC-Link voltage. For the primary side a PI control loop is implemented to regulate the DC-Link voltage at the desired reference V_{DC}^*, producing at its output the active power demand necessary to correctly regulate the DC-Link voltage. The active and reactive power references, P^*, Q^*, plus the output of the PI control loop are then used to calculate the

desired line current amplitudes, I_a^*, I_b^*, I_c^*, and the phase shift between grid voltage and current on each phase, φ_a, φ_b, φ_c, on the basis of the active and reactive power definitions shown in (5.5) and (5.6).

$$P = \frac{V_{peak} I_{peak}}{2} \cos(\varphi) \tag{5.5}$$

$$Q = \frac{V_{peak} I_{peak}}{2} \sin(\varphi) \tag{5.6}$$

From (5.5) and (5.6) it is possible to obtain the desired current reference amplitude and phase shift as defined in (5.7) and (5.8).

$$I_j^* = \frac{2\left(\frac{P^*}{3}\right)}{V_{peak} \cos(\varphi_j)} \quad , \quad j = a, b, c \tag{5.7}$$

$$\varphi_j = \operatorname{atan}\left(\frac{3Q^*}{P^*}\right) \quad , \quad j = a, b, c \tag{5.8}$$

The current reference is then calculated considering the voltage angles obtained by three single phase PLLs, θ_a, θ_b and θ_c. As for PR natural reference frame control, the use of a single phase PLL increases the converter ride-through capabilities [54], [123] by detecting the grid voltage angle independently on each phase. The current references are calculated as shown in (5.9), (5.10) and (5.11).

$$i_a^*(t_k + \omega T_s) = I_a^* \sin(\theta_a - \varphi_a + \omega T_s) \tag{5.9}$$

$$i_b^*(t_k + \omega T_s) = I_b^* \sin(\theta_b - \varphi_b + \omega T_s) \tag{5.10}$$

$$i_c^*(t_k + \omega T_s) = I_c^* \sin(\theta_c - \varphi_c + \omega T_s) \tag{5.11}$$

The term ωT_s is added in order to consider the current reference at the desired sampling instant. For the given references, the Dead-Beat control law generates, independently on each phase, the desired converter voltage reference in order to obtain zero current error at the next sampling period by using the demanded current for the next sampling instant as a reference.

$$v_{c1A}^*(t_k + \omega T_s) = v_{1A}(t_k + \omega T_s) + \frac{L}{T_s}[i_a^*(t_k + \omega T_s) - i_a(t_k + \omega T_s)] \tag{5.12}$$

$$v_{c1B}^*(t_k + \omega T_s) = v_{1B}(t_k + \omega T_s) + \frac{L}{T_s}[i_a^*(t_k + \omega T_s) - i_a(t_k + \omega T_s)] \tag{5.13}$$

$$v_{c1C}^*(t_k + \omega T_s) = v_{1C}(t_k + \omega T_s) + \frac{L}{T_s}[i_a^*(t_k + \omega T_s) - i_a(t_k + \omega T_s)] \tag{5.14}$$

A detailed description of Dead-Beat control is given in Chapter 7, including practical implementation issues. Simulation results are provided for Dead-Beat current control of the two port SST in [54], [123], [145] demonstrating a fast active and reactive power tracking even under extreme grid voltage disturbances.

5.2 Modulation techniques for UNIFLEX-PM converter

As already described in Chapter 2, PWM techniques currently in literature can be divided in two main classes: carrier based PWM in which the switching instants are determined by the intersection of a sinusoidal reference signal with carrier signals, and calculation based PWM in which the switching instants are calculated in every sampling period by a specific procedure.

The most common carrier based methods are Phase-Shifted Carrier Modulation (PSCM) [154], [155] and Level Shifted Carrier Modulation (LSCM) [117], [156]. PSCM had the advantage that naturally absorbs equal power from each DC-Link. It is, however, inferior with regards to THD when compared with some types of LSCM in a three phase system [117].

Amongst the different calculation based PWM for single-phase Cascaded H-Bridge converters, the most common include Selective Harmonic Elimination (SHE) [155]–[164], which aims to reduce or eliminate low order harmonics whilst controlling the fundamental component of a generic waveform, and single-phase versions of Space Vector Modulation, denoted as Average Value Modulation (AVM) [103] and 1-Dimentional Modulation (1DM) [165], [166], both based on the application of the two nearest voltage levels. SHE techniques are able to switch the converter devices at the supply fundamental frequency but are not strictly a PWM technique; thus, they have not been considered for this particular application.

For all the aforementioned reasons, PSCM, AVM and 1DM are considered and described in detail in the following sub-sections.

5.2.1 Phase Shifted Carrier Pulse Width Modulation

Multi-carrier PWM strategies are well researched in literature and can be implemented with different arrangements of modulating and carrier signals. The most popular is the PSCM method which is frequently applied to CHB based converter structures. For an n-cell converter n-carrier signals phase shifted by π/n, one for each of the n H-Bridges cascaded in a single multi-level phase, are used. Adding the n output voltages of the n cascaded H-Bridge cells, will result in an output voltage with up to $2n+1$ levels as shown in Figure 5.7 for a 7-level CHB.

Using such an approach, the cancellation of all carrier harmonics groups up to the n^{th} carrier is obtained. PSCM modulation has the following positive effects:

- Every cell shows the same moving average value, so the switching, conduction loss and power is equally shared amongst the H-Bridge cells of the converter.
- There is never a voltage cancellation of a positive voltage step of a cell by a negative voltage of another [154].

In Figure 5.7 an example of operation of PSCM on a single phase 7-level CHB converter is presented. It possible to observe that the commutations are distributed evenly amongst the HBs and that voltage cancellation is avoided as expected.

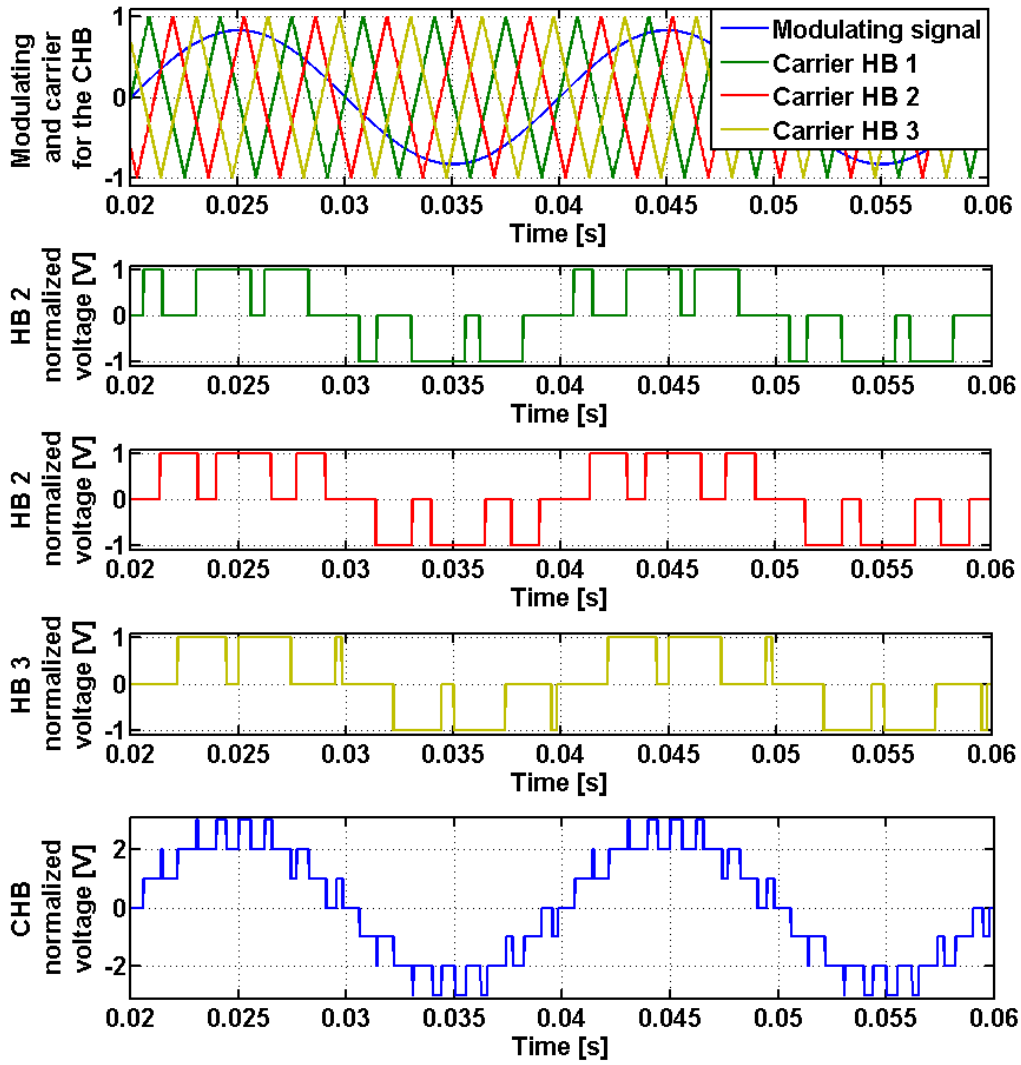


Figure 5.7 PSCM working principle applied to a 7-level CHB.

The main drawback associated with PSCM is represented by the generation of low order harmonics if an imbalance on the DC-link voltages occurs [154]. Moreover, from a practical point of view, an *n*-cell cascaded converter requires *n* hardware timers for the generation of the

carrier waveforms. As a consequence, for high values of n, different microcontrollers should be employed and synchronized, or further hardware (such as an FPGA) may be required.

5.2.2 Space Vector Modulation

Two different SVM schemes have been considered AVM [103] and 1DM [165], [166]. Both schemes are suitable for applications on a CHB based SST converter.

5.2.2.1 Average Voltage Modulation

This method, proposed in [103], is achieved by applying the two adjacent converter voltage levels from the possible $2n+1$ at each sampling period, T_s, to create the required voltage reference, v_c^*. The two levels are time weighted to achieve the condition that the time integral of the voltage command must be equal to the sum of the time integrals of the selected voltages. In order to calculate the time intervals in which the selected voltage levels have to be applied, equation (5.15) has to be considered.

$$\int_{t_k}^{t_k+T_s} v_c^* dt = V_n t_1 + V_{n+1} t_2 \tag{5.15}$$

V_n and V_{n+1} represent the input voltage vectors selected during the time period of t_k ... t_k+T_s. V_n is the voltage level immediately below v_c^* and V_{n+1} is the voltage level immediately above v_c^*. Hence, t_1 and t_2 represent the on-duration times intervals associated with V_n and V_{n+1} respectively. The values of t_1 and t_2 must always satisfy (5.16).

$$t_1 + t_2 = T_s \tag{5.16}$$

Since the voltage command, v_c^*, is maintained constant during one period of the switching cycle, it is possible to assume that:

$$v_c^* T_s = V_n t_1 + V_{n+1} t_2 \tag{5.17}$$

From (5.16) and (5.17) it is easy to obtain the two switching intervals t_1 and t_2. Such a technique assures that, in the considered application, commutations are performed only between adjacent voltage levels; however, the commutations are not equally distributed during the modulation period and amongst the different converter cells. This may result in asymmetric loss distribution amongst the H-Bridge cells as shown from the simulations results in [103].

3.2.2.2 1-Dimensional Modulation

Another method based on the selection on the two nearest voltage levels is the single-phase multi-level 1DM technique [165], [166] which can additionally employ redundant states to obtain either a cell power equalisation, or a minimisation of the commutations of the converter. The possible converter states are represented in a one-dimensional region, grouped by the different converter voltage that they can produce. Referring to the 5-level CHB of Figure 2.6 and using the notation introduced in Section 2.1.3 the possible converter states in the one dimensional region can be calculated as shown in Figure 5.8.

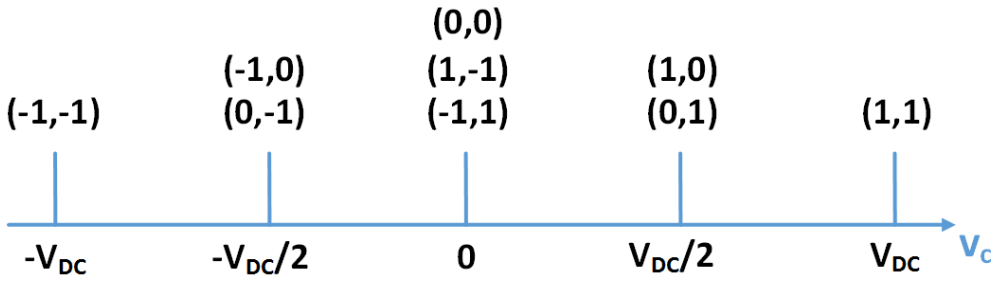


Figure 5.8 One-dimensional region for a 5 level CHB.

Based on the converter voltage reference v_c^*, the modulator chooses the converter states to be applied between the one that can produce the two nearest voltage levels to v_c^*. In the example of Figure 5.9, considering the DC-Link voltages balanced at $V_{DC}/2$, the switching instants can be calculated as follows for a sampling interval T_s.

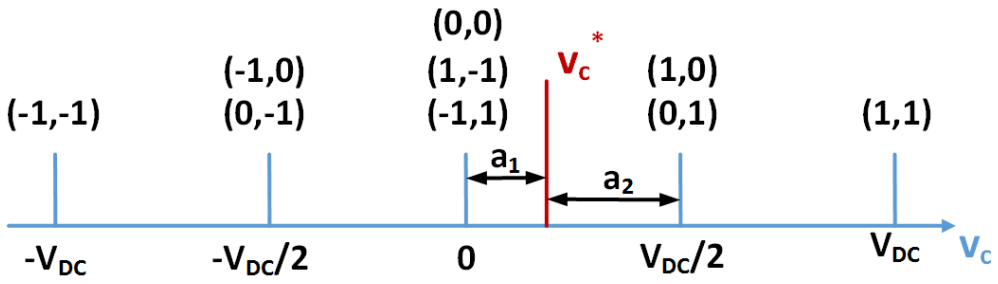


Figure 5.9 First example of 1DM working operation.

The results of the 1DM modulation algorithm is a vector able to produce a zero voltage level for a time interval t_1 and a vector that can produce a voltage value of $V_{DC}/2$ for a time interval t_2 as defined by (5.18) and (5.19).

$$t_1 = \frac{2}{V_{DC}}(a_1 - 0)T_s \tag{5.18}$$

$$t_2 = \frac{2}{V_{DC}}\left(a_2 - \frac{V_{DC}}{2}\right)T_s \tag{5.19}$$

The state redundancy can be used to minimise the commutations in the converter cells or balance the voltage on the DC-Link capacitors.

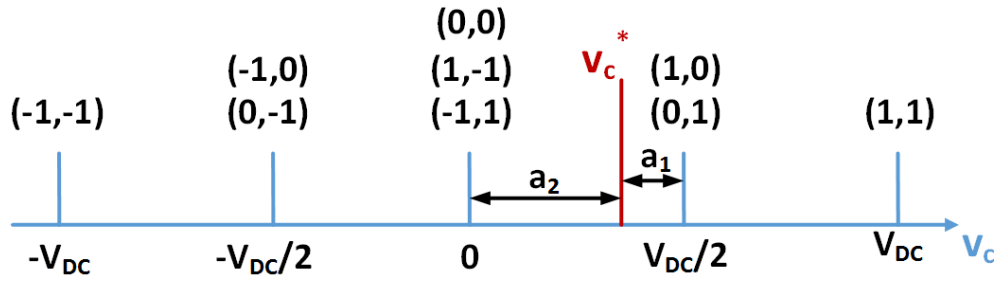


Figure 5.10 Second example of 1DM working operation.

If a v_c^* is closer to $V_{DC}/2$, as shown in Figure 5.10, this voltage level is applied first for a time interval, t_1, and the zero voltage level is applied for a time interval, t_2, calculated as shown in (5.20) and (5.21).

$$t_1 = \frac{2}{V_{DC}}\left(a_1 - \frac{V_{DC}}{2}\right)T_s \tag{5.20}$$

$$t_2 = \frac{2}{V_{DC}}(a_1 - 0)T_s \tag{5.21}$$

The main advantage of 1DM is to propose a unified SVM scheme for single phase multilevel CHB converters [165] independently from the DC-Link voltage levels using predefined lookup tables that consider the ratio between the voltages on the DC-Link capacitors and the sign of the current flowing into the converter [166]. Moreover, by ensuring that only one commutation occurs per sampling period asymmetric voltage pulses are obtained from the converter reducing the harmonic distortion of the composite converter voltage waveform.

However, such a method does not evenly distribute the commutations amongst the cells and does not impose a constraint ensuring one commutation per sampling period. These two features are important in high power applications where a reduced number of commutation implies a reduction in losses and heating stress of the devices.

5.3 Control method used for the SST of the UNIFLEX-PM project

Experimental tests have been previously performed on the UNIFLEX-PM converter described in Chapter 3 using the simplified synchronous reference control scheme of Figure 5.11 [44], [167], [168].

The DC-Link voltage control is achieved, as for the scheme of Figure 5.11 using a PI controller that generates the desired *d*-axis current I_d^*. The *q*-axis current reference is chosen directly from the user in order to achieve the desired reactive power, omitting the PI control on the reactive power in order to release computational resources on the DSP.

The current control is implemented using a feed-forward controller. Neither the three phase sequence decomposition method nor the PIR current controller had been implemented, in contrast with the control scheme of Figure 5.2. For this reason the control scheme of Figure 5.11 is not capable of operating effectively in the presence of unbalances in the grid voltage.

In order to consider load current unbalances and asymmetries in the single HB, an additional DC-Link voltage balancing control is necessary to maintain the balanced power flow towards each cell [133], [162], [167]. The DC-Link voltage balancing control requires three PI controllers for each phase. Each PI control regulator modifies the modulation index of the single HB cell in order to obtain balanced DC-Link voltages as shown in Figure 5.11. The modified modulation index $\hat{m}_{ij}$ are calculated using the following expression.

$$\hat{m}_{ij} = k_{ij} m_{ij} = \frac{\Delta_{ij}}{\sum_{k=1,2,3} \Delta_{kj}} m_{ij} \quad , \quad i = 1,2,3 \quad , \quad j = a,b,c \tag{5.22}$$

Where k_{ij} is the modulation index variations required by the PI controllers, based on their outputs Δ_{ij}, and m_{ij} is the modulation index for the *i*-th HB of the *j*-th phase calculated by the current control.

Experimental results are shown in [44], [133], [167] demonstrating good performance under balanced load conditions. However this is the only control scheme that has been implemented on the UNIFLEX-PM converter and, as stated before, the control response to grid voltage unbalances and variations, in frequency, amplitude and phase, has not been analysed and tested experimentally.

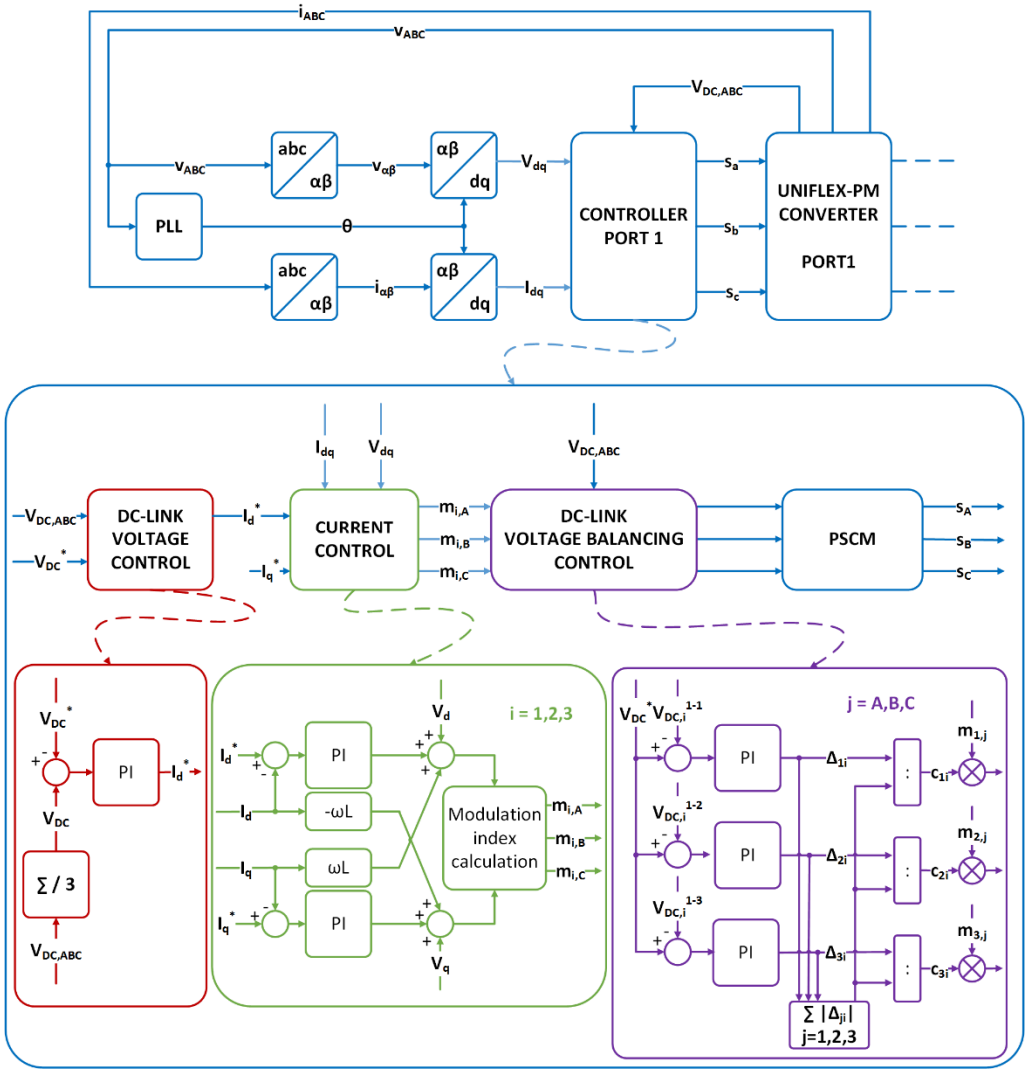


Figure 5.11 Simplified control scheme of synchronous reference frame control on port 1 of the UNIFLEX-PM converter (used in experimental tests).

5.4 Model Predictive Control

Amongst the control techniques that have not been considered in [123] Finite Control Set Model Predictive Control, denoted also for sake of simplicity as Model Predictive Control (MPC) [71], [73]–[78], represents a viable alternative to the control techniques presented in the previous sections. In the past decade, MPC has been widely proposed as a promising solution for the control of power converters due to its fast dynamic response, lack of modulation, easy inclusion of nonlinearities and constraints of the system, possibility of incorporating nested control loops in only one loop and the flexibility to include other system requirements in the controller [55], [71], [72], [78]–[84].

MPC uses a converter model to predict its future behaviour over a finite time horizon. On the basis of this model, MPC solves an optimisation problem where a sequence of future actuations is obtained by minimising a cost function which represents the desired behaviour of the system. The best performing actuation is then applied and all the calculations are repeated every sample period. Considering that power converters are systems with a finite number of states, given by the possible combinations of the state of the switching devices, the MPC optimisation problem can be simplified and reduced to the prediction of the behaviour of the system for each possible state. Then, each prediction is evaluated using the cost function and the state that minimises it, is selected [71]. This is a different approach that has been successfully applied for the current control in a three-phase inverters [83], [100], matrix converters [80], [101], active rectifiers [102], [103], and control of induction machines [98], [104]–[108]. The main drawbacks of MPC are:

1. The absence of a modulator forces the control to choose only amongst a limited number of converter switching states, applied for the whole sampling period. This generates a larger ripple in the system waveforms, and results in an increased (and variable) switching frequency in comparison to other control solutions.
2. The absence of a PWM technique forces the control to produce fixed width pulses resulting in a degradation of the converter voltage THD, especially for low values of switching frequency.
3. For multilevel converters with a high numbers of levels MPC requires significant computational effort, resulting in a complicated practical digital implementation.

5.5 Chapter summary

In this chapter the control and modulation techniques already proposed during the UNIFLEX-PM project are described in details highlighting advantages and disadvantages of the different techniques.

In particular, four different control structures, in synchronous, stationary and natural reference frames, are described in detail. These techniques include linear controllers such as PI, PR, PIR regulators and Dead-Beat controllers.

Three different modulation techniques for CHB converters are described. In particular the attention was focused on PSCM and two different SVM schemes, respectively named AVM and 1DM.

Between all the proposed control and modulation techniques, a synchronous reference control with PI regulator and active DC-Link capacitor voltages control, which has been previously implemented for experimental testing on the UNIFLEX-PM demonstrator, is described in detail.

In order to propose an alternative to the previously tested control methodology, the MPC concept is introduced, describing its advantages and disadvantages; several applications in which MPC approach has been successfully proposed has been also described. In particular in [78], [169]–[171], MPC is applied to CHB converters demonstrating its effectiveness as a control method for the SST considered in this work. The MPC derivation is described in Chapter 8 while in Chapter 9 a novel MPC control that include a modulation technique in the minimisation process is presented.

Chapter 6
Novel modulation techniques for Cascaded H-Bridge converters

This chapter describes a novel modulation technique, particularly suitable for high-power CHB converters and named Distributed Commutation Modulation (DCM). The DCM strategy aims to minimize the converter commutations and distribute them, for any amplitude of the voltage reference, equally amongst the different converter cells. In order to improve the system operating performance when power unbalance between the cells is present, an extension to the DCM algorithm is also proposed in this chapter. This aims to minimise the unbalance of the DC-Link voltages across the different converter cells in order to obtain high-quality waveforms and maintain converter modularity. Moreover the device voltage drop and on-state resistance, which may be of use in lower voltage applications such as those relating to automotive drive, are compensated. Simulation and experimental results are included in order to validate the proposed modulation technique used in conjunction with the DBC described in Chapter 7.

6.1 Distributed Commutation Modulator

This section presents a novel dedicated PWM technique for use with single-phase (or multi-phase) multi-level Cascaded H-Bridge Converters. The proposed modulation strategy aims to minimise the converter commutations and distribute them, for any amplitude of the voltage reference, amongst the different converter cells in order to evenly distribute the stress on the power switches, improving their reliability, without compromising the quality of the voltage waveform. Such characteristics are particularly important in high power grid-connected converters used as an interface for renewable energy sources or Smart Grid applications.

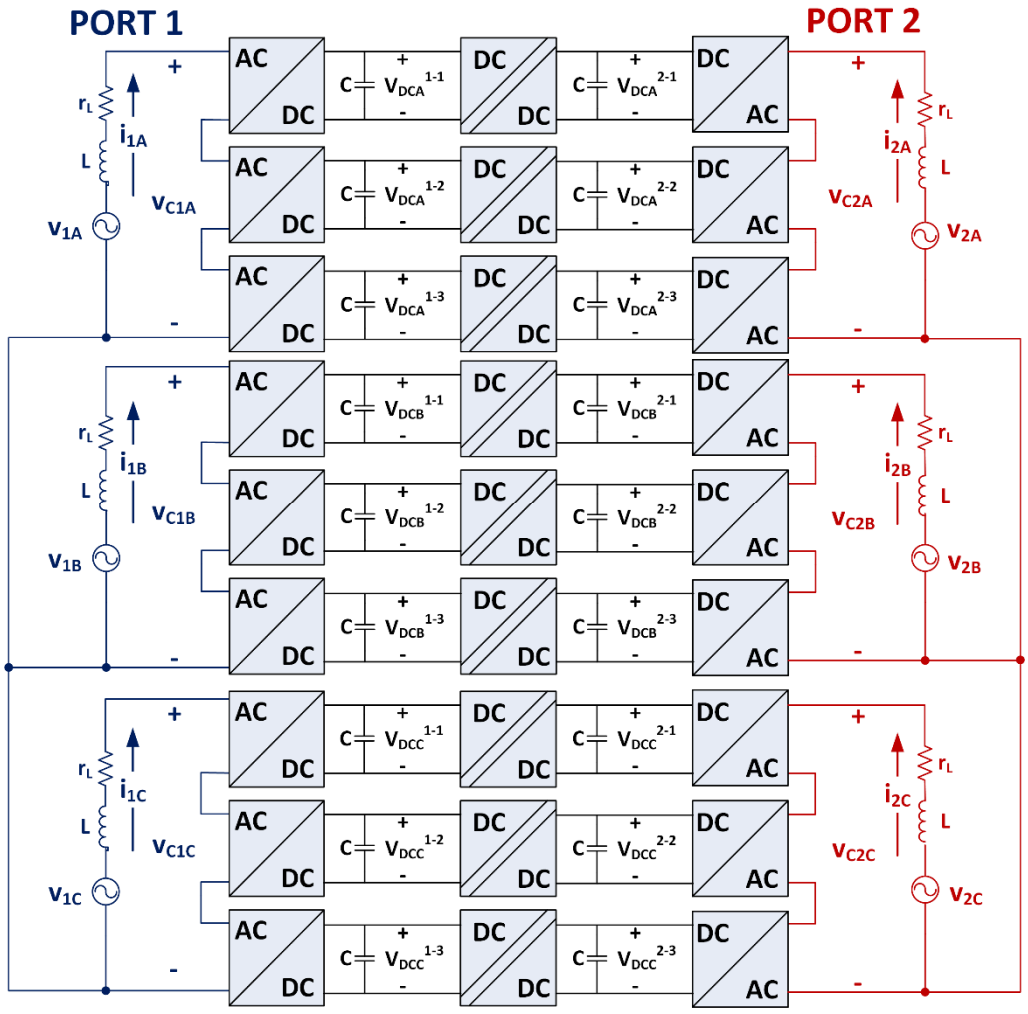


Figure 6.1 UNIFLEX-PM demonstrator two ports converter structure.

When the CHB converter is used in active rectifier configuration, in operating conditions where an unbalance in power flow between the single HB cells is produced, an unbalance on the DC-Link voltages is produced; in this case an active DC-Link voltage balancing technique is

proposed with the aims to minimise the unbalance of the DC-Link voltages, for any amplitude of the voltage reference, amongst the different converter cells in order to obtain high-quality waveforms with a low switching frequency.

Moreover the device voltage drop and on-state resistance, which in high-power, low voltage applications such as automotive applications may have a significant impact on the quality of the produced voltage, are compensated. The proposed modulation technique is described referring to the port 1, phase A of UNIFLEX-PM demonstrator shown in Figure 6.1, highlighted in Figure 6.2.

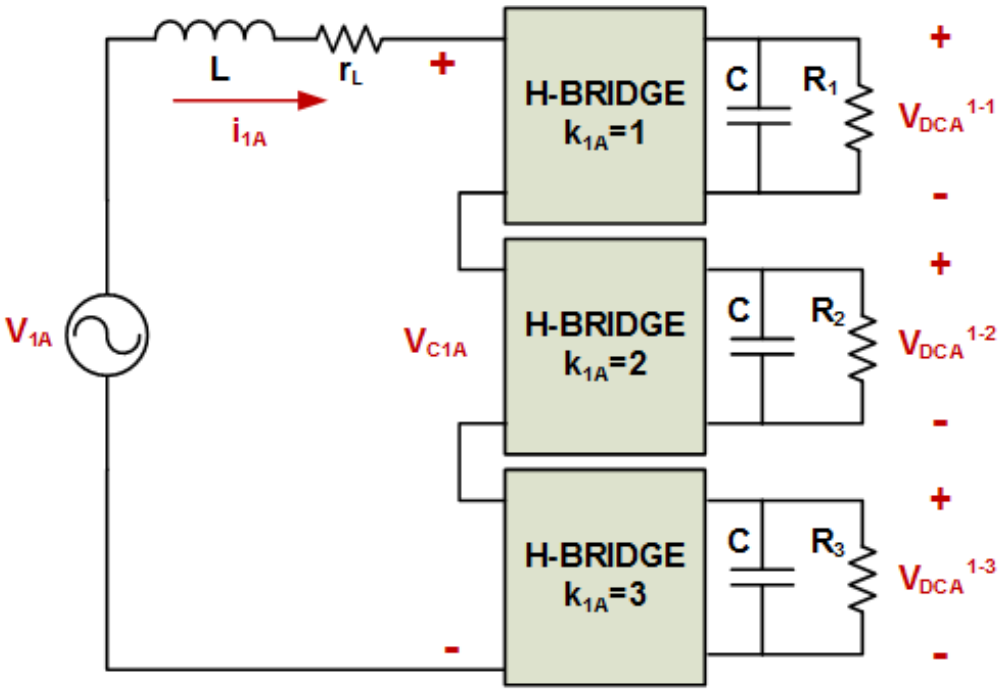


Figure 6.2 UNIFLEX-PM demonstrator phase A / port 1 circuit connected as an active rectifier, with resistive DC loads.

6.1.1 Distributed Commutation Modulation algorithm description

In normal operating conditions, the DCM technique allows only one commutation of a single HB leg during one sampling interval and impose sequential switching of the single HB cells, forcing each HB to commutate only one time every *n* sampling periods.

The commutations are permitted only between adjacent voltage levels and, in every sampling period, there is only one commutation of a single H-Bridge.

The flowchart of the proposed method, considering an *n*-cell converter is shown in Figure 6.3 with the symbols defined as follows:

- k_{1A} indicates the current HB enabled to commutate; its value represent the HB selected to switch, between the *1*st and n^{th} HB.
- $State_{1A}(k_{1A}) = -1, 0, +1$ is the state of single HB cell, using the notation of Figure 2.8, defined by k_{1A}.
- dv_{1A} is the error between normalized voltage reference v_{N1A}^*, in range *-n ...+n*.

$$dv_{1A} = v_{N1A}{}^* - v_{hb,1A} \tag{6.1}$$

v_{N1A}^* is defined from the converter voltage reference v_{c1A}^*, considering the DC-Link voltages are equal and regulated at the desired voltage reference V_{DC}^* by the control, and $v_{hb,1A}$ is the sum of the states on the other HBs that have not been selected to switch:

$$v_{N1A}{}^* = \frac{v_{C1A}{}^*}{V_{DC}{}^*} \tag{6.2}$$

$$v_{hb,1A} = \sum_{i=1, i\neq k_{1A}}^{n} state_{1A}\,(k_{1A}) \tag{6.3}$$

- $u_{old,1A}$ is the previous switching state of the HB defined by k_{1A}.
- $u_{new,1A}$ is the new switching state of the HB defined by k_{1A}.
- T_m is the numerical integer representation of the sampling period.
- $t_{x,1A}$ is the switching time instant inside the considered sampling period, in range $0…T_m$, of the of the HB defined by k_{1A}.

The modulation algorithm begins with an update of the current order of commutation of the *n* H-Bridges evaluated on the base of which H-Bridge has commutated in the previous sampling interval, with k_{1A} being the candidate H-Bridge for switching. Then the algorithm calculates the voltage error dv_{1A}, which represents the desired average voltage value that the k_{1A}-th HB would have to produce in a sampling period using the actual voltage level and the next applicable level.

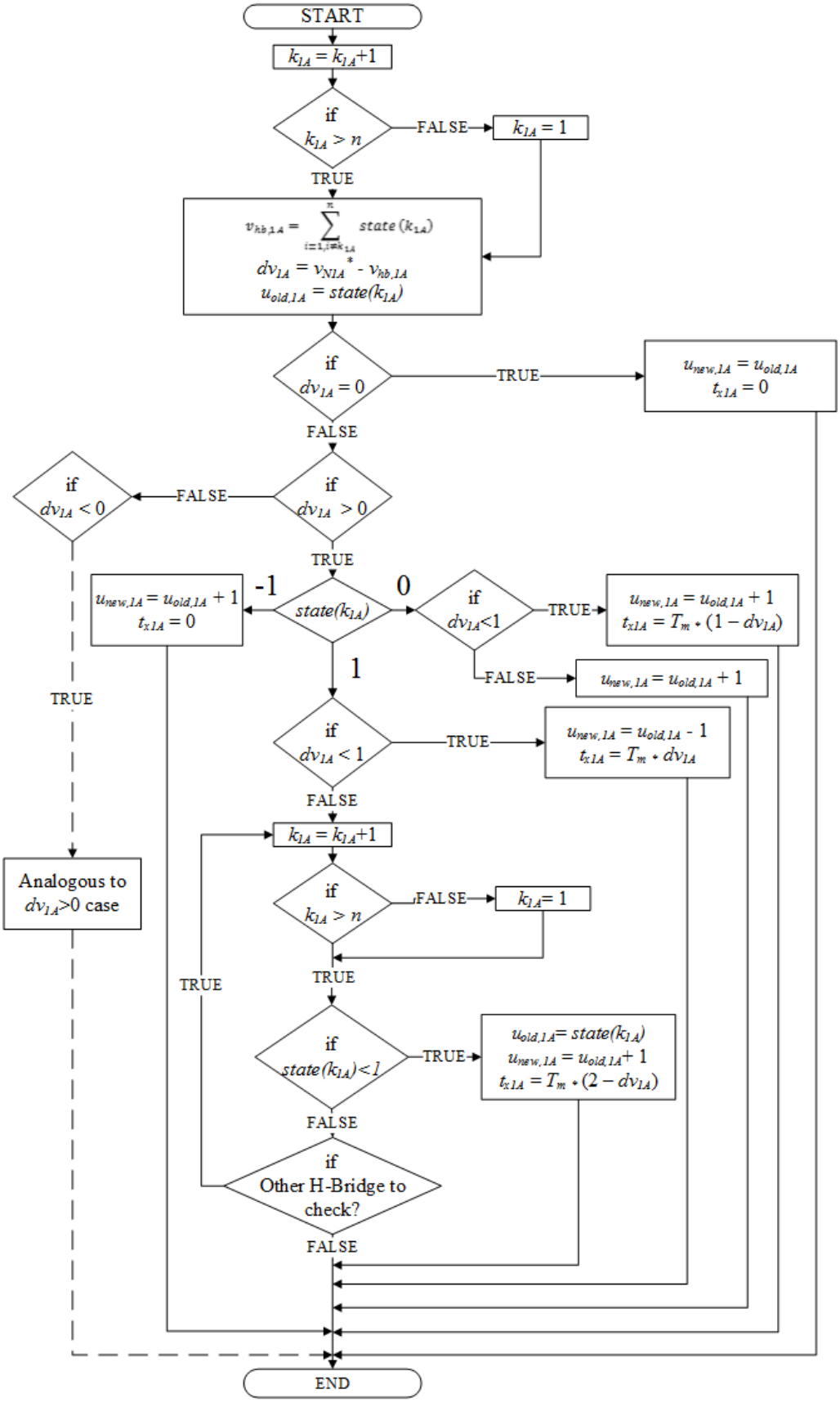


Figure 6.3 Operational flowchart of the proposed Distributed Commutations Modulation (DCM) technique.

In case of a positive error, the algorithm verifies if cell k_{1A} is able to commutate on the basis of its state. The following three cases for the state are possible:

- *state(k_{1A})=-1* : the selected HB cell cannot produce the required positive voltage with only one commutation, so the error can be reduced by switching to *state(k_{1A})= 0* immediately and applying the 0 level during the whole sampling period;
- *state(k_{1A})=0* : the selected HB cell can produce the required voltage with one commutation, so the switching instant is calculated as follows;

$$t_{x1A} = T_m(1 - dv_{1A}) \tag{6.4}$$

  if $dv_{1A}>1$ the error can be reduced switching to *state(k_{1A})=1* immediately and applying the 1 level is applied for the whole sample period;
- *state(k_{1A})=1* : the selected HB cell cannot produce a voltage larger than the current one applied. In this case the algorithm verifies whether $dv_{1A}<1$; if so, the voltage error can be reduced by continuing to apply the highest voltage level for an interval equal to the following value;

$$t_{x1A} = T_m dv_{1A} \tag{6.5}$$

  then switching to *state(k_{1A})=0*; otherwise the HB selected from k_{1A} is not commutated and the algorithm checks if another cell, amongst the remaining *n-1,* can commutate to a voltage level larger than its current one. If this is possible, the switching instant is calculated as follows.

$$t_{x1A} = T_m(2 - dv_{1A}) \tag{6.6}$$

An analogous procedure is performed in the case of a negative voltage error dv_{1A} and three cases are possible:

- *state(k_{1A})=1* : the selected HB cannot produce the required negative voltage with only one commutation; in this case the error can be reduced by switching to *state(k)= 0* immediately and applying the 0 level during the whole sampling period;
- *state(k_{1A})=0* : the selected HB can produce the required voltage with one commutation, so the switching instant is calculated as follows;

$$t_{x1A} = T_m(1 + dv_{1A}) \tag{6.7}$$

if dv_{1A}<1 the error can be reduced by switching to *state*(k_{1A})=*-1* immediately and applying the -1 level for the whole sample period;

- *state(k)=-1* : the selected HB cannot produce a voltage lower than the current one applied. In this case the algorithm verifies whether dv_{1A}>*-1*; if so, the voltage error can be reduced by continuing to apply the highest voltage level for an interval equal to the following value;

$$t_{x1A} = -T_m dv_{1A} \tag{6.8}$$

then switching to *state*(k_{1A})=*0*; otherwise the HB selected from k_{1A} is not commutated and the algorithm checks if another cell, among the remaining *n-1*, can commutate to a voltage level lower than its current one; if this is possible, the switching instant is calculated as follows.

$$t_{x1A} = -T_m(2 + dv_{1A}) \tag{6.9}$$

Diagrams showing the procedure corresponding to the previous mentioned situations are illustrated in Figure 6.4.

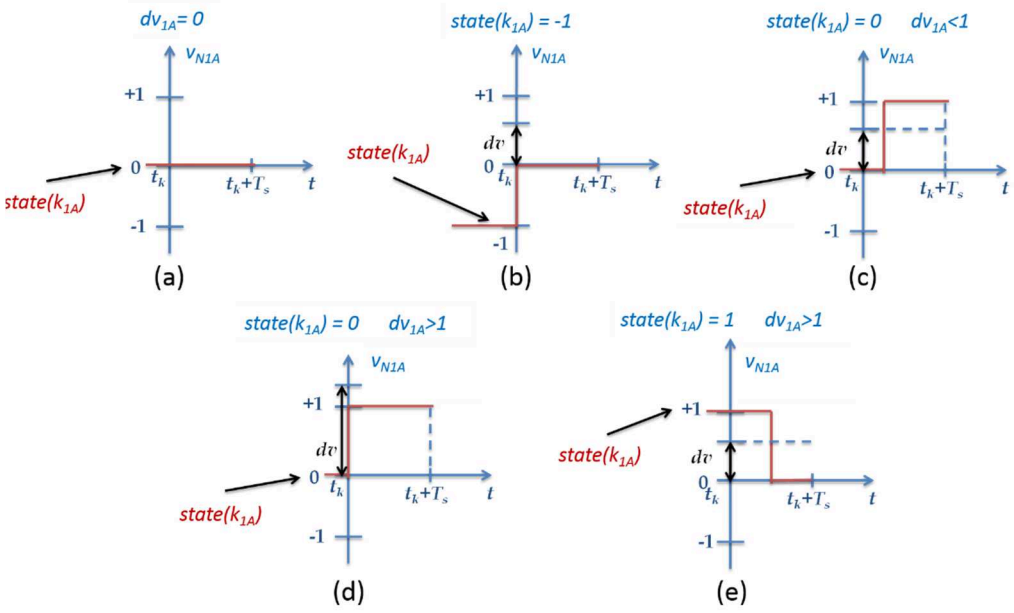


Figure 6.4 Behaviour of the proposed DCM technique at the sampling instant t_k during one sampling interval T_s for dv_{1A}>0: (a) dv_{1A}=0; (b) state(k_{1A})=-1; (c) state(k_{1A})=0 and dv_{1A}<1;(d) state(k_{1A})=0 and dv_{1A}>1; (e) state(k_{1A})=1 and dv_{1A}<1.

A first example of operation is given in Figure 6.5, where a multilevel waveform is generated using the DCM technique by commutating sequentially the three HBs of a 7-Level CHB converter.

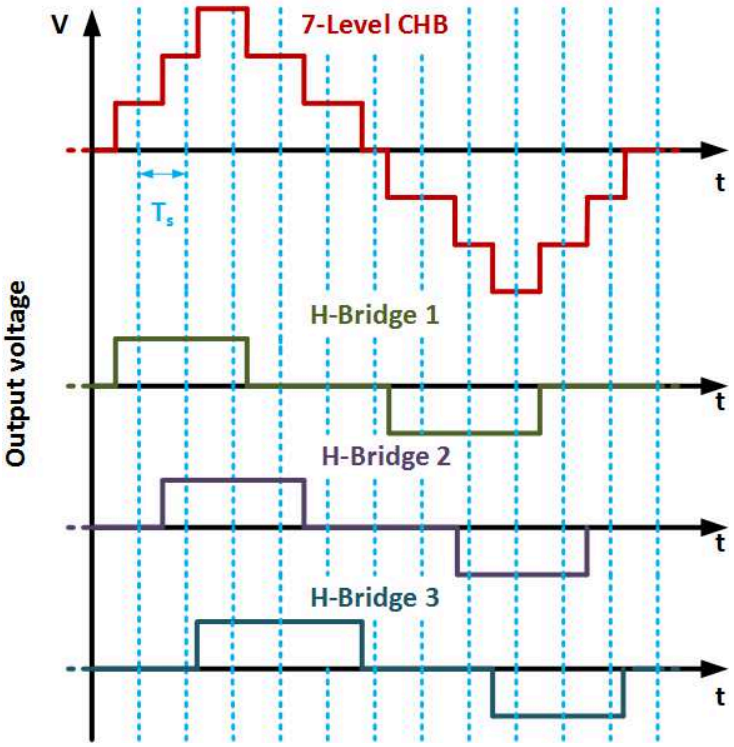


Figure 6.5 DCM technique working principle: multilevel waveform generation.

A second example of operation is given in Figure 6.6 where the converter is controlled in order to obtain a positive square waveform. As it is possible to see from the first waveform in Figure 6.5 and Figure 6.6, the sampling frequency is:

$$f_s = \frac{1}{T_s} \tag{6.10}$$

The signal produced by the converter has a switching frequency f_{sw} equal to f_s. The single H-Bridges are forced to commutate sequentially, resulting in a switching frequency for each H-Bridge of:

$$f_{sw,HB} = \frac{f_{sw}}{3} \tag{6.11}$$

By taking advantage of the zero state redundancy, it is possible to obtain, for a single device of the H-Bridge, a switching frequency equal to the following value.

$$f_{sw,Q} = \frac{f_{sw,HB}}{2} \tag{6.12}$$

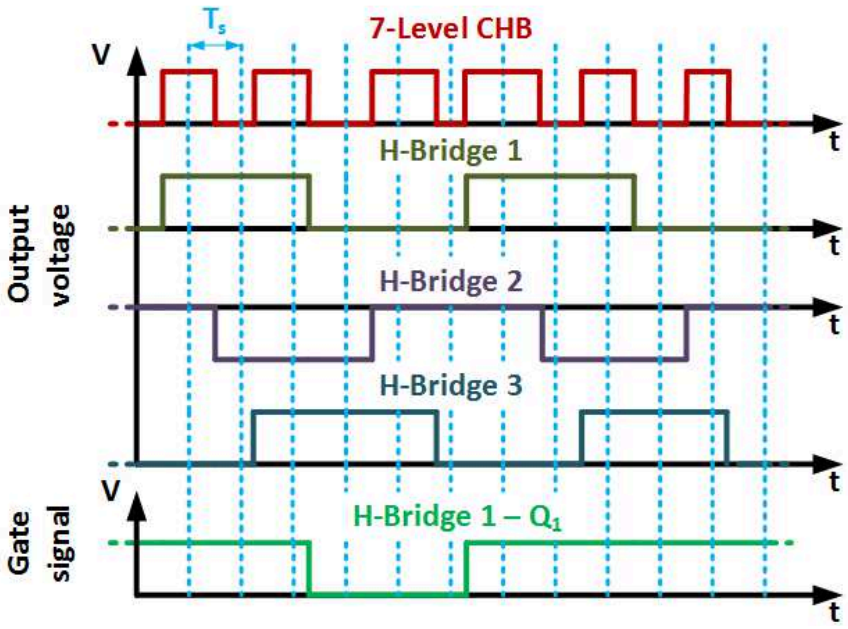


Figure 6.6 DCM technique working principle: square waveform generation.

Clearly, this operating condition is not always feasible when a multi-level waveform is produced. For example, in the case of a 7-level CHB, when DCM is applied for a normalised voltage between 2 and 3 (or -2 and -3), usually the selected HB needs to commutate for two consecutive sampling intervals, as shown in Figure 6.7.

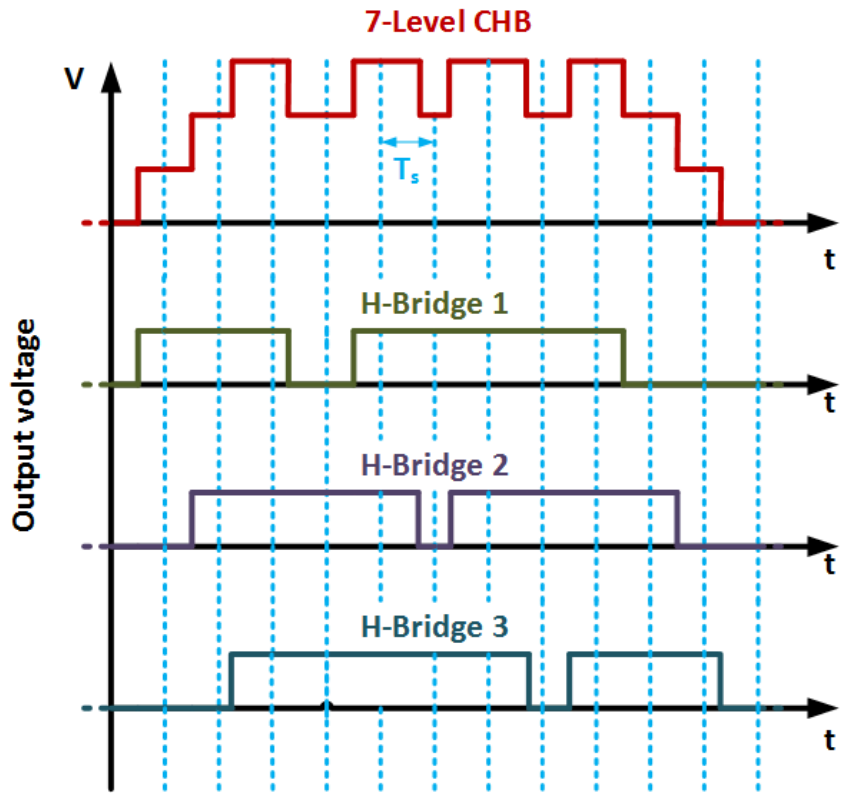


Figure 6.7 DCM technique working principle: not sequential operation.

Two main issues have been identified using this technique:

- The DC-Link voltage balance is achieved only when applying the same load on the three H-Bridges; in any other case an additional control is required.
- In case of high power, low voltage applications such as automotive applications, when the converter can have much more than 7 voltage levels, the device voltage drops and on-state resistance affect negatively the behaviour of the modulator, in term of produced converter voltage and current THD.

An additional algorithm, described below, has been implemented to overcome these issues.

6.1.2 Active DC-Link Voltage balancing and device parasitic component compensation for DCM

The main goal of the proposed improved DCM algorithm is to minimise the DC-Link voltages unbalance, for any amplitude of the voltage reference, amongst the different converter cells in order to obtain high-quality waveforms with a low switching frequency and maintain the converter modularity [172]. In order to achieve such a goal, a fast control response to counteract any unbalance on the DC loads is required. For this reason the "balancing algorithm" is fully integrated into the modulation scheme, without using any additional controllers. It is important to specify that, since one of the targets of the proposed improved algorithm is to equalize the voltages on the capacitors, their average value is considered as the reference voltage on each DC-link capacitors. At the same time the total DC-Link voltage is regulated at its reference value using a Proportional Integral action external to the modulator. In addition, the device voltage drops and on-state resistance are compensated. This feature is particularly important when a converter with a high number of levels and relatively low DC-Link voltages is considered as for example automotive applications. In fact in these applications the device voltage drops and on state resistance degrade the converter voltage harmonic content, resulting in a higher converter voltage THD. As already described for the standard DCM, the commutations are permitted only between adjacent voltage levels i.e. it is possible to switch only one leg of one H-Bridge cell during every sampling interval. The algorithm is modular and applicable to a generic *n*-level CHB converter; however increasing the number of voltage levels the required computational effort increase.

6.1.2.1 Device voltage drop and on-state resistance effect compensation

The device voltage drop and on-state resistance effect is compensated considering, instead of the measured DC-Link voltages, the effective voltages generated by the converter [173]. Referring to Figure 6.8, for one H-Bridge cell three parasitic voltages, dependent on the current direction and amplitude, are defined as follows.

$$V_0 = sign(i_{1A}) * (V_d + V_q) - i_{1A} * (R_d + R_q) \tag{6.13}$$

$$V_+ = -2 * (V_q + |i_{1A}|R_q) \tag{6.14}$$

$$V_- = 2 * (V_d + |i_{1A}|R_d) \tag{6.15}$$

Where V_d, V_q are respectively the diode and transistor voltage drops while, R_d, R_q are the diode and transistor on-state resistances. These parameters can be found in the device datasheets and depend on the current flowing in the device and the operating temperature. Finally i_{1A} is the current flowing on the AC side of the considered H-Bridge cell. Considering the state of each H-Bridge and the sign of the current i_{1A} flowing through the selected cell, it is possible to calculate the effective voltages generated by the converter as follows:

- If a zero voltage state is applied, considering voltage drops and on-state resistance of the devices, a voltage is produced at the output of the cell, defined by:

$$V_{DCA,eff}{}^{1-j} = V_0 \ , \ j = 1,2,3 \tag{6.16}$$

- If positive power is transferred (applied voltage and AC current have the same sign) the transistors are conducting and the generated voltage is:

$$V_{DCA,eff}{}^{1-j} = V_{DCA}{}^{1-j} + V_+ \ , \ j = 1,2,3 \tag{6.17}$$

- If negative power is transferred (applied voltage and AC current have different signs) the diodes are conducting and the generated voltage is

$$V_{DCA,eff}{}^{1-j} = V_{DCA}{}^{1-j} + V_- \ , \ j = 1,2,3 \tag{6.18}$$

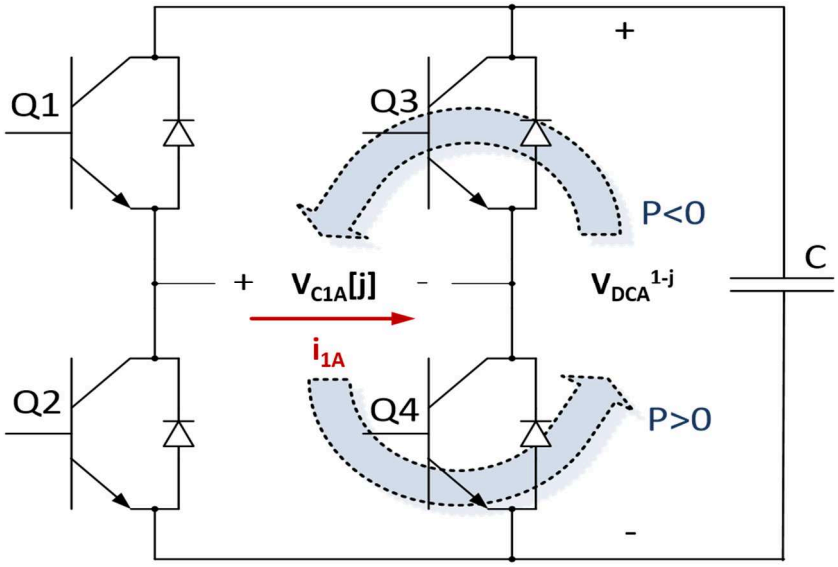


Figure 6.8 Power flow in each H Bridge.

6.1.2.2 DC Link Voltage balancing algorithm

The algorithm is based on the application of iterative conditions in order to achieve the desired balance of the DC-Link voltages without losing the modularity of the algorithm. The modulation algorithm begins with an update of the current order of commutation of the three H-Bridges. Considering the measurements of the DC-Link voltages $V_{DCA}{}^{1\text{-}1}$, $V_{DCA}{}^{1\text{-}2}$, $V_{DCA}{}^{1\text{-}3}$, the average DC-Link voltage is calculated as in (4.19) and considered as reference value.

$$V_{DCA}{}^{1-AVG} = \frac{1}{3}\sum_{j=1\dots n}^{3} V_{DCA}{}^{1-j} = \frac{V_{DCA}{}^{1-TOT}}{3} \tag{6.19}$$

Then the DC-Link voltage error is calculated for every H-Bridge as shown in (4.20).

$$V_{DCA,err}{}^{1-j} = V_{DCA}{}^{1-AVG} - V_{DCA,eff}{}^{1-j} \tag{6.20}$$

The absolute values of $V_{DCA,err}{}^{1\text{-}j}$ are then ranked from the highest value to the lowest one and, on this basis, the H-Bridge switching order is defined. H-Bridge k_{1A} is then selected to switch during the current interval and it is possible to calculate the normalised voltage, dv_{1A}, which has to be applied from the H-Bridge k_{1A} as follows.

$$dv_{1A} = \frac{v_{C1A}{}^{*} - \sum_{j\neq k_{1A}} state(j) * V_{DCA,eff}{}^{1-j}}{V_{DCA,eff}{}^{1-k_{1A}}} \quad , \quad state(k_{1A}) \neq 0 \tag{6.21}$$

$$dv_{1A} = \frac{v_{C1A}{}^{*} + V_0 - \sum_{j\neq k_{1A}} state(j) * V_{DCA,eff}{}^{1-j}}{V_{DCA,eff}{}^{1-k_{1A}}} \quad , \quad state(k_{1A}) = 0 \tag{6.22}$$

Where v_{C1A}^* is the desired voltage reference and *state(k_{1A})* is the current state of the H-Bridge selected to switch. The voltage error dv_{1A} represents the desired value that H-Bridge k_{1A} has to produce in a sampling period using the current voltage level and the next applicable level. In steady state operation usually $|dv_{1A}|<1$; however it is possible, especially during fast transients of the voltage reference, that the absolute value of dv_{1A} becomes larger than 1. In the case of a positive error, the algorithm verifies if cell k_{1A} is able to commutate on the basis of its state and if the required commutation increases or not of the DC-Link voltages unbalance. The following three cases for the state of H-Bridge k_{1A} are possible:

- *state(k_{1A})=-1* The current cell cannot produce the required positive voltage with only one commutation so the error can be reduced by applying the 0 level during the whole sampling period; this commutation is allowed only if ${V_{DCA}}^{1-k_{1A}}$ and the AC current i_{1A} have the same sign;
- *state(k_{1A})=0* The current cell can produce the required voltage with one commutation, so the switching instant is calculated as follows

$$t_{x1A} = T_m \left[1 - \left(dv_{1A} - \frac{V_+}{{V_{DCA}}^{1-k_{1A}}}\right)\right] \quad , \quad i_{1A} \leq 0 \tag{6.23}$$

$$t_{x1A} = T_m \left[1 - \left(dv_{1A} - \frac{V_-}{{V_{DCA}}^{1-k_{1A}}}\right)\right] \quad , \quad i_{1A} \geq 0 \tag{6.24}$$

  If $dv_{1A}>1$, it is clear from eq. (4.49) and (4.50) that $t_x<0$. In this case $t_x=0$ is imposed. This commutation is allowed only if ${V_{DCA,err}}^{1-k_{1A}}$ and the AC current i_{1A} have the same sign;
- *state(k_{1A})=1* The current cell cannot produce a voltage greater than the current one. In this case the algorithm verifies if $dv_{1A}<1$ so the voltage error can be reduced by remaining with the highest voltage level for an interval equal to

$$t_{x1A} = T_m \left(dv_{1A} - \frac{V_0}{{V_{DCA}}^{1-k_{1A}}}\right) \tag{6.25}$$

  This commutation is allowed only if ${V_{DCA,err}}^{1-k_{1A}}$ and the AC current i_{1A} have different signs.
- *otherwise* the algorithm checks if another cell can commutate to a voltage level greater than its current one without increasing the unbalance on the DC-Link voltages.

In Figure 6.9 a switching pattern example for a positive error is described. As described in equations (6.13)-(6.18), the effective voltage applied by the converter is related to the current sign. Depending on the previously applied state, it is possible to determine 3 cases for the new commutation where the sign of the current determines the switching time as described in equations (6.23)-(6.25). Clearly this commutation is allowed only if it does not increase the DC-Link voltage error.

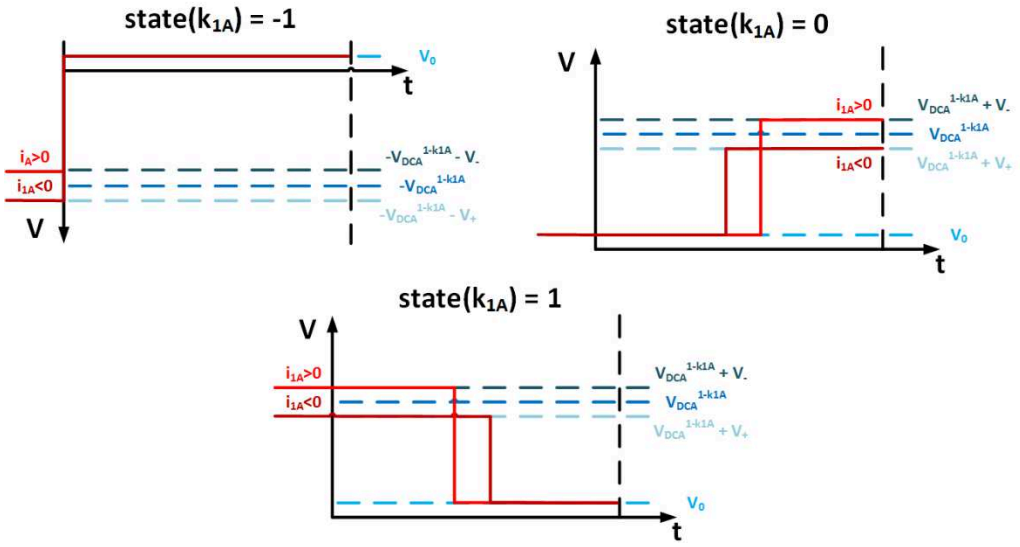


Figure 6.9 Possible switching patterns for 0<dv<1.

In the case of a negative error, the algorithm verifies if cell k_{1A} is able to commutate on the basis of its state and if the required commutation increases or not the DC-Link voltages unbalance. The following three cases for the cell k_{1A} state are possible:

- *state*(k_{1A})=*1* The current cell cannot produce the required negative voltage with only one commutation so the error can be reduced applying the 0 level during the whole sampling period; this commutation is allowed only if ${V_{DCA,err}}^{1-k_{1A}}$ and the AC current i_{1A} have different signs;
- *state*(k_{1A})=*0* The current cell can produce the required voltage with one commutation, so the switching instant is calculated as

$$t_{x1A} = T_m \left[1 + \left(dv_{1A} - \frac{V_+}{{V_{DCA}}^{1-k_{1A}}}\right)\right] \quad , \quad i_{1A} \leq 0 \tag{6.26}$$

$$t_{x1A} = T_m \left[1 - \left(dv_{1A} - \frac{V_-}{{V_{DCA}}^{1-k_{1A}}}\right)\right] \quad , \quad i_{1A} \geq 0 \tag{6.27}$$

If dv_{1A}<*-1*, it is clear from (6.26) and (6.27) that t_{x1A}<0. In this case t_x=0 is imposed. This commutation is allowed only if ${V_{DCA,err}}^{1-k_{1A}}$ and the AC current i_{1A} have different signs;

- *state*(k_{1A})=*-1* The current cell cannot produce a voltage greater than actual one. In this case the algorithm verifies if dv_{1A} >*-1* so the voltage error can be reduced by remaining with the highest voltage level for an interval equal to

$$t_{x1A} = -T_m\left(dv_{1A} - \frac{V_0}{{V_{DCA}}^{1-k_{1A}}}\right) \tag{6.28}$$

This commutation is allowed only if ${V_{DCA,err}}^{1-k_{1A}}$ and the AC current i_{1A} have the same sign;

- *otherwise* the algorithm checks if another cell can commutate to a voltage level lower than its current one without increasing the unbalance on the DC-Link voltages.

6.2 Simulation results for the proposed modulation techniques

Simulations has been carried out in Matlab\Simulink in order to prove the effectiveness of the proposed modulation methods. A single 7-level CHB is considered in the simulations.

6.2.1 Distributed Commutation Modulation

The performance of DCM algorithm has been tested in simulation and compared to Phase Shifted Carrier Modulation (PSCM) and Average Voltage Modulation (AVM), considering a 3-cell CHB able to produce a 7-level output voltage waveform. In Figure 6.10 simulation results are shown considering only the open-loop modulation algorithms in ideal operating conditions, i.e. considering a sinusoidal reference for the modulators with a modulation index $m=0.83$. The value of m is chosen to produce a 7 level waveform and allow the AVM modulator to switch all three H-Bridges. Under these conditions a comparison between the three modulation techniques is possible with the H-Bridges operating under the same conditions. For this comparison a 300Hz carrier frequency is considered, resulting in a total CHB sampling frequency of 1800Hz.

Figure 6.10a shows the modulated voltage waveform and the sinusoidal reference for PSCM while Figure 6.10c and Figure 6.10e illustrate the obtained modulated voltage waveform, for AVM and DCM respectively. The main differences between AVM and the other techniques is evident when comparing Figure 6.10b, Figure 6.10d and Figure 6.10f, where the voltage on a single H-Bridge is considered. It is clear that AVM does not distribute the commutations along the modulating signal period; thus, when the reference signal is small, only one H-Bridge commutates whilst the others are not used. In this example, both PSCM and DCM techniques equally distributes 24 commutations per H-Bridge per period, while the AVM produces 20, 24, 28 commutations per period amongst the three cells respectively.

Figure 6.10g shows the comparison between the harmonic content of the different modulation strategies in the case of modulation index equal to 0.83. AVM presents two large magnitude harmonics (35th and 37th) around the commutation frequency while in PSCM and DCM the switching frequency harmonics are spread; however, the harmonics magnitudes of the proposed modulation are much lower than the PSCM ones.

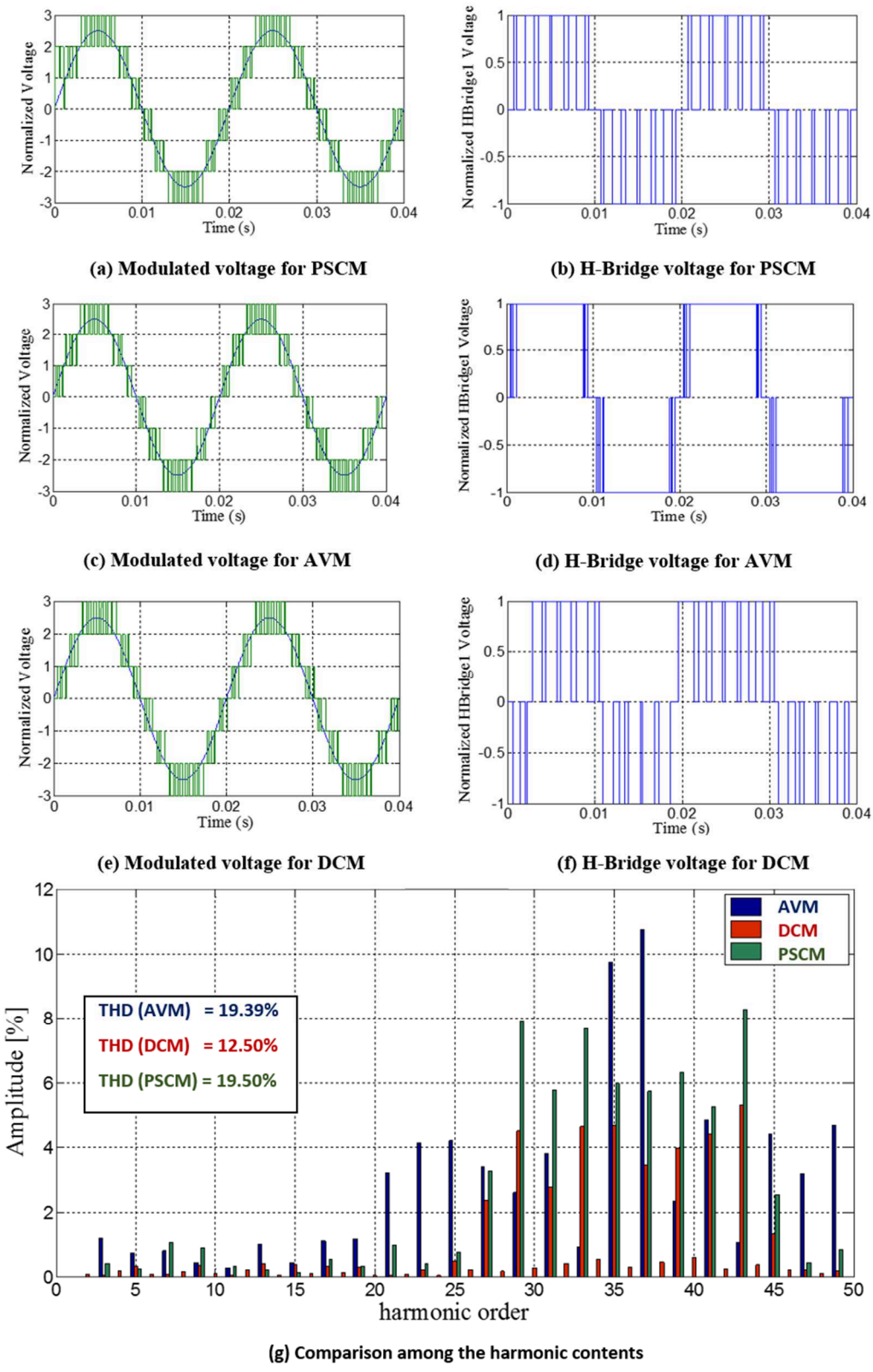


Figure 6.10 Comparison among the voltage waveforms produced by the three considered modulation techniques.

Moreover, up to the 25th harmonic, PSCM and DCM present negligible harmonic content. Another difference is that DCM presents some even harmonics in its spectrum (as a result of the decision making process creating a slight asymmetry in the waveform), but the amplitude of these components is insignificant. The Total Harmonic Distortion (THD), defined in (6.29), is equal to 19.50% for PSCM, 19.39% for AVM and 12.50% for DCM.

$$THD\ [\%] = \frac{100\sqrt{\sum_{n=2}^{k} V_n{}^2}}{V_1} \tag{6.29}$$

Figure 6.11 shows, for every H-Bridge, that the switching frequency for PSCM and for DCM is evenly shared among the different H-bridges for every value of the modulation index.

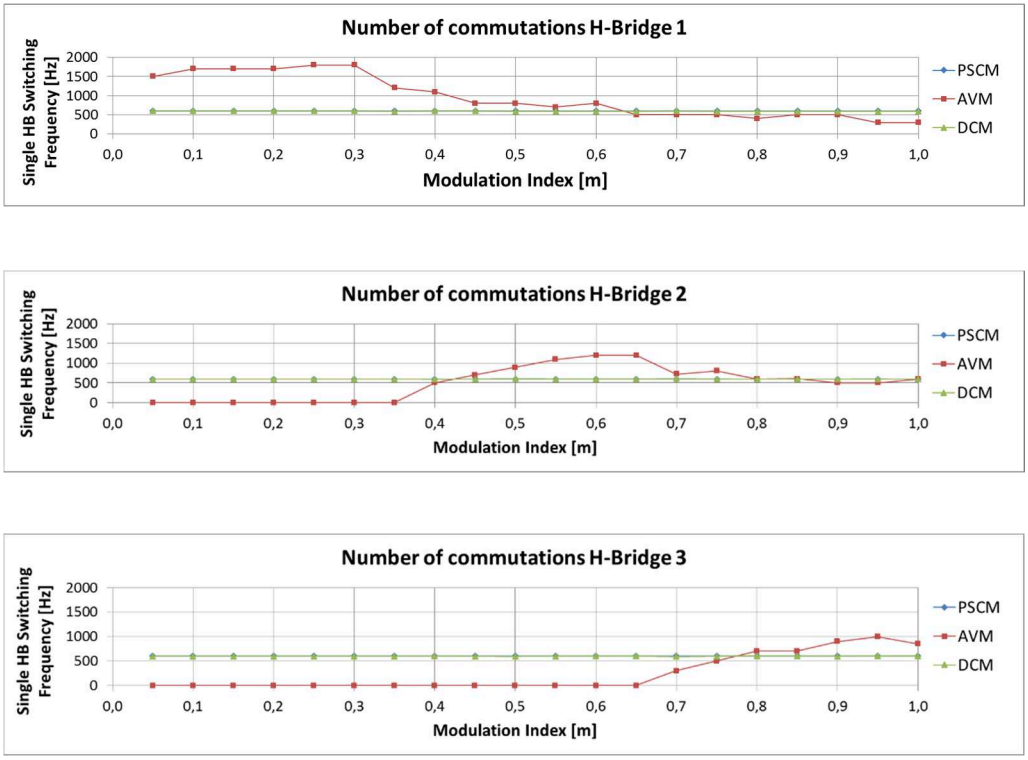
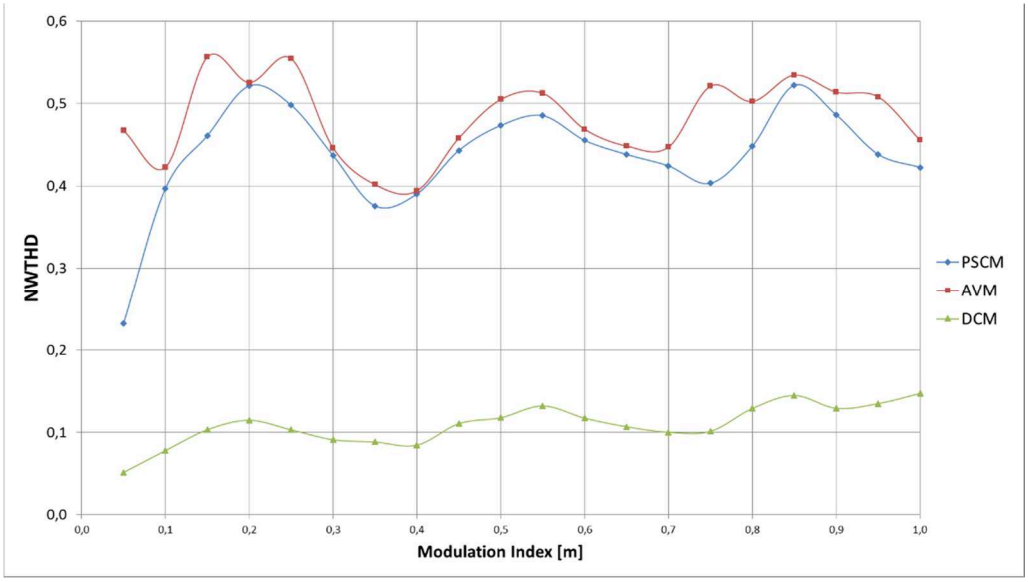


Figure 6.11 Comparison of the switching frequency on H-Bridges versus modulation index.

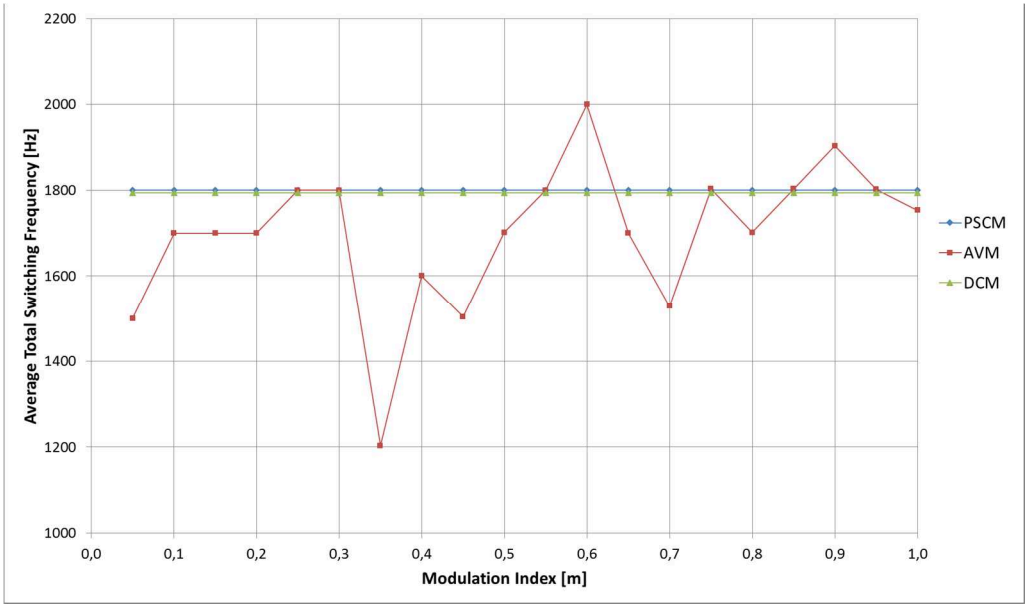
The reduced harmonic content produced by the proposed modulation is highlighted by the Normalized Weighted Total Harmonic Distortion (NWTHD) plotted in Figure 6.12a against the modulation index for each modulation technique, where NWTHD is defined as in (6.30).

$$NWTHD\ [\%] = \frac{100\sqrt{\sum_{n=2}^{k} \left(\frac{V_n}{n}\right)^2}}{V_1} \tag{4.30}$$

This comparison shows the improved performance of DCM across the whole range of *m*. Since the proposed modulation procedure, as highlighted in the previous section, does not produce any commutations in some sampling period, the system switching frequency is lower than the control sampling frequency; so, as can be noted from Figure 6.12b, the switching frequency for the DCM is always less or equal to the one produced by PSCM and only in a limited interval greater than AVM one.



(a) NWTHD



(b) Switching frequency

Figure 6.12 NWTHD and switching frequency versus modulation index for the three considered modulation techniques.

6.2.2 Distributed Commutation Modulation including DC-Link voltage balancing algorithm and device parasitic components compensation

In order to test the proposed algorithm DC-Link voltage balancing algorithm, an AC current control needs to be implemented. In this case the dead-beat controller, described in Chapter 7, is used. A 7-level CHB converter is simulated using Simulink SimPower Systems toolbox and considering variable resistive loads on the DC side of each H-Bridge as shown in Figure 6.2.

In this case the main issue is maintaining balanced voltages on the DC side of each H-Bridge, i.e. $V_{DCA}^{1-1}=V_{DCA}^{1-2}=V_{DCA}^{1-3}$, resulting a viable option to test the capability of a DC-Link voltages balancing algorithm. The simulation parameters are shown in Table 6.1.

Table 6.1 Simulation parameters for DCM.

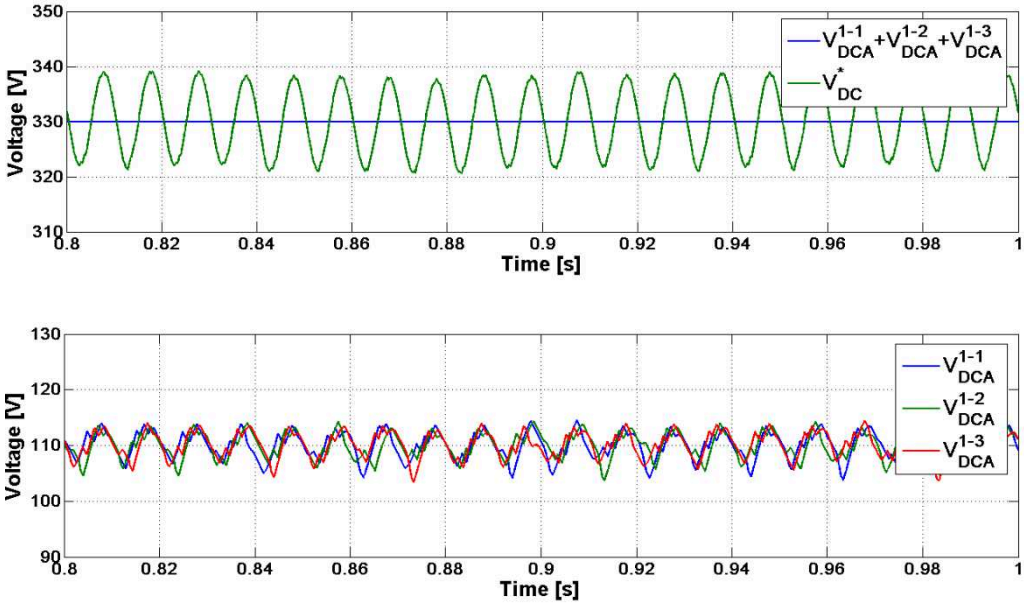
Name	**Description**	**Value**	**Unit**
V_d	Diode voltage drop	3	[V]
V_q	Transistor voltage drop	5	[V]
R_d	Diode on-state resistance	0.5	[mΩ]
R_q	Transistor on-state resistance	1	[mΩ]
r_L	Leakage resistance	1	[Ω]
L	Inductance	11	[mH]
C	Capacitance	3300	[μF]
f_s	Sampling frequency	2500	[Hz]

Large values of diode and transistor voltage drops are used in simulations to highlight the performance of the voltage drop compensation for this reduced scale converter. In this section the proposed modulation technique has been compared and contrasted with the DCM modulation.

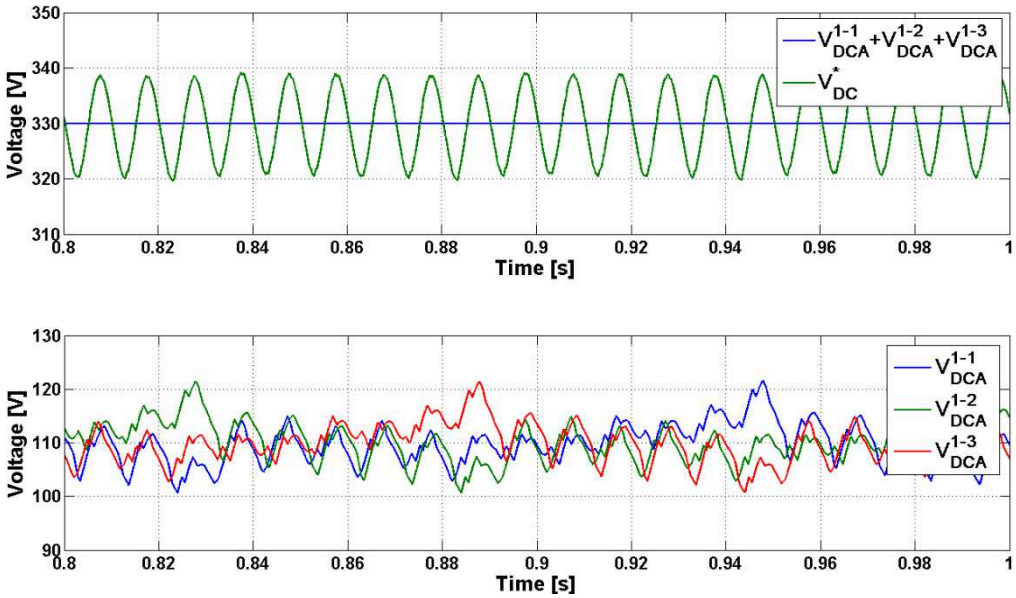
6.2.2.1 Balanced DC loads

A first comparison between the DCM technique with and without DC-Link voltage balancing and device parasitic components compensation is performed considering three balanced DC loads of 20Ω. In this case, it is possible to see the performance improvement due to the proposed introduction of the device voltage drop and on-state resistance compensation.

Figure 6.13 shows that the total DC-Link voltage tracks the desired reference and the single DC-Link voltages are well balanced. Using the proposed modulation technique the produced DC-Link voltage ripple is around the 9% of the nominal DC-Link voltage, resulting lower of the ripple produced by the classic DCM modulator (18% of nominal DC-Link voltage).



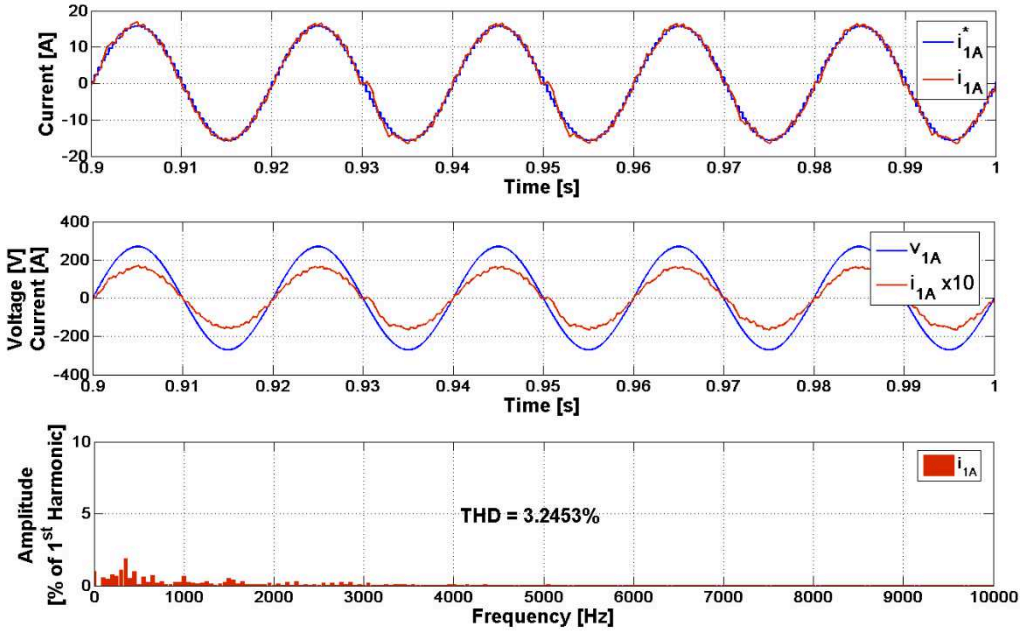
(a) DCM with DC Link voltage balancing algorithm and device voltage drops, ON resistance compensation



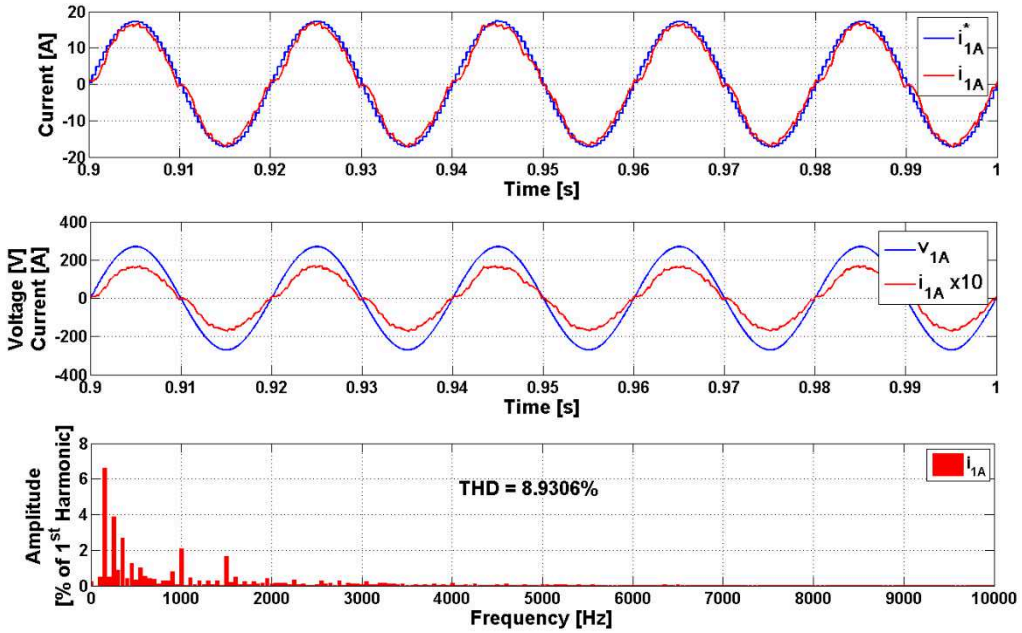
(b) DCM

Figure 6.13 Total and single DC-Link voltage for balanced DC loads.

Figure 6.14 shows the converter AC current with a total switching frequency of 1.25kHz, compared with the current reference and with the AC supply voltage. The current follows the reference with insignificant error and the supply current and voltage are in phase as required. Moreover, the current harmonic content is characterised by a low THD value using the proposed modulator, due to the device parasitic components compensation.



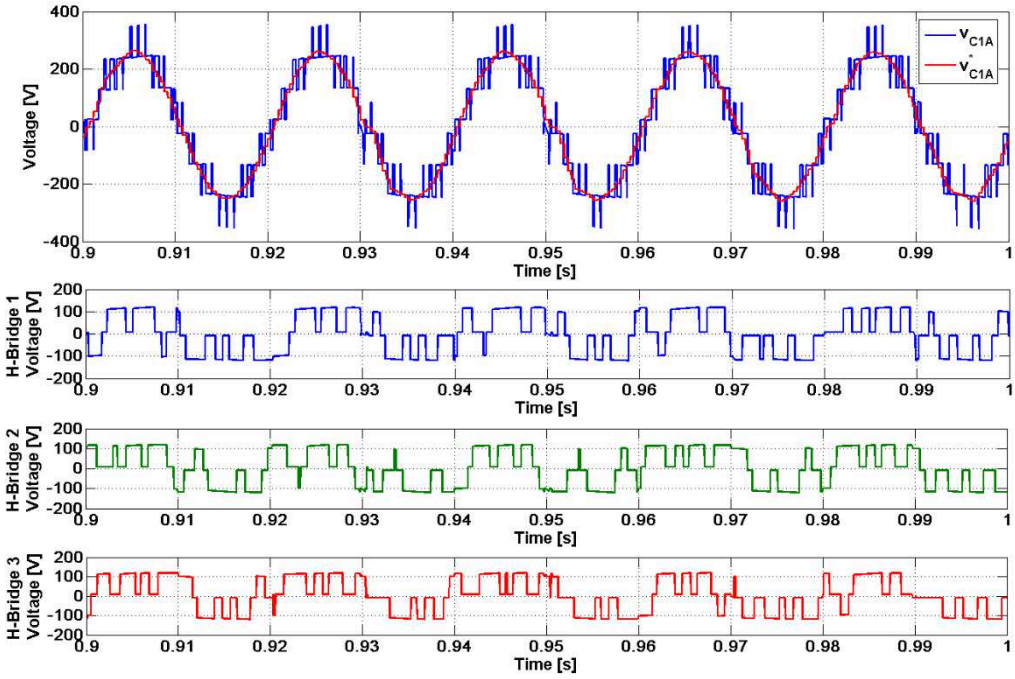
(a) DCM with DC Link voltage balancing algorithm and device voltage drops, ON resistance compensation



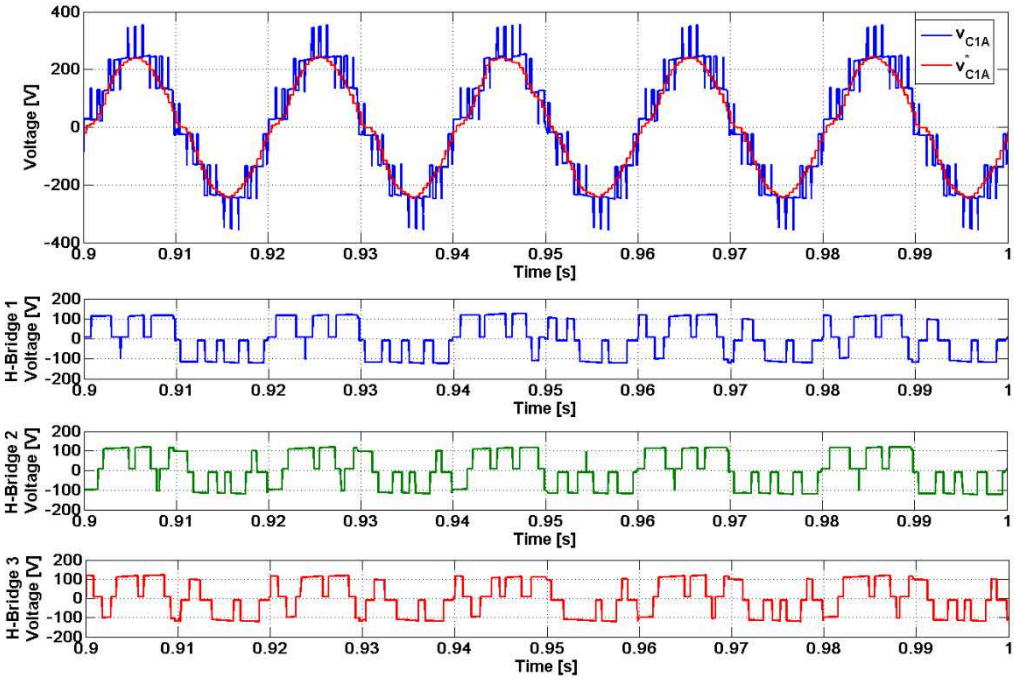
(b) DCM

Figure 6.14 AC Current, Current reference, AC Voltage and Current Harmonic content for balanced DC loads.

Figure 6.15 shows the converter voltage compared with the modulation voltage reference and the single H-Bridge output voltages. It is possible to observe that a good distribution of commutations amongst the three H-Bridges is obtained in both cases.



(a) DCM with DC Link voltage balancing algorithm and device voltage drops, ON resistance compensation

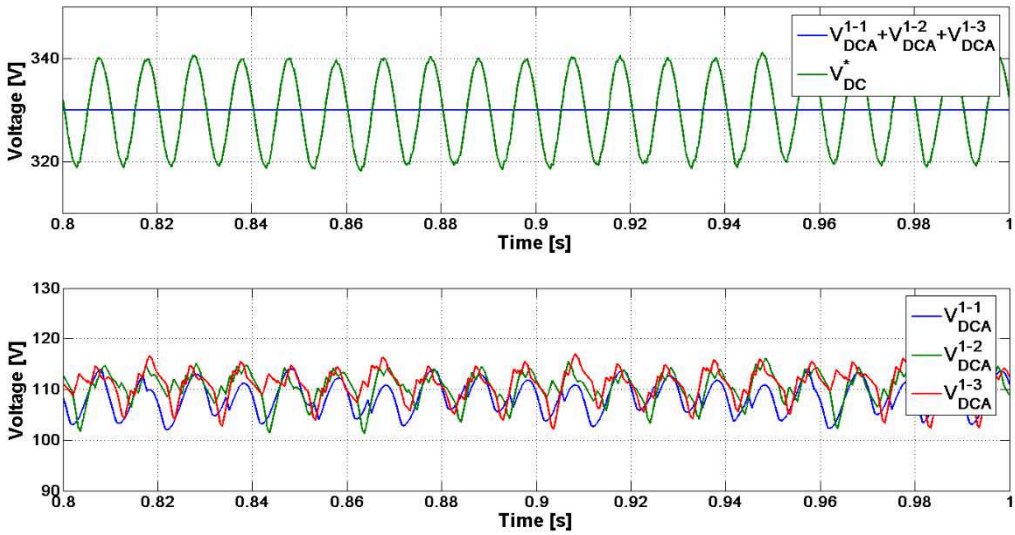


(b) DCM

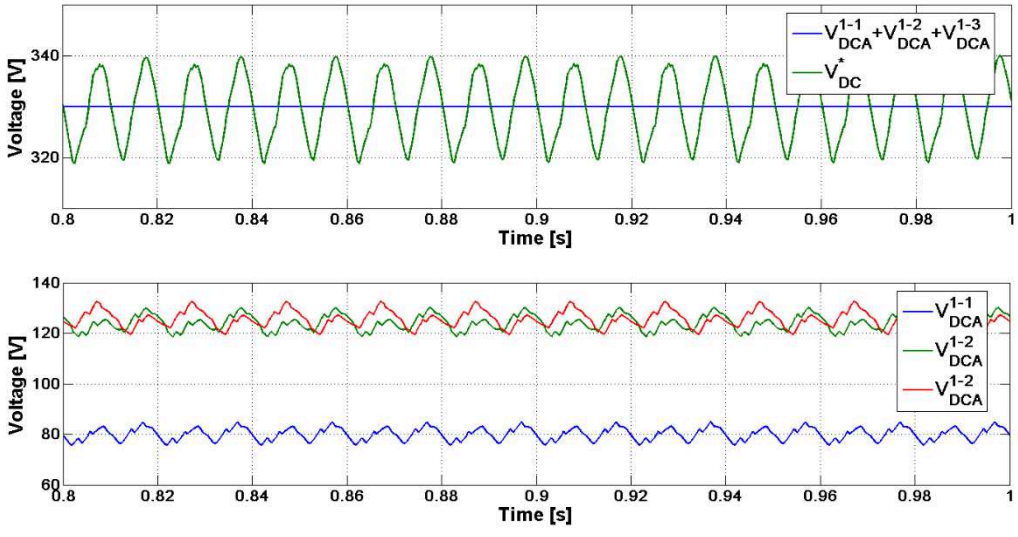
Figure 6.15 Converter voltage and reference, single H-Bridge produced voltage for balanced DC loads.

6.3.2.2 Unbalanced DC loads

A comparison between the DCM technique with and without DC-Link voltage balancing and device parasitic components compensation is performed considering three unbalanced DC loads of respectively 10Ω-20Ω-30Ω is presented. Such operation can be observed in solid state transformers [93], as well as in inverter with battery feeds [174] and the performance of the DC-Link voltage balancing algorithm can be clearly observed. Figure 6.16 shows that the total DC-Link voltage follows the desired reference and the single DC-Link voltages are well balanced using the proposed modulation technique while the simple DCM modulator produces an unbalance of the DC-Link voltages.



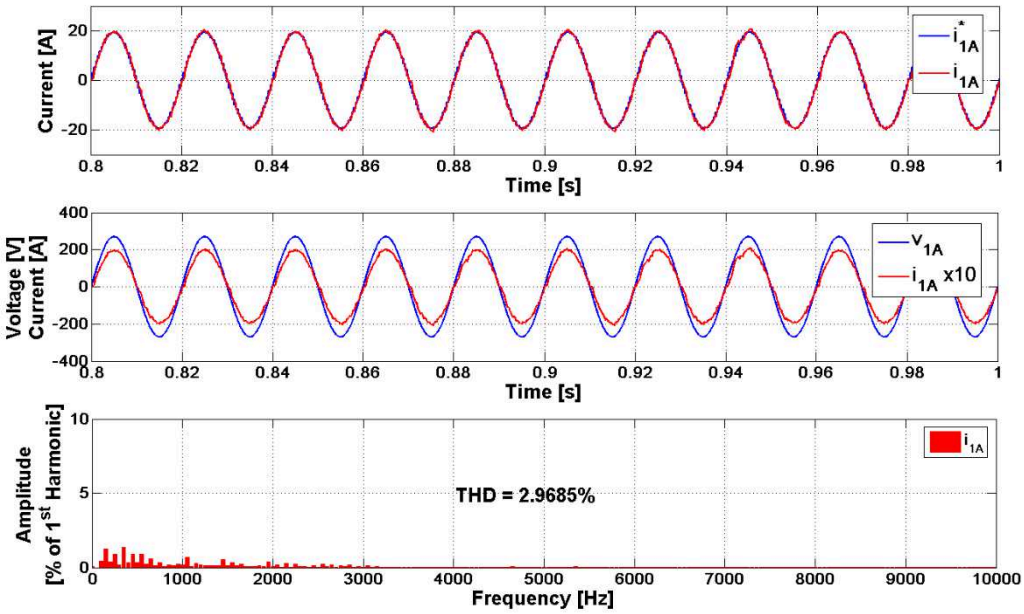
(a) DCM with DC Link voltage balancing algorithm and device voltage drops, ON resistance compensation



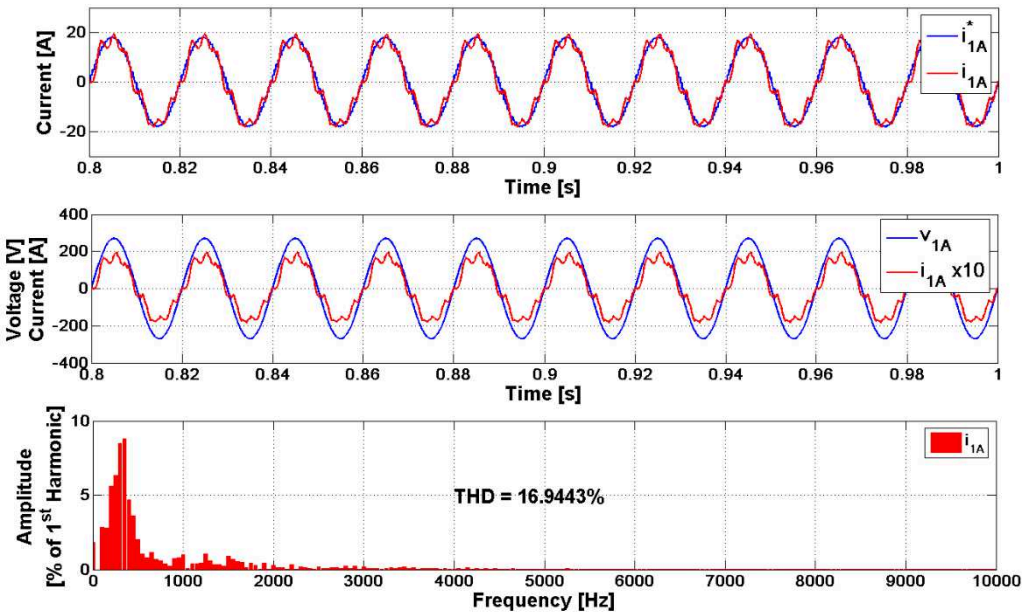
(b) DCM

Figure 6.16 Total and single DC-Link voltages for unbalanced DC loads.

Figure 6.17 shows the converter AC current for a total switching frequency of 1.25kHz, compared with the current reference and with the supply AC voltage. The proposed modulation technique ensure that the current tracks the reference with a small error while the current and supply voltage are in phase as required; moreover, the current harmonic content is characterised by a low THD value. Conversely, the simple DCM modulator generates high distortion of the AC current due to the unbalance of the DC-Link voltages.



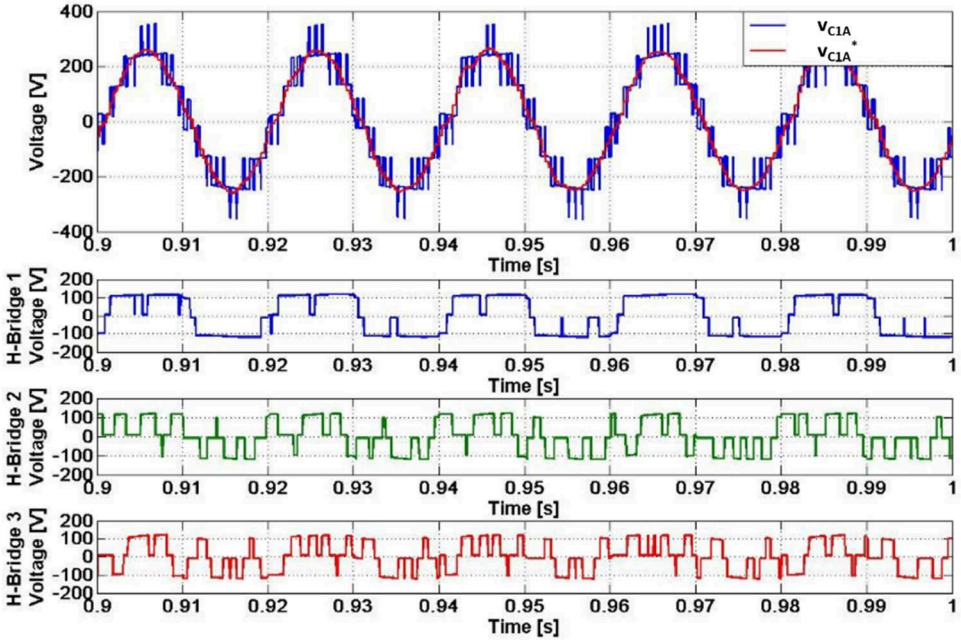
(a) DCM with DC Link voltage balancing algorithm and device voltage drops, ON resistance compensation



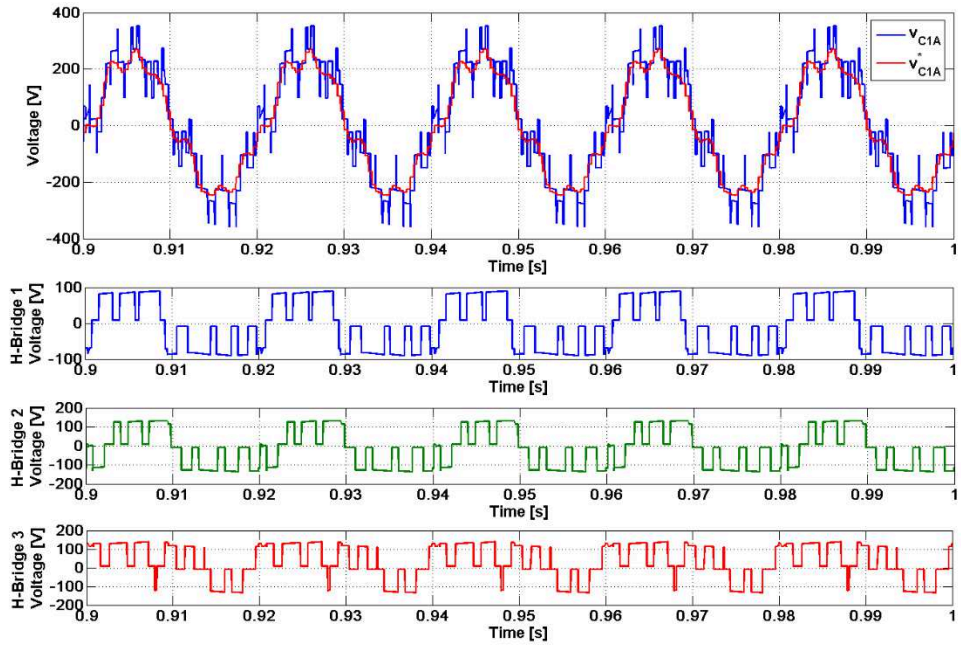
(b) DCM

Figure 6.17 AC Current, Current reference, AC Voltage and Current Harmonic content for unbalanced DC loads.

Figure 6.18 shows the converter voltage compared with the modulation voltage reference and the individual H-Bridge voltages. In order to obtain three balanced DC-Link voltages, the even distribution of commutations amongst the three H-Bridges is lost using the proposed modulator. The DCM modulator produces an even distribution of commutations amongst the three H-Bridges, but the high distortion of the AC current generates a distorted voltage reference which affects the Dead-Beat control.



(a) DCM with DC Link voltage balancing algorithm and device voltage drops, ON resistance compensation



(b) DCM

Figure 6.18 Converter voltage and reference and single H-Bridge produced voltages for unbalanced DC loads.

6.3 Experimental results for the proposed modulation techniques

In order to deeply investigate the performance of the proposed modulation technique, experimental tests have been carried out on a single-phase 7-level CHB converter, which allows more flexibility in measurements and system configuration, and on one phase of the UNIFLEX-PM converter, already described in Chapter 2.

6.3.1 7-Level, 3kW, Cascaded H-Bridge converter

The 7-level CHB converter, assembled and tested at the University of Nottingham, is shown in Figure 6.19 configured according to Figure 6.2.

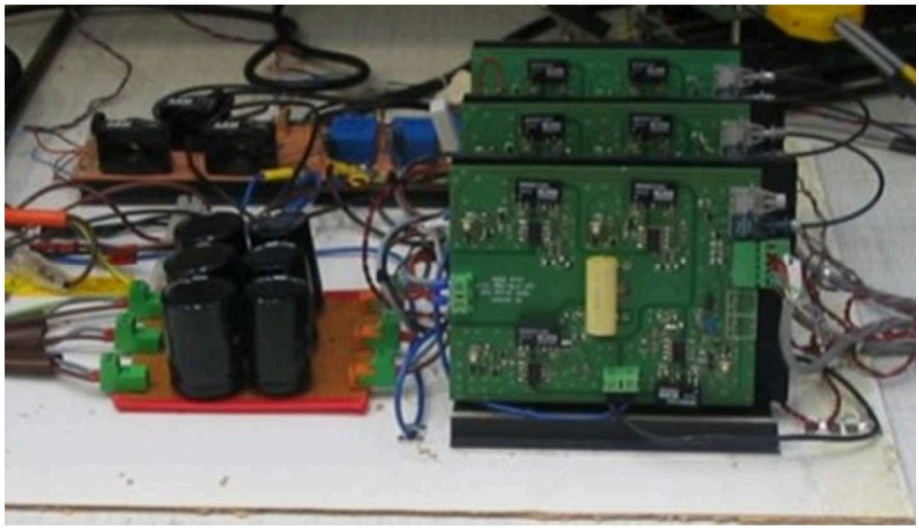


Figure 6.19 Seven Level CHB converter used for experimental verification

The converter is composed of three Semikron SK30GH123 H-Bridge modules, three DC-Link capacitors, three resistive loads and one AC side inductor. The control scheme for the converter is implemented using a Texas Instruments TI6711DSK board. This is interfaced to an FPGA card designed at the University of Nottingham. A total of 5 measurements are required to operate the converter: 3 DC-Link capacitor voltages, the AC voltage and current.

Two different operational modes are used for the converter to verify the modulation behaviour: inverter mode with fixed DC-Link voltages and an RL AC load and active rectifier mode with resistive DC loads and an inductive line filter at the grid interface. The former has been used in an open-loop configuration with the DC-Link voltages provided by three isolated DC voltage sources; the active rectifier mode has been used in a closed-loop configuration with the AC

voltage provided by an electronic AC power supply. This is used in order to be able to differentiate between low order harmonics generated by the converter, and these in the AC supply. In the latter case the proposed DBC is used to regulate the DC-Link voltages at the desired value. The experimental tests have been conducted using the parameters shown in Table 6.2. The first experimental test using the DCM without voltage balancing algorithm and device parasitic effects compensation is illustrated in Figure 6.20.

Table 6.2 Experimental parameters for 3kW prototype testing.

Name	**Description**	**Units**	**Value**
C	DC-Link Capacitor / H-Bridge	[μF]	3300
R	Load Resistor / H-Bridge	[Ω]	57 / var
L	Inductor	[mH]	11
f_s	Control sampling frequency / Active Rectifier configuration	[kHz]	10 / 2.5
f_{sw}	Converter switching frequency / Active Rectifier configuration	[kHz]	5 / 1.25
f_{sw}	Converter switching frequency / Inverter configuration	[kHz]	2.5
V_{DC}	DC Voltage / H-Bridge / Inverter configuration	[V]	60
V_d	Diode voltage drop	[V]	1.3
V_q	Transistor voltage drop	[V]	2.1
R_d	Diode on resistance	[mΩ]	32
R_q	Transistor on resistance	[mΩ]	52

The test has been performed in inverter mode with a modulation index of 0.83 and a switching frequency of 830Hz per H-Bridge, corresponding to a total apparent switching frequency of 2.5kHz. Such a test demonstrates that the proposed modulation strategy produces a symmetrical and repetitive voltage waveform.

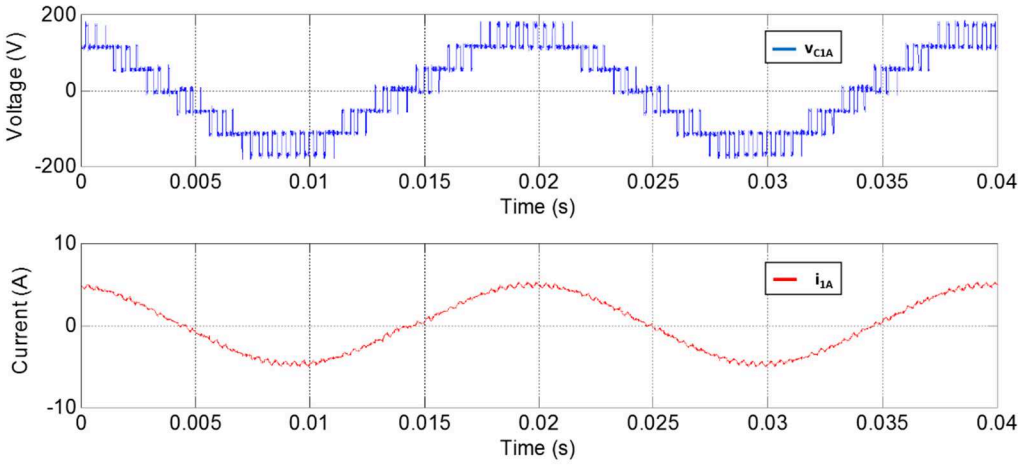


Figure 6.20 DCM: modulated voltage waveforms and current for 50 Hz modulating signal in open-loop configuration.

The second experimental test uses DCM without a voltage balancing algorithm and device parasitic components compensation. The results, shown in Figure 6.21, has been obtained with the converter in active rectifier mode under closed-loop control using a Dead-Beat current controller and an apparent switching frequency of 5kHz corresponding to a switching frequency of approximately 1.6kHz per H-Bridge.

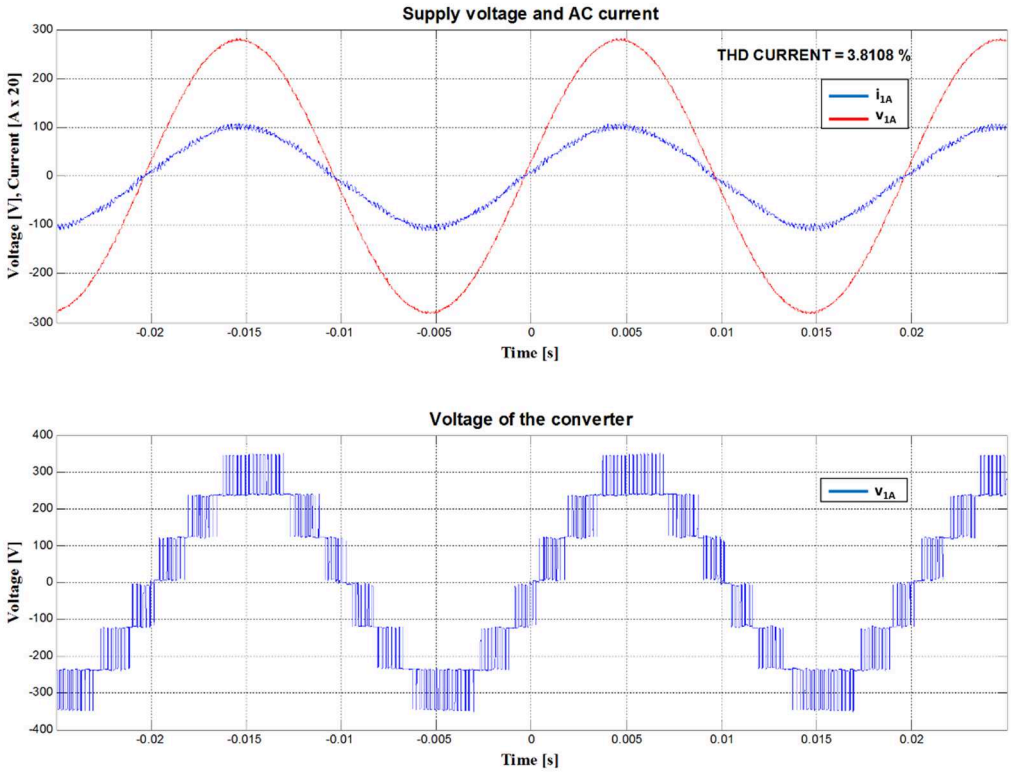


Figure 6.21 DCM: AC current, AC voltage and modulated voltage waveform for 50 Hz modulating signal in closed-loop configuration.

The modulation technique is able to produce very well balanced converter voltage waveforms under closed-loop control, where measurement errors and DC-Link ripple can potentially produce a distorted reference for the modulator. The AC current is in phase with the supply voltage, as required from the controller, and is characterised by a low harmonic content.

Figure 6.22 shows the modulated voltage waveform, obtained for a 50 Hz reference signal, the corresponding H-Bridge voltages and the line current obtained in the same operating conditions as the previous result but at a lower apparent switching frequency of 1kHz, corresponding to an approximate switching frequency per H-Bridge of around 300Hz. This test demonstrates that the proposed strategy still produces an accurate voltage waveform at lower switching frequency. This is particularly important for high power converters to reduce the switching losses. The even

distribution of the commutation between the three H-Bridges and the equalisation of the DC link voltages is clear since the peak value of each H-Bridge waveform is the same. As shown in Figure 6.22 some minor errors related with DC link voltage balance and commutation distribution can be observed. These errors are caused by the dynamics of the DC control loop, which distorts the reference signal for the modulator, and asymmetries in the converter, which generates a small unbalance of the DC Link voltages. For example, the DC load resistances differ by around 5% to the nominal value (56.4Ω, 57.3Ω and 56.5Ω compared to a nominal value of 57Ω), affecting the natural voltage balance capability of the DCM. By including the DC-Link voltage balancing algorithm in DCM technique the modulator is able to correct this DC-Link voltage unbalance and work with variable load resistors on the DC-Link.

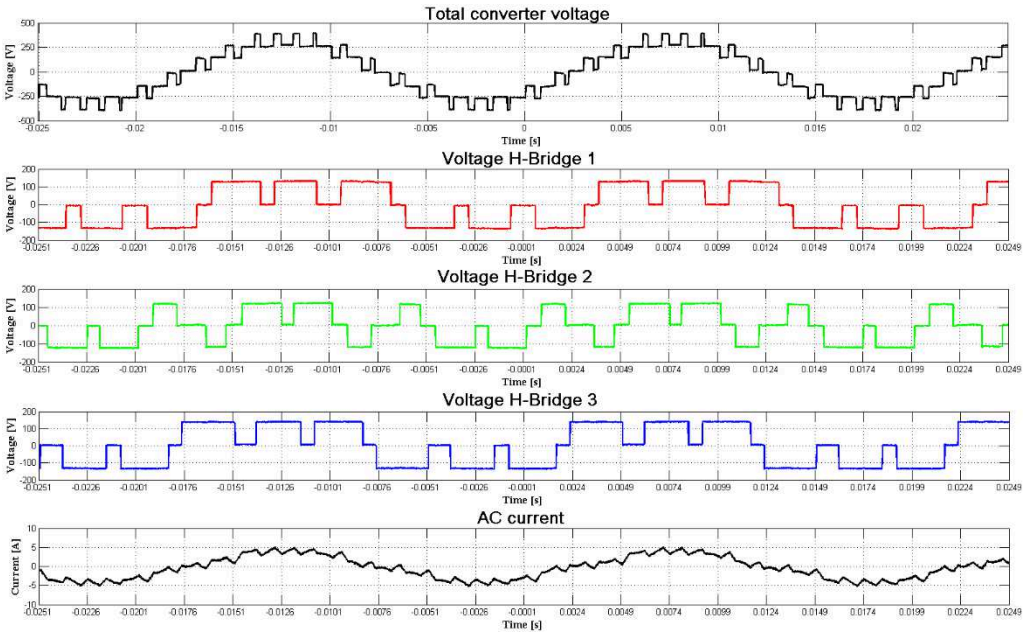


Figure 6.22 Modulated voltage waveforms and AC current for 50 Hz modulating signal in closed-loop configuration.

In order to prove the efficacy of the DC-Link voltage balancing algorithm, three additional experimental tests are performed; in this case an autotransformer is used as AC voltage supply in order to consider a more realistic operational environment. The first one considers three balanced DC loads of 57Ω. The results, shown in Figure 6.23, allow the evaluation of the performance of the proposed modulator. There is no phase-shift between converter current and supply voltage as required and the current harmonic content presents a low THD value, despite the harmonic content introduced by the supply voltage and the presence of error and noise on the

measurement. Compared with the simulation results, the current THD presents a value approximately three times higher. This is mainly associated with the uncertainty on the values of the parasitic components parameters. In fact in the experimental test the nominal values are considered for R_d, R_q, V_d and V_q even if they presents variable values, dependant on current flowing through the devices and their temperature. The use of detailed lookup table describing the parasitic parameters nonlinearities may improve the resulting AC current THD.

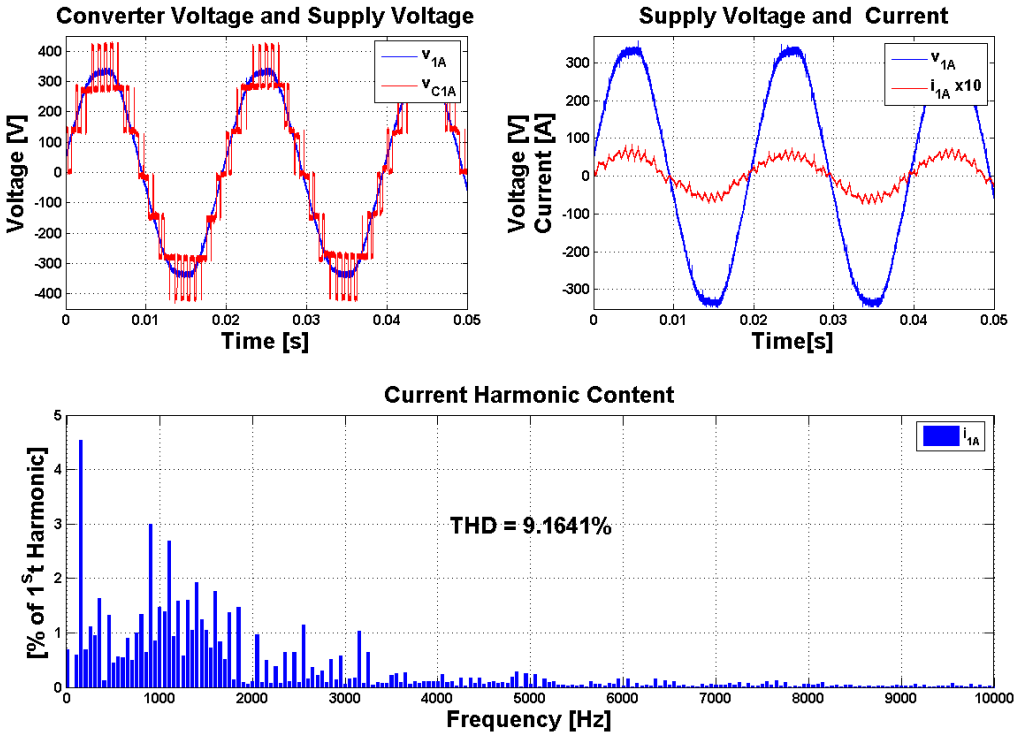


Figure 6.23 Experimental results for DCM with DC Link voltage balancing algorithm and device voltage drops, ON resistance compensation for balanced DC loads.

The second test and third test consider two DC loads transients, respectively from 63Ω-63Ω-64Ω to 51Ω-51Ω-52Ω and from 46Ω-46Ω-47Ω to 72Ω-72Ω-73Ω. The results, presented in Figure 6.24 for the second test and in Figure 6.25 for the third test, show the performance of the DC-Link voltage balancing algorithm. The DC-link voltage balance is consistently maintained and, after each step variation on the DC load, the control system recovers the desired total DC voltage value following the dynamic of the PI controller on the total DC-Link voltage. The total DC-Link voltage reference is calculated dynamically from the AC voltage RMS value and presents some distortion that does not affect the control behaviour. Moreover, the supply voltage and AC current are in phase as desired, presenting a reasonable current distortion considering the non-ideal supply voltage.

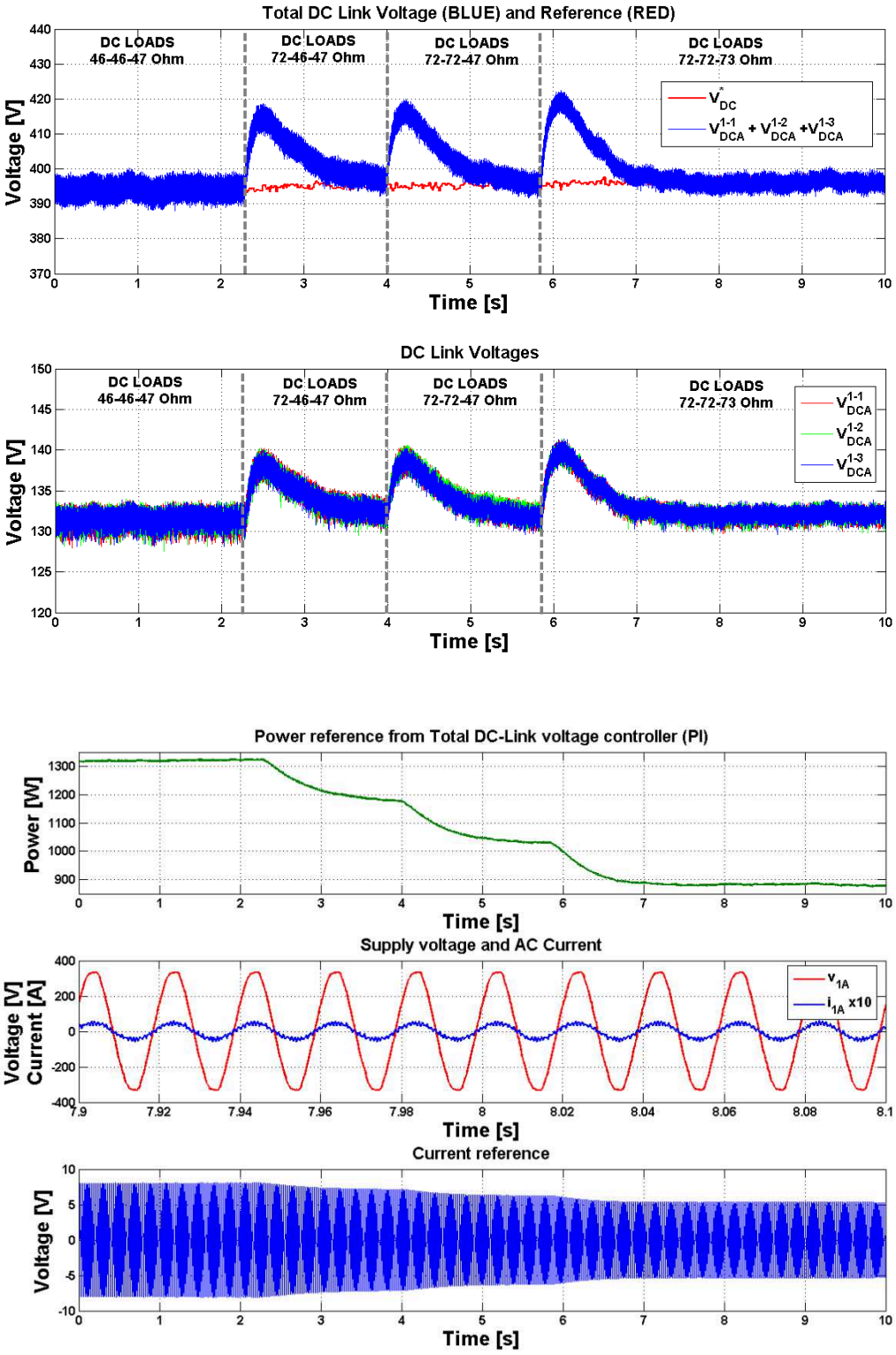


Figure 6.24 Experimental results for DCM with DC Link voltage balancing algorithm and device voltage drops, ON resistance compensation for unbalanced DC loads: first test.

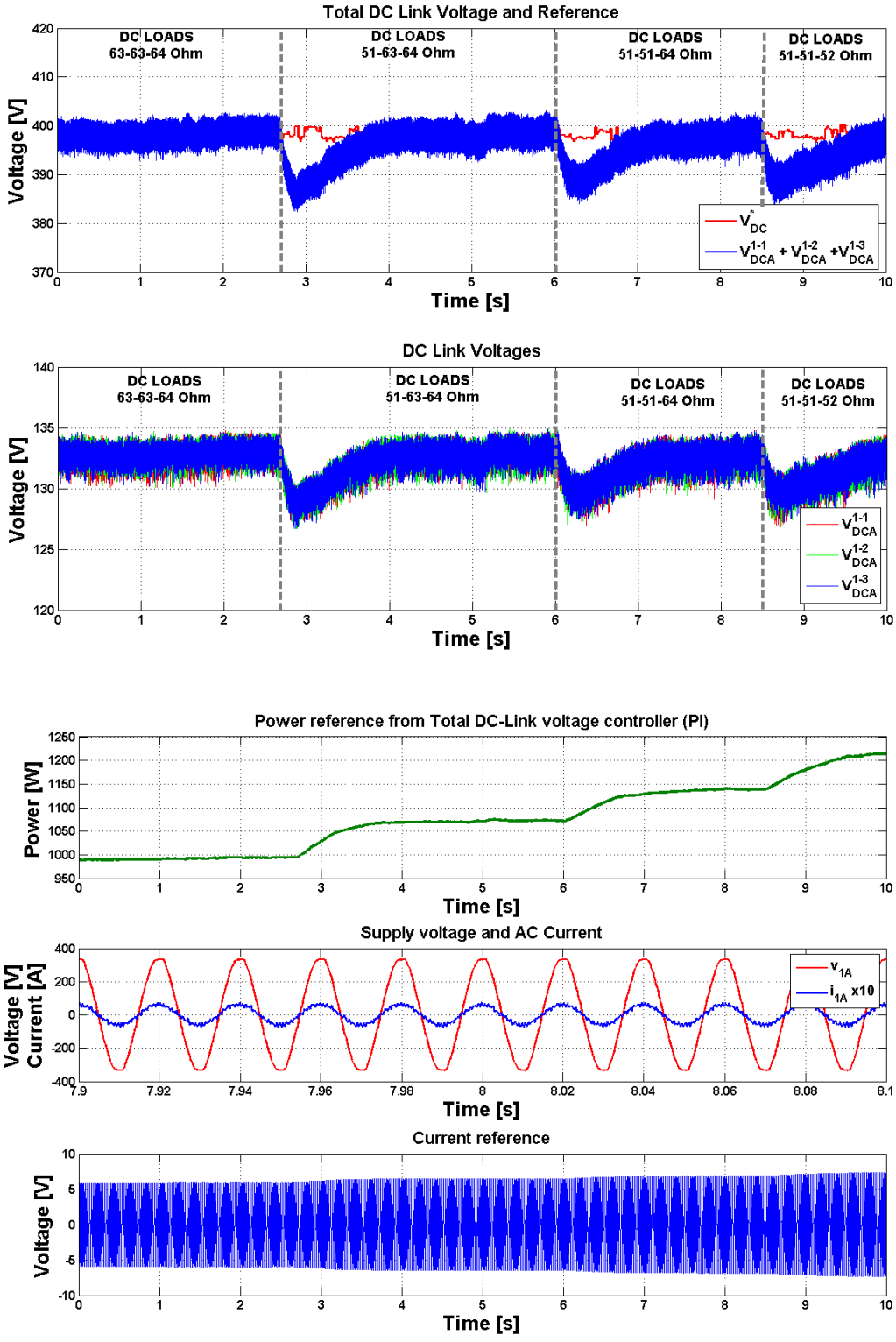


Figure 6.25 Experimental results for DCM with DC Link voltage balancing algorithm and device voltage drops, ON resistance compensation for unbalanced DC loads: second test.

6.3.2 Single phase Back-To-Back Solid State Transformer

Further experimental results have been obtained using the Back-To-Back configuration of Figure 6.26, on phase A of the UNIFLEX-PM demonstrator, described in Chapter 2, with the parameters of Table 6.3.

Table 6.3 DCM testing on UNIFLEX-PM converter experimental parameters

Name	Description	Value	Unit
V_d	Diode voltage drop	2.5	[V]
V_q	Transistor voltage drop	3.4	[V]
R_d	Diode on resistance	0.17	[mΩ]
R_q	Transistor on resistance	0.35	[mΩ]
r_L	Leakage resistance	0.3	[Ω]
L	Inductance	11	[mH]
C	Capacitance	3300	[μF]
R	Load resistance	30	[Ω]
f_s	Sampling frequency	2500	[Hz]

The test is performed on the UNIFLEX-PM converter using the proposed technique and the DCM technique.

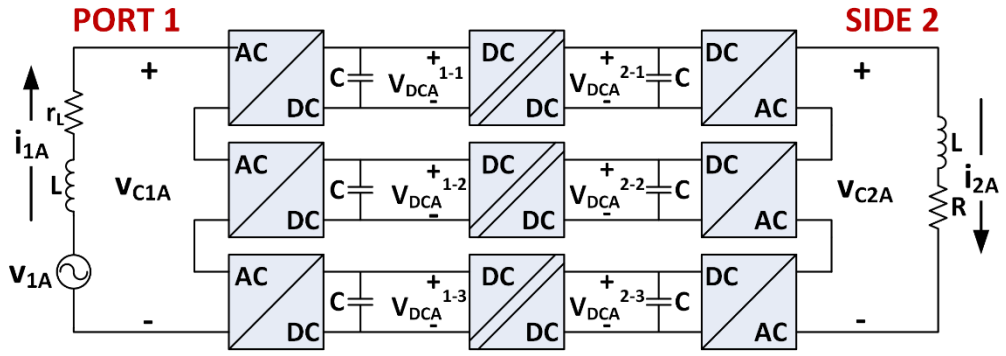


Figure 6.26 Single-phase, back-to-back configuration used for DCM testing on UNIFLEX-PM demonstrator.

The results, presented Figure 6.27 for the classic DCM and in Figure 6.28 for the improved DCM algorithm, show that even if a symmetrical converter is considered, the device parasitic components and unbalances in the power flow of the single Back-To-Back cells cause an unbalance in the DC-Link voltages which impact the generated converter voltage and line current using DCM. In particular, looking at the harmonic contents comparison of Figure 6.29 the line current has a THD greater than 10%. With the proposed technique the devices parasitic components are compensated and the capacitor voltages are actively balanced resulting in a line current THD of 6.5%.

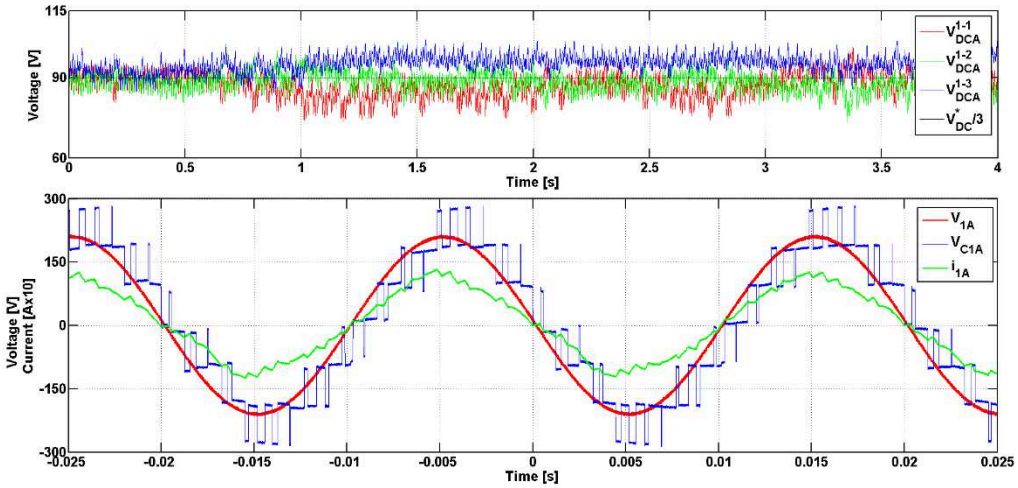


Figure 6.27 Classic DCM implementation on UNIFLEX-PM converter port 1 phase A: AC voltage and current, converter voltage and DC-Link voltages.

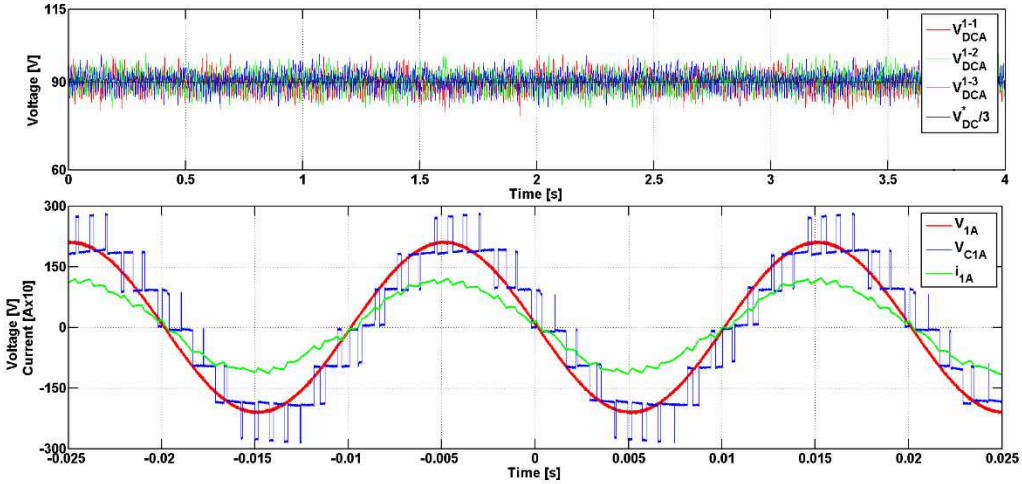


Figure 6.28 Improved DCM implementation on UNIFLEX-PM converter port 1 phase A: AC voltage and current, converter voltage and DC-Link voltages.

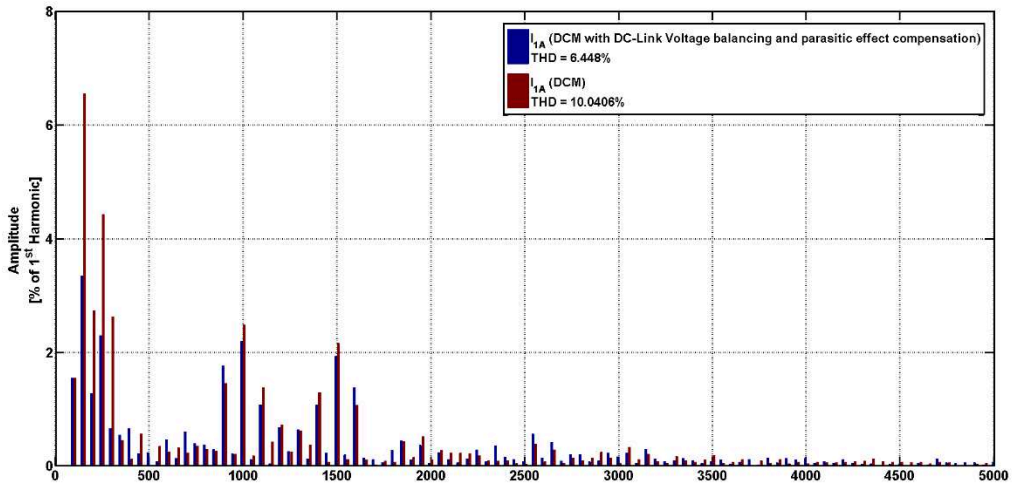
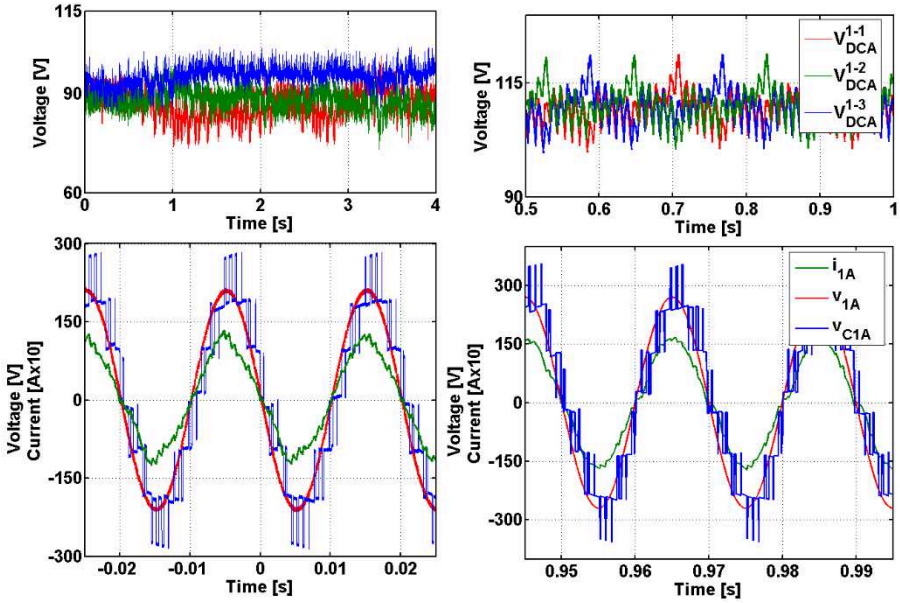


Figure 6.29 AC current harmonic content and THD comparison between simple and improved DCM.

6.4 Simulation and experimental results comparison

In Figure 7.31 the waveform obtained using the classic DCM technique described in Section 6.1.1, experimentally on the UNIFLEX-PM demonstrator and in simulation, are compared.



(a) Experimental **(b) Simulation**

Figure 6.30 Comparison between experimental and simulation results for classic DCM: DC-Link voltages, Converter voltage, AC voltage and current.

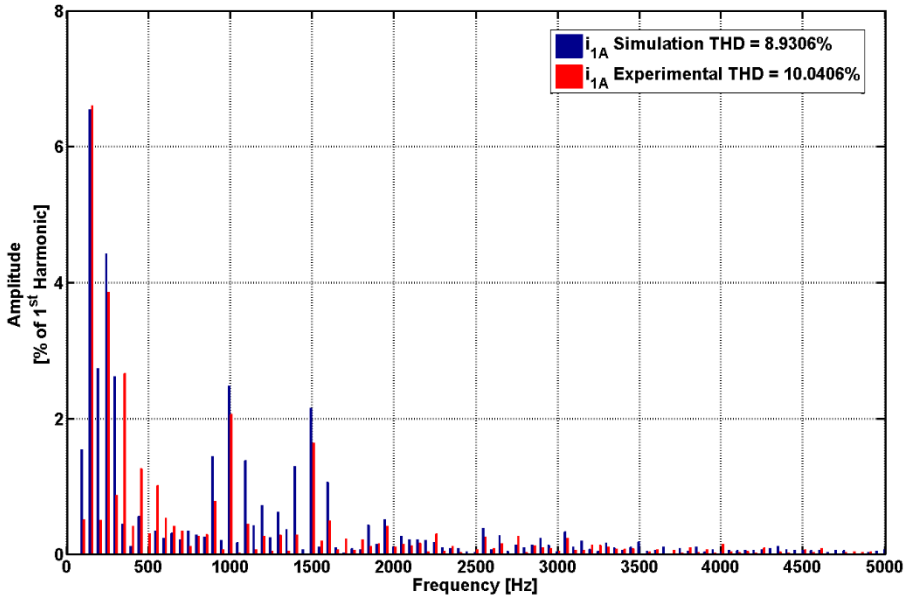
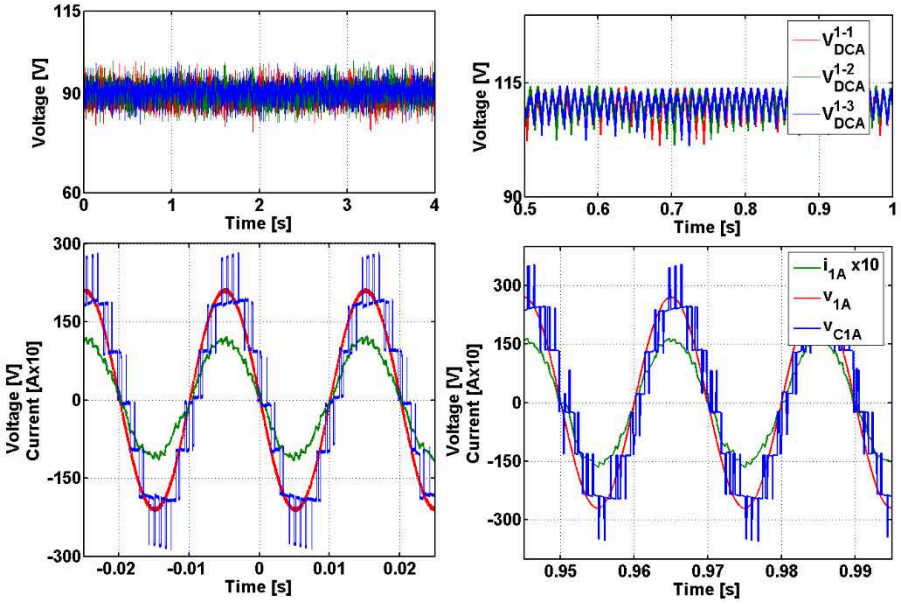


Figure 6.31 Comparison between experimental and simulation results for classic DCM: AC current harmonic content.

Clearly the asymmetries present in the real converter generate a noticeable unbalance between the DC-Link voltages which, together with Dead Times and measurement errors, generates a higher current distortion. The harmonic spectra for both results are presented in Figure 6.31. In

Figure 7.31 the waveform obtained using the improved DCM technique described in Section 6.1.2, experimentally on the UNIFLEX-PM demonstrator and in simulation, are compared. In this case the asymmetries present in real converter are compensated by the DC-Link voltage balancing algorithm. However Dead Times and measurement errors, still affect negatively the current harmonic content, as shown from Figure 7.323.



(a) Experimental **(b) Simulation**

Figure 6.32 Comparison between experimental and simulation results for DCM with DC Link voltage balancing algorithm and device voltage drops, ON resistance compensation: DC-Link voltages, Converter voltage, AC voltage and current.

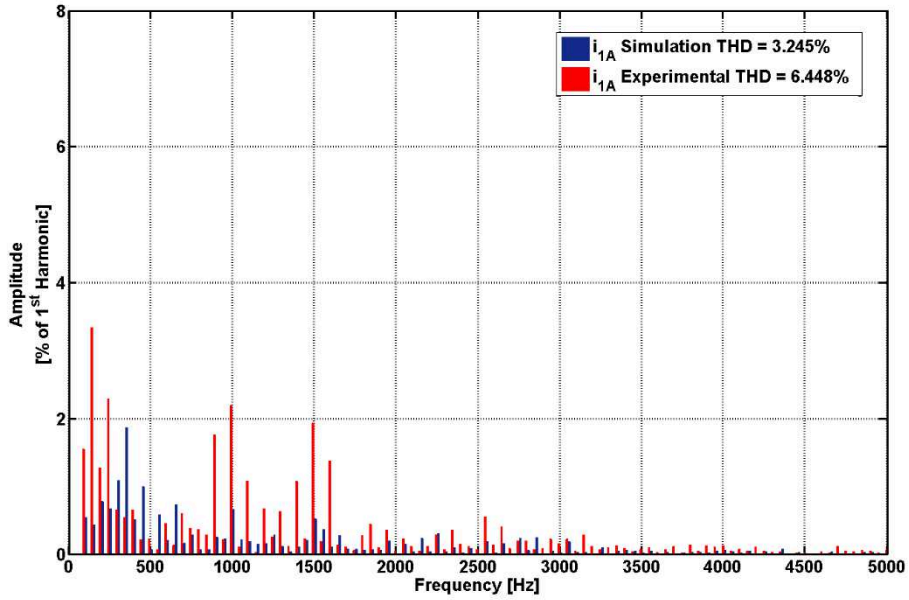


Figure 6.33 Comparison between experimental and simulation results for DCM with DC Link voltage balancing algorithm and device voltage drops, ON resistance compensation: AC current harmonic content.

6.5 Chapter summary

In this chapter a modulation scheme particularly suitable for high power CHB converters and name Distributed Commutation Modulation is described. In particular the DCM algorithm and its capability to distribute the commutations amongst the devices are described and analysed in detail.

However, using this modulation scheme the DC-Link voltage balance is achieved only applying the same load on the single HBs of the CHB converter and in any other case an additional control is required. Moreover, in case of high power, low voltage applications such as automotive applications, the device voltage drops and on-state resistance affect negatively the behaviour of the modulator.

In order to overcome these limitations two modifications to the original DCM algorithm are proposed in order to maintain the DC-Link capacitors voltages balanced for any load conditions and/or compensate the devices parasitic components.

Simulation results for DCM and its modified version are shown in comparison with PSCM, and AVM; the obtained results show that, when the converter is working as an inverter, DCM provides better switching loss management than AVM since it is able to distribute the commutations amongst the converter cells. When compared to PSCM, DCM is able to provide waveforms with a lower THD value, since it is able to generate asymmetrical voltage components.

On the other hand when the converter is working as an active rectifier and the device parasitic components are included in the simulation, the modification to the original DCM algorithm allow to obtain superior waveform quality with respect to the classical DCM and it is possible to maintain the DC-Link capacitor voltages balanced for any DC load conditions.

Experimental results, obtained on a 7-Level 3kW CHB converter and on the UNIFLEX-PM demonstrator are shown to validate the proposed modulation techniques; the obtained results validate the simulation results even if higher THD values for the converter voltages and currents are obtained, mainly because of the non idealities present in the real converter.

Chapter 7
Dead Beat control for a 2 port Solid State Transformer

Dead beat control strategies have proved to be very attractive and effective for current control in power converters. However, they are substantially dependent on the system model and on the selected discretisation method. This chapter will address the last issue by analysing different discretisation procedures and proposing an improvement to the classic Dead-Beat current control.

In High-Power applications, with increased voltages and/or currents, the losses associated with the switching of the semiconductors can have a significant impact on the converter efficiency. In order to minimise this effect, a switching frequency as low as possible must be used which unfortunately impact the controller performances. To mitigate such effects, a more accurate derivative approximation, used in the discretised control law of a Dead-Beat algorithm based controller is proposed.

Simulation results from Matlab/Simulink and experimental results from the UNIFLEX-PM demonstrator have been included in order to validate the approach undertaken.

7.1 Dead-Beat current control

In this section starting from the classic Dead-Beat current control derivation, a modified Dead-Control formulation, based on higher order derivative discretization is proposed. The control expression is derived for phase A, port 1 of a 7-Level CHB SST, shown in Figure 7.1.

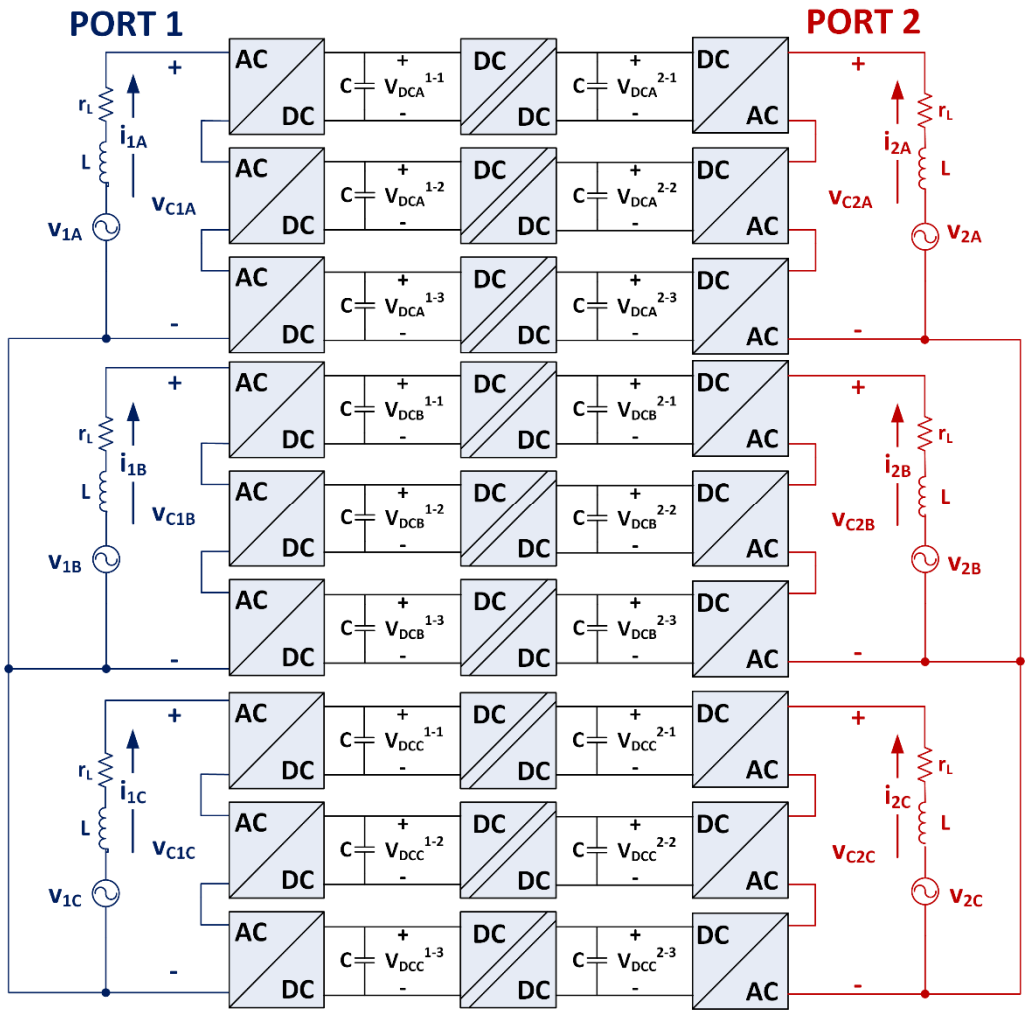


Figure 7.1 UNIFLEX-PM demonstrator two ports converter structure.

In fact, the same control approach can be equivalently applied to single phase or three phase, four wire systems where the converter voltage could be produced by any voltage source topology. Based on this considerations, to describe the control formulation is sufficient to consider the equivalent model of the AC side of one phase, shown in Figure 7.2, having the control on the other phases and ports exactly the same structure.

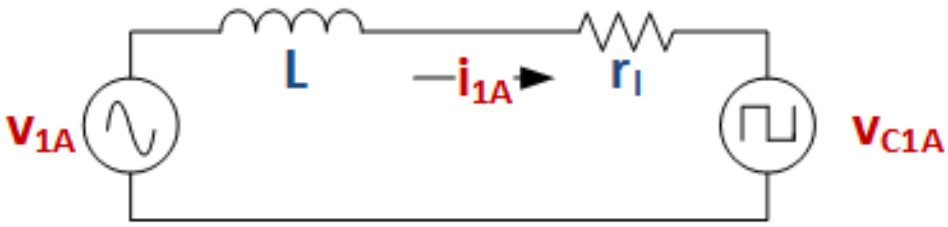


Figure 7.2 Equivalent AC circuit of the UNIFLEX-PM demonstrator, phase A, port 1.

From Figure 7.2 the AC model can be defined as follows:

$$v_{1A}(t) - v_{C1A}(t) = L\frac{di_{1A}(t)}{dt} - r_L i_{1A}(t) \tag{7.1}$$

Where v_{1A} is the AC supply voltage, v_{C1A} is the voltage applied by the converter and i_{1A} is the AC current filtered by the inductor L with a winding resistance r_L. In order to replicate the operational mode of a digital implementation, a discrete time model is required. Considering the sampling instant t_k and the discrete variable k the model can be discretised as shown in (7.2).

$$v_{1A}(t_k) - v_{C1A}(t_k) = L\frac{di_{1A}(t)}{dt}\bigg|_{t=t_k} - r_L i_{1A}(t_k) \tag{7.2}$$

It should be noted that the discretization of the derivative is a key factor in obtaining an accurate approximation of the continuous model in a discrete time domain. The discrete model has to take into account the real system limitations, such as the intrinsic delay of one sampling interval, T_s, introduced by implementation using a microcontroller or a DSP.

7.1.1 Classic Dead-Beat Current control derivation

Applying the forward Euler method to (7.2) and using the derivative approximation shown in (7.3) the discretised equation in (7.4) is obtained.

$$\frac{di_{1A}(t)}{dt}\bigg|_{t=t_k} = \frac{i_{1A}(t_k + T_s) - i_{1A}(t_k)}{T_s} \tag{7.3}$$

$$v_{1A}(t_k) - v_{C1A}(t_k) = \frac{L}{T_s}[i_{1A}(t_k + T_s) - i_{1A}(t_k)] - r_L i_{1A}(t_k) \tag{7.4}$$

Equation (7.4) is then applied to calculate the current prediction of equation (7.5), in order to compensate for the single sampling interval delay introduced by the digital implementation of

the control law, where $v_{C1A}(t_k)$ is the voltage applied by the converter at the previous sampling interval.

$$i_{1A}(t_k + T_s) = \left[1 + r_L \frac{T_s}{L}\right] i_{1A}(t_k) + \frac{T_s}{L}[v_{1A}(t_k) - v_{C1A}(t_k)] \quad (7.5)$$

The derivative approximation of (7.3) is then used to calculate the discretised model at the time instant $t_k + T_s$, where the control action is actually applied.

$$v_{1A}(t_k + T_s) - v_{C1A}(t_k + T_s) = \frac{L}{T_s}[i_{1A}(t_k + 2T_s) - i_{1A}(t_k + T_s)] - r_L i_{1A}(t_k + T_s) \quad (7.6)$$

From (7.6) it is possible to calculate the Dead-Beat control law, substituting (7.5) into (7.6) and imposing a requirement that the current at the following sampling instant is equal to the desired current reference i_{1A}^*. The result is the converter voltage v_{C1A}^* that must be applied to regulate the line current i_{1A} to the desired reference i_{1A}^* in one sampling period with, ideally, zero error.

$$v_{C1A}^*(t_k + T_s) = v_{1A}(t_k + T_s) + v_{1A}(t_k) - v_{C1A}^*(t_k) - \frac{L}{T_s}\left\{i_{1A}^*(t_k + 2T_s) - \left[1 + r_L \frac{T_s}{L}\right] i_{1A}(t_k)\right\} \quad (7.7)$$

7.1.2 Derivative discretization issues for low sampling frequency control

The discretisation approach considered in section 7.1.1 is based on the finite difference method. In fact the expression of (7.3) can be derived using a Taylor's series expansion [175].

$$i_{1A}(t_k + T_s) = \sum_{j=0}^{\infty} \frac{1}{j!} i_{1A}(t_k)^{(j)} T_s{}^j \quad (7.8)$$

In (7.8) t_k is the current discrete time instant, T_s is the sampling interval and $i_{1A}(t_k)^{(j)}$ is the j-th derivative of i_{1A} calculated in t_k. Considering T_s>0 and the Taylor's expansion truncated at the 1st order, it is possible to obtain two different expressions from (7.8), where $O(T_s{}^p)$ represents high order terms, i.e. a quantity that tends to zero, when $T_s \rightarrow 0$, as fast as $T_s{}^p$.

$$i_{1A}(t_k + T_s) = i_{1A}(t_k) + T_s i_{1A}(t_k)^I + O(T_s) \quad (7.9)$$

$$i_{1A}(t_k - T_s) = i_{1A}(t_k) - T_s i_{1A}(t_k)^I + O(T_s) \quad (7.10)$$

From (7.9) and (7.10) it is possible to obtain two first order approximations of the first derivative, shown in (7.11) and (7.12).

$$D_+ i_{1A}(t_k) = \frac{i_{1A}(t_k + T_s) - i_{1A}(t_k)}{T_s} = i_{1A}(t_k)^I + O(T_s) \tag{7.11}$$

$$D_- i_{1A}(t_k) = \frac{i_{1A}(t_k) - i_{1A}(t_k - T_s)}{T_s} = i_{1A}(t_k)^I + O(T_s) \tag{7.12}$$

Considering that the discretisation method is applied to a Dead-Beat control and that (7.11) and (7.12) have the same truncating error, of these two first order approximations only (7.11) will be considered in the rest of this chapter. To obtain a second order approximation the Taylor series expansion of (7.1) is truncated at the 2nd order obtaining the following expressions.

$$i_{1A}(t_k + T_s) = i_{1A}(t_k) + T_s i_{1A}(t_k)^I + \frac{1}{2} {T_s}^2 i_{1A}(t_k)^{II} + O\left({T_s}^2\right) \tag{7.13}$$

$$i_{1A}(t_k - T_s) = i_{1A}(t_k) - T_s i_{1A}(t_k)^I + \frac{1}{2} {T_s}^2 i_{1A}(t_k)^{II} + O\left({T_s}^2\right) \tag{7.14}$$

The derivative approximation is then calculated by subtracting (5.14) from (5.13) and dividing by $2T_s$ as follows:

$$D_c i_{1A}(t_k) = \frac{i_{1A}(t_k + T_s) - i_{1A}(t_k - T_s)}{2T_s} = i_{1A}(t_k)^I + O\left({T_s}^2\right) \tag{5.15}$$

A better approximation can be obtained by including the higher order terms of the Taylor's series expansion; however, this approach requires more samples to be recorded. In particular, it is possible to truncate the Taylor's series after the 5th order [175] as in (5.16), where the matrix *A* is defined by (5.17).

$$\begin{bmatrix} i_{1A}(t_k - 2T_s) \\ i_{1A}(t_k - T_s) \\ i_{1A}(t_k) \\ i_{1A}(t_k + T_s) \\ i_{1A}(t_k + 2T_s) \end{bmatrix} = A \begin{bmatrix} i_{1A}(t_k) \\ i_{1A}(t_k)^I \\ i_{1A}(t_k)^{II} \\ i_{1A}(t_k)^{III} \\ i_{1A}(t_k)^{IV} \end{bmatrix} \tag{7.16}$$

$$A = \begin{bmatrix} 1 & -2T_s & \frac{1}{2}(2T_s)^2 & -\frac{1}{6}(2T_s)^3 & \frac{1}{24}(2T_s)^4 \\ 1 & -T_s & \frac{1}{2}{T_s}^2 & -\frac{1}{6}{T_s}^3 & \frac{1}{24}{T_s}^4 \\ 1 & 0 & 0 & 0 & 0 \\ 1 & T_s & \frac{1}{2}{T_s}^2 & \frac{1}{6}{T_s}^3 & \frac{1}{24}{T_s}^4 \\ 1 & 2T_s & \frac{1}{2}(2T_s)^2 & \frac{1}{6}(2T_s)^3 & \frac{1}{24}(2T_s)^4 \end{bmatrix} \tag{7.17}$$

From (7.16) and (7.17) is possible to obtain an approximation of the first derivative applying a linear combination of the first vector in (7.16) with coefficient h_1, h_2, h_3, h_4, h_5.

$$D_1 i_{1A}(t_k) = [h_1 \quad h_2 \quad h_3 \quad h_4 \quad h_5] \begin{bmatrix} i_{1A}(t_k - 2T_s) \\ i_{1A}(t_k - T_s) \\ i_{1A}(t_k) \\ i_{1A}(t_k + T_s) \\ i_{1A}(t_k + 2T_s) \end{bmatrix} \tag{7.18}$$

Applying (7.16) to (7.18) and collecting the coefficients related to the same derivative, it can be observed that, in order to obtain the desired approximation of the first derivative, is necessary to impose the constraint $D_1(t_k)=i_{1A}(t_k)^I$. By imposing this constraint the system which defines the coefficients of the linear combination can be written as in (7.19).

$$\begin{bmatrix} 1 & 1 & 1 & 1 & 1 \\ -2 & -1 & 0 & 1 & 2 \\ 4 & 1 & 0 & 1 & 4 \\ -8 & -1 & 0 & 1 & 8 \\ 16 & 1 & 0 & 1 & 16 \end{bmatrix} \begin{bmatrix} h_1 \\ h_2 \\ h_3 \\ h_4 \\ h_5 \end{bmatrix} = \begin{bmatrix} 0 \\ 1 \\ \overline{T_s} \\ 0 \\ 0 \\ 0 \end{bmatrix} \tag{7.19}$$

Solving the system in (7.19) the desired approximation of the derivative of the 5th order is obtained, as shown in (7.20).

$$D_1 i_{1A}(t_k) = \frac{1}{3T_s}\left[\frac{i_{1A}(t_k - 2T_s)}{4} - 2i_{1A}(t_k - T_s) + 2i_{1A}(t_k + T_s) + \frac{i_{1A}(t_k + 2T_s)}{4}\right] \tag{7.20}$$

$$D_1 i_{1A}(t_k) = i_{1A}(t_k)^I + O\left({T_s}^5\right) \tag{7.21}$$

A first approach to calculate the approximation error produced by the three different solutions, defined by (7.11), (7.15) and (7.20), can be made by considering the following sinusoidal function.

$$i(t) = sin(\omega t) \tag{7.22}$$

In this case the derivative at $t=t_k$ is equal to the angular coefficient of the line tangent to $i(t)$ at the time instant t_k and can be analytically calculated as in (7.23) in order to define the tangent line equation in (5.24).

$$i^I(t_k) = \left.\frac{dI(t)}{dt}\right|_{t=t_k} = \omega\, cos(\omega t_k) \tag{7.23}$$

$$T(t, t_k) = i(t_k) + i^I(t_k)(t - t_k) \tag{7.24}$$

Using this approach an approximation of the tangent line equation is obtained for each derivative discretisation method resulting in three tangent line equation approximations at a specified time instant t_k, respectively $T_+(t,t_k)$, $T_C(t,t_k)$ and $T_I(t,t_k)$, described from (7.25), (7.26) and (7.27) for the three considered derivative discretisation, $D_+I(t_k)$, $D_CI(t_k)$ and $D_1I(t_k)$.

$$T_+(t,t_k) = i(t_k) + D_+i(t_k)(t-t_k) \tag{7.25}$$

$$T_C(t,t_k) = i(t_k) + D_Ci(t_k)(t-t_k) \tag{7.26}$$

$$T_1(t,t_k) = i(t_k) + D_1i(t_k)(t-t_k) \tag{7.27}$$

In Figure 7.3 a comparison between (7.24) and the three different tangent lines, obtained by using the previous derivative approximation methods, is shown for t_k=*0.003s*, considering a sampling frequency f_s= *1kHz*. It is clear that the expressions described in (7.20) and (7.15) approximate the line tangent to $i(t_k)$ with a minimal error.

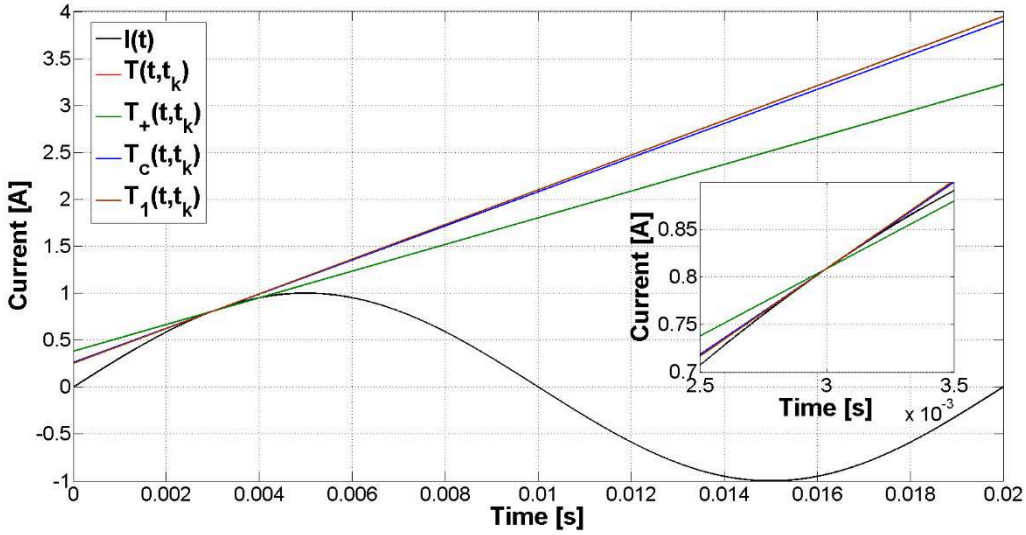


Figure 7.3 Comparison between different derivative's approximations in ideal conditions: line tangent to a sinusoidal function for t_k=0.003s and f_s=1kHz.

In Figure 7.4 the approximation of the derivative is compared with the analytical solution described in (7.23) considering the normalized errors, $E_+(t_k)$, $E_C(t_k)$ and $E_I(t_k)$, defined as:

$$E_+(t_k) = 100\left|\frac{D_+i(t_k) - i^I(t_k)}{\omega}\right| \tag{7.28}$$

$$E_C(t_k) = 100\left|\frac{D_Ci(t_k) - i^I(t_k)}{\omega}\right| \tag{7.29}$$

$$E_1(t_k) = 100\left|\frac{D_1i(t_k) - i^I(t_k)}{\omega}\right| \tag{7.30}$$

The approximation of the derivative described in (7.11) has an error that raises with the non-linearity of the curve *i(t)* while (7.15) maintains an error under 2% and (7.20) under 0.1%.

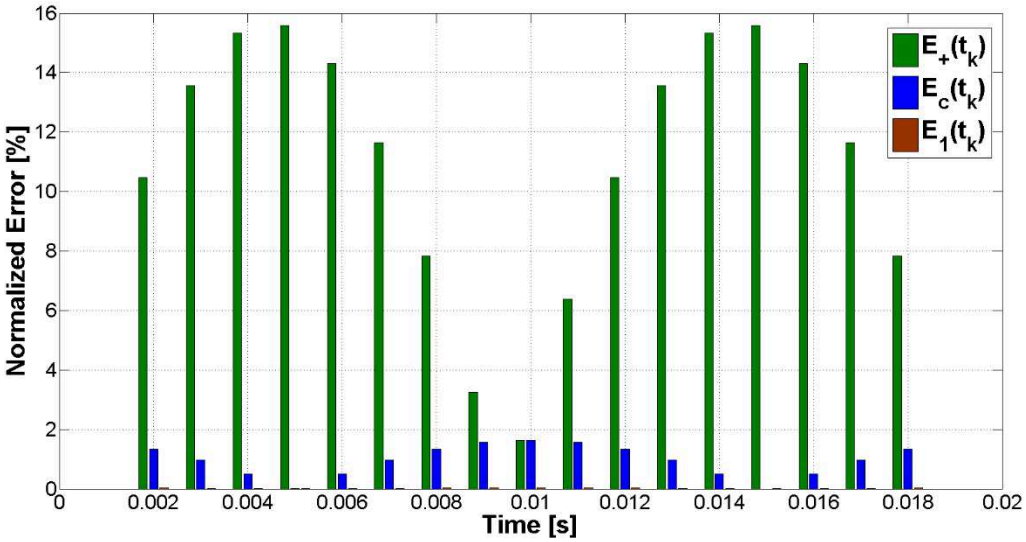


Figure 7.4 Comparison between different derivative's approximations in ideal conditions: normalized error for T_s=0.001s.

Figure 7.5 shows the results obtained when white noise is added to the function *i(t)* in (7.22), in order to reproduce more realistic measurement conditions. The results shows that (7.15) perform the best approximation to the line tangent to $i(t_k)$. It is possible to explain this behaviour by considering that expression (7.20) requires the value of *i(t)* in four different sampling instants. If the measurement is corrupted by noise using (7.20) a larger error is introduced in the derivative's approximation.

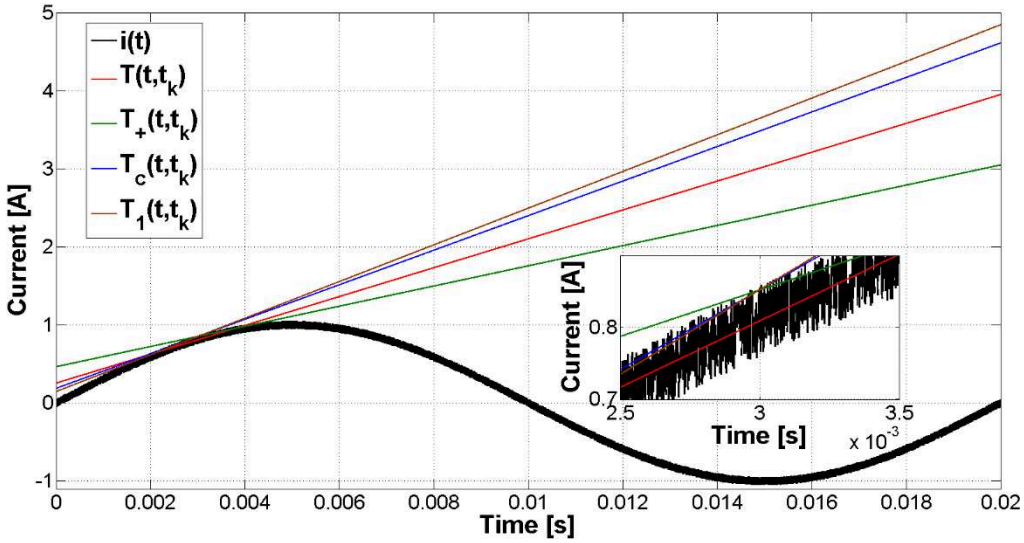


Figure 7.5 Comparison between different derivative approximations in real conditions: line tangent to a sinusoidal function: t_k=0.003s; f_s=1kHz.

In Figure 7.6 a comparison between the normalized errors in presence of white noise, calculated as in (7.28), (7.29) and (7.30), is shown. Clearly the approximation of the derivative described in (7.11) still has the largest error but (7.15) has an error that is comparable with the one obtained from (7.20). Considering that (7.15) has a lower computational overhead and, under real operating conditions, has the lowest error, it can be concluded that is the best choice to approximate the derivative and, thus, is used to design the proposed Dead-Beat current control.

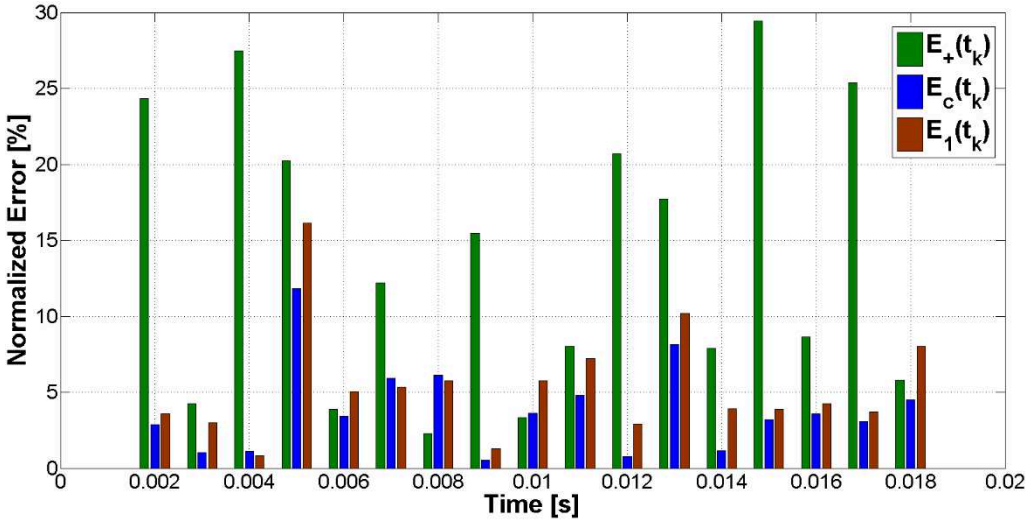


Figure 7.6 Comparison between different derivative's approximations in real conditions: normalized error for T_s=0.001s.

7.1.3 Proposed Dead-Beat current control

From (7.2) the Dead-Beat control law is obtained applying the desired approximation for the derivative [93], [175], [176], described in (7.15), and imposing the requirement that the current in the next sampling interval is equal to the desired current reference i_{1A}^*, obtaining the control law shown in (7.31).

$$v_{C1A}^*(t_k + T_s) = v_{1A}(t_k + T_s) - \frac{L}{2T_s}[i_{1A}^*(t_k + 2T_s) - i_{1A}(t_k)] + r_L i_{1A}^*(t_k + T_s) \quad (5.31)$$

As a consequence of the delay introduced by the digital implementation, at the sampling instant t_k the reference for the converter at the sampling instant t_k+T_s is calculated [175]. For this case no other predictions are needed to compensate the computational delay introduced by the digital implementation, since the controller is able to generate the desired converter voltage reference using only the current measured at the time instant t_k.

The overall control scheme is shown in Figure 7.7 where $V_{DCA}^{1\text{-}TOT}$ is the total DC-Link capacitors voltage on phase A, port 1 of the 7-Level CHB SST and V_{DC}^{*} is the desired total DC-Link voltage reference.

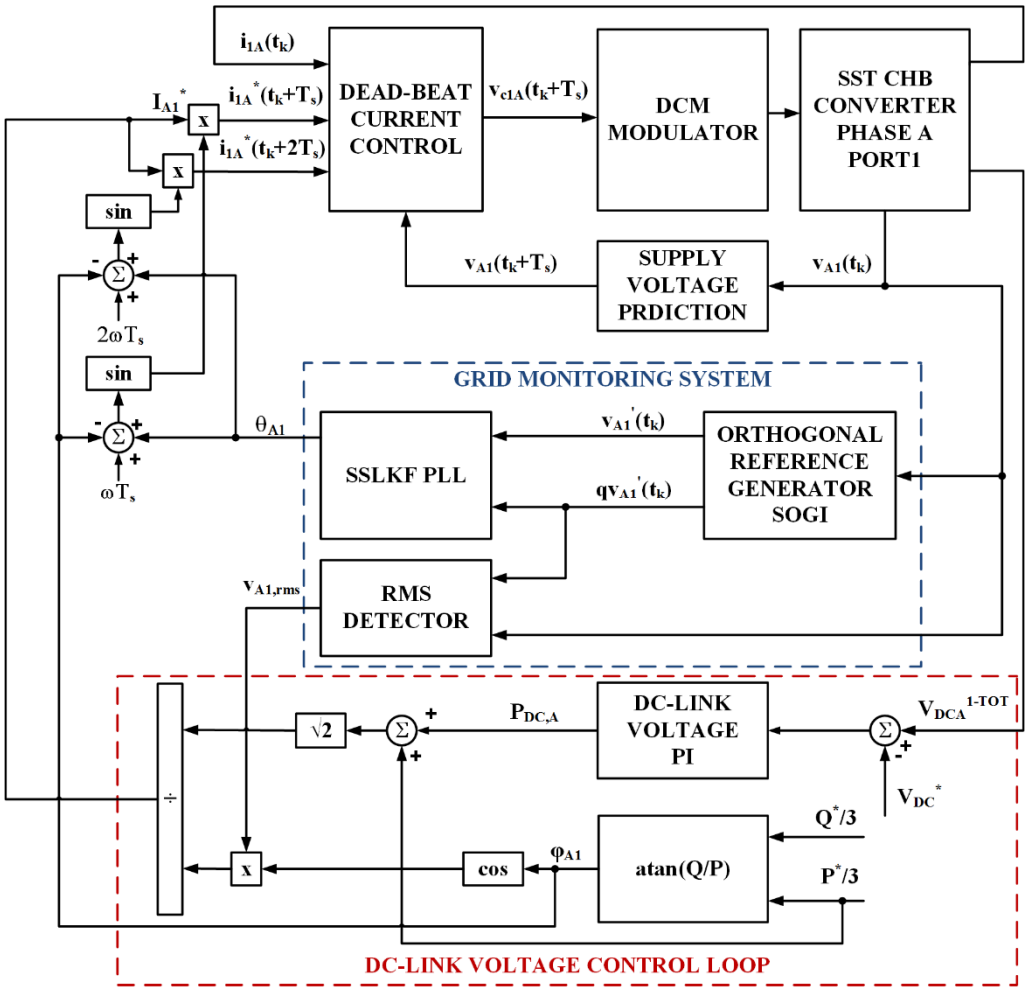


Figure 7.7 Dead-Beat control system block diagram.

The aim of the control is to provide the AC current necessary to regulate the DC link voltage at the required reference and also therefore regulate active and reactive power at the desired references P^{*} and Q^{*}. The power is considered equally shared between the three phases and for this reason the power references are divided by three on each phase. The AC current reference is calculated on the basis of the required active and reactive power, P^{*}, Q^{*}, the active power required to regulate the total DC-Link voltage on phase A port 1, $P_{DC,A}$, and the angle and RMS value of the AC voltage, respectively θ_{A1}, and $V_{A1,RMS}$.

$$\varphi_{A1} = atan\left(\frac{\frac{P^*}{3} + P_{DC,A}}{Q^*}\right) \tag{7.32}$$

$$i_{1A}{}^*(t_k + iT_s) = \frac{{}^{P^*}/_3 + P_{DC,A}}{\cos(\varphi_{A1})\, V_{A1,rms}\sqrt{2}} sin(\theta + iT_s - \varphi_{A1}) \quad , \quad i = 1{,}2 \tag{7.33}$$

Clearly since the DC-Link capacitor voltages are independently controlled on the three phases, asymmetries between the converter phases are compensated by the DC-Link voltage control by controlling $P_{DC,A}$. The design of the PI controller is described in Appendix B while the single phase SSLKF PLL/SOGI and the RMS detector has already been described in Chapter 4.

The output of this cascaded control is an average voltage reference for the converter AC side voltage in the next sampling period. A suitable modulation technique is required to apply this demand to the converter; the DCM technique with DC-Link voltage balancing algorithm has been decided to be applied as already discussed in the previous chapter.

The Dead-Beat current control also requires the prediction of the supply voltage v_{A1} that is obtained from previous periods as described in Appendix A, assuming ideal supply operating conditions.

7.1.4 Frequency analysis

Considering the circuit of Figure 7.2 a discrete time frequency analysis has been performed for both the classic and the proposed improved DBC. The current control block scheme is shown in Figure 7.8 where *P(z)* is the discretized transfer function of the circuit, *C(z)* is the DBC transfer function and z^{-1} is a unitary delay of a sampling interval T_s.

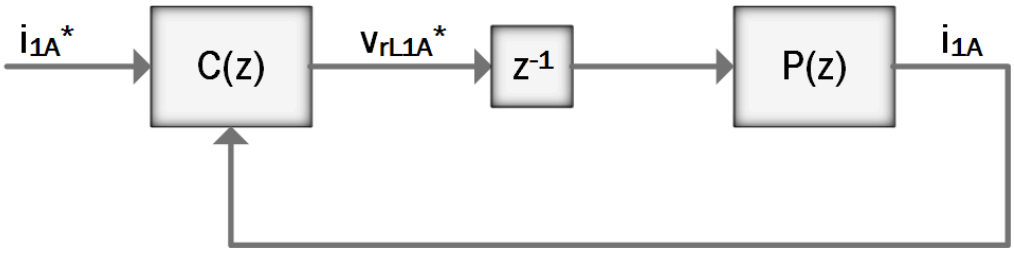


Figure 7.8 Simplified DBC block scheme for frequency analysis.

The circuit transfer function can be derived considering an ideal prediction of the supply voltage starting from the continuous time model.

$$v_{1A}(t) - v_{C1A}(t) = v_{rL1A}(t) = L\frac{di_{1A}(t)}{dt} + r_L i_{1A}(t) \tag{7.34}$$

$$G_{PLANT}(s) = \frac{i_{1A}(s)}{v_{rL1A}(s)} = \frac{1}{r_L + sL} \tag{7.35}$$

To simplify the analytical model description the voltage across the inductor v_{rL1A}, defined by the inductance L and the winding resistance r_l, is considered as the plant input instead of the converter voltage v_{c1A}. In this way any prediction of the voltage across the inductor imply that the prediction of the supply voltage is known. The discrete time model, at a given sampling frequency T_s, is obtained from the discretised model of equation (7.31) as follows.

$$i_{1A}(k+1) = \alpha_1 i_{1A}(k) + \alpha_2 v_{rL1A}(k) \tag{7.36}$$

$$\alpha_1 = e^{-\frac{r_L}{L}T_S} \cong 1 - \frac{r_L T_s}{L} \tag{7.37}$$

$$\alpha_2 = \frac{1}{r_L}\left(1 - e^{-\frac{r_L}{L}T_S}\right) \cong \frac{T_s}{L} \tag{7.38}$$

$$G_{PLANT}(z) = \frac{i_{1A}(z)}{v_{rL1A}(z)} = \frac{\alpha_2}{z - \alpha_1} \tag{7.39}$$

The control transfer function is calculated for both the classic and the proposed DBC. Considering the classic DBC derivation the control law can be expressed, from (7.7) and (7.36)-(7.38), as follows.

$$v_{rL1A}{}^*(k+1) = \beta_2 i_{1A}{}^*(k+2) + \beta_1 i_{1A}(k+1) =$$

$$= \beta_2 i_{1A}{}^*(k+2) + \alpha_1\beta_1 i_{1A}(k) + \alpha_2\beta_1 v_{rL1A}(k) \tag{7.40}$$

The control constants β_1 and β_2 can be calculated by using knowledge of the model parameters. It should be noted that the approximation is valid only in case of time invariant model parameters.

$$\beta_1 = 1 - \frac{r_L T_s}{L} \cong \alpha_1 \tag{7.41}$$

$$\beta_2 = \frac{L}{T_s} \cong \frac{1}{\alpha_2} \tag{7.42}$$

The DBC transfer function can be calculated as follows.

$$G_C(z) = \left[\frac{v_{rL1A}{}^*(z)}{i_{1A}(z)}\right]_{i_{1A}{}^*(z)=0} + \left[\frac{v_{rL1A}{}^*(z)}{i_{1A}{}^*(z)}\right]_{i_{1A}(z)=0} =$$

$$= \beta_2 \frac{z^2 - {\beta_1}^2}{z + \beta_1} = \beta_2 \frac{(z - \beta_1) * (z + \beta_1)}{z + \beta_1} \tag{7.43}$$

The closed loop transfer function of the system, *G(z)*, is then calculated as in (7.44).

$$G(z) = G_C(z) G_{PLANT}(z) z^{-1} = \frac{\alpha_2}{z - \alpha_1} \beta_2 \frac{(z - \beta_1)(z + \beta_1)}{z + \beta_1} z^{-1} \cong z^{-1} \tag{7.44}$$

In this case the DBC control behaves like a delay of one sampling interval. For the case where the approximations of (7.36) and (7.37) are not valid, the zero-pole cancellation is no longer perfect as shown in Figure 7.9 for variations of *L* and in Figure 7.10 for variations of r_l.

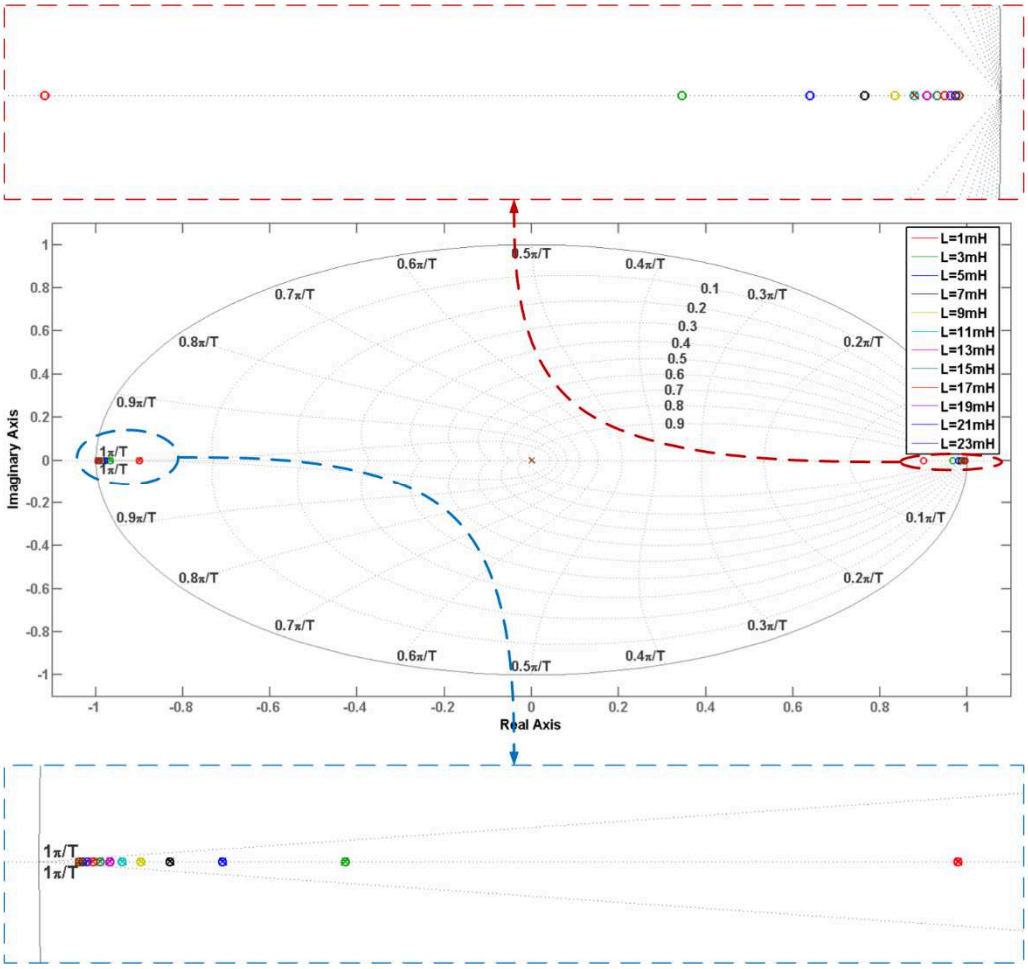


Figure 7.9 Pole-Zero map for the classical DBC at different values of L.

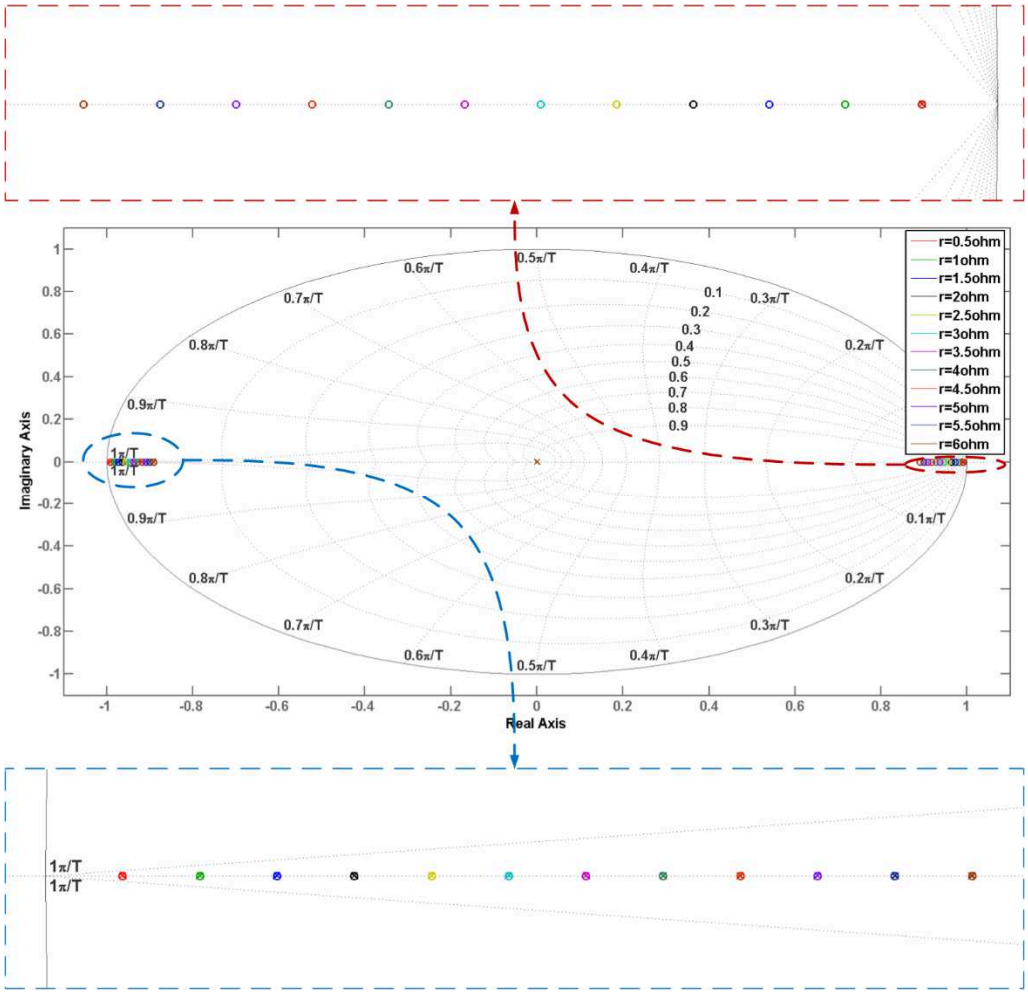


Figure 7.10 Pole-Zero map for the classical DBC at different values of r_L.

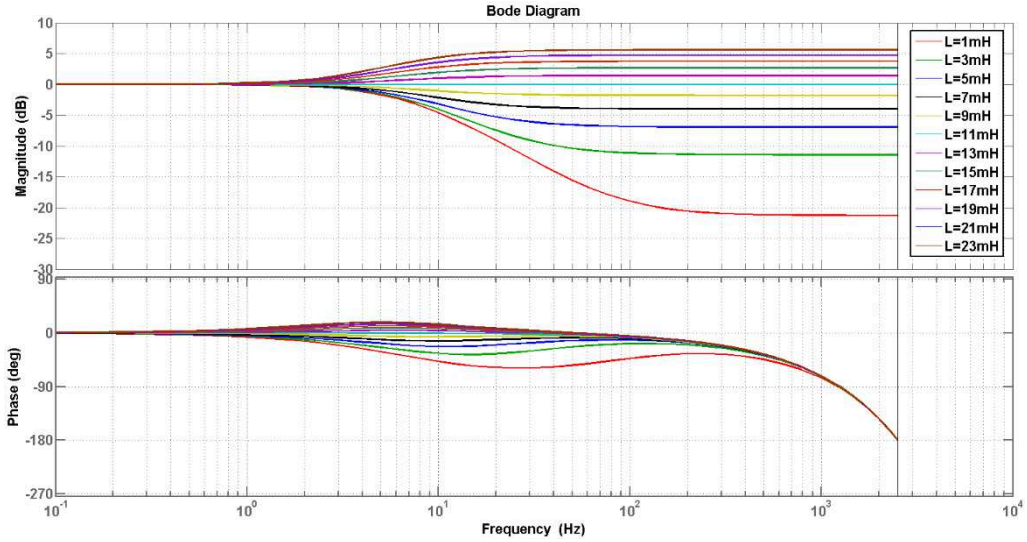


Figure 7.11 Bode diagram the classical DBC at different values of L.

This effect results in a dynamic behaviour dependant on the errors of model parameters as shown in Figure 7.11 for variations of *L* and in Figure 7.12 for variations of r_l. In particular, should be noted that for values of *L* larger than the actual value the system starts to behave as a High-Pass filter, amplifying the noise on the current measurement.

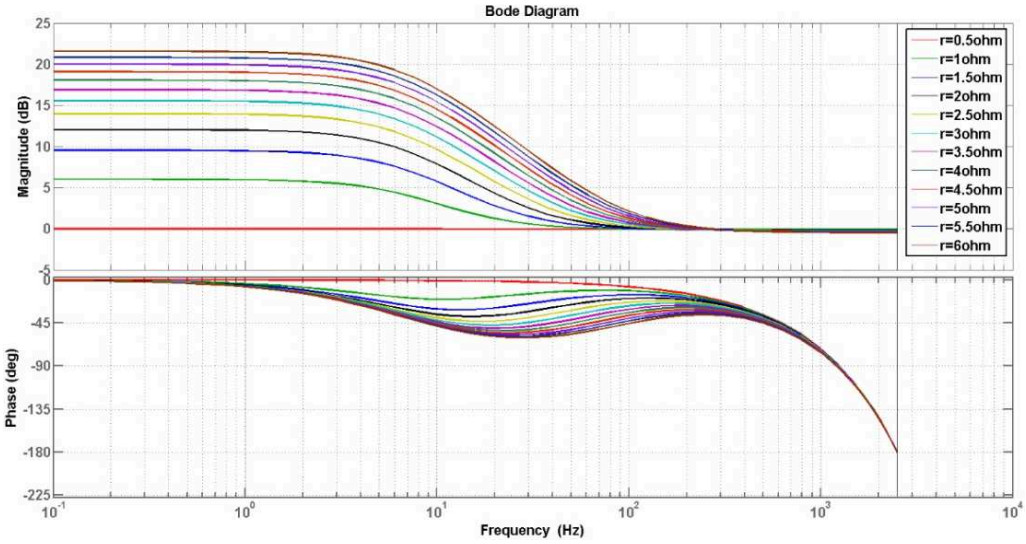


Figure 7.12 Bode diagram the classical DBC at different values of r_L.

Using the same method the proposed DBC can be expressed as in (7.45).

$$v_{rL1A}{}^*(k+1) = \gamma_2 i_{1A}{}^*(k+2) + \gamma_1\gamma_2 i_{1A}(k+1) - \gamma_2 i_{1A}(k) \tag{7.45}$$

In (7.45) the control parameters, γ_1 and γ_2, are a function of the discretised model parameters as shown in (7.46) and (7.47).

$$\gamma_1 = \frac{2r_L T_s}{L} \cong 2(1-\alpha_1) \tag{7.46}$$

$$\gamma_2 = \frac{L}{2T_s} \cong \frac{1}{2\alpha_2} \tag{7.47}$$

The DBC transfer function, obtained using the 2nd order derivative approximation, is shown in (7.48). Compared with the classic DBC transfer function, (7.48) presents two zeroes at different frequencies from the poles of the plant transfer function and a pole in the origin.

$$G_C(z) = \left[\frac{v_{rL1A}{}^*(z)}{i_{1A}(z)}\right]_{i_{1A}{}^*(z)=0} + \left[\frac{v_{rL1A}{}^*(z)}{i_{1A}{}^*(z)}\right]_{i_{1A}(z)=0} = \gamma_2 \frac{z^2 + z\gamma_1 - 1}{z} \tag{7.48}$$

This result can be highlighted from the expression of the closed loop transfer function *G(z)* where two poles in the origin are present.

$$G(z) = G_C(z)G_{PLANT}(z)z^{-1} = \frac{\alpha_2}{z-\alpha_1}\gamma_2\frac{z^2+z\gamma_1-1}{z}z^{-1} = \frac{\alpha_2}{z-\alpha_1}\gamma_2\frac{z^2+z\gamma_1-1}{z^2} \quad (7.49)$$

A parametric analysis of (7.49) for variation of *L,* shown in Figure 7.13, and for variation of r_L, shown in Figure 7.14, has been carried out. The results have highlighted that two poles in the origin of *G(z)* and one zero is cancelled almost perfectly from the pole of $G_{PLANT}(z)$. However a zero outside the unitary circle can be noticed.

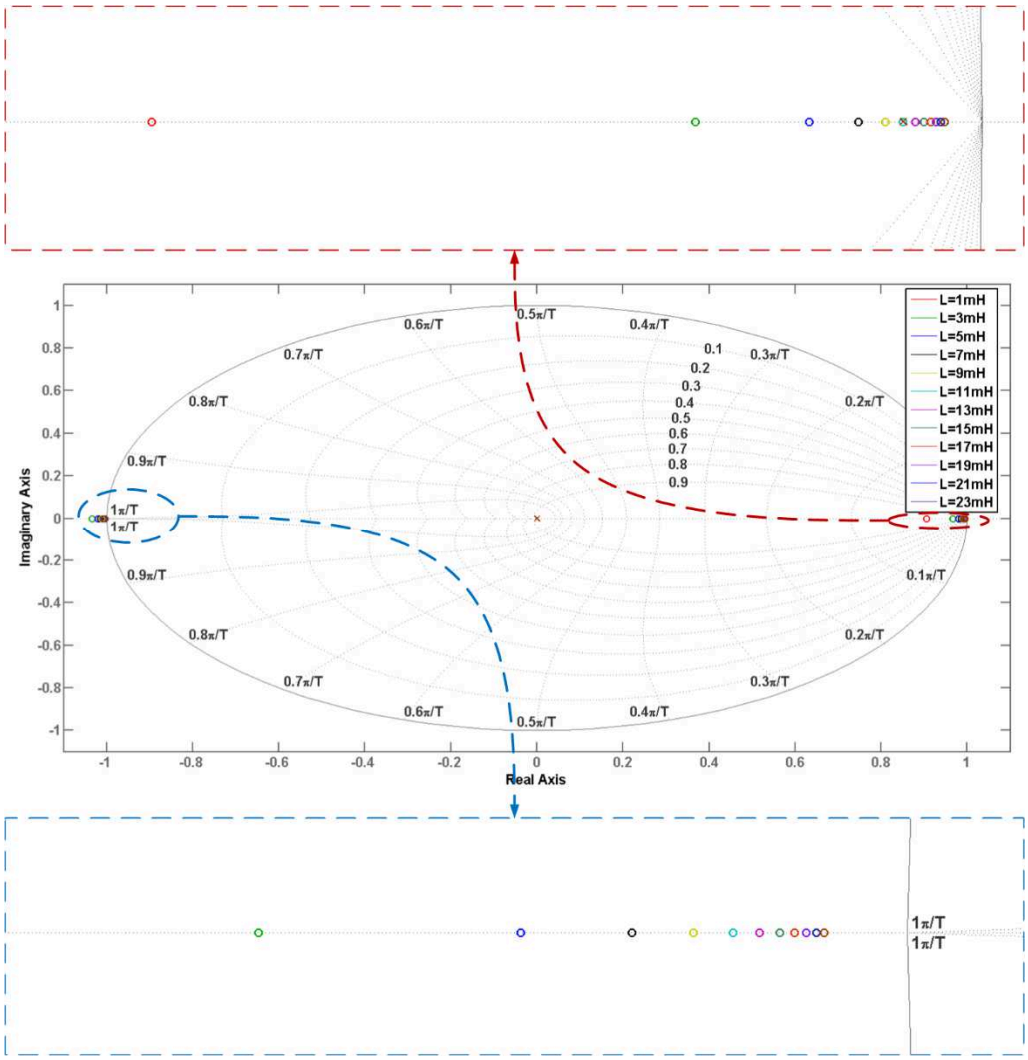


Figure 7.13 Pole-Zero map for proposed DBC varying L.

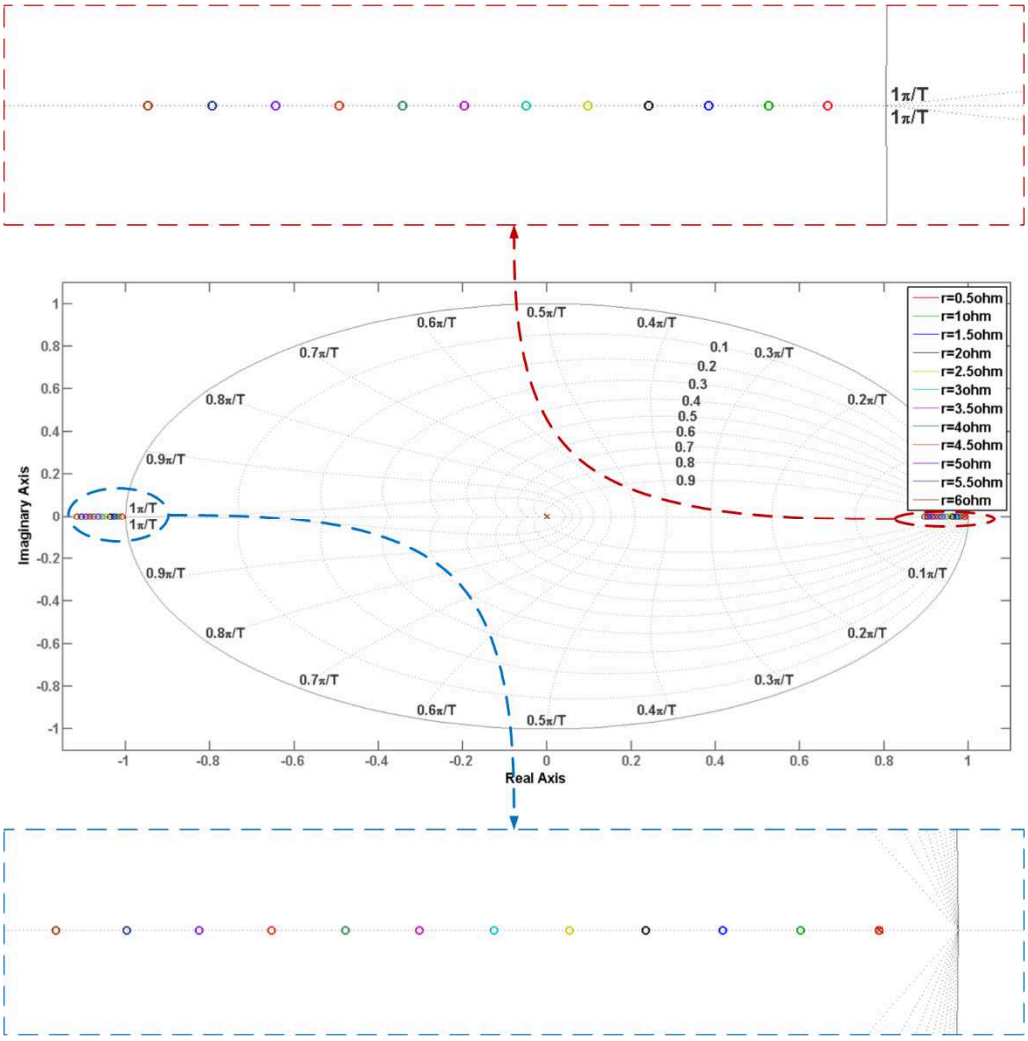


Figure 7.14 Pole-Zero map for proposed DBC varying r_L.

This effect results in a more robust behaviour of the overall system to model parameter variations, when compared to the traditional DBC, as shown in Figure 7.15 for variation of *L* and in Figure 7.16 for variation of r_L. The magnitude and phase of *G(z)* drop off when the frequency approaches the Nyquist frequency closing the system bandwidth and reducing the effect of switching and high frequency noise on measurement whilst maintaining good dynamic performance in terms of bandwidth, phase and gain margin.

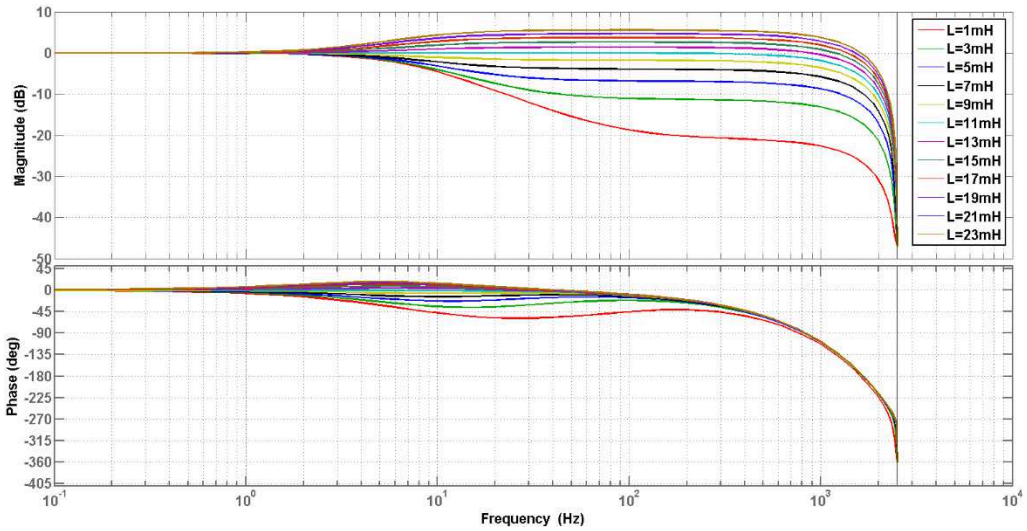


Figure 7.15 Bode diagram for proposed DBC varying L.

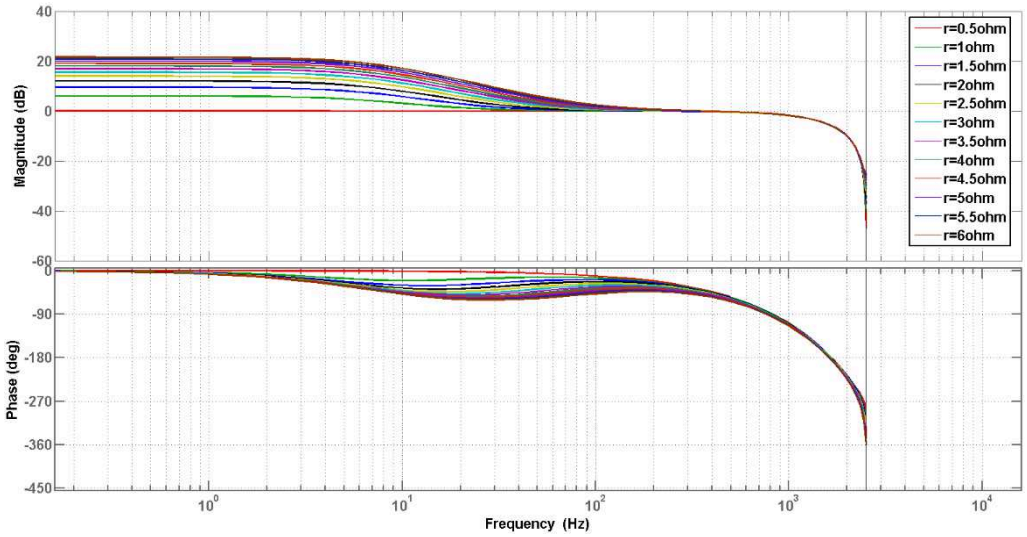


Figure 7.16 Bode diagram for proposed DBC varying r_L.

7.2 Simulation results for Dead-Beat control applied to a Solid State Transformer

This section considers the implementation of the proposed DBC on a 7-Level CHB converter, such as the one used during the UNIFLEX-PM project, to develop a three phase SST. A simulation of DBC with DCM and an active voltage balancing algorithm has been carried out for the overall 2-port UNIFLEX-PM SST converter. The devices voltage drops and on-state resistances compensation is not considered in this case being the simulation based on the equivalent model of Figure 3.7 that doesn't include any devices parasitic components. The simulation parameters are set to be equal to the UNIFLEX-PM SST converter rated parameter of Table 3.1 and the control sampling frequency has been chosen equal to the 5kHz derived from project specifications. This results in a fixed switching frequency equal to the half of the sampling frequency when using the DCM technique.

Figure 7.17 shows the active and reactive power tracking for DBC controller when power variations are considered. The DBC produces low ripple and accurate power reference tracking. A small but variable steady state error is produced on the reactive power; it can be explained considering the model discretisation error that cause an undesired additional phase shift between the supply voltage and current, such as supply voltage prediction errors. An overshoot, of one sampling interval duration, is produced on the active power on port 2; this is related with the proposed DBC derivation that does not provide the ideal response of a Dead-Beat controller, i.e. zero tracking error in one sampling interval.

Figure 7.18 shows the DC-Link voltage tracking for both controllers. During power references variations, the slow response of the PI controller affects the DC voltage tracking of the overall control system which produce a maximum DC-Link voltage variation of around 1.5% of the nominal value at time 2.2s where the active power flow is reversed. However, since there is an active DC-Link voltage balancing algorithm implemented in the modulator, the DC voltage on each capacitor of each phase is maintained balanced within 1.5% of the nominal value. Clearly it is possible to improve the performance of the DC-Link voltage controller but additional notch filters or a higher order controller may be required.

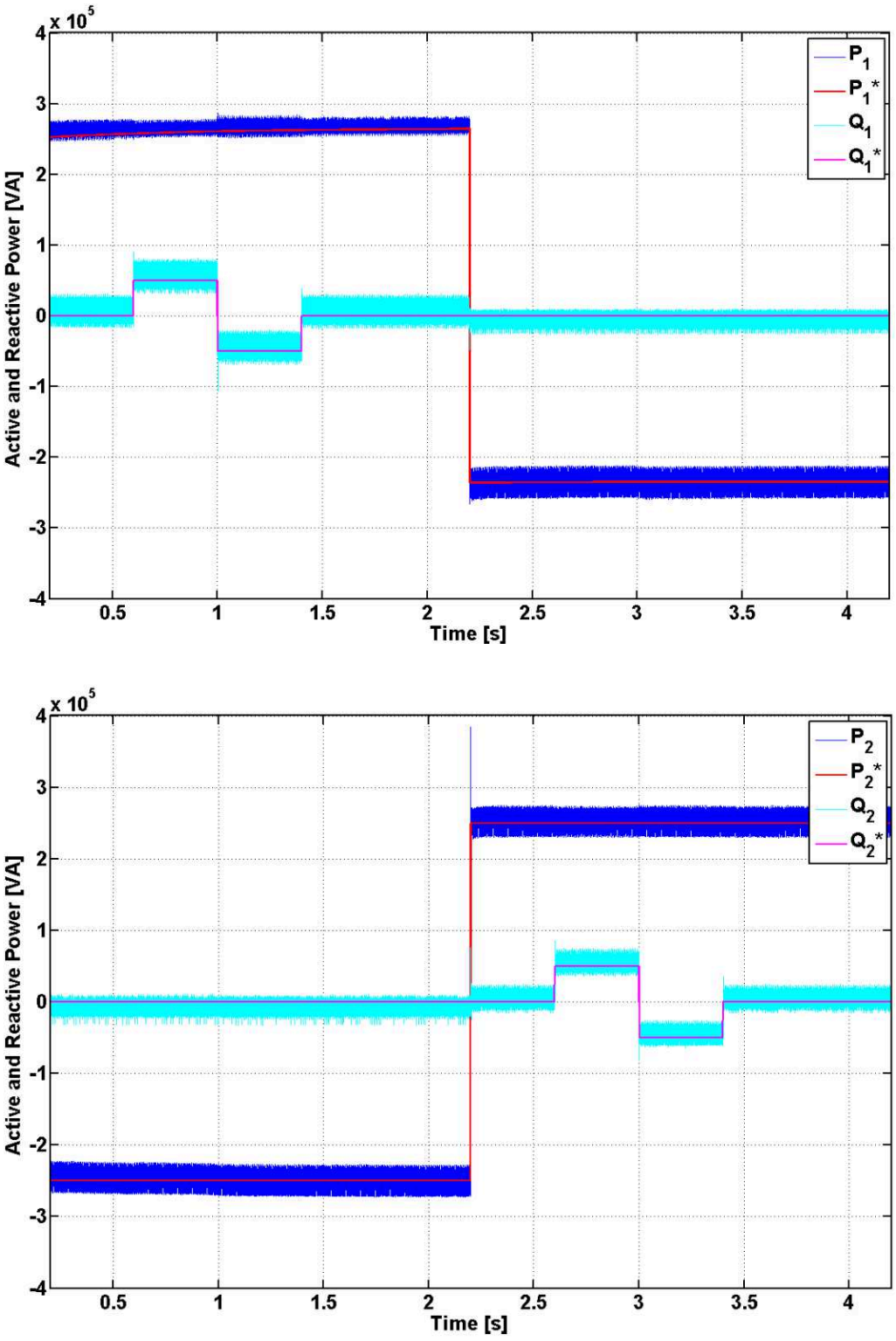


Figure 7.17 DBC simulation for UNIFLEX-PM SST converter: active and reactive power flow vs references on the two SST sides.

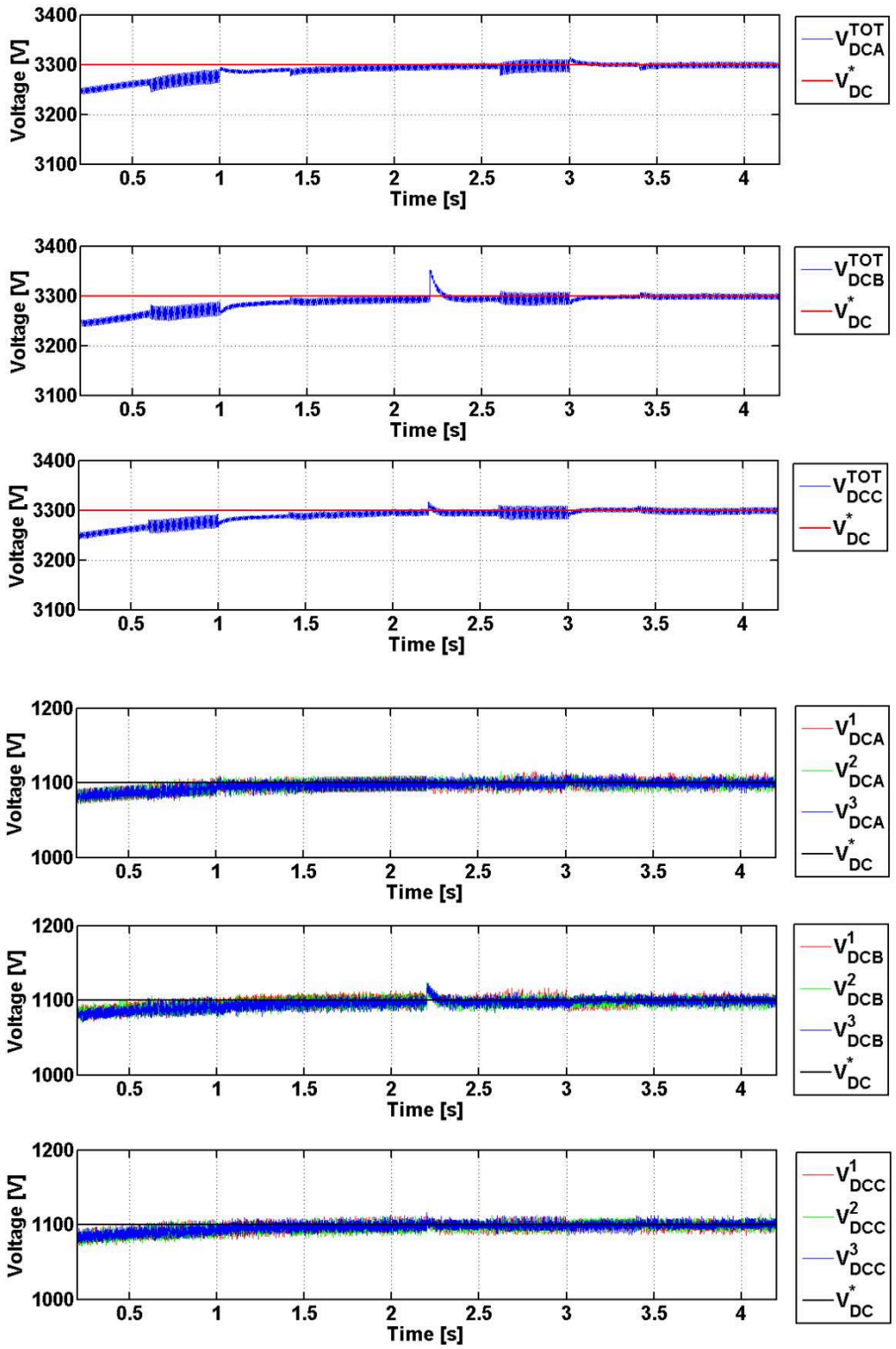


Figure 7.18 DBC simulation for UNIFLEX-PM SST converter: total DC-Link voltages on each phase vs DC-Link voltage reference and single DC-Link capacitors voltages.

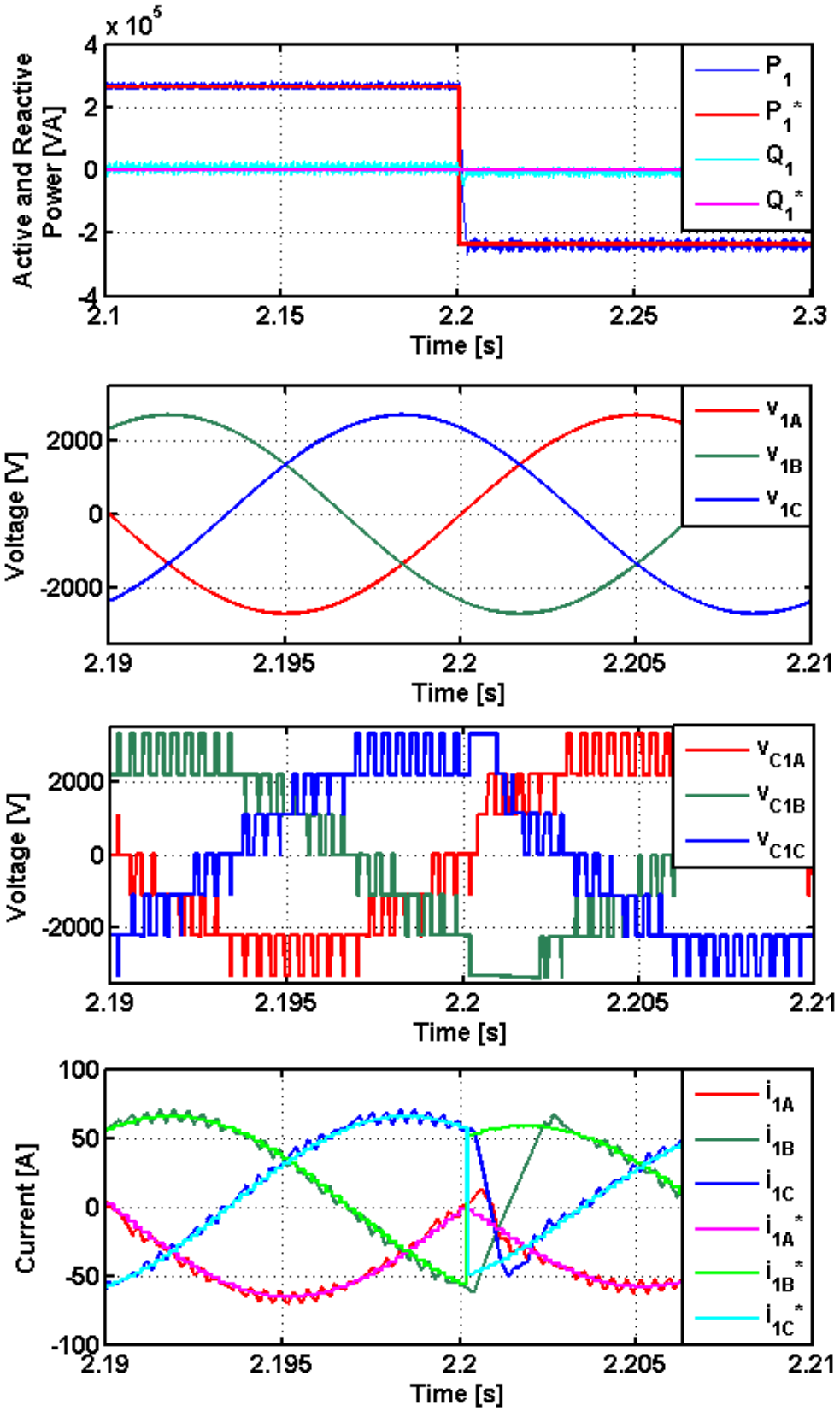


Figure 7.19 DBC simulation for UNIFLEX-PM SST converter: grid voltage, converter voltage and AC current vs current reference on the three phases of both side of the SST converter when an active power reference step from 250kW to -250kW is applied on port 1 at time2.2s.

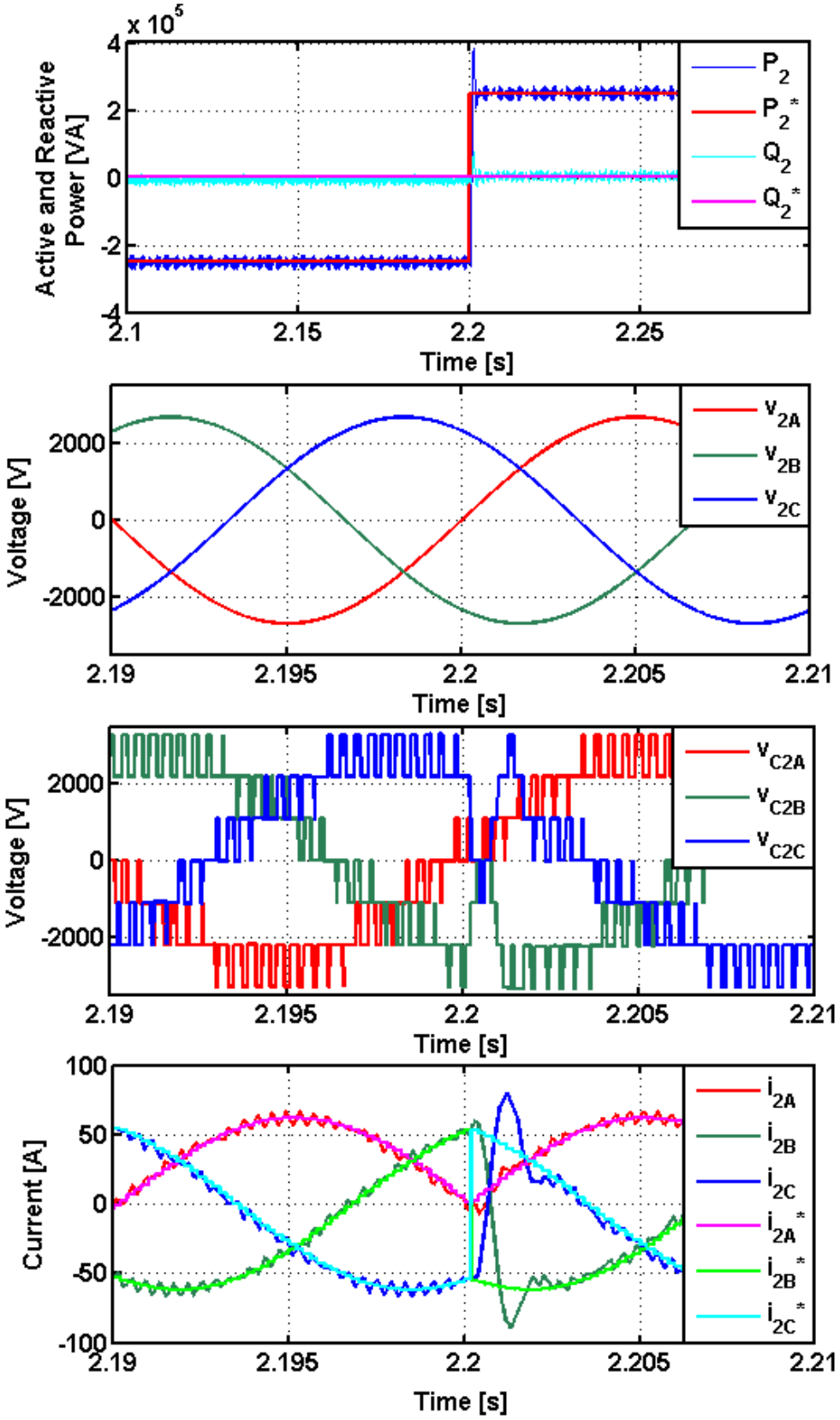


Figure 7.20 DBC simulation for UNIFLEX-PM SST converter: grid voltage, converter voltage and AC current vs current reference on the three phases of both side of the SST converter when an active power refernce step from -250kW to 250kW is applied on port 2 at time2.2s.

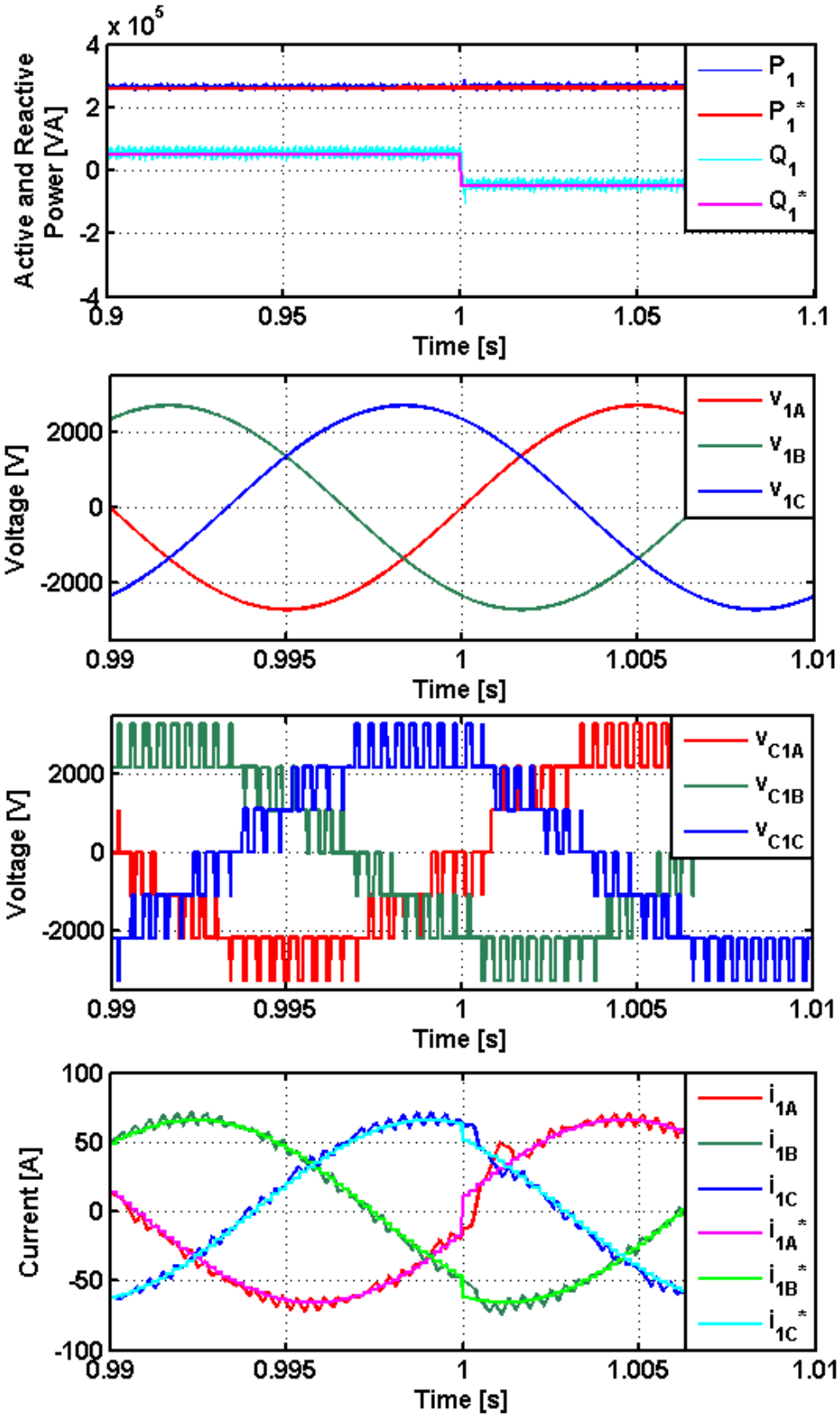


Figure 7.21 DBC simulation for UNIFLEX-PM SST converter: grid voltage, converter voltage and AC current vs current reference on the three phases of both side of the SST converter when a reactive power reference step from 50kVAR to -50kVAR is applied on port 1 at time 1s.

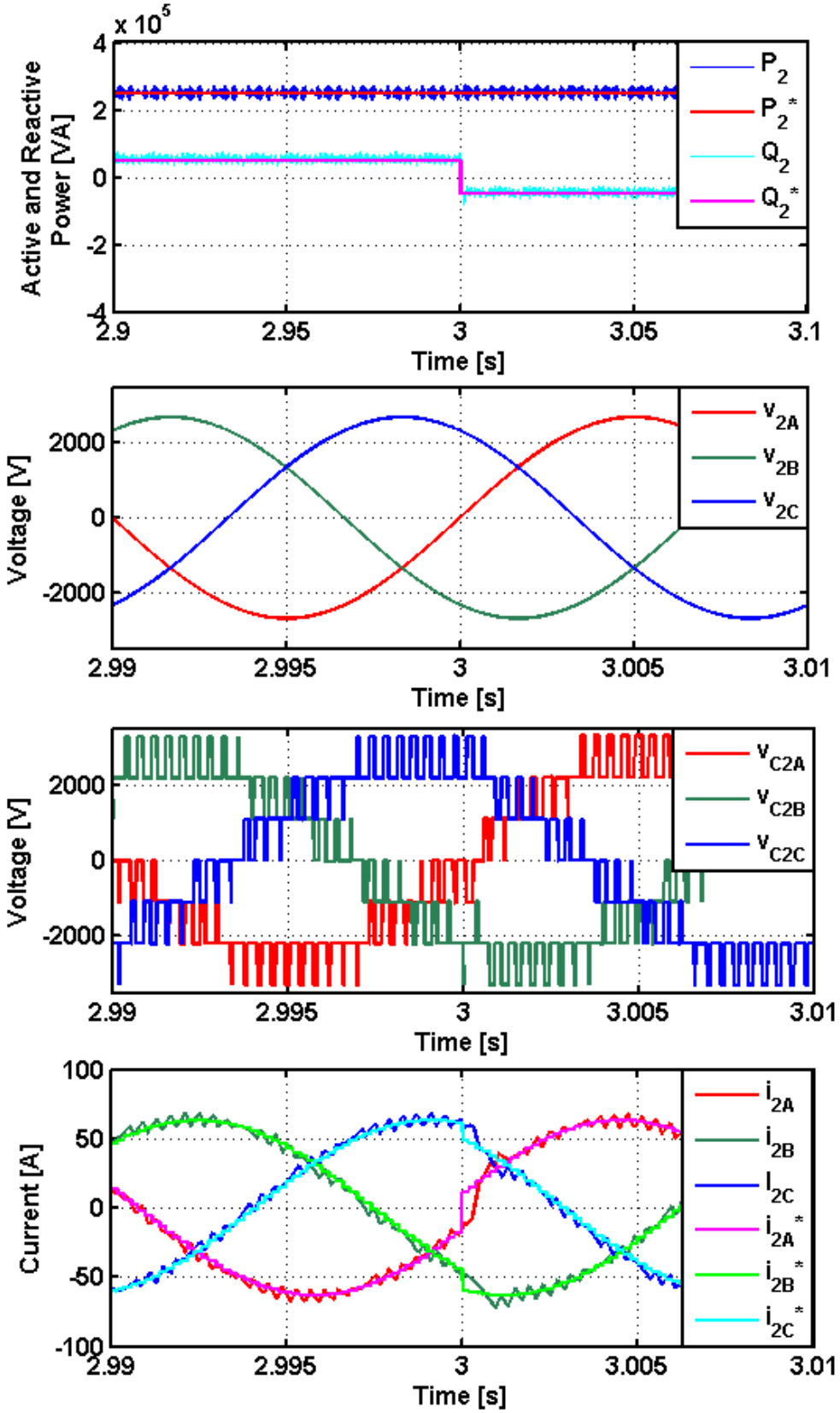


Figure 7.22 DBC simulation for UNIFLEX-PM SST converter: grid voltage, converter voltage and AC current vs current reference on the three phases of both side of the SST converter when a reactive power reference step from 50kVAR to -50kVAR is applied on port 2 at time 3s.

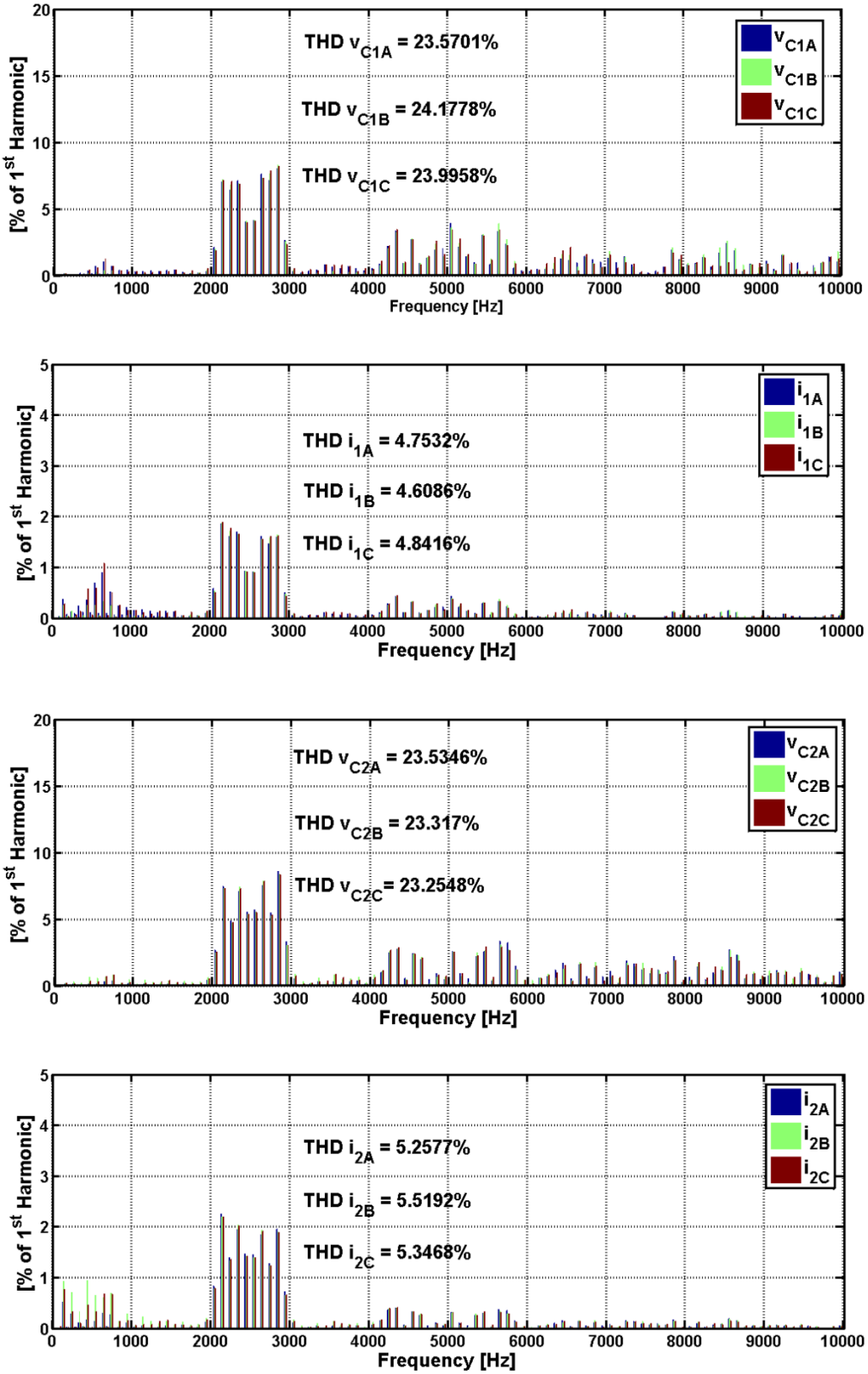


Figure 7.23 DBC simulation for UNIFLEX-PM SST converter: AC current and converter voltages harmonic content on the three phases of both sides of the SST converter.

Figure 7.19, Figure 7.20, Figure 7.21 and Figure 7.22 show the grid voltages, AC, currents and converter voltages on the three phases of both sides of the SST converter. As illustrated in Figure 7.19 and Figure 7.20, when an active power step from of 250kW is applied and the control reacts with a fast response with the only limitation given by the DC-Link voltage controller.

In Figure 7.21 and Figure 7.22 a reactive power step from 50kVAR to 50kVAR is applied and also in this case the DBC provides fast current tracking.

Figure 7.23 shows the AC currents and converter voltages harmonic content on the three phases of both the SST converter sides; it is clear that the switching frequency of DBC is equal to 2.5kHz (100 commutations per period). The harmonic content is mainly concentrated around multiple of the switching frequency, producing a THD of approximately 24% for the converter voltages and 5% for the AC currents.

7.3 Experimental results for Dead Beat Control applied to a Solid State Transformer

Experimental testing has been carried out on the two port UNIFLEX-PM SST converter considering the configuration shown in Figure 3.14. In this case port 1 is connected to the grid and port 2 is connected to a RL load. With such a configuration it is possible to validate the proposed control under non-ideal grid conditions, using the converter prototype shown in Figure 3.8. The experimental parameters are shown in Table 7.1. Results are shown only for port 1 since the control on port 2 is identical with the only exception that the DC-Link voltage control is not required and the absence of a grid connection on port 2.

Table 7.1 DBC experimental parameters.

Name	**Description**	**Value**	**Unit**
C	DC-Link capacitor	3100	[μF]
r_L	Inductor resistance	0.5	[Ω]
L	AC filter inductance	11	[mH]
R_{LOAD}	Load resistance	30	[Ω]
V_{1peak}	Rated peak value of the AC supply on port 1 (line-to-line)	212	[V]
V_{2peak}	Rated peak value of the AC supply on port 2 (line-to-line)	212	[V]
V_{DC}	Capacitor voltage	92	[V]
$f_{sw,DC/DC}$	Switching frequency of DC/DC converter	2500	[Hz]
T_s	Sample time	0.2	[ms]

In Figure 7.24, steady state results of DBC are presented for phase A, port 1. The converter voltage shows a waveform with a THD of approximately 22% while the current has a low ripple characteristic with a THD of approximately 3%. In Figure 7.25 an active power step from 0W to 3kW is considered. In order to ensure that the finite delay introduced by the DC/DC converter does not affect the DC-Link voltage control response, the active power reference is slowed down using a ramp generator, taking 0.2s to reach its target value. The generated active power is around 3.8 kW as the extra 800W are required to regulate the DC-Link voltages and compensate for DC/DC converter losses which are high at this low power level as a result of the absence of soft switching. The DC-Link voltages takes almost 1s to recover the tracking after the change in power, with a maximum error of about 18% of the nominal value. The AC currents and voltages are in phase as desired and the control shows effective current tracking.

In Figure 7.26 a reactive power step from 0VAR to -3kVAR, while an active power of 1.8kW is delivered to port 2, is considered. In this case, because reactive power is managed independently on the two side on the converter, the dynamic of the DC-Link voltage control is not affected by reactive power variations and there is no need to slow down the reactive power reference. The obtained power tracking matches the simulations results dynamic and the DC-Link voltages remain regulated and balanced at the desired value with neglectable error.

The AC voltages ad currents shown in Figure 7.25 and Figure 7.26 demonstrate that the current tracking is lost only for few milliseconds before the control recover the tracking.

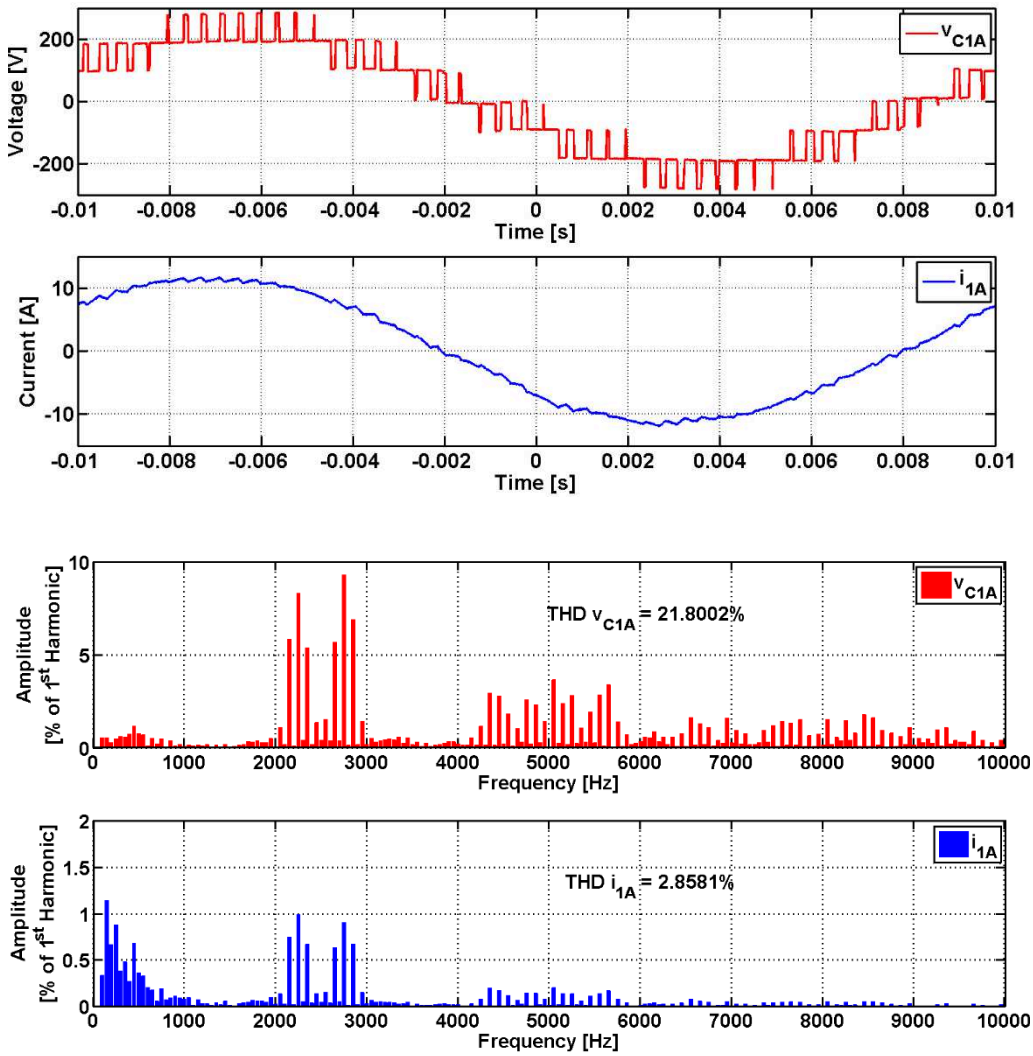


Figure 7.24 Experimental results for DBC on UNIFLEX-PM converter: steady state converter voltage and AC current on phase A, port 1.

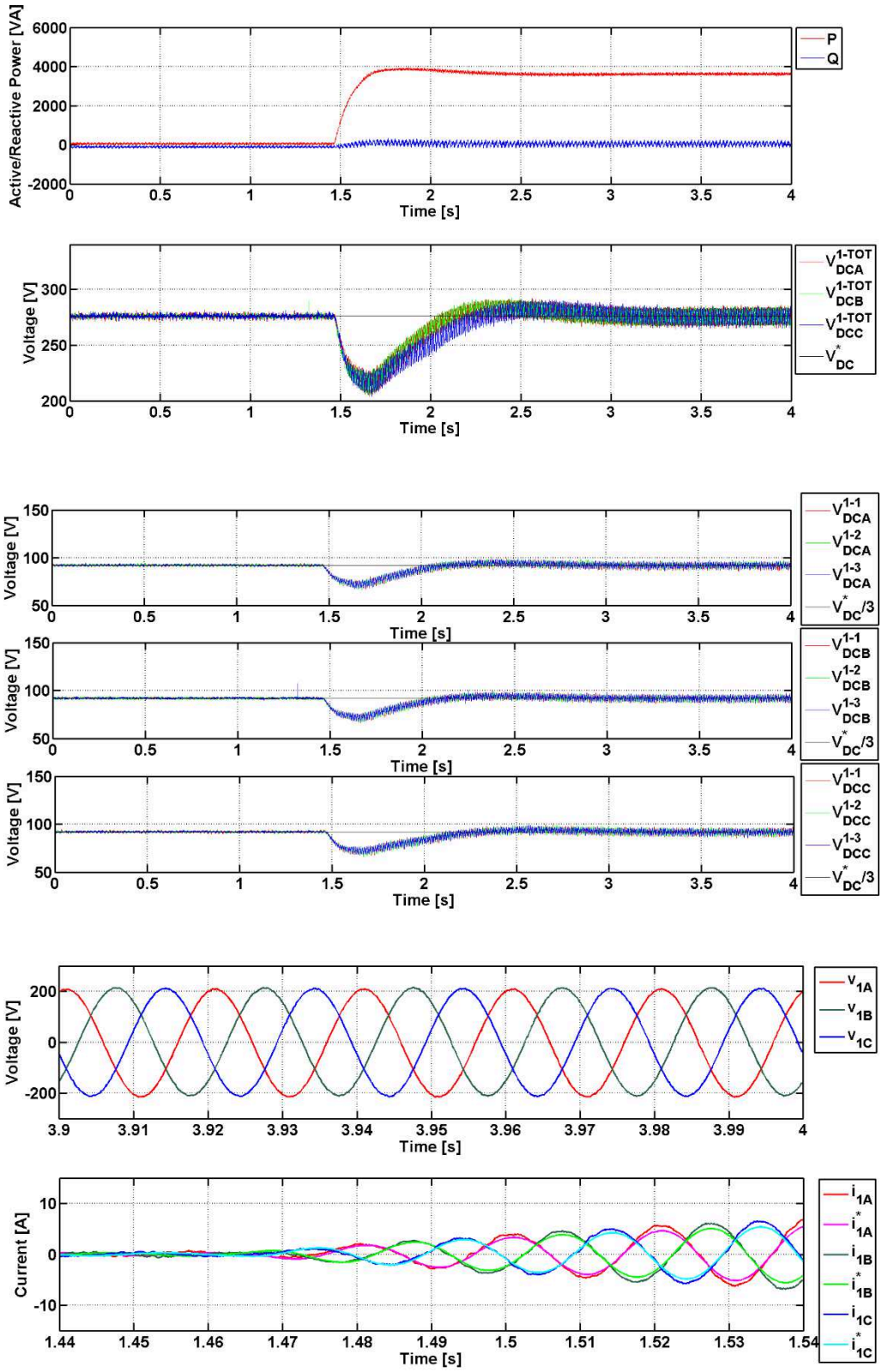


Figure 7.25 Experimental results for DBC on UNIFLEX-PM SST converter: Active and Reactive power, DC-Link voltages, grid voltages and AC currents vs current references on port 1 when an active power step from 0kW to 3kW is demanded to the SST converter at time 1.5s.

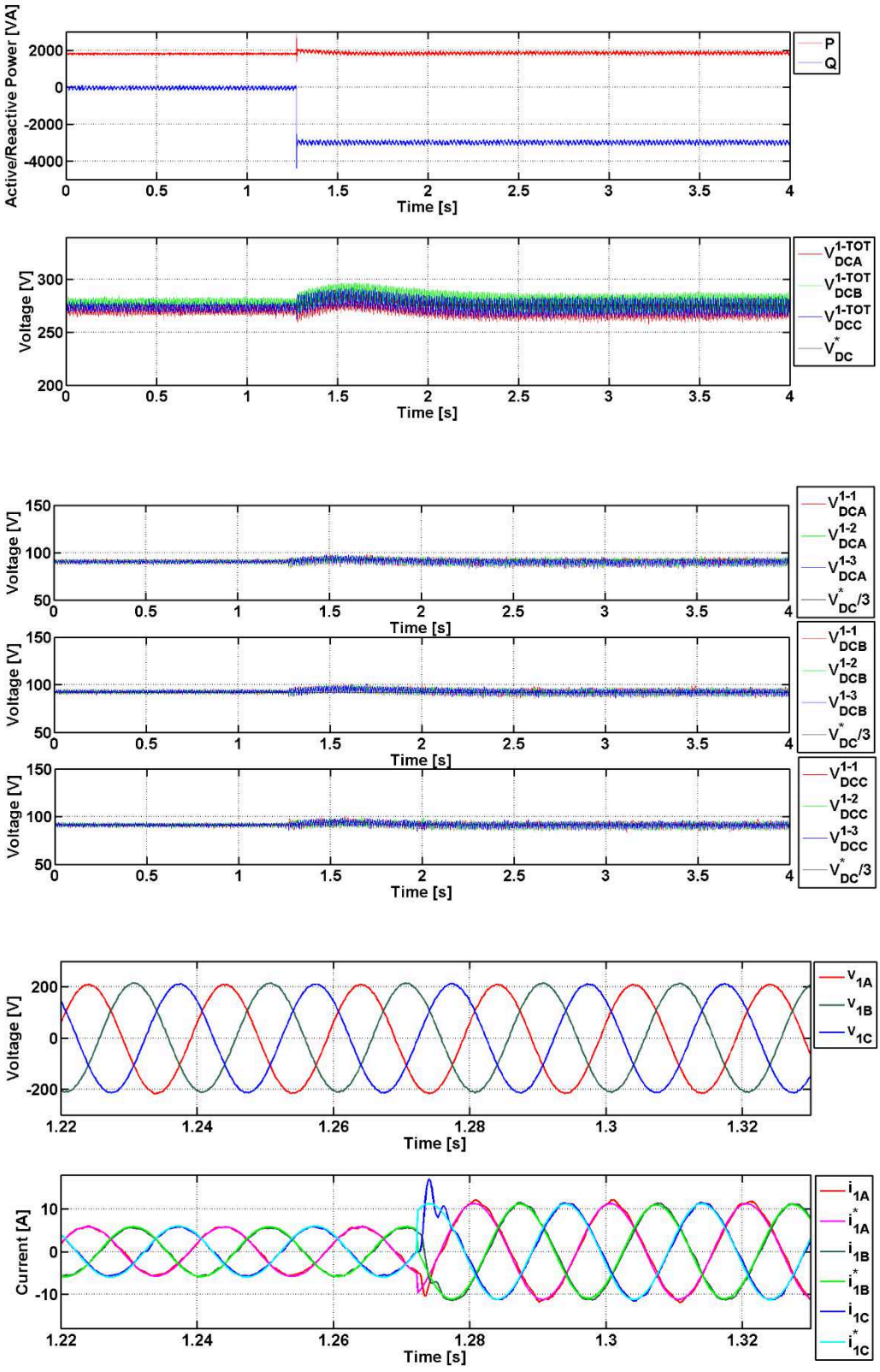


Figure 7.26 Experimental results for DBC on UNIFLEX-PM converter: active and reactive power, DC-Link voltages, grid voltages and AC currents vs current references on port 1 when a reactive power step from 0kW to -3kVAR is demanded to the SST converter at time 1.25s.

More experimental tests have been conducted under non-ideal grid conditions. During the experimental testing the power references are fixed to P^*=2500W and Q^*=0VAR and four non-ideal grid conditions are considered in Figure 7.27, Figure 7.28, Figure 7.29 and Figure 7.30, respectively for the cases of grid voltage frequency variations, phase jumps, amplitude variations and unbalances. These conditions are generated using a Chroma 61511 Programmable AC Source, rated 12 kVA.

The first test has considered a supply frequency step excursion from 50Hz to 53Hz (6% of nominal value), as shown in Figure 7.27. The DBC attempts to recover the synchronisation between AC voltage and current providing zero reactive power. However, a phase shift between AC current and voltage is produced for two supply periods before this is achieved; this behaviour can be explained considering that the supply frequency is detected dynamically using a zero-crossing detector on the filtered voltage at the output of the SOGI, introducing a delay of one supply period. The frequency error affects the current reference calculation and the voltage prediction producing an undesired transient of two supply periods.

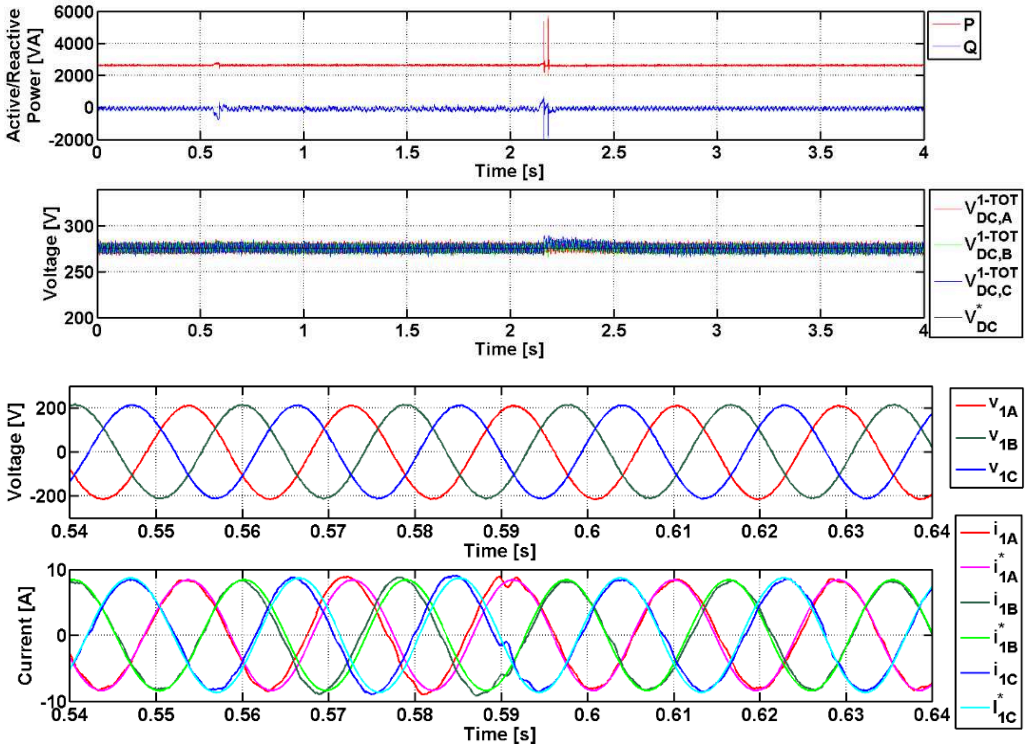


Figure 7.27 Experimental results for DBC on UNIFLEX-PM SST converter: active and reactive power, total DC-Link voltages, grid voltages and AC currents on port 1 of the SST converter when a frequency step from 50Hz to 53Hz is applied at time 0.6s and a frequency step from 53Hz to 50Hz is applied at time 2.2s.

In the second test a phase jump of 30° is considered, as shown in Figure 7.28. The DBC takes one supply cycle to recover the synchronisation between AC voltage and current. The DC-link voltage and power tracking is never lost as a result of the phase jump.

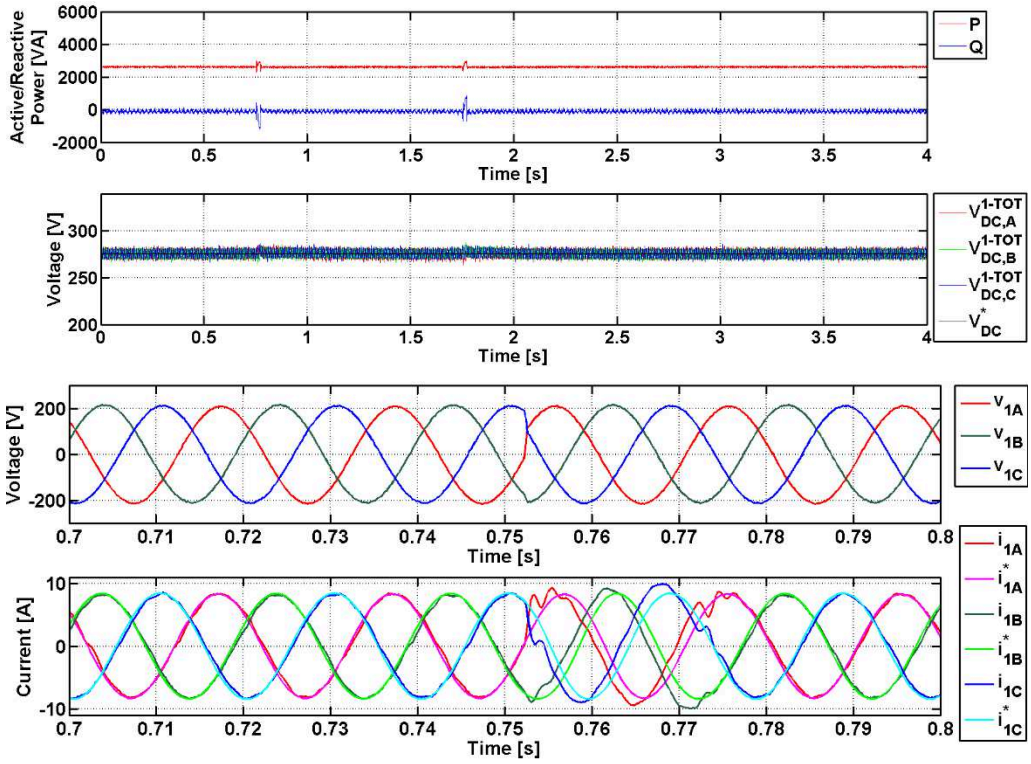


Figure 7.28 Experimental results for DBC on UNIFLEX-PM SST converter: active and reactive power, total DC-Link voltages, grid voltages and AC currents on port 1 of the SST converter when a phase jump from 0° to 30° is applied at time 0.75s and a phase jump from 30° to 0° is applied at time 1.75s.

In the third test a supply voltage amplitude excursion from 150V RMS to 130V RMS (20% of nominal value) is considered, as shown in Figure 7.29. In this case the DBC presents a slow response, in terms of DC-Link voltage and power tracking; the slow dynamic response of the PI controller affects the dynamic of the whole system.

In fact, in this case the DAB DC/DC converter is modelled as a capacitor and the same DC voltage on each converter port is considered, while, in real operation, the equalization of the DC-Link voltages is given by the DC/DC converter, introducing a delay between the two converter sides and a limitation in the response of DBC to active power step. A design optimization of the DC-Link voltage controller can improve the transient response, but a higher order controller may be required.

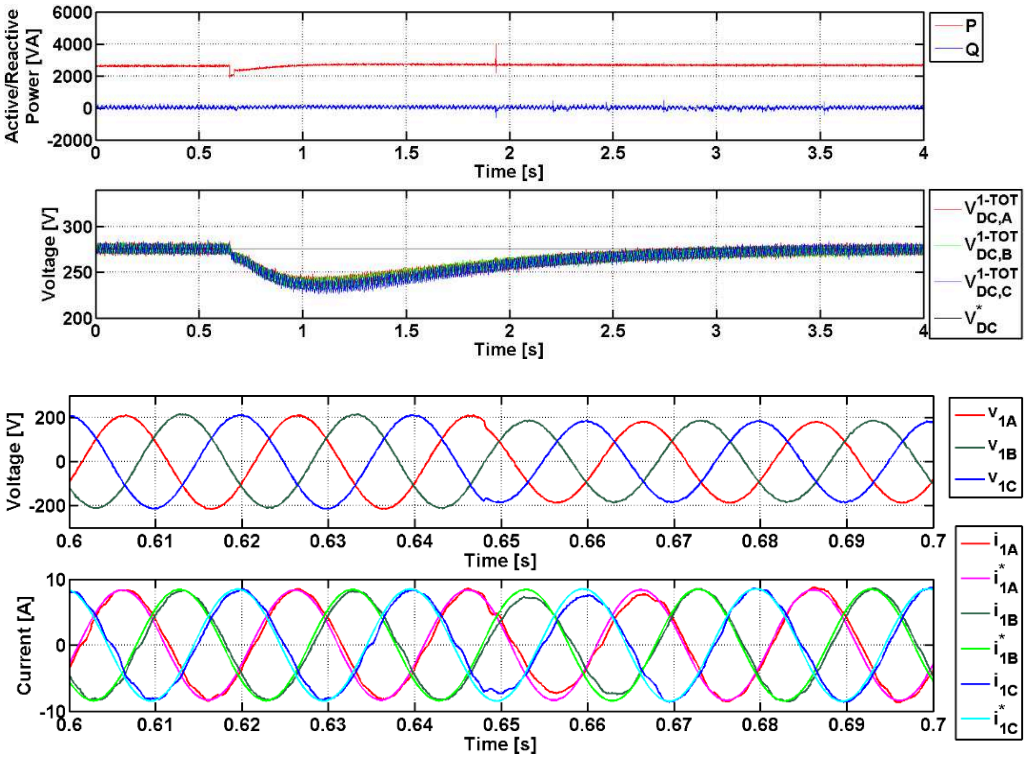


Figure 7.29 Experimental results for DBC on UNIFLEX-PM SST converter: active and reactive power, total DC-Link voltages, grid voltages and AC currents on port 1 of the SST converter when an amplitude step from 150V RMS to 130V RMS is applied at time 0.6s and an amplitude step from 130V RMS to 150V RMS is applied at time 1.9s.

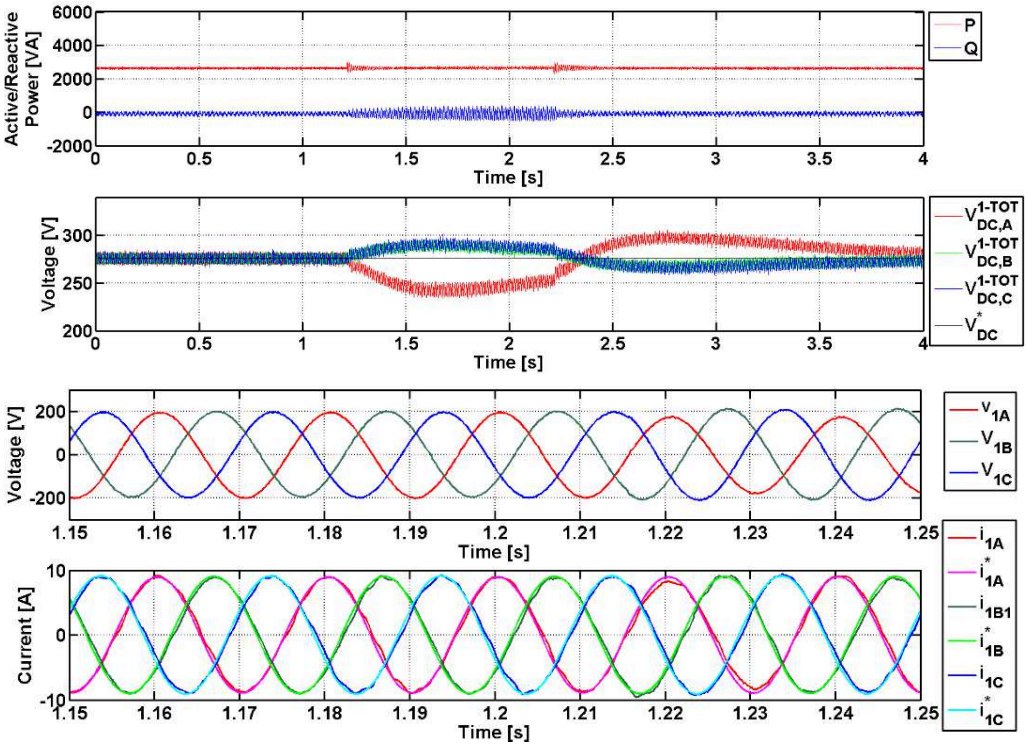
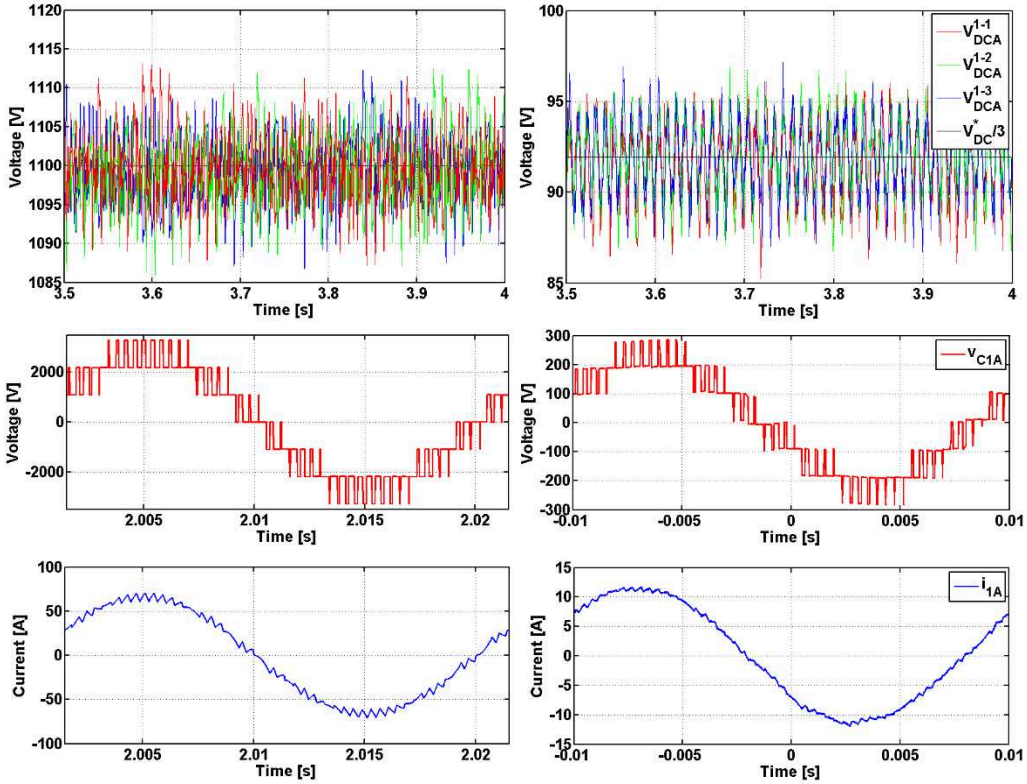


Figure 7.30 Experimental results for DBC on UNIFLEX-PM SST converter: active and reactive power, total DC-Link voltages, grid voltages and AC currents on port 1 of the SST converter when a voltage unbalance of 10% is applied.

Finally, a supply voltage unbalance, characterised by positive to negative ratio of 10% is considered in Figure 7.30. In this case the slow dynamic response of the DC-Link PI controller affects the control and the DC-Link voltage tracking is lost for almost two seconds. Moreover, in this case also the DC-Link voltage balance between the three phases is affected. As a four wire, three phase system is accounted, the produced currents are balanced even in presence of unbalanced voltages.

7.4 Simulation and experimental results comparison

In Figure 7.31 the waveform obtained using the DBC technique described in this chapter, experimentally on the UNIFLEX-PM demonstrator and in simulation, are compared.



(a) Simulation **(b) Experimental**

Figure 7.31 Comparison between experimental and simulation results for Dead-Beat Control: DC-Link voltages, Converter voltage, AC voltage and current.

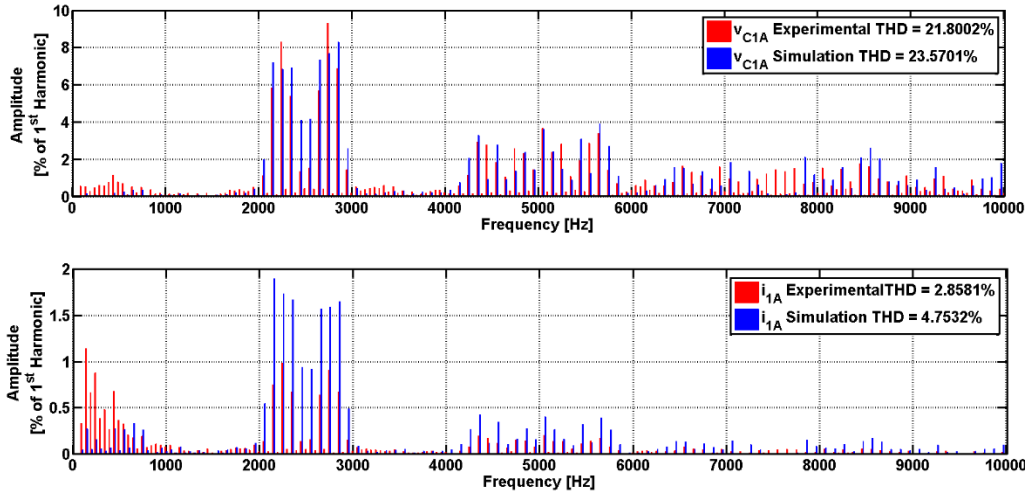


Figure 7.32 Comparison between experimental and simulation results for Dead-Beat Control: Converter voltage and AC current harmonic content.

As it can be noted, DC-Link voltages, converter voltage and AC current on phase A, port 1 of the UNIFLEX-PM demonstrator present similar waveforms, with the only difference in the different operating point between simulation and experimental tests and the absence of a grid connection on port 2.

However the different operative points affects the amplitude of the AC current and, thus the filtering capability of the line inductance, considered of the same value in both simulation and experimental tests.

This results in the harmonic contents of Figure 7.32, where the converter voltage presents a similar spectrum in both cases with additional low frequency harmonics produced by the real converter and mainly related with noise measurements and Dead-Times. On the other hand the AC current spectrum presents a visible difference between simulation and experimental tests. In fact even if low frequency harmonics are provided by the real converter, the AC current THD results lower for the experimental tests as a consequence of the different operative point considered in simulation and experimental testing.

7.5 Chapter summary

In this chapter a DBC current control with PI DC-Link voltage control is presented. In particular, the traditional DBC derivation is described for the proposed system and a modification to the traditional DBC derivation, based on higher orders derivative discretization is proposed to increase the control stability.

A frequency analysis is carried out for both controllers, showing that the higher order derivative discretization results in an attenuation of the higher order overall system harmonics, close to the Nyquist frequency and, as a consequence, in an improved system stability to model parameters variations, without resulting in a significant variation of the system transient response.

Simulation and experimental results has been carried out, considering the UNIFLEX-PM demonstrator SST topology for the improved DBC method with the modified DCM technique described in Chapter 6; results shows that the control is able to operate effectively under several operating conditions providing low THD waveforms, having its only limitation in the tuning of the DC-Link voltage controller.

Chapter 8
Model Predictive Control for a 2 port Solid State Transformer

Model Predictive Control (MPC) boast many potential advantages such as: fast dynamic response, easy inclusion of nonlinearities and other system constraints, the ability to incorporate nested control loops in only one loop as well as the flexibility to include other system requirements in the controller.

MPC may consider a continuous control set; in this case the implementation requires the inclusion of a suitable modulation in the control system. However, taking into account the finite number of output states of a converter, the finite control set MPC is considered because of its robustness to system disturbances and the absence of a modulator.

This chapter derives an MPC algorithm for use in CHB converters from first principles. Simulation results from Matlab/Simulink and experimental work from the UNIFLEX-PM demonstrator are used to validate the approaches presented.

8.1 Model Predictive Control description

Model Predictive Control (MPC) is based, like the Dead-Beat Control, on the prediction of the system response to a change in control variables in order to achieve a minimum error in the next one, two or more sampling periods depending on the prediction horizon that has been selected for the application [177]–[180]. In fact, while the control horizon is usually restricted to one or two sampling periods in order to not increase excessively the control computational weight and ensure fast transient response, the prediction horizon may be extended to improve the control stability as demonstrated in [178], [180]. The MPC output is a discrete set of values that can be directly applied to command the converter and it is chosen by minimising a cost function which considers the error between the current and the desired reference.

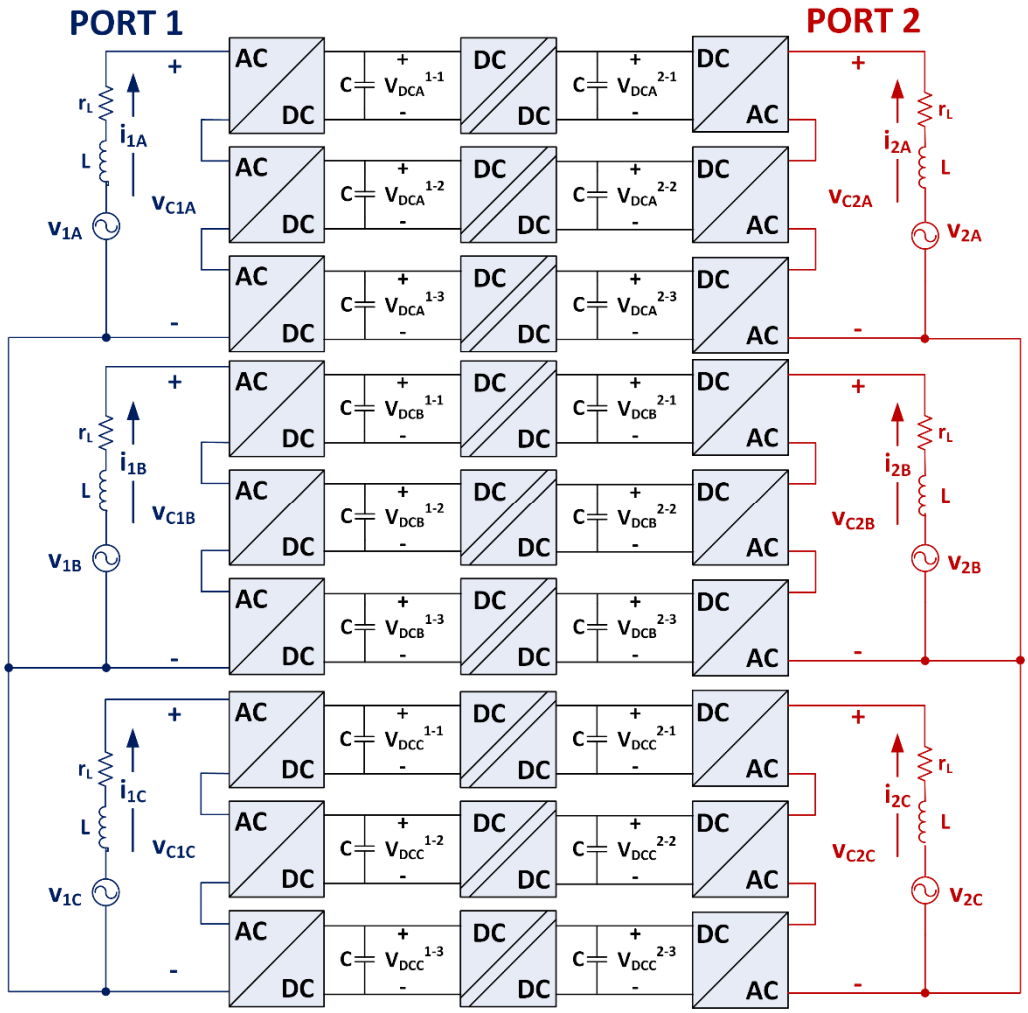


Figure 8.1 UNIFLEX-PM demonstrator two ports converter structure.

In this chapter the Model Predictive current Control is described in detail highlighting the modification applied to the classic control algorithm to improve the output waveform quality and control stability. The proposed control is then validated through simulations and experimental testing on the 7-level CHB SST structure of Figure 8.1.

8.1.1 Classic control derivation

The MPC current control [176], [181], whose working principle is shown in the flowchart of Figure 8.2, is derived for the converter model of Figure 8.3, which considers phase A, port 1 of the SST model of Figure 8.1 and it is described by equations (7.1)-(7.4).

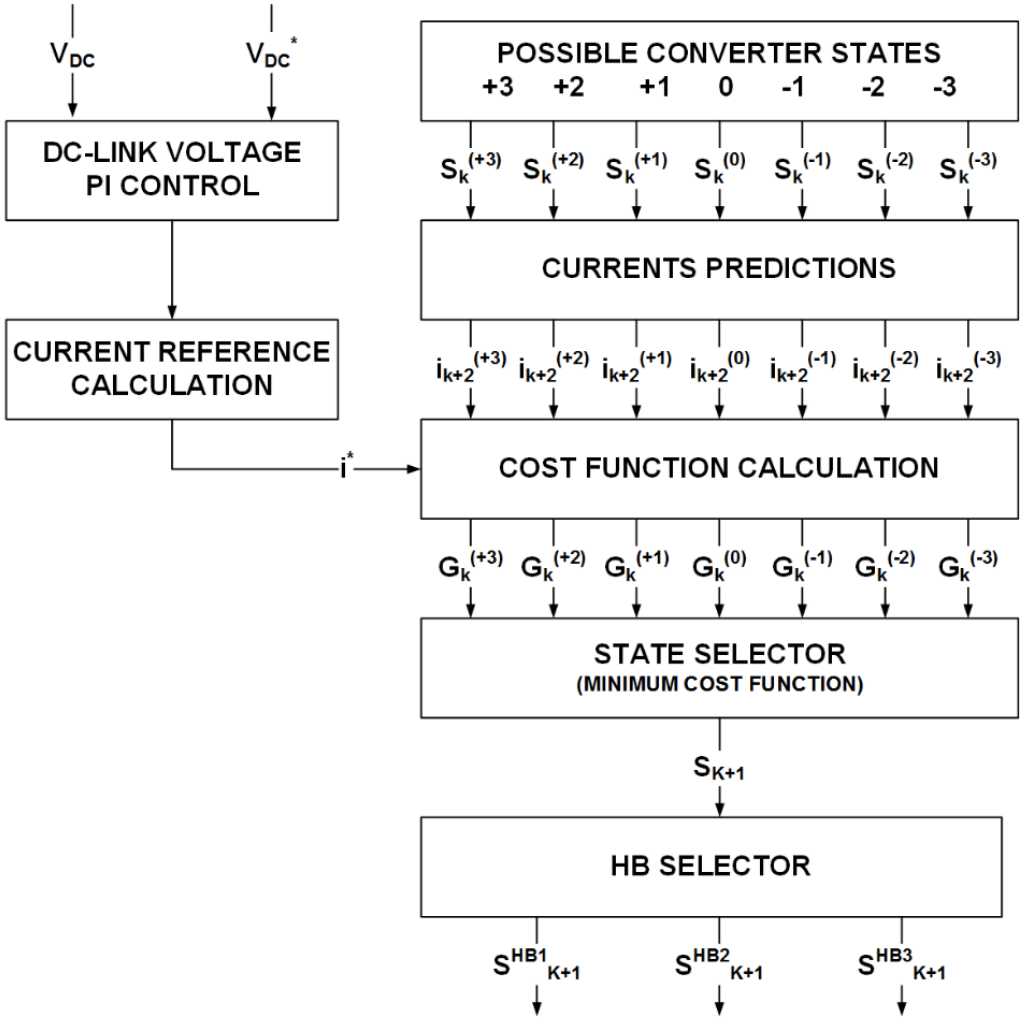


Figure 8.2 Classic MPC working principle flowchart.

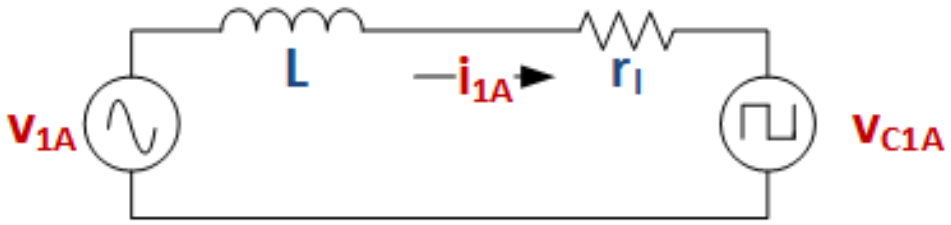


Figure 8.3 Equivalent AC circuit of the UNIFLEX-PM demonstrator, phase A, port 1.

In particular, the discretised model of equation (7.4) is used to obtain the current prediction at the sampling instants $t_k + Ts$ and $t_k + 2T_s$, with the discrete variable k, expressed by equations (8.1) and (8.2), where v_{1A} is the AC supply voltage, v_{C1A} is the voltage applied from the CHB and i_{1A} is the AC current filtered by the inductor L with a winding resistance r_L. The time instant where the model is discretised take in account the real system limitations, as the intrinsic delay of one sampling interval, T_s, introduced by the digital implementation. In this case in order to obtain a two-step ahead current prediction two single step prediction are used: the prediction of (8.1) is used to compensate the delay introduced by the DSP while (8.2) represents the control actuation that has to be computed at the time instant t_k.

$$i_{1A}(t_k + T_s) = \left[1 + r_L \frac{T_s}{L}\right] i_{1A}(t_k) + \frac{T_s}{L}[v_{1A}(t_k) - v_{C1A}(t_k)] \tag{8.1}$$

$$i_{1A}(t_k + 2T_s) = \left[1 + r_L \frac{T_s}{L}\right] i_{1A}(t_k + T_s) + \frac{T_s}{L}[v_{1A}(t_k + T_s) - v_{C1A}(t_k + T_s)] \tag{8.2}$$

In (8.2) $v_{c1A}(t_k+T_s)$ represent the converter voltage which will be applied during the next sampling interval and is clearly related to the selected converter state. In fact, assuming that the DC-Link voltages are balanced and regulated at the desired reference V_{DC}^* the converter voltage can be expressed as follows, where s_{1A} represents the total CHB state on phase A, expressed in a range between -3 and 3.

$$v_{C1A}(t_k + T_s) = s_{1A}(t_k + T_s)\frac{V_{DC}^*}{3} \tag{8.3}$$

Between all the possible converter states the one that minimises a defined cost function is applied during the next sampling interval. In the case of current control, the selected cost function considers the absolute value of the current error, shown in equation (8.4).

$$G_{1A} = |i_{1A}(t_k + 2T_s) - i_{1A}^*(t_k + 2T_s)| \tag{8.4}$$

Even though the classic derivation of model predictive current control presents a fast response and an easier implementation several disadvantages can be highlighted:

- A DC-Link voltage control (PI) is required which could instead be implemented as part of the MPC cost function.
- There is no limitation on the number of devices that can be allowed to switch in the same switching interval potentially resulting in increased switching loss when compared with more conservative solutions such as the proposed DBC, where only one leg of one HB is allowed to switch during every sampling interval.
- The same converter states can be applied for more sampling intervals, resulting in a variable converter switching frequency.
- Since a converter state applied for the whole sampling interval, is not possible to achieve ideally zero error at the next sampling interval as is the case for DBC, increasing current harmonic distortions.
- The control inherently allows simultaneous switching and waveform, as shown in Figure 8.4, resulting in a peak current sampling. Moreover particular care has to be taken to avoid the noise produced switching the converter affects the sampled measurements.

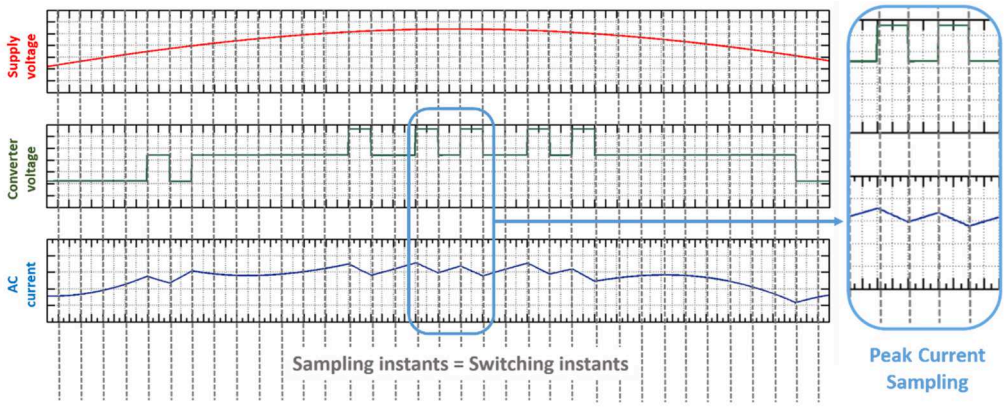


Figure 8.4 Classic MPC switching and sampling instants.

In order to overcome these disadvantages the MPC control has been modified in order to improve the control performances.

8.1.2 Proposed Model Predictive Control

Because the control directly applies one switching state for the whole sampling interval, it is necessary to acquire the measurements in the centre of the sampling period in order to obtain the average supply current as shown in Figure 8.5.

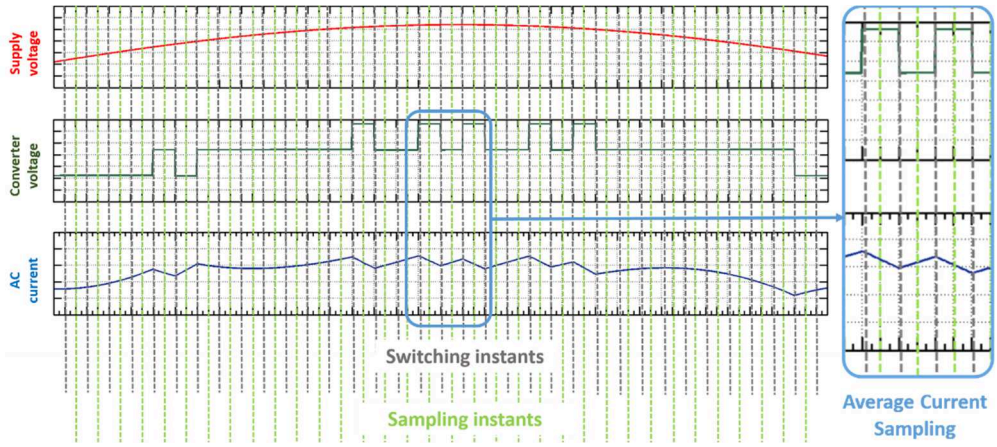


Figure 8.5 Proposed MPC switching and sampling instants.

On this basis the control is structured as follows [176]:

- The current reference is calculated from active and reactive power reference adding a term based the variation of energy in the DC-Link voltage capacitance, avoiding the use of PI controllers.
- Current predictions are calculated for the average supply current and a current cost function is defined using the absolute value of the current tracking error at the time instant $t_k + 2T_s$.
- A dynamic DC-Link voltage reference with a user defined time horizon is calculated.
- DC-Link voltage predictions are calculated and a cost function is defined using the absolute value of the DC-Link voltage error at the time instant $t_k + 2T_s$.
- Only one leg of one HB is allowed to switch at each sampling instants.
- A "HB selector" is implemented to determine which HB to switch in order to maintain balanced the DC-Link voltages and/or distribute the commutation amongst the CHB devices.

The obtained control, whose working principle is shown in the flowchart of Figure 8.6, is described in details in the following sections.

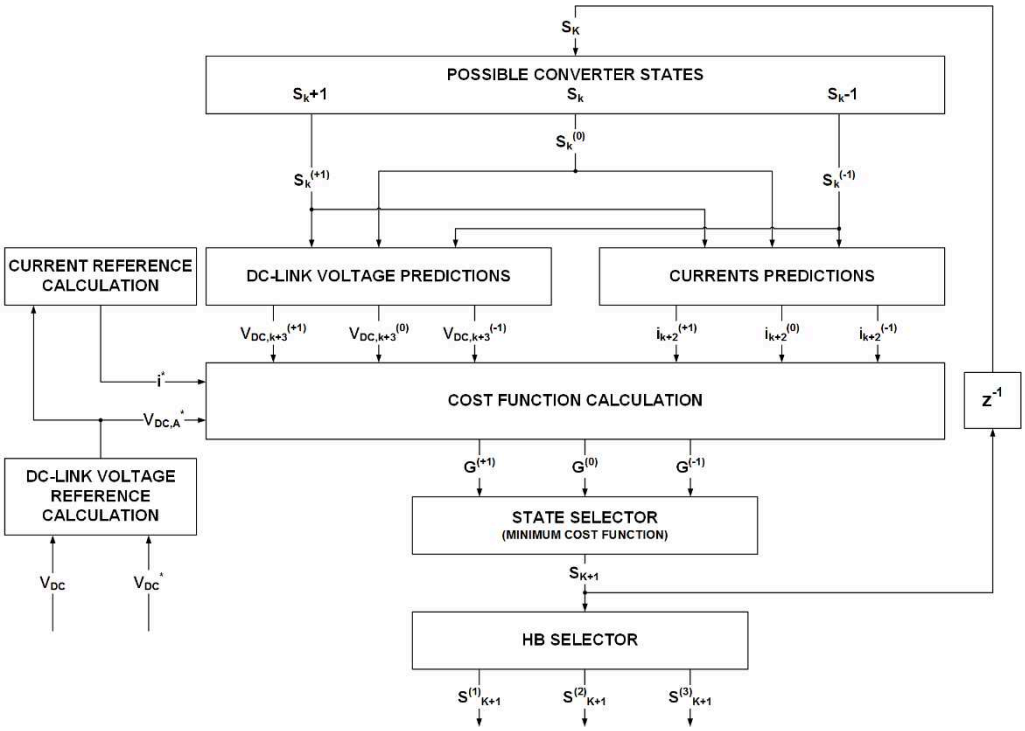


Figure 8.6 Proposed MPC working principle flowchart.

8.1.2.1 Current Model Predictive Control

Starting from (8.1), the model is discretised around the sampling instants t_k, obtaining, for the model of Figure 8.3 the following expression.

$$i_{1A}(t_k + T_s) = \left[1 + r_L \frac{T_s}{L}\right] i_{1A}(t_k) + \frac{T_s}{L}[v_{1A}(t_k) - v_{C1A}(t_k)] \tag{8.5}$$

Since the average current is held for one sampling interval it is possible to impose the following expression for the control.

$$i_{1A}(t_k) = i_{1A}(t_k - 0.5T_s) \tag{8.6}$$

In this case the first prediction is then obtained on the basis that the current at the previous sampling instant is:

$$i_{1A}(t_k + T_s) = \left[1 + r_L \frac{T_s}{L}\right] i_{1A}(t_k - 0.5T_s) + \frac{T_s}{L}[v_{1A}(t_k) - v_{C1A}(t_k)] \tag{8.7}$$

In the same way the current prediction at the sampling instant t_k+T_s is calculated.

$$i_{1A}(t_k + 2T_s) = \left[1 + r_L \frac{T_s}{L}\right] i_{1A}(t_k + T_s) + \frac{T_s}{L}[v_{1A}(t_k + T_s) - v_{C1A}(t_k + T_s)] \tag{8.8}$$

The current cost function defined in (8.4) is then calculated.

8.1.2.2 DC-Link voltage Model Predictive Control

For the current reference calculation and DC-Link voltage prediction the dynamic of the DC side of the converter has to be modelled.

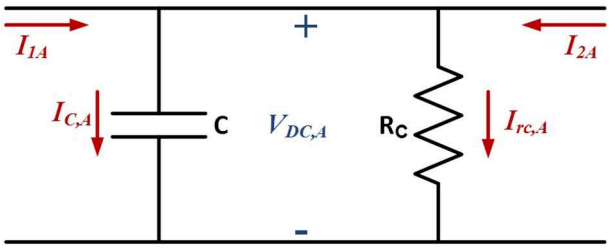


Figure 8.7 DC equivalent circuit for phase A.

The dynamics of the isolated DC-DC converter can be neglected, considering that it has a completely independent control with the aim of maintaining equal voltages on its two sides. The current flowing in one phase of the converter is the same for the three H-Bridge belonging to the same phase and, considering the power absorption balanced between the H-Bridges on the same phase, the equivalent model of Figure 8.7 can be considered for phase A. The current equation that describes the circuit of Figure 8.7 is:

$$I_{1A}(t) + I_{2A}(t) = I_{C,A}(t) + I_{Rc,A}(t) \tag{8.9}$$

Considering that R_c represents the losses in the capacitors and in the DC-DC converter, its value is unknown and cannot be modelled. For control purpose $R_c = \infty$ is assumed, obtaining the following equations.

$$I_{1A}(t) + I_{2A}(t) = \frac{v_{C1A}(t)i_{1A}(t) + v_{C2A}(t)i_{2A}(t)}{V_{DC,A}} \tag{8.10}$$

$$I_{C,A}(t) = C\frac{dV_{DCA}(t)}{dt} \tag{8.11}$$

To decouple the DC-Link voltage control from the secondary side control a dynamic approximation is needed. In particular, if the power needed to regulate the DC-link voltage is smaller compared to the desired power flow through the back-to-back converter, it is possible to assume, for balanced AC loads:

$$v_{C2A}(t)i_{2A}(t) = \frac{P_2(t)}{3} \cong -\frac{{P_1}^*(t)}{3} = -v_{C1A}(t){i_{1A}}^*(t) \tag{8.12}$$

Thus, the following approximated model of the DC side of the converter is obtained.

$$C\frac{dV_{DCA}(t)}{dt} = \frac{v_{C1A}(t)}{V_{DCA}(t)}[i_{1A}(t) - {i_{1A}}^*(t)] \tag{8.13}$$

By integrating equation (8.13) between t_k and $t_k + T_s$ the following equations are obtained.

$$C\int_{V_{DC,A}(t_k)}^{V_{DC,A}(t_k+T_s)} dV_{DCA}(t) = \int_{t_k}^{t_k+T_s} \frac{v_{C1A}(t)}{V_{DCA}(t)}[i_{1A}(t) - {i_{1A}}^*(t)]\,dt \tag{8.14}$$

$$V_{DC,A}(t_k + T_s) - V_{DC,A}(t_k) = \frac{1}{C}\int_{t_k}^{t_k+T_s} \frac{v_{C1A}(t)}{V_{DCA}(t)}[i_{1A}(t) - {i_{1A}}^*(t)]\,dt \tag{8.15}$$

The DC-Link voltages are sampled at the same time instant as the currents in order to maintain synchronization between the voltage control and the current control. In order to solve the integral in (8.15) the average value during one sampling interval is considered instead of the instantaneous values obtaining the following approximated expression.

$$\int_{t_k}^{t_k+T_s} \frac{v_{C1A}(t)}{V_{DCA}(t)}[i_{1A}(t) - {i_{1A}}^*(t)]\,dt \cong T_s\frac{{v_{C1A}}^{avg}(t_k)}{{V_{DCA}}^{avg}(t_k)}\left[{i_{1A}}^{avg}(t_k) - {i_{1A}}^{*avg}(t_k)\right] \tag{8.16}$$

Assuming that DC-Link voltage variations are sufficiently small during one sampling interval, the average value of DC-Link voltage is considered equal to its value at the instant t_k.

$${V_{DCA}}^{avg}(t_k) \cong V_{DCA}(t_k) \tag{8.17}$$

As MPC provides just one converter voltage state to be applied for the whole sampling interval, the converter voltage average value is equal to the selected voltage vector at the time instant t_k. On the other hand the average current applied in one sampling interval is equal to the current sampled in the middle of the sampling interval.

$${v_{C1A}}^{avg}(t_k) = v_{C1A}(t_k) \tag{8.18}$$

$${i_{1A}}^{avg}(t_k) = i_{1A}(t_k + 0.5T_s) \tag{8.19}$$

$${i_{1A}}^{*avg}(t_k) = {i_{1A}}^*(t_k + 0.5T_s) \tag{8.20}$$

Substituting (8.16)-(8.20) in (8.15) the DC-Link voltage prediction is obtained. A two-step prediction is required. The first prediction compensates the one-step delay introduced by the sampling.

$$V_{DCA}(t_k + T_s) = V_{DCA}(t_k) + \frac{T_s}{C}\frac{v_{C1\mathrm{A}}(t_k)}{V_{DCA}(t_k)}[i_{1\mathrm{A}}(t_k + 0.5T_s) - {i_{1A}}^*(t_k + 0.5T_s)] \quad (8.21)$$

Considering that the control is executed with a half-step delay with respect to the sampling instants, it is possible to make the following approximation.

$$i_{1A}(t_k + 0.5T_s) = i_{1A}(t_k + T_s) \quad (8.22)$$

Combining equations (8.22) with equation (8.21) and iterating the results, the following expressions are obtained.

$$V_{DCA}(t_k + T_s) = V_{DCA}(t_k) + \frac{T_s}{C}\frac{v_{C1\mathrm{A}}(t_k)}{V_{DC,A}(t_k)}[i_{1\mathrm{A}}(t_k + T_s) - {i_{1A}}^*(t_k + T_s)] \quad (8.23)$$

$$V_{DCA}(t_k + 2T_s) = V_{DCA}(t_k + T_s) + \frac{T_s}{C}\frac{v_{C1\mathrm{A}}(t_k + T_s)}{V_{DCA}(t_k + T_s)}[i_{1\mathrm{A}}(t_k + 2T_s) - {i_{1A}}^*(t_k + 2T_s)] \quad (8.24)$$

Moreover, assuming the DC-Link voltage is well regulated by the control, it is possible to make another approximation on the converter voltage, using the following relation between the converter state and the produced converter voltage.

$$s_{1A}(t_k) = \frac{v_{C1\mathrm{A}}(t_k)}{V_{DCA}(t_k)} \quad (8.25)$$

Applying (8.25) to (8.23)-(8.24) the final expressions for the DC-Link voltage predictions are obtained.

$$V_{DCA}(t_k + T_s) = V_{DCA}(t_k) + \frac{T_s}{C}s_{1A}(t_k)[i_{1\mathrm{A}}(t_k + T_s) - {i_{1A}}^*(t_k + T_s)] \quad (8.26)$$

$$V_{DCA}(t_k + 2T_s) = V_{DCA}(t_k + T_s) + \frac{T_s}{C}s_{1A}(t_k + T_s)[i_{1\mathrm{A}}(t_k + 2T_s) - {i_{1A}}^*(t_k + 2T_s)] \quad (8.27)$$

The cost function is then defined also for the DC-Link voltage as it follows.

$$G_{V1A} = \left|V_{DC,A}(t_k + 2T_s) - {V_{DC,A}}^*(t_k)\right| \quad (8.28)$$

The calculation of current and DC-Link voltage references is described in the following section.

8.1.2.3 Current and DC-Link voltage references calculation

On the basis of the DC model of Figure 8.7, the current reference value considers the variation of energy in the capacitors, and aims to provide the necessary amount of power flow through the converter to regulate the DC-Link voltage at the desired value. Considering balanced power between the phases, the following equation is obtained.

$$\frac{P_1(t)}{3} + \frac{P_2(t)}{3} = \frac{1}{2} C \frac{dV_{DCA}(t)^2}{dt} \tag{8.29}$$

In (8.29) P_1 is set to be equal to desired active power reference P_1^* plus a variation of power necessary to maintain the capacitor charged at the desired DC-Link voltage, while P_2 is set to be equal to the desired active power reference P_2^*.

$$\frac{P_1(t)}{3} = \frac{P_1^*}{3} + \frac{dP_{DCA}(t)}{dt} \tag{8.30}$$

$$\frac{P_2(t)}{3} = \frac{P_2^*}{3} \tag{8.31}$$

Substituting (8.30) and (8.31) in (8.29) and assuming the balance between the requested power on the two sides of the converter the following expressions are obtained.

$$\frac{P_1^*}{3} + \frac{P_2^*}{3} = 0 \tag{8.32}$$

$$\frac{dP_{DCA}(t)}{dt} = \frac{1}{2} C \frac{dV_{DCA}(t)^2}{dt} \tag{8.33}$$

Integrating (8.33) between t_k and t_k+T_s and imposing the DC-Link voltage at the next sampling interval equal to desired DC-Link voltage reference V_{DCA}^* as in equation (8.34) the expression of equation (8.35) is obtained.

$$V_{DCA}(t_k + T_s) = V_{DCA}^*(t_k) \tag{8.34}$$

$$P_{DCA}(t_k + T_s) = P_{DCA}(t_k) + \frac{1}{2} C \left[V_{DCA}^{*2}(t_k) - V_{DCA}^2(t_k) \right] \tag{8.35}$$

Equation (8.35) represents the energy necessary to maintain the DC-link voltage regulation for one sampling period. It is important to note that equation (8.35) doesn't consider any losses in the DC circuit and the resulting steady state error is reduced using the DC-Link voltage control in the predictive algorithm. The current reference is then calculated as in (8.36) and (8.37).

$$i_{1A}{}^{*}(t_k + iT_s) = \frac{{P^*}/{3} + P_{DCA}}{\cos(\varphi_{A1,,AC})\, V_{A1,rms}\sqrt{2}} sin(\theta_{1A} + iT_s - \varphi_{A1} + 0.5T_s) \quad , \; i = 1{,}2 \quad (8.36)$$

$$\varphi_{A1} = atan\left(\frac{{P^*}/{3} + P_{DCA}}{Q^*}\right) \quad (8.37)$$

The half-step delay in the current sampling introduces an additional terms in (8.36) in order to maintain the current reference calculation synchronised with the current sampling. The DC-Link voltage reference value is suitably limited to a ramp variation in order to avoid interactions with the dynamic of the current control and undesired distortion on the grid current. A factor *N*, representing the DC-Link voltage reference horizon, is used for this purpose.

$$V_{DCA}{}^{*}(t_k) = V_{DC}{}^{*} + \frac{V_{DC}{}^{*} - V_{DCA}(t_k)}{N} \quad (8.38)$$

8.1.2.4 H-Bridge state selector

The converter state, selected by the MPC, is applied by applying a combination of appropriate HBs states. The HB selected to switch is determined by a set of iterative rules with the aim of maintaining equal voltage on the DC-Link capacitors, distributing the commutations equally across the HBs and reduce the overall switching frequency. In particular the HB selected, from all of the HBs that can produce the desired converter voltage, is the one that respects the following rules:

- Only one leg of a single HB is allowed to switch, if necessary, at every switching instant.
- If the DC-Link voltages are unbalanced, the HB with the largest unbalance, but the best opportunity for DC voltage error reduction, is selected to switch.
- If the DC-Link voltages are well balanced or is not possible to reduce the unbalance by applying the desired converter state, the HB that has switched the least in the past switching instants is selected.

It can be noticed that the MPC state selector follows exactly the same rules as the DCM modulator with the active voltage balancing algorithm, described in Chapter 6.

8.1.2.5 Overall control scheme

The total cost function is chosen to be a weighted combination of the current and DC-Link voltage cost functions.

$$G_{1A} = w_I G_{I1A} + w_V G_{V1A} \tag{8.39}$$

The two weighting factor w_I and w_V can be adjusted to achieve the desired the control performance. Typically the weighting factors are set in order to have $w_V > w_I$; in fact, since the current cost function G_{IIA} already includes the amount of current necessary to charge at the desired voltage the DC-Link capacitor, it is usually verified the condition $G_{IIA} > G_{VIA}$ and the two weighting factors are used to equalise the values of DC-Link voltage and current cost functions. It is clear that G_{VIA} is important to reduce the DC-Link voltage steady state error, related with the converter losses that are not considered in G_{IIA}. Based on this considerations the ratio w_V/w_I is typically set to the minimum value that allows to achieve zero steady state error on the DC-Link voltage.

Using this approach the DC-Link voltage and AC current errors minimisation are achieved at the same sampling instant, $t_k + 2T_s$. The overall control scheme for a single phase of the converter is shown in Figure 8.8 where the absence of a modulation scheme should be noted.

The aim of the method is to control the AC current and the DC link voltages at the required references, and obtaining the desired active and reactive power (P^* and Q^*). Considering the global cost function of equation (8.39), the state selected is the one that minimises the current error and the DC-Link Voltage error at time $t_k + 2T_s$. The result is that the DC-Link voltage prediction depends on the current prediction obtaining a global cost function where both the targets of the control are coupled.

This coupling allow the MPC scheme to compute the converter state that minimise the tracking error on both AC current and DC-Link voltage, without producing any DC component on the line current. A similar control scheme is adopted on each phase of port 2 with the only difference that in this case a DC-Link voltage control is not required and only the current control is

implemented. As for DBC, MPC requires the prediction of the supply voltage v_{A1} that is obtained from previous periods as described in Appendix A, assuming ideal supply operating conditions.

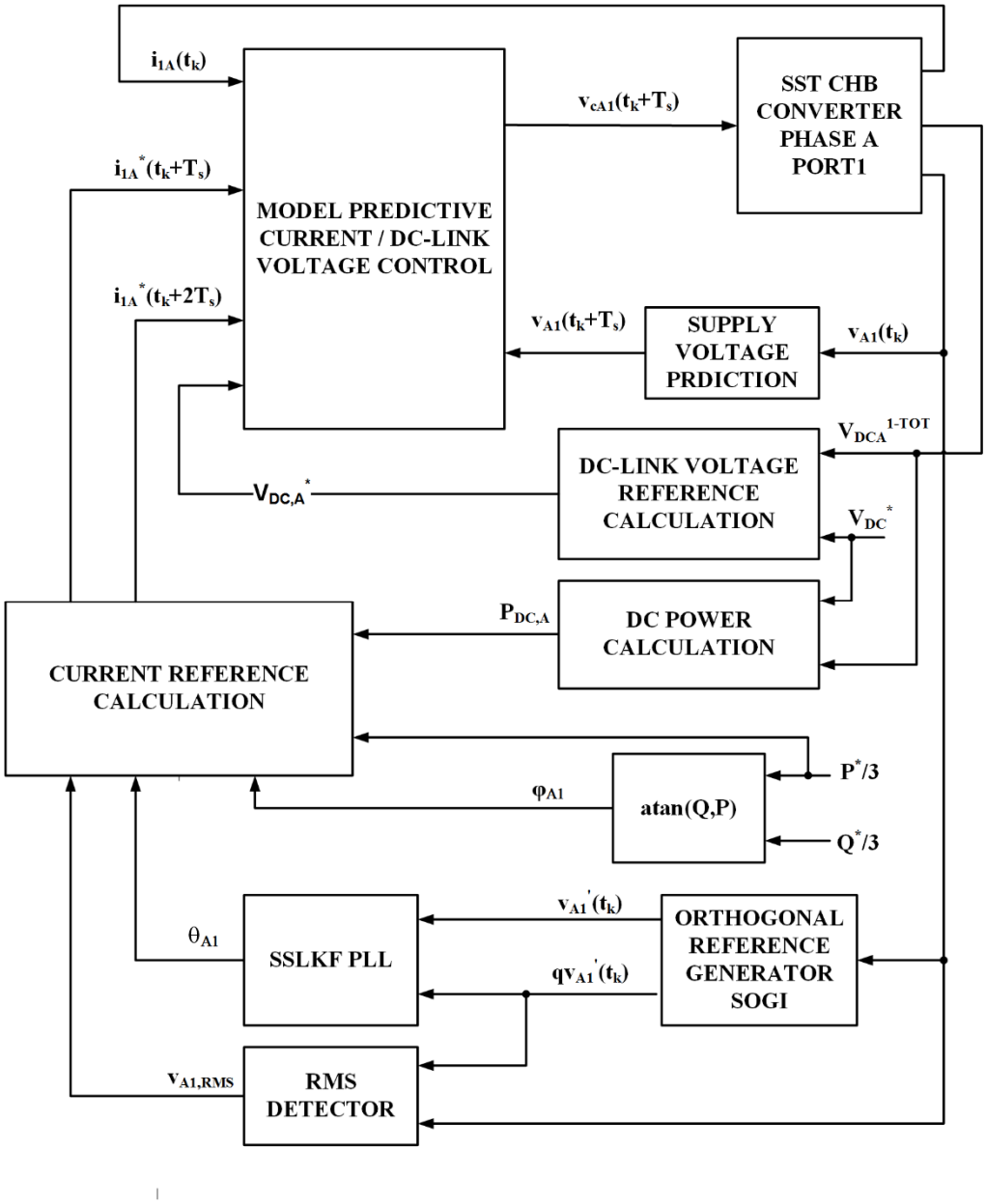


Figure 8.8 Model Predictive Control block scheme on the grid connected of the AC/DC/AC converter.

8.2 Simulation results for Model Predictive current / DC-Link voltage control

A simulation of the MPC algorithm has been carried out for the overall for the 7-Level CHB SST of Figure 8.1. The simulation parameters are set to be equal to those on the UNIFLEX-PM demonstrator as rated in Table 3.1. The control sampling frequency has been chosen equal to 5kHz as per previous specifications; however, in this case the converter presents a variable switching frequency below 2.5kHz. Table 8.1 shows the MPC parameters adopted in the simulation.

Table 8.1 MPC simulation parameters.

Name	***Description***	***Value***
N	DC-Link voltage reference horizon	3
w_I	Current control weighting factor	1
w_V	DC voltage control weighting factor	0.5
$\mathbf{R_e}$	Equivalent DC-Link resistance	1kΩ

Figure 8.9 shows the active and reactive power tracking of the MPC control when power variations are considered. Clearly, the MPC produces a higher ripple with respect to DBC but an accurate average power tracking is maintained. As for DBC, a steady state error is produced on reactive power of about 6% of the converter rated power and also in this case can be explained considering the model discretisation errors, which causes an undesired phase shift between the supply voltage and current of half sampling period; however this error can be compensated by using additional compensation terms in the current reference calculation when needed, as for example in really high power applications.

Figure 8.10 shows the DC-Link voltage tracking for MPC. It is possible to notice that in this case optimal DC-Link voltage tracking is achieved even during power references perturbations, in contrast with DBC. Moreover, since an active DC-Link voltage balancing algorithm is implemented in the state selector, the DC voltage on each capacitor of every phase is well regulated minimal error. It is important to highlight the faster dynamics of the MPC DC-Link voltage control when compared to the traditional PI control implemented in the DBC. Since the

MPC current and DC-Link controller coupled together, it is possible to design the parameters of the DC-Link voltage controller in order to achieve a wider bandwidth compared to the PI regulator in DBC. In particular in the case of the performed simulation, the DC-Link voltage reach the steady state in a number of sample defined by *N* in Table 8.1.

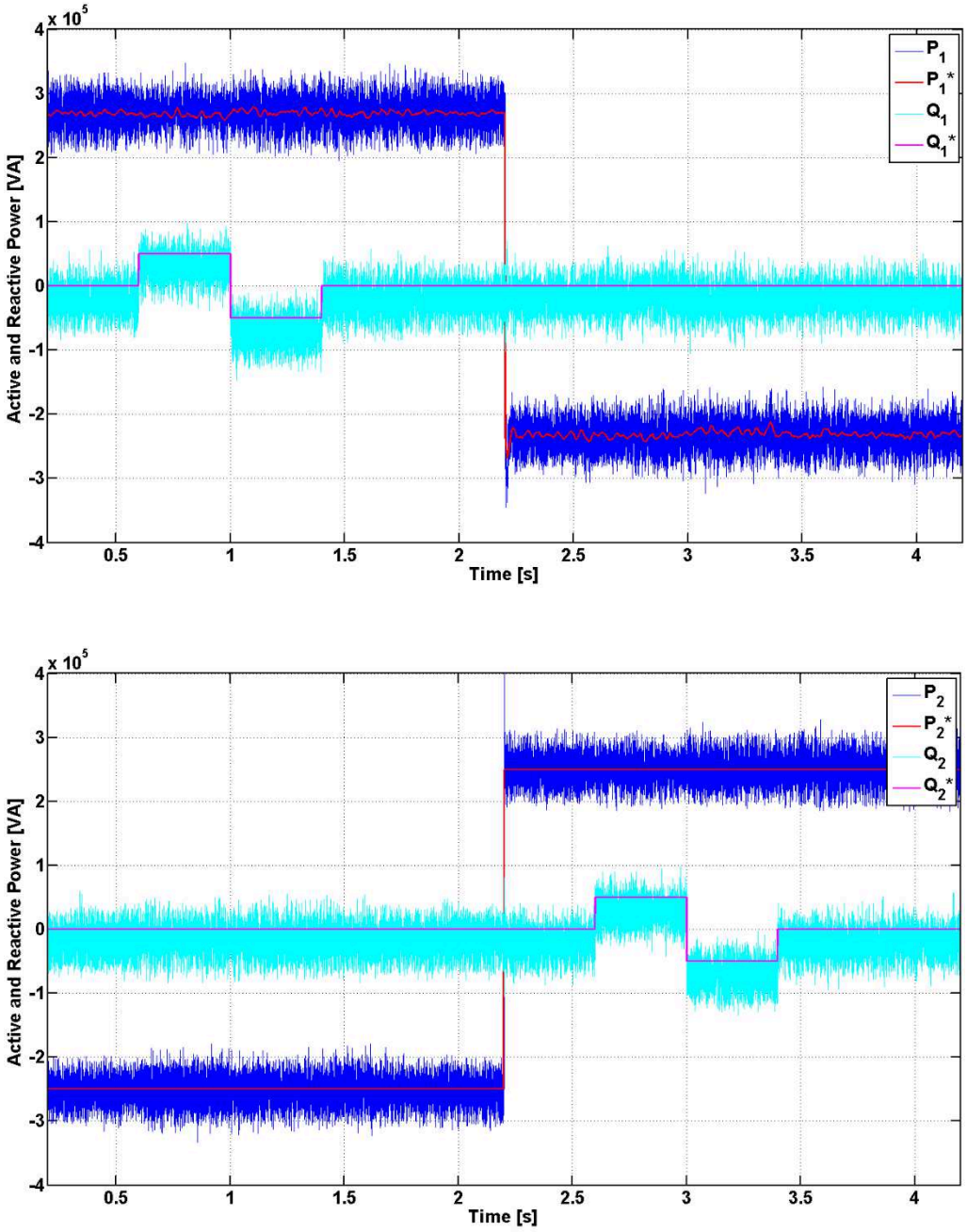


Figure 8.9 MPC simulation for UNIFLEX-PM SST converter: active and reactive power flow vs references on the two SST sides.

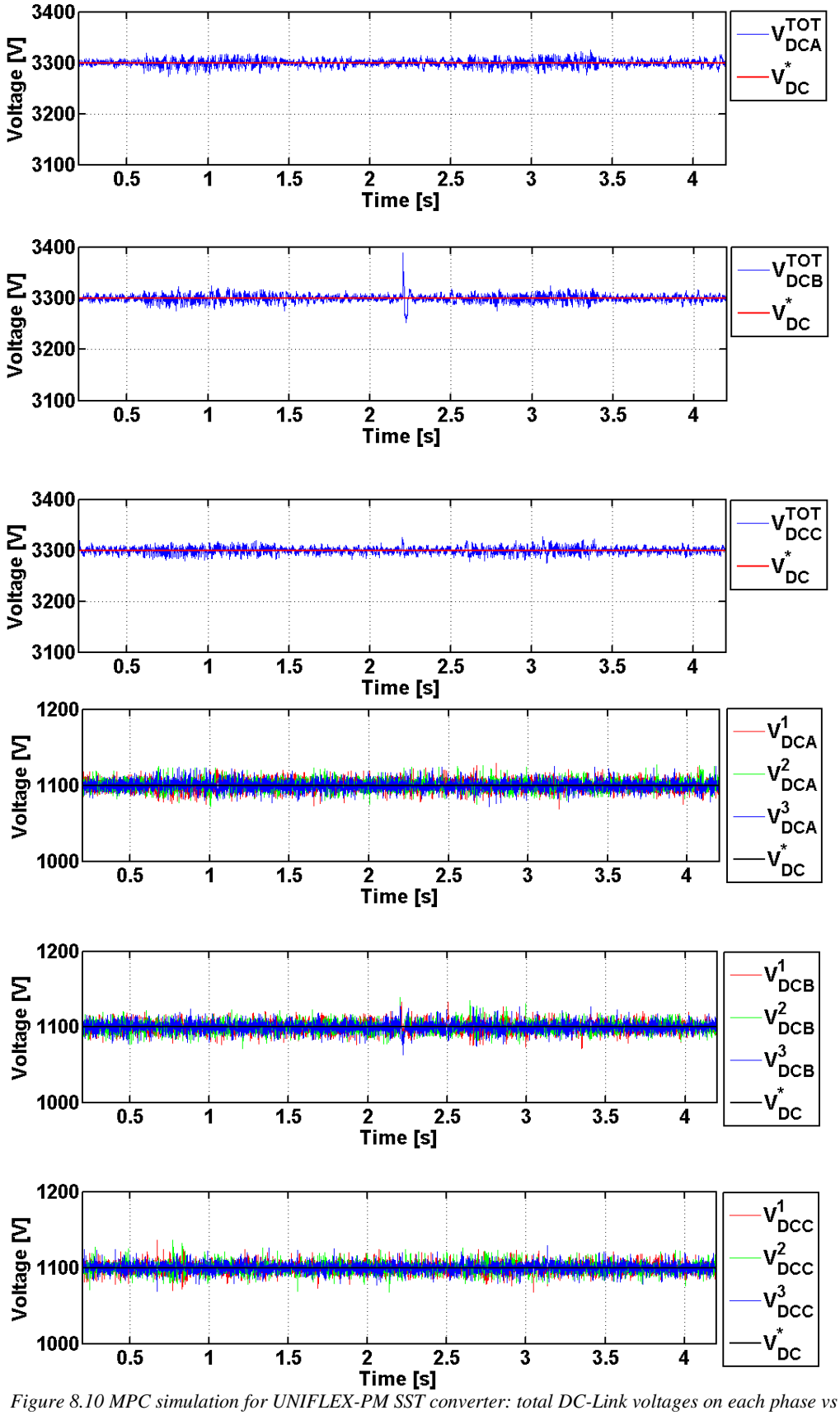


Figure 8.10 MPC simulation for UNIFLEX-PM SST converter: total DC-Link voltages on each phase vs DC-Link voltage reference and single DC-Link capacitors voltages.

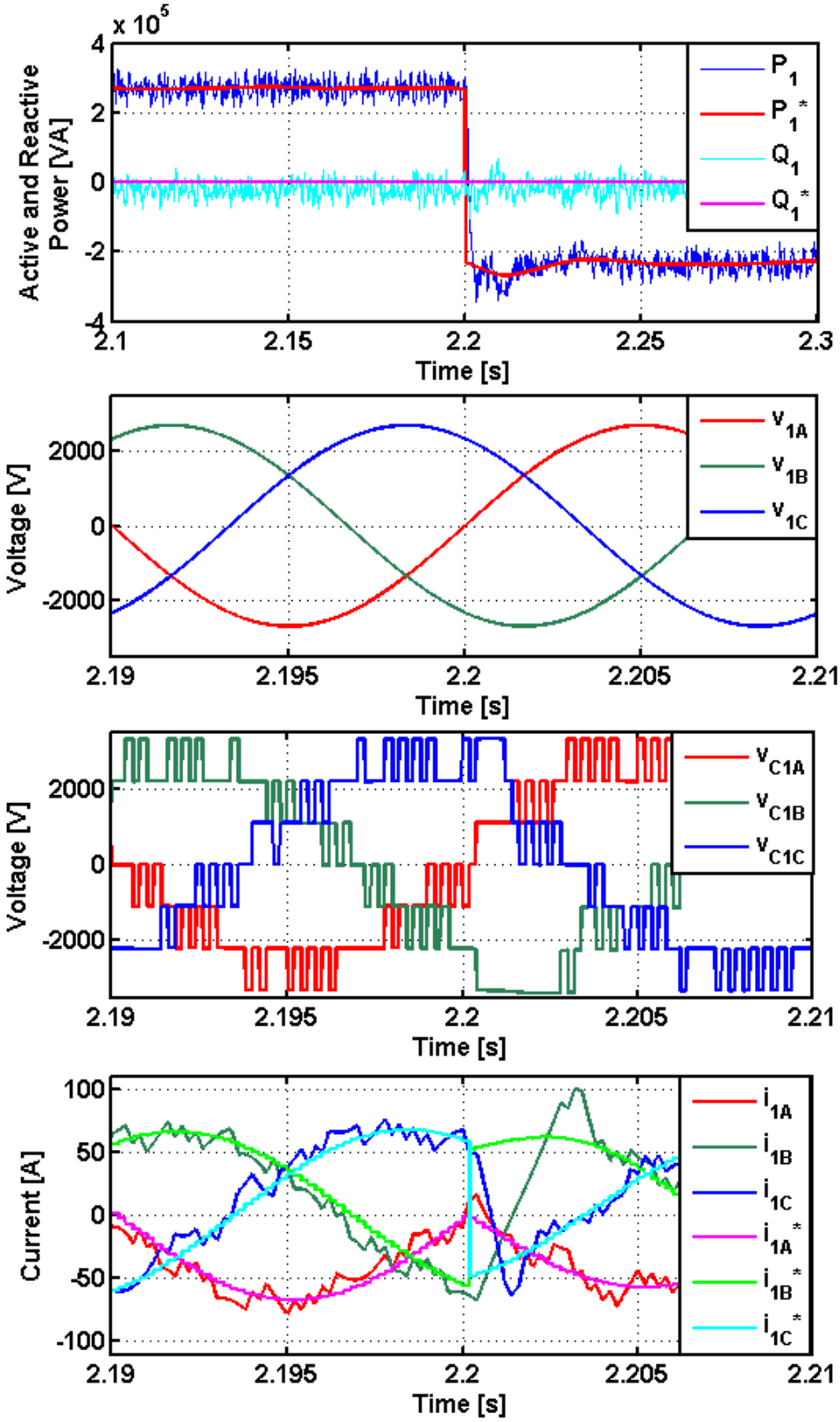


Figure 8.11 MPC simulation for UNIFLEX-PM SST converter: grid voltage, converter voltage and AC current vs current reference on the three phases of both side of the SST converter when an active power reference step from 250kW to -250kW is applied on port 1 at time2.2s.

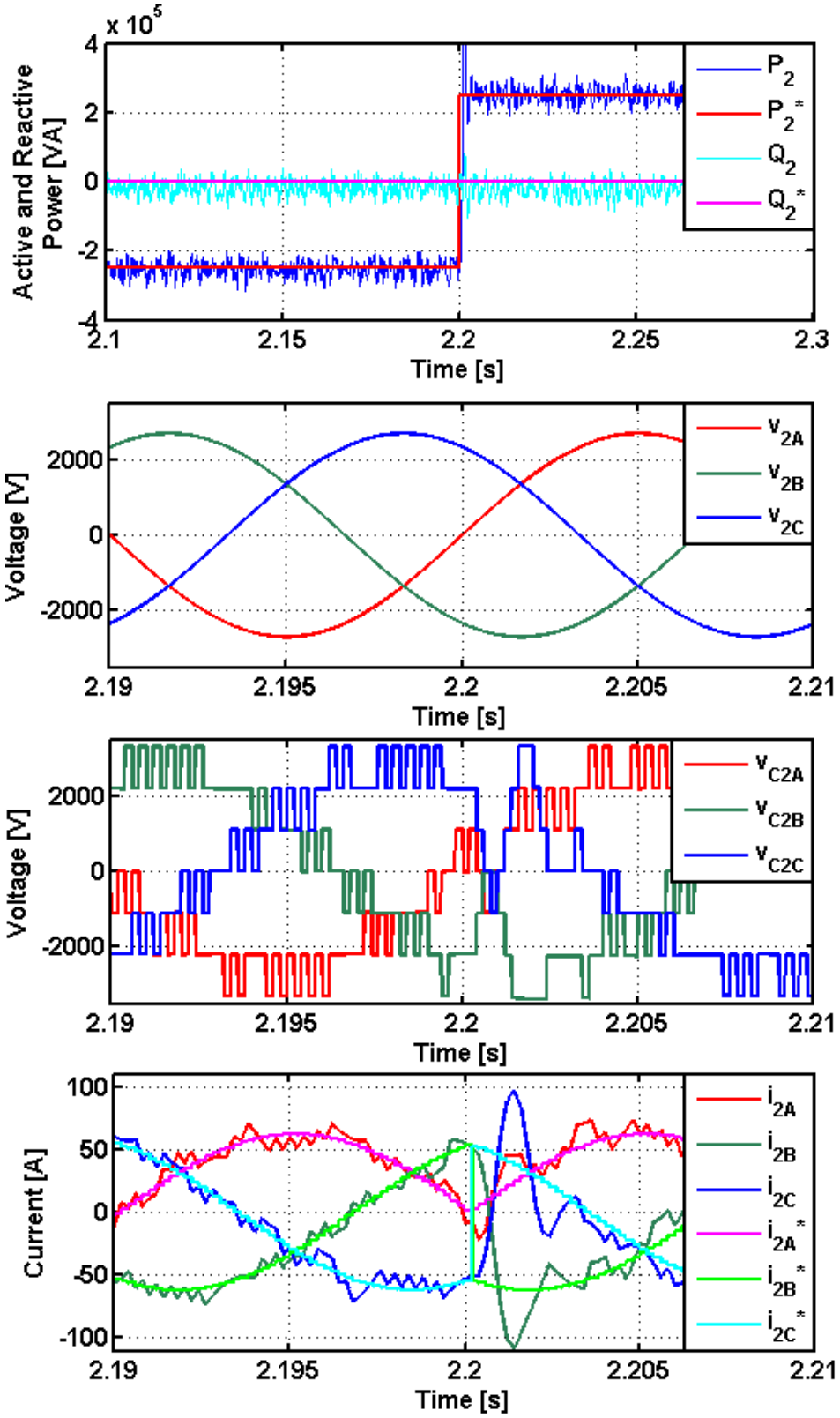


Figure 8.12 MPC simulation for UNIFLEX-PM SST converter: grid voltage, converter voltage and AC current vs current reference on the three phases of both side of the SST converter when an active power reference step from -250kW to 250kW is applied on port 2 at time2.2s.

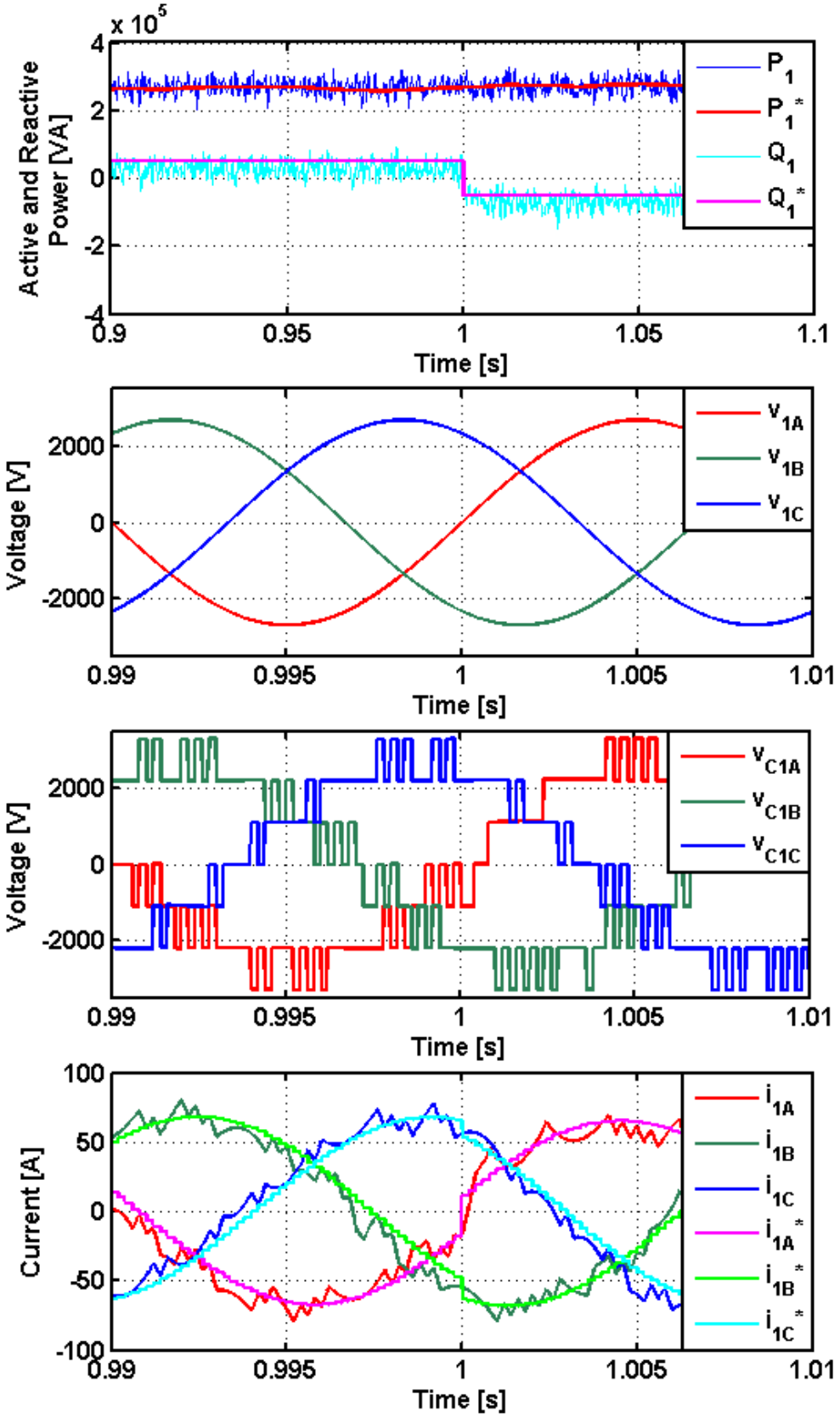


Figure 8.13 MPC simulation for UNIFLEX-PM SST converter: grid voltage, converter voltage and AC current vs current reference on the three phases of both side of the SST converter when a reactive power reference step from 50kVAR to -50kVAR is applied on port 1 at time 1s.

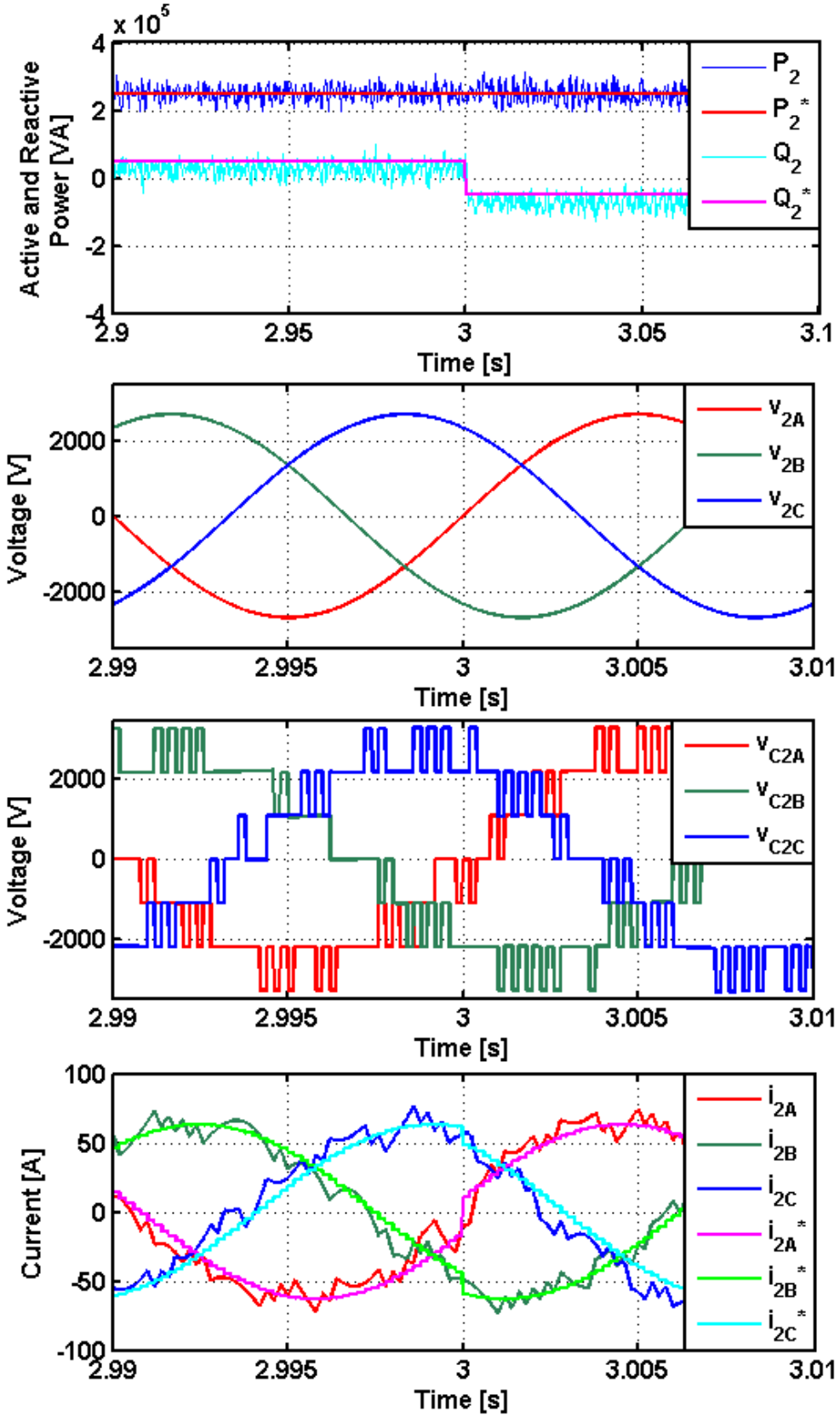


Figure 8.14 MPC simulation for UNIFLEX-PM SST converter: grid voltage, converter voltage and AC current vs current reference on the three phases of both side of the SST converter when a reactive power reference step from 50kVAR to -50kVAR is applied on port 2 at time 3s.

Figure 8.11, Figure 8.12, Figure 8.13 and Figure 8.14 show the MPC transient response to step changes in the active and reactive power references. From these figures it is clear that MPC produces sinusoidal AC currents with the higher harmonic distortions with respect to DBC. In Figure 8.11and Figure 8.12 an active power step of 250kW is applied and the control react to the transient with a fast response. In Figure 8.13 and Figure 8.14 a reactive power step from 50kVAR to -50kVAR is applied and also in this case the MPC provides fast current tracking. It can be observed from these figures that the main limitation of MPC is due to the absence of a PWM scheme. By using a finite control set MPC is it possible to apply only a limited number of average voltage values during one sampling interval. This behaviour causes a considerable oscillation between adjacent voltage states and results in high current ripple. In all Figure 8.11, Figure 8.12, Figure 8.13 and Figure 8.14 is possible to see that, even if a fast response to active and reactive power step is achieved with MPC, the phase currents present a much higher distortions when compared to DBC. Moreover, the converter voltage pulse width is variable at values multiple of T_s. As a result the switching frequency is not constant and, in particular, presents values lower than the sampling frequency with a relationship which is dependent on the load conditions.

Figure 8.15 shows the harmonic spectrum of converter voltages and AC currents, calculated considering one period of the waveforms in steady state conditions. Moreover, Figure 8.15 shows that the switching frequency of the MPC waveforms are below 2.5kHz, producing a harmonic spectrum which is spread across the frequency range with a THD of approximately 24-26% for the converter voltages on the primary side of the SST. These low frequency harmonics, produced by the converter, are not filtered effectively by the line inductance resulting in a current THD that is approximately 12-14% (and variable) for the AC currents on the primary side of the SST. The spectrum results different on the three phases as a consequence of the variable switching frequency of MPC that allows the control to produce non-periodic waveforms even in steady state operative conditions. The effective reduction in device switching frequency does, however, howe a positive effect on the overall converter efficency. Since the converter voltage waveforms vary from a period to another, only one converter voltage and current periods are considered to calculate the harmonic content.

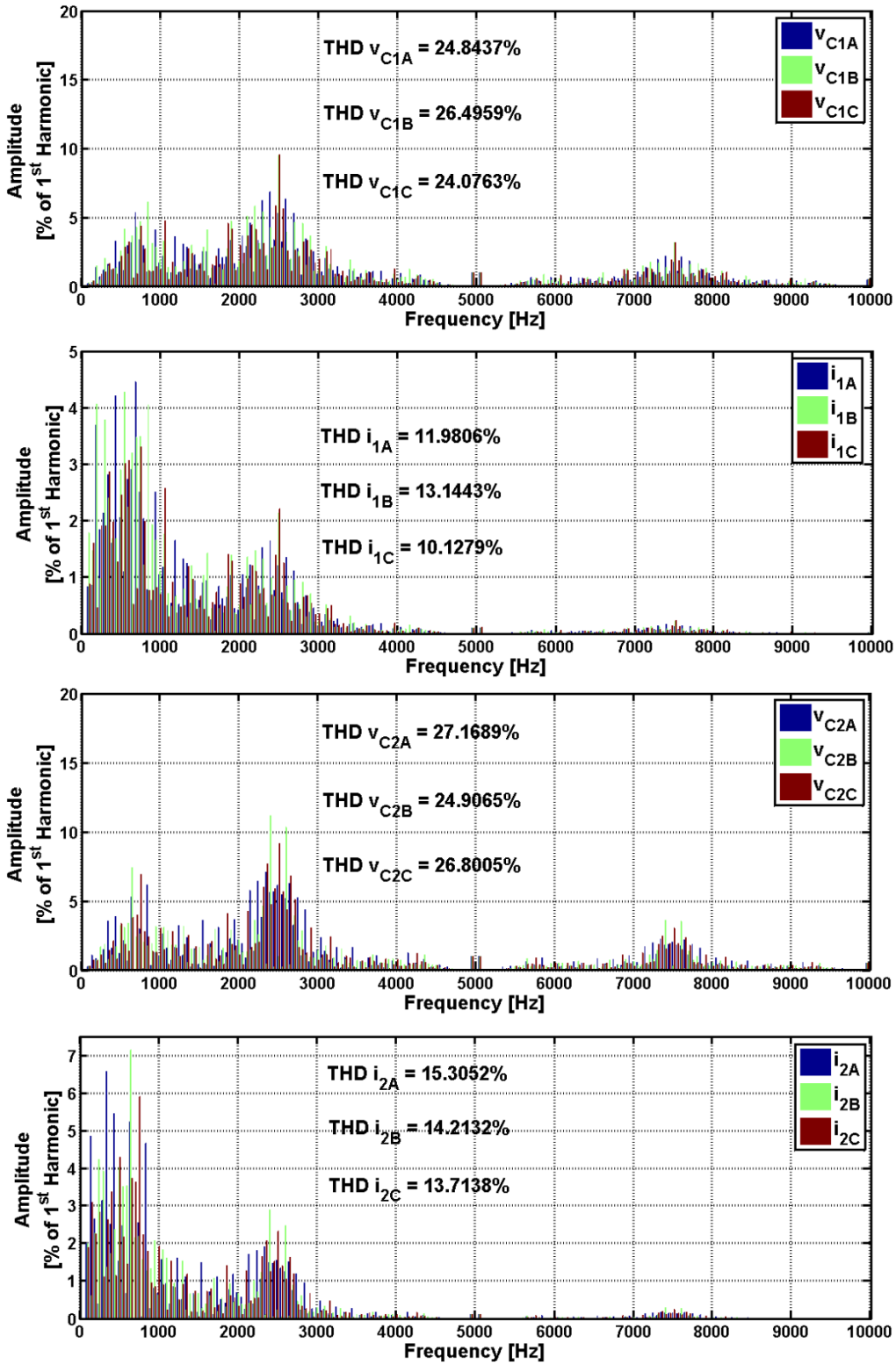


Figure 8.15 MPC simulation for UNIFLEX-PM SST converter: AC current and converter voltages harmonic content on the three phases of both sides of the SST converter.

8.3 Experimental results for Model Predictive Control on Universal and Flexible Power Management converter

Experimental testing has been carried out on the two port UNIFLEX-PM demonstrator considering the configuration shown in Figure 3.14 and the overall control scheme of Figure 8.8 on port 1 whilst on port 2 only the current control is implemented. In this case port 1 is connected to the grid and port 2 is connected to a resistive load. The proposed controller has been tested under non-ideal grid conditions using the converter prototype shown in Figure 3.8. The experimental parameters are shown in Table 8.2. The weighting factor value for the DC-Link voltage has been increased when compared to simulations in order to meet the zero steady state requirement on the real converter taking into account the finite delay introduced by the DC/DC converter. Results are shown only for port 1 since the control on port 2 is identical with the only exception that the DC-Link voltage control is not required on port 2 and there is no grid connection on port 2.

Table 8.2 MPC experimental parameters.

Name	*Description*	*Value*	*Unit*
C	DC-Link capacitor	3100	[μF]
r_L	Inductor resistance	0.5	[Ω]
L	AC filter inductance	11	[mH]
R_{LOAD}	Load resistance	30	[Ω]
V_{1peak}	Rated peak value of the AC supply on port 1 (line-to-line)	212	[V]
V_{2peak}	Rated peak value of the AC supply on port 2 (line-to-line)	212	[V]
V_{DC}	Capacitor voltage	92	[V]
$f_{sw,DC/DC}$	Switching frequency of DC/DC converter	2500	[Hz]
T_s	Sample time	0.2	[ms]
N	DC-Link voltage reference horizon	100	/
w_I	Current control weighting factor	1	/
w_V	DC voltage control weighting factor	5	/

In Figure 8.16 steady state performance of the MPC method are analysed for phase A, port1. The converter voltage shows a variable switching frequency waveform with a THD of approximately 25% while the current has a THD of approximately 7%.

Care should be taken since, even if the converter voltage THD doesn't differ from the DBC converter voltage THD, the low order harmonics presents with the MPC method are weakly attenuated by the line inductance and therefore results in a significant line current THD.

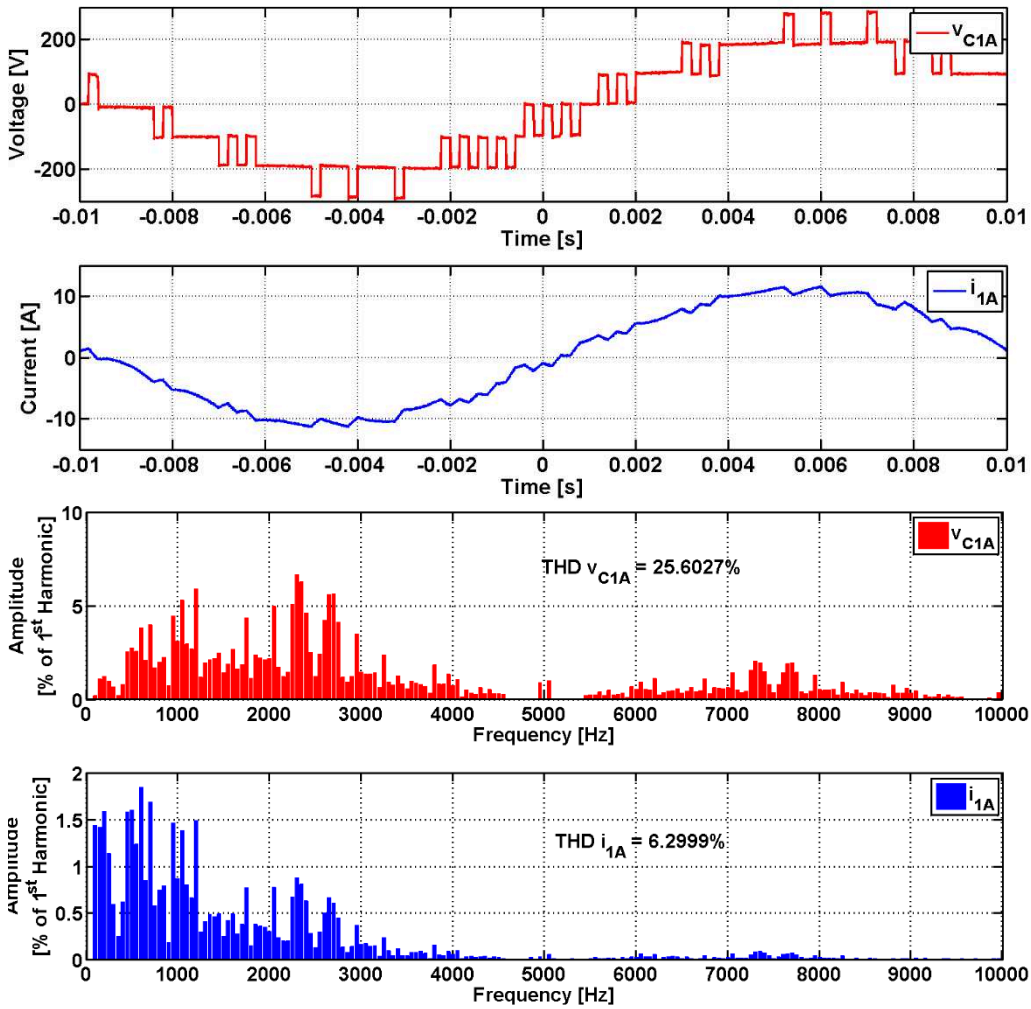


Figure 8.16 Experimental results for MPC on UNIFLEX-PM SST converter: steady state converter voltage and AC current on phase A, port 1.

In Figure 8.17 an active power step from 0W to 3kW is considered. As for the DBC, the finite delay introduced by the DC/DC converter has to be considered and, in order avoid interactions with the DC-Link voltage control response, the active power reference variation has to be limited. Also in this case a ramp generator is implemented, taking 0.2s to meet its target value. From the figure, the generated active power is around 3.8 kW. The extra 800W is requested by the DC-Link voltage control in order to regulate the DC-Link voltages at the desired value and compensate the overall converter losses. The improved performance of the MPC DC-Link voltage controller when compared to the traditional PI control implemented in the DBC is clear and the DC-Link voltages take around 0.4s to recover the DC-Link voltage tracking with a maximum error of about 10% of the nominal value.

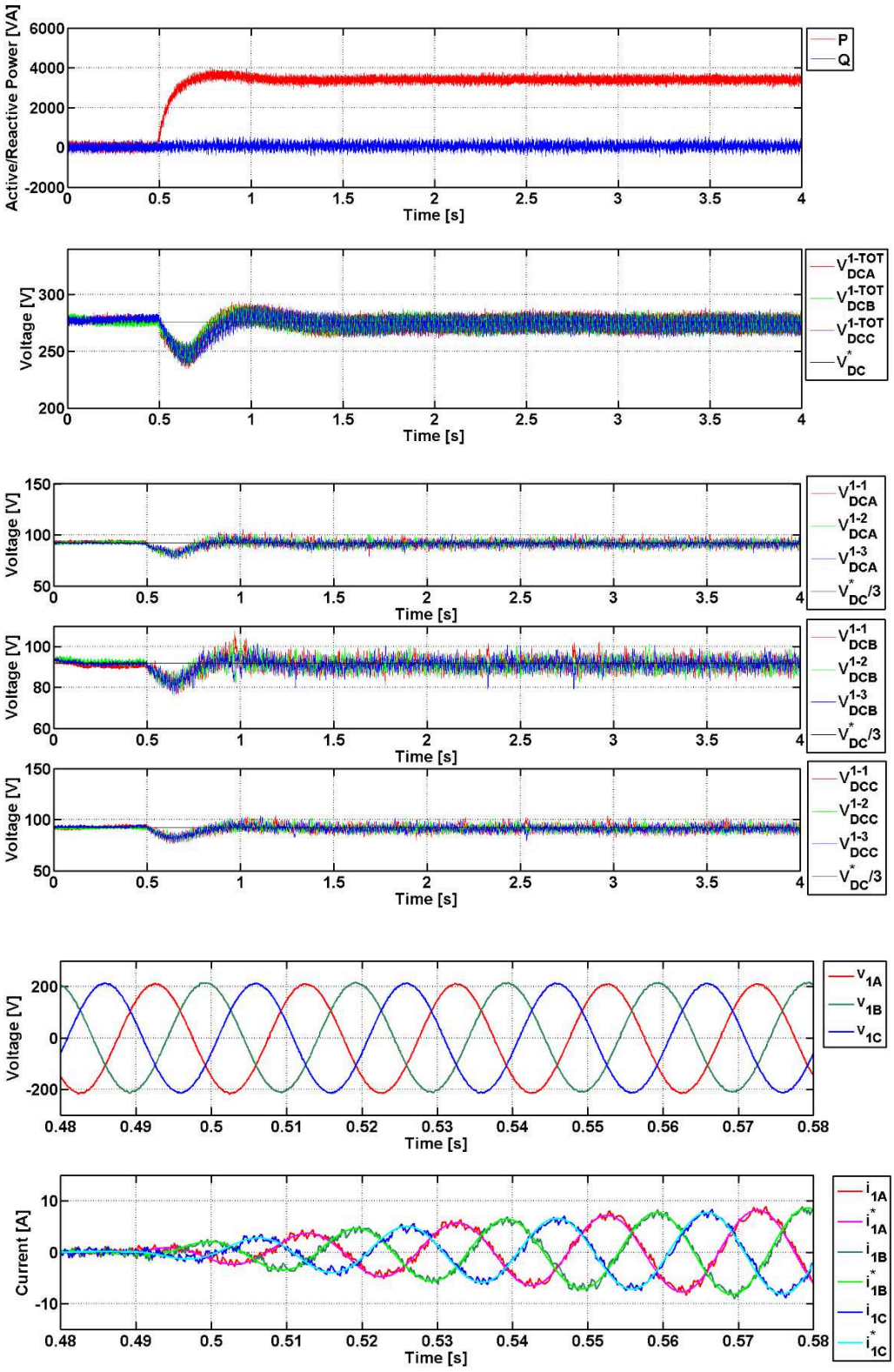


Figure 8.17 Experimental results for MPC on UNIFLEX-PM SST converter: Active and Reactive power, DC-Link voltages, grid voltages and AC currents vs current references on port 1 when an active power step from 0kW to 3kW is demanded to the SST converter at time 0.5s.

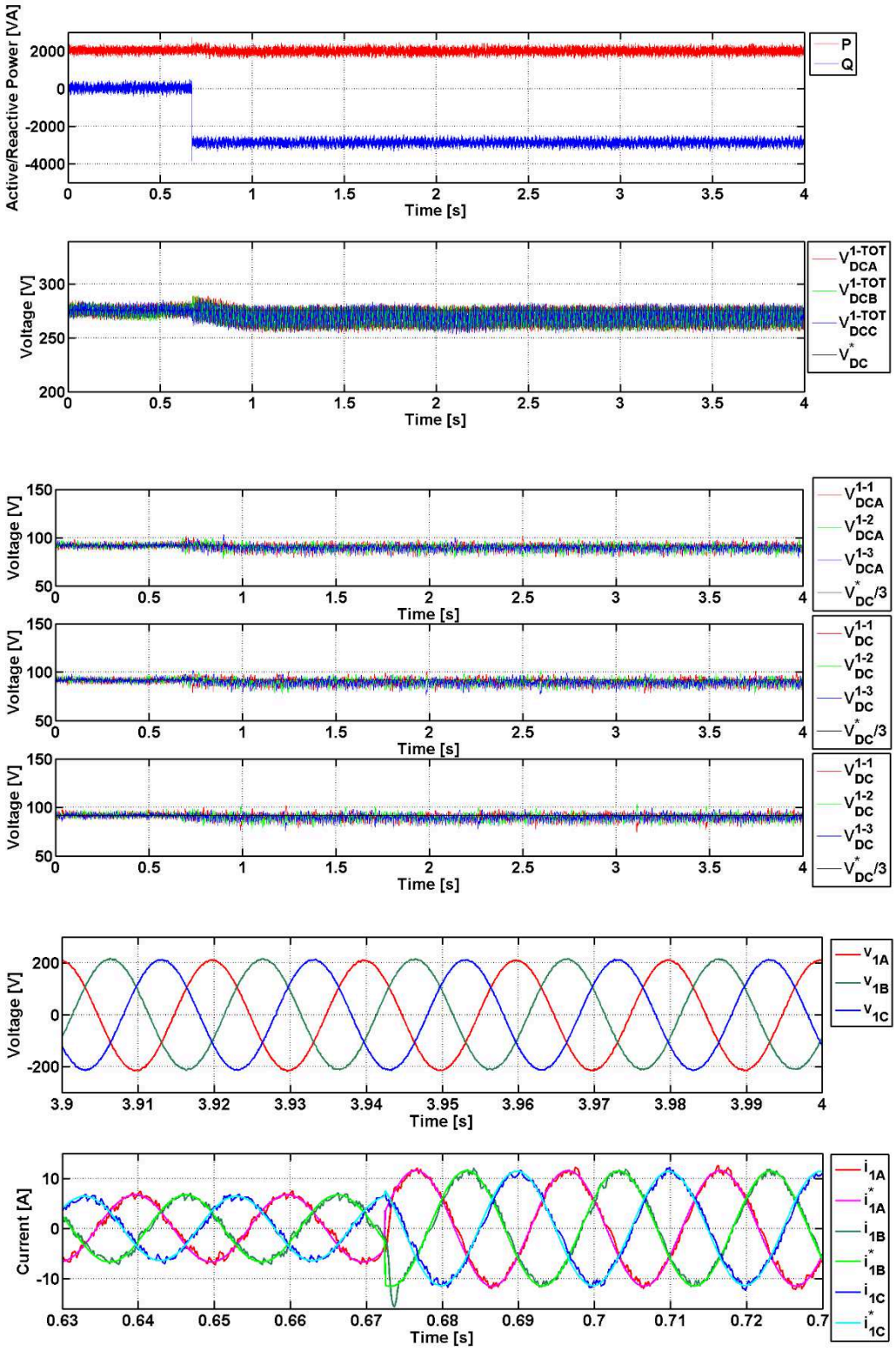


Figure 8.18 Experimental results for MPC on *UNIFLEX-PM converter: active and reactive power, DC-Link voltages, grid voltages and AC currents vs current references on port 1 when a reactive power step from 0kW to -3kVAR is demanded to the SST converter at time 0.673s.*

On the other hand, even if AC currents and voltages are in phase as desired, the MPC current control shows a higher current ripple, due to the variable switching frequency and the absence of PWM technique in the control algorithm. In Figure 8.18 a reactive power step from 0VAR to -3kVAR, while an active power of 1.8kW is delivered to port 2, is considered. In this case, because reactive power is managed independently on the two side on the converter, the dynamic of the DC-Link voltage control is not affected from reactive power variations and there is no need to slow down the reactive power reference. The obtained power tracking match the simulations results dynamic and the DC-Link voltages remains regulated and balanced at the desired value with neglectable error. Moreover, the AC voltages ad currents show that the current tracking is lost only for few milliseconds before the control recover the optimal tracking. More experimental tests have been conducted under non-ideal grid conditions.

More experimental tests have been conducted under non-ideal grid conditions. During the experimental testing the power references have been fixed to P*=2.5kW and Q*=0kVAR and the following non-ideal grid conditions have been considered in Figure 8.19, Figure 8.20, Figure 8.21, Figure 8.22:

- Frequency variations.
- Phase jumps.
- Grid voltages excursions.
- Grid voltages unbalances.

Such conditions are generated with the aid of a programmable power AC source, rated 12 kVA.

The first test has considered an instantaneous supply frequency excursion from 50Hz to 53Hz (6% of nominal value), as shown in Figure 8.19. The MPC recovers synchronisation between AC voltage and current providing zero reactive power in a single sampling interval, during which a phase shift between AC current and voltage is produced; also in this case the supply frequency is detected dynamically using a zero-crossing detector on the filtered voltage at the output of a SOGI, introducing a delay of one supply period. It is the frequency error which affects the current reference calculation and the voltage prediction resulting in an undesired transient of one supply period.

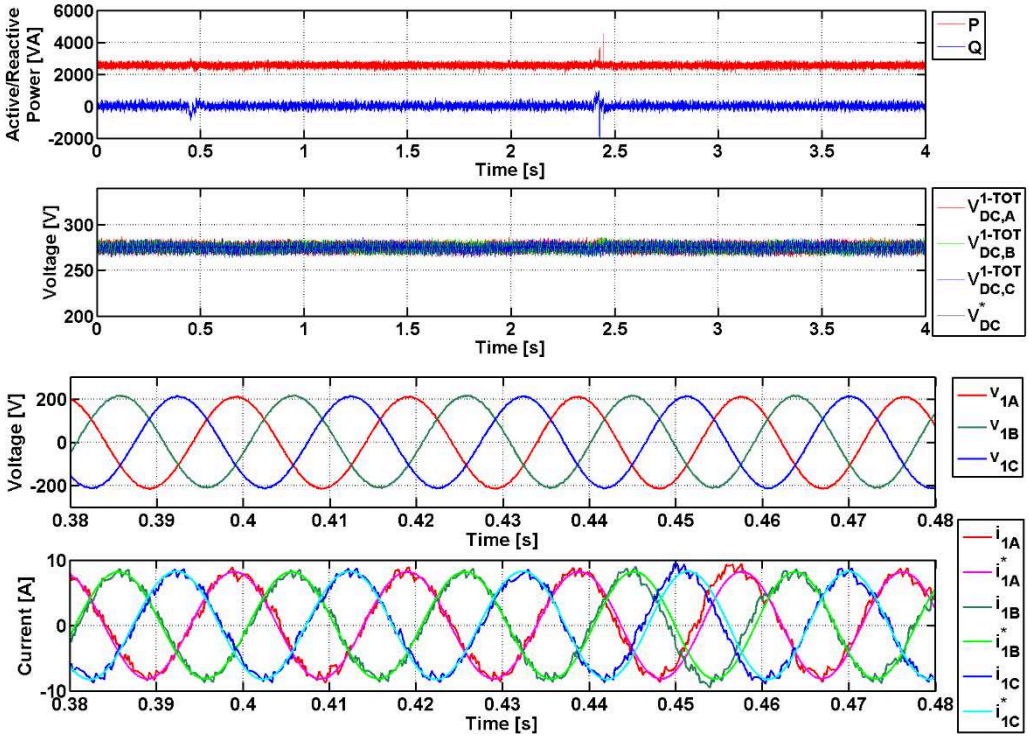


Figure 8.19 Experimental results for MPC on UNIFLEX-PM SST converter: active and reactive power, total DC-Link voltages, grid voltages and AC currents on port 1 of the SST converter when a frequency step from 50Hz to 53Hz is applied at time 0.5s and a frequency step from 53Hz to 50Hz is applied at time 2.4s.

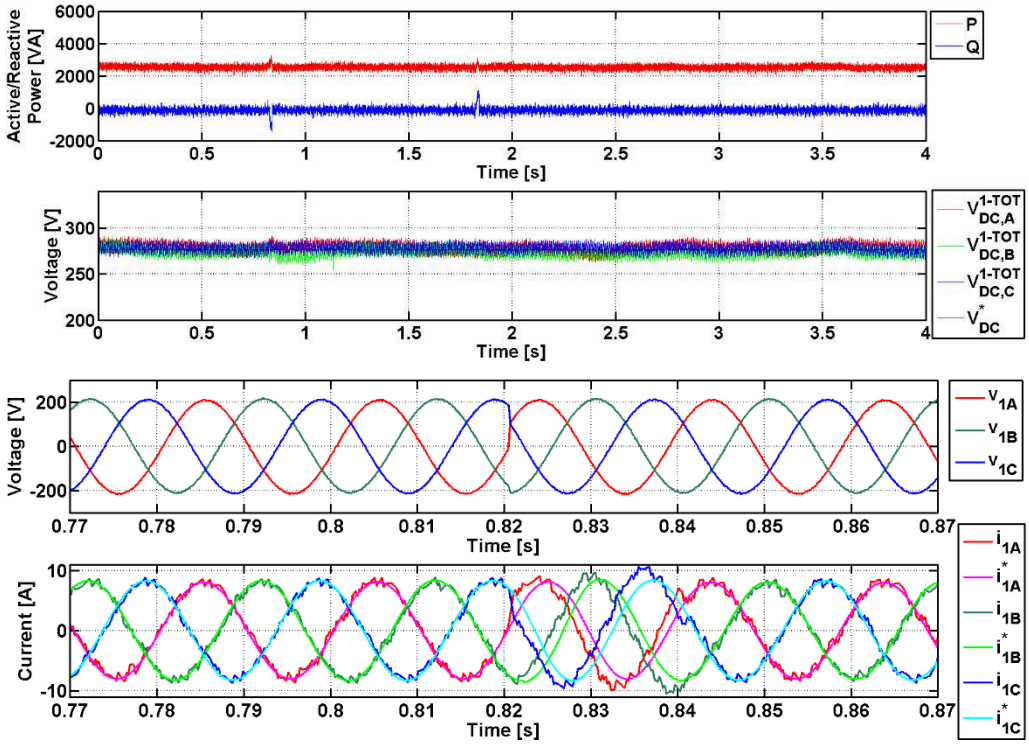


Figure 8.20 Experimental results for MPC on UNIFLEX-PM SST converter: active and reactive power, total DC-Link voltages, grid voltages and AC currents on port 1 of the SST converter when a phase jump from 0° to 30° is applied at time 0.85s and a phase jump from 30° to 0° is applied at time 1.8s.

In the second test an instantaneous phase jump of 30° is considered, as shown in Figure 8.20. The MPC method takes one supply cycle to recover synchronisation between the AC voltage and current. The DC-link voltage tracking is never lost as result of the phase jump as well as the active and reactive power tracking.

In the third test a supply voltage amplitude excursion from 150V RMS to 130V RMS (20% of nominal value) is considered, as shown in Figure 8.21. In this case the MPC method presents a fast response for the DC-Link voltage and power tracking; the fast dynamic response of the MPC DC-Link voltage controller shows a much improved dynamic performances when compared to DBC method.

Finally, a supply voltage unbalance, defined by the positive sequence to negative sequence ratio, of 10% is considered in Figure 8.22; the DC-Link voltages are maintained well regulated with minimal variation. Also in this case, because a four wire the produced currents are balanced even in presence of unbalanced currents.

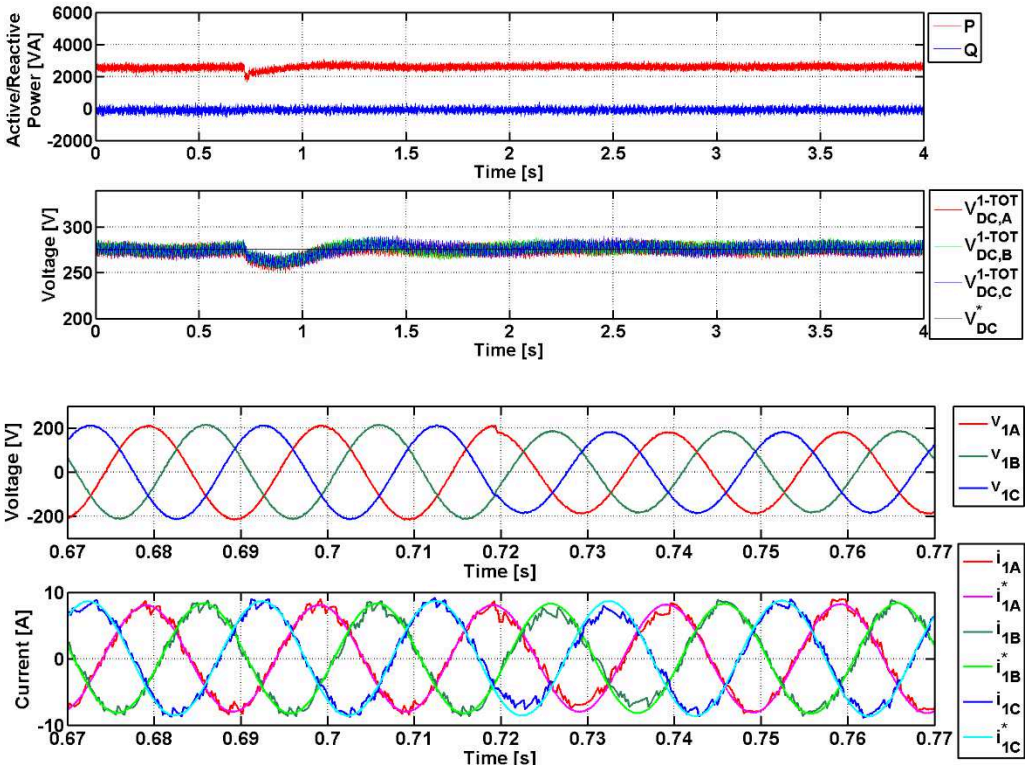


Figure 8.21 Experimental results for MPC on UNIFLEX-PM SST converter: active and reactive power, total DC-Link voltages, grid voltages and AC currents on port 1 of the SST converter when an amplitude step from 150V RMS to 130V RMS is applied at time 0.7s.

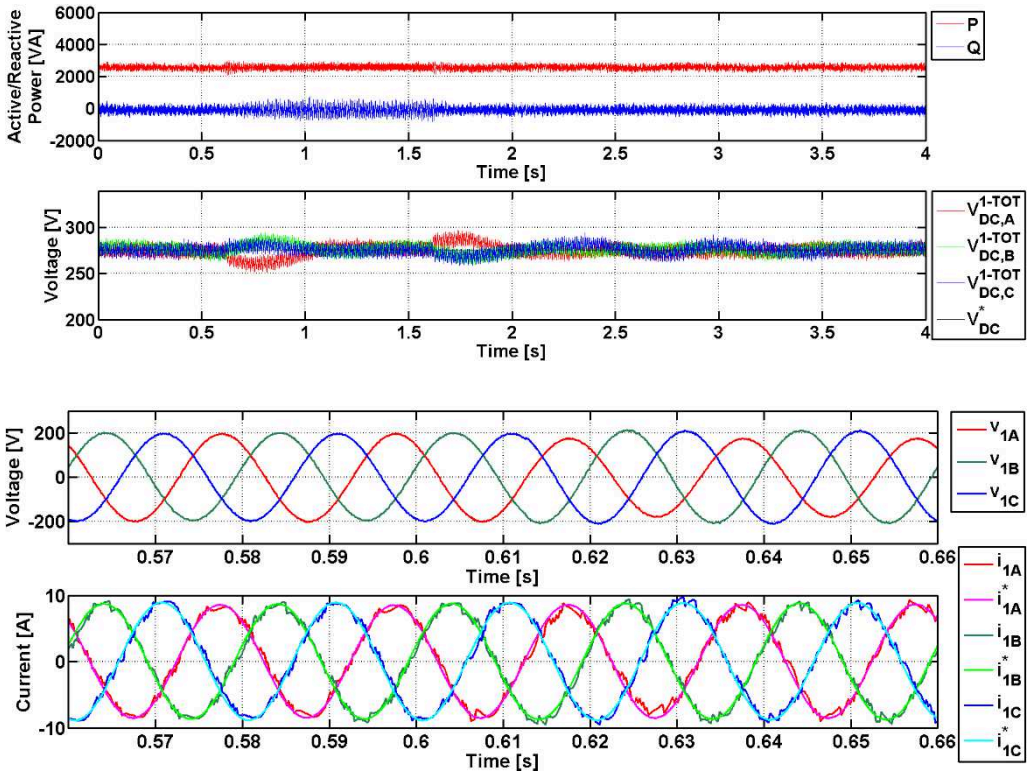


Figure 8.22 Experimental results for MPC on UNIFLEX-PM SST converter: active and reactive power, total DC-Link voltages, grid voltages and AC currents on port 1 of the SST converter when a voltage unbalance of 10% is applied.

8.4 Simulation and experimental results comparison

In Figure 8.23 the waveform obtained using the MPC technique described in this chapter, experimentally on the UNIFLEX-PM demonstrator and in simulation, are compared.

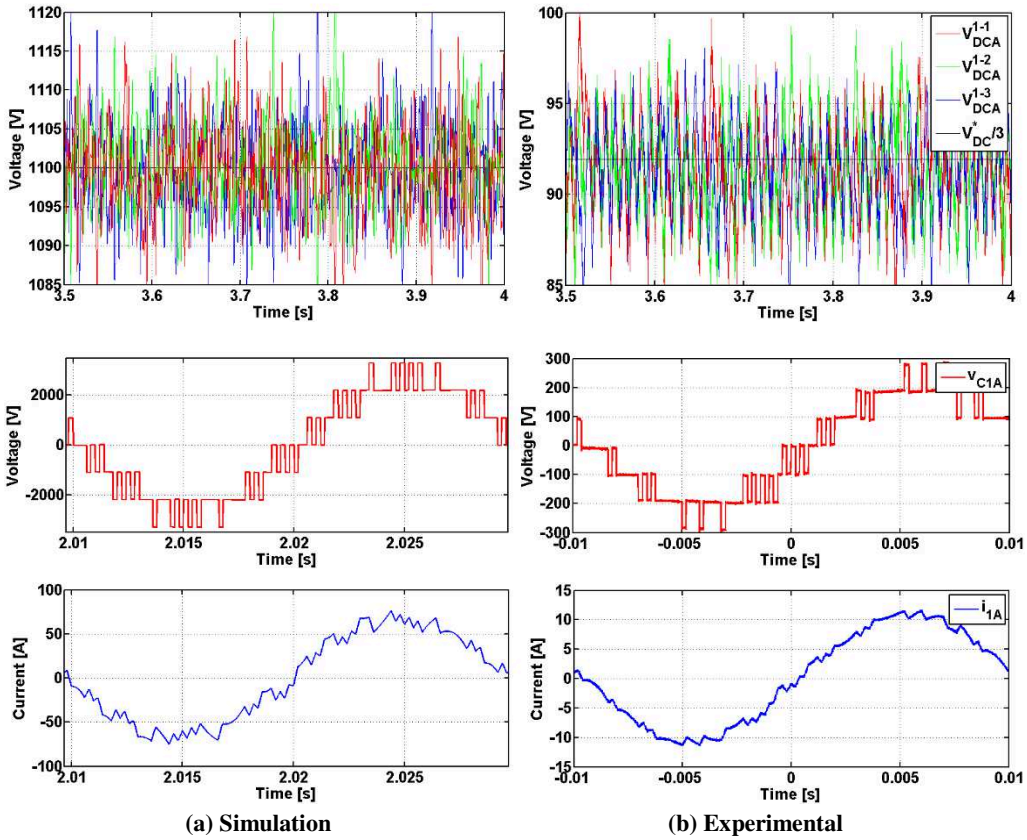


Figure 8.23 Comparison between experimental and simulation results for Model Predictive Control: DC-Link voltages, Converter voltage, AC voltage and current.

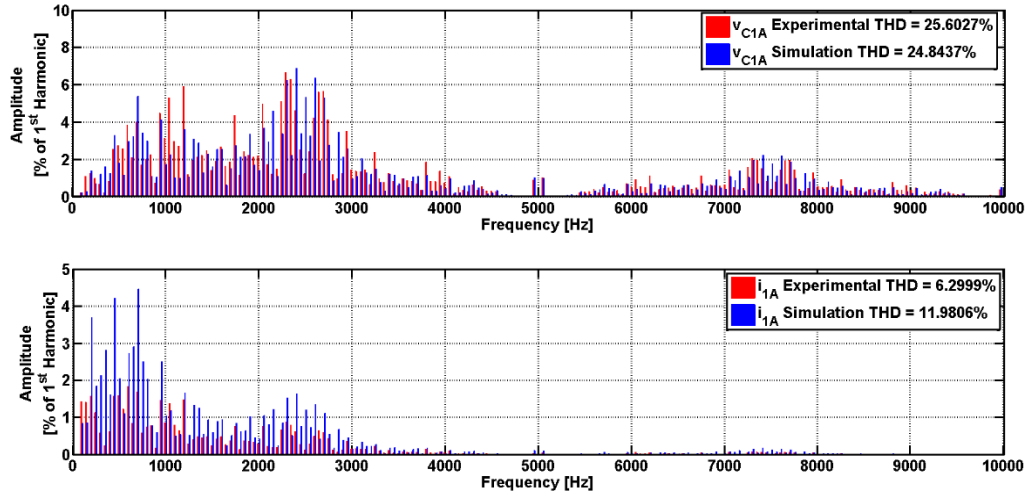


Figure 8.24 Comparison between experimental and simulation results for Model Predictive Control: Converter voltage and AC current harmonic content.

As it can be noted, DC-Link voltages, converter voltage and AC current on phase A, port 1 of the UNIFLEX-PM demonstrator present similar waveforms, with the only difference in the different operating point between simulation and experimental tests and the absence of a grid connection on port 2.

However the different operative points affects the amplitude of the AC current and, thus the filtering capability of the line inductance, considered of the same value in both simulation and experimental tests.

This results in the harmonic contents of Figure 8.24, where the converter voltage presents the classical MPC spectrum, with the harmonics widely spread over all the considered frequency range. On the other hand, the AC current spectrum presents a visible difference between simulation and experimental tests. In fact even if the converter voltage THD is higher in experimental tests than in simulation, the AC current THD results lower for the experimental tests, as a consequence of the different operative points.

8.5 Chapter Summary

In this chapter a MPC that includes in the cost function AC current and DC-Link voltage control is presented. In particular the traditional MPC current control derivation is described for the proposed system and MPC current / DC-Link voltage control is proposed; the control description includes the AC current and DC-Link voltage predictions and the DC-Link capacitors voltage balancing capability of the proposed control. The proposed control is able to effectively control the AC current on each phase whilst maintaining the DC-Link capacitor voltages balanced.

With respect to the classic MPC current control the proposed MPC does not need an external DC-Link voltage control; however it is still possible to actively regulate the DC-Link voltage on each capacitor since it is included in the control cost function.

Moreover, the constraints included in the proposed control reduce the required number of calculations, resulting in a lower computational weight with respect to the classical MPC implementation.

Simulation and experimental results has been carried out, considering the UNIFLEX-PM demonstrator SST topology; results shows that the control is able to operate effectively under several operating conditions providing a fast and accurate DC-Link voltage regulation.

However, the lack of a PWM technique and the inherent variable switching frequency of the MPC method affects the AC waveforms quality, resulting in a high value of the AC current THD, approximately double of the one obtained using the DBC described in Chapter 7.

Chapter 9
Modulated Model Predictive Control for a 2 port Solid State Transformer

In this chapter a novel control technique, named Modulated Model Predictive Control (M^2PC), is introduced with the aim to increase the performance of traditional Model Predictive Control.

The proposed controller takes into account the cost function value for different states of the converter introducing a suitable modulation scheme in the minimization algorithm. M^2PC allows retention of all the advantages of MPC as multi-objective control strategy, but produces an increased performance in terms of power quality.

The proposed control technique is described in detail, validated through simulation in Matlab/Simulink and experimental testing on the UNIFLEX-PM demonstrator, and represents one of the main contribution of this PhD work.

9.1 Modulated Model Predictive Control description

The Modulated Model Predictive Control (M^2PC) [182] includes a suitable modulation scheme in the cost function minimization of the MPC alghorithm. To avoid increasing the complexity of the controller, especially in the case of multi-objective cost functions, M^2PC method is based on the evaluation of the cost function for a selected number of states. In this thesis a modulation scheme particularly suitable for high power converters, and similar to the one used in DBC control is proposed, maintaining the previously described limitations and advantages for MPC. At every sampling period, only one leg of one H-Bridge is allowed to switch obtaining a total switching frequency of the CHB that is half of the sampling frequency.

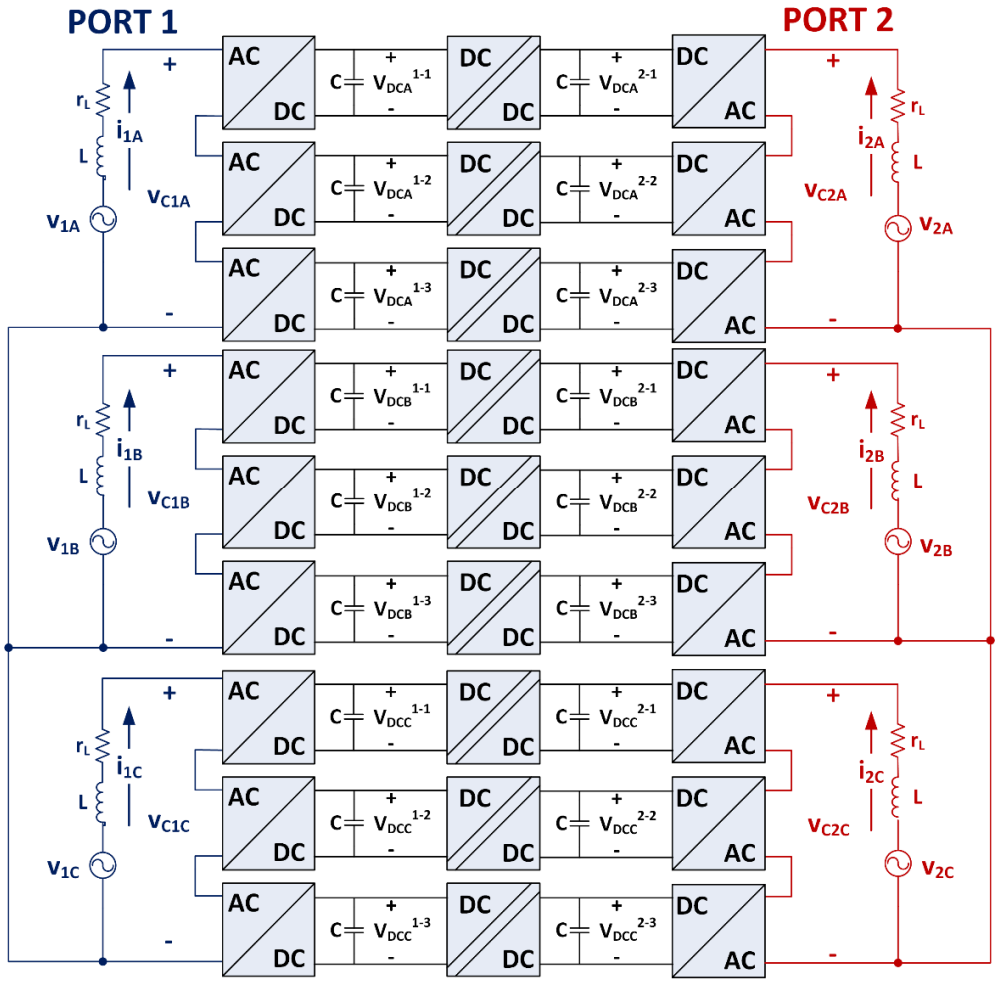


Figure 9.1 UNIFLEX-PM demonstrator two ports converter structure.

Moreover, as described for MPC in Chapter 8, the selected switching pattern helps to reduce the controller computational requirements. However, in the case of M^2PC the switching times are

calculated on the basis of the cost function values for the selected states, as described in the following sections. The M²PC control is derived for phase A, port 1 of the 7-Level CHB SST of Figure 9.1 and two different implementation of M²PC control are considered in this chapter: a double nested control loop including a DC-Link PI control and an M²PC current control and a single loop M²PC DC-Link voltage/current control. In the first case it is possible to appreciate the similarities between DBC and M²PC current control while, in the second case, the main advantages of M²PC with respect to DBC and MPC are highlighted.

The operating principle of the M²PC current control is shown in Figure 9.2 for a generic sampling instant t_k where the current prediction process and the switching times calculation are highlighted.

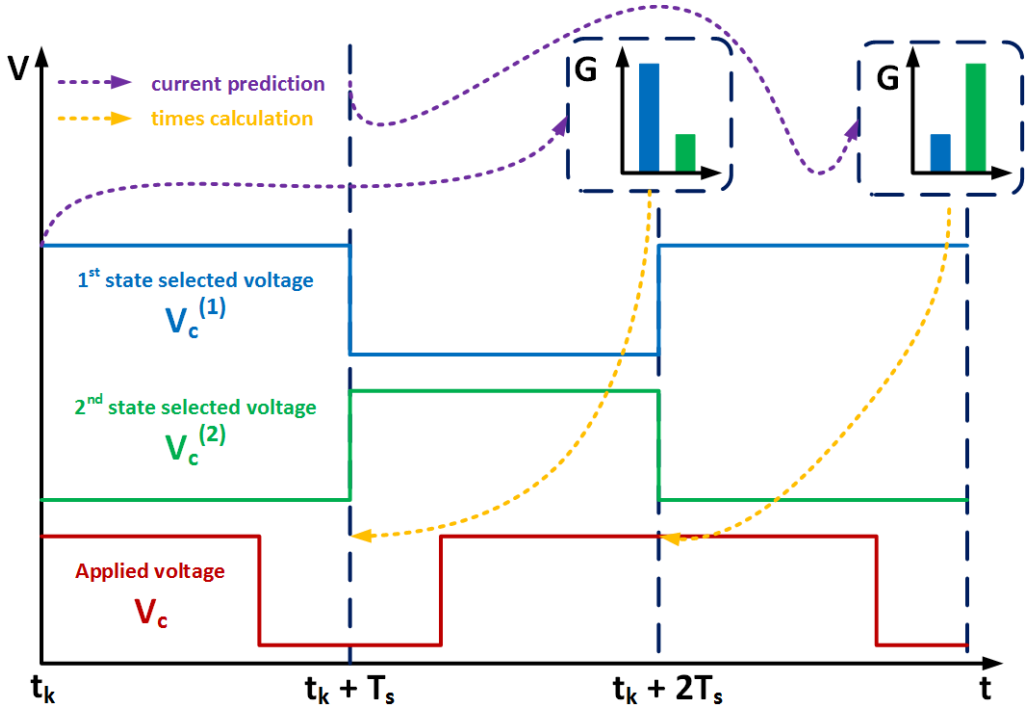


Figure 9.2 M²PC working principle.

At the time t_k the cost function is calculated for both the selected vectors $V_c^{(1)}$ and $V_c^{(2)}$. These vectors are applied at the time $t_k + T_s$ for an interval that is inversely proportional to the value of the related cost functions. Since the cost function associated with $V_c^{(2)}$ is lower than the one associated with $V_c^{(1)}$ in this example, $V_c^{(2)}$ is applied for a longer time with respect to $V_c^{(1)}$, in the time interval $t_k + T_s \ldots t_k + 2T_s$. Conversely, at the time $t_k + T_s$, the cost function associated with

$V_c^{(1)}$ is lower than the one associated with $V_c^{(2)}$ and $V_c^{(1)}$ is applied for a longer time with respect to $V_c^{(2)}$, in the time interval $t_k + T_s \ldots t_k + 2T_s$. As a result, the applied voltage V_c shows a pattern similar to the one obtained applying a modulation technique. It can be also noticed from Figure 9.2 that M^{2}PC operation is equivalent to two predictive current control operating in parallel, and applying actually to the converter a combination of these two predictive current control. In this case, in order to minimize the converter switching frequency, at the beginning of any sampling interval the last state applied at the previous sampling interval has been selected. However, the M^{2}PC working principle is applicable to any combination of converter states. The overall cost function that is going to be minimized with M^{2}PC is represented by the following equation:

$$G_{M2PC} = t_{1A}{}^{(1)} G_{1A}{}^{(1)} + t_{1A}{}^{(2)} G_{1A}{}^{(2)} \tag{9.1}$$

where $G_{IA}{}^{(1)}$, $G_{IA}{}^{(2)}$, $t_{IA}{}^{(1)}$ and $t_{IA}{}^{(2)}$ are the total cost functions and switching intervals, associated with the two selected vectors, on phase A, port 1 of the SST.

9.1.1 Modulated Model Predictive current control

The M^{2}PC current control scheme, resuming all the aforementioned characteristics, is shown in Figure 9.3. An external DC-Link voltage control loop is still necessary as shown in the block scheme to generate the appropriate current reference, highlighting some similarities between DBC+DCM and M^{2}PC current control. In particular it will be shown that if the switching times in M^{2}PC are chosen to be the optimal, the two control strategies achieve the same target under the same limitations, obtaining the same control performances.

Considering the converter model of Figure 9.4 described by equations (9.2) and (9.3), the discrete time model is determined, by the sampling instant t_k and the discrete time variable k.

$$v_{1A}(t) - v_{C1A}(t) = L\frac{di_{1A}(t)}{dt} - r_L i_{1A}(t) \tag{9.2}$$

$$v_{1A}(t_k) - v_{C1A}(t_k) = L\frac{di_{1A}(t)}{dt}\bigg|_{t=t_k} - r_L i_{1A}(t_k) \tag{9.3}$$

Where v_{IA} is the AC supply voltage, v_{C1A} is the voltage at the CHB output and i_{IA} is the AC current filtered by the inductor L with a leakage resistance r_L.

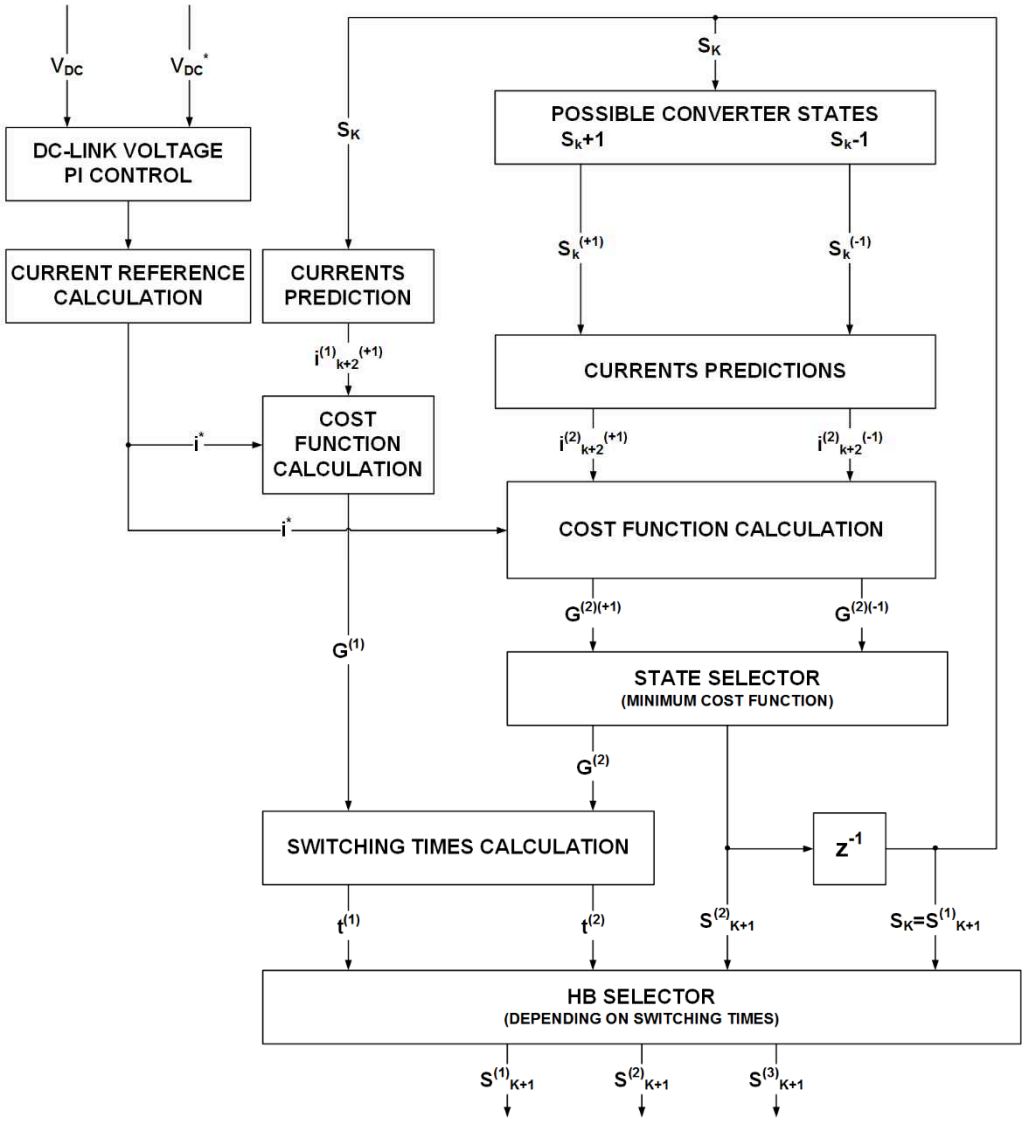


Figure 9.3 M²PC current control flowchart.

The time instant where the model is discretized has to take into account the real system limitations such as, for example, the intrinsic delay of one sampling interval T_s, introduced by the DSP.

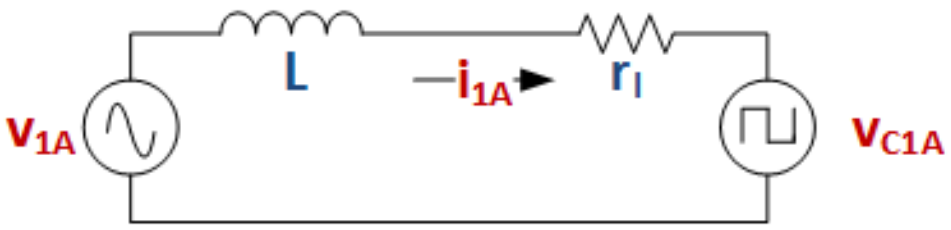


Figure 9.4 Equivalent AC circuit of the UNIFLEX-PM demonstrator, phase A, port 1.

In this case the 2nd order derivative discretization of (9.4) is applied to (9.3) obtaining the discrete time model in (9.5).

$$\left.\frac{di_{1A}(t)}{dt}\right|_{t=t_k} = \frac{i_{1A}(t_k + T_s) - i_{1A}(t_k - T_s)}{2T_s} \tag{9.4}$$

$$v_{1A}(t_k) - v_{C1A}(t_k) = \frac{L}{T_s}[i_{1A}(t_k + T_s) - i_{1A}(t_k - T_s)] - r_L i_{1A}(t_k) \tag{9.5}$$

At every sampling instant, two vectors are selected. The first vector $v_{c1A}{}^{(1)}$ applied to the converter is the same one applied at the end of the previous sampling interval as shown in (9.5):

$$v_{c1\mathrm{A}}{}^{(1)}(t_k + T_s) = v_{c1\mathrm{A}}{}^{(2)}(t_k) \tag{9.6}$$

A two step ahead current prediction is then calculated for the vector $v_{c1A}{}^{(1)}$ as follows.

$$i_{1\mathrm{A}}{}^{(1)}(t_k + 2T_s) = i_{1\mathrm{A}}(t_k) - \frac{2T_s r_L}{L} i_{1\mathrm{A}}(t_k + T_s) + \frac{2T_s}{L}\left[v_{1\mathrm{A}}(t_k + T_s) - v_{c1\mathrm{A}}{}^{(1)}(t_k + T_s)\right] \tag{9.7}$$

Considering the control working properly with an optimal current tracking, it is possible to approximate the term related with the inductor resistance r_L using the current reference instead of the current prediction at the instant $t_k + T_s$, incurring in a negligible error. The following current prediction is obtained in (9.8) and the relative cost function is calculated in (9.9).

$$i_{1\mathrm{A}}{}^{(1)}(t_k + 2T_s) = i_{1\mathrm{A}}(t_k) - \frac{2T_s r_L}{L} i_{1\mathrm{A}}{}^{*}(t_k + T_s) + \frac{2T_s}{L}\left[v_{1\mathrm{A}}(t_k + T_s) - v_{c1\mathrm{A}}{}^{(1)}(t_k + T_s)\right] \tag{9.8}$$

$$G_{1A}{}^{(1)} = \left|i_{1\mathrm{A}}{}^{(1)}(t_k + 2T_s) - i_{1\mathrm{A}}{}^{*}(t_k + 2T_s)\right| \tag{9.9}$$

The second vector $v_{c1A}{}^{(2)}$ is chosen between the two vectors adjacent to $v_{c1A}{}^{(1)}$, on the basis of the current predictions of (9.10) and (9.11) and, using the same approximation applied to $v_{c1A}{}^{(1)}$, the vector that minimises the cost function of (9.12) is selected.

$$i_{1\mathrm{A}}{}^{(2)}(t_k + 2T_s) = i_{1\mathrm{A}}(t_k) - \frac{2T_s r_L}{L} i_{1\mathrm{A}}(t_k + T_s) + \frac{2T_s}{L}\left[v_{1\mathrm{A}}(t_k + T_s) - v_{c1\mathrm{A}}{}^{(2)}(t_k + T_s)\right] \tag{9.10}$$

$$i_{1\mathrm{A}}{}^{(2)}(t_k + 2T_s) = i_{1\mathrm{A}}(t_k) - \frac{2T_s r_L}{L} i_{1\mathrm{A}}{}^{*}(t_k + T_s) + \frac{2T_s}{L}\left[v_{1\mathrm{A}}(t_k + T_s) - v_{c1\mathrm{A}}{}^{(2)}(t_k + T_s)\right] \tag{9.11}$$

$$G_{1A}{}^{(2)} = \left|i_{1\mathrm{A}}{}^{(2)}(t_k + 2T_s) - i^{*}{}_{1\mathrm{A}}(t_k + 2T_s)\right| \tag{9.12}$$

The proposed selection method for the second vector has two major advantages: it reduces the complexity of the controller and reduces the device switching frequency. In fact, the next H-Bridge to switch is selected in order to maintain the DC-Link voltage balanced and distribute the commutations amongst the cells, on the basis of the principles of the DCM modulator, making the control suitable for high power applications. The switching times for the two selected vectors are calculated by solving the following linear system of equations:

$$\begin{cases} {t_{1A}}^{(1)} = \dfrac{K_{1A}}{{G_{1A}}^{(1)}} \\ {t_{1A}}^{(2)} = \dfrac{K_{1A}}{{G_{1A}}^{(2)}} \\ {t_{1A}}^{(1)} + {t_{1A}}^{(2)} = T_s \end{cases} \tag{9.13}$$

Once the value of K_{IA} is obtained from (9.12), the following expressions for the switching times are obtained.

$${t_{1A}}^{(1)} = T_s \frac{{G_{1A}}^{(2)}}{{G_{1A}}^{(1)} + {G_{1A}}^{(2)}} \tag{9.14}$$

$${t_{1A}}^{(2)} = T_s \frac{{G_{1A}}^{(1)}}{{G_{1A}}^{(1)} + {G_{1A}}^{(2)}} \tag{9.15}$$

Equations (9.14) and (9.15) represent a sub-optimal solution for the vector application times based on empirical considerations about the current error related to the control. In fact in this case it is not possible to calculate the optimal value of ${t_{IA}}^{(1)}$ and ${t_{IA}}^{(2)}$ that minimize the cost function as done in previous works.

However it is possible to demonstrate that the current error for MPC is higher compared to M^{2}PC. In MPC current control, the current error in one sampling interval is equal to the following cost function.

$$G_{MPC} = {G_{1A}}^{(1)} \tag{9.16}$$

While in M^{2}PC the current error can be approximated as in (9.17), considering $T_s << 1$. In fact for small values of Ts the current error in one sampling interval can be considered equal to the average of the errors produced by the two applied states, weighted by the calculated states duty cycles.

$$G_{M2PC} \cong \frac{t_{1A}{}^{(1)} G_{1A}{}^{(1)} + t_{1A}{}^{(2)} G_{1A}{}^{(2)}}{2T_s} \tag{9.17}$$

In fact $G_{IA}{}^{(1)}$ and $G_{IA}{}^{(2)}$ represent the error committed if the associated states are applied for the whole sampling interval. Substituting (7.14) and (7.15) in (7.17) the following expression is obtained.

$$G_{M2PC} = \frac{G_{1A}{}^{(1)} G_{1A}{}^{(2)}}{G_{1A}{}^{(1)} + G_{1A}{}^{(2)}} < G_{1A}{}^{(1)} \tag{9.18}$$

Looking at (9.18) it can be stated that M^{2}PC produce a current error in one sampling interval that is always lower than the error produced by the classic MPC current control:

$$G_{M2PC} < G_{MPC} \tag{9.19}$$

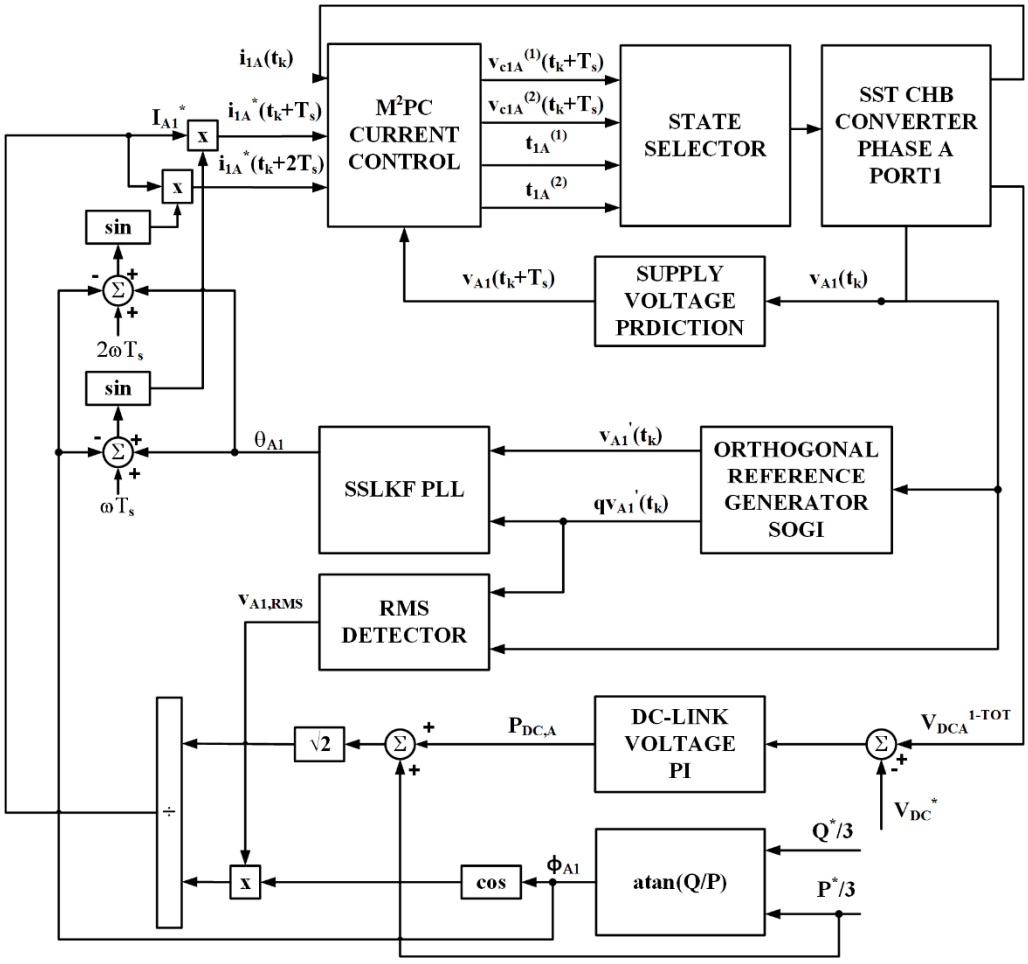


Figure 9.5 M^{2}PC current control overall control scheme.

The overall M²PC current control block scheme is shown in Figure 9.5. It includes the M²PC inner AC current control loop and the outer DC link voltage PI control loop; in particular the latter is able to set the DC-Link voltage at the required reference voltage and hence allow the desired power flow, defined by the active and reactive power reference P^*, Q^*. This block scheme is similar to the one of Figure 7.7, implemented for the DBC control. The power is considered equally shared among the three phases and for this reason the power references are divided by three on each phase.

The AC current reference is calculated on the basis of the total required active and reactive power, P^*, Q^*, the active power required to regulate the total DC-Link voltage on the primary side of the SST, $P_{DC,A}$, and the angle and RMS value of the AC voltage, respectively θ_{A1}, and $V_{A1,RMS}$.

$$\varphi_{A1} = atan\left(\frac{\frac{P^*}{3} + P_{DC,A}}{Q^*}\right) \tag{9.20}$$

$$i_{1A}{}^*(t_k + iT_s) = \frac{{}^{P^*}\!/_3 + P_{DC,A}}{\cos(\varphi_{A1})\, V_{A1,rms}\sqrt{2}} sin(\theta + iT_s - \varphi_{A1}) \quad , \quad i = 1{,}2 \tag{9.21}$$

The design of the PI controller is described in Appendix B while the single phase SSLKF PLL/SOGI and the RMS detector have already been described in Chapter 4. The supply voltage prediction is here also needed and it is implemented using the method described in Appendix A.

9.1.2 Modulated Model Predictive DC-Link voltage / current control

In this case the M²PC current control described in the previous paragraph is used in combination with a predictive DC-Link voltage controller; the control block diagram of the complete strategy is shown in Figure 9.6. As for M²PC current control the converter model of Figure 9.4 is considered for the control algorithm description. At every sampling instant, two voltage vectors are selected by the control routine. The first selected vector, $v_{c1A}{}^{(1)}$, is the same one applied to the converter at the end of the previous sampling interval, while the second selected vector,$v_{c1A}{}^{(2)}$, is chosen between the two vectors adjacent to $v_{c1A}{}^{(1)}$.

$$v_{c1\mathrm{A}}{}^{(1)}(t_k + T_s) = v_{c1\mathrm{A}}{}^{(2)}(t_k) \tag{9.22}$$

$$v_{c1\mathrm{A}}{}^{(2)}(t_k + T_s) = v_{c1\mathrm{A}}{}^{(1)}(t_k + T_s) \pm \frac{V_{DC,A}(t_k)}{3} \tag{9.23}$$

The vector application times are calculated on the basis of the cost functions values related with $v_{c1A}{}^{(1)}$ and the selected $v_{c1A}{}^{(2)}$.

$$t_{1A}{}^{(1)} = T_s \frac{G_{1A}{}^{(2)}}{G_{1A}{}^{(1)} + G_{1A}{}^{(2)}} \tag{9.24}$$

$$t_{1A}{}^{(2)} = T_s \frac{G_{1A}{}^{(1)}}{G_{1A}{}^{(1)} + G_{1A}{}^{(2)}} \tag{9.25}$$

In this case the cost functions are no more represented by just the current error since they are composed by a linear combination of current and DC-Link voltage error.

$$G_{1A}{}^{(1)} = w_I \cdot G_{I1A}{}^{(1)} + w_V \cdot G_{V1A}{}^{(1)} \tag{9.26}$$

$$G_{1A}{}^{(2)} = w_I \cdot G_{I1A}{}^{(2)} + w_V \cdot G_{V1A}{}^{(2)} \tag{9.27}$$

$G_{I,1A}{}^{(1)}$ and $G_{VDC,1A}{}^{(1)}$ represent, respectively, the current and the DC-Link voltage error committed by applying $v_{c1A}{}^{(1)}$ for the whole sampling interval. In the same way, $G_{I,1A}{}^{(2)}$ and $G_{VDC,1A}{}^{(2)}$ represent, respectively the current and the DC-Link voltage error committed by applying $v_{c1A}{}^{(2)}$ for the whole sampling interval. The calculation of the cost functions is described in the following paragraphs.

9.1.2.1 M²PC DC-Link voltage/current control: current control

The current control is exactly the same as the one described in section 9.1.1. It is based on the two step ahead current prediction for the two converter voltage states $v_{c1A}{}^{(1)}$ and $v_{c1A}{}^{(2)}$, calculated as in (9.28) and (9.29). The associated cost functions, are then defined by (9.30) and (9.31).

$$i_{1\mathrm{A}}{}^{(1)}(t_k + 2T_s) = i_{1\mathrm{A}}(t_k) - \frac{2T_s r_L}{L} i_{1\mathrm{A}}{}^{*}(t_k + T_s) + \frac{2T_s}{L}\left[v_{1\mathrm{A}}(t_k + T_s) - v_{c1\mathrm{A}}{}^{(1)}(t_k + T_s)\right] \tag{9.28}$$

$$i_{1\mathrm{A}}{}^{(2)}(t_k + 2T_s) = i_{1\mathrm{A}}(t_k) - \frac{2T_s r_L}{L} i_{1\mathrm{A}}{}^{*}(t_k + T_s) + \frac{2T_s}{L}\left[v_{1\mathrm{A}}(t_k + T_s) - v_{c1\mathrm{A}}{}^{(2)}(t_k + T_s)\right] \tag{9.29}$$

$$G_{I1A}{}^{(1)} = \left|i_{1\mathrm{A}}{}^{(1)}(t_k + 2T_s) - i_{1\mathrm{A}}{}^{*}(t_k + 2T_s)\right| \tag{9.30}$$

$$G_{I1A}{}^{(2)} = \left|i_{1\mathrm{A}}{}^{(2)}(t_k + 2T_s) - i_{1\mathrm{A}}{}^{*}(t_k + 2T_s)\right| \tag{9.31}$$

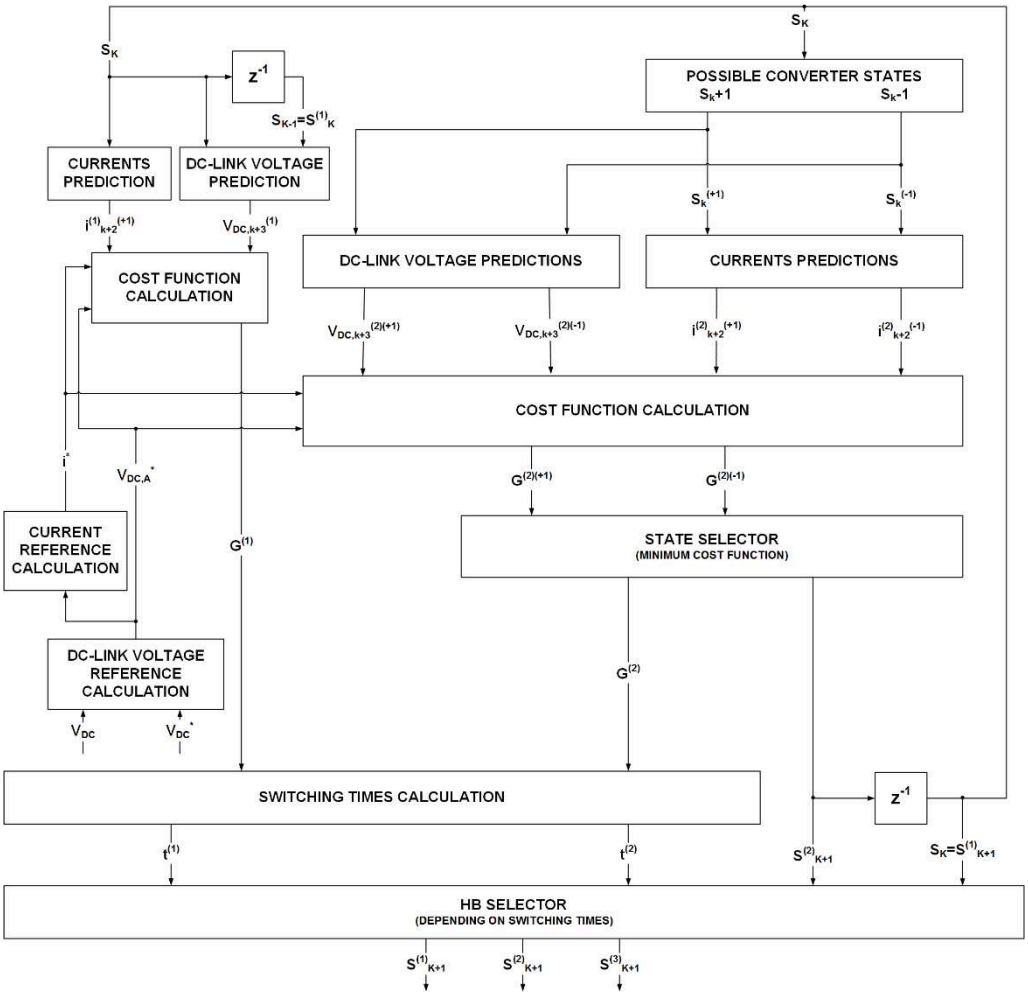


Figure 9.6 M²PC DC-Link voltage/current control flowchart.

9.1.2.2 M²PC DC-Link voltage/current control: DC-Link voltage control

Referring to Figure 9.7 the dynamics of the DC side of the converter is modelled as in Chapter 8, neglecting the presence of the DC-DC converter.

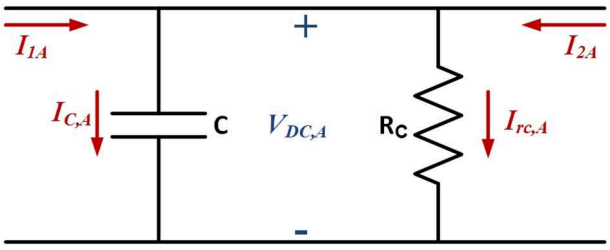


Figure 9.7 DC equivalent circuit for phase A.

The current equation that describes the circuit of Figure 9.7 is the following. Thus, the following approximated model of the DC side of the converter is obtained.

$$C\frac{dV_{DCA}(t)}{dt} = \frac{v_{C1A}(t)}{V_{DCA}(t)}[i_{1A}(t) - {i_{1A}}^{*}(t)] \tag{9.32}$$

The DC-Link voltages are sampled at the same time instant of the currents in order to maintain the voltage control synchronous with the current control. Integrating equation (9.32) between t_k and $t_k + T_s$ the following relations of (9.33) and (9.34) are obtained.

$$C\int_{V_{DCA}(t_k)}^{V_{DCA}(t_k+T_S)} dV_{DCA}(t) = \int_{t_k}^{t_k+T_s} \frac{v_{C1A}(t)}{V_{DCA}(t)}[i_{1A}(t) - {i_{1A}}^{*}(t)]\,dt \tag{9.33}$$

$$V_{DCA}(t_k + T_s) - V_{DCA}(t_k) = \frac{1}{C}\int_{t_k}^{t_k+T_s} \frac{v_{C1A}(t)}{V_{DCA}(t)}[i_{1A}(t) - {i_{1A}}^{*}(t)]\,dt \tag{9.34}$$

In order to solve the integral in (9.34) the average values of the time domain quantities during one sampling interval are considered instead of the instantaneous values obtaining the approximation of (9.35).

$$\int_{t_k}^{t_k+T_s} \frac{v_{C1A}(t)}{V_{DCA}(t)}[i_{1A}(t) - {i_{1A}}^{*}(t)]\,dt \cong T_s \frac{{v_{C1A}}^{avg}(t_k)}{{V_{DCA}}^{avg}(t_k)}\left[{i_{1A}}^{avg}(t_k) - {i_{1A}}^{*avg}(t_k)\right] \tag{9.35}$$

Assuming small DC-Link voltage variations during one sampling interval, the average value of DC-Link voltage is considered to be equal to its value at the instant t_k.

$${V_{DC,A}}^{avg}(t_k) \cong V_{DCA}(t_k) \tag{9.36}$$

The main difference between M^{2}PC and MPC is that, in the case of M^{2}PC, the average converter voltages and currents during a sampling interval are considered. In M^{2}PC two voltage vectors are applied during a sampling interval, therefore the converter voltage average value is equal to the expression of (9.37).

$${v_{C1A}}^{avg}(t_k) = {t_{1A}}^{(1)}(t_k){v_{C1A}}^{(1)}(t_k) + {t_{1A}}^{(2)}(t_k){v_{C1A}}^{(2)}(t_k) \tag{9.37}$$

For the same reason the average current produced in one sampling interval is considered equal to the current sampled at the end of the sampling interval.

$${i_{1A}}^{avg}(t_k) = i_{1A}(t_k + T_s) \tag{9.38}$$

$${i_{1A}}^{*avg}(t_k) = {i_{1A}}^{*}(t_k + T_s) \tag{9.39}$$

Substituting (9.35)-(9.39) in (9.34) the one step ahead DC-Link voltage prediction is obtained.

$$V_{DCA}(t_k + T_s) = V_{DCA}(t_k) + \frac{T_s}{C}\frac{v_{C1A}{}^{avg}(t_k)}{V_{DCA}(t_k)}[i_{1A}(t_k + T_s) - i_{1A}{}^{*}(t_k + T_s)] \quad (9.40)$$

The two step ahead DC-Link voltage prediction is calculated, at the time instant t_k+2T_s, for the two voltage vectors that wants to be generated during the next sampling interval.

$$V_{DCA}{}^{(1)}(t_k + 2T_s) = V_{DCA}(t_k + T_s) + \frac{T_s}{C}\frac{v_{C1A}{}^{(1)}(t_k + T_s)}{V_{DCA}(t_k + T_s)}\left[i_{1A}{}^{(1)}(t_k + 2T_s) - i_{1A}{}^{*}(t_k + 2T_s)\right] \quad (9.41)$$

$$V_{DCA}{}^{(2)}(t_k + 2T_s) = V_{DCA}(t_k + T_s) + \frac{T_s}{C}\frac{v_{C1A}{}^{(2)}(t_k + T_s)}{V_{DCA}(t_k + T_s)}\left[i_{1A}{}^{(2)}(t_k + 2T_s) - i_{1A}{}^{*}(t_k + 2T_s)\right] \quad (9.42)$$

Considering the DC-Link voltage well regulated by the control, it is possible to make a further approximation on the converter voltage, using the following relation between converter state and produced converter voltage.

$$s_{1A}(t_k) = \frac{v_{C1A}(t_k)}{V_{DCA}(t_k)} \quad (9.43)$$

Applying (9.43) to (9.41) and (9.42) the final expression of the DC-Link voltage prediction is obtained.

$$V_{DCA}{}^{(1)}(t_k + 2T_s) = V_{DCA}(t_k + T_s) + \frac{T_s}{C}s_{1A}{}^{(1)}(t_k + T_s)\left[i_{1A}{}^{(1)}(t_k + 2T_s) - i_{1A}{}^{*}(t_k + 2T_s)\right] \quad (9.44)$$

$$V_{DCA}{}^{(2)}(t_k + 2T_s) = V_{DCA}(t_k + T_s) + \frac{T_s}{C}s_{1A}{}^{(2)}(t_k + T_s)\left[i_{1A}{}^{(2)}(t_k + 2T_s) - i_{1A}{}^{*}(t_k + 2T_s)\right] \quad (9.45)$$

The cost functions associated with $v_{c1A}{}^{(1)}$ and $v_{c1A}{}^{(2)}$ are then calculated also for the DC-Link voltage as follows.

$$G_{V1A}{}^{(1)} = \left|V_{DCA}{}^{(1)}(t_k + 2T_s) - V_{DCA}{}^{*}(t_k)\right| \quad (9.46)$$

$$G_{V1A}{}^{(2)} = \left|V_{DCA}{}^{(2)}(t_k + 2T_s) - V_{DCA}{}^{*}(t_k)\right| \quad (9.47)$$

9.1.2.3 Overall M²PC DC-Link voltage/current control scheme

The next step is to derive an expression for the system AC reference current. Starting from the DC model of Figure 9.7, the current reference calculation considers the variation of energy stored in the capacitors in order to provide the necessary amount of power to regulate the DC-Link

voltage to the desired value according to the following equation, considering the power balanced between the phases:

$$\frac{P_1(t)}{3} + \frac{P_2(t)}{3} = \frac{1}{2} C \frac{dV_{DC,A}(t)^2}{dt} \tag{9.48}$$

In (9.48) P_1 is considered equal to desired active power reference P_1^* plus the variation of power necessary to maintain the capacitor charged at the desired DC-Link voltage, while P_2 is considered equal to the desired active power reference P_2^*.

$$\frac{P_1(t)}{3} = \frac{P_1^*}{3} + \frac{dP_{DC,A}(t)}{dt} \tag{9.49}$$

$$\frac{P_2(t)}{3} = \frac{P_2^*}{3} \tag{9.50}$$

Substituting (9.49) and (9.50) in (9.48) and considering the balance between the requested power on the two sides of the converter, the following expressions are obtained:

$$\frac{P_1^*}{3} + \frac{P_2^*}{3} = 0 \tag{9.51}$$

$$\frac{dP_{DCA}(t)}{dt} = \frac{1}{2} C \frac{dV_{DCA}(t)^2}{dt} \tag{9.52}$$

Integrating (9.51) between t_k and t_k+T_s and imposing the DC-Link voltage at the next sampling interval equal to desired DC-Link voltage reference $V_{DC,A}^*$, equation (9.53) is obtained. It calculates the energy necessary to maintain the DC-link voltage well regulated for one sampling period:

$$V_{DC,A}(t_k + T_s) = V_{DCA}^*(t_k) \tag{9.53}$$

$$P_{DCA}(t_k + T_s) = P_{DCA}(t_k) + \frac{1}{2} C \left[V_{DCA}^{*2}(t_k) - V_{DCA}^2(t_k) \right] \tag{9.54}$$

It is important to notice that equation (9.54) does not consider any losses in the DC circuit, modelled by R_c in Figure 9.7, and the steady state error is reduced using the DC-Link voltage control in the predictive algorithm. $P_{DC,A}$ is then used to calculate the current reference as follows:

$$\varphi_{A1} = atan\left(\frac{P^*/_3 + P_{DCA}}{Q^*} \right) \tag{9.55}$$

$$i_{1A,AC}{}^{*}(t_k + iT_s) = \frac{P^{*}/_3 + P_{DCA}}{\cos(\varphi_{A1})\, V_{A1,rms}\sqrt{2}} sin(\theta_{1A} + iT_s - \varphi_{A1}) \quad , \quad i = 1{,}2 \quad (9.56)$$

The DC-Link voltage reference calculation it is limited by a ramp variation in order not to affect the dynamics of the current control and avoid undesired distortion on the grid current.

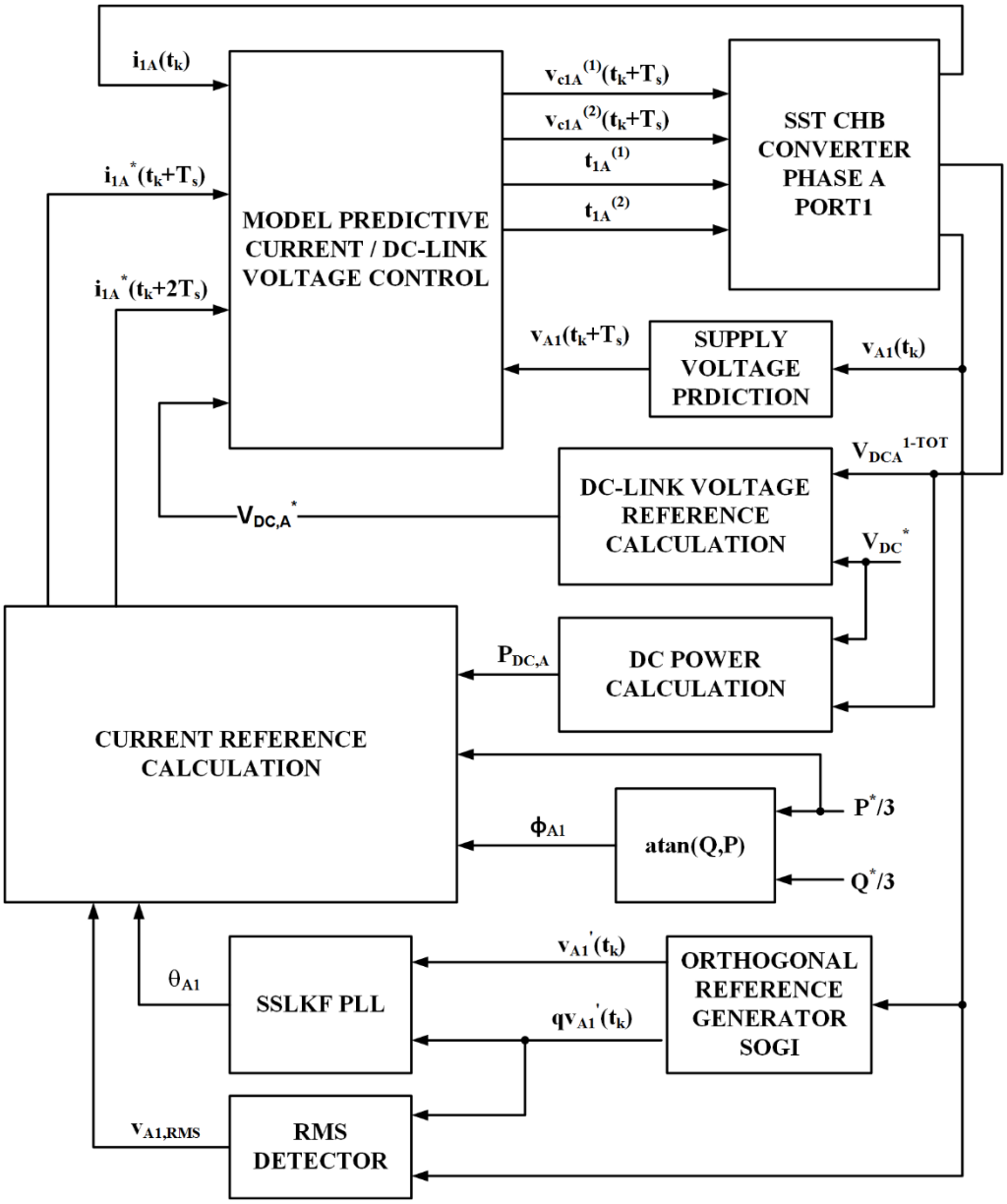


Figure 9.8 M²PC DC-Link voltage/current control overall block scheme.

A factor *N*, representing the DC-Link voltage reference horizon, is used for this purpose.

$$V_{DCA}{}^{*}(t_k) = V_{DC}{}^{*} + \frac{V_{DC}{}^{*} - V_{DCA}(t_k)}{N} \quad (9.57)$$

The overall control scheme for the converter is shown in Figure 9.8 where the modulation scheme is integrated in the controller as described above.

Once the converter state and switching instants are calculated by M^2PC, a combination of the HBs states is applied to produce the desired converter state. The HB selected to switch is determined by a set of iterative rules, as for DBC and MPC, with the aim of maintaining the voltage on the DC-Link capacitors balanced, distribute the commutations amongst the HBs and reduce the overall switching frequency. In particular, among all the HBs that can produce the desired converter voltage, the one that respect the following rules is chosen to be switched:

- Only one leg of one HB is allowed to switch, if necessary, at every switching instant.
- If the DC-Link voltages are unbalanced, the HB with the larger unbalance and that is able to reduce it by changing its state, is selected to switch.
- If the DC-Link voltages are well balanced or is not possible to reduce the unbalance by applying the desired converter state, the HB that commutated less in the past switching instants is chosen to be switched.

It can be noticed that the M^2PC state selector follow the same rules of the DCM modulator with active voltage balancing algorithm, described in Chapter 6 and differs only in the switching instant calculation that is directly implemented in the cost function minimization algorithm.

9.2 Simulation results for the Modulated Model Predictive Control on the Universal and Flexible Power Management demonstrator

Simulation tests of M^{2}PC current and current/DC-Link voltage control have been carried out for the SST converter of Figure 9.1. The simulation parameters are set to be equal to the UNIFLEX-PM demonstrator rated parameter of Table 3.1 and Table 9.1, with the exception of the DC-Link voltage reference, set to 3600V. It results in a DC-Link voltage on each capacitor of 1200V.

Table 9.1 M^{2}PC simulation parameters.

Name	*Description*	*Value*
N	DC-Link voltage reference horizon	100
w_I	Current control weighting factor	1
w_V	DC voltage control weighting factor	5
R_c	Equivalent DC-Link resistance	1kΩ

9.2.1 Modulated Model Predictive current control

Figure 9.9 shows the active and reactive power tracking using M^{2}PC current control when power variations are considered while Figure 9.10 shows the DC-Link voltages regulation. It is possible to notice that the DC-Link voltages shows a dynamics similar to the one obtained with DBC. In fact, during power references variations, the slow PI controller response affects the DC voltage tracking with variations on each phase of around 2.1% of the nominal value. Moreover using the M^{2}PC current control, since an active DC-Link voltage balancing algorithm is implemented in the modulator, the DC voltage on each capacitor of each phase is maintained balanced with oscillation of 2.1% of the nominal value.

Looking at Figure 9.11, Figure 9.12, Figure 9.13 and Figure 9.14, M^{2}PC produces sinusoidal AC currents with minimal harmonic distortions, achieving results comparable to DBC. In Figure 9.11 and Figure 9.12 an active power step of 250kW is applied and the control react with a fast response but producing higher transient oscillations, compared to DBC and MPC. In Figure 9.13 and Figure 9.14 a reactive power step from 50kVAR to -50kVAR is applied; also in this case M^{2}PC control provides a fast current tracking and it can be highlighted that using M^{2}PC current control an intrinsic PWM scheme, is implemented and the current ripple is reduced. In both Figure 9.12 and Figure 9.14 it is possible to see that a fast response to active and reactive power

reference variation is achieved with M^{2}PC and the phase current presents a ripple comparable to the one achieved by DBC.

Looking at Figure 9.15, it is clear that the switching frequency of M^{2}PC is constant to a value of 2.5kHz, as for DBC, producing an harmonic content on the converter voltages with a THD of approximately 24%. Being the harmonics produced by the converter mainly located around the switching frequency and its multiple, they are largely filtered by the line inductance resulting in a THD of 4.7% for the AC currents.

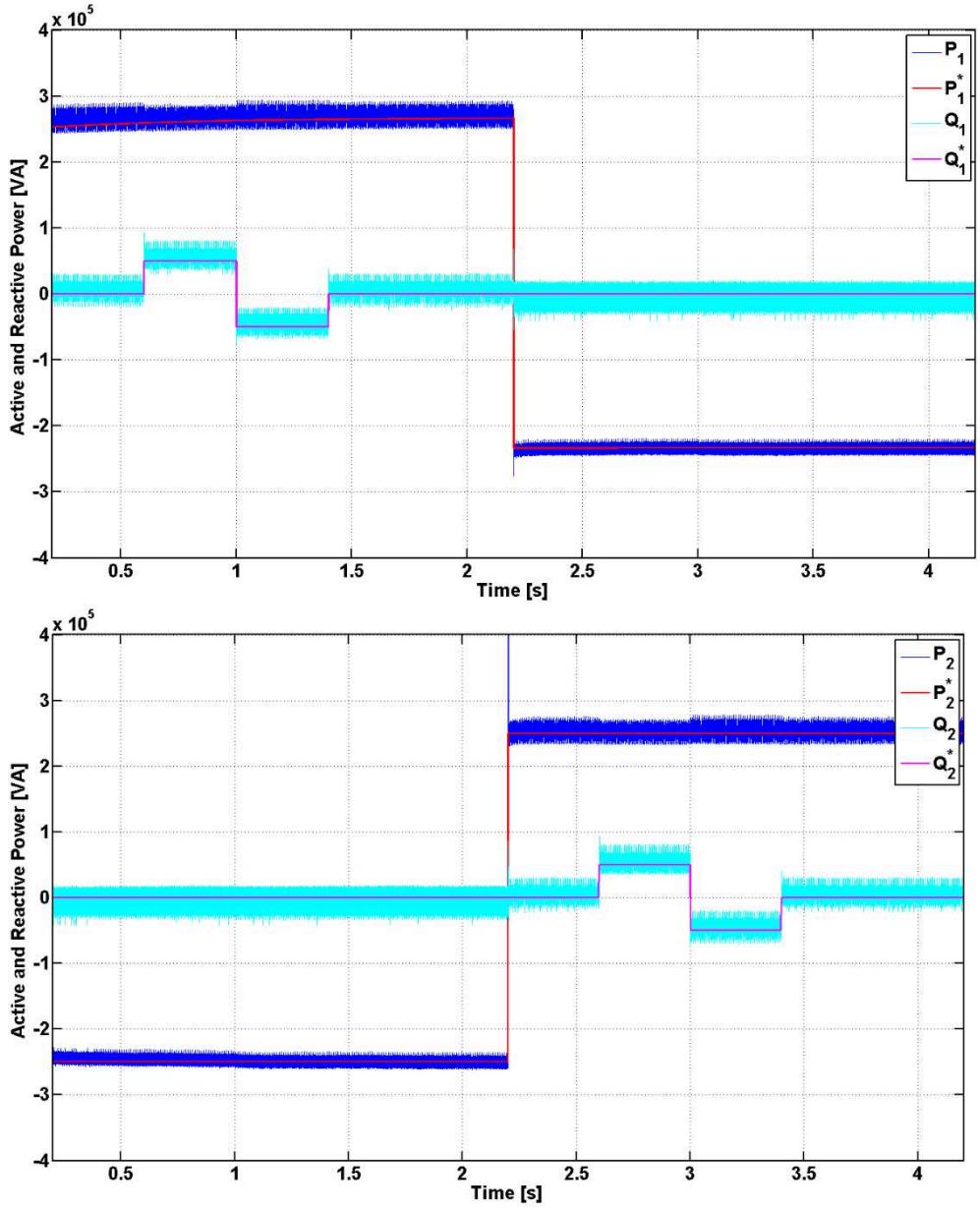


Figure 9.9 M^{2}PC current control simulation for UNIFLEX-PM SST converter: active and reactive power flow vs references on the two SST sides.

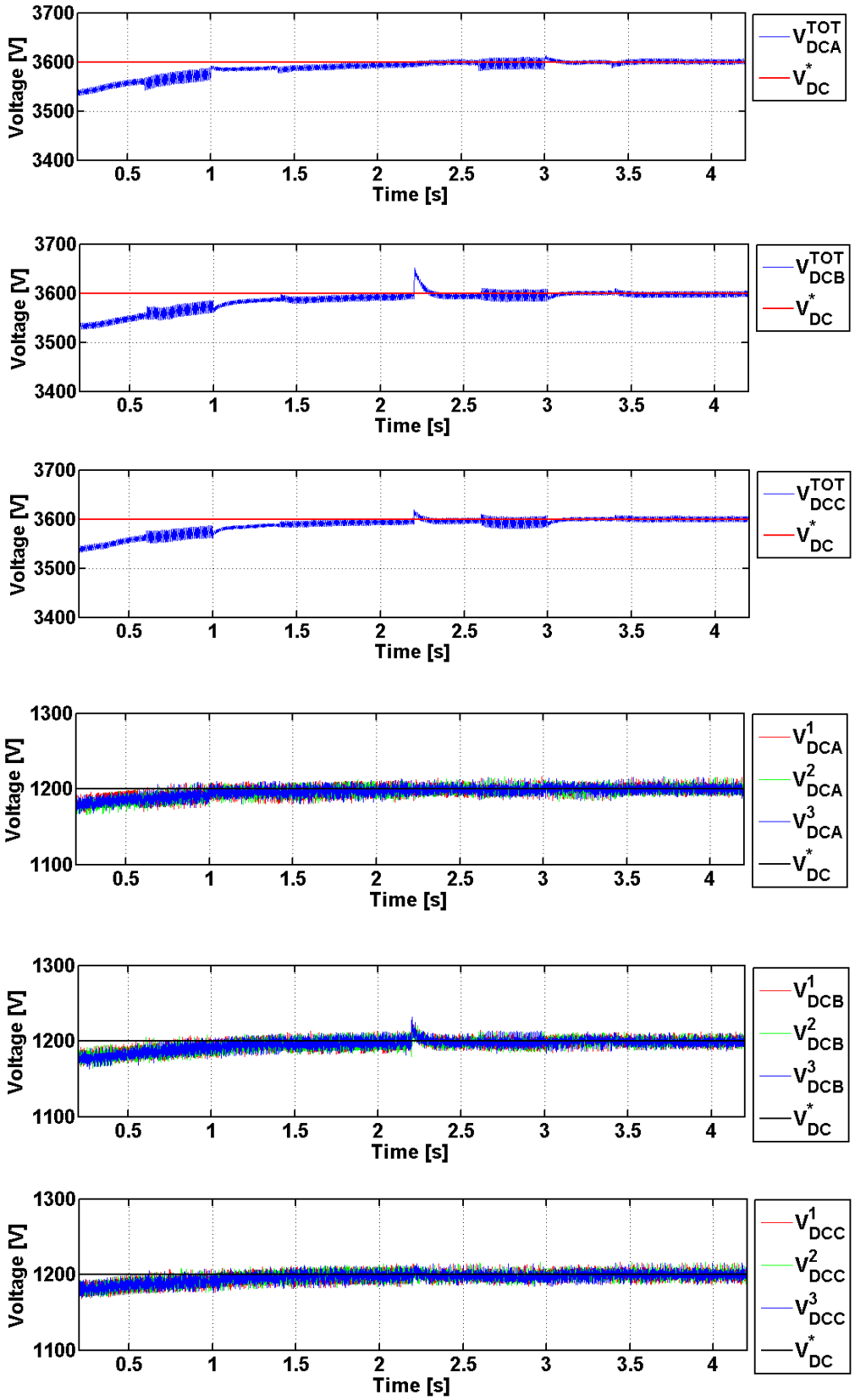


Figure 9.10 M²PC current control simulation for UNIFLEX-PM SST converter: total DC-Link voltages on each phase vs DC-Link voltage reference and single DC-Link capacitors voltages.

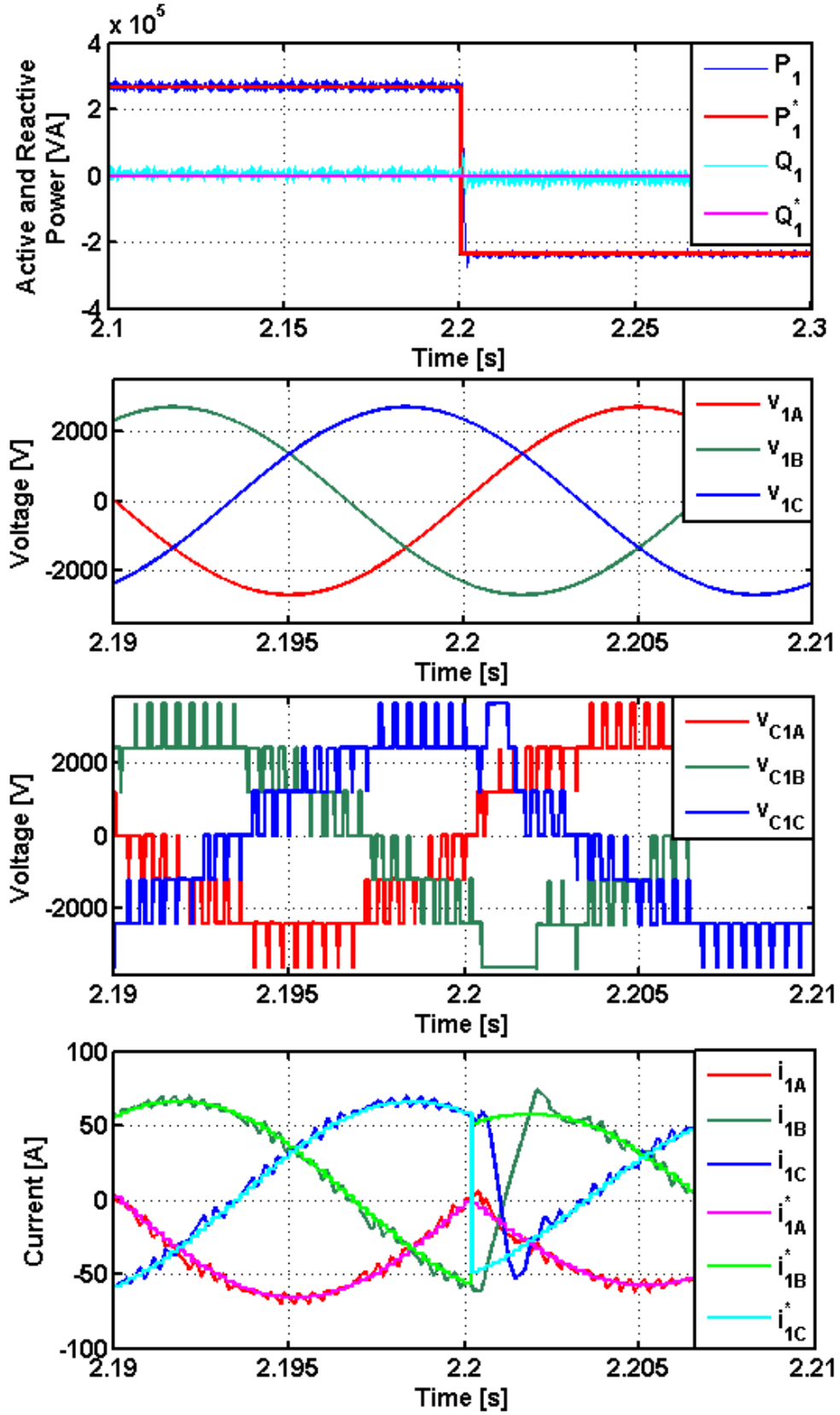


Figure 9.11 M²PC current control simulation for UNIFLEX-PM SST converter: grid voltage, converter voltage and AC current vs current reference on the three phases of both side of the SST converter when an active power reference step from 250kW to -250kW is applied on port 1 at time2.2s.

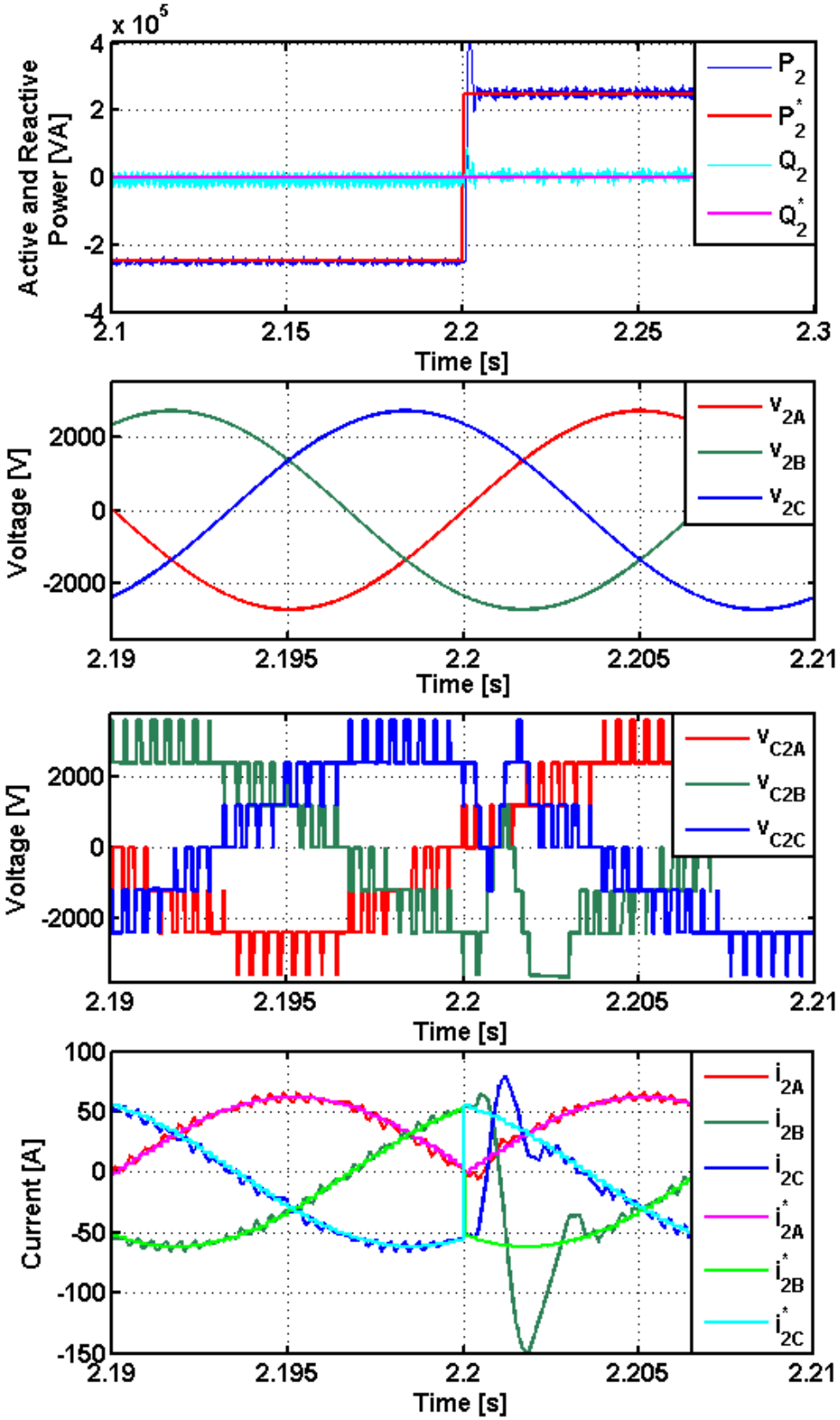


Figure 9.12 M²PC current control simulation for UNIFLEX-PM SST converter: grid voltage, converter voltage and AC current vs current reference on the three phases of both side of the SST converter when an active power reference step from -250kW to 250kW is applied on port 2 at time2.2s.

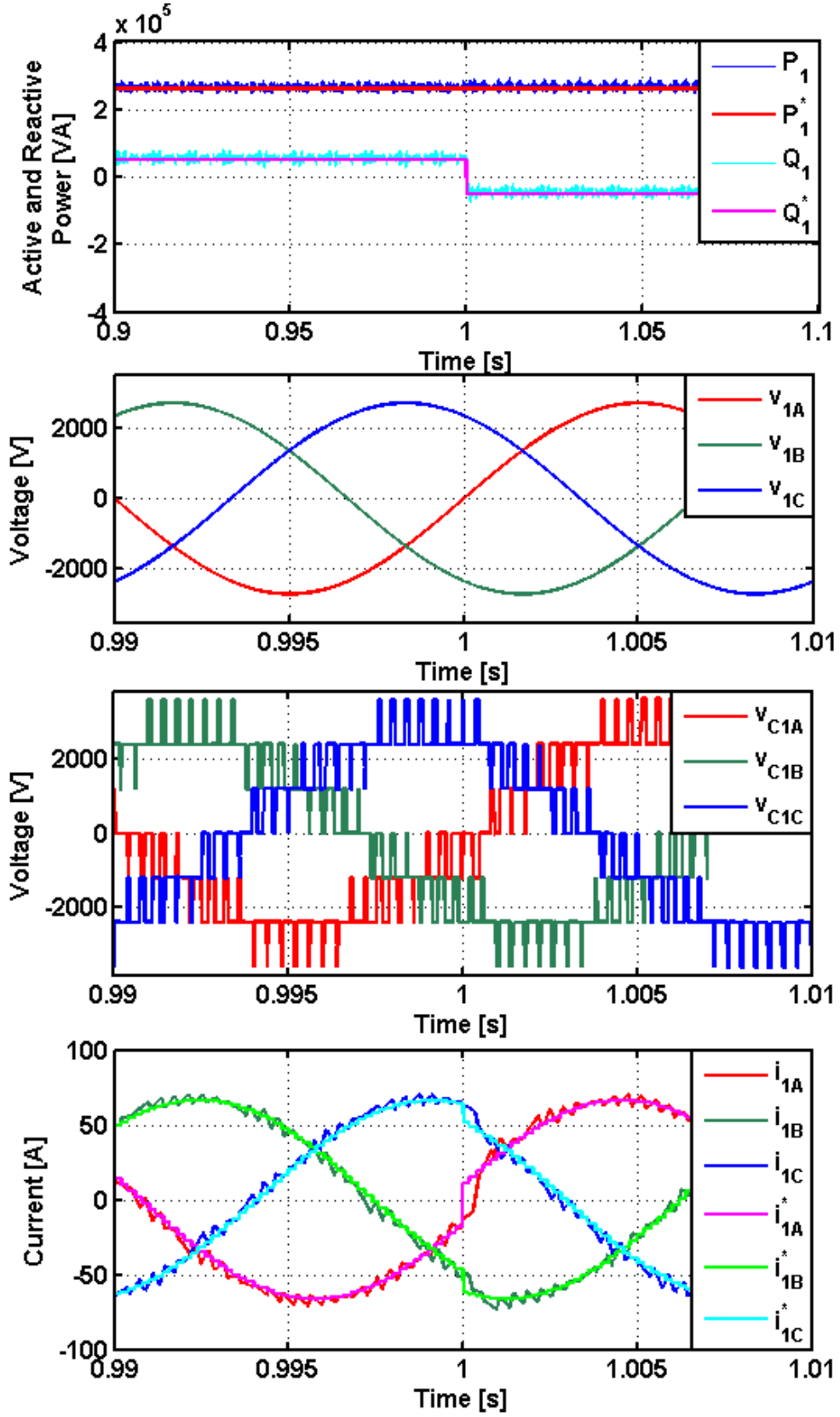


Figure 9.13 M²PC simulation for UNIFLEX-PM SST converter: grid voltage, converter voltage and AC current vs current reference on the three phases of both side of the SST converter when a reactive power reference step from 50kVAR to -50kVAR is applied on port 1 at time 1s.

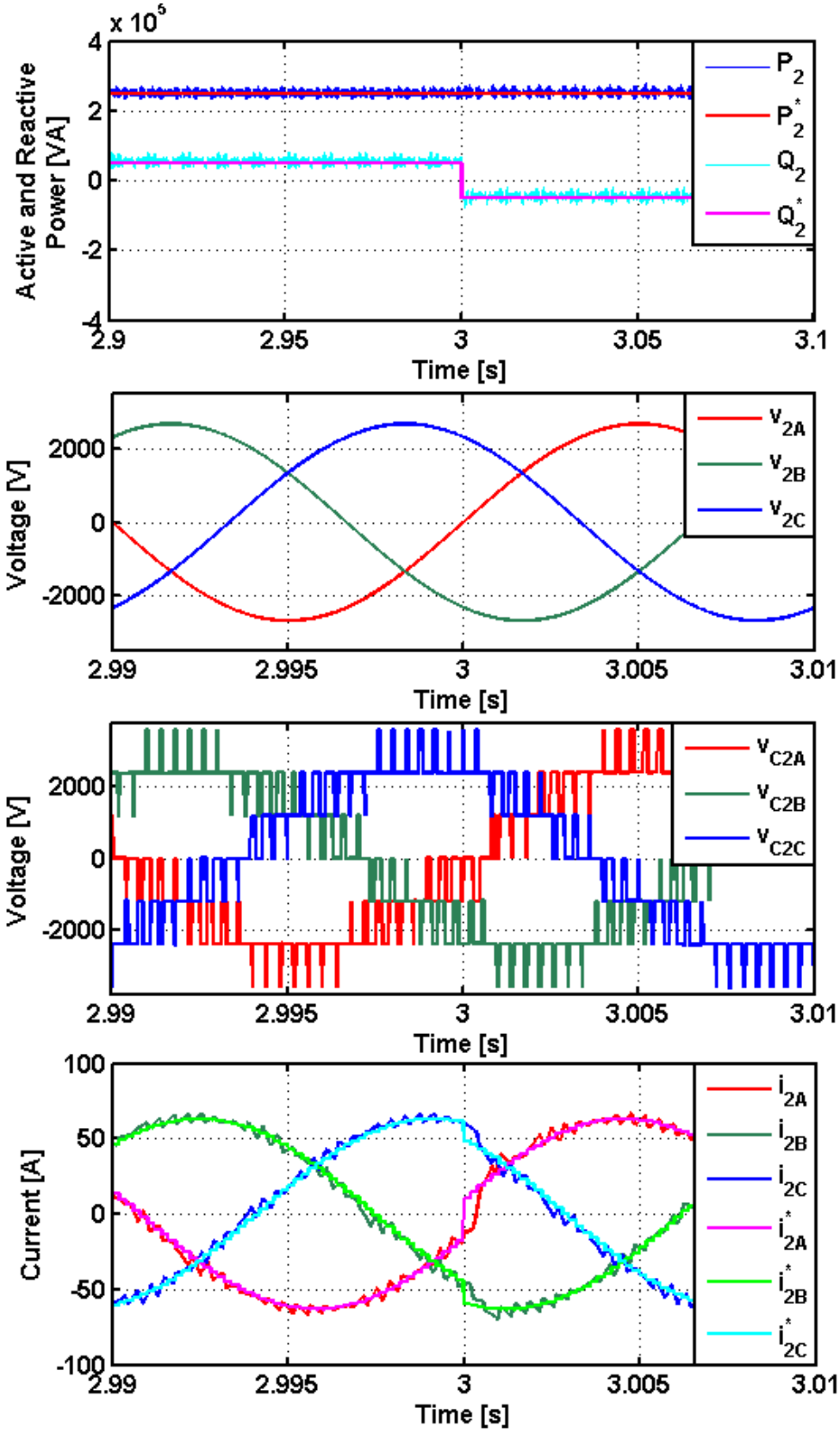


Figure 9.14 M²PC simulation for UNIFLEX-PM SST converter: grid voltage, converter voltage and AC current vs current reference on the three phases of both side of the SST converter when a reactive power reference step from 50kVAR to -50kVAR is applied on port 2 at time 3s.

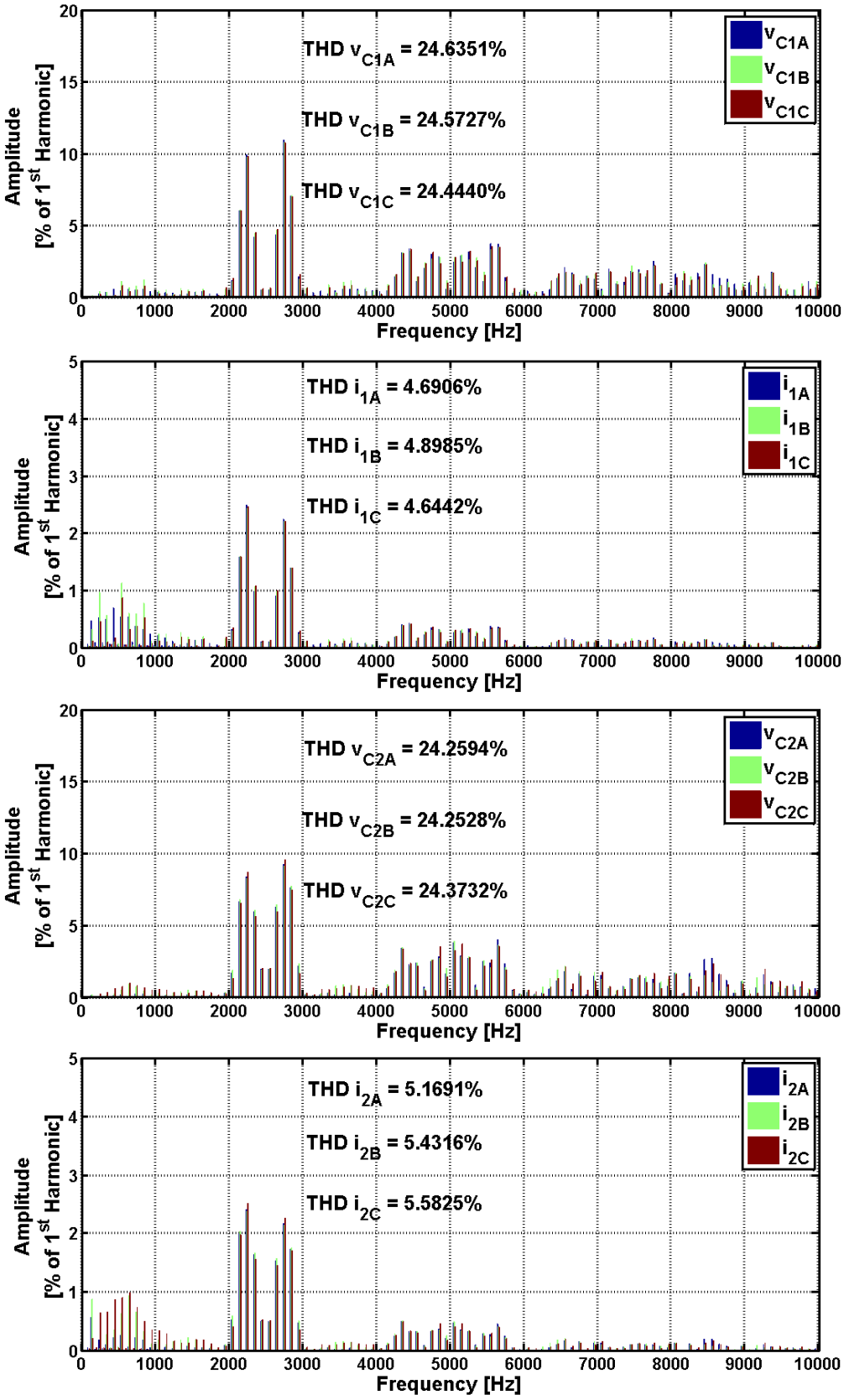


Figure 9.15 M²PC current control simulation for UNIFLEX-PM SST converter: AC current and converter voltages harmonic content on the three phases of both sides of the SST converter.

9.2.2 Modulated Model Predictive DC-Link voltage/current control

Figure 9.16 shows the active and reactive power tracking for the overall M^{2}PC DC-Link voltage/current control when active and reactive power variations are considered while, Figure 9.17 shows the DC-Link voltages behaviour. It is possible to notice that the DC-Link voltages shows a dynamic similar to the one obtained with MPC. In fact, during power references variations, the predictive DC-Link voltage controller present a faster response respect to the classic PI controller. Moreover the DC voltage tracking presents negligible steady state errors, with DC voltage variations. Also in this case an active DC-Link voltage balancing algorithm is implemented in the modulator, and the DC voltage on each capacitor of each phase is maintained balanced with negligible oscillation.

Looking at Figure 9.18, Figure 9.19, Figure 9.20 and Figure 9.21, M^{2}PC produces sinusoidal AC currents with minimal harmonic distortions, achieving results comparable to DBC. In Figure 9.18 and Figure 9.19 an active power reference step of 250kW is applied and the control react with a fast response but producing higher oscillations, compared to DBC and MPC. In Figure 9.20 and Figure 9.21 a reactive power step from 50kVAR to -50kVAR is applied and also in this case M^{2}PC control provides a fast current tracking. It can be highlighted that using M^{2}PC current control, thanks to the presence of an intrinsic PWM scheme, the current ripple is reduced compared to MPC.

In both Figure 9.19 and Figure 9.21 it is possible to see that a fast response to active and reactive power reference steps is achieved with M^{2}PC and the phase current presents a ripple comparable to the one achieved by DBC.

In fact, from Figure 9.22, it is clear that the switching frequency of M^{2}PC is constant to a value of 2.5kHz, as for DBC, producing an harmonic content on the converter voltages with a THD of about 26%. Being the harmonics produced by the converter mainly located around the switching frequency and its multiples, they are largely filtered by the line inductance resulting in a THD of 5.7% for the AC currents. Compared to DBC, the AC current THD produced from M^{2}PC presents slightly higher values; however, compared to MPC a significant improvement in terms of current and, consequently, power quality, can be noticed.

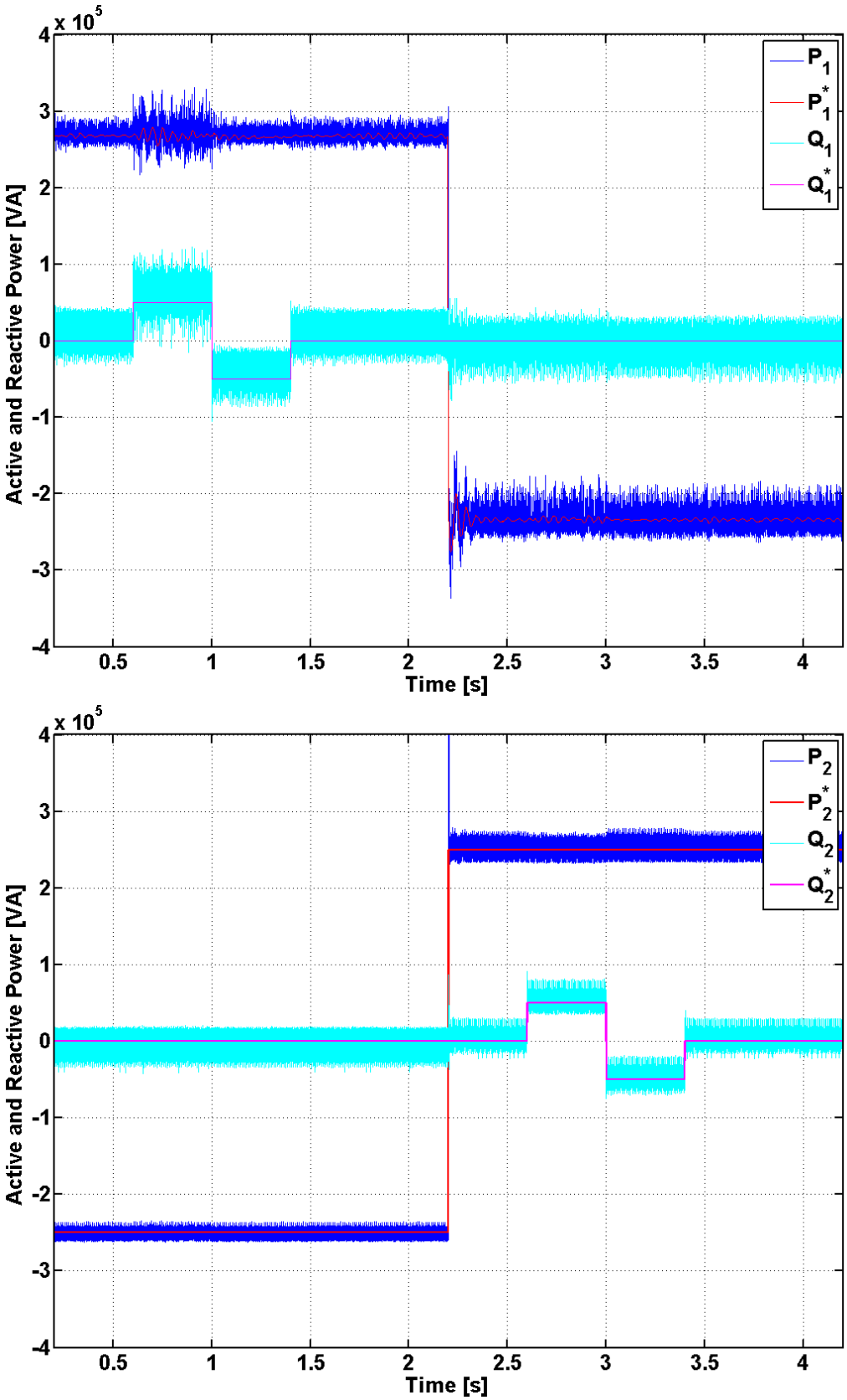


Figure 9.16 M²PC DC-Link voltage / current control simulation for UNIFLEX-PM SST converter: active and reactive power flow vs references on the two SST sides.

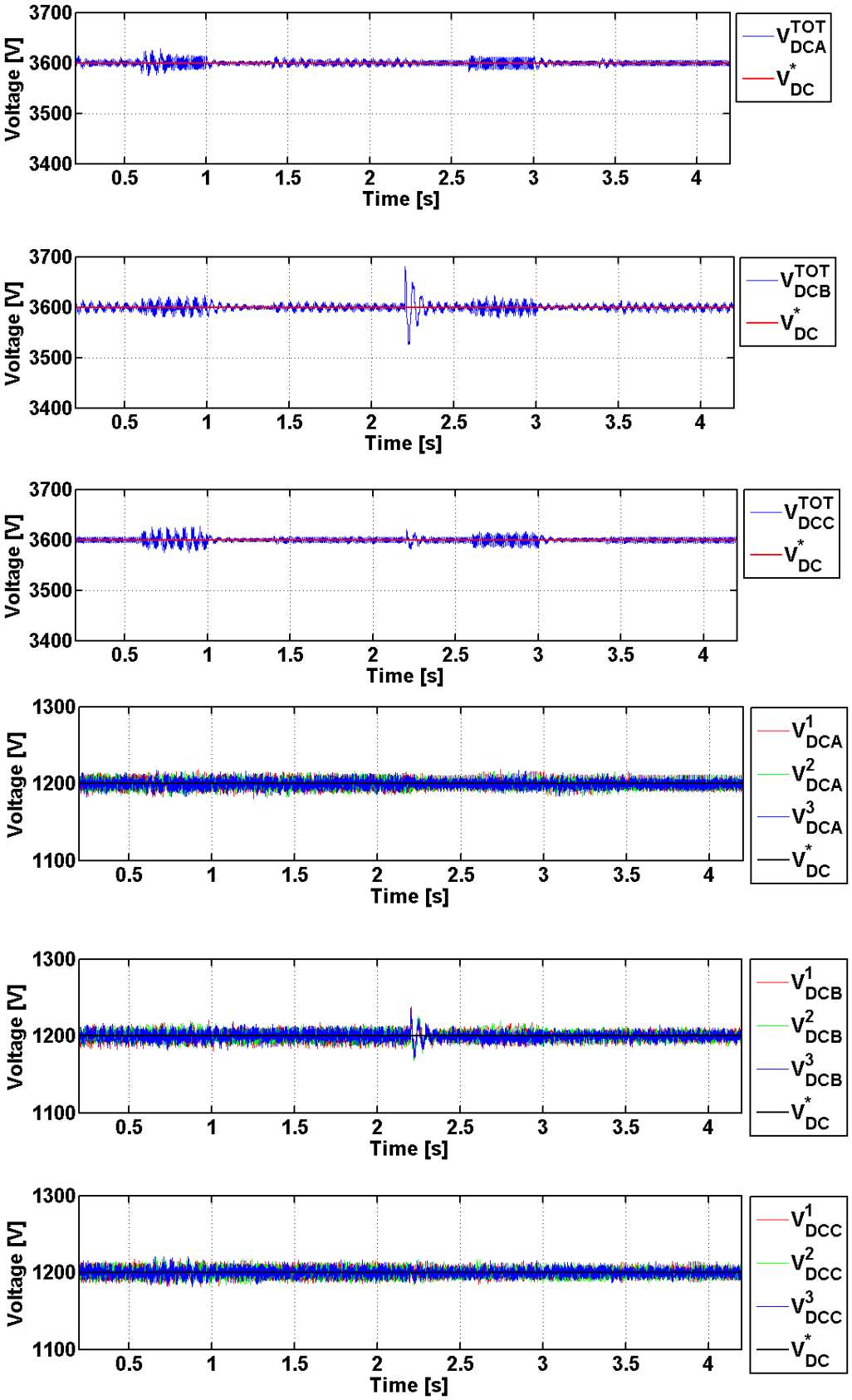


Figure 9.17 M²PC DC-Link voltage / current control simulation for UNIFLEX-PM SST converter: total DC-Link voltages on each phase vs DC-Link voltage reference and single DC-Link capacitors voltages.

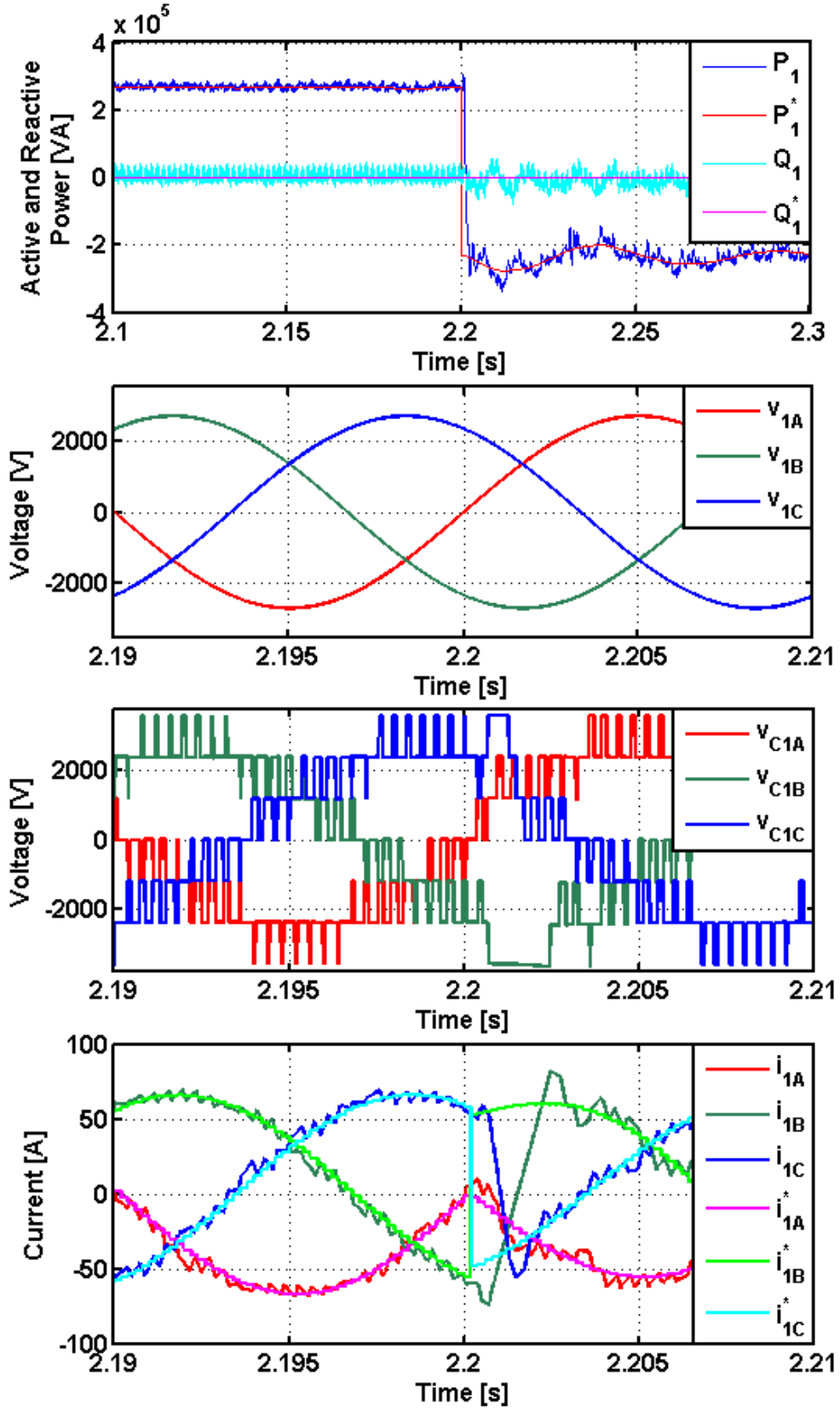


Figure 9.18 M²PC DC-Link voltage / current control simulation for UNIFLEX-PM SST converter: grid voltage, converter voltage and AC current vs current reference on the three phases of both side of the SST converter when an active power reference step from 250kW to -250kW is applied on port 1 at time2.2s.

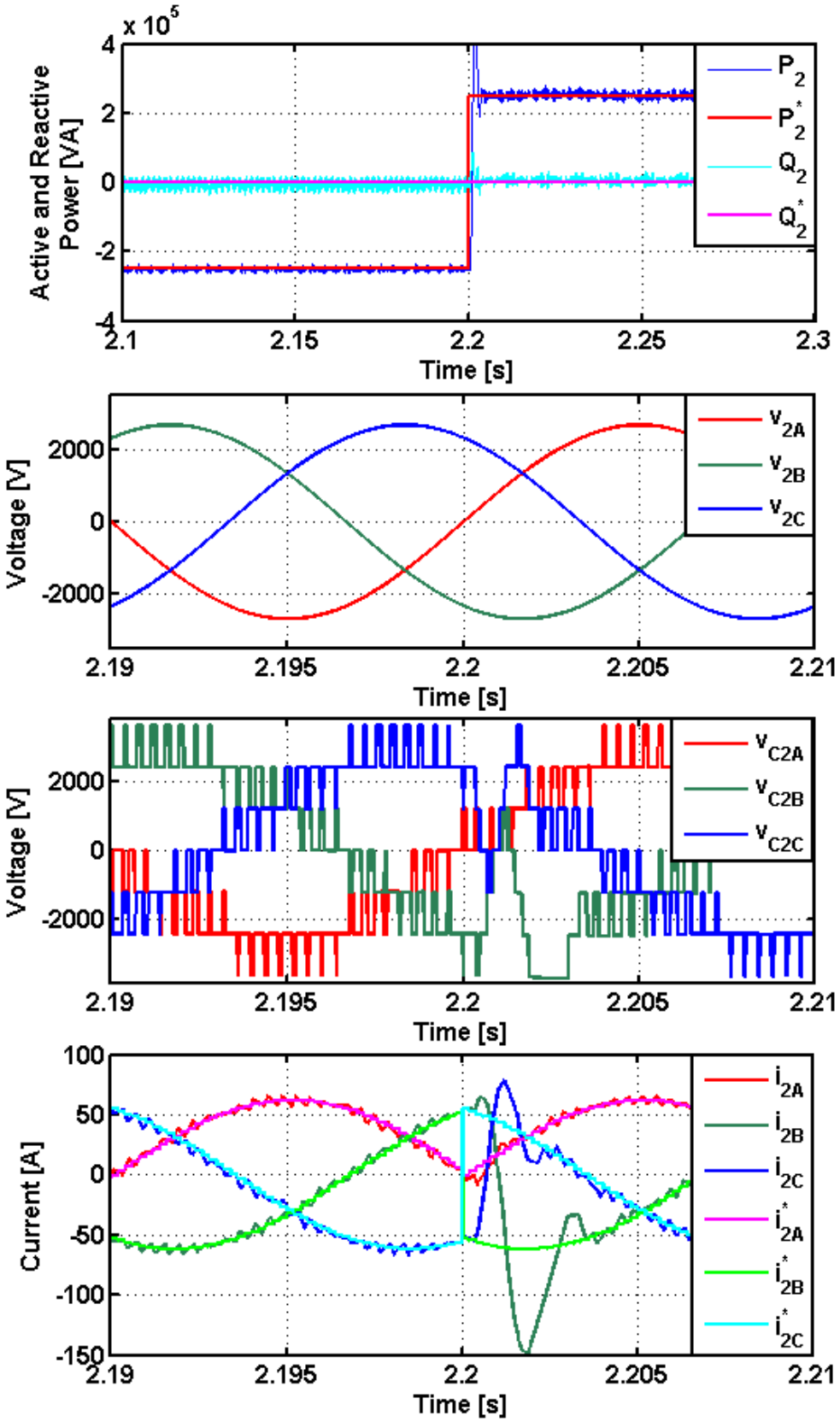


Figure 9.19 M²PC DC-Link voltage / current control simulation for UNIFLEX-PM SST converter: grid voltage, converter voltage and AC current vs current reference on the three phases of both side of the SST converter when an active power reference step from -250kW to 250kW is applied on port 2 at time2.2s.

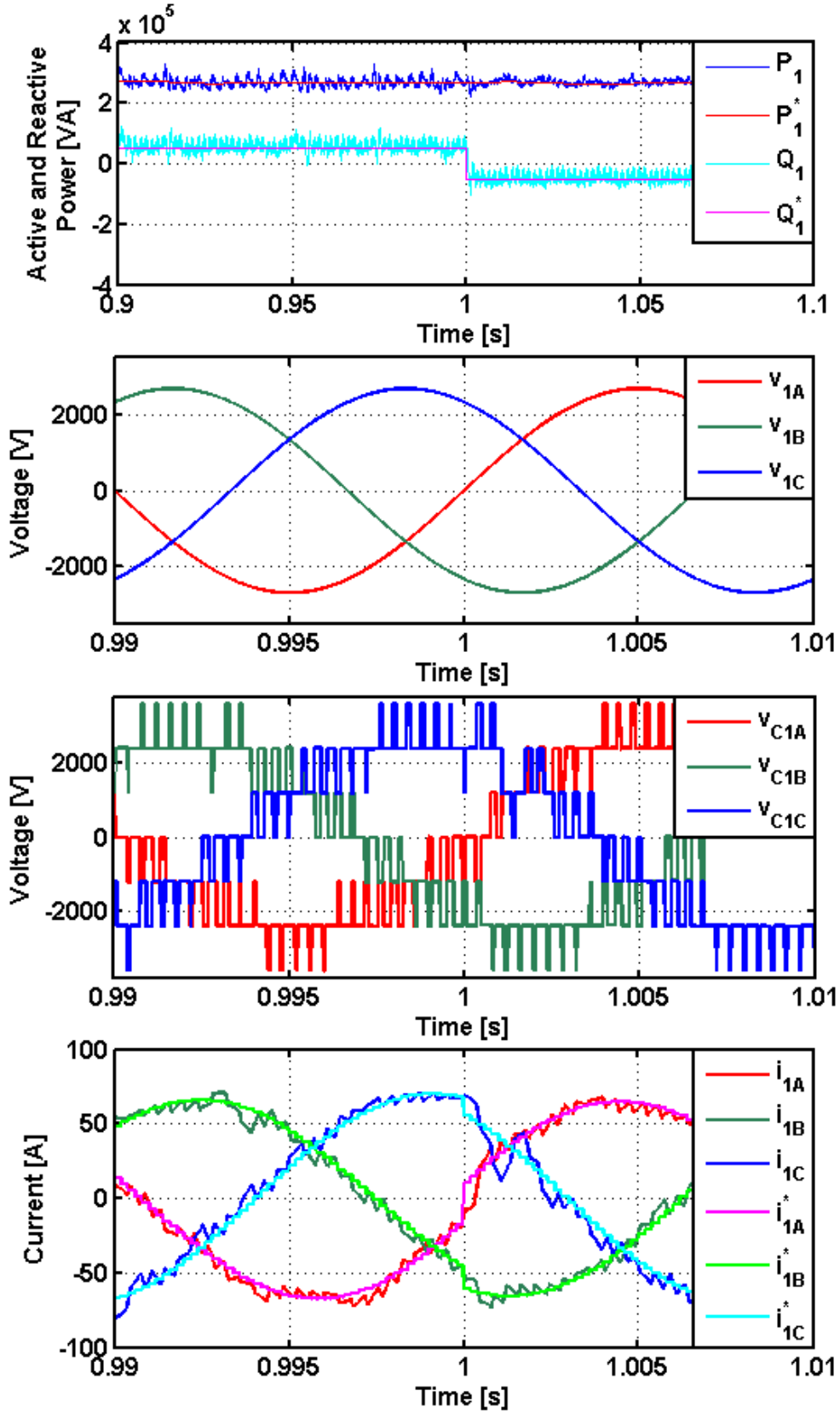


Figure 9.20 M²PC DC-Link voltage / current control simulation for UNIFLEX-PM SST converter: grid voltage, converter voltage and AC current vs current reference on the three phases of both side of the SST converter when a reactive power reference step from 50kVAR to -50kVAR is applied on port 1 at time 1s.

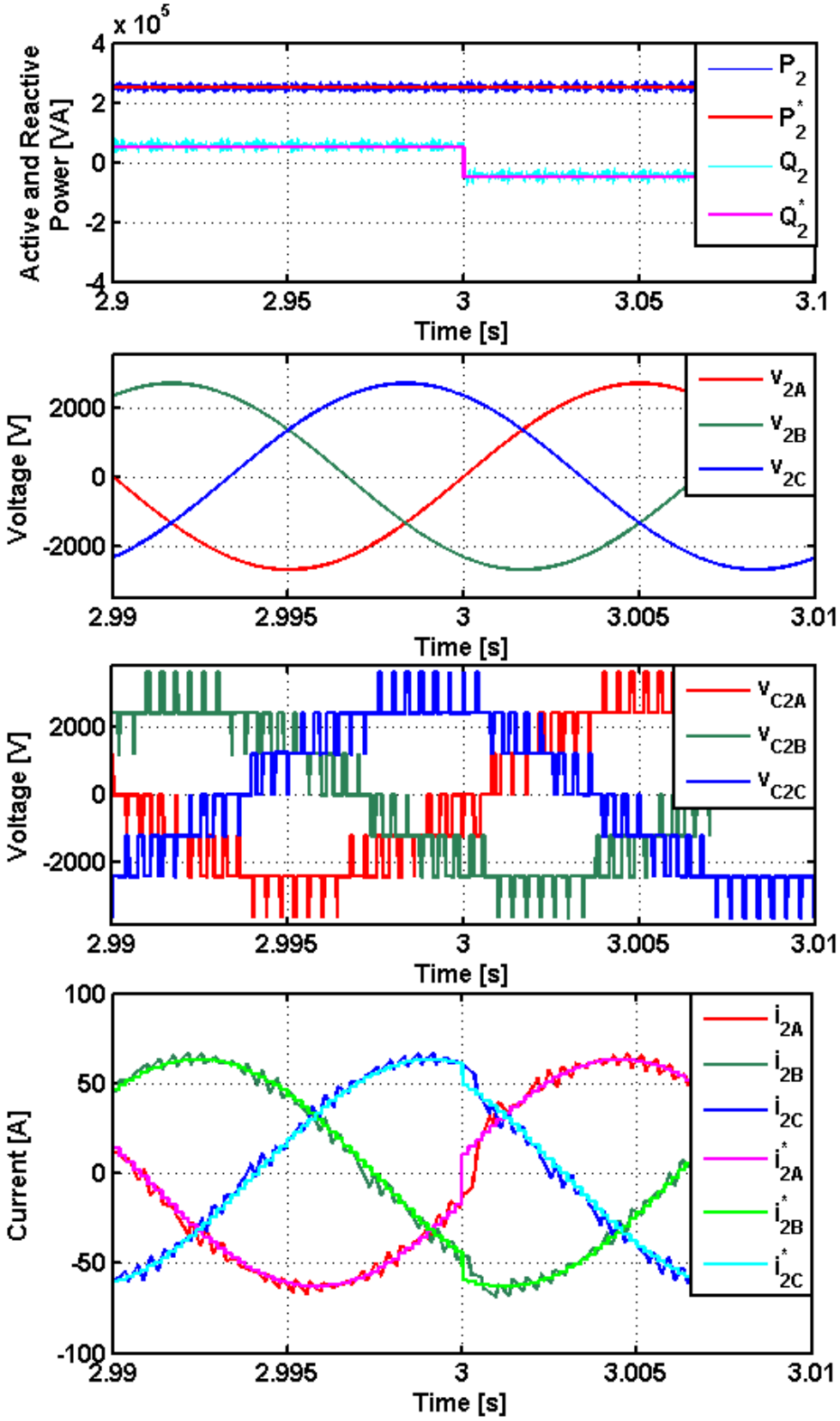


Figure 9.21 M²PC DC-Link voltage / current control simulation for UNIFLEX-PM SST converter: grid voltage, converter voltage and AC current vs current reference on the three phases of both side of the SST converter when a reactive power step from 50kVAR to -50kVAR is applied on port 2 at time 3s.

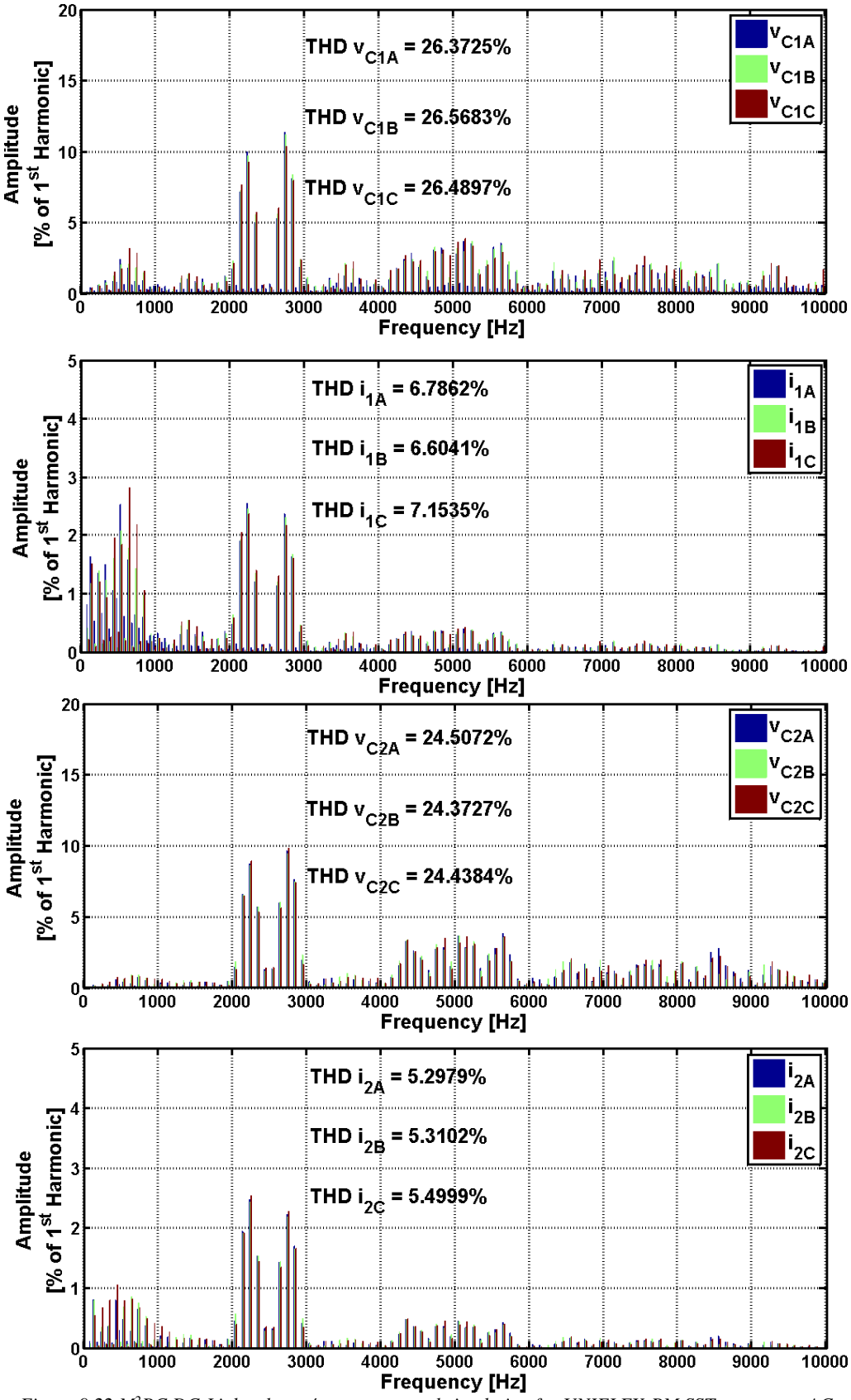


Figure 9.22 M²PC DC-Link voltage / current control simulation for UNIFLEX-PM SST converter: AC current and converter voltages harmonic content on the three phases of both sides of the SST converter.

9.3 Experimental results for the Modulated Model Predictive Control on the Universal and Flexible Power Management demonstrator

Experimental testing has been carried out on the two port UNIFLEX-PM demonstrator considering the configuration shown in Figure 3.14 and the overall control schemes of Figure 9.5 (current control) and Figure 9.8 (DC-Link voltage / current control) on port 1 while on port 2 only the current control of Figure 9.5 is implemented.

The proposed controllers have been tested under non-ideal grid conditions using the converter prototype shown in Figure 3.8. In this case port 1 is connected to the grid, and port 2 is connected to a passive load. The experimental parameters are shown in Table 9.2. Experimental results are shown only for port 1 being the control on port 2 identical with the only two following exception that the DC-Link voltage control is not required there is no grid connection on port 2.

M^{2}PC current control and M^{2}PC current DC-Link voltage / current control results are presented separately in order to appreciate similarities between M^{2}PC current control and DBC and the improvement to the overall performance using M^{2}PC DC-Link voltage / current control.

Table 9.2 M^{2}PC experimental parameters.

Name	**Description**	**Value**	**Unit**
C	DC-Link capacitor	3100	[μF]
r_L	Inductor resistance	0.5	[Ω]
L	AC filter inductance	11	[mH]
R_{LOAD}	Load resistance	30	[Ω]
V_{1peak}	Rated peak value of the AC supply on port 1 (line-to-line)	212	[V]
V_{2peak}	Rated peak value of the AC supply on port 2 (line-to-line)	212	[V]
V_{DC}	Capacitor voltage	92	[V]
$f_{sw,DC/DC}$	Switching frequency of DC/DC converter	2500	[Hz]
T_s	Sample time	0.2	[ms]
N	DC-Link voltage reference horizon	100	/
w_I	Current control weighting factor	1	/
w_V	DC voltage control weighting factor	0.1	/

9.3.1 Modulated Model Predictive current control

In Figure 9.23 the steady state performance of M^{2}PC are analysed for phase A, port1. The converter voltage shows a fixed switching frequency of 2.5kHz with a THD of approximately 22% while the current presents an harmonic content mainly located around the switching

frequency with a THD of about 3%. Similarities between M^{2}PC and DBC converter voltages and current spectrum can be appreciated, with the main part of the harmonic content located around the switching frequency. A small part of low frequency harmonic content is present using M^{2}PC. However the current harmonic distortion is highly reduced with M^{2}PC respects to MPC.

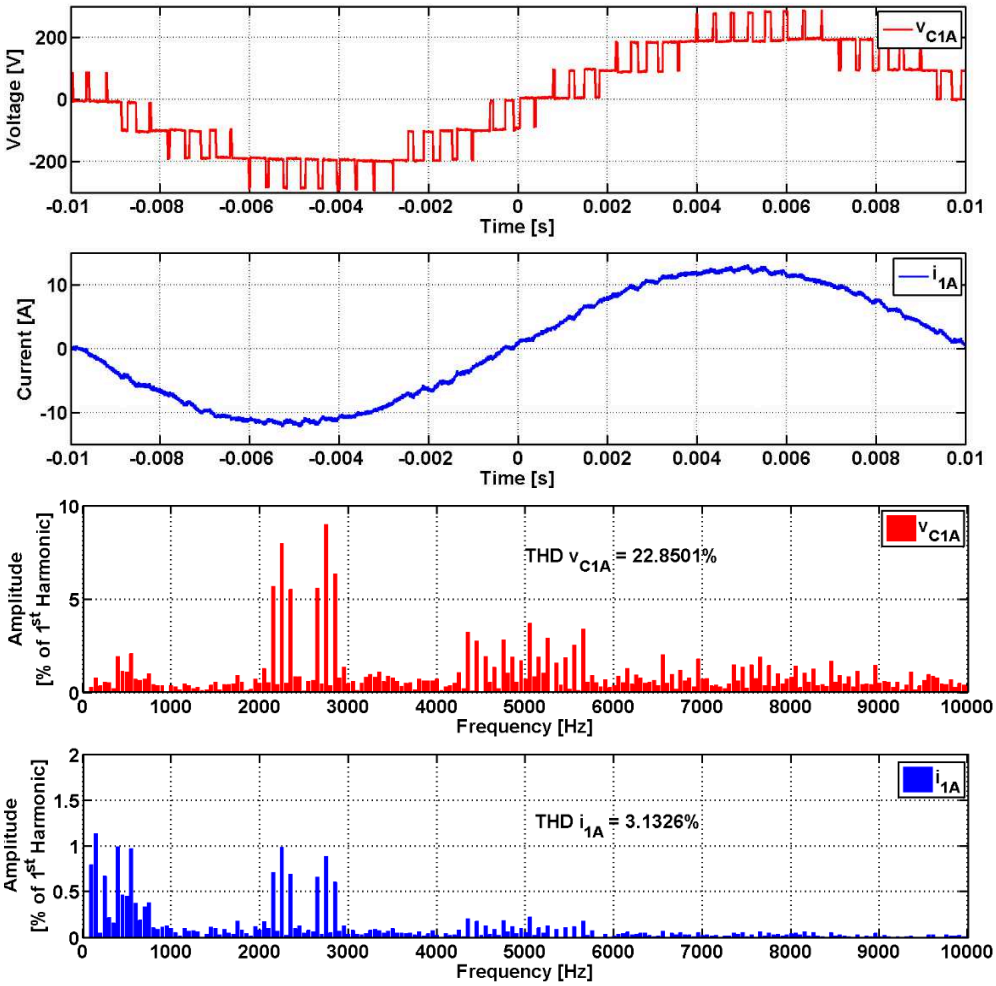


Figure 9.23 Experimental results for M^{2}PC current control on UNIFLEX-PM SST converter: steady state converter voltage and AC current on phase A, port 1.

Figure 9.24 shows an active power reference step from 0W to 3kW. As for DBC and MPC, a ramp generator is implemented to avoid that the finite delay introduced by the DC/DC converter affects the power control. As it is possible to notice the generated active power is around 3.8 kW. The extra 800W are requested by the PI DC-Link voltage control to regulate the DC-Link voltages at the desired value and compensate the DC/DC converter losses. The traditional PI DC-Link voltage control implemented in M^{2}PC current control limits the performance in terms of DC-Link voltage transient dynamic, as already described for DBC.

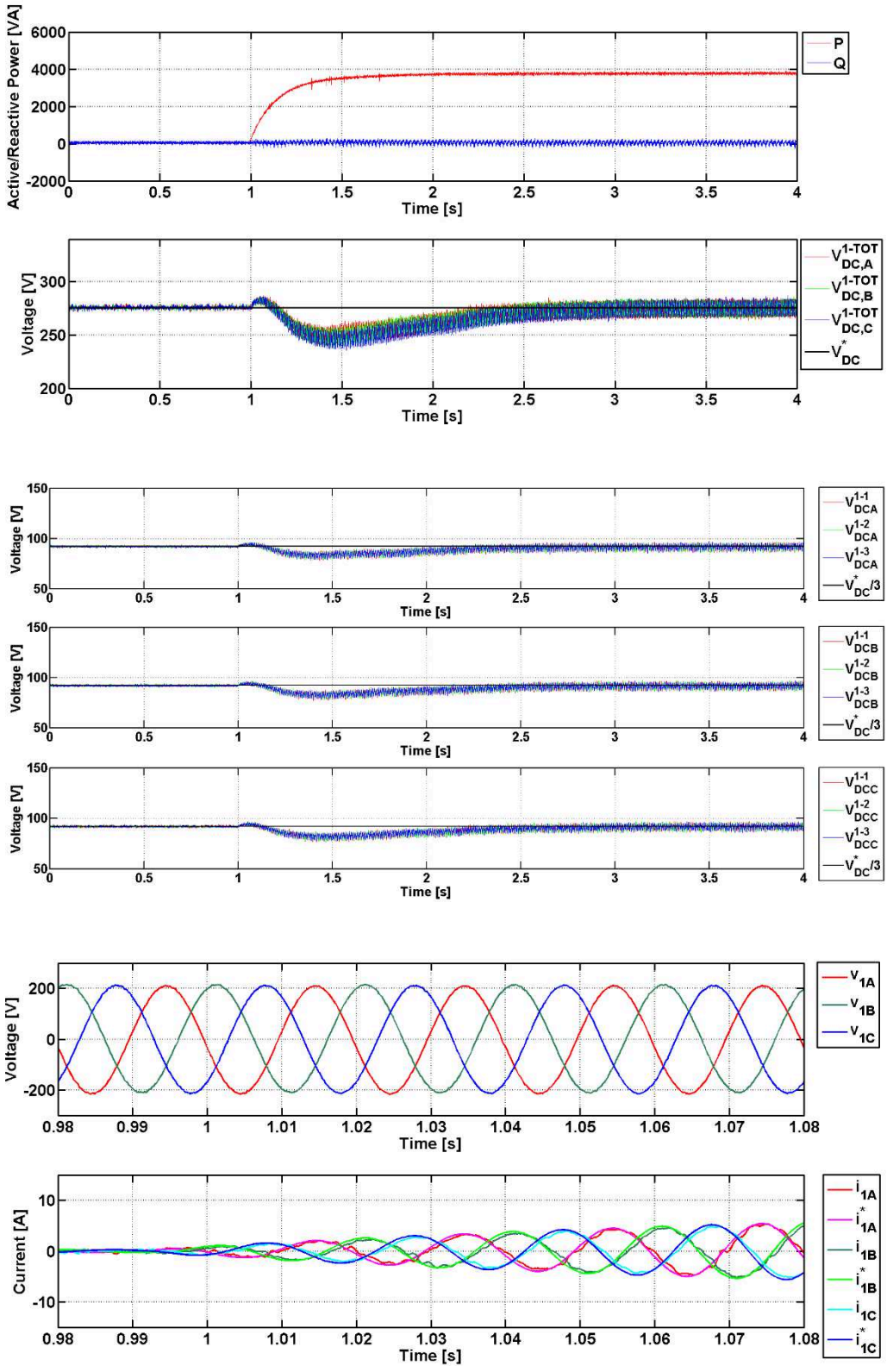


Figure 9.24 Experimental results for M²PC current control on UNIFLEX-PM SST converter: Active and Reactive power, DC-Link voltages, grid voltages and AC currents vs current references on port 1 when an active power step from 0kW to 3kW is demanded to the SST converter at time 1s.

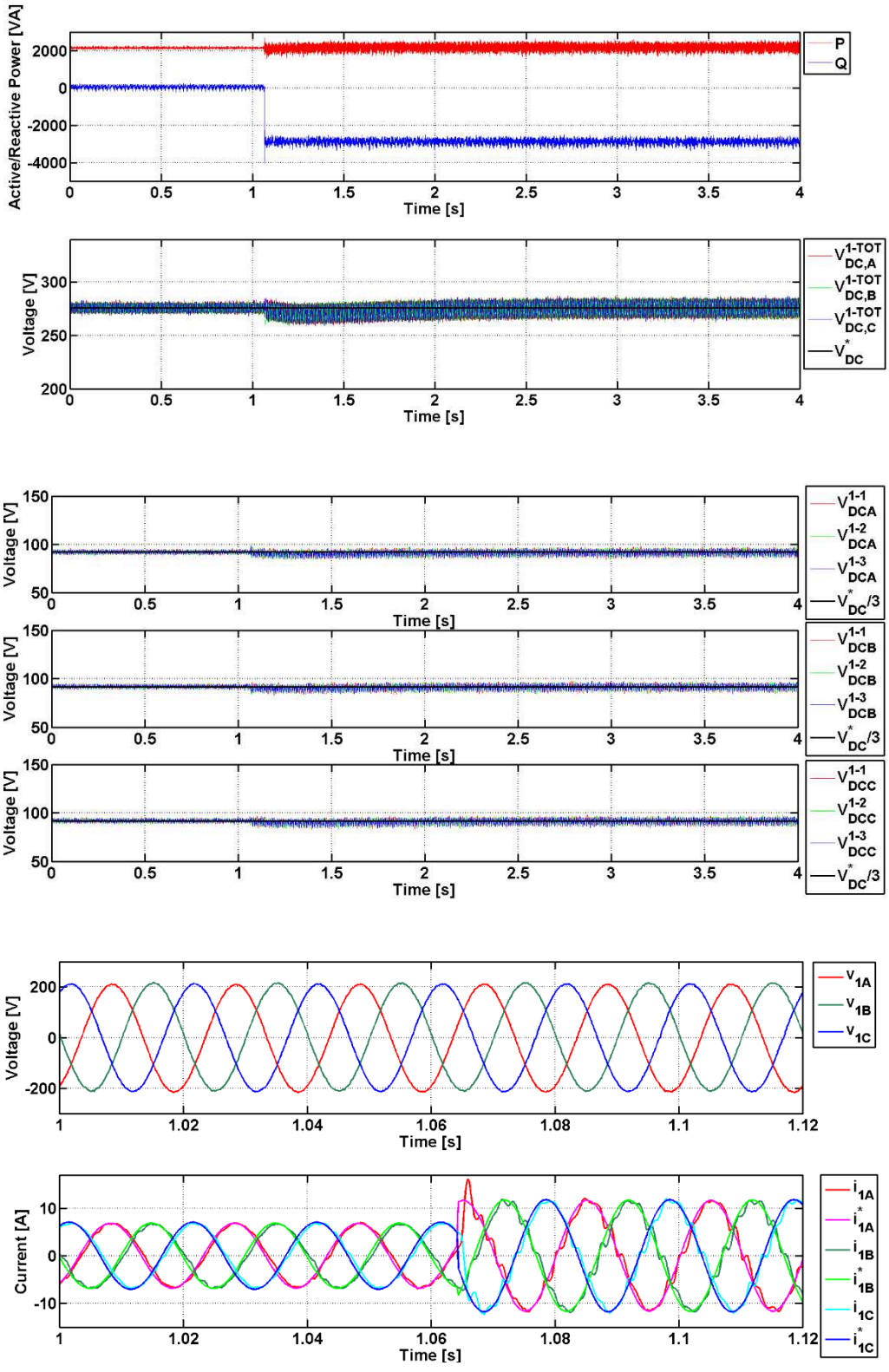


Figure 9.25 Experimental results for M²PC current control on *UNIFLEX-PM converter: active and reactive power, DC-Link voltages, grid voltages and AC currents vs current references on port 1 when a reactive power step from 0kW to -3kW is demanded to the SST converter at time 1.065s.*

A time of about 1.5s are necessary to recover the DC-Link voltage tracking with a maximum error of about 10% of the nominal value. On the other hand, since an intrinsic modulation technique is implemented in M^2PC, the AC currents and voltages are in phase, as desired, with minimal current ripple.

In Figure 9.25 a reactive power reference step from 0VAR to -3kVAR is considered, while an active power of 1.8kW is delivered to port 2. In this case M^2PC presents a current distortion when negative reactive power is provided, mainly due to the selected operative point; in fact, since the voltage vectors application times has been chosen using a suboptimal approach, their values at high modulation index values starts to differ from the optimal solution, generating distortions in the converter waveforms. However, M^2PC is still able to provide a lower current THD, compared with MPC.

More experimental tests have been conducted under non-ideal grid conditions. During the experimental testing, the power references are fixed to P*=2500W and Q*=0VAR and four non-ideal grid conditions. Frequency and amplitude variation, phase jumps and unbalances on the grid voltage have been considered in order to emulate the most common grid instabilities. The relative tests results are shown in Figure 9.26, Figure 9.27, Figure 9.28, Figure 9.29, respectively. These conditions are generated with the aid of a programmable power AC source, rated at 12kVA.

The first test has considered a supply frequency excursion from 50Hz to 53Hz (6% of nominal value), as shown in Figure 9.26. M^2PC recovers the synchronism between AC voltage and current in two supply periods; also in this case the supply frequency is detected dynamically using a zero-crossing detector on the filtered voltage at the output of the SOGI, introducing a delay of one supply period. The frequency error affects the current reference calculation and the voltage prediction producing an undesired transient of one supply period.

In the second test a phase jump of 30° is considered, as shown in Figure 9.27. M^2PC control takes two supply cycle to recover the synchronism between AC voltage and current; compared to DBC, more current oscillations are present with M^2PC during the transient. The DC-link voltage tracking is never lost during the phase jump as well as the power tracking.

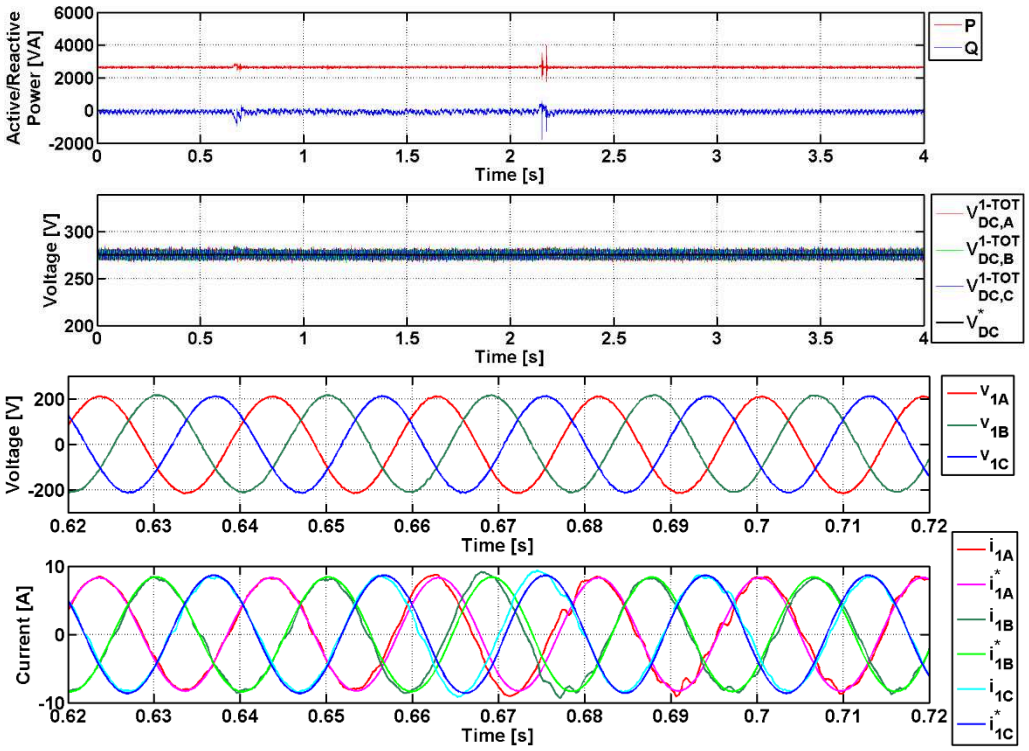


Figure 9.26 Experimental results for M²PC current control on UNIFLEX-PM SST converter: active and reactive power, total DC-Link voltages, grid voltages and AC currents on port 1 of the SST converter when a frequency step from 50Hz to 53Hz is applied at time 0.7s and a frequency step from 53Hz to 50Hz is applied at time 2.2s.

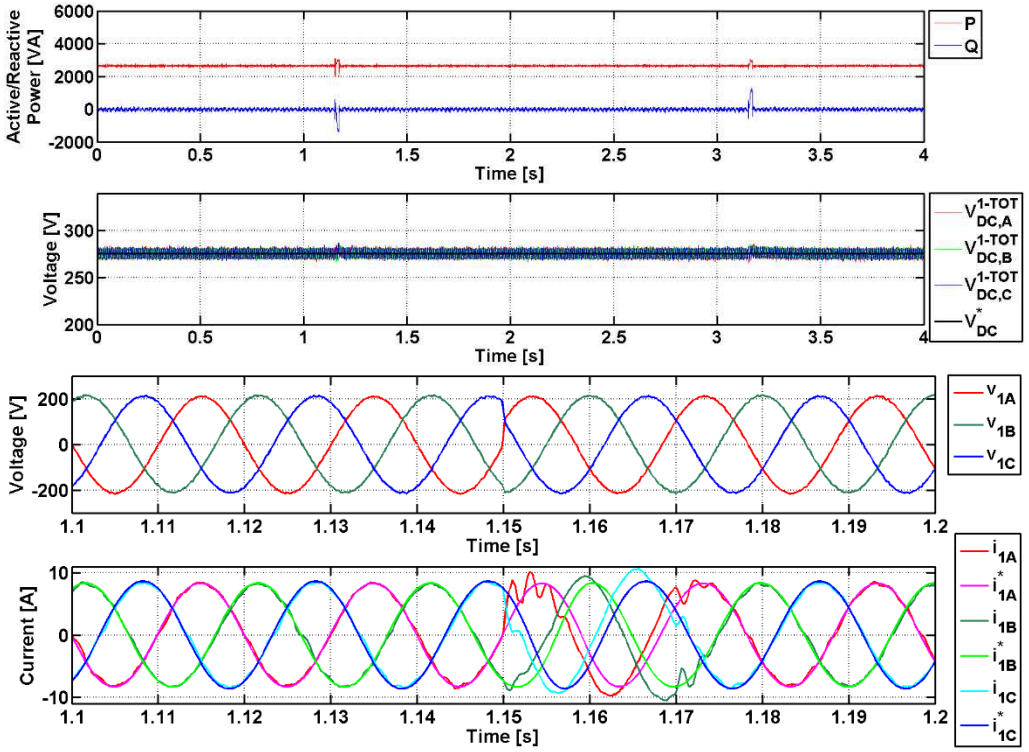


Figure 9.27 Experimental results for M²PC current control on UNIFLEX-PM SST converter: active and reactive power, total DC-Link voltages, grid voltages and AC currents on port 1 of the SST converter when a phase jump from 0° to 30° is applied at time 1.2s and a phase jump from 30° to 0° is applied at time 3.2s.

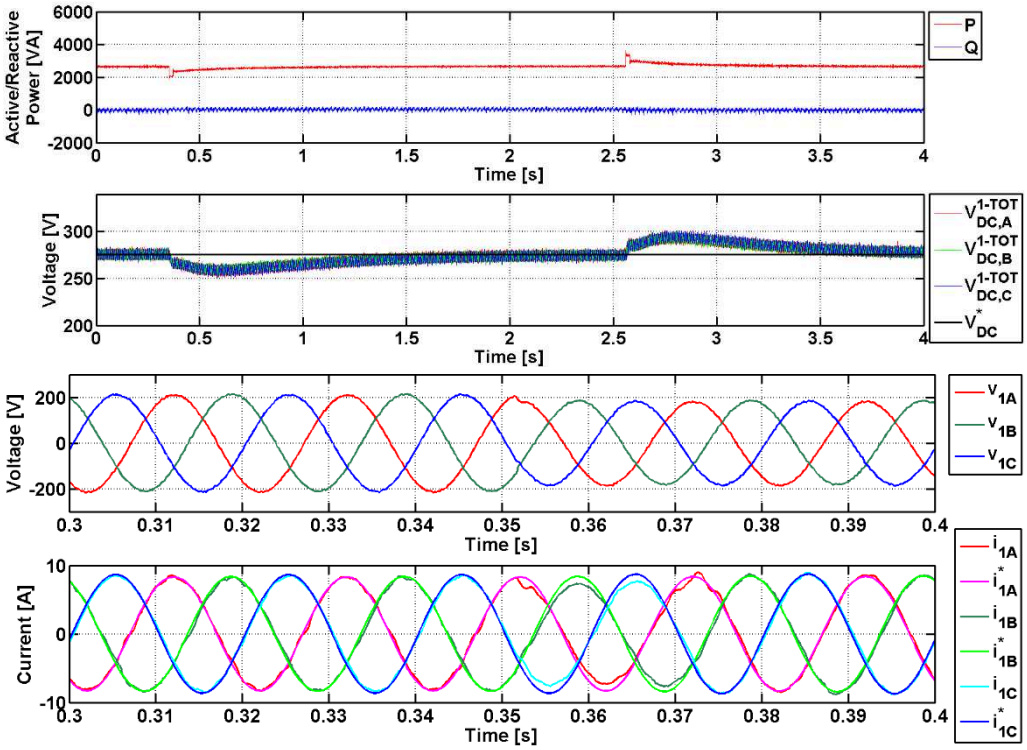


Figure 9.28 Experimental results for M²PC current control on UNIFLEX-PM SST converter: active and reactive power, total DC-Link voltages, grid voltages and AC currents on port 1 of the SST converter when an amplitude step from 150V RMS to 130V RMS is applied at time 0.4s and an amplitude step from 130V RMS to 150V RMS is applied at time 2.6s.

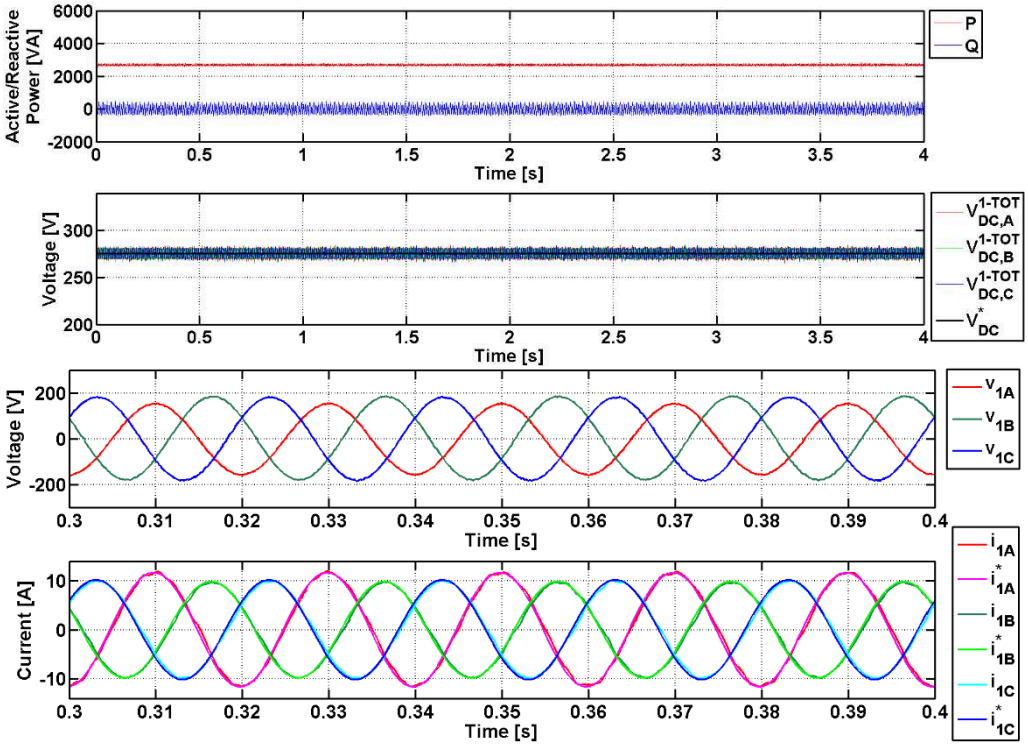


Figure 9.29 Experimental results for M²PC current control on UNIFLEX-PM SST converter: active and reactive power, total DC-Link voltages, grid voltages and AC currents on port 1 of the SST converter when a voltage unbalance of 10% is applied.

In the third test a supply voltage amplitude excursion from 150V RMS to 130V RMS (20% of the nominal value) is considered, as shown in Figure 9.28. In this case M^2PC presents a response similar to DBC, in terms of DC-Link voltage and power tracking; the dynamic response of the PI DC-Link voltage controller limits the transient response during voltage excursions.

Finally, a supply voltage unbalance, defined as positive sequence divided by negative sequence, of 10% is considered in Figure 9.29; the DC-Link voltages are maintained well regulated with minimal variations. In this case, because a four wire, three phase system is considered, the produced currents are balanced even in the presence of unbalanced currents. In fact the produced zero sequence current flows in the neutral wire and the neutral potential is not affected by voltage unbalances.

9.3.2 Modulated Model Predictive DC-Link voltage/current control

In Figure 9.30 the steady state performances of M^2PC DC-Link voltage / current control are analysed for phase A, port1 of the UNIFLEX-PM demonstrator. The converter voltage shows a variable switching frequency waveform with a THD of approximately 24.5% while the current presents a reduced low order harmonic content with respect to MPC, with a THD of approximately 4.5%. In fact, since an intrinsic modulation technique implemented directly in the cost function minimization algorithm, the switching frequency is maintained constant and the harmonic are concentrated around the switching frequency. However the switching instants are calculated using an empirical method and some calculation errors, especially in real systems affected by measurement noise, can occur. These errors generate low frequency harmonics that increase the THD with respect to DBC, but maintaining lower values than MPC.

In Figure 9.31 an active power reference step from 0W to 3kW is considered. As for DBC and MPC, the finite delay introduced by the DC/DC converter has to be considered and, in order not to affect the DC-Link voltage control response, the active power reference has to have its dynamics reduced using a ramp generator. As it is possible to notice the generated active power is around 3.8 kW with the additional 800W requested by the DC-Link voltage control in order to control appropriately the DC-Link voltages at the desired value and compensate the DC/DC

converter losses. Moreover the improved performance of the MPC DC-Link voltage controller with respect to the traditional PI control implemented in DBC and M^{2}PC current control can be highlighted. In fact, looking at the DC-Link voltages, around 0.7s are necessary to recover the DC-Link voltage tracking with a maximum error of about 10% of the nominal value.

With respect to MPC this actually takes a longer time; in fact a lower value for the weight on the DC-Link voltage cost function is used with the aim to reduce the current distortion. M^{2}PC current / DC-Link voltage control produce low ripple current waveforms, in phase with the supply voltages on each phase as desired; in fact the intrinsic modulation technique implemented directly in the cost function minimization allows to provide better current quality with respect to MPC.

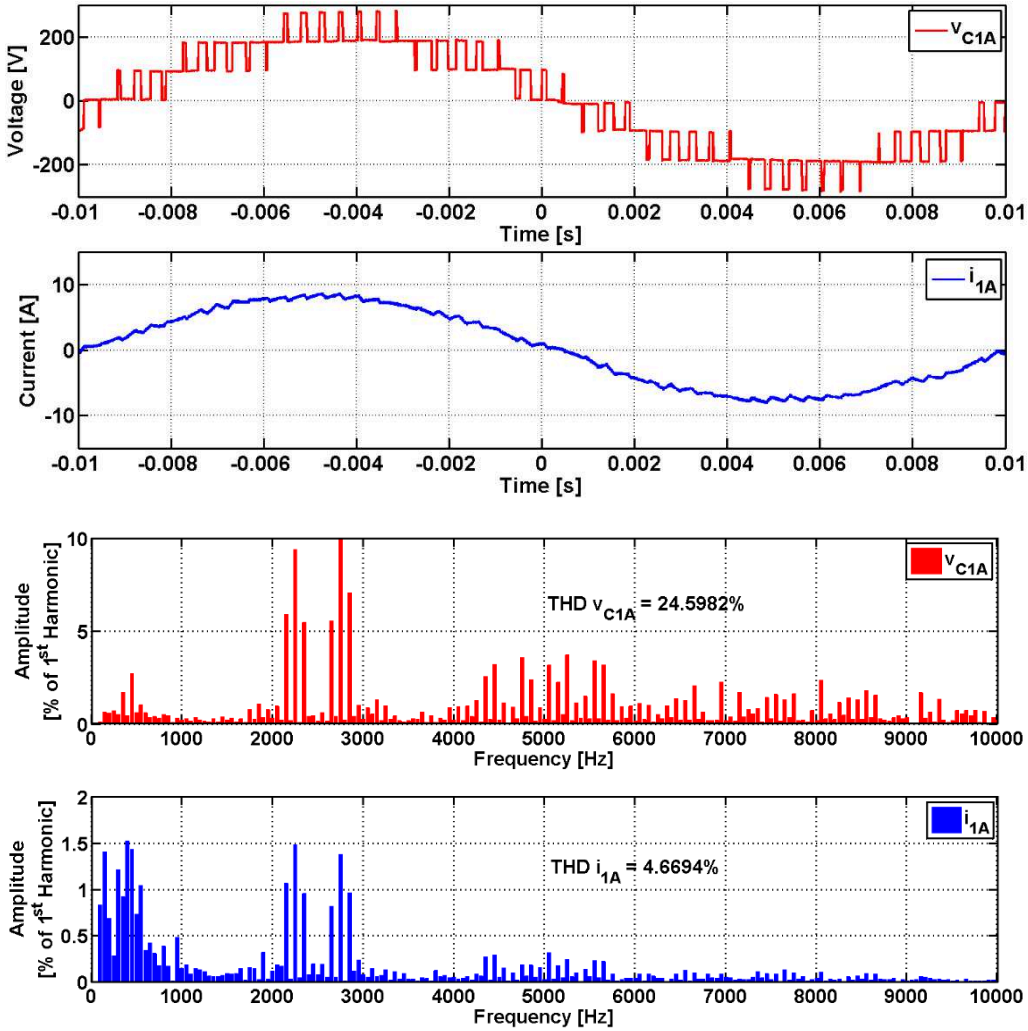


Figure 9.30 Experimental results for M^{2}PC DC-Link voltage / current control on UNIFLEX-PM SST converter: steady state converter voltage and AC current on phase A, port 1.

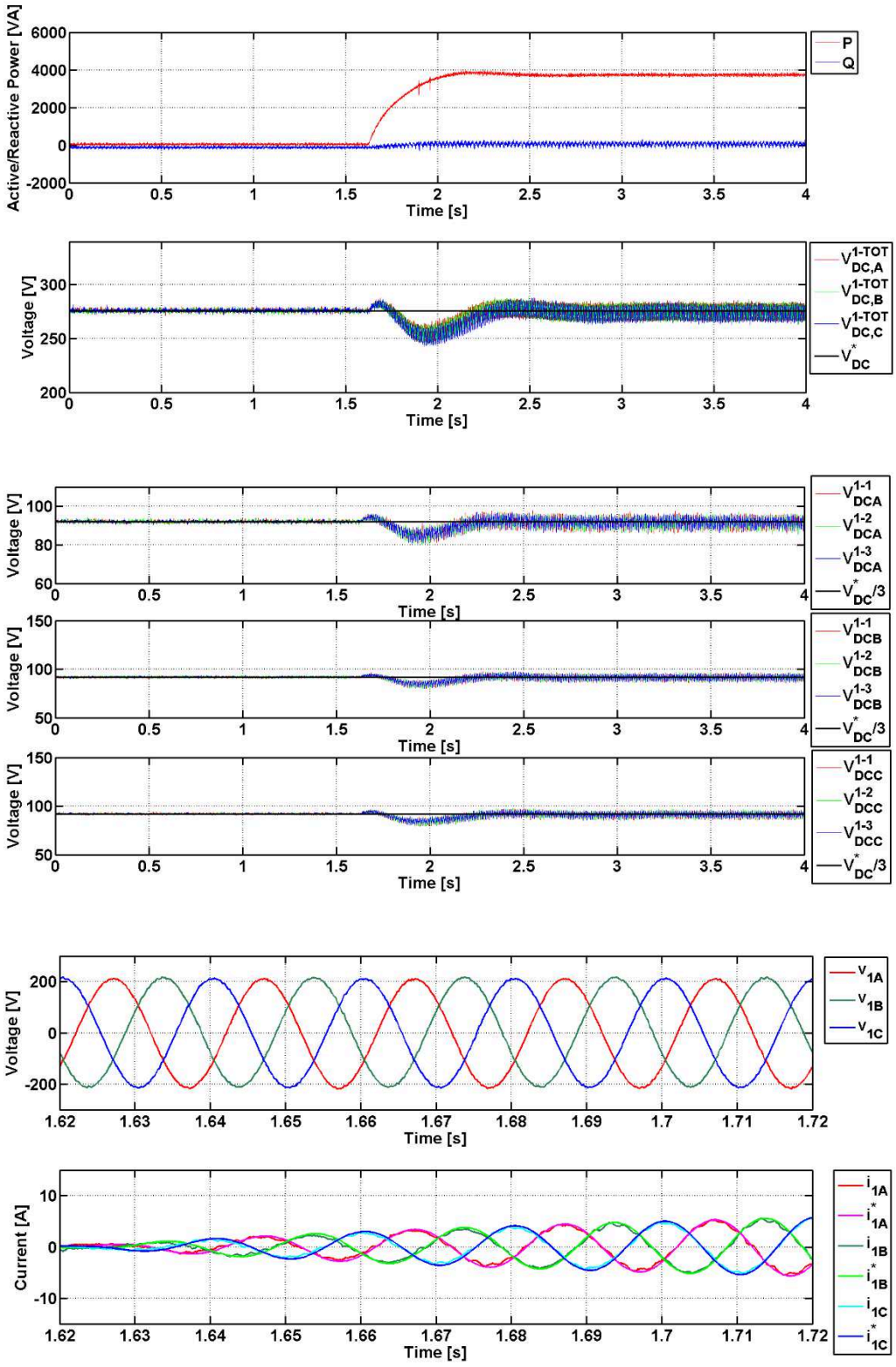


Figure 9.31 Experimental results for M²PC DC-Link voltage / current control on UNIFLEX-PM SST converter: Active and Reactive power, DC-Link voltages, grid voltages and AC currents vs current references on port 1 when an active power step from 0kW to 3kW is demanded to the SST converter at time 1.65s.

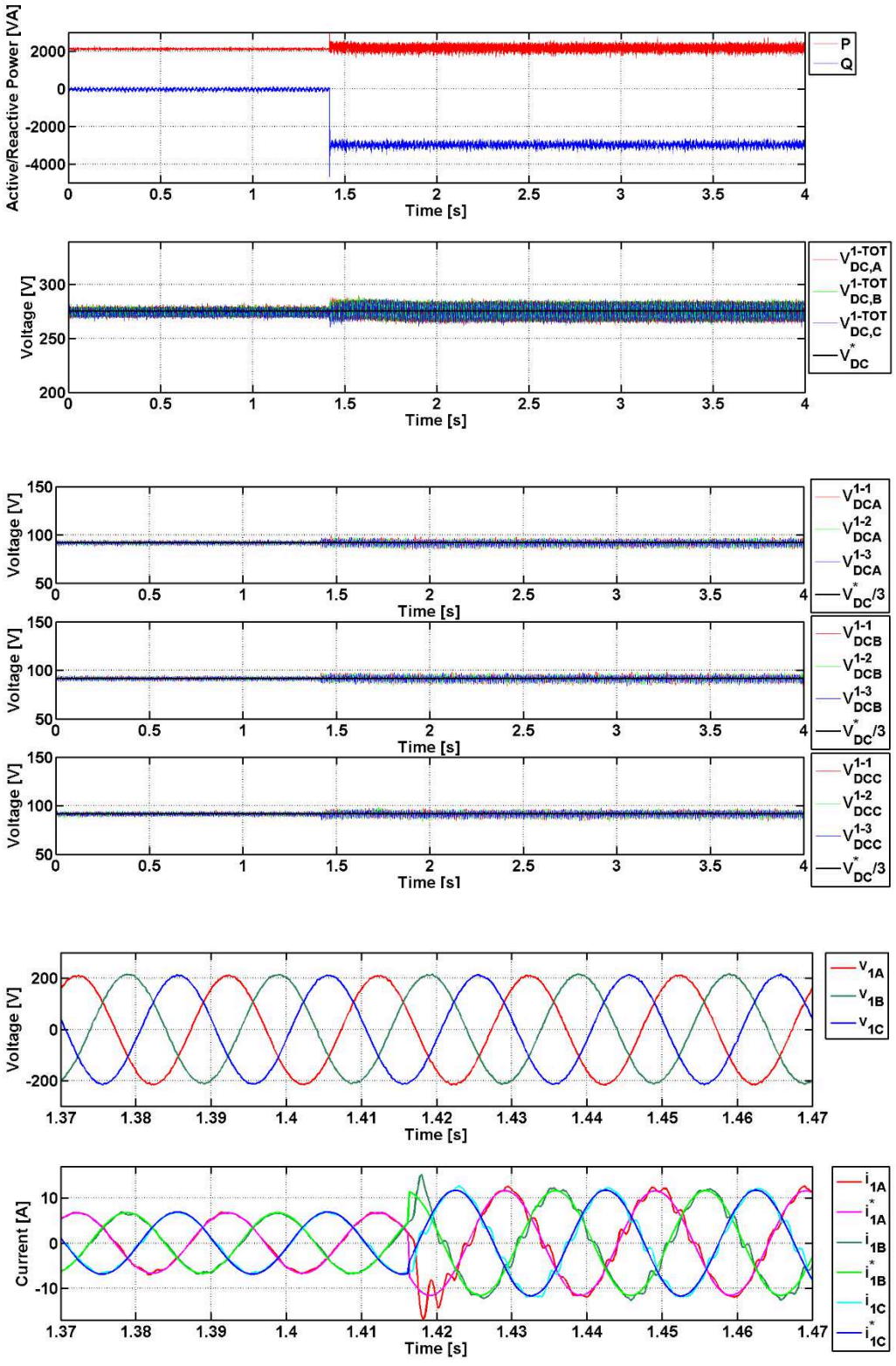


Figure 9.32 Experimental results for M²PC DC-Link voltage / current control on UNIFLEX-PM converter: active and reactive power, DC-Link voltages, grid voltages and AC currents vs current references on port 1 when a reactive power step from 0kW to -3kW is demanded to the SST converter at time 1.45s.

Figure 9.32 considers a reactive power reference step from 0VAR to -3000VAR, while an active power of 1.8kW is delivered to port 2. In this case, because the reactive power is managed independently on the two sides of the converter, the dynamics of the DC-Link voltage control is not affected from reactive power variations and there is no need to slow the reactive power reference down. The obtained power tracking matches the simulations results and the DC-Link voltages remains regulated and balanced at the desired value with negligible error. Looking at AC voltages ad currents, the current tracking is lost only for few milliseconds before the control recovers the optimal tracking. As for M^2PC current control, distortion appears on the current waveform because of the selected operative point. In fact has been observed that, for a limited range of modulation indexes, M^2PC presents performance similar to DBC. Outside this range the current presents a hybrid spectrum between MPC and DBC.

More experimental tests have been conducted under non-ideal grid conditions. During the experimental testing the power references are fixed to P*=2500W and Q*=0VAR and four non-ideal grid conditions are considered in Figure 9.33, Figure 9.34, Figure 9.35 Figure 9.36, respectively. These conditions are generated with the aid of a programmable power AC source, rated at 12 kVA.

The first test has considered a supply frequency excursion from 50Hz to 53Hz (6% of nominal value), as shown in Figure 9.33. In this case the supply frequency is detected dynamically using a zero-crossing detector on the filtered voltage at the output of the SOGI, introducing a delay of one supply period. The frequency error affects the current reference calculation and the voltage prediction producing an undesired transient of one supply period. In this scenario M^2PC recovers the synchronism between AC voltage and current in two supply periods.

In the second test a phase jump of 30° is considered, as shown in Figure 9.34. M^2PC control takes one and half supply cycles to recover the synchronism between AC voltage and current. The DC-link voltage tracking is never lost between the phase jump as well as the power tracking. With respect to DBC more current oscillations are produced during transients.

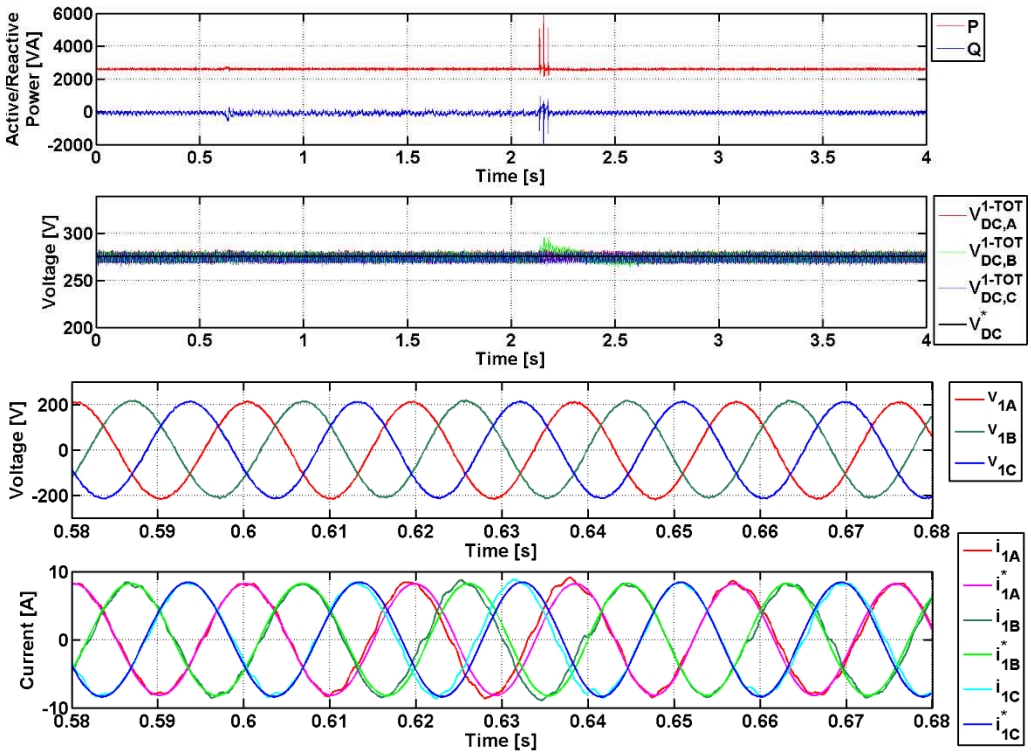


Figure 9.33 Experimental results for M²PC DC-Link voltage / current control on UNIFLEX-PM SST converter: active and reactive power, total DC-Link voltages, grid voltages and AC currents on port 1 of the SST converter when a frequency step from 50Hz to 53Hz is applied at time 0.6s and a frequency step from 53Hz to 50Hz is applied at time 2.2s.

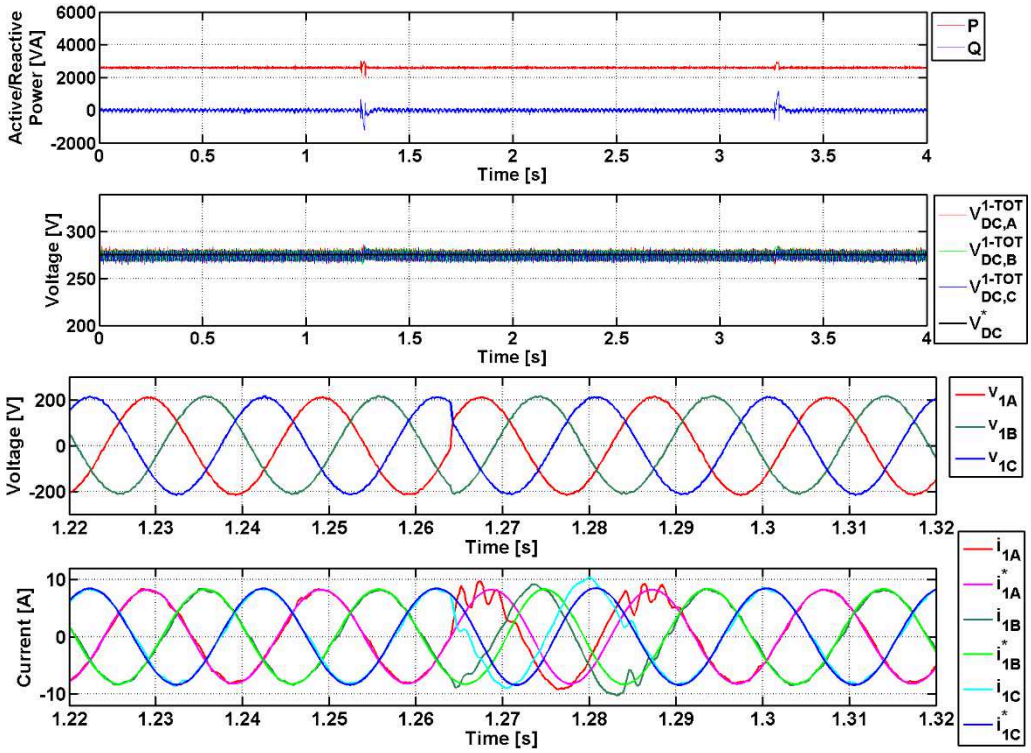


Figure 9.34 Experimental results for M²PC DC-Link voltage / current control on UNIFLEX-PM SST converter: active and reactive power, total DC-Link voltages, grid voltages and AC currents on port 1 of the SST converter when a phase jump from 0° to 30° is applied at time 1.3s and a phase jump from 30° to 0° is applied at time 3.25s.

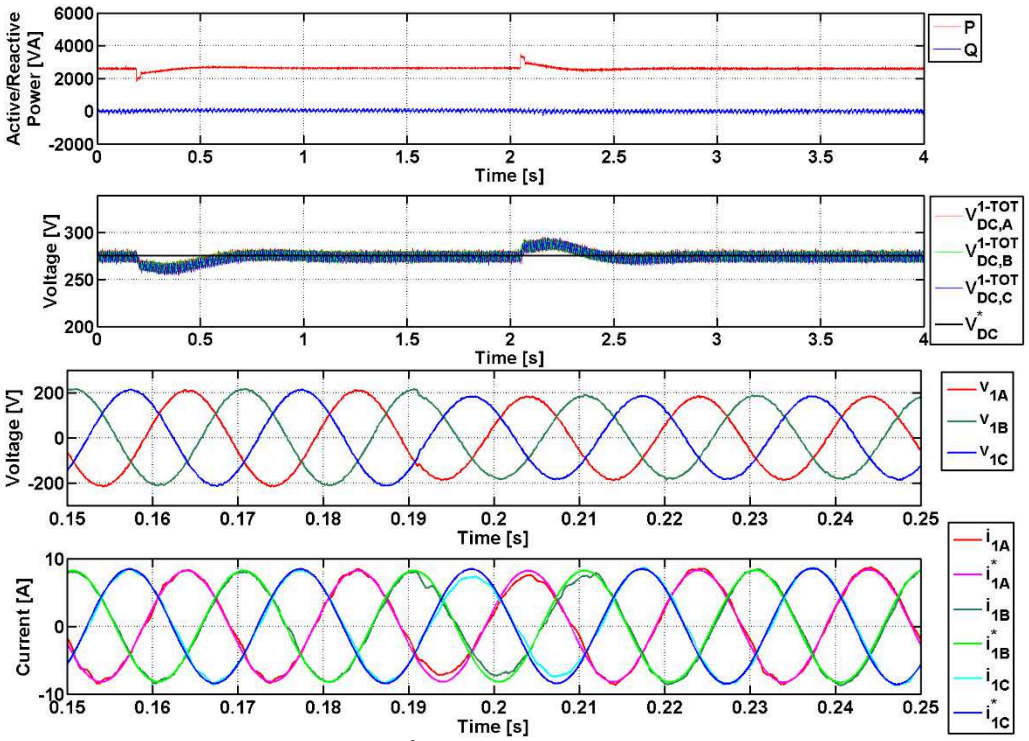


Figure 9.35 Experimental results for M²PC DC-Link voltage / current control on UNIFLEX-PM SST converter: active and reactive power, total DC-Link voltages, grid voltages and AC currents on port 1 of the SST converter when an amplitude step from 150V RMS to 130V RMS is applied at time 0.25s and an amplitude step from 130V RMS to 150V RMS is applied at time 2.1s.

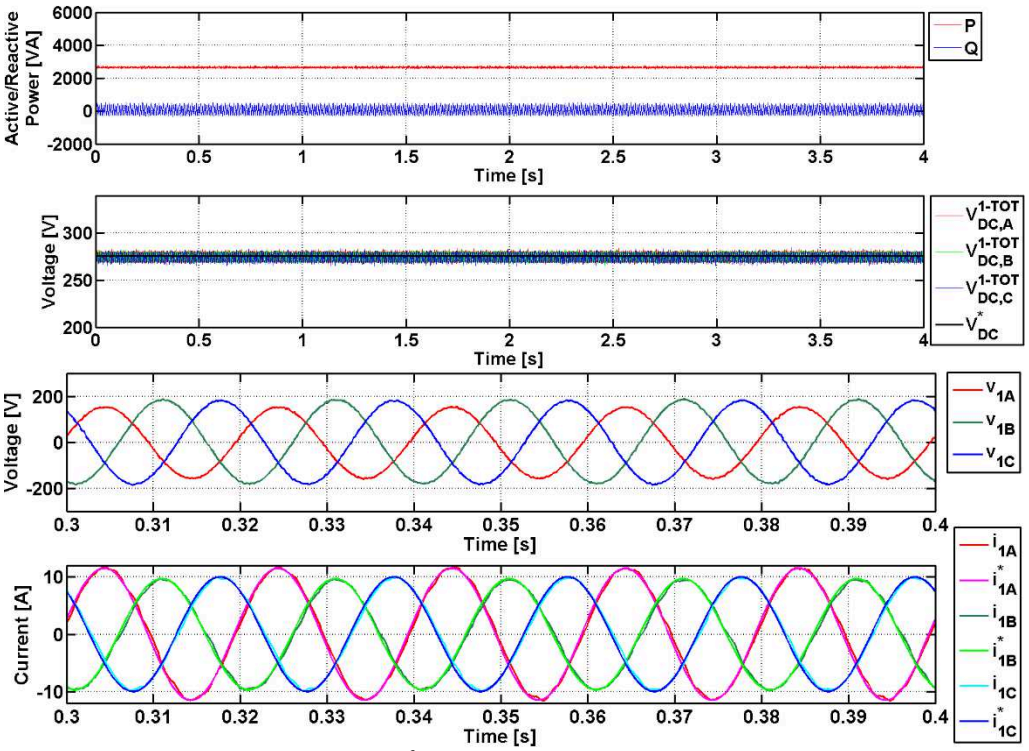


Figure 9.36 Experimental results for M²PC DC-Link voltage / current control on UNIFLEX-PM SST converter: active and reactive power, total DC-Link voltages, grid voltages and AC currents on port 1 of the SST converter when a voltage unbalance of 10% is applied

In the third test a supply voltage amplitude excursion from 150V RMS to 130V RMS (20% of nominal value) is considered, as shown in Figure 9.35. In this case M^2PC presents a fast response, in terms of DC-Link voltage and power tracking; the fast dynamic response of the M^2PC DC-Link voltage controller allows to obtain improved dynamic performances with respect to DBC. However, being the current cost function weight reduced with respect to MPC, a transient of 0.25s is necessary to recover the DC-Link voltage tracking with a maximum DC-Link voltage excursion of 6% of the nominal value.

Finally, a supply voltage unbalance, defined as positive sequence divided by negative sequence, of 10% is considered in Figure 9.36; the DC-Link voltages are maintained well regulated with minimal variations, being the control implemented on a four wire, three phase system.

9.4 Simulation and experimental results comparison

In this section experimental and simulation results obtained for the 7-Level CHB SST converter are compared for both M^{2}PC current and DC-Link voltage/current control.

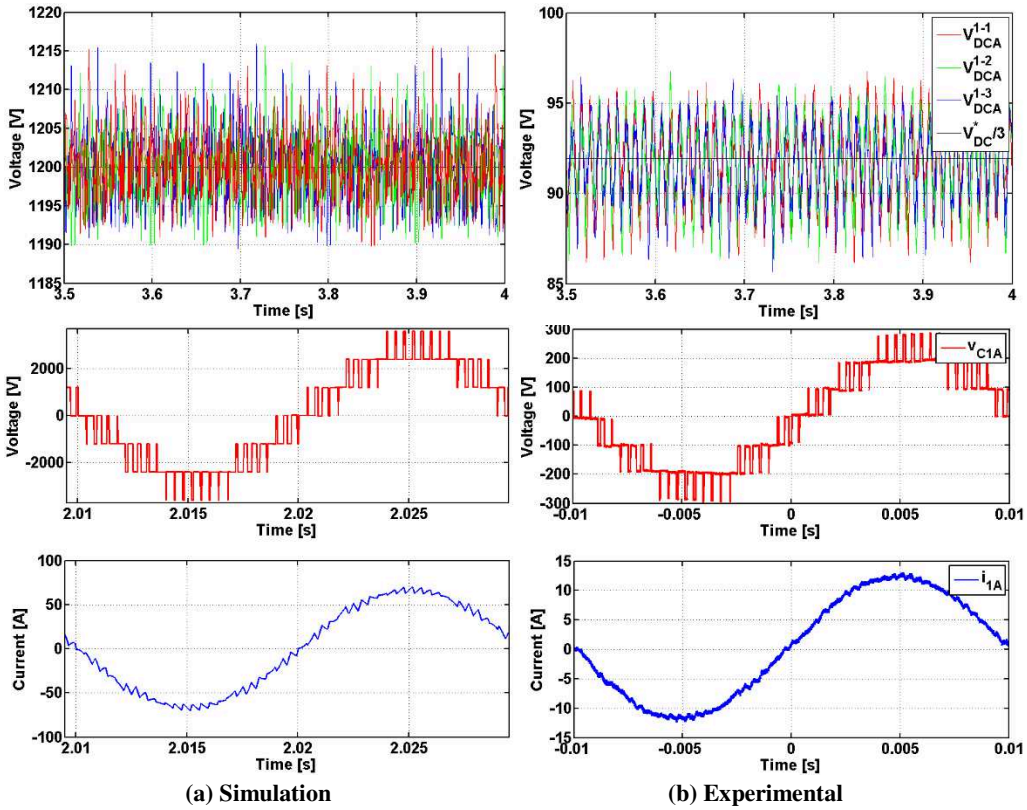


Figure 9.37 Comparison between experimental and simulation results for Modulated Model Predictive current Control: DC-Link voltages, Converter voltage, AC voltage and current.

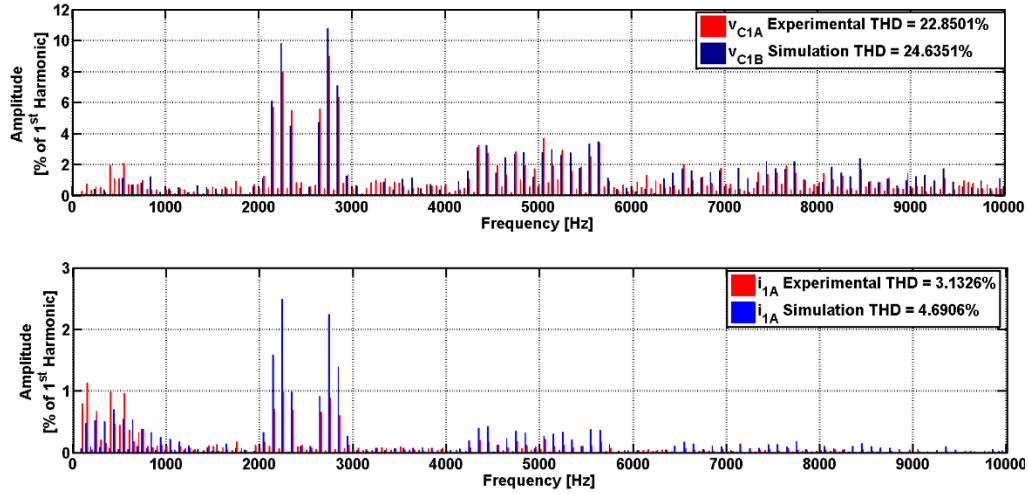


Figure 9.38 Comparison between experimental and simulation results for classic Modulated Model Predictive current Control: Converter voltage and AC current harmonic content.

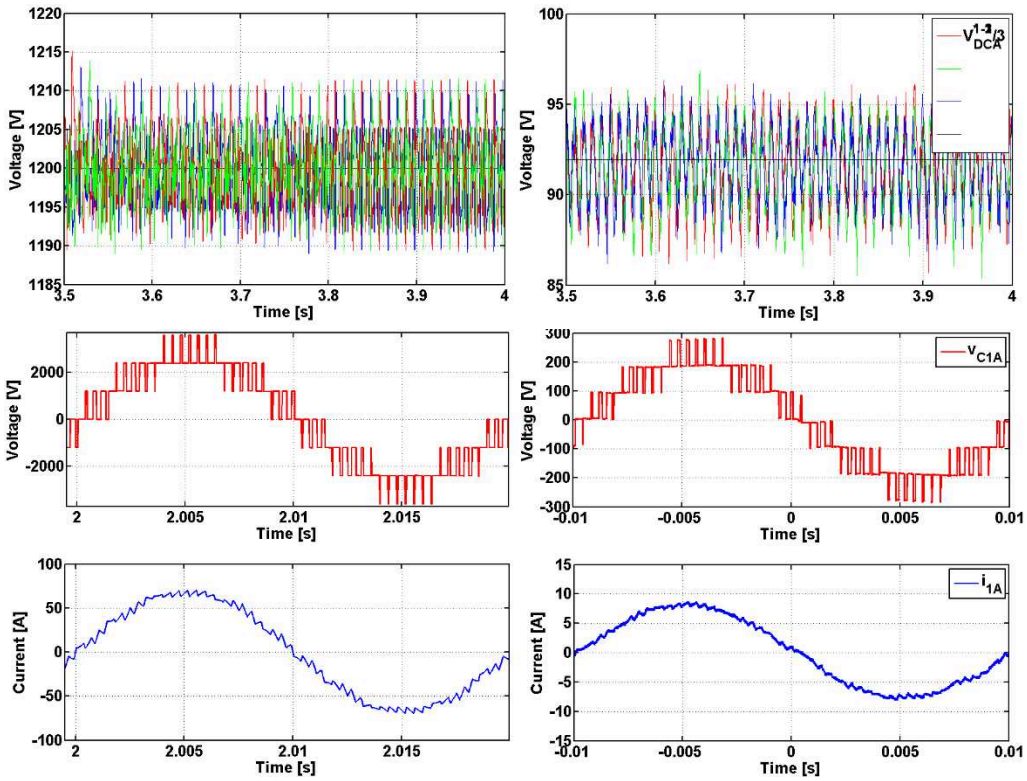


Figure 9.39 Comparison between experimental and simulation results for Modulated Model Predictive DC-Link voltage/current Control: DC-Link voltages, Converter voltage, AC voltage and current.

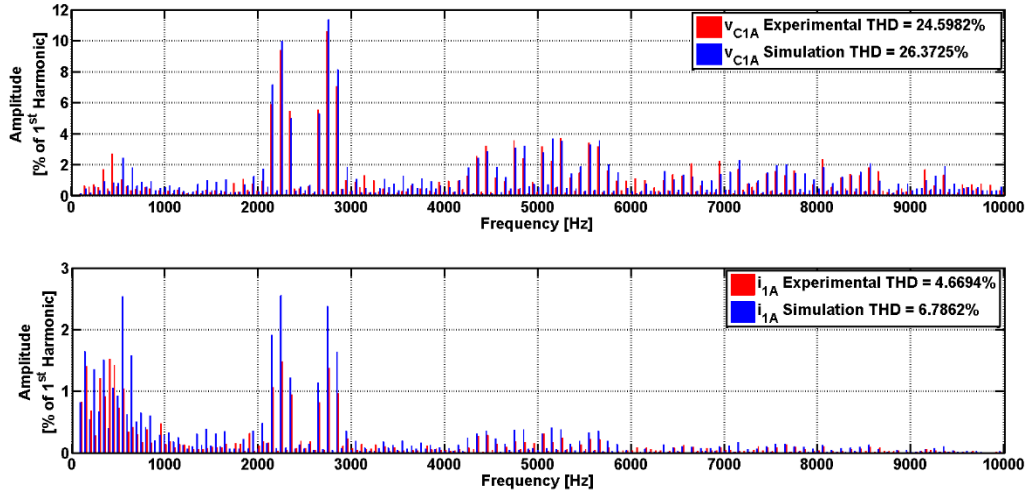


Figure 9.40 Comparison between experimental and simulation results for Modulated Model Predictive DC-Link voltage/current Control: Converter voltage and AC current harmonic content.

In Figure 9.37 the waveform obtained using the M^{2}PC current control technique described in this chapter, experimentally on the UNIFLEX-PM demonstrator and in simulation, are compared. As it can be noted, DC-Link voltages, converter voltage and AC current on phase A, port 1 of the UNIFLEX-PM demonstrator present similar waveforms, with the only difference in the

different operating point between simulation and experimental tests and the absence of a grid connection on port 2.

However, similarly to the results obtained with DBC and MPC, the different operative points affects the amplitude of the AC current and, thus the filtering capability of the line inductance, considered of the same value in both simulation and experimental tests.

This results in the harmonic contents of Figure 9.38, where the converter voltage presents a similar spectrum in both cases with additional low frequency harmonics produced by the real converter and mainly related with noise measurements and Dead-Times. On the other hand the AC current spectrum presents a visible difference between simulation and experimental tests. In fact even if low frequency harmonics are provided by the real converter, the AC current THD results lower for the experimental tests as a consequence of the different operative point considered in simulation and experimental testing.

Similar results are obtained for M^2PC current / DC-link voltage control as shown in Figure 9.39 and Figure 9.40.

9.5 Chapter summary

In this chapter a control technique implementing an intrinsic modulation scheme in the predictive control algorithm, named M^2PC is proposed. In particular, the M^2PC technique is described in details considering two different control designs: a M^2PC current control with traditional PI DC-Link voltage control and an M^2PC current DC-Link voltage control that implement both the control variable regulation in a single control loop.

In contrast with the DBC proposed in Chapter 7, M^2PC does not necessarily requires an external DC-Link voltage control, since it is possible to include the DC-Link voltage control in the M^2PC cost function.

With respect to the MPC of Chapter 8, the intrinsic modulation scheme included in the M^2PC allows to obtain higher quality AC waveforms with a lower THD without excessively increase the required computational time necessary to run the control routine.

Simulation and experimental results has been carried out, considering the UNIFLEX-PM demonstrator SST topology; results shows that the control is able to operate effectively under several operating conditions providing a fast and accurate DC-Link voltage regulation.

Moreover the produced converter voltage and AC currents present low THD values, comparable with the ones obtained using the DBC method described in Chapter 7.

Chapter 10
Experimental results comparison, conclusions and further work in the area

This chapter presents a resume of the research work carried out in this PhD project, together with experimental results using the four proposed control strategies compared in several operative conditions, highlighting the advantages of M^2PC control and its wide capabilities.

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10.1 Motivation, design and control solutions for Universal and Flexible Power Management converter

In recent years the electrical grid, based on a passive structure, is facing several issues related with the high penetration of RES or, in general, weak grid conditions. In fact DG systems may affects negatively the produced power quality in terms of increased power interruptions, voltage regulation, harmonics content, voltage sag. To improve the grid stability and permanently solve these issues, the electrical power grid may be redesigned in a smart grid with multidirectional power flow. In this scenario power electronics represents an enabling technology for improving the reliability and the stability of the future electrical power grid. Between al possible power electronics converter topologies, multilevel converters represents an attractive solution to design high power converters using reliable medium power devices already available on the market. Multi-level converters presents several advantages with respect to the classic two-level converter in terms of output power quality, reducing the Total Harmonic Distortion of the output waveforms, and as a consequence, filtering requirements.

In particular, CHB converters presents several benefits, avoiding extra clamping diodes or capacitors as in NPC and FC converters, having an high modularity and requiring less components to achieve the same number of levels with respect to other multilevel topologies. CHB converters have been commercialized for very high power (up to 31MVA) application that require high power quality, as active filters, reactive power compensation, PEV and PHEV, grid interfacing of photovoltaic generation, uninterruptible power supplies and magnetic resonance imaging. Focusing in particular on grid interface applications, SSTs present several advantages. In fact SSTs use less copper and allow several control features that are not achievable with classic transformers as frequency, phase shift and power flow control.

Recently a CHB based SST has been realized as a demonstrator, during the UNIFLEX-PM project. The UNIFLEX-PM demonstrator has been designed with a three port structure; however it is possible to operate it as a standard two port SST, by disconnecting port 3 from the circuit. The cascaded converter structure is based on identical fundamental AC/AC cells; each cell is composed by four HBs, two capacitor and a Medium Frequency (MF) transformer. Two HBs are

used to implement the CHB converter on the two sides while the other two HBs are used to implement the DC/DC converter and provides the necessary insulation between grid and loads on different converter ports. In order to control the UNIFLEX-PM demonstrator, the recent advances in microcontroller and DSP technologies allows the implementation of novel and more sophisticated control techniques, in comparison with linear control techniques. Moreover, modulation techniques for multilevel converters may take advantage of the additional degrees of freedom present in multilevel converters. In this thesis the attention is focused on the predictive control family and four different control solutions has been implemented on the UNIFLEX-PM demonstrator using its two port configuration.

10.2 Experimental results comparison

Experimental results are obtained with the parameters of Table 7.1, Table 8.2 and Table 9.2 respectively for DBC, MPC and M^{2}PC. Regarding DBC a test is performed on the UNIFLEX-PM converter using the two proposed modulation techniques. The results are presented for port 1, phase A of the UNIFLEX-PM demonstrator and a sampling frequency of 5kHz.

Figure 10.1 show that, using DCM, even if a symmetrical converter is considered the device parasitic parameters and unbalances in the power flow of the single Back-To-Back cells cause an unbalance in the DC-Link voltages, which is reflected on the generated converter voltage and line current. In particular the line current presents a THD of more than 10%. On the other hand using the proposed technique the devices parasitic effects are compensated and the capacitor voltages are actively balanced, resulting in a line current THD of 6.5%. For this reason the DCM technique with active voltage balancing algorithm and parasitic effect compensation has been implemented with DBC.

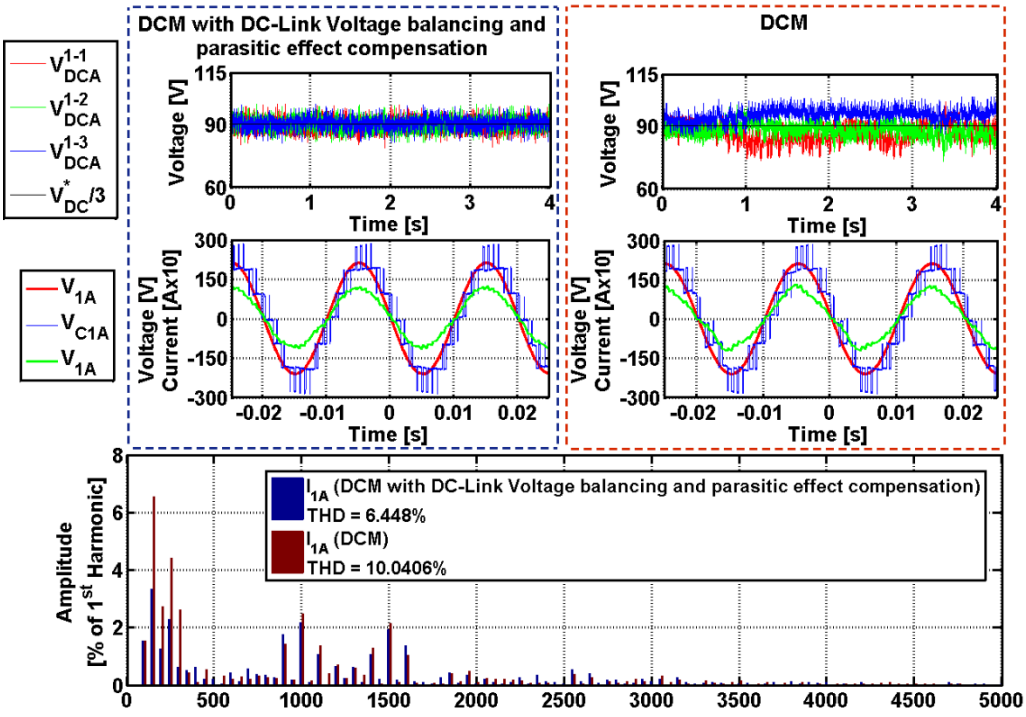

Figure 10.1 Dead-Beat current control performances with the two proposed modulation techniques for a sampling frequency of 2.5kHz.

In Figure 10.2 the produced converter voltages on port 1, phase A of the UNIFLEX-PM demonstrator with the four proposed controllers have been compared. The results show the peculiarity of the four controllers: DBC and M^{2}PC produce a pulse-width modulated waveform with constant switching frequency equal to half of the sampling frequency, while MPC produce a variable switching frequency waveform. This results in a higher grade of distortion on the line current as shown in Figure 10.3.

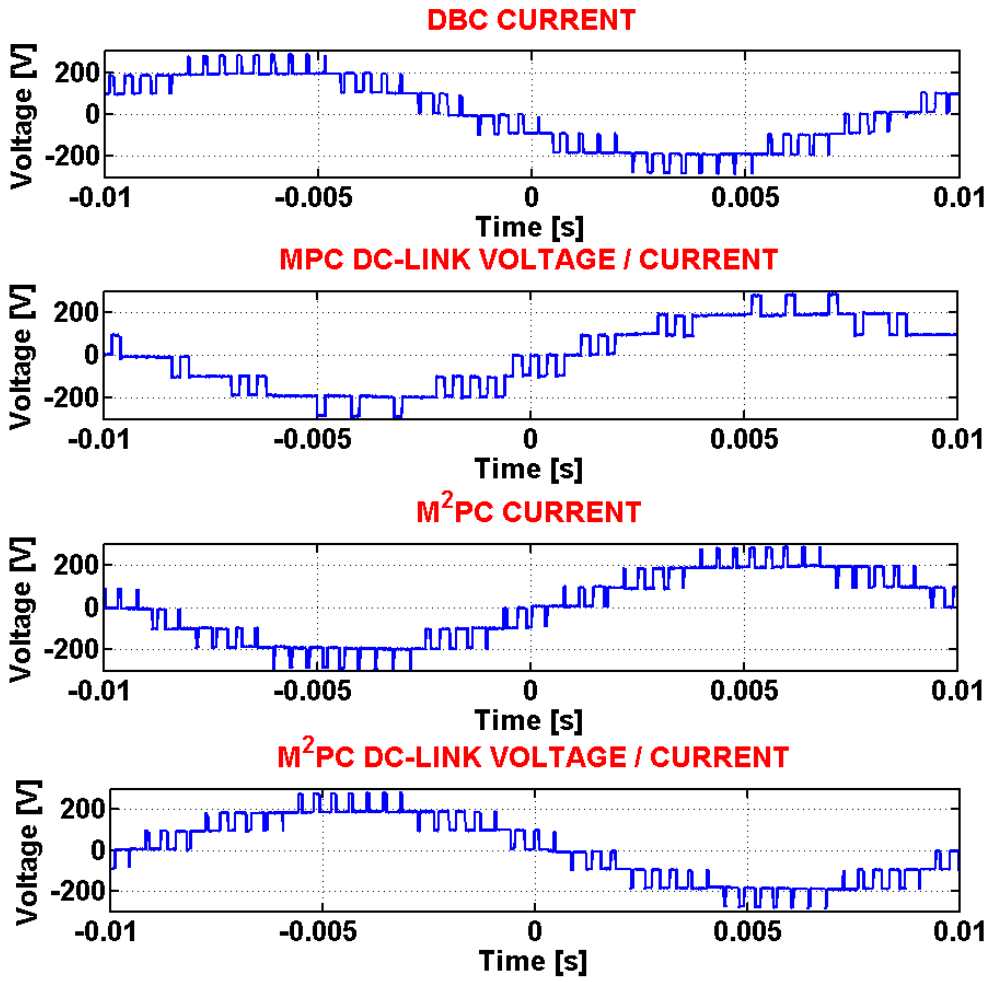

Figure 10.2 Produced converter voltages on port 1, phase A with the four proposed controllers.

In fact, looking at the converter voltage spectrum for the four implemented controllers shown in Figure 10.4, it is possible to see that while DBC produce a harmonic content mainly located around the switching frequency, MPC voltage harmonics are spread over all the spectrum below the switching frequency. In particular the produced harmonics are only partially attenuated by the line inductor resulting in a higher current harmonic content as shown in Figure 10.5.

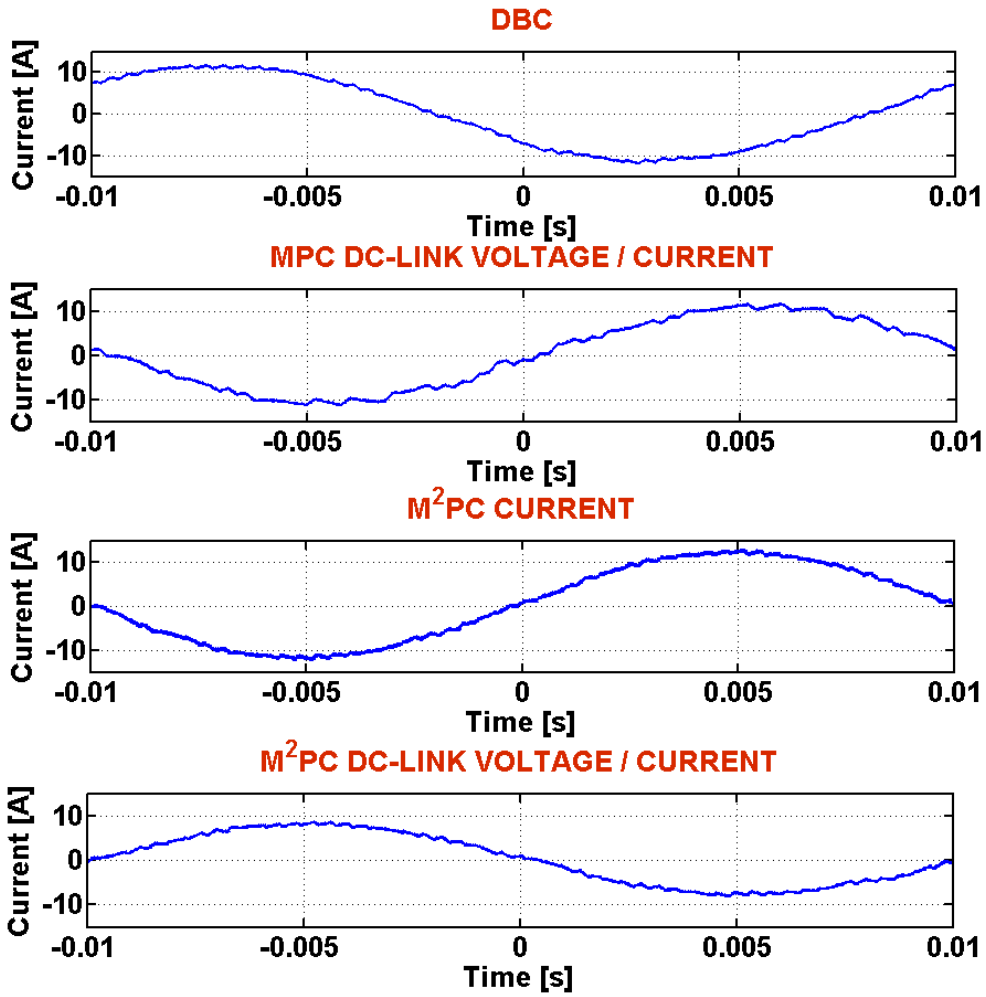

Figure 10.3 Produced line currents on port 1, phase A with the four proposed controllers.

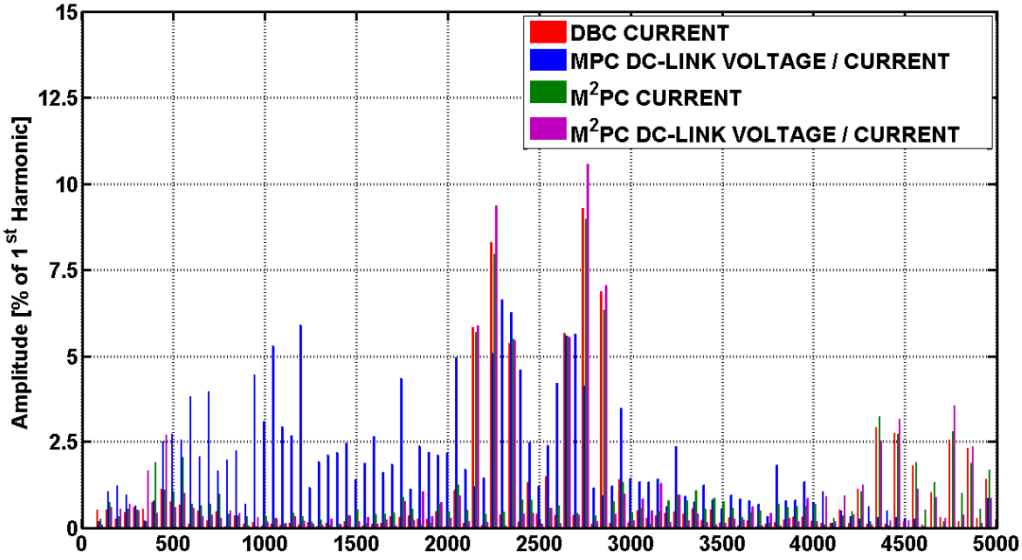

Figure 10.4 Converter voltage harmonic contents on port 1, phase A with the four proposed controllers.

On the other hand M²PC current control provides similar performances compared with DBC, in term of converter voltage and current spectrum, even if a reduced amount of low frequency harmonics are still present. This behaviour is mainly due to the empiric approach used to calculate the switching instants. Including the DC-Link voltage control inside the M²PC cost function, the current / DC-Link voltage controller, the harmonic content slightly increase whilst maintaining better performances respect to MPC.

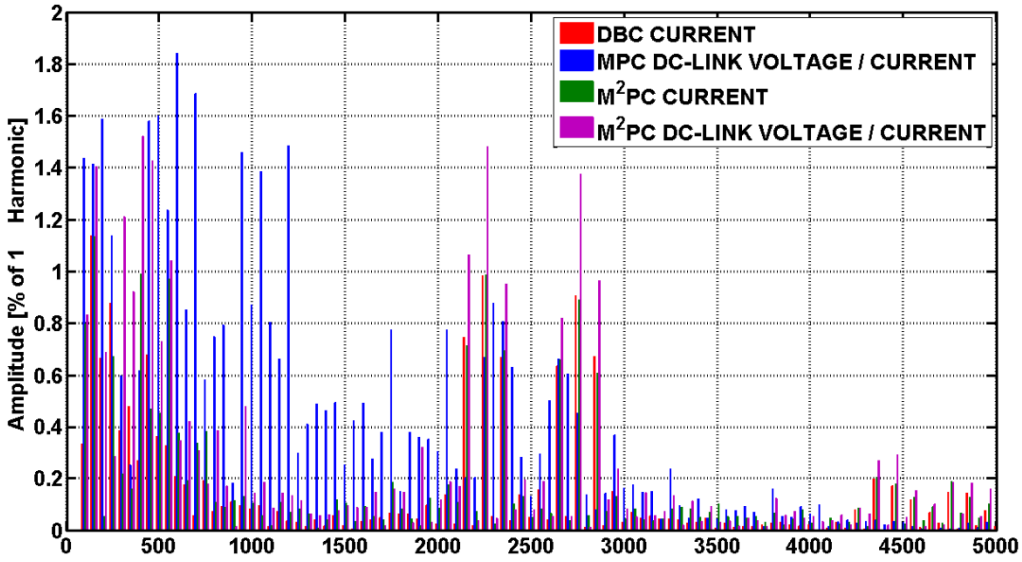

Figure 10.5 Line current harmonic contents on port 1, phase A with the four proposed controllers.

In Table 10.1 the converter waveforms THD, obtained with the four controllers, are compared. The lower THD value is obtained with DBC, but M²PC current control presents comparable converter voltage and line current THD. Using M²PC current / DC-Link voltage control the THD values increases, but still remains below to the one obtained with MPC.

Table 10.1 Converter voltage and line current THD on port 1, phase A with the four proposed controllers.

CONTROL	*CONVERTER VOLTAGE THD [%]*	*AC CURRENT THD [%]*
DBC CURRENT	**21.8002**	**2.8581**
MPC DC-LINK VOLTAGE / CURRENT	**25.6027**	**6.2999**
M²PC CURRENT	**22.8501**	**3.1326**
M²PC DC-LINK VOLTAGE / CURRENT	**24.5982**	**4.6694**

Another important point to analyse in order to evaluate the four control performances is the DC-Link voltage controller implementation. The active/reactive power and the DC-Link voltages on each phase of port 1 are shown, respectively, in Figure 10.6 and Figure 10.7 when an active power step from 0kW to 3kW is requested. The active power reference step is smoothed using a ramp generator in order to meet the desired active power reference in 0.1s. This is required in order to avoid that the dynamics of the DC/DC converter in each UNIFLEX-PM demonstrator cell affects the behaviour of the DC-Link voltage control.

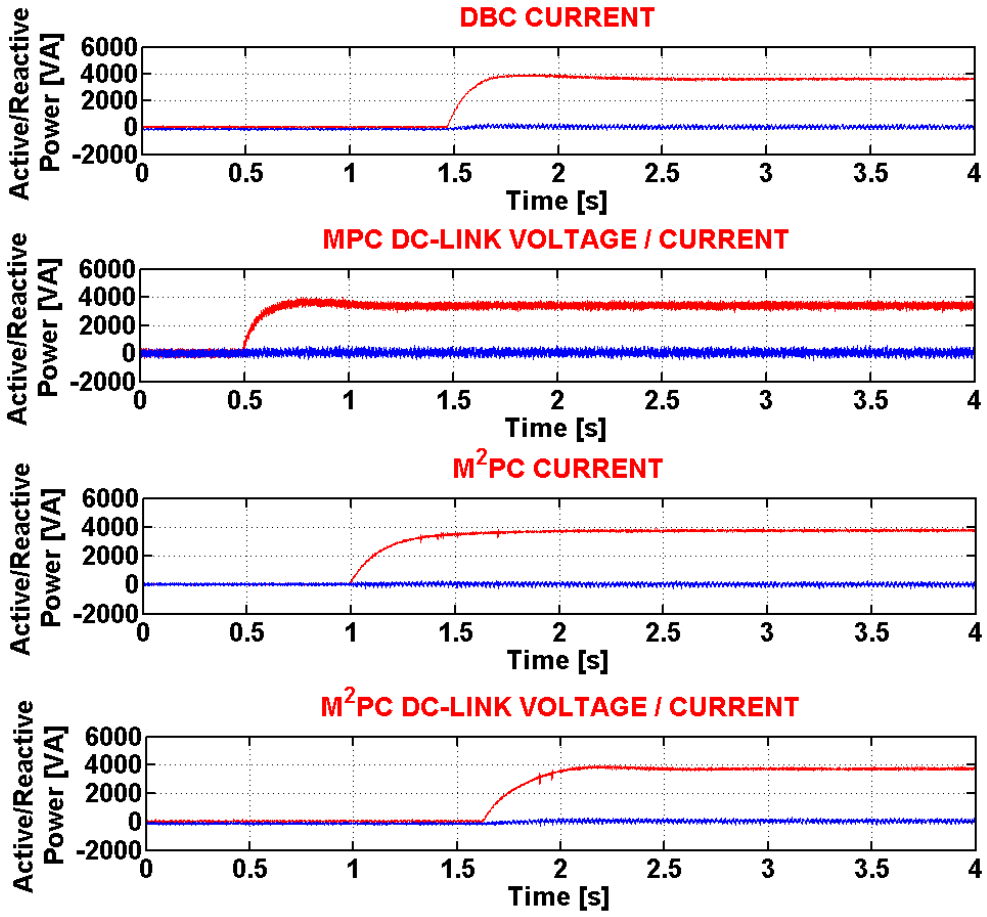

Figure 10.6 Active and reactive power transients on port 1with the four proposed controllers during an active power reference step change.

When the active power step is applied, all the four controllers present a similar dynamic on tracking the active power reference. However several differences can be appreciated observing the DC-Link voltages. In particular DBC has the worst performances resulting in largest DC-Link voltage excursion (approximately 50V) and requiring almost 1s to recover the DC-Link

voltage tracking, while MPC has the best performances, resulting in a voltage excursion of 25V and recovering the DC-Link voltage tracking in approximately 0.3s. On the other hand, M^{2}PC current control with the same PI DC-Link voltage controller of DBC results in a voltage excursion of 25V but it requires 1.5s to recover the DC-Link voltage tracking. M^{2}PC current / DC-Link voltage control presents a voltage excursion of 25V but and recovers the DC-Link voltage tracking in approximately 0.5s.

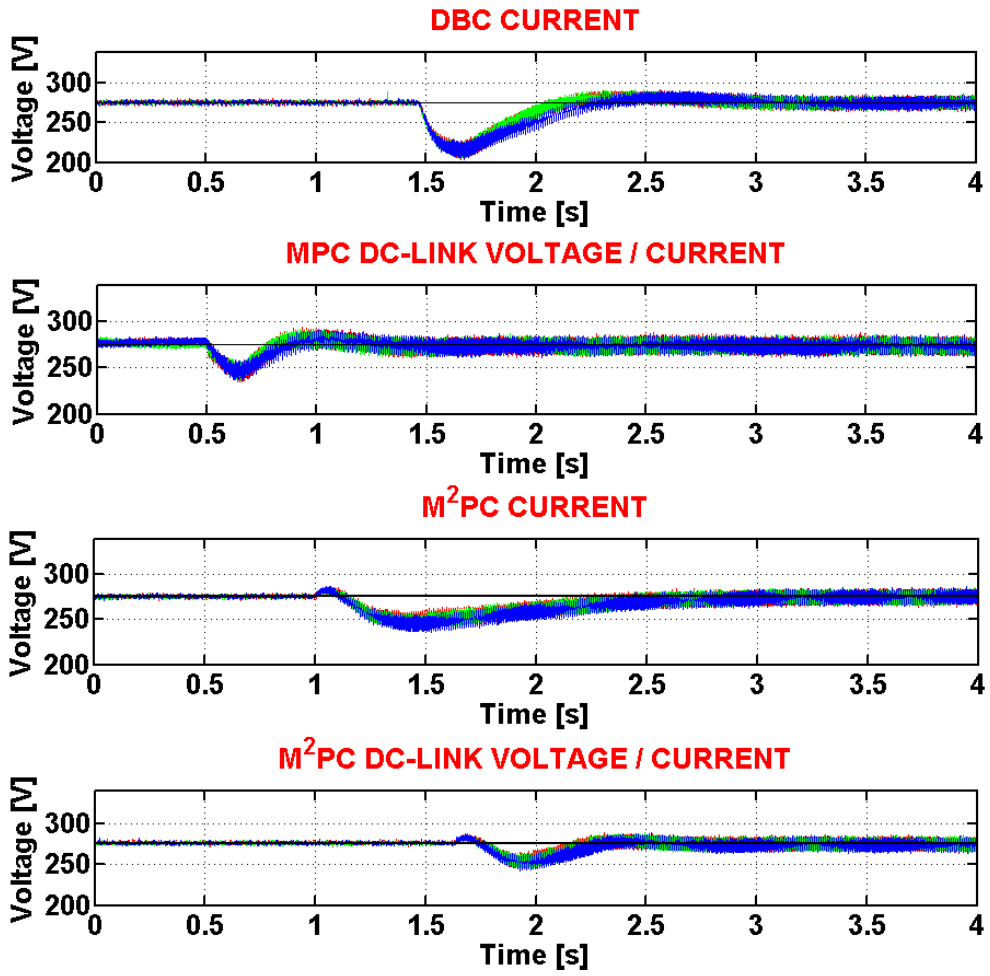

Figure 10.7 DC-Link voltages on port 1with the four proposed controllers during an active power step.

In Table 10.2 the DC-Link voltage excursion and transient duration, obtained with the four controllers, are compared. The best performances are obtained with MPC, but M^{2}PC DC-Link/current control presents comparable values.

Table 10.2 DC-Link voltage maximum excursion and transient duration with the four proposed controllers.

CONTROL	*DC-LINK VOLTAGE EXCURSION [V]*	*DC-LINK VOLTAGE TRANSIENT DURATION [%]*
DBC CURRENT	**50**	**1**
MPC DC-LINK VOLTAGE / CURRENT	**25**	**0.3**
M^2PC CURRENT	**25**	**1.5**
M^2PC DC-LINK VOLTAGE / CURRENT	**25**	**0.5**

10.3 Achievement to date

During this PhD research four different control strategies and two modulation techniques, particularly designed for high-power CHB, have been proposed, designed and implemented on the UNIFLEX-PM demonstrator. The converter topology has been realised with the specific purpose of finding a viable a cost effective solution to provide the requested flexibility of the future Smart-Grid. In fact, the UNIFLEX-PM demonstrator topology is capable to replace the transformer in a MV substation with enhanced power routing capabilities with respect to classical solutions.

The first control technique that has been proposed is a Dead-Beat current control with an external PI DC-Link voltage control loop. Dead-Beat control is based on the prediction of the system response to a change in control variables in order to achieve (ideally) zero error in the next one, two or more sampling periods. The output of this control is an average value (i.e. continuous) and it is chosen by imposing the current value at the next sampling period equal to the desired reference. The Dead-Beat current control has been implemented using a 2^{nd} order derivative approximation in order to achieve accurate operation [93], [175], [176], [183]. The control action is applied to the converter by a modulation technique, particularly suitable for high-power CHB converters and named Distributed Commutation Modulation, has been designed and implemented on the UNIFLEX-PM demonstrator to work in conjunction with the Dead-Beat current control. The DCM strategy aim to minimize the converter commutations and distribute them, for any amplitude of the voltage reference, amongst the different converter cells [184], [185]. In order to improve the operating performance when power unbalance between the cells is present, an extension to DCM algorithm has been also proposed with the aim of minimizing the unbalance of the DC-Link voltages amongst the different converter cells in order to obtain high-quality waveforms and maintain converter modularity. Moreover the devices voltage drops and on-state resistances are compensated using this technique [172], [186].

The second implemented control solution is a finite control set Model Predictive Control, widely considered as a promising approach for the control of power converters, due to its fast dynamic response, easy inclusion of nonlinearities and system constraints, ability to incorporate nested

control loops in only one loop and the flexibility to include other system requirements in the controller. MPC, considers a model of the system in order to predict its future behaviour over a time horizon. On the basis of this model, MPC solves an optimization problem where a sequence of future actuations is obtained by minimizing a cost function, which represents the desired behaviour of the system. The best performing actuation is then applied and the calculations are repeated at every sample period. MPC aim to control directly AC current and DC-Link voltages using only one global cost function on each phase without the need of additional PI control loops [176], [181]. Simulation and experimental results show a good transient response in all the cases taken into account; however, being one state applied for the whole sampling interval without using any PWM technique, the AC current presents a larger value of THD, compared with DBC. This behaviour is the consequence of the low frequency harmonic produced by the converter using MPC that worsen the line inductance filtering capabilities. On the other hand the DC-Link voltage controller results in having a fast dynamics without requiring an excessive effort to appropriately tune the cost function weights. In conclusion MPC performances are worsened by the absence of a PWM technique in the state selection.

The last control technique that has been introduced is denoted as Modulated Model Predictive Control and includes a suitable modulation scheme in the cost function minimization of the MPC algorithm. To avoid increasing the complexity of the controller, especially in the case of multi-objective cost functions, M^2PC is based on the evaluation of the cost function for a selected number of states. A modulation scheme particularly suitable for high power converters, and similar to the one used in DBC control is reproduced with the switching times calculated on the basis of the cost function values for the selected states. The control has been proposed in two different versions: Modulated Model Predictive Current Control with external PI DC-Link control loop and M^2PC with both AC current and DC-Link voltage included in the cost function, appropriately weighted. In the first case the M^2PC control presents performances similar to DBC, in terms of AC current THD and transient response; in the second case the M^2PC control presents performances that can be considered as a trade-off between DBC current quality and MPC DC-Link voltage regulation capabilities. Even if further investigations might be needed on the

theoretical stability demonstration of M²PC, the proposed technique represents an attractive solution to implement a fast dynamics, easy tuning control on high power, low switching frequency multilevel converters. In fact M²PC allows retention of all the advantages of MPC as multi-objective control strategy, but produces an increased performance in terms of power quality. M²PC has been proposed for both current control, requiring a PI DC-Link voltage controller, and current/DC-Link voltage control, avoiding additional control loops [182], [187], [188]. Simulation and experimental results shows performances that represents a trade off between the optimal current tracking of DBC and the fast DC-Link voltage transient response of MPC.

The obtained experimental results on the UNIFLEX-PM demonstrator has been compared in the previous section and the results are resumed in Table 10.3. On the basis of these results, it can be stated that M²PC DC-Link voltage current control represent the best control solution among the four that have been considered because of its capability to maintain an high power quality and DC-Link voltage tracking without the need of an external DC-Link voltage control loop.

Table 10.3 Experimental result comparison.

CONTROL	*AC CURRENT THD [%]*	*DC-LINK VOLTAGE EXCURSION [V]*	*DC-LINK VOLTAGE TRANSIENT DURATION [%]*
DBC CURRENT	**2.8581**	**50**	**1**
MPC DC-LINK VOLTAGE / CURRENT	**6.2999**	**25**	**0.3**
M²PC CURRENT	**3.1326**	**25**	**1.5**
M²PC DC-LINK VOLTAGE / CURRENT	**4.6694**	**25**	**0.5**

All these novel advances have published by the author of this thesis in internationally recognised peer reviewed conferences and journals.

10.4 Further work in the area

As shown in this thesis, predictive control and, in particular, Finite Control Set Model Predictive Control represent an attractive solution to control high power multilevel converters and presents several advantages such as fast dynamic response, no need of modulation, easy inclusion of nonlinearities and constraints of the system, possibility of incorporating nested control loops in only one loop and the flexibility to include other system requirements in the controller. However several disadvantages can also be identified:

- The absence of a modulation scheme affect the overall MPC performances especially when a low switching frequency, and thus a low sampling frequency, are required as in case of high power converters.
- MPC is in general computationally heavy. State variables predictions and cost function have to be evaluated for any possible applicable converter state and, in case of multilevel converters, the number of possible states increase exponentially with the number of voltage levels.
- MPC is sensitive to not negligible model parameters variations. In particular, when a high power grid connected converter is considered the variation in the grid impedance might affect the MPC overall performances.
- Even if MPC is commonly proposed for power converters control, the theoretical background is limited and it results in not having a deterministic procedure to choose the cost function weights values.

This research project proposes the M^2PC technique, a solution that deals mainly with the first two points. However other solutions are currently been researched; an option to reduce the computational effort is to use a cost function for each converter cell, in case of modular converters, using a technique denoted as Distributed Model Predictive Control. Another option that allow the use of a suitable modulation technique is to optimize the cost function offline finding an expression for the converter voltage reference that has to be applied to the converter using a modulator.

Regarding the third point a grid impedance estimator can be used to work in parallel with the predictive controller or directly within the MPC cost function minimization algorithm, on the basis of current and converter voltage sampling at different sampling instants.

Regarding the fourth point it might be possible to apply the Lyapunov stability theory to MPC, in a discrete time domain. In particular the control stability may be verified only for a certain range of cost function weights values giving useful indication in this direction.

Considering a wider range of power electronics applications for MPC it is worth to be mentioned that SiC and GaN devices are defining new standards for power electronics converters, in terms of power density and/or maximum switching frequency at rated power. These new family of devices may allow MPC implementation at higher sampling frequency and it may result in improving the quality of the voltage produced by the converter. In this case the goals to achieve may be:

- Provide the necessary prediction accuracy over a smaller sampling interval; it requires low noise measurements and may also include additional filters on the measurement that have to be compensated by the control.
- Make MPC implementation on real control system feasible at the higher sampling frequencies (as example higher than 100kHz); it may require to implement MPC control directly on FPGAs that ensure higher clock frequency with respect to a DSP.

In conclusion it can be stated that MPC represents nowadays a valid alternative to traditional control techniques for high power multilevel convert control, providing faster dynamic response to transients. Several modifications to the classical MPC algorithm can be made in order to improve produced converter voltage quality and reduce the computational time on the control circuitry. Moreover, predictive control may represent the state of the art in power electronics converters in the next decades benefiting of advance in both power electronics and control technologies to increase its feasibility in practical implementations, especially at high sampling frequencies

Appendix A
Supply Voltage Prediction

The supply voltage prediction is necessary to accurately running the four proposed controllers. A methodology, already proposed in [103] and based on the assumption that the supply voltage maintain a repetitive waveform, is considered and described in details in the following paragraphs.

A.1 Supply voltage prediction derivation

Considering the supply voltage on phase A, port 1 of the UNIFLEX-PM converter, $v_{1A}(t)$, and its discrete time representation at the sampling instant t_k+T_s it is possible to obtain the following equation:

$$v_{1A}(t_k + T_s) = \frac{1}{T_s}\int_{t_k}^{t_k+T_s} v_{1A}(t)\,dt \qquad (A.1)$$

The integral is calculated numerically using a trapezoidal approximation of the integral and resulting in the following equation:

$$\frac{1}{T_s}\int_{t_k}^{t_k+T_s} v_{1A}(t)\,dt = \frac{1}{T_s}\frac{v_{1A}(t_k + T_s) + v_{1A}(t_k)}{2}T_s = \frac{v_{1A}(t_k + T_s) + v_{1A}(t_k)}{2} \qquad (A.2)$$

In this work the supply voltage waveform has been considered perfectly cyclical and a repetitive. The previous supply voltage period is therefore stored and used for the prediction calculation instead of the current one as shown by the following equation:

$$\frac{1}{T_s}\int_{t_k}^{t_k+T_s} v_{1A}(t)\,dt \cong \frac{v_{1A}(t_k + T_s - \mu T_s) + v_{1A}(t_k - \mu T_s)}{2} \qquad (A.3)$$

Where μ represent the number of samples at a sampling time T_s for each period of the supply voltage, defined from its angular frequency ω as shown in (A.4).

$$\mu = \frac{2\pi}{\omega T_s} \qquad (A.4)$$

In (A.4) ω represents the angular frequency of the supply voltage. Clearly the procedure described before is completely iterative and allow to provide a filtered supply voltage prediction approximation using the following general expression:

$$v_{1A}(t_k + iT_s) \cong \frac{v_{1A}(t_k + iT_s - \mu T_s) + v_{1A}(t_k + iT_s - T_s - \mu T_s)}{2} \qquad (A.5)$$

A.2 Simulation results

Simulation results are shown to prove the effectiveness of the proposed supply voltage prediction. In Figure A.0.1 in case of ideal supply voltage and using a sampling frequency of 5kHz it is possible to appreciate the accurate generation of the supply voltage prediction at the sampling instants t_k+T_s and t_k+2T_s.

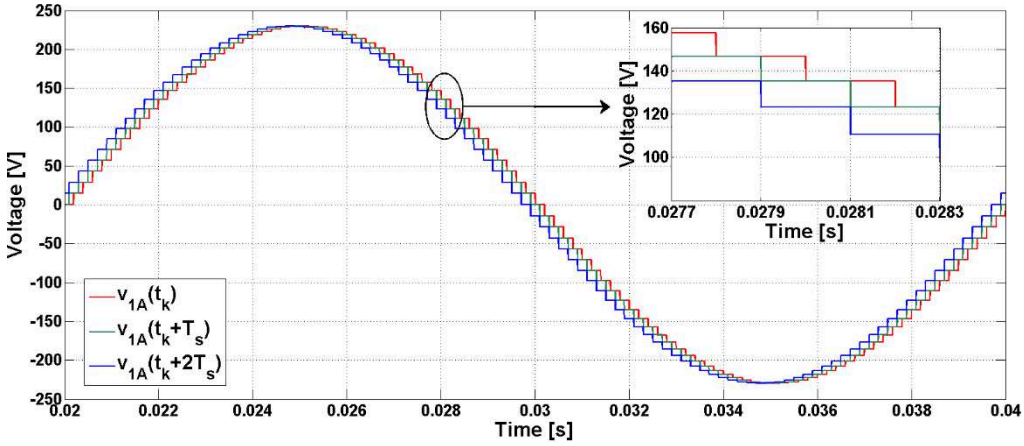

Figure A.0.1 Supply voltage prediction in the case of ideal supply voltage.

The same simulation has been carried out considering $v_{A1}(t_k)$ corrupted by noise on measurements and the results are shown in Figure A.0.2. Even if the measurement noise affects the supply voltage predictions, being the voltage step between two sampling instants not constant as in the ideal case, the produced supply voltage predictions are still acceptable, even if the overall control will be slightly affected.

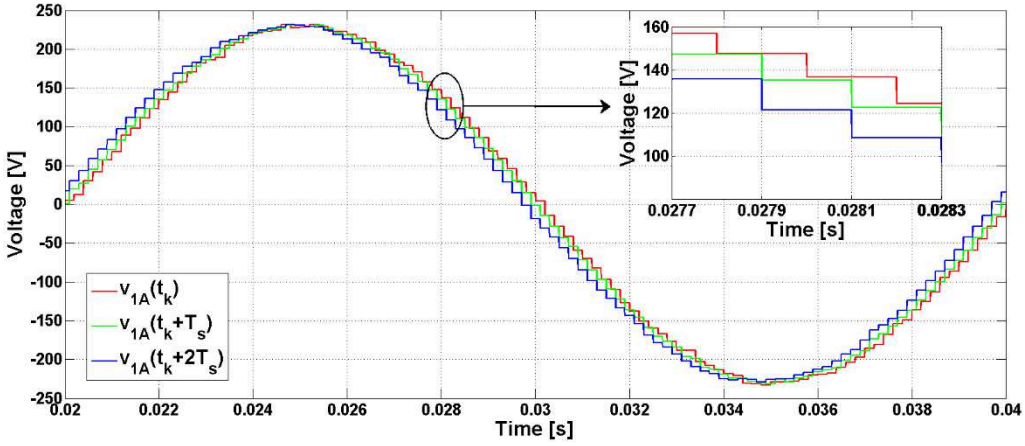

Figure A.0.2 Supply voltage prediction in the case of supply voltage corrupted by noise on the measurement.

Appendix B
Proportional-Integral controller design for the DC-Link voltage controller

In this appendix the tuning of the PI controller, used for the DC-Link voltage loop in conjunction with DBC and M^2PC current control, is described. The control is at first designed in continuous time domain and it is then shown that the same tuning can be used for a digital implementation by means of discretisation at the sampling frequency T_s.

B.1 Plant description

Considering the DC-Link voltage control implemented only on port 1 and that an additional algorithm is used in the current control to balance the DC voltage on each capacitor of each phase, the circuit shown in Figure B.0.1 can be used for the PI control design with the parameters reported in Table 3.1.

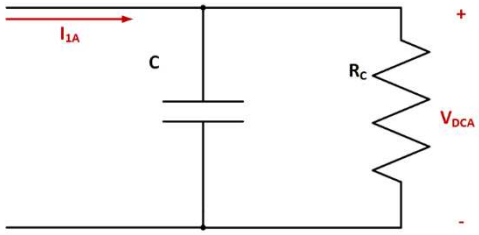

Figure B.0.1 Circuit used for DC-Link voltage PI controller tuning on phase A.

V_{DCA} represents the total DC-Link voltage on one phase, I_{1A} is the DC current flowing in the circuit, C is the DC-Link voltage capacitance and R_C is a resistance that represent the losses in the DC-Link circuit and DC/DC converter. Moreover, as described in details in section 7.1.3 for DBC, the current control has a fast dynamics with a negligible effect on the DC-Link voltage control, resulting in the block scheme of Figure B.0.2.

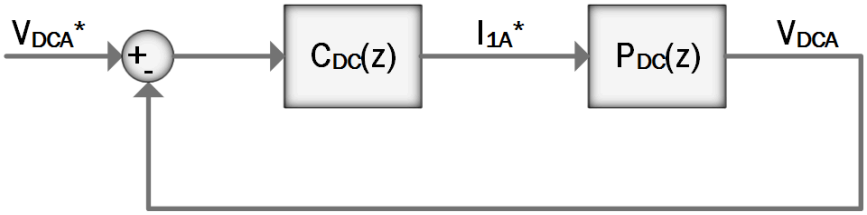

Figure B.0.2 Block scheme for DC-Link voltage PI control.

On the basis of this consideration the PI controller, described by $C_{DC}(z)$, is able to directly provide the desired DC current I_{1A}^* to the DC-Link circuit, described by $P_{DC}(z)$, in order to maintain the total DC-Link voltage V_{DCA} regulated at the desired value V_{DCA}^*. The continuous time transfer function $P_{DC}(s)$ is derived from the circuit equation as shown below.

$$I_{1A}(t) = C\frac{dV_{DC,A}(t)}{dt} + \frac{V_{DC,A}(t)}{R_C} \tag{B.1}$$

$$P_{DC}(s) = \frac{V_{DC,A}(s)}{I_{1A}(s)} = \frac{R_C}{1 + sR_CC} \tag{B.2}$$

It is clearly possible to obtain the digital approximation of $P_{DC}(s)$ considering the discretized model in (B.3) and applying the z-transformation as follows.

$$V_{DC,A}(k+1) = \delta_1 V_{DC,A}(k) + \delta_2 I_{1A}(k) \tag{B.3}$$

$$P_{DC}(z) = \frac{V_{DC,A}(z)}{I_{1A}(z)} = \frac{\delta_2}{z - \delta_1} \tag{B.4}$$

Where δ_1 and δ_2 are equal to the following values:

$$\delta_1 = e^{-\frac{1}{R_C C}T_s} \cong 1 - \frac{T_s}{R_C C} \tag{B.5}$$

$$\delta_2 = R_C\left(1 - e^{-\frac{1}{R_C C}T_s}\right) \cong \frac{T_s}{C} \tag{B.6}$$

Since R_C unknown a parametric analysis is shown in Figure B.0.3 in order to identify the control performances in function of R_C.

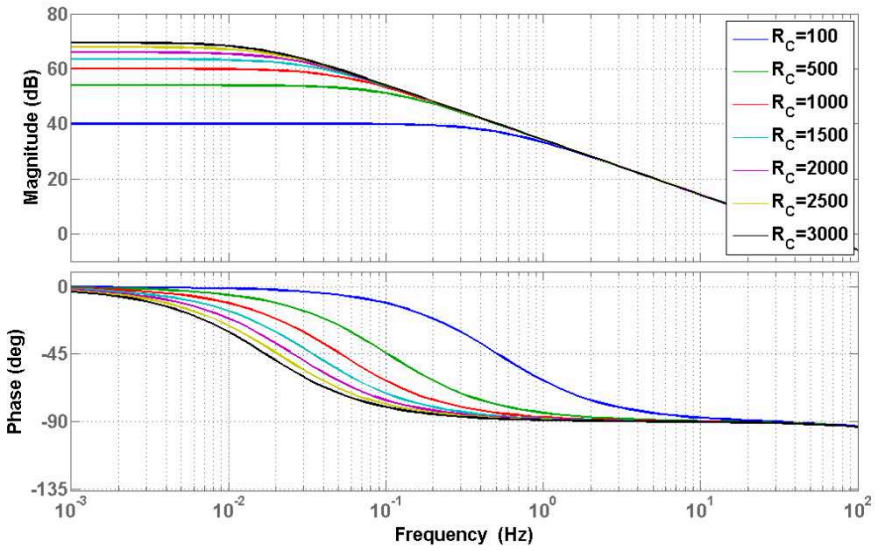

Figure B.0.3 Parametric analysis of $P_{DC}(z)$ for variation of R_C.

From Figure B.0.3 it is clear that the lower is the value of R_C, more the control gain have to be higher to achieve the desired phase margin φ_m and crossover frequency ω_c. The PI control is then tuned considering the worst case scenario between all the considered values of R_C. For this reason a value of R_C=*1kΩ* has been selected. In fact considering the parameters of Table 3.1, when the power is equally shared between the three fundamental cells on each phase, this value results in a DC/DC converter efficiency of around 96% when the losses in the capacitors are not considered.

B.2 PI DC-Link voltage control design

The PI control design is at first considered in a continuous time system, where the PI control transfer function, $C_{DC}(s)$, is derived as follows:

$$e(t) = V_{DC,A}(t) - V_{DC,A}{}^{*}(t) \tag{B.7}$$

$$I_{1A}{}^{*}(t) = K_{PDC}e(t) + K_{IDC}\int_0^t e(\tau)d\tau \tag{B.8}$$

$$C_{DC}(s) = \frac{I_{1A}{}^{*}(t)}{e(t)} = \frac{K_{IDC} + sK_{PDC}}{s} = K_{PDC}\left(1 + \frac{1}{s\tau_{IDC}}\right) \quad , \quad \tau_{IDC} = \frac{K_{PDC}}{K_{IDC}} \tag{B.9}$$

The transfer function of (B.2) is then expressed in function of frequency, i.e. $s=j\omega$, in order to calculate its gain, $|P_{DC}(j\omega)|$ and phase $\Phi_{DC}(j\omega)$:

$$P_{DC}(j\omega) = \frac{R_C}{1 + j\omega R_C C} = \frac{R_C(1 - j\omega R_C C)}{1 - \omega^2 {R_C}^2 C^2} \tag{B.10}$$

$$|P_{DC}(j\omega)| = \frac{R_C}{\sqrt{1 + \omega^2 {R_C}^2 C^2}} \tag{B.11}$$

$$\Phi_{DC}(j\omega) = \tan^{-1}(\omega R_C C) \tag{B.12}$$

From [189] it is possible to calculate the proportional gain K_{PDC} and integral gain K_{IDC} of the PI control, in order to achieve the desired phase margin φ_m and crossover frequency ω_c as follows.

$$\theta = 180° + \varphi_m - \Phi_{DC}(j\omega_c) \tag{B.13}$$

$$K_{PDC} = \frac{-\cos(\theta)}{|P_{DC}(j\omega_c)|} \tag{B.14}$$

$$K_{IDC} = \frac{\omega_c \sin(\theta)}{|P_{DC}(j\omega_c)|} \tag{B.15}$$

For the control of the DC-Link voltage a conservative design approach has been selected, considering the effect of noise and disturbances in the real system. In particular a crossover frequency equal to half of the AC voltage fundamental frequency and a phase margin of 82° has been selected, resulting in the following PI gain parameters.

$$\begin{cases} \varphi_m = 82° \\ \omega_c = 25Hz \end{cases} \rightarrow \begin{cases} K_{PDC} = 0.4823 \\ K_{IDC} = 10.4897 \end{cases} \tag{B.16}$$

The design is validated through the bode diagram analysis of the open loop and closed loop overall system transfer function, respectively $P_{DC}(s)C_{DC}(s)$ and $P_{DC}(s)C_{DC}(s)/[1+P_{DC}(s)C_{DC}(s)]$, as shown in Figure B.0.4 and Figure B.0.5.

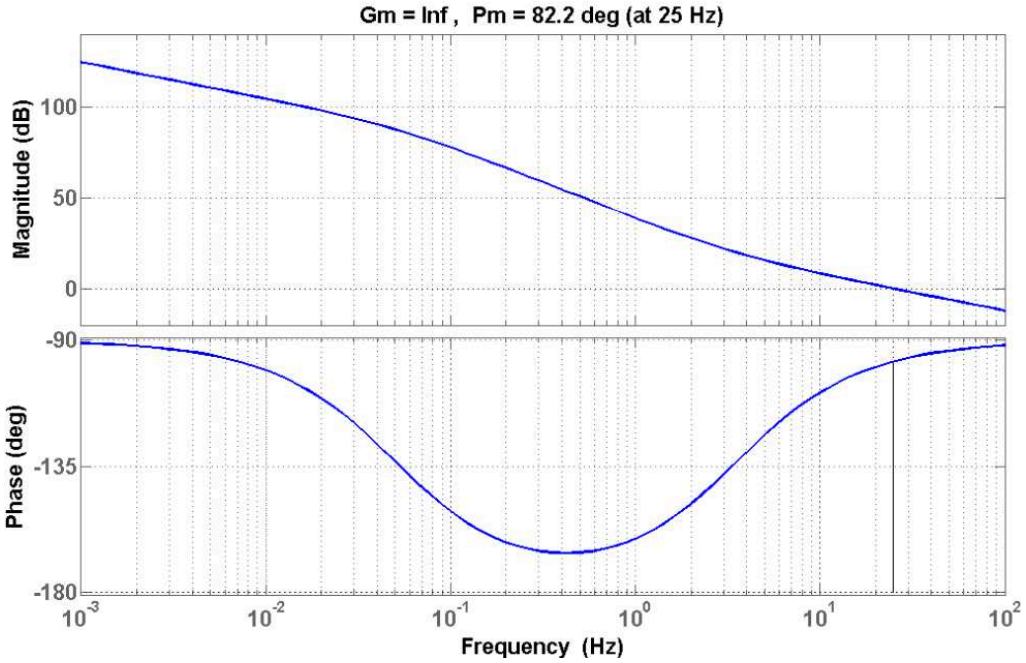

Figure B.0.4 Open loop continuous transfer function $C_{DC}(s)P_{DC}(s)$ and relative phase and gain margins.

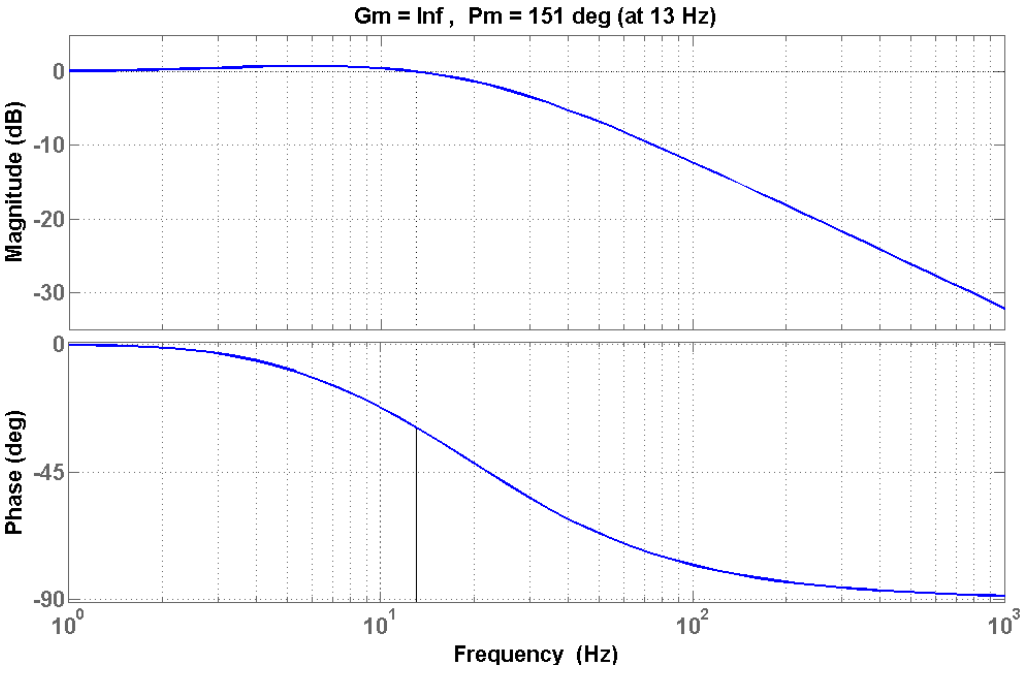

Figure B.0.5 Closed loop continuous transfer function $C_{DC}(s)\ P_{DC}(s)/[1+C_{DC}(s)\ P_{DC}(s)]$ and relative phase and gain margins.

The same control design is then discretised using the selected sampling time T_s and then tested in order to assure that the control performances of the continuous case are retained. The PI control transfer function, $C_{DC}(z)$, can be derived as follows, using Tustin approximation to approximate the integral term:

$$e(k) = V_{DC,A}(k) - V_{DC,A}{}^{*}(k) \tag{B.17}$$

$$I_{1A}{}^{*}(k) = K_{PDC}e(k) + \frac{T_s K_{IDC}}{2}[e(k+1) + e(k)] \tag{B.18}$$

$$C_{DC}(z) = \frac{I_{1A}{}^{*}(z)}{e(z)} = K_{PDC} + \frac{T_s K_{IDC}}{2}\frac{z+1}{z-1} \tag{B.19}$$

The controller is designed in the *w*-plane in order to maintain design specifications similar to the one for continuous systems [190] obtaining the following transfer functions $P_{DC}(w)$ for the DC circuit and $C_{DC}(w)$ for the controller.

$$w = \frac{2}{T_s}\frac{z-1}{z+1} \;\;,\;\; z = \frac{1 + \left(\frac{T_s}{2}\right)w}{1 - \left(\frac{T_s}{2}\right)w} \tag{B.20}$$

$$C_{DC}(w) = K_{PDC} + \frac{K_{IDC}}{w} = K_{PDC}\left(1 + \frac{1}{\tau_{IDC}w}\right) \tag{B.21}$$

$$P_{DC}(w) = \frac{\delta_2\left[1 - \left(\frac{T_s}{2}\right)w\right]}{(1-\delta_1) + \left(\frac{T_s}{2}\right)(1+\delta_1)w} = \frac{\frac{\delta_2}{1-\delta_1}\left[1 - \left(\frac{T_s}{2}\right)w\right]}{1 + \frac{\left(\frac{T_s}{2}\right)(1+\delta_1)}{1-\delta_1}w} = \frac{\zeta_1\left[1 - \left(\frac{T_s}{2}\right)w\right]}{1 + \zeta_2 w} \tag{B.22}$$

$$\zeta_1 = \frac{\delta_2}{1-\delta_1} \tag{B.23}$$

$$\zeta_2 = \frac{\left(T_s/2\right)(1+\delta_1)}{1-\delta_1} \tag{B.24}$$

It is then it is possible to calculate its gain, $|P_{DC}(j\omega)|$, and phase, $\Phi_{DC}(j\omega)$, of $P_{DC}(j\omega)$ from (B.20) and (B.22) as follows:

$$P_{DC}(j\omega) = \frac{\zeta_1\left[1 - \left(T_s/2\right)j\omega\right]}{1 + \zeta_2 j\omega} = \frac{\zeta_1\left\{\left[1 - \zeta_2\left(T_s/2\right)^2\omega^2\right] - j\omega\left[\zeta_2 + \left(T_s/2\right)\right]\right\}}{1 + {\zeta_2}^2\omega^2} \tag{B.25}$$

$$|P_{DC}(j\omega)| = \frac{\sqrt{\left[1-\zeta_2\left({}^{T_s}/_{2}\right)^2\omega^2\right]^2+\omega^2\left[\zeta_2+\left({}^{T_s}/_{2}\right)\right]^2}}{1+{\zeta_2}^2\omega^2} \tag{B.26}$$

$$\Phi_{DC}(j\omega) = \tan^{-1}\left(\frac{\left[\zeta_2+\left({}^{T_s}/_{2}\right)\right]}{\left[1-\zeta_2\left({}^{T_s}/_{2}\right)^2\omega^2\right]}\right) \tag{B.27}$$

The same design rules used for the continuous time system are then applied to the digital system, using equations (B.13), (B.14) and (B.15). In this way, with the same control specifications of (B.16), but using the gain and phase of $P_{DC}(j\omega)$ at the crossover frequency obtained from (B.26) and (B.27) the following control constants are obtained.

$$\begin{cases}\varphi_m = 82^\circ \\ \omega_c = 25Hz\end{cases} \rightarrow \begin{cases}K_{PDC} = 0.4823 \\ K_{IDC} = 10.4892\end{cases} \tag{B.28}$$

The design is validated through the bode diagram analysis of the open loop and closed loop overall system transfer functions, respectively $P_{DC}(z)C_{DC}(z)$ and $P_{DC}(z)C_{DC}(z)/[1+P_{DC}(z)C_{DC}(z)]$, as shown in Figure B.0.6 and Figure B.0.7.

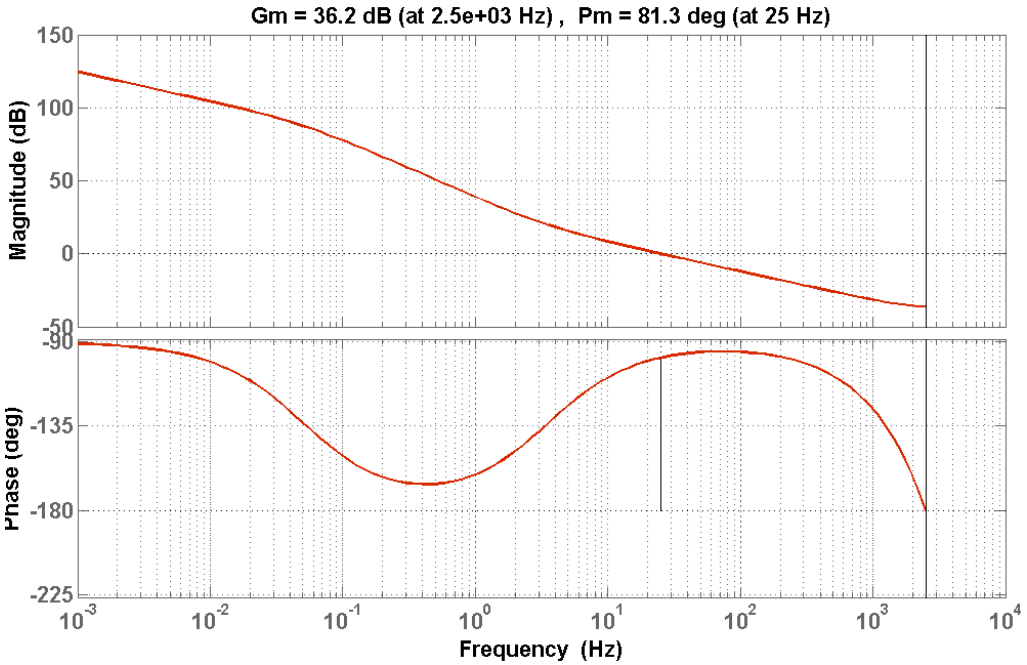

Figure B.0.6 Open loop discrete transfer function $C_{DC}(z)P_{DC}(z)$ and relative phase and gain margins.

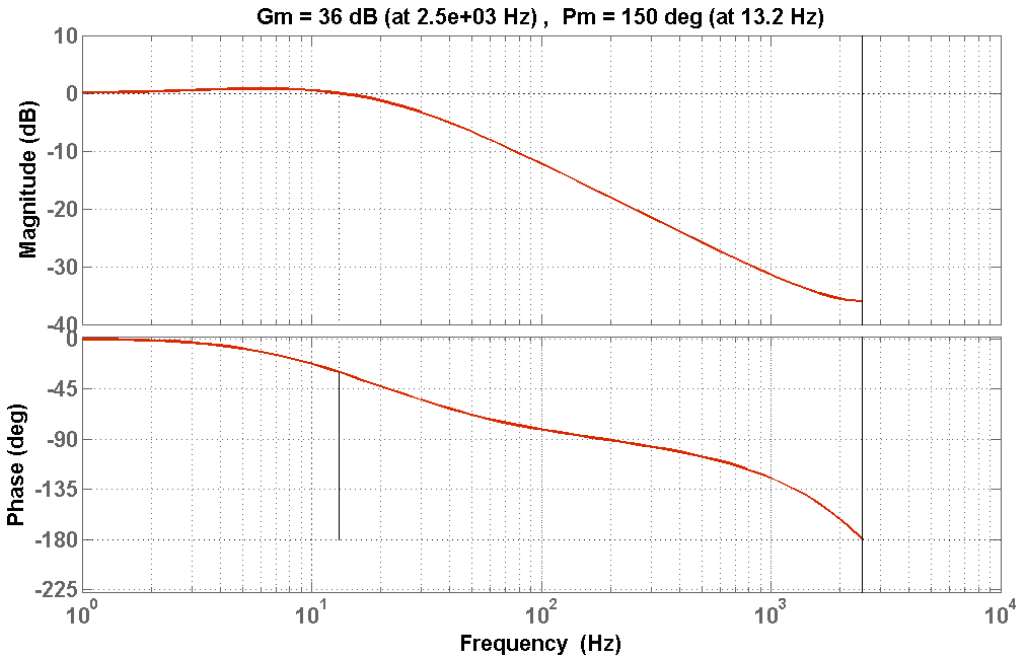

Figure B.0.7 Closed loop discrete transfer function $C_{DC}(z)\ P_{DC}(z)/[1+C_{DC}(z)\ P_{DC}(z)]$ and relative phase and gain margins.

The results show that the discretization have a negligible effect on the system performances being the time constants in $P_{DC}(s)$ and $C_{DC}(s)$ at a frequencies much lower than $2/T_s$. On the basis of all previous considerations the following values have been used in both simulation and experimental testing for DC-Link voltage PI control.

$$\begin{cases} K_{PDC} = 0.5 \\ K_{IDC} = 10 \end{cases} \tag{B.28}$$

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