High Frequency-Link Cycloconverters for Medium Voltage Grid Connection

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Abstract

As the deployment of renewable generation increases in the worldwide electrical grids, the development of distributed energy storage becomes more and more of an essential requirement. Energy storage devices connected at Medium Voltage allows for much higher powered deployments and this Ph.D. will focus on the power converter used to interface the energy storage device to the electrical grid.

Multi-level converters can be used to provide this interface without huge filtering requirements or the need of a Low Frequency step up transformer. However traditional Multi-level converter topologies require a large number of electrolytic capacitors, reducing the reliability and increasing the cost. Multi-level converters constructed from a Cycloconverter Topology do not require any additional electrolytic capacitors, however the High Frequency transformer, used to provide isolation has to be considerably larger.

This Ph.D. will investigate a novel hybrid converter topology to provide an interface between an energy storage device, such as a super-capacitor or battery, to the Medium Voltage grid, designed for high reliability and power density. This topology is called The Hybrid Cycloconverter Topology and is based on a Cycloconverter Topology connected to an auxiliary 3-Phase VSI.

A comprehensive simulation study is carried out to investigate the semiconductor losses of this novel converter topology and compared against two alternative topologies. An experimental converter is constructed to validate the theory of operation and to justify its effectiveness.

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Contents

Chapter 1

Introduction

Our society is and has been growing at an exponential rate, fuelled by an exponential consumption of energy and resources. The industrial revolution was triggered by the exploitation of fossil fuels, initially with coal and to keep pace with the growth of society this was expanded to include oil and natural gas. Due to the concept of peak finite resource production [1], fossil fuel production will struggle to keep pace with the growth of society. With the realization that the production of oil would not be able to supply our future society needs, there is a constant search for alternative sustainable source of energy.

This shortfall in energy production, combined with the concept of energy independence, has resulted in a revival of the deployment of large scale renewable energy generating capacity in the National Grid, spurred on with heavy government subsidies. The penetration of electrical energy from wind power and Photovoltaics (PVs) into the worldwide electricity transmission networks is currently increasing exponentially. The goal of European Commission (EU) is to reach 20% of energy generated from renewable sources by 2020. There is a similar plan of 25% by 2025 in USA [2].

The risk of environmental degradation from gaseous pollutants from the use of fossil fuels [3] is another and potentially more important factor for an increased interest in both renewable energy and a higher efficiency in the energy network.

Solar PVs and wind turbines generate varying quantities of power depending on weather conditions and the periods of peak generation do not align themselves with that of peak consumption. Therefore alternative power generation sources or energy storage systems are required. They have to have a rapid response to changing load profiles. Traditional solutions to compensate for varying demand are gas powered stations and pumped hydro, but smaller scale localized storage is able to provide greater grid stability, increased energy efficiency and reduced cost [4].

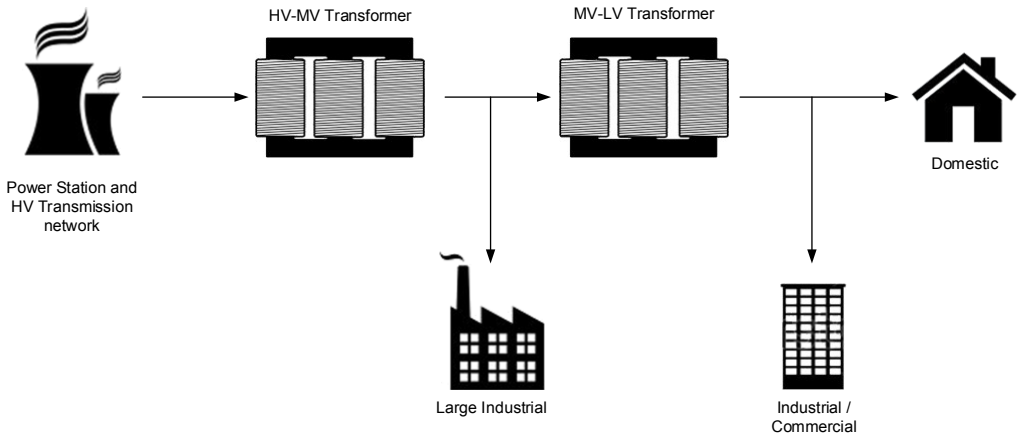


Figure 1.1: Traditional power network topology

Rising energy prices are a financial motivation for improving the efficiency of the whole power system: supply, transmission and distribution. A number of applications traditionally fuelled by oil or gas are now transitioning to electricity as a power source due to the increased efficiency it offers. These applications include heating buildings using water, ground or air source heat pumps, cooking using induction hobs and transportation using electric and hybrid electric vehicles.

This increased energy demand is predicted to result in an increased strain on the existing electrical infrastructure and significant investment will be needed to ensure network stability. This investment can be in the form of energy storage devices placed near the point of either generation and consumption (or both); maximizing the installed power in the transmission cables, reducing losses and increasing capacity. The traditional grid structure is shown in Figure 1.1.

The concept of a Smart Grid, where real time information and communications technology is used to control and monitor the electricity transmission network,

can have a wide variety of applications and implementations. The Smart Grid can result in an electricity transmission network that has improved stability and increased reliability and can facilitate demand to more closely match supply, thereby reducing the need for redundant generation capacity.

A key factor in the matching of supply and demand is that of Demand Side Management (DSM) where the pricing of electricity is dynamically adjusted so the consumer has a financial incentive to use energy at a particular time of day. This will also lead to the introduction of a market for energy storage so as to stabilize the electricity price [5].

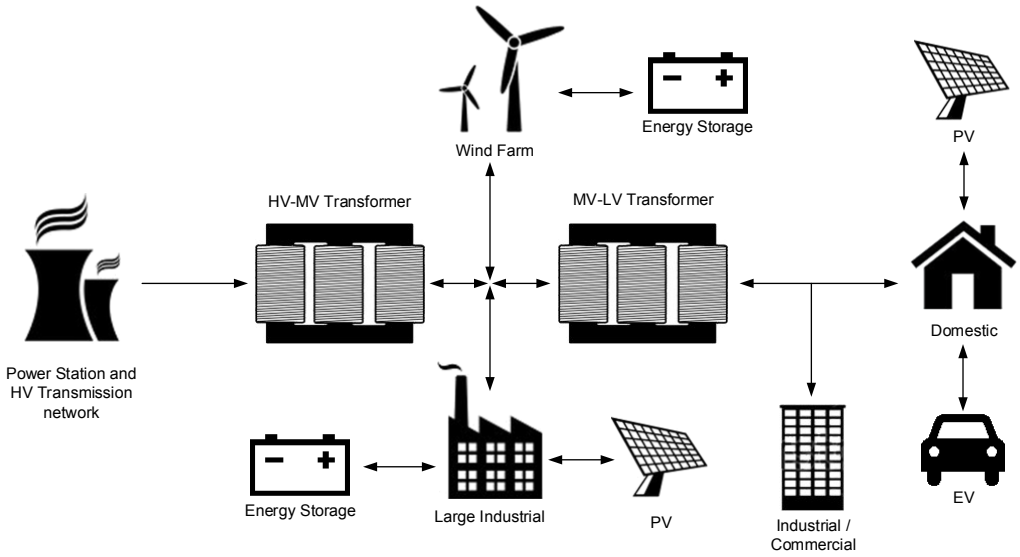


Figure 1.2: Future power network topology

Another way of matching supply and demand is the use of intelligent energy storage. Intelligent in this case means devices' power usage or production is centrally controlled. A financial incentive to provide this service will lead to small scale deployments both at point of use and generation, as shown in Figure 1.2. This will result in reduced load variations in the grid, maximum utilization of the installed power in the transmission network and reducing losses.

A potential European super grid [6] will increase the energy transferred between countries on a much larger scale so that peaks in electrical supply or demand can be averaged over a wider area. However this does not negate the use of smaller localized energy storage and in fact distributed energy storage will play a key role in stabilizing a network of this scale.

All of these factors, combined with the advancement of enabling technology such as Medium Voltage Insulated Gate Bipolar Transistors (IGBTs), are resulting in considerable academic and commercial interest in Medium and High Voltage power converters for the integration of energy storage devices into the Medium Voltage grid.

Additional features that would help to improve the efficiency and stability of the AC transmission network would be a compensation for reactive power and harmonic elimination from non-linear loads and these are features that should be incorporated into the development of advanced power converters for this application [7].

1.1 Existing Solutions to Interface an Energy Storage Device to the MV Grid

In order to meet the requirements for the changing topology of the electrical transmission network, research is required into both energy storage devices and techniques to interface the energy storage devices into the grid. This Ph.D. will focus on the interface between the energy storage device and the Medium Voltage (MV) grid. In this thesis Low Voltage is defined as below 1kV AC or 1.5kV DC, Medium Voltage is defined as between 1kV to 35kV AC or 1.5kV to 50kV DC and High Voltage is above 35kV AC or 50kV DC.

Energy storage systems, using batteries or super-capacitors as storage devices, have to minimize the size and cost of the electrical system in order to increase the cost effectiveness of the additional infrastructure, and increase competitiveness between alternative solutions, such as gas turbines, pumped hydro and flywheel energy storage systems [8].

Traditionally, energy storage devices can be integrated into the electrical transmission network using Low Voltage (LV) converters and step up Low Frequency (LF) transformers. This technique has many benefits; low voltage switching devices can be used, resulting in a high switching frequency and therefore high quality current waveforms. The step up transformers also have high reliabil-

ity and low losses. However this converter topology has one key disadvantage. The LF transformer is an extremely large, heavy and expensive item and this makes this converter topology financially unsuitable for many applications. At high power levels the required conductor cross section can make this converter topology financially unsuitable.

A second approach is to use high power MV switching devices, such as Integrated Gate Commutated Thyristors (IGCTs) or Thyristors to switch directly at the Medium Voltage. These converters will have very low conduction losses in the switching devices and this can result in an extremely efficient converters. However IGCTs are not able to switch at high frequencies due to the high switching losses from these switching devices. As such the filters required make this converter large and expensive. These converters will also have a relatively slow transient response due to the stored energy in the AC filters. The topology is generally reserved for MW scale power converters e.g. High Voltage Direct Current (HVDC) [9] [10].

Multilevel converters offer a novel approach. By series connecting lower voltage devices, a Medium Voltage converter is able to switch directly at the Medium Voltage, avoiding the LF transformer. The high quality waveforms require significantly less filtering than for the case when MV switching devices are used. However the majority of topologies available commercially, require a large number of electrolytic capacitors to provide the voltage steps; these electrolytic capacitors are large, expensive and prone to failure [11] [12].

To provide isolation between the DC and AC network with a multilevel converter a High Frequency (HF) transformer can be used. Isolation between the networks will result in a significant cost reduction for the infrastructure required to meet the requirements for grounding and safety of the energy storage device.

A Cycloconverter topology when used for a multilevel converter can reduce the number of electrolytic capacitors required, thereby reducing the size, cost and increasing the reliability. However the HF transformer, used to provide the isolation between the networks, has to process a greater maximum power compared with the transformer in a voltage source multilevel topology, resulting in a larger size. This is due to the fact that the peak voltage and current are $sqrt2$ greater than the Root Mean Square (RMS), resulting in twice the peak power. The volt-

age source multilevel topologies contain electrolytic capacitors that store energy and supplement the power from the transformer, allowing the transformer to be sized for the average, rather than the peak.

A Hybrid Multilevel Converter is the name given to a converter constructed from a series of varied modular converter topologies and results in a converter with the combined advantages of the modular component topologies. This can result in a converter with reduced losses, higher power rating, increased waveform quality or to address a specific issues with a single converter topology. For the Cycloconverter Topology, it is desirable to increase the power rating whilst maintaining the same HF transformer. This can be done by using an additional auxiliary 3-Phase Voltage Source Inverter (VSI), forming a Hybrid Cycloconverter Topology. The Hybrid Cycloconverter Topology increases the voltage, and therefore power rating with the same switching devices and transformer.

This research will focus on the design, simulation, construction and testing of this novel hybrid converter topology and will compare its performance in simulation to existing converter topologies.

1.2 Objectives of the Research Project

This Ph.D. research project is aimed at looking at advanced power converters to interface an energy storage device, such as a super-capacitor or battery, on to the Medium Voltage grid.

The objectives of this thesis are:

- To evaluate the current research into medium voltage multilevel converters in order to justify the research and development of a novel converter topology.
- To develop a novel hybrid converter topology based on the Cycloconverter.
- To evaluate the performance of this hybrid converter topology in simulation against existing topologies in terms of switching and conduction device losses.

- To experimentally validate the operation of the hybrid converter and evaluate its performance.

The demonstration converter constructed for this thesis is used purely to demonstrate the effectiveness of this converter topology and will not be connected to an energy storage device or medium voltage grid. For testing, the maximum voltage of any component on the demonstrator will be limited to 1000V with the power rating of this converter limited to 15kW. Variable AC and DC supplies will instead be used for the AC and DC networks. The demonstration must provide electrical isolation between the AC and DC network using a HF transformer. The conversion efficiency must be greater than 85% when operating at or above 10% of the rated power. The converter must meet the requirements with regard to harmonic currents in BS EN 61000-3-3 for a Class A appliance [13] as shown in Table 1.1 and 1.2. The topology of the demonstration converter must allow for the construction of a Medium Voltage converter using a series of Low Voltage converter modules. The demonstration converter will however operate at Low Voltage and will therefore be constructed from only one Low Voltage main converter module per phase. To achieve this each main converter module must provide isolation between the DC and AC terminals.

Harmonic order	3	5	7	9	11	13	15	17	19
Current (A)	2.3	1.4	0.77	0.40	0.33	0.21	0.08	0.07	0.06

Table 1.1: BS EN 61000-3-3 limits for odd harmonic current emissions

Harmonic order	2	4	6	8	10	12	14	16	18
Current (A)	1.08	0.43	0.30	0.23	0.18	0.15	0.13	0.12	0.10

Table 1.2: BS EN 61000-3-3 limits for even harmonic current emissions

1.3 Thesis Structure and Content

Chapter 2 introduces the state of the art for Medium Voltage grid connected converters. The theory of multilevel converters is introduced with the advantages given. The main existing topologies are discussed along with the advantages and disadvantages of each topology. Focus is given to the Cycloconverter topologies

and topologies formed in a Hybrid manner from dissimilars. Potential solutions meeting the converter requirements are investigated followed by the justification for the selection of a novel Hybrid Cycloconverter Topology. The Triple VSI Topology is selected as a benchmark to provide a comparison between the Cycloconverter and the Hybrid Cycloconverter based topologies. This comparison will be undertaken in Chapter 3 and 4.

Chapter 3 analyses in detail the three converter topologies: the benchmark Triple VSI, the Cycloconverter and novel Hybrid Cycloconverter Topologies. The operation of the converters, the control schemes and the modulation techniques are described followed by an investigation into the distribution of the reference voltage in the Hybrid Cycloconverter between the auxiliary 3-Phase VSI and Cycloconverter (Main Converter) blocks. This 8voltage reference distribution is required in order to reduce the peak power in the Main Converter whilst minimizing the installed power in the auxiliary converter.

Simulation studies are carried out in Chapter 4 to investigate the switching and conduction losses in the Hybrid Cycloconverter Topology with a comparison against the losses in the Cycloconverter and the benchmark Triple VSI Topology. These simulations are used to validate the development and research into the novel Hybrid Cycloconverter Topology by demonstrating the improvement it offers in terms of efficiency and power rating over the traditional Cycloconverter Topology, thus increasing the competitiveness of a Cycloconverter type solution against the benchmark Triple VSI Topology (Figures 8.2, 8.14 and 8.17).

Chapter 5 documents the design and construction of a 15kW LV demonstration experimental converter. This experimental converter can be configured as the Cycloconverter and the Hybrid Cycloconverter and will be used to demonstrate the effectiveness of the Hybrid Cycloconverter Topology and the improvement it offers against the Cycloconverter module (Main Converter) when used alone. It also covers the sensing of the analogue voltages and currents used to control the converter, the implementation of the modulation schemes in the Field-Programmable Gate Array (FPGA) and the protection circuitry to protect the converter in the case of a fault.

Chapter 6 documents the design and construction of the high frequency trans-

formers required for the experimental converter. The selection of the core materials and copper profile is justified and an explanation behind the winding arrangement is given. A simulation is then carried out into core losses, magnetizing current and peak flux in the transformer for a number of modulation techniques for both the Cycloconverter and Hybrid Cycloconverter Topologies. This simulation is carried out to validate the selection of the modulation technique used in the experimental converter as opposed to providing an accurate breakdown of the experimental losses that are presented in Chapter 8.

Chapter 7 documents the design and testing of the control schemes required for the experimental converter. This chapter covers the techniques used to control the AC currents, maintain the DC link capacitor voltage of the auxiliary 3-Phase VSI and distribute the converter reference voltage between the converter blocks. This chapter builds on the work carried out in Chapter 3 by elaborating the control structures in more detail and documenting the control scheme implemented in the experimental converter.

Chapter 8 presents the results obtained in the laboratory from the testing of the experimental converter configured as both the Cycloconverter and the Hybrid Cycloconverter Topologies. The efficiency of the two converters is recorded when providing power to a resistive load acting as the AC network, and the transfer of power from the AC network to the DC network and vice versa. Key current and voltage waveforms are presented for each test, along with their respective Fourier Transforms. An analysis of the harmonic content and the impact that the harmonics have on the operation of the converter is described.

Chapter 9 concludes the thesis, summarizing the work carried out, the knowledge gained, the original features, the potential improvements and further research that could continue the progression of this converter topology. This is followed by several appendices containing information on the derivation of controllers, the models used in simulation, the schematic diagrams of the demonstrator converter and tables of the experimental results.

Chapter 2

Overview of Medium Voltage Converter Technology

This chapter will introduce the main topologies used for medium voltage power converters documented in the literature. The history of each topology will be given, focusing on the key progressions and developments along with any issues that have been encountered, explicitly or not. A more in-depth analysis of the operation of the novel Hybrid Cycloconverter Topology will be given, along with the Cycloconverter and Triple VSI topologies, in Chapter 3.

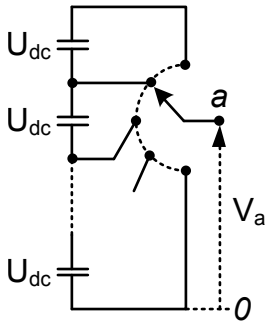


Figure 2.1: Fundamental idea behind a Multilevel inverter

The areas of research in the development of Multilevel Converters up until 2002 was summarized by Jose Rodriguez [14]. This paper includes the majority of the topologies, modulation schemes, control methods and applications of Multilevel Converters being researched and in use today. Multilevel Converters are able to

switch high voltages with LV switching devices, significantly reducing switching losses and producing a waveform with discrete voltage steps. This waveform will have a significantly reduced harmonic content, requiring less filtering to achieve a given Total Harmonic Distortion (THD). Figure 2.1 shows the fundamental idea behind a Multilevel Converter: the output voltage at point a can be connected to a series of voltage sources U_{dc}, in this case capacitors, in order to create an output waveform, V_a, with discrete voltage steps equal to U_{dc}. It is also possible to construct a current source Multilevel Converter using multiple Medium Frequency (MF) transformers to create the isolated sources. This arrangement has larger transformers but no longer relies on electrolytic capacitors in the intermediary link.

In general the issue with Multilevel Converters is that the capacitors required to create these voltage sources have high ripple currents and are therefore large, expensive and prone to failure [12].

This chapter will describe the operation of the Diode-Clamped and Flying capacitor inverters (Section 2.1) before investigating converters based on a Multicell approach (Section 2.2). The Cycloconverter will then be introduced (Section 2.3) with an analysis of 3 common variations and two modulation techniques. The concept of a Hybrid Multilevel Converter will be explained with advantages and disadvantages of this arrangement given. A number of papers documenting experimental or simulation studies based on a number of different hybrid circuit configurations will be described. A summary of the key findings will conclude this chapter.

Converters discussed in this chapter will normally require isolation between the DC and AC network, however this depends on the application. The number of isolated sources required will depend on the number of levels in the converter and the topology selected, for example traditional Multicell Multilevel Converters need an isolated power supply for each cell. However the Flying Capacitor converter relies on capacitors to provide the required Voltage levels and therefore only requires one isolated supply.

It is possible to construct a converter without isolation between the AC grid network and the DC energy storage network, such as a battery or super-capacitor

array. However without isolation, the installation would require a significant investment in infrastructure for safety and grounding would be required for the energy storage network in order to ensure safe operation of the converter. Maintenance of the battery array would be particularly difficult as the whole converter would have to be powered down before any maintenance could occur. The DC voltage sources will have significant coupling to earth resulting in an earth leakage current. Earth leakage will cause additional power losses as well as increased safety and grounding issues [15] [16] as any ungrounded metalwork could be charged up to a hazardous voltage.

One of the requirements set for this project was isolation between the AC and DC network to allow for the converter topology to be used as a Low Voltage module in a Medium Voltage converter and as such an additional isolated DC-DC converter will be required for every topology that does not have an inherent isolation capability (e.g. the Cycloconverter). A low frequency transformer could be used instead but this project is also focused on reducing the size and weight of the transformer, and as such a DC/DC converter with isolation provided by a Medium Frequency (MF) Transformer should be used. Chapter 3 will investigate in detail one isolated DC/DC converter suitable for this application, the Dual Active Bridge (DAB) converter.

2.1 Series Connected Multilevel Converters

2.1.1 The Diode-Clamped Inverter

The first paper documenting a Diode-Clamped Multilevel Inverter was published in 1981 [17], followed by further research [14], [18], [19], and [20]. This converter was called the Neutral Point Clamp (NPC) Inverter and was able to construct a 3-level Pulse Width Modulation (PWM) AC waveform. The schematic of this inverter is shown in Figure 2.2. This inverter used clamping diodes to connect the AC voltage to a number of different series connected capacitors. The inverter does not inherently have isolation between the DC and AC network so an additional isolated DAB converter would be required.

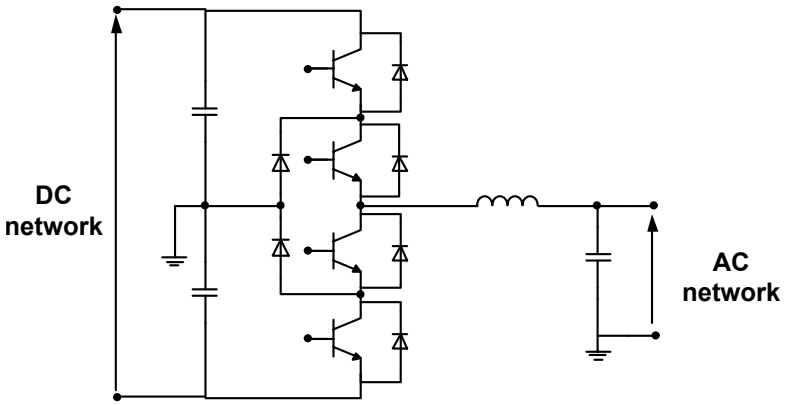


Figure 2.2: Diode Clamped Multilevel inverter

The original converter was called the NPC inverter but as converters with a greater number of levels were researched, a more generalized name, the Diode-Clamped Multilevel Inverter was used for this type of topology with any number of levels.

The 3 level Diode-Clamped Multilevel Inverter is a commonly used topology for high power industrial motor drives to produce a voltage waveform with a reduced switching harmonic content, allowing for a lower switching frequency converter or lower machine losses [21] from the reduced HF harmonic currents, resuling in lower eddy currents in the windings of the machine.

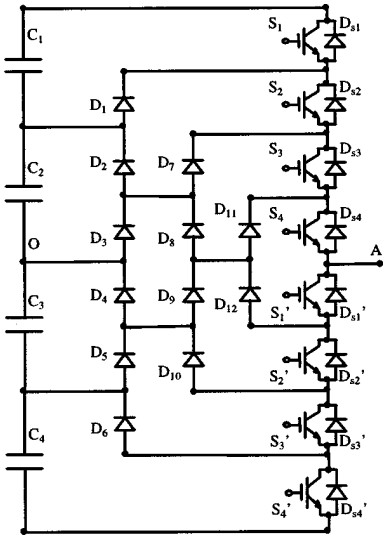


Figure 2.3: 5 level Diode-Clamped Multilevel inverter [22]

A modification to the Diode-Clamped inverter [22], shown in Figure 2.3 reduces the conduction path for a converter with more than 3 levels by arranging the clamping diodes (D1-D12) in a pyramid arrangement. However this converter topology is still not able to address the main issue with the Diode Clamped Multilevel inverter: the number of clamping diodes has a quadratic relationship to the number of levels in the converter and as such a converter with a large number of levels is impractical to implement at a high power level [14].

2.1.2 The Flying-Capacitor Inverter

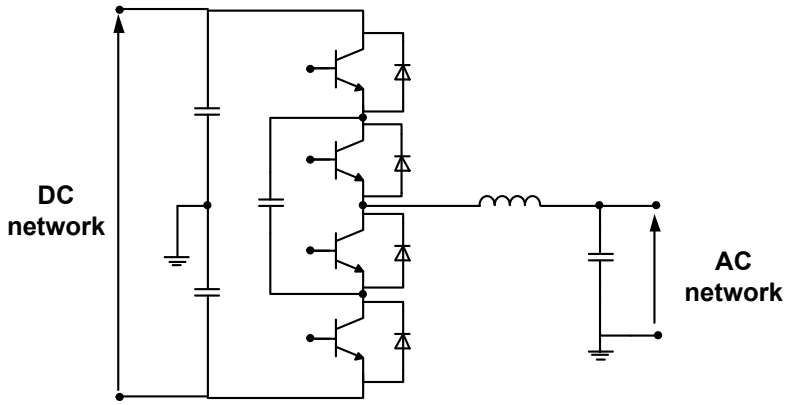


Figure 2.4: Flying Capacitor Multilevel inverter

The Flying-Capacitor inverter is introduced [23] and is named "the Versatile Multilevel Cell" [14] [24] and [25]. The switches are used to connect positive or negative capacitor voltages to the output so as to synthesize the desired Multilevel waveform.

This topology is able to utilize much smaller capacitors because all the Flying Capacitors in this converter can be modulated at high frequency. This allows them to be sized for the switching frequency voltage ripple and not the grid frequency voltage ripple. This is found to have a number of advantages [23] as well as being able to operate without isolated power supplies for the gate drives. This utilizes a bootstrap technique [26].

This topology shares a similar disadvantage to the Diode-Clamped Multilevel Inverter in that the number of Flying Capacitors has a quadratic relationship

to the number of levels of the converter. Therefore the topology is not suitable for a converter with a large number of output levels [14]. The converter will also require a control scheme to ensure that the Flying Capacitors maintain the correct voltage [25]. As isolated voltage sensors are expensive to implement accurately, this adds a significant cost and complexity to the converter.

2.2 Cascaded Multicell Converters

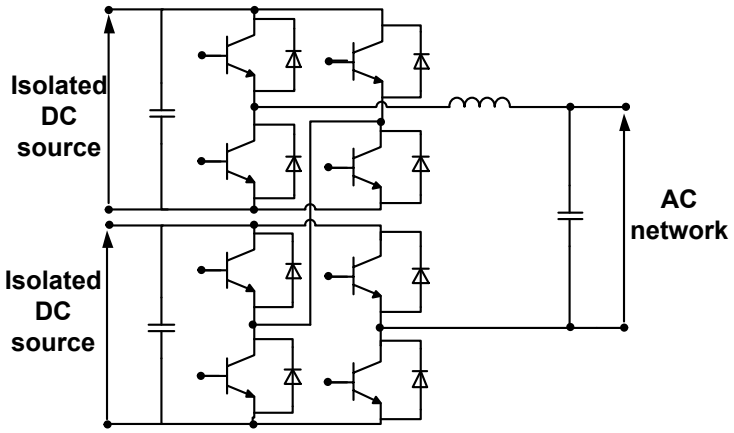


Figure 2.5: Cascaded H-Bridge multicell inverter

The Cascaded H-Bridge Multicell inverter, shown in Figure 2.5, constructs a Multilevel inverter from a number of voltage sources connected to H-Bridge cells [14] [27] [28]. Each H-Bridge can connect positive or negative capacitor voltages to the output so as to synthesize the desired Multilevel waveform. Each voltage source can be an isolated DC/DC supply or alternatively floating capacitors can be used with a control strategy designed to maintain the capacitor voltages.

An illustrative application of this converter is the Cascaded Multicell motor drive [27]. This implements a 3-Phase, 2MVA, 3.3kV, 7-level voltage source inverter using 1.7kV IGBTs. The inverter uses modules constructed from a back to back 3-Phase PWM converter as an active rectifier and a single phase inverter connected by a common DC link capacitor. For each phase of the AC motor, three of these modules are connected in series, resulting a total of 9 modules for a 3-Phase converter. The paper justifies the use of this topology against that of the

Diode Clamped or Flying Capacitor converters by saying that "it is difficult to implement more than a four level inverter because of inherent capacitor voltage balance problems and the requirement of increased voltage rating of the clamping diodes". A similar conclusion is reached by M. Hiller et al. [28]. This converter utilizes a grid frequency transformer to provide isolation. Due to the requirements for this project set out in Chapter 1 a high frequency transformer and associated converter, such as the DAB converter, would be required to provide isolation instead.

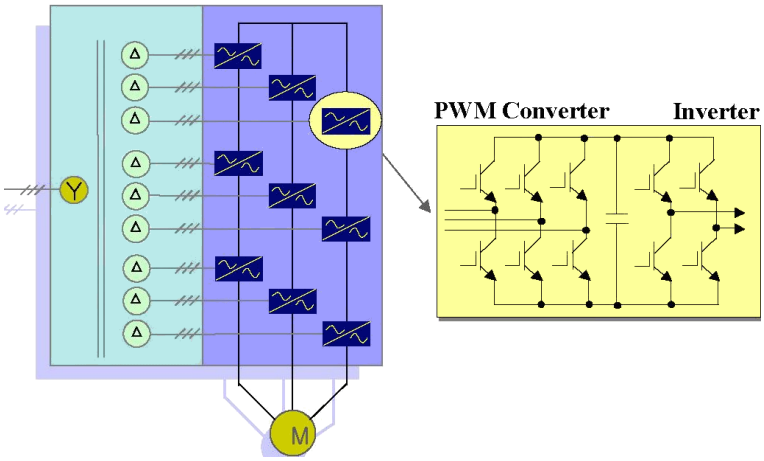


Figure 2.6: 2MVA, 3.3kV 7-level inverter drive [27]

2.2.1 Modular Multi-Level Converter

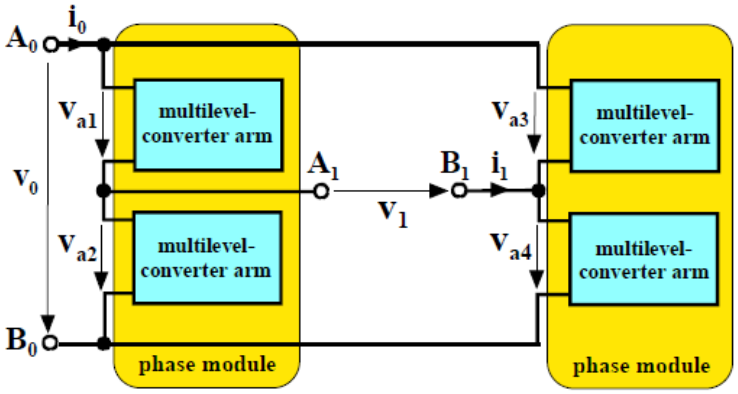


Figure 2.7: M^{2}LC topology, from [29]

Recent developments in the commercialization of Multilevel Converters has been introduced by Siemens AG and the Universität der Bundeswehr, München, with

the Modular MultiLevel Converter (M^2LC). Figure 2.7 shows the general M^2LC converter structure; a series of Multilevel Converter arms are connected in such a way to form a medium voltage H-Bridge. V_0 is the primary converter voltage, with i_0 the primary current. V_1 is the secondary converter voltage, with i_1 the secondary current. The M^2LC can be used for either AC-AC converters, for use as a variable speed drive for large motors connected to an AC grid or as a DC-AC inverter for connection between HVDC lines or energy storage components and the AC grid.

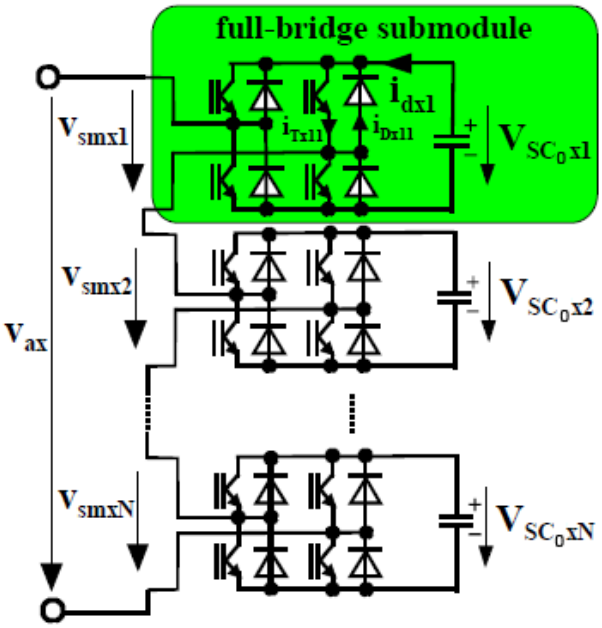


Figure 2.8: M^2LC Modular Multi-Level Converter arm composed of full-bridge sub-modules for AC-AC or DC-AC conversion [29]

A series of papers [28], [30] and [31] describe the development of the converter and results for a 2MW prototype are documented in [29].The final converter was constructed as a 3-Phase, 8 bridges per phase AC-AC Multilevel Converter with a 17 level output waveform and a 2MW power rating. It was designed as a variable speed drive for rail traction applications, converting the 15kW/16.7Hz from the overhead lines to the variable frequency, variable voltage required to drive the motor.

In [28], the authors discuss the disadvantages of the Diode-Clamped Multilevel Inverter, justifying the development of the M^2LC topology. "An extension of the number of levels in the output voltage (more than three) is possible, but leads

to a significant increase in the number of clamping diodes required, so that the mechanical design of low inductive commutation paths becomes complex, difficult and expensive." Therefore the Diode Clamped or Flying Capacitor topologies are not suitable for Medium Voltage converters with a large number of output levels and this was the motivation behind the development of this new topology for this application.

The building block of the M^{2}LC converter is that of sub-modules constructed from a floating capacitor connected to an H-Bridge (Figure 2.8). The voltage across the output of the H-Bridge therefore can be +V_{DC}, -V_{DC} or 0V, depending on how the H-Bridge is switched. Many of these sub-modules are connected in series to form a higher voltage Multilevel Converter arm. Four of these Multilevel Converter arms are connected in such a way to form a single phase H-Bridge, as shown in Figure 2.7. The peak voltage rating of the M^{2}LC converter is the sum of the capacitor voltage in one of the Multilevel Converter arms.

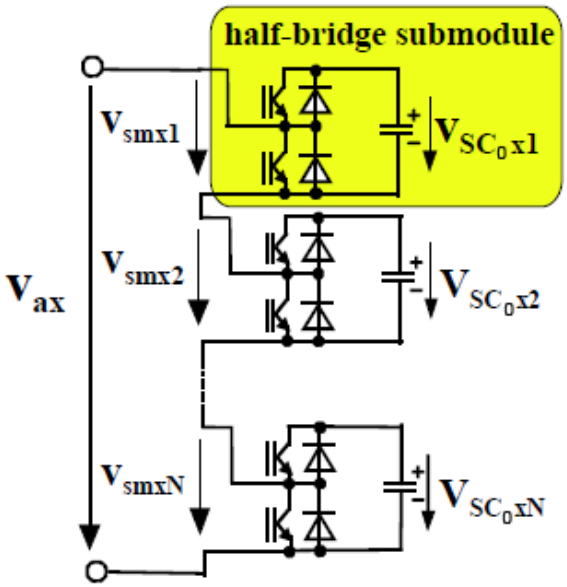


Figure 2.9: M^{2}LC Modular Multi-Level Converter arm composed of half-bridge sub-modules for DC-AC conversion, from [29]

When operating as an AC/AC converter, the M^{2}LC is configured as full-bridge sub-modules, (Figure 2.9), whereas for a DC/AC inverter the M^{2}LC can be configured with full-bridge or half-bridge sub-modules (Figure 2.8), with the full-bridge modules offering redundancy but requiring twice the silicone for the same power rating. The converter is designed in such a way that it can be easily reconfigured

within a few hours allowing for a modular approach that can facilitate repairs or reconfigurations easily [29]. The M^2LC converter utilizes a floating capacitor instead of an isolated DC power supply [28], requiring an accurate monitoring of the capacitor voltage and an adaptive modulation technique to ensure that it remains within set limits. This results in a converter with a complex control system requiring a large number of voltage sensors.

2.2.2 Modular Cascaded H-Bridge Converter

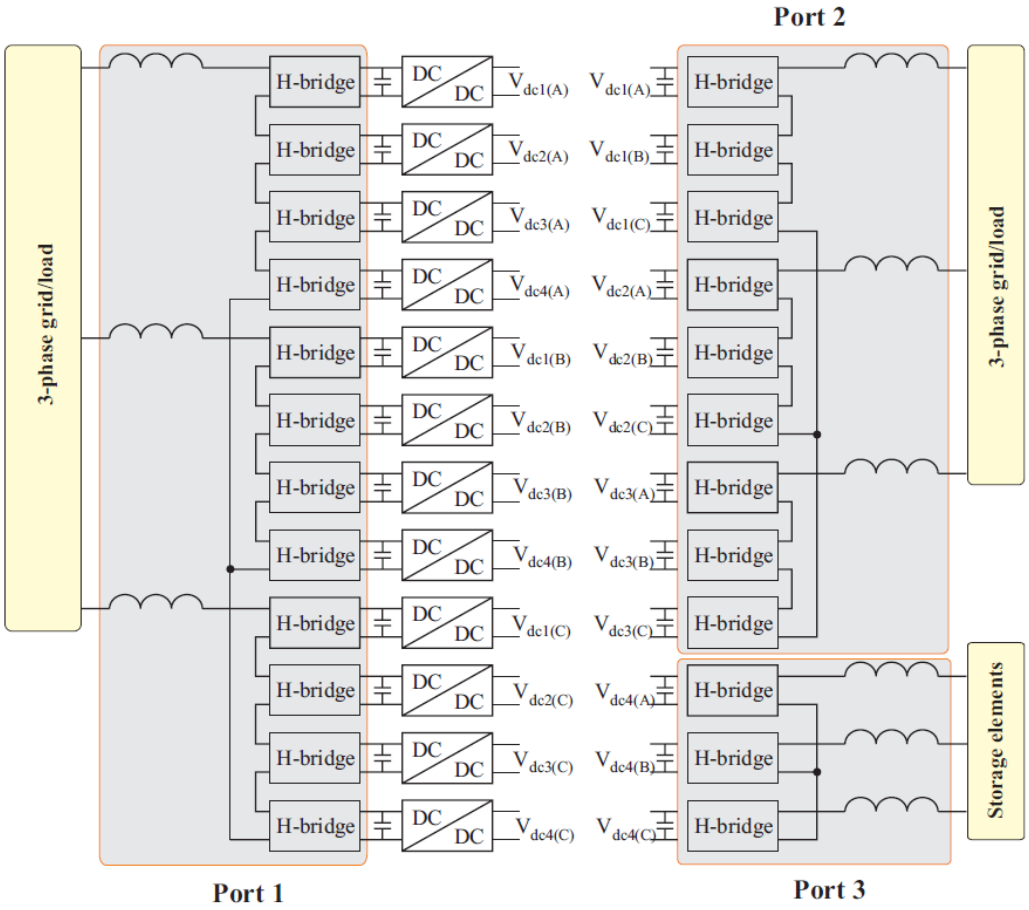


Figure 2.10: UNIFLEX H-Bridge topology

The UNIFLEX-PM Multilevel Converter topology, [32], [33], [34], [35], was designed in collaboration with ABB, Dynex Semiconductor, Areva, the University of Nottingham, Aalborg University and others. A 3-port, 415V/3.3kV, 500kVA prototype was constructed at the University of Nottingham in 2008.

The structure of the UNIFLEX-PM modular cascaded H-Bridge converter consists of identical reconfigurable Low Voltage (below 1kV) H-Bridge and DAB DC/DC modules allowing for the connection of multiple asynchronous AC or DC grids. The H-Bridges provide the grid interface and the DC/DC converters provide isolation, allowing for the series connection of modules in order to interface with a higher voltage grid.

The experimental UNIFLEX-PM converter was constructed from 12 isolated modules, each consisting of an input H-Bridge, DAB DC/DC converter and output H-Bridge. The converter was configured as a 3 port AC converter with two 3.3kV ports and one 415V port. All the ports are able to connect to asynchronous grids with the two 3.3kV ports designed for isolated grids or renewable energy sources and the third port is designed for an energy storage device or LV grid.

2.3 Multilevel Cycloconverter Topologies

Converters based on series connected Multilevel inverters require a number of devices proportional to the square of the number of levels. Therefore series connected Multilevel inverters are unsuitable as Medium Voltage Multilevel Converters with more than 5 levels. Cascaded Multilevel Converters do not suffer from this problem, however they require that there is isolation between each cell instead of only between the AC and DC network. The UNIFLEX-PM converter achieves isolation by utilizing a DAB DC/DC converter and the M^2LC converters achieve isolation by utilizing floating capacitors as isolated voltage sources; the modulation strategy ensures the capacitors are kept at the correct voltage.

These two solutions require very large electrolytic capacitors to store energy, either in the intermediary DC link for UNIFLEX-PM style converters, or as the floating capacitors in M^2LC style converters. Electrolytic capacitors are large, expensive and prone to failure [36] and therefore an alternative topology, with a reduced number of electrolytic capacitors will provide an attractive alternative. This topology is based on a VSI, high frequency transformer and Cycloconverter. It forms the basis of the Ph.D. investigation.

A technique for creating a DC-AC converter using a VSI, HF transformer and Cycloconverter has been reported [37] [38] [39] [40] [41] [42] [43] [44] [45] [46]. This converter topology provides both isolation and inversion and therefore does not require an additional isolated DC-DC converter.

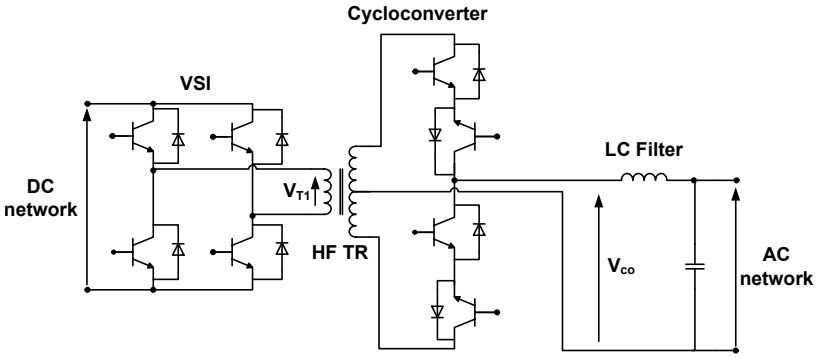


Figure 2.11: Single leg Cycloconverter Topology

The concept is a logical progression from the standard PWM VSI inverter connected to a LF transformer. Figure 2.11 shows the simplest version of the Cycloconverter Topology and will be used for the initial explanation. One technique for modulating the converter is to generate a 50Hz PWM sine wave modulated by a square wave at the switching frequency on V_{T1}, resulting in every other PWM pulse being inverted. This Voltage waveform is passed through the HF Transformer for isolation before being demodulated by the Cycloconverter by rectifying the pulses in the appropriate direction to synthesize the required 50Hz waveform, V_{C0}. The theory of the operation of this technique is very similar to that of Amplitude Modulation used for radio communication [47].

An alternative technique for modulating this converter is to generate a square wave with a 50% duty cycle with the VSI and then to construct the AC PWM voltage waveform by switching the Cycloconverter in order to vary the non-inverted to inverted duty cycle for each square wave VSI pulse. However this approach has the disadvantage of higher transformer core losses and is harder to achieve Zero Voltage Switching (ZVS) with the Cycloconverter.

This topology has the advantage of not containing any additional electrolytic capacitors apart from in the DC link. However the utilization of the installed power in the transformer and the switching devices is not as efficient as with the DC/DC DAB converter, due to the lack of energy storage device in the

intermediary link resulting in the whole converter processing the peak power, rather than the average. Care needs to be taken when implementing the switching strategy due to the connection of two current sources: the leakage inductance in the transformer and the output inductor both act as current sources and a current mismatch when connecting these two inductors will result in very large voltage spikes. Clamp circuits or snubbers across the switching devices need to be used to protect the devices from destruction from these voltage spikes.

Three circuit arrangements are possible as shown in Figures 2.11, 2.12 and 2.13. Figure 2.11 shows the simplest possible Cycloconverter configuration which uses only 2 bi-directional switches. However this requires a transformer with two windings on the secondary with the same RMS current, resulting in a transformer with a greater size and cost due to the $\sqrt{2}$ greater RMS current in the windings.

A single leg converter is discussed [37] where the authors use a centre tapped transformer secondary, with a bi-directional switch connected to both the upper and lower taps, as in Figure 2.11. The primary VSI however is constructed in a similar fashion with a centre tapped primary winding and a uni-directional switch attached to both the upper and lower tap. This results in a transformer with twice the required copper volume but only 6 transistors are used, resulting in a much simplified control scheme. For low power applications (i.e. Uninterruptible Power Supply (UPS)) and in 1988 when analogue control schemes were preferable, this would have greatly reduced the cost and complexity of the converter. However for modern high power converters, the reduction of the transformer size is a key factor in reducing the cost of the converter.

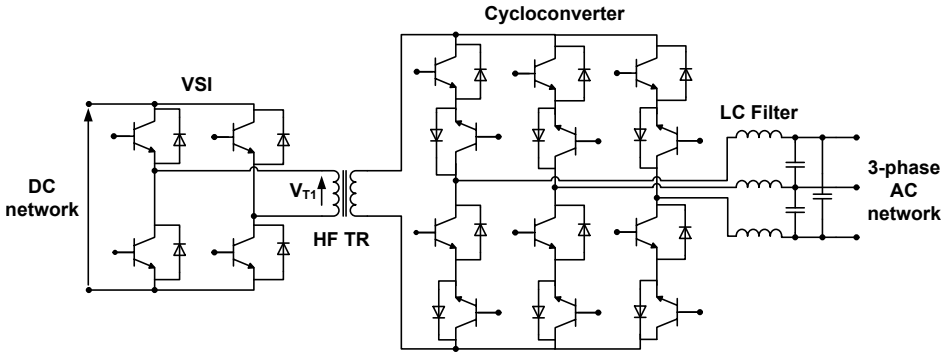


Figure 2.12: Three leg, 3-Phase Cycloconverter Topology

A 3-Phase Cycloconverter is shown in Figure 2.12 [38]. A VSI is used to generate

a square wave with 50% duty cycle on the primary winding of the transformer. A 3 phase Cycloconverter is then used to construct the required 50Hz waveform from the square wave pulses on the secondary of the transformer. One can achieve Zero Current Switching (ZCS) in the VSI but to achieve this one has to assume that the Cycloconverter stage is hard switched [38].

Reference [39] improves on the 3-Phase converter by implementing a regenerative clamp to recover the energy from the leakage inductance in the transformer during switching. A technique for zero voltage switching in the Cycloconverter stage is also presented. In order to reduce voltage overshoots in the Cycloconverter during switching the concept of current build up in the transformer leakage inductance to the value of the AC network current is introduced. However no mention is given to converter operation in 4 quadrants and it is likely that this converter is only able to operate with reduced switching losses in 2 out of 4 quadrants. It is not trivial to achieve soft switching with the Cycloconverter in all modes of operation.

In [40], the author introduces the concept of a natural commutated 3-Phase Cycloconverter based on phase angle control, allowing for the removal of the clamp circuit. Energy contained in the leakage inductance is fed back to the DC voltage source via a method described as "commutation overlap". A reverse voltage is applied by the VSI before commutating the Cycloconverter. Four switches in the Cycloconverter are switched on, short-circuiting the transformer and resulting in the full VSI reverse voltage appearing across the leakage inductance. This Voltage causes the current in the transformer to reduce and turn negative. When the current in the transformer is equal to the AC grid current the diodes will naturally perform commutation. This commutation technique only works when the current and voltage have the same polarity and as such also only works in 2 out of the 4 quadrants.

In [41], operation of a 3-Phase three leg Cycloconverter (Figure 2.12) is presented at 20kVA power rating. In order to reduce the conduction losses in the Cycloconverter output stage, Thyristors are used instead of IGBTs. As Thyristors do not have a turn off capability and require special measures to prevent accidental turn on, this paper concentrates on modulation strategies that will ensure that the Cycloconverter will commutate as desired. The prototype converter is constructed, operating at 500Hz and the modulation strategies developed are tested

experimentally. The results showed that both modulation schemes functioned as desired.

The advantage of the three leg Cycloconverter Topology is that the MF transformer provides power for all 3 phases. The power level is therefore constant across a cycle, provided the three phases are operating with balanced sinusoidal loads. This results in a transformer with a reduced size to that of the single phase converter. However in the three leg Cycloconverter Topology, the 3 phases are connected at a neutral point, thus not allowing this converter topology to be used as a module in a Multilevel Converter.

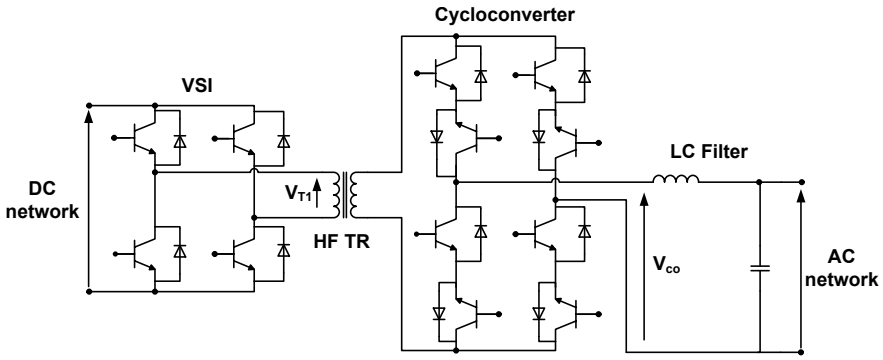


Figure 2.13: Two leg Cycloconverter Topology

A more suitable topology is based on a single phase Cycloconverter Topology, as shown in Figure 2.13 [43] [44] [45] [48]. This converter topology can be utilized to construct a 3-Phase converter by connecting three single phase converters to a common neutral point and a Multilevel Converter can be constructed from multiple single phase modules connected in series. However the installed power in the transformer will be twice as large as the transformer in the DAB converter used in the UNIFLEX-PM project. This is due to the fact that the peak power transferred by the DAB converter is the average AC grid power, whereas for the Cycloconverter the peak power is the same as the peak AC grid power, as there is no form of energy storage in this converter. The copper and iron sections of the transformer therefore have to be sized according to the peak power rather than the average.

A definitive switching strategy [42], is for a Thyristor based two leg single phase Cycloconverter (Figure 2.13) for 16.7Hz railway fed applications. Additional capacitor snubbers are placed across all the switching devices in the Cycloconverter

in order to realize ZVS or ZCS in both the Cycloconverter and the VSI. A detailed description of the commutation process is given. This switching strategy is based on a 50% duty cycle waveform generated by the primary VSI. This is more suited to the 3-Phase Cycloconverter as it significantly increases the difficulty of the commutation as well as increasing the transformer core losses, whilst offering no benefit for a single phase converter. The results from [42] are based only on a simulation study.

A comparative study of different converter topologies for railway traction applications is given in [43], focusing on the two leg Cycloconverter. Initially a series connected H-Bridge topology is presented and a comparative study of losses is performed against a traditional grid frequency transformer, with the total weight of the two converters remaining constant. A two leg Cycloconverter Topology (Figure 2.13), constructed with multiple levels is then introduced. This has the advantage of isolation and soft switching when compared with the series connected H-Bridge topology. The authors utilize capacitor snubbers on the DC network VSI to realize reduced switching losses in the whole converter. A small scale single phase, single module converter is constructed with experimental waveforms (3A, 230V grid voltage). Even at this current, significant voltage overshoots ($\pm$180V) are reported. For Medium Voltage applications a snubber and clamp circuit connected to the Cycloconverter would still be essential and significant losses may be present in this area of the converter.

In [44] the authors construct a 10kVA version of the 2-leg Cycloconverter with experimental waveforms to validate the operation. In [45] a 15kV, 16.7Hz, 1.2MVA 16 module Multilevel Converter is constructed using the same topology. A thorough investigation into losses and the practical implementation of the converter is given. The experimental converter is reported to be 50% lighter, 20% smaller and 3% more efficient than a converter based on a traditional VSI H-Bridge connected to a grid frequency transformer.

Two kinds of Sinusoidal PWM (SPWM) switching strategies for the two leg Cycloconverter are presented [46] to investigate a reduction in output filter size, transformer losses and switching losses with low power experimental converter waveforms. The authors compare the operation of the Cycloconverter when the PWM is generated by the VSI against a 50% duty cycle method (as used in [43]). The authors claim that ZVS is only possible with the PWM generated by the

VSI, however a previous paper [42] shows otherwise. The conclusion is that when the PWM is performed by the VSI and rectified by the cycloconverter, the transformer, filter and switching losses can be significantly reduced [46].

The two leg Cycloconverter appears to be the most suitable Cycloconverter Topology to meet the aims of project as give in Chapter 1. The transformer size is considerably smaller than that in the single leg Cycloconverter and it is able to be used as a module in a series connected Multilevel Converter. However this converter has one main disadvantage that makes it unsuitable as the sole converter. The transformer has to be designed to handle twice the peak power as the transformer in the DAB converter for a given RMS power rating, due to the peak current and the peak Voltage Time Area (VTA) being $\sqrt{2}$ bigger that the RMS current and VTA. The utilization of an additional converter, connected to a floating capacitor, designed to inject reactive power resulting in a reduction of the peak power in the transformer is an attractive proposal. This is an example of a Hybrid Converter.

2.4 Hybrid Converter Topologies

A Hybrid Converter is a converter that is constructed from multiple devices with different current or voltage ratings. This allows the converter to be as efficient as possible, by utilizing high power devices with lower conduction losses, as well as producing a high quality waveform using smaller power devices with lower switching losses. This approach can be applied to any of the Multilevel Converter topologies mentioned previously. The approach can also combine multiple varying converter topologies in order to create a novel Hybrid Converter topology containing the advantages of all the component converters.

The switching losses of semiconductor devices increase non-linearly with blocking voltage. A MV converter constructed from MV switching devices will switch at a very low frequency in order for the switching losses to remain at an acceptable level. This converter will require very large AC filters to reduce the current harmonics to the specified level. Multilevel converters constructed from series connected LV switching devices can operate at a very high switching frequency

with very low switching losses, with the switching frequency and conduction losses increasing linearly with the number of levels. The conduction losses for a multilevel converter constructed from LV switching devices are much greater than a converter constructed from MV devices. By combining both MV and LV devices in one converter, one is able to have the advantages of both devices. The MV devices provide the majority of the voltage and therefore output power, resulting in low conduction losses. The LV devices switch at a high frequency to generate a high quality waveform requiring small output filters.

The issue with Hybrid Converters is that they are inherently not as modular as other Multilevel Converters. The M^2LC converter can be constructed from hundreds of identical modules, allowing for redundancy, reconfigurability and the economy of scale. Hybrid Converters will usually only have one or two Medium Voltage modules for each phase, resulting in higher manufacturing costs and reduced robustness. If one module fails, a converter phase is lost.

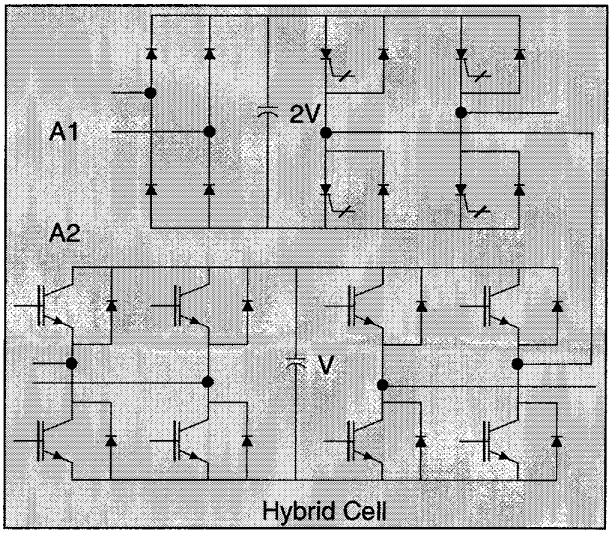


Figure 2.14: One Leg of a Hybrid Multilevel Converter [49]

The concept of a Hybrid Multilevel Converter is justified in [50] which states that "The switching losses of medium voltage IGBTs strongly increase with the blocking voltage of the IGBT. For a good exploitation of the IGBT the switching losses compared to the conduction losses in the IGBT should not get too high. The optimal ratio of switching and conduction losses is similar for different types of IGBT with different blocking voltages. Keeping this ratio constant, the pulse frequency of the IGBT needs to be reduced with higher blocking voltages" where

the pulse frequency is the switching frequency of the converter.

This Hybrid concept is implemented in [49] to create a Hybrid Multilevel Converter constructed from two types of modules, one operating with twice the DC link of the other. Both of these modules are shown in Figure 2.14 (A1 + A2). The higher voltage module, A1, is constructed from IGCTs and operates at 2.2kV while the lower voltage module, A2, is constructed from IGBTs and operates at 1.1kV. The resulting converter has 7 levels, with the high voltage device switching at the fundamental frequency and the low voltage device switching at 1.4kHz. This converter had the advantages of a high switching speed and therefore waveform quality, due to the IGBT, as well as the ability to produce a medium voltage waveform with relatively low conduction losses, due to the IGCT. The performance of this converter was only presented as a simulation study.

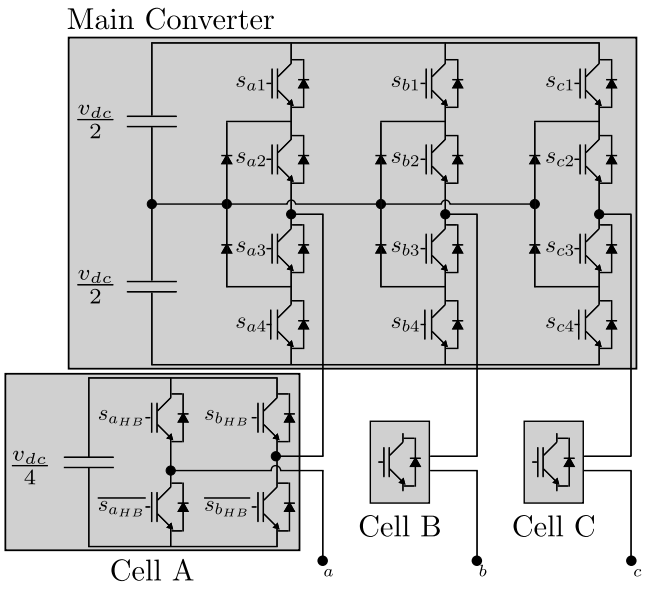


Figure 2.15: Diode Clamped Multilevel Hybrid Cycloconverter [51]

Reference [51], shown in Figure 2.15, is based on a Diode Clamped 3 level 3-Phase inverter with an additional high frequency Cell constructed from a H-Bridge and floating capacitor. A modulation technique is proposed based on a state machine that utilizes redundant switching states to naturally balance the floating capacitor voltage. However due to the requirement of maintaining the floating capacitor voltage, a reduction in the modulation index is required. Hence the maximum AC voltage is the same as that obtained by using a single Diode Clamped 3 level inverter. A simulation study is carried out to study the

stability of the converter and the effectiveness of the state machine to maintain the correct floating capacitor voltage. The converter was found to charge up the floating capacitor cells in 6 seconds from initial start up and maintain the Voltage with a ripple of approximately 1.5V.

As mentioned above, the significant issue with the Cycloconverter Topology is that the MF transformer has be designed to process twice the peak power of the competing DAB topology as both the peak flux density and peak current are $\sqrt{2}$ times bigger than the RMS.

The use of an additional converter, connected to a flying capacitor would be able to not only improve the quality of the output waveform but it would be able to increase the utilization of the installed power in the MF transformer. This additional converter could be connected in series to reduce the peak flux density in the core or in parallel to reduce the peak current. The transformer core size has a limit in cross-sectional set by the maximum allowable flux density for the given magnetic material, irrespective of core losses.

For a MF transformer with a ferrite core the maximum allowable flux density results in a minimum core cross-sectional area with very low losses. The peak current has no such hard limit in cross-sectional area and is instead limited by the losses in the conductor. As this research is focused on reducing the transformer size, a series arrangement was selected as this will result in the greatest reduction in transformer size, allowing the core to come closer to the thermal limit of the material rather than the peak flux density.

The size of the electrolytic capacitor required for the additional converter would be minimal when compared to the capacitors required in the DC link of the converter, so would not significantly impact the size, cost or reliability of the converter. This will be the focus of this Ph.D. as it is felt that a converter of this design is both novel and has the potential to meet the requirements of this project as specified in Chapter 1.

2.5 Summary

This chapter has summarized the key topologies and developments in the area of Medium Voltage Multilevel Converters.

Series connected topologies, namely the Diode-Clamped Multilevel Inverter and the Flying Capacitor Multilevel Inverter are discussed first, highlighting the issues relating to these two topologies: There is a quadratic relation between the number of devices (clamping diodes or Flying Capacitors) and the number of converter levels. This makes them unsuitable for MV converters with a large number of levels.

Multicell topologies overcome the problems of a large number of devices for converters with more than three levels. Two examples have been described: the M^2LC and the UNIFLEX-PM converters. The key issues relating to the Multicell converter topologies are the requirement of a large number of isolated voltage sources or large DC link electrolytic capacitors. This in turn requires individual expensive voltage measurement and an advanced control scheme to maintain the capacitor voltage (in the case of the M^2LC converter) as well as reduced converter reliability and increased size and cost.

Cycloconverters however do not store energy in the intermediary link and therefore do not suffer from the disadvantages of additional electrolytic capacitors. Three common Cycloconverter circuit configurations have been discussed and each configuration was analysed in terms of its suitability for the inverter requirements of the project requirements given in Chapter 1.

The requirements for this project are for a converter with a small transformer and additional energy storage devices and high reliability whilst maintaining reasonable efficiency.

The Cycloconverter Topology was selected due to its inherent ability for soft-switching, allowing for high frequency operation, therefore minimizing the size of the high frequency transformer. This will also result in the converter having a lower weight and longer lifetime due to the absence of electrolytic capacitors in

the intermediary link when compared with a VSI based converter.

The result of this analysis was the selection of 2-leg Cycloconverter over the single leg Cycloconverter due to the reduced size of the transformer. The 2-leg Cycloconverter was selected in preference to the 3-leg Cycloconverter due to the ability for the 2-leg Cycloconverter to be used as a single phase module in a Hybrid Multilevel Converter, allowing a higher voltage converter to be constructed from multiple LV modules. The 3-leg Cycloconverter, due to the connection within the converter of the neutral point, is not able to be used as a converter module in a Hybrid Converter and therefore would be unable to meet the requirements of this project. This has resulted in the selection of the 2-leg Cycloconverter as the main converter topology.

Finally the advantages and disadvantages of a Hybrid Cycloconverter were discussed: The advantages are the reduction in conduction losses with no increase in switching losses, and the increased output waveform quality requiring less filtering. The disadvantages are the lack of modularity in the converter resulting in reduced redundancy and increased cost, and the requirement of additional energy storage devices.

It was concluded that for this project the advantages of a Hybrid topology outweigh the disadvantages. The final converter topology consists of three two leg single phase Cycloconverters connected to an auxiliary 3-Phase VSI. This converter topology was selected to reduce the size of the MF transformer. As with the traditional two leg Cycloconverter Topology, the installed power in the transformer has to be greater than the RMS power, as much as twice the value in some cases. By utilizing an additional converter, not only is there the possibility of a reduction in the switching harmonics in the AC grid current waveform, but the installed power in the Cycloconverter can be reduced by injecting power when the AC grid voltage is at the peak and recovering this power during the low points in the AC grid voltage cycle.

Chapter 3

Overview of Topologies

This chapter describes the Cycloconverter Topology and compares its operation with that of the benchmark Triple VSI Topology. The Hybrid Cycloconverter Topology is then introduced; this is a converter based on the Cycloconverter Topology but containing an additional auxiliary 3-Phase VSI. The most effective technique to split the converter AC voltage demand between the Main Converter, constructed from the Cycloconverter and VSI stage, and the additional auxiliary 3-Phase VSI is investigated so as to provide a significant reduction in peak power from the Cycloconverter whilst only requiring a low power auxiliary 3-Phase VSI. The division of voltage between the converters is analysed on a harmonic level in order to establish the optimum balance when utilizing a converter with no neutral connection. Switching waveforms from the converters are simulated in order to gain an insight into the performance of each converter with regard to the transformer core loss, copper loss and core area.

3.1 Triple VSI Topology

In order to explain the operation of the Cycloconverter Topology, the operation of the simpler benchmark converter, the Triple VSI Topology, will be analysed first. A single phase converter will initially be described, followed by the 3-Phase variant. The Triple VSI Topology is a DC – AC bi-directional converter designed

to interface a DC network to an AC network, with a high frequency transformer to provide isolation. The Triple VSI Topology is constructed from 3 H-Bridges, called VSI 1, 2 and 3.

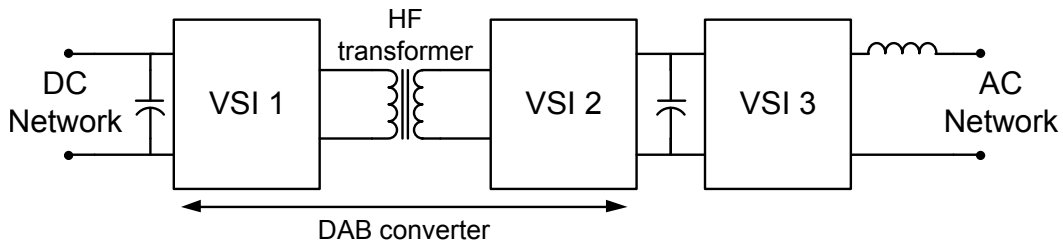


Figure 3.1: Single phase Triple VSI based topology converter structure

The single phase Triple VSI Topology converter structure is shown in Figure 3.1 and can be broken down into 2 parts; a DAB DC-DC converter to provide isolation, constructed from VSI 1, VSI 2 and a HF transformer. VSI 3 is used to provide the interface with the AC network. The Triple VSI Topology is a well researched and documented converter topology and has shown itself to be a competitive topology for high power, MV applications [32]. It includes large electrolytic capacitors as energy storage devices in the intermediary DC link.

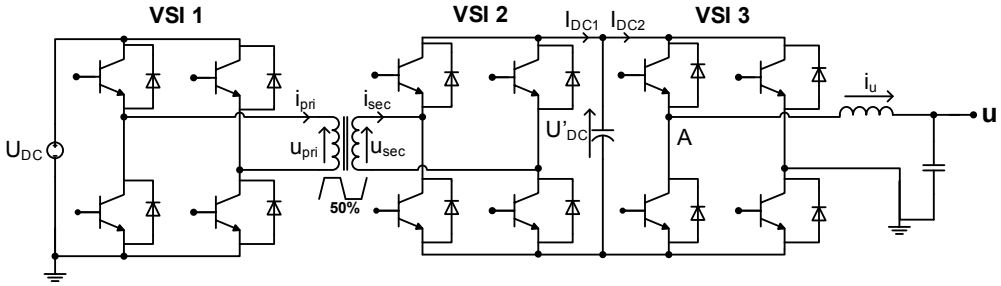


Figure 3.2: Single phase Triple VSI Topology schematic

The energy storgae contained in the Triple VSI converter results in the peak power processed by the DAB being equal to the average power processed by the whole converter, resulting in lower losses and the ability to utilize smaller switching devices and transformer. The additional electrolytic capacitors are the main disadvantage of the Triple VSI Topology due to the increased cost, size and unreliability that they add.

3.1.1 The Dual Active Bridge Converter

The single phase Dual Active Bridge (DAB) converter [52], is utilized in [35] to provide isolation between two power networks via a high frequency transformer. The DAB converter can be thought of as two AC voltage sources, u_{pri} and u_{sec}, connected by the leakage inductance of the transformer, Figure 3.2. As with any AC transmission network, the inductance and phase shift between two voltage sources controls the direction and amplitude of the power flow. With the DAB converter, a square wave is generated by Voltage Source Inverter (VSI) 1 and 2 instead of a sine wave.

Triple VSI based Topology Control Scheme

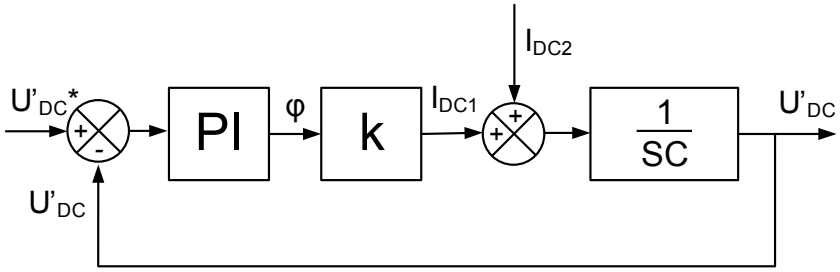
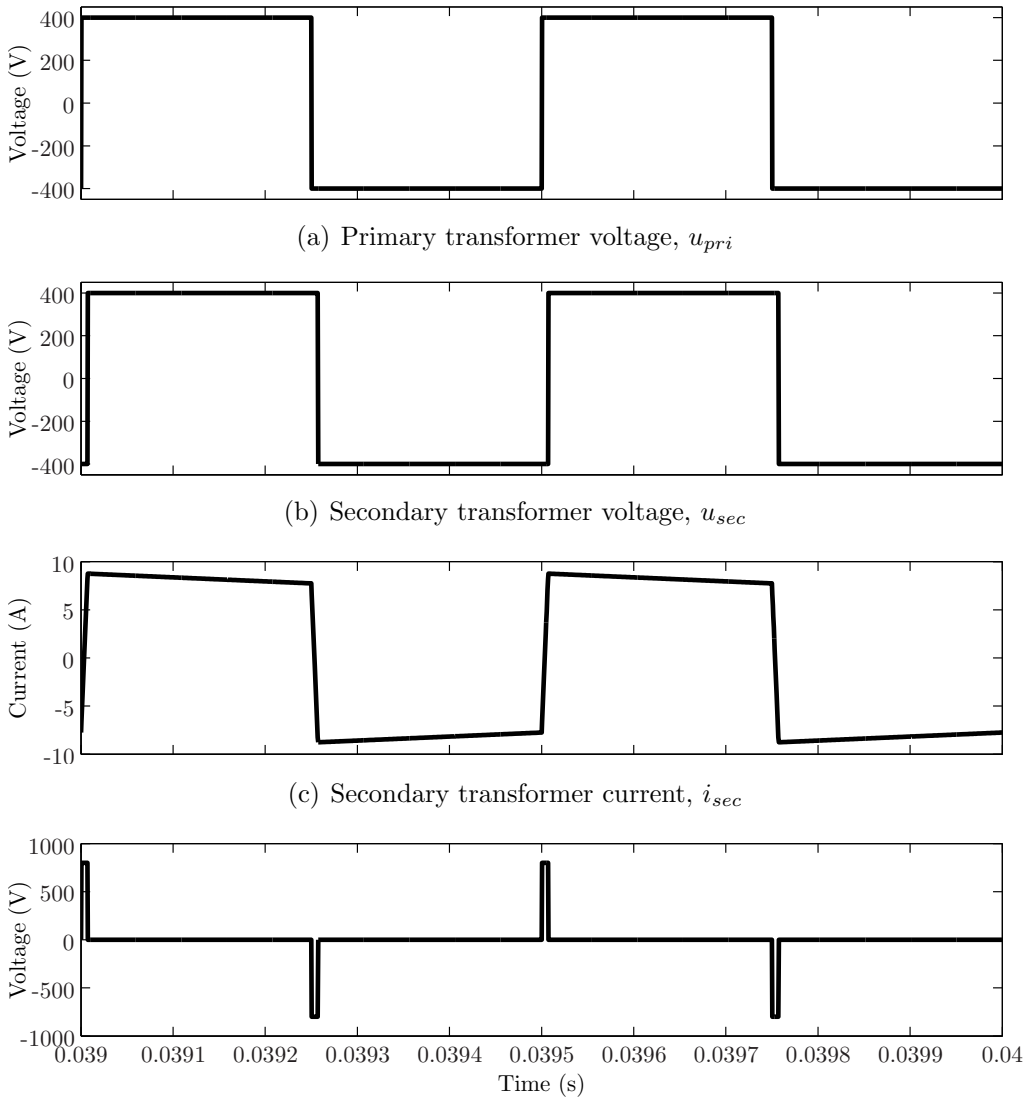


Figure 3.3: DAB converter control diagram

The control scheme for the DAB converter is based on keeping the intermediary DC link voltage, U'_{DC}, constant for all powers fed to the grid. The voltage U'_{DC} is controlled so as to be equal to the DC network voltage, U_{DC}. Figure 3.3 shows the control system diagram. The controller measures U'_{DC} and subtracts it from $U'_{DC}*$ to give an error voltage. This error is fed into a PI controller and the output is the desired phase shift, ϕ, between the two square wave voltage sources, increasing i_{sec} and hence I_{dc1}. The current to VSI 3, I_{DC2} is seen as a disturbance to the control system. It will have a 100Hz component but the capacitor will be large enough so that the 100Hz will not appear on on U'_{DC}.

In order to calculate the relationship between ϕ and I_{dc1}, the value of the constant k needs to be established.

Operation of DAB Converter



(a) Primary transformer voltage, u_{pri}

(b) Secondary transformer voltage, u_{sec}

(c) Secondary transformer current, i_{sec}

(d) Voltage across transformer leakage inductance, u_{pri} - u_{sec}

Figure 3.4: Waveforms from the DAB section of the Single phase Triple VSI based topology

The magnitude of i_{sec} is proportional to the phase shift between the two voltage sources, u_{pri} and u_{sec}. The introduction of ϕ between u_{pri} and u_{sec} results in a short period of time at which there is a voltage drop across the leakage inductance, L_{leak}, in the transformer. The drop is the sum of the two DC links ($U_{DC} + U'_{DC}$) (Figure 3.4(d)). This results in a change in current in the transformer of:

$$\Delta i_{pri} = \frac{(U_{DC} + U'_{DC})\Delta T}{L} \tag{3.1}$$

If the magnetizing current of the transformer is small, we have:

$$I_{DC} = |i_{sec}| = |i_{pri}| \tag{3.2}$$

and the change of current of (3.1) is equal to:

$$2|i_{sec}| = 2|I_{DC1}| \tag{3.3}$$

therefore:

$$I_{dc1} = \frac{(U_{DC} + U'_{DC})\Delta T}{2l} \tag{3.4}$$

we have:

$$\Delta T = \frac{\phi T}{2\pi} \tag{3.5}$$

where T is the period of the square wave.

Finally if we assume U'_{DC} is well controlled and $= U_{DC}$ then:

$$I_{dc1} = \frac{U_{DC} T}{2l\pi}\phi = k\phi \tag{3.6}$$

Techniques to Reduce Switching Losses

Based on the work described in [53] and [54], the switching strategy for the DAB converter in the Triple VSI Topology will be investigated. One of the advantages of the DAB converter is that significantly reduced switching losses can be obtained using capacitor snubbers (Figure 3.5).

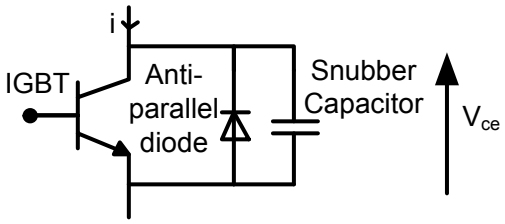


Figure 3.5: Arrangement of snubber capacitors across switching devices

The turn off losses are reduced due to the snubber capacitor limiting the dV/dt during the switching transition. At turn on, the current, i, is initially negative and the anti-parallel diode conducts first and the snubber capacitor is therefore discharged before the IGBT starts conducting when the current turns positive. Hence the IGBT turns on when $V_{ce} = 0$, a Zero Voltage Switching (ZVS) transition. However when operating at low power levels, the current will fall to zero before the snubber capacitor has been fully discharged and instead will be discharged into the IGBTs, stressing them and increasing the switching losses above the level of a standard hard switched converter without snubbers.

It is therefore necessary to ensure that there is always a minimum current passing through the transformer and at low power levels the transformer current can be supplemented by a reactive current to prevent this from occurring. At these power levels the efficiency of the DAB converter will be significantly reduced. The converter that will be simulated in this research will not use any capacitor snubbers and the turn off transitions will be hard switched. This is to reduce the complexity of the switching strategy of the DAB converter. Soft switching for this converter has already been experimentally verified [55] and therefore requires no further validation. If this converter were to be utilized for a practical application soft switching with snubber capacitors could be utilized.

Transformer Parameters

The leakage inductance, L_{leak}, of the transformer is a key element in controlling the power flow in the DAB converter. If the phase shift between the primary and secondary windings is made too large the reactive power transferred for building up the current in the transformer will be a similar magnitude to the real power transferred during the remainder of the cycle. It is therefore sensible to limit the phase shift to a maximum value, for example 10%. Depending on the switching frequency and L_{leak}, this will limit the current transferable by the converter to a maximum value. L_{leak} will also influence the accuracy in control of the power transferred by the converter.

As with all digital systems, there are a finite number of discrete phase angle steps between u_{pri} and u_{sec} that can be selected. With a smaller L_{leak} there will be a greater difference in current for each step change in phase angle. Due to the voltage drop across the switching devices and winding resistance in the transformer, the current, i_{sec} through L_{leak} will decrease when $u_{pri} = u_{sec}$. A larger L_{leak} will reduce the rate at which i_{sec} decreases therefore reducing the i_{sec} (peak) for a given average current. Therefore the design of the transformer and L_{leak}, is crucial to the construction of a converter based on this topology and should be specified to allow the maximum power the converter is designed to supply. An excessively large L_{leak} will result in the sampling delays in the control system and the resolution of the ADCs and DACs introducing a significant error in ϕ.

The magnetizing inductance of the transformer should be as large as possible to reduce the magnetizing current and the winding resistances should be as small as possible, particularly at high frequencies, to reduce the copper losses, whilst not adding excessive size, cost and weight to the converter. The loses in the core of the transformer due to eddy currents should be minimized by the selection of a suitable core material for the frequency of operation. Amorphous metal or ferrite alloys are suitable for this application due to the high electrical resistance of these materials.

The inverter stage of the converter utilizes VSI 3 to connect the DC link, U'_{DC}, to the AC voltage network, u. The converter generates a pulse width modulated

voltage waveform V_{A0} and utilizes an inductor to create an alternating current at the fundamental frequency. The PWM waveform can be generated by a number of methods, either analogue or digital, e.g.(Space Vector PWM (SVPWM), Sinusoidal PWM (SPWM) or Harmonic Elimination PWM (HEPWM)). The operation of this type of converter has been well documented so will not be investigated further in this document. The DC link capacitor has to provide enough stored energy over half a 50Hz cycle so that the U_{DC2} is a constant value, without a 100Hz variation, as well as having a low enough Equivalent Series Resistance (ESR) to prevent overheating from the high frequency current ripple.

3.1.2 3-Phase Triple VSI Converter Operation

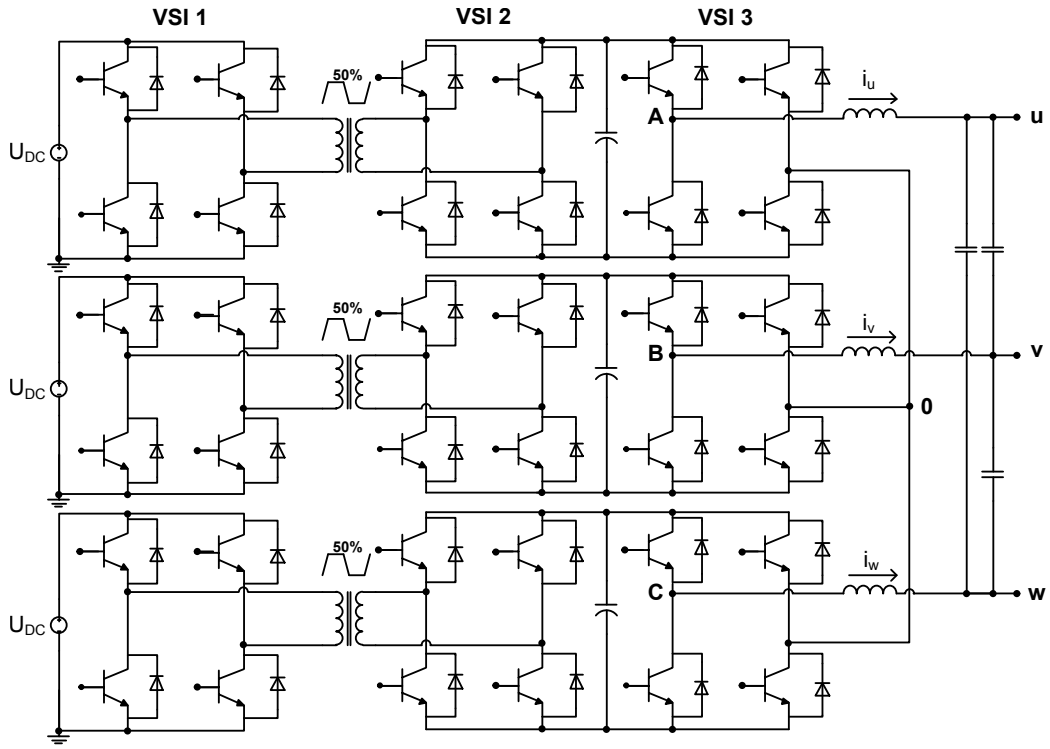


Figure 3.6: Triple VSI Topology schematic

By connecting three single phase converters together, a 3-Phase converter can be constructed, as shown in Figure 3.6. Each converter operates independently and the AC network currents, i_u i_v i_w, can be controlled independently or as a 3-Phase system.

Common Mode Harmonic Injection

Triplen harmonics are harmonics that are multiples of three of the fundamental (3^{rd}, 6^{th}, 9^{th} etc.). They are called common mode in that they have the same phase for all three phases for a 3-Phase system. When the triplen voltage harmonics are added to each phase, they will be cancelled in the line to line output voltage, u_{A0}, u_{B0} and u_{C0}.

An injection of common mode triplen harmonics into the demand voltage waveform, u_{A0}, u_{B0} and u_{C0}, results in a peak voltage reduction required by each phase, whilst maintaining the same line to line voltage. This can result in a smaller cored transformer if the peak flux is fixed, due to the fact that U_{DC} and U'_{DC} can be reduced. This has been utilized in order to achieve a modulation index greater than 1 [56], or to increase the utilization factor of the DC link voltage [57].

All triplen harmonics are cancelled and therefore are suitable for this technique [58]. However [57] demonstrates that the peak voltage reduction is achievable with just the 3^{rd} harmonic and calculates the optimum amplitude of the harmonic as being $^1/_6$ of the size of the fundamental, resulting in an increase in the modulation index by 15.5%. Common mode harmonic cancellation is shown to be a feature exploited by SVPWM [56] and as such many converters controlled with SVPWM are likely to already benefit to a degree from this reduction, although it is unlikely to be optimized.

For nonsinusodial waveforms, the envelope of a 3-Phase waveform can be centred around zero using an injection of common mode harmonics using the Max-Min approach [59]. This technique sums together the maximum and minimum value of any of the three phases and divides the total by 2. The Max-Min waveform is then subtracted from each of the three phases and the resulting waveform will have distributed a voltage peak in any one phase amongst the other two, allowing the converter to operate with a lower DC link voltage for a given Modulation Index (MI). The mathematical expression for the Max-Min implementation is:

$$u_{Max-Min} = \frac{Max({u_u}^*, {u_v}^*, {u_w}^*) + Min({u_u}^*, {u_v}^*, {u_w}^*)}{2} \tag{3.7}$$

The disadvantage with common mode harmonic injection is that the neutral point in the converters will now be at the potential of the injected common mode harmonic. Therefore the converter will not be able to provide a neutral point to the system, and so will only be able to provide power to loads that do not require a neutral. This will reduce the applications the converter is suitable for, including any phase imbalance correction and harmonic compensation.

Inverter Current Control Scheme for Triple VSI Based Topology

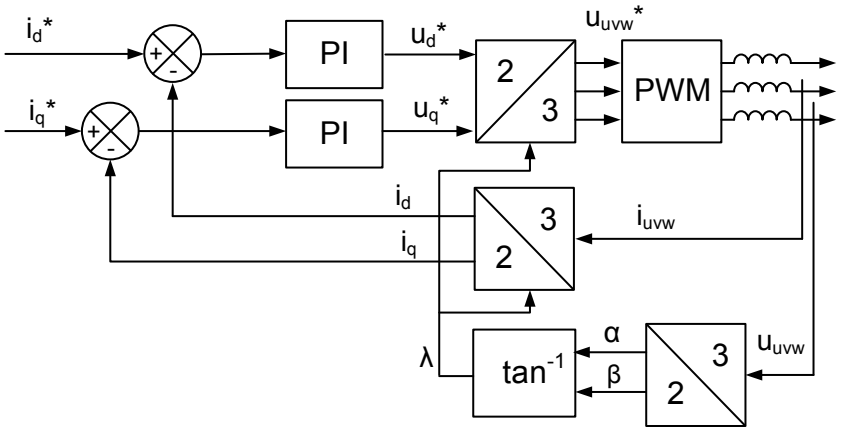


Figure 3.7: 3-Phase control system diagram

Figure 3.7 shows the devised control scheme for the VSI 3 for the triple VSI based converter. VSI 3 will utilize a *d-q* current controller in which the *d-axis* is oriented on the voltage vector of u_{uvw}. The 3-Phase output current is converted into the *d-q* domain and for both the *d* and *q-axis*, the measured output current is subtracted from the current demand to give the error current. This error current is fed into a PI controller to produce an output demand voltage. This demand is converted back into the *ABC* domain to give the 3-Phase output voltage vectors. For this experimental converter, $i_d{}^*$ and $i_q{}^*$ will be varied during the testing, with $i_d{}^*$ the reference for the real power transferred by the converter, and $i_q{}^*$ the reactive. If operating from a system with a fixed power output, i_d and i_q will be the resultant and therefore the control system would need to be designed in the opposite direction. However for this application the DC link is considered to be an ideal DC source able to source or sink current indefinitely without it affecting the DC link voltage.

3.2 Cycloconverter Topology

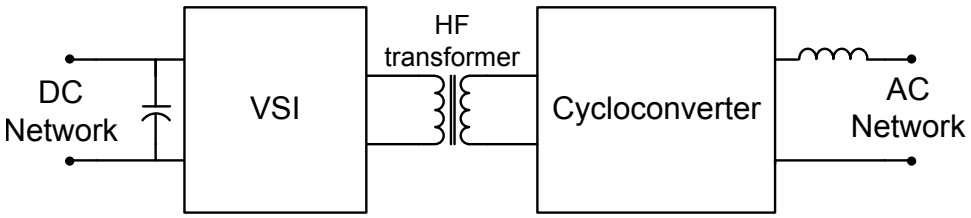


Figure 3.8: Single phase Cycloconverter Topology converter structure

The Cycloconverter Topology is a bi-directional DC – AC converter that utilizes a high frequency transformer for isolation between the DC and AC networks. To interface the DC network to the transformer, an H-Bridge is used, constructed from unidirectional switches and called the VSI stage. To interface the AC network to the transformer, an H-Bridge is used, constructed from bi-directional switches. This section will be called the Cycloconverter stage. Figure 3.8 shows the single phase Cycloconverter Topology structure.

The Cycloconverter Topology does not contain any additional energy storage devices, resulting in a potentially smaller, lighter and more reliable converter which could be suitable for applications that are deemed too critical to failure to allow for electrolytic capacitors (for example aerospace). However this means that the instantaneous power has to be processed by the whole converter, and the transformer and switching devices have to be scaled accordingly.

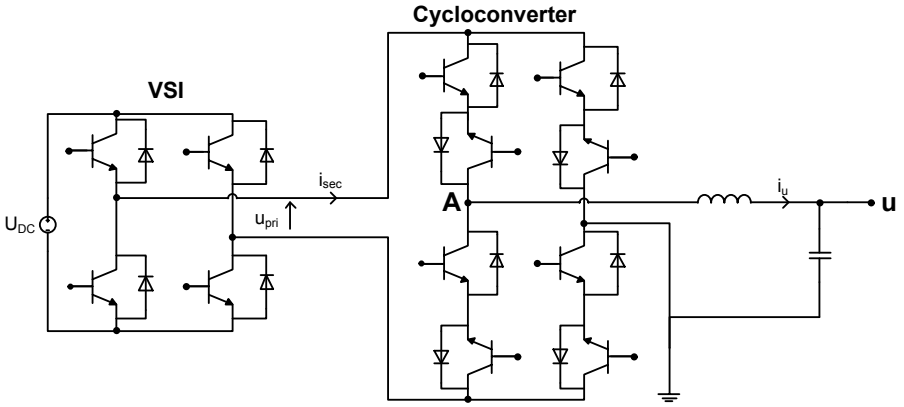
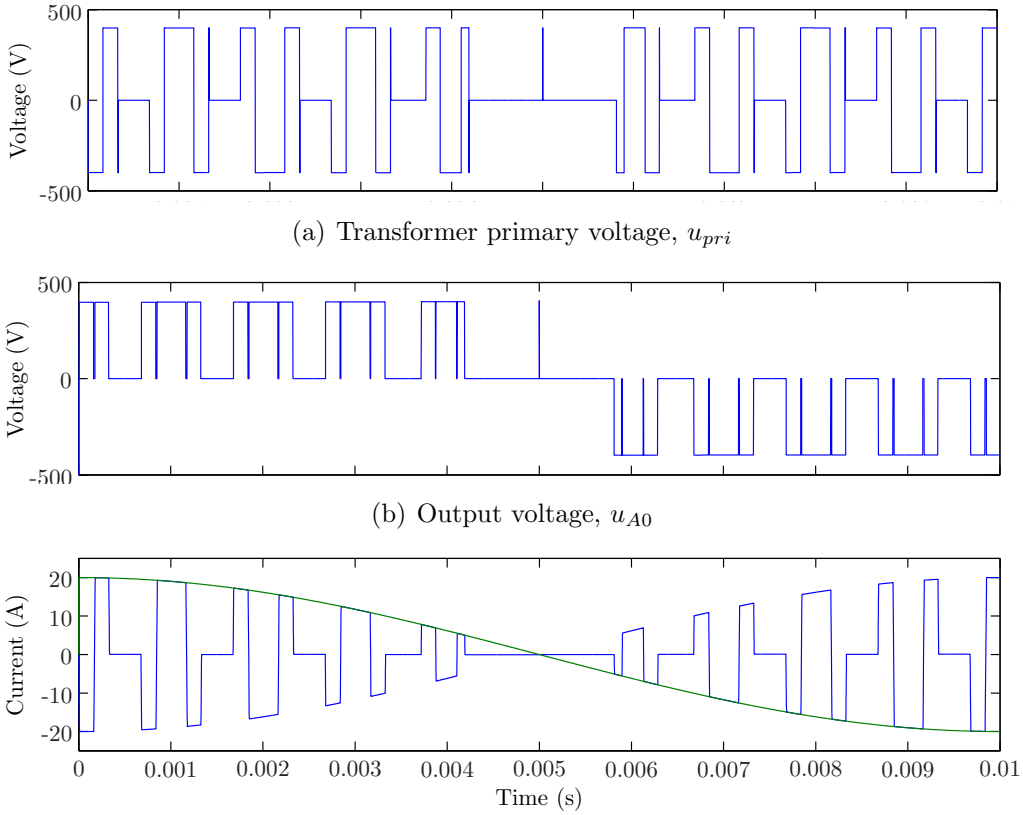


Figure 3.9: Simplified single phase Cycloconverter Topology schematic without HF transformer

The operation of the Cycloconverter Topology relies on a different principle of operation to the Triple VSI Topology, due to the lack of a voltage source on the AC side of the transformer. For the initial explanation, a simplified single phase model (Figure 3.9) will be used. A more in-depth analysis of the actual 3-Phase converter, describing switching strategies and the effect of component parameters on the circuit operation, will then be given.

The schematic shown in Figure 3.9 can transfer power to and from the AC network to the DC network. The VSI is able to produce a 3 level waveform, u_{pri}, of $+U_{DC}$, 0 and $-U_{DC}$, Figure 3.10(a). As in the simplified case $u_{pri} = u_{sec}$, the Cycloconverter is able to connect u_{pri} to u_{A0} either directly or by inverting u_{pri} ($+U_{DC}$ becomes $-U_{DC}$ or $-U_{DC}$ becomes $+U_{DC}$), Figure 3.10(b). It can be seen that the Cycloconverter stage acts as a polarity controllable rectifier and is able to rectify the square wave produced at u_{pri} either positively or negatively depending on the required polarity of u_{A0}. The current in the transformer, i_{sec}, is shown in Figure 3.10(c).



(a) Transformer primary voltage, u_{pri}

(b) Output voltage, u_{A0}

(c) Transformer current, i_{sec} with AC current envelope, i_u, i_v or i_w

Figure 3.10: Operation of Cycloconverter Topology showing key current and voltage waveforms

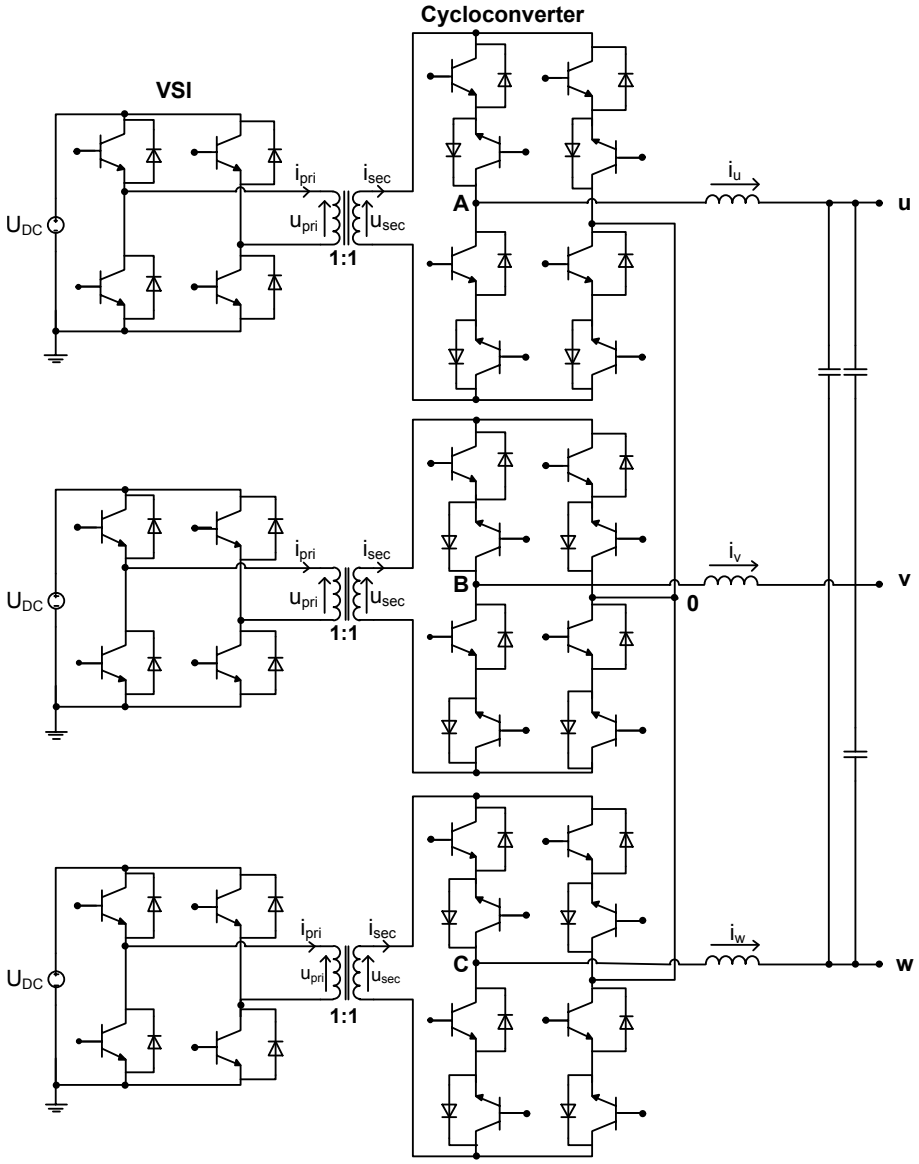


Figure 3.11: Cycloconverter Topology schematic

To provide isolation between the DC and AC networks a transformer is required. In order to reduce the size of this transformer, the waveform applied to the primary, u_{pri}, has to consist of square wave operating at a frequency many times higher than the fundamental AC line voltage. To achieve this the desired AC PWM waveform, u_{A0}, is broken up into alternating positive and negative pulses, transmitted over the high frequency transformer, Figure 3.10(a), and then reassembled by the Cycloconverter, Figure 3.10(b). The issues with this topology revolve around the parasitic components in the transformer, specifically the leakage inductance, that add considerable complexity to the switching of the converter.

Figure 3.11 shows the schematic diagram of the complete Cycloconverter Topology. The VSI stage is constructed from 4 IGBTs and diodes connected in a standard H-Bridge arrangement. The Cycloconverter stage is constructed from 8 IGBTs and diodes connected in pairs in a back to back arrangement. This creates a bi-directional H-Bridge formed from 4 bi-directional switches. The 3-Phase converter is constructed from three of the single phase converters, with the AC line connected in a star arrangement and the DC line connected in parallel.

The control scheme for the Cycloconverter Topology will be the same as that for VSI 3 in the Triple VSI Topology. The switching strategy will be managed by the FPGA and will be considered to be ideal for the control system design. The Cycloconverter Topology will be assumed to be an ideal voltage source connected to a line inductor. The control system diagram is shown in Figure 3.7.

3.2.1 Switching Strategies for Cycloconverter Topology

The switching strategy for Cycloconverter Topology has been researched [60] [44] and techniques are demonstrated to ensure that all switching transitions are either ZVS or ZCS, resulting in minimal switching losses. This will allow the Cycloconverter Topology to switch at a much higher frequency than other hard switched converters whilst maintaining low switching losses. For the simulation models and experimental converter the turn off transitions in the VSI stage will be hard switched to reduce the complexity of the modulation technique.

PWM Voltage Pulse Generation

The VSI stage is able to generate three voltage levels on the primary of the transformer, u_{pri}, $+U_{DC}$, $-U_{DC}$ and 0. The Cycloconverter stage can connect the transformer secondary to u_{A0}, invert the connection or short circuit u_{A0}. It is therefore possible to generate a sine based PWM voltage waveform at u_{a0} with one of two possible techniques. The VSI stage can be used to generate a square wave at u_{pri} with a 50% duty cycle and a 3-level PWM pulse can be constructed from this at u_{A0} by the Cycloconverter stage [60] [44]. The other approach is to

use the primary VSI stage to generate a PWM waveform multiplied by a high frequency (i.e. 5kHz) square wave at u_{pri} and the Cycloconverter stage unfolds this waveform to recreate the fundamental PWM waveform.

The first technique is advantageous as it is well researched and has the ability to utilize one primary VSI stage on a transformer with multiple windings to create a 3-Phase converter. However this switching strategy has the disadvantage of increasing core losses, due to the fact that the core operates with a constant flux density over half a period of the output waveform even when the voltage required by the converter is not at its peak.

The second technique allows for the core losses to be reduced by reducing the VSI duty cycle when the output voltage from the converter is not at its peak. However to prevent the copper losses in the transformer from increasing, the Cycloconverter should be short circuited when a zero pulse is required by the converter, otherwise the free-wheeling output current will flow through the transformer. This technique also operates the Cycloconverter stage under ZVS with no additional components.

Impact of Modulation Technique on the Transformer Core Flux

A 3-level PWM pulse is generated at u_{pri} using a Sinusoidal PWM (SPWM) technique as shown in Figure 3.12(a), using two triangle carriers compared against the demand sine wave. In order to utilize this pulse train with the Cycloconverter Topology, the polarity of the pulse is inverted one or more times per cycle. 3 novel techniques for achieving this are shown in Figure 3.12.

To compare the techniques with regard to transformer sizing, the waveforms were integrated and plotted in Figure 3.12(e). The first technique has a huge value of peak to peak flux which will therefore lead to an excessive transformer core size. The second technique has non-zero flux during between each PWM pulse, resulting in excessive core losses. The third technique has reduced peak flux and zero flux during the u_{pri} zero voltage pulses, however this technique has one extra switching transition for every pulse, resulting in higher switching losses in the converter.

A table summarizing the results is shown in 3.1 with the data normalized to a square wave modulation technique for the Cycloconverter Topology. The peak to peak value of flux is of interest as it defines the minimum core cross-sectional area for a transformer constrained by peak flux density. The RMS flux is of interest as it allows for a rough approximation of core losses for waveforms that have a similar spectral density however for an accurate prediction of core losses the harmonic spectrum of the voltage waveform needs to be analysed in order to calculate the losses for each frequency. The number of switching transitions is of interest as it relates to the switching losses of each modulation scheme in the semiconductor devices. Chapter 6 will document a more in-depth simulation of the transformer for the three modulation techniques, covering the magnetizing current, peak flux and core losses.

	Modulation 1	Modulation 2	Modulation 3
P-P flux (pu)	1.97	0.99	0.99
RMS flux (pu)	1.18	0.79	0.27
SW transitions (per Hz)	1	1	1.33

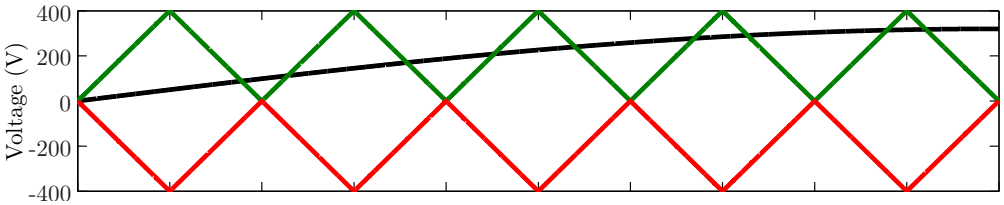
Table 3.1: Comparison of 3 modulation techniques for the cycloconverter

Commutation Process of Cycloconverter Stage

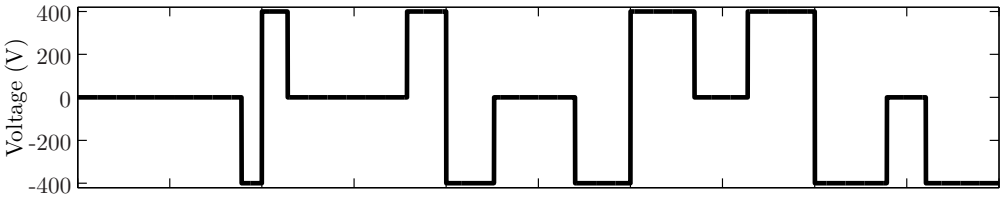
In order to illustrate the operation, we will limit the explanation to the phase u_{A0}. As this is a 3-Phase converter this explanation also applies to the other two phases, u_{B0} and u_{C0}.

The complexity of the switching strategy comes from the fact that the leakage inductance, L_{leak}, in the transformer acts as a current source as does the line inductive filter. Therefore it is only possible to switch the Cycloconverter stage when the value of these two current sources is equal, otherwise the mismatch will destroy the switching devices. Care needs to be taken in order to build up the u_{A0} in L_{leak} to the value of the AC current, i_u and therefore i_{sec}, before switching the Cycloconverter stage.

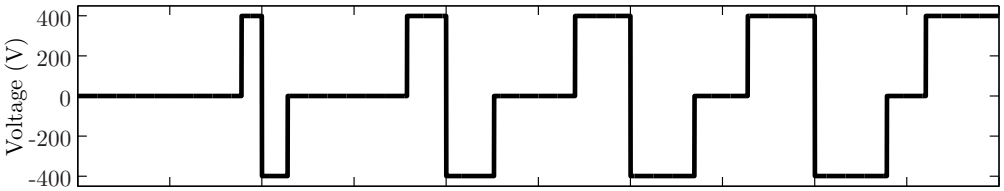
By applying a voltage to u_{pri} and short circuiting u_{sec}, it is possible to build the



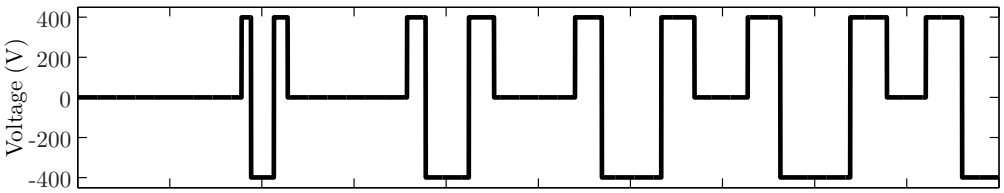
(a) Triangle carriers and demand sine wave



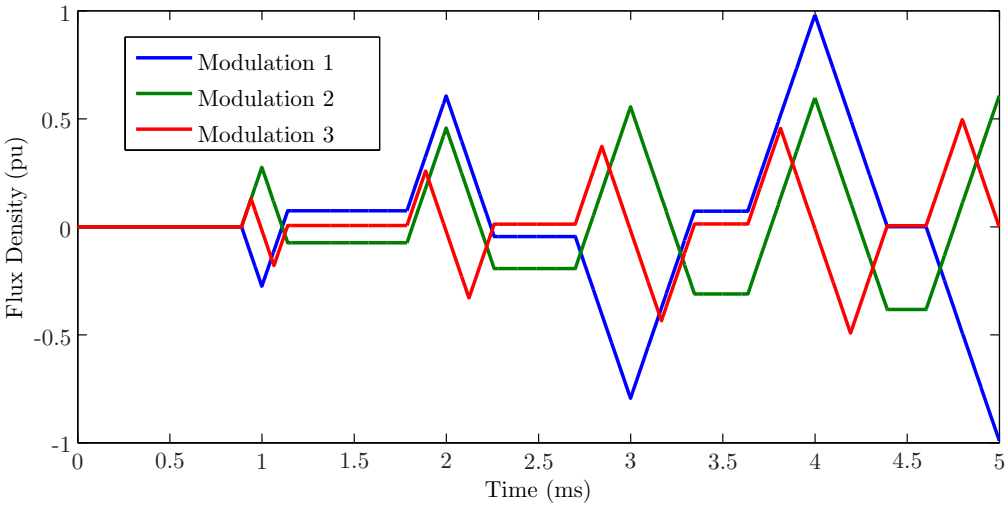
(b) u_{pri}, transformer primary voltage with Modulation Technique 1



(c) u_{pri}, transformer primary voltage with Modulation Technique 2



(d) u_{pri}, transformer primary voltage with Modulation Technique 3



(e) Transformer core flux density with 3 proposed modulation techniques, normalized to square wave modulation technique

Figure 3.12: Analysis of flux in transformer core

current in i_{sec}. The direction of i_{sec} will depend on the polarity of the applied voltage to u_{pri}. When the AC voltage, u_{u0}, and current, i_u, have the same polarity, i_{sec} will build up and the integrated diodes in the IGBTs will naturally perform the commutation as soon as $i_{sec} = i_u$. If i_u and u_{u0} have different polarities then this process has to be controlled due to the fact that the current needs to be built up in the reverse direction before commutation will occur.

In this case a reverse voltage is first applied to u_{pri} so that i_{sec} builds up in the correct direction. When i_{sec} has matched the value of i_u, the Cycloconverter stage commutates and connects u_{sec} to u_{A0}. The correct polarity pulse is then applied to u_{pri} by the VSI stage. There will always be a small current error between the two sources at commutation, even with the commutation performed by the diodes, due to reverse recovery, and as such a clamp or snubber circuit must always be used to absorb this extra energy.

3.2.2 Transformer Design Considerations

The most important parameter in the construction of the transformer is the transformer leakage inductance, L_{leak}. A greater value of L_{leak} will help to reduce the required energy the clamp or snubber circuit has to absorb at each switching transition for a given time delay error from processing (due to the stored energy being $^1/_2 L_{leak} I^2$), but a large value of L_{leak} will distort the AC waveform because of the excessive time required to build up i_{sec} to the correct value before switching. For this converter it was decided to minimize the leakage inductance and use switching devices in the Cycloconverter stage with minimal reverse recovery.

The magnetizing inductance should be as large as possible to reduce the magnetizing current and the winding resistances should be as small as possible, particularly at high frequencies, to reduce the copper losses, while not adding excessive size, cost and weight to the converter. The core should be manufactured from a material that has a high resistance to prevent excessive core losses from eddy currents.

3.3 The Hybrid Cycloconverter Topology

The Hybrid Cycloconverter Topology is shown in Figure 3.13 and is an extension to the 3-Phase Cycloconverter Topology, created by adding an additional auxiliary 3-Phase VSI between the star point and each phase of the Cycloconverter stage. The auxiliary 3-Phase VSI is connected to a flying capacitor and is only able to inject reactive power. For this converter the VSI stage, Cycloconverter stage and HF Transformer will be called the Main Converter.

By shaping the voltage demand of each phase of the Main Converter, e.g. u_{a3}, and injecting an equal but opposite distortion on the auxiliary 3-Phase VSI voltage demand, e.g. u_{30}, it is possible to significantly reduce the peak voltage synthesized by the Main Converter whilst insuring that the phase voltage remains constant so there is no net power transfer from the auxiliary 3-Phase VSI. This will allow the voltage ratings of the switching devices and the peak flux in the transformer in the Main Converter to be considerably reduced, making it more competitive with the Triple VSI Topology.

The following section investigates three different waveform shaping techniques. The analysis is based on a sinusoidal demand voltage and division of u_{u0} between u_{A3} and u_{30}. The analysis will present different 'shapes'; the demand waveform of the Main Converter, e.g. u_{A3}, and the demand waveform of the additional auxiliary 3-Phase VSI, e.g. u_{30}. These shapes are constructed so that u_{A3} and u_{30} are summed to form u_{u0} which is equal to the sinusoidal demand voltage, e.g. u_{A0}. Due to the inherent common mode cancellation of a 3-Phase converter, the harmonic content of each waveform shaping technique was analysed in order to establish the most effective technique for reducing the peak voltage with the minimal size of the additional components.

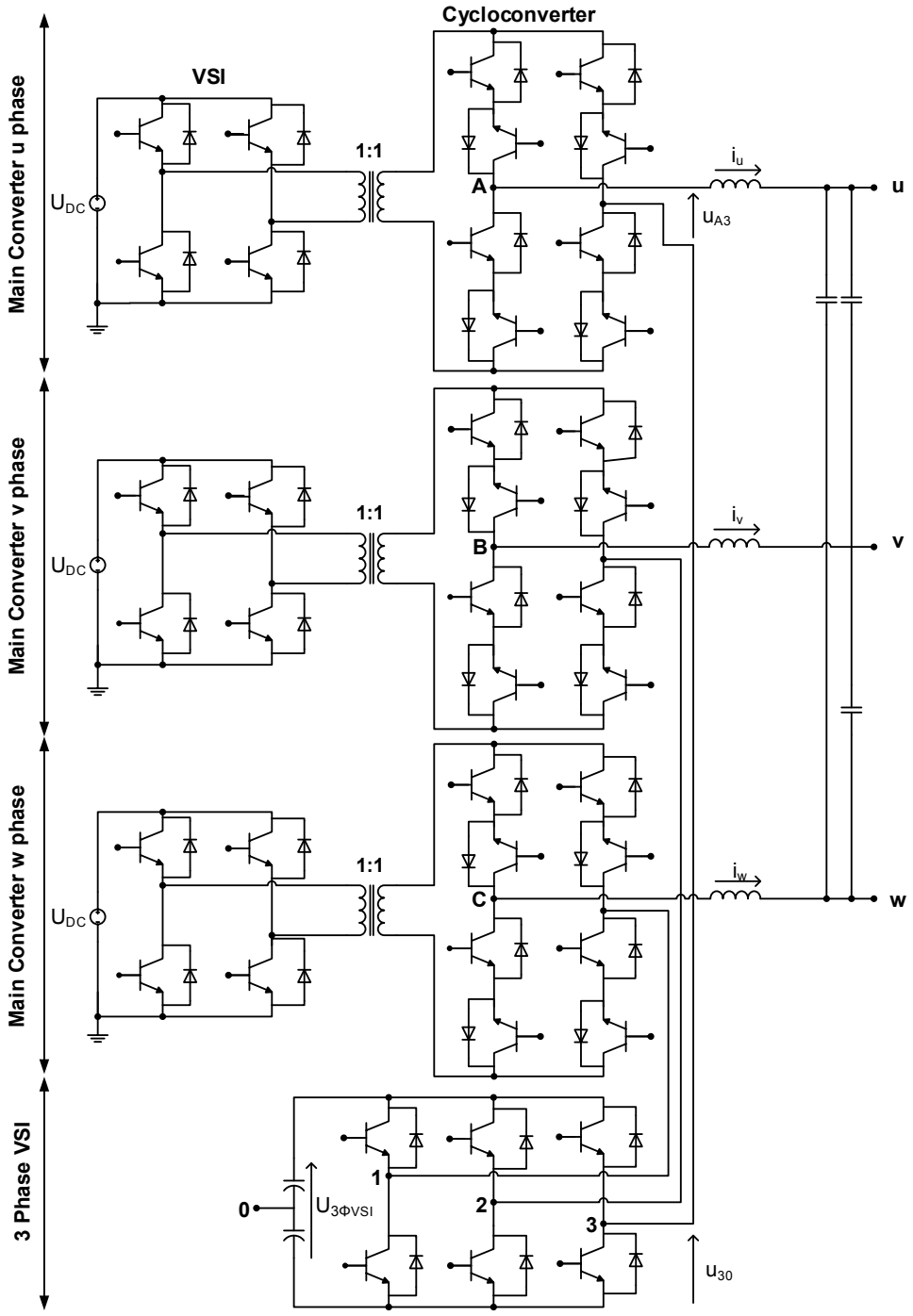


Figure 3.13: Hybrid Cycloconverter Topology schematic based on a auxiliary 3-Phase VSI and 3 Main Converters (Cycloconverter, VSI and HF Transformer)

3.3.1 Voltage Distribution Scheme 1: the Shifted and Clipped Waveform Shape

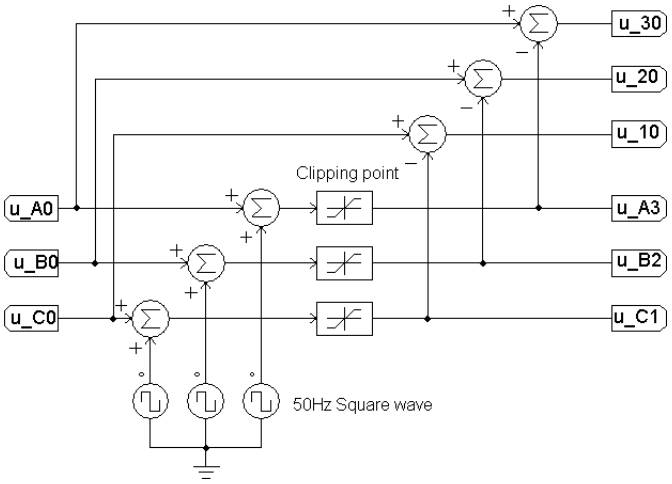


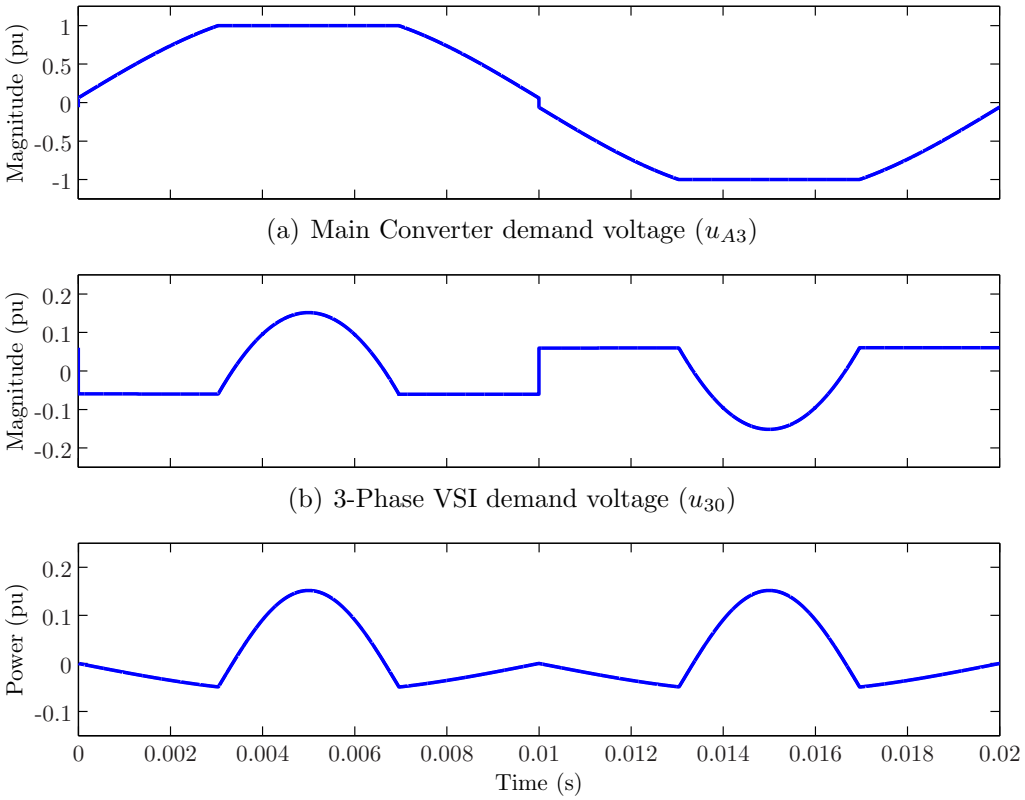
Figure 3.14: Division of voltage demand between Main Converters and additional 3-Phase VSI for the Shifted and Clipped waveform shape

Without any triplen cancellation, an efficient waveform shape for utilizing $U_{3\Phi VSI}$ is shown in Figure 3.15 and 3.16. It is based on assuming $U_{3\Phi VSI}$ is constant and utilizing this voltage fully ($U_{3\Phi VSI} = u_{30}$) when the required u_{A0} is low. This allows U_{DC} to be reduced by the greatest amount whilst ensuring no net energy transfer from $U_{3\Phi VSI}$. Figure 3.14 shows how this waveform shape was implemented in simulation.

The Main Converter demand voltage, e.g. u_{A3}, is generated for the Shifted and Clipped waveform shape by adding a 50Hz square wave to the total phase demand, e.g. u_{A0}, and clipping the resulting waveform at a set point. The demand voltage waveform for the 3-Phase VSI, e.g. u_{30}, is generated by subtracting the Main Converter demand from the total phase demand voltage, e.g. u_{A0}. With this modulation scheme the injected harmonics contain a fundamental component and therefore require an adaptive control strategy that will vary the amplitude of the square wave used to construct the waveform shape based on the phase angle of the current. This is to prevent the power transferred to the flying capacitor to be non zero over half a cycle.

Figure 3.15 shows the shifted and clipped waveform shape with a $U_{3\Phi VSI}$ amplitude of $0.3pu$ and Figure 3.16 shows the waveform shape with a $U_{3\Phi VSI}$ of $0.6pu$.

It can be seen in Figure 3.15 that the peak in demand voltage (Figure 3.15(b)) with a $U_{3\Phi VSI}$ of 0.12pu is as the same time as the peak in the Main Converter demand voltage (Figure 3.15(a)). With a $U_{3\Phi VSI}$ of 0.3pu (Figure 3.16) it can be seen that during the peak in Main Converter demand voltage (Figure 3.16(a)) the demand voltage of the 3-Phase VSI (Figure 3.16(b)) is not at the maximum value and this is to maintain zero power transfer over half a cycle (Figure 3.16(c)).



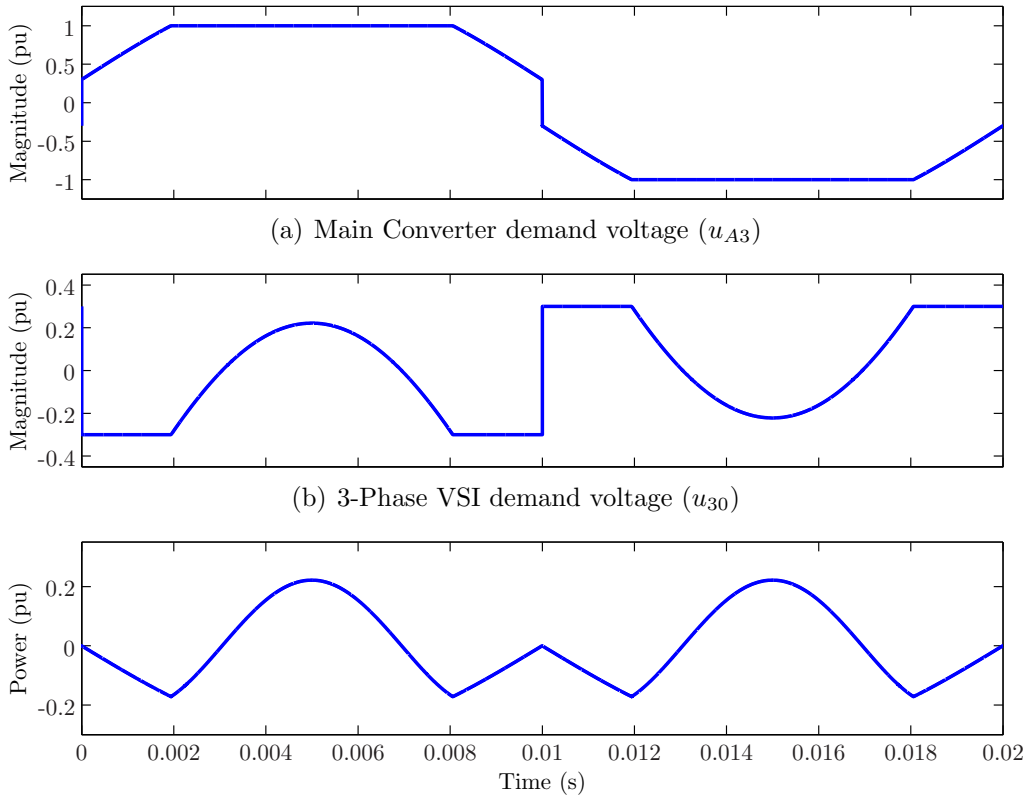
(a) Main Converter demand voltage (u_{A3})

(b) 3-Phase VSI demand voltage (u_{30})

(c) 3-Phase VSI power ($u_{30}i_u$)

Figure 3.15: Scheme 1, the Shifted and Clipped voltage distribution scheme, VSI amplitude = 0.12pu

For voltage distribution schemes involving triplen cancellation, the harmonic content of the injected waveform becomes much more important and as such there is no simple method for establishing the most efficient use of the additional auxiliary 3-Phase VSI. Two techniques have been presented here, a trapezoid based waveform shape and a clipped sine wave derived shape. Future research could be carried out using an iterative method to establish the most efficient waveform shape based on the amplitude of the VSI for a given fundamental amplitude.



(a) Main Converter demand voltage (u_{A3})

(b) 3-Phase VSI demand voltage (u_{30})

(c) 3-Phase VSI power ($u_{30}i_u$)

Figure 3.16: Scheme 1, the Shifted and Clipped voltage distribution scheme, VSI amplitude = 0.3pu

3.3.2 Voltage Distribution Scheme 2: the Trapezoidal Waveform Shape

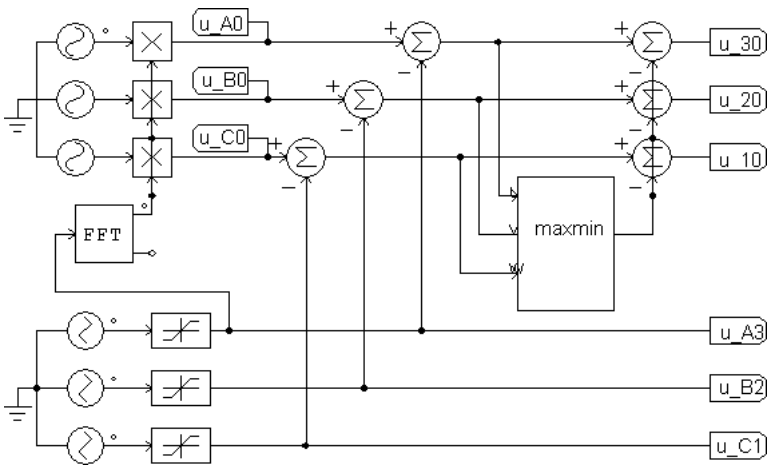
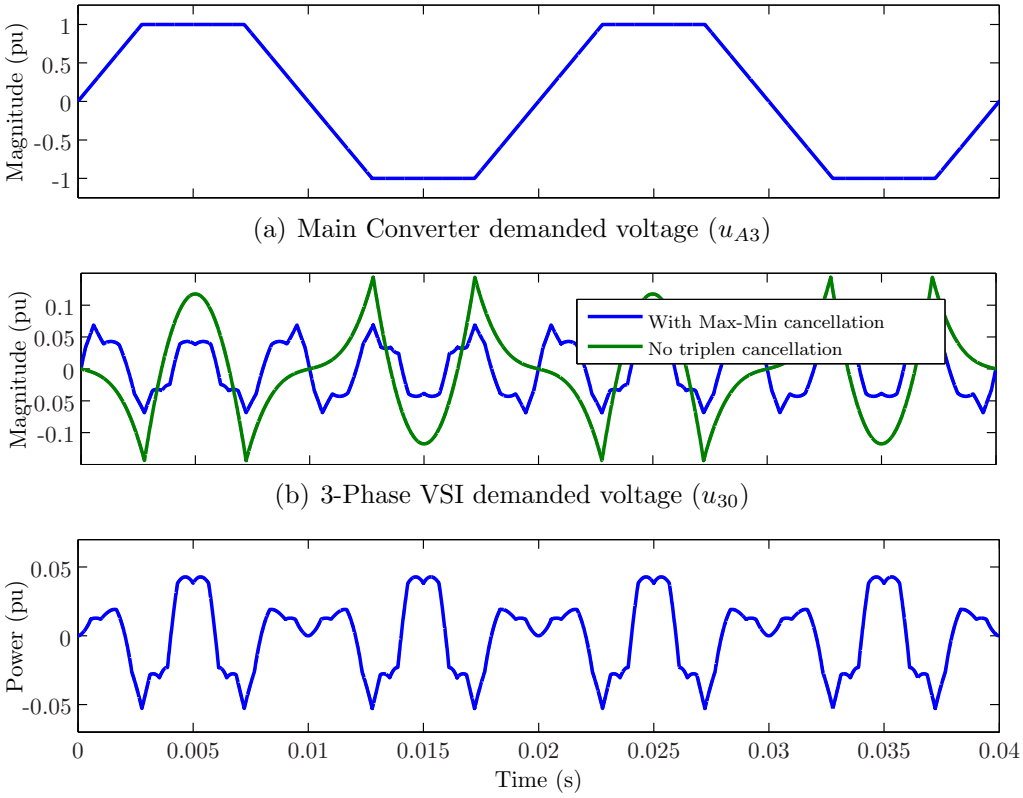


Figure 3.17: Division of voltage demand between Main Converters and additional 3-Phase VSI for the Trapezoid voltage distribution scheme

Figure 3.18 shows a voltage distribution scheme based on a trapezoid shape. The Main Converter reference waveform, e.g. u_{A3}, is generated by clipping a trapezoid at a set point. The resulting fundamental amplitude component of this waveform, calculated as a DC component with the PSIM FFT block, is the total converter demand voltage, e.g. u_{A0}. In an experimental converter the amplitude of the fundamental component would need to be stored in a lookup table for a given trapezoid angle and clipping point. The demand voltage for the 3-Phase VSI, e.g. u_{30} is calculated by subtracting u_{A0} from u_{A3} followed by the removal of the envelope offset and triplen using the Max-Min block (equation 3.7).



(a) Main Converter demanded voltage (u_{A3})

(b) 3-Phase VSI demanded voltage (u_{30})

(c) 3-Phase VSI power ($u_{30}i_u$)

Figure 3.18: Scheme 2, the Trapezoid based voltage distribution scheme

This voltage distribution scheme was selected due to the fact that a trapezoid meets many of the criteria required for good performance; it has a flat top, allowing the DC link voltage of the single phase VSI, U_{DC}, to be capped at a set value and sloping sides resulting in lower amplitude higher order odd harmonics than is the case for a square wave. As all triplen harmonics will be cancelled the only substantial harmonics for the auxiliary 3-Phase VSI to modulate are the 5^{th}, 7^{th} and 11^{th}. The slope of the trapezoid is varied in order to measure the

increase in the AC fundamental, u_{u0} and the required DC link of the auxiliary 3-Phase VSI, $U_{3\Phi VSI}$, for a constant DC link voltage, U_{DC}. With a low amplitude trapezoid angle, the shape is more triangular, and as such will require a high voltage rated VSI and will produce a waveform with a below unity *pu* fundamental amplitude. It will however contain less high frequency harmonic components. As the trapezoid becomes more like a square wave, the amplitude of the fundamental, u_{u0}, will increase as will the auxiliary 3-Phase VSI voltage u_{30}. Figure 3.17 shows how this waveform shape was implemented in simulation.

When the angle of the sides of the trapezoid increases to such an extent that the cycloconverter generates a square wave at u_{A3}, the auxiliary 3-Phase VSI DC link voltage, $U_{3\Phi VSI}$, is required to be twice as large as U_{DC}. The peak fundamental voltage at u_{A0} will now be $^4/_\pi$ compared with the peak voltage of u_{A3} (and U_{DC}). A balance therefore should be found between U_{DC} and $U_{3\Phi VSI}$.

3.3.3 Voltage Distribution Scheme 3: Sine, 3rd and Clipped Waveform Shape

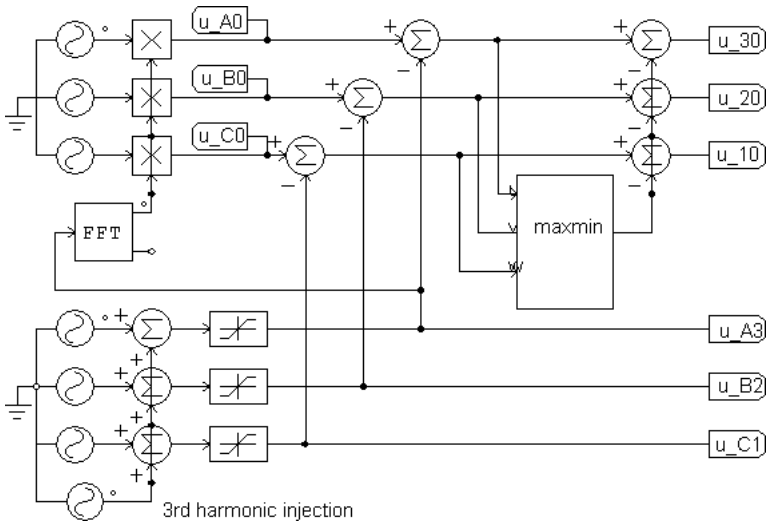


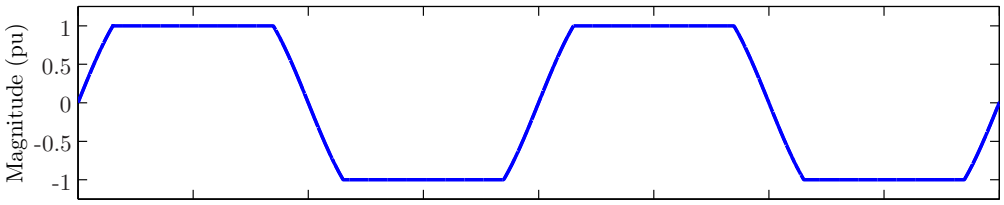
Figure 3.19: Division of demanded voltage between Main Converters and additional 3-Phase VSI for the Sine, 3rd and Clipped waveform shape

A third voltage distribution scheme was devised in order to fully utilize the installed power in the additional converter with only a low amplitude u_{30} waveform.

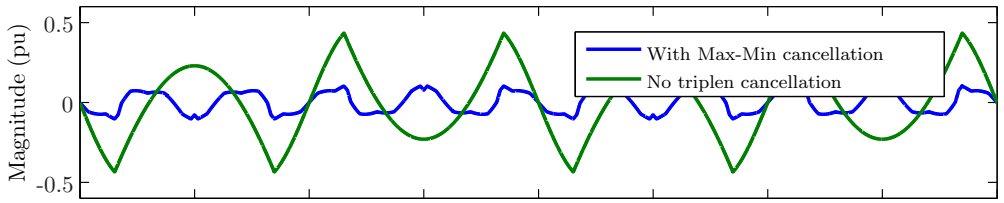
This is due to the fact that the trapezoid requires a substantial $U_{3\Phi VSI}$ to produce a fundamental voltage below unity *pu*.

Further, to take into account the triplen cancellation ability of the converter, an additional 3rd order harmonic is added to the converter voltage demand (e.g. $u_u{}^*$) before being clipped at a set point.

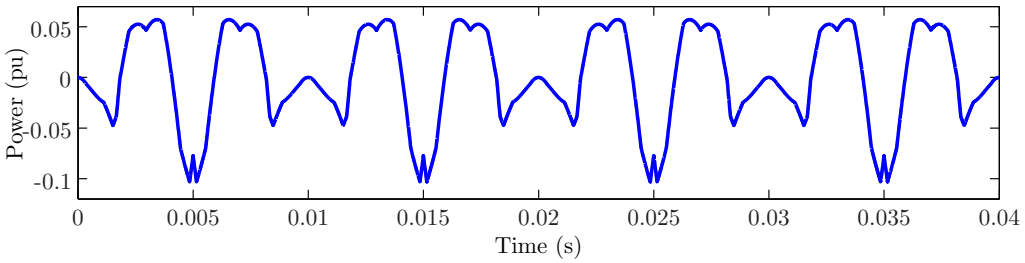
The Main Converter reference waveform, e.g. u_{A3}, is generated by adding a third harmonic to a fundamental sine wave and clipping the resulting waveform at a set point. The resulting fundamental component of this waveform, calculated with the FFT block, is the total converter demand voltage, e.g. u_{A0}. In an experimental converter the fundamental amplitude would need to be stored in a lookup table for a given waveform shape. The demand voltage for the 3-Phase VSI, e.g. u_{30} is calculated by subtracting u_{A0} from u_{A3} followed by the removal of the envelope offset and triplens using the Max-Min block (equation 3.7). Figure 3.19 shows how the voltage distribution scheme was implemented in simulation.



(a) Main Converter demand voltage (u_{A3})



(b) 3-Phase VSI demanded voltage (u_{30})



(c) 3-Phase VSI power ($u_{30}i_u$)

Figure 3.20: Scheme 3, the Sine, 3rd and Clipped based voltage distribution scheme

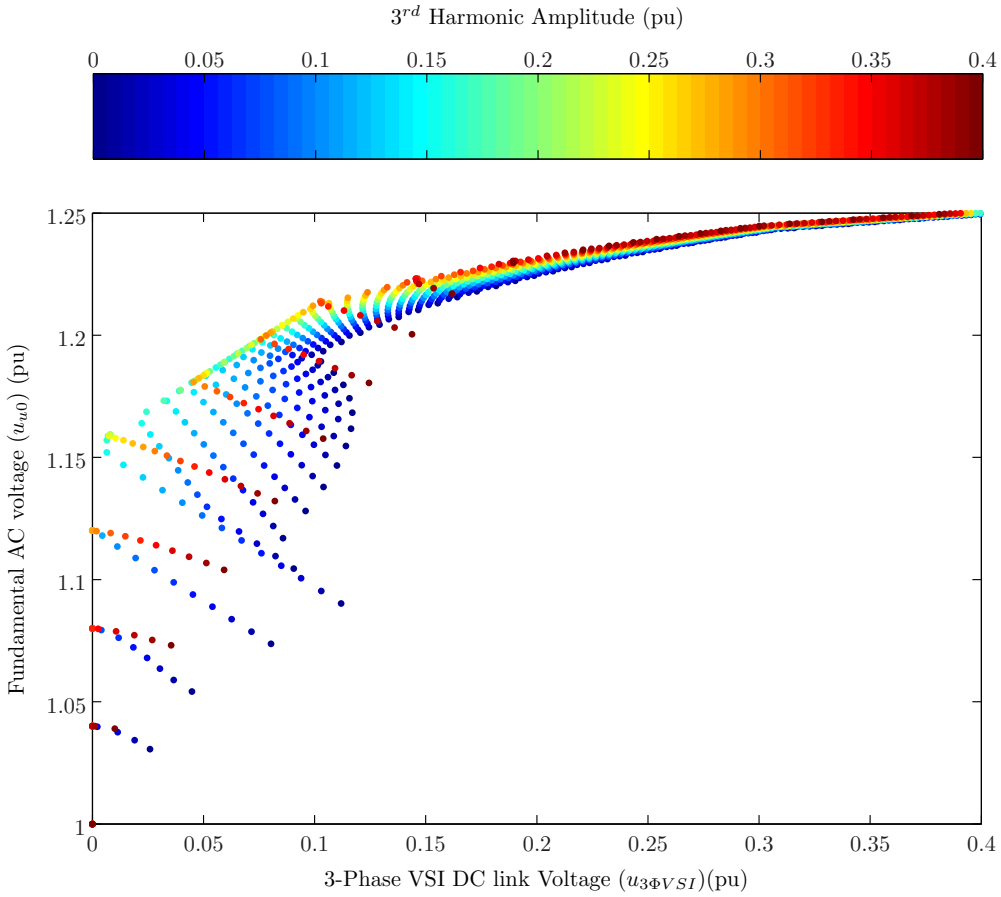


Figure 3.21: Voltage Distribution Scheme 3, based on a shape comprised of a clipped sine and 3rd harmonic waveform, with varying 3rd harmonic amplitudes

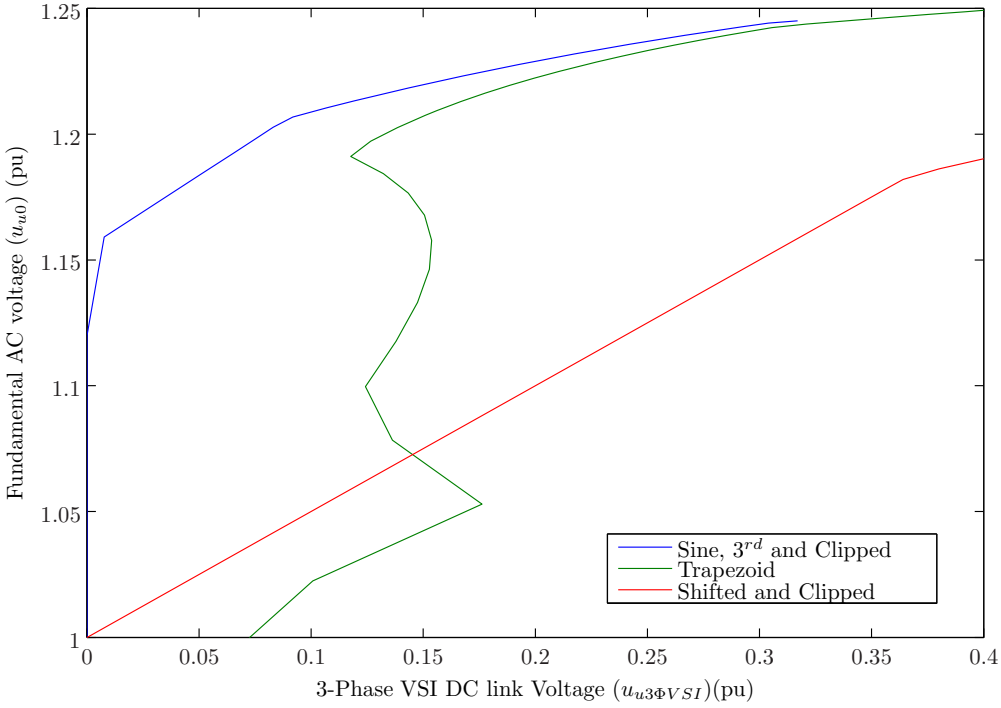


Figure 3.22: Comparison of 3 proposed modulation schemes

3.3.4 Comparison of Proposed Voltage Distribution Schemes on Hybrid Cycloconverter Topology Performance, Based on Average Model Simulations

An average model simulation was carried out to investigate the required $U_{3\Phi VSI}$ compared with the total converter output voltage, u_{u0}, for the 3 proposed voltage distribution schemes. An average model simulation ignores the PWM switching of the converter and instead assumes the Cycloconverter and auxiliary 3-Phase VSI produce the demanded voltages exactly. The AC fundamental u_{u0} is displayed against $U_{3\Phi VSI}$.

An average model simulation is one in which the switching harmonics are not considered and the PWM waveform is replaced with an ideal variable voltage source. Figure 3.21 shows the results from Scheme 3 for a range of values $(0 - 0.255)$ of additional 3^{rd} harmonic. The clipping point was set at 1 and the amplitude of the sine wave was varied. Figure 3.22 shows the results from the three proposed voltage distribution schemes. Scheme 1 shows the worst performance due to the fact that this modulation scheme does not take advantage of the triplen cancellation ability of the converter. Scheme 2 has good performance with a $U_{3\Phi VSI}$ greater than 0.18. However below this value Scheme 3 has the best performance due to the inherent triplen cancellation ability of this converter.

3.4 Comparison of Topology Performance Based on Switching Model Simulations

In order to compare the relative size of the transformer for the Triple VSI, the Cycloconverter and the Hybrid Cycloconverter Topologies, a simulation was carried out that included the switching of the converters so as to obtain the transformer voltage and current waveforms.

The output power from the three converters was kept constant; the output voltage was 230V RMS phase-neutral and the output current was 14A RMS. A transformer magnetizing inductance of $10mH$ was included in the simulation for all the

converter topologies. The Hybrid based topology utilized Scheme 3 (the Sine, 3rd and Clipped waveform shape) as the selected voltage distribution scheme. The shape was constructed with a $0.813pu$ Main Converter amplitude and a $0.085pu$ auxiliary 3-Phase VSI amplitude.

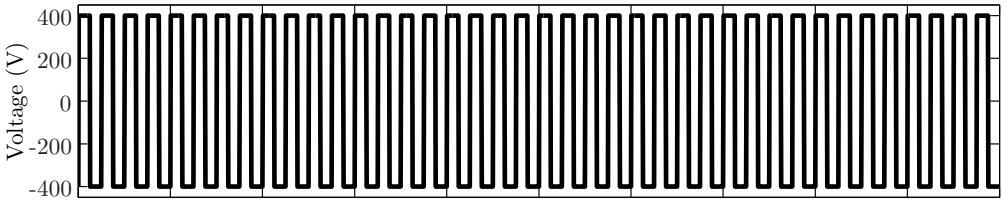
Figure 3.23(a) shows the primary voltage waveform, u_{pri}, Figure 3.23(b) the integrated primary voltage waveform, $\int u_{pri}$ and Figure 3.23(c) the transformer secondary current, u_{sec}, for the Triple VSI Topology. Figure 3.24 shows the Fast Fourier transform (FFT) of these respective waveforms. It can be seen that due to the square shape of the voltage in Figure 3.23(a) and trapezoid shape of the current, 3.23(c), the harmonic content of these waveforms are centred on a single frequency and its odd harmonics (Figure 3.24(a) and 3.24(c)).

Figure 3.25(a) shows the primary voltage waveform, u_{pri}, Figure 3.25(b) the integrated primary voltage waveform, $\int u_{pri}$ and Figure 3.25(c) the transformer secondary current, u_{sec}, of the Cycloconverter Topology and Figure 3.26(a), 3.26(b) and 3.26(c) shows the FFT of these respective waveforms. It can be seen that the harmonic content of these waveforms have been spread over a greater frequency range, due to the multiplexing of the PWM waveform with a high frequency square wave.

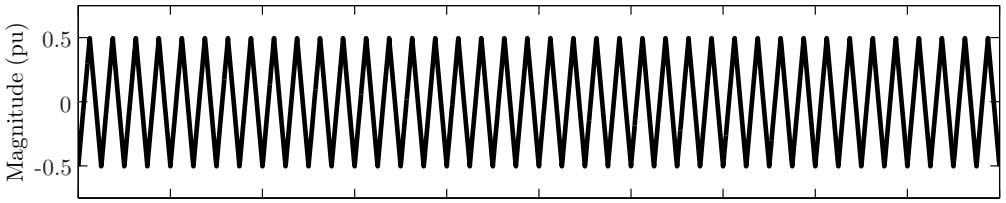
Figure 3.27(a) shows the primary voltage waveform, u_{pri}, Figure 3.27(b) the integrated primary voltage waveform, $\int u_{pri}$ and Figure 3.27(c) the transformer secondary current, u_{sec}, for the Hybrid Cycloconverter Topology and Figure 3.28(a), 3.28(b) and 3.28(c) show the FFT of these respective waveforms. The Hybrid Cycloconverter Topology has voltage, current and flux waveforms similar to the Cycloconverter Topology, however the 3rd harmonic side-bands in the transformer current have a lower amplitude. A more detailed analysis will be carried out in Chapter 6.

	Cycloconverter	Hybrid
P-P flux (pu)	1.52	1.3
RMS voltage (pu)	0.71	0.74
RMS flux (pu)	0.94	0.95
RMS Current (pu)	1.42	1.38

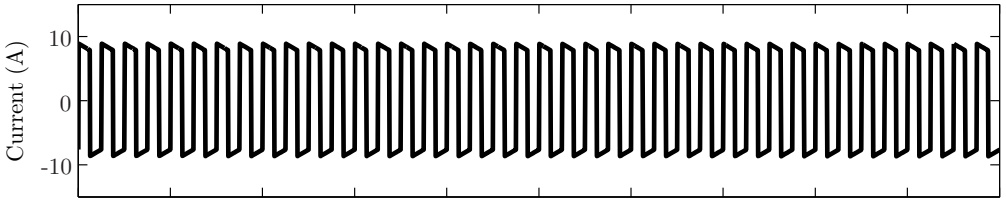
Table 3.2: Transformers requirements in pu, compared against the requirements of the DAB converter ($1pu$)



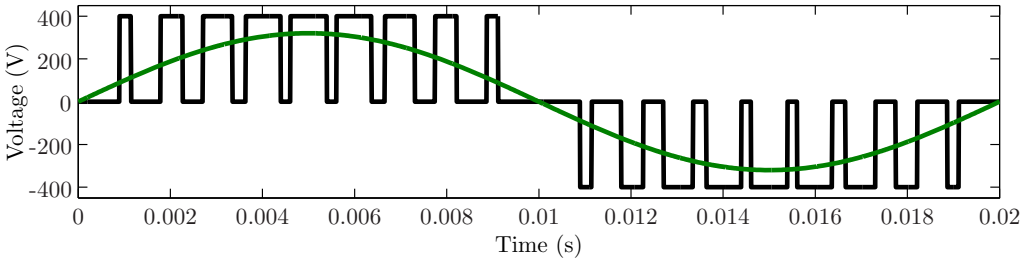
(a) Primary voltage waveform, u_{pri}



(b) Integrated u_{pri}, $\propto$ core flux

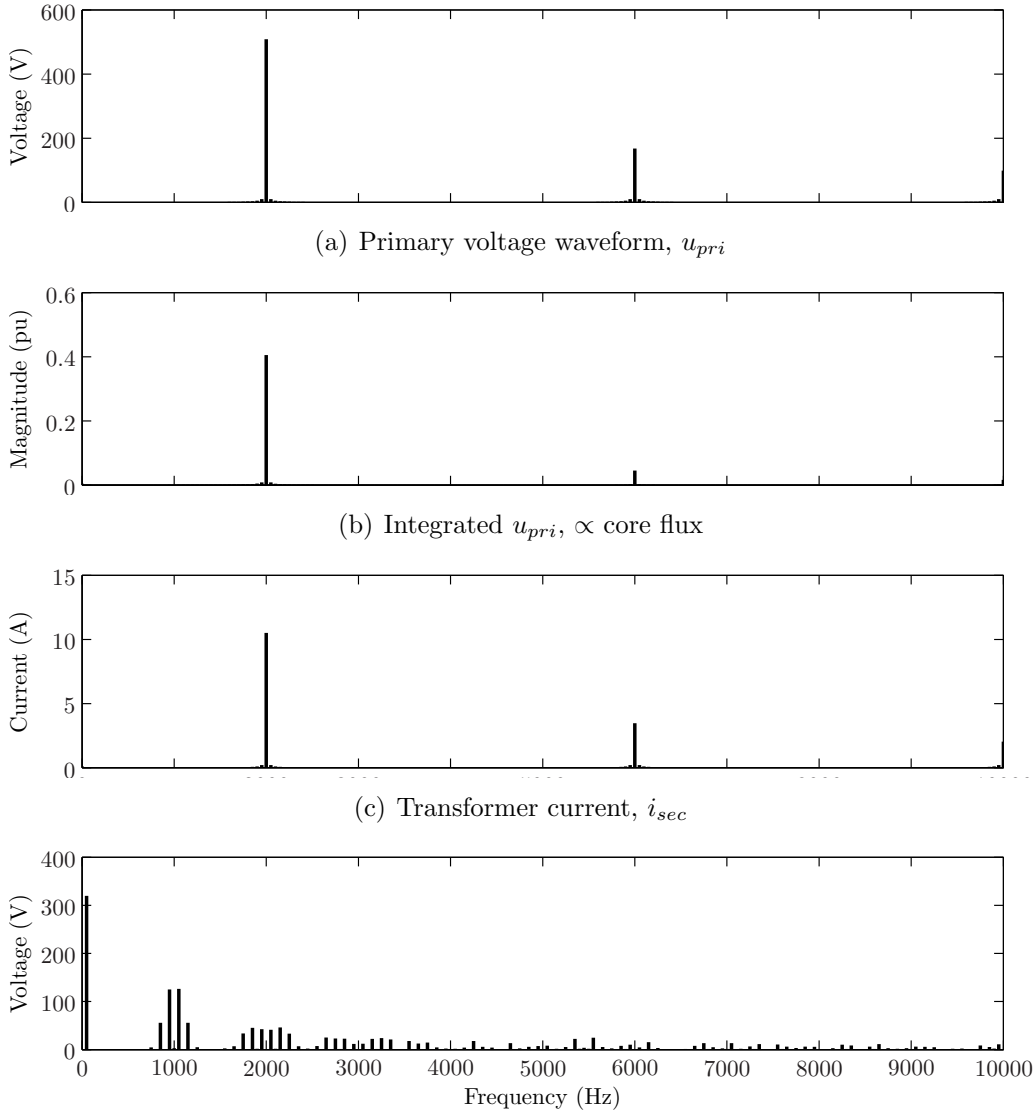


(c) Transformer current, i_{sec}



(d) Converter grid voltage, u_{A0} and voltage demand

Figure 3.23: Triple VSI converter transformer waveforms



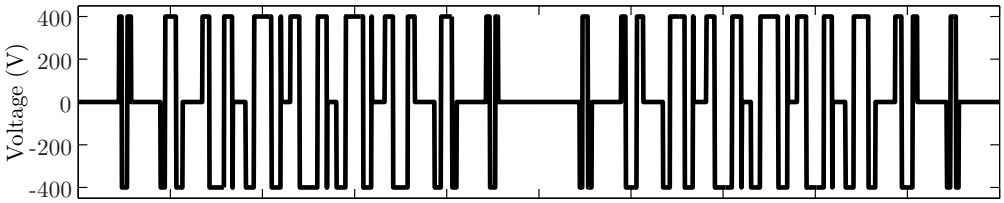
(a) Primary voltage waveform, u_{pri}

(b) Integrated u_{pri}, $\propto$ core flux

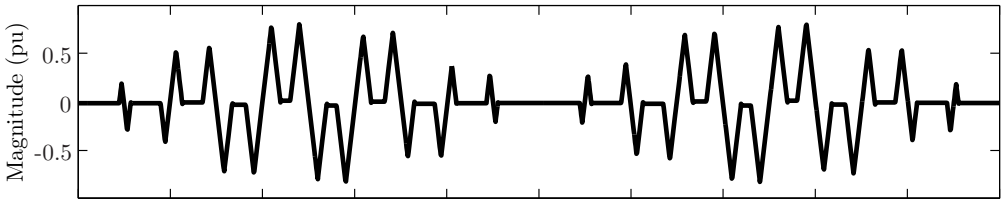
(c) Transformer current, i_{sec}

(d) Converter grid voltage, u_{A0}

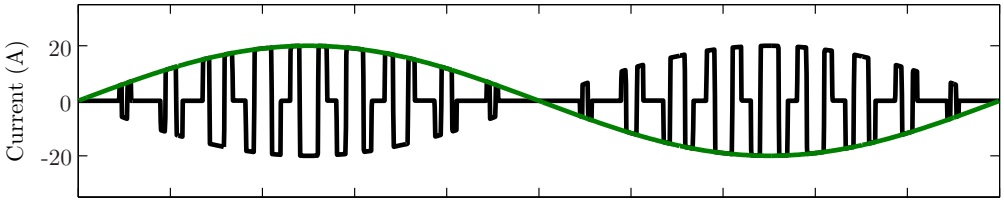
Figure 3.24: FFT of Triple VSI converter transformer waveforms



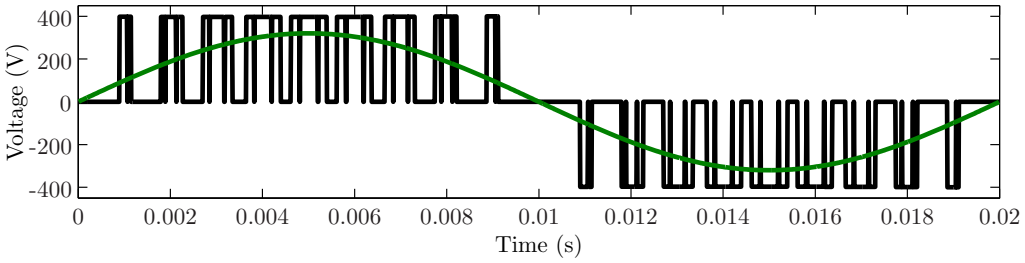
(a) Primary voltage waveform, u_{pri}



(b) Integrated u_{pri}, $\propto$ core flux

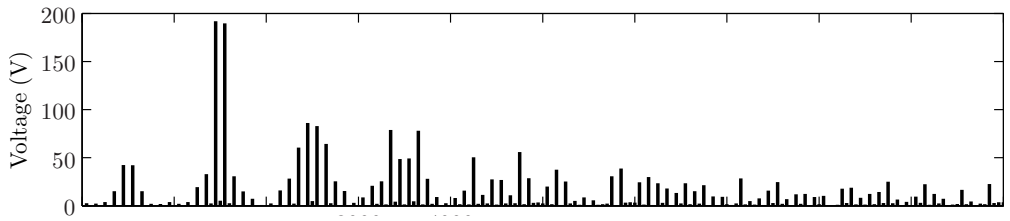


(c) Transformer current, i_{sec} and AC grid current envelope, i_u, i_v or i_w

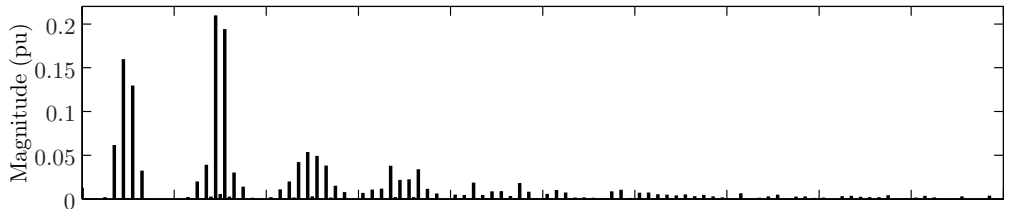


(d) Converter grid voltage, u_{A0} and voltage demand

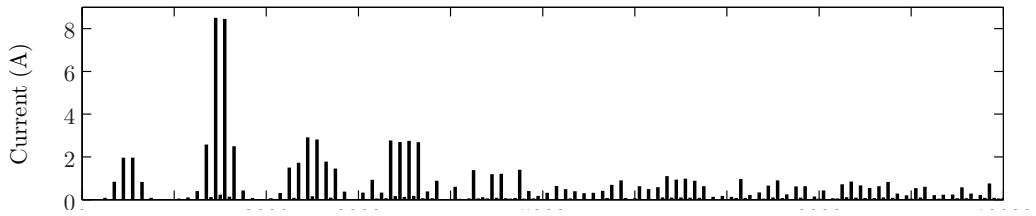
Figure 3.25: Cycloconverter transformer waveforms



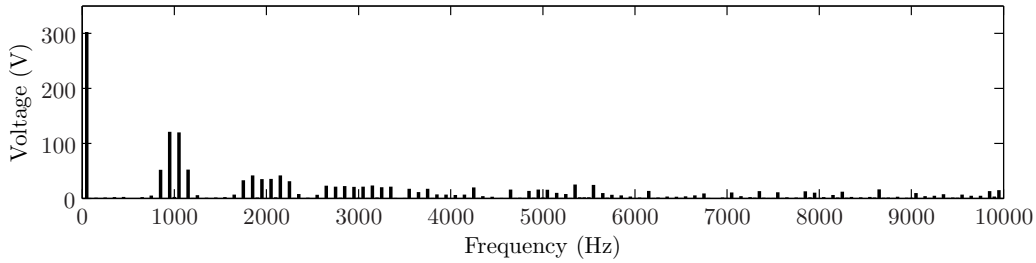
(a) Primary voltage waveform, u_{pri}



(b) Integrated u_{pri}, $\propto$ core flux

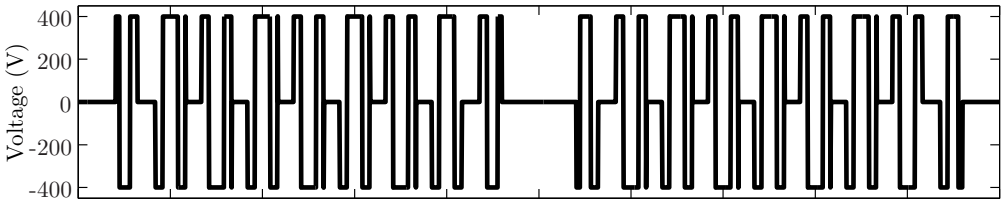


(c) Transformer current, i_{sec}

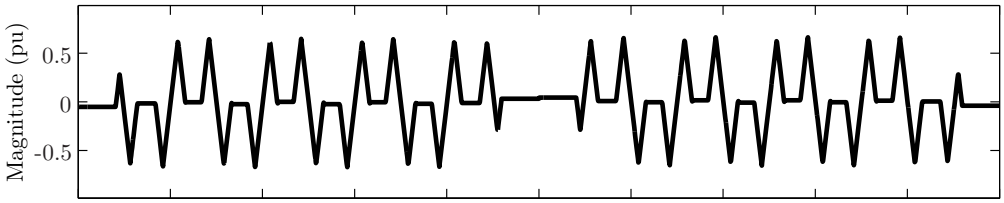


(d) Converter grid voltage, u_{A0}

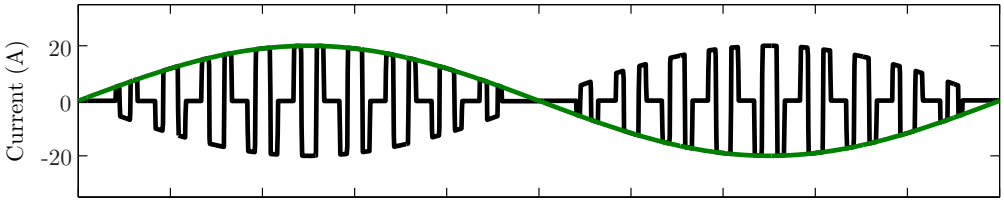
Figure 3.26: FFT of Cycloconverter transformer waveforms



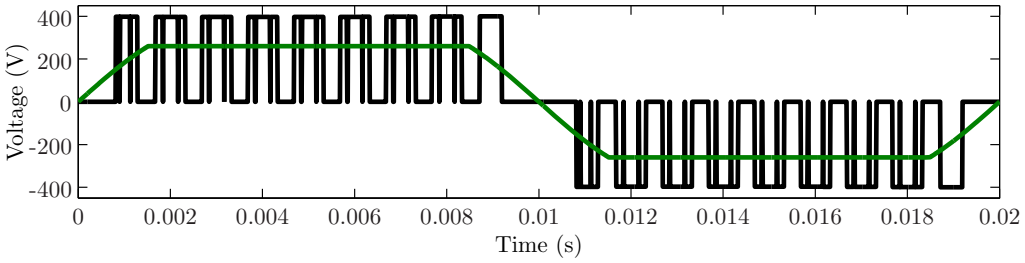
(a) Primary voltage waveform, u_{pri}



(b) Integrated u_{pri}, $\propto$ core flux

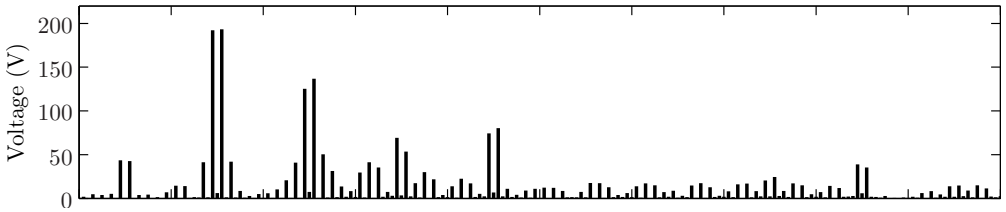


(c) Transformer current, i_{sec} and AC grid current envelope, i_u, i_v or i_w

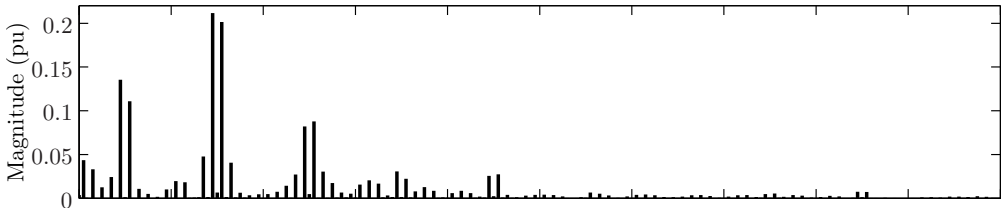


(d) Main Converter voltage, u_{A0} and voltage demand

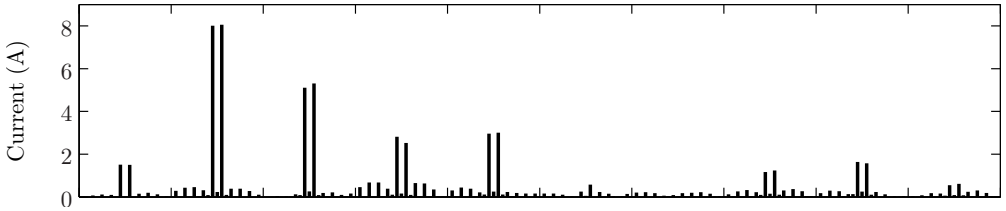
Figure 3.27: Hybrid Cycloconverter transformer waveforms



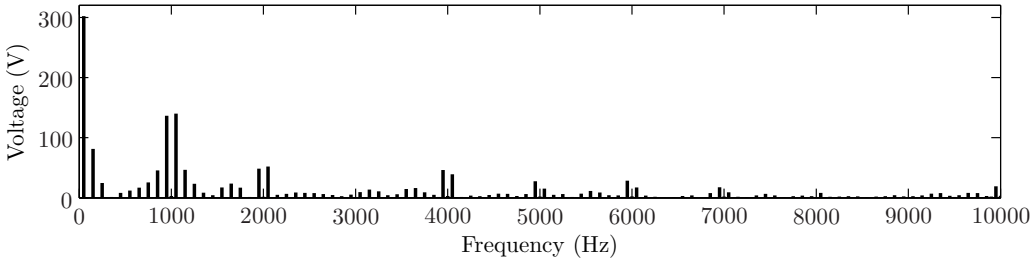
(a) Primary voltage waveform, u_{pri}



(b) Integrated u_{pri}, $\propto$ core flux



(c) Transformer current, i_{sec}



(d) Main Converter voltage, u_{A0}

Figure 3.28: FFT of Hybrid Cycloconverter transformer waveforms

From figures 3.23, 3.25 and 3.27 the RMS values of u_{pri}, i_{sec} and $\int u_{pri}$ and the peak to peak flux are calculated and displayed in pu in Table 3.2. One pu was the requirement of the DAB converter so as to approximately compare the losses in the Cycloconverter and Hybrid Cycloconverter Topologies against the benchmark Triple VSI Topology. The RMS flux was included in the table as it allows for an approximate comparison of the core losses for the modulation schemes, however an accurate estimation of the core losses requires the calculation of core losses for every harmonic in the primary voltage waveform.

The peak to peak flux values were also calculated in order to estimate in pu the minimum core size to prevent saturation for the two converters. The table shows that the Cycloconverter Topology has considerably lower core losses ($0.71pu$) and considerably higher copper losses ($1.42pu$). However the peak to peak flux value will result in the core material having a 52% greater cross sectional area than for the benchmark Triple VSI Topology to prevent saturation.

This will result in very low utilization of the installed power in the core material, greatly adding to the cost and size of the converter. The Hybrid Cycloconverter Topology aims to improve on this by having similar core and copper losses, whilst requiring a peak to peak flux value of $1.3pu$, 17% lower than that of the Cycloconverter Topology.

3.5 Summary

In this chapter, the Hybrid Cycloconverter Topology has been investigated and the operation compared with that of the Cycloconverter and Triple VSI Topologies. The operation of all 3 converters and their switching strategies has been analysed and the importance of the transformer leakage inductance discussed.

The chapter has discussed the effect of injecting triplen harmonics to reduce the peak power from a 3-Phase converter as part of a study into the Hybrid Cycloconverter Topology. This study looked at the peak flux in the transformer core as well as the division of power between the Cycloconverters and auxiliary 3-Phase VSI.

A range of wave shaping techniques to split the AC grid power in the Hybrid Cycloconverter Topology between the auxiliary 3-Phase VSI and the Main Converter was investigated. The resulting harmonic content was analysed in order to establish the most effective shape for a significant reduction in peak power from the Main Converter, whilst only requiring a low power auxiliary 3-Phase VSI.

Switching waveforms from simulation results for the three converter topologies were presented allowing for an analysis of waveform quality and transformer stressing, based on the switching harmonic content of the waveforms.

Chapter 4

Converter Losses for the Cycloconverter Topologies

This chapter investigates the switching and conduction losses of the Cycloconverter topologies for interfacing a DC energy storage device to an AC grid. The previous chapter introduced the commonly produced and researched topologies for this application as well as a novel Hybrid Topology based on the Cycloconverter with an additional auxiliary 3-Phase VSI. This research is focused on the Cycloconverter topologies and utilizes the Triple VSI Topology as a benchmark.

The operation, advantages and disadvantages of the Cycloconverter and Hybrid Cycloconverter topology were discussed in Chapter 3, Section 3.2 and 3.3 respectively as well as for the Triple VSI Topology that is discussed in Section 3.1. The schematic diagrams for The Cycloconverter Topology, Hybrid Cycloconverter Topology and Triple VSI Topology are shown again in this chapter in Figures 4.1, 4.2 and 4.4 respectively. For the Cycloconverter topologies, the loss simulation was carried out at two switching frequencies, to discover if at high frequency the ability of these converters to soft switch would result in lower losses than the benchmark Triple VSI Topology. For The Hybrid Cycloconverter Topology, a Reverse Blocking IGBT (RB IGBT) was also simulated, as it was reasoned that this would reduce the Cycloconverter stage conduction losses by allowing each pair of devices to be placed in parallel rather than series. For the Triple VSI Topology, a lower current device was utilized for VSI 1 and 2 (Figure 4.1), as

these devices only have to process the average power rather than the peak. It was therefore reasoned that the high current devices would be under used even when running at full power, resulting in excessive switching losses.

In order to evaluate the converter losses of the three converter topologies, the circuits were simulated to estimate the switching and conduction losses in the IGBTs and diodes. The simulation was carried out using the PSIM simulation package with the Thermal Module. This chapter will describe the techniques used to simulate the proposed converters, the simulation models used and the circuit parameters. It will then go on to describe and analyse the results and draw conclusions.

This simulation was carried out across a the full range of phase shift between voltage and current and at 25%, 75% and 100% load as this should illistrate the converters opreating with losses dominated by switching, conduction and when the converter switching and conduction losses are of a similar magnitude. Due to the lack of energy storage in the Cycloconverter topologies the losses when processing reactive power will be much greater than the Triple VSI Topology, due to the fact that the first two modules in the Triple VSI Topology, VSI 1 and VSI 2, and the high frequency transformer only have to process the real average power. The Cycloconverter Topology however has to process the peak power with every device as well as the transformer, increasing the losses.

The Hybrid Cycloconverter Topology with the additional auxiliary 3-Phase VSI aims to reduce the peak power processed by the Cycloconverter, thereby reducing the conduction losses and installed power in the converter, making it more competitive with the Triple VSI Topology. However the energy stored in this converter is still far less than for the VSI and therefore will not be able to remove the reactive power load from the transformer and primary VSI. Therefore the results will be more constant across the phase angle for the two Cycloconverter topologies, whereas the Triple VSI Topology will have a large variation of losses with phase shift between current and voltage, with a minimum at 90^{o} and 270^{o}. The Cycloconverter topologies will still have lower losses at 90^{o} and 270^{o}. This is because when the current is at a peak value the duty cycle will be at minimum, allowing the majority of the current to free wheel through the Cycloconverter stage without passing through the transformer and the primary VSI.

4.1 Converter Topologies

4.1.1 Triple VSI Topology (T1)

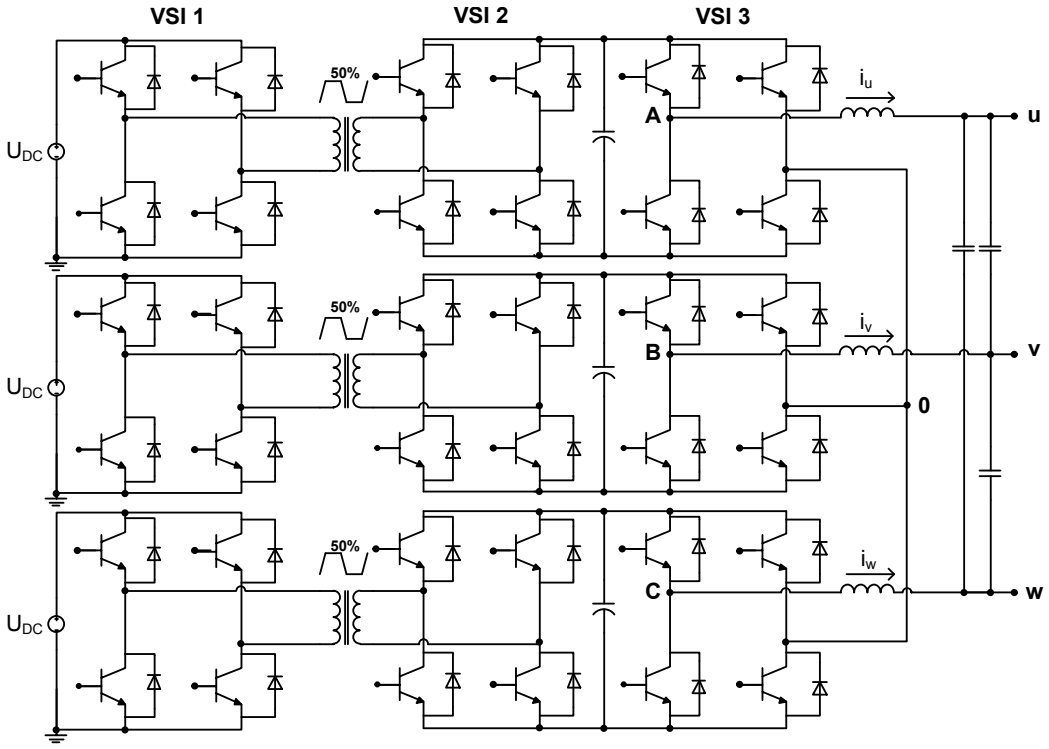


Figure 4.1: Converter topology constructed from three VSIs and a high frequency transformer

Figure 4.1 shows the Triple Voltage Source Inverter (VSI) Topology used as a benchmark for the Cycloconverter study. This converter can be split into two separate stages, VSI 1 and 2 form a DC/DC converter connected to a high frequency transformer to provide isolation, and VSI 3 is used to generate a sinusoidal PWM waveform. VSI 1 and 2 are connected each side of the high frequency transformer and are used to generate a high frequency square wave on the primary and secondary; the phase shift between them used to control the amplitude and direction of power flow. To ensure that the intermediary DC link capacitor remains at a constant voltage, a Proportional Integral (PI) controller can be used to keep the DC link voltages of VSI 1 and 2 constant, or a more advanced control technique involves direct determination of the AC output power from the converter as a feed-forward component into the control system design. This topology schematic diagram is shown again here in Figure 4.1.

4.1.2 Cycloconverter Topology (T2)

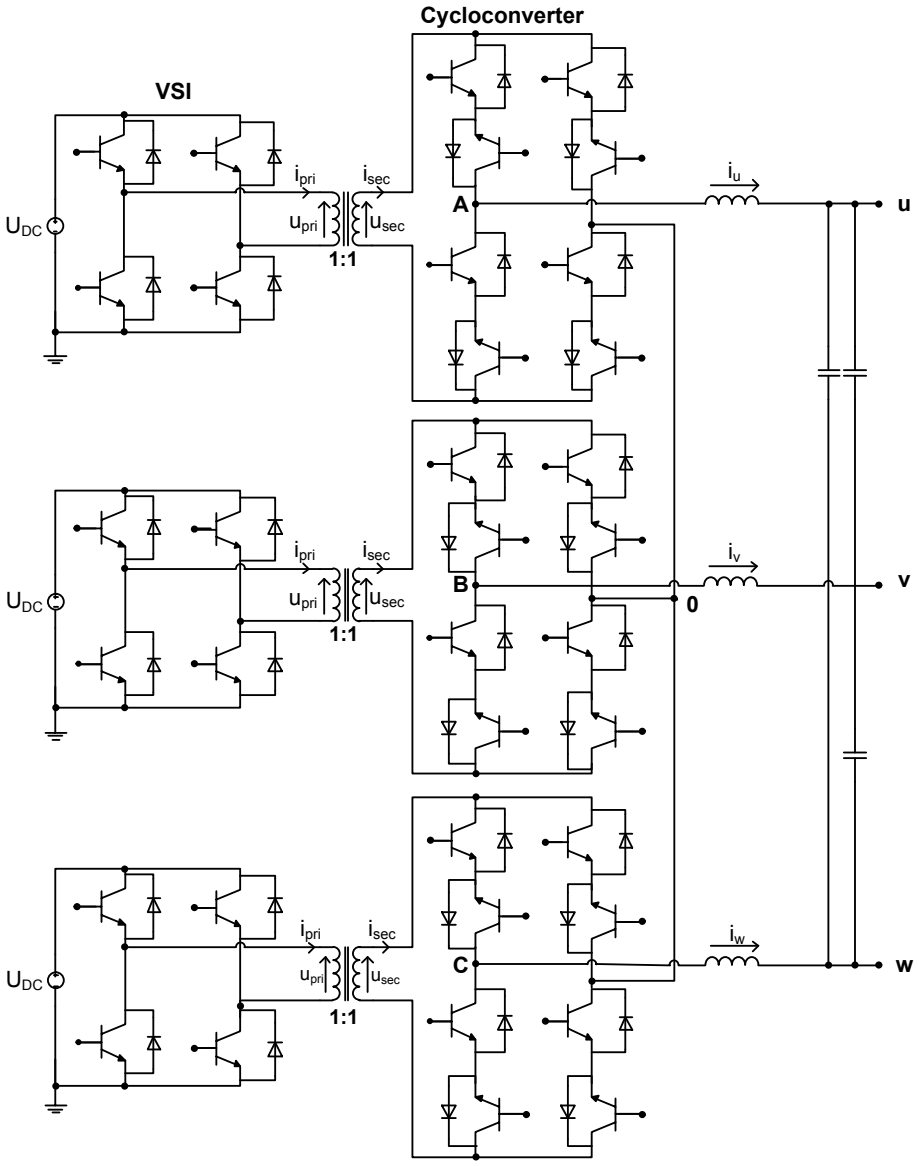
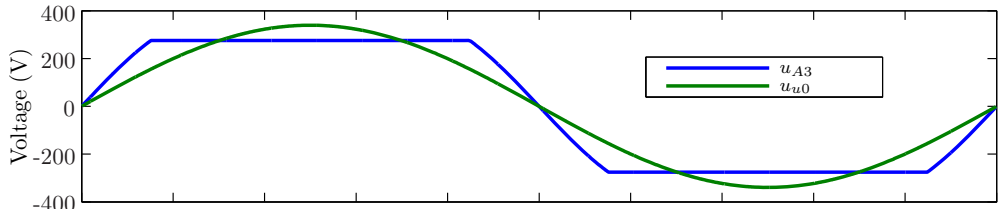


Figure 4.2: Cycloconverter topology constructed from a Voltage Source Inverter connected to an unfolding Cycloconverter via a high frequency transformer

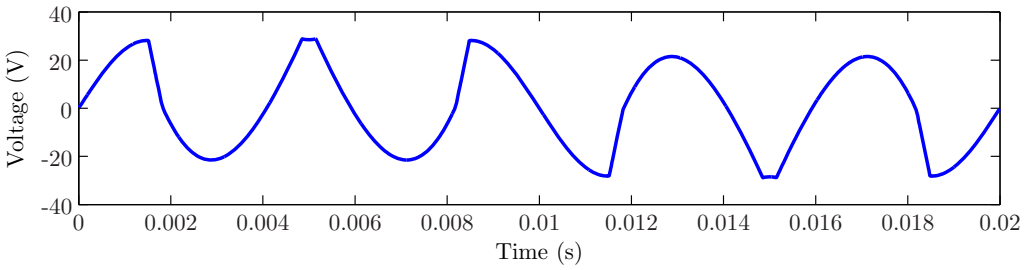
Figure 4.2 shows The Cycloconverter Topology. This converter operates with the primary VSI generating a high frequency 3-level square wave containing the desired PWM output waveform (u_{pri}). The Cycloconverter output stage then unfolds the waveform on the secondary of the transformer (u_{sec}) to reconstruct the low frequency sine wave at the AC terminal of the converter (u_{uvw}). This modulation scheme with associated waveforms has been described in Chapter 3, Section 3.2 and the schematic diagram is shown again here in Figure 4.2. This

technique allows for a high frequency transformer to be used, reducing the size weight and cost of the converter without requiring any additional intermediary energy storage devices compared to a converter that operates with a line frequency transformer, without an unfolding Cycloconverter stage.

4.1.3 Hybrid Cycloconverter Topology (T3)



(a) Main Converter demand voltage, u_{A3}, and total converter demand voltage, u_{u0}



(b) 3-Phase VSI demand voltage, u_{30}

Figure 4.3: Hybrid Cycloconverter topology Cycloconverter and auxiliary 3-Phase VSI reference waveforms

The second Cycloconverter topology utilizes an auxiliary 3-Phase VSI to inject reactive power. For this converter, the primary VSI, Cycloconverter stage and HF transformer will be called the Main Converter. To fully utilize the extra auxiliary 3-Phase VSI, harmonics are injected into the reference waveform of the Main Converter. This allows for a greater output voltage to be generated by the total converter (u_{uvw}) without requiring devices with a higher voltage in the Main Converter. It does however require an additional auxiliary 3-Phase VSI but the installed power in this converter is minimal compared to the installed power in the Main Converter and so will have a minimal effect on the total installed power in the system. This topology is discussed in detail in Chapter 3, Section 3.3 and the schematic diagram is shown again here in Figure 4.4.

The harmonics to be injected into the Cycloconverter waveform, u_{cyc}, have been selected in a previous study and the investigation into waveform shapes is shown in Chapter 3, Section 3.3. The reference waveform for the unfolded Cycloconverter stage is constructed from combining a 50Hz fundamental with a low amplitude third harmonic and then clipping the output voltage waveform. The Cycloconverter waveform shape, u_{A3}, is shown in Figure 4.3 as well as the reference for the additional auxiliary 3-Phase VSI, u_{30}. Clipping the waveform adds odd harmonics and due to the fact that the triplen harmonics will be cancelled, the additional injected third harmonic reduces the peak voltage yet further without increasing the amplitude from the required additional converter.

4.2 Loss Estimation Technique

The conduction losses from a converter can be easily estimated by multiplying the device current by the on state forward voltage drop. This forward voltage drop can be obtained from the device datasheet, can be experimentally measured or calculated from the semiconductor physics. For this simulation, the information from the device datasheet was utilized to estimate the forward voltage for a given current level.

Switching losses during a switching transition can be calculated using a wide range of techniques. One can use the energy loss figure during a switching transition from the device datasheet and scale the value accordingly. Alternatively one can use a physics based model to multiply the instantaneous voltage across a device with the current through the device.

M. Bland introduces a way of approximating the losses associated with a converter by simplifying the switching of a device into approximations made from geometric shapes [61]. He then goes on to experimentally justify his results. In comparison the Saber simulation package is used to simulate the instantaneous voltage and current across the device to calculate the instantaneous power loss [62]. This model includes thermal feedback to take into account the varying performance at different temperature ranges, so the losses will vary as the device heats up. This allows for a more accurate simulation of a final converter to generate a

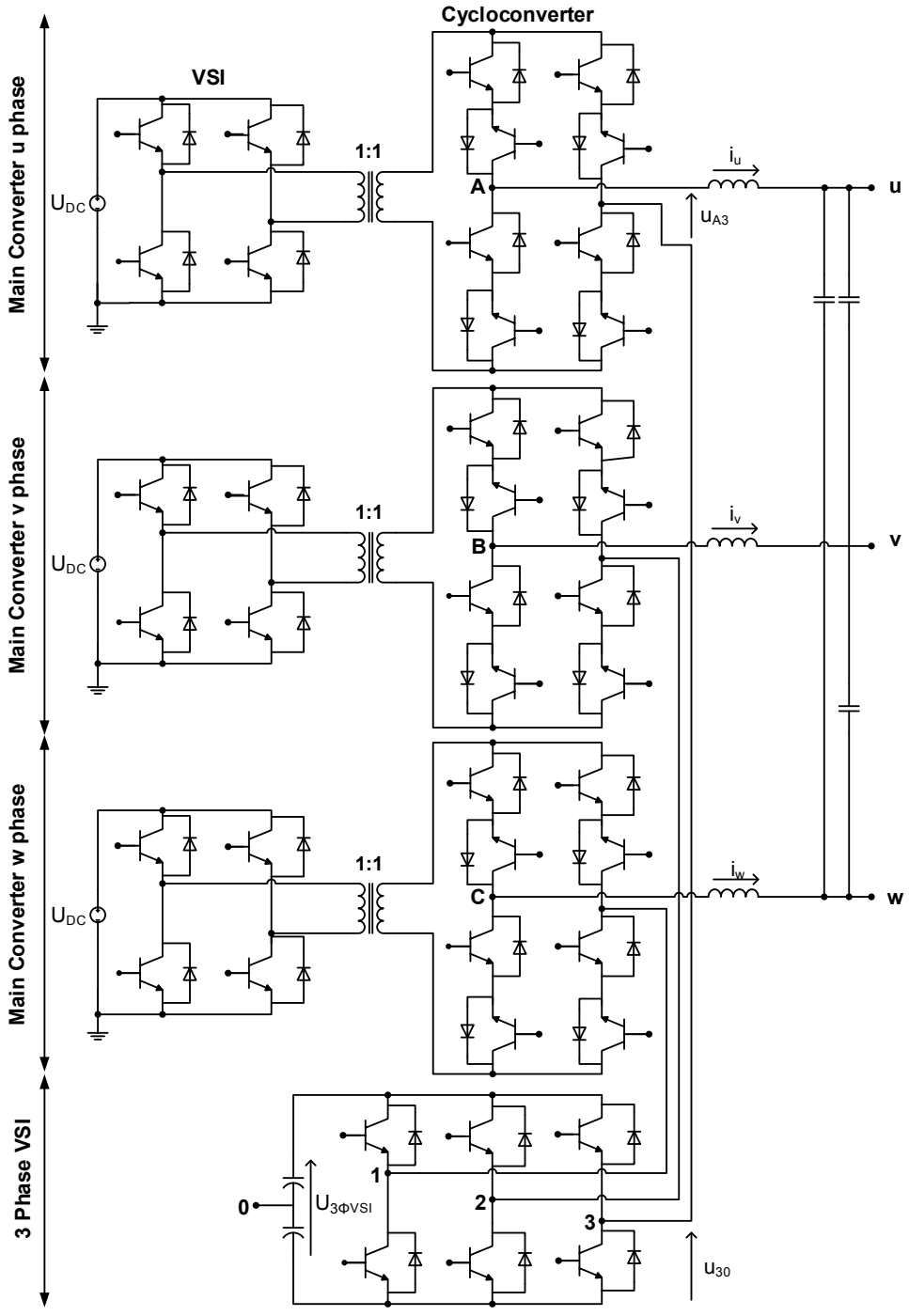


Figure 4.4: Hybrid Cycloconverter topology constructed from a Voltage Source Inverter connected to an unfolding Cycloconverter, via a high frequency transformer with an auxiliary 3-Phase VSI

temperature profile that can be used to estimate the lifetime of the converter with a particular heat-sink, ambient temperature and load profile. This requires a much higher resolution of simulation so does not allow for the rapid comparison of different converters, but theoretically will provide a more accurate result and will allow for a greater prediction of device stress than can even be measured from an experimental converter. However this technique requires a very high precision model for these results to be valid which is not obtainable without experimental measurement or specific information regarding the surface area of each region of the semiconductor. As such this technique is not suitable for this simulation and instead the PSIM Thermal Module was used.

The PSIM Thermal Module utilizes an ideal switching transition and estimates the switching energy loss from graphs obtained in the component datasheet. The value for this energy loss is then scaled accordingly for the current and voltage that the device is being switched at. No thermal feedback is included in this model, however the energy lost from the switching device can be used to estimate temperature based on a specific thermal environment. This model has the advantage that the circuit is simulated quickly, allowing for a wide range of parameters to be varied, and that it is based on experimental data from the component datasheet. No experimental investigation into device performance is required and therefore this technique is suitable for the initial comparison of topologies.

4.2.1 Circuit Parameters

The losses were calculated at 5 power levels and at 16 different power factor angles from 1 to -1 (0 to 360^o phase shift between current and voltage). The IGBTs selected were the Infineon FS35R12W1T4 and the FS25R12W1T4 for the lower current devices for the VSI 1 and 2 of Figure 4.1. The initial comparison was carried out with a 5kHz switching frequency, however to investigate how the losses varied with frequency the simulation was repeated at 10kHz. The additional auxiliary 3-Phase VSI for The Hybrid Cycloconverter Topology used the IRF4228PbF Metal Oxide Semiconductor Field Effect Transistor (MOSFET) for the simulation. A MOSFET was able to be used due to the reduced DC link of this converter. The Hybrid Cycloconverter Topology was also simulated using a reverse blocking IGBT, IXRH 40N120, for the Cycloconverter stage. This was to

try to reduce the conduction losses in this converter so that the switching devices could be placed in series rather than parallel. The parameters of the simulation are shown in table 4.1 and the device parameters are shown in Section A.2 of Appendix A. The selection of a 70µH leakage inductance for the Triple VSI Topology discussed in Chapter 3, Section 3.1. For the Cycloconverter and Hybrid Cycloconverter topologies, the converter was simulated with a leakage inductance of 35µH as this was seen as the minimum value possible for a transformer of an appropriate size.

	T1 LP	T1 HP	T2	T3	T3 RB
Leakage inductance	70µH		35µH		
Magnetizing inductance	10mH				
Low power	3.9kW			4.8kW	
Medium power	11.7kW			14.4kW	
High power	15.6kW			19.2kW	

Table 4.1: Circuit parameters

4.2.2 Simulated Devices

FS35R12W1T4 IGBT

The FS35R12W1T4 was used as main switching device in the converters. It is a 1200V device with a maximum current rating, $I_{c(max)}$, of 70A and an average current rating, $I_{c(nom)}$, of 35A.

FS25R12W1T4 IGBT

A second IGBT was simulated in order to evaluate the affect of utilizing smaller devices in VSI 1 and 2 of the Triple VSI Topology (Figure 4.1). It is also a 1200V device but has a reduced $I_{c(max)}$ of 50A and an $I_{c(nom)}$ of 25A.

IRF4228PbF MOSFET

In order to minimize the switching and conduction losses of the additional auxiliary 3-Phase VSI in The Hybrid Cycloconverter Topology, the circuit was simulated with a high current, low voltage MOSFET as a switching device. The MOSFET is rated with a maximum voltage V_{DS} of 150V and a maximum repetitive peak current I_{RP} of 170A. A higher voltage MOSFET would significantly increase the conduction and switching losses so it is important to select the lowest voltage device possible, with an appropriate voltage headroom to allow for voltage overshoots from switching.

IXRH 40N120 Reverse Blocking IGBT (RBIGBT)

To reduce the conduction losses in the Cycloconverter stage of The Hybrid Cycloconverter Topology, a RB IGBT was used. This device has a lower forward drop than a diode and IGBT in series and the conduction losses should be significantly reduced. It does however have considerably larger reverse recovery charge, Q_{rr}, and gate capacitance. The RB IGBT used is a 1200V device with an $I_{c(25)}$ of 55A.

4.2.3 PSIM Thermal Module Loss Calculation

PSIM simulates the switching of power semiconductor devices in a functional way and does not calculate any switching transients. The Thermal Module continues to use this simulation technique and estimates the switching losses based on a measurement of the voltage across and current through the device before and after the switching transition. It then uses this information to look up the value of the switching energy loss from the component datasheet. In order to turn this value into a power loss, the energy loss is summed over one 50Hz time period, T, and multiplied by the inverse of this time period.

The conduction losses are estimated using the datasheet to look up the forward voltage drop across the device for a particular current. This forward voltage drop

is then used in the simulation at the next time step. The results of the calculated losses, especially the switching losses, are only approximation and many factors are not taken into account.

Diode Losses

The integrated diode conduction losses are calculated as follows, where T is the time period of one 50Hz cycle:

$$P_{cond} = \frac{1}{T}\int_0^T [V_f(t) \cdot I_f(t)]dt \tag{4.1}$$

The diode turn-on losses are neglected and are not considered.

If the current being turned off at the switching instant is I_{fi} and the off voltage is V_{cei}, then the energy lost at the turn off transition is $E_{rr}(I_{fi})$, where the E_{rr} function for a nominal voltage V_{ce_nom} is shown in Appendix A, Section A.2. The total power lost in one cycle is therefore, where T is the time period of one 50Hz cycle:

$$P_{off} = \frac{1}{T}\sum_0^T \frac{f_{sw} \cdot E_{rr}(I_{fi}) \cdot V_{cei}}{V_{ce\_nom}} \tag{4.2}$$

Alternatively if E_{rr} is not given, but Q_{rr} is, then the turn off losses can be calculated as, where T is the time period of one 50Hz cycle:

$$P_{off} = \frac{1}{T}\sum_0^T \frac{f_{sw} \cdot Q_{rr}(I_{fi})}{4} \tag{4.3}$$

If only the peak reverse recovery current and reverse recovery time (I_{rr} and t_{rr}) are given, then the turn off losses can be calculated as, where T is the time period of one 50Hz cycle:

$$P_{off} = \frac{1}{T}\sum_{0}^{T}\frac{f_{sw}\cdot t_{rr}(I_{fi})\cdot I_{rr}(I_{fi})}{8} \tag{4.4}$$

IGBT Losses

The IGBT conduction losses are calculated as follows, where T is the time period of one 50Hz cycle:

$$P_{cond} = \frac{1}{T}\int_{0}^{T}[V_{ce\_sat}(t)\cdot I_{ci}(t)]dt \tag{4.5}$$

If the current being turned off at the switching instant is I_{ci} and the off voltage is V_{cei}, then the energy lost at the turn off transition is $E_{on}(I_{fi})$, where the E_{on} function for a nominal voltage V_{ce_nom} is shown in Appendix A, Section A.2. The total power lost during turn off in one cycle is therefore, where T is the time period of one 50Hz cycle:

$$P_{on} = \frac{1}{T}\sum_{0}^{T}\frac{f_{sw}\cdot E_{on}(I_{ci})\cdot V_{cei}}{V_{ce\_nom}} \tag{4.6}$$

If the current being turned off at the switching instant is I_{ci} and the off voltage is V_{cei}, then the energy lost at the transition is $E_{off}(I_{fi})$, where the E_{off} function for a nominal voltage V_{ce_nom} is shown in Appendix A, Section A.2. The total power lost during turn on in one cycle is therefore:

$$P_{off} = \frac{1}{T}\sum_{0}^{T}\frac{f_{sw}\cdot E_{off}(I_{ci})\cdot V_{cei}}{V_{ce\_nom}} \tag{4.7}$$

Where E_{off} is the transistor turn-off energy losses and T is the time period of one 50Hz cycle.

MOSFET Losses

The MOSFET conduction losses are calculated as follows, where T is the time period of one 50Hz cycle:

$$P_{cond} = \frac{1}{T}\int_0^T [{I_{drain}}^2(t) \cdot R_{DS(on)}(t)]dt \tag{4.8}$$

If the current being turned on at the switching instant is I_{ci} then the energy lost at the transition is $E_{on}(I_{fi})$, where E_{on} is calculated based on the information of the gate current, input, output and reverse transfer capacitances and the gate charge of the MOSFET. These values are shown in Appendix A, Section A.2. The total power lost during turn on in one cycle is therefore, where T is the time period of one 50Hz cycle:

$$P_{on} = \frac{1}{T}\sum_0^T f_{sw} \cdot E_{on}(I_{ci}) \tag{4.9}$$

If the current being turned off at the switching instant is I_{ci} then the energy lost at the transition is $E_{off}(I_{fi})$, where E_{off} is calculated based on the information of the gate current, input, output and reverse transfer capacitances and the gate charge of the MOSFET. These values are shown in Appendix A, Section A.2. The total power lost during turn off in one cycle is therefore, where T is the time period of one 50Hz cycle:

$$P_{off} = \frac{1}{T}\sum f_{sw} \cdot E_{off}(I_{ci}) \tag{4.10}$$

4.3 Simulation Results

4.3.1 General Remarks

Figure 4.5 shows the total conduction and switching losses for the three topologies, as a function of the phase angle between current and voltage. The power loss results are given as a percentage of the total AC output power from the converter.

The switching losses are dependent on the DC link voltage of the converter and an increase in current has less of an effect than for conduction losses. The switching losses for a MOSFET are indpendant of current, whereas for a IGBT the turn on energy increases non-linearly with current and the IGBT turn off losses increase linearly with current. However the majority of losses however are due to the the diode reverse recovery losses which plateau at high current levels.

The conduction losses of a switching devices increase non-lineary with with current due to the on state resistance and the resulting square law power loss, I^2R. There is an additional linear component of losses with respect to current, relating to the on state voltage drop across the semiconductor PN junction, $V_{pn}I$ and these two elements are combined to to give the total semiconductor conudction losses. As MOSFETs do not contanin a PN junction, when the device is on it is purely resistive and the conduction losses only contain the I^2R component.

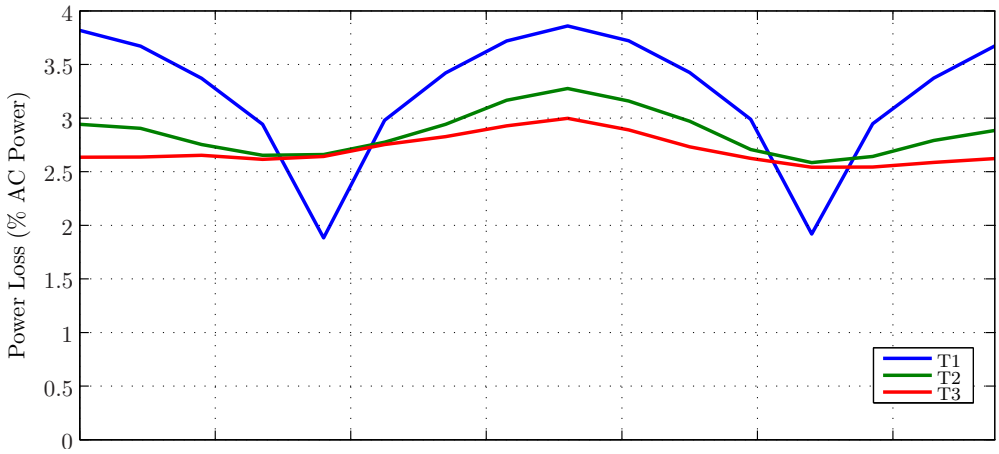
From Figure 4.5 it can be seen that at low power levels the Cycloconverter topologies have lower losses than the Triple VSI Topology for most of the phase angle range, whereas at higher powers the VSI has lower losses. This is due to the fact that the Cycloconverter stage in the Cycloconverter has very low switching losses but high conduction losses, due to the fact that there is always 2 IGBTs and 2 diodes in the conduction path. The VSI however only has 2 IGBTs or 2 diodes in the conduction path but operates with hard switching for some of the switching transients. Because the switching losses do not vary much with current, at low powers the hard switched VSI topology will have greater losses. At high powers the increased conduction losses will cause the Cycloconverter topologies to have greater losses.

As the phase angle between the voltage and current increases, the quantity of real power produced by the converters will reduce until it reaches 0 at 90°. At this point VSI 1 and 2 and the high frequency transformer in the Triple VSI Topology will no longer be processing any power, as all of the reactive power will be provided by the DC link capacitor connected to VSI 1 and 2. The Cycloconverter topologies will continue to process the reactive power throughout the converter as this topology contains no additional energy storage devices. There will continue to be some variation in power loss with phase angle due to the fact that the duty cycle of the Cycloconverter is at a minimum during the current peak, when the phase shift is 90°, and the output current will be free-wheeling through the Cycloconverter stage more of the time. The Hybrid Cycloconverter Topology has a lower variation in power loss due to the increased utilization of this converter across the whole of the cycle and therefore there will be less time for the voltage to be at a minimum during the peaks in current.

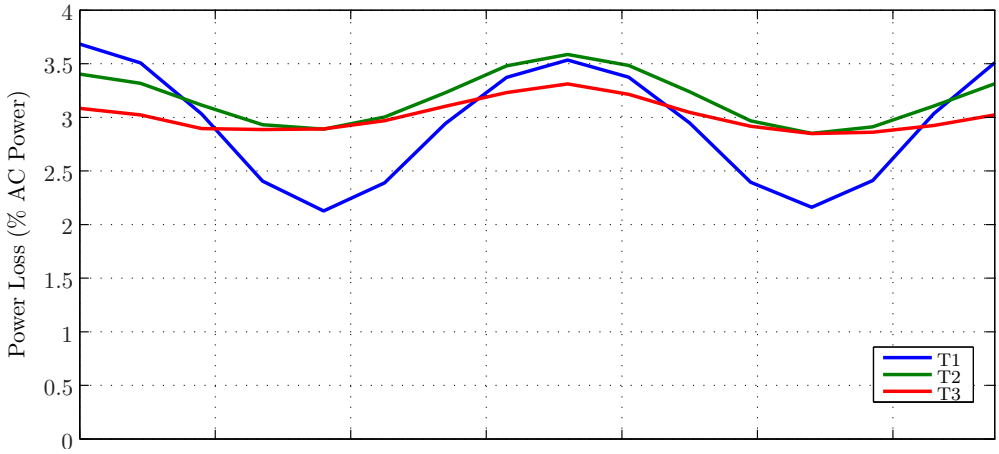
4.3.2 Analysis of the Benchmark VSI Converter Losses (T1)

Figure 4.6 shows the converter losses when operating at low, medium and high power respectively. The output section, VSI 3, has almost constant losses with phase angle, with the IGBTs producing the majority of the losses when in phase and the diode conduction losses producing the majority of the conduction losses when 180° out of phase. This is because when this converter operates with the current in phase with the voltage, the IGBTs conduct the current and when they are out of phase the diodes conduct. The switching losses in the diodes and IGBTs remain constant across the whole range of power factor angles. As the power output is increased from the converter, the percentage conduction losses increase significantly and the percentage switching losses are reduced. This is because the conduction losses have a square law relationship with current and the switching losses do not.

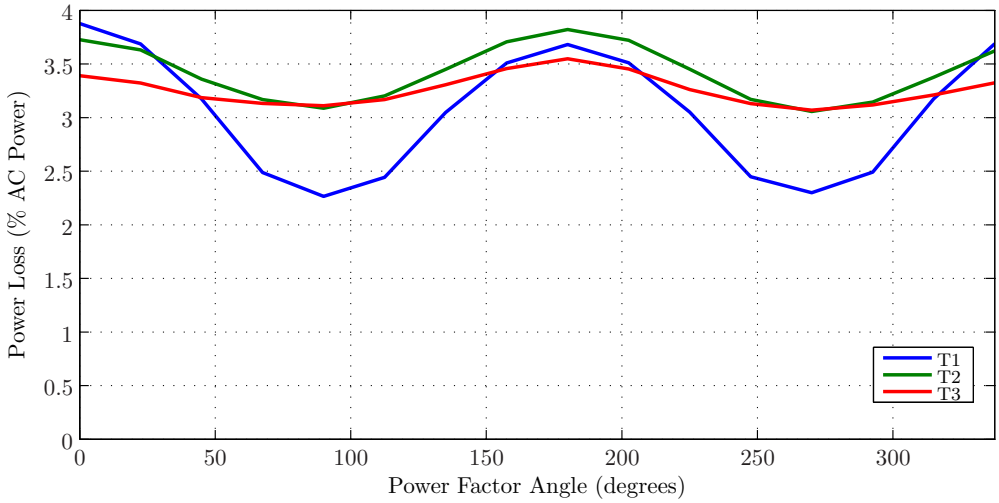
As previously explained VSI 1 and 2 have a large variation in conduction losses with phase angle, due to the fact that these sections of the converter only process real power. The switching losses for these VSIs should be constant and it is unknown why at 90° they almost drop to zero. This may be due to a simula-



(a) 25% load



(b) 75% load



(c) 100% load

Figure 4.5: Results from losses simulation from 3 converters at 25%, 75% and 100% load. T1: Triple VSI Topology, T2: Cycloconverter Topology, T3: Hybrid Cycloconverter Topology with auxiliary 3-Phase VSI

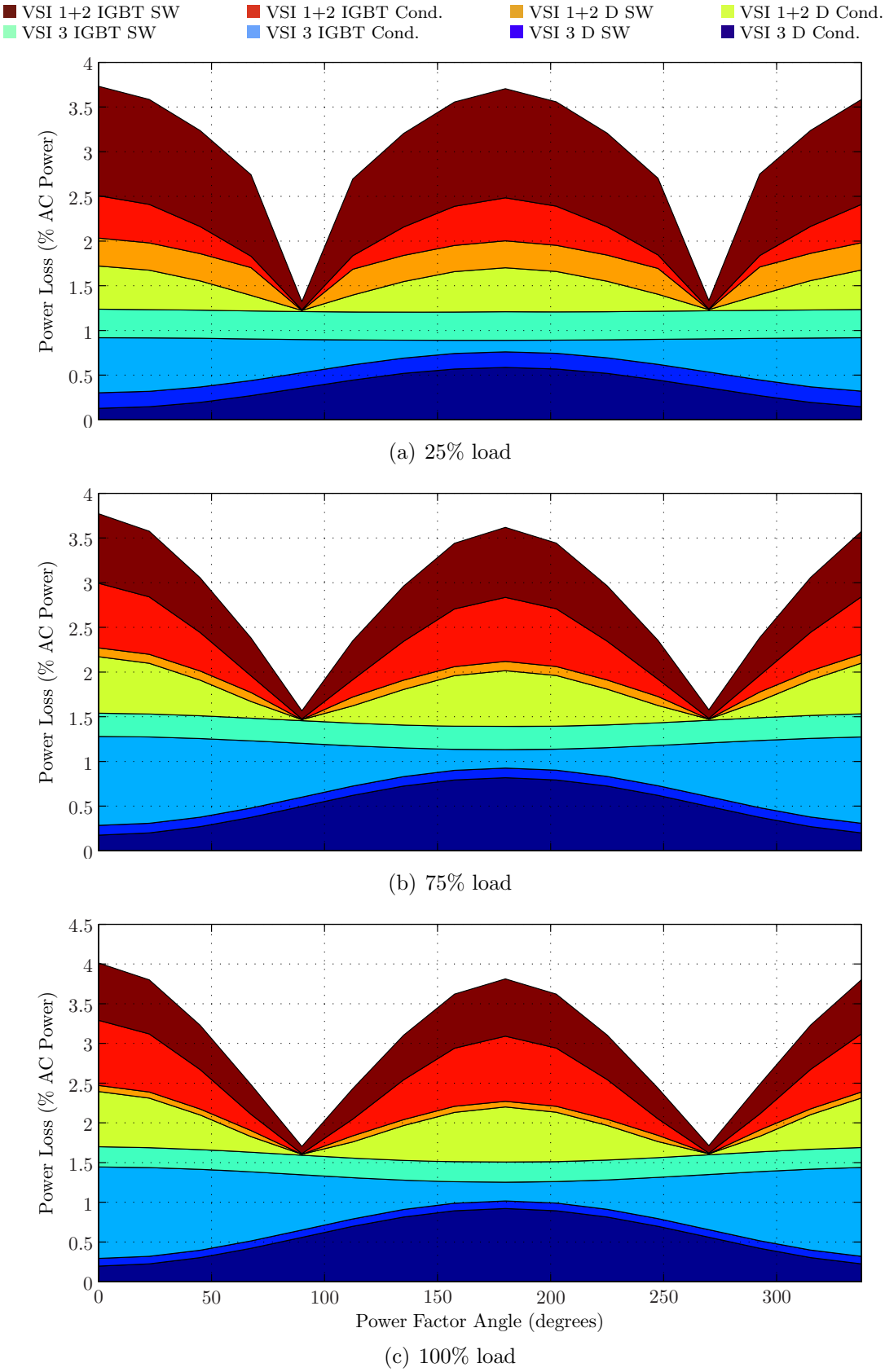
tion error when operating the converter with zero real power. When the whole converter operates at low power, in Figure 4.6(a), the switching losses from these two sections of the converter contribute significantly to the total losses in the converter and in this situation it would be sensible to use a lower current rated device instead.

The simulation is repeated for the Triple VSI Topology using 25A IGBTs for VSI 1 and 2. This is possible because of the reduced current required to be processed by these devices as the capacitors in this topology allow these devices to only process the average power and not the peak. Using devices that are overrated increases the switching losses unnecessarily, causing excessive losses at low power levels, as shown in Figure 4.6(a).

Figure 4.7 shows the VSI converter losses when operating at low, medium and high power respectively with both the 25A and 35A devices. Figure 4.7(a) shows that at low power the 25A device has considerably lower losses (e.g. 0.1% to 0.4%) across the whole of the power range. At higher powers this effect is reversed when the current and voltage are in phase. However when the phase shift approaches 90°, the 25A device continues to have lower losses due to the minimal power processed by VSI 1 and 2. Overall the performance of the 25A device is better or equal to that of the 35A device over the majority of the operating range.

4.3.3 Analysis of Cycloconverter Topology Losses (T2)

The breakdown of The Cycloconverter Topology losses are shown in Figure 4.8. It can be seen that the conduction losses in the Cycloconverter stage from the IGBTs and diodes remain constant regardless of the phase shift between voltage and current. This is due to the fact that the load current always passes through two IGBTs and two diodes at the same time, whatever the phase shift between current and voltage waveform. The fact that this topology continuously has the load current flowing through two diodes and two IGBTs in the Cycloconverter stage results in a converter with considerably larger conduction losses than Triple VSI Topology. However The Cycloconverter Topology is able to operate with reduced switching losses.

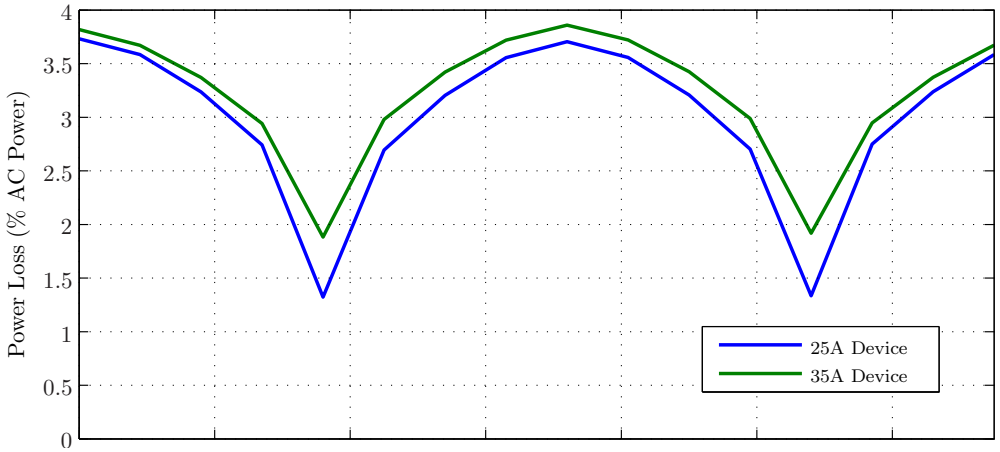


(a) 25% load

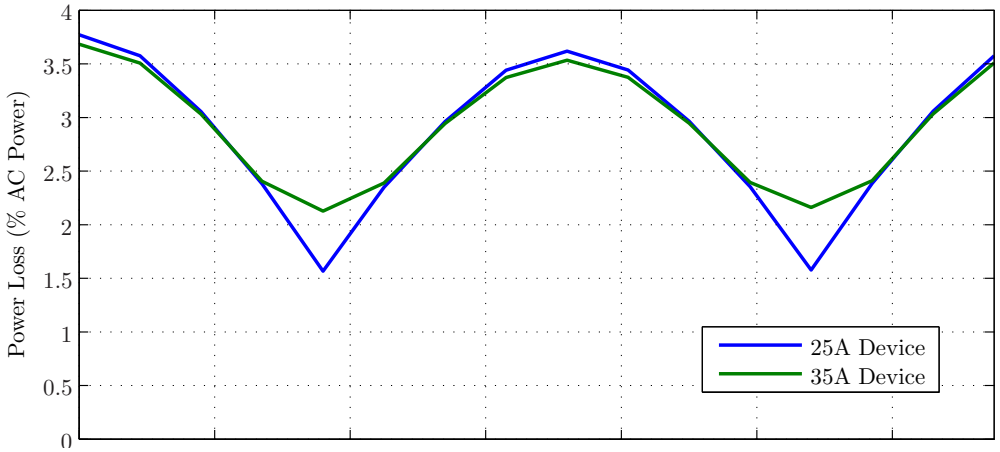
(b) 75% load

(c) 100% load

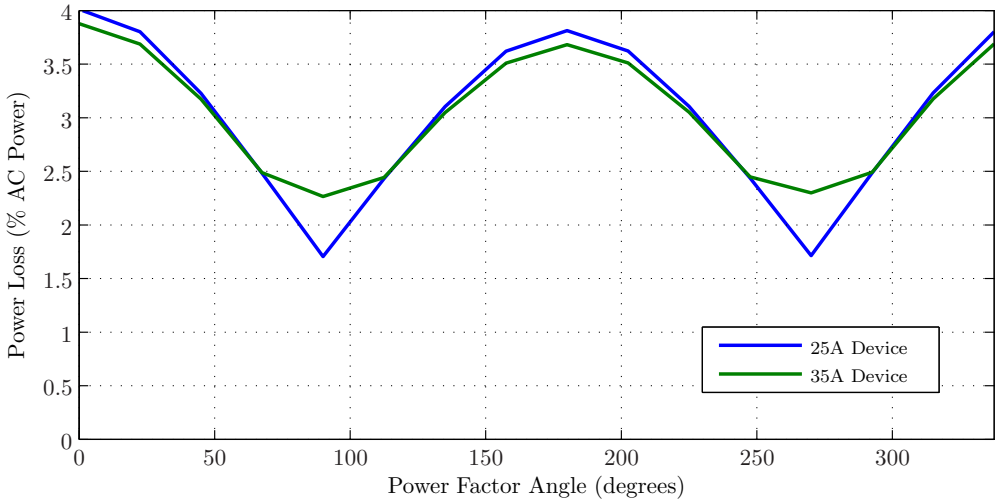
Figure 4.6: Breakdown of losses from Triple VSI Topology at 25%, 75% and 100% load



(a) 25% load

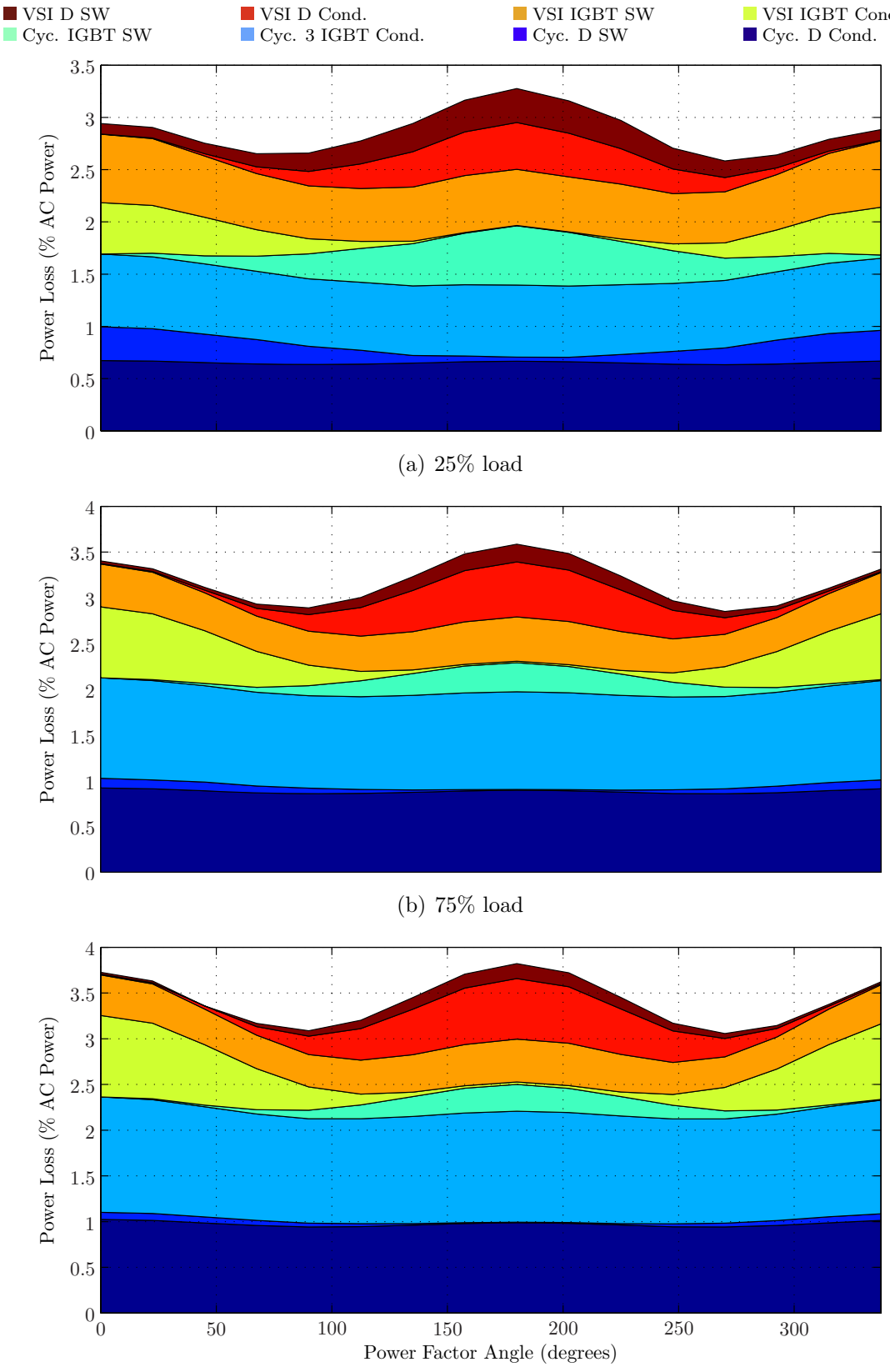


(b) 75% load



(c) 100% load

Figure 4.7: Comparison of losses with two different devices (25A and 35A) are used in VSI 1 and 2 in the VSI Converter Topology operating at 25%, 75% and 100% load



(a) 25% load

(b) 75% load

(c) 100% load

Figure 4.8: Breakdown of losses from Cycloconverter Topology at 25%, 75% and 100% load

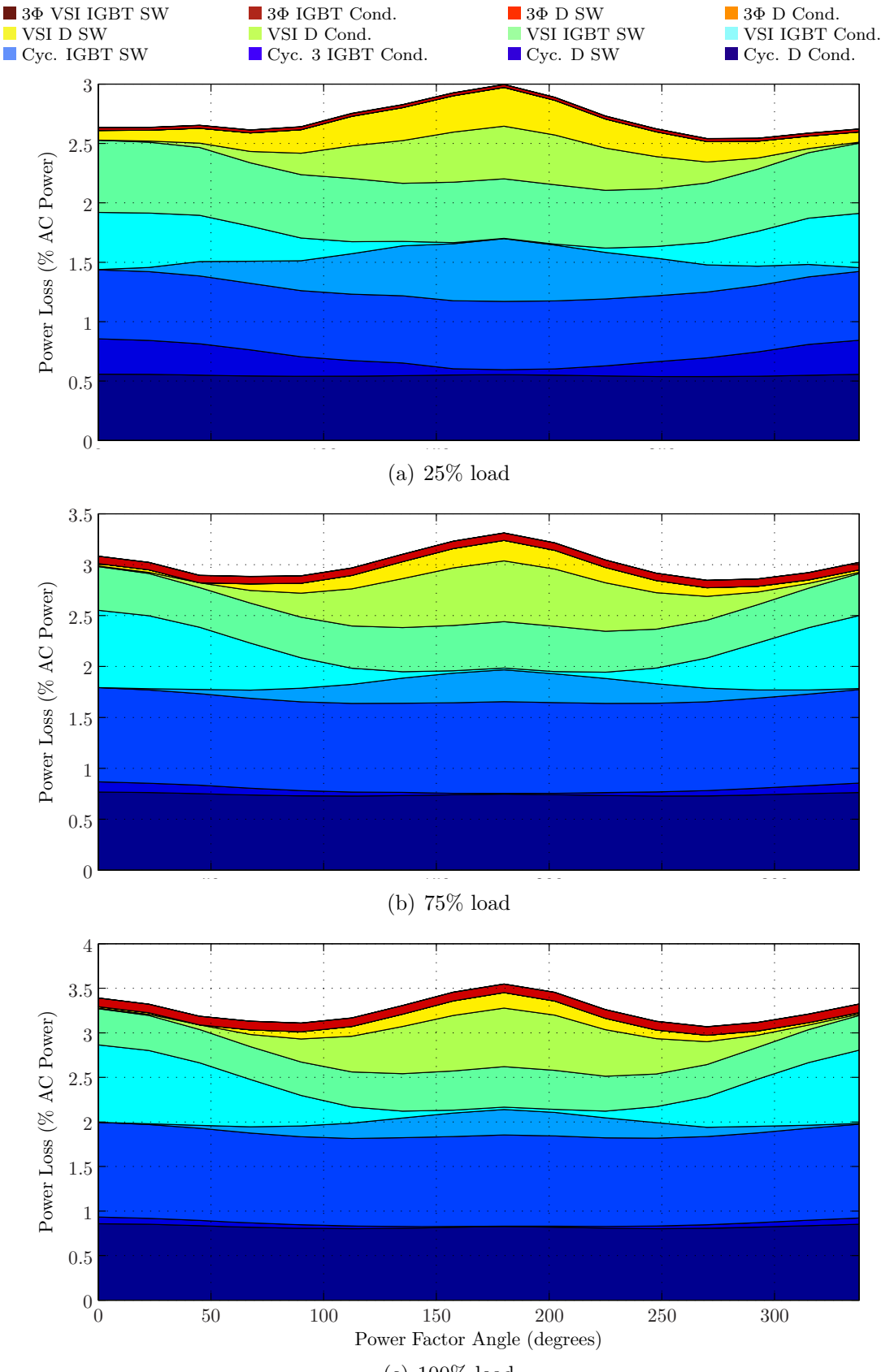
The switching losses in the Cycloconverter increase with phase shift. This is due to the fact that when the current and voltage are in the same direction, the Cycloconverter stage only acts as a rectifier and the diodes are the devices that switch. When the current and voltage are in different directions, the Cycloconverter stage has to switch at the same rate as the VSI on the primary side of the HF transformer.

The primary VSI switching losses for both IGBT and diode are constant across the full range of phase angles as each switching device still switches the same number of times each cycle. The primary IGBT and diode losses sum to a constant value; when the current is in phase with the voltage all of the losses are in the IGBTs and when the current is out of phase all of the conduction losses are in the diodes. This is because when the converter is transferring power from the DC network to the AC network the IGBTs will conduct the current and when the converter is transferring power from the AC network to the DC network the diodes will conduct and the IGBT and diode conduction losses are approximately equal for a given current.

In order to discover the effect on losses that doubling the switching has on the converter, the simulation was repeated with a switching frequency of 10kHz. Figure 4.8 shows that the higher frequency converter has considerably higher losses, approximately 1%, at all power levels. This increase in losses from twice the switching frequency may be compensated by a reduction in the transformer size, so it might be the case that for specific applications where size and weight are a premium, such as aerospace, switching at high frequency is more suitable. The switching losses in every switching device in the converter have doubled which is the predicted result based on the simulation model used.

4.3.4 Analysis of Hybrid Cycloconverter with Auxiliary 3-Phase VSI (T3)

Figure 4.9 shows the breakdown of losses from The Hybrid Cycloconverter Topology. The Hybrid Cycloconverter Topology is able to produce an output voltage waveform 23% greater than the other two converters whilst using the same devices for the VSI and Cycloconverter stage. This increased power output results

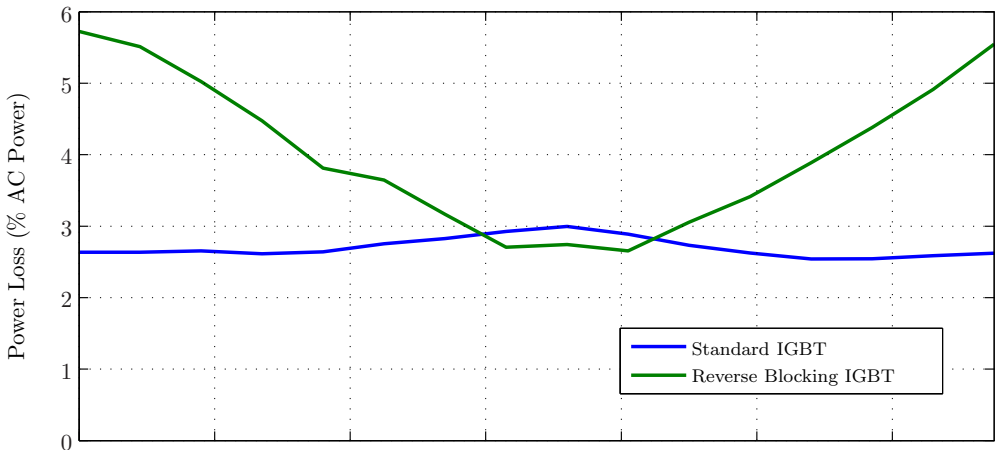


(a) 25% load

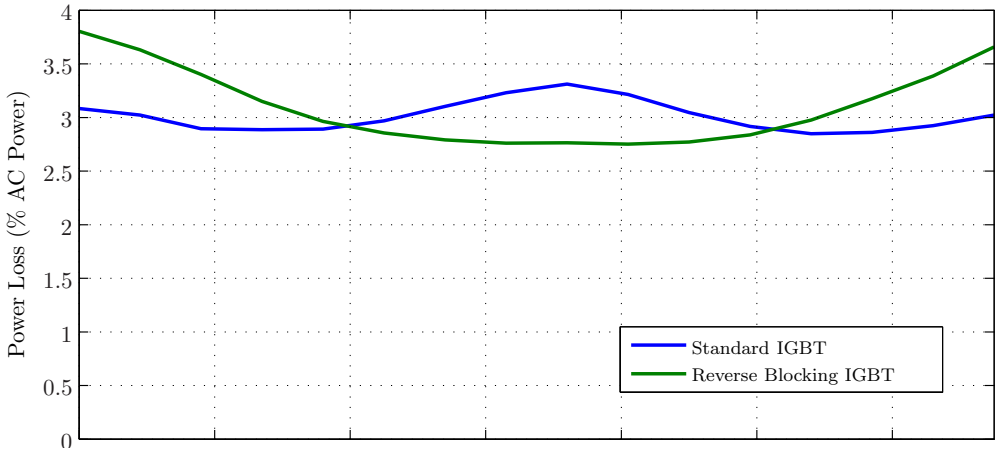
(b) 75% load

(c) 100% load

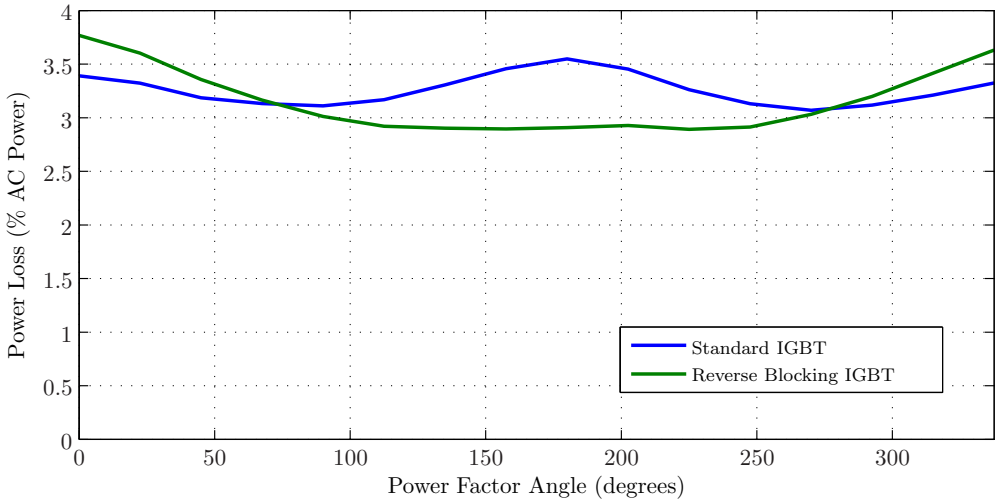
Figure 4.9: Breakdown of losses from Hybrid Converter Topology at 25%, 75% and 100% load



(a) 25% load



(b) 75% load



(c) 100% load

Figure 4.10: Comparison of losses with standard and reverse blocking IGBT used in the Cycloconverter section of the T3 converter operating at 25%, 75% and 100% load

in lower percentage conduction losses in the Cycloconverter stage. In the primary VSI the DC link is kept constant so the average current has to therefore increase. This results in slightly higher primary conduction losses. This, combined with a reverse blocking IGBT, reduces the full power losses of The Hybrid Cycloconverter Topology by 30% and results in the converter with the highest efficiency.

Figure 4.10 shows a comparison between The Hybrid Cycloconverter Topology with standard devices and reverse blocking devices in the Cycloconverter stage. The RB IGBT has large reverse recovery charge and as such when the diodes in the Cycloconverter are the switching devices, the total losses from the converter are considerably larger in the reverse blocking model. However when the current and voltage are 180^o out of phase the IGBTs switch instead. As a result the total losses from this converter are much lower because there are only two semiconductors in the Cycloconverter stage conduction path, instead of 4 for the standard devices.

4.3.5 Further Discussion of Losses

This section compares the losses from the 6 topology variations at the same phase angle and power level in order to allow for an in depth comparison to be made so that conclusions can be made regarding the suitability of a particular converter to a specific application. This comparison was performed at two different switching frequencies to discover if a particular topology would be more suitable for high frequency applications. For this comparison the converters were split into two sections, the components connected to the primary side of the transformer and the DC network (from now on called the primary converter) and the components connected to the secondary side of the transformer or the AC network (from now on called the secondary converter). For the Triple VSI Topology, VSI1 is the primary converter and VSI 2+3 are the secondary converter. The Cycloconverter topologies are split so that VSI stage is the primary converter and the Cycloconverter stage is the secondary converter. All the loss results in the comparison are given in percentage of total converter AC power.

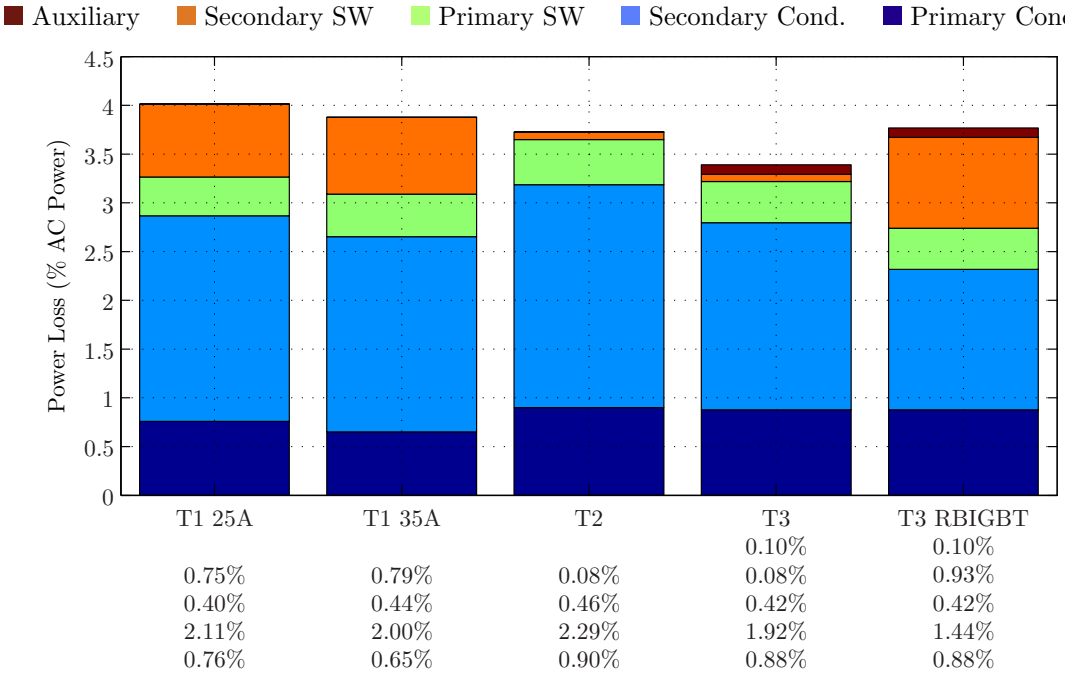
Analysis of Converter Supplying Real Power to the Grid

Figure 4.11 shows the direct comparison of the investigated topologies and the proposed variations at low frequency (5kHz) and high frequency (10kHz) with zero phase shift between the current and voltage from the output of the converter.

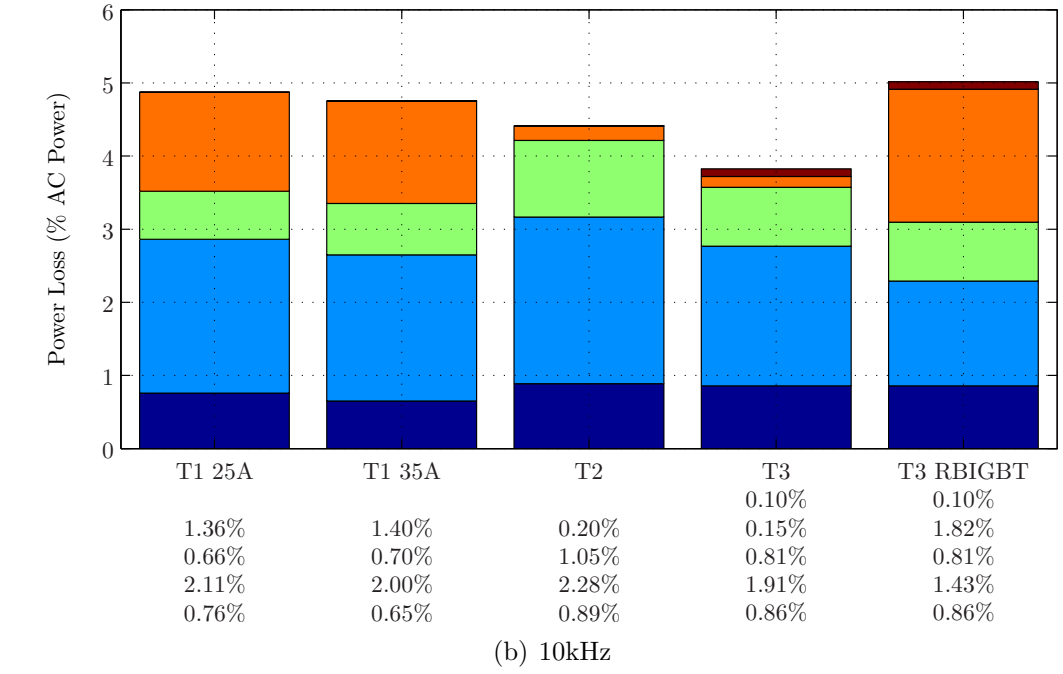
The primary converter conduction losses are greater in the Cycloconverter topologies (T2, T3) compared with the Triple VSI Topology (T1) due to the greater power variation. The Cycloconverter Topology (T2) has the greatest losses of 0.90% and the two arrangements of The Hybrid Cycloconverter Topology (T3) having losses of 0.88%, due to the increased power processed by these converters. The 25A Triple VSI Topology (T1) has greater losses than the 35A device, due to the reduced silicon area of the 25A device (0.65% compared with 0.76%). At the high switching frequency, the primary conduction losses remain within 0.02% of the low switching frequency results.

The Cycloconverter Topology (T2) has the greatest power loss in the secondary converter (2.29%) due to the fact that there are 4 semiconductors continuously in the conduction path. The Triple VSI Topology (T1) has losses of 1.35% in VSI 3 and this is combined with the losses of VSI 2 (the primary converter) to give the secondary converter losses (2.11% and 2.00% for the 25A and 35A device respectively). The Hybrid Cycloconverter Topology (T3) has reduced losses of 1.92% due to the increased power processed by this converter whilst operating at the same output current. The Hybrid Cycloconverter Topology has considerably reduced losses (1.44%) due to the fact that there are only 2 devices in the conduction path. This converter also processes a higher power with the same current. At the higher switching frequency the secondary conduction losses do not change by more than 0.01%.

The switching losses in the primary converter are within a 0.06% range for all of the converters (0.40% – 0.46%) at the low switching frequency, whereas at the high switching frequency the losses are lowest with the Triple VSI Topology (T1) (0.40% for the 25A and 0.44% for the 35A). The 35A device has greater losses due to the increased E_{on} and E_{off} values for a given I_c in the component datasheet, shown in Appendix A, Section A.2. The primary switching losses in The Cycloconverter Topology more than double and result in this converter



(a) 5kHz



(b) 10kHz

Figure 4.11: Comparison of losses of the converters at full power. 0° phase shift between voltage and current

having the greatest switching losses at high frequency (1.05%). This is due to the fact that the primary converter for this topology a hard switched turn off. The Hybrid Cycloconverter Topologies (T3) also have a hard switched turn off in the primary converter, but these converters both have reduced losses at high frequency (0.81%) compared with The Cycloconverter Topology (T2) due to the increased power processed by these converters.

The switching losses in the secondary converter are greatest in the Triple VSI Topology, with the 25A devices having lower losses than the 35A device (0.75% compared with 0.79%). The Cycloconverter topologies have considerably reduced losses (0.8% for The Cycloconverter Topology (T2) and Hybrid Cycloconverter Topology (T3)) due to the soft switching nature of the Cycloconverter stage. The Hybrid Cycloconverter Topology with the RB IGBT has large secondary converter switching losses of 0.93%, due to the poor reverse recovery of the integrated diodes in the Reverse blocking IGBT.

At the higher switching frequency, the switching losses in the secondary converter of the Triple VSI Topologies (T1) almost double to 1.36% and 1.4% respectively. In the Cycloconverter topologies (T2, T3) the switching losses in the secondary converter will also double to 0.2% and 0.15% for the Cycloconverter and Hybrid Cycloconverter Topology respectively. The Hybrid Cycloconverter Topology with the RB IGBT will also have its switching losses doubled to 1.82%. This corresponds to the expected result; as the switching frequency is doubled the switching losses should also double.

The losses in the auxiliary 3-Phase VSI remain at 0.1% for both high frequency and low frequency operation due to the fact that the majority of the losses in this converter are conduction losses (the MOSFETs used are capable of operating at a considerably higher switching frequency, up to 1MHz). The losses in the auxiliary converter do not change as the phase shift between voltage and current varies.

Analysis of Converter Supplying Reactive Power

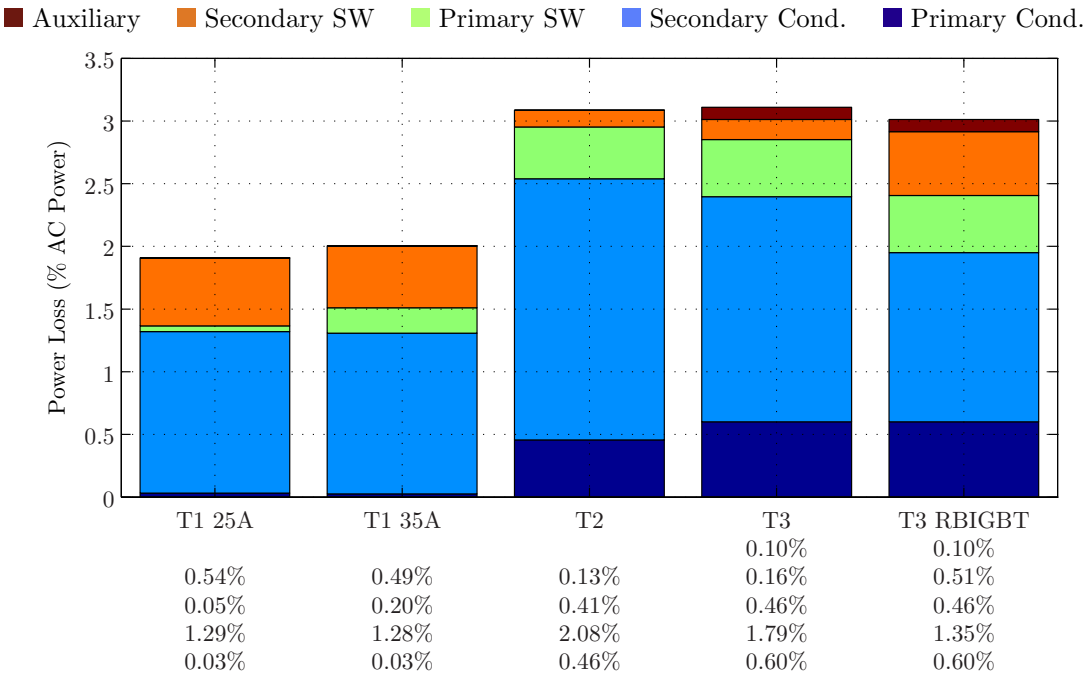
Figure 4.12(a) and 4.12(b) show the direct comparison of the investigated topologies and the proposed variations at low frequency (5kHz) and high frequency

(10kHz) with 90° phase shift between the current and voltage from the output of the converter.

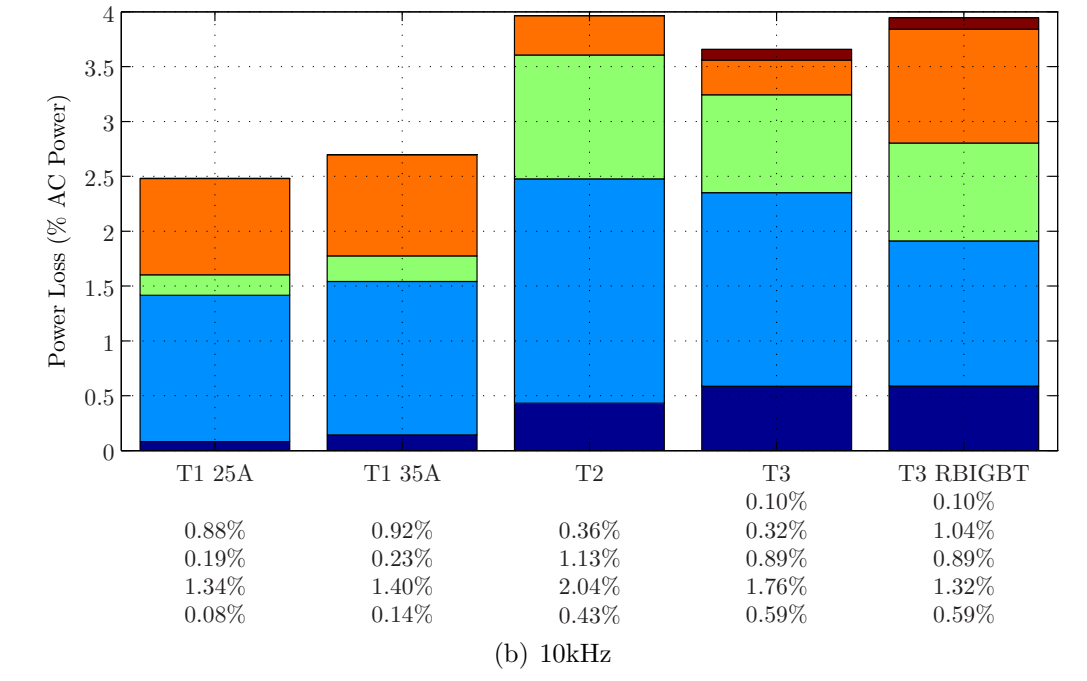
The conduction losses of the primary converter are lowest in the Triple VSI Topologies (T1) with both 0.03% for both the 25A and 35A devices. As the primary converters do not process any power, there is no advantage in a component with a large silicon area. The Hybrid Cycloconverter Topology (T3) and The Hybrid Cycloconverter Topology with RB IGBT have the same conduction losses on the primary converter (0.60%) due to the same current through these devices. The Cycloconverter Topology (T2) has reduced losses of 0.46% because of the fact that there is no instant when the voltage and current are at a peak with this converter. At the higher switching frequency, the conduction losses do not vary more that 0.02% for the Cycloconverter (T2) and Hybrid topologies (T2 and T3). The primary conduction losses in the Triple VSI Topology (T1) increased by more than double; however this may be due to a simulation errors when operating with zero current.

The conduction losses in the secondary converter continue to be lowest in the Triple VSI Topology (T1) with 1.29% and 1.28% for the 25A and 35A devices respectively due to the low losses in VSI 2. The Cycloconverter Topology (T2) has the greatest conduction losses at 2.08% due to the fact that there are always 4 devices in the conduction path. The Hybrid Cycloconverter Topology (T3) has reduced losses of 1.79% due to the increased power processed by this converter. The RB IGBT reduces this conduction losses further to 1.35% by only having 2 devices in the output conduction path. At the higher switching frequency the secondary converter conduction losses in the Cycloconverter topologies (T2 and T3) do not vary by more than 0.04%.

The primary switching losses are lowest with the Triple VSI Topology (T1), due to the fact that this section of the converter continues to not process any power (0.15% and 0.20% for the 25A and 35A device respectively). The Hybrid Cycloconverter Topology (T3) has the highest switching losses in the primary converter (of 0.46%) due to the fact that there is longer duration when there is substantial current and the voltage is at a maximum. The Cycloconverter has primary switching losses of 0.41%. At the higher switching frequency the losses in the Hybrid Cycloconverters (T3) double to 0.89% and for the Cycloconverter the losses more than double to 1.13%. This is for an unknown reason. The Triple VSI



(a) 5kHz



(b) 10kHz

Figure 4.12: Comparison of losses of the converters at full power. 90° phase shift between voltage and current

Topology (T1) increase its switching losses to 0.19% and 0.23% for the 25A and 35A device respectively but as it continues to not process any power this result may not be accurate.

The secondary switching losses are lowest for The Cycloconverter Topology (0.13%) followed by The Hybrid Cycloconverter Topology (0.16%). The RB IGBT still sufferers from high switching losses (0.51%) due to the reverse recovery in the integrated diodes, however these losses are now considerably reduced as for half the time the IGBTs are switching and not the diodes. The Triple VSI Topology (T1) now has a similar level of switching losses in the secondary converter as the reverse blocking IGBT, at 0.54% and 0.49% for the 25A and 35A devices respectively; the 25A device having lower losses due to the fact that VSI 2 does not process any power, so there is a disadvantage from a bigger silicone area.

The losses in the auxiliary 3-Phase VSI remain at 0.1% for both high frequency and low frequency operation due to the fact that the majority of the losses in this converter are conduction losses.

Analysis of Converter Drawing Real Power From the Grid

Figure 4.13 shows the direct comparison of the investigated topologies and the proposed variations at low frequency (5kHz) and high frequency (10kHz) with ninety degrees phase shift between the current and voltage from the output of the converter.

The conduction losses in the primary converter are similar for all of the 5 converter variations. The 25A VSI (T1) converter has the highest losses and the other converters have losses of 0.65-0.69%. At the higher switching frequency the conduction losses in the primary converter do not vary by more than 0.01%.

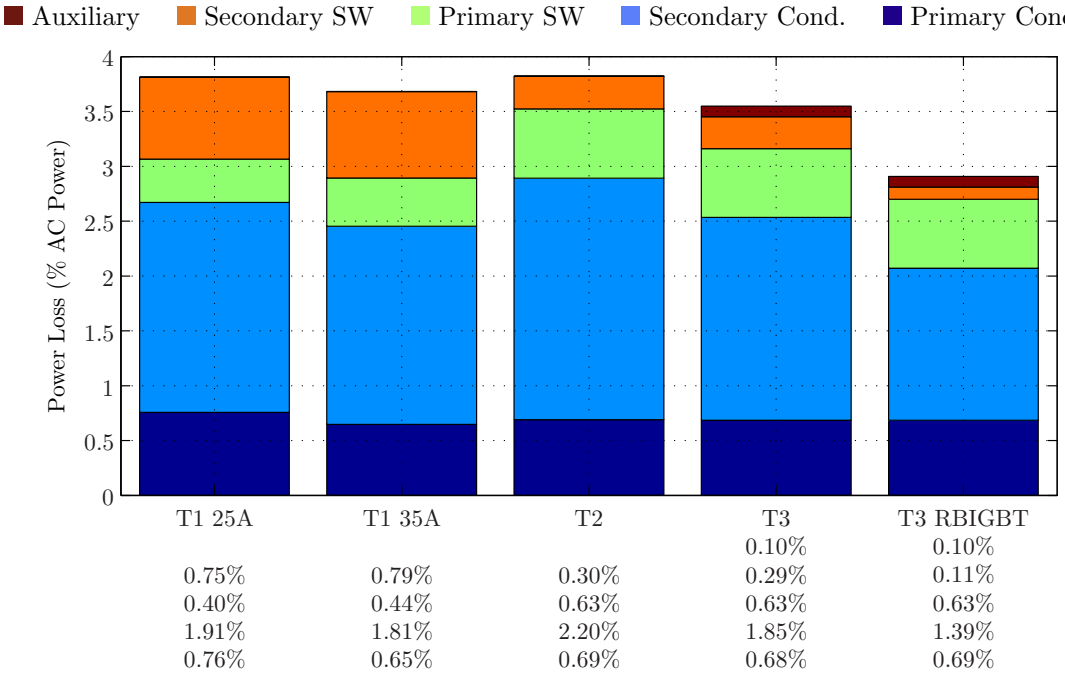
The secondary conduction losses show more of a variation across the range of converter; the Hybrid Cycloconverter with RB IGBT (T3) converter has the lowest at 1.39%, due to only having 2 devices in the conduction path, followed by the VSI (T1) topologies. The 25A device has a loss of 1.91% and the 35A% device has a loss of 1.81%; the increased silicon are showing a benefit in this case.

VSI 3 losses are 1.15% for both theses converters as the both use the same devices in the output stage. At the higher switching frequency, the secondary conduction losses vary by a marginally larger amount (0.06%) but this is not outside the margin for error.

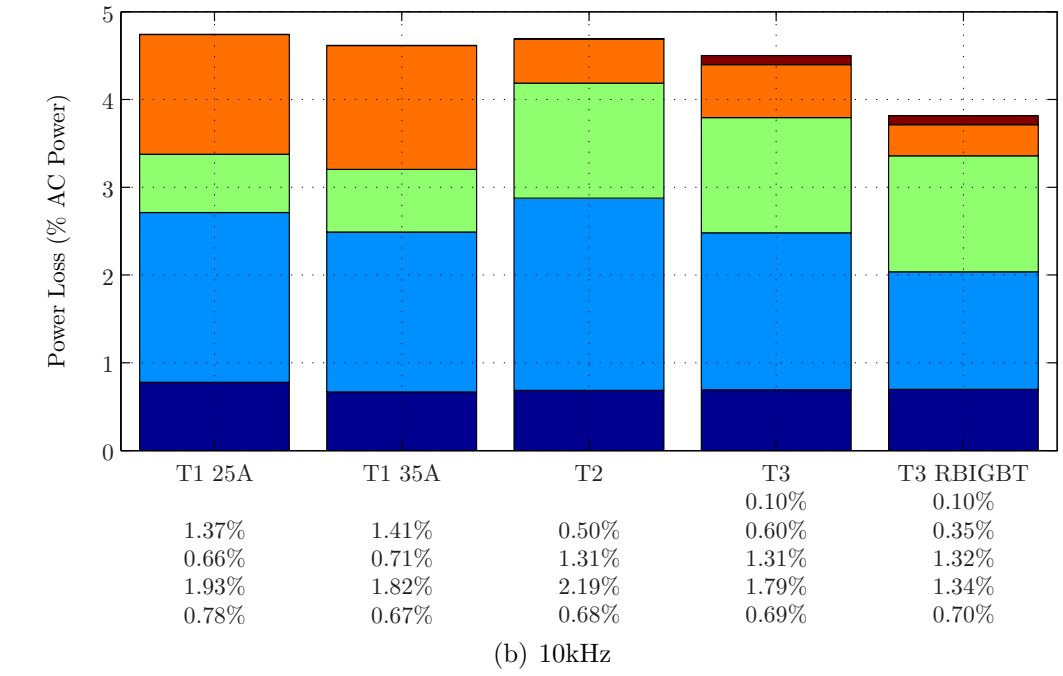
The primary switching losses are constant for the Cycloconverter (T2) and Hybrid (T3) topologies at 0.63% and 0.40% and 0.44% for the 25A and 35A VSI (T1) respectively. This is due to the fact that the primary VSI on the Cycloconverter Topologies has some hard switched transitions. At the higher switching frequency, the Cycloconverter topologies primary switching losses are more than doubled to 1.31%, whereas for the Triple VSI Topology the switching losses only increase to 0.66% and 0.70% for the 25A and 35A device respectively.

The secondary switching losses are lowest for The Hybrid Cycloconverter Topology (T3) with the RB IGBT (0.11%) as the IGBTs are now switching instead of the diodes, preventing the huge reverse recovery losses that have been witnessed in the previous graphs. The Hybrid Cycloconverter Topology (T3) has the next lowest losses (0.29%) followed by the Cycloconverter (T2) with 0.30%. Due to the hard switched nature of the Triple VSI Topology, this converter has the largest secondary switching losses with 0.75% for the 25A device and 0.79% for the 35A device. At the higher switching frequency, the secondary switching losses from the Triple VSI Topology is almost doubled to 1.37% and 1.41% for the 25A and 35A device respectively. The switching losses in the secondary converter from The Cycloconverter Topology (T2) have not increased as much as for The Hybrid Cycloconverter Topology (T3) and are now 0.50% and 0.60%. This is for an unknown reason. The Hybrid Cycloconverter Topology with RB IGBTs has increased to 0.35% but it continues to have the lowest secondary switching losses.

The losses in the auxiliary 3-Phase VSI remain at 0.1% for both high frequency and low frequency operation due to the fact that the majority of the losses in this converter are conduction losses.



(a) 5kHz



(b) 10kHz

Figure 4.13: Comparison of losses of the converters at full power. 180° phase shift between voltage and current

4.3.6 Extrapolation of Losses with Switching Frequency

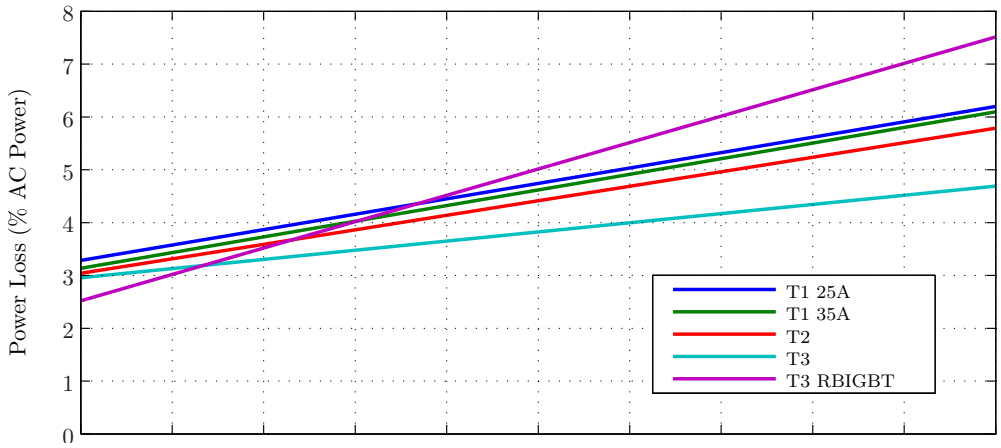
The results from the converters' operating at full power and 5kHz and 10kHz were extrapolated over 0-20kHz so that the crossover frequency between the converters with the lowest losses could be found. The results from this extrapolation is shown in Figure 4.14.

Figure 4.14(a) shows that when the current and voltage are in phase, at very low frequencies The Hybrid Cycloconverter Topology (T3) with the RB IGBT has the lowest losses. However due to the high reverse recovery losses in the reverse blocking diode the efficiency of this converter rapidly decreases with frequency. The Hybrid Cycloconverter Topology (T3) has the smallest increase in efficiency over the frequency range and therefore performs best at high frequencies. The Cycloconverter Topology (T2) and the Triple VSI Topology (T1) have a lower separation over the frequency range, with The Cycloconverter Topology (T2) having lower losses than the Triple VSI Topology (T1), the Triple VSI Topology with the 35A device having lower losses than the 25A device, due to the lower conduction losses in this device.

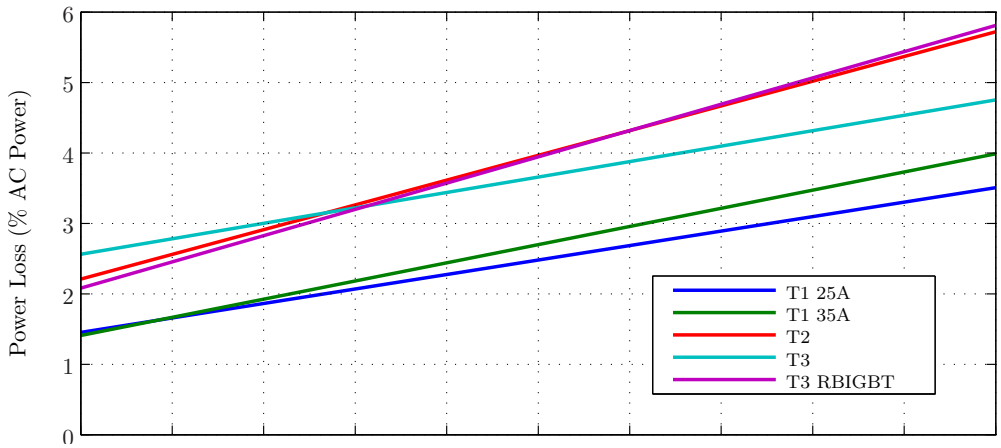
With a 90^o phase shift between voltage and current, Figure 4.14(b) shows that the Triple VSI Topology (T1) has considerably lower losses than the other converters, due to the fact that VSI 1 + 2 in this converter only process the average power, which is zero. The 25A device has lower losses that the 35A device because these devices are no longer processing any current so the device with the smallest switching losses has lower overall losses.

The Hybrid Cycloconverter Topology has lower losses than The Hybrid Cycloconverter Topology with RB IGBT and The Cycloconverter Topology above 6kHz, whereas below 6kHz The Hybrid Cycloconverter Topology with the RB IGBT has lower losses.

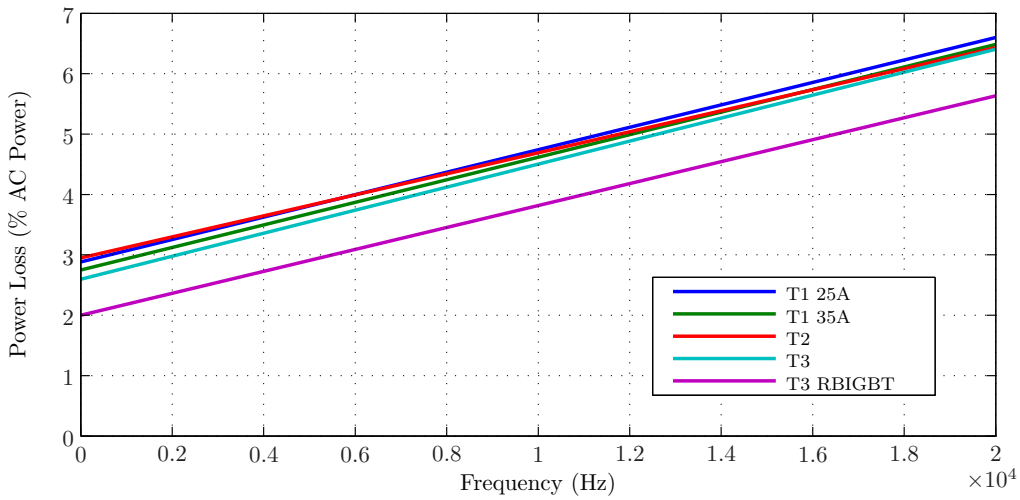
At a phase shift of 180^o, Figure 4.14(c) shows the order of the converters in terms of efficiency is more constant as the frequency varies; the RB IGBT has the by far the lowest losses, followed by the other 4 simulated converters. The Hybrid Cycloconverter Topology (T3) has the next lowest losses for the whole of the frequency range. The Cycloconverter Topology (T2) has the highest losses at low



(a) 0° phase shift between voltage and current



(b) 90° phase shift between voltage and current



(c) 180° phase shift between voltage and current

Figure 4.14: Extrapolation of converter losses with frequency for the 5 converter variations operating at full power

frequencies whereas above 15kHz it has a similar efficiency as The Hybrid Cycloconverter Topology (T3). The 35A Triple VSI Topology (T1) has consistently lower losses than the converter with the 25A devices.

4.3.7 Analysis of Reverse Recovery in Cycloconverter

The large reverse recovery losses of the integrated diode in the RB IGBT of 0.93%, shown in the "Secondary SW" line of Figure 4.11(a), resulted in an investigation into the causes of this additional loss and the impact that this could have on the converter. In order to achieve this, a dynamic device model was used in Saber Simulator. Unlike the ideal PSIM model, this model is able to accurately simulate the voltage across the device and the current through the device during the switching transitions.

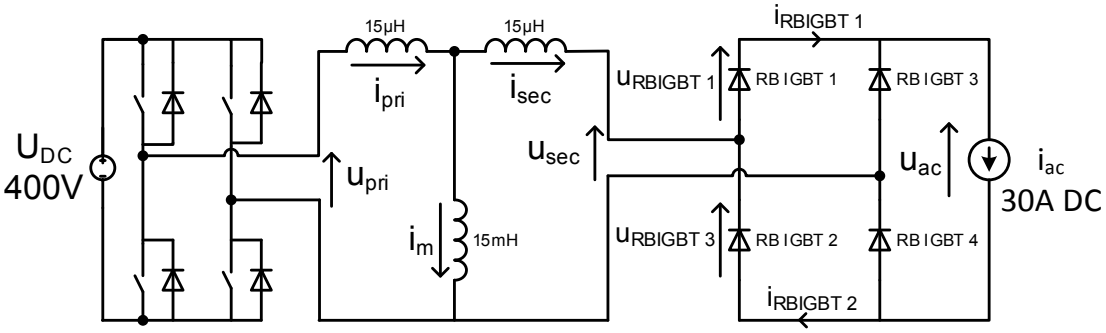


Figure 4.15: Cycloconverter Topology model used to investigate the reverse recovery from the internal diode of the RB IGBT with Saber

As the model was only used to investigate one particular phenomena, the Cycloconverter circuit model, Figure 4.15, was used to reduce simulation time and to solely investigate this one phenomena. This model utilized an ideal DC voltage source connected to a VSI constructed from ideal IGBTs and diodes, a transformer modelled using primary, secondary and magnetizing inductance and no isolation. The RB IGBTs were modelled using the diode model with reverse recovery. This model includes on state resistance, forward voltage drop, t_{rr}, Q_{rr}, and C_j the junction capacitance. These parameters were obtained from the component datasheet and are shown the Appendix. Figure 4.15 shows the schematic of the simulated model.

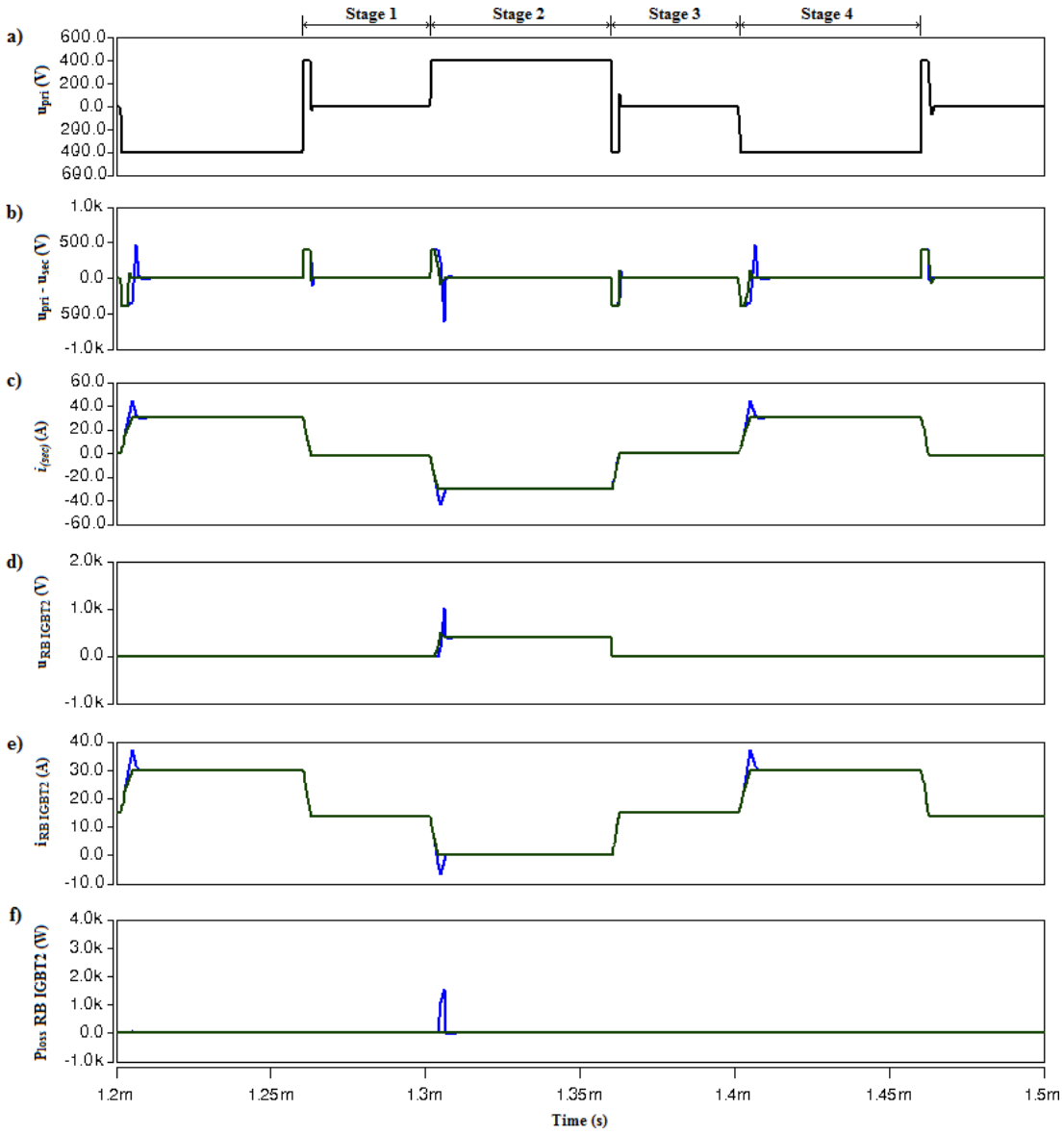


Figure 4.16: Voltage and current through Cycloconverter diodes with reverse recovery charge taken into account. $Q_{rr} = 35\mu$ C
a) u_{pri} – Voltage across transformer primary
b) u_{pri} - u_{sec} – Voltage across leakage inductance
c) i_{sec} – Current through transformer secondary leakage inductance
d) $u_{RBIGBT2}$ – Voltage across RB IGBT 2
e) $i_{RBIGBT2}$ – current through RB IGBT 2
f) $P_{loss}RBIGBT2$ – Power loss in RB IGBT 2

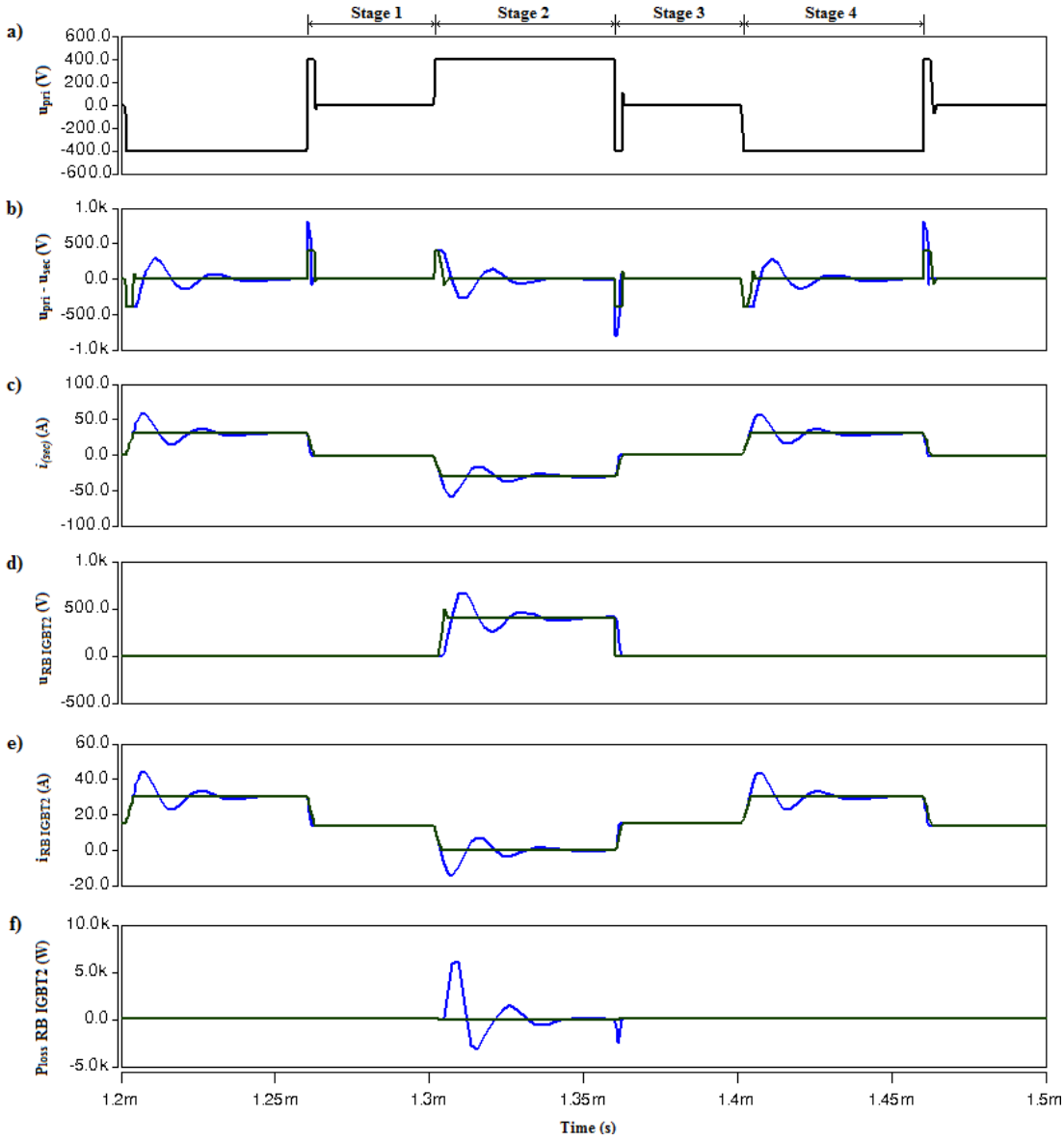


Figure 4.17: Voltage and current through Cycloconverter diodes with gate capacitance and reverse recovery charge taken into account. $Q_{rr} = 35\mu$ C, $C_j = 90$nF
a) u_{pri} – Voltage across transformer primary
b) u_{pri} - u_{sec} – Voltage across leakage inductance
c) i_{sec} – Current through transformer secondary leakage inductance
d) $u_{RBIGBT2}$ – Voltage across RB IGBT 2
e) $i_{RBIGBT2}$ – current through RB IGBT 2
f) $P_{loss}RBIGBT2$ – Power loss in RB IGBT 2

No diode forward recovery effects was included in the model since these are minimal compared with the reverse recovery and reliable data was not available from the component datasheet.

Chapter 3, Section 3.2 analysed the operation of The Cycloconverter Topology and split the operation of the Cycloconverter into 4 different stages. For this simulation only the situation when the current was in phase with the voltage was analysed. The results from this simulation are shown in Figure 4.16 when just the diode reverse recovery, Q_{rr}, is taken into account, and 4.17 when the diode reverse recovery, Q_{rr}, and the junction capacitance, C_j is taken into account.

For the first stage the output current, i_{ac}, is free-wheeling through all 4 of the integrated diodes in the RB IGBT (RB IGBT 1-4).

The second stage is when a positive voltage is applied by VSI 1 to the transformer, u_{pri}. As the 4 RB IGBTs are still conducting, u_{sec} is short circuited and the whole of u_{pri} appears across the leakage inductance ($u_{pri} - u_{sec}$). This results in the current through the leakage inductance, i_{sec}, increasing negatively, the di/dt limited by the value of the leakage inductance. This causes the total current through RB IGBT 2+3 to decrease, and RB IGBT 1+4 to increase (RB IGBT 2+3 will have $\frac{i_{ac}}{2} - i_{sec}$ and RB IGBT 1+4 will have $\frac{i_{ac}}{2} + i_{sec}$).

When i_{sec} is equal to i_{ac}, in an ideal situation, RB IGBT 1+4 diodes would carry all the current and RB IGBT 2+3 diodes would switch off. This would result in the transformer output being connected to the output of the Cycloconverter and the voltage would no longer be across the leakage inductance and instead would be at the output of the converter. However when the integrated reverse-blocking diode in the RB IGBT is taken into account, u_{sec} continues to be short circuited until all of the reverse recovery charge, Q_{rr}, has been removed, resulting in an overshoot in i_{sec} compared with i_{ac}. For the simulation with the junction capacitance taken into account (Figure 4.17) this current overshoot causes large oscillations at the resonant frequency of the combined leakage inductance and junction capacitance (68kHz). This will cause very high losses in the RB IGBTs and may even destroy the devices if an inadequate snubber or clamp circuit is used.

For stage three an open circuit is applied by the IGBTs in VSI 1 and the energy contained in i_{pri} is returned to the supply by the integrated diodes in VSI 1. The fourth stage is the same as the second stage, only the current in i_{sec} builds up positively and the current in RB IGBT 2+3 increases and the current in RB IGBT 1+4 decreases.

One technique that could be used to reduce this overshoot is to apply a short circuit to the primary of the transformer during this reverse recovery time. This could result in the current level through the leakage inductance being kept constant, at i_{ac}, until the diodes have switched completely off. If, at low di/dt, the diode reverse recovery charge does not vary much from the datasheet value, this may result in the switching time of the diode becoming excessively large. This would need to be investigated further with experimental data as there is very little information relating to this situation available.

4.4 Summary

This chapter has investigated the semiconductor losses for the two Cycloconverter topologies against that of the Triple VSI Topology. It has introduced the techniques used for simulating the losses in order to obtain results at different phase angles and power loads. This was repeated at twice the switching frequency to discover whether one of the topologies better suited to a converter operating at a higher switching frequency. The results have then been presented and further analysis has been carried out to investigate the reverse recovery losses and the effect that these additional losses will have on the operation of the converter. A solution has been proposed, however this will require further investigation before it should be implemented.

When processing reactive power the Triple VSI Topology has the lowest losses, due to the transformer and VSI 1 and 2 only processing real power. The losses in the Cycloconverter topologies are predominately conduction losses in the Cycloconverter stage and as such the utilization of a RB IGBT with considerably lower forward voltage should result in a more efficient converter. However some of the results show excessively high diode reverse recovery whilst other results

do not. These results should therefore be experimentally verified before conclusions can be drawn about the performance of the reverse blocking IGBTs. The Hybrid Cycloconverter Topology produces a higher voltage than the traditional Cycloconverter Topology and therefore shows constantly lower conduction losses across the whole power range and therefore overall efficiency.

The Hybrid Cycloconverter Topology showed the lowest increase in losses when the switching frequency was doubled, and therefore this topology would better suited to high frequency operation. The 25A device in the Triple VSI Topology had a lower increase in losses compared with the 35A device, although the improvement was minimal. The Cycloconverter Topology showed a similar increase in losses to the 25A device in the Triple VSI topology.

The results from conduction losses should be fairly accurate, due to the fact that information relating to voltage drop against current from experimental results is available in each component datasheet. The reverse recovery losses however are far more dependent on circuit operation and obtaining reliable information requires experimental analysis as the available information is designed for a hard switched converter. For example in a diode datasheet, the reverse recovery charge is normally given at a particular di_F/dt, or a range of di_F/dt, at a particular voltage and current.

For the specific example of The Cycloconverter Topology, no information on reverse recovery is given for very low di_F/dt as this is limited by the leakage inductance in the transformer and will be orders of magnitude smaller than in a hard switched converter. The di_F/dt of The Cycloconverter Topology is in the range of 15A/μ s, and the information in the datasheet is usually given in the range of 100 - 600 A/μ s. This may result in the reverse recovery losses from the Cycloconverter stage being completely different in an experimental converter than the predictions from simulation.

The second cause of error in the simulation will be due to the technique that PSIM utilizes to calculate the losses from a switching transition. PSIM measures the voltage and current before and after the switching event and uses the current to look up or calculate the E_{rr} for a given current. PSIM then scales this result based on the voltage being applied. This may only work accurately for a hard

switched converter, as when a diode is soft switched the current and voltage should be zero at the switching transition. The instance at which the voltage and current are sampled will therefore have a huge impact on the simulated losses.

Another potential source of error in the simulation is that the device models used by PSIM are based on device characteristics at one temperature, 125°C. Depending on the semiconductor losses for each converter, the actual substrate temperature will vary from this value depending on the conduction and switching losses of the switching device.

The characteristics of the actual device will differ from the modelled device effecting the losses in the converter. A more accurate approach would be to calculate the losses after each switching period and using a thermal model of the switching device and cooling solution, derive the semiconductor temperature. The switching device model would incorporate the effect of temperature on the device, allowing for a more accurate prediction of converter losses.

This technique would require a farm more detailed circuit model and would result in a much greater simulation time. This would not be suitable for the simulation carried out in this chapter as it would not be feasible to carry out a comparison of many different circuit configurations arrangements.

Chapter 5

The Experimental Converter Rig

This chapter will document the construction of the experimental converter, used to verify the operation and validate the performance of the Cycloconverter and Hybrid Cycloconverter Topologies. This will confirm aspects of the performance and simulation results presented earlier in this thesis. This chapter will first cover the control flow and the hardware construction before covering the implementation of modulation and switching strategy, analogue voltage and current measurements and the protection circuitry.

5.1 Overall Converter System Design

The experimental converter was constructed in a modular fashion. Some components and circuits were designed specifically for this project. Some component designs were used from earlier projects at the University of Nottingham; these included the FPGA board, the Single Phase VSI Printed Circuit Board (PCB) and the Three Phase VSI PCB. Figure 5.1 shows a block diagram of the entire system. A single DC source was connected to the three Single Phase VSIs.

For the initial testing a 1.5kW, 360V DC power supply, the EA-PSI 8360-15 was used. When testing at full power, with bi-directional power flow, a 4 quadrant 60kW, 500V DC power supply was used, the Regatron TopCon.GSS. A voltage

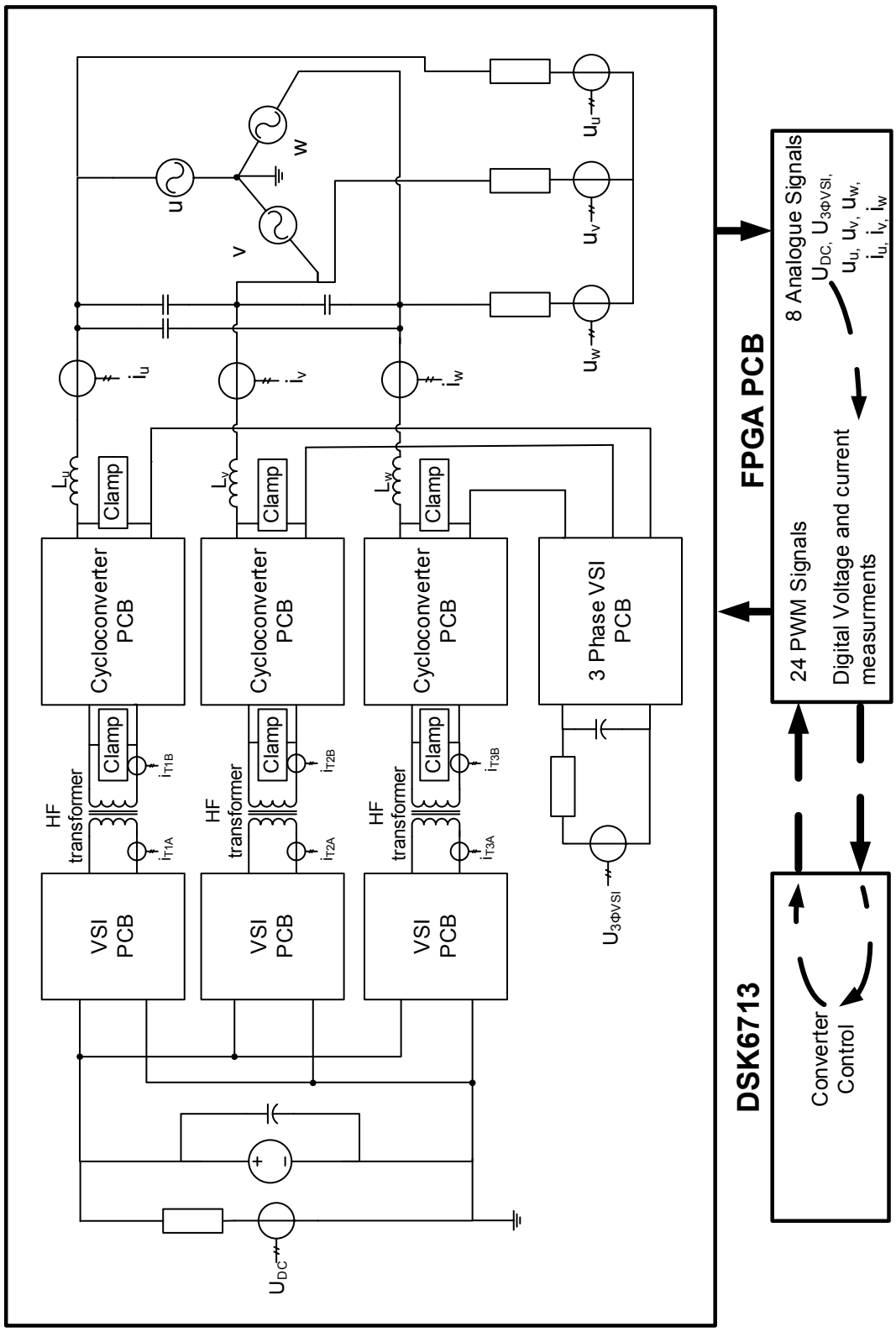


Figure 5.1: Block diagram of complete converter

sensor, U_{DC}, and a 3.2mF electrolytic capacitor is also connected across the DC link. The size of this capacitor is dictated not by the required amount of stored energy but instead by the capacitor current rating, limited by the ESR of the device.

The capacitor has not been optimized for this converter and has been over specified, however by utilizing an excessively large capacitor the ESR losses will be reduced, as will the chance of a failure of the capacitor from overheating. The VSIs are connected to the Cycloconverters via a High Frequency (HF) transformer. Section 5.2 describes the Single Phase VSI construction and Section 5.3 describes the auxiliary 3-Phase VSI. The Cycloconverter is described in Section 5.4. Chapter 6 will cover the design and construction of this transformer.

No.	Process	Location
1	Isolated analogue sensors read AC voltages and currents	Analogue sensors
2	Interrupt generated	FPGA
3	A2D conversion is performed	FPGA
4	Analogue to Digitals (A2Ds) read and scaled	DSP
5	Control calculations performed	DSP
6	Current polarity determined	DSP
7	Current controller produces reference	DSP
8	Buffered reference until next interrupt	FPGA
9	PWM signals generated	FPGA
10	Signals sent to power boards via optical connections	FPGA
11	Dead time added in hardware	VSI
12	IGBTs switched	Power PCB

Table 5.1: Converter control flow

The analogue sensors used for measuring of the 3 AC voltages, v_u, v_v, v_w, and currents, i_u, i_v, i_w required for the control of the converter are described in Section 5.5.

To protect the converter from over-voltages from an interruption in current in the AC inductor or leakage inductance in the transformers, a clamp circuit is placed on the primary and secondary windings of the transformers. This voltage protection circuit is described in Section 5.7.1.

To protect the converter from over-currents from transformer saturation, additional current sensors with a built in over-current trip are placed on the primary and secondary windings of the transformers. An Enable Loop is used with these current sensors to disable the converter in the case of an over current. This over current protection circuit is described in Section 5.7.2.

The FPGA is directly mapped to the Digital Signal Processor (DSP) memory, using the External Memory Interface (EMI) connector, allowing for the transfer of these digital measurements to the DSP. The DSP performs grid synchronization, implements the control system and the distribution of power between the Cycloconverter and auxiliary 3-Phase VSI. The converter reference voltages are transferred back to the FPGA using the common memory and the FPGA performs modulation. The PWM signals are sent to the converter via Fibre Optics from a optical expansion board mounted on top of the FPGA. Table 5.1 shows the converter control flow.

The FPGA is connected to the power PCBs using Avago Technologies HFBR-1521 transmitters, 1mm diameter fibre optic cable and Avago Technologies HFBR-2521 receivers. Using this system provides complete isolation between the control stage and power stage. This is required not only for safety but to prevent noise from entering the control board that could otherwise occur if copper co-axial cable was used.

5.2 Single Phase VSI Construction

The DC sides of the transformers are connected to the DC link via three VSI PCBs, one for each phase of the converter. These were designed in [63] and were built, populated and tested by the author. Each PCB uses a 30A 1200V IGBT module, a Semikron Semitop SK30GH123, containing 4 IGBTs and four anti-parallel diodes, rated at 30A and 1.2kV. 600V devices could have been used, reducing switching losses but these devices were selected to allow for the potential of testing the converter at Medium Voltage. The signals to this converter can either be voltage, current or optical signals. For this converter, two optical connectors were utilized, one for each H-Bridge leg, with one for the enable

line. The enable line was required to switch off all the IGBTs, otherwise there would always be two IGBTs off and two on. The converter inverts the signals to generate the four switching pulses required for the four IGBTs. To prevent Shoot-Through, a variable dead time is introduced. This is added using an analogue RC filter, Diode and a Schmitt trigger. The Schematic of the VSI circuit is shown in Appendix B. The Single Phase H-Bridge is shown in Figure 5.2.

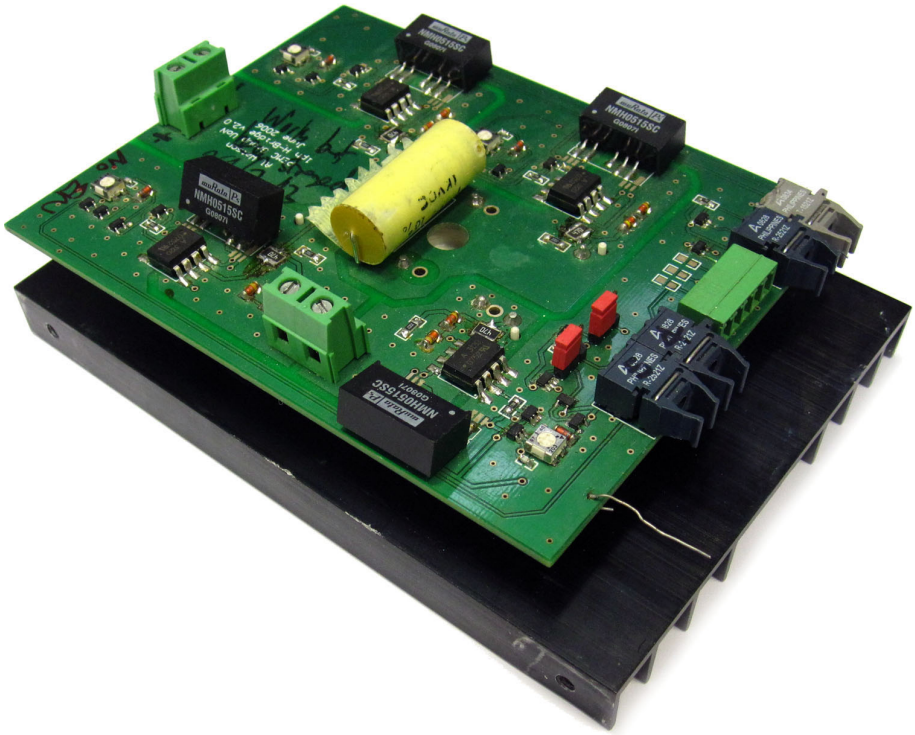


Figure 5.2: Single Phase H-Bridge

5.3 Auxiliary 3-Phase VSI Construction

The 3 Phase VSI was based on a PCB designed for the EON Supercapattery project at the University of Nottingham [64]. A unit was built, populated and tested by the author. An Infineon FS30R06W1E3 IGBT module was used as the switching device. This module contains six IGBTs and six anti-parallel diodes, arranged as a three bridge legs, rated at 600V and 30A. A lower voltage module could have been used but this would required a redesigned PCB. The Schematic of the 3-Phase VSI PCB is shown in Appendix B. Three or six fibre optic receivers can be used with the signals inverted and dead time added when three receivers

are used. For this project the three fibre optic connectors were utilized. The enable fibre optic connector was held high with an always on fibre optic transmitter on the optical expansion board as there is no requirement for all of the IGBTs to be off simultaneously.

This PCB contains an electrolytic DC link capacitance of 5.6mF, rated at 150V, used as the floating capacitance for the auxiliary 3-Phase VSI converter. The value of this capacitance dictates the bandwidth of the 3-Phase VSI DC link control system, with a smaller capacitance requiring a faster controller. A value of 5.6mF was used as it allowed for a low bandwidth controller and the components were already available form the EON Supercapattery project. This value was not optimized for this application, however it will result in extremely low capacitor ESR losses and will reduce the chance of failure of the capacitor from overheating. The auxiliary 3-Phase VSI is shown in Figure 5.3.

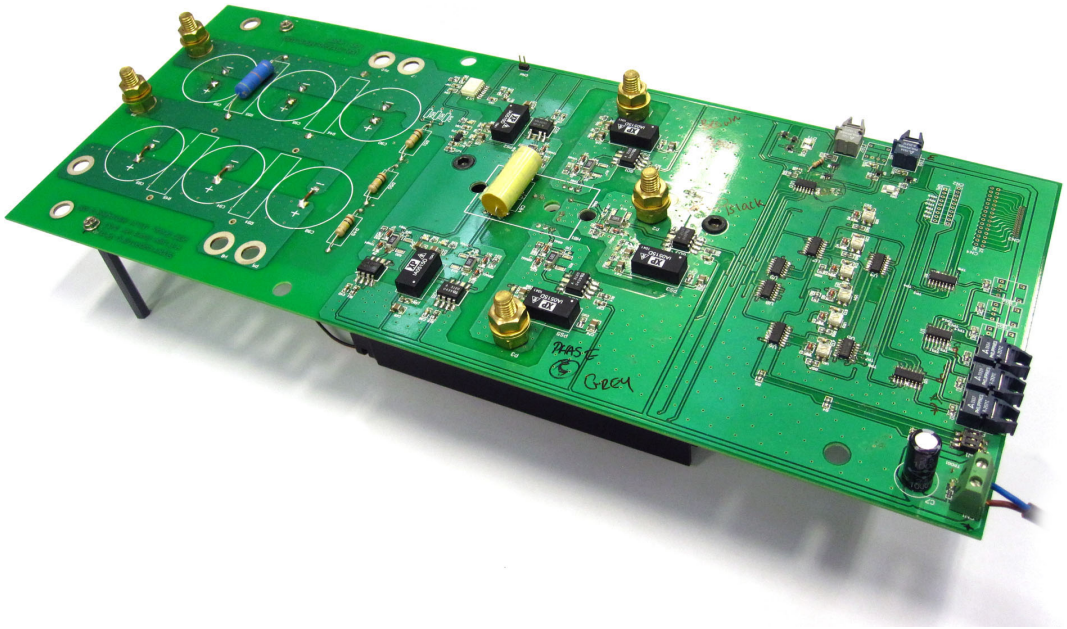


Figure 5.3: Auxiliary 3-Phase VSI PCB

5.4 Cycloconverter Construction and Design

The Cycloconverter PCB was designed and constructed specifically for this project by the author. Eight discrete switching devices are used, IXDR30N120D1, each

containing one IGBT and one anti-parallel diode, rated at 1200V and 35A. These devices have an electrically isolated back to allow for mounting to a common heat-sink. This negates the use of insulating silicone pads, reducing the thermal resistance between the devices and the heat-sink and increasing the ease of assembly. For each Cycloconverter PCB, the eight IGBTs are mounted to single Power PCB and eight individual Gate Drive PCBs, allowing for a single Gate Drive PCB to be replaced in the case of a failure.

Figure 5.4: Assembled Cycloconverter, with Power, Gate Drive and Control PCBs visible

The schematic for the Power PCB is shown in Figure 5.5 and the Gate Drive board is shown in Figure 5.6. The complete set of Schematics of the Cycloconverter circuit, including the Power PCB, the Control PCB and the Gate Drive PCB is shown in Appendix B. Three Cycloconverter PCBs were used for this project, one for each phase of the converter, as shown in Figure 5.1. The Cycloconverter is shown in Figure 5.4.

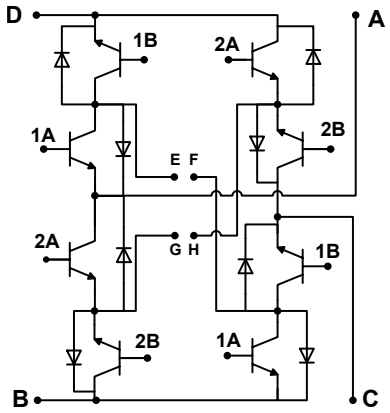


Figure 5.5: Cycloconverter Power PCB Schematic

Figure 5.5 shows the schematic diagram of the Cycloconverter PCB. The terminals labelled B and D were connected to the HF transformer and the terminals labelled A and C were connected to the AC inductor and 3-Phase VSI respectively. The Cycloconverter PCB was designed to be able to operate as a back to back VSI, with four 4mm terminals, labelled E, F and G, H, for connection to an external DC link capacitor, or as a Cycloconverter with the terminals left unconnected. This will allow for a future comparison to be made between the Cycloconverter and the back to back VSI topologies using the same PCB. The IGBTs are arranged in a back to back fashion, acting as bi-directional switches. 4 Signal lines are used, $1A$, $1B$, $2A$ and $2B$ with each signal connected to two IGBTs.

The Gate Drive PCB is mounted between the IGBT and the Power PCB, connecting to the Gate and Emitter of each IGBT. The board includes two back to back 19V Zener diodes, $Z1$ and $Z2$, across the gate of the IGBT for protection, a 19Ω gate resistor, $R3$, to limit the gate current and a pull down resistor, $R4$, to ensure that the IGBT remains off when the Gate Drive power is removed. The gate of the IGBT is driven by an Avago Technologies HCPL-3120 optocoupler that provides isolation between the IGBT and the logic circuit and is able to produce up to 2A of gating current.

Power is provided to the board at 5V and is converted to the ±15V relative to the Emitter of the IGBT required to drive the gate using an XP Power IA0515D isolated DC-DC converter module. The HCPL-3120 package contains a Light Emitting Diode (LED) on the logic side and the Anode is connected to Vcc via

a pull up resistor, inverting the signal. The Cathode is connected to an open collector Integrated Circuit (IC) mounted on the Control PCB above. As LEDs are current fed devices, this arrangement is relatively immune to noise.

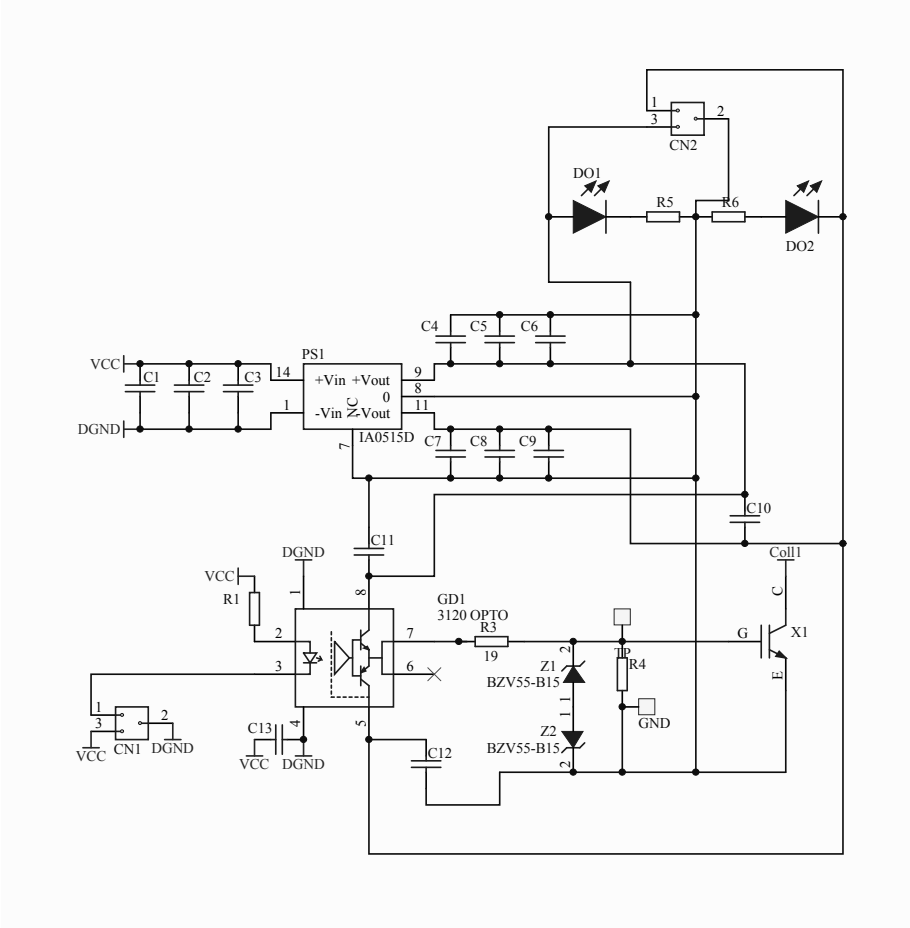


Figure 5.6: Cycloconverter Gate Drive PCB Schematic

This approach provides complete electrical isolation between the control DSP and FPGA and the switching semiconductors, with the both the optocoupler and isolated DC-DC converters rated for at least 1000V isolation between the logic level voltage and AC voltage level sections of the converter. This isolation is required for safety and protection of the LV sensors and equipment.

5.5 Analogue Sensors

Figure 5.1 shows the location of the analogue voltages and currents that need to be read for the control of the converter. These are the 3 AC voltages, u_u, u_v, u_w, the 3 AC currents, i_u, i_v, i_w, and the DC link voltage of the main converter, U_{DC} and the auxiliary 3-Phase VSI, $U_{3\Phi VSI}$.

To measure the AC and DC voltages, LEM LV-25P voltage transducers were used. These voltage transducers can measure up to 500V and provide galvanic isolation between the measured voltage and the secondary circuit. They rely on the Hall Effect to provide voltage measurement and require an external resistor in series with the device to produce a current proportional to the voltage to be measured. It is important that the resistor has minimal temperature dependence. Non-inductive planar Thick Film power resistors made by BI Technologies were used for this application. These resistors have a temperature coefficient of $\pm$100ppm/^{o}C and combined with a large surface area and high power rating give a minimal temperature drift over the operational range.

LEM LV-25P voltage transducers work by measuring the flux around the wire conducting the current to the series resistor. An equal but opposite flux is generated by a compensating current from the voltage transducer and this current is directly proportional to the voltage to be measured. This current is connected to the FPGA PCB where it is converted to a voltage by a 100Ω resistor in parallel to the A2D converter.

The sensing of AC currents was carried out using LEM LA-100-P with one complete turn over the current transducer, increasing the current measurement accuracy and decreasing the maximum measurable current to 50A. LEM LA-100-P current transducers work by measuring the flux around the wire conducting the current to be measured. An equal but opposite flux is generated by a compensating current from the current transducer and this current is directly proportional to the current to be measured. This current is connected to the FPGA PCB where it is converted to a voltage by a 100Ω resistor in parallel to the A2D converter.

The reading of the Analogue measurements is performed at the start of each Interrupt Service Routine (ISR). In this way the currents and voltages are sampled

at the same point in the switching cycle, when the converter is free-wheeling. This automatically filters out any switching ripple in both current and voltage. For this to operate correctly the bandwidth of the analogue sensors needs to be considerably higher than the ISR frequency. The analogue sensors are not filtered to the Nyquist frequency, instead a synchronous sampling approach is taken to eliminate the ripple harmonics. However the advantages of the removal of the switching ripple without introducing an additional delay in the control of the converter considerably outweigh the aliasing noise.

5.6 DSP and FPGA Design

The C6711 is a 32-bit floating point high performance DSP. The DSP was programed with the C programing language using Code Composer Studio from Texas Instruments. To transfer data between the DSP and FPGA, the DSP memory can be directly addressed by the FPGA.

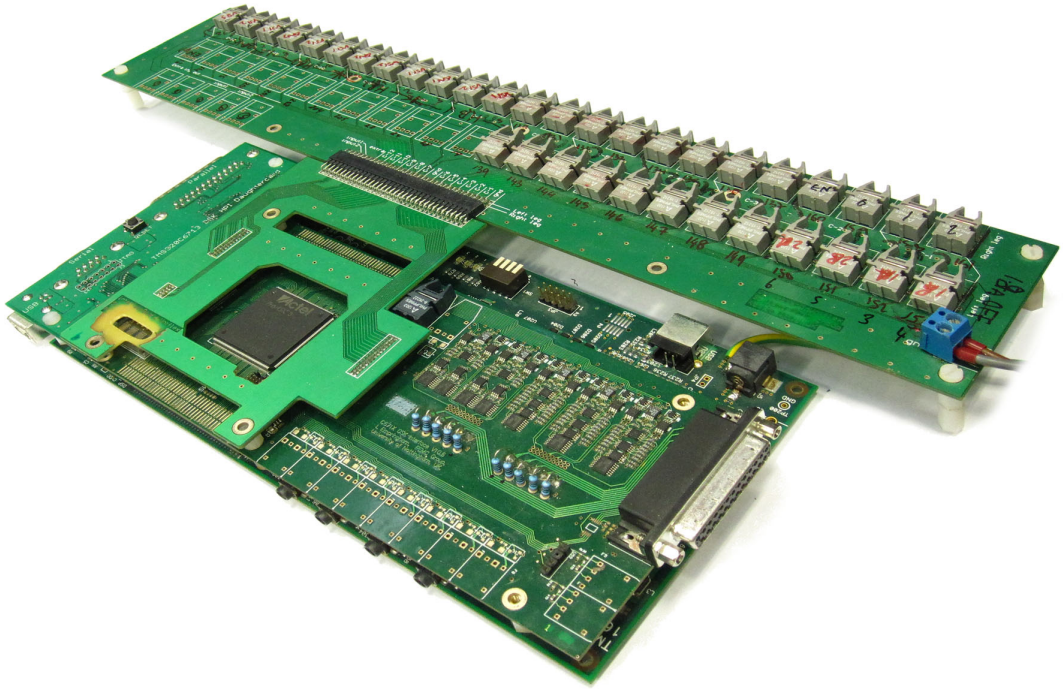


Figure 5.7: FPGA, DSP and optical expansion board

group has designed and manufactures its own FPGA PCB. Figure 5.7 shows the FPGA, DSP and optical expansion board. The FPGA PCB contains 10 12-bit A2D converters and signal conditioning components. Hardware trips are provided via the use of a digital potential divider and a comparator, allowing for an analogue trip point to be set using the DSP via the common memory. This will protect the converter in the case of an over-current in the AC network or an over voltage on the DC link of the Single Phase VSI and auxiliary 3-Phase VSI. A watchdog timer in the FPGA is used to protect the converter in the case of a crash in the main DSP program loop. The FPGA was clocked at 50MHz to allow for very precise control of switching times, particularly for the current build up delay in Mode 3. This is discussed in more detail in Section 5.6.3.

5.6.1 Generation of the Interrupt

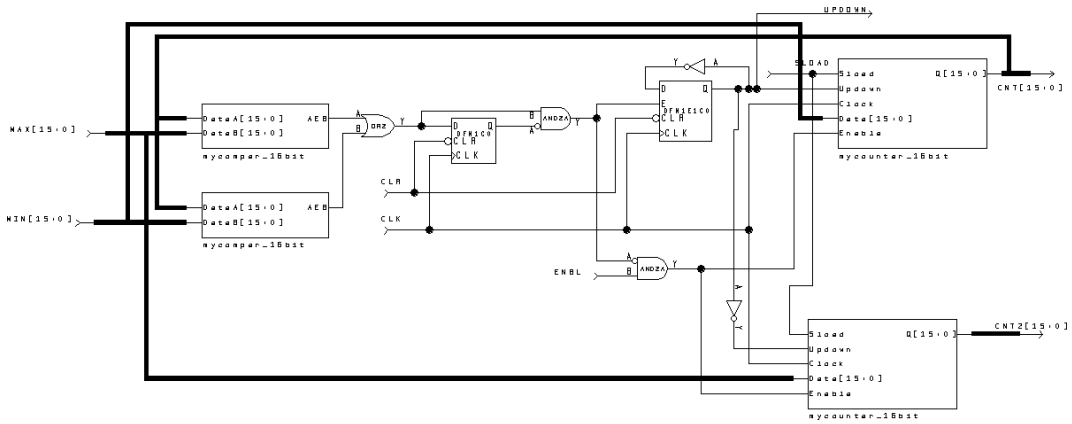


Figure 5.8: Carrier and ISR generation block in FPGA

The Interrupt Service Routine (ISR) is used to trigger the DSP, running the program loop, reading the A2Ds and performing calculations.

The Interrupt is generated using an up/down counter with the direction of the counter reversed when limits are reached. Figure 5.8 shows the FPGA schematic that generates the ISR. MAX and MIN are the limits of the counter set in the DSP. MIN is usually set to 0 and MAX is set to give the required ISR frequency, given a 50MHz FPGA clock frequency. The comparators $mycompar\_16bit$ are used to invert the direction line when the counter output is equal to the counter output (CNT). A rising edge trigger is placed on the direction signal,

$UPDOWN$, connected via a Pulse Stretch block (Shown in Appendix B) and this is used to trigger the interrupt of the DSP. The output of the counter, CNT, is a triangle wave and this is used as one of the carriers for SPWM generation. A complementary counter, connected to the direction line, via an inverter, is used to generate the 90º phase shifted carrier, $CTN2$, required for PWM modulation of the Cycloconverter and VSI.

5.6.2 PWM Generation

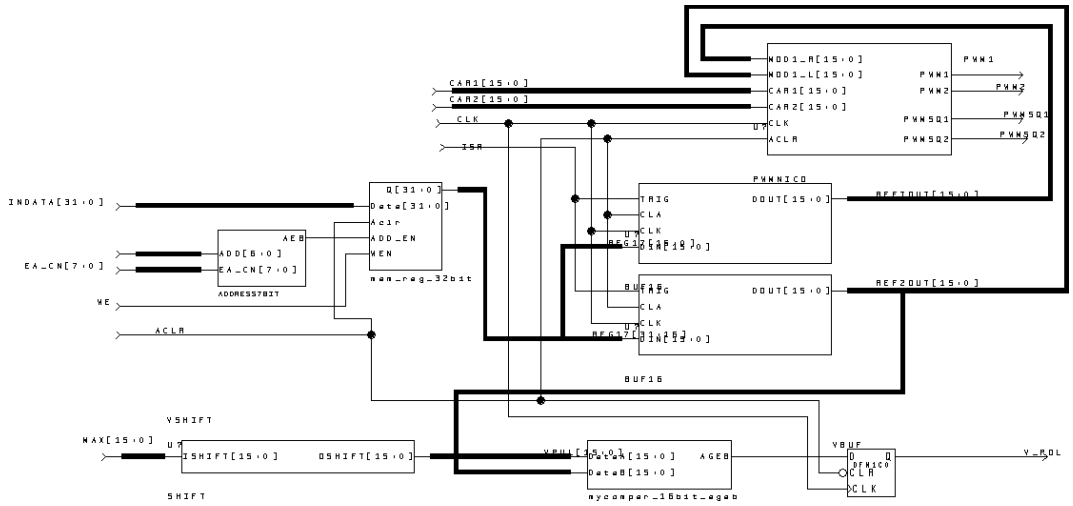


Figure 5.9: PWM generation block in FPGA

A diagram showing the PWM generation block in the FPGA is shown in Figure 5.9. The reference signal from the DSP is first buffered for one ISR period in $BUF16$, to prevent the reference signal from changing at an unspecified time after the DSP has finished performing the calculations for the next set of pulses. An additional buffered reference signals is generated by halving the reference wave, via a bit-shift, to generate a second set of pulses half the width of the first. This is to generate the 3 pules required for the Modulation Technique 3, described in Chapter 6. The PWM signals are then generated by comparing the two triangle wave carriers, $CAR1$ and $CAR2$, against the buffered reference wave, $REF1OUT$ and $REF2OUT$. The polarity of the voltage, required to establish the correct mode for the Cycloconverter and VSI modulation, Section 5.6.3, is also calculated in this FPGA block. It is calculated by comparing the buffered reference signal from the DSP against half the maximum up/down counter limit.

The PWM pulses for the 3 Phase VSI are generated in an additional FPGA block shown in Appendix B using one triangle wave carrier compared against the 3 reference signals from the DSP. This gives a set of 3 PWM pulses, one for each phase of the converter.

5.6.3 Cycloconverter and VSI Modulation

Each Cycloconverter and associated VSI operate under 3 modes of operation. The first mode, Mode 1 is the unknown current mode when the polarity of the current is too low to be determined. The second mode, Mode 2 is when the AC current has the same polarity as AC voltage. The third mode, Mode 3 is when the AC current has an opposite polarity to the AC voltage. The polarity of the voltage and current is calculated at the start of each ISR. The voltage polarity is calculated directly in the FPGA, shown in Figure 5.8, and the current polarity is calculated in the DSP and transferred to the FPGA via the common memory interface. During the time between pulses, all switches in the Cycloconverter are switched on, allowing the free-wheeling current to reverse if necessary.

To reduce the effect of the on-board dead time, this modulation strategy switches the VSI 1 and 2 signals at the start of the ISR but the VSI enable line is held low until the start of the PWM pulse. As the dead time is only added to the switching of the VSI 1 and 2 signals, and not the Enable signal, this results in one less dead time delay per ISR period.

Figure 5.10 shows the Cycloconverter and VSI modulation block in the FPGA. The Cycloconverter outputs are $1A$, $2A$, $1B$, $2B$ and the VSI outputs are $VSI1$, $VSI2$ and VSI_{EN}. $IPOS$ and $INEG$ are the positive and negative current polarity signals from the DSP. When both are 0, the current is below the threshold and the converter will be operating in Mode 1. $VPOL$ is the voltage polarity signal and $PWM1$, $PWM2$, $PWMSQ1$ and $PWMSQ2$ are the PWM generation block outputs, as shown in Figure 5.9. $DELAY$ is the delay time allowed for commutation to occur in Mode 3. EN is the enable line, CLK is the 50MHz clock and $ACLR$ is the reset signal used during the initialization of the FPGA. In the following section the operation of this block will be described in a high level due to the complexity of the operation of this block.

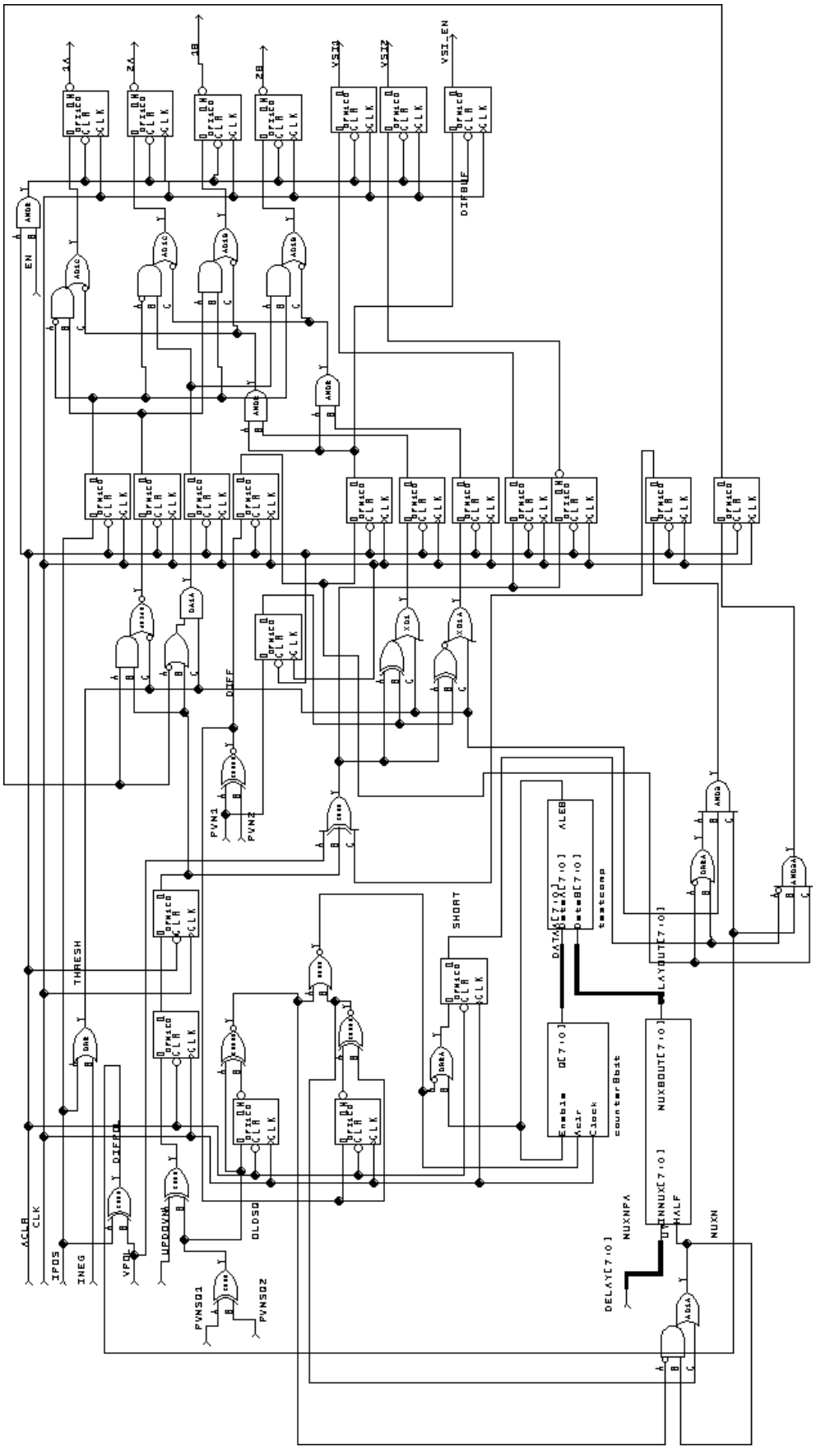


Figure 5.10: Cycloconverter and VSI modulation block in FPGA

Figures 5.11 - 5.13 show the experimental Cycloconverter and VSI FPGA switching signals and associated AC voltages and currents. VSI1 is the first leg of the VSI. The second leg of the VSI is the inverse of this signal. VSI EN is the VSI enable line. 1A, 1B, 2A and 2B FPGA switching signals are connected to the Cycloconverter IGBTs as shown in Figure 5.5.

Operation in Mode 1

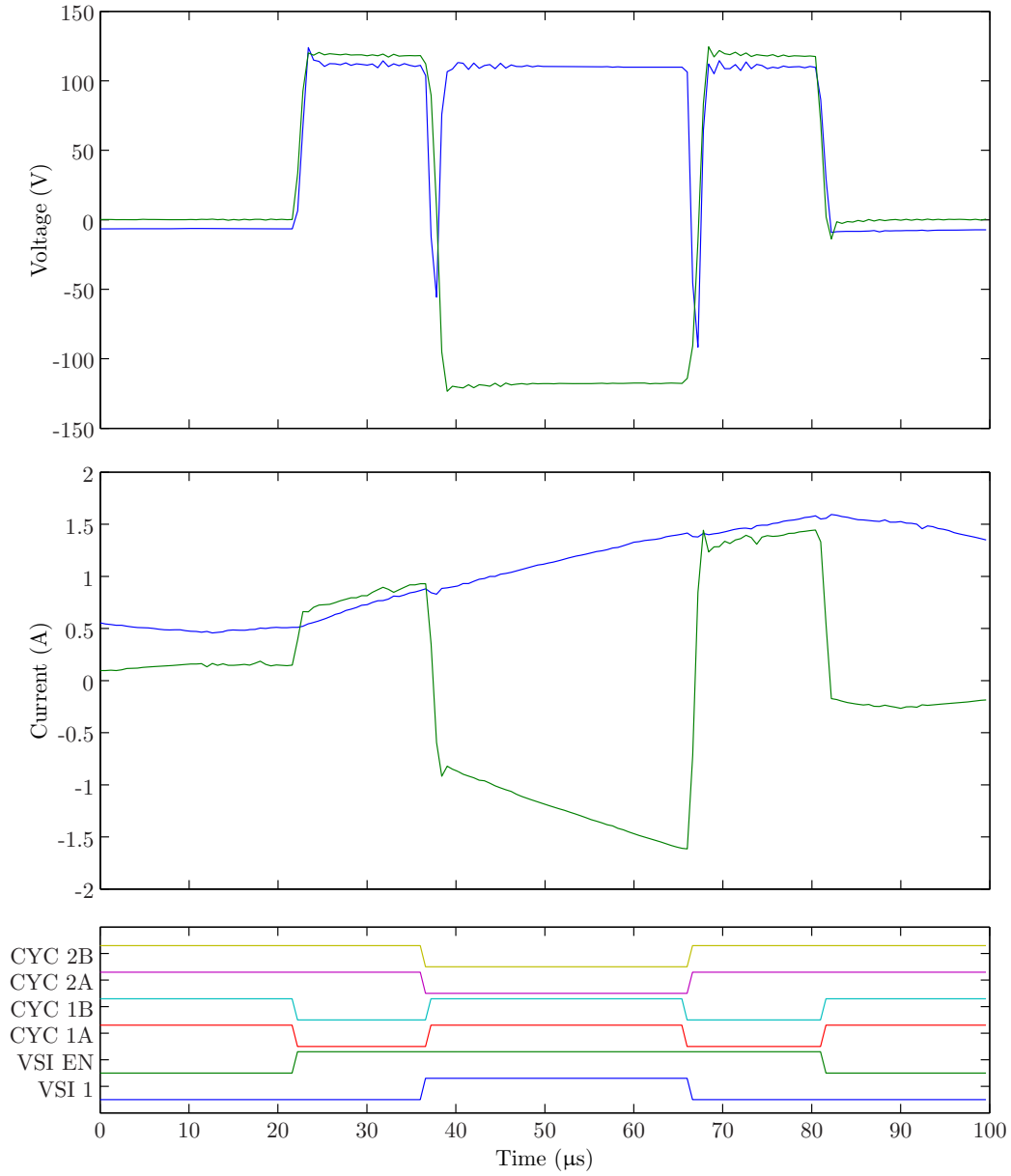


Figure 5.11: Cycloconverter Mode 1: Unknown Current. Blue waveforms u_u and i_u. Green waveforms u_{pri} and i_{pri}

Figure 5.11 shows the FPGA signals and current and voltage waveform when the converter is operating in Mode 1. In this mode 1A and 1B Cycloconverter signals are switched simultaneously when rectifying in one direction and 2A and 2B are switched simultaneously when rectifying in the other. When operating in this mode, commutation relies on the clamp circuit of Section 5.7.1 to protect the devices from voltage spikes from the mismatch of currents in the leakage inductance in the transformer and the AC line inductor. However this mode should only be operational for a small amount of time, when the current is changing polarity, and as such the losses from this mode are minimal over the whole of one 50Hz cycle. This mode is also only operational when the current is at a low value, minimizing the energy contained in the over voltage spike.

Operation in Mode 2

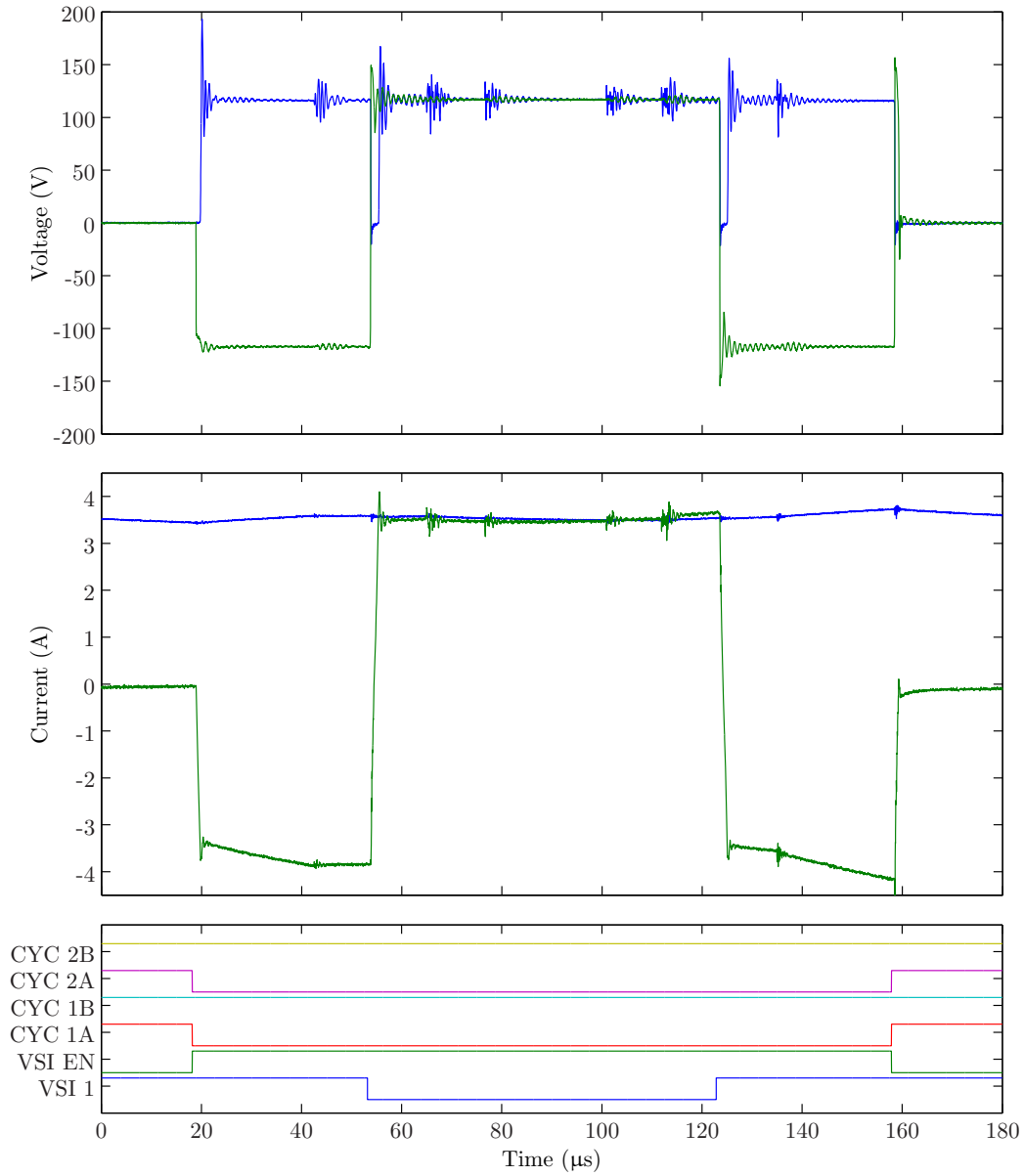


Figure 5.12: Cycloconverter Mode 2: same polarity voltage and current. Blue waveforms u_u and i_u. Green waveforms u_{pri} and i_{pri}

Figure 5.12 shows the FPGA signals and current and voltage waveform when the converter is operating in Mode 2. In this mode 1A and 2A are turned on when the current is flowing in one direction and 1B and 2B when the current is flowing in the other direction. In this mode of operation commutation is performed by the anti-parallel diodes resulting in Zero Voltage Switching (ZVS) and minimal clamp currents.

Operation in Mode 3

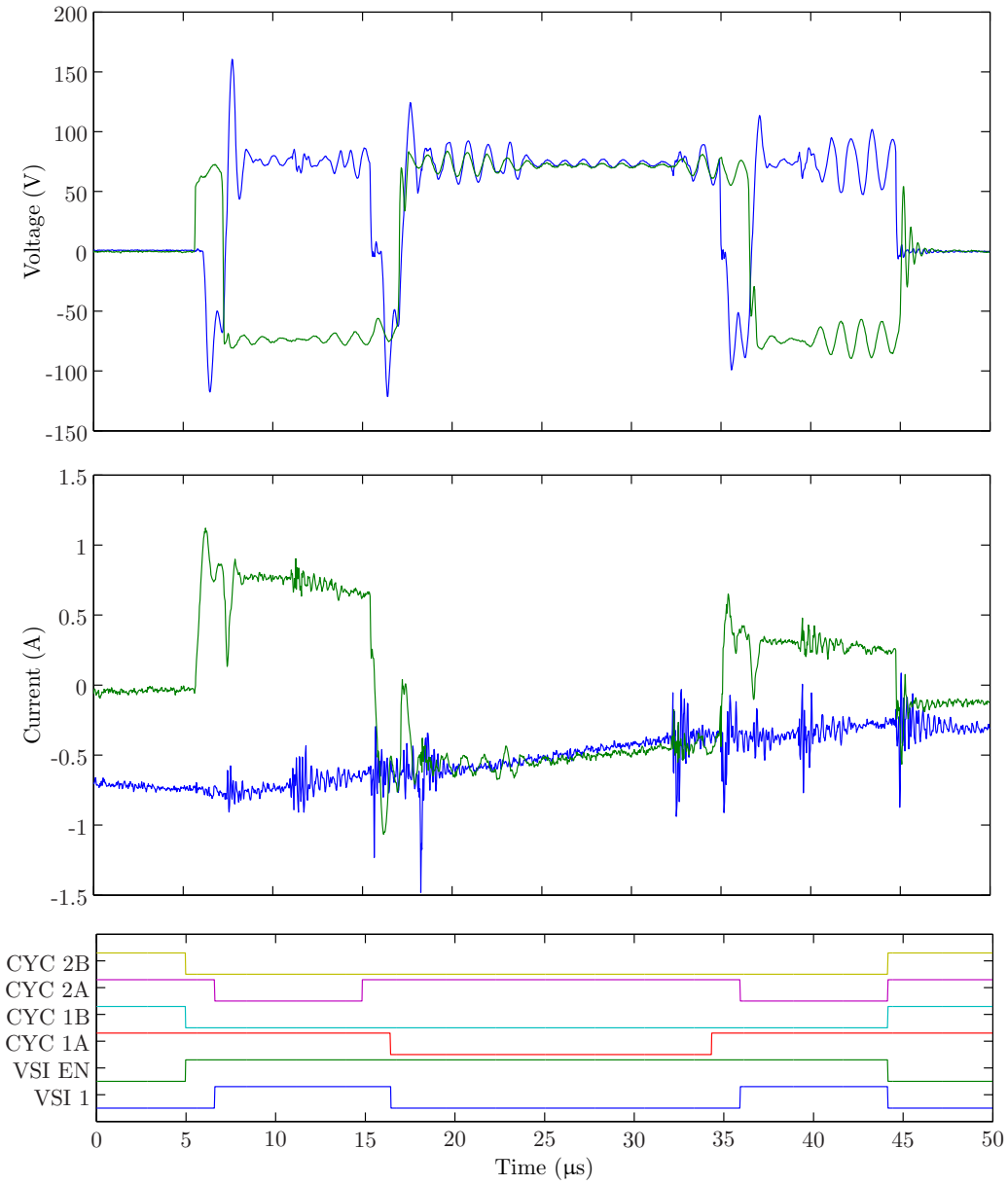


Figure 5.13: Cycloconverter Mode 3: different polarity voltage and current. Blue waveforms u_u and i_u. Green waveforms u_{pri} and i_{pri}

Figure 5.13 shows the FPGA signals and current and voltage waveform when the converter is operating in Mode 3. For the first pulse a reverse voltage is applied by the VSI, with the commutation is performed in the Cycloconverter by the anti-parallel diodes as in Mode 2 (1A, 2A). After the commutation has occurred current polarity is fixed by turning off the 2 IGBTs that are not conducting (2A) and the correct polarity pulse is applied by VSI 1. This process is inverted for the

second pulse and repeated for the third. The time allowed for commutation to occur is calculated in the DSP based on the AC current and the estimated time required to build up this current in the leakage inductance of the transformer, given the DC voltage and inductance value. Some overhead is given to allow for the switching of the IGBTs and the additional dead time in the VSI. An excessive dead time value will result in a significantly reduced MI available from the converter, whereas a too low value for the commutation time will result in the current falling to zero and the energy contained in the AC inductor being transferred into the clamp circuits, due to there no longer being a current path.

5.7 Protection Circuits

5.7.1 Overvoltage Protection

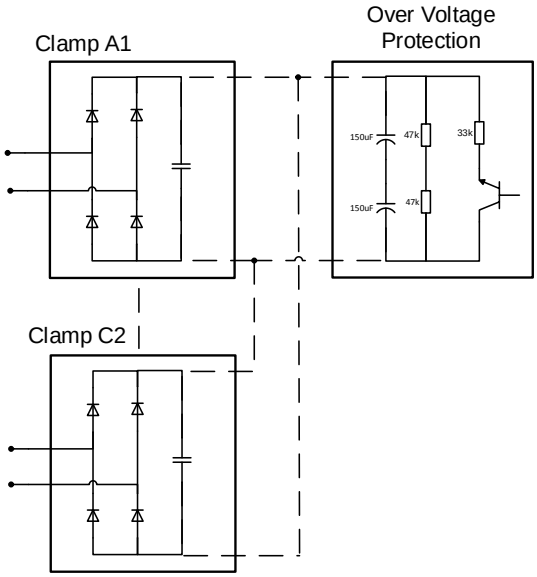


Figure 5.14: Clamp Schematic Diagram

Voltage clamp circuits at the input and output of the Cycloconverter and are employed in the converter as shown in Figure 5.1. A Common issue with a Cycloconverter topology is an over reliance on a clamp circuit to perform commutation, placed between the Cycloconverter and AC inductor, labelled A2, B2 and C2. The implemented switching strategy was specifically designed to reduce

over voltage spikes by ensuring that the transformer current is equal to the AC current as commutation occurs. The clamp circuit should therefore only be required for commutation when the current polarity is unknown (Mode 1). During testing the voltage of the clamp circuit was recorded to ensure that this was the case. The clamp circuit is constructed from a bridge rectifier and capacitor for storing the energy from the clamp circuit. An over voltage protection circuit is used to prevent the capacitors from an over voltage by switching on a dump load resistor when the voltage rises above 850V.

In the event of a hardware trip, on the Enable Loop (see Section 5.7.2) or in the FPGA, the current in the leakage inductance on the Cycloconverter side of the transformer would no longer have a current path and this could lead to the destruction of the IGBTs in the Cycloconverter. To prevent this from occurring additional clamp circuits, A1, B1, C1, was placed across the Cycloconverter side of the transformer in order to absorb the stored energy in the case of a trip. All of the clamp circuits share a common over voltage protection circuit, as shown in Figure 5.14. During normal operation this clamp circuit should not have any affect on the operation of the converter.

5.7.2 Overcurrent Protection

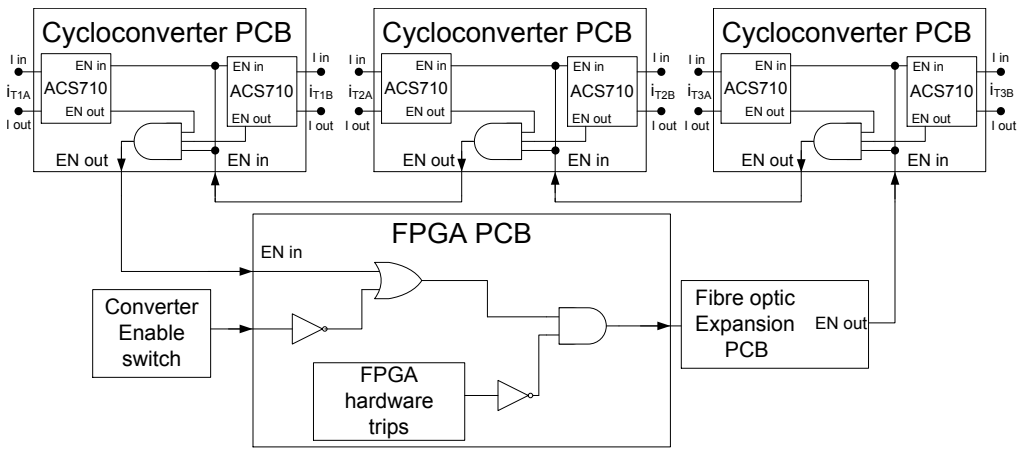


Figure 5.15: Enable Loop block diagram

To protect the Cycloconverter and Single Phase VSI PCBs from over currents due to transformer saturation an additional protection circuit, an Enable Loop

was used. An enable loop is used to allow for a large number of over-current sensors whilst requiring only one optical receiver and one optical transmitter on the FPGA. ACS710 hall effect current sensors are connected to both the primary and secondary windings of each transformer and have an over-current threshold set at 30A. In Figure 5.1 at the start of this chapter these current sensors are labelled i_{T1A}, i_{T1B}, i_{T2A}, i_{T2B}, i_{T3A} and i_{T3B}.

If any of the current sensors connected to the Enable Loop detect a current higher than the over-current threshold, the sensor will trip, pulling the EN out line of the respective Cycloconverter Control PCB low. Figure 5.15 shows a block diagram of the Enable Loop. The Enable Loop is connected in such a way as that the signal travels from the FPGA using one of the fibre optic outputs from the optical expansion board, to all 3 Cycloconverter Control PCBs in turn, via the EN in and EN out fibre optic connectors, before returning back to the FPGA via an optical connector mounted directly on the FPGA board. A switch is connected to the FPGA that is used to enable and disable the converter. When this enable switch is off and the converter is disabled, the FPGA Enable Loop Out signal becomes high, allowing the over current protection circuitry to be reset. When the enable switch is turned on, the PWM signals are enabled and the Enable Loop signal from the FPGA will only remain high provided the Enable Loop in signal is high, indicating that none of the Cycloconverters have tripped.

5.8 Summary

This chapter has documented the design and construction of the experimental converter that will be used to validate the simulation work. The design of the VSI, 3 Phase VSI and Cycloconverter was described. The excessive voltage rating of the VSI and auxiliary 3-Phase VSI was discussed with the justification being the possibility of future Medium Voltage testing.

The operation of the analogue sensors used to control the converter were discussed along with the modulation strategy of the Cycloconverters and VSI for all 3 modes of operation. The techniques used to implement this modulation strategy in the FPGA were described as well as the protection circuitry, used to protect the

converter in the case of an over-current or over-voltage fault.

The construction of the clamp circuit used to perform modulation in Mode 1 and the additional clamp circuit to protect the converter in the case of a trip was described before finally describing the Enable Loop, an additional protection circuit to prevent over-currents from transformer saturation from damaging the converter.

The voltage rating of the auxiliary 3-Phase VSI was 600V, significantly higher than the 100V DC link voltage required by the converter topology resulting in increased switching times and losses. A future improvement to the converter would be to utilize 160V MOSFETs instead but this would require a redesigned auxiliary 3-Phase VSI PCB.

For the initial construction, clamp circuits were placed only on the AC side of the Cycloconverter but this resulted in the destruction in one of the switching devices after an over current trip on the Enable Loop. A future modification to the Cycloconverter would be to incorporate the clamp circuits directly on the Power PCB in order to reduce the current loop area, reducing the voltage overshoots when the clamp circuit facilitates commutation.

The voltage rating of the converter is limited by the voltage rating of the clamp circuit; the capacitors are rated at 450V each, resulting in a maximum clamp voltage of 850V. Oscillations caused by reverse recovery of the Cycloconverter diodes and the resonance between the diode parasitic capacitance and the leakage inductance in the transformer result in voltage overshoot of 15% or more. To prevent the clamp circuit over voltage protection circuit dissipating excessive energy, this limits the DC link voltage to around 360V. This in turn limits the AC voltage to approximately 200V RMS due to the requirement of a significant overhead in MI when the modulation of the converter is operating in Mode 3, to compensate for the delay time to perform commutation.

Chapter 6

Transformer Design and Simulation

This chapter will describe the selection of the transformer core and the winding materials, followed by the design of the experimental transformer. This chapter will then document a simulation of the transformer core to compare the three modulation techniques for the Cycloconverter and the Hybrid Cycloconverter and a benchmark 50% modulation technique. These modulation techniques have been introduced in Chapter 2. A comparison of the performance of each modulation technique and converter will be made. The comparative criteria will be the minimization of peak flux density, minimization of magnetizing current and minimization of core loss.

This chapter will then conclude with a justification for the selected modulation technique used for the experimental converter.

6.1 Core Materials

The transformer for the Cycloconverter Topology is designed for operation at a switching frequency greater than 10kHz. To minimize core eddy current losses the core material has to have a high electrical resistance. Ferrite and Metglas Amor-

phous Metal cores are two suitable materials. Ferrite cores are constructed from a non-conductive iron oxide and exhibit negligible eddy current loss. However Ferrite cores have a low flux density before saturation, 0.3-0.5T, have significant hysterisis loss and have a highly non-linear BH curve, as shown in Figure 6.1. This results in a core with a greater number of windings and higher magnetizing current at higher flux densities, increasing the magnetizing current losses.

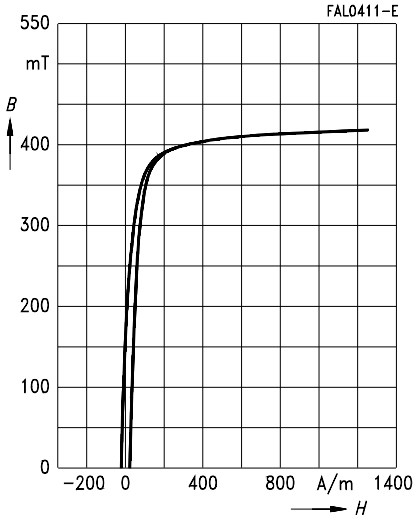


Figure 6.1: BH curve of N27 Ferrite at 100°C, from [65]

Amorphous Metal cores have a much higher flux density before saturation, 1.3-1.5T, however this material has some electrical conductivity. This core material is therefore not recommended for very high frequency operation, > 10kHz [66]. The high switching frequency of the converter resulted in the selection of Ferrite as a core material. The ferrite core was an N27 material, selected from the recommendations in [67] for a power transformer operating at 10-100kHz. The transformer was designed to operate near the point of saturation to keep the transformer core size to a minimum thereby maximizing the power density of the converter.

6.2 Winding Materials

The winding area of the transformer needs to be large enough to accommodate the required number of turns with a suitably large conductor, minimizing the

conduction losses. The thickness of the copper should be less than twice the skin depth at the frequency of operation in order to ensure that the conductor is fully utilized. The skin effect is the result of eddy currents in the conductor interfering with the current flowing down the wire, leading to reduced currents in the centre of the wire and increased currents on the surface [68]. The skin depth is an approximation dictating the depth at which the material will no longer have any significant contribution to the current handling capacity of the conductor.

The skin depth, δ, is calculated using the equation:

$$\delta = \sqrt{\frac{\rho}{\pi f \mu}} \tag{6.1}$$

Where ρ is the resistivity the conductor, which is $1.68 \times 10^{-7}\Omega$m for copper, and μ is the absolute permeability, $4\pi \times 10^{-7}$H/m. This equation gives a skin depth for copper wire of 0.5mm at 15kHz.

Copper foil and Litz wire both have a large surface area relative to cross sectional area and can be used if the required diameter of a copper conductor is greater than twice the skin depth of traditional winding wire. Copper foil has large surface area compared with the volume and therefore will have an even current distribution, provided the thickness of the foil is less than double the skin depth. Litz wire is a collection of individually isolated strands woven in such a way to evenly distribute the current in each of the strands, negating both the skin and proximity effects.

The current waveform of the transformer is a trapezoidal shape, containing higher frequency harmonics in addition to the fundamental. The most significant current harmonics are the 3^{rd}, 5^{th} and 7^{th}. These current harmonics will have a smaller corresponding skin depth than the fundamental and therefore the conductor radius should be approximately five times smaller than the calculated skin depth of the fundamental.

For a high power transformer operating at below 20kHz, the minimum transformer core cross sectional area is governed by the maximum allowable flux den-

sity for a given magnetic material, as the core losses will not be a limiting factor. Core saturation occurs when all of the magnetic regions have aligned and it is no longer possible to increase the magnetic flux in the material any further. Once a core has reached a point of saturation the core material will no longer contain any increase in the magnetic in flux; this will increasingly leak into the air surrounding the core, which is subject to a much lower permeability (μ).

The net result is a significant reduction in magnetizing inductance. Once the core becomes saturated the magnetizing current can quickly reach a dangerous level, often before any protection circuitry has come into effect. To reduce this over current, an air gap can be added to the core. The air gap has a powerful demagnetizing effect by shearing over the hysteresis loop [69]. This will result in a core with a greater magnetizing current during normal operation but significantly reduced lower magnetizing current under saturated conditions. The demagnetizing effect of an air gap will also reduce the chance of saturation from asymmetrical voltage waveforms and is an industry standard for inverter driven HF transformer design.

The core material is an expensive, large and heavy item. The low saturation flux density of Ferrite N27 means that to prevent saturation the core has to be considerably larger in volume compared to other materials for a given flux. The high electrical resistance of the core means that the eddy current losses are almost zero. The resulting core is heavy, large and an expensive component in the converter that has relatively low losses. A reduction in size of the core of the transformer, without allowing saturation will significantly increase the competitiveness of a converter topology and the increase in core losses will have a minimal impact on the total losses in the converter.

6.3 Design of the High Frequency Transformer

The transformer is designed to have a 1:1 turns ratio. The number of turns and core cross sectional area is designed using the Steinmetz parameters of the core material to give a maximum flux density, B_{max}, of 0.4T when a 5kHz, 400V, 50% duty cycle square wave is applied to the primary winding of the transformer, u_{pri}.

The Steinmetz parameters however can only give an estimate of core losses and peak flux density and it was decided that a further simulation should be carried out with a more detailed transformer model in order to more accurately predict core losses, magnetizing current and flux density for a complex waveform shape.

The number of turns required for the transformer is calculated using:

$$N = \frac{u_{pri}}{B_{max} 4 A_e f} \tag{6.2}$$

Where u_{pri} is the amplitude of the square wave voltage applied to the primary winding of the transformer and A_e is given in the transformer datasheet as 840mm^2. Using this equation gives N, the primary (and secondary) turns equal to 60.

Figure 6.2: Photograph of an assembled transformer

Figure 6.2 shows a photograph of one assembled transformer and Figure 6.3 shows a diagram of the transformer and windings. The core was constructed from an "U" and "I" Ferrite N27 sections with a 0.2mm air gap between the two

sections, giving a total air gap of 0.4mm. A sectionalized approach is used for the windings, where the primary winding is split in two and wound on either side of the secondary winding, to reduce the leakage inductance of the transformer. For each transformer, two coils are wound, mounted on each leg of the core. Each coil is wound with 15 primary turns first followed by 30 secondary turns and finally another 15 primary turns. This gives a total of 30 primary and secondary turns on each coil and the coils are connected in series, giving a total of 60 primary and 60 secondary turns.

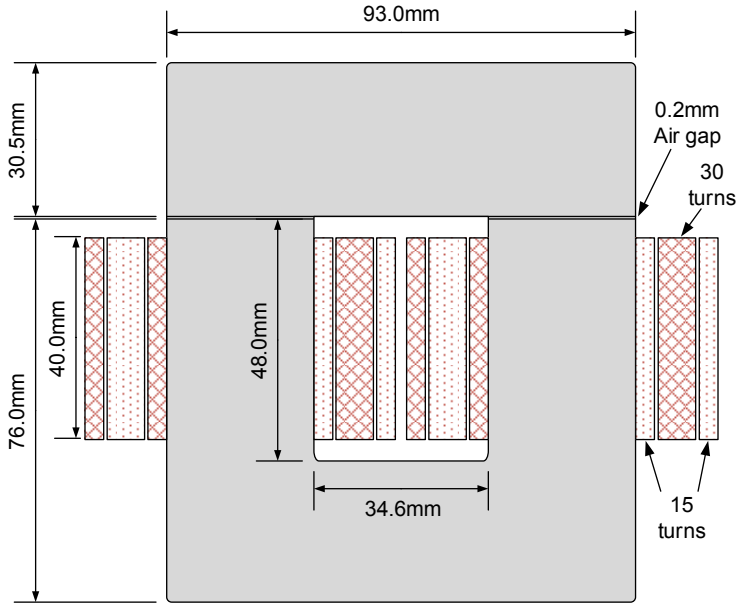


Figure 6.3: Transformer Design Schematic, scale = 2:3

A copper foil conductor with a width of 40mm and a thickness of 0.15mm was selected to fill the winding area of the transformer, whilst allowing room for insulation between the windings and external connectors. Copper foil was selected for the transformer due to lower cost and ease of construction when compared with Litz wire. An open circuit and short circuit test was performed on the transformers and the results from one transformer are shown in Figures 6.4, 6.5 and 6.6 with the raw data presented in Appendix C.

Figure 6.4 show the electrical resistance of the core increases almost linearly with frequency up until 40kHz. This justifies the conductor profile selected for the transformer and the electrical resistance of the core will allow the conductor losses in the core to be at a minimum value.

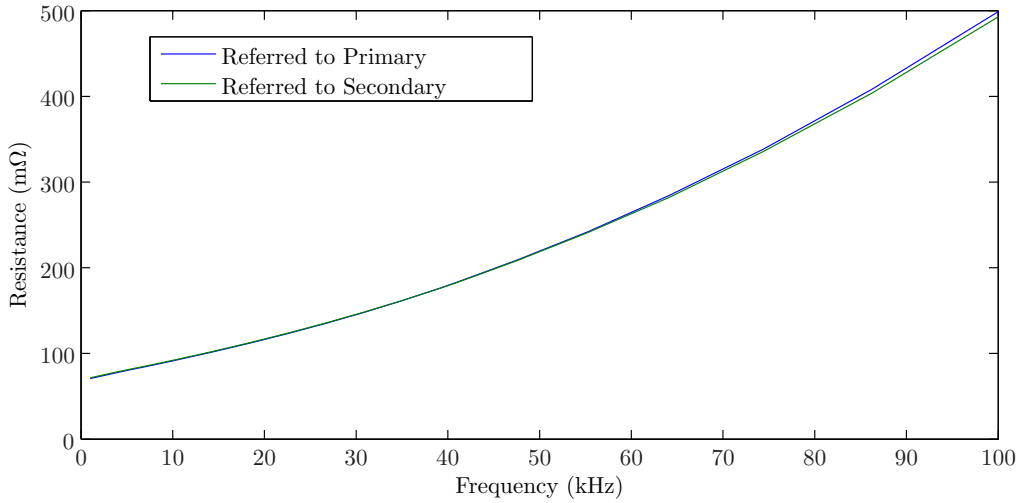


Figure 6.4: Electrical Resistance of an Assembeld Transformer

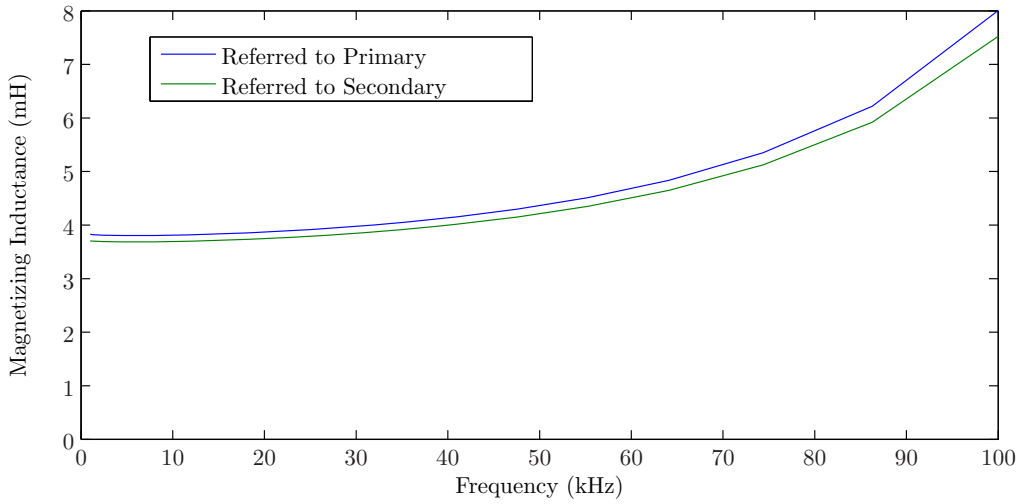


Figure 6.5: Magnetizing Inductance of an Assembeld Transformer

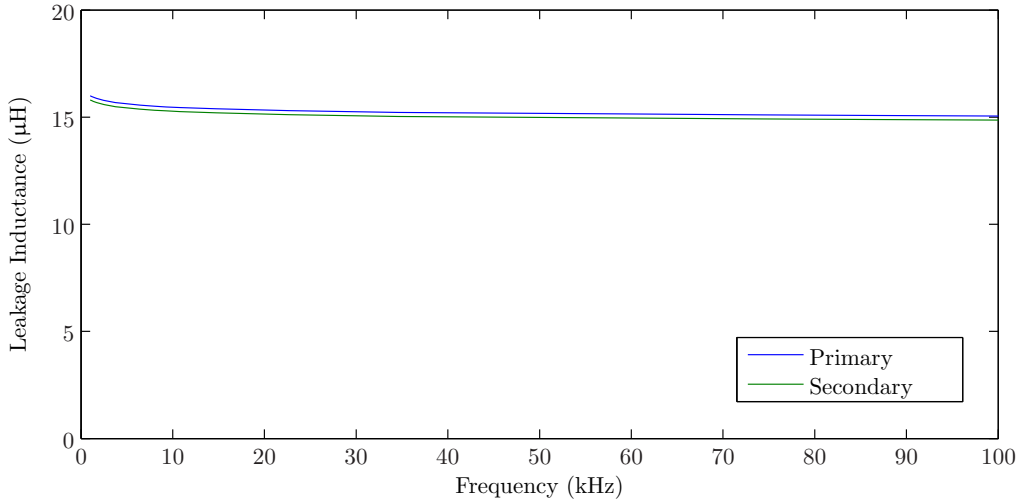


Figure 6.6: Leakage Inductance of an Assembeld Transformer

Figure 6.5 shows the magnatizing inductance of the core and shows it has a value of 3.7mH at the frequency of operation of the converter. Figure 6.6 shows the leakage inductance of the converter and shows it has a value of 15μH at the frequncy of operation of the converter.

6.4 Simulation of Core Flux Density, Magnetizing Current and Core Losses

The purpose of the simulation is to establish the peak flux density for the Cycloconverter and Hybrid Cycloconverter Topologies with a comparison of the modulation techniques described in Chapter 3 in order to justify the modulation technique used for the final converter. The simulated modulation techniques are a 50% duty cycle square wave, Modulation Technique 1, Modulation Technique 2 and Modulation Technique 3. These are defined in Chapter 3, Section 3.2. The simulation will also investigate the core losses and magnetizing current of the transformer for each of the modulation techniques.

To provide a fair comparison between the modulation techniques, the triangle carrier frequency was adjusted for each modulation technique to give 10k switching transitions per second. This resulted in a triangle carrier frequency of 5kHz for Modulation Technique 1 and 2, 3.75kHz for Modulation Technique 3 and a 5kHz 50% duty cycle modulation technique. The DC link of the converters, U_{DC}, was set at 300V and the modulation index was varied to adjust the magnitude of the AC voltage from the converter u_{uvw}. The simulation is carried out with an ideal voltage source connected to the primary winding of the transformer, u_{pri}, and no secondary winding.

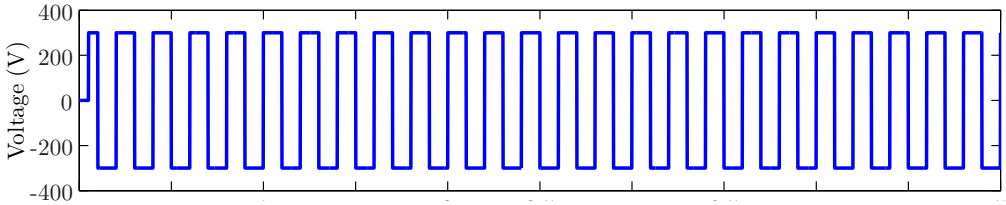
The transformer is modelled using the Magnetic Elements components in PSIM. To simulate the transformer correctly, a test simulation with a square wave voltage source was used to establish and verify the core parameters. The values for the inductance per turns squared, A_L, saturation flux, ϕ_{sat}, the core effective cross sectional area, A_c, the core effective length were obtained from the Ferrite N27 core and material datasheets, while the values for the core coefficients, R, K_1, K_{exp1}, K_2 and K_{exp2} were determined iteratively, as recommended in the

PSIM tutorial document on defining the saturable core element [70]. The core coefficients are used to fit the PSIM model to the B-H curve contained in the core datasheet and do not relate to a specific quantity. The core coefficients K_1 and K_{exp1} correspond to the point of saturation of the core, with K_1 relating to the point at which saturation occurs and K_{exp1} relating to the sharpness of this transition. The core coefficients K_2 and K_{exp2} correspond to the second knee point in the saturation region, with K_2 relating to the point at which this knee poin occurs and K_{exp2} relating to the sharpness of this transition. The core parameters used for simulation are shown in Appendix A.

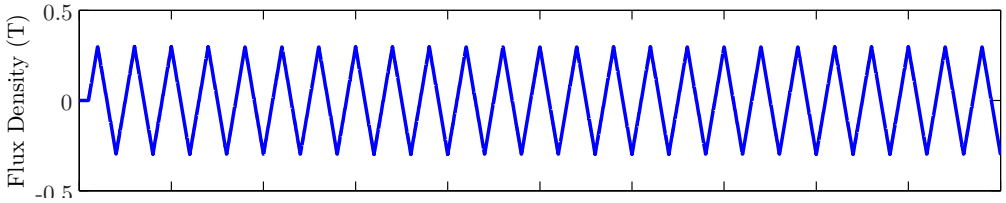
The PSIM documentation does not specify how the core losses are calculated, however it was ascertained from the simulated waveforms that instantaneous core power loss is calculated for every PWM pulse. For each PWM pulse, the value of the magnetic flux density is calculated using a lookup table and the integration of the primary voltage,u_{pri}, using the BH curve of the simulated core. The core loss is calculated by the application of a wave voltage source, proportional to the calculated flux density in the core, to a constant resistance representing the core hysteresis losses, R_{core}. This simulation does not take into account the harmonic content of the applied primary voltage, u_{pri}. This approach is only an approximation as in the experimental converter the core BH curve and losses will be dependent on frequency and as this simulation demonstrates the three modulation schemes for the Cycloconverter and Hybrid Cycloconverter all have identical losses. To correctly simulate core losses the losses for each harmonic need to be calculated from the Steinmetz paramers of the core material.

6.4.1 Modulation Techniques

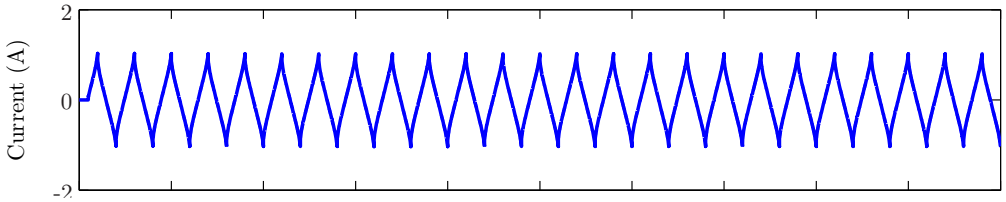
The waveforms from the simulation of the 50% duty cycle modulation technique and the three devised modulation techniques are shown in Figures 6.7, 6.8, 6.9 and 6.10. For each modulation technique the transformer primary voltage u_{pri}, transformer core flux and magnetizing current is shown for $^1/_4$ of a 50Hz cycle for u_{uvw}. The other $^3/_4$ of the 50Hz cycle will show a repeat of the displayed waveforms. A sinusoidal reference waveform is used to generate u_{pri} for the figures, as used for the Cycloconverter Topology. However the simulation was also repeated with the reference waveform for the Hybrid Cycloconverter Topology.



(a) u_{pri} transformer primary voltage

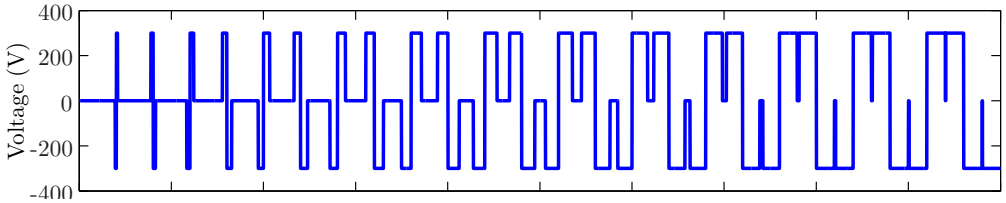


(b) Flux Density

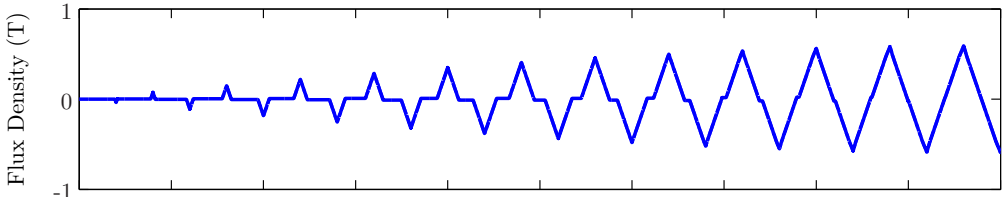


(c) Magnetizing Current

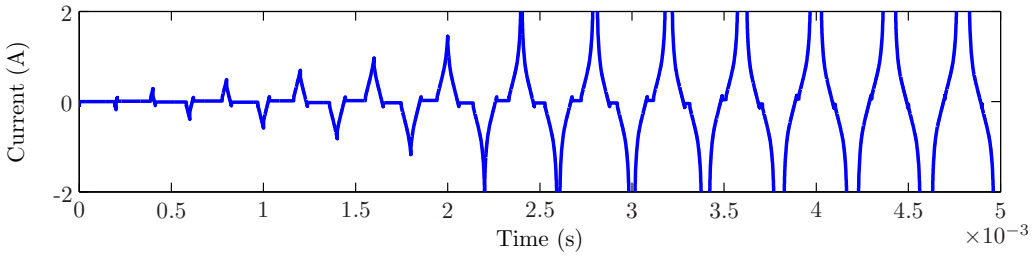
Figure 6.7: 50% Duty Cycle



(a) u_{pri} transformer primary voltage

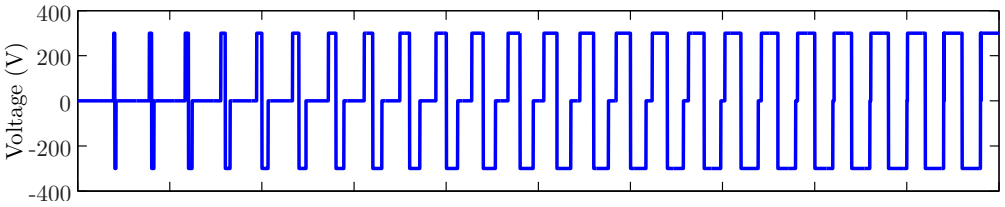


(b) Flux Density

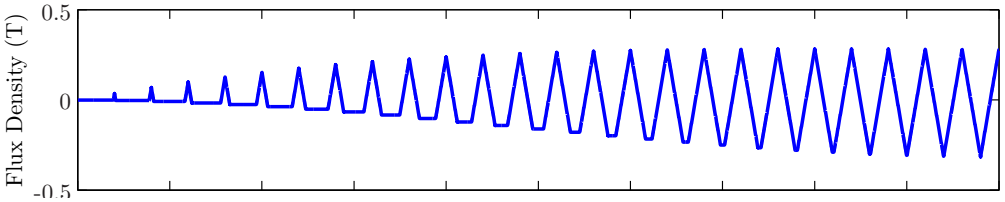


(c) Magnetizing Current

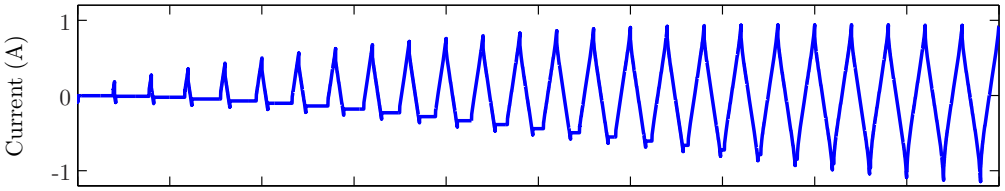
Figure 6.8: Modulation Technique 1, $u_{uvw} = 212$V



(a) u_{pri} transformer primary voltage

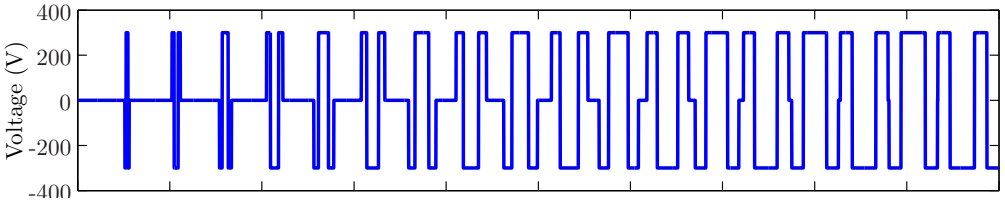


(b) Flux Density

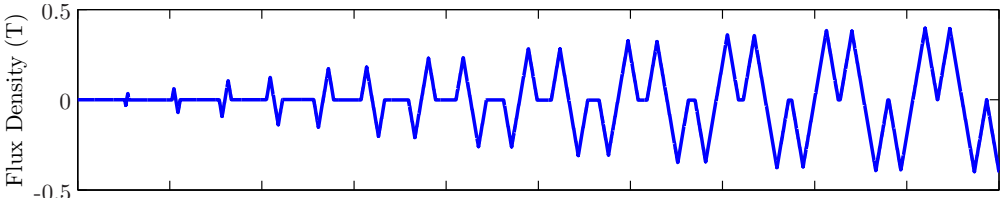


(c) Magnetizing Current

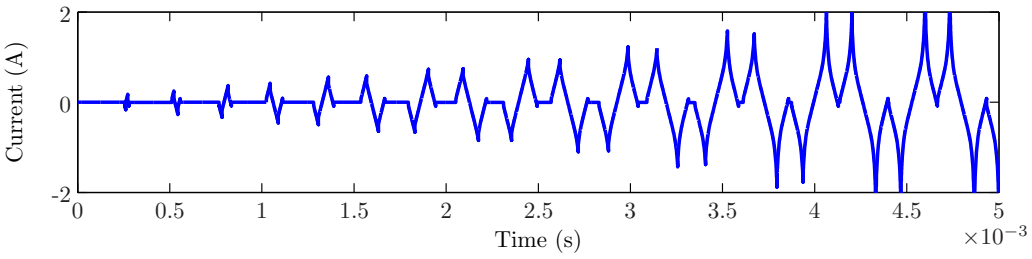
Figure 6.9: Modulation Technique 2, $u_{uvw} = 212$V



(a) Modulation Technique 3 u_{pri} transformer primary voltage



(b) Flux Density



(c) Magnetizing Current

Figure 6.10: Modulation Technique 3, $u_{uvw} = 212$V

The amplitude of u_{uvw} used for the figures was 212V RMS, corresponding to a MI of 1.

The benchmark 50% duty cycle modulation technique waveforms are shown in Figure 6.7. The 50% duty cycle modulation technique operates by applying a constant duty cycle square wave to the primary winding of the transformer, u_{pri}, with the Cycloconverter used to create the 3-Phase AC PWM waveform. The voltage waveform applied to the primary winding of the transformer is shown in Figure 6.7(a). This modulation technique has a flux density, Figure 6.7(b), magnetizing current, Figure 6.7(c) and core losses that is independent of the instantaneous magnitude of u_{uvw}, and instead are only related to U_{DC} and the frequency of the square wave.

The waveforms for Modulation Technique 1 are shown in Figure 6.8. Modulation Technique 1 alternates each set of u_{pri} PWM pulses with each set of PWM pulses producing flux with a polarity opposite to that of the previous set of PWM pulses. This results in a doubling of the maximum peak to peak flux density value over two PWM pulses compared with the 50% duty cycle modulation technique. The core flux waveform is shown in Figure 6.8(b). From the magnetizing current waveforms, Figure 6.8(c), it can be seen that the core has started to saturate with this modulation technique and the peak magnetizing current is considerably greater than 2A. This modulation technique will require a core with twice the area compared with the benchmark 50% duty cycle modulation technique and therefore does not fulfil the requirements of this converter.

An improvement to this modulation technique with regard to peak flux density, Modulation Technique 2 does not reverse every second set of pulses. The waveforms for Modulation Technique 2 are shown in Figure 6.9, with the transformer primary voltage waveform shown in Figure 6.9(a). This modulation technique achieves a reduction in peak to peak flux, Figure 6.9(b), but this modulation technique has an asymmetrical flux waveform 6.9(b) which can result in a net DC component in flux after a complete 50Hz cycle.

It was decided that for an experimental converter the risk of saturation from the asymmetrical flux of Modulation Technique 2 was too great. Any discrepancy in switching times of the H-Bridge legs or any voltage pulses from the recovery of the

magnetizing current energy would always have the same polarity. These pulses would result in additional flux being summed in the transformer core, leading to a DC component and saturation after a number of PWM pulses.

The waveforms from Modulation Technique 3 are shown in Figure 6.10. Modulation Technique 3 splits each PWM pulse into three, one $^1/_4$ positive, one $^1/_2$ negative, one $^1/_4$ positive and reverses the polarity of every other PWM pulse, as shown in Figure 6.10(a). This modulation technique has a symmetrical flux waveform with zero DC offset, Figure 6.10(b) and has a lower peak flux value compared with Modulation Technique 2. This modulation technique also shows signs of core saturation in the magnetizing current waveform 6.10(c). For the experimental converter the triangle carrier frequency will be 5kHz, instead of 3.75kHz for this simulated modulation technique. This will result in increased switching losses, however core saturation will be prevented even when operating with an MI of 1.

6.4.2 Cycloconverter Topology Transformer Simulation Results

Figures 6.11, 6.12 and 6.13 show the results from the simulation of the transformer core for a range of modulation techniques for the Cycloconverter Topology. Figure 6.11 shows the peak flux density in the core of the transformer, Figure 6.12 shows the RMS magnetizing current for the transformer core and Figure 6.13 shows the transformer core power losses, averaged over one cycle.

Figure 6.11 shows the results from the simulation of the peak flux density in the transformer core for the Cycloconverter Topology. The 50% duty cycle modulation technique has a constant peak flux density of 0.3T. The value of u_{uvw} does not affect the transformer primary voltage with this modulation technique, as the PWM is generated by the Cycloconverter and u_{pri} has a constant duty cycle.

Modulation Technique 1 has a constant relationship between peak flux density and AC voltage, with a peak flux level of 0.6T when modulating 212V RMS for u_{uvw}. This peak flux density is twice the peak flux of the benchmark 50% duty

cycle modulation technique. Modulation Technique 2 has a maximum flux density of 0.31T when modulating at 212V RMS for u_{uvw} and due to the unsymmetrical nature of the flux waveform, Figure 6.9(c), when modulating higher amplitude voltages for u_{uvw}, the rate of increase in peak flux with respect to u_{uvw} is reduced.

Modulation Technique 3 has a linear relationship between peak flux and u_{uvw}, that is greater than the peak flux of Modulation Technique 2 due to the lower frequency of the triangle carrier wave used for modulation.

Performing the transformer simulation highlighted the importance of the DC component in flux. A 50% duty cycle square wave modulation technique will inherently have a zero DC component in flux under steady state operation, provided that the switching transistors are identical. However if a soft start technique is not implemented the first pulse will result in a DC offset in flux, potentially leading to saturation of the core, as the peak in magnetic field strength will be twice the steady state value. This DC offset will gradually fall to zero from the dampening action of the winding resistance. The addition of an air gap into the core will result in lower saturation current and a demagnetizing effect resulting in the shearing over of the hysteresis loop [69]. This will however only compensate for a small DC component, for example from differences in the performance of the switching devices, and a soft start technique will still be required to prevent saturation, where the first pulse has a duty cycle of half the subsequent pulses. This is shown in Figure 6.7(a).

For the Cycloconverter Topology, Modulation Techniques 1 and 3 provide inherent cancellation of any DC offset and do not have any soft starting requirements. Modulation Technique 2 was found to result in a 50Hz component in flux that even in simulation resulted in a significant DC component in flux after a number of 50Hz cycles.

Figure 6.12 shows the results from the transformer core simulation for the RMS magnetizing current for the Cycloconverter Topology. The 50% duty cycle modulation technique has a constant value of magnetizing current of 0.5A RMS for the Cycloconverter Topology. Modulation Technique 1 and 3 show a greater increase in magnetizing current at high values of u_{uvw} due to the saturation of the core. Modulation Technique 2 has a linear relationship between magnetizing current

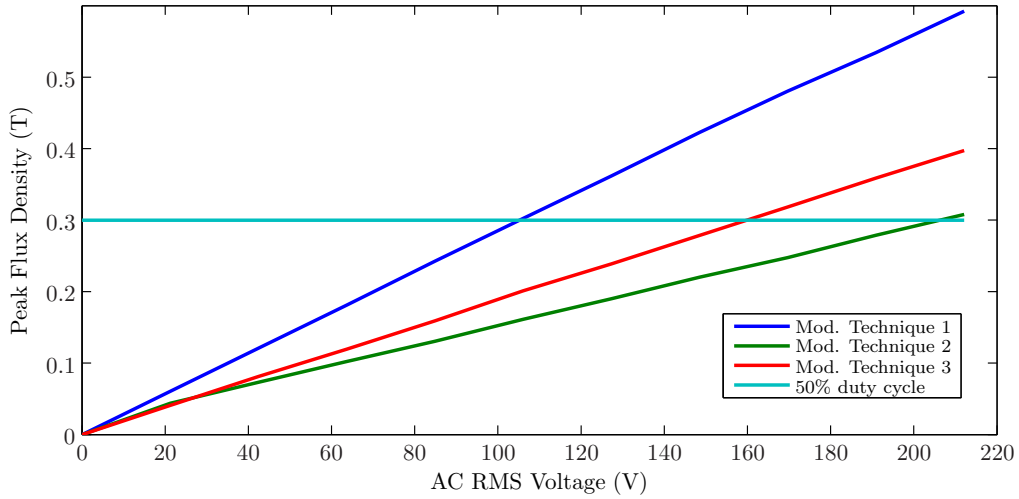


Figure 6.11: Cycloconverter peak flux density against u_{uvw}

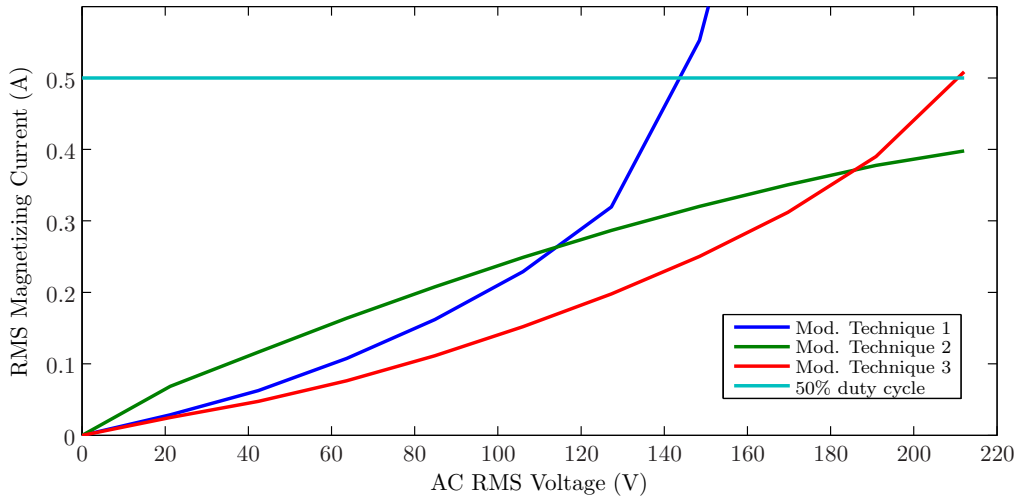


Figure 6.12: Cycloconverter magnetizing current against u_{uvw}

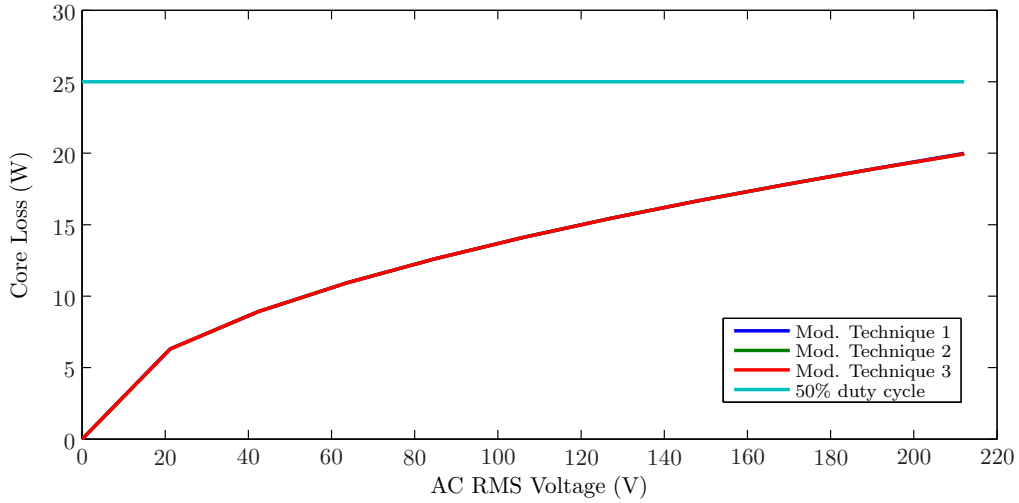


Figure 6.13: Cycloconverter core loss against u_{uvw}. Modulation Techniques 1-3 have identical losses

and AC voltage.

Figure 6.13 shows the results from the transformer core simulation for the core losses for the Cycloconverter Topology. The 50% duty cycle modulation technique has a constant value of core losses 25W, considerably greater than for the three proposed modulation techniques. The three modulation techniques have an almost identical core losses with for a given value of u_{uvw}. This is due to the techniques employed by PSIM to estimate core losses based on the Voltage Time Area (VTA) of u_{pri}. The maximum core losses for the three modulation techniques was 20W when u_{uvw} was 212V RMS.

6.4.3 Hybrid Cycloconverter Topology Transformer Simulation Results

Figures 6.14, 6.15 and 6.16 show the results from the simulation of the transformer core for a range of modulation techniques for the Hybrid Cycloconverter Topology. Figure 6.14 shows the peak flux density in the core of the transformer, Figure 6.15 shows the RMS magnetizing current for the transformer core and Figure 6.16 shows the transformer core power losses, averaged over one cycle.

The results for the peak flux from the modulation strategies for Hybrid Cycloconverter Topology. Figure 6.14 shows an almost identical trend to that of the Cycloconverter Topology, however the additional voltage from the Hybrid Cycloconverter Topology results in an increase of 23% in AC RMS Voltage, u_{uvw}, in relation to peak flux density for all 3 Modulation Techniques. The maximum value of u_{uvw} is also increased by 23% for the 50% duty cycle modulation strategy, whilst the peak flux density remained at 0.3T.

The transformer RMS magnetizing current for the Hybrid Cycloconverter Topology, Figure 6.15, shows a similar trend to that of the Cycloconverter Topology, with the 50% duty cycle modulation having the same value of magnetizing current, of 0.5A RMS, but with a greater maximum AC RMS voltage, u_{uvw}. Saturation starts to have a significant effect on Modulation Techniques 1 and 3 at a higher value of AC RMS voltage with the Hybrid Cycloconverter Topology

compared with that of the Cycloconverter Topology. This occurs at a u_{uvw} of 150V AC RMS instead of 130V AC RMS for Modulation Technique 1 and a u_{uvw} of 240V AC RMS instead of 190V AC RMS for modulation technique 3 . The magnetizing current for all modulation techniques is lower per AC RMS voltage than with the Cycloconverter Topology.

Figure 6.16 shows the results from the transformer core simulation for the core losses for the Hybrid Cycloconverter Topology. The 50% duty cycle modulation technique has a constant value of core losses of 25W, greater than the maximum value for the three proposed modulation techniques. The three modulation techniques have almost identical core losses with for a given value of u_{uvw}. The maximum core losses for the Hybrid Cycloconverter Topology are slightly greater that that of the Cycloconverter Topology, 23W compared with 20W, however the losses per u_{uvw} are lower due to the increased voltage available from this converter.

A simulation investigating the copper losses in the transformer was not carried out due to time restraints and the requirement of an alternative simulation technqiue to provide valid results. The PSIM simulation package, used for the core loss simulation, does not take into account the harmominc content of the waveform. If the same techques used to calculate the transformer core losses were applied to the transformer conductor losses, all of the modulation schemes would show identical results.

An alternative approach, based on a harmonic analysis of the current waveform would have to be used instead. For each current harmonic, the I^2Rlosses would need to be calculated and these would then be summed to give the total losses in the conductor. With this technique the rise time of the current waveform has have a significant impact of the core losses as a faster rise time would result in greater high frequency components and therefore greater losses. In the experimental converter the skin effect of the core would limit these high frequency current harmonics and this would need to be taken account of in simulation.

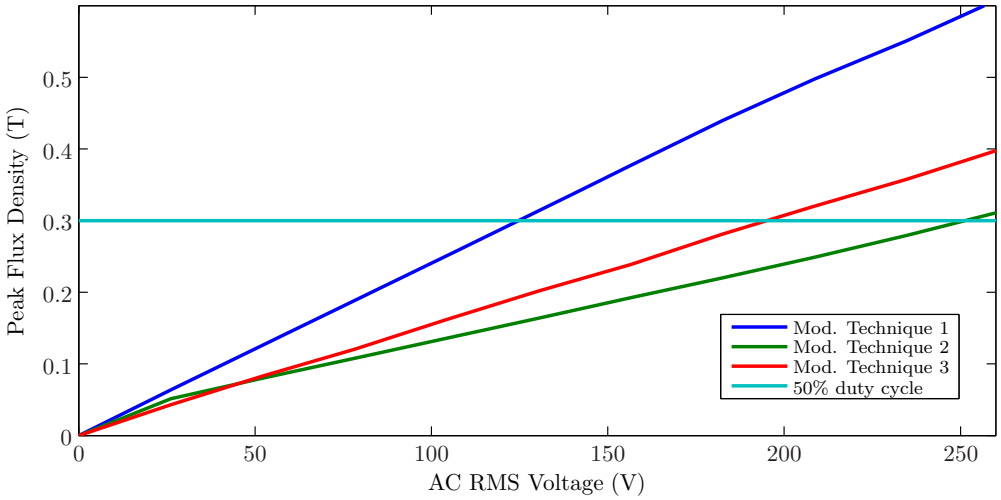


Figure 6.14: Hybrid Cycloconverter peak flux density against u_{uvw}

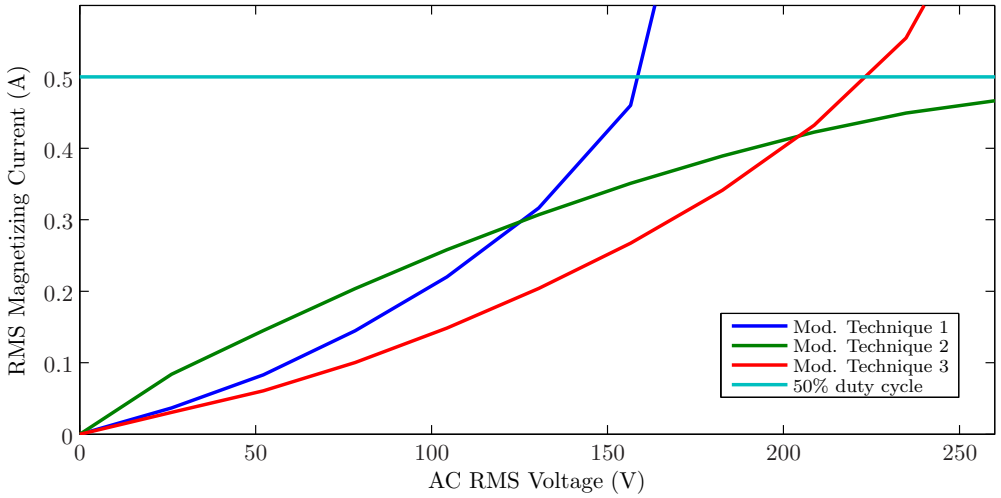


Figure 6.15: Hybrid Cycloconverter magnetizing current against u_{uvw}

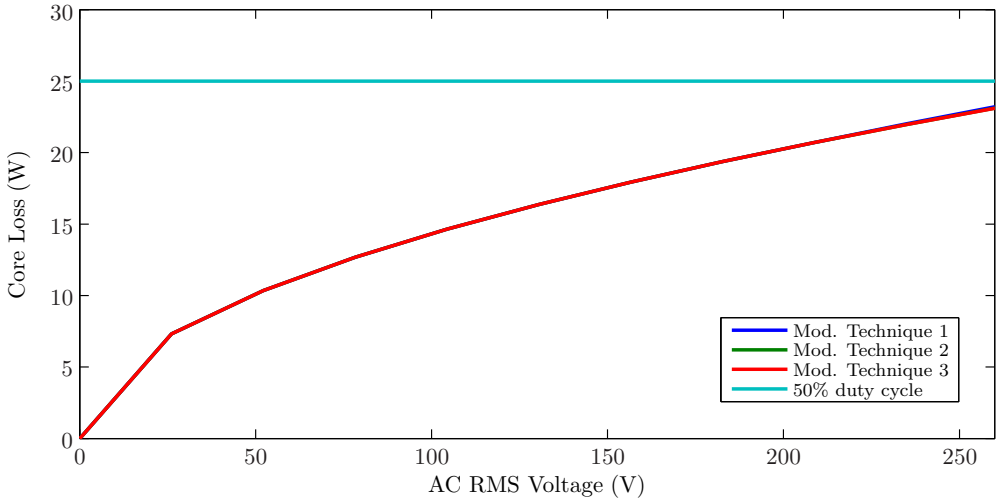


Figure 6.16: Hybrid Cycloconverter core loss against u_{uvw}. Modulation Techniques 1-3 have identical losses

6.5 Summary

This chapter has documented the design and simulation of the High Frequency (HF) transformer for the Cycloconverter and Hybrid Cycloconverter Topologies. The design of the transformer covered the selection of the core materials and the copper conductor profile. The arrangement of the windings and the transformer core materials was shown. Once the transformer had been parametrized, the chapter considered the simulation of the transformer, in terms of peak flux density, core power losses and magnetizing current. Three modulation techniques were compared for the Cycloconverter and the Hybrid Cycloconverter. A 50% duty cycle modulation technique was also used an an illustrative benchmark.

A 50% duty cycle modulation technique resulted in the highest core losses and magnetizing current, however the peak flux was considerably reduced compared with both the Cycloconverter and Hybrid Cycloconverter Topologies. This modulation technique was not selected however due to the difficulty of achieving zero voltage switching in the Cycloconverter.

The approach of splitting each PWM waveform into 3 pulses, Modulation Technique 3, was found to result in a lower peak flux and magnetizing current than Modulation Technique 1 and the symmetry and lack of DC component in the flux density waveform was seen as a key advantage preventing core saturation in the experimental converter compared with Modulation Technique 2. In the simulation, Modulation Technique 3 showed signs of saturation when modulating high values of u_{uvw}. However for the experimental converter the switching frequency will be increased to 5kHz from 3.75kHz. This will result in an increase of u_{uvw} by $^1/_3$ before saturation occurs.

The Hybrid Cycloconverter Topology was able to modulate a 23% higher AC RMS voltage, u_{uvw}, whilst maintaining the same maximum peak flux for all 3 modulation techniques, and the 50% duty cycle modulation technique, which justifies the Hybrid Cycloconverter Topology in terms of increasing the installed power in the High Frequency (HF) Transformer, one of the key aims of this project.

Chapter 7

Converter Controller Designs

This chapter will first outline the strategies used to control the 3-Phase AC currents, i_{uvw}. The AC line current controller works independently of any other control strategies that have been implemented in the converter and results in a demand voltage for the total 3-Phase converter, including the auxiliary 3-Phase VSI, three Cycloconverters and three Single Phase VSIs. However the Cycloconverter and Single Phase VSI are controlled from the same voltage demand and for the control purposes, the Single Phase VSI and the Cycloconverter are combined and called the 'Main Converter'. This is shown in Figure 7.1.

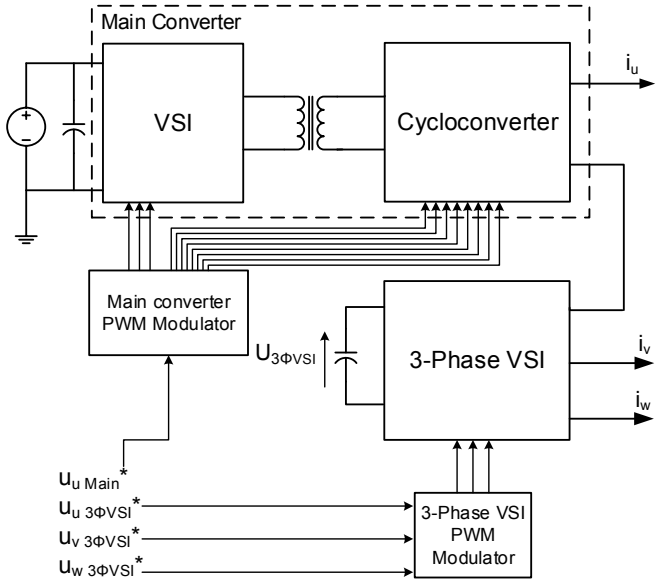


Figure 7.1: Converter topology and control system, showing one phase of the Main Converter

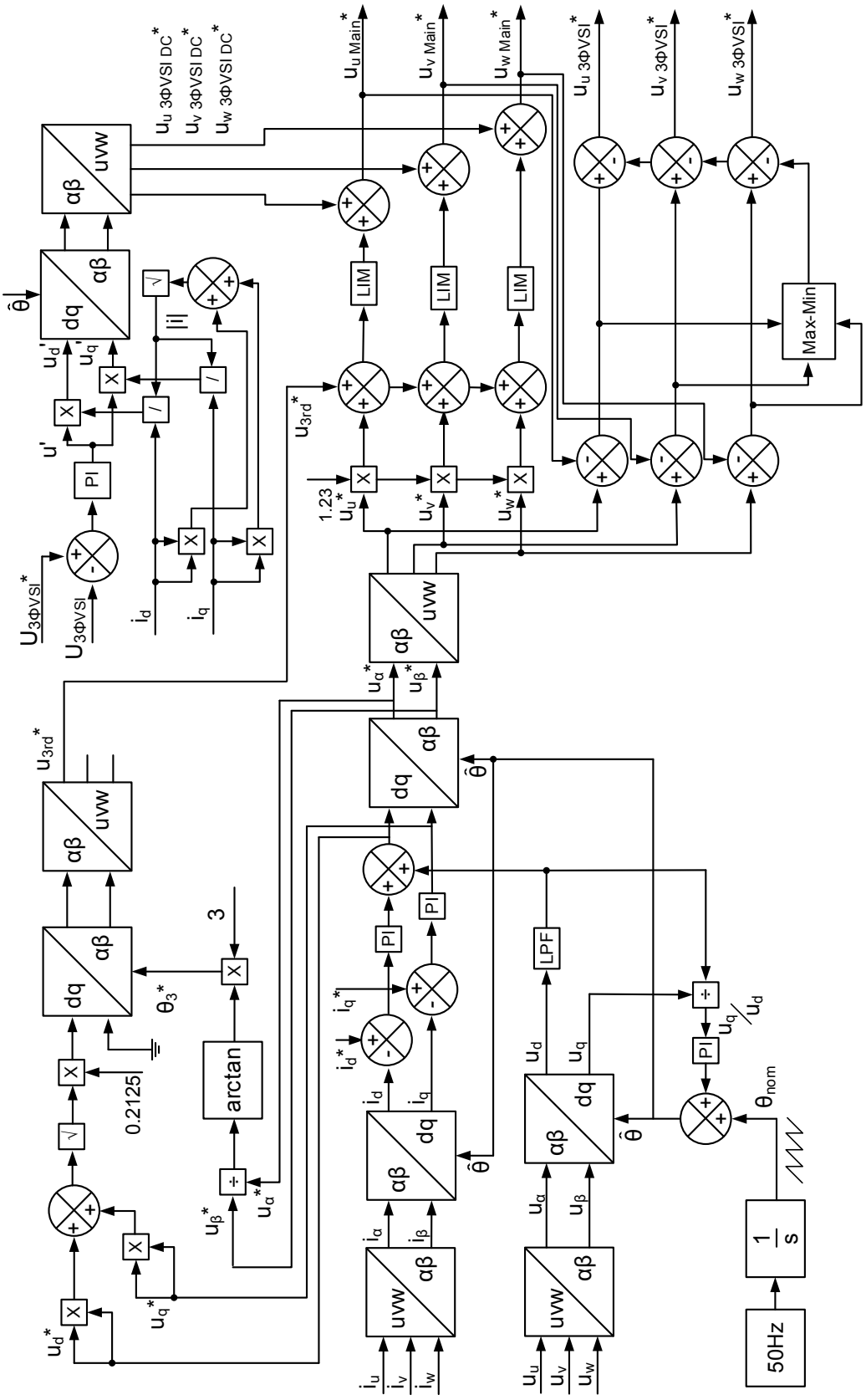


Figure 7.2: Complete control system diagram

This chapter will then go on to discuss the division of the AC voltage demand from the AC line current controller between the three Main Converters and the auxiliary 3-Phase VSI and the control of the DC link capacitor voltage. The auxiliary 3-Phase VSI provides only reactive power and has no DC side power source or sink. Therefore the DC link capacitor voltage is maintained solely by the transfer of energy from or to it by the Main Converter and this control scheme must not affect the voltage produced by the total 3-Phase converter or therefore the AC line currents.

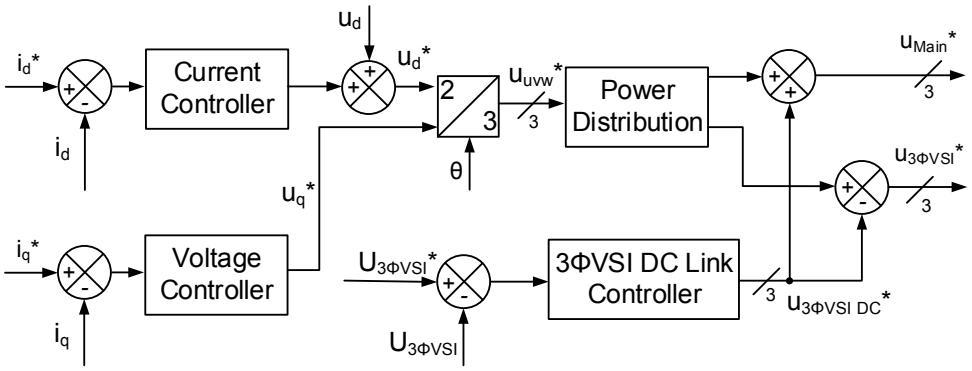


Figure 7.3: Generalized system controller design

Figure 7.1 shows the arrangement of the total converter system, constructed from the three Main Converters and an auxiliary 3-Phase VSI. Only one Main Converter is shown. The experimental converter has three Main Converters, one for each AC phase. In Figure 7.1, i_u, i_v and i_w are the AC currents, $U_{3\Phi VSI}$ is the 3-Phase VSI DC link Voltage, ${u_{main}}^*$ are the 3-Phase demand voltages for the three Main Converters, ${u_{u3\Phi VSI}}^*$, ${u_{v3\Phi VSI}}^*$ and ${u_{w3\Phi VSI}}^*$ are the u v w demand voltages for the auxiliary 3-Phase VSI. Figure 7.4 shows a vector diagram of the 3-phase AC voltages or currents to the the stationary α-β reference frame and the d-q rotating reference frame.

The current controller is based on the transformation of the 3-Phase currents into the d-q rotating reference frame orientated on the grid voltage u_u using the RMS convention. This results in equivalent DC currents corresponding to real and reactive power. This allows for a Proportional Integral (PI) controller based control system as the controller is required to have an infinite gain at DC.

Figure 7.3 shows a generalized system controller design and Figure 7.2 shows the complete control system design. i_d and i_q are the measured real and reactive

currents, i_d* and i_q* are the reference real and reactive grid currents. The outputs of the current controllers are u_d* and u_q*. These are transformed into the 3-Phase demand voltages ${u_{uvw}}^*$ for the Main Converter and auxiliary 3-Phase VSI.

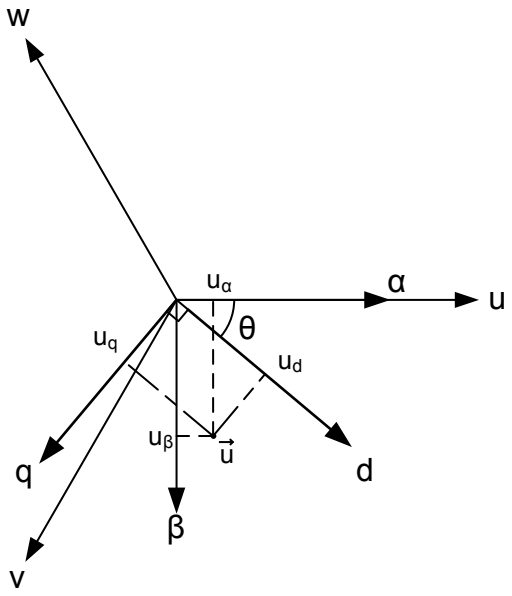


Figure 7.4: Vector diagram of uvw - α-β - d-q transformations

The control of the DC link of the auxiliary 3-Phase VSI measures the auxiliary 3-Phase VSI DC link voltage, $U_{3\Phi VSI}$ and subtracts it from the reference DC link voltage, ${U_{3\Phi VSI}}^*$. This error voltage is fed into a voltage controller and results in the production of a demand voltage, ${u_{3\Phi VSIDC}}^*$, in phase with the demanded converter voltage, ${u_{uvw}}^*$. ${u_{3\Phi VSIDC}}^*$ is subtracted from the demand voltage from the auxiliary 3-Phase VSI and added to the demand voltage from the Main Converter, ${u_{main}}^*$. The effect on the demand voltage from the total converter is therefore zero.

The auxiliary 3-Phase VSI DC link voltage controller will result in an increase in the demand voltage from the Cycloconverter and care needs to be taken to prevent this from causing saturation of the transformer. Under normal operation ${u_{3\Phi VSIDC}}^*$ should be of a low value as the converter balancing control is designed to result in no net power transfer and therefore the DC link controller is only required to compensate for losses in the converter or current harmonics that cause a power unbalance.

7.1 Grid Synchronization

To convert the 3-Phase currents into the d-q rotating reference frame the angle of the grid voltage, $\hat{\theta}$, needs to be obtained. The 3-Phase voltages are measured and transformed to the stationary α-β reference frame using:

$$u_\alpha = \frac{\sqrt{2}}{3}u_u - \frac{\sqrt{2}}{6}u_v - \frac{\sqrt{2}}{6}u_w \tag{7.1}$$

$$u_\beta = \frac{1}{\sqrt{6}}u_v - \frac{1}{\sqrt{6}}u_w \tag{7.2}$$

The angle of the grid was obtained using a Phase Lock Loop (PLL) based on a PI controller. An alternative approach uses an arctan function, however a PLL was selected due to the reduction in processing power in the DSP and a greater rejection of any distortion on the AC line voltages when compared with the arctan approach [71].

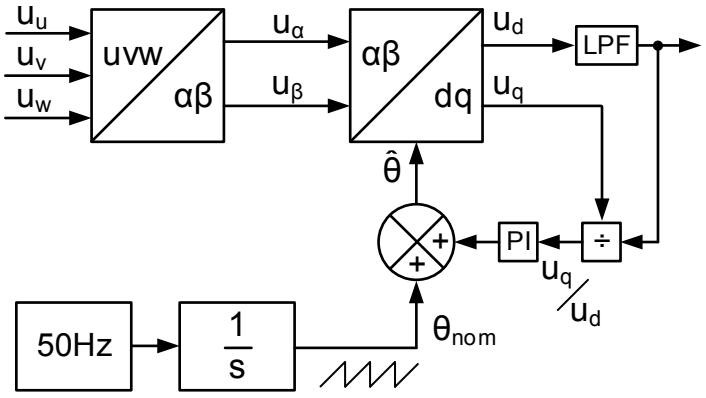
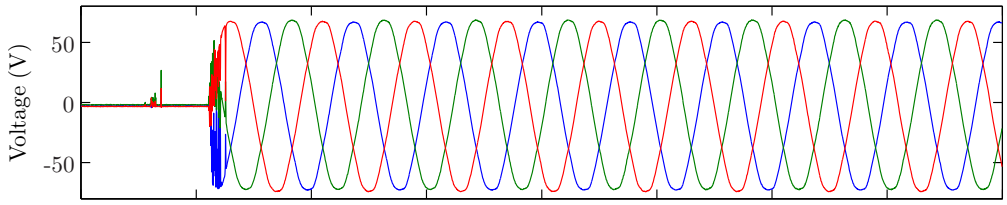


Figure 7.5: PLL grid synchronization control

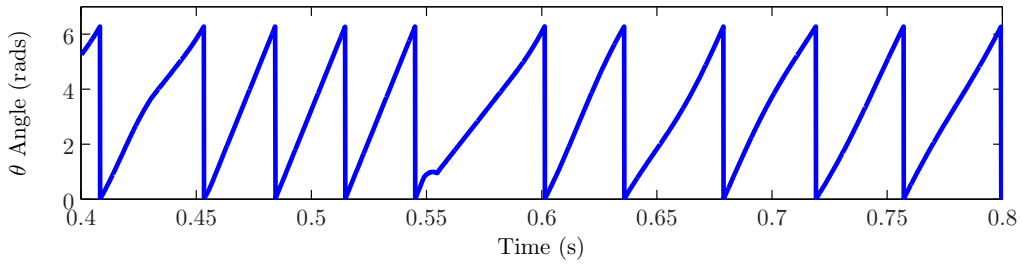
The PLL functions by controlling u_q to zero resulting in the grid voltage estimation angle $\hat{\theta}$. $\hat{\theta}$ is obtained by adding a nominal angle θ_{nom} (obtained by a counter counting from 1 - 2π every 20ms) to the output of the PI u_q controller. To prevent the PLL from potentially synchronizing 90° out of phase the PI controller actually acts on u_q/u_d. u_d and u_q are obtained from u_α and u_β by:

$$u_d = u_\alpha \cos\theta + u_\beta \sin\theta \tag{7.3}$$

$$u_q = -u_\alpha \sin\theta + u_\beta \cos\theta \tag{7.4}$$



(a) 3 Phase Voltages u_u (red), u_v (blue), u_w (green)



(b) Grid angle $\hat{\theta}$

Figure 7.6: Waveforms from PLL Based Grid Synchronization

Figure 7.6 shows the experimental AC voltage waveforms, 7.6(a) and the converter grid angle $\hat{\theta}$, 7.6(b). At 0.46s the converter is connected to the AC grid and the PI controller is enabled. In this case it takes approximately a further 0.3s before the PLL is locked to the grid angle. This is a worst case example as the grid was switched on when the nominal grid angle, θ_{nom} was 90° out of phase with the actual grid voltage angle, θ. A lock would be obtained more quickly if this was not the case.

7.2 Current Controller

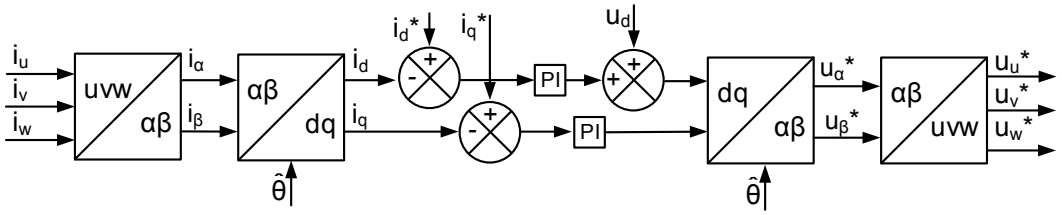


Figure 7.7: Current control loop schematic

Figure 7.7 shows a schematic of the current controller. Using the grid voltage angle, $\hat{\theta}$, obtained using the PLL grid synchronization controller, the AC grid currents, i_u i_v i_w, are transformed into i_d and i_q by equations:

$$i_\alpha = \frac{\sqrt{2}}{3} i_u - \frac{\sqrt{2}}{6} i_v - \frac{\sqrt{2}}{6} i_w \tag{7.5}$$

$$i_\beta = \frac{1}{\sqrt{6}} i_v - \frac{1}{\sqrt{6}} i_w \tag{7.6}$$

$$i_d = i_\alpha \cos\theta + i_\beta \sin\theta \tag{7.7}$$

$$i_q = -i_\alpha \sin\theta + i_\beta \cos\theta \tag{7.8}$$

The currents i_d and i_q represent the real and reactive components of the AC currents. The reference currents, $i_d{}^*$ and $i_q{}^*$ are set by the user. $i_d{}^*$ is obtained for the amount of real power the converter is to handle. $i_q{}^*$ is obtained from the amount of reactive power that is to be injected into the grid. They are subtracted from the measured values, i_d and i_q, to give an error for the d and q axes. Two PI controllers are used to control the i_d and i_q errors to zero.

The current controller design was based on the assumption that the converter

acted as an ideal voltage source and the plant was the AC inductor. Figure 7.8 shows the simplified AC plant model used for the controller design.

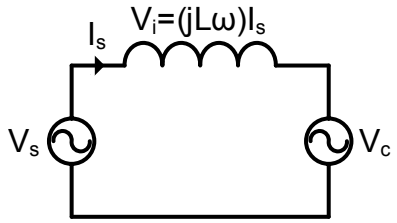


Figure 7.8: AC Model

Figure 7.9 shows a phasor diagram of the converter. The phase shift between converter voltage, V_C and AC grid voltage, V_s controls the voltage drop across the AC inductor, V_i and therefore the converter current, I_s.

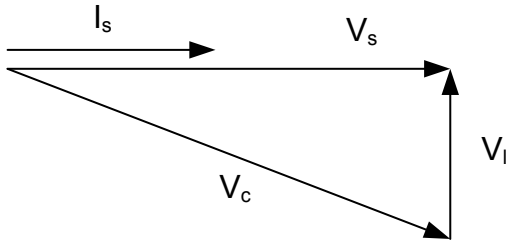


Figure 7.9: Phasor diagram showing converter operating at unity power factor

Figure 7.10 shows the control loop used in the design of the current controller. The R and L values of $Gp(s)$ are taken from the converter line inductance with has a 0.08Ω resistive element and and inductance of 3.05mF.

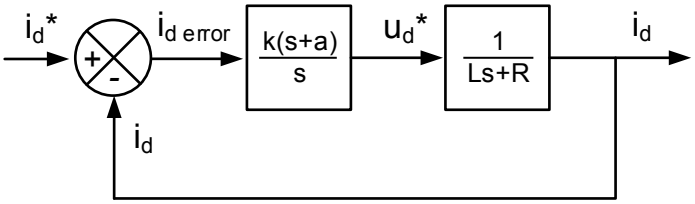


Figure 7.10: Closed-loop current controller

As the plant, $Gp(s)$, is first order in nature, $Gc(s)$ is a PI controller. Using pole placement, the controller was designed to a achieve a bandwidth of 530Hz with ideal damping and a phase margin of 77°. The controller design is:

$$Gc(s) = 11.873\left(\frac{s+986}{s}\right) \tag{7.9}$$

The output from the d axis controllers is summed with the grid voltage, u_d, so that the AC demand voltages, ${u_{uvw}}^*$ are equal to the AC grid voltage, u_{uvw}, when the converter is first switched on. The AC demand voltages are converted to the three converter demand phase voltages, ${u_u}^*$ ${u_v}^*$ ${u_w}^*$ using equations:

$$u_\alpha = u_d \cos\theta - u_q \sin\theta \tag{7.10}$$

$$u_\beta = u_d \sin\theta + u_q \cos\theta \tag{7.11}$$

$$u_u = \sqrt{2}u_\alpha \tag{7.12}$$

$$u_v = -\frac{1}{\sqrt{2}}u_\alpha + \sqrt{\frac{3}{2}}u_\beta \tag{7.13}$$

$$u_w = -\frac{1}{\sqrt{2}}u_\alpha - \sqrt{\frac{3}{2}}u_\beta \tag{7.14}$$

These demand phase voltages are the demand voltages for the whole converter, including the Main Converter and auxiliary 3-Phase VSI. The division of power between the Main Converter and the auxiliary 3-Phase VSI is outlined in the following section. This will also cover the control of the DC link voltage of the auxiliary 3-Phase VSI and the peak power reduction of the Cycloconverter.

7.3 3-Phase VSI DC Link Control

To charge up the auxiliary 3-Phase VSI DC link capacitor during start-up and maintain the correct DC link voltage during steady state operation, a control scheme was implemented results in a 3-Phase sinusoidal voltage, $u_{3\Phi VSIDC}{}^*$, that is synchronized to the phase with the AC line current, i_{uvw}. $u_{3\Phi VSIDC}{}^*$ is added to the demand voltage of the Main Converter, $u_{main}{}^*$ and is subtracted from the demand voltage of the auxiliary 3-Phase VSI, $u_{3\Phi VSI}{}^*$. The demand voltage for the total converter therefore remains unchanged from the demand voltage from the current controller, $u_{uvw}{}^*$.

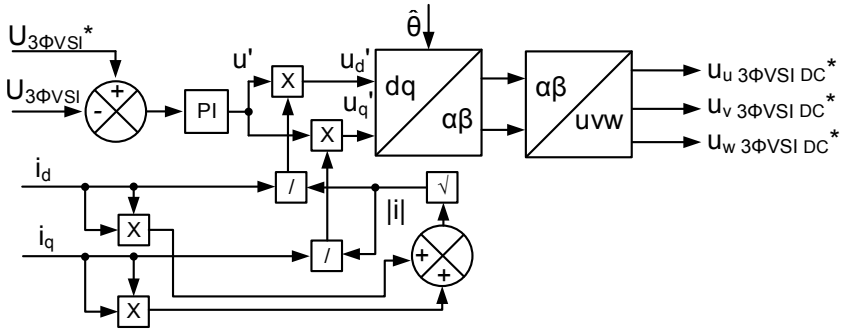


Figure 7.11: 3-Phase VSI DC link control schematic

Figure 7.11 shows a schematic of the auxiliary 3-Phase VSI DC link controller. The voltage of the DC link, $U_{3\Phi VSI}$ is measured and subtracted from the DC link reference voltage, $U_{3\Phi VSI}{}^*$ to give an error voltage. This error voltage is fed into a PI controller, giving the amplitude of the required demand voltage required to bring the error to zero.

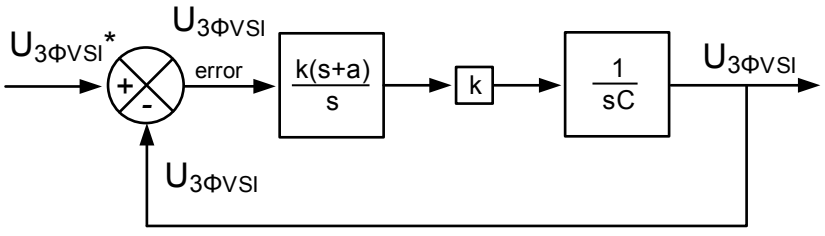


Figure 7.12: Closed-loop auxiliary 3-Phase VSI DC link controller

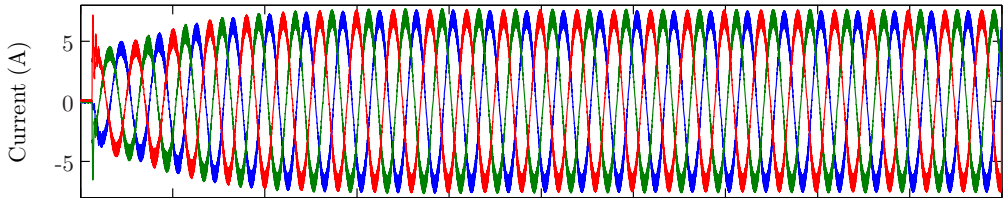
The output of the PI controller is a voltage, which when multiplied by the AC current magnitude and divided by the 3-Phase VSI DC link voltage, produce a

current into the 3.6mF 3-Phase VSI DC link capacitor. The AC current magnitude and 3-Phase VSI are replaced by a single constant, k, to simplify the design of the controller.

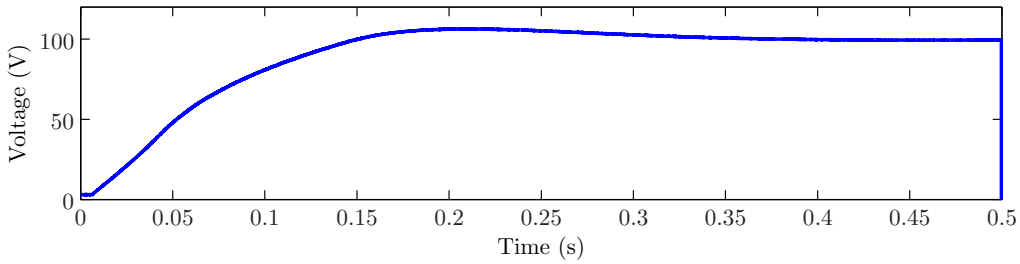
As the plant is first order in nature, Gcs, is a PI controller. Using Venable's approach, the controller was designed to a achieve a bandwidth of 10Hz with critical damping. The controller design is:

$$Gc(s) = \frac{71.4}{s}(1 + \frac{s}{36.28}) \tag{7.15}$$

To synchronize this voltage with the AC grid current, this demand voltage, u' is multiplied by $i_d/|i|$ and $i_q/|i|$ to give demand voltages $u_d{}'$ and $u_q{}'$. These demand voltages are converted to the α-β frame and to the 3-Phase AC voltages ${u_{u3\Phi VSI}}^*$ ${u_{v3\Phi VSI}}^*$ ${u_{w3\Phi VSI}}^*$. These voltage demands are added to the demand voltage for the Main Converter and subtracted from the demand voltage for the auxiliary 3-Phase VSI, as shown in Figure 7.3.



(a) AC line currents, i_{uvw}



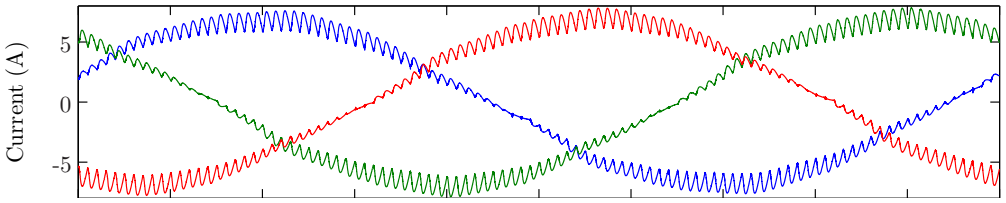
(b) 3-Phase VSI DC link voltage, $U_{3\Phi VSI}$

Figure 7.13: Hybrid Cycloconverter AC line currents and auxiliary 3-Phase VSI DC link voltage, charging with an RL load, ${U_{3\Phi VSI}}^* = 100$V

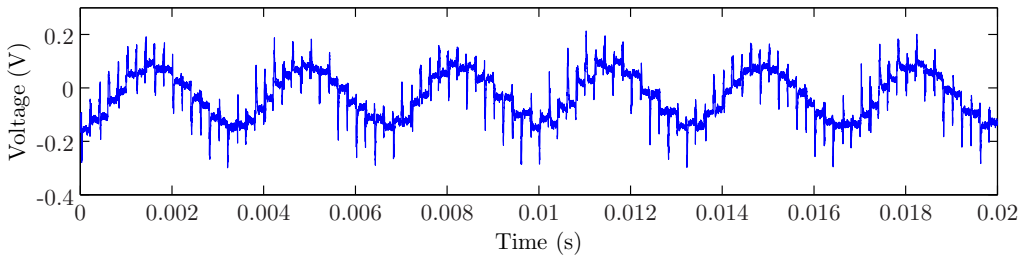
Experimental results from the DC link control circuit are shown in Figure 7.13 and 7.14. The AC line currents, i_{uvw} and the auxiliary 3-Phase VSI DC link voltage, $U_{3\Phi VSI}$ are shown, with Figure 7.13 showing the charging of the auxiliary 3-Phase

VSI DC link capacitor and Figure 7.14 showing the performance of the auxiliary 3-Phase VSI DC link controller under steady state operation.

The charging of the DC link capacitor attached to $U_{3\Phi VSI}$ occurs once the AC line currents i_{uvw} increase above 1A RMS. Figure 7.13 shows that the reference voltage, $U_{3\Phi VSI}{}^{*}$, of 100V is reached within 150ms followed by a slight overshoot to 110V. This overshoot will not have any negative impact on the operation of the converter and is well within the voltage limits of the DC link capacitor and switching devices, even if 150V MOSFETs were used.



(a) Converter current, u_{uvw}



(b) 3-Phase VSI DC link voltage, $U_{3\phi VSIDC}$, AC coupling

Figure 7.14: Hybrid Cycloconverter AC line currents and auxiliary 3-Phase VSI DC link voltage, under steady state operation with an RL load, $U_{3\Phi VSI}{}^{*}= 100V$

Figure 7.14 shows the AC line currents, i_{uvw} and the steady state voltage ripple on $U_{3\Phi VSI}$. Figure 7.14(b) is AC coupled and has a DC offset of 100V. The ripple on $U_{3\Phi VSI}$ is under 0.4V peak-peak and this falls well within the performance requirements of the auxiliary 3-Phase VSI DC link controller.

7.4 Cycloconverter and 3-Phase VSI Power Distribution

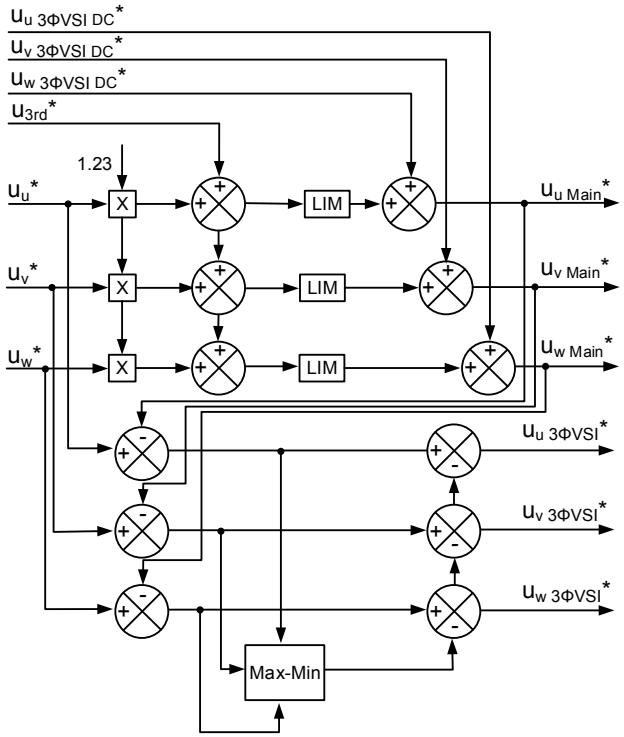


Figure 7.15: Distribution of demand voltage between Main Converter and 3-Phase VSI

Figure 7.15 shows the distribution of the demand voltage from the current controller between the Main Converter and the auxiliary 3-Phase VSI, with the addition of the demand voltage from the auxiliary 3-Phase VSI DC link controller. This distribution scheme is based on the Voltage Distribution Scheme 3: Sine, 3rd and Clipped Waveform Shape as described in Chapter 3, Section 3.3 and that section explains the reasons for this wave shaping technique. The demand voltages for the Main Converter, $u_{umain}{}^*$, $u_{vmain}{}^*$ and $u_{umain}{}^*$ are calculated in the following manner. The current controller demand voltages, $u_u{}^*$, $u_v{}^*$ and $u_w{}^*$, are multiplied by a constant, 1.7 and then combined with the injected 3rd harmonic that is described later in this chapter. A limit is imposed on the demand voltages before being combined with the demand voltages from the auxiliary 3-Phase VSI DC link controller, $u_{u3\Phi VSI}{}^*$, $u_{v3\Phi VSI}{}^*$ and $u_{w3\Phi VSI}{}^*$.

The demand voltages for the auxiliary 3-Phase VSI are calculated by subtracting

the demand voltages for the Main Converter, $u_{umain}{}^*$, $u_{vmain}{}^*$ and $u_{umain}{}^*$, from the demand voltages from the current controller, $u_u{}^*$, $u_v{}^*$ and $u_w{}^*$. Finally the triplen harmonics, $u_{triplen}{}^*$ are subtracted giving the demand voltages for the auxiliary 3-Phase VSI, $u_{u3\Phi VSI}{}^*$, $u_{v3\Phi VSI}{}^*$ and $u_{w3\Phi VSI}{}^*$.

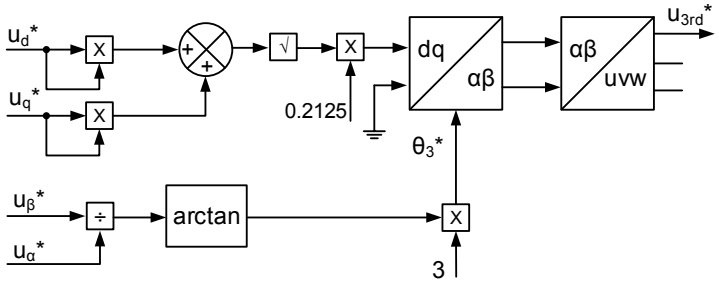
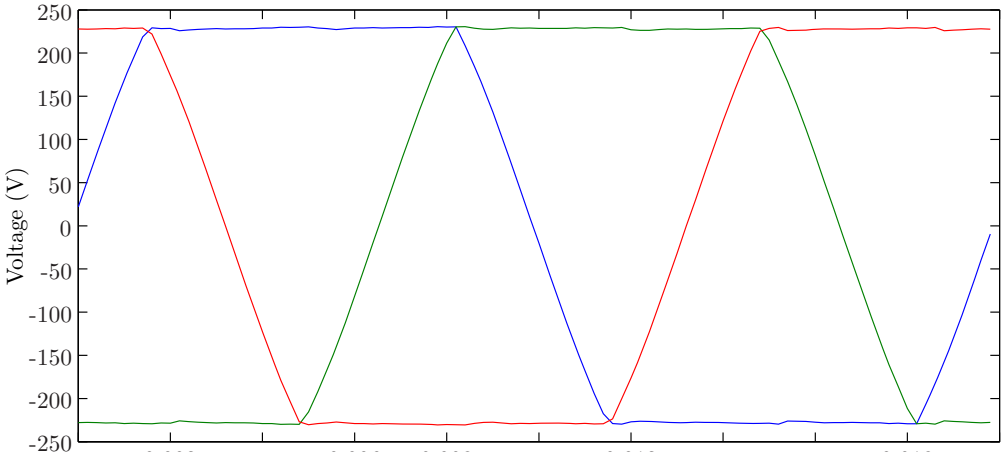
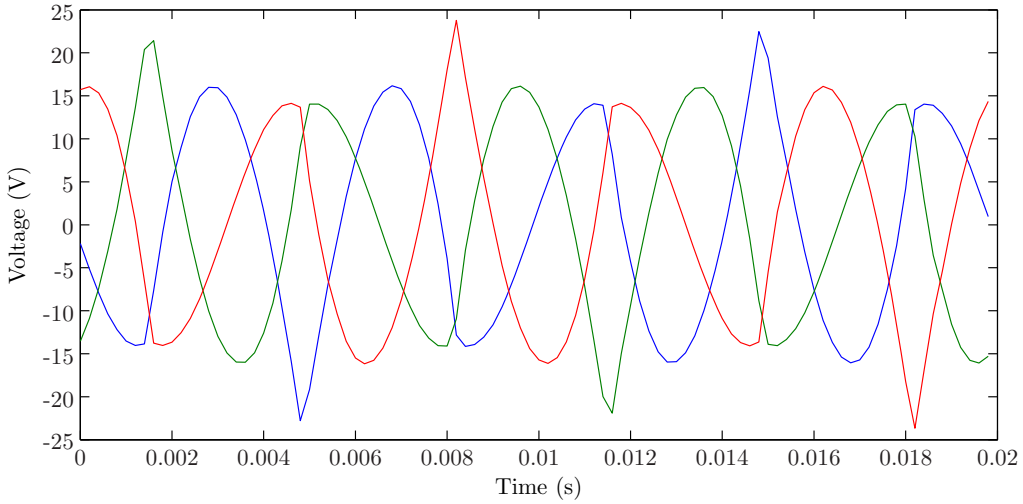


Figure 7.16: 3rd harmonic injection synchronized to the demand voltage



(a) Main Converter demand voltages, $u_{umain}{}^*$ (blue), $u_{vmain}{}^*$ (green) and $u_{umain}{}^*$ (red)



(b) 3-Phase VSI demand voltages $u_{u3\Phi VSI}{}^*$ (blue), $u_{v3\Phi VSI}{}^*$ (green) and $u_{w3\Phi VSI}{}^*$ (red)

Figure 7.17: 3-Phase VSI and Main converter reference waveforms captured from DSP

The generation of the 3rd harmonic, u_{3rd} is shown in Figure 7.16 and is achieved by multiplying the magnitude of the current controller demand voltage, u_{uvw} by 0.2125 and converting it to a Sine wave at 150Hz, in phase with u_{uvw}. This is achieved using an angle, θ_3^*, calculated using an *arctan* function. An *arctan* function is used, instead of a PLL, due to the time delay a PLL takes to respond to a step change in demand voltage.

Figure 7.17 shows experimental waveforms captured in the DSP that show the division of the demand voltage from the Hybrid Cycloconverter ($u_{uvw}{}^*$) between the Main Converter ($u_{main}{}^*$) and the auxiliary 3-Phase VSI ($u_{3\Phi VSI}{}^*$). The experimental waveforms match the theoretical waveforms, both in shape and amplitude, calculated in Chapter 3, confirming the validity of the simulations.

7.5 Cycloconverter Feed-Forward Control

The build up of current in the transformer to allow comutation to be performed in the Cycloconverter stage by the diodes for Mode 2 and 3 operation, the dead time in the VSI and the the delay due to commutation of the diodes in the Cycloconverter all subtract from the VTA of each PWM pulse. To compensate for this, an additional feed-forward component is added to the 3-Phase demand voltages for the Main Converter. This feed-forward component is calculated at each interrupt for the subsequent PWM pulse, based on the mode of operation and the AC current magnitude. The feed-forward component is calculated as a time delay, allowing for it to be added to the Modulation Index (MI) of the demand voltages, multiplied by the Interrupt Service Routine (ISR) frequency.

A high performance resonant controller would be able to entirely compensate for this distortion in the AC voltages, whereas a PI controller will only be able to minimize it. However a feed-forward approach was selected due to the simplicity and increased stability it offers. The feed-forward component is derived from first principles and is based on the estimated commutation time. This estimated time combines the AC current build up delay, the dead time and the switching time of the converter. It was discovered however that this feed-forward component was not able to compensate for this distortion entirely and a PI controller was

required to ensure that the AC current was free of harmonic components. However the addition of an approximate feed-forward component significantly reduces the performance requirements from the PI controller.

The first PWM pulse does not have a dead time delay because it is the enable line that is switched and not the PWM signal. The second and third pulses do have a dead time, during which all of the IGBTs are switched off. The turning on of the VSI is performed under zero current conditions. The switching off of the VSI results in the transformer current commutating from the IGBTs to the anti-parallel diodes of the opposite IGBTs, resulting in the current falling to zero as the energy stored in the leakage inductance is returned to the supply. This is a hard switched transition. The IGBTs are then switched on, after the dead time delay of 0.75µs. Provided the current has not fallen to zero by the point at which the IGBTs have switched on, the dead time of the VSI has no effect on the distortion of the AC voltage and it is purely due to the delay from the building up of current in the leakage inductance. If however the current falls to zero before the IGBTs have switched on, then the current will not start building up for the next pulse until it has.

The time delay for the building up the current in the leakage inductance of the transformer, T_{build}, is calculated from the time required to build up a current in the transformer with the AC side of the transformer shorted by the Cycloconverter and the DC side connected to U_{DC} via the Single Phase VSI. T_{build} is given by:

$$T_{build} = \frac{L_{leakage} i_{AC}}{V_{DC}} \tag{7.16}$$

The dead time of the Single Phase VSI is set in hardware and has a constant value of $T_{deadtime} = 0.7\mu s$.

The commutation of the Cycloconverter is performed by the anti-parallel diodes. This delay time is estimated from the reverse recovery value in the IGBT datasheet. However the datasheet only contains information on the delay time above 100A/µs while the converter ${}^{di}/_{dt}$ is limited to around 10A/µs by the leakage inductance in the transformer the delay time for the diode reverse recovery is given by $T_{rr} = 0.25\mu s$.

The feed-forward component when the converter is operating in Mode 1 is:

$$T_{Mode1} = 3.5\mu s \tag{7.17}$$

The calculation is based on three switching pulses, resulting in current build-up delays and the Cycloconverter commutation occurring three times per ISR. The dead time value only needs to be compensated for twice, due to an absence of a dead time delay on the first pulse. The commutation is performed using the clamp circuit to limit the voltage across the AC side of the converter to around 800V. The resulting voltage across the leakage inductance in the transformer is therefore either 1200V or 400V depending on the actual current polarity with respect to the demand voltage. During this time the AC voltage is negative with respect to the correct AC voltage so to compensate for this delay the feed-forward component needs to be twice as large. The best case is selected for the feed-forward term (1200V) with a reliance on the current controller to make up for any discrepancy. As the current is of a low value in Mode 1 this potential error should not be significant. There is no build up delay due to the small value of AC current and its transient nature.

The feed-forward component when the converter is operating in Mode 2 is:

$$T_{Mode2} = 4.2T_{build} + 0.8\mu s \tag{7.18}$$

$$T_{Mode2} = 2.6T_{build} + 2.2\mu s \tag{7.19}$$

The calculation is based on three switching pulses, resulting in current build up delays and Cycloconverter commutation occurring 3 times per ISR. The dead time value only needs to be compensated for twice, due to an absence of a dead time delay on the first pulse. No dead time due to the fact that diodes in VSI perform commutation.

The feed-forward component when the converter is operating in Mode 3 is:

$$T_{Mode3} = 3T_{build} + 3T_{deadtime} + 3T_{rr} + 6\mu s \tag{7.20}$$

The Mode 3 commutation time is similar to that of Mode 2, however the feed-forward time delay has to account for the additional 1µ s per pulse time delay for the reverse pulse. The is at a voltage of $-u_{DC}$ once the converter has commutated and 0V during commutation. From experimentally measuring the commutation time it was discovered that the commutation time was $0.7T_{build}$ per pulse.

7.6 Summary

This chapter has documented the control strategies implemented in this converter. These include the grid synchronization controller, the current controller and the DC link controller. The implementation of the distribution of power between the auxiliary 3-Phase VSI and Main converter is also documented, based on the voltage distribution scheme that shifted and clipped the waveform shape.

To compensate for distortion caused by the commutation of the Cycloconverter and dead time in the VSI, the addition of a feed forward term to the demand voltage of the Main Converter was described. It was found that even with this feed-forward term the current controller is still required to eliminate the distortion in the AC voltage when the Main Converter changes its mode of operation. Future research could focus on using a more advanced control strategy, for example a repetitive controller, to completely eliminate any distortion in the AC voltage and the need to have feed-forward terms.

Chapter 8

Experimental Results

This chapter descries the experimental evaluation of the Cycloconverter and Hybrid Cycloconverter Topologies to compare converter losses and 3-Phase AC waveform quality. The tests that were carried out are described to establish the performance of the converters under a range of operating conditions and to justify the additional auxiliary 3-Phase VSI in The Hybrid Cycloconverter Topology, in terms of power output and converter losses.

The tests investigated the transfer of power from the DC network to a resistive load bank, the transfer of power from the AC network to the DC network, the transfer of power from the DC network to the AC network and a test from 0° to 360° phase shift between voltage and current at i_{uvw} 10A RMS. The equipment used to perform measurements and acquire waveforms is described. Specifications and accuracy are given.

A comparison between the simulation carried out in Chapter 4 and the experimental converter will be made, highlighting differences between the two tests and common features and trends between the simulation and experimental results.

The chapter then concludes with a a comparative assessment of the performance of the Cycloconverter and Hybrid Cycloconverter Topologies, discussing any complications arising during the testing, and presenting a range of potential solutions for further research.

8.1 Experimental Set Up

8.1.1 Experimental Strategy

The Regatron TopCon GSS 60kW variable bi-directional DC power supply was used as the DC network and connected to U_{DC} on the Cycloconverter and Hybrid Cycloconverter Topologies. This allows the converters to be tested with bi-directional power transfer between the DC and AC network with the DC link, U_{DC}, set at 350V. 350V was selected as it was the maximum voltage the converter could operate at whilst keeping the clamp voltage under 800V. To test the performance of the Cycloconverter and Hybrid Cycloconverter Topologies the losses in the converters were measured and the AC current waveforms were captured to analyse the harmonic distortion.

The first test that was carried out tested the power transfer from the DC network to a 3-phase resistive load bank. This test was carried out to ensure the voltage distribution scheme and current controller was working correctly before connection to an AC grid. For this test the voltage waveforms from the converters were recorded to verify the correct operation of the voltage distribution of the AC demand voltage, ${u_{uvw}}^*$ between the Main Converter, ${u_{main}}^*$, and the auxiliary 3-Phase VSI, ${u_{3\Phi VSI}}^*$, as described in Chapter 7.

The second test that was carried out tested the power transfer from the AC network to the DC network, the third test tested the power transfer from the DC network to the AC network and the fourth test changed the phase shift between voltage and current from 0º to 360º in 11.25º increments. For these tests a 60kVA bi-directional AC supply, the Regatron TS.ACS AC power supply was used. A bi-directional 3-Phase programmable supply was used, as opposed to a connection to the AC grid, since it acts as an ideal voltage source providing a stable frequency and voltage with no voltage harmonics. This resulted in reduced harmonic currents and increased consistency between measurements.

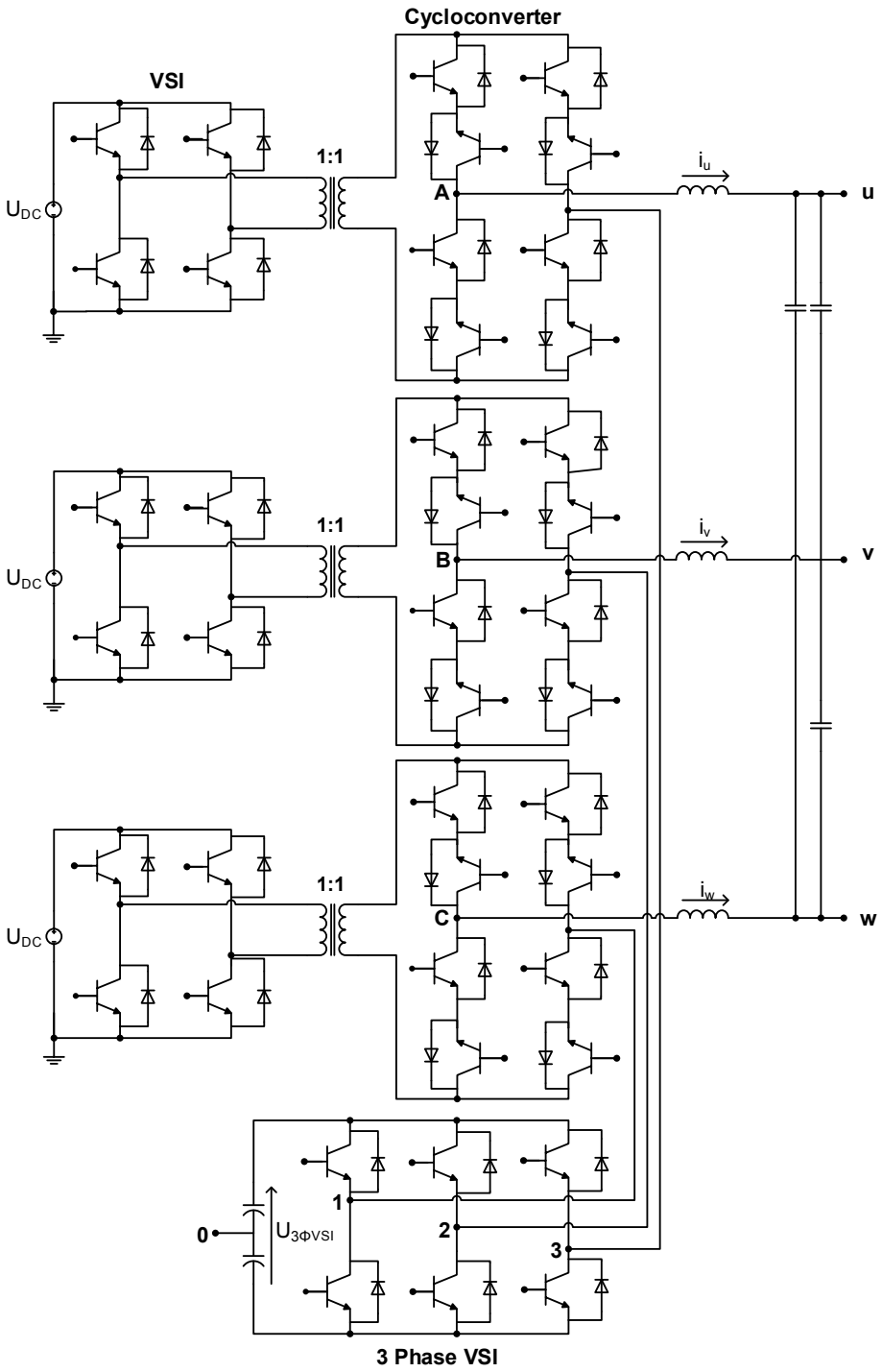


Figure 8.1: Schematic of the two tested converters with the terminals labelled 1, 2 and 3 on the auxiliary 3-Phase VSI connected together for The Cycloconverter Topology

8.1.2 Experimental Measurement Techniques

To measure the losses in the converters, two Newtons4th KinetiQ PPA5530 power analysers were used. The power analysers have an accuracy of 0.02% ± 100mV when measuring voltage, 0.02% ± 10mA accuracy when measuring current and have an accuracy of 0.06% ± 3W when calculating power. They have a frequency range of DC to 2MHz. For measuring the power from the DC network, one PPA5530 was connected between the TopCon GSS DC power supply and 3.2mF DC link capacitor of the 3 single phase VSIs. For measuring the power from the AC network one PPA5530 was connected between the the u, v, w terminals on the converter and the Chroma Power supply or 3-Phase resistor bank, depending on the test being carried out.

In order to calculate the efficiency of a power converter the accuracy of the measurement equipment becomes paramount. This is due to the resulting error in power measurement being dependant on power processed, rather than the losses in the system. As such with a highly efficient and high powered converter, measuring the efficiency using this technique may results in a wider margin of error than the total energy lost in the converter, invalidating the results. In this case an alternative approach using a calorimeter would have to be used. With 90% converter efficiency, the accuracy when calculating losses using the power analyser is therefore 1.2% ± 6W which is an acceptable level of error.

The current and voltage waveforms from the converters were measured using LEM PR30 current probes and Testek TT-SI 51 active differential voltage probes. The LEM PR30 has a range of 30A, a bandwidth of 100kHz and an accuracy of 1% ± 2mA. The Testek TT-SI 51 has a range of ± 700V, a bandwidth of 50MHz and an accuracy of 1% ± 1mV. The HF Transformer current waveforms, i_{pri}, were captured using a PEM CWA Rogowski Current Transducer with a bandwidth of 0.1Hz to 16MHz and an accuracy of 1% ± 60mA. The waveforms were captured on a Agilent 200MHz MSOX3024 oscilloscope on the high resolution setting. The high resolution setting uses boxcar averaging to reduce the random noise and increase the effective vertical resolution to 12-bit. FFTs were performed on the 16,000 recorded waveform data points using MATLAB. The bandwidth of the current probes was acceptable for this application as the harmonic content of the current waveforms were only assessed up to the 20^{th} harmonic (1kHz) and due

to the large value of the inductive AC filter any harmonics greater than this will have a minimal value. The Digital PWM signals were captured using the Agilent oscilloscope digital channels directly from the FPGA.

The losses presented in the following section include all of the losses in the system, apart from the gate drive and control circuitry. This includes the losses from the 27kΩ discharge resistor connected to U_{DC}, the 50kΩ shunt resistor for measuring U_{DC}, the 20kΩ shunt resistor for measuring $U_{3\Phi VSI}$ and the three 40kΩ shunt resistors for measuring u_u, u_v and u_w.

As discussed in Chapter 6, the core of the High Frequency (HF) transformer was constructed with an air gap in order to reduce the chance of saturation from an asymmetrical PWM voltage waveform. The losses from the transformer core and magnetizing current was experimentally measured at approximately 30W with a 300V DC link voltage, U_{DC}, when modulating a 150V AC voltage, u_{uvw}. This value was obtained from the power analyser connected to the DC network, with the three Cycloconverter stages disconnected, and therefore includes the switching and conduction losses for the VSI stage. This loss could be reduced if the air gap was reduced or removed, from the reduction in magnetizing current. However this will lead to a much greater chance of saturation and was therefore not experimentally tested.

The clamp circuit also resulted in additional losses from the 94kΩ discharge resistor connected across the DC link of the clamp circuit. A pre-charge circuit was used with the clamp to prevent the converter from tripping when the converter is first enabled. The pre-charge circuit attached to the clamp charged the DC link of the clamp to 775V and under normal operation the clamp voltage did not increase above this value. The clamp pre-charge circuit was not included in the losses measurement and the proportion of losses in the clamp discharge resistor attributable to the pre-charge circuit and the converter was not measured.

To filter the current ripple from the measured 3-Phase AC currents (i_{uvw}) in the DSP, the measurement was performed when the current in the converters was free-wheeling. This results in the measured current in the DSP being up to 0.5A lower than the actual RMS current. To prevent this, the sampling frequency from the analogue sensors could be doubled, sampling the peak and the trough of i_{uvw}

for each PWM pulse. Two values could then be averaged to give a more precise current reading.

8.1.3 Problems and Suggested Solutions

It was found during testing that the converter was not able to operate sufficiently well when providing entirely reactive power on the AC network. When the phase shift between voltage, u_{uvw}, and current, i_{uvw}, was between 65° to 125°, and 245° to 295°, the zero crossing distortion in the current resulted in distorted current waveforms.

A proposed solution to the problem is be to use an alternative modulation approach when a converter phase is under Mode 1 operation. This alternative modulation approach is to short circuit the switching devices when a converter phase (e.g. u_u) is operating under the current threshold of Mode 2 and 3. For a converter without a neutral connection, the other two converter phases (e.g. u_v and u_w), are used to compensate for the loss in voltage. This is only be suitable if the AC current i_{uvw} was considerably larger than the current threshold of Mode 2 or 3. Experimental waveforms for the Cycloconverter, along with the associated FFTs, using this alternative modulation approach are shown in Section 8.7.

8.2 Results for Power Transfer From the DC Network into a Resistive Load

The initial testing of the converters was carried out to establish the losses with power transfer from the DC network to a resistive load. The DC network was connected to the TopCon GSS power supply and the AC network connected to a star connected 3-Phase resistive load bank. For the Cycloconverter this resistive load bank was 26.6Ω and for the Hybrid Cycloconverter this resistive load bank was 32Ω, a 25% increase. The AC current demand, $i_d{}^*$, was increased in 0.2A steps from 1.1A to 7.7A. The reference voltage of the auxiliary 3-Phase VSI DC link in The Hybrid Cycloconverter Topology, $U_{3\Phi VSI}{}^*$, was set at 100V.

8.2.1 Comparison of The Cycloconverter Topology and Hybrid Cycloconverter Topology Losses

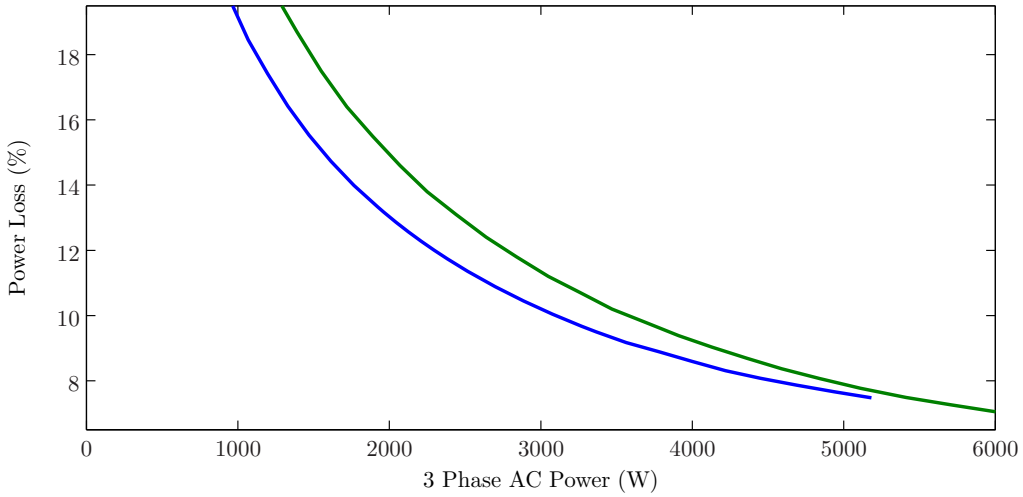


Figure 8.2: Cycloconverter (blue) and Hybrid Cycloconverter (green) power losses against AC power into resistive load

The results from the testing of the converter losses when transferring power from the DC network into a resistive load are shown in Figure 8.2. The Hybrid Cycloconverter has has lower losses for a given power level due to the reduced current and increased voltage for a given power level from the auxiliary 3-Phase VSI. The maximum power from the Hybrid Cycloconverter is 6kW due to the greater voltage avaliable from this converter and this results in a 0.6kW greater maximum power than from the Cycloconverter. The losses in both converters is approximately the same when operating at their respective maximum power. The increase in maximum power from the Hybrid Cycloconverter is is due to the 23% greater 3-Phase AC voltage (u_{uvw}) available from the Hybrid Cycloconverter for a given U_{DC}. A table showing the raw data used for Figure 8.2 is included in Appendix C.

8.2.2 Comparison of the AC Current Quality of the Cycloconverter and Hybrid Cycloconverter Topologies

Figure 8.3 shows the AC currents (u_u, u_v, u_w) from the Cycloconverter when tested with a 3-Phase resistive load as the AC network. The current waveform

has very little distortion as is demonstrated in the FFT of i_u in 8.3 with all harmonics below 0.8%. This level of harmonic distortion is negligible and will not significantly affect the losses in the converter.

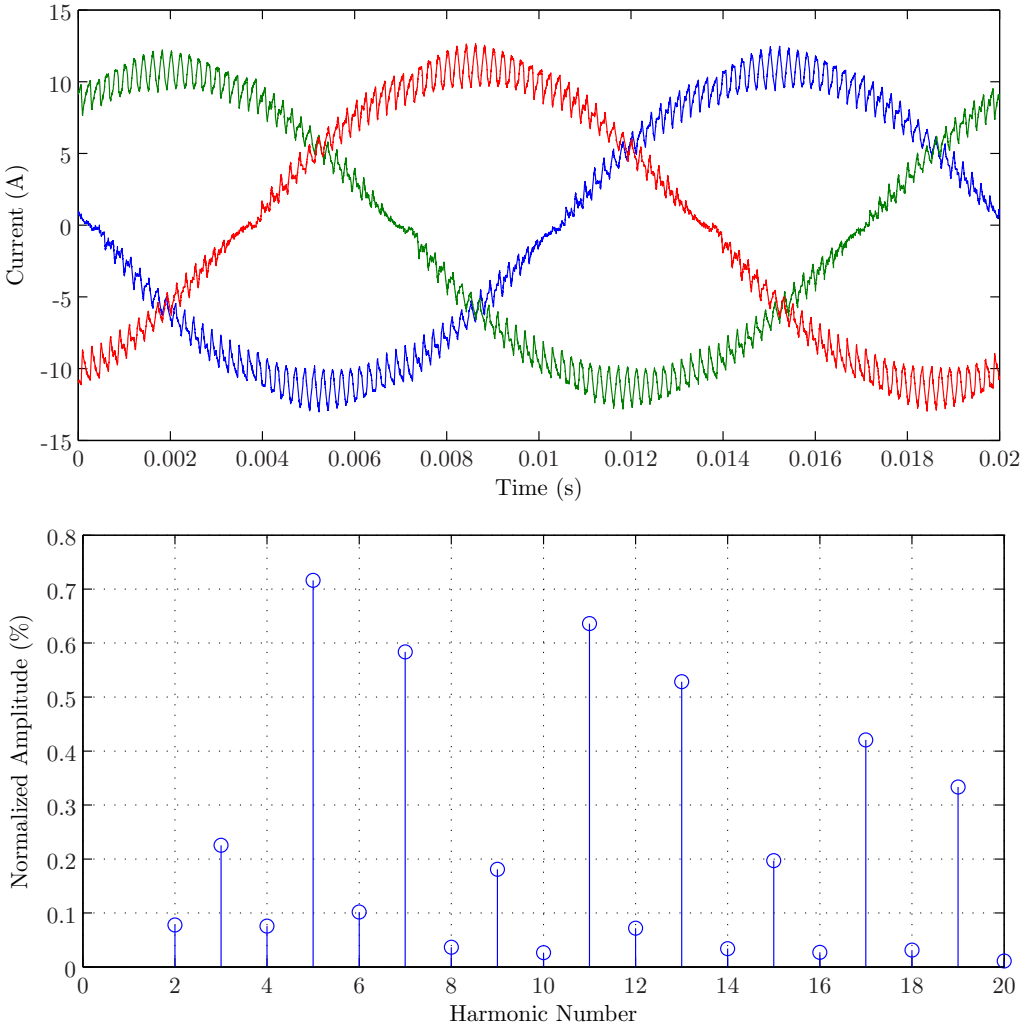


Figure 8.3: Cycloconverter AC currents and associated FFT, u_u (blue), u_v (red) and u_w (green), into 3-Phase resistive load. i_{uvw} = 7.7A RMS

Figure 8.4 shows the AC currents (u_u, u_v, u_w) from The Hybrid Cycloconverter Topology when connected to a resistive load as the AC network. This waveform contains greater harmonic distortion when compared with The Cycloconverter Topology current waveform, as demonstrated in the FFT of i_u, in 8.4(b). In particular there is a 2.4% 5^{th} harmonic with all the other harmonics below 1%. There is additional harmonic distortion on The Hybrid Cycloconverter Topology current waveforms, Figure 8.4, when compared to Cycloconverter Topology current waveforms, Figure 8.3. This could be due to the increase in demanded

voltage from the main converter around the zero crossing in current, resulting in significant zero crossing distortion from Mode 1 operation.

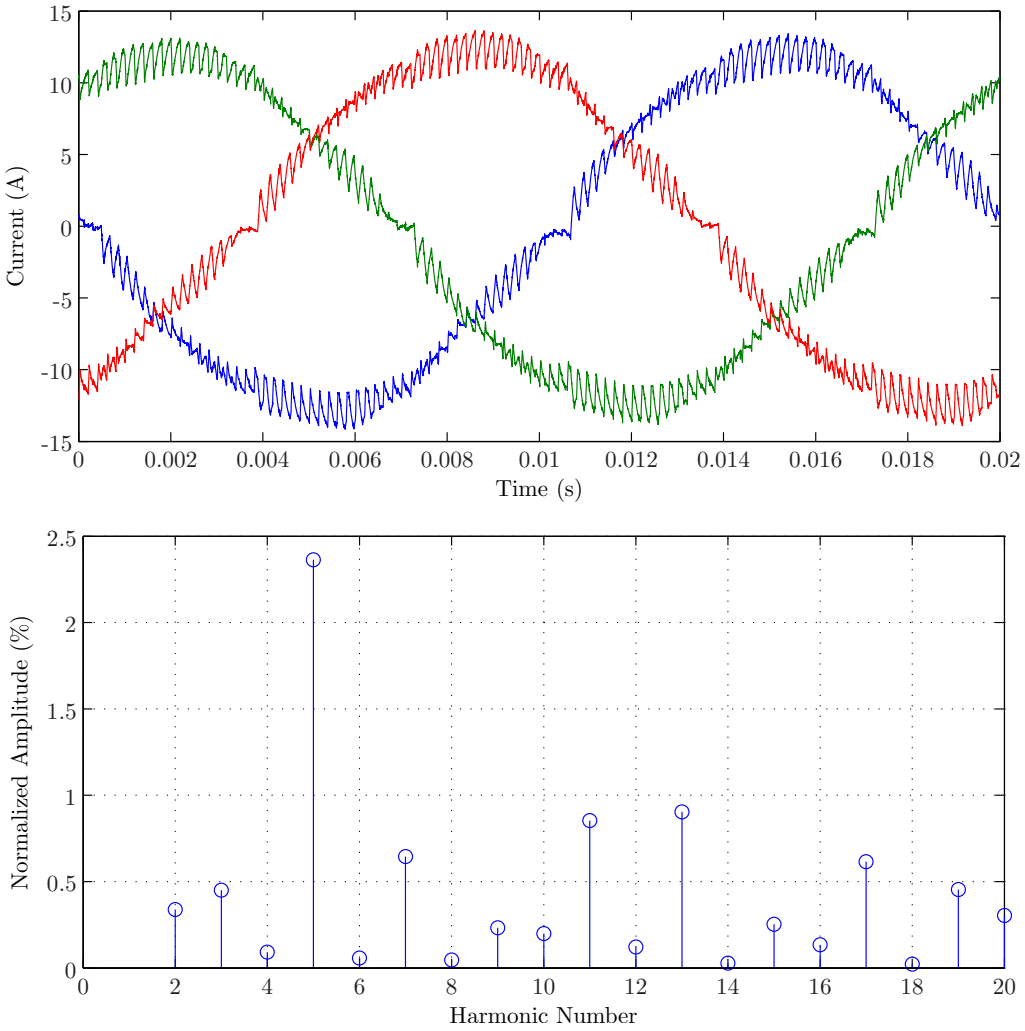


Figure 8.4: Hybrid Cycloconverter AC currents and associated FFT, u_u (blue), u_v (green) and u_w (red), into 3-Phase resistive load, ${U_{3\Phi VSI}}^* = 100$V

8.2.3 Comparison of the AC Voltages of the Cycloconverter and Hybrid Cycloconverter topologies

For this test the PWM voltage waveforms from the Cycloconverter and Hybrid Cycloconverter topologies were captured. This was to verify the effectiveness of the voltage distribution control scheme of The Hybrid Cycloconverter Topology (see Chapter 3 and 7). An FFT was carried out on the captured waveforms to investigate the the effect of injecting the auxiliary VSI voltage terms of fundamental

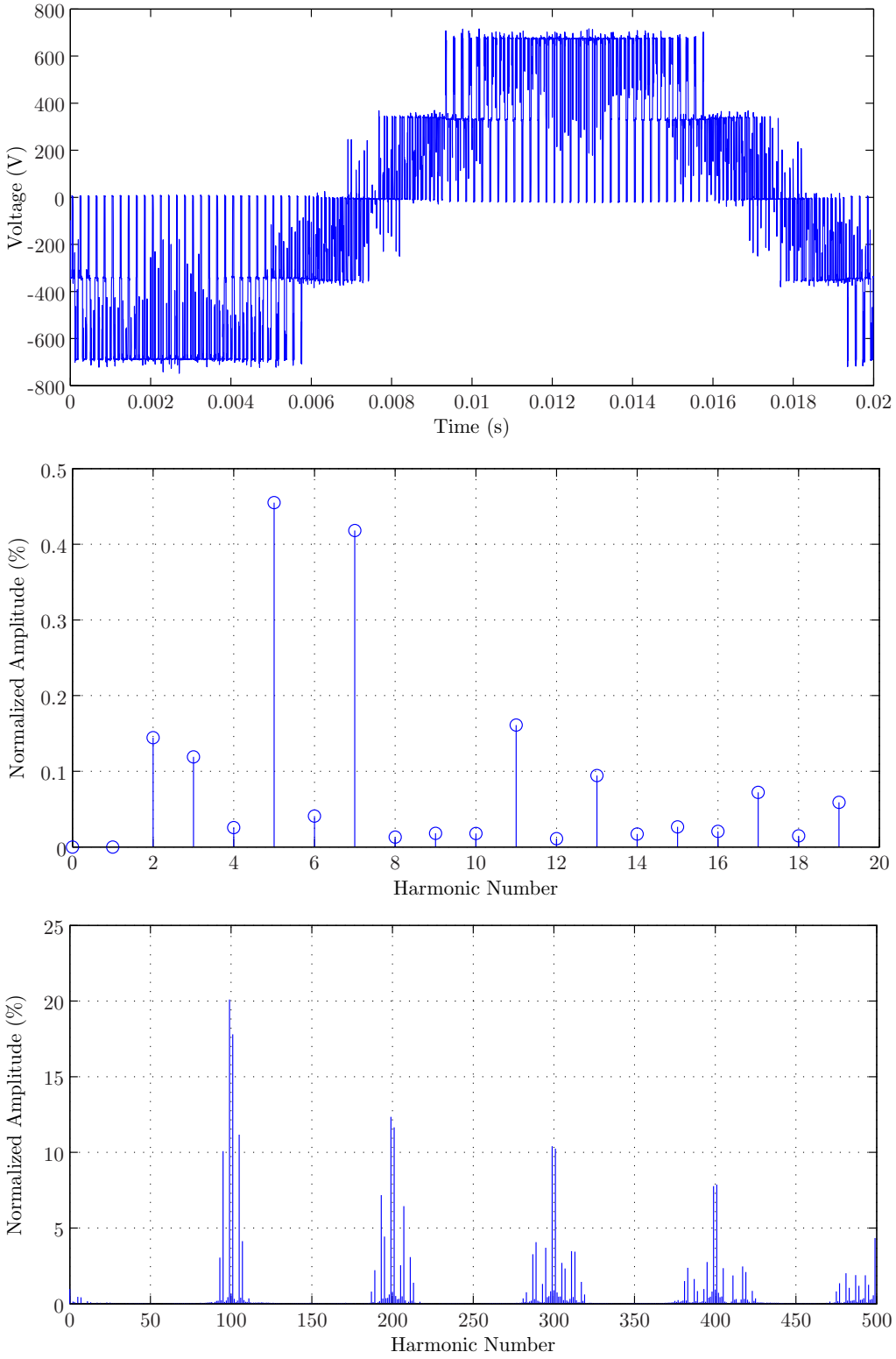
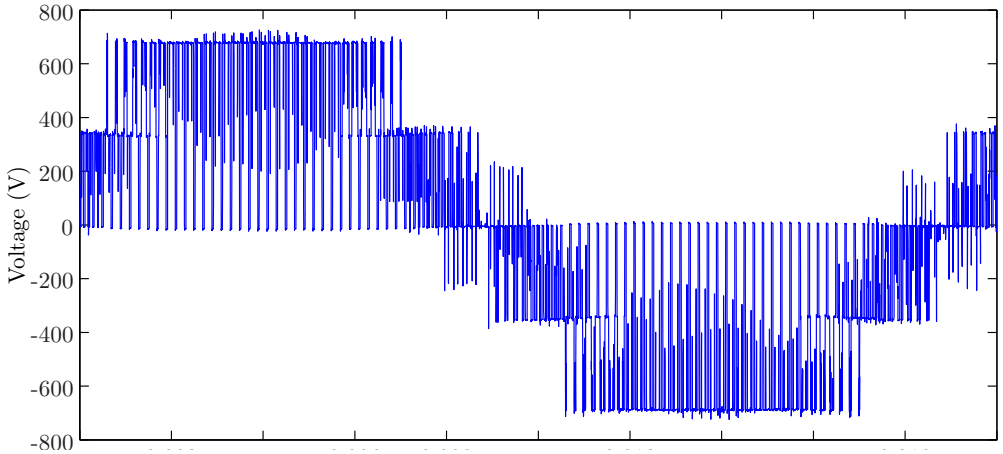
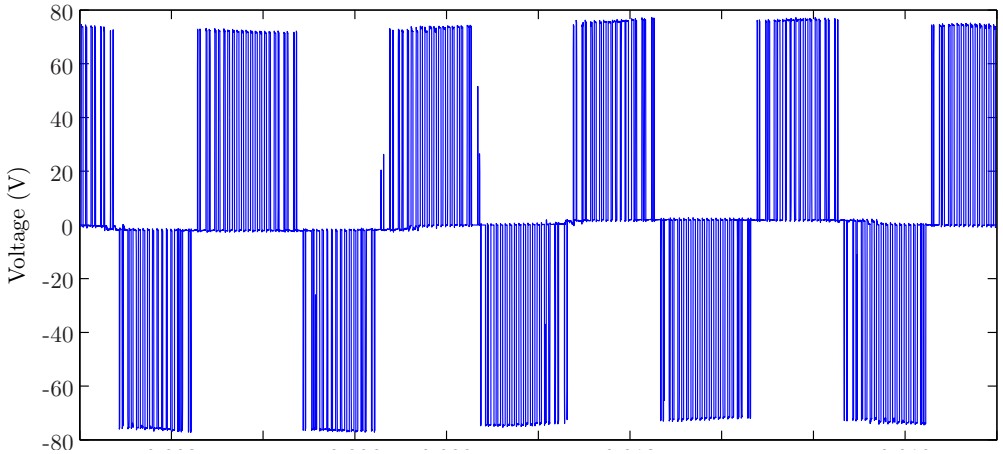


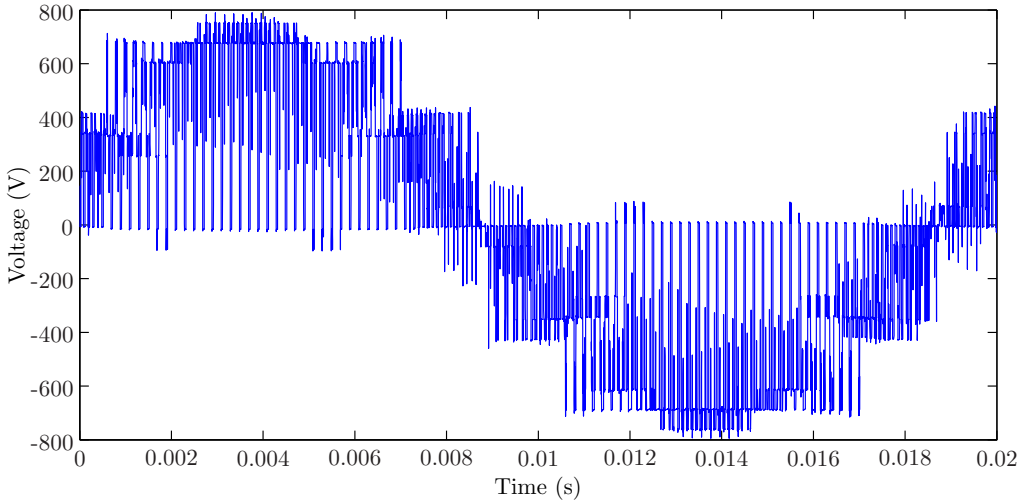
Figure 8.5: Cycloconverter Topology voltage waveform u_A-u_B



(a) Calculated Main Converter Voltage Waveform $(u_{AB}) - (u_{12})$

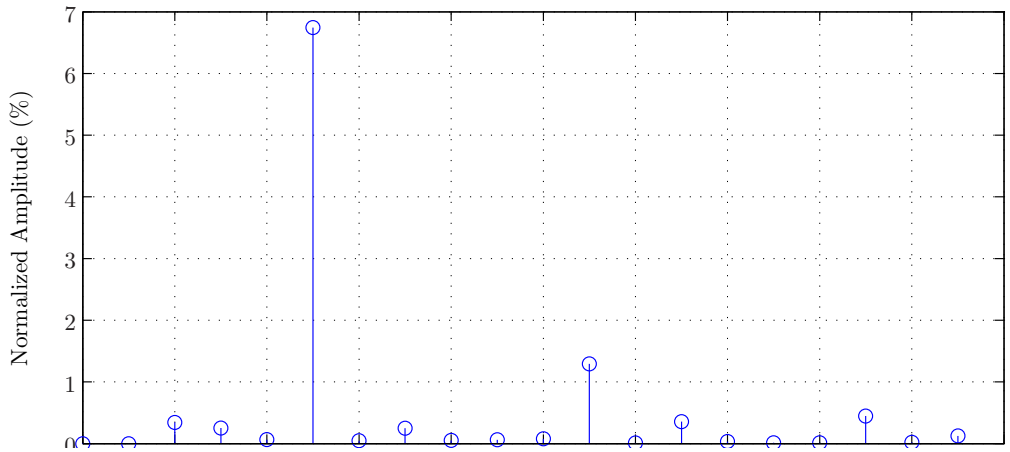


(b) 3-Phase VSI Voltage Waveform u_{12}

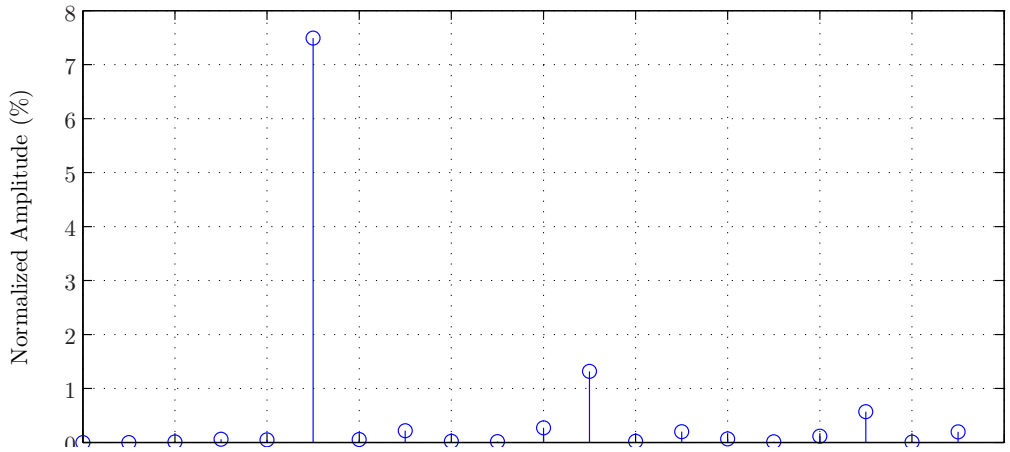


(c) Total Hybrid Cycloconverter Topology Voltage Waveform u_{AB}

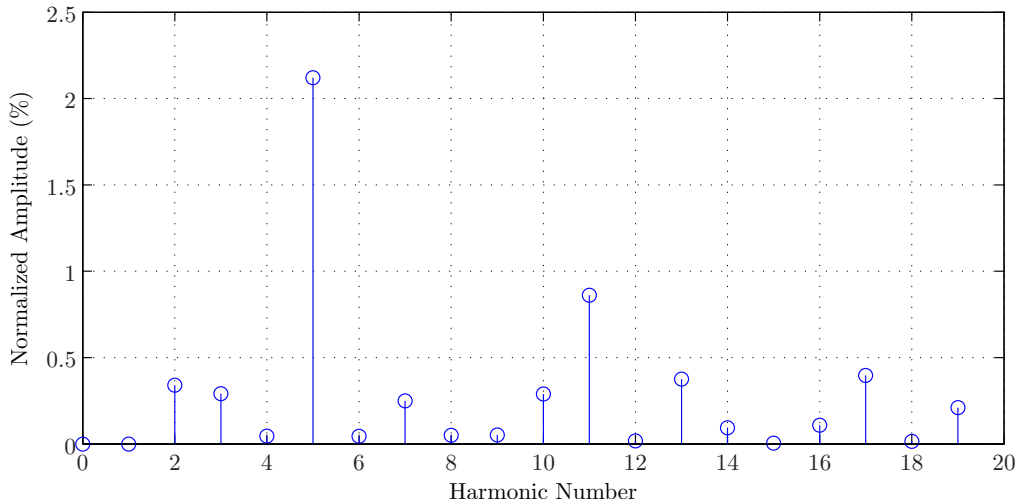
Figure 8.6: Hybrid Cycloconverter Topology voltage waveform



(a) Low Frequency FFT of Calculated Main Converter Voltage Waveform

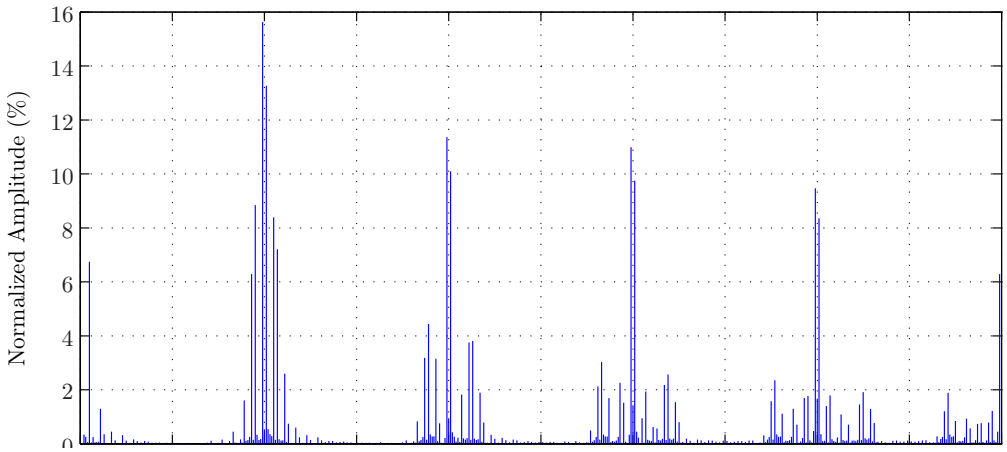


(b) Low Frequency FFT of 3-Phase VSI Voltage Waveform

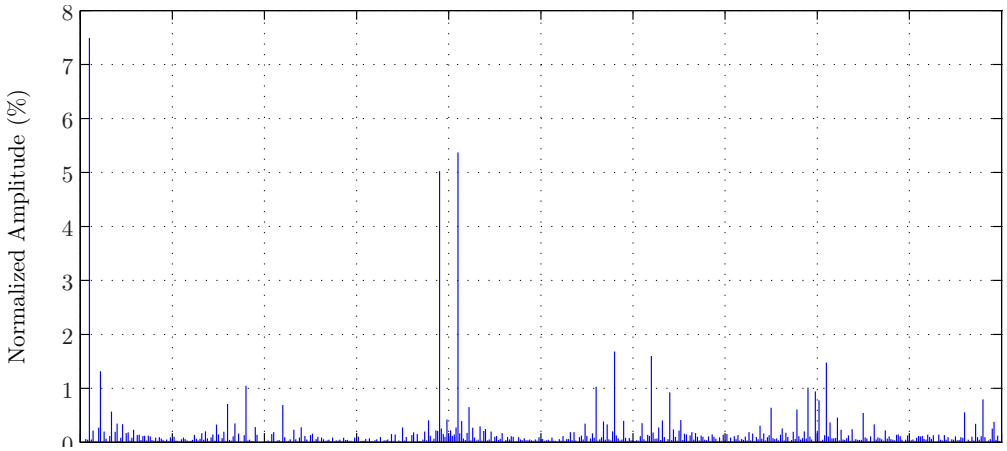


(c) Low Frequency FFT of Total Hybrid Cycloconverter Topology Voltage Waveform

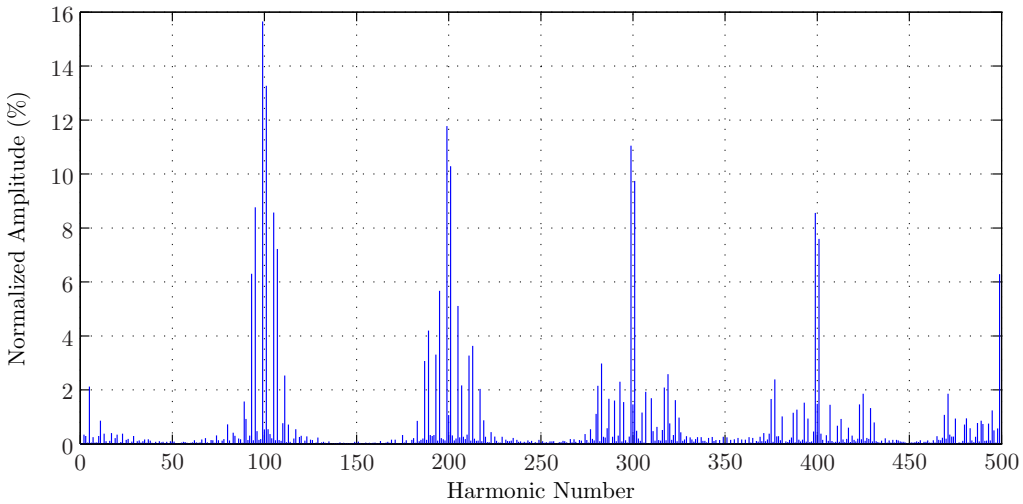
Figure 8.7: Low Frequency FFT of Hybrid Cycloconverter Topology u_u Phase - u_v Phase voltage waveform



(a) High Frequency FFT of Calculated Main Converter Voltage Waveform



(b) High Frequency FFT of 3-Phase VSI Voltage Waveform



(c) High Frequency FFT of Total Hybrid Cycloconverter Topology Voltage Waveform

Figure 8.8: High Frequency FFT of Hybrid Cycloconverter Topology AC u_u- u_v voltage waveform

and switching harmonics when compared with The Cycloconverter Topology.

Figure 8.5 shows the phase-phase voltage waveform, u_{AB} from The Cycloconverter Topology. The voltage probes are connected to u_A and to u_B in Figure 8.1. When operating as a Cycloconverter Topology the terminals of the auxiliary 3-Phase VSI labelled u_1, u_2 and u_3 are connected together. The Low Frequency (LF) FFT of the voltage waveform, Figure 8.5(b), shows that there is very little distortion near the fundamental frequency, with a 0.45% 5^{th} harmonic, a 0.41% 7^{th} harmonic with all other harmonics below 0.2%.

The High Frequency (HF) FFT of The Cycloconverter Topology voltage waveform, Figure 8.5(c), shows that there is a peak at the 99^{th} harmonic, of 20% and a peak of the 101^{st} harmonic of 18%. These switching harmonics are repeated at multiples of the switching frequency PWM with a decreasing amplitude due to the square wave nature of the PWM pulses.

Figure 8.6 shows the phase-phase voltage waveform from The Hybrid Cycloconverter Topology. The voltage probes are connected to u_A and to u_B in Figure 8.1. The LF FFT of the voltage waveform, Figure 8.7(c), illustrates the operation of the voltage distribution scheme. The injected harmonics into the demand voltage to the Main Converter, $u_{main}{}^*$, Figure 8.6(a) contain a 6.8% amplitude 5^{th} harmonic, a 1.2% 11^{th} harmonic and a 0.5% 18^{th} harmonic that is cancelled by a similar amplitude harmonic injected by the auxiliary VSI with opposite phase shift, Figure 8.6(b). The resulting phase-phase voltage waveform, Figure 8.6(c), and associated LF FFT (Figure 8.7 contain much lower amplitude 5^{th}, 11^{th} and 18^{th} harmonics. This voltage division scheme adds some distortion to the AC voltage waveform, due to the additional dead time and conduction losses in the hybrid converter, and this results in a 2.1% 5^{th} harmonic and a 0.8% 11^{th} harmonic, with all other harmonics below 0.5%.

The HF FFT of the voltage waveform, Figure 8.8(c), shows a similar spectrum to The Cycloconverter Topology HF FFT. However the switching harmonic amplitudes are relatively lower due to the 23% increased amplitude fundamental. The auxiliary 3-Phase VSI does not however directly improve the switching harmonic spectrum. Further research could investigate modulation techniques for the auxiliary 3-Phase VSI in order to reduce the switching frequency harmonics

on u_{uvw}.

8.2.4 Analysis of Switching Waveforms

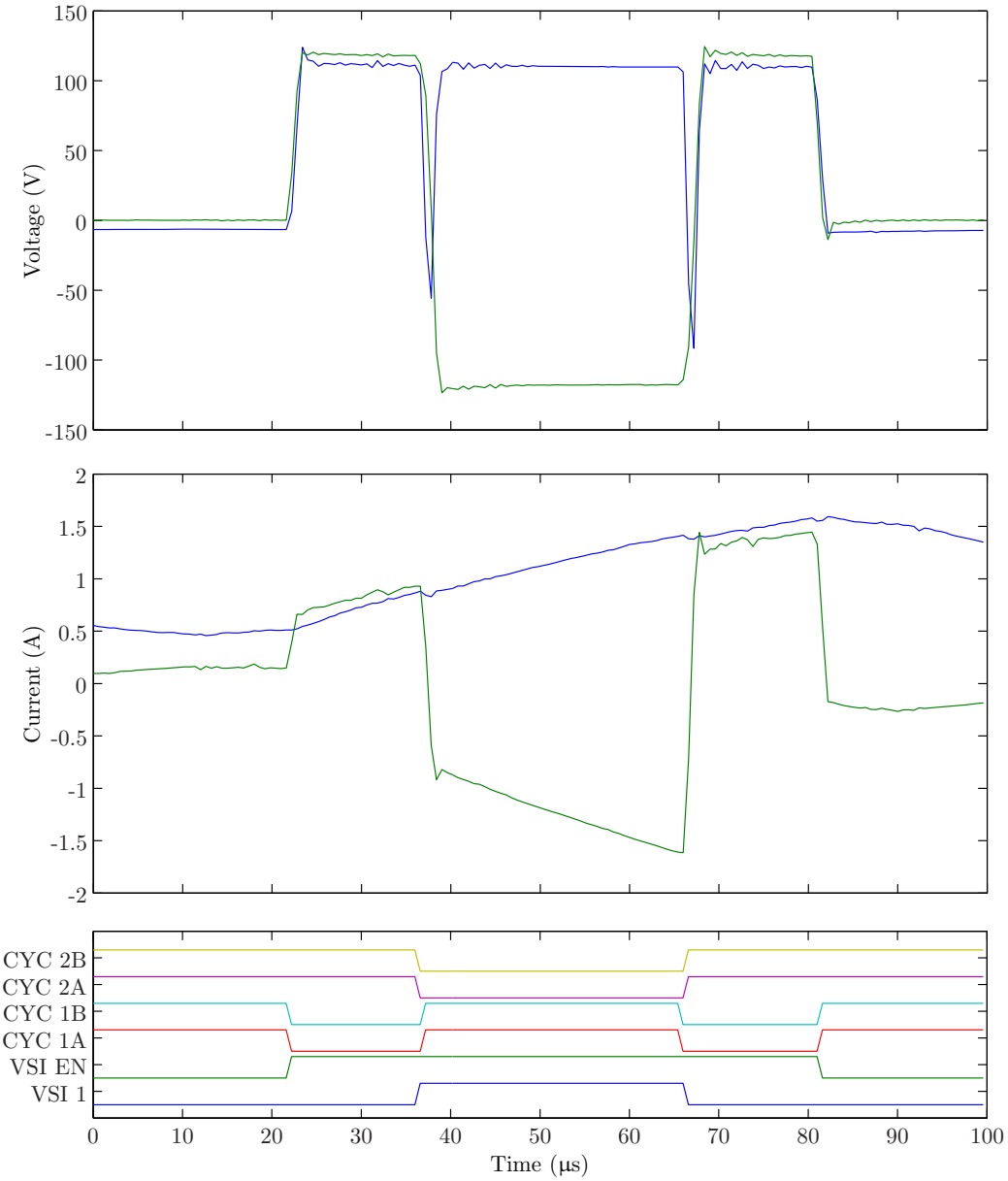


Figure 8.9: Cycloconverter Mode 2: Unknown Current. Blue waveforms u_u and i_u. Green waveforms u_{pri} and i_{pri}

In order to establish the effect of the commutation and switching strategy of the Cycloconverter topology under the three different modes of operation, the voltage

and current waveforms of the transformer primary and AC current waveforms were captured and analysed. This chapter will not repeat the description of the different modes of operation as this has already been covered in Chapter 5. This section will only cover the switching of the Cycloconverter as the switching of the Auxiliary 3-Phase VSI is not novel [72] and both the Cycloconverter and Main Converter in the Hybrid Converter exhibit the same commutation process as is documented in this section.

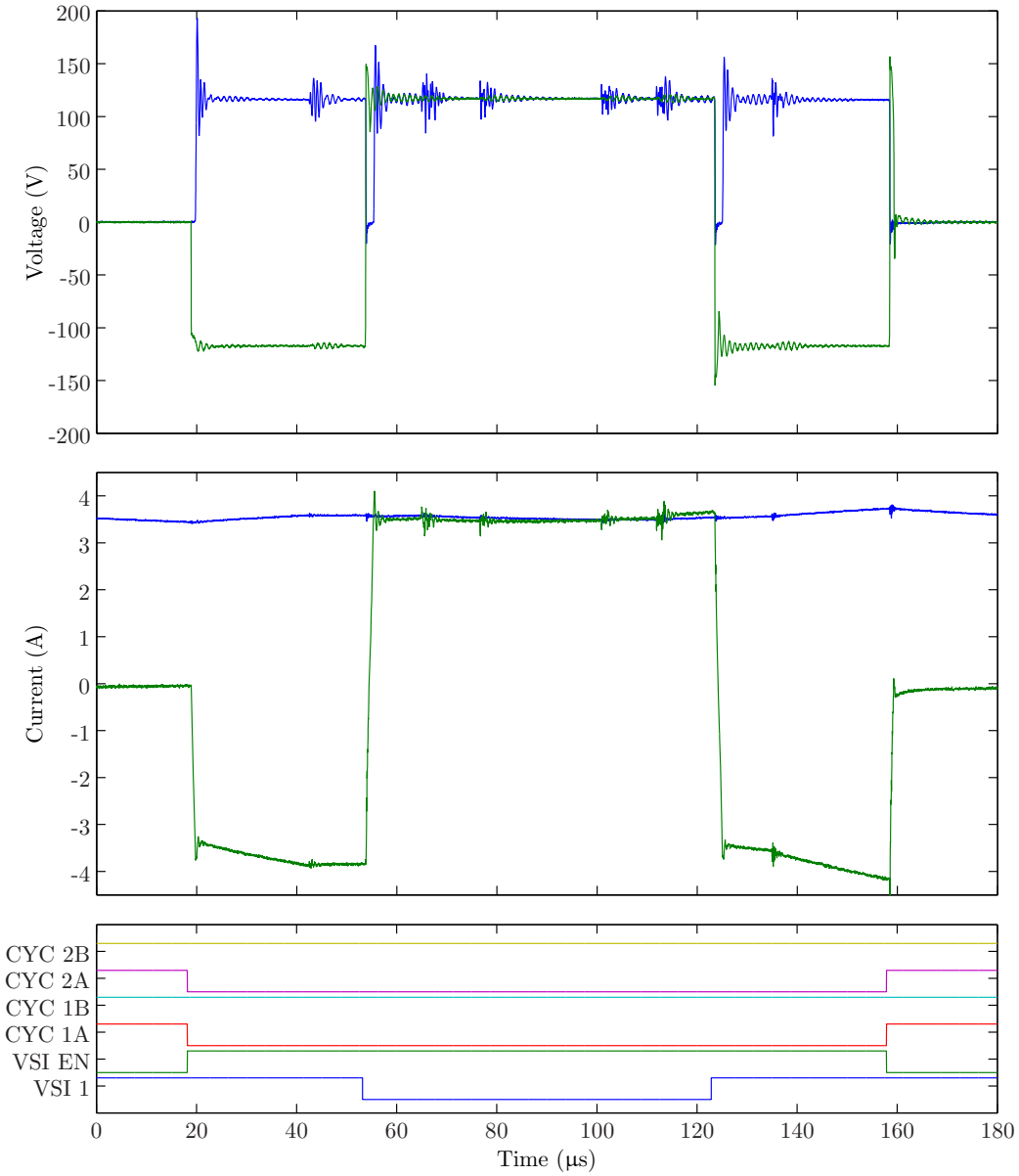


Figure 8.10: Cycloconverter Mode 2: same polarity voltage and current. Blue waveforms u_u and i_u. Green waveforms u_{pri} and i_{pri}

Figure 8.9 shows the voltage and current switching waveforms and PWM pulses

of the Cycloconverter when operating under Mode 1. Only 400 data points were captured for this waveform so it is not possible to see the build up time or the peak voltage overshoot. There is a very small time delay between the first pulses of u_{pri} and the commutation of the converter and the resulting voltage u_u.

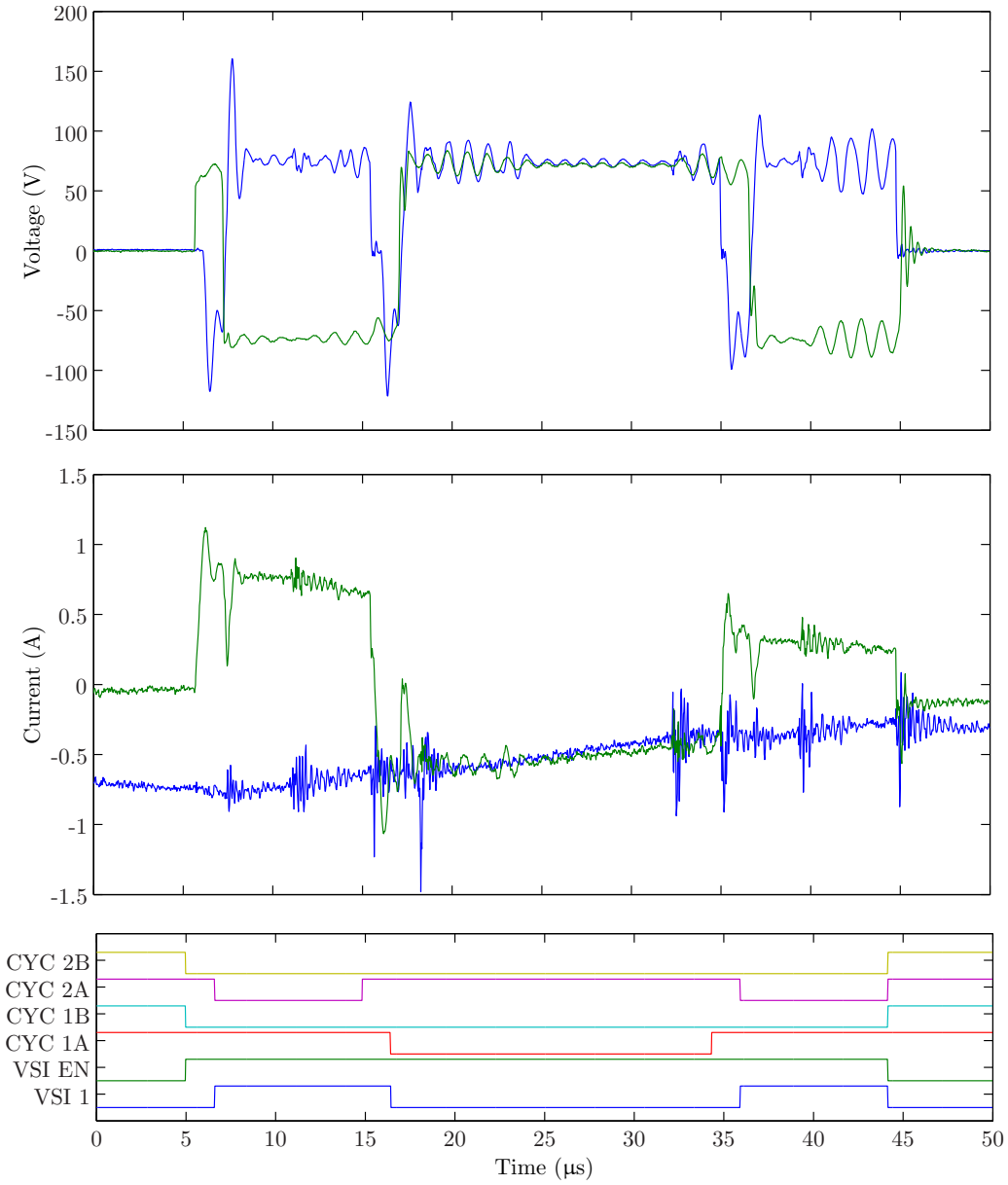


Figure 8.11: Cycloconverter Mode 3: different polarity voltage and current. Blue waveforms u_u and i_u. Green waveforms u_{pri} and i_{pri}

The build up of current in leakage inductance in the HF transformer, i_{pri} to the value of the AC current, i_u. For the second pulse u_u falls to $-U_{DC}$ during the time taken for i_{pri} to reverse polarity and build up to the value of $-i_u$. There is a silght

dip in i_u at this point as the energy to build up the current in the HF transformer is extracted from the AC inductor. Once i_{pri} is equal to i_u, commutation has been performed and u_u rises to U_{DC}. The third pulse repeats the commutation process but in the opposite direction.

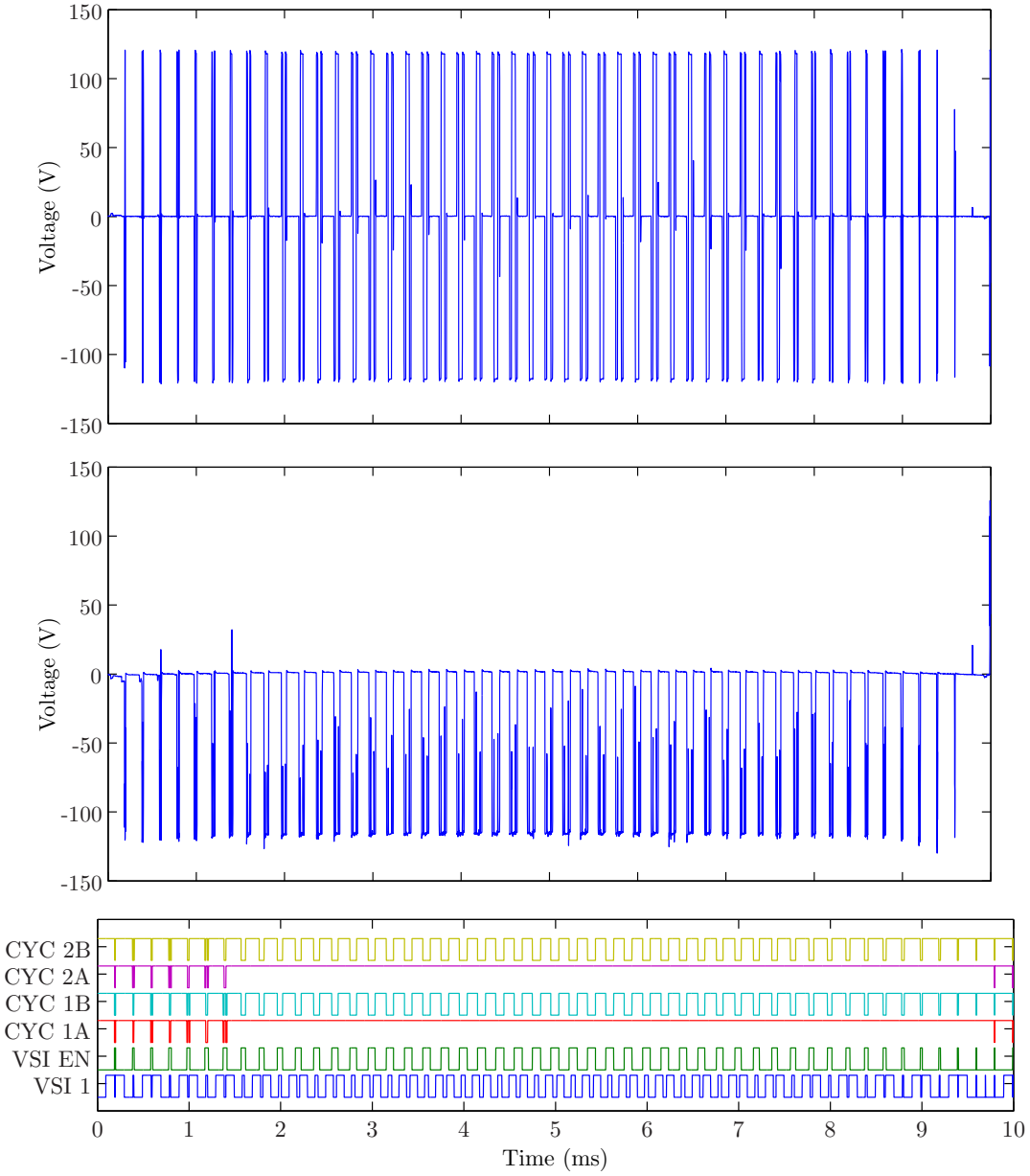


Figure 8.12: Cycloconverter Topology Voltages (u_{pri} top figure, u_u middle figure) and PWM signals (bottom figure)

Figure 8.10 shows the Cycloconverter when operating under Mode 2. This waveform has been captured using the full 16000 data points on the oscilloscope and it more clearly shows the time delay between the voltage pulse on u_{pri} and the

voltage at u_u, during which the current is being built up in the HF transformer leakage inductance and the devices have performed commutation. There is a significant voltage overshoot, of $^2/_3$ of U_{DC}, on u_u from the current overshoot in i_{pri} with respect to i_u due to the reverse recovery in the Cycloconverter diodes. The energy contained in this overshoot results in a damped oscillation from the resonance of the HF transformer leakage inductance and the junction capacitance C_j in the Cycloconverter stage.

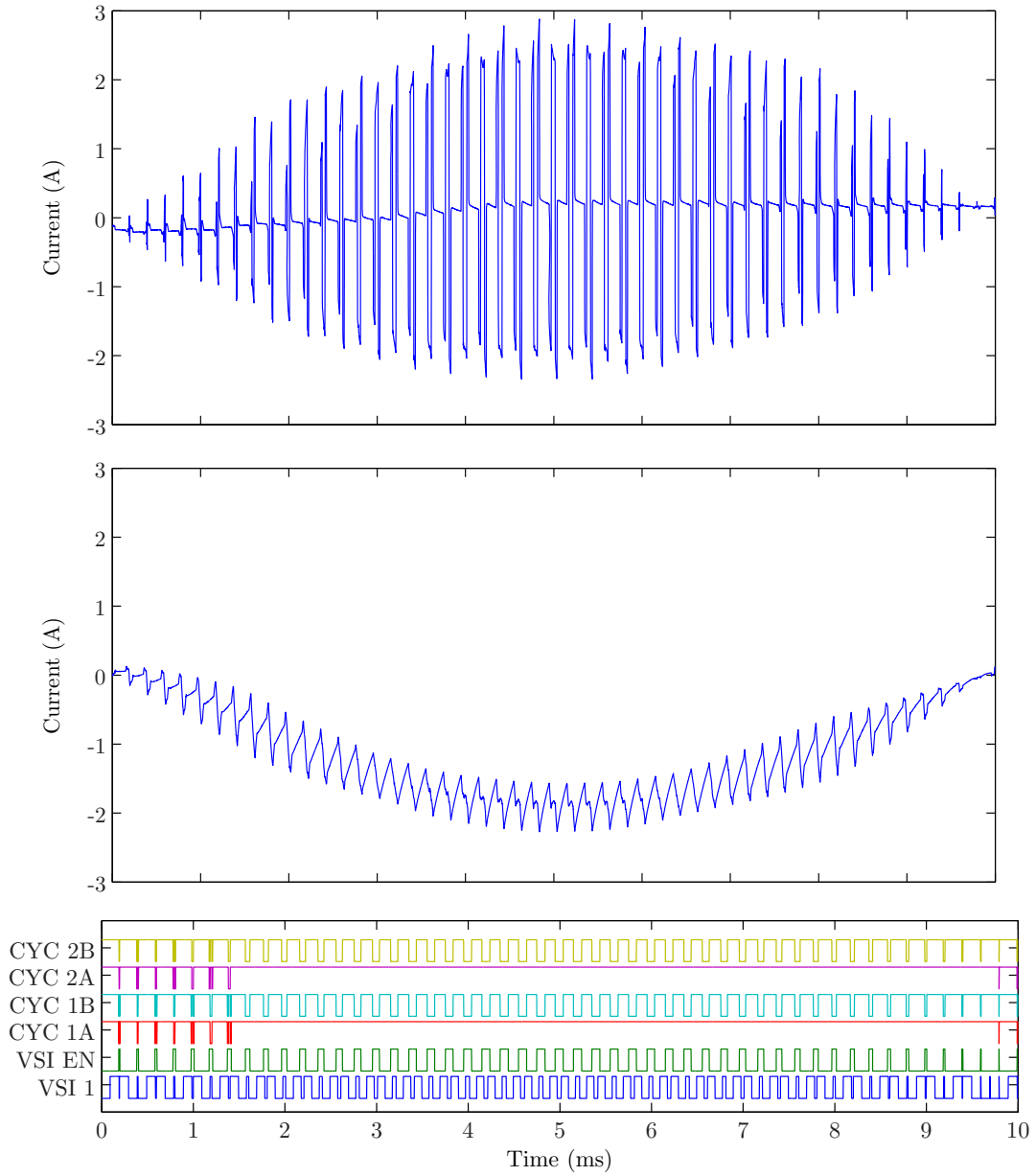


Figure 8.13: Cycloconverter Topology Currents (i_{pri} top figure, i_u middle figure) and PWM signals (bottom figure)

These wavforms show the same features as the waveforms from the simulated converter in Chapter 4, Section 4.3.7. The switching of the other converter phases also causes resonance on u_u. At the end of the third pulse there is a positive spike on u_{pri} where the the energy contained in the leakage inductance of the transformer is transferred back to U_{DC} via the diodes in the VSI.

Figure 8.11 shows the voltage and current waveforms when the Cycloconverter is operating under Mode 3. This waveform is captured using the oscilloscopes full 16,000 data points but due to the lower time base the resonance from the switching of the Cycloconverter can be seen more clearly. The frequency of oscillation is approximately 1MHz and at this frequency the skin effect will cause the resistance of the HF transformer to dampen the oscillations quickly.

Figures 8.12 and 8.13 show the current and voltage waveforms from the Cycloconverter for half a 50Hz cycle. For the first 1.5mS the converter is operating in Mode 1 and for the last 0.25mS the converter is operating under Mode 3. For the rest of the half cycle the converter is operating in Mode 2. These graphs show the unfolding of the voltage generated by the VSI, Figure 8.12, by the Cycloconverter stage and the the resulting current waveform, Figure 8.13, under all modes of operation. For these figures the top waveform are the prmary voltage and current waveforms (u_{pri} and i_{pri}), and the middle figures are the AC voltage and current waveforms (u_u and i_u).

8.3 Results for Power Transfer from the AC to DC Networks

The second set of tests were carried out to establish the losses in the converters with the DC network connected to the Regatron TopCon GSS DC power supply and the AC network connected to the Regatron TC.ACS Programmable 3-Phase AC power supply.

The 3-Phase d-axis AC current demand, $i_d{}^*$ was increased in 0.5A increments from 2A to 15A. The test was carried out with a DC link voltage, U_{DC} of 350V and an AC voltage, u_{uvw}, of 150V RMS for The Cycloconverter Topology and

185V RMS for The Hybrid Cycloconverter Topology. This represents a 23% increase, as expected from the addition of the auxiliary 3-Phase VSI. Both of these converters were operating near their corresponding maximum Modulation Index (MI).

8.3.1 Comparison of The Cycloconverter Topology and Hybrid Cycloconverter Topology Losses

Figure 8.14 shows the losses results from the Cycloconverter and Hybrid Cycloconverter topologies with the transfer of power from the AC network to the DC network. The percentage lost in The Cycloconverter Topology reaches a minimum value of 10% at 3.5kW AC power. With increasing AC power, the percentage power lost in the converter rises to a maximum value of 10.6% when the converter is operating at the maximum power of 6.8kW.

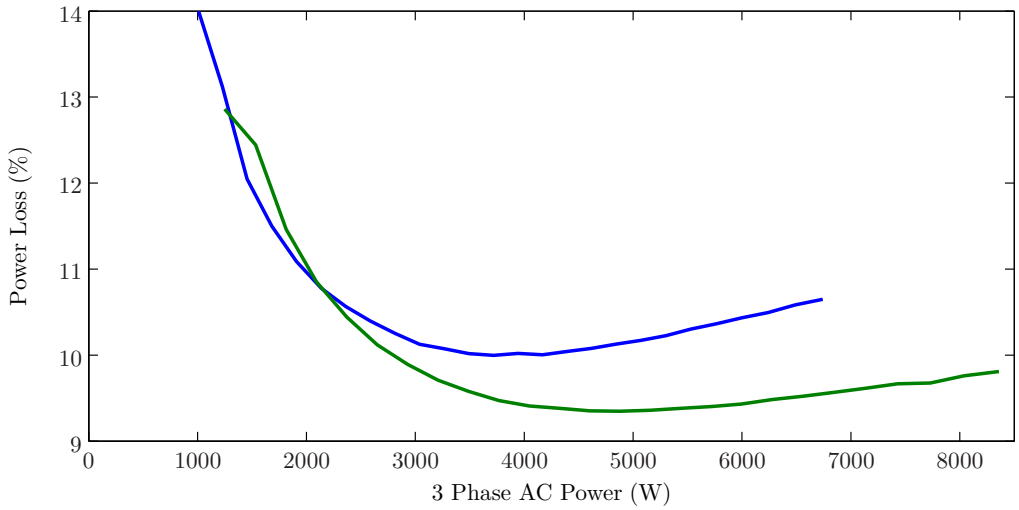


Figure 8.14: Cycloconverter Topology (blue) and Hybrid Cycloconverter Topology (green) power losses against AC power (power transfer from AC network to DC network)

The percentage lost in The Hybrid Cycloconverter Topology reaches a minimum value of 9.4% at 4kW AC power. With increasing AC power the percentage of power lost in this converter remains at a fairly constant value up until 6kW whereupon rising to 9.8% when the converter is operating at the maximum power of 8.3kW

This results shows that the additional auxiliary 3-Phase VSI in The Hybrid Cycloconverter Topology is able to significantly increase the utilization of the installed power in HF transformer and switching devices whilst improving on the losses in the converter above 2kW by 0.5-1%. The experimental data used for Figure 8.14 is included in Appendix C.

8.3.2 Comparison of AC Current Quality for Cycloconverter and Hybrid Cycloconverter Topologies

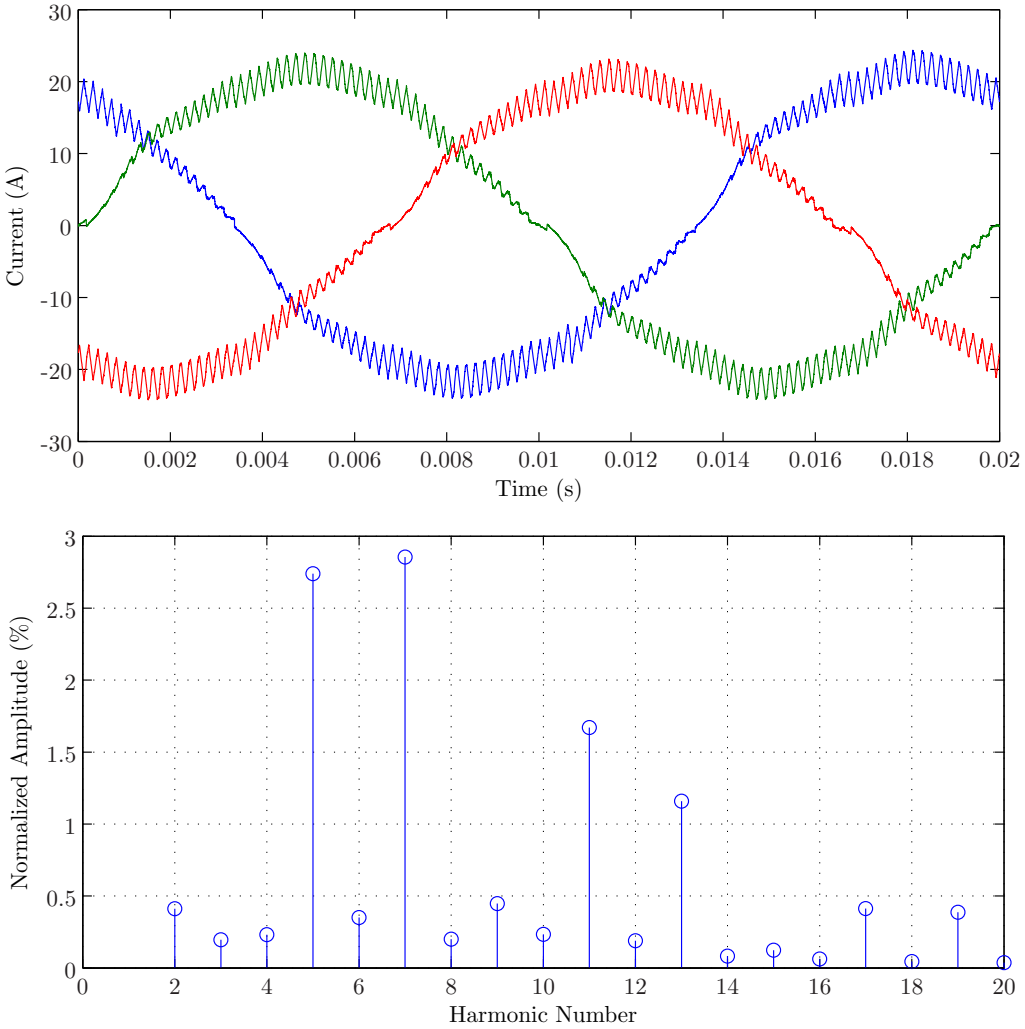


Figure 8.15: Cycloconverter Topology currents and associated FFT, excluding fundamental. i_{uvw} 15A RMS, u_{uvw} 150V RMS, U_{DC} 350V.

Figure 8.15 shows the 3-Phase AC currents, i_{uvw}, and associated FFT of i_u from The Cycloconverter Topology when transferring power from the AC network to the DC network. There is a noticeable zero crossing distortion present in each current waveform, due the operation of the converter in Mode 1. Because of the lack of a neutral connection, this distortion is distributed over the 3 phases, resulting in a glitch in each current 6 times per cycle, resulting in a 5^{th} and 7^{th} harmonic. The FFT of the current waveform, Figure 8.15 shows a 2.9% amplitude 7^{th} harmonic and 2.8% amplitude 5^{th} that is the result of this glitch.

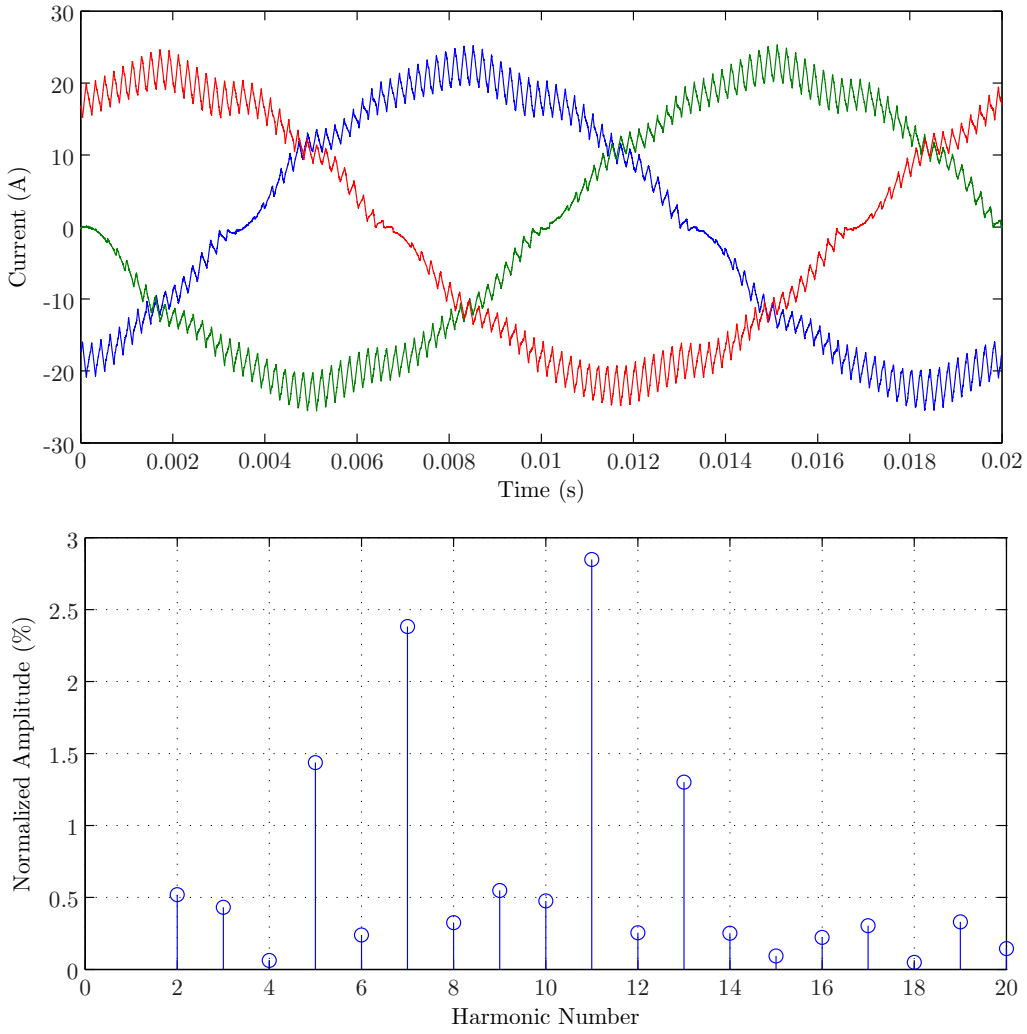


Figure 8.16: Hybrid Cycloconverter Topology currents and associated FFT, excluding fundamental. i_{uvw} 15A RMS, u_{uvw} 150V RMS, U_{DC} 350V, U_{VSI} 100V.

Figure 8.16 shows the 3-Phase AC currents, i_{uvw}, and associated FFT of i_u from The Hybrid Cycloconverter Topology when transferring power from the AC network to the DC network. As well as the zero crossing glitch from the Main

Converter, the waveform has additional distortion from the voltage distribution between the Main Converter and auxiliary 3-Phase VSI. The FFT of the current waveform, Figure 8.16 shows a 2.8% amplitude 11^{th} harmonic, a 2.4% amplitude 7^{th} and a 1.5% amplitude 5^{th} that is the result of the zero crossing glitch and the voltage distribution scheme between the Auxiliary and Main Converter.

8.4 Results for Power Transfer from the DC to AC Networks

The third set of tests were carried out to establish the losses in the converters with the DC network connected to the Regatron TopCon GSS power supply and the AC network connected the Regatron TC.ACS bi-directional programmable 3-Phase AC source with power transfer from the DC network to the AC network.

The 3-Phase d-axis AC current demand, $i_d{}^*$ was increased in 0.5A increments from 2A to 15A. The test was carried out with a DC link voltage, U_{DC} of 350V and an AC voltage, u_{uvw}, of 150V RMS for The Cycloconverter Topology and 185V RMS for The Hybrid Cycloconverter Topology which represents a 23% increase. Both of these converters were operating near their corresponding maximum MI.

8.4.1 Comparison of The Cycloconverter Topology and Hybrid Cycloconverter Topology Losses

Figure 8.17 shows the losses results from The Cycloconverter Topology and Hybrid Cycloconverter Topology with the transfer of power from the DC network to the AC network. At low power levels The Cycloconverter Topology has a greater efficiency, however above 2.5kW The Hybrid Cycloconverter Topology has lower losses.

Above 2.5kW the percentage lost in The Cycloconverter Topology reaches a minimum value of 9.3% at 2.5kW AC power. With increasing AC power the percent-

age of the power lost in the converter rises to a maximum value of 10.7% when the converter is operating at the maximum power of 7kW.

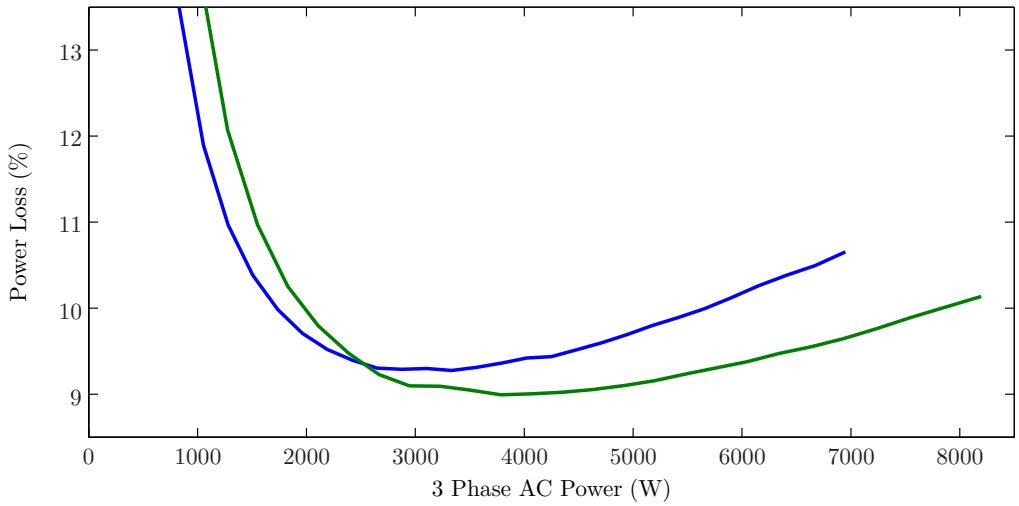


Figure 8.17: Cycloconverter (blue) and Hybrid Cycloconverter topologies (green) power losses against AC power, power transfer from DC network to AC network

Above 2.5kW the percentage lost in The Hybrid Cycloconverter Topology reaches a minimum value of 9% at 4kW AC power. With increasing AC power the percentage power loss in this converter rises to a maximum value of 10.1% when the converter is operating at the maximum power of 8.2kW.

These results show that the auxiliary 3-Phase VSI in The Hybrid Cycloconverter Topology is able to significantly increase the utilization of the installed power in HF transformer and switching devices whilst improving on the losses in the converter above 2.5kW by around 0.5-1%. The experimental data used for Figure 8.14 is included in Appendix C.

When operating with power transfer from the DC network to the AC network, both the Cycloconverter and Hybrid Cycloconverter topologies have an increased efficiency at medium power levels compared to the case when operating with a power transfer from the AC network to the DC network. This is due to the additional switching losses required for Mode 3 operation, as demonstrated in the switching loss simulation in Chapter 4.

8.4.2 Comparison of The Cycloconverter Topology and Hybrid Cycloconverter Topology AC Currents

Figure 8.18 shows the 3-Phase AC currents, i_{uvw}, and associated FFT of i_u from The Cycloconverter Topology when transferring power from the DC network to the AC network. The current waveform contains a significant zero crossing distortion. The FFT of the current waveform shows that the distortion in AC grid voltage results in a waveform containing 1.4% 13^{th}, 1.8% 11^{th}, 3.2% 7^{th} and a 2.9% 5^{th} harmonic.

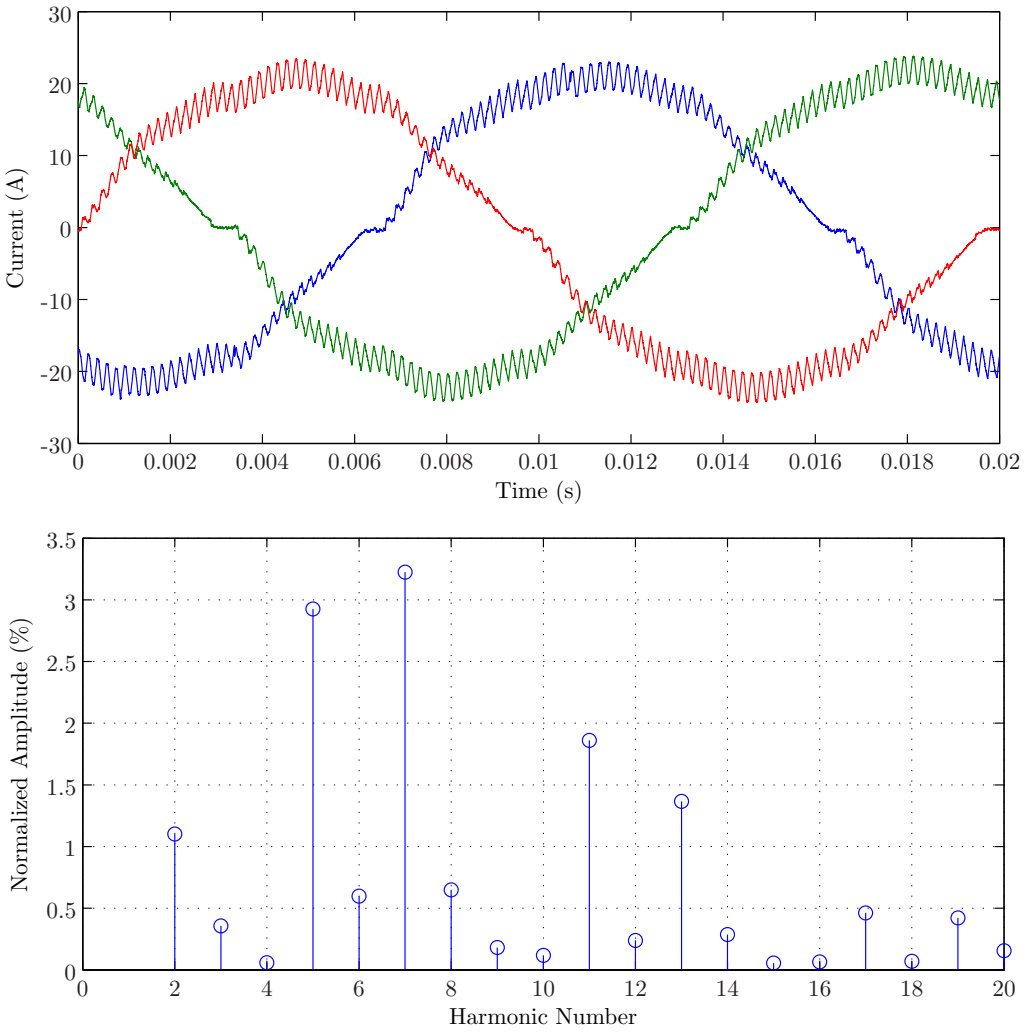


Figure 8.18: Cycloconverter Topology currents and associated FFT, excluding fundamental. i_{uvw} 15A RMS, u_{uvw} 150V RMS, U_{DC} 300V.

Figure 8.19 shows the 3-Phase AC currents, i_{uvw}, and associated FFT of i_u from

The Hybrid Cycloconverter Topology when transferring power from the DC network to the AC network. The zero crossing distortion from the Main Converter and the distortion arising from the voltage distribution control between the Main Converter and auxiliary 3-Phase VSI result in a distorted current waveform. The FFT, Figure 8.19(b), shows a 1.2% 13$^{\text{th}}$ harmonic, a 2.8% 11$^{\text{th}}$ harmonic, a 2.3% 7$^{\text{th}}$ harmonic and a 1.6% 5$^{\text{th}}$ harmonic.

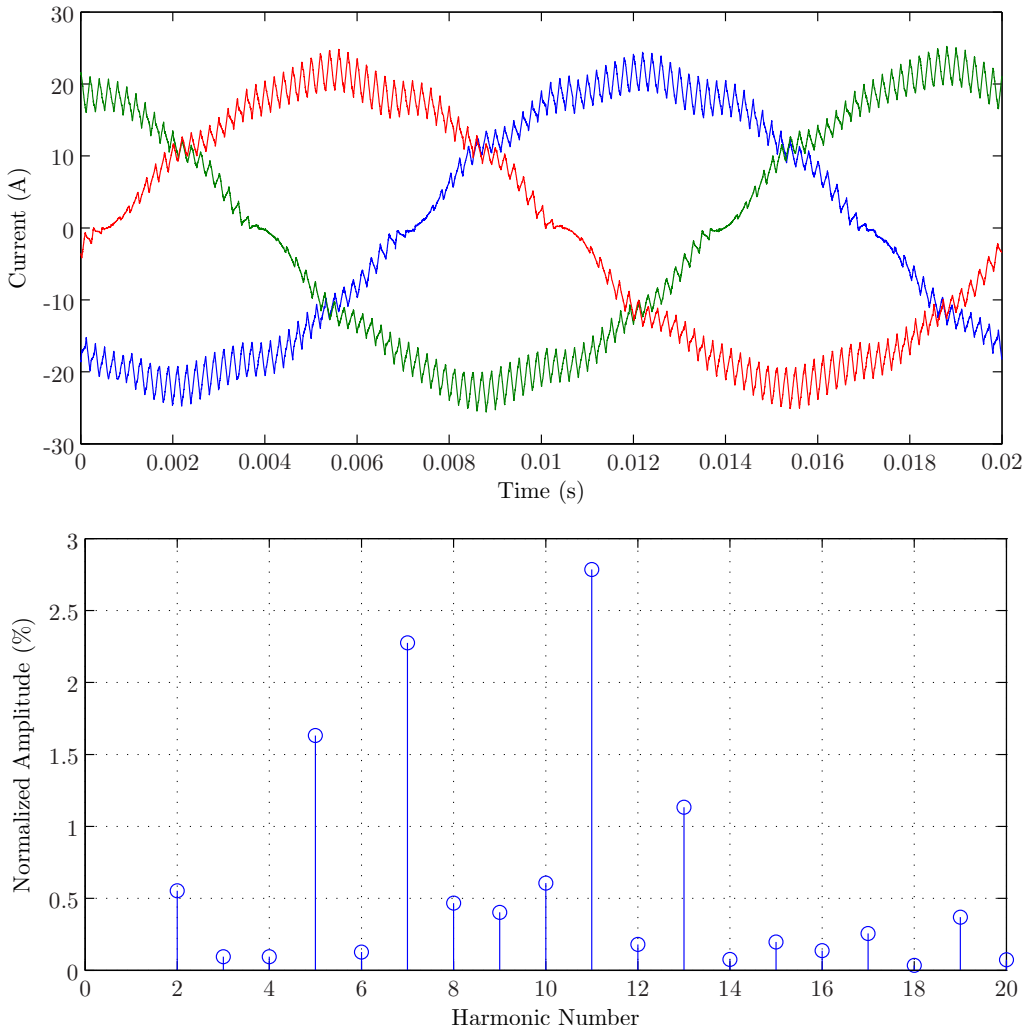


Figure 8.19: Hybrid Cycloconverter Topology currents and associated FFT, excluding fundamental. i_{uvw} 15A RMS, u_{uvw} 150V RMS, U_{DC} 300V, U_{VSI} 75V.

8.5 Results for Power Transfer across the range of power factor angles

The fourth set of tests were carried out to establish the losses in the converters with the DC network connected to the Regatron TopCon GSS power supply and the AC network connected the Regatron TC.ACS bi-directional programmable 3-Phase AC source. The phase shift between $i_{uvw}{}^{*}$ u_{uvw}, was increased in 11.25° increments from 0° to 360°, with $i_{uvw}{}^{*}$ set at 10A RMS. The test was carried out with a DC link voltage, U_{DC} of 350V and an AC voltage, u_{uvw}, of 150V RMS for The Cycloconverter Topology and 185V RMS for The Hybrid Cycloconverter Topology which represents a 23% increase. Both of these converters were operating near their corresponding maximum MI.

Figure 8.20 shows the real AC power, the DC power and the total converter losses for the Cycloconverter and Hybrid Cycloconverter topologies from 0° to 360°. The results show maximum losses at 180° due to the additional switching losses from the converter operating under Mode 3. When processing reactive power, with a phase shift of 90° or 270° the losses in both converters is at a minimum due to the peak current from the converter coinciding with the minimum duty cycle in the VSI, resulting in lower power losses in the VSI. However increased distortion in i_{uvw} at specific phase angels results in increased losses in the AC inductor that is evident in the non-smooth power loss graphs in Figure 8.20. This is due to the zero crossing distortion from both converters when operating under Mode 1.

The losses in the Cycloconverter are consistently greater than the losses in the Hybrid Cycloconverter with all phase shift angles by at least 0.1%. The maximum occurs at 180° where the losses in the Cycloconverter are 0.5% greater than the losses in the Hybrid Cycloconverter Topology.

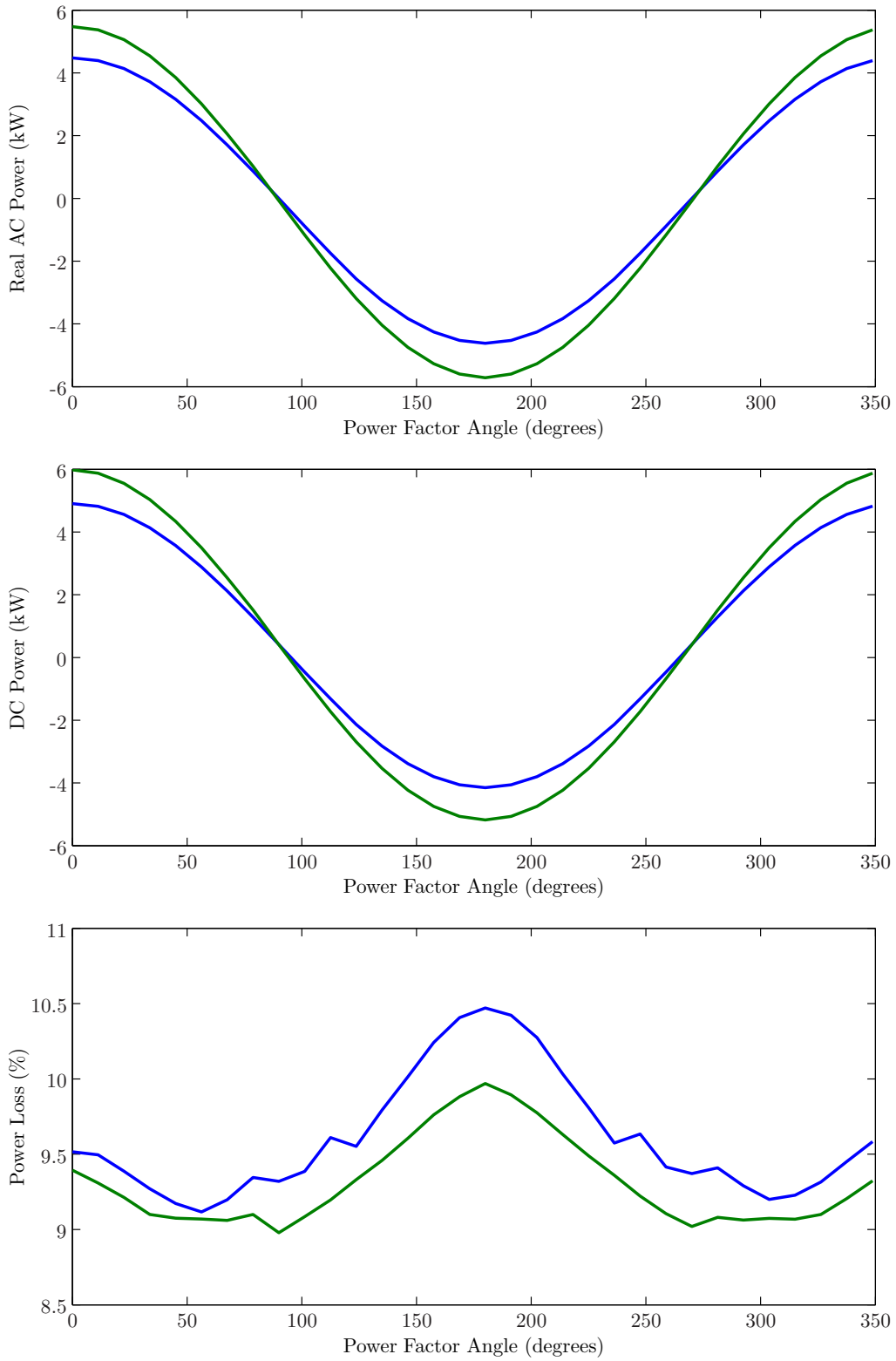


Figure 8.20: Losses in Cycloconverter (Blue) and Hybrid Cycloconverter (Green) against phase shift between voltage and current

8.6 Discussion of Results in Relation to Simulation

The converter losses simulation, presented in Chapter 4, was carried out before the design of the experimental converter was finalized. Therefore a direct comparison between the experimental converter loss results and the losses results in Chapter 4 can not be made and a second simulation, carried out with the exact devices and paramenters, was not carried out due to time restraints. This is due to differences between the experimental and simulated converter and the different testing parameters. A further simulation with models designed from the experimental converter was not carried out due to time restraints. The converter was simulated with a DC link voltage of 400V and an AC voltage of 230V RMS for The Cycloconverter Topology and 280V RMS for The Hybrid Cycloconverter Topology. The experimental converter was tested with a DC link voltage of 350V with an AC voltage of 150V RMS for The Cycloconverter Topology and 185V RMS for The Hybrid Cycloconverter Topology. As the majority of the losses in the converters are conduction losses, an increase in AC voltage results in an increase in converter power without a significant increase in converter losses. This results in reduced power losses as a percentage of output power.

The simulation used was carried out using Infineon FS35R12WT4 IGBTs for all switching devices in The Cycloconverter Topology. The auxiliary 3-Phase VSI in The Hybrid Cycloconverter Topology used IRF4228PfB MOSFETs as the switching devices in the auxiliary 3-Phase VSI. In the experimental converter the IGBTs used were the Semikron SK30GH123 for the Single Phase VSI stage, IXDR30N120D1 for the Cycloconverter stage and FS30R06W1E3 for the auxiliary 3-Phase VSI. The IGBTs used in the simulation and experimental converter will show a similar level of switching and conduction losses, however the losses in the auxiliary 3-Phase VSI will be considerably reduced, both switching and conduction, due to the use of IGBTs instead of MOSFETs in the experimental converter.

The simulation in Chapter 4 only investigated the conduction and switching losses in the switching devices. The results contained in this chapter contain the total system losses from the transferring power between the AC and DC network. The losses in the transformer and line inductor will have a significant impact on the

losses in the experimental converter resulting in a higher percentage of losses in this chapter compared with the losses presented in Chapter 4.

The work presented in Chapter 4 is still valid and trends apparent in simulation results show similarities to trends in the experimental converter results. Approximately there is 2% increase in converter losses at rated power when transferring power from the DC network to the AC network compared with transferring power from the AC network to the DC network, both in simulation and experimental results. This is due to the increased switching losses for the current build up in Mode 3 modulation. The increase in conduction losses between low and medium power operation, and between medium power and high power operation show approximately a 0.5% increase in converter losses for both the simulation and experimental results.

The fourth test that tested the converters' with a phase shift between voltage and current from 0° to 360° shows a similar trend to the losses presented in the simulation study in Chapter 4 with the maximum losses for both the Cycloconverter and Hybrid Cycloconverter occurring with a phase shift between voltage and current of 180° and 0°. The losses at 180° are bigger than the losses at 0° due to the increased switching under Mode 1 operation and this in evident in both the simulations and experimental results. The Cycloconverter has greater losses experimentally than the Hybrid Converter than in simulation, however as the simulation only took into account the losses in the switching devices, this discrepancy could be due to the reduced losses in the HF transformer in the Hybrid Converter when operating with these phase shifts.

8.7 Zero Crossing Compensation

In order to compensate for the zero crossing distortion in the Cycloconverter, an alternative modulation strategy was tested that set the MI of the phase experiencing a zero crossing in current to zero and compensating for this using the other two phases. The disadvantage of this modulation technique is that it requires up to a $\sqrt{3}$ times greater U_{DC} for a given u_{uvw}, depending on the phase shift between voltage and current, therefore reducing the utilization of the installed power in

the HF transformers.

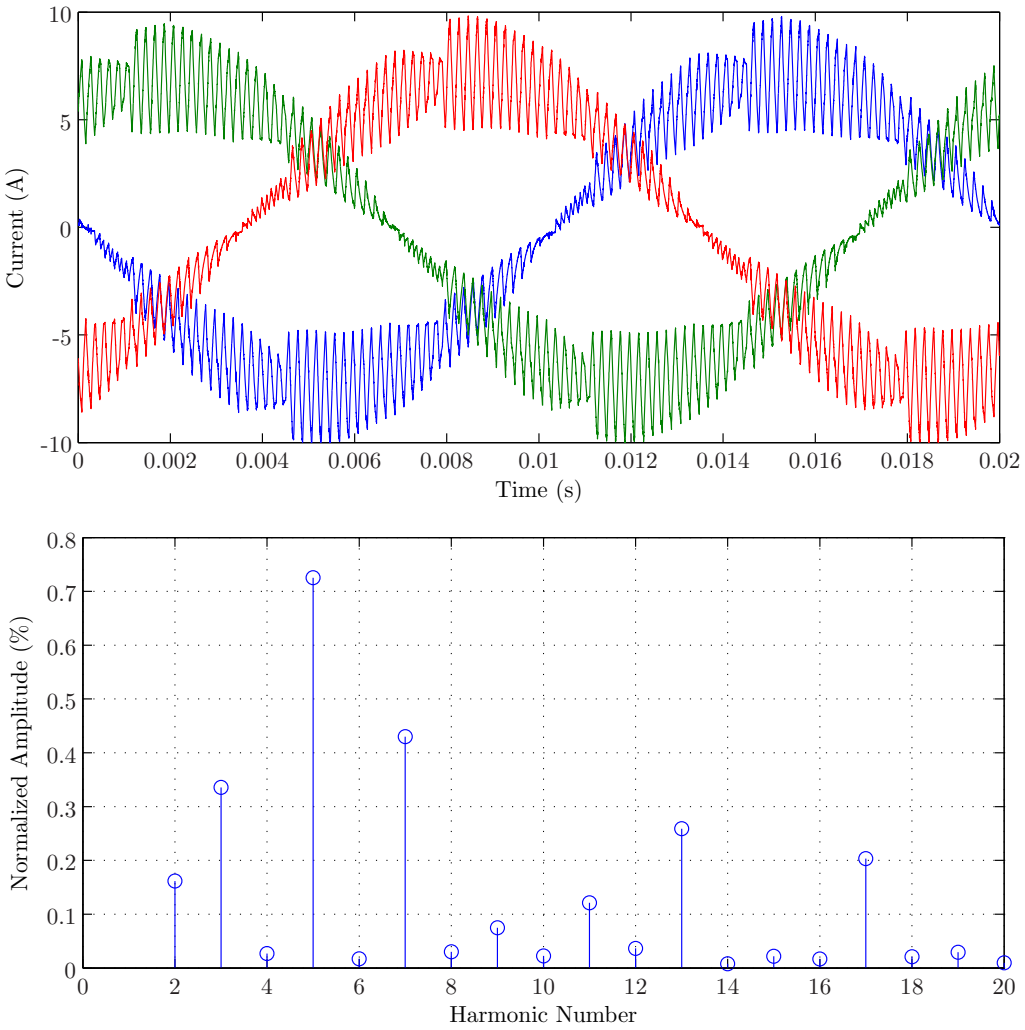


Figure 8.21: Cycloconverter AC currents and associated FFT, u_u (blue), u_v (green) and u_w (red), into 3-Phase resistive load, zero crossing compensation. i_{uvw} 5A RMS

Figure 8.21 shows the Cycloconverter current waveforms when transferring power to a 3-Phase resistive load bank when modulated to prevent the zero crossing glitch. The harmonic spectrum shows significantly reduced 7^{th}, 11^{th} 13^{th} 15^{th} and 19^{th} harmonics.

Figure 8.22 shows the Cycloconverter current waveforms using the modulation scheme to prevent the zero crossing glitch when transferring power from the DC network to the AC network. The FFT shows a 0.6% 11^{th}, a 1.5% 7^{th}, a 1% 5^{th}, a 0.6% 3^{rd} and a 1.5% 2^{nd} harmonic. The 3^{rd} harmonic is due to a unbalance in one

of the three phases, resulting in incomplete cancellation of the triplen harmonics. This could be due to a manufacturing differences in one of the HF transformers or a switching device or a connector exhibiting a higher resistance.

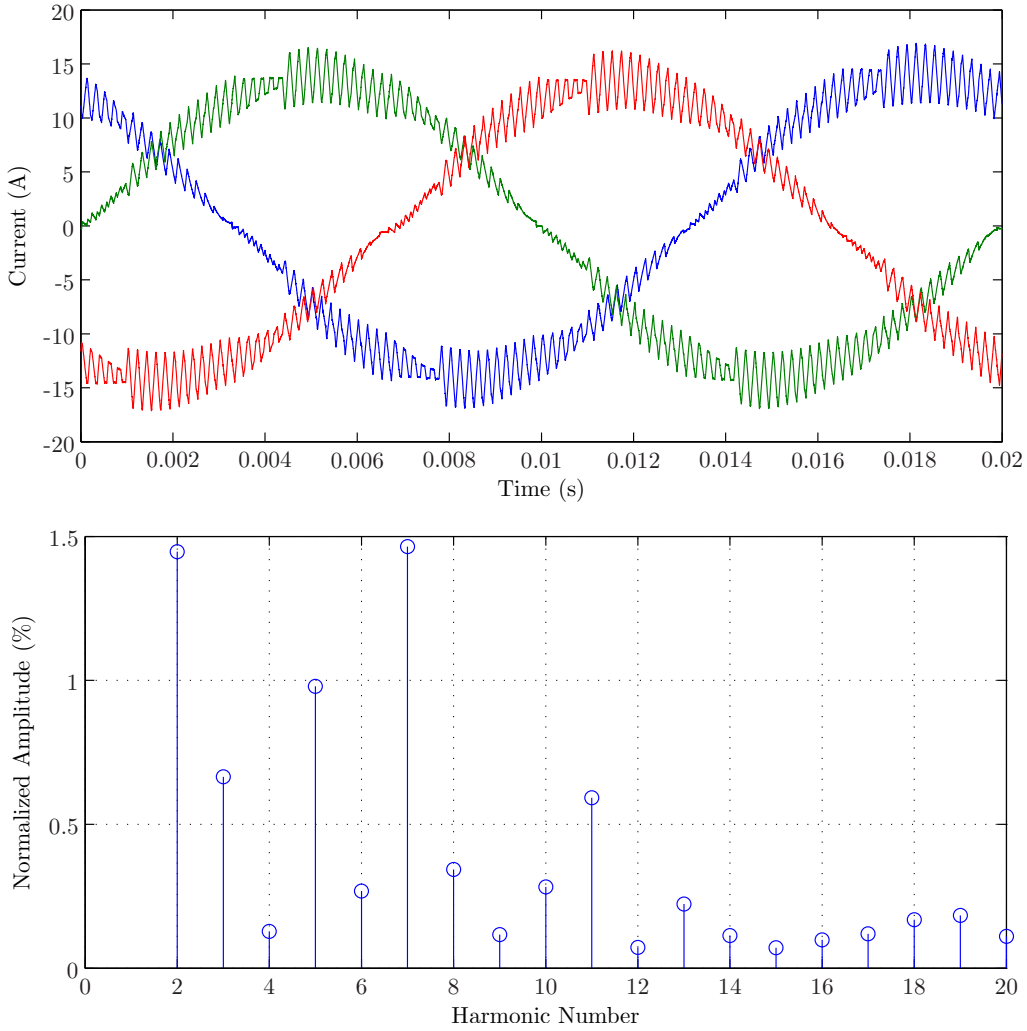


Figure 8.22: Cycloconverter AC currents and associated FFT, u_u (blue), u_v (green) and u_w (red), DC to AC i_{uvw} 10A RMS, zero crossing compensation

The 1.5% 2nd harmonic could be due to a sampling error in the DSP using this modulation technique. It was also discovered that the switch between zero crossing and the normal modulation strategy occurred at a different instant for the positive and negative half of each waveform. This could also result in even harmonics and could be due to a minimal offset in current measurement in the DSP. This could be corrected by using the diodes to measure current polarity instead of a hall effect current sensor [73].

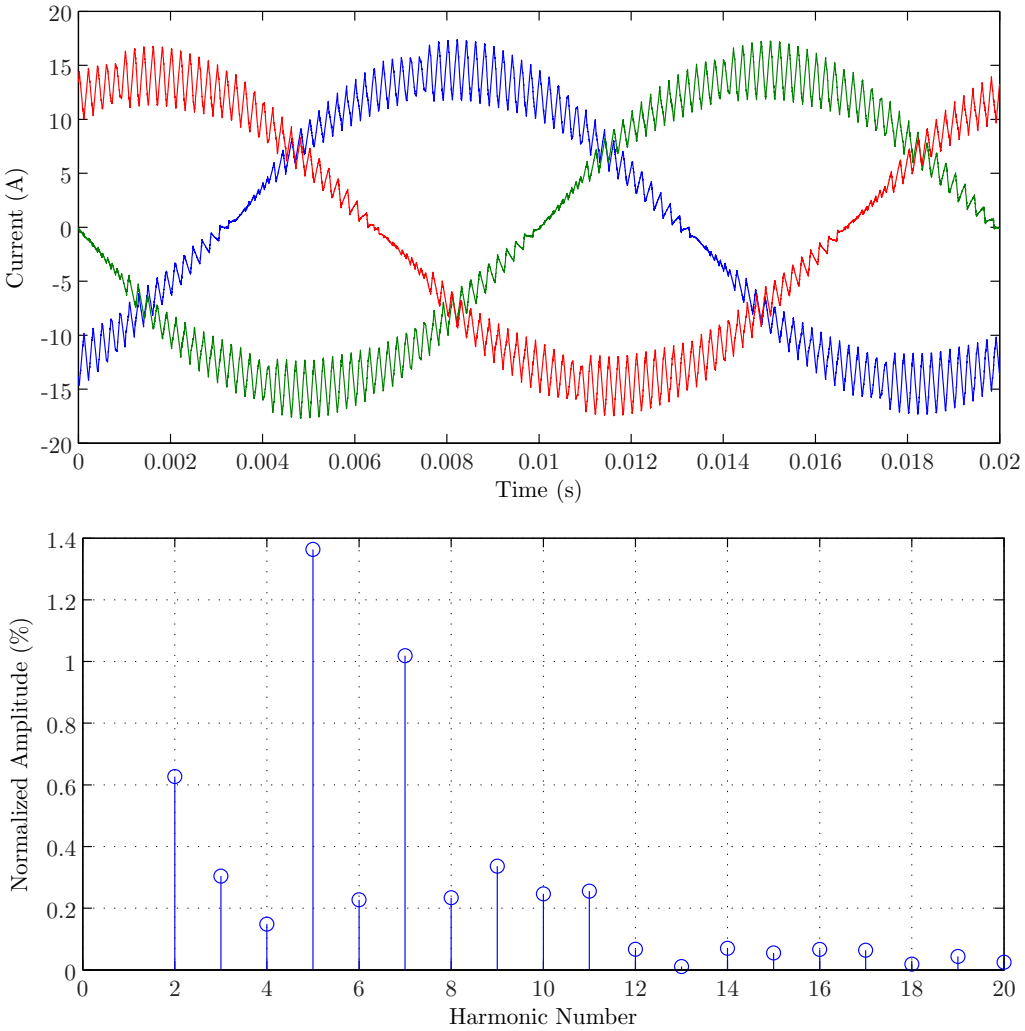


Figure 8.23: Cycloconverter AC currents and associated FFT, u_u (blue), u_v (green) and u_w (red), AC to DC i_{uvw} 10A RMS, zero crossing compensation

Figure 8.23 shows the Cycloconverter current waveforms using the modulation scheme to prevent the zero crossing glitch when transferring power from the AC network to the DC network. It can be seen in the FFT that the harmonics content is significantly reduced, compared with Figure 8.15, with a 1.4% 5^{th} and a 1% 7^{th}.

8.8 Conclusion

This chapter has presented the results obtained experimentally for the Cycloconverter and Hybrid Cycloconverter topologies. A number of objectives were set out for the laboratory prototype in Chapter 1 and the results have confirmed the validity of the experimental prototype. The causes of imperfections in the converter current waveforms have been explained with potential solutions given.

The losses in the Cycloconverter and Hybrid Cycloconverter topologies were tested in 4 different situations. The first test that was carried out with a passive 3-Phase resistive load bank. The second, third and fourth tests were carried out with using a bi-directional 3-Phase AC power supply. The second test tested the converters' losses in transferring power from the AC network to the DC network. The third test that was carried tested the converters' losses in transferring power from the DC network to the AC network. The fourth test tested the converters from 0^o to 360^o degrees phase shift between AC voltage and current.

The result from the losses test when connected to a resistive load showed The Cycloconverter Topology has lower losses over the full power range, with the maximum power from the Hybrid Cycloconverter over 0.7kW greater than that of the Cycloconverter. The 23% greater resistance of the load bank combined with the 23% u_{uvw} for a given U_{DC} from the Cycloconverter resulted in a higher power level for a given current and therefore a greater efficiency. When connected to a resistive load, both the 3-Phase AC converter currents and the 3-Phase AC converter voltages increase with AC power, whereas when connected to an AC voltage source, the AC voltage remains constant and only the 3-Phase AC currents increases. This results in increased losses at low power levels under this test.

The result from testing the power transfer from the AC network to the DC network showed that The Hybrid Cycloconverter Topology was up to 1% more efficient than The Cycloconverter Topology as well as having a 1.3kW greater maximum power level. The results from testing the power transfer from the DC network to the AC network showed that when processing more than 2.5kW, the efficiency of the Hybrid Cycloconverter Topology improved with power levels when compared against the Cycloconverter Topology. However for all waveform there was increased distortion on The Hybrid Cycloconverter Topology waveform

which will have resulted in increased the losses in the AC inductor. At medium power levels the power losses in both converters was greater when transferring power from the DC network to the AC network than from the AC network to the DC network. This was due to the additional switching required for Mode 3 operation.

The result from testing the power transfer from the DC network to the AC network showed that The Hybrid Cycloconverter Topology was up to 1% more efficient than The Cycloconverter Topology as well as having a 1.3kW greater maximum power level. The results from testing the power transfer from the DC network to the AC network showed that when processing more than 2.5kW, the efficiency of the Hybrid Cycloconverter Topology improved with power levels when compared against the Cycloconverter Topology. The losses in transferring power from the AC network to the DC network had a minimum value that was 0.3% lower than when transferring power from the DC network to the AC network. The losses at maximum power were however almost 0.2% greater. It is believed this is due to the lower MI required from the converters with power flow from the AC network to the DC network due the voltage drops across the HF transformer and switching devices subtracting from U_{DC} with power flow from DC to AC and adding to U_{DC} with power flow from the AC network to the DC network.

The result from testing a sweep of the phase shift between voltage and current showed that the Hybrid Cycloconverter has consistently lower losses when compared to the Cycloconverter, with up to 0.5% lower losses with a phase shift of 180°. There was a minimum value of losses at 90° for both converters due to the low duty cycle of the converters when the current was at a peak value. There were additional harmonics in the current waveform for both converters that resulted in a graph that wast not smooth, however it showed a similar trend to the simulations carried out in Chapter 4.

The implementation of a modulation scheme to prevent the zero crossing distortion in the Cycloconverter resulted in a significant reduction to the harmonic distortion in the AC current waveforms, i_{uvw}, however this modulation scheme required a U_{DC} $\sqrt{3}$ times greater for a give u_{uvw} and therefore reduced the utilization of the installed power in the HF transformer and switching devices.

Chapter 9

Conclusion

This thesis has proposed and researched a novel Hybrid Cycloconverter Topology, designed for interfacing a DC network to an AC network, whilst providing isolation between the two networks. The DC network is designed to be connected to an energy storage device and the AC network represents a Medium Voltage grid. The topology was developed to reduce the cost per kW of installed power in the power converter, increasing the competitiveness of energy storage devices based on batteries or super-capacitors.

Traditional solutions for bi-directional DC–AC power converters, required to perform this role, use Low Voltage power converters connected to a step up transformer. This is appropriate for low powered applications, for example in a UPS. For high powered applications, such as HVDC, Medium Voltage switching devices, IGCTs or Thyristors, are directly connected to the Medium Voltage grid. Both of these converter topologies require large magnetic components, either through transformers or AC filters, increasing the cost and therefore reducing the suitability of either of these converter topologies for many lower cost, medium power applications.

Research into suitable alternative converter topologies for medium power applications have focused on Cascaded Multicell Converters. These converters significantly reduce the requirements of the magnetic materials with the use of HF transformers and high frequency switching of the power converters. However this

family of converter topologies require a large number of electrolytic capacitors, increasing cost and reducing reliability. Multilevel converters based on Cycloconverter topologies reduce the required number of electrolytic capacitors. However the HF transformer can be up to twice the size.

Hybrid converter topologies can combine a number of modules formed of differing converter topologies to form a converter that can offer significant benefits when compared to the individual converter topology modules. This research has focused on the incorporation of an auxiliary 3-Phase VSI converter with 3 single phase Cycloconverters, in order to increase the power rating of the converter, whilst keeping the transformer and switching devices in the main Cycloconverters constant.

9.1 Summary of Achievements

Existing converter topologies were evaluated in order to establish the state of the art for bi-directional modular Medium Voltage DC–AC power converters utilizing a high frequency transformer to provide isolation. This evaluation resulted in the proposal and justification of a novel Hybrid Cycloconverter Topology to fulfil the requirements of this project.

An initial investigation into the operation, control and modulation techniques for the Hybrid Cycloconverter and Cycloconverter Topologies was carried out along with for the Triple VSI converter topology that was used as a benchmark. A modulation strategy for the Cycloconverter and Hybrid Cycloconverter Topologies was proposed to minimize peak flux density whilst preventing a build up of a DC component in flux. This is essential to maximize the power density of the demonstrating converter whist minimizing the chance of saturation in the transformer core.

The Hybrid Converter Topology was then simulated, along side the Cycloconverter and benchmark Triple VSI Topology, in order to comparatively evaluate the losses in the 3 converters. This simulation was carried out at low, medium and high power levels, and for each power level the converters were simulated

across a range of phase shifts between the AC network voltage and current.

To optimize the converter topologies, a second simulation was carried out with reverse blocking IGBTs in the Hybrid Cycloconverter Topology and 25A IGBTs, instead of 35A IGBTs, in the Triple VSI Topology. Reverse blocking IGBTs are arranged with each pair of switching devices connected in parallel, as opposed to the series connection of standard IGBTs, resulting in significantly reduced conduction losses in the Cycloconverter stage. However it was established from further simulation that the large reverse recovery charge of the reverse blocking IGBTs resulted in significant overshoot in the transformer current causing resonance with the parasitic capacitance across the switching devices of the Single Phase VSI. This made the use of Reverse Blocking IGBTs unsuitable for the demonstrator converter.

A further simulation was carried out with the Hybrid Cycloconverter, along side the Cycloconverter and benchmark Triple VSI Topology, at an alternative switching frequency. From the results the losses in the three converter topologies were extrapolated from 0–2kHz so as to demonstrate the suitability of the Hybrid Cycloconverter Topology for High Frequency (HF) operation.

An experimental prototype was designed and constructed that could be arranged as both a Cycloconverter and a Hybrid Cycloconverter Topology. This was to validate the increase in AC network voltage, and therefore power, that the Hybrid Cycloconverter offers against the Cycloconverter Topology using the same HF transformer and switching devices.

The selection of the core materials and conductor profile for the HF transformer was documented and the final transformer design was presented. A simulation of the transformer core was performed to justify the transformer design and the selection of the modulation strategy for the Cycloconverter and Hybrid Cycloconverter Topologies. This simulation presented the peak flux density, magnetizing current and core losses for the proposed modulation strategy along side three alternatives. Each modulation technique was also evaluated for a DC flux component that could result in core saturation.

The control scheme and modulation strategy was designed and implemented on

a DSP and an FPGA. The control scheme incorporated the control of the AC converter currents, the charging and maintenance of the DC link in the auxiliary 3-Phase VSI, and the demand voltage distribution between the Main Converter and the auxiliary 3-Phase VSI. The modulation strategy was implemented in logic on the FPGA and incorporated three modes of operation, depending on the polarity of the AC voltage and current.

Experimental performance of the novel Hybrid Cycloconverter Topology is evaluated against the Cycloconverter Topology for an increase in AC power, losses and current harmonics for bi-directional power flow. This converter was tested at 15A RMS for both the Cycloconverter and the Hybrid Cycloconverter topologies. An increase of 23% in converter voltage, and therefore power, from the Hybrid Converter topology, validates the research and development that has been carried out in this project.

9.2 Summary of the Originality in the Thesis

The original aspects of this thesis are:

- The design, simulation, construction and experimental verification of a novel converter topology, the Hybrid Cycloconverter Topology.
- Development of technique to divide converter voltage demand between the Main Converter and the auxiliary 3-Phase VSI for the Hybrid Cycloconverter Topology , published in [74].
- The implementation of a modulation technique for Cycloconverter based topologies that minimizes peak flux, the DC flux component, and allows for soft switching in the Cycloconverter stage.

9.3 Further Work

The experimental converter achieved the aims of this project. However a number of improvements that were not implemented due to time constraints could improve

the converter performance in terms of efficiency and AC current waveform quality.

The experimental converter current waveforms, for both the Cycloconverter and the Hybrid Cycloconverter topologies, show significant zero crossing distortion. An alternative modulation strategy was tested for the Cycloconverter that compensated for this zero crossing distortion, however it requires up to a $\sqrt{3}$ times greater U_{DC} for a give u_{uvw}, dependant on the phase shift between voltage and current.

To compensate for a distorted AC network voltage, resonant harmonic controllers could be used. These improvements in current waveform quality would also improve the converter efficiency, particularly for the Hybrid Cycloconverter, by reducing the losses from the current harmonics in the AC network inductive filter.

To aid in the development of this converter topology, a breakdown of losses could be performed on the demonstrator converter using a combination of further testing of the Hybrid Converter Topology and HF transformer, together with the simulation of the transformer losses with the converter losses based on accurate device models. This would highlight the weakest components in the system, allowing for optimization to reduce losses and increase performance.

Further advances could involve the replacement of the IGBTs in the auxiliary 3-Phase VSI with MOSFETs, reducing switching and conduction losses, whilst an increase in the clamp circuit voltage rating would allow for the testing at a greater AC network voltage. Operation at a higher voltage will significantly improve the efficiency of the experimental converter topologies as the majority of losses in the Hybrid Cycloconverter Topology are conduction losses not switching losses.

To reduce the requirements of the AC inductive filter, an investigation could be carried out into minimizing the switching harmonics in the Hybrid Converter Topology by controlling the precise switching instants of the auxiliary 3-Phase VSI and shaping the resulting converter AC voltage waveform.

No attempt was made to reduce the switching losses in the Single Phase VSI stage of the Main Converter in the Hybrid Converter Topology. A capacitive

snubber could potentially reduce the turn off losses in this stage of the converter. However further research would need to be carried out to establish the most effective snubber arrangement and the effect the snubber would have on each switching transition.

Finally a further simulation based study into modulation techniques could be carried out using an evolutionary algorithm to establish the optimum voltage distribution between the Main Converter and the auxiliary 3-Phase VSI in the Hybrid Converter Topology in terms of installed power in the auxiliary converter against the increase in total converter power.

To progress the development of this converter topology, a new demonstrator converter could be developed for operation with connection to a Medium Voltage AC network. This converter would be constructed from multiple Main Converter modules and a single low powered auxiliary 3-Phase VSI. To increase the voltage rating of this converter, Thyristors could be used instead of IGBTs as the main switching devices in the Cycloconverter stage. Using this approach the voltage rating of a potential converter based on the Hybrid Cycloconverter Topology could be increased to the tens of kilovolts range.

Improvements in switching device technology, particularly Silicon Carbide (SiC) MOSFETs could allow for much higher switching frequencies, due to the reduced switching losses. Using SiC diodes would also result in zero reverse recovery, reducing the comutation time of the Main Converter and preventing an overshoot in current in the leakage inductance of the HF transformer. Before this can occur for this application the financial competitiveness of this new technology first needs to be evaluated.

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Glossary

C_{iss} . . . . . Transistor input capacitance

C_j . . . . . IGBT junction capacitance

C_{oss} . . . . . Transistor output capacitance

C_{rss} . . . . . Transistor reverse transfer capacitance

E_{off} . . . . . Transistor turn-off energy losses

E_{on} . . . . . Transistor turn-on energy losses

E_{rr} . . . . . Diode reverse recovery energy

f_{sw} . . . . . Switching frequency

$Gc(s)$ . . . . . Controller open loop transfer function

$Gp(s)$ . . . . . Plant open loop transfer function

i_α . . . . . α axis AC current

i_β . . . . . β axis AC current

I_c . . . . . Collector current

i_d . . . . . d axis AC current

i_d^* . . . . . d axis AC current demand

I_{DC} . . . . . DC link current

I_{drain} . . . . . Transistor drain current

I_f . . . . . Forward current

i_{pri} . . . . . Transformer primary current

i_q . . . . . q axis AC current

i_q^* . . . . . q axis AC current demand

I_{RP} . . . . . Repetitive peak current

I_{rr} . . . . . Diode peak reverse recovery current

i_{sec} . . . . . Transformer secondary current

i_u . . . . . u phase AC current

i_v . . . . . v phase AC current

i_w . . . . . w phase AC current

i_{uvw} . . . . . 3-Phase AC current

L_{leak} . . . . . Transformer leakage inductance

P_{cond} . . . . . Conduction losses

P_{off} . . . . . Turn off power loss

P_{on} . . . . . Turn on power loss

Q_g . . . . . Transistor total gate charge

Q_{gd} . . . . . Transistor gate-to-drain charge

Q_{gs} . . . . . Transistor gate-to-source charge

Q_{rr} . . . . . Diode reverse recovery charge

$R_{DS(on)}$ . . . . . Transistor on state resistance

T . . . . . 50Hz time period

$\hat{\theta}$ . . . . . Estimated 3-Phase AC voltage angle

θ_{nom} . . . . . Nominal AC voltage angle

θ_3^* . . . . . 3$^{\text{rd}}$ harmonic voltage angle

t_{rr} . . . . . Diode reverse recovery time

u_{A0} . . . . . u phase AC voltage to neutral before line inductor

u_α . . . . . α axis AC voltage

u_{B0} . . . . . v phase AC voltage to neutral before line inductor

u_β . . . . . β axis AC voltage

u_{C0} . . . . . w phase AC voltage to neutral before line inductor

u_d . . . . . d axis AC voltage

U_{DC} . . . . . DC link Voltage

$u_{main}{}^*$ . . . . . Main Converter demand AC voltage

u_{pri} . . . . . Transformer primary Voltage

u_q . . . . . q axis AC voltage

u_{sec} . . . . . Transformer secondary Voltage

u_{3rd} . . . . . 3^{rd} harmonic AC voltage

$u_{3\Phi VSI}{}^*$ . . . . . 3-Phase demand voltage for 3-Phase VSI

$U_{3\Phi VSI}$ . . . . . 3-Phase VSI DC link voltage

$U_{3\Phi VSI}{}^*$ . . . . . 3-Phase VSI DC link demand voltage

$u_{3\Phi VSIDC}{}^*$ . . . . AC voltage demand from 3-Phase VSI DC link controller

$u_{triplen}{}^*$ . . . . . Triplen harmonics demand voltage

u_u . . . . . u phase AC voltage

$u_u{}^*$ . . . . . u phase AC voltage demand

$u_{umain}{}^*$ . . . . . u phase demand voltage for Main Converter

$u_{u3\Phi VSI}{}^{*}$ . . . . . u phase demand voltage for 3-Phase VSI

u_{uvw} . . . . . 3-Phase AC voltages

$u_{uvw}{}^{*}$ . . . . . 3-Phase voltage demand

u_{v} . . . . . v phase AC voltage

$u_{v}{}^{*}$ . . . . . v phase AC voltage demand

$u_{vmain}{}^{*}$ . . . . . v phase demand voltage for Main Converter

U_{VSI} . . . . . 3-phase VSI DC link Voltage

$u_{v3\Phi VSI}{}^{*}$ . . . . . v phase demand voltage for 3-Phase VSI

u_{w} . . . . . w phase AC voltage

$u_{w}{}^{*}$ . . . . . w phase AC voltage demand

$u_{umain}{}^{*}$ . . . . . w phase demand voltage for Main Converter

$u_{w3\Phi VSI}{}^{*}$ . . . . . w phase demand voltage for 3-Phase VSI

V_{ce} . . . . . Transistor collector-emitter Voltage

V_{ce_sat} . . . . . Transistor saturation Voltage

V_{f} . . . . . Diode forward Voltage drop

V_{DS} . . . . . Transistor drain-source Voltage

V_{GS} . . . . . Transistor gate-source Voltage

Acronyms

A2D . . . . . Analogue to Digital

DAB . . . . . Dual Active Bridge

DSM . . . . . Demand Side Management

DSP . . . . . Digital Signal Processor

EMI . . . . . External Memory Interface

ESR . . . . . Equivalent Series Resistance

FFT . . . . . Fast Fourier transform

FPGA . . . . . Field-Programmable Gate Array

HEPWM . . . . . Harmonic Elimination PWM

HF . . . . . High Frequency

HVDC . . . . . High Voltage Direct Current

IC . . . . . Integrated Circuit

IGBT . . . . . Insulated Gate Bipolar Transistor

IGCT . . . . . Integrated Gate Commutated Thyristor

ISR . . . . . Interrupt Service Routine

LED . . . . . Light Emitting Diode

LF . . . . . Low Frequency

LV . . . . . Low Voltage

M^2LC . . . . . Modular MultiLevel Converter

MF . . . . . Medium Frequency

MI . . . . . Modulation Index

MOSFET . . . . Metal Oxide Semiconductor Field Effect Transistor

MV . . . . . Medium Voltage

NPC . . . . . Neutral Point Clamp

PCB . . . . . Printed Circuit Board

PEMC . . . . . Power Electronics and Machine Control

PI . . . . . Proportional Integral

PLL . . . . . Phase Lock Loop

PV . . . . . Photovoltaic

PWM . . . . . Pulse Width Modulation

RB IGBT . . . . Reverse Blocking IGBT

RMS . . . . . Root Mean Square

SIC . . . . . Silicon Carbide

SPWM . . . . . Sinusoidal PWM

SVPWM . . . . . Space Vector PWM

THD . . . . . Total Harmonic Distortion

UPS . . . . . Uninterruptible Power Supply

VSI . . . . . Voltage Source Inverter

VTA . . . . . Voltage Time Area

ZCS . . . . . Zero Current Switching

ZVS . . . . . Zero Voltage Switching

List of Figures

Appendix A

Device and Circuit parameters

A.1 PSim schematics

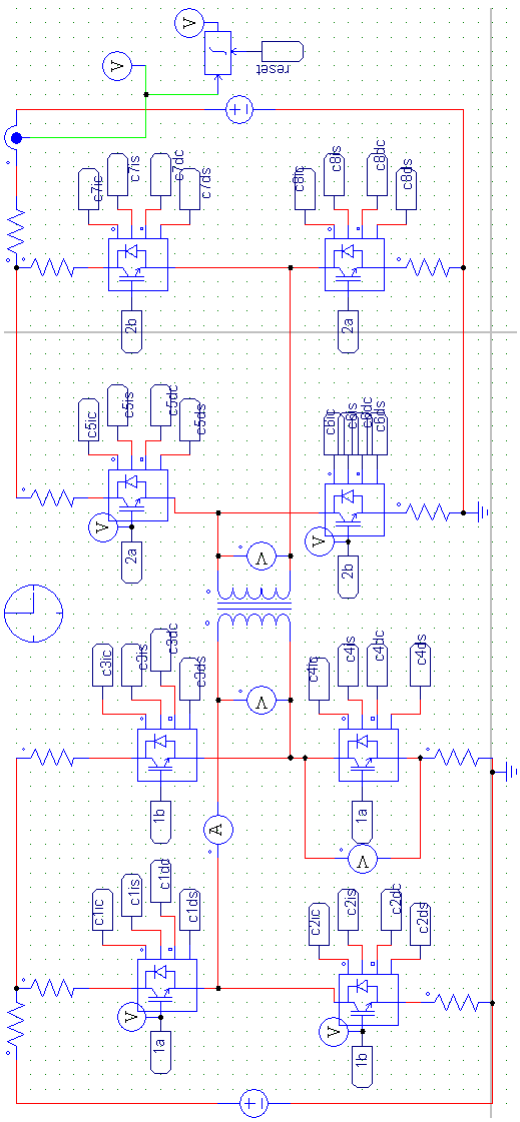


Figure A.1: Schematic of VSI 1 + 2 (DC/DC converter) in the Triple VSI Topology

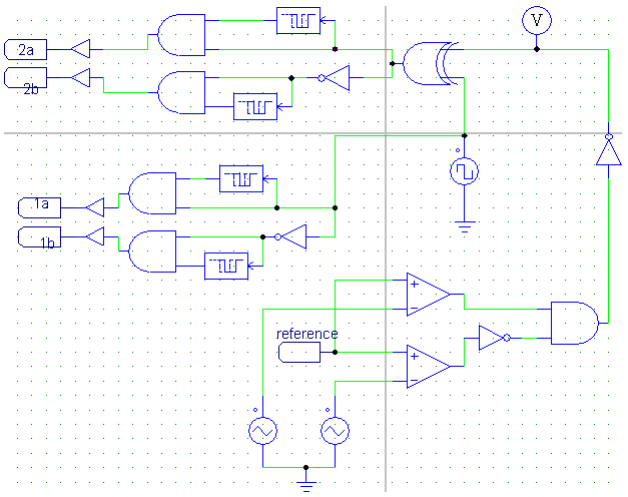


Figure A.2: Switching strategy of VSI 1 + 2 (DC/DC converter) in the Triple VSI Topology

Figure A.3: Schematic of VSI 3 in the Triple VSI Topology

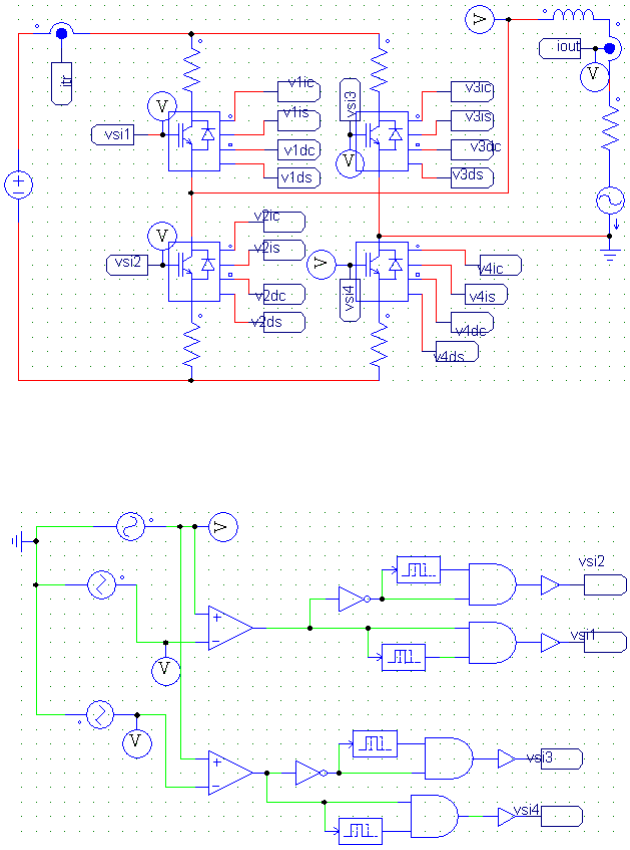


Figure A.4: Switching strategy of VSI 3 in the Triple VSI Topology

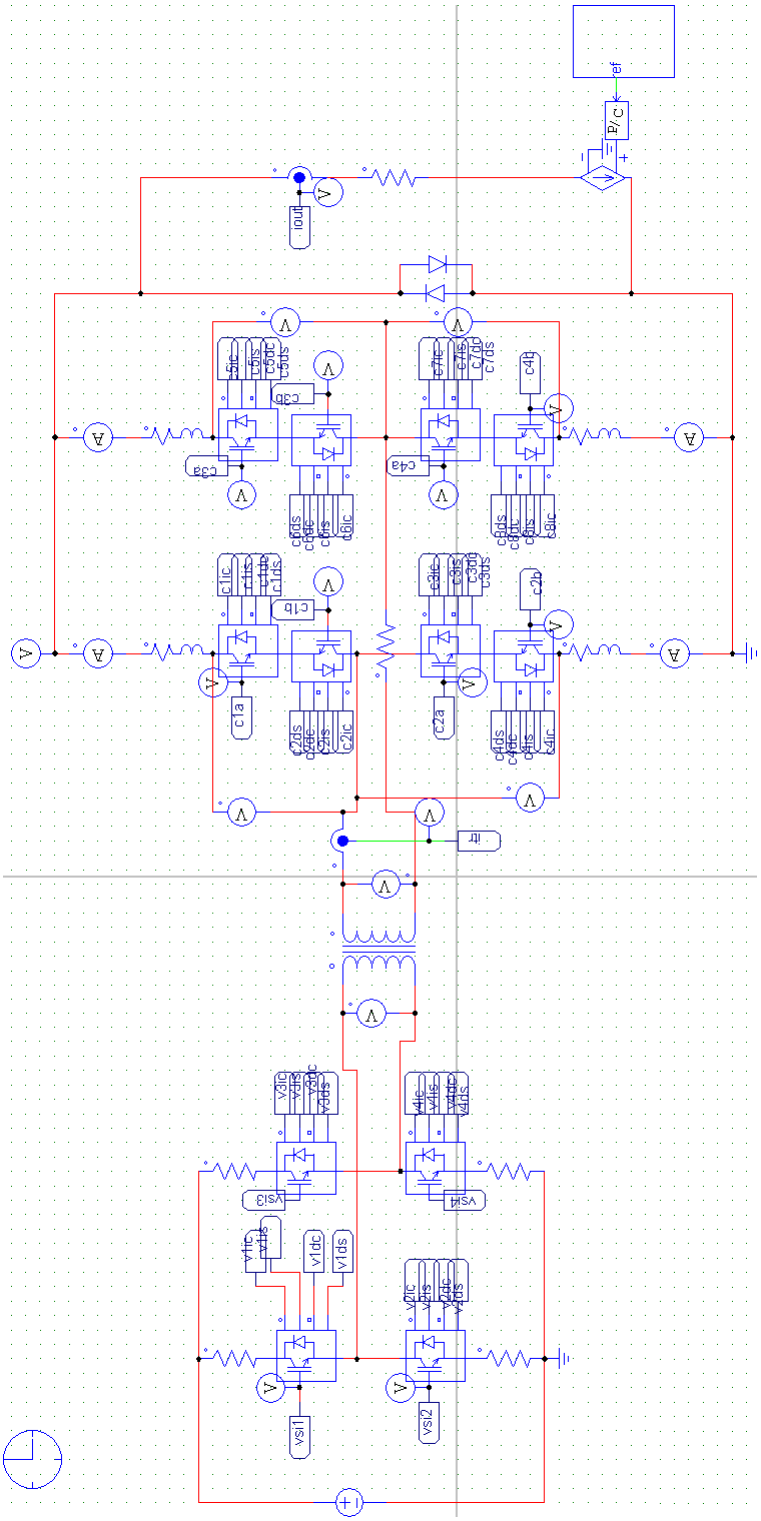


Figure A.5: Main Converter from Cycloconverter and Hybrid Cycloconverter Topology schematic

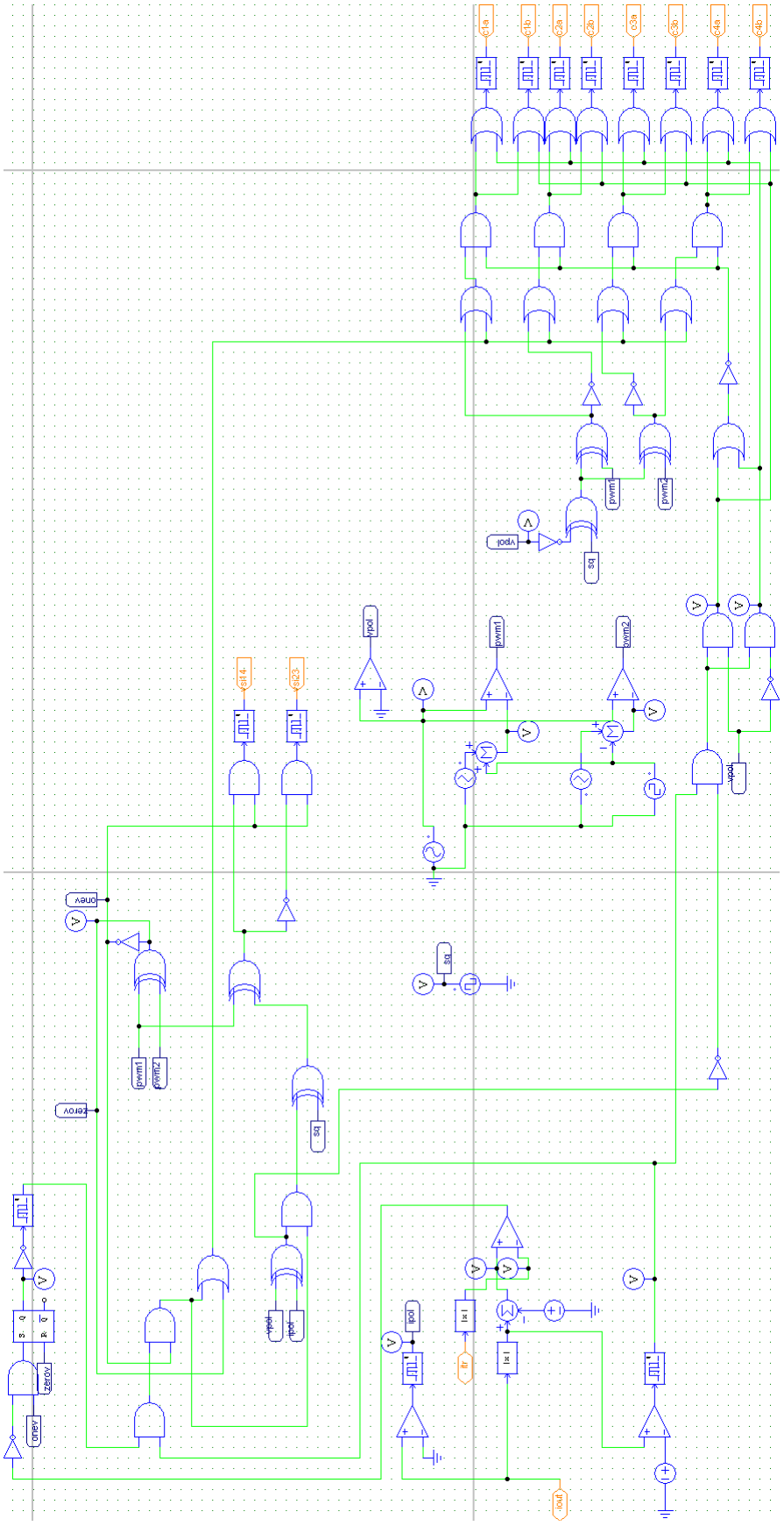


Figure A.6: Cycloconverter Topology switching strategy

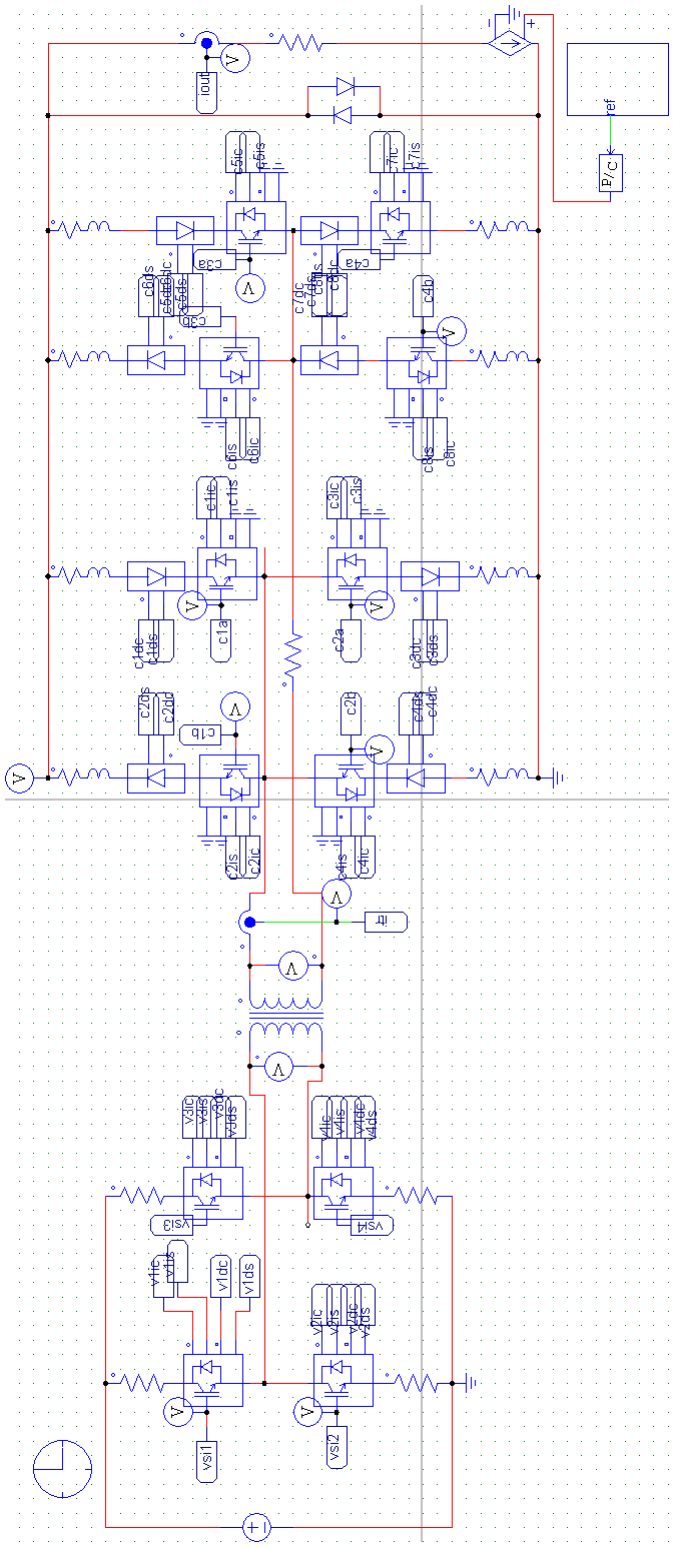


Figure A.7: Hybrid Cycloconverter Topology reverse blocking IGBT schematic

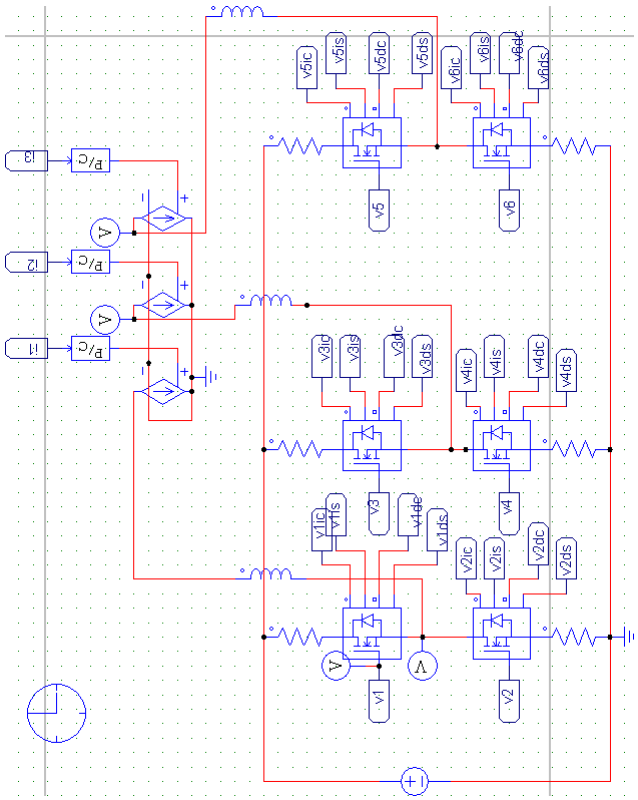


Figure A.8: Schematic of the auxiliary 3-phase VSI for the Hybrid Cycloconverter Topology

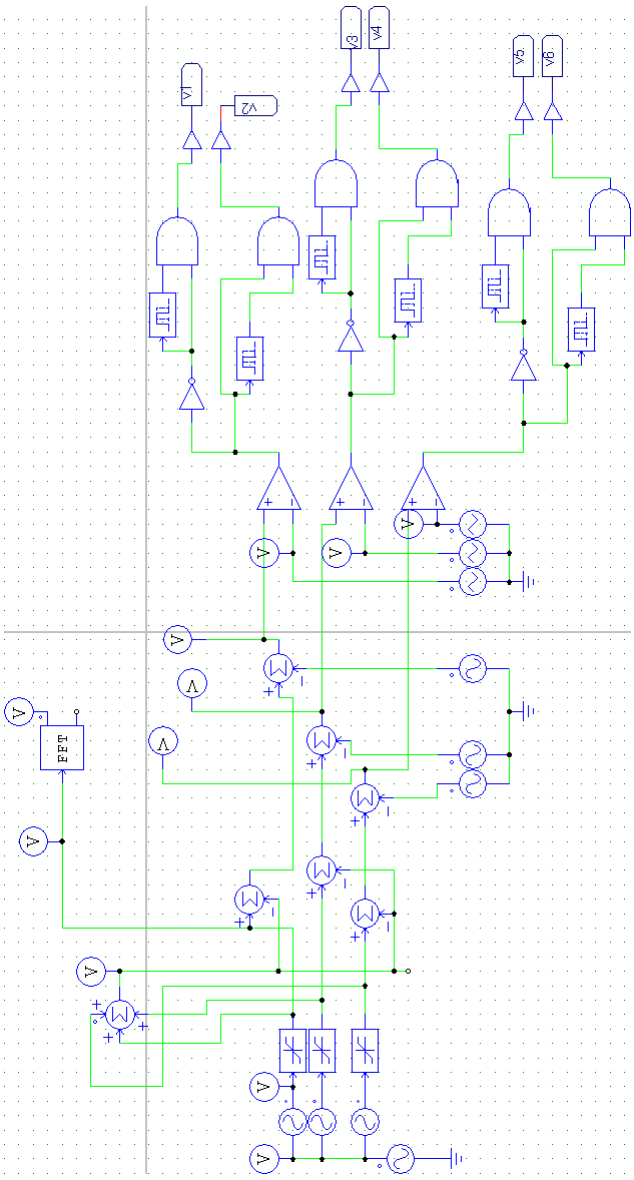
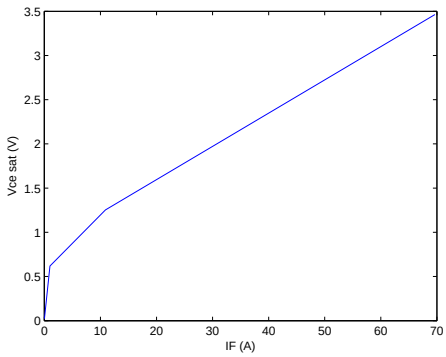


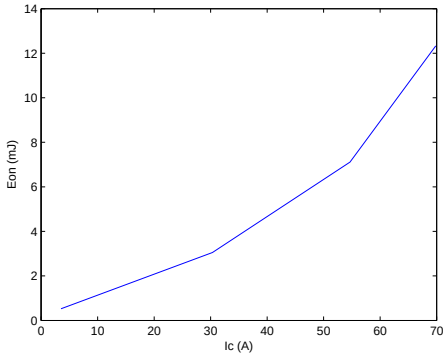
Figure A.9: Switching strategy of the auxiliary 3-phase VSI in the Hybrid Cycloconverter Topology

A.2 Device parameters

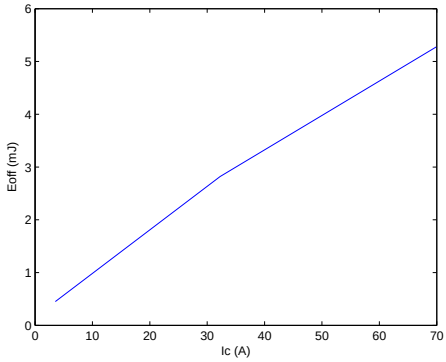
A.2.1 FS35R12W1T4 IGBT module



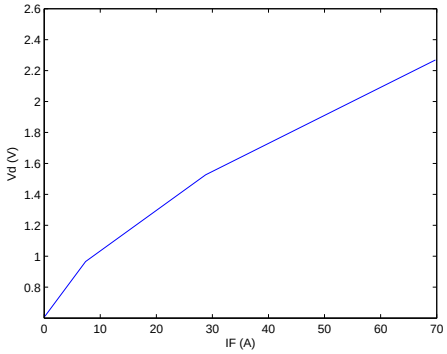
(a) V_{ce_sat} vs. I_c



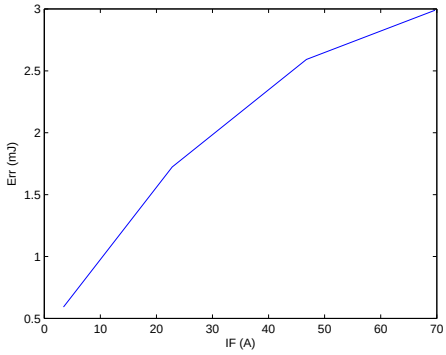
(b) E_{on} vs. I_c



(c) E_{off} vs. I_c



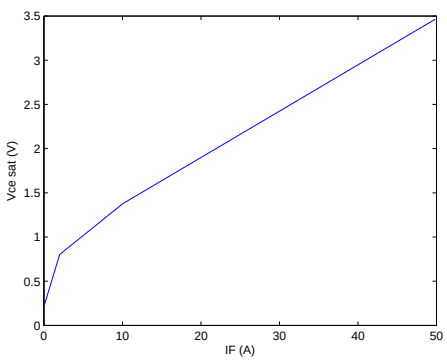
(d) V_f vs. I_f



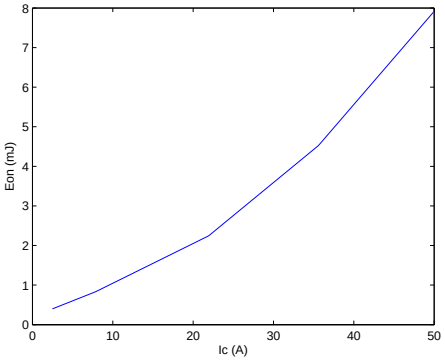
(e) E_{rr} vs. I_f

Figure A.10: Characteristics of the FS35R12W1T4 35A, 1200V IGBT @ 125^0C

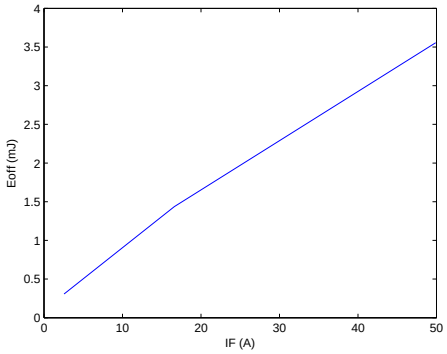
A.2.2 FS25R12W1T4 IGBT module



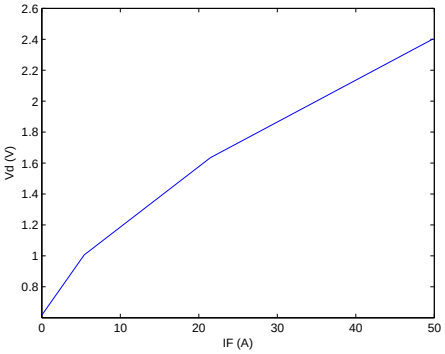
(a) V_{ce_sat} vs. I_c



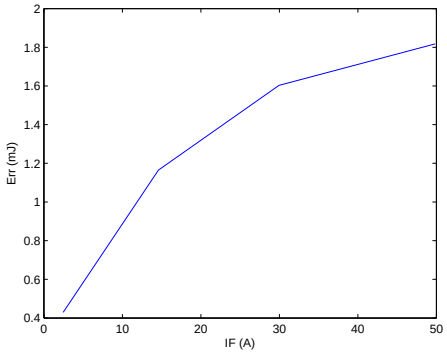
(b) E_{on} vs. I_c



(c) E_{off} vs. I_c



(d) V_f vs. I_f



(e) E_{rr} vs. I_f

Figure A.11: Characteristics of the FS25R12W1T4 25A, 1200V IGBT @ 125^0C

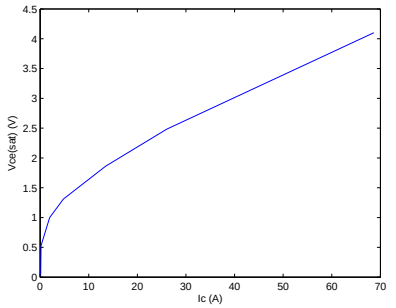
A.2.3 IRF4228PbF MOSFET

The information from the component datasheet that was used for the model is shown in table A.1.

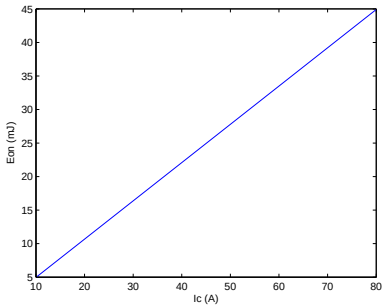
Device parameter	Value
$R_{DS(on)}$	0.012Ω
$V_{GS}(th)$	4V
Q_g	71nC
Q_{gs}	18nC
Q_{gd}	21nC
C_{iss}	4530pF
C_{oss}	550pF
C_{rss}	100pF
V_f	0.7V
t_{rr}	76ns
Q_{rr}	0.23µC

Table A.1: Characteristics of the IRF4228PbF 150A, 150V MOSFET @ 125^0C

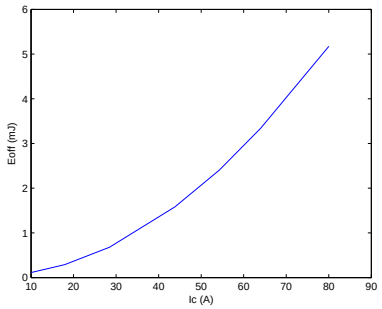
A.2.4 IXRH 40N120 reverse blocking IGBT module



(a) V_{ce_sat} vs. I_c



(b) E_{on} vs. I_c



(c) E_{off} vs. I_c

Figure A.12: Characteristics of the IXRH 40N120 40A, 1200V reverse blocking IGBT @ 125^0C

The reverse recovery charge, Q_{rr}, was simulated as 35µC at 600V and when the reverse blocking diode junction capacitance, C_j, was included in the simulation, the value was 90nF.

A.3 Transformer Parameters

	Value
A_L	$5.13\mu H/T^2$
R	1Ω
ϕ_{sat}	$462\mu Wb$
K_1	0.73
K_{exp1}	7
K_2	0.72
K_{exp2}	48

Table A.2: PSIM Transformer core parameters

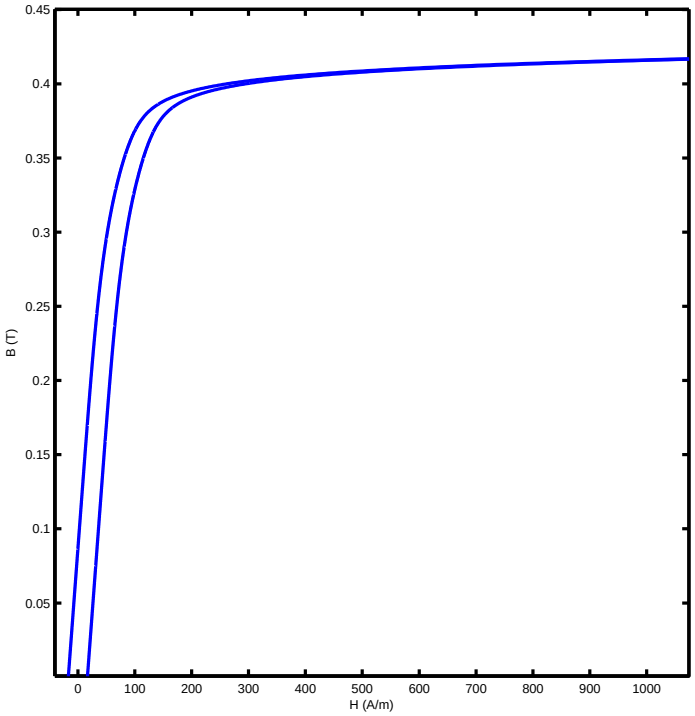


Figure A.13: BH curve of PSIM transformer model

Appendix B

Schematic Diagrams

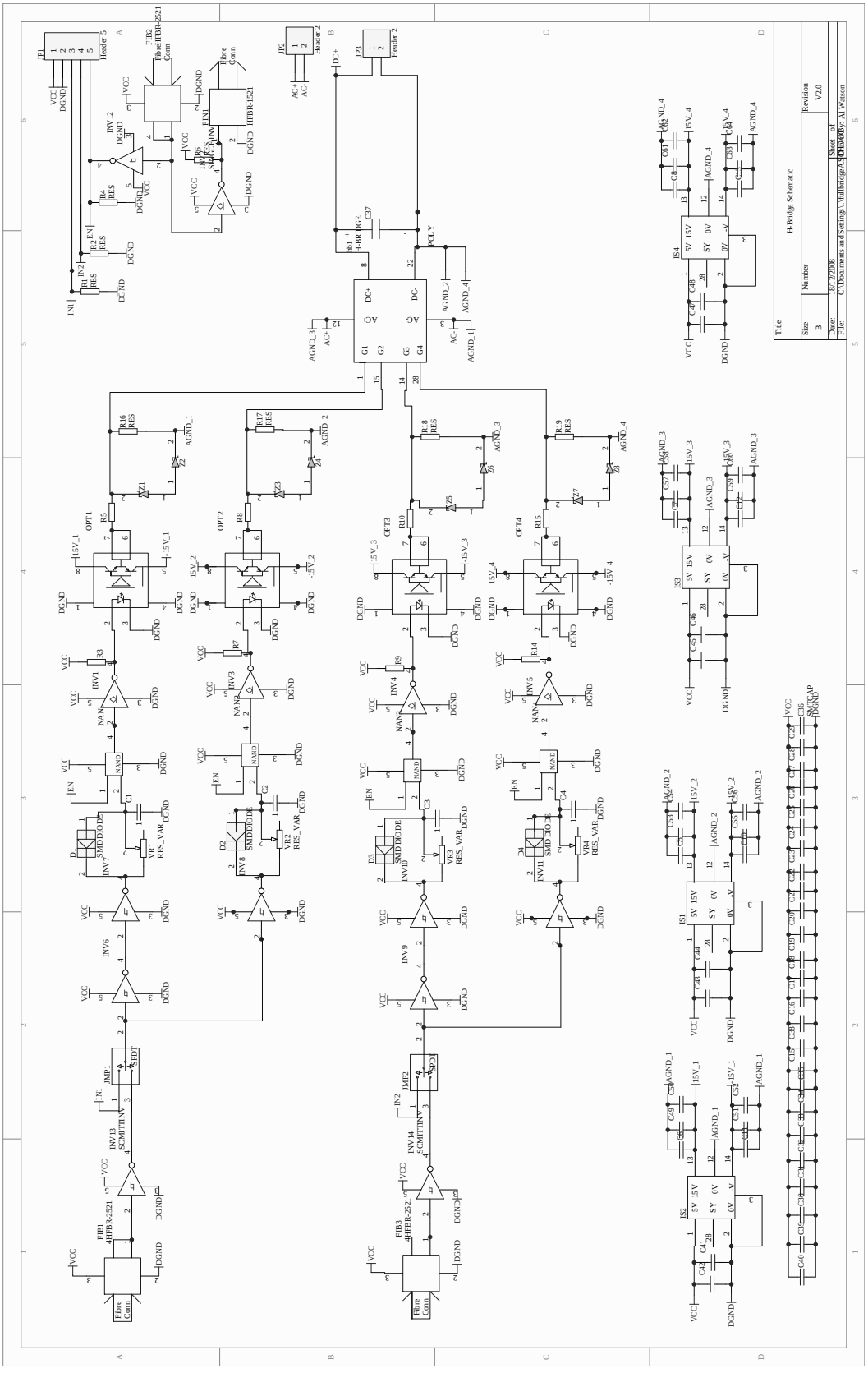


Figure B.1: Single Phase VSI Schematic

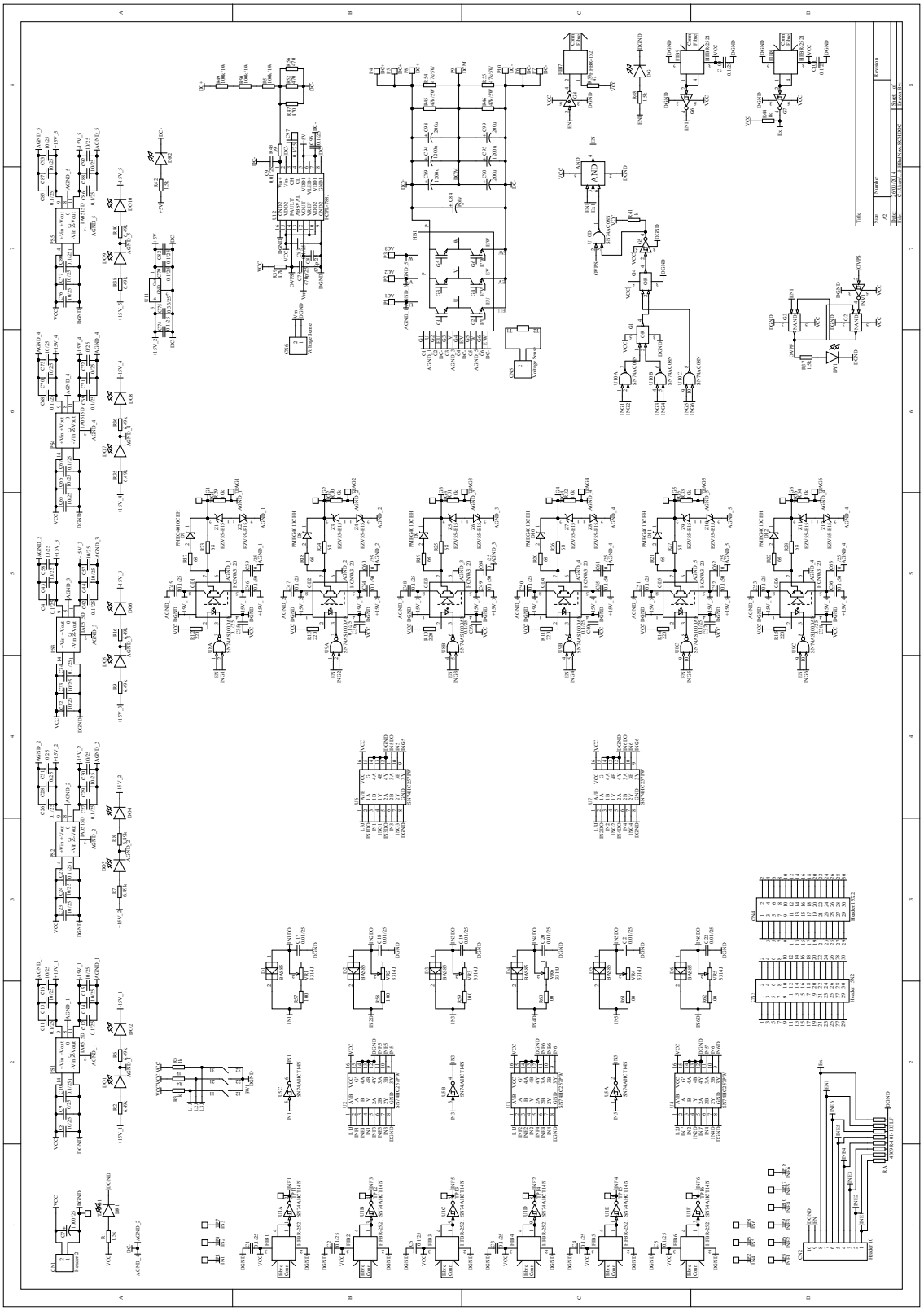


Figure B.2: 3 Phase VSI Schematic

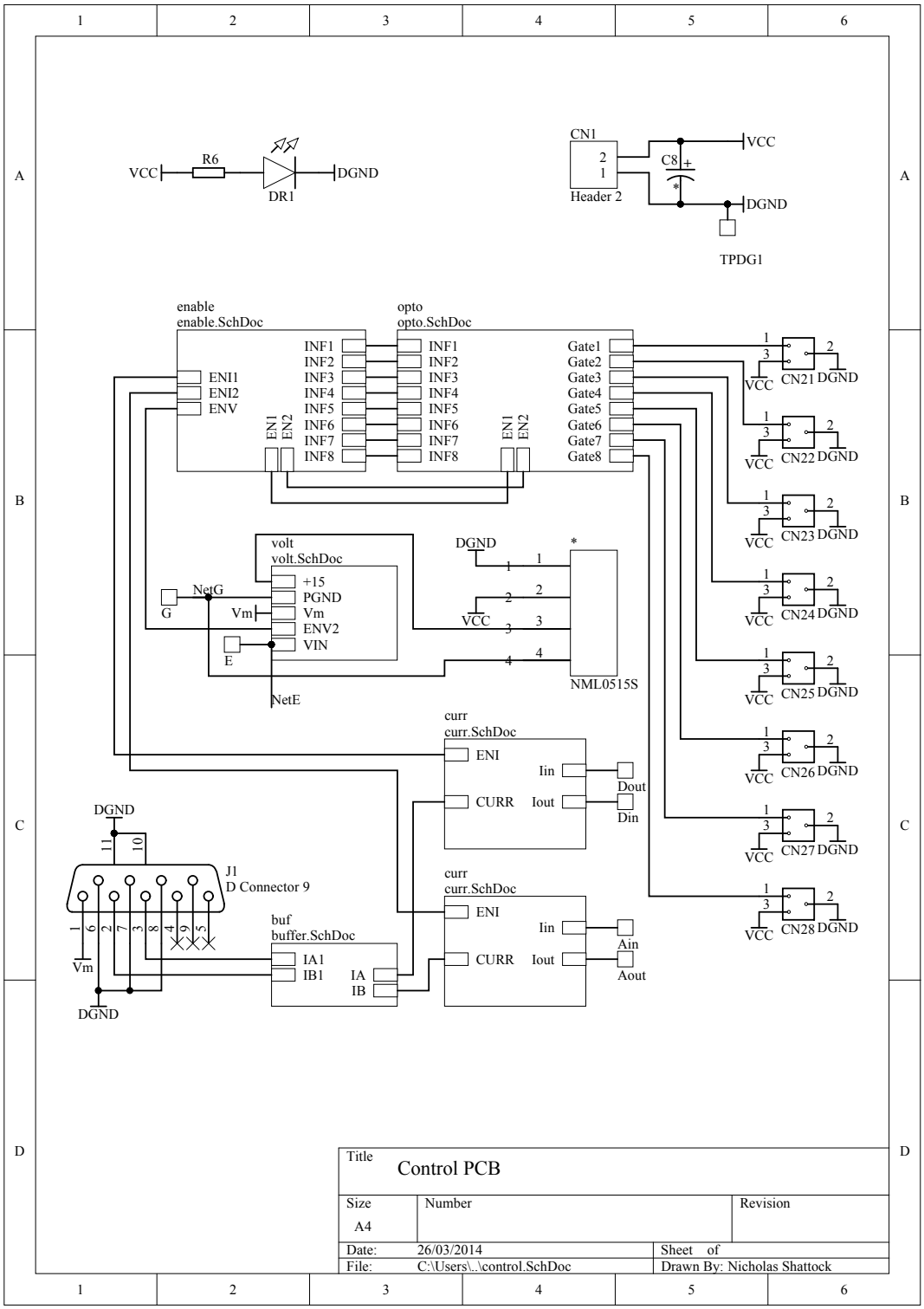


Figure B.3: Cycloconverter Control PCB Schematic

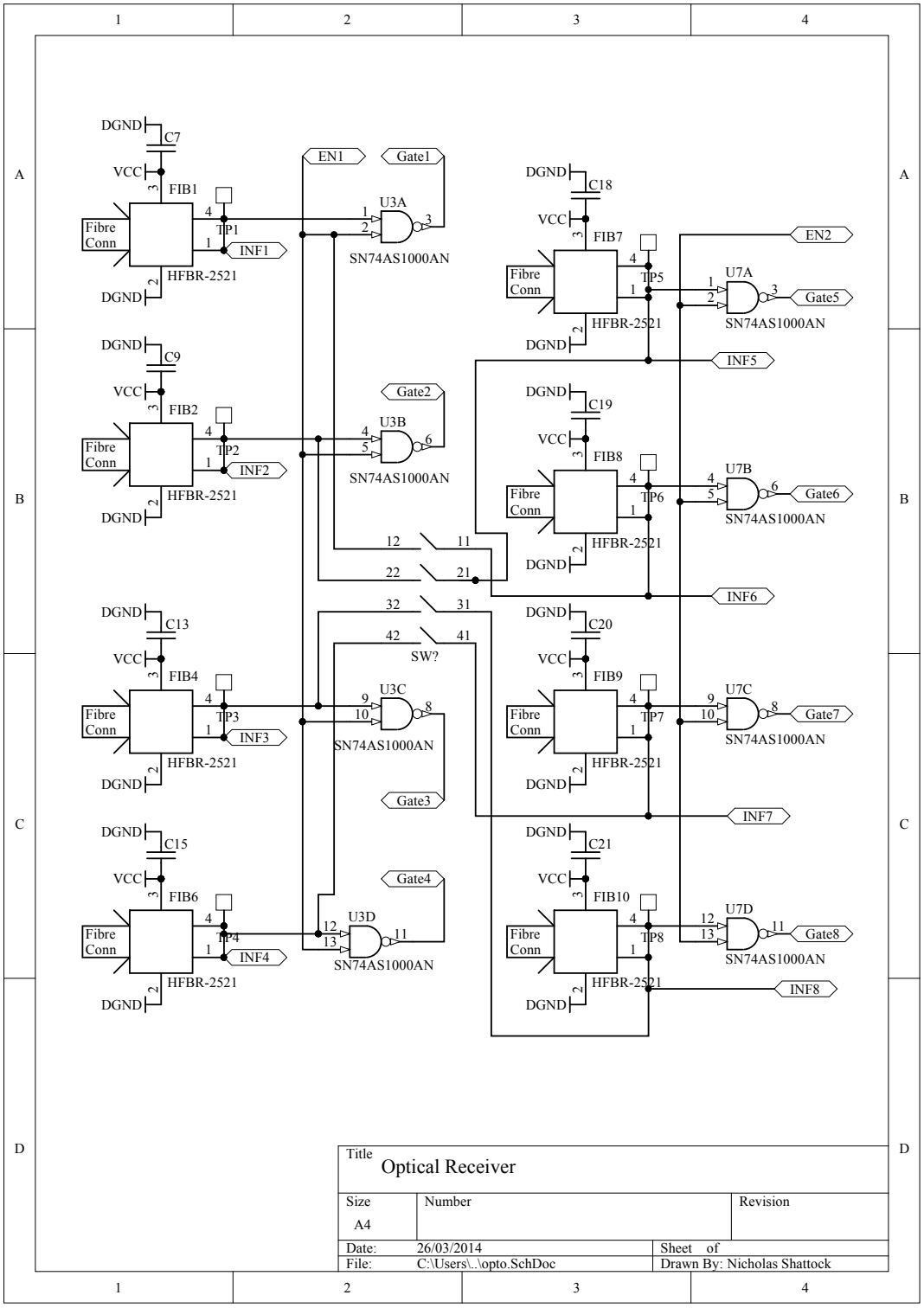


Figure B.4: Schematic of Optical receiver section of Cycloconverter Control PCB

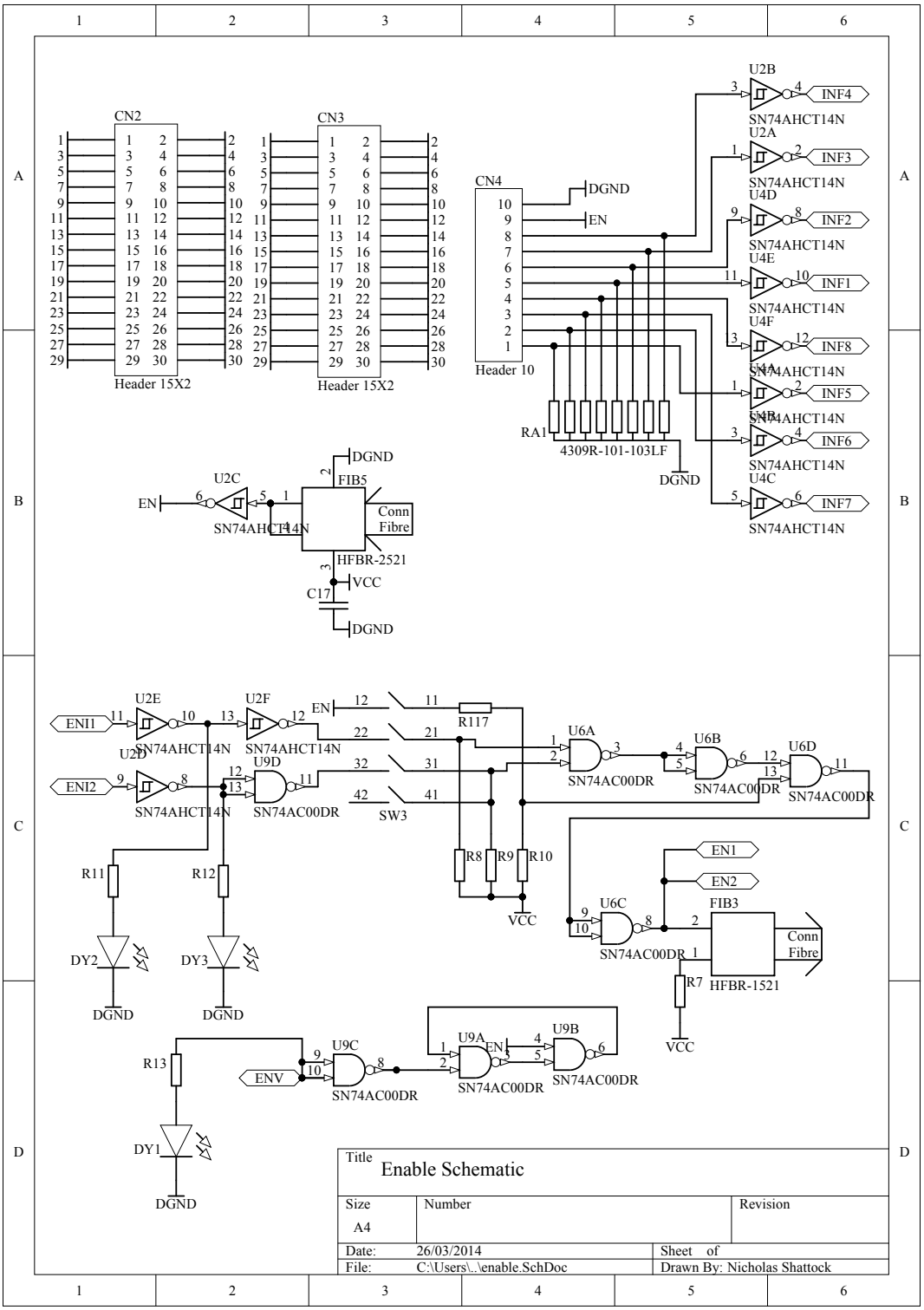


Figure B.5: Schematic of Enable section of Cycloconverter Control PCB

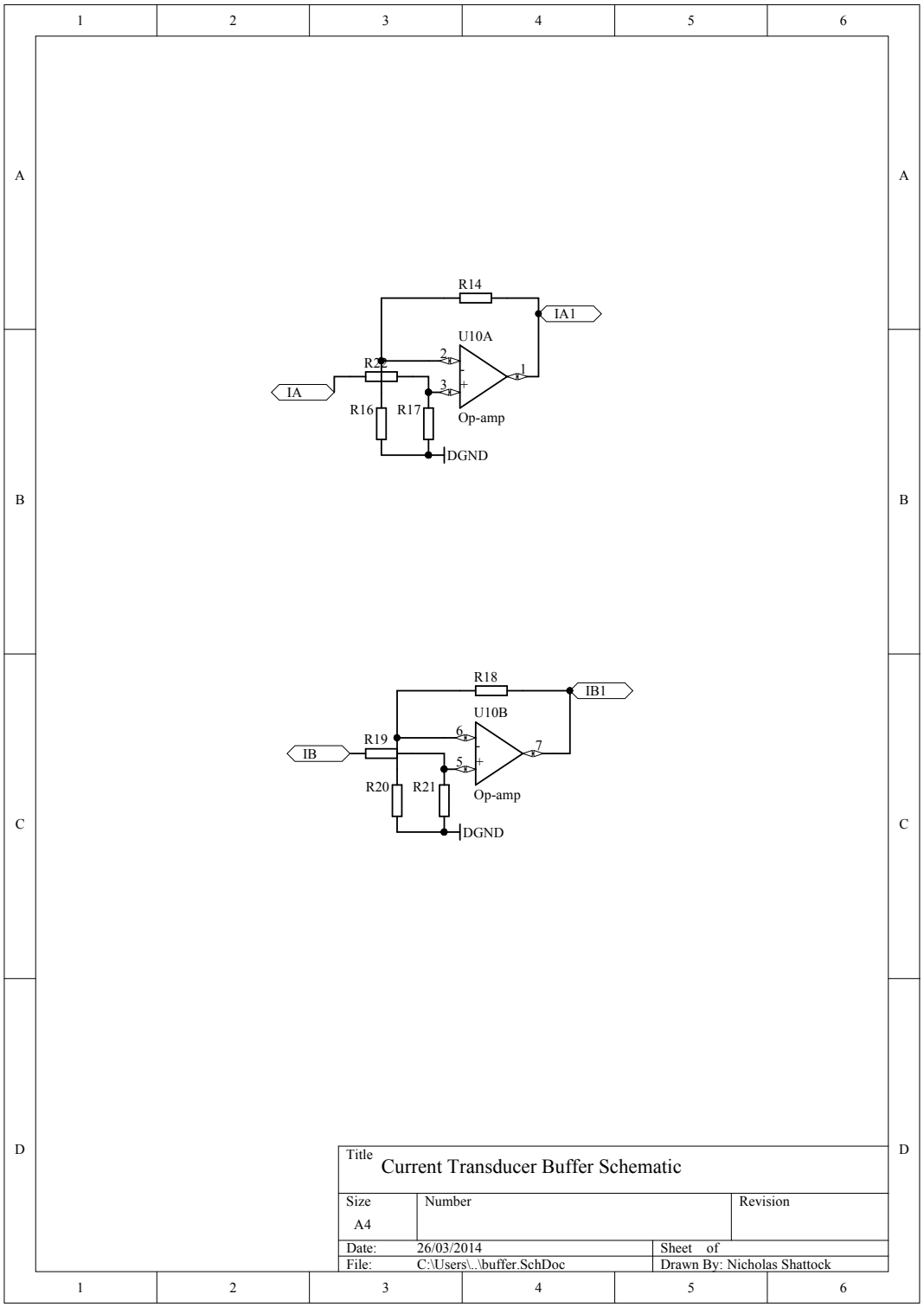


Figure B.6: Schematic of Buffer section of Cycloconverter Control PCB

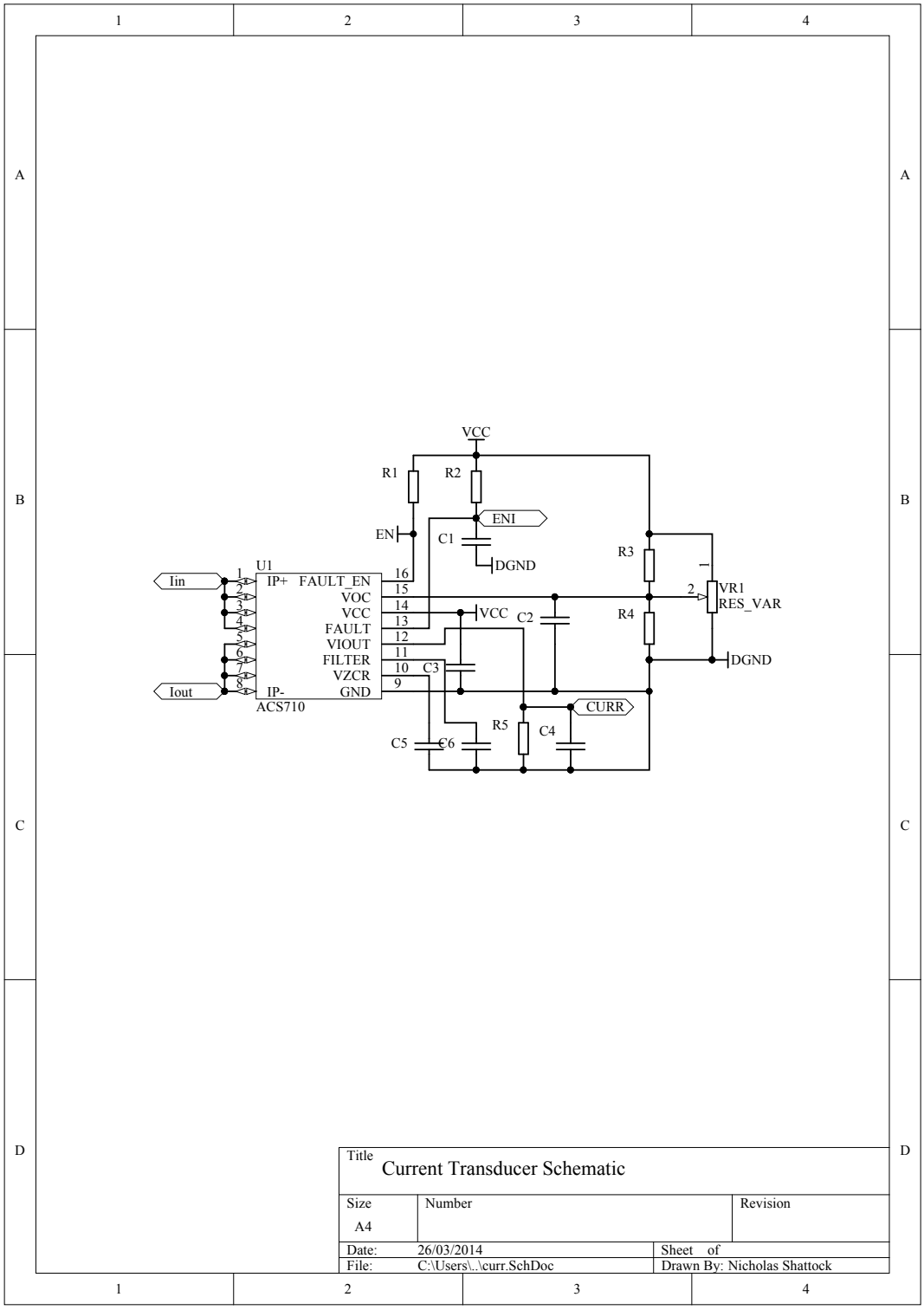


Figure B.7: Schematic of over current protection section of Cycloconverter Control PCB

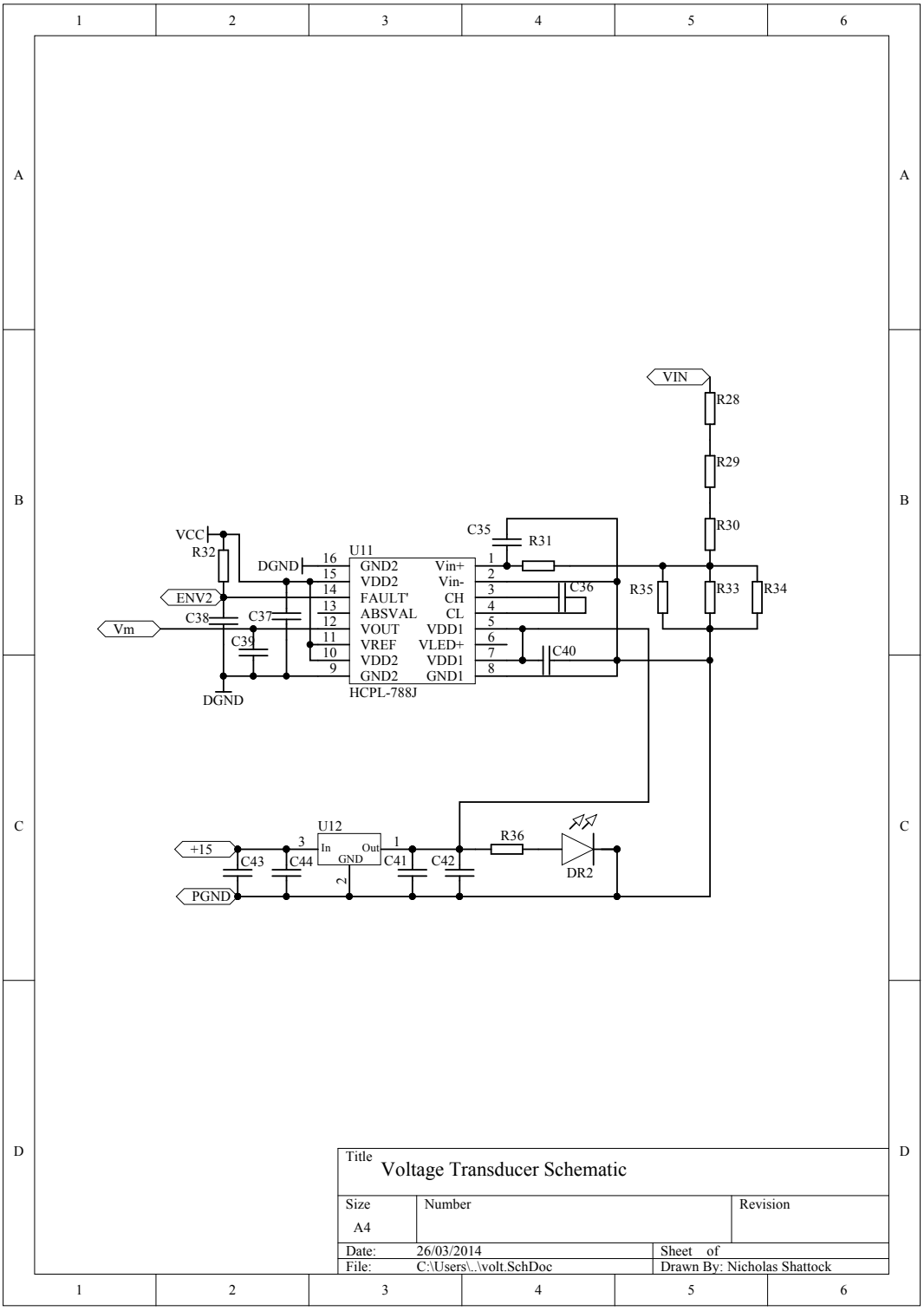


Figure B.8: Schematic of over Voltage protection section of Cycloconverter Control PCB

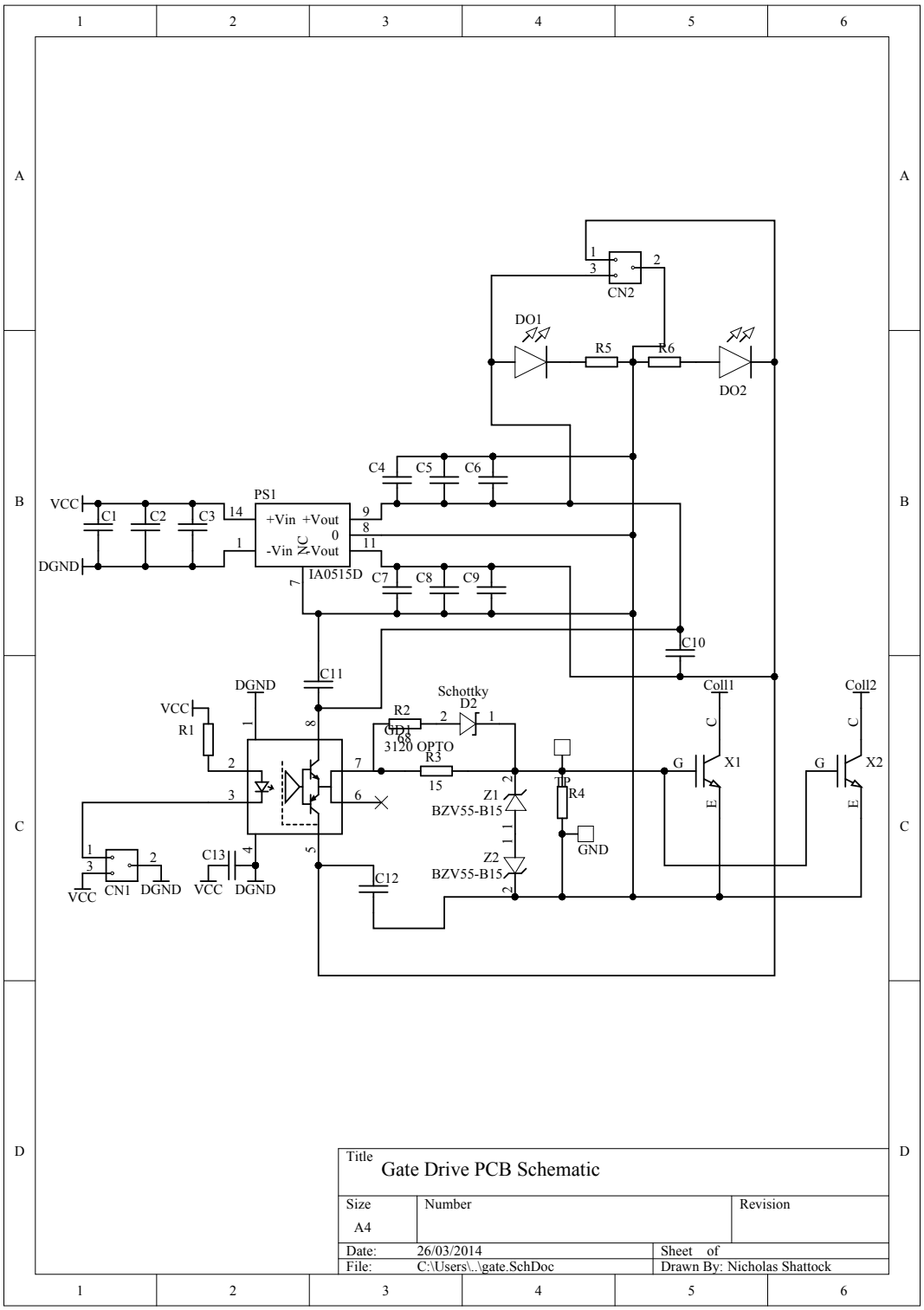


Figure B.9: Gate Drive Schematic

Appendix C

Results Tables

C.1 Transformer Parameters

Frequency (kHz)	Primary Magnetizing Inductance (mH)	Secondary Magnetizing Inductance (mH)	Primary Resistance (Ω)	Secondary Resistance (Ω)
1.00	3.59	3.59	0.22	0.22
1.16	3.59	3.58	0.25	0.24
1.35	3.59	3.58	0.27	0.26
1.56	3.58	3.58	0.31	0.29
1.81	3.58	3.57	0.34	0.33
2.10	3.58	3.57	0.38	0.37
2.44	3.57	3.57	0.42	0.40
2.83	3.57	3.57	0.45	0.45
3.28	3.57	3.56	0.50	0.49
3.81	3.56	3.56	0.54	0.53
4.42	3.56	3.56	0.59	0.58
5.13	3.56	3.56	0.62	0.62
5.95	3.56	3.56	0.67	0.65
6.90	3.57	3.56	0.71	0.70
8.01	3.57	3.56	0.75	0.73
9.29	3.57	3.56	0.76	0.75
10.78	3.58	3.57	0.82	0.80
12.50	3.59	3.57	0.81	0.79
14.51	3.60	3.59	2.13	2.15
16.83	3.62	3.60	2.01	2.38
19.53	3.65	3.62	2.63	2.62
22.65	3.68	3.65	2.93	2.95
26.28	3.69	3.68	3.34	3.33
30.49	3.74	3.74	3.87	3.87
35.38	3.81	3.81	4.53	4.53
41.04	3.91	3.91	5.43	5.48
47.62	4.05	4.05	6.72	6.74
55.25	4.26	4.25	8.88	8.89
64.10	4.58	4.57	12.44	12.51
74.36	5.09	5.08	19.39	19.50
86.28	5.98	5.96	35.40	35.42
100.10	7.85	7.81	83.29	83.03

Table C.1: Phase u Transformer Parameters, open circuit test

Frequency (kHz)	Leakage Inductance Referred to Primary (μH)	Leakage Inductance Referred to Secondary (μH)	Resistance Referred to Primary (mΩ)	Resistance Referred to Secondary (mΩ)
1.00	14.77	14.62	77.15	75.63
1.16	14.74	14.59	77.44	76.04
1.35	14.71	14.56	78.11	76.49
1.56	14.67	14.53	78.69	77.05
1.81	14.63	14.49	79.36	77.69
2.10	14.59	14.45	80.11	78.43
2.44	14.56	14.42	80.99	79.31
2.83	14.52	14.38	82.00	80.33
3.28	14.48	14.34	83.19	81.49
3.81	14.44	14.31	84.57	82.84
4.42	14.40	14.27	86.13	84.40
5.13	14.36	14.23	87.92	86.17
5.95	14.32	14.19	89.94	88.17
6.90	14.29	14.15	92.29	90.48
8.01	14.25	14.12	95.00	93.12
9.29	14.24	14.08	98.87	96.19
10.78	14.17	14.04	102.14	100.08
12.50	14.14	14.01	106.47	104.50
14.51	14.11	13.98	111.53	109.67
16.83	14.08	13.95	117.78	115.68
19.53	14.05	13.92	125.00	123.03
22.65	14.02	13.89	133.87	131.81
26.28	13.99	13.86	144.77	142.51
30.49	13.96	13.83	157.98	155.72
35.38	13.93	13.80	174.34	172.05
41.04	13.90	13.77	194.71	192.47
47.62	13.88	13.75	220.54	218.04
55.25	13.85	13.72	252.48	250.19
64.10	13.82	13.69	294.40	291.54
74.36	13.80	13.67	346.91	344.63
86.28	13.77	13.64	415.38	412.56
100.10	13.74	13.61	504.21	500.96

Table C.2: Phase u Transformer Parameters, short circuit test

Frequency (kHz)	Primary Magnetizing Inductance (mH)	Secondary Magnetizing Inductance (mH)	Primary Resistance (Ω)	Secondary Resistance (Ω)
1.00	3.66	3.65	0.22	0.22
1.16	3.66	3.65	0.24	0.24
1.35	3.66	3.64	0.26	0.27
1.56	3.65	3.64	0.29	0.29
1.81	3.65	3.64	0.34	0.32
2.10	3.65	3.63	0.37	0.35
2.44	3.64	3.63	0.41	0.75
2.83	3.64	3.63	0.45	0.46
3.28	3.64	3.62	0.50	0.50
3.81	3.64	3.62	0.54	0.54
4.42	3.64	3.62	0.58	0.59
5.13	3.64	3.61	0.63	0.63
5.95	3.64	3.61	0.67	0.68
6.90	3.65	3.61	0.71	0.72
8.01	3.65	3.62	0.73	0.75
9.29	3.66	3.62	0.76	0.78
10.78	3.66	3.62	0.74	0.81
12.50	3.67	3.63	0.76	1.97
14.51	3.67	3.64	2.16	2.13
16.83	3.68	3.67	2.42	2.37
19.53	3.69	3.69	2.71	2.66
22.65	3.71	3.71	3.05	3.00
26.28	3.74	3.75	3.34	3.42
30.49	3.84	3.80	4.01	3.96
35.38	3.92	3.89	4.68	4.70
41.04	4.03	3.99	5.75	5.66
47.62	4.20	4.15	7.23	7.06
55.25	4.44	4.38	9.66	9.48
64.10	4.81	4.74	14.08	13.64
74.36	5.43	5.32	22.98	21.98
86.28	6.56	6.38	44.90	41.92
100.10	9.10	8.71	121.21	108.48

Table C.3: Phase v Transformer Parameters, open circuit test

Frequency (kHz)	Leakage Inductance Referred to Primary (μH)	Leakage Inductance Referred to Secondary (μH)	Resistance Referred to Primary (mΩ)	Resistance Referred to Secondary (mΩ)
1.00	13.34	13.54	67.19	70.63
1.16	13.32	13.52	67.50	70.95
1.35	13.30	13.49	67.87	71.38
1.56	13.27	13.47	68.29	71.81
1.81	13.24	13.44	68.77	72.24
2.10	13.21	13.41	69.32	72.79
2.44	13.18	13.38	69.99	73.49
2.83	13.15	13.35	70.73	74.19
3.28	13.13	13.33	71.61	75.03
3.81	13.10	13.30	72.63	76.04
4.42	13.07	13.27	73.80	77.17
5.13	13.04	13.25	75.16	78.49
5.95	13.01	13.22	76.74	80.02
6.90	12.99	13.19	78.56	81.72
8.01	12.96	13.17	80.69	83.75
9.29	12.97	13.17	83.20	86.90
10.78	12.91	13.11	86.43	89.40
12.50	12.88	13.09	90.15	93.08
14.51	12.86	13.07	94.69	97.45
16.83	12.84	13.05	99.97	102.84
19.53	12.81	13.02	106.57	109.32
22.65	12.79	13.00	114.61	117.29
26.28	12.77	12.98	124.65	127.22
30.49	12.75	12.96	137.14	139.59
35.38	12.73	12.94	152.76	155.24
41.04	12.70	12.91	172.53	175.23
47.62	12.68	12.89	197.66	200.29
55.25	12.66	12.87	229.95	232.66
64.10	12.64	12.85	271.38	273.80
74.36	12.61	12.82	325.00	327.62
86.28	12.59	12.80	395.13	397.30
100.10	12.56	12.77	485.36	487.80

Table C.4: Phase v Transformer Parameters, short circuit test

Frequency (kHz)	Primary Magnetizing Inductance (mH)	Secondary Magnetizing Inductance (mH)	Primary Resistance (Ω)	Secondary Resistance (Ω)
1.00	3.83	3.71	0.22	0.22
1.16	3.82	3.70	0.24	0.24
1.35	3.82	3.70	0.27	0.27
1.56	3.82	3.70	0.29	0.29
1.81	3.82	3.70	0.32	0.32
2.10	3.81	3.69	0.35	0.35
2.44	3.81	3.69	0.39	0.38
2.83	3.81	3.69	0.43	0.42
3.28	3.81	3.69	0.47	0.46
3.81	3.81	3.69	0.51	0.50
4.42	3.81	3.69	0.55	0.54
5.13	3.80	3.69	0.60	0.58
5.95	3.80	3.69	0.63	0.63
6.90	3.80	3.69	0.68	0.67
8.01	3.81	3.69	0.72	0.71
9.29	3.81	3.69	0.75	0.73
10.78	3.81	3.70	0.78	0.77
12.50	3.82	3.70	0.81	0.81
14.51	3.83	3.71	0.86	0.81
16.83	3.85	3.72	0.90	0.86
19.53	3.87	3.74	0.95	0.93
22.65	3.89	3.77	0.98	0.90
26.28	3.93	3.80	0.98	0.91
30.49	3.98	3.85	1.01	0.92
35.38	4.05	3.92	1.07	0.96
41.04	4.16	4.02	1.30	1.12
47.62	4.30	4.15	1.89	1.65
55.25	4.51	4.35	2.88	2.53
64.10	4.84	4.65	5.08	4.51
74.36	5.35	5.12	9.86	8.61
86.28	6.22	5.92	21.11	18.43
100.10	8.02	7.53	55.48	48.32

Table C.5: Phase w Transformer Parameters, open circuit test

Frequency (kHz)	Leakage Inductance Referred to Primary (μH)	Leakage Inductance Referred to Secondary (μH)	Resistance Referred to Primary (mΩ)	Resistance Referred to Secondary (mΩ)
1.00	15.80	16.00	71.65	70.74
1.16	15.77	15.97	72.04	71.14
1.35	15.74	15.93	72.46	71.58
1.56	15.71	15.89	72.96	72.11
1.81	15.66	15.86	73.56	72.71
2.10	15.63	15.82	74.23	73.41
2.44	15.59	15.79	75.01	74.20
2.83	15.56	15.75	75.92	75.12
3.28	15.52	15.72	76.97	76.19
3.81	15.49	15.68	78.16	77.40
4.42	15.46	15.65	79.55	78.79
5.13	15.42	15.61	81.12	80.40
5.95	15.39	15.57	82.95	82.23
6.90	15.36	15.54	85.04	84.34
8.01	15.32	15.51	87.42	86.79
9.29	15.29	15.48	90.25	89.62
10.78	15.26	15.45	93.95	93.18
12.50	15.23	15.42	97.88	97.26
14.51	15.20	15.39	102.76	102.21
16.83	15.17	15.36	108.52	107.97
19.53	15.14	15.33	115.53	114.99
22.65	15.12	15.30	123.99	123.44
26.28	15.09	15.28	134.23	133.83
30.49	15.06	15.25	147.20	146.81
35.38	15.04	15.23	163.17	162.86
41.04	15.01	15.20	182.95	183.34
47.62	14.99	15.18	208.60	209.17
55.25	14.97	15.15	240.97	241.90
64.10	14.94	15.13	281.94	284.13
74.36	14.92	15.11	335.49	338.17
86.28	14.89	15.08	403.97	408.48
100.10	14.87	15.06	493.40	499.48

Table C.6: Phase w Transformer Parameters, short circuit test

C.2 Experimental Converter Loss Results

$i_d{}^*$	U_{DC}	I_{DC}	DC W	u_{uvw}	i_{uvw}	AC W	Loss W	Loss % AC
1.1	350.18	0.57	198.88	35.00	1.20	125.27	73.61	58.76
1.3	350.15	0.74	258.52	41.22	1.41	174.09	84.43	48.50
1.5	350.18	0.93	325.63	47.42	1.63	230.57	95.06	41.23
1.7	350.18	1.15	401.75	53.58	1.84	294.62	107.13	36.36
1.9	350.17	1.39	484.99	59.74	2.05	366.29	118.70	32.41
2.1	350.17	1.65	575.41	65.87	2.26	445.35	130.06	29.20
2.3	350.14	1.93	673.52	71.98	2.47	531.70	141.82	26.67
2.5	350.14	2.23	778.91	78.07	2.68	625.28	153.63	24.57
2.7	350.13	2.55	890.48	84.13	2.88	725.86	164.62	22.68
2.9	350.13	2.89	1009.20	90.15	3.09	833.43	175.77	21.09
3.1	350.12	3.25	1134.40	96.15	3.29	947.78	186.62	19.69
3.3	350.14	3.62	1265.90	102.11	3.50	1068.70	197.20	18.45
3.5	350.12	4.02	1404.60	108.03	3.70	1196.20	208.40	17.42
3.7	350.11	4.43	1548.20	113.92	3.90	1329.80	218.40	16.42
3.9	350.10	4.86	1697.90	119.76	4.10	1469.60	228.30	15.53
4.1	350.08	5.30	1853.30	125.56	4.30	1615.40	237.90	14.73
4.3	350.07	5.76	2014.10	131.33	4.50	1766.90	247.20	13.99
4.5	350.04	6.24	2180.80	137.05	4.69	1924.30	256.50	13.33
4.7	350.01	6.73	2352.50	142.74	4.89	2087.30	265.20	12.71
4.9	350.04	7.24	2529.20	148.37	5.08	2255.50	273.70	12.13
5.1	350.04	7.76	2710.90	153.96	5.27	2429.10	281.80	11.60
5.3	350.01	8.29	2897.60	159.51	5.47	2607.70	289.90	11.12
5.5	350.01	8.84	3088.80	164.99	5.66	2791.00	297.80	10.67
5.7	349.97	9.39	3284.00	170.42	5.84	2978.80	305.20	10.25
5.9	349.97	9.96	3482.70	175.78	6.03	3170.20	312.50	9.86
6.1	349.98	10.54	3684.80	181.05	6.21	3365.20	319.60	9.50
6.3	349.97	11.13	3890.20	186.25	6.40	3563.40	326.80	9.17
6.5	349.90	11.79	4120.50	192.44	6.58	3784.40	336.10	8.88
6.7	349.88	12.41	4340.40	197.73	6.76	3996.90	343.50	8.59
6.9	349.88	13.07	4569.30	203.10	6.95	4218.70	350.60	8.31
7.1	349.88	13.76	4809.60	208.54	7.14	4450.20	359.40	8.08
7.3	349.88	14.47	5058.70	214.01	7.33	4690.00	368.70	7.86
7.5	349.85	15.19	5312.10	219.39	7.52	4933.90	378.20	7.67

Table C.7: Cycloconverter power losses against AC power into resistive load

$i_d{}^*$	U_{DC}	I_{DC}	DC W	u_{uvw}	i_{uvw}	AC W	Loss W	Loss % AC
1.1	350.21	0.77	268.35	45.53	1.26	170.82	97.53	57.10
1.3	350.23	1.00	349.51	53.48	1.48	236.05	113.46	48.07
1.5	350.22	1.26	440.73	61.40	1.70	311.40	129.33	41.53
1.7	350.20	1.55	541.18	69.26	1.92	396.40	144.78	36.52
1.9	350.20	1.87	651.21	77.05	2.14	490.80	160.41	32.68
2.1	350.18	2.21	770.60	84.78	2.35	594.45	176.15	29.63
2.3	350.18	2.57	897.68	92.44	2.56	706.95	190.73	26.98
2.5	350.17	2.96	1033.70	100.04	2.77	828.11	205.59	24.83
2.7	350.17	3.37	1176.60	107.56	2.98	957.56	219.04	22.87
2.9	350.16	3.80	1327.40	115.03	3.19	1095.10	232.30	21.21
3.1	350.12	4.26	1487.40	122.40	3.39	1240.20	247.20	19.93
3.3	350.11	4.73	1652.30	129.68	3.59	1392.40	259.90	18.67
3.5	350.09	5.22	1823.00	136.87	3.79	1551.60	271.40	17.49
3.7	350.08	5.72	1999.80	143.98	3.99	1717.40	282.40	16.44
3.9	350.05	6.24	2182.30	151.00	4.19	1889.70	292.60	15.48
4.1	350.02	6.78	2370.10	157.96	4.38	2068.40	301.70	14.59
4.3	350.03	7.34	2564.70	164.85	4.57	2253.10	311.60	13.83
4.5	350.02	7.90	2763.40	171.65	4.76	2443.80	319.60	13.08
4.7	350.02	8.49	2968.00	178.38	4.95	2639.90	328.10	12.43
4.9	349.99	9.08	3176.20	185.04	5.13	2841.40	334.80	11.78
5.1	349.97	9.69	3389.30	191.63	5.31	3048.20	341.10	11.19
5.3	349.97	10.32	3608.50	198.12	5.50	3259.70	348.80	10.70
5.5	349.95	10.95	3830.40	204.50	5.67	3474.70	355.70	10.24
5.7	349.93	11.59	4053.50	210.77	5.85	3692.00	361.50	9.79
5.9	349.83	12.23	4277.50	216.88	6.02	3910.60	366.90	9.38
6.1	349.89	12.88	4504.80	222.89	6.19	4131.70	373.10	9.03
6.3	349.88	13.54	4735.80	228.85	6.35	4357.20	378.60	8.69
6.5	349.87	14.23	4976.00	234.88	6.52	4591.80	384.20	8.37
6.7	349.86	14.96	5232.40	241.13	6.70	4841.70	390.70	8.07
6.9	349.83	15.76	5510.10	247.73	6.89	5113.00	397.10	7.77
7.1	349.81	16.62	5811.30	254.68	7.08	5406.60	404.70	7.49
7.3	349.80	17.51	6124.30	261.63	7.28	5709.70	414.60	7.26
7.5	349.77	18.39	6429.90	268.25	7.47	6007.10	422.80	7.04

Table C.8: Hybrid Cycloconverter power losses against AC power into resistive load

$i_d{}^*$	U_{DC}	I_{DC}	DC W	u_{uvw}	i_{uvw}	AC W	Loss W	Loss % AC
-2.0	2.31	150.95	1000.20	2.55	350.64	859.81	140.39	14.04
-2.5	2.80	150.91	1228.30	3.10	350.49	1067.10	161.20	13.12
-3.0	3.29	150.86	1455.00	3.66	350.63	1279.70	175.30	12.05
-3.5	3.78	150.82	1681.90	4.25	350.65	1488.50	193.40	11.50
-4.0	4.28	150.77	1908.40	4.85	350.66	1696.80	211.60	11.09
-4.5	4.77	150.73	2134.90	5.44	350.66	1904.80	230.10	10.78
-5.0	5.27	150.68	2361.40	6.03	350.67	2111.90	249.50	10.57
-5.5	5.77	150.63	2587.90	6.62	350.68	2318.90	269.00	10.39
-6.0	6.27	150.60	2814.10	7.21	350.72	2525.60	288.50	10.25
-6.5	6.77	150.55	3039.50	7.80	350.72	2731.70	307.80	10.13
-7.0	7.27	150.52	3265.90	8.39	350.75	2936.90	329.00	10.07
-7.5	7.77	150.47	3491.30	8.97	350.79	3141.60	349.70	10.02
-8.0	8.27	150.43	3717.40	9.55	350.79	3345.80	371.60	10.00
-8.5	8.77	150.39	3943.20	10.19	348.88	3548.10	395.10	10.02
-9.0	9.27	150.34	4168.20	10.77	348.88	3751.20	417.00	10.00
-9.5	9.78	150.31	4394.20	11.35	348.89	3952.90	441.30	10.04
-10.0	10.28	150.27	4619.70	11.93	348.90	4154.10	465.60	10.08
-10.5	10.78	150.23	4846.20	12.50	348.90	4355.40	490.80	10.13
-11.0	11.29	150.18	5072.30	13.08	348.94	4556.40	515.90	10.17
-11.5	11.80	150.15	5301.00	13.66	348.95	4758.90	542.10	10.23
-12.0	12.31	150.10	5530.60	14.24	348.94	4960.80	569.80	10.30
-12.5	12.83	150.06	5763.20	14.83	348.96	5165.90	597.30	10.36
-13.0	13.36	150.03	5999.30	15.42	348.99	5373.30	626.00	10.43
-13.5	13.90	149.98	6240.70	16.03	349.00	5585.70	655.00	10.50
-14.0	14.46	149.92	6487.00	16.65	348.96	5800.50	686.50	10.58
-14.5	15.03	149.89	6742.10	17.35	347.96	6024.10	718.00	10.65

Table C.9: Cycloconverter power losses against AC power, power transfer from AC to DC networks

$i_d{}^*$	U_{DC}	I_{DC}	DC W	u_{uvw}	i_{uvw}	AC W	Loss W	Loss % AC
-2.0	2.37	185.60	1248.80	3.35	340.52	1088.20	160.60	12.86
-2.5	2.88	185.57	1533.30	3.98	350.66	1342.50	190.80	12.44
-3.0	3.37	185.54	1814.00	4.63	347.58	1606.10	207.90	11.46
-3.5	3.86	185.50	2093.20	5.37	347.62	1866.10	227.10	10.85
-4.0	4.35	185.46	2372.40	6.12	347.64	2124.70	247.70	10.44
-4.5	4.85	185.42	2651.50	6.86	347.66	2383.20	268.30	10.12
-5.0	5.34	185.39	2931.10	7.61	347.67	2641.20	289.90	9.89
-5.5	5.84	185.34	3209.60	8.35	347.69	2898.00	311.60	9.71
-6.0	6.34	185.33	3489.00	9.09	347.71	3154.80	334.20	9.58
-6.5	6.84	185.27	3767.00	9.82	347.74	3410.20	356.80	9.47
-7.0	7.34	185.25	4046.20	10.55	347.77	3665.50	380.70	9.41
-7.5	7.83	185.20	4324.00	11.28	347.78	3918.30	405.70	9.38
-8.0	8.34	185.16	4602.70	12.01	347.82	4172.30	430.40	9.35
-8.5	8.84	185.14	4881.00	12.74	347.82	4424.70	456.30	9.35
-9.0	9.34	185.11	5159.90	13.46	347.86	4677.00	482.90	9.36
-9.5	9.84	185.06	5437.70	14.18	347.90	4927.60	510.10	9.38
-10.0	10.34	185.03	5716.80	14.90	347.90	5179.30	537.50	9.40
-10.5	10.85	184.99	5996.20	15.63	347.92	5430.70	565.50	9.43
-11.0	11.35	184.96	6277.10	16.35	347.89	5681.80	595.30	9.48
-11.5	11.86	184.92	6559.80	17.08	347.97	5935.20	624.60	9.52
-12.0	12.38	184.88	6845.50	17.81	348.03	6190.60	654.90	9.57
-12.5	12.90	184.85	7134.90	18.56	348.03	6448.90	686.00	9.61
-13.0	13.44	184.80	7429.20	19.31	348.03	6711.00	718.20	9.67
-13.5	13.98	184.77	7731.10	20.10	348.03	6983.00	748.10	9.68
-14.0	14.54	184.72	8040.00	20.88	348.06	7255.40	784.60	9.76
-14.5	15.12	184.68	8358.90	21.70	348.05	7539.00	819.90	9.81

Table C.10: Hybrid Cycloconverter power losses against AC power, power transfer from AC to DC networks

$i_d{}^*$	U_{DC}	I_{DC}	DC W	u_{uvw}	i_{uvw}	AC W	Loss W	Loss % AC
2.0	2.42	151.40	1054.40	3.37	350.27	1179.80	125.40	11.89
2.5	2.90	151.45	1280.30	4.07	350.22	1420.70	140.40	10.97
3.0	3.39	151.50	1507.10	4.76	350.15	1663.60	156.50	10.38
3.5	3.88	151.54	1734.60	5.46	350.11	1907.80	173.20	9.99
4.0	4.37	151.59	1962.60	6.16	350.08	2153.10	190.50	9.71
4.5	4.87	151.63	2191.00	6.87	350.05	2399.60	208.60	9.52
5.0	5.37	151.67	2419.50	7.57	350.03	2646.80	227.30	9.39
5.5	5.86	151.72	2648.50	8.29	349.97	2894.90	246.40	9.30
6.0	6.36	151.76	2876.90	9.00	349.93	3144.10	267.20	9.29
6.5	6.86	151.80	3105.00	9.71	349.91	3393.70	288.70	9.30
7.0	7.36	151.84	3333.90	10.43	349.89	3643.10	309.20	9.27
7.5	7.86	151.88	3563.00	11.15	349.88	3894.80	331.80	9.31
8.0	8.36	151.92	3792.40	11.87	349.82	4147.40	355.00	9.36
8.5	8.86	151.96	4021.80	12.60	349.79	4400.70	378.90	9.42
9.0	9.36	151.94	4249.10	13.31	349.85	4650.00	400.90	9.43
9.5	9.86	151.98	4479.40	14.04	349.81	4905.60	426.20	9.51
10.0	10.37	152.02	4710.70	14.78	349.77	5162.80	452.10	9.60
10.5	10.87	152.06	4942.90	15.53	349.75	5422.00	479.10	9.69
11.0	11.38	152.10	5177.00	16.28	349.72	5684.30	507.30	9.80
11.5	11.90	152.14	5414.30	17.04	349.66	5949.80	535.50	9.89
12.0	12.42	152.19	5654.50	17.82	349.63	6219.50	565.00	9.99
12.5	12.96	152.23	5899.90	18.61	349.57	6497.00	597.10	10.12
13.0	13.50	152.28	6150.80	19.43	349.54	6781.80	631.00	10.26
13.5	14.06	152.33	6408.30	20.27	349.50	7073.60	665.30	10.38
14.0	14.64	152.38	6674.10	21.13	349.45	7374.60	700.50	10.50
14.5	15.24	152.43	6949.10	22.04	349.45	7689.50	740.40	10.65

Table C.11: Cycloconverter power losses against AC power, power transfer from DC to AC networks

$i_d{}^*$	U_{DC}	I_{DC}	DC W	u_{uvw}	i_{uvw}	AC W	Loss W	Loss % AC
2.0	1.97	185.96	1011.60	3.30	350.21	1152.80	141.20	13.96
2.5	2.44	186.00	1276.60	4.10	350.09	1430.70	154.10	12.07
3.0	2.92	186.04	1551.60	4.94	350.02	1721.80	170.20	10.97
3.5	3.41	186.08	1828.90	5.77	350.01	2016.40	187.50	10.25
4.0	3.90	186.13	2107.00	6.62	349.98	2313.40	206.40	9.80
4.5	4.40	186.17	2386.10	7.47	349.94	2612.20	226.10	9.48
5.0	4.89	186.21	2665.90	8.33	349.88	2911.90	246.00	9.23
5.5	5.39	186.25	2945.90	9.21	349.82	3213.90	268.00	9.10
6.0	5.88	186.29	3225.60	10.08	349.80	3518.90	293.30	9.09
6.5	6.38	186.34	3506.00	10.94	349.80	3823.20	317.20	9.05
7.0	6.87	186.38	3786.40	11.81	349.80	4126.90	340.50	8.99
7.5	7.37	186.42	4067.00	12.69	349.80	4433.20	366.20	9.00
8.0	7.87	186.46	4348.00	13.57	349.74	4740.30	392.30	9.02
8.5	8.37	186.50	4629.40	14.46	349.71	5048.50	419.10	9.05
9.0	8.88	186.54	4912.90	15.35	349.73	5359.90	447.00	9.10
9.5	9.37	186.58	5193.30	16.23	349.70	5668.80	475.50	9.16
10.0	9.88	186.63	5476.50	17.14	349.65	5982.10	505.60	9.23
10.5	10.38	186.67	5761.20	18.04	349.59	6297.30	536.10	9.31
11.0	10.89	186.71	6047.90	18.95	349.56	6615.00	567.10	9.38
11.5	11.41	186.75	6337.10	19.88	349.52	6937.40	600.30	9.47
12.0	11.93	186.80	6630.70	20.82	349.47	7263.80	633.10	9.55
12.5	12.43	186.84	6928.70	21.77	349.44	7596.90	668.20	9.64
13.0	12.97	186.89	7233.10	22.75	349.39	7939.00	705.90	9.76
13.5	13.52	186.94	7545.10	23.77	349.35	8291.20	746.10	9.89
14.0	14.09	186.99	7865.90	24.81	349.30	8653.30	787.40	10.01
14.5	14.68	187.04	8196.10	25.88	349.26	9026.80	830.70	10.14

Table C.12: Hybrid Cycloconverter power losses against AC power, power transfer from DC to AC networks

Angle	U_{DC}	I_{DC}	DC W	u_{uvw}	i_{uvw}	AC W	Loss W	Loss % AC
0.00	346.79	14.17	4906.00	151.98	9.86	4479.70	426.30	9.52
11.25	346.79	13.92	4819.60	151.88	9.87	4394.20	425.40	9.50
22.50	346.82	13.16	4557.80	151.70	9.88	4137.30	420.50	9.39
33.75	346.86	11.94	4134.70	151.50	9.91	3719.40	415.30	9.27
45.00	346.93	10.30	3569.60	151.27	9.94	3158.70	410.90	9.17
56.25	347.00	8.33	2886.00	151.04	9.99	2477.60	408.40	9.12
67.50	347.05	6.12	2119.20	150.86	10.07	1707.20	412.00	9.20
78.75	347.14	3.72	1286.90	150.68	10.14	868.23	418.67	9.35
90.00	347.19	1.21	414.37	150.55	10.23	-3.14	417.51	9.32
101.25	347.28	1.51	-466.24	150.42	10.30	-886.69	420.45	9.39
112.50	347.40	3.80	-1317.20	150.31	10.31	-1747.70	430.50	9.61
123.75	347.54	6.16	-2137.80	150.23	10.22	-2565.70	427.90	9.55
135.00	347.63	8.14	-2823.00	150.18	10.24	-3261.70	438.70	9.79
146.25	347.67	9.75	-3384.50	150.16	10.26	-3833.10	448.60	10.01
157.50	347.74	10.95	-3801.00	150.16	10.27	-4259.80	458.80	10.24
168.75	347.74	11.69	-4058.80	150.18	10.28	-4525.00	466.20	10.41
180.00	347.74	11.95	-4150.60	150.24	10.28	-4619.70	469.10	10.47
191.25	347.74	11.69	-4058.30	150.19	10.28	-4525.20	466.90	10.42
202.50	347.71	10.95	-3799.50	150.15	10.27	-4259.80	460.30	10.28
213.75	347.67	9.75	-3384.30	150.15	10.26	-3833.70	449.40	10.03
225.00	347.60	8.13	-2822.40	150.17	10.24	-3261.80	439.40	9.81
236.25	347.54	6.16	-2135.90	150.22	10.22	-2564.80	428.90	9.57
247.50	347.43	3.91	-1315.10	150.30	10.32	-1746.70	431.60	9.63
258.75	347.31	1.51	-465.75	150.41	10.30	-887.52	421.77	9.42
270.00	347.23	1.21	415.15	150.53	10.24	-4.67	419.82	9.37
281.25	347.16	3.73	1290.40	150.68	10.14	868.86	421.54	9.41
292.50	347.06	6.12	2122.10	150.85	10.06	1705.90	416.20	9.29
303.75	346.98	8.34	2888.90	151.04	9.99	2476.80	412.10	9.20
315.00	346.92	10.31	3571.80	151.26	9.94	3158.40	413.40	9.23
326.25	346.86	11.94	4137.10	151.49	9.91	3719.80	417.30	9.32
337.50	346.80	13.17	4560.50	151.69	9.88	4137.10	423.40	9.45
348.75	346.79	13.93	4823.60	151.87	9.87	4394.30	429.30	9.58

Table C.13: Cycloconverter power loss against power factor angle

Angle	U_{DC}	I_{DC}	DC W	u_{uvw}	i_{uvw}	AC W	Loss W	Loss % AC
0.00	346.59	17.28	5981.30	186.61	17.28	5476.70	504.60	9.39
11.25	346.72	16.95	5870.80	186.48	16.95	5370.80	500.00	9.31
22.50	346.77	16.03	5552.80	186.31	16.03	5057.90	494.90	9.21
33.75	346.82	14.53	5034.20	186.10	14.53	4545.40	488.80	9.10
45.00	346.87	12.52	4339.80	185.89	12.52	3852.30	487.50	9.08
56.25	346.95	10.09	3498.30	185.70	10.09	3011.10	487.20	9.07
67.50	347.06	7.33	2539.80	185.53	7.33	2053.10	486.70	9.06
78.75	347.16	4.38	1516.80	185.39	4.38	1028.00	488.80	9.10
90.00	347.28	1.18	408.28	185.25	1.18	-74.03	482.31	8.98
101.25	347.41	2.05	-678.85	185.14	2.05	-1166.90	488.05	9.09
112.50	347.50	4.97	-1725.10	185.05	4.97	-2219.10	494.00	9.20
123.75	347.59	7.75	-2689.60	184.99	7.75	-3190.80	501.20	9.33
135.00	347.69	10.18	-3536.10	184.93	10.18	-4044.20	508.10	9.46
146.25	347.74	12.18	-4229.80	184.93	12.18	-4745.80	516.00	9.61
157.50	347.81	13.66	-4745.30	184.93	13.66	-5269.70	524.40	9.76
168.75	347.83	14.59	-5067.90	184.97	14.59	-5598.70	530.80	9.88
180.00	347.82	14.91	-5181.00	185.02	14.91	-5716.50	535.50	9.97
191.25	347.81	14.59	-5067.50	184.97	14.59	-5599.00	531.50	9.89
202.50	347.77	13.66	-4745.20	184.94	13.66	-5270.30	525.10	9.78
213.75	347.71	12.18	-4228.90	184.93	12.18	-4746.20	517.30	9.63
225.00	347.63	10.18	-3535.00	184.94	10.18	-4044.70	509.70	9.49
236.25	347.55	7.75	-2688.10	184.98	7.75	-3190.90	502.80	9.36
247.50	347.44	4.97	-1724.10	185.05	4.97	-2219.50	495.40	9.22
258.75	347.32	2.04	-677.66	185.14	2.04	-1166.80	489.14	9.11
270.00	347.21	1.19	409.07	185.26	1.19	-75.47	484.54	9.02
281.25	347.10	4.36	1512.40	185.39	4.36	1024.60	487.80	9.08
292.50	346.97	7.33	2538.90	185.54	7.33	2052.10	486.80	9.06
303.75	346.88	10.10	3498.90	185.71	10.10	3011.50	487.40	9.07
315.00	346.78	12.53	4339.90	185.90	12.53	3852.80	487.10	9.07
326.25	346.70	14.54	5034.30	186.11	14.54	4545.50	488.80	9.10
337.50	346.64	16.04	5553.30	186.32	16.04	5058.80	494.50	9.21
348.75	346.61	16.96	5872.90	186.49	16.96	5372.10	500.80	9.32

Table C.14: Hybrid Cycloconverter power loss against power factor angle