
# Three-Level Z-Source Hybrid Direct AC-AC Power Converter Topology

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## Abstract

Voltage source inverter (VSI) is the traditional power converter used to provide variable voltage and frequency from a fixed voltage supply for adjustable speed drive and many other applications. However, the maximum ac output voltage that can be synthesized by a VSI is limited to the available dc-link voltage.

With its unique structure, the Z-source inverter can utilise shoot-through states to boost the output voltage and provides an attractive single-stage dc-ac conversion that is able to buck and boost the voltage. For applications with a variable input voltage, this inverter is a very competitive topology. The same concept can equally be extended to the two-stage matrix converter, where a single Z-source network is inserted in its virtual dc-link. The topology formed is, thus, quite straightforward. Its modulation is, however, non-trivial if advantages like voltage buck-boost flexibility, minimum commutation count, ease of implementation, and sinusoidal input and output quantities are to be attained simultaneously.

This thesis presents two novel space vector modulation methods for controlling a three-level Z-source neutral point clamped VSI to enable the use of a boost function. The second of the two space vector modulation methods is then adopted and applied to a three-level, two-stage matrix converter with a Z-source network inserted in its virtual dc-link to increase the voltage transfer ratio beyond the intrinsic 86.6% limit. Simulation results are supported by experimental verification from two laboratory prototype converters.

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# List of Terms

| Notation | Meaning | Notation | Meaning |
|---|---|---|---|
| V | Volt | A | Ampere |
| $\Omega$ | Ohm | H | Henry |
| F | Farad | Hz | Hertz |
| $ac$ | Alternating current | $V_{pn}$ | Full dc-link voltage |
| $dc$ | Direct current | $ASD$ | Adjustable speed drive |
| $PWM$ | Pulse width modulation | $NPC$ | Neutral point clamped |
| $V_{DC}$ | DC supply | $SVM$ | Space vector modulation |
| $NTV$ | Nearest three vectors | $SVD$ | Space vector diagram |
| $GTO$ | Gate turn-off thyristor | $v_o$ | Neutral point voltage |
| $MOS$ | Metal-oxide-semiconductor | $i_o$ | Neutral point current |
| $MCT$ | MOS controlled thyristor | $VSI$ | Voltage source inverter |
| $IGBT$ | Integrated gate bipolar transistor | $IGCT$ | Integrated gate commutated transistor |
| $V_{pn,avg}$ | Average dc-link voltage | $v_D$, $v_{D_1}$, $v_{D_2}$ | Diode voltage drop |
| $RB$ | Reverse blocking | $p, n$ | DC-link terminals |
| $o$ | DC-link midpoint | $T_{sw}$ | Switching period |
| $V_0$ | Zero voltage vector | $V_{po}$, $V_{no}$ | Split dc-link voltages |
| $V_{S_i}$ | Small voltage vectors | $V_{M_i}$ | Medium voltage vectors |
| $V_{L_i}$ | Large voltage vectors | $V_{om}$ | Amplitude of $\vec{V}_{out}(t)$ |
| $m_I$ | Modulation index of inversion stage | $\vec{V}_{out}(t)$ | Reference output voltage vector |
| $REC$ | Reduced element count | $FST$ | Full-shoot-through |
| $L_1$, $L_2$ | Z-source inductors | $UST$ | Upper-shoot-through |
| $C_1$, $C_2$ | Z-source capacitors | $\hat{V}_i$ | Effective dc-link voltage |
| $V_{As}$, $V_{Bs}$, $V_{Cs}$ | Output line-to-load neutral voltages | $V_{Ao}$, $V_{Bo}$, $V_{Co}$ | Output line-to-dc link midpoint voltages |
| $V_{po,avg}$, $V_{no,avg}$ | Average values of $V_{po}$ and $V_{no}$ | $V_{AB}$, $V_{BC}$, $V_{CA}$ | Output line-to-line voltages |
| $MOSFET$ | Metal-oxide-semiconductor Field-effect transistor | $m_R$ | Modulation index of Rectification stage |
| $LST$ | Lower-shoot-through | $q$ | Voltage transfer ratio |
| $DSP$ | Digital signal processor | $SMC$ | Sparse matrix converter |

| Notation | Meaning | Notation | Meaning |
|---|---|---|---|
| $PCB$ | Printed circuit board | $R_d$ | Damping resistor |
| $d_{V_{Si}}$,$d_{V_{Mi}}$,$d_{V_{Li}}$ | Duty ratios of small, medium, large vectors | $\vec{I}_{in}(t)$ | Reference input current vector |
| $I_{in}$ | Amplitude of reference input current vector | $\theta_{out}$ | Angle of reference output voltage vector |
| $NTVV$ | Nearest three virtual vectors | $V_{V0}$ | Virtual zero voltage vector |
| $V_{V_{S_i}}$ | Virtual small voltage vectors | $V_{V_{M_i}}$ | Virtual medium voltage vectors |
| $V_{V_{L_i}}$ | Virtual large voltage vectors | $d_x$, $d_y$, $d_z$ | Duty ratios of virtual voltage vectors |
| $i_a$, $i_b$, $i_c$ | Three phase input currents | $ULST$ | Upper-lower-shoot-through |
| $T_{st}$ | Full-shoot-through time | $T_u$ | Upper-shoot-through time |
| $T_l$ | Lower-shoot-through time | $T_{ulst}$ | Total upper-lower-shoot-through time |
| $B$ | Boost factor for FST operation | $B'$ | Boost factor for ULST operation |
| $\hat{V}_{xo}$ | Peak fundamental ac phase-to-neutral voltage | $\hat{V}_{xy}$ | Peak fundamental ac line-to-line voltage |
| $V_{C_1}$, $V_{C_2}$, $V_C$ | Average Z-source capacitor voltage | $\hat{V}_{i\_UST}$ | DC-link voltage during UST states |
| $\hat{V}_{i\_LST}$ | DC-link voltage during LST states | $\hat{V}_{i\_NST}$ | DC-link voltage during NST states |
| $V_{sa}$, $V_{sb}$, $V_{sc}$ | Supply voltages | $I_A$, $I_B$, $I_B$ | Output currents |
| $V_a$, $V_b$, $V_c$ | Three-phase input voltages to matrix converter | $V_A$, $V_B$, $V_C$ | Three-phase output voltages |
| $\omega_i$ | Frequency of supply voltages | $\omega_o$ | Frequency of output voltages |
| $\phi_i$, $\phi_o$ | Input and output phase displacement angles | $V_{im}$ | Amplitude of input phase voltages |
| $V_{env}$ | Rectified input voltage envelope value | $\omega_c$ | Cut-off frequency of input filter |
| $d_\gamma$, $d_\delta$, $d_{0,rec}$ | Duty ratios for input current vectors | $d_\alpha$, $d_\beta$, $d_{0,inv}$ | Duty ratios for output voltage vectors |
| $L_f$, $C_f$ | Input filter inductor and capacitor | $C_c$, $R_c$ | Clamp capacitor and resistor |
| $TMC$ | Two-stage matrix converter | $VSMC$ | Very sparse matrix converter |
| $USMC$ | Ultra sparse matrix converter | $FPGA$ | Field programmable gate array |

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# Chapter 1

# Introduction

## 1.1 Background of dc-to-ac power conversion

The two-level voltage source inverter (VSI) is the traditional power converter used to provide variable voltage and frequency from a fixed voltage supply for adjustable speed drive (ASD) and many other applications. However, the fast $dv/dt$ transitions in the output waveforms generated by the two-level VSI have been reported as causing motor bearing and winding insulation breakdown problems in ASD applications [1, 2]. Furthermore, due to the lack of semiconductor devices with suitable power ratings, devices have to be series-connected in order to achieve high voltage operation. This connection creates difficulties in ensuring static and dynamic sharing of voltage stress across the series-connected semiconductor switches [3].

Multilevel converter topologies have been developed to overcome these deficiencies in two-level VSIs for medium and high voltage applications [4, 5, 6]. Multilevel converters are able to construct the output waveforms with smaller voltage steps thereby imposing a lower stress than two-level VSIs on motor bearing and winding insulation. By constructing the output waveforms with multiple voltage steps, the output waveforms more closely resemble the desired sinusoidal waveforms and the output

harmonic distortion is improved. Multilevel converter structures enable the voltage stress across the power semiconductor devices to be decreased with the increase in number of voltage levels, enabling the use of medium voltage rated semiconductor devices to construct converters for high voltage, high power applications.

Nevertheless, the maximum ac output line-to-line voltage that can be synthesized by multilevel VSIs (and for that matter all VSIs) can not exceed the available dc-link voltage. For applications where the dc source is not constant, for example fuel cells [7, 8], photovoltaic arrays [9], and during supply voltage sags, a dc-dc boost converter is often needed to boost the dc voltage to meet the required output voltage or to allow the nominal operating point to be favourably located [10, 11]. This additional converter increases the system complexity, cost and reduces efficiency.

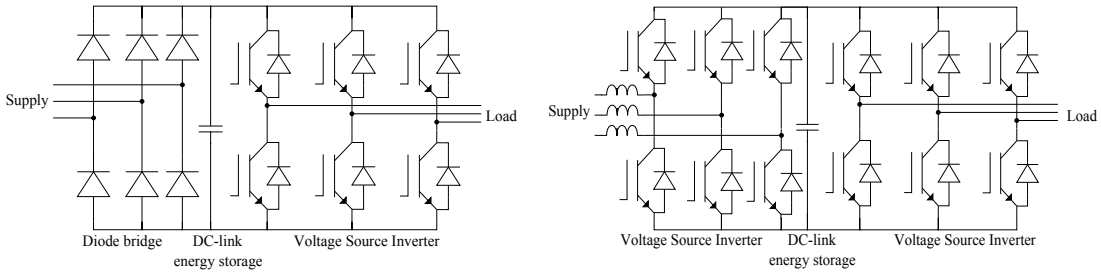
## 1.2 Background of ac-to-ac power conversion

The most common topology for ac-ac power conversion is based on a diode bridge rectifier at the supply side and a VSI at the load side, figure 1.1(a). The control of the output of this two stage converter is achieved by modulating the duty cycles of the devices in the inverter stage to produce near sinusoidal output currents at the desired amplitude and frequency.

Figure 1.1(a) shows the large capacitor that is usually placed across the dc-link to provide a stiff dc voltage source and energy storage between the two stages. A large capacitance is needed but within a reasonable volume, therefore electrolytic capacitors are normally used for the dc-link. Electrolytic capacitors typically occupy 30-50% of the total volume of the converter for power levels greater than a few kW and in addition to this they are temperature sensitive [12].

Due to the diode bridge front end, the inverter circuit shown in figure 1.1(a) will draw input currents that are rich in 5th and 7th order harmonics, which can become a significant problem at increased power levels. This problem can be solved by

employing an active PWM rectifier front end as shown in figure 1.1(b), which can be modulated to draw near sinusoidal input currents. This circuit, which is known as a back-to-back converter, has the added advantage that the power flow can be bi-directional. However the dc-link capacitors are still large and additional input inductors are required.




(a) Diode bridge rectifier and VSI (b) Back-to-back VSI

Figure 1.1: Common configurations of indirect ac-ac converters

An alternative ac-ac power converter topology is the matrix converter. The matrix converter, shown in figure 1.2, consists of an array of bi-directional switches where any input phase can be connected to any output phase. The duty cycle of the switches can be modulated to produce the desired average output amplitude and frequency. The matrix converter is also described as a direct ac-ac converter because it requires no intermediate energy storage.

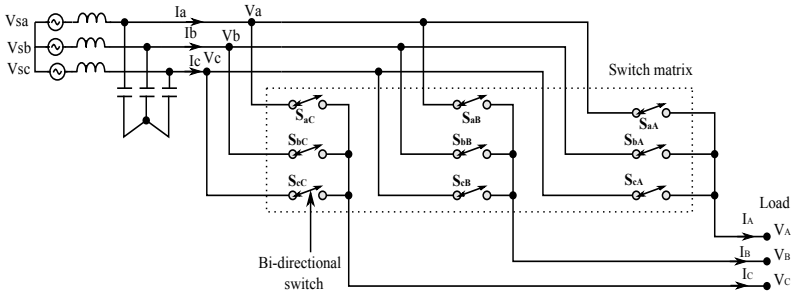



Figure 1.2: Matrix Converter

Much of the work on matrix converters over the past three decades have concentrated on modulation algorithms and, more recently, on the practical implementation issues; all of which have largely been solved. One of the key benefits of matrix converter technology is the possibility of greater power density due to the absence of a dc-link.

This is translated into a realistic advantage if the filter size is also optimised by having a sufficiently high switching frequency. This means, though, a compromise between filter size and semiconductor switching losses must be found [13].

Another approach for direct ac-ac power conversion is the two-stage matrix converter, shown in figure 1.3. The two-stage matrix converter is an indirect form of the matrix converter, providing similar input/output performances of the conventional matrix converter [14]. The two-stage matrix converter provides additional benefits in comparison to the conventional matrix converter such as reduced number of switches [15], possibility for cost effective multi-drive systems [16] and it can be a platform for more complex converter structures [17].

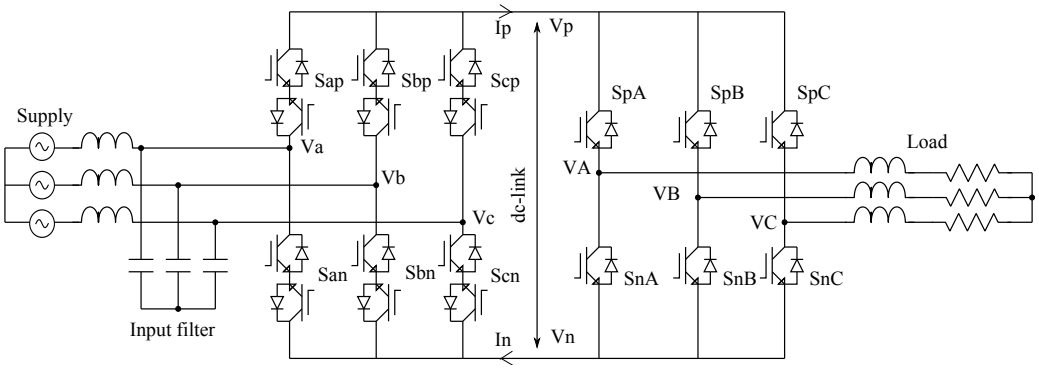



Figure 1.3: Two-stage Matrix Converter

However, matrix converter topologies have some limitations. They require a high number of power semiconductor devices and the maximum output voltage of the matrix converter is limited to 86.6% of the input voltage [18]. These limitations are mainly due to the fact that matrix converters do not use energy storage. Also, the waveform quality of a matrix converter can be directly affected by input side voltage disturbances such as unbalanced supply, sags, dips and harmonics.

Despite these drawbacks, the significant advantages of the matrix converter have encouraged extensive research into the implementation of the topology. Different techniques to maintain the load voltage quality and maximum voltage transfer ratio during input voltage disturbances have been investigated in the literature [19, 20, 21, 22].

## 1.3 The Z-source converter

The Z-source converter is a relatively recent converter topology that exhibits a voltage buck-boost capability. Figure 1.4 shows a voltage-type Z-source inverter. In a Z-source inverter, a symmetric lattice $LC$ filter is inserted between the dc-link and the dc voltage source. The Z-source inverter is able to boost or buck voltage in dc-ac inversion and able to develop variable voltage and frequency ac output voltages [23]. The voltage boost capability of the Z-source inverter is achieved by inserting shoot-through states in the inverter PWM switching pattern.

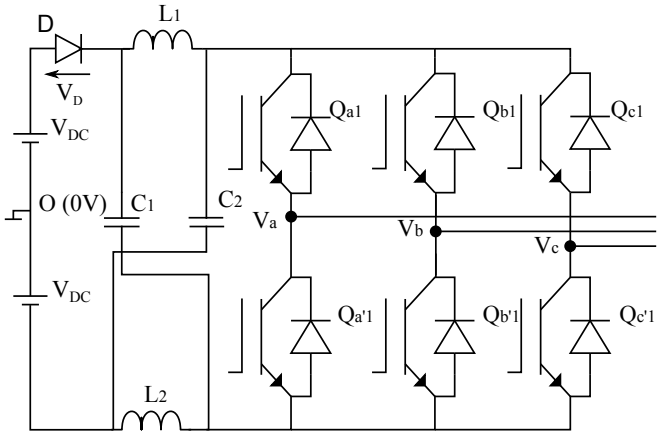



Figure 1.4: A Z-source Inverter

The advantages of the Z-source inverter are the increased reliability by allowing the shoot-through between upper and lower power switches on any phase leg and insensitivity to dc bus voltage variation due to the boost or buck voltage inversion [23].

### 1.3.1 Target application areas for Z-source converters

Z-source converters are especially useful for three-phase applications where the required line-to-line voltages for the loads are higher than the terminal voltages of the dc sources. Possible examples could be grid connected distribution generation systems based on renewable energy sources such as photovoltaic systems, wind turbines and fuel cell stacks [24]. Other examples include integrated starter alternator systems

for automotive applications and adjustable speed drive systems in applications such as conveyor belts, fans and water pumps [25].

## 1.4 Motivation and objectives of the project

The purpose of this work is to investigate two hybrid power converter topologies. In the first hybrid converter a Z-source network is inserted between a dc voltage source and the dc-link of a three-level NPC inverter to enable the use of a boost function. In the second hybrid converter approach a Z-source network is inserted in the virtual dc-link of a three-level, two-stage matrix converter in order to increase the voltage transfer ratio.

The main objectives of the project are:

i. investigate the Z-source concept to add boost capability to an NPC inverter;

ii. investigate the Z-source concept to improve the intrinsic maximum voltage transfer ratio limit of the three-level, two-stage matrix converter;

iii. achieve space vector modulation of these hybrid converters;

iv. validate the proposed modulation methods using a low power experimental prototype.

## 1.5 Thesis outline

The thesis is organised as follows.

In Chapter 2, a technology overview of the three-level, neutral-point-clamped voltage source inverter (NPC VSI) is given. The operating principles and space vector

modulation for the NPC VSI are reviewed in this chapter. The neutral-point balancing problem of the NPC VSI and the associated control methods are discussed. Finally, simulation results are presented to show the effectiveness of the NPC VSI in generating proper output waveforms and balancing the neutral-point voltage.

Chapter 3 gives an overview of the three-level, Z-source neutral-point-clamped inverter. The operating principles and space vector modulation for the Z-source NPC inverter are reviewed in this chapter. Simulation results are also presented to demonstrate the voltage buck-boost capabilities of the Z-source NPC inverter.

Chapter 4 presents the technology overview of the two-stage matrix converter. The chapter discusses, in detail, the principles of the bidirectional switch cell, current commutation, modulation techniques, design of input filter and circuit protection issues for the two-stage matrix converter. Simulation results are also presented to show the ability of the converter to generate sinusoidal input and output waveforms.

Chapter 5 discusses the operating principles and modulation strategy for the three-level, two-stage matrix converter. Simulation results are also presented.

Chapter 6 presents the operating principles and modulation strategy for the proposed three-level, Z-source hybrid direct ac-ac power converter. Simulation results are also presented to show the ability of the converter and to demonstrate the voltage buck-boost capability.

Chapter 7 presents the hardware implementation of the prototype three-level, Z-source hybrid direct ac-ac power converter. This chapter describes the overall structure of the prototype converter and explains the design of each circuit in detail.

Chapter 8 presents the experimental results obtained during experimental verification of the chosen SVM-based techniques presented in earlier chapters.

The thesis is concluded in Chapter 9 where possible future extensions of the work accomplished are also discussed.

# Chapter 2

# Three-Level Neutral Point Clamped Inverter

## 2.1 Introduction

This chapter gives a review of the neutral point clamped (NPC) inverter topology from operating principles to the related modulation strategies, which are well established in the literature. The neutral-point balancing problem of the NPC inverter and associated control methods are also discussed. This chapter will serve as the foundation for the modulation of the Z-source NPC inverter (Chapter 3), the three-level, two-stage matrix converter (Chapter 5) and the three-level, Z-source hybrid direct power converter (Chapter 6). The chapter will conclude with the simulation results for the NPC inverter, which prove the ability of the NPC inverter to generate multilevel outputs and the elimination of the neutral-point balancing problem by using the concept of virtual vectors.

## 2.2 Inverter configuration

Figure 2.1 shows the simplified circuit diagram of a three-level NPC inverter. Each inverter leg is composed of four active switches with anti-parallel diodes, $S_{1X}$ to $S_{4X}$. On the dc side of the inverter, the dc bus capacitor is split into two, providing a neutral point '$o$'. The diodes connected to the neutral point, $D_{X1}$ and $D_{X2}$, are the clamping diodes. When switches $S_{2X}$ and $S_{3X}$ are turned on, the appropriate inverter output terminal is connected to the neutral point through one of the clamping diodes. The voltage across each of the dc capacitors is $V_{DC}$, which is normally equal to half of the total dc voltage $V_{pn}$. With a finite value for $C_1$ and $C_2$, the capacitors can be charged or discharged with the neutral-point current $i_o$, potentially causing neutral-point voltage deviation.

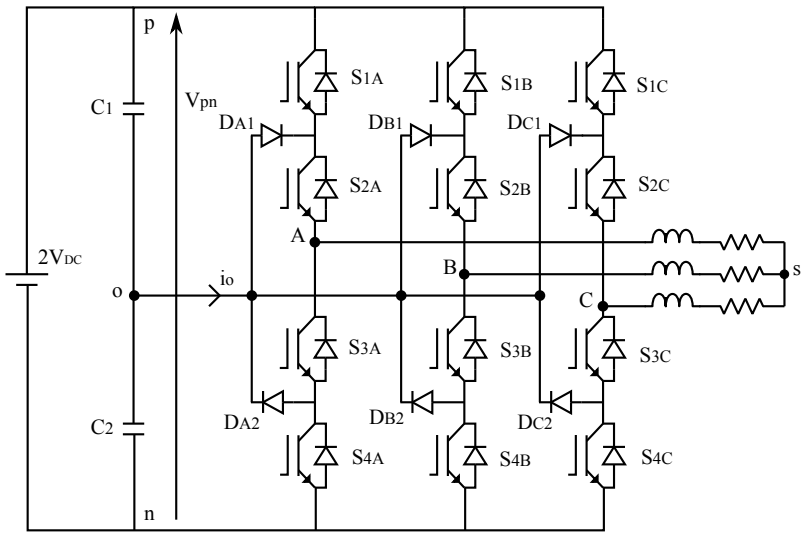



Figure 2.1: Three-level NPC inverter

In order to generate the three-level output, the switching devices in each phase leg are controlled according to the switching combinations shown in table 2.1. At any time, only two of the switching devices are turned on and the output terminal can be connected to any of the dc-link points ($p$, $o$ or $n$), which can be represented by a switching state (P, O, or N); for example switching state P represents the connection of the output terminal to the dc-link point '$p$'. Using the dc-link middle point '$o$' as the reference, the NPC inverter is able to generate three distinct voltage levels at the

output terminal of each phase leg, $V_{Xo}$, which can be determined by (2.1).

$$V_{Xo} = V_{DC} \cdot (m_{X1} - m_{X3}) \tag{2.1}$$

where $m_{X1}$ and $m_{X3}$ represent the switch combinations ($S_{1X}$ & $S_{2X}$) and ($S_{3X}$ & $S_{4X}$) in each phase leg ($X\epsilon$\{A,B,C\}), which is '1' when both switches in the combination are 'on' and '0' otherwise.

| $S_{1X}$ | $S_{2X}$ | $S_{3X}$ | $S_{4X}$ | $V_{Xo}$ | Switching state |
|---|---|---|---|---|---|
| ON | ON | OFF | OFF | $V_{DC}$ | P |
| OFF | ON | ON | OFF | 0 | O |
| OFF | OFF | ON | ON | $-V_{DC}$ | N |

Table 2.1: Switching combination in each phase leg of the NPC inverter ($X\epsilon$\{A,B,C\})

For a three-phase three-level NPC inverter, there are twenty-seven possible switching states that represent the connections of the output terminals ($A$, $B$ and $C$) to the dc-link points $p$, $o$, and $n$. Having a star-connected load applied to the NPC inverter, as illustrated in figure 2.1, these switching states are able to generate specific output phase (line-to-load neutral, $s$) and line-to-line voltages, as shown in table 2.2. The output phase voltages with respect to the load neutral, $s$, can be determined using (2.2) while the line-to-line voltages can be determined using (2.3).

$$\begin{aligned}
V_{As} &= \frac{2}{3} \cdot V_{DC} \cdot \{m_{A1} - m_{A3} - \frac{1}{2}[m_{B1} - m_{B3} + m_{C1} - m_{C3}]\} \\
V_{Bs} &= \frac{2}{3} \cdot V_{DC} \cdot \{m_{B1} - m_{B3} - \frac{1}{2}[m_{A1} - m_{A3} + m_{C1} - m_{C3}]\} \\
V_{Cs} &= \frac{2}{3} \cdot V_{DC} \cdot \{m_{C1} - m_{C3} - \frac{1}{2}[m_{A1} - m_{A3} + m_{B1} - m_{B3}]\}
\end{aligned} \tag{2.2}$$

Referring to table 2.2, the NPC inverter is able to produce five distinct voltage levels ($\pm\ 2V_{DC}$, $\pm\ V_{DC}$ and $0V$) for the output line-to-line voltages.

$$\begin{aligned}
V_{AB} &= V_{Ao} - V_{Bo} = V_{DC} \cdot [m_{A1} - m_{A3} + m_{B1} - m_{B3}] \\
V_{BC} &= V_{Bo} - V_{Co} = V_{DC} \cdot [m_{B1} - m_{B3} + m_{C1} - m_{C3}] \\
V_{CA} &= V_{Co} - V_{Ao} = V_{DC} \cdot [m_{C1} - m_{C3} + m_{A1} - m_{A3}]
\end{aligned} \tag{2.3}$$

| Switching states | | | Output phase voltages | | | Output line-to-line voltages | | |
|---|---|---|---|---|---|---|---|---|
| A | B | C | $V_{As}$ | $V_{Bs}$ | $V_{Cs}$ | $V_{AB}$ | $V_{BC}$ | $V_{CA}$ |
| P | P | P | 0 | 0 | 0 | 0 | 0 | 0 |
| O | O | O | 0 | 0 | 0 | 0 | 0 | 0 |
| N | N | N | 0 | 0 | 0 | 0 | 0 | 0 |
| P | O | O | $\frac{2}{3}\cdot V_{DC}$ | $-\frac{1}{3}\cdot V_{DC}$ | $-\frac{1}{3}\cdot V_{DC}$ | $V_{DC}$ | 0 | $-V_{DC}$ |
| O | P | O | $-\frac{1}{3}\cdot V_{DC}$ | $\frac{2}{3}\cdot V_{DC}$ | $-\frac{1}{3}\cdot V_{DC}$ | $-V_{DC}$ | $V_{DC}$ | 0 |
| O | O | P | $-\frac{1}{3}\cdot V_{DC}$ | $-\frac{1}{3}\cdot V_{DC}$ | $\frac{2}{3}\cdot V_{DC}$ | 0 | $-V_{DC}$ | $V_{DC}$ |
| P | P | O | $\frac{1}{3}\cdot V_{DC}$ | $\frac{1}{3}\cdot V_{DC}$ | $-\frac{2}{3}\cdot V_{DC}$ | 0 | $V_{DC}$ | $-V_{DC}$ |
| O | P | P | $-\frac{2}{3}\cdot V_{DC}$ | $\frac{1}{3}\cdot V_{DC}$ | $\frac{1}{3}\cdot V_{DC}$ | $-V_{DC}$ | 0 | $V_{DC}$ |
| P | O | P | $\frac{1}{3}\cdot V_{DC}$ | $-\frac{2}{3}\cdot V_{DC}$ | $\frac{1}{3}\cdot V_{DC}$ | $V_{DC}$ | $-V_{DC}$ | 0 |
| N | O | O | $-\frac{2}{3}\cdot V_{DC}$ | $\frac{1}{3}\cdot V_{DC}$ | $\frac{1}{3}\cdot V_{DC}$ | $-V_{DC}$ | 0 | $V_{DC}$ |
| O | N | O | $\frac{1}{3}\cdot V_{DC}$ | $-\frac{2}{3}\cdot V_{DC}$ | $\frac{1}{3}\cdot V_{DC}$ | $V_{DC}$ | $-V_{DC}$ | 0 |
| O | O | N | $\frac{1}{3}\cdot V_{DC}$ | $\frac{1}{3}\cdot V_{DC}$ | $-\frac{2}{3}\cdot V_{DC}$ | 0 | $V_{DC}$ | $-V_{DC}$ |
| N | N | O | $-\frac{1}{3}\cdot V_{DC}$ | $-\frac{1}{3}\cdot V_{DC}$ | $\frac{2}{3}\cdot V_{DC}$ | 0 | $-V_{DC}$ | $V_{DC}$ |
| O | N | N | $\frac{2}{3}\cdot V_{DC}$ | $-\frac{1}{3}\cdot V_{DC}$ | $-\frac{1}{3}\cdot V_{DC}$ | $V_{DC}$ | 0 | $-V_{DC}$ |
| N | O | N | $-\frac{1}{3}\cdot V_{DC}$ | $\frac{2}{3}\cdot V_{DC}$ | $-\frac{1}{3}\cdot V_{DC}$ | $-V_{DC}$ | $V_{DC}$ | 0 |
| P | N | N | $\frac{4}{3}\cdot V_{DC}$ | $-\frac{2}{3}\cdot V_{DC}$ | $-\frac{2}{3}\cdot V_{DC}$ | $2\cdot V_{DC}$ | 0 | $-2\cdot V_{DC}$ |
| P | P | N | $\frac{2}{3}\cdot V_{DC}$ | $\frac{2}{3}\cdot V_{DC}$ | $-\frac{4}{3}\cdot V_{DC}$ | 0 | $2\cdot V_{DC}$ | $-2\cdot V_{DC}$ |
| N | P | P | $-\frac{4}{3}\cdot V_{DC}$ | $\frac{2}{3}\cdot V_{DC}$ | $\frac{2}{3}\cdot V_{DC}$ | $-2\cdot V_{DC}$ | 0 | $2\cdot V_{DC}$ |
| N | N | P | $-\frac{2}{3}\cdot V_{DC}$ | $-\frac{2}{3}\cdot V_{DC}$ | $\frac{4}{3}\cdot V_{DC}$ | 0 | $-2\cdot V_{DC}$ | $2\cdot V_{DC}$ |
| P | N | P | $\frac{2}{3}\cdot V_{DC}$ | $-\frac{4}{3}\cdot V_{DC}$ | $\frac{2}{3}\cdot V_{DC}$ | $2\cdot V_{DC}$ | $-2\cdot V_{DC}$ | 0 |
| N | P | N | $-\frac{2}{3}\cdot V_{DC}$ | $\frac{4}{3}\cdot V_{DC}$ | $-\frac{2}{3}\cdot V_{DC}$ | $-2\cdot V_{DC}$ | $2\cdot V_{DC}$ | 0 |
| P | O | N | $V_{DC}$ | 0 | $-V_{DC}$ | $V_{DC}$ | $V_{DC}$ | $-2\cdot V_{DC}$ |
| O | P | N | 0 | $V_{DC}$ | $-V_{DC}$ | $-V_{DC}$ | $2\cdot V_{DC}$ | $-V_{DC}$ |
| N | P | O | $-V_{DC}$ | $V_{DC}$ | 0 | $-2\cdot V_{DC}$ | $V_{DC}$ | $V_{DC}$ |
| N | O | P | $-V_{DC}$ | 0 | $V_{DC}$ | $-V_{DC}$ | $-V_{DC}$ | $2\cdot V_{DC}$ |
| P | N | O | $-V_{DC}$ | $V_{DC}$ | 0 | $2\cdot V_{DC}$ | $-V_{DC}$ | $-V_{DC}$ |
| O | N | P | 0 | $-V_{DC}$ | $V_{DC}$ | $V_{DC}$ | $-2\cdot V_{DC}$ | $V_{DC}$ |

Table 2.2: Switching states for the three-phase NPC inverter

## 2.3 State of the art in modulation strategies

The scope of this chapter is limited to the three-level NPC converter shown in figure 2.1. It focuses on the use of this topology in applications allowing high switching frequency pulse-width modulation (PWM).

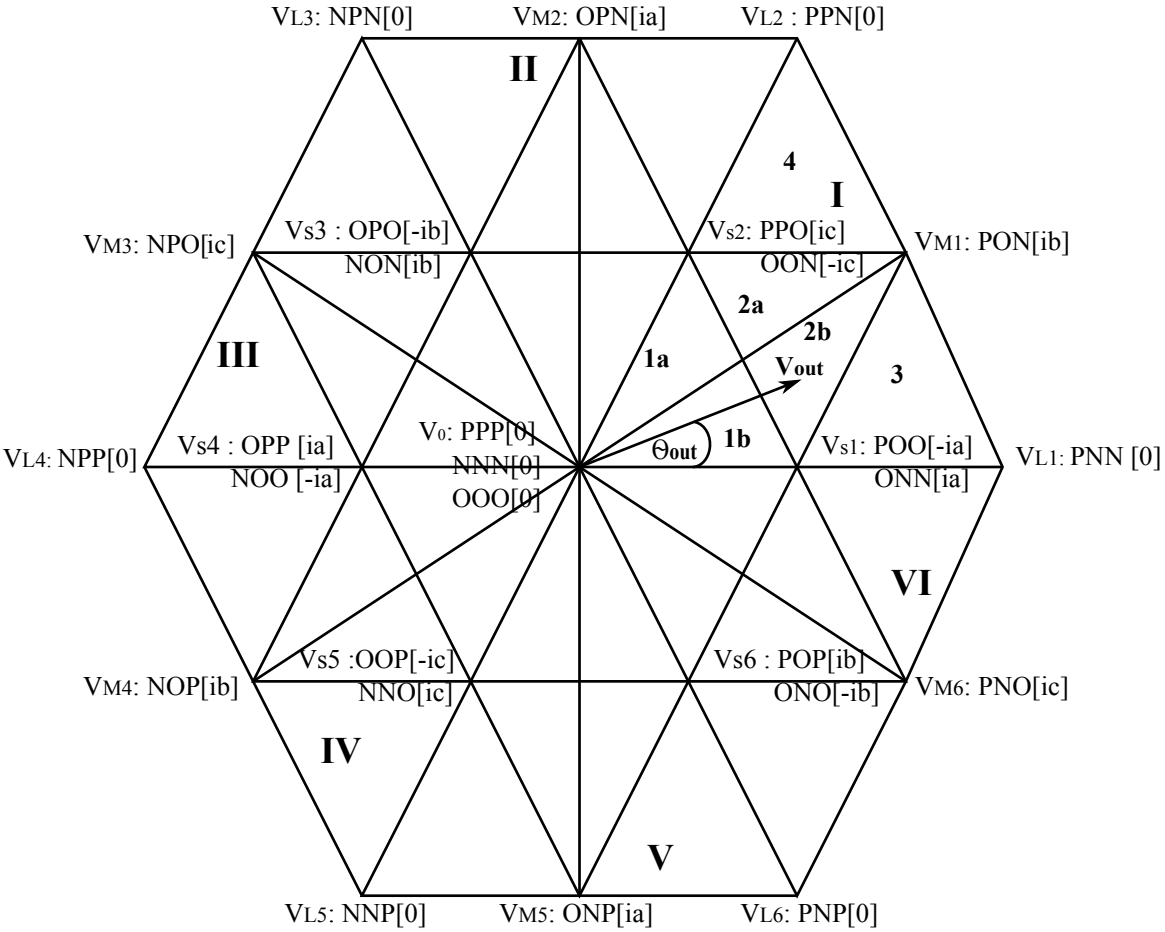



Figure 2.2: Space vector diagram of the NPC inverter with NPC leg states and associated neutral-point current, $i_o$.

There have been many studies with regard to the different possible modulation strategies suitable for this converter [26, 27, 28, 29, 30, 31, 32, 33, 34, 35, 36, 37, 38, 39, 40, 41, 42, 43, 44, 45, 46, 47, 48, 49, 50, 51, 52, 53, 54, 55, 56, 57, 58, 59, 60, 61]. The proposed strategies can be classified into two groups, according to their different implementation:

- Carrier-based modulation, where a modulating signal is compared to two triangular carrier waveforms.
- Space-vector-modulation (SVM), where the modulation is defined from a vectorial representation of the available converter switching states.

In fact, as discussed in [48], for any carrier-based modulation there is an equivalent SVM and vice versa. Therefore, in the following, the discussion of the different modulation methods appearing in the literature will be presented, for simplicity, with reference to the converter space vector diagram shown in figure 2.2.

The three-level NPC converter has twenty-seven valid switching states corresponding to all the combinations of connections of each phase to the dc-link points $p$, $n$ and $o$. These switching states define nineteen space vectors in the diagram of figure 2.2, classified as zero ($V_0$), small ($V_{Si}$), medium ($V_{Mi}$), and large ($V_{Li}$), where $i = 1, 2, ...6$. The rotating reference vector, $\vec{V}_{out}$, represents the desired three-phase output voltage. It is synthesized in each switching cycle by a sequence of converter voltage space vectors such that the product of the reference vector and the sampling period equals the sum of the voltage multiplied by the time interval of the chosen space vectors. For instance, if the tip of $\vec{V}_{out}$ is in triangle 3, $V_{S1}$, $V_{M1}$ and $V_{L1}$ are chosen. Therefore,

$$\begin{aligned} d_{V_{S1}} \cdot V_{S1} + d_{V_{M1}} \cdot V_{M1} + d_{V_{L1}} \cdot V_{L1} &= \vec{V}_{out} \\ d_{V_{S1}} + d_{V_{M1}} + d_{V_{L1}} &= 1 \end{aligned} \tag{2.4}$$

where $0 \leq d_{V_{S1}}, d_{V_{M1}}, d_{V_{L1}} \leq 1$ are the duty-ratios of vectors $V_{S1}$, $V_{M1}$, and $V_{L1}$, respectively in the particular switching cycle analysed. Whenever a vector can be generated by more than one switching state, an additional selection of one switching state or a combination of several has to be made. This is the case for the zero and small vectors. Finally, the sequence over time of the application of the selected converter switching states has to be decided for every switching cycle.

To define a modulation strategy, we need to select, for every possible modulation index $m_I$ and for every switching cycle within one line-cycle of the reference vector $\vec{V}_{out}$, the voltage vectors we will use to synthesize $\vec{V}_{out}$, the switching states we will

use to produce those voltage vectors, and the sequence over time of the selected switching states. With this noted, it is clear that there are a large number of possible modulation strategies.

Several modulation options have been explored. Most of them, both carrier-based and SVM-based, select the nearest-three vectors (NTV) for every position of the reference vector. This typically guarantees a lower output-voltage harmonic distortion compared to other alternatives. Modulation solutions have been proposed in order to avoid narrow on and off pulses for the controlled devices [29, 34, 36, 53]; minimize the converter losses [37, 48, 53, 56]; minimize the output-voltage harmonic distortion [38, 46, 61]; and solve the neutral-point voltage balancing problem [26, 27, 28, 32, 33, 39, 40, 41, 42, 43, 44, 45, 47, 48, 50, 51, 52, 53, 54, 55, 56, 57, 60].

The narrow pulse problem is mainly relevant when gate turn-off thyristors (GTOs) are used. With the development of the insulated gate bipolar transistor (IGBT) technology in the past few years, providing devices with higher voltage ratings, this problem has become less significant. The minimisation of the converter losses is achieved by reducing the number of switching states applied per switching cycle and particularly avoiding those switching the phase carrying the highest current.

To characterise the output harmonic distortion and aid in the definition of modulation strategies, a novel figure, the harmonic distortion factor (HDF), based on a per switching-cycle evaluation of the harmonic flux, has been proposed [46]. However, while this figure provides a measure of the total harmonic distortion (THD), it does not provide any insight into the distribution of harmonic levels within the output voltage spectra. There is also no explicit expression to compute the output voltage THD as a function of HDF.

Finally, a large number of contributions have concentrated on studying and solving an inherent problem in multilevel diode-clamped topologies: the balancing of the dc-link capacitor voltages. Correct operation of the three-level NPC converter requires that the neutral-point voltage $v_o$ must be the average of the positive and negative

voltages: $v_p$ and $v_n$. This is equivalent to say that the voltage across both dc-link capacitors ($C_1$ and $C_2$) must be the same. This ensures that the voltage stress that all semiconductors must withstand is the same, uniformly spreading the switching losses and improving the reliability.

Let us define the dc-link capacitor voltage unbalance as the difference between the capacitor voltages and the corresponding balanced value. On one hand, some authors study the response of the converter when having an unbalance in the line-cycle-average voltage across the dc-link capacitors [26, 27, 40, 41, 42, 47, 48, 51, 53, 54]. They investigate the inherent stability of the converter dc-link balance as a function of the modulation strategy and load, and propose a closed-loop control affecting the zero component of the output three-phase voltages [26, 27, 40] and other methods [41, 51] to eliminate those unbalances. As explained in [51] and [54], except for cases where the load introduces even and non-multiple of third harmonic currents, the line-cycle-average unbalance is typically corrected naturally without the addition of any closed-loop control. The addition of such types of control, however, helps speed-up the process of recovering the line-cycle-average voltage balance of the dc-link capacitors.

On the other hand, if conventional converter modulation strategies are applied to the three-level converter, a low-frequency (three times the fundamental frequency of the output voltage) oscillation of the capacitor voltages $v_{C1}$ and $v_{C2}$ occur. The neutral-point voltage oscillation increases the voltage stress on the devices. It also generates harmonics around the sixth-order harmonic in the output voltage.The resulting load current also presents this low-frequency distortion. Other load power factors may even increase the dc-link unbalance. A simple solution to this problem would be to increase the dc-link capacitors $C_1$ and $C_2$. However, in general, a significant increase in capacitance is required to satisfactorily suppress the low-frequency voltage oscillation, which not only means a significant increase in converter volume and cost but also a reduction in converter control bandwidth in applications where the system connected to the dc side behaves as a current source. Therefore, efforts have been directed towards solving this problem through defining an appropriate modulation pattern [32, 33, 39, 42, 44, 45, 52, 60].

The neutral-point voltage balancing problem arises from the existence of a non-zero neutral-point current $i_o$. Each converter switching state in figure 2.2 causes a particular neutral-point current, $i_o$. These are specified in brackets in the diagram of figure 2.2. The switching states corresponding to the zero and large vectors introduce a current $i_o$ equal to zero. The two switching states associated with a small vector introduce a current equal to a phase current but opposite in sign. Finally, the switching states producing medium vectors introduce an $i_o$ equal to a phase current different from the phase currents introduced by neighbouring small vectors.

The objective is to define a modulation strategy such that the average $i_o$ in every switching cycle equals zero. Most of the modulation solutions appearing in the literature select the NTV to synthesize the reference vector and then choose an appropriate combination of switching states for the small vectors in order to guarantee that the average $i_o$ equals zero or to obtain a non-zero average $i_o$ in order to correct any pre-existing unbalance. However, these solutions are unable to maintain the dc-link voltage balance for high modulation indices and low power factors as demonstrated in [45]. The reason is that the neutral-point current introduced by the medium vectors cannot be always fully compensated, in NTV modulation strategies by distributing the small vectors' duty ratio into the two associated switching states. This problem has led some authors to introduce additional switching networks to guarantee the neutral-point voltage balancing [41, 50]. Other authors [32, 39] propose modulation solutions eliminating the use of medium vectors. However, these modulation strategies unnecessarily increase the output-voltage high-frequency distortion.

## 2.4 Space vector modulation

Space vector modulation is a PWM strategy that uses the concept of space vectors to compute the duty cycles of the switches. As indicated earlier, the operation of each inverter phase leg of a traditional NPC inverter can be represented by three switching states P, O, and N. Taking all three phases into account, the converter has a total

of twenty-seven valid switching states. These twenty-seven possible switching states define nineteen space vectors as shown in figure 2.2. The rotating reference vector $\vec{V}_{out}$ represents the desired three-phase output voltage.

### 2.4.1 Nearest three vector SVM

In NTV SVM strategies, the nearest three space vectors are selected to synthesize the reference vector [29, 34, 45, 52, 61, 53]. Assuming that the operation of the converter is three-phase balanced and not considering converter harmonics, we have

$$V_{As}(t) + V_{Bs}(t) + V_{Cs}(t) = 0 \tag{2.5}$$

where $V_{As}(t)$, $V_{Bs}(t)$ and $V_{Cs}(t)$ are the instantaneous phase to load neutral voltages. From mathematical point of view, one phase voltage is redundant since given any two phase voltages, the third one can be readily calculated. This interdependence can be relaxed by transforming to a two-dimensional space using (2.6).

$$\begin{bmatrix} V_\alpha(t) \\ V_\beta(t) \end{bmatrix} = \frac{2}{3} \begin{bmatrix} 1 & -\frac{1}{2} & -\frac{1}{2} \\ 0 & \frac{\sqrt{3}}{2} & -\frac{\sqrt{3}}{2} \end{bmatrix} \begin{bmatrix} V_{As}(t) \\ V_{Bs}(t) \\ V_{Cs}(t) \end{bmatrix} \tag{2.6}$$

A space vector can be generally expressed in terms of the two-phase voltages in the $\alpha - \beta$ plane

$$\vec{V}_{out}(t) = V_\alpha(t) + jV_\beta(t) \tag{2.7}$$

Substituting (2.6) into (2.7), we have

$$\vec{V}_{out}(t) = \frac{2}{3}\left[V_{As}(t)e^{j0} + V_{Bs}(t)e^{j2\pi/3} + V_{Cs}(t)e^{j4\pi/3}\right] \tag{2.8}$$

where $e^{jx} = \cos(\mathrm{x}) + \mathrm{jsin(x)}$ and $x = 0, 2\pi/3$ or $4\pi/3$.

All the switching state combinations listed in table 2.2 can be transformed into nineteen space vectors with fixed directions, as shown in table 2.3.

| Switching states | | | Output voltage vectors | | |
|---|---|---|---|---|---|
| A | B | C | Vector | Magnitude | Angle |
| P | P | P | $V_0$ | 0V | 0 |
| O | O | O | | | |
| N | N | N | | | |
| P | O | O | $V_{S1}$ | $\frac{2}{3} \cdot V_{DC}$ | 0 |
| O | N | N | | | |
| P | N | N | $V_{L1}$ | $\frac{4}{3} \cdot V_{DC}$ | 0 |
| P | O | N | $V_{M1}$ | $\frac{2}{\sqrt{3}} \cdot V_{DC}$ | $\pi/6$ |
| P | P | O | $V_{S2}$ | $\frac{2}{3} \cdot V_{DC}$ | $\pi/3$ |
| O | O | N | | | |
| P | P | N | $V_{L2}$ | $\frac{4}{3} \cdot V_{DC}$ | $\pi/3$ |
| P | O | N | $V_{M2}$ | $\frac{2}{\sqrt{3}} \cdot V_{DC}$ | $\pi/2$ |
| O | P | O | $V_{S3}$ | $\frac{2}{3} \cdot V_{DC}$ | $2\pi/3$ |
| N | O | N | | | |
| N | P | N | $V_{L3}$ | $\frac{4}{3} \cdot V_{DC}$ | $2\pi/3$ |
| N | P | O | $V_{M3}$ | $\frac{2}{\sqrt{3}} \cdot V_{DC}$ | $5\pi/6$ |
| O | P | P | $V_{S4}$ | $\frac{2}{3} \cdot V_{DC}$ | $\pi$ |
| N | O | O | | | |
| N | P | P | $V_{L4}$ | $\frac{4}{3} \cdot V_{DC}$ | $\pi$ |
| N | O | P | $V_{M4}$ | $\frac{2}{\sqrt{3}} \cdot V_{DC}$ | $-5\pi/6$ |
| O | O | P | $V_{S5}$ | $\frac{2}{3} \cdot V_{DC}$ | $-2\pi/3$ |
| N | N | O | | | |
| N | N | P | $V_{L5}$ | $\frac{4}{3} \cdot V_{DC}$ | $-2\pi/3$ |
| O | N | P | $V_{M5}$ | $\frac{2}{\sqrt{3}} \cdot V_{DC}$ | $5\pi/6$ |
| P | O | P | $V_{S6}$ | $\frac{2}{3} \cdot V_{DC}$ | $-\pi/3$ |
| O | N | O | | | |
| P | N | P | $V_{L6}$ | $\frac{4}{3} \cdot V_{DC}$ | $-\pi/3$ |
| P | N | O | $V_{M6}$ | $\frac{2}{\sqrt{3}} \cdot V_{DC}$ | $-\pi/6$ |

Table 2.3: The magnitude and angle of each voltage space vector formed by the switching states of the NPC inverter using the space vector transformation

#### 2.4.1.1 Calculation of duty cycles

Figure 2.3 shows the space vector diagram for sector I. The SVM for the NPC inverter is based on "volt-second balancing" principle; that is, the product of the reference voltage $\vec{V}_{out}$ and sampling period $T_{sw}$ equals the sum of the voltage multiplied by the time interval of chosen space vectors. The reference vector $\vec{V}_{out}$ can be synthesized by three nearest stationary vectors.

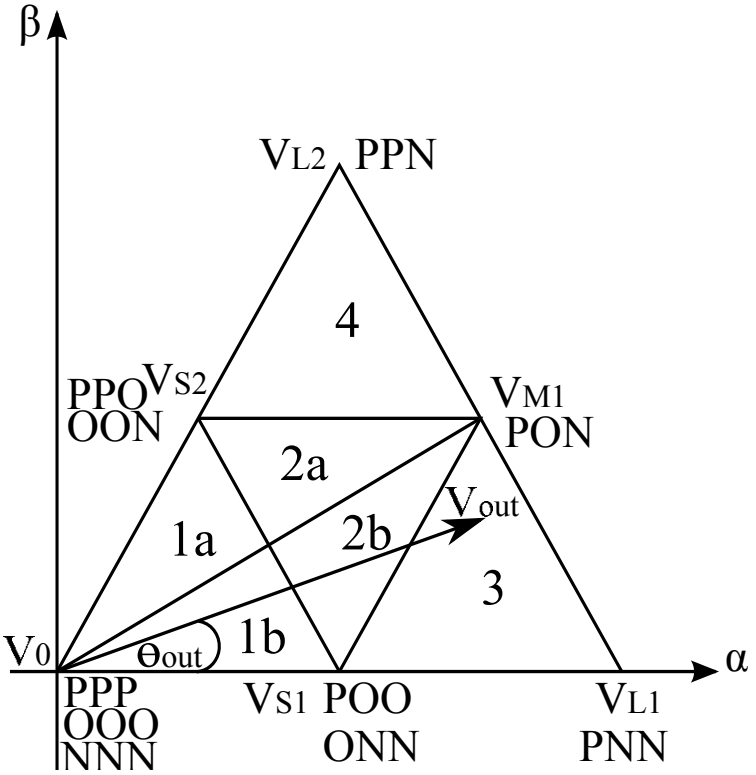



Figure 2.3: Space vector diagram for sector I of a three-level NPC inverter

For instance, when $\vec{V}_{out}$ falls into triangle 3 the nearest three vectors are $V_{S1}$, $V_{M1}$ and $V_{L1}$, from which

$$\begin{aligned} d_{V_{S1}} \cdot V_{S1} + d_{V_{M1}} \cdot V_{M1} + d_{V_{L1}} \cdot V_{L1} &= \vec{V}_{out} \\ d_{V_{S1}} + d_{V_{M1}} + d_{V_{L1}} &= 1 \end{aligned} \tag{2.9}$$

where $d_{V_{S1}}$, $d_{V_{M1}}$,$d_{V_{L1}}$ are the duty-ratios of vectors $V_{S1}$, $V_{M1}$, and $V_{L1}$, respectively in the particular switching cycle analysed. It must be noted that $\vec{V}_{out}$ can also be synthesized by other space vectors instead of the "nearest three". However, it will

cause higher harmonic distortion in the inverter output voltage, which is undesirable in most cases. The voltage vectors $V_{S1}$, $V_{M1}$, $V_{L1}$ and $\vec{V}_{out}$ in figure 2.2 can be expressed as:

$$\begin{aligned} \vec{V}_{S1} &= \frac{1}{3} \cdot (2V_{DC}) \\ \vec{V}_{M1} &= \frac{\sqrt{3}}{3} \cdot e^{j\pi/6} \cdot (2V_{DC}) \\ \vec{V}_{L1} &= \frac{2}{3} \cdot (2V_{DC}) \\ \vec{V}_{out} &= V_{out} \cdot e^{j\theta_{out}} \end{aligned} \tag{2.10}$$

Substituting (2.10) into (2.9), the duty ratios of the nearest three voltage vectors are given by:

$$\begin{aligned} d_{V_{S1}} &= 2 - 2m_I \sin(\pi/3 + \theta_{out}) \\ d_{V_{M1}} &= 2m_I \sin(\theta_{out}) \\ d_{V_{L1}} &= 2m_I \sin(\pi/3 - \theta_{out}) - 1 \end{aligned} \tag{2.11}$$

where $m_I$ is the modulation index and $\theta_{out}$ is the angle of the reference vector within the sector. A similar procedure is used to derive the duty ratios of the selected voltage vectors for the other triangles.

#### 2.4.1.2 Switching sequences

To complete the modulation process, the selected voltage vectors are applied to the output according to a particular switching sequence. Ideally, a switching sequence is formed in such a way that a high quality output waveform is obtained with minimum number of switching transitions. Whenever a vector can be generated by more than one switching state, an additional selection of one switching state or a combination of several has to be made. This is the case for the zero and small vectors and forms the basis of the dc-link capacitor voltage balancing technique for SVM. It must be noted that there are other switching sequences that can be used depending on the SVM algorithm adopted such as radial-state SVM and zero common-mode voltage SVM [62].

The sequence over time of the application of the selected converter switching states has to be decided for every switching cycle. For example in triangle 3 the voltage vectors $V_{S1}$, $V_{M1}$ and $V_{L1}$ are selected to synthesize the reference vector $\vec{V}_{out}$ so we use the switching sequence ONN $\rightarrow$ PNN $\rightarrow$ PON $\rightarrow$ POO.

In the following section, the neutral-point balancing problem of the NPC inverter and associated control methods are reviewed.

### 2.4.2 Nearest three virtual vector (NTVV) SVM

In this section the NTVV SVM is reviewed. This modulation strategy is capable of controlling the neutral-point voltage over the full range of converter output voltage, for any load (linear or non-linear), and for all load power factors. This solution was originally proposed in [63].

#### 2.4.2.1 Definition of virtual space vectors

In a conventional NTV technique the reference vector, $\vec{V}_{out}$, is synthesized in each switching cycle by a sequence of the nearest three vectors. Whenever a vector can be generated by more than one switching state, an additional selection of one switching state or a combination of several has to be made. This is the case for the zero and small vectors.

The neutral-point current corresponding to each switching state is specified in brackets in figure 2.2. As noted earlier [45], the average neutral-point current, $i_o$, in a switching cycle must be zero to avoid a noticeable variation of the neutral-point voltage. The appropriate combination of switching states must be selected for the small vectors in order to achieve this goal, but as shown in [45], this is not possible when the modulation index $m_I$ is high and for low power factors. This is due to the fact that in these conditions, the neutral-point current introduced by the medium vectors

can not be fully compensated by the neutral-point current introduced by the small vectors.

To achieve full control of the neutral-point voltage, a set of new virtual vectors is defined as a linear combination of the vectors corresponding to certain switching states [63]. The new virtual vectors ($V_{V0}$, $V_{VSi}$, $V_{VMi}$, and $V_{VLi}$), where $i = 1, 2, ...6$, shown in figure 2.4 for the first sector of the space vector diagram shown in figure 2.2, have an associated average current, $i_o$, in each switching cycle equal to zero.

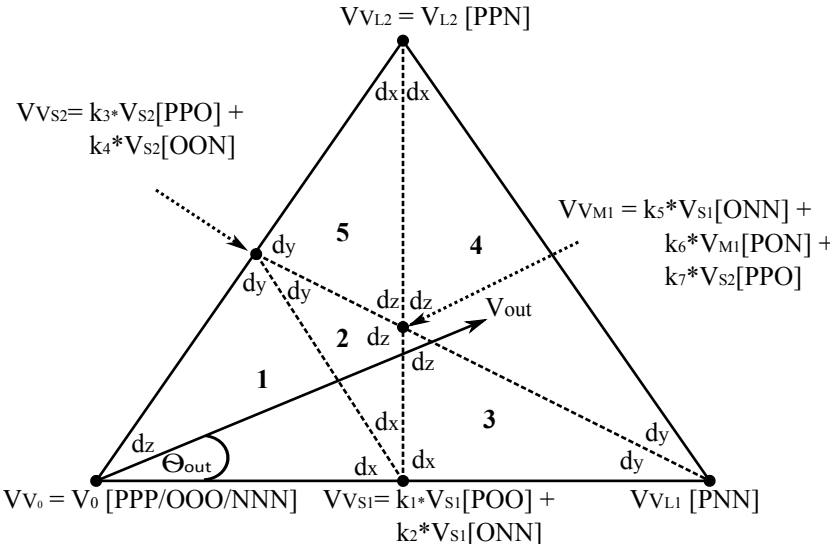



Figure 2.4: Virtual space vectors for the first sector of the SVD

- $V_{V0}$ is formed with $V_0$, which obviously generates a neutral-point current, $i_o$, equal to zero because all output terminals are connected to an identical dc-link point, so there is no current flowing in the dc-link capacitors.

- $V_{VSi}$ are obtained from an equal combination of two switching states having the same associated $i_o$ but opposite in sign. For example, if vector $V_{VS1}$ is selected for a period of time $t_{VS}$, switching state ONN will be active for $(\frac{1}{2}) \cdot t_{VS}$, and POO will be active for the remaining $(\frac{1}{2}) \cdot t_{VS}$. Therefore, the average $i_o$ in $t_{VS}$ will be:

$$\frac{1}{t_{VS}} \cdot \{\frac{1}{2} \cdot t_{VS} \cdot i_a + \frac{1}{2} \cdot t_{VS} \cdot (-i_a)\} = 0$$

- $V_{VMi}$ are obtained from an equal combination of three switching states having an associated $i_o$ equal to $i_a$, $i_b$ and $i_c$, respectively, and $i_a + i_b + i_c = 0$. For instance, if vector $V_{VM1}$ is selected for a period of time $t_{VM}$, switching state ONN will be active for $(\frac{1}{3}) \cdot t_{VM}$, PON will be active for $(\frac{1}{3}) \cdot t_{VM}$, and PPO will be active for $(\frac{1}{3}) \cdot t_{VM}$. Therefore, the average $i_o$ in $t_{VM}$ will be:

$$\frac{1}{t_{VM}} \cdot \{\frac{1}{3} \cdot t_{VM} \cdot i_a + \frac{1}{3} \cdot t_{VM} \cdot i_b + \frac{1}{3} \cdot t_{VM} \cdot i_c\} = 0$$

- $V_{VLi}$ are obtained from the switching states that define $V_{Li}$, all of them having an associated $i_o$ equal to zero.

#### 2.4.2.2 Selection of virtual space vectors

The synthesis of the reference vector in each switching cycle is performed using the nearest three virtual vectors. This defines five small triangular ($\Delta$) regions in the diagram of figure 2.4 where the constants $k_1 = k_2 = k_3 = k_4 = 1/2$ and $k_5 = k_6 = k_7 = 1/3$. The selected virtual vectors in the cases where the tip of $\vec{V}_{out}$ is in triangles 1 to 5 are specified in table 2.4.

| $\Delta$ | Selected virtual vectors |
|---|---|
| 1 | $V_{V0}$, $V_{VS1}$, $V_{VS2}$ |
| 2 | $V_{VS1}$, $V_{VS2}$, $V_{VM1}$ |
| 3 | $V_{VS1}$, $V_{VM1}$, $V_{VL1}$ |
| 4 | $V_{VL1}$, $V_{VM1}$, $V_{VL2}$ |
| 5 | $V_{VS2}$, $V_{VM1}$, $V_{VL2}$ |

Table 2.4: Selection of virtual vectors for each triangular region

The duty cycle of each selected vector in each switching cycle is calculated as:

$$\begin{aligned} d_{VV1} \cdot VV_1 + d_{VV2} \cdot VV_2 + d_{VV3} \cdot VV_3 &= \vec{V}_{out} \\ d_{VV1} + d_{VV2} + d_{VV3} &= 1 \end{aligned} \tag{2.12}$$

where $V_{Vj}$ corresponds to the $j^{th}$ selected virtual vector $\{j = 1, 2, 3\}$.

The corresponding duty cycles of the different switching states can then be calculated. Table 2.5 presents the duty cycle equations for the selected virtual vectors in each triangle, where $m_I$ is the modulation index of the NPC inverter and $\theta_{out}$ is the angle of the reference vector, $\vec{V}_{out}$, within the sector.

| $\Delta$ | $d_x$ | $d_y$ | $d_z$ |
|---|---|---|---|
| 1 | $m_I[\sqrt{3}\cos\theta_{out} - \sin\theta_{out}]$ | $2m_I \sin\theta_{out}$ | $1 - m_I[\sqrt{3}\cos\theta_{out} + \sin\theta_{out}]$ |
| 2 | $2 - m_I[\sqrt{3}\cos\theta_{out} + 3\sin\theta_{out}]$ | $2 - 2\sqrt{3}m_I \cos\theta_{out}$ | $3m_I[\sqrt{3}\cos\theta_{out} + \sin\theta_{out}] - 3$ |
| 3 | $2 - m_I[\sqrt{3}\cos\theta_{out} + 3\sin\theta_{out}]$ | $\sqrt{3}m_I \cos\theta_{out} - 1$ | $3m_I\sqrt{3}\sin\theta_{out}$ |
| 4 | $0.5m_I[\sqrt{3}\cos\theta_{out}+3\sin\theta_{out}]-1$ | $2 - 2\sqrt{3}m_I \cos\theta_{out}$ | $1.5m_I[\sqrt{3}\cos\theta_{out} - \sin\theta_{out}]$ |
| 5 | $0.5m_I[\sqrt{3}\cos\theta_{out}+3\sin\theta_{out}]-1$ | $\sqrt{3}m_I \cos\theta_{out} - 1$ | $3-1.5m_I[\sqrt{3}\cos\theta_{out}+\sin\theta_{out}]$ |

Table 2.5: Duty cycle equations for the selected virtual vectors in each triangle

#### 2.4.2.3 Switching states sequence

Finally, the sequence over time within a switching cycle of the application of the different switching states has to be decided. The chosen switching states' order is such that the sequence of connection of each phase to the dc-link points ($p$, $o$ or $n$) is the symmetrical *p-o-n-o-p*.

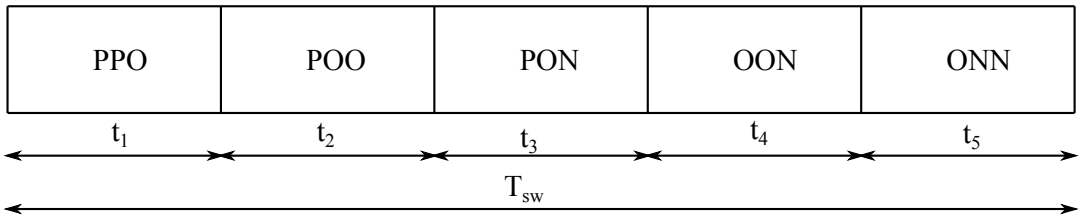



Figure 2.5: The NTVV switching pattern for the case where $\vec{V}_{out}$ is located in triangle 2 of sector I

As an example, in triangle 2 of sector I, the virtual vectors $V_{VS1}$, $V_{VS2}$, and $V_{VM1}$ are selected to synthesize the reference vector. Based on the NTVV technique, these virtual vectors are formed with the voltage vectors: $V_{S1}$ (PPO/OON), $V_{S2}$ (POO/ONN) and $V_{M1}$ (PON). These voltage vectors are applied to the output according to the switching sequence: PPO $\rightarrow$ POO $\rightarrow$ PON $\rightarrow$ OON $\rightarrow$ ONN. For a switching period, $T_{sw}$, the active time of each voltage vector in this switching sequence is determined

using (2.13). In order to reduce the output harmonic content, the switching sequence is reversed in the next switching cycle so that a double-sided switching sequence is formed. Figure 2.5 illustrates the switching sequence during the first switching cycle. A similar procedure can be applied to all the other triangles shown in the vector diagram of figure 2.4. Table A.1 lists all the switching sequences for triangles 1 to 5 in all the six sectors.

$$\begin{aligned} t_1 &= \frac{1}{3} \cdot d_{VM1} \cdot T_{sw} + \frac{1}{2} \cdot d_{VS2} \cdot T_{sw} \\ t_2 &= \frac{1}{2} \cdot d_{VS1} \cdot T_{sw} \\ t_3 &= \frac{1}{3} \cdot d_{VM1} \cdot T_{sw} \\ t_4 &= \frac{1}{2} \cdot d_{VS2} \cdot T_{sw} \\ t_5 &= \frac{1}{3} \cdot d_{VM1} \cdot T_{sw} + \frac{1}{2} \cdot d_{VS1} \cdot T_{sw} \end{aligned} \tag{2.13}$$

## 2.5 Simulation results

The effectiveness of the NTVV technique in balancing the neutral-point voltage has been proven through simulations using SABER®. Figures 2.6 and 2.7 compare the performance of a conventional NTV and the NTVV techniques. In the conventional NTV technique, the duty cycle assigned to the small vectors is equally shared in every switching cycle by the corresponding two switching states, and $V_0$ is implemented by switching state {OOO}.

The comparison is performed at a high modulation index ($m_I = 0.95$) where the NTV strategy can not control the neutral-point voltage. The low-frequency neutral-point voltage oscillation incurred by the NTV technique can be observed in figure 2.6. Instead, the NTVV technique completely controls the neutral-point voltage (see figure 2.7). In fact, the NTVV strategy controls the neutral-point voltage for all modulation indices $m_I$ and load power factor.

However, this benefit in dc-link voltage balance is achieved at the expense of an

increased output-voltage high-frequency distortion. The resulting load currents have got higher THD (1.99%) compared to those of the NTV strategy (0.9%). Furthermore, for the same switching frequency and high modulation indices, the NTVV technique requires 133% the number of commutations in the NTV strategy. This increase in the number of commutations is due to the fact that the NTVV strategy always employs five different switching states per switching cycle while the NTV technique uses only four with high modulation indices and for the majority of switching cycles. The additional commutations lead to an increase in switching losses.

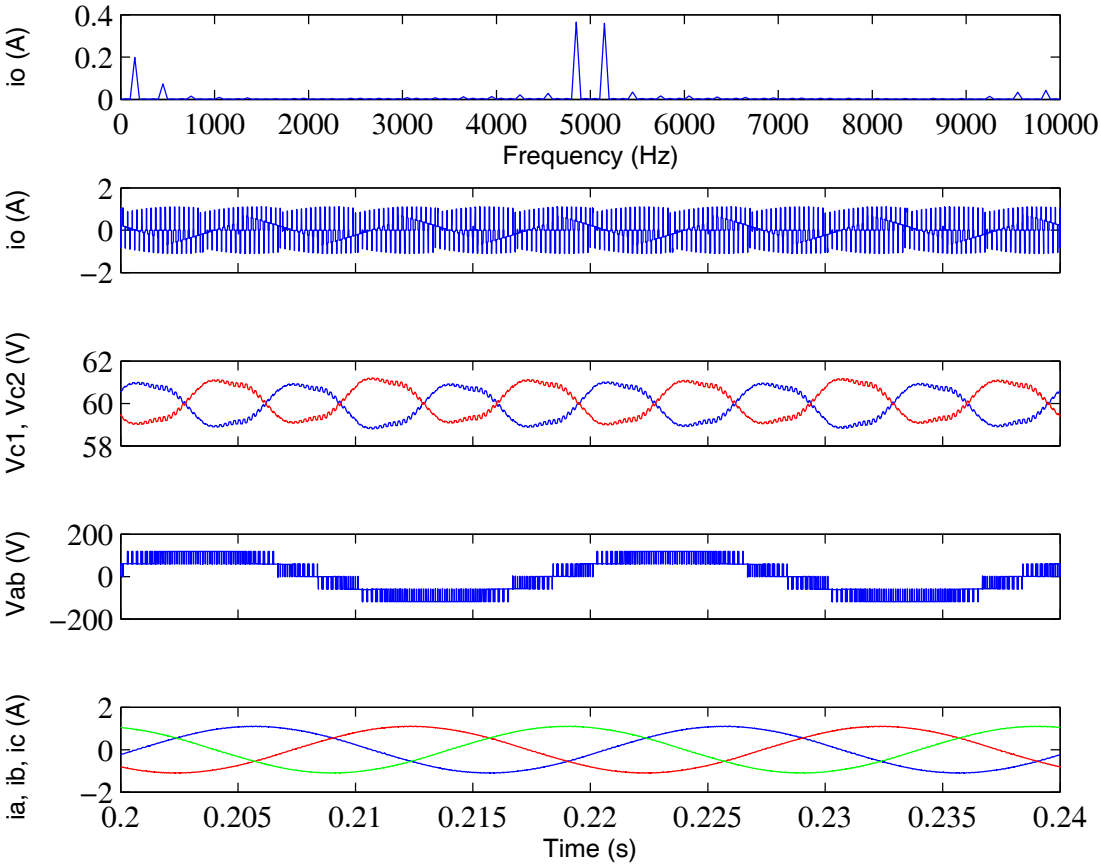



Figure 2.6: NTV technique simulation results for the following conditions: $V_{pn}$= 120V, $m_I = 0.95$, $f_{sw}$= 5kHz, $C_1 = C_2 = 200\mu$F, $R_L$=57.6Ω and $L_L$=35.5mH

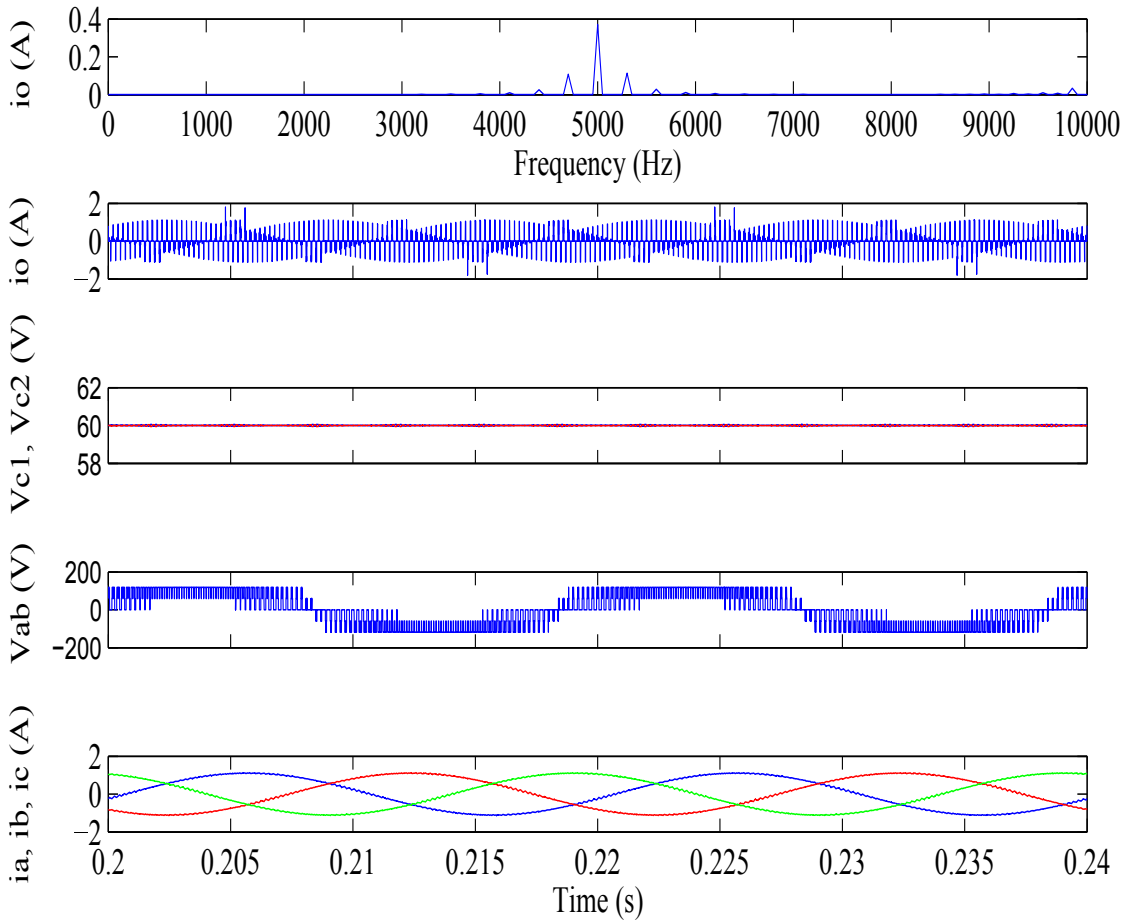



Figure 2.7: NTVV technique simulation results for the following conditions: $V_{pn}$= 120V, $m_I = 0.95$, $f_{sw}$= 5kHz, $C_1 = C_2 = 200\mu$F, $R_L$=57.6Ω and $L_L$=35.5mH

## 2.6 Conclusions

This chapter has provided a comprehensive analysis of the three-level diode clamped inverter, also known as neutral-point clamped (NPC) inverter. A number of issues have been discussed, including the inverter configuration, operating principle, space vector modulation techniques, and the neutral-point voltage balancing problem. In order to balance the capacitor voltages, the average neutral-point current over each switching cycle must be zero. This ensures equal dc-link capacitor voltages are maintained for the three-level NPC inverter to generate proper output waveforms. Simulation results have been used to demonstrate the effectiveness of the methods presented.

# Chapter 3

# Three-Level Z-Source Neutral Point Clamped Inverter

## 3.1 Introduction

This chapter reviews the state-of-the-art in three-level, Z-source NPC inverters. The circuit configuration and operating principles of this converter are described. Also, two modified space vector modulation schemes for controlling the converter are explained in detail. Finally, simulation results are used to verify the proposed modified SVM-based algorithms.

## 3.2 Overview of Z-source inverter

The topology of a two-level Z-source inverter is shown in figure 3.1. The only difference between the Z-source inverter and a traditional VSI is the presence of a Z-source network comprising two inductors ($L_1$ and $L_2$) and two capacitors ($C_1$ and $C_2$) connected between the dc source and the inverter circuit. The diode $D$ is needed to ensure

unidirectional power flow. To enable bidirectional power flow, an IGBT switch can be connected in anti-parallel to the diode. The unique feature of the Z-source inverter is that the fundamental output ac voltage can be controlled to be any value between zero and (theoretically) infinity regardless of the dc source voltage. Thus, the Z-source inverter is a voltage buck-boost inverter that has a very wide range of obtainable output voltage. Conventional VSIs cannot provide such features.

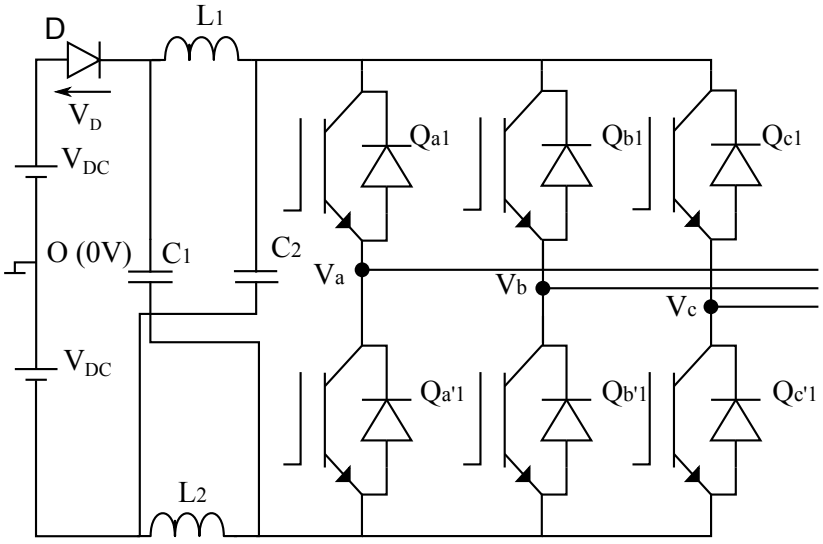



Figure 3.1: Topology of a two-level Z-source inverter

The two-level Z-source inverter bridge has fifteen permissible switching states unlike the traditional VSI that has eight. The traditional three-phase VSI has six active states when the dc voltage is impressed across the load and two zero states when the load terminals are shorted through either the lower or upper three switches, respectively. The two-level Z-source inverter bridge has seven extra zero states (termed shoot-through states) when the load terminals are shorted through both upper and lower switches of any one phase leg (i.e., both switches are turned on), any two phase legs, or all three phase legs. These shoot-through states are forbidden in a traditional VSI for obvious reasons. The Z-source network makes the shoot-through zero states permissible and provides the means by which boosting operation can be obtained.

Critically, any of the shoot-through states can be substituted for normal zero states without affecting the PWM pattern seen by the load. Therefore, for a fixed switching

cycle, insertion of shoot-through states within the zero intervals with the active states maintained constant will not alter the normalized volt-second average per switching cycle seen by the ac load. Instead, with the shoot-through states inserted, the effective inverter dc-link voltage $\hat{V}_i$ can be stepped up as given in (3.1) [23]. Consequently, taking also the PWM modulation index $m_I$ into account, the fundamental ac output line-to-line voltage $\hat{V}_{xy}(x\epsilon\{a,b,c\},\ y\epsilon\{a,b,c\})$, with $x \neq y$, can be expressed by (3.2)

$$\hat{V}_i = \frac{2V_{DC} - v_D}{(1 - 2 \cdot T_{st}/T_{sw})} = B \cdot (2V_{DC} - v_D), \qquad B \geq 1 \tag{3.1}$$

$$\hat{V}_{xy} = m_I \cdot \hat{V}_i = B \cdot \{m_I \cdot (2V_{DC} - v_D)\} \tag{3.2}$$

where $T_{st}$ and $T_{sw}$ are the shoot-through interval and switching period, respectively, $B$ is the boost factor and the term in parenthesis represents the line-to-line ac output voltage of a traditional VSI. Equations (3.1) and (3.2) show that the ac output voltage of a Z-source inverter can be regulated from zero to the normal maximum by altering $m_I$ and maintaining $B = 1$, or can be boosted above that obtainable with a traditional VSI by choosing $B > 1$. The Z-source concept can be extended to three-level inverters such as the NPC inverter as described in the following section.

## 3.3 Three-level Z-source NPC inverter

### 3.3.1 Circuit configuration

The conventional three-level NPC inverter is commonly used as the preferred topology for medium voltage ac drives and has recently been explored for low voltage renewable grid interfacing applications because it gives a better harmonic performance than the two-level inverter and can employ low voltage rated devices for medium voltage applications. In spite of its generally favourable output performance, the three-level NPC inverter is constrained by its inability to perform voltage-boost operation if no

additional dc-dc boost stage is added to its front-end. To overcome this limitation, a voltage buck-boost Z-source NPC inverter was proposed [64], with two Z-source networks added between two isolated dc sources and a conventional NPC inverter circuit, as shown in figure 3.2. The added Z-source networks are responsible for balanced voltage boosting upon shooting through any of the inverter phase legs. A shoot-through of the inverter phase legs will not cause any damage to the semiconductor switches because they are protected from a sudden surge in current by the Z-source inductors. The normal dead-time delay is not required.

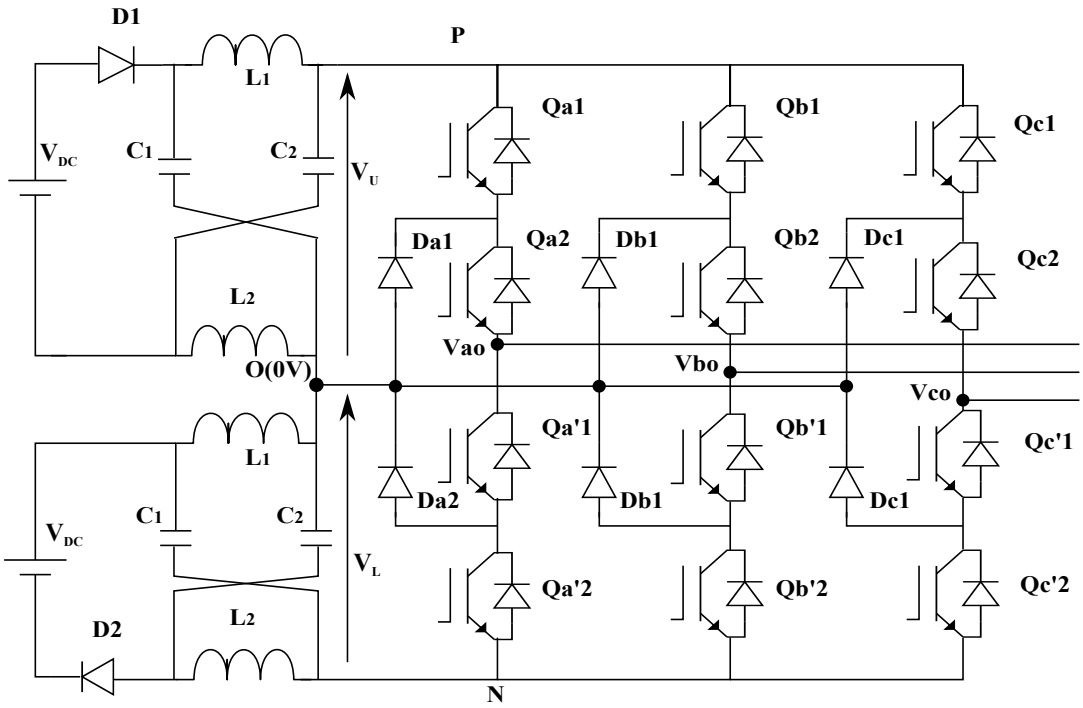



Figure 3.2: Topology of a Z-source NPC inverter with two Z-source networks

For the upper Z-source network, voltage boosting can be effected by turning on, for example, devices Qa1, Qa2 and Qa'1 with diode Da2 forward biased, whereas for the lower Z-source network, a similar effect can be achieved by turning on Qa2, Qa'1 and Qa'2 with diode Da1 forward biased. It must be pointed out here that the two Z-source networks must not be boosted simultaneously to avoid short-circuiting the full dc link, and preferably they should be boosted for equal time intervals to avoid dc voltage unbalance.

In spite of its effectiveness in achieving voltage buck-boost conversion, the Z-source NPC inverter shown in figure 3.2 is expensive because it uses two Z-source networks, two isolated dc sources and requires a complex modulator for balancing the boosting of each Z-source network. In order to overcome the cost and complexity issues, the design of a Z-source NPC inverter using a single Z-source network was proposed [65]. Figure 3.3 shows the topology of a Z-source NPC inverter that employs a single Z-source network and a split dc source.

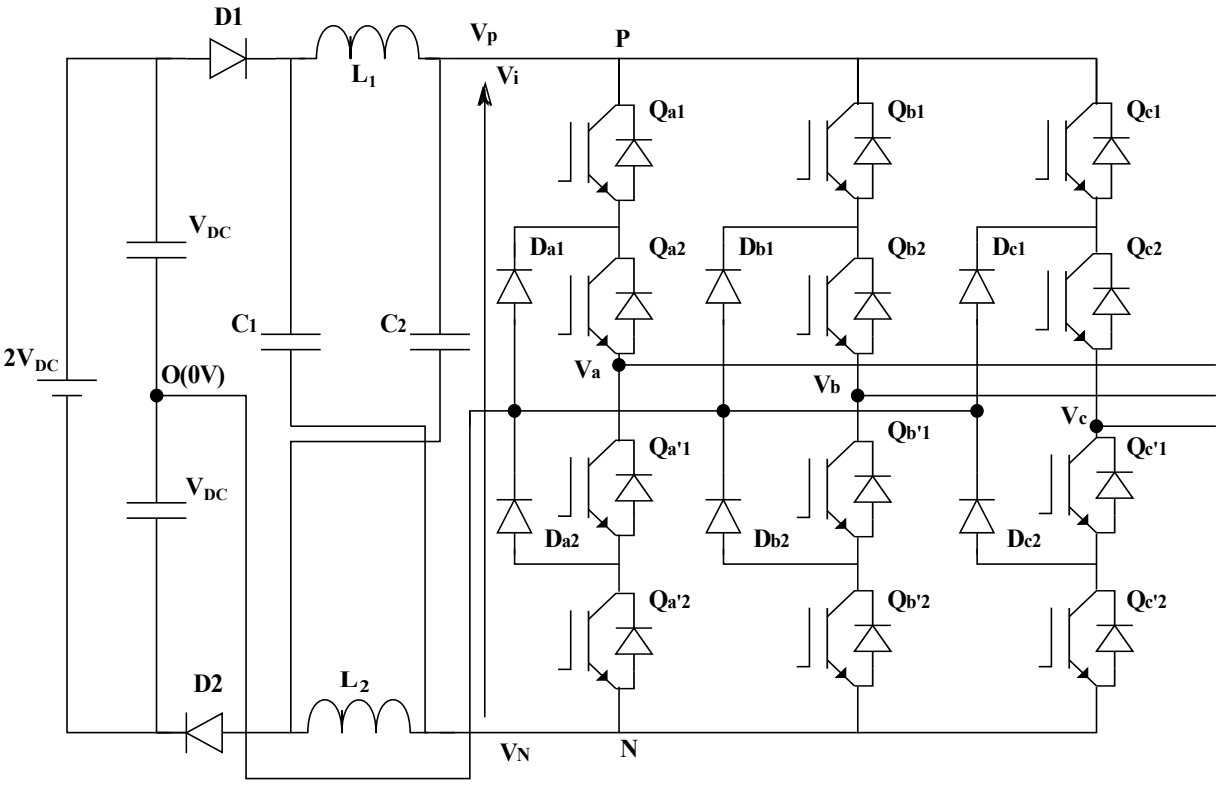



Figure 3.3: Topology of a Z-source NPC inverter with a single Z-source network

To describe the operating principle of the reduced element count (REC) Z-source NPC inverter shown in figure 3.3, we concentrate initially on the operation of one phase leg. The operation of each phase leg of a conventional NPC inverter can be represented by three switching states P, O and N. Switching state P denotes that the upper two switches in a phase leg are gated on, N indicates that the lower two switches conduct and O signifies that the inner two switches are gated on.

Each phase leg of the REC Z-source NPC inverter has three extra switching states

which resemble the 'O' state of the conventional NPC inverter. These extra switching states occur when all four of the switches in any phase leg are gated on [termed full shoot-through (FST)], or the three upper switches in any phase leg are gated on [termed upper shoot-through (UST)] or the three bottom switches in any phase leg are gated on [termed lower shoot-through (LST)]. These shoot-through states are forbidden in the traditional NPC inverter because they would cause a short circuit of the dc side capacitors. Again, the Z-source network makes these shoot-through states permissible and provides the means for boost operation.

### 3.3.2 Circuit analysis of the REC Z-source NPC inverter

Among the three-level Z-source power converter topologies reported to date, the Z-source NPC inverter implemented using a single Z-source network is considered to be an optimized topology in terms of component count [66]. Referring to figure 3.3, the REC Z-source NPC inverter is supplied with a split dc source. The middle point ($O$) of the series connected capacitors is taken as the reference. By controlling the switches of each phase leg according to the combinations presented in table 3.1, each output phase voltage $\hat{V}_{xo}(x\epsilon\{a,b,c\})$ has three possibilities: $V_i/2$, 0 and $-V_i/2$.

| State Type | ON Switches | ON Diodes | $V_{XO}$ | Switching State |
|---|---|---|---|---|
| NST | Qx1,Qx2 | D1,D2 | $+V_i/2$ | P |
| NST | Qx2,Qx'1 | D1,D2,{Dx1 or Dx2} | 0 | O |
| NST | Qx'1,Qx'2 | D1,D2 | $-V_i/2$ | N |
| FST | Qx1,Qx2,Qx'1,Qx'2 | — | 0 | F |
| UST | Qx1,Qx2,Qx'1 | Dx2,D1 | 0 | U |
| LST | Qx2,Qx'1,Qx'2 | Dx2,D1 | 0 | L |

Table 3.1: Switching States of an REC Z-source NPC inverter

When the REC Z-source NPC inverter is operated as a traditional NPC inverter ( i.e., without any shoot-through states), then $\hat{V}_i$ is equivalent to $(2V_{DC} - v_{D_1} - v_{D_2})$. As noted earlier, with this kind of operation, the maximum obtainable output line-to-line voltage cannot exceed the available dc source voltage. Therefore, to obtain an output line-to-line voltage greater than the available dc source voltage, shoot-through

states are carefully inserted into selected phase legs to boost the dc-link voltage to $\hat{V}_i > (2V_{DC} - v_{D_1} - v_{D_2})$ before it is inverted by the NPC circuit. Thus, the REC Z-source NPC inverter can boost and buck the output line-to-line voltage with a single stage structure. In [67], the switching states UST (U) and LST (L) were identified in addition to the FST and NST (P, O, N) states that had been reported earlier in [65]. There are, therefore, two shoot-through operating modes for the REC Z-source NPC inverter. These are known as the full-shoot-through operating mode (uses the FST and NST states) and the upper-lower-shoot-through (ULST) operating mode (uses the UST, LST and NST states).

#### 3.3.2.1 Full-shoot-through operating mode

Figure 3.4 shows the equivalent circuits for analysis. Here, figure 3.4(a) shows the simplified equivalent circuit for the non-shoot-through states while figure 3.4(b) shows it for the full-shoot-through states.

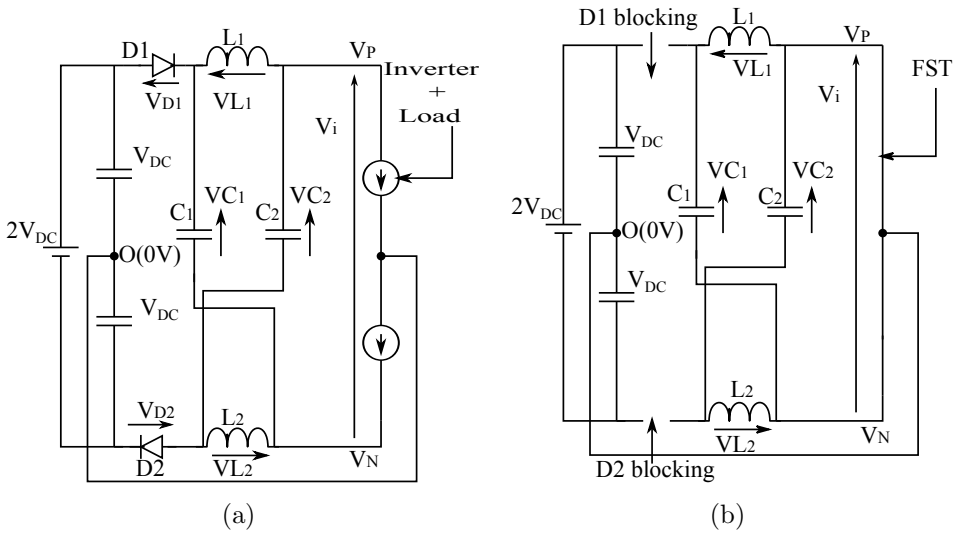



Figure 3.4: Simplified representation of REC Z-source NPC inverter in (a) non-shoot-through states and (b) full-shoot-through states

Assuming that the Z-source network is symmetrical ($L_1 = L_2 = L$ and $C_1 = C_2 = C$) and the diodes D1 and D2 are identical, the voltage expressions for the non-shoot-

through states are:

$$v_{L_1} = 2V_{DC} - v_{C_2} - v_{D1} - v_{D2} \qquad v_{L_2} = 2V_{DC} - v_{C_1} - v_{D1} - v_{D2} \tag{3.3}$$

$$v_P = \frac{+\hat{v_i}}{2} \qquad v_N = \frac{-\hat{v_i}}{2} \tag{3.4}$$

$$v_i = v_{C_1} + v_{C_2} - 2V_{DC} + v_{D1} + v_{D2} \tag{3.5}$$

Similarly, the voltage expressions for the full-shoot-through states are as follows:

$$v_{L_1} = v_{C_1} \qquad v_{L_2} = v_{C_2} \tag{3.6}$$

$$v_P = v_N = 0V \tag{3.7}$$

Averaging $v_{L_1}$ and $v_{L_2}$ over a switching cycle, we have:

$$V_{C_1} = V_{C_2} = V_C = \left\{ \frac{1 - \frac{T_{st}}{T_{sw}}}{1 - \frac{2T_{st}}{T_{sw}}} \right\} \cdot (2V_{DC} - v_{D1} - v_{D2}) \tag{3.8}$$

$$\hat{V_i} = \left\{ \frac{1}{1 - \frac{2T_{st}}{T_{sw}}} \right\} \cdot (2V_{DC} - v_{D1} - v_{D2}) \tag{3.9}$$

Using (3.9), the peak ac output line-to-line voltage $\hat{V}_{xy}(x\epsilon\{a, b, c\},\ y\epsilon\{a, b, c\})$, with $x \neq y$, for the REC Z-source NPC inverter is derived as follows:

$$\hat{V}_{xy} = m_I \cdot \hat{V_i} = B \cdot \{m_I \cdot (2V_{DC} - v_{D1} - v_{D2})\} \tag{3.10}$$

where $m_I$ is the modulation index and $B = 1/(1-2T_{st}/T_{sw})$ is the boost factor, which preferably should be set to unity ($T_{st}/T_{sw} = 0$) for voltage-buck operation and $B > 1$ for voltage-boost operation. For voltage-buck operation, $\hat{V_i} = (2V_{DC} - v_{D_1} - v_{D_2})$ since $B = 1$, implying that the three distinct voltage levels that the inverter can assume are $+(2V_{DC} - v_{D_1} - v_{D_2})/2$, 0, and $-(2V_{DC} - v_{D_1} - v_{D_2})/2$, which, in principle, are similar to those of a traditional three-level NPC inverter.

The simplest full-shoot-through operating mode requires all four switches in a phase leg to be turned on. This is not a minimal loss approach since, for instance, switching phase 'a' from $+(2V_{DC} - v_{D_1} - v_{D_2})/2 \rightarrow$ FST $\rightarrow$ 0V would require switches {Qa1, Qa2, Qa'1, Qa'2} changing from {ON ,ON, OFF, OFF} $\rightarrow$ {ON, ON, ON, ON} $\rightarrow$ {OFF, ON, ON, OFF}. An alternative full-shoot-through operating mode which gives

minimal loss uses two phase legs to create the shoot-through path. This requires, for example, synchronization of the turn on times of switches Qa1 from phase 'a' and Qc'2 from phase 'c' at the start of a FST state. Doing so creates a time interval during which switches {Qa1, Qa2, Qa'1} from phase 'a' and {Qc2, Qc'1, Qc'2} from phase 'c' are gated on simultaneously to create a shoot-through path [65]. The FST operating mode can be implemented with the alternative phase opposition disposition (APOD) carrier-based modulation only [67]. This is because it is in the APOD carrier-based modulation alone that we have a set of zero three-phase line-to-line voltages (state {O,O,O}) at either the start or end of a half carrier cycle. Both {O,O,O} and FST states indistinctly produce a set of zero three-phase line-to-line voltages that can replace one another for altering the inverter output gain, without introducing distortion to the external load. The output line-to-line voltages obtained using the full-shoot-through operating mode do not have adjacent level switching due to the use of the APOD modulation scheme. Therefore, the upper-lower-shoot-through operating mode is generally preferred and is the option adopted in this work.

#### 3.3.2.2 Upper-lower-shoot-through operating mode

The upper-lower-shoot-through operating mode is generally preferred to the full-shoot-through mode because it produces an output voltage with enhanced waveform quality [67]. Figure 3.5(a) shows the simplified equivalent circuit for the UST states while figure 3.5(b) shows that of the LST states. It should be noted that there are multiple ways of creating the UST and LST states using different phases. The choice between these is discussed later.

Assuming that the Z-source network is symmetrical and the diodes D1 and D2 are identical, the voltage expressions for the upper shoot-through states are:

$$v_{L_1} = V_{DC} - v_{D1} \tag{3.11}$$

$$v_P = 0V \qquad\qquad v_N = V_{DC} - V_{C_1} - v_{D1} \tag{3.12}$$

Similarly, the voltage expressions for the lower shoot-through states are:

$$v_{L_2} = V_{DC} - v_{D2} \tag{3.13}$$

$$v_P = -V_{DC} + V_{C_2} + v_{D2} \qquad v_N = 0V \tag{3.14}$$

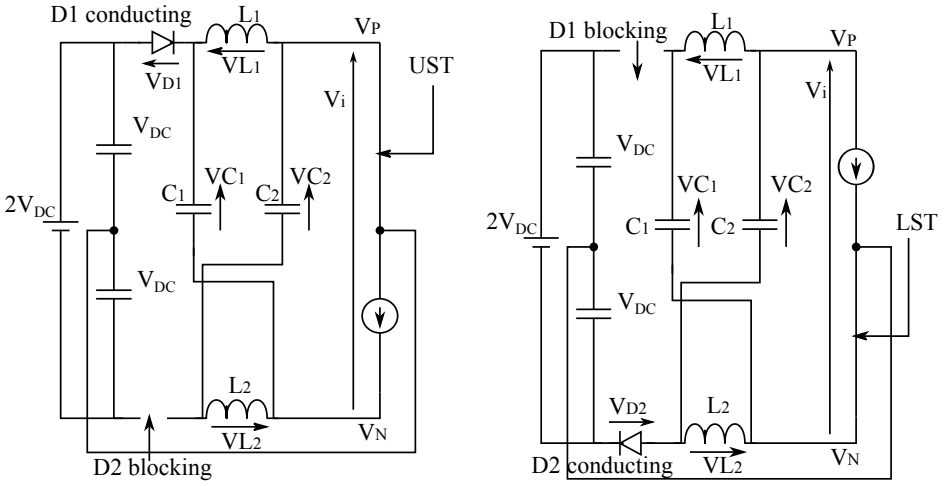



Figure 3.5: Simplified representation of REC Z-source NPC inverter in (a) upper shoot-through states and (b) lower shoot-through states

Let us denote the duration of UST and LST states by $T_u$ and $T_l$ respectively. Also, it is assumed that $T_u$ and $T_l$ are equal (this is necessary to ensure symmetrical operation) and denote the total upper and lower shoot-through duration by $T_{ulst}$. At steady state, the average voltage across the inductors is zero, therefore averaging the inductor voltages over one switching period we have:

$$V_{C_1} = V_{C_2} = V_C = \left\{ \frac{1 - \frac{T_{ulst}}{2T_{sw}}}{1 - \frac{T_{ulst}}{T_{sw}}} \right\} \cdot (2V_{DC} - v_{D1} - v_{D2}) \tag{3.15}$$

Substituting (3.15) into (3.5), we have the dc-link voltage $\hat{V}_i$ during the NST states as:

$$V_{i\_NST} = \left\{ \frac{1}{1 - \frac{T_{ulst}}{T_{sw}}} \right\} \cdot (2V_{DC} - v_{D1} - v_{D2}) \tag{3.16}$$

Similarly, when (3.15) is substituted into (3.12) and (3.14), noting that $V_i = V_P - V_N$, we have the dc-link voltage during the UST and LST states as:

$$V_{i\_UST} = V_{i\_LST} = \left\{ \frac{1}{1 - \frac{T_{ulst}}{T_{sw}}} \right\} \cdot (V_{DC} - v_{D1}) = \left\{ \frac{1}{1 - \frac{T_{ulst}}{T_{sw}}} \right\} \cdot (V_{DC} - v_{D2}) \tag{3.17}$$

It is noted from (3.16) and (3.17) that the higher dc-link voltage is present during the NST states and it is twice the dc-link voltage available during the UST and LST states, as required. The fundamental peak ac output line-to-line voltage $\hat{V}_{xy}(x\epsilon\{a,b,c\}$, $y\epsilon\{a,b,c\})$, with $x \neq y$, for the REC Z-source NPC inverter is thus given by:

$$\hat{V}_{xy} = m_I \cdot V_{i\_NST} = B' \cdot \{m_I \cdot (2V_{DC} - v_{D1} - v_{D2})\} \tag{3.18}$$

where $B' \geq 1$ is the boost factor. Comparing (3.9) and (3.16), it is noted that the same effective dc-link voltage can be obtained by setting $T_{ulst} = 2T_{st}$, where the maximum values of $T_{ulst}$ and $T_{st}$ are $T_{sw}$ and $0.5T_{sw}$, respectively.

## 3.4 Selection of Z-source component values

An usual concern accompanying Z-source converters is capacitor and inductor sizing. These components should normally be small and at the same time be able to filter the converter ripples [23]. Based on this compromise, a relevant study is found in [68] and a summary is given below.

Let the peak ripples and average values of capacitor voltages and inductor currents be defined as $\Delta V_c$, $\Delta I_l$, $\bar{V_c}$ and $\bar{I_l}$, respectively. Assuming linear variation of waveforms, $\Delta V_c$ and $\Delta I_l$ can be written as

$$\Delta V_c = \frac{\bar{I_c}\Delta t}{C} \qquad\qquad \Delta I_l = \frac{\bar{V_l}\Delta t}{L} \tag{3.19}$$

Considering a shoot-through period of $T_{ulst}$, $C_{1,2}$ and $L_{1,2}$ can be found as:

$$C_{1,2} = \frac{\bar{I_l}T_{ulst}}{8\Delta V_c} \qquad\qquad L_{1,2} = \frac{\bar{V_c}T_{ulst}}{8\Delta I_l} \tag{3.20}$$

These can more conveniently be written as:

$$C_{1,2} = \frac{1.5m_I I_{im} cos(\phi)\bar{V_c}T_{ulst}}{32V_{DC}(1 - 0.5T_{ulst}/T_{sw})\Delta V_c} \quad L_{1,2} = \frac{V_{DC}(1 - 0.5T_{ulst}/T_{sw})\bar{I_l}T_{ulst}}{3m_I I_{im} cos(\phi)\Delta I_l} \tag{3.21}$$

where $I_{im}$ is the peak phase current on the ac side and $\phi$ is the power factor angle of the load on the ac side of the inverter. Thus if $V_{DC}$, $I_{im}$, $\phi$, $T_{ulst}$, $T_{sw}$ and $m_I$

are known, $C_{1,2}$ and $L_{1,2}$, for any control strategy can be calculated to result in the desired levels of ripples.

In the following sections, two novel modified SVM techniques for controlling the Z-source NPC inverter are presented. These are the NTV and NTVV techniques. As discussed in Chapter 2, the NTV technique is not able to eliminate the neutral-point balancing problem of the traditional NPC inverter completely. As a result, using the NTV technique to control a three-level, two-stage matrix converter (Chapter 5) becomes very difficult. Fortunately, the NTVV technique is able to eliminate the neutral-point balancing problem of the NPC inverter completely. This allows the NTVV technique to be used to control a three-level, two-stage matrix converter with ease. The NTVV technique for controlling the Z-source NPC inverter will therefore serve as the foundation for the control of the three-level, Z-source hybrid direct ac-ac power converter discussed in Chapter 6.

## 3.5 Novel NTV SVM for Z-source NPC inverter

The NTV technique for controlling the traditional NPC inverter has been described in Chapter 2. A similar process is used for the modulation of the Z-source NPC inverter. The duty cycles of the switches are calculated in the same way as described in section 2.3.1 and will not be repeated here. The only difference between the NTV technique for controlling the traditional NPC inverter and that of the Z-source NPC inverter is associated with the insertion of shoot-through states in the PWM switching pattern. It must be stated that this novel NTV SVM strategy for the Z-source NPC inverter was first proposed by the author in [69].

### 3.5.1 PWM switching pattern

In order to achieve minimal number of switches changing between two adjacent states, a seven-segment switching sequence is adopted in NTV SVM. It is convenient to perform "origin shifting" and subsequently perform a three-level modulation using two-level principles [49, 70]. In figure 2.2, if we shift the origin from {PPP/OOO/NNN} to {POO/ONN}, then the equivalent null (E-null) state is transferred to {POO/ONN} while the equivalent active (E-active) states are transferred to {PPP/OOO/NNN}, {PPO/OON}, PON and PNN, respectively.

To introduce shoot-through states, it is necessary to determine where the UST and LST states can be inserted, and on which phase, in order that the normalised volt-second area applied to the load is unchanged from that of the standard NPC inverter case discussed earlier. In addition, it is desirable to ensure that no extra commutations are introduced. Theoretically, a shoot-through state can be introduced on any phase that is switched to the zero (0) level without affecting that phase voltage.

| UST states | LST states |
|---|---|
| UNN | PLO |
| UON | POL |
| OUN | PPL |
| NUN | LPO |
| NUO | OPL |
| NOU | LPP |
| NNU | LOP |
| UNO | OLP |
| ONU | PLP |

Table 3.2: The permissible upper and lower shoot-through states

However, the effect on the line-to-line voltages must also be taken into account. It should be noted that when any phase has UST state applied, the positive rail ($P$) is at the same potential as the dc mid-point ($O$). Similarly, during LST state, the negative rail ($N$) is at the same potential as the dc mid-point ($O$). Consequently, it is only possible to use the UST state on a given phase when it is connected to '$O$' and the other two phases are connected to either '$O$' or '$N$' in order to get the

correct line-to-line voltages. Similarly, a LST state can only be used when the other two phases are connected to '$O$' or '$P$'. Therefore, the permissible upper and lower shoot-through states are as shown in table 3.2.

Taking the above into account, the objective is to deploy the UST/LST states for voltage boosting in an optimal way that does not increase the number of commutations. A modified PWM sequence which achieves this can be derived as discussed below.

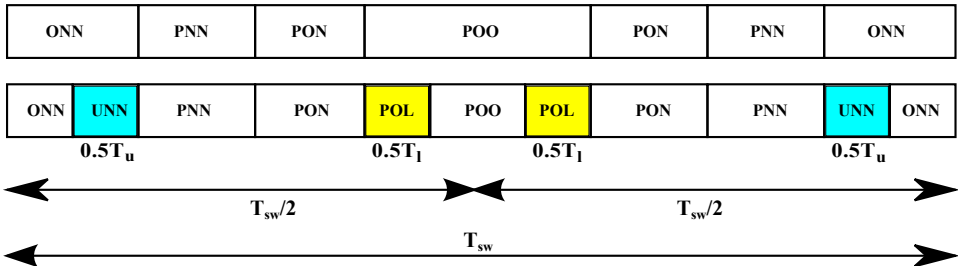



Figure 3.6: NTV modulation for the REC Z-source NPC inverter using the ULST mode with reference vector in triangle 3

Figure 3.6 shows the seven-segment PWM switching pattern for modulating a conventional NPC inverter and an REC Z-source NPC inverter when the reference output voltage vector, $\vec{V}_{out}$, is in triangle 3, sector I, of the space vector diagram shown in figure 2.2. Comparing the sequences shown in figure 3.6, it is observed that the only difference between them is the insertion of UST/LST states in the E-null states of the REC Z-source NPC inverter. Insertion of shoot-through states at these places do not result in additional switching since, for example, the transition from ONN to PNN can be achieved by switching devices {Qa1, Qa2, Qa'1, Qa'2} from {OFF, ON, ON, OFF} $\rightarrow$ {ON, ON, ON, OFF} $\rightarrow$ {ON, ON, OFF, OFF} [71]. The phase 'a' voltage during the UST state is the same as that of the 'O' state because during the UST state the voltage $(V_{DC} - V_{D_1})$ is dropped across inductor $L_1$ and the voltage seen by phase 'a' is 0V (see figure 3.5(a)). Hence the UNN and ONN states can supplement each other for voltage boosting without modifying the line-to-line volt-second average (normalised by taking the boost factor into account).

Applying the same analysis and moving on to the second transition, PNN $\rightarrow$ PON,

where phase 'b' switches from the N state to the O state, no shoot-through state is inserted (note that it is not possible to introduce UST or LST for the PON state for the reasons discussed earlier). Moving forward again to the third transition, PON →POO where phase 'c' switches from the 'N' state to the 'O' state, a LST state is inserted since the switching of devices {Qc1, Qc2, Qc'1, Qc'2} from {OFF, OFF, ON, ON} → {OFF, ON, ON, ON} → {OFF, ON, ON, OFF} will not affect phases 'a' and 'b' which remain clamped to points '$P$' and '$O$', respectively. The phase 'c' voltage during the LST state is equal to that of the 'O' state since the voltage $(V_{DC} - v_{D_2})$ is dropped across inductor $L_2$ and the voltage seen by phase 'c' is 0V (see figure 3.5(b)). This means that the POL and POO states can supplement each other for voltage boosting without modifying the produced volt-second average (normalised by taking the boost factor into account). A similar process is repeated for all the other triangles in sector I.

From the above discussions, it is noted that the shoot-through states are inserted at the E-null to E-active state transitions with no shoot-through states inserted at the E-active to E-active state transitions. It is also noted that the shoot-through states do not affect the PWM control of the inverter, because they equivalently produce the same zero voltage at the load terminals. Another feature noted with the ULST modulation strategy is that the UST and LST states are introduced for only half of the total shoot-through duration of $T_{ulst}$, unlike the FST modulation strategy, where the Z-source network is shorted for the total shoot-through duration. Therefore, to produce the same boost factor for the ULST and FST schemes we need to set $T_{ulst}/T_{sw} = 2T_{st}/T_{sw}$. The available shoot-through period is limited by the E-null period that is determined by the modulation index according to (3.22) for the simple boost control method [72, 73].

$$\frac{T_{ulst}}{2T_{sw}} = \frac{T_{st}}{T_{sw}} = \frac{T_u}{T_{sw}} = \frac{T_l}{T_{sw}} = 1 - m_I \tag{3.22}$$

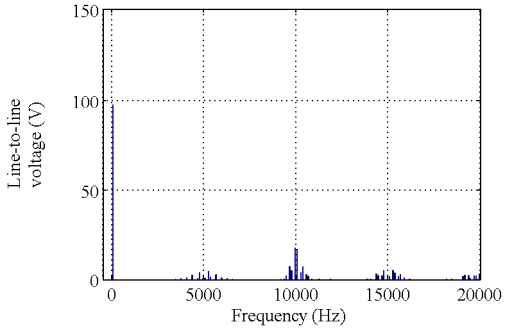
### 3.5.2 Simulation results

To verify the NTV SVM-based modulation algorithm, simulations were performed in SABER®. The Z-source network was implemented using 6.3-mH inductors and 2200-$\mu$F capacitors, and powered by a 120-V split dc supply. An R-L load comprising 20-$\Omega$ resistors and 10-mH inductors was used to verify the theoretical findings.

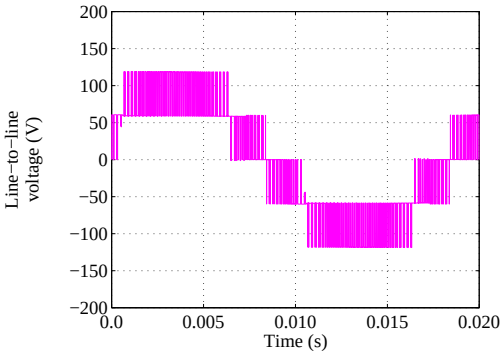
The boosting ability of the Z-source NPC inverter is demonstrated by considering a modulation index, $m_I = 0.825$, and a shoot-through ratio, $T_{ulst}/T_{sw} = 0.0$, for the non-boost case. For this case the maximum output line-to-line voltage that can be achieved is limited to $m_I \times (2V_{DC} - v_{D_1} - v_{D_2})$. With $v_{D_1} = v_{D_2} = 0.7$V, we expect the peak value of the fundamental output voltage to be 97.8V. This is clearly seen in figure 3.7(a) where the output line-to-line voltage shows a peak fundamental component of 97.8V as expected according to (3.18). The inverter dc-link voltage is obviously not boosted and the peak value of the output line-to-line voltage is maintained at 118.6V by the dc source according to (3.16) as shown in figure 3.7(b). The phase-to-neutral voltage, $V_{ao}$, gives an expected value of 59.3V (figure 3.7(c)). A set of balanced sinusoidal load currents (THD = 1.2%) are also observed (figure 3.7(d)). The voltages across the Z-source capacitors $V_{C1} = V_{C2} = V_C$ are clearly maintained at 118.6V since no boosting is commanded (figure 3.7(e)). Similarly, the dc-link voltage seen by the NPC inverter circuit, $V_i$, is maintained at 118.6V (figure 3.7(f)).

Next, boosting was commanded by using a modulation index, $m_I = 0.825$, and shoot-through ratio, $T_{ulst}/T_{sw} = 0.3$. From (3.16), this yields a boost factor of 1/0.7 (=1.43) and hence the expected peak fundamental line-to-line voltage is 97.8×1.43 (=139.9V). Figure 3.8 shows the corresponding boosted inverter waveforms. The spectrum of the output line-to-line voltage shows a peak fundamental value of 140V as expected. Also, the dc-link voltage has been boosted to an expected value of 170V (see (3.16)). It is also noted that the line currents are not distorted (THD = 1.2%) even when shoot-through states are intentionally inserted into the appropriate phase legs because of the presence of the Z-source network.

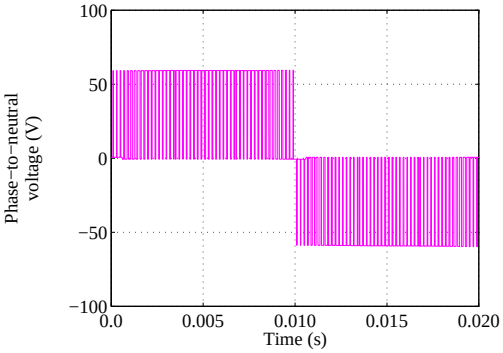
The voltages across the Z-source capacitors are boosted to an expected value of 144V (see (3.15)). In addition, the dc-link voltage seen by the NPC circuit assumes two distinct levels of 170V and 85V respectively. The simulation results show that the REC Z-source NPC inverter, with the modified NTV modulation algorithm, is able to boost the output line-to-line voltage to a value higher than the available dc supply with sinusoidal output currents.



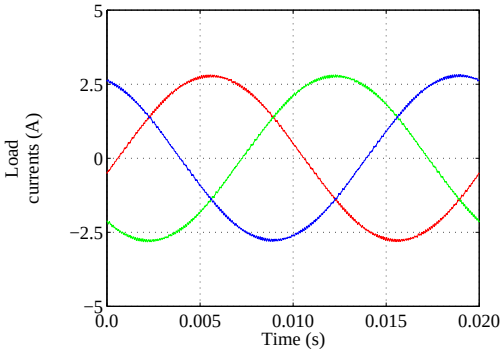

(a) Spectrum of line-to-line voltage, Vab



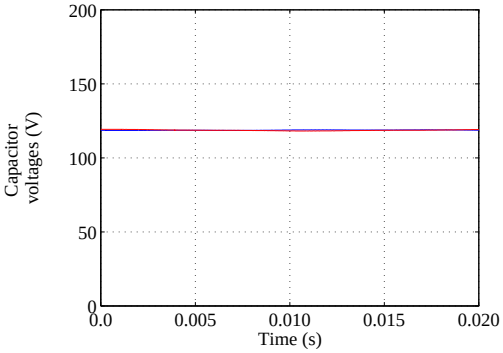

(b) Line-to-line voltage, $V_{ab}$



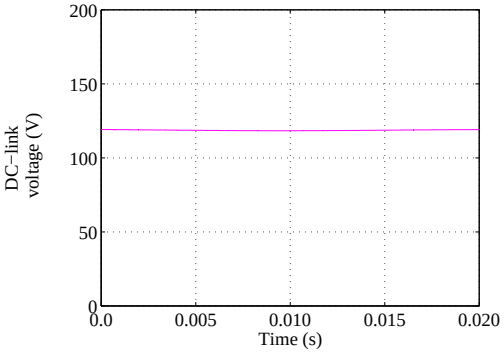

(c) Phase-to-neutral voltage, Vao




(d) Load currents

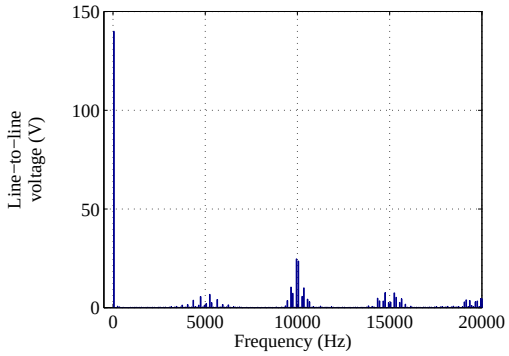



(e) Capacitor voltages, $V_{C_1}$,$V_{C_2}$

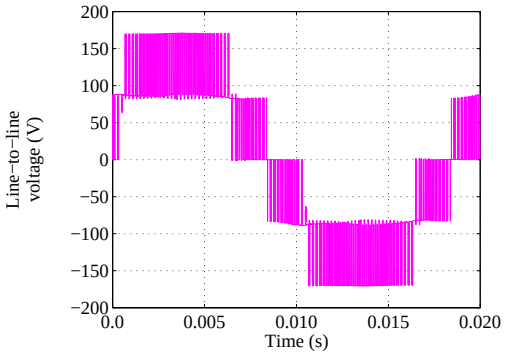



(f) DC-link voltage, $\hat{V}_i$

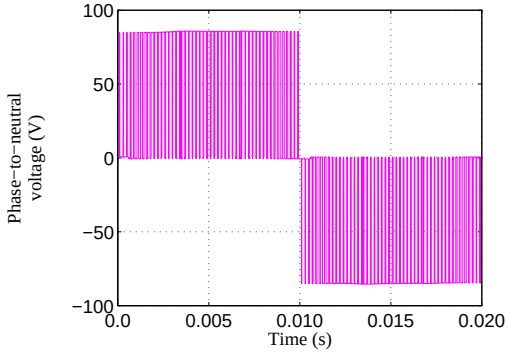
Figure 3.7: Simulation results of the three-level Z-source NPC inverter in an ULST operating mode with $m_I = 0.825$, $T_{ulst}/T_{sw} = 0.0$



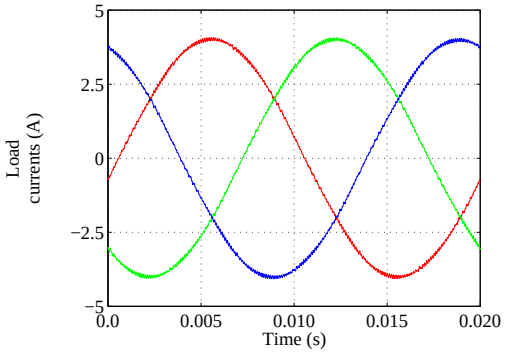

(a) Spectrum of line-to-line voltage, Vab



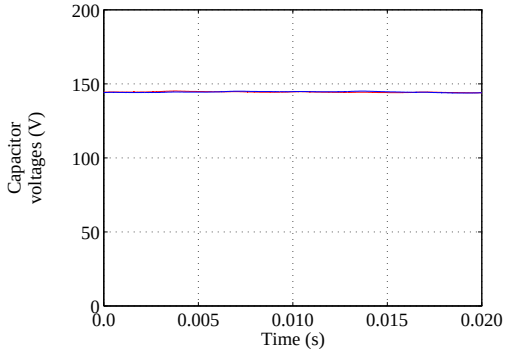

(b) Line-to-line voltage, $V_{ab}$



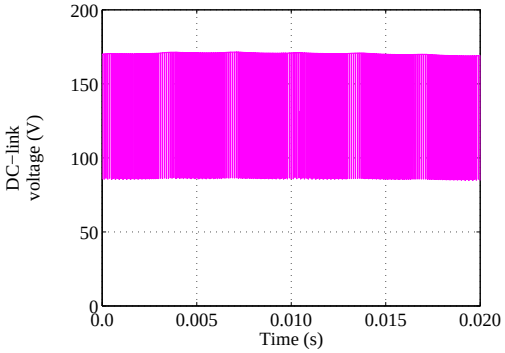

(c) Phase-to-neutral voltage, Vao




(d) Load currents




(e) Capacitor voltages, $V_{C_1}$,$V_{C_2}$




(f) DC-link voltage, $\hat{V}_i$

Figure 3.8: Simulation results of the three-level Z-source NPC inverter in an ULST operating mode with $m_I = 0.825$, $T_{ulst}/T_{sw} = 0.3$

## 3.6 Novel NTVV SVM for Z-source NPC inverter

The NTVV technique for controlling the traditional NPC inverter has been described in Chapter 2. A similar process is used for the modulation of the Z-source NPC inverter. The duty cycles of the switches are calculated in the same way as described in section 2.3.2 and will not be repeated here. The only difference between the NTVV technique for controlling the traditional NPC inverter and that of the Z-source NPC inverter is associated with the insertion of shoot-through states in the PWM switching pattern. Again, it must be stated that the modified NTVV SVM for the Z-source NPC presented here has not been reported before in the literature.

### 3.6.1 PWM switching pattern

To ensure that the Z-source NPC inverter is able to perform voltage buck-boost operation, shoot-through states are carefully inserted into selected phase legs. We consider only the insertion of UST and LST states since the FST states can not be used with the NTVV technique. The objective is to deploy the UST/LST states for voltage boosting in an optimal way that does not increase the number of commutations. A modified PWM sequence which achieves this can be derived as discussed below.

Consider the situation when the reference output voltage vector, $\vec{V}_{out}$, is located in triangle 4 of the vector diagram shown in figure 2.4. The reference vector is synthesized by using the virtual vectors: $\vec{V}_{V_{M1}}$, $\vec{V}_{V_{L1}}$ and $\vec{V}_{V_{L2}}$. These virtual vectors are formed by using the voltage vectors: $\vec{V}_{S1}$[ONN], $\vec{V}_{M1}$[PON], $\vec{V}_{S2}$[PPO], $\vec{V}_{L1}$[PNN] and $\vec{V}_{L2}$[PPN]. The voltage vectors are applied to the output according to the switching sequence PPO $\rightarrow$ PPN $\rightarrow$ PON $\rightarrow$ PNN $\rightarrow$ ONN. To insert shoot-through states, we consider the first transition (PPO $\rightarrow$ PPN) where it is noted that phase '$c$' makes a transition from the 'O' state to the 'N' state while phases '$a$' and '$b$' remain in the 'P' state. Therefore a LST state can be inserted next to the 'PPO' state without introducing any volt-second error.

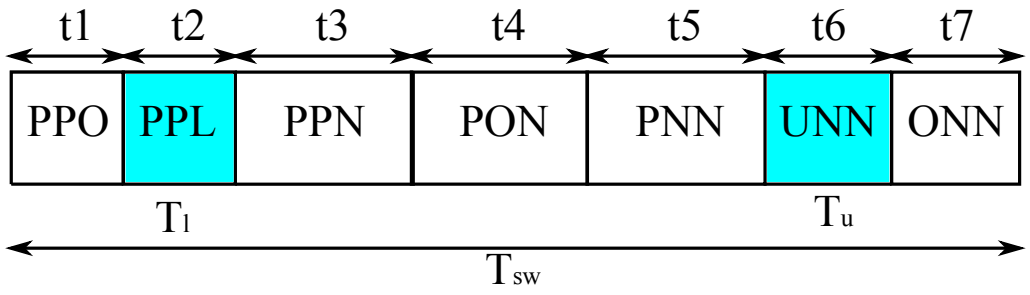



Figure 3.9: The switching pattern for the Z-source NPC inverter using ULST mode for the case where $\vec{V}_{out}$ is located in triangle 4 of sector I.

Moving on to the next transition (PPN → PON), no shoot-through states can be inserted because the condition that needs to be met for the insertion of UST or LST state is not satisfied. Similarly, no shoot-through state can be inserted at the (PON → PNN) transition for the same reason. Next, moving on to the (PNN → ONN) transition, it is noted that phase '$a$' makes a transition from the 'P' to 'O' state while phases '$b$' and '$c$' remain in the 'N' state. Therefore, an UST state can be inserted next to the 'ONN' state without introducing any extra commutations since the condition for insertion of UST state is satisfied. Figure 3.9 shows the PWM switching pattern for the case described above. In order to reduce the output harmonic content, the switching sequence is reversed in the next switching cycle so that a double-sided switching sequence is formed. For a switching period, $T_{sw}$, the active time of each voltage vector is given by (3.23).

$$\begin{aligned}
t_1 &= \frac{1}{3} \cdot d_{VM1} \cdot T_{sw} + \frac{1}{2} \cdot d_{VS2} \cdot T_{sw} - T_l \\
t_2 &= T_l \\
t_3 &= \frac{1}{2} \cdot d_{VS1} \cdot T_{sw} \\
t_4 &= \frac{1}{3} \cdot d_{VM1} \cdot T_{sw} \\
t_5 &= \frac{1}{2} \cdot d_{VS2} \cdot T_{sw} \\
t_6 &= T_u \\
t_7 &= \frac{1}{3} \cdot d_{VM1} \cdot T_{sw} + \frac{1}{2} \cdot d_{VS1} \cdot T_{sw} - T_u
\end{aligned} \tag{3.23}$$

A similar procedure can be applied to all the other triangles shown in the vector

diagram of figure 2.4. Table A.2 shows all the switching sequences for triangles 1 to 5 in all the six sectors.

### 3.6.2 Simulation results

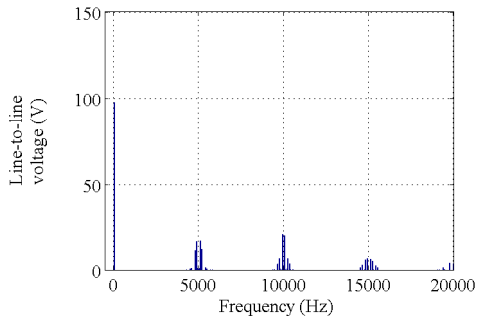
To verify the NTVV SVM-based modulation algorithm, simulations were performed in SABER®. The Z-source network was implemented using 6.3-mH inductors and 2200-$\mu$F capacitors, and powered by a 120-V split dc supply. An R-L load comprising 20-$\Omega$ resistors and 10-mH inductors was used to verify the theoretical findings.

The boosting ability of the Z-source NPC inverter is demonstrated by first considering a modulation index, $m_I = 0.825$, and a shoot-through ratio, $T_{ulst}/T_{sw} = 0.0$, for the non-boost case. The fundamental component of the output line-to-line voltage that can be achieved is limited to $m_I \times (2V_{DC} - v_{D_1} - v_{D_2})$. With $v_{D_1} = v_{D_2} = 0.7$V, we expect the peak value of the fundamental component to be 97.8V. This is clearly seen in figure 3.10(a) where the output line-to-line voltage shows a peak fundamental component of 97.8V as expected according to (3.18). The inverter dc-link voltage is obviously not boosted and the peak value of the output line-to-line voltage is maintained at 118.6V by the dc source according to (3.16) as shown in figure 3.10(b). The phase-to-neutral voltage, $V_{ao}$, gives an expected value of 59.3V (figure 3.10(c)). A set of balanced sinusoidal load currents (THD = 2.3%) are also observed (figure 3.10(d)). The voltages across the Z-source capacitors $V_{C1} = V_{C2} = V_C$ are clearly maintained at 118.6V since no boosting is commanded (figure 3.10(e)). Similarly, the dc-link voltage seen by the NPC inverter circuit, $V_i$, is maintained at 118.6V (figure 3.10(f)).

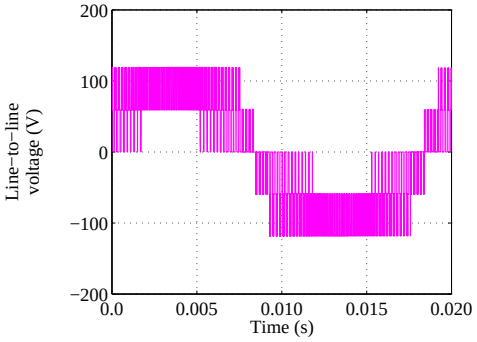
Next, the modulation index is maintained at $m_I = 0.825$ but boosting is commanded by setting the shoot-through ratio, $T_{ulst}/T_{sw} = 0.3$. From (3.16), this yields a boost factor of 1/0.7 (=1.43) and hence the expected peak fundamental line-to-line voltage is 0.825×118.6×1.43 (= 139.9V). The corresponding boosted inverter waveforms are shown in figure 3.11. The spectrum of the output line-to-line voltage shows a peak

fundamental value of 140V as expected. Also, the dc-link voltage has been boosted to an expected value of 170V (see (3.16)) . The voltages across the Z-source capacitors are boosted to an expected value of 144V (see (3.15)). In addition, the dc-link voltage seen by the NPC circuit assumes two distinct levels of 170V and 85V, respectively. However, it is observed that there is an increase in the output current distortion (THD = 2.8%) during the boost mode but it is within acceptable limits.

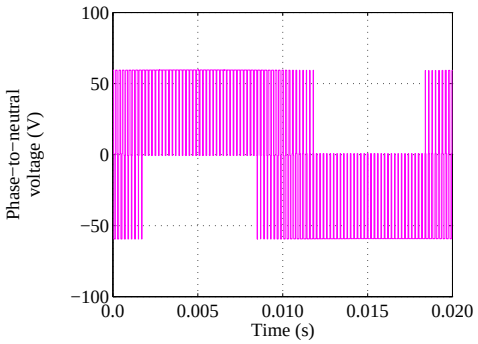
The simulation results show that the REC Z-source NPC inverter, with the modified NTVV modulation algorithm, is able to boost the output line-to-line voltage to a value higher than the available dc supply with sinusoidal output currents.



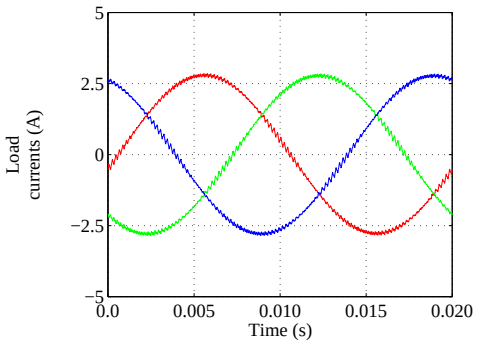

(a) Spectrum of line-to-line voltage, Vab



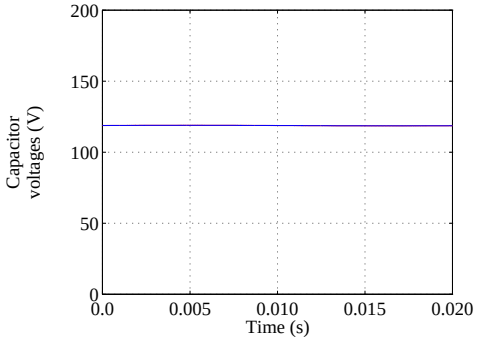

(b) Line-to-line voltage, $V_{ab}$



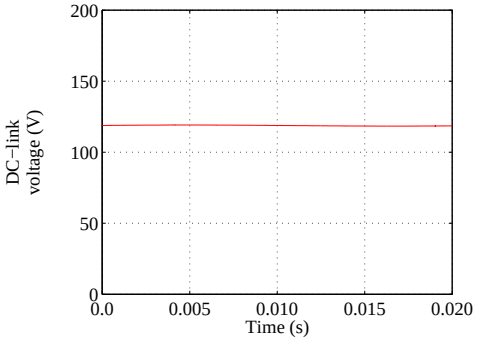

(c) Phase-to-neutral voltage, Vao




(d) Load currents

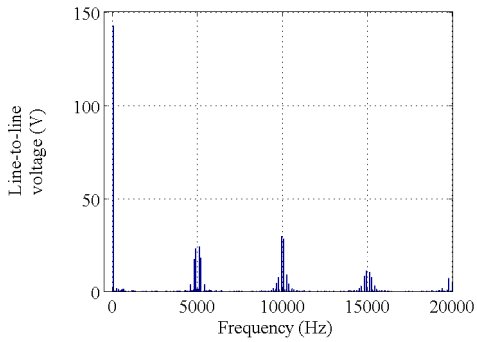



(e) Capacitor voltages, $V_{C_1}$,$V_{C_2}$

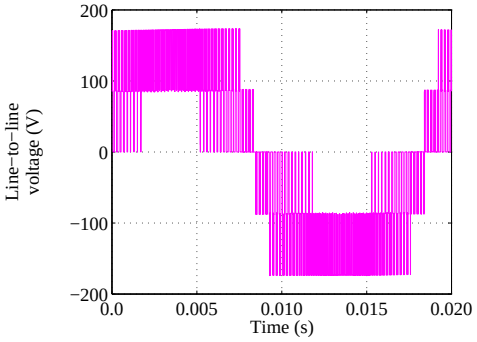



(f) DC-link voltage, $\hat{V}_i$

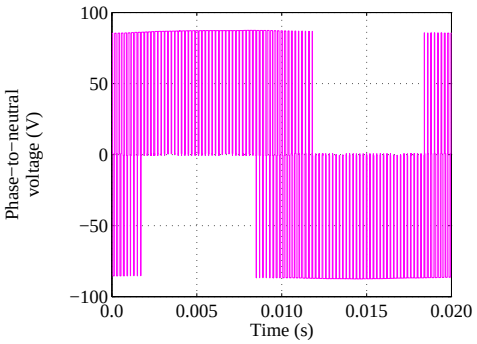
Figure 3.10: Simulation results of the three-level Z-source NPC inverter in an ULST operating mode with $m_I = 0.825$, $T_{ulst}/T_{sw} = 0.0$



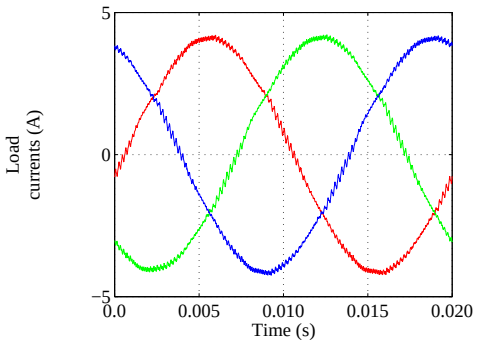

(a) Spectrum of line-to-line voltage, Vab



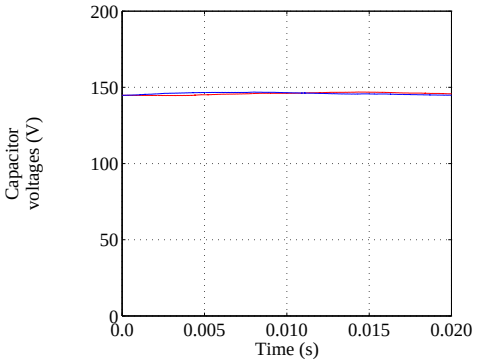

(b) Line-to-line voltage, $V_{ab}$



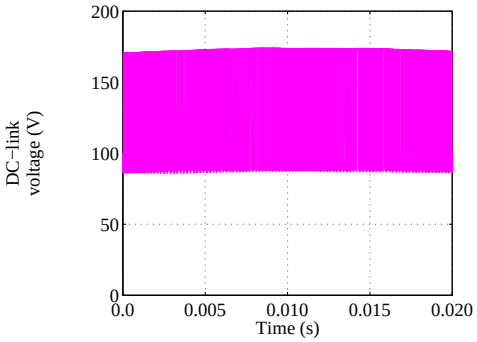

(c) Phase-to-neutral voltage, Vao




(d) Load currents




(e) Capacitor voltages, $V_{C_1}$,$V_{C_2}$




(f) DC-link voltage, $\hat{V}_i$

Figure 3.11: Simulation results of the three-level Z-source NPC inverter in an ULST operating mode with $m_I = 0.825$, $T_{ulst}/T_{sw} = 0.3$

## 3.7 Conclusions

In this chapter, the operating principles and two novel modified SVM techniques for the Z-source NPC inverter have been reviewed. Using carefully inserted upper and lower shoot-through states in the conventional NPC inverter state sequence, the Z-source NPC inverter functions with the correct volt-second average and voltage boosting capability regardless of the angular position of the reference vector. In both SVM techniques presented, the insertion of shoot-through states is implemented in such a way that the number of device commutations is kept at a minimum during a sampling period, similar to that needed by a conventional NPC inverter. Simulation results have been used throughout to verify the presented concepts.

From the simulation results it is noted that the NTV SVM technique presents better output waveform quality with both the phase and line-to-line voltages having adjacent level switching and the output currents having a very low THD value (1.2%) for both the non-boost and boost modes of operation. The NTVV SVM technique however presents output phase and line-to-line voltages that have got more high-frequency distortions (no adjacent level switching) and inferior output current quality (THD = 2.3%) for the non-boost mode of operation. The output current quality deteriorates (THD = 2.8%) during the boost mode when shoot-through states are inserted. The NTV SVM is therefore superior to NTVV SVM for controlling the Z-source NPC inverter.

# Chapter 4

# Two-Stage Direct AC-AC Power Converter

## 4.1 Introduction

This chapter introduces the two-stage matrix converter. The advantages of using the two-stage matrix converter approach over the conventional matrix converter are discussed. Also, the bi-directional switch arrangement, current commutation techniques, modulation techniques and protection issues of the two-stage matrix converter are explained in detail. In addition, a comparison between the two-stage matrix converter and the conventional matrix converter is given. Finally, simulation results of the two-stage matrix converter are presented to show the operation of the topology.

## 4.2 Conventional matrix converter

### 4.2.1 Overview

The matrix converter concept was first introduced in the early 1970s with the pioneering work of L. Gyugi and B. Pelly on 'Static Power Frequency Changer' followed by their publication in 1976 [74]. The matrix converter is a direct ac-to-ac power converter which uses an array of $m$ x $n$ controlled bi-directional switch cells to connect each of the $m$ input lines to each of the $n$ output lines. The ability of the bi-directional switch cell to conduct current in both directions and block voltage of both polarities enables an $m$ x $n$ matrix converter to generate an $n$-phase variable output voltage with unrestricted frequency from an $m$-phase ac supply voltage without using any intermediate energy storage elements. The circuit is also known as the "single-stage" or "direct" matrix converter since it converts ac-to-ac in one stage. The basic circuit diagram of a conventional *3* x *3* matrix converter is shown in figure 4.1.

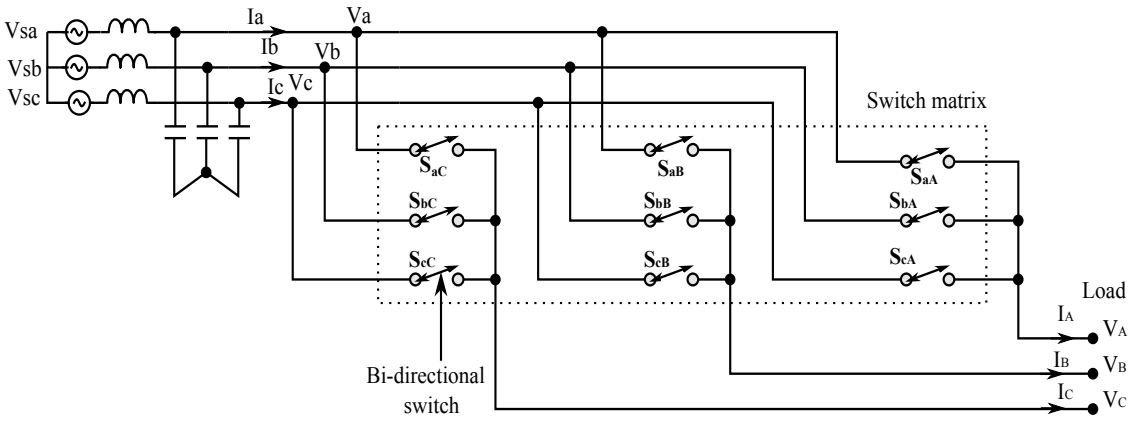



Figure 4.1: Conventional three-phase to three-phase matrix converter

The conventional *3* x *3* matrix converter has been extensively researched due to its potential as a substitute for the traditional ac-dc-ac converter in ac motor drives, especially in aerospace applications [75]. Some of the benefits provided by the matrix converter are as follows:

i. Sinusoidal input and output currents

ii. Adjustable input displacement factor, irrespective of the load conditions

iii. Inherent bi-directional power flow

iv. Generation of variable frequency and variable voltage to the load

v. Possibility of high power density due to minimum use of passive components.

However, the matrix converter has the following disadvantages. The converter needs eighteen power semiconductor devices for its operation thereby increasing the cost and complexity of the converter. The maximum undistorted load voltage which it can provide is limited to 86.6% of the supply voltage. Therefore, the use of the matrix converter to drive standard voltage motors will result in reduced flux due to lower voltages. This reduces the torque at rated current. The absence of any energy storage in the main power conversion makes the matrix converter sensitive to grid disturbances such as unbalanced voltages, harmonics, sags, etc.

In the recent past most of the practical difficulties in implementing the matrix converter have been solved [13]. In this section only the operating principles and modulation schemes for the *3* x *3* matrix converter are reviewed, which is sufficient to understand the derivation of the two-stage matrix converter topology.

As shown in figure 4.1, the matrix converter is normally fed by a voltage source and, for this reason, the input terminals should not be short circuited. If the switches cause a short circuit between the input voltage sources, infinite current flows through the switches and damages the circuit. On the other hand, the load has typically an inductive nature and, for this reason, an output phase must not be left open. If any output terminal is open-circuited, the voltage across the inductor and consequently across the switches is infinite thereby damaging the switches as a result of the over-voltage.

### 4.2.2 Mathematical model

The *3* x *3* matrix converter will form the basis of the discussion in this subsection but the basic idea can be extended to the general $m$ x $n$ matrix converter by simply adding more bi-directional switch cells. In the following, lower case suffixes denote the input phases and upper case suffixes denote the output phases as shown in figure 4.1.

Assuming ideal switching, a mathematical model for the topology in figure 4.1 can be derived using the concept of switching functions [18]. The switching function, $S_{ij}$, for the switch connecting input line $i$ to output line $j$, is defined to be '1' when the switch is on and '0' when the switch is off. The instantaneous voltage and current relationships can then be written as given in (4.1) and (4.2) respectively.

$$\begin{bmatrix} v_A(t) \\ v_B(t) \\ v_C(t) \end{bmatrix} = \begin{bmatrix} S_{aA}(t) & S_{bA}(t) & S_{cA}(t) \\ S_{aB}(t) & S_{bB}(t) & S_{cB}(t) \\ S_{aC}(t) & S_{bC}(t) & S_{cC}(t) \end{bmatrix} \begin{bmatrix} v_a(t) \\ v_b(t) \\ v_c(t) \end{bmatrix} \tag{4.1}$$

$$\begin{bmatrix} i_a(t) \\ i_b(t) \\ i_c(t) \end{bmatrix} = \begin{bmatrix} S_{aA}(t) & S_{aB}(t) & S_{aC}(t) \\ S_{bA}(t) & S_{bB}(t) & S_{bC}(t) \\ S_{cA}(t) & S_{cB}(t) & S_{cC}(t) \end{bmatrix} \begin{bmatrix} i_A(t) \\ i_B(t) \\ i_C(t) \end{bmatrix} \tag{4.2}$$

Due to the lack of free-wheeling diodes in the matrix converter configuration there is a fundamental restriction on the permissible switching combinations. Short circuits of the capacitive input and open circuits of the inductive output must be avoided. This means that at any instant one and only one switch on each output phase must be closed. This is stated in a switching function in (4.3).

$$S_{aj} + S_{bj} + S_{cj} = 1, \qquad j\epsilon\{A, B, C\} \tag{4.3}$$

With these restrictions, the *3* x *3* matrix converter has twenty-seven valid switching states [18]. For the following analysis, it is assumed that (4.3) is obeyed and the commutation between switches is instantaneous. Equations (4.1) and (4.2) give the

instantaneous relationship between input and output quantities. To derive modulation rules, it is also necessary to consider the switching pattern that is employed. This typically follows a form similar to that shown in figure 4.2.

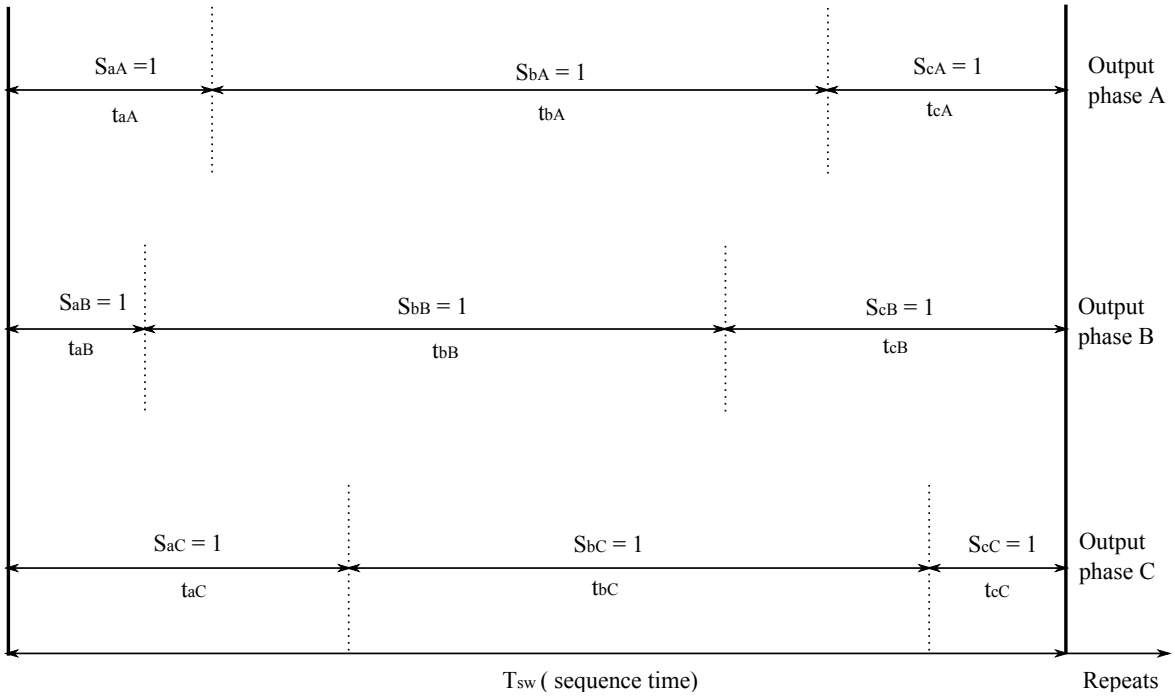



Figure 4.2: General form of switching pattern

To determine the average behaviour of the converter at output frequencies well below the switching frequency a modulation duty cycle can be defined for each switch. Let $m_{kj}$(t) be the duty cycle of switch $S_{kj}$, defined as $m_{kj}$(t) = $t_{kj}/T_{sw}$, which can have the following values:

$$0 < m_{kj} < 1 \qquad k\{a,b,c\}, \qquad j\{A,B,C\}. \tag{4.4}$$

The low-frequency transfer matrix is defined by

$$M(t) = \begin{bmatrix} m_{aA}(t) & m_{bA}(t) & m_{cA}(t) \\ m_{aB}(t) & m_{bB}(t) & m_{cB}(t) \\ m_{aC}(t) & m_{bC}(t) & m_{cC}(t) \end{bmatrix}. \tag{4.5}$$

The low-frequency components of the output phase voltage and input current are

given by (4.6) and (4.7), respectively.

$$\begin{bmatrix} v_A(t) \\ v_B(t) \\ v_C(t) \end{bmatrix} = \begin{bmatrix} m_{aA}(t) & m_{bA}(t) & m_{cA}(t) \\ m_{aB}(t) & m_{bB}(t) & m_{cB}(t) \\ m_{aC}(t) & m_{bC}(t) & m_{cC}(t) \end{bmatrix} \begin{bmatrix} v_a(t) \\ v_b(t) \\ v_c(t) \end{bmatrix} \tag{4.6}$$

$$\begin{bmatrix} i_a(t) \\ i_b(t) \\ i_c(t) \end{bmatrix} = \begin{bmatrix} m_{aA}(t) & m_{aB}(t) & m_{aC}(t) \\ m_{bA}(t) & m_{bB}(t) & m_{bC}(t) \\ m_{cA}(t) & m_{cB}(t) & m_{cC}(t) \end{bmatrix} \begin{bmatrix} i_A(t) \\ i_B(t) \\ i_C(t) \end{bmatrix} \tag{4.7}$$

Various modulation strategies have been proposed and each derived modulation strategy defines the values of each element ($m_{kj}$(t)) within (4.5) differently. In the following subsection, the popular modulation strategies that have been proposed for the conventional matrix converter will be briefly reviewed in order to facilitate the explanation of the derivation of the two-stage matrix converter topology.

### 4.2.3 Modulation techniques for the direct matrix converter

#### 4.2.3.1 The modulation problem and basic solution

The modulation problem normally considered for the matrix converter can be stated as follows. Given a set of input voltages, $v_{in}$(t), and an assumed set of output currents, $i_{out}$(t):

$$v_{in}(t) = V_{im} \cdot \begin{bmatrix} \cos(\omega_i t) \\ \cos(\omega_i t + \frac{2\pi}{3}) \\ \cos(\omega_i t + \frac{4\pi}{3}) \end{bmatrix}, \qquad i_{out}(t) = I_{om} \cdot \begin{bmatrix} \cos(\omega_o t + \phi_o) \\ \cos(\omega_o t + \phi_o + \frac{2\pi}{3}) \\ \cos(\omega_o t + \phi_o + \frac{4\pi}{3}) \end{bmatrix} \tag{4.8}$$

find a modulation matrix M(t) such that

$$v_{out}(t) = qV_{im} \cdot \begin{bmatrix} \cos(\omega_o t) \\ \cos(\omega_o t + \frac{2\pi}{3}) \\ \cos(\omega_o t + \frac{4\pi}{3}) \end{bmatrix}, \qquad i_{in}(t) = q\cos(\phi_o) I_{om} \cdot \begin{bmatrix} \cos(\omega_i t + \phi_i) \\ \cos(\omega_i t + \phi_i + \frac{2\pi}{3}) \\ \cos(\omega_i t + \phi_i + \frac{4\pi}{3}) \end{bmatrix} \tag{4.9}$$

and that the constraint equation (4.3) is satisfied. In (4.9), $q$ is the voltage transfer ratio, $\omega_i$ and $\omega_o$ are the input and output frequencies and $\phi_i$ and $\phi_o$ are the input and output phase displacement angles, respectively. There are two basic solutions to this problem which were derived by Venturini [76, 77]:

$$[M1(t)] = \frac{1}{3}\begin{bmatrix} 1+2q\cos(\omega_m t) & 1+2q\cos(\omega_m t-\frac{2\pi}{3}) & 1+2q\cos(\omega_m t-\frac{4\pi}{3}) \\ 1+2q\cos(\omega_m t-\frac{4\pi}{3}) & 1+2q\cos(\omega_m t) & 1+2q\cos(\omega_m t-\frac{2\pi}{3}) \\ 1+2q\cos(\omega_m t-\frac{2\pi}{3}) & 1+2q\cos(\omega_m t-\frac{4\pi}{3}) & 1+2q\cos(\omega_m t) \end{bmatrix}, \tag{4.10}$$

with $\omega_m$ = ($\omega_o$ - $\omega_i$)

$$[M2(t)] = \frac{1}{3}\begin{bmatrix} 1+2q\cos(\omega_m t) & 1+2q\cos(\omega_m t-\frac{2\pi}{3}) & 1+2q\cos(\omega_m t-\frac{4\pi}{3}) \\ 1+2q\cos(\omega_m t-\frac{2\pi}{3}) & 1+2q\cos(\omega_m t-\frac{4\pi}{3}) & 1+2q\cos(\omega_m t) \\ 1+2q\cos(\omega_m t-\frac{4\pi}{3}) & 1+2q\cos(\omega_m t) & 1+2q\cos(\omega_m t-\frac{2\pi}{3}) \end{bmatrix}, \tag{4.11}$$

with $\omega_m$ = -($\omega_o$ - $\omega_i$)

The solution in (4.10) yields $\phi_i = \phi_o$, giving the same phase displacement at the input and output of the converter, whereas the solution in (4.11) yields $\phi_i$ = -$\phi_o$, giving reversed phase displacement at the input. Combining the two solutions provides the means for input displacement factor control.

$$M(t) = \alpha_1 \cdot M_1(t) + \alpha_2 \cdot M_2(t) \tag{4.12}$$

where $\alpha_1 + \alpha_2 = 1$.

Setting $\alpha_1 = \alpha_2$ gives unity input displacement factor regardless of the load displacement factor. Other possibilities exist, through the choice of $\alpha_1$ and $\alpha_2$, to have a leading displacement factor (capacitive) at the input with lagging displacement factor (inductive) load at the output and vice versa.

This basic solution represents a direct transfer function approach and is characterised by the fact that, during each switching period ($T_{sw}$), the average output voltage is equal to the demand output voltage, $v_{out}$(t). For this to be possible the demand output voltages must fit within the input voltage envelope for all operating conditions.

Using this solution the maximum value of input to output voltage ratio ($q$) that the converter can achieve is 50%.

An improvement in the achievable voltage transfer ratio to 86.6% is possible by adding common-mode voltages to the demand output voltages as shown in (4.13).

$$v_{out}(t) = qV_{im} \cdot \begin{bmatrix} \cos(\omega_o t) - \frac{1}{6}\cos(3\omega_o t) + \frac{1}{2\sqrt{3}}\cos(3\omega_i t) \\ \cos(\omega_o t + \frac{2\pi}{3}) - \frac{1}{6}\cos(3\omega_o t) + \frac{1}{2\sqrt{3}}\cos(3\omega_i t) \\ \cos(\omega_o t + \frac{4\pi}{3}) - \frac{1}{6}\cos(3\omega_o t) + \frac{1}{2\sqrt{3}}\cos(3\omega_i t) \end{bmatrix} \tag{4.13}$$

The common-mode voltages have no effect on the output line-to-line voltages, but allow the demand output voltages to fit within the input voltage envelope with a value of $q$ up to 86.6% [78].

#### 4.2.3.2 Venturini modulation methods

The first method attributable to Venturini [76, 77] is defined by (4.10) and (4.11). However, calculating the switch timings directly from these equations is cumbersome for a practical implementation. They are more conveniently expressed directly in terms of the input voltages and the demand output voltages (assuming unity displacement factor) in the form of (4.14).

$$m_{kj} = \frac{t_{kj}}{T_{sw}} = \frac{1}{3}\left[1 + \frac{2v_k v_j}{v_{im}}^2\right], \qquad k\epsilon\{a,b,c\}, \qquad j\epsilon\{A,B,C\}. \tag{4.14}$$

This method is ideally suited for real time implementation but it is of little practical significance because of the 50% voltage transfer ratio limitation.

Venturini's optimum method [79, 80] employs the common-mode addition technique defined in (4.13) to achieve a maximum voltage transfer ratio of 86.6%. The output voltage demand waveforms now make full use of the input voltage envelope. The common-mode voltages will cancel out in a three-phase load in the same way as they do with common-mode addition in a conventional inverter. To achieve this, the target

output voltages in (4.9) are modified to those given in (4.13). It must be noted that for a matrix converter, the common-mode voltages of both the input and output frequencies are added to achieve the optimum output. If unity displacement factor is required, it has been shown in [80] that the equation given in (4.14) becomes:

$$m_{kj} = \frac{t_{kj}}{T_{sw}} = \frac{1}{3}\left[1 + \frac{2v_k v_j}{v_{im}}^2 + \frac{4q}{3\sqrt{3}}\sin(\omega_i t + \beta_k)\sin(3\omega_i t)\right], \tag{4.15}$$

for $k \,\epsilon\, \{a, b, c\}$ and $j \,\epsilon\, \{A, B, C\}$
$\beta_k \,\epsilon\, \left\{0, \frac{2\pi}{3}, \frac{4\pi}{3}\right\}$ for $k \,\epsilon\, \{a, b, c\}$, respectively.

Note that, in (4.15), the demand output voltages $v_j$ include the common-mode addition defined in (4.13). Equation (4.15) provides the basis for real-time implementation of the optimum amplitude Venturini method which is readily handled by microprocessors up to switching frequencies of tens of kilohertz. Input displacement factor control can be introduced into the formulation in (4.15) by inserting a phase shift between the measured input voltages and the voltages, $v_k$, inserted into (4.15). However, it should be noted that the output voltage limit reduces from $0.866V_{im}$ for input displacement factors other than unity.

#### 4.2.3.3 Scalar modulation methods

The scalar modulation method of Roy [81] is based on the idea of calculating the switch actuation signals directly from measurements of the instantaneous input voltages and comparing their relative magnitudes following the algorithm below:

I) Assign subscript $M$ to the input which has a different polarity to the other two inputs.

II) Assign subscript $L$ to the smallest (absolute) of the other two inputs. The third input is assigned subscript $K$.

The modulation duty cycles are then given by:

$$\begin{aligned} m_{Lj} &= \frac{(v_j - v_M)v_L}{1.5V_{im}^2} \\ m_{Kj} &= \frac{(v_j - v_M)v_K}{1.5V_{im}^2} \\ m_{Mj} &= 1 - (m_{Lj} + m_{Kj}), \end{aligned} \tag{4.16}$$

for $j\epsilon\{A, B, C\}$.

Again, common-mode addition is used with the demand voltages $v_j$ to achieve 86.6% voltage ratio capability. Despite the apparent differences, this method yields virtually identical switch timings to the optimum Venturini method. Expressed in the form of (4.15), the modulation duty cycles for the scalar method are given in (4.17)

$$m_{kj} = \frac{t_{kj}}{T_{sw}} = \frac{1}{3}\left[1 + \frac{2v_k{v_j}^2}{v_{im}} + \frac{2}{3}\sin(\omega_i t + \beta_k)\sin(3\omega_i t)\right]. \tag{4.17}$$

for $k\,\epsilon\,\{a, b, c\}$ and $j\,\epsilon\,\{A, B, C\}$
$\beta_k\,\epsilon\left\{0, \frac{2\pi}{3}, \frac{4\pi}{3}\right\}$ for $k\,\epsilon\,\{a, b, c\}$, respectively.

At maximum output voltage ($q = \sqrt{3}/2$), (4.15) and (4.17) are identical. The only difference between the methods is that the right most term is used in conjunction with $q$ in the Venturini method and is fixed at its maximum value in the scalar method. The effect on output voltage is negligible except at low switching frequencies where the Venturini method is superior.

#### 4.2.3.4 SVM methods

The SVM method is well known in conventional PWM inverters and has its roots in the "space phasor" method of representing and analysing three-phase machines. This method of analysis is particularly popular with workers in the area of field orientated (or vector) control since it allows visualisation of the spatial and time relationships between the resultant current and flux vectors (or space phasors) in various reference frames. The SVM method was first used with matrix converters in [82] where a new

PWM control technique of forced commutated cycloconverters was introduced based on the space vector representation of the voltages in the complex plane. With a matrix converter, the SVM can be applied to the output voltage and input current control. A comprehensive discussion of the SVM and its relationship to other methods is provided in [82]. Here, we just consider output voltage control to establish the basic principles.

The voltage space vector of the demand output voltages is defined in terms of the line-to-line voltages by (4.18).

$$\vec{V}_{out}(t) = \frac{2}{3}(v_{AB} + v_{BC} \cdot e^{j2\pi/3} + v_{CA} \cdot e^{j4\pi/3}) \tag{4.18}$$

In the complex plane, $\vec{V}_{out}(t)$ is a vector of constant length ($qV_{im}\sqrt{3}$) rotating at angular frequency $\omega_o$. The basis of the SVM technique is that the possible output voltages for the converter (for each permissible switching state) are expressed in the same form as (4.18). At each sampling instant, the position of $\vec{V}_{out}(t)$ is compared with the possible vectors and the desired output voltage is synthesized by time averaging (within the switching interval) between adjacent vectors to give the correct mean voltage. This is a relatively simple process for conventional dc-link inverter since there are only eight possible switching states. Two of these give zero volts (termed zero vectors) and the others are at the vertices of a regular hexagon. The locations and length of the possible output space vectors are fixed in the case of a dc-link inverter. The situation with a matrix converter is more complex since there are twenty-seven possible switching states and the input voltages are time varying.

The twenty-seven possible switching states for a *3* x *3* matrix converter can be classified with the following characteristics.

- *Group I*: Each output line is connected to a different input line. Output space vectors are constant in amplitude, rotating (in either direction) at the supply angular frequency.
- *Group II*: Two output lines are connected to a common input line; the remaining

output line is connected to one of the other input lines. Output space vectors have varying amplitude and fixed direction occupying one of six positions regularly spaced 60 ° apart. The maximum length of these vectors is $2/\sqrt{3}V_{env}$ where $V_{env}$ is the instantaneous value of the rectified input voltage envelope.

- *Group III*: All output lines are connected to a common input line. Output space vectors have zero amplitude (i.e., located at the origin).

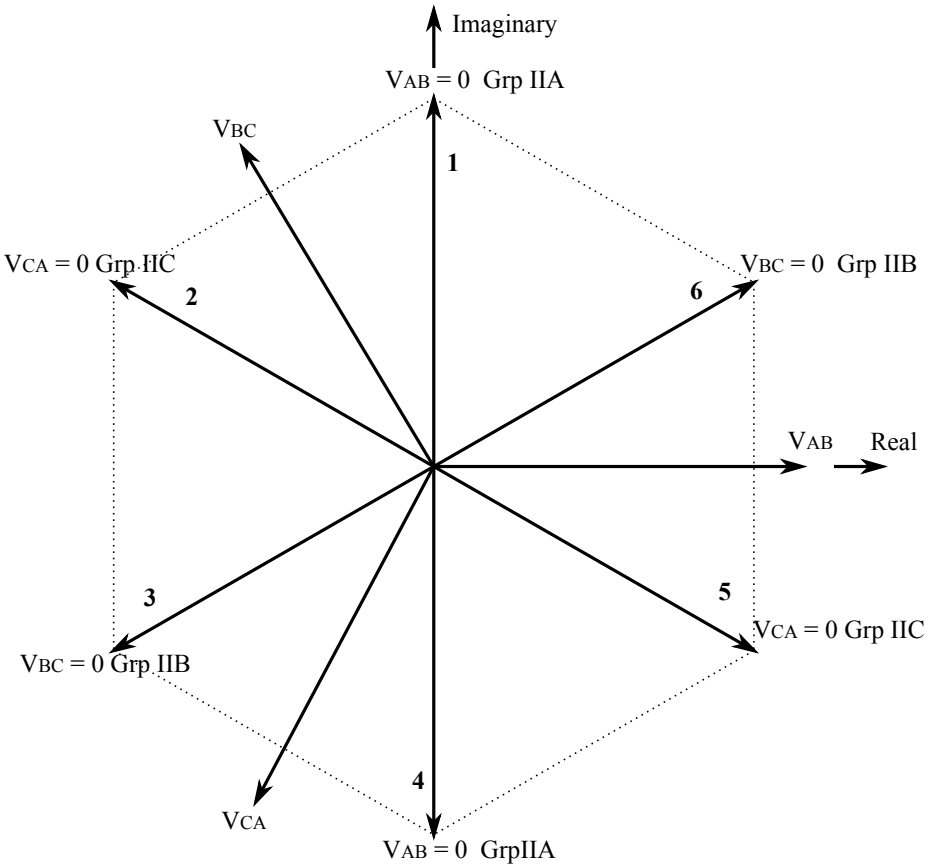



Figure 4.3: Output voltage space vectors

The method used to select the vectors to produce the desired output vector at each sampling instant is not unique. A simple method is described here. Other more complex methods, giving better performance are possible [83] but the underlying concept is the same.

SVM usually does not use the Group I vectors due to the time variation of their

positions. The desired output is synthesized from Group II active vectors and the Group III zero vectors. The hexagon of possible output vectors is shown in figure 4.3, where Group II vectors are further sub-divided dependent on which output line-to-line voltage is zero.

Figure 4.4 shows an example of how $\vec{V}_{out}(t)$ could be synthesized when it lies in the sextant between vector 1 and vector 6. $\vec{V}_{out}(t)$ is generated through time averaging by choosing the time spent in vector 1 ($t_1$) and vector 6 ($t_6$) during the switching period. Here, it is assumed that the maximum length vectors are used, although that does not have to be the case. From figure 4.4, the relationship in (4.19) is found

$$\begin{aligned} t_1 &= \frac{|V_{out}|}{V_{env}} T_{sw} \sin(\theta_{out}) \\ t_6 &= \frac{|V_{out}|}{V_{env}} T_{sw} \sin(\frac{\pi}{3} - \theta_{out}) \\ t_0 &= T_{sw} - (t_1 + t_6) \end{aligned} \tag{4.19}$$

where $t_0$ is the time spent in the zero vector (at the origin).

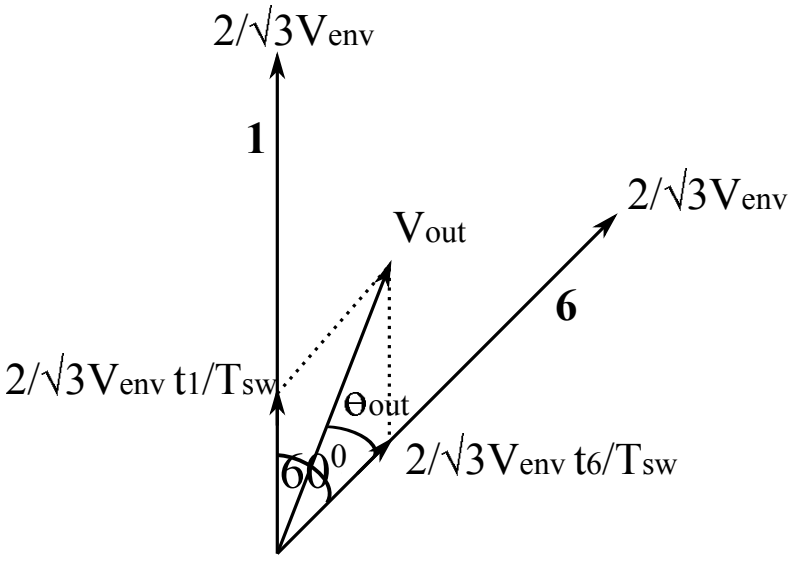



Figure 4.4: Example of output voltage space-vector synthesis

There is no unique way for distributing the times $(t_1, t_6, t_0)$ within the switching period. A method suggested by some authors is to arrange them symmetrically with the zero state in the middle as shown in figure 4.5. However, several variations of the

SVM method have been proposed [83, 84]. These more sophisticated methods take into account the desired input current direction making it possible to draw sinusoidal input currents with controllable displacement factor.

For good harmonic performance at the input and output ports, it is necessary to apply the SVM to input current control and output voltage control. This generally requires four active vectors in each switching period, but the principle is the same. Under balanced input and output conditions, the SVM technique yields similar results to the other methods mentioned earlier. However, the increased flexibility in choice of switching vectors for both input current and output voltage control can yield useful advantages under unbalanced conditions.

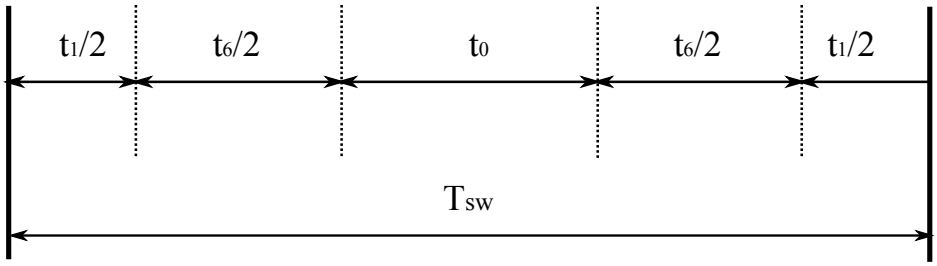



Figure 4.5: Possible way of allocating states within the switching period

#### 4.2.3.5 Indirect modulation methods

These methods aim to increase the maximum voltage ratio above the 86.6% limit of other methods [85, 86]. To do this, the modulation process expressed in terms of output phase voltages defined in (4.9) is expressed in a more compact form (4.20)

$$[\mathbf{v_{out}}(t)] = [\mathbf{M}(t)][\mathbf{v_{in}}(t)] \tag{4.20}$$

and split into two steps as indicated in (4.21)

$$[\mathbf{v_{out}}(t)] = ([\mathbf{A}(t)][\mathbf{v_{in}}(t)])[\mathbf{B}(t)] \tag{4.21}$$

In (4.21), pre-multiplication of the input voltage by $[\mathbf{A}(t)]$ generates a "fictitious dc link" and post-multiplication by $[\mathbf{B}(t)]$ generates the desired output by modulating

the "fictitious dc link". $[\mathbf{A}(t)]$ is generally referred to as the "rectifier transformation" and $[\mathbf{B}(t)]$ as the "inverter transformation" due to the similarity in concept with a traditional rectifier/dc-link/inverter system. $[\mathbf{A}(t)]$ is given by (4.22).

$$[\mathbf{A}(t)] = K_A \begin{bmatrix} \cos(\omega_i t) \\ \cos(\omega_i t + \frac{2\pi}{3}) \\ \cos(\omega_i t + \frac{4\pi}{3}) \end{bmatrix}^T \tag{4.22}$$

Hence,

$$[\mathbf{A}(t)][\mathbf{v_{in}}(t)] = K_A V_{im} \begin{bmatrix} \cos(\omega_i t) \\ \cos(\omega_i t + \frac{2\pi}{3}) \\ \cos(\omega_i t + \frac{4\pi}{3}) \end{bmatrix}^T \begin{bmatrix} \cos(\omega_i t) \\ \cos(\omega_i t + \frac{2\pi}{3}) \\ \cos(\omega_i t + \frac{4\pi}{3}) \end{bmatrix} = \frac{3K_A V_{im}}{2} \tag{4.23}$$

$[\mathbf{B}(t)]$ is given by (4.24)

$$[\mathbf{B}(t)] = K_B \begin{bmatrix} \cos(\omega_o t) \\ \cos(\omega_o t + \frac{2\pi}{3}) \\ \cos(\omega_o t + \frac{4\pi}{3}) \end{bmatrix} \tag{4.24}$$

Hence,

$$[\mathbf{v_{out}}(t)] = ([\mathbf{A}(t)][\mathbf{v_{in}}(t)])[\mathbf{B}(t)] = \frac{3K_A K_B V_{im}}{2} \begin{bmatrix} \cos(\omega_o t) \\ \cos(\omega_o t + \frac{2\pi}{3}) \\ \cos(\omega_o t + \frac{4\pi}{3}) \end{bmatrix} \tag{4.25}$$

From (4.25) the voltage ratio is $q = 3K_A K_B/2$. The steps $[\mathbf{A}(t)]$ and $[\mathbf{B}(t)]$ must be implemented by a suitable choice of switching states. There are many ways of doing this, which are discussed in detail in [85] and [86]. To maximise the voltage ratio, the step $[\mathbf{A}(t)]$ is implemented so that the most positive and most negative input voltages are selected continuously. This yields $K_A = 2\sqrt{3}/\pi$ with a "fictitious dc-link" of $3\sqrt{3}V_{im}/\pi$ (the same as a six-pulse diode bridge with resistive load). $K_B$ represents the modulation index of a PWM process and has the maximum value (square-wave modulation) of $2/\pi$ [85]. The overall voltage ratio $q$ therefore has the maximum value of $6\sqrt{3}/\pi^2 = 105.3\%$.

The voltage ratio obtainable is obviously greater than that of other methods but the improvement is only obtained at the expense of the quality of either the input currents, the output voltages or both. For values of $q > 86.6\%$, the mean output voltage no longer equals the demand output voltage in each switching interval. This inevitably leads to low frequency distortion in the output voltage and/or the input current compared to other methods with $q < 86.6\%$. For $q < 86.6\%$, the indirect method yields very similar results to the direct methods.

## 4.3 Two-stage matrix converter

### 4.3.1 Overview

The two-stage matrix converter consists of a current source rectifier (CSR) at the supply side and a VSI at the load side. The circuit diagram of the two-stage matrix converter is shown in figure 4.6. The rectification stage consists of six bidirectional switches. This stage is implemented as a three-phase to two-phase matrix converter. Each output terminal of the rectification stage is maintained at unipolar voltages, $V_p$ and $V_n$. Therefore, the voltage difference in the two output phases, $V_{pn}$, becomes a variable voltage dc-link.

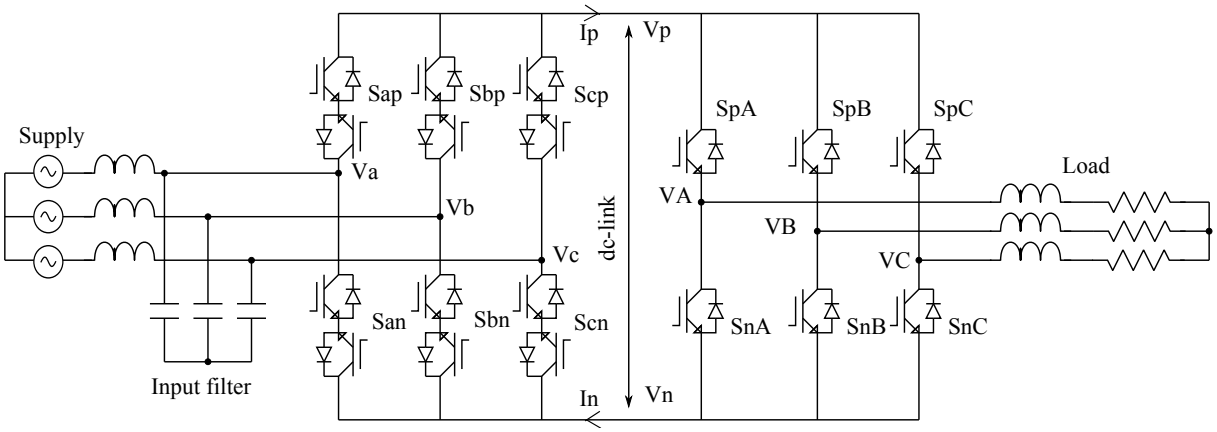



Figure 4.6: Two-stage matrix converter

The inversion stage uses six unidirectional switches with anti-parallel diodes. The function of this stage is similar to a traditional VSI. The inversion stage uses the variable dc-link voltage, $V_{pn}$, to generate the variable amplitude, variable frequency voltage demand for the inductive load.

The two-stage matrix converter uses the same number of semiconductor devices as a conventional matrix converter. The overall transfer function of the two-stage matrix converter can be expressed in the following matrix equations [14]:

$$\begin{bmatrix} V_A \\ V_B \\ V_C \end{bmatrix} = \begin{bmatrix} S_{pA} & S_{nA} \\ S_{pB} & S_{nB} \\ S_{pC} & S_{nC} \end{bmatrix} \begin{bmatrix} V_p \\ V_n \end{bmatrix} \tag{4.26}$$

$$\begin{bmatrix} V_p \\ V_n \end{bmatrix} = \begin{bmatrix} S_{ap} & S_{bp} & S_{cp} \\ S_{an} & S_{bn} & S_{cn} \end{bmatrix} \begin{bmatrix} V_a \\ V_b \\ V_c \end{bmatrix} \tag{4.27}$$

The above equations are similar to (4.1), which shows that the operation of the two-stage matrix converter is similar in principle to the conventional matrix converter using the indirect model. This equivalence is valid only if the switching matrices are equivalent (4.28).

$$\begin{bmatrix} S_{aA} & S_{bA} & S_{cA} \\ S_{aB} & S_{bB} & S_{cB} \\ S_{aC} & S_{bC} & S_{cC} \end{bmatrix} = \begin{bmatrix} S_{pA} & S_{nA} \\ S_{pB} & S_{nB} \\ S_{pC} & S_{nC} \end{bmatrix} \cdot \begin{bmatrix} S_{ap} & S_{bp} & S_{cp} \\ S_{an} & S_{bn} & S_{cn} \end{bmatrix} \tag{4.28}$$

### 4.3.2 SVM for the two-stage matrix converter

Derived from the indirect transfer function approach, the two-stage matrix converter consists of a current source rectification stage and a voltage source inversion stage. The modulation is therefore similar in concept to the indirect SVM for the conventional matrix converter discussed in [18]. A review of the SVM implementation for the two-stage matrix converter is given in the following subsections with reference to the symbols and conventions used in figure 4.6.

#### 4.3.2.1 The rectification stage - input current SVM

The rectification stage can be considered as a *3 x 2* matrix converter. The two output phases should provide a unipolar voltage. A short circuit of the supply lines should also be avoided. Therefore, the safe switching combinations of the rectification stage are limited to nine as shown in table 4.1. Out of the nine possible switching combinations only six, $I_1$ – $I_6$, can produce non-zero currents at the dc-link when a load is connected. The other three are zero switching states, $I_0$. The currents generated by all these switching states can be represented in the complex plane as shown in figure 4.7.

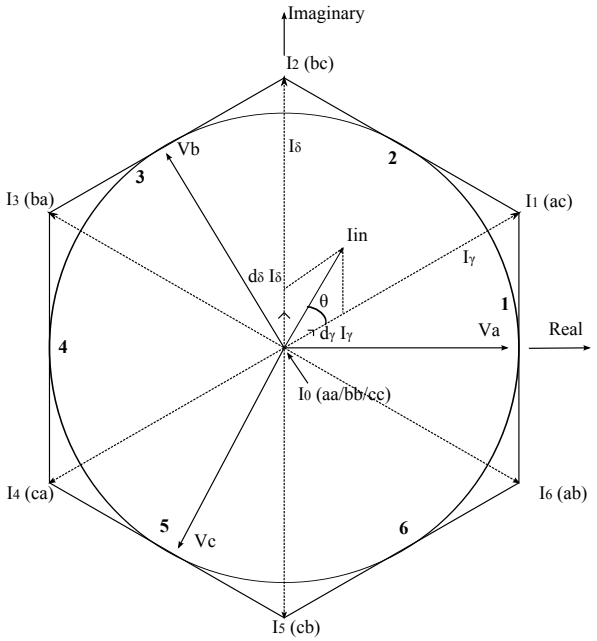



Figure 4.7: Space vector representation of the rectification stage.

The space vector diagram of the rectifier, shown in figure 4.7, is divided into six sectors. The input current reference vector, $\vec{I}_{in}$, can be synthesized by two adjacent active current vectors ($I_\gamma$ and $I_\delta$) and a zero-current vector, $I_0$, in a given sector. The proportion between the two adjacent current vectors gives the direction and the zero current vector controls the magnitude of the reference vector. For a switching period, $T_{sw}$, the input current reference vector $\vec{I}_{in}$ can be synthesized as:

$$\vec{I}_{in} = d_\gamma I_\gamma + d_\delta I_\delta \tag{4.29}$$

where $d_\gamma$ and $d_\delta$ are the duty ratios of the vectors $I_\gamma$ and $I_\delta$, respectively within the switching period. These duty cycles are calculated as follows:

$$\begin{aligned} d_\gamma &= m_R \cdot \sin(\pi/3 - \theta_{in}) \\ d_\delta &= m_R \cdot \sin(\theta_{in}) \end{aligned} \tag{4.30}$$

where $m_R$ is the modulation index of the rectification stage

$$0 \leq m_R = \left(\frac{I_{in}}{I_{pn}}\right) \leq 1 \tag{4.31}$$

and $\theta_{in}$ is the angle of the input reference vector, $\vec{I}_{in}$, within the sector. The duty ratio of the zero current vector, $I_0$, is given as

$$d_{0,rec} = 1 - (d_\gamma + d_\delta). \tag{4.32}$$

| Switch combination | | | | | | dc link | | Symbol |
|---|---|---|---|---|---|---|---|---|
| $S_{ap}$ | $S_{bp}$ | $S_{cp}$ | $S_{an}$ | $S_{bn}$ | $S_{cn}$ | $I_p$ | $I_n$ | |
| 1 | 0 | 0 | 0 | 0 | 1 | $I_a$ | $I_c$ | $I_1(ac)$ |
| 0 | 1 | 0 | 0 | 0 | 1 | $I_b$ | $I_c$ | $I_2(bc)$ |
| 0 | 1 | 0 | 1 | 0 | 0 | $I_b$ | $I_a$ | $I_3(ba)$ |
| 0 | 0 | 1 | 1 | 0 | 0 | $I_c$ | $I_a$ | $I_4(ca)$ |
| 0 | 0 | 1 | 0 | 1 | 0 | $I_c$ | $I_b$ | $I_5(cb)$ |
| 1 | 0 | 0 | 0 | 1 | 0 | $I_a$ | $I_b$ | $I_6(ab)$ |
| 1 | 0 | 0 | 1 | 0 | 0 | $I_a$ | $I_a$ | $I_0(aa)$ |
| 0 | 1 | 0 | 0 | 1 | 0 | $I_b$ | $I_b$ | $I_0(bb)$ |
| 0 | 0 | 1 | 0 | 0 | 1 | $I_c$ | $I_c$ | $I_0(cc)$ |

Table 4.1: Available switching state combinations of the rectification stage

#### 4.3.2.2 Elimination of zero current vectors in the rectification stage

During the zero voltage switching states, the load currents circulate through the inversion stage. Therefore, the dc-link current which is delivered by the rectification stage becomes zero. If the rectification stage switching coincides with the inverter stage zero state, a zero current commutation is possible as proposed in [87]. This technique reduces the switching losses in the rectification stage [88]. In order to use

this technique, it is desired that the zero current vectors are completely eliminated in the rectification stage. This can be done by adjusting the rectification stage duty cycles as follows:

$$\begin{aligned} d_\gamma^R &= \frac{d_\gamma}{d_\gamma + d_\delta} \\ d_\delta^R &= \frac{d_\delta}{d_\gamma + d_\delta} \end{aligned} \tag{4.33}$$

The modulation index of the rectification stage is fixed at $m_R = 1$. This process will ultimately modify the average dc-link voltage over a switching period

$$V_{pn,avg} = d_\gamma^R \cdot V_{l-l\gamma} + d_\delta^R \cdot V_{l-l\delta} \tag{4.34}$$

which varies with time. $V_{l-l\gamma}$ and $V_{l-l\delta}$ are the active input voltage vectors.

#### 4.3.2.3 The inversion stage - output voltage SVM

All the possible switch combinations for the inversion stage and corresponding voltages produced at each output phase are shown in table 4.2. The switching states which can short circuit the dc link are avoided. Therefore, two switches in each output phase, $S_{py}$ and $S_{ny}$ with y $\epsilon \{A, B, C\}$, are operated in compliment to each other.

| Switch combination $S_{pA}$,$S_{pB}$,$S_{pC}$, | Load voltage | | | | | | Symbol |
|---|---|---|---|---|---|---|---|
| | $V_A$ | $V_B$ | $V_C$ | $V_{AB}$ | $V_{BC}$ | $V_{CA}$ | |
| 100 | $V_p$ | $V_n$ | $V_n$ | $V_{pn}$ | 0 | $-V_{pn}$ | $V_1(100)$ |
| 101 | $V_p$ | $V_n$ | $V_p$ | $V_{pn}$ | $-V_{pn}$ | 0 | $V_2(101)$ |
| 001 | $V_n$ | $V_n$ | $V_p$ | 0 | $-V_{pn}$ | $V_{pn}$ | $V_3(001)$ |
| 011 | $V_n$ | $V_p$ | $V_p$ | $-V_{pn}$ | 0 | $V_{pn}$ | $V_4(011)$ |
| 010 | $V_n$ | $V_p$ | $V_n$ | $-V_{pn}$ | $V_{pn}$ | 0 | $V_5(010)$ |
| 110 | $V_p$ | $V_p$ | $V_n$ | 0 | 0 | $V_{pn}$ | $V_6(110)$ |
| 000 | $V_n$ | $V_n$ | $V_n$ | 0 | 0 | 0 | $V_0(000)$ |
| 111 | $V_p$ | $V_p$ | $V_p$ | 0 | 0 | 0 | $V_0(111)$ |

Table 4.2: Allowable switch combination for the inversion stage

According to table 4.2, only six switch combinations can produce non-zero output voltages. The other two switch combinations produce a zero output voltage. Therefore, the resultant demand line-to-line output voltage vector defined by

$$\vec{V}_{out}(t) = \frac{2}{3}\left[V_{AB}(t)e^{j0} + V_{BC}(t)e^{j2\pi/3} + V_{CA}(t)e^{j4\pi/3}\right] \tag{4.35}$$

can use only seven discrete values, $V_0$ to $V_6$. These seven discrete values can be represented by stationary vectors in the complex plane as shown in figure 4.8. The magnitude of each vector is equal to the dc-link voltage, $|V_{pn}|$. The switch combination vectors divide the complex plane into six sectors. In the complex plane, the demand line-to-line output voltage, $V_{out}$, is a vector of constant length rotating at the angular frequency of the load, $\omega_0$.

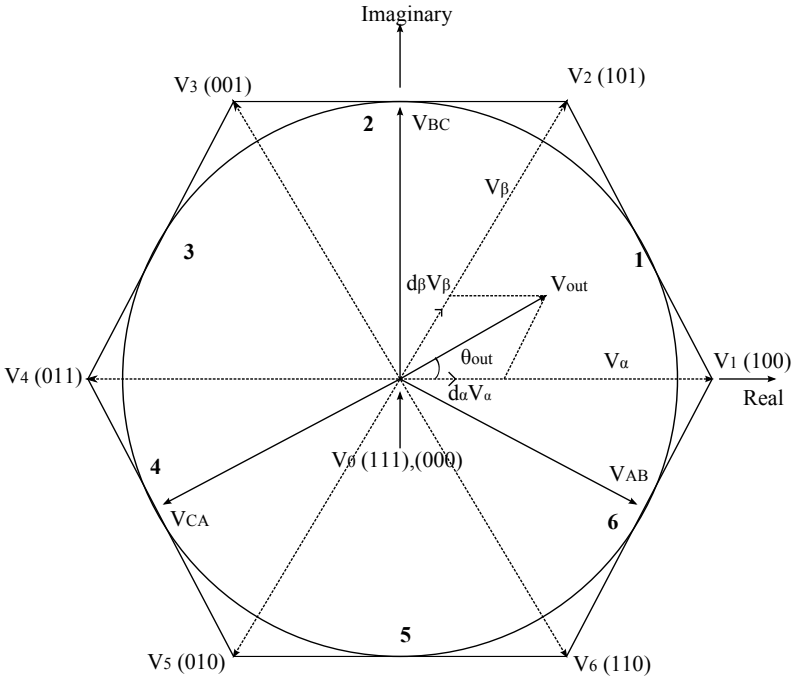



Figure 4.8: Space vector representation for the inversion stage.

The space vector of the desired output voltage

$$V_{out}(t) = \sqrt{3} \cdot V_{om} \cdot e^{j(\omega_0 t - \varphi_0 + \pi/6)} \tag{4.36}$$

can be synthesized by using two adjacent switch combination vectors, $V_1 - V_6$, and a zero voltage vector, $V_0$. This process is shown in figure 4.8, where $\vec{V}_{out}$ is the sampled

value of the desired load voltage at any instant within one switching interval, $T_{sw}$.

$$\vec{V}_{out} = d_\alpha \cdot \vec{V}_\alpha + d_\beta \cdot \vec{V}_\beta \tag{4.37}$$

$\vec{V}_\alpha$ and $\vec{V}_\beta$ are the adjacent switch combination voltage vectors. Therefore, the duty cycles of the adjacent switch combination vectors, $d_\alpha$ and $d_\beta$, can be obtained

$$\begin{aligned} d_\alpha &= m_I \cdot \sin(\pi/3 - \theta_{out}) \\ d_\beta &= m_I \cdot \sin(\theta_{out}) \\ d_{0,inv} &= 1 - (d_\alpha + d_\beta) \end{aligned} \tag{4.38}$$

where, $m_I$ is the modulation index of the inversion stage

$$0 \leq m_I = \left( \frac{\sqrt{3} \cdot V_{om}}{V_{pn}} \right) \leq 1. \tag{4.39}$$

#### 4.3.2.4 Synchronisation of the rectification and inversion stage switching

The modulation of the rectification and inversion stages need to be synchronised to ensure a correct balance of the input currents and the output voltages over a switching period. This is shown in figure 4.9. The synchronisation also allows the alignment of the zero voltage state switching in the inversion stage to coincide with the rectification stage switching. This technique reduces the switching losses in the rectification stage. The output currents are supplied proportionately by the active input current vectors in order to minimise the distortions in the input current. As a result, the switching sequence of the inversion stage becomes a double-sided asymmetric PWM with the sequence: $V_0 - V_\alpha - V_\beta - V_0 - V_\beta - V_\alpha - V_0$.

The demand input current vector $\vec{I}_{in}(\mathrm{t})$ is generated through time averaging by choosing the time spent by $\vec{I}_{in}(\mathrm{t})$ in vector $I_\gamma$ ($t_\gamma$) and vector $I_\delta$ ($t_\delta$) during the switching period. Similarly, the demand output voltage vector $\vec{V}_{out}(\mathrm{t})$ is generated through time averaging by choosing the time spent by $\vec{V}_{out}(\mathrm{t})$ in vector $V_\alpha$ ($t_\alpha$), vector $V_\beta$ ($t_\beta$) and vector $V_0$ ($t_{0,inv}$) during the switching period. From figure 4.9, the relationships in (4.40) and (4.41) are found for the rectification and inversion stages, respectively.

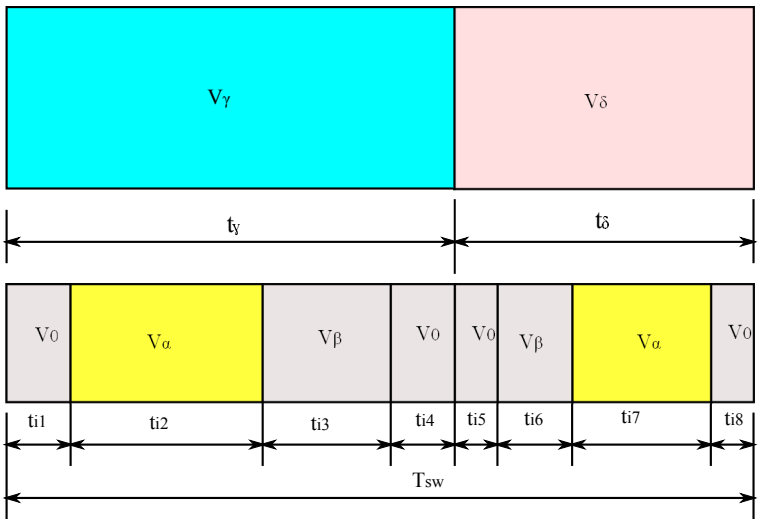



Figure 4.9: Switching sequence of the rectification and inversion stages of the two-stage matrix converter.

Rectification stage:

$$\begin{aligned} t_\gamma &= d_\gamma^R \cdot T_{sw} \\ t_\delta &= d_\delta^R \cdot T_{sw} \\ t_\gamma + t_\delta &= T_{sw} \end{aligned} \tag{4.40}$$

Inversion stage:

$$\begin{aligned} t_\alpha &= d_\alpha \cdot T_{sw} = d_\alpha \cdot (t_\gamma + t_\delta) \\ t_\beta &= d_\beta \cdot T_{sw} = d_\beta \cdot (t_\gamma + t_\delta) \\ t_{0,inv} &= d_{0,inv} \cdot T_{sw} = d_{0,inv} \cdot (t_\gamma + t_\delta) \end{aligned} \tag{4.41}$$

The times spent by the demand output voltage vector $\vec{V}_{out}(\mathrm{t})$ in vectors $V_\alpha$, $V_\beta$ and $V_0$ ($t_\alpha$, $t_\beta$ and $t_{0,inv}$) are then shared in proportion between the times spent by the demand input current vector $\vec{I}_{in}(\mathrm{t})$, $t_\gamma$ and $t_\beta$, so that we have the following relationships:

$$
\begin{aligned}
t_{i1} &= 0.5 \cdot d_{0,inv} \cdot d_{\gamma}^{R} \cdot T_{sw} = 0.5 \cdot d_{0,inv} \cdot t_{\gamma} \\
t_{i2} &= d_{\alpha} \cdot d_{\gamma}^{R} \cdot T_{sw} = d_{\alpha} \cdot t_{\gamma} \\
t_{i3} &= d_{\beta} \cdot d_{\gamma}^{R} \cdot T_{sw} = d_{\beta} \cdot t_{\gamma} \\
t_{i4} &= t_{i1} \\
t_{i5} &= 0.5 \cdot d_{0,inv} \cdot d_{\delta}^{R} \cdot T_{sw} = 0.5 \cdot d_{0,inv} \cdot t_{\delta} \\
t_{i6} &= d_{\beta} \cdot d_{\delta}^{R} \cdot T_{sw} = d_{\alpha} \cdot t_{\delta} \\
t_{i7} &= d_{\alpha} \cdot d_{\delta}^{R} \cdot T_{sw} = d_{\beta} \cdot t_{\delta} \\
t_{i8} &= t_{i5}
\end{aligned}
\tag{4.42}
$$

### 4.3.3 Simulation results

The model of the two-stage matrix converter shown in figure 4.6 has been simulated using SABER®, based on the specification presented in Appendix B. Figure 4.10 shows the waveforms generated by the rectification stage while figure 4.11 shows the waveforms generated by the inversion stage of the two-stage matrix converter using the SVM technique. Figure 4.10(a) shows the input voltages which are balanced. Referring to figure 4.10(b), the input current $i_a$ has significant high frequency distortions. By using a low-pass $LC$ filter, the switching harmonics are filtered out so that a set of sinusoidal, balanced input currents is obtained at the supply side as shown in figure 4.10(c). Due to the zero-current vector cancellation, the dc-link voltage generated by the rectification stage does not contain zero levels so the average value of the dc-link voltage, $V_{pn,avg}$, is not constant as clearly shown in figure 4.10(d).

By building the dc-link voltage with chops of the input line-to-line voltages, the output terminal (line-to-supply neutral) voltage, $V_A$, of the two-stage matrix converter (figure 4.11(a)) is obviously generated with the voltage levels within the envelope of the input voltages. For each switching period, the output terminal voltage consists of two-levels ($V_p$ and $V_n$), which are the input voltages connected to the dc-link. As shown in figure 4.11(b), the inversion stage is able to generate three-level line-to-line output voltages.

Finally, the input (figure 4.10(c)) and output (figure 4.11(c)) current waveforms of the two-stage matrix converter evidently prove the ability to perform sinusoidal input and output operation with the aid of the SVM technique.

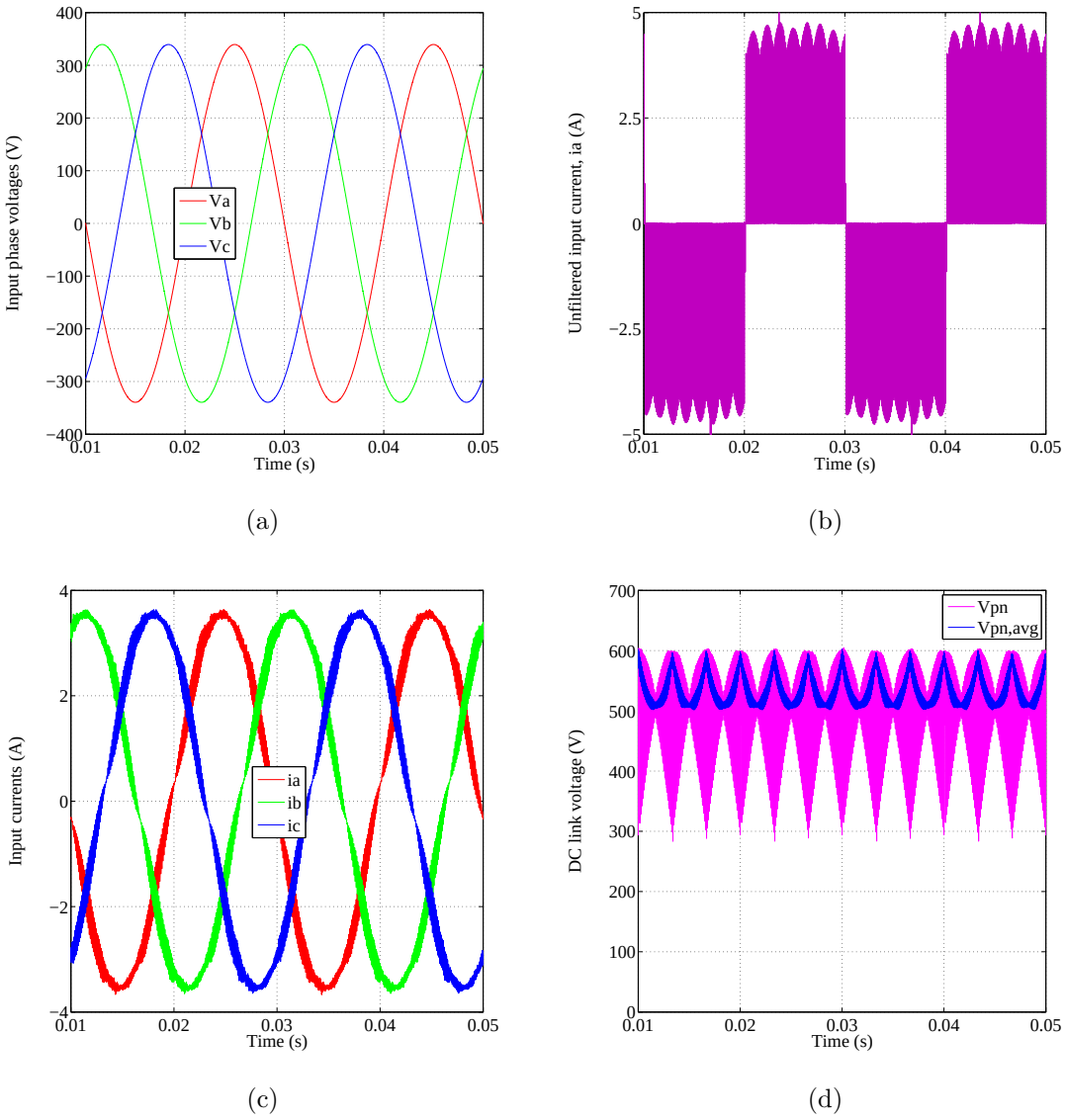



Figure 4.10: Simulation waveforms of the rectification stage of the two-stage matrix converter showing (a) input voltages, (b) unfiltered input current $i_a$, (c) filtered input currents and (d) dc-link voltage

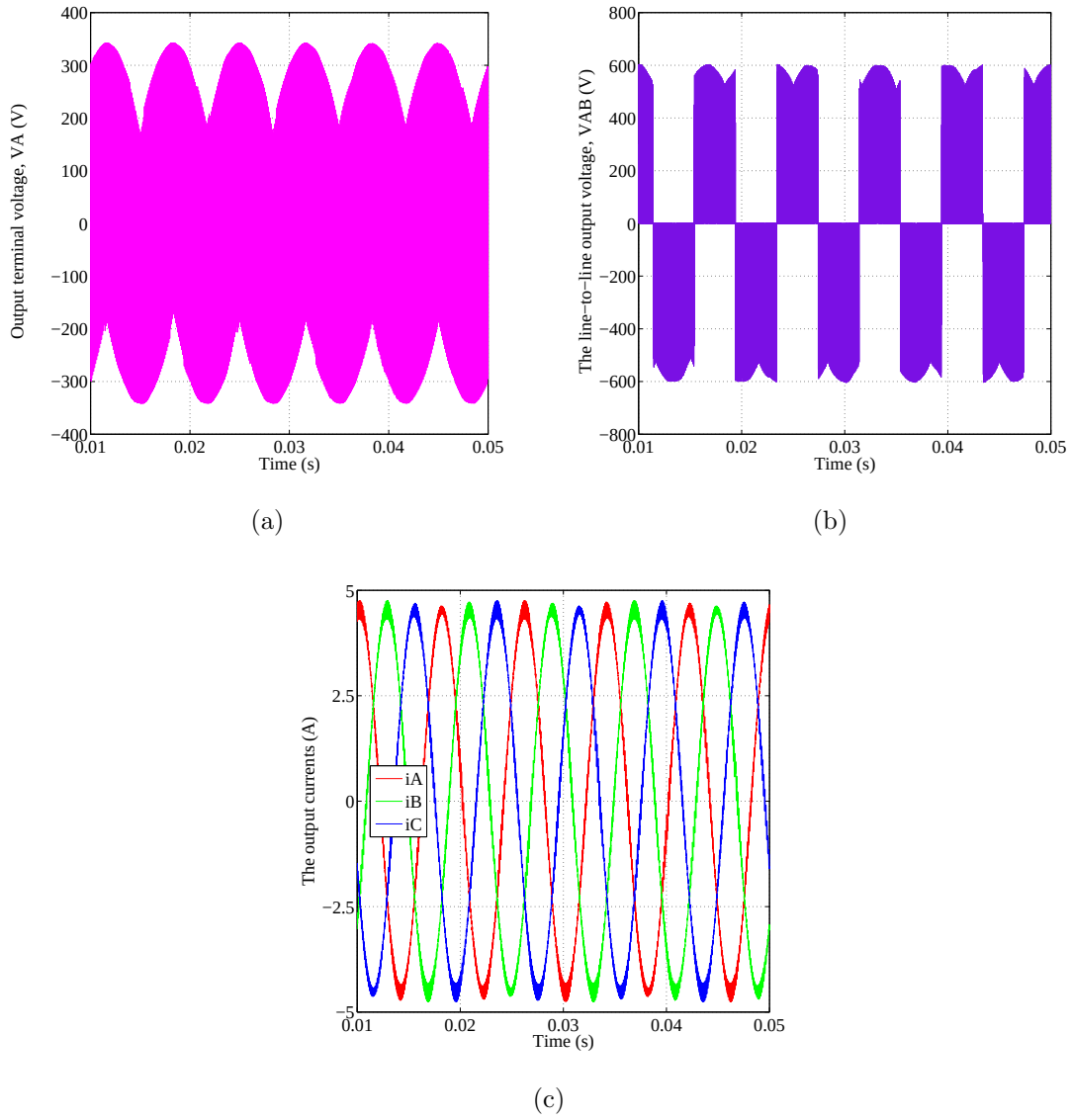



Figure 4.11: Simulation waveforms of the inversion stage of the two-stage matrix converter showing (a) output phase to supply neutral voltage $V_A$, (b) line-to-line voltage $V_{AB}$ and (c) output currents

## 4.4 Bidirectional switch configurations

The matrix converter requires a bidirectional switch capable of blocking voltage and conducting current in both directions. Unfortunately, there are no such devices available that fulfil these needs, so discrete devices need to be used to construct suitable bidirectional switch cells. The choice of bidirectional switches also dictates which current commutation methods can be used. This section describes some possible bidirectional switch configurations and the advantages and disadvantages of each arrangement. In the discussion below it has been assumed that the switching device would be an IGBT, but other devices such as MOSFETs, MCTs and IGCTs can be used in the same way.

### 4.4.1 Diode bridge bidirectional switch cell

The most simple bidirectional switch arrangement is the diode bridge switch cell. This arrangement consists of an IGBT at the centre of a single-phase diode bridge arrangement and is shown in figure 4.12.

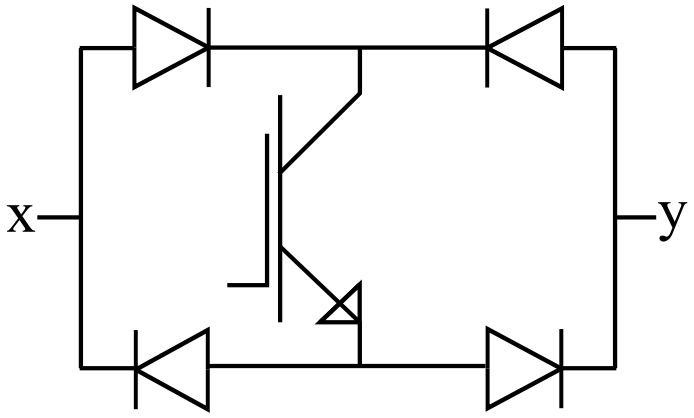



Figure 4.12: Diode bridge bidirectional switch

The main advantage of this arrangement is that only one active device is needed, reducing the cost of the power circuit and the complexity of the control/gate drive circuits. Conduction losses are relatively high since there are three devices in each

conduction path. The direction of the current through the switch cannot be controlled. This is a disadvantage, as many of the advanced commutation techniques described later rely on independent control of the current in each direction.

### 4.4.2 Common-emitter bidirectional switch cell

This switch arrangement consists of two diodes and two IGBTs connected in anti-parallel as shown in figure 4.13. The diodes are included to provide the reverse blocking capability. There are several advantages in using this arrangement when compared with the diode bridge switch cell. The first is that it is possible to independently control the direction of the current. Conduction losses are also reduced since only two switches carry the current at any one time. One possible disadvantage is that each bidirectional switch cell requires an isolated power supply for the gate drives.

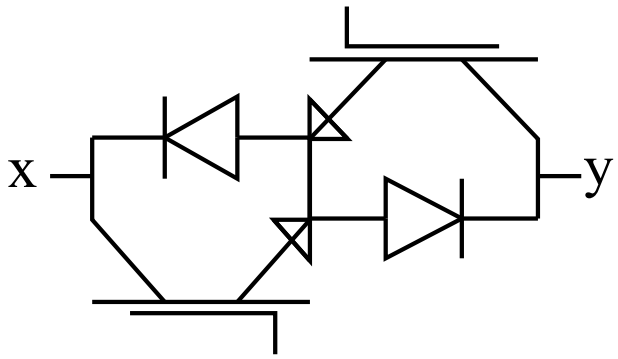



Figure 4.13: Common-emitter bidirectional switch

### 4.4.3 Common-collector bidirectional switch cell

This arrangement is similar to the previous one but the IGBTs are arranged in a common collector configuration as shown in figure 4.14. The conduction losses are the same as the common emitter configuration. A possible advantage of the common collector configuration is that only six isolated power supplies are needed to supply the

gate drive signals of a *3 x 3* matrix converter. However, in practice, other constraints such as the need to minimize stray inductance mean that operation with only six isolated supplies is generally not viable. Therefore, the common emitter configuration is generally preferred for creating the matrix converter bidirectional switch cells [13].

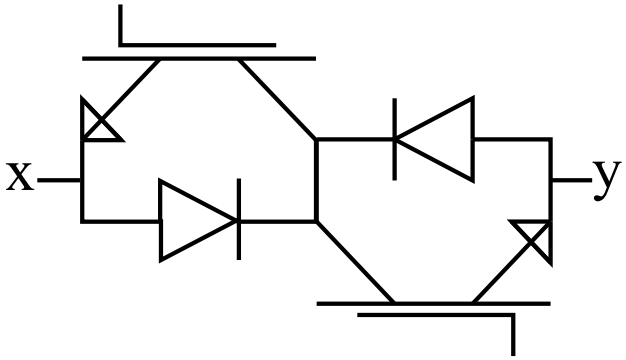



Figure 4.14: Common-collector bidirectional switch

Both the common collector and common emitter configurations can be used without the central common connection, but this connection provides some transient benefits during switching. In the common emitter configuration, the central connection also allows both devices to be controlled from one isolated gate drive power supply.

### 4.4.4 Anti-parallel reverse blocking IGBTs (RB-IGBTs)

If the switching devices used for the bidirectional switch have a reverse voltage blocking capability then it is possible to build the bidirectional switches by simply placing two devices in anti-parallel as shown in figure 4.15. This arrangement leads to a very compact converter with the potential for substantial improvements in efficiency [89]. The main feature of the RB-IGBT is its reverse voltage blocking capability, which eliminates the need for diodes. At any instant, there is only one device conducting the current in any direction so the conduction losses are lower than the other arrangements [89, 90]. Each RB-IGBT must behave as a free wheeling diode due to the lack of serially connected discrete diode. The latest technology makes the RB-IGBT work as a reverse-recovery diode when the RB-IGBT is turned off by a negative anode-

cathode bias [91]. However, to date the RB-IGBTs have shown poor reverse recovery characteristics which decreases the efficiency by increasing the switching losses and has prevented widespread use of this configuration.

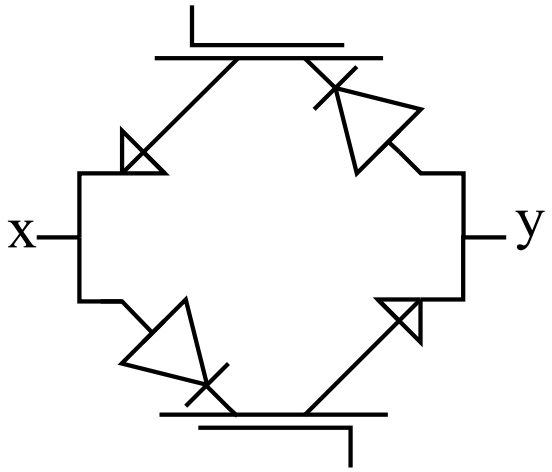
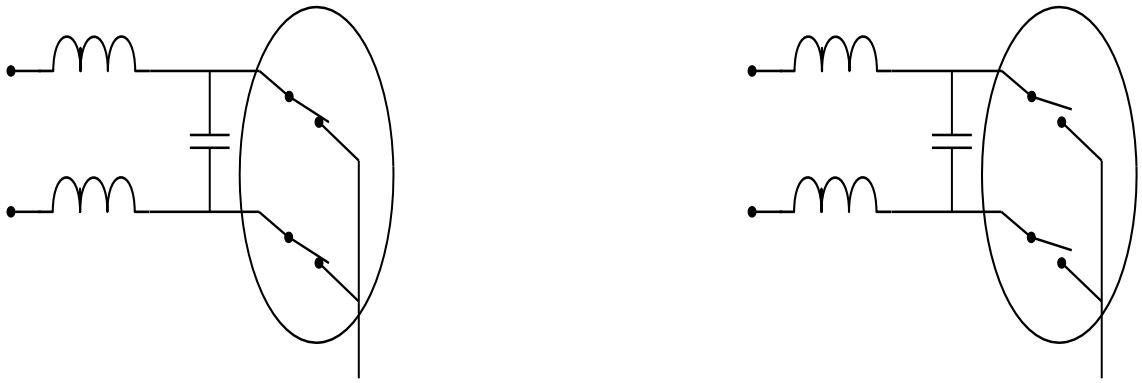



Figure 4.15: Reverse blocking IGBT bidirectional switch cell

## 4.5 Current commutation techniques

Reliable current commutation between switches in matrix converters is more difficult to achieve than in conventional VSIs since there are no natural free-wheeling paths. The commutation has to be actively controlled at all times with respect to two basic rules. These basic rules can be visualized by considering just two switch cells on one phase of a matrix converter. It is important that no two bidirectional switches are switched on at any instant, as shown in figure 4.16(a). This would result in line-to-line short circuits and the destruction of the converter due to over currents. Also, the bidirectional switches for each output phase should not all be turned off at any instant, as shown in figure 4.16(b). This would result in the absence of a path for the inductive load current, causing large over-voltages. These two considerations cause a conflict since semiconductor devices cannot be switched instantaneously due to propagation delays and finite switching times.



(a) Short circuit of capacitive input (b) Open circuit of inductive output

Figure 4.16: These conditions must be avoided for safe operation

## 4.5.1 Basic current commutation

### 4.5.1.1 Dead-time commutation

The dead-time method is commonly used in inverter circuits. The load current free-wheels through the anti-parallel diodes during the dead-time period. In the case of a matrix converter using dead-time commutation will cause an open circuit of the load. This will result in large voltage spikes across the switches which would destroy the converter unless snubbers or clamping devices are used to provide a path for the load current during the dead-time period [92, 93, 94]. This method is undesirable since the energy in the snubber circuit is lost during every commutation. In addition to this the bidirectional nature of the matrix converter circuit further complicates the snubber design. The clamping devices and the power loss associated with them also results in increased converter volume.

### 4.5.1.2 Overlap commutation

This method also breaks the rules of matrix converter current commutation and needs extra circuitry to avoid destruction of the converter. In overlap current commutation, the incoming switch is turned on before the outgoing one is turned off. This will cause

a line-to-line short circuit during the overlap period unless extra line inductance is added to slow the rise of the current [95]. This is not a desirable method since the inductors are in the main conduction path so the conduction losses would be increased. In addition to this there will be significant distortion of the output voltage waveform during the overlap period. The switching time for each commutation is increased and will vary with commutation voltage which may cause control problems.

One possible advantage of these simple commutation methods is that the diode bridge bidirectional switch arrangement may be used. However, this advantage is outweighed by the problems discussed above. For these reasons the advanced commutation methods described below are now preferred in all matrix converters.

### 4.5.2 Advanced commutation methods

A reliable method of current commutation, which obeys the rules, uses a four-step commutation strategy in which the direction of current flow through the commutation cells can be controlled. To implement this strategy, the bidirectional switch cell must be designed in such a way as to allow the direction of the current flow in each switch cell to be controlled.

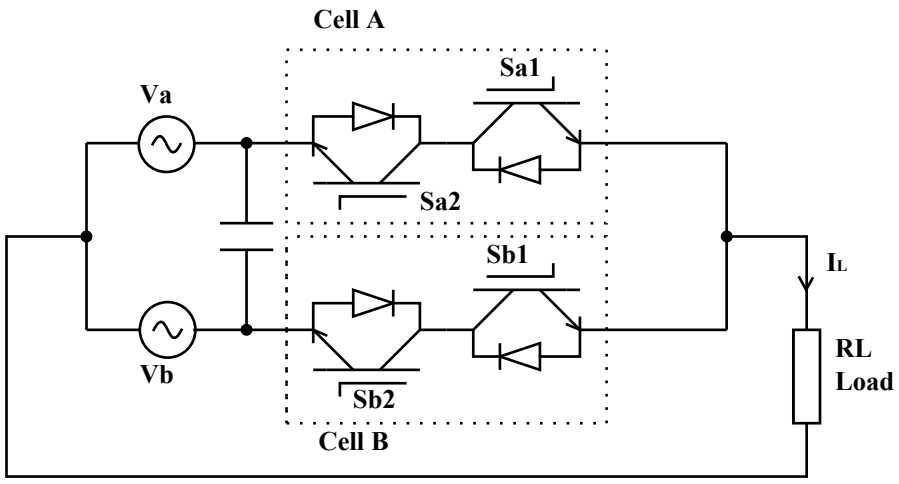
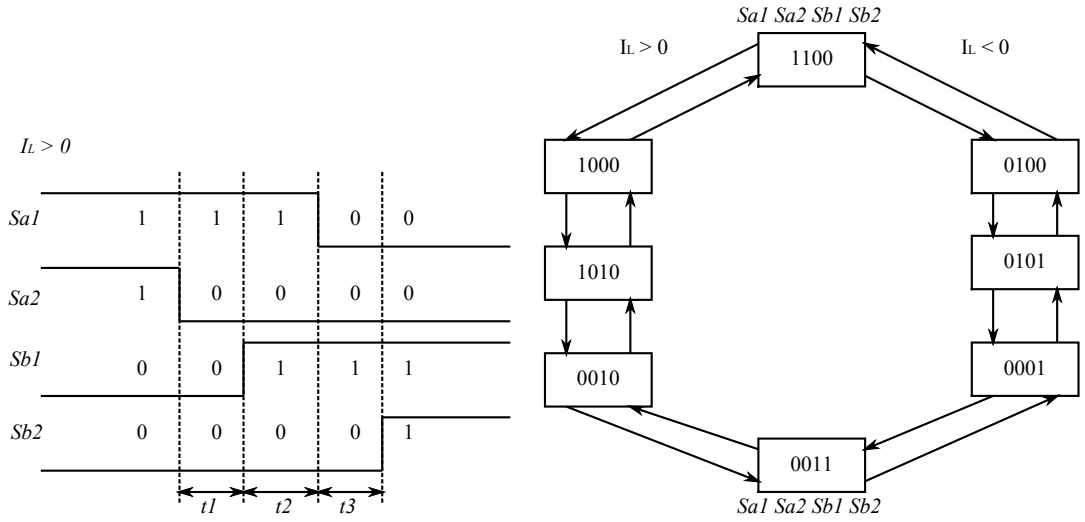



Figure 4.17: A two-phase to single-phase matrix converter

#### 4.5.2.1 Current-direction-based commutation

Figure 4.17 shows a schematic of a two-phase to single-phase matrix converter. In steady state, both of the devices in the active bidirectional switch cell are gated to allow both directions of current flow. The following explanation assumes that the load current is in the direction shown and that the upper bidirectional switch cell (cell A) is closed. When a commutation to cell B is required, the current direction is used to determine which device in the active switch cell is not conducting. This device is then turned off. In this case, device $S_{a2}$ is turned off. The device that will conduct the current in the incoming switch cell is then gated, $S_{b1}$ in this example. The load current transfers to the incoming device either at this point or when the outgoing device $S_{a1}$ is turned off. The remaining device in the incoming switch cell ($S_{b2}$) is turned on to allow current reversals. This process is shown as a timing diagram in figure 4.18(a); the delay added between each switching event is determined by the device characteristics. Figure 4.18(b) shows the state diagram for this strategy for the load current in both directions.




(a) Timing diagram for $I_L$ >0 (b) State diagram

Figure 4.18: Current-direction-based four-step commutation

This method allows the current to commutate from one switch cell to another without causing a line-to-line short circuit or a load open circuit. One advantage of this

technique is that the switching losses in the silicon devices are reduced by 50% because half of the commutaion process is soft switching and, hence, this method is often called "semi-soft current commutation" [92].

However, the above technique relies on knowledge of the output line current direction. This can be difficult to reliably determine in a switching power converter, especially at low current levels in high-power applications where traditional current sensors such as Hall-effect probes are prone to producing uncertain results. To avoid these current measurement problems, a technique for using the voltage across the bidirectional switch cell to determine the current direction has been developed. This method allows very accurate current direction detection with no external current sensors [96].

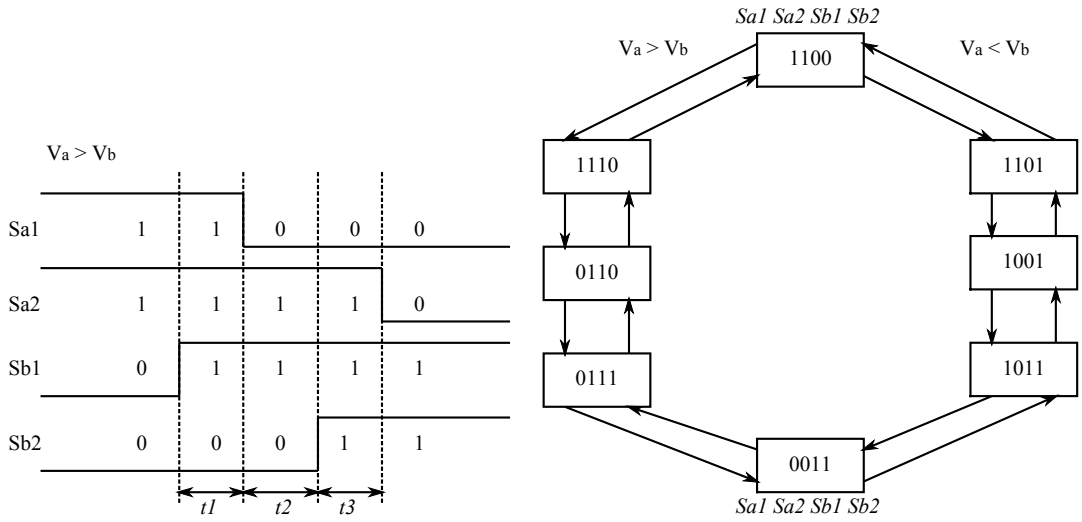
#### 4.5.2.2 Relative-voltage-magnitude-based commutation

The relative-voltage-magnitude-based commutation technique is a semi-soft commutation strategy that relies on the knowledge of the relative magnitudes of the input voltages to determine the switch sequence for each commutation. The concept of this strategy is to form a free-wheeling path in each bidirectional switch cell involved in commutation. The commutation process begins by identifying the 'free-wheeling' device in each bidirectional switch cell based on the relative magnitudes of the input voltages.

From figure 4.17, considering the case where $V_a > V_b$, the switches $S_{a2}$ and $S_{b1}$ are the 'free-wheeling' devices in bidirectional switch cells A and B, respectively. Based on the timing diagram shown in figure 4.19(a), the commutation sequence begins by gating on the free-wheeling device $S_{b1}$ in the incoming bidirectional switch cell, Cell B. With the free-wheeling paths available in both bidirectional switch cells, the non-free-wheeling device $S_{a1}$ in the outgoing cell, cell A, can be turned off. Then, the non-free-wheeling device, $S_{b2}$ is turned on. Finally, to complete the commutation sequence, the free-wheeling device $S_{a2}$ is gated off. Similar to the current-direction-based commutation strategy, a delay is introduced between each switching state change. The state

diagram of the relative-voltage-magnitude-based commutation strategy is shown in figure 4.19(b).

By applying this strategy the commutation between two bi-directional switches can be safely implemented. However, if the relative magnitudes of the input voltages are not measured correctly, a short circuit path can be mistakenly formed due to the wrong selection of free-wheeling devices. Therefore, reliable measurement of the input voltages is required in order to ensure that this commutation strategy is effective.




(a) Timing diagram for $I_L > 0$ (b) State diagram

Figure 4.19: Relative-voltage-magnitude-based four-step commutation

#### 4.5.2.3 Selection of a suitable current commutation technique for the two-stage matrix converter

In the current-direction-based commutation technique, the switching due to a wrong current sign could cause the load to be disconnected from the source. To protect against this situation a clamp circuit is usually used to provide a path for the inductive current. Therefore, conventional matrix converters typically use the current-direction-based four-step current commutation. The load current in a traditional matrix converter contains small amount of high frequency components due to inductive motor loads. This makes the detection of the load current direction relatively

simple.

For the two-stage matrix converter the four-step commutation is only necessary in the rectification stage of the converter. In this case, the direction of the dc-link current or the relative magnitude of the supply voltages can be used for the four-step current commutation. The dc-link current contains large amount of high frequency switching components which makes the accurate detection of the current direction difficult. For this reason it is more appropriate to use the relative-voltage-magnitude-based four-step current commutation strategy for the rectification stage of the two-stage matrix converter. Dead-time current commutation can be used for the inversion stage, where anti-parallel diodes in the IGBT switches provide a path for the inductive load currents.

## 4.6 Practical issues

### 4.6.1 Input filter

The input current waveforms of the two-stage matrix converter contain switching frequency components. These input current components can be reduced by adding an input filter to the power converter. A simple low pass $LC$ filter offers a cost and volume effective [92, 97] solution for attenuating these unwanted switching frequency components. The requirements for the filter are as follows [97]:

(1) to have a cut-off frequency lower than the switching frequency of the converter;

(2) to minimize its reactive power at the grid frequency;

(3) to minimize the volume and weight for capacitors and inductors;

(4) to minimize the filter inductance voltage drop at rated current in order to avoid a reduction in the voltage transfer ratio.

The input filter configuration for the two-stage matrix converter is shown in figure 4.20, where the filter capacitors ($C_f$) are connected in a star arrangement and inductors ($L_f$) are connected in series with the supply lines. This forms a second order filter, with a cut-off frequency designed to be much lower than the switching frequency in order to provide considerable attenuation at the switching frequency.

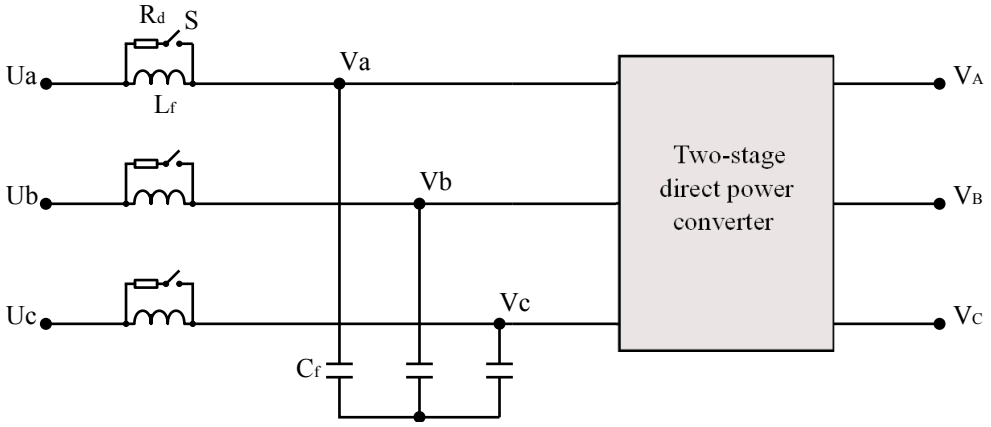



Figure 4.20: The input filter configuration

The cut-off frequency, $\omega_c$, of the filter is configured by the choice of capacitor and inductor based on (4.43).

$$\omega_c = \frac{1}{\sqrt{L_f C_f}} \tag{4.43}$$

By choosing the capacitance $C_f$, the filter inductance $L_f$ can be determined using (4.43). However, the filter inductance must ensure minimum voltage drop at the rated current, which is lower than the value determined using (4.44) [13].

$$L_f \leq \frac{\sqrt{\left(\frac{\Delta V}{V_n}\right) - 2 \cdot \left(\frac{\Delta V}{V_n}\right)^2}}{\omega_i} \cdot \frac{V_n}{I_n} \tag{4.44}$$

where $\Delta V$ is the maximum voltage drop across the filter inductor; $V_n$ and $I_n$ are the rated supply phase voltage and current, respectively. In most situations, a compromise between $L_f$ and $C_f$ has to be made. A low filter capacitance offers a high input displacement factor, but requires a large inductance to achieve the required cut-off frequency. However, the maximum permissible voltage drop limits the size of the inductor.

Even-though the $LC$ filter smooths out the input current, it can cause undesirable disruption of the matrix converter during power-up. This transient response can appear when a voltage step is applied to the $LC$ filter circuit, which can cause destructive over-voltage to the converter. Hence, a method of connecting a damping resistor, $R_d$, and a switch, $S$, in parallel with the inductor $L_f$ has been proposed [97] for alleviating this problem. The selected damping resistor, $R_d$, has to be smaller than the reactive impedance at the cut-off frequency:

$$R_d \leq \omega_c L_f \tag{4.45}$$

Referring to figure 4.20, $S$ is initially turned on during the power-up. Due to the smaller resistance of $R_d$, the current mostly flows through the damping resistors instead of the inductors, which improves the waveforms during the power-up procedure. Once the filter capacitor is fully charged to the supply voltages, $S$ is turned off.

The presence of the input filter can also yield unstable operation depending on the converter topology and control strategy adopted [98, 99]. The input filter must therefore be designed in conjunction with the control system of the matrix converter. The introduction of the damping resistor $R_d$ in the input filter design improves significantly the system stability.

### 4.6.2 Over-voltage protection

In a two-stage matrix converter over-voltages can appear when the converter is disabled either from the supply side or from the load side. At the supply side, the over-voltage can occur due to line perturbations or transients due to the input filter during the power-up procedure. Over-voltage at the load side can occur due to the unexpected shut down of the converter, for example in an over-current situation. When all the bi-directional switch cells are turned off there are no free-wheeling paths for the current to discharge the stored energy within the load inductance, causing an over-voltage. Therefore, an additional protection circuit is required to protect the converter circuit from any damage. A clamp circuit is the most appropriate solution

to avoid over-voltage on both the supply and load sides of the converter. The next section describes the clamp circuit for the two-stage matrix converter.

### 4.6.3 The clamp circuit

A clamp circuit can be used to protect the converter from over voltages [100]. The clamp circuit consists of eight fast recovery diodes with a clamp capacitor ($C_c$) and resistor ($R_c$) connected in parallel, as shown in figure 4.21.

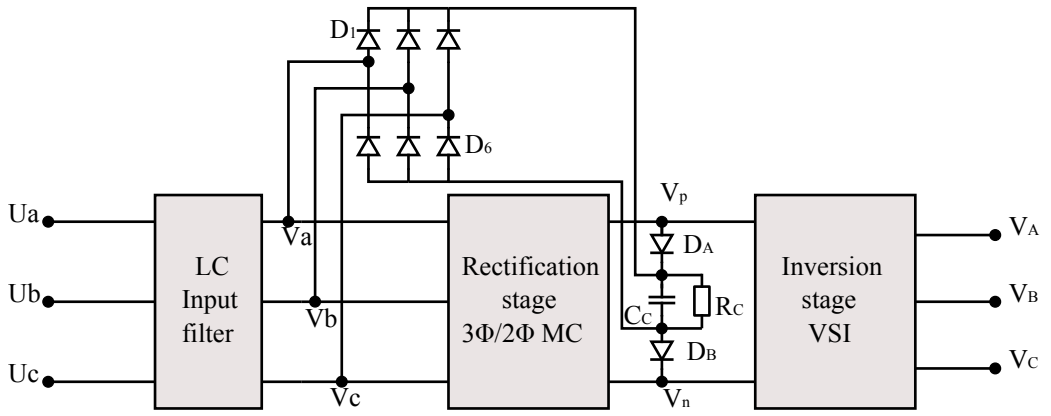



Figure 4.21: A clamp circuit configuration for the two-stage matrix converter

During an over voltage situation on the supply side the fast recovery diodes provide the path for the current, which charge up the capacitor. The energy stored in the clamp capacitor is then dissipated by the resistor $R_c$. Two anti-parallel diodes are connected to the inversion stage. During an over-voltage situation on the load side, diodes $D_A$ and $D_B$ provide a free-wheeling path for the inductive load current, charging up the clamp capacitor.

A comprehensive analysis for the design of the clamp circuit for matrix converters in induction motor applications was described in [101]. The value of the clamp capacitor ($C_c$) can be estimated using the following equation:

$$C_c = \frac{\frac{3}{2} \cdot {I_{lim}}^2 (L_{\delta,S} + L_{\delta,R})}{{V_{max}}^2 - {V_{LL}}^2} \tag{4.46}$$

where, $I_{lim}$ is the maximum current limit of the converter, $(L_{\delta,S} + L_{\delta,R})$ is the total motor leakage inductance; $V_{max}$ is the maximum acceptable voltage level of the clamp capacitor which is less than the voltage rating of the semiconductor devices. $V_{LL}$ is the steady state voltage across the clamp capacitor, which is approximately the peak amplitude of the supply line-to-line voltage.

## 4.7 Advantages of the two-stage matrix converter over the conventional matrix converter

The two-stage matrix converter offers the same inherent benefits of the conventional matrix converter such as sinusoidal input currents, unity input displacement factor and bidirectional power flow. The two-stage matrix converter offers simplified PWM control in comparison to the conventional matrix converter because the two-stage matrix converter can be divided into a CSR at the input and a VSI at the output and the individual converters modulated separately [87, 102]. In some applications, the two-stage matrix converter may be preferred to the conventional matrix converter due to the advantages discussed in this section. The following sub-sections explain some of the advantages of the two-stage matrix converter in comparison to the conventional matrix converter.

### 4.7.1 Safer commutation

Referring to figure 4.9, while a current commutation is implemented at the rectification stage, a zero voltage vector is produced by the inversion stage. By using the zero voltage vector, the dc-link current is zero. Hence, the switches of the rectification stage are commutated at zero current, which gives a safer commutation environment and lower switching losses for the rectification stage [14].

### 4.7.2 Reduced number of switches

The two-stage matrix converter provides the possibility to reduce the number of semiconductor components [88], therefore, these converters are also called "sparse matrix converters". The sparse matrix converter topologies benefit from reduced cost and complexity due to the reduced number of switches. In addition, all these topologies can provide unity input displacement factor, sinusoidal input and output currents similar to the conventional matrix converters. The process of reducing the switches is performed in the rectification stage. Figure 4.22 shows four possibilities of the rectifier side.

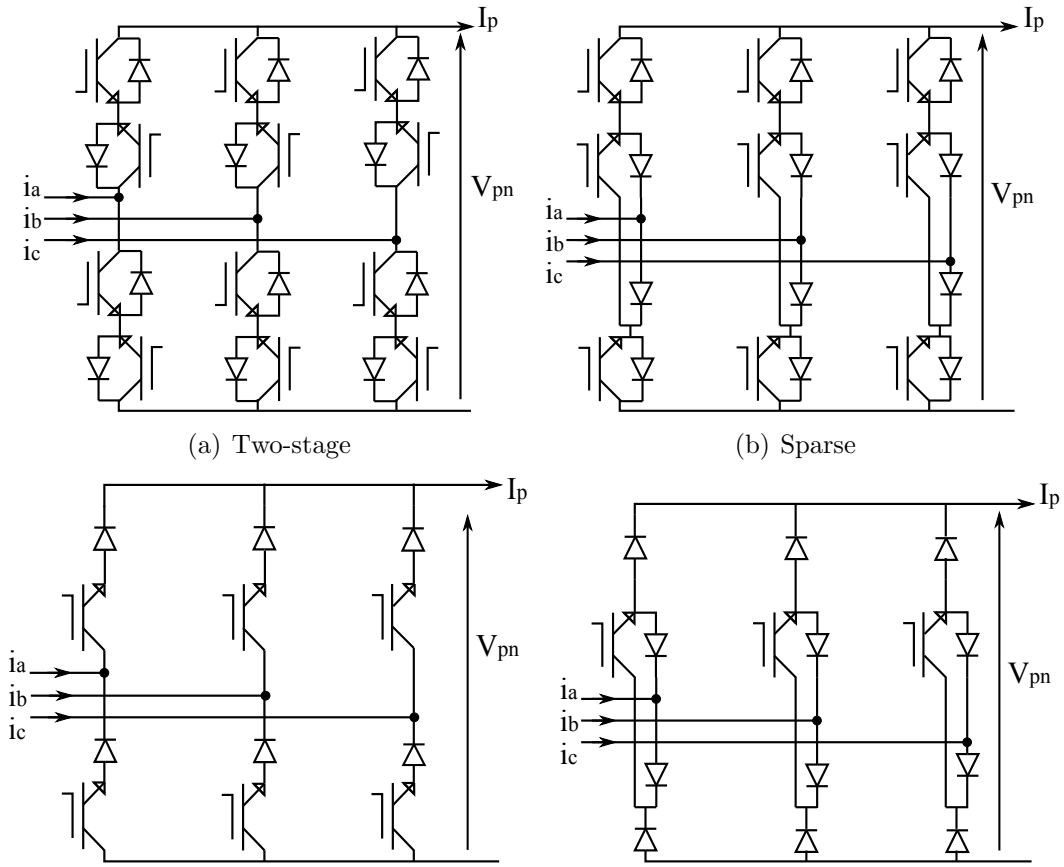



Figure 4.22: Two-stage matrix converter rectifier possibilities.

The two-stage matrix converter (TMC) rectifier (figure 4.22(a)) is composed by six four-quadrant bidirectional switch cells and needs twelve IGBT gate drives. The

TMC rectifier side has always two diodes and two IGBTs in conduction, whatever the control of the converter. The sparse matrix converter (SMC) rectifier (figure 4.22(b)) has the same characteristics as that of the TMC but the number of required IGBT gate drives is reduced to nine. The very sparse matrix converter (VSMC) rectifier (figure 4.22(c)) has the number of required IGBT gate drives reduced to six. The ultra sparse matrix converter (USMC) rectifier (figure 4.22(d)) is the simplest controllable structure among the four solutions since only three gate drives are needed. The VSMC and USMC rectifiers cannot create bidirectional power flow as opposed to the other two solutions. Due to the same reason, the load power factor which can be achieved using the VSMC and USMC is limited to a minimum of 0.86 [103]. In the case of the SMC and USMC, two additional devices (one IGBT and one diode for the SMC, and two diodes for the USMC) are involved in conducting the dc-link current. Therefore, the SMC and USMC suffer from high conduction losses in comparison to the VSMC and the TMC [88].

### 4.7.3 Cost effective multi-drive system

In traditional multi-drive systems, a single rectification stage can be coupled to several inversion stages using a common dc-link energy storage [104]. This method provides cost effective solution due to the sharing of the front end rectifier stage but several limitations are noted. Among them is the safety of the system. Having large energy storage with electrolytic capacitors, the system can be vulnerable to massive destruction, dc-link short-circuits, etc. As a solution a cost effective multi-drive system using the two-stage matrix converter was proposed [14], which eliminates the use of energy storage in the dc-link. This technique uses several VSIs connected in parallel and fed from a CSR with no dc-link capacitor in order to independently control several three phase loads. The dc-link is supplied using a single rectification stage. This multi-drive topology is shown in figure 4.23.

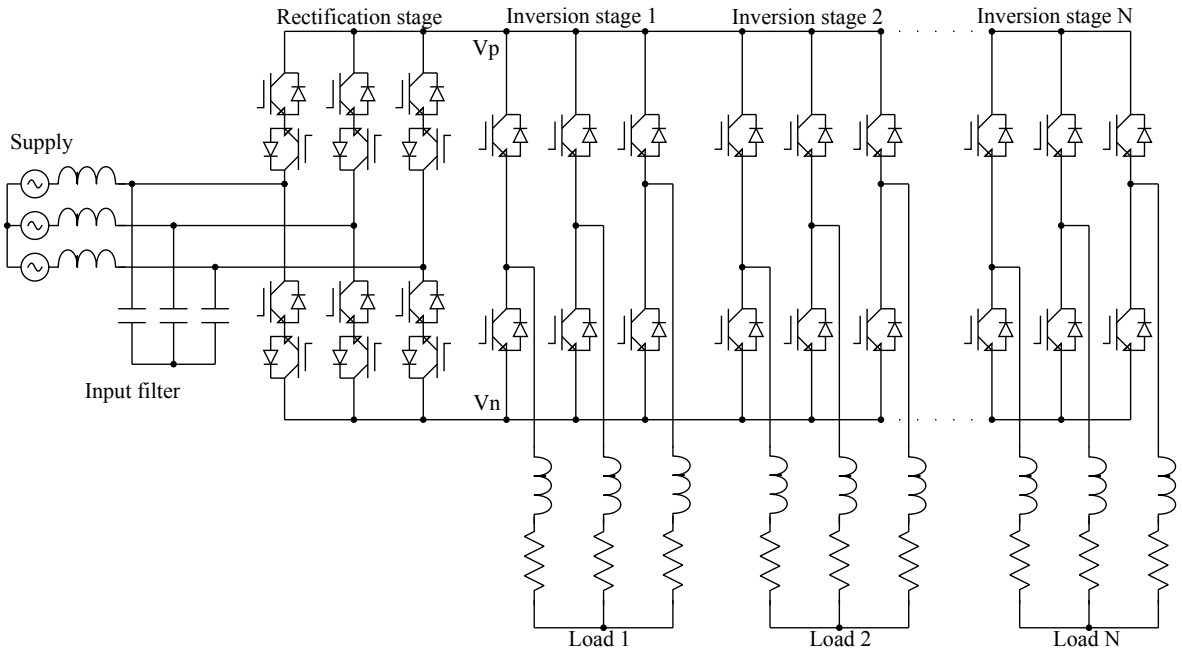



Figure 4.23: The multi-drive solution based on a two-stage matrix converter

## 4.8 Comparison of conventional and two-stage matrix converters

In the previous sections, the conventional and two-stage matrix converters were assumed to be ideal. However, there are several different sources for non-ideal performance and they affect these converters in practice. These effects become more important when the two converters are compared because they are identical under ideal circumstances.

This section presents a brief comparison of the non-ideal characteristics of the conventional and two-stage matrix converters. The characteristics compared are the supply current quality, voltage transfer ratio and the semiconductor power losses.

### 4.8.1 Supply current quality

Under ideal conditions, the conventional and two-stage matrix converters produce identical supply currents with identical load currents. However, in reality the two-stage matrix converter has lower supply current quality when compared to the conventional matrix converter under the same operating conditions. The reasons for the disparity are the different main circuits, which leads also to partly different safe commutation methods. The supply current distortion of the conventional matrix converter depends on the output current distortion while the real dc-link of the two-stage matrix converter increases supply current distortion compared to the conventional matrix converter [105].

### 4.8.2 Voltage transfer ratio

The two-stage matrix converter has lower voltage transfer ratio in most operation conditions because real semiconductor components have different effects due to the different main circuit structure and safe commutation methods [106].

### 4.8.3 Semiconductor power losses

The two-stage matrix converter has higher power losses than the conventional matrix converter in most loading conditions. The conventional matrix converter losses depend mainly on the load current magnitude whiles the two-stage matrix converter losses depend on the active load power. The power losses of the conventional matrix converter are smaller except the case of high load current and low output/input voltage ratio. The reasons for the disparity are the different main circuits, which leads also to partly different safe commutation methods. When the output active power is low and output load current is near rated value, the two-stage matrix converter has lower losses. However, the situation changes depending on the semiconductors used in each case [106, 107].

The comparison of the conventional and two-stage matrix converter semiconductor power losses can also be realized for classical industrial applications with constant rms load current (similar to a constant motor torque). A typical comparison of the two converters shows that the conventional matrix converter efficiency is better for high motor frequency, whereas the two-stage matrix converter is better at low frequency. If the ASD mainly runs at low speed, then it may be judicious to favour the two-stage matrix converter. Otherwise, the conventional matrix converter is more appropriate [108].

The conventional matrix converter losses are relatively constant since the rms input voltage is constant with the same switching frequency. All the conventional matrix converter switches are similar and conduct the same rms load currents. For the two-stage matrix converter, at low frequency, the inverter has long duration of free-wheeling, so a very little part of the load current passes through the rectifier. In contrast, at high frequencies, the inverter has reduced free-wheeling states. Thus, the two-stage matrix converter losses are proportional to the load frequency for a constant flux control [108].

For the global speed range, the conventional matrix converter has got a power losses peak value about 20% smaller than the two-stage matrix converter. This peak value defines the sizing of the cooling system which can thereby be significantly reduced with the conventional matrix converter solution compared to the two-stage matrix converter. The two-stage matrix converter creates unbalanced losses between the rectifier and the inverter switches which increases the volume of the cooling system. Indeed, the rectifier presents only conduction losses whereas the inverter presents all the switching losses in addition to conduction losses [108].

However, the advantages of the two-stage matrix converter mentioned earlier namely simplified PWM control, safer commutation, reduced number of switches and cost effective multi-drive system makes the two-stage matrix converter the preferred choice in many applications.

## 4.9 Conclusions

In this chapter, the two-stage matrix converter topology from the converter derivation, modulation strategy and hardware implementation has been reviewed. Derived from the indirect transfer function approach proposed for the conventional matrix converter, the two-stage matrix converter is able to generate high quality input and output waveforms identical to the conventional matrix converter by applying SVM. The operation of the two-stage matrix converter topology has been shown through simulation results.

In the hardware implementation, similar to the conventional matrix converter, bidirectional switch cells and associated commutation techniques are required for the two-stage matrix converter to effectively perform a four-quadrant operation. A procedure for designing a suitable and effective input filter for the two-stage matrix converter is also presented so that a set of sinusoidal input currents can be obtained at the supply side. For protecting the two-stage matrix converter, a clamp circuit and damping resistors are essential to protect the converter from any damage due to over-voltages that can occur either at the supply or load side.

Finally, the advantages of the two-stage matrix converter over the conventional matrix converter are reviewed and a comparison of the two topologies in terms of supply current quality, voltage transfer ratio and semiconductor power losses has been reviewed.

# Chapter 5

# Three-Level Two-Stage Direct AC-AC Power Converter

## 5.1 Introduction

The three-level, two-stage matrix converter [109] is used as the basic topology from which the three-level, Z-source hybrid direct ac-ac power converter (Chapter 6) is derived. This chapter describes the operating principles and SVM technique for controlling the three-level, two-stage matrix converter. Simulation results are presented to show the effectiveness of this topology to generate the desired input and output waveforms.

## 5.2 Circuit configuration

The three-level, two-stage matrix converter can be divided into a rectification stage and an inversion stage, as shown in figure 5.1. Like the traditional two-stage matrix converter, a *3 x 2* matrix converter is used as the rectifier to generate a switching dc-

link voltage, $V_{pn}$, for the inversion stage. The rectified dc-link voltage is split into dual voltage supplies, $V_{po}$ and $V_{no}$, by connecting the dc-link mid-point '$o$' to the neutral-point of the star-connected input filter capacitors. These dual voltage supplies are then used to feed the back-end NPC VSI to generate the required three-level phase-to-neutral voltages. Taking the dc-link mid-point '$o$' as a reference, there are three voltage levels at the dc-link: $V_{po}$, $0V$ and $V_{no}$. Based on these dc-link voltages, the inversion stage can be modulated to generate multilevel output voltage waveforms.

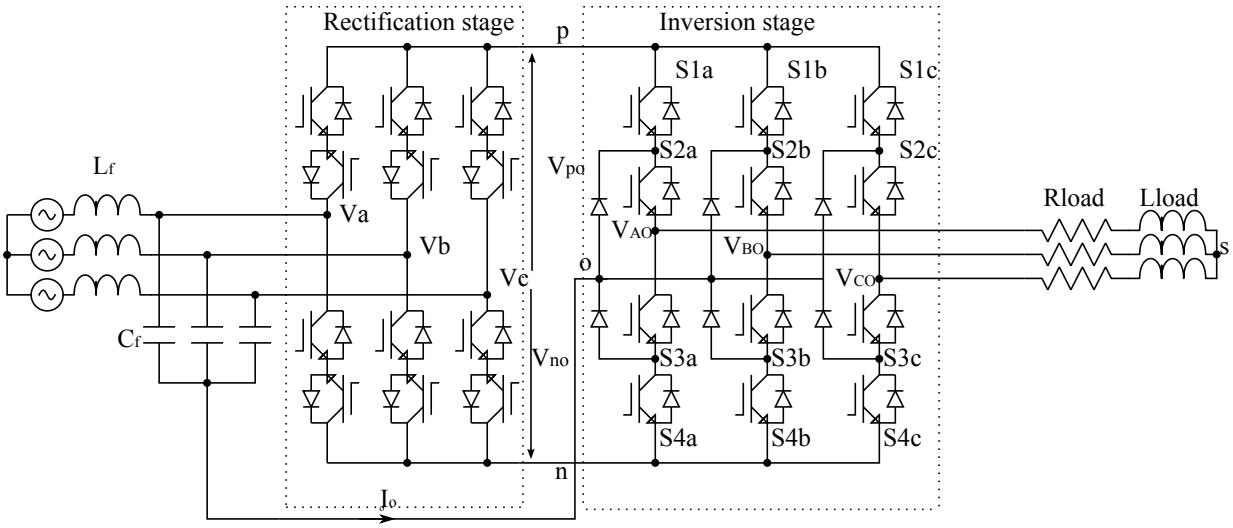



Figure 5.1: Three-level two-stage matrix converter

At any instant, only two bidirectional switches in the rectification stage can be turned on to connect an input line-to-line voltage to the dc-link points '$p$' and '$n$'. Thus, the rectification stage can be represented with two conducting switches that connect the positive voltage level to the dc-link terminal '$p$' and negative voltage level to the terminal '$n$', as illustrated in figure 5.2. It is easily noted that the equivalent circuit shown in figure 5.2 is similar to the conventional NPC VSI. For instance, if the rectification stage connects the input line-to-line voltage $V_{ab}$ to the dc-link, the voltage $V_{po}$ is equal to the input line-to-neutral point voltage $V_{ao}$ while $V_{no}$ equals $V_{bo}$. Upon modulating the switching devices in each phase-leg of the inversion stage according to the switching combinations shown in table 5.1, each output terminal voltage,$V_{ko}$ ($k\epsilon$\{A,B,C\}), of the inversion stage has three possible voltage levels: $V_{po}$, $0V$ and $V_{no}$, which proves that it is able to generate multilevel output voltages.

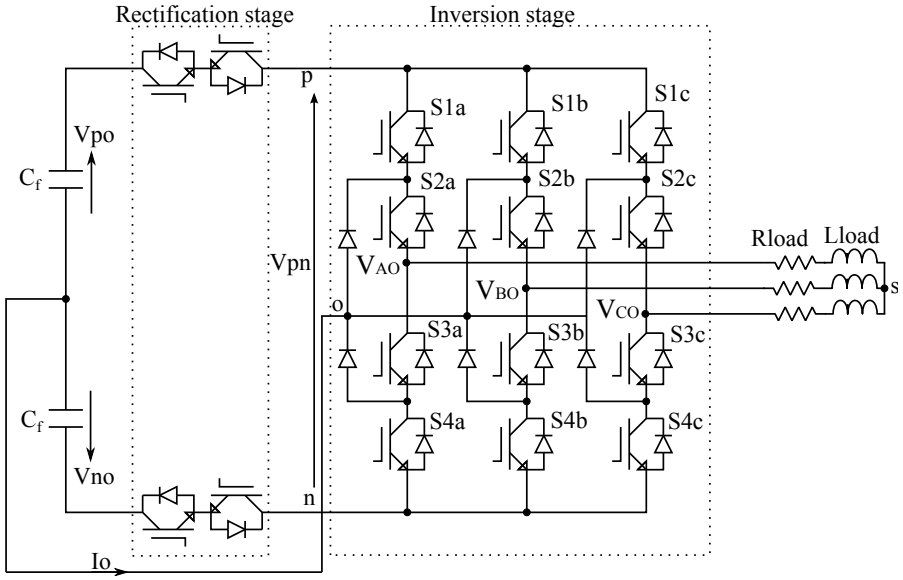



Figure 5.2: The equivalent state of the three-level two-stage matrix converter with the rectification stage represented by two conducting switches

This converter offers all the benefits of the conventional two-stage matrix converter namely adjustable input displacement factor, high quality input current waveforms, capability of regeneration and the absence of bulky and limited lifetime energy storage components. However, one of the drawbacks of the converter is its complicated circuit configuration. Its circuit consists of twenty-four switches and thirty diodes. It is possible, however, to reduce the number of switches in the rectification stage as elaborated in Chapter 4. As a result of the high number of switches, a complex modulation strategy is required to control this converter. Also, the neutral-point balancing problem of the conventional NPC VSI is inherited. This problem could cause distortion of the output voltage waveform if the neutral-point current, $i_o$, flowing through the input filter capacitors is not controlled properly.

| $S_{1x}$ | $S_{2x}$ | $S_{3x}$ | $S_{4x}$ | $V_{ko}$ | Switching state |
|---|---|---|---|---|---|
| ON | ON | OFF | OFF | $V_{po}$ | P |
| OFF | ON | ON | OFF | 0 | O |
| OFF | OFF | ON | ON | $V_{no}$ | N |

Table 5.1: The switching combination for the switches in each phase leg of the inversion stage ($x\epsilon$\{a,b,c\})

In order to modulate the converter to produce a set of balanced, sinusoidal input and output waveforms, different modulation strategies have been proposed [12, 110, 111]. In [12], an SVM technique based on the concept of virtual vectors, was derived and applied to this converter. In the following section, the SVM technique for controlling this converter is presented based on the operating principles and SVM techniques for the NPC VSI and *3 x 2* matrix converter presented in Chapters 2 and 4, respectively.

## 5.3 Space vector modulation

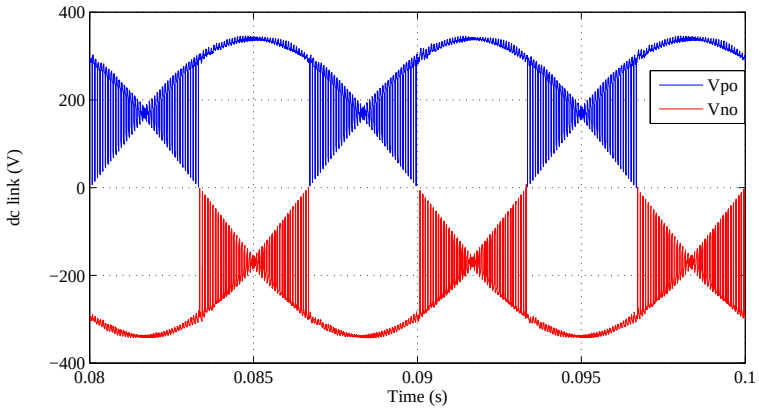
The SVM strategy for controlling the three-level, two-stage matrix converter was proposed in [12]. A review of this modulation strategy is presented below.

From the strategy proposed in [12], the rectification and inversion stages of this converter are modulated using SVM. In each stage, a combination of vectors is produced to synthesise a reference vector of a given magnitude and phase. After the determination of the vectors and their associated duty cycles, the modulation pattern of the converter then combines the switching states for both stages so that the correct balance of input currents and output voltages can be obtained for each sampling period. The rectification stage is modulated in the same way as that described for the traditional two-stage matrix converter (Chapter 4) and will not be repeated here. The only difference between the SVM techniques for this converter and that of the traditional two-stage matrix converter is associated with the inversion stages.

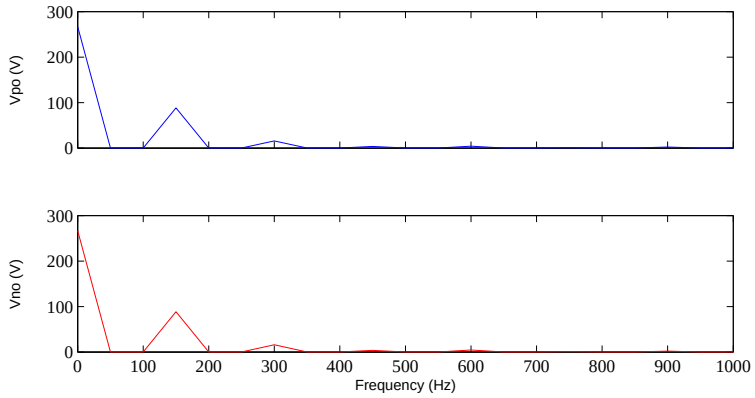
### 5.3.1 The inversion stage

The NPC VSI is used for the inversion stage of this converter, as shown in figure 5.1. The connection between the dc-link mid-point '$o$' and the neutral-point of the star-connected input filter capacitors is essential to provide the required dual voltage supplies and a zero voltage mid-point. In order to operate the converter to generate

proper multilevel output voltages, the modulation of the inversion stage must ensure that the average neutral-point current over a switching period is zero [12]. From table 5.1, each output terminal of the inversion stage can be connected to the dc-link point '$o$' for the zero voltage level ($V_{ko} = 0V$).




(a) $V_{po}$ and $V_{no}$




(b) The spectra of the dc-link voltages

Figure 5.3: The dc-link voltages, $V_{po}$ and $V_{no}$, provided by the rectification stage with supply frequency, $f_i = 50Hz$

Whenever the output terminal is connected to point '$o$', the neutral-point current, $i_o$, would cause unequal charging or discharging of the input filter capacitors, depending on the loading condition. Without proper control, the unequal voltage levels of the input filter capacitors would affect the dc-link voltages provided by the rectification stage, which would directly impact on the ability of the inversion stage to generate proper multilevel outputs, causing output voltage distortion. This situation is similar

to the neutral-point balancing problem of the conventional NPC VSI.

The modulation of the inversion stage must be able to apply the variable dc-link voltages, $V_{po}$ and $V_{no}$, to generate the desired output voltages. As shown in figure 5.3(a), $V_{po}$ and $V_{no}$ provided by the rectification stage are obviously not constant. From figure 5.3(b), their average values over a modulating (fundamental) period are however equal. The spectra of these dc-link voltages consist of a dc component and a 3rd order harmonic of the supply frequency that is inherently included in the rectification stage's output when it is modulated using SVM. The inversion stage is modulated based on the averages of the dc-link voltages, $V_{po,avg}$ and $V_{no,avg}$.

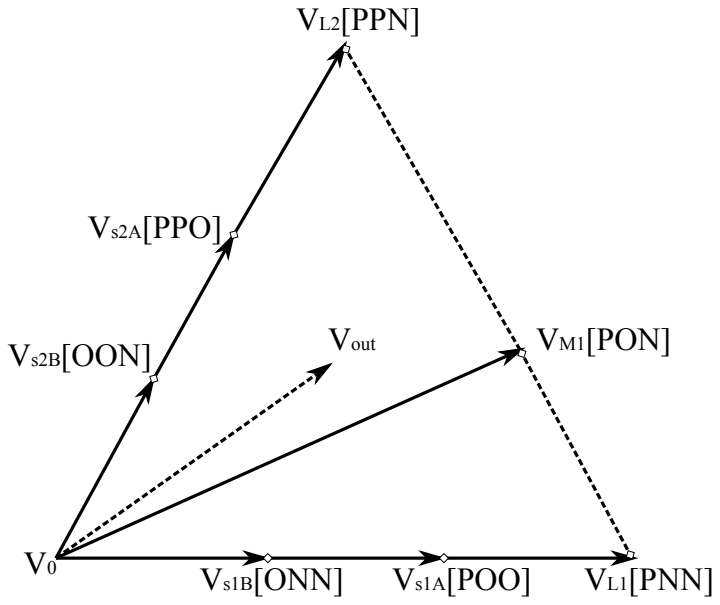



Figure 5.4: The voltage vectors generated by unequal dc-link voltages when $V_{po,avg} > V_{on,avg}$

Since SVM is applied to the inversion stage, the effects of unequal average dc-link voltages on the voltage space vectors must be examined. For this reason, the output voltages generated by the switching states of the inversion stage have to be determined. Similar to the NPC VSI, the inversion stage of this converter has twenty-seven possible switching states that represent the connection of the output terminals to their respective dc-link points ($p$, $n$ or $o$), as shown in table 2.2. In order to facilitate explanation, only the switching states listed in table 5.2 are analysed. The output

phase voltages generated by each switching state are determined using (5.1), which is derived based on (2.2) but expressed in terms of $V_{po,avg}$ and $V_{on,avg}$ (= -$V_{no,avg}$), $m_{x1}$ and $m_{x3}$ represent the switch combinations ($S_{1x}$ & $S_{2x}$) and ($S_{3x}$ & $S_{4x}$) in each phase leg ($x$ $\epsilon$\{a, b, c\}), which is '1' when both switches in the combination are on and '0' otherwise.

| | | | Output phase voltages | | | Output voltage space vectors | | |
|---|---|---|---|---|---|---|---|---|
| A | B | C | $V_{As}$ | $V_{Bs}$ | $V_{Cs}$ | Vector | Magnitude | Angle |
| P | P | P | 0 | 0 | 0 | | | |
| O | O | O | 0 | 0 | 0 | $V_0$ | 0V | 0 |
| N | N | N | 0 | 0 | 0 | | | |
| P | O | O | $\frac{2}{3}x$ | $-\frac{1}{3}x$ | $-\frac{1}{3}x$ | $V_{s1A}$ | $\frac{2}{3}x$ | 0 |
| O | N | N | $\frac{2}{3}y$ | $-\frac{1}{3}y$ | $-\frac{1}{3}y$ | $V_{s1B}$ | $\frac{2}{3}y$ | 0 |
| P | N | N | $\frac{2}{3}(x+y)$ | $-\frac{1}{3}(x+y)$ | $-\frac{1}{3}(x+y)$ | $V_{L1}$ | $\frac{2}{3}(x+y)$ | 0 |
| P | O | N | $\frac{1}{3}(2x+y)$ | 0 | $-\frac{1}{3}(x+2y)$ | $V_{M1}$ | $\frac{2}{3}\sqrt{(x^2+xy+y^2)}$ | $\tan^{-1}(\frac{\sqrt{3}x}{2x+y})$ |
| P | P | O | $\frac{1}{3}x$ | $\frac{1}{3}x$ | $-\frac{2}{3}x$ | $V_{s2A}$ | $\frac{2}{3}x$ | $\pi/3$ |
| O | O | N | $\frac{1}{3}y$ | $\frac{1}{3}y$ | $-\frac{2}{3}y$ | $V_{s2B}$ | $\frac{2}{3}y$ | $\pi/3$ |
| P | P | N | $\frac{1}{3}(x+y)$ | $\frac{1}{3}(x+y)$ | $-\frac{2}{3}(x+y)$ | $V_{L2}$ | $\frac{2}{3}(x+y)$ | $\pi/3$ |

Table 5.2: The output phase voltages and voltage space vectors generated by the switching states of the inversion stage.

Referring to table 5.2, where $x = V_{po,avg}$ and $y = V_{on,avg}$, it is obvious that the output phase voltages generated by each switching state depend on the connected dc-link voltage(s). For instance, switching state $POO$ applies only the dc-link voltage $V_{po,avg}$ to the output. Hence, the output phase voltage generated by $POO$ is clearly different from that generated by $ONN$, which uses only $V_{on,avg}$. However, when the neutral-point current '$i_o$' is controlled to be zero over a switching period we have the situation whereby $V_{po,avg} = V_{on,avg}$ and the output phase voltages generated by $POO$ and $ONN$ would be identical.

$$\begin{aligned} V_{As} &= \frac{1}{3}\{V_{po,avg}(2m_{a1} - m_{b1} - m_{c1}) - V_{on,avg}(2m_{a3} - m_{b3} - m_{c3})\} \\ V_{Bs} &= \frac{1}{3}\{V_{po,avg}(2m_{b1} - m_{a1} - m_{c1}) - V_{on,avg}(2m_{b3} - m_{a3} - m_{c3})\} \\ V_{Cs} &= \frac{1}{3}\{V_{po,avg}(2m_{c1} - m_{a1} - m_{b1}) - V_{on,avg}(2m_{c3} - m_{a3} - m_{b3})\} \end{aligned} \tag{5.1}$$

Using the space vector transformation given in (5.2), these switching states can be converted into voltage space vectors as shown in table 5.2. As an example, the voltage

space vectors for the case where $V_{po,avg} > V_{on,avg}$ are shown in figure 5.4. Compared to figure 2.3, the small voltage vectors ($V_{S1}$ and $V_{S2}$) and medium voltage vector ($V_{M1}$) are obviously affected by the unequal average dc-link voltages while the large voltage vectors ($V_{L1}$ and $V_{L2}$) remain unchanged because $V_{po,avg}$ plus $V_{on,avg}$ equals $V_{pn,avg}$. At any instant, except when $V_{po,avg} = V_{on,avg}$, each redundant switching state of the small voltage vectors (e.g.$V_{S1}$) generates a different magnitude of voltage vector ($V_{S1A}$ and $V_{S1B}$) due to the use of different dc-link voltages. On the other hand, the medium voltage vector ($V_{M1}$) does not only have a varying amplitude but also a varying phase depending on $V_{po,avg}$ and $V_{on,avg}$. As shown in figure 5.4, these voltage space vectors with varying amplitude and phase (only for $V_{M1}$) complicate the process of synthesizing the reference output voltage vector, $\vec{V}_{out}$, for the inversion stage.

$$\vec{V}_{out}(t) = \frac{2}{3}\left[V_{As}(t)e^{j0} + V_{Bs}(t)e^{j2\pi/3} + V_{Cs}(t)e^{j4\pi/3}\right] \tag{5.2}$$

To effectively modulate the inversion stage using SVM to generate the desired outputs, the NTVV technique is a very good option. The ability of the NTVV technique to control the neutral-point balancing problem of the conventional NPC VSI has been shown in Chapter 2. Therefore, by applying the NTVV technique to the inversion stage, the average neutral-point current over a switching period can be controlled to be zero, thus preventing the voltage levels of the input filter capacitors deviating from the desired levels. The concept of defining virtual vectors, by linearly combining the voltage space vectors, in NTVV is able to overcome the modulation complication caused by deviation of the dc-link voltages from their desired levels as a result of the flow of neutral-point current. By linearly combining different voltage space vectors to form a set of virtual vectors with constant magnitude and fixed direction, as shown in figure 5.5, the process of synthesizing the reference output voltage vector, $\vec{V}_{out}$, can be greatly simplified.

As shown in figure 5.5, the virtual medium vector ($V_{V_{MV1}}$) and virtual small vectors ($V_{V_{SV1}}$ and $V_{V_{SV2}}$) are formed by linear combinations of different voltage vectors. The effects of the deviation of the dc-link voltages on the small and medium voltage vectors are taken care of by introducing the constants $k_1$ to $k_7$ to control the active time of these voltage vectors within the combination. At any sampling instant, $k_1$ to

$k_7$ are varied according to the small and medium voltage vectors in order to maintain the magnitudes and angles of $V_{V_{MV1}}$, $V_{V_{SV1}}$ and $V_{V_{SV2}}$, shown in figure 5.5, that are obtained by using equal average dc-link voltages ($V_{po,avg} = V_{on,avg} = V_{pn,avg}/2$).

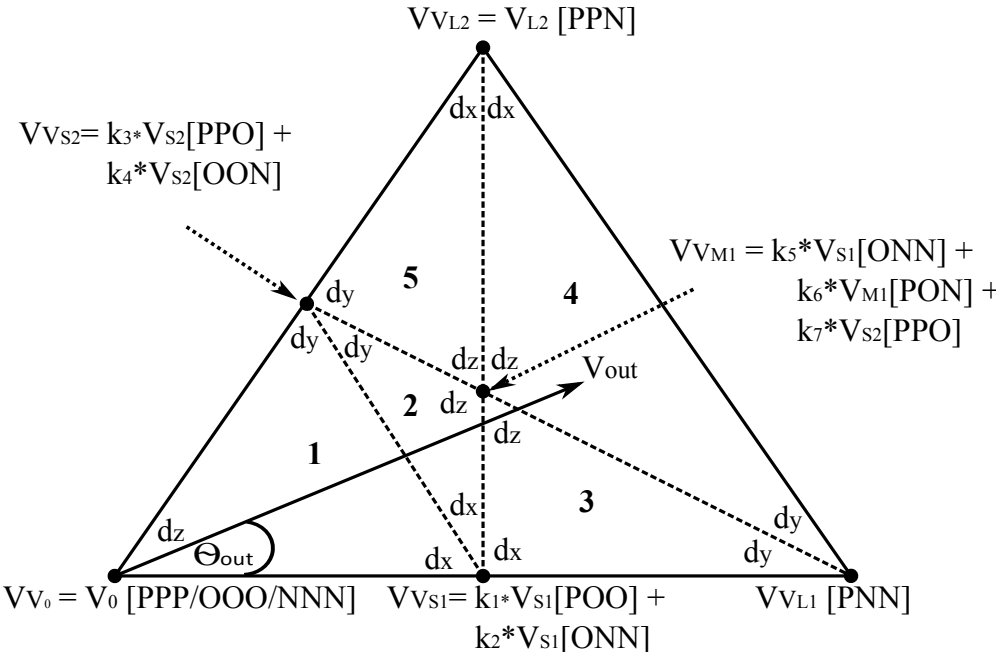



Figure 5.5: Sector I of the SVD for the inversion stage modulated using NTVV

By defining the constants $k_1 = k_2 = k_3 = k_4 = 1/2$ and $k_5 = k_6 = k_7 = 1/3$, $V_{V_{SVi}}$ and $V_{V_{MVi}}$ for the inversion stage are formed such that the average neutral-point current, $i_o$, equals zero in each switching period. The synthesis of the reference output voltage vector, $\vec{V}_{out}$, is performed using the nearest three virtual vectors. This defines five small triangular regions as shown in figure 5.5. Table 5.3 presents the duty cycle equations for the selected virtual vectors in each triangle ($\Delta$), where $m_I$ is the modulation index of the inversion stage given by (5.3) and $\theta_{out}$ is the angle of the reference vector, $\vec{V}_{out}$, within the sector. To complete the modulation process of the inversion stage, the voltage vectors that form the selected virtual vectors are applied to the output according to the switching sequences shown in table A.1.

$$m_I = \frac{\sqrt{3} \cdot |\vec{V}_{out}|}{V_{pn,avg}} \tag{5.3}$$

| $\Delta$ | $d_x$ | $d_y$ | $d_z$ |
|---|---|---|---|
| 1 | $m_I[\sqrt{3}\cos\theta_{out} - \sin\theta_{out}]$ | $2m_I \sin\theta_{out}$ | $1 - m_I[\sqrt{3}\cos\theta_{out} + \sin\theta_{out}]$ |
| 2 | $2 - m_I[\sqrt{3}\cos\theta_{out} + 3\sin\theta_{out}]$ | $2 - 2\sqrt{3}m_I \cos\theta_{out}$ | $3m_I[\sqrt{3}\cos\theta_{out} + \sin\theta_{out}] - 3$ |
| 3 | $2 - m_I[\sqrt{3}\cos\theta_{out} + 3\sin\theta_{out}]$ | $\sqrt{3}m_I \cos\theta_{out} - 1$ | $3m_I\sqrt{3}\sin\theta_{out}$ |
| 4 | $0.5m_I[\sqrt{3}\cos\theta_{out}+3\sin\theta_{out}]-1$ | $2 - 2\sqrt{3}m_I \cos\theta_{out}$ | $1.5m_I[\sqrt{3}\cos\theta_{out} - \sin\theta_{out}]$ |
| 5 | $0.5m_I[\sqrt{3}\cos\theta_{out}+3\sin\theta_{out}]-1$ | $\sqrt{3}m_I \cos\theta_{out} - 1$ | $3-1.5m_I[\sqrt{3}\cos\theta_{out}+\sin\theta_{out}]$ |

Table 5.3: Duty cycle equations for the selected virtual vectors in each triangle

### 5.3.2 Synchronization between the input and output stages

The switching states of the rectification and inversion stages are synchronised within each switching interval. This ensures a balance of input currents and output voltages within a switching interval. As an example, let us consider the case where the vector $\vec{I}_{in}$ is located in sector 2 while $\vec{V}_{out}$ is located in triangle 4 of sector I. For the rectification stage, the selected current vectors are: $\vec{I}_1$ (= $\vec{I}_\gamma$) and $\vec{I}_2$ (= $\vec{I}_\delta$); the virtual vectors selected for the inversion stage are: $\vec{V}_{V_{M1}}$, $\vec{V}_{V_{L1}}$ and $\vec{V}_{V_{L2}}$. Based on the NTVV technique, these virtual vectors are formed by using the voltage vectors: $\vec{V}_{S1}$[ONN], $\vec{V}_{L1}$[PNN], $\vec{V}_{S2}$[PPO], $\vec{V}_{M1}$[PON] and $\vec{V}_{L2}$[PPN]. The voltage vectors are applied to the output according to the switching sequence PPO $\rightarrow$ PPN $\rightarrow$ PON $\rightarrow$ PNN $\rightarrow$ ONN.

The selected voltage vectors for the inversion stage are arranged in a double-sided switching sequence but with unequal halves, with each half corresponding to the active times of the selected current vectors. This ensures a minimum number of switching transitions. Based on this example, the modulation pattern for the converter is shown in figure 5.6. The time interval for each voltage vector of the inversion stage's switching sequence can be determined using (5.4).

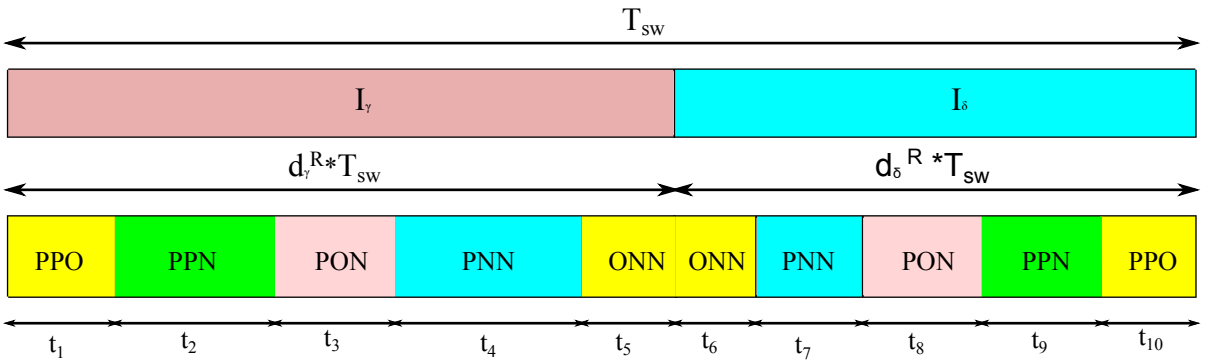



Figure 5.6: The switching pattern for the three-level two-stage matrix converter for the case where the input reference vector, $\vec{I}_{in}$, is located in sector 2 while the output reference vector, $\vec{V}_{out}$, is located in triangle 4 of sector I.

$$
\begin{aligned}
t_1 &= \frac{1}{3} \cdot d_z \cdot d_\gamma^R \cdot T_{sw} \\
t_2 &= d_x \cdot d_\gamma^R \cdot T_{sw} \\
t_3 &= \frac{1}{3} \cdot d_z \cdot d_\gamma^R \cdot T_{sw} \\
t_4 &= d_y \cdot d_\gamma^R \cdot T_{sw} \\
t_5 &= \frac{1}{3} \cdot d_z \cdot d_\gamma^R \cdot T_{sw} \\
t_6 &= \frac{1}{3} \cdot d_z \cdot d_\delta^R \cdot T_{sw} \\
t_7 &= d_y \cdot d_\delta^R \cdot T_{sw} \\
t_8 &= \frac{1}{3} \cdot d_z \cdot d_\delta^R \cdot T_{sw} \\
t_9 &= d_x \cdot d_\delta^R \cdot T_{sw} \\
t_{10} &= \frac{1}{3} \cdot d_z \cdot d_\delta^R \cdot T_{sw}
\end{aligned}
\tag{5.4}
$$

## 5.4 Simulation results

The NTVV modulation technique designed for this converter has been verified using the SABER® simulation platform with the simulation parameters chosen as presented in Appendix B. The effectiveness of the modulation strategy in maintaining the

voltage levels of the input filter capacitors is evaluated first.

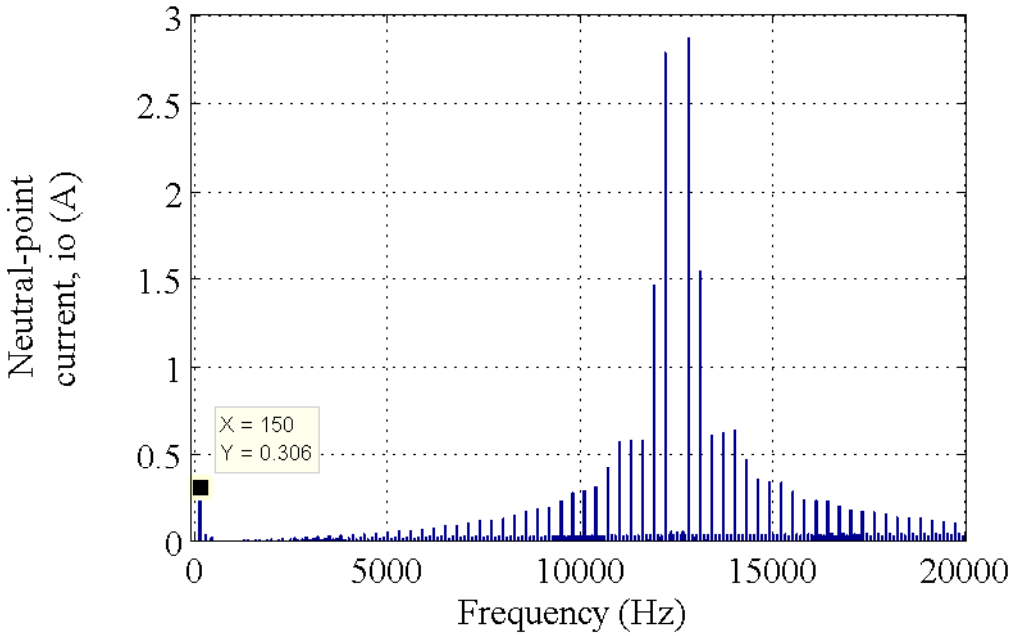



Figure 5.7: The spectra of the neutral-point current, $i_o$

As already noted, the connection from the dc-link middle point '$o$' to the neutral-point of the input filter capacitors is essential but the neutral-point current, $i_o$, can cause deviation from the desired voltage levels of the input filter capacitors. The average neutral-point current over a switching period must be zero in order to maintain the correct voltage levels of the input filter capacitors. The spectra of $i_o$ is shown in figure 5.7 where it is noted that the magnitude of the fundamental component is zero, the only significant harmonic present being the 3rd harmonic of the supply frequency (150 Hz). This ensures that the voltage levels of the input filter capacitors remain balanced, as shown in figure 5.8. These results clearly show the ability of the modulation technique to control the neutral-point current to be zero over each switching period and maintain the voltage levels of the input filter capacitors.

The input current waveforms, shown in figure 5.9, are clearly sinusoidal and balanced which demonstrates the ability of the NTVV modulation technique to control the converter to generate a set of sinusoidal, balanced input currents.

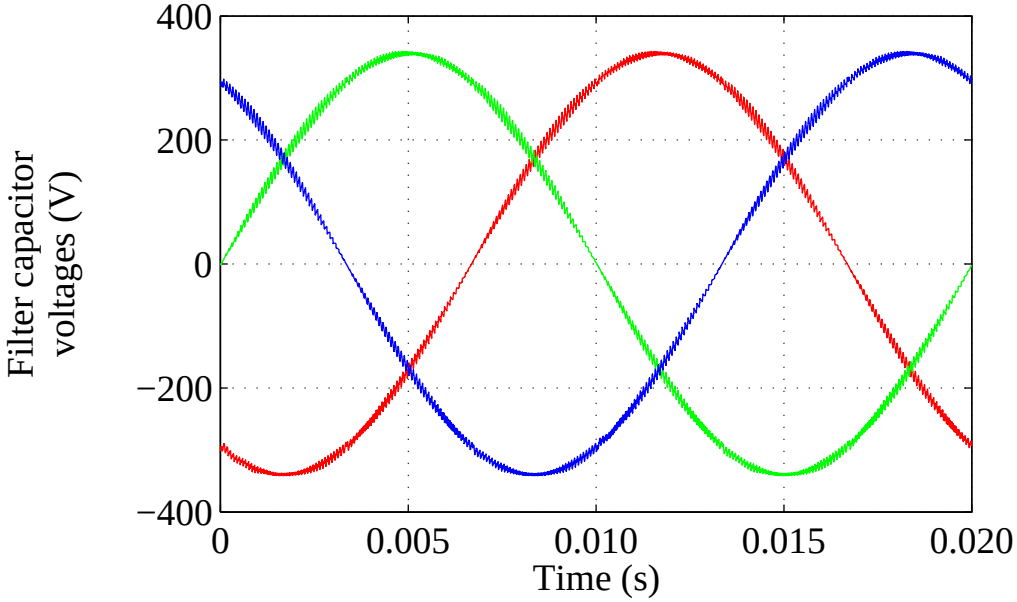



Figure 5.8: The voltage levels of the input filter capacitors

Figure 5.10 shows the dc-link voltages provided by the rectification stage. By splitting the variable dc-link voltage $V_{pn}$ (figure 5.10(a)) into dual voltage supplies, the inversion stage is supplied with $V_{po}$ and $V_{no}$, which are also variable, as shown in figure 5.10(b). In order to demonstrate the ability of the converter to generate multilevel outputs, figure 5.11 shows the output waveforms generated by this topology with $m_I$ = 0.9. At high modulation indices, the converter obviously generates three distinct voltage levels for $V_{Ao}$, as shown in figure 5.11(a). From figure 5.11(b), the line-to-line voltage consists of five levels which evidently proves the ability of this converter to generate multilevel output voltages. To examine whether the voltage levels are properly applied to generate the desired outputs, the output currents of the converter are shown in figure 5.11(c). These currents are clearly sinusoidal and balanced.

At low modulation indices, the output waveforms produced by this converter are similar to those produced by the conventional two-stage matrix converter as shown in figure 5.12.

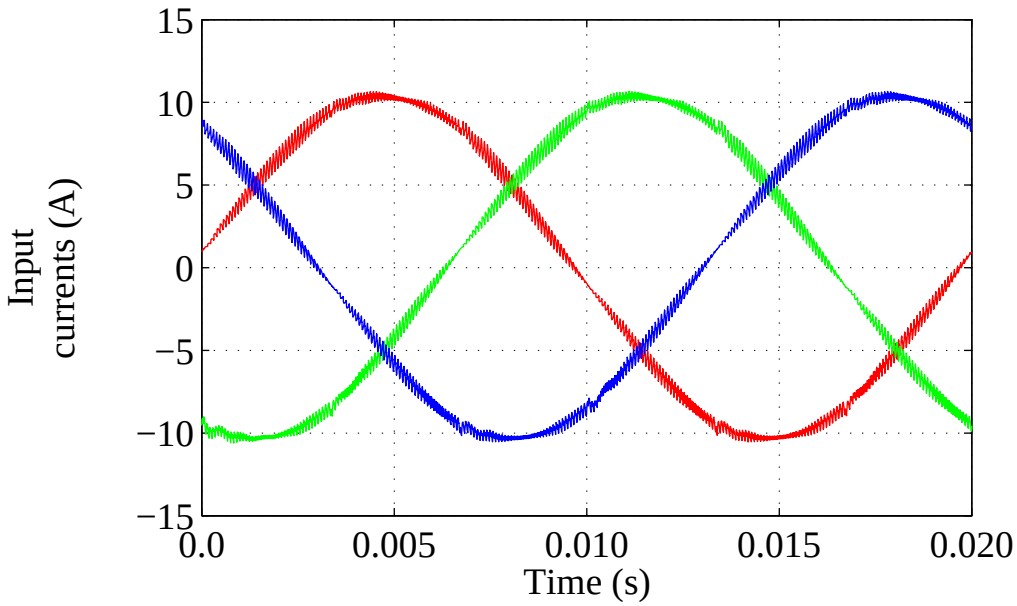
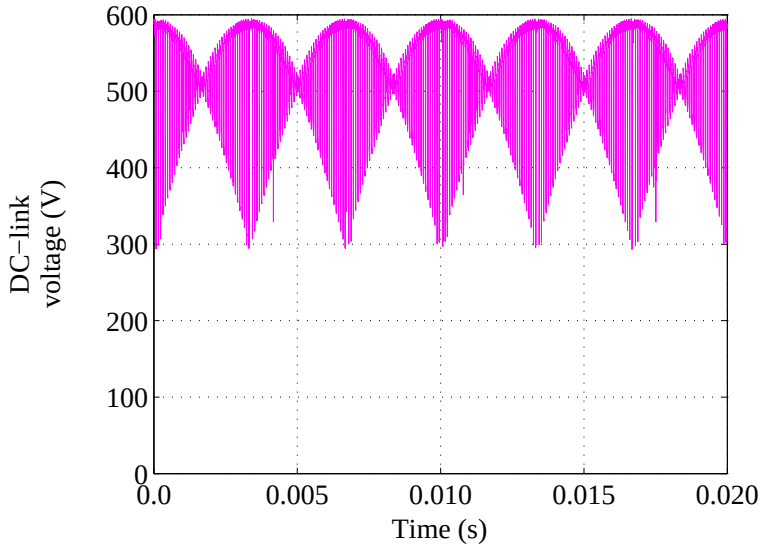
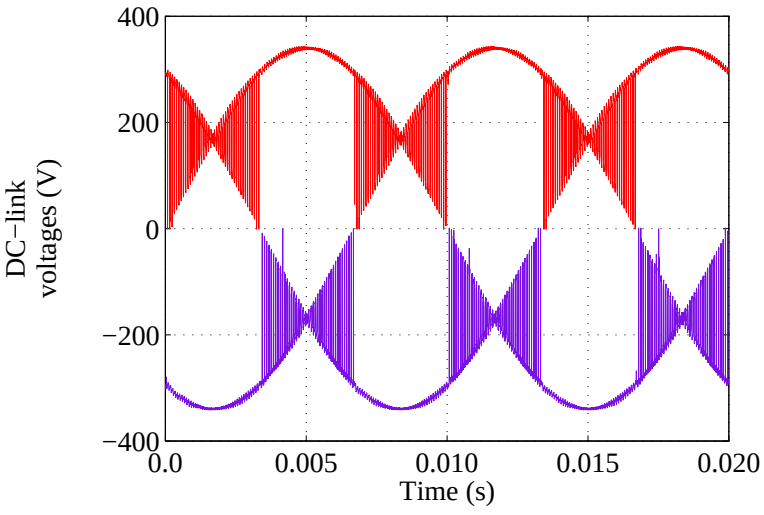



Figure 5.9: The filtered three-phase input currents

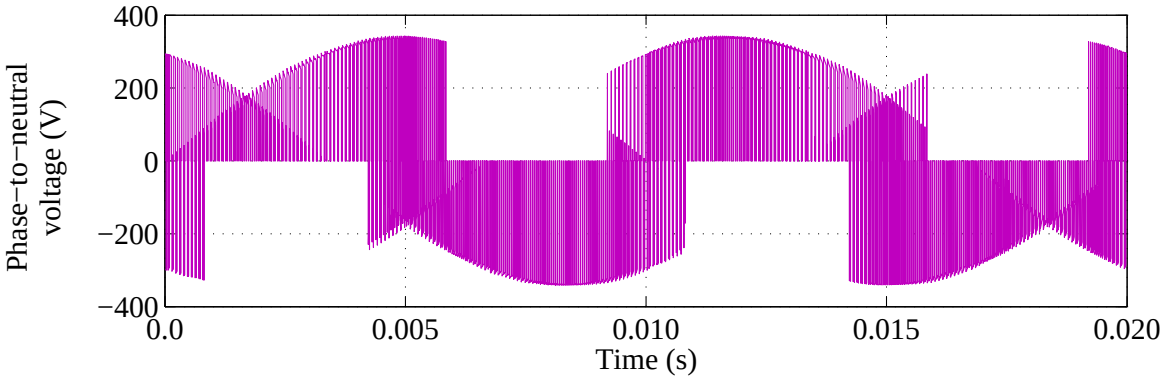



(a)

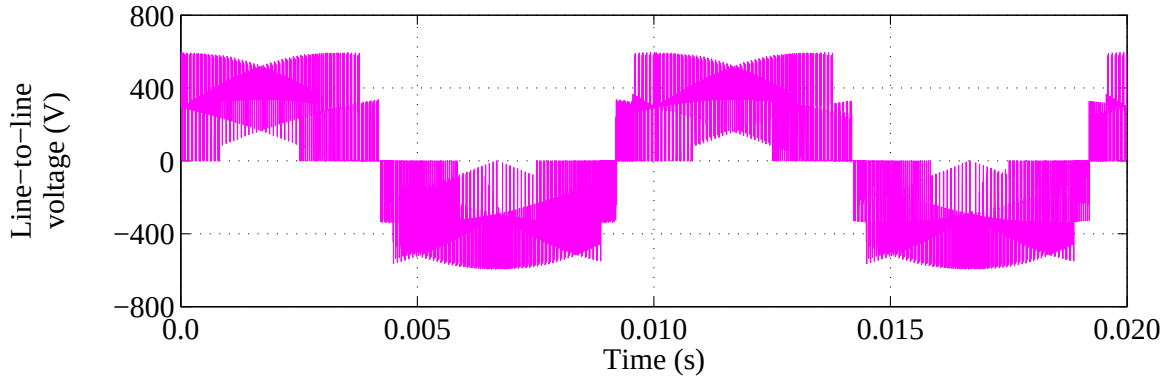



(b)

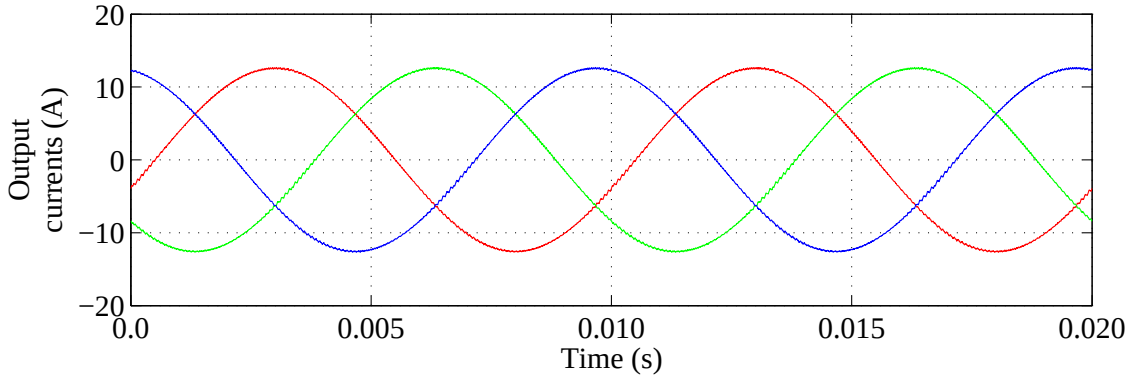
Figure 5.10: The dc-link voltages provided by the rectification stage (a) $V_{pn}$ (b) $V_{po}$ and $V_{no}$




(a)

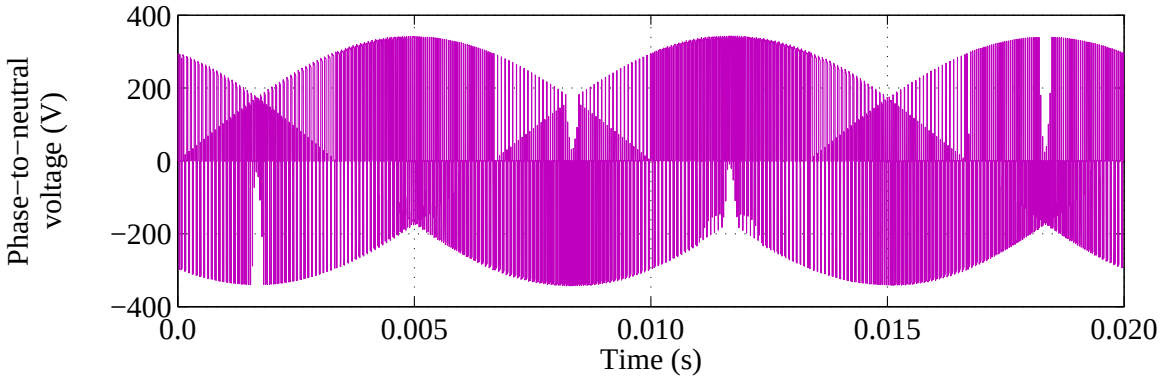



(b)

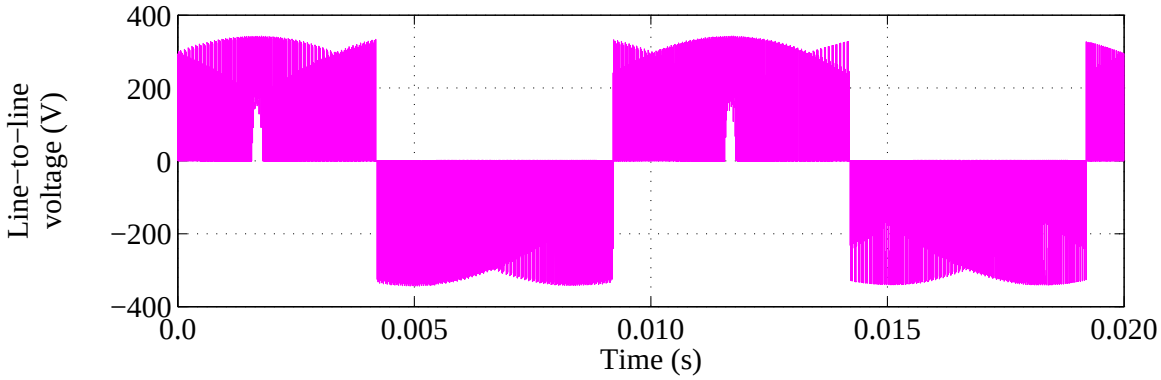



(c)

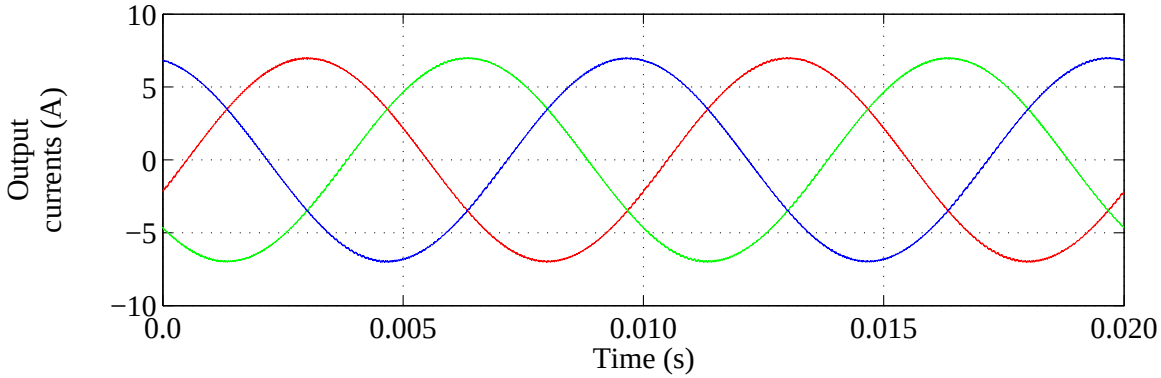
Figure 5.11: The output waveforms generated by the three-level two-stage matrix converter when the modulation index of the inversion stage, $m_I = 0.9$




(a)




(b)




(c)

Figure 5.12: The output waveforms generated by the three-level two-stage matrix converter when the modulation index of the inversion stage, $m_I = 0.5$

## 5.5 Conclusions

In this chapter, the principle of operation and SVM technique for controlling the three-level, two-stage matrix converter have been presented. The issues related to the neutral-point current and the resulting deviation of the input filter capacitors' voltages from the desired levels have been discussed. The concept of virtual vectors has been used to ensure that the average neutral-point current over a switching period is zero. This ensures that the correct average dc-link voltages are applied to the inversion stage of the converter to generate the required output waveforms. Simulation results have been used throughout to verify the operation of the converter.

# Chapter 6

# Three-Level Z-Source Hybrid Direct AC-AC Power Converter

## 6.1 Introduction

The ability of the three-level, two-stage matrix converter to generate multilevel output voltages has been shown in Chapter 5. This converter inherits the main disadvantage of the conventional two-stage matrix converter: its output voltage is limited to 86.6% of its input voltage. Therefore, it is not possible to run a standard machine at its full rating. Different techniques to maintain the output voltage quality and maximum voltage transfer ratio have been investigated in the literature [19, 21, 22]. However, most of these techniques can provide a maximum of 86.6% voltage transfer. Therefore, investigation into an alternative topology that overcomes the maximum voltage transfer ratio limitation of the three-level, two-stage matrix converter while maintaining all its benefits is very much welcome.

This chapter presents a three-level, Z-source hybrid direct ac-ac power converter, which could overcome the above mentioned deficiency in the three-level, two-stage matrix converter. This converter is an extension of the three-level, two-stage matrix

converter with a Z-source network in its virtual dc-link to add a boost function. Due to the boost capability, the converter can be used to drive standard voltage motors. It maintains a higher effective dc-link voltage by using shoot-through states of the inversion stage in conjunction with the Z-source network to boost the output voltage of the rectification stage to a higher value so that the inversion stage can synthesize higher output voltages.

In this chapter, an SVM technique for controlling the three-level, Z-source hybrid direct ac-ac power converter is described. The operating principles of the converter are discussed first. Then a detailed explanation of the modulation technique is given. Finally, simulation results are presented to show the effectiveness of the proposed SVM-based algorithm in allowing the converter to operate in the voltage buck-boost mode.

## 6.2 Circuit configuration

As shown in figure 6.1, the three-level, Z-source hybrid direct power converter consists of a rectification stage, a Z-source network and an NPC VSI in cascade. Similar to the two-stage matrix converter, the rectification stage is a *3 x 2* matrix converter that is used to build up a switching dc-link voltage, $V_{pn}$, for the inversion stage and to maintain sinusoidal input currents. The output voltage of the rectification stage is thus responsible for feeding the back-end Z-source NPC inverter. The split supply of the Z-source NPC inverter is effectively formed by two of the input filter capacitors without requiring additional storage capacitors.

At any instant, only two bidirectional switches in the rectification stage are turned on to connect the input line-to-line voltage to the dc-link. The positive voltage level is applied to the dc-link '$p$' terminal and negative voltage level to the '$n$' terminal, as shown in table 6.1. Therefore, the rectification stage can be represented with two conducting switches, $S_{xp}$ and $S_{xn}$ ($x\epsilon$\{a, b, c\}), that connect the positive voltage level to the dc-link terminal '$p$' and the negative voltage level to the dc-link terminal '$n$'

as shown in figure 6.2.

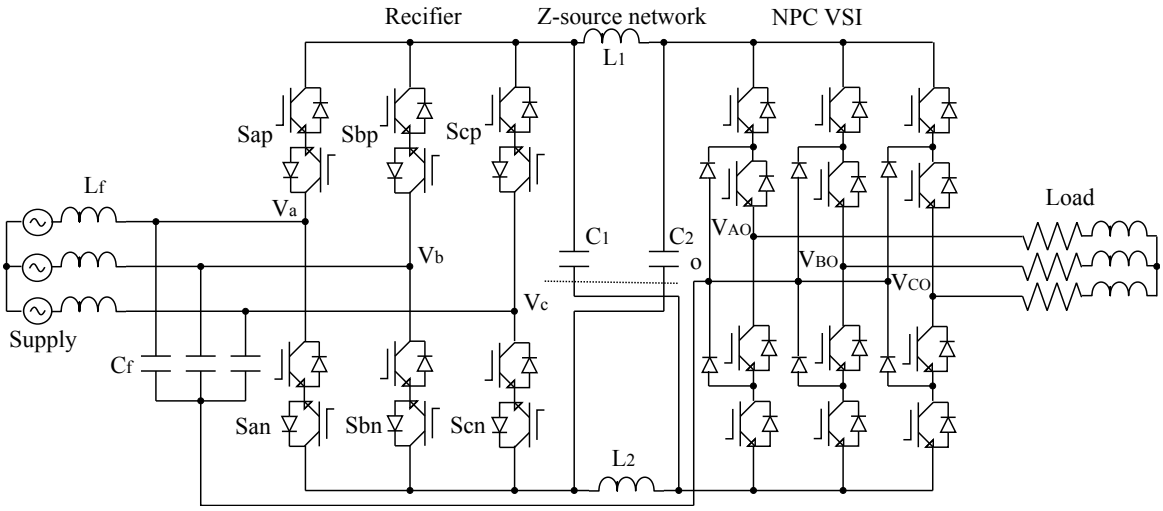



Figure 6.1: The three-level Z-source hybrid direct power converter.

By connecting the dc-link middle point '$o$' to the neutral-point of the star-connected input filter capacitors, the dc-link voltage, $V_{pn}$, is split into dual voltage supplies, $V_{po}$ and $V_{no}$. The middle point '$o$' acts as a zero voltage neutral-point. The circuit given in figure 6.2 clearly resembles the Z-source NPC inverter. Using the dc-link middle point '$o$' as a reference, there are obviously three voltage levels available: $V_{po}$, $0V$ and $V_{no}$. At any instant, the inversion stage can be operated using these three voltage levels.

| Switch combination | | | | | | DC-link | | |
|---|---|---|---|---|---|---|---|---|
| $S_{ap}$ | $S_{bp}$ | $S_{cp}$ | $S_{an}$ | $S_{bn}$ | $S_{cn}$ | $V_{po}$ | $V_{no}$ | $V_{pn}$ |
| 1 | 0 | 0 | 0 | 0 | 1 | $V_{ao}$ | $V_{co}$ | $V_{ac}$ |
| 0 | 1 | 0 | 0 | 0 | 1 | $V_{bo}$ | $V_{co}$ | $V_{bc}$ |
| 0 | 1 | 0 | 1 | 0 | 0 | $V_{bo}$ | $V_{ao}$ | $V_{ba}$ |
| 0 | 0 | 1 | 1 | 0 | 0 | $V_{co}$ | $V_{ao}$ | $V_{ca}$ |
| 0 | 0 | 1 | 0 | 1 | 0 | $V_{co}$ | $V_{bo}$ | $V_{cb}$ |
| 1 | 0 | 0 | 0 | 1 | 0 | $V_{ao}$ | $V_{bo}$ | $V_{ab}$ |

Table 6.1: The switching combinations for the rectification stage (1 = on, 0 = off)

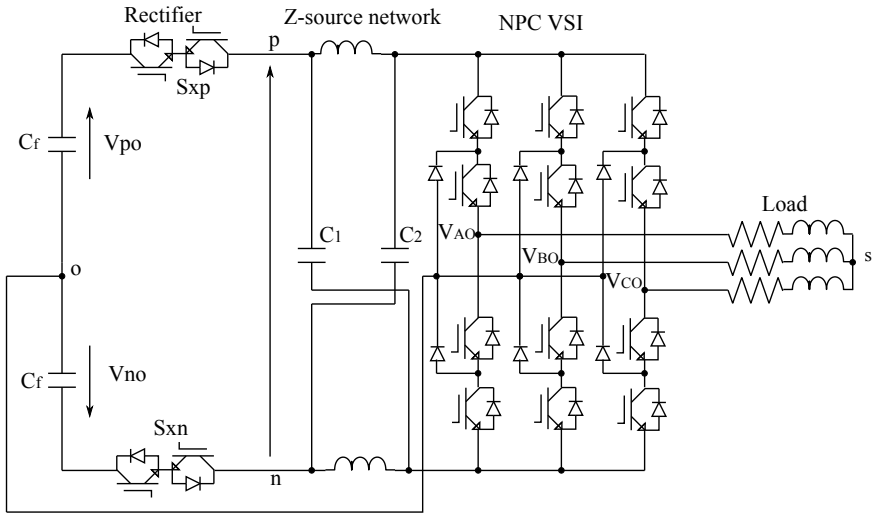



Figure 6.2: The equivalent state circuit of the three-level Z-source hybrid direct power converter with the rectification stage represented by using two conducting switches.

## 6.3 Circuit analysis

The circuit analysis for the Z-source NPC inverter has been given in Chapter 3. A similar analysis can be done for the three-level, Z-source hybrid direct power converter. Also, the different shoot-through states that can be used with the Z-source NPC inverter have been described in Chapter 3.

Figure 6.3 shows the simplified equivalent circuits for the converter during the non-shoot-through, upper-shoot-through and lower-shoot-through states. From figure 6.3(a), it is observed that the NPC inverter is transferring energy from the source to the load. In figure 6.3(b), the upper-shoot-through state is introduced by turning on the three upper switches in a phase leg of the inversion stage and simultaneously turning off the conducting lower bidirectional switch cell of the rectification stage. Energy from the source is therefore partially transferred to the load when in an upper-shoot-through state. A similar situation happens in figure 6.3(c) for the lower-shoot-through state. Through the proper combination of the above three possibilities, the inverter output voltage can be stepped up or down, as already verified in Chapter 3 for the Z-source NPC inverter.

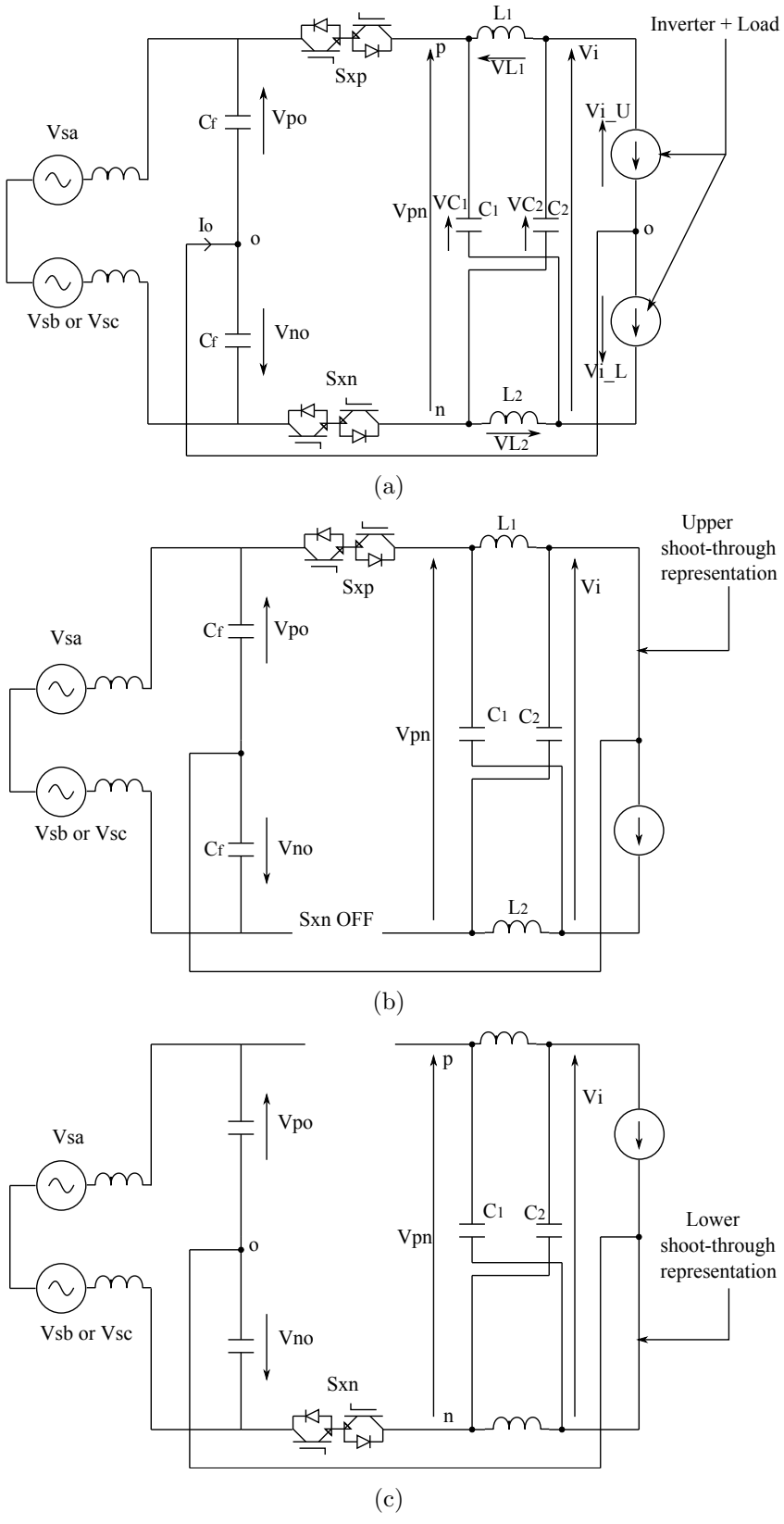



Figure 6.3: Simplified representation of the three-level Z-source hybrid direct power converter during (a) NST, (b) UST and (c) LST states

From figure 6.3(a), let us assume that the Z-source network is symmetrical ($L_1 = L_2 = L$ and $C_1 = C_2 = C$), then $V_{L_1} = V_{L_2} = V_L$ and $V_{C_1} = V_{C_2} = V_C$ and the voltage expressions for the non-shoot-through states, shown in figure 6.3(a), are as follows:

$$V_{po} = V_L + V_{i\_U}, \qquad V_{pn} = V_L + V_C, \qquad -V_{no} = V_L - V_{i\_L} \tag{6.1}$$

Similarly, the voltage expressions for the upper-shoot-through and lower-shoot-through states are as follows:

*Upper-shoot-through*

$$V_{i\_U} = 0, \qquad V_L = V_{po}, \qquad -V_{i\_L} + V_L = V_C \tag{6.2}$$

*Lower-shoot-through*

$$V_{i\_L} = 0, \qquad V_L = -V_{no}, \qquad V_{i\_U} + V_L = V_C \tag{6.3}$$

Let us assume that the duration of the UST and LST states are $T_u$ and $T_l$, respectively, and the switching period is $T_{sw}$. Also, we assume that $T_u$ and $T_l$ are equal (to ensure symmetrical operation) and denote the total combined UST and LST duration by $T_{ulst}$. At steady state, the average voltage across the inductors is zero; therefore, averaging the inductor voltages over one switching period, we have:

$$V_{C_1} = V_{C_2} = V_C = V_{pn} \cdot \left\{ \frac{T_{sw} - 0.5T_{ulst}}{T_{sw} - T_{ulst}} \right\} \tag{6.4}$$

Using (6.1) to (6.4), the voltages $V_{i\_U}$ and $V_{i\_L}$ appearing at the input of the NPC circuit can be expressed as follows:

$$\begin{aligned} V_{i\_U} &= (V_{no} + V_C) \cdot \left\{ \frac{T_{sw} - 0.5T_{ulst}}{T_{sw}} \right\} \\ V_{i\_L} &= (V_{po} - V_C) \cdot \left\{ \frac{T_{sw} - 0.5T_{ulst}}{T_{sw}} \right\} \end{aligned} \tag{6.5}$$

As noted in Chapter 5, the average values of $V_{po}$ and $V_{no}$ over a modulating period are equal. Therefore, from (6.5), it is noted that the split voltages, $V_{i\_U}$ and $V_{i\_L}$, fed to the NPC inverter will also have equal average values over a fundamental period. The equal average voltages can be guaranteed only if the modulation of the converter

is such that the average neutral-point current, $i_o$, over a switching period is zero. The expression for computing the line-to-line ac output voltage magnitude $\hat{V}_{out,LL}$ is also derived in (6.6), whose gain of $m_I/(1 - T_{ulst}/T_{sw})$ matches that produced by the traditional dc-ac Z-source NPC inverter.

$$\hat{V}_{out,LL} = m_R \cdot V_{pn} \cdot \left\{ \frac{m_I}{1 - T_{ulst}/T_{sw}} \right\} \tag{6.6}$$

As expected this converter has the same voltage buck-boost capability as the Z-source NPC inverter discussed earlier in section 3.3. However, unlike the Z-source NPC inverter, the complication introduced here is the need to simultaneously produce sinusoidal input and output waveforms in addition to voltage buck-boost capability. Realizing this additional requirement would need proper coordination of the rectification stage and inversion stage modulation to ensure that the neutral point current is zero during each switching period.

## 6.4 Space vector modulation

The SVM technique discussed in Chapter 5 can be applied to this converter by modifying the switching states to include upper and lower shoot-through states. The rectification stage is modulated in the same way as that described for the traditional two-stage matrix converter (Chapter 4) and will not be repeated here. Similarly, the modulation of the inversion stage is the same as that described in section 3.5.

### 6.4.1 Synchronization between input and output stages

The switching states of the rectification and inversion stages of the converter are synchronised within each switching interval. This ensures a balance of input currents and output voltages within a switching interval. To ensure that the converter is able to perform voltage buck-boost operation, shoot-through states are carefully inserted into selected output phase legs. The PWM switching pattern for modulating the

Z-source NPC inverter has been given in section 3.5. A similar procedure is applied to the inversion stage of this converter to enable voltage buck-boost capability.

As an example, let us consider the situation where the input current reference vector $\vec{I}_{in}$ is located in sector 2 while the output voltage reference vector $\vec{V}_{out}$ is located in triangle 4 of sector I. For the rectification stage, the selected current vectors are: $\vec{I}_1(ac)$ $(= \vec{I}_\gamma)$ and $\vec{I}_2(bc)$ $(= \vec{I}_\delta)$; the virtual vectors selected for the inversion stage are: $\vec{V}_{V_{M1}}$, $\vec{V}_{V_{L1}}$ and $\vec{V}_{V_{L2}}$. Based on the NTVV technique, these virtual vectors are formed by using the voltage vectors: $\vec{V}_{S1}$[ONN], $\vec{V}_{L1}$[PNN], $\vec{V}_{S2}$[PPO], $\vec{V}_{M1}$[PON] and $\vec{V}_{L2}$[PPN]. The voltage vectors are applied to the output according to the switching sequence: PPO $\rightarrow$ PPN $\rightarrow$ PON $\rightarrow$ PNN $\rightarrow$ ONN. To command voltage buck-boot operation, shoot-through states are inserted into selected phase legs as described earlier in section 3.5 to give the switching sequence: PPO $\rightarrow$ PPL $\rightarrow$PPN $\rightarrow$ PON $\rightarrow$ PNN $\rightarrow$ UNN $\rightarrow$ ONN.

In order to reduce the output voltage harmonic content, the selected voltage vectors for the inversion stage are arranged in a double-sided switching sequence but with unequal halves, with each half corresponding to the active times of the selected current vectors. Based on this example, the modulation pattern for the converter is shown in figure 6.4. The time interval for each voltage vector of the inversion stage's switching sequence can be determined using (6.7). Table A.2 shows all the switching sequences for the inversion stage for triangles 1 to 5 in all the six sectors of the space vector diagram shown in figure 2.2.

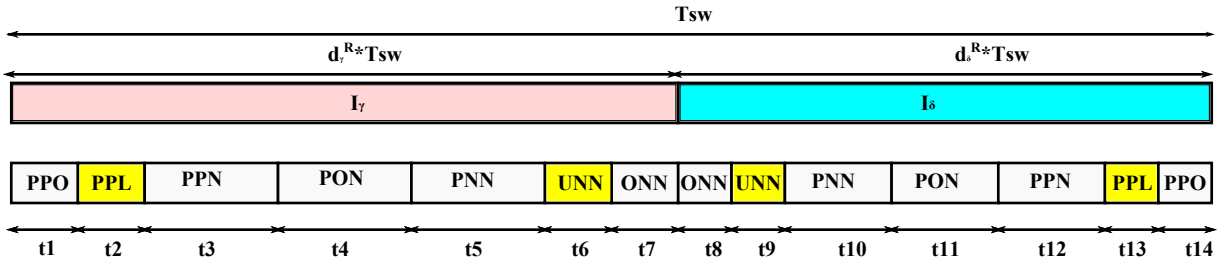



Figure 6.4: The switching pattern for the three-level Z-source hybrid direct power converter for the case where the input reference vector, $\vec{I}_{in}$, is located in sector 2 while the output reference vector, $\vec{V}_{out}$, is located in triangle 4 of sector I.

$$
\begin{aligned}
t_1 &= \frac{1}{3} \cdot d_z \cdot d_\gamma^R \cdot T_{sw} - \frac{1}{2} \cdot d_\gamma^R \cdot T_l \\
t_2 &= \frac{1}{2} \cdot d_\gamma^R \cdot T_l \\
t_3 &= d_x \cdot d_\gamma^R \cdot T_{sw} \\
t_4 &= \frac{1}{3} \cdot d_z \cdot d_\gamma^R \cdot T_{sw} \\
t_5 &= d_y \cdot d_\gamma^R \cdot T_{sw} \\
t_6 &= \frac{1}{2} \cdot d_\gamma^R \cdot T_u \\
t_7 &= \frac{1}{3} \cdot d_z \cdot d_\gamma^R \cdot T_{sw} - \frac{1}{2} \cdot d_\gamma^R \cdot T_u \\
t_8 &= \frac{1}{3} \cdot d_z \cdot d_\delta^R \cdot T_{sw} - \frac{1}{2} \cdot d_\delta^R \cdot T_u \\
t_9 &= \frac{1}{2} \cdot d_\delta^R \cdot T_u \\
t_{10} &= d_y \cdot d_\delta^R \cdot T_{sw} \\
t_{11} &= \frac{1}{3} \cdot d_z \cdot d_\delta^R \cdot T_{sw} \\
t_{12} &= d_x \cdot d_\delta^R \cdot T_{sw} \\
t_{13} &= \frac{1}{2} \cdot d_\delta^R \cdot T_l \\
t_{14} &= \frac{1}{3} \cdot d_z \cdot d_\delta^R \cdot T_{sw} - \frac{1}{2} \cdot d_\delta^R \cdot T_l
\end{aligned}
\tag{6.7}
$$

## 6.5 Simulation results

To verify the findings proven earlier, the three-level, Z-source hybrid direct power converter was first simulated with SABER® based on the specifications as presented in Appendix B. The simulation exercise is divided into two parts, namely buck and boost modes, respectively.

## 6.6 Buck mode

For the buck mode of operation the parameters used are $m_R$=1.0, $m_I$=0.9 and $T_{ulst}/T_{sw}$=0.0. The input current waveforms, shown in figure 6.5, are sinusoidal and balanced. This shows the ability of the modulation strategy to control the converter to generate a set of balanced, sinusoidal input currents.

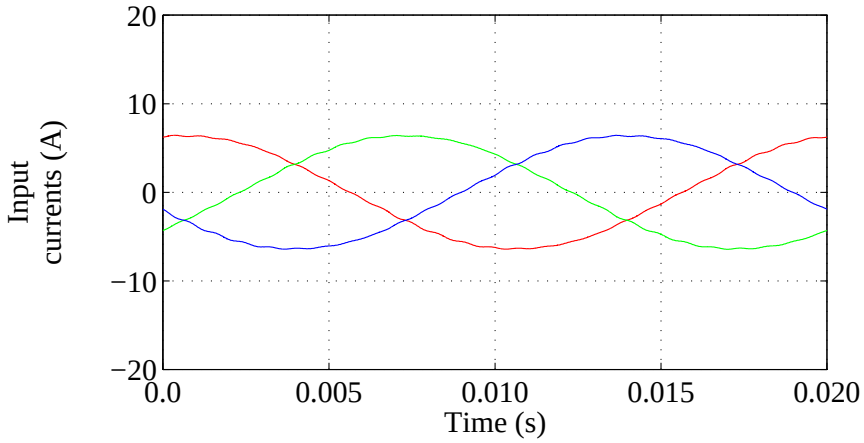



Figure 6.5: Input currents when controlled with $m_I$=0.9 and $T_{ulst}/T_{sw}$=0.0.

Figure 6.6 shows the dc-link voltage provided by the rectification stage. Since no zero vectors are used in the rectification stage's modulation, this voltage does not touch zero and its average value is not constant but variable.

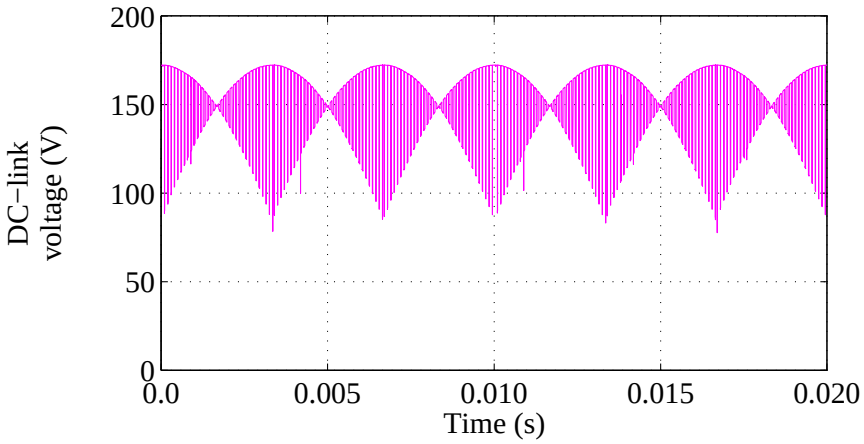



Figure 6.6: Full dc-link voltage when controlled with $m_I$=0.9 and $T_{ulst}/T_{sw}$=0.0.

By splitting the variable voltage $V_{pn}$ into dual voltage supplies, the inversion stage is supplied with $V_{po}$ and $V_{no}$, which are also variable, as shown in figure 6.7.

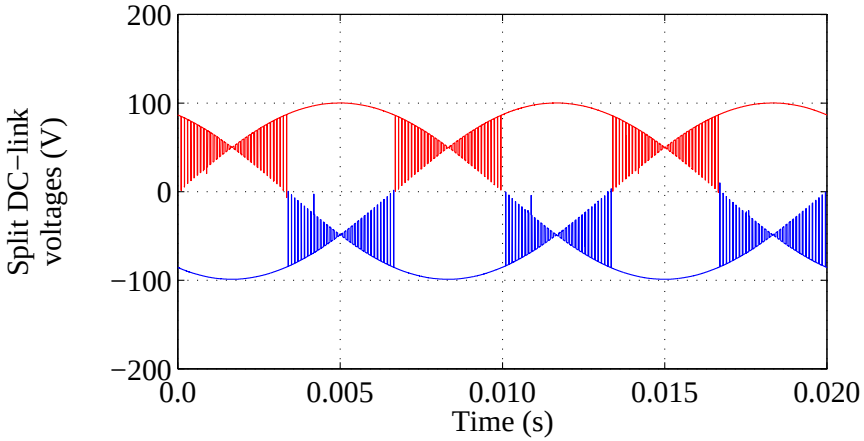



Figure 6.7: Split dc-link voltages when controlled with $m_I$=0.9 and $T_{ulst}/T_{sw}$=0.0.

In order to demonstrate the ability of the converter to generate multilevel outputs, figure 6.8 presents the output waveforms generated by this topology. The spectra of the output line-to-line voltage is shown in figure 6.8(a), where it is noted that the magnitude of the fundamental component is 135V ($m_R \cdot m_I \cdot V_{pn,avg}$ = 1.0×0.9×150 = 135V), exactly the same value as a three-level, two-stage matrix converter would produce under similar conditions. From figure 6.8(b), the line-to-line voltage consists of five levels which evidently proves the ability of the converter to generate multi-level output voltages. To examine whether the voltage levels are properly applied to generate the desired outputs, the load currents of the converter are shown in figure 6.8(c). These currents are clearly balanced and sinusoidal.

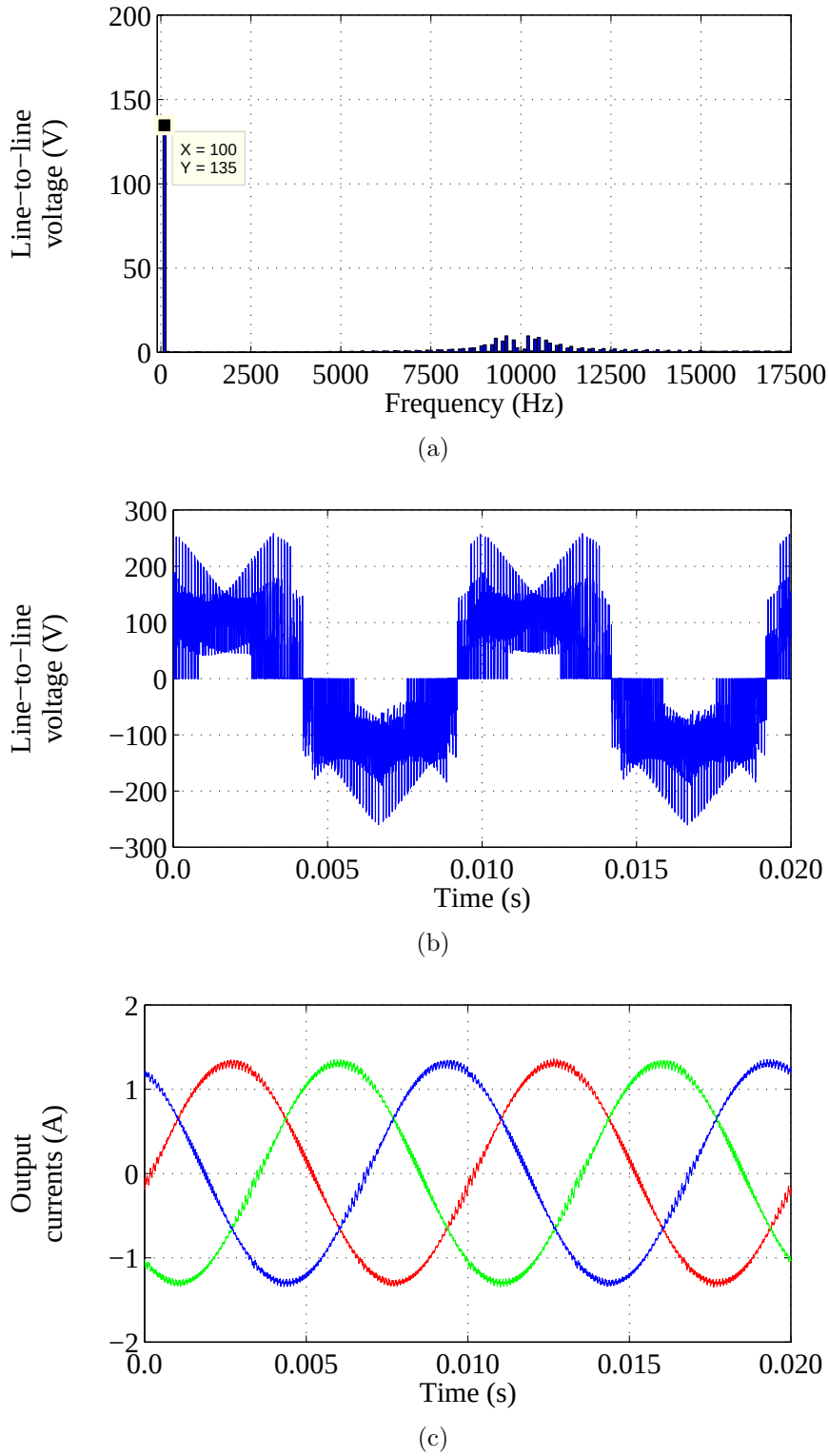



Figure 6.8: The output waveforms generated by the three-level, Z-source hybrid direct power converter when $m_I$=0.9 and $T_{ulst}/T_{sw}$=0.0.

## 6.7 Boost mode

To command boost operation, shoot-through states are inserted into selected phase legs of the inversion stage. The parameters used are $m_R = 1.0$, $m_I = 0.9$ and $T_{ulst}/T_{sw} = 0.1732$.

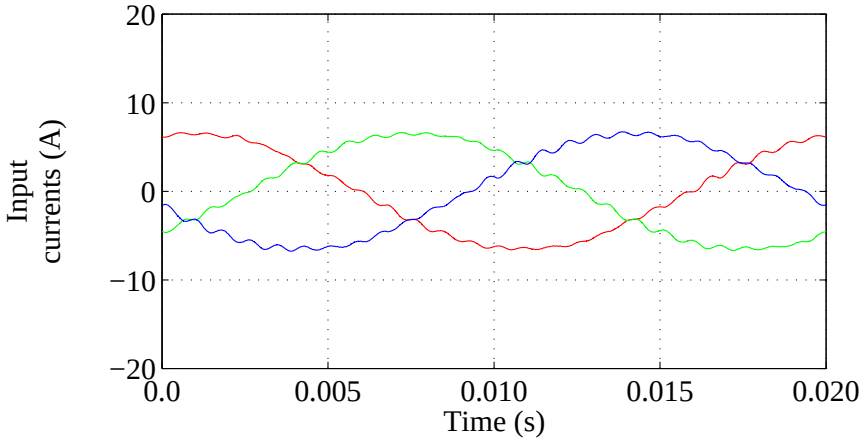



Figure 6.9: Input currents when controlled with $m_I$=0.9 and $T_{ulst}/T_{sw}$=0.1732.

The input currents are shown in figure 6.9, which clearly shows that the currents are still balanced and sinusoidal. It must be commented that the input filter capacitors are bigger than what would normally be used in a standard three-level, two-stage matrix converter. This is because these capacitors not only have to filter out the high frequency input current components but also have to provide a low impedance path for the input currents during the boost mode when shoot-through states are applied and the rectifier is decoupled from the Z-source network. Using small input filter capacitors will result in very large ripples on the current waveforms. However, since there is a limit of capacitance that can be used for the input filter, we are not able to eliminate all the ripples completely but they are within acceptable limits.

As discussed in Chapter 3, the capacitance and inductance of the Z-source network are selected based on the acceptable ripple levels of the capacitor voltage and inductor current, respectively. It has been shown in [112] that Z-source passive component sizes for this topology depend heavily on the system voltage-to-current ratio for a defined

rating. It is also anticipated that the interaction of the input filter and Z-source network may lead to stability issues for this topology which has not been considered in this work.

Figure 6.10 shows the dc-link voltage provided by the rectification stage. It is clear that the dc-link voltage provided by the rectification stage essentially remains unaffected by the insertion of shoot-through states. By splitting the variable voltage $V_{pn}$ into dual voltage supplies, the inversion stage is supplied with $V_{po}$ and $V_{no}$, which are also variable, as shown in figure 6.11.

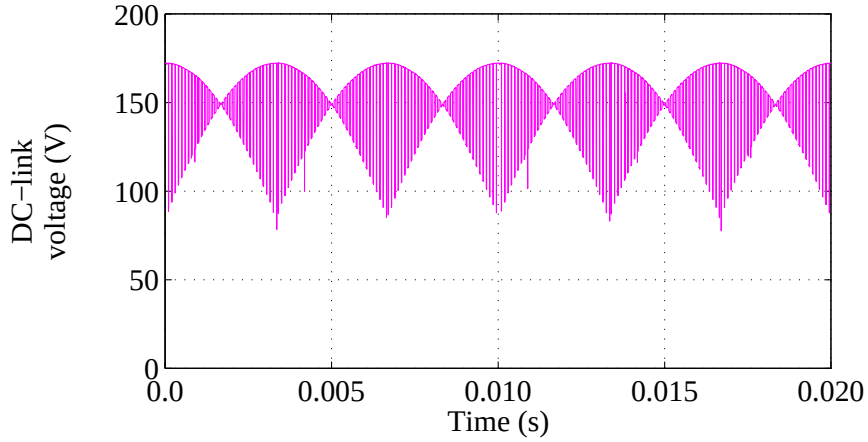



Figure 6.10: Full dc-link voltage when controlled with $m_I = 0.9$ and $T_{ulst}/T_{sw} = 0.1732$.

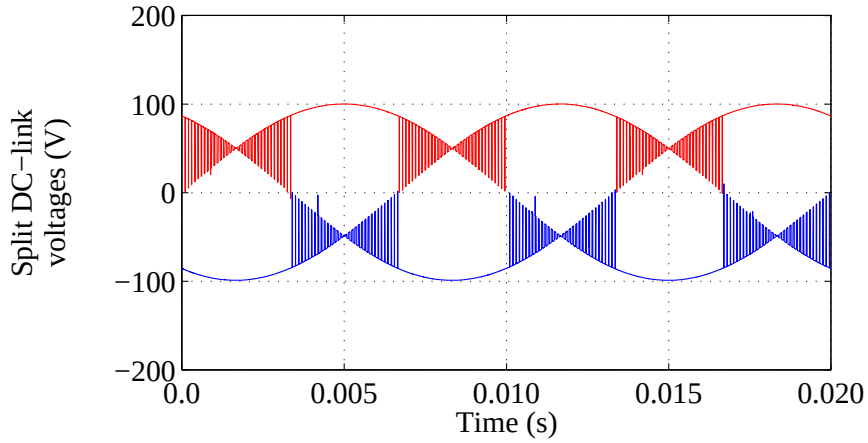



Figure 6.11: Split dc-link voltages when controlled with $m_I = 0.9$ and $T_{ulst}/T_{sw} = 0.1732$.

In order to show that the converter can produce a voltage transfer ratio higher than 86.6%, we refer to figure 6.12. The spectra of the output line-to-line voltage of the converter is shown in figure 6.12(a). From this figure, it is noted that the magnitude of the fundamental component is 163V (94%) which is higher than the intrinsic maximum voltage ($100 \cdot \sqrt{3} \cdot 0.866 = 150$V) that can be produced by the three-level, two-stage matrix converter operating with a supply phase peak voltage of 100V. Figure 6.12(b) shows the output line-to-line voltage of this converter which clearly displays the boosted five-level voltage. The load currents are also shown in figure 6.12(c) which are still fairly balanced and sinusoidal even though shoot-through states have been intentionally inserted into the various output phase legs.

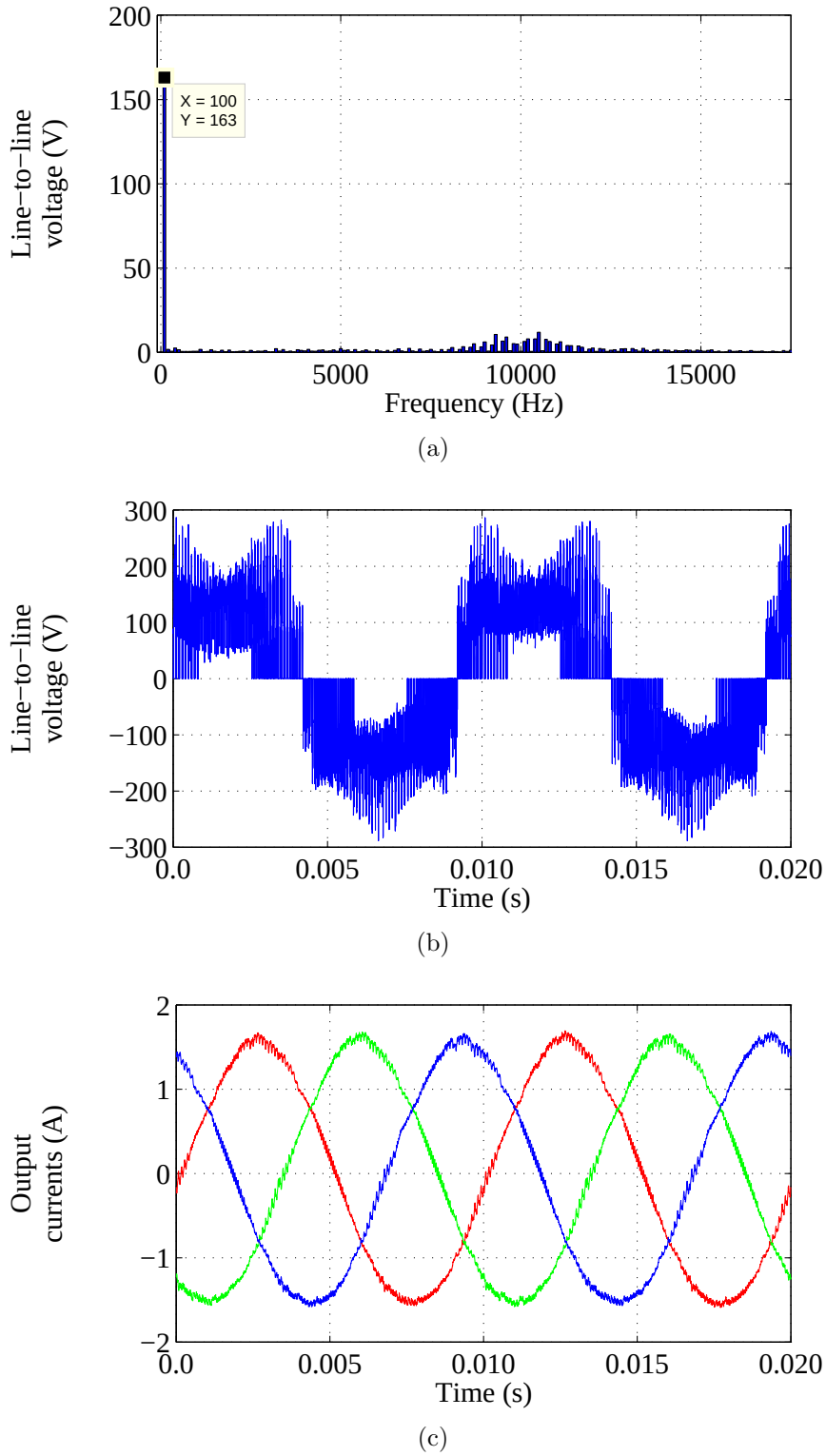



Figure 6.12: Boosted output waveforms of the three-level, Z-source hybrid direct power converter (a) spectra of output line-to-line voltage, (b) output line-to-line voltage and (c) output line currents when $m_I$=0.9 and $T_{ulst}/T_{sw}$=0.1732.

## 6.8 Conclusions

In this chapter, the principle of operation and modified SVM technique for controlling the three-level, Z-source hybrid direct ac-ac power converter has been presented. The hybrid converter can provide a voltage transfer ratio of more than 86.6% (94% in this case) as well as produce sinusoidal input and output quantities. Achieving these benefits is not at all trivial and calls for the proper coordination of the modulation of the rectification and inversion stages, a careful insertion of shoot-through states in the output state sequence as well as controlling the average neutral-point current to be zero over each switching period. The findings presented in this chapter are promising, and have been verified in simulation. The design and construction of a laboratory prototype converter is presented in Chapter 7 to validate these findings with experimental results.

# Chapter 7

# Experimental Converter

## 7.1 Introduction

This chapter presents the design and construction of the experimental converter used to validate the work presented in this thesis. The measurement circuits, power circuits, protection circuit and gate drives used throughout this work are described in detail. Also, the control hardware used to implement the space vector modulation for the converter are introduced in this chapter.

## 7.2 Converter design

To validate the simulation work carried out in the previous chapters a Z-source NPC inverter and a *3 x 2* matrix converter are required. The *3 x 2* matrix converter is used to provide a split dc supply for the Z-source NPC inverter. The resulting converter is called a three-level, Z-source hybrid direct ac-ac power converter in this thesis. Converter modulation is implemented using a DSP and an FPGA with a series of circuits which allow information such as gate drive signals and measurement signals

to be transferred to and from the power PCB boards. Figure 7.1 shows a schematic of the entire system used for the converter control. A photograph of the complete experimental converter is shown in figure 7.2. Details of the key parts of this converter are now discussed.

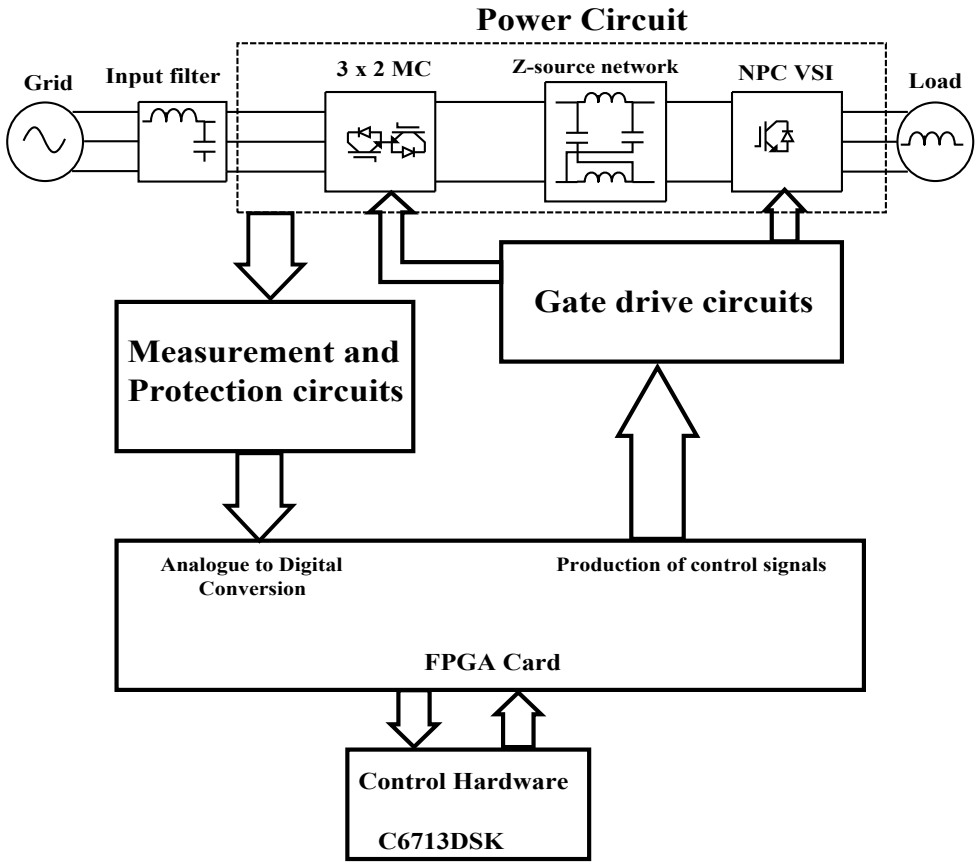



Figure 7.1: The overall prototype system block diagram.

### 7.2.1 Measurement circuits

The measurements required for the converter control are the three input phase voltages, the clamp capacitor voltage for protection purposes and the three load currents. The four voltages are measured using LEM LV 25-P voltage transducers. These transducers have an isolation voltage of several kilovolts and can measure up to 600V. The load currents are continuously monitored using three current transducers, LEM LAH 25-NPs, to ensure that the prototype converter does not operate at over the maximum

current level. The output of both of these transducers is a current proportional to the primary side signal (voltage or current). This signal is terminated on the FPGA card with a burden resistor to convert the signal to a voltage. This method of termination aids in the noise immunity of the transmitted signals.

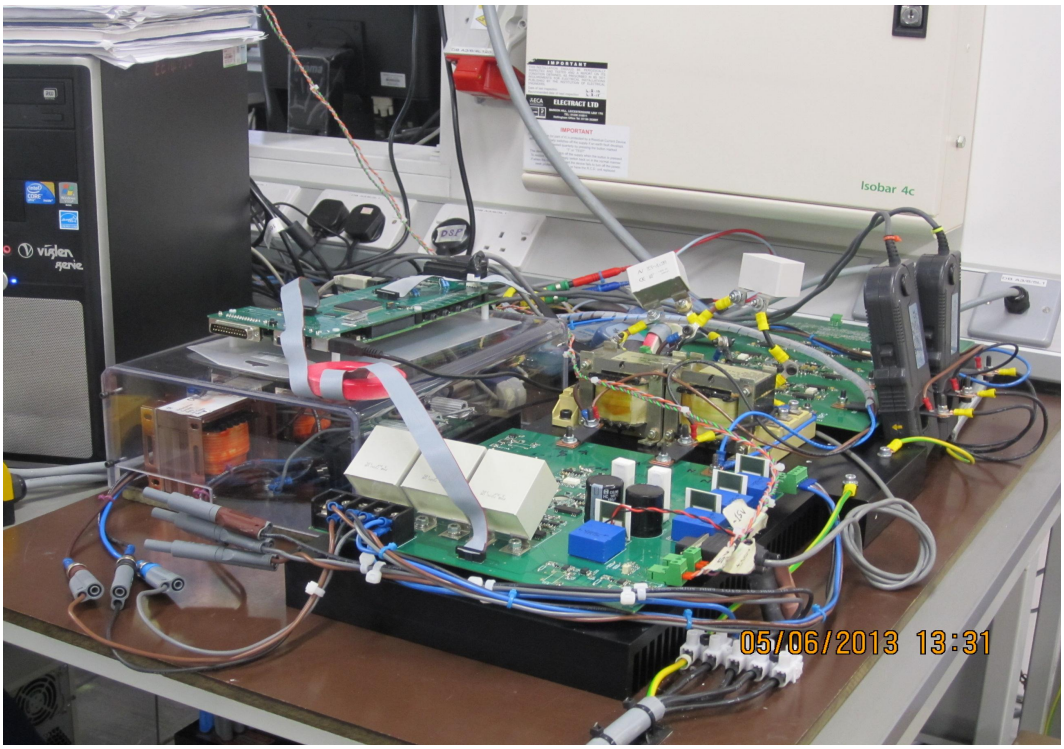



Figure 7.2: The overall prototype three-level, Z-source hybrid direct power converter.

Commutation of current between the bidirectional switch cells in the *3 x 2* matrix converter is achieved using the relative-voltage-magnitude-based commutation technique described in Chapter 4. The relative magnitudes of the input phase voltages are compared using voltage sign detection circuits and this information along with the modulation demand enables the FPGA control program to determine the correct commutation sequence and transmit it to the gate drives. The gate drives provide electrical isolation between the control platform and the power circuit and convert the logic level outputs from the FPGA into levels suitable for driving power semiconductor devices.

In order to apply the relative-voltage-magnitude-based commutation strategy to the

rectification stage, three voltage direction detection circuits (figure 7.3) were built to determine the signs of the input line-to-line voltages applied to the bidirectional switches. As shown in this figure the potential divider ($R_1$ and $R_2$) generates an output voltage ($V_+$) that is a fraction of the input voltage for the comparator. For this case the input voltage is $V_{ab}$. By using the back-to-back Schottky diodes, $V_+$ is limited to $\pm 0.7$V and is used as a non-inverting input for the comparator. This non-inverting input is compared with the inverting input, which is connected to the common 'ground' ($V_b$), to determine the voltage direction. For the case where $V_a > V_b$, the comparator generates a high logic signal. A capacitor is connected across the inputs of the comparator to filter out the high frequency jittering that occurs at the zero crossing of the voltage.

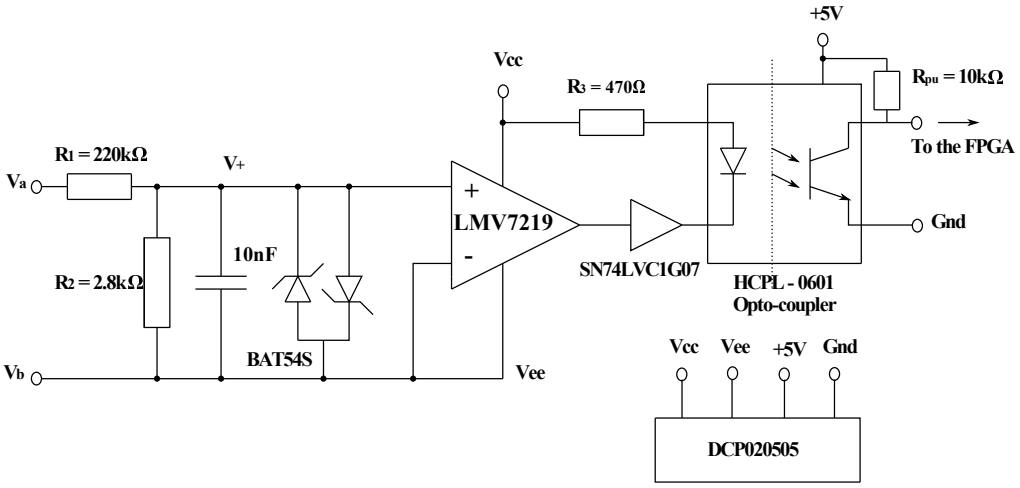



Figure 7.3: The schematic diagram of the voltage direction detection circuit.

Since an input phase voltage is used as the reference point for the voltage direction detection circuit, an isolated power supply (DCP020505) is needed. An opto-coupler is also needed to provide the electrical isolation between the high input voltages and the control platform. A buffer, SN74LVC1G07, is used to drive the opto-coupler in order to generate the logic signal for the FPGA according to the comparator's output state.

### 7.2.2 Power and protection circuits

For the experimental verification of the prototype converter, a 7.5kW three-level, Z-source hybrid direct power converter has been built. As discussed in Chapter 6, this converter consists of a rectification stage and an inversion stage. The rectification stage uses six Semikron SK60GM123 IGBT modules (60A/1200V), with each IGBT module connected in common-emitter configuration to form a bidirectional switch cell. The IGBT modules are mounted directly onto a custom-designed six-layer PCB where the supply (three-phase voltage supply) and output terminals (dc-link points: $p$, $o$ and $n$) of the rectifier are placed on either side of the PCB, as shown in figure 7.4.

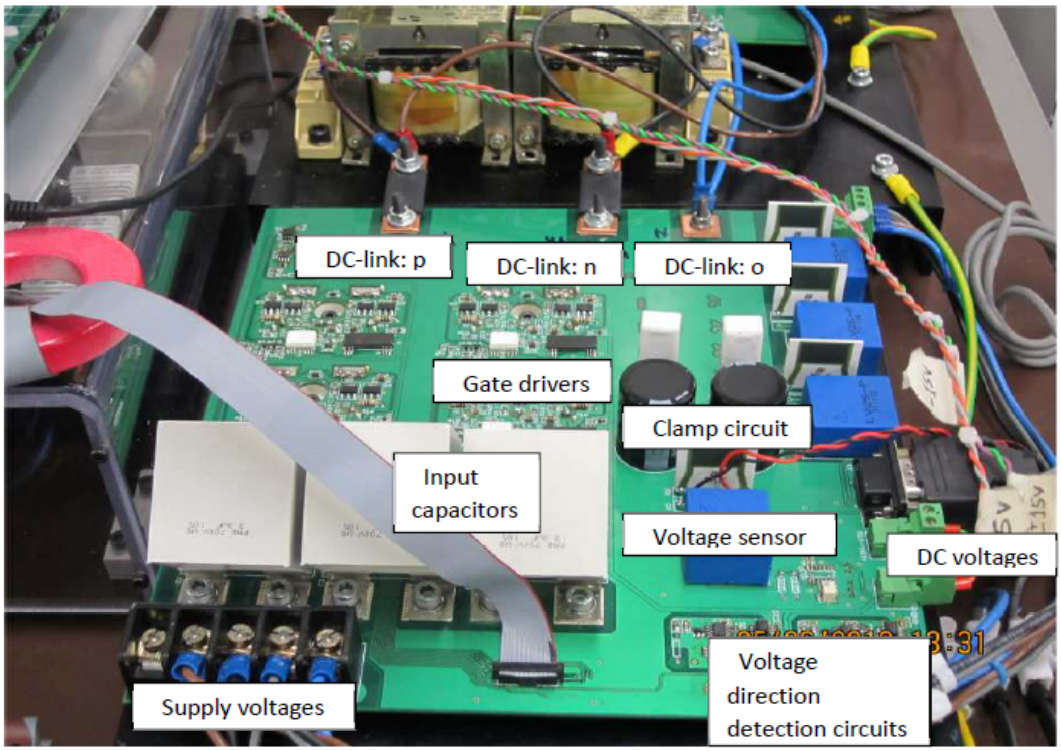



Figure 7.4: The rectification stage circuit board

The top layer of this multi-layer PCB is the signal plane that consists of the gate drive circuits, the gate signal tracks and the dc voltage supply tracks. Each gate drive circuit is built close to its respective IGBT module to ensure a smooth commutation process and reduce any parasitic effects. The input filter capacitors are connected

close to the input terminals on the PCB in order to reduce the stray inductance in the device conductive loops.

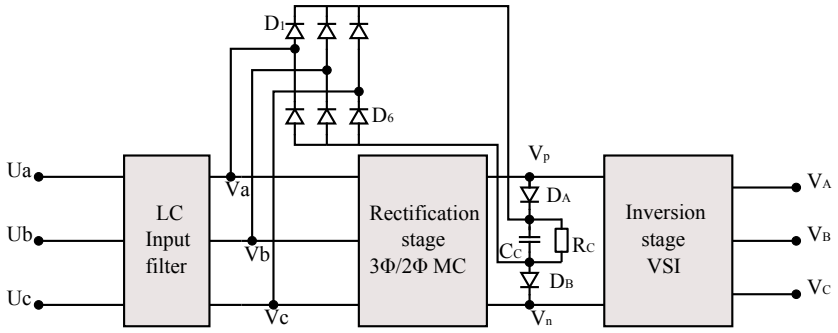



Figure 7.5: A clamp circuit configuration for two-stage matrix converters

To connect the IGBT modules to the input and output terminals, the three inner layers of the PCB are used as the power planes. Each power plane provides the power rails that represent the input voltage connections, the neutral-point track ($o$), the positive ($p$) and negative ($n$) dc-links. The neutral-point plane provides a connection from the dc-link middle point '$o$' to the neutral-point of the star-connected input filter capacitors. By using the power planes the connection inductance to the IGBT modules is minimized. The first inner layer closest to the top layer is used as a ground plane so that radiated noise from the signal tracks and power planes is mainly confined within the substrate between the planes and the ground plane instead of being coupled to one another.

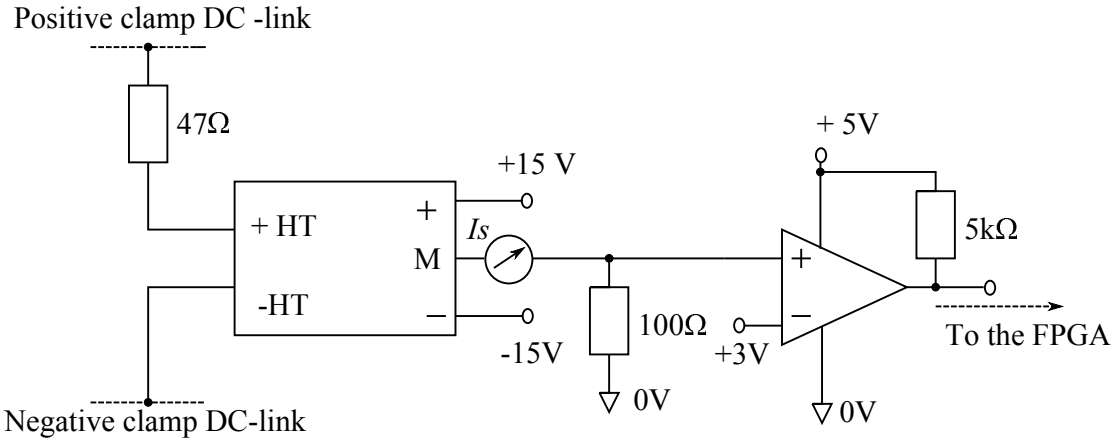



Figure 7.6: The over-voltage detection circuit

As shown in figure 7.4, a clamp circuit is built on the PCB of the rectification stage. The clamp circuit is a protection circuit that limits the over-voltage level on the supply side and dc-link of the converter in order to ensure safe operation. For this prototype, eight 8EWF12S fast recovery diodes were used to construct the clamp circuit, which have been placed on the bottom layer of the PCB. Each diode has a rating of 1200V, 8A. During over-voltage, the converter is shut down and the fast-recovery diodes provide paths for the dc-link current to charge up two series-connected electrolytic capacitors of 150$\mu$F, 450V. The stored energy is then dissipated by the 47k$\Omega$ resistor that is connected in parallel with each capacitor. The schematic of the clamp circuit is shown in figure 7.5.

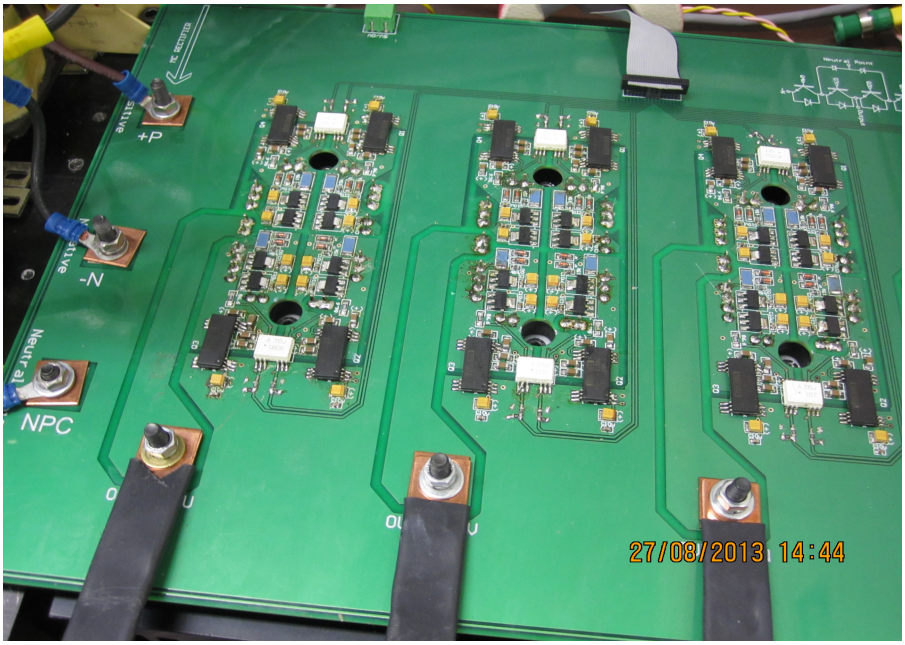



Figure 7.7: The PCB for the inversion stage of the prototype converter.

To detect an over-voltage, a detection circuit was built to monitor the clamp circuit dc-link voltage. Referring to figure 7.6, the dc-link voltage of the clamp circuit is measured using a LEM LV 25-P voltage transducer. The reference voltage for the transducer is the non-inverting input of the comparator. A maximum value of 600V has been set for this converter. The comparator will generate a high logic signal for the FPGA if the clamp circuit dc-link voltage is higher than 600V.

The inversion stage of this converter requires three APTGL60TL120T3G NPC modules, as shown in figure 7.7. Each APTGL60TL120T3G NPC module comprises four series-connected IGBTs with anti-parallel diodes and two clamping diodes. Connection between the rectification and inversion stages is through a Z-source network. Heat sinks are attached to the IGBT modules for cooling purposes.

### 7.2.3 Gate drive circuits

A gate signal is required for the turn-on and turn-off of the power semiconductor devices. The requirement of the gate drive depends on the type of semiconductor device and their voltage/current rating. For this converter, IGBT switching devices are used to construct the front-end rectifier and the back-end NPC inverter, respectively. Like the MOSFET, the IGBT is a voltage-controlled switching device that requires very small current when gated, leading to a simple gate drive design.

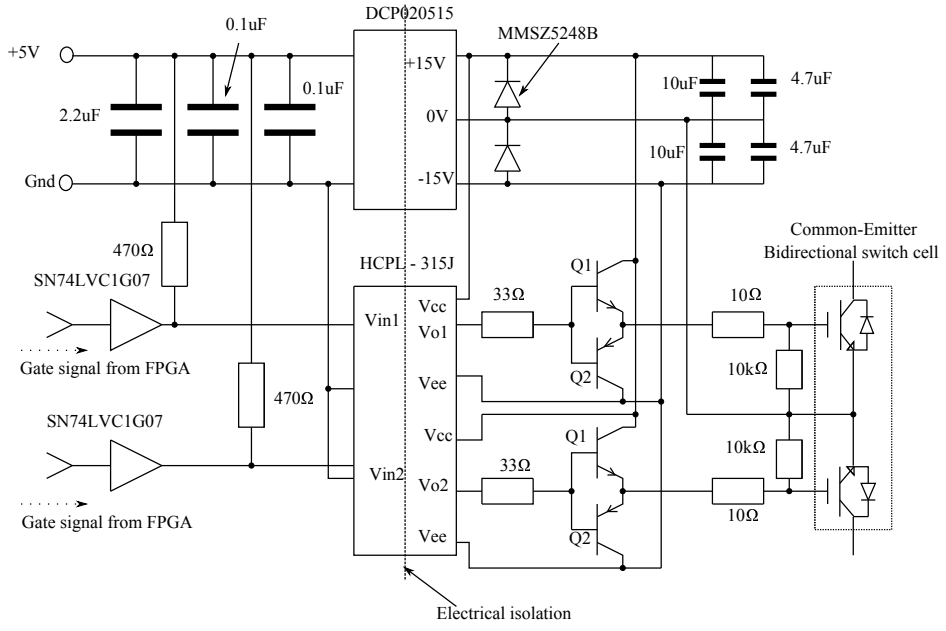



Figure 7.8: The schematic diagram of the gate drive for the bidirectional switch cells.

The *3 x 2* matrix converter PCB contains the gate drive circuits for the bidirectional switch cells. Figure 7.8 shows the gate drive schematic for the common-emitter bidi-

rectional switch cell arrangement used in the rectification stage of the converter. This bidirectional switch cell is constructed using two IGBTs and therefore requires two gating signals. The gate drive consists of an HCPL-315J high speed opto-coupler, capable of driving 0.5A peak current into two IGBTs or MOSFETs. The logic side of the opto-coupler is driven by an open collector gate which is connected to the interface electronics of the gate drive circuit. Each opto-coupler is supplied by an isolated ±15V supply provided by Texas Instruments DCP020515DU 2W, 5V to ±15V converter.

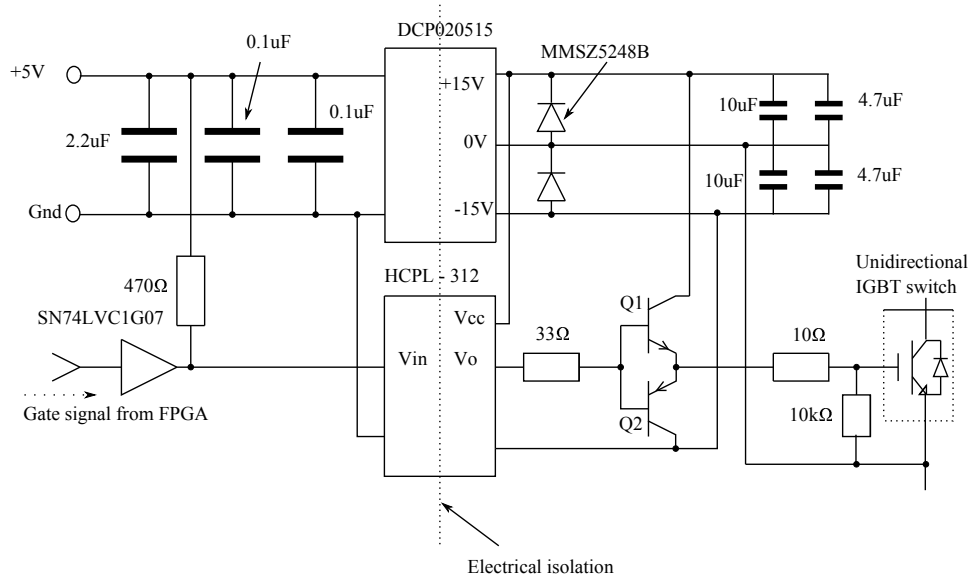



Figure 7.9: The schematic diagram of the gate drive circuit used for the unidirectional switch cell in the inversion stage.

The outputs of the opto-coupler are fed to two push-pull amplifiers, formed with discrete NPN and PNP transistors (FZT790A and FZT690B) whose outputs are fed to the IGBTs through 10Ω gate resistors. These resistors were selected to drive the IGBTs as quickly as possible, in an effort to reduce switching losses in the converter whilst not allowing the gate circuit to resonate as a result of the stray inductance in the circuit and the capacitance around the IGBTs and diodes.

Each IGBT gate is protected from over-voltages at the gate by two 15V zener diodes (not shown) connected back to back. These diodes ensure that the gate is never exposed to a device voltage greater than the maximum of 20V. A final 10kΩ resistor

is connected across the gate-emitter connection of each IGBT. This resistor ensures that in the absence of a drive circuit, such as may occur if the opto-coupler or miniature power supply fails, the gate emitter capacitance cannot charge via the parasitic capacitance in the device resulting in an unexpected turn on.

The inversion stage uses unidirectional switches; a schematic of the gate drive circuit used for the unidirectional switch is shown in figure 7.9. This gate drive is essentially the same as that used for the bidirectional switch cells.

## 7.3 Control platform

The SVM techniques described in the simulation chapters are applied experimentally through a combination of an Actel FPGA card, designed by the Power Electronics Machines and Control group of the University of Nottingham and a Texas Instruments C6713DSK board.

### 7.3.1 FPGA card

In order to gather sufficient data for effective modulation and protection, the FPGA board provides 10 channels for A/D conversions and 11 channels for digital inputs. A photograph of the FPGA card is shown in figure 7.10. Figure 7.11 shows the measured variables connected to the FPGA card in this prototype. Operated with a clock frequency of 50MHz, the FPGA retrieves data from the 12-bit A/D conversion channels and digital input channels, then stores this information in registers which are memory mapped into the DSP's external memory interface. Thus the DSP has access to registers containing the sampled signals which are required for the space vector modulation. The FPGA creates an interrupt for the DSP at a frequency of 10kHz. The interrupt routine carries out the space vector modulation as shown in simulations, and sends data to the FPGA regarding the switching requirements for

the next interrupt period. By interpreting control signals from the DSP, the FPGA determines the sequence of the switching signals to be transmitted to the gate drives via the output pins.

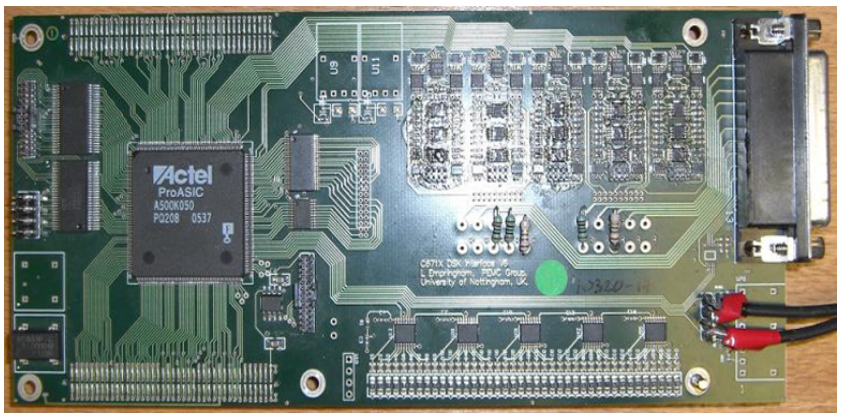



Figure 7.10: The FPGA card used for this prototype.

For the safe commutation of current between the switching devices of the converter, the FPGA is programmed to perform the relative-voltage-magnitude-based commutation for the bidirectional switches of the rectification stage. No dead-time is employed for the unidirectional switches of the inversion stage because of the presence of the Z-source network.

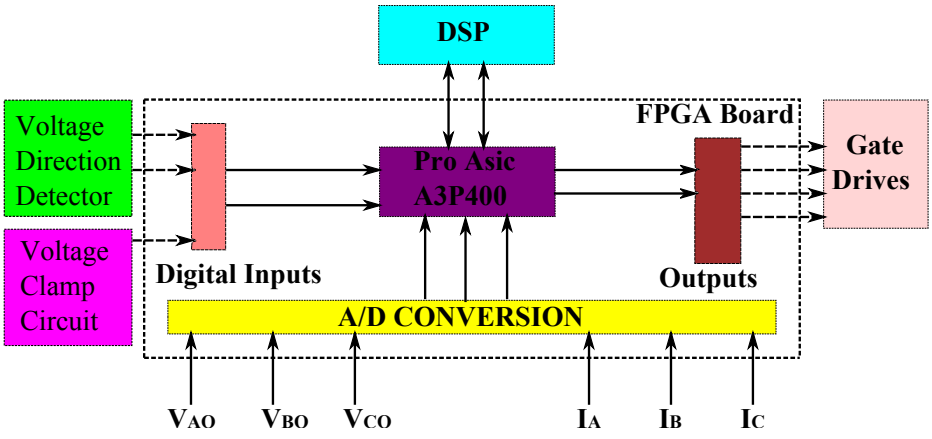



Figure 7.11: The inputs and outputs of the FPGA card.

The FPGA also has several safety circuits. A comparator on the FPGA board can monitor transducer output signal so that if the output current or clamp capacitor voltage rises above a certain threshold, all of the switches are turned off and the

phase enable line is taken low. The converter trip can also be triggered in software by sending a signal to the trip register inside the FPGA.

A watchdog timer is included inside the FPGA program. This is simply a timer that resets every time it receives a signal from the DSP. This signal is sent at the start of every interrupt routine. Failure to reset this timer, and therefore allowing it to overflow, will result in the converter tripping. This ensures that if communication is lost between the DSP and FPGA board, the converter will turn off.

### 7.3.2 C6713DSK

The C6713 is a 32-bit floating point, high performance DSP which can be programmed in C using Code Composer Studio from Texas Instruments. The main purpose of the DSP is to calculate the switching signal requirements for the modulation.

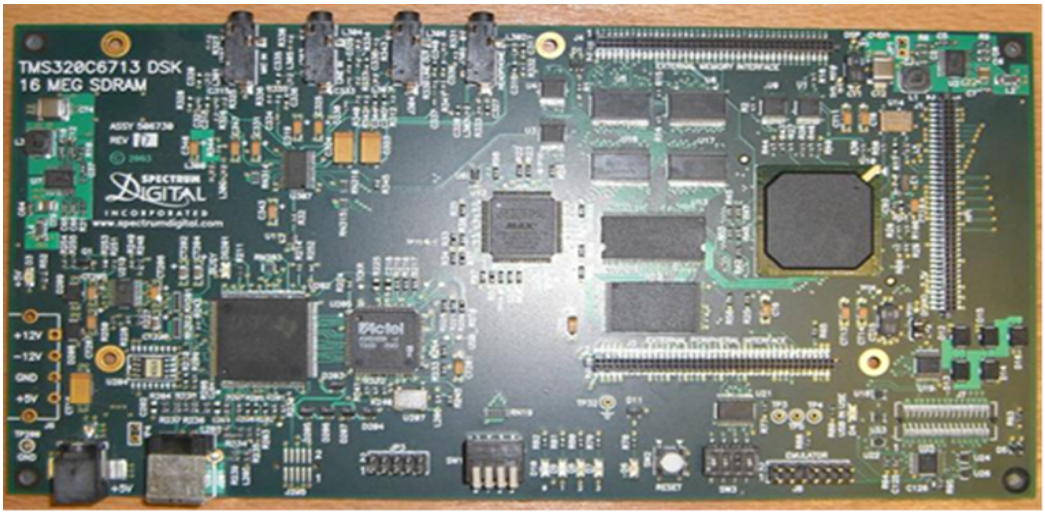



Figure 7.12: The Texas C6713 DSP card.

The FPGA card is directly memory mapped in the DSK's memory by using the External Memory Interface (EMIF) connector on the DSK. This enables the DSP to have access to all of the digitally converted transducer outputs as well as to registers giving feedback on the converter status such as trips. A photograph of the C6713 DSK card is shown in figure 7.12.

## 7.4 Conclusions

This chapter has described the design and construction of a three-level, Z-source hybrid direct ac-ac power converter. The design and functionality of the control and interface circuits have also been described. This converter will be used to validate the modulation methods presented in previous chapters.

# Chapter 8

# Experimental Results

## 8.1 Introduction

To verify the simulation and theoretical work presented in this thesis the three-level, Z-source hybrid direct ac-ac power converter (3ZHDPC) design presented in Chapter 7 has been practically implemented. This chapter presents the experimental results for this converter and the Z-source NPC inverter using the modified SVM schemes and directly compare them with simulation results to ensure validity.

## 8.2 Experimental setup

The experimental converter is arranged so that results can be captured in order to validate the NTV and NTVV schemes developed in Chapter 3 for the REC Z-source NPC inverter. A similar exercise is implemented to capture results in order to validate the NTVV scheme developed in Chapter 6 for the 3ZHDPC. Results are taken using a LeCroy Waverunner 6050 oscilloscope using a combination of differential voltage probes and currents probes.

## 8.3 Z-source NPC inverter results

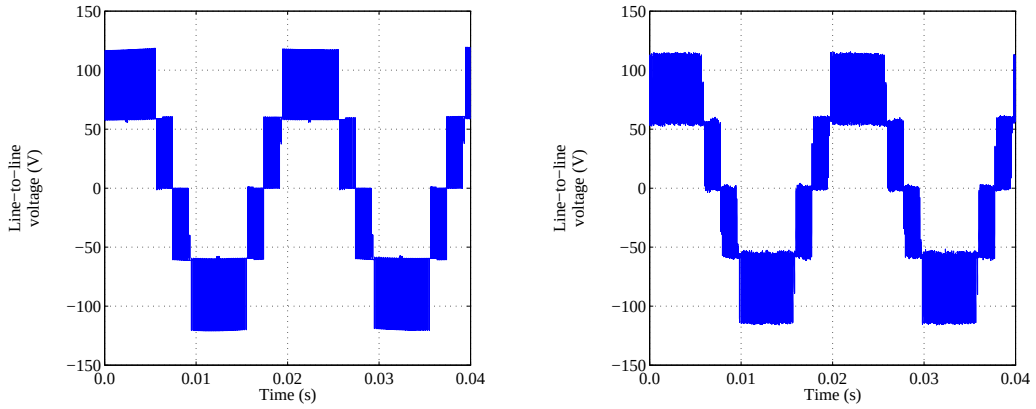
The inversion stage of the prototype converter was fed by a split dc supply to capture results for the Z-source NPC inverter. Both the NTV and NTVV SVM techniques for controlling the Z-source NPC inverter described in sections 3.4 and 3.5 have been validated experimentally. A balanced R-L load consisting of 57.6-Ω resistive bank and 10-mH inductive bank readily available in the laboratory was used. The Z-source network was implemented using 6.3-mH inductors and 2200-$\mu$F capacitors and fed by a 120-V dc supply. The voltage buck-boost capability of the Z-source NPC inverter has been demonstrated. The following subsections present the results obtained from the Z-source NPC inverter.

### 8.3.1 Control with NTV SVM technique

In order to validate the modelling strategy presented in section 3.4 and to demonstrate the viability of the NTV SVM algorithm, a simulation has been run with the same conditions as the experimental work and the results compared with the experimental results. These results are compared for both the buck and boost modes of operation.

#### 8.3.1.1 Buck mode of operation

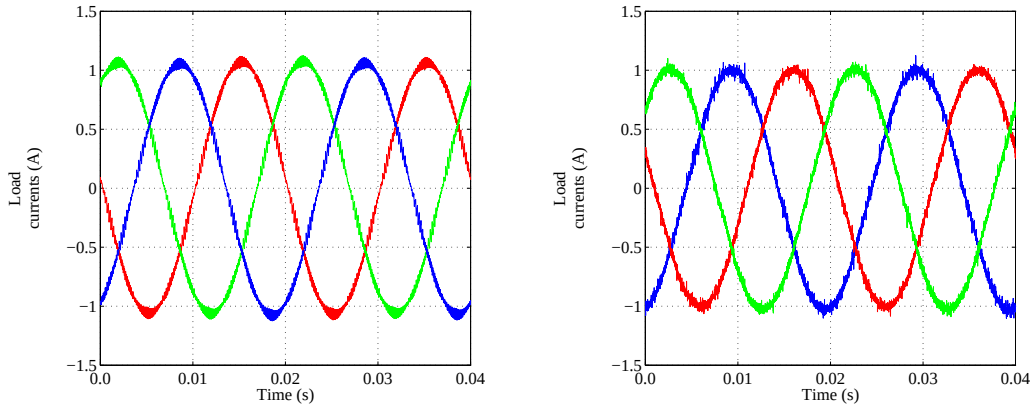
The converter is first operated in the buck mode by setting the modulation index to $m_I$=0.9 and shoot-through ratio to $T_{ulst}/T_{sw}$=0.0, respectively. With these parameters the maximum level of the output line-to-line voltage that can be achieved is limited to (120 - $2v_D$). With $v_D$ = 0.7V, the expected maximum level of the output voltage is 118.6V. The simulation and experimental results are shown in figure 8.1. It is clearly seen in figure 8.1(a) that the inverter dc-link voltage is not boosted and the maximum level of the output line-to-line voltage is maintained at 118.6V by the dc source in simulations. The experimental output line-to-line voltage, shown in figure 8.1(b), clearly matches the simulation results.




(a) (b)

Figure 8.1: Results showing (a) Simulated line-to-line output voltage and (b) Experimental line-to-line output voltage with $m_I = 0.9$ and $T_{ulst}/T_{sw} = 0.0$.

The load currents are shown in figure 8.2 for both the simulation and experimental conditions. It is noted that both plots are sinusoidal and balanced with the experimental plots matching closely the simulation waveforms.

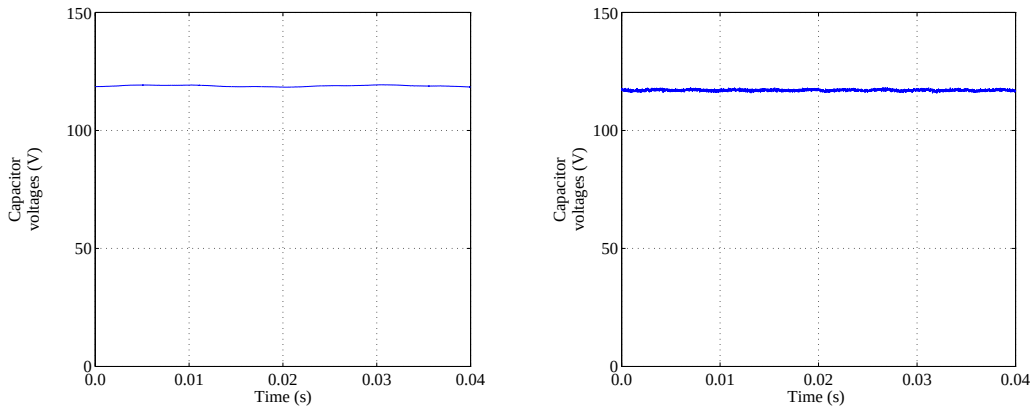



(a) (b)

Figure 8.2: Results showing (a) Simulated load currents and (b) Experimental load currents with $m_I = 0.9$ and $T_{ulst}/T_{sw} = 0.0$.

Figure 8.3 shows the waveforms for the Z-source capacitor voltages. These voltages ($V_{C_1}$, $V_{C_2} = V_C$) are also maintained at 118.6V in simulations since no boosting is commanded (figure 8.3(a)). Figure 8.3(b) shows the corresponding experimental plot

which is similar to the simulation plot.

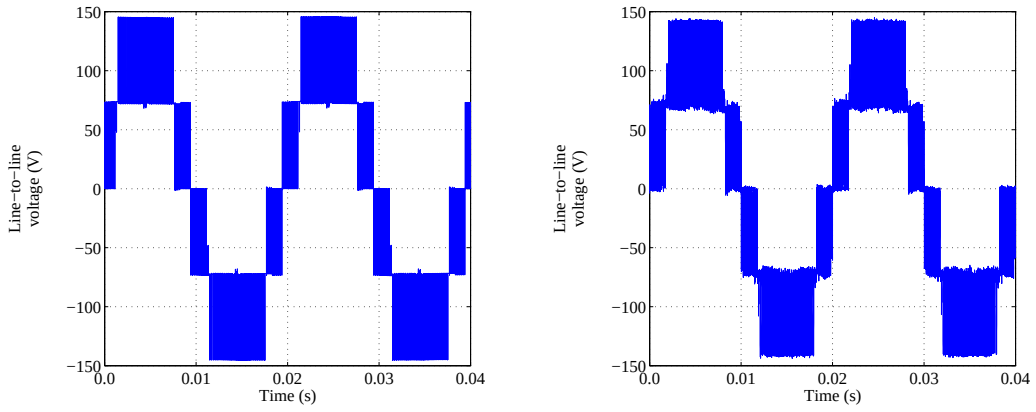



(a) (b)

Figure 8.3: Results showing (a) Simulated Z-source capacitor voltages and (b) Experimental Z-source capacitor voltages with $m_I = 0.9$ and $T_{ulst}/T_{sw} = 0.0$.

#### 8.3.1.2 Boost mode of operation

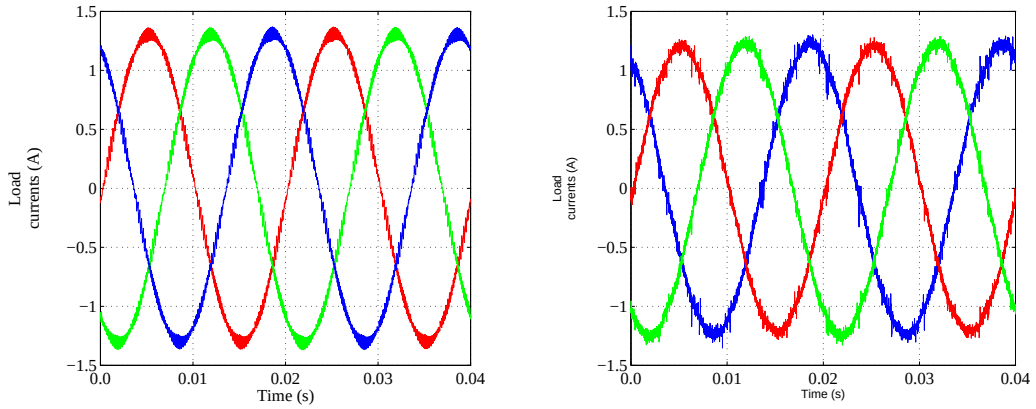
Next, boosting was commanded by maintaining the modulation index at $m_I$=0.9 and incrementing the shoot-through ratio to $T_{ulst}/T_{sw}$=0.1732.




(a) (b)

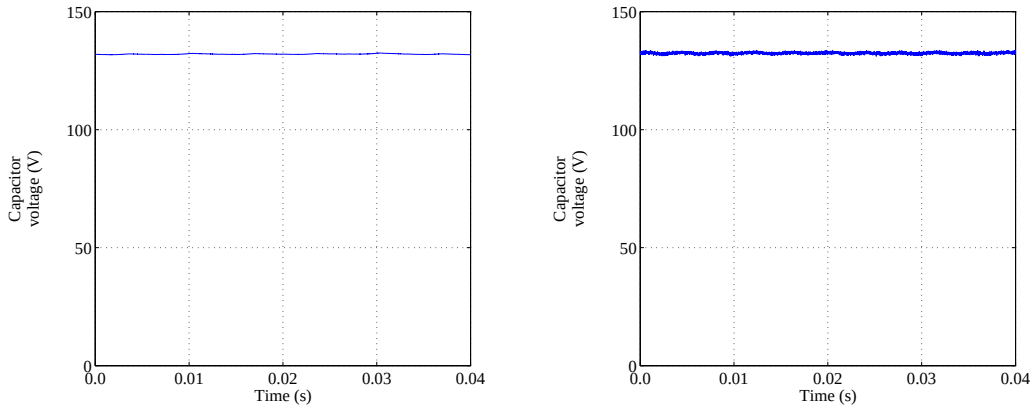
Figure 8.4: Results showing (a) Simulated line-to-line output voltage and (b) Experimental line-to-line output voltage with $m_I = 0.9$ and $T_{ulst}/T_{sw} = 0.1732$.

This is expected to give a boost factor, B'=1.21. Hence, the expected maximum level of the output line-to-line voltage is 118.6×1.21 (= 143.4V). Figure 8.4 shows the corresponding boosted output line-to-line voltage waveforms for the simulation and experimental conditions. It is noted in figure 8.4(a) that the simulation waveform attains a maximum level of 143V. This is clearly matched by the experimental waveform in figure 8.4(b).




(a) (b)

Figure 8.5: Results showing (a) Simulated load currents and (b) Experimental load currents with $m_I = 0.9$ and $T_{ulst}/T_{sw} = 0.1732$.




(a) (b)

Figure 8.6: Results showing (a) Simulated Z-source capacitor voltages and (b) Experimental Z-source capacitor voltages with $m_I = 0.9$ and $T_{ulst}/T_{sw} = 0.1732$.

The corresponding boosted load current waveforms are shown in figure 8.5. It is ob-

served that the load currents remain sinusoidal and balanced even when boosting is commanded by inserting shoot-through states in the output phase legs. Moreover, it is noted that the experimental results match the simulation results very closely. The waveforms of the boosted Z-source capacitor voltages are shown in figure 8.6. It is clear that these voltages have been boosted to the required value of 132V in simulations (figure8.6(a)). The corresponding experimental plot, shown in figure 8.6(b), is very close to the simulation waveform.

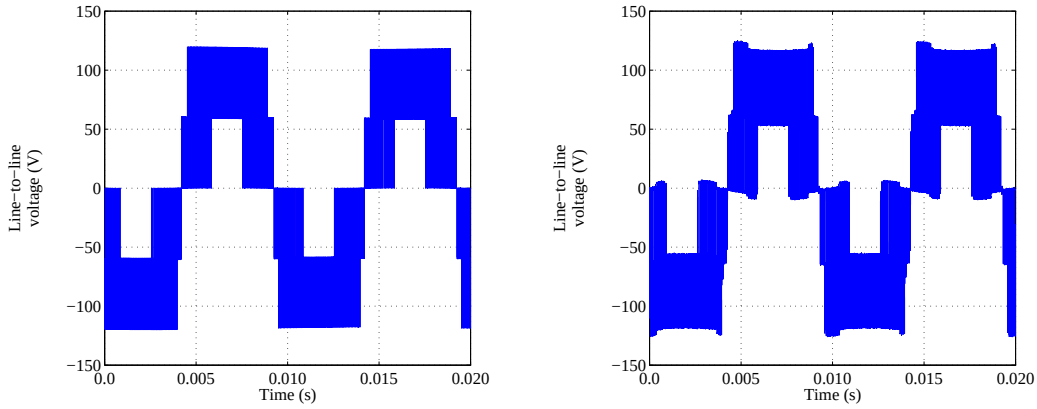
The above results have demonstrated the ability of the Z-source NPC inverter to generate multilevel output voltages and perform voltage buck-boost operation with the NTV SVM technique. The presented results match the theoretical findings presented in section 3.4 and clearly validate the modelling strategy presented earlier.

### 8.3.2 Control with NTVV SVM technique

In order to validate the modelling strategy presented in section 3.5 and to demonstrate the viability of the NTVV SVM algorithm, a simulation has been run with the same conditions as the experimental work and the results compared with the experimental results. These results are compared for both the buck and boost modes of operation.

#### 8.3.2.1 Buck mode of operation

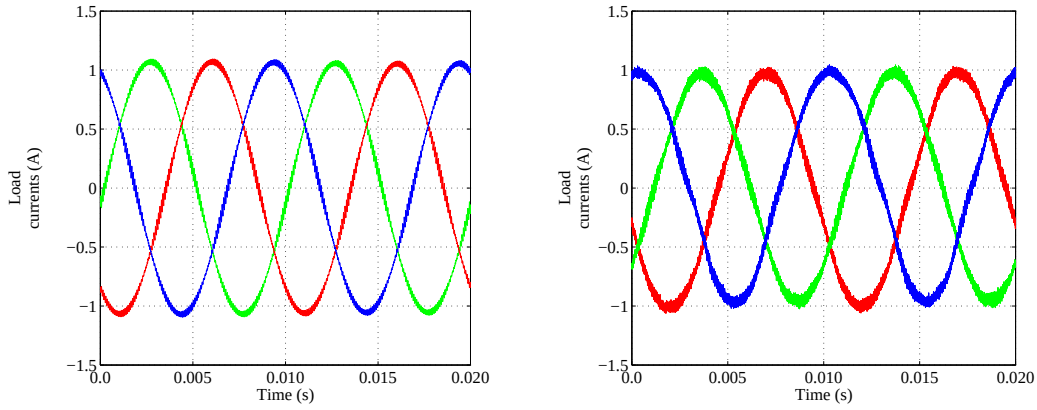
The Z-source NPC inverter was operated in the buck mode by using a modulation index, $m_I$=0.9, and a shoot-through ratio, $T_{ulst}/T_{sw}$=0.0, respectively. As already demonstrated for the NTV SVM strategy, the expected maximum level of the output line-to-line voltage achievable with these parameters is limited to 118.6V. Figure 8.7(a) shows the simulation waveform whilst figure 8.7(b) shows the experimental waveform under these conditions. It is clearly seen that the simulation plot shows a maximum level of 118.6V for the output line-to-line voltage. It is also noted that the experimental waveform matches that of the simulation.




(a) (b)

Figure 8.7: Results showing (a) Simulated line-to-line output voltage and (b) Experimental line-to-line output voltage with $m_I = 0.9$ and $T_{ulst}/T_{sw} = 0.0$.

Figure 8.8(a) shows the load current waveforms for the simulation conditions whilst figure 8.8(b) shows that of the experimental conditions. It is obvious that both plots show sinusoidal and balanced currents with the experimental waveforms closely matching the simulation.

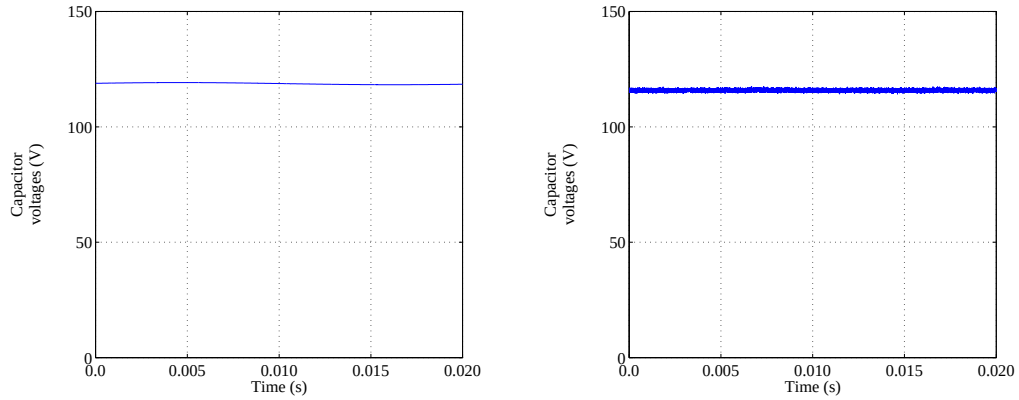



(a) (b)

Figure 8.8: Results showing (a) Simulated load currents and (b) Experimental load currents with $m_I = 0.9$ and $T_{ulst}/T_{sw} = 0.0$.

The waveforms for the Z-source capacitor voltages are shown in figure 8.9. These voltages are also maintained at 118.6V in simulations (figure 8.9(a)). The corresponding

experimental plot which closely matches the simulation plot is shown in figure 8.9(b).

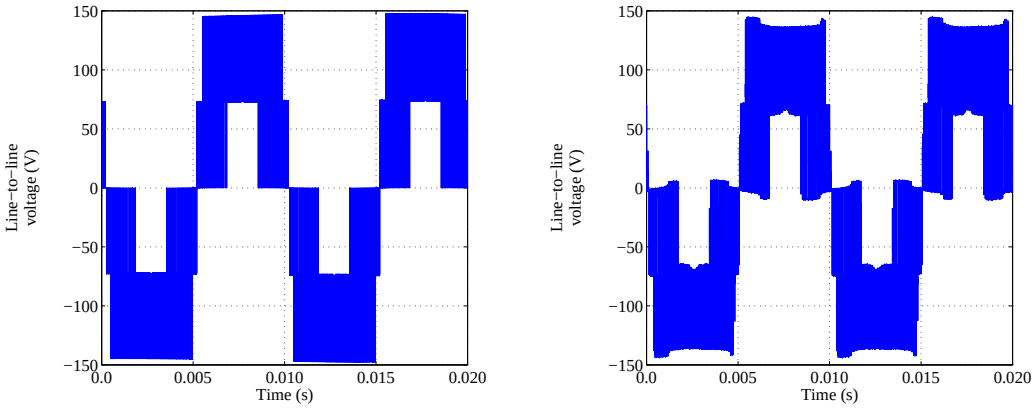



(a) (b)

Figure 8.9: Results showing (a) Simulated Z-source capacitor voltages and (b) Experimental Z-source capacitor voltages with $m_I = 0.9$ and $T_{ulst}/T_{sw} = 0.0$.

#### 8.3.2.2 Boost mode of operation

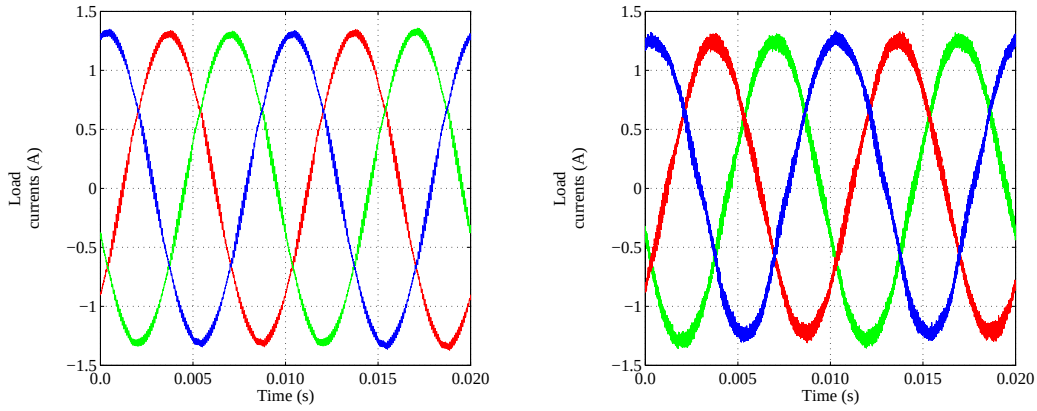
The boosting ability of the Z-source NPC inverter is demonstrated by maintaining the modulation index at $m_I = 0.9$ and incrementing the shoot-through ratio to $T_{ulst}/T_{sw} = 0.1732$.




(a) (b)

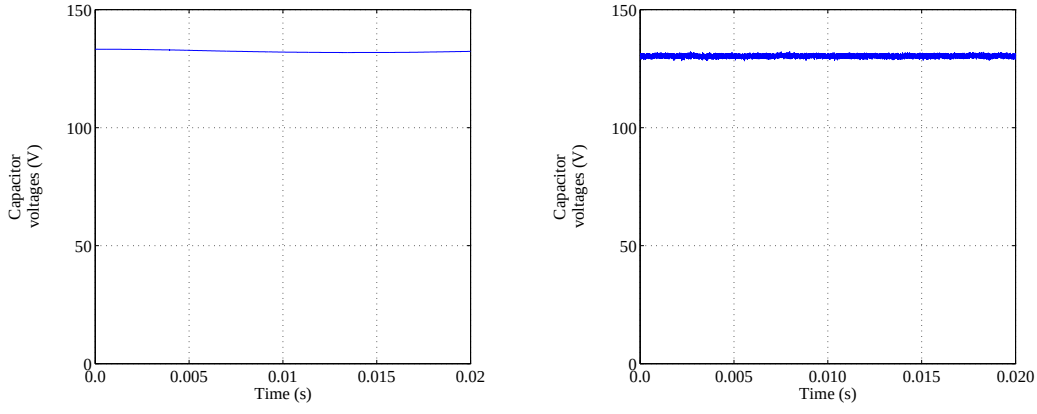
Figure 8.10: Results showing (a) Simulated line-to-line output voltage and (b) Experimental line-to-line output voltage with $m_I = 0.9$ and $T_{ulst}/T_{sw} = 0.1732$.

This yields a boost factor of B'=1.21 hence the expected maximum level of the output line-to-line voltage is 143V. The boosted output line-to-line voltage for both the simulation and experimental conditions are shown in figure 8.10. In figure 8.10(a) it is noted that the maximum level of the output line-to-line waveform attains a value of 143V in simulations as expected. The corresponding experimental waveform is shown in figure 8.10(b) which clearly matches the simulation waveform.




(a) (b)

Figure 8.11: Results showing (a) Simulated load currents and (b) Experimental load currents with $m_I = 0.9$ and $T_{ulst}/T_{sw} = 0.1732$.




(a) (b)

Figure 8.12: Results showing (a) Simulated Z-source capacitor voltages and (b) Experimental Z-source capacitor voltages with $m_I = 0.9$ and $T_{ulst}/T_{sw} = 0.1732$.

The boosted load currents are also shown in figure 8.11. It is noted that the currents

remain sinusoidal and balanced in the boost mode with the experimental waveforms matching the simulation waveforms closely. The boosted Z-source capacitor voltages are shown in figure 8.12 for both the simulation and experimental conditions. From the simulation waveform (figure 8.12(a)) it is noted that the capacitor voltages have been boosted to the required value of 132V. It is also noted that the experimental result resembles that of the simulation as shown in figure 8.12(b).

The ability of the Z-source NPC inverter to generate multilevel output voltages and perform voltage buck-boost operation with the NTVV SVM technique have been demonstrated with the results presented. These results clearly match the theoretical findings presented in section 3.5 and therefore validate the modelling strategy presented earlier.

In the next section, the dc-source is replaced with a *3 x 2* matrix converter. The resulting topology is the three-level, Z-source hybrid direct ac-ac power converter. Topology-wise, this converter is not very different from the Z-source NPC inverter, the obvious difference being the replacement of the dc-source with an active rectifier. The three-level, Z-source hybrid direct power converter has the additional task of producing sinusoidal input currents in addition to output voltage buck-boost capability. The results obtained from this converter are now presented.

## 8.4 3ZHDPC results

The prototype three-level, Z-source hybrid direct power converter has also been tested in the laboratory in order to validate the ability of the converter to generate multilevel output voltages, perform voltage buck-boost operation as well as maintain a set of balanced, sinusoidal input and output currents. The experimental parameters for all results are as follows:

- Input phase voltage: $V_{in}$ = 100V (peak), $f_i$ = 50Hz

- Input filter: $L_f$ = 0.08-mH, $C_f$ = 202-$\mu$F, $R_d$ = 56-$\Omega$
- Load: $R_{load}$ = 57.6-$\Omega$, $L_{load}$ = 10-mH
- Output frequency: $f_{out}$ = 100Hz
- Switching frequency $f_{sw}$ = 10kHz

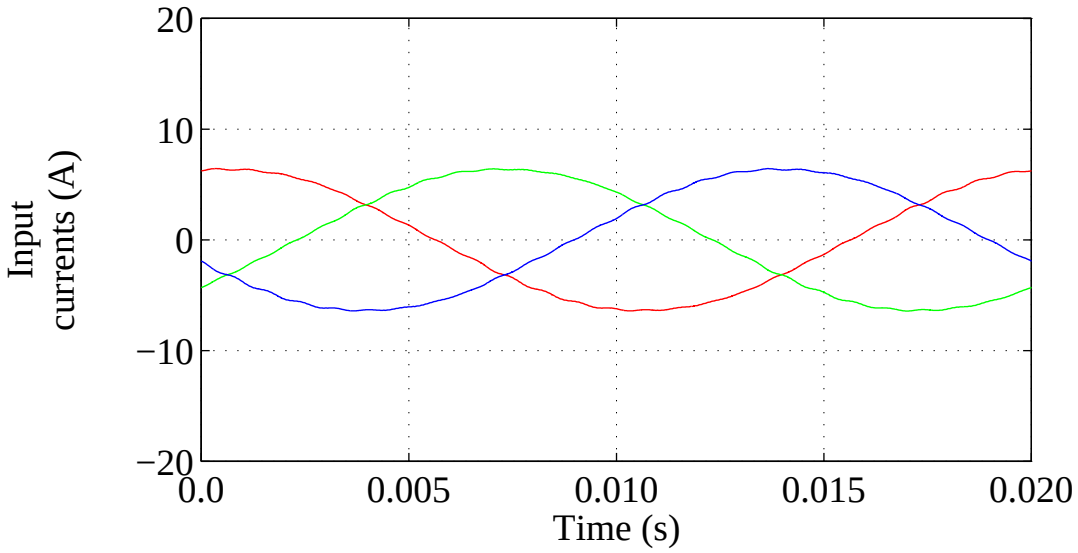
As discussed in section 6.7, a large input filter capacitor is required to filter out the high frequency input current components and also provide a low impedance path for the input currents during the boost mode when shoot-through states are applied and the rectifier is decoupled from the Z-source network. Here too, the experimental validation is divided into two parts namely buck and boost modes, respectively.

### 8.4.1 Buck mode

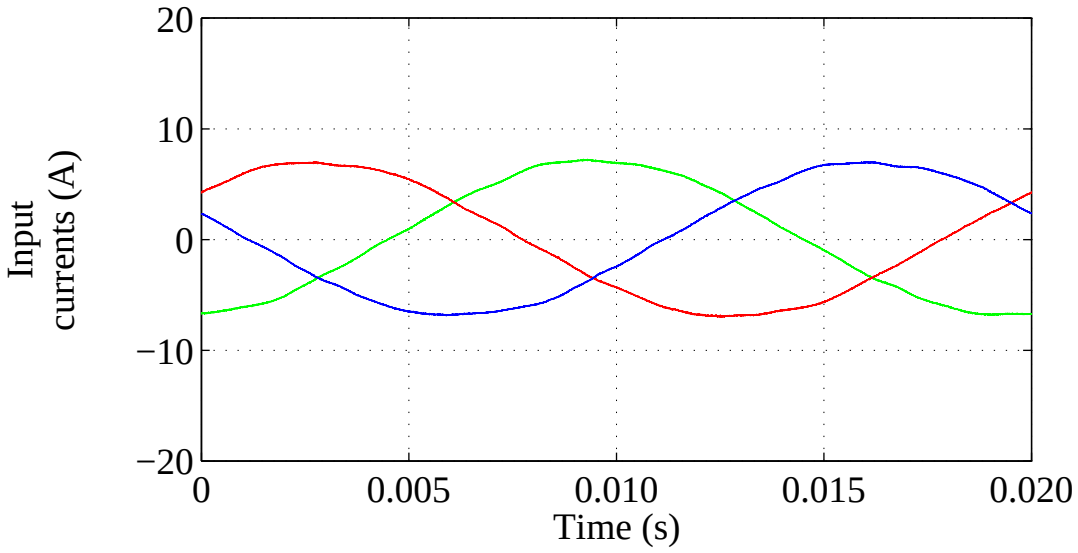
For the buck mode the modulation indices of the rectification and inversion stages were set to $m_R$=1.0 and $m_I$=0.9, respectively, while the shoot-through ratio was set to $T_{ulst}/T_{sw}$=0.0.

A simulation has been run with the same conditions as the experimental work in an effort to validate the modelling strategy used in Chapter 6 and to demonstrate the viability of the proposed SVM-based algorithm. The input current waveforms for this simulation is compared with the experimental results in figure 8.13. It can be observed that the two plots are very similar. Both current waveforms are obviously sinusoidal and balanced.

The simulated and experimental waveforms of the variable dc-link voltage produced by the *3 x 2* matrix converter are shown in figure 8.14. The similarity between these waveforms is clearly obvious. A comparison can also be made with the split dc-link voltages as shown in figure 8.15. It should be clear that the waveforms are indeed similar.




(a)




(b)

Figure 8.13: Results showing (a) Simulated input currents and (b) Experimental input currents

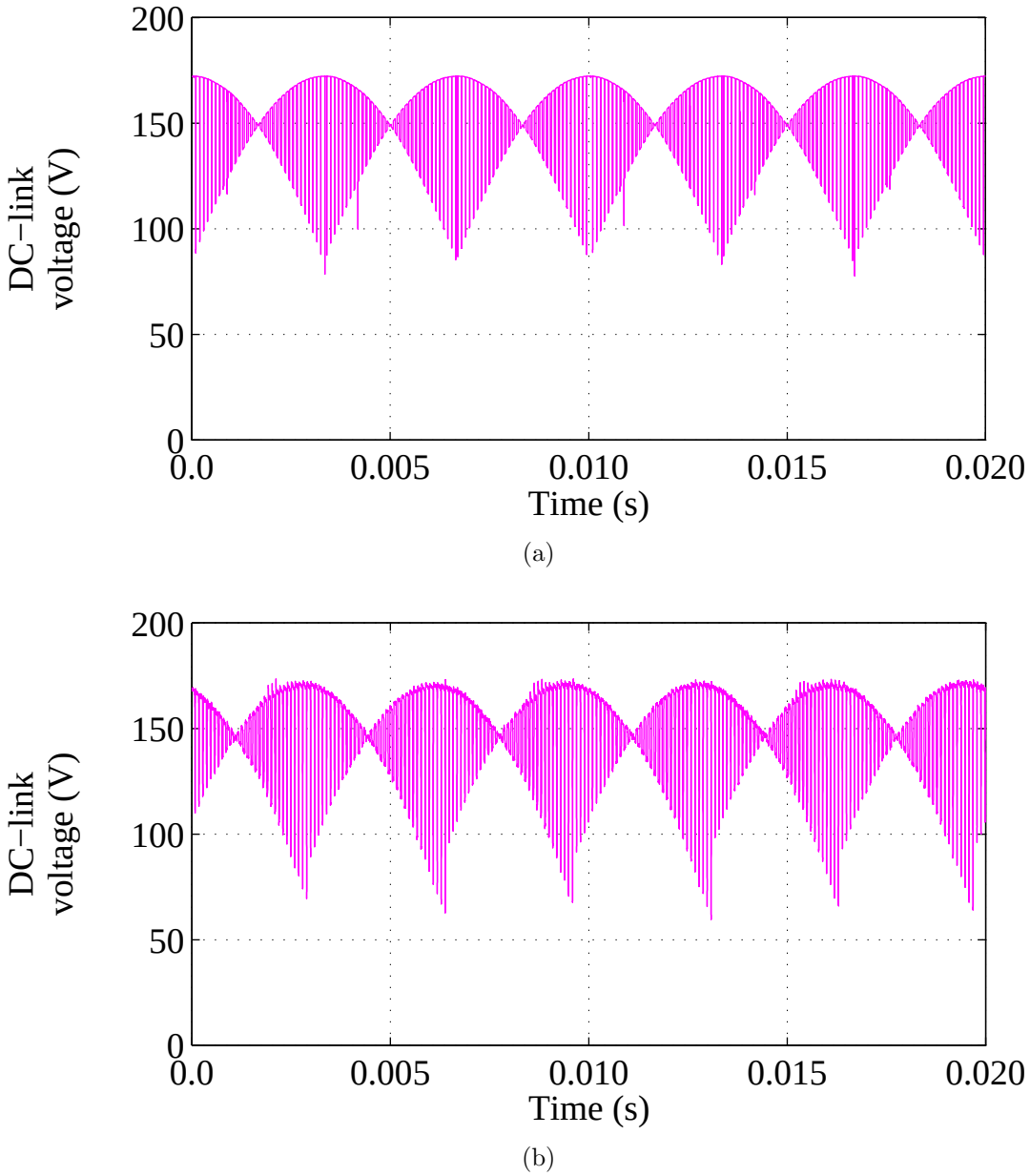
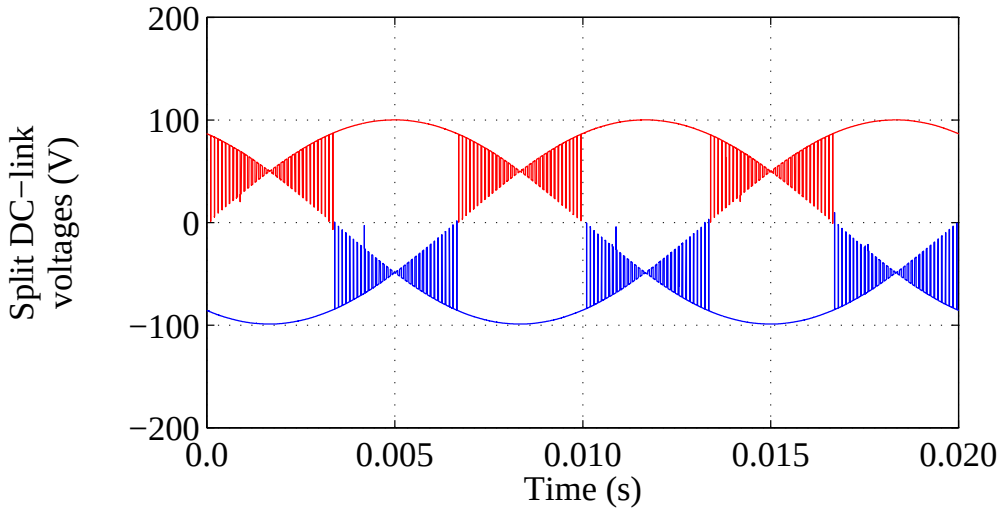
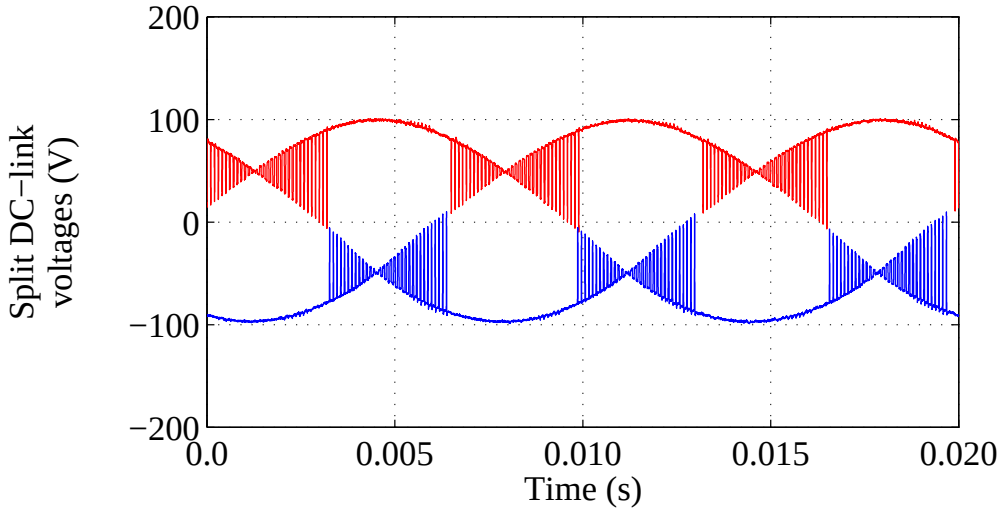



Figure 8.14: Results showing (a) Simulated full dc-link voltage and (b) Experimental full dc-link voltage



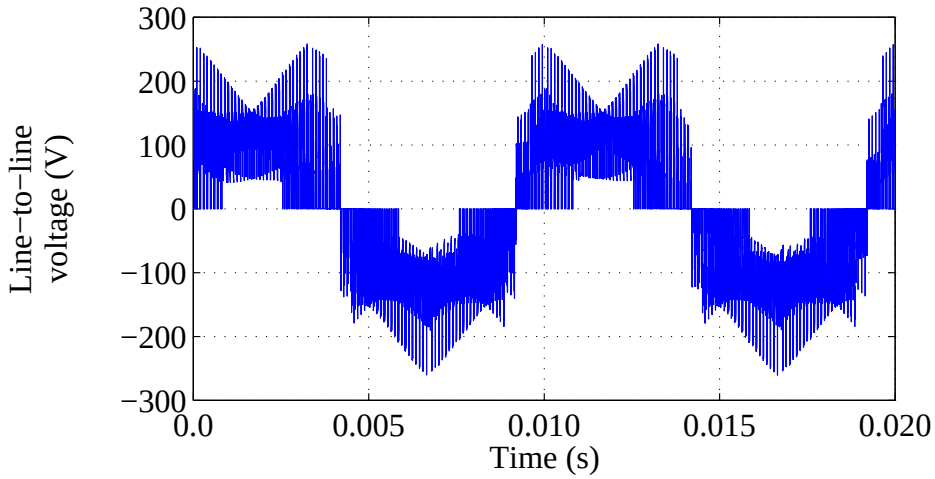

(a)



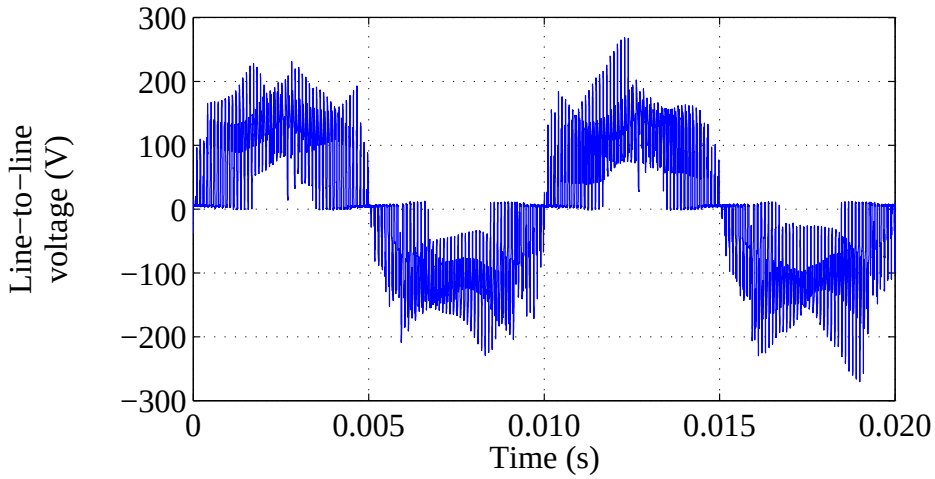

(b)

Figure 8.15: Results showing (a) Simulated split dc-link voltage and (b) Experimental split dc-link voltage

The output waveforms generated by the prototype converter under the above conditions are also compared with the simulation results as shown in figures 8.16 and 8.17, respectively. In figure 8.16 it is noted that the output line-to-line voltage attains five levels and the two plots are very similar. The output currents are also observed to be sinusoidal and balanced in both plots of figure 8.17.

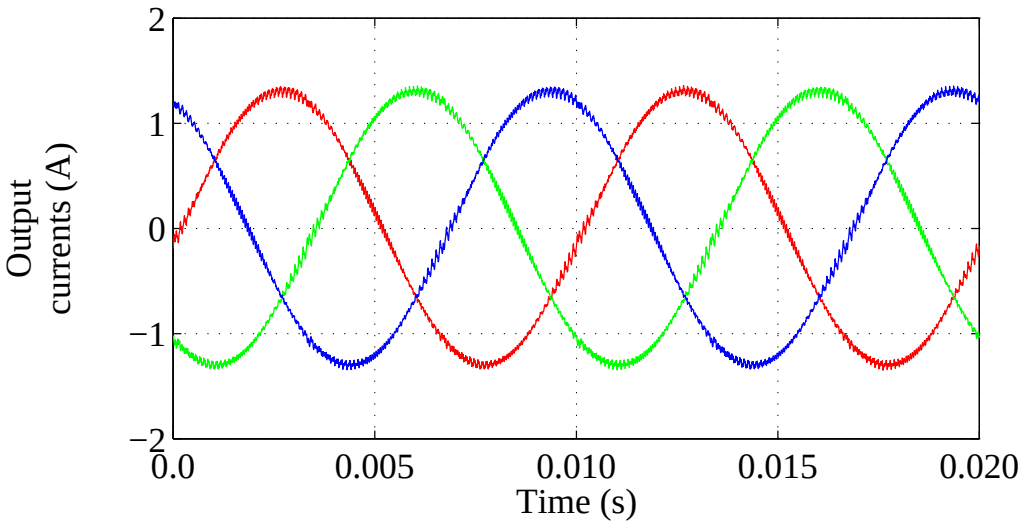



(a)

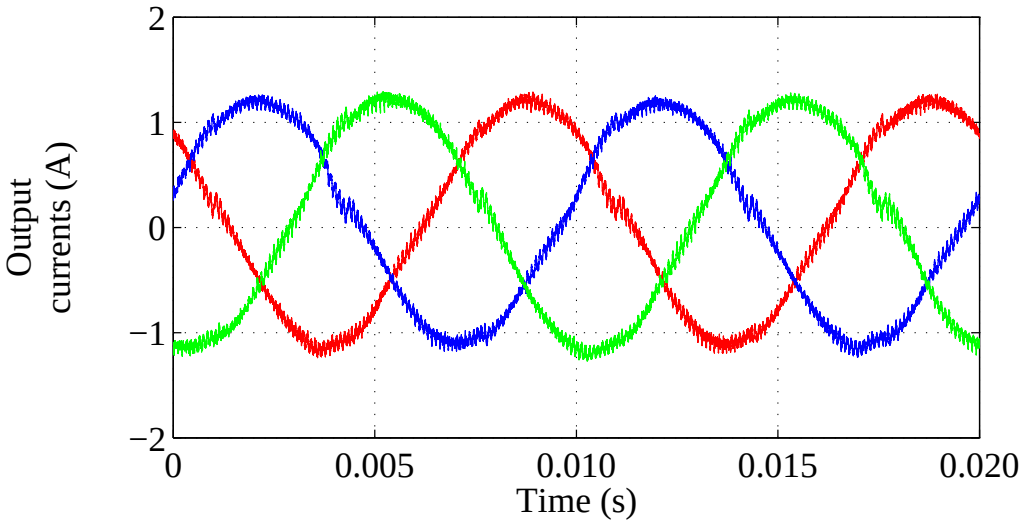



(b)

Figure 8.16: Results showing (a) Simulated output line-to-line voltage and (b) Experimental output line-to-line voltage when $m_R = 1.0$, $m_I = 0.9$ and $T_{ulst}/T_{sw} = 0.0$.




(a)

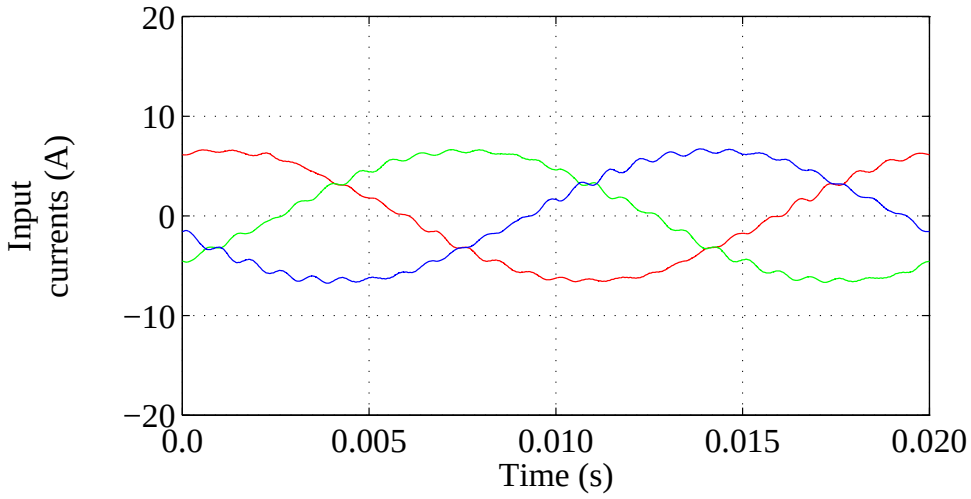



(b)

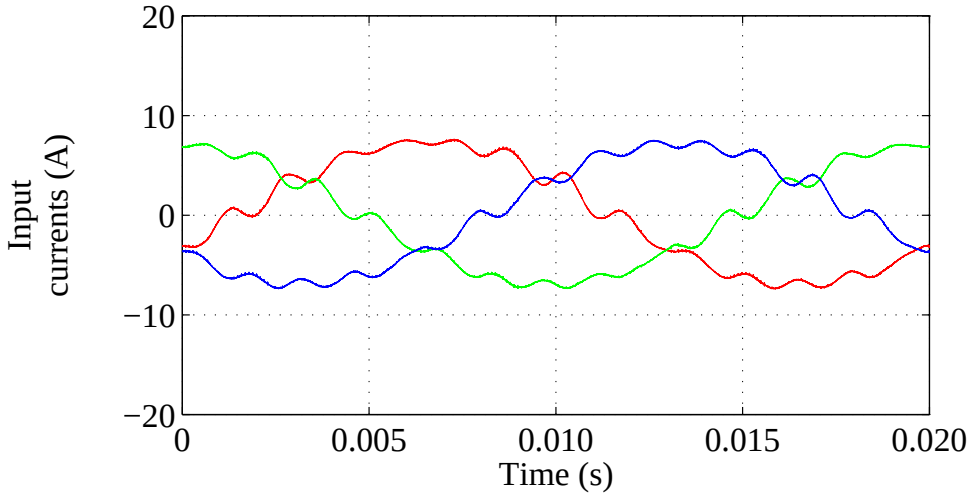
Figure 8.17: Results showing (a) Simulated output currents and (b) Experimental output currents when $m_R = 1.0$, $m_I = 0.9$ and $T_{ulst}/T_{sw} = 0.0$.

### 8.4.2 Boost mode

To command boost mode, the modulation indices of the rectification and inversion stages were maintained at $m_R = 1.0$ and $m_I = 0.9$, respectively, but the shoot-through ratio was incremented to $T_{ulst}/T_{sw} = 0.1732$. For this condition too, a simulation has been run with the same conditions as the experimental work and the two results compared.



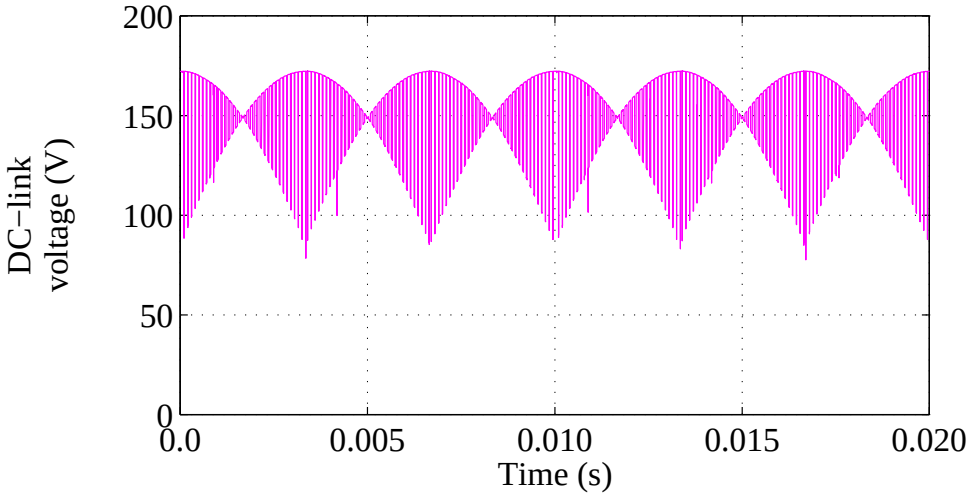

(a)



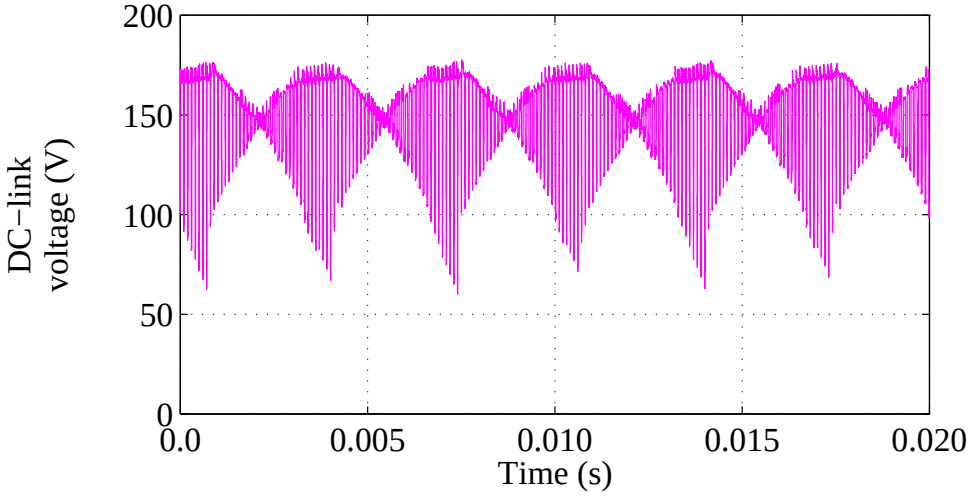

(b)

Figure 8.18: Results showing (a) Simulated input currents and (b) Experimental input currents

First, the input current waveforms are compared in figure 8.18 where it is noted that the two plots are very similar. It is also obvious that both current waveforms are still balanced and sinusoidal even with the insertion of shoot-through states in the inversion stage of the converter.




(a)

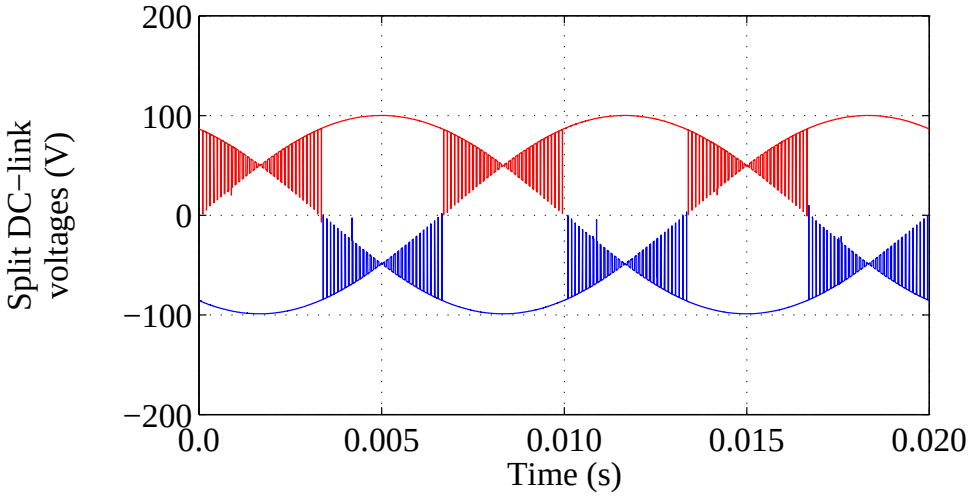



(b)

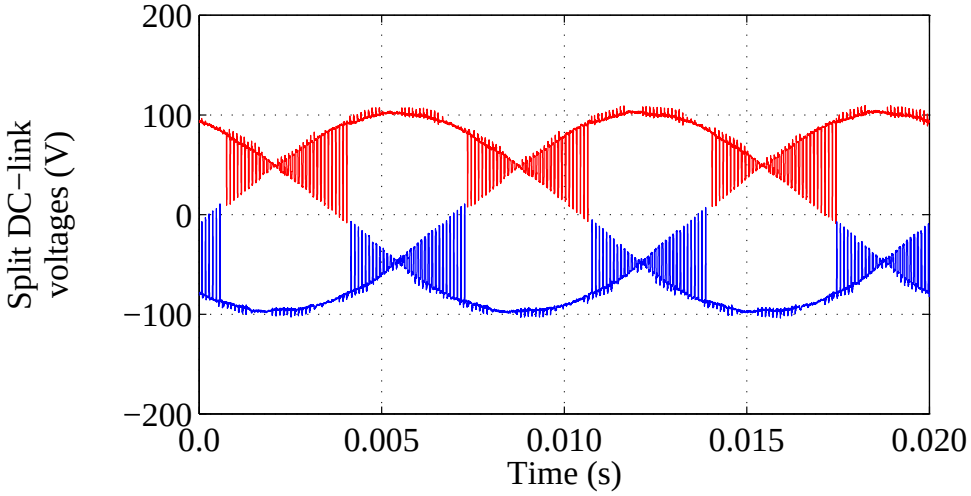
Figure 8.19: Results showing (a) Simulated full dc-link voltage and (b) Experimental full dc-link voltage

The higher distortion is as a result of the disconnection/reconnection of the rectifier from/to the Z-source network during the introduction and removal of shoot-through

states. As already discussed in section 6.7, this ripple can be completely eliminated by using very large input filter capacitors. However, there is a limit to the size of capacitors that can be used for input filters. Therefore, a compromise has to be made between capacitor size and acceptable ripple levels.




(a)



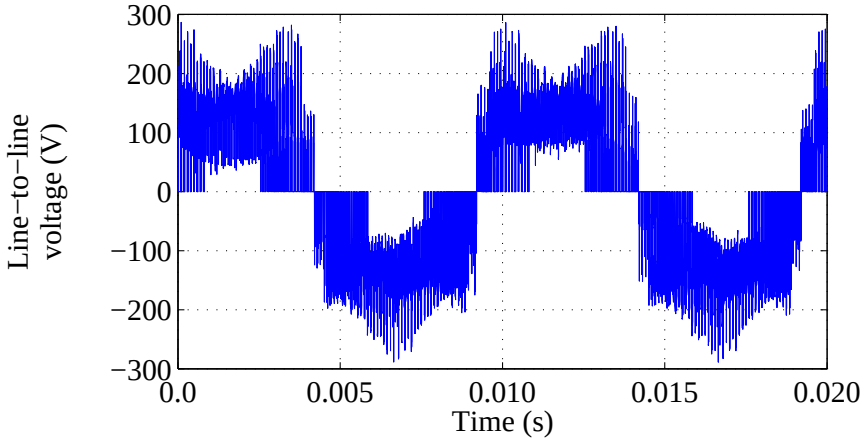

(b)

Figure 8.20: Results showing (a) Simulated split dc-link voltage and (b) Experimental split dc-link voltage

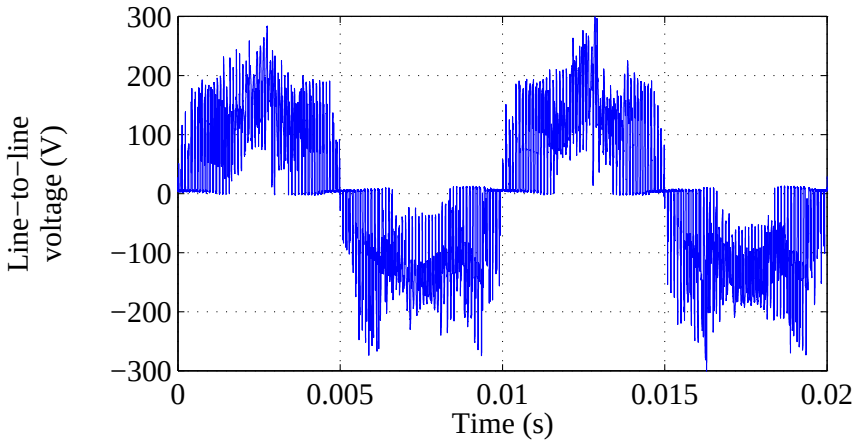
Figure 8.19 shows the simulated and experimental waveforms of the variable dc-link voltage produced by the *3 x 2* matrix converter. It is noted that the plots are similar

to those of the buck mode. Thus, the dc-link voltage is not affected by the shoot-through states of the inversion stage because the input filter capacitors are able to maintain a fairly constant voltage during the boost mode with shoot-through states.

Similarly, the split dc-link voltages applied to the back-end Z-source NPC inverter are shown in figure 8.20 for the simulated and experimental conditions. Here too, it is clear that the simulation and experimental results are similar and not affected by the insertion of shoot-through states.



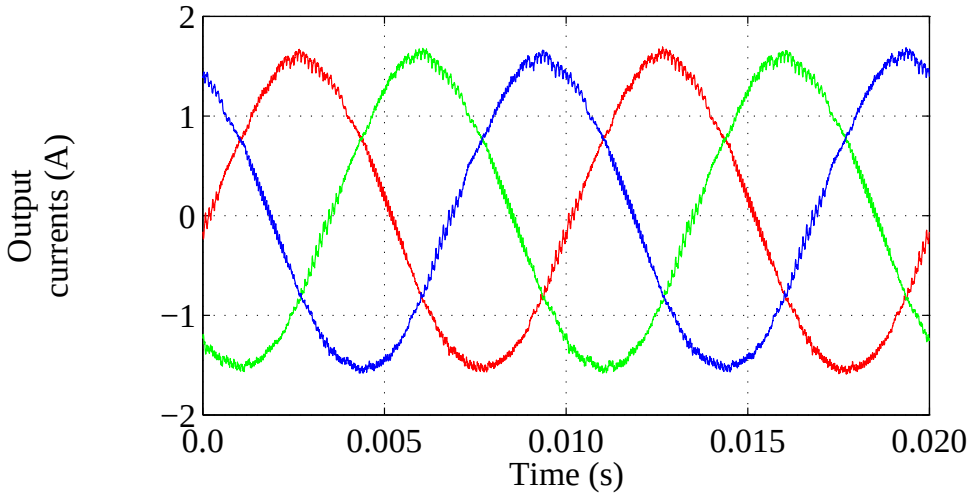

(a)



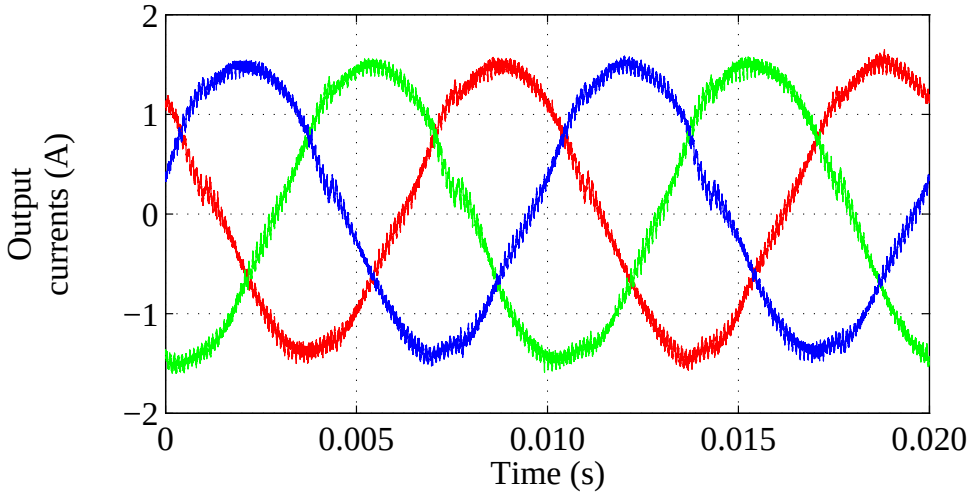

(b)

Figure 8.21: Results showing (a) Simulated output line-to-line voltage and (b) Experimental output line-to-line voltage when $m_R = 1.0$, $m_I = 0.9$ and $T_{ulst}/T_{sw} = 0.1732$

The boosted output waveforms generated by the prototype converter under these conditions are also compared with the simulation plots as shown in figures 8.21 and 8.22, respectively. In figure 8.21, it is noted that the output line-to-line voltage plots are similar and have both been boosted to a value higher than the buck mode case. The output currents are also observed to be similar and boosted as well. The currents still remain balanced and sinusoidal after shoot-through states have been inserted as shown in figure 8.22.




(a)




(b)

Figure 8.22: Results showing (a) Simulated output currents and (b) Experimental output currents when $m_R = 1$, $m_I = 0.9$ and $T_{ulst}/T_{sw} = 0.1732$

## 8.5 Conclusions

This chapter has presented the results taken from the experimental converters. The results taken from the two prototype converters clearly correspond well to the simulation results. This outcome validates the abilities of the converters to perform voltage buck-boost operation in generating multilevel output voltages. In addition to the above, the 3ZHDPC is able to produce sinusoidal, balanced input currents. It has been found that the input filter of this converter has to be designed to offer a low impedance path for the input currents during the voltage-boost mode when the rectifier is decoupled from the Z-source network in addition to filtering out the high frequency input current components. This translates into smaller filter inductance and bigger filter capacitance.

# Chapter 9

# Conclusions

Due to the recent advancements in the field of power conversion, the need has arisen to design converters which can operate successfully with variable voltage sources such as fuel cells and photovoltaic arrays. The conventional VSI, which is the most commonly used type of converter, suffers from the drawback that it cannot boost the voltage of the input source. Thus, a separate voltage-boosting dc-dc converter is needed to interface the variable-voltage source with the conventional VSI. This cascaded arrangement of two power converters increases not only the complexity of the circuit and control but also the cost and space requirement.

In order to satisfy the pressing needs for a single converter capable of voltage buck-boost, many new converter topologies have been proposed in the recent past. Among these new topologies, the Z-source converter has attracted wide attention over the others mainly because it continues to employ a conventional VSI as the power converter with a modified dc-link stage. The Z-source concept can be applied to the entire spectrum of power conversion: dc-to-ac, ac-to-dc, ac-to-ac and dc-to-dc. This thesis has presented two topologies: Z-source NPC inverter and three-level, Z-source hybrid direct ac-ac power converter. These converters are able to perform voltage buck-boost function by introducing shoot-through states into the null states of the conventional NPC converter's PWM switching pattern.

A literature review of the conventional NPC inverter and its modulation methods have been given in Chapter 2. Two SVM techniques for controlling the traditional NPC inverter have been described in detail. These methods are the nearest three vectors (NTV) and nearest three virtual vectors (NTVV) SVM techniques. It has been noted that the NTVV technique is able to eliminate the inherent problem of neutral-point voltage deviation of the NPC inverter completely by using vectors that ensure that the average neutral-point current over each sampling period is zero.

These SVM techniques for controlling the traditional NPC inverter were then modified to include upper and lower shoot-through states in the PWM switching pattern to control the Z-source NPC inverter in Chapter 3. A detailed circuit analysis of the Z-source NPC inverter has been carried out to prove the ability of this converter to overcome the buck-only constraint of the traditional NPC inverter. Simulation results have been used to verify the theoretical findings.

In order to extend the Z-source concept to ac-ac power conversion, matrix converter theories have been thoroughly investigated. This study is presented in Chapter 4 where the derivation of the two-stage matrix converter topology from the conventional matrix converter has been explained in detail. The two-stage matrix converter provides additional benefits in comparison to the conventional matrix converter such as reduced number of switches, possibility for cost effective multi-drive systems and it can be a platform for more complex converter structures. The SVM technique for controlling the two-stage matrix converter has been presented and simulation results have been used to demonstrate the operation of this converter.

In Chapter 5, the multilevel concept has been integrated into the two-stage matrix converter topology to generate multilevel output voltages. Simulation results have been presented to show the ability of the three-level, two-stage matrix converter to generate multilevel output waveforms. The scope of applications for this converter has not grown significantly because of its limited voltage transfer ratio of 86.6%. To address this issue, a Z-source network is inserted in the virtual dc-link of this converter to add boost functionality. The resulting topology is the three-level, Z-source

hybrid direct ac-ac power converter. The topological derivation of this converter is straightforward and its operating modes are not different from the Z-source NPC inverter presented earlier. However, the modulation of this converter to simultaneously produce voltage buck-boost flexibility and generate sinusoidal input and output waveforms is very challenging.

A novel modified SVM technique for controlling the three-level, Z-source hybrid direct ac-ac power converter has been presented in Chapter 6. The ability of this converter to perform voltage buck-boost operation and generate sinusoidal input and output waveforms have been demonstrated with simulation results. It has been discovered that the input filter of this converter will have to provide a low impedance path for the input currents during the voltage-boost mode when shoot-through states are inserted into the output phase legs and the rectifier is decoupled from the Z-source network. This translates into smaller filter inductance and bigger filter capacitance.

An experimental converter rated at 7.5kW was used to verify the novel modified SVM techniques presented in this work. The converter was controlled using a combination of DSP and FPGA systems. First, the converter was operated as an inverter to validate the simulation results of the Z-source NPC inverter. The experimental results captured from this converter matched those taken from simulation closely. The converter was then operated as a direct ac-ac converter to capture results for the three-level, Z-source hybrid direct ac-ac power converter. Experimental results captured from this converter also matched those taken from simulation closely.

## 9.1 Summary of achievements

The work presented in this thesis has been an exciting opportunity to give a small contribution to research on the Z-source conversion concept. As mentioned in Chapter 1, this research aims were:

i. investigate the Z-source concept to add boost capability to an NPC inverter;

ii. investigate the Z-source concept to improve the intrinsic maximum voltage transfer ratio limit of the three-level, two-stage matrix converter;

iii. achieve space vector modulation of these hybrid converters;

iv. validate the proposed modulation methods using a low power experimental prototype.

The following points summarise the achievements presented in this thesis.

- A literature review and methods of modulation for an NPC inverter and matrix converter topologies have been made.
- A novel NTV SVM method of modulation for Z-source NPC inverter has been made in detail. A comprehensive circuit analysis of the Z-source NPC inverter has been presented.
- A novel NTVV SVM method of modulation for Z-source NPC inverter has also been made in detail. This method ensures that the Z-source concept for three-level inverter circuits can effectively be extended to direct ac-to-ac power conversion.
- A novel three-level Z-source hybrid direct ac-ac power converter with voltage buck-boost capability has been presented. A comprehensive circuit analysis of this converter has also been presented.
- A novel SVM method of modulation for the three-level, Z-source hybrid direct ac-ac power converter has been given.
- A novel selection of input filter components to reduce input current ripples of the three-level, Z-source hybrid direct ac-ac power converter to within acceptable limits has been made.

The experience gained from this project made it possible to complete the analysis of two Z-source converter topologies in spite of the time constraints. The analysis

and SABER® simulation were a challenge in terms of implementing the space vector modulation to give the best performance of the three-level, Z-source hybrid direct ac-ac power converter. The work done also included the experimental design to provide experimental data from a real converter to validate the analysis. The goals set at the outset have been achieved but more could possibly be done to realise the inherent merit of using the Z-source conversion concept at high voltage levels and a few ideas are suggested in the future work.

## 9.2 Further work

In order to enable this work to progress the following advances could be made:

- A derivation of the small signal model for the Z-source NPC inverter when operated with the upper-lower-shoot-through mode to implement closed-loop control of the converter.
- Implementation of the Z-source NPC inverter as a motor drive.
- A derivation of the small signal model for the three-level, Z-source hybrid direct ac-ac power converter operated with the upper-lower-shoot-through mode.
- Optimization of the input filter design for the three-level, Z-source hybrid direct power converter.
- An implementation of the three-level, Z-source hybrid direct power converter as a motor drive.

## 9.3 Publications resulting from the work

The work carried out over the course of this project has resulted in the publication of one journal and two conference papers. These papers are listed in appendix C.

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# Appendix A

# NTVV modulation sequences

## A.1 Chapters 2 and 5

| Triangle | Sector | t1 | | | t2 | | | t3 | | | t4 | | | t5 | | | t6 | | | t7 | | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | | a | b | c | a | b | c | a | b | c | a | b | c | a | b | c | a | b | c | a | b | c |
| 1 | 1 | P | P | P | P | P | O | P | O | O | O | O | O | O | O | N | O | N | N | N | N | N |
| | 2 | P | P | P | P | P | O | O | P | O | O | O | O | O | O | N | N | O | N | N | N | N |
| | 3 | P | P | P | O | P | P | O | P | O | O | O | O | N | O | O | N | O | N | N | N | N |
| | 4 | P | P | P | O | P | P | O | O | P | O | O | O | N | O | O | N | N | O | N | N | N |
| | 5 | P | P | P | P | O | P | O | O | P | O | O | O | O | N | O | N | N | O | N | N | N |
| | 6 | P | P | P | P | O | P | P | O | O | O | O | O | O | N | O | O | N | N | N | N | N |
| 2 | 1 | P | P | O | P | O | O | P | O | N | O | O | N | O | N | N | | | | | | |
| | 2 | P | P | O | O | P | O | O | P | N | O | O | N | N | O | N | | | | | | |
| | 3 | O | P | P | O | P | O | N | P | O | N | O | O | N | O | N | | | | | | |
| | 4 | O | P | P | O | O | P | N | O | P | N | O | O | N | N | O | | | | | | |
| | 5 | P | O | P | O | O | P | O | N | P | O | N | O | N | N | O | | | | | | |
| | 6 | P | O | P | P | O | O | P | N | O | O | N | O | O | N | N | | | | | | |
| 3 | 1 | P | P | O | P | O | O | P | O | N | P | N | N | O | N | N | | | | | | |
| | 2 | P | P | O | P | P | N | O | P | N | O | O | N | N | O | N | | | | | | |
| | 3 | O | P | P | O | P | O | N | P | O | N | P | N | N | O | N | | | | | | |
| | 4 | O | P | P | N | P | P | N | O | P | N | O | O | N | N | O | | | | | | |
| | 5 | P | O | P | O | O | P | O | N | P | N | N | P | N | N | O | | | | | | |
| | 6 | P | O | P | P | N | P | P | N | O | O | N | O | O | N | N | | | | | | |
| 4 | 1 | P | P | O | P | P | N | P | O | N | P | N | N | O | N | N | | | | | | |
| | 2 | P | P | O | P | P | N | O | P | N | N | P | N | N | O | N | | | | | | |
| | 3 | O | P | P | N | P | P | N | P | O | N | P | N | N | O | N | | | | | | |
| | 4 | O | P | P | N | P | P | N | O | P | N | N | P | N | N | O | | | | | | |
| | 5 | P | O | P | P | N | P | O | N | P | N | N | P | N | N | O | | | | | | |
| | 6 | P | O | P | P | N | P | O | N | P | N | N | P | N | N | O | | | | | | |
| 5 | 1 | P | P | O | P | P | N | P | O | N | O | O | N | O | N | N | | | | | | |
| | 2 | P | P | O | O | P | O | O | P | N | N | P | N | N | O | N | | | | | | |
| | 3 | O | P | P | N | P | P | N | P | O | N | O | O | N | O | N | | | | | | |
| | 4 | O | P | P | O | O | P | N | O | P | N | N | P | N | N | O | | | | | | |
| | 5 | P | O | P | P | N | P | O | N | P | O | N | O | N | N | O | | | | | | |
| | 6 | P | O | P | P | O | O | P | N | O | P | N | N | O | N | N | | | | | | |

Table A.1: The switching sequence for the NPC inverter modulated using using NTVV PWM

## A.2 Chapters 3 and 6

| Triangle | Sector | t1 | | | t2 | | | t3 | | | t4 | | | t5 | | | t6 | | | t7 | | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | | a | b | c | a | b | c | a | b | c | a | b | c | a | b | c | a | b | c | a | b | c |
| 1 | 1 | P | P | P | P | P | O | P | O | O | O | O | O | O | O | N | O | N | N | N | N | N |
| | 2 | P | P | P | P | P | O | O | P | O | O | O | O | O | O | N | N | O | N | N | N | N |
| | 3 | P | P | P | O | P | P | O | P | O | O | O | O | N | O | O | N | O | N | N | N | N |
| | 4 | P | P | P | O | P | P | O | O | P | O | O | O | N | O | O | N | N | O | N | N | N |
| | 5 | P | P | P | P | O | P | O | O | P | O | O | O | O | N | O | N | N | O | N | N | N |
| | 6 | P | P | P | P | O | P | P | O | O | O | O | O | O | N | O | O | N | N | N | N | N |
| 2 | 1 | P | P | O | P | O | O | P | O | L | P | O | N | U | O | N | O | O | N | O | N | N |
| | 2 | P | P | O | O | P | O | O | P | L | O | P | N | O | U | N | O | O | N | N | O | N |
| | 3 | O | P | P | O | P | O | L | P | O | N | P | O | N | U | O | N | O | O | N | O | N |
| | 4 | O | P | P | O | O | P | L | O | P | N | O | P | N | O | U | N | O | O | N | N | O |
| | 5 | P | O | P | O | O | P | O | L | P | O | N | P | O | N | U | O | N | O | N | N | O |
| | 6 | P | O | P | P | O | O | P | L | O | P | N | O | U | N | O | O | N | O | O | N | N |
| 3 | 1 | P | P | O | P | O | O | P | O | L | P | O | N | P | N | N | U | N | N | O | N | N |
| | 2 | P | P | O | P | P | L | P | P | N | O | P | N | O | U | N | O | O | N | N | O | N |
| | 3 | O | P | P | O | P | O | L | P | O | N | P | O | N | P | N | N | U | N | N | O | N |
| | 4 | O | P | P | L | P | P | N | P | P | N | O | P | N | O | U | N | O | O | N | N | O |
| | 5 | P | O | P | O | O | P | O | L | P | O | N | P | N | N | P | N | N | U | N | N | O |
| | 6 | P | O | P | P | L | P | P | N | P | P | N | O | U | N | O | O | N | O | O | N | N |
| 4 | 1 | P | P | O | P | P | L | P | P | N | P | O | N | P | N | N | U | N | N | O | N | N |
| | 2 | P | P | O | P | P | L | P | P | N | O | P | N | N | P | N | N | U | N | N | O | N |
| | 3 | O | P | P | L | P | P | N | P | P | N | P | O | N | P | N | N | U | N | N | O | N |
| | 4 | O | P | P | L | P | P | N | P | P | N | O | P | N | N | P | N | N | U | N | N | O |
| | 5 | P | O | P | P | L | P | P | N | P | O | N | P | N | N | P | N | N | U | N | N | O |
| | 6 | P | O | P | P | L | P | P | N | P | P | N | O | P | N | N | U | N | N | O | N | N |
| 5 | 1 | P | P | O | P | P | L | P | P | N | P | O | N | U | O | N | O | O | N | O | N | N |
| | 2 | P | P | O | O | P | O | O | P | L | O | P | N | N | P | N | N | U | N | N | O | N |
| | 3 | O | P | P | L | P | P | N | P | P | N | P | O | N | U | O | N | O | O | N | O | N |
| | 4 | O | P | P | O | O | P | L | O | P | N | O | P | N | N | P | N | N | U | N | N | O |
| | 5 | P | O | P | P | L | P | P | N | P | O | N | P | O | N | U | O | N | O | N | N | O |
| | 6 | P | O | P | P | O | O | P | L | O | P | N | O | P | N | N | U | N | N | O | N | N |

Table A.2: The switching sequence for the Z-source NPC inverter modulated using the NTVV modulation strategy.

# Appendix B

# Parameters Used

## B.1 Simulation analysis

### B.1.1 The two-stage matrix converter (Chapter4)

■ Supply:

- input voltages, $V_{in,rms} = 240$V
- input frequency, $f_i = 50$Hz

■ Input filter:

- Inductor, $L_f = 0.7$-mH
- Capacitor, $C_f = 3.3$-$\mu$F
- Damping resistor, $R_d = 56$-$\Omega$

■ Load:

- Resistor, $R_{load} = 57.6$-$\Omega$
- Inductor, $L_{load} = 10$-mH

■ Output:

- At a modulation index, $m_I = 0.9$
- Output frequency, $f_{out} = 125$Hz

■ Switching frequency, $f_{sw} = 10$kHz

### B.1.2 The three-level two-stage matrix converter (Chapter5)

■ Supply:

- input voltages, $V_{in,rms} = 240$V
- input frequency, $f_i = 50$Hz

■ Input filter:

- Inductor, $L_f = 0.7$-mH
- Capacitor, $C_f = 10$-$\mu$F
- Damping resistor, $R_d = 20$-$\Omega$

■ Load:

- Resistor, $R_{load} = 20$-$\Omega$
- Inductor, $L_{load} = 10$-mH

■ Output:

- At a modulation index, $m_I = 0.9$
- At a modulation index, $m_I = 0.5$
- Output frequency, $f_{out} = 100$Hz

■ Switching frequency, $f_{sw} = 12.5$kHz

### B.1.3 The three-level, Z-source hybrid direct power converter (Chapter6)

■ Supply:

- input voltages, $V_{in,peak} = 100$V
- input frequency, $f_i = 50$Hz

■ Input filter:

- Inductor, $L_f = 0.081$-mH
- Capacitor, $C_f = 200$-$\mu$F
- Damping resistor, $R_d = 56$-$\Omega$

■ Z-source network:

- Inductor, $L_{1,2} = 2.1$-mH
- Capacitor, $C_{1,2} = 0.47$-$\mu$F

■ Load:

- Resistor, $R_{load} = 57.6$-$\Omega$
- Inductor, $L_{load} = 10$-mH

■ Output:

- Operating in buck mode, $m_I = 0.9$, $T_{ulst}/T_{sw} = 0$, $V_{out,peak} = 135$V
- Operating in boost mode, $m_I = 0.9$, $T_{ulst}/T_{sw} = 0.1732$, $V_{out,peak} = 163$V
- Output frequency, $f_{out} = 100$Hz

■ Switching frequency, $f_{sw} = 10$kHz

# Appendix C

# Published Papers

The following papers were published with material directly relating to this thesis:

## C.1 Journal paper

i. Effah, F.B.; Wheeler, P.; Clare, J.; Watson, A.,"Space-Vector-Modulated Three-Level Inverters With a Single Z-Source Network," Power Electronics, IEEE Transactions on , vol.28, no.6, pp.2806-2815, June 2013

## C.2 Conference papers

i. Effah, Francis B.; Watson, Alan J.; Wheeler, Patrick W.; Clare, Jon C.; De-Lillo, Liliana, "Space-vector-modulated three-level Z-source hybrid direct AC-AC power converter," Power Electronics and Applications (EPE), 2013 15th European Conference on , vol., no., pp.1-10, 2-6 Sept. 2013

ii. Effah, F.B.; Watson, A.J.; Wheeler, P.W.; Clare, J.C.; Sunter, S., "Optimal switching pattern for space vector modulated Z-source NPC inverter," Power

Electronics, Machines and Drives (PEMD 2012), 6th IET International Conference on , vol., no., pp.1-6, 27-29 March 2012