The High-Frequency Application

of

Double-Barrier Resonant Tunnelling Diodes

by

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This Thesis is dedicated to my wife Karen, and my family for their love and support, and to all those who helped me along the way.

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ABSTRACT

The aim of this Thesis was to try to develop an understanding of the growth and fabrication of Double Barrier Resonant Tunnelling (DBRT) diodes, in order to enhance their properties at millimetre wave frequencies (ie. above 35GHz). Chapter 1 introduces the DBRT diode and outlines some of its applications while Chapter 2 describes aspects of device fabrication. Chapter 3 discusses the solid-state and quantum mechanical aspects which determine the DBRT's current-voltage characteristics and Chapter 4 describes an extensive parametric study relating the device properties to the high frequency behaviour. Chapter 5 covers the applications of DBRT devices at high frequencies and presents some of the results achieved so far.

Besides the primary objective of studying the properties which determine the high frequency application of DBRT devices (via. the characterization of an extensive range of structures grown for the project), the other goal was to try to improve upon the results of other workers in terms of generating power and to improve the efficiency of up and down conversion at millimetre wave frequencies. Perhaps the most promising application of DBRT devices is as self-oscillating mixers (SOM) which can also provide conversion gain (due to the wide bandwidth of the negative differential resistance) at the intermediate frequency. This is of great importance since it negates the need to generate a local oscillator signal and dispenses with complicated image-rejection mixer arrangements (for superheterodyne mixing) and amplification stages, which are very difficult to build and are expensive at millimetre wave frequencies. Whilst working in collaboration with staff at the University of Leeds, department of Electronic and Electrical Engineering a SOM was fabricated on microstrip which gave a modest gain at around 10GHz. Similarly a DBRT diode was operated in waveguide at 106GHz and provided -9.8dBm of power as measured on a spectrum analyzer. Both of these results represent (to the authors knowledge) the best results currently seen for DBRT devices in the UK and Europe.

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CHAPTER 1

Double Barrier Resonant Tunnelling and its Application to High Frequency Devices

1.1 Introduction: an outline of the device and its operation

The process of tunnelling is a quantum-mechanical phenomena which was first used to describe α-particle decay and it is a direct demonstration of the wave-mechanical nature of matter. Tunnelling occurs when a particle with an energy less than required to classically surmount a barrier is able to pass through the barrier. The explanation for this behaviour involves a description of the "particle" by a probability distribution function or wavefunction. One of the properties of this wavefunction is that neither it nor its first derivative can be discontinuous in space. This implies that at a potential discontinuity there is a finite probability of finding a particle on either side of the discontinuity and that the wavefunction may penetrate into an otherwise classically forbidden region. For a sufficiently thin (<100Å) barrier the probability that the particle will be found on the other side is high (Figure 1.8); this probability of the particle being found on the opposite side of a thin barrier is referred to as tunnelling through the barrier. Single barrier tunnelling is extensively discussed throughout the literature on quantum-mechanics [1, 2, 3] and will only be summarised here.

In the field of semiconductors, tunnelling has been exploited since the late fifties. In 1958, Esaki first applied the theory of tunnelling to explain the behaviour of the

devices which bare his name [4]. These (Esaki tunnel) devices were at the time routinely used at higher frequencies than those based on the Schottky principle. The increased understanding of Schottky devices together with the advent of field-effect transistors and the difficulty in the control of fabrication of the tunnel diodes lead to their demise except for a few specialist applications where they outperformed Schottkies. Nevertheless tunnel devices were used at microwave frequencies and even millimetre-wave frequencies in the early days [5,6] as low-power oscillators (and detectors), and also in parametric (reflection) amplifiers. Extensive research into their properties was carried out at this time and it is this work which has expedited the recent application of double barrier resonant tunnelling diodes [7,8].

The majority of tunnel devices rely on only one tunnel barrier but the exact nature of the tunnelling process is not always the same; e.g. band-to-band tunnelling in the case of the early (Esaki) semiconductor devices or Cooper-pair tunnelling in the case of the superconductor-insulator-superconductor junctions. This Thesis will only be concerned with semiconductor conduction-band barrier devices and the specific case of double barrier devices. The double barrier devices described in this thesis owe their characteristics to the process of sequential tunnelling [10], rather than (as the title of this work suggests) to resonant tunnelling. The equivalence of these two "pictures" is discussed by Weil & Vinter and it is sufficient for the present purposes to realise that the current through devices of this type is the same whichever transmission process is taking place [9,10, 52]. The misnomer in the title of this work (resonant) is defended, due to the widespread use of the term which is immediately associated with the type of operation.

Double barrier resonant tunnelling (DBRT) devices were first proposed by Esaki in 1970 [11], but it was not until 1974 that the first demonstration of negative differential resistance by this method was seen [49]. This demonstration was made possible by the advent of Molecular Beam Epitaxy (MBE), which allowed monolayer control of the growth of heterostructure devices and therefore the growth of the necessary thin barriers (<100Å). Because of its importance with regard to the production of DBRT's

the process of MBE is more fully discussed in Chapter 2. With the control of barrier widths down to several monolayers (~20Å) the operation of these devices was possible well into the millimetre-wave range of frequencies with current densities of 1 $*10^5$ Acm^{-2} [12, 13, 14, 15]. By the late 1980's, operation of DBRT diodes had been observed up to 420GHz for the GaAs/AlAs material system [16].

One of the main present limitations to the maximum frequency of operation is the resistance of the contacts which sets a limit to the R.C. product such that reducing the contact area beyond a certain point has a detrimental effect on the resistance of the contact (which is set by the specific contact resistance). The operation of DBRT's at higher frequencies (>500GHz) is often facilitated by the use of alternative material systems mainly through an accompanying improvement in the minimum specific contact resistance [17].

Another important and often quoted feature of DBRT's is the peak-to-valley current ratio. This ratio of the peak and valley currents is considered to be an indication of the control of the growth conditions and especially the quality of the interfaces between the different materials. Large values of the peak-to-valley ratio, together with large current densities are often viewed as permitting high values of available output power if the device is operated as an oscillator. It has been postulated that the maximum available output power of such an oscillator should be given by the relationship $3/16\Delta I\Delta V$, where the value 3/16 arises from the sinusoidal shape of the oscillating waveform [18]. However, in reality this calculation should also include the power lost in the resistance in series with the device due to both the contacts and the load. Therefore, the low value of negative differential resistance (NDR) which results from the high peak-to-valley ratios and high current densities presents problems with extracting this power, especially if operated in a waveguide environment ($Z_0 \approx 350$ Ohms).

A useful method for increasing the NDR without reducing the peak-to-valley ratio or the peak current is by increasing ΔV; this may be achieved by incorporating a low

doped "drift" region in the collector of the device where the electrons can gain more energy from the bias circuit and, because of the extra voltage drop across the device (including the NDR region), can supply more energy to the load [19, 20, 21, 22]. The maximum operating frequency of the device is also increased by reducing the capacitance per unit area as a result of the extra depletion in this low-doped drift region. Devices which deliberately set out to use low-doped drift regions are referred to as quantum well injection transit-time (QWITT) devices, although it is now thought that many of the earlier quantum well oscillators embodied this principle in their operation.

For the work presented in this Thesis, many different layer structures were developed to investigate the effects of growth (if any) and fabrication-dependent effects on the microwave behaviour of DBRT diodes (Chapters 2 and 4). In addition, many of these devices were investigated in various microwave applications (Chapter 5). To underpin this work, a fuller treatment of the theory of operation is presented in Chapter 3. The overall objective of the study was to develop a fuller understanding of DBRT's and their potential future applications in microwave and millimetre-wave systems.

1.2 A review of some elementary relevant background semiconductor theory

This review is deemed necessary to introduce some of the semiconductor properties upon which the DBRT's rely. A précis of many of the useful properties of GaAs has been previously reviewed by Blakemore [23]. Figure 1.1 shows the (standard) band structure diagram for GaAs. This band structure is modified by the introduction of fractions of aluminium into the lattice; the interface between GaAs and the $Ga_{1-X}Al_XAs$ alloy gives rise to many of the interesting conduction properties which are discussed and exploited in this Thesis.

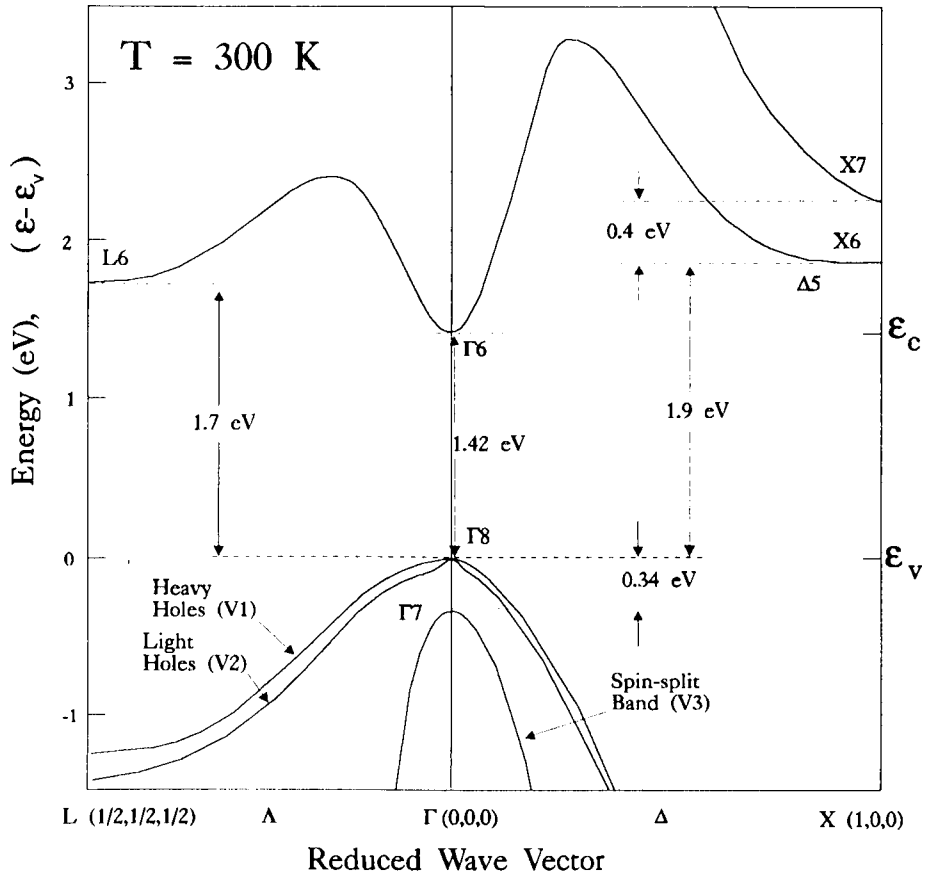


Figure 1.1 Energy-band structure for GaAs

The band structure is a result of the underlying crystal structure of the material (see Figure 1.2). In the compound semiconductor GaAs each atom is surrounded by four nearest neighbours of the other atomic species and arranged in a tetrahedron. The resulting lattice is termed the "zincblende" lattice, and the crystal structure is described by two interpenetrating face-centred cubic lattices each of which contains a single atomic species, and the lattices are separated from one-another by one quarter of a body diagonal [24]. The bonding between these nearest neighbours is covalent but the presence of the oppositely-charged ion species displaced from one-another produces a dipole. The displacement of this dipole gives rise to the complicated phonon behaviour seen in such compound semiconductors. Another more practical result of

the two interpenetrating face-centred cubic lattices of differing atomic species is that there are planes of both atoms of a single species (and associated bonds) which, depending on their crystallographic orientation, can be preferentially attacked by acid-peroxide based etches [25]. Of the eight {111} planes in the crystal lattice of GaAs, four planes contain only arsenic atoms and four contain only gallium atoms. This results in many useful device processing techniques (section 2.6) and also facilitates easy cleaving along the {110} family of planes.

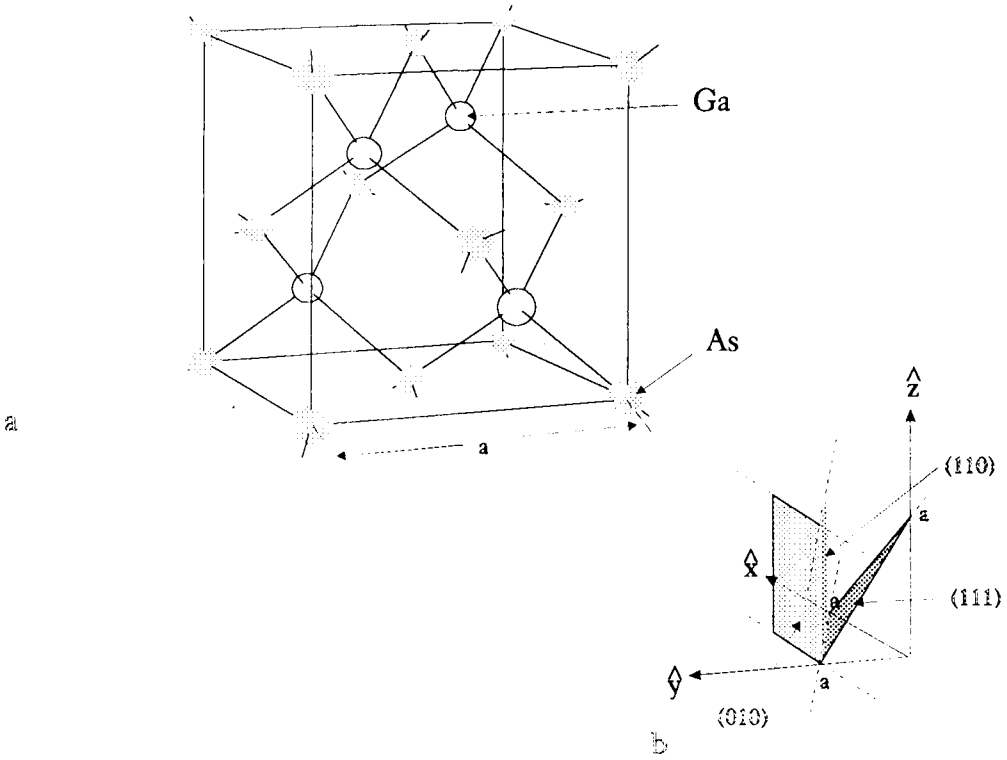


Figure 1.2 (a) Crystal Lattice for GaAs, (b) the family of crystal planes for GaAs

The behaviour of the outermost (current carrying) electrons of the atoms in a semiconductor is controlled by the underlying periodic field of the fixed atoms in the crystal. The rapidly-varying potential requires a non-classical description of the resulting motion and which determines the reaction of an electron to a change in potential. An approximation to the potential which an electron in a semiconductor experiences is described by Kronig & Penney and has been discussed at length by Nag among many others [26, 27]. The solution of the time-independent Schrödinger equation to the periodic potential leads to only certain allowed values for the wave function. The electron wave function is referred to as a Bloch function or Bloch wave and the electrons described by these Bloch waves are then only permitted to have energies within certain bands which are separated by other bands of forbidden energies (gaps). Imperfections in this periodic lattice, as a result of the presence of impurities, give rise to allowed (impurity) energy levels within these forbidden bands. The upper-most bands determine the normal electrical characteristics. The top two allowed bands are termed the conduction and valence bands. The lowest states in the conduction band and the highest states in the valence band, together with those of the impurity states, are of direct relevance to carrier transport. In this Thesis we shall be concerned only with the current carried by the electrons.

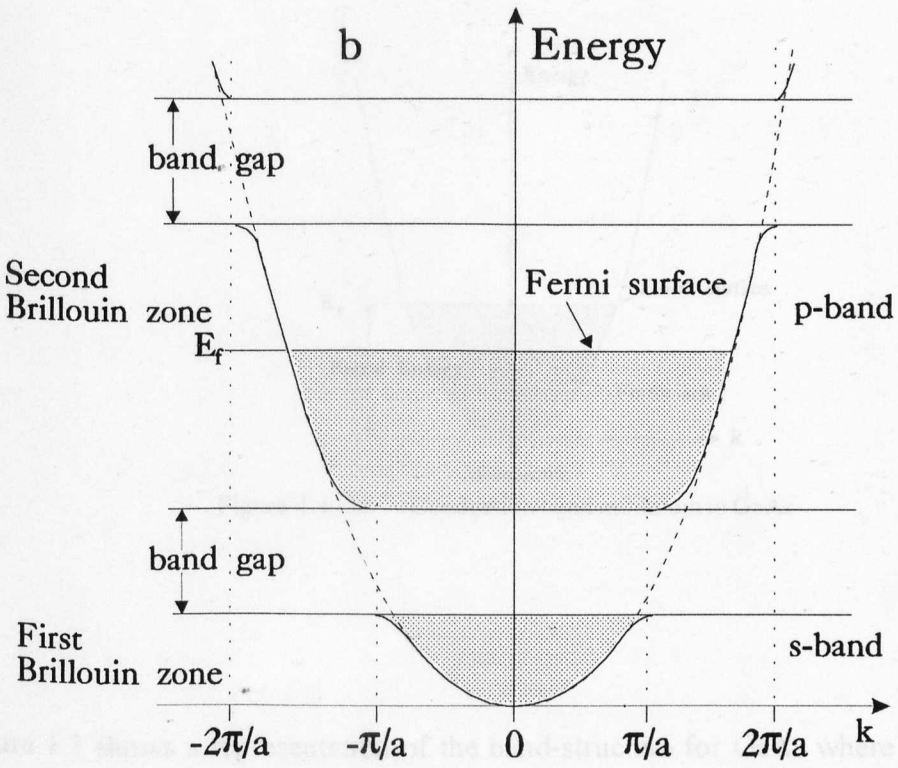


Figure 1.3 Reduced zone representation of conduction band for GaAs

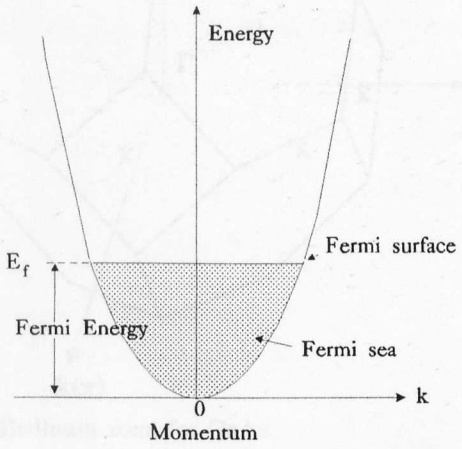


Figure 1.4 Conduction band minimum in GaAs

Figure 1.3 shows a representation of the band-structure for GaAs where the value of E is periodically dependent on k. This "picture" is referred to as the reduced zone representation of k-space. Figure 1.4 follows on from Figure 1.3 and shows only the region around the conduction band minimum. A diagram of the first Brillouin zone for GaAs is shown in Figure 1.6 and this results in the E-k diagram of potential versus momentum for GaAs, shown in Figure 1.1. The band structure of GaAs has only been firmly established relatively recently (1976) using UV electro-reflectance of schottky barriers [29]. Electrons preferentially occupy the region around the lowest minimum in the conduction band referred to as the zone centre and in GaAs the resulting constant energy surface is spherical. The most important directions through the

Brillouin zone for GaAs in terms of the electronic band structure are from the zone centre (Γ) to the X,L and K points at the zone boundary.

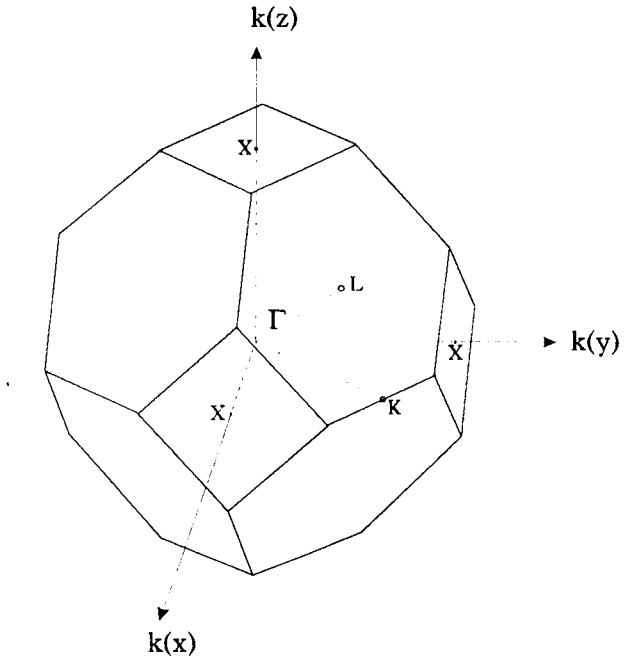


Figure 1.6 Brillouin zone for GaAs

By using the concept of an "effective mass" in place of the free electron mass, the electron behaviour in the presence of an electric field can be described by classical mechanics. An effective mass is defined by the rate of change of group velocity divided by the accelerating force i.e. $1/m^* = (1/\hbar^2).d^2E/dk^2$. In the special case where the E-k curve (Figure 1.3) is parabolic, this effective mass is also given by $1/m^* = (1/\hbar^2k).dE/dk$ i.e. the crystal momentum divided by the group velocity. Under conditions of high electric fields the electrons may gain sufficient energy (in comparison with that associated with the lattice vibrations) to move higher "up" the E-k curve. At energies greater than about 100meV from the conduction band bottom

the non-parabolicity of the E-k relationship implies modifications to both the effective mass and the density of available conduction band states which are appropriate to the bottom of the band. These modifications are well-explained by Blakemore [23] and need to be borne in mind since such second-order effects may be extremely important in some specific cases of tunnelling. The electron effective mass is much smaller than the free-electron mass and is generally directionally-dependent within the crystal. The value of the effective mass is important in DBRT's in helping to determine the tunnelling coefficient. Expressions for calculating the value for the effective mass (conductivity effective mass at 300K) of an electron are used in later calculations and are given in the review article by Adachi [28] and are as follows:

$$m_e^{\Gamma} = 0.067 + 0.083x \tag{1.1a}$$

$$m_e^{X} = 0.32 - 0.06x \tag{1.1b}$$

$$m_e^{L} = 0.11 + 0.03x \tag{1.1c}$$

In the diagrams which follow and which are used to pictorially represent the process of resonant tunnelling it is only the region around the very centre of the conduction band minimum (Figure 1.3) which is shown. The minima for the X, L, and K directions are at much higher energies and are therefore usually ignored. This assumes that the electrons do not reach sufficiently high energies (by comparison with $kT_{lattice}$) so as to scatter into these valleys (an effect used in Gunn devices). However, for the process of resonant tunnelling this may not always be true, since the electrons leaving the quasi-confined state in the well (formed by the two barriers of $Ga_{1-X}Al_XAs$) are, for the devices studied in this Thesis, at energies typically 100meV above the conduction band minimum in the collector contact. After being emitted from the well these electrons are further accelerated by the electric field in the "drift" region of the collector. In extreme cases the electrons may gain sufficient energy to transfer to an adjacent valley and the device would behave more like a "hot-emitter" Gunn (or

camel) diode.

Another case where the above simplification (of considering only the minimum to be occupied) may be incorrect is when the alloy fraction of aluminium is increased beyond about 0.4. At these high aluminium fractions, the Γ and L valley minima cross one another with the result that the L valley becomes the lower minimum. A similar effect can be achieved by varying the hydrostatic pressure while keeping the aluminium fraction constant. The nature of the band-gap then becomes indirect (i.e. the conduction-band minimum and the valence-band minimum are no longer adjacent with respect to the Brillouin zone centre). Some of the devices studied in this thesis have barriers composed of AlAs (NU-298, NU-456, NU-457, NU-462 and NU-366). For devices from these layers the electron transport in the regions of the semiconductor where the nature of the band-gap changes (Γ-L), involves a proportion of the electrons which were in the Γ minimum transferring to the L minimum (with a loss of a phonon and an increase in effective mass). The "simple" picture of tunnelling therefore, may involve a contribution due to the electrons which have transferred to the L valley during tunnelling and which would transfer back again to the Γ valley when in the collector referred to as "mixing". In the layer structures mentioned, the barriers were only 17Å thick and the tunnelling times were thought to be sufficiently short so as to limit the number of electrons which may experience this mixing. However, if the barriers were increased in width while maintaining the high aluminium fraction this mixing may become a problem. To the author's knowledge, measurements of the (high-frequency) effects of mixing on tunnelling have not been discussed in the literature and so it is impossible to evaluate the possible effects of such mixing on the devices discussed in this Thesis.

1.3 Double-barrier resonant tunnelling

As described in the previous section, the term double barrier resonant tunnelling is

used to describe a special case of double barrier heterostructure tunnelling where the tunnelling process is dominated by coherent transmission rather than sequential transmission. In coherent transmission the phase of the particle (in this case, an electron) is preserved as it traverses from the emitter to the collector. Sequential transmission on the other hand, does not require that the electron retain its original phase (or, in effect, retain a knowledge of where it has been) [30]. A more complete mathematical description of heterostructure tunnelling follows in Chapter 3, but the following is given by way of an introduction.

1.3.1 The qualitative description of tunnelling

Resonant tunnelling is the specific case of tunnelling where the proximity of two tunnel barriers, and the resultant quantum confinement, favours a resonant enhancement of the tunnelling probability for a particles with a wavelength equal to (or a half integral number of) the distance between the barriers. This resonant enhancement of tunnelling, for electrons within a specific range of energies, corresponds to a peak followed by a trough in the current-voltage characteristic when a bias voltage is applied.

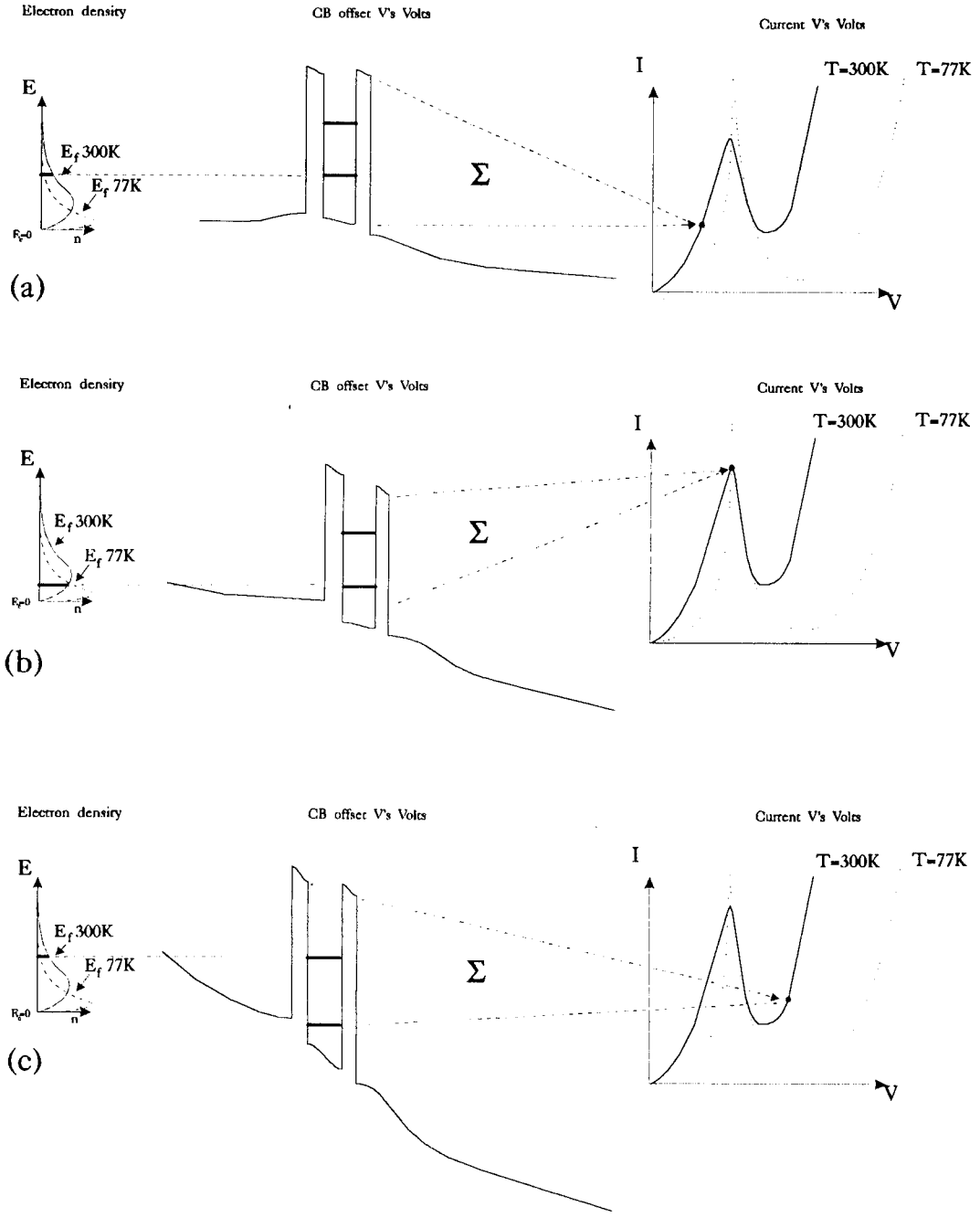


Figure 1.7 Representation of tunnelling versus applied bias, leading to current versus bias.

The current is a convolution of the electron distribution (Fermi-Dirac) in the emitter contact and the corresponding tunnelling probability which is a function of the applied bias. More qualitatively, at low bias the electrons in the emitter experience the combined (and very low) transmission probability of both barriers (Figure 1.7(a)). However, for a small number of electrons in the high energy tail of the Fermi-Dirac distribution in the emitter there exists a resonant enhancement of the tunnelling probability. It is these electrons which contribute to the majority of the observed current. As the applied bias is increased, greater numbers of the electrons (reflecting the shape of the Fermi-Dirac distribution) are available for tunnelling and the current increases. At some point during the increase in the applied bias there is a maximum in the number of electrons available for tunnelling (corresponding to the peak in the Fermi-Dirac distribution) and this corresponds to a maximum in the current through the device (Figure 1.7(b)). As the bias is increased further the current drops due to a reduction in the number of electrons with the "correct" resonant energy. Apart from the range of resonant energies the transmission probability is very low, so that even the electrons in the high energy tail are unlikely to tunnel (Figure 1.7(c)) unless, of course, these electrons are in resonance with a second quasi-confined state or they can tunnel through (or over) the reduced potential barrier near the top of the barriers. As the bias is again increased an ever-increasing number of electrons can tunnel through higher quasi-confined states or through the top of the barriers and the current then rises again.

1.3.2 The quantitative description of tunnelling

For simplicity only the steady-state transport in one dimension (1-D) (i.e. the tunnelling direction) will be considered and the behaviour of this wavefunction at an interface and a barrier is represented by Figure 1.8(a&b, respectively).

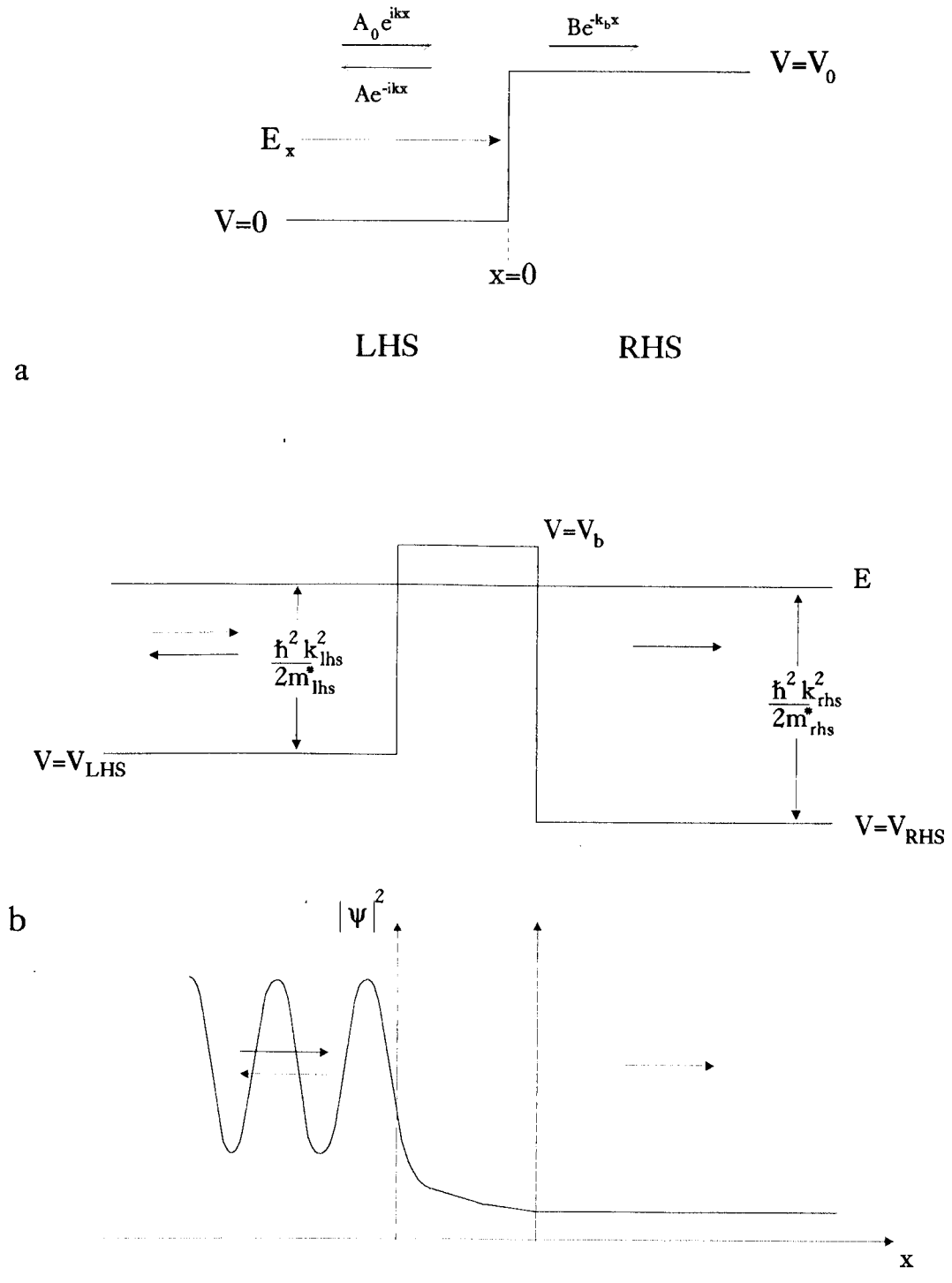


Figure 1.8 Representation of the behaviour of the wavefunction at (a) an interface, and (b) a barrier,

The motion of the particle is described by the 1-D time independent (steady-state) Schrödinger equation (1.2), which describes quantum mechanically the motion of a particle in a region of space.

The solution of the 1-D steady-state Schrödinger equation yields the wavefunction (1.4) of the particle under consideration.

The 1-D time independent Schrödinger equation is as follows:

$$-\frac{\hbar^2}{2m^*}\frac{d^2\psi}{dx^2} + V(x)\psi = E_x\psi \qquad (1.2)$$

where: ψ represents the probability amplitude of finding the particle in this region of space (i.e. at x), $[(-\hbar^2/2m^*).(d^2\psi/dx^2)]$ is the kinetic energy of the system, V(x) is the potential energy and E_x is the energy of the system in the x direction, given by :

$$E_x = E - \frac{\hbar^2 k_y^2}{2m^*} - \frac{\hbar^2 k_z^2}{2m^*} \quad . \qquad (1.3)$$

E represents the total energy of the system and the terms $\hbar^2k^2/2m^*$ are the kinetic energy in the appropriate directions.

To predict the behaviour of a particle at an interface, Equation 1.2 is solved for each region adjacent to the interface. These solutions describe the wavefunction in each region and take the form:

$$\psi(x) = A\exp(ik_x x) + B\exp(-ik_x x) \quad , \qquad (1.4)$$

where A and B represent the amplitudes of the waves travelling towards and reflected from the interface, respectively, and

$$k_x = \left[\frac{2m^*}{\hbar^2}(E_x - V_0) \right]^{\frac{1}{2}} . \qquad (1.5)$$

E_x is the energy of the particle in the x direction and V_0 is the potential energy in this region of space. The subscript zero represents X= 0 at the interface (Figure 1.8 (a)).

The solutions for the wavefunction $\psi(x)$, and $(1/m^*.d\psi/dx)$ on each side of the interface are equated (which guarantees the conservation of flux on both sides). This is shown as:

$$\psi_{lhs}(x_0) = \psi_{rhs}(x_0) \qquad (1.6)$$

and

$$\frac{1}{m^*_{lhs}} \frac{d\psi_{lhs}}{dx} \Big|_{x=x_0} = \frac{1}{m^*_{rhs}} \frac{d\psi_{rhs}}{dx} \Big|_{x=x_0} . \qquad (1.7)$$

The solution of these equations can be carried out algebraically for simple potential profiles or by using various approximate methods (e.g. the Wentzel, Kramers-Brillouin [WKB] method), although such methods may have restricted application. The result of the conservation of flux on either side of the interface (and also barrier, if sufficiently thin) is that the wavefunction of the particle can be found on the other side (Figure 1.8 (b)).

Recently, various computer-intensive approaches have been introduced. These include the transfer matrix approach (Chapter 3, and [33]) and a hybrid monte-carlo/quantum mechanical technique [31]; such techniques may be of value for situations where the potential varies rapidly in different device regions.

1.3.3 Some useful expressions for understanding DBRT's

Before going on to discuss the potential of the DBRT device for high frequency applications, a few simple calculations will be introduced which illustrate the dependence of some of the characteristics of the device without resort to the more complex treatment of Chapter 3.

The position of the quasi-confined state in the well is calculated using elementary quantum mechanics and the equations mentioned in the previous section for a single barrier. In the more involved treatment of Bastard the number of confined states in a potential well is given by [34]:

$$n(L) = 1 + Intg.\left[\sqrt{\frac{2m^{*}V_{b}L_{w}^{2}}{\pi\hbar^{2}}}\right], \tag{1.8}$$

where: n(L) represents the number of confined energy levels (as a function of well width), Intg. represents the integer value of the expression in brackets and V_b describes the barrier potential with respect to the well bottom. Equation 1.8 follows on from an algebraic solution of the following two equations:

$$k_{w}\tan\left(k_{w}\frac{L_{w}}{2}\right) = k_{b} \tag{1.9a}$$

$$k_{w}\,cotan\left(k_{w}\frac{L_{w}}{2}\right) = -k_{b} \tag{1.9b}$$

where k_w and k_b are defined by equations 1.5 and which themselves are solutions to equation 1.4 for the two regions (barrier and well) and are due to the condition that both the wavefunction and its first derivative must be continuous.

In the case where the barriers are infinitely high ($k_b \rightarrow 0$) then the solutions to Equations 1.9 (a) & (b) are $k_w L = n\pi$ (n = 1,2,..) and give [34]:

$$E_n = \frac{\hbar^2\pi^2}{2m^*L_w^2} n^2 \ . \qquad (1.10)$$

The above equation gives an approximate position for the confined energy levels with respect to the bottom of the well. This is accurate provided the electron experiences infinitely high confining barriers. However, in the case where the barriers are of a finite height then equations 1.9 (a) & (b) must be solved to reveal the more accurate position of the confined state. If the barriers are no longer of infinite width, then the treatment of Chapter 3 must be used to find the position of the energy levels which are now only quasi-confined .

From a knowledge of the position of the quasi-confined energy levels we can estimate the time for an electron to escape from the well [10]. The escape time is determined mainly by the value of the transmission coefficient through the collector barrier, which can be approximated as follows:

$$T_x = \frac{16\,E_x(V_b - E_x)}{V_b^2}\, e^{-2k_b L_b} \ , \qquad (1.11)$$

where: E_x is the incident energy, V_b is the barrier potential, L_b is the barrier length and k_b (from Equation 1.5) is the attenuation factor in the barrier, ie.

$$k_b = \left[\frac{2m_b^*(V_b - E_x)}{\hbar^2}\right]^{\frac{1}{2}} \ , \qquad (1.12)$$

where m_b^* is the effective mass in the barrier.

The velocity of an electron in the well can now be calculated [50] from

$$v_w = \left(\frac{2E_1}{m_w^*}\right)^{\frac{1}{2}} , \qquad (1.13)$$

where: E_1 is the energy of the first quasi-confined state (assumed to be the energy of interest, ie. responsible for the first current peak) and m_w* is the effective mass of an electron in the well. The escape rate is then given by the product of the attempt rate (τ^{-1}_{att}), (the number of times per second that the electron is incident on the barrier) and the transmission coefficient (T_x) of that barrier.

The attempt rate is given by :

$$\tau_{att.}^{-1} = \frac{v_w}{2\,(L_w + 1/k_b)} , \qquad (1.14)$$

where (L_w + $1/k_w$) is simply the effective well width. This is the width of the well plus the penetration length of the electron in the barriers (assumed to be the same for both barriers) and is approximately equal to the exponential decay factor for the barrier in question. The escape rate is now given by;

$$T_{esc.}^{-1} = \tau_{att.}^{-1}\, T_x \qquad (1.15)$$

From the above equations the reader can gain an appreciation of the suitability of a particular DBRT device to an application, with respect to its frequency limitations. For such applications, however, a knowledge of the approximate device operating-point impedance is also required, which requires approximate calculations of the type described in Chapter 3.

1.4 The contribution of device models to the understanding and application of DBRT devices

Section 1.1 through to 1.3 describe the background to understand DBRT's and the possible high frequency applications in which such devices can be used is briefly touched on in section 1.5. However, before a device can be exploited to the full, an understanding of both it and its interaction with the system is required. This can be achieved by careful measurement and relating these measurements to the physical processes within the device; this procedure often leads to an equivalent circuit representation for the device, which may be thought of as essentially a summary of its impedance behaviour. This procedure has indeed been attempted and is described in Chapter 4. These measurements, and the equivalent circuit models which they suggest, can be used to design the necessary circuit to optimise the match between the device and the system. An understanding of the match between the device and the system is necessary to achieve the "best" performance for the combination. In order to evaluate the match both the system and the device tend (for simplicity) to be represented by equivalent circuit descriptions. These equivalent circuits seek to describe a simple circuit which, over a limited range of frequencies and conditions, represents the behaviour of the device or system. The various equivalent-circuit models which have historically been developed to represent a device are described below.

1.4.1 Model alternatives and usefulness

Possible models and how they relate to the devices are described as follows :-

Small-Signal models

Through the measurement of the device S-parameters (small-signal by nature), a system can be designed based on this data alone. This requires that devices exhibiting similar characteristics will be available when the system is subsequently realized. This is a very precise approach provided that there is a good degree of consistency in reproducing the original device. System designs based on this approach can be intolerant of individual device-to-device variation unless such a range of actual devices was used at the design stage. As an example of how such small-signal models can be important in system design is that in the case of an oscillator (which is a large-signal problem), where the start-up conditions are often a result of small-signal conditions.

In the case of relatively simple devices, measurements of the d.c. current-voltage and capacitance-voltage characteristics can be made and a lumped-element equivalent circuit model arrived at.

As a more sophisticated development of the above approach, the d.c. behaviour can be approximated from experience by a more detailed and physically realistic model of the device. From this, the current-voltage and impedance behaviour may be predicted without necessarily representing the device in terms of a lumped element circuit. This approach is built on a knowledge and experience of previous devices but, if the physical understanding is quantitatively correct, it can also be used for the design of systems which incorporate devices which are unavailable prior to system design.

Large-Signal models

Unfortunately for the application of many types of device including the DBRT the small-signal information is not always sufficient to predict the behaviour when used in high power applications. Examples of this are when the devices are used as oscillators or harmonic up-converters (multipliers) and down-converters (mixers). The prediction of the non-linear (large-signal) behaviour from first principles is an extremely difficult task [35]. Often the more accurate and physical a model for a solid-state device is, then the greater is the possibility to develop a non-linear model from this solid-state model. Fortunately, in most cases, a knowledge of the small-signal behaviour can often be sufficient to design an approximate large-signal system.

Non-linear large-signal behaviour can be measured using "load-pull" measurements and, as in the previous small-signal case, it is often best to use this data to design the system rather than proceeding from a less accurate theoretical model. This is especially the case for the large-signal treatment where the confidence in the model may be modest. Load-pull techniques are easiest to understand in the case of an oscillator, where the device is operated as an oscillator and the load and embedding impedance is adjusted to provide the maximum available output power. The condition for this maximum power transfer to the load takes place only if the load and embedding impedance are the complex conjugate of the device impedance. Hence, this impedance can be evaluated by optimising the embedding network for maximum power transfer and then removing the device and measuring the impedance of this network as seen from the device plane. This is a more complex procedure than for gathering the small-signal impedance and suffers from the limitation of requiring relatively high oscillator powers (>1mW) in order to measure the sensitivity of this power transfer to the match presented by the embedding network. The lack of high powers was found to be the problem with carrying out such measurements on the DBRT devices which are described in this

Thesis.

Noise models

Noise models are also useful in integrated system design in a similar way as to the above cases. As in the large-signal case, and due to the complicated nature of noise behaviour, it is often best to carry out these noise measurements on the proposed devices, if these are available, and then to optimise the integrated system around this data also. Very little data has been gathered on the noise behaviour of DBRT's due mainly to the power and dynamic-range requirements of most noise measurement systems [36]. The noise in most systems is often many orders of magnitude lower in power than the signal of interest. The magnitude of this noise power relative to the signal then determines the lowest power at which the system provides a useful performance. If, as in the case of the DBRT devices, the maximum output power is low, then the available noise power is often difficult to measure with accuracy and this was again the case in this study.

Chapter 4 seeks to develop small-signal equivalent circuit models for the DBRT devices used in this Thesis, through extensive broadband small-signal impedance measurements. These broadband measurements were also attempted up to 100GHz but were unsuccessful, for the reasons discussed in Chapter 5.

1.5 Potential high-frequency uses of resonant tunnelling devices

The application of DBRT's for devices which are suitable for high frequency application is described in Chapter 5; the following section seeks to describe what DBRT devices offer by way of improvement on existing devices for microwave and millimetre-wave applications. The two major classes of solid-state device for these applications are (I) "Hot-electron" devices and (II) Schottky barrier devices. The discussion will be related to these two device types to attempt to show the comparative advantages of DBRT's in such applications.

(I) Hot-electron devices suffer from the limitation of a time delay associated with the gain in energy (or heating) of the carriers (usually electrons due to their higher mobility). This time delay results in an intrinsic high frequency cut-off for the resultant negative differential resistance, which for fundamental oscillation (in this case, transferred electron devices) tends to be around 75 GHz (30-40 mW) and 95 GHz (50-60 mW) for GaAs and InP diodes respectively. Second and third harmonic operation of these transferred electron devices is often used to overcome these limitations but the d.c. to a.c. efficiency decreases rapidly with increasing harmonic number. The results quoted in the literature which have been achieved to date are: 7mW @ 180 GHz and 0.2 mW @ 272 GHz for the second and third harmonics respectively [37].

The frequency and amplitude stability of the carrier contribute to the overall noise for hot-electron devices, together with other sources such as shot, thermal and 1/f noise. In DBRT diodes, only the shot and perhaps the thermal contributions to the overall noise figure could be expected to show an improvement [38]. This is because factors such as stability will affect each device equally, depending more on external factors such as the interaction with

the embedding network etc., while the shot, thermal and 1/f noise is material- and mode-of-operation dependent. Shot noise, in particular, is thought to be higher in the hot electron class of devices than in the tunnelling class of devices, due to an increase in the rate of collisions of electrons (and therefore variations in the current) with the lattice as they become hot and prior to transfer to the lower mobility valley. It is the difference in this noise [38] which favours the transferred electron device over the avalanche and impact ionization devices. Tunnelling is considered to be an inherently "quiet" process and is expected to yield lower noise figures for oscillators using this type of device. The low power achieved by the DBRT devices described in this Thesis (section 5.2) proved to be a limitation which prevented the making of accurate noise measurements.

(II) The schottky-based devices are widely used as detectors and harmonic converters. Their major drawback is that many of their properties are determined by the semiconductor surface prior to forming the schottky contact, and thus are difficult to control fully.

One major application for schottky diodes at microwave and millimetre wave frequencies is as detectors (and harmonic down-converters), where the magnitude of the rectified output signal is proportional to the power of the signal received. The devices can be operated at zero bias, but are more often operated at low bias. However, milliwatt levels of signal power are often required to provide acceptable output voltages and for lower power applications conventional tunnel or superconducting-insulator-superconducting tunnel diodes are used. It is these lower-power (room temperature), more sensitive applications which would undoubtably benefit from the use of DBRT devices. The control of the current-voltage characteristic which is possible for double barrier devices is such that the characteristics can be tailored to exhibit very strong non-linearities in the region of zero volts and thus should favour

zero biased detection or mixing. For example this might be achieved by altering the position of the conduction band by using InGaAs in the collector, AlGaAs barriers, an InGaAs well and a GaAs emitter. This should result in a current-voltage characteristic very similar to a tunnel diode but with the extra control of the impedance permitted by varying the width of the well, the barriers and the emitter and collector doping independently. The "buried" nature of the active region in the DBRT devices also favours improved power handling by reducing the number and effect of impurities and surface states on the local electric field which is often responsible for the premature breakdown effects of Schottky barrier devices.

Schottky devices are also used in Harmonic up-converters or multipliers and again their characteristics suffer from the lack of control and power limitations due to their surface dependent properties. The buried nature of DBRT devices and the greater control of their current-voltage characteristics imply that they are a natural choice for harmonic multipliers [39, 40, 41, 42]. This is especially so in the case of DBRT's which exhibit anti-symmetric (mirrored about the origin) current-voltage characteristics; such devices when operated at zero applied volts do not favour up-conversion to even harmonics and thus make ideal triplers or quintuplers. The lack of even harmonics greatly simplifies the necessary embedding circuit for producing a tripler and there is also the possibility of higher efficiencies due to the lack of power lost in even-harmonic conversion. "Back-to-back" schottkies have been used in the past for application where the suppression of even harmonics was desirable, but again their properties are not as easily controlled as those of DBRT's and especially since identical devices are required. For harmonic multiplication, the application of high local oscillator powers is favoured to help to overcome the loss associated with such conversion and again the buried nature of the active region of DBRT devices and their very high current capabilities should permit higher "drive" powers than are possible using schottky devices. The anti-symmetry possible in DBRT's also favours sub-harmonic mixing and again the

extra control of the current-voltage characteristics and the low levels of applied bias offer the advantage of lower local oscillator power requirements than schottky devices.

Self-oscillating mixing (SOM) occurs when the device produces its own local oscillator signal and can simultaneously mix this with the main (received) signal to produce an intermediate frequency (IF). This dispenses with the need for a separate local oscillator which, at millimetre wave frequencies, can greatly reduce system cost. The capability of DBRT devices to operate as SOM's together with their ability to provide gain at the IF is perhaps one of the most promising applications of DBRT's [43, 44, 45, 46]. These applications are not new and were first attempted using conventional Esaki tunnel diodes. However, the lack of control of fabrication of the original tunnel diodes resulted in great difficulties in achieving a specific impedance, and was no doubt a significant factor influencing their use.

In addition to the two main classes of device considered above, it is appropriate to mention planar doped barrier (PDB) devices [47, 48]. Like DBRT diodes, these devices depend on the improved growth capabilities of MBE (or MOCVD) and rely on a buried barrier, together with the level of adjacent-layer doping, to control the d.c. and high frequency characteristics. The surface-dependent properties of the schottky devices are thus avoided and the control of the d.c. and a.c. characteristics are also improved. However, the properties of the PDB devices do not presently offer any extra degree of control in the d.c. and ac. characteristics compared to DBRT devices. This is mainly due to the fact that the characteristics of the PDB device result from a blend of the properties of the barrier together with the levels of doping in the adjacent layers. By comparison the characteristics of the DBRT device depend principally on the properties of the barrier and well regions with respect to one another. The PDB devices have been proposed as a potential future replacement in applications which require tight control of the characteristics of

the schottky devices [47, 48], especially with regard to the noise figure. Similarly, there is an excellent potential for the DBRTD's to fulfil this objective but perhaps without some of the drawbacks of the planar doped barrier devices.

1.6 Conclusion

This chapter has introduced the DBRT and given an indication of its background operational physics and likely applications. Particular mention has been made of the use of device models in improving both the physical understanding of device performance and future system applications. The objective of this Thesis is to attempt to demonstrate that DBRT-based systems have a significant role in millimetre and microwave applications, and that this follows from the devices physical properties which complement and extend those of both established devices (e.g. Transferred electron devices, Schottky-barrier devices) and novel devices such as the PDB.

1.7 References:

[1] French, A.P. & Taylor, E.F. (1979). An introduction to quantum physics. *M.I.T Introductory Physics Series.*

[2] Burstein, E. & Lundqvist, S., Eds. (1969). Tunneling phenomena in solids: Plenum Press. N.Y.

[3] Duke, C.B. (1969). Tunneling in solids: Academic Press. N.Y.

[4] Esaki., L. (1958). New phenomena in narrow germanium p-n junctions. *Phys. Rev.* **109**, 603.

[5] Sterzer, F. & Nelson, D. (1960). Tunnel-diode microwave oscillators. *Proc. Inst. Radio Eng.*, 744-753.

[6] Trambarulo, R. & Burrus, C. (1960). Esaki diode oscillators from 3-40 kMC. *Proc. Inst. Radio Eng.*, 1776-1777.

[7] Lee, M.A., Easter, B. & Bell. H.A. (1967). Tunnel diodes. Ed. Prof. G.D. Sims: Chapman and Hall Ltd.

[8] Gentile, S.P. (1962). Basic theory and application of tunnel diodes: Van Nostrand Co. Inc.

[9] Weil, T. & Vinter, B. (1987). Equivalence between resonant tunneling and sequential tunneling in double barrier diodes. *Appl. Phys. Lett.* **50**(18), 1281.

[10] Booker, S.M. (1992). Theory of tunnelling in double-barrier heterostructures. Ph.D Thesis, University of Nottingham.

[11] Esaki, L. & Tsu, R. (1970). Superlattice and negative differential conductivity in semiconductors. *IBM J. Res. Dev.* **14**, 61-65.

[12] Sollner, T.C.L.G., Goodhue, W. D., Tannenwald, P.E., Parker, C.D. & Peck, D.D. (1983). Resonant tunnelling through quantum wells at frequencies up to 2.5 Thz. *Appl. Phys. Lett.* **43**(6), 588-590.

[13] Sollner, T.C.L.G., Brown, E.R., Goodhue, W.D. & Le, H.Q. (1987). Observation of Millimeter wave oscillators from resonant tunneling diodes and some theoretical considerations of ultimate frequency limits. *Appl. Phys. Lett.* **50**(6), 322-334.

[14] Brown, E.R., Goodhue, W.D. & Sollner, T.C.L.G. (1988). Fundamental oscillations up to 200 GHz in resonant tunneling diodes and new estimates of their maximum oscillation frequency from stationary-state tunneling theory. *J. Appl. Phys.* **64**(3), 1519-1529.

[15] Rydberg, A., Grönqvist, H. & Kollberg, E. (1988). A theoretical and experimental investigation on millimeter-wave quantum well oscillators. *Microwave & Optical Technol. Lett.* **1**(9), 333-336.

[16] Brown, E.R., Sollner, T.C.L.G., Parker, C.D., Goodhue, W.D. & Chen, C.L. (1989). Oscillations up to 420 GHz in GaAs/AlAs resonant tunneling diodes E. R. Brown. *Appl. Phys. Lett.* **55**(17), 1777-1779.

[17] Brown, E.R. Söderström, J.R. Parker, C.D. Mahoney, L.J. Molvar, K.M. McGill, T.C. (1991). Oscillations up to 712GHz in InAs/AlSb resonant tunneling diodes. *Appl. Phys. Lett.* **58**(20), 2291-2293.

[18] Trambarulo, R.F. (1961). Int. Solid-state circuits Conf. Philadelphia PA.

[19] Song, I. & Pan, D. (1987). Efficiency and power output of the quantum injection transit time device. *IEEE Electron Dev. Lett.* **8**(12), 560-562.

[20] Kesan, V., Neikirk, D., Blakey, P., Streetman, B. & Linton, T. (1988). The influence of transit-time effects on the optimum design and maximum oscillation frequency of quantum well oscillators. *IEEE Trans. Electron. Dev.* **35**(4), 405-413.

[21] Song, I. & Pan, D. (1988). Analysis and simulation of the quantum well injection transit time diode. *IEEE Trans. Electron. Dev.* **37**(12), 2315-2321 .

[22] Botula, A. & Wang, K. (1990). Improved small-signal analysis of the quantum well injection transit time diode. *IEEE Trans. Electron. Dev.* **37**(1), 58-66.

[23] Blakemore, J.S. (1982). Semiconducting and other major properties of gallium arsenide. *J. Appl. Phys.* **53**(30), R123-R181.

[24] Kittel, C. (1986) 6th. ed introduction to solid-state physics: J wiley N.Y.

[25] Shaw, D.W. (1981). Localised GaAs etching with acid hydrogen peroxide solutions. *J. Electrochem. Soc. Solid-State Science & Technol.* **128**(4), 874-880.

[26] Kronig, R. & Penney, W. (1931). *Proc. R. Soc. A* **130**, 499-513.

[27] Nag, B. (1972). Theory of electrical transport in semiconductors. Pergamon. N.Y.

[28] Adachi, S. (1985). GaAs, AlAs, and $Al_xGa_{1-x}As$: Material parameters for use in research and device applications. *J. Appl. Phys.* **58**(3), R1-R29.

[29] Aspens, D.E., Olson, C.G. & Lynch, D.W. (1976). *Phys. Rev. Lett.* **378**. 766.

[30] Booker, S.M., Sheard, F.M. & Toombs, G.A. (1992). Effect of inelastic scattering on resonant tunnelling in double-barrier heterostructures. *Semicond. Sci. Technol.* **7**, B439-441.

[31] Collins, S., Lowe, D. & Barker, J.R. (1988). Resonant tunnelling in heterostructures: Numerical simulation and quantitatve analysis if the current density. *J. Appl. Phys.* **63**(1), 142-149.

[32] Kane, E.O. (1969). Tunneling phenomena in solids. Ed. E. Burstein & S.Lundqvist: *NATO ASI series*: Denmark (1967).

[33] Ricco, B. & Azbel, M. (1984). Physics of resonant tunneling: the 1-D double-barrier case. *Phys. Rev. B* **29**(4). 1970-1981.

[34] Bastard, G. (1988). Wave Mechanics Applied to Semiconductor Heterostructures: Les Éditions de Physique.

[35] Siegel, P.H., Kerr, A.R. & Hwang, W. (1984). Topics in the optimisation of millimeter-wave mixers. *NASA Technical Paper, Report Number 2287.*

[36] Demarteau, J.I.M., Heyker, H.C., Kwaspen, J.J.M., Van de Roer, T.G. & Kaufmann, L.M.F. (1991). Microwave noise of a DBRT diode over the full bias voltage. *Electronics Lett.* **27**(1), 7-8.

[37] Rydberg, A. (1990). High efficiency and output power from second and third harmonic millimetre-wave InP-TED oscillators at frequencies above 170 Ghz. *IEEE Electron. Dev. Lett.* **11**(10), 439-441.

[38] Sze, S.M. (1981). Physics of Semiconductor Devices: J. Wiley, N.Y.

[39] Rydberg, A., Grönqvist, H. & Kollberg, E. (1989). Millimeter-wave quantum well oscillators and multipliers. *Microwave & Optical Technol. Lett.*

[40] Rydberg, A. & Grönqvist, H. (1989). Quantum-well high-efficiency millimetre-wave frequency tripler. *Electron. Lett.* **25**(5), 348-349.

[41] Batelaan, P. & Frerkin, M. (1987). Quantum-well multipliers. *Int. Conf. on IR & Millimetre waves.* **M1.7**, 14-15

[42] Bouregba, R., Lippens, D., Palmeteer, L., Bockenhoff, E., Bogey, M., Destombes, J.L. & Leeluse, A. (1990). Frequency multiplication using resonant tunnelling diode with output at sub-millimetre wavelengths. *Electron. Lett.* **26**(21), 1804-1805.

[43] Sollner, T.C.L.G., Brown, E.R., Goodhue, W.D. & Le, H.Q. (1990). Physics of quantum electron devices. Springer series in electronics and photonics **28**, Ch. 6: Springer-verlag, Berlin.

[44] Millington, G. Miles, R. E. Pollard, R. D. Steenson, D. P. & Chamberlain, J. M. (1991). A resonant tunnelling diode self-oscillating mixer with conversion gain. *IEEE Microwave and Guided Wave Letters* **1**(11), 320-322

[45] Millington, G. Miles, R. E. Pollard, R. D. Steenson, D. P. & Chamberlain, J. M. (1993). Millimetre-wave self-oscillating mixers using resonant tunnelling devices. ((awaiting publication))

[46] Robertson, M. & Lesurf, J. (1991). Self-oscillating mixing in a quantum-well double barrier diode at W-band. *Int. J. IR & MM-waves* **12**(12), 1379-1385.

[47] Kearney, M.J. & Dale, I. (1990). GaAs planar doped barrier diodes for mixer and detector applications. *GEC J. Res.* **8**(1), 1-12.

[48] Kearney, M.J., Kelly, M.J., Davies, R.A., Kerr, T.M., Rees, P.K., Condie, A. & Dale, I. (1989). Asymmetric planar doped diodes for mixer and detector applications. *Electron. Lett.* **25**(21), 1454-1455.

[49] Chang, L.L., Esaki, L. & Tsu, R. (1974). Resonant tunnelling in semiconductor double barriers. *Appl. Phys. Lett.* **24**, 593-595.

[50] Sheard, F. *Personal communication*, Department of Physics, University of Nottingham.

CHAPTER 2

Processing and Device Fabrication

2.1 Introduction

As discussed in Chapter 1.3, it is important to understand the effect on device performance of both semiconductor material parameters and parasitic contributions in order to achieve the optimum high frequency operation of DBRT devices. As their name suggests, parasitic contributions detract from the ideal performance and typically act to limit the upper frequency of operation; the material parameters, on the other hand, are used to establish the required operating characteristic. Parasitic contributions can further be divided into low frequency effects and high frequency effects. The present section of this thesis will be concerned mainly with low frequency effects such as contact resistance and excessive shunt capacitance. High frequency parasitic contributions may be important at W-band and above. The more significant of these are: skin effect and frequency-dependent spreading resistance, possible carrier transit-time effects (and other inductive effects) and, perhaps, fringing capacitance.

A discussion of other effects which are important at sub-millimetre wavelengths [1,2] will be left until chapter 4. These effects include: carrier transit-time through the "drift" region, charge transport time through the double barrier region and the time required to re-establish equilibrium upon a rapid change in voltage. Many of the experimental limitations noted so far in DBRT's [25] have been the result of low frequency parasitics (such as contact resistance). Therefore some time will be devoted

to discussing these effects.

Unfortunately, the contributions of the material parameters cannot always be separated from the above parasitic contributions since, for example, to achieve a desirable operating characteristic (i.e. in terms of the current versus voltage profile), it may be necessary to use material parameters which contribute to an undesirable effect of a parasitic. An obvious example is the use of larger areas to increase the operating current, and hence the output power. This carries with it the penalty of a reduced operating frequency (all other things being equal) due to increased shunt capacitance across the junction. Similarly, the device design and layout have important implications with regard to the control of the parasitics which are discussed in section 2.6 of this thesis. First it is important to describe layer growth in order to enable the reader to appreciate the significance and control of the various regions of the DBRT device.

2.2 Layer growth

It has only been in the last twenty years that the epitaxial growth of III-V compounds by the process of molecular beam epitaxy (MBE) has routinely yielded layers suitable for the fabrication of high frequency (room temperature) devices. Since the class of devices on which this thesis is devoted (DBRT's) relies heavily on the atomic scale abruptness and quality of the interfaces, made possible only by MBE, then a summary of the important growth conditions used for these wafers is given below.

Molecular beam epitaxy is more-or-less a variant of an ultra-high vacuum evaporation process. This is carried out in a system with a typical base pressure, after bake-out, in the mid 10^{-11} (Torr) range. In this process the careful control of the evaporated flux of molecules (in the case of arsenic) and atoms (in the case of gallium, aluminium and silicon) makes possible the accurate growth of the subsequent layers. The molecular and atomic species are adsorbed onto the surface of the substrate before reacting

together to form a new layer which is of the same crystal structure (epitaxial) as the underlying material. The temperature of the substrate, the flux densities, and the flux densities relative to one another, are the main controlling factors of growth. The growth rate is typically arranged to be around one monolayer a second. This rate is high enough to keep down the amount of unintentional impurities incorporated in the layer, but can be interrupted almost instantaneously using shutters on each of the source cells.

The detail of the growth mechanism of III-V material is discussed by Foxon et al and by Joyce [15, 16]. In summary, the gallium atoms preferentially stick to the surface of the substrate and it is this gallium flux which determine the growth rate of the GaAs. The growth conditions are adjusted via the flux ratios so that there is an excess of arsenic molecules to prevent a gallium-rich surface. In our system the arsenic is in the form of As_4; only enough of these excess As_4 molecules are adsorbed to react with the gallium already present and any excess arsenic is again desorbed. The As_4 molecules dissociate only in the presence of paired gallium sites prior to which both species exist in weakly bound and mobile precursor state. By introducing aluminium and varying its proportion in the GaAs layer it is possible to alter the band-gap in this material . This has been referred to as "band-gap engineering" by F. Capasso and others [26]. The band-gap is un-equally distributed between the conduction band and the valence bands of the two adjacent materials. A 65% distribution, in favour of the conduction band, is often assumed and this ratio is fairly well established [17]. This discontinuity in the conduction band is utilized in the DBRT class of devices; two barriers are formed using this technique which act to confine the conduction band electrons in the GaAs "well". As a result of this confinement these electrons can move in only two dimensions in the plane of the barriers. The two dimensional confinement of the electron wavefunction results in quantized energy levels above the bottom of the conduction band in this well region. The passage of the electrons from outside (and through) this well region is only possible when they have sufficient energy in the emitter to reach these quasi-confined energy levels. Some parametric studies of the growth conditions on d.c. device behaviour have been carried out by

Söderström et al [18] and Cheng et al [19] and will form the bulk of this Thesis (in terms of high-frequency effects) and will be discussed further in Chapters 3 and 4.

The exact values used for the conduction band offset at 300K can be calculated from the following band-gap (in eV) versus aluminium fraction, shown by Adachi [20]

$$\begin{aligned} E_g^{\Gamma}(x) &= 1.425 + 1.155x + 0.37x^2 \\ E_g^{X}(x) &= 1.911 + 0.005x + 0.245x^2 \\ E_g^{L}(x) &= 1.734 + 0.574x + 0.055x^2 \end{aligned} \qquad 2.1(a)$$

For comparison the Band-gap energies (in eV, for $0.2<x<0.55$) at 4K have been calculated by Henning et al [21]:

$$\begin{aligned} E_g^{\Gamma}(x) &= 1.519 + 1.34x \\ E_g^{X}(x) &= 2.036 + 0.16x \\ E_g^{L}(x) &= 1.775 + 0.792x \end{aligned} \qquad 2.1(b)$$

These values are used in Chapter 3.2 for the calculation of transmission coefficient of a DBRT device as a function of applied voltage in order to determine the resulting current through the device.

The details of the MBE system at Nottingham in which the layers were grown are as follows: the substrate is more or less equidistant (about 12.5cm) from all the source cell apertures and each cell is thermally isolated from its neighbour by a liquid nitrogen jacket. This arrangement also serves to minimise the degree of cross-contamination between the cells. The typical cell temperatures for the growth of GaAs in this system are maintained at: 1150 °C ± 1 °C for the gallium cell, 300 °C ± 1 °C for the arsenic and 1300 °C ± 1 °C for the silicon cell. These temperatures vary slightly depending on the degree of depletion of the source material. The substrate temperature is maintained at around 580 - 630 °C ± 1 °C and is rotated at around 20 r.p.m. to assist with the uniformity of layer growth. The thickness of the different

layers is adjusted to be a multiple of the rotation and growth rate in order to preserve layer thickness uniformity across the wafer. The overall residual doping is around $7*10^{13}$ cm^{-3} N-type [28] and is due to sulphur and silicon impurities in the arsenic source material.

Silicon doping levels up to about $1*10^{19}$ cm^{-3} are possible where the silicon occupies the donor site of gallium almost exclusively (N-type). However above this concentration, referred to as the solubility limit, there is a large degree of compensation. Above the solubility limit the silicon increasingly occupies the acceptor site of the group III (arsenic) species and no longer contributes to the current carried by the electrons. The electron mobility is also reduced, above this solubility limit, through increasing (but electrically ineffective) ionised impurity scattering. The temperature of the silicon cell in the Nottingham Varian Gen-II, required to achieve N_d-N_a of $2*10^{18}$ cm^{-3}, is ~ 1300 °C; for N_d-N_a = $2*10^{17}$ cm^{-3} it is 1190 °C and for N_d-N_a = $2*10^{16}$ cm^{-3} it is 1090 °C. To grow a typical cladding layer of 1000Å of GaAs material with N_d-N_a = $2*10^{17}$ cm^{-3} would take around 6 minutes. During this time an appreciable fraction of the grown layer thickness is required for the doping to fall from the initial value of N_d-N_a = $2*10^{18}$ cm^{-3}. The cell at this temperature (when N_d-N_a = $2*10^{18}$), would take about 3 minutes to cool from 1300°C to 1190°C, for which N_d-N_a = $2*10^{17}$. Hence, the initial 500 Å would be a transition region between N_d-N_a = $2*10^{18}$ cm^{-3} and $2*10^{17}$ cm^{-3}. This fact should be borne in mind when any modelling of the voltage distribution throughout the device is carried out; furthermore, the transition region is not necessarily symmetric on either side of the active region. Abrupt changes in doping can be achieved by using either a growth interrupt and delay (for the silicon cell to cool to the lower temperature), or by using a second silicon cell set to the lower temperature.

The gallium and aluminium flux densities are calibrated prior to growth using the technique of reflection high energy electron diffraction (RHEED) in the growth chamber. The ratio of the arsenic flux to the gallium flux is then set by measuring the partial pressures of each species using an ion-mass spectrometer and then adjusting

the arsenic cell temperature to give the required value. The dopant (Si) fluxes are too small to be measured in situ and require calibration using C-V or Hall measurements from a previous growth run. The intensity of the RHEED pattern is high when there is a large degree of atomic smoothness across the surface of the substrate, which is usually the case at the beginning of growth and also on completion of each monolayer thereafter. The growth, however, proceeds in islands and usually involves many planes at once. As the number of these simultaneous growth planes increases the overall intensity of the RHEED pattern decreases. This, then, gives some indication of the surface roughness and if the gallium cell is "shuttered" for several seconds the RHEED pattern can be seen to recover to near its starting intensity as the surface smoothness also recovers. This technique is often used to improve the interface quality when the roughness is an important parameter in the operation of devices fabricated from such layers.

Another important point to note when growing, and indeed modelling, the thinner layers is that the initial flux density immediately upon opening the shutter of a cell, which has been closed for some time, may be as much as 20% greater than when the shutter has been open for some hundreds of seconds, Clinton et al [14]. In the case of aluminium for a steady-state flux at a certain temperature, a recommended adjustment would be to initially open the shutter at 10°C below the set-point, or to open the shutter for a slightly shorter time than would otherwise be calculated for the required thickness. The exact times and temperatures for this operation are arrived at empirically. The effect of this flux transient may result in the barriers being one or two monolayers thicker than planned due to, in the case of AlAs, an excess of aluminium being deposited on the wafer when the shutter is just opened. In the case of a fractional amount of aluminium in the barrier the flux transient may increase the fraction of the aluminium in $Al_xGa_{1-x}As$ and subsequently the barrier height rather than the width. Hence, for modelling purposes, the calculated barrier height and thickness may need to be adjusted to achieve a reasonable fit between the modelled and experimental currents.

The importance of reducing contact resistances will be discussed later. In the future it may be possible to exploit MBE growth techniques directly to reduce contact resistances [4,6]. A brief discussion of two possible methods will now be given.

It is possible to grow a capping layer of Indium Arsenide on GaAs despite its having quite a different lattice spacing (δ = 7E-2, where $\delta = (a_{epi} - a_{subs})/a_{subs}$ and should not exceed $\pm 3*10^{-4}$ for good epitaxial growth). The resultant morphology is smooth but the electrical and optical properties of the layer are much poorer than those of bulk InAs. Nevertheless, it should be possible to use such a system to improve the contact resistance.

The use of heavily doped ($10^{19}cm^{-3}$ grown at low temperature ~200°C) and delta-doped surface layers is presently under investigation at Nottingham for fabrication of unalloyed (requires slight alloying in the case of $10^{19}cm^{-3}$ material) contacts to GaAs. This delta-doping process is where the growth of the final layers of GaAs are interrupted by closing the shutter of the gallium cell and opening the silicon shutter. This allows the deposition of a large quantity of silicon interstitially (to an areal density of $2\text{-}3*10^{13}$ cm^{-3}), resulting in an electron density of approximately $1*10^{19}$ cm^{-3} at the surface. The layer growth is then continued by closing the silicon shutter and opening the gallium shutter once more. The process is repeated several times and the number of monolayers of GaAs grown between the silicon delta doped regions determine the position of the resulting Fermi level. This technique is used to reduce the barrier between the bulk GaAs and the metal contact layers and is preferable to the normal means of forming highly doped surface layers if annealing is to be avoided. This is because at the high growth temperature of the layers studied in this thesis (580°C), lesser amounts of silicon will be incorporated in the GaAs than the ideal value (which is approximately $1*10^{19}$ cm^{-3}). The reason for this reduction in silicon content is because thermodynamic competition between the silicon and gallium atoms during their simultaneous deposition favours gallium. The delta-doping process avoids these problems and permits high levels of doping at the surface.

2.2.1 A summary of the layers grown for the project

The following table summarises the layers grown for the project and the purpose of the differing growth requirements. Also shown are the primary reason for which these layers were grown:

LAYER I/D	SUBSTRATE	CATEGORY	COMMENTS (PRIMARILY GROWN FOR:)
Group 1: to establish contact procedures			
452	SI	2 10^{18} cm^{-3} GaAs	Used for TLM contact tests
Group 2: primarily grown/used for modelling studies			
195	N^+	DBRT: 56Å, 40% barriers, 50Å well, 25Å ud. spacers, 500Å 2 x 10^{18} cm^{-3} GaAs cladding layer	For impedance and modelling studies. Oscillation in waveguide at X band studied in early experiments.
453	N^+	DBRT: Asymmetric height barriers, 51Å well, 42Å bottom barrier width 40% $Al_xGa_{1-x}As$, 40Å AlAs top barrier, 51Å ud. spacers, 1000Å 1 x 10^{17} cm^{-3} cladding layers	To investigate asymmetric barriers in models, contributing to possible inductive and charge storage effects.
454	N^+	As for 453 but asymmetric barrier positions swapped	As above, but with asymmetry in other sense.
455	N^+	DBRT: symmetric control differing from 453 and 454 only by symmetric barriers of 42Å 40% $Al_xGa_{1-x}As$	Symmetric structure; control for 453 and 454.
469	N^+	DBRT: as 455, but with extra drift region of 1000Å of 2 x 10^{16} cm^{-3} on bottom collector contact	Asymmetric doping. Used to investigate QWITT behaviour. Strong oscillator o/p in microstrip, also used for self oscillating mixer studies at X-band.
606	N^+	DBRT: as 469 but 3000Å of drift region instead of 1000Å	Longer drift region (3000Å) than in 469 (1000Å). Not yet studied but should improve on power performance.

LAYER I/D	SUBSTRATE	CATEGORY	COMMENTS (PRIMARILY GROWN FOR:)
Group 3: primarily grown for oscillators and mixers			
298	N^+	17Å AlAs barriers, 43Å well, no ud. spacers, 4000Å 2 x 10^{17} cm^{-3} cladding layers	Oscillator output at 85 GHz. Grown as a repeat of Sollner's structure to confirm that we could grow AlAs barriers and dope right up to the barriers.
366	N^+	As 298, but 1500Å, 5 x 10^{16} cm^{-3} drift region	SOM and oscillator behaviour at 85 GHz.
367	N^+	As 366, but symmetric 1500Å, 2 x 10^{17} cm^{-3} drift regions	Multiplier structure, symmetry favours second harmonic supression should peform well at W-band. Devices awaiting tests.
552	N^+	As 366, but 3000Å drift region	Processing not yet completed. Power yield should exceed that of 366 although the transit time delay may be excessive.
418	N^+	As 298, but 12Å AlAs barriers 34Å Well 17Å ud. spacers and 1000Å, 7 x 10^{15} cm^{-3} drift region	Attempt to "improve" on 366 like structure. No NDR observed down to 77K.
Group 4: primarily grown for detector studies			
234	N^+	Superlattice/barrier structure with 38Å thick middle barrier	Three period superlattice where most of the field should be droped across the middle barrier. Growth tests and early detector studies.
365	N^+	As 234, but different SL period	No NDR.
368	N^+	Repeat of 234	10 GHz detector studies attempted. Seemed to be compromised by excessive capacitance
207	N^+	57Å AlGaAs barriers, 1200Å well	PART studies.
167	N^+	As 207, but 600Å well	PART studies.

LAYER I/D	SUBSTRATE	CATEGORY	COMMENTS (PRIMARILY GROWN FOR:)
Group 5: primarily grown for 3 terminal devices			
610	SI	DBRT based on 455 + FET	Gateable SOM and oscillator application, device impedance should be tunable and so could potentially optimise output power. Likewise SOM frequency may be tunable.
614	SI	DBRT + FET	Gateable SOM and oscillator application, growth repeat of above layer.
636	SI	DBRT based on 455 + VARACTOR	Gateable SOM and oscillation application but tuning should be possible via. a reactance and should not degrade performance unlike FET.
Group 6: miscellaneous			
456	N+	As 298	Grown to assess repeatability of growth on device modelling and DLTS study.
457	N+	As 456, but lower growth temperature	Grown to assess growth temperature effects on possible deep traps. DLTS studies planned in parallel with device modelling.
462	N+	As 456, but with extra spacer layers adjacent to barriers	Grown to assess diffusion effects during growth and implication on RF behaviour

Table 2.1 Summary of wafers grown and their proposed purpose use

Figures 2.1-2.9 show a comparison of some of the current-voltage characteristics which have been recorded during the course of the study for this Thesis and result from the differences in the layer structure as detailed in Table 2.1 and described in Chapter 3.

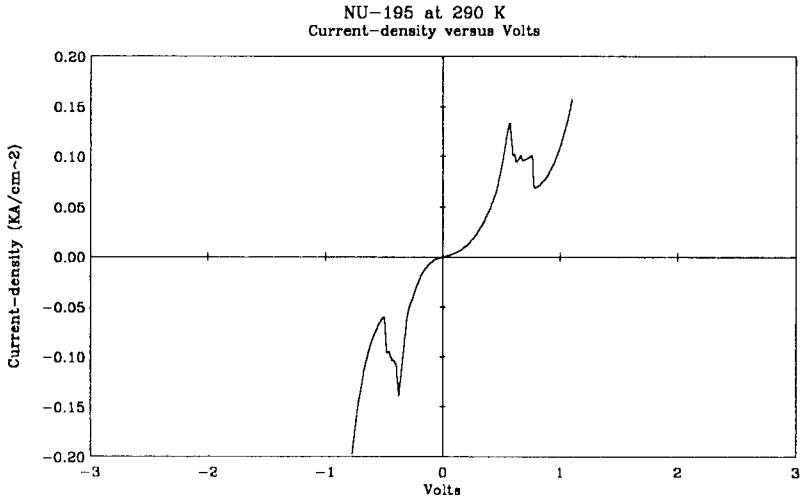


Figure 2.1 (a)

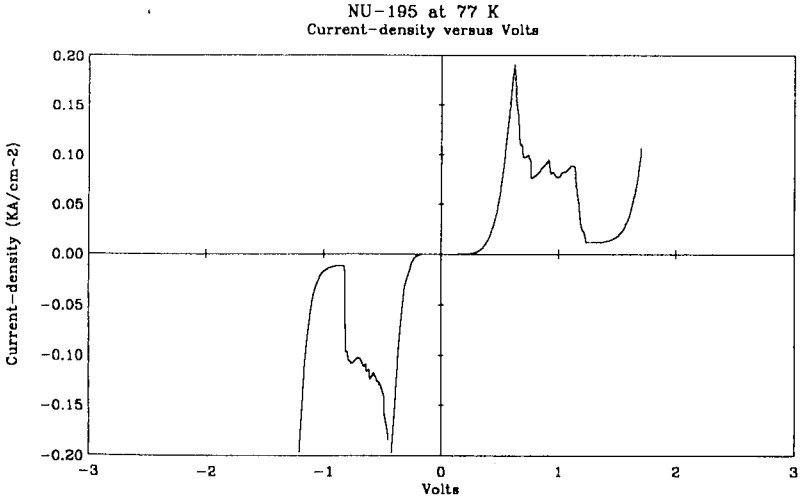


Figure 2.1 (b)

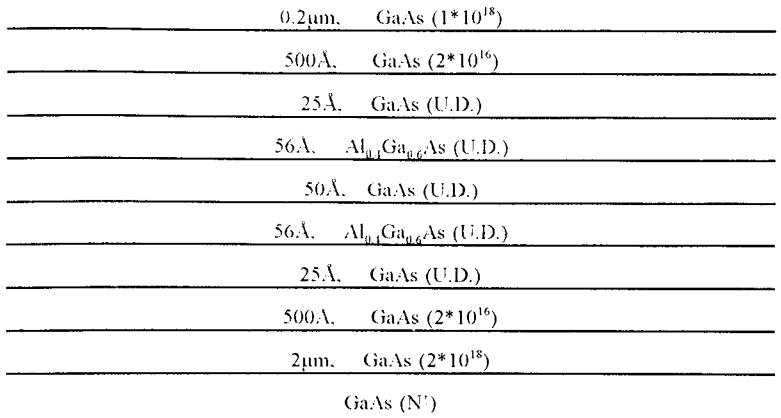


Figure 2.1 (c) Layer structure for NU-195

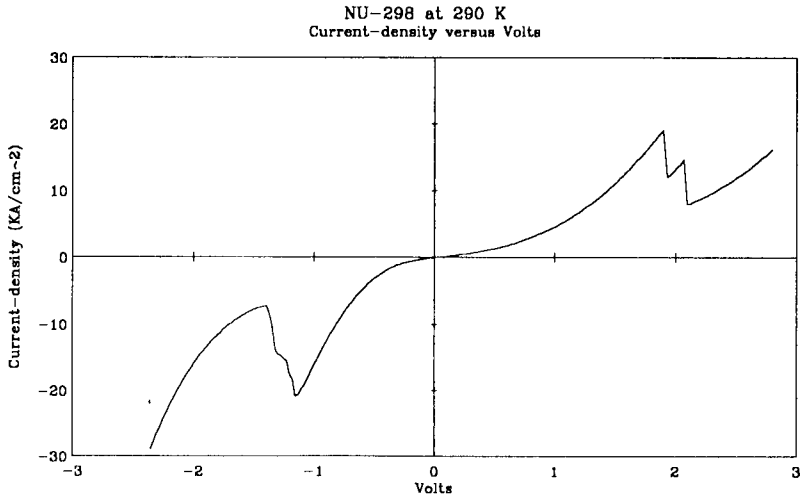


Figure 2.2 (a)

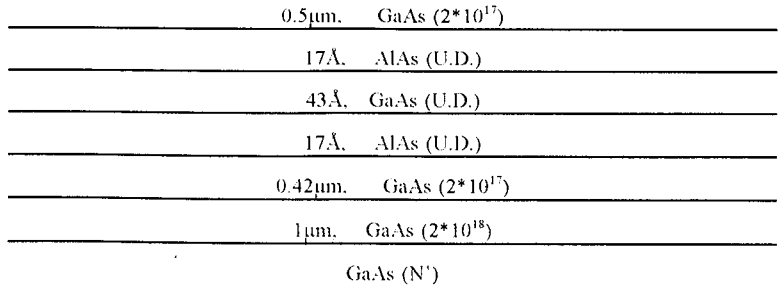


Figure 2.2 (b) Layer structure for NU-298

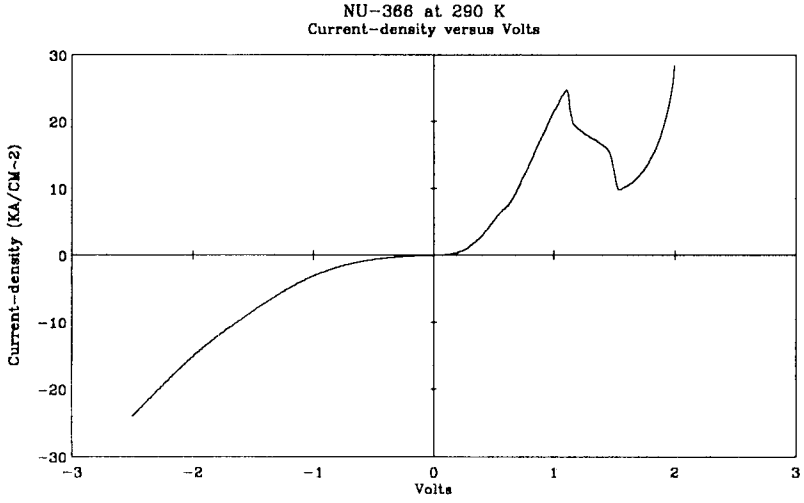


Figure 2.3 (a)

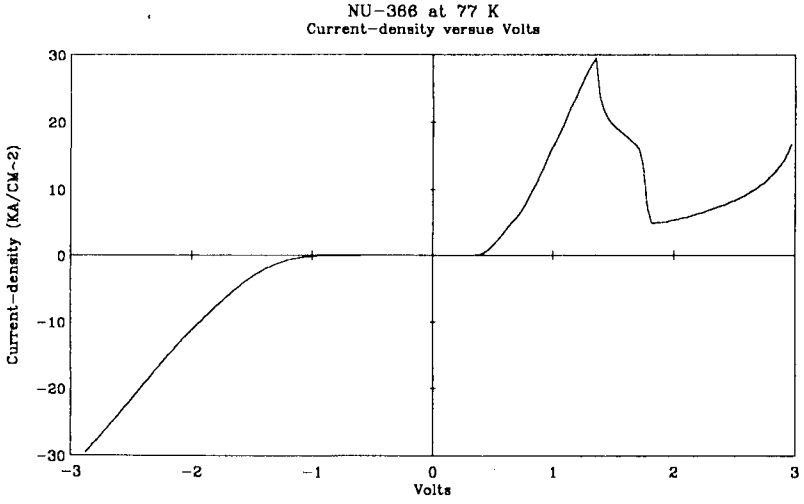


Figure 2.3 (b)

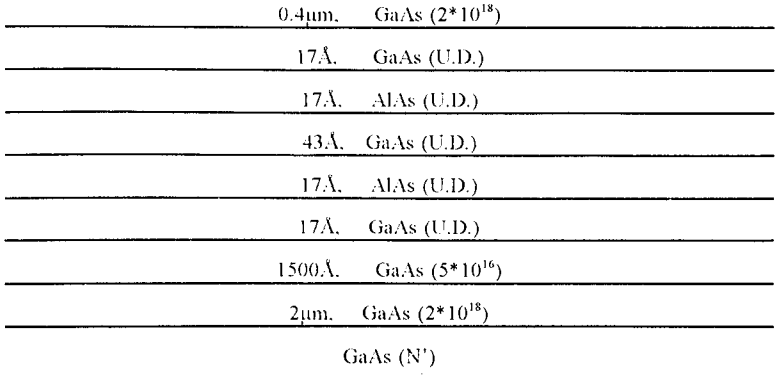


Figure 2.3 (c) Layer structure for NU-366

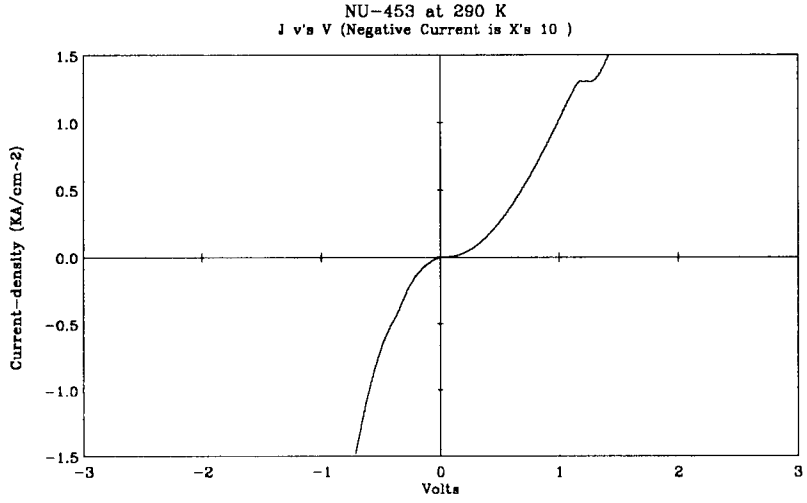


Figure 2.4 (a)

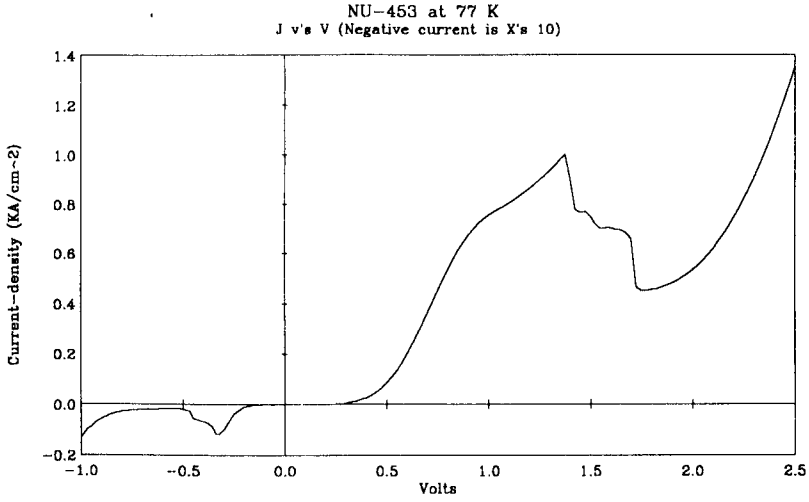


Figure 2.4 (b)

0.5μm. GaAs ($1*10^{18}$)
0.1μm. GaAs ($1*10^{17}$)
51Å. GaAs (U.D.)
40Å. AlAs (U.D.)
51Å. GaAs (U.D.)
43Å. $Al_{0.4}Ga_{0.6}As$ (U.D.)
51Å. GaAs (U.D.)
0.1μm. GaAs ($1*10^{17}$)
2μm. GaAs ($1*10^{18}$)
GaAs (N^+)

Figure 2.4 (c) Layer structure for NU-453

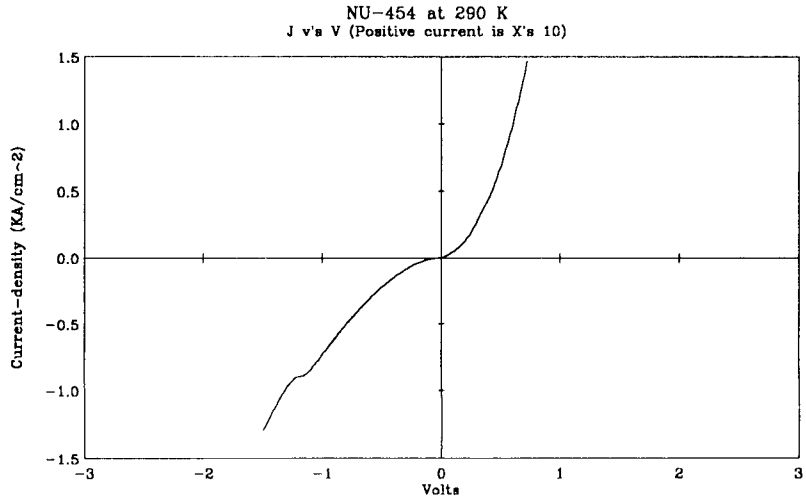


Figure 2.5 (a)

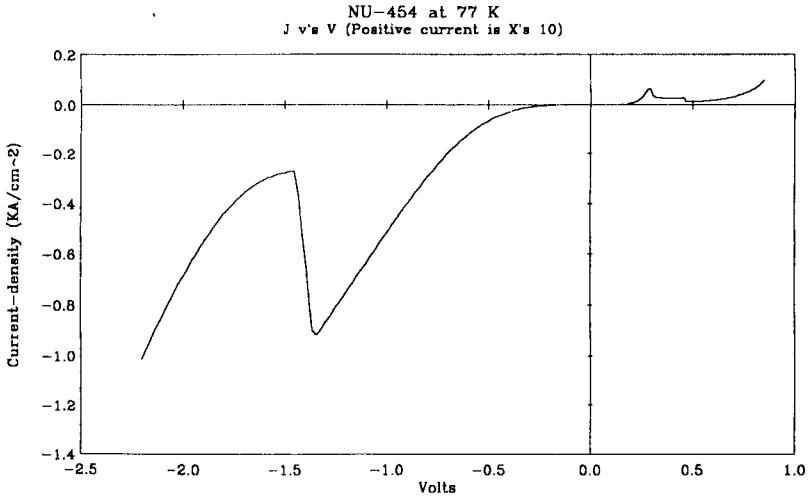


Figure 2.5 (b)

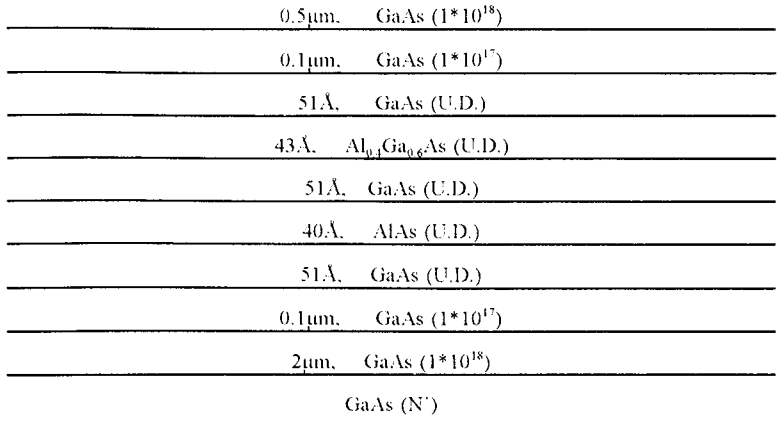


Figure 2.5 (c) Layer structure for NU-454

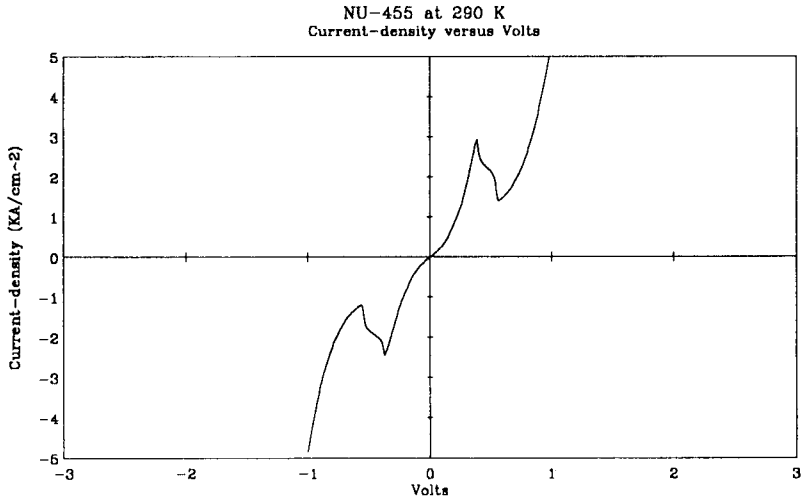


Figure 2.6 (a)

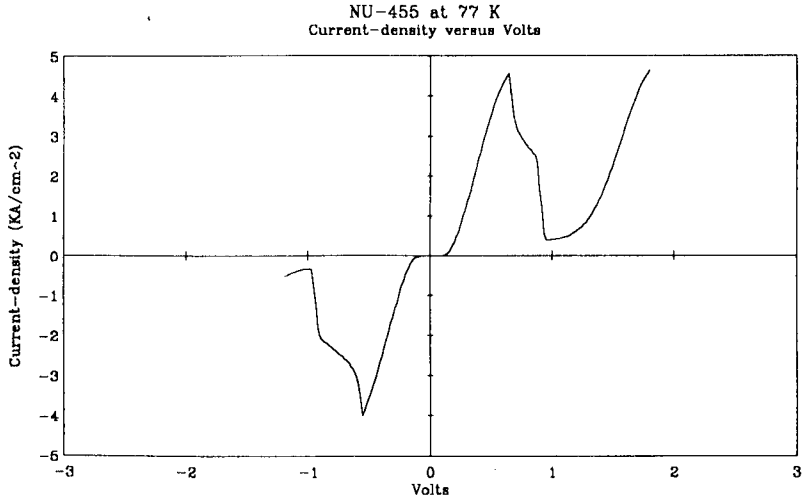


Figure 2.6 (b)

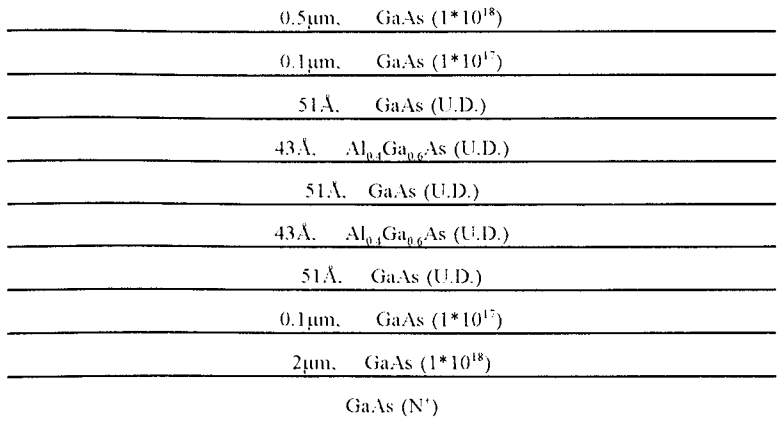


Figure 2.6 (c) Layer structure for NU-455

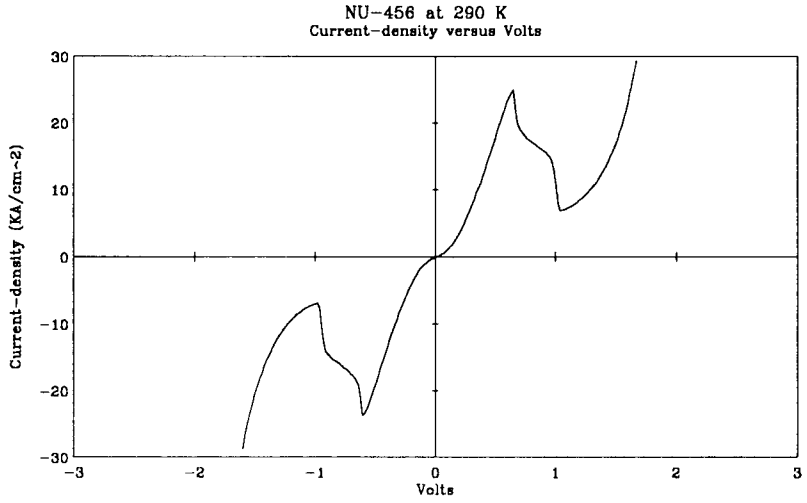


Figure 2.7 (a)

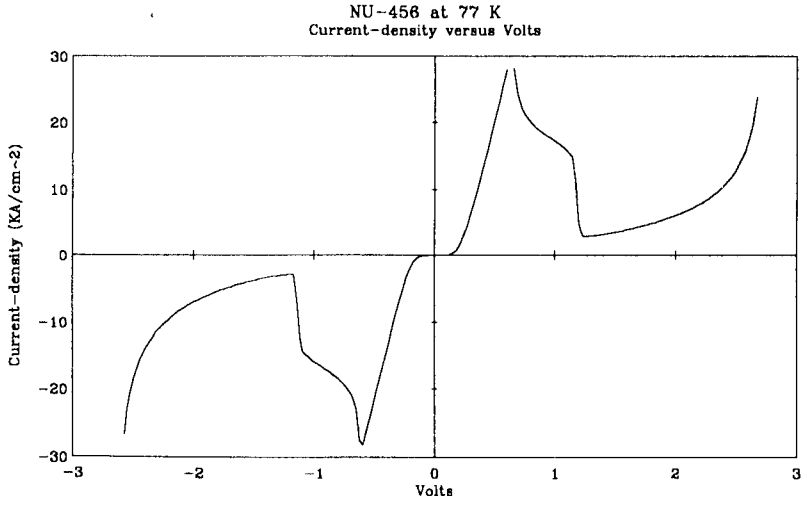


Figure 2.7 (b)

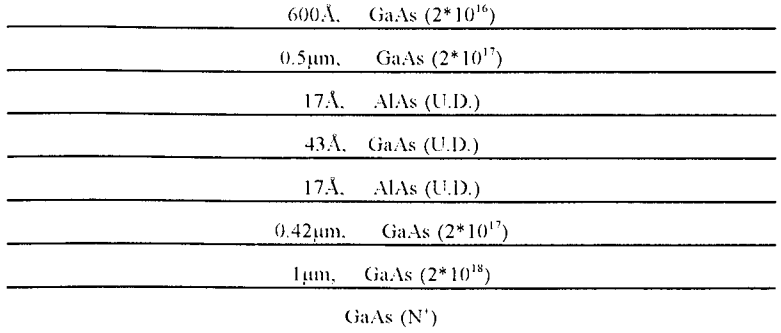


Figure 2.7 (c) Layer structure for NU-456 (similar to NU-298 but grown at 630°C)

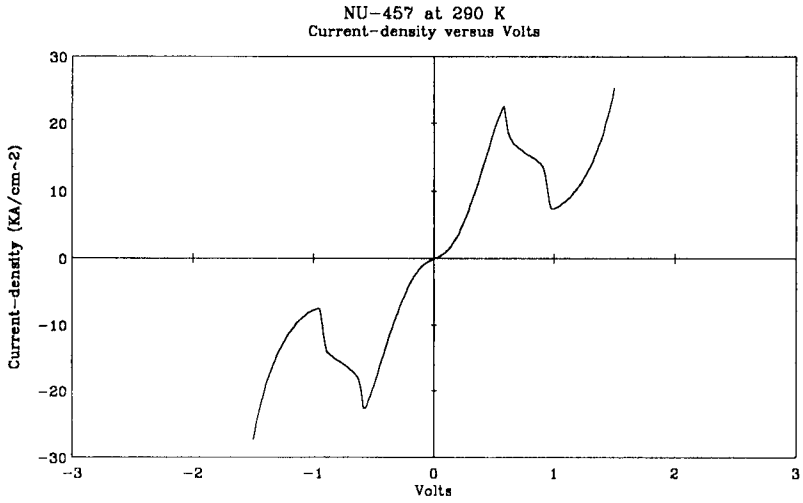


Figure 2.8 (a)

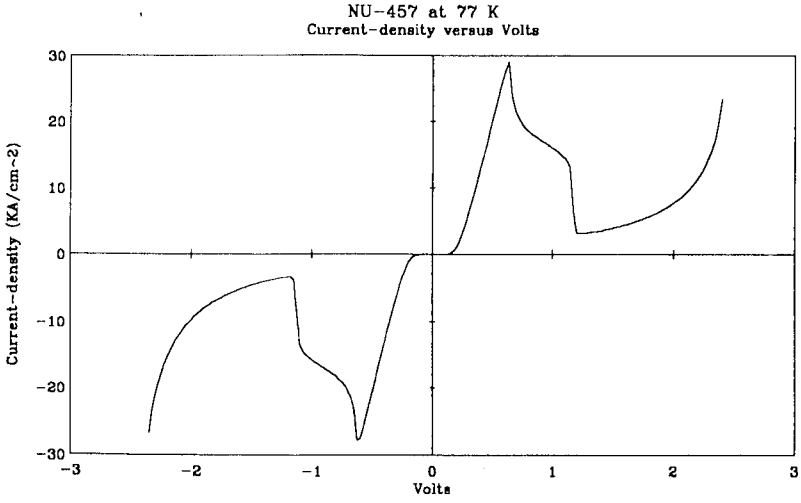


Figure 2.8 (b)

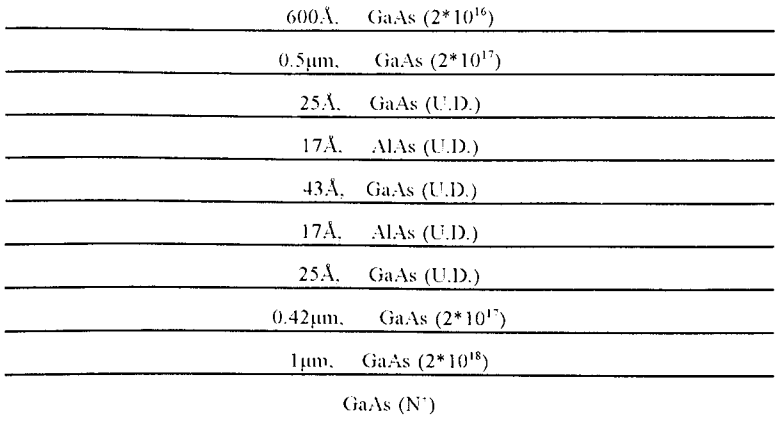


Figure 2.8 (c) Layer structure for NU-457 (as NU-456 but with 25Å spacer layers)

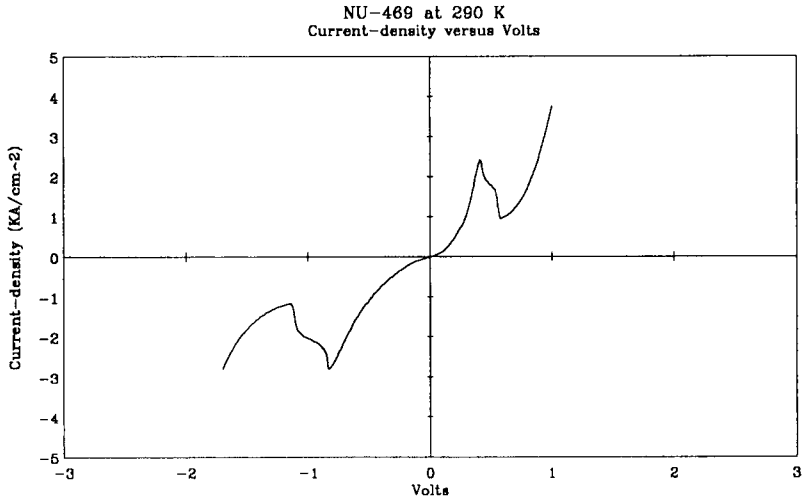


Figure 2.9 (a)

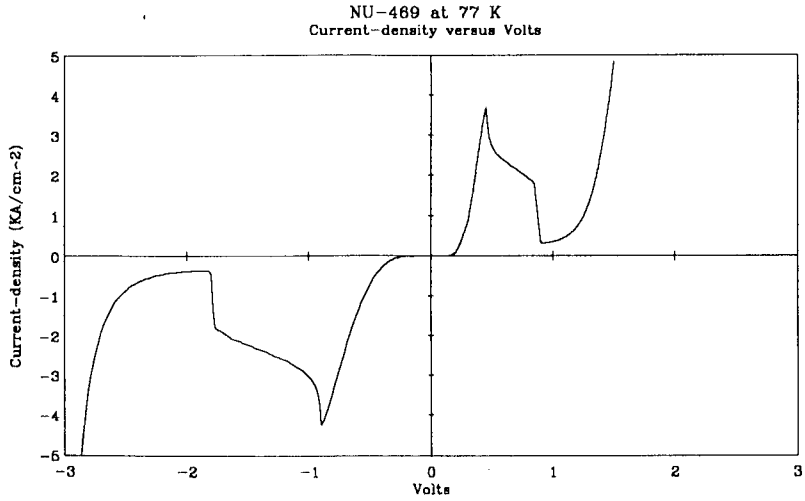


Figure 2.9 (b)

0.5μm. GaAs ($1*10^{18}$)
0.1μm. GaAs ($1*10^{17}$)
51Å. GaAs (U.D.)
43Å. $Al_{0.4}Ga_{0.6}As$ (U.D.)
51Å. GaAs (U.D.)
43Å. $Al_{0.4}Ga_{0.6}As$ (U.D.)
51Å. GaAs (U.D.)
0.1μm. GaAs ($2*10^{16}$)
0.1μm. GaAs ($1*10^{17}$)
2μm. GaAs ($1*10^{18}$)
GaAs (N^+)

Figure 2.9 (c) Layer structure for NU-469

2.3 Contact resistance and its contribution to device performance

One of the most important factors which determine the ultimate performance of most two terminal semiconductor devices is the resistance of the contact between the "outside world" and the conducting layers of the semiconductor. Often as in (three terminal) Field Effect Transistors (FET's), these contacting interfaces can involve quite large areas, hence minimising this contact resistance. This is possible in FET's because the ultimate performance is more usually dependent on the gate-contact characteristics. However, in two terminal devices, which are required to have large current-handling capability, the contact resistance is of primary importance. In such devices the luxury of having large areas to minimise the resistance is often precluded by the associated parallel-plate capacitance of the active region which (if large) would act to shunt any high frequency signals around this active region.

The standard "model" of the formation of low resistance "Ohmic" contacts to N-type GaAs is discussed in the paper by R.P. Gupta and W.S. Khokle [3]; these workers use a metallisation similar to that used for the contacts reported in this thesis. Other parametric studies have been carried out [23], where the concentration of germanium was varied and the resultant changes in morphology and resistance were noted. The Ohmic contact is formed by depositing a suitable combination of "contact" metal layers on the wafer and "annealing" to form an alloy with the underlying GaAs material. During the annealing process, the gallium atoms from the GaAs diffuse into the top metallisation layers leaving vacancies in the semiconductor. Germanium atoms in the contact metallisation in turn diffuse into the vacated gallium sites which then behave electrically as donors. The process of this substitution reaction is correctly referred to as the formation of a Frenkel defect [3]. When alloying takes place above the eutectic temperature of AuGe (356°C for eutectic mixtures of AuGe (12% Ge)), gallium diffuses to the boundaries of the gold grains forming a AuGa layer at the

interface. Under the same conditions germanium diffuses into the semiconductor and is incorporated onto lattice sites, forming donors. Arsenic loss during the alloying process is not substantial at temperatures up to the optimum alloying temperature (400-450°C) and for the short times involved. In consequence the net result is N-type doping. Higher alloying temperatures increase the amount of gallium dissolution and accompanying germanium in-diffusion, thus increasing the donor concentration at the interface. This process ceases when there is a sufficiently high concentration of gallium in the gold of the contact metal to saturate it, thereby inhibiting further out-diffusion from the semiconductor. Although increasing the temperature will allow further germanium in-diffusion to occur an increasing degree of arsenic dissociation also increases the number of acceptors. As a result, there is an optimum temperature for maximising N_d - N_a at the interface between the semiconductor and the contact metal. Beyond this optimum point the contact resistance will again be degraded. Gupta and Khokle's model [3] suggests that the doping achieved at the junction of the AuGeNi to N-Type interface is in the region of $5*10^{18}/cm^3$ and that the resultant barrier height is in the region of 0.4eV.

The grain size of the gold in the contact metallisation is a very important parameter for achieving optimum contact resistance especially for very small contacts. In the present study this was not investigated, but it is noted that a preferred value, according to Gupta and Khokle [3], would be a grain size of 1000Å. The presence of AuGe and NiAs(Ge) crystallites has been detected [23] and it is thought that these crystallites play an important part in the mechanism of contact conduction. These germanium-rich spikes protrude deeply into the GaAs and the overall resistance of the contact is dominated by the spreading resistance of these spikes [29], which in turn limit the size of the device, if a uniform resistance is to be achieved. It should be possible that, if necessary, this parameter could be controlled by adjusting the temperature of the substrate during deposition of the contact metallisation or alternatively by optimisation of the slice-to-source separation which acts to adjust the temperature of the evaporant as it solidifies on the semiconductor surface.

Following the findings of Gupta and Khokle [3] with regard to an optimum alloying temperature, a temperature of 400-450°C was chosen for the present study, with alloying times of around 20-30 seconds. A tubular furnace was mostly used for alloying although some initial experiments were carried out using a hot-plate method [32]. A brief description of the alloying and the alternative methods of alloying will now be given:

(i) Tubular furnace method.

The furnace temperature was set at 750°C with a 10% H_2 in argon, reducing atmosphere. A low thermal mass paddle was used which also incorporated a thermocouple on its underside to indicate the temperature reached. The paddle was inserted after allowing the gas flow to stabilize (typically after 5 minutes) and after purging all of the oxygen from the system. The paddle on which the substrate was placed was withdrawn when the appropriate temperature was reached, allowing 20-30°C of overshoot. Usually this occurred when the temperature reached 380°C and the time spent above 350°C was recorded. This control was limited but was deemed sufficient and was repeatable enough for our present purposes. This is demonstrated by subsequent evaluations of the contact resistance, which were performed using the Transmission line method (TLM) of Reeves et al [8].

(II) Hot-plate method.

The hot-plate method involves placing a hot-plate in a dry-box which is again purged with a reducing gas mixture. The wafer to be alloyed is then introduced via a load-lock after a suitable waiting time. The slice is placed on the hot-plate, using gloves and tweezers. The hot-plate temperature is typically 430-470°C and the slice is removed from the hot-plate after 20-30 seconds. This method has proven satisfactory for annealing contacts to Field Effect Transistors. However, permanently purging the dry-box with the "forming" gas

proved expensive, and residual oxygen (which degraded the contacts) was present in the system without such purging and as a result, the furnace method was chosen in preference to the hot-plate method of alloying.

The ideal technique for alloying, in terms of both control and repeatability is undoubtedly the rapid thermal anneal (RTA) system. This is due mainly to the control of the ramp-up and more importantly ramp-down rates and the shorter durations above the alloying threshold which are possible using this technique. Unfortunately an RTA system was not at our disposal at Nottingham but would be the ideal method for characterisation and optimisation of the alloying conditions for our chosen metallisation procedure.

The contact metallisation aimed for in the present study was: 100Å-Ni, 700Å-AuGe, 1000Å-Ni, 1500-2000Å-Au. The (1000Å) nickel inter-diffusion layer was later replaced by titanium to try to improve the surface morphology. Titanium was considered a better barrier to the out-diffusion of the germanium towards the top gold contact rather than inwards toward the GaAs (in previous work on other systems, it had been found that excess gold tends to preferentially getter any germanium in its vicinity). The apparent contact resistance of the actual devices was not degraded as a result of this change in metallisation (from nickel to titanium) although rigorous contact trials using the TLM approach were not conducted, mainly because of the time required for such trials. The surface morphology of the contacts formed with titanium (and subsequently alloyed) did seem to be an improvement over those made using the previous nickel inter-diffusion layer. This was of importance because only the ohmic contact was used for the dry-etching mask and thus complete metal coverage was vital. The presence of pin-holes (where there was no metal) would permit etching through the contact and perhaps damage to the active region. As a future improvement, introduction of a nickel layer (say 500Å thick) between the titanium and the gold may be advantageous. This layer would help harden the top metal and, as a result, improve the bonding characteristics. It is thought that after alloying, this nickel would to some extent inter-diffuse throughout the top gold contact thereby increasing the strength of

subsequent bonds made to this material. There remains a need to improve the bonding technique to the 20μm diameter DBRT devices and such a procedure, if successful, would be of value.

The degree of control of the evaporated thicknesses of the thin nickel and the AuGe achieved in this study and shown in Table 2.2, is limited. This is because in the case of AuGe the two materials have different vapour pressures, and therefore do not evaporate simultaneously at the same rate. As a result the AuGe must be evaporated to completion, and the use of shuttering to control the resultant thickness is not recommended. Separate evaporation of the gold and germanium to produce the AuGe layer may improve the degree of control by allowing the ratio of these materials to be varied to achieve an optimum resistance. This was not possible in the present study because of a limitation in the number of separate sources (4-hearths) therefore a commercial eutectic mixture of AuGe was used.

A summary of the results from the contact resistance trials is seen on Table 2.2; the metallisation used throughout was 40Å-Ni, 520Å-AuGe, 385Å-Ni, 1820Å-Au.

The following table describes the results of contact resistance measurements which were carried out on test material in order to evaluate the contacting process. This was to be used to provide process control information for later use on DBRT devices.

NU-106 Alloyed in Nottingham Tube Furnace				
	Removed @ 350°C Max. T° 403°C	Removed @ 370°C Max. T° 418°C	Removed @ 400°C Max. T° 441°C	
Area 1	L_T = 1.4 µm R_{SH} = 127 Ω/□ ρ_C = 2.7E-6 Ωcm²	L_T = 2.0 µm R_{SH} = 128 Ω/□ ρ_C = 5.3E-6 Ωcm²	L_T = 1.0 µm R_{SH} = 128 Ω/□ ρ_C = 1.3E-6 Ωcm²	
Area 2	Not calculated, between 1 & 3	L_T = 1.17 µm R_{SH} = 116 Ω/□ ρ_C = 1.6E-6 Ωcm²	L_T = 1.2 µm R_{SH} = 130 Ω/□ ρ_C = 1.8E-6 Ωcm²	
Area 3	L_T = 2.1 µm R_{SH} = 146 Ω/□ ρ_C = 6.5E-6 Ωcm²	L_T = 1.9 µm R_{SH} = 137 Ω/□ ρ_C = 5.0E-6 Ωcm²	Not calculated, between 1 & 2	
Samples alloyed at Philips Components on Hot-Plate				
	Alloyed @ 380°C Duration 20 Sec.	Alloyed @ 400°C Duration 10 Sec.	Alloyed @ 400°C Duration 20 Sec.	Alloyed @ 420°C Duration 20 Sec.
Area 1	Not calculated, between 2 & 3	Not calculated, between 2 & 3	Not calculated, between 2 & 3	L_T = 1.6 µm R_{SH} = 85 Ω/□ ρ_C = 2E-6 Ωcm²
Area 2	L_T = 6.3 µm R_{SH} = 77.2 Ω/□ ρ_C = 3.1E-5 Ωcm²	L_T = 3.0 µm R_{SH} = 82 Ω/□ ρ_C = 7.6E-6 Ωcm²	L_T = 8.0 µm R_{SH} = 61 Ω/□ ρ_C = 3.9E-5 Ωcm²	L_T = 2.1 µm R_{SH} = 82.6 Ω/□ ρ_C = 3.6E-6Ωcm²
Area 3	L_T = 6.3 µm R_{SH} = 74.6 Ω/□ ρ_C = 2.9E-5 Ωcm²	L_T = 3.4 µm R_{SH} = 81 Ω/□ ρ_C = 9.7E-6 Ωcm²	L_T = 4.3 µm R_{SH} = 80.8 Ω/□ ρ_C = 1.5E-5 Ωcm²	L_T = 1.8 µm R_{SH} = 85 Ω/□ ρ_C = 2.7E-6Ωcm²

Table 2.2 Comparison of alternative alloying methods and temperatures. The Symbols used to characterise the resistance of the contact, were as follows: L_T refers to the transfer length (µm), R_{SH} describes the sheet resistance of the surface layers outside the contact and is measured in Ω per square (the resistance of an arbitrary sized square of the material). ρ_C is the contact resistivity (Ωcm²) and provides a good indication of the quality of the contact between the contact and the "outside-world".

As a comment on Table 2.2 , it should be noted that the samples alloyed at Nottingham displayed poor morphology when the alloying temperature was 400°C (maximum temperature reached = 440°C). The lower temperature of 370°C was chosen for withdrawal, which still gave acceptable contact resistance but with improved morphology. The hot-plate method tends to result in better morphology but this has not been investigated fully. Although higher alloying temperatures are also suggested from this initial study together with shorter alloying times, these possibilities were not fully explored since trials using the furnace method gave satisfactory results. Differing values of sheet resistance were observed between the samples alloyed using the hot-plate and the tube furnace. The reason for this is at present unclear. However, the implied higher doping of the samples processed using the hot-plate should improve the contact resistance (R_{SH}), although from Table 2.2 this can not be seen to be significantly different from those samples processed using the tube furnace.

It is worth mentioning again at this point that there are device-size limitations on the control of contact resistance. In most devices this is not a problem, although for future work on smaller devices than those used for this study, this fact may need to be considered. As mentioned previously, and according to Gueret et al [9], the grain size effects can pose a problem when they become an appreciable fraction of the contact size. These workers found that for contacts of 2μm or less in side (ie. equating to ~2μm in diameter or less) there was an unexpected spread in contact resistances between similar sized contacts. This was attributed to variation in the granular structure of the alloyed interface. Since, if such small contacts were necessary, it would be a difficult task to characterise and control this problem then careful consideration should be given to minimising these possible effects. Alternatively, preparations should be made to select the best devices for the required application. See also section 2.7 for possible alternatives to help improve this situation.

2.3.1 Other resistive contributions

Table 2.3 shows the contributions to the total calculated resistance as a function of device area. The contributions are: the specific contact resistance, and the resistance of a typical low-doped epitaxial cladding layer. The total parasitic device resistance is simply the sum of these two contributions. The resistance of the cladding layer is calculated using the following formula:

$$R=\frac{L}{N_d.q.\mu.A} \tag{2.2}$$

where: N_d = doping in the layer, μ = mobility of carriers in layer (μ ~5000$cm^2V^{-1}S^{-1}$ for $N_d=1*10^{17}$ cm^{-3} and μ ~6000 $cm^2V^{-1}S^{-1}$ for $1*10^{16}$ cm^{-3}), A = area of the device and L = length of the layer.

Dev. diameter (μm)	1	2	5	10	20	50
	Resistance Ω					
$R_{cont.}$ if ρ_C=2E-6Ωcm²	255	64	10	2.5	0.64	0.1
$R_{cont.}$ if ρ_C=2E-7Ωcm²	25.5	6.4	1.0	0.25	0.064	0.01
Cladding layer 1000 Å of $1*10^{17}$ cm^{-3}	13.2	3.3	0.5	0.1	0.03	0.005

Table 2.3 Resistance contributions due to the contact resistivity versus the device diameter and compared to the resistance contribution due to the low-doped "drift" region.

From Table 2.3 it can be seen that the dominant resistance of the smaller devices is due to the contacts, even with idyllic values for the specific contact resistance in the mid 10^{-7} Ωcm^2 (which represents very good contacts). Note also the not insignificant

contribution of the cladding layers, which (if undepleted) represent an unnecessary excess resistance in series with the device. This is especially true for the case of $1*10^{16}$ cm^{-3} doped cladding layers where the resistances would be an order of magnitude greater than those shown above.

2.3.2 Frequency dependent resistances

Dickens [10] considered the frequency dependence of the series resistance of a point contact diode. He showed that a significant correction to R_s (the series resistance) need only be made when the frequency is much greater than 100GHz. This is however, only true when we consider the immediate vicinity of the contact and is not necessarily true when the RF path length to ground is large as for the devices used in this Thesis. DeLoach [11] also considered this problem and his analysis may be applied to a simplified representation of the DBRT's used in the present study.

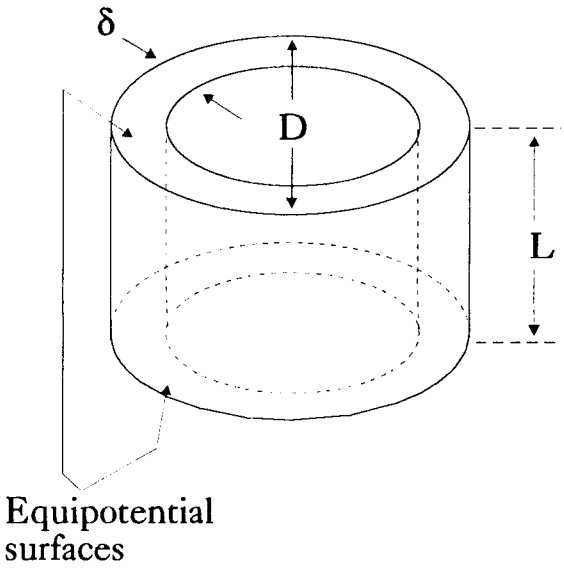


Figure 2.10 (a) Representation of the high frequency path to ground due to the side-walls of the chip.

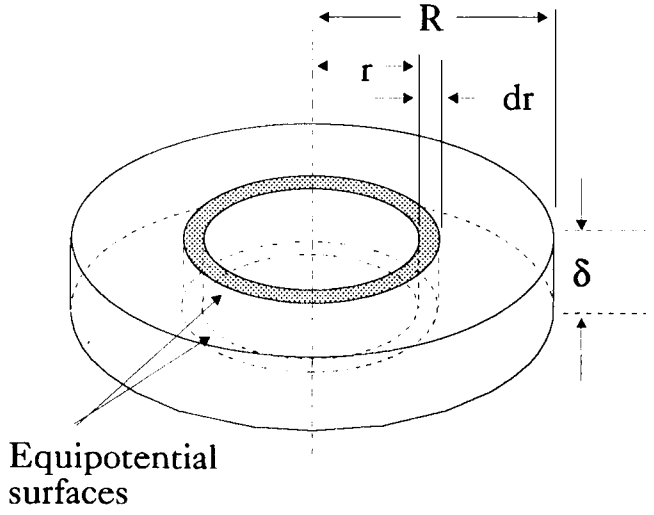


Figure 2.10 (b) Representation of the high frequency current path along the surface of the chip.

with reference to Figure 2.10(a), and making the mathematical simplification of using a radius of 160 μm to represent a 250 μm in-side chip, the resistance of a cylinder of thickness δ, where δ is the "skin depth" may be written as :

$$R_{sk}=\frac{\rho L}{\pi\delta(D-\delta)} \tag{2.2}$$

where D is the diameter of the cylinder, L is its length and ρ the d.c. resistivity. The skin depth is given by:

$$\delta=\frac{1}{\sqrt{F\pi\mu_0\sigma}} \tag{2.3}$$

where F is the frequency, and σ is the conductivity of the surface and side-walls.

For example, for a substrate doping of $2*10^{18}$ cm^{-3} the characteristic frequency-dependent skin depths are (Equation 2.3): 63μm, 18μm and 6.3μm for 1GHz, 12GHz and 100GHz respectively. Equation 2.2 represents the side-wall resistance and results in extra frequency-dependent resistive contributions of the chip side-walls alone of: 0.081Ω, 0.195Ω and 0.514Ω for 1Ghz, 12GHz and 100GHz respectively (this calculation assumes D = 320μm which is appropriate for a 250μm chip) .

If we now consider frequency dependent resistance of the thin disc of semiconducting material which carries the high frequency current along the surface of the chip (shown in Figure 2.10 (b)):

$$R_{disc}=\frac{\rho}{2\pi\delta}[Ln\frac{b}{a}] \tag{2.4}$$

where ρ is the resistivity of the substrate, δ is the "Skin-depth" and b and a are the respective outer and inner radii of the disc.

Using Equation 2.4, the extra frequency dependent resistive contributions due to

conduction through this thin disc of material to the edge of the chip are:-

For a 20μm diameter device: 0.11Ω, 0.38Ω and 1.1Ω for 1GHz, 12GHz and 100GHz respectively. For a 5μm dia. device: 0.16Ω, 0.57Ω and 1.64Ω for 1GHz, 12GHz and 100GHz respectively.

The sum of the resistances of the side-walls and the thin disc of conducting surface device material is the total frequency dependent resistance to ground from the device mesa bottom contact. For a 5μm dia. device this resistance is modest (0.8Ω at 12GHz), although this figure represents a (frequency-dependent) increase in resistance of some 0.6Ω from 1GHz to 12GHz. At 100GHz these frequency-dependent contributions exceed 2 Ohms, becoming a significant part of the overall contact resistance in the case of the 5μm dia. device.

From the above example it can be seen that for optimum performance at and beyond 100 GHz the device geometry, with respect to the contacts and current path lengths, needs to be considered carefully. An alternative method for alleviating these frequency-dependent resistances is to use a co-planar device layout (see Figure 2.12). Finally note that this frequency-dependent resistance will appear (in an equivalent circuit model) between the collector contact and ground of the DBRT and should, as a result, produce a frequency-dependent voltage shift of the differential resistance. This frequency-dependent voltage shift of the differential resistance was not obvious for the measurements discussed in Chapter 4 but may be noticeable if the measurements were carried out at 100GHz.

2.4 Device layout and mask design

The mask-set was designed for exclusive use on the N^+ substrates, since all of the high-frequency applications previously reported elsewhere, up to this moment in time, used devices made from such material in conjunction with either bonded or whiskered contacts. This previous work looked promising and it was thought that we should initially try to duplicate these results before attempting to extend the work to higher frequencies or to other areas which required different layer structures and device designs.

To cover all foreseeable requirements a wide selection of device sizes was incorporated on one mask-set. The individual chip size was limited by the possible packages to be used. Since devices operating at 75-110GHz ie. W-Band were envisaged, and the main commercially-available package design (Pico-Pill) was for chips with a side $\leq 250\mu m$, the chip size (and hence the pattern repeat period) was thus determined. The mask-set also required alignment markers for both gross and fine alignment to ease device processing. The whisker-contactable chips required a multi-dot type of pattern to facilitate unguided contacting. On the other hand, the bonded devices needed to incorporate larger overlay contact pads to allow bonding to the smaller area devices if they proved necessary.

Device sizes were: $100\mu m$, $50\mu m$, $20\mu m$, and $10\mu m$ in diameter (for the bonded devices) and $10\mu m$, $5\mu m$, $2\mu m$ and $1\mu m$ diameter (for the whiskered devices). Each of the "whiskered" chips could only incorporate a single device size in order to avoid confusion as to the size contacted. On the other-hand, the bonded chips could contain a variation in device size, provided careful note was taken of which device was bonded to prior to packaging (or encapsulation). Additionally it was thought to be advantageous to incorporate a selection of smaller devices which could be probed

using a four-point method for d.c. characterisation with the aim of allowing accurate investigation of the contact resistances. This possibility required the use of overlaid pads of sufficient size to allow contact by the four probes. Figure 2.11 shows a plan view of some of the features in the overall design, and Figure 2.12 shows a S.E.M. photograph of a device about to be whisker-contacted.

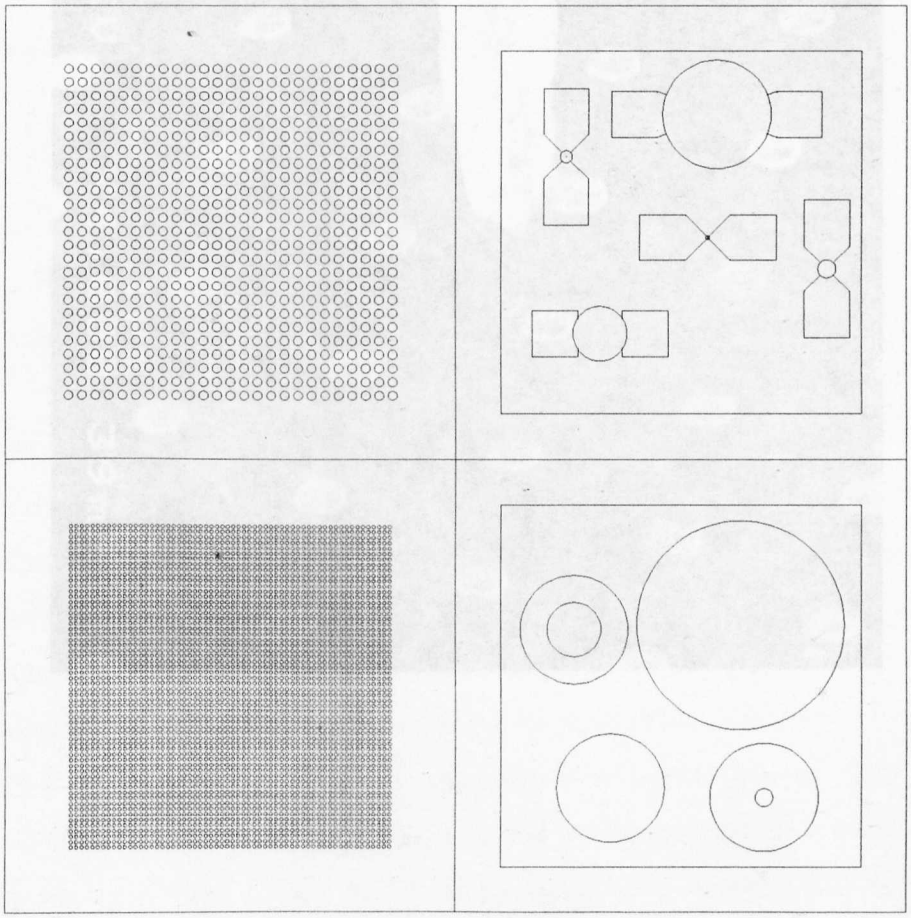


Figure 2.11 Plan view of the mask-set used to fabricate the devices used in this Thesis. Device sizes range from 100μm to 2μm in diameter.

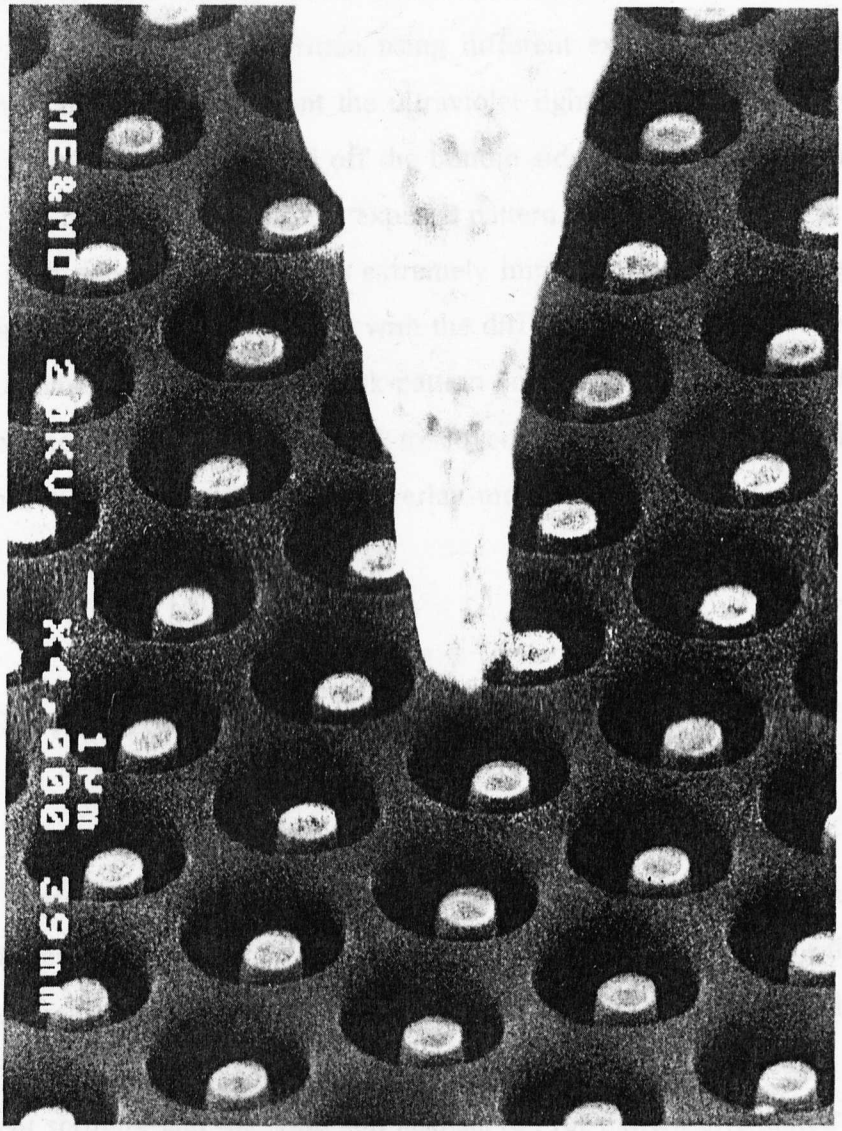


Figure 2.12 Whisker contacting of a 1μm device.

The masks were fabricated using the SERC facility at the Rutherford Appleton Laboratory (RAL) on low expansion boro-silicate glass and were coated with an anti-reflection layer. The smaller device areas required separation from the other patterns in order that they could be written using different exposure conditions. The anti-reflection coating was to prevent the ultraviolet light which was reflected from the substrate from being re-reflected off the bottom side of the mask and thereby over-exposing the resist and blurring the exposed pattern. This reduction in scattered light together with good mask contact is extremely important in small devices. The low-expansion glass was chosen to help with the difficult re-alignment process from one mask to another, by minimising mask-pattern positional variations with temperature. Four separate masks were sufficient to cover the stages of mesa etching, ohmic deposition, dielectric patterning and overlay-metal deposition.

2.5 Device processing

In order to provide a reference flat for good device alignment and subsequent scribing the substrates were cleaved along a crystal plane by nicking the edge of the wafer and subsequently breaking away from this stressed point. The cleaved edge therefore followed the natural crystal orientation. The new alignment edge assisted the subsequent scribing and breaking and also served for pattern orientation prior to any preferential etching which may have need to be done. This alignment is important and ideally should be within 2° of the crystal axis, otherwise a poor yield of cleaved devices would result. The wafer was separated into pieces of 1cm in side, which were cleaned using a three solvent boil (Trichloroethylene, Acetone and then Isopropyl alcohol) prior to further processing.

Mesa etching was initially to be accomplished by a wet-chemical process, but for the smaller devices this resulted in excessive under-cutting of the mask pattern (typically,

with good resist adhesion, etching down by 1μm results in an under-cut of 1μm on all sides) which rendered the smallest devices unusable. The use of wet-chemical etching nevertheless allowed rapid layer characterization to be achieved by permitting all the processing to be carried out at Nottingham.

The main type of resist used throughout the processing, was Hunts BPRS-150, spun at 4000-5000 r.p.m., giving a 1-1.2μm thick layer which was cured (soft-baked) in a convection oven at 110°C for 30 minutes. Exposure of the resist was carried out using a Karl Süss MJB-3 aligner with a typical intensity of $11mWcm^{-2}$, and wavelength of 365nm (U.V.) light for a duration of approximately 8 seconds. Contact between the mask and the substrate should ideally be to within the wavelength of the exposed radiation in order to achieve the ultimate resolution for this form of (contact) lithography [22]. One micron patterning proved just possible on these small pieces of material provided all other conditions were favourable. More frequently, however, 2μm was the minimum feature size achievable.

Due to the difficulty of re-alignment and under-cutting, a single stage ohmic deposition and mesa etch was preferred for defining the active device area. This was achieved by using the ohmic metallisation as the reactive-ion etch (RE) mask. This proved very successful and especially favoured the devices of 5μm diameter and below; indeed, 1μm diameter devices were formed but never studied because the 5μm diameter ones were found to be suitable for use at 100GHz and could (in principle) provide much more power. Detector (and possibly multiplier) applications may favour smaller area devices through better matching, although this has yet to be investigated.

The conditions for ohmic deposition have been discussed at length in section 2.2. However, a light etch of the GaAs surface material was carried out just prior to placing the material in the evaporator for ohmic deposition. The purpose of this was to try to clean the surface both for adhesion purposes and to provide as uncontaminated a surface as possible prior to deposition. Again, the merits of this procedure are unquantified but the end results were satisfactory and so the etching

process was retained. After ohmic deposition and annealing the mesa's were reactively ion-etched using a $SiCl_4$ low pressure (20mTorr) process. The low pressure of 20mTorr improved the slope of the sidewalls and minimised the undercutting. The etching took about 10 minutes to etch a depth of 1μm, using a power of about 60 watts, and was uniform across the wafer. It was apparent (from where some spots of metal had been inadvertently deposited) that this dry-etching process could be used to etch down to such depths on features as small as 1000Å in diameter. This conclusion may prove useful in the fabrication of sub-micron DBRT devices.

The next stage involved the planarization of the surface. This was a necessity for the whisker-contacted devices, where a relatively thick dielectric layer was needed to guide the whisker onto the top contact. This process eased the contacting process by allowing contact to be achieved without direct microscopic manipulation (unguided) in the position of the whisker point. A stereoscopic-zoom microscope was used where possible to avoid over-driving the whisker once contact was made; a curve-tracer was used to show the instant of electrical contact. Sometimes the whisker needed to be slightly over-driven to improve the contact, and at times the applied voltage needed to be increased to more than a few volts (with a large series resistance in series >500 Ohms) before a low resistance contact could be achieved. In such cases it was useful to visually check beforehand that contact had indeed been achieved.

Planarization was achieved using a polyimide dielectric layer of about 1.5μm thickness. A harder material such as silicon dioxide (or better still silicon nitride) would have been preferred but the thickness required would have been too great for the different expansion coefficients of the material involved. Layers up to about 5000Å of SiO_2 can be deposited but for much thicker layers adhesion becomes a problem, due to the relaxation of stress at the interface when the deposited layer cools from the deposition temperature (typically 300°C) to room temperature. After removal of any edge beading, and curing of the polyimide at 250°C for about two hours, a layer of 2000-3000Å of aluminium is evaporated on top. This is then patterned as usual with resist and the exposed aluminium is etched using a mixture of acetic, nitric

and orthophosphoric acids. After removal of the remaining resist using acetone or by exposure and developing, the exposed polyimide can be patterned using an oxygen plasma (10 minutes at 100 watts). A slightly higher pressure of 100mTorr during the polyimide etching helps to reduce the slope of the side-walls which are then a better guide for the whisker. The aluminium is subsequently removed using neat developer, which may also help to clean the contacts by removing a small amount of the polyimide. It is not unknown for slight amounts of the polyimide to either remain or be redeposited on the contacts which are being uncovered.

The next logical stage would have been the deposition of overlay pads for the d.c. probe devices and the bonded devices. However this stage was omitted because of the relatively soft nature of the polyimide, which was thought might actually degrade the subsequent bonding through poor adhesion of the overlaying metal. An additional possible hazard was the poor coupling of the ultrasonic bonding power to the soft material. In view of these problems and the extra processing stages involved (together with the possibility for something to go wrong), the potential risk was considered not to be worthwhile and these extra steps were forgone.

The final remaining steps were to thin the wafer down to 100μm, deposit and alloy a back-contact and then scribe and separate the individual devices. The thinning was necessary for two reasons: principally to ensure the devices fitted into the Pico-pill packages (the maximum tolerable chip height could only have been 400μm, and even this may introduce an extra parasitic frequency dependent resistive loss as discussed in section 2.22.) but also to improve the scribe-and-break process. It can be readily appreciated that for optimum cleavage the thickness of the wafer should be less than the separation of the scribed lines and (from practical experience) ideally half the thickness or less. The surface of the wafer in the region of the proposed scribed line must also be free of any covering dielectrics or metals. This is to ensure that the diamond scribe can concentrate an optimum degree of stress in the scribed region. Failure to achieve this will result in a drastic reduction in device yield.

The back-contact is alloyed at typically ~50°C below that of the top-contact. The reason for this was to try to minimise the effects of this elevated temperature process on the top-contact, although extensive investigation of the effects of a higher temperature re-alloy on the resistance of these top-contacts has not been undertaken. The poorer specific contact resistance of the back-contact (resulting from the lower temperature of alloying) could be tolerated because of its very much larger area compared to that on the front side.

Cleaving was achieved by the simple process of stressing the wafer on the front-side by rolling with a roller of an appropriate diameter (eg. a diameter of between 4 and 8 times the chip repeat spacing is appropriate) on the back-side. It is important that rolling is only carried out in the direction perpendicular to the scribe lines at which breaking is required and not obliquely to them. Prior to this breaking process, the wafer was mounted bottom-side down onto a low tack sticky film. This film can be stretched once the chips have been broken to separate each chip from its neighbour, thereby easing removal and preserving the correct "geographical" position on the wafer. This is the industry-standard method for handling such small GaAs devices and the chip-ejection process can even be semi-automated at this stage if the necessary equipment is available.

2.5.1 Packaging and whisker contacting

The package chosen for use at X-band (8-12GHz) was of the S-4 type. At W-band (75-110GHz), the Pico-pill type of package was used. Both of these packages are common two terminal device packages. One variant, however, was the "Leadless Inductive Device" (or LID) type of package. This has an extremely low associated shunt capacitance of around 20fF and is therefore ideal for high frequency detectors. This was used for early detector measurements at MEDL in Lincoln. For the W-band studies however, the packageless mounting of whisker contacted devices was

preferred. This was again to minimise the associated shunt capacitance of the contacted device. Whisker contacting could be tolerated for our work since mechanical stability was not a key issue. However a departure from whiskering would be necessary for any practical widespread application; with careful design this need not, however compromise the overall performance of a system. Whisker-contacting was achieved using either an integral whisker-mounted block design (Chapter 5), or a "sharpless" whisker mounted "package". The sharpless packaging technique was developed by its namesake [30] and has long been favoured as a low parasitic yet portable package for very high frequency devices (usually above 35 GHz) and consists simply of a thin section of waveguide (about 2-3 mm) within which the whisker contact is made. This waveguide section is then inserted between the output (or input) waveguide; a tuning section and a sliding short-circuit incorporated at the other side. This technique was used for all measurements above 75GHz except for the W-band multiplier measurements which required specialist cavities.

A large number of whiskers on pins were purchased from Philips Components at Stockport. These consisted of 0.9mm diameter pins on which was mounted 25μm nickel coated Invar wire. The wire was about 700μm long and sharpened to a point of about 0.5μm radius. In the later stages of the work shorter whiskers on smaller pins were required, and for this purpose 10μm diameter phosphor-bronze wire was used. This thin wire was sharpened electro-chemically under a microscope using a 10% solution of nitric acid (initially) and a voltage source; tip radii of 1-2μm were obtained which were adequate for the present purpose.

The Pico-pill packages were in fact rarely used because (without the use of the overlay pads) the smallest bondable device proved to be 20μm. This tended to be too large to be used at W-band, due to excessive junction (shunt) capacitance. It was also thought that the shunt capacitance of the package might have compromised the modest performance of the DBRT devices. The S-4 (X-band) package was extensively used for the lower frequency work. Such packages have previously been used by the author at frequencies as high as 35GHz for Esaki tunnel (backward) diodes.

Bonding was carried out using a K&S ultra-sonic wedge-bonder which was set-up to handle 10μm diameter gold wire. Background heat was not usually required, but if this was needed then the maximum temperature could only be about 100°C. This temperature was limited because silver-epoxy was used to provide electrical and physical contact to the back-side of the chip and it became soft if the temperature was to high. From previous experience bonding temperatures of 200-250°C would have been preferred. The industry-standard method to attach chips to such packages is by using a gold-germanium solder preform; these preforms melt at around 350°C and, when cool, provide excellent electrical and thermal contact. Attempts were made to use this process but the preforms seemed to preferentially scavenge the thin (2000-3000Å) gold on the back-side of the DBRT chips and leave them un-attached. The minimum size of dèvice which could be bonded using this technique was 20μm in diameter and, without using overlay pads, this also limited the active areas to this size. These 20μm diameter devices proved satisfactory as oscillators at X-band once the appropriate low impedance matching conditions had been achieved.

2.6 Future processing improvements

For future work the move to a co-planar device layout should greatly enhance the high frequency performance, mainly by the reduction of d.c. and h.f. parasitic resistances. The effects of fringing capacitance on the surface and the shunt capacitance of the substrate would then need to be carefully considered. The use of thinned semi-insulating substrates should greatly reduce some of these possible shunt losses and the careful layout of top contacts should minimise the fringing effects. The proximity of the emitter and collector contacts and the use of high conductivity gold pads or tracks to connect to the outside world, should also minimise the frequency-dependent spreading resistance which would otherwise result from long path lengths to ground on the relatively poor-conductivity substrate material (see Figure 2.13). Finally, the ability to define the active region by selectively under-cutting the emitter contact [24,27] should permit the reduction of the emitter contact resistance.

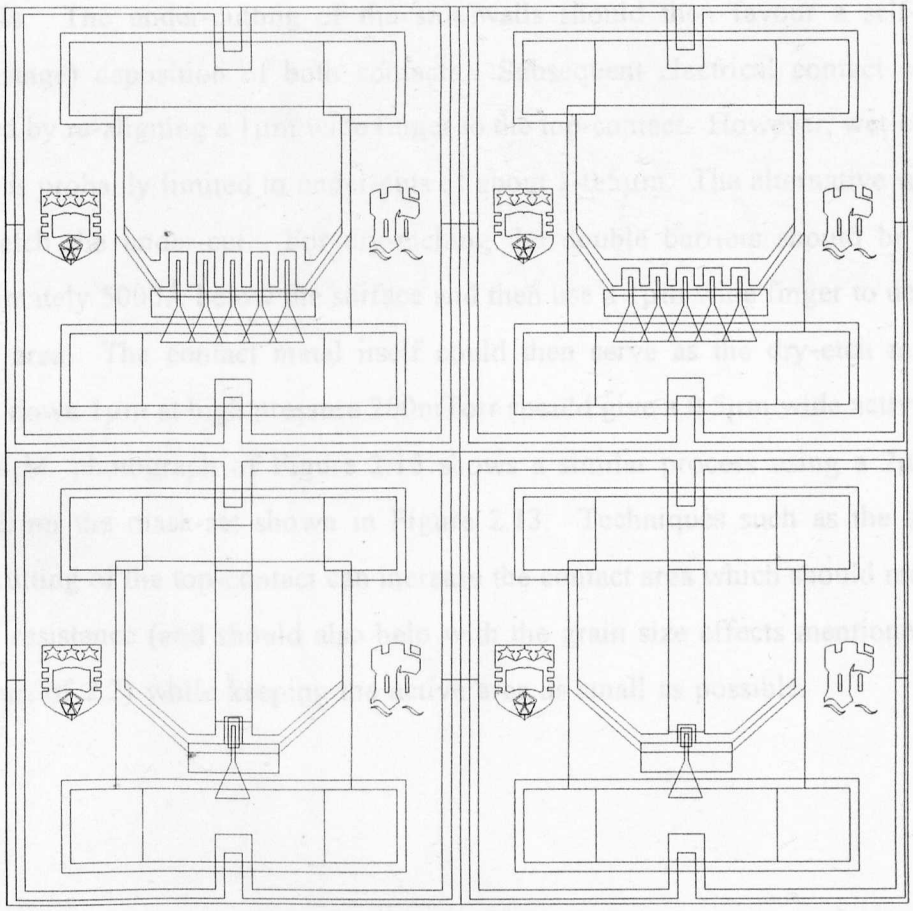


Figure 2.13 Mask layout for co-planar devices on semi-insulating GaAs

The method to be used for such a co-planar device would be as follows:

The emitter contact would be defined by using one or other of two methods; a stripe of resist running in the direction of the crystal plane and thereby permitting selective undercutting perpendicular to this direction (see the S.E.M. photo in Figure 2.14). If the resist width was, for example, 5μm wide then by etching down 1μm using an acid-peroxide based etch the resultant strip should be about 3μm wide with under-cut sidewalls. The under-cutting of the side-walls should then favour a self-aligned (single-stage) deposition of both contacts. Subsequent electrical contact could be achieved by re-aligning a 1μm wide finger to the top-contact. However, wet-chemical etching is probably limited to under-cuts of about 1-0.5μm. The alternative would be to dry-etch the under-cut. For dry-etching the double barriers should be located approximately 5000Å below the surface and then use a 1μm wide finger to define the contact area. The contact metal itself could then serve as the dry-etch mask and etching down 1μm at high pressure 200mTorr should give a 0.5μm wide active width. The S.E.M. photograph of Figure 2.15 shows a similar process using a 2μm wide finger from the mask-set shown in Figure 2.13. Techniques such as the selective under-cutting of the top-contact can increase the contact area which should reduce the contact resistance (and should also help with the grain size effects mentioned in the latter part of 2.2) while keeping the active area as small as possible.

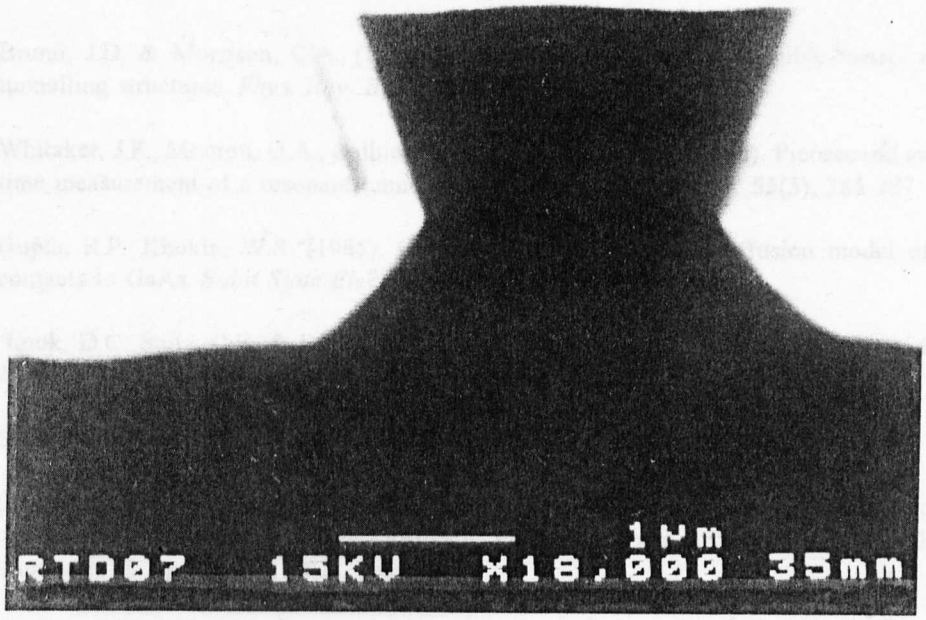


Figure 2.14 Photograph of the degree of under-cutting possible using a selective acid-peroxide etch.

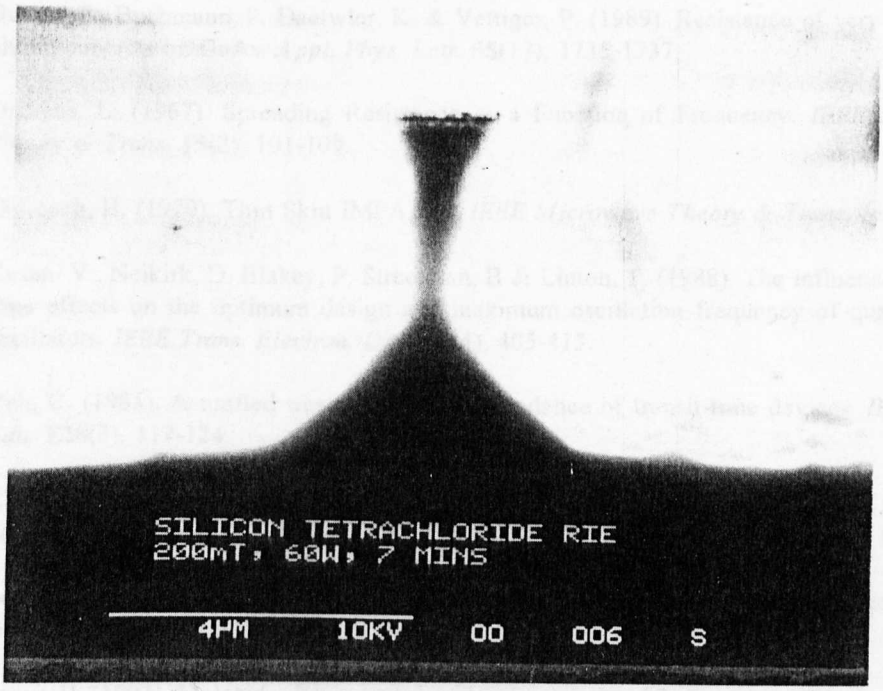


Figure 2.15 Photograph of the degree of under-cutting possible using dry-etching [31]

2.7 References:

[1] Bruno, J.D. & Morrison, C.A. (1988). Limiting response time of double-barrier resonant tunnelling structures. *Phys. Rev. Bull.* **37**(12), 7098-7101.

[2] Whitaker, J.F., Mourou, G.A., Sollner, T.C. & Goodhue, W.D. (1988). Picosecond switching time measurement of a resonant tunnelling diode. *Appl. Phys. Lett.* **53**(5), 385-387.

[3] Gupta, R.P. Khokle, W.S. (1985). Gallium-vacancy-dependent diffusion model of ohmic contacts to GaAs. *Solid State Electronics* **28**(8), 823-830.

[4] Look, D.C. Stutz, C.E. & Evans, K.R. (1990). Unpinning of GaAs surface Fermi level by 200°C molecular beam epitaxial layer. *Appl. Phys. Lett.* **57**(24), 2570-2572.

[5] Stall, R., Wood, C.E. & Eastman, L.F. (1979). *Electronic Lett.* **15**, 800.

[6] Dilorenzo, J.V., Nicheus, W.C. & Cho, B.Y. (1979). Non alloyed and in situe ohmic contacts to highly doped n-type GaAs layers grown by molleeular beam epitaxy (MBE) for field effect transistors. *J. Appl. Phys.* **50**(2), 951-954.

[7] Muto, S., Inata, T. et al. (1987). Quantum well width dependence of negative differential resistance of $In_{0.52}Al_{0.48}As$ / $In_{0.53}Ga_{0.47}As$ resonant tunnelling barriers grown by MBE. *Jap. J. Appl. Phys.* **26**(3), 220-222.

[8] Reevs, G.K. & Harrison, H.B. (1982). Obtaining the specific contact resistance from transmission line model measurements. *IEEE Electron. Dev. Lett.* **3**(5), 111-113.

[9] Gueret, P., Buehmann, P. Daetwler, K. & Vettiger, P. (1989). Resistance of very small area ohmic contacts on GaAs. *Appl. Phys. Lett.* **55**(17), 1735-1737.

[10] Dickens, L. (1967). Spreading Resistance as a Function of Frequency. *IEEE Microwave Theory & Trans.* **15**(2), 101-109.

[11] DeLoach, B. (1970). Thin Skin IMPATTS. *IEEE Microwave Theory & Trans.* Jan., 72-74.

[12] Kesan, V., Neikirk, D. Blakey, P. Streetman, B & Linton, T. (1988). The influence of transit time effects on the optimum design and maximum oscillation frequency of quantum well oscillators. *IEEE Trans. Electron. Dev.* **35**(4), 405-413.

[13] Yeh, C. (1985). A unified treatment of the impedance of transit-time devices. *IEEE Trans. Edu.* **E28**(3), 117-124.

[14] Clinton, P., Truscott, W. & Wen, F. (1988). Elimination of flux transients from molecular-beam epitaxy source cells following shutter operation. *J. Vac. Sci. & Tech.* **6**(4), 1099-1104.

[15] Foxon, T. & Harris, J. (1986). The growth of high purity III-V structures by molecular beam epitaxy. *Philips J. Res.* **41**(3), 313-324.

[16] Joyce, B. (1991). Molecular beam epitaxy of semiconductor films - atomic dimension control and evaluation of crystal growth dynamics. *Contemporary Physics* **32**(1), 21-34.

[17] Heterojunction band discontinuities: Physics & device applications. Capasso, F. & Margaritondo, G. (1987): North-Holland

[18] Söderström, J. & Andersson, T. (1989). GaAs/AlGaAs Resonant tunnelling diodes: The dependence of the peak-to-valley current ratio on the barrier thickness and height. *Superlattices & Microstructures* **5**(1), 109-113 .

[19] Cheng, P. & Harris, J. (1989). Effect of Si doping in AlAs barrier layers of AlAs-GaAs-AlAs double barrier resonant tunnelling diodes. *Appl. Phys. Lett.* **55**(6), 572-574.

[20] Adachi, S. (1985). GaAs AlAs and $Al_xGa_{1-x}As$: Material parameters for use in research and device applications. *J. App. Phys.* **58**(3), R1-R29.

[21] Henning, J. & Ansems, J. (1988). *Semicond. Sci. & Tech.* **3**(4), 361-365.

[22] Karl Suss technical report (1991). **V5**(Q1)

[23] Kim, T. & Chung, D. (1985). The effects of Germanium concentration on the compound formation and morphology of gold-based contacts to gallium arsenide. *J. Vac. Sci. Tech.* **4**(3), 762-768.

[24] Iida, S. & K. Ito, K. (1971). Selective etching of Gallium Arsenide Crystals in H_2SO_4-H_2O_2-H_2O system. *J. Electrochem. Soc. S.S. Science* **118**(5), 768-771.

[25] Brown, E.R., Sollner, T.C.L.G., Parker, C.D., Goodhue, W.D. & Chen, C.L. (1989). Oscillations up to 420 GHz in GaAs/AlAs resonant tunneling diodes. *Appl. Phys. Lett.* **55**(17), 1777-1779.

[26] Sollner, T.C.L.G. Brown, E.R. Parker, C.D. & Goodhue, W.D. (1990). High-frequency applications of resonant tunneling devices. Electronic properties of multilayers and low-dimensional semiconductor structures. Eds. J. M. Chamberlain, L. Eaves & J-C. portal. NATO ASI series-b **123**: Plenum N.Y.

[27] Shaw, D.W. Localized GaAs etching with acid hydrogen peroxide solutions. (1981). *J. Electrochem. Soc: Solid-State science & Tech.* **128**(4), 874-880.

[28] Stanaway, M.B. (1989). *Inst. of Phys. Conf. Series* **95**, Ch. 4, 295.

[29] Childs, K.D. & Baker, J.M. (1986). Microstructure studies of AuNiGe ohmic contacts to N-type GaAs. *J. Vac. Sci. & Tech.* **4**(4), 903-911.

[30] Sharpless, W.M. (1956). Wafer-type Millimetre wave rectifiers. *Bell Syst. Tech. J.* **35**, 1385-1402.

[31] Photograph and etching courtesy of M. Pate at the Sheffield University III-V Device Processing Facility (1993).

[32] Henry, H.G. Dawson, D.E. Lemnios, Z.J. & Kim, H. (1984). Hot-plate alloying for ohmic contacts to GaAs. *IEEE Trans. Electron. Dev.* **31**(8), 1100-1103.

CHAPTER 3

Theory of Double Barrier Device Operation

3.1 Introduction

This chapter discusses the main theoretical aspects of operation of the DBRT class of devices which relate to the performance of the device both at d.c. and at high frequencies. The most significant factors are the layer parameters of the double barrier region, and to a lesser extent those in the immediate vicinity of the barriers. Sections 3.2 and 3.3 introduce the relevant theory behind the operation while the subsequent sections deal with the specific devices used in this study. Finally, the high frequency implications of these layer-dependent parameters is dealt with in section 3.4. The reader is also referred to the general introduction given in section 1.3 of Chapter 1, and the measured current-voltage characteristics shown in Chapter 2.2.

It is worth pointing out that the modelling of a device's behaviour, in response to a stimulation, invariably requires much simplification to solve an otherwise intractable problem. The accuracy of the subsequent modelled performance is therefore only appropriate to the strict conditions which were assumed prior to constructing the model. By the very nature of this sort of modelling, the process is an iterative one requiring successive evolution towards a final model. Depending on the required application of the model, the accuracy of the final "picture" can usually be relaxed. For example, in the present study, this relaxation will be possible if all that is required is a qualitative understanding of the important factors needed to influence the growth

of further layers. However, a more detailed quantitative model was also sought which, it was hoped, could provide sufficiently accurate results to contribute parameters for other types of models relating to high frequency performance. The accuracy of the modelling is therefore dependent on the initial assumptions, and also the accuracy required of the final result also imposes constraints throughout the model hierarchy. The aim of this study was to relate the layer characteristics to the high frequency performance; this performance is dependent on the d.c. effects of these material parameters.

Some of the main material parameters which affect this performance are introduced and will subsequently be discussed further. These are :

(I) The exact composition and characteristic lengths of the double barriers and well regions. These determine the overall transmission coefficient of the structure, and hence (to a first order) the transmission characteristics (section 3.3.2).

(II) The degree of scattering in the well. This results in a loss of phase of the transmitted electrons with respect to those at resonance (section 3.3.3).

Due to the significance of the second factor further discussion surrounding the degree of scattering in the well, will now be given :

In the devices studied here, scattering is thought to occur mainly at the interfaces of the barriers with the well, rather than in the well itself, due to the very thin wells used. The presence of undoped spacer layers can also effect the amount of scattering and thereby the valley current, by reducing the degree of silicon interdiffusion between the moderately-doped cladding layers and the barriers [1, 2, 3]. However, an alternative explanation for the improved (lower) valley current has been proposed by Cheng and Harris [4].

Another significance of the spacer layers is via their ability to modify the position of

the Fermi energy adjacent to the barriers which can, under certain bias conditions, profoundly affect the freedom of the electrons in these adjacent layers (section 3.3.5). In the case of the emitter this determines the proportion of electrons with the correct momentum to tunnel to the collector. This latter effect is important mainly at low temperatures and for devices with a larger spacer layer thickness'. Similarly, the doping in the cladding layers also determines the number of electrons which can tunnel (once they reach the resonant energy) by controlling the position of the fermi energy in the emitter with respect to that of the confined state in the well (section 3.2). In the case of the collector cladding layer, the doping here determines the length of the depletion region and hence the voltage drop across this region (section 3.3.5). This, in turn, contributes to the position of the peak current with respect to the applied bias.

3.2 Calculation of Fermi energies for DBRT structures

3.2.1 Introduction and results

For the samples used in this study only the electron concentration is of interest. The contribution to the room temperature conductivity from intrinsic conduction may also be neglected, since typical emitter-dopant concentrations are of the order of $1*10^{17}cm^{-3}$ ($1*10^{23}m^{-3}$). The position of the Fermi energy must be known accurately in order to calculate the number and spread of electrons able to tunnel. For the range of doping used in the present samples, an impurity band may be formed which overlaps with the conduction band. The presence of this impurity band means that at low temperatures there is a metallic-like fermi sea of electrons in the conduction band. At room temperature, however, donor atoms can bind electrons, although in this case a certain fraction of these atoms will be ionised.

We have calculated the approximate position of the fermi level for a range of donor densities appropriate to emitter dopings used in the present devices and for a range of

temperatures. The results are shown in Table 3.1.

Doping	$2*10^{16}/cm^3$	$5*10^{16}/cm^3$	$1*10^{17}/cm^3$	$2*10^{17}/cm^3$	$2*10^{18}/cm^3$
Temperature	Position of E_F	Position of E_F	Position of E_F	Position of E_F	Position of E_F
0 K	4 meV	7 meV	11 meV	18 meV	86 meV
77 K	- 8.4 meV	-3.7 meV	-0.4 meV	2.6 meV	11 meV
300 K	- 80 meV	- 60 meV	- 44 meV	- 30.6 meV	8.6 meV

Table 3.1

In accordance with usual practice, the Fermi energy (E_F) is referred to the energy at the bottom of the conduction band, which is taken as zero. The details of the calculation will now be given below [5,36]. Table 3.2 shows a summary (for the convenience of the reader) of the symbols used in this calculation.

Table 3.2 Symbols used in calculation of fermi energies

Energies		
	Electron energy relative to CB edge	E
	Fermi energy	E_F
	Fermi energy at T= 0 K	E_F^0
	Donor energy (below CB)	E_D
	Band gap energy	E_G
Wavevectors		
	Fermi wavevector	k_F
	Screening wavevector	k_S
	Electron wavevector	k
Densities (per unit volume)		
	Number of donors	N_D
	Number of neutral donors	N_{D0}
	Number of electrons in conduction band	N_e
	Density of states at bottom of CB	$N_C(T)$
Standard quantities		
	Bohr radius	a_0
	Electron effective mass	m^*
	Electron charge	e
	Boltzmann's constant	k_B
	"Dielectric constant" (12.5 for GaAs)	ε_r
	Permittivity of free space	ε_0
Other quantities		
	$\beta = 1/k_BT$	
	$\zeta = \beta E_F$	
	$x = \beta E$	
	$F_{1/2}(\zeta)$, the Fermi half-integral	

3.2.2 Conditions for the formation of an impurity band

The condition for the formation of an impurity state has been given by Rogers et al (1970) [6] as;

$$k_S a_0 < 1.2 \tag{3.1}$$

where k_s is the screening wavevector of an ionised donor impurity with a potential;

$$\Phi(r) = \frac{e}{4\pi\varepsilon_r\varepsilon_0 r} e^{-k_S r} \tag{3.2}$$

and a_0 is the Bohr radius:

$$a_0 = \frac{\hbar^2 4\pi\varepsilon_r\varepsilon_0}{m^* e^2} \tag{3.3}$$

The screening wavevector of the electron (degenerate fermi gas) can be taken as;

$$k_S = \left(\frac{N_e e^2}{\varepsilon_r\varepsilon_0}\frac{3}{2E'}\right)^{\frac{1}{2}} \tag{3.4}$$

where E' may be taken as the Fermi energy at T = 0 K (E_F^0) , for the calculation at 0K, and $3/2.k_BT$ for the calculation at 300K. E_F^0 may be calculated from:

$$E_F^0 = \frac{\hbar^2 k_F^2}{2m^*} \tag{3.5 a}$$

$$k_F = (3\pi^2 N_e)^{1/3} \tag{3.5 b}$$

Estimates of the product $k_S a_0$ will now be made.

At 0K (4.2K in practice), for a doping of $N_D = 10^{17}cm^{-3}$, a value of $E_F^0 = 11.7meV$ may be calculated from 3.5 (a) and (b). Assuming that $N_D = N_e$, from (3.4),

k_S=0.14 * 10 ^{9} m^{-1} and since a_0 = 9.8nm (for GaAs), $k_S a_0$=1.3. Since $k_S a_0$>1.3, in this case, it is concluded that donors cannot bind electrons and a degenerate metallic-like Fermi "sea" is formed in the conduction band.

At 300K ($k_B T$= 26meV), for the same doping, the conditions are non-degenerate since $k_B T$>11.7meV. The same calculation now yields $k_S a_0$=0.74 and individual donors can bind electrons. It is therefore essential to the calculation of Fermi level that the presence of the donor energy E_D below the conduction band be recognised.

At the intermediate temperature 77K, $k_B T$=6.7meV ie. E_F^0>6.7meV so degenerate (4.2K case) statistics apply.

3.2.3 Calculation of Fermi level at 0K

This will proceed from equations 3.5 (a) & (b). The results are shown in the first row of Table 3.1 for several dopant concentrations. It is assumed that we have a degenerate Fermi "gas" in the conduction band.

3.2.4 Calculation of Fermi level at 300K

As noted earlier, $k_S a_0$<1.2 and we have a non-degenerate system. Although an impurity band is formed (as is the case at lower temperatures), some individual donors will bind electrons and the rest will be in the conduction band. The position of the Fermi level is then obtained from:

$$N_e = \frac{(2m^*)^{3/2}}{2\pi^2 \hbar^3 \beta^{3/2}} \int_0^\infty \frac{x^{1/2}}{e^{(x-\zeta)}+1}\, dx \qquad (3.6)$$

which can be re-written as;

$$N_e = N_c \frac{2}{\sqrt{\pi}} F_{1/2}(\zeta) \tag{3.7}$$

where $F_{1/2}(\zeta)$ is the standard Fermi half-integral.

N_c is defined as:

$$N_c(T) = 2\left(\frac{m^* k_B T}{2\pi \hbar^2}\right)^{3/2} \tag{3.8}$$

in the extreme non-degenerate; $E_F \ll -kT$ or $N_D \leq \frac{1}{2}N_c$ limit (high temperature).

$$F_{1/2}(\zeta) = \frac{\sqrt{\pi}}{2} e^{\zeta} \tag{3.9}$$

so that

$$N_e \approx N_c e^{\zeta} = N_c e^{\frac{E_F}{k_B T}} \tag{3.10}$$

It is instructive to use this approximation, initially, for the calculation of E_F at 300K. Assuming all the donors are ionised ie. $N_D = N_e$. From (3.8), $N_c(T)=4.36*10^{17}cm^{-3}$ so when $N_e = N_D = 10^{17}cm^{-3}$, from (3.9) and (3.10) :

$$F_{1/2}(\zeta) = \left(\frac{\sqrt{\pi}}{2}\right)\left(\frac{N_D}{N_C}\right) = 0.20 \tag{3.11}$$

From standard tables [35] $\zeta = -1.4$ and (from definition of ζ) $E_F = -1.4*k_BT = -36.3meV$. Thus the Fermi level is negative ie well below the bottom of the conduction band. Note that it is also greater than the typical value for E_D ($\approx$5meV).

A more complete calculation for the non-degenerate case may be performed taking into account the binding of some electrons to individual donor atoms. This uses the

charge neutrality equation:

$$N_e + N_{D0} = N_D \tag{3.12}$$

(the role of the acceptors is neglected) Using (3.10), together with the expression

$$N_{D0} = \frac{N_D}{1 + \frac{1}{2}e^{(-E_D - E_F)\beta}}, \tag{3.13}$$

which (provided $E_F \ll E_D$) may be approximated as:-

$$N_{D0} \simeq 2N_D e^{(E_D + E_F)\beta}, \tag{3.14}$$

we can substitute in (3.12) to obtain:

$$N_c e^{\zeta} + 2N_D e^{\beta E_D} e^{\zeta} = N_D . \tag{3.15}$$

Solving (3.15) for e^{ζ}, and using $E_D \approx 5$meV and $N_c = 4.36*10^{17}cm^{-3}$, we have $e^{\zeta} \approx 0.15$ giving $E_F = -48$meV. The rather lower value obtained in comparison with the previous estimate (-36meV) indicates that some of the electrons have indeed been frozen out on donors. It is this procedure or the (preferred although less intuitive) more general itterative computer solution of the complete form (neglecting assumptions about E_F) of equation 3.12 which is used to calculate Fermi energies (N-type only) at 300K; the results are shown in Table 3.1.

3.2.5 Calculation of Fermi level at 77K

Problems arise at 77K if it is assumed that all the donors are ionised ie. $E_F < -kT$ or $N_D \leq \frac{1}{2}N_C$. Typically only a fraction of the donors are ionised and in this case equation 3.12 has again to be solved itteratively in order to find the position of the Fermi energy. Provided however, the conditions for non-degeneracy apply then: (at 77K) $k_B T = 6.7$meV and $N_c = 5.7*10^{16}cm^{-3}$, so for the case where $N_D = 2*10^{16}cm^{-3}$ ($N_D \leq \frac{1}{2}N_C$) can we assume that nearly all the donors are ionised ie. $N_c = N_D$ and as each donor

provides one electron, the expression (3.7) may therefore be written as:

$$N_e = N_D = \frac{2N_c}{\sqrt{\pi}} F_{1/2}(\zeta) \qquad (3.16)$$

So for $N_D=2*10^{16}cm^{-3}$ we have $F_{1/2}(\zeta)=0.31$ and using the previous tabular procedure, a value of $\zeta \approx -0.8$ may be calculated giving $E_F= -5.3meV$ for $N_D=2*10^{16}cm^{-3}$ neglects any "freeze-out" of electrons on the donors. Again for the values shown in Table 3.1 the more general (itterative) solution of equation 3.12 was preferred for calculating the position of the Fermi energy at 77K and given the broad range of doping used for the wafers grown for this study. It can be seen that even for doping in the region of $2*10^{16}cm^{-3}$ there are some electrons which have been frozen out on the donors ie.: $E_F= -8.4$ rather than $E_F= -5.3$ (as calculated from equation 3.16).

3.3 D.C. Tunnelling theory

In Chapter 1, the tunnelling at a single barrier is reviewed. Equations (1.5) and (1.6) are derived which ensure the conservation of flux on both sides of the barrier. The evaluation of these equations can be carried out algebraically for simple potential profiles or by using various approximate methods such as the WKB method. Recently, more exact solutions such as the transfer matrix approach and Monte Carlo solutions of the semiclassical transport equations have been developed to describe complicated potential profiles. These approaches are discussed in the standard text-books [7]; the transfer matrix technique is perhaps the best method for quantitatively describing the tunnelling at a single barrier in one-dimension.

3.3.1 Transfer matrix treatment

The transfer matrix technique has been discussed by Kane (1969) and by Ricco and Azbel (1984), among others.[8, 9] and what follows is the application of these techniques to the particular case of the DBRT device.

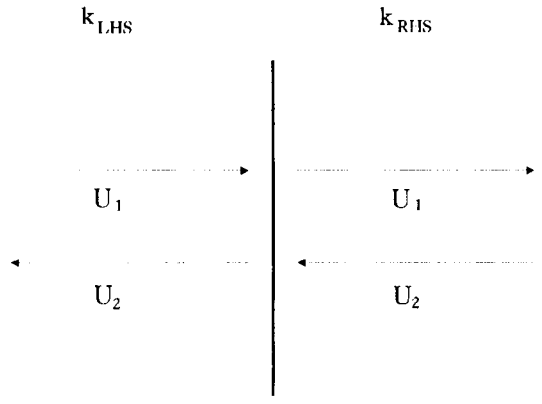


Figure 3.1 Representation of the interface

Consider tunnelling at the interface shown in Figure 3.1, in general, the equation for the wavefunction of an electron (1.3) can be represented by:

$$U(x)=U_1^{\rightarrow}(x)+U_2^{\leftarrow}(x) \ , \tag{3.17}$$

where the arrows show the direction of propagation.

Describing equations (1.5) and (1.6) in this fashion, leads to

$$U_1^{\rightarrow}(<a)+U_2^{\leftarrow}(<a)=U_1^{\rightarrow}(>a)+U_2^{\leftarrow}(>a) \tag{3.18}$$

and

$$\frac{ik_{lhs}}{m^*_{lhs}}[U_1^{\rightarrow}(<a)-U_2^{\leftarrow}(<a)]=\frac{ik_{rhs}}{m^*_{rhs}}[U_1^{\rightarrow}(>a)-U_2^{\leftarrow}(>a)] \ . \tag{3.19}$$

(where the interface is at x = a (Fig. 3.1)) and solving equations 3.18 and 3.19 for $U_1^{\rightarrow}(<a)$ and $U_2^{\leftarrow}(<a)$ gives:

$$2U_1^{\rightarrow}(<a)=\left(1+\frac{k_{rhs}m^*_{lhs}}{k_{lhs}m^*_{rhs}}\right)U_1^{\rightarrow}(>a)+\left(1-\frac{k_{rhs}m^*_{lhs}}{k_{lhs}m^*_{rhs}}\right)U_2^{\leftarrow}(>a)\ , \tag{3.20}$$

and

$$2U_2^{\leftarrow}(<a)=\left(1-\frac{k_{rhs}m^*_{lhs}}{k_{lhs}m^*_{rhs}}\right)U_1^{\rightarrow}(>a)+\left(1+\frac{k_{rhs}m^*_{lhs}}{k_{lhs}m^*_{rhs}}\right)U_2^{\leftarrow}(>a)\ . \tag{3.21}$$

These equations may be put in matrix form:

$$\begin{bmatrix}U_1^{\rightarrow}(<a)\\U_2^{\leftarrow}(<a)\end{bmatrix}=\frac{1}{2}\begin{bmatrix}\left(1+\frac{k_{rhs}m^*_{lhs}}{k_{lhs}m^*_{rhs}}\right) & \left(1-\frac{k_{rhs}m^*_{lhs}}{k_{lhs}m^*_{rhs}}\right)\\ \left(1-\frac{k_{rhs}m^*_{lhs}}{k_{lhs}m^*_{rhs}}\right) & \left(1+\frac{k_{rhs}m^*_{lhs}}{k_{lhs}m^*_{rhs}}\right)\end{bmatrix}\begin{bmatrix}U_1^{\rightarrow}(>a)\\U_2^{\leftarrow}(>a)\end{bmatrix}\ , \tag{3.22}$$

which is summarised as :

$$U(<a)=M\,U(>a)\ , \tag{3.23}$$

where M is the transfer matrix describing the transmission and reflection at the interface x =a. Similarly, for the case of a region of space of width (w), across which the potential is now constant,

$$U_1^{\rightarrow}(x+w)=A_1^{\rightarrow}e^{ik(x+w)}\ \equiv e^{ikw}U_1^{\rightarrow}(x) \tag{3.24}$$

describes the right-going wave, and

$$U_2^{\leftarrow}(x+w)=A_2^{\leftarrow}e^{-ik(x+w)} \equiv e^{ikw}U_2^{\leftarrow}(x) \tag{3.25}$$

represents the left-going wave.

Again, these equations can be given in matrix form such as

$$U(x)=C\ U(x+w)\ , \tag{3.26}$$

where

$$C=\begin{bmatrix} e^{-ikw} & 0 \\ 0 & e^{ikw} \end{bmatrix}. \tag{3.27}$$

If E>V then the waves are travelling plane-waves and, as before,
$k = [2m^*(E-V)/\hbar^2]^{1/2}$. If, on the other hand, E<V then the waves are decaying imaginary waves ie. $k = i\alpha$, and $\alpha = |[2m^*(V-E)/\hbar^2]^{1/2}|$. The matrix C now becomes;

$$C=\begin{bmatrix} e^{\alpha w} & 0 \\ 0 & e^{-\alpha w} \end{bmatrix}. \tag{3.28}$$

Following on from this, the approach may be applied to a double barrier structure by considering the interfaces and regions of constant potential in turn. For the interface between the emitter and the first (ie. emitter) barrier, the transfer matrix is M_{Ebe}, where:

$$M_{Ebe}=\frac{1}{2}\begin{bmatrix} \left(1+\frac{ik_{be}m_e^*}{k_e m_{be}^*}\right) & \left(1-\frac{ik_{be}m_e^*}{k_e m_{be}^*}\right) \\ \left(1-\frac{ik_{be}m_e^*}{k_e m_{be}^*}\right) & \left(1+\frac{ik_{be}m_e^*}{k_e m_{be}^*}\right) \end{bmatrix} \equiv \frac{1}{2}\begin{bmatrix} M_{11} & M_{12} \\ M_{21} & M_{22} \end{bmatrix}, \tag{3.29}$$

and for the emitter barrier, the matrix is:

$$B_e = \begin{bmatrix} e^{k_{be}L_{be}} & 0 \\ 0 & e^{-k_{be}L_{be}} \end{bmatrix} \equiv \begin{bmatrix} B_{11} & 0 \\ 0 & B_{22} \end{bmatrix}. \tag{3.30}$$

For the interface between the emitter barrier and the well, the relevant matrix is:

$$M_{beW} = \frac{1}{2}\begin{bmatrix} \left(1 - \frac{ik_w m_{be}^*}{k_{be} m_w^*}\right) & \left(1 + \frac{ik_w m_{be}^*}{k_{be} m_w^*}\right) \\ \left(1 + \frac{ik_w m_{be}^*}{k_{be} m_w^*}\right) & \left(1 - \frac{ik_w m_{be}^*}{k_{be} m_w^*}\right) \end{bmatrix} \equiv \frac{1}{2}\begin{bmatrix} M_{11} & M_{12} \\ M_{21} & M_{22} \end{bmatrix}. \tag{3.31}$$

For the well itself, the appropriate matrix is:

$$W = \begin{bmatrix} e^{-ik_w L_w} & 0 \\ 0 & e^{ik_w L_w} \end{bmatrix} \equiv \begin{bmatrix} W_{11} & 0 \\ 0 & W_{22} \end{bmatrix}. \tag{3.32}$$

For the well-to-collector barrier interface:

$$M_{Wbc} = \frac{1}{2}\begin{bmatrix} \left(1 + \frac{ik_{bc} m_w^*}{k_w m_{bc}^*}\right) & \left(1 - \frac{ik_{bc} m_w^*}{k_w m_{bc}^*}\right) \\ \left(1 - \frac{ik_{bc} m_w^*}{k_w m_{bc}^*}\right) & \left(1 + \frac{ik_{bc} m_w^*}{k_w m_{bc}^*}\right) \end{bmatrix} \equiv \frac{1}{2}\begin{bmatrix} M_{11} & M_{12} \\ M_{21} & M_{22} \end{bmatrix}, \tag{3.33}$$

and for the collector barrier alone:

$$B_c = \begin{bmatrix} e^{k_{bc}L_{bc}} & 0 \\ 0 & e^{-k_{bc}L_{bc}} \end{bmatrix} \equiv \begin{bmatrix} B_{11} & 0 \\ 0 & B_{22} \end{bmatrix}. \tag{3.34}$$

Finally, for the interface between the collector barrier and the collector:

$$M_{bcC} = \frac{1}{2}\begin{bmatrix} \left(1 - \frac{ik_c m^*_{bc}}{k_{bc} m^*_c}\right) & \left(1 + \frac{ik_c m^*_{bc}}{k_{bc} m^*_c}\right) \\ \left(1 + \frac{ik_c m^*_{bc}}{k_{bc} m^*_c}\right) & \left(1 - \frac{ik_c m^*_{bc}}{k_{bc} m^*_c}\right) \end{bmatrix} \equiv \frac{1}{2}\begin{bmatrix} M_{11} & M_{12} \\ M_{21} & M_{22} \end{bmatrix}. \tag{3.35}$$

Hence for transmission through the complete structure:

$$\begin{bmatrix} U_1^- \\ U_2^- \end{bmatrix}_{lhs} = \frac{1}{16}\begin{bmatrix} M_{11} & M_{12} \\ M_{21} & M_{22} \end{bmatrix}\begin{bmatrix} B_{11} & 0 \\ 0 & B_{22} \end{bmatrix}\begin{bmatrix} M_{11} & M_{12} \\ M_{21} & M_{22} \end{bmatrix}\begin{bmatrix} W_{11} & 0 \\ 0 & W_{22} \end{bmatrix}\begin{bmatrix} M_{11} & M_{12} \\ M_{21} & M_{22} \end{bmatrix}\begin{bmatrix} B_{11} & 0 \\ 0 & B_{22} \end{bmatrix} * \begin{bmatrix} M_{11} & M_{12} \\ M_{21} & M_{22} \end{bmatrix}\begin{bmatrix} U_1^- \\ U_2^- \end{bmatrix}_{rhs} \tag{3.36}$$

or in short-hand ; $\mathbf{U}_{lhs} = \mathbf{M}^T.\mathbf{U}_{rhs}$.

In the case of transmission only, then $U_2^-{}_{rhs}=0$ and the overall transmission coefficient T is:

$$T = \frac{1}{\left|M_{11}^T\right|^2} \tag{3.37}$$

In order to use this equation to evaluate the transmission probability, the particle fluxes need to be considered. The transmission coefficient resulting from (3.37) must be multiplied by terms relating the particle velocities in the regions on either side of the overall barrier ie. $k_{rhs}/k_{lhs}(1/|M_{11}^{T}|^{2})$. If the simple ("flat-bands") case is considered, k_{rhs} and k_{lhs} are equal.

By a similar process to that used for the transmission coefficient, the reflection coefficient may be obtained as:

$$R = \left| \frac{M_{21}^{T}}{M_{11}^{T}} \right|^{2} , \tag{3.38}$$

and since from the conservation of flux T + R = 1, then:

$$\left|M_{11}^{T}\right|^{2} - \left|M_{21}^{T}\right|^{2} = \frac{k_{rhs}}{k_{lhs}} \tag{3.39}$$

The Fortran source code for the solution to the above equation (3.37) can be seen in the appendix A.2. The application of equation (3.37) to evaluate the transmission coefficient of the layers used in this Thesis is shown in Figures 3.2 - 3.5. The usefulness of this, considering the shortcomings of the flat-band approach, is limited but it does serve to give an indication of the implications of the layer-thickness variations on the transmission coefficient as shown in Figures 3.2-3.5 and also a feeling for the transmitted current which is a function of this coefficient.

3.3.2 Layer-structure effects on the transmission coefficient

Figures 3.2-3.5 show some of the interesting effects of the layer structure on the transmission coefficient for the ideal case of flat barriers:-

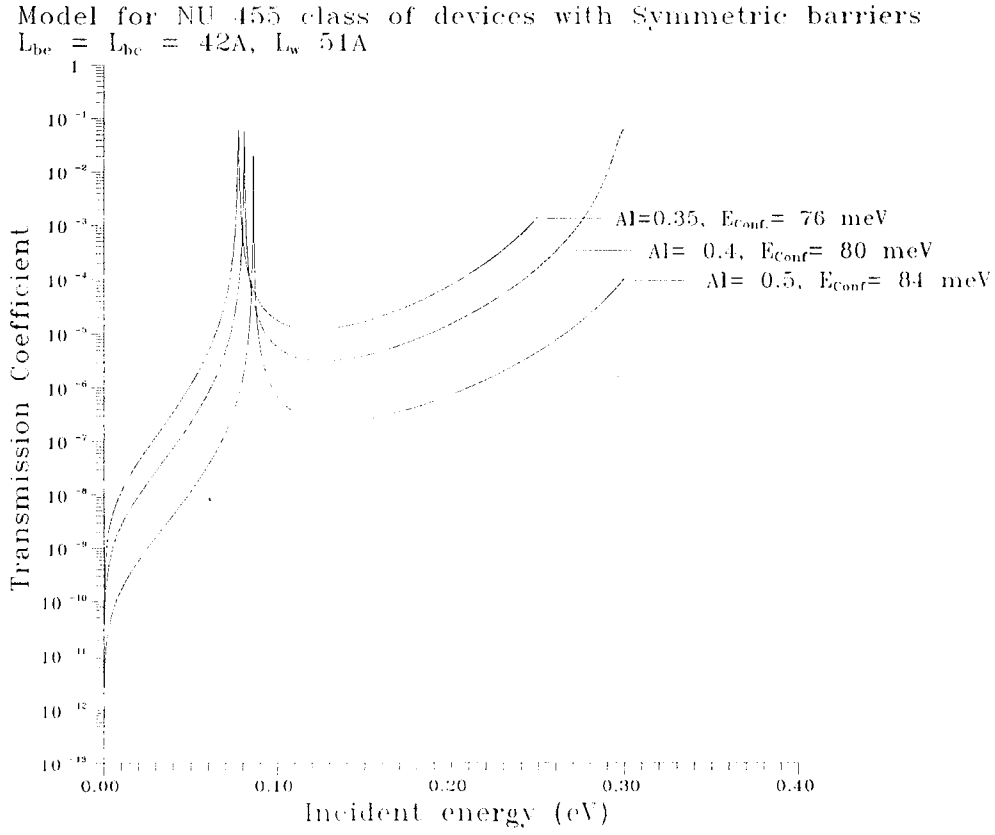


Figure 3.2

In the above figure we can clearly see the effect of the barrier height (via the aluminium fraction) on the position of the confined state in the well. The drop in the position of $E_{Conf.}$ compared to an infinitely high barrier calculation (93meV) results from the penetration of the wavefunction for the electron into the barriers (in the real case) and can represent a significant modification which should not be neglected. The full width half maximum (f.w.h.m.) differs markedly between the above curves and represents the much more significant effect of, for the lower barrier, a broadening in confined state energies. The result of this broadening in the confined states is that more current can pass through the device when it is biased on resonance, all other things being equal.

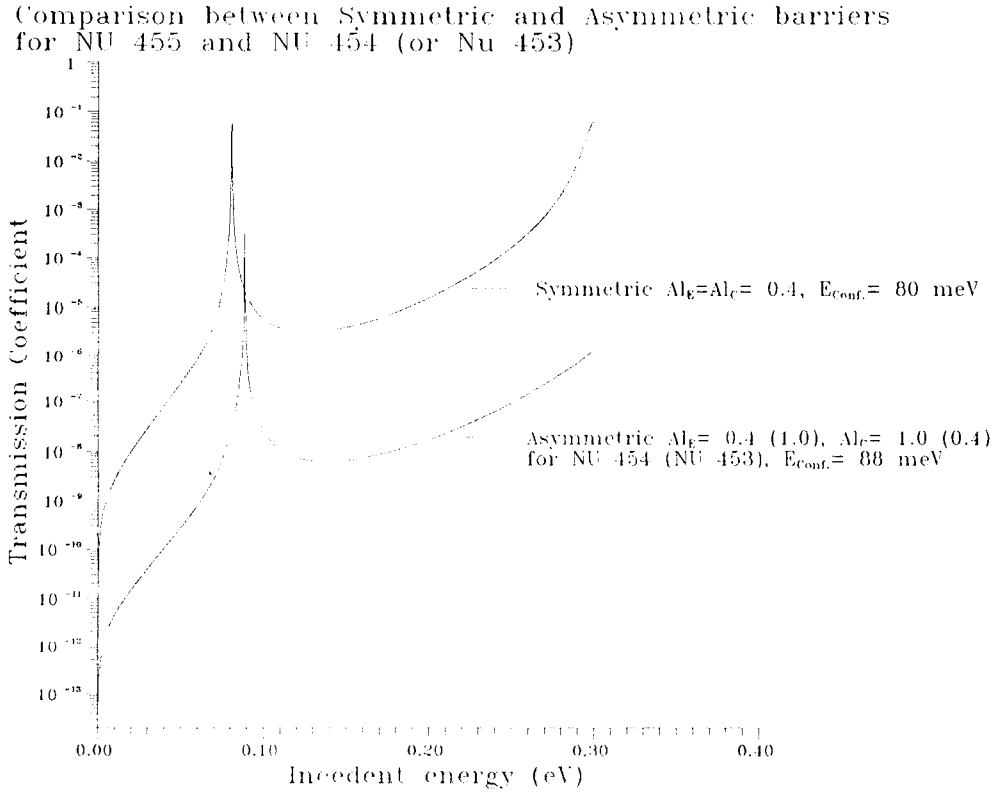


Figure 3.3

The above figure demonstrates the effect of asymmetric barriers on : the overall transmission coefficient, the f.w.h.m. and the position of the confined state in the well with respect to the conduction band edge. The overall transmission coefficient is greatly reduced (by about 300 times), as is the f.w.h.m.. The combined effect is to greatly reduce the current passing through the device and especially the peak current on resonance. The effects on the ratio of the peak-to-valley current are less obvious and cannot be evaluated accurately without some knowledge of the distribution of electrons in the emitter. The position of the confined state in the well is clearly different between the symmetric antisymmetric cases, which should be reflected in the positions of the peak currents seen experimentally.

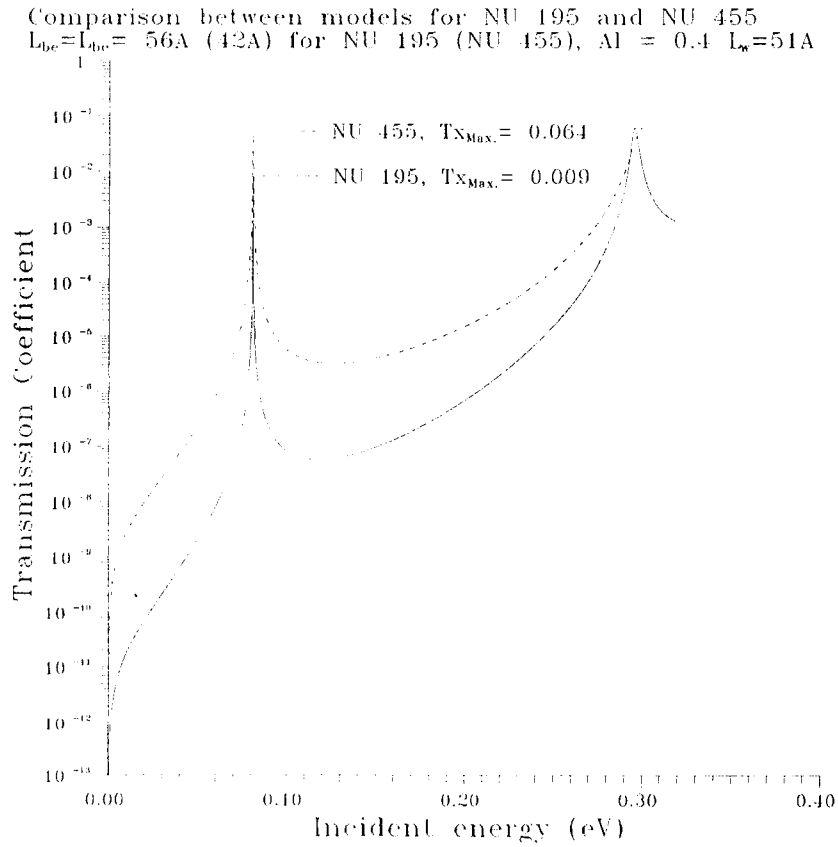


Figure 3.4

In the figure above the difference between wafers NU-195 and NU-455 can be seen. That is, the effect of the increased barrier thickness of wafer NU-195 is to reduce the overall transmission coefficient and to decrease the f.w.h.m.. The combined results of these effects are to reduce the peak current of devices from NU-195 compared with those from NU-455. However it is not so clear how this will affect the peak-to-valley current ratios. The model predicts that the position of the peak currents should not be different, except through unintentional differences in the doping etc.of the two layers, and this is reflected in Figures 2.1(a) versus 2.6(a). In the general case however, where $k_{rhs} \neq k_{lhs}$ it cannot be assumed that all the incident carriers will contribute to the transmitted current without first being scattered. As a result of this various numerical methods are used to calculate the transmission and reflection probabilities and to take account of the degree of scattering.

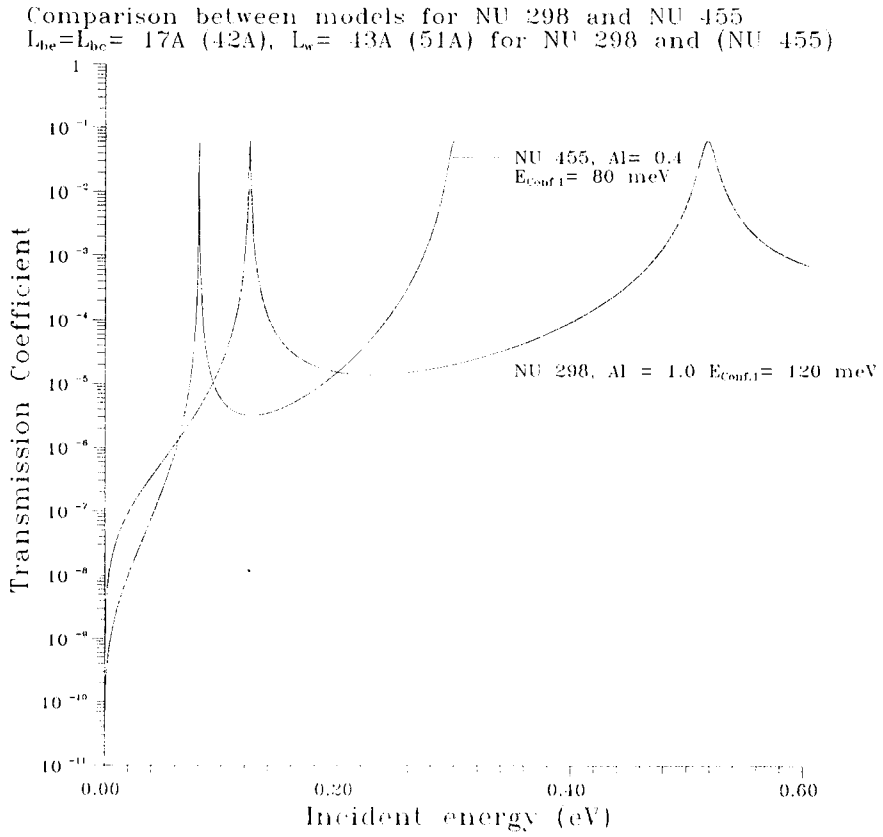


Figure 3.5

The above figure shows the comparison between the NU-455 and the NU-298 class of devices. The position of the confined-state as a result of the difference in well widths can be clearly seen (as is reflected by the positions of the current peaks in Figure 2.2(a) versus 2.6(a)) as can the difference in the f.w.h.m.. Surprisingly, the difference in the overall transmission coefficients is only modest. The increased width of the f.w.h.m for the NU-298 class of devices results in a considerable increase in current (Figure 2.2(a)) through a broadening of the confined-state energies due to the reduced thickness of the barriers compared to the NU-455 class of devices.

3.3.3 Effect of inelastic scattering

The effects of inelastic scattering have been widely investigated by many workers [10, 11, 12, 13]. Generally these authors find that the tunnelling current is independent of the exact nature of the tunnelling mechanism (resonant or sequential) provided that the resonant energy is well-defined (ie. much less than the spread in Fermi-energies in the emitter) [13]. Johnson and Grincwajg (1987) found that for typical experimental parameters the degree of scattering is high and that the tunnelling process is therefore almost completely sequential [10]. This was also reasoned by S Luryi [14] on the basis of observed detectivity of DBRT devices in the THz frequency range [15]. Indeed, Morkoc et al [16] have demonstrated that negative differential resistance can result from tunnelling from three dimensions (emitter) into two dimensions (well), in the absence of resonant enhancement. The dominant transmission mechanism depends on the ratio of the scattering time to the time required for the resonance to build up (resonant-state life time) [17]; if the scattering time is much shorter than the resonant lifetime then the degree of coherence will be reduced accordingly. Calculations which consider the loss of coherence and the distribution of incident carriers, together with a voltage-dependent transmission probability and charge build-up in the well, are not trivial [18]. The following is a brief discussion of how some of these calculations are carried out, leading to an explanation of how scattering is accounted for. The actual calculation for the current through the structure will be presented in section 3.3.4.

In order to gain more insight into the transmission process the transmission coefficient is written in terms of the single barrier case, using the amplitude coefficients ($t = 1/M_{11}^{T}$) rather than particle fluxes ($T = k_{rhs}/k_{lhs}(1/|M_{11}^{T}|^{2})$). The transmission coefficient is:

as ;

$$t = \frac{1}{M_{11}^{T}} = \frac{1}{M_{11}^{e}M_{11}^{c}e^{-ik_wL_w} + M_{12}^{e}M_{21}^{c}e^{ik_wL_w}}, \tag{3.40}$$

which can be rewritten as:

$$t = \frac{\dfrac{1}{M_{11}^{e}M_{11}^{c}e^{-ik_wL_w}}}{1 + \dfrac{M_{12}^{e}M_{21}^{c}}{M_{11}^{e}M_{11}^{c}}e^{2ik_wL_w}}. \tag{3.41}$$

It is more convenient to write (3.41) in terms of the reflection coefficients, which are:

$$r_e^{\leftarrow} = -\frac{M_{12}^{e}}{M_{11}^{e}}, \qquad r_c^{\rightarrow} = \frac{M_{21}^{c}}{M_{11}^{c}}, \tag{3.42}$$

where $r_e^{\leftarrow}$ and $r_c^{\rightarrow}$ are the reflection amplitudes of the left-going (right-going) wave in the well from the emitter barrier (collector). Letting $r_e^{\leftarrow} = |r_e^{\leftarrow}|e^{i\phi e}$ and $r_c^{\rightarrow} = |r_c^{\rightarrow}|e^{i\phi c}$, and then substituting for $R_e = |r_e^{\leftarrow}|^2$, $R_c = |r_c^{\rightarrow}|^2$, $T_e = k_w/k_e|t_e|^2$ and $T_c = k_e/k_w|t_c|^2$, T may be evaluated as:

$$T = \frac{T_eT_c}{1 + R_eR_c - 2(R_eR_c)^{1/2}Cos\,\chi}. \tag{3.43}$$

The total phase change due to the round trip in the well and reflection at each barrier is χ, where $\chi = 2k_wL_w + \theta_e + \theta_c$, and θ_e & θ_c are the phase changes as a result of

reflection from the emitter and collector barriers. The third term in the denominator represents the modification to the transmission coefficient as a result of the finite height of the barriers and the resulting increase in the effective well-width due to the penetration of the wavefunction into the barriers. To evaluate the phase it is useful to express the single barrier matrix elements in terms of complex numbers ie. $M_{11}= M_{22}^{*}= A+iB$ and $M_{12}= M_{21}^{*}= C+iD$. It is also useful to use the flux conservation property: $M_{11}= M_{22}^{*}$, $M_{12}= M_{21}^{*}$. The phase change as a result of reflection at each barrier (θ) is then evaluated by writing the reflection at each barrier (r) in terms of both magnitude and phase:

$$r_c^{\rightarrow} = \frac{M_{21}}{M_{11}} = \frac{C-iD}{A+iB} = \sqrt{\frac{C^2+D^2}{A^2+B^2}}\, e^{-i(\phi_{21}+\phi_{11})} , \tag{3.44}$$

where ϕ_{21} & ϕ_{11} are the matrix element phases and $r_c^{\rightarrow}$ is the reflection amplitude (for the collector barrier in this example) of a right-going wave incident from the left hand (well) side.

The phase change is calculated as:

$$\tan\theta_c^{\rightarrow} = \frac{DA+CB}{CA-DB} = \frac{2k_w k_{bc}(k_{bc}^2+k_c^2)\tanh k_{bc}L_{bc}}{k_{bc}^2(k_w^2-k_c^2)-(k_{bc}^4-k_w^2k_c^2)\tanh^2 k_{bc}L_{bc}} . \tag{3.45}$$

Similarly for the emitter barrier:

$$r_e^{\leftarrow} = -\frac{M_{12}}{M_{11}} = -\frac{C+iD}{A+iB} = \sqrt{\frac{C^2+D^2}{A^2+B^2}}\, e^{i(\phi_{21}+\pi-\phi_{11})} \tag{3.46}$$

where ϕ_{21} & ϕ_{11} are as before and $r_e^{\leftarrow}$ is the reflection amplitude (for the emitter barrier in this example) of a left-going wave incident from the right hand (well) side, and the phase change is:

$$\tan\theta_e^{\leftarrow} = -\frac{AD-BC}{AC+BD} = \frac{2k_w k_{be}(k_{be}^2+k_w^2)\tanh k_{be}L_{be}}{k_{be}^2(k_w^2-k_e^2)-(k_{be}^4-k_e^2k_w^2)\tanh^2 k_{be}L_{be}} . \tag{3.47}$$

Considering now the reflection coefficient, in terms of the amplitude:

$$r = \frac{U_2^{\leftarrow lhs}}{U_1^{\rightarrow lhs}} = \frac{e^{-ik_w l_w} M_{21}^e M_{11}^c + e^{ik_w l_w} M_{22}^e M_{21}^c}{e^{-ik_w l_w} M_{11}^e M_{11}^c + e^{ik_w l_w} M_{12}^e M_{21}^c} \quad . \tag{3.48}$$

This can be re-expressed as

$$r = \frac{\vec{r_e} + e^{2ik_w l_w} \dfrac{M_{22}^e}{M_{11}^e} \vec{r_c}}{1 - e^{2ik_w l_w} \overleftarrow{r_e} \vec{r_c}} \tag{3.49}$$

The picture when scattering is included may now be developed, and we begin by re-writing equation (3.41) as:

$$t = \frac{t_e t_c e^{ik_w L_w}}{1 - \overleftarrow{r_e} \vec{r_c} e^{2ik_w L_w}} \quad , \tag{3.50}$$

We can represent the damping in the well by replacing the factor e^{ikwLw} by $\gamma^{1/2} e^{ikwLw}$. The damping parameter γ is the probability that, after a single well traversal, the electron remains unscattered [19]. The amplitude transfer coefficient then becomes:

$$t = \frac{t_e t_c \gamma^{1/2} e^{ik_w L_w}}{1 - \overleftarrow{r_e} \vec{r_c} \gamma e^{2ik_w L_w}} \quad . \tag{3.51}$$

For the reflection coefficient, from equation (3.49), including damping we get:

$$r = \frac{\vec{r_e} + \gamma\, e^{2ik_w l_w} \dfrac{M_{22}^e}{M_{11}^e} \vec{r_c}}{1 - \gamma\, e^{2ik_w l_w} \overleftarrow{r_e} \vec{r_c}} \quad . \tag{3.52}$$

This results in a modification to the coherent transmission coefficient, as follows:

$$T_{coh} = \frac{T_e T_c \gamma}{1 + \gamma^2 R_e R_c - 2(R_e R_c)^{1/2} \gamma Cos\chi} \tag{3.53}$$

This may be compared with (3.43) for zero scattering. Similarly, for the reflection coefficient in terms of particle fluxes,

$$R_{coh} = \frac{R_e + \gamma^2 R_c - 2\gamma (R_c R_c)^{1/2} Cos\chi}{1 + \gamma^2 R_c R_e - 2\gamma (R_c R_c)^{1/2} Cos\chi} \,. \tag{3.54}$$

3.3.4 Evaluation of D.C. current through a DBRT

The current density is the sum of the number of electrons tunnelling through a unit area of the barrier multiplied by their velocity :

$$J_{LR} = \Sigma F(k).(-ev_{LR}) \tag{3.55}$$

where the summation is over electron k states and v_{LR} is the velocity from left to right (ie. emitter to collector). The calculation must take account of the double barrier transmission coefficient, the number of electrons which have sufficient energy to tunnel to the collector (Figure 3.6) and the probability that there is an available unoccupied state in the collector. This latter factor is given by $(1 - f_r(E_r))$ where E_r is the energy of an electron in the collector.

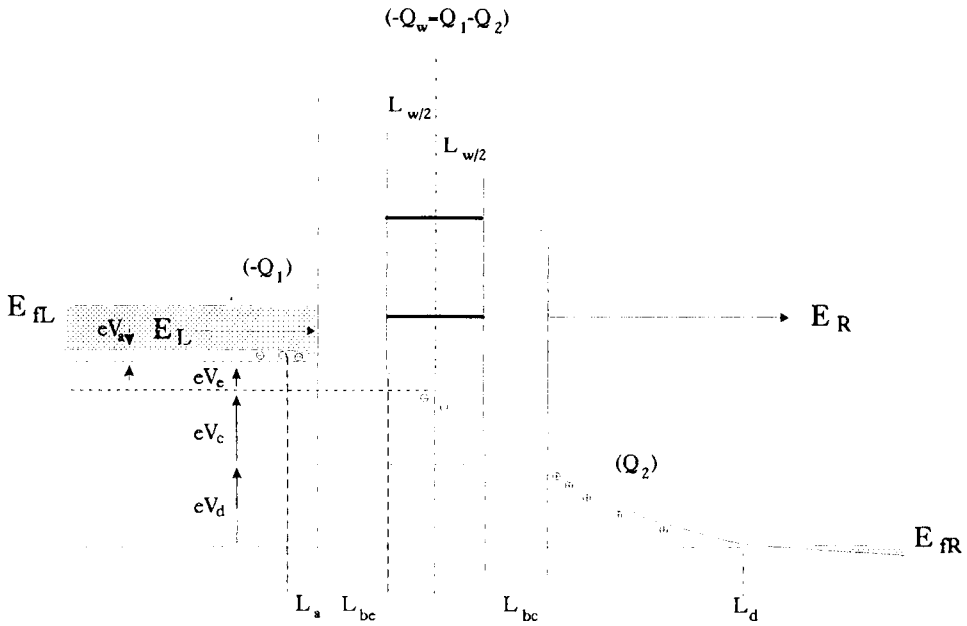


Figure 3.6 Representation of the conduction band under bias and the Voltage and Energy distribution.

According to Duke (1969) [20];

$$f_l(E_l)=(1+e^{\beta(E_l-E_{fl})})$$
$$f_r(E_r)=(1+e^{\beta(E_r-E_{fr})}) \tag{3.56}$$

where the subscript l denotes the left (emitter) side and E_f is a fermi level from Figure 3.6, $E_l=E_r+E_{fl}-E_{fr}-eV$, and V is the applied bias. To carry out this calculation the procedure is as follows:

The volume of k-space per k value is $\Delta k=8\pi^3/V$ and the volume of k-space per electron (since each k can accommodate 2 electrons) is $\Delta k=8\pi^3/2V$. So $\Sigma F(k)=V/6\pi^3\Sigma F(k)\Delta k$, and as $\Delta k\rightarrow 0$ then:

$$\frac{1}{V}\sum_{V\to\infty} F(k)=\int\frac{1}{6\pi^3}F(k)dk \ . \tag{3.57}$$

Hence, knowing that the velocity of the electron is $v_x=\hbar k_x/m^*$, then

$$J_{LR}=-\frac{e}{6\pi^3\hbar}\int dk_l^2 f_l(E)\,(1-f_r(E))\,T_{tot}(E_x)dE_x \ . \tag{3.58}$$

But $d^2k_l=(2\pi m^*/\hbar^2)dE_l$, so:

$$J_{LR}=-\frac{em^*}{2\pi^2\hbar^3}\int dE_l f_l(E)\,(1-f_r(E))\,T_{tot}(E_x)dE_x \ . \tag{3.59}$$

Similarly for current flow from right to left:

$$J_{RL}=-\frac{em^*}{2\pi^2\hbar^3}\int dE_l f_r(E)\,(1-f_l(E))\,T_{tot}(E_x)dE_x \ . \tag{3.60}$$

But since T_x is the same in both directions, then $J_T=J_{LR}-J_{RL}$, and the total current is

therefore:

$$J_T = -\frac{em^*}{2\pi^2 \hbar^3}\int dE_\parallel \, [f_l(E) - f_r(E)] \, T_{tot}(E_x) dE_x \tag{3.61}$$

If at zero bias $E_l = E_r$ and $E_{fl} = E_{fr} = E_f$ ie similar doping on either side, then using the relations in equation (3.56),

$$J = -\frac{em^*}{2\pi^2 \hbar^3}\int dE_\parallel \, [f(E) - f(E+eV)] \, T_{tot}(E_x) dE_x \ . \tag{3.62}$$

This is more often written as;

$$J(E_x) = -\frac{em^* kT}{2\pi^2 \hbar^3} Ln\left[\frac{1 + e^{\beta(E_f - E_x)}}{1 + e^{\beta(E_f - E_x - eV)}}\right] \int T_{tot}(E_x) dE_x \ . \tag{3.63}$$

T_{tot} in this case is the overall transmission coefficient, given by the sum of the coherent and sequential particle transmission coefficients. The sequential coefficient is simply the difference between the coherent transmission and reflection coefficients (the sum of which no longer equals unity) multiplied by the probability of this flux making its way to the collector rather than back to the emitter. This is given by:

$$T_{seq} = (1 - T_{coh} - R_{coh})\left(\frac{T_c}{T_e + T_c}\right) \ . \tag{3.64}$$

The results of equations 3.63 and 3.64 can then be calculated using a computer [18]. Such an example is shown in Figures 3.7 and 3.8 for a device with a similar layer structure as NU-455. Figure 3.7 shows the measured current-voltage characteristic together with the theoretically calculated current for a 20μm diameter device at a temperature of 300K, while Figure 3.8 shows the same device at 77K.

The agreement between the theoretical current-voltage characteristic and the measured characteristic is good, except for the position and shape of the current peak. In order to achieve a match between the magnitude of the current peak in the theoretical case and that measured required the height of the barriers in the theoretical model to be reduced slightly. This was achieved by reducing the aluminium concentration in the barriers from 40% to 35%. In reality the aluminium concentration in the barriers would remain similar to the value used during the wafer growth, and the lower value indicated by the theoretical model is thought to reflect effects such as barrier-lowering.

The apparent barrier-lowering is thought to arise due to the sensitivity of the thin barriers to (dopant) charge which diffuses into these otherwise undoped regions during growth. Electrical charge redistribution also occurs throughout the double barrier region due to the differing levels of doping in adjacent layers and this will also affect the height of the barriers. The relationships of 2.1 (a&b) have also been investigated experimentally only for relatively thick layers (usually many ten's of nanometres) and it is unknown if the same relationships would also hold for very thin barriers.

The different shape of the measured and calculated characteristics in the region of the NDR (Figure 3.7 & 3.8) results mainly from oscillation and self-rectification which occurs only in the case of the measured current-voltage characteristic. The differences in the position of the current peak (for the measured and calculated cases) is thought to be due to the exact conduction band profile in the vicinity of the emitter barrier. A more accurate analysis of the problem would require a fully self-consistent solution of both the Schrödinger and Poisson equations throughout the emitter accumulation and barrier regions.

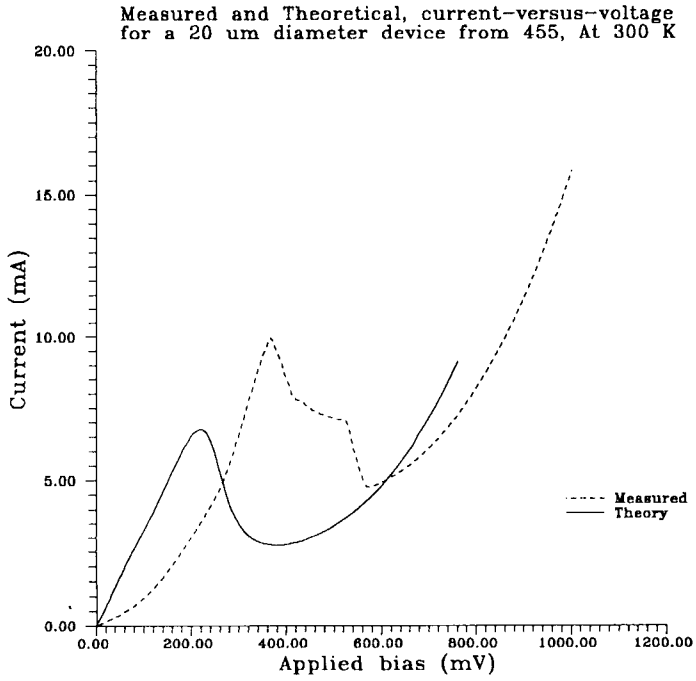


Figure 3.7 Comparison between the measured and calculated d.c. characteristics, at 300K

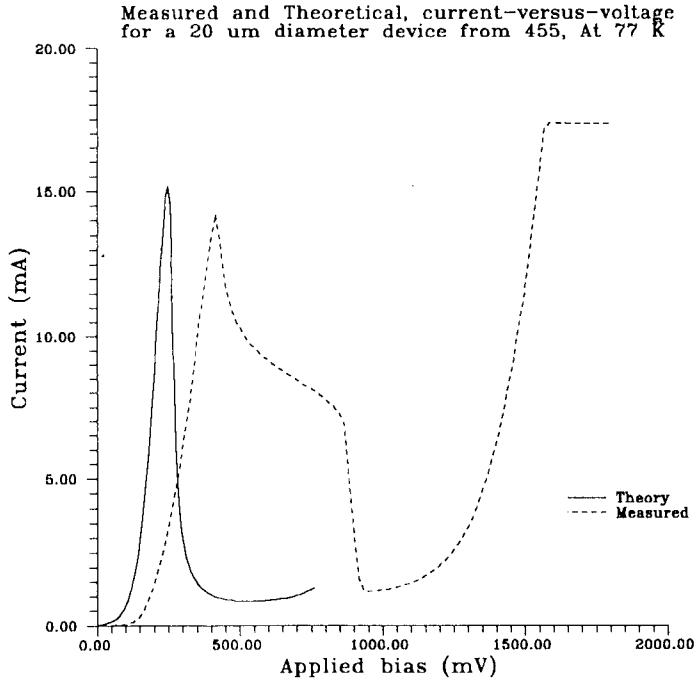


Figure 3.8 Comparison between measured and calculated d.c. characteristics, at 77K.

Similar arguments apply when comparing the current-voltage characteristics at the higher temperature of 300K; the main difference being the shape of the theoretical characteristic below resonance. This is thought to highlight a problem with the computer calculation and is associated with the conduction band profile in the region adjacent to the emitter barrier. This represents a significant source of error in the theoretical calculation of the differential resistance, which would otherwise be very useful for high frequency modelling from first principles (see sections 4.4 and 4.5).

From Figure 3.7 & 3.8 it can be seen that the theoretical evaluation of the current-voltage characteristic for a particular layer structure, can (with some reservations) yield quite an acceptable "first-guess" at the eventual current-voltage profile for an actual device and this, in turn, can assist with layer optimisation and limited high frequency design.

3.3.5 Distribution of the applied voltage across the device

A calculation of the exact voltage distribution throughout a DBRT device is far from trivial, ideally requiring the self-consistent solution of the Poisson and Schrödinger equations throughout the device taking into consideration the point-to-point variations in the conduction band profile and electron density. Such studies have been carried out by several workers [21, 22, 23] who found that the band-bending of the conduction band in the spacer layers adjacent to the emitter barrier (accumulation region) can profoundly affect the voltage distribution through the entire device.

The effect on the current-voltage characteristic is mainly through the distribution of the electron density in the emitter as a function of energy and applied voltage and under some bias conditions a third barrier in the emitter may be formed (Figure 3.9).

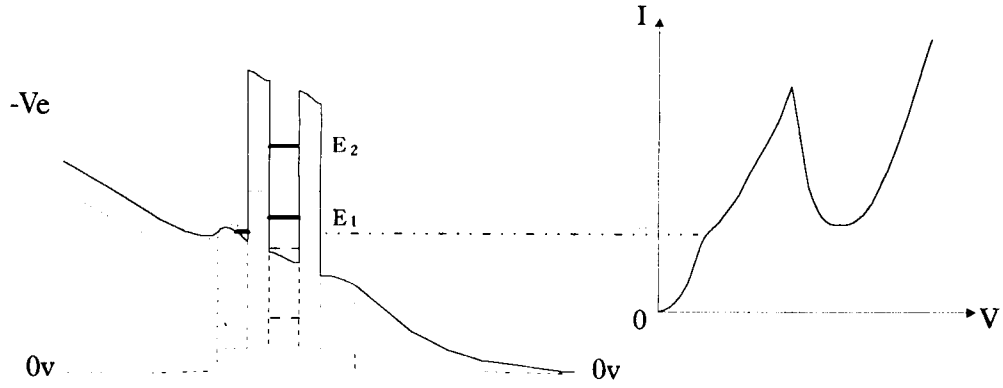


Figure 3.9 Shows the effect of bias on the formation of a third barrier in the emitter and how this manifests itself on the current-voltage characteristic

The effect of the formation of the third barrier on the tunnelling current is a small dog-leg in the resulting current-voltage characteristic at a lower voltage than that of the resonant current peak corresponding to the first confined state in the well. For a practical example of this phenomena see Figure 3.3 (a&b) in Chapter 2.

Exact calculation of the accumulation length versus the applied voltage would be very useful, but if this calculation were to accommodate the formation of a two-dimensional confined state in the accumulation region under certain (high) bias conditions and the possibility of formation of a third barrier as discussed above, then the calculation would be very complicated indeed [23]. Techniques based on the

methods of Fang and Howard [24, 25] have been used to gain an approximate value for the voltage dropped across this region [26], although these are not self-consistent in the true sense and are not sufficient to describe the behaviour over a wide range of temperatures.

At room temperature, since the degree of degeneracy is only modest for the typical levels of doping ($2*10^{17}cm^{-3}$) used in these samples, the screening length which we shall use is the Debye screening length (~96Å for $2*10^{17}cm^{-3}$) which is considered in addition to any undoped spacer lengths. Hence, the overall accumulation length is of the order of 100-150Å (50Å spacers) at low bias, and is thought to remain fairly constant even up to fairly high biases. The voltage dropped across the Debye screening length is simply given by the field developed across the emitter barrier (which in turn is dependent on such effects as charge stored in the well of the DBRT), together with the field across the collector barrier and collector contact depletion regions. Unfortunately, as a result of the voltage-dependent charge build-up in the well, the voltage distribution across the DBRT needs to be calculated by a self-consistent method. The calculation of the voltage distribution across the DBRT in the computer program used for this study [18] is carried out as follows:-

The field across the accumulation region is calculated by first choosing a voltage across this region; the applied voltage is calculated subsequently as a result of this emitter voltage step. From a knowledge of the field across the emitter barrier, and initially assuming that this field is similar to that across the collector barrier (ie. no charge build-up), then we can calculate the field at the edge of the depletion region in the collector contact. By using Poisson's equation the length of the depletion region and the accompanying voltage drop can then be calculated. As a result of the field across the emitter barrier for the chosen incident energy, and hence the resulting field across the double barrier region, the transmission coefficient and current through the device can be calculated. These calculations will also give the applied voltage across the device for this level of current from the sum of the combined voltage drops (Figures 3.7 & 3.8). The calculation is then repeated, but now including any resulting

charge build-up in the well, until successive calculations converge. This process is then repeated over the range of incident energies to give the overall current-voltage characteristic.

In detail, this is achieved (referring to Figure 3.6) by letting V_e be the voltage across the emitter ($l_e=L_a+S_e+L_{be}+L_w/2$) and equating the fields induced across the other layers such that the field across the collector, plus that due to any charge stored in the well, equals the field across the emitter (S_c & S_e are the lengths of the spacer layers). ie.

$$E_e = E_c + \frac{Q_w}{\varepsilon_r \varepsilon_0} \quad , \tag{3.65}$$

where $l_c=L_w/2 + L_{bc}+S_c$ and L_a is the accumulation length which is taken to be approximately equal to the Debye screening length. Similarly the field across the depletion region, which is calculated using Poissons equation, is equated with the field across the collector giving the voltage across the depletion region, giving:

$$V_d = \frac{\varepsilon_r \varepsilon_0 E_c^2}{2eN_d} \quad . \tag{3.66}$$

As discussed earlier, the charge in the well (Q_w) is calculated by an iterative process and the potential distribution is adjusted accordingly. Figure 3.6 shows the potential distribution across a typical device and Figures 3.7 and 3.8 show an example of the current-voltage characteristic for a typical symmetric-barrier device (from wafer NU-455).

From Figures 3.7 and 3.8, it can be seen that the match between the magnitude and position of the peak in transmission for the experimental and calculated current-voltage characteristics is by no means exact. The shift in the position of the current peak along the voltage axis is due to a combination of voltage drops from a number of sources, together with other inaccuracies in the calculation. One obvious voltage drop, which is not considered using the present model, is across the excess contact

resistances in the collector. In addition, there will also be differences between the doping levels in the depletion region which are assumed for the purposes of calculation (most notably the doping gradients) and the doping levels (possibly varying by a factor of two) which actually occur. These differences will lead to inaccurate depletion lengths. Inaccuracies in the position of the confined state in the well with respect to the emitter fermi level will also occur as a result of the assumed barrier heights and widths being slightly different from the actual barriers. Finally, inaccuracies will also occur in the width of (and therefore voltage dropped across) the accumulation layer in the emitter contact which are again a result of inaccurate modelling of the exact doping profile in the emitter adjacent to the barriers.

It is with regard to the penultimate source of error listed above that thermally activated resonant tunnelling (TART) studies were undertaken. The physical barrier thicknesses could have been measured using transmission electron microscopy, but the "electronic" width would not necessarily be the same as the physical thickness and, furthermore, the heights of the barriers would still be unknown. These barrier heights are traditionally calculated (Chapter 2.1 (a&b)) from a knowledge of the aluminium fraction in the barriers. However, it was suspected that for the thinner barriers used in this study these calculated heights may have exceeded their actual value. Comparison between the position of the measured confined-state energy (as obtained from the TART studies) and those of a simple flat-band transfer-matrix calculation (3.3.2), should allow the actual barrier heights to be confirmed.

3.3.6 Thermally activated resonant tunnelling studies

The theory of thermally activated resonant tunnelling (TART) has been discussed by Leadbeater and Sheard [26, 27]. At any temperature other than absolute zero there will be a distribution in energy of the carriers in the emitter contact, rather than a well-defined level which separates occupied from un-occupied levels. As the temperature increases the density of the electrons as a function of energy spreads out to cover a broader range of energies (Figure 1.7). At higher temperatures, there may

be sufficient numbers of electrons which are already at the resonant energy in the high-energy tail of the distribution. The application of only a small external applied voltage will disturb the equilibrium and so permit these (resonant) electrons to move to the collector and cause a current to flow. Hence, by varying the temperature at several fixed voltages below resonance, we can evaluate the position of the resonant energy with respect to the fermi level in the emitter.

For the level of doping used in these samples (and for the sake of simplicity), we assume that the position of the fermi energy in the emitter is constant over the range of temperatures studied. As can be seen from Table 3.1, this assumption may need to be viewed with caution for some levels of doping. Another source of error is that at very low biases (equivalent to less than kT) the possible flow of electrons (and hence current), will depend on the occupancy of the available levels in the collector contact. This will cause the plots of Ln(J/T) versus (1/T) to deviate from the predicted behaviour. Also, at voltages above that required to achieve resonance the possibility of excess current as a result of electrons travelling either over the barrier, or through a second resonant state, will produce a deviation with the predicted behaviour.

Returning to equation (3.63) , and expressing it with respect to a saturation current (J_0)

$$J = J_0 T Ln\left[\frac{1+e^{\beta(E_f-E_{xl})}}{1+e^{\beta(E_f-E_{xr}-eV)}}\right]. \qquad (3.67)$$

Considering only the higher-energy electrons in the tail of the Fermi-Dirac distribution ($E_f - E_x \gg kT$), and also using a sufficiently high bias that the occupancy of the collector levels is very low ($eV \gg kT$), then equation (3.67) reduces to;

$$Ln\left(\frac{J}{T}\right) = Ln(J_0) - \frac{E_{xl}}{kT} \qquad (3.68)$$

Hence a plot (Figure 3.10) of Ln (J/T) versus (1/T) should yield a straight line with

a gradient $(-E_{xl}/k)$. By repeating this for several biases and plotting E_{xl} as a function of this voltage, and extrapolating E_{xl} to zero volts (Figure 3.11), this should give an approximation to the position of the confined state energy with respect to the Fermi level in the emitter. These comparisons have been made for the layers used in this study and are summarised in Table 3.3.

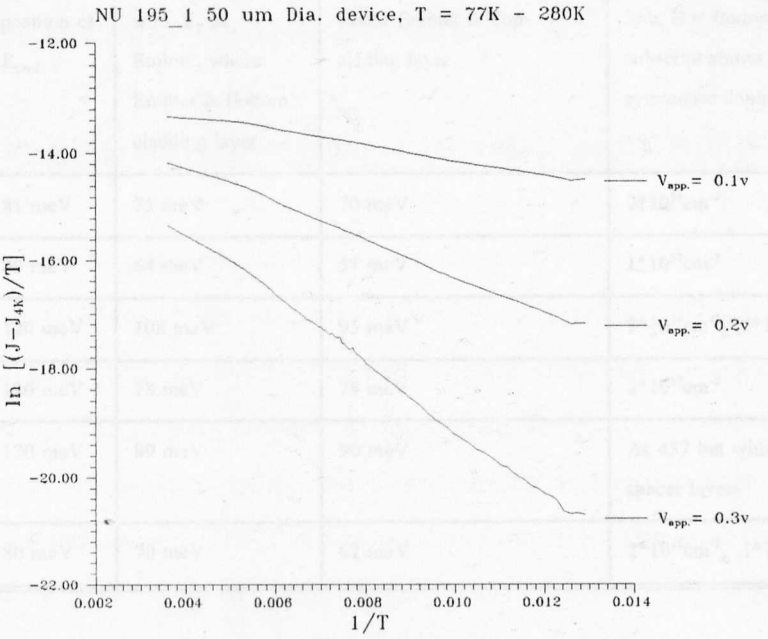


Figure 3.10 Plot of Ln(J/T) versus 1/T for three different biases

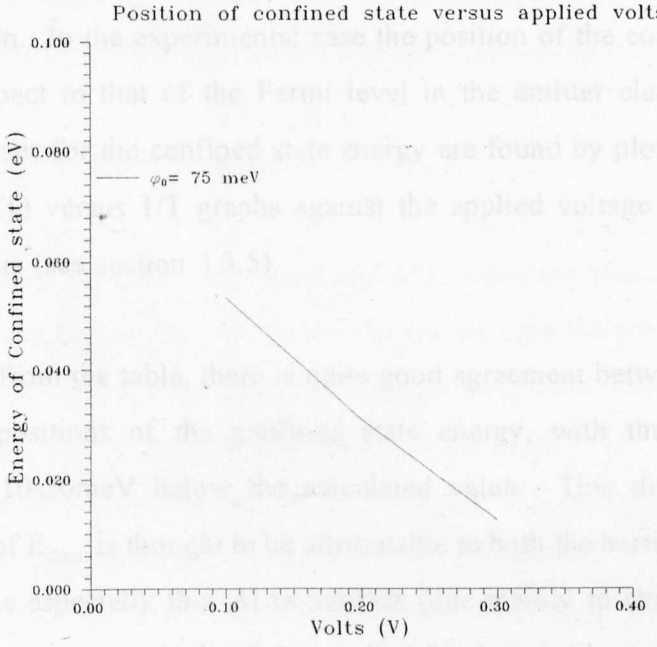


Figure 3.11 Plot of Gradient versus applied voltage

Layer Number	Calculated (Ideal) position of $E_{Conf.}$	Measured position of $E_{Conf.}$ @ 0V w.r.t. E_F in Emitter, where Emitter is Bottom cladding layer	Measured position of $E_{Conf.}$ @ 0V w.r.t. E_F in Emitter, where Emitter is Top clading layer	Doping of cladding layers: Sub.T = Top layer Sub. B = Bottom layer No subscript shows symmetric doping
195	81 meV	75 meV	70 meV	$2*10^{16}cm^{-3}$
455	80 meV	64 meV	57 meV	$1*10^{17}cm^{-3}$
366	120 meV	108 meV	95 meV	$5*10^{16}cm^{-3}_B$,$2*10^{18}cm^{-3}_T$
457	120 meV	78 meV	78 meV	$2*10^{17}cm^{-3}$
462	120 meV	89 meV	90 meV	As 457 but with 25A u.d. spacer layers
469	80 meV	70 meV	62 meV	$2*10^{16}cm^{-3}_B$,$1*10^{17}cm^{-3}_T$

Table 3.3

Table 3.3 shows a comparison of the position of the confined state in the well using the flat-band (unbiased) transmission coefficient model with the experimentally evaluated position. In the experimental case the position of the confined state in the well is with respect to that of the Fermi level in the emitter cladding layer. The experimental values for the confined state energy are found by plotting the gradients (Φ) of the Ln(J/T) versus 1/T graphs against the applied voltage and extrapolating these to the y-axis (see section 3.3.5).

As may be seen from the table, there is quite good agreement between the measured and calculated positions of the confined state energy, with the measured value typically being 10-20meV below the calculated value. This discrepancy for the measured value of $E_{Conf.}$ is thought to be attributable to both the barrier fore-shortening in the case of the especially thin AlAs barriers (due mainly to charge redistribution and to a lesser extent as a result of the applied bias) and the position of the Fermi level in the emitter layer relative to the conduction band edge and hence the confined state in the well.

Some further points arising from the TART study will now be considered :

(I) Effect of emitter doping on the position of $E_{Conf.}$

Comparing the various measured values of $E_{Conf.}$ shown in Table 3.3, it may be seen that for different wafers: NU-195 and NU-455 where $E_F \approx$-8.4meV and $E_F \approx$-0.4meV respectivley, the 10meV difference in $E_{Conf.}$ is approximately due to the differences in the respective Fermi level positions. This conclusion is vindicated in the case of asymmetric doping (NU-469, NU-366) where the position of $E_{Conf.}$ with respect to the Fermi level in the emitter is clearly dependent on the level of doping in the emitter and which is now dependent on which side of the DBRT is acting as the emitter. The slight residual bias-dependent differences in the position of the confined state in the nominally symmetrically doped wafers (NU-195 & NU-455) of 5-7meV is probably due to slight growth-direction dependent features which alter the exact position of the conduction band edges, and hence the distribution of electrons at the interface to the barriers from the emitter contacting layers and tends to be exacerbated by the lower resonant energy compared to NU-457 and NU-462.

(II) Effect of well thickness on position of $E_{Conf.}$

In the case of wafers NU-195 and NU-455 where the aluminium fraction and therefore the barrier heights are similar (as also are the well widths), there is only a very slight modification in the calculated position of the confined state in the well, due to the different barrier thicknesses (NU-195: 56Å, NU-455: 42Å). However, the position of the confined state energies for NU-455 and NU-366 differ markedly. This is simply a reflection of the different well widths ie. 51Å for NU-195 and NU-455 class of devices, and 43Å for the NU-366/457/462 class.

(III) Effect of spacer layers on position of $E_{Conf.}$

The presence of spacer layers appears to shift the position of the confined state to a higher energy relative to the fermi energy in the emitter, as can be seen between the measured results of wafers NU-457 and NU-462. The reason for this is suspected to be a combination of an additional slight extra voltage drop across the wider accumulation region (formed in the emitter due to the presence of the un-doped spacer layer), and some slight zero biased band-bending near the barriers due to the charge redistribution as a result of the differences in doping. The result of these effects is to raise the apparent position of $E_{Conf.}$ with respect to the Fermi level in the emitter.

3.4 Theory of high-frequency resonant tunnelling

3.4.1 Charge build-up in the well on resonance

An important factor in determining both the accurate voltage distribution throughout a DBRT device and some of their high frequency characteristics is the charge build-up in the well as a function of the applied voltage. The charge build-up in the well-region is as a result of the presence of both the coherent electron wavefunction and the non-coherent (scattered) electrons prior to their tunnelling out into the collector. Hence, for most practical semiconductors at room temperature, the degree of scattering in the well is the most significant contribution to charge build-up in the well. The coherent charge, $Q_{Coh.}$, (in the well) is given by the integration of the charge density in the well (or the integration of the wave function in the well) with respect to the applied voltage [18]. Thus:

$$Q_{coh} = e\int_0^{L_w} |\psi|^2 dx \tag{3.69}$$

at each incident well energy, which according to Booker [19] gives;

$$Q_{coh}(E) = \frac{eLwT_e\Gamma}{(1-\gamma R_e^{1/2}R_c^{1/2})^2 + 4\gamma R_e^{1/2}R_c^{1/2}Sin^2\phi} \tag{3.70}$$

for the coherent charge density where Γ represents the width of the confined state in the well. Γ is given by;

$$\Gamma = \frac{(1+\gamma R_c)(1-\gamma)}{-Ln\gamma} + \frac{(R_{coh}^{1/2}\gamma Sin(2k_wL_w - \theta_e) + Sin\theta_e)}{k_wL_w} \ . \tag{3.71}$$

The sequential charge density is simply the product of the sequential current and the time for this charge to tunnel through the collector barrier, τ_c or:

$$Q_{seq}(E) = J_{seq}(E)\,\tau_c(E) \ . \tag{3.72}$$

The decay rate (τ_c^{-1}) of the charge in the well is the time that the electron takes to make one traversal of the effective well-width multiplied by the tunnelling probability. This is:

$$\tau_c^{-1} = \frac{\frac{\hbar k_w}{m_w^*}}{2\,(L_w + k_{be}^{-1} + k_{bc}^{-1})}\,T_c \tag{3.73}$$

where, $\hbar k_w/m_w^*$ = velocity of an electron in the well and $(L_w + k_{be}^{-1} + k_{bc}^{-1})$ is the effective well width. T_c is the transmission coefficient through the collector barrier.

Hence the total charge is the sum of the sequential and the coherent charges:

$$Q_{tot} = Q_{seq} + Q_{coh} \quad . \tag{3.74}$$

It is these relationships that have been used to calculate the self-consistent voltage distribution through a DBRT device by including the effects of charge build-up in the well.

S. Luryi [14] considered the coherent state lifetime and came to the conclusion that the fundamental speed limit of a DBRT, as a result of this lifetime, was not appropriate in determining the frequency response of the devices used by Sollner [29]. These findings are consistent with the predominantly sequential picture of tunnelling where it is the tunnelling time of the sequential charge through the collector barrier which usually determines the limit of the frequency response [28,30].

The importance of the collector barrier in the sequential tunnelling picture is not surprising since usually this barrier has the greatest field across it and, as a result, is often the most "transparent". To study accurately the behaviour of the charge as a function of frequency would require a time-dependent solution of the Schrödinger equation for the barriers, the well region, and the adjacent layers including the accumulation region. This time dependent solution would also need to be solved self-consistently with the solution of the Poisson equation across the complete structure. This is a complex undertaking which has yet to be compared directly with both experimental results and from a theoretical point-of-view, and has only been performed in part by a few groups world-wide [31, 32].

In the light of these problems the small-signal response of the DBRT devices has more often been calculated using a steady-state solution for the Schrödinger equation for the barrier and well regions (tunnelling is considered to be instantaneous for the experimental case), but considering the time-dependent redistribution of charge throughout the structure (ie. the charge separation lengths and associated

conductances). The structure is then modelled in the form of reservoirs of charge which are separated by characteristic lengths in parallel with specific values of conductance [33]. This approach is based on the sequential description of tunnelling where the evaluation of the various components tends to be quite intuitive. A more detailed description of the approach is described below.

3.4.2 Small-signal A.C. response: the sequential tunnelling model.

The frequency dependence of the small-signal impedance of a DBRT diode is approximated by the following analysis, in which the amplitude of the a.c. signal is considered small enough that the barrier heights remain constant. This approach is still thought to hold for the relatively low frequencies studied here, and extensive data (Chapter 4) has been collected to support these arguments. The basis for this confidence is the assumption that the transit-time for the electron through each barrier is very much shorter than the period of the high frequency signal.

The DBRT structure for this model is considered as two capacitors with a common central plate. The negative charge contained in the accumulation and well regions is terminated on the positive charge of the depletion region. Associated with these reservoirs of charge are parallel conductances which depend on the transmission through the emitter and collector barriers [33].

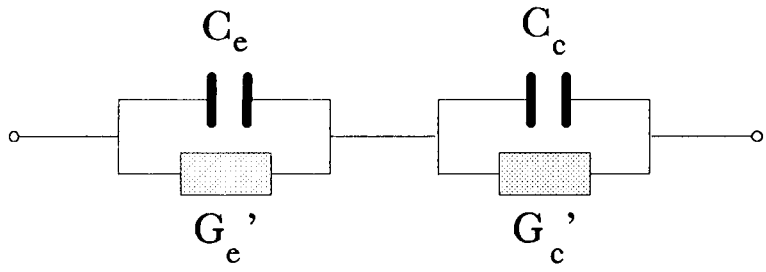


Figure 3.12 Equivalent circuit representation arising from the sequential tunnelling model of Sheard & Toombs [33]

With reference to Figure 3.12, the current through the collector barrier is given by;

$$I_c = \frac{Q_w}{\tau_c} \tag{3.75}$$

where τ_c^{-1} is the decay rate through the collector barrier, given by equation (3.73). The current through the emitter barrier is much more difficult to calculate, since this depends on the decay rate through the emitter barrier and also on the occupancy of the available states in the emitter. I_e is given by:

$$I_e = f(V_e) - (\frac{Q_w}{\tau_e}) \tag{3.76}$$

where $f(V_e)$ is a function which is dependent on the energy range of available states in the emitter, their occupancy and the level broadening of the confined state in the well [34]. The decay rate through the emitter barrier (τ_e^{-1}) is calculated in a similar

way to that for the collector barrier. For these equations to hold it is assumed that the tunnelling time through the barriers is effectively instantaneous compared to the period of the signal. At d.c., $I = I_e = I_c$, giving

$$I = \frac{\tau_c^{-1}}{\tau_e^{-1} + \tau_c^{-1}} f(V_e) \ . \tag{3.77}$$

From charge continuity the charge stored in the well is:

$$Q_w = Q_c - Q_e \ , \tag{3.78}$$

and the voltage distribution is:

$$V = V_e + V_c = \frac{Q_e}{C_e} + \frac{Q_c}{C_c} \ . \tag{3.79}$$

Expressing the oscillating voltage in exponential terms ($\tilde{V} = Ve^{i\omega t}$), and then considering only the small (differential) a.c. component. δV is then

$$i\omega \delta Q_w = \delta I_e - \delta I_c \tag{3.80}$$

where δI_e is given from equation (3.76) by:

$$\delta I_e = \frac{df}{dv_e} \delta V_e - \frac{\delta Q_w}{\tau_e} \ . \tag{3.81}$$

From this we can evaluate

$$\delta Q_w = \frac{\delta V_e R_{chg}^{-1}}{i\omega + \tau_0^{-1}} \ , \tag{3.82}$$

where $R_{chg}^{-1} = (df/dV_e)$ and is the conductance which controls the charging of the well or $R_{chg} = (\tau_{chg}/C_e)$, and $\tau_0^{-1} = \tau_e^{-1} + \tau_c^{-1}$.

The impedance is split into two parts ($Z(\omega) = Z_e(\omega)+Z_c(\omega)$), where $Z_e(\omega) = \delta V_e/\delta I$ and $Z_c(\omega) = \delta V_c/\delta I$. Using the continuity of charge relationships ($dQ_e=(I-I_e)$ and $dQ_c=(I-I_c)$) leads to:

$$Z_e^{-1} = i\omega C_e + \frac{1}{R_{chg}} \frac{i\omega + \tau_c^{-1}}{i\omega + \tau_0^{-1}} \tag{3.83}$$

for the emitter barrier. Similarly, for the collector barrier:

$$Z_c^{-1} = i\omega C_c + \frac{1}{R_c} \frac{\tau_{chg}^{-1}}{i\omega + \tau_0^{-1} + \tau_{chg}^{-1}} \tag{3.84}$$

where $R_c = (\tau_c/C_c)$. Equations (3.83) and (3.84) can be represented in conventional form shown in Figure 3.12 where G_e' and G_c' are the inverse of the right-most terms on the right hand side of these equations and R_{dc} [33] is:

$$R_{dc}^{-1} = \frac{\frac{\tau_c^{-1}}{\tau_0^{-1}} \frac{C_c}{C_e + C_c} R_{chg}^{-1}}{1 + \frac{\tau_0}{C_e + C_c} R_{chg}^{-1}} . \tag{3.85}$$

In the above expression, τ_e, τ_c, C_e and C_c can be calculated using a computer model [18] which yields the tunnelling rates and the voltage distribution throughout the device, and hence the charge-separation lengths. The application of these equations (3.83-3.85) to the high frequency behaviour of the devices studied in this Thesis is discussed in the latter part of the following chapter.

3.5 References:

[1] Riechert, H., Bernklau, D., Reithmaier, J. & Schnell, R. (1990). MBE growth and post annealing of GaAs based resonant tunnelling structures, viewed in relation to interface roughness., 6th International Conference on MBE, San Diego.

[2] Liu, H.C. & Coon, D.D. (1988). Interface roughness and island effects on tunnelling in quantum wells. *J. Appl. Phys* **64**(12), 6785-6789.

[3] Rudberg, B. (1990). Interface roughness and asymmetric current-voltage characteristics in resonant tunnelling. *Semicond. Sci. Technol.* **5** 600-603.

[4] Cheng, P. & Harris, J. (1989). Effect of Si doping in AlAs barrier layers of AlAs-GaAs-AlAs double barrier resonant tunnelling diodes. *Appl. Phys. Lett.* **55**(6), 572-574.

[5] Sheard, F.W. (1992) *Private communication*. Department of Physics, Nottingham University

[6] Rogers, F.J. Graboske, H.C. Harwood, D.J. (1970). Bound Eigenstates of the static screened coulomb potential. *Phys. Rev. A*(1), 1577-1586.

[7] French, A.P. & Taylor, E.F. (1978). An introduction to quantum physics: MIT Introductory Physics Series.

[8] Kane, E.O. (1969). Tunneling phenomena in solids. Eds. E. Burstein & S.Lundqvist, Plenum. N.Y.

[9] Ricco, B. & Azbel, M. (1984). Physics of resonant tunneling: the 1-D double-barrier case. *Phys. Rev. B*, **29**(4), 1970-1981.

[10] Jonson, M. & Grinewajg, A. (1987). Effect of inelastic scattering on resonant and sequential tunneling in double barrier heterostructures. *Appl. Phys. Lett.* **51**(21), 1729-1731.

[11] Stone, A. & Lee, P. (1985). Effect of inelastic processes on resonant tunneling in one dimension. *Phys. Rev. Lett.*, **54**(11), 1196-1199.

[12] Wolak, E. Lear, K.L. Pinter, P.M. Hellman, E.S. Park, B.G. Weil, T. Harris, J.S. & Thomas, D. (1988). Elastic scattering centers in resonant tunneling diodes. *Appl. Phys. Lett.* **53**(3), 201-203.

[13] Weil, T. & Vinter, B. (1987). Equivalence between resonant tunneling and sequential tunneling in double barrier diodes. *Appl. Phys. Lett.* **50**(18), 1281-1283.

[14] Luryi, S. (1985). Frequency limit of double barrier resonant-tunneling oscillators. *Appl. Phys. Lett.* **47**(5), 490-492.

[15] Sollner, T.C.L.G., Goodhue, W.D.,Tannenwald, P.E.,Parker, C.D. & Peck, D.D. (1983). Resonant tunneling through quantum wells at frequencies up to 2.5 THz. *Appl. Phys. Lett.* **43**(6), 588-591.

[16] Morkoc, H., Chen, J., Reddy, U., Henderson, T. & Luryi, S (1986). Observation of a negative differential resistance due to tunneling through a single barrier into a quantum well. *Appl. Phys. Lett.* **49**(2), 70-72.

[17] Capasso, F., Mohammed, K. & Cho, A. (1986). Resonant tunneling through double barriers, perpendicular quantum transport phenomena in superlattices and their device applications. *IEEE J. Quantum Electron.* **22**(9), 1853-1869.

[18] Booker, S. M. (1992). Theory of tunnelling in double-barrier heterostructures. *PhD. Thesis*, Department of Physics, University of Nottingham

[19] Booker, S. (1992). Effect of inelastic scattering on resonant tunnelling in double-barrier heterostructures. *Semicond. Sci. Technol.* **7B**, 439.

[20] Duke, C. (1969). Tunneling in solids: Academic Press. N.Y.

[21] Mounaix, P., Vanbesian, O. & Lippens, D. (1990). Effect of cathode spacer layer on the current voltage characteristics of resonant tunneling diodes. *Appl. Phys. Lett.* **57**(15), 1517-1519.

[22] Koenig, E., Huang, C. & Jogai, B. (1990). Independence of peak current from emitter spacer layer width in AlGaAs/GaAs resonant tunneling diodes. *J. Appl. Phys.* **68**(11), 5905-5907.

[23] Koenig, E., Jogaî, B., Paulus, M., Huang, C. & Bozada, C. (1990). Charge quantization on current voltage characteristics of AlGaAs/GaAs resonant tunneling diodes with spacer layers *J. Appl. Phys.* **68**(7), 3425-3430.

[24] Fang, F. & Howard, W. (1966). Negative field-effect mobility on (100) Si surfaces. *Phys. Rev. Lett.* **16**(18), 797-799.

[25] Stern, F. & Howard, W. (1967). Properties of semiconductor surface inversion layers in the electric quantum limit. *Phys. Rev.* **163**, 816-835.

[26] Leadbeater M. L. (1990) Resonant tunnelling in semiconductor heterostructures. *PhD. Thesis*, Department of Physics, University of Nottingham

[27] Sheard, F.W. (1992) *Private communication.* Nottingham University, Department of Physics

[28] Frensley, W.R. (1988). Quantum transport calculation of the frequency response of resonant tunneling heterostructure devices. *Superlatt. & Microstruct.* **4**(4/5), 497-501.

[29] Sollner, T.C.L.G. Goodhue, W.D. Tannenwald, P.E. Parker, C.D. & Peck, D.D. (1983). Resonant tunneling through quantum wells at frequencies up to 2.5 THz. *Appl. Phys. Lett.* **43**(6), 588-590.

[30] Sheard, F.W. (1992). *Private communication.* Nottingham University, Department of Physics

[31] Mains, R.K. & Haddad, G. (1988). Time-dependent modeling of resonant-tunneling diodes from direct solution of the schrödinger equation. *J. Appl. Phys.* **64**(7), 3564-3569.

[32] Liu, H.C. (1987). Time-dependent approach to double-barrier quantum well oscillators. *Appl. Phys. Lett.* **52**(6), 453-455.

[33] Sheard, F.W. & Toombs, G.A. (1989). Space-charge effects and ac response of resonant-tunneling double-barrier diodes. *Solid-State Electron.* **32**(12), 1443-1447.

[34] Sheard, F.W. & Toombs, G.A. (1988). Space-charge buildup and bistability in resonant-tunneling double-barrier structures. *Appl. Phys. Lett.* **52**(15), 1228.

[35] Blakemore J. S. (1952) Carrier concentrations and Fermi levels in semi-conductors. Standard telecommunications laboratories, *Electrical communication*, 131-153.

[36] Sze S. M. (1981) Physics of semiconductor devices. John Wiley & Sons, NY.

CHAPTER 4

High Frequency Characterisation and Equivalent Circuit Models

4.1 Introduction

This chapter discusses the characterisation of DBRT devices at microwave frequencies which was carried out using a Hewlett Packard 8510B vector network analyzer to gather small-signal impedance information (via. S-parameters) for the device under test (d.u.t.) in terms of (magnitude and phase). The measurements were made in a co-axial cavity from 45 MHz to 12 GHz, but waveguide cavities were also used on occasion. The relatively narrow bandwidth associated with waveguide measurements does not permit multi-decade frequency characterisation without the use of different cavities, and therefore the co-axial environment was favoured.

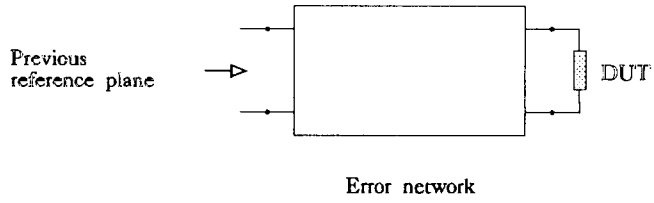
The measured impedances are subsequently compared with those derived from an appropriate equivalent circuit model, using a commercially available software program ("Microwave-Harmonica") the results of which are given in 4.4 and 4.5. With the use of lumped-element equivalent circuit models the small-signal microwave impedance can be linked to device-dependent characteristics. Often these characteristics can then be associated with specific layer differences between devices and can highlight the more significant of these differences in relation to the overall device performance.

Various models have been developed to link the small-signal behaviour with the

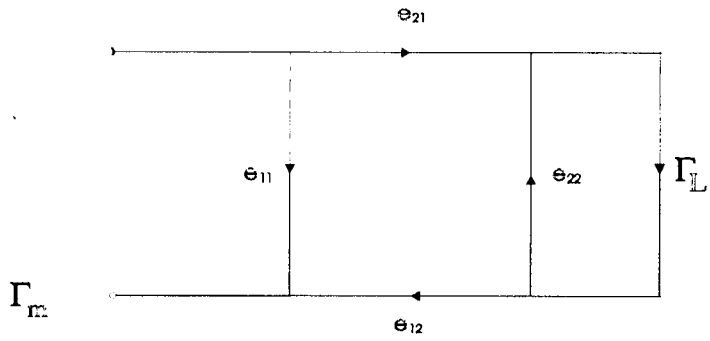
device-dependent parameters (section 4.3) but most lumped-element models only indicate the more significant of these layer dependent characteristics. A more direct relationship between the layer characteristics and the device impedance was sought (section 4.3.2), which involved separating some of the lumped elements into further lumped elements of a more detailed form. These more refined models were intended for use as vehicles in the design of improved devices and in the subsequent design of systems using these devices.

4.1.1 Measurement set-up

As mentioned in the introduction, the measurements were carried out using an HP 8510B network analyzer. For the room temperature measurements a precision (HP) co-axial test fixture was used, and for the combined low temperature (77 K) and room temperature measurements a co-axial mount with a built-in heat-sink was constructed, which screwed directly onto an APC-7 connector which was connected to a precision co-axial, jointed arm. Calibration was achieved automatically using a combination of standard loads (open-circuit, short-circuit and 50 ohm) to establish the reference plane at the connector of the co-axial mount. This calibration data was stored internally in the network analyzer and the necessary de-embedding of the received signal, using this data, was carried out almost instantaneously before being displayed (in effectively "real-time") on the c.r.t.. Further de-embedding to remove the package parasitics was considered desirable and was achieved using the varactor de-embedding procedure [1]. In this approach this additional de-embedding procedure is used to calibrate to the device plane within the test-fixture and more importantly into the S-4 package itself; this is achieved by lumping the reflections from the various discontinuities into an intermediate error network between the device and the previous reference plane. This intermediate network contains all the "error terms" (Figure 4.1) which were calculated from measurements on the varactor impedance at several bias voltages.



a



b

Figure 4.1 The intermediate error network which can accommodate the differences between the old and new reference planes.

The impedance of the varactor as a function of bias was measured at a low frequency (1MHz) and the error terms for each of the higher frequencies were derived by evaluation of this known impedance (providing the varactor cut-off frequency is much higher than the proposed measurement frequency) [2]. These error terms are subsequently used to de-embed the actual measured values for a similarly packaged device (chip) under test. The procedure is as follows.

With regard to Figure 4.1, equation (4.1) describes the complex error terms;

$$\Gamma_m = e_{11} + \frac{e_{12}e_{21}\Gamma_L}{1 + e_{22}\Gamma_L} \tag{4.1}$$

where Γ_m is the measured reflection coefficient and Γ_L is that of the load; e_{11} and e_{22} represent the loss of the signal and the mismatch of the d.u.t. respectively and where the frequency response of the intermediate network is represented by e_{21} and e_{12}. The three unknown error terms contained in the intermediate network are: e_{11}, e_{22} and the product $e_{12}.e_{21}$.

Once the error coefficients have been found the unknown reflection coefficient can be calculated using:-

$$\Gamma_L = \frac{\Gamma_m - e_{11}}{e_{22}(\Gamma_m - e_{11}) + e_{12}e_{21}} \,. \tag{4.2}$$

The reflection coefficients Γ_L and Γ_m are themselves given by the usual expression (4.3) and also from this expression the load and measured impedances can be derived.

$$\Gamma = \frac{Z_r - Z_0}{Z_r + Z_0} \tag{4.3}$$

where Z_0=50ohms and is the characteristic impedance of the (co-axial) test circuit, while Z_r is the impedance of the discontinuity from which a reflection takes place.

4.1.2 Samples used for parametric study

In this section the device preparation and range of layer structures used in the subsequent studies are described. The implications of these device variations are then investigated in section 4.4 from the effect of these variations (via. the equivalent circuit element values) on the device's impedance.

(a) Device preparation

As mentioned in Chapter 2, the devices used in this study were encapsulated in S-4 packages. Gold bond-wire of 12.5μm in diameter was used for electrical contact to the devices, and was chosen to allow bonds to be made directly to the 20μm diameter mesa's. The wire was bonded in a V-type configuration, with the mid-point being bonded to the top contact of the DBRT. Before final encapsulation the device was inspected and its d.c. properties checked using a curve-tracer. Consistency in both the packaging and bonding were necessary in order that the measured characteristics were more likely to be those of the device and not artifacts of the packaging. In the present study this was possible since all the factors from the device fabrication through to the packaging stage were carried out by the author. Slight variations in the lengths of bond-wire were unavoidable due to differences in device thicknesses. These differences were typically within ±10% of the overall thickness (100μm) and the thinning was achieved by using a mixture of mechanical abrasion followed by chemical etching from the initial value of around 450μm. It was assumed that variations in the length of bond-wire would be very small in relation to the effects of the device itself since the typical overall bond-wire inductances and resistances from top-to-bottom of a similar S-4 package (using a 25 μm in diameter bond-wire) for the V-configuration and for the I-configuration [3] were only ~0.46nH & 0.35ohms, and 0.79nH & 0.6ohms respectively. The difference in length of the bond wire with and without the device being present (100μm), only represents an ~7% difference in the inductance (ie. ~0.03nH) and hence the variation in thickness accounts for a small fraction (less than 1.5%) of the overall bond-wire inductance. V-type wire-bonds were used throughout, although in some cases an I-bond was inadvertently formed by half of the V-bond breaking away. Usually this was observed (and recorded) before the device was encapsulated. The resultant I-bond would be expected to approximately double the inductive contribution of the usual (V) bond. However, the varactor de-embedding procedure should remove the normal inductive contribution of the bond-wire used for the varactor. Hence the majority of the bond-wire inductance would be cancelled, except for an unobserved I-bond or from slight differences between the

bonding of the varactor and that for the devices used in this study. For example, the most likely type of bonding used for the varactor (exact data was not available) would be a V-bond using 25μm diameter gold wire, which would compare favourably with a 10μm diameter V-bond in terms of the inductance (0.80nH versus 0.85nH) [3]. The effects of the bondwire therefore should be removed after de-embedding to within several tenths of a nano-henry. Similarly the capacitive (shunt) effects of the package should also be removed after varactor de-embedding.

The signal power (at the measurement plane) used for the first group of measurements was set at about -20dBm (10μW) while for later measurements the power was about -27dBm. The signal power was maintained at an approximately constant level using the internal levelling circuit of the 8510 which compensated for frequency-dependent losses within the network analyzer itself. The signal power is an important consideration for "active" devices whose impedance will vary with excessive signal drive power (ie. large-signal régime).

(b) Layer structures used

Table 4.1 shows the layers and device sizes used to evaluate the effects on the impedance of such material characteristics as: asymmetric barriers, barrier thickness and heights and the effect of the length of the depletion region.

Dev. id .	Dia. (μm)	Temp. K	Polarity	Volts (V)
195/1	50	300	Positive	0.0, 0.1, 0.2, 0.3, 0.4, 0.5, 0.51, 0.52, 0.53, 0.54, 0.55, 0.56, 0.57, 0.58, 0.59, 0.6, 0.7
			Negative	0.0, 0.1, 0.2, 0.3, 0.4, 0.42, 0.44, 0.46, 0.48, 0.5, 0.6, 0.7
366/1	20	300	Positive	0.0, 0.5, 1.0, 1.1, 1.2, 1.3, 1.4, 1.5, 1.6, 1.7, 2.0
			Negative	0.0, 0.5, 1.0, 1.5, 2.0, 2.5, 3.0
368/2	50	300	Positive	0.0, 0.1, 0.2, 0.3, 0.32, 0.34, 0.36, 0.38, 0.4, 0.5, 0.6, 0.7, 0.8, 0.9, 1.0
			Negative	0.0, 0.1, 0.2, 0.3, 0.4, 0.5, 0.6, 0.7, 0.8, 0.9, 1.0
		77	Positive	0.0, 0.1, 0.2, 0.3, 0.4, 0.5, 0.6, 0.7, 0.8, 0.9, 1.0
			Negative	0.0, 0.1, 0.2, 0.3, 0.4, 0.5, 0.6, 0.7, 0.8, 0.9, 1.0, 1.1
453/4	50	300	Positive	0.0, 0.3, 0.6, 0.9, 1.0, 1.1, 1.2, 1.3, 1.4, 1.5
			Negative	0.0, 0.2, 0.4, 0.6, 0.8, 1.0
		77	Positive	0.0, 0.5, 1.0, 1.2, 1.4, 1.5, 1.6, 1.8, 2.0
			Negative	0.0, 0.2, 0.3, 0.4, 0.5, 0.6, 0.8, 1.0
453/6	100	300	Positive	0.0, 0.5, 1.0, 1.1, 1.2, 1.3, 1.4, 1.5
			Negative	0.0, 0.2, 0.4, 0.6, 0.8, 1.0
		77	Positive	0.0, 0.3, 0.4, 0.6, 0.8, 0.9, 1.2, 1.6
			Negative	0.0, 0.2, 0.3, 0.4, 0.5, 0.6, 0.7, 0.8
454/4	20	300	Positive	0.0, 0.1, 0.2, 0.3, 0.4, 0.5, 0.6, 0.7, 0.8, 0.9
			Negative	0.0, 0.4, 0.8, 0.9, 1.0, 1.1, 1.2, 1.3, 1.4, 1.5, 1.6
		77	Positive	0.0, 0.1, 0.2, 0.3, 0.4, 0.5, 0.6, 0.7, 0.8, 0.9, 1.0
			Negative	0.0, 0.4, 0.8, 0.9, 1.0, 1.1, 1.2, 1.3, 1.4, 1.5, 1.6,

Dev. id .	Dia. (μm)	Temp. K	Polarity	Volts (V)
454/1	50	300	Positive	0.0, 0.1, 0.2, 0.3, 0.4, 0.5, 0.6
			Negative	0.0, 0.5, 0.8, 0.9, 1.0, 1.1, 1.2, 1.3, 1.5, 2.0
		77	Positive	0.1, 0.2, 0.3, 0.4, 0.5, 0.6, 0.7, 0.9
			Negative	0.0, 0.5, 1.0, 1.1, 1.2, 1.3, 1.4, 1.5,1.6
454/6	100	300	Positive	0.0, 0.1, 0.2, 0.3, 0.4, 0.5, 0.6, 0.7, 0.8
			Negative	0.0, 0.5, 1.0, 1.1, 1.2, 1.3, 1.4, 1.5, 2.0
		77	Positive	0.0, 0.1, 0.2, 0.3, 0.4, 0.5, 0.6, 0.7, 0.8
			Negative	0.0, 0.5, 1.0, 1.1, 1.2, 1.3, 1.4, 1.5, 1.6, 2.0
455/1	20	300	Positive	0.0, 0.2, 0.3, 0.4, 0.5, 0.6, 0.7, 0.8, 1.0
			Negative	0.0, 0.2, 0.3, 0.4, 0.5, 0.6, 0.7, 0.8, 1.0
		77	Positive	0.0, 0.3, 0.4, 0.5, 0.6, 0.7, 0.8, 1.2, 1.6
			Negative	0.0, 0.2, 0.3, 0.4, 0.5, 0.6, 0.8, 1.2, 1.6
455/3	50	300	Positive	0.0, 0.2, 0.3, 0.4, 0.5, 0.6, 0.7, 0.8, 1.0
			Negative	0.0, 0.2, 0.3, 0.4, 0.5, 0.6, 0.7, 0.8, 1.0
		77	Positive	0.0, 0.2, 0.4, 0.5, 0.6, 0.7, 0.8, 1.0, 1.2, 1.4
			Negative	0.0, 0.2, 0.4, 0.5, 0.6, 0.7, 0.8, 1.0, 1.2, 1.4
455/5	20	300	Positive	0.0, 0.05, 0.1, 0.15, 0.2, 0.25, 0.3, 0.35, 0.4, 0.45, 0.5, 0.55, 0.6, 0.65, 0.7, 0.75, 0.8, 0.85, 0.9, 0.95, 1.0
			Negative	0.0, 0.05, 0.1, 0.15, 0.2, 0.25, 0.3, 0.35, 0.4, 0.45, 0.5, 0.55, 0.6, 0.65, 0.7, 0.75, 0.8, 0.85, 0.9, 0.95, 1.0

Dev. id .	Dia. (μm)	Temp. K	Polarity	Volts (V)
456/1	20	300	Positive	0.0, 0.1, 0.2, 0.3, 0.4, 0.5, 0.6, 0.7, 0.8, 0.9, 1.0, 1.1, 1.2, 1.3, 1.4, 1.5, 1.6, 1.7, 1.8, 1.9, 2.0
			Negative	0.0, 0.1, 0.2, 0.3, 0.4, 0.5, 0.6, 0.7, 0.8, 0.9, 1.0, 1.1, 1.2, 1.3, 1.4, 1.5, 1.6, 1.7, 1.8, 1.9, 2.0
		77	Positive	0.0, 0.4, 0.5, 0.7, 0.8, 0.9, 1.1, 1.2, 1.3, 1.5, 1.6, 2.0
			Negative	0.0, 0.4, 0.5, 0.7, 0.8, 0.9, 1.1, 1.2, 1.3, 1.5, 1.6, 2.0
456/1 as above but -3dBm lower power	As above	300	Positive	0.0, 0.2, 0.4, 0.5, 0.6, 0.7, 0.8, 0.9, 1.0, 1.1, 1.2, 1.4
			Negative	0.0, 0.2, 0.4, 0.5, 0.6, 0.7, 0.8, 0.9, 1.0, 1.1, 1.2, 1.4
456/1	As above	300	Positive	0.0, 0.1, 0.2, 0.3, 0.4, 0.5, 0.6, 0.7, 0.8, 0.9, 1.0, 1.1, 1.2, 1.3, 1.4
			Negative	0.0, 0.1, 0.2, 0.3, 0.4, 0.5, 0.6, 0.7, 0.8, 0.9, 1.0, 1.1, 1.2, 1.3, 1.4
456/3	20	300	Positive	0.0, 0.1, 0.2, 0.3, 0.4, 0.5, 0.6, 0.7, 0.8, 0.9, 1.0, 1.1, 1.2, 1.3
			Negative	0.0, 0.1, 0.2, 0.3, 0.4, 0.5, 0.6, 0.7, 0.8, 0.9, 1.0, 1.1, 1.2, 1.3
456/4 I-Bond	20	300	Positive	0.0, 0.1, 0.2, 0.3, 0.4, 0.5, 0.6, 0.7, 0.8, 0.9, 1.0, 1.1, 1.2, 1.3, 1.4
			Negative	0.0, 0.1, 0.2, 0.3, 0.4, 0.5, 0.6, 0.7, 0.8, 0.9, 1.0, 1.1, 1.2, 1.3, 1.4
469/1a I-bond	20	300	Positive	0.0, 0.05, 0.1, 0.15, 0.2, 0.25, 0.3, 0.35, 0.4, 0.45, 0.5, 0.55, 0.6, 0.65, 0.7, 0.75, 0.8, 0.85, 0.9
			Negative	0.0, 0.1, 0.2, 0.3, 0.4, 0.5, 0.6, 0.7, 0.8, 0.9, 1.0, 1.1, 1.2, 1.3, 1.4, 1.5, 1.6, 1.7
469/1b	50	300	Positive	0.0, 0.2, 0.3, 0.4, 0.5, 0.6, 0.7, 0.8, 1.0
			Negative	0.0, 0.4, 0.8, 0.9, 1.0, 1.1, 1.2, 1.3, 1.4, 1.6, 2.0
		77	Positive	0.0, 0.2, 0.4, 0.5, 0.6, 0.8, 1.0, 1.2, 1.4, 1.5
			Negative	0.0, 0.5, 1.0, 1.2, 1.4, 1.5, 1.6, 1.8, 2.0, 2.5, 3.0

Table 4.1 Devices studied from a selection of layer structures, device diameters, temperature and bias; each voltage represents measurements of impedance at 201 frequency points from 45MHz to 12GHz.

4.2 Device measurements: 0.4-12 GHz

Table 4.1 summarises the devices used in the study, and some of the parameters which effect the high frequency behaviour are:

Temperature
Area
Bonding configuration
Barrier thickness & height
Symmetry of barriers
Presence of collector drift region

This section brings together the experimental results, and is necessarily rather lengthy. The section is arranged as follows: Sections 4.2.1 and 4.2.2 discuss and validate the collection and recording of data and includes the data-reduction procedure and the repeatability of the results. Section 4.2.3 discusses the effects of temperature on the impedance and section 4.2.4 deals with the shunting effects of the junction capacitance on the high frequency signal, via the area. The behaviour is shown in Figures 4.11 and discussed in section 4.2.5. The final three factors from the list above are discussed in section 4.2.6 in which comparisons are made between the impedance of devices with different layer designs. The polarity of the applied bias shows dramatic differences for the asymmetric layers in terms of the impedance versus voltage behaviour. For all of the subsequent comparisons, the bonding and the device area are similar except for the thin barrier devices fabricated from layers NU-456 and NU-366. These layers yielded devices with such high current densities that the diameter had to be reduced to 20μm to avoid destructive overheating when biased on resonance.

4.2.1 Data reduction procedure

Measurements were made at each of the voltages shown in Table 4.1 and after de-embedding were stored as (201 numbers) complex numbers covering the frequency range 0.045-12GHz. The data for frequencies below 0.4GHz were ignored because they proved to be insufficiently reproducible, while the remaining data was reduced to only thirteen values of impedance covering the range between 0.4 and 12GHz. The data was subsequently stored as real and imaginary numbers in an IBM compatible format. The reduction in the number of data points was simply to improve the management of the large volume of data and to reduce the file size for input to the modelling software, which simplified appending the appropriate data block to each circuit-file model. The data reduction procedure was checked by plotting the data for a device from NU-455 against the complete data (Figure 4.2 a&b). The data in these figures is both the measured data and the interpolated values which have been generated by "Microwave-Harmonica" (by cubic spline fitting) to fit the thirteen measured values. This procedure is performed automatically by "Microwave-Harmonica" to extend the data in the measured data block to coincide with the frequency range specified in the model. From Figure 4.2 a&b it can be seen that both the selection of the thirteen measured values describes the overall trend of the data rather well, and that the cubic spline fitting performed by "Microwave-Harmonica" is adequate for describing these impedance trends.

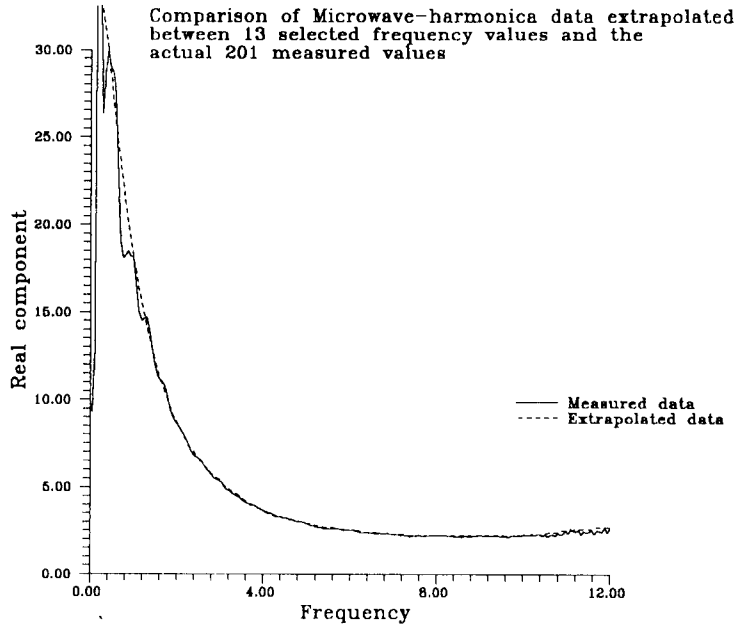


Figure 4.2 a

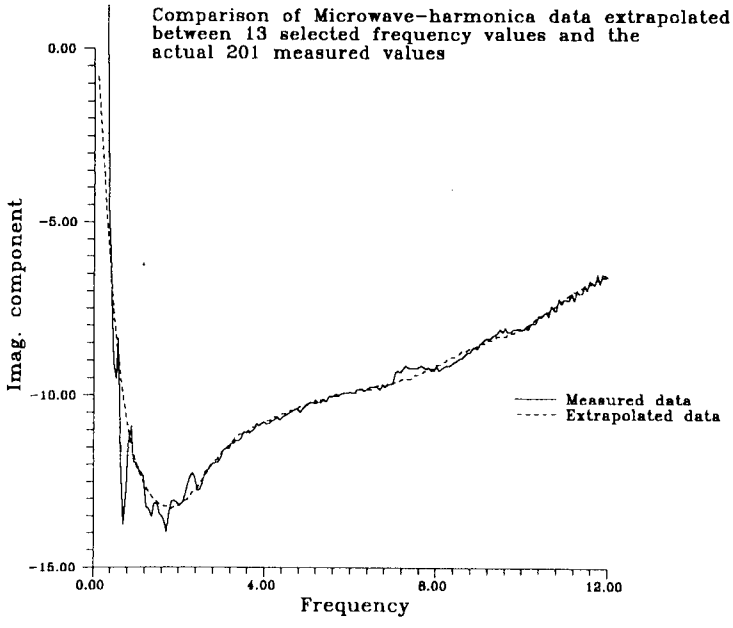


Figure 4.2b Extrapolated impedance v's actual measured values

As a check on the de-embedding procedure Figure 4.3 shows the impedance after de-embedding, of an S-4 package which was short-circuited using a 10 μm V-bond to the bottom of the package. The extra length of bond-wire (from what would otherwise be the top of the chip) to the bottom of the package would not be removed by the de-embedding procedure since this constitutes an extra length of wire in addition to that used for providing contact to the varactor. The measured S-4 short-circuit may therefore show a slight excess inductance and resistance, as is indeed the case.

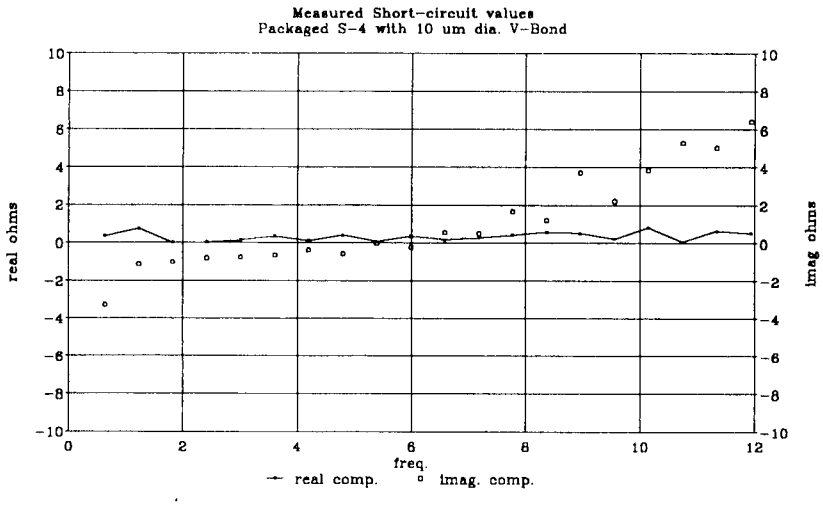


Figure 4.3 Impedance of short-circuit S-4 after de-embedding

4.2.2 Repeatability of results

Due to the differences in the signal power used to make the measurements on different occasions the results of different runs were not compared except for the special cases of 456/1, and 455/1 (run 1) and 455/5 (run 2). In the case of 456/1 the aim was to test the repeatability of the measurements made on the same device on different occasions, and for 455/1 & /5 on two similar devices (with near identical current-voltage characteristics). Comparison was then made between the -23 dBm results of run 1, and the results from run 2 which were made at -27 dBm.

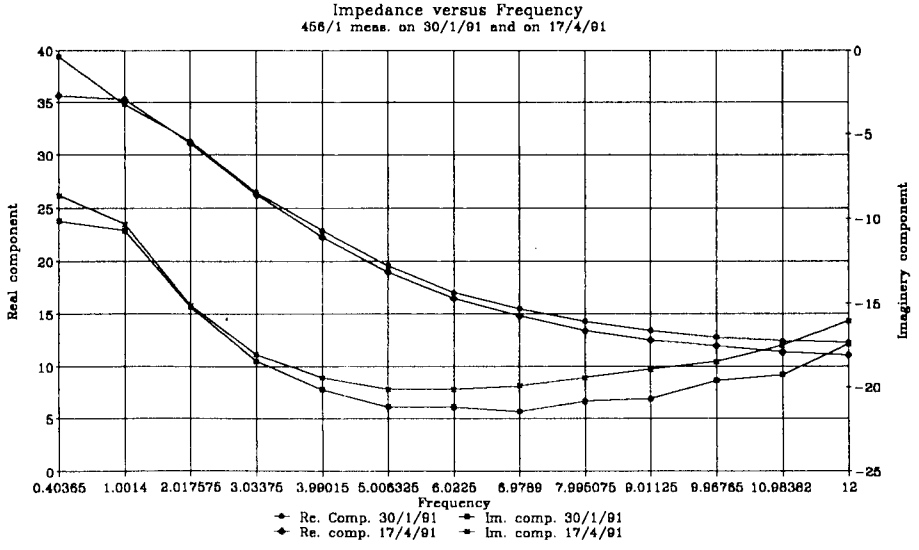


Figure 4.4 Comparison of the same device measured on different occasions.

Figure 4.4 shows the comparison of 456/1 measured on run 1 with those of run 2. The repeatability of measurements on the same device on successive occasions is shown to be excellent, with less than 10% difference in either the components.

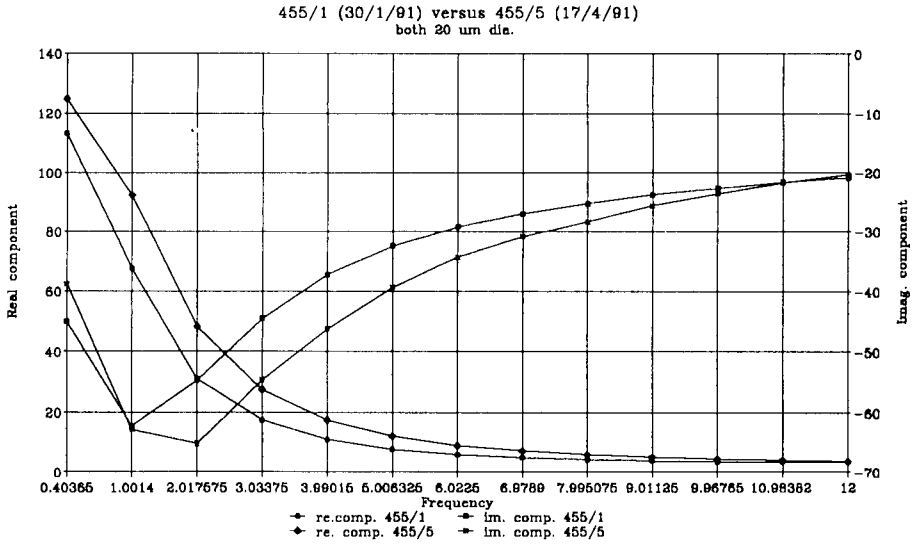


Figure 4.5 Comparison of similar devices measured on different occasions.

Figure 4.5 shows the comparison between 455/1 (run 1) and 455/5 (run 2). Both are 20μm in diameter and most importantly, exhibit near identical current-voltage characteristics (see Figure 4.6). The devices are shown to have very similar impedance characteristics proving that it is possible to fabricate nearly identical

devices, provided that the current-voltage characteristics are similar and the bonding and encapsulation are also the same.

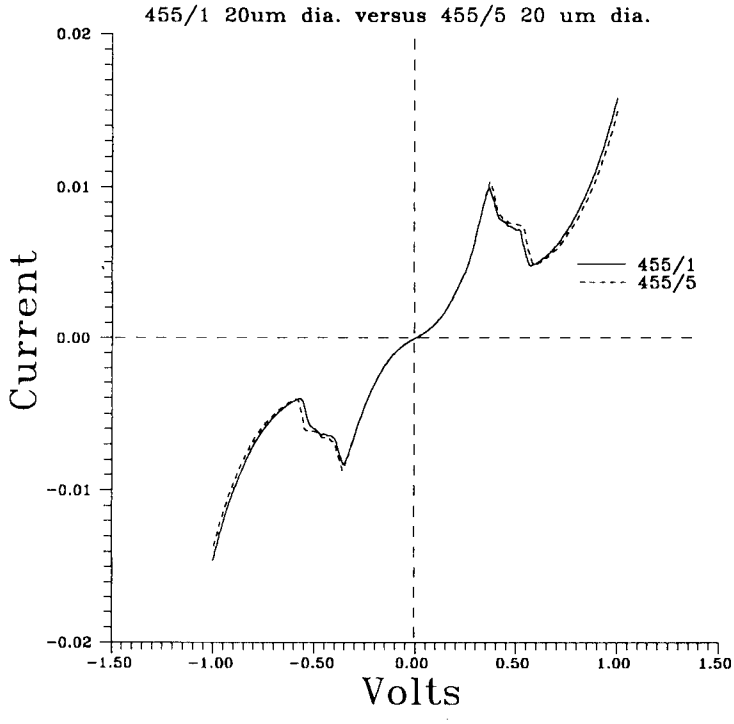


Figure 4.6 Comparison of the current-voltage characteristics for two similar devices.

Devices 456/1 and 456/3 were measured on the same occasion and were also intended to demonstrate the repeatability of measurements on similar devices. The investigation was, however, complicated by significant differences in the current-voltage characteristics. These differences were unexpected and were thought to arise from damage during the bonding stage or from variations in the layer structure which may

arise from "geographical" variations across the wafer. A similar problem of poor comparison between the current-voltage characteristics of 456/1 and 456/4 (I-bond) hindered the investigation of the effects on the impedance arising solely from the differences in bonding configuration; these differences can only be inferred from subsequent differences in the device models (section 4.4.4 for 456/1 and 456/3 and 456/4).

4.2.3 Effect of temperature on impedance

Device impedance was also investigated as a function of bias and frequency at two fixed temperatures (77K and 290K). Figures 4.7-4.10 show some of the results of this investigation.

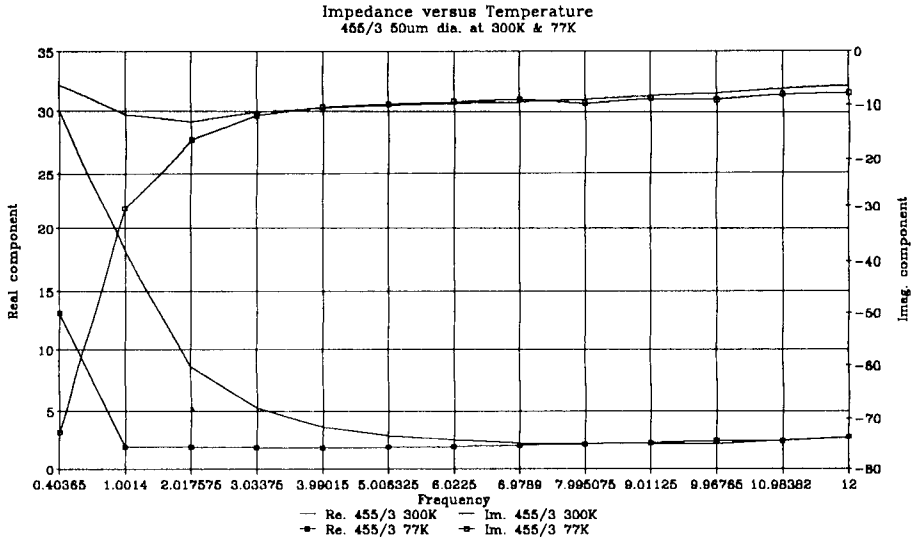


Figure 4.7 Effect of temperature on impedance of 455 class of devices.

From Figure 4.7 the effect of temperature on the impedance can be seen to increase the magnitude of both the real and imaginary components of the impedance, especially at the lower frequencies, and to increase the rate of change of impedance as a function of voltage. The general behaviour of the device impedance as a function of frequency is discussed in section 4.5 and is shown in the sequence of Figure 4.11. The effect of temperature is understandable since the magnitude of the current at low temperature is much reduced while the rate of change of current as a function of voltage increases. This is because at low temperature there is a reduction in the temperature broadening of the spread in energies of the incident electrons (ie. the supply function, see Figure 1.7) which reduces the number of electrons that can tunnel at low bias, and also

increases the rate of change of current with bias. This effect was discussed in chapter 3. The effects of temperature on impedance is more clearly observed by using a different "graphical" representation as is shown in Figure 4.8.

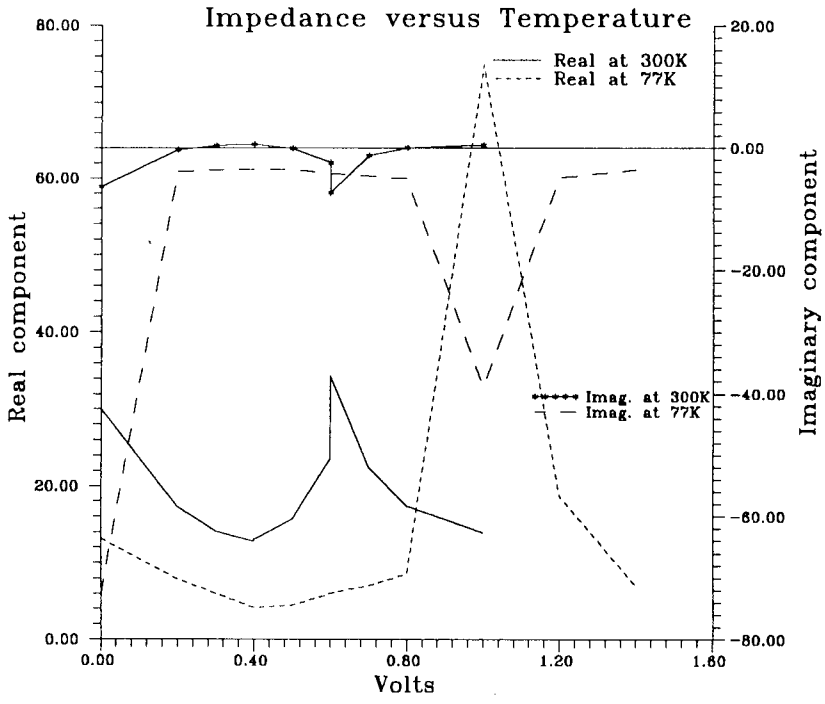


Figure 4.8 Device 455/3 (50μm dia. at 0.4GHz) showing the magnitude of the real and imaginary values of impedance.

Figure 4.8 shows the variation in impedance as a function of bias at two different temperatures and reflects the differences in the current-voltage characteristic for 455/3 at the two temperatures. The shift to higher voltages of the impedance-versus-voltage characteristic with diminishing temperature is mirrored in the increased magnitude of the d.c. peak current and the greater peak-to-valley current swing, accompanied by the

shift to higher voltages of the peak current and increased spreading of the peak-to-valley voltage as the temperature is lowered. Reducing the temperature tends to mimic the effect of increasing the thickness of the barriers and reducing the thickness of the well slightly in terms of the effect of impedance versus voltage.

4.2.4 Effect of area on impedance

Shown in Figure 4.9 is the effect of device area on the impedance at zero volts, while Figure 4.10 shows the variation in impedance versus voltage as a function of device area.

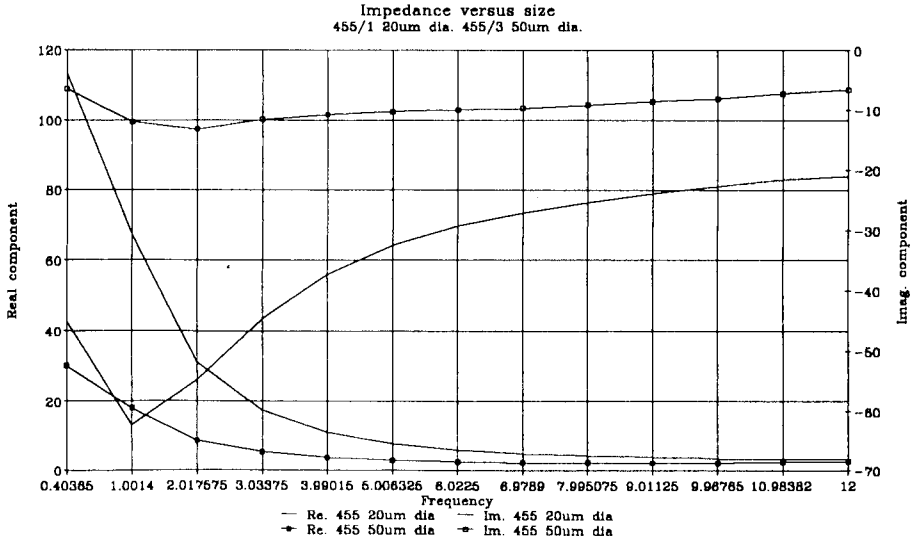


Figure 4.9 Effect of device size on impedance (@ 0v) where 455/3 is 50 μm in diameter and 455/1 is 20 μm in diameter.

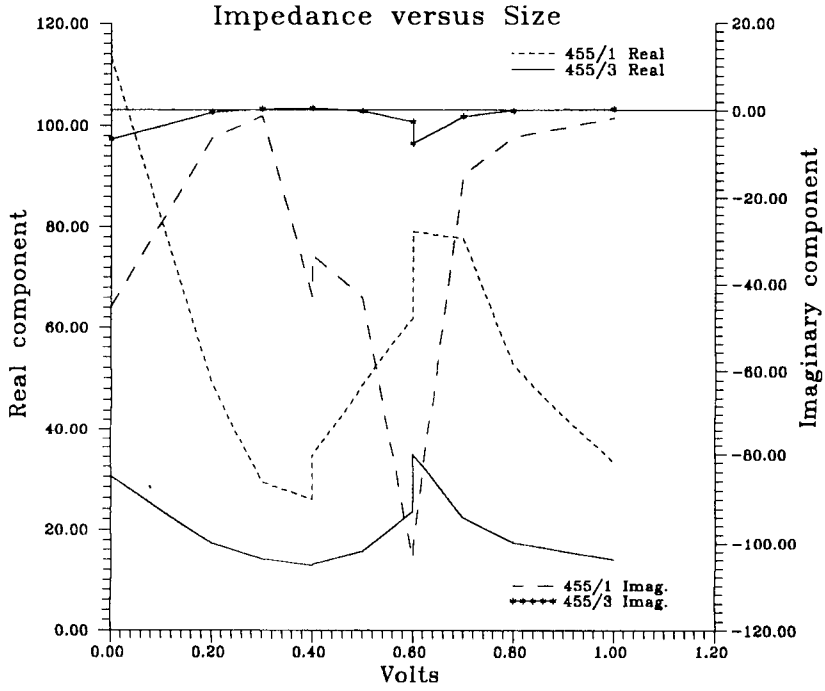


Figure 4.10 Effect of device size on impedance versus applied bias.

With regard to Figure 4.9, the trends shown are predictable with both the real and imaginary components increasing with reduced active device area as would be expected. The difference is approximately similar to the ratio of the device area.

The real and imaginary values of impedance shown in Figure 4.10 can be seen to scale approximately with area. The reason that this scaling is only approximate is that in the simplest description each of the real and imaginary components of the impedance depend on the parallel combination of the capacitance and resistance and not on the single elements alone.

4.2.5 Typical impedance trends as a function of frequency

The following series of Figures 4.11 (a-m) illustrate (for a 20μm diameter device from layer NU-455, device 455/1), how the increasing signal frequency appears to overlook the impedance variation seen at lower frequencies. This is consistent with what would be expected from the simple parallel combination of capacitance and resistance often used to approximate the DBRT device.

$$Z_{\parallel} = \frac{R}{1 + R^2\omega^2C^2}(1 - jR\omega C) \tag{4.4}$$

The following series of Figures 4.11 (a-m), show the real and imaginary components (in ohms) as a function of applied bias, at each of the thirteen different frequencies, which were chosen to represent the behaviour over the complete range of frequencies.

From Equation 4.4 the magnitude of both the real and imaginary components of the impedance tends to decrease with increasing frequency and this is reflected in Figure 4.11.

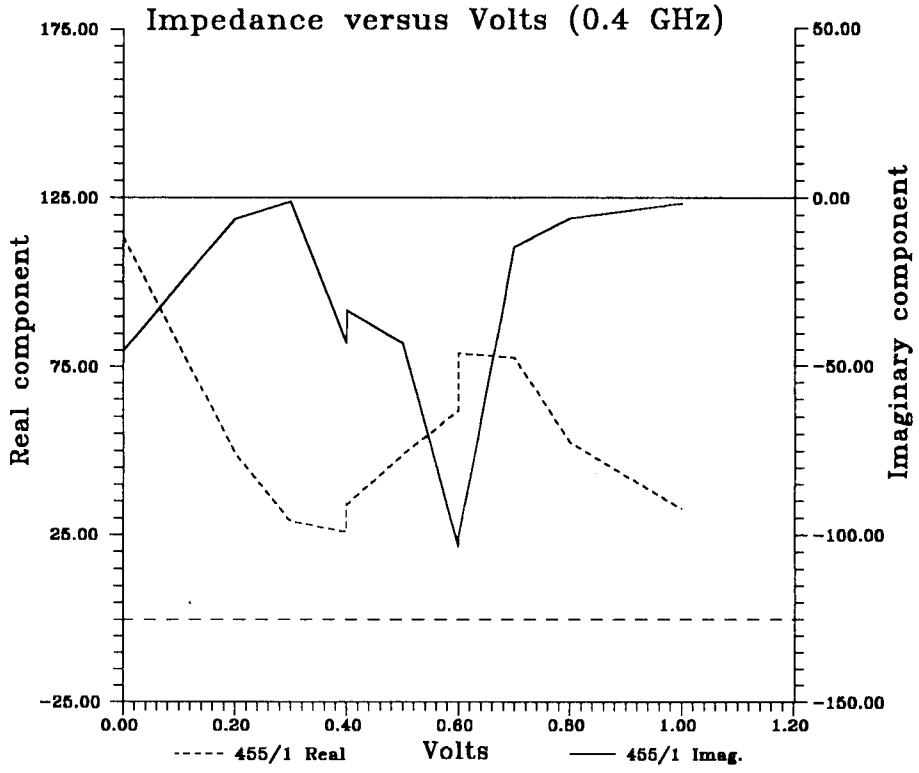


Figure 4.11 a

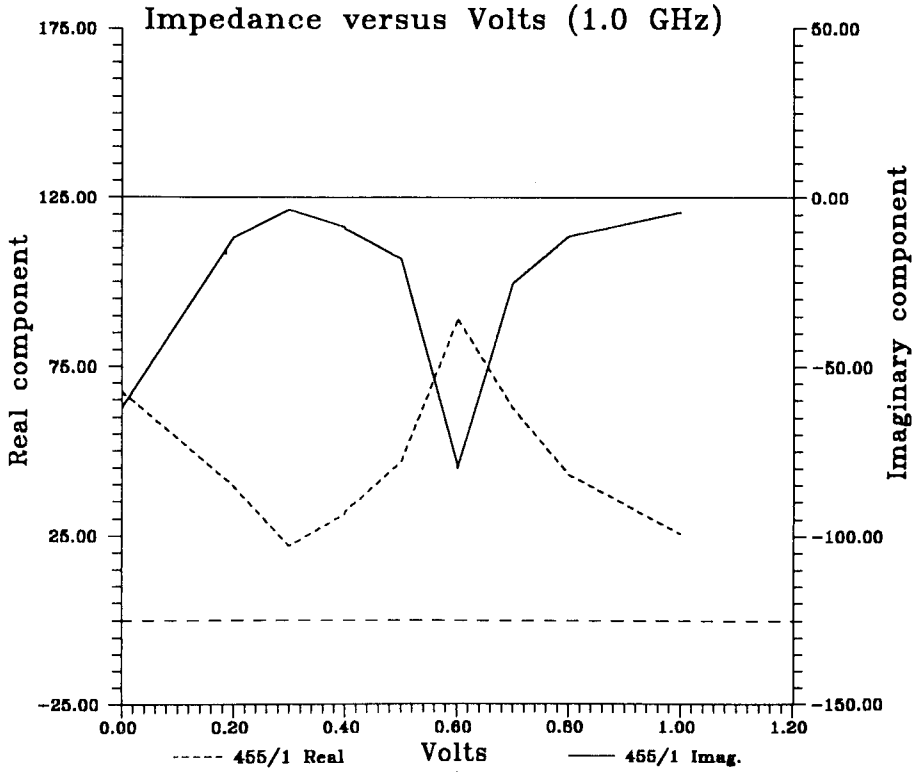


Figure 4.11 b

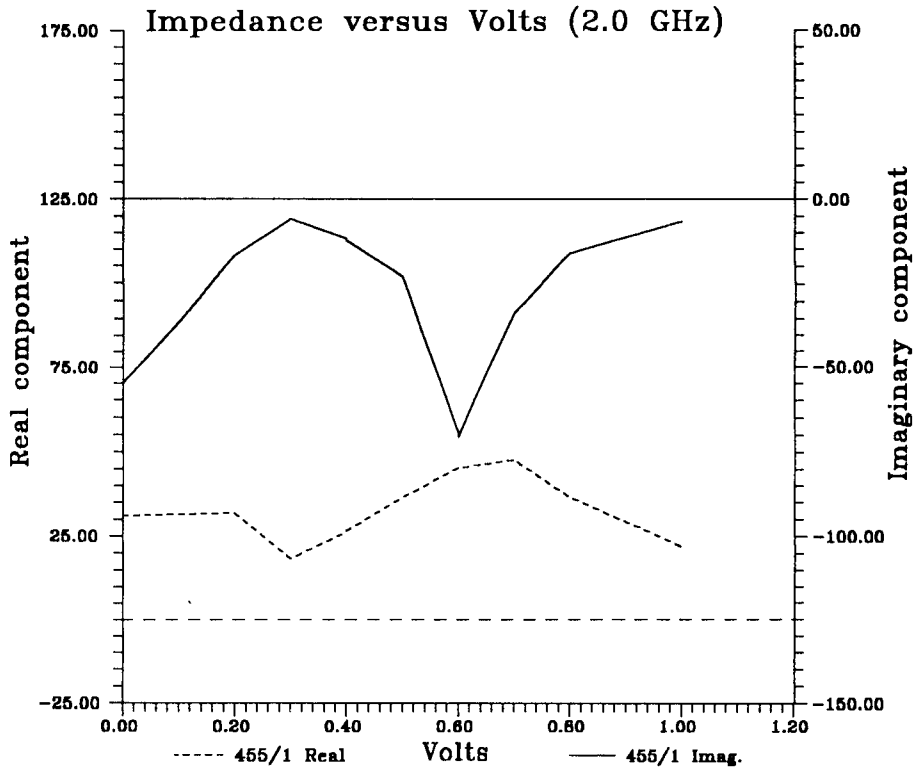


Figure 4.11 c

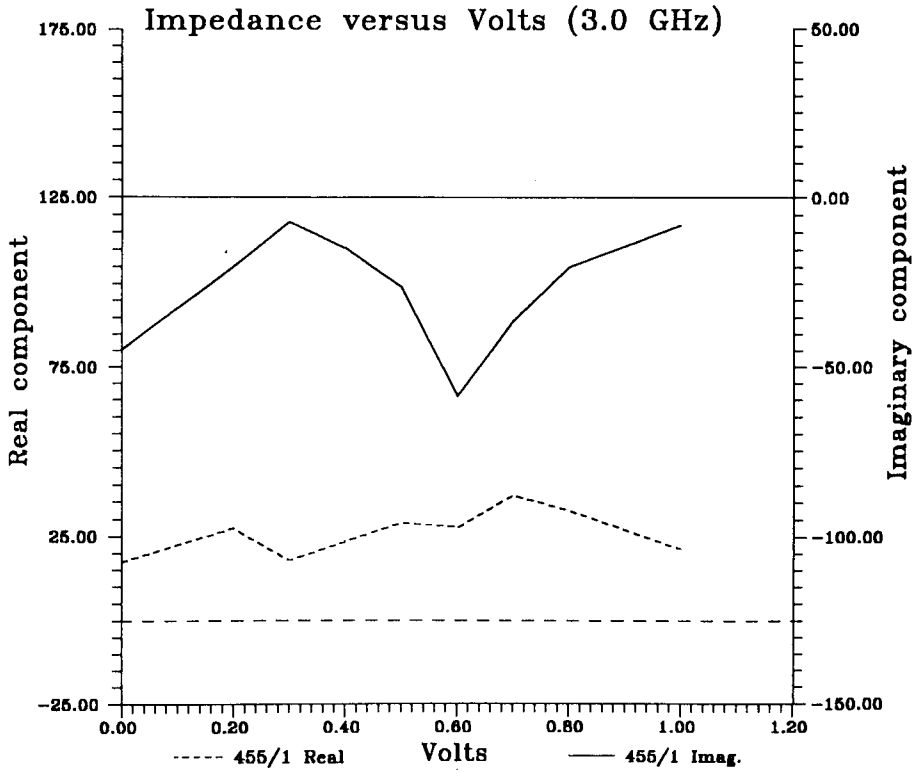


Figure 4.11 d

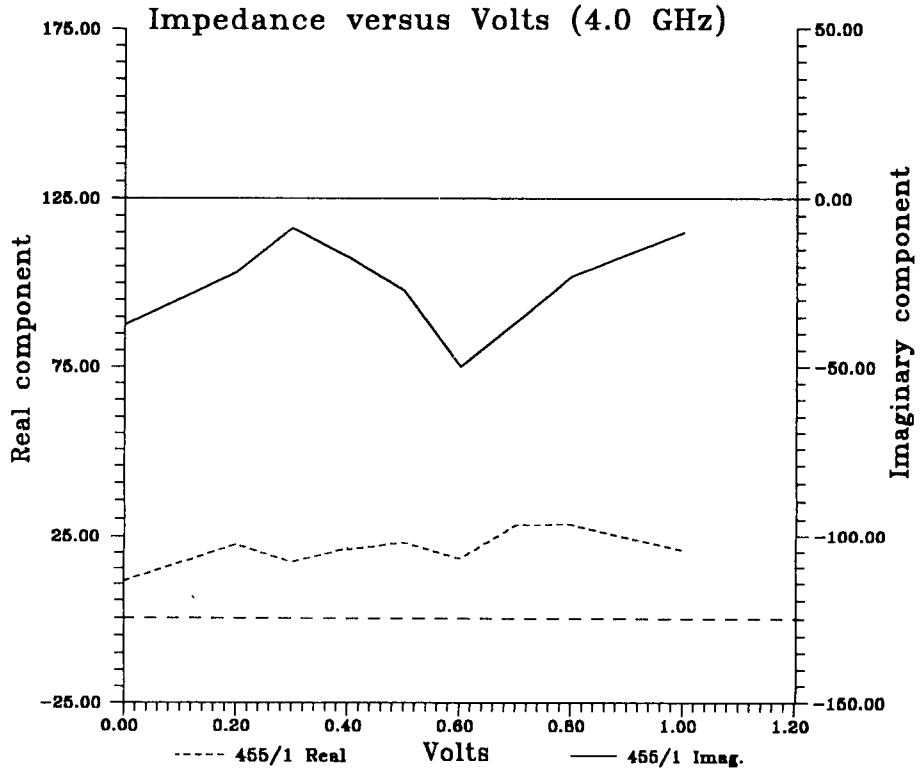


Figure 4.11 e

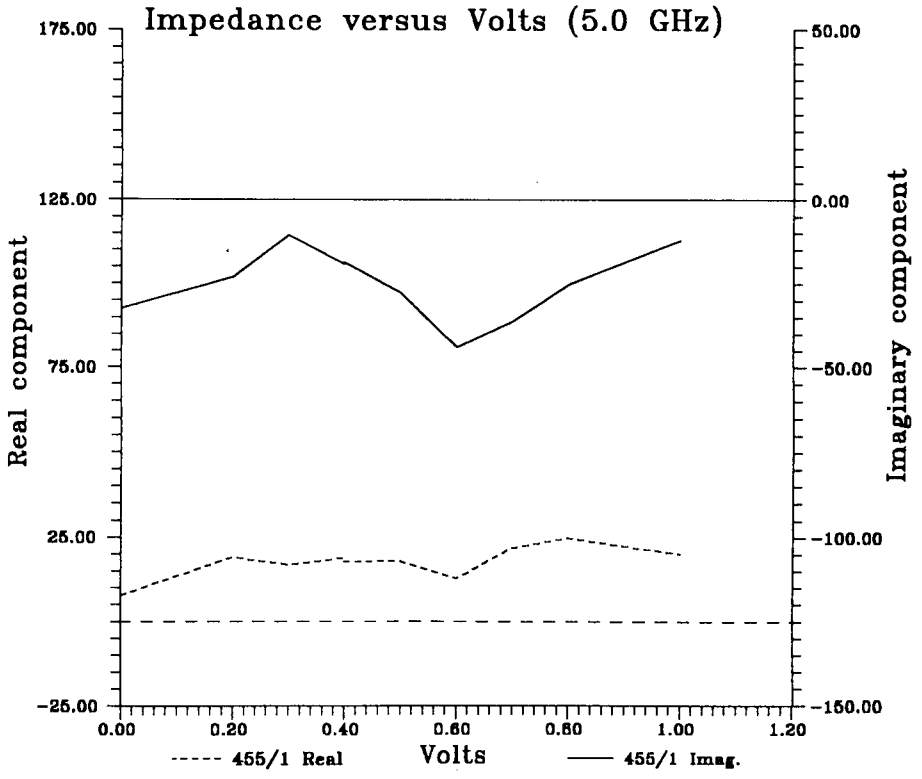


Figure 4.11 f

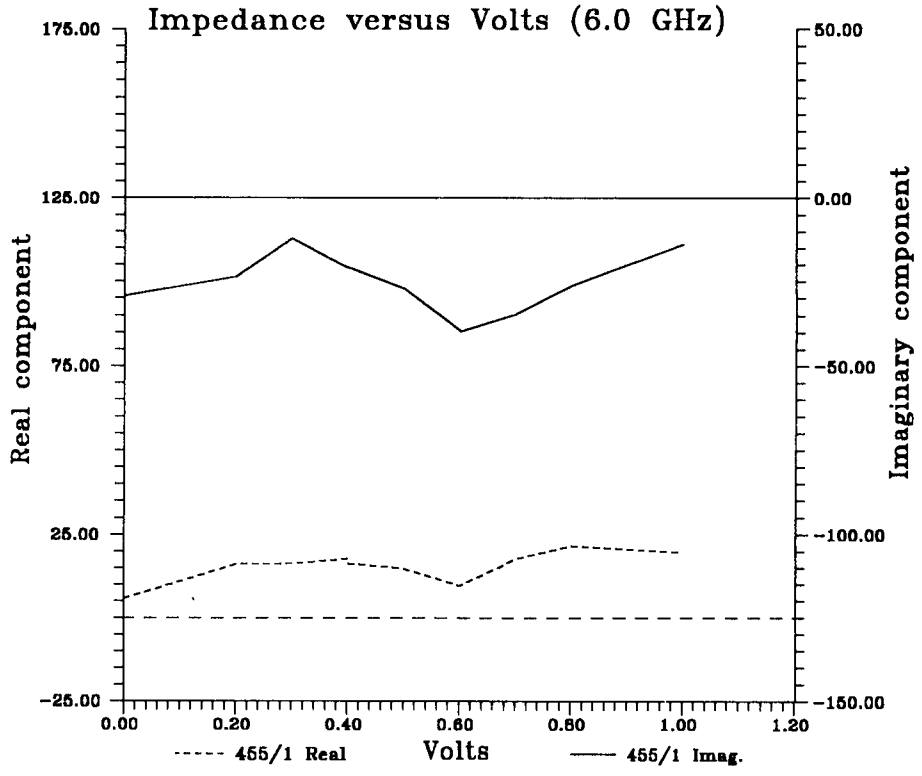


Figure 4.11 g

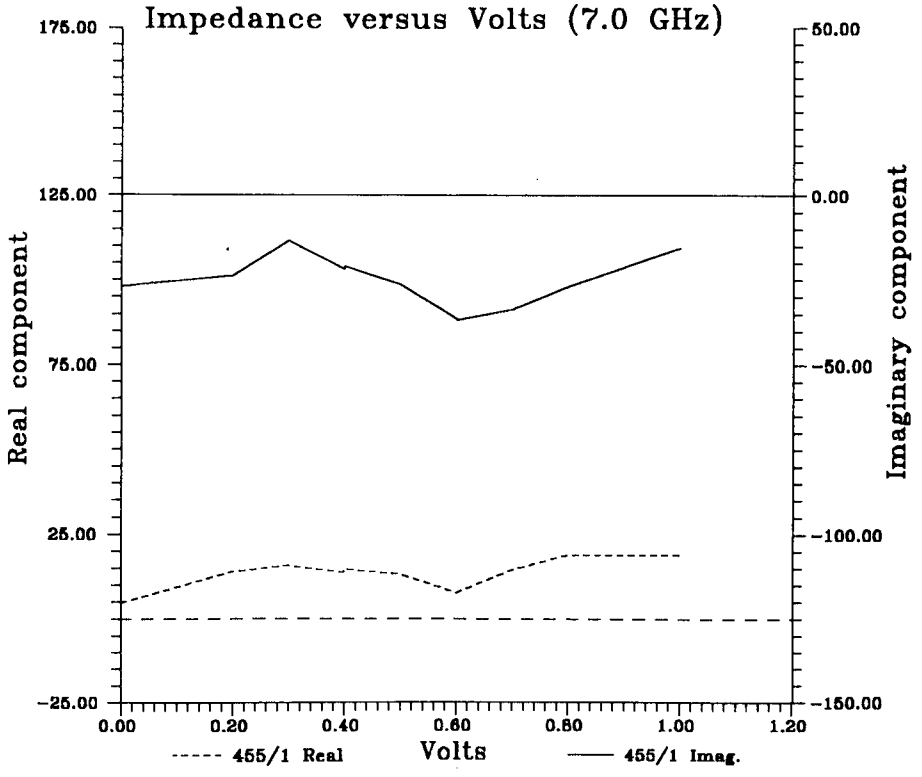


Figure 4.11 h

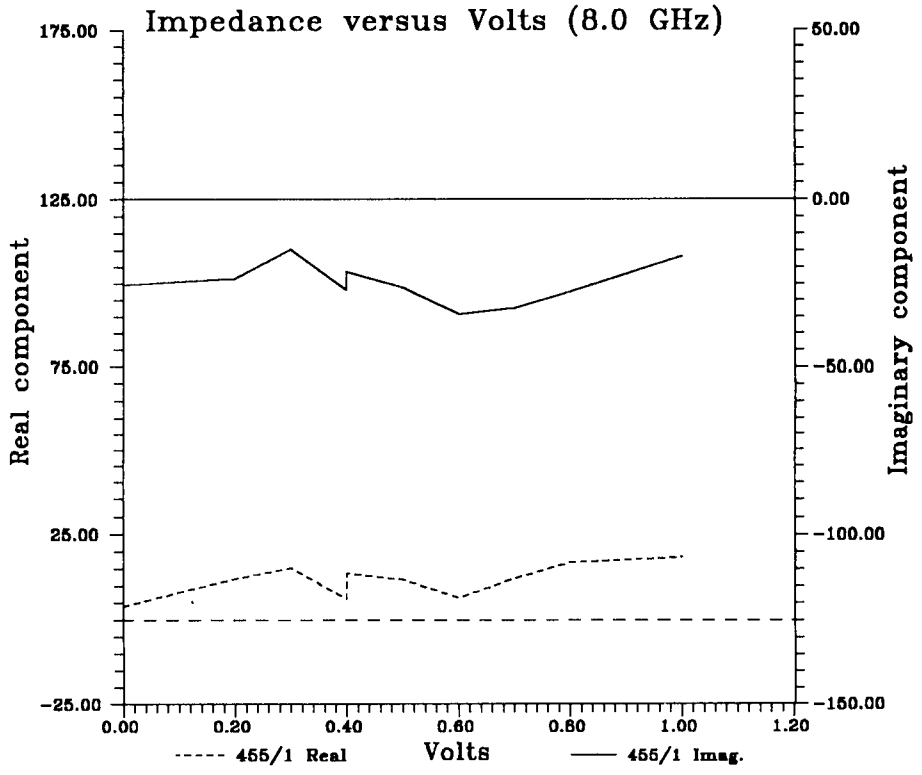


Figure 4.11 i

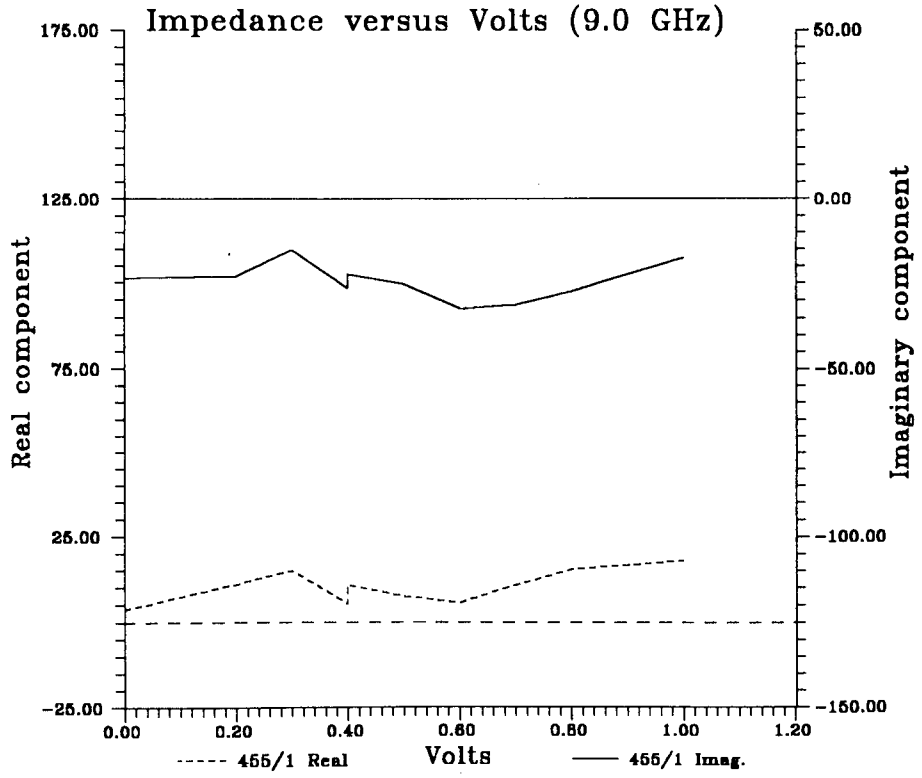


Figure 4.11 j

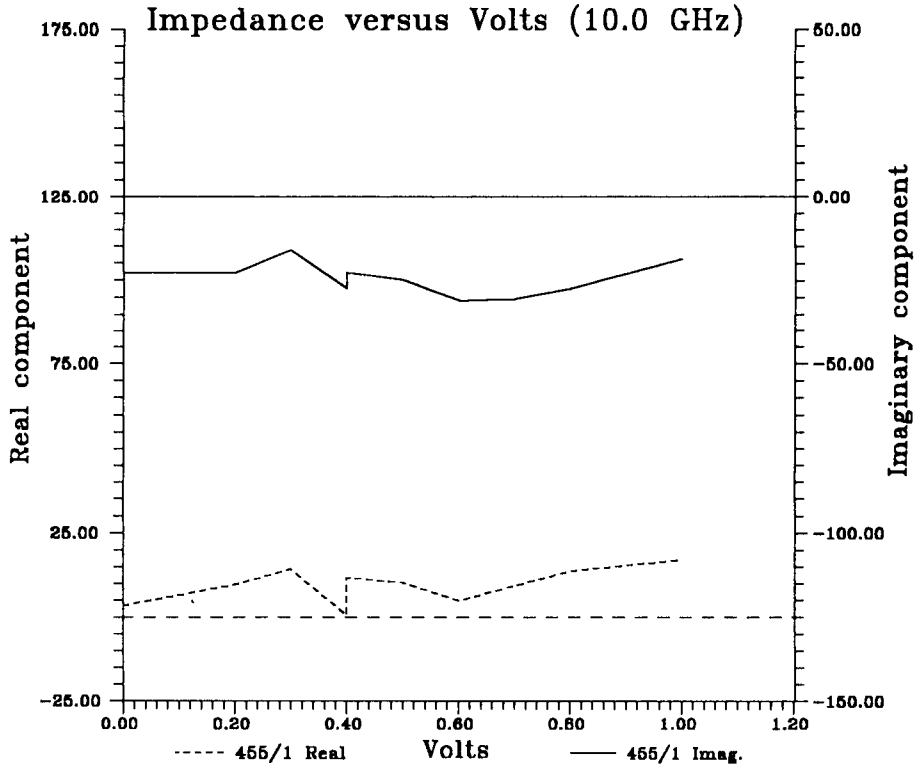


Figure 4.11 k

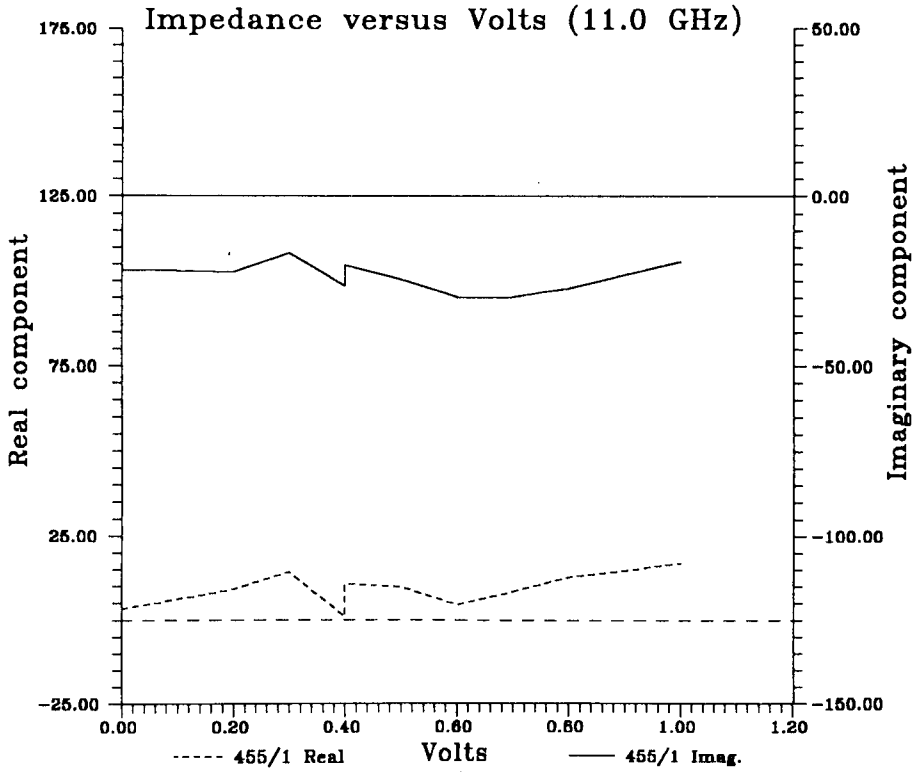


Figure 4.11 l

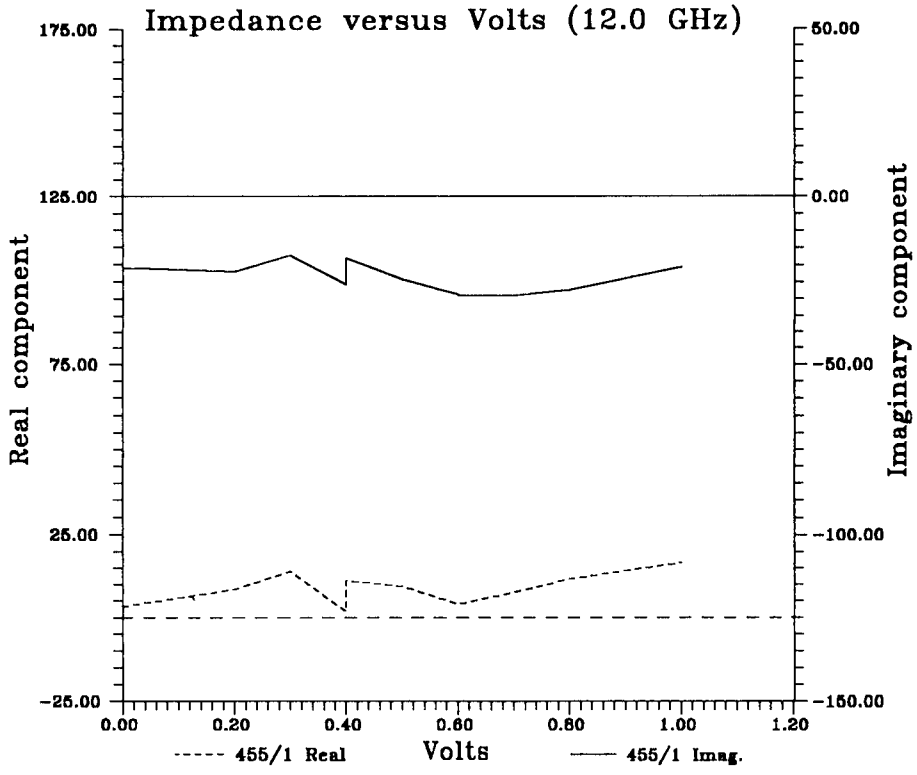


Figure 4.11 m

The frequency-dependent trend of reducing impedance shown for Figures 4.11 (a- m) is similar for all the devices measured. The variation between different layers mainly results from the area and the separation of the charged plates (via doping regions) in each device. The overall shape however, is dependent on the layer structure of the device in question but the trend with frequency will be preserved in the case of other structures. For the device shown in Figure 4.11 the region of NDR is between about 0.3-0.6v (see also Figure 4.6) and this is reflected in the series of figures by an increase in the magnitude of impedance over this range of voltage. In the general case (in Figure 4.11) the increase in magnitude of impedance in the NDR region is reduced at higher frequencies there remains a slight "notch" in the impedance (8-12GHz) which is thought to arise through a slight instability over this range of frequencies. The NDR (if stabilized) can also lead to the phenomenon of reflection-gain at certain

frequencies which can result in sharp changes in behaviour and often to negative values for the real component of impedance (for example see Figure 4.12 (a&b)).

4.2.6 Effect of layer structure on impedance

The following Figures (4.12-4.18) summarise graphically the effects of microscopic layer-dependent variation on device impedance as a function of voltage. These effects are shown for the lower frequency of 0.4 GHz since this most clearly demonstrates the layer-to-layer differences. The polarity-dependent impedance, shown as "a" or "b" of Figures (4.12-4.18), highlight mainly the layers where either the barriers or the adjacent doping are un-symmetric throughout the device structure. Reverse bias ("b" figures) implies that the top contact of the device is negative with respect to the bottom contact.

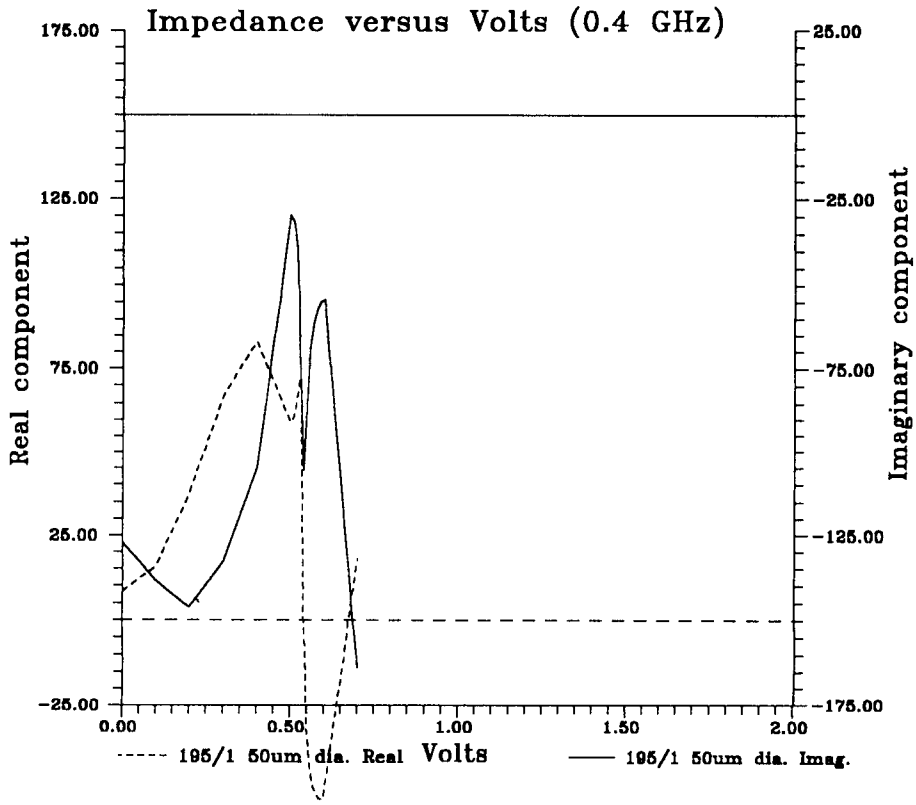


Figure 4.12 a

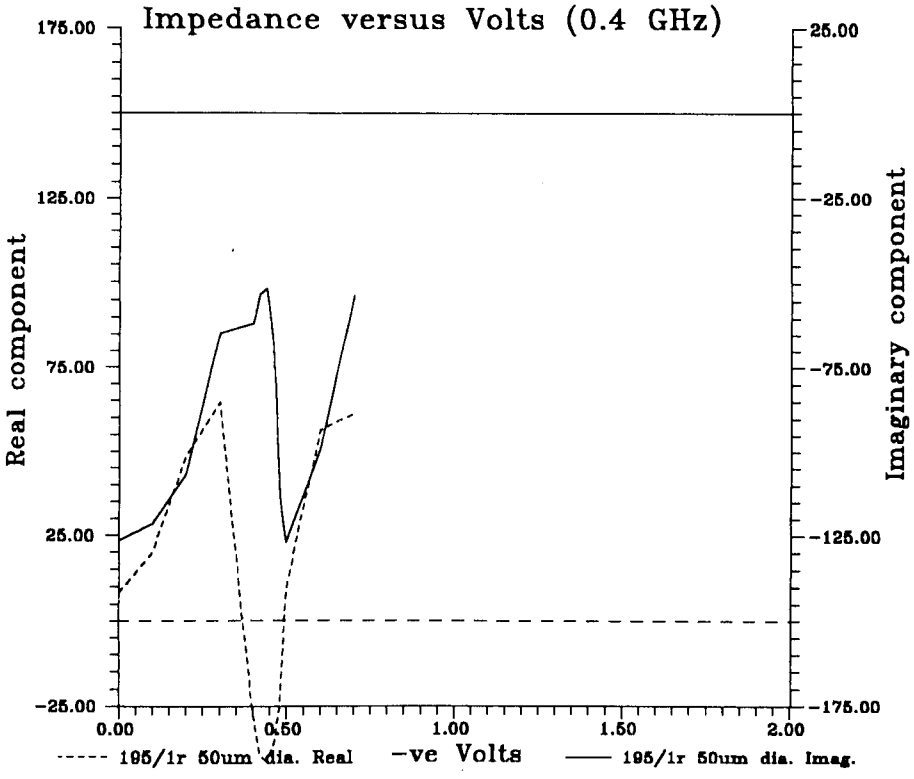


Figure 4.12 b

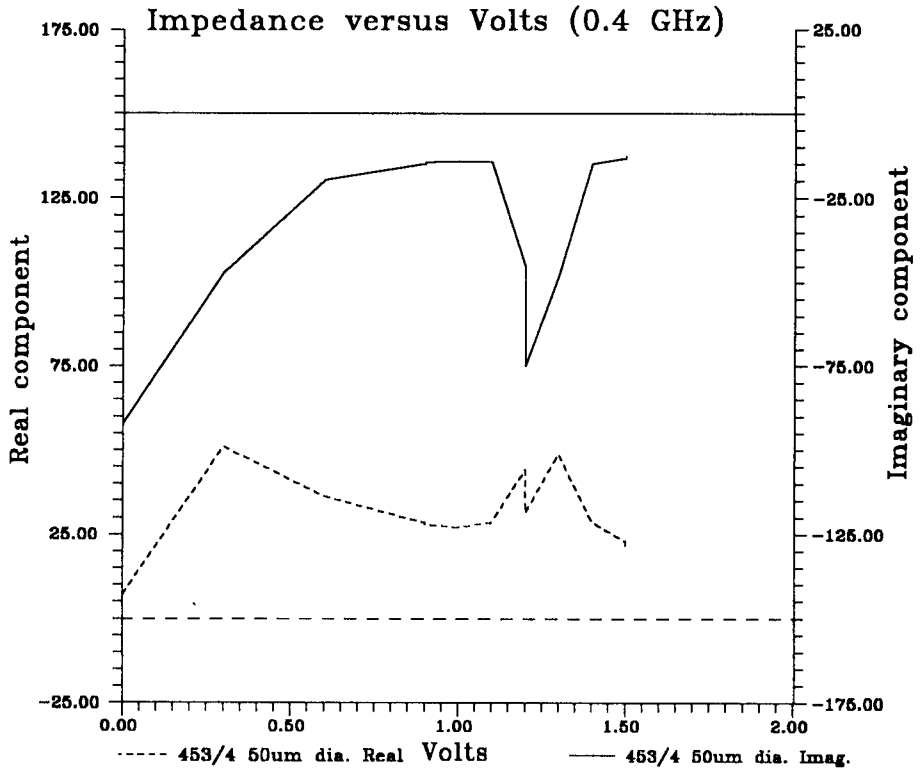


Figure 4.13 a

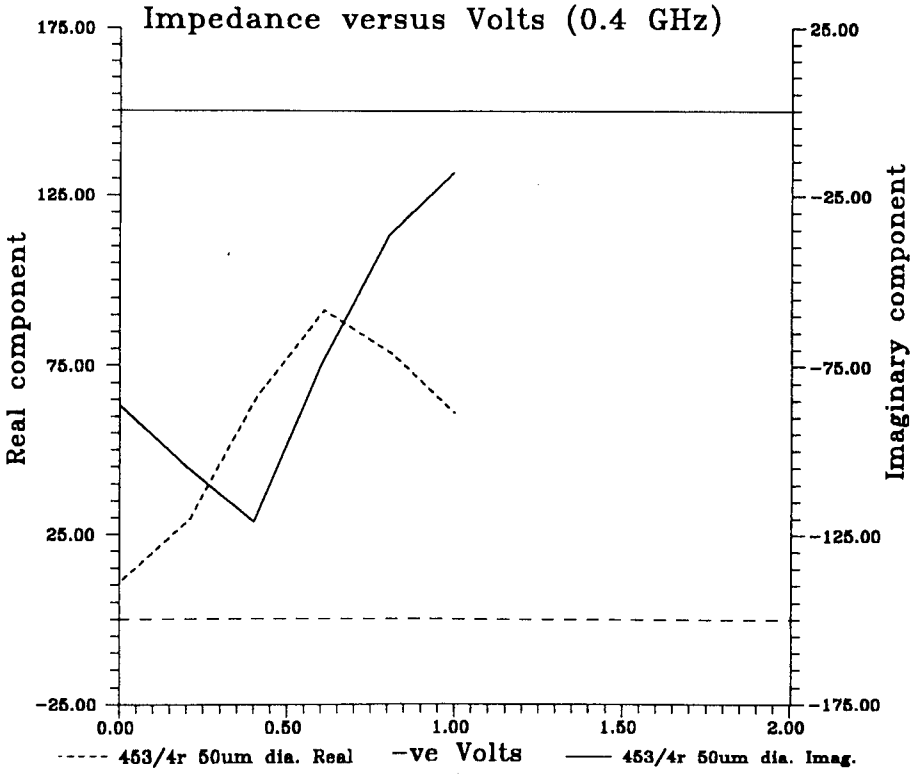


Figure 4.13 b

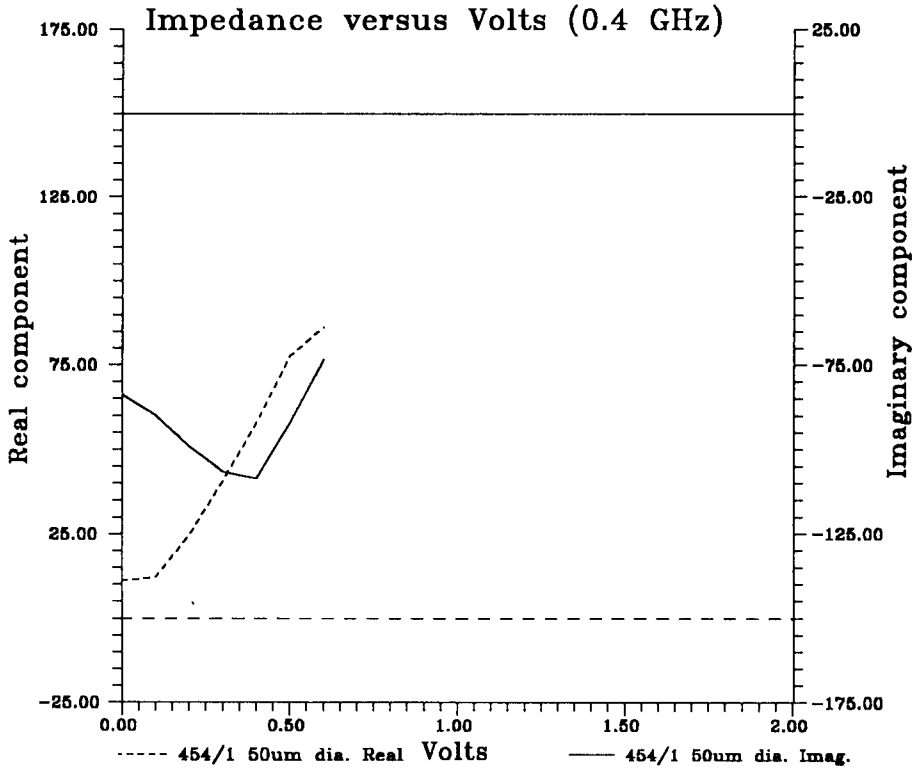


Figure 4.14 a

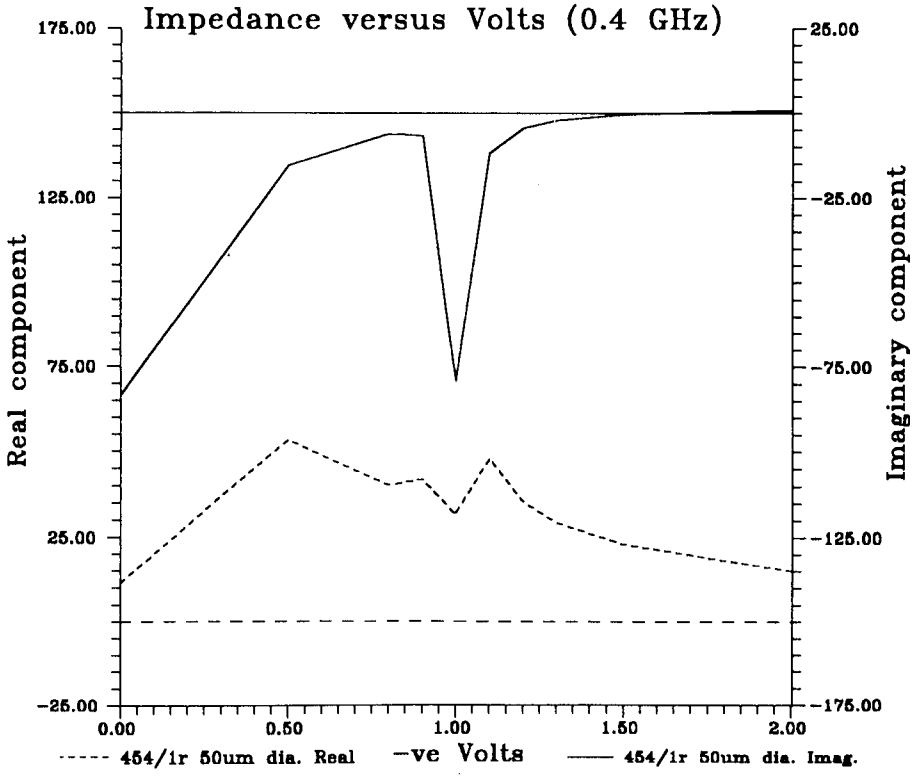


Figure 4.14 b

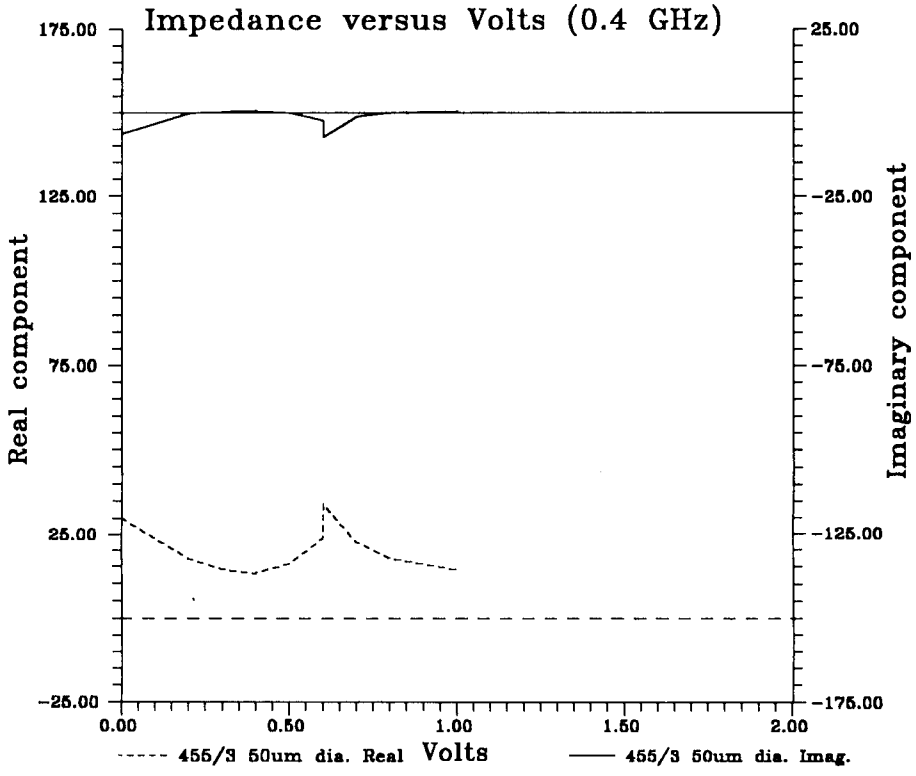


Figure 4.15 a

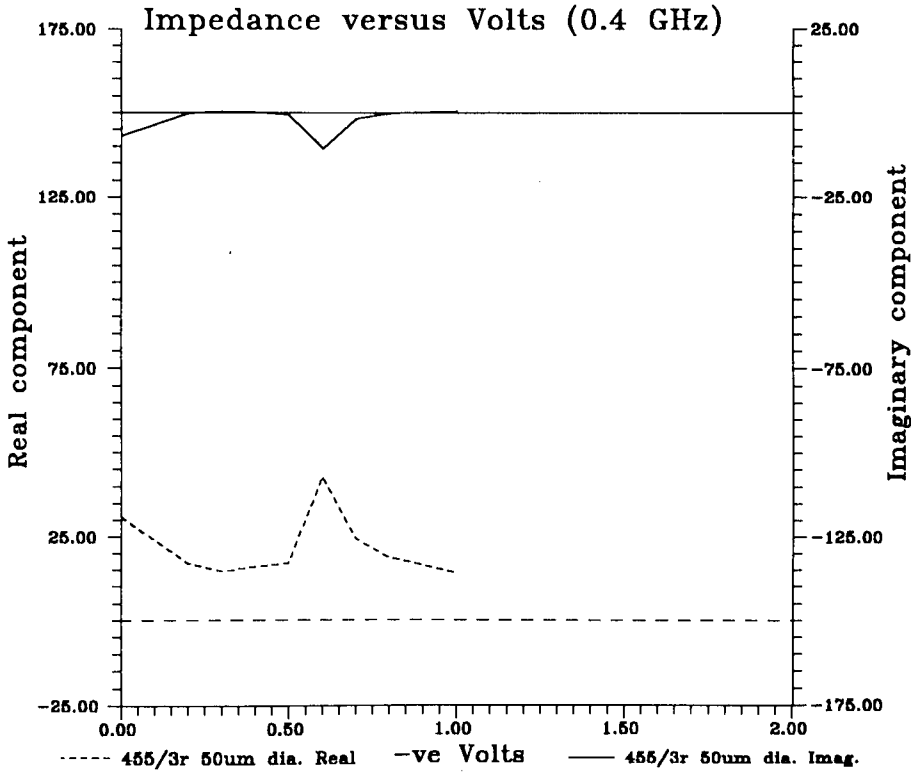


Figure 4.15 b

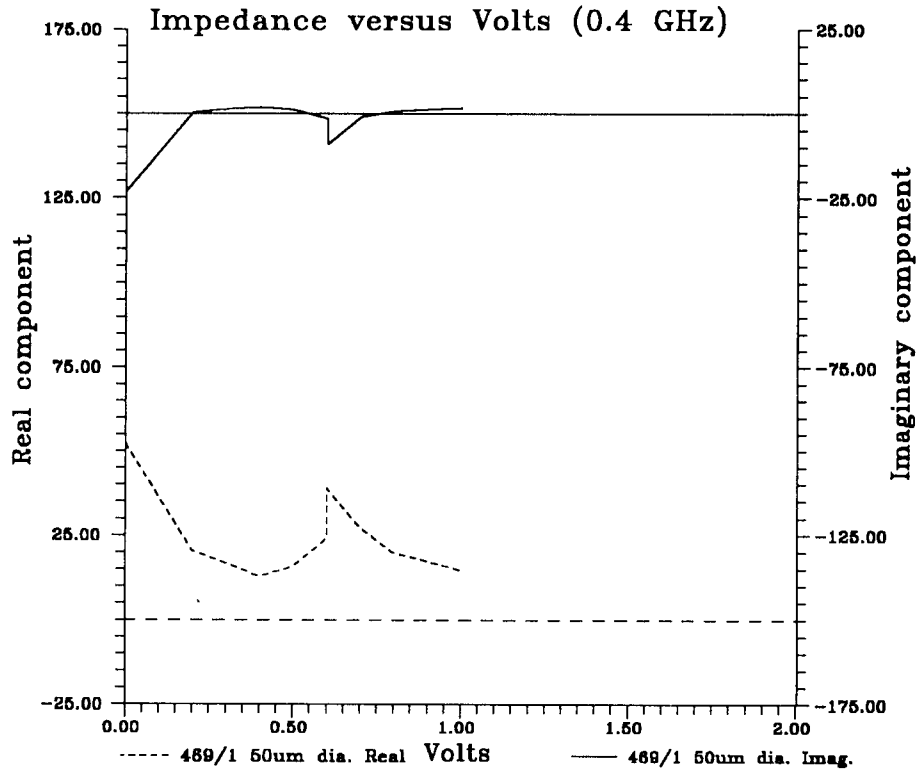


Figure 4.16 a

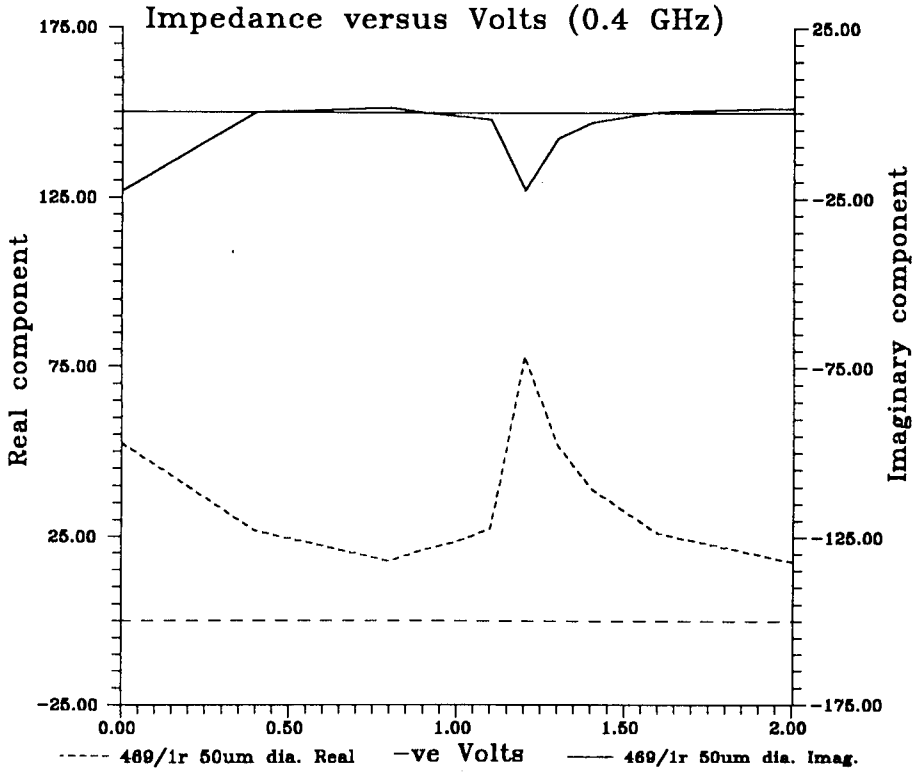


Figure 4.16 b

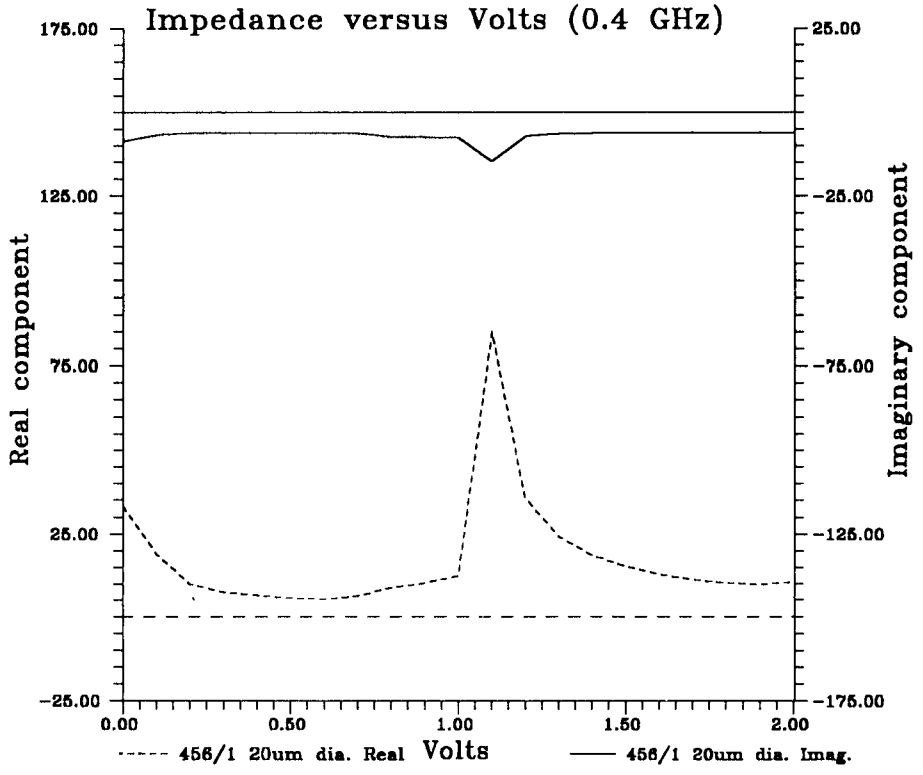


Figure 4.17 a

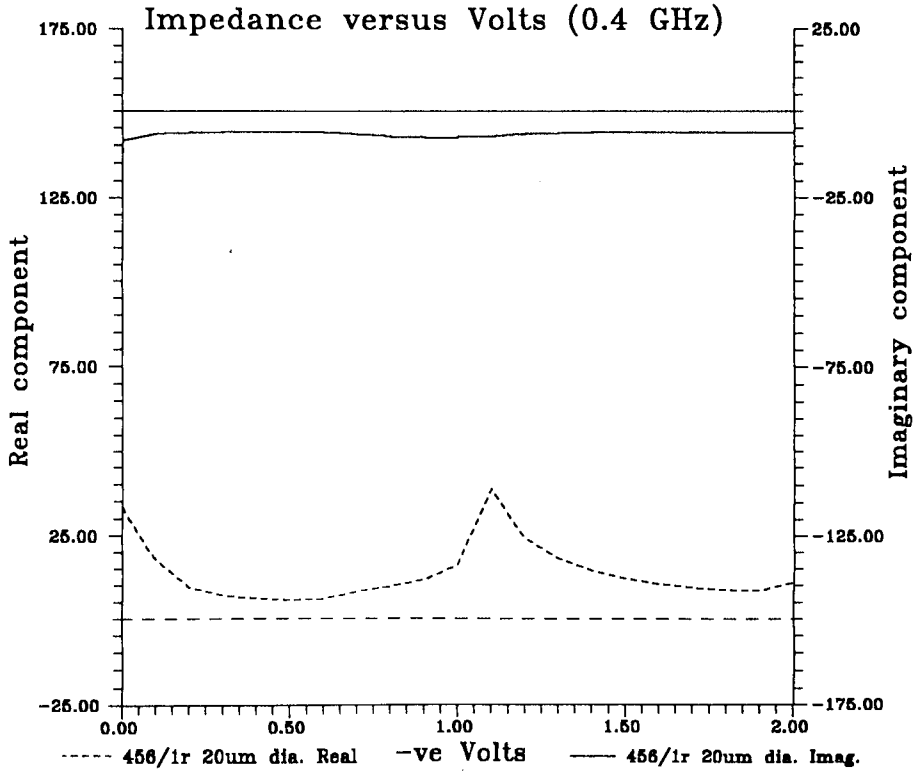


Figure 4.17 b

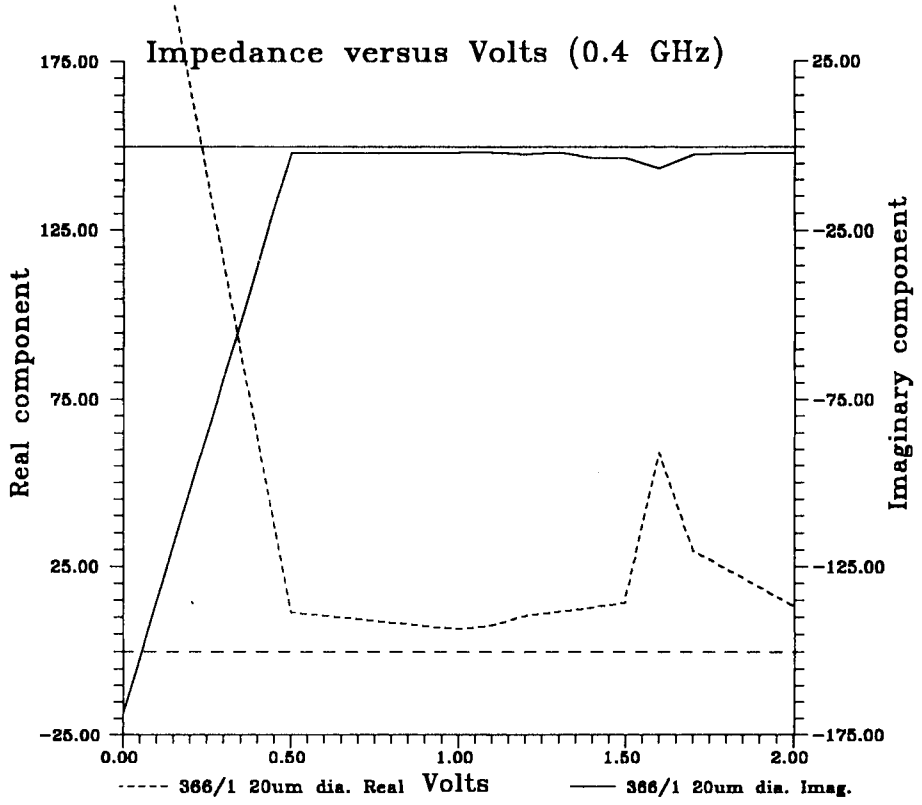


Figure 4.18 a

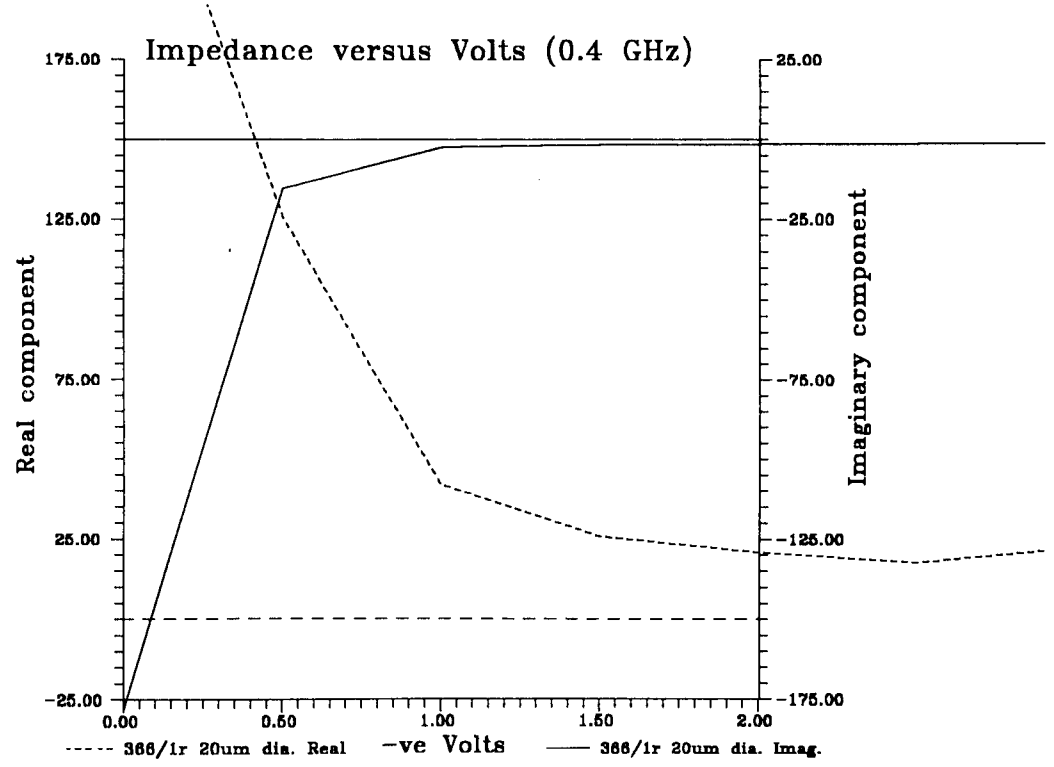


Figure 4.18 b

To understand the general trends of Figures (4.12-4.18) it is appropriate to begin with the intentionally symmetric wafers eg. NU-195, NU-455 and NU-456. The discussion in this section is helped by referring to a model of a DBRT device which is discussed more fully in section 4.3.1, Figure 4.20 and Equation 4.4. This model, due to Gering et al [4] considers the DBRT junction as a combination of a resistor and capacitor in parallel. The resistor is represented by the differential resistance and the capacitor is simply the parallel-plate junction capacitance arising from the charge separation length at the junction.

The trends in the measured real and imaginary resistances result from the parallel combination of the device junction capacitance and resistance, as noted in 4.2.5. It is therefore difficult to visualize the consequences of the individual real and imaginary impedance trends from the behaviour of either the capacitance or the resistances taken separately. This combination effect explains why the imaginary component of impedance initially decreases with bias, rather than increasing as might be expected as a result of the reducing (voltage-dependent) value of capacitance. As a result the behaviour of the imaginary component of the impedance and that of the real component tend to "mirror" one another. This is demonstrated most clearly in Figure 4.15, and the dependence of the impedance (on either the capacitance or the resistance of the junction) results mainly from whichever component is dominant at this frequency. A qualitative description of the initial trend in the impedance-versus-voltage characteristic shown in Figure 4.15, is that near zero bias both the differential resistance and the capacitance are high and decrease quite rapidly with increasing bias.

As may be seen from Figure 4.15(a&b) the behaviour is indeed symmetric with polarity as expected from the symmetry of the layer structure. This is not necessarily only dependent on the layer symmetry since unexpected changes (as a result of bonding damage etc.) can nevertheless alter the symmetry in the current-voltage

characteristic and result in polarity-dependent impedance characteristics. The current-voltage characteristic is therefore a good indicator of the degree of symmetry or lack of it which can be expected in the impedance-versus-voltage behaviour. Figure 4.15 also demonstrates how the impedance changes in the vicinity of resonance (0.4v) and how the impedance peaks when the device is biased in the valley region (0.7v).

The relationship between the asymmetric layer structures and their high frequency impedance is shown in Figures 4.13 and 4.14 for the strongly asymmetric structures of NU-453 and NU-454. Again it is important to interpret the overall impedance behaviour as a result of the combination of the resistance and the capacitance. The reduced symmetry of the structures NU-453 and NU-454 increases the resistance, especially at low voltages, and this alters the relative importance of the capacitance on the overall impedance as compared to the symmetric case (eg. NU-455). The effect of increasing bias in the case of Figure 4.13(a) to beyond about 0.3 volts restores the balance in the relative importance of the resistance and capacitance to that seen for the symmetric structures, ie a much lower resistance together with a lower value of capacitance.

The following figures show an approximation for determining the device impedance based on only the current-voltage characteristic and a knowledge of the layer structure. Figure 4.19(a) demonstrates how the differential resistance is calculated from the measured current-voltage characteristic while Figure 4.19(b) shows the match between the measured real component of the impedance for 455/3 and the differential resistance calculated from the d.c. current-voltage characteristic. However, it is worth remembering that the magnitude of the real part of the impedance is given by the real part of the combined junction resistance and capacitance, which would account for slight differences in the measured real component of the impedance versus the calculated differential resistance. Figure 4.19(c) shows the differential resistance and capacitance calculated solely from theory (section 3.3.4).

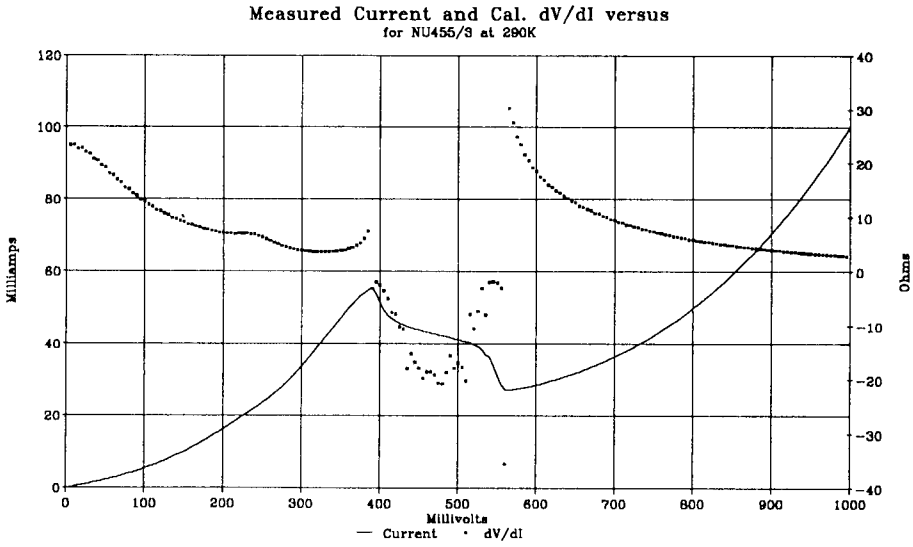


Figure 4.19 a Measured I-V (solid line) & calculated dI-dV (dotted line) versus voltage.

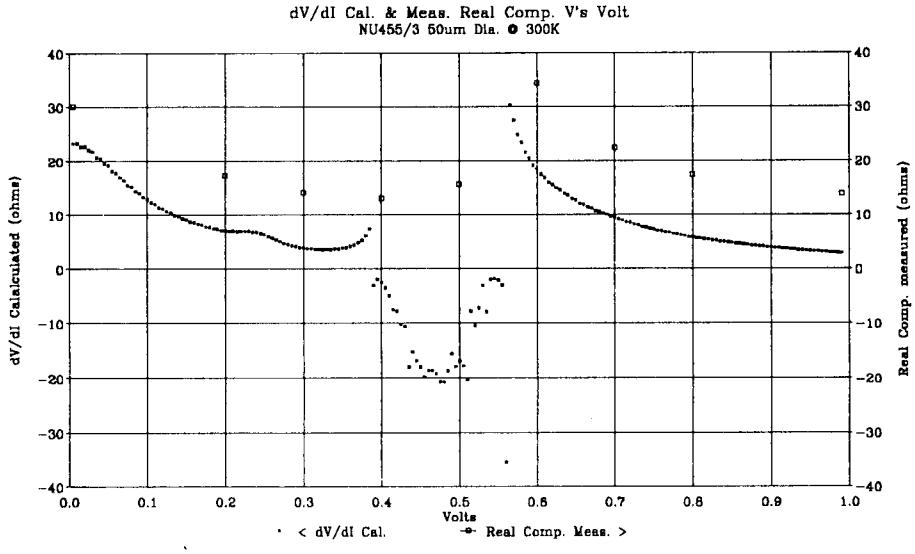


Figure 4.19 b Measured real component of impedance (open boxes) & calculated dI-dV (dotted line) versus voltage.

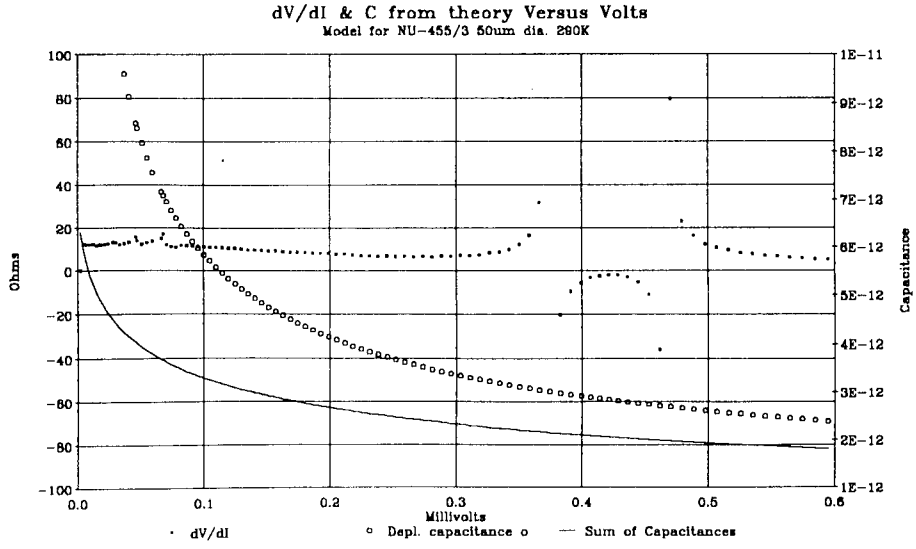


Figure 4.19 c Differential resistance and capacitance calculated from theory.

From Figure 4.19(c) (compared to Figure 4.19(b)) it can be seen that there is an approximate match between the theoretical behaviour and the measured performance. It is doubtful if this approximate performance is sufficient for system designers. But, such simple estimates of performance based on a measured current-voltage characteristic may help in the selection of likely layer structures for a proposed application.

The trends discussed in the previous paragraphs and shown in Figures 4.12-4.18 give only an indication of the effects of layer parameters on device performance and a more detailed examination requires the device to be represented by an equivalent circuit. It is the variation of the component values in this equivalent circuit which allows a more quantifiable measurement of the effects of layer structure on the impedance.

4.3 Development of equivalent circuit models

The development of an appropriate circuit model to represent the high frequency behaviour of a DBRT tends to proceed from the simplest possible circuit, with the addition of extra components to describe the effects of the package or to improve the fit with the experimental measurements.

4.3.1 The initial model

The starting point for many of these equivalent circuits consists of three series-connected components and follows on from the equivalent circuits used to describe Esaki tunnel diodes [5,6]. An early variation of these circuits was proposed by Gearing et al [4,7] and this circuit is shown in Figure 4.20.

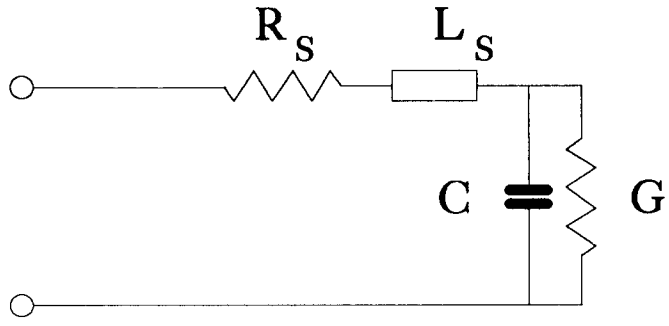


Figure 4.20 A simple equivalent circuit

The most significant difference proposed by Gering et al, between this "new" equivalent circuit and those previously used to describe Esaki diodes, was the inclusion of a series inductor in excess of any inductive contributions of the bondwire (which they believed had been accounted for in their de-embedding procedure). Their explanation for the physical origin of this component was tentatively attributed to the delays associated with the time taken for the confined electrons to tunnel out from the well; the accompanying phase delay is manifest as an inductance. Hence the first element in the circuit is an inductor which includes any possible excess bondwire contributions, but principally accounts for phase delays associated with the electron transport through the semiconductor layers themselves. The value for this inductance proposed by Gering et al [4], was found to be independent of the value of applied bias. Thus it was not thought to be associated with the transit-time delay through the depletion region formed in the collector (under applied bias), which would otherwise be expected to be voltage-dependent.

The second element is a resistor which is the sum of the semiconductor top-contact resistance, the resistance of the semiconducting layers adjacent to the double barrier region itself (cladding layers) and possible excess bondwire resistances which have not been fully de-embedded.

The third element is due to the ("active") junction of the DBRT and consists of two elements, a resistor and capacitor in parallel, both of which are voltage-dependent. The resistance is an approximation of the junction resistance given by the differential of the d.c. current-voltage relationship (to represent the small-signal a.c. resistance), while the capacitance is the approximation of the parallel-plate junction capacitance of the "active" region of the DBRT device.

The value of this junction capacitance is calculated from the sum of the lengths of the undoped double-barrier region and the accumulation and depletion regions. This sum is simply the separation length of the charges in the more heavily doped anode and cathode layers of the semiconductor. The voltage dependence of this capacitance is found from a knowledge of the field across the device from the theoretical model, and is required to give the correct value for the current through the device. The value of capacitance, (obtained via the voltage distribution and hence the depletion lengths across the device) given by the (theoretically) calculated current-voltage characteristic is only approximate, since knowledge of the layer doping and thickness is not exact. Also required for accurate prediction of the voltage distribution throughout the DBRT are quantitative representations of the charge build-up in the well and accumulation regions. However, for accurate system design based on a specific structure then the capacitance-versus-voltage behaviour of the device is best found by low frequency measurements [8,9].

As was previously mentioned, the relatively simple equivalent circuit model shown in Figure 4.20 contains components which are effectively lumped elements arising from a collection of physical contributions in the semiconductor which themselves are not strictly discrete. This description therefore, may not accurately describe the effect that these distributed contributions have on the broadband impedance. An example of a component which is missing from the simple model, or which would be contained within another component of the model (and so obscured), is the effect of the charge

build-up in the well on resonance. Another such example would be the delays associated with the transfer of charge into and out from the well (ie. inductance) which, if present (and large), would more correctly appear near or in series with the junction resistance and in parallel with its capacitance. Hence this would be expected to be shorted by the parallel junction capacitance at high frequencies. This shunting effect would not occur if the inductance appeared as shown in the previous model. In consequence other, more refined, equivalent circuit models have been developed which seek to include some of these effects.

4.3.2 A more accurate model

The purpose of the following model shown in Figure 4.21 was to seek to improve the match between measured device performance and the predicted performance using a more physically realistic equivalent circuit [10]. The difference between the model of Figure 4.21 and that of Figure 4.20 is that the double-barrier region is more appropriately described by an additional capacitance and series (charging) resistance in parallel with the capacitance associated with the accumulation and depletion regions.

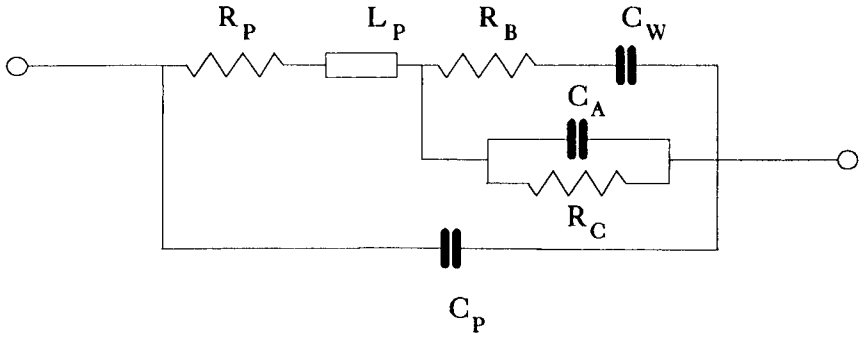


Figure 4.21 A more exact model

The additional capacitance and its series resistance represents the possible effect of stored charge in the well on the high frequency impedance.

The model was arrived at by breaking the junction capacitance into two components; one being the normal depletion capacitance and the other due to the charge in the well. Hence the charge in the depletion region is terminated on both the accumulated charge in the well and also on that accumulated in the emitter region. The depletion capacitance (C_A) and junction resistance (R_C) are then in parallel with a series combination of the well capacitance (C_W) and its associated charging resistance (R_B).

The charging of the well capacitance is controlled by a resistance which in the case of the symmetric structure is simply the more "opaque" emitter barrier. This situation may be complicated if there is a great deal of charge already in the well; under these circumstances the occupancy of the well states determines the charging of the well and, in effect, limits the current through the device. This is likely to occur if the transmission through the collector barrier was very much lower than that of the emitter, thereby favouring the storage of charge in the well. However, the extra charge stored in the well (due to the more opaque collector barrier) may be balanced by the reduced number and spread in energy of the confined states in the well (occurring as a result of the large asymmetry in the barriers, see Figure 3.3) and leading to a reduction in the current. The net result may not be a noticeable increase in the well capacitance. The charging resistance in the above case of a more "opaque" collector barrier may now be controlled instead by the rate at which charge tunnels out of the well through this collector barrier, rather than the emitter barrier as in the case of the symmetric structures.

It was a consideration of the above effects on the charge storage in the well, and the possible inductive effect (of the extra time delay for the charge to tunnel through the

collector barrier) which motivated the growth of the asymmetric and symmetric series of structures (NU-453, NU-454 & NU-455). The inductive effect of the delay in the charge tunnelling out of the well is discussed in the next section and was included in the final model (section 4.4 and Figure 4.23) used to describe the device. This final equivalent circuit model is simply the combination of the previous more accurate model with that proposed by Brown et al [11]. Before this final model is discussed, however, three further relevant models will be reviewed briefly.

4.3.3 High frequency cut-off model

In the previous section the possible requirement of an inductance in series with the junction conductance was discussed. The necessity for this component in the equivalent circuit was noted by Gering et al [4] but was placed in series with the junction capacitance as well as the junction resistance. Brown et al [11], on the other hand, placed this inductance in series with the junction resistance but in parallel with the junction capacitance as shown in Figure 4.22. Their rationale for placing the inductance at this point in the circuit was to explain the observed premature roll-off in the measured oscillation power which could not otherwise be accounted for by the simple parallel combination of a resistance and capacitance alone.

Brown et al [11] attributed this inductance, which they termed the "Quantum inductance", to the temporal delay associated with the quasi-bound state lifetime of electrons in the well. This was theoretically based on the results of the quantum-mechanical Liouville equation in the limit where the frequency approaches the quasi-bound state lifetime and results in the imaginary component of the small-signal transfer admittance becoming inductive [12]. The value for this inductance (L_{QW}), they suggested, was approximated to the quasi-bound state lifetime (τ) divided by the junction conductance (G). However, this then results in the value of this inductance

becoming negative in the negative differential conductance region. This negative inductance should then be used in their model, since their measurements were made when the device was indeed biased in this voltage range (ie for oscillation to take place). Also, during their measurements the device was being operated in the large-signal regime, but their theoretical calculations were based on a small-signal analysis. Furthermore, this analysis was based on the coherent picture of device operation and not the sequential picture (see section 3.3.3); the times associated with establishing the resonant state in the coherent case have been shown to be inconsistent with the operation of these devices at very high frequencies [13,17].

Despite this criticism of the calculations of Brown et al [12] there arguably remains a requirement for some sort of inductive effect (perhaps associated with the tunnelling and dwell times of electrons in the well) responsible for the premature roll-off in oscillator performance. However, the need remains for the frequency dependent skin-effects (along the top and sides of the multi-dot chip, Chapter 2.3.3) to be properly accounted for at these very high frequencies, before attributing the premature roll-off in performance to an "intrinsic" quantum inductance. For a recent discussion based on linear response theory see Fu & Dudley [14]. In the final model (4.4.4) an inductance has been included, but its value was only found to be significant under certain circumstances.

4.3.4 The quantum well injection transit-time model

A quantum well injection transit-time (QWITT) model for a DBRT with an accompanying low doped "drift" or transit-time region adjacent to the collector barrier was first proposed by V. P. Kesan et al [15]. In this model the presence of an extra length of depleted semiconducting material "down-stream" of the collector barrier causes a phase delay which, if added to the delay associated with the electrons tunnelling through the barriers, can result in an improved efficiency in generating

microwave power at a particular frequency [16]. In some cases the phase delay of the active region together with the "transit-time" region become comparable with the oscillation period, which may favour transferral of the kinetic energy from the d.c. field to the a.c. field.

For completeness the following is a discussion of the implications of the presence of such a "drift" region. However, for the measurement frequencies used in this study, the phase delay associated with the time taken for the carriers to cross the drift region is very small and therefore was not thought to contribute to an excess inductance.

From the treatment of Kesan et al. [15] the following is an expression for the specific impedance of the transit-time region which is itself dependent on the injection conductance of the double barrier region and in turn depends on the bias point is given by;

$$Z_{tt}=\frac{W}{j\omega\epsilon}\left[1-\frac{\sigma}{\sigma+j\omega\epsilon}\frac{1-\exp(-j\theta_d)}{j\theta_d}\right] . \tag{4.5}$$

Where ε is the dielectric constant of the drift region, $\theta_d = \omega W/v_s$ is the drift angle where v_s is the saturation velocity and W is the length of the drift region. The normalized injection conductance is

$$\sigma = l\left(\frac{\partial j_{QW}}{\partial V_{QW}}\,|v_0\right) \tag{4.6}$$

and where j_{QW} and V_{QW} are the instantaneous current density and voltage, v_0 is the d.c. bias voltage and l the length of the double barrier region.

To demonstrate the significance of this transit-time effect in relation to a typical device structure as used in this study, the above equations are solved for the impedance of the transit-time region alone. Consider a 50μm diameter device from NU-455 at two frequencies 12 & 100GHz. At each of these frequencies two examples of specific conductivity of the double barrier region of $\pm 2.5*10^{6}\Omega^{-1}m^{-2}$ were chosen, to represent both a positive and negative differential junction resistance. The two examples of specific conductivity are for bias conditions corresponding to before and during resonance. The impedance is calculated for a typical depletion region length of 500Å where the sum of the barrier and well regions is 150Å. The normalized injection conductance becomes $\pm 37*10^{-3}\Omega^{-1}m^{-1}$ from (4.6), and if the velocity through the drift region is $4*10^{5}ms^{-1}$ this represents a drift angle of $1.5*10^{-3}$ & $12*10^{-3}$ radians for 12 & 100GHz respectively. Hence the (series) impedance of the transit-time region is:

$Z_{TT} = \pm 0.014*10^{-3} - j3.18$ at 12GHz, and $Z_{TT} = \pm 0.2*10^{-3} - j\ 0.377$ at 100GHz.

It is worth noting that the reactive components equate to a capacitances of value 4.17pF and 4.22pF respectively, and that this is simply the parallel-plate capacitance of a depletion region of width 496Å and of 50μm in diameter. These findings are consistent with such small delay angles, and suggest that transit-time effects through a depletion region of this thickness contributes only slight inductances even up to frequencies as high as 100GHz. However, for frequencies of many hundreds of giga-hertz, and depletion lengths greater than this, the delay angles are without doubt significant.

4.3.5 A more physical model

This model was introduced in section 3.4.2 and consists simply of two parallel combinations of a resistance and capacitance which are then connected in series. This description is for the junction (or double barrier) region alone, and the two parallel combinations in series represent the two barriers. The model was developed to describe the effect on impedance of charge build-up in the well. The model also contains expressions for the impedance of each barrier which explicitly rely on the tunnelling and well-charge escape times and so should be well suited to model the microwave behaviour. The main drawback of this very physical approach is that it relies upon accurate calculations of the barrier-tunnelling and stored-charge escape times and these are exponentially dependent on the height and width of the barriers. Hence, this more physical approach to modelling is very sensitive to the calculation of these heights and lengths. An accurate model to describe the voltage distribution throughout the device, which also takes account of the charge build-up in the well, is therefore essential to use this model approach with confidence.

One such theoretical calculation was described in Chapter 3 but unfortunately it did not fully account for charge build-up in the well on resonance for the strongly asymmetric structures of NU-453 and NU-454. However, for the symmetric structures such as from NU-455 the match between the modelled and measured current-voltage characteristics were reasonable (Figures 3.6 & 3.7). The model described in the previous paragraph does not include effects due to contact and spreading resistances, nor does it include vestigial bond-wire contributions, and so it has to be embedded in another circuit model which does account for these factors.

From Chapter 3, the small-signal a.c. model is developed again as a reminder and is as follows:-

The decay rate through the collector barrier is τ_c^{-1}, given by equation (3.73) and the decay rate through the emitter barrier (τ_e^{-1}) is calculated in a similar way to that for the collector barrier. The conductance which controls the charging of the well $R_{chg}^{-1}=(df/dV_e)$ and is also $R_{chg}=(\tau_{chg}/C_e)$, and $\tau_0^{-1} = \tau_e^{-1} + \tau_c^{-1}$. The impedance can then be divided into two parts, $Z(\omega) = Z_e(\omega) + Z_c(\omega)$ where, $Z_e(\omega) = \delta V_e/\delta I$ and $Z_c(\omega)=\delta V_c/\delta I$, giving:

$$Z_e^{-1} = j\omega C_e + \frac{1}{R_{chg}} \frac{j\omega + \tau_c^{-1}}{j\omega + \tau_0^{-1}} \tag{3.83}$$

for the emitter barrier and similarly for the collector barrier,

$$Z_c^{-1} = j\omega C_c + \frac{1}{R_c} \frac{\tau_{chg}^{-1}}{j\omega + \tau_0^{-1} + \tau_{chg}^{-1}} , \tag{3.84}$$

where $R_c = (\tau_c/C_c)$.

The circuit realization for these two parallel combinations of elements is shown in Figure 4.22, where G_e' and G_c' are the right-most terms in equations 3.83 and 3.84, which in turn can be thought of as being composed of a series combination of resistive and reactive components. The performance of this model compared with the measured impedance (for a device from NU-455) is shown in section 4.5.

Through algebraic manipulation (for the low frequency extreme ie. all τ's$<<1/f$), equations 3.83 and 3.84 could be combined to represent a parallel combination of a

resistance and a capacitance (where each real and imaginary component would consist of a number of terms), and the circuit of Figure 4.22 would reduce to that of Figure 4.20. Hence at low frequencies, the real and imaginary components of the overall circuit combination ($G_e^{-1} + G_c^{-1}$), may be dominated by terms which reduce to a capacitance (which is the sum of the barrier capacitances in series), in parallel with the terms which reduce to the overall d.c. conductance. The equivalence of the various models can then be appreciated.

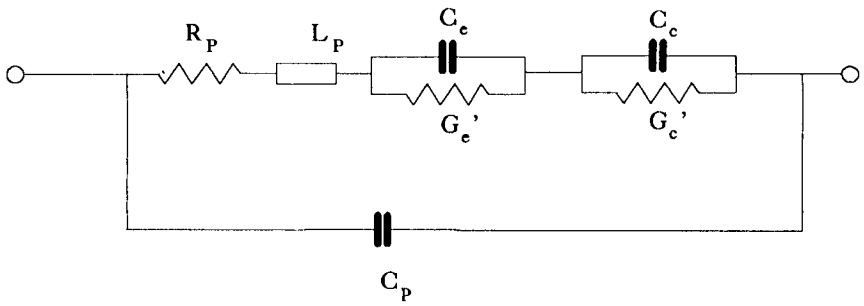


Figure 4.22 A more physical model

4.4 Reconciliation of results with the model behaviour

In section 4.3 we discussed the various small-signal models which have been proposed to describe the high frequency behaviour of DBRT devices. In this section we set out to compare the frequency performance of some of these equivalent circuit models with the experimental data, collected up to 12GHz, and covering many different devices from specifically chosen layer structures. The study was to have been complemented by small-signal impedance measurements up to 100GHz (Chapter 5.1.1). This further study was intended to better illuminate effects such as transit-time delays through the low doped layers adjacent to the double barriers themselves (section 4.3.3), and delays associated with the transfer of charge into and out from the well region. For further

details see Chapter 5.

4.4.1 Comparing modelled and measured device performance

The process used to assess the match between the performance of a model and the performance of a measured device involves a simple visual comparison between the frequency behaviour of the model and that of the measured device, when both are displayed graphically on a Smith-chart. This form for graphically viewing the impedance was chosen because of the ease of presenting (i) the wide range of impedance observed through normalisation to 50 ohms and (ii) the use of a scale which magnifies the effect of changes in impedance when the impedance is itself small. In addition, the balance between the real and imaginary components of the impedance can be seen in the Smith-chart from their behaviour with respect to: the circles of constant resistance, the central equator (which shows the solely real component) and the arcs of constant reactance which represent positive reactance, or inductance, above the equator and represent negative reactance or capacitance below the equator.

The component values in the equivalent circuit model were chosen initially from simple calculations of parallel plate capacitance values and contact resistances, and a knowledge of the differential resistance of the d.c. current-voltage characteristic at each of the bias points. The values for the other components remained negligible unless a finite value was found to be necessary to achieve a reasonable fit to the measured behaviour. The values for the different elements were varied individually in what approximated to a logarithmic search method and then the other elements were varied iteratively until the best possible match was achieved.

4.4.2 Effect of Signal-power on measured impedance

The following are a few cautionary notes concerning the measurement of small-signal impedance of non-linear devices: Firstly, the incident power of the signal needs to be as low as possible without adversely affecting the measurement accuracy. Secondly, at certain points on the current-voltage characteristic where the resistance is high even such small incident signal powers can be sufficient to modify the average position of the operating point on the current-voltage characteristic at which the impedance is being measured and so small-signal conditions no longer apply. This is especially true if there is a strong degree of asymmetry in the current-voltage characteristic in addition to a high resistance. This situation may occur at zero bias, as in detector applications [17]. Finally, when connected to the network analyzer it proved difficult to bias the device to an exact point on the current-voltage characteristic. As a result of these problems the exact operating point on the current-voltage characteristic at which the microwave measurements were carried out is slightly uncertain.

4.4.3 Effect of device conductance on the confidence of the models

The effect of either very high junction capacitance or conductance was seen to shunt the probe signal past some of the more "interesting" components of the model. That is those components of the model which would otherwise describe some of the more physical processes associated with the active region of the device. In consequence the sensitivity of the performance of the device to these components of the model was reduced if either component was very much larger than another.

The instantaneous impedance of a DBRT device is strongly dependant on the layer structure and the bias voltage, and, in practice, many equivalent circuit models will describe the actual impedance behaviour under different conditions for devices from

the same layer structure. The ephemeral nature of these models therefore can obscure the evidence which would support one particular equivalent circuit model in preference to the alternatives. The obvious solution would be to measure many such devices from many different layers and to develop models for each example. This is exactly what was attempted in the course of this study but for reasons described previously, such a study was limited by the magnitude of the task and the manual approach used. An ideal method for overcoming these problems would be to carry out on-wafer auto-probing at microwave frequencies, to measure the impedance of a very large selection of devices and layer structures at many biases and to automate the development of equivalent circuit models for each of these measurements.

4.4.4 Explanation for device behaviour in terms of equivalent circuit values

For clarity the following description of the device behaviour is restricted to only one equivalent circuit and this is shown in Figure 4.23. This circuit can be seen to be a combination of the circuits described in section 4.3 and was used because it was best suited to describe the performance measured under many different conditions. It can be seen that under certain conditions where some of the component values reduce to very small values, the circuit of Figure 4.23 reduces to that proposed by others such as was discussed in section 4.3.1 (ie. Figure 4.20). This is also evident for example in Table 4.2(j) where the values of L_{40} and C_{50} required by the model can be seen to be negligible.

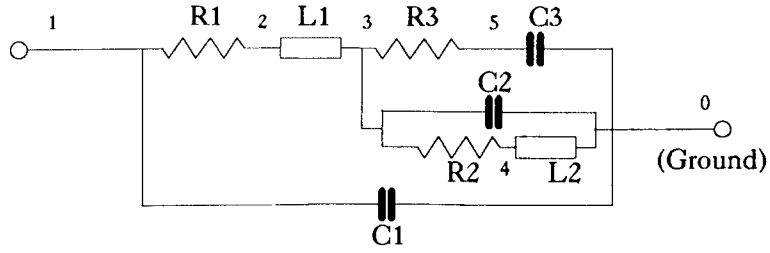


Figure 4.23 A more comprehensive equivalent circuit layout.

In the circuit diagram shown in Figure 4.23 the elements and their correspondence to components of the actual device are as follows:-

C1 between nodes 1 and ground (node 0) describes any excess shunt capacitance due to the package which may not have been de-embedded completely and which should be low with respect to the other capacitances used in the model.

R1 between nodes 1 and 2 represents: the sum of the contact resistance, any excess bondwire resistance which has not been de-embedded and the frequency dependent spreading resistance due to the "skin-effect" in the surface layers.

L1 between nodes 2 and 3 represents any excess bondwire inductance and any other inductive contributions in series with the junction and thought to arise from the properties of layers adjacent to the barriers, under certain conditions.

R2 between nodes 3 and 4 represents the junction resistance.

L2 between nodes 4 and 0 or ground takes account of delays associated with the time taken to establish equilibrium in the field across the double barrier region in response to a rapid change in the potential applied across this region. Such delays have been suggested by Sollner et al [18,14] and are represented as an inductance in series with the junction conductance.

C2 between nodes 3 and ground represents the capacitance depending on the separation length of charges in the emitter and collector regions of the devices.

R3 between nodes 3 and 5 is considered to be a resistance which determines

the rate of charging or discharging of charge in the well, and was therefore difficult to estimate. An initial value was based on a small multiple of the junction resistance and was subsequently varied to improve the match between the measured and the modelled performance if required.

Finally C3 between nodes 5 and ground represents a capacitor associated with the charge stored in the well. This was used as necessary to improve the match between the measured and the modelled performance.

The effects of excess bond wire inductance ($L_{2,3}$) can be seen in Table 4.2(g & h), where an I-bond 4.2(h) appears to contribute an extra 0.2nH in series with the device itself. This is in agreement with the reported findings mentioned in section 4.14. Values of series inductance much greater than this hint at either a very thin "neck" in the bond wire which could have occurred during the bonding process and which would have gone un-noticed during the d.c. inspection, or contributions arising from layer-dependent processes in the device itself, such as transit-time delays etc. If this excess inductance ($L_{2,3}$, as seen in Table 4.2(a, i, and j)) does indeed arise from such transit-time effects in the depleted fraction of this low doped region, as suggested by Kesan et al [15], then these effects could be expected to be field (ie. voltage) dependent and their value should therefore vary with voltage. However, no such voltage-dependence is observed for $L_{2,3}$ (see Table 4.2 (a)).

There were however, cases where evidence supporting the presence of $L_{2,3}$ was found but no I-bond was suspected for example in devices from NU-195, NU-366 and NU-469, all of which contain one or more wide low-doped "cladding" regions. As mentioned previously the lack of an obvious voltage dependence in the value of $L_{2,3}$ (for these layers) suggests that the depletion effects are not responsible. It is noted

however, that the inductance $L_{2,3}$ does seem to be associated with the presence of these "drift" (or "cladding") regions.

The value of parallel-plate junction capacitance ($C_{3,0}$) seen throughout Table 4.2(a-j) is not found to be simply dependent on area alone but also on the layer structure. Usually, however, this area-dependent scaling is appropriate for predicting the approximate value of junction capacitance (for devices from the same layer structure), as is shown in Table 4.2(e&f, and also i&j). Some layer-structure dependence of the junction capacitance was anticipated but the large variations shown in Table 4.2(c&f), for devices of similar area and nominally similar layers adjacent to the junction, were unexpected. An explanation for this behaviour will be suggested later.

The effect of temperature on the impedance-versus-voltage characteristic is shown in Figure 4.8 for device 455/3. These measurements have also been made for 455/1 and 456/1 and the equivalent circuit elements are shown in Table 4.2(e,f and g respectively). The points of note are that at low bias the junction conductance is very low ($R_{3,4}^{-1}$) while the value at finite bias rises very rapidly. It can also be seen that at low temperature (Table 4.2(e,f &g)), when the value of junction conductance is very low (at 0v), the junction capacitance is simultaneously very large and the value of $R_{1,2}$ rises slightly due to poorer contact resistance. Also at low temperature the application of a finite bias drops this capacitance to a value which is similar to that for the same voltage at room temperature. Again the reasons for this are unclear but the correspondence (of low conductance and high capacitance) is also seen in other devices at room temperature, such as 453/4, 454/4 and 195/c.

The effect of layer structure on the performance will now be discussed. The primary objective was to try to isolate the effect of the individual barriers and especially the effect of the collector barrier, on the overall performance. The effects of both the asymmetry of barrier heights and the barrier thicknesses is discussed at length later but

a brief introduction will now be given.

The collector barrier was thought to influence the time taken for the electrons to escape to the collector region when confined in the well, and so changes in the barrier height and thickness should greatly affect the inductance associated with the well and also the charge storage in the well. Similar studies have been carried out by others but they relied on increases in the thickness of the collector barrier to increase the tunnelling time. In the present study, changes were made in the height of the collector barrier. These studies have previously been carried out by Eaves et al at d.c. and at very low frequencies [19]. However, for the present high frequency study, the variation of barrier thickness was thought to introduce a second variable, namely, a change in junction capacitance as a result of the thickness variation. Therefore, the variation of barrier height rather than width was chosen to control the tunnelling time.

The contribution of layers which are adjacent to the barriers to the overall impedance, was investigated mainly through the effect on the required value of the modelled junction capacitance. In particular, the effect of especially long "drift" or transit-time regions adjacent to the barriers was also expected to be seen clearly from the measurements and the subsequent equivalent circuit values.

The value of capacitance used in the models was found initially by simple parallel-plate calculations based on the separation of the more heavily doped layers in the emitter and collector regions but including an extra length related to depletion effects at zero applied bias. The eventual values quoted in Table 4.2 were then arrived at by varying these initial values to improve the match between modelled and measured performance. The extra length referred to above is included to account for cases where the asymmetric doping on either side of the barriers would cause a slight dipole to be formed. At zero applied voltage this length should be relatively easy to calculate, however under an applied bias both an accumulation and depletion region

are formed. An accurate calculation of the bias-dependent accumulation and depletion lengths is difficult (Chapter 3) but an approximate length for the depletion region can be found from a knowledge of the doping in this region, and by using an abrupt junction calculation. Generally the agreement between the calculated value of junction capacitance and the value required for the model is good (± 30% for the low conductance devices from layers NU-195, NU-453 & NU-454). Unfortunately, this was not the case for the higher conductance devices from NU-366, NU-455, NU-456 and NU-469 with the calculated value being typically >250% of the measured zero biased value (see Table 4.2 and the layer structure diagrams in A1).

The low value suggested (by the model) for the junction capacitance of devices from NU-366, NU-455, NU-456 and NU-469 (Table 4.2) corresponds to apparent charge separation lengths of two or more times the lengths which could be justified by simple calculation. The reason for these results was unknown but there does seem to be an association between the low value of capacitance and a correspondingly high value of conductance as suggested from the models.

In the case of the devices which were asymmetrically doped on either side of the junction (NU-366 and NU-469), a zero biased depletion region could be expected to form. The approximate length of this depletion region can be calculated from the Debye screening length in the lower doped layer adjacent to the barriers, which is ~200Å for NU-366 and ~300Å for NU-469. With the addition of this extra length to that of the undoped barrier and other layers, then the simple calculation for the capacitance agrees much more closely with the value suggested by the models. For devices from NU-455 and NU-456 the doping is symmetric on either side of the barriers, and the presence of a significant zero-biased depletion region was not expected. Hence, for devices from layers NU-455 and NU-456, the low values of capacitance suggested from the measurements and the subsequent models must have arisen from a different mechanism to the formation of depletion regions due to

asymmetric doping. It should be noted that, in the case of the low temperature measurements on devices from NU-455, the suggested model value for capacitance was in much better agreement with the value calculated from the layer structure (see Table 4.2(e&f)). For example at 77K, the modelled value of the junction capacitance for 50μm and 20μm diameter devices increases from 2pF to 16pF and from 0.6pF to 3.8pF respectively, which would require an approximate sixfold reduction in depletion length. The most likely explanation for the lower than expected values of $C_{3,0}$,which were suggested from models for devices from NU-455 and NU-456, is that the especially low values of conductance (particularly at higher voltages) compromise the accuracy of the measured values and confuse the subsequent values of the equivalent circuit elements.

Table 4.2 (a-j) summarises the comparative results of measured S-parameters with those calculated from equivalent circuits with elements which are arrived at by initial calculations and thereafter by iterative adjustment. The final values were chosen to give good agreement between the measured and modelled impedance when viewed on smith-charts (Figures 4.23-4.27). Device-to-device and layer structure differences are revealed by comparison between the values suggested by the equivalent circuits and listed in Table 4.2.

APPLIED BIAS	EQUIVALENT CIRCUIT ELEMENT VALUES FOR DEVICE 195_C 50 μm Dia.							
(V)	R_{12} (Ω)	L_{23} (nH)	R_{34} (Ω)	L_{40} (nH)	R_{35} (Ω)	C_{50} (pF)	C_{30} (pF)	C_{10} (pF)
0.0	0.2+0.01*f	0.3	2000	0.01	8000	0.01	9	0.03
0.1	0.2+0.01*f	0.3	1300	0.01	5000	0.01	8	0.03
0.2	0.2+0.01*f	0.3	650	0.01	400	0.03	7.5	0.03
0.3	0.2+0.01*f	0.3	350	0.01	500	0.1	6.7	0.03
0.4	0.2+0.01*f	0.3	220	0.01	500	0.01	6	0.03
0.5	0.2+0.01*f	0.3	80	0.01	500	1.5	5.5	0.03
0.52	0.2+0.01*f	0.3	100	0.01	500	1.5	5	0.03
0.54	0.2+0.01*f	0.3	100	0.01	500	1.5	5	0.03
0.56	0.2+0.01*f	0.3	-250	0.01	500	0.05	4.8	0.03
0.58	0.2+0.01*f	0.3	-250	0.01	500	0.05	4.8	0.03
0.6	0.2+0.01*f	0.3	-250	0.01	500	0.05	4.8	0.03
0.7	0.2+0.01*f	0.3	1500	0.01	500	0.05	7	0.03

Table 4.2 a

APPLIED BIAS	EQUIVALENT CIRCUIT ELEMENT VALUES FOR DEVICE 366_1 20 μm Dia.							
(V)	R_{12} (Ω)	L_{23} (nH)	R_{34} (Ω)	L_{40} (nH)	R_{35} (Ω)	C_{50} (pF)	C_{30} (pF)	C_{10} (pF)
0.0	0.5+0.01*f	0.01	380	0.01	1000	0.03	0.42	0.03
0.5	0.5+0.01*f	0.01	11	0.07	100	0.03	0.8	0.03
1.0	0.5+0.01*f	0.01	6	0.04	100	0.03	0.8	0.03
1.2	0.5+0.01*f	0.01	9	0.12	100	0.03	0.8	0.03
1.4	0.5+0.01*f	0.01	12.5	0.85	100	0.03	0.8	0.03
1.6	0.5+0.01*f	0.01	59	0.01	100	0.03	0.3	0.03
2.0	0.5+0.01*f	0.01	12.5	0.09	100	0.03	0.7	0.03
-0.5	0.5+0.01*f	0.01	125	0.01	100	0.03	0.12	0.03
-1.0	0.5+0.01*f	0.01	41	0.01	100	0.01	0.13	0.03
-1.5	0.5+0.01*f	0.01	25.5	0.01	100	0.01	0.16	0.03
-2.0	0.5+0.01*f	0.01	20	0.01	100	0.01	0.16	0.03
-2.5	0.5+0.01*f	0.01	17	0.01	100	0.01	0.15	0.03
-3.0	0.5+0.01*f	0.01	21.5	0.01	100	0.01	0.1	0.03

Table 4.2 b

APPLIED BIAS	EQUIVALENT CIRCUIT ELEMENT VALUES FOR DEVICE 453_4 50 μm Dia.							
(V)	R_{12} (Ω)	L_{23} (nH)	R_{34} (Ω)	L_{40} (nH)	R_{35} (Ω)	C_{50} (pF)	C_{30} (pF)	C_{10} (pF)
0.0	0.2+0.01*f	0.01	1500	0.01	3000	0.5	12.5	0.03
0.3	0.2+0.01*f	0.01	100	0.01	200	1	10	0.03
0.6	0.2+0.01*f	0.01	50	0.01	200	2	10	0.03
0.9	0.2+0.01*f	0.01	35	0.01	200	0.5	10	0.03
1.0	0.2+0.01*f	0.01	35	0.01	200	0.5	11	0.03
1.2	0.2+0.01*f	0.01	250	0.01	1000	0.5	12	0.03
-0.2	0.2+0.01*f	0.01	400	0.01	1600	0.3	10	0.03
-0.4	0.2+0.01*f	0.01	300	0.01	1000	0.3	7	0.03
-0.6	0.2+0.01*f	0.01	160	0.01	1000	0.3	5	0.03
-0.8	0.2+0.01*f	0.01	100	0.01	500	0.3	3	0.03
-1.0	0.2+0.01*f	0.01	70	0.01	300	0.7	2	0.03

Table 4.2 c

APPLIED BIAS	EQUIVALENT CIRCUIT ELEMENT VALUES FOR DEVICE 454_4 20 μm Dia.							
(V)	R_{12} (Ω)	L_{23} (nH)	R_{34} (Ω)	L_{40} (nH)	R_{35} (Ω)	C_{50} (pF)	C_{30} (pF)	C_{10} (pF)
0.0	0.3+0.01*f	0.01	400	0.01	1000	0.03	1.3	0.03
0.2	0.3+0.01*f	0.01	200	0.01	100	0.03	1	0.03
0.4	0.3+0.01*f	0.01	60	0.01	200	0.3	1	0.03
0.6	0.3+0.01*f	0.01	19	0.02	100	0.4	1	0.03
0.8	0.3+0.01*f	0.01	14	0.01	100	0.01	1	0.03
-0.4	0.3+0.01*f	0.01	190	0.01	100	0.03	1.1	0.03
-0.8	0.3+0.01*f	0.01	130	0.01	500	0.3	1.2	0.03
-1.0	0.3+0.01*f	0.01	190	0.01	400	0.3	1.1	0.03
-1.2	0.3+0.01*f	0.01	100	0.01	600	0.3	1	0.03

Table 4.2 d

APPLIED BIAS	EQUIVALENT CIRCUIT ELEMENT VALUES FOR DEVICE 455_1 20 μm Dia.							
(V)	R_{12} (Ω)	L_{23} (nH)	R_{34} (Ω)	L_{40} (nH)	R_{35} (Ω)	C_{50} (pF)	C_{30} (pF)	C_{10} (pF)
0.0	0.5+0.01*f	0.001	144	0.01	1000	0.6	0.6	0.03
0.2	0.5+0.01*f	0.001	53.5	0.3	300	0.8	0.6	0.03
0.4	0.5+0.01*f	0.001	-88	0.31	200	0.8	0.6	0.03
0.6	0.5+0.01*f	0.001	180	0.01	800	0.2	0.45	0.03
0.8	0.5+0.01*f	0.001	57	0.5	200	0.6	0.5	0.03
1.0	0.5+0.01*f	0.001	36	0.3	150	0.8	0.5	0.03
AS ABOVE BUT MEASUREMENTS CARRIED OUT AT 77 K								
0.0	1.5+0.01*f	0.001	2000	0.01	4000	0.01	3.8	0.03
0.4	1.5+0.01*f	0.001	-80	0.01	100	0.2	0.4	0.03
0.6	1.5+0.01*f	0.001	50	0.01	100	0.01	0.4	0.03
0.8	1.5+0.01*f	0.001	-37	0.01	100	0.01	0.8	0.03

Table 4.2 e

APPLIED BIAS	EQUIVALENT CIRCUIT ELEMENT VALUES FOR DEVICE 455_3 50 μm Dia.							
(V)	R_{12} (Ω)	L_{23} (nH)	R_{34} (Ω)	L_{40} (nH)	R_{35} (Ω)	C_{50} (pF)	C_{30} (pF)	C_{10} (pF)
0.0	0.1+0.01*f	0.01	35	0.01	150	2	2	0.03
0.2	0.1+0.01*f	0.01	20	0.01	40	4	2	0.03
0.4	0.1+0.01*f	0.01	16	0.01	20	5	2	0.03
0.6	0.1+0.01*f	0.01	20	0.8	100	3.1	1.5	0.03
0.8	0.1+0.01*f	0.01	20	0.01	100	3	1.5	0.03
1.0	0.1+0.01*f	0.01	16	0.01	30	2	1.5	0.03
AS ABOVE BUT MEASUREMENTS CARRIED OUT AT 77 K								
0.0	1.0+0.01*f	0.01	450	0.01	1000	0.01	16	0.03
0.2	1.0+0.01*f	0.01	8	0.01	30	0.01	1.6	0.03
0.4	1.0+0.01*f	0.01	5	0.01	15	0.01	1.5	0.03
0.6	1.0+0.01*f	0.01	-6	0.01	15	0.01	3	0.03
0.8	1.0+0.01*f	0.01	-7	0.01	20	0.01	3	0.03
1.0	1.0+0.01*f	0.01	100	0.01	400	0.01	1.5	0.03

Table 4.2 f

APPLIED BIAS	EQUIVALENT CIRCUIT ELEMENT VALUES FOR DEVICE 456_1 20 μm Dia.							
(V)	R_{12} (Ω)	L_{23} (nH)	R_{34} (Ω)	L_{40} (nH)	R_{35} (Ω)	C_{50} (pF)	C_{30} (pF)	C_{10} (pF)
0.0	0.5+0.01*f	0.01	34	0.01	1000	0.01	1	0.03
0.2	0.5+0.01*f	0.01	10	0.07	1000	0.01	0.6	0.03
0.4	0.5+0.01*f	0.01	6	0.05	1000	0.01	0.4	0.03
0.6	0.5+0.01*f	0.01	6	0.07	100	0.01	0.4	0.03
0.8	0.5+0.01*f	0.01	10	0.07	1000	0.01	0.4	0.03
1.0	0.5+0.01*f	0.01	15	0.07	1000	0.01	0.4	0.03
1.2	0.5+0.01*f	0.01	35	0.25	1000	0.01	0.4	0.03
1.4	0.5+0.01*f	0.01	18	0.12	1000	0.01	0.3	0.03
1.6	0.5+0.01*f	0.01	12	0.1	1000	0.01	0.3	0.03
1.8	0.5+0.01*f	0.01	10	0.07	1000	0.01	0.3	0.03
AS ABOVE BUT MEASUREMENTS CARRIED OUT AT 77 K								
0.0	3.0+0.02*f	0.01	800	0.02	1000	0.01	1	0.03
0.4	3.0+0.02*f	0.01	6	0.01	50	0.01	0.4	0.03

Table 4.2 g

APPLIED BIAS	EQUIVALENT CIRCUIT ELEMENT VALUES FOR DEVICE 456_4 20 μm Dia. I-bond							
(V)	R_{12} (Ω)	L_{23} (nH)	R_{34} (Ω)	L_{40} (nH)	R_{35} (Ω)	C_{50} (pF)	C_{30} (pF)	C_{10} (pF)
0.0	0.5+0.01*f	0.2	55	0.01	1000	0.01	2	0.03
0.2	0.5+0.01*f	0.2	15	0.01	1000	0.01	1.6	0.03

Table 4.2 h

APPLIED BIAS	EQUIVALENT CIRCUIT ELEMENT VALUES FOR DEVICE 469S_1 20 μm Dia.							
(V)	R_{12} (Ω)	L_{23} (nH)	R_{34} (Ω)	L_{40} (nH)	R_{35} (Ω)	C_{50} (pF)	C_{30} (pF)	C_{10} (pF)
0.0	2+0.02*f	0.3	300	0.01	1000	0.01	0.6	0.03
0.2	2+0.02*f	0.34	55	0.01	1000	0.01	0.5	0.03
0.4	2+0.02*f	0.3	26	0.01	1000	0.01	0.45	0.03
-0.2	2+0.02*f	0.3	150	0.01	1000	0.01	0.34	0.03
-0.4	2+0.02*f	0.3	87	0.01	1000	0.01	0.2	0.03

Table 4.2 i

APPLIED BIAS	EQUIVALENT CIRCUIT ELEMENT VALUES FOR DEVICE 469_1 50 μm Dia.							
(V)	R_{12} (Ω)	L_{23} (nH)	R_{34} (Ω)	L_{40} (nH)	R_{35} (Ω)	C_{50} (pF)	C_{30} (pF)	C_{10} (pF)
0.0	0.1+0.01*f	0.55	70	0.01	300	0.01	4	0.03
0.2	0.1+0.01*f	0.55	24	0.08	1000	0.03	3	0.03
0.3	0.1+0.01*f	0.55	20	0.01	1000	0.03	2.6	0.03
0.4	0.1+0.01*f	0.55	15	0.01	500	0.03	3	0.03
0.5	0.1+0.01*f	0.55	18	0.01	1000	0.03	2.5	0.03
0.6	0.1+0.01*f	0.55	19	0.01	1000	0.03	2	0.03
0.7	0.1+0.01*f	0.55	30	0.01	1000	0.03	2	0.03
0.8	0.1+0.01*f	0.55	22	0.01	1000	0.03	2	0.03
-0.4	0.1+0.01*f	0.55	30	0.01	1000	0.03	1.4	0.03
-0.8	0.1+0.01*f	0.55	20	0.01	1000	0.03	1.2	0.03
-1.0	0.1+0.01*f	0.55	26	0.01	1000	0.03	1.1	0.03
-1.2	0.1+0.01*f	0.55	90	0.01	1000	0.03	1.0	0.03
-1.4	0.1+0.01*f	0.55	43	0.01	1000	0.03	0.9	0.03

Table 4.2 j

Let us now consider the asymmetric barrier-height devices made from NU-453 and NU-454 (Table 4.2(c&d)); the "control" devices are made from NU-455 (Table 4.2(e&f)). These devices (NU-453 & NU-454) did not show the expected enhancement in the inductance associated with the time taken for the charge to tunnel into or out from the well (tens of nanoseconds rather than a few picoseconds, although it must be remembered that such calculations are exponentially dependent on the value of certain components, and therefore prone to large sources of inaccuracy (see equations 1.11-1.15)). In the case of the high barrier example where the escape time of an electron in the well is of the order of nanoseconds, delays associated with this time would very probably show up at the measured frequencies. In order to further investigate the delays arising from these effects, impedance measurements were attempted at 100GHz, as mentioned in Chapter 5.

According to Brown et al [18] the value for the "quantum-inductance" is thought to be proportional to the escape-time divided by the junction conductance. However, this should lead to very high values of inductance at low bias voltages which should also drop rapidly at higher applied voltages. These effects have not been seen in our devices and so cannot be confirmed. The presence of a significant value of quantum-well-inductance ($L_{4,0}$) did seem to be favoured in the models of NU-366, NU-455, and NU-456 (Table 4.2(b,e,f & g)) and this was also bias-dependent to an extent. The presence of the quantum-inductance in NU-366, NU-455 and NU-456 coincides with these being the higher conductance devices, although from the voltage dependence of the values which appear in the models (Table 4.2(b,e,f & g)) this correspondence is not straight forward [14] and must also be strongly influenced by other effects which are not yet understood. The values for this quantum-inductance do seem to peak around resonance which corresponds with the conditions where there are the greatest number of electrons tunnelling into and out from the well. Further measurements at higher frequencies could again shed more light on these and so reveal their origins.

The asymmetric devices of NU-453 and NU-454 also seemed to show an enhanced polarity-dependent charge storage capacitance ($C_{5,0}$) for the condition where the least

transparent barrier is the collector barrier. Under these conditions the collector barrier should enhance the degree of charge build-up in the well and this is indeed seen from Table 4.2(c&d). For layer NU-453 the collector barrier is the least transparent under forward bias and for NU-454 the reverse is true. The reason for the charge storage capacitance being smaller than that of a similarly sized device from NU-455 (where both barriers are similar to the more transparent barriers of NU-453 and NU-454) is that the lack of symmetry (in layer NU-453 and NU-454) reduces the number of allowed states at resonance and hence the resonant current and charge. This reduced transmission probability and therefore the reduced number of allowed states (peak half-width) is demonstrated in Figure 3.3. The reduction in the number of allowed states tends to mask the effect of charge build-up by reducing the absolute quantity of allowed charge in the well. There is undoubtably always a trade-off between the charge build-up due to asymmetry and the reduction in the number of allowed resonant states and therefore the amount of charge in the well at any one time due to the degree of asymmetry. Thus it is probably not possible to control either of these capacitances separately.

The importance of the charge build-up can perhaps be most clearly seen by its strong influence on the current-voltage characteristic and, although these effects were studied by Booker [20], he showed that from the theoretical model the effect on the d.c. characteristic was difficult to quantify accurately. The relatively large degree of charge build-up resulting from the reduced transparency of the collector barrier can be seen in Figures 2.4 & 2.5 for NU-453 & NU-454 where the rate at which the current increases with increasing applied bias is high. This is due to the presence of increased charge in the well which as a result dramatically increases the field across the collector barrier, and so rapidly reduces its height and increases the overall transmission. In the case where the lower barrier is the collector barrier the charge storage, and hence the resulting field across this barrier is not enhanced and so the overall transmission current is reduced.

Figures 4.23-4.27 show (for some of the more interesting voltages at which the

measurements were made) the match which was achieved between the behaviour of the models and the measured impedance for devices from wafers: NU-195, NU-366, NU-453, NU-455 and NU-469. Slight deviations from a good fit between the modelled performance and the measurements can be seen in some of the figures, and a discussion of the reasons for this follows.

The performance of the model for 195/1 versus its measured impedance (Figures 4.23(a-d&f) {at 0.7v}) is very good, except when the device is biased into the resonant region of the current-voltage characteristic (Figure 4.23(e&f) {at 0.6v}). In this region of the characteristic the negative differential resistance (NDR) can (if the real component of the embedding impedance is much lower than the magnitude of the NDR) allow oscillations to occur in the device, and so lead to confusion in the measurements. If the device were biased in the NDR region of the characteristic but remained stable, then there is a good probability that the reflected "probe" signal, (with which the impedance is measured) could suffer parametric amplification. Under such circumstances, the measured impedance would appear outside the unity-gain circle of the smith-chart. This effect is shown by the model but not by the measured device since the device is difficult to bias in a stable fashion in the NDR region. Measurements were made on another occasion [10], which did indeed show the effect of parametric amplification.

Figures 4.23-4.27 demonstrate the match between the measured and the modelled S-parameters and the element values which were used to achieve this matching are listed in Table 4.2.

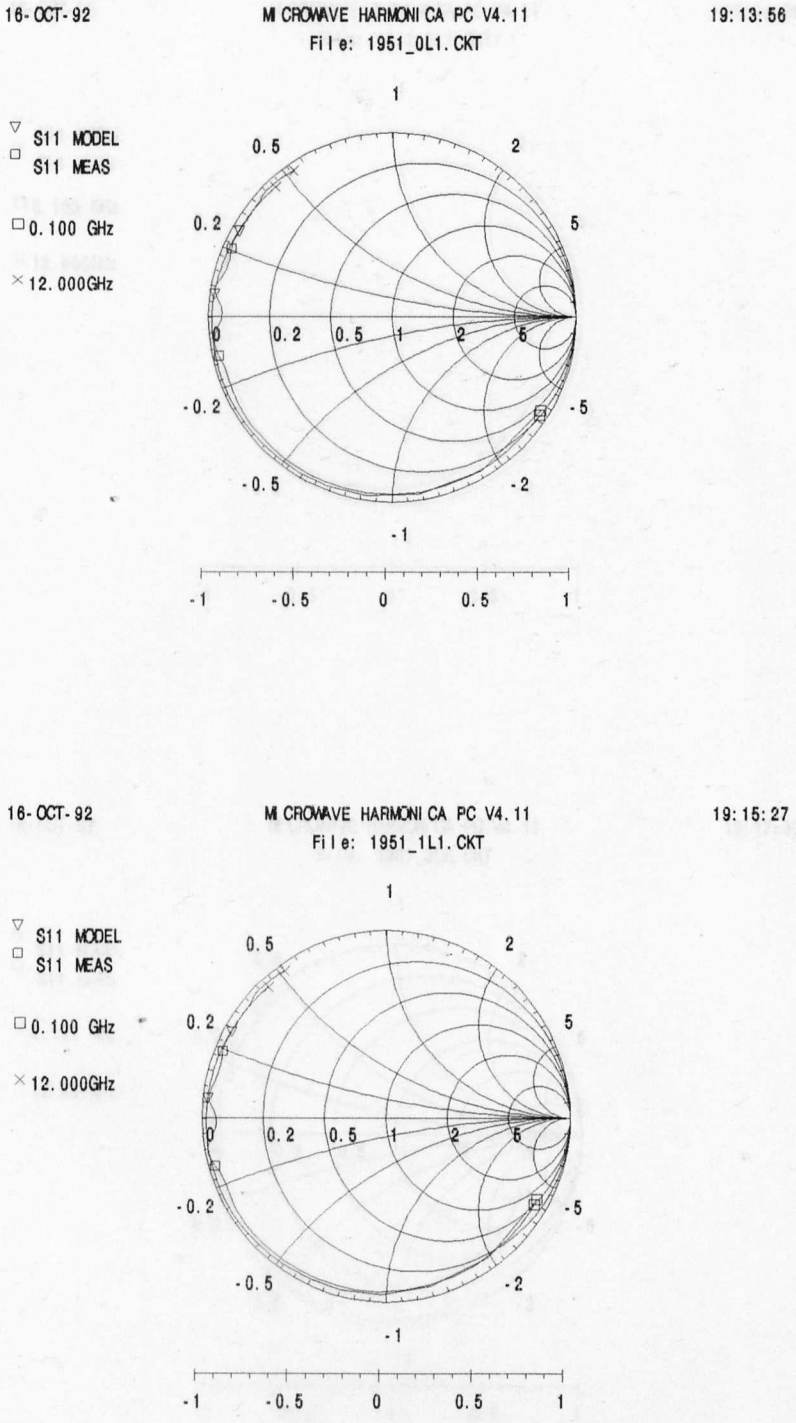
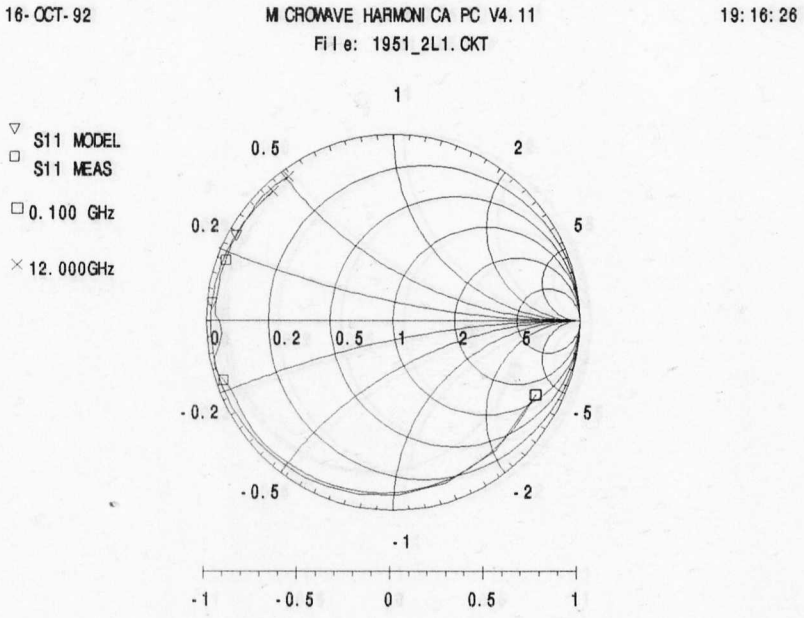


Figure 4.23 a Device 195/1 at 0.0 and 0.1 volts



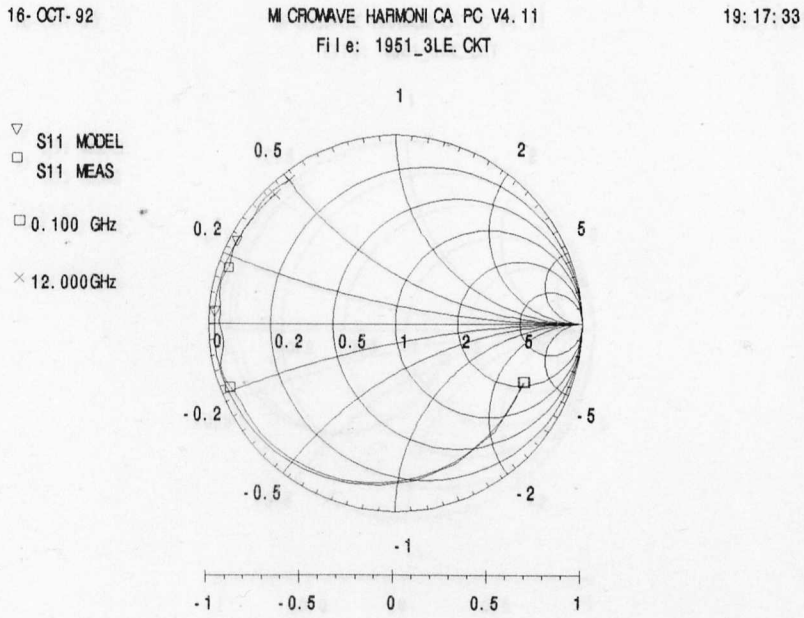
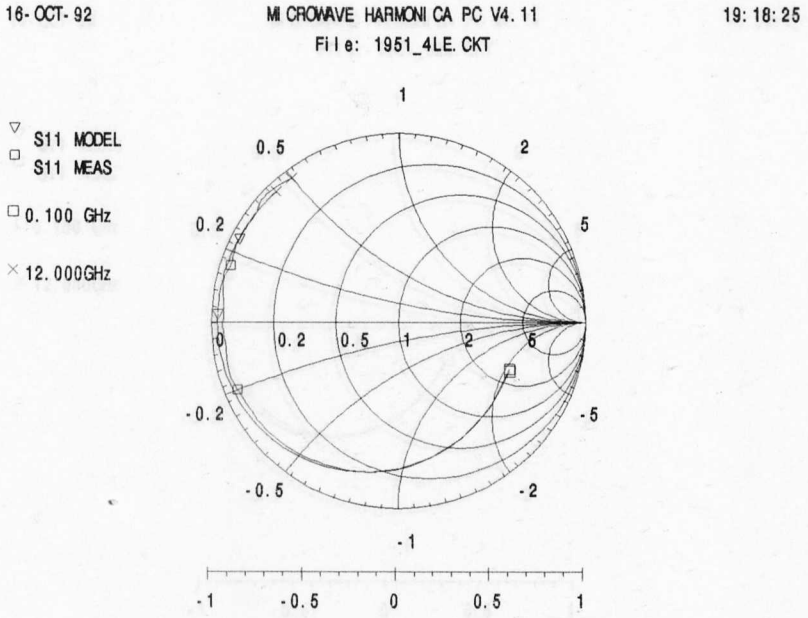


Figure 4.23 b Device 195/1 at 0.2 and 0.3 volts



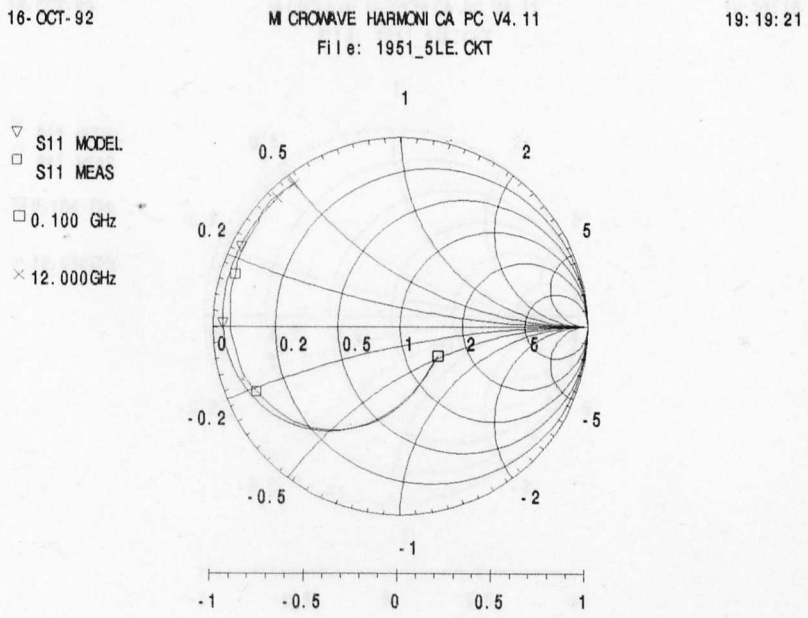
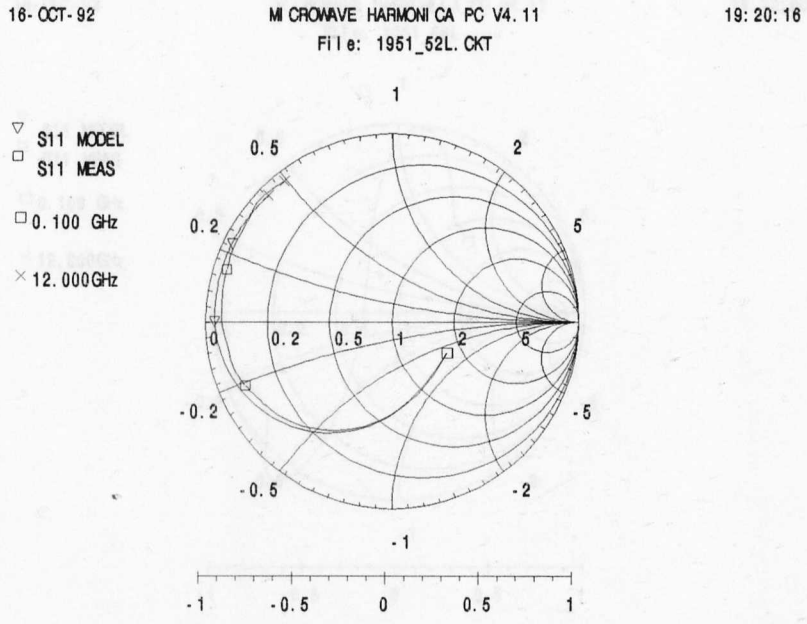


Figure 4.23 c Device 195/1 at 0.4 and 0.5 volts



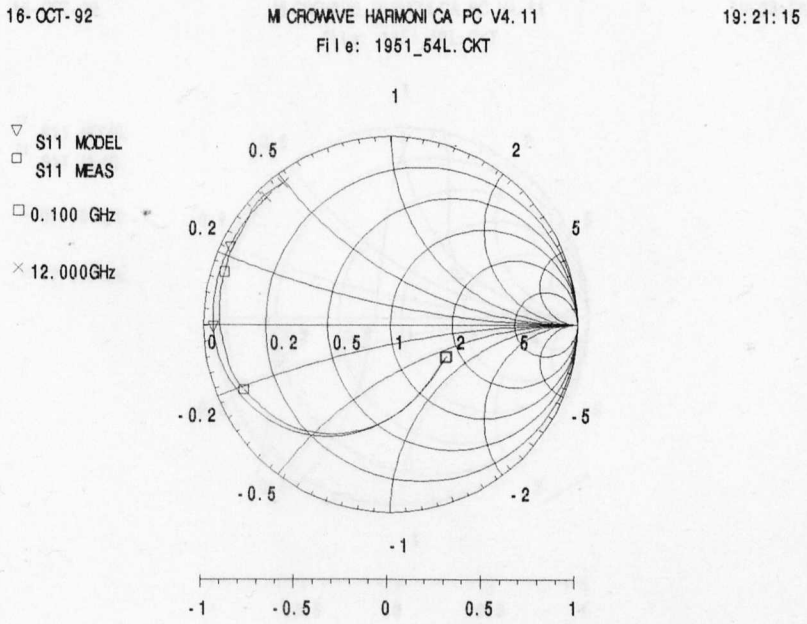
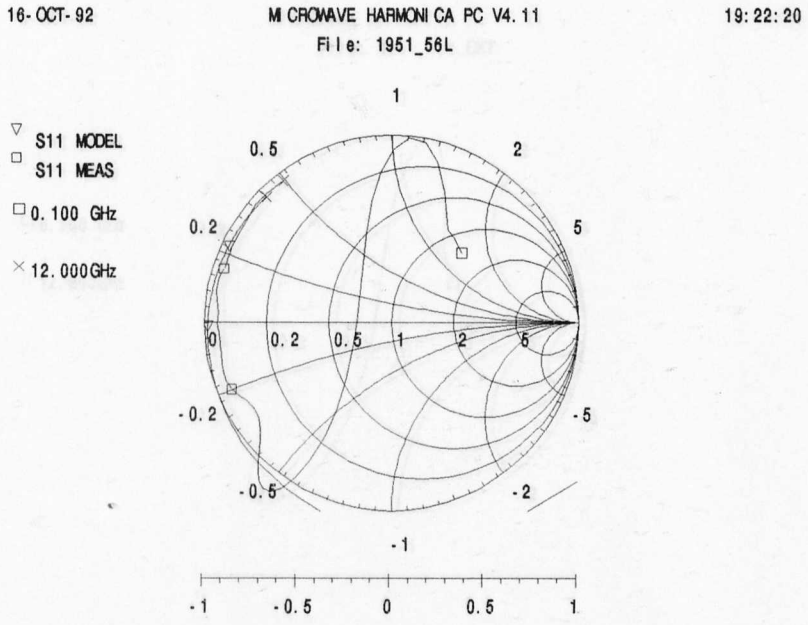


Figure 4.23 d Device 195/1 at 0.52 and 0.54 volts



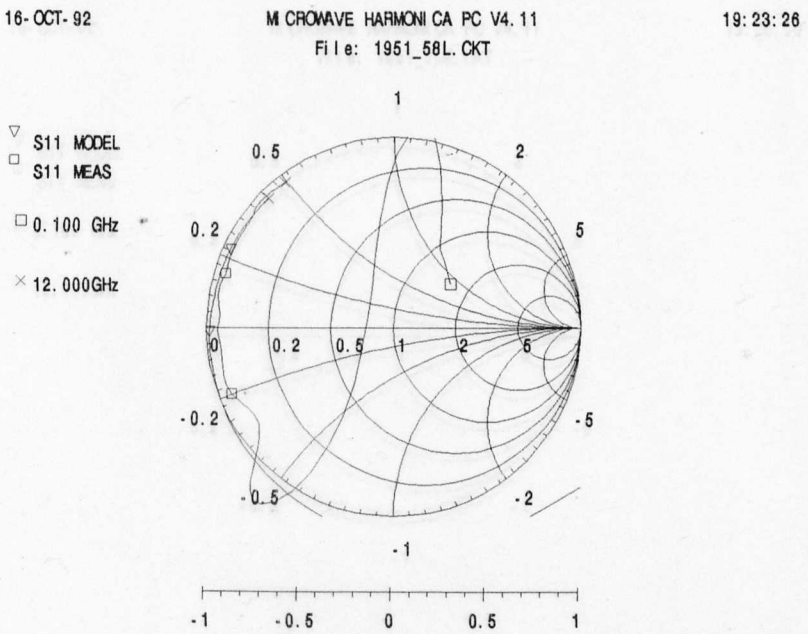
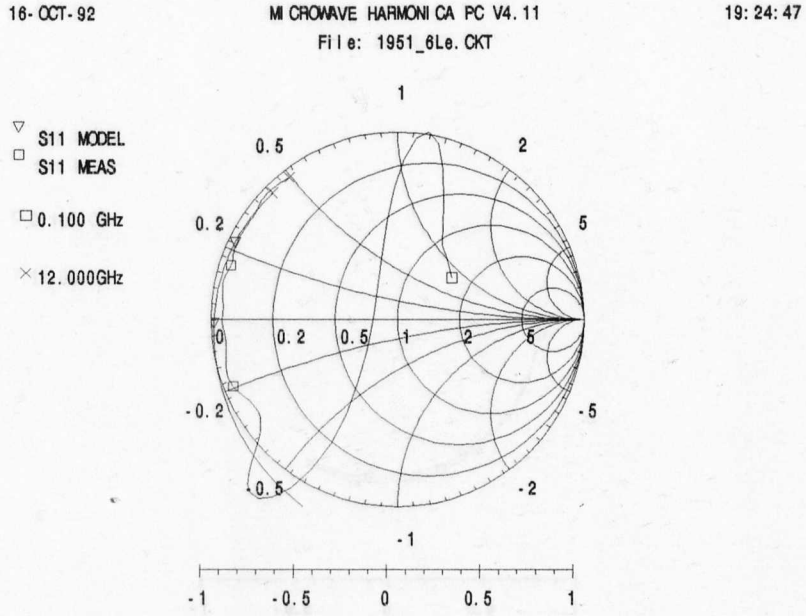


Figure 4.23 e Device 195/1 at 0.56 and 0.58 volts



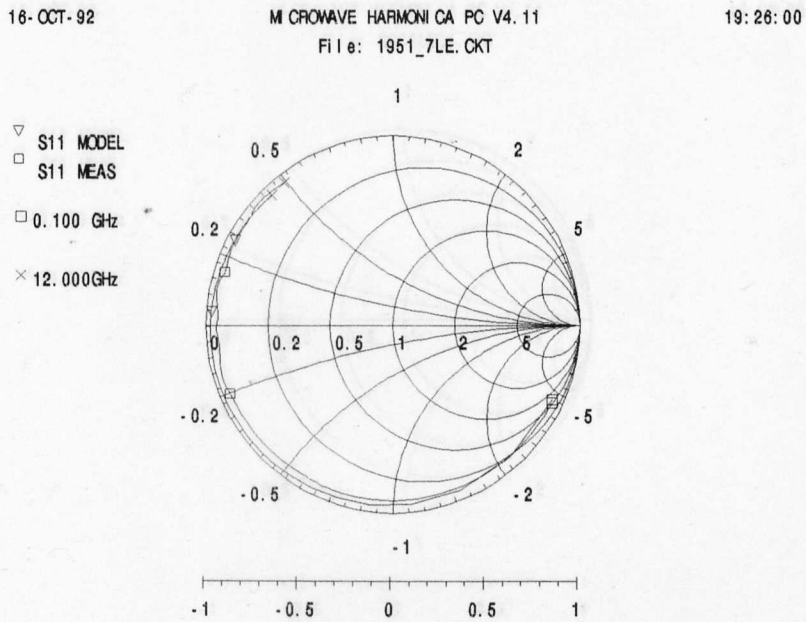
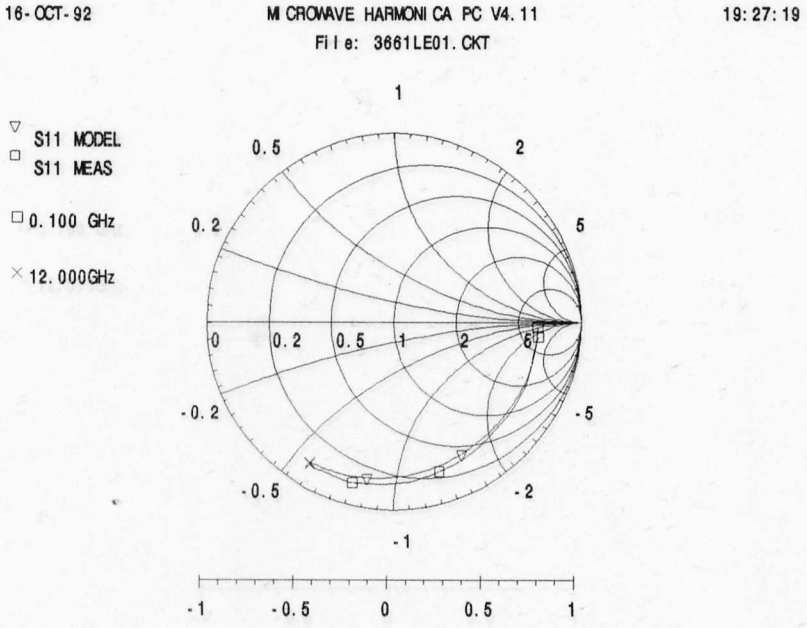


Figure 4.23 f Device 195/1 at 0.6 and 0.7 volts



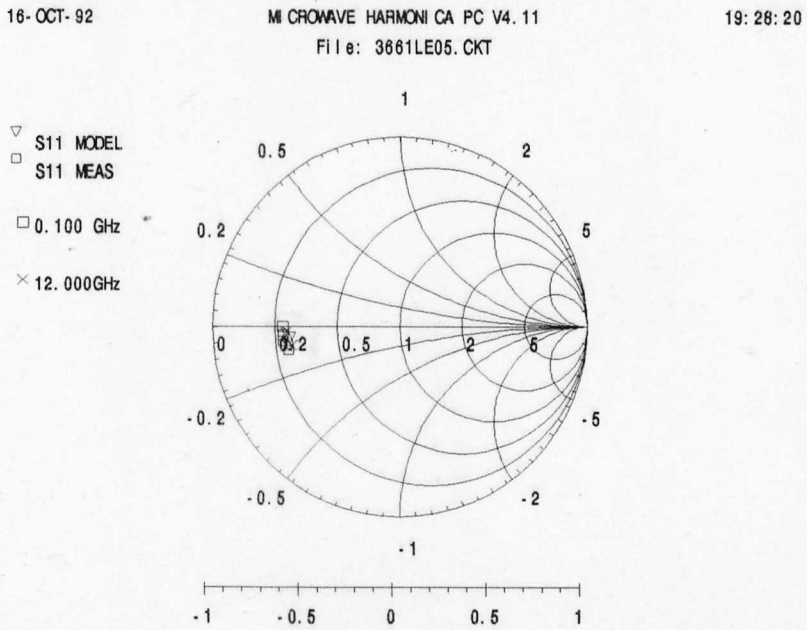
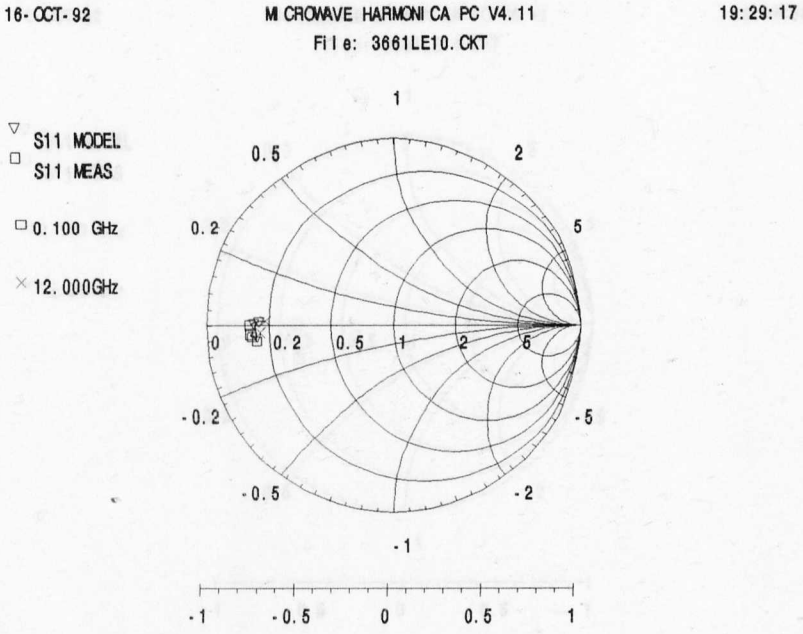


Figure 4.24 a Device 366/1 at 0.0 and 0.5 volts



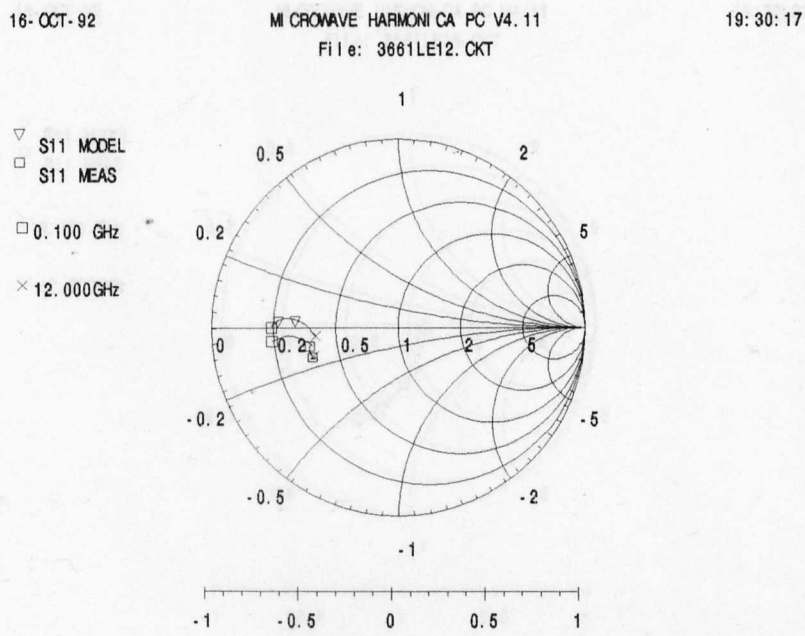
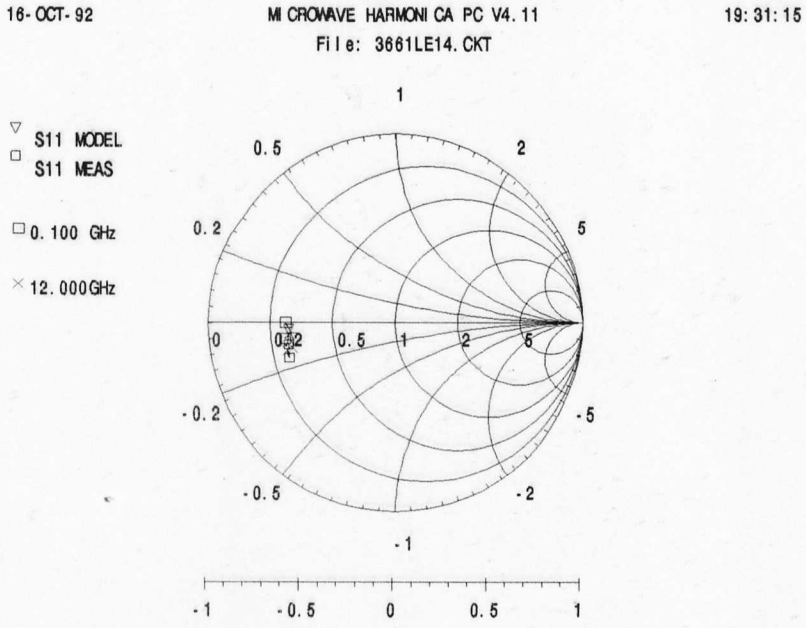


Figure 4.24 b Device 366/1 at 1.0 and 1.2 volts



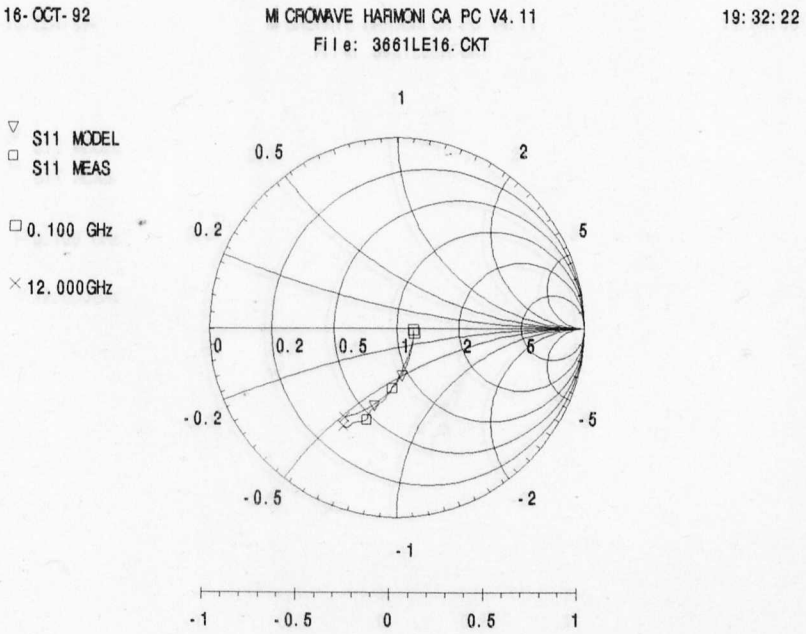
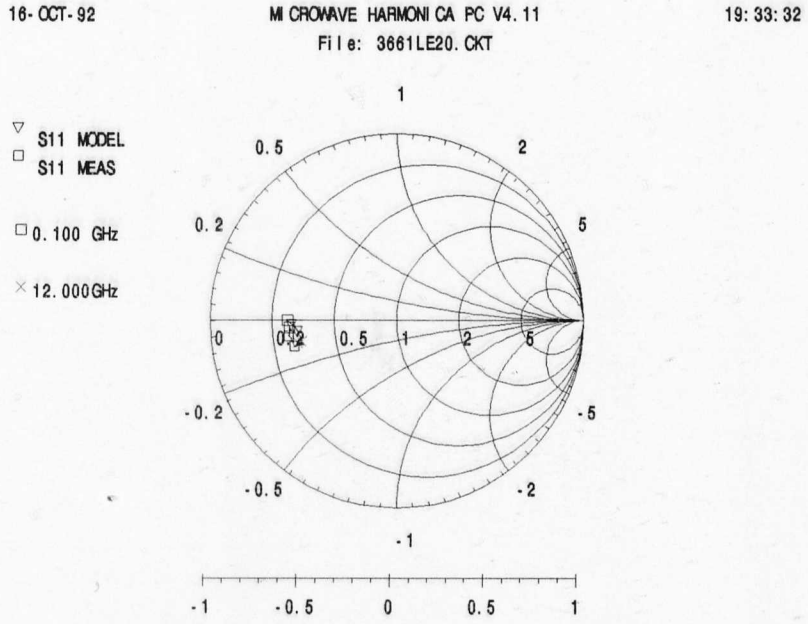


Figure 4.24 c Device 366/1 at 1.4 and 1.6 volts



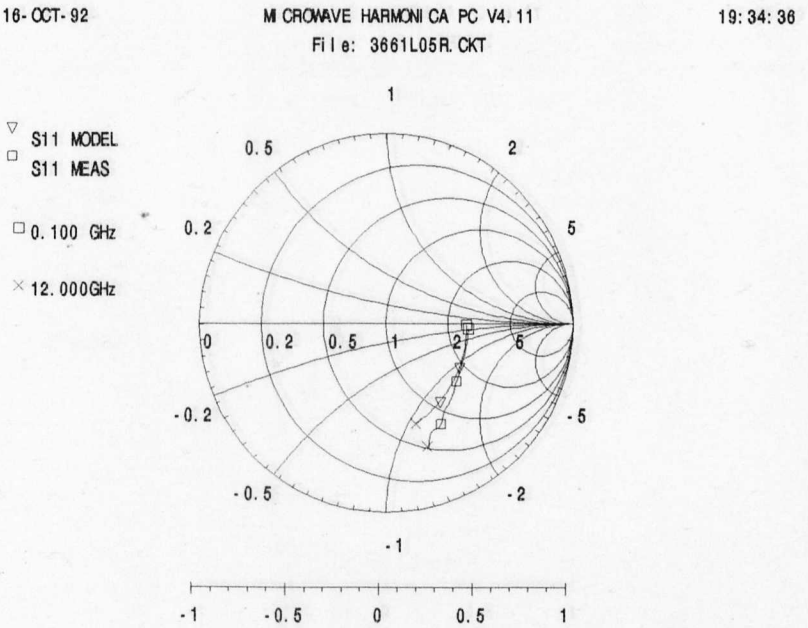
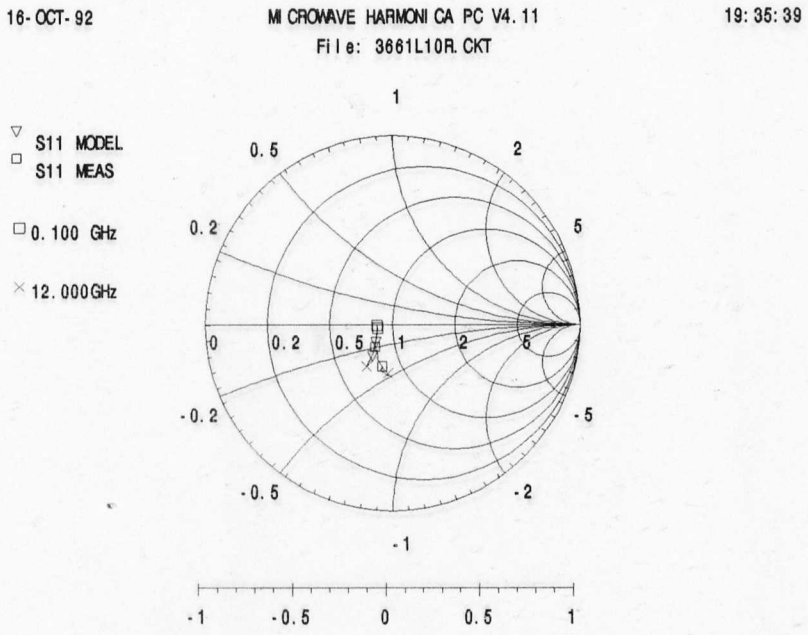


Figure 4.24 d Device 366/1 at 2.0 and -0.5 volts



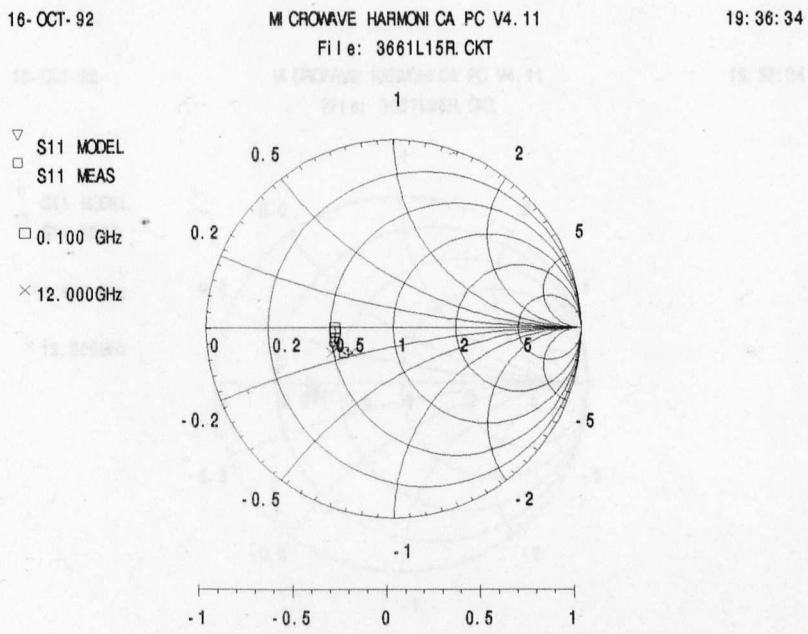
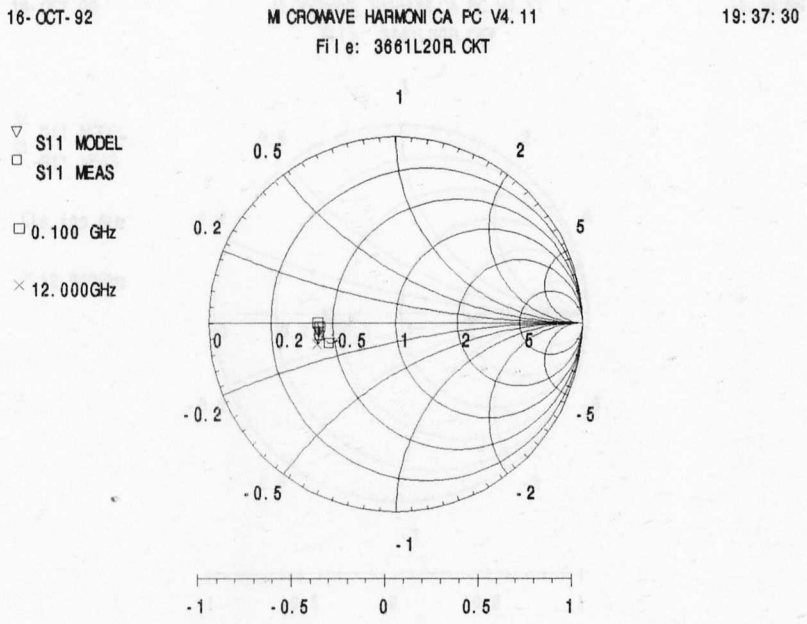


Figure 4.24 e Device 366/1 at -1.0 and -1.5 volts



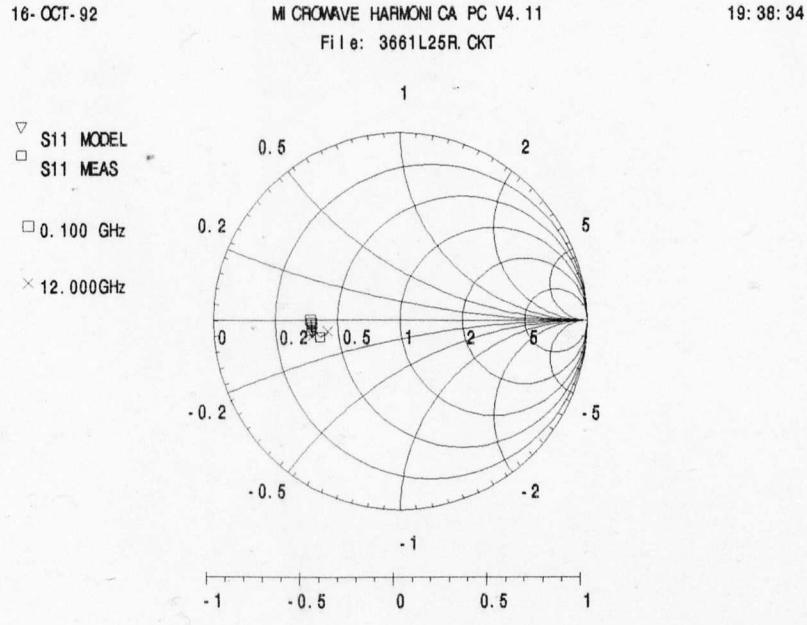


Figure 4.24 f Device 366/1 at -2.0 and -2.5 volts

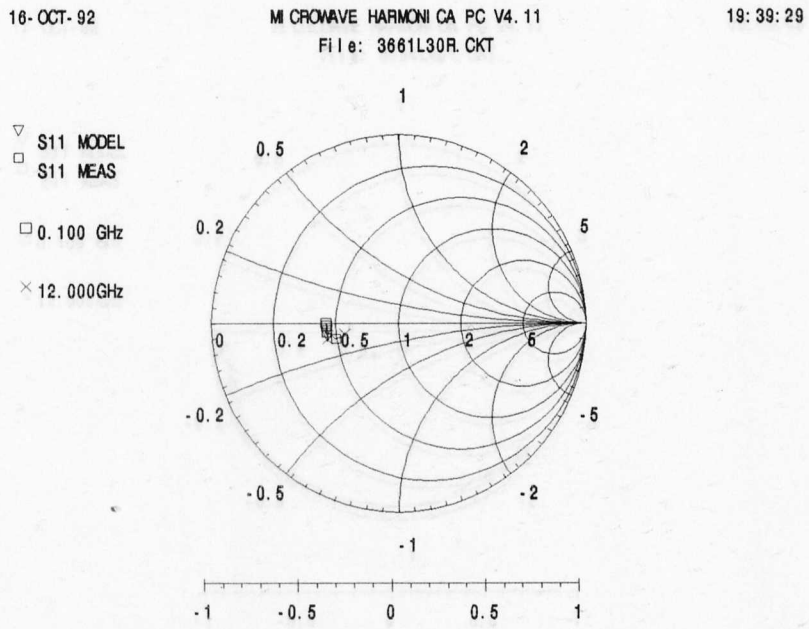
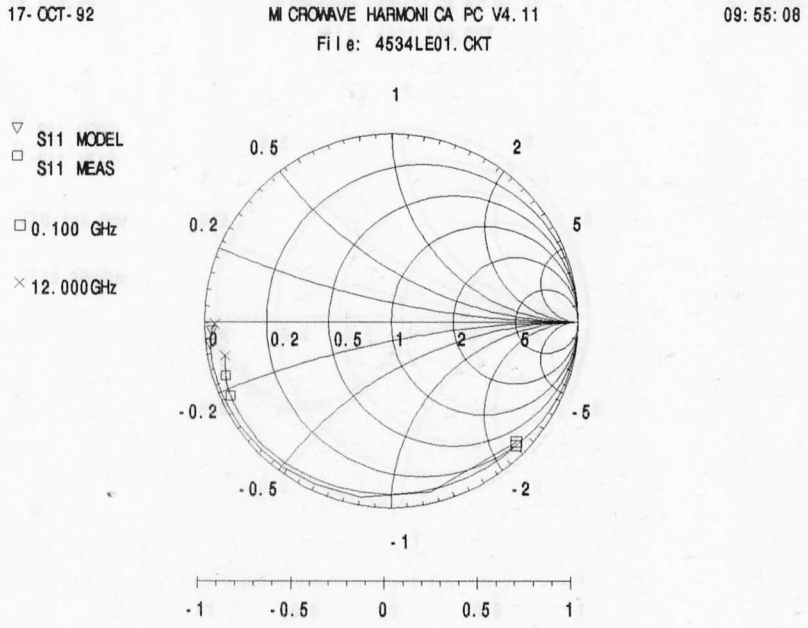


Figure 4.24 g Device 366/1 at -3.0 volts



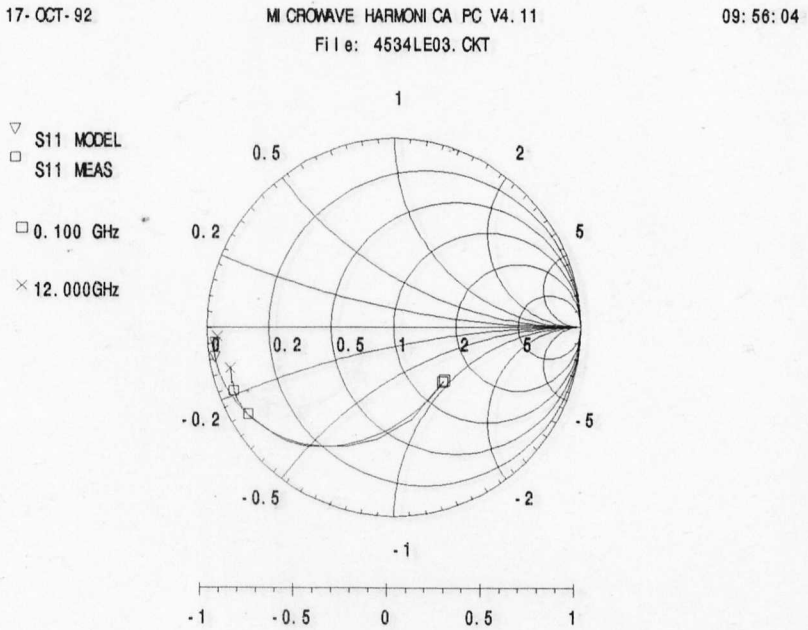
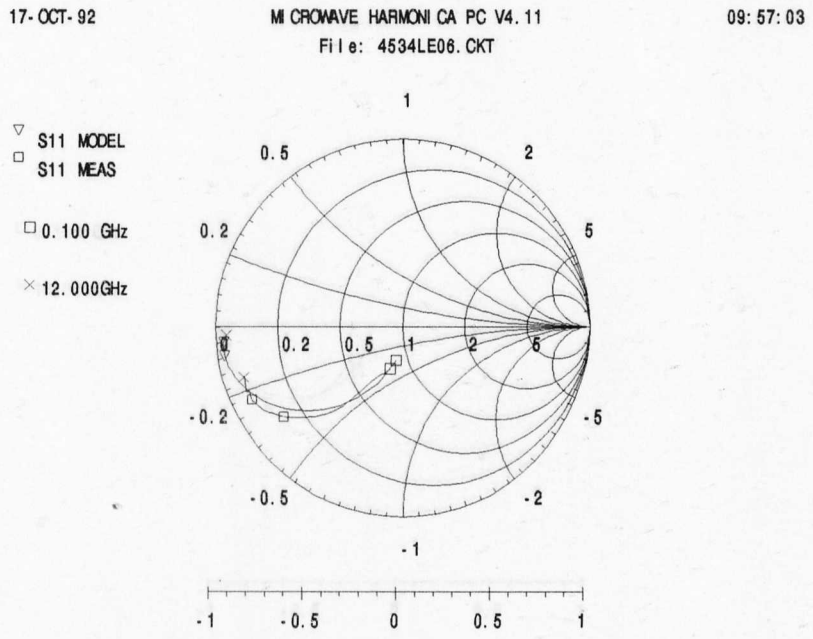


Figure 4.25 a Device 453/4 at 0.0 and 0.3 volts



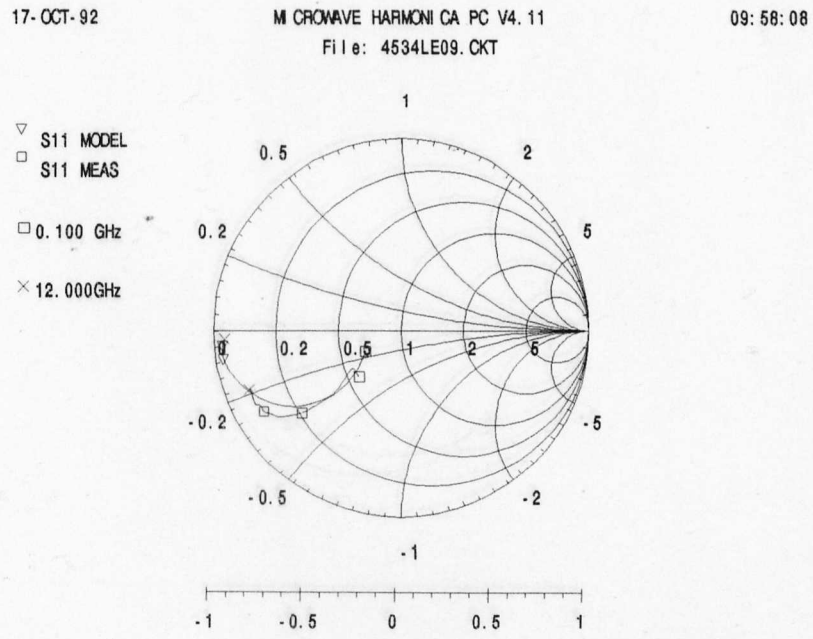
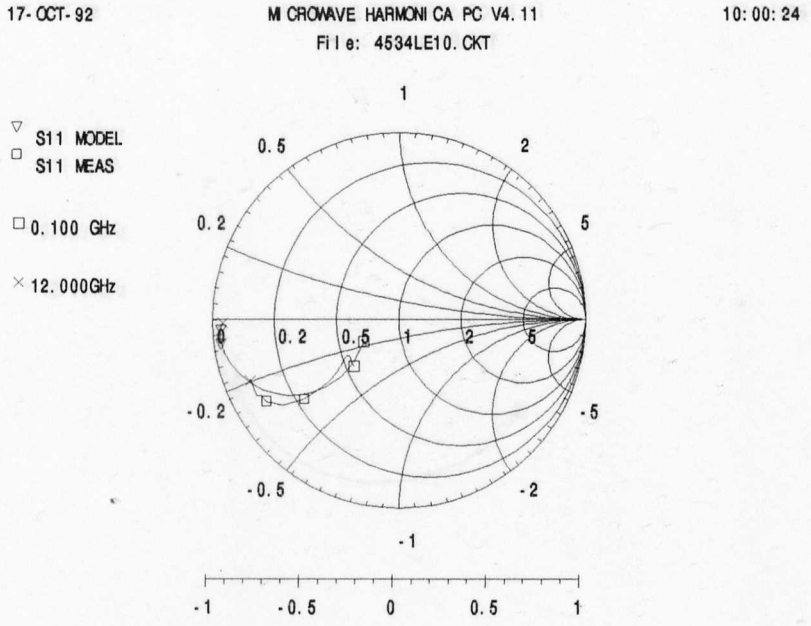


Figure 4.25 b Device 453/4 at 0.6 and 0.9 volts



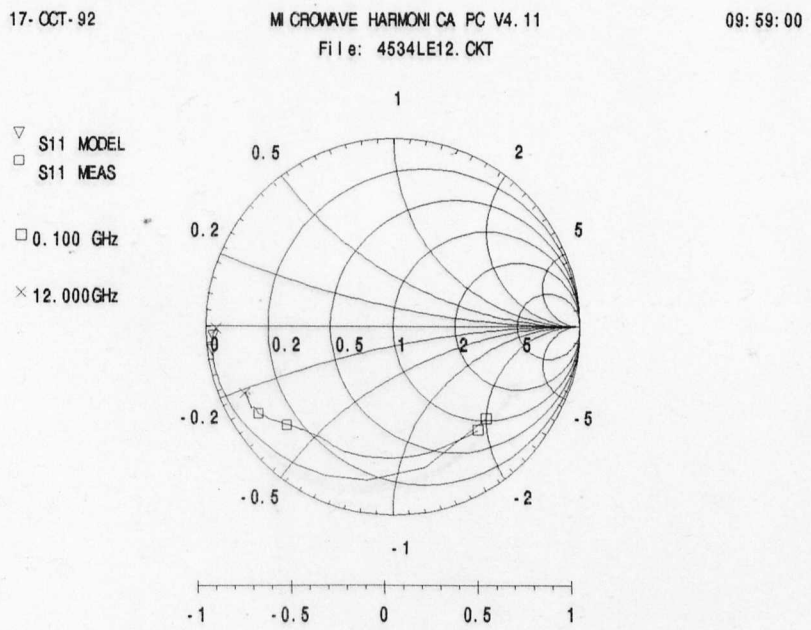
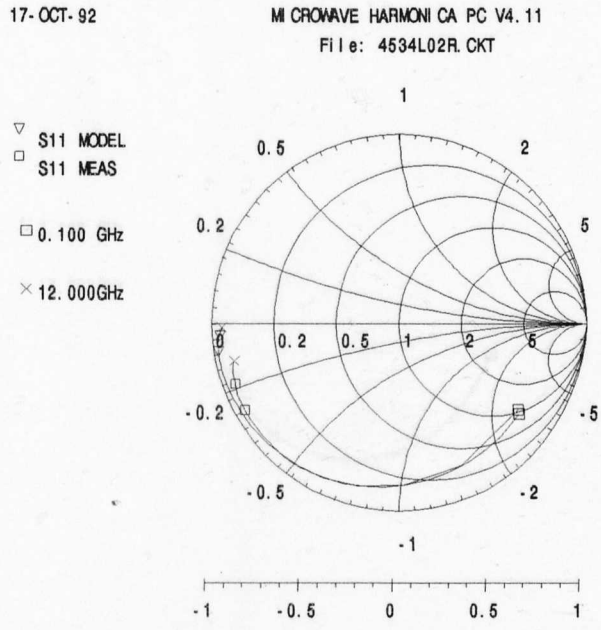


Figure 4.25 c Device 453/4 at 1.0 and 1.2 volts



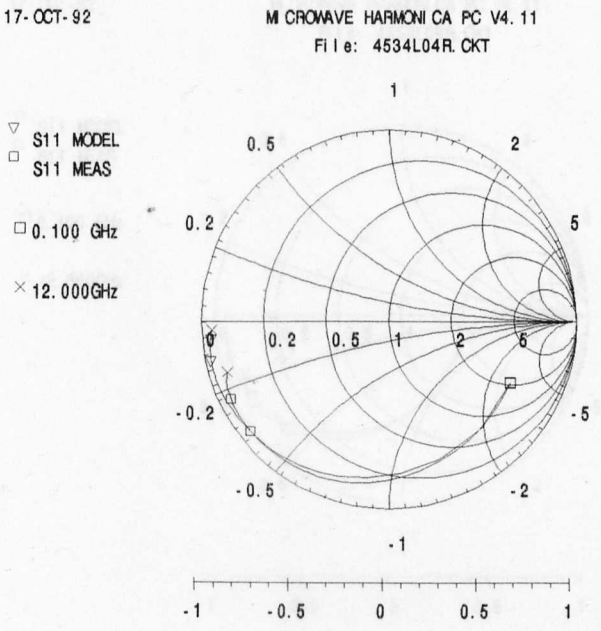
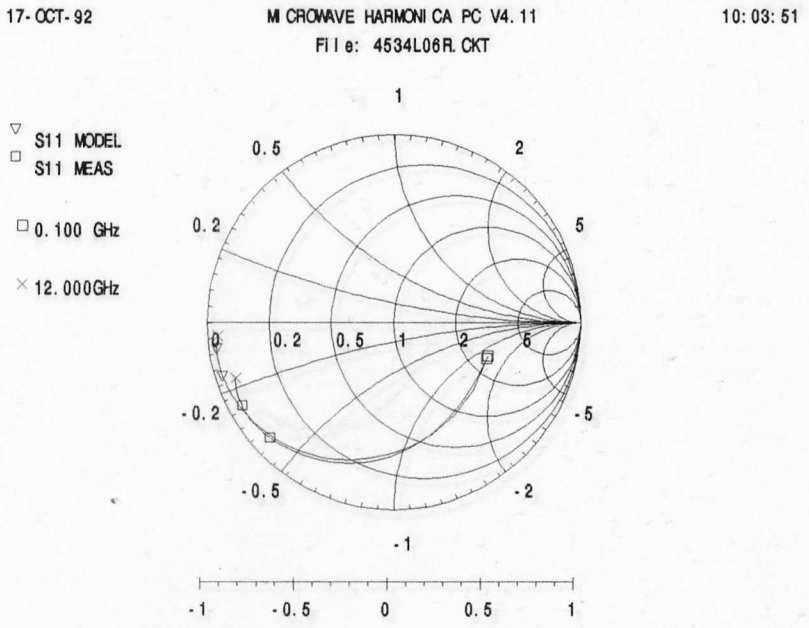


Figure 4.25 d Device 453/4 at -0.2 and -0.4 volts



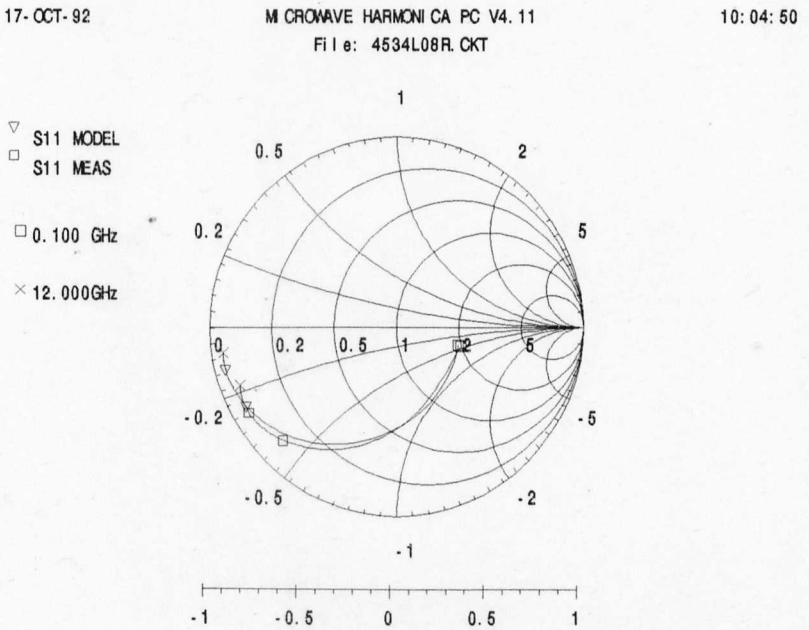


Figure 4.25 e Device 453/4 at -0.6 and -0.8 volts

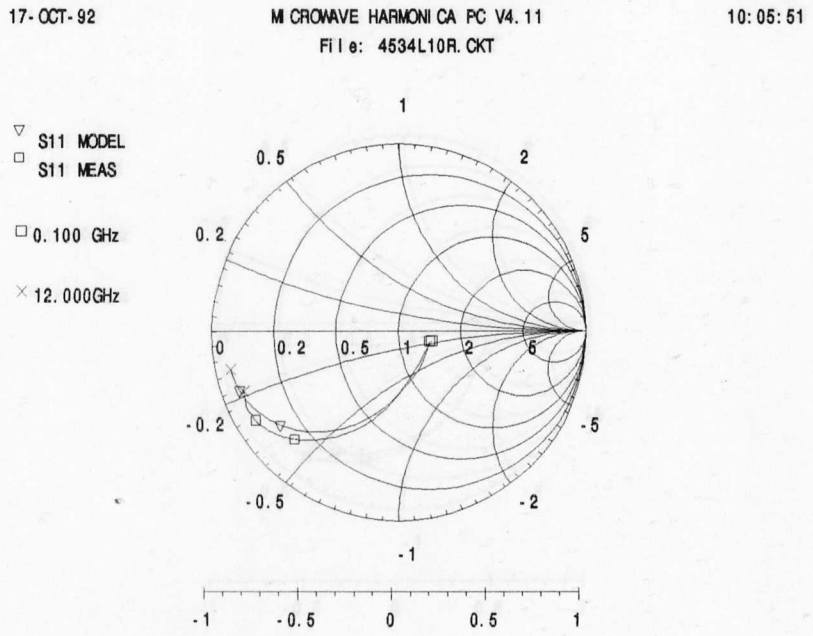
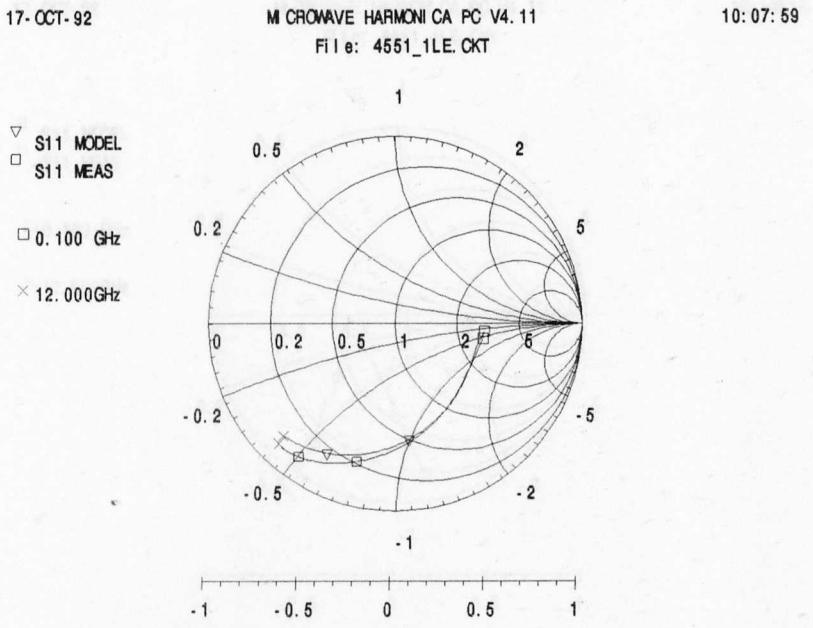


Figure 4.25 f Device 453/4 at -1.0 volts



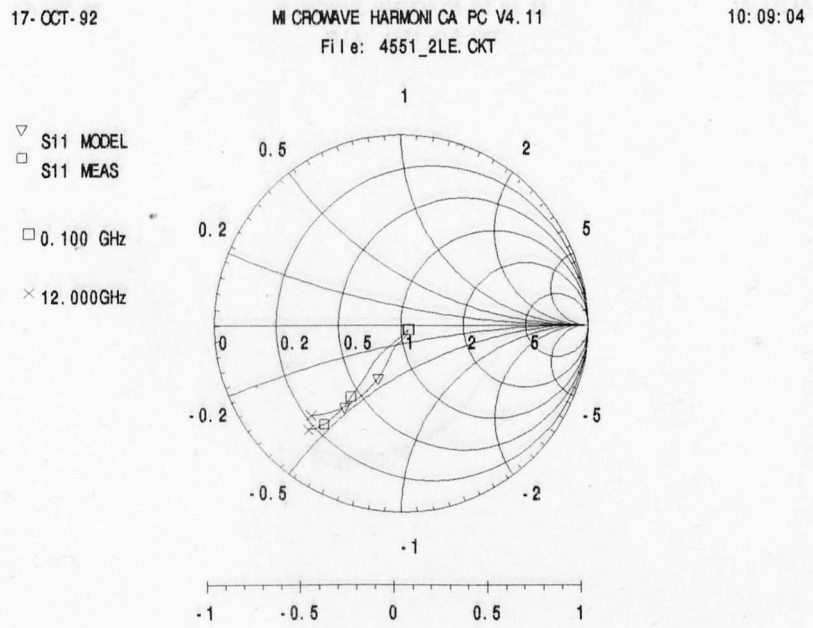
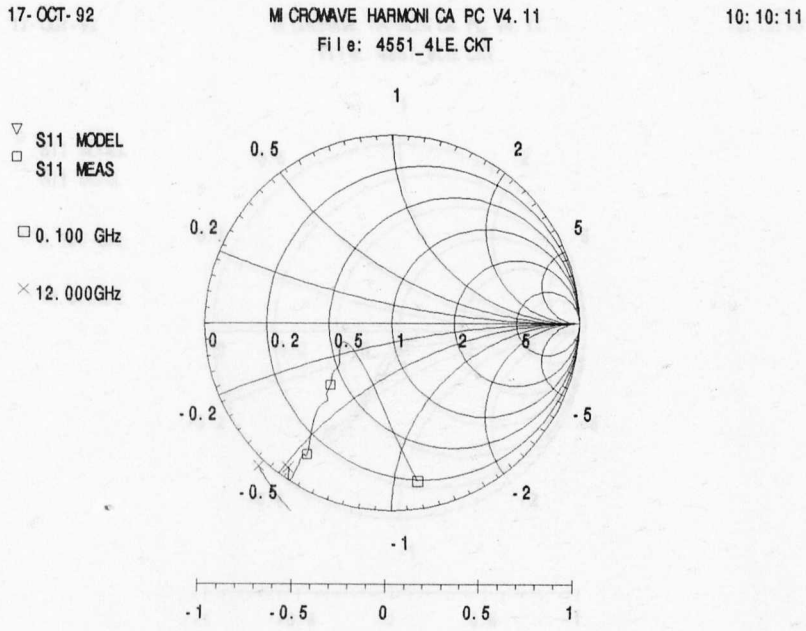


Figure 4.26 a Device 455/1 at 0.0 and 0.2 volts



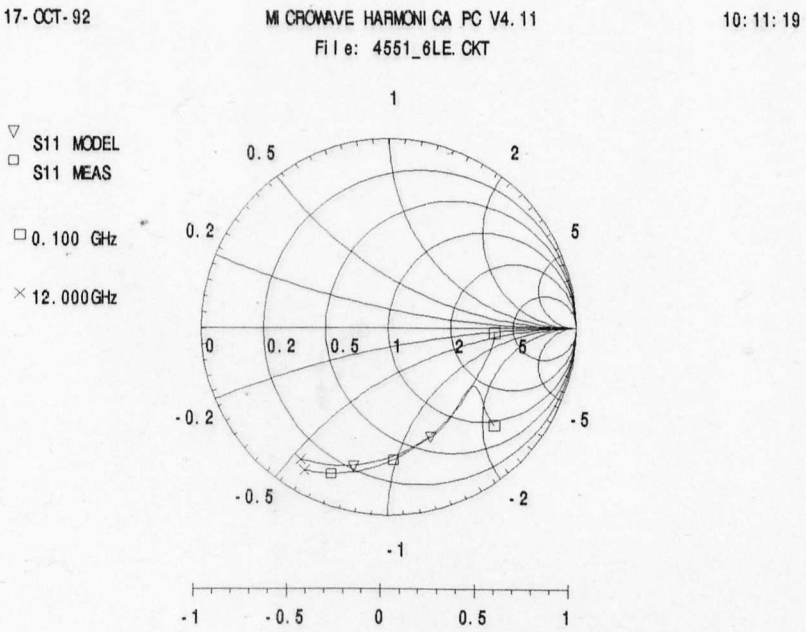
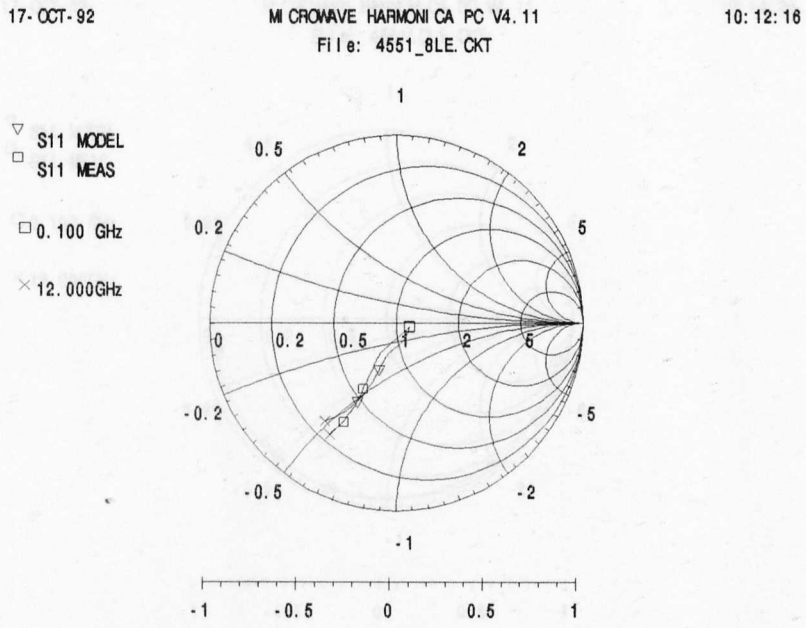


Figure 4.26 b Device 455/1 at 0.4 and 0.6 volts



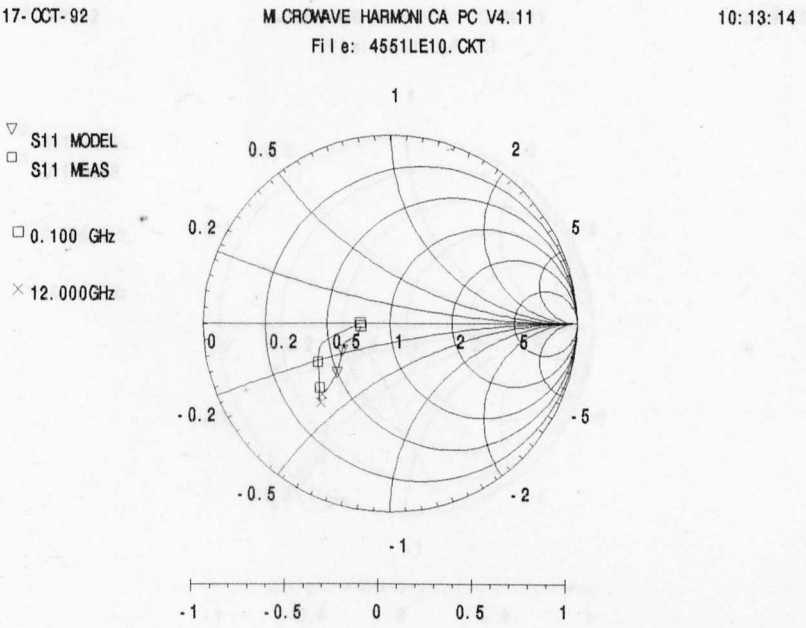
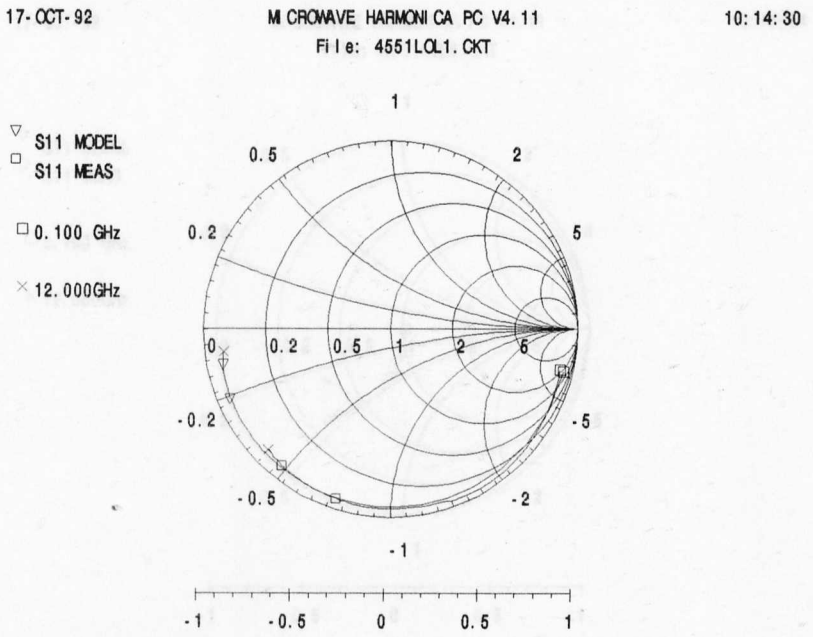


Figure 4.26 c Device 455/1 at 0.8 and 1.0 volts



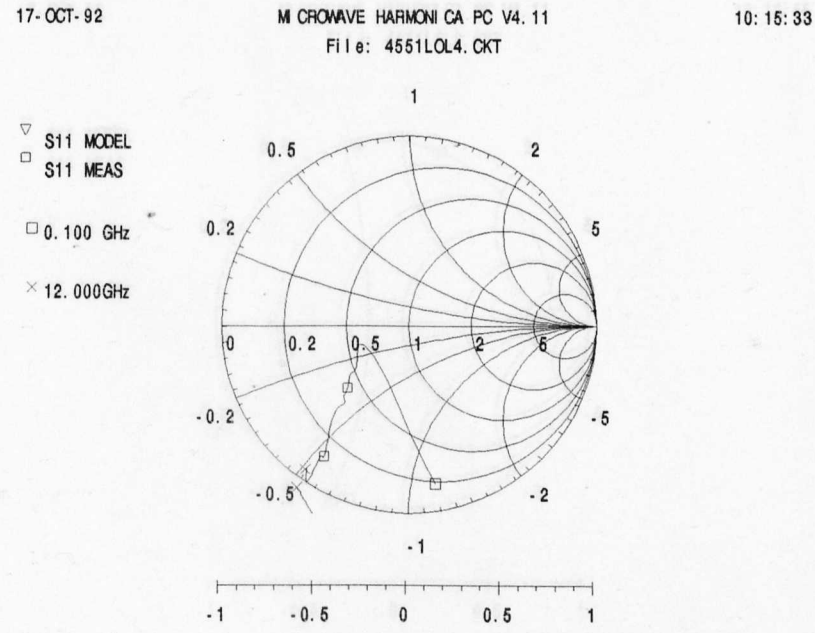
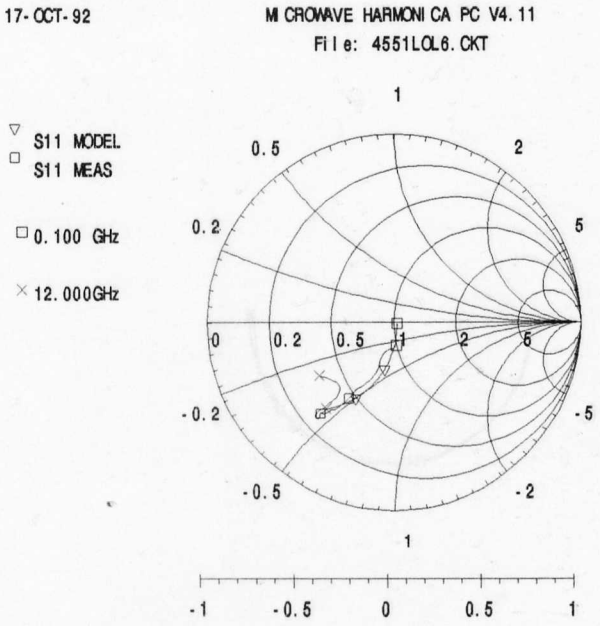


Figure 4.26 d Device 455/1 at 77K and at 0.0 and 0.4 volts



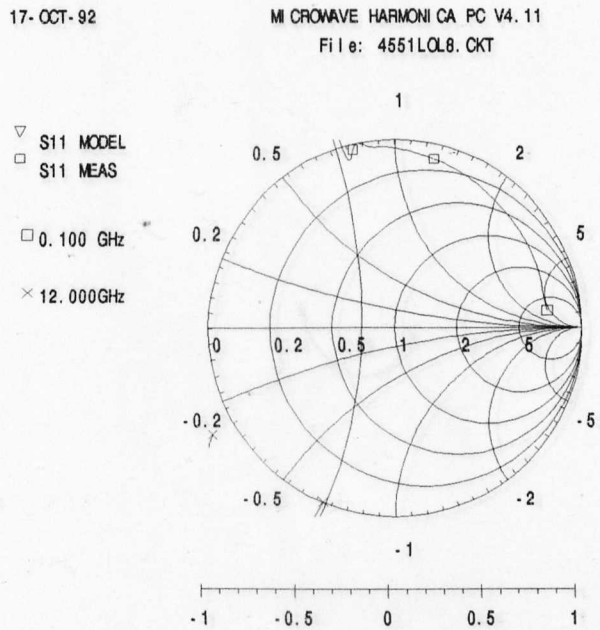
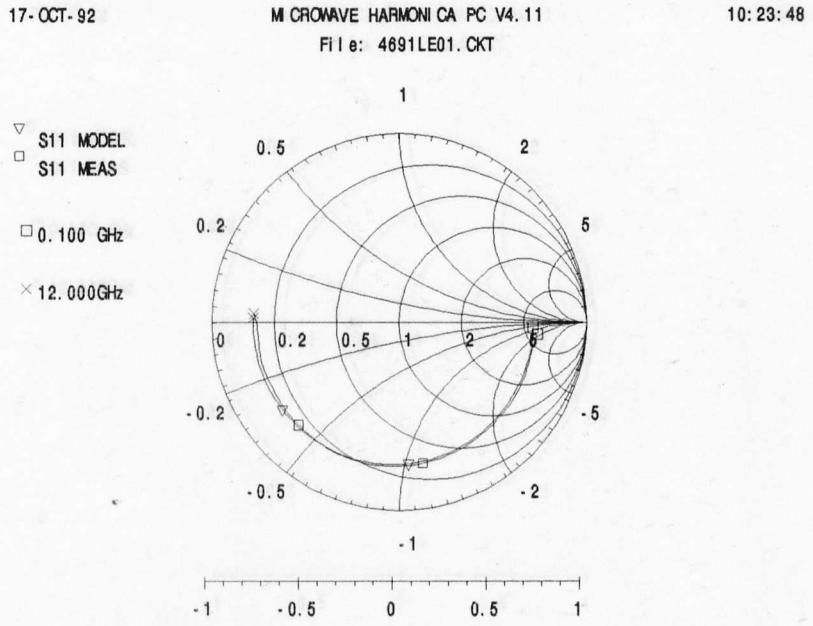


Figure 4.26 e Device 455/1 at 77K and at 0.6 and 0.8 volts



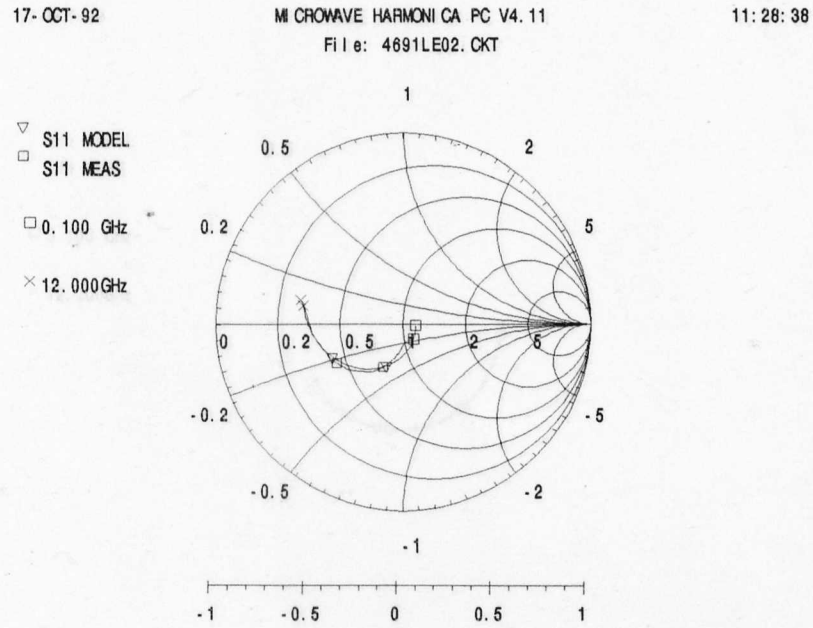
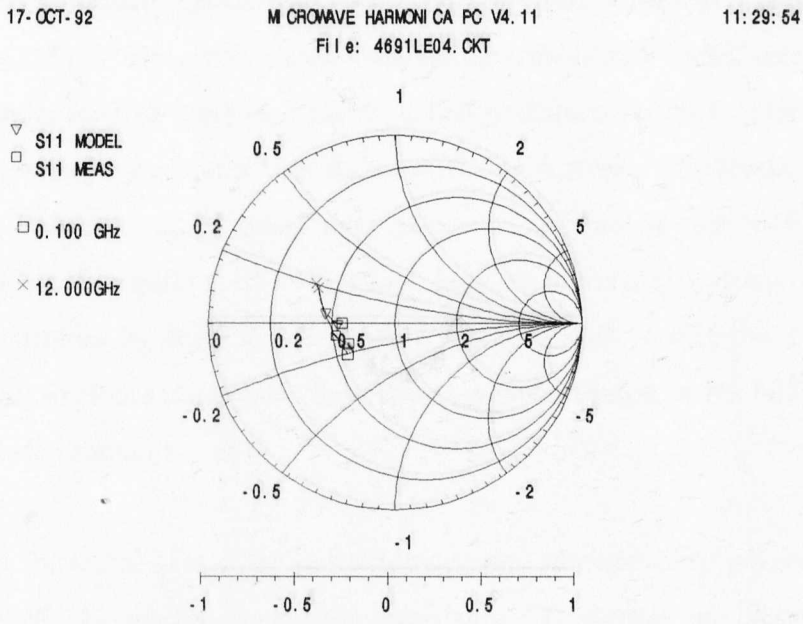


Figure 4.27 a Device 469/1s at 0.0 and 0.2 volts



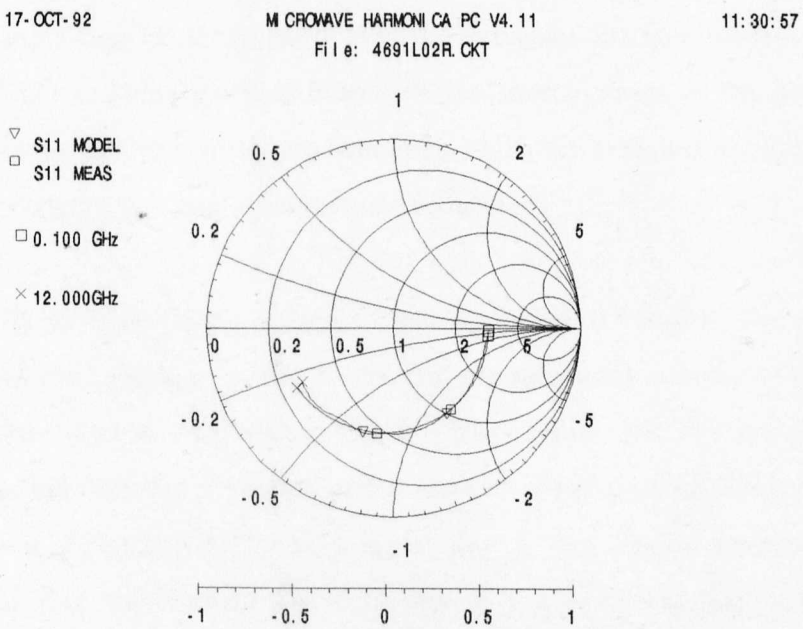


Figure 4.27 b Device 469/1s at 0.4 and -0.2 volts

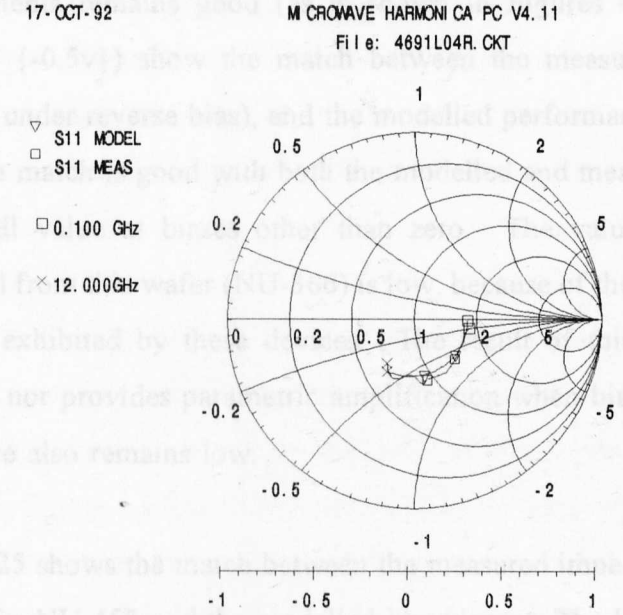


Figure 4.27 c Device 469/1s at -0.4 volts

For device 366/1, shown in Figure 4.24, the measured impedance at biases other than zero is generally very low, but the match between the modelled performance and the measurements remains good (as is shown in Figures 4.24(a-d) {2.0v}). Figures 4.24(d-g) {-0.5v}) show the match between the measured impedance, (where the device is under reverse bias), and the modelled performance, also under reverse bias. Again the match is good with both the modelled and measured impedances dropping to a small value at biases other than zero. The value of the NDR for devices fabricated from this wafer (NU-366) is low, because of the high current densities (thin barriers) exhibited by these devices. The result of this is that the device neither oscillates nor provides parametric amplification when biased in the NDR region; the impedance also remains low.

Figure 4.25 shows the match between the measured impedance of a device fabricated from wafer NU-453 and the modelled impedance. The lower conductance, resulting from the asymmetric barriers, can be seen from the relatively high impedance shown by device 453/1, and this impedance remains fairly high even at high bias as for example, in Figure 4.25(c). The match between the modelled impedance and the measured impedance is not as good as in the examples for other devices (4.23, 4.24, 4.26 and 4.27) and this perhaps illustrates the shortcomings of the present models when describing devices with layer structures which differ significantly from the ideal case for resonant tunnelling (symmetric barriers).

Device 455/1 oscillates at 0.4 volts, as is shown in figure 4.26(b). The reason for the difference in the behaviour of the model and the measured impedance is the same as was described earlier for device 195/1. The reason for the departure, at low frequencies, between the modelled and measured impedance for device 455/1 at 0.6 volts (Figure 4.26(b) {0.6v}), was again due to the device becoming unstable. However, at this bias voltage the instability only occurred at the lower frequency, where the magnitude of the NDR was greater than that of the embedding network thereby allowing oscillation to take place only at this point. The behaviour of 455/1 was also studied at low temperature (Figure 4.26(d&e)), and the device can be seen

to be unstable at voltages between 0.4 to 0.8 volts. The wider voltage range over which the device is unstable is simply a reflection of the increased peak-to-valley current and voltage swing, as can be seen in a typical d.c. current-voltage characteristic measured at 77K shown in Figure 2.6. The poor match between the modelled performance and the measured impedance is simply a result of this oscillation; where the device is stable (at 0.0 volts, shown in Figure 4.26(d)) the match is again reasonable.

Figure 4.27 (device 469/1s) demonstrates the good match between the measured and modelled impedance for both positive and negative applied bias. The effect of the low-doped region on the substrate side of the double barriers can be seen by comparing Figure 4.27(a) {0.2v} with 4.27(b) {-0.2v}; when the electrons are injected into this low-doped region (reverse bias), the impedance is greater than when the upper barrier is the collector. This is again a reflection of the shape of the current-voltage characteristic, as can be seen in Figure 2.9.

In conclusion, section 4.4, together with Figures 4.23-4.27, demonstrates the usefulness of equivalent circuit models for investigating the significance of the factors which contribute to the high frequency performance. Such equivalent circuit models are therefore an important first step in developing an understanding of the relationship between the layer structure and the device behaviour, and are necessary for optimising device designs in order to achieve further improvements in the performance of systems using this type of structure.

4.5 Evaluation of the more physical model

The following discussion concerns the more physical model developed *ab initio* in chapter 3.4 and also studied in chapter 4.3.5, and how the performance of this model compares to the measured impedance of a 20μm diameter device from wafer number NU-455. The values which appear in Table 4.3 were calculated from a knowledge of

the approximate voltage distribution throughout the device structure, using the computer program mentioned in Chapter 3, and also using the equations 1.11-1.15. The analysis is given for a 20μm diameter device with a similar layer structure to NU-455. The results of these latter equations are again only approximate, since their value depends on the accuracy of factors such as the transmission coefficient, the barrier heights and the position of the confined state in the well. All of the factors, in turn, depend strongly on the accuracy of the theoretical model. From a comparison of the current-voltage characteristics shown in Figure 3.6 and 3.7 it can be seen that the accuracy of the theoretical model is not yet ideal.

Referring to Table 4.3 and Figures 4.28-4.31 it may be seen that in order to achieve the best correspondence for the various voltages used, the theoretical current-voltage characteristic needs to be scaled in order to make the voltage at which the current peaks coincident with the measured peak. The theoretical model was then able to calculate the appropriate voltage distribution throughout the device, and therefore, the corresponding reduction in the height of the barriers and the length of the depletion region resulting from the applied voltage.

The correspondence between the applied voltage and the most appropriate voltage for the theoretical characteristic is shown in columns one and two of Table 4.3 and was calculated from the current-voltage characteristics of Figure 3.6 and 3.7 (ie. $V_{Th}*1.8=V_{App}$ for 300K, and $V_{Th}*1.6=V_{App}$ for 77K).

The capacitance of the emitter region was calculated to be 2pF for a 20μm diameter device ($L_{Acc}+L_{bE}+1/2L_w$, (100+42+25Å)). The capacitance of the collector region ($1/2L_w+L_{bC}+L_S+L_{dep}$, (25+42+50+$L_{dep}$Å)), which includes the depletion region, is detailed in column four of Table 4.3.

Columns seven and ten give the escape time of the electrons in the well through the emitter and collector barriers respectively. These calculations are based on the height and transmission of these barriers (given in columns 5,6, & 8,9 of Table 4.3 via.

equation 1.11) and are only approximate for the reasons stated in the introduction to this section. Also, with regard to the calculation (via equation 1.15) of the escape times shown in Table 4.3, the effect of the occupancy of the regions into which the tunnelling occurs is neglected and, which if high, will inhibit tunnelling and so greatly increase the escape time. This would be expected to affect the emitter barrier in particular, and introduces another source of error into these theoretical models.

Columns eleven and twelve show (respectively) the value of the differential resistance calculated from the theoretical characteristic and the value of resistance required to give a reasonable fit to the measured impedance. From the current-voltage characteristics shown in Figure 3.6 and 3.7 it can be seen that the slope of the theoretical current-voltage characteristic differs markedly from that of the measured characteristic and this represents a significant shortcoming in the present theoretical model. The reasons for these shortcomings are discussed at length in Chapter 3, and should be reduced by the evolution of improved theoretical models.

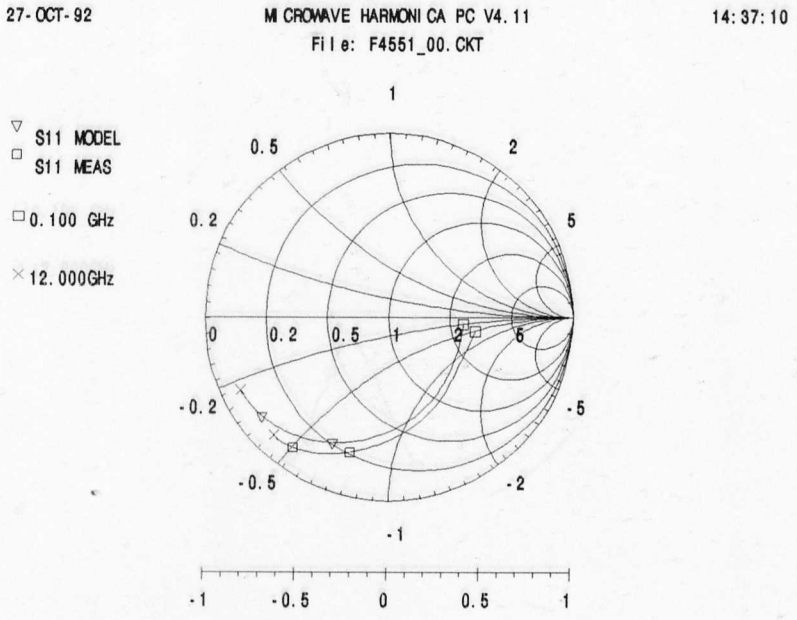
Evaluation of theoretical model values as used in the more physical model for "Microwave Harmonica (M.H.)" at 300 K											
Applied bias (V)	(2)	(3)	(4)	(5)	(6)	(7)	(8)	(9)	(10)	(11)	(12)
0.0	0.0	10	2.6	240	11.9	1.7	238	12	1.7	28	100
0.2	0.11	275	0.85	215	19.4	1.0	186	36	0.6	30	60
0.4	0.22	390	0.66	198	27.6	0.75	150	84	0.25	-556	-556
0.6	0.33	476	0.56	185	36.7	0.56	121	179	0.11	-74	120
0.8	0.44	554	0.5	172	49.3	0.42	95	358	0.06	171	71
Model values for 77 K											
0.0	0.0	16	2.6	240	12	1.7	238	12	1.7	362	1000
0.4	0.24	407	0.64	197	28	0.75	147	90	0.23	8.5	-80

Table 4.3 The above table summarises the values which were used in the "Microwave Harmonica" simulation which were calculated using the theoretical model discussed in chapter 3. Column (1) represents the applied bias (V), column (2) shows the equivalent bias (V) of the model. Columns (3) and (4) describe the calculated length of the depletion length (Å) and the Capacitance (pF) which results from the sum of the charge separation lengths respectively. Columns (5,6, and & 7) and (8,9, and 10) describe the barrier heights in meV, the resultant transmission coefficient ($*10^{-3}$) and the subsequent escape times (pS) of the emitter and collector barriers, respectively. Finally, columns (11) and (12) show the calculated value for the differential resistance (Ω) and the value suggested by the model (Ω) from the fit with the measurements

The following Figures 4.28-4.31 illustrate the match between the performance of the "Microwave-Harmonica" model (the values of which are summarised in Table 4.3) based on the *ab initio* calculations, and the measured impedance. The agreement between the performance of the equivalent circuit (with components derived from *ab initio* calculations) and the measured performance is shown in Figure 4.28 (top) to be quite good at zero bias. At low temperature (Figure 4.31 (top)) the agreement between the model and the measurements is even better. This is simply a reflection

of the effect of the reduced conductance at low temperature. The lack of agreement between the modelled and measured behaviour when biased on resonance was expected to be poor since in the case of the theoretically calculated components, their magnitude can vary by large amounts and these effects are not attenuated by the interaction with the embedding network. Hence, the measured performance only shows a degree if instability (Figure 4.29 (top) and 4.31 (bottom)) while the calculated performance suggests reflection coefficients in excess of unity.

The poorer agreement between the modelled and measured performance shown in Figure 4.30 is, possibly a result of the effect of a low conductance on the measured values of impedance.



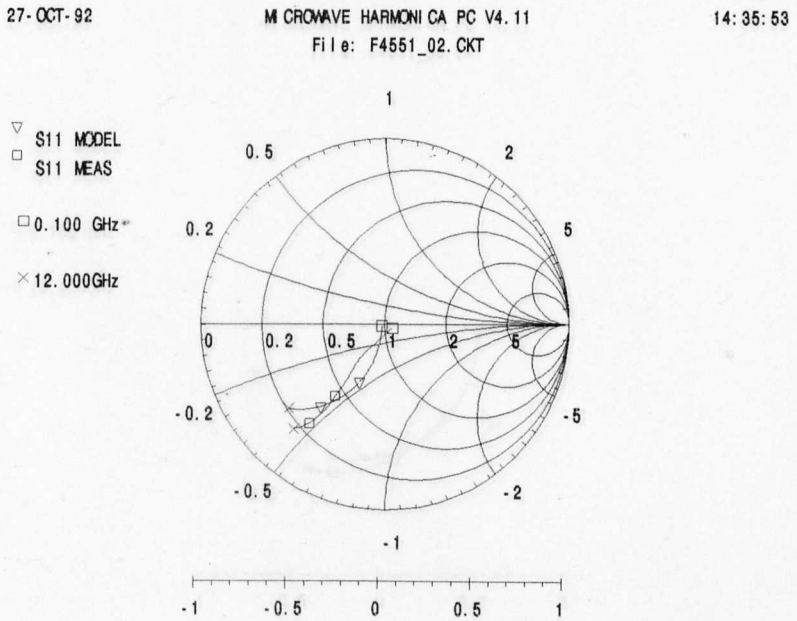
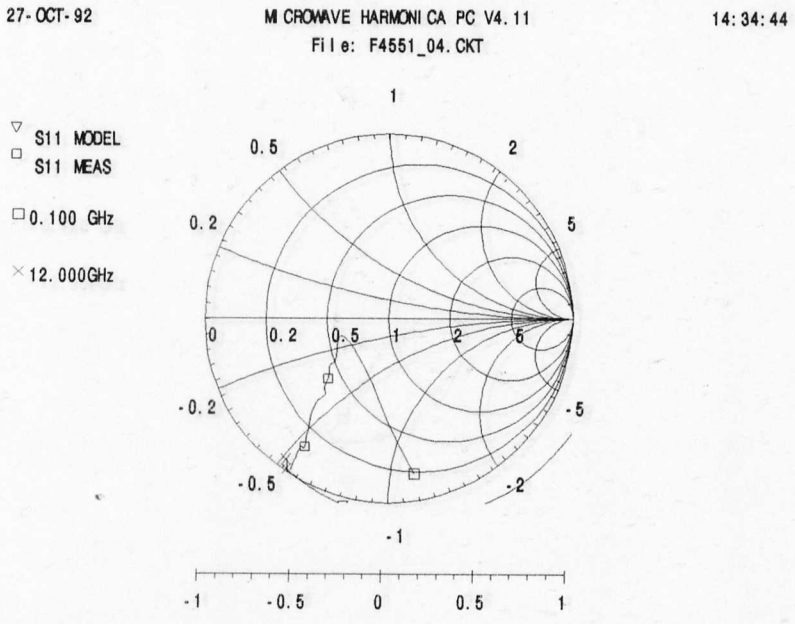


Figure 4.28 Theoretical model versus measured impedance at 0.0 and 0.2 volts applied bias



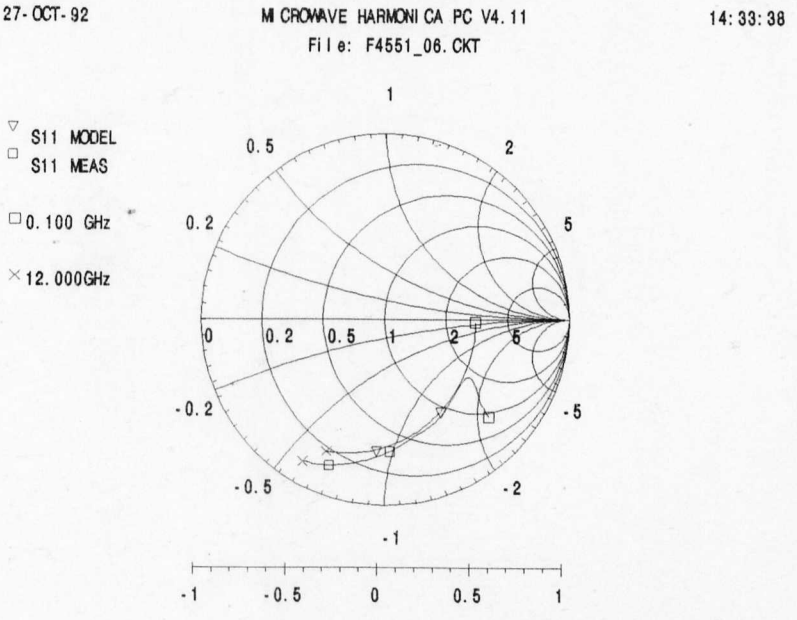


Figure 4.29 Theoretical model versus measured impedance at 0.4 and 0.6 volts applied bias

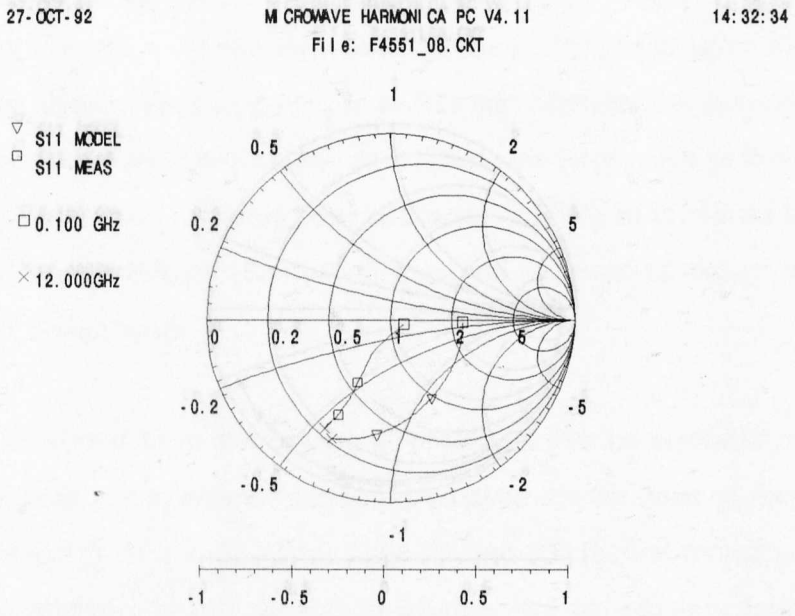


Figure 4.30 Theoretical model versus measured impedance at 0.8 volts applied bias

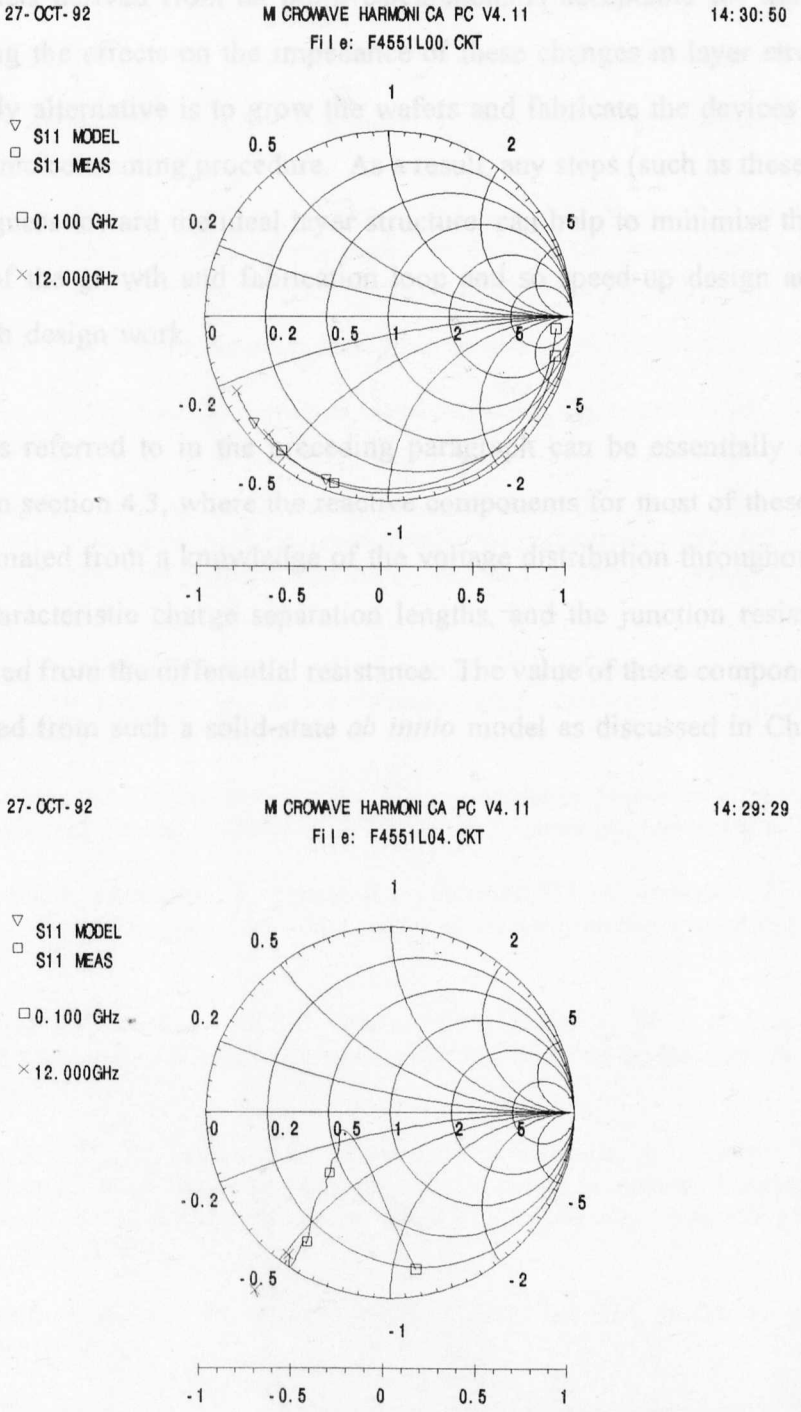


Figure 4.31 Theoretical model at 77 K versus measured impedance at 0.0 and 0.4 volts.

In conclusion, the parammetric study of the implications of layer structure differences on the high-frequency behaviour of DBRT's has been carried out. The performance of the models derived from *ab initio* calculations is acceptable for the purposes of investigating the effects on the impedance of these changes in layer structure, given that the only alternative is to grow the wafers and fabricate the devices and this can be a very time consuming procedure. As a result, any steps (such as these) to improve the initial guess toward the ideal layer structure, can help to minimise the number of iterations of the growth and fabrication loop and so speed-up design and lower the cost of such design work.

The models referred to in the preceding paragraph can be essentially any of those discussed in section 4.3, where the reactive components for most of these models can be approximated from a knowledge of the voltage distribution throughout the device and the characteristic charge separation lengths, and the junction resistance can be approximated from the differential resistance. The value of these components can then be calculated from such a solid-state *ab initio* model as discussed in Chapter 3.

4.6 References:

[1] Pollard, R (1992). *Private Communication*. Leeds University Department of Electronic and Electrical Engineering.

[2] Hackborn, R.A. (1968). An automatic network analyzer system. *Microwave J.* **11**, 45-52.

[3] G. Millington (1991). *Private Communication*. Leeds University Department of Electronic and Electrical Engineering.

[4] Gearing, J.M., Crim, D.A., Morgan, D.G., Coleman, P.D., Kopp, W. & Morkoc, H. (1987). A small-signal equivalent-circuit model for GaAs-$Al_xGa_{1-x}As$ resonant tunneling hetero-structures at microwave frequencies. *J. Appl. Phys.* **61**(1), 271-276.

[5] Sterzer, F. (1961). Tunnel-diode microwave oscillators. *Proc. IRE*, 744-753.

[6] Sterzer, F. (1965). Analysis of GaAs tunnel diode oscillators. *IEEE Trans. Electron. Dev.* **12**, 242-245.

[7] Shewchuk, T.J., Chapin, P.C., Gering, J.M. & Coleman, P.D. (1985). Microwave admittance characterisation of GaAs-$Al_XGa_{1-X}As$ resonant tunneling heterostructures. *IEEE proc. Advanced concepts high speed semiconductor devices and circuits*, 370-379. Cornell University, Ithaca, N.Y.

[8] Sammut, C.V. & Cronin, N.J. (1992). Comparison of measured and computed conversion loss from a resonant tunnelling device multiplier. *IEEE Microwave and Guided Wave Letters*, **2**(12), 486

[9] Sammut, C.(1992). An Investigation of the microwave properties of resonant tunnelling devices. *PhD. Thesis*, Department of Physics and Astronomy, University of Bath.

[10] Miles, R.E., Millington, G., Pollard, R.D., Steenson, D.P., Chamberlain, J.M. & Henini, M. (1991). Accurate equivalent circuit model of resonant tunnelling diodes. *Electronics Lett.* **27**(5), 427-428.

[11] Brown, E.R., Söllner, T.C.L.G., Parker, C.D., Goodhue, W.D. & Chen, C.L. (1989). Oscillations up to 420 GHz in GaAs/AlAs resonant tunneling diodes. *Appl. Phys. Lett.* **55**(17), 1777-1779.

[12] Sollner, T.C.L.G., Brown, E.R., Parker, C.D. & Goodhue, W.D. (1990). High-frequency applications of resonant-tunnelling devices. Electronic properties of multilayers and low-dimensional semiconductor structures. Eds. J.M. Chamberlain, L. Eaves & J-C portal. NATO ASI Series B: **231**.

[13] Luryi, S. Frequency limit of double-barrier resonant tunneling oscillators. *Appl. Phys. Lett.* **47**(5), 490-492.

[14] Fu, Y. & Dudley, S. (1993). Quantum Inductance with linear response theory. *Phys. Rev. Lett.* **70**(1), 65-68.

[15] Kesan, V.P., Neikirk, D.P., Streetman, B.G. & Blakey, P.A. (1987). A new transit-time device using quantum well injection. *IEEE Electron Dev. Lett.* **8**, 129-131.

[16] Song, I. & Pan, D. (1987). Efficiency and power output of the quantum-well injection transit-time device. *IEEE Electron Dev. Lett.* **8**, 560-562.

[17] Sollner, T.C.L.G., Goodhue, W. D., Tannenwald, P.E., Parker, C.D. & Peck, D.D. (1983). Resonant tunnelling through quantumwells at frequencies up to 2.5 Thz. *Appl. Phys. Lett.* **43**(6), 588-590.

[18] Brown, E.R. Parker, C.D. Sollner, T.C.L.G. (1989). Effect of quasi bound-state lifetime on the oscillation power of resonant tunneling diodes. *Appl. Phys. Lett.* **54**(10), 934-936.

[19] Eaves, L. (1990). Analogies in optics and micro electronics. Ed. W. van Haeringen. & D. Lenstra, 227-242: Kluwer Academic Pub. Netherlands.

[20] Booker, S.M. (1992) Theory of tunnelling in double-barrier heterostructures. *Ph.D Thesis.* University of Nottingham.

CHAPTER 5

Device Measurements and Applications

5.1 Introduction

This chapter examines the attempts to measure the small-signal impedance at W-band (75-110GHz) on sòme of the DBRT structures mentioned previously. To the author's knowledge such measurements have not yet been reported in the literature but were thought to be important for extending the characterization work mentioned in Chapter 4, and for the improved design of embedding networks at these higher frequencies.

The latter part of the chapter examines the results of some of the applications of the DBRT devices in generating and receiving microwave and millimetre-wave radiation.

5.1 Millimetre-wave impedance measurement

As was mentioned in the above introduction attempts were made to measure the impedance of the DBRT devices, with the aim of understanding the layer-dependent characteristics which affect the millimetre-wave properties of the devices.

5.1.1 Small-signal measurement (waveguide)

The measurements at 100GHz (W-band) were complicated by the lack of affordable "off-the-shelf" impedance measuring equipment, and in particular a broadband high-

power source. The lack of such a source required the use of an amplifier and harmonic up-converter (multiplier), the output power of which was approximately 0dBm, while the loss through the measurement system was about 15dB. The elaborate linearisation and calibration of the diodes, and subsequently the whole system, was accomplished by storing intermediate calibration data on a microcomputer.

The technique used to measure the W-band impedance was based on a quasi six-port technique (Figure 5.1(a)). In this technique, information on the power measured at four of the ports (as a result of reflections from the load port with the signal input forming the sixth port) relates to the complex impedance of the load [1], and as shown in Figure 5.1(b). The state of the system is altered using a four position waveguide switch and the three power ratios (in response to measurements on a flush short-circuit, offset short and a matched load) determine the complex reflection coefficient of the device under test. The output voltages of the detector diodes are non-linear with respect to both incident power and frequency, and require a complicated calibration and linearisation procedure. It was important to carry out this calibration procedure over as large a dynamic range as possible. Typically this range was slightly less than 20dB ie. the output of the multiplier (0dBm) minus the loss through the system, (15dB) down to the reasonable lower limit of the detector diodes (-35dBm). The measured voltages for the different states of the system were recorded at each of the ports for known power levels (ie. the linearisation procedure) and subsequent unknown powers were calculated by interpolation from the previous voltages. The accuracy of the power measured at each port relative to other ports determined the accuracy of the measured impedances; clearly this accuracy is dependent on the stability and calibration of the detector diodes. Once the initial stages of calibration have been carried out, the system can be calibrated using an intermediate error network as described in Chapter 4. The error terms are: firstly, the three values of precision open, offset open (l_1&l_2), short and off-set short (l_1&l_2), and, secondly, the varactor impedance at three different bias voltages. The values of the error terms for both calibration procedures are used for de-embedding to the measurement plane in the first instance, and then via the varactor to the plane of the device itself.

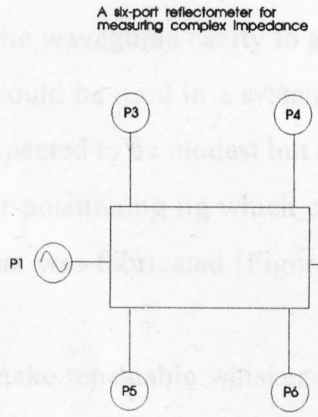


Figure 5.1 (a) Schematic of a six-port reflectometer

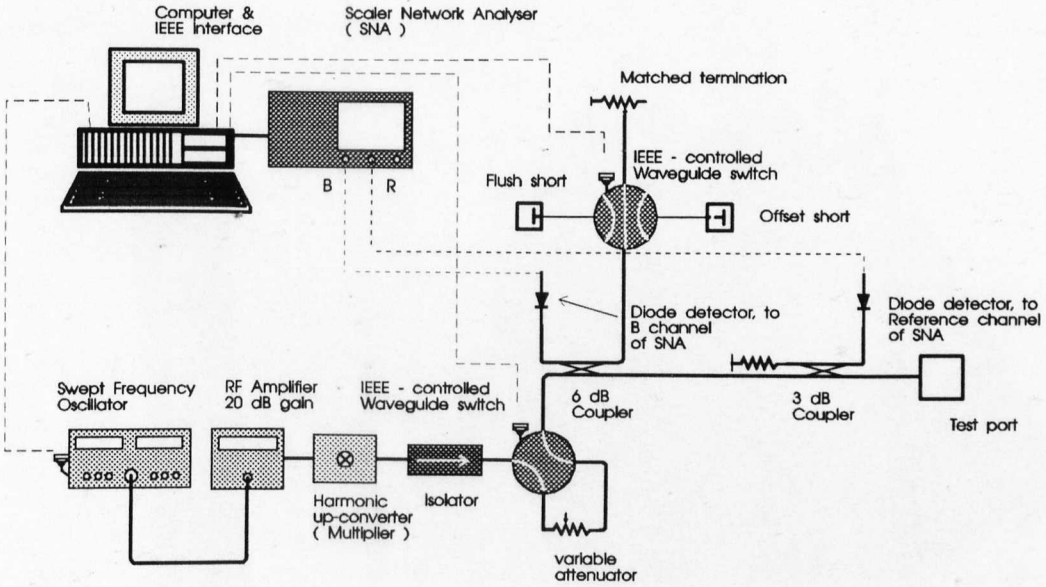


Figure 5.1 (b) W-band multistate reflectometer for measuring vector impedances

The devices used for the impedance measurements were of the point-contact type and were measured directly in the waveguide cavity to avoid package parasitics, and since this was how the devices would be used in a system. The accuracy of measurements made in this fashion was expected to be modest but nevertheless was thought to useful impedance data. A whisker-positioning jig which combined a waveguide cavity with interchangeable chip-carriers was fabricated (Figure 5.2(a)).

The aim of the jig was to make repeatable whisker contact using the same whisker to a selection of devices on separate carriers. These carriers (Figure 5.2(c)) formed the bottom of the waveguide cavity and were machined to be as near identical as possible. The method of making measurements on a varactor diode in place of the DBRT diode (on a similar chip-carrier) would allow easy de-embedding to be carried out, provided that the cavity was not altered significantly during the changing of the chip carriers and recontacting (raising and lowering of the whisker). The results after de-embedding using the varactor method should give the impedance of the DBRT device alone.

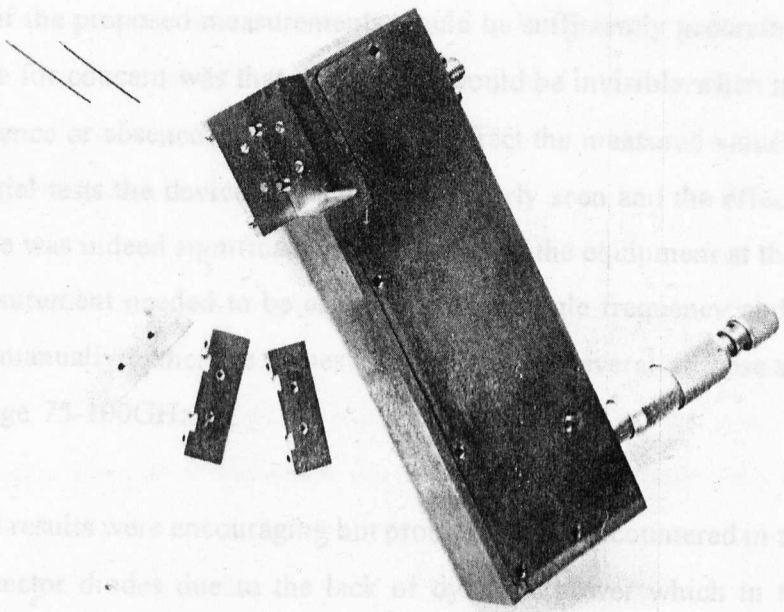


Figure 5.2(a) W-band measurement (whisker) jig

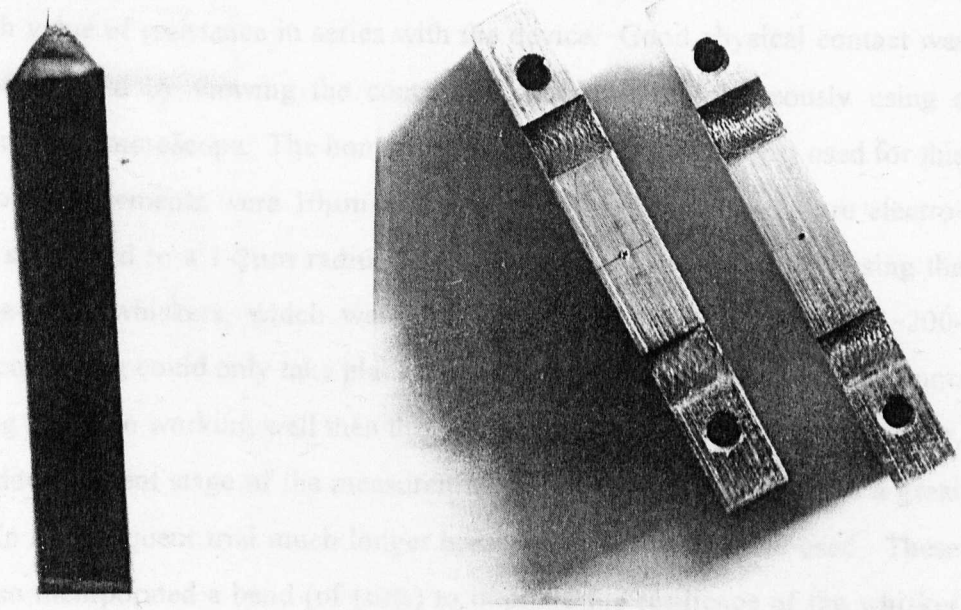


Figure 5.2 (b) Whisker & pin, (c) Interchangeable chip-carriers

The whisker-contacting jig was subsequently made and tests were carried out to discover if the proposed measurements would be sufficiently accurate and repeatable. One cause for concern was that the devices would be invisible when in the cavity and their presence or absence would not greatly affect the measured values of impedance. In the initial tests the device (varactor) was clearly seen and the effect of bias on the impedance was indeed significant. A limitation of the equipment at the time, was that each measurement needed to be carried out at a single frequency and we could only expect to manually gather the values of impedance at several of these spot frequencies in the range 75-100GHz.

The initial results were encouraging but problems were encountered in the linearisation of the detector diodes due to the lack of dynamic power which in turn resulted in software-related problems. Also during the initial trials the problem of recontacting the devices was encountered. A great deal of finesse was required to contact a whisker without damaging the point, especially where contact had been made to the device and for whatever reason (thought to be surface dirt or oxide), an electrical contact was not achieved. The solution to this problem involved applying a high voltage to the device, while it was protected (from the subsequent high current surge) using a high value of resistance in series with the device. Good physical contact was achieved beforehand by viewing the contacting procedure simultaneously using a curve-tracer and a microscope. The home-made whiskers (Figure 5.2(b)) used for this stage of the measurements were 10μm diameter phosphor-bronze and were electro-chemically sharpened to a 1-2μm radius point. Experience suggested that using the initial home-made whiskers, which were straight and as short as possible (~200-300μm), recontacting could only take place a few times before the point became blunt. If everything had been working well then this would have been satisfactory. However, during the development stage of the measurements this problem proved to be a great handicap. In a subsequent trial much longer home-made whiskers were used. These whiskers also incorporated a bend (of sorts) to improve the resilience of the whisker point by allowing the whisker to bend more under the contact pressure. In the measurements which followed the devices could no longer be "seen". It was

concluded therefore that the short whisker, together with the presence of the whisker-pin in the waveguide, were important criteria for providing a match between the device and the waveguide. Attempts at varactor de-embedding during these early stages proved unsuccessful, due mainly to the stability of the system and problems linearising the detectors.

In conclusion, the attempts at measuring the small-signal impedance at 100GHz were abandoned due to the lack of maturity of the measurement system and the difficulty of achieving sufficiently repeatable whisker contacts. As the system develops and becomes more automated and especially if the stability and sensitivity of the detectors can be improved, then attempts may again be made to measure the impedance of DBRT devices in waveguide.

The future however, for DBRT devices seems to be in a stripline environment where lower impedances can be achieved and where track tolerances are more easily controlled than the micro-machining required for sub-millimetre waveguide circuits. It is also then, more appropriate to measure the impedance of the devices in these environments. Stripline techniques allow an improved impedance match between the devices and the microwave circuit, and hence improve the power coupling to and from the diode. However, stability of the DBRT devices may now pose a problem (in these more closely matched circuits) if impedance is to be measured, and the circuits may need to be un-matched to facilitate these measurements. Sections 5.2.3 and 5.7 discuss more aspects of these stripline circuits with respect to incorporating DBRT devices in millimetre-wave circuits of the future.

5.1.2 Small-signal impedance measurement (Quasi-optical)

As an alternative to measuring the DBRT impedance in waveguide, a quasi-optical method is possible [2]. The DBRT diode itself remained in waveguide, thereby easing contact formation and subsequent de-embedding (if this had been carried out), without

the need to introduce quasi-optical coupling directly to the device (perhaps by using planar antennae). It was considered too great a task for the present study to undertake a full de-embedding procedure for the device impedance when in a quasi-optic environment. This would have required complete characterization of many different types of planar antennae before the device impedance could itself be found. Instead a horn antenna provided the coupling between the quasi-optical network and the waveguide. The microwave signal was fed into the waveguide and device via the horn antenna and a high density poly-ethylene (HDPE) lens, where the coupling efficiency for such horn antennae and lenses were in the region of 90%. The techniques of de-embedding should in principle enable the effects of the horn and waveguide to be removed in a similar way to the case when using conventional microwave techniques. The experimental set-up used for carrying out quasi-optic measurements of this type is described in detail in Chapter 10 of Millimetre-wave Optics, Devices and Systems [2].

There are three main reasons which favour the quasi-optical approach for measuring impedance at high millimetre and sub-millimetre wave frequencies. First: the loss through such systems is very much lower than that of conventional waveguide. Second: the frequency bandwidth over which the quasi-optical network can perform is very much wider than is permitted for waveguide (70-500GHz versus 75-110, 90-140, 110-170 and 140-220 etc.). The system limitations are more dependent on weaknesses of particular elements of the circuit ie signal sources, horns, device cavities and detectors. Third: the measurement depends on the difference between the polarization angle and path length difference of the reflected signal (from the DUT) and that of a reference signal (the polarization angle, path length and amplitude of which, can be controlled), which gives the complex reflection coefficient of the DUT. The measurement is based on a null point (or minimum) detection, when the signals are combined [ie precisely out of phase], and this removes the need to know the precise amplitude of the power falling on the detectors. This insensitivity to power removes a major source of error, which otherwise would require extensive characterization of the detectors and is dependent on their stability etc. [3].

Good as such a system is, for measuring impedance at high millimetre-wave frequencies, accurate de-embedding of the devices still remains a problem. Also, the lack of an electronically controlled swept-frequency source limited the system's usefulness, in much the same way as it did for the waveguide measurements mentioned in the previous section. To the author's knowledge, techniques of de-embedding (similar to those which have been carried out in waveguide) have not yet been reported for such quasi-optical measurements. As a result of the time required to develop these techniques and to perfect such a system, impedance measurements on existing DBRT devices were not, to the authors knowledge, attempted.

5.1.3 Large-signal impedance measurement

The measurement of impedance in the non-linear régime (ie. large-signal) is complicated at millimetre-wave frequencies in the same way as the small-signal measurements discussed in sections 5.1.1 and 5.1.2. That is, small-signal measurement capabilities are required before the large-signal measurements can be attempted (ie. loads can be measured and their complex conjugates evaluated). To the author's knowledge such large-signal measurements at millimetre-wave frequencies have not been reported in the literature. Perhaps this is again due to the lack of available output power from existing DBRT devices. In the future, as devices and small-signal measurement capabilities improve, it should be possible to improve the design of oscillator embedding circuits in order to make large-signal measurements, and subsequently, to improve the resulting oscillators.

5.2 DBRT diodes as oscillators

The usefulness of DBRT diodes in the generation of microwave and millimetre-wave power has already been introduced in Chapter 1, and the success achieved in this respect (using devices fabricated from some of the material grown during the course

of this study) is described below.

The results can be divided into those measured using a quasi-optical approach and those measured using conventional waveguide techniques. The quasi-optical approach clearly shows the device's ability to either simultaneously operate at multiple frequencies, or to oscillate and up-convert this power to higher harmonics. Such behaviour can be seen (and can occur) because of the large inherent bandwidth of such quasi-optical systems. Care therefore, needs to be exercised in interpreting such spectra since multiple reflections can occur within the system and would give similar results. Waveguide techniques, on the other hand, tend to quickly attenuate the frequencies outside the band (75-110GHz) and are also limited by the bandwidth of the spectrum analyzer (mixer) and generally so show "cleaner" spectra.

5.2.1 Quasi-optical measurement of oscillators

The measurement system used for measuring the output power spectrum of a device differs from the one used to measure its impedance, but is based on the same principles. Figure 5.3 shows a schematic of the circuit which could be used to measure impedance. However, due to the degree of difficulty of de-embedding (lack of appropriate loads) and the lack of investment (time and effort) in this area, such impedance measurements were never carried out.

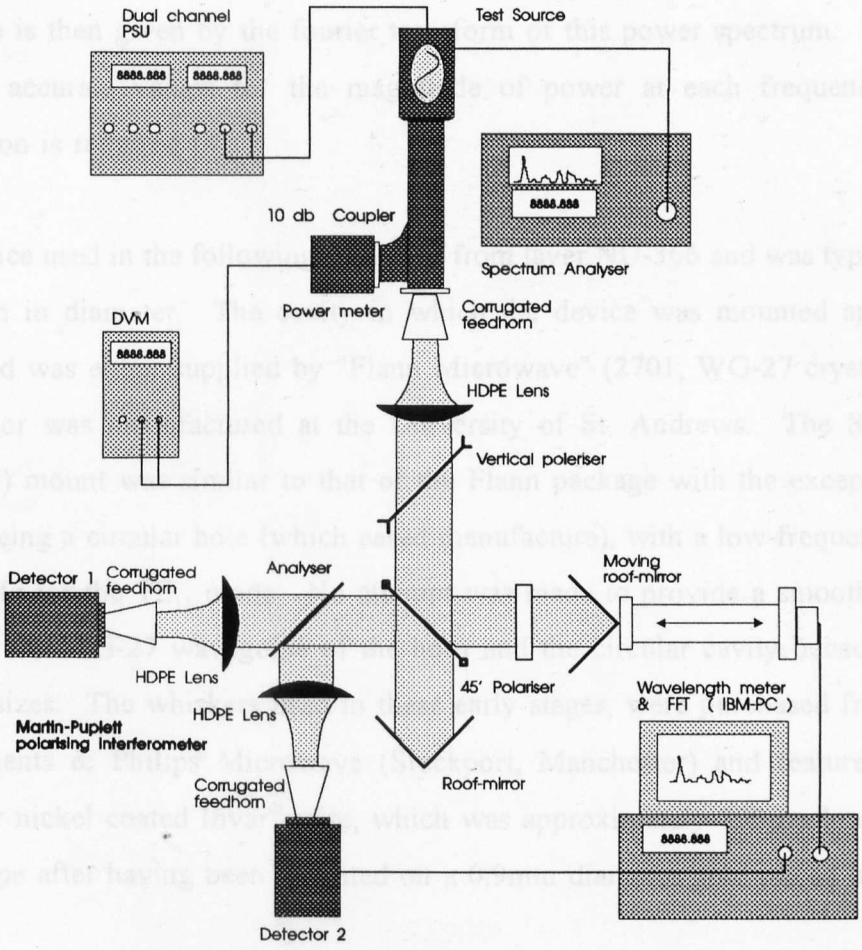


Figure 5.3 Quasi-optical set-up for measuring the output spectrum of a DBRT device

The circuit uses a very sensitive broadband "Golay" detector and phase-locked amplifier and again makes use of a Martin-Puplett polarizing interferometer to count the in-phase wavelengths as the length of the resonant cavity is varied. The frequency response is then given by the fourier transform of this power spectrum. In order to achieve accurate values for the magnitude of power at each frequency, careful calibration is required [4].

The device used in the following figures is from layer NU-366 and was typically 5μm or 10μm in diameter. The cavity in which the device was mounted and whisker contacted was either supplied by "Flann Microwave" (2701, WG-27 crystal-detector mount) or was manufactured at the University of St. Andrews. The St Andrews (circular) mount was similar to that of the Flann package with the exception of the cavity being a circular hole (which eased manufacture), with a low-frequency cut-off of 76GHz for the TE_{11} mode. No attempt was made to provide a smooth transition between the WG-27 waveguide of the horn and the circular cavity because of their similar sizes. The whiskers used in these early stages, were purchased from Philips Components & Philips Microwave (Stockport, Manchester) and featured a 25μm diameter nickel coated Invar® wire, which was approximately 800μm long and bent into shape after having been mounted on a 0.9mm diameter gold plated brass pin.

Initial results were achieved using 5μm diameter devices from wafer NU-298, but the smaller levels of power available from these devices quickly lead to their replacement by devices from layer NU-366. The modest levels of output power (a few micro-watts, measured on another occasion using a boonton power meter) exhibited by the DBRT's at these high frequencies is not thought to be intrinsic to the devices but through the poor match with the external circuit. Although the values of maximum available power based on the current-voltage characteristics [5,20,38] look promising, the fraction of this power available to drive the load approximately that of the total

power minus the power dissipated in the load (essentially, $\Delta I/2.(R_L-R_{NDR})$ [38], Figure 5.5 shows a typical output spectrum for such a device and its current-voltage characteristic is shown in Figure 5.4.

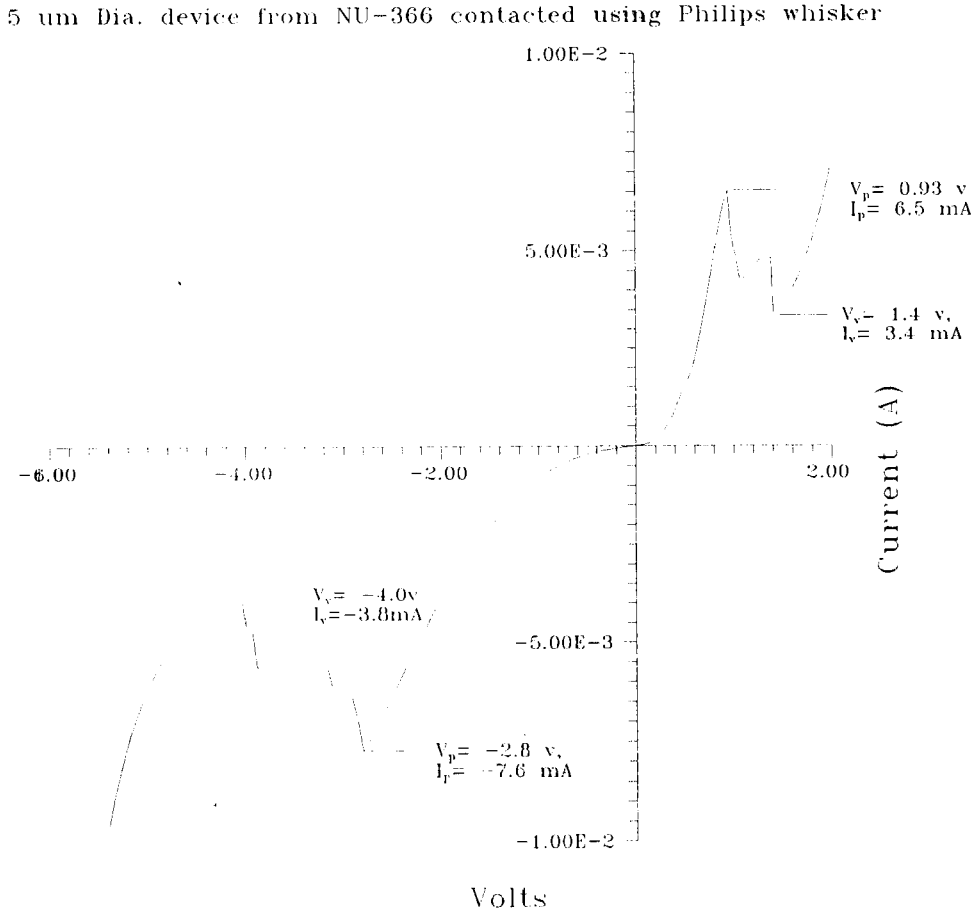


Figure 5.4 Current-voltage characteristic for a typical device from wafer NU-366

NU-366 had similar barrier and well widths to NU-298 but included a low-doped "drift" region in the collector. These structures (NU-366 & NU-298) were similar to

those used by Rydberg et al [13,39] and Sollner et al [8,21] and have previously yielded devices which oscillated at over 100GHz. The device sizes available were 10μm, 5μm and 2μm (in diameter) but most of the results were achieved using the 5μm devices, since this size was typical of the devices used by others.

It should be noted that the following results describe only a brief study of the DBR T device using the quasi-optical approach, mainly because of the difficulty associated with the manufacture of cavities and mounting of devices. In-depth studies would require a greater supply of cavities and whiskers and realistically small-signal impedance values of the device and the embedding networks.

From Figure 5.4 it can be seen that the current-voltage characteristic of devices from NU-366 is not symmetric (with respect to the position of the current peak) with regard to the polarity of the applied voltage. The magnitude of the current peak, however, remains largely unaffected by the voltage drop across the collector "drift" region, while it is the product of the voltage difference and current difference in the NDR region which approximates to the maximum power available for a device (3/16 $\Delta I.\Delta V$)[5]. Hence in an ideal case, the maximum power available from a typical device from NU-366 is approximately four times greater for the negative biased polarity than for the positive biased polarity (Figure 5.4). This conclusion is reflected in the relative power outputs shown in Figures 5.5 and 5.6 for the two polarities. The relative magnitudes of the output power were 2184 (arb. units) and 8828 (arb. units) for the forward and reverse biases respectively. The difference in oscillation frequency for the different polarities is thought to result from the difference in magnitude of the NDR and also from the differences in the junction capacitance for the different polarities. These differences in frequency are thought to be only slight due to the effect of the embedding network (mainly the whisker) in determining the oscillation conditions. Another example of this voltage-dependent oscillation is shown in Figures 5.6 and 5.7 where for a similar polarity the frequency differs by 22.5GHz for a change in bias from -3.53 to -3.60. In these examples (Figures 5.6 and 5.7) we can see that there are apparently two stable "states" (frequencies) each of which is

reproducible to 1MHz and depends on the exact bias point on the current-voltage characteristic and therefore on the two differing values of NDR at these two operating points. A technique to exploit this bias dependent frequency behaviour by controlling the slope of the NDR region using a third "gate" electrode, is discussed in section 5.6.

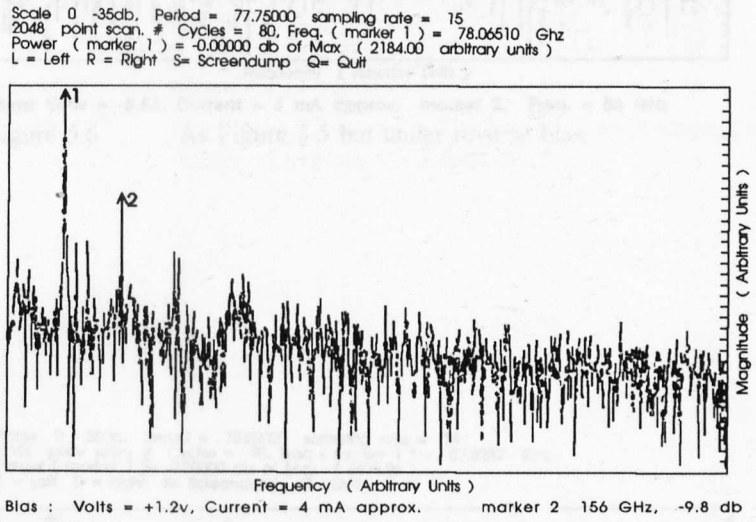
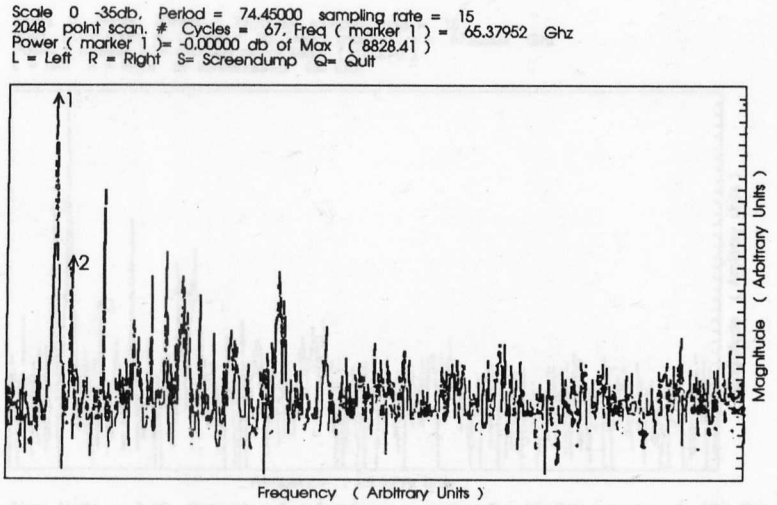
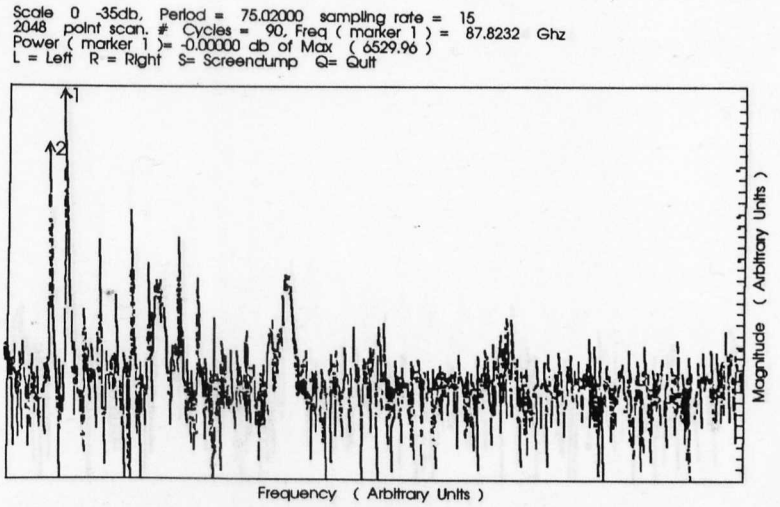


Figure 5.5 Output spectrum for a 5 μm dia. device from 366 under forward bias



Bias: Volts = -3.53, Current = 5 mA approx. marker 2, Freq. = 86 GHz

Figure 5.6 As Figure 5.5 but under reverse bias



Bias: Volts = -3.60, Current = 5 mA approx. marker 2, 65 GHz

Figure 5.7 As Figure 5.6 but at an increased bias

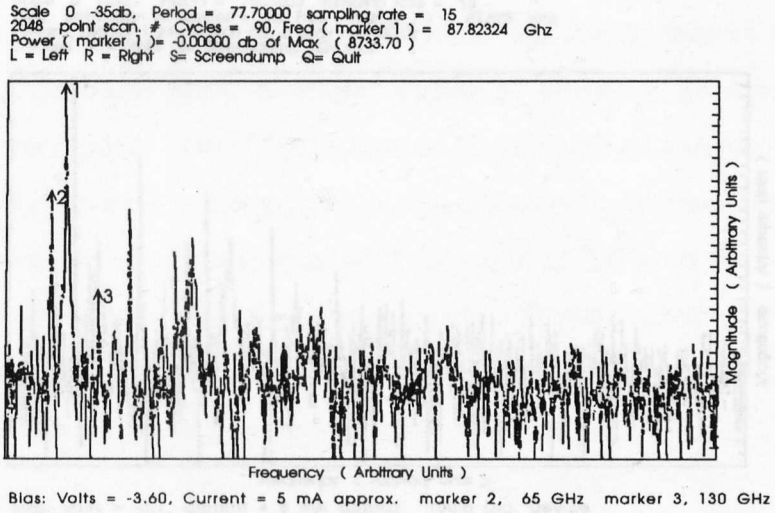


Figure 5.8 As Figure 5.7 but with the addition of an extra length of waveguide on the output side

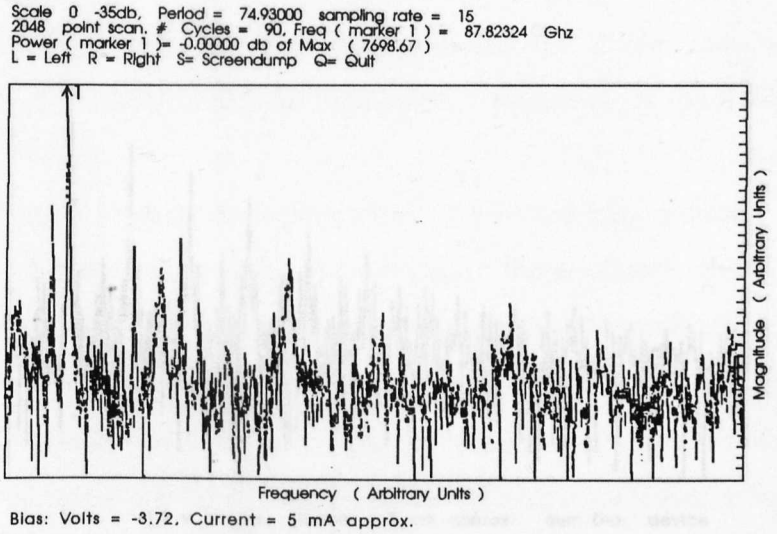


Figure 5.9 As Figure 5.8 but with an isolator rather than the extra length of waveguide

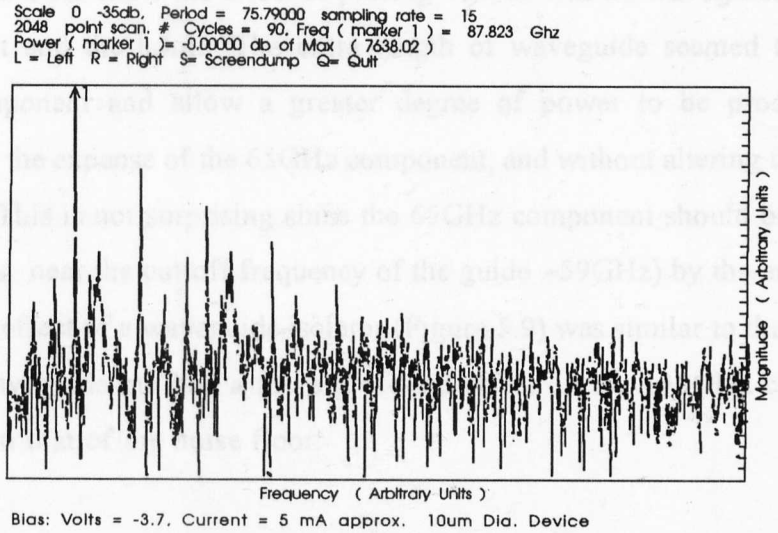


Figure 5.10 Output spectrum of a 10μm dia. device from 366 (forward biased) in a circular "home-made" cavity

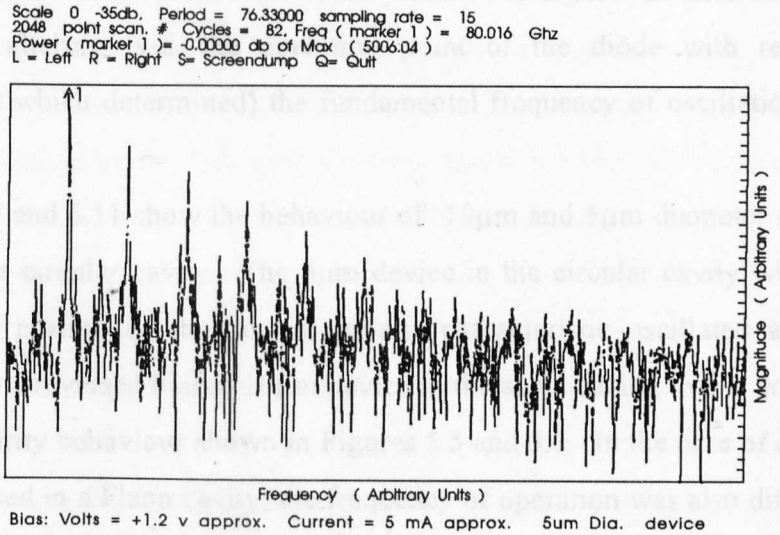


Figure 5.11 As Figure 5.10 but for a 5μm dia. device under negative bias

Figures 5.7 and 5.8 show the effect of placing 4cm of WG-27 waveguide between the Flann mount and the horn. The extra length of waveguide seemed to favour the 87GHz component and allow a greater degree of power to be produced at this frequency at the expense of the 65GHz component, and without altering the oscillation frequency. This is not surprising since the 65GHz component should be particularly attenuated (ie. near the cut-off frequency of the guide ~59GHz) by the extra length of guide. The effect of a waveguide isolator (Figure 5.9) was similar to that of the extra length of waveguide but had a more profound effect on the 130GHz component by reducing it to that of the noise floor.

During the course of these measurements it was found that the position of the back-short affected the power (by up to 30%) at 65GHz and 87GHz independently, tending to favour one or other frequency. As a result, each of these frequencies of oscillation were suspected of being independent fundamental modes of operation. That is, if the observed oscillation was taking place at a harmonic then the lower harmonic power together with the conversion loss would prevent the signal reflected from the back-short from altering (via. the operating point of the diode with respect to the environment which determined) the fundamental frequency of oscillation.

Figures 5.10 and 5.11 show the behaviour of 10μm and 5μm diameter devices when placed in the circular cavity. The 5μm device in the circular cavity when biased in the forward portion of the current-voltage characteristic oscillated at a different frequency to a reversed biased 10μm device in the same cavity, this is consistent with the bias polarity behaviour shown in Figures 5.5 and 5.6. In the case of a 5μm device forward-biased in a Flann cavity, the frequency of operation was also different to that of a similar-sized device under similar bias conditions (forward bias) in the circular cavity and the output power was slightly greater (5006 (Fig. 5.11) versus 2184 (Fig. 5.5)). The changes were small, however, considering the change in cavities etc. but they indicate that the DBRT devices oscillate fairly easily independently of the exact nature of the cavities in which they sit. This is probably a reflection of the influence of the "over-sized" (800μm) whiskers on the operation of these particular device-cavity

combinations. Unfortunately, at the time these measurements were carried out there were no home-made whiskers available.

In conclusion the DBRT devices provided only modest amounts of fundamental mode power at millimetre-wave frequencies, for reasons discussed previously, and also because attempts were not made to optimise the cavities nor to improve the whisker contacts. The sensitivity of the operating frequency to bias is noted, as is the readiness of the devices to operate simultaneously at many specific frequencies (due to the broadband NDR).

5.2.2 Waveguide measurements of oscillators

Similar studies of the potential of DBRT's to generate microwave and millimetre-wave power were undertaken in waveguide. Millimetre-wave power was observed for 5μm diameter devices in the Flann cavities although no spectra were recorded. Power measurements (using a spectrum analyzer) revealed similar powers to those measured by quasi-optical methods. However, the latest result in a Sharpless-type package using 200μm long (10μm dia.) whiskers was -9.8dBm. Unfortunately, the device stopped oscillating before a spectrum could be recorded. Most of the work in waveguide concentrated on 8GHz to 12GHz (X-band) frequency range, since this was a convenient range where components were readily available and the machining tolerances were easily achieved. Also, the devices could be larger (50 and 20μm dia.) and therefore wire-bonded and packaged (S-4). The effects of the embedding network were also much more easily studied. Again, however, very little work was carried out to optimise the X-band cavities in order to favour oscillation. Efforts were mainly concerned with measuring the impedance of the packaged devices as was discussed in chapter 4. Figures 5.12 and 5.13 show the typical output power spectra at X-band, for a 50μm diameter device from NU-104 (NU-195 was a repeat of this structure) and a 20μm diameter device from NU-298.

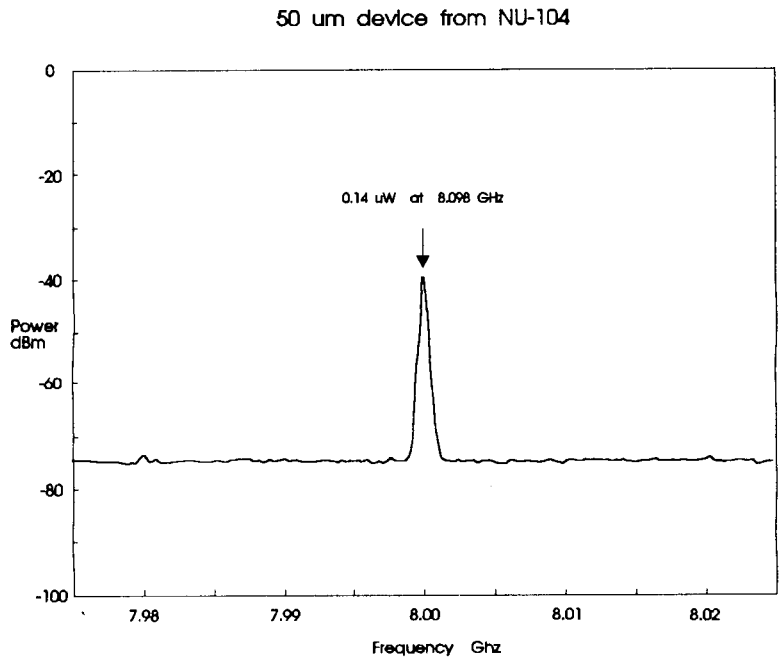


Figure 5.12 Output spectrum of a 50μm dia. device from NU-104 when oscillating in waveguide

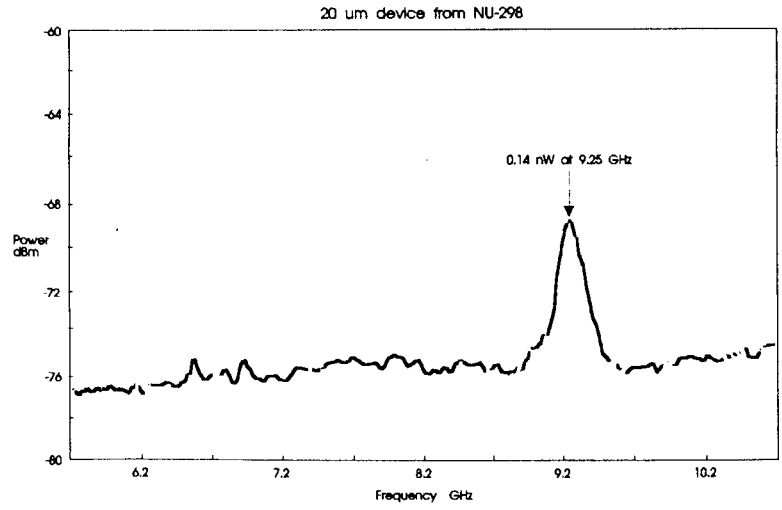


Figure 5.13 Output spectrum of a 20μm dia. device from NU-298 when oscillating in waveguide

The measured powers were again low, at around a tenth of a micro-watt for the 50μm device and a tenth of a nano-watt for the 20μm device. Another result, of approximately 20μW (-17dBm) for a 20μm device from NU-469, represented (for a device in waveguide) the best output power at this frequency for this project up to this moment in time. However, often the devices oscillated at many different frequencies and the total power available from the device was distributed across the bandwidth permitted by the waveguide. Improved matching between the impedance of the waveguide and the devices should yield greater powers, but this is limited by the large inherent impedance mismatch between such low impedance devices (a few ohms) and the waveguide (370 ohms). The advantage however, of waveguide is that high-Q (many hundreds) cavities are possible although as the frequency increases the losses also increase and reduce the possible Q's. The machining of such cavities at sub-millimetre wave frequencies is also extremely difficult.

An alternative to mounting the device directly in waveguide is to mount the device in stripline [37] and then use a stripline-to-waveguide transition to match the impedances. The advantage of stripline is that, in general, much lower impedances are possible. Unfortunately, stripline is a more lossy environment and therefore the Q's of such circuits are much smaller. Techniques for analysing and modelling the various kinds of stripline environments at millimetre-wave frequencies are still immature and represent the most important difficulty for realizing such millimetre-wave oscillators.

5.2.3 Microstrip measurements

In order to achieve an improved match to the packaged DBRT devices a simple microstrip circuit was fabricated. This consisted of a 50Ω transmission line on 10Thou. Duroid® with a co-axial connector to the bias network/filter on one end, and the packaged device connected to ground on the other. A tuning stub was placed some distance from the device and was used to balance the reactive component of the

device in order that the device sees an approximate conjugate match with the circuit into which it "looks".

Figures 5.15 and 5.16 show the output spectrum for a 20μm diameter device from NU-469. From Figure 5.15 it can be seen that the device is again oscillating at many different frequencies simultaneously. As was thought, the improved match between the microstrip circuit and the device, does indeed result in increased output power.

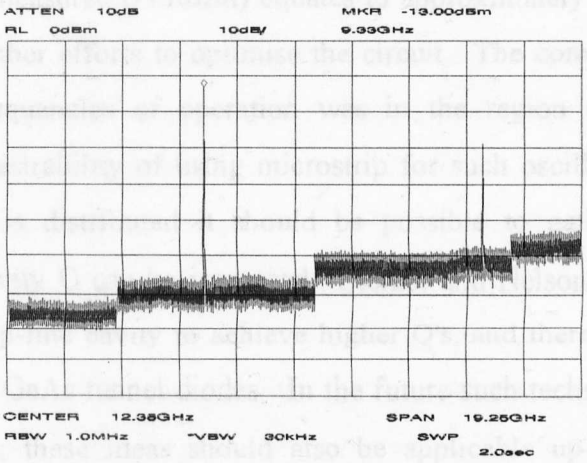


Figure 5.14 Output spectrum of a 20μm dia. device from NU-469 when measured in microstrip

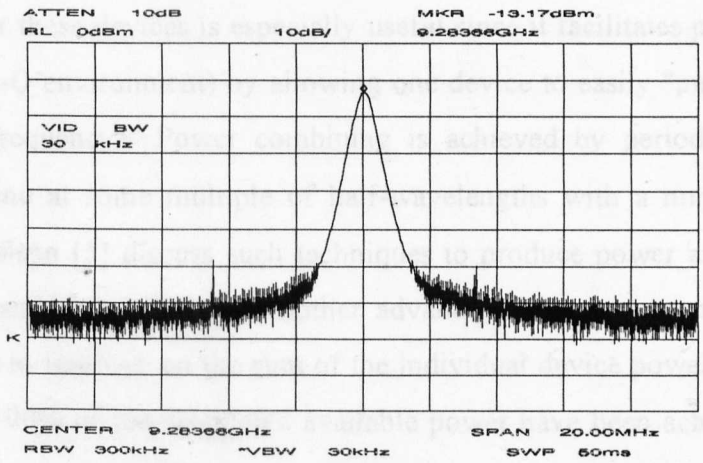


Figure 5.16 As Figure 5.15 but over a reduced bandwidth

The output power measured (-13dBm) equates to approximately 50μW, and this was achieved without other efforts to optimise the circuit. The combined power at each of the discrete frequencies of operation was in the region of 250μW and this demonstrates the desirability of using microstrip for such oscillators. Although the 250μW of power is distributed it should be possible to gather this at a single frequency if the cavity Q can be increased. Sterzer and Nelson [5] have designed a re-entrant microstrip-line cavity to achieve higher Q's, and therefore greater powers, using conventional GaAs tunnel diodes. In the future such techniques could be used for DBRT devices; these ideas should also be applicable up to millimetre wave frequencies (losses withstanding).

5.2.4 Power combining

Although the output power of individual DBRT devices is presently small, techniques of power combining should alleviate some of these problems. The broadband nature of the NDR for these devices is especially useful since it facilitates power combining (in a moderate-Q environment) by allowing one device to easily "pull" its neighbour to the same frequency. Power combining is achieved by periodically loading a transmission line at some multiple of half-wavelengths with a number of devices. Sterzer and Nelson [5] discuss such techniques to produce power at 0.85GHz using a hybrid-ring and three diodes. Another advantage in power combining is that it seems possible to improve on the sum of the individual device powers and as a result efficiencies of 90% of the calculated available power have been achieved [5].

At sub-millimetre wave frequencies the fabrication of microstrip ring circuits and other distributed circuits should be favoured by using monolithic techniques. The main rationale for using these techniques being to reduce the physical size of the circuits and therefore the associated losses. For example, $\lambda_g=\lambda_0/\sqrt{\varepsilon_{eff}}$ where λ_0 is the free-space wavelength, λ_g is the wavelength in the transmission line and ε_{eff} is the effective (high-frequency in microstrip) dielectric constant for GaAs (~8.2). Hence,

at 200GHz where λ_0 is 1.5mm then λ_g=524μm. This is only two individual chip separations for present devices, and is (in the discrete case) set by the ability to break and handle the individual devices. Hence the losses could be minimised by reducing unnecessary lengths of transmission lines. This can be achieved with ease monolithically while preserving the accuracy in the circuit fabrication by using photo-lithographic techniques. The main disadvantage of monolithic techniques is that great confidence in the performance of the initial circuit design is required since slight changes are difficult to make subsequently. The incorporation of active tuning devices (varactors) in the monolithic circuit may help to effect such alterations, but probably only as a method for fine-tuning the performance.

Other techniques to minimise the circuit losses may include the subsequent removal of much of the lossy substrate material by etching. This etching could take place once the circuit has been mounted in the waveguide and the plated metal tracks of the circuit could then be almost self-supporting.

In conclusion, the power combining of DBRT devices offers the potential to achieve usable amounts of possibly low-noise sub-millimetre wave power, especially if this can be achieved monolithically.

5.2.5 Noise of DBRT's as oscillators

An important criteria in the acceptability of oscillators and one which possibly favours DBRT devices, is the associated noise of the devices used to generate the power. Fundamental mode operation is usually preferable for an oscillator in that it can help to minimise the overall noise, by removing the need for harmonic up-conversion using extra devices and circuits. The noise figures for "conventional" tunnel devices were found to be 20-30dB lower than the Gunn devices of that time [6] and suggests that oscillators fabricated using DBRT devices should also yield low noise figures. Few examples have been described in the literature on such noise measurements. One such

example is by Demarteau et al [7]. In this example, the noise figure for the DBRT device biased in the active region of the current-voltage characteristic was measured in a reflection amplifier configuration and was found to be 5.5 at the lowest. However, for this example [7] neither the device nor the embedding network were optimised and therefore potential exists for these figures to be improved.

5.3.1 DBRT diode's as harmonic up-converters or multipliers

The low level of fundamental mode power which have been achieved to date using DBRT devices has prompted other groups to investigate the potential of these devices to up-convert a lower frequency signal [8,9,10,11&17]. This lower frequency signal is usually generated using a gunn diode oscillator and it is the higher harmonics which are extracted.

The harmonic oscillator cavities are usually based on either crossed waveguides (where the direction of the guides is perpendicular to one another) or separate waveguides with a coupling network between them. The latter approach permits the optimisation of each cavity-device combination and generally allows more control of the overall multiplier design and leading to enhanced efficiencies[12].

Varactor triplers have been operated to provide 3-4mW at 195-235GHz with an efficiency of around 10% [12]. These results were achieved using a varactor diode with a junction capacitance of 15fF, a series resistance of 9ohms and a reverse breakdown of 15volts. A particular characteristic which favours the use of DBRT devices as multipliers is in the special case of odd harmonic multiplication. The anti-symmetry in the current-voltage characteristic results in the suppression of even harmonics provided that the device is operated at zero bias or at a bias which results in the matching of the anti-symmetry on both sides. Hence, the complicated design of adjacent harmonic idling circuits is much simplified since the second harmonic is absent if the DBRT is used as a tripler.

For comparison with the above results for a varactor diode, DBRT devices have achieved efficiencies of 1.2% (equating to 0.8mW output power) at 250GHz using unoptimised cavities [9]. The results achieved for the devices discussed in this thesis and measured at the university of St. Andrews [4], showed third harmonic operation (for devices from NU-298 and NU-367) giving less than a micro-watt at 255GHz with a 85GHz "pump" power of 20mW, and represent an efficiency of less than 0.005%!

5.3.2 Quantum barrier varactors

The quantum barrier varactor (QBV) [15] seeks to improve upon the DBRT as a multiplier by having a similar anti-symmetric current-voltage characteristic but with a much lower conductance and therefore less lossy. The existing DBRT devices [which were mainly fabricated for use as oscillators] were mainly designed to have high current densities (high conductance). For harmonic multiplication the power dissipated in this high conductance is "lost" to the multiplier and so a very much higher resistance (more reactive) device is needed. This can be achieved using high single barriers rather than double barriers. Rydberg et al [15] describe tripler efficiencies of 5% and output powers of 2mW at 210-280GHz and quintupler efficiencies of 0.2% at 310GHz using a QBV diode.

The main advantage of quantum barrier varactors, as harmonic multipliers in place of conventional schottky diodes, is that the current-voltage characteristic of the QBV's is again anti-symmetric and therefore the production of even harmonics (at zero bias) is suppressed as for a DBRT diode. Also, the "active-junction" of the QBV is buried and therefore it should not suffer from the surface noise contributions and power limitations of the schottky devices. Given time, the QBV will probably replace the schottky diode as a multiplying element, due to the extra degree of control in "tailoring" the impedance of the QBV by the independent use of the barrier height and the emitter and collector doping [16].

5.4 DBRT diodes as harmonic down-converters or mixers

DBRT devices have been used as Mixers and Detectors [18,19,20] where the control of the current-voltage characteristic (especially the effective barrier height via. the well width] and the large degree of asymmetry possible at low bias also favour their use in place of conventional schottky devices. Often in applications where either temperature stability or low-level (and low-noise) detection (at zero applied bias) capabilities are required then the schottky devices are superseded by tunnel diodes. Furthermore, the use of DBRT devices at cryogenic temperatures is straightforward and the current-voltage characteristics can again be easily controlled leading to the possibility of zero-bias low-noise operation.

To the author's knowledge, the use of DBRT devices as sub-millimetre wave mixers and detectors has not been extensively investigated using devices and material specifically grown for the purpose. That is, most of the structures grown to date have been with oscillator applications in mind and in consequence tend to have higher conductances than needed for good mixers or detectors.

5.4.1 DBRT diodes as sub-harmonic mixers

One of the most straightforward applications of DBRT devices would be as a substitute for the special class of devices such as sub-harmonic mixers [19]. In the conventional case two back-to-back schottky diodes are connected in anti-parallel and in this arrangement a sub-harmonic ($F_{L.O}/2$) of the "normal" local-oscillator frequency is required to mix-down the I.F. from the signal. The advantage of this is that in the sub-millimetre frequency range a local-oscillator of only approximately half the signal frequency is required to receive the I.F. Another advantage is in the simplification of the circuit design. That is, the wide frequency separation between the signal, L.O. and I.F. permits simple filtering to prevent their unwanted interaction.

As a result of this anti-parallel arrangement, even harmonics (similar to the case of the multiplier) which are generated by the mixer in response to the L.O., are suppressed. If this were not the case, the resulting harmonics may interfere with the signal. Specifically, the image signal $((2f_{L.O.}-f_{Sig.})+(f_{L.O.}-f_{I.F.}))$ is much reduced since the second harmonic of the L.O. is absent due to the anti-symmetry (of back-to-back schottkies or a DBRT) of the current-voltage characteristic. In real terms, a carrier of ~360GHz could be de-modulated using a sub-harmonic mixer with an L.O. supplied by a InP gunn operated at second harmonic (7mW at 180GHz). As an example Galin [22] quotes figures of 900K double side-band noise temperature at an I.F. of 1GHz and a signal frequency of 183GHz .

The DBRT device offers the potential to simplify circuits using sub-harmonic mixers by replacing the anti-parallel schottky devices with a single DBRT diode. The DBRT device can be operated without need of bias (and therefore associated noise) and in the case of point-contacted devices only one point contact needs to be made, thereby simplifying a difficult process. Also, as a result of the discussion in the preceding paragraph, the DBRT diode operates in an essentially single sideband (SSB) mode due to the lack of significant signal power being received at the image frequency and therefore a complicated (balanced) circuit design is nor required to achieve optimum efficiency. A theoretical analysis has been undertaken by Smith et al [19] which discusses the DBRT parameters (current-voltage) needed to provide optimum system performance.

To date, the only known demonstration of the capabilities of a DBRT device as a sub-harmonic mixer is by Smith [19] and Sollner et al [20] who, using a DBRT, achieved a conversion loss of 12dB for a 50GHz L.O. and a signal of 100GHz, and is comparable to the results of others using back-to-back schottkies[24].

5.4.2 DBRT diodes as self-oscillating mixers

The most promising application of DBRT devices in terms of receivers is as self-oscillating mixers (SOM's). The capability of a DBRT device to produce its own L.O. offers a great advantage, especially at sub-millimetre frequencies, where the provision of an external L.O. would often require harmonic operation of the device producing the L.O. with an attendant increase in device and circuit complexity and expense. Yet another advantage of a SOM is the possibility of conversion gain during the mixing process (rather than the usual conversion loss).

The conversion gain capabilities come about via the NDR of the device at the I.F. Hence, power can be extracted from the d.c. bias circuit and transferred to the I.F. signal leading to the gain observed. Early SOM's using Esaki tunnel diodes are usually referred to as harmonic converters and conversion gains of 15-25dB have been reported [25,&26]. However, achieving optimum embedding impedances at the relevant frequencies and arranging the characteristics of the Esaki tunnel diode to provide conversion gain at an appropriate frequency, is very difficult to achieve. This, together with the limitations in fabricating Esaki tunnel diodes with specific characteristics (which were discussed in Chapter 1) limited their widespread use.

With the degree of control available for fabricating DBRT devices with suitable characteristics, the development of the SOM may see a resurgence. Sollner et al [20] reported a DBRT device operating as a self-oscillating-mixer at 46-48GHz and for a signal frequency of 48.4GHz, with a best conversion gain of 5dB. The results achieved by the present author and collaborators is shown in Figure 5.17(a&b) [27]. At best 4dB of conversion gain was achieved for a 10.9083GHz signal and with the DBRT oscillating at 10.9478GHz. Similar experiments were attempted at W-band, but the lack of optimization resulted in conversion losses in the region of 30dB with a best loss of about 19dB at an I.F. of 1129MHz and using a -26dBm, 85GHz signal [28,29,14].

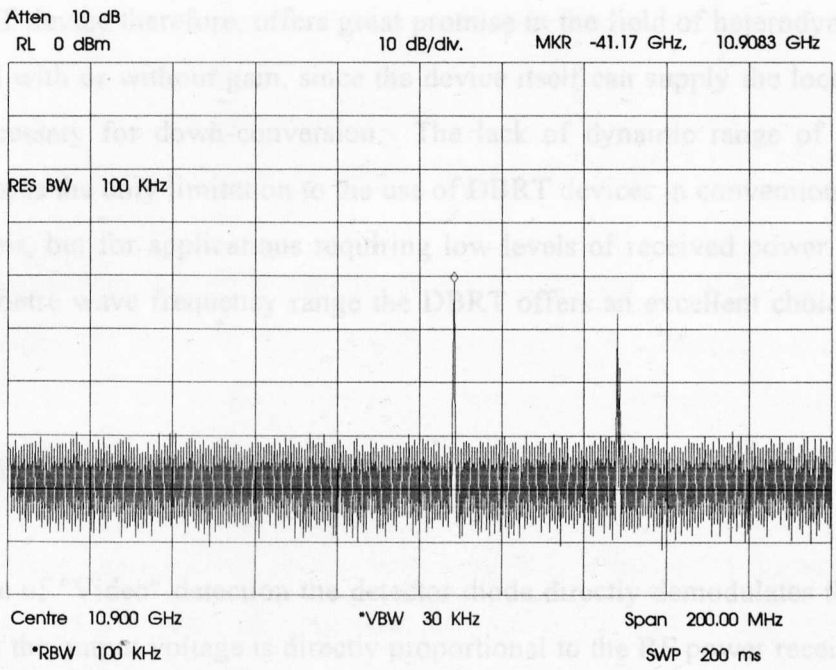


Figure 5.17 (a)

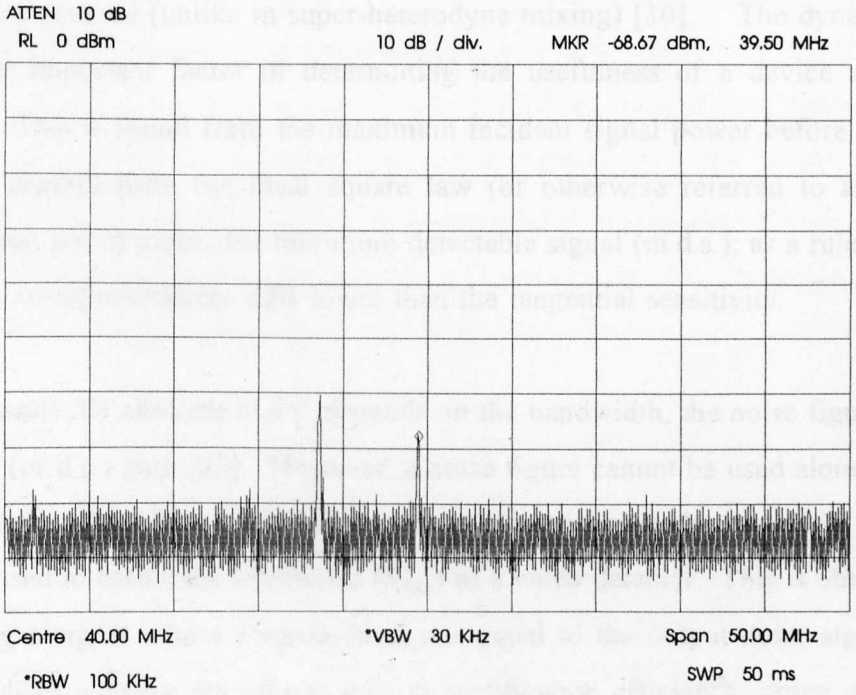


Figure 5.17 (b)

The DBRT device therefore, offers great promise in the field of heterodyne detection as a SOM with or without gain, since the device itself can supply the local oscillator signal necessary for down-conversion. The lack of dynamic range of the present devices poses the only limitation to the use of DBRT devices in conventional RADAR applications, but for applications requiring low levels of received power in the high sub-millimetre wave frequency range the DBRT offers an excellent choice.

5.5 DBRT diodes as detectors

In the case of "Video" detection the detector diode directly demodulates the received signal and the output voltage is directly proportional to the RF power received (ie. the square of the input (signal) voltage); this class of devices is sometimes referred to as square-law detectors. As in the case of mixers, the series resistance and junction capacitance of the devices are first order factors which determine the response of the diode. Likewise, the shape of the current-voltage characteristic is also of primary importance to the performance. The junction capacitance is particularly significant for detection since the rectified current is proportional to the input power divided by the capacitance squared (unlike in super-heterodyne mixing) [30]. The dynamic range is another important factor in determining the usefulness of a device as a video detector. This is found from the maximum incident signal power before the output response departs from the ideal square law (or otherwise referred to as the 1dB compression point) minus the minimum detectable signal (m.d.s.); as a rule-of-thumb the m.d.s. is approximately 4dB lower than the tangential sensitivity.

For a detector the absolute m.d.s. depends on the bandwidth, the noise figure and the RF. to IF (or d.c.) gain [30]. However, a noise figure cannot be used alone to define the sensitivity of a video receiver. Instead, a value known as the tangential sensitivity (TSS) is used to define the sensitivity (S_{TSS}) of a video detector. This is obtained [30] by finding a signal whose magnitude is just equal to the output noise signal of the device (which includes the effects such as rectification efficiency, video impedance,

noise, video amplifier bandwidth and noise figure) in response to a 1 milliwatt input signal. It may be shown that:-

$$S_{TSS} = \frac{1}{\beta Z_v} [4\, Y kT B_v (f_v + N_r - 1)]^{1/2} \qquad (5.1)$$

where: β is the short-circuit current sensitivity ($I_{S.C.}/P_{I/P}$ (ie, $\mu A/\mu W$)), Z_v is the video impedance (dV/dI), B_v is the video amplifier bandwidth, f_v is the video amplifier noise figure, and N_r is the noise temperature ratio of the detector diode. Y is an experimentally determined factor (related to the edge-to-edge height of the noise to its R.M.S. value when displayed on an oscilloscope). For detector applications the ideal current-voltage characteristic is one where there is a maximum curvature in this characteristic at the point of operation; the ability to control the current-voltage characteristic of the DBRT device should therefore favour its use in detector applications.

The use of DBRT diodes as detectors at very high sub-millimetre wave frequencies has been demonstrated by Sollner et al [18]. As a result of these experiments and their agreement with the expression for current responsivity [31], Sollner et al were able to show that the charge transport time through the DBRT structure was less than the period of the incident radiation [ie. $6*10^{-14}$ seconds]. This work demonstrated the capability of DBRT devices to operate up to THz frequencies, and provided strong evidence to support the sequential picture of tunnelling. The results were later reinforced by Chitta et al [32,33] who compared the energy dependence of the FIR radiation in influencing the current-voltage characteristic, and obtained estimates of the sequential tunnelling time from such FIR measurements.

The use of DBRT diodes as detectors was investigated (briefly) at X-band and at W-band. The X-band results were achieved using an experimental set-up at Marconi Electronic Devices Ltd. which was traditionally used to measure the tangential sensitivity of schottky diodes. These diodes had a 7μm diameter active area, with a junction capacitance of around 120fF and a 15μm diameter overlay bond-pad to ease

bonding. For measurement purposes, the devices were mounted in a low capacitance package such as a leadless inductive device (LID) so as to avoid shunting any of the signal past the active region of the device.

The smallest devices available at the time were 20μm in diameter and were fabricated using material from NU-298. Unfortunately, by comparison with the schottky devices the TSS of this DBRT device (which gave the best results of any of the DBRT's) was some 19-25dB higher at -31dBm and when biased at 1mA. The reasons for this poor result were mainly thought to be twofold: the junction capacitance was very much higher (approximately 10 times) than that of a typical schottky, and the current-voltage characteristics were not optimised for detection (ie. symmetric I-V). In fact the current-voltage characteristic for the DBRT from NU-298 was symmetric at about zero volts and as such required a bias to shift the operating point into one or other quadrant of the characteristic in order that any rectification can take place at all. Also, the thinness of the barriers used in NU-298 results in a very low impedance device which again degrades the detection capabilities since the device is poorly matched to the video amplifier which has an input impedance of 250Ω.

These results at X-band were not investigated further either by using smaller devices or improved layer structures because of the time involved in growth and fabrication of specific devices for such studies. A qualitative detector study was also carried out at W-band which simply involved varying the bias applied to a DBRT device when such a device was illuminated at 85GHz in a Flan® mount. As can be seen from Figure 5.18 The effect of the incident radiation is to "smooth-out" the peak and valley excursions of the current-voltage characteristic. This is thought to occur as a result of the rectification of the incident radiation by the shape of the current-voltage characteristic at the operating point. Hence, in the region of the current-voltage characteristic where the current changes rapidly in response to a small shift in applied voltage, the effect of the incident radiation is to "average-out" the characteristic (via. the small a.c. voltage) and so smooth the peak or valley current.

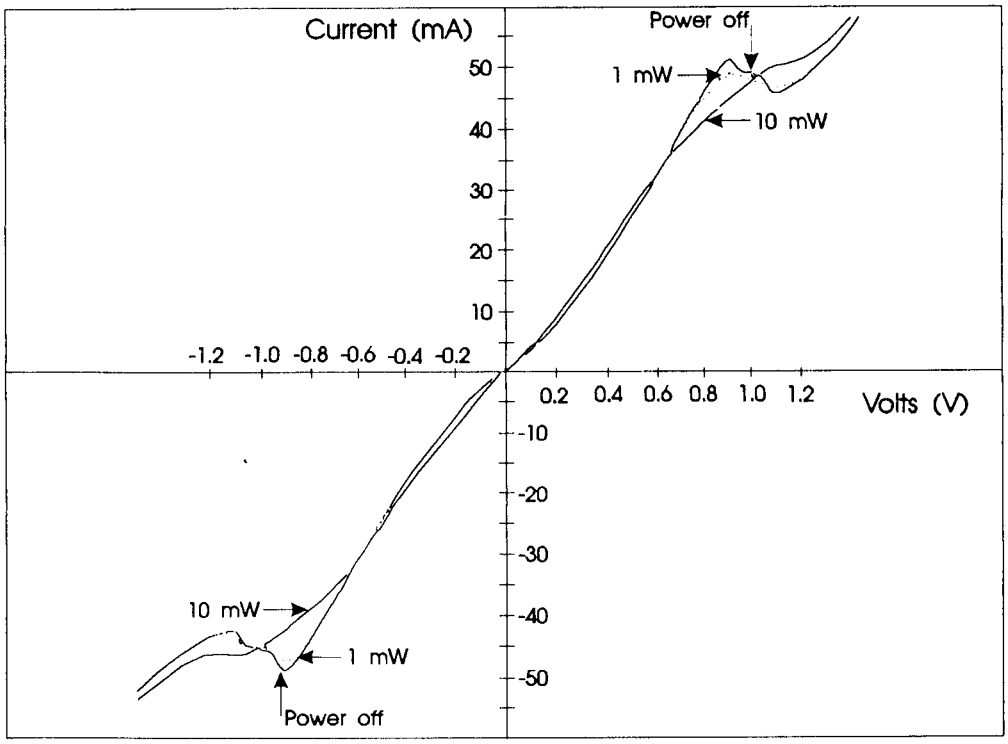


Figure 5.18 Effect of incident radiation (85GHz) power on the current-voltage characteristics of 5μm diameter DBRT device.

Figure 5.18 provides only a qualitative example of detection, but it nevertheless shows that such devices can be used at these frequencies and could perhaps be employed as a tool to optimise the embedding impedance (by giving an indication of the amount of incident power coupled to the device) if the device was not otherwise oscillating.

5.6 Three terminal DBRT devices

The sensitivity of a system to the impedance of a DBRT presents difficulties in system design and optimum operation. The possibility, therefore, of varying the impedance of a DBRT without otherwise affecting its operating point would be of great benefit to the system designer [35,36]. Indeed, this could lead to improved operation of DBRT devices as oscillators where the operation frequency could be "tuned" by varying the gate voltage. To the author's knowledge there have been no applications of such three terminal devices at microwave frequencies. Layers NU-610,NU-614 and NU-636 (A1) were grown to suit three terminal operation. Layer's NU-610 and NU-614 incorporated 4500Å of $1*10^{17}cm^{-3}$ in the collector. This low doped material between the collector barrier and the collector contacts was on top of semi-insulating material and by "gateing" this layer should introduce a variable voltage drop across the collector. Hence, the magnitude of NDR and also the impedance at the operating point should be controllable by using this third "gate" electrode. This variation of impedance, by incorporating what is effectively a field-effect-transistor in the collector of a DBRT, behaves as a lossy element. That is, the impedance is varied by introducing extra series resistance by reducing the cross-section of the collector. Layer NU-636 contained a third barrier (200Å, 20% (Al)) placed 500Å ($1*10^{17}cm^{-3}$) away from the collector barrier of the DBRT. It was intended that the field across the third barrier in the collector and the accompanying depletion region formed on the anode side of this barrier could be varied independently from the field across the DBRT. The result should, in principle, behave in a similar way to a DBRT in series with a quantum-barrier-varactor. That is, the impedance should be variable by changing the reactance of the overall device and should be, in principle, less lossy than using the resistance to affect this change in the impedance. Three terminal devices of this type include the THETA (tunnel injection ballistic transistor), CHINT (charge injection transistor) and the NERFET (negative resistance FET) [14,39,40,41]. Unfortunately, the difficulty in fabricating a three terminal device with sufficiently small dimensions has up to now prevented these structures from being assessed (at the University of

Nottingham) at high frequencies.

5.7 Conclusions

The usefulness of DBRT devices for generating and detecting high frequency millimetre wave radiation has yet to be firmly established, but from the studies mentioned in this thesis and those under investigation by other workers the niche applications of DBRT devices will soon be fully appreciated. The present three-terminal (lateral transport) devices, such as field-effect transistors, exhibit characteristic delays which require ever-reducing dimensions in order to perform at higher frequencies. This, in turn, results in a concomitant reduction in the number of carriers and therefore a frequency/power trade off. However, present pseudomorphic high-mobility electron transistors with nanometre sized gates [34] can in principle perform in the millimetre wave frequency range, although reaching such high frequencies is becoming ever more difficult using this approach. The solution may lie in the use of hetero-junction bipolar transistors or ballistic transistors where the length of the base can be easily controlled to the monolayer scale. Such devices may indeed be similar to DBRT's where the presence of a double barrier at the base-collector interface can provide an important extra degree of control between the emitter and collector. However, as with all (small) perpendicular transport devices the ability to contact the very thin bases is of paramount importance and a factor in determining the frequency of operation of practical devices via. contact resistances and parallel-plate and fringing capacitances.

5.8 References:

[1] Perkins, M. & Pollard, R. (1990). Millimetre-wave vector measurements using multistate reflectometers with diode detectors. *IEEE Int. Microwave Symposium Dig.*, 1037-1040.

[2] Lesurf, J.C.G. (1990). Millimetre-wave Optics, Devices and Systems: A. Hilger. N.Y.

[3] Harvey, A.R. & Lesurf, J.C.G. (1990). A Millimetre wave, single mode, quasi-optical, complex reflectometer operating as a nulling bridge. 15th Int. Conf. IR & MM Waves, Orlando.

[4] Robertson, M.R. (1992). Novel Solid-State MM-Wave Sources. *Ph.D Thesis.* University of St. Andrews.

[5] Sterzer, F. & Nelson, D.E. (1961). Tunnel-diode microwave oscillators. *Proc. IRE*, 744-753.

[6] Watson, H. A. (1969). Microwave semiconductor devices and their circuit applications: McGraw-Hill, N.Y.

[7] Demarteau, J.I.M., Heyker, H.C., Kwaspen, J.J.M., Van De Roer, T.G. & Kaufmann, L.M. (1991). Microwave noise of a DBRT diode over the full bias range. *Electron. Lett.***27**(1), 7-8.

[8] Sollner, T.C.L.G. Brown, E.R. Parker, P.E. & Goodhue, W.D. (1990). High-frequency applications of resonant tunneling devices. Electronic properties of multilayers and low-dimensional semiconductor structures. Ed. J. M. Chamberlain, L. Eaves & J-C Portal. NATO ASI series-b **123**: Plenum, N.Y.

[9] Rydberg, A. & Grönqvist, H. (1989). Quantum-well high-frequency millimetre-wave frequency tripler. *Electron. Lett.* **25**(5), 348-349.

[10] Batelaan P. D. & Frerkin M. A. (1987). Quantum well multipliers. *IEEE Conf. Proc. Infrared and millimetre waves*: Ed. R.J. Temkin, N.Y.

[11] Sammut, C.V. & Cronin, N.J. (1992). Comparison of measured and computed conversion loss from a resonant tunneling device multiplier. *IEEE Microwave and Guided Wave Letters*, **2**(12), 486.

[12] Erickson, N.R. (1982). A Frequency tripler for 230 GHz. *Conf. Proc. European Microwaves*, 288-292.

[13] Gronqvist, H. Rydberg, A. Kollberg, E. (1989). Quantum well oscillators: Study of local oscillator technologies for heterodyne spectroscopy in the 300-100 micron region: Appendix to ESA report 6916/86/NL/PB(SC). Chalmers University of technology, Goteborg, Sweden.

[14] Imamura, K. Muto, S. Yokoyama, N. (1988). Resonant-tunneling hot electron transistors (RHETs) using an InGaAs/In(AlGa)As heterostructure. *Fujitsu Sci. Tech. J.* **24** (1), 54-59.

[15] Kollberg, E. Rydberg, A. (1989). Quantum-barrier-varactor diodes for high-efficiency millimetre-wave multipliers. *Electron. Lett.* **25**(25), 1696-1698.

[16] Kollberg, E. & Rydberg, A. (1989). Quantum-barrier-varactor diodes for high-efficiency millimetre-wave multipliers. *Electron. Lett.* **25**(25), 1696-1698.

[17] Bouregba, R., Lippens, D., Palmateer, L., Bockenhoff, E., Bogey, M., Destombes, J.L. &

Lecluse, A. (1990). Frequency multiplication using resonant tunnelling diode with output at submillimetre wavelengths. *Electron. Lett.* **26**(21), 1804-1805.

[18] Sollner, T.C.L.G., Goodhue, W.D.,Tannenwald, P.E.,Parker, C.D. & Peck, D.D. (1983). Resonant tunneling through quantum wells at frequencies up to 2.5 THz. *Appl. Phys. Lett.* **43**(6), 588-591.

[19] Smith, P.M., Conn, D.R. & Xu, J. (1989). The limits of resonant tunneling diode subharmonic mixer performance. *J. Appl. Phys.* **66**(3), 1454-1458.

[20] Sollner, T.C.L.G., Brown, E.R. & Le, H.Q. (1988). Microwave and millimeter-wave resonant-tunnelling devices. *The Lincoln Laboratory Journal* **1**(1), 89-105.

[21] Liu, H.C. Sollner, T.C.L.G. (1993). High-frequency resonant-tunneling devices, in High-speed heterostructure devices: Semiconductors & Semimetals, Eds. R.A. Kiehl & T.C.L.G. Sollner.

[22] Galin, I. (1987). An improved structure for subharmonically pumped millimeter-wave mixers. *IEEE Conf. Proc.* T5.7, 123-124.

[23] Smith, P.M., Conn, D.R. & Xu, J. (1989). The limits of resonant tunneling diode subharmonic mixer performance. *J. Appl. Phys.* **66**(3), 1454-1458.

[24] Carlson, E.R., Schneider, M.V. & McMaster, T.F. (1978). Subharmonically pumped millimeter wave mixers. *IEEE Microwave Theory & Trans.* **26**(10), 706-715.

[25] Oxley, T.H. (1964). Backward diodes as mixers at microwave frequencies. *J. Electronics & Control.* **17**, 1.

[26] Chang, K.K.N. Heilmeier, G.H. Prager, H.J. (1960). Low-noise tunnel-diode down converter having conversion gain. *Proc. IRE* **48**, 854-858.

[27] Millington, G., Miles, R.E., Pollard, R.D., Steenson, D.P. & Chamberlain, J.M. (1991). A resonant tunnelling diode self-oscillating microwave mixer with conversion gain. *IEEE Microwave & guided wave Lett.* **1**(11), 320-322.

[28] Robinson, M.R. & Lesurf, J.C.G. (1991). Self-oscillating mixing in a double barrier diode at W-band. *Int. J. of Infrared & Millimetre Waves* **12**(12), 1379-1385 .

[29] Millington, G., Miles, R.E., Pollard, R.D., Steenson, D.P. & Chamberlain, J.M. (1993). Millimetre-wave self-oscillating mixers using resonant tunnelling devices. (Submitted).

[30] Oxley, T.H. (1980). Microwave solid-state devices and applications: Eds. D.V. Morgan & M.J. Howes. IEE Microwave summer school, Leeds University.

[31] Torrey, H.C. & Whitmer, C.A. (1948). Crystal Rectifiers: McGraw-Hill N.Y.

[32] Chitta, V.A., de Bekker, R.E.M., Maan, J.C., Hawksworth, S.J., Chamberlain, J.M., Henini, M. & Hill, G. (1992). Far infrared response of double barrier resonant tunnelling structures. *Surface Science* **263**, 227-230.

[33] Chitta, V.A. de Bekker, R.E.M. Maan, J.C. Hawksworth, S.J. Chamberlain, J.M. Henini, M. Hill, G. (1992). Phonon-assisted tunnelling in sequential resonant tunnelling devices. *Semicond. Sci. & Technol.* **7**, 432-435.

[34] Adams, J.A. Thayne, I.G. Taylor, M.R.S. Wilkinson, C.D.W. Beaumont, S.P. Johnson, N.P. Kean, A.H. Stanley, C.R. (1990). Very high frequency performance of nanometre scale GaAs MESFETS. *Electron. Lett.* **26**(14), 1019-1020.

[35] Bonnefoi, A.R., Chow, D.H. & McGill, T.C. (1985). Inverted base-collector tunnel transistors. *Appl. Phys. Lett.* **47**(8), 888-890.

[36] Woodward, T.K. McGill, T.C. Chung, H.F. Burnham, R.D. (1987). Integration of a resonant-tunneling structure with a metal-semiconductor field-effect transistor. *Appl. Phys. Lett.* **51** (19), 1542-1544.

[37] Kerr, A.R. Mattauch, R.J. Grange, J.A. (1977). A new mixer design for 140-220 GHz. *IEEE Trans. Microwave Theory and Tech.*, 399-401.

[38] Gentile, S.P. (1962). Basic theory and application of tunnel diodes: Van Nostrand, Canada.

[39] Luryi, S. (1987). Heterojunction band discontinuities: Physics and device applications. Eds. F. Capasso & G. Margaritondo. Elsevier science, B.V.

[40] Heiblum, M. Thomas, D. I. Knoedler, C. M. & Nathan, M. I. Tunnelling hot-electron transfer amplifier: a hot electron GaAs device with current gain. (1985). *Appl. Phys. Lett.* **47**. 1105-1107.

[41] Heiblum, M. Nathan, M. I. Thomas, D. I. & Knoedler, C. M. Direct observation of ballistic transport in GaAs. (1985). *Phys. Rev. Lett.* **55**. 2200-2204.

[42] Luryi, S., Kastalsky, A., Gossard, A.C. & Hendel, R.H. (1984). Charge injection transistor based on real-space hot-electron transfer. *IEEE Trans. Electron. Devices* **31**(6), 832-839.

[43] Kastalsky, A., Luryi, S., Gossard, A.C. & Hendel, R. (1984). A field-effect transistor with a negative differential resistance. *IEEE Electron. Device Lett.* **5**(2), 57-60.

[44] Kastalsky, A., Kiehl, R.A., Luryi, S., Gossard, A.C. & Hendel, R.H. (1984). Microwave generation in NERFET. *IEEE Electron. Device Lett.* **5**(8), 321-323.

A.1

NU-165

0.5μm, GaAs ($2*10^{18}$)
500Å, GaAs ($5*10^{14}$ / $2*10^{16}$)
25Å, GaAs (U.D.)
55Å, $Al_{0.4}Ga_{0.6}As$ (U.D.)
50Å, GaAs (U.D.)
55Å, $Al_{0.4}Ga_{0.6}As$ (U.D.)
25Å, GaAs (U.D.)
500Å, GaAs ($5*10^{14}$ / $2*10^{16}$)
3μm, GaAs ($2*10^{18}$)
GaAs (S.I.)

NU-234/368

0.3μm, GaAs ($4*10^{18}$)
20Å, GaAs (U.D.)
24Å, $Al_{0.4}Ga_{0.6}As$ (U.D.) * 3 (repeat)
20Å, GaAs (U.D.) * 3 (repeat)
20Å, GaAs ($5*10^{17}$) * 3 (repeat)
20Å, GaAs (U.D.) * 3 (repeat)
38Å, $Al_{0.4}Ga_{0.6}As$ (U.D.)
20Å, GaAs (U.D.) * 3 (repeat)
20Å, GaAs ($5*10^{17}$) * 3 (repeat)
20Å, GaAs (U.D.) *3 (repeat)
24Å, $Al_{0.4}Ga_{0.6}As$ (U.D.) * 3 (repeat)
20Å, GaAs (U.D.)
1.2μm, GaAs ($4*10^{18}$)
0.8μm, GaAs ($4*10^{18}$)
0.2μm, GaAs ($4*10^{18}$)
GaAs (N^+)

NU-365

0.4μm, GaAs ($2*10^{18}$)
500Å, GaAs ($5*10^{17}$)
17Å, GaAs (U.D.)
17Å, AlAs (U.D.) * 3 (repeat)
17Å, GaAs (U.D.) * 3 (repeat)
17Å, GaAs ($5*10^{17}$) * 3 (repeat)
17Å, GaAs (U.D.) * 3 (repeat)
30Å, AlAs (U.D.)
17Å, GaAs (U.D.) * 3 (repeat)
17Å, GaAs ($5*10^{17}$) * 3 (repeat)
17Å, GaAs (U.D.) * 3 (repeat)
17Å, AlAs (U.D.) * 3 (repeat)
17Å, GaAs (U.D.)
500Å, GaAs ($5*10^{17}$)
2μm, GaAs ($2*10^{18}$)
GaAs (N^+)

NU-367

0.4μm, GaAs ($2*10^{18}$)
0.15μm, GaAs ($2*10^{17}$)
17Å, GaAs (U.D.)
17Å, AlAs (U.D.)
42Å, GaAs (U.D.)
17Å, AlAs (U.D.)
17Å, GaAs (U.D.)
0.15μm, GaAs ($2*10^{17}$)
2μm, GaAs ($2*10^{18}$)
GaAs (N^+)

NU-418

0.5μm. GaAs ($2*10^{18}$)
17Å. GaAs (U.D.)
13Å. AlAs (U.D.)
34Å. GaAs (U.D.)
13Å. AlAs (U.D.)
17Å. GaAs (U.D.)
0.1μm. GaAs ($7*10^{15}$)
2μm. GaAs ($2*10^{18}$)

GaAs (N^+)

NU-462

600Å. GaAs ($2*10^{16}$)
0.5μm. GaAs ($2*10^{17}$)
25Å. GaAs (U.D.)
17Å. AlAs (U.D.)
42Å. GaAs (U.D.)
17Å. AlAs (U.D.)
25Å. GaAs (U.D.)
0.4μm. GaAs ($2*10^{17}$)
1μm. GaAs ($1*10^{18}$)

GaAs (N^+)

NU-552

0.4μm. GaAs ($2*10^{18}$)
17Å. GaAs (U.D.)
17Å. AlAs (U.D.)
42Å. GaAs (U.D.)
17Å. AlAs (U.D.)
17Å. GaAs (U.D.)
0.3μm. GaAs ($5*10^{16}$)
2μm. GaAs ($2*10^{18}$)

GaAs (N^+)

NU-606

0.5μm. GaAs ($1*10^{18}$)
0.1μm. GaAs ($1*10^{17}$)
51Å. GaAs (U.D.)
43Å. $Al_{0.4}Ga_{0.6}As$ (U.D.)
51Å. GaAs (U.D.)
43Å. $Al_{0.4}Ga_{0.6}As$ (U.D.)
51Å. GaAs (U.D.)
0.3μm. GaAs ($2*10^{16}$)
0.1μm. GaAs ($1*10^{17}$)
2μm. GaAs ($1*10^{18}$)

GaAs (N^+)

NU-610/614

0.78μm, GaAs ($1*10^{18}$)
0.1μm, GaAs ($1*10^{17}$)
51Å, GaAs (U.D.)
43Å, $Al_{0.4}Ga_{0.6}As$ (U.D.)
51Å, GaAs (U.D.)
43Å, $Al_{0.4}Ga_{0.6}As$ (U.D.)
51Å, GaAs (U.D.)
0.1μm, GaAs ($1*10^{17}$)
0.3μm, GaAs ($1*10^{18}$)
0.45μm, GaAs ($1*10^{17}$)
2μm, GaAs (U.D.)
GaAs (S.I.)

NU-636

0.53μm, GaAs ($2*10^{18}$)
500Å, GaAs ($1*10^{17}$)
17Å, GaAs (U.D.)
17Å, AlAs (U.D.)
43Å, GaAs (U.D.)
17Å, AlAs (U.D.)
17Å, GaAs (U.D.)
500Å, GaAs ($1*10^{17}$)
200Å, $Al_{0.2}Ga_{0.8}As$ (U.D.)
0.4μm, GaAs ($2*10^{17}$)
1μm, GaAs ($2*10^{18}$)
1μm, GaAs (U.D.)
GaAs (S.I.)

A.2

```
      PROGRAM TXDBRTD

C     written by P Steenson to calculate the transmission coefficient of a DBRT
C     initially neglecting bias. and simply calculating for a range of incident energies
C     upto to the barrier tops.


      COMPLEX*16 N11,N12,O11,O12,O21,O22,P11,P12,P21,P22,
     + Q11,Q21,T11,e
      REAL*8 Ei,Me,Mbe,Mw,Mbc,Mc,ke,kbe,kw,kbc,kc,Tx,
     + Einc,mult,a,b,c,d
      REAL*4 Ve,Vbe,Vw,Vbc,Vc,Lw,Lbe,Lbc,m,hbar,fractE,
     + fractC,q,de

      DIMENSION Einc(9001),Tx(9001)
      INTEGER Nl,N,I
      CHARACTER Fname*31
      PARAMETER (m=.91E-30,
     + hbar=1.06E-34,
     + fractE=.99,
     + fractC=.99,
     + temp=290,
     + PI=3.141593,
     + perm=8.85E-12,
     + er=12.5,
     + q=1.6e-19,
     + Nl=7900,
     + de=1E-4)

      Mw=.067
      Me=.067
      Mc=.067
      Mbe=(.083*fractE+.067)
      Mbc=(.083*fractC+.067)
      Vbe=(80*fractE*1E-2)
      Vbc=(80*fractC*1E-2)
      Ve=0
      Vw=0
      Vc=0
      Fname='D:\P_DATA\MODEL\Ttemp.dat'
      Lw=43E-10
      Lbe=17E-10
      Lbc=17E-10
      WRITE (6,300) '********** Program Running **********'

      DO 10 I=1,Nl

         Ei=(Ei+de)
         Einc(I)=Ei
         mult=DSQRT(2*m*q/(hbar*hbar))
         ke=mult*DSQRT(Me*(Ei-Ve))
         kbe=mult*DSQRT(Mbe*(Vbe-Ei))
```

```
        kw=mult*DSQRT(Mw*(Ei-Vw))
        kbc=mult*DSQRT(Mbc*(Vbc-Ei))
        kc=mult*DSQRT(Mc*(Ei-Vc))
C       WRITE (6,100) 'MULT ',mult,' ke ',ke,' kbe ',kbe
C       WRITE (6,100) 'kw ',kw,' kbc ',kbc,' kc ',kc
        a=(kbe*Me)/(ke*Mbe)
        b=(kw*Mbe)/(kbe*Mw)
        c=(kbc*Mw)/(kw*Mbc)
        d=(kc*Mbc)/(kbc*Mc)
        e=DCMPLX(0,kw*Lw)
        N11=DCMPLX(1,a)
        N12=DCMPLX(1,-a)
        O11=EXP(kbe*Lbe)*DCMPLX(1,-b)
        O12=EXP(kbe*Lbe)*DCMPLX(1,b)
        O21=EXP(-kbe*Lbe)*DCMPLX(1,b)
        O22=EXP(-kbe*Lbe)*DCMPLX(1,-b)
        P11=(CDEXP(-e))*(DCMPLX(1,c))
        P12=(CDEXP(-e))*(DCMPLX(1,-c))
        P21=(CDEXP(e))*(DCMPLX(1,-c))
        P22=(CDEXP(e))*(DCMPLX(1,c))
        Q11=EXP(kbc*Lbc)*DCMPLX(1,-d)
        Q21=EXP(-kbc*Lbc)*DCMPLX(1,d)
        T11=(N11*O11+N12*O21)*(P11*Q11+P12*Q21)+
     +      (N11*O12+N12*O22)*(P21*Q11+P22*Q21)
        Tx(I)=16*kc/(ke*((T11)*DCONJG(T11)))
C       WRITE (6,400) ' END OF ITTERATION ',I
10    CONTINUE

      OPEN (UNIT=6, FILE=Fname, STATUS='NEW')

      DO 30 N=1,NI

        WRITE (6,200) 'mV= ',Einc(N),',Tx= ',Tx(N)

30    CONTINUE

      CLOSE (6,STATUS='KEEP')
      WRITE (6,300) 'The data should now be stored'
100   FORMAT(1X,A,E11.4E2,A,E11.4E2,A,E11.4E2)
200   FORMAT(1X,A,E11.4E2,A,E11.4E2)
300   FORMAT(1X,A)
400   FORMAT(1X,A,I4)
      END
```

A.3

PUBLICATIONS TO DATE

1. Zarea, A. Sellai, A. Raven, M.S. Steenson, D.P. Chamberlain, J.M. Henini, M. & Hughes, O.H. (1990). Impedance analysis of GaAs/(AlGa)As resonant tunnel diodes in the NDR region. *Electron. Lett.* **26**, 1522.

2. Zarea, A. Sellai, A. Raven, M.S. Steenson, D.P. Chamberlain, J.M. Henini, M. & Hughes, O.H. (1990). Small signal analysis of resonant tunnel diodes in the bistable mode. *ESSDERC* 90: Ed. W. Eccleston & P.J. Rosser. Adam Hilger, Bristol.

3. Miles, R.E. Millington, G. Pollard, R.D. Steenson, D.P. Chamberlain, J.M. Henini, M. (1991). An accurate equivalent circuit model of resonant tunnel diodes. *Electron. Lett.* **27**, 428.

4. Sellai, A. Zarea, A. Raven, M.S. Steenson, D.P. Chamberlain, J.M. Henini, M. & Hughes, O.H. (1991). Voltage step response of Al(Ga)As/GaAs resonant tunnel diodes. *Superlatt. & Microstruct.* **10**, 63.

5. Sellai, A. Zarea, A. Raven, M.S. Steenson, D.P. Chamberlain, J.M. Henini, M. & Hughes, O.H. (1990). Double barrier resonant tunnel diode three-state logic. *Electron. Lett.* **26**, 61.

6. Millington, G. Miles, R.E. Pollard, R.D. Steenson, D.P. Chamberlain, J.M. (1991). A resonant tunnelling diode self-oscillating mixer with conversion gain. *Microwave & Guided Wave Lett.* **1**, 320.

7. Millington, G. Miles, R.E. Pollard, R.D. Steenson, D.P. Chamberlain, J.M. & Henini, (1993). M. Millimetre-wave self-oscillating mixers using resonant tunnelling devices. *(Awaiting publication)*. European microwaves Conf. Madrid.