The Parallel Resonant DC Link Inverter–A Soft Switching Inverter Topology with PWM Capability

Dipl.–Ing. Markus Krogemann

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List of primary symbols

C_{DS}	drain-source capacitance
C_r	resonant capacitor
δ	duty ratio
$\mathrm{f_{sw}}$	switching frequency
$i_a(t)$	output current in phase a
$i_D(t), i_T(t)$	diode and transistor current
I_i	initial resonant link current
$i_{L_r}(t)$	resonant inductor current
I_o	dc link output current
I_{ox}	future dc link output current
I_p	peak resonant link current
I_r	remaining resonant link current
L_r	resonant inductor
m	modulation index
ω_r	resonant frequency
ω_{ref}	reference frequency
ϕ	phase angle
P_{in}, P_{out}	inverter input and output power
R_D, R_T	forward resistance in diode and transistor
S_a, S_b, S_c	switch state in phase a, b, c
$t_{d(off)}$	turn-off delay time
$t_{d(on)}$	turn-on delay time
t_{fi1}, t_{fi2}	current fall time

t_{fv1}, t_{fv2}	voltage fall time
τ_{hl}	carrier lifetime
T_{j}	junction temperature
T_{min}	minimum vector on-time
t_{pw}	PWM pulse width
$t_{pw_{min}}$	minimum PWM pulse width
T_r	duration of resonant cycle
t_{ri}	current rise time
t_{rv}	voltage rise time
$v_{C_r}(t)$	resonant capacitor voltage
V_{dc}	dc link voltage
$v_{D_{drop}}$	diode forward voltage drop
v_{DS}	drain-source voltage
v_{GS}	gate-source voltage
$V_{GS(th)}$	gate-source threshold voltage
$v_{T_{drop}}$	transistor on-state voltage drop
V_S	dc link voltage
Z_r	resonant circuit characteristic impedance

Abstract

Soft-switching inverters have over the last decade received a lot of attention by researchers owing to the reduction or virtual elimination of switching losses that these circuits can achieve. Possible improvements in EMC performance due to the reduced levels of dv/dt have among other advantages triggered the development of a still growing number of zero-voltage or zero-current switching inverter circuits. More recently, the trend seems to have shifted from continuously resonant systems over to quasi-resonant topologies due to advantages in terms of device stresses and PWM compatibility. In this work, continuously resonant as well as quasi-resonant techniques are reviewed. A quasi-resonant circuit will be implemented in a three-phase PWM inverter system controlled by a network of transputers. It will be examined to which degree the working principle of this Parallel Resonant DC Link (PRDCL) inverter affects the PWM compatibility and a suitable PWM strategy will be presented and implemented. The modified PWM technique shows output quality comparable to standard PWM methods while being fully compatible with the operation of the resonant link. The conversion efficiency and EMC performance of a PWM inverter drive based on the PRDCL circuit will be measured and compared to its hard-switched equivalent. It will be shown that improvements over hard-switching inverters are possible. However, the investigation of the PRDCL PWM inverter also reveals a number of drawbacks which limit the achievable switching frequency and adversely affect the conversion efficiency. Despite the many previous publications these problems have generally been overlooked in the past.

Chapter 1

Introduction

1.1 Introduction

Induction motors with squirrel-cage rotors are found in numerous industrial applications because of their low cost and rugged construction. When induction motors are operated directly from the line voltages, they run at a nearly constant speed, determined by the line voltage frequency and the number of poles in the machine.

Variable speed drives using induction machines therefore require power electronic circuits that are capable of producing sinusoidal voltages of varying frequency and magnitude. The technology most commonly applied to cater for this is to rectify the ac voltages coming from the utility and to supply a matrix of switches that connect the positive and negative rail of the resulting dc voltage in quick alternation to the input phases of the ac machine. This type of inverter circuit is known as voltage source inverter (VSI). Applying adequate modulation techniques, it is possible to create voltages that – in conjunction with inductive loads – lead to phase currents that are approximately sinusoidal.

The quality of this approximation depends mainly on the number of switching actions

that take place during each period of the desired fundamental of the output voltage waveform. The higher this number – ie. the switching frequency – is, the better the output waveform quality will be. Increases in the switching frequency have in the past been achieved through improved semiconductor devices that allow faster turn-on and turn-off processes.

However, since the input to the inverter is a stiff dc voltage supply and the inverter switches are operated in a switch-mode in which they are required to turn on and turn off the entire load current, they are subjected to very high switching stresses and switching power losses. These losses stem from the fact that during switching, the switches are subjected to voltage and current simultaneously – a condition known as "hard-switching". To illustrate the problem consider one leg of a full-bridge dc-dc converter or a dc-ac inverter as shown in Figure 1.1. The load is assumed to be inductive (eg. induction machine).

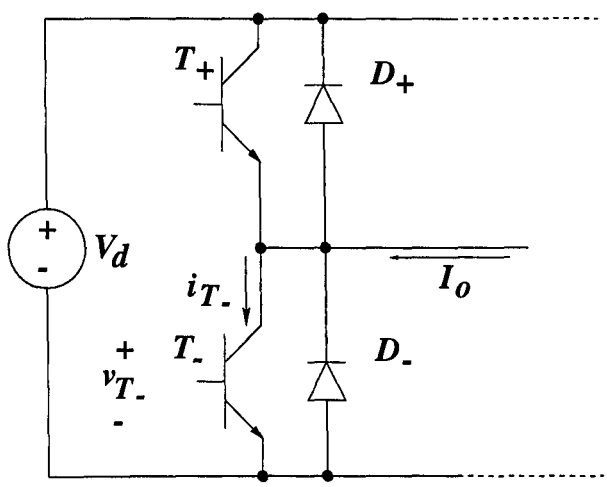

Figure 1.1: One inverter leg.

Due to the load inductance, the output current I_o is regarded as constant for the short switching interval. Figure 1.2a shows the linearised voltage and current waveforms for the lower switch T_-. Initially, T_- is conducting the load current I_o. Upon receiving a control signal to turn T_- off, the switch voltage v_{T_-} increases to V_d plus some overshoot voltage that is due to stray inductances. After that, the current i_{T_-} falls to zero and I_o is carried by D_+. During the turn-off process, the power loss in

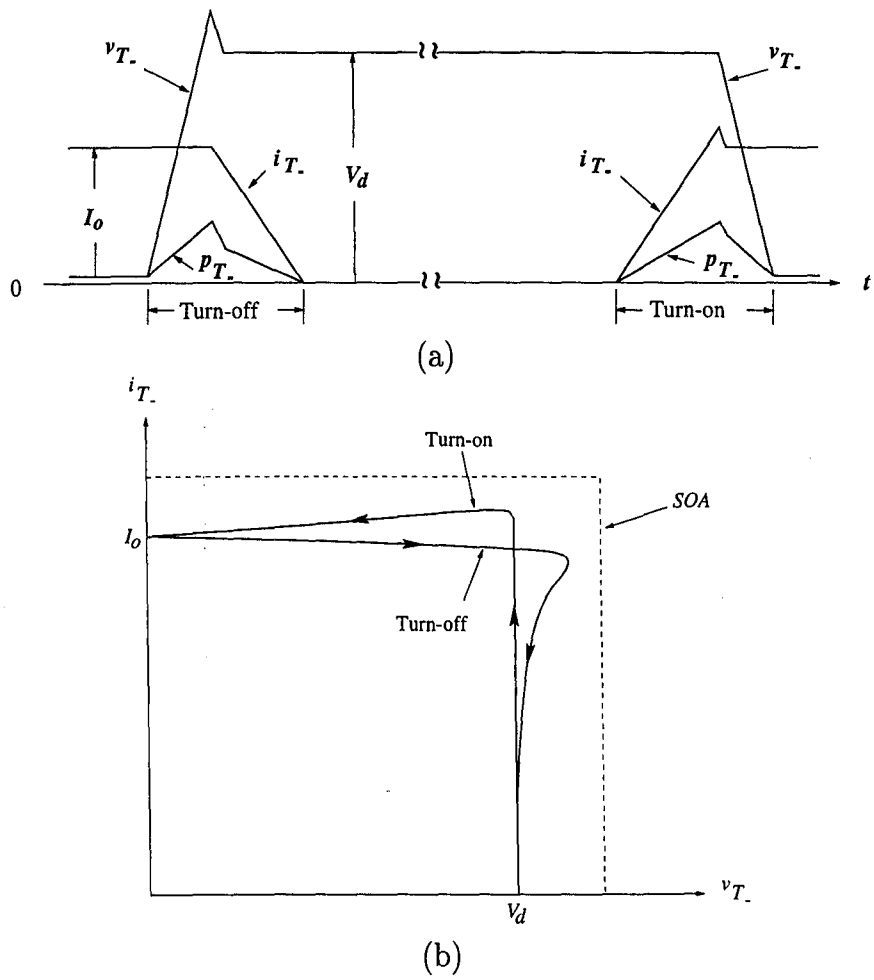

Figure 1.2: Hard-switching of inductive load: (a) voltage and current waveform for turn-on and turn-off; (b) switching loci.

the switch is $p_{T\_} = v_{T\_} i_{T\_}$.

Now consider the case when $T\_$ is to be turned on. Before $T\_$ is turned on, the load current I_o is conducted by D_+. After closing $T\_$, $i_{T\_}$ increases to I_o plus the reverse-recovery current of D_+. The power loss during turn-on is again given by $p_{T\_} = v_{T\_} i_{T\_}$.

The resulting switching loci in the $v_T - i_T$ plane are shown in Figure 1.2b. Due to the simultaneous presence of a large switch voltage and current, the switch has to withstand high switching stresses which must be kept below a safe operating area (SOA) as shown by the dashed lines.

The average power loss that is related to switching increases linearly with the switching frequency. The limiting factor for the switching frequency is the maximum allowable loss in the switching devices. The resulting heat has to be removed from the semiconductor switches to ensure they are operated within their thermal limitations or the switching frequency has to be decreased. Typical commercial designs are therefore found to be thermally limited with switching losses accounting for 30–50% of total device losses [3]. If switching losses could be eliminated this would allow a significant increase of inverter switching frequency and current rating before thermal limitations occur, thus improving device utilisation and power density.

Other significant drawbacks of the switch-mode operation used in inverters are the high levels of dv/dt and di/dt that are due to fast switching transitions required to keep the switching losses in the switch as low as possible. These are a major source of conducted and radiated electro-magnetic interference (EMI). The high levels of dv/dt at the output terminals can also lead to insulation problems in machines.

In order to achieve good output current quality, a good transient response, low acoustic noise and high power density, it is necessary to use high switching frequencies. Higher switching frequencies however can only be realized if the problems of switch

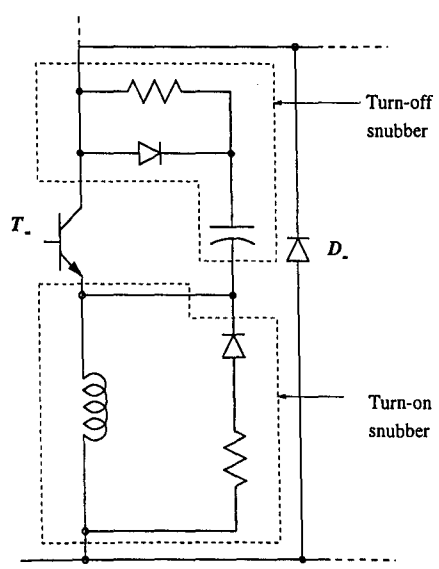

Figure 1.3: Lower half of inverter leg with turn-on and turn-off snubbers.

stresses, switching losses and the EMI associated with switch-mode converters can be

overcome.

The switch stresses can be reduced by connecting dissipative snubber circuits, consisting of diodes and passive components, to the switches as shown for the lower half of an inverter leg in Figure 1.3. However, the application of snubbers merely shifts the switching power loss from the switch to the snubber circuit and does not provide a reduction in the overall switching power loss. Figure 1.4 shows the resulting switching loci for hard-switching of an inductive load with snubber circuits applied.

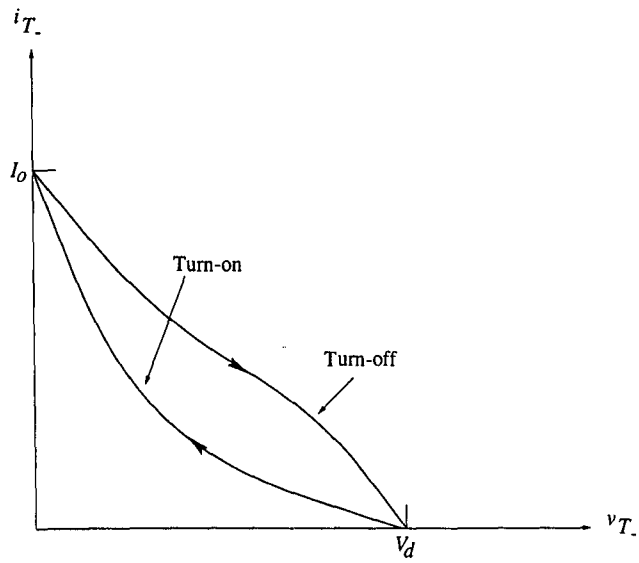

Figure 1.4: Switching loci for hard-switching with snubbers.

To realize high switching frequencies in converters, the aforementioned problems are avoided if each switch in a converter changes its status only when the voltage across it and/or the current through it is zero at the switching instant. Such a switching condition is known as "soft-switching" and can be achieved as a result of a combination of proper converter topologies and switching strategies.

To provide for either a zero voltage or zero current condition (or both), most soft-switching inverters apply some form of resonant LC network between the ac/dc and dc/ac sides of a converter circuit and are therefore broadly classified as "resonant converters." This LC network is used to resonate either the current in the devices or the voltage across the devices to zero for long enough to allow soft turn-off and turn-

on of all devices that require a status change. The dv/dt and di/dt in the devices is therefore limited by the resonant tank components and can be greatly reduced compared with the hard-switched case.

Figure 1.5 shows switching loci for the case that both turn-on and turn-off occur under soft-switching conditions. Switching loci for the hard-switched case are shown as dashed curves to allow comparison.

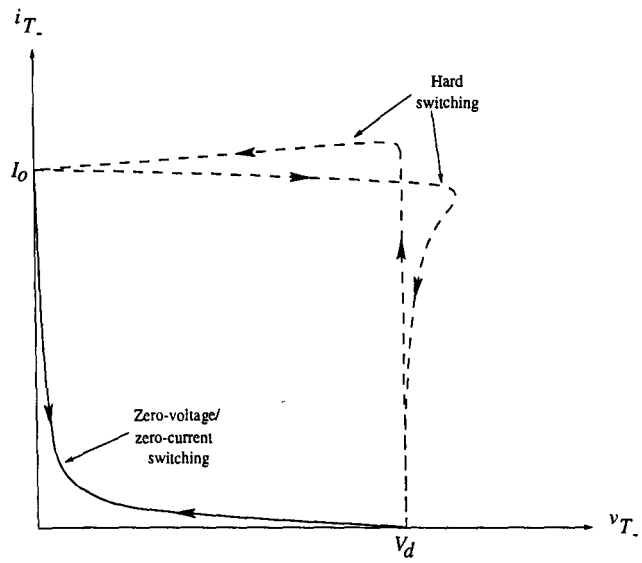

Figure 1.5: Trajectories for zero-voltage/zero-current switching.

Due to the reduction of switching losses that can be achieved, soft-switching inverter topologies have over the past ten years gained increasing interest by researchers. As a result, increases in switching frequency seem to be possible by applying new inverter topologies and switching strategies rather than as a consequence of improved semiconductor materials. Soft-switching topologies possess a number of inherent advantages over hard-switching topologies that are realized to varying degrees in the many approaches presented so far. They include:

- reduction of switching losses down to virtual elimination
- possibility of increased switching frequencies allowing smaller filter components
- reduced device cooling requirements leading to

- reduced size/cost and better device utilisation
- low dv/dt or di/dt leading to
- less electromagnetic emission and
- reduced audible noise

It is expected that new legislations in the field of electro-magnetic compatibility (EMC) will require products with improved filter circuits in order to meet the specifications. Soft-switching inverters are regarded as an alternative solution to avoid EMI and it is therefore expected that they will receive a lot of attention with regard to EMC regulations.

The aim of this project is to analyse whether soft-switching technologies can achieve the above mentioned benefits in a realistic design example. This analysis will be done by means of an experimental three-phase prototype inverter. Any advantages gained will be evaluated against the increase in complexity that is required to achieve them. In addition to that, research work will be carried out to develop and implement suitable modulation strategies for soft-switching inverters and compare their performance to well established modulation techniques used in conventional hard-switched inverters.

It is found that while improvements over hard-switching inverters are possible in some areas, the PRDCL PWM inverter also reveals a number of drawbacks which limit the benefits that can be achieved. These drawbacks adversely affect the conversion efficiency and restrict the maximum switching frequency. Some of the problems found with the PRDCL inverter have been overlooked in previous publications.

1.2 Structure of this work

The remainder of this thesis is subdivided into the following chapters:

- Chapter 2 will introduce a number of soft-switching topologies and highlight their respective merits and shortcomings.
- A more detailed analysis of a particular type of soft-switching inverter topology will be carried out in Chapter 3. The construction of a three-phase transputer-controlled experimental prototype is also described in this chapter.
- The impact of the operational characteristics of soft-switching inverters on applicable modulation strategies will be addressed in Chapter 4. For the topologies discussed in Chapter 3, a suitable modulation strategy is developed and analysed.
- In Chapter 5, an analytical examination of the overall losses of the verified soft-switching inverter is given.
- Chapter 6 contains experimental results of the three-phase prototype inverter.
- Finally, in Chapter 7, conclusions are drawn from the present work and an outlook on the problems that remain to be solved in future work is given.

Chapter 2

Soft-switching inverters

2.1 Introduction

This chapter will give a short review of work that was previously carried out in the field of soft-switching inverters. The following sections will introduce a number of topologies and highlight their respective merits and shortcomings. Consequences of the various circuits for suitable modulation techniques will be pointed out and this was used among other criteria to decide which topology was to be implemented in a prototype inverter.

To explain the operation of the different circuits, we will use the following classification, to distinguish between the two main approaches:

1. Continuously resonant systems, in which the LC network is permanently in resonance and

2. Discontinuously resonant systems, in which a resonant transition is initiated only when required, ie. when the modulation strategy demands reconfiguration of the inverter switch matrix.

2.2 Continuously resonant systems

The majority of resonant systems in the past have been continuously resonant systems in which an *LC* network that is inserted between the dc and the ac side of a converter is excited to resonate the dc bus voltage or current to zero in a periodic manner [1–7]. The occurrences of these zero voltage or zero current instants allow soft turn-off and turn-on of all inverter devices that require a status change. This family of resonant converters can be sub-classified in resonant ac link schemes and resonant dc link schemes.

Resonant ac link converter. Figure 2.1 shows two types of resonant ac link converters, one employing a parallel-resonant circuit while the other one uses a series-resonant arrangement. The ac resonant circuits lead to link voltages and currents of

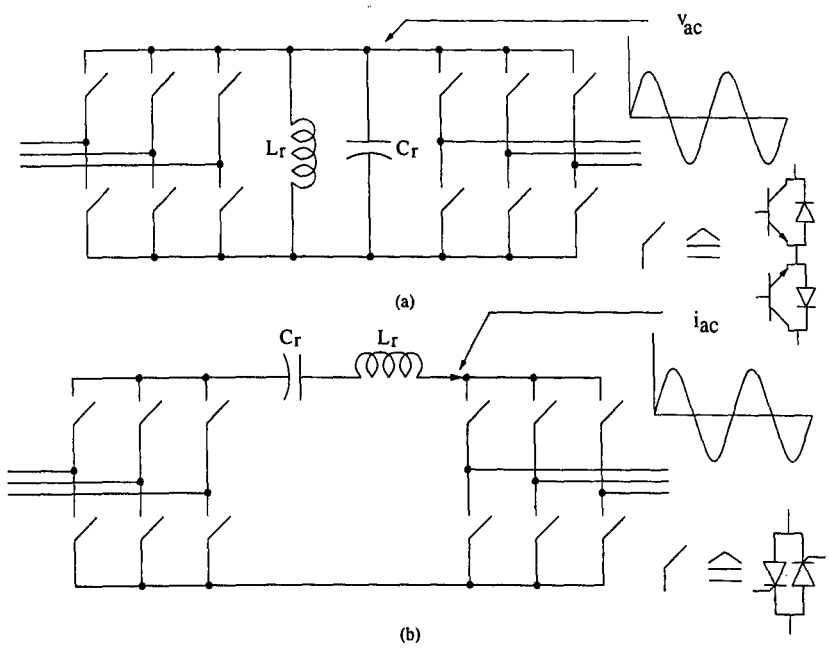

Figure 2.1: Resonant ac link schemes: (a) Parallel-resonant converter; (b) series-resonant converter.

both polarities so that the switches for the input and output side of the converter have to be capable of carrying both positive and negative currents as well as blocking both polarities of voltage. This makes the use of bidirectional switches necessary

which can be realised as shown on the right in Figure 2.1.

In the parallel-resonant circuit, an oscillating voltage is produced across the resonant components which allows zero-voltage switching (ZVS) after each half cycle of the oscillation. In a conventional dc voltage source inverter a large electrolytic capacitor is connected across the dc link that serves as a temporary energy storage to supply fast changing currents drawn from the link. In a resonant ac link converter the circuit element that provides the temporary energy storage is the LC tank, having a much smaller energy storage capacity than the electrolytic capacitor in a conventional voltage source inverter. Any imbalance between output and input current drawn from the link therefore adversely influences the link waveform which leads to distorted output waveforms and device protection problems when the voltage or current peak at levels that are higher than expected. To limit the extent of the link waveform variations, the average input and output powers have to be balanced to maintain constant energy in the link [2].

The series-resonant circuit is excited by the application of a driving voltage across the resonant inductor which leads to a high-frequency sinusoidal current flowing through the resonant components. After each half cycle of the link oscillation, the current has a zero crossing and reverses direction at which instant the switch matrices can be reconfigured as required (zero-current switching, ZCS). Since the current naturally goes through zero, the devices do not need to be self-commutated and thyristors connected in antiparallel can be used to make up the bidirectional switches. One inherent disadvantage of the series-resonant circuit is that the resonant components are in the main power transfer path and thus have to carry the full load current. This leads to significant losses in the resonant tank, particularly in the equivalent series resistance (ESR) of the inductor.

Both ac resonant circuits dictate that all switchings take place at the zero crossings of the link waveforms where the dv/dt or di/dt respectively reach their maximum values. The time available for reconfiguration of the inverter switch matrices is therefore very short and highly accurate timing is required for these circuits. The sampled nature of

the zero-voltage/zero-current occurrences also places restrictions on the modulation strategies that can be used. Since switching is restricted to the zero-crossings of the link waveforms, one half cycle of the link waveform becomes the basic unit from which the output waveform can be synthesised. Discrete modulation patterns have to be used that apply either a negative or positive half cycle of the link waveform to the output phases. These modulation techniques and their consequences on the output waveform quality will be discussed in detail in Chapter 4.

Resonant dc link converter. Two resonant dc link circuits are shown in Figure 2.2. In both circuits the high frequency resonance of the link is offset by a dc

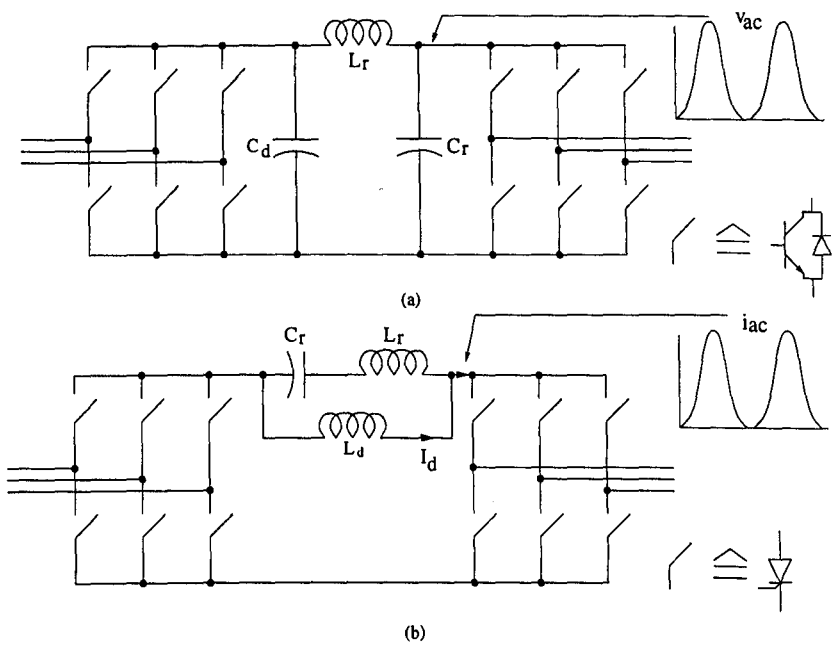

Figure 2.2: Resonant dc link schemes: (a) Parallel-resonant converter; (b) series-resonant converter.

level. While the parallel-resonant circuit is equipped with an additional dc link capacitor C_d that keeps the dc component of the link voltage constant, the series-resonant circuit has an additional choke L_d that carries the dc component of the link current. The link voltage or current do not change their polarity, which means that unidirectional switches are sufficient for these circuits as illustrated in Figure 2.2. In the parallel-resonant dc link circuit, the resonant network is excited by the load side in-

verter by first closing all devices to inject an initial current in the resonant inductor. When this current has been reached, half of the switches are opened and the voltage first resonates to about twice the supply voltage level, then swings back to zero at which point the inverter bridge can be shorted again to inject sufficient magnetic energy for the next cycle. The required initial current has to be controlled to compensate for losses in the resonant tank and the switching devices. It also depends on the present and future load condition which makes current measurement and prediction necessary. The oscillation of the link voltage allows zero-voltage switching (ZVS) of the inverter devices at the zero-voltage periods. However, voltage stresses for the inverter switches result from the resonant action of the LC elements. A dc link resonant cycle is initiated with a fixed value of initial energy in the resonant tank to make sure that the voltage can be brought back to zero under the instantaneous load condition. This requires voltage stresses across the dc link that exceed twice the supply voltage level in steady state operation and can reach more than three times that level in the presence of load transients [3].

The series-resonant dc-link circuit, which is the dual of the parallel-resonant scheme, is excited by pre-charging the resonant capacitor with an initial voltage. This is done by opening all switches in the load side inverter so that the current in the dc link inductor L_d charges the resonant capacitor to its desired voltage. The initial voltage plays the same role as the initial current in the parallel-resonant scheme, ie. to cover the losses in the resonant tank and to inject sufficient energy into the resonant tank to maintain link zero crossings for the following resonant cycle. After the pre-charging, a resonant cycle is started by closing the appropriate switches in the load side inverter. When the link current returns to zero (ZCS), the thyristors in the load side bridge turn off (natural commutation). The resonant capacitor is discharged at this moment and a reverse voltage is therefore applied across all switches. This reverse voltage will then increase with a rate of change that is determined by the dc link current and by the value of the resonant capacitor. The peak current that has to be conducted by the inverter switches is about twice as high as the dc current component. The fact that the current naturally returns to zero and that there is a subsequent period of negative voltage across the dc link means that thyristors can be used for the switching

devices, making this circuit inexpensive in its construction and interesting for high power applications.

Like the resonant ac link circuits, the resonant dc link circuits allow switching only at discrete instants in time. Therefore, a suitable modulation strategy has to be of a discrete nature and the output voltage or current will consist of resonant pulses of varying polarity. The resonance in the two dc resonant schemes is offset by a dc level which makes these circuits very sensitive to losses in the LC tank. If insufficient energy is injected into the resonant tank to overcome all losses, the zero-voltage/current instants will be lost and soft-switching becomes impossible. Unlike the resonant ac schemes, the possible switching instants do not occur at maximum dv/dt or di/dt so that more time is available for reconfiguration of the inverter switches. Exactly how long the zero voltage or zero current condition exists depends on how long the inverter bridge remains shorted or open respectively to inject energy into the resonant tank for the next cycle.

Actively clamped resonant dc link inverter A way of reducing the voltage stresses in the resonant dc link inverter with the help of an additional branch in the circuit (clamp) has been described in [3]. This branch consists of a clamp capacitor C_C, precharged to the desired clamp level minus the supply voltage and an additional switch S_7 with an antiparallel diode. This extra branch allows reduction of the voltage stress to K times the supply voltage where $2 > K > 1$. The actively clamped resonant dc link inverter (ACRDCLI) is therefore regarded as potentially the most promising inverter type within the class of continuously resonant dc link inverters. A simplified circuit diagram for this topology is shown in Figure 2.3.

The ACRDCLI is operated as follows: Initially, the dc bus is shorted by closing all inverter switches to inject magnetic energy into the resonant inductor. When the short is released, the link voltage resonates towards its natural peak. As soon as it reaches KV_S, the clamp diode starts conducting thus limiting the bus voltage. The clamp switch can then be turned on under zero voltage and will eventually take over

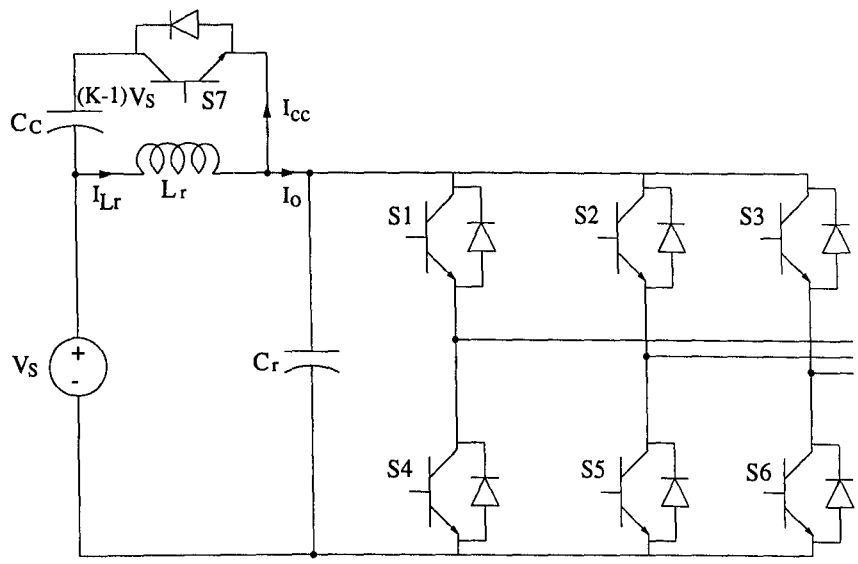

Figure 2.3: Circuit schematic of an actively clamped resonant dc link inverter.

conduction from the clamp diode. The charge that has been transferred to the clamp capacitor is now recovered. When the net charge is zero, the clamp switch is turned off again and the LC tank completes its resonant cycle back to zero volts.

The reduction in voltage stress however leads to a decrease in link switching frequency down to zero for $K = 1$ [3]. Thus, a lower limit exits below which clamping is not practical.

Research results indicate that the working principle can be applied over a wide range of power ratings [7] and that link frequencies – ie. switching frequencies – of 60 kHz are feasible using IGBT switching devices [5].

As was the case for the other continuously resonant circuits, zero voltage periods occur at fixed instants so that switching of the inverter matrix is only possible at these predefined points in time. As will be shown in Chapter 4, this has undesirable consequences on the output current quality. As a conclusion from this, research activities have been undertaken that led to the development of discontinuously resonant systems. The aim of this is to be able to create zero-voltage instants on demand in order to overcome the restrictions placed on inverter switching by the continuously resonant systems. Some of these systems are explained in the following sections.

2.3 Discontinuously resonant systems

As mentioned in the previous section, many soft-switching systems employ a resonant link that reduces the link voltage to zero at periodic instants and thus restrict inverter switching to these instants.

However, some more recent research has been focused on the development of discontinuously resonant systems in order to overcome this drawback [15–23]. The underlying idea is to resonate the dc link voltage to zero only on demand, ie. when switching of the inverter devices is required. One such development is the Resonant Pole converter [3] that is presented in the following section.

More recent developments have introduced not only a resonant LC circuit but also a varying number of additional switches in the resonant link in order to allow initiation of a resonant cycle at any desired point in time [17–21]. Two parallel resonant circuits that employ this working principle will be introduced in Section 2.3.2.

2.3.1 Resonant pole inverter

Figure 2.4a shows a schematic of a single-phase resonant pole circuit. The two devices S_1 and S_2 are configured in an inverter pole together with a resonant LC tank to provide zero-voltage switching conditions for both devices. The operation of the circuit is as follows: soft-switching implies that at device turn-on the antiparallel diode is conducting. Therefore, switch S_1 is kept on until the current i_L reaches a positive reference value I_p. At this point, S_1 is turned off and the current is transferred to the capacitor C_R. The resonant pole voltage V_m resonates to the negative supply rail, thus forcing diode D_2 into conduction. Thus zero-voltage turn-off is provided by the presence of C_R. When D_2 is forward biased, S_2 can be turned on in a lossless manner. While S_2/D_2 conducts, i_L decreases and eventually reaches $-I_p$ at which point S_2 can be turned off and the sequence repeats itself. The relevant waveforms for the resonant pole circuit are shown in Figure 2.4b.

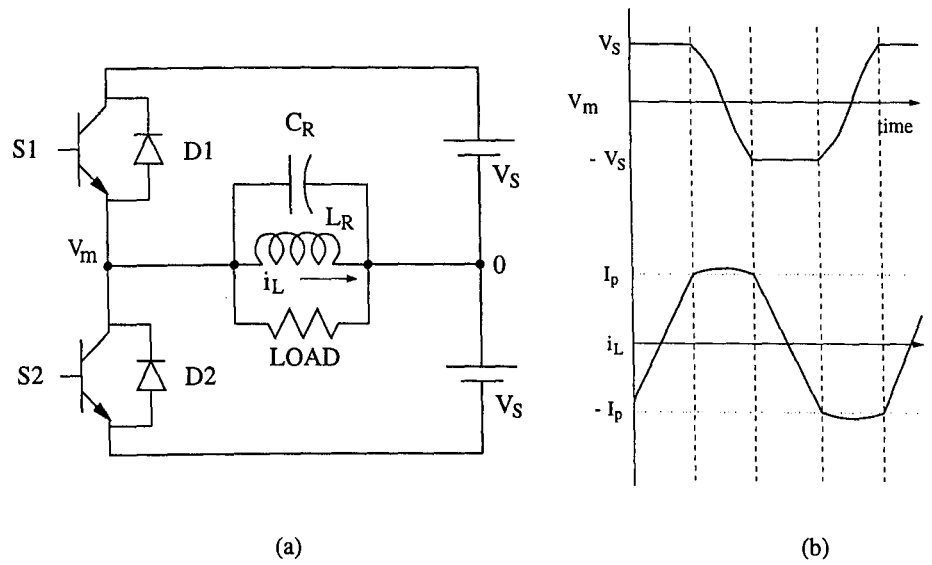

Figure 2.4: (a) Single-phase resonant pole circuit schematic. (b) Pole voltage V_m and inductor current i_L.

To utilise the resonant pole principle for dc/ac conversion, a filter capacitor C_f — which is much greater than the resonant capacitor — is connected in series with the resonant inductor L_R as shown in Figure 2.5. The load is placed across the filter capacitor. In order to produce say a dc voltage V_o across a load resistance R,

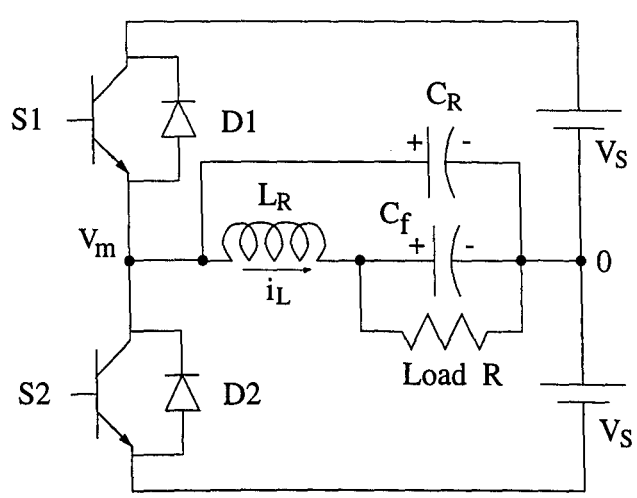

Figure 2.5: Single-phase resonant pole circuit with filter capacitor for dc/ac conversion.

the average inductor current has to equal V_o/R. To generate this average current, the positive and negative trip currents ($\pm I_p$) have to be adjusted accordingly. In a similar way, sinusoidal reference voltages can be created by sinusoidally varying the

trip levels. Figure 2.6 shows a three-phase realisation of the resonant pole inverter (RPI) with filter capacitors $C11 - C33$.

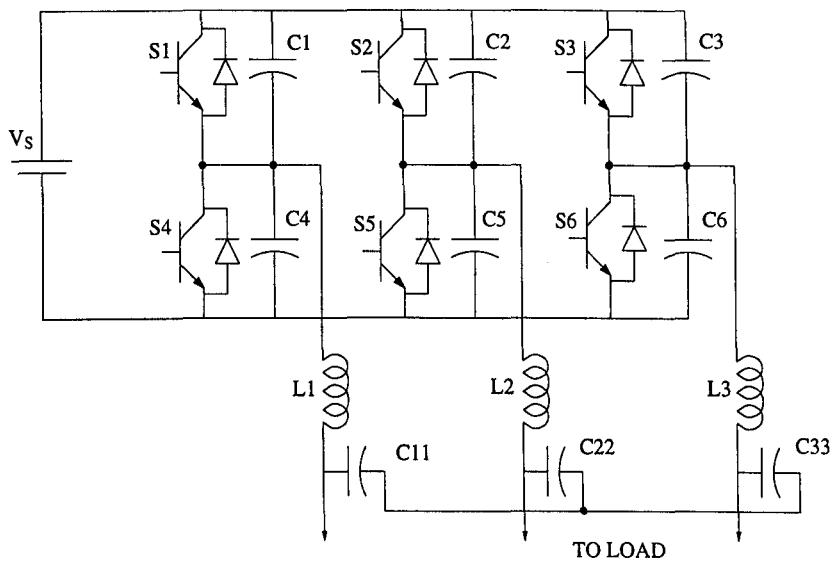

Figure 2.6: Three-phase resonant pole inverter.

Allowable switching instants are constrained by two conditions. Firstly, in order to ensure zero-voltage switching, it is necessary that current is flowing in the switch to be turned off. Secondly, the magnitude of this current has to be sufficient to resonate the pole voltage to the opposite supply voltage rail so that the antiparallel diode of the switch that is to be turned on takes over conduction before the switch receives its turn-on signal.

A performance limiting constraint of the system is that the switching frequency varies with the output voltage V_o. In [3] it was shown that for a given load current, as V_o varies from zero to 0.8 V_S, the switching frequency varies from its maximum f_{max} to 0.36 f_{max}. At maximum output voltage ($V_o = V_S$) the switching frequency reaches zero. Hence, the maximum obtainable modulation index is limited by the minimum acceptable switching frequency. For a sinusoidally varying reference voltage, the switching frequency would sweep from a maximum at the zero crossing of the reference voltage to a minimum at the peak output voltage.

Another disadvantage of the RPI is that it requires high quality filter capacitors.

While for UPS applications, filters are required anyway, this adds additional costs when used in drive applications. Another drawback is that the resonant components have to be selected specifically for a given load.

2.3.2 Parallel resonant dc link inverter (PRDCL)

A number of discontinuously resonant link circuits employing a parallel resonant link arrangement in conjunction with additional switches have been reported in the literature [16–18, 20, 21]. These have in common that the resonant link is only active when the bus voltage has to be reduced to zero in order to commutate the inverter switches. Figure 2.7 shows two such parallel resonant dc link inverter circuits.

Both circuits apply the same basic idea. The resonant inductor is precharged with an initial current. Then, switch S_1 is opened which separates the rectifier side from the inverter side. The energy stored in the resonant inductor then leads to the discharge of the resonant capacitor (C_2 and C_R respectively) so that the voltage across the link is brought down to zero. After the inverter switch matrix has been reconfigured, the resonant capacitor is recharged to supply voltage level with the energy stored in the resonant inductor and S_1 is closed again. The cycle is initiated by closing S_2 and S_3 and can be started at any desired time. The inverter switchings are therefore not restricted to periodically occurring zero voltage instants but can be performed whenever the modulation strategy dictates it.

A more detailed discussion of the operation of the two circuits will be given in Chapter 3. However, two distinct advantages can be identified at this stage.

- The voltage across the dc link is resonated from supply voltage level down to zero and back to the supply voltage again. Hence, the voltage stress for the inverter devices never exceeds the supply voltage.
- A resonant cycle can be initiated at any time which enables inverter switching at any desired instant.

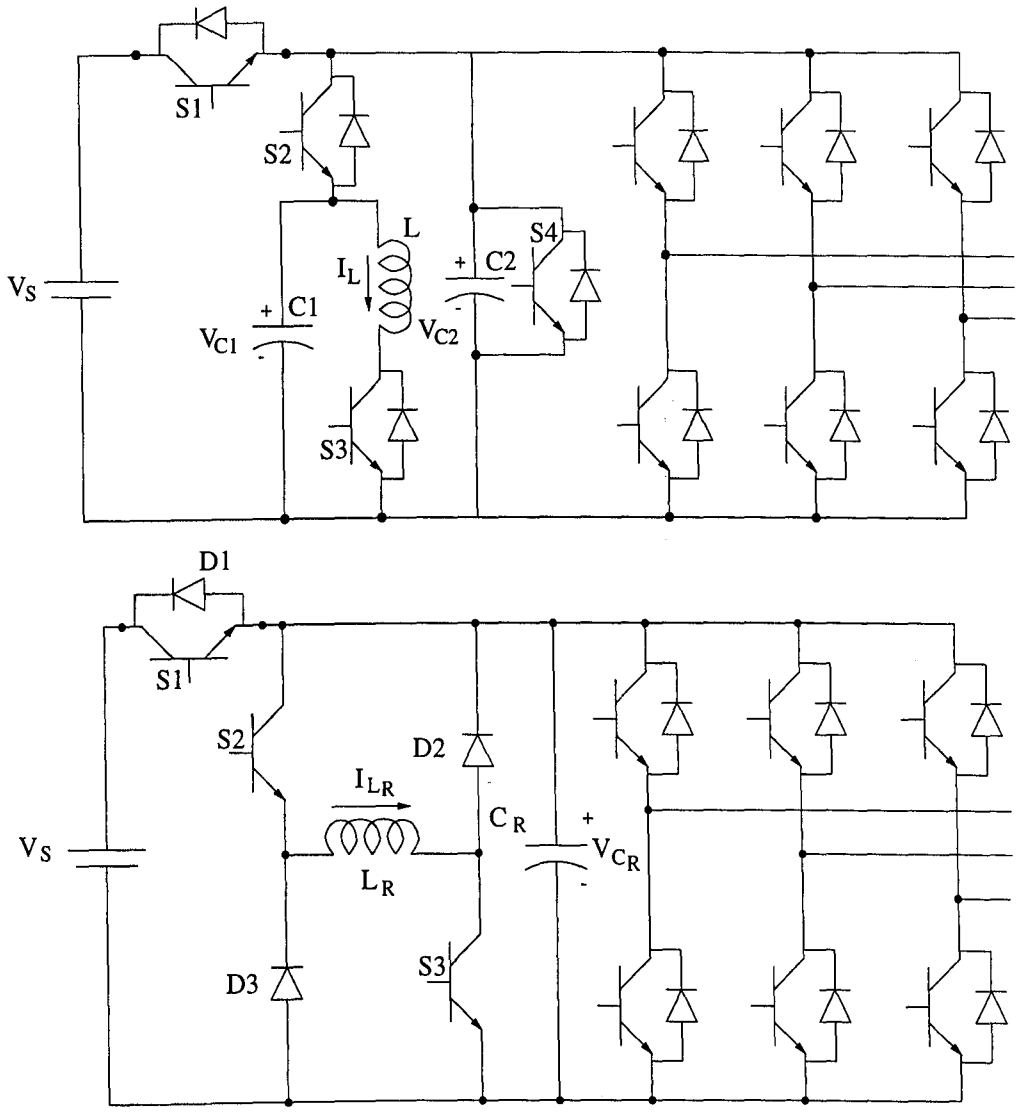

Figure 2.7: Circuit schematics of two discontinuously resonant parallel resonant dc link inverters.

2.4 Summary

A number of soft-switching circuits have been introduced and their respective merits and shortcomings have been pointed out. A list of the major advantages and disadvantages of each approach is given in Table 2.1 on the following page.

In order to achieve good output current quality, modern inverters apply modulation techniques that require high accuracy in the timing of the inverter switchings.

Principle	Inverter circuit	Advantages	Disadvantages
Continuously resonant	Parallel resonant ac link		Inverter switching constrained to link zero crossings when dv/dt is at maximum. Bidirectional switches required. Average input and output power have to be balanced.
	Series resonant ac link	Switching at zero-current crossings allows use of thyristors.	Resonant tank components lie in main power transfer path. Inverter switching constrained to link zero crossings when di/dt is at maximum. Bidirectional switches required.
	Parallel resonant dc link		High voltage stress for inverter devices. Inverter switching restricted to periodic instants.
	Series resonant dc link	Thyristors can be used as switching devices.	Inverter devices have to carry high currents. Inverter switching restricted to periodic instants.
	Actively clamped resonant dc link	Voltage stress reduced to less than $2V_S$.	Inverter switching restricted to periodic instants. Clamping reduces the resonant/switching frequency. Additional switch required.
Discontinuously resonant	Resonant pole	Commutations are not restricted to periodic instants. Independent commutation of each output phase.	Switching frequency decreases with increasing modulation. Expensive filter capacitors required. Resonant tank components are load dependent
	Parallel resonant dc link	No additional voltage stress for inverter devices. Unconstrained inverter switching.	Additional switches required.

Table 2.1: Advantages and drawbacks of soft-switching topologies.

Continuously resonant systems would not allow the application of such modulation strategies since the switching is confined to the periodic occurrence of zero crossings of the link waveforms. The resonant pole inverter suffers from the fact that the switching frequency varies with modulation depth and that it requires expensive filters. It was therefore decided to concentrate work on the parallel resonant dc link circuits with discontinuous operation. They do not restrict inverter switching and the inverter devices are not subjected to higher stresses than in a normal, hard-switched voltage source inverter. The following chapter therefore analyses two such circuits in more detail and describes the fabrication of experimental prototypes.

Chapter 3

Parallel resonant dc link inverter

3.1 Introduction

In this chapter, two single-phase, soft-switching prototype inverters will be analysed and their operation verified through simulation and experiment. Both systems apply a parallel resonant dc link to resonate the dc bus voltage down to zero when required by the switching strategy. The first circuit was presented in [17] where the authors claimed that it is capable of providing high-frequency, three-phase dc-ac power conversion. A low power (50W) prototype inverter using MOSFETs as switching devices was presented in a later publication [18].

The second topology was first described in [20]. It was claimed to have minimum voltage stress for all inverter and auxiliary devices, the voltage being limited to the input voltage. Like the first one, it was also found to be able to provide zero-voltage instances when required and of controllable length. This allows the implementation of switching strategies that require accurate pulse positioning. Simulation results for a three-phase system switching at 20kHz were presented.

It will be shown that the second type has a number of advantages over the first circuit,

mainly concerning the timing of the on/off signals for the auxiliary devices. The first type also suffers from high voltage stress for one of the auxiliary devices. Hence it was decided to implement the second circuit in a three-phase prototype inverter.

A description of the construction of this prototype and its transputer control will be given at the end of this chapter.

3.2 PRDCL inverter type I

Figure 3.1 shows the circuit of a Parallel Resonant DC Link Inverter in a simplified manner where the inverter input has been replaced by a current source. This simplification is justified since the duration of a resonant cycle can be made very short with regard to changes in the output currents by appropriate selection of the resonant tank components [17]. Note however, that the value of the inverter input current is bound to take step changes during a transition, ie. after all inverter switches have taken on their new states.

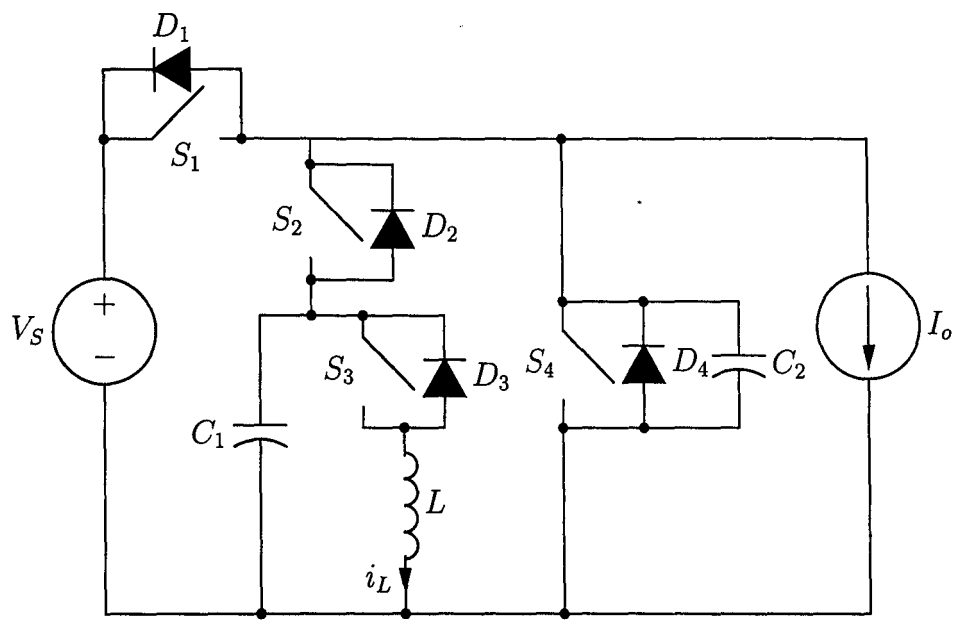

Figure 3.1: Parallel Resonant DC Link Inverter Type I.

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zero at this moment, switching of the inverter switches is not permitted and S_3 is closed instead under zero current condition (ZCS). The current i_L in the inductor then increases linearly until a critical value I_i is reached. The energy stored in the inductor ($\frac{1}{2}LI_i^2$) will have to be sufficient to resonate both C_1 and C_2 back to V_S to complete the resonant cycle. This mode is valid for the interval $[t_0, t_1]$.

When i_L reaches I_i, S_1 can be turned off under zero voltage (ZVS) and the energy stored in L will begin to discharge both C_1 and C_2 in a resonant manner. At t_2, i_L reaches its positive peak value $I_{L,max}$ and both v_{C_1} and v_{C_2} will be zero. S_2 is then opened while S_4 is closed. In this way, the PRDCL circuit is divided into two parts and the voltage v_{C_2} is clamped to zero in order to allow a change of inverter switch position under zero voltage condition. The resonant circuit now consists of L and C_1 and v_{C_1} goes through its negative peak value $-V_{C_1,max}$. At the end of this mode (t_3), i_L reaches its negative maximum value and starts to rise again towards zero. In order to recharge C_1 and C_2 to V_S, switches S_2 and S_4 must change their states again, from open to closed and vice versa. At t_4, while i_L is still negative at a value $-I_q$, both capacitors are recharged to V_S and S_1 can be turned on again under zero voltage. Finally, i_L will go back to zero and S_3 can be turned off with zero current at $t = t_5$. All switches will then remain in their positions until another status change in the PWM inverter will be required.

As can be seen, all additional switches in the PRDCL are operated under zero voltage conditions (ZVS) except switch S_3, which is turned on and off under zero current (ZCS). The delay that occurs between initiation of a resonant cycle and the zero voltage condition as well as the total time needed for completion of one resonant cycle needs to be kept as small as possible. As will be seen in a design example the resonant transition frequency f_r can be made very large compared to the inverter switching frequency f_s by appropriate selection of the resonant devices L, C_1 and C_2.

3.2.2 Waveform analysis

Detailed waveform analysis is performed in [17]. The analysis is based on the following assumptions:

- The resonant inductor is much smaller than the load inductance.
- The inverter input current can be regarded as a constant current source I_o for the duration of a resonant transition.
- All devices and components are ideal and the voltage source V_S is ripple-free.

These assumptions allow us to simplify the circuit for the purpose of analysis to the one shown in Figure 3.1. The quantities of particular interest during the resonant transition are i_L and v_{C_1}. For notational clarity, we let

$$\begin{aligned} \omega_1 &= \frac{1}{\sqrt{LC}} \\ C &= C_1 + C_2 \\ z_0 &= \sqrt{\frac{L}{C}} \end{aligned}$$

For the time interval $[t_0, t_1]$ v_{C_1} will stay at V_S while i_L ramps up linearly with

$$i_L = \frac{V_S}{L}(t - t_0) \tag{3.1}$$

The following interval $[t_1, t_2]$ yields

$$v_{C_1}(t) = -(I_i - I_o)z_0 \sin\omega_1(t - t_1) + V_S \cos\omega_1(t - t_1) \tag{3.2}$$

$$i_L(t) = (I_i + I_o)\cos\omega_1(t - t_1) + \frac{V_S}{z_0}\sin\omega_1(t - t_1) - I_o \tag{3.3}$$

For the interval $[t_2, t_3]$ we have

$$v_{C_1}(t) = -V_{C_1,max}\sin\omega_2(t - t_2) \tag{3.4}$$

$$i_L(t) = I_{L,max}\cos\omega_2(t - t_2) \tag{3.5}$$

where

$$\omega_2 = \frac{1}{\sqrt{LC_1}} \tag{3.6}$$

$$V_{C_1,max} = \omega_2 L I_{L,max} \tag{3.7}$$

$$I_{L,max} = \frac{V_S}{z_o} + I_o \tag{3.8}$$

During $[t_3, t_4]$, the capacitors C_1 and C_2 are recharged and the describing equations are

$$v_{C_1}(t) = (I_{L,max} - I_o) z_o \sin \omega_1 (t - t_3) \tag{3.9}$$

$$i_L(t) = (I_o - I_{L,max}) \cos \omega_1 (t - t_3) - I_o \tag{3.10}$$

The remaining interval $[t_4, t_5]$ consists of v_{C_1} constant at V_S and i_L ramping up linearly to zero again. During the whole cycle, v_{C_2} equals v_{C_1} except for the interval $[t_2, t_3]$ where v_{C_2} is clamped to zero to enable the inverter switches to change to their required states under zero voltage. Note that the duration of this zero voltage period is not determined by the resonant elements but can be specified to allow sufficient dwell time for the inverter switches to change to their desired new states.

The resonant cycle has a transition frequency of

$$f_r = \frac{1}{t_5 - t_0} \tag{3.11}$$

With the results given above, it is possible to derive the waveforms of i_L and v_{C_1} that were given in Figure 3.2.

3.2.3 Design considerations

One design objective is the minimization of $V_{C_1,max}$ as well as $I_{L,max}$ to keep the voltage and current stress of the auxiliary switching devices low. The resonant transition frequency should be as high as possible to allow a high inverter switching frequency and to minimize the duration of the zero voltage notch in the output voltage.

From the results of the previous section it can be seen that it is possible to distribute the device stresses in the resonant circuit through choice of the characteristic impedance z_0. A compromise situation in which $z_0 = V_S/I_o$ gives a maximum value for the resonant current of $I_{L,max} = 2I_o$ and a maximum value for the voltage across C_1 of $V_{C_1,max} = 2V_S$ (Equations 3.7 and 3.8). The maximum current has to be conducted by S_3 and S_2 has to block the maximum voltage. The resulting waveforms for this compromise solution are shown in Figure 3.2. By appropriate selection of the resonant components L, C_1 and C_2 it is possible to yield a different distribution of device stresses, ie. one can either reduce the maximum current stress while increasing the maximum voltage or vice versa. This fact is demonstrated in Figure 3.3, which shows a normalized plot of the maximum capacitor voltage against the maximum inductor current for a fixed resonant frequency. The situation in Figure 3.2 with z_0

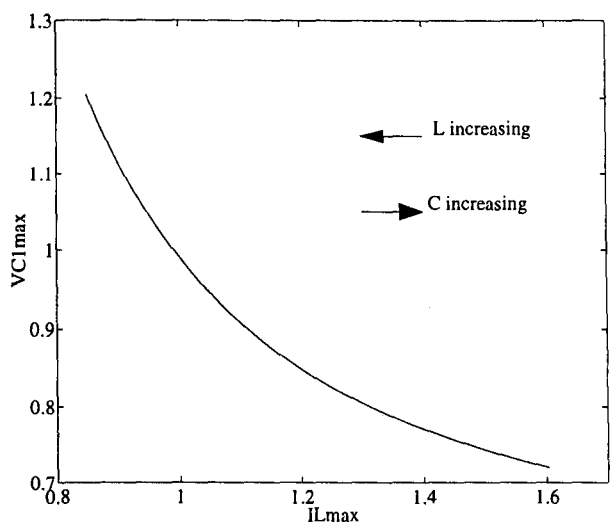


Figure 3.3: Maximum capacitor voltage against maximum inductor current for a fixed resonant frequency with varying L, C_1 and C_2.

as given above has been chosen to normalize the plot in Figure 3.3.

The graph given in Figure 3.4 shows how the maximum voltage and current stresses vary with the value of the characteristic impedance z_0. In this example, C_1 and C_2 are fixed while L is variable. z_0 is normalised with respect to the previously discussed compromise value. Note that the resonant frequency is not fixed in this case.

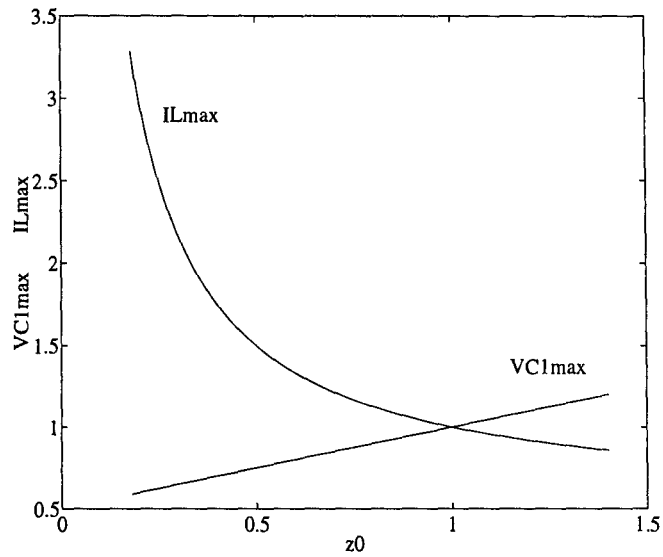


Figure 3.4: $I_{L,max}$ and $v_{C_1,max}$ as functions of z_0. C_1 and C_2 fixed.

Given a desired resonant transition frequency, the equations that were derived and the graphs given in this section can be used to select resonant components which lead to device stresses that lie within the specifications for the switching devices that are to be used.

3.2.4 Simulation results

To validate the theoretically derived equations given above and in order to gain a deeper insight into the behaviour of the resonant circuit, a PSPICE model of the PRDCL inverter was developed, based on the simplified circuit in Figure 3.1. The PSPICE model for an ideal, voltage-controlled switch was used and the switching instants were calculated off-line. The PWM inverter is modeled by a current source whose value changes as a step function from $+I_o$ to $-I_o$ during the first resonant transition. Step changes in the inverter input current will inevitably occur under normal operating conditions and their influence on the behaviour of the resonant circuit has to be examined. Figure 3.5 contains a plot of the inductor current i_L as well as the inverter input current I_o for two successive resonant cycles while Figure 3.6 shows the voltage across C_1. As can be seen in the two plots, the resonant current

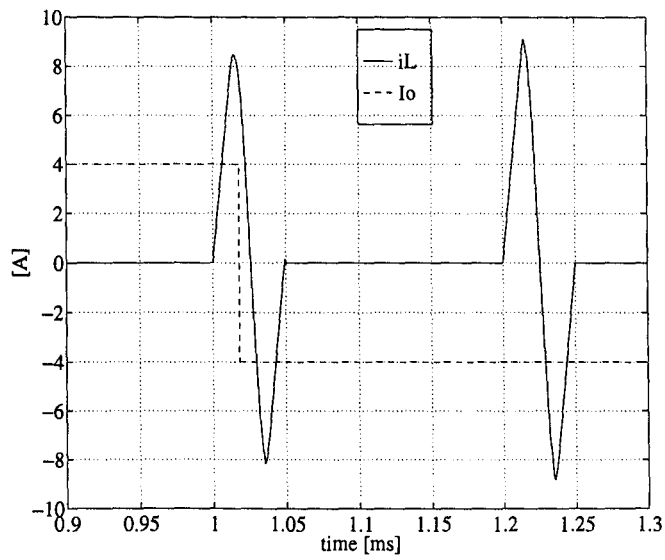


Figure 3.5: PSPICE simulation result for i_L.

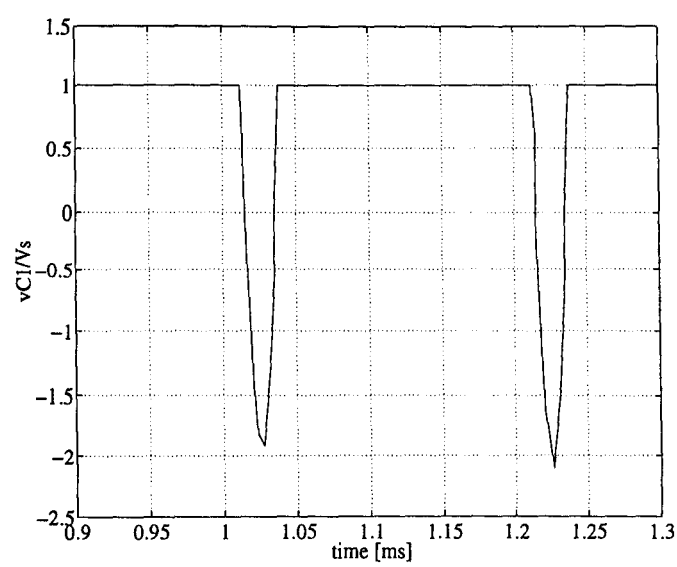


Figure 3.6: PSPICE simulation result for v_{C_1}.

as well as the resonant voltage both have higher peak values in the second resonant transition than in the first. This is due to the reversal of inverter input current that takes place during the first resonant cycle. Maintaining the same switching instants in the second cycle means that more energy is transferred to the resonant tank than would be necessary to complete the cycle. A current prediction scheme in the control strategy of the inverter is therefore necessary to ensure resonance is maintained while no more than the necessary magnetic energy is stored in L.

3.2.5 Experimental results of single-phase prototype inverter

To further verify the theoretical results, a prototype of the proposed circuit was built. The switching devices were chosen to be IGBTs rated at 600 V and a continuous current of 13A. The values of the resonant components were $L = 47.5\mu$H, $C_1 = 0.47\mu$F and $C_2 = 0.047\mu$F, yielding a resonant transition frequency of about 32kHz. The control logic for the switching instants of the auxiliary switches S_1 to S_4 was constructed using CMOS-logic gates. The voltage across C_1 and the inductor current i_L are measured and fed into the control circuit. The supply voltage V_S is 70V at a maximum inverter input current of about 1A. The basic operation of the PRDCL inverter is not dependent on the number of inverter legs. Therefore, only one inverter leg was built up and a center-tapped voltage source was chosen. The load consisted of a series connected RL network. Resulting waveforms of the resonant current and dc bus voltage are shown in Figure 3.7. It can be seen that the dc bus voltage resonates to zero and is clamped to that value for about 15 μs. The experimental results agree well with the theoretically predicted behaviour.

Increasing the resonant transition frequency proved to be not a trivial task, mainly because of the rather large number of firing signals that have to be timed with high accuracy. The control logic has to react very accurately and quickly to the zero crossings of v_{C_1}. Any mistiming in the switch signals for S_2 and S_4 leads to loss of energy in the resonant tank which may in turn mean that the link voltage does not resonate back to supply level, thus making soft-switching of S_1 impossible. Another

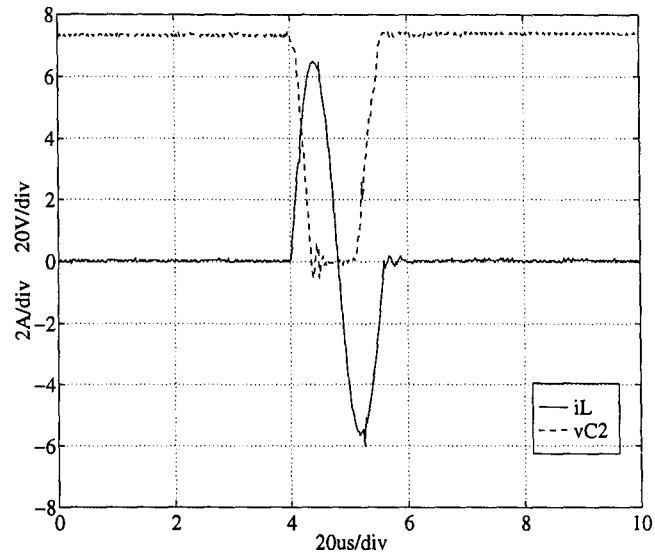


Figure 3.7: DC-link voltage and resonant current of prototype inverter.

drawback of the circuit is the high voltage stress for S_2 that – depending on the resonant tank layout – lies around twice the supply voltage level.

3.3 PRDCL inverter type II

Due to the drawbacks of the first PRDCL scheme, it was decided to investigate a second circuit that operates on a similar principle. Figure 3.8 shows the simplified circuit of this second Parallel Resonant DC Link Inverter. Here again, the inverter input has been replaced by a current source to simplify the analysis.

It will be shown that the diodes D_2 and D_3 conduct the resonant current for a large portion of a resonant cycle. The circuit therefore requires less firing signals for a resonant transition which makes control easier than for the previous system. Also, all additional switches as well as the inverter switches only have to block the supply voltage as compared to about twice the supply voltage level that one auxiliary switch has to block in the first scheme.

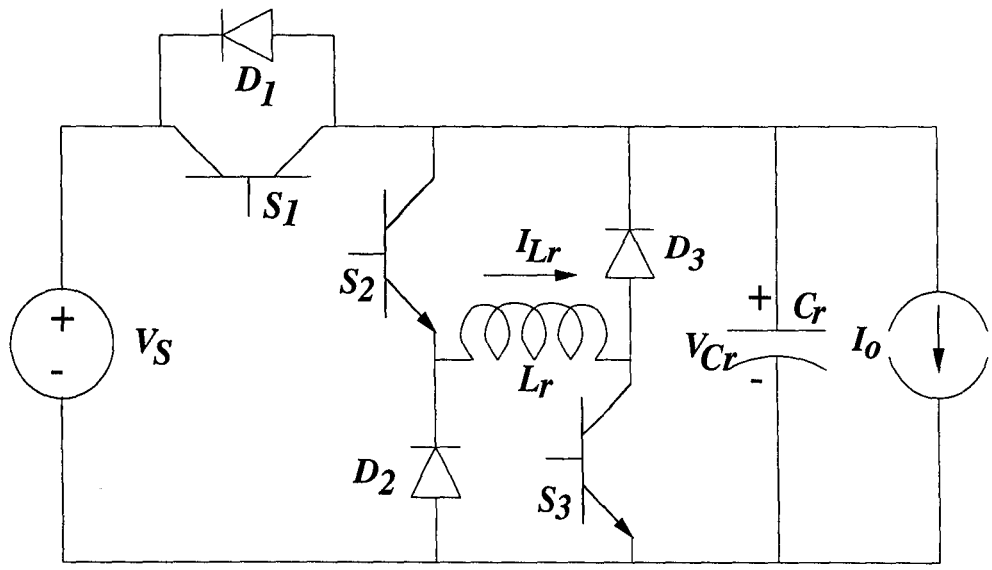


Figure 3.8: Parallel Resonant DC Link Inverter Type II.

3.3.1 Operational Principle

The circuit's operational principle will be explained in a similar way as for the first PRDCL inverter. The assumptions that are made are the same as before:

- The resonant inductor L_r is much smaller than the load inductance.
- The inverter input current can be regarded as a constant current source I_o for the duration of a resonant transition.
- All devices and components are ideal.

Consider the simplified circuit in Figure 3.8: A parallel resonant LC circuit is formed by L_r and C_r. This resonant tank — together with some additional switches (S_1 to S_3) — is inserted between the voltage source V_S and the input of a PWM inverter, modelled by a constant current source. The analysis given here can also be found in [20]. Figure 3.9 contains a plot of the link waveforms for a resonant cycle.

For the analysis of the different modes of operation during one resonant cycle, the system is assumed to be initially (at $t = t_0$) in steady state. At this point, switch

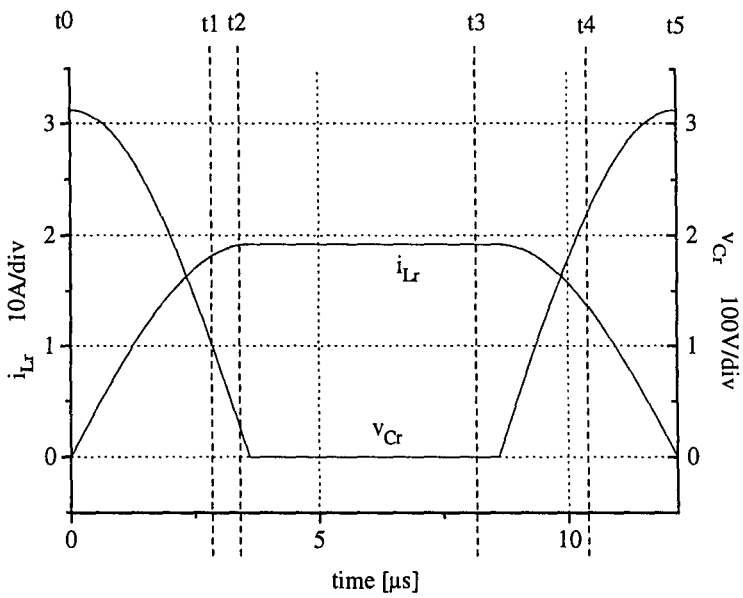


Figure 3.9: Waveforms of i_{L_r} and v_{C_r} at a resonant transition frequency of 82kHz.

S_1 is closed and switches S_2 and S_3 are open, ie. V_S is connected to the input of the PWM inverter. At t_0, the switching strategy may demand a change of state of any of the inverter switches in order to produce a desired output current waveform. The voltage across C_r equals V_S at this time, hence switching of the inverter switches is not permitted and S_2 and S_3 are closed instead under zero current condition (ZCS). The current i_{L_r} in the inductor then increases linearly until a critical value I_i is reached. This initial current will ensure that sufficient energy is stored in L_r to complete the resonant cycle. Its value depends on the present as well as the future output current and has to be predicted in order to control the amount of energy that is stored in L_r. This mode is valid for the interval $[t_0, t_1]$.

When i_{L_r} reaches I_i, S_1 can be turned off under zero voltage (ZVS) and the magnetic energy stored in L_r will begin to discharge C_r in a resonant manner. At t_2, i_{L_r} reaches its positive peak value I_p and v_{C_r} and hence the dc bus voltage are zero. This resonant mode lasts for the interval $[t_1, t_2]$.

At $t = t_2$, the diodes D_2 and D_3 take over the resonant current and the voltage v_{C_r} is clamped to zero in order to allow a change of inverter switch state in a zero voltage

condition. Assuming lossless components, the freewheeling current will remain at its peak value for the duration of this mode $[t_2, t_3]$. The zero voltage time can be chosen to allow sufficient time for all turn-on and turn-off processes in the inverter plus a safety margin to prevent shoot-through of the inverter devices.

To end this mode, S_2 and S_3 are opened again under zero voltage. Resonance between L_r and C_r sets in again and the current now flows through the diodes D_2 and D_3, recharging C_r to V_S. This mode is valid for $[t_3, t_4]$. The current i_{L_r} decreases in a resonant way and some energy (I_r) will remain in the inductor at the end of this mode. At t_4, S_1 can be turned on again with zero voltage and the antiparallel diode D_1 starts conducting.

The remaining energy returns to the voltage source via the diode D_1 with the current decreasing linearly to zero during $[t_4, t_5]$. All switches will then remain in their states until another status change in the PWM inverter is required.

As can be seen, all the additional switches in this PRDCL circuit are actuated in a zero voltage condition (ZVS) except switches S_2 and S_3, which are turned on with zero current (ZCS) but turned off with zero voltage. In comparison with the first PRDCL inverter, less gating signals have to be timed per resonant link cycle. This is due to the fact that the diodes D_2 and D_3 conduct the resonant current for most of the duration of a resonant cycle, thus making control of the PRDCL type II inverter simpler. Another advantage over the first type is that the voltage stress of all additional devices and the inverter devices is limited to supply voltage level.

Figure 3.10 shows the current paths in thick lines for all modes of a resonant transition.

3.3.2 Waveform analysis

For the analysis of the waveforms of interest within the inverter (ie. i_{L_r} and v_{C_r}) the following assumptions are made:

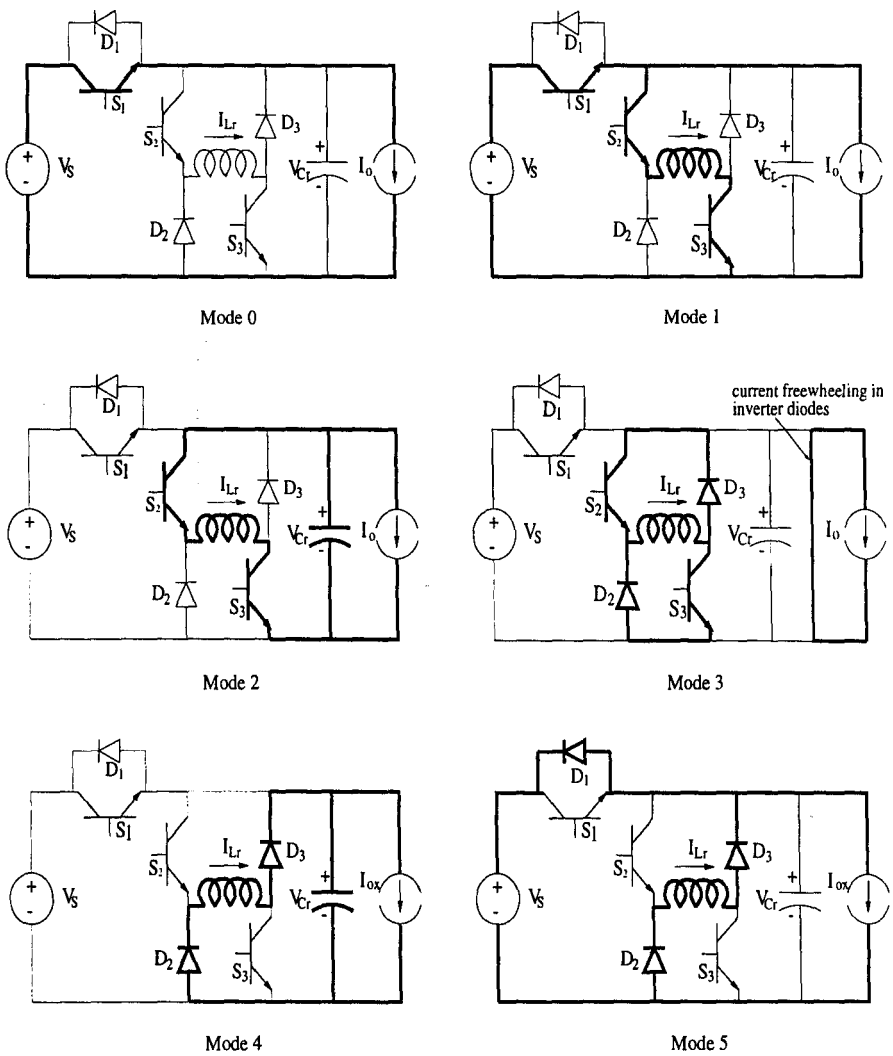


Figure 3.10: Current paths for all modes of a resonant transition.

- The inverter input current does not change appreciably during one resonant cycle.
- The devices and components are ideal and the supply voltage V_S is ripple-free.

These assumptions allow us to simplify the circuit for the purpose of analysis to the one shown in Figure 3.8. Appendix B contains derivations for the equations in this section. We define the following parameters:

1. Resonant frequency, $\omega_r = \frac{1}{\sqrt{L_r C_r}}$
2. Characteristic impedance, $Z_r = \sqrt{\frac{L_r}{C_r}}$

For the time interval $[t_0, t_1]$, v_{C_r} will stay at V_S while i_{L_r} ramps up linearly to the initial value I_i:

$$i_{L_r}(t) = \frac{V_S}{L_r} t \tag{3.12}$$

$$v_{C_r}(t) = V_S \tag{3.13}$$

The duration of this mode is

$$T_1 = \frac{L_r I_i}{V_S}. \tag{3.14}$$

The following interval $[t_1, t_2]$ yields

$$i_{L_r}(t) = \frac{V_S}{Z_r} \sin(\omega_r t) + (I_i + I_o)\cos(\omega_r t) - I_o \tag{3.15}$$

$$v_{C_r}(t) = V_S \cos(\omega_r t) - (I_i + I_o) Z_r \sin(\omega_r t) \tag{3.16}$$

This mode will last for

$$T_2 = \frac{1}{\omega_r} \arctan\left(\frac{V_S}{Z_r(I_i + I_o)}\right) \tag{3.17}$$

At the end of this mode, the inductor current will have reached its peak value I_p that can be obtained from (3.15) as

$$I_p = i_{L_r}(t_2) = \sqrt{(I_i + I_o)^2 + \left(\frac{V_S}{Z_r}\right)^2} - I_o \tag{3.18}$$

For the interval $[t_2, t_3]$ the capacitor voltage is clamped to zero while the resonant current freewheels in a path made up by diodes D_2/D_3 and switches S_2/S_3. The equations for this mode are:

$$i_{L_r}(t) = I_p \tag{3.19}$$

$$v_{C_r}(t) = 0 \tag{3.20}$$

The previous mode is valid until S_2 and S_3 are switched off again. Hence the instant when this happens can be controlled so that it becomes possible to keep the voltage at zero for as long as it takes to switch the inverter switches to their new states

plus a safety margin to prevent shoot-through. The inductor current stays constant in theory; in practice the equivalent series resistance of the choke plus the on-state voltage drops of the diodes and transistors will mean that i_{Lr} decreases.

During $[t_3, t_4]$, the capacitor C_r is recharged to V_S with the resonant current flowing through the diodes D_2 and D_3 into C_r. The describing equations are:

$$i_{L_r}(t) = (I_p - I_{ox})\cos(\omega_r t) + I_{ox} \tag{3.21}$$

$$v_{C_r}(t) = Z_r(I_p - I_{ox})\sin(\omega_r t) \tag{3.22}$$

This mode is valid for

$$T_4 = \frac{1}{\omega_r}\arcsin\left(\frac{V_S}{Z_r(I_p - I_{ox})}\right). \tag{3.23}$$

where I_{ox} denotes the output current for the new inverter state. I_{ox} has to be predicted in order to determine the correct initial current in the inductor. At the end of this mode, the remaining current in the inductor can be obtained from (3.21) as

$$I_r = i_{L_r}(t_4) = \sqrt{(I_p - I_{ox})^2 - \left(\frac{V_S}{Z_r}\right)^2} + I_{ox} \tag{3.24}$$

When the capacitor voltage reaches V_S at $t = t_4$, diode D_1 will start to conduct and clamp the voltage to V_S. S_1 can now be turned on again with zero voltage. The remaining energy in the inductor is returned to the voltage source. The equations for the interval $[t_4, t_5]$ are:

$$i_{L_r}(t) = \frac{-V_S}{L_r}t + I_r \tag{3.25}$$

$$v_{C_r}(t) = V_S \tag{3.26}$$

This mode is valid for

$$T_5 = \frac{L_r I_r}{V_S}. \tag{3.27}$$

With the previous results it is possible to derive waveforms of the relevant quantities i_{L_r} and v_{C_r} during a resonant cycle. A plot of these waveforms for a resonant transition frequency of 82kHz and no load was shown in Figure 3.9.

3.3.3 Design considerations

As mentioned before, the stored energy in the resonant inductor L_r must be large enough to charge the resonant capacitor C_r back to V_S. A necessary condition for safe operation of the link can be derived from (3.24):

$$I_p \geq \frac{V_S}{Z_r} + I_{ox} \tag{3.28}$$

The load current I_{ox} of the next inverter state can be predicted from the instantaneous phase currents as

$$I_{ox} = S_a I_a + S_b I_b + S_c I_c \tag{3.29}$$

where S_x denotes the switch status of the respective inverter phase. From (3.18) and (3.28) the initial current I_i has to satisfy the following condition:

$$I_i \geq \sqrt{\left(\frac{V_S}{Z_r} + I_o + I_{ox}\right)^2 - \left(\frac{V_S}{Z_r}\right)^2} - I_o \tag{3.30}$$

A graphical representation of the relation between present inverter input current I_o, next inverter input current I_{ox} and required initial current I_i is given in Figure 3.11.

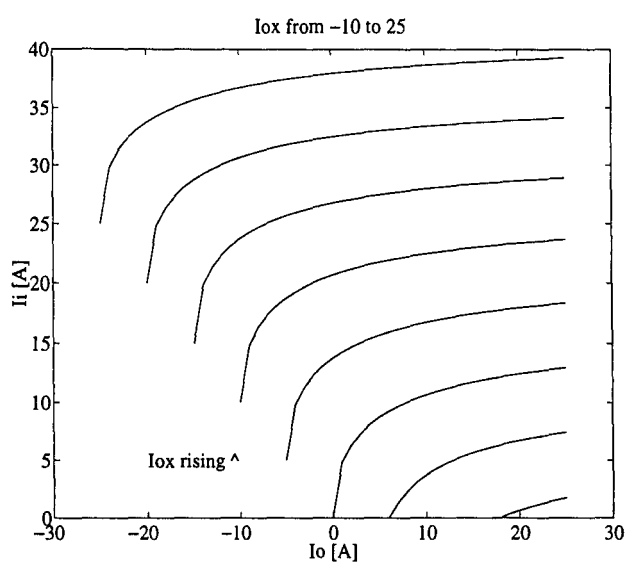


Figure 3.11: Required initial current I_i as function of I_o and I_{ox}.

It is important to note that the resonant transition frequency also depends on I_o and I_{ox} respectively. Figure 3.12 shows a plot of the resonant frequency for different

values of I_o and I_{ox}. As can be seen in Figure 3.9, the voltage across the dc bus never

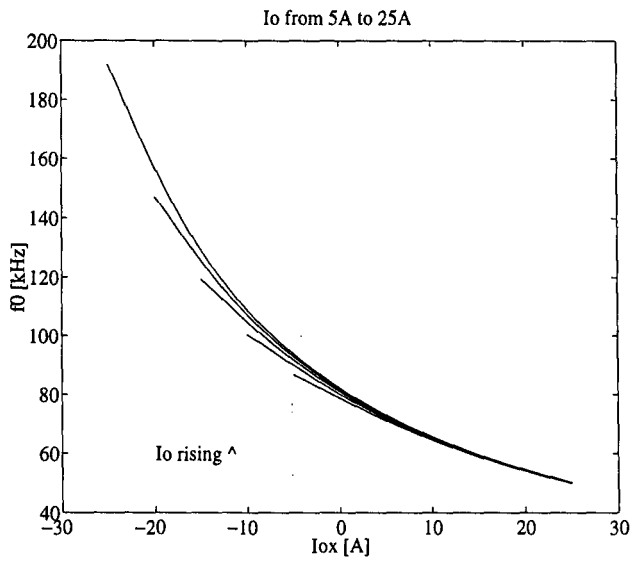


Figure 3.12: Resonant transition frequency f_0 as function of I_o and I_{ox}.

exceeds V_S during a resonant cycle. The voltage stresses for all additional devices S_1 to S_3 will therefore be limited to V_S. The minimum pulse width that can be created

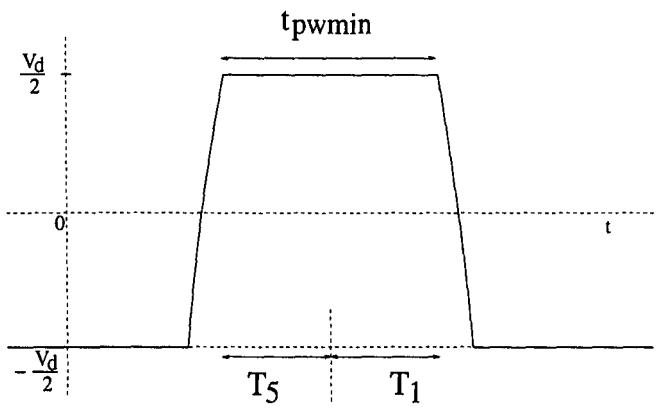


Figure 3.13: Derivation of minimum possible pulse width.

by the PRDCL inverter can be derived as the sum of T_1 and T_5. To illustrate this fact, Figure 3.13 shows a theoretical waveform of the phase-to-midpoint voltage of a three-phase PRDCL inverter and the connection between T_1, T_5 and $t_{pw_{min}}$. Under the assumption that I_i is optimally controlled the worst case minimum pulse width is given by

$$t_{pw_{min}} = \frac{2L_r}{V_S}\sqrt{I_{omax}\left(\frac{V_S}{Z_r} + I_{omax}\right)}. \tag{3.31}$$

3.3.4 Simulation results

A SABER simulation of a single-phase PRDCL inverter in H-bridge configuration was developed in order to verify the theoretical analysis. The values for L_r and C_r are 47.5μH and 0.141μF respectively. The load consists of an RL series combination with 10Ω resistance and 30mH inductance. Figure 3.14 shows resonant link current i_{L_r}, resonant capacitor voltage v_{C_r} and load current i_o for one resonant cycle. The

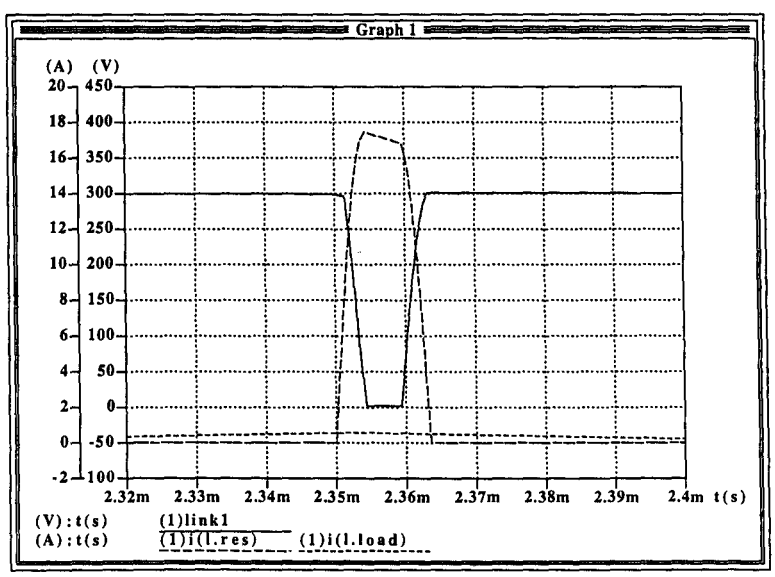


Figure 3.14: Simulated dc-link voltage, resonant inductor current and load current of single phase PRDCL inverter.

resonant inductor has a series resistance of 100mΩ which leads to the drop in current that can be seen in the graph. Also visible is a slight glitch in the capacitor voltage at the beginning of the resonant cycle. At this point, the resonant current should be supplied by the large dc bus capacitors. However, due to the inherent inductance of these electrolytic capacitors which was included in the model, C_r is slightly discharged when S_2 and S_3 turn on.

The next figure shows two successive resonant cycles. Note that the initial current I_i is the same for both transitions. For the first cycle, the dc link current before commutation (I_o) is negative and positive after commutation. For the second commutation the opposite is true. According to (3.18) this leads to a higher peak current I_p in

the second transition than in the first which is clearly reflected in the graph. After the first commutation, I_{ox} is positive and hence tends to remove energy from the link whereas after the second commutation, the dc-link current will be negative ie. the dc-link current I_{ox} supports the recharging of C_r which results in the higher peak current. The simulation results confirm the theoretical analysis and prove the work-

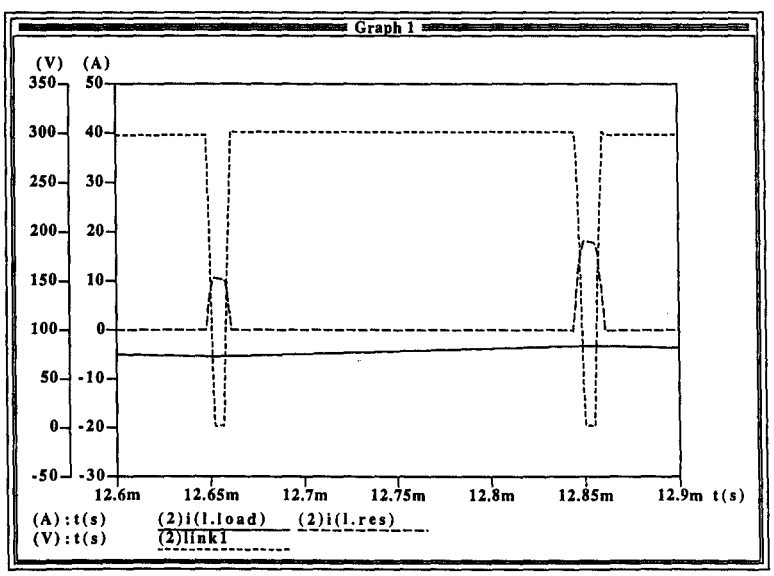


Figure 3.15: Simulated dc-link voltage, resonant inductor current and load current of single phase PRDCL inverter.

ing principle. The necessity of initial current control and hence a current prediction also becomes evident.

3.3.5 Experimental results of single-phase prototype inverter

A prototype of the proposed inverter circuit was built up using IGBTs as switching devices. The device ratings are identical for S_1 to S_3 (600V, 70A[1]). The values of the resonant components are $L_r = 37.3\mu$H and $C_r = 0.141\mu$F, yielding a no-load resonant transition frequency of about 82kHz. The firing pulses for the auxiliary switches S_1 to S_3 are produced by a network of transputers and customised interface circuits that will be presented in Section 3.5. The supply voltage V_S is 312V. Resulting waveforms

[1]at $T_j = 25°C$, 39A at $T_j = 125°C$

of the resonant current and dc link voltage for no load are shown in Figure 3.16.

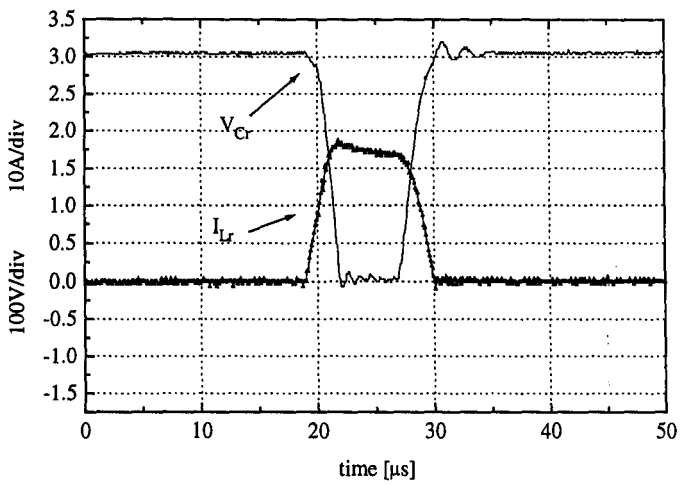


Figure 3.16: DC-link voltage and resonant current of prototype inverter.

It can be seen that the dc link voltage resonates to zero and is clamped to that value for about $5\mu s$. During this time it is possible to change the states of the inverter switches without switching losses. The resonant current does not stay quite constant but decreases due to losses in the resonant components (mainly L_r) and in the switching devices. The resonant link action takes $11.6\mu s$, leading to a resonant transition frequency of about 86kHz. This corresponds well with the theoretically predicted value. The resonant tank components have the same values that led to the results shown in Figure 3.9. The calculated peak current is 19.2A which again agrees well with the practical result given above. At the beginning of the resonant cycle (when S_2 and S_3 turn on), C_r can be seen to be slightly discharged. The reason for this is that the comparatively small resonant capacitor has a much better high frequency response than the large electrolytic dc link capacitors and thus provides some of the current in L_r at this point. Any stray inductance along the path between C_r and the dc link contributes to this phenomenon. The ringing at the end of the resonant cycle is due to the same reason. Any residual current left in L_r after v_{C_r} has resonated back to dc link voltage level will tend to overcharge C_r rather than return to the dc link capacitors, thus setting up the oscillation shown in Figure 3.16.

3.4 Comparison of PRDCL circuits

When comparing the two PRDCL inverter topologies, two distinctive advantages of the second type over the first one become apparent:

- No additional voltage stress for the auxiliary as well as the inverter devices.
- A resonant cycle requires less switching action by the auxiliary devices.

For the second inverter type, the voltage stress is limited to V_S for all additional devices while it can be up to $2V_S$ and higher for one of the devices (S_2) for the first type.

With regard to the necessary switching action it can be noted that the resonant cycle requires less frequent activation of the auxiliary switches for the second type than for the first one. In the second case, the diodes conduct the resonant current for a large part of the cycle and switches S_2 and S_3 only have to be turned on once and then turned off again.

It is intuitive that for given devices with their respective turn-on and turn-off times the switching sequence that occurs in the second type will require less time.

The experimental results confirm this assumption: The 32kHz resonant transition frequency that were achieved for the first prototype circuit did not appear to be an upper limit looking at the device ratings. However, increasing the frequency was not straightforward since the switching edges in the resonant cycle sequence come to lie very close to each other. In the second case, the diodes D_2 and D_3 take over the resonant current between the second and third step. Hence it is not necessary to produce any accurate gating pulses during that time. The resonant transition frequency of 86kHz therefore did not appear to cause any problems in the turn-on and turn-off process of the devices.

Creating and transmitting the timing signals also appears to be an easier task than for the first case, simply because there are less signals to be timed.

As a conclusion from the above, it was decided that future work should be focused on the second PRDCL inverter circuit and a three-phase prototype was developed.

3.5 Realisation of three-phase PRDCL inverter

3.5.1 Power circuit design

To implement the PRDCL circuit in a three-phase inverter system, a commercial IGBT inverter was modified and supplied with the resonant dc link circuit. Figure 3.17 shows where the dc link of the IGBT inverter has to be split up and the resonant link

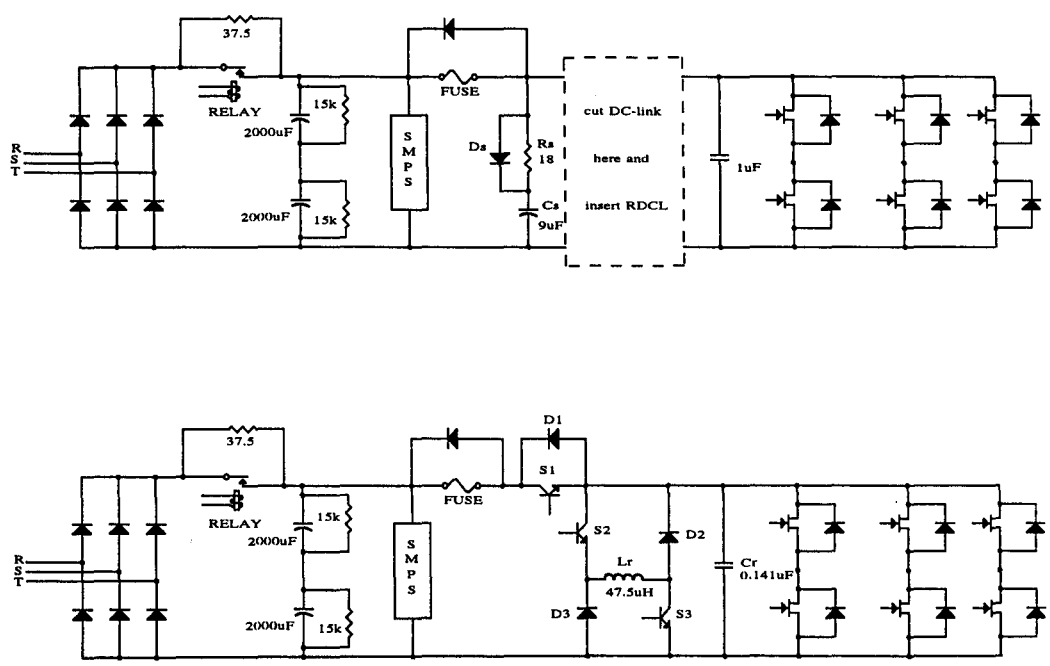


Figure 3.17: Transformation of regular three-phase IGBT inverter into three-phase PRDCL inverter.

inserted. The snubber circuits as well as the small high frequency capacitor across the dc bus were removed. The zero-voltage period was chosen to be 5μs because the commercial inverter uses a 5μs dead-time. In order to prevent shoot through of the inverter devices it was therefore decided to leave the dead-time unchanged, even though the switching takes place at zero voltage. For IGBTs with shorter dead-time requirements or faster turn-off times, the zero voltage time can be decreased which will allow faster resonant transition times and consequently higher switching frequencies. The original PWM generator of the commercial inverter was replaced by a purpose-built interface in order to allow synchronisation of the PWM gating signals with the firing pulses for the auxiliary devices. This circuit will be described in a later section.

Resonant tank component selection

The appropriate resonant tank components can be determined with the following criteria in mind:

- desired resonant transition frequency
- desired dv/dt
- peak current in L_r and hence in S_2 and S_3
- losses in the resonant link (mainly in L_r)

An optimisation procedure would therefore proceed as follows: First, a desired resonant transition frequency has to be specified. The maximum allowable peak current in the inductor is the second condition that has to be satisfied by the chosen components. In order to keep losses low, the resonant inductor should be as small as possible. However, the smaller the resonant inductance becomes, the bigger the peak current will be. Hence there is a lower limit for the inductor. An iterative Pascal procedure was developed that starts off by ensuring that the desired resonant frequency is obtained, then tries to minimize L_r while at the same time testing if I_p does not exceed

its limit. This optimisation procedure was given the following constraints: Resonant frequency at least 60kHz for all load conditions, I_p not greater than 35A, desired maximum output current I_{omax} 15A and V_S 312V. The results for these conditions are given in 3.1. The components that were chosen for the experimental prototype

Source voltage (V_S)	312V
Maximum output current (I_{omax})	15A
Resonant inductor (L_r)	42.6μH
Resonant capacitor (C_r)	0.175μF
Peak inductor current (I_p)	35A
Resonant transition frequency (f_{rmin})	60kHz

Table 3.1: Results of optimisation procedure for resonant tank components.

are given in Table 3.2. The resonant capacitor C_r was constructed by paralleling three

Source voltage (V_S)	312V
Maximum output current (I_{omax})	15A
Resonant inductor (L_r)	37.3μH
Resonant capacitor (C_r)	0.141μF
Peak inductor current (I_p)	42.7A
Resonant transition frequency (f_{rmin})	59.34kHz

Table 3.2: Experimental resonant tank components.

polypropylene capacitors of 0.047μF each. These capacitors are characterised by low loss and good high frequency performance. Since the dv/dt across C_r is modest, the current in C_r will not be excessive. For the chosen resonant tank components, the current in C_r does not exceed $-I_{C_r max}$=49A. The resonant inductor was made of 4 wires of 1.04mm diameter, twisted together and wound on an air core of 64mm diameter. The winding consists of only one layer so that losses due to proximity effect should not play an important role. The twisting is done to keep skin effect losses low.

Switching device selection criteria

As was shown in Section 3.3.3 the voltage stress for the main inverter devices as well as the auxiliary devices in the resonant link never exceeds the supply voltage level. Hence the auxiliary devices do not need to have a higher voltage rating than the main devices. The project is aimed at proving the capability of the PRDCL inverter to operate at medium to high power levels. Therefore, the devices that come into consideration are IGBTs, MCTs — and for very high power — GTOs. Recent research suggests that MCTs lead to far higher switching losses in zero voltage conditions than IGBTs [39], mostly due to a much longer turn-off current tail as compared to IGBTs. Therefore, the devices chosen for this project were fast switching IGBTs. To determine the required current capability of the additional devices, one has to consider the desired power level with given resonant tank components. It can be noted that S_1 has to conduct the load current plus the initial current I_i while the devices S_2 and S_3 have to conduct the peak current in the resonant inductor. For instance, with a DC-link voltage of 312V, a desired maximum inverter input current of 15A and resonant tank components as given above, the maximum current stresses for the additional devices are given in Table 3.3. The devices chosen for S_1–S_3 and

Source voltage (V_S)	312V
Maximum output current (I_{omax})	15A
Resonant inductor (L_r)	37.3μH
Resonant capacitor (C_r)	0.141μF
Peak current for S_2/S_3	42.7A
Peak initial current (I_{imax})	30.3A
Peak current for S_1 ($I_{omax} + I_{imax}$)	45.3A

Table 3.3: Maximum current stresses for additional devices.

D_1–D_3 are shown in Table 3.4 together with some information from their data sheets.

	S_1–S_3	D_1–D_3
Device name	IRGPC50F	BYT 30P-800
Voltage rating	600V	800V
Current rating ($T_j = 25°C$)	70A	70A
($T_j = 125°C$)	39A	
Forward voltage drop	<= 1.7V	<= 1.9V

Table 3.4: Voltage and current ratings for additional devices.

3.5.2 Current prediction and measurements

As was explained in Section 3.3.3, information about the current as well as the future inverter input current is needed to determine the required initial current in the resonant inductor. Hence, two output phase currents are measured through hall effect current transducers whose output signals are passed through filters and then into an AD converter. Assuming that the load has no neutral connection, the third output phase current can be calculated from the other two. The actual and future switch states are determined by the modulation strategy and are therefore known. By applying (3.29), the current signals can thus be used to predict the future inverter input current. This information can be used to determine the required initial current in the inductor using the inequality (3.30) which is repeated here for convenience.

$$I_i \geq \sqrt{\left(\frac{V_S}{Z_r} + I_o + I_{ox}\right)^2 - \left(\frac{V_S}{Z_r}\right)^2} - I_o$$

It should be noted that the inequality can only be solved by real numbers as long as the term under the square root does not become negative. This happens when the sum of I_o and I_{ox} are negative and bigger than $-2\frac{V_S}{Z_r}$ (see Appendix B). In Figure 3.11 this effect is illustrated by the sudden end of the lines when $I_o = -I_{ox}$. Figure 3.18 shows a three-dimensional representation of I_i in relation to I_o and I_{ox}. In this graph, the area for which the result of (3.30) becomes complex is shown as zeros ($z = 0$). When according to (3.30) I_i becomes imaginary, a second condition is used to derive a real value for the required initial current. In Section 3.3.2, the duration of the

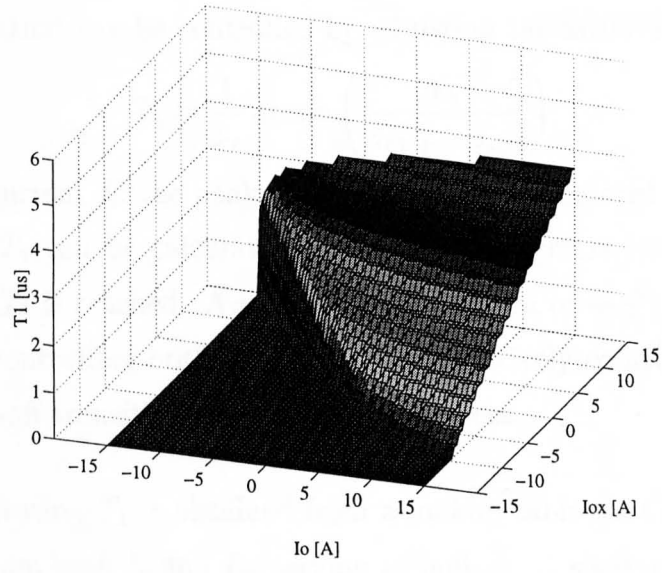


Figure 3.18: Surface plot of T_1 as derived with Equation (3.30).

resonant discharge of C_r was given by

$$T_2 = \frac{1}{\omega_r} \arctan\left(\frac{V_S}{Z_r(I_i + I_o)}\right) \tag{3.32}$$

A plot of this expression as a function of $\frac{V_S}{Z_r(I_i+I_o)}$ in Figure 3.19 shows that to guarantee that T_2 does not exceed a certain limit, the argument has to be chosen smaller than some threshold value. For a given I_o, I_i is the only variable in the above expression,

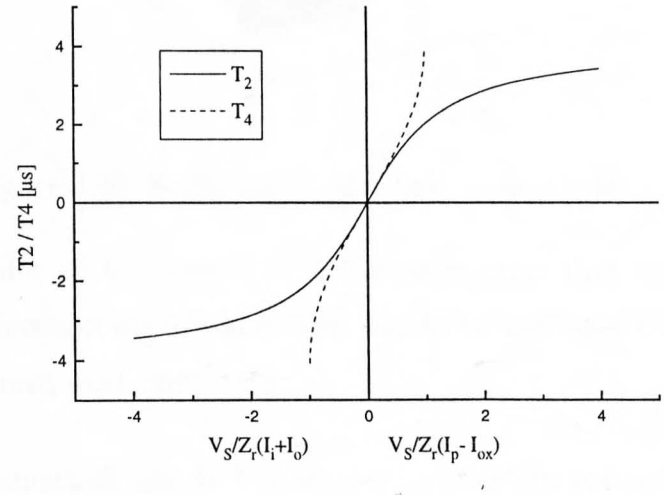


Figure 3.19: Plot of T_2 and T_4 as functions of $\frac{V_S}{Z_r(I_i+I_o)}$ and $\frac{V_S}{Z_r(I_p-I_{ox})}$ respectively.

hence it can be chosen to fulfill the requirement.

Another quantity that can be controlled by adjusting the initial current is T_4:

$$T_4 = \frac{1}{\omega_r} \arcsin\left(\frac{V_S}{Z_r(I_p - I_{ox})}\right) \tag{3.33}$$

Given an initial current I_i, the peak current I_p can be calculated using (3.18). With this information T_4 can be calculated and I_i can be iteratively increased until the desired value for T_4 is reached. A plot of T_4 as function of $\frac{V_S}{Z_r(I_p - I_{ox})}$ is also given in Figure 3.19. By controlling both T_2 and T_4, one effectively controls the dv/dt for all turn-on and turn-off transitions of the inverter devices.

In the control software, T_1 is obtained from a lookup table that is calculated at the start of the program with I_o and I_{ox} serving as indices. A surface plot of this lookup table including the modifications according to (3.32) is shown in Figure 3.20. When

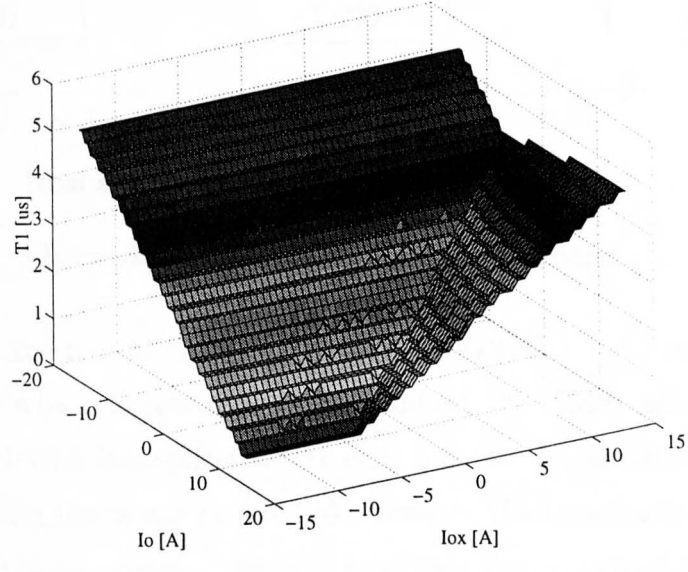


Figure 3.20: Surface plot of actual lookup table for T_1.

comparing this plot with Figure 3.18, it becomes clear that in order to guarantee successful link operation the initial current has to be increased over the value derived using (3.30) for most load conditions.

To allow measurement of the dc bus voltage, a resistive voltage divider was placed in parallel with the resonant capacitor. The divided signal is passed to a comparator that goes high when v_{C_r} returns to V_S and thus leads to the turn-on of S_1 under zero voltage.

3.5.3 Transputer control of three-phase PRDCL inverter

A network of three T800 transputers is applied to control the IGBT inverter, the resonant dc link circuit and an A-D converter that is used to quantize phase current measurements and supply them to the attached transputer (see Figure 3.21). The

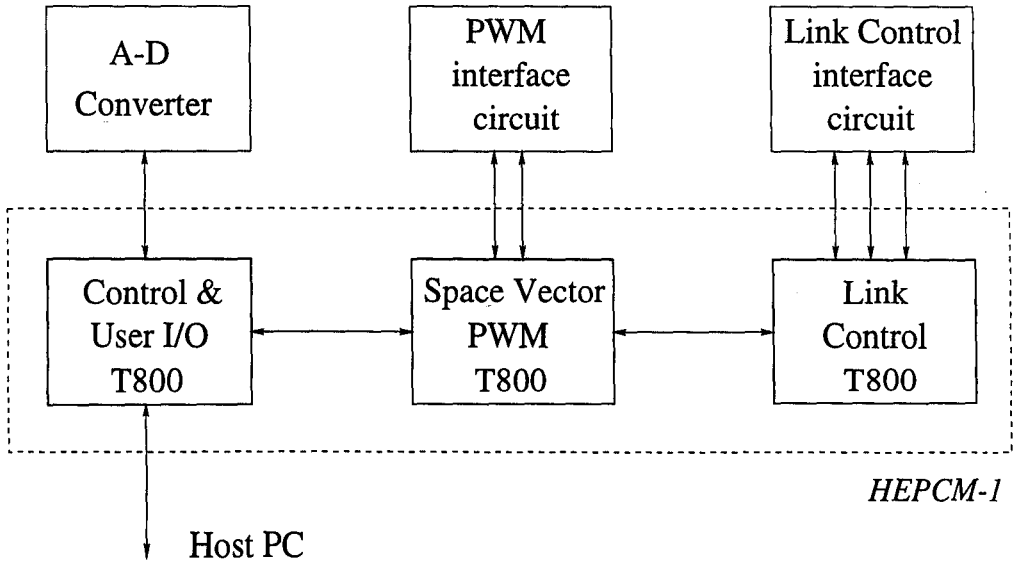


Figure 3.21: Schematic of Transputer network.

three tansputers are mounted on a PC card (HEPCM-1 [56]) represented by the dashed rectangle which is installed in a standard PC. Each arrow in Figure 3.21 represents one link of a transputer where each has four bi-directional links available. Links that lie within the rectangle are links between the transputers while the arrows that leave the rectangle represent links to hardware that is external to the transputer board. The actual connections on the HEPCM-1 that constitute the links are made with special jumpers so that a large number of constellations is possible. The one chosen is a simple pipeline with no connection from the third transputer back to the first. The ideal constellation depends on the application and in the present case, the Link Control requires three external links and does not need to communicate directly with Control & User I/O, thus the third transputer in the pipeline is the obvious choice. The PWM procedure has to communicate with both Control & User I/O and Link Control and hence is run on the second transputer. Control & User I/O needs to communicate with the host and so it is intuitive to run this procedure on the first

transputer.

The data exchange with the external hardware interfaces is carried out by the Inmos C011 link adapter chip [55]. This chip provides a serial communication link with 20 Mbit/s data rate. A handshake protocol between transputer and link adapter is used to signal that data is ready to be sent to the transputer or received by the link adapter. A more detailed description of the function of this link adaptor can be found in Appendix A.3. The function of each of the external hardware interfaces that were developed will be described briefly in the following sections. The circuit diagrams can be found in Appendix A. Following the hardware descriptions, some fragments of Occam code are shown to illustrate the approach that was taken to implement each task on a transputer as well as supplying the necessary communication between each of them.

3.5.3.1 Overseer and User I/O

The main task of the overseer and I/O block is to maintain a communication link between the user and the program running on the transputers. Parameters and commands are passed on from user input to the relevant procedures, ie. PWM Generation and Link Control. The second task is to control the sampling process of the AD-converter and to read sampled data out as soon as it becomes available. Only one link adaptor is required to control and read the AD-converter, making use of its bi-directional parallel bus.

3.5.3.2 PWM generator

The PWM generator circuit uses the Intel 82C54 timer chip to create gating signals for the three phases of the IGBT inverter. The chip contains three 16-Bit counters and is clocked at 5MHz, allowing a resolution of 200ns for each pulse. Two link adaptors are used: One to address the appropriate timer and to initiate the writing

of data to it. The other one outputs the pulse widths that are calculated in the PWM procedure to the parallel input of the 82C54 (**D1–D7**).

3.5.3.3 Link control

The Link control circuit produces the gating pulses for the additional devices in the resonant link. Each PWM switching edge requires two timed pulses for the resonant link devices so a total of six timed pulses are required for a PWM modulation period with three switching edges. Two 82C54 chips are supplied for this purpose. In order to output the pulses from the appropriate timer, a dual multiplexer is applied that can select between four different inputs. The control inputs **A** and **B** in Figure 3.22 receive logic signals from another Intel 82C54 timer and some additional logic gates as shown. The outputs of the other two 82C54 circuits are connected to the inputs **1C0–1C2** and **2C0–2C2** respectively. Three link adaptors are used to control and load the timers. Timing diagrams that show the operation of the multiplexer circuit are given in Appendix A.5.

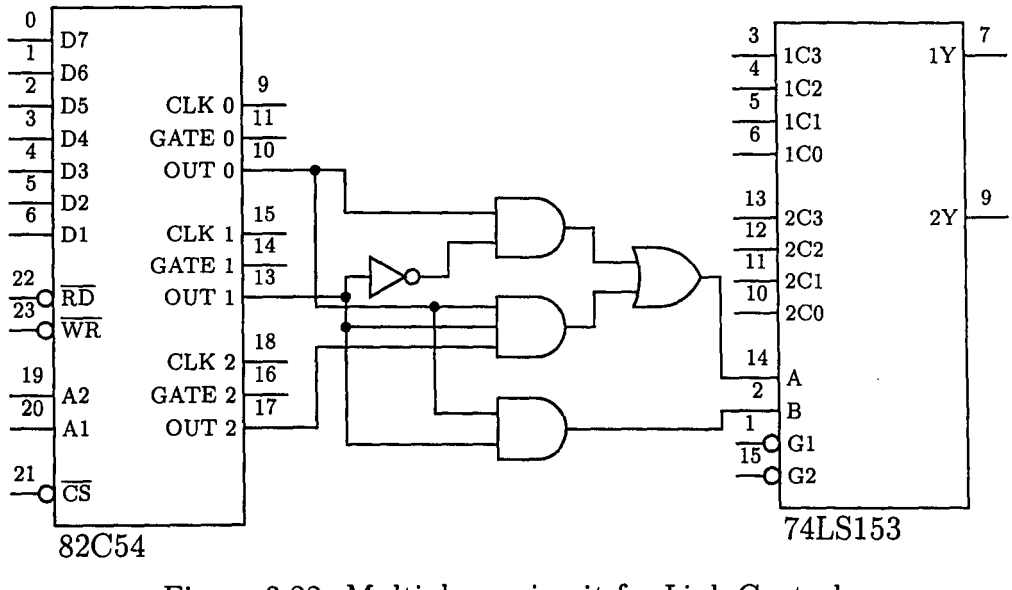


Figure 3.22: Multiplexer circuit for Link Control.

3.5.4 Realisation of control software in OCCAM

The OCCAM programming language was developed specifically to be used with transputers in real-time applications that require parallel processing [53]. Hence it provides constructs that allow the distribution of a program on a number of transputers and also for communication and synchronisation of the various parts of a program. Some passages of the PRDCL control software are given below. Some notational aspects of OCCAM are shown in these examples. A fold begins with three periods and contains a number of statements. It is used to make source code more readable. The scope of a statement can be derived from indentations. For instance, after a SEQ statement, all the statements that lie within the scope of the SEQ command have to be indented by two blanks. Further nesting leads to appropriately more blanks.

The allocation of certain tasks to certain transputers is reflected in the way the software is distributed on the three transputers. Each transputer runs one procedure and all procedures (or rather the transputers on which they are run) are communicating with each other. PWM communicates with Link control and Control & User I/O communicates with PWM. Finally, Control & User I/O communicates with the host PC that runs a Turbo Pascal program which allows to pass parameters and commands to the software running on the transputers and to receive data from the transputers and display it on the host PC.

The only mechanism that Occam provides for the exchange of data between procedures is communication through channels. These channels have to be declared for a certain data type and no other type can be passed through them. It is important to make sure that when a procedure requires input through a channel from another procedure that the data is actually presented at the channel, otherwise the inputting procedure waits for the outputting procedure and the so-called deadlock occurs. In a deadlock situation, the execution of the program stops and in our context that would mean that the calculation and outputting of PWM gating pulses stops. This would endanger the inverter devices and has to be avoided. Below are some fragments of code that show how the control software was realised as well as some key concepts of

the Occam programming language.

Control & User I/O The first procedure that forms part of the Control & User I/O block is called overseer and begins with a WHILE TRUE statement which means that the program is essentially running forever once it has been started. The procedure header contains the channel declarations which in this case are all INT16 channels (an integer with a 16 Bit representation). Occam assumes that tasks are run in parallel, so a special construct has to be used to indicate which statements have to be executed sequentially. This is done by the SEQ construct in the line following the WHILE TRUE. Channel communication is performed as follows: `from.host ? choice` This statement means that the channnel from.host is expecting data that will be stored in the variable choice. The following IF statement has a TRUE option followed by a SKIP statement to avoid deadlock. The skip statement does nothing but if the TRUE SKIP sequence would not be provided and none of the if options were true, the execution of the program would stop. If a change in modulation index and frequency is required, the new reference frequency is read in and then sent to the control procedure: `supervisor.to.control ! frequency`. The control procedure which is executed on the same transputer as the overseer procedure starts with the declaration of the required communication channels followed by another WHILE TRUE loop. Inside this loop, a PRI PAR statement effects that the code that lies within the PRI PAR scope is executed with a higher priority than code that does not lie within this scope. Also, the high priority timers become accessible to the procedure which means that timing can be performed with an accuracy of $1\mu s$. The following lines contain code that update the PWM procedure, initiate analog to digital conversions and read out the results. The PRI ALT statement means that for a specified time ("wait") the procedure monitors if data is presented on a channel and skips otherwise. In a PRI PAR there have to be at least two processes that run concurrently. In the control procedure however we do not want another process apart from the one just described which is why the second process is just a dummy SKIP. The desired angle and the magnitude of the output voltage is calculated in the control procedure and sent to the PWM procedure.

```
PROC overseer (CHAN OF INT16 control.to.supervisor,
                    supervisor.to.control, from.host, to.host)
  WHILE TRUE
    SEQ
      from host ? choice
      IF
        choice=(change frequency and modulation index)
          SEQ
            from.host ? frequency
            supervisor.to.control ! frequency
        choice=(update host)
          SEQ
            control.to.supervisor ? Ia
            control.to.supervisor ? Ib
            to.host ! Ia
            to.host ! Ib
            to.host ! frequency
            to.host ! Vref
        TRUE
          SKIP

PROC control (CHAN OF REAL32 pwm.to.control, control.to.pwm,
              CHAN OF INT16 control.to.supervisor,
              supervisor.to.control)
  WHILE TRUE
    PRI PAR
      SEQ
        ... calculate voltage.angle and Vref
        control.to.pwm ! voltage.angle
        control.to.pwm ! Vref
        ... read AD converters and send currents to PWM
        clock ? now
        PRI ALT
          supervisor.to.control ? frequency
          clock ? AFTER (now PLUS wait)
            SKIP
      SKIP  -- dummy
```

Space Vector PWM The PWM procedure gets the desired voltage vector angle and the magnitude of the output voltage from the control procedure. From that, the switching times are calculated and downloaded to the counters. The switching frequency of the inverter is adjusted by storing the time just before triggering of the counters occurs and comparing the elapsed time after all calculations with a reference value (delay.slot). When this reference time has elapsed, a signal is sent to the Link Control procedure to trigger the counters after which the PWM counters are triggered as well.

```
PROC pwm (CHAN OF REAL32 control.to.pwm, pwm.to.control,
          CHAN OF INT pwm.to.link.control, link.control.to.pwm)
PRI PAR
  WHILE TRUE
    SEQ
      clock ? now
      ... trigger counters with previous values
      ... get voltage angle, Vd and segment counter from control
      ... calculate switching times
      ... calculate Io..Ioxxx and send to Link control
      ... output switching times to PWM generator board
      clock ? AFTER (now PLUS (delay.slot))
      pwm.to.link.control ! trigger
  SEQ
    SKIP
```

Link Control The Link control procedure works in a similar way as the PWM procedure does. The PWM switching times are received from the PWM procedure as well as the predicted inverter input current values for the next three switch states (Io..Ioxxx). After that, the timing of the auxiliary switches is calculated and the values are downloaded to the appropriate counters. When the trigger signal arrives from the PWM procedure the counters are triggered.

```
PROC link.control (CHAN OF INT pwm.to.link.control,
link.control.to.pwm)
  PRI PAR
    WHILE TRUE
      SEQ
     ... get next switching times from PWM
     ... get Io..Ioxxx from PWM
     ... obtain timing for auxiliary switches from Io..Ioxxx
     ... load counters on link control board
     pwm.to.link.control ? trigger
     ... trigger all counters
    SEQ
      SKIP
```

3.5.5 Protection circuitry

Two protection circuits are supplied, one to prevent damage of the inverter devices due to a deadlock of the transputer program and an overcurrent protection for the resonant link devices. The PWM inverter is protected by its own protection circuits.

PWM watchdog If the transputer program should get deadlocked as explained in Section 3.5.4, no new gating signals would be produced and the inverter switches would remain in their present states. This could lead to destruction of the devices since the current would only be limited by the load inductances. To avoid this, a watchdog circuit is used that monitors the gating signals coming from the PWM generator circuit. An 8-Bit counter is used that is incremented every two microseconds. After 512 microseconds, the counter runs over and takes its output high which in turn leads to the disabling of the PWM inverter. Therefore, if the transputers do not output new pulses for more than 512 microseconds, they are assumed to be deadlocked and the inverter is safely turned off. The circuit diagram of the deadlock protection is given in Appendix A.2.

Overcurrent protection To protect the auxiliary devices in the resonant link in the case of an accidental short-circuit, the current through S_1 is measured by a Hall effect current transducer and fed into a comparator. When the trip-level is exceeded, a latch ensures that S_1 and S_3 stay switched on regardless of any gating signals while S_2 stays off, thus creating a free-wheeling path for any current flowing in the resonant inductor. If all switches were switched off, the current in the inductor — which would potentially be large after an accidental short circuit — could only flow into the resonant capacitor, possibly charging it up to voltage levels that would be dangerous for the auxiliary as well as the inverter devices. A schematic of the protection circuit is given in Appendix A.1.

3.6 Summary

In this chapter two discontinuously resonant circuits were described and analysed. Simulations and experimental prototypes were developed to verify the operational principles and to find out how they perform in practical systems. It was found that the second type has a number of advantages over the first one. A three-phase

prototype was therefore developed on the basis of the second circuit. The design of this three-phase power circuit and the control hardware and software were described in the previous section.

Chapter 4

Modulation Strategies

4.1 Introduction

In this chapter, a number of modulation strategies will be introduced and their advantages and drawbacks will be pointed out. After a section about Sigma Delta modulation ($\Sigma\Delta$M), the well established Pulse Width modulation (PWM) technique will be described and various different representatives of this approach will be compared. A comparison of the merits and shortcomings of PWM and $\Sigma\Delta$M follows which shows the superiority of PWM. However, because of the restrictions of the PRDCL inverter discussed in Chapter 3, the standard PWM strategies need to be modified for effective use with the PRDCL circuit. Modified strategies that are suitable for the PRDCL inverter circuit are discussed and verified by simulation results.

4.2 Sigma Delta Modulation

In Chapter 2 it was explained that due to the sampled nature of their resonant link action, continuously resonant soft switching inverter systems do not allow the

application of modulation techniques in which the switching edges have to be freely positioned at arbitrary points in time and with high accuracy. Conventional PWM techniques demand this freedom in positioning of pulses and can therefore not be applied in this kind of inverter circuit. A suitable set of modulation techniques for these systems is the class of delta modulation techniques and in particular the Sigma Delta Modulation ($\Sigma\Delta$M). Delta modulation techniques have been used in the field of communication technology for a long time. Their properties will be the subject of the following section.

4.2.1 Operational Principle

An idealized block diagram of a $\Sigma\Delta$ modulator is shown in Figure 4.1. It basically

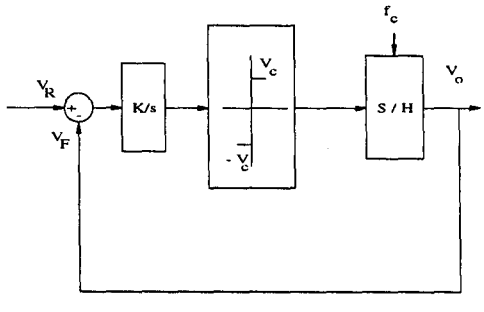


Figure 4.1: Block diagram of a Sigma Delta Modulator.

consists of an integrator, a quantizer and a sample and hold circuit. The output voltage is fed back to the input and the difference between reference and output voltage (the error) is integrated. The output of the quantizer is $+V_c$ for positive error and $-V_c$ for negative error. This output is sampled with the link frequency f_c. Consider the ACRDCL circuit described in Chapter 2. In a three-phase ACRDCL inverter, the output voltage of each inverter phase is controlled by a separate $\Sigma\Delta$ modulator leading to a sequence of sinusoidal pulses of varying polarity in the phase

voltages. Let the modulation index m be defined as

$$m = \frac{\text{peak fundamental phase voltage}}{\text{dc link voltage}/2} \tag{4.1}$$

The plot in Figure 4.2 shows a simulation result for the inverter output phase-to-midpoint voltage at a modulation index of $m = 0.8$ and a resonant frequency of the link of 10kHz. The phase voltage is normalised with respect to $V_q = V_{dc}/2$. The

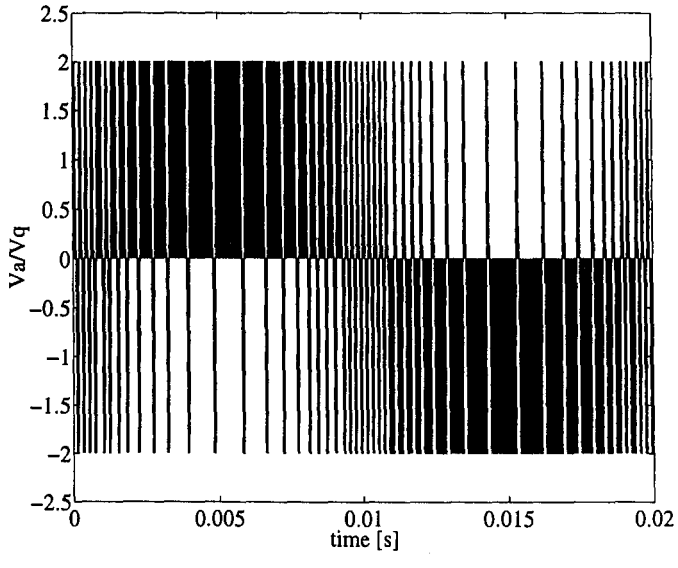


Figure 4.2: Phase voltage for Sigma Delta modulation.

line-to-line voltage together with the line-to-line reference waveform for a modulation index of $m = 0.4$ and 20kHz resonant frequency is shown in Figure 4.3. A section of the original plot has been enlarged to illustrate the poor behaviour of the line-to-line voltage. It can be seen that $\Sigma\Delta$M as such tends to synthesize line-to-line voltages that sometimes avoid the zero state and switch between two opposite voltages instead. The "Polarity consistency rule" however states, that the switched voltage should at least assume the same polarity as the reference voltage. The rule helps to identify ill-designed PWM schemes [26]. As can be seen in Figure 4.3, the $\Sigma\Delta$M scheme violates the polarity consistency rule. This effect becomes more pronounced with low modulation depths.

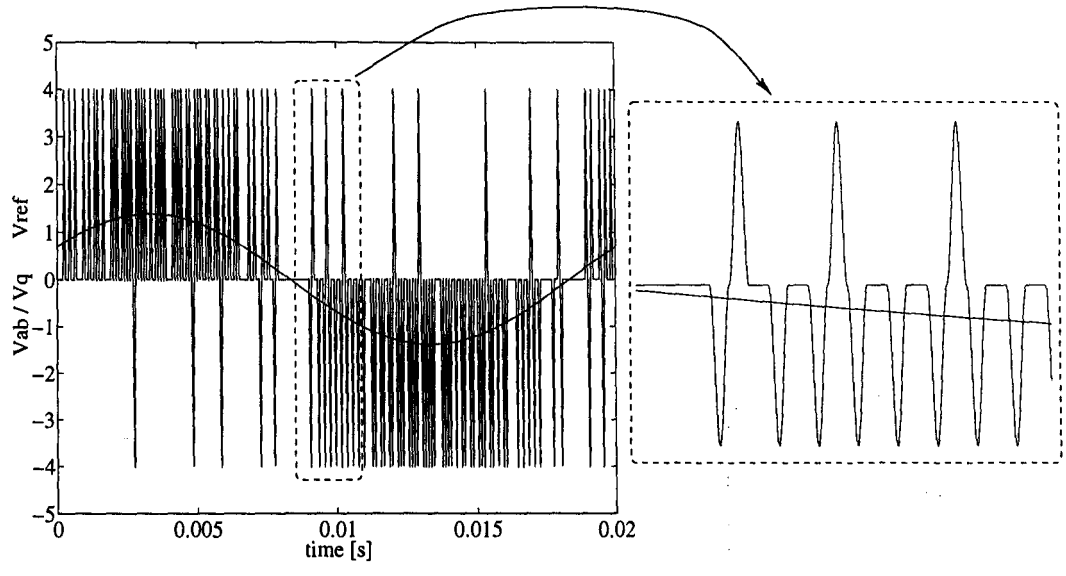


Figure 4.3: Line-to-line voltage for Sigma Delta modulation.

4.2.2 Frequency Spectrum

The frequency spectrum for ΣΔM has been analysed extensively through simulation [8–10] and more recently analytically [11, 12]. Some results are presented here. Consider the phase voltage spectrum in Figure 4.4 for a system with a resonant frequency of 10kHz and a modulation index of $m = 0.8$: The following characteristics of ΣΔM

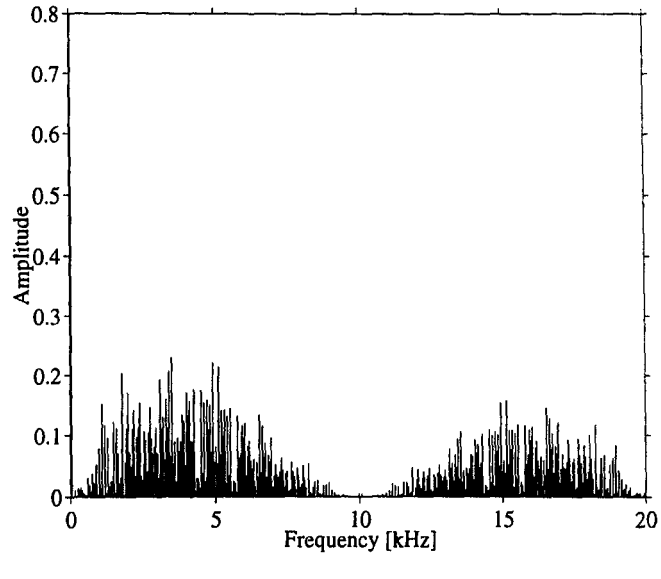


Figure 4.4: Spectrum of Sigma Delta Modulation.

become apparent:

- The spectrum contains significant energy at subharmonics of the inverter switching frequency (ie. the sampling/link frequency f_c).
- The spectrum is spread over a wide frequency band.
- The spectrum shows an approximate symmetry around $f_c/2$, which is a result of the sampled nature of $\Sigma\Delta$M.

The spread nature of the spectrum can be explained with the variable switching frequency of $\Sigma\Delta$M. The first two features in particular are highly undesirable in electrical drives applications and have prompted efforts to optimize and improve the modulation patterns.

4.2.3 Optimized $\Sigma\Delta$M

Some research has been undertaken to overcome the disadvantageous features of $\Sigma\Delta$M that were mentioned in the previous section. One approach exploits the discrete nature of $\Sigma\Delta$M and analyses each possible combination of positive and negative pulses using a cost function that models the behaviour of an electrical machine [13]. However, the required computation times become too long for high ratios of link to output frequency ($\frac{f_S}{f_R} > 80$). For a highly dynamic drive system (ie. vector control), it is also necessary to update the voltage and frequency demand for every output modulation period (reciprocal of inverter switching frequency), making it necessary to store and access large lookup tables for the pulse patterns. This has to be regarded as impractical and a clear disadvantage against PWM-based systems that determine the required pulse patterns in real time.

Another method regards the energy in the difference of the output due to the ideal input (usually a sinusoid) and the output due to the $\Sigma\Delta$ modulation as a measure of the quality of a modulation pattern [14]. The optimum pattern is then found through a binary search algorithm in which many branches can be eliminated from the search, making the algorithm less demanding on computation time.

Both techniques however do not allow to change the underlying characteristics of ΣΔM. They merely allow to choose the modulation pattern that has a minimum of the disadvantageous characteristics mentioned above.

A more practical approach is based on the already mentioned polarity consistency rule. It addresses the fact that ΣΔM as such tends to synthesize line-to-line voltages that avoid the zero state as was shown in Figure 4.3. A modified ΣΔ modulator that selects the zero state when appropriate can easily be implemented [9]. In all cases where this modulator chooses the zero state, the ordinary ΣΔM would produce either a positive or a negative pulse in the line-to-line voltage. A plot of the simulation results for such a modulator is shown in Figure 4.5, where the simulation parameters are the same as for Figure 4.3. For this modified ΣΔM, the polarity consistency rule

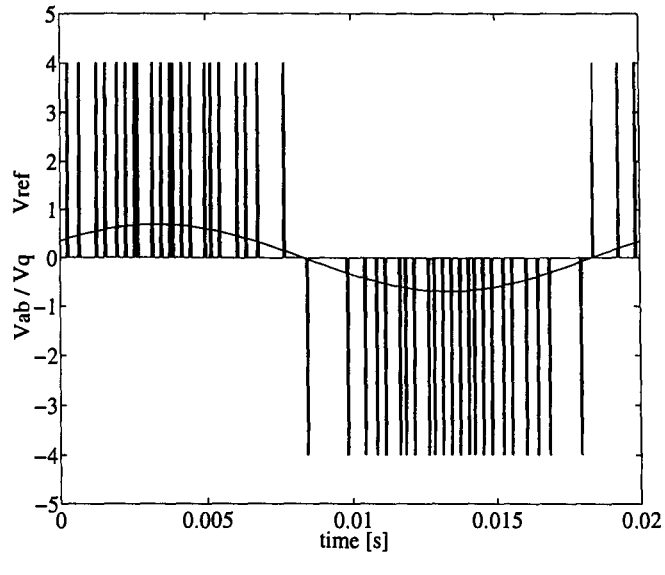


Figure 4.5: Line-to-line voltage for modified Sigma Delta modulation.

is not violated. Again, the underlying characteristics of ΣΔM are not changed but the frequency spectrum can be improved over the unmodified case for low modulation depths.

To conclude, it can be said that mainly due to constraints placed on switching instants, ΣΔM does not lead to as great an improvement in the spectral quality of the output voltage as the increase in switching frequency would suggest. It was found that high-frequency ΣΔ modulated systems generate more undesirable low-frequency

components in the output waveform than systems employing low-frequency PWM [10]. Optimized modulation patterns do not improve the situation significantly and become impractical due to the size of lookup tables that would be required to achieve instantaneous voltage and frequency control as real-time PWM systems do.

4.3 Pulse Width Modulation techniques

Pulse Width Modulation has been applied in power electronics for a long time and the properties of the various approaches have been covered extensively in the literature [24–31]. In this work, only carrier based methods are considered. These techniques have in common the use of subcycles of constant time duration where a subcycle is defined as the duration T_S during which each inverter leg assumes two consecutive switching states of opposite voltage polarity.

4.3.1 Subharmonic modulation method

The method employs a triangular carrier signal that is compared with the sinusoidal reference signal. Each inverter phase is controlled by its own modulator with the appropriate reference waveform. Switching instants occur where the triangular signal and the reference waveform intersect. A variation of the subharmonic modulation method (SHM) applies a distorted reference waveform that contains triplen harmonics (eg. added third harmonic). Adding a third harmonic with an amplitude of a sixth of the fundamental amplitude maximizes output voltage while adding a quarter of the fundamental amplitude yields an increase in output voltage of about 15% and at the same time an improved spectrum due to centralization of the zero states [30].

The switched voltage waveforms are modified in a way that their fundamental content is increased while no additional current harmonics are produced since triplen harmonics cancel each other in a three-phase system. Figure 4.6 shows the phase

voltage spectrum for a typical PWM strategy. The carrier to output frequency ratio is 23 and the modulation index is one. A third harmonic with a magnitude of 25% of the fundamental is added to the reference waveform. When comparing this spectrum

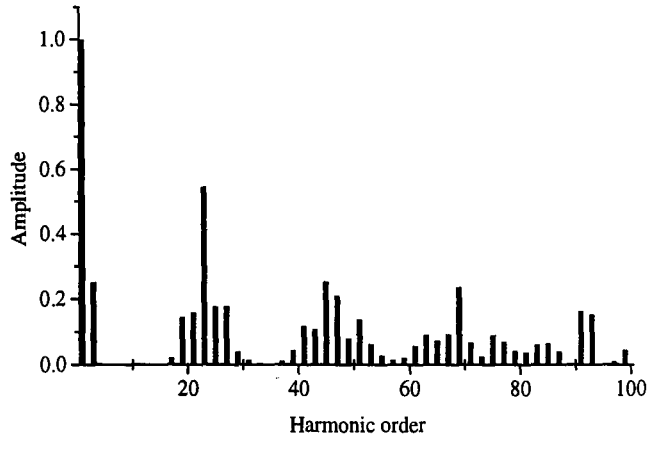


Figure 4.6: Phase voltage spectrum of regular sampled, asymmetric PWM.

with the one obtained through $\Sigma\Delta$M, the following positive characteristics of PWM become apparent.

- There is no significant amount of energy below the switching frequency.
- Harmonics mainly occur at integer multiples of the switching frequency.
- The switching frequency is constant.

The use of subcycles of constant duration (ie. constant switching frequency) leads to a harmonic spectrum that features two sidebands that are centered around the switching frequency and additional harmonic components at integer multiples of the switching frequency. Due to natural interaction between the phases, the zero state will be selected in the line-to-line voltage without extra measures, this being a necessary condition for an optimum modulation strategy [9]. It is also important to note that the third harmonic that can be seen in the phase voltage spectrum will be cancelled

out in a three-phase system with the neutral disconnected so it will not appear in the line-to-line voltage spectrum.

It is intuitive that the quality of the output spectrum mainly depends on the switching

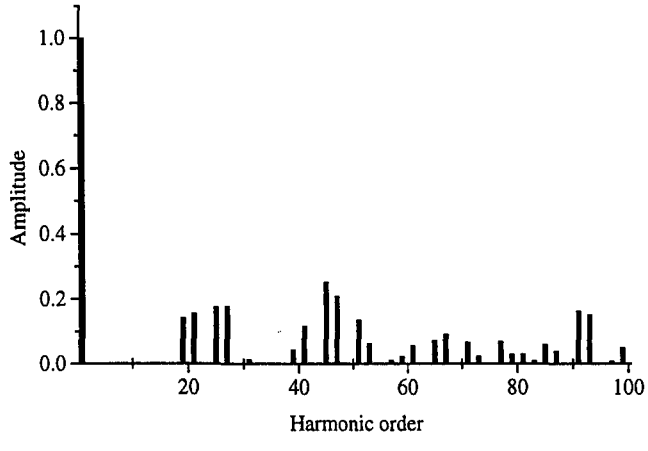


Figure 4.7: Line-to-line voltage spectrum of regular sampled, asymmetric PWM.

frequency. The higher the switching frequency, the higher the first harmonics in the output spectrum will be. With the predominantly inductive loads encountered in power electronics, this will lead to phase currents that contain only little energy in high frequency components. Figure 4.7 shows the line-to-line voltage spectrum of a typical PWM under the same conditions as in Figure 4.6. It can be seen that no triplen harmonics occur in the line-to-line spectrum.

4.3.2 Sampling methods

Natural sampling: In the past, a technique referred to as natural sampling has been widely used in PWM inverter control, mainly because of its simplicity and ease of implementation in analogue circuitry [29]. As shown in Figure 4.8, the technique uses a triangular carrier signal that is directly compared with a sinusoidal reference waveform to determine the switching instants. The resulting pulsewidth is therefore

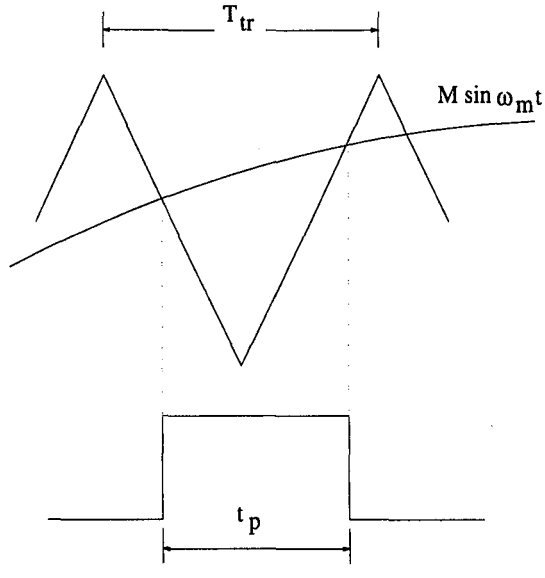


Figure 4.8: Natural sampled PWM.

proportional to the instantaneous amplitude of the reference signal at the time when the carrier and reference waveforms intersect. This makes it impossible to determine the pulsewidths analytically and prediction of pulsewidths cannot be performed.

Regular sampling: The development of powerful and affordable microprocessors has led to the widespread application of a technique called regular sampled PWM. The main feature of this approach is that the (sinusoidal) modulation signal is sampled at either carrier frequency (symmetric PWM) or twice the carrier frequency (asymmetric PWM). Figure 4.9 shows the case of symmetric PWM where the sampled value of the reference waveform is kept constant for a whole period of the carrier waveform (T_{tr}). Both edges of the resulting pulse are equally modulated whereas in the case of asymmetric PWM the leading and trailing edges of each pulse are defined by two subsequent samples of the modulating wave, leading to different amounts of modulation for each edge. As a result of the sampling process, the widths of the pulses are proportional to the amplitudes of the modulating waveform at uniformly spaced sampling times. With the sampling points and sampled values defined, the resulting pulses can be predicted in their widths as well as in their positions which was not the case for natural sampled PWM. Furthermore, it is now possible to derive

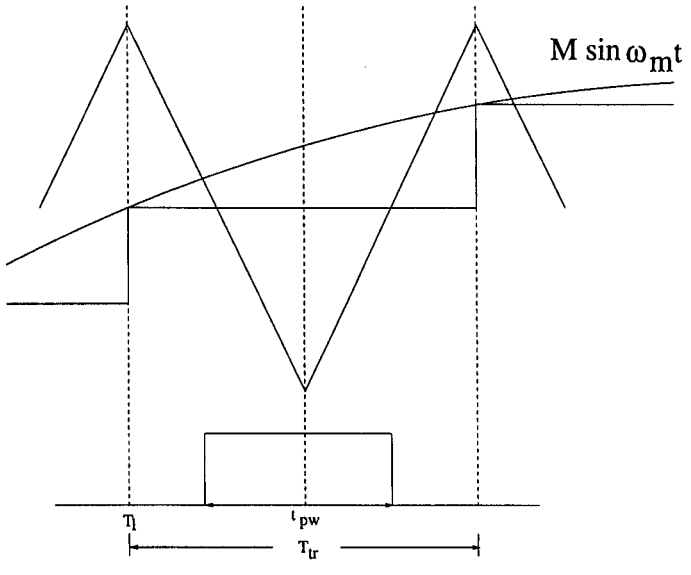


Figure 4.9: Regular sampled PWM (symmetric).

a simple equation for the pulsewidth. With regard to Figure 4.9, we can write:

$$\lambda = \frac{M \sin \omega_m T_1}{4} T_{tr} \tag{4.2}$$

and therefore

$$t_{pw} = \frac{T_{tr}}{2}(1 + 2\lambda) \tag{4.3}$$

for symmetric PWM and

$$t_{pw} = \frac{T_{tr}}{4}(1 + \lambda) \tag{4.4}$$

for asymmetric PWM.

4.3.3 Synchronous and asynchronous PWM

In order to make maximum use of the spectral qualities of PWM, the switching frequency should be at its maximum allowed value over the widest possible output frequency range. Two basic techniques of control are in use.

Synchronous operation: In this method, the ratio of inverter switching to output frequency is required to be an integer number. It is therefore necessary to change the

ratio of switching to output frequency at discrete points in the output frequency range in order to ensure that the maximum permissible switching frequency is not exceeded (gear changing). With this mode of control, it is vital to adjust the switching patterns to make the fundamentals of the output voltage match on both sides of the frequency ratio transition. Otherwise, switching transients that can be very significant may appear when gear changing takes place. Due to technological advances in the fields of power semiconductors and the emergence of powerful yet affordable microprocessors, synchronous operation is today confined to few applications, typically at very high power levels and low switching frequencies (eg. traction). To achieve highly dynamic drives (eg. vector control), modern drive systems update reference voltage and frequency for every PWM sample so synchronous techniques cannot be employed for high performance drives. Large lookup tables are required to store information about the switching angles for each possible combination of modulation index and reference frequency.

Asynchronous operation: This method applies a fixed switching frequency over the whole output frequency range of the inverter. In this mode there is no need for a synchronization of inverter switching and output frequency. The ratio increases for decreasing output frequency and becomes a minimum at the maximum output frequency. Asynchronous operation is preferred over synchronous operation for a number of reasons:

- It allows to update reference voltage and frequency for every PWM sample, making highly dynamic operation possible.
- All firing instants are calculated in real time so no large lookup tables are required.
- No gear changing with the related transients occurs.

4.3.4 Space Vector PWM

The space vector modulation technique involves the vectorial decomposition of a desired voltage space vector $\vec{v}^*$ into voltage vectors that can be output by a typical three-phase inverter. Figure 4.10 shows all the voltage vectors that can be produced. Eight different states exist, including two null states where either all upper switches

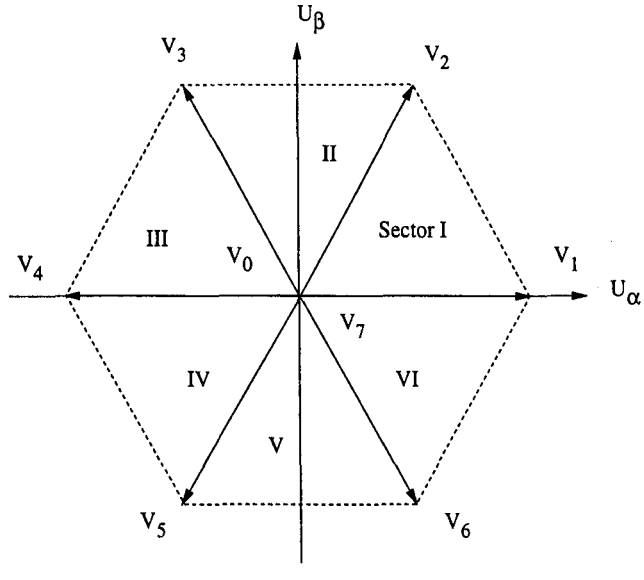


Figure 4.10: Inverter output voltage space vectors.

or all lower switches in a three-phase inverter are switched on.

Consider the case shown in Figure 4.11 where the reference voltage vector $\vec{v}^*$ lies in sector I. This voltage vector can be obtained by equating voltage-time integrals [28]:

$$\vec{v_1}T_1 + \vec{v_2}T_2 = \vec{v^*}T_s \tag{4.5}$$

The time T_0 for which a zero voltage vector has to be selected can then be obtained by:

$$T_0 = T_s - T_1 - T_2$$

The same equations can be applied to the remaining sectors of the reference voltage plane. A lookup table containing sine and cosine values for reference angles in the range of $(0 \leq \gamma \leq \pi/3)$ is sufficient to calculate the switching times for a complete output waveform period in space vector modulation.

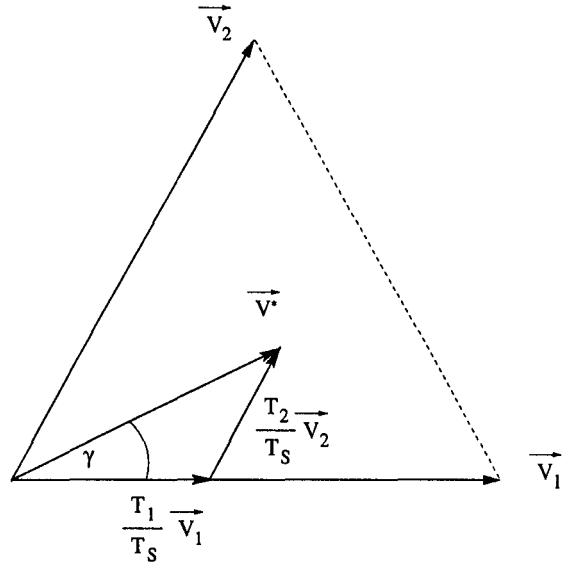


Figure 4.11: Derivation of switching times by decomposition of reference voltage vector.

The minimum switching frequency for each inverter leg is obtained when the transition from one inverter state to the following is carried out by switching only one inverter leg. This condition is met by starting from one zero state, then switching the two voltage vectors that are required to obtain $\vec{v}^*$ and finishing with the other zero state. Three output phase voltages for a minimum switching frequency sequence are plotted in Figure 4.12. The optimum switching sequences that result in minimum switching

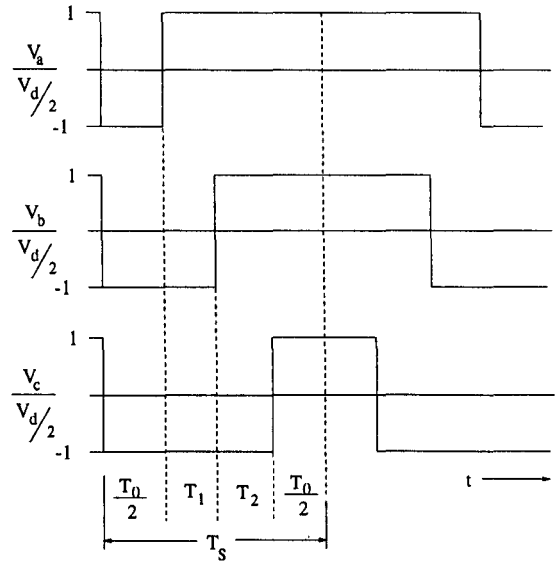


Figure 4.12: Minimum switching frequency pulse pattern of space vector PWM.

frequency for all sectors of the switching state plane are listed in Table 4.1. Note that

Sector	*Voltage vector sequence*							
I	v_0	v_1	v_2	v_7	v_7	v_2	v_1	v_0
II	v_0	v_3	v_2	v_7	v_7	v_2	v_3	v_0
III	v_0	v_3	v_4	v_7	v_7	v_4	v_3	v_0
IV	v_0	v_5	v_4	v_7	v_7	v_4	v_5	v_0
V	v_0	v_5	v_6	v_7	v_7	v_6	v_5	v_0
VI	v_0	v_1	v_6	v_7	v_7	v_6	v_1	v_0

Table 4.1: Voltage vector sequence for minimum switching frequency.

T_0 is shared evenly between v_0 and v_7 at the beginning of a switching period and the end respectively to obtain the optimum switching sequence shown in Figure 4.12.

It can be shown [27] that space vector modulation produces switching sequences that are equivalent to regular sampled asymmetric PWM waveforms produced with a modulating waveform V_{SVM}, given by

$$V_{SVM} = \begin{cases} \frac{3}{2}\sin(\omega t) & 0 \leq \omega t \leq \frac{\pi}{6} \\ \\ \frac{\sqrt{3}}{2}\sin\left(\omega t + \frac{\pi}{6}\right) & \frac{\pi}{6} \leq \omega t \leq \frac{\pi}{2} \end{cases} \tag{4.6}$$

The rest of the waveform can be derived from its quarter wave symmetry. A plot of V_{SVM} is given in Figure 4.13. To allow comparison with regular sampled PWM, the modulating waveform (curve b) is regarded as the sum of a desired fundamental sinewave component, (curve a), and a triangular third harmonic waveform, (curve c). By using Fourier analysis, the modulating waveform can then be expressed as [31]

$$V_{SVM} = m[\sin(\theta) + \Delta(\theta)] \tag{4.7}$$

where

$$\begin{aligned} \Delta(\theta) &= \sum_{r=0}^{\infty} \frac{1}{\sqrt{(3)}\pi} \frac{(-1)^r}{[(2r+1) - \frac{1}{3}][(2r+1) + \frac{1}{3}]} \sin[(2r+1)3\theta] \\ \theta &= \omega t + \phi \end{aligned} \tag{4.8}$$

The spectral qualities of regular sampled PWM are preserved in space vector PWM. From equation 4.8, we find that the amplitude of the third harmonic in V_{SVM} is

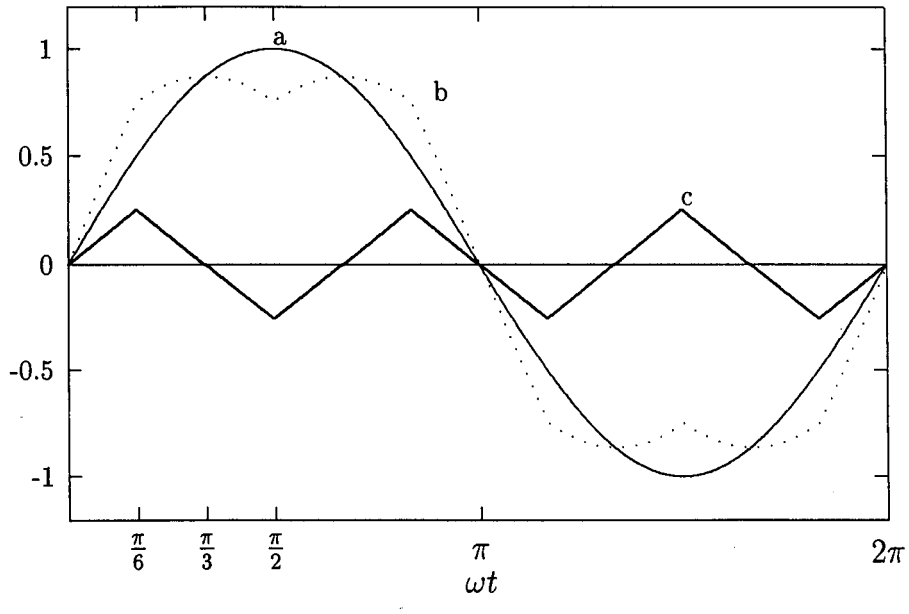


Figure 4.13: Space vector phase voltage components.

about 21% of the desired fundamental. The fundamental output voltage is increased by about 15% [26] and hence is the same as for regular sampled PWM with an added third harmonic of 25% of the fundamental. Figure 4.14 shows the line-to-line voltage spectrum for space vector modulation with the same conditions as in Figure 4.6. As expected, there are almost no differences between the two spectra.

To conclude this introduction to PWM, two definitions follow that play an important role in the analysis of PWM strategies:

1. overmodulation: For subharmonic modulation PWM without added third harmonic, overmodulation is reached when the modulation index is greater than one. The region where $m \leq 1$ is called linear region. For space vector modulation, overmodulation is reached when the reference vector exceeds the hexagon in Figure 4.10. This happens for $m > 1.15$.

2. six-step mode: In this mode, no commutation takes place in an output phase for 180 degrees of the reference waveform. The output voltage consists of unpulsed rectangular blocks. In terms of space vector modulation, the resulting output

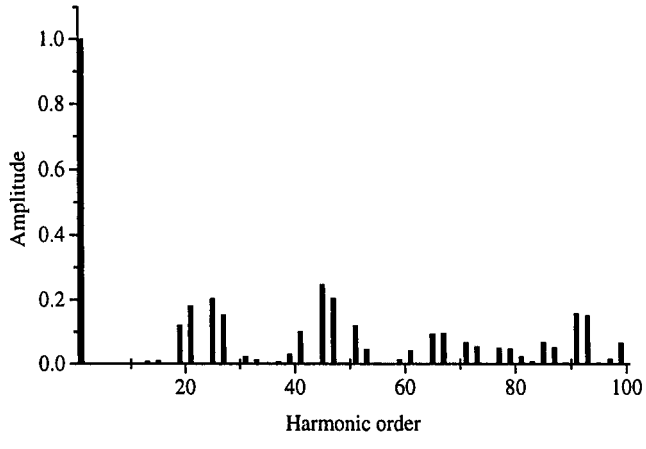


Figure 4.14: Line-to-line voltage spectrum of space vector PWM.

vector is placed at the position of an active vector for a sixth of the output waveform period.

4.4 Comparison of PWM and ΣΔM

As mentioned in Section 4.2.2, the energy contained in the subharmonic band is an undesired feature of ΣΔM [10]. Comparisons between PWM and ΣΔM have shown that comparable performance in terms of total harmonic distortion (THD) can be achieved with switching frequencies that are much higher than under PWM. The necessary ratio in switching frequency varies between different publications and ranges from a ratio of four [8] to ratios of about six [12]. Mertens finds in [12] that in the case of full bridge inverters where the zero state can be used, ΣΔM is always inferior for small modulation depth, but is superior at a modulation depth larger than 0.3 if the frequency ratio is greater than 5.6. A definitive result does not appear to have been reached in this matter since the analysis of ΣΔM is complicated due to the highly nonlinear spectral behaviour [11; 12].

As a conclusion, it can be stated that it would be desirable to combine the advantages

of soft-switching with those of pulse width modulation. Due to the absence of switching losses, this would also allow an increase in switching frequency under PWM, a factor that uniquely determines the quality of the output waveforms.

4.5 Modified PWM for PRDCL inverter

A number of modified PWM techniques for the PRDCL inverter and similar, soft-switching PWM inverters have been proposed [20, 21, 23, 32, 33]. Many of these approaches apply so-called two-phase switching, ie. only two phases are commutated during a sampling period. Other proposals include the application of variable sampling time to ensure that no pulses are created that are shorter than the minimum allowable pulsewidth. In the following, these techniques are reviewed and some simulation results are given. Firstly, the reasons why standard PWM cannot be applied with the PRDCL inverter are discussed. This leads to the development of a modified asynchronous space vector method that is well suited for the PRDCL inverter. It can ensure safe operation of the PRDCL circuit over the whole modulation range while it preserves all the positive characteristics of space vector modulation.

4.5.1 Considerations for PWM using the PRDCL inverter

From the operation of the PRDCL inverter that was explained in Section 3.3, we can derive some consequences for a suitable PWM strategy.

- There has to be a minimum dwell time between switching edges to ensure that the resonant link can be operated for each one.
- Space vector techniques have the inherent advantage of determining vector-on durations, ie. the distance between switching edges.

- Modern drive systems apply asynchronous PWM for instantaneous voltage and frequency control.

The first point shows one of the drawbacks of the PRDCL inverter. Every time a phase has to be commutated, the link voltage has to be brought down to zero, then the voltage is kept at this level for a safety margin to prevent shoot through in the inverter leg and finally the voltage is resonated back to supply level again. In order to ensure that this process can be completed for each switching edge in each phase, the switching times have to be kept at a minimum distance from each other. This is not the case in hard-switched PWM where each phase can switch whenever it is demanded by the modulation strategy.

In space vector modulation, vector-on times are computed which represent the distance (in time) between two switching edges in two different phases. Since it is exactly this quantity that needs to be controlled to ensure safe operation of the PRDCL inverter it makes sense to start with space vector techniques when looking for a modified strategy.

A number of synchronous PWM techniques for the PRDCL and similar inverter circuits have been published some of which will be presented in the following sections. However, as was already mentioned, asynchronous techniques represent the standard approach for modern drive systems and therefore synchronous strategies have to be discarded as impractical in high performance drives.

4.5.2 Two-phase switching

In the first publications about the PRDCL inverter as well as in similar inverter topologies, a modified space vector technique has been applied in which only two commutations occur in a sampling period [20, 21, 34]. The technique has been described in an earlier paper [32], where the main advantage was found to be its ease of implementation that made it possible to perform all the required operations in

a single chip microcontroller. The switching sequence for this so-called two-phase switching is **VaVbZVbVa** where Va and Vb are the two active vectors of a sector of the reference plane and Z represents a zero vector (V0 or V7). Figure 4.15

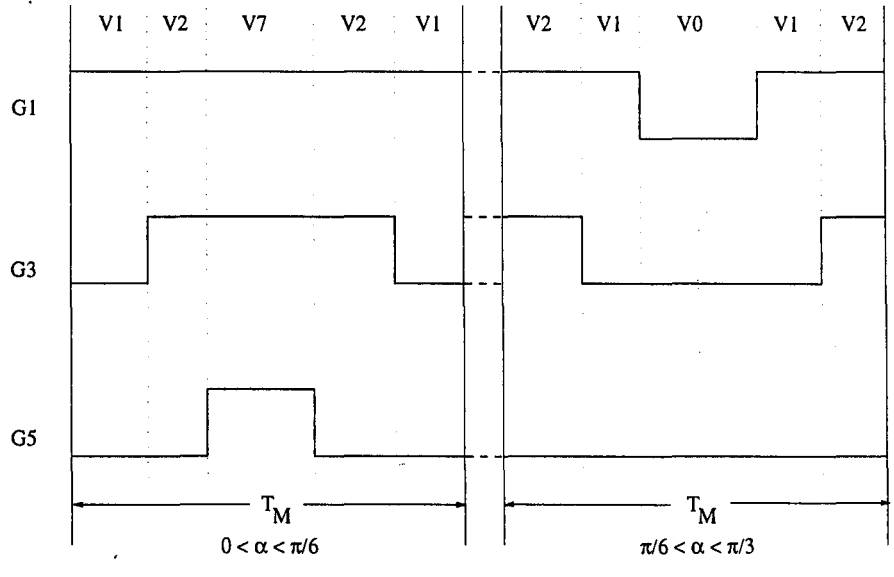


Figure 4.15: Gate signals for two-phase modulation.

shows the gate signals for two- phase modulation. As can be seen, one phase is not commutated during a sampling period T_M. The commutation rhythm is changed to **VbVaZVaVb** for $(\frac{\pi}{6} < \alpha < \frac{\pi}{3})$ to start the commutation sequence with the longer of the two active vectors. The obvious advantage of the technique when applied to the PRDCL inverter, is that the number of switchings is about 30 percent less than for the subharmonic modulation method (SHM) thus reducing the number of times that the resonant link has to be activated in a sampling period by 30%. The vector on-times can be calculated from the same equations (4.5) as for space vector modulation. In order to achieve good spectral performance it is important to make sure that there is an odd number of samples in each reference sector as can be seen from the spectra in Figure 4.16, making two-phase switching a synchronous PWM technique. The frequency ratio for odd number of samples per sector is 23 at unity modulation index to allow comparison with standard PWM (Figure 4.6). It can be seen that a number of additional lines appear in the spectrum compared to regular sampled PWM but most of the harmonics still occur around the switching frequency and integer multiples thereof. For even number of samples per sector however, the spectrum

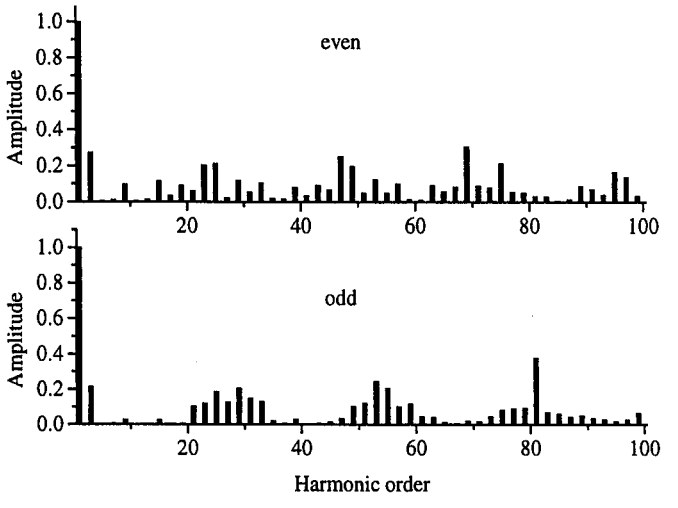


Figure 4.16: Phase voltage spectra for even and odd number of samples per reference sector.

contains harmonics over a wide frequency region and does no longer resemble the typical PWM output spectrum.

Single-phase soft-switching: In addition to two-phase switching, a technique known as single-phase soft switching has been used for the PRDCL inverter that was first described in [15]. Figure 4.17 shows the well known actively clamped resonant dc link converter, this time however with the bulk of the bus capacitor connected across the individual devices. The equivalent capacitance across the dc link during a resonant cycle is $3C_d$, where C_d is the capacitance across each individual inverter device. Whenever an active device has to be turned off, this can be done under soft switching conditions due to the presence of individual snubber capacitance. Say for instance that S_1 is conducting current and has to be turned off during a resonant cycle. The current is transferred to the capacitor across it and causes a rise in voltage until the diode D_4 in antiparallel with S_4 starts conducting. As a result of the snubber capacitance across the device, this turn-off can be regarded as a soft-switching event.

Applied to the PRDCL inverter, this principle allows the device to be switched off without initiating a resonant transition. This means that the minimum dwell time

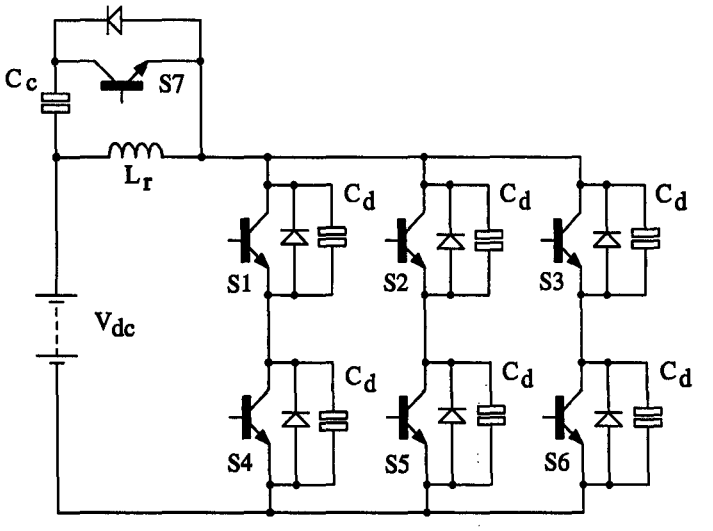


Figure 4.17: Schematic of three-phase actively clamped resonant dc link converter with resonant capacitor shared among all devices.

between switching edges can be made shorter, allowing a higher switching frequency with given resonant components and switching devices.

However, as later work on the switching behaviour of IGBTs under soft-switching conditions has shown, the assumptions made for this approach cannot be fully justified [40, 41]. The capacitor across a turning-off device can help to reduce the turn-off loss of an IGBT, but the subsequent current tail was found to be even longer than in the hard-switched case [40]. This tail current bump is a result of inadequate charge removal from the drift region and occurs under low dv/dt conditions. Under hard switching, the high dv/dt across the turning-off device helps to sweep these charge carriers out of the drift region but under zero-voltage-switching, this sweep-out mechanism is much smaller and the only other mechanism available for removing the charge carriers is recombination. The enhanced tail current leads to high turn-off losses that are dependent on the output dv/dt and the device temperature [42]. Hence, the turn-off according to this principle is not a lossless operation.

Research into the turn-on behaviour of IGBTs under zero voltage has shown that when the device begins to conduct, a voltage spike appears across it owing to an effect called 'dynamic saturation' [41]. This voltage will also appear across the parallel capacitor.

As a result, the energy stored in it will then be dissipated in the device leading to an oscillation with a magnitude depending on the size of the parallel capacitor. The turn-on loss resulting from this snubber dump can be very significant and large circulating currents can be set up between the snubber capacitor and the device package which may even overstress the device [42].

4.5.3 Space Vector PWM with variable sampling time

A PWM strategy that is suitable for application in the PRDCL inverter has to ensure that no pulses are created that cannot be produced due to the resonant link action required while at the same time voltage and frequency control are maintained as in the hard-switched PWM case. The pulsewidths that are produced by the modulation strategy are not the only criterion to be monitored though. In order to guarantee that all commutations occur under soft-switching conditions, the distances between switchings in different phases have to be controlled too. As an example let us assume that two pulses are required in phase a and b of a three-phase inverter that are both longer than the minimum pulsewidth that can be created by the PRDCL inverter. If the switching edges of these pulses are too close to each other to complete a resonant cycle for both, then the modulation algorithm has to modify the switching pattern to avoid this situation despite the fact that the pulses are longer than the minimum pulsewidth. In this context, the space vector technique has an inherent advantage over subharmonic modulation techniques because the result of equation (4.5) always gives the distance between two switching edges.

Consider the Space Vector technique as explained in Section 4.3.4. The values for T_0, T_1 and T_2 depend on the position of the reference vector within the voltage triangle in Figure 4.11. T_0 for instance will be shorter in the center of the triangle (reference angle close to $\pi/6$) than in the outer regions of the triangle. The active vectors on the other hand will be long when the reference vector is close to the respective active vector and short when it is close to the other active vector. Figure 4.18 shows a plot of the vector times T_0, T_1 and T_2 against the reference angle γ which extends from

0 to $\pi/3$ (see Figure 4.11). The switching frequency in this case is 2.25kHz with a modulating frequency of 50Hz and a modulation index of 1.15 which is just below overmodulation for space vector modulation. It can be seen that while T_0 becomes

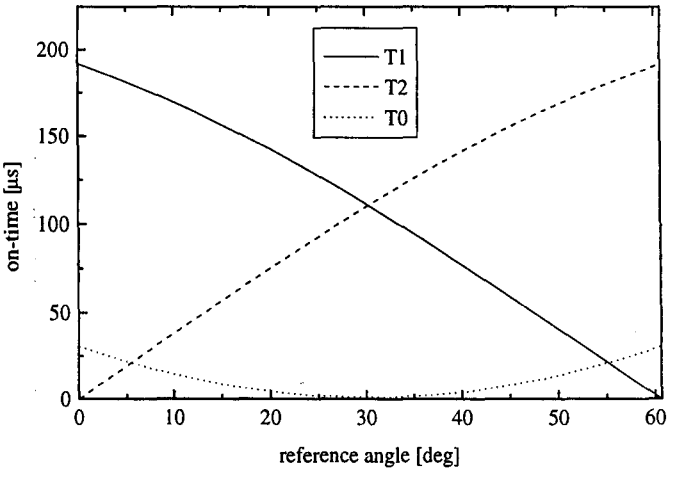


Figure 4.18: Plot of T_0, T_1 and T_2 in μs as functions of the reference angle γ (in degrees).

shortest in the center of a reference sector ($\gamma \approx \pi/6$), T_2 starts from zero for $\gamma = 0$ and T_1 becomes shortest for $\gamma = \pi/3$.

A technique also known as *Pulse Frequency Modulation* has been described in [33] that allows control of the minimum length of the zero voltage vector in space vector modulation (ie. T_0). The method applies a variable sampling time that can ensure that T_0 does not fall below a desired level. We introduce the sampling time ΔT as a function of the reference angle γ as

$$\Delta T = 1/(Nf)g(\gamma) \tag{4.9}$$

where N equals the number of output pulses per reference cycle. The function $g(\gamma)$ can be any function with a period being one sixth of the output modulation function period and a unity average value. To study the effects of this variable sampling time, consider the following control function $g(\gamma)$:

$$g(\gamma) = 1 + \zeta \cos(6\gamma) \tag{4.10}$$

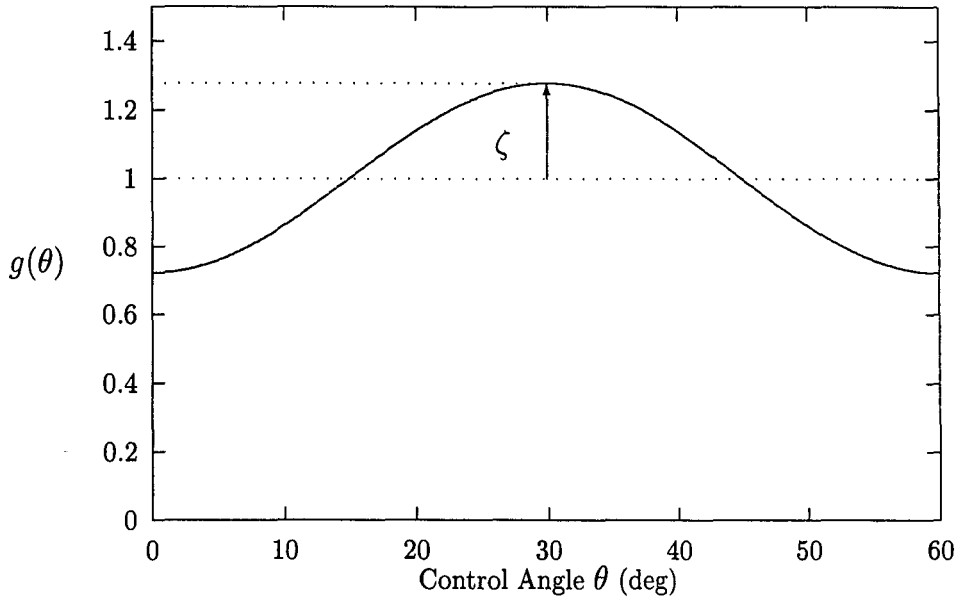


Figure 4.19: Modulation function for sampling interval.

where ζ is the modulation depth of the sampling interval function ($-1 < \zeta < 1$). As shown in Figure 4.19, a positive ζ leads to a shortening of ΔT around $\gamma = \pi/6$ whereas for a negative ζ, ΔT is lengthened in this region. In this way, a negative ζ results in values for T_0 that are longer around $\gamma = \pi/6$ than would be in the case of conventional space vector modulation. The result in Figure 4.19 was obtained with $\zeta = -0.278$. For $\zeta = 0$, pulse frequency modulation becomes normal pulse width modulation.

Figure 4.20 shows the line-to-line voltage spectrum of a simulation of space vector PWM with variable sampling time. The switching to fundamental output frequency ratio is 30, the modulation index $m = 1$ and the modulation depth of the sampling interval function $\zeta = -0.278$. A comparison with Figure 4.14 shows some additional lines in the spectrum but the general characteristics of space vector modulation can be found again in space vector modulation with variable sampling time.

The main drawback of the proposed method is that the number of output pulses per cycle has to be a multiple of six to maintain the symmetry of the 3-phase waveforms [33], ie. the scheme is synchronous and hence not practical for most systems as explained in Section 4.3.3. Furthermore, only T_0 can be controlled in this way while T_1

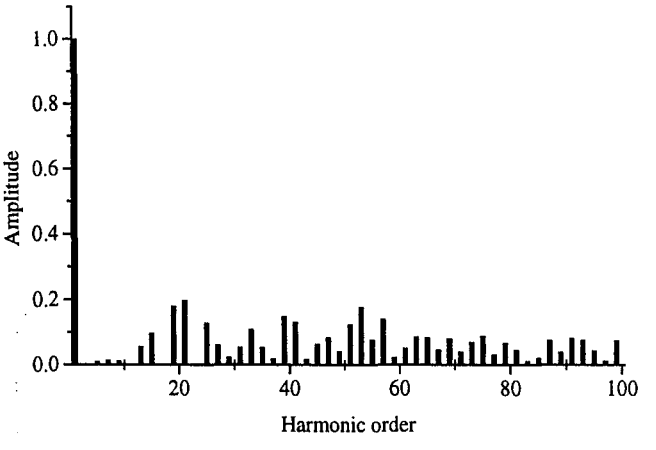


Figure 4.20: Line-to-line voltage spectrum of pulse frequency modulation.

and T_2 can still take on values that are too short to guarantee safe operation of the PRDCL inverter. This was the main motivation behind the modified space vector modulation explained in the following section.

In [21], the authors applied a combination of two-phase switching, variable sampling time and single-phase switching in order to keep the duty cycle for the resonant link low while ensuring that the minimum dwell time requirement is satisfied. All the disadvantages that were mentioned about the three techniques remain valid though which does not make this modulation strategy an attractive choice.

4.5.4 Space Vector PWM with vector dropping algorithm

A space vector PWM algorithm has been presented in [36] that allows a continuous transition to the six-step mode which is treated as a special case of single-phase modulation. A further modified version of this algorithm has been developed here to make it suitable for use with the PRDCL inverter. Vector on-durations are always calculated from the same set of equations (4.5), even in the overmodulation region. Control of the minimum pulsewidth t_{min} is achieved by controlling the on-time of the

zero-vector T_0. Over the whole modulation region, three situations can occur:

1. $t_{min} < T_0$: In this case, the reference vector can be composed using three vectors as explained in Section 4.3.4.

2. $0 < T_0 < t_{min}$: This means that the reference vector is still inside the hexagon (see Figure 4.10) and could in theory be implemented by using the three appropriate vectors as above. However, due to T_0 being shorter than t_{min} the pulsewidth becomes too short and the on-times of the vectors are changed as follows:

$$\begin{aligned} T_1' &= T_1 + T_0/2 \\ T_2' &= T_2 + T_0/2 \\ T_0' &= 0 \end{aligned} \tag{4.11}$$

3. $T_0 < 0$: The reference vector exceeds the hexagon (overmodulation) and in this case the following corrections are made:

$$\left.\begin{aligned} T_1' &= T_1 \\ T_2' &= T_2 + T_0 \\ T_0' &= 0 \end{aligned}\right\} \quad 0 \leq \alpha < \pi/6 \tag{4.12}$$

$$\left.\begin{aligned} T_1' &= T_1 + T_0 \\ T_2' &= T_2 \\ T_0' &= 0 \end{aligned}\right\} \quad \pi/6 \leq \alpha < \pi/3 \tag{4.13}$$

The minimum pulsewidth now depends on the shorter of the two active vector on-times. If the shorter of these two is less than t_{min}, additional corrections are required:

$$\left.\begin{aligned} T_1'' &= T_S \\ T_2'' &= 0 \\ T_0'' &= 0 \end{aligned}\right\} \quad 0 \leq \alpha < \pi/6 \tag{4.14}$$

$$\left.\begin{aligned} T_1'' &= 0 \\ T_2'' &= T_S \\ T_0'' &= 0 \end{aligned}\right\} \quad \pi/6 \leq \alpha < \pi/3 \tag{4.15}$$

With this correction no commutation occurs during the sampling time. The resulting vector is placed at the position of an active vector. This means, that the six-step mode has been reached. The corrections made in the second case ($0 < T_0 < t_{min}$) lead to a resulting vector with a length that is greater than the reference vector and an angular position that is shifted towards the middle of the sector (Figure 4.21). The corrections made in the third case ($T_0 < 0$) result in the shorter of the two active

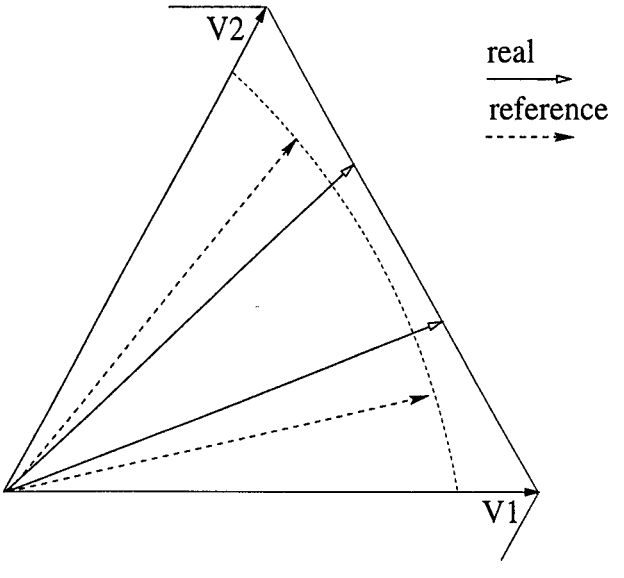


Figure 4.21: Vector positions for overmodulation when $0 < T_0 < t_{min}$.

vectors being shortened, while the longer one remains unchanged. For a reference angle of ($0 < \alpha < \pi/6$) the actual vector therefore lags the reference vector while it leads the desired vector for ($\pi/6 < \alpha < \pi/3$).

Modified version for PRDCL inverter: In order to implement this modified version of space vector PWM for the PRDCL inverter, the following facts have to be considered:

- The PRDCL inverter can only produce pulses that are not shorter than

$$t_{pw_{min}} = \frac{2L_r}{V_S}\sqrt{I_{omax}\left(\frac{V_S}{Z_r} + I_{omax}\right)} \tag{4.16}$$

- Short vector on-times have to be eliminated too, since they mean that the switching edges in two phases are very close to each other.

- In space vector pwm, short vector on-times occur

  1. For high modulation depths near the center of each sector of the hexagon (Figure 4.10) due to the short T_0.
  2. Near the boundaries between sectors either T_2 (reference vector has just entered sector) or T_1 (reference vector is about to leave sector) are very short, regardless of the instantaneous modulation depth.

A modified version of the algorithm with vector dropping described above was developed by the author that takes into consideration the requirements of the PRDCL inverter. The algorithm is an extension of the previous one and controls not only the size of T_0 but also the on-times T_1 and T_2. Let T_{min} the minimum allowable on-time of a voltage vector which is not the same as the previously used t_{min}, the minimum pulsewidth. The following shows which situations can occur and how the algorithm deals with them:

1. T_1 or T_2 too short: As explained above, this can happen when the reference vector comes to lie close to one of the boundaries of a sector. Two cases can be identified (equivalent for T_1 and T_2):

   - $T_{min}/2 < T_1 < T_{min}$: In this case, T_1 is prolonged to its minimum allowable value T_{min} and the added time will be subtracted from T_0 in a later step.
   - $T_1 < T_{min}/2$: This will lead to the dropping of T_1 and in a later step, T_0 will be increased by T_1.

2. T_0 too short: This will usually occur around the middle of a sector as explained earlier. This means, that except for overmodulation in a very high region ($m \approx 2.3$ according to [36]), T_1 and T_2 will be longer than T_{min}, if only after the above corrections. As can be seen in Figure 4.12, T_0 leads to a pulse that is carried over into the following sampling interval, so no actual switching occurs after $T_0/2$. In symmetric pwm, $T_0/2$ will be same in two subsequent sampling intervals while there may be a small difference between the two in the case of

asymmetric pwm. As regards correction of T_0, again the following two cases are considered:

- $T_{min}/2 < T_0 < T_{min}$: The algorithm extends T_0 to T_{min} and subtracts half of the amount needed from T_1 and the other half from T_2.
- $T_0 < T_{min}/2$: T_0 will be dropped and added to T_1 and T_2 in equal shares.

The above situations can be written formally:

1. T_1 or T_2 too short:

$$\left.\begin{aligned} T_1' &= T_{min} \\ T_2' &= T_2 \\ T_0' &= T_0 - (T_{min} - T_1) \end{aligned}\right\} \quad T_{min}/2 < T_1 < T_{min} \tag{4.17}$$

$$\left.\begin{aligned} T_1' &= 0 \\ T_2' &= T_2 \\ T_0' &= T_0 + T_1 \end{aligned}\right\} \quad T_1 < T_{min}/2 \tag{4.18}$$

2. T_0 too short:

$$\left.\begin{aligned} T_1' &= T_1 - (T_{min} - T_0)/2 \\ T_2' &= T_2 - (T_{min} - T_0)/2 \\ T_0' &= T_{min} \end{aligned}\right\} \quad T_{min}/2 < T_0 < T_{min} \tag{4.19}$$

$$\left.\begin{aligned} T_1' &= T_1 + T_0/2 \\ T_2' &= T_2 + T_0/2 \\ T_0' &= 0 \end{aligned}\right\} \quad T_0 < T_{min}/2 \tag{4.20}$$

These corrections will affect the resulting length and position of the output voltage vector as follows (see Figure 4.22):

1. T_1 or T_2 too short:

- $T_{min}/2 < T_1 < T_{min}$: The resulting vector will be longer than the reference vector and pushed towards the boundary of the reference voltage sector that represents the vector whose on-time was extended.
- $T_1 < T_{min}/2$: The switched vector will be shorter than the reference vector and pushed towards the center of the voltage triangle.

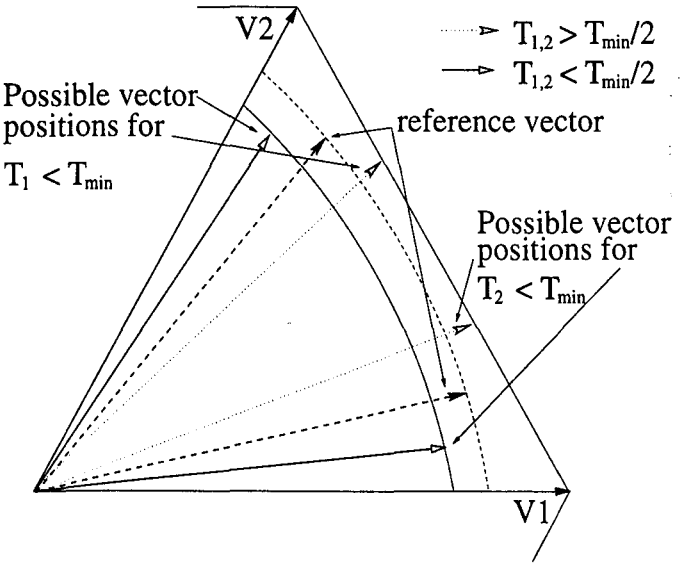


Figure 4.22: Consequences of T_1 or T_2 being too short.

2. T_0 too short (see Figure 4.23):
   - $T_{min}/2 < T_0 < T_{min}$: The modifications that are possible in this case lead to a vector that is shorter than the reference vector and an angular position that is changed in different ways, depending on the location of the reference vector within a sector. The extra time required to increase T_0 to T_{min} is taken to equal shares off T_1 and T_2. Therefore, if T_1 is longer than T_2, the resulting vector will be pushed towards the boundary of the voltage triangle that represents $\vec{v_1}$ and vice versa for $T_2 > T_1$. For the case that $T_1 = T_2$ ($\alpha = \pi/6$), the angular position remains unchanged.
   - $T_0 < T_{min}/2$: In this case, the resultant vector will be longer than the reference vector and the angular position will be pushed towards the boundary that represents the shorter of the two active vectors.

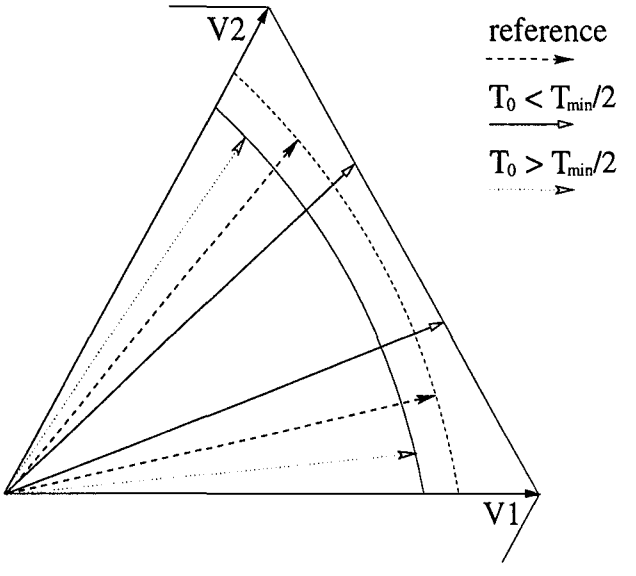


Figure 4.23: Consequences of T_0 being too short.

Note, that the removal of short vector on-times also means that no pulses are produced that are shorter than $T_{min}/2$ so that no extra pulse dropping is required after the vector on-times have been corrected.

To demonstrate the consequences of the modulation strategy on the vector on-times T_0, T_1 and $T2$, consider Figure 4.24 that shows a plot of the modified on-times and for comparison the vector on-times for normal space vector modulation. It can be seen how for instance the short vector on-time T_2 at the beginning of a reference sector leads to modifications to T_0 while T_1 is modified at the end of a reference sector (angle $\approx \pi/3$). Note that both T_1 and T_2 are either set to zero and hence dropped or extended to the minimum vector on-time T_{min} of 20μs.

A simulation of this modified space vector algorithm has been developed and the resulting line-to-line voltage spectrum is shown in Figure 4.25. To make comparison with the original space vector results easy, the results for normal space vector modulation are plotted in the same figure. For better visibility of the additional lines in the spectrum, the fundamental component is not shown. The carrier to output frequency ratio for both modulation strategies is 43 at unity modulation index. The minimum on-time for a voltage vector amounts to 8.6% of the PWM sampling period. There are hardly any differences between the two spectra, hence the modified space vector

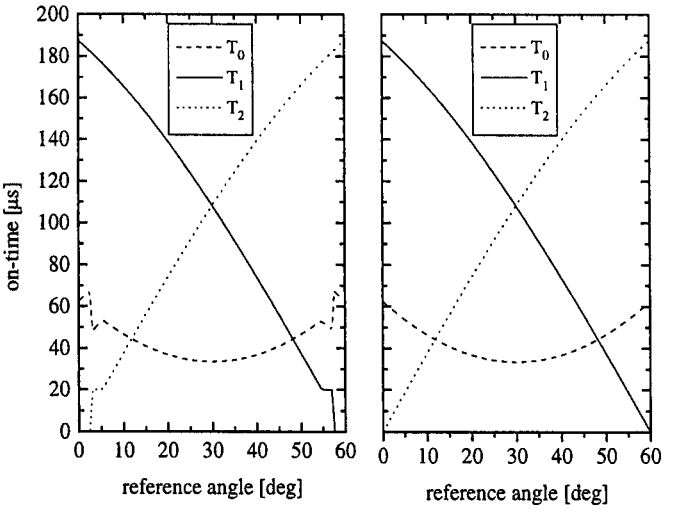


Figure 4.24: Effect of modification on vector on-times for 2kHz switching frequency, 50Hz output frequency and $T_{min} = 20\mu$s at unity modulation index. Left: modified; right: normal space vector modulation.

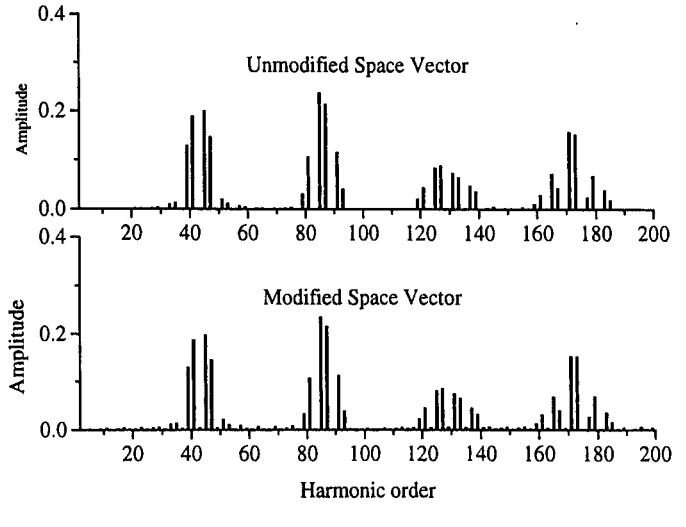


Figure 4.25: Line-to-line voltage spectrum for normal and modified space vector modulation; fundamental component not shown.

algorithm can be regarded as a viable modulation strategy for the PRDCL inverter with an output waveform quality similar to that of space vector modulation.

A distortion factor analysis has been carried out for the modified space vector modulation with different ratios of T_{min} to the PWM sample length. It is intuitive that the spectral performance will deteriorate when this ratio is increased. For the analysis, a computer program has been developed that outputs the phase voltages for various types of PWM methods including the one with vector dropping. For this analysis, the distortion factor is defined by

$$DF = \frac{1}{V_1}\sqrt{\sum_{k=2}^{\infty}\left(\frac{V_k}{k}\right)^2} \times 100\% \tag{4.21}$$

where V_k is the k-th harmonic voltage component. Shown below is a plot of the distortion factor for ratios of T_{min} to sample length from 4% to 20%. The ratio of modulation index to output frequency is kept constant (constant V/f). According to

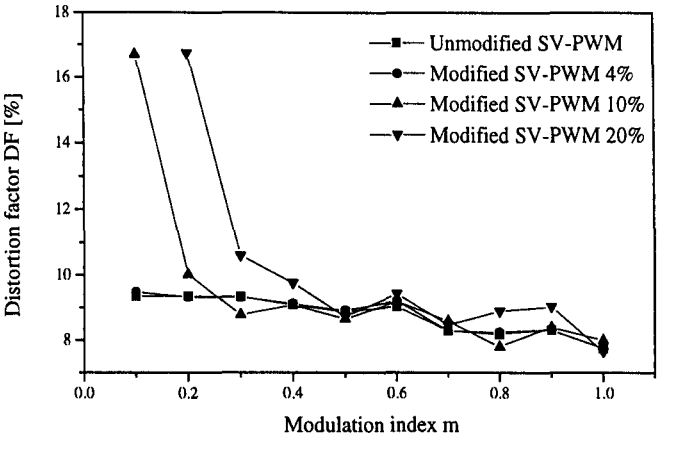


Figure 4.26: Distortion factor for different ratios of T_{min} to PWM sample length.

Figure 4.26, the distortion factor is nearly unchanged for low ratios of T_{min} to sample length while it becomes unacceptably large for higher ratios and at low modulation depths. The proposed modulation strategy is therefore a good choice provided the resonant link transitions can be made short enough to allow a sufficiently short value

for T_{min}. Device switching times as well as target switching frequency are determining factors in this context.

4.6 Loss of fundamental output voltage

As already mentioned in Section 3.3.5, the zero voltage gaps appear in every phase voltage whenever a switching event takes place. This inevitably leads to a reduced output voltage. In order to examine the effect on the amplitude of the fundamental output voltage component, a simulation was developed that calculates the output voltages of the PRDCL inverter, taking into account the zero voltage gaps. The results of the simulation shown in Figure 4.27 are for a PRDCL inverter using the components given in Table 3.2. The resonant transition used in the simulation is for a present and future load current of 5A which are both regarded to be constant for a whole PWM output period. While this does not represent a realistic situation the results are still expected to be accurate since the real resonant transition frequency will vary around a mean value which in this case is 71kHz (resonant transition time 14.1μs). As can be seen from the results, the fundamental component is indeed smaller

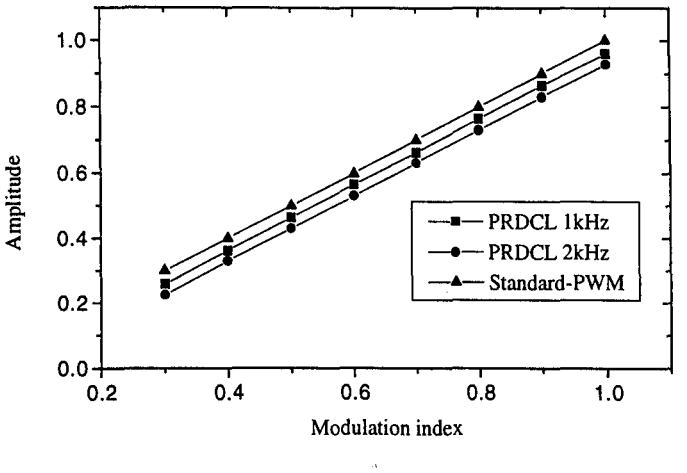


Figure 4.27: Amplitude of fundamental component for standard PWM and PRDCL PWM.

than for standard (hard-switched) PWM. As can be expected, the effect becomes more pronounced for increasing switching frequencies. The results are obtained for a constant V/f modulation and the loss of fundamental is seen to be constant over the modulation range. For a switching frequency of 1kHz, the fundamental component is about 4% smaller than for standard PWM while the reduction increases to about 7% for 2kHZ switching frequency. This loss of fundamental is an inherent weakness of the PRDCL inverter and similar systems. The magnitude of the loss of fundamental output voltage obviously depends on the time that the resonant transition takes in relation to the switching frequency and thus on the speed of the switching devices that are used.

4.7 Summary

In this chapter a number of modulation techniques were described and their respective performances were compared. It was shown that the well known PWM techniques produce superior output waveform quality compared to discrete modulation techniques like $\Sigma\Delta$ modulation. However, the application of PWM techniques in soft-switching inverters is not a straightforward task. Various modified PWM techniques have been presented in the literature some of which were presented and compared in Section 4.5. It was shown that these techniques are usually synchronous and, owing to the modifications they apply to the PWM output patterns, lead to spectral performances that are inferior to standard PWM. A space vector modulation technique with vector dropping was therefore developed and verified by simulation. The modified space vector technique is asynchronous and shows a spectral performance that is comparable to unmodified space vector modulation as long as the minimum vector on-time stays within reasonable limits. The technique is fully compatible with the working principle of the PRDCL inverter and similar systems and is very easy to implement. It is therefore regarded as a viable modulation strategy for the PRDCL and similar inverters with an output quality that can rival that of unmodified space vector modulation.

Chapter 5

Loss analysis

5.1 Introduction

This chapter analyses the losses in the PRDCL PWM inverter and compares them to those in a conventional hard-switched system. The semiconductor losses in an inverter can be split up in switching losses and conduction losses. The first section briefly describes the switching behaviour of IGBTs to illustrate the loss mechanisms that occur under hard-switching and soft-switching. We will then derive expressions for the conduction losses that occur in both hard-switching and soft-switching PWM inverters. The additional losses that stem from the introduction of the PRDCL circuit into the inverter system will be evaluated in Section 5.4.2. Finally, the respective merits and shortcomings of the PRDCL system and conventional inverters are compared.

5.2 Switching characteristics of IGBTs

The insulated gate bipolar transistor (IGBT) stems from the desire to combine characteristics of MOSFETs (fast switching times, voltage controlled) with the lower con-

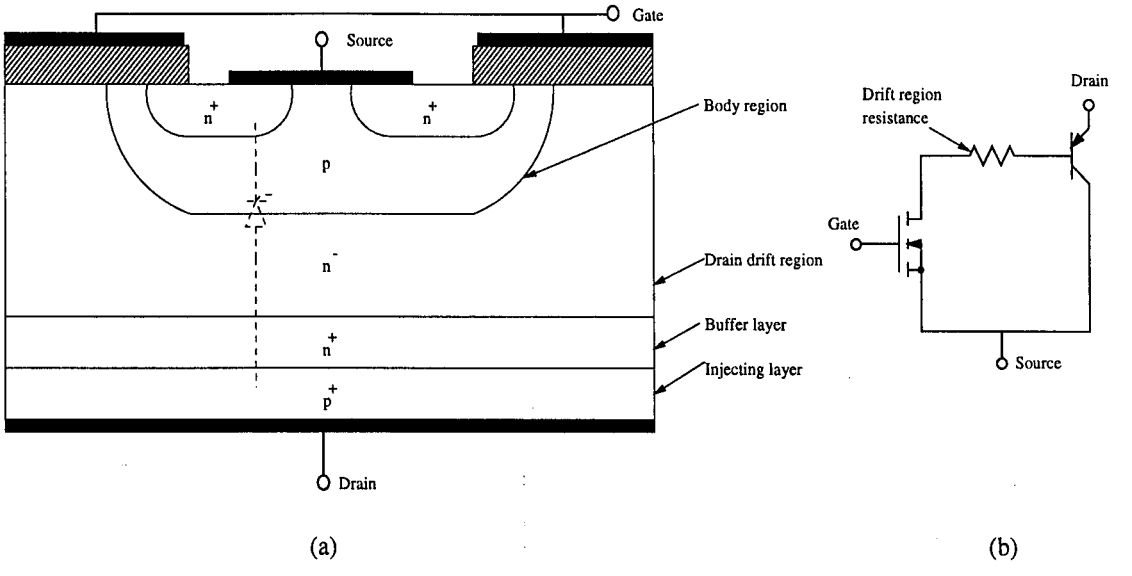


Figure 5.1: (a) Vertical cross section of an IGBT; (b) equivalent circuit for the IGBT.

duction losses of BJTs. The vertical structure of an IGBT is shown in Figure 5.1(a) and an equivalent circuit model is given in Figure 5.1(b). It consists of a Darlington circuit with a *pnp* transistor as the main transistor and a MOSFET as the driving transistor. The switching characteristics of the IGBT can be explained on the basis of this equivalent circuit.

5.2.1 Hard switching

Turn-on transient: Figure 5.2 shows idealised waveforms of drain current i_D and drain-source voltage v_{DS} for the turn-on transient of an IGBT with input voltage V_d and load current I_o [37]. It is assumed that the IGBT is feeding an inductive load with a freewheeling diode. In order to keep the analysis simple at this point, the diode is assumed to be ideal with no reverse-recovery current. In practice however, the reverse-recovery process is responsible for a large portion of the turn-on losses. Initially, while the gate-source voltage v_{GS} begins to rise, there is a turn-on delay time $t_{d(on)}$ until the threshold voltage $V_{GS(th)}$ of the MOSFET portion of the IGBT is reached. After that, the load current begins to rise sharply. The time that it takes for the current to build up from zero to I_o is the current rise time t_{ri}. The rise of gate-

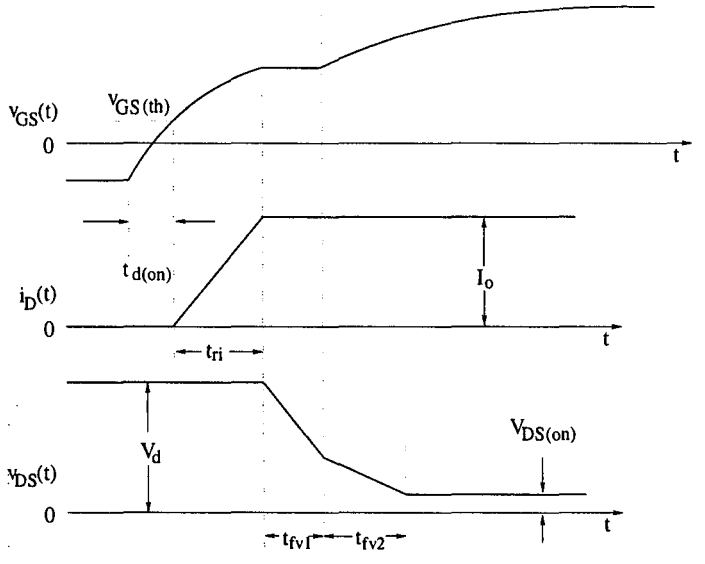


Figure 5.2: Voltage and current waveforms for IGBT turn-on.

source voltage v_{GS} is exponential, owing mainly to the gate-source capacitance of the IGBT C_{GS} and the resistance between gate driver and gate (usually some resistance is deliberately placed there to avoid high-frequency oscillations). When the drain current has reached I_o, the drain-source voltage begins to fall in two distinct time intervals t_{fv1} and t_{fv2}. The first part corresponds to the MOSFET portion of the IGBT turning on. The final on-state value of v_{DS} is only reached after t_{fv2}, when the bipolar portion of the IGBT has fully turned on. During t_{fv1}, the gate-source voltage is clamped to V_{GS,I_o}, the value that is required to maintain a drain current of I_o. When the MOSFET portion of the IGBT has turned on (after t_{fv1}) the gate-source voltage becomes unclamped and continues its growth to the gate drive supply voltage. Switching power losses occur due to the overlap of current and voltage in the device during t_{ri}, t_{fv1} and t_{fv2}.

Turn-off transient: The voltage and current waveforms for the turn-off transient are shown in Figure 5.3. Three distinct intervals can be distinguished. The turn-off delay time $t_{d(off)}$ and the subsequent voltage rise time t_{rv} are governed by the MOSFET part of the IGBT. The turn-off delay time $t_{d(off)}$ represents the time that the driver circuit requires to lower the gate-source voltage sufficiently to induce a decrease in drain current. After that, the first of two distinct current-fall intervals

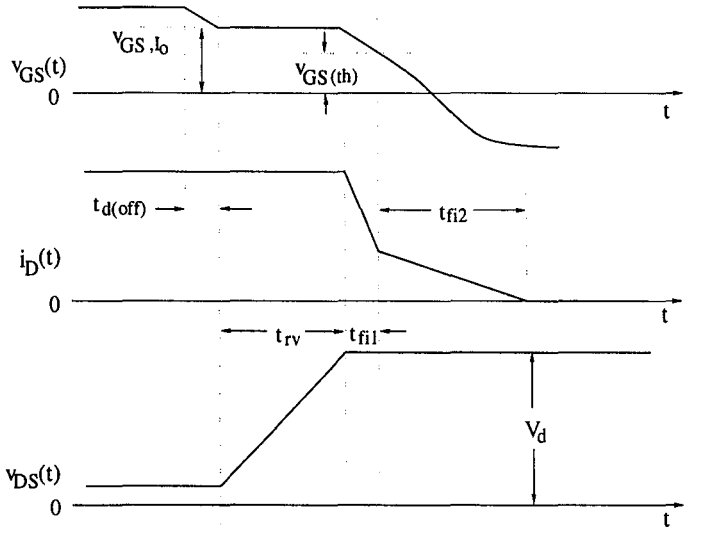


Figure 5.3: Voltage and current waveforms for IGBT turn-off.

starts. The current falls sharply during t_{fi1}, corresponding to the MOSFET part switching off. The subsequent "tail current" during t_{fi2} occurs as a result of stored charge in the bipolar section of the IGBT. With the MOSFET section being off and no reverse voltage applied to the IGBT, there is no possibility for removing the stored charges by carrier sweep-out [37]. Instead, the only mechanism that is available to get rid of the stored charge carriers is by recombination within the IGBT. In order to achieve low on-state voltage drop, the lifetime of these excess-carriers has to be large which corresponds to long t_{fi2} intervals. This however is undesirable since the power dissipation in the IGBT will be high during this interval with the voltage having reached its off-state value. A trade-off between on-state losses and fast turn-off times has to be made in the design process of an IGBT, as for other minority-carrier devices such as BJTs and thyristors. Switching power losses occur due to simultaneous presence of current and voltage in the device during t_{rv}, t_{fi1} and t_{fi2}.

5.2.2 Soft-switching

Zero-voltage switching

Due to the rising interest of researchers in soft-switching inverter topologies, the switching behaviour of IGBTs under zero voltage switching condition has been the subject of a number of publications [40–43]. Various unexpected and undesired characteristics have been observed for both zero-voltage switching (ZVS) and zero-current switching (ZCS) that could not be predicted from manufacturer's data sheets. The following characteristics that deviate from the predicted behaviour were found for ZVS:

- At turn-on, the IGBT exhibits an additional conduction loss component which is dependent on the di/dt in the device. Resulting voltage drops of 6–10V were observed which cannot be accounted for by the amount of inherent package and circuit parasitic inductance present. The underlying effect has been termed "conductivity modulation lag" and was found to be sensitive to temperature too [41]. The conductivity modulation lag was explained as follows: During turn-on, the injection of minority carriers into the base of the bipolar section within the IGBT lags behind the rate at which drift region conductivity can be modulated. This results in an inductive behaviour leading to excessive forward voltage drops.

  The dynamic voltage saturation spike at turn-on means that if any snubber capacitance C_r is present across the device, energy will be stored in it and dissipated in the device, leading to an oscillation. For larger values of C_r there will be a larger oscillation with the possibility of overstressing and destroying the device.

- At turn-off, the current waveform exhibits a tail current "bump" that was found to be larger than under hard-switching conditions [40]. This tail current bump is a result of inadequate charge removal from the drift region. The phenomenon

occurs under low dv/dt conditions particularly for high temperatures [42]. Under hard switching, the high dv/dt at turn-off helps to sweep these charge carriers out of the drift region but under ZVS, this sweep-out mechanism is much smaller and the only other mechanism available for removing the charge carriers is recombination.

The enhanced tail current limits the available switching frequency of the device and introduces power loss during the turn-off transient that depends on the output dv/dt and the temperature. An important factor in determining the turn-off losses of an IGBT was found to be the carrier lifetime τ_{hl}. While the drift-region resistivity (the quantity that determines the forward conduction voltage drop of an IGBT) decreases with increasing values of τ_{hl}, the turn-off losses that are due to the tail current bump increase with carrier lifetime [41]. The higher losses mainly result from an increase in stored charge that has to be drained during the turn-off transient, ie. an elevated tail current.

Zero-current switching

The switching behaviour under zero-current switching was experimentally analysed in [40] and [44]. The following results were obtained.

- Turn-on Losses: Turn-on loss in a zero-current switching IGBT was found to be much reduced compared to hard switching [44]. In a conventional PWM inverter, the reverse recovery of the antiparallel diode plays an important role in determining the turn-on loss. In a resonant converter, this problem will be much reduced because the recovery process is smoothed owing to the presence of a resonant inductor in the circuit. In the PRDCL circuit, only S_2 and S_3 are switched on in a zero-current situation. For these switches, the problem of reverse recovery does not exist since they are not supplied with antiparallel diodes. However, a significant overlap of current and voltage was observed during turn-on in [44] owing to parasitic inductance of the IGBT package and

the already mentioned dynamic saturation which occurs under both ZVS and ZCS.

- Turn-off losses: Two loss mechanisms occur during the hard turn-off process of an IGBT, the overlap between switch voltage and current and the loss due to the tail current. When using ZCS, the overlap between the switch voltage and current is eliminated, so the loss attributed to the overlap is non-existent. The soft reduction of the IGBT collector current leads to reduced levels of minority carriers in the IGBT and the remaining carriers can be recombined in less time than for the hard-switched case. As a result, the tail current and the corresponding turn-off loss is significantly reduced. It was found that the turn-off losses are reduced by about two-thirds and twofold for slow and fast devices respectively [40].

5.3 Switching loss

5.3.1 Inverter switching loss

The IGBT modules used in the inverter side of the PRDCL system are Mitsubishi's CM100DY-24H. To evaluate their switching power loss, the manufacturer's data book [58] recommends the following equation:

$$\begin{aligned} P_{\text{SW}} &= \left(E_{\text{SW(on)}} + E_{\text{SW(off)}}\right) f_{\text{sw}} \frac{1}{2\pi} \int_0^{\pi} \sin x dx \\ &= \left(E_{\text{SW(on)}} + E_{\text{SW(off)}}\right) f_{\text{sw}} \frac{1}{\pi} \end{aligned} \tag{5.1}$$

$E_{\text{SW(on)}}$ and $E_{\text{SW(off)}}$ are the turn-on and turn-off switching loss respectively per IGBT pulse. Their values can be read from graphs plotted against collector current. Equation 5.1 shows that the switching losses are a linear function of the switching frequency f_{sw}.

5.3.2 PRDCL switching loss

The loss mechanisms described in Section 5.2.2 are expected to occur in the PRDCL devices. However, they are difficult to quantify and mathematical models to predict these losses have not yet been developed. Therefore, they will not be considered in the following analysis. The influence of this simplification will be seen in any discrepancies between predicted and measured losses.

5.4 Conduction loss

Conduction losses occur due to the forward voltage drop across conducting transistors and diodes. These losses are functions of the current that is flowing through the device. The voltage drops can be approximated by linear functions:

$$v_{T_{drop}} = V_T + R_T i_T \tag{5.2}$$

$$v_{D_{drop}} = V_D + R_D i_D \tag{5.3}$$

V_T and V_D are constant voltage components (threshold voltages) and R_T and R_D represent the equivalent resistances of the resistive voltage drop across transistor and diode respectively. With these expressions, the instantaneous conduction loss in transistor and diode can be expressed as

$$p_T = v_{T_{drop}} i_T = V_T i_T + R_T i_T^2 \tag{5.4}$$

$$p_D = v_{D_{drop}} i_D = V_D i_D + R_D i_D^2 \tag{5.5}$$

5.4.1 Inverter conduction loss

In order to obtain the conduction loss in a three-phase inverter, it is required to know the current through each device for all the periods during which each device is conducting. The conduction times however are dependent on the modulation index

and strategy as well as the load power factor. To simplify conduction loss analysis, a method based on probabilities was described in [47]. The method evaluates the probability of a transistor in an inverter leg receiving an on-signal. Consider the single-phase inverter shown in Figure 5.4. The load is assumed to consist of a counter EMF in series with a resistor and an inductor.

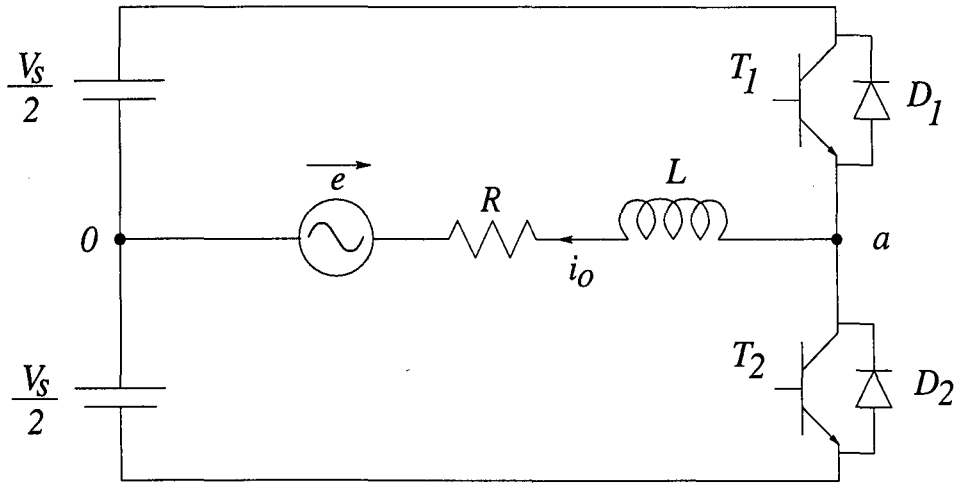


Figure 5.4: Single-phase inverter.

The probability of receiving an on-signal is derived from the average phase-to-midpoint voltage that is required to produce a reference current i_{ref}. Let us assume that the switching frequency is sufficiently high compared with the inverter output frequency, and that the average value $\bar{i_o}$ of the load current (average taken over a short period) is the same as the reference current.

$$\bar{i_o} = i_{ref} = \sqrt{2} I_{ref} \sin(\omega_{ref} t - \phi) \tag{5.6}$$

I_{ref} is the RMS value and ϕ the phase angle of the reference current respectively. To produce this reference current, the phase-to-midpoint voltage v_{a0} should have an average value given by

$$\bar{v}_{a0} = e + \sqrt{2} I_{ref} Z_L \sin(\omega_{ref} t - \phi + \Theta) \tag{5.7}$$

In this equation, Z_L denotes the load impedance $Z_L = \sqrt{R^2 + (\omega_{ref} L)^2}$, Θ the load power factor and e the back EMF generated by the load. The back EMF is usually

a sinusoidal voltage, so $\bar{v}_{a0}$ can be expressed in the form

$$\bar{v}_{a0} = k\frac{V_S}{2}\sin\omega_{ref}t \tag{5.8}$$

where k is the modulation index. When for instance the average value of the output voltage is zero, both transistors in an inverter leg have equal probabilities of receiving on-signals, hence

$$P_{T_1ON} = P_{T_2ON} = \frac{1}{2} \tag{5.9}$$

where P_{T_1ON} denotes the probability of T_1 being fired. On the other hand, if the inverter were to produce the maximum possible average value of output voltage ($\frac{V_S}{2}$), the probabilities would have to be

$$P_{T_1ON} = 1 \quad \text{and} \quad P_{T_2ON} = 0 \tag{5.10}$$

In general, the probabilities of T_1 and T_2 receiving on-signals are related to the average output voltage $\bar{v}_{a0}$ by

$$P_{T_1ON} = \frac{1}{2} + \frac{1}{2}\frac{\bar{v}_{a0}}{V_S/2} \tag{5.11}$$

$$P_{T_2ON} = \frac{1}{2} - \frac{1}{2}\frac{\bar{v}_{a0}}{V_S/2} \tag{5.12}$$

The direction of the load current i_o determines which device will actually carry the load current when an on-signal is received for instance by T_1. Suppose the load current is positive. When T_1 receives an on-signal, current will flow through T_1. When T_1 receives an off-signal (ie. T_2 receives an on-signal) current will flow through D_2. So for positive i_o, we can obtain the conduction loss for T_1 and D_2 as

$$p_{T_1} = P_{T_1on}\left(V_T i_{ref} + R_T i_{ref}^2\right) \tag{5.13}$$

$$p_{D_2} = P_{T_2on}\left(V_D i_{ref} + R_D i_{ref}^2\right) \tag{5.14}$$

For a sinusoidal reference current, i_o will be equally long positive and negative. The average value of conduction loss for T_1 and D_2 for one output cycle can therefore be obtained by integration of (5.13) and (5.14) over half an inverter output period as

$$P_{T_1} = \frac{1}{2\pi}\int_{\phi}^{\pi+\phi} P_{T_1on}\left(V_T i_{ref} + R_T i_{ref}^2\right) d(\omega_{ref}t) \tag{5.15}$$

$$P_{D_2} = \frac{1}{2\pi}\int_{\phi}^{\pi+\phi} P_{T_2on}\left(V_D i_{ref} + R_D i_{ref}^2\right) d(\omega_{ref}t) \tag{5.16}$$

To obtain the total conduction loss for a three-phase inverter we have to sum up the conduction losses for T_1 and D_2 and multiply the result by the number of devices in the inverter:

$$P_{cd} = 6\,(P_{T_1} + P_{D_2}) \tag{5.17}$$

For the case of three-phase PWM inverters with sinusoidal reference currents, the average value of phase-to-midpoint voltage for example in phase a is given by Equation 5.8. As was shown in Section 4.3.4, the modulating waveform (average phase-to-midpoint voltage) of space vector modulation can be expressed as a sum of sinusoids, so the technique described here can be extended to obtain the conduction loss for space vector modulation. The resulting expressions are given in Appendix D.

Figure 5.5 shows the sum of switching and conduction losses plotted against switching frequency for a load power factor of 0.67 (inductive) and 6A peak output current at a modulation index of k= 0.96. The sum of switching and conduction losses can be

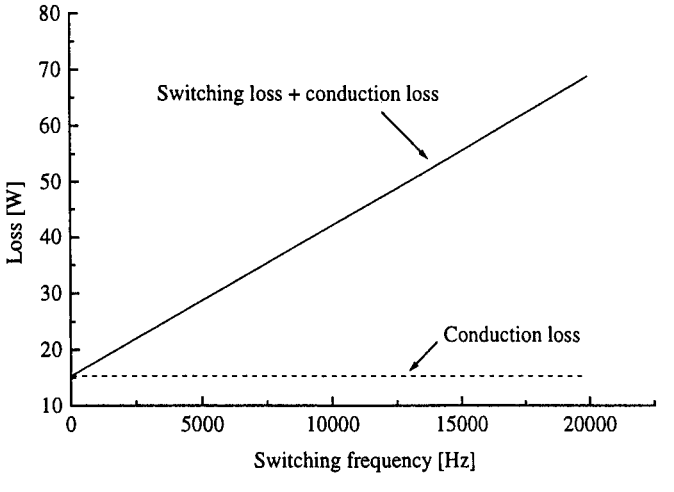


Figure 5.5: Switching and conduction losses for space vector modulation.

seen to be a linear function of switching frequency while the conduction loss stays constant.

5.4.2 Conduction loss introduced by PRDCL circuit

The conduction loss in a PRDCL inverter system is higher than that of a conventional PWM inverter due to the introduction of additional semiconductor devices and resonant components L_r and C_r. In order to achieve good output waveform quality, the resonant transition frequency has to be chosen much higher than the inverter switching frequency. Therefore, the additional conduction loss can be accounted for mainly by the presence of S_1 which has to conduct the full load current plus the initial current during a resonant transition. A very simplified approach to evaluating the additional loss can be developed using the following assumptions [17]:

- all devices have equal voltage drops given by (5.2),
- the conduction loss introduced by the resonant transition is negligible and
- at any point in time (other than during a commutation), three inverter devices are conducting current (transistors or diodes).

Given below is the equivalent circuit for the PRDCL inverter system based on the above assumptions. The three resistances R_T of the main inverter devices can be

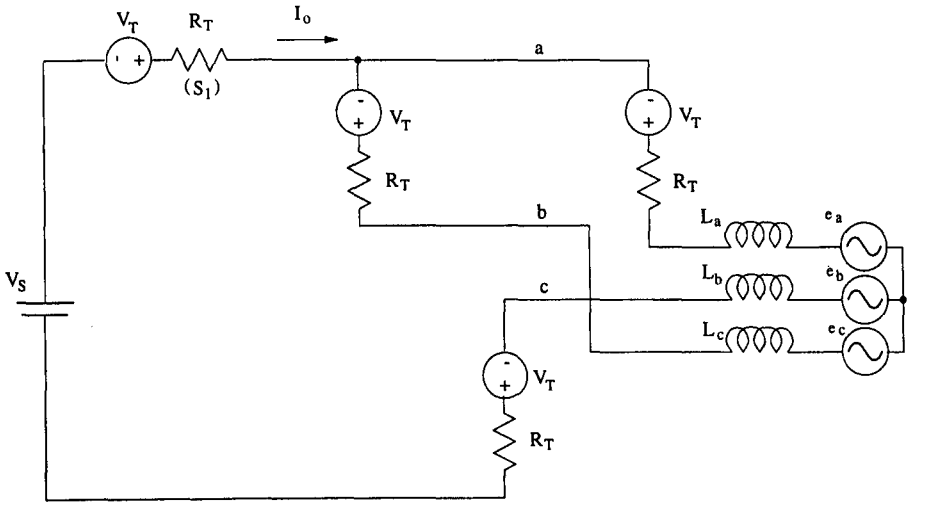


Figure 5.6: Equivalent circuit for conduction loss evaluation.

combined to $R_t = 1.5R_T$ while the constant voltage drops add up to $V_t = 2V_T$. The

conduction loss in a conventional PWM inverter can then be written as the sum of a resistive component P_{R_T} and of a component P_{V_T} that is due to the constant voltage drops:

$$I_o^2 R_t + I_o V_t = \underbrace{1.5 I_o^2 R_T}_{P_{R_T}} + \underbrace{2 I_o V_T}_{P_{V_T}} \tag{5.18}$$

The conduction loss in the PRDCL inverter is given by

$$I_o^2 R_t + I_o V_t = \underbrace{2.5 I_o^2 R_T}_{P_{R_T}} + \underbrace{3 I_o V_T}_{P_{V_T}} \tag{5.19}$$

Hence this rather crude first approach results in a resistive loss component that is 66% greater than for a conventional inverter and a constant voltage drop component that is increased by 50%.

The IGBT used for S_1 is an IRGPC50F for which the manufacturer's data book [57] recommends the use of the following conduction model to evaluate conduction loss:

$$\begin{aligned} v_{T_{drop}} &= V_T + aI^b \\ &= (V_1 + V_2 T) + (a_1 + a_2 T) I^{(b_1 + b_2 T)} \end{aligned} \tag{5.20}$$

where V_1 to b_2 are constants, T is the temperature in ^oC and I is the current flowing through the device. Note that the simple constants in (5.2) have been replaced by temperature dependent expressions. The conduction model parameters V_1 to b_2 are given in Table E.3 in Appendix E. The manufacturer's data sheet [59] for the diodes in the resonant link circuit (BYT 30PI800) recommends the use of the following equation to evaluate its conduction loss

$$v_{D_{drop}} = V_D + R_D i_D \tag{5.21}$$

where $V_D = 1.47$V and $R_D = 0.01\Omega$.

For a load level of 1kW at a dc link voltage of 300V the average dc link current will be about 3.3A. Using (5.20), the conduction loss in S_1 can be calculated to be around 5W. Using this simple approach, the PRDCL circuit gives lower overall losses than a hard-switched inverter for switching frequencies higher than 1800Hz under the same load conditions as used in Figure 5.5.

In order to refine the analysis, the conduction loss occurring during a resonant transition has to be taken into consideration. Since the current waveform cannot be described by a single function over the whole conduction interval, the calculation is broken up into five intervals. The following equations can be derived for a resonant cycle:

$$p_{mode1}(t) = v_{T_{drop}}(t)I_o + 3v_{T_{drop}}(t)i_{L_r}(t) + R_{L_r}i_{L_r}^2(t) \quad (5.22)$$

$$p_{mode2}(t) = 2v_{T_{drop}}(t)i_{L_r}(t) + R_{L_r}i_{L_r}^2(t) \quad (5.23)$$

$$p_{mode3}(t) = \left(v_{T_{drop}}(t) + v_{D_{drop}}(t)\right) i_{L_r}(t) + R_{L_r}i_{L_r}^2(t) \quad (5.24)$$

$$p_{mode4}(t) = 2v_{D_{drop}}(t)i_{L_r}(t) + R_{L_r}i_{L_r}^2(t) \quad (5.25)$$

$$p_{mode5}(t) = 3v_{D_{drop}}(t)i_{L_r}(t) + R_{L_r}i_{L_r}^2(t) \quad (5.26)$$

$v_{T_{drop}}(t)$ and $v_{D_{drop}}(t)$ have been introduced as functions of time since they depend on the current which itself is a function of time. R_{L_r} is the equivalent series resistance (ESR) of the resonant inductor L_r.

The conduction losses for each sub-interval are then summed up and divided by the duration of a resonant cycle to give the average loss for a resonant transition. Figure 5.7 shows the calculated conduction loss for $I_o = I_{ox} = 3.3$A. This scenario represents the worst possible case in terms of the required initial current in the resonant tank while the best case is given when I_o is positive and $I_{ox} = -I_o$ (see Figure 3.11). The duration of a worst-case cycle is 12.6μs while for the best case it is only 11.4μs. The resonant tank design is the same as described in Section 3.5.1 and the dc resistance of L_r was measured to be 40mΩ. The calculation reveals that the energy per worst-case resonant transition is 0.83mJ while the average power is 66.1W. For the best-case transition the energy loss is 0.5mJ and the average power $P_{av} = 44.1$W. Assuming that the average value of energy loss per resonant cycle is the mean value of the worst-case and best-case values, we can evaluate the contribution of the resonant link to the total conduction loss by multiplying the average energy by six times the switching frequency for the six switching edges in a PWM output period. The result is 4W for 2kHz switching frequency. Note that this assumes that the resonant link is activated for each switching edge and no vector dropping occurs. In this example, the contribution of the equivalent resistance of the resonant inductor to the conduction

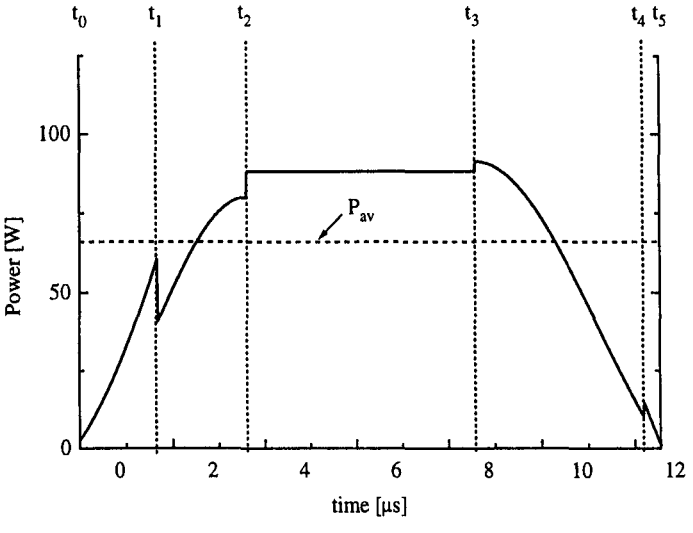


Figure 5.7: Ideal waveform of conduction loss during worst-case resonant transition and average power.

loss amounts to 21%. A reduction of the zero-voltage time from the presently used 5μs would improve the situation significantly. The effect of zero-voltage time and its practical implications will be discussed in the following section.

From the results obtained so far it is clear that it is not appropriate to neglect the conduction loss incurred in the resonant link for the evaluation of the overall efficiency of the PRDCL inverter. Given these results, the refined approach to calculate the conduction loss is as follows:

1. For a given power level, the energy loss per resonant cycle is calculated using Equations (5.22–5.26) for the worst-case and best-case values of I_o and I_{ox}. The mean of these two values is taken as the average energy loss per resonant cycle.

2. The conduction loss owing to the resonant link action can then be calculated by multiplying the energy derived in step one by six times the switching frequency.

3. The conduction loss in S_1 is calculated using the conduction model with the average dc link current derived from the power level. The duty ratio of S_1 is

$$\delta_{S_1} = 1 - 6 f_{\mathrm{sw}} T_r \tag{5.27}$$

where f_{sw} is the switching frequency and T_r the duration of a resonant cycle.

4. The two conduction loss components of the PRDCL circuit are then summed together with the conduction loss in the main inverter. Note that the components that stem from the PRDCL circuit vary with switching frequency.

5.4.3 Discussion of zero-voltage time

As already mentioned in the previous section, a reduction of the zero-voltage time would significantly reduce the conduction loss produced by the PRDCL circuit. It would also allow higher switching frequencies and reduce the loss of fundamental voltage as discussed in Section 4.6. However, a number of practical implications have to be considered. Conventional PWM inverters provide a dead-time between the turn-off of a transistor and the turn-on of the second transistor in the same inverter leg. In a zero-voltage switched inverter, it would theoretically be possible to eliminate this dead-time and send turn-off and turn-on signals simultaneously. However, this would lead to the certain destruction of the switching devices in case resonance should fail and the zero-voltage condition not obtained. Furthermore, the discussion in Section 5.2.2 has shown that zero-voltage switching actually leads to an extended tail current so the minimum dead-time has to be chosen with respect to this.

With these practical considerations in mind, it was felt that a reduction or even elimination of dead-time would establish a too great risk of inverter shoot-through given that the manufacturer chose a safety margin of 5μs. The dead-time was therefore left unchanged despite the knowledge that in order to achieve a performance from a PRDCL inverter that can compete with existing hard-switched systems in terms of efficiency and switching frequency, the zero-voltage time would have to be reduced significantly.

5.5 Total losses

Figure 5.8 shows all loss components for a PRDCL system operating at 1kW output power and a load power factor of 0.6 (inductive). The load power factor was chosen to allow comparison with measured results where an *RL*-load with a load power factor of 0.6 will be used. Note that the load power factor only influences the main inverter conduction loss and does not affect the additional conduction loss introduced by the PRDCL circuit. It is assumed that the load current stays constant with increasing switching frequency. Note that the output power of the PRDCL inverter reduces below 1kW at high switching frequencies due to the loss of fundamental voltage discussed earlier in Section 4.6. As can be seen the conduction loss owing to the resonant link action increases with switching frequency while the conduction loss in S_1 decreases. Taking all the loss components into account, it is interesting to note that the PRDCL inverter has no efficiency advantage over a hard-switched inverter regardless of switching frequency. Increasing the output power while leaving the other

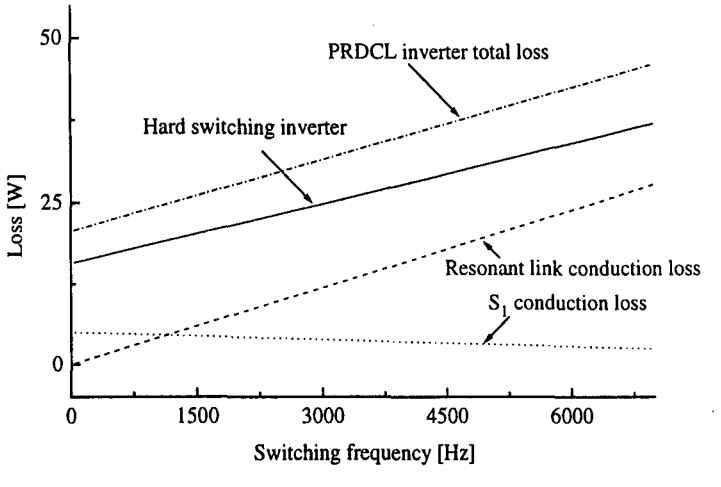


Figure 5.8: PRDCL inverter and hard-switched inverter losses for 1kW output power; zero-voltage time 5μs.

parameters unchanged however does alter the situation as can be seen in Figure 5.9 which shows results for an output power of 2.5kW at the same load power factor as before. Here we find that the PRDCL inverter does produce lower overall losses

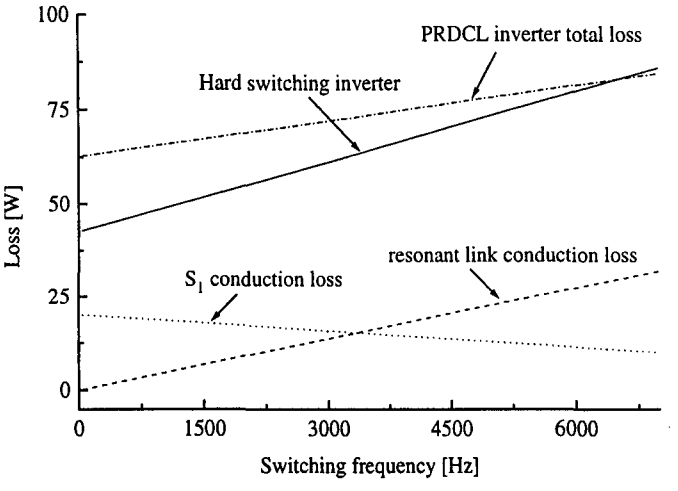


Figure 5.9: PRDCL inverter and hard-switched inverter losses for 2.5kW output power; zero-voltage time 5μs.

for switching frequencies in excess of 6.5kHz. Note however that the frequency range over which a useful efficiency gain can be achieved is limited, considering the effects of the 5μs zero-voltage gaps on the output voltage. The conduction loss for S_1 becomes negative beyond a switching frequency of 14kHz which indicates that the duty ratio of S_1 becomes negative at this point and hence there is no output voltage left. For switching frequencies beyond 7kHz the duty ratio for S_1 falls below 0.5 which means that the voltage source V_S is connected to the inverter input for less than half the duration of an output period, resulting in substantial loss of fundamental output voltage as discussed in Section 4.6.

To achieve high switching frequencies it would be necessary to reduce the zero-voltage time considerably. Figure 5.10 shows the results for the same conditions as in Figure 5.9 but for a zero-voltage time of 1μs. The practical problems associated with a reduction of zero-voltage time have been discussed in Section 5.4.3. Now the PRDCL inverter becomes more efficient than its hard-switched counterpart for switching frequencies above 4.5kHz which seem achievable in practice given that owing to the 1μs dead-time requirement the IGBT devices have to be fast switching types anyway. The switching frequency at which the duty ratio for S_1 falls below 0.5 is 10.5kHz in this example.

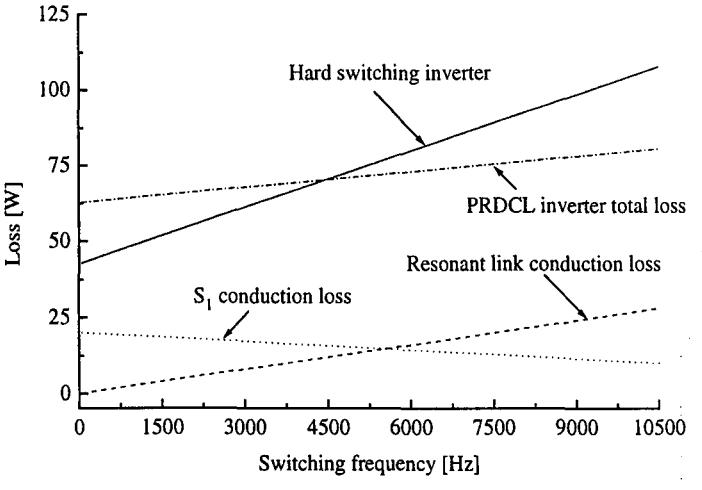


Figure 5.10: PRDCL inverter and hard-switched inverter losses for 2.5kW output power; zero-voltage time 1μs.

5.6 Summary

This chapter has analysed the different loss mechanisms that occur in hard switching PWM inverters and the PRDCL PWM inverter. The switching behaviour of IGBTs under hard- and soft-switching conditions has been explained and it was found that zero-voltage switched IGBTs reveal a number of unexpected characteristics like dynamic voltage saturation and an extended tail current at turn-off. When analysing the losses in the PRDCL inverter it was found that conduction loss increases with switching frequency which is not the case for conventional inverters. In order to keep conduction loss in the PRDCL circuit low, it is important to keep the zero-voltage gap as narrow as possible. This is true not only for the PRDCL inverter examined in this work but equally concerns similar inverters that have been proposed [16, 17, 22, 34, 35]. The problems associated with the frequent activation of the resonant link — loss of fundamental voltage, increase in conduction loss — is an inherent disadvantage of the soft switching principle applied in these circuits and will ultimately limit the performance of all the systems presented so far. In order to reduce the number of times the resonant link has to be activated, many designs apply individual snubber capacitors across the inverter devices to allow soft turn-off independent of the resonant

link state. However, as outlined in Section 5.2.2 this leads to oscillations at turn-on which result in an increase of turn-on loss and can potentially damage the switching devices.

It was also found that the simple approach given in [17] to evaluate the additional conduction loss owing to the presence of the resonant link is inappropriate and a refined approach was suggested that takes into account the losses incurred during a resonant cycle.

It was shown that the PRDCL inverter is capable of achieving higher overall conversion efficiency than a hard-switched inverter but the switching frequency domain over which this is practicable is restricted and careful design of the resonant link is required. It should be noted however that the additional loss components that occur under zero-voltage switching as described in Section 5.2.2 are not included in the analysis of the PRDCL circuit's overall efficiency. Therefore, the realistically achievable efficiency benefits of the PRDCL inverter system are expected to be even more limited than the findings of this chapter suggest.

Chapter 6

Practical results

6.1 Introduction

The following sections contain measurement results for the experimental prototype PRDCL inverter. One section deals with the currents and voltages that can be measured in the resonant link circuit. Another section demonstrates the soft-switching capability of the PRDCL inverter by showing currents and voltages for an inverter device during commutation. The next section is devoted to the inverter output quantities, ie. the load current for different types of load and the output voltages. The last section in this chapter shows results of an experiment carried out to determine the EMC performance of the PRDCL inverter. Each section explains the techniques applied to obtain the measurements and comments on the results with regard to the expected outcome. Where necessary, the theoretical background to an experiment is given.

6.2 Resonant link waveforms

The practical results shown in this section all concern the waveforms that are introduced by the PRDCL circuit, ie. that do not exist in an ordinary, hard-switched voltage source inverter. The waveforms that are shown allow a deeper insight into the operation of the resonant link circuit under load and also provide information about the voltage and current stresses to which the auxiliary devices are subjected.

All results were obtained at a dc link voltage of 312V. The first measurement shows the voltage v_{C_r} across the resonant capacitor and the resonant inductor current i_{L_r} for a resonant transition at an output power level of about 700W (RL-load, power factor 0.77). Two sub-oscillations are visible. The first one occurs when v_{C_r} reaches zero

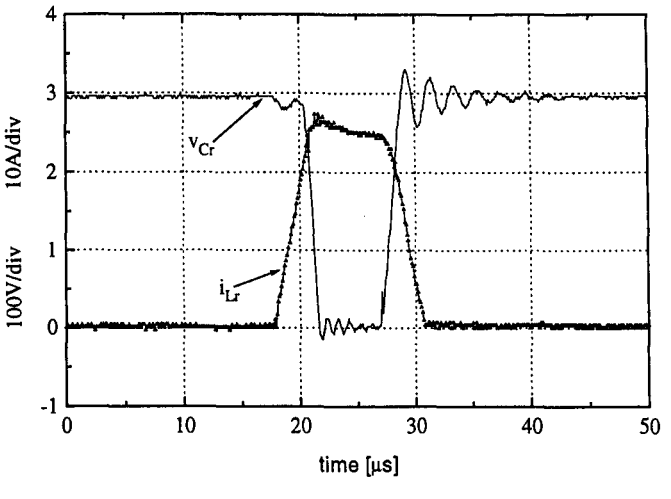


Figure 6.1: Resonant transition waveforms for RL-load.

and the second one when v_{C_r} returns back to dc link voltage level. The oscillation around zero voltage is due to a resonance between stray inductances and C_r and gets triggered by the current that circulates through D_2, S_2 and D_3, S_3 (see Figure 6.2). The natural frequency of the resonance is about 1MHz.

The second oscillation occurs when the capacitor voltage reaches V_S and has a natural frequency of about 500kHz. This sub-oscillation will be further analysed in the

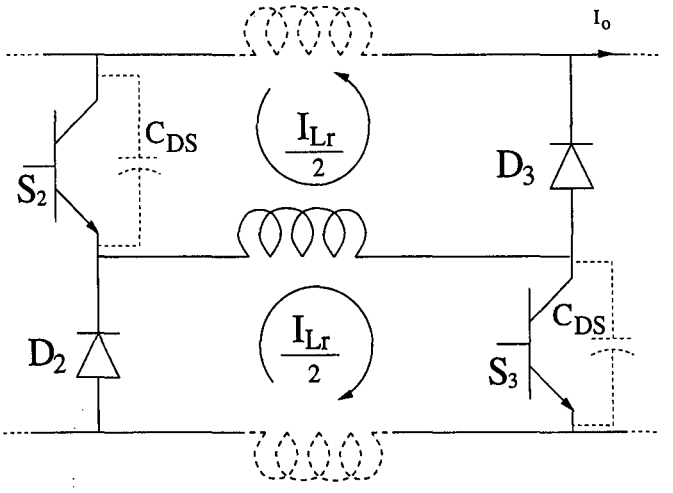


Figure 6.2: Equivalent circuit for zero-voltage period including parasitic drain-source capacitances and stray inductances.

following paragraph.

The voltage across the auxiliary switch S_1 and current through it during a resonant transition are shown in Figure 6.3. Before and after a resonant transition, S_1 carries the sum of all three phase output currents. At the beginning of the resonance, i_{S_1} rises sharply and S_1 carries both the load current and the initial current I_i that is required to complete the resonant cycle. As soon as S_1 is turned off, the voltage across it rises with a dv/dt that is determined by the resonance between L_r and C_r. The current falls sharply at first but the existence of a current tail is clearly visible in Figure 6.3. As soon as the resonant capacitor voltage v_{C_r} has swung back to supply voltage level, a sub-oscillation can be observed in the current. This oscillation corresponds to the ringing of v_{C_r} shown in Figure 6.1. It is triggered by the remaining current I_r in the resonant inductor which is a result of excessive energy stored in the resonant link. The ringing is much smaller in the no-load waveforms shown in Figure 3.16 where the initial energy is closer to its ideal value. The remaining current charges C_r over supply voltage level and as a result, resonance occurs between C_r and the stray inductance along the path between C_r and V_S. From the waveforms in Figure 6.3, it can be seen that S_1 turns off and on under zero voltage.

The next figure shows voltage and current for S_2 during a resonant transition. The

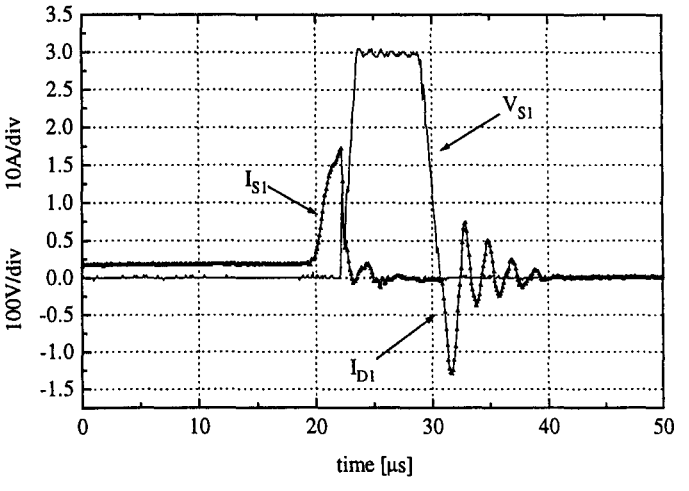


Figure 6.3: Voltage across and current through S_1 for a resonant transition.

dotted lines are used to separate between the different modes of the resonant transition. For the interval $[t_0$–$t_2]$, the resonant link current is conducted by S_2 and S_3. After v_{C_r} has fallen to zero, two current loops are formed by D_2, S_2 and D_3, S_3 respectively as shown in Figure 6.2. For the following interval $[t_2$–$t_3]$, the current is shared

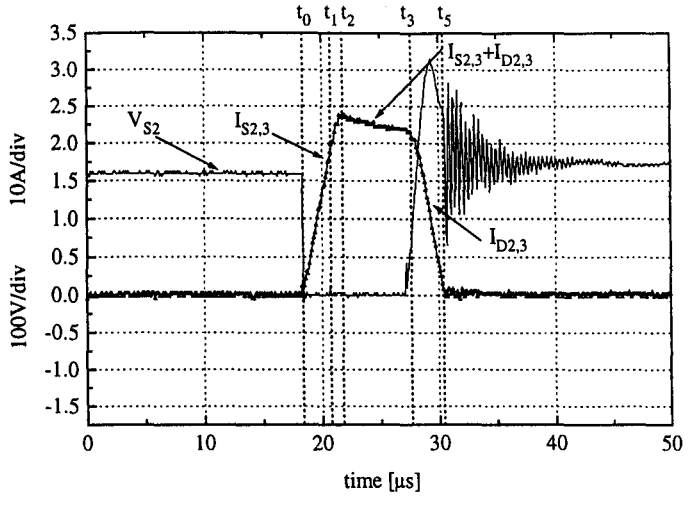


Figure 6.4: Voltage across and current through S_2 for a resonant transition.

equally between the diodes and transistors. When S_2 and S_3 are opened to recharge C_r, the diodes take over the whole current for the rest of the resonant transition ($[t_3$–$t_5]$). When S_2 first turns on, the voltage across it falls to its on-state value and

remains there until it turns off again. The voltage then rises with the same dv/dt as v_{C_r}. The voltage shoots over its steady state value and a slow oscillation starts which is the same as the one shown in Figures 6.1 and 6.3 for v_{C_r} and i_{S_1} respectively. This slow oscillation is superimposed by a high frequency oscillation which starts as soon as the current has fallen to zero, ie. as soon as D_2 and D_3 stop conducting. The oscillation is triggered by a step in the voltage which appears across the diodes at turn-off (see Figure 6.5) and is due to resonance between the drain-source capacitance C_{DS} of the IGBTs S_2 and S_3 and the resonant inductor L_r plus stray inductance (see Figure 6.2). Note that both terminals of the resonant inductor are floating at the end of a resonant transition. In this situation, an oscillation is likely to occur. The peak voltage of the oscillation however does not reach levels that would endanger the auxiliary devices.

It can be seen that S_2 turns on in a ZCS situation with a di/dt that is limited by the presence of L_r so that dynamic saturation effects should be small. Turn-off of S_2 takes place under zero voltage.

Figure 6.5 shows the current and voltage waveforms for diode D_2 during a resonant transition. Note that before the current reaches its maximum value at t_2, it is conducted by S_2 and S_3. After that, the diodes D_2 and D_3 form two current loops with S_2 and S_3 as shown in Figure 6.2. A jump occurs in v_{D_2} at the time when S_2 and S_3 turn on. The voltage across D_2 at this time can be derived as

$$v_{D_2} = v_{L_r} + v_{S_2} = L_r \frac{di_{L_r}}{dt} + V_{CE(sat)} \approx 296V \tag{6.1}$$

When S_1 turns off the voltage across the diode starts falling with the same dv/dt as v_{C_r}. The diodes start conducting as soon as v_{C_r} has fallen to zero (t_2) and the voltage across them falls to their on-state value. As soon as the diodes turn off (current returns to zero at t_5), the voltage exhibits another jump and starts oscillating around its steady state value which is less than half the supply voltage. The steady state values of the voltages across S_2 and D_2 will be determined by their respective parasitic capacitances. The oscillation is the same as was shown in Figure 6.4 for S_2. Again, the peak voltage does not pose a threat to any of the devices in the resonant link

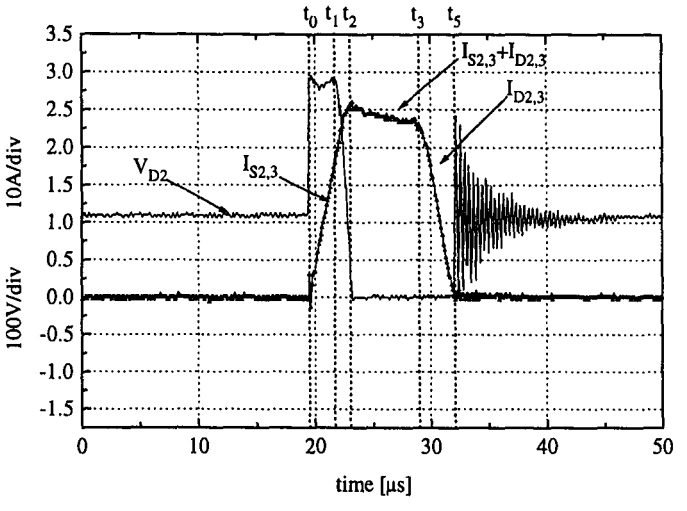


Figure 6.5: Voltage across and current through D_2 for a resonant transition.

or the main inverter so it is not considered harmful in this respect. The ringing is however expected to produce electro-magnetic interferences that deteriorate the EMC performance of the PRDCL inverter.

The waveforms for D_3 and S_3 look similar to the ones shown for D_2 and S_2 respectively.

6.3 Soft turn-on and turn-off

In order to verify the soft-switching capability of the experimental prototype inverter, the current through and voltage across one inverter device have to be measured. In a standard inverter, the current through a particular device cannot easily be obtained and therefore, the following technique was applied: A Rogowski-coil [48] was used to measure the current in the rightmost inverter leg as shown in Figure 6.6. Simultaneously the voltage across the device was measured. The transients of current and voltage for a commutating switching device depend on the instantaneous load condition. Measuring both quantities simultaneously allows to differentiate between the four possible scenarios that can occur:

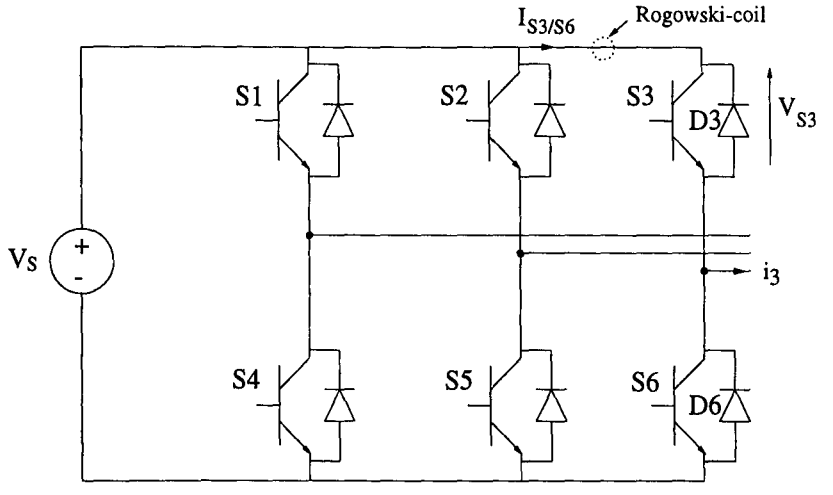


Figure 6.6: Application of Rogowski-coil to measure the current in a switching device.

1. For positive load current i_3 a soft turn-on of S_3 requires that first the voltage falls to zero and after that the current rises to i_3 when the turn-on signal is received by S_3. Before that, i_3 is carried by D_6. This situation is shown in Figure 6.7.

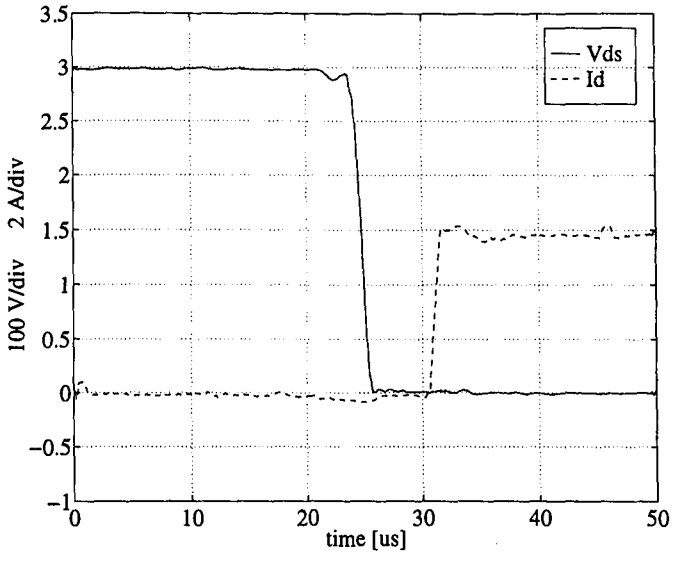


Figure 6.7: Drain-source voltage V_{DS} and drain current I_D for turn-on of S_3 with positive phase current i_3.

2. A turn-off of S_3 with positive i_3 behaves dually: When the turn-off signal is received, the current falls to zero and is taken over by D_6. After the zero-

voltage period, the voltage across the device resonates to V_S. Figure 6.8 shows measured quantities for this condition.

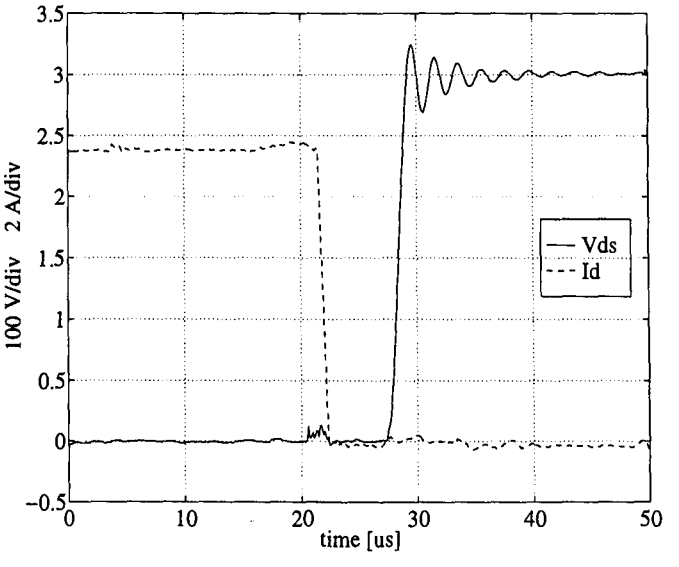


Figure 6.8: Drain-source voltage V_{DS} and drain current I_D for turn-off of S_3 with positive phase current i_3.

3. For negative load current i_3, the soft turn-on of S_3 starts with a falling voltage across the device. As soon as S_6 receives the turn-off signal, the diode D_3 takes over the current. Since by this time the voltage has fallen to zero, the turn-on of S_3 is a soft-switching event. Figure 6.9 shows the device voltage and current for this situation. Note that the current appears negative since it is carried by the antiparallel diode D_3.

4. A turn-off of S_3 with negative load current behaves in the opposite way: As soon as S_6 receives its turn-on signal, the current falls to zero. Immediately afterwards, the voltage resonates to V_S, marking the end of a resonant cycle. Again, voltage and current are not simultaneously present in the device, making this turn-off a soft-switching event. Measured quantities are given in Figure 6.10.

The measured results agree well with the expected behaviour and it can be seen that the PRDCL circuit allows soft turn-on and turn-off of the inverter devices.

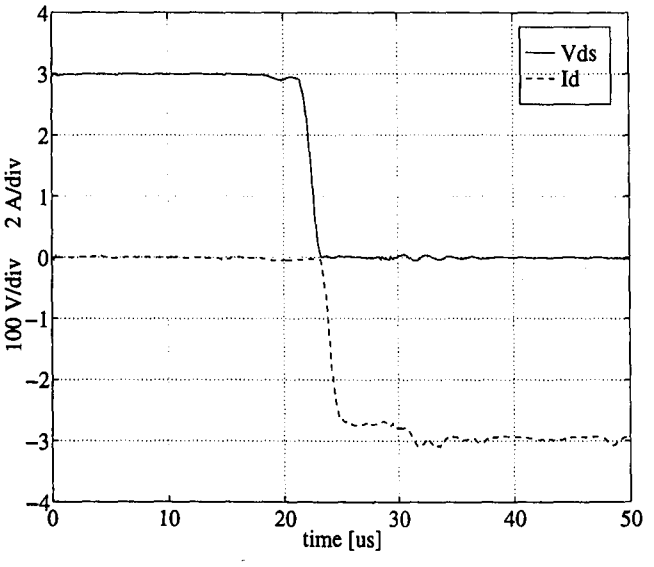


Figure 6.9: Drain-source voltage V_{DS} and drain current I_D for turn-on of S_3 with negative phase current i_3.

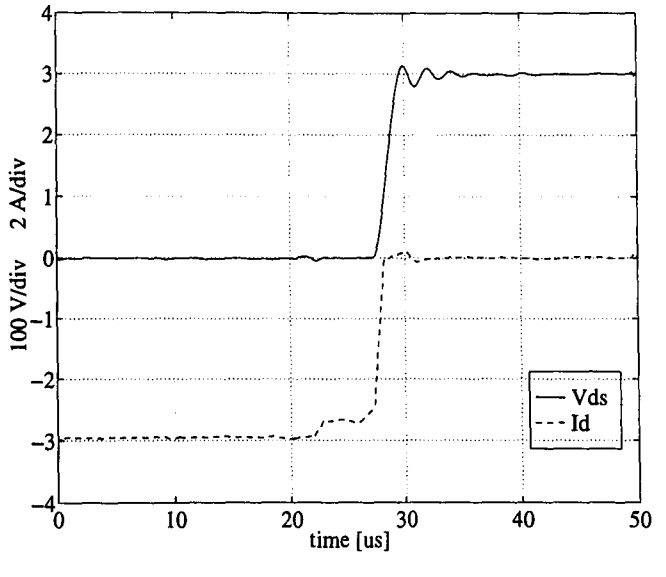


Figure 6.10: Drain-source voltage V_{DS} and drain current I_D for turn-off of S_3 with negative phase current i_3.

6.4 Inverter output voltages and currents

To assess the output waveform quality of the PRDCL PWM inverter, one line-to-line voltage and one phase current were measured for different load conditions.

6.4.1 *RL*-load

An *RL*-load consisting of a series combination of a three-phase resistor and a three-phase inductor was used to obtain the following results. The phase current i_a for the *RL*-load is given in Figure 6.11. The output power level is 700W at a power factor of 0.77 and a switching frequency of 1kHz. The effect of the switching frequency on the

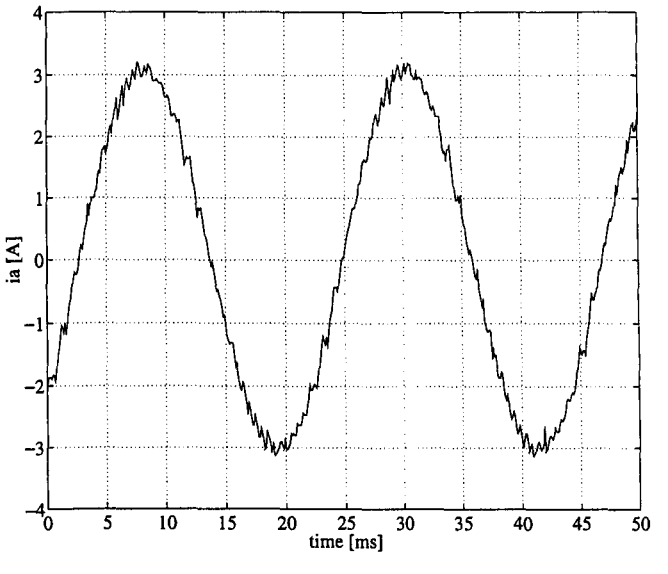


Figure 6.11: Phase current i_a for *RL*-load; switching frequency 1kHz, output frequency 45Hz.

output waveform can be seen in the next plot. It shows the phase current i_a for the same conditions as used for Figure 6.11 but at a switching frequency of 2kHz. It can be seen that the output current is less distorted in the second case since the dominant harmonics of the output current spectrum will be higher in frequency and hence more attenuated than for the lower switching frequency. The amplitude of the current is also lower in the second case than in the first although the same modulation index

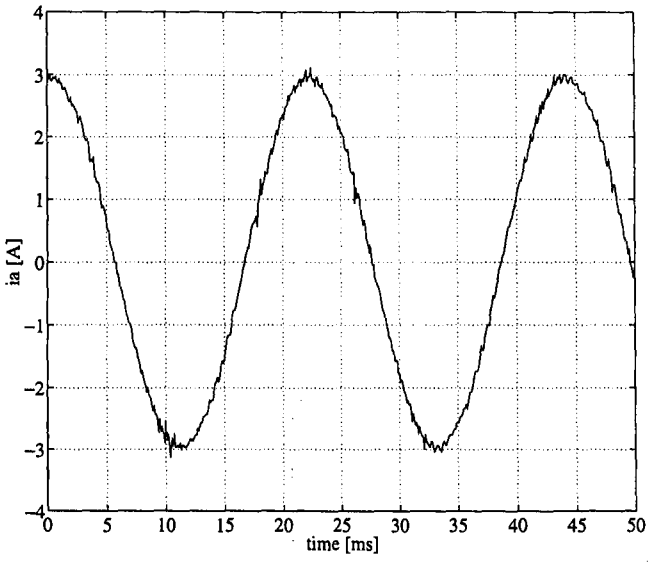


Figure 6.12: Phase current i_a for RL-load; switching frequency 2kHz, output frequency 45Hz.

of $m = 0.9$ was used to obtain both results. This illustrates the effect of the loss in fundamental output voltage that is due to the notches introduced by the resonant link action as explained in Section 4.6. T_{min} was set to $20\mu s$ for this and all other experiments. From Figure 6.12 we can see that the fundamental amplitude is reduced by about 3.3% compared to the one for 1kHz switching frequency which, considering the quantization error of the digital oscilloscope used to record the results, corresponds well with the theoretically derived value of 4% reduction (see Section 4.6).

The next graph shows the line-to-line voltage at an output frequency of 35Hz and switching frequency 1kHz. The patterns produced do not look different from conventional PWM line-to-line voltages. A zoomed version of the line-to-line voltage in Figure 6.14 reveals the notches that are introduced by the resonant link action. Each notch represents a switching event in one of the other line-to-line voltages. Ringing at the ends of the resonant transitions is due to the mechanisms discussed earlier.

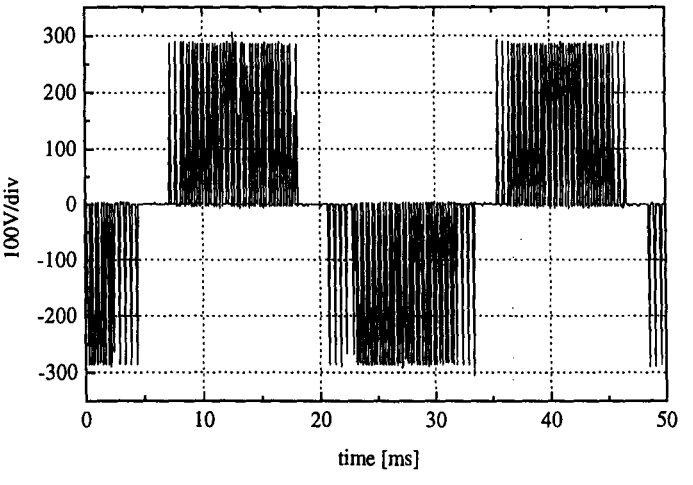


Figure 6.13: Line-to-line voltage for *RL*-load; switching frequency 1kHz, output frequency 35Hz.

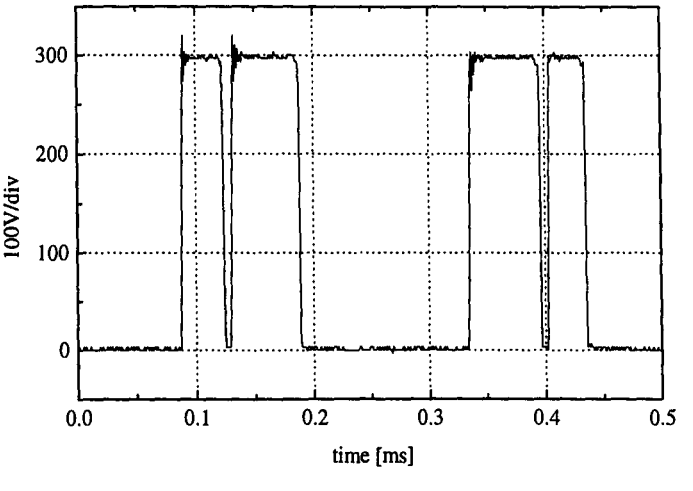


Figure 6.14: Line-to-line voltage for *RL*-load; switching frequency 1kHz, output frequency 25Hz.

6.4.2 Induction machine load

The next graphs show results measured with an induction machine load. The induction machine was driving an unloaded dc-machine. Figure 6.15 shows the phase current i_a for an output frequency of 45Hz at a switching frequency of 1kHz while the next graph shows the same current for a switching frequency of 2kHz. The improve-

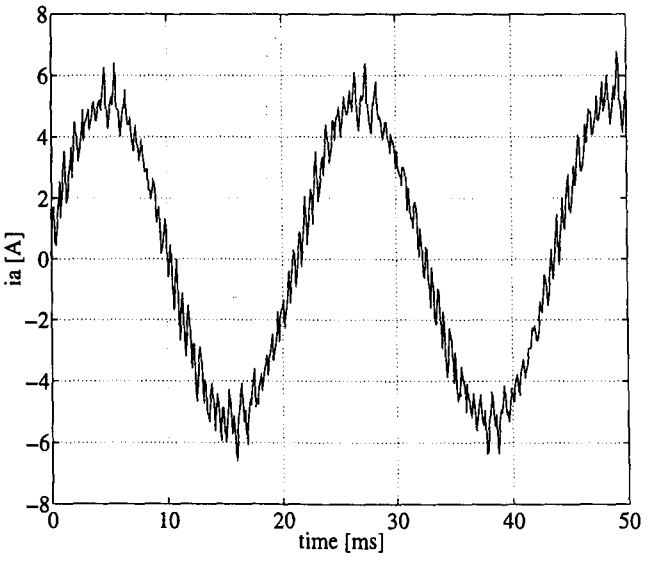


Figure 6.15: Phase current for induction machine load at 1kHz switching frequency, output frequency 45Hz.

ment in output current quality that can be expected from doubling the switching frequency is clearly visible in Figure 6.16. The last plot in this series shows the phase-to-midpoint voltage (inverter midpoint) for the induction machine load. Again we can see from the graph that every commutation is performed with dv/dt levels that are governed by the resonant tank components. The output waveforms look as can be expected from a PWM inverter with the exceptions of the zero-voltage gaps that are introduced in the line-to-line voltages. With the present settings of switching frequency and minimum vector on-time T_{min}, the quality of the output current is very similar to that obtained with conventional hard-switched PWM.

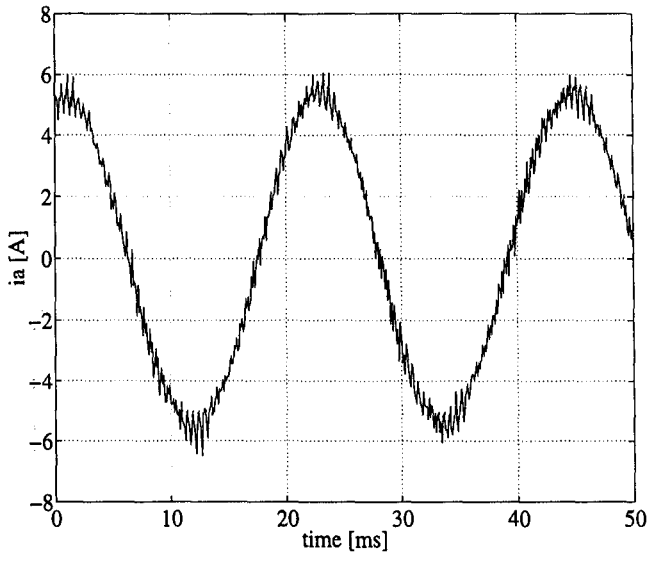


Figure 6.16: Phase current for induction machine load at 2kHz switching frequency, output frequency 45Hz.

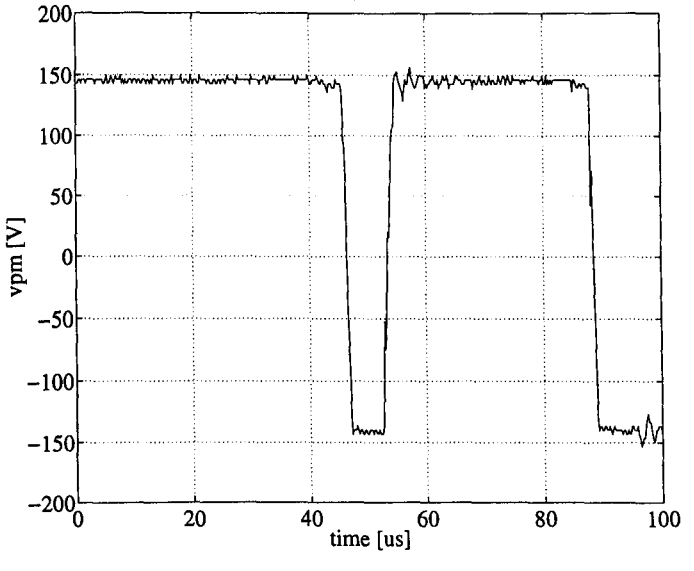


Figure 6.17: voltage Phase-to-midpoint voltage for induction machine load at 1kHz switching frequency, 25Hz output frequency.

6.5 Measured losses

To evaluate the losses in the PRDCL inverter system, a simple approach was taken that compares the power on the input and output sides of the inverter by measuring three phase currents and three line-to-line voltages using two power analysers (Voltech PM 3000) as shown in Figure 6.18. The results should allow us to derive general trends for the dependency of conversion efficiency on switching frequency for hard- and soft-switching. The following plot shows input and output power for hard-switching

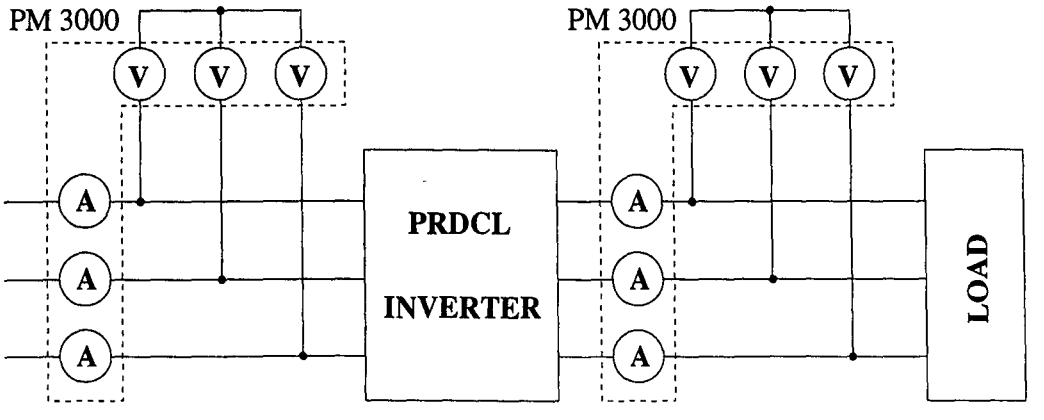


Figure 6.18: Experimental setup for power loss measurement.

with an *RL*-load. The output power lies around 1kW and the load power factor is

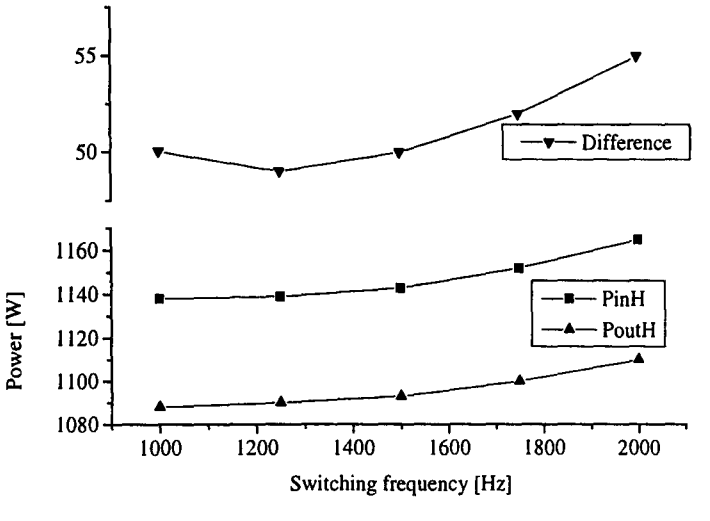


Figure 6.19: Input and output power for 1kW load; hard-switching.

0.6. The results are also given in numerical form in Table 6.1 which shows that the difference between input and output power varies between 44W and 51W which is about 20W greater at 1kHz switching frequency than predicted using the approach developed in Section 5.5. This difference between the prediction and the real result can be accounted for by power losses that were not considered in Section 5.5, ie. in the gate drivers and other control circuitry in the conventional inverter. These consume together 22W which was measured with the inverter running and switching at no load (modulation index zero). Subtracting these 22W leaves differences between

f_{sw} [Hz]	$P_{in} - P_{out}$ [W]	predicted $P_{in} - P_{out}$ [W]	predicted - measured [W][a]
1000	44	24.3	+2.3
1250	45	25.2	+2.2
1500	47	26.1	+1.1
1750	49	27	0.0
2000	51	28	−1.0

Table 6.1: Predicted and measured differences between input and output power for hard-switching.

[a]after subtraction of 22W for gate drivers, etc.

the predicted and measured results that vary from +2.3W (predicted losses higher than measured losses) for 1kHz switching frequency to −1.0W for 2kHz switching frequency. These discrepancies can be attributed to experimental error and reading errors for the conduction and switching power loss diagrams given in the data book [58]. An increase in switching losses with rising switching frequency can be clearly seen in Figure 6.19, although the total switching losses and the increase are small in the chosen power and switching frequency range. The measured results confirm the validity of the prediction methods used.

The next plot (Figure 6.20) shows the result for soft-switching. Note that in order to guarantee stable link transitions at this power level it was necessary to increase the energy injected in the resonant tank by making I_i greater than its calculated ideal value. This increase in resonant tank energy is required due to the power losses that occur in the link during a resonant transition which mean that the capacitor

voltage v_{C_r} does not return to V_S unless the losses are compensated for by injecting surplus energy. These losses occur in the resonant inductor L_r which is in the current path for the whole resonant cycle and in the auxiliary semiconductor devices. They are not taken into account by the inequality (3.30) that is used to derive the ideal value of I_i. The losses could be significantly reduced by making the zero-voltage gap shorter than the presently used $5\mu s$ that were chosen for safety reasons as discussed in Section 3.5.1.

To achieve robust operation it was found that I_i had to be increased until the argument for the arctan function in

$$T_2 = \frac{1}{\omega_r} \arctan\left(\frac{V_S}{Z_r(I_i + I_o)}\right) \tag{6.2}$$

is less than or equal to 0.75. As explained in Section 3.5.2 (6.2) provides a way of ensuring that resonance is maintained by making the argument $\frac{V_S}{Z_r(I_i+I_o)}$ smaller (ie. by increasing I_i).

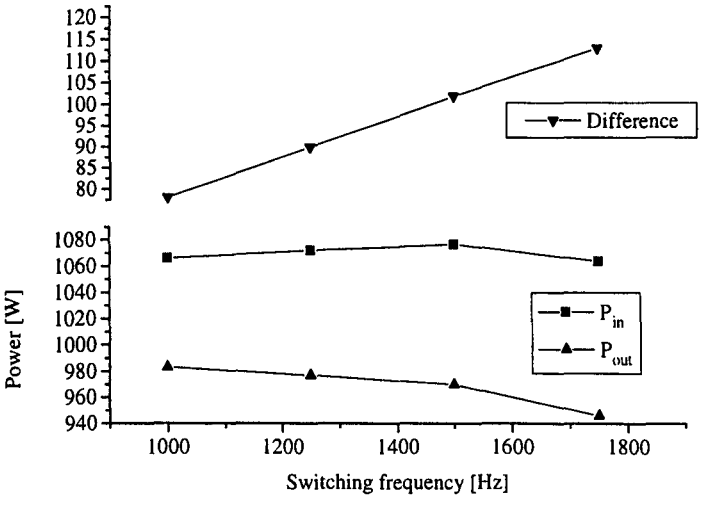


Figure 6.20: Input and output power for 1kW load; soft-switching.

Taking into account the required increase in I_i, the predicted results for input and output power are shown in Figure 6.21 and given numerically in Table 6.2. The predicted difference between input and output power varies between 28.1W and 35.5W

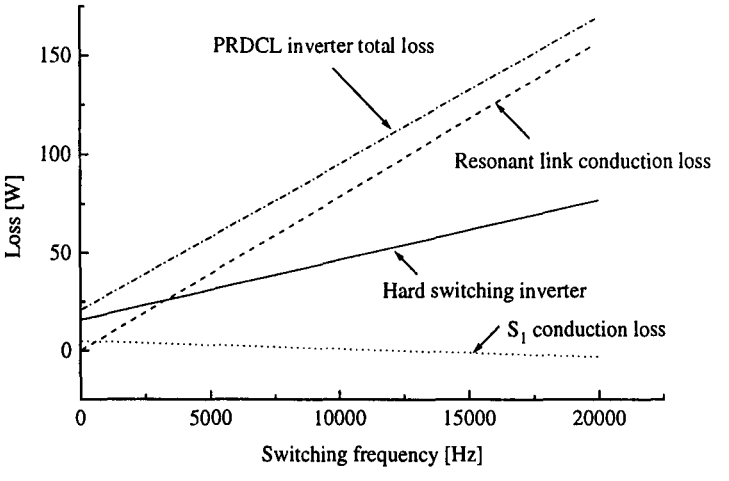


Figure 6.21: PRDCL inverter and hard-switched inverter losses for 1kW output power with increased I_i; zero-voltage time 5μs.

after subtracting 22W for power losses in gate drivers and other control circuitry. The measured difference between input and output power is greater than the predicted result by between 28W for 1kHz to 57W for 1.75kHz. This indicates that there are additional loss components that were not taken into consideration in the analysis so far and which increase with switching frequency. One origin of these losses are switching losses that occur under soft-switching.

f_{sw} [Hz]	$P_{in} - P_{out}$ [W]	predicted $P_{in} - P_{out}$ [W]	predicted - measured [W][a]
1000	78	28.1	−27.9
1250	90	30	−38
1500	102	31.8	−48.2
1750	113	33.7	−57.3
2000	51	35.	—[b]

Table 6.2: Predicted and measured differences between input and output power for soft-switching.

[a] after subtraction of 22W for gate drivers, etc.
[b] experiment had to be stopped due to overtemperature condition of S_1.

These are due to "dynamic voltage saturation" and the enhanced current tail of IGBTs under zero-voltage switching as described in Section 5.2.2. While the inverter

devices are only switched at say 1.75kHz, the switching frequency for S_1, S_2 and S_3 is six times this value, thus $f_{\text{sw,link}} = 10.5\text{kHz}$. Hence the majority of these additional losses is expected to occur in the auxiliary devices. In fact from the experiment it is clear that the extra losses are mainly dissipated in S_1 which at 2kHz switching frequency became so hot that its maximum permissible junction temperature was exceeded and the switch destroyed.

Another reason for the unexpected high losses in S_1 is the fact that it is in a transient condition for most of the time and has to conduct high pulse currents (ie. I_i) in addition to the inverter input current. The conduction model given in [57] is an approximation that is only valid for steady state conduction, a state that is defined by a voltage across the IGBT of less than 5% of the supply (dc link) voltage. S_1 however rarely ever reaches this state so the conduction model leads to predicted losses that are below the actual losses. The fact that S_1 has to carry the full load current as well as the initial current for each resonant transition has to be regarded as a serious drawback of the PRDCL circuit.

6.6 EMC measurements

To compare the EMC performance of the PRDCL inverter with conventional hard-switching, the conducted emissions were measured for both cases. Conducted emissions result from the high levels of dv/dt in an inverter system. The voltage waveforms contain a wide band of frequencies which lead to the excitation of electromagnetic oscillations at the various natural frequencies of the system. Because of the stray capacitance and parasitic inductance which are distributed throughout the drive system, some of these natural frequencies are in the radio frequency range [49].

There are two components of high frequency current flowing in the drive system. While differential mode currents flow between phases at the drive input and output sides, common mode current flows between the output phases and the drive system's earth. The flow of this common mode current is a result of the capacitances between

motor windings and motor frame and stray capacitance between the switching devices and the drive case and the high levels of dv/dt that are applied across these capacitances owing to the switching action in the inverter. In a soft-switching inverter, it is expected that the common mode current will be much reduced due to low dv/dt at the inverter output. In order to measure these phenomena, an experimental setup as shown in Figure 6.22 was used. A line impedance stabilisation network (LISN [49]) is

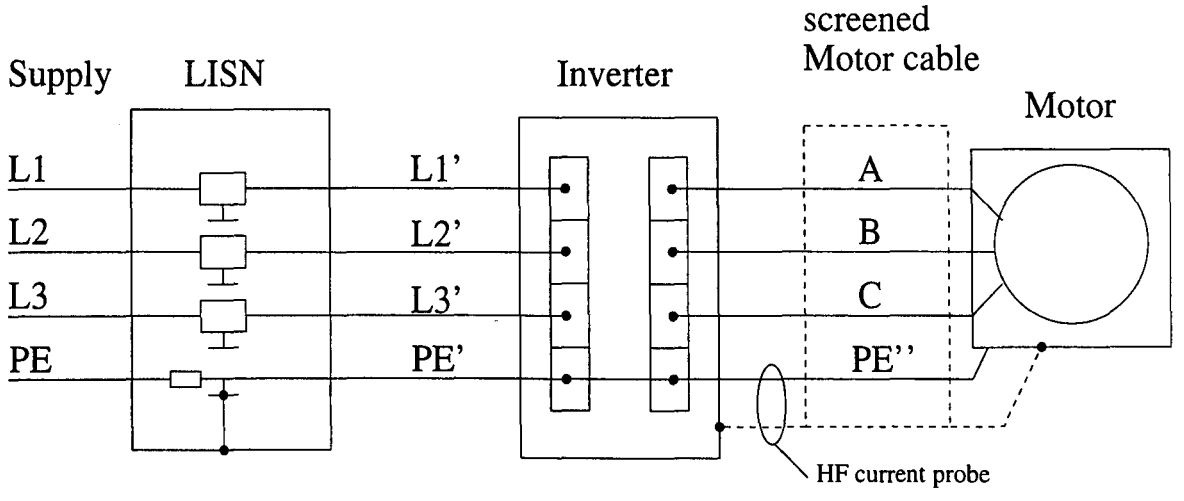


Figure 6.22: Experimental setup for EMC measurements.

inserted between the utility supply and the drive. The LISN stops interference entering the system under test and diverts the high frequency current drawn by the drive through a defined impedance of 50Ω. The conducted interference, both common and differential mode can then be determined by measuring the voltage drop across the LISN impedance. The drive is supplied from the LISN through an unscreened cable while the cable between drive and motor is screened and has a length of about 10m. The earth current and the current in the cable screen are measured with a single high frequency current probe. In the following, the term earth current is therefore used to denote both the earth return current and the current in the cable screen. All measurements were taken with the induction machine load as described in Section 6.4.2 at 25Hz output frequency and no load.

The EMC phenomena under hard-switching are illustrated in Figure 6.23 which shows the earth current and two line-to-line voltages. At each switching event, a current spike appears in the earth current.

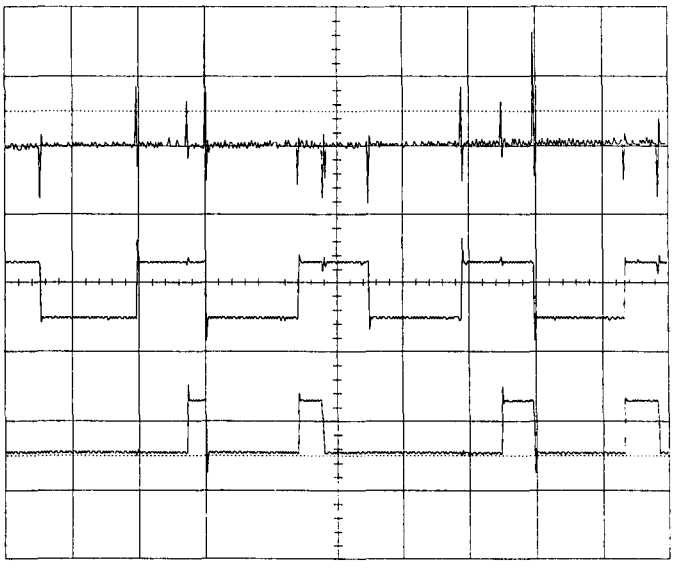


Figure 6.23: Earth/screen current and two line-to-line voltages for hard-switched PWM (0.2ms/div, 0.5A/div, 400V/div).

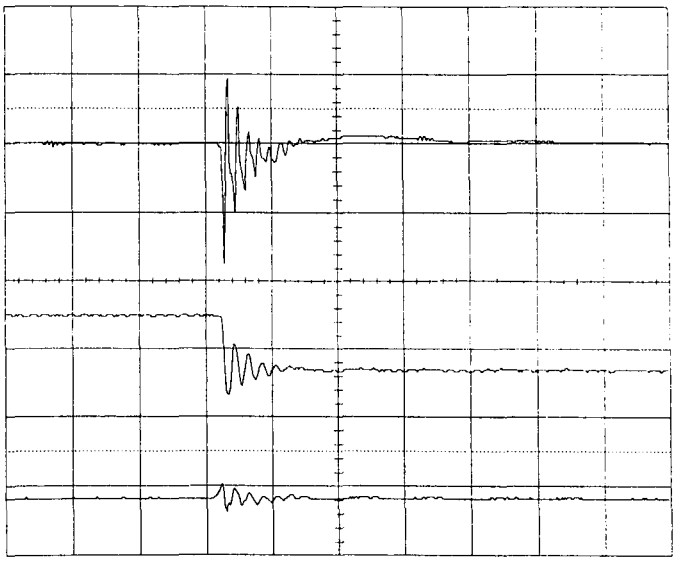


Figure 6.24: Earth/screen current and two line-to-line voltages for hard-switched PWM (2μs/div, 0.5A/div, 400V/div).

The zoomed version of this plot is shown in Figure 6.24. Here it can be seen that each switching event is also followed by a high frequency oscillation on the motor line-to-line voltages. This oscillation is caused by a resonant LC link between phases of the motor and motor cable and represents a differential mode at the output side of the drive. The oscillation can lead to peak voltages at the motor terminals of up to twice the dc link voltage and poses a real threat to the insulation of induction machines especially when long cables are used between inverter and machine [50]. Soft switching leads to low levels of dv/dt thus reducing the effect of resonance between cable and machine. The current in the earth cable results from the high dv/dt and the capacitance between the motor windings and the motor frame. Consequently, reduced levels of dv/dt should lead to a reduction of this current. The following figure (Figure 6.25) shows the same voltages and current as for Figure 6.24 for soft-switching. The transition in the line-to-line voltages occurs with a modest dv/dt

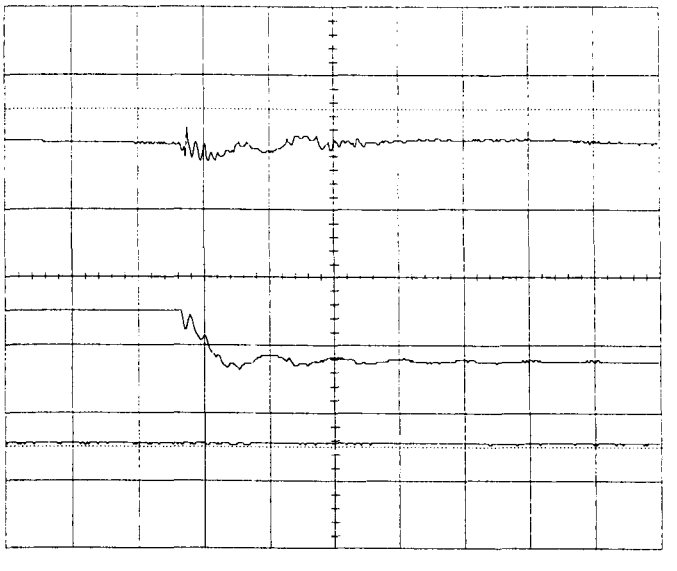


Figure 6.25: Earth/screen current and two line-to-line voltages for soft-switched PWM (2μs/div, 0.5A/div, 400V/div).

which is governed by the resonant transition of the PRDCL circuit. No high frequency oscillation is visible on any of the two line-to-line voltages. The amplitude of the spike in the earth current is much lower than in the hard-switched case, 0.15A as compared to 0.875A respectively. The reduction in the earth current becomes more evident in Figure 6.26 which shows another incident of the same switching event as before with a

different scaling for the current. The amplitude of the current oscillation lies around 0.19A and therefore is less than a quarter of what it amounts to in the hard-switched case.

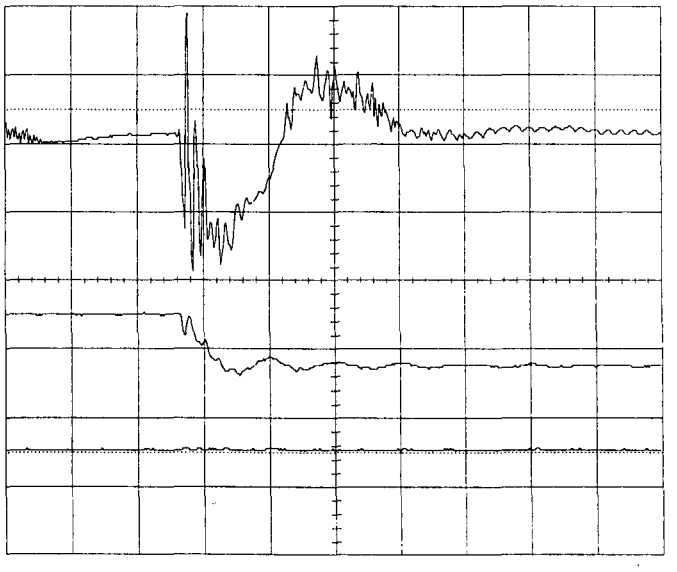


Figure 6.26: Earth/screen current and two line-to-line voltages for soft-switched PWM (2μs/div, 100mA/div, 400V/div).

EMC measurements are normally performed in the frequency domain so it is interesting to examine the spectrum of the earth current. To obtain this measurement, the signal from the high frequency current probe was fed to a spectrum analyser. The results are shown in Figures 6.27 and 6.28 where each figure contains the spectra for hard-switching and soft-switching under otherwise identical conditions. Figure 6.27 shows the spectrum over a frequency range from 9kHz to 3MHz. In the frequency range from 0.7 MHz to 1.8 MHz, the amplitude spectrum of the earth current is lower for the soft-switched case than for hard-switching while for the remaining frequency regions, the EMI performance is found to be inferior for soft-switching. This result is unexpected insofar as the amplitude spectrum around 3MHz is concerned. In the time domain result for hard-switching (Figure 6.24) an oscillation of about 3MHz can clearly be seen in the earth current which does not occur under soft switching (Figure 6.25). We would therefore expect less common mode emission in this frequency range for soft-switching yet the measured spectra suggest otherwise. A conclusive explanation for this phenomenon was not found but clearly the different operating

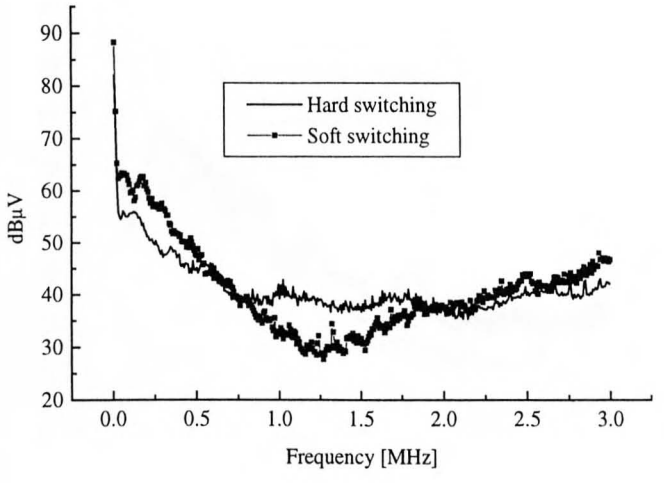


Figure 6.27: Spectra of earth return current for hard- and soft-switching; Frequency range 9kHz–3MHz.

principle of the PRDCL inverter with its resonant link transitions does not allow to make a simple connection between time domain and frequency domain results. It has to be assumed that the high-frequency ringing of the link voltage at the end of a resonant transition (not seen in Figure 6.25 but cf. eg. Figure 6.14) also contributes to the common mode emission seen in the spectra.

The spectrum for a frequency range from 9kHz to 30MHz is shown in Figure 6.28 which again shows that soft-switching is only superior over a limited frequency range while it performs worse over most of the frequency band. The reduction in conducted emission in the earth return cable over a limited frequency range is an encouraging result. The fact that over the remaining frequency ranges the performance of the soft-switching system is actually inferior to hard-switching can be explained with two mechanisms generating interference.

The notches that appear in the phase voltages as a result of the resonant link transitions produce additional common mode current. Since the notches occur in all phases at the same time they represent a very large common mode excitation signal. The effect of the notches is expected to contribute significantly to the common mode emissions in the low frequency range (below 0.7MHz in Figure 6.27). Secondly, the

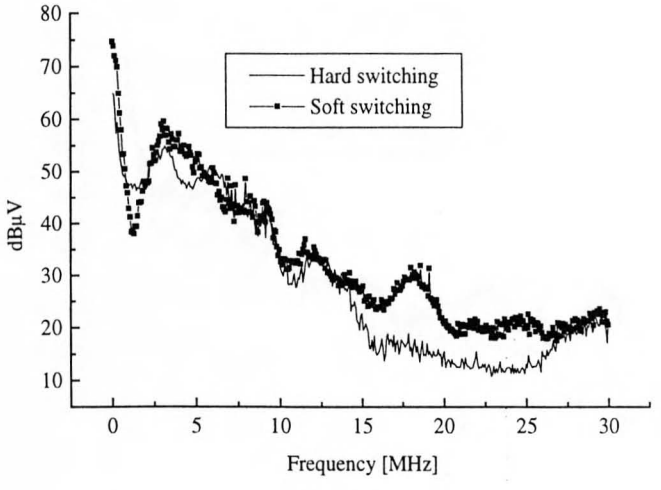


Figure 6.28: Spectra of earth return current for hard- and soft-switching; Frequency range 9kHz–30MHz.

oscillation at the end of resonant transitions is expected to produce extra common mode emission. These emissions will be dominant in the high frequency range (above 1.8MHz in Figure 6.27). Note however that as already mentioned in Section 6.2 this ringing could be significantly reduced if not avoided in a system carefully designed to minimize stray reactance. The inferior performance in this frequency range is therefore not regarded as an inherent weakness of the PRDCL inverter system.

Figure 6.29 shows the output of the LISN for one supply voltage phase. The LISN measures both common mode and differential mode emissions simultaneously and it is therefore impossible to evaluate each mode separately from the results obtained. Soft-switching is seen to produce more conducted emission over almost the entire frequency range from 150kHz to 30MHz. Only for some frequency values is the result for soft-switching equal to the one for hard-switching. The increase in conducted emissions is due to differential and common mode effects which are a result of the resonant link transitions. Since the common mode results for soft-switching were superior to the hard-switched case for the frequency region from 0.7MHz to 1.8MHz, it has to be assumed that an increase in differential mode effects due to the resonant link transitions is responsible for the inferior LISN result in this frequency range.

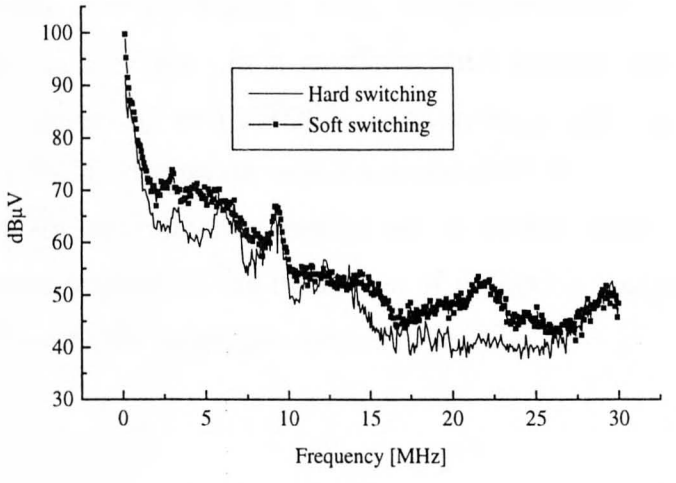


Figure 6.29: Spectra of LISN output for hard- and soft-switching; Frequency range 150kHz–30MHz.

6.7 Summary

The experimental results given in this chapter largely confirm the theoretical analysis. The PRDCL inverter is shown to be capable of providing a soft-switching environment for the inverter switches as well as the auxiliary switches while applying true PWM. The measured output quantities reveal the same characteristics as for any hard-switched inverter applying PWM with the exception of the zero-voltage notches that are introduced in the line-to-line voltages. The conversion efficiency was found to be worse for the PRDCL system than for an equivalent hard-switched system. This is mainly due to conduction losses in the resonant link, both in the resonant inductor L_r and the auxiliary switching devices. The measured power losses were considerably higher than predicted which suggests that switching losses under zero-voltage switching play an important role for an assessment of the overall efficiency of a soft-switching inverter. The EMC performance showed improvements for certain frequency ranges but overall the experimental prototype performed worse than its hard-switched counterpart. Some of the additional emission can be accounted for by the high frequency ringing seen in the resonant capacitor voltage. This ringing is a result of inevitable stray inductances and sub-optimal control of initial current,

two design issues that have to be addressed in a realistic drive operating at medium to high power levels. For the present work, a commercial inverter was modified to operate as a PRDCL inverter. In a carefully built system that is designed solely for the purpose of operating as a PRDCL inverter, stray inductances could be much reduced and the EMC performance would consequently be improved. The low dv/dt can be verified in the experimental results and is a clear advantage in the light of high voltage stresses applied to the insulation of induction motors as a result of the fast switching action of the latest generation of IGBTs.

Chapter 7

Conclusions

This work has described the design and implementation of a three-phase parallel resonant dc link circuit in a PWM inverter drive system. The theoretical analysis of the circuit's operation was confirmed by simulation and practical results taken from an experimental prototype inverter. A modified space vector algorithm that is compatible with the operational principle of the PRDCL inverter was developed and implemented on a network of transputers. Measurements of the conversion efficiency and the EMC performance of the prototype inverter were carried out.

The principle of the PRDCL inverter and similar circuits is to provide a short zero-voltage period in the dc link of the inverter for each switching event on the output side of the inverter. It was seen from the results of the prototype inverter that this zero-voltage gap allows soft-switching of the PWM inverter devices. Furthermore, the topology restricts the peak voltage stress of the inverter devices to the dc-bus voltage. The three additional switches that are required are also subjected to voltages limited to V_S, with the exception of sub-oscillations that peak at higher values and which occur due to stray inductances.

The working principle of the PRDCL inverter and similar circuits requires a minimum dwell time between switching edges in order to ensure that a resonant cycle can be

initiated and completed for each switching event. Standard PWM techniques cannot take this requirement into consideration and a number of modified PWM techniques have been described in the research literature. These methods were however found to be either synchronous [16, 20, 21, 34] which is an undesirable feature in modern drive systems or to produce output currents with a much higher harmonic content than standard PWM methods [22, 23]. To overcome these problems, a modified space vector modulation was developed and implemented which takes into account the requirements of the PRDCL circuit while preserving the spectral quality of standard space vector modulation.

The practical results taken from the experimental prototype validate the working principle and the suitability of the modified space vector modulation. The measured losses revealed that even though all inverter switches and additional switches are switched under soft-switching conditions, additional loss components exist that can only be accounted for by switching losses in the inverter and auxiliary devices. Recent research results confirming this assumption have shown unexpected loss components in IGBTs under both zero-voltage and zero-current switching [41]. These include

1. a di/dt dependent turn-on voltage spike due to conductivity modulation lag and
2. an elevated tail current "bump" under low output dv/dt switching conditions.

Previous publications about the PRDCL inverter and similar circuits [16–18, 20–23, 34] have lacked analytical and experimental efficiency evaluations. It has been claimed for a circuit similar to the one analysed in this work that the additional losses introduced by the resonant link transitions are negligible [17, 18]. This claim was found to be unsubstantiated by theoretical and particularly by experimental results. Reliable loss predictions will have to include loss components that occur under soft-switching and which have so far been neglected.

The results indicate that in order to obtain the maximum benefit from soft switching topologies, existing devices have to be improved with regard to the undesired behaviour that was found in present designs. Desirable characteristics would be a

combination of the switching behaviour of MOSFETs with the low on-state voltage of IGBTs which led to the suggestion of the "super efficient switch" [51], a combination of MOSFET and IGBT in the same package. MCTs have lower on-state losses than IGBTs but show larger current-tails at turn-off under zero voltage so a trade-off between conduction and switching loss is necessary.

It was shown in Chapter 5 that overall improvements in conversion efficiency are possible. However, this would require high inverter switching frequencies which in turn would mean that the resonant link devices have to switch at very high frequencies (six times the inverter switching frequency). As the experimental results have shown, this leads to problems with the auxiliary devices particularly for high load currents. Alternatively, it has been suggested to supply every inverter switching device with a small snubber capacitor instead of using a single resonant capacitor. This would make every inverter device turn-off a soft switching event, thus reducing the number of times that a resonant cycle has to be initiated. However, as was discussed in [40] and [42], this leads to the dumping of the energy stored in the snubber capacitor in the device at turn-on which sets up oscillations that could even overstress the device. It was therefore decided that in order to safely ensure zero-voltage for each switching event it is necessary to actively resonate the link voltage down to zero for every switching edge.

The measurement of EMC performance did reveal improvements in certain frequency ranges but also showed worse performance for the rest of the frequency band. The high-frequency emission that was found to be greater in the PRDCL inverter than for hard-switching is a result of high-frequency ringing in the dc-link voltage. In a system that is specifically designed to operate as a PRDCL inverter, stray inductance could be avoided to a much higher degree than in the prototype inverter which is a modification of a conventional PWM inverter. This high frequency radiation would therefore be much reduced in a carefully designed system whereas the additional low frequency components which are due to the notches in the line-to-line voltages are an inherent feature of the PRDCL inverter and similar circuits. The reduced dv/dt levels at the output however inevitably reduce the conducted EMI in certain frequency

ranges and are a very desirable feature in the face of tighter EMC regulations and insulation problems in induction machines driven by modern IGBT inverters.

The aim of this project was to assess the viability of a soft-switching inverter capable of applying PWM in a medium to high power range. It was shown that the PRDCL topology is capable of providing a soft-switching environment while applying PWM. A number of drawbacks of the circuit however remain to be solved. Firstly, the additional device count of three switches and three diodes will make it difficult for the PRDCL inverter to become an acceptable choice in a highly competitive field where the initial capital cost of a drive is very important. Secondly, the fact that the initial current has to be controlled for each resonant transition means another increase in complexity. Thirdly, the additional conduction losses introduced by the resonant link were found to be significant and much higher than predicted. The loss of fundamental output voltage that is due to the zero-voltage notches in the line-to-line voltages is another inherent drawback of the proposed technology. It has not been identified by previous publications where it was assumed that the zero-voltage period can be kept arbitrarily short. Even if this could be done (see discussion of zero-voltage gap in Section 5.4.3), finite amounts of time would be required to resonate the resonant link voltage to zero and back to the dc link voltage so volt-seconds would be lost in any case. The loss of fundamental can be kept in acceptable limits by making the zero-voltage time short which is also important in order to keep the losses in the resonant link low.

In order to achieve good output current quality and an improved conversion efficiency, the target switching frequency needs to be high and although this is one of the reasons why soft-switching has attracted a lot of interest, for the present topology it means that the resonant link devices have to switch at very high frequencies which appears unrealistic for medium to high output powers given the switching times of presently available IGBTs.

As an overall assessment of the potential for soft-switching inverters it can be stated that due to the problems of $\Sigma\Delta$ modulation that were discussed in Chapter 4, only

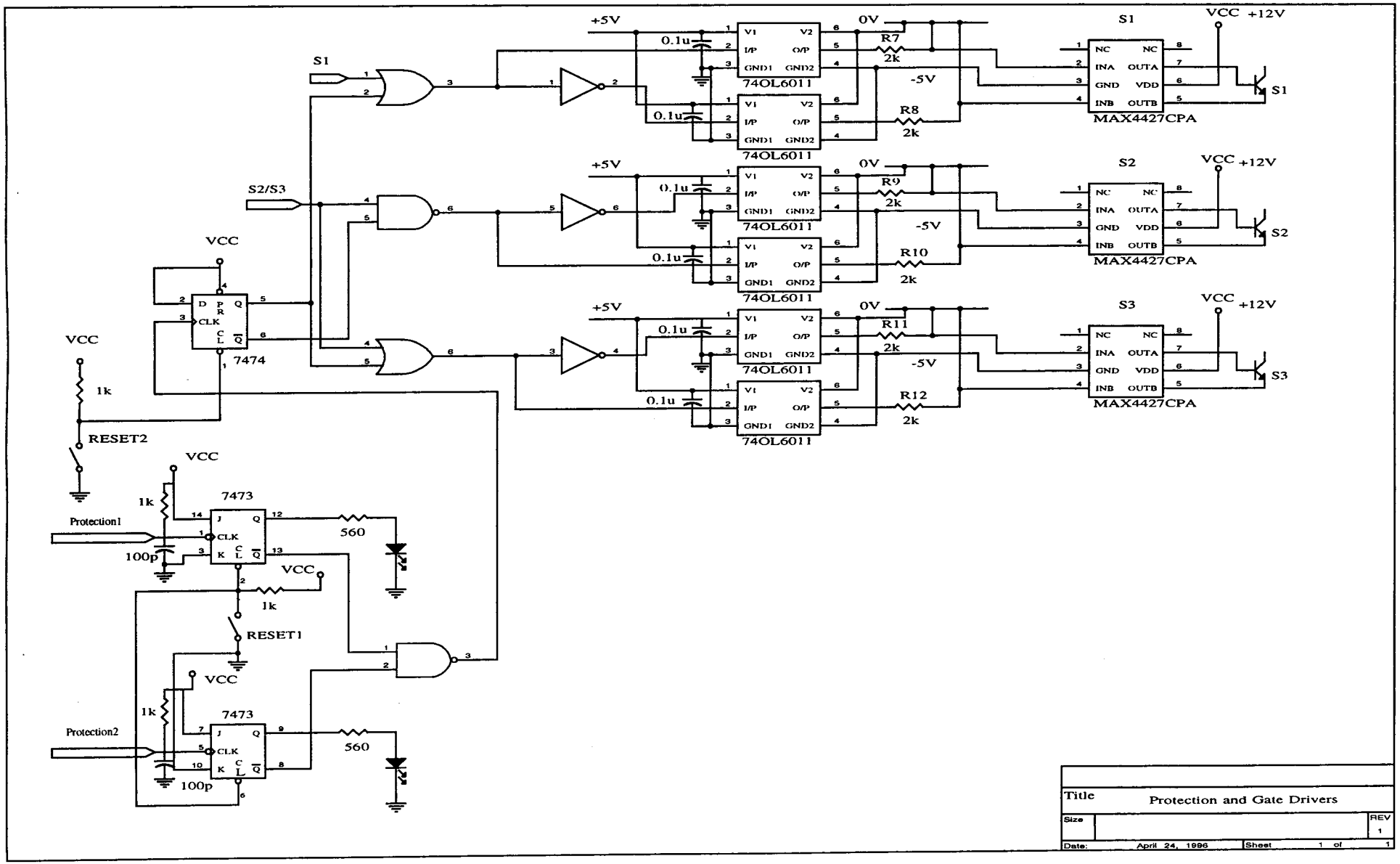
those resonant link schemes which are PWM compatible are likely to gain acceptance [52]. Any improvements of such circuits over traditional hard-switching inverters have to be weighed against their additional cost and complexity. It is likely that more significant advances in converter technology will continue to come from new developments in semiconductors rather than from new inverter topologies.

Appendix A

Circuit descriptions

A.1 Protection and gate drive circuits

The protection circuit has the task to protect the resonant link devices in the case of accidental short circuits or other conditions leading to currents that exceed the device ratings. Rather than turning all devices off, the protection circuit closes switches $S1$ and $S3$ to provide a path in which the resonant inductor current can circulate as was explained in Section 3.5.5. This is done by the arrangement of OR and AND gates that receive the gating signals (labeled S1 and S2/S3 in the circuit diagram given on the next page) and the protection signal at their inputs. The actual gate drivers are single-chip circuits (MAX4427CPA) with two separate inputs and outputs. They are supplied from a +12V supply and referenced to -5V. By driving the two inputs with signals of opposite polarities this leads to gate voltages of $\pm$17V. Between the gate drivers and the logic that controls them, six opto-couplers (740L6011) are used to provide electrical separation of the control circuit from the power circuit.


+5V
0V
-5V
0.1u
74OL6011
V1
V2
I/P
O/P
GND1
GND2
R7
R8
R9
R10
R11
R12
2k
S1
S2
S3
VCC +12V
NC
INA
OUTA
GND
VDD
INB
OUTB
MAX4427CPA
S2/S3
VCC
7474
D
PR
CLK
CL
Q
1k
RESET2
7473
J
K
100p
560
Protection1
Protection2
RESET1
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Protection and Gate Drivers
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REV
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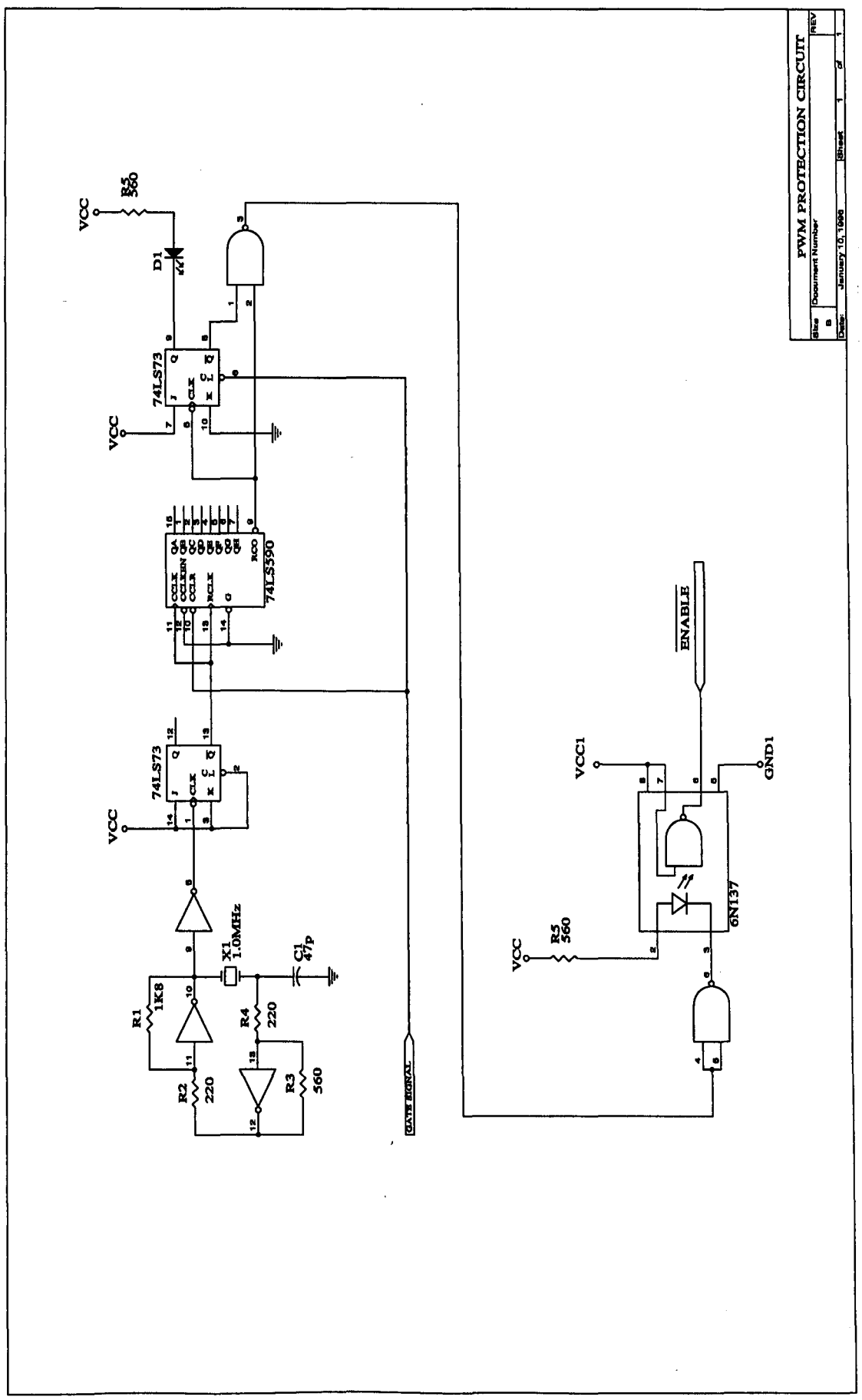
1 of 1

A.2 PWM watchdog



A.3 C011 link adaptor

The Inmos C011 link adaptor provides an interface between a serial link and a microprocessor system bus, via an 8-bit bi-directional interface. The message transmission is synchronised using handshaken byte streams. The C011 can be configured in one of two modes with two serial link speeds available for each mode. The configuration used in all the following circuits is mode 1 with a serial link speed of 20 Mbits/sec. Input to the link works as shown in the timing diagram below. **IValid** has to be taken high to notify the link adaptor that there is valid data present at the inputs **I0-I7**. The link adaptor then reads in the data through the serial link and acknowledges receipt on **IAck**. **IValid** is then taken low and the handshake is completed by taking **IAck** low. Output from the link adaptor is performed as shown in the next timing

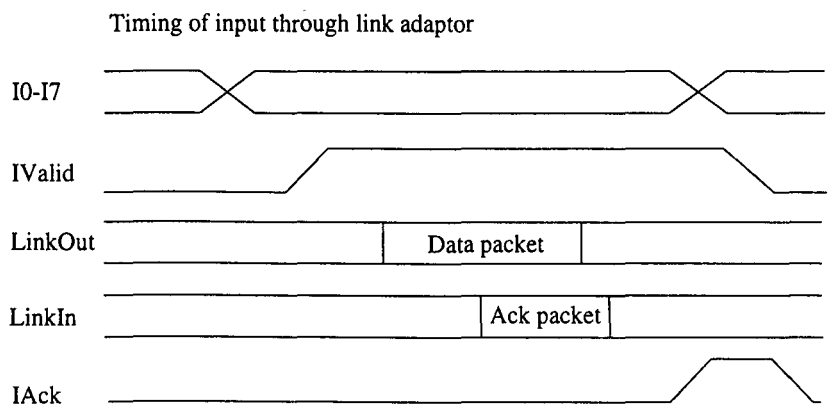
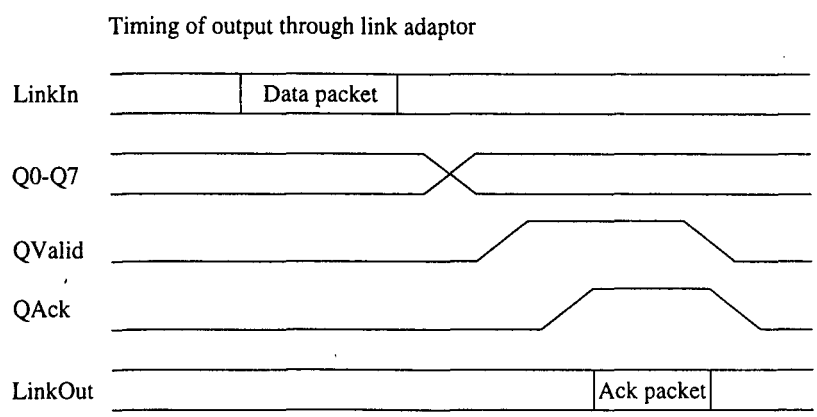
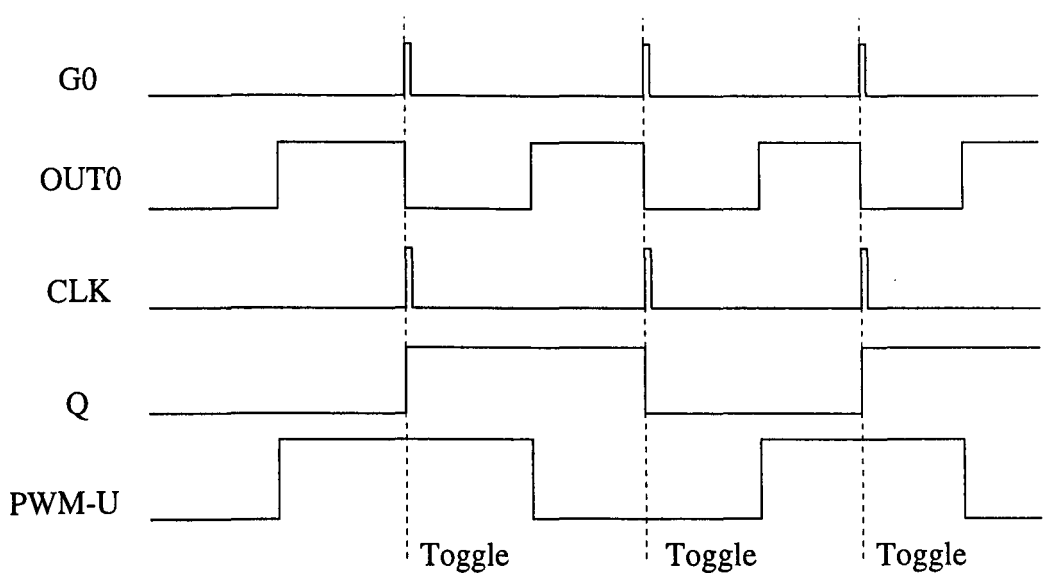


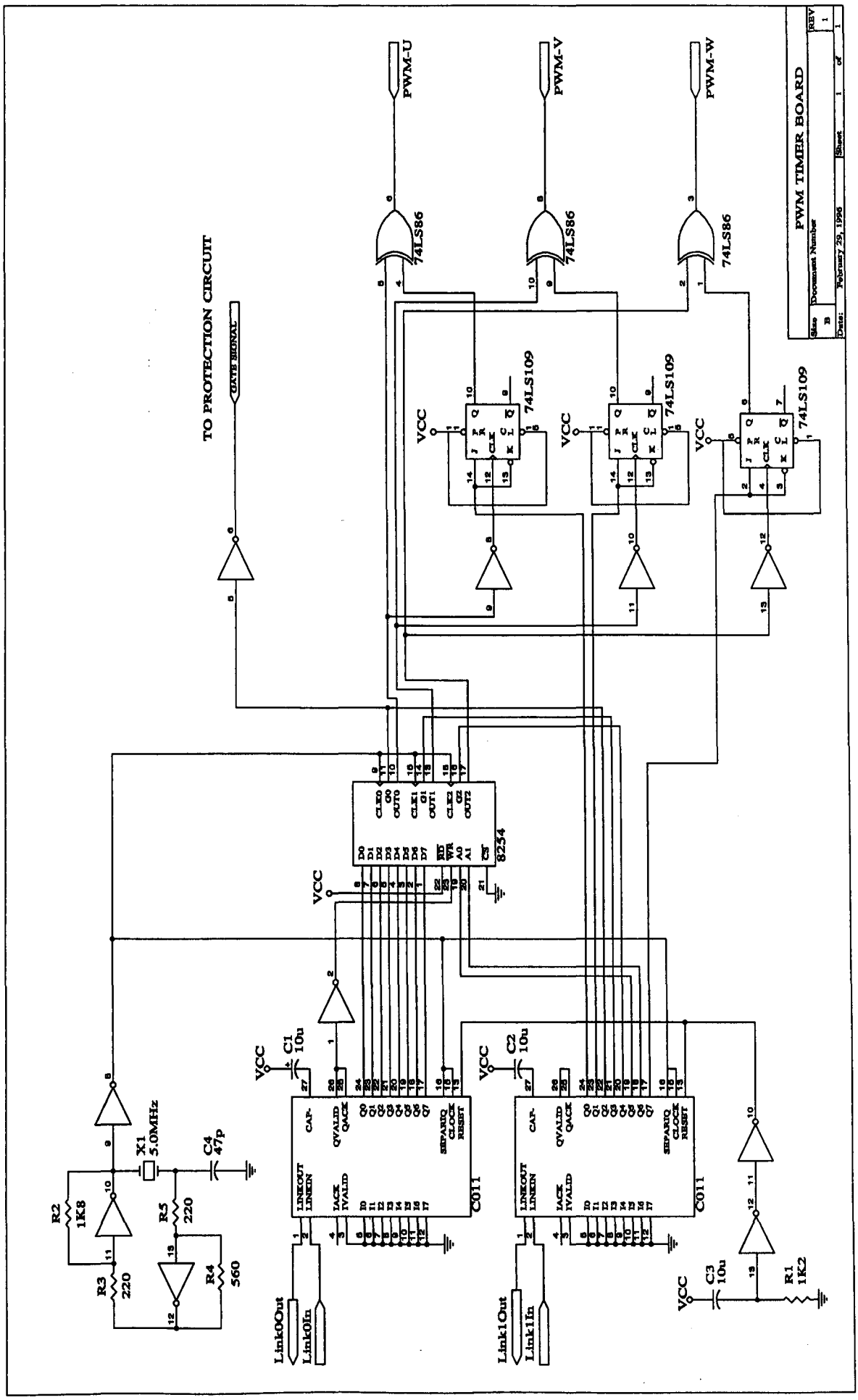
diagram. The link adaptor takes **Qvalid** high when data is ready at the outputs **Q0-Q7**. When the receiver acknowledges receipt of the data on **QAck**, **QValid** is taken low again and the handshake is completed by taking **QAck** low.



A.4 PWM generator circuit

The PWM generator circuit uses an Intel 8254 chip that contains three 16-Bit timers. Each timer is used to generate the gating signals for one inverter leg. When triggered, the output of each timer goes low and starts counting down from the value that has been loaded into it. When the count reaches zero, the output goes high again. A 5MHz crystal is used to generate a clock signal, allowing a resolution of 200ns for the PWM pulses and a maximum pulse duration of 32767 * 200ns=6.5534ms. One C011 link adaptor is used to address the 8254 chip through the two address lines **A0** and **A1** and for triggering the counters by pulling the pins **G0** to **G2** high. The other link adaptor initiates writing when valid data is present at its outputs by pulling **QValid** high and presents the data through the outputs **Q0** to **Q7** to the data inputs **D0** to **D7** of the 8254 timer. The diagram below shows how the combination of flip-flop (74LS109) and XOR gate (74LS86) produce a PWM signal for one inverter leg from the output **OUT0** of the timer circuit. **Q** and **CLK** denote outputs and inputs of the flip-flop and **G0** is the trigger input of the counter. Each time the output of the timer chip goes low, the flip-flop toggles its output state, which leads to the waveforms shown below. The trigger signal is also used as an input for the PWM watchdog circuit that was described in Section 3.5.5.




PWM TIMER BOARD
PWM-U
PWM-V
PWM-W
74LS86
74LS109
TO PROTECTION CIRCUIT
GATE SIGNAL
8254
C011
X1
5.0MHz
C4
47p
R2
1K8
R3
220
R4
560
R5
220
C1
10u
C2
10u
C3
10u
R1
1K2
VCC
Link0Out
Link0In
Link1Out
Link1In

A.5 Link control circuit

The link control circuit uses the same approach as the PWM generator circuit to produce gating pulses for the resonant devices S_1 to S_3. Two 8254 timer chips are supplied to create the pulses while a third timer chip is used to select the inputs of a multiplexer 74LS153. This is necessary because a PWM output period consists of three switching edges each of which requires separately timed pulses for the auxiliary switching devices. The multiplexer is used to select the appropriate timer outputs (**OUT0-OUT2**) and to apply their output signals to the gate drivers for S_1 to S_3. The maximum number of link adaptors that can be controlled by one transputer is three so that one link adaptor has to be used for loading two timers – one that outputs the gating pulses for S_1 and one that controls the multiplexer inputs. A common data bus is therefore used to supply data to two 8254 timer chips. One link adaptor loads the timer for S_2 and S_3 and one is supplied to address the timers by means of the address lines **A0** and **A1** when they are loaded.

The following three timing diagrams show how the link control circuit treats the three different situations that can occur under the modulation strategy that was described in Section 4.5.4. **A** and **B** are the multiplexer control lines that select which input is to be selected and **1C0** to **2C2** are the multiplexer inputs connected to the timer outputs. The switching times are labeled as 'Tabs' in the diagrams and are shown as dashed lines.

The first possible scenario is that no voltage vector needs to be dropped, ie. there are three distinct switching edges in one PWM output period. This situation is shown in Figure A.1.

If however one vector needs to be dropped, two phases in the inverter switch at the same time, ie. the 'Tabs' are identical. The situation where Tab1=Tab2 is shown in the figure below.

As can be seen the second input of the multiplexer is not selected in this case (**A** stays

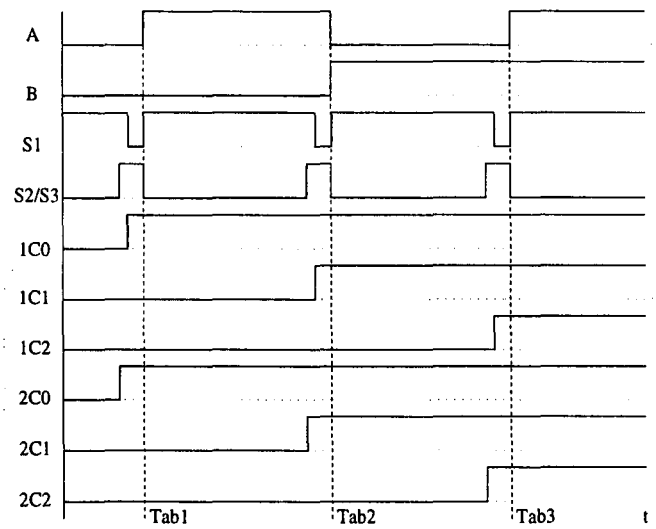


Figure A.1: Timing diagram when resonance is initiated for every switching edge.

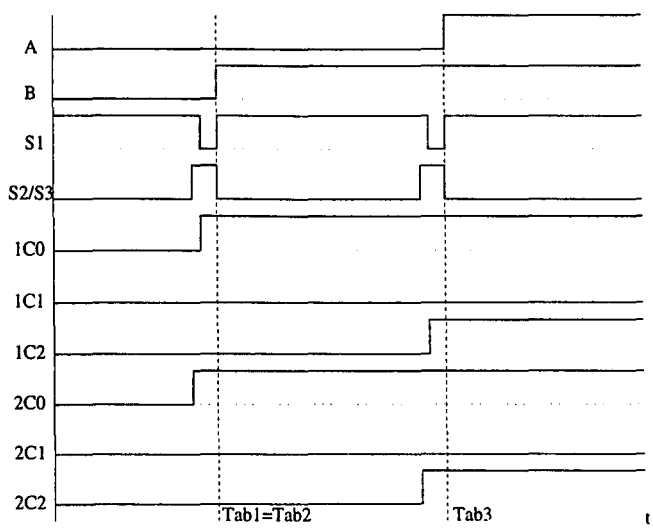


Figure A.2: Timing diagram for Tab1=Tab2.

low at t=Tab1). This means that the timer outputs for the second commutation are skipped since only two switching edges exist in this case. The third possible situation is similar and occurs when Tab2=Tab3. This case is shown below and it can be seen that the third input of the multiplexer is not selected.

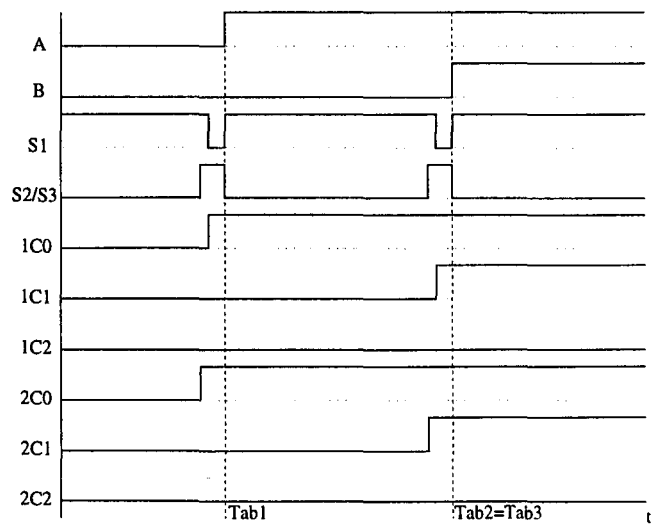
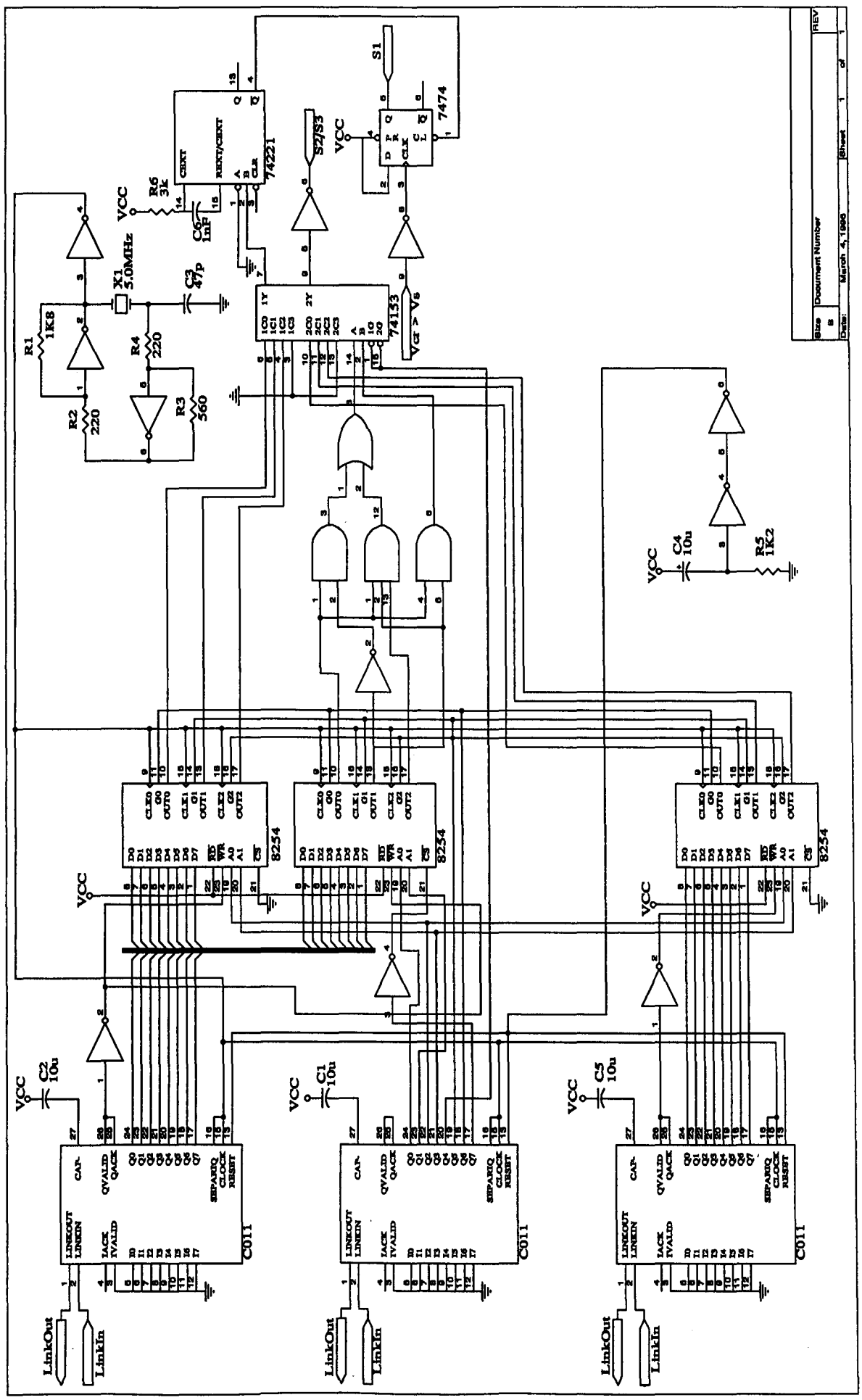
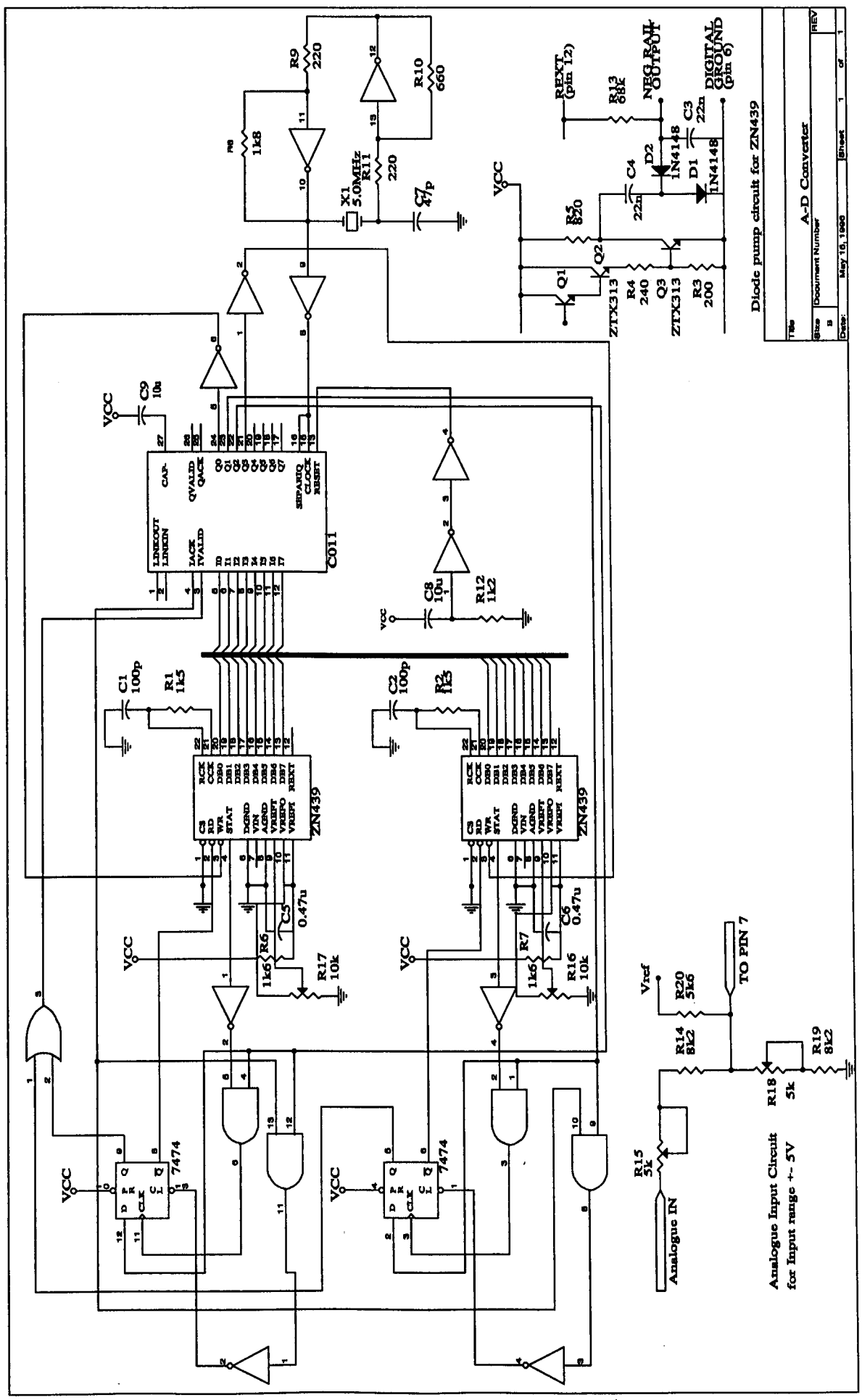


Figure A.3: Timing diagram for Tab2=Tab3.


S1
S2/S3
VCC
R6
31k
C6
1nF
74221
7474
X1
5.0MHz
C3
47p
74133
VCF > V6
R1
1K8
R4
220
R2
220
R3
560
C4
10u
R5
1K2
8254
C2
10u
C1
10u
C5
10u
C011
LinkOut
LinkIn
Size
Document Number
REV
Date: March 4, 1996
Sheet 1 of 1

A.6 AD-converter circuit

The A-D converter board uses two 8-Bit A-D converter chips (ZN439). A common data bus allows to read in the data of both converter chips through the same link adapter. Two A-D converters were chosen to allow simultaneous conversion of two phase currents. A number of logic gates and flip-flops allow control of both converters with the same link adaptor. A diode pump circuit is required to create a negative reference voltage at pin 12 of the ZN439 that is used by the comparators in the A-D converter. The already familiar 5MHz clock circuit is provided and a resistive divider is used to provide the appropriate input voltage at pin 7 of the A-D converter. The resistive divider is designed for an input voltage range of ± 5V.


Diode pump circuit for ZN439
A-D Converter
Analogue Input Circuit
for Input range +- 5V
Analogue IN
TO PIN 7
NEG RAIL OUTPUT
DIGITAL GROUND (pin 6)
REXT (pin 12)
VCC
Vref
ZN439
C011
7474
ZTX313
IN4148

Appendix B

Solution of PRDCL differential equations

The describing equations for modes 1,3 and 5 of a resonant transition in the PRDCL inverter are simple linear equations while modes 2 and 4 are governed by resonance between L_r and C_r. For these modes, the differential equations are solved using the Laplace transform technique. The durations of the resonant modes are also derived.

Mode 2 $[t_1, t_2]$**:** The Kirchhoff equations are:

$$v_{C_r} = v_{L_r} \tag{B.1}$$

$$i_{L_r} = -I_o - i_{C_r} \tag{B.2}$$

Currents and voltages in the resonant components are related by

$$v_{L_r} = L_r \frac{di_{L_r}}{dt} \tag{B.3}$$

$$i_{C_r} = C_r \frac{dv_{C_r}}{dt} \tag{B.4}$$

Hence we find

$$v_{L_r} = -L_r C_r \frac{d^2 v_{C_r}}{dt^2} \tag{B.5}$$

and

$$\frac{d^2 v_{C_r}}{dt^2} + \frac{1}{L_r C_r} v_{C_r} = 0 \tag{B.6}$$

This second-order differential equation is solved in the Laplace domain where the time-domain variable $v_{C_r}(t)$ becomes the s-domain variable $V_{C_r}(s)$.

$$s^2 V_{C_r} - s v_{C_r}(t_1) - \frac{dv_{C_r}}{dt}(t_1) + \frac{1}{L_r C_r} V_{C_r} = 0 \tag{B.7}$$

The initial conditions are:

$$v_{C_r}(t_1) = V_S \tag{B.8}$$

$$\frac{dv_{C_r}}{dt}(t_1) = \frac{i_{C_r}(t_1)}{C_r} = \frac{-i_{L_r}(t_1) - I_o}{C_r} = \frac{-I_i - I_o}{C_r} \tag{B.9}$$

Rearranging (B.7) gives

$$V_{C_r}(s) = v_{C_r}(t_1)\frac{s}{s^2 + 1/L_r C_r} + \frac{dv_{C_r}}{dt}(t_1)\frac{1}{s^2 + 1/L_r C_r} \tag{B.10}$$

With (B.8) and (B.9) the inverse Laplace transform of (B.10) yields

$$v_{C_r}(t) = V_S \cos\left(\frac{1}{\sqrt{L_r C_r}} t\right) + \left(\frac{-I_i - I_o}{C_r}\sqrt{L_r C_r}\sin\left(\frac{1}{\sqrt{L_r C_r}} t\right)\right) \tag{B.11}$$

Using the parameters $\omega_r = \frac{1}{\sqrt{L_r C_r}}$ and $Z_r = \sqrt{\frac{L_r}{C_r}}$ the solution becomes:

$$v_{C_r}(t) = V_S \cos(\omega_r t) - (I_i + I_o) Z_r \sin(\omega_r t) \tag{B.12}$$

To obtain an expression for the inductor current i_{L_r} we first derive i_{C_r}:

$$i_{C_r}(t) = C_r \frac{dv_{C_r}}{dt} = -\frac{V_S}{Z_r}\sin(\omega_r t) - (I_i + I_o)\cos(\omega_r t) \tag{B.13}$$

Using (B.2) gives:

$$i_{L_r}(t) = \frac{V_S}{Z_r}\sin(\omega_r t) + (I_i + I_o)\cos(\omega_r t) - I_o \tag{B.14}$$

This mode is finished when the voltage across C_r has reached zero. T_2 can therefore be obtained by:

$$V_S \cos(\omega_r T_2) - (I_i + I_o)\, Z_r \sin(\omega_r T_2) = 0 \tag{B.15}$$

$$T_2 = \frac{1}{\omega_r}\arctan\left(\frac{V_S}{Z_r(I_i + I_o)}\right) \tag{B.16}$$

Mode 4 $[t_3, t_4]$: For this mode, the Kirchhoff equations are:

$$v_{C_r} = -v_{L_r} \tag{B.17}$$

$$i_{L_r} = I_{ox} + i_{C_r} \tag{B.18}$$

The relations between currents and voltages in the resonant components are again given by (B.3) and (B.4). Thus

$$v_{L_r} = L_r C_r \frac{d^2 v_{C_r}}{dt^2} \tag{B.19}$$

and

$$\frac{d^2 v_{C_r}}{dt^2} + \frac{1}{L_r C_r} v_{C_r} = 0 \tag{B.20}$$

In the Laplace domain this gives:

$$s^2 V_{C_r} - s v_{C_r}(t_3) - \frac{dv_{C_r}}{dt}(t_3) + \frac{1}{L_r C_r} V_{C_r} = 0 \tag{B.21}$$

The initial conditions are:

$$v_{C_r}(t_3) = 0 \tag{B.22}$$

$$\frac{dv_{C_r}}{dt}(t_3) = \frac{i_{C_r}(t_3)}{C_r} = \frac{i_{L_r}(t_3) - I_{ox}}{C_r} = \frac{I_p - I_{ox}}{C_r} \tag{B.23}$$

Rearranging (B.21) gives

$$V_{C_r}(s) = \frac{I_p - I_{ox}}{C_r} \left(\frac{1}{s^2 + 1/L_r C_r} \right) \tag{B.24}$$

Using (B.22) and (B.23) the inverse Laplace transform of (B.24) gives

$$v_{C_r}(t) = \frac{I_p - I_{ox}}{C_r} \sqrt{L_r C_r} \sin\left(\frac{1}{\sqrt{L_r C_r}} t \right) \tag{B.25}$$

and finally

$$v_{C_r}(t) = (I_p - I_{ox}) Z_r \sin(\omega_r t) \tag{B.26}$$

The current i_{C_r} is given by:

$$i_{C_r}(t) = C_r \frac{dv_{C_r}}{dt} = (I_p - I_{ox}) \cos(\omega_r t) \tag{B.27}$$

Using (B.18) gives:

$$i_{L_r}(t) = (I_p - I_{ox}) \cos(\omega_r t) + I_{ox} \tag{B.28}$$

Mode 4 is finished when the voltage v_{C_r} reaches V_S. Its duration can therefore be obtained by:

$$(I_p - I_{ox}) Z_r \sin(\omega_r T_4) = V_S \tag{B.29}$$

$$T_4 = \frac{1}{\omega_r} \arcsin\left(\frac{V_S}{Z_r(I_p - I_{ox})}\right) \tag{B.30}$$

Appendix C

Current prediction

Consider inequality (C.1) which can be used to determine the required initial current for a resonant transition (cf. Section 3.3.3).

$$I_i \geq \sqrt{\left(\frac{V_S}{Z_r} + I_o + I_{ox}\right)^2 - \left(\frac{V_S}{Z_r}\right)^2} - I_o \tag{C.1}$$

To find out for which values of I_o and I_{ox} the calculation has a real result substitute A for $(I_o + I_{ox})$.

$$\begin{aligned} I_i &\geq \sqrt{\left(\frac{V_S}{Z_r} + A\right)^2 - \left(\frac{V_S}{Z_r}\right)^2} - I_o \\ I_i &\geq \sqrt{A^2 + 2A\frac{V_S}{Z_r}} - I_o \end{aligned} \tag{C.2}$$

A real result can only be obtained when the term under the square root is not negative, hence to find out for which values of A the result will be imaginary, we write

$$\begin{aligned} A^2 + 2A\frac{V_S}{Z_r} &< 0 \\ A + 2\frac{V_S}{Z_r} &< 0 \qquad\qquad (A > 0) \\ A &< -2\frac{V_S}{Z_r}. \end{aligned} \tag{C.3}$$

Since both V_S and Z_r are positive constants, the inequality (C.3) cannot be satisfied for positive A which means that (C.1) has a real result whenever $(I_o + I_{ox}) \geq 0$. For

negative A, the inequality becomes

$$A + 2\frac{V_S}{Z_r} > 0 \qquad (A < 0) \tag{C.4}$$

$$A > -2\frac{V_S}{Z_r} \tag{C.5}$$

Imaginary results therefore occur for $(-2\frac{V_S}{Z_r} < A < 0)$. To obtain real values for the required initial current even when (C.1) has imarginary results the techniques explained in Section 3.5.1 are applied.

Appendix D

Conduction losses

The IGBT modules used in the inverter are Mitsubishi's CM100DY-24H. No values for V_T, V_D and R_T, R_D respectively are given in the data sheet [58] but instead the voltage drops for the IGBT and the antiparallel diode are read from the graphs given in [58] for the given RMS value of current I_{ref} and these are then used to determine the instantaneous power loss. The analysis is then carried out as described in Section 5.4.1. Note that the voltage drops are determined for a certain current level and hence are not functions of time in the following analysis. They are therefore introduced as constants $V_{T_{drop}}$ and $V_{D_{drop}}$.

According to [27], the phase-to-midpoint voltage for space vector modulation is given by

$$V_{SVM} = \begin{cases} \frac{3}{2}\sin(\omega t) & 0 \leq \omega t \leq \frac{\pi}{6} \\ \\ \frac{\sqrt{3}}{2}\sin\left(\omega t + \frac{\pi}{6}\right) & \frac{\pi}{6} \leq \omega t \leq \frac{\pi}{2} \end{cases} \tag{D.1}$$

The method described in Section 5.4.1 can therefore be applied to evaluate the conduction loss under space vector modulation. To obtain the conduction loss for one transistor and its antiparallel diode, we split the integral in (5.15) into two parts:

$$P_{T_{11}} = \frac{1}{\pi}\int_{\phi}^{\phi+\frac{\pi}{6}} \left(\frac{1}{2} + \frac{3}{4}k\sin(\omega_r t)\right)\left(V_{T_{drop}}\sqrt{2}I_{ref}\sin(\omega_r t - \phi)\right) d\omega_r t \tag{D.2}$$

$$P_{T_{12}} = \frac{1}{\pi}\int_{\phi+\frac{\pi}{6}}^{\phi+\frac{\pi}{2}} \left(\frac{1}{2} + \frac{1}{4}\sqrt{3}k\sin\left(\omega_r t + \frac{\pi}{6}\right)\right)\left(V_{T_{drop}}\sqrt{2}I_{ref}\sin(\omega_r t - \phi)\right) d\omega_r t \quad \text{(D.3)}$$

The sum of these two integrals gives us the conduction loss per transistor:

$$P_{T_1} = P_{T_{11}} + P_{T_{12}} \quad \text{(D.4)}$$

The same approach is taken with (5.16):

$$P_{D_{21}} = \frac{1}{\pi}\int_{\phi}^{\phi+\frac{\pi}{6}} \left(\frac{1}{2} - \frac{3}{4}k\sin(\omega_r t)\right)\left(V_{D_{drop}}\sqrt{2}I_{ref}\sin(\omega_r t - \phi)\right) d\omega_r t \quad \text{(D.5)}$$

$$P_{D_{22}} = \frac{1}{\pi}\int_{\phi+\frac{\pi}{6}}^{\phi+\frac{\pi}{2}} \left(\frac{1}{2} - \frac{1}{4}\sqrt{3}k\sin\left(\omega_r t + \frac{\pi}{6}\right)\right)\left(V_{D_{drop}}\sqrt{2}I_{ref}\sin(\omega_r t - \phi)\right) d\omega_r t \quad \text{(D.6)}$$

The conduction loss per diode is then obtained by

$$P_{D_2} = P_{D_{21}} + P_{D_{22}} \quad \text{(D.7)}$$

and the total conduction loss in the inverter is given by

$$P_{cd} = 6(P_{T_1} + P_{D_2}). \quad \text{(D.8)}$$

Solving the integrals in (D.2, D.3 and D.5, D.6), we can derive P_{T_1} as

$$P_{T_1} = \frac{\sqrt{2}I_{ref}}{48\pi}V_{T_{drop}}\left(6k\pi\cos\phi + 9k\sin\phi - \sqrt{3}k\pi\sin\phi + 24\right) \quad \text{(D.9)}$$

and P_{D_2} as

$$P_{D_2} = \frac{\sqrt{2}I_{ref}}{48\pi}V_{D_{drop}}\left(\sqrt{3}k\pi\sin\phi + 24 - 6k\pi\cos\phi - 9k\sin\phi\right). \quad \text{(D.10)}$$

Appendix E

Information from data sheets

Symbol	Parameter	Test conditions	Min	Typ	Max	Unit
$V_{CE(sat)}$	Collector-emitter saturation voltage	$T_j = 25^oC$ $I_C = 100A$,	-	2.5	3.4	V
		$T_j = 125^oC$ V_{GE} =15V	-	2.25	-	V
$t_{d(on)}$	Turn-on delay time	$V_{CC} = 600V$, $I_C = 100A$	-	-	250	ns
t_r	Turn-on rise time	$V_{GE} = 15V$	-	-	350	ns
$t_{d(off)}$	Turn-off delay time	$R_G = 3.1\Omega$	-	-	300	ns
t_f	Turn-off fall time	Resistive load switching	-	-	350	ns
V_{EC}	Emitter-collector voltage	$I_E = 100A$, $V_{GE} = 0V$	-	-	3.5	V
t_{rr}	Reverse recovery time	$I_E = 100A$, $di_E/dt = -200A/\mu s$	-	-	250	ns

Table E.1: Electrical characteristics for CM100DY-24H IGBT module.

Symbol	Parameter	Test conditions	Min	Typ	Max	Unit
$V_{CE(sat)}$	Collector-emitter saturation voltage	$I_C = 39A$	-	1.4	1.7	V
		$I_C = 70A$	-	2.0	-	V
		$I_C = 39A$, $T_j = 150^oC$	-	1.7	-	V
$t_{d(on)}$	Turn-on delay time	$V_{CC} = 480V$, $I_C = 39A$	-	24	-	ns
t_r	Turn-on rise time	$V_{GE} = 15V$	-	50	-	ns
$t_{d(off)}$	Turn-off delay time	$R_G = 5\Omega$	-	270	540	ns
t_f	Turn-off fall time		-	210	360	ns

Table E.2: Electrical characteristics for IRGPC50F IGBT; $T_j = 25^oC$ unless otherwise specified.

Parameter	Value
V_1	0.871
V_2	$-1.92 \times 10-3$
a_1	0.045
a_2	1.19×10^{-4}
b_1	0.751
b_2	2.87×10^{-4}

Table E.3: Conduction model parameters for IRGPC50F IGBT.

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