Characterization and Emulation of a New Supercapacitor-type Energy Storage Device

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Abstract

The work in this thesis focuses on the characterization, modeling and emulation of both the supercapacitor and the new supercapattery energy storage device. The characterization involves the selection of dynamic models and experimental methodologies to derive model parameters. The characterizing processes focus on predicting short-term device dynamics, energy retention (self-discharging) and losses and round-trip efficiency. A methodology involving a pulse current method is applied for the first time to identify a model parameter to give fast device dynamic characteristics and a new constant power cycling method is used for evaluating round-trip efficiency. Experimental results are shown for a number of supercapacitor and supercapattery devices and good results are obtained. The derived models from the characterization results are implemented into the emulator system and the emulator system is used to mimic the dynamic characteristics of a scaled-up 1kW supercapattery device. The thesis also addresses voltage equalizing circuits and reports a study that investigates efficiency, a cell voltage deviation and voltage equalizing time for different control methods.

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List of Acronyms

ADC	an analog-to-digital converter unit
BW	bandwidth
CAPCOM	capture and compare unit
CC	the constant current cycling method
CCC	the constant current cycling method
CCM	continuous conduction mode
CNTs	carbon nanotubes
CPC	the constant power cycling method
CPLD	complex programmable logic device
CV	the constant voltage method
DAC	a digital-to-analog converter unit
DCM	discontinuous conduction mode
DSP	digital signal processor
DUT	device under test
EIS	an electrochemical impedance spectroscopy
FFT	Fast Fourier Transform

FPGA	field-programmable gate array
FSR	Full scale range
GEIS	galvano-electrochemical impedance spectroscopy
GM	gain margin
HEV	Hybrid electric vehicle
HIL	hardware in loop
KCL	Kirchhoff's current law
LUT	look-up table algorithm
NTC	negative temperature coefficient
PCC	the pulse constant current method
PEIS	potentio-electrochemical impedance spectroscopy
PI	proportional and integral controller
PM	phase margin
PSU	power supply unit
PV	photovoltaic
PWM	pulse width modulation
RMS	root mean square
SC	supercapacitors and supercapatteries
SCP	supercapattery
SDVC	self-discharging voltage or potential decay
SOC	supercapacitor state of charge

List of Symbols

ω	angular frequency (rad/s)
τ	complex pore time constant
μC	microcontroller
τ_N	RC time constants at the time range N^{th}
η_{RT}	charge-discharge (round-trip) efficiency
η_{RT_EXP}	experimental round-trip efficiency
η_{EST_Duty}	estimated round-trip efficiency from the charge-discharge duty cycle
η_{EST_V}	estimated voltage-based round-trip efficiency
α	learning factor in Gauss-Newton algorithm
Δ	increment factor in Gauss-Newton algorithm
ΔV	step voltage at the beginning/ending of the charging/discharging period
ΔV_{Max}	maximum cell voltage deviation between the maximum cell voltage and the minimum cell voltage within the same series-connected stack
$\Delta\eta_{RT}$	error between the estimated and the experimental round-trip efficiency

ΔE_{Loss}	error between the estimated and the experimental round-trip energy loss
ΣR_S	sum of series resistance of InterCell transformers
ΣL_L	sum of leakage inductance of InterCell transformers
a	polynomial coefficient of nominator terms in z-domain
A	polynomial coefficient of nominator terms in s-domain
b	polynomial coefficient of denominator terms in z-domain
B	polynomial coefficient of denominator terms in s-domain
C	ideal capacitance
C_0	initial capacitance
$Cell$	battery or supercapacitor cells
C_a	auxiliary capacitor for voltage equalizers
C_{add}	capacitance of the additional RC branch in model IV_2
C_d	delay branch capacitance
C_{DL}	double layer capacitance (induced by the electrical potential at the electrode/electrolyte interface)
C_{EMU}	filtered capacitor for emulator system
C_i	immediate branch capacitance
C_{in}	input capacitor for voltage equalizers
C_l	long-term branch capacitance
C_S	series capacitance
C_T	intermediate energy storage capacitors for voltage equalizers

C_V	voltage-dependent capacitance (F/V)
d	duty cycle
d_{CD}	charge-discharge duty cycle
d_{Eq}	equalizing duty cycle
D	diodes for voltage equalizers
D_{Cond}	cell diode conduction loss
D_{Sw}	cell diode switching loss
E_C	charging energy
$E_{C\_EST\_V}$	estimated voltage-based charging energy
E_D	discharging energy
$E_{D\_EST\_V}$	estimated voltage-based discharging energy
E_{Loss_charge}	charging energy loss
E_{Loss_EST}	estimated charge-discharge (round-trip) energy loss
$E_{Loss\_EST\_I}$	estimated current-based round-trip energy loss
$E_{Loss\_EST\_IFFT}$	estimated current-based round-trip energy loss with the FFT
$E_{Loss\_EST\_V}$	estimated voltage-based round-trip energy loss
E_{Loss_RT}	charge-discharge (round-trip) energy loss
E_{Stored}	the maximum stored energy inside a fly-back transformer
E_{Stored_Stack}	stored energy inside the supercapacitor stack
EPR	equivalent parallel resistance
EPR_{I_Leak}	equivalent parallel resistance derived from supercapacitor leakage current

EPR_{SDVC}	equivalent parallel resistance derived from supercapacitor self-discharge voltage characteristic
$Error$	error between the model impedance and the actual impedance
ESR	equivalent series resistance
ESR_k	equivalent series resistance at a frequency k^{th}
ESR_{period}	supercapacitor equivalent series resistance at a frequency of charge-discharge cycling period
ESR_W	transformer winding resistance
f_{CD}	charge-discharge cycling frequency, which a reciprocal of T_{CD}.
f_{sw}	switching frequency
f_{sw_eq}	equivalent switching frequency at the emulator output response
$i_{Charger}$	instantaneous charging current either for the supercapacitor stack or the emulator
i_{CH}	instantaneous emulator channel current
i_{CH}^{*}	instantaneous emulator channel current reference
i_{EMU}	emulator current
i_{EMU}^{*}	emulator current reference
i_j	instantaneous current at each sampling point j^{th}
i_{leak}	leakage current
i_L	inductor current of Rig I
i_{SC}	instantaneous current applied to the supercapacitor in time domain

i_{SC_Ref}	instantaneous supercapacitor current reference output from the DAC unit of Rig I
$\hat{i}_{TP}$	peak transformer primary winding current
i_{TP}	transformer primary winding current
i_{TS}	transformer secondary winding currents
I_{ch}	constant charging current applied to the supercapacitor
I_{Cell}	constant supercapacitor cell currents
I_{disch}	constant discharging current applied to the supercapacitor
I_{ds_max}	MOSFET rated drain-source current
I_{CH}	emulator channel current in s-domain
I_{EMU}	emulator current in s-domain or z-domain
I_{F_max}	diode rated forward current
I_k	harmonic current at a frequency k^{th}
I_{leak}	leakage current or floating current
I_P	constant current pulse
$I_{response}$	current response of a supercapacitor after applying the voltage signal
$I_{R\_dissipate}$	cell dissipative current
I_{SC}	instantaneous current applied to the supercapacitor in s-domain
I_{SC_cmin}	minimum supercapacitor current during the charging period in the constant power cycling mode
I_{SC_cmax}	maximum supercapacitor current during the charging period in the constant power cycling mode

I_{SC_dmin}	minimum supercapacitor current during the discharging period in the constant power cycling mode
I_{SC_dmax}	maximum supercapacitor current during the discharging period in the constant power cycling mode
I_{SC_max}	maximum supercapacitor charge-discharge current (equivalent to the supercapacitor rated current)
J	Jacobian matrix
K_{P_I}	proportional gain of the current controller
K_{P_V}	proportional gain of the voltage controller
K_{I_I}	integral gain of the current controller
K_{I_V}	integral gain of the voltage controller
L_i	intermediate energy storage inductors for voltage equalizers
L_{in}	input inductor for voltage equalizers
L_L	leakage inductance
L_m *or* L_M	magnetizing inductance
L_N	lower boundaries of RC time constants at the time range N^{th}
L_{P_Leak}	leakage inductance of the transformer primary winding
L_S	series inductance
L_{S_Leak}	leakage inductance of the transformer secondary winding
M	modulation index for controlling the emulator
M_P	time multiplying factor
n	number of supercapacitor cells connected in series
n_p	number of experimental data point used in fitting algorithm

N	number of parallel RC branches or number of series-connected cells
N_a	transformer turn ratio (= N_P:N_S)
N_{CH}	number of interleaved channel
N_{Har}	number of harmonics
N_P	primary winding turns of a transformer
N_S	secondary winding turns of a transformer
N_{Samp}	number of sample points over a single charge-discharge period
N_{ZP}	number of a single impedance connected in parallel
N_{ZS}	number of a single impedance connected in series
p_{EMU}	instantaneous emulator power reference (the product of the emulator current and the emulator voltage)
p_j	calculated instantaneous power at each sampling point j^{th}
p_{SC}	instantaneous power applied to the supercapacitor (the product of the supercapacitor current and the supercapacitor voltage)
p_{SC_Ref}	instantaneous supercapacitor power reference
P	constant power
P_C	constant charging power level
P_{C_avrg}	average charging power
P_D	constant discharging power level
P_{D_avrg}	average discharging power discharge cycling period
P_{IFFT_k}	harmonic power loss at a frequency k^{th} algorithm
P_{SC}	the applied constant power at the supercapacitor terminals

Q	switching device
Q_{Cond}	MOSFET conduction loss
QD_{Cond}	anti-parallel diode conduction loss
QD_{Sw}	anti-parallel diode switching loss
Q_{Sw}	MOSFET switching loss
R^2	R-square
R_{add}	resistance of the additional RC branch in model IV_2
R_C	current collector resistance
R_d	delay branch resistance
R_{Dump}	energy dumping resistor
R_{el}	electrolyte resistance (deduced from the electrolyte conductivity)
R_i	immediate branch resistance
R_{In}	interface resistance from the rough aspect of the electrode/electrolyte interface
R_l	long-term branch resistance
R_{Pri}	resistance of the transformer primary winding
R_{sense}	shunt resistance current
R_S	series resistance
R_{Sec}	resistance of the transformer secondary winding
$R_{Separator}$	separator resistance
$RMSE$	root-mean-square error
s	s-domain parameter

SSE	sum-of-square error
STD	standard deviation
t_i	start time of the integration time interval
t_f	final time of the integration time interval
T_C	charging period
T_{CD}	charge-discharge period
T_D	discharging period
T_{Eq}	equalizing period
T_P	pulse period
T_S	sensor sampling frequency
T_{Samp}	sampling time interval
T_{SC}	supercapacitor surface temperature
TEL	total equalizing loss (as a percentage of the charging energy loss)
v_C	instantaneous voltage across ideal capacitor
v_{EMU}	emulator terminal voltage
v_{EMU}^*	emulator terminal voltage reference
v_{Lm}	voltage across the magnetizing inductance of the fly-back transformer
v_{SC}	supercapacitor instantaneous terminal voltage in time domain
v_{Stack}	SC stack voltage
$V_{applied}$	applied voltage signal
V_{avrg}	average voltage from V_i and V_f in the PCC method

$V_{Average}$	mean value of cell voltages of series-connected stack
V_{bias}	applied bias voltage across supercapacitors
V_C	voltage across ideal capacitors
V_{C0}	voltage across initial capacitance C_0
V_{CH}	applied voltage of an interleaved channel
V_{Cmin}	ideal capacitor voltage at the end of the discharging mode or the beginning of the charging mode
V_{Cmax}	ideal capacitor voltage at the end of the charging mode or the beginning of the discharging mode
V_{ds_max}	MOSFET rated drain-source voltage
V_{EMU}	emulator terminal voltage in s-domain or z-domain
V_{EMU}^{*}	emulator terminal voltage reference in s-domain or z-domain
V_f	steady-state final supercapacitor voltage measured across terminals
V_F	diode forward voltage drops
V_i	steady-state initial supercapacitor voltage measured across terminals
V_P	supercapacitor cell voltage measured across terminals
V_{r_max}	diode rated reverse voltage
V_{Rated}	cell rated voltage
V_S	constant voltage source
V_{SC}	supercapacitor instantaneous terminal voltage in s domain
V_{SC_cmin}	minimum SC terminal voltages during the charging period in the constant power cycling mode

V_{SC_cmax}	maximum SC terminal voltages during the charging period in the constant power cycling mode
V_{SC_dmin}	minimum SC terminal voltages during the discharging period in the constant power cycling mode
V_{SC_dmax}	maximum SC terminal voltages during the discharging period in the constant power cycling mode
x_{EST}	estimated data points
x_{EXP}	experimental data points
$\overline{x}_{EXP}$	mean value of experimental data points
X_k	fitting coefficient
Y_k	fitting time constant
z	z-domain parameter
Z	single impedance
Z_{add}	additional parallel RC branch of the SC model IV_2
Z_P	parallel-connected impedance
Z_{Pore}	complex pore impedance
Z_S	series-connected impedance
Z_{SC}	supercapacitor actual complex impedance
Z_{SC_est}	model impedance
Z_{SC_I}	model I: the adaptive series-connected RC model
Z_{SC_II}	model II: the transmission-line RC mode
Z_{SC_III}	model III: the parallel RC branch model

Z_{SC_IV}	model IV: the series-parallel RC model
$Z_{SC\_IV\_2}$	model IV_2: the series-parallel RC model with an additional RC branch
$Z_{SC\_IV\_3}$	model IV_3: the series-parallel RC model without a series inductance L_S
Z_{SC_V}	model V: the combined model between series-parallel and parallel-branch RC models
Z_{SP}	series-parallel-connected impedance

Chapter 1 Introduction

The current trend in electrical generation, distribution and transmission is developing towards a smart grid concept. For this concept to be applied it is essential to have more energy storage units integrated with an existing electrical grid [1,2]. For grid applications, several energy storage technologies are considered. Stored energy can be revised in different mediums and forms, for example, pumped hydro and compressed air (potential energy), battery and supercapacitor (chemical energy), flywheel (mechanical kinetic energy) and superconductive magnetic (magnetic energy) [3]. Each energy storage technology has its own limitation in terms of specific power (kW/kg), specific energy (kWh/kg), energy retention period, life cycle and so on as discussed in [3]. Note that large-scale superconductive magnetic and fly-wheel energy storage are generally not thought to be feasible due to cost and safety reasons [4]. Thus, these two energy storages will not be discussed further.

In utility scale applications (e.g. load leveling), pumped hydro and compressed air have been in-use for decades [4]. However, the location and size of these technologies are limited geographically and geologically. Many of the feasible sites have been exploited already [5]. Since this infrastructure is usually located in remote areas, the electricity cost in transmission and distribution to the point-of-loads during peak time would be more than that of distributed energy storage types [2,6]. In addition, renewable energy penetration (e.g. from wind and PV) to the grid has increased [7], which encourages the deployment of energy storage units at these sites to avoid transmission-line power congestion and help power smoothing [8]. Therefore, a wide variety of alternative storage media are being investigated and developed toward the distributed energy storage concept.

Electrochemical energy storage (e.g. battery, supercapacitor, fuel cell etc.) seems to be a suitable solution since they can be expanded to large scale [9]. Electrochemical energy storage also has a high round-trip efficiency and do not have geographical limitations [2,3]. However, the main drawback of electrochemical energy storage is life-cycle time and cost. For this reason, the issues of long-life and low-cost electrochemical energy storage have gained public interest. New electrochemical energy storages are required to have (i) long life (ii) low cost (iii) high specific energy and (iv) high specific power, so that energy management schemes can become more flexible and effective against intermittent energy from renewable energy sources and peak load demand.

At the present time, there is no electrochemical storage device that can provide suitable solutions for many applications, so a hybrid energy storage system is realized from high specific energy and high specific power devices to fulfil the requirements [10]. For example, in automotive and micro-grid applications, a combination of batteries and supercapacitors are used [3,11-13]. The supercapacitors have a long lifetime in terms of charge cycles (e.g. 1 million cycles), high specific power and wide operating temperature range, but they have low specific energy. On the other hand, batteries have higher specific energy but lower specific power than that of supercapacitors. Batteries are also sensitive to operating temperature, and they require an accurate charge profile to increase their lifetime. Therefore, hybridizing these two technologies improves each individual limitation, which results in a higher system efficiency and an extended battery life [14].

1.1 The Supercapatteries

Alternatively, it would be good if supercapacitors could have higher specific energy, so batteries can be excluded from the system. This idea has led to a novel energy storage device, the “supercapattery”, which is being developed at the University of Nottingham [15,16]. The supercapattery is reported to have higher specific energy than commercially available supercapacitors and higher specific power than conventional lead-acid batteries. Its place on Ragone plot compared to other well-known energy storage devices is illustrated in Figure 1.1.

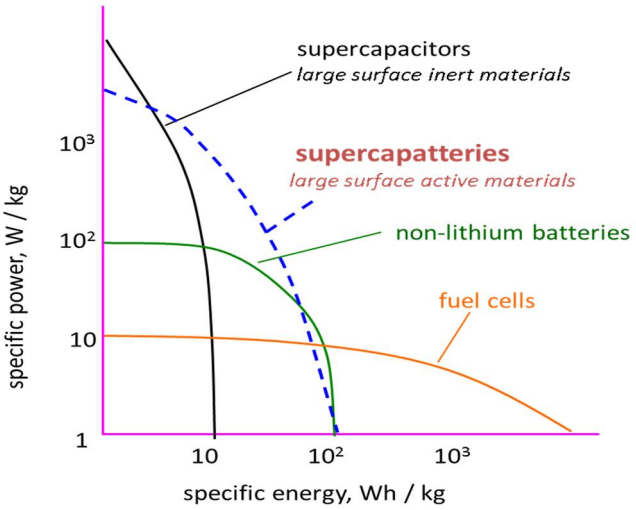


Figure 1.1 Ragone plot in simplistic view to show the comparison of specific power versus specific energy characteristics between different types of electrochemical devices

The supercapattery technology is based on carbon nanotubes (CNTs) [17-19] working in an aqueous electrolyte while commercial supercapacitor technology is based on activated carbon with an organic electrolyte. The CNTs inside the supercapattery is depicted in Figure 1.2. The CNTs increase the electrode accessible surface area, so that more charges can be stored, which in turn, increases specific energy. The CNT technology is expected to enhance specific energy of commercial supercapacitors by approximately four times [15,20]. Particularly, laboratory supercapattery samples have been considered to form stacks having a specific energy =20.3 Wh/kg, and a specific power = max 143.7 kW/kg [21]. More details will be given in Section 3.2.

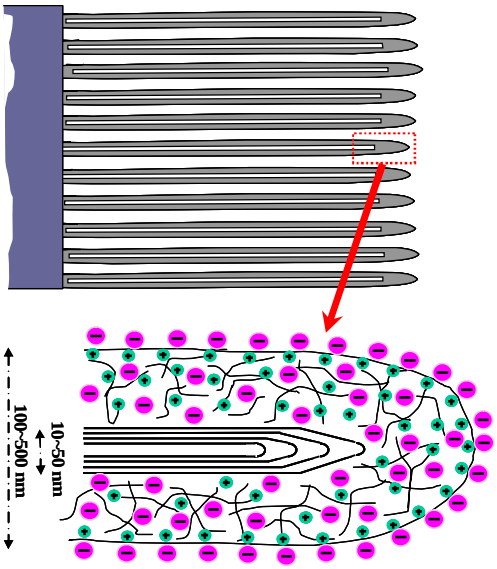


Figure 1.2 Improved charge conduction and penetration by employing porous composites of carbon nanotubes and redox materials (3rd generation supercapacitor) [19]

The supercapattery is safe and environmental friendly. The supercapattery life cycle is expected to be very high since the charge-storing mechanism is completely reversible. Therefore, the supercapattery energy storage system seems to be suitable solution that fits with the discussed criteria. The research work at Nottingham into supercapatteries has been concentrated in designing and building of a stack using bipolar plates [11], as illustrated in Figure 1.3. In the following texts, SC stands for both supercapacitor and supercapattery.

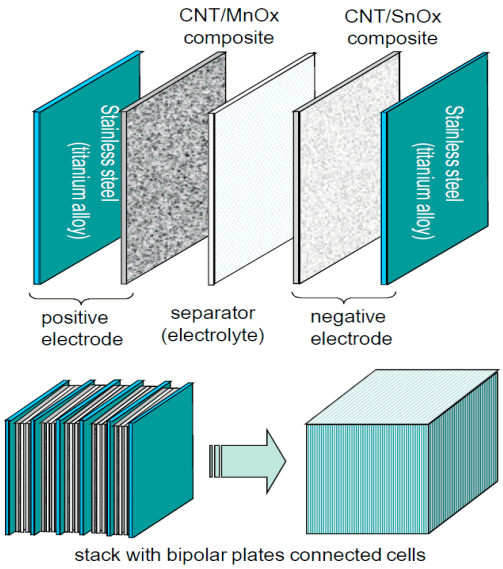


Figure 1.3 The high voltage stack assembly from individual supercapattery cells [17,18]

1.2 Problems Relating to Supercapacitors and New Chemical Energy Storage Devices

There are four main problems addressed in this thesis.

1. It is essential to understand SC electrical behavior and be able to derive their models before using them. These models help electrical engineers to improve our understanding about the devices. From the SC characterization standards BS EN 62391-1:2006 [22], the constant current charge-discharge is used to determine the simple RC model representing the SC characteristic. However, the simple RC model fails to represent SC characteristics in most applications, particularly during transient conditions [23,24]. Therefore, different characterization techniques and more complex models have been researched [25-35]. One of the most widely used techniques in electrochemical communities is electrochemical

impedance spectroscopy. In [28], the spectroscopy method and the series-parallel RC model is used in the SC characterization. However, special and expensive equipment is required to perform this technique, and the technique itself is limited to characterizing small capacity and low voltage SC stacks [30]. A pulse current method is used as an alternative method for the SC characterization since it is low-cost and simple. Previous research only applied the pulse current method for use with the single RC model [34]. This thesis develops the pulse current method for use with the more complex series-parallel RC model. This enables the faster dynamics and relaxation characteristic of the device to be taken into account. The results are compared with that of the electrochemical impedance spectroscopy.

2. A round-trip efficiency is an important parameter that is used to justify cost-effective investment of each energy storage technology [2,8]. For SCs, the efficiency has been investigated experimentally under current-control methods [34,36-40]. However, the SC state-of-charge depends on their terminal voltages, so the SCs in many applications are operated under power-control (i.e. to follow a power demand from the load) rather than current control. This is the case for HEVs, hybrid excavators, wind turbines, elevators, port rubber-tyred gantry cranes [41-48]. This thesis will address a new constant power cycling method for evaluating the round-trip efficiency which is felt to be more appropriate for SC cycling applications.

3. In a round-trip efficiency estimation, it is sufficient and accurate to use the simple RC model with the voltage-dependent capacitance [37,49]. However, in this research, it is found that the proposed estimation method is acceptable only when the SC is operated under room temperature and forced cooling. When the SC temperature changes due to energy loss, the efficiency is overestimated. The error may be due to the “out-of-date” resistance and capacitance used in the estimation algorithm when the operating temperature has changed since both parameters depend on the operating temperature [50,51]. Therefore, to make an investigation independent from the capacitance parameter, this research focuses on the energy loss estimation through updating resistance.

4. An unbalance cell voltage problem arises from the series-connected SC cells due to slight mismatches between the characteristic of each cell. These arise from manufacturing process [52]. An unbalanced cell voltage condition causes earlier degradation cell performance [53]. Thus, voltage equalizers are used to minimize cell voltage divergence. However, it is found that investigation of efficiency improvement as the equalizer complexity increases has not been sufficiently reported. This thesis investigates the design and operation of a single-switch fly-back voltage equalizer.

Another aspect of the thesis will be the emulation of SC at power up to 1kW. This emulation facility is very useful because:

- The system response employing an SC at a power level higher than the actual device can be evaluated.
- The problems related to limitation and safety regulation in university laboratories operating large electrochemical stacks require certification and increase protection equipment cost.
- The problems related to risk and material cost to prototype very large stacks of the supercapattery in-house during initial development phase are minimized.
- It speeds up testing to finalize the SC into the energy storage system since Hardware-in-loop (HIL) testing can be performed in order to verify the control design of a power electronic interface suitable for the newly developed energy storage device at a higher power level than the actual laboratory lab device can handle.

1.3 The Objectives of the Thesis

The objectives of this thesis are:

1. To develop a new approach to model the accurate dynamic SC characteristic based on a simple pulse testing method. Previous research has only applied pulse methods to derive simple models, which are insufficient for characterizing the dynamic performance of the SCs.

2. To develop a new approach for evaluating SC round-trip efficiency and energy loss, which are simpler and easier to implement. The proposed method is elegant since it requires only the charge-discharge duty cycle to calculate the efficiency.
3. To develop a new approach for estimating SC round-trip energy loss accurately. By updating the SC resistance change during the constant power cycling in the energy loss estimation, the errors can be reduced by <10%.
4. To analyze a design trade-off of a single-switch fly-back voltage equalizer. The converter design trade-off is between the equalizing time, the equalizing effectiveness and the total equalizing loss. Such a study has not been done before.
5. To implement an electronic emulator with a bi-directional half-bridge converter with interleaving connection of InterCell transformers [54,55] to replicate the supercapattery dynamic behavior. By using the emulator, issues relating to cost of implementation, university laboratory safety regulation and inconsistency behavior of the device are minimized. Hardware-in-loop (HIL) testing can be performed in order to verify the control design of a power electronic interface suitable for the newly developed energy storage device at a higher power level than the actual laboratory lab device can handle.

To meet the objectives, the PhD work was done in steps as shown in Figure 1.4.

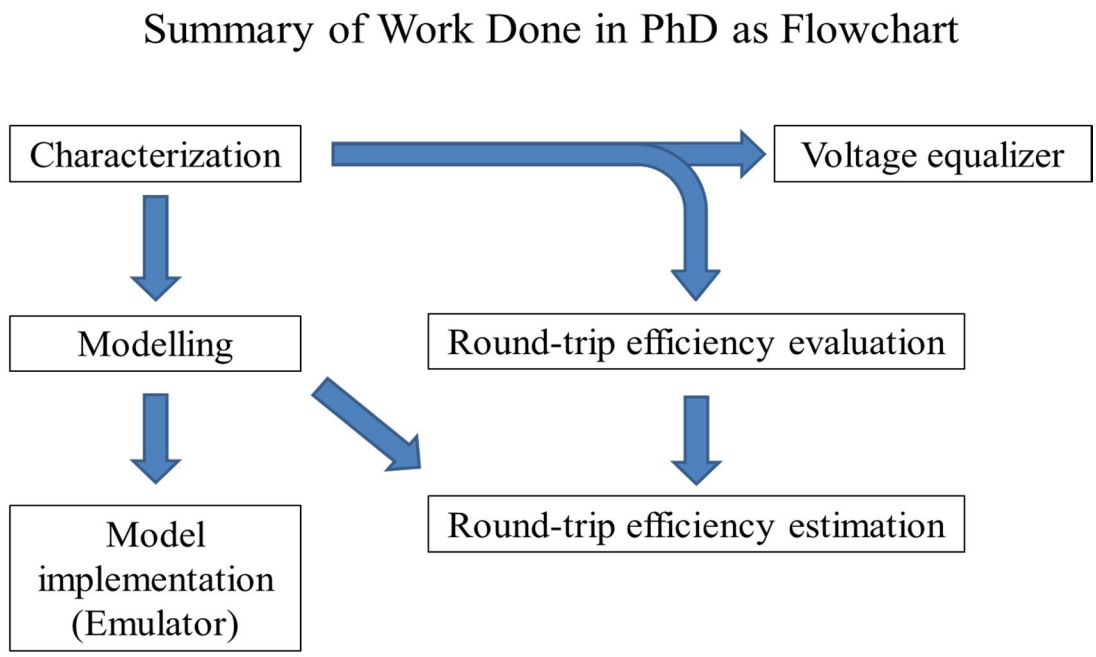


Figure 1.4 Summary of work done in PhD as flowchart

1.4 Methodology and the Thesis Layout

To describe the output research objectives, this thesis is organized into 7 chapters, and the outline of the thesis is:

Chapter 1. A brief description about characteristics and construction of the supercapattery is presented. Four main problems of SC and new electrochemical energy storage are specified, which leads to the objectives and scope of the thesis. The thesis layout is outlined.

In Chapter 2, SC characterization standards are described and discussed. In the standard method, the constant current method is applied with the simple RC model to characterize SCs. However, the simple RC model fails to represent SC characteristics in most applications, particularly during transient condition [23,24]. Additional limitations of the simple RC model in representing the SC characteristics under large operating temperature ranges, wide operating voltage ranges and long energy retention periods, are also described. A literature review of SC models and characterization methods is summarized. The characterization methods are grouped as methods to identify SC model parameters and to evaluate SC round-trip efficiency and energy loss. For the methods in the first group, there are four methods described: the electrochemical impedance spectroscopy, the non-standard current method, the pulse current method and the constant voltage method. The first three are used to characterize short-term SC characteristic while the constant voltage method is used to characterize the long-term SC characteristic. Among the first three methods, the impedance spectroscopy is the most widely used in electrochemical communities. Thus, this method is considered as a benchmark in this thesis. However, special and expensive equipment is required to perform this technique, and the technique itself is limited to characterizing small capacity and low voltage SC stacks [30]. The non-standard current and a pulse current methods are developed and used as alternative approaches due to their simplicity and low cost. The pulse current method used in this thesis is developed from the non-standard current method. Previous research only used the pulse current method with the simple RC model [34]. Therefore, the pulse current method with the series-parallel RC model is used and described in detail.

The methods in the second group are: the constant current cycling method and the constant power cycling method. The round-trip efficiency has been investigated experimentally under current-control methods [34,36-40]. However, the SC state-of-charges depend on their terminal voltages, so the SCs are usually operated under a power-control mode. Therefore, a new constant power cycling method of evaluating the round-trip efficiency is described. The method is felt to be more appropriate given the SC cycling applications. In addition, the method is elegant since it requires only the charge-discharge duty cycle to calculate the efficiency.

Additionally, in Chapter 2, the SC round-trip efficiency and energy loss estimation schemes are described. It is sufficient and accurate to use the simple RC model with the voltage-dependent capacitance [37,49]. However, in this research, it is found that the proposed estimation method is acceptable only when the SC is operated under room temperature and forced cooling. In this research a methodology is proposed that will give enhanced accuracy under wide temperature conditions. Three schemes are described, which are voltage-based, current-based and current-based with the FFT algorithm.

Chapter 3 gives descriptions of three experimental rigs used for the SC characterization. The description also includes the rig pros and cons and their possible operating modes. One of the rigs can also be used as an emulator system. The specifications of the device under test from their datasheets are included and compared. The characterization methods presented in Chapter 2 are combined as three characterizing processes. A process is an algorithm in which the methods are applied in order to gain better accuracy, correlation and consistency of results from different characterization methods. The processes identify model parameters representing the SC short-term and long-term characteristic and also evaluate the SC round-trip efficiency. In these processes, some useful characterization techniques taken from the SC characterization standards (in Chapter 2) are applied where appropriate to improve the result reproducibility.

Chapter 4 presents experimental results of the SC characterization. The results are divided and presented in three groups. These are results used for deriving model parameters for representing the SC short-term and long-term characteristics, and for evaluating round-trip efficiency and energy loss. The results used for deriving the

model representing the SC short-term characteristic are obtained from the pulse constant current (large-signal) and the electrochemical impedance spectroscopy (small-signal) methods. The derived models are evaluated and cross-evaluated between the two methods. The results used for deriving the model representing the SC long-term characteristic are obtained from a constant voltage method, but this model is not included in the final structure that is used in the emulator. To evaluate round-trip efficiency and energy loss, a constant power cycling method is used. The results are compared with those of the SC round-trip and energy loss estimation from the schemes presented in Chapter 2.

Chapter 5 explains problems related to unbalanced cell voltage of a series-connected SC stack. Several voltage equalizer topologies are summarized from literature and characterized as either dissipative or regenerative. The investigation on efficiency improvement as complexity of the equalizer current increases is undertaken. Specifically, the design and operation of a single-switch flyback voltage equalizer topology is investigated. In this chapter, two control modes are proposed: a constant switching frequency mode and a constant peak current control mode. The investigations of the equalization time, the effectiveness of equalization (i.e. maximum voltage deviation) and the total energy loss of both the equalizer and stack under the two different control modes are presented. The performance comparison against an active-dissipative voltage equalizer is also investigated.

Chapter 6 describes the electronic emulator concept. A literature review of battery and SC emulators is given. The emulator design requirements are (i) response speed of the emulator during transients, (ii) flexibility of implementing both model and controller and (iii) complexity of both the model and controller structures. These are also discussed. Previous research reported a bi-directional half-bridge converter with interleaved topology for a battery emulation [56]. The converter had a fast dynamic response current and a high equivalent switching frequency. However, one can reduce ripple current further than that of [56]. To do this, the converter requires a larger magnetic size or an increase in the number of channels keep. Alternatively, one may keep the number of channels low but use coupled inductors or InterCell transformers [54,55]. Therefore, in this thesis, a number of six-channel bi-directional half-bridge converters with interleaved connection of InterCell transformers are used

to achieve a high power level emulator with high dynamic response and accurate output current and voltage waveforms. Two control methods for this converter, the separated channel current control, and the total current control with compensation, are also included. The supercapattery emulator implementation and operation are described, and the model selection criterion and scalability are explained. The emulator experimental results are presented as two sections. First, the performance of the power electronic emulator is evaluated. Then the emulator with the supercapattery model is evaluated and compared with the actual device result under the same testing conditions.

Chapter 7 contains the conclusion of the thesis. This chapter summarizes the work and main outcomes of the PhD research work. It also provides possible future researches that can be developed further from the work presented in the thesis. A list of publications from the research is also given.

1.5 Summary of Achievements

- New method to model dynamic SC characteristic. This method uses simple pulse current, which can be considered as a non-destructive technique to characterize the SC. The result of this simple method is used to produce a detailed SC model, which is as accurate as the traditional electrochemical impedance spectroscopy method. The method can be applied to large-capacitance and high-voltage stacks (no stack size limitation) that may already be integrated within the system (i.e. no need to remove to conduct the test). This has resulted in publication [35].
- New method to evaluate SC round-trip efficiency. This method applies a constant power cycling through the SC, which is felt to be more appropriate given the SC cycling applications. The method is simple and easy to implement. The method is elegant since it requires only the charge-discharge duty cycle to calculate the efficiency, so any changes within the device characteristic during the test due to temperature and etc. can be detected online. This has resulted in publication [15,57].

- New approaches for estimating SC round-trip energy loss. Three schemes are described, which are voltage-based, current-based and current-based with the FFT algorithm. In the energy loss estimation, the last method uses an updated SC resistance value which changes during the constant power cycling. The errors are reduced to less than 10%.
- A design trade-off analysis of a single-switch fly-back voltage equalizer. The converter design trade-off is between the equalizing time, the equalizing effectiveness and the total equalizing loss. Such a study has not been done before. This has resulted in publication [58].
- The supercapattery emulator is implemented and tested at a constant power level of 1kW, which is scaled up from the actual device by ten times. Hardware-in-loop (HIL) testing can be performed in order to verify the control design of a power electronic interface suitable for the newly developed energy storage device at a higher power level than the actual laboratory lab device can handle. This has resulted in publication [59].

Chapter 2 Characterizing Methods and Modelling of Supercapacitors and Supercapatteries

2.1 Introduction

To design a supercapacitor (SC) energy storage system, the size of the energy storage devices must be determined together with the devices' power capability that is able to feed and to extract a specific amount of energy for a particular time and under reasonably high efficiency conditions. This specifies the maximum continuous current of the device. After the sizing design and the device and stack construction, it is desirable to gain as much information as possible about them in order to ensure their performance before integrating them into a system. At least, the device electrical and thermal characteristics including any related safety issues should be known since this information is required for designing the cooling and safety equipment.

If the devices are off-the-shelf products (i.e. Maxwell® Ultracapacitor), the rated voltage, rated continuous current, peak current with specified duration, and the leakage current are the main parameters usually provided by the manufacturer. If the devices are laboratory prototypes (i.e. supercapattery), this information is not generally available. It is noted, however, that information obtained either from datasheets or from the producers of laboratory prototypes can only be used as a guideline since the exact characteristics depend on the specific operating condition of each application. In addition, among the devices themselves, there are variations

due to imperfect manufacturing processes and storage conditions. For these reasons, to have all the device information, device characterization is beneficial or necessary. In addition, the characterization process is important not for integrating the devices into a system, but to monitor the devices' condition.

A goal of characterization is to obtain a model that can represent the electrical performance closest to the devices' behavior for all operating conditions. However, such a model would be complicated and the characterization process is intensive and time consuming. Therefore, a simple series RC equivalent circuit is usually first employed to represent SC characteristics. The model consists of an equivalent series resistance, *ESR*, and an ideal capacitance, *C*. This model can represent SC characteristics at an acceptable level, so it can be used for a control plant design of a DC-DC converter interfacing a SC stack. To determine the simple RC model parameters, a constant current charge-discharge method is used. The method is described in published SC characterization standards [22,60-63] and manufacturing application notes [64-67], which will be presented and discussed in Section 2.2.

However, it will be shown later that the simple RC model fails to represent SC characteristics in most applications. This is due to the device characteristics and their parameters, which are affected by frequency, applied DC-bias voltage and temperature [51]. The limitation of the series RC model will be discussed in Section 2.3. Therefore, it is necessary to develop improved models that can better represent the behavior. The SC models and the methods to determine them will be discussed in Section 2.4 and 2.5, respectively. In this thesis, a pulse constant current method and an electrochemical impedance spectroscopy method are used. The model itself will be derived from a series-parallel connected RC circuit. Note that in addition to supercapacitors (SCs), the supercapattery (SCP) device will also be modeled and characterized since the operation principles are the same. In the following texts, SC stands for supercapacitors or supercapatteries.

The SC self-discharging characteristic is an important aspect affecting model parameter identification. The factors that affect SC self-discharging characteristic are investigated and discussed in [68]. In this thesis, the SC self-discharging characteristic is monitored and recorded but is not included in the final equivalent

model. This is due to the lack of proper equipment to control temperature and to do long-period data-logging.

The SC efficiency is another interesting topic for both research and industrial communities [36,38-40,57]. Since SCs are bi-directional power-flow energy storage devices, the round-trip efficiency is used as a measure of the total operating system efficiency. The round-trip efficiency is calculated from the amount of discharging energy per charging energy over a single charge-discharge cycling period where the initial and the final voltage of the SC stack are equal. If the round-trip efficiency of the technology is low, thus overall efficiency (i.e. energy storage devices + interface converters) is further reduced. Thus, it is interesting to determine the round-trip efficiency of SCs at different operating voltage and power levels giving a clear picture of the technology capabilities of the device and how to exploit them. A method used to determine round-trip efficiency of SCs is discussed in Section 2.6. The estimation method of round-trip efficiency is also developed step-by-step and is presented in Section 2.6.

The problem of the round-trip efficiency estimation in real life is that the results can be ambiguous and inaccurate since parameters will change due to SC regenerative [69,70] and temperature-dependent phenomena [51]. Indeed, it is important to identify when the SC approaches its end of life. The development of an online tool to monitor efficiency and to predict changes in performance is desired [37,71]. This can give a projection of the trade-off boundary between round-trip efficiency and service life of a SC stack. However, SC aging process is out of scope of this thesis.

2.2 Supercapacitor Characterization Standards and Testing Procedures

In this section, published SC characterization standards (IEC62391:2006 [22,60] and IEC62576:2010 [61]), testing manuals [62,63], and manufacturing application notes [64-67] are discussed and compared. To determine *ESR* and *C*, a constant current charge-discharge method (CC) presented in [22,60,61,64-67] is used.

The CC consists of a charging period, a voltage holding period, and a discharging period, as depicted in Figure 2.1. In each testing step, the following tasks are performed,

- Charging period: the cell is charged with a constant current of I_{ch} until the cell voltage reaches a cell rated voltage, V_{rated}.
- Voltage holding period: the cell voltage is maintained as a constant either, at equal or slightly below V_{rated} for fixed period of time.
- Discharging period: the cell is discharged with a constant current of I_{disch} until the cell voltage reaches minimum or within a safety level.

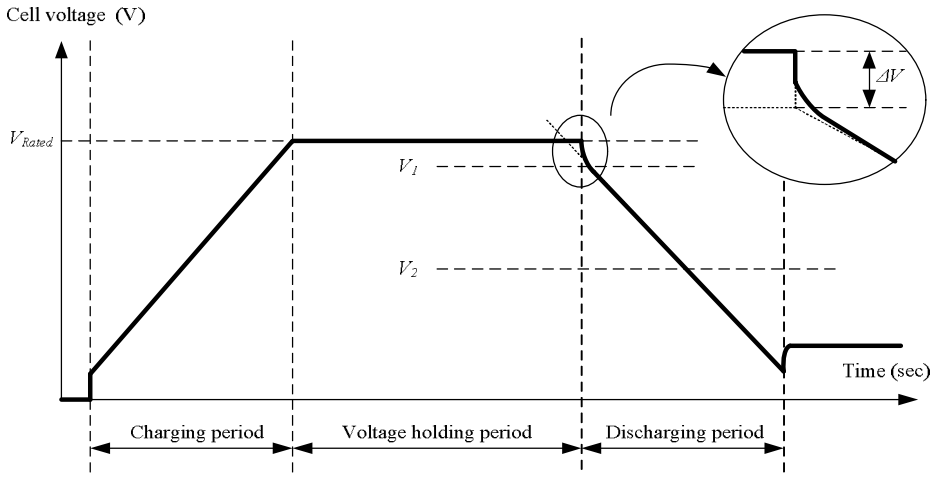


Figure 2.1 Voltage-time characteristics of the constant current charge-discharge method used for determining *ESR* and *C* in IEC62391 and some manufacturers application notes

All voltage, current and time information is recorded for all steps, so *C* is calculated as:

$$C = \frac{I_{disch}(t_2 - t_1)}{V_1 - V_2} \tag{2.1}$$

where I_{disch} is the constant discharge current, V_1 and V_2 are two pre-defined voltage levels, and t_1 and t_2 are times at two measured voltage levels.

Meanwhile, the *ESR* is determined by:

$$ESR = \frac{\Delta V}{I_{disch}} \tag{2.2}$$

where ΔV is a step voltage at the beginning of the discharging period.

Considering all standards [22,60,61,64-67] and testing manuals [62,63], the procedures are designed according to the way the SCs are used, so many testing parameters such as operating voltage range, working temperature, charge-discharge periods and etc. , are defined differently. Therefore, the testing standards can be used only as a guideline on studying characteristic of SCs since there are many limitations of RC model which will be summarized in the next section. The detail difference between the standards and the testing manuals is presented in Appendix A.

Some of techniques and procedures presented in many SC testing standards are very useful since they can improve consistency of the experimental results. They have been adopted into our characterization procedure presented in Section 3.5. These techniques can be summarized as below:

- Technique 1: During the device pre-conditioning period, the device is short circuit for between 1 to 24 hours [22], depending on the DUT capacity, to ensure the stability of chemical compounds inside the testing cell (i.e. completely discharged condition). This is important particularly for an energy-dense energy storage type, which requires longer pre-conditioning time than a power-dense type.
- Technique 2: The amount of an applied current during charging/discharging during the pre-conditioning period is dependent on the SC size (defined as Amp per Farad·Volt) [22] and should be limited to a proper level. Applying the very high charging current (i.e. full rated current) can cause the cell temperature to increase which, in turn, changes the cell characteristics from its steady-state condition. In this study, the charging current rate of 75mA/F [65] or lower [22] is used before starting the EIS method and the PCC method, so the temperature change due to the pre-conditioning process is minimized.
- Technique 3: The voltage holding period should be 1 hour or more by using the CV method before commencing the EIS and the PCC methods. For self-discharging, the holding period is 8 hours [22]. This is very important for the energy-dense energy storage type since they require longer time than the power-dense type to stabilize the cell (i.e. to distribute all charges within the cell).

- Technique 4: The IR voltage drop due to *ESR* subjected to the high applied constant current is observed from the SC voltage response either within 10ms or 20ms duration [32] after the moment when a discharge current is applied. If applicable, the measurement tool should be able to record 5mV resolution and 100ms sampling intervals or less [61].

2.3 Limitation of the Simple RC Equivalent Model

In the previous section, several SC testing standards are presented. All of them employ the simple RC equivalent model to represent SCs' behaviour. However, the SCs' internal chemistry is not simple and this is affected by operating conditions:

- operating time period (e.g. transient or steady-state condition)
- operating voltage range
- energy retention period (i.e. self-discharging)
- operating temperature

If SCs are employed mainly in steady-state applications where the voltage characteristic during the transient period is not important, the series RC equivalent circuit can be used. Unlike normal electrolytic or film capacitors, the SCs have multiple time constants (like a RC transmission-line), so the single RC model cannot be used during transient periods. This effect is due to the porous activated carbon electrode of SCs, which is explained by porous theory in [23,24] as presented in Figure 2.2.

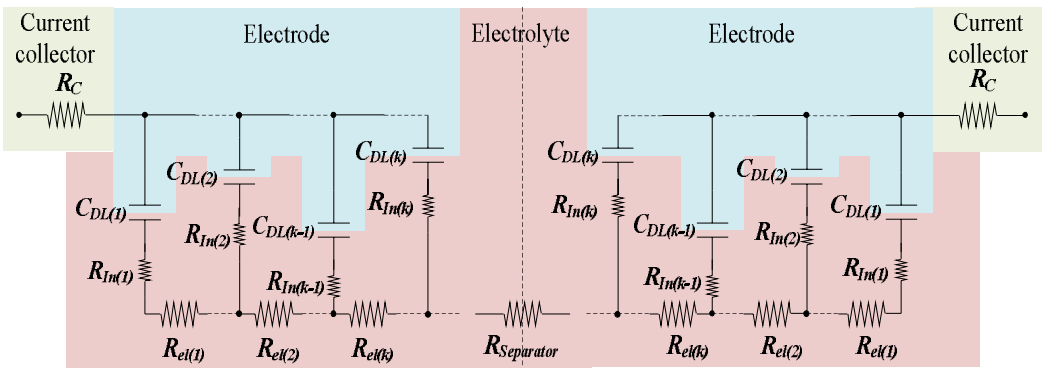


Figure 2.2 Porous model electrode of SCs (reprinted from [24], Figure 3)

Where R_C is a current collector resistance, R_{In} is an interface resistance (from the rough aspect of the electrode/electrolyte interface), R_{el} is an electrolyte resistance (deduced from the electrolyte conductivity), $R_{Separator}$ is a separator resistance, and C_{DL} is double layer capacitance (induced by the electrical potential at the electrode/electrolyte interface).

The operating voltage of SCs also affects the performance [51]. As will be shown later, the *ESR* and *C* parameters of the RC model are nonlinear voltage-dependent. Therefore, there will be a discrepancy in the stack voltage between the experimental result and the simulation, which uses a RC model obtained from a single DC bias voltage condition. The best practice is to limit the operating voltage in the experiment and use the *ESR* and *C* determined at the average of the experimental operating voltage in the simulation.

The single RC model may also fail in applications, which are required to hold energy in the stacks for long time (i.e. long energy retention period) [31,68,72,73]. This is due to self-discharging of SCs, where their terminal voltage gradually decreases during an open-circuit condition. The amount of leakage energy is defined by its leakage current, I_{Leak}, which can be represented by adding an equivalent parallel resistor, *EPR*, connected in parallel with *C* in the simple RC model. A method used to characterize self-discharging and the leakage current is the constant voltage test, which will be presented in Section 2.5.1.5.

From [50,51], the operating temperature also has an effect on performance and model parameters (i.e. both *ESR* and *C*). This can be explained by the effect of temperature on the electrolyte conductivity [50]. Thermal models are studied in [74-77] for a single cell and as a module, but they are out of scope of this thesis.

To account for all factors that affect SC device, more complex models are proposed in the literature, which will be presented next. Additionally, to obtain model parameters for the complex equivalent models and to fully understand the SC characteristic, more complicated characterizing methods are also employed in this study. These will be presented in Section 2.5.

2.4 Supercapacitor Equivalent model Literature Review

There are several SC equivalent models proposed in literature, which are the adaptive series RC model [34], the transmission-line RC model [29,39,78], the parallel RC branch model [32,33], the series-parallel RC model [28,31,35], the combined model between series-parallel and parallel-branch RC models [79] and the nonlinear model [24,80].

2.4.1 Model I: The Adaptive Series-connected RC Model

Since SCs have a voltage-dependent characteristic, an adaptive series-connected RC model is usually applied. This equivalent model is the same as the simple RC model but the R and C parameters in this model are varied with an applied DC-bias voltage [34] as presented in Figure 2.3. This equivalent model represents the steady state condition better than the single RC.

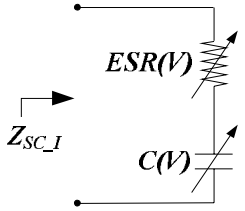


Figure 2.3 Model I: An adaptive series-connected RC model

However, since this model does not have multiple RC networks (i.e. more RC orders), it cannot explain the SC transmission-line characteristic as mentioned in the previous section (Figure 2.2).

2.4.2 Model II: The Transmission-line RC Model

To represent the SC transmission-line characteristic, a transmission-line RC model (so called 'ladder' model in [29]) is employed and is presented in Figure 2.4. Each component pair (i.e. R_iC_i) represents a different time constant, and when combined will yield a transmission-line effect that occurs in the real term of the SC characteristic. By increasing the model order, N, the model can address the charge re-distribution phenomenon between an interface of SCs porous electrodes and their

electrolyte. In order not to increase N too much, an automatic order reduction and selection method is developed in [78].

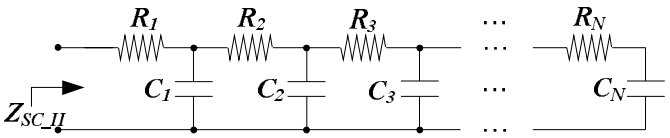


Figure 2.4 Model II: The N transmission-line RC model

2.4.3 Model III: The Parallel RC Branch Model

In [32,33], a similar modeling is proposed using a parallel set of series RC configuration (so called 'branch') presented in Figure 2.5. A model order of 3 is recommended in [32], and these 3 RC branches are called intermediate R_iC_i, delay R_dC_d and long-term R_lC_l. They are presented in Figure 2.6 (a). Each branch represents a time constant corresponding to their names. Thus, the order is minimized while preserving its accuracy at a reasonable trade-off. The main difference between the models of [29] and [32] is the way they represent the voltage-dependent characteristics. In [32], this is represented by modifying C_i with voltage-dependent differential characteristic as presented in Figure 2.6 (b) and calculated by

$$C_i = C_0 + C_V V_{C0} \tag{2.3}$$

Where C_0 is an initial capacitance, C_V is a voltage-dependent capacitor (express in F/V), and V_{C0} is a voltage across C_0. Meanwhile, in [29], the voltage-dependent effect is observed and is considered in all the model parameters, but they are too complicated to be implemented into the modeling algorithm, particularly when the model order increases.

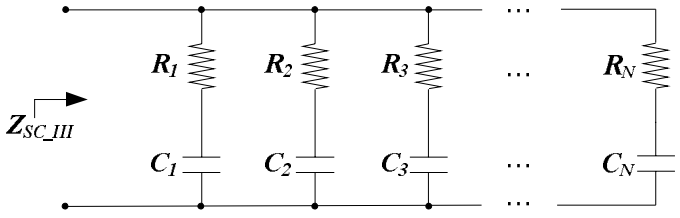


Figure 2.5 Model III: The N parallel RC branch model

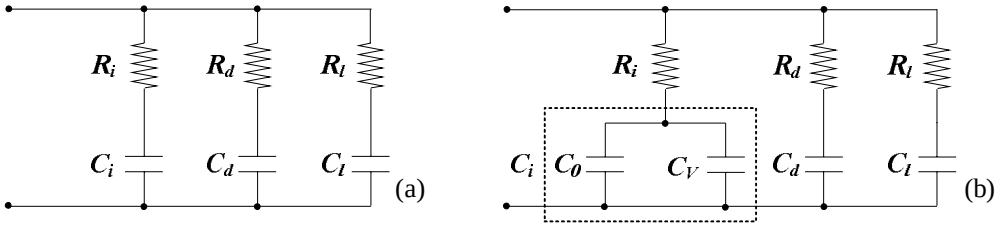


Figure 2.6 Three-branch parallel RC model consisting of an immediate, a delay and a long-term branches (a) normal structure (b) with expanded immediate branch

2.4.4 Model IV: The Series-parallel RC Model

Alternatively, to explain the porosity of SC electrodes and to relate SC models with their physical electrode structures, a complex pore impedance, Z_{Pore}, with an added inductance has been introduced in [28,31,81]. The equivalent model is presented in Figure 2.7 and the SC impedance, Z_{SC}, is then described by (2.4).

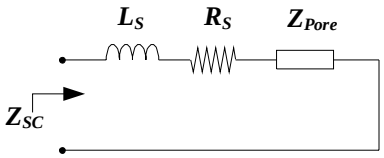


Figure 2.7 The SC model with a complex pore impedance and an added inductance

$$Z_{SC}(j\omega) = R_S + j\omega L_S + Z_{Pore}(j\omega) \tag{2.4}$$

where ω is a frequency (rad/s), R_S is the series resistance, L_S is the equivalent series inductance or a stray inductance that may come with the device leads, and Z_{Pore} is the complex impedance that models the porosity of the SC electrodes given by:

$$Z_{Pore}(j\omega) = \frac{\tau \coth(\sqrt{j\omega\tau})}{C_S\sqrt{j\omega\tau}} \tag{2.5}$$

From (2.5), the Z_{Pore} can be described by 2 parameters, C_S and τ only. In [28], the Z_{Pore} can be substituted by a series-parallel RC structure as presented in Figure 2.8 and this model is called the series-parallel RC model,

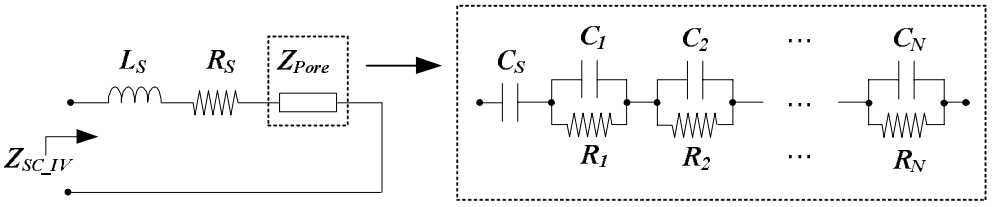


Figure 2.8 Model IV: The *N* series-parallel RC model with an added inductance

where

$$C_1 = C_2 = C_N = \frac{C_S}{2} \tag{2.6}$$

$$R_N = \frac{2\tau}{\pi^2 N^2 C_S} \tag{2.7}$$

This model utilizes series-parallel RC components to represent voltage due to charge re-distribution within the pores of the SC electrodes. The model presented of Figure 2.8 is convenient for simulation and control design purposes. The R_S and C_S in model IV can be considered as equivalent to the immediate branch of model III since in the high frequency range, C_1 to C_N of model IV become short-circuit. In addition, the voltage-dependent and temperature-dependent characteristics are accounted for by the τ parameter [28], which impacts directly on the parameters R_N, C_S and C_N, as described in (2.5)-(2.7).

In [35], model IV is also proposed. However, the concept of defining RC parameters is not based on a complex pore impedance, rather it is similar to model III approach, and will be detailed in Section 2.5.1.3.

The impedance model II, III and IV utilize RC components to describe the SC characteristic, so it is possible for each model to convert from one to another. In [82], a conversion among the three equivalent models is presented up to the 3rd order. As the model order increases, the conversion becomes difficult and complicated.

2.4.5 Model V: The Combined Model between Series-parallel and Parallel-branch RC Model

In [79], a combination of the parallel RC branch model III and the series-parallel RC model IV is proposed. This becomes the impedance model V, and is shown in Figure 2.9. The inductance L_S is neglected. This model can describe the SC characteristic over a large range of frequency since it uses model IV to describe the transient response characteristic and model III to describe the long relaxation period characteristic. The order is a summation of a number of series parallel branches, N_S, and a number of series parallel branches, N_P. However, as will be shown in next,

model V is actually redundant compared to model IV. This is because model IV can represent both the transient and the relaxation periods of the SC characteristic if a proper defined time frame is applied in a curve-fitting algorithm [79].

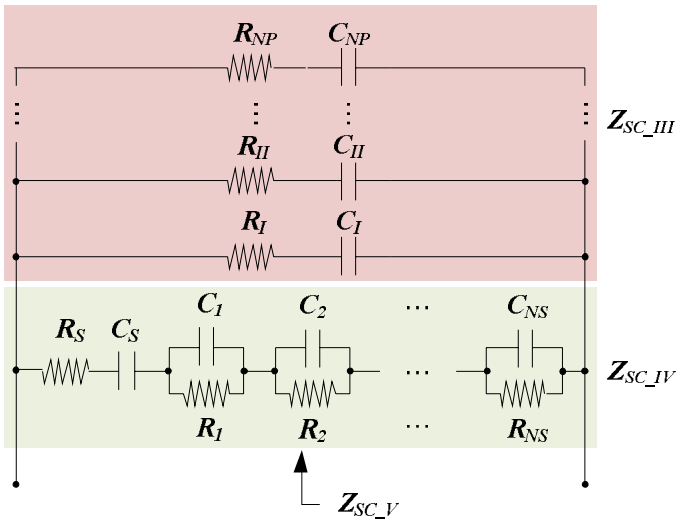


Figure 2.9 Model V: The combination of model III and model IV with $(N_S+N_P)^{th}$ order

2.4.6 Model VI: The Nonlinear Model

Another type of model used to represent SC characteristics is the fraction nonlinear model, here called model VI [24,80]. This equivalent model is not based on electrical components but employs a nonlinear equation to describe the voltage-dependent characteristics. The nonlinear equations presented in [24,80] are suitable for implementation in an embedded digital platform such as microcontrollers and DSPs. However, this model mainly is used for aging monitoring and failure diagnosis purpose and not for describing and reproducing dynamic behavior of SCs [24,80]. Therefore, this model is not used in our emulator application where SC dynamic behavior is intended to be replicated.

For model II to V, the self-discharging characteristic also can be included by connecting the *EPR* in parallel with the Z_{SC} as discussed. However, self-discharging also depends on the applied DC-bias voltage, the SC stack temperature and the charging duration of an applied constant voltage source. Therefore, it cannot be represented only with the fixed *EPR* parameter [31,73,83]. To investigate the self-discharging characteristic and to understand the variation of the *EPR* parameter fully, a climate chamber and long observation times (more than 1 year) are required for

controlling the testing temperature and letting device to reach its steady-state. This is done in [83].

In this thesis, the SC self-discharging characteristic is monitored and recorded but it is not included in the model due to the lack of proper equipment. The chosen equivalent model for the emulator approach should:

- represent the voltage dependent characteristic (all presented models are applicable)
- ready to be implemented in a digital platform as will be shown in Chapter 6 that not all the equivalent models can be implemented on a digital platform.
- be expandable to account for the series and parallel of cells.

In the next section, the methods used to characterize SCs and to obtain the models presented in this section will be discussed.

2.5 SC Characterization Methods

In this section, the SC characterization methods are described according to the characterizing objectives. The first objective is to identify model parameters representing SC short-term and long-term characteristics presented in Section 2.5.1, and the second objective is to evaluate SC round-trip efficiency presented in Section 2.5.2.

2.5.1 Characterization Methods for Extracting SC Model Parameters

In this section, four methods used to identify SC parameters are described. These are (a) the electrochemical impedance spectroscopy method (EIS), (b) the non-standard constant current method (Non-standard CC), (c) the pulse constant current method (PCC) and (d) the constant voltage method (CV). The first three methods are used to characterize short-term SC characteristic while the CV is used to characterize the long-term SC characteristic. The long-term SC characteristic is also an interesting topic, but it is not the main focus of this study. Therefore, the CV

method is included here just to complete the SC characterization, and the detail is described in Section 2.5.1.5.

In general, the EIS method is viewed as a frequency-domain approach while the Non-standard CC and the PCC methods are viewed as time-domain approaches. Additionally, small-signal disturbances are applied to the EIS method, whilst large-signal disturbances are applied to the non-standard CC method and the PCC method. Each method can be used interchangeably to verify the model parameters obtained by other methods.

2.5.1.1 Electrochemical Impedance Spectroscopy Method

The EIS method is broadly used in the electrochemical research community to characterize electrochemical energy storage devices, which can be fuel cells, batteries and SCs [25-27]. Additionally, this method explores the characteristic of the device under test (DUT) by applying a small sinusoidal signal disturbance with different frequencies. The output response at the device terminals is measured in both amplitude and phase shift information relative to the disturbance, which leads to finding a complex impedance as a function of frequency, $Z_{SC}(j\omega)$, at the particular frequency, ω, of the disturbance. If the applied frequency is swapped within a frequency range of interest (i.e. from 10mHz to 100Hz and from 100Hz to 10kHz), a full-range frequency dependent complex impedance is found. The operating mode of the EIS machine can be either voltage control (so called potentio electrochemical impedance spectroscopy (PEIS) in [84]) or current control (so called galvano electrochemical impedance spectroscopy (GEIS) in [84]). Since our DUT is a capacitive type, PEIS is used and the $Z_{SC}(j\omega)$ is calculated by (2.8) where $V_{applied}(j\omega)$ is the applied voltage signal and $I_{response}(j\omega)$ is the current response.

$$Z_{SC}(j\omega) = \frac{V_{applied}(j\omega)}{I_{response}(j\omega)} \tag{2.8}$$

However, electrochemical energy storage devices often have non-linear characteristics [85], so (2.8) is invalid for a nonlinear system. To minimize this nonlinearity effect, a small amplitude of $V_{applied}(j\omega)$ signal is usually used [86]. The amplitude of 10mV is recommended [85] because it is considered as a good trade-off

between measurement accuracy of the $I_{response}(j\omega)$ signal and the nonlinearity problem. This value will be used in our experiment.

In addition, when applying a sinusoidal waveform of $V_{applied}(j\omega)$ signal to SC devices, the $I_{response}(j\omega)$ signal is also a periodic but non-sinusoidal. Thus, in modern EIS equipment, Fast Fourier Transform (FFT) analysis is employed in decomposing the periodic signal of both the voltage and the current. Only the fundament information of both voltage and current signals are used in the calculation of $Z_{SC}(j\omega)$ for the particular ω value. The $Z_{SC}(j\omega)$ information is usually presented as a Nyquist plot presented as real/imaginary parts versus frequency [35].

Only model II, IV and VI are proposed for use with the EIS methods [28-31]. In this thesis, model IV is employed with the EIS method, however, there is a modification of the model parameter fitting process to the actual $Z_{SC}(j\omega)$. From [35], a goodness of fit can be improved with an additional RC branch, R_{add} and C_{add}. These R_{add} and C_{add} parameters are independent from those R and C parameters calculated by (2.6) and (2.7), and their roles are for fitting low frequency range of the Z_{SC} information. The time constant of $R_{add}C_{add}$ is much larger than those of Z_{Pore}. Thus, the Z_{SC_IV} becomes the $Z_{SC\_IV\_2}$ as presented in Figure 2.10.

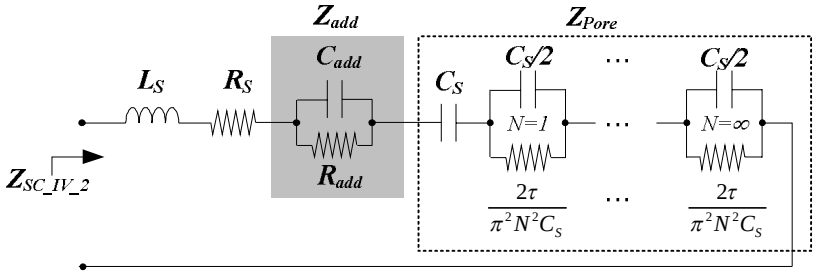


Figure 2.10 Model IV_2: The *N* series-parallel RC model with an additional RC branch

The model parameter fitting algorithm used in this thesis is the Gauss-Newton method [32]. The Gauss-Newton is a well-known method that is used to find the minimum of the sum of squares of any vector. In parameter identification, the vector is $Error(j\omega)$ between the model impedance model, Z_{SC_est}, and the actual impedance, Z_{SC}. The process to do curve fitting as presented in Figure 2.11 where the Z_{SC_est} impedance model in this case is the $Z_{SC\_IV\_2}$ model. The results of fitting will be presented in Chapter 4. For full detail description of the Gauss-Newton method, see Appendix D.

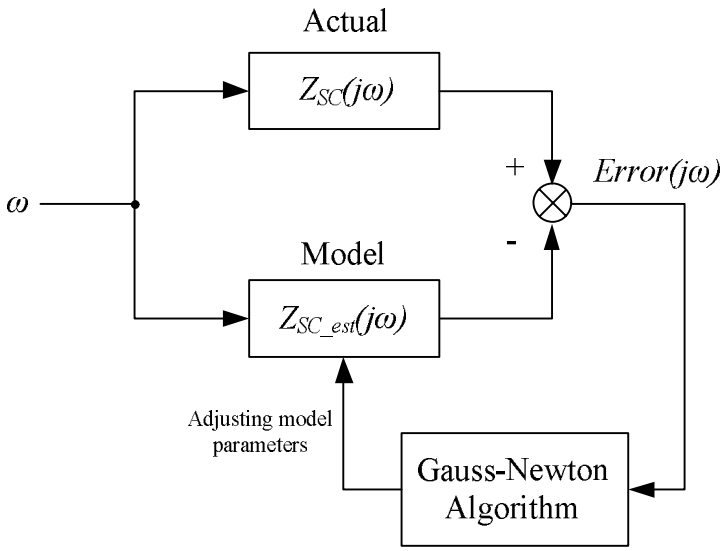


Figure 2.11 Curve fitting process with Gauss-Newton method

The parameter identification process consists of:

- STEP1: searching for the point C and its corresponding frequency, where the SC impedance curve intersects with the real axis (Imaginary(Z_{SC}) = 0) as shown in Figure 2.12. This frequency point represents the resistance R_S of model IV.
- STEP2: use the positive imaginary impedance information to calculate the average value of L_S of model IV.
- STEP3: apply the Gauss-Newton algorithm to the negative imaginary impedance information and determine C_S and τ with the least square error method.
- STEP4: use C_S and τ to derive C_N and R_N parameters inside the Z_{Pore} according to (2.6) and (2.7).
- STEP5: select R_{add} and C_{add} to minimize the error between the experimentally determined response and the model impedance at the low frequency range (i.e. $\omega \rightarrow 0$).
- STEP6: re-do STEP3 to STEP5 if the discrepancy between the model impedance and the real SC impedance is too high/and stop when error becomes stable.

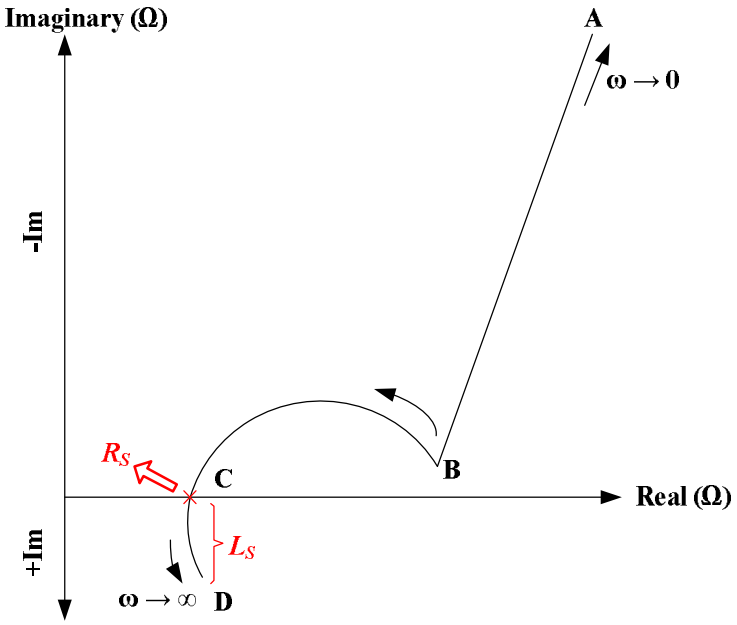


Figure 2.12 The typical Nyquist plot of the SC impedance

2.5.1.2 Non-standard Constant Current Methods

Several standard CC methods are presented and discussed in Section 2.2. In this section, non-standard CC methods used in literatures [32,33] are explained. The parameter identification process of the non-standard CC method is similar to the standard CC method. However, in the non-standard CC method, the SC voltage-time information during the relaxation period (i.e. the period after removing an applied current) is also included in the identification process. This relaxation period information is used to analyse extra RC network in additional to the single RC model.

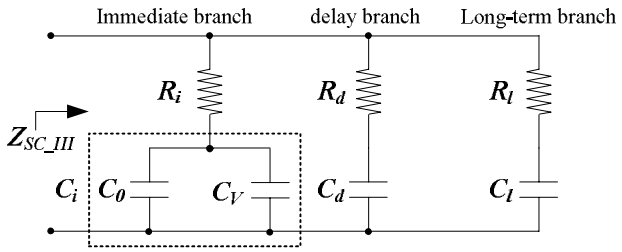


Figure 2.13 Three-branch parallel RC model consisting of an immediate branch, a delay branch and a long-term branch with expanded immediate branch

In [32,33], the Z_{SC_III} impedance structure is employed and is presented again as Figure 2.13. Both methods used in [32,33], derive the immediate branch parameters (i.e. R_i, C_0 and C_V) during the charging period only. The R_i is derived from the IR voltage drop at the moment that the charging is applied. The C_0 is derived from a

50mV increment voltage from the IR voltage drop. Meanwhile, the C_V is derived from two voltage points during the charging period based on the assumption that the capacitance is varied linearly with the bias voltage as (2.3) and all of the charging goes to the immediate branch only. After removing the charging current, the relaxation voltage-time information is used for deriving the delay and long-term RC parallel braches for time constants of >100s.

Since the DUT is charged to the DUT rated voltage with the rated constant current from a completely discharged condition, the charging period falls within a range from less than a second to 100's of seconds depending on the DUT capacity. This charging period may exceed the time constant of the immediate RC branch, so the assumption that there is no charge going to the delay and the long-term branches becomes invalid. Additionally, the immediate branch RC parameters derived from this charging duration cannot accurately reproduce the DUT voltage response faster than the derived time constant. This is the limitation of this technique. Therefore, the PCC method is employed to solve the non-standard CC drawbacks, which will be described in the next section.

2.5.1.3 Pulse Constant Current Method

In [34,35], the PCC method is used to characterize SC behaviors. In the PCC procedure, the constant current is applied in a pulse pattern. The amplitude and time duration of the applied pulse constant current can be defined differently depending on time constants used in applications and selected SC models. The pulse current pattern can be used to investigate the SC voltage-dependent capacitance and voltage-dependent resistance characteristics.

In [34], the pulse-train constant current is used together with the adaptive series-connected RC model (model I), and it is clear that the observed resistance and capacitance are changed with the applied DC-bias voltage in both charging and discharging periods. However, as discussed in Section 2.3 and 2.4, there is the transmission-line effect in SCs, so the complex RC models (presented in Section 2.4) are employed together with the technique presented in the author's paper [35].

2.5.1.4 The Proposed Pulse Constant Current Method

In [35], the PCC with a long rest time is applied to the SC. The recorded voltage-time information from the experiment is used to derive the parameters of the impedance model IV. However, the parameters used in this model IV does not derive from the complex impedance pore concept as mentioned in Section 2.4. Therefore, there is a modification in model IV as shown in Figure 2.14 and it is named $Z_{SC\_IV\_3}$, where: R_S and C_S are series resistance and series capacitance, and R_1&C_1, …, R_N&C_N are parallel RC connected pairs. In addition, in the PCC method, the pulse current is considered as ideal. L_S is excluded from the model.

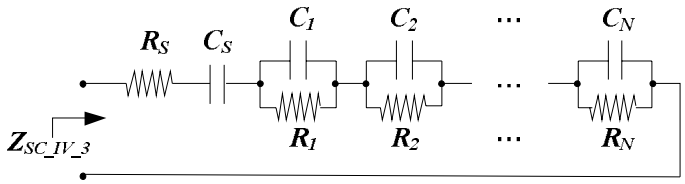


Figure 2.14 Model IV_3: The N series-parallel RC model without L_S

When applying a negative constant current pulse, I_P, for a short time, T_P, it will discharge the SC. If the $Z_{SC\_IV\_3}$ model is used (Figure 2.14) and steady-state initial and final conditions, V_i and V_f, are assumed (i.e. all paralleled R&C pairs are considered discharged), all the energy lost during the pulse is taken only from C_S. At the moment the current pulse stops, the SC's terminal voltage, v_{SC}, shows an instantaneous step change equal to the voltage drop across R_S (i.e. $I_P R_S$ voltage drop) as depicted in Figure 2.15. After reaching steady state again, the C_S voltage should accurately describe the amount of charge lost during the current pulse. The v_{SC}, after removing I_P, starts to decline as the cell finishes its relaxation process (i.e. changing to self-discharging mode). These two situations reveal directly the size of R_S and C_S. Note that in practice, since R_S is also voltage-dependent, the voltage drop across R_S when the pulse is applied may be unequal to the voltage drop after removing the pulse. Therefore, R_S is calculated from an average of the two conditions. An average of V_i and V_f is also calculated and used to establish the $R_S(V_{bias})$ and the $C_S(V_{bias})$ relationships.

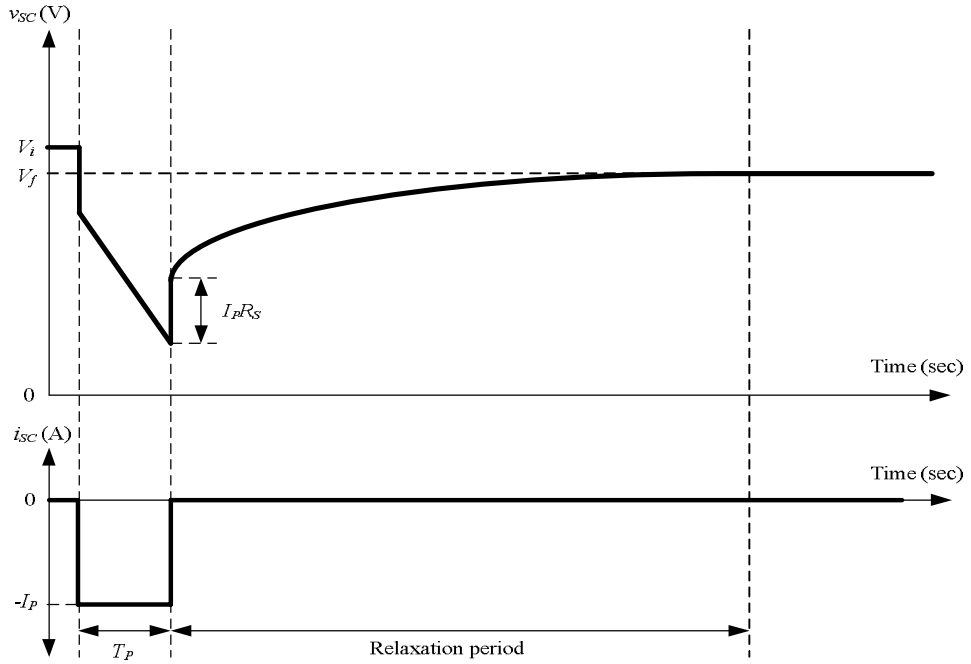


Figure 2.15 A SC voltage under a negative pulse constant current

The equivalent impedance of Figure 2.14, which is also the $V_{SC}(s)$ to $I_{SC}(s)$ transfer function of the equivalent circuit, is shown in Figure 2.15, and is derived as:

$$Z_{SC\_IV\_3}(s) = R_S + \frac{1}{sC_S} + \sum_{k=1}^{N} \frac{R_k}{(sR_kC_k)+1} \tag{2.9}$$

The disturbance is a current pulse, which can be modeled in the s-domain as:

$$I_{SC}(s) = \frac{1-e^{-T_P s}}{s} I_P \tag{2.10}$$

Multiplying (2.9) with (2.10) yields the voltage response of the model in the s-domain. Performing an inverse Laplace transform to obtain the voltage response in the time-domain and considering the voltage response only after removing the pulse, which results in:

$$v_{SC}(t) = \sum_{k=1}^{N} \left(-X_k e^{-Y_k t}\right) + \frac{I_P}{C_S} T_P + V_i \tag{2.11}$$

where

$$X_k = \left(1-e^{-Y_k T_P}\right) R_k I_P;\ Y_k = \frac{1}{R_k C_k}$$

The voltage response information after removing the pulse current (i.e. during relaxation period) can be fitted by using a sum of exponential terms via a curve fitting tool as there will be a direct and simple solution for mapping each term in (2.11) with the X_k and Y_k. Before starting the curve fitting, the range of X_k and Y_k must be defined. In [79], it is recommended to select the exponential time constant sufficiently different from each other, so during the transient condition of each RC pair, the other RC pairs can be considered to be in steady state. In [79], the time intervals are suggested to be set equidistant on a logarithmic scale, so the range of Y_k terms are defined as:

Range k=1: $\frac{1}{\tau_0} < Y_1 < \frac{1}{M_P \tau_0} = \frac{1}{\tau_1}$

Range k=2: $\frac{1}{\tau_1} < Y_2 < \frac{1}{M_P \tau_1} = \frac{1}{\tau_2}$

… … … … …

Range k=*N*: $\frac{1}{\tau_{N-1}} < Y_N < \frac{1}{M_P \tau_{N-1}} = \frac{1}{\tau_N}$

where M_P is a time multiplying factor and $\tau_0,\ldots, \tau_N$ are time constants of each range. The upper limits of the lower ranges are set equal to the lower limit of the next upper range. In addition, M_P is the parameter that distinguishes exponential time constants since it makes fitting process of each adjacent time constant become effective and independent from each other. From [79], transients can be considered extinguished after five times the time constant, because 99.3% of the steady state value is reached at this time. Therefore, to guarantee that each transient seen by each RC pair is finished before the beginning of the next one, M_P is chosen to be more than 5.

However, for the X_k terms, there is no well-defined rule like the Y_k terms. Considering from (2.11), since the X_k terms are actually the coefficients of the exponential terms, they control the effectiveness of each time constant on the relaxation voltage curve. In addition, since the SC voltage relaxation after removing discharged pulse current is used, the range of the X_k term in this thesis are defined as:

Range $k = 1$: $-L_1 < X_1 < 0$

Range $k = 2$: $-L_2 < X_2 < 0$

… … … …

Range $k = N$: $-L_N < X_N < 0$

where L_1, L_2 ,…, L_N are lower boundaries of each range and they are defined as $L_1 < L_2 < \ldots < L_N$.

In the fitting process using the MATLAB® Curve Fitting Toolbox, the coefficient X_k and Y_k may hit pre-defined searching boundaries (τ_N and L_N). When this occurs, a 'fixed at bound' message occurs. These boundaries have to be adjusted and expanded step-by-step to let the fitting algorithm explore all possible fitting conditions. In addition, the choice of values of M_P, τ_0, L_1,…, L_N and N parameters affect the goodness of fitting. In particular, N, τ_0, and M_P are important. N affects model complexity directly whilst τ_0 and M_P control the time duration that the model covers. If M_P is set too high, the time response between the adjacent time constant ranges will be poor.

2.5.1.5 Constant Voltage Method

To investigate the long-term SC characteristic or the energy retention, the constant voltage (CV) method is used. By applying the CV method for a long period, the steady-state voltage level is confirmed as charges are fully distributed within the SC pores on the electrode surface. The energy retention characteristic is then observed.

The energy retention characteristic can be defined by the self-discharging voltage characteristic, *SDVC* (or so called potential decay in [87]), and a leakage current, I_{Leak} (or so called floating current in [87]). A *SDVC* is observed from the terminal voltage of the DUT when it is disconnected from sources. On the other hand, I_{Leak} is a record of the steady-state current that is fed from a constant voltage source to maintain the DUT voltage. Both I_{Leak} and *SDVC* are usually observed and measured at several different DC-bias voltage conditions across the DUT. If the *EPR* is used to model SC energy retention, *EPR* can derived from:

$$v_{SC}(t) \approx v_{SC}(0) e^{-\frac{t}{EPR_{SDVC} C}} \rightarrow EPR_{SDVC} = -\frac{t}{C \ln\left(v_{SC}(t)/v_{SC}(0)\right)} \tag{2.12}$$

$$EPR_{I\_Leak} = \frac{V_S}{I_{Leak}} \tag{2.13}$$

Where $v_{SC}(0)$ and $v_{SC}(t)$ are measured SC voltages at t = 0 and at time t after removing the SC from the CV source, C is rated capacitance, I_{Leak} is a measured leakage current, V_S is an applied constant voltage.

These energy retention terms are chosen and used in different applications. The term is chosen according to the way the DUT is operated in the application. For example, in UPS and stand-by energy storage applications, the energy storage stack is connected to the fixed DC voltage level during the stand-by period, so I_{Leak} is chosen. On the other hand, in some applications, SC stacks may be charged or discharged and left unused for some time. In this case, a *SDVC* term is chosen. In addition, the *SDVC* term should not be confused with the SC relaxation characteristic that occurs after disconnecting the devices from the power supply. The voltage observation periods are on a different time scale (e.g. less than 10 minutes for the relaxation period and tens of minutes or more for the self-discharging period). In this study, both terms are investigated.

The duration of applied CV method depends on the energy retention period of each application. In the IEC standard EN 62391-1:2006 [22], it is recommend to charge with the CV method at the rated voltage of DUT for 8 hours. Consequently, the DUT is disconnected and its voltage is observed for either 16 or 24 hour periods. However, in the IEC standard EN 62576:2010, which is applied particularly for HEV application, the DUT terminal voltage is observed for 72 hours after disconnecting from the CV source. In [83], the *SDVC* investigation time can be > 24 hours (e.g. from days to months and months to years). In this study, the observation period is chosen depending on the DUT energy capacity (i.e. the rated C and the rated voltage), which will be detailed in Section 4.2.5.

2.5.1.6 Summary of the SC Models and the SC Characterization Methods for Extracting the SC Model Parameters

The estimated models that have been presented in Section 2.4 are now mapped against and are matched with the identification methods presented in Section 2.5.1 as shown in Table 2.1. Since the standard CC method can be applied only to a single RC model, it was decided to be excluded.

Table 2.1 Mapping of the equivalent models against characterizing methods

	Method to determine model		
Model	PCC	Non-standard CC	EIS
I	[34]	-	-
II	-	-	[29,30]
III	-	[32,33]	-
IV	[35]	-	[28,31]
V	-	[79]	-
VI	[24]	-	[80]

Theoretically, all equivalent models can be used in conjunction to any of the presented characterization techniques. However, in practice, some models are easy to be analyzed using the time domain response technique (i.e. using the non-standard CC and the PCC methods) but they are very difficult to be analyzed using the frequency domain response technique (i.e. using the EIS method) and vice versa. The incompatible pairs have been left blank in Table 2.1. It can be noted that model I received low interest from literatures because it cannot represent the SC relaxation characteristic.

The advantages and disadvantages of using each of the selected SC characterizing technique are summarized in Table 2.2.

Table 2.2 Advantages and disadvantages of each characterizing technique

	CC		PCC	EIS
	Standard	Non-standard		
Model complexity	Poor ☹	Excellent ☺	Excellent ☺	Excellent ☺
Model accuracy during transient	Poor ☹	Good ☺	Excellent ☺	Excellent ☺
Processing time	Short ☺	Medium ☺	Medium ☺	Long ☹
Limitation	Depending on the rated voltage and the rated current and rise time of the power supply			

The characterizing procedure stated in the standard CC method is designed for producing the characterizing results that fit with the single RC model only. The results cannot be applied to very complicated models, and for this reason the method itself has limited/poor model complexity. In addition, the single RC model cannot represent the SC relaxation, so its transient accuracy is poor. On the other hand, this method has short characterizing time because the model is simple.

The other three methods, the EIS method, the non-standard CC method and the PCC method can allow for high modeling complexity and very accurate results. However, these methods take more effort/time to process. In particular, the EIS method characterizing time can span from fraction of an hour to hours depending on the number of frequency testing points and the minimum frequency testing.

Special equipment called potentiostat/galvalnostat is required to perform the EIS method. This equipment technology relies on linear regulators to control the testing voltage and the current, which have small rise time and fall time (μs range). Currently the technology is limited to 50V with 1A or 5V with 100A as specified in the manufacturer (Bio-Logic) product range. Therefore, based on the specification, only low voltage devices of limited capacitance (<1kF) can be characterized with the EIS technique. On the other hand, the standard CC method, the non-standard CC method and the PCC method have their capabilities limited by the rated voltage, the rated current and the current rise time of the power supply used.

In this study, the EIS and the PCC methods are selected to determine the equivalent model parameters because it allows the comparison between models derived from

different techniques (frequency domain based and time domain based). From Table 2.1, model IV and VI can be determined by either the EIS or the PCC methods. However, as mentioned in the previous section, model VI is used for age monitoring and failure diagnosis and not for describing and reproducing the dynamic behavior of SCs. Therefore, model IV is chosen to represent the SC dynamic characteristic. Model IV is also used in the emulator application presented in Chapter 6. A comparison of the derived model parameters from the EIS and PCC experimental results will be shown in Chapter 4.

2.5.2 Characterization Methods for Evaluating Round-trip Efficiency of SC

SC efficiency has been investigated experimentally using large signal methods. There are sinusoidal current [36], quasi-square wave current [37], constant current [34,38,39] and constant power [40]. However, the methods discussed in [38-40] focus on evaluating and analyzing SC efficiency separately either during charging or discharging. These methods [38-40] are simple to apply, but they may be irrelevant to the way SCs are operated in typical applications. Since SCs, which are bi-directional power-flow energy storage devices, are likely to be charged and discharged at high constant power level, SCs should be evaluated in a charge-discharge cycle [34,36,37], where initial and final SC voltages are the same (i.e. a round-trip pattern). In this thesis, only methods used to evaluate a SC round-trip efficiency, η_{RT}, and energy loss, E_{Loss_RT}, over a charge-discharge cycle are considered and discussed. A round-trip efficiency is an efficiency evaluated through a charge-discharge pattern.

2.5.2.1 The Sinusoidal Current Method

In [36], the η_{RT} and E_{Loss_RT} are investigated under an applied sinusoidal current. An air-cooled open-type calorimeter is employed to verify the energy loss calculation. By measuring the difference between input and output air temperature of the calorimeter and calculating the air-flow rate together with a specific heat of air and an air density, the SC power loss and finally E_{Loss_RT} can be determined. However, it is difficult to apply this technique to large SC systems due to the physical limitation of calorimeter size. Poor accuracy of temperature measurement

and difficulty in managing inlet/outlet air-flow rate become more pronounced with increased calorimeter size.

2.5.2.2 The Quasi-square Wave Current Method

In [37], a charge-discharge quasi-square wave current is applied to the SC at low-frequency e.g. mHz). The applied current cycling period is fixed at 60sec, but the maximum constant current (e.g. 50A, 100A and 150A) and the charging and discharging periods are varied. The method proved to be useful to evaluate η_{RT} against RMS current. On the other hand, a square-wave charge-discharge constant-current method [34] is very simple to use, and it is discussed in the next section.

2.5.2.3 Constant Current Cycling Method

In [34], a square-wave charge-discharge constant-current and a pulse-train charge-discharge constant-current are applied at several current levels. In both methods, the current is controlled constant according to their patterns during cycling (i.e. either a square wave or a pulse-train shapes), and the SC stack voltage information is used only for toggling the current direction when the min/max voltage thresholds are reached. The square wave method can be considered as a traditional method that has been used to characterize a battery having a nonlinear V-I characteristic. In both methods, to evaluate the SC η_{RT} and E_{Loss_RT}, an integration of the SC power waveform, constructed from the SC voltage-current information per charge-discharge cycle, is required. The η_{RT} and E_{Loss_RT}, are calculated by:

$$\eta_{RT} = \frac{-\int_{0}^{T_D} p_{SC}\,dt}{\int_{0}^{T_C} p_{SC}\,dt} = \frac{-E_D}{E_C} \tag{2.14}$$

$$E_{Loss\_RT} = E_C + E_D \tag{2.15}$$

Where p_{SC} is the instantaneous power through the SC (the product of current, i_{SC}, and voltage, v_{SC}), E_C is the charging energy, E_D is the discharging energy, T_C is the charging period, and T_D is the discharging period.

However, unlike batteries, the state of charge (SOC) for SC depends on the terminal voltages, so a constant current cycling (CCC) method is not equivalent to a constant power cycling (CPC) method. The power waveform constructed from these CCC methods is not close to a square wave, and when performing numerical integration (e.g. using a trapezoidal rule) on this non-square power waveform, errors arise from the sampling frequency limitation of the equipment. The error can be accumulated further if the charge-discharge period is long (e.g. in range of 100s of seconds), which occurs at low constant current cycling setting and wide SC voltage operating range.

Alternatively, a constant power cycling (CPC) can be used to evaluate the SC η_{RT} and SC E_{Loss_RT} [57], and this will be detailed in the next section.

2.5.2.4 The Proposed Method: Constant Power Cycling Method

The CPC method is originally used in aging tests [88] to study SC degradation. However, the author adopts this method, for the first time, for evaluating SC η_{RT} and SC E_{Loss_RT} in [57]. In addition, operating SCs in the power control mode is relevant to many applications, such as in HEVs [41-44], hybrid excavators [45], wind turbines [46], elevators [47], port rubber-tyred gantry cranes [48] and so on. Constant power control is also commonly used for determining the SC power-energy characteristic subject to voltage limits [49].

Since the SC SOC depends on its terminal voltage, SCs are usually operated in a power control mode according to the power demand from the load rather than constant current control. Thus, the SC stack voltage, v_{SC}, is used in deriving a current reference, i_{SC_Ref}, according to a power reference, p_{SC_Ref} as:

$$i_{SC\_Ref} = \frac{p_{SC\_Ref}}{v_{SC}} \tag{2.16}$$

In the CPC method, as in the CCC method, the v_{SC} is also used for toggling the current direction as well as the power direction when the min/max voltage thresholds are reached. For the CPC method, the time period is slightly more than the CCC method for the same maximum applied current and the same SC operating voltage range. However, the error due to the sampling problem (i.e. truncation error) in the

power waveform integration is minimised even though the sampling frequency is low. This is because the numerical integration is performed effectively on the square power waveform.

2.6 Round-trip Efficiency and Energy Loss Estimation Methods

In this section, the SC round trip efficiency and round-trip energy loss estimation methods are discussed and presented. Three authors have used models of various complexities to do this [37,39,49].

In [39], the SC transmission-line model (model II) determined from a method similar to the EIS (i.e. utilizing a frequency response technique) is used for SC efficiency estimation. The model parameters take into account the SC voltage dependency and temperature effect, so the model voltages fit well to the actual SC transient voltages over a wide range of operating temperature (-10 to 40°C) and voltages (0 to 100V). Both the actual and model voltage-current profiles at different temperature conditions are used to calculate the amount of processed energy. In addition, the resistive components in the model and the real part of the actual SC impedance are also used to calculate the SC energy loss at different temperatures. Thus, excluding the SC energy loss from the total processing energy, the SC efficiency-temperature relationship is established.

In [49], the single RC model determined from a cyclic voltammogram is used in the efficiency estimation of the SC operating in the constant power mode. In the electrochemical research community, cyclic voltammetry is widely used for characterizing electrochemical devices. The method allows the user to set a scan rate (mV/s) to charge/discharge the DUT within the voltage setting limits. However, the parameters derived from the cyclic voltammogram are limited to specific test conditions, so they cannot be applied to different conditions.

In both [39] and [49], the SC efficiency is evaluated and estimated at either charging and discharging separately (i.e. not round-trip manner). Therefore, it cannot be used for our applications.

In [37], the SC transmission-line model determined from the quasi-square wave charge-discharge current method at low-frequency range (e.g. mHz) is used to represent the SC characteristic. The model is simplified further to the simple RC structure with the voltage-dependent capacitor, and this simplified model is used to estimate the SC round trip efficiency. The experimental results in [37] show a good agreement with the estimated the SC round trip efficiency over a wide range of applied constant current. However, the error between the experiment and the estimation is increased at higher applied current levels. This increased error may be due to the increasing stack temperature, which in turn, causes the SC parameters determined at the testing temperature to change. This small error in the estimated efficiency actually means a large error in the estimated energy loss.

From [39] and [37], one can conclude that to estimate the SC round trip efficiency and the SC round-trip energy loss accurately, the DC-bias voltage and the operating temperature must be considered since they affect the parameters; there must be updated during the estimation process. From [49] and [37], it is shown that the simple RC model is sufficient for estimating the SC round trip efficiency and loss.

2.6.1 The Proposed Methods for Round-trip Efficiency and Energy Loss Estimation

To account for the impact of DC bias voltage and temperature on the estimation of the SC round-trip efficiency, η_{RT}, and the energy loss, E_{Loss_RT}, the author proposes four estimation approaches, which are:

- the estimation based on SC charge-discharge duty cycle under CPC (Section 2.6.1.1)
- the estimation based on SC voltage measurement (Section 2.6.1.2)
- the estimation based on SC current measurement (Section 2.6.1.3)
- the estimation based on SC current measurement with the FFT algorithm (Section 2.6.1.4)

The methods are arranged in order of increasing complexity. To evaluate energy loss, the first method uses time duration and the SC power information. The second uses the SC voltage and the impedance information, and the third and the fourth use

the SC current and the impedance information. All four approaches will be verified in relation to the η_{RT} and E_{Loss_RT}, and the discrepancies between the estimated and the experimental results will be presented in Chapter 4.

2.6.1.1 Efficiency Estimation Based on the Duty Cycle Method

As mentioned in Section 2.5.2.4, the CPC method is employed to evaluate SC round-trip efficiency. In this method, SC round-trip efficiency can be estimated directly from a charge-discharge duty cycle, d_{CD} [57]. If the SC is operated in the CPC mode, the p_{SC} waveform can be depicted as Figure 2.16, where T_{CD} is a charge-discharge period, T_C is a charging period, T_D is a discharging period, P_C is a constant charging power level, and P_D is a constant discharging power level.

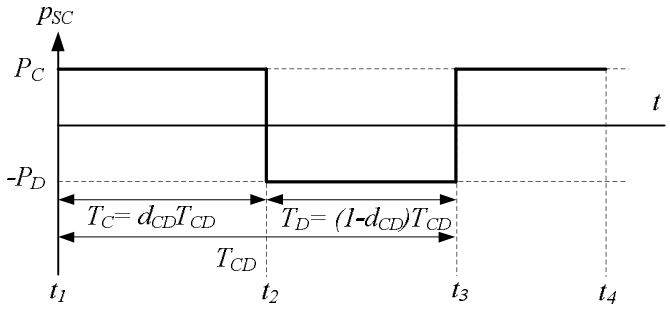


Figure 2.16 Supercapacitors operated under the constant power cycling mode

From (2.14) and Figure 2.16, $p_{SC} = P_C$ for T_C and $p_{SC} = -P_D$ for T_D. The estimated round-trip SC efficiency from the duty cycle, η_{EST_Duty}, can be defined as:

$$\eta_{EST\_Duty} = \frac{|P_D T_D|}{|P_C T_C|} \tag{2.17}$$

Since $T_D = T_{CD} - T_C$ and $d_{CD} = \frac{T_C}{T_{CD}}$, (2.17) becomes

$$\eta_{EST\_Duty} = \left|\frac{P_D}{P_C}\right|\left(\frac{T_{CD} - T_C}{T_C}\right) = \left|\frac{P_D}{P_C}\right|\left(\frac{T_{CD}}{T_C} - 1\right) = \left|\frac{P_D}{P_C}\right|\left(\frac{1}{d_{CD}} - 1\right) \tag{2.18}$$

If P_D and P_C are equal and constant (= P), then:

$$\eta_{EST\_Duty} = \frac{1}{d_{CD}} - 1 \tag{2.19}$$

Equation (2.18) can be considered as an online method for estimating η_{RT} of the SC operated under the CPC since they use the measured d_{CD}, and the measured power to calculate efficiency. In addition, if the power level during charging and discharging is controlled perfectly equal ($|P_C| = |P_D|$) since there is no DC voltage offset from voltage and current sensors, then the estimated η_{RT} from (2.19) is derived only from the time information.

This method is considered as the quickest and the simplest method that can estimate η_{RT} from the CPC profile. However, it does not give information related to the SC model parameters. Thus, it cannot be used to investigate the change inside the SC device, which is important for studying SC aging analysis and SC regenerative effects.

2.6.1.2 Energy Loss Estimation Based on Voltage Measurement

The author proposes that the analytical efficiency and the analytical energy loss formulas presented in [49] can be combined to estimate η_{RT} and E_{Loss_RT}. In [49], the single RC model (presented here again as Figure 2.17)

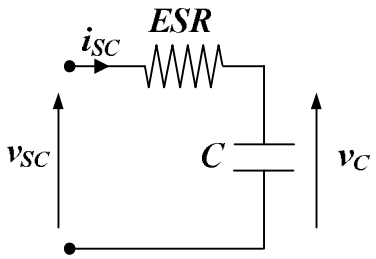


Figure 2.17 Simplified RC model of a SC

According to the SC model in Figure 2.17,

$$v_{SC}(t) = v_C(t) + i_{SC}(t)\,ESR \tag{2.20}$$

where v_C is the ideal capacitor voltage, v_{SC} is the terminal voltage, and i_{SC} is the current flowing through the SC. Since the stack is operated in the CPC mode:

$$i_{SC}(t)\,v_{SC}(t) = P_{SC} \Rightarrow i_{SC}(t) = \frac{P_{SC}}{v_{SC}(t)} \tag{2.21}$$

where P_{SC} is the applied constant power at the SC terminals. It is positive in the charging mode and negative in the discharging mode. Figure 2.18 depicts the ideal

capacitor voltage, the terminal voltage, the operating current and the operating power waveforms during the CPC method. In Figure 2.18, V_{Cmin} and V_{Cmax} are minimum and maximum ideal capacitor voltages, V_{SC_cmin} and V_{SC_cmax} are minimum and maximum SC terminal voltages during the charging period, V_{SC_dmin} and V_{SC_dmax} are minimum and maximum SC terminal voltages during the discharging period, I_{SC_cmin} and I_{SC_cmax} are minimum and maximum SC current during the charging period, I_{SC_dmin} and I_{SC_dmax} are minimum and maximum SC current during the discharging period, P_C is the charging constant power and P_D the discharging constant power.

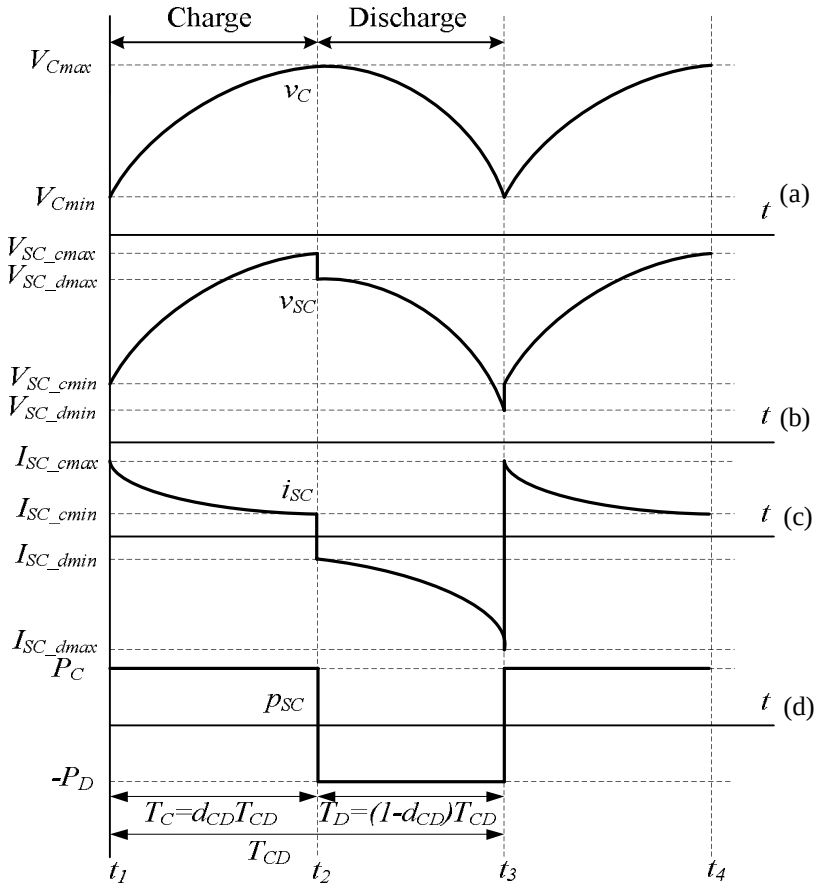


Figure 2.18 SC typical waveforms for the CPC method based on the RC model: a) ideal capacitor voltage; b) terminal voltage; c) current and d) power.

In order to find the relationship between v_C and v_{SC} under the CPC mode, i_{SC} is substituted from (2.21) into (2.20):

$$v_{SC}^2(t) - v_C(t)v_{SC}(t) - P_{SC}ESR = 0 \tag{2.22}$$

Solving for v_T by using the common quadratic formula and considering only the positive solution:

$$v_{SC}(t)=\frac{v_C(t)+\sqrt{v_C^2(t)+4P_{SC}ESR}}{2} \tag{2.23}$$

where for efficient operation, $v_{SC}(t)>\frac{v_C(t)}{2}$.

Re-arranging (2.21) for P_{SC} and substituting $i_{SC}(t)$ as $i_{SC}(t)=C(dv_C/dt)$ where C is the capacitance, yields

$$P_{SC}=v_{SC}(t)C\frac{dv_C}{dt}\Rightarrow P_{SC}dt=\left(Cv_{SC}(t)\right)dv_C$$

From (2.23), substituting $v_{SC}(t)$ in:

$$P_{SC}dt=\frac{C}{2}\left(v_C(t)\right)dv_C+\left(\frac{C}{2}\sqrt{v_C^2(t)+4P_{SC}ESR}\right)dv_C \tag{2.24}$$

and performing the analytical integration on both sides of (2.24) assuming P_{SC} is constant during the integration interval, then:

$$P_{SC}\int_{t_i}^{t_f}dt=\frac{C}{2}\int_{v_{Ci}}^{v_{Cf}}\left(v_C(t)\right)dv_C+\frac{C}{2}\int_{v_{Ci}}^{v_{Cf}}\left(\sqrt{v_C^2(t)+4P_{SC}ESR}\right)dv_C \tag{2.25}$$

Here t_i and t_f are the start and the final times of the integration time interval respectively, and v_{Ci} and v_{Cf} are the ideal capacitor voltages at t_i and t_f. Using a commercial symbolic solver program, the complicated integration term in (2.25) can be solved using the following relationship:

$$\int\left(\sqrt{x^2+4P_{SC}ESR}\right)dx=\frac{1}{2}x\sqrt{x^2+4P_{SC}ESR}+2P_{SC}ESR\,ln\left(x+\sqrt{x^2+4P_{SC}ESR}\right) \tag{2.26}$$

Using (2.26) and performing integration on all terms of (2.25), yields the SC input or output energy during the integration time interval, $[t_i, t_f]$:

$$\begin{aligned}E=P_{SC}\,t\Big|_{t_i}^{t_f}&=C\frac{v_C^2}{4}\Bigg|_{v_{Ci}}^{v_{Cf}}+C\frac{v_C\sqrt{v_C^2+4P_{SC}ESR}}{4}\Bigg|_{v_{Ci}}^{v_{Cf}}\\&+CP_{SC}ESR\,ln\left(v_C+\sqrt{v_C^2+4P_{SC}ESR}\right)\Big|_{v_{Ci}}^{v_{Cf}}\end{aligned} \tag{2.27}$$

From (2.27), the integration limits (i.e. t_i, t_f, v_{Ci} and v_{Cf}) of the charging period and the discharging period are different. The integration limits are inspected from Figure 2.18 and shown in Table 2.2.

Table 2.3 The integration limits during the charging and the discharging periods taken from Figure 2.18

Operation	t_i	t_f	t_f-t_i	v_{Ci}	v_{Cf}
Charging	t_1	t_2	T_C	V_{Cmin}	V_{Cmax}
Discharging	t_2	t_3	T_D	V_{Cmax}	V_{Cmin}

Thus, from (2.27) and Table 2.2, the inflow (charging) and outflow (discharging) of energy at constant power operation of P_C and P_D respectively can be determined as:

$$E_C = P_C T_C = C\frac{v_C^2}{4}\Bigg|_{V_{C\,min}}^{V_{C\,max}} + C\frac{v_C\sqrt{v_C^2+4P_C ESR}}{4}\Bigg|_{V_{C\,min}}^{V_{C\,max}} + CP_C ESR\,ln\left(v_C+\sqrt{v_C^2+4P_C ESR}\right)\Bigg|_{V_{C\,min}}^{V_{C\,max}} \tag{2.28}$$

$$E_D = P_D T_D = C\frac{v_C^2}{4}\Bigg|_{V_{C\,max}}^{V_{C\,min}} + C\frac{v_C\sqrt{v_C^2+4P_D ESR}}{4}\Bigg|_{V_{C\,max}}^{V_{C\,min}} + CP_D ESR\,ln\left(v_C+\sqrt{v_C^2+4P_D ESR}\right)\Bigg|_{V_{C\,max}}^{V_{C\,min}} \tag{2.29}$$

Thus, the estimated voltage-based round-trip efficiency, η_{EST_V}, and the estimated voltage-based round-trip energy loss, $E_{Loss\_EST\_V}$, are obtained by using (2.28) and (2.29) assuming constant discharging and charging powers of P_D = -P and P_C = P, respectively as:

$$\eta_{EST\_V} = \frac{-E_{D\_EST\_V}}{E_{C\_EST\_V}} \tag{2.30}$$

$$E_{Loss\_EST\_V} = E_{D\_EST\_V} + E_{C\_EST\_V} \tag{2.31}$$

where:

$$E_{C\_EST\_V} = \frac{C_{Period}}{4}\left(V_{C\_max}^2 - V_{C\_min}^2\right)$$
$$+C_{Period} P_{C\_avrg} ESR_{Period} ln\left(\frac{V_{C\_max} + \sqrt{V_{C\_max}^2 + 4P_{C\_avrg} ESR_{Period}}}{V_{C\_min} + \sqrt{V_{C\_min}^2 + 4P_{C\_avrg} ESR_{Period}}}\right)$$
$$+\frac{C_{Period}}{4}\left(V_{C\_max}\sqrt{V_{C\_max}^2 + 4P_{C\_avrg} ESR_{Period}} - V_{C\_min}\sqrt{V_{C\_min}^2 + 4P_{C\_avrg} ESR_{Period}}\right)$$
$$E_{D\_EST\_V} = -\frac{C_{Period}}{4}\left(V_{C\_max}^2 - V_{C\_min}^2\right)$$
$$+C_{Period}\left|P_{D\_avrg}\right| ESR_{Period} ln\left(\frac{V_{C\_max} + \sqrt{V_{C\_max}^2 - 4\left|P_{D\_avrg}\right| ESR_{Period}}}{V_{C\_min} + \sqrt{V_{C\_min}^2 - 4\left|P_{D\_avrg}\right| ESR_{Period}}}\right)$$
$$-\frac{C_{Period}}{4}\left(V_{C\_max}\sqrt{V_{C\_max}^2 - 4\left|P_{D\_avrg}\right| ESR_{Period}} - V_{C\_min}\sqrt{V_{C\_min}^2 - 4\left|P_{D\_avrg}\right| ESR_{Period}}\right)$$

Note that C_{Period} and ESR_{Period} are C and ESR read from the EIS result at a frequency = $1/T_{CD}$. P_{C_avrg} and P_{D_avrg} are the average powers during the charging and discharging period. Since this method only employs voltage information from the power cycling experiment, it is referred as 'Voltage-based' energy loss estimation.

However, as will be shown later in Chapter 4 that achieving an accurate energy loss estimation is more difficult than achieving an accurate round-trip estimation. Considering 100J of processed energy and 90% η_{RT}, the energy loss is 10J. A 1% error in the η_{RT} estimation gives an estimated energy loss of 11J or 10% error. For this reason, the E_{Loss_RT} is also considered for further analysis.

2.6.1.3 Energy Loss Estimation Based on Current Measurement

As an alternative method to the voltage-based approach, a conventional power loss calculation based on the RMS current of a constant value resistor, R, ($P_R = I_{RMS}^2 R$) is applied to evaluate the E_{Loss_RT} over a single charge-discharge period, T_{CD}. From the measurement, an instantaneous current i_j at each sampling point j^{th} and ESR_{Period} are obtained, so an instantaneous power loss P_j can be calculated as (2.32). By accumulating this power loss for N_{Samp} sample points over a single T_{CD}, a total power loss is obtained. By multiplying this total loss with a sampling time T_{Samp}, the estimated current-based round-trip energy loss, $E_{Loss\_EST\_I}$, is calculated by (2.33). Since this method only employs the current information from the power cycling experiment, it is referred as 'Current-based' energy loss estimation.

$$P_j = i_j^2 ESR_{Period} \tag{2.32}$$

$$E_{Loss\_EST\_I} = \sum_{j=1}^{N_{Samp}} \left(P_j\right) T_{Samp} \tag{2.33}$$

However, by using (2.33) and the ESR_{period} read from the EIS results at a frequency $=1/T_{CD}$, the E_{Loss_EST} can be overestimated. The comparison between the experimental and the estimated results will be presented in Chapter 4. In the EIS method, the applied current is sinusoidal and the derived *ESR* is valid at the applied frequency condition. On the other hand, the current used in the CPC mode is periodic but non-sinusoidal. Therefore, the non-sinusoidal current should be decomposed by the Fast Fourier Transform (FFT) algorithm. The harmonics can be analyzed with the *ESR* determined from the EIS method at the same frequency. This FFT analysis method is presented next.

2.6.1.4 Energy Loss Estimation Based on Current Measurement with the FFT Algorithm

Instead of processing the measured current in a time domain as done in Section 2.6.1.3, it can be processed in the frequency domain. By applying an FFT algorithm, fundamental, harmonics and DC offset components of the current are obtained separately at a specific frequency. Then using the fundamental and harmonic components I_k with ESR_k extracted from the EIS method at a matched frequency, a power loss, P_{IFFT_k}, can be calculated from (2.34). Consequently, by accumulating this power loss for N_{Har} harmonics, the total power loss is obtained. Multiplying this quantity by T_{CD}, the estimated SC current-based FFT round-trip energy loss, $E_{Loss\_EST\_IFFT}$, is calculated by (2.35).

$$P_{IFFT\_k} = I_k^2 ESR_k \tag{2.34}$$

$$E_{Loss\_EST\_IFFT} = \sum_{k=1}^{N_{Har}} \left(P_{IFFT\_k}\right) T_{CD} \tag{2.35}$$

As will be shown later in Section 4.4.3 that there is a big reduction in estimated energy loss when the FFT method is applied. This improvement is due to interpolating the *ESR*s calculated from the discrete measured impedance over

frequency. However, the difficulty in using this method is the large number of frequency points required from the EIS testing process especially in the low frequency range (<1Hz). Therefore, practically, the ESR_k at missing frequencies, f_k, is determined from a linear interpolation between the 2 adjacent measured *ESR*-frequency points (e.g. $ESR_1@f_1$ and $ESR_2@f_2$) as depicted in Figure 2.19.

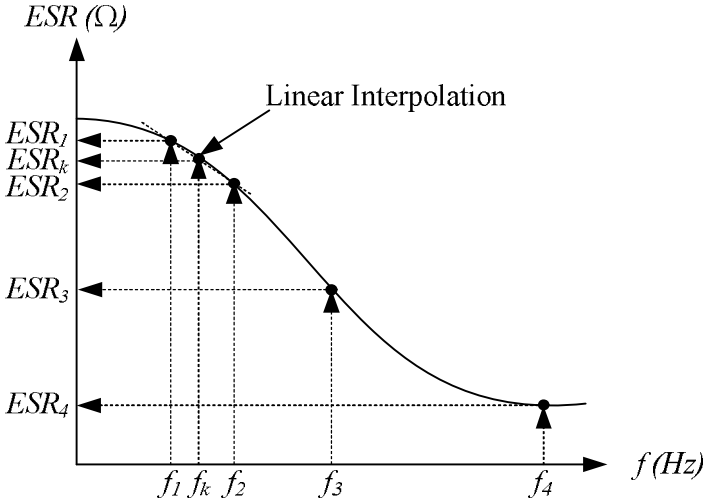


Figure 2.19 Process to map *ESR*s out at the requested frequency of harmonic currents

2.6.1.5 Summary of Round-trip Efficiency and Energy Loss Estimation Methods

In summary, in the η_{RT} and the E_{Loss} estimation process, a stack current, a stack voltage and stack power information obtained during the CPC experiment are used as input parameters together with the stack impedance versus frequency information obtained from the EIS method. The η_{RT} and the E_{Loss} estimation methods are divided into the duty-cycle, the Voltage-based, the Current-based and the Current-based with FFT, which use formulas as summarized in Figure 2.20. The advantages and disadvantages of each loss estimation method are summarized in Table 2.4.

From Table 2.4, the duty cycle method is the simplest among other proposed methods. The duty cycle method uses d_{CD} to estimate the efficiency, which can be captured and calculated precisely by high sampling-frequency digital oscilloscopes, so the error can be low. This method requires that P_C equals P_D. On the other hand, the voltage measurement method, the current measurement method and the current measurement method with the FFT algorithm use the SC impedance information obtained through the EIS test to perform the estimation, which make them more complex that the duty cycle method.

The voltage measurement method can estimate both the efficiency and loss whist both of the current measurement methods can only estimate the loss. It gives high error in the loss estimation as it uses many different measurement values in the calculation (i.e. the error of each measurement combines).

The current measurement methods calculate the loss using a single variable model dependent; the real SC impedance information, so they offer better loss estimation. By employing the FFT algorithm, the loss estimation can be improved further as the loss is calculated for all relevant frequency domain current components.

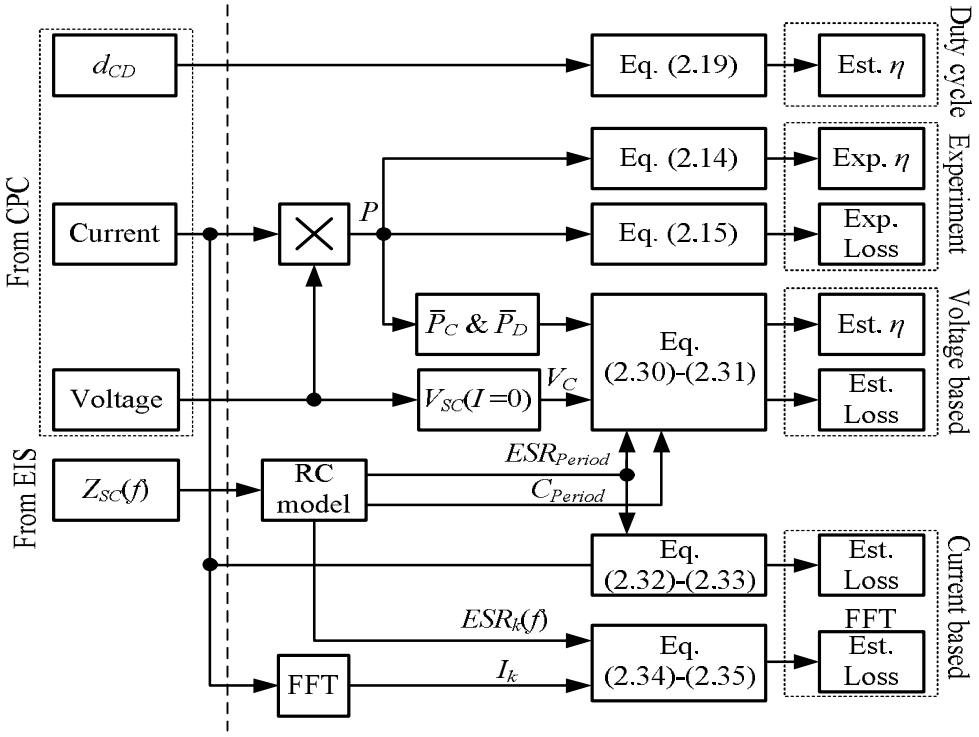


Figure 2.20 Summary of the processes for calculating experimental and estimated energy loss (current-based and voltage-based)

Table 2.4 Advantages and disadvantages of each method

	Duty cycle method	Voltage measurement	Current measurement	Current measurement with the FFT
Method complexity	Very simple ☺	Average ☺	Simple ☺	Complex ☹
Estimated parameters	Only efficiency ☹	Both efficiency and loss ☺	Only loss ☹	Only loss ☹
Requirements/ limitations	P_C=P_D	Use the SC impedance information and the error also depends on the impedance accuracy		
Loss error	Low	High	Medium	Low

2.7 Conclusion

In this chapter, the SC characterization standards are presented and summarized. Some techniques presented in the standards are useful, so they are adopted in the characterization process used in this study to improve consistency of the experimental results.

The single RC model cannot represent the SC characteristics since the SCs are affected by operating time period (transient or steady-state condition), operating voltage range, energy retention period (self-discharging) and operating temperature. Therefore, several SC models reported in literature are discussed and employed. In this study, the series-parallel RC model is selected, and is used in the emulator application as will be presented in Chapter 6.

In addition, the characterization methods are presented and divided mainly into 2 groups according to the characterizing objectives, which are to identify model parameters representing SC characteristics and to evaluate the SC round-trip efficiency.

To identify model parameters representing SC characteristics, three methods, which are an electrochemical impedance spectroscopy (EIS), a pulse constant current (PCC) and a constant voltage (CV), are used. The first two methods are used to identify the SC short-term response model parameters, and the third method is used to identify the SC long-term response model parameter.

To evaluate SC round-trip efficiency, a constant power cycling method (CPC) is employed. In addition, to estimation the SC round-trip efficiency and SC energy loss, four estimation approaches are proposed, which are the duty-cycle, the Voltage-based, the Current-based and the Current-based with FFT.

Chapter 3 Experimental Rigs and the SC Characterization Processes

3.1 Introduction

In this chapter, the devices under test and the experimental rigs of supercapacitors (SCs) are presented and described.

The DUTs in this project are the Maxwell® PC5 SC, the Maxwell® BMOD SC 15V stack, the ELIT® SC 20V stack and the supercapattery prototypes. The specification of each device is presented in Section 3.2. The Maxwell® PC5 SCs were assembled as a stack, which has the specification similar to the supercapattery stack, so the performance of both Maxwell® SC stack and supercapattery stack can be compared. The specification of the Maxwell® SC stack is presented in Section 3.3.

There were three rigs used in the characterization work, which are a switched-mode converter with an analog hysteresis current control (Rig I), a six-channel interleaved switched-mode converter with a digital PI current control (Rig II) and commercial linear current regulators (Rig III). The detail of each rig is presented in Section 3.4. Additionally, Rig III is also used as a SC emulator system in Chapter 6.

The characterizing methods presented in Chapter 2 are combined as three processes and are presented in Section 3.5. These are:

- Process to identify model parameters representing SC short-term characteristics
- Process to identify model parameters representing SC long-term characteristics
- Process to evaluate SC round-trip efficiency

3.2 Supercapacitors and the Supercapattery

Commercial SCs are available in different packages (discrete or modular), different constructions (prismatic or cylindrical), different types (high energy or high power series), and with different electrolytes (organic or aqueous). The SCs tested in this project are listed below, and the specifications extracted from their datasheets are summarized in Table 3.1.

- Maxwell® PC series PC5 4F 2.5V
- Maxwell® BC power series 15V module BMOD0052 P015 52F
- ELIT® 20V supercapacitor
- Supercapattery prototype stacks

For organic-based electrolyte SCs, the Maxwell® PC5 (Figure 3.1) is the smallest capacitance device having only 4F and 2.5V per cell. This cell was tested at the initial phase of this project, and it was built for comparison with the nineteen-cell supercapattery prototype stack (Figure 3.4) which has the similar specification. The BMOD0052 (52F 15V) SC module as presented in Figure 3.2 was also tested. This module is assembled from the BCAP0310 P250 (310F 2.5V) devices. All Maxwell® SCs are built with organic electrolyte, which is commonly used by many manufacturers (e.g. NESSCAP®, LS® Ultracap, IOXUS® and so on).

For aqueous-based electrolyte SCs, the ELIT® SC 20V stack (Figure 3.3) and the supercapattery (Figure 3.4) were tested. Two supercapattery prototypes were used in this project: the nineteen-cell stack and the three-cell stack. The supercapattery technology is based on carbon nanotubes (CNTs) and is different from commercial SCs which use activated carbon. The supercapattery specifications provided from the School of Chemical Engineering, University of Nottingham, are also listed in the Table 3.1. The experimental results of the Maxwell® PC5 and the nineteen-cell supercapattery devices will be presented in Chapter 4. The nineteen-cell stack is optimized for higher specific power and is compromised in energy capability. Meanwhile, the three-cell stack is optimized for increased energy density and compromises on power capability.

Figure 3.1 Maxwell® PC series PC5 4F 2.5V

Figure 3.2 Maxwell® BC BMOD power series 15V module BMOD0052 P015 52F

Figure 3.3 ELIT® supercapacitor 92F 20V

Figure 3.4 Supercapattery nineteen-cell stack 0.7F 19V

The results for the Maxwell® BMOD0052, ELIT® SC and the three-cell supercapattery devices are found in Appendix B in order to reduce the length of the main text.

Table 3.1 Summarize parameters of each device from datasheet

Parameters from datasheet	Maxwell® Ultracapacitors		ELIT® Supercapacitor	Supercapattery (information from Chem. Eng. Dept.)	
	PC5	BMOD0052 P015 (Module)		Nineteen-cell stack	Three-cell stack
ESR at DC (mΩ)	400	14.5	<4.2	N/A	N/A
ESR at 1kHz (mΩ)	290	8	N/A	N/A	N/A
Maximum Continuous Current (A)	1	20	N/A	6	2
Leakage current (μA)	20	1000	N/A	N/A	N/A
Equivalent Capacitance (F)	4	52	92	1	30
Maximum Voltage (V)	2.5	15	20	19	5
Usable Specific Power (kW/kg)	0.47	2.7	0.94*	N/A	N/A
Maximum Specific Power (kW/kg)	1.35†	10.3	N/A	147.3	N/A
Maximum Specific Energy (Wh/kg)	0.87‡	2.39	0.42‡	20.3	N/A
Weight (kg)	0.004	0.68	12.2	N/A	N/A
Electrolyte type	Organic type		Aqueous type		
Technology	Activated carbon			CNTs	
References	[89]	[90,91]	[92,93]	N/A	N/A

*Usable Specific Power = $\frac{0.12V_{max}^2}{ESR_{DC}mass}$, † Maximum Specific Power= $\frac{V_{max}^2}{4ESR_{1kHz}mass}$ and, ‡ Maximum Specific Energy = $\frac{0.5CV_{max}^2}{3600mass}$. Unit of each variable used calculation is V_{max} in V, C in F, ESR_{DC} and ESR_{1kHz} in mΩ and $mass$ in kg. Some parameters are not available and are marked as N/A since the required parameters used in the calculation are not specified in the manufacturer datasheets (e.g. weight, volume, ESR_{DC}, ESR_{1kHz}, etc.)

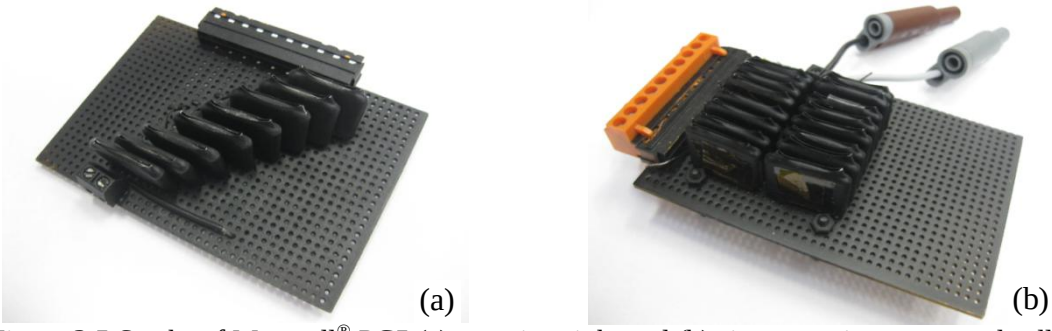
3.3 Supercapacitor Stack Construction

SC voltages per unit cell are very small (e.g. 1-2.7V) and are series-connected as a stack to achieve a useful working voltage level found in many applications. To assemble several discrete SC cells into a module, it is preferable to use identical SC cells to reduce the unbalanced cell voltage problem. This unbalanced cell voltage problem still occurs, however, and proposed solutions are discussed in Chapter 5.

There were 2 Maxwell® SC stacks assembled manually in the lab. These are:

- PC5 Stack I: A stack of eight series-connected Maxwell® PC5 SCs presented in Figure 3.5 (a). It has equivalent capacitance of 0.5F at 20V
- PC5 Stack II: A stack of sixteen series-parallel connected Maxwell® PC5 SCs presented in Figure 3.5 (b). It has equivalent capacitance of 1F at 20V

The PC5 Stack I (0.5F 20V) and the PC5 Stack II (1F 20V) were assembled such that their stack capacitances and stack voltages are comparable to the nineteen-cell stack supercapattery (0.7F 19V) presented in the previous section. The stacks were painted black for the purpose of thermal image inspection.



(a) (b)

Figure 3.5 Stacks of Maxwell® PC5 (a) contains eight and (b) sixteen series-connected cells

To recap, each stack specification is summarized in Table 3.2.

Table 3.2 Manually assembling SC stack specifications

Stack	*C* (F)	*ESR* @DC (mΩ)	Rated current (A)	Rated voltage (V)
PC5 Stack I	0.5	3200	1	20
PC5 Stack II	1	1600	2	20

3.4 Experimental Rigs

Three rigs were used to characterize the SCs in this work. These are a switched-mode converter with an analog Hysteresis current control (Rig I), a six-channel interleaved switched-mode converter with a digital PI current control (Rig II) and a commercial linear current regulator (Rig III).

3.4.1 Rig I: A Switched-mode Power Converter with an Analog Hysteresis Current Controller

To perform the CPC mode for the SC round-trip efficiency evaluation and the PCC mode for the SC parameter identification, a low-power prototype converter was designed and implemented as shown in Figure 3.6 and Figure 3.7. It consists of a controller unit, a bi-directional half-bridge DC-DC converter, a protection circuit and the Maxwell® PC5 stack I. The controller unit contains a Hysteresis current control board, an Infineon® microcontroller starter kit XC164CM V2.0, an analog-to-digital (ADC) and digital-to-analog (DAC) board, and a CPLD logic controller board. Since the PC5 stack I was constructed from eight series-connected PC5 SCs, voltage discrepancies build up. To avoid cell over-voltage, a protection circuit is fitted such that both the cell voltage and the total stack voltage can be monitored all the time.

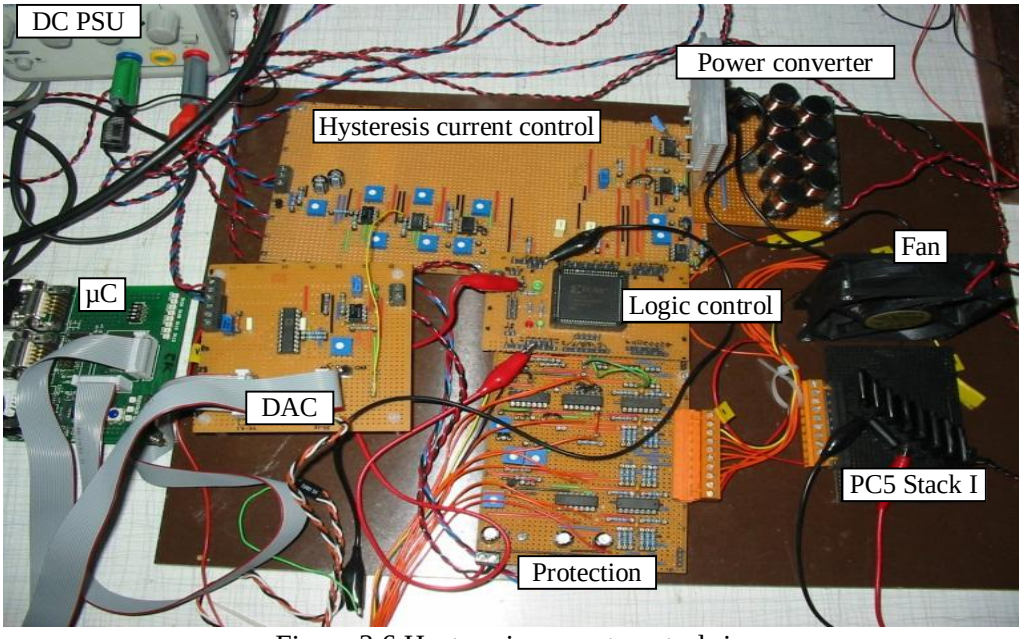


Figure 3.6 Hysteresis current control rig

The control block diagram and the schematic diagram of the automatic charge-discharge cycling system are presented in Figure 3.7. In this rig, the operating modes, which are the PCC, the CCC and the CPC modes, can be selected from the program stored inside the microcontroller.

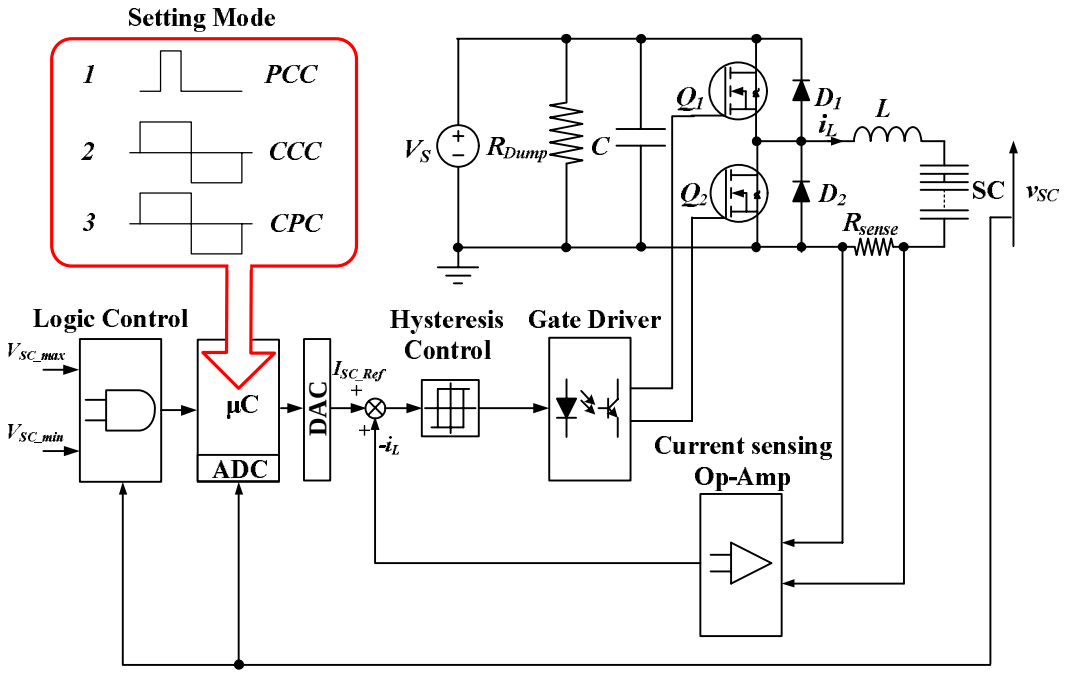


Figure 3.7 Rig I control block diagram

In the PCC and the CCC modes, only the current control is required, so the current feedback loop alone is sufficient to operate the system. In the CPC mode, a voltage feedback loop is also required in addition to the current control loop for imposing a constant power.

In the current control loop, an inductor current signal, i_L, is measured by using a 50mΩ current shunt resistor, R_{sense}. The shunt resistor current information is passed through the LF411 current sensing op-amp, which has gain-bandwidth of 4MHz. The gain is selected to be 20 and the bandwidth is limited to 200kHz since increasing gain beyond this level will results in the system noise amplification. In addition, in the current feedback loop, an analog active low-pass filter is used to limit the signal frequency up to 36kHz by using 20kΩ and 220pF. This filter setting is sufficient for limiting the high-frequency noise higher than the switching frequency, which is ≈10kHz. At i_L = 1A to 6A current, the LF411 senses 50 to 300mV and outputs 1 to 6V, which is sufficient for the next stage signal processing. During the experiment, a current offset problem occurs due to the LF411 output voltage offset and this offset

affects the charge-discharge current control. To minimize this offset problem, the offset is adjusted externally by a variable resistor before conducting the experiments. The current signal is further fed to a Hysteresis controller and follows the current reference, i_{SC_Ref}, output from the DAC unit. The LM311 comparator is used to implement the Hysteresis function.

For the voltage feedback loop, the SC voltage signal, v_{SC}, is only used to limit the SCs stack voltage between the minimum SC operating voltage, V_{SC_min}, and the maximum SC operating voltage, V_{SC_max}. This voltage limitation is controlled by the LM339 comparators on the logic board. When the v_{SC} reaches one of the limits, the logic board will send a signal to force the system to toggle from one state (i.e. charging) to the complementary one (i.e. discharging). The voltage signal is measured directly (non-isolate) and is scaled to 5V for interfacing with the µC ADC unit purpose. The voltage signal is also filtered by RC low-pass filter with cut-off frequency at ≈20-30Hz before fed to the comparators. This low cut-off frequency is acceptable for the voltage measurement since the voltage signal is only used for calculating the current reference from the constant power. The v_{SC} is read via the 10-bit ADC unit of the microcontroller and is used with a constant power Look-up Table algorithm (LUT) to output the i_{SC_Ref} to the Hysteresis current control board via the 12-bit ANALOG DAC312 DAC unit. With 10-bit ADC, the voltage measurement resolution is $20V/(2^9-1) \approx 39mV$ as one bit is reserved for a sign bit.

3.4.2 Rig II: A Six-channel Interleaved Switched-mode Power Converter with a Digital PI Current Controller

This rig was built for evaluating high power SCs (i.e. higher voltage and current rated SCs) that cannot be achieved with Rig I. The rig employs an interleaved converter configuration (i.e. paralleling several identical converters), so this rig can provide a high output current with low ripple current and high dynamic profile (i.e. fast slew rate) to the SCs. This rig is shown in Figure 3.8 and the schematic and control diagrams are shown in Figure 3.9 and Figure 3.10. Rig II can be used either as an SC charger or an SC emulator. Further information about the SC emulator work will be presented in Chapter 6.

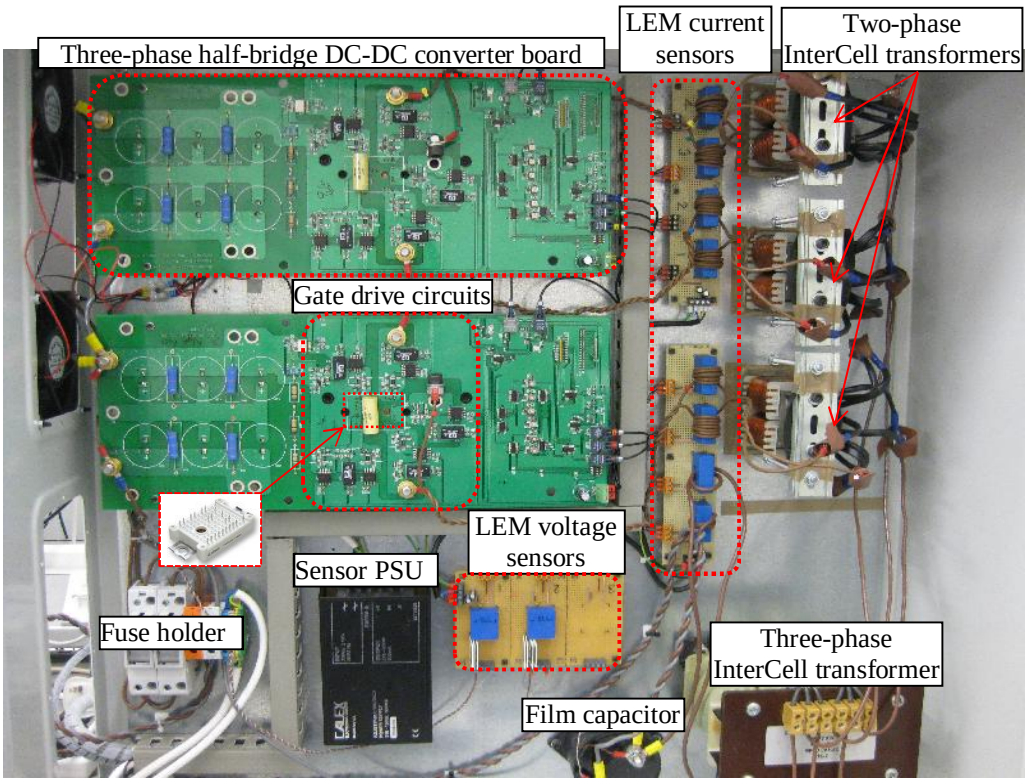


Figure 3.8 The SC charger/emulator system built from six interleaved parallel DC-DC converters

From Figure 3.8, the rig consists of:

- The three-phase bi-directional half-bridge DC-DC converter boards
- The Hall-effect LEM® current and voltage sensors and their sensor PSU
- The two-phase InterCell transformers and the three-phase InterCell transformer (The InterCell description will be presented in Chapter 6.)
- A high voltage film capacitor and the fuses and fuse holders

On the converter board there are 6 gate-driver circuits for driving the Infineon® FS30R06W1E3 IGBT power module, which contains three-phase bi-directional half-bridge DC-DC converters rated at 600V 30A.

For the sensors, the Hall-effect LEM® LA-55P current sensors and the Hall-effect LEM® LV-25P voltage sensors were used. The sensor specifications are shown in Table 3.3.

Table 3.3 The LEM LA-55P current sensor and the LEM LV25-P voltage sensor specifications

Specification	LA-55P	LV25-P
Linearity error	< 0.15%	< 0.2%
Offset	±0.2mA	±0.15mV
Accuracy	0.9% at rated value	0.8% at rated value
Response time	< 1μs	40μs
Rated Primary current	50A	10mA
Conversion ratio	1:1000	2500:1000

From Table 3.3, both sensor types have small linearity error and offset error. Therefore, both voltage and current sensors were calibrated through a Ballatine® 1620A transconductance and a Datron® model 4705 multifunction calibrator, respectively. The Ballatine® machine is a precision current source, which outputs an accurate current level according to the input voltage fed from the Datron® machine. By performing the calibration, the nonlinearity error and the offset from the sensor gain is minimized, which in turn reduces the unbalanced current flowing through each interleaved DC-DC converter.

The SC charger/emulator system schematic diagram is presented in Figure 3.9. In Figure 3.9, the channel currents, i_{CH1}-i_{CH6} are measured through the Hall-effect LEM current sensors while the v_{SC} and V_S are measured through the Hall-effect LEM voltage sensors. Both current and voltage signals are converted digitally by the FPGA ADC unit (Figure 3.11) and the information is sent to the DSP.

The SC charger/emulator control block diagram is presented in Figure 3.10. Both current and voltage information (i_{CH1}-i_{CH6}, V_S, and v_{SC}) are used in the control algorithm according to the selected operating mode (e.g. the PCC, the CCC and the CPC modes), which is stored in the DSP. The modulation indexes, M_1-M_6, are calculated inside the DSP, and they are converted to the PWM signals by the PWM generators inside the FPGA. The FPGA and DSP digital platform is presented in Figure 3.11, which shows the FPGA and the DSP boards, FPGA ADC units, FPGA PWM output ports and a DSP daughter card. Note that a DSP daughter card is used for changing operating mode and updating control parameters between the DSP board and the PC online.

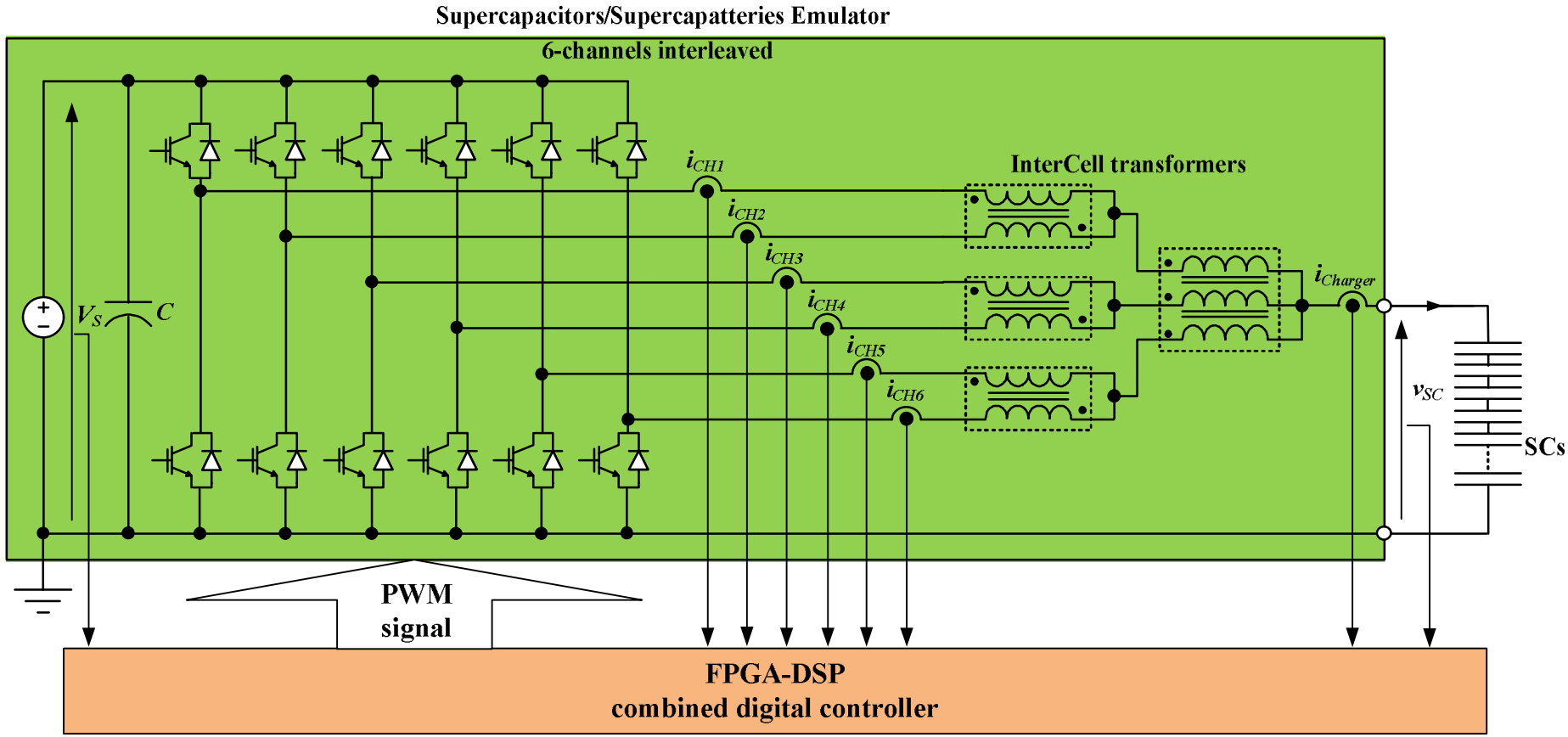


Figure 3.9 The SC charger/emulator system schematic diagram

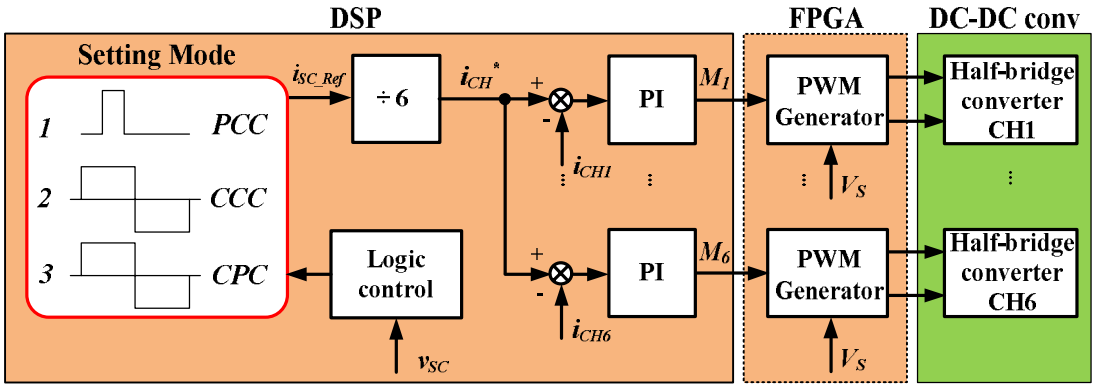


Figure 3.10 Control block diagram for the SC charger/emulator system (Rig II)

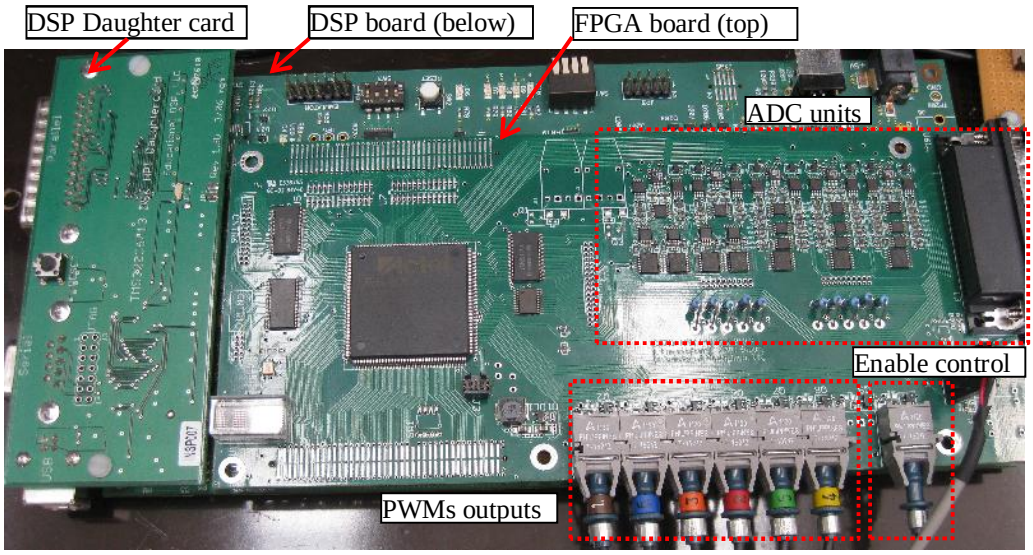


Figure 3.11 FPGA-DSP Digital control platform

One of the reasons that a combined FPGA-DSP digital platform was used is the DSP board does not have an ADC unit. In addition, unlike the microcontroller, the Texas Instruments TMS320C6713 DSP starter board does not have PWM generator units (e.g. Capture and Compare (CAPCOM) unit like in the Infineon microcontroller). Therefore, the FPGA board is also used for PWM signal generation for controlling the six-channel interleaved converter. With the FPGA assistance, the DSP processing time is reduced, which allows resource for programming complex tasks (e.g. supercapattery emulation).

From Figure 3.11, only 6 PWM signals generated from the FPGA board are used to control 6 half-bridge converter legs (i.e. one signal per leg). This is done to reduce a number of the PWM signal output ports from the FPGA board. The 6 PWM signals sent from the FPGA are fed into the deadtime generator circuitry on the DC-DC converter, so 12 gate signals for the upper and the lower switches are generated complementarily from a single PWM signal. Note that the deadtime is adjusted to be 1μs.

The charger/emulator cabinet (Figure 3.8) is used as the emulator. A duplicated system is built for the charger function (Figure 3.12). It is wise to put the emulator into the cabinet, and leave the charger system as an experimental rig as it is easy to change and adjust current and voltage measurement range of the system sensors when the rig is on an experiment table. To control the two separate systems, two FPGA-DSP digital control platforms and two PCs are required as shown in Figure 3.13.

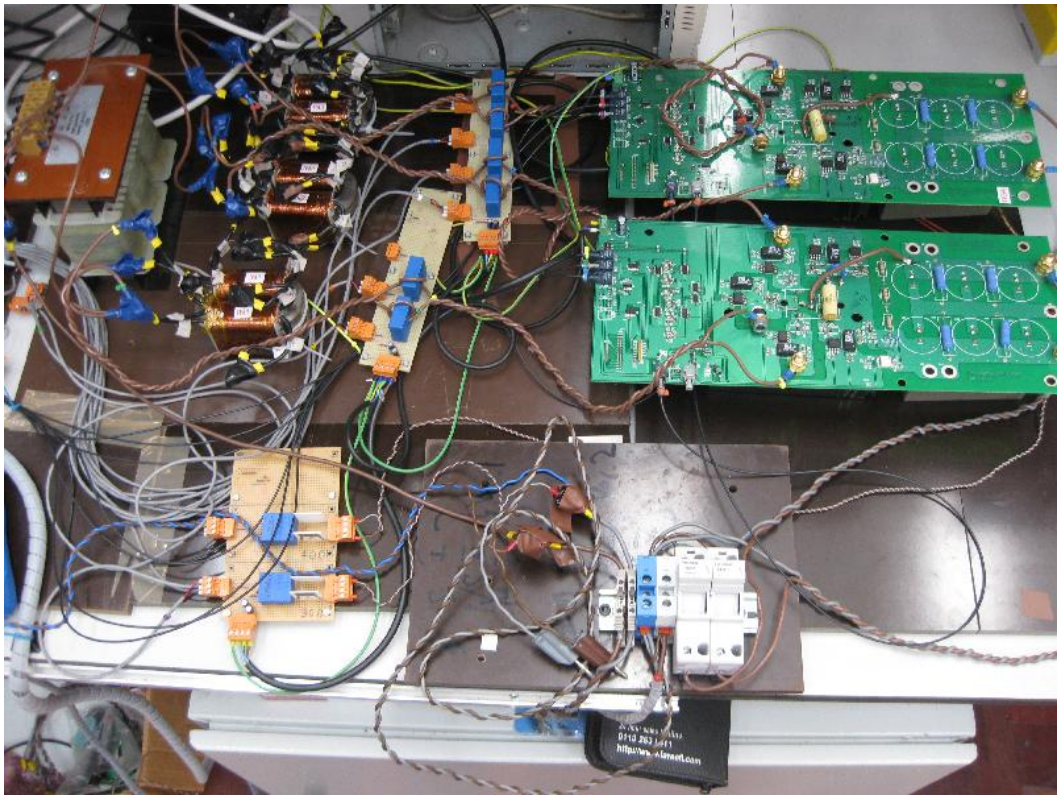


Figure 3.12 The SC charger system based on the same configuration as the emulator

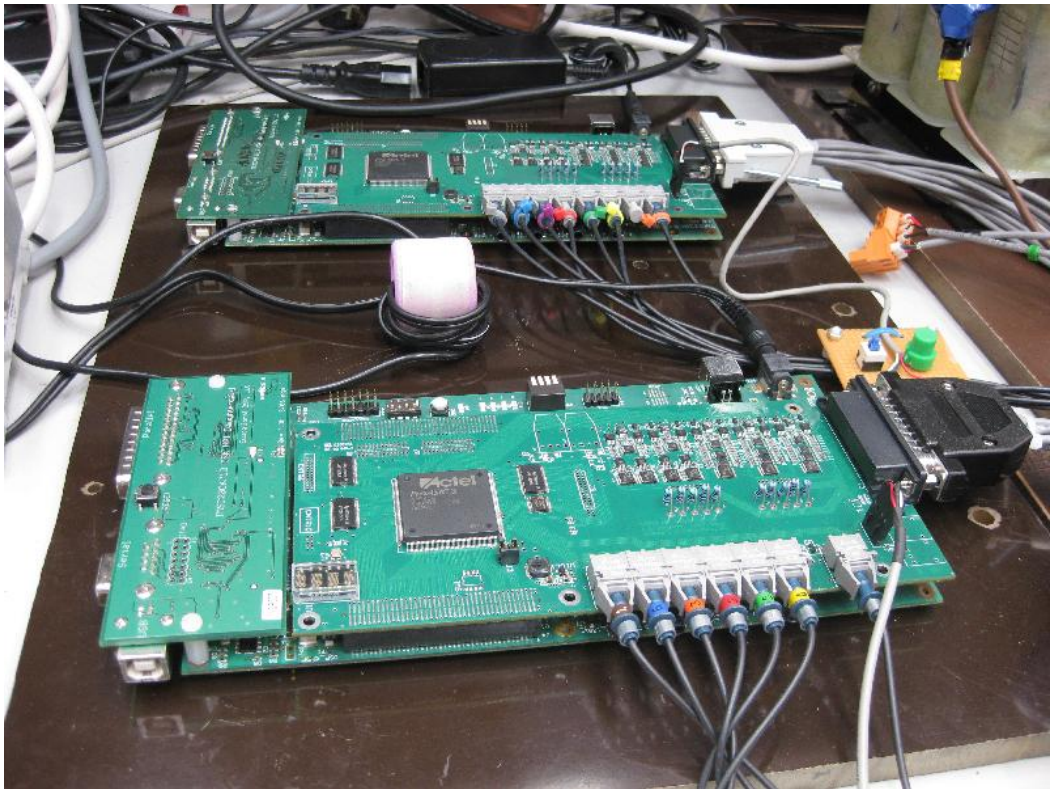


Figure 3.13 Double FGPA-DSP digital control platforms for the SC charger and the emulator systems

3.4.3 Rig III: Commercial Linear Current Regulator

Two commercial linear current regulators were used in this study, which are AUTOLAB® and Bio-Logic SAS as shown in Figure 3.14 and Figure 3.15.

(a) (b)

Figure 3.14 AUTOLAB® machines (a) potentiostat/galvanostat PGSTAT302N (b) current booster 10A

(a) (b)

Figure 3.15 Bio-Logic SAS machines (a) potentiostat/galvanostat/EIS SP-150 (b) current booster 20A VMP3 module

These commercial linear current regulators are controlled by desktop PCs using software from their manufacturers (e.g. AUTOLAB® with NOVA software and Bio-Logic SAS with EC-lab software). The equipment employs a linear current regulator to achieve high slew rate and low ripple current, which is essential for the EIS testing, particularly in the high frequency region (i.e. 1-10kHz range). The regulators are equipped with high-precision current and voltage sensors (e.g. 16 bits ADC sampling at a range of 10kHz or below), which are crucial for the EIS method where the applied sinusoidal voltage peak-to-peak is very small (e.g. 10mV). These specifications make the SC pre-conditioning process easy because the regulators can control and hold the SC voltage precisely both in terms of magnitude and time

duration. The measurement accuracy and resolution of both machines are shown in Table 3.4. Additionally, since both are based on linear current regulator technology, they can perform the PCC method with a sharp rising current (i.e. high slew rate), which may not be achievable from the switched-mode power converter. Unfortunately, Rig III was not available when the device was in healthy condition, so the PCC method was performed by Rig I.

Table 3.4 The measurement accuracy and resolution of AUTOLAB and Bio-Logic machines

Specification	AUTOLAB with 10A Booster	Bio-Logic with 20A Booster
Voltage accuracy	±0.2% FSR	< 0.1% FSR
Voltage resolution	0.3μV minimum	5-300μV (5μV on 200 mV and 300μV on 20V)
Voltage limit	±10V	±10V or 0-20V
Current accuracy	±0.5% FSR	< 0.1% FSR
Current resolution	0.0003% FSR	0.004% FSR

In the School of Chemical Engineering of the Faculty of Engineer at the University of Nottingham, the supercapattery was prototyped. The AUTOLAB regulator was used to perform the EIS method on the supercapattery device. The AUTOLAB® potentiostat/galvanostat PGSTAT302N and the current booster 10A are presented in Figure 3.14 (a) and Figure 3.14 (b). The machine applied voltage is limited to 5V initially, which can be scaled up to 30V with a potential divider circuit. Only the EIS function is used in this machine.

On the other hand, the Bio-Logic SAS machine was used to characterize the Maxwell® SCs, particularly the high capacitance SC stacks. The Bio-Logic potentiostat/galvanostat/EIS SP-150 and the current booster 20A VMP3 module are shown in Figure 3.15. The machine with its booster can provide +/-20A and +/-20V to the DUT. Another advantage of the Bio-Logic machine is it can perform a sequence of either same or different testing techniques (e.g. EIS, PCC, CCC, CPC and so on), which reduces supervisory time dramatically.

In summary, there are 3 rigs used in the SC characterization, and their advantages and disadvantages, possible operating modes are listed in Table 3.5.

Table 3.5 Comparison of three SC charger rigs

Specification	Rig I	Rig II	Rig III
Ripple current and voltage	Small ☺	Small ☺	Very small ☺
Overshoot current	Small ☺	Small ☺	Very small ☺
Current response time	Fast ☺	Fast ☺	Very fast ☺
Processing power	Low ☹ (only useful for evaluate laboratory prototypes)	High ☹	Low ☺ (limited by processing current and voltage but useful for lab testing)
Accuracy	High ☺	Acceptable ☺	Very high ☺
Current offset problem	Small ☺	High ☹	Very small ☺
Energy loss	Low ☺	Low ☺	High ☹
Additional benefit	No load plant transfer function require (good for fast prototyping) ☺	Utilize conventional DC-DC interface converter structure for SCs ☺	Able to record long-run experimental results via the PC ☺
Possible operating mode	PCC, CCC and CPC	PCC, CCC and CPC	EIS, PCC, CCC, CV and CPC

3.5 The SC Characterizing Processes

To improve the consistency of the experimental results, several SC characterizing processes are proposed and are described in this section. The characterization processes are a combination of methods presented in Section 2.5. The techniques summarized from the SC standard testing presented at the end of Section 2.2 are also applied and are included in these processes. The processes are divided into 3, which are used to:

- identify model parameters representing SC short-term characteristic (Section 3.5.1).
- identify model parameters representing SC long-term characteristic (Section 3.5.2).
- evaluate the SC round-trip efficiency (Section 3.5.3).

3.5.1 Process to Identify Parameters Representing SC Short-term Characteristics

To investigate SC short-term characteristic and to obtain the SC parameters, the EIS, the PCC and the CV methods are combined as the process shown in Figure 3.16. The SC is short-circuited for 24 hours or more before commencing the test. The process starts with the EIS sub-process of Figure 3.17, which is used to inspect the cell characteristic and its health. The Z_{SC} information is recorded and used later in the model parameter identification process presented in Section 2.5.1.1. After finishing the EIS sub-process, the SC cell is subjected to the large-signal pulse current test, which is in the PCC sub-process of Figure 3.18. The voltage-time information before and after applying the pulse current is recorded for the model parameter identification process of Section 2.5.1.4. At the end of the process, the EIS sub-process can be repeated again optionally to check the condition of the cell and to inspect any SC characteristic change due to the large-signal testing.

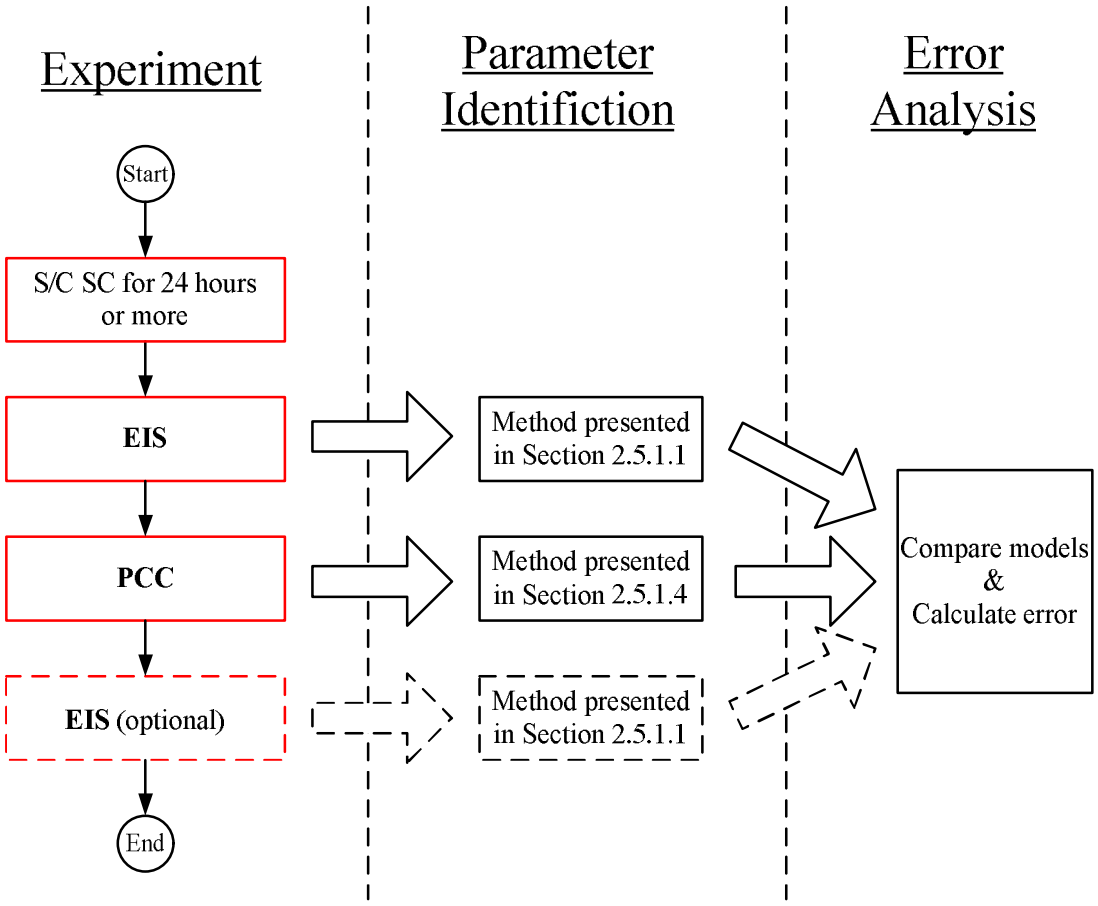


Figure 3.16 Process to identify parameters representing SC short-term characteristic

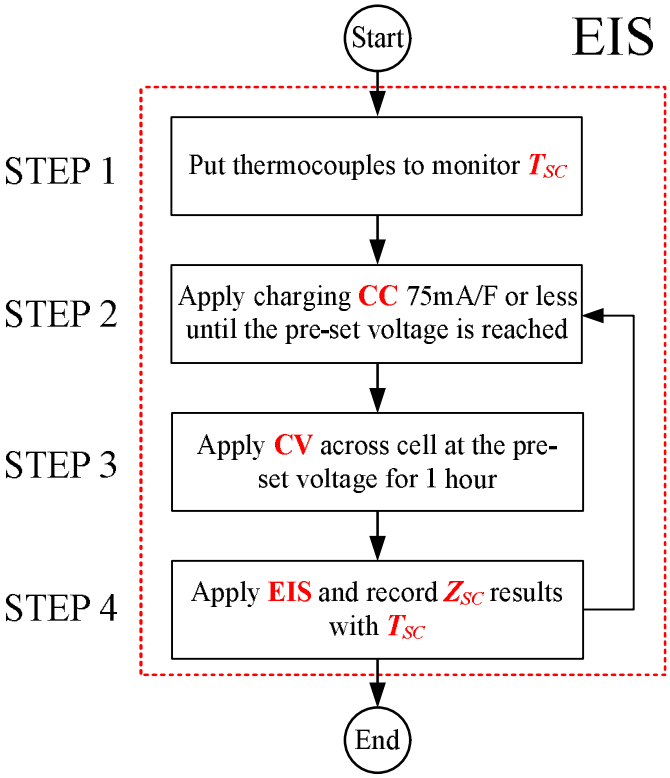


Figure 3.17 The EIS sub-process used in Figure 3.16

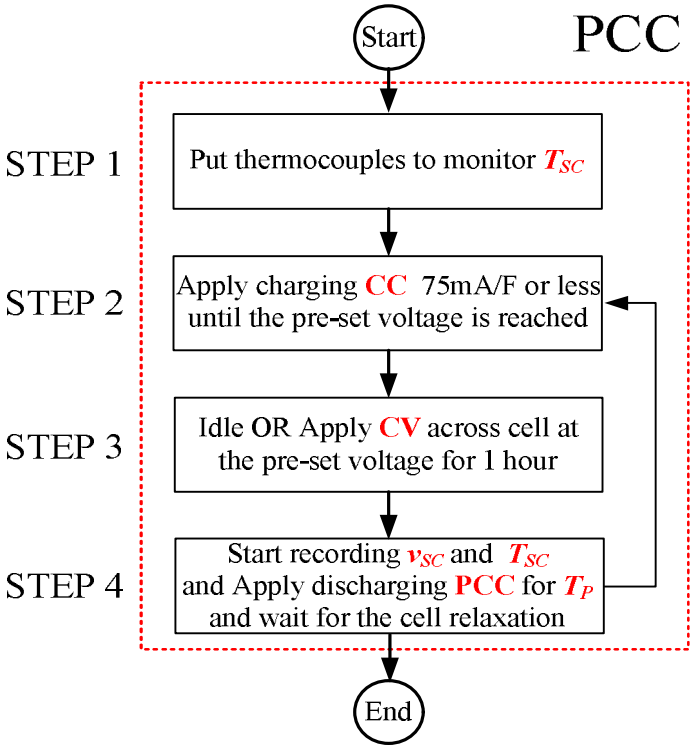


Figure 3.18 The PCC sub-process used in Figure 3.16

Figure 3.17 and Figure 3.18 describe the details of the EIS and the PCC sub-processes. In STEP 1 of both sub-processes, thermocouples are installed on the cell to monitor the SC cell temperature, T_{SC}, before and after commencing the test. In STEP 2, the cell is charged with the CC method at a rate of 75mA/F or less to change the DC-bias voltage. During this period, T_{SC} is observed to ensure that T_{SC} is slightly changed since changing in operating temperature affects some SC parameters as discussed in Section 2.3. In STEP 3, the CV method is applied to hold the cell voltage. The voltage holding period is set to 1 hour to ensure that the cell has reached the steady-state condition and the charges fairly distributed. In testing small capacitance cells, the 1 hour period may be reduced. Finally, in STEP 4, the EIS or PCC methods are applied. Note that in STEP4 of the PCC sub-process, the v_{SC} recording is started before applying the PCC. If more DC-bias voltage points are required, STEP2 to STEP4 are repeated.

For the EIS method in the Figure 3.17, only AUTOLAB and Bio-Logic machines (Rig III) can be used. For the PCC method, all rigs can be used. Since Rig III can perform both the EIS and the PCC methods, it is convenient to use Rig III to do both. However, the current limitation of Rig III is 20A, so the higher PCC testing is done with Rig II.

3.5.2 Process to Identify SC Parameters Representing SC Long-term Characteristics

According to Section 2.5.1.5, there are two terms used to represent the SC energy retention characteristic; these are the *SDVC* and the I_{Leak}. Both terms are determined through the CV process as described in Figure 3.19. However, different sub-processes are used for determining each term. The sub-processes used in the *SDVC* and the I_{Leak} are the CV-I and the CV-II respectively as described in Figure 3.20 and Figure 3.21.

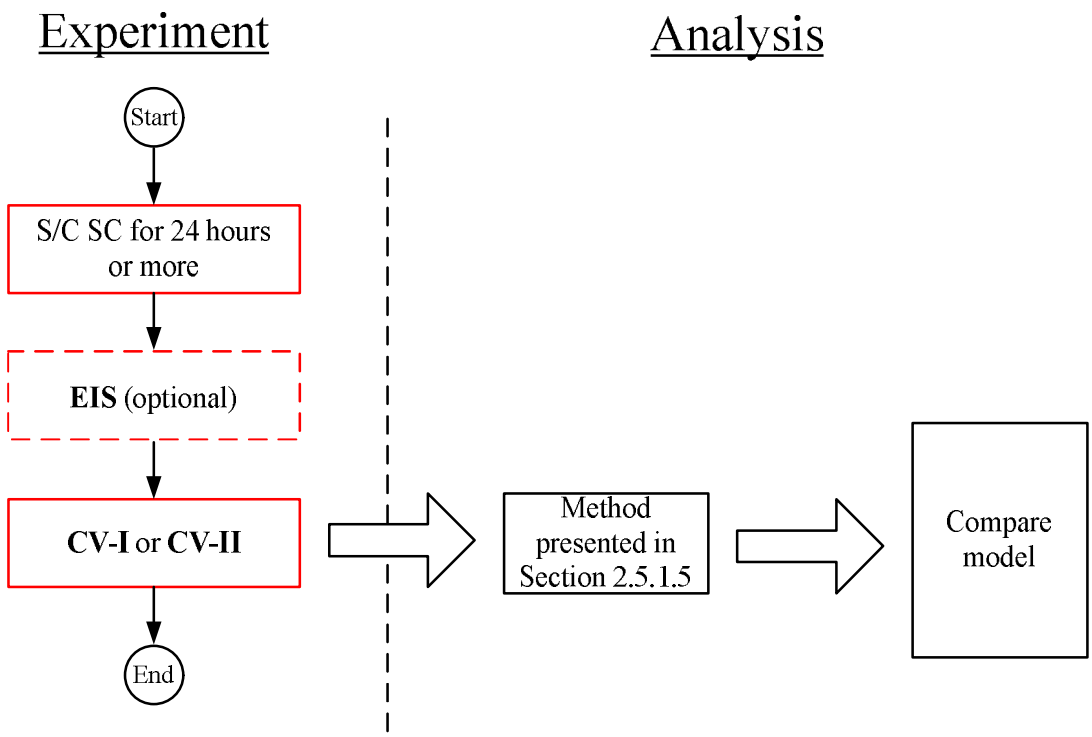


Figure 3.19 Process to identify parameters representing SC long-term characteristic

From Figure 3.19, the SC is short-circuited for 24 hours or more before commencing the test. Before starting the CV sub-process, the EIS sub-process (Figure 3.17), can be applied optionally to inspect the SC cell characteristic and its health. Then either the CV-I (Figure 3.20) or CV-II (Figure 3.21) sub-processes are chosen. The obtained experimental results are analyzed with the method presented in Section 2.5.1.5 and the derived *EPR* parameters from different CV method are compared.

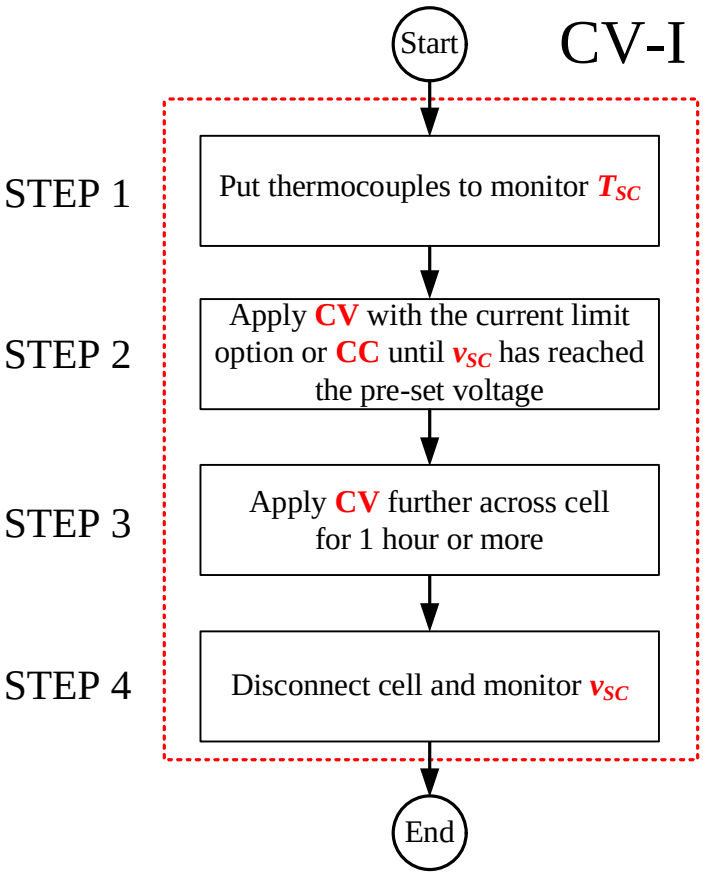


Figure 3.20 The CV-I sub-process used in Figure 3.19

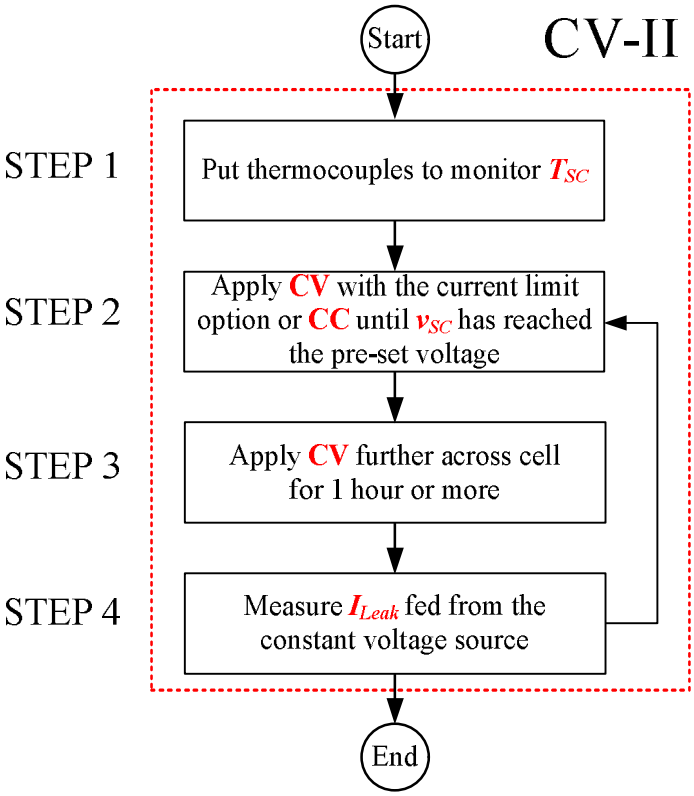


Figure 3.21 The CV-II sub-process used in Figure 3.19

Figure 3.20 and Figure 3.21 describe the details of the CV-I and the CV-II sub-processes. In STEP 1, for both CV sub-processes, thermocouples are installed on the cell to monitor the T_{SC} before and after commencing the test. In STEP 2, the cell is charged with the CV method with the current limit condition, which is done either by connecting a shunt resistor externally or internally by the CV PSU to change the DC-bias voltage. The pre-set voltage depends on the point of interest and is usually varied from 50% to 100% of the rated SC voltage. During this period, the T_{SC} is observed carefully to ensure that the T_{SC} is slightly changed. The duration of the applied CV in STEP 2 may be varied due to the chosen shunt resistor value ($\approx 100\Omega$ or less). In STEP 3, the CV method is applied further for 1 hour or more to ensure that the SC cell has reached steady-state condition. Finally, in STEP 4 of the CV-I sub-process, the SC cell is disconnected and connected to the voltage measurement data logger. The data logger can start earlier at STEP 2 if the SC voltage-time characteristic is of interest. The data logging duration is varied with SC capacity. In this study, the *SVDC* information is monitored between 50% and 100% of the rated SC voltage.

On the other hand, in STEP 4 of the CV-II sub-process, the amount of current fed from the CV PSU (i.e. I_{Leak}), which maintains the SC voltage, is recorded. If more DC-bias voltage points are needed, STEPs 2-4 are repeated.

3.5.3 Process to Evaluate SC Round-trip Efficiency

According to Section 2.5.2.4, to investigate SC round-trip efficiency, the EIS, the CPC and the CV methods are combined as the process presented in Figure 3.22.

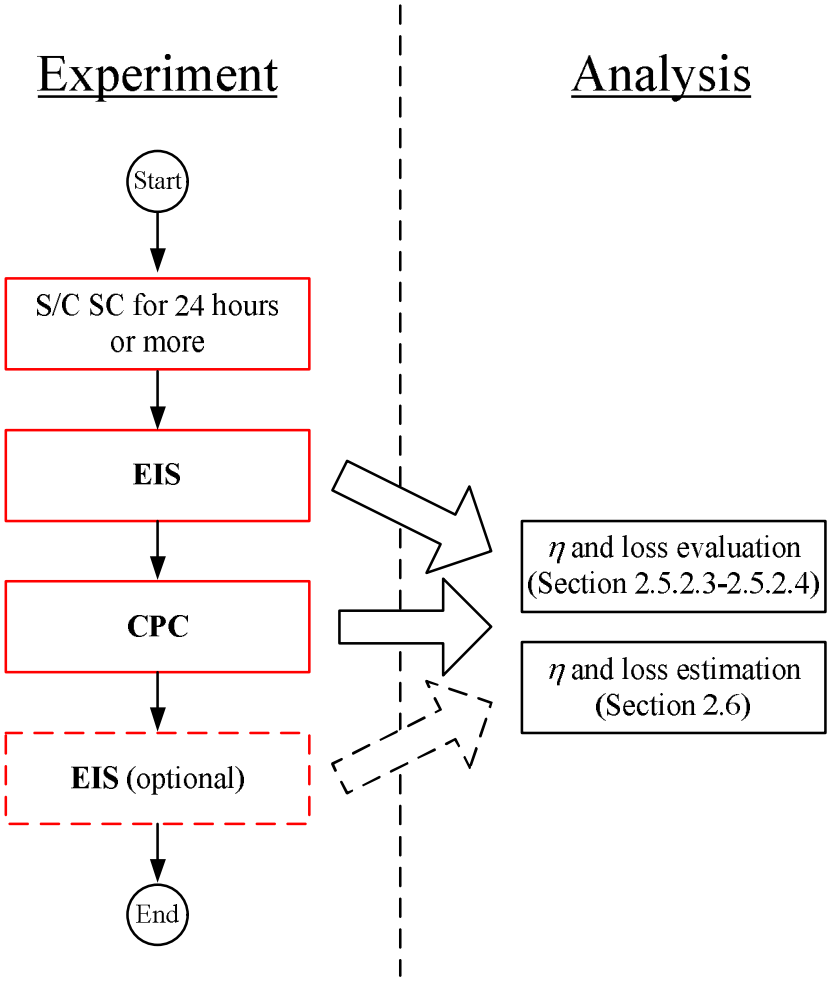


Figure 3.22 Combined methods for evaluating SC round-trip efficiency

Referring to Figure 3.22, again the SC is short-circuited for 24 hours or more before commencing the test. Then, the process starts with the EIS sub-process (Figure 3.17) as usual, which is used to inspect the cell characteristic and its health. The Z_{SC} information is recorded and is used later in the SC round-trip efficiency and energy loss estimation presented in Section 2.6. After finishing the EIS sub-process, the SC cell is subjected to the large-signal test, which is in the CPC sub-process of Figure 3.23.

At the end of the process, the EIS sub-process can be repeated again to check the condition of the cell and to inspect any change due to the large-signal testing.

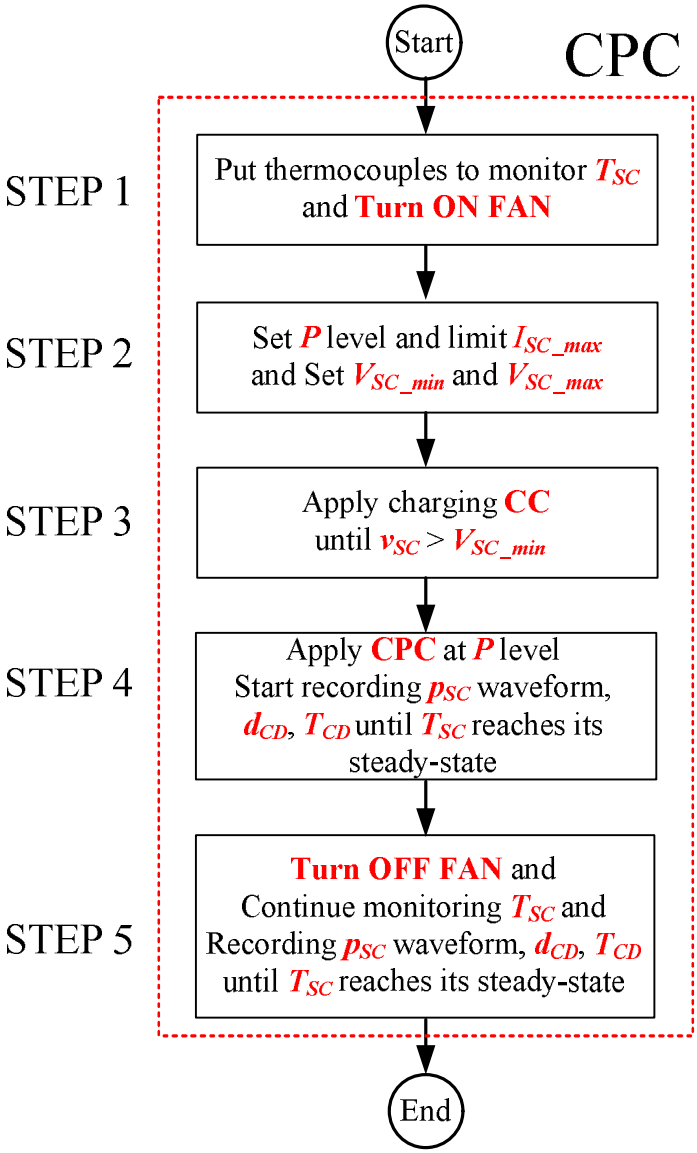


Figure 3.23 The CPC sub-process used in Figure 3.22

Referring to Figure 3.23, the CPC sub-process is started with the SC cell thermocouple positioning. Also in STEP 1, the fan is turned on before applying the CPC test. Thus, T_{SC} due to the heat generated from the CPC test is kept below the rated SC operating temperature. In STEP 2, a constant power level, P, a maximum SC current, I_{SC_max}, and the voltage limits, V_{SC_min} and V_{SC_max}, are set before commencing the CPC test. The I_{SC_max} is calculated from P/V_{SC_min} such that the operating current is limited below the rated current. In STEP 3, the cell is charged with the CC method at the level below I_{SC_max} until v_{SC} is greater than V_{SC_min}. Then, in STEP 4, the operating mode is changed from the CC to the CPC with the pre-set P level. It is important that the p_{SC}, d_{CD} and T_{CD} information is recorded immediately after the CPC method has started (i.e. capturing the first CPC information) as the

heat generated during initialization will affect the T_{SC} and SC characteristic. The CPC method with forced-cooling continues until T_{SC} has reached its steady-state level (e.g. 1 hour). In STEP 5, the fan is turned off, and T_{SC} is monitored together with the measurement of same parameters as in STEP 4 until T_{SC} has reached the new steady-state level (e.g. 1 hour).

3.6 Conclusion

In this chapter, a description of the SC tests (the Maxwell® SC, the ELIT SC and the supercapattery devices) are presented and discussed. These devices are chosen since they are built based on different electrode coating technology (i.e. activated carbon and carbon nanotube) and different electrolytes (i.e. organic and aqueous). The Maxwell® PC5 SCs are assembled as a stack, which has the specification similar to the supercapattery stack, so both the Maxwell SC stack and the supercapattery performance can be compared.

The detail of three different experimental rigs are described and presented together with their possible operating modes. The advantages and disadvantages of each rig are discussed.

Three SC characterization processes have been presented. These processes have included the techniques to improve consistency of the experimental results presented in Section 2.2. These processes are used to obtain the experimental results presented in the next chapter.

Chapter 4 Experimental Results

4.1 Introduction

In this chapter, experimental results from tests on the Maxwell® PC5 SC and the supercapattery stack I (19 cells) are presented. The results of experiments for deriving both the SC short-term and long-term characteristics are presented and discussed in Section 4.2. The results for evaluating the SC round-trip efficiency and energy loss are presented and discussed in Section 4.3. In Section 4.4, the SC round-trip and energy loss estimation methods presented in Section 2.6 are compared to the experimental results of Section 4.3.

The results for the Maxwell® BMOD0052 stack, ELIT SC stack and the supercapattery stack II (3 cells) have also been taken, but for reasons of space and readability, they are not included in the main text. They are included in Appendix B.

4.2 Experimental Results for Deriving the SC Characteristics

The electrochemical impedance spectroscopy method (EIS) and the pulse constant current (PCC) method are used in SC short-term model characterization. Since the EIS is a well-known method and is considered as non-destructive (i.e. small signal), the EIS method is applied to all SC devices to study their impedance-frequency characteristics. The experimental results are presented in Section 4.2.1. The model identification method presented in Section 2.5.1.1 is applied and the model parameters are derived and are presented in Section 4.2.2.

Meanwhile, the PCC method is used as an alternative approach to the EIS method. The PCC method is selected for some devices only, and the experimental results are presented in Section 4.2.3. The model identification method presented in Section 2.5.1.4 is applied, and the model parameters are presented within the same section.

In addition, to improve the consistency of the experimental results between the PCC method and the EIS method, the process presented in Section 3.5.1 is employed, and the comparison between the models derived from both methods are presented and discussed in Section 4.2.4.

At the end of this section, the SC long-term characteristic is studied experimentally by employing the CV method. The experimental results are presented in Section 4.2.5, which show the comparison of energy retention performance of different SCs.

4.2.1 SC Characterization Results Using the Electrochemical Impedance Spectroscopy (EIS) Method

The EIS experimental results are obtained by using Rig III with either the AUTOLAB® machine with NOVA software or the Bio-Logic machine with EC-Lab® software. As discussed in Section 2.5.1.1, the 10mV sinusoidal voltage signal is used in the EIS methods applied to all devices under test (DUTs).

4.2.1.1 The Maxwell® PC5 SC

Firstly, the EIS method is applied to a single cell of the Maxwell PC5 SC to study its impedance-frequency characteristic. The EIS testing condition is zero-bias voltage and frequency sweep is from 10mHz to 1kHz. If the simple RC model is assumed, the impedance result can be presented as *C* and *ESR* versus frequency as shown in Figure 4.1 and Figure 4.2. The EIS method with the same setting condition is also applied to the stack of eight series-connected and 16 series-parallel connected PC5 cells. These are included in Figure 4.1 and Figure 4.2.

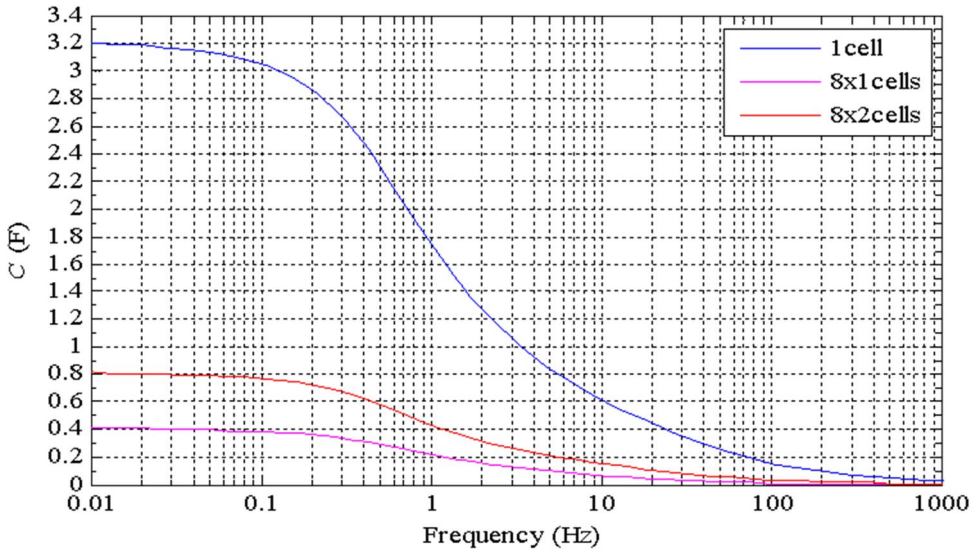


Figure 4.1 Equivalent capacitance versus frequency range 10mHz to 1kHz of Maxwell® PC5 as a single cell, stacks of eight series-connected cells and sixteen series-parallel connected cells at zero-bias voltage

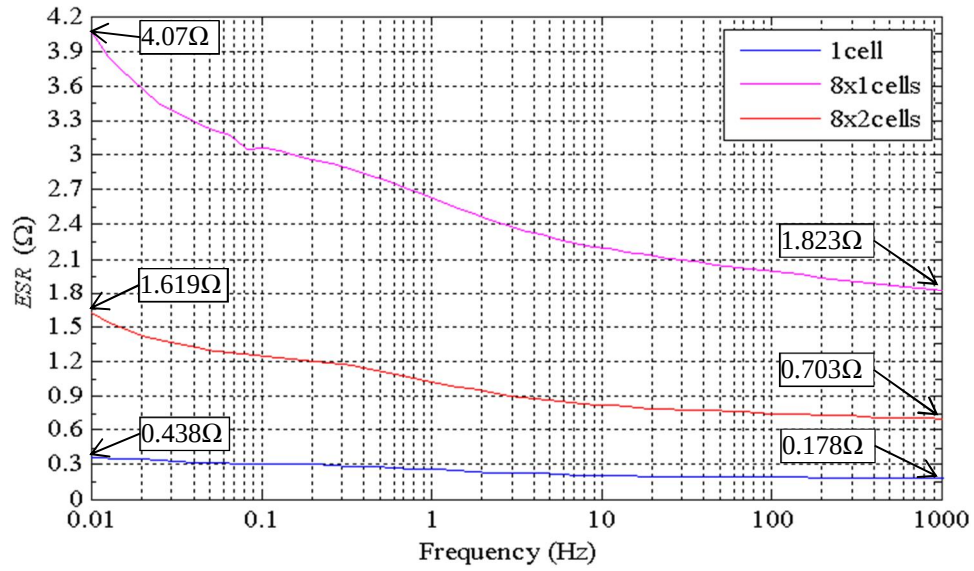


Figure 4.2 Equivalent series resistance versus frequency range 10mHz to 1kHz of Maxwell® PC5 as a single cell, stacks of eight series-connected cells and sixteen series-parallel connected cells at zero-bias voltage

Referring to Figure 4.1, the capacitance of the Maxwell® PC5 single cell at the lowest frequency (10mHz) is 3.2F, which is lower than the rated value specified in the datasheet (4F) [89]. Also the capacitances of the assembled stacks at 10mHz are 0.4F and 0.8F, which are less than the calculated values of 0.5F and 1F. Allowing for a ±20% capacitance tolerance as specified in the datasheet [89], the impedance results are reasonable. This capacitance tolerance is not from the manufacturing process as the stack results also indicate a similar conclusion. As the frequency increases, the capacitances reduce towards 0 at 1kHz.

From Figure 4.2, the ESR-frequency characteristics are presented. For the single Maxwell® PC5 cell, the *ESR* at 10mHz is 0.438Ω, which is higher than the rated value specified in the datasheet (0.4Ω@DC). Meanwhile, the *ESR* at 1kHz is 0.178Ω, which is lower the rated (0.29Ω@1kHz). However, allowing for a ±25% in resistance tolerance as specified in the datasheet [89], the measured resistance is acceptable. The discrepancy between the measured and rated values at low and high frequencies may be due to the different testing temperature condition and extra resistance from the lead cables. From the test result, it was shown that the information specified in the device datasheet can be used as a guideline only, so all devices should be analyzed before use in the application.

Next, the EIS method is applied to the Maxwell® PC5 stack II (8x2 cells) but this time with DC bias voltages of 2V, 4V, 5V, 10V and 15V. The impedance at zero-bias voltage is also included for comparison. Since this SC is intended to be used in the low frequency range (i.e. charge-discharge period between 1s to 10s), the maximum testing frequency is reduced to 100Hz. The experimental results are presented in Figure 4.3 and Figure 4.4.

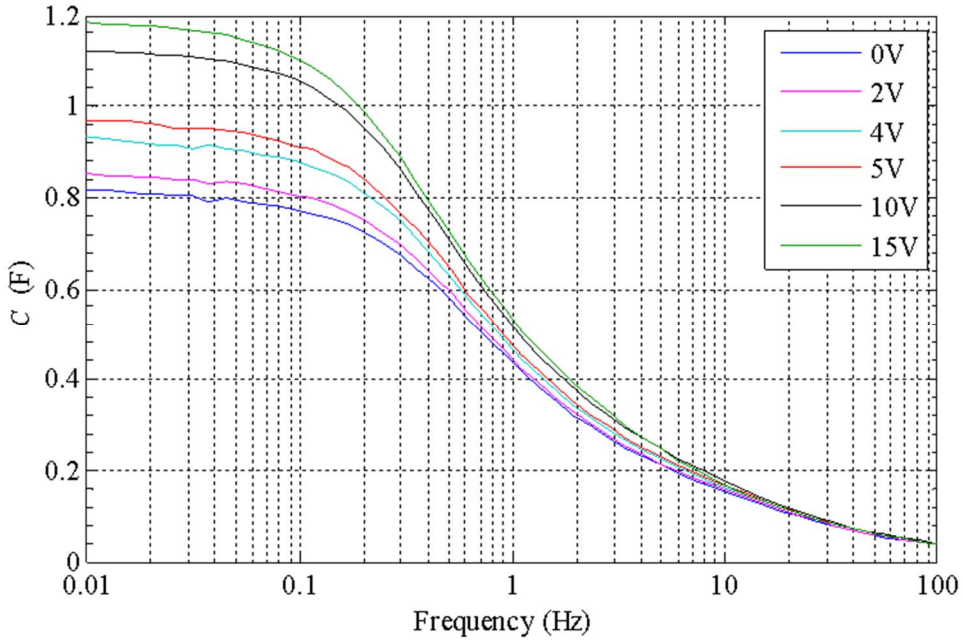


Figure 4.3 Equivalent capacitance versus frequency range 10mHz to 100Hz of the Maxwell® PC5 stack II (8x2 cells) at the applied voltage of 0V, 2V, 4V, 5V, 10V and 15V

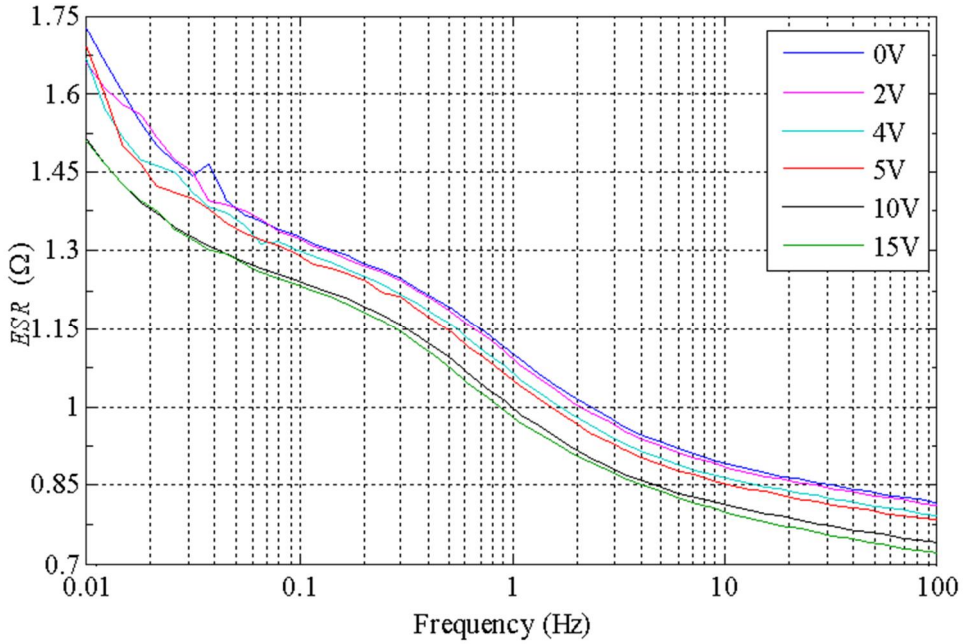


Figure 4.4 Equivalent series resistor versus frequency range 10mHz to 100Hz of Maxwell® PC5 II (8x2 cells) at the applied voltage of 0V, 2V, 4V, 5V, 10V and 15V

From Figure 4.3, the capacitance at the low frequency clearly depends on the applied DC-bias voltage. At 10mHz, the capacitance is increased as the applied DC-bias voltage increases. The 10mHz capacitance values are re-plotted against the applied DC-bias voltages as shown in Figure 4.5. Considering a nominal capacitance of 1F (4F×2/8 = 1F), the calculated values are within ±20% of 1F (i.e. between 0.8F and 1.2F), which matches with the information specified in the datasheet [89]. One can predict from the graph in Figure 4.5, that if the DC-bias voltage is increased to rated (i.e. 20V), the capacitance-voltage curve will reach ≈1.3F. Figure 4.5 shows that the capacitance-voltage relationship is close to linear.

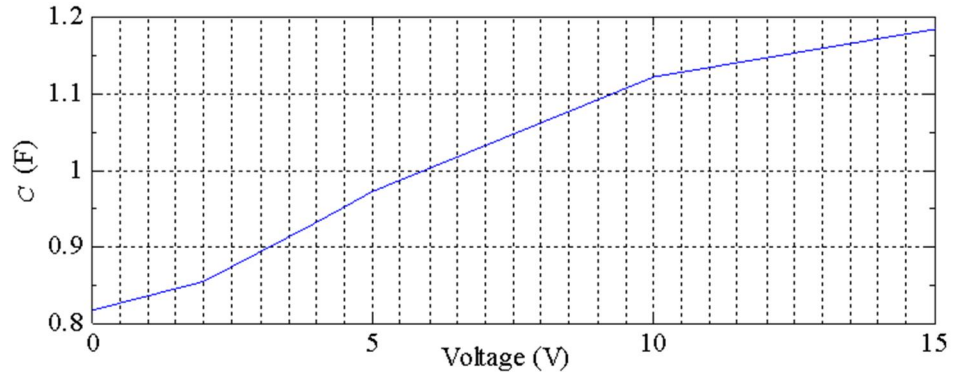


Figure 4.5 Equivalent capacitance versus DC-bias voltage of the Maxwell® PC5 stack II (8x2 cells) at 10mHz

It is also seen that the *ESR* is reduced when the applied DC-bias voltage increases. As shown in Figure 4.6, the *ESR* is reduced by ≈14% at 10mHz and 16% at 100Hz

when the DC-bias is increased from 0V to 15V. Figure 4.6 also shows that the resistance-voltage relationship is close to linear for both 10mHz and 100Hz conditions.

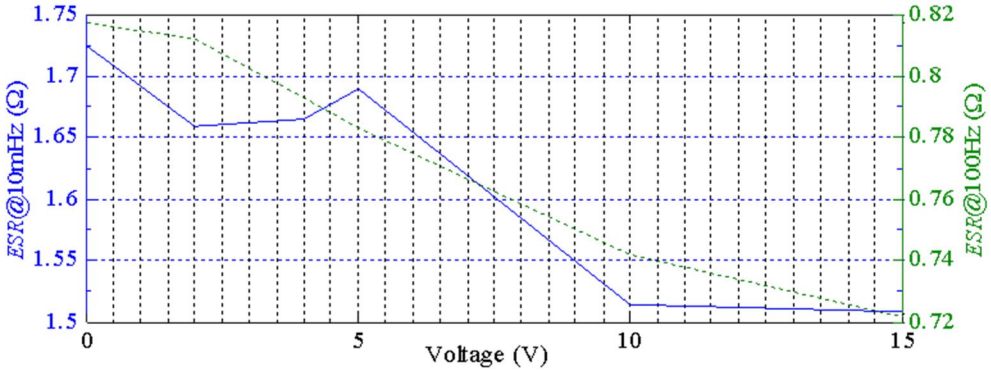


Figure 4.6 Equivalent series resistance versus DC-bias voltage of the Maxwell® PC5 stack II (8x2 cells) at 10mHz and 100Hz

4.2.1.2 The Supercapattery Stack I (Nineteen-cell Stack)

The EIS method with the same frequency sweep setting is applied to the supercapattery nineteen-cell stack with DC-bias voltages of 2.5V, 5V, 10V, and 15V. Again, the impedance result at zero-bias voltage is also included for comparison. The experimental results based on the simple RC model are presented in Figure 4.7 and Figure 4.8.

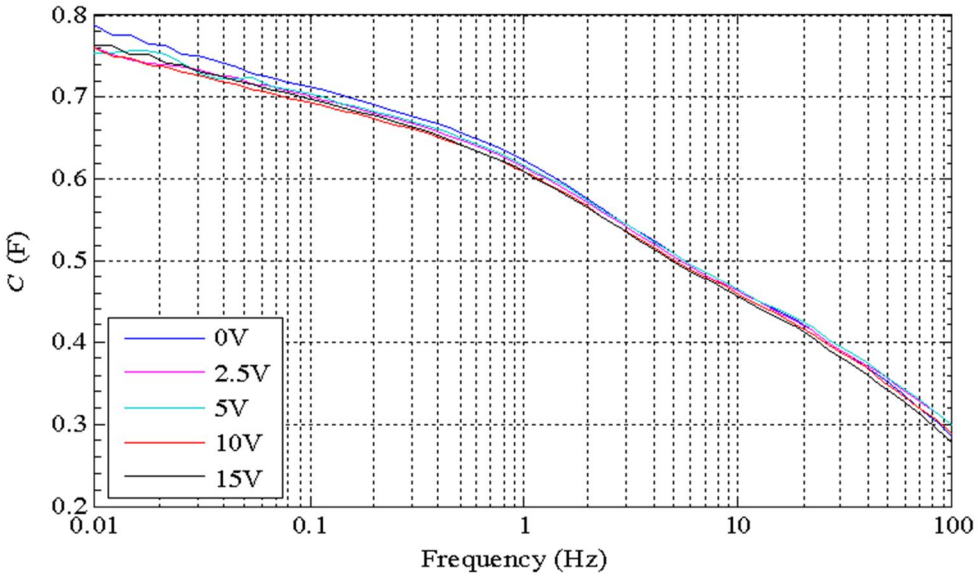


Figure 4.7 Equivalent capacitance versus frequency range 10mHz to 100Hz of the nineteen-cell supercapattery stack at the applied voltages of 0V, 2.5V, 5V, 10V and 15V

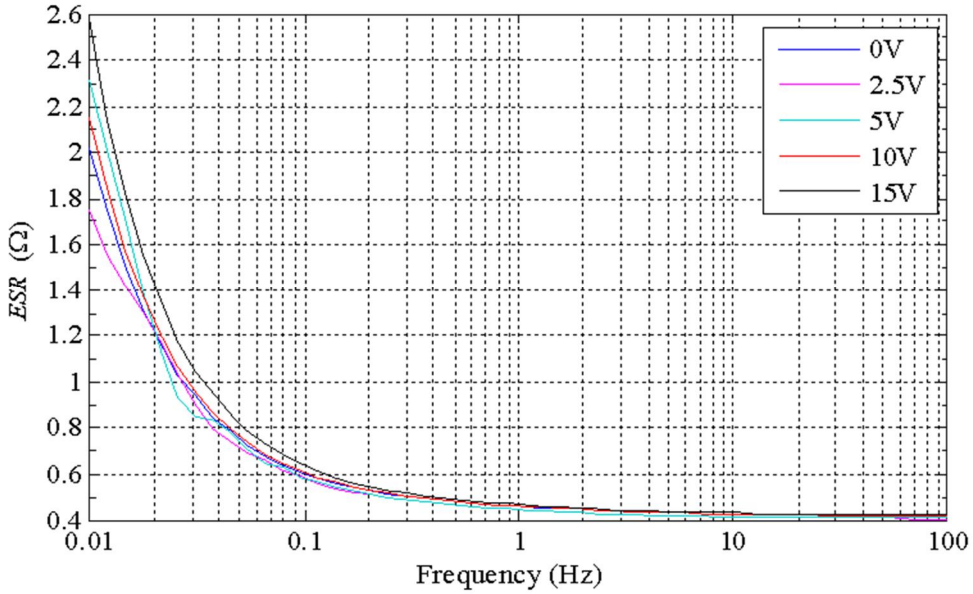


Figure 4.8 Equivalent series resistor versus frequency range 10mHz to 100Hz of the supercapattery nineteen-cell stack at the applied voltage of 0V, 2.5V, 5V, 10V and 15V

From Figure 4.7, the capacitance at 10mHz decreases as the DC-bias voltage increases. However, as the frequency reduces further (e.g. 1mHz), the capacitance projection is expected to reach approximately 1F. The capacitances at 10mHz are re-plotted against the applied DC-bias voltages as shown in Figure 4.9.

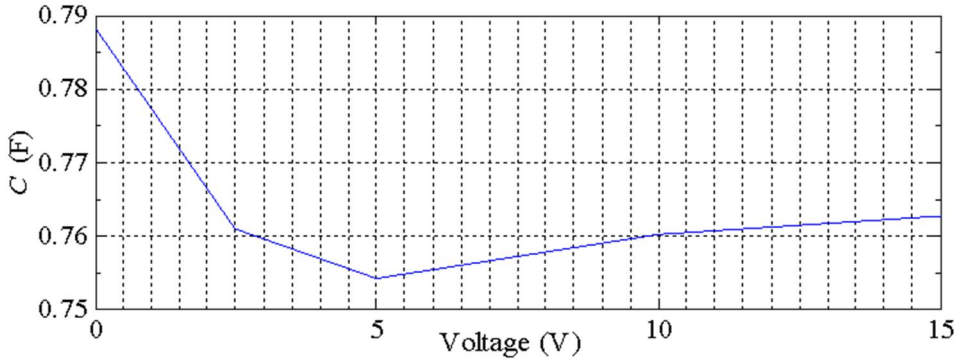


Figure 4.9 Equivalent capacitance versus DC-bias voltage of the supercapattery nineteen-cell stack at 10mHz

From Figure 4.9, the capacitance is changed by max 5% over the 15V DC-bias sweep, and the average value is 0.775F, which is less than the rated value specified by the School of Chemical Engineering (Table 3.1). From Figure 4.8, the *ESR* is increased when the DC-bias voltage increases. The *ESR*s at 10mHz and 100Hz are changed by max 35% and 4% respectively when the DC-bias is increased from 0V to 15V as shown in Figure 4.10. At 10mHz, the DC-bias voltage has a reverse effect on the supercapattery *ESR* (i.e. increasing the DC-bias voltage will increase the *ESR*)

when compared with the Maxwell SCs (i.e. increasing the DC-bias voltage will reduce the *ESR*).

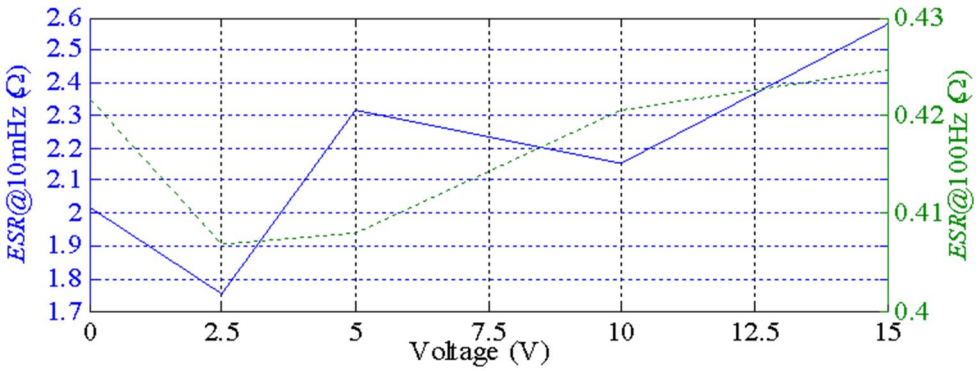


Figure 4.10 Equivalent series resistance versus DC-bias voltage of the supercapattery nineteen-cell stack at 10mHz and 100Hz

4.2.1.3 Summary of the EIS Experimental Results

The experimental impedance-frequency-voltage characteristics of several devices presented in terms of *ESR* and *C* are summarized in the Table 4.1.

Table 4.1 Summarize figure numbers of *C* and *ESR* of each device

Device	Parameters	
	C	*ESR*
Maxwell® PC5 single cell	Increase as bias voltage increases	Decrease as bias voltage increases
Maxwell®PC5 Stack I (8×1)		
Maxwell®PC5 Stack II (8×2)		
Maxwell® BMOD0052 P015 (Module)		
Supercapattery stack II (three-cell stack)	Decrease as bias voltage increases	Increase as bias voltage increases
Supercapattery stack I (nineteen-cell stack)		
ELIT		

For the Maxwell SCs, at zero-bias voltage condition, the results show that the derived *C* at 10mHz are lower than the values specified at DC in the datasheet. If DC-bias voltage is applied, the full frequency range *C* is increased for all frequencies with the 10mHz values are spanning ±20% of the rated values. The effect of the DC-bias voltage also affects the *ESR* over all frequencies. The 10mHz and the 100Hz *ESR*s are chosen to represent the low and the high frequency *ESR*s. Both *ESR*s at zero-bias voltage condition are slightly different from the datasheet, but they are within ±25% tolerance range. As the DC-bias increases, both *ESR*s fall below that of the zero-bias voltage values. Considering the effect of the applied DC-bias voltage,

the relationship between the *ESR* and the *C* parameters and the DC-bias voltage is almost linear.

For the supercapattery stacks, the experimental results are presented for the stack I and the stack II (Appendix B). The experimental results show that the DC-bias voltage has different effects on the *ESR* and *C* of stack I and stack II. Considering the stack I: when the DC-bias is increased, the full frequency range *ESR* increases but the full frequency range *C* decreases. Again the 10mHz and the 100Hz *ESRs* are chosen to represent the low and the high frequency *ESR*s. The results show that as the DC-bias increases from 0 to 15V, the 10mHz *ESR* is increased by 35% while the 100Hz *ESR* is increased by only 4%. The capacitance at 10mHz decrease by 5% over 15V swept bias voltage. For the supercapattery stack II, when the DC-bias is increased from 0 to 3V, the 10mHz ESR is increased by 5% while the 1kHz *ESR* is decreased by 8%. The *C* for this stack seems to have high sensitivity to the DC-bias change, changing by 16% over the 0-3V bias voltage condition.

The EIS method has also applied to the large capacitance SC stacks from the Maxwell BMOD and the ELIT (Appendix B). The Maxwell BMOD stack shows similar results to the Maxwell PC5 stack, and the ELIT stack shows similar results to the supercapattery stack I. However, the Maxwell BMOD result also shows a resonant frequency in the low frequency range at 200Hz, which does not occurr in the small capacitance stacks. This result is used in calculating the stray inductance within the module: 12nH for C = 52F. For the ELIT result, the result cannot be used to determine the stray inductance since the actual device stray inductance is overwhelmed by the lead cable stray inductance.

The results presented in this section provide an insight into the device impedance at low and high frequency at different applied DC-bias voltage level and gives an idea how to utilize the device in the optimized way. In the next section, the EIS experimental results presented in this section will be used in the model identification method to obtain the model parameters.

4.2.2 Model Parameters from the EIS Results

In this section, the EIS experimental results of the Maxwell PC5 stack II, the supercapattery stack I (Section 4.2.1) are used with the model identification method proposed in Section 2.5.1.1. The model parameters obtained in this section will be compared and evaluated with the PCC method later in Section 4.2.3. The model identification method is also used with the supercapattery stack II, and the results are included in Appendix B.

There are three statistical definitions considered in this study to justify goodness of fitting between the experimental results and the model. They are sum-of-square error (*SSE*), R-square (or written as R^2), and root-mean-square error (*RMSE*), which can be calculated by:

$$SSE = \sum_{i=1}^{n_p} \left(x_{EST\_i} - x_{EXP\_i} \right)^2 \tag{4.1}$$

$$R^2 = 1 - \frac{SSE}{\sum_{i=1}^{n_p} \left(x_{EST\_i} - \bar{x}_{EXP} \right)^2} \tag{4.2}$$

$$RMSE = \sqrt{\frac{SSE}{n_p}} \tag{4.3}$$

where n_p is number of experimental data points, x_{EST} and x_{EXP} are estimated and experimental data points, and $\bar{x}_{EXP}$ is a mean value of experimental data.

However, from (4.1), the *SSE* parameter depends on both the actual error and number of experimental data points used in the fitting algorithm. A small *SSE* can be due to a small number of experimental data points, but it does not always mean good fitting (i.e. least error achievement). Therefore, the *SSE* is only used in calculating the R^2 and the *RMSE* as defined in (4.2) and (4.3). The parameters R^2 and the *RMSE* will be used to justify good fitting in this study. The closer R^2 to 1 and the lower the *RMSE* indicate better fitting.

4.2.2.1 The Maxwell PC5 Stack II (8x2)

The EIS experimental results at 0V, 5V and 10V DC-bias voltages are selected and are re-plotted as Nyquist plot as shown in Figure 4.11.

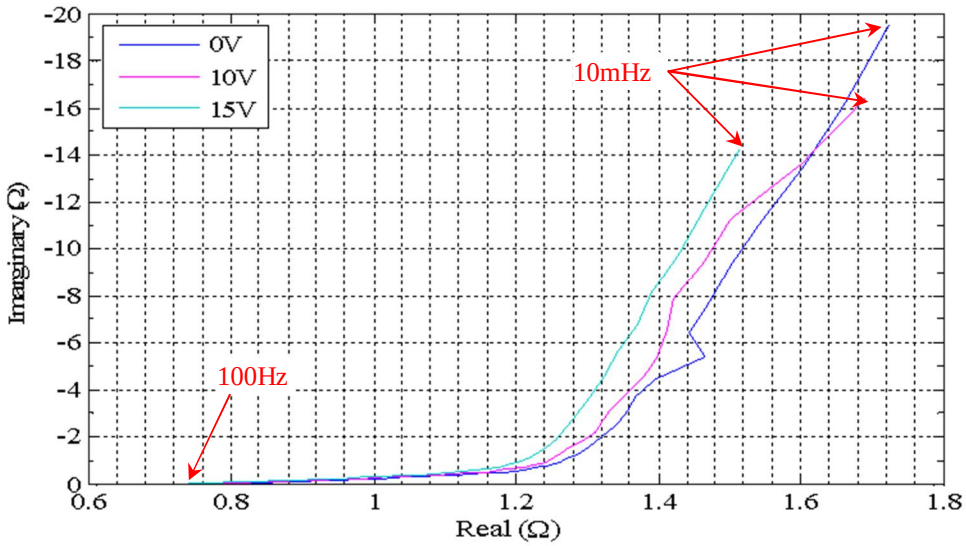


Figure 4.11 Imaginary versus real components of the complex impedance of the Maxwell® PC5 SC stack II at zero-bias, 10V and 15V DC-bias voltages

First, the measured complex impedance at zero-bias voltage is fed to the Gauss–Newton algorithm presented in Section 2.5.1.1, which is designed to fit the impedance of model IV presented here again as Figure 4.12.

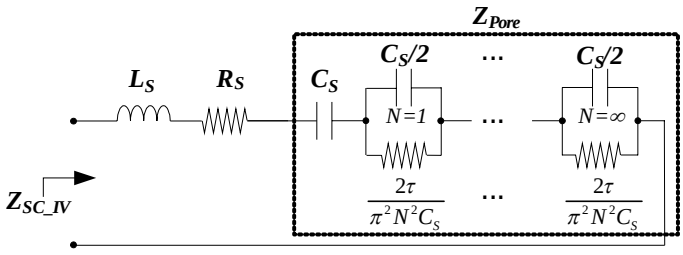


Figure 4.12 Model IV: The *N* series-parallel RC model with an added inductance

However, since the impedance results had been obtained up to 100Hz, the SC positive imaginary information is missing and the L_S parameter cannot be calculated. The L_S parameter is selected to minimum as 20nH, which is typical for SC and its purpose is just to complete the equivalent circuit. The L_S value is only affected the imaginary term at the high frequency range (i.e. >1kHz), so this parameter does not affect the overall fitting parameters involving the imaginary term. The fitting algorithm selects the R_S from the real term of the impedance at the highest frequency

point available from the experimental result (i.e. 100Hz). The fitting algorithm yields C and τ as shown in Table 4.2.

Table 4.2 Model IV parameters derived from the zero-bias voltage EIS experimental result of Maxwell® PC5 stack

N	R_S (Ω)	L_S (nH)	C_S (F)	τ	Real *RMSE* (10^{-3})	Imaginary *RMSE* (10^{-3})	Real R^2 (max=1)	Imaginary R^2 (max=1)
3	0.8174	20	0.8125	1.7124	90.2	49.9	0.875	0.9998
30	0.8174	20	0.8121	1.4073	104.3	47.3	0.8326	0.9998

From Table 4.2, two different parallel RC-branch numbers, N, of model IV are investigated. In the first case, only 3 branches are used in modeling the SC complex pore impedance, Z_{Pore}, while in the second case, 30 branches are used. The calculated impedances from both equivalent circuits are presented and compared with the measured impedance (denoted as "EXP") in Figure 4.13.

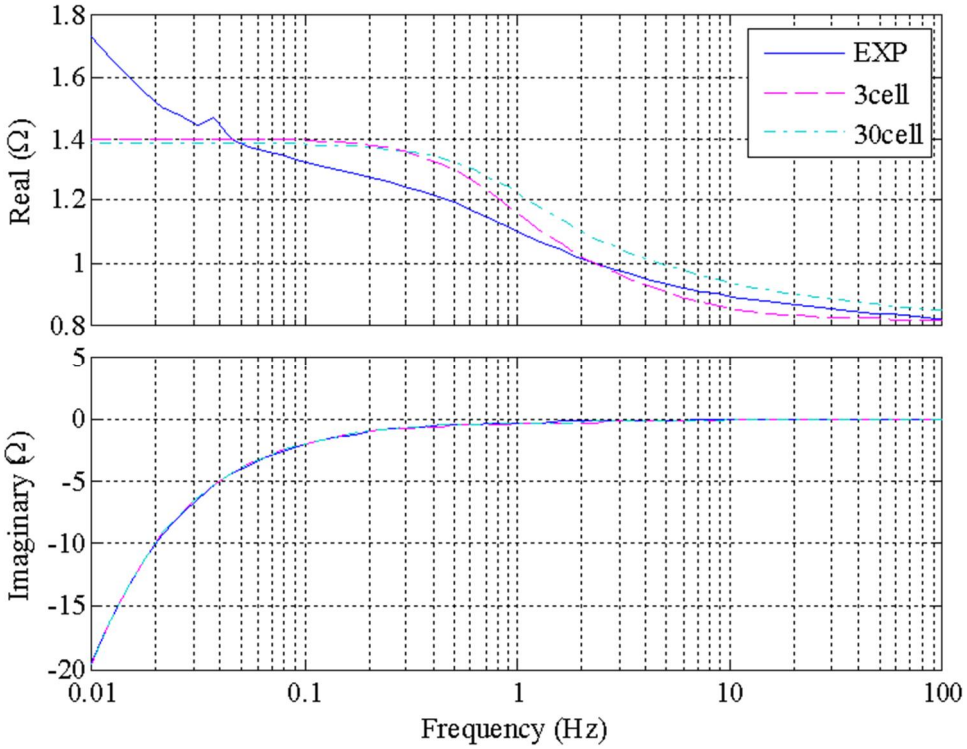


Figure 4.13 Real and imaginary impedance terms versus frequency of the zero-bias voltage measured and model IV (3 cells and 30 cells) of the Maxwell® PC5 stack II

From Table 4.2, the 3-RC parallel branch circuit impedance fits the measurement with an accuracy similar to that of the 30-RC parallel branch circuit, which reveals the sufficiency of the three-cell circuit. However, both impedances obtained on the basis of the model shown in Figure 4.12 do not quite fit the real term of the measured

impedance, particularly at very low frequencies (i.e. below 1Hz). The real impedance below 1Hz is interesting for CPC operation since the CPC charge-discharge period is usually more than a second (<1Hz).

To improve the impedance modeling accuracy at the frequency range below 1Hz, an additional RC parallel branch impedance, Z_{add}, with a larger time constant than the time constants of Z_{Pore} is included as proposed in the author's paper [35]. This is model IV_2, and it is presented here again as Figure 4.14.

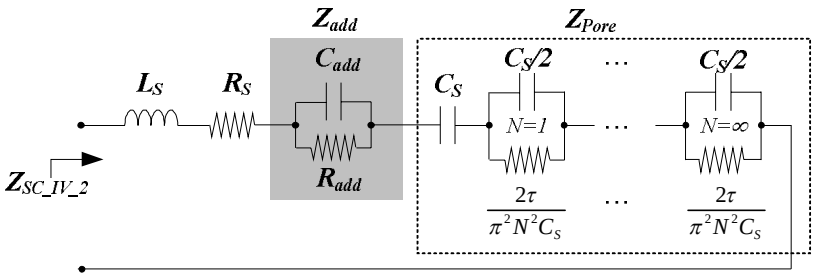


Figure 4.14 Model IV_2: The *N* series-parallel RC model with an additional RC branch

The Gauss–Newton algorithm is used again to identify model IV_2 circuit parameters from the same experimental result. The model parameters are given in Table 4.3. The measured and estimated impedances are compared as shown in Figure 4.15 and Figure 4.16. It is clear that both the calculated real and imaginary parts of model IV_2 are in excellent agreement with the measured values.

From Table 4.3, the R_{add} and C_{add} are chosen by in order to minimize the real and the imaginary *RMSE* and increasing real R^2. The R_{add} and C_{add} can be identified accurately by applying additional Gauss-Newton algorithm separately from that of the Z_{Pore} parameter identification. The improved fitting algorithm becomes more complicated, however, the result is improved slightly as R^2 is getting closer to 1. In addition, the fitting improvement may not represent actual SC characteristic since the impedance information at the low frequency region (i.e. < 10mHz) that the R_{add} and C_{add} intend to fit is usually very difficult to determine due to the long duration of the experiment and the self-discharging effect. Therefore, it was considered to be out of the scope of the SC dynamic characteristic modeling and was decided to analyze the SC self-discharging effect separately with CV method as presented in Section 4.2.5.

Table 4.3 Model IV_2 parameters derived from the zero-bias voltage EIS experimental result of Maxwell® PC5 stack

N	R_{add} (Ω)	C_{add} (F)	R_S (Ω)	L_S (nH)	C_S (F)	τ	Real *RMSE* (10^{-3})	Imaginary *RMSE* (10^{-3})	Real R^2 (max=1)	Imaginary R^2 (max=1)
3+1	0.783	18.5	0.813	20	0.836	1.46	34.9	28.7	0.9811	0.9999

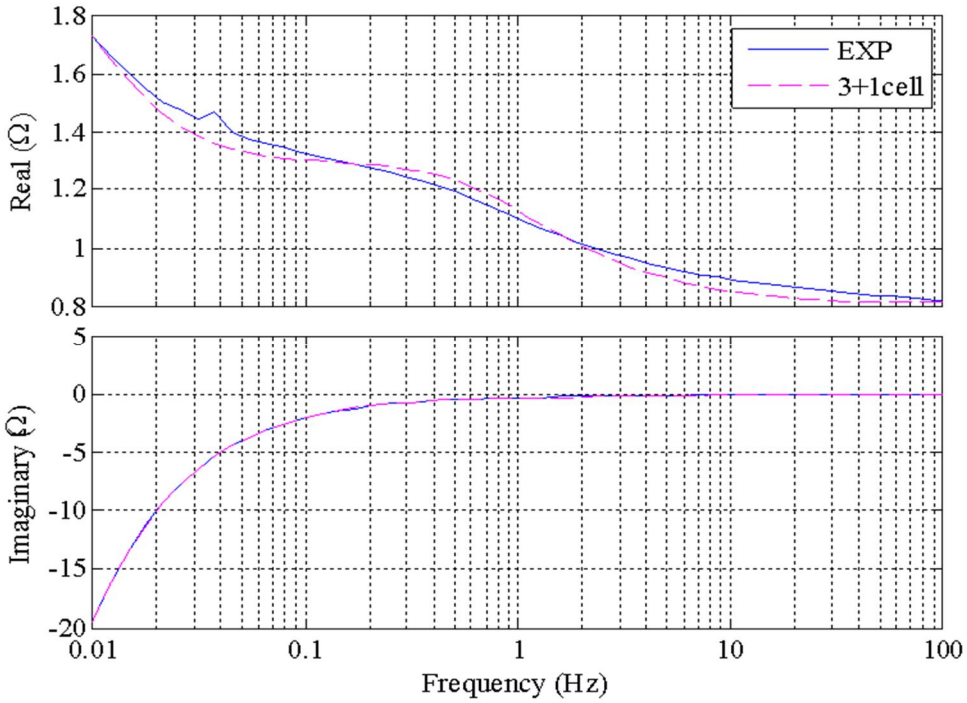


Figure 4.15 Real and imaginary impedance terms versus frequency of the zero-bias voltage measured and model IV_2 (3+1 cells) of the Maxwell® PC5 stack II

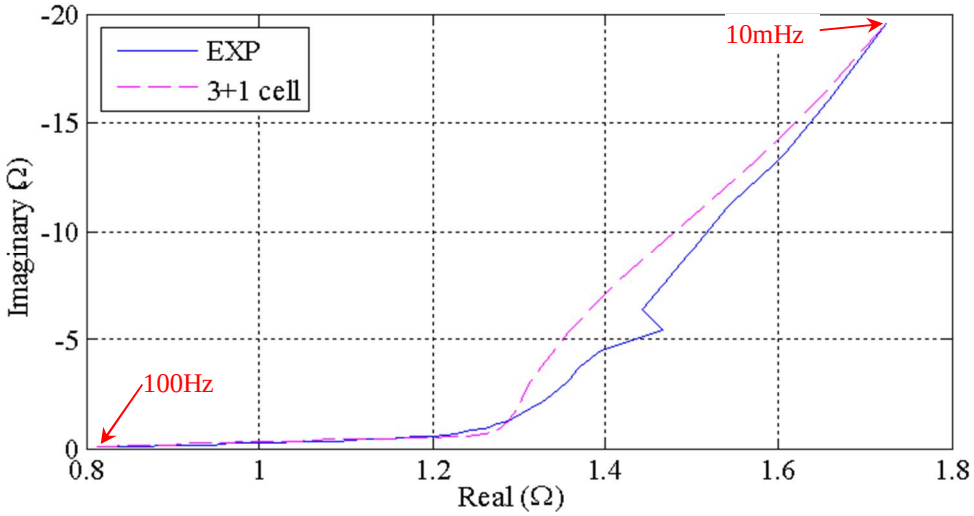


Figure 4.16 Imaginary versus real impedance terms of the zero-bias voltage measured and model IV_2 (3+1 cells) of the Maxwell® PC5 stack II

Next, the Gauss–Newton algorithm is applied again to the 10V DC-bias voltage impedance-frequency experimental result using model IV_2. The 10V bias result is used for further comparison with the model derived from the PCC result in Section 2.5.1.3. The model parameters are shown in Table 4.4. The measured and the estimated impedances are compared as shown in Figure 4.17 and Figure 4.18.

Table 4.4 Model IV_2 parameters derived from the 10V DC-bias EIS experimental result of Maxwell® PC5 stack

N	R_{add} (Ω)	C_{add} (F)	R_S (Ω)	L_S (nH)	C_S (F)	τ	Real *RMSE* (10^{-3})	Imaginary *RMSE* (10^{-3})	Real R^2 (max=1)	Imaginary R^2 (max=1)
3+1	0.4	24.6	0.7419	20	1.1412	1.9710	26.9	27	0.9866	0.9999

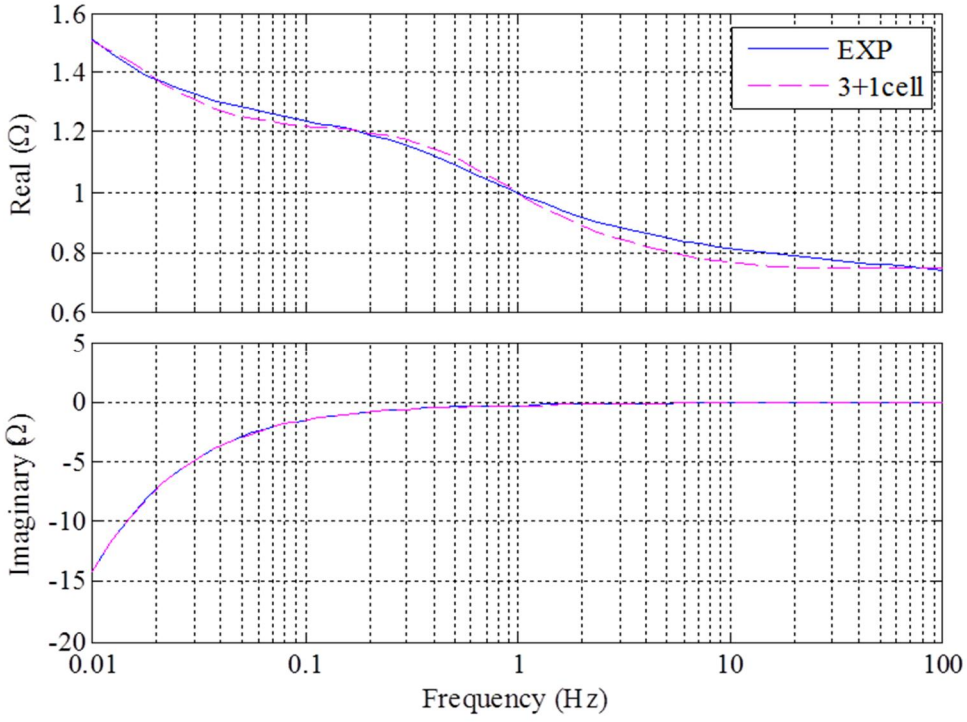


Figure 4.17 Real and imaginary impedance terms versus frequency of the 10V-bias measured and model IV_2 (3+1 cells) of the Maxwell® PC5 stack II

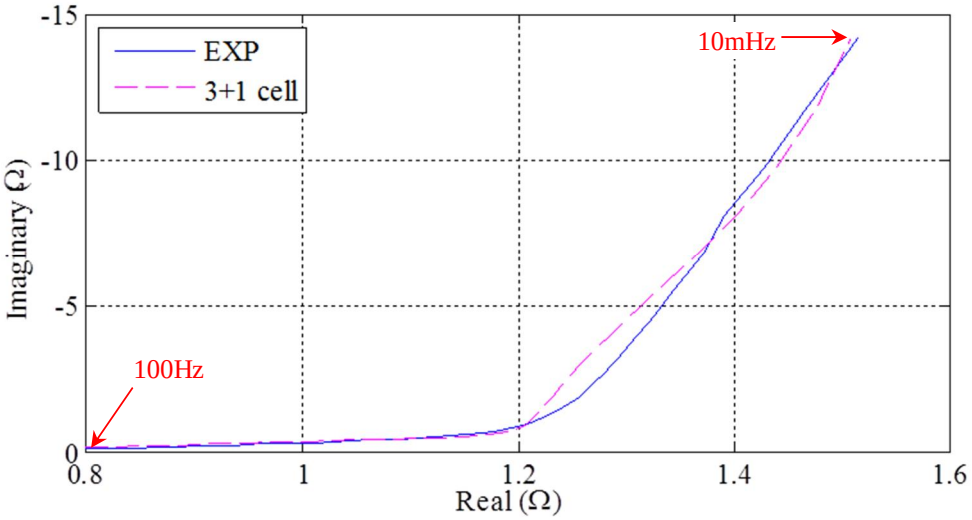


Figure 4.18 Imaginary versus real impedance terms of the 10V-bias measured and model IV_2 (3+1 cells) of the Maxwell® PC5 stack II

4.2.2.2 The Supercapattery Stack I (Nineteen-cell Stack)

The identification process is applied to the experimental results obtained in Section 4.2.1.2 to derive model parameters based on model IV_2. The EIS experimental result at 10V DC-bias is processed with the identification method since it will be used for further evaluation and comparison with the PCC result. The experimental and modeled impedance results at the 10V bias condition are compared in Figure 4.19 and Figure 4.20. The derived model parameters are presented in Table 4.5.

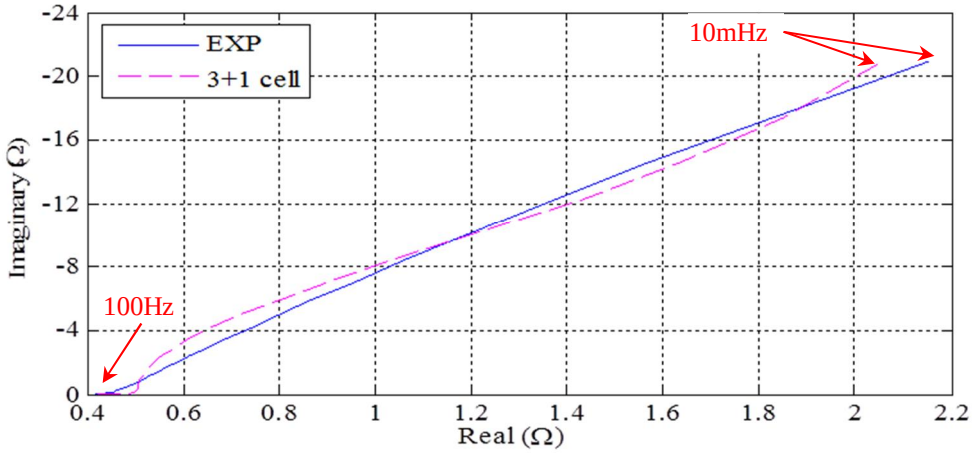


Figure 4.19 Imaginary versus real impedance terms of the 10V-bias measured and model IV_2 (3+1 cells) of the supercapattery stack I

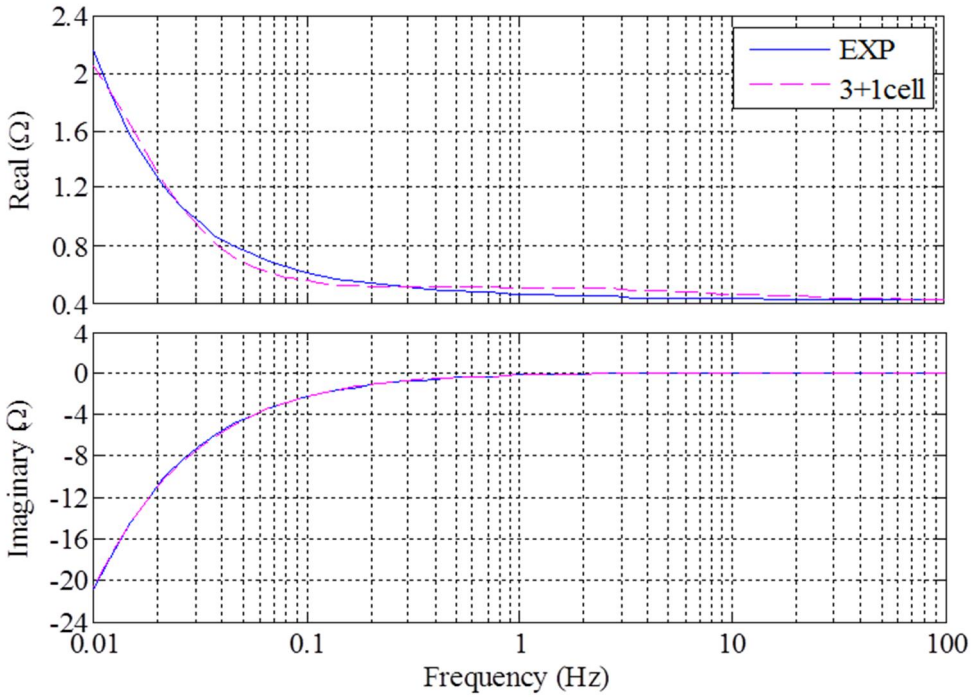


Figure 4.20 Real and imaginary impedance terms versus frequency of the 10V-bias measured and model IV_2 (3+1 cells) of the supercapattery stack I

Table 4.5 Model IV_2 parameters derived from the EIS experimental result of the supercapattery stack I at various DC-bias voltages

DC-bias voltage (V)	R_{add} (Ω)	C_{add} (F)	R_S (Ω)	L_S (nH)	C_S (F)	τ	Real *RMSE* (10^{-3})	Imaginary *RMSE* (10^{-3})	Real R^2 (max=1)	Imaginary R^2 (max=1)
0	1.8	5.15	0.4217	20	0.8247	0.2350	43.8	52.8	0.9845	0.9998
2.5	2	5.5	0.4069	20	0.8024	0.2247	44	56.8	0.9810	0.9998
5	2.1	4.7	0.4080	20	0.8087	0.2295	67.5	109.2	0.9726	0.9994
10	2.25	4.8	0.4205	20	0.8083	0.2428	42.7	62.4	0.9872	0.9998
15	2.4	4	0.4246	20	0.8212	0.2702	59.5	99.7	0.9832	0.9996

Note that in Chapter 6, the supercapattery model will be implemented into the emulator system. Therefore, the identification method is re-applied to the EIS experimental results for all available DC-bias voltages to study the relationship between the model parameters and the applied DC-bias voltage. These parameters are also included in Table 4.5 and the goodness of fitting between the model and experiment are excellent. Both the real and imaginary *RMSE*s are small, and real and imaginary R^2 are close to 1.

From Table 4.5, the R_{add} and C_{add} values were chosen to improve the goodness of fitting between the model and the experimental results. The R_{add} parameters are

selected in the same pattern as the experimental results presented in Figure 4.9 (i.e. when increasing applied DC-bias voltage, the *ESR* is increased). The C_{add} parameters are selected such that the real and imaginary *RMSE*s are minimized. Again the R_S is selected from the highest frequency point of each applied DC-bias voltage experimental results, and L_S is set to 20nH. The fitting algorithm yields the C_S and τ, which are plotted against the applied bias voltage as shown in Figure 4.21 and Figure 4.22. The trend line in Figure 4.21 and Figure 4.22 resemble those of Figure 4.9 and Figure 4.10 where the *C* and *ESR* increase with increasing applied DC-bias voltage. The *ESR* is directly affected by the R_N parameter which is itself proportional to the τ parameter as:

$$R_N = \frac{2\tau}{\pi^2 N^2 C_S} \tag{4.4}$$

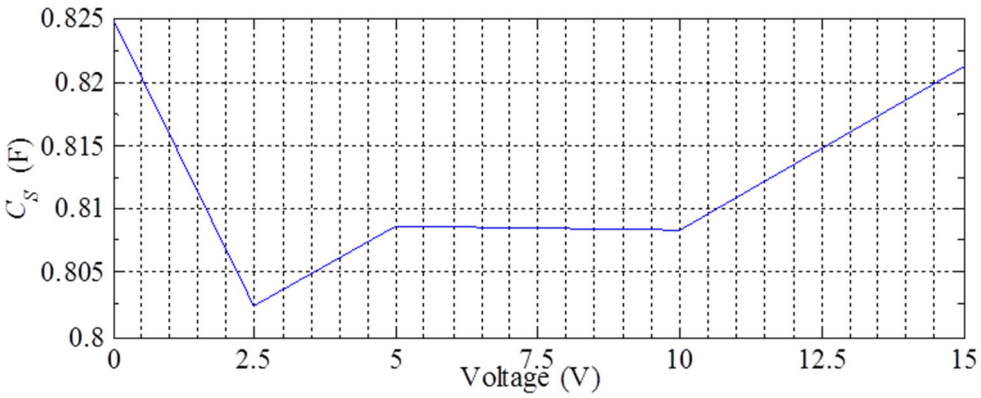


Figure 4.21 The C_S versus the applied DC-bias voltage

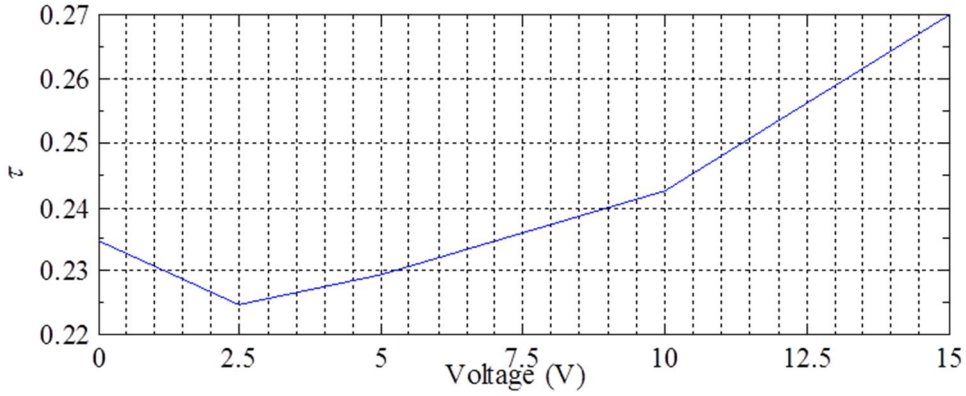


Figure 4.22 The τ versus the applied DC-bias voltage

4.2.3 SC Characterization Results using the Pulse Constant Current (PCC) method and its model identification algorithm

So far only the small signal method (i.e. EIS) has been used to characterize the DUTs. In this section the PCC, which is considered as a large-signal method, is applied as described in Section 2.5.1.3. The PCC method is performed by Rig I to obtain the experimental results of the Maxwell® PC5 stack II and both the supercapattery prototype nineteen-cell and three-cell stacks. The experimental result for the three-cell stack is presented in Appendix B. In addition, the PCC experiment is done after the EIS method as suggested in Section 3.5.1 to obtain consistency results. The model parameters obtained in this section will be compared with the EIS results and evaluated with the EIS method in Section 4.2.4.

4.2.3.1 The Maxwell PC5 Stack II

The Maxwell® PC5 stack II is subjected to the discharged PCC, I_{SC}, at I_P=-2A for the period, T_P = 2.6s. The I_P level and the T_P duration are chosen such that the SC relaxation voltage is revealed as much as possible. The SC voltage response, v_{SC}, is recorded as presented in Figure 4.23. The initial SC stack voltage before applying the PCC, V_i, is 13.2V, and the final SC stack voltage after removing the PCC, V_f, is 8.5V. Thus, the average voltage, V_{avrg}, is 10.85V. The v_{SC} waveform shown in Figure 4.23 is filtered digitally so that the steady-state condition of the voltage after removing the PCC can be observed clearly. However, in the parameter fitting process, the non-filtered v_{SC} is used, so the derived model parameters are not affected by the filtering effect.

The voltage response after removing the PCC (i.e. during the relaxation period) can be fitted by using a sum of exponential terms as described in (2.11), which is presented here again as (4.5), via the MATLAB® Curve Fitting Toolbox™. There will be a direct and simple solution for mapping each term with an exponential coefficient, X_k, and an inverse of time constant, Y_k.

$$V_{SC}(t) = \sum_{k=1}^{N}\left(-X_k e^{-Y_k t}\right) + const \tag{4.5}$$

where N is a number of exponential terms use. N is also represents a number of RC parallel cell used in the model.

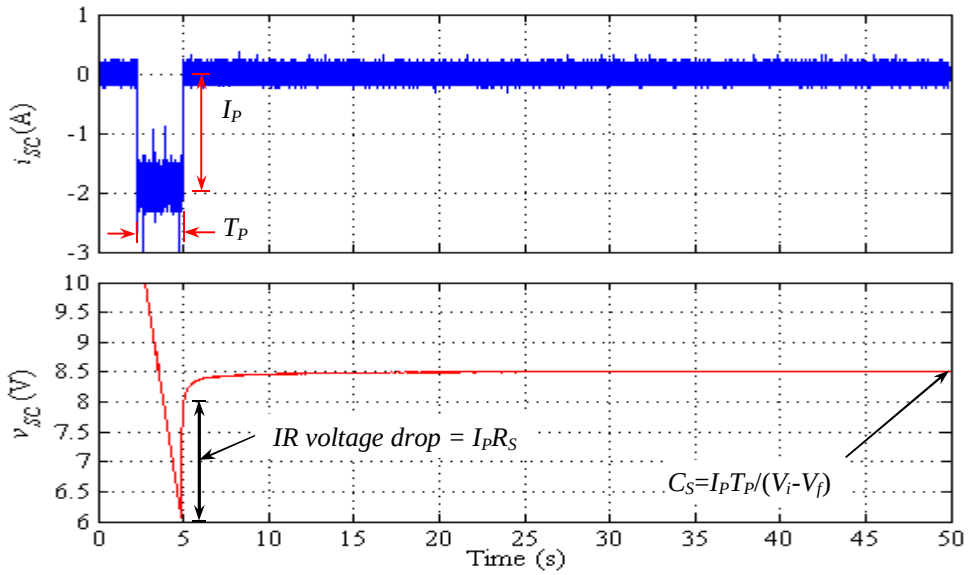


Figure 4.23 Experimental result of the discharged PCC on the Maxwell® PC5 SC stack II (filtered voltage version) (I_P = –2A, T_P = 2.6s, V_i = 13.2V and V_f = 8.5V)

In the fitting process, the min/max boundaries of the X_k and Y_k terms are defined according to Section 2.5.1.3. When the searching algorithm is reported with 'Fixed at bound', the boundary is expanded such that the fitting algorithm can explore the suitable fit parameters independently. This results in better fitting performance. The fitting coefficients X_k and Y_k, *RMSE* and R^2 are presented in Table 4.6.

Table 4.6 The fitted coefficients and the error from the MATLAB® Curve Fitting Toolbox™ at various N

N	X_1	Y_1	X_2	Y_2	X_3	Y_3	X_4	Y_4	*const*	*RMSE* (10^{-3})	R^2 (max=1)
1	0.557	1.435							8.497	28.59	0.7403
2	0.136	0.21	0.67	4.366					8.506	21.26	0.8564
3	0.105	0.161	0.333	1.997	0.483	11.07			8.508	20.79	0.8627
4	0.099	0.153	0.248	1.578	0.489	7.517	0.185	88.31	8.508	20.75	0.8632

From Table 4.6, as N increases from 1 to 2, the fitting error is reduced dramatically, but the improvement is small when N is increased further. In addition, the *RMSE* and R^2 parameters are plotted against N as presented in Figure 4.24. Note that the *RMSE* and R^2 represent the error and goodness of fit between the model and the experiment result only at the period after removing the PCC. The fitting is very good as seen by

low *RMSE*. However, the R^2 is low since the algorithm tries to fit the noisy experimental signal.

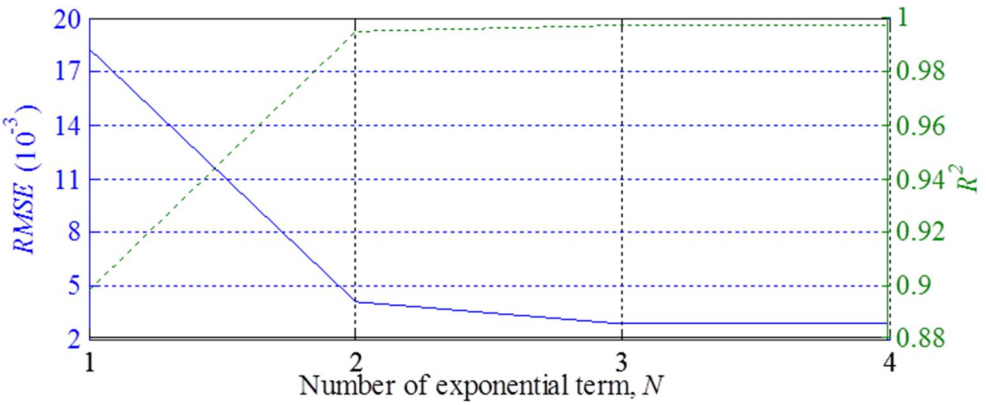


Figure 4.24 Goodness of fit represented in *RMSE* and R^2 versus number of exponential term, *N*

Model IV_3 presented in Figure 2.14 is used with the PCC method, and it is presented here as Figure 4.25. The model is used together with the fitting coefficients presented in Table 4.6 to derive the model parameters according to (4.6)-(4.9). The derived model parameters are presented in Table 4.7.

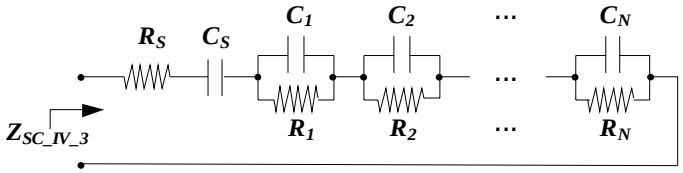


Figure 4.25 Model IV_3: The *N* series-parallel RC model without L_S

$$X_k = \left(1 - e^{-Y_k T_P}\right) R_k I_P \tag{4.6}$$

$$Y_k = \frac{1}{R_k C_k} \tag{4.7}$$

$$R_S = \frac{IR\ voltage\ drop}{I_P} \tag{4.8}$$

$$C_S = \frac{I_P T_P}{\left(const - V_i\right)} \tag{4.9}$$

The model of Figure 4.25 with the parameters shown in Table 4.7 has been evaluated with the MATLAB® SimPowerSystem Toolbox™. The comparison between the model voltage response and the experimental result was performed both after the

pulse period and during the pulse period. The results are shown in Figure 4.26 and Figure 4.27.

Table 4.7 The RC parameters extracted from Table 4.6 based on model IV_3 (expressed in Ω and F)

N	R_1	C_1	R_2	C_2	R_3	C_3	R_4	C_4	R_S	C_S
1	0.285	2.442							0.705	1.103
2	0.162	29.438	0.335	0.683					0.705	1.107
3	0.154	40.49	0.167	2.995	0.242	0.374			0.705	1.108
4	0.152	43.174	0.126	5.03	0.245	0.544	0.093	0.122	0.705	1.109

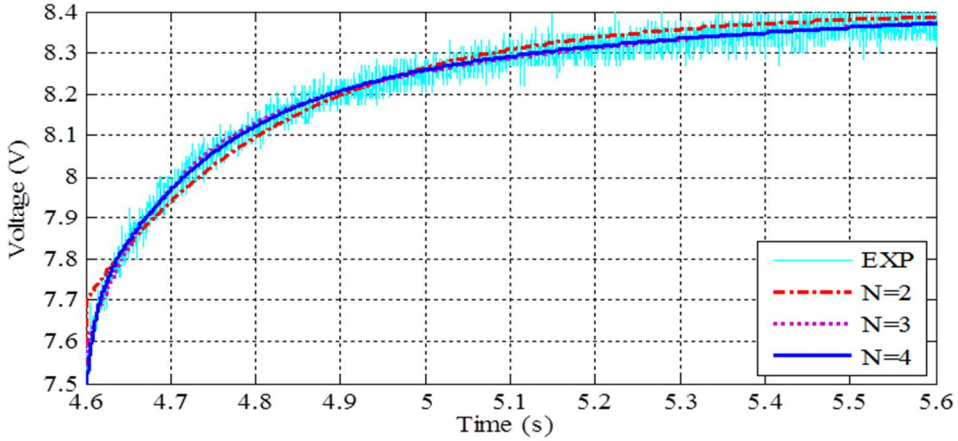


Figure 4.26 The comparison of the voltage response after removing the PCC between the experimental result and the simulations with different model order N used

From Figure 4.26, the model voltage response fits the experimental results very well despite the low R^2 from Table 4.6. As expected, as N increases, the model fits better with the experiment in the period after removing PCC. By visual inspection, the curve fitting improvement presented in Figure 4.26 is in agreement with the error presented in Table 4.6.

From Figure 4.27, the precision of the model, which was tuned for the voltage response after removing the PCC, shows a significant improvement from $N = 2$ to $N = 3$ for the response during the current pulse. The improvement is minor from $N = 3$ to 4. It is therefore considered that an order of $N = 4$ gives the best trade-off between performance versus model complexity for the Maxwell PC5 stack II.

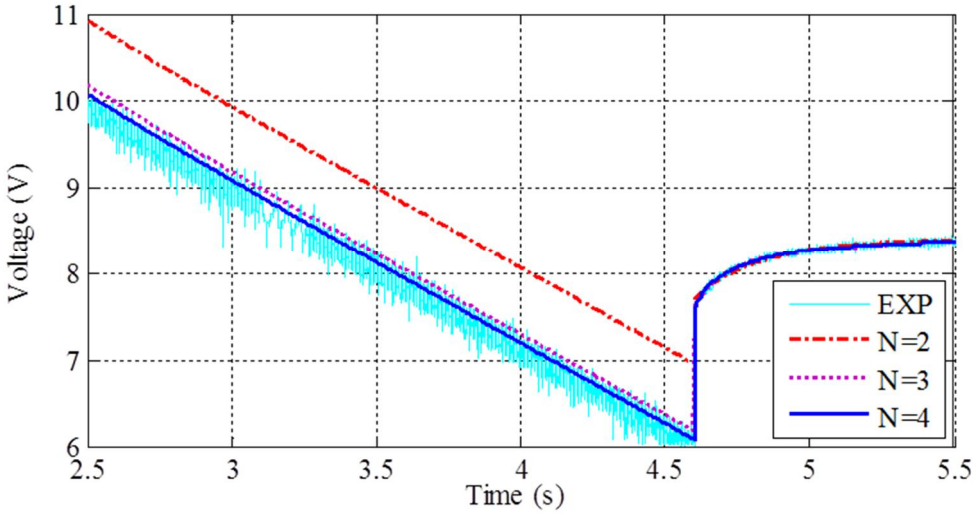


Figure 4.27 The comparison of the voltage response during the PCC between the experimental result and the simulations with different model order *N*

4.2.3.2 The Supercapattery Stack I (Nineteen-cell Stack)

The supercapattery stack I is also characterized by the PCC at I_P = -5.8A for T_P = 168.3ms, and the v_{SC} is recorded as shown in Figure 4.28. The V_i, V_f and V_{avrg} are 10.24V, 9.107V and 9.67V. For this device, a digital filter is applied to remove noise from the experimental signal, so the fitting result is expected to improve. However, the fitting result is acceptable only in the relaxation period. It does not show good agreement with the entire waveform as was the case with the Maxwell stack. This poor fitting is due to the poor recorded v_{SC}, which is distorted by the measurement equipment.

However, the derived model in this section is still useful despite the experimental signal being distorted and filtered. As will be seen in Section 4.2.4.2, the derived model is in agreement with the EIS-based model. The PCC method was re-applied to the supercapattery stack I after a period of 6 months. Degradation had occurred, with the results shown in Appendix B.

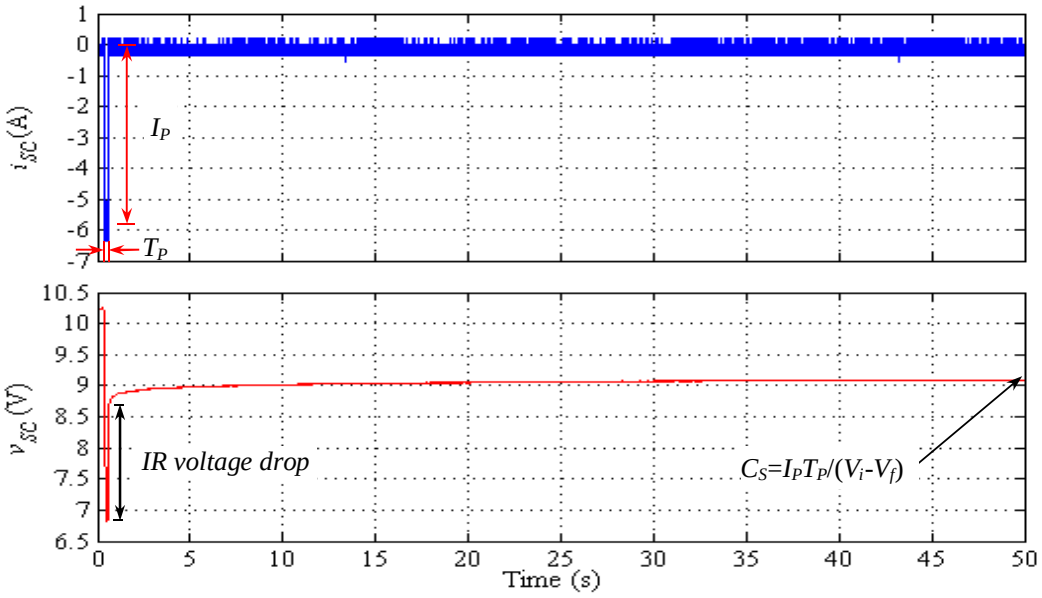


Figure 4.28 Experimental result of the discharged PCC on the supercapattery stack I (I_P = –5.8A, T_P = 163.8ms, V_i = 10.24V and V_f = 9.107V)

The curve fitting toolbox is used with the experimental signal as before, and the coefficients X_k and Y_k, the *RMSE* and the R^2 are presented in Table 4.8. Similar to the Maxwell PC5 stack II, as N increases from 1 to 2, the fitting error is reduced dramatically, but the improvement is small when N is increased further. The *RMSE* and R^2 are also presented Table 4.8, which indicates the error and the goodness of fit between model and experiment. By using (4.6)-(4.9) and the fitting coefficient presented in Table 4.8, the model parameters are derived as presented in Table 4.9.

Table 4.8 The fitted coefficients and the error from the MATLAB® Curve Fitting Toolbox™ at various N

N	X_1	Y_1	X_2	Y_2	X_3	Y_3	X_4	Y_4	*const*	*RMSE* (10^{-3})	R^2 (max=1)
1	0.207	0.115							9.083	16.11	0.9041
2	0.165	0.071	0.253	2.1					9.095	7.79	0.9775
3	0.159	0.065	0.209	1.443	0.911	205			9.098	4.74	0.9917
4	0.144	0.049	0.122	0.544	0.204	6.076	0.094	324.7	9.107	2.88	0.9969

Table 4.9 The RC parameters extracted from Table 4.8 based on model IV_3 (expressed in Ω and F)

N	R_1	C_1	R_2	C_2	R_3	C_3	R_4	C_4	R_S	C_S
1	1.9098	4.5532							0.3793	0.8183
2	2.4658	5.7385	0.1498	3.1799					0.3793	0.8268
3	2.6008	5.9473	0.1714	4.0426	0.1570	0.0311			0.3793	0.8290
4	3.1029	6.5665	0.2472	7.4445	0.0559	2.9453	0.0162	0.1906	0.3793	0.8356

Model IV_2 with the parameters of Figure 4.25 shown in Table 4.9 is simulated. The comparison between the model and the experimental results both after the pulse period and during the pulse period are shown in Figure 4.29 and Figure 4.30, respectively.

From Figure 4.29, for an order of N = 4, the fitting is acceptable in the period after the PCC. From Figure 4.30, the fitting result during the pulse period is not good even when an order of N=4 is used. This is due to the signal filtering and distortion.

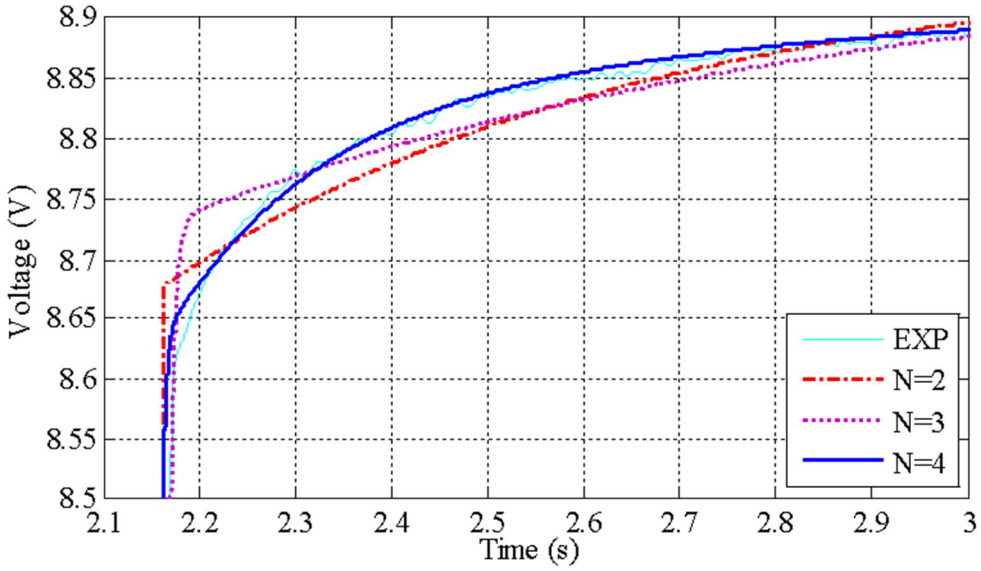


Figure 4.29 The comparison of the voltage response during applying the PCC between the experimental result and the simulations with different model order N used

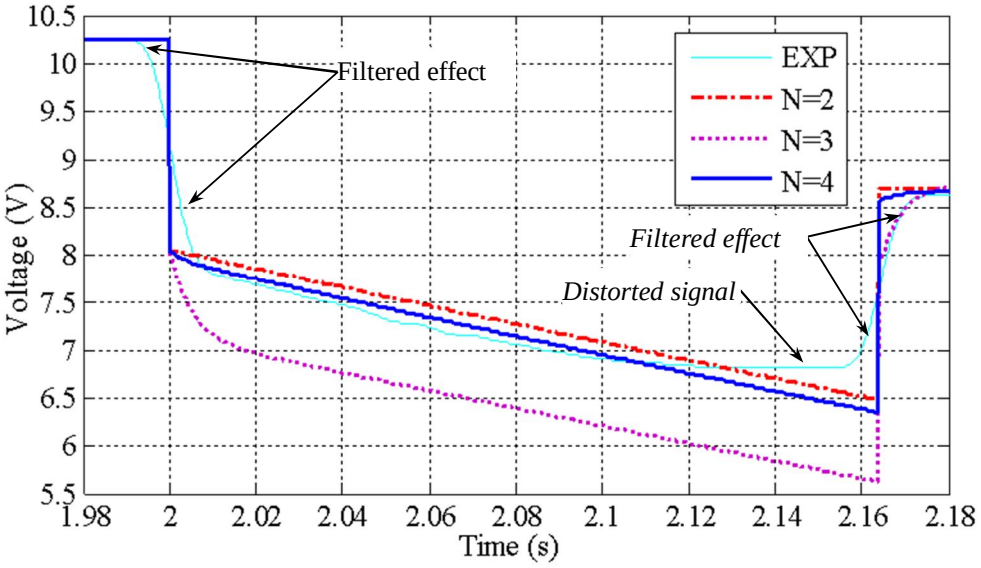


Figure 4.30 The comparison of the voltage response after removing the PCC between the experimental result and the simulations with different model order N used

4.2.4 Evaluation of the Electrochemical-Impedance-Spectroscopy-based and the Pulse-Constant-Current-based models

In this section, the EIS-based and the PCC-based models are evaluated and compared with the experimental results under the EIS and the PCC methods through simulation. The chosen devices are the Maxwell® PC5 stack II and the supercapattery stacks I. The evaluation of the supercapattery stack II is included in Appendix B.

4.2.4.1 The Maxwell® PC5 Stack II (8x2)

Firstly, the frequency response of the PCC-based model of Figure 4.25 is evaluated and the result (denoted as PCC) is compared with the experimental results (denoted as EIS-EXP) and with the EIS-based model (denoted as EIS) presented in Figure 4.18. The results are shown in Figure 4.31 and Figure 4.32. Note that all results are either obtained or derived from nearly the same DC bias-voltage of 10V.

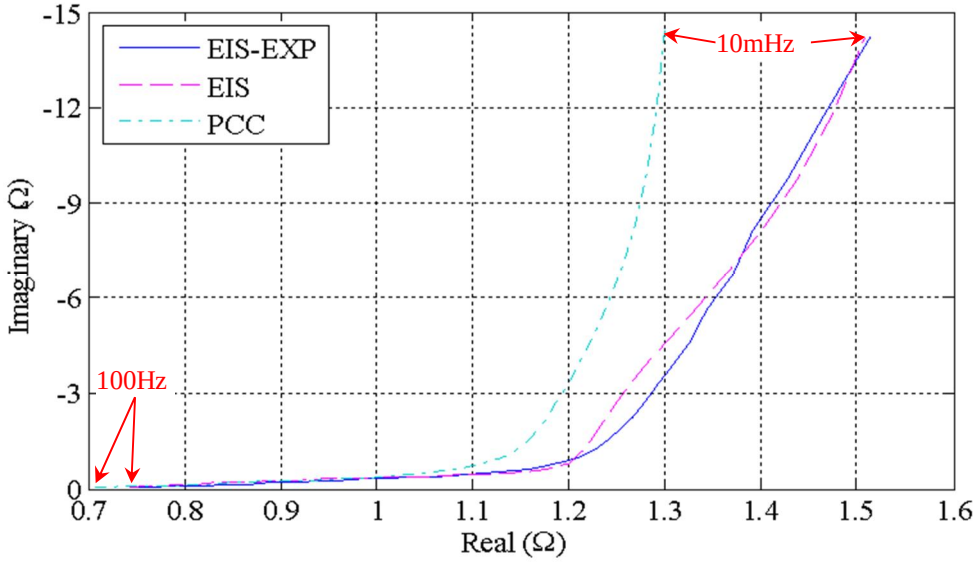


Figure 4.31 Imaginary versus real impedance terms of the 10V-bias EIS experimental result, the EIS-derived and the PCC-derived results of the Maxwell PC5 stack II

Figure 4.31 shows the imaginary versus the real impedance terms of the PCC, the EIS, and the EIS-EXP results. In the low frequency range, the real impedance part of the PCC is less than both the EIS-EXP and the EIS. The results are re-plotted as the real and the imaginary impedance terms versus frequency and shown in Figure 4.32.

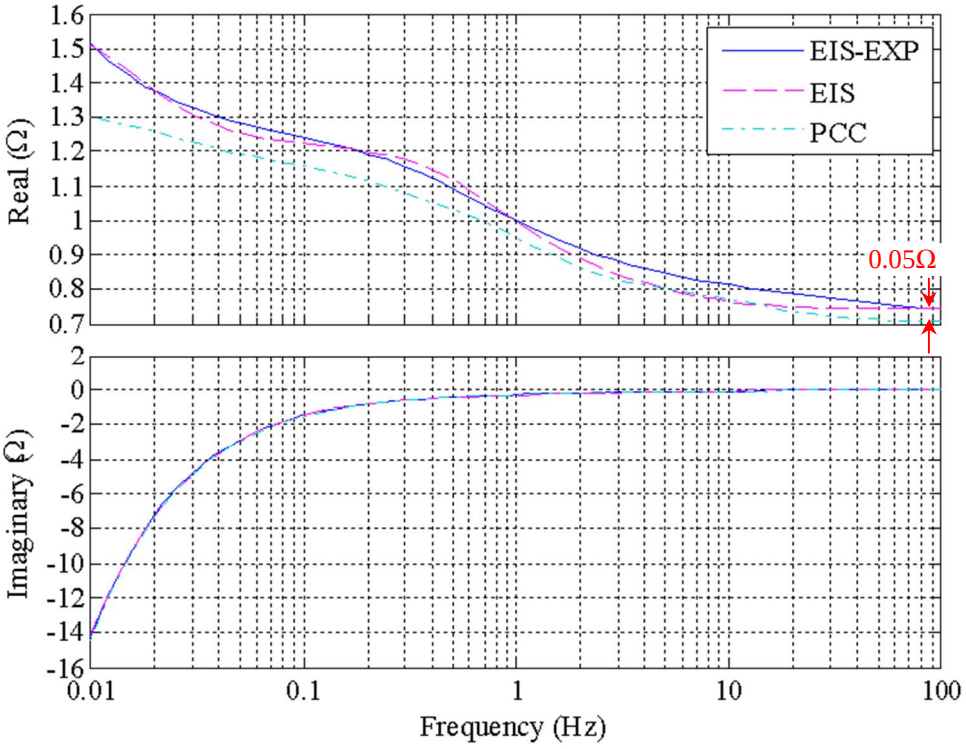


Figure 4.32 Real and imaginary impedance terms versus frequency of the 10V-bias EIS experimental result, the EIS-derived and the PCC-derived results of the Maxwell PC5 stack II

The imaginary impedance part of the PCC fits the EIS-EXP very well. However, there is the offset error in the real impedance part between the PCC and the EIS-EXP. In addition, from Figure 4.32, it can be seen that if the R_S component of the PCC is increased by approximately 50mΩ, the real impedance part of the PCC would fit that of the EIS-EXP better. This extra resistance derives probably from the lead cable and the plug connection that are used in the EIS measurement. To justify the goodness of fit, the errors between the PCC and the EIS-EXP, and between the EIS and the EIS-EXP, are calculated and presented in Table 4.10. The high discrepancy between the PCC and the EIS-EXP is confirmed with the higher real *RMSE* and the lower real R^2 than the EIS.

Table 4.10 Error between the EIS and the PCC models and the EIS experimental result

Model from	Real *RMSE* (10^{-3})	Imaginary *RMSE* (10^{-3})	Real R^2 (max=1)	Imaginary R^2 (max=1)
EIS	26.688	27.014	0.9866	0.9999
PCC	78.962	59.323	0.8846	0.9996

Next, the EIS-based model is evaluated with the PCC simulation, and the result is compared with the PCC-based model and the PCC experimental result (denoted as PCC-EXP) as shown in Figure 4.33 and Figure 4.34.

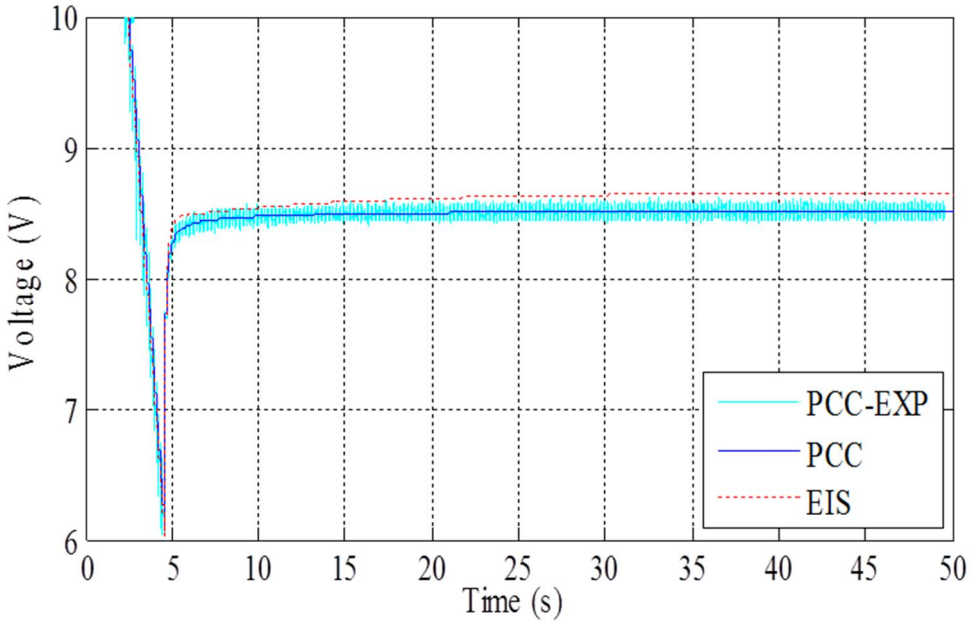


Figure 4.33 The comparison of the voltage response from the PCC method between the EIS-based model, the PCC-based model and the PCC experimental result

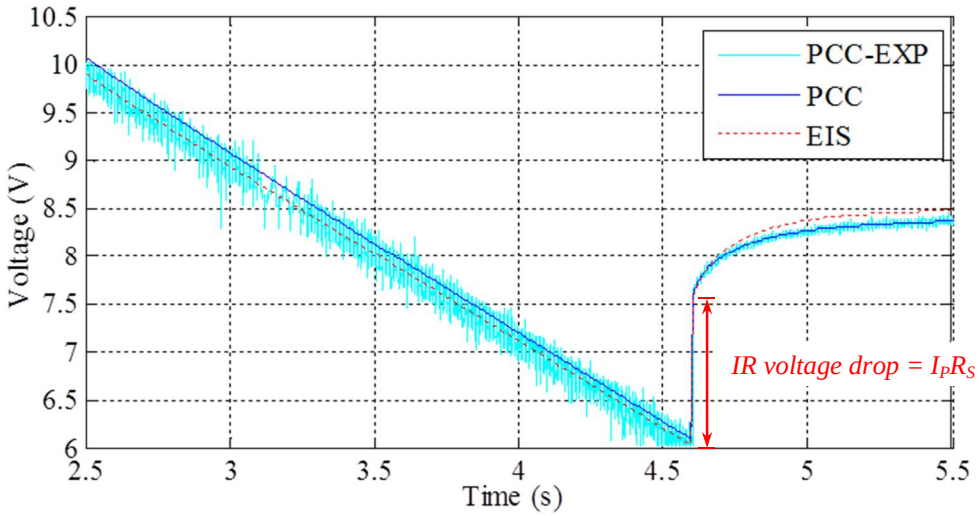


Figure 4.34 The comparison of the voltage response during applying and removing the PCC between the EIS-based model, the PCC-based model and the PCC experimental result

From Figure 4.33, considering the voltage response after removing the PCC (i.e. the relaxation period), the EIS has the final steady-state voltage and error higher than both the PCC and the PCC-EXP. This discrepancy is explained by the difference in the C_S value used in each model. The EIS and the PCC C_S parameters are 1.141F and

1.109F, which cause the EIS bouncing voltage after discharge to become slightly higher than that of the PCC.

During the applying PCC period, the EIS voltage response fits the PCC-EXP better than the PCC as indicated in Figure 4.34 that the EIS voltage response is placed directly at the middle of the PCC-EXP. This effect is due to the different in the C_S and the R_S parameters used in each model. The R_S parameters of the EIS and the PCC, which are 0.7419Ω and 0.705Ω, affect directly the IR voltage drop after removing the PCC. Note that the small difference in R_S and C_S parameters between the two models is probably due to slightly mismatch in the comparison of the model parameters with small difference in the DC-bias voltage. The DC-bias voltage of the PCC method is calculated as an averaged value from the initial and final voltages while in the EIS method, the applied DC-bias is fixed.

4.2.4.2 The Supercapattery Stack I (Nineteen-cell Stack)

Firstly, the frequency response of the PCC-based model presented of Figure 4.25 is simulated and the result (PCC) is compared with the experimental results (EIS-EXP) and with the EIS-based model (EIS) presented in Figure 4.19. The comparison is shown in Figure 4.35 and Figure 4.36. Note that all results are either obtained or derived from nearly the same DC bias-voltage of 10V.

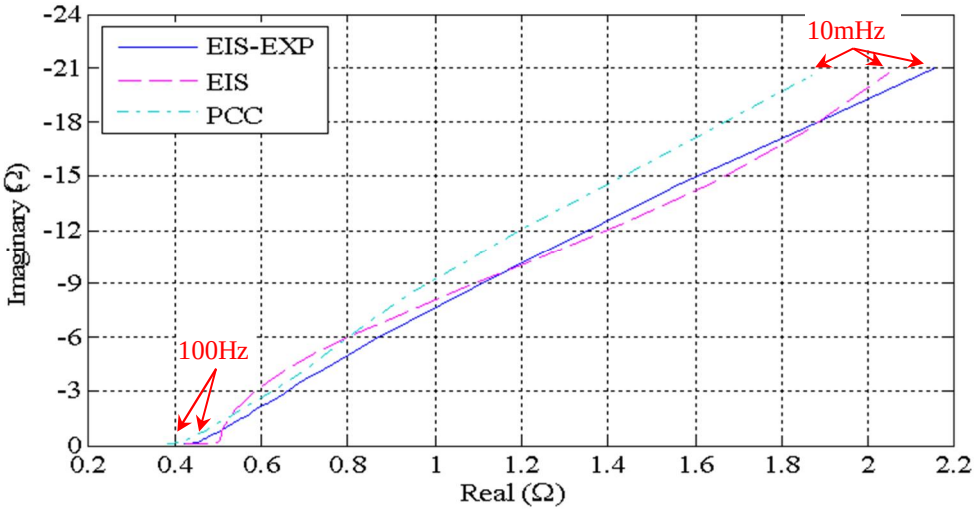


Figure 4.35 Imaginary versus real impedance terms of the 10V-bias EIS experimental result, the EIS-derived and the PCC-derived results of the supercapattery stack

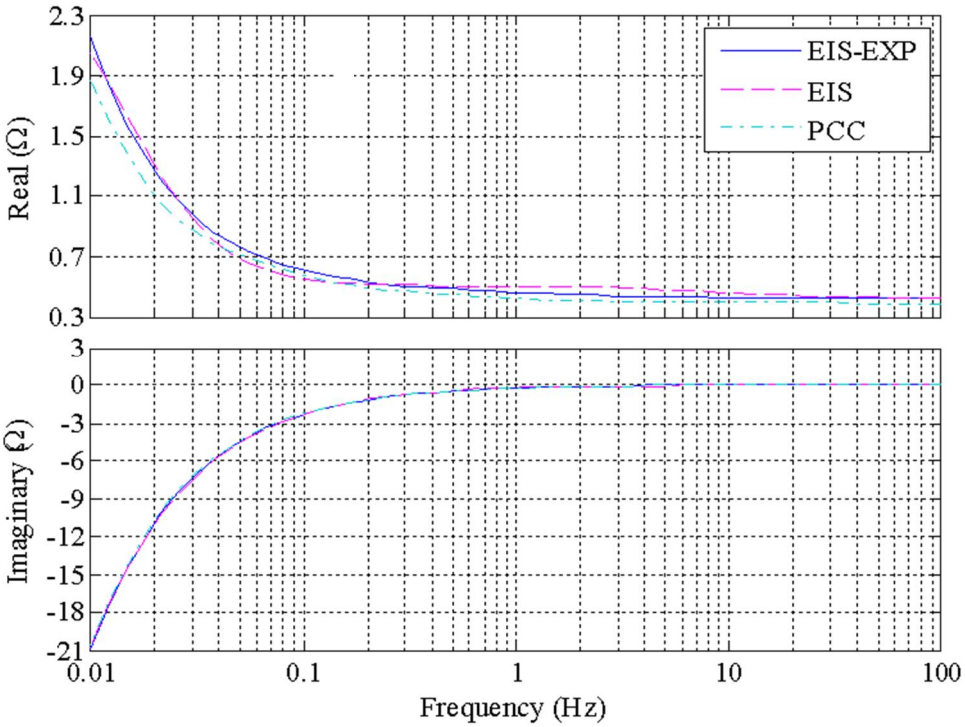


Figure 4.36 Real and imaginary impedance terms versus frequency of the 10V-bias EIS experimental result, the EIS-derived and the PCC-derived results of the supercapattery stack

Figure 4.35 shows the imaginary versus the real impedance terms of the PCC, the EIS, and the EIS-EXP results. The real impedance part of the PCC is less than both the EIS-EXP and the EIS for the entire frequency range. It is clearly seen that as the frequency decreases, the real impedance part of the PCC diverges from both the EIS-EXP and the EIS. The results are re-plotted as the real and the imaginary impedance terms versus frequency as presented in Figure 4.36. The discrepancies between the PCC and the EIS-EXP, and between the EIS and the EIS-EXP in both the real and the imaginary plots are very small. In addition, the imaginary impedance part of the PCC fits the EIS-EXP very well. However, there is an offset error ≈40mΩ for the real impedance part between the PCC and the EIS-EXP. The errors between the PCC and the EIS-EXP, and between the EIS and the EIS-EXP are presented in Table 4.11. The high discrepancy between the PCC and the EIS-EXP is confirmed with the higher real *RMSE* and the lower real R^2 than the EIS.

Table 4.11 Error between the EIS and the PCC models and the EIS experimental result

Model from	Real *RMSE* (10^{-3})	Imaginary *RMSE* (10^{-3})	Real R^2 (max=1)	Imaginary R^2 (max=1)
EIS	45.67	62.388	0.9872	0.9998
PCC	78.349	88.787	0.9569	0.9996

Next, the EIS-based model is evaluated with the PCC method, and the result is compared with both the PCC-based model and the PCC experimental result (denoted as PCC-EXP) as shown in Figure 4.37 and Figure 4.38.

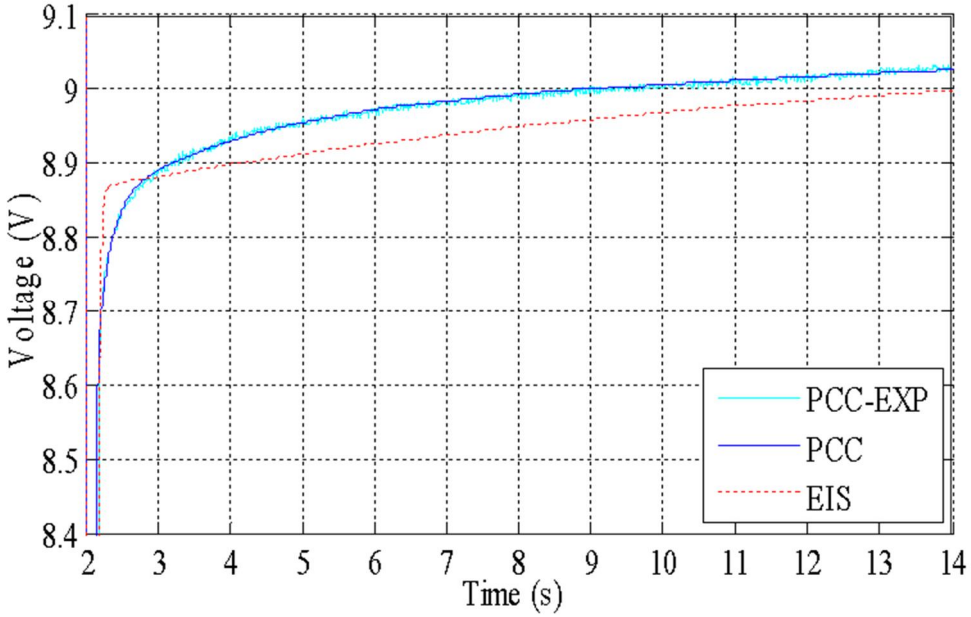


Figure 4.37 The comparison of the voltage response after removing the PCC between the EIS-based model, the PCC-based model and the PCC experimental result

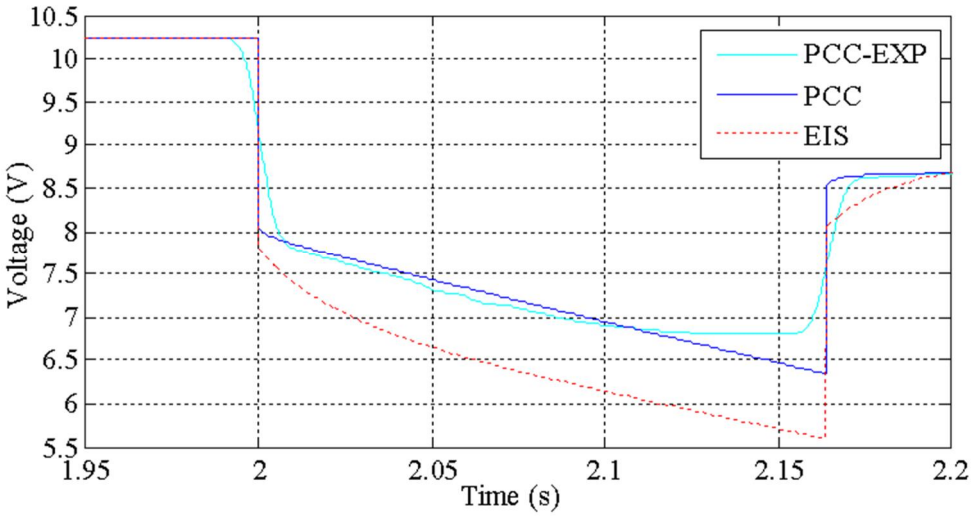


Figure 4.38 The comparison of the voltage response during applying the PCC method between the EIS-based model, the PCC-based model and the PCC experimental result

From Figure 4.37, considering the voltage response after removing the PCC (i.e. the relaxation period), the EIS has the final steady-state voltage and error lower than the PCC and the PCC-EXP. Again this discrepancy is explained by the difference in the C_S value used in each model. The EIS and the PCC C_S parameters are 0.8083F and

0.8356F, which cause the PCC bouncing voltage after discharge to become higher than that of the EIS.

Figure 4.38 shows the voltage responses during the PCC period. The PCC voltage response fits the PCC-EXP better than the EIS even though their R_S parameters are slightly different (i.e. 40mΩ) as indicated in the frequency response testing. Thus, a small mismatch in the model parameters between the EIS and the PCC as indicated in the frequency response testing can yield large discrepancies in the voltage response in the large signal test.

4.2.5 SC Characterization Results Using the Constant Voltage (CV) Method

As discussed in Section 2.5.1.5, the constant voltage method (CV) is employed to evaluate the long-term performance of the Maxwell PC5 stack II and the supercapattery stack I (nineteen-cell). The process presented in Section 3.5.2 is also applied here to improve the result consistency.

Firstly, the CV method is applied to both devices at the device rated In addition, there is a 10Ω shunt resistor connected in series with the CV source to limit the starting current when charging both devices from completely discharged conditions. The choice of resistor affects the starting current, the charging time and the energy retention performance [72]. In this experiment, the chosen 10Ω shunt resistor yields good trade-offs between the charging time, the charging current and the self-discharging duration. The charging is applied to both devices for approximately 1 hour even though the device rated voltages are reached (i.e. 20V and 19V for the Maxwell PC5 stack II and the supercapattery stack I). The experimental results are presented in Figure 4.39 and Figure 4.40.

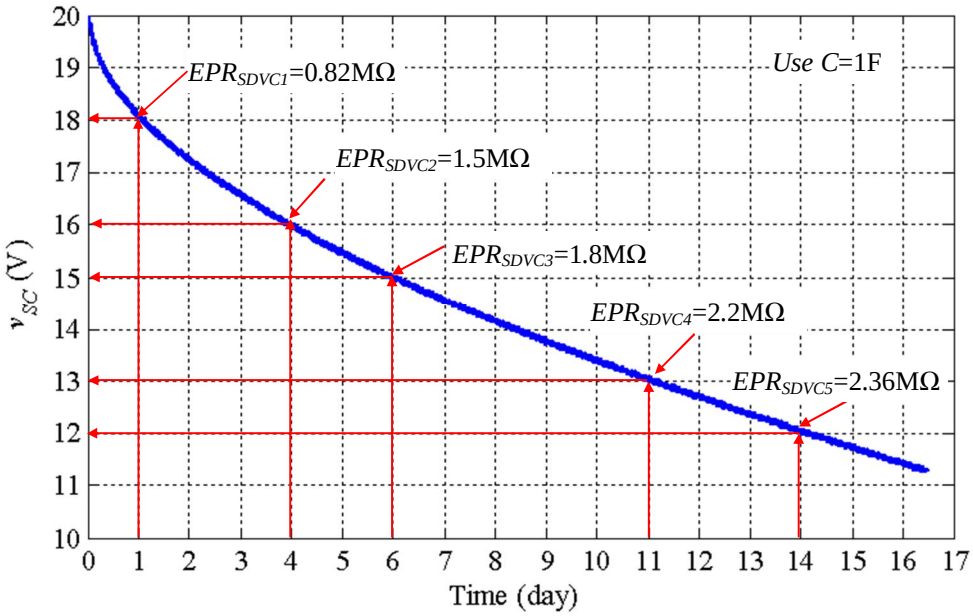


Figure 4.39 The self-discharging voltage of the Maxwell PC5 stack II

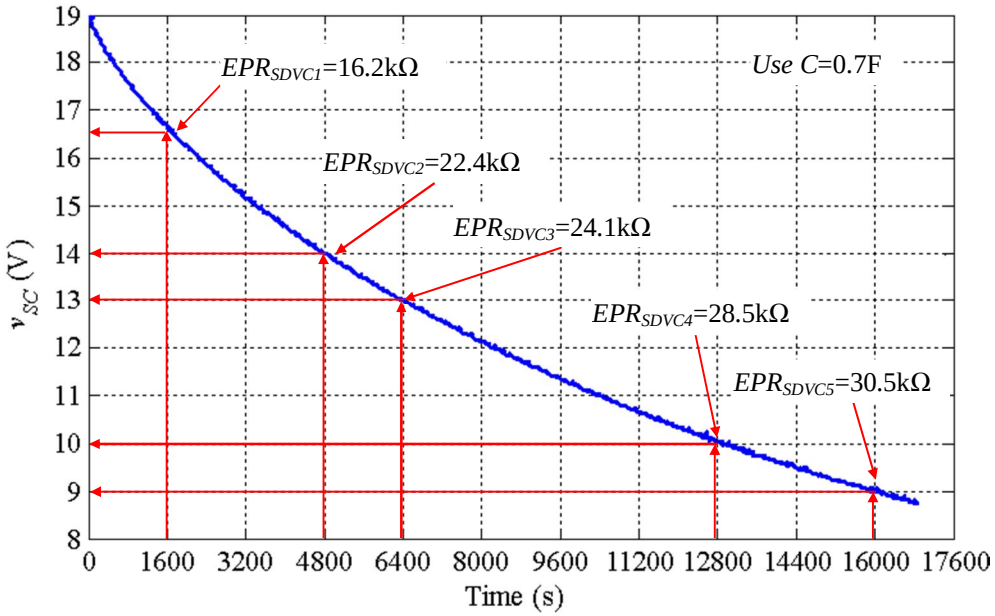


Figure 4.40 The self-discharging voltage of the supercapattery stack I

From these figures, the self-discharging duration of both devices is seen to be completely different. The results are therefore presented in the different time scales (i.e. days for the Maxwell® SC and seconds for the supercapattery). It was found that the technology based on the aqueous electrolyte (the supercapattery) has higher self-discharging rate than that of the organic electrolyte (i.e. Maxwell). Equation (2.12) is applied to the v_{SC} experimental results, and the equivalent parallel resistor for the self-discharge voltage characteristic, EPR_{SDVC}, is calculated and shown in both Figure 4.39 and Figure 4.40. Equation (2.12) is presented here again as (4.10).

$$v_{SC}(t) \approx v_{SC}(0) e^{-\frac{t}{EPR_{SDVC} C}} \rightarrow EPR_{SDVC} = -\frac{t}{C \ln\left(v_{SC}(t)/v_{SC}(0)\right)} \tag{4.10}$$

From (4.10), as v_{SC} decreases, EPR_{SDVC} is increased for both devices. Initially, after disconnecting the CV source, the v_{SC} for the Maxwell® SC drops dramatically with the calculated *EPR* is as low as 0.82MΩ at 18V (1 day). The *EPR* is increased by approximately 3 times (2.36MΩ) after the v_{SC} has dropped to 12V (14 days). For the v_{SC} of the supercapattery, the calculated *EPR* is very low at 16.2kΩ at 16.5V (1600s), and the *EPR* is approximately doubled (30.5kΩ) after the v_{SC} has dropped to 9V (16000s).

However, as shown in the frequency response of Figure 4.9, the *C* used in the calculation is depended on the DC-bias voltage. The calculated *EPR* may not represent the actual leakage resistance at the specified DC-bias voltage. Thus, an alternative process is used by connecting the CV source across the supercapattery stack and measuring the charging current, which will replenish the leakage energy. This process is called the "CV-with-floating-current". The charging time is approximately 1 hour interval for each voltage point. The charging current and the charging voltage are recorded and used with (4.11).

$$EPR_{I\_Leak} = \frac{V_S}{I_{Leak}} \tag{4.11}$$

The result for the supercapattery is presented in Figure 4.41. Note that this technique is difficult to apply to the Maxwell® SC since its leakage current is very small and a very high precision current measurement device is required.

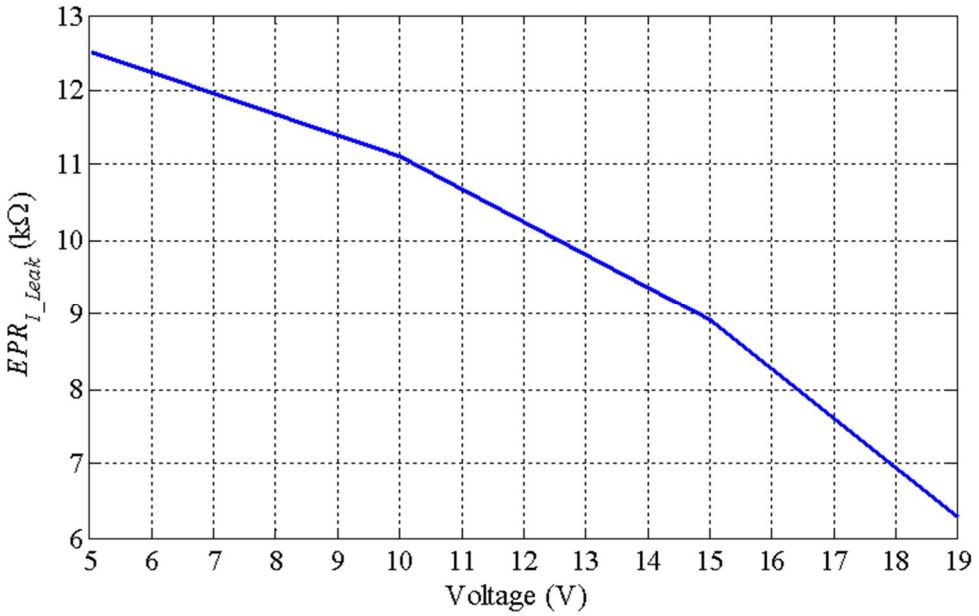


Figure 4.41 The supercapattery stack I *EPR* from the CV with floating current process

In Figure 4.41, the current measurement is recorded through a digital ammeter. With the measured voltage and current, V_S and I_{Leak}, the EPR_{I_Leak} is calculated. As the applied voltage decreases, the EPR_{I_Leak} is increased. However, EPR_{I_Leak} is much smaller than the EPR_{SDVC}.

In this section, the CV method has been used to characterize long-term characteristic of the Maxwell® PC5 stack II and the supercapattery stack I. The results indicate that the energy retention capability of the Maxwell is much better than the supercapattery as indicated by the higher derived *EPR* value in the MΩ range compared with the 10kΩ range of the supercapattery. The supercapattery is being further investigated with the "CV-with-floating-current" process. The results show lower derived *EPR* than the conventional CV method.

As mention in Section 2.1, the SC self-discharging characteristic is not included in the final equivalent model. This is due to the lack of proper equipment to control temperature, to do long-period data-logging and to measure very small current (i.e. μA range). The results obtained in this section are used only for the technology comparison purposes.

Next, the round-trip efficiency and the energy loss of the Maxwell PC5 stack I and II are evaluated by the constant power cycling method, and the experimental results of each device are presented.

4.3 Round-trip Efficiency and Energy Loss Evaluation

As discussed in Section 2.5.2.4, the constant power cycling method (CPC) is employed to evaluate a SC round-trip charge-discharge efficiency, η_{RT}, and energy loss, E_{Loss_RT}, over a charge-discharge cycle. The CPC method is performed using Rig I. The experiment in this section is done according to the SC characterizing process presented in Section 3.5.3. The DUTs are the Maxwell® PC5 stacks I and II, and their experimental results are presented. In addition, the duty cycle method presented Section 2.6.1.1 is applied to all devices to estimate the η_{RT} due to its simplicity.

4.3.1 The Maxwell® PC5 Stack I (8x1)

Firstly, the Maxwell® PC5 stack I (i.e. 8 cells of series Maxwell® PC5) was tested using the CPC method at the constant power, P, of 7, 10 and 15W with the operating voltage range, V_{SC_min}-V_{SC_max}, of 7-20V, 10-20V and 15-20V. The choice of testing conditions (i.e. P, V_{SC_min} and V_{SC_max}) is limited by the device rated current of 1A and the rated voltage of 20V. Thus, to test at higher power, the minimum voltage is increased in order not to exceed the maximum current of 1A that can be handled by the SC. Some experimental results of the CPC testing on the Maxwell® PC5 stack I are presented in Figure 4.42 (7W & 7-20V), Figure 4.43 (10W & 10-20V) and Figure 4.44 (15W & 15-20V). In the CPC mode, the SC current, i_{SC}, has to be adjusted in a nonlinear fashion according to the SC terminal voltage, v_T, in order to maintain a SC power, p_{SC}, constant as P. The measurement results shown in Figure 4.42, Figure 4.43 and Figure 4.44 were recorded earlier in the work by using a lower spec LeCroy® WaveSurfer 424 oscilloscope (8bit), a LeCroy® differential voltage probe ADP 300 and a LeCroy® current probe CP150. The sampling period, T_{Samp}, was 0.2ms.

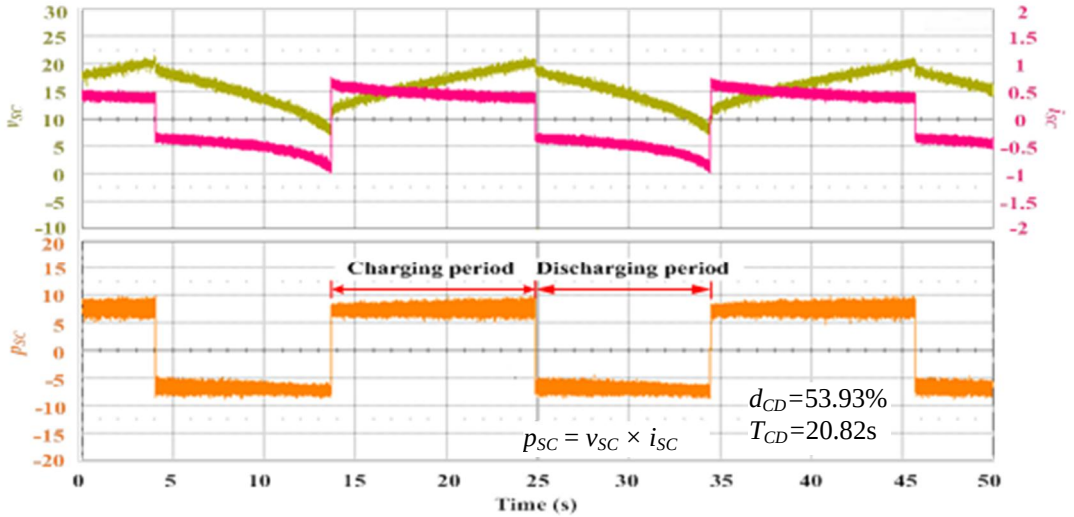


Figure 4.42 The voltage, current and power waveform of the Maxwell® PC5 stack I during the CPC tests at P = 7W, V_{SC_min} = 7V and V_{SC_max} = 20V

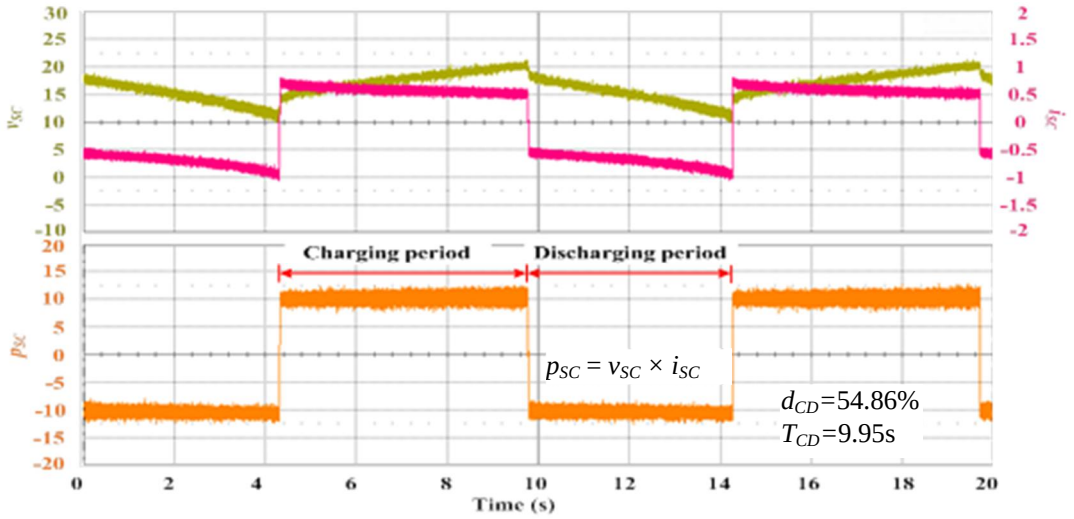


Figure 4.43 The voltage, current and power waveform of the Maxwell® PC5 stack I during the CPC tests at P = 10W, V_{SC_min} = 10V and V_{SC_max} = 20V

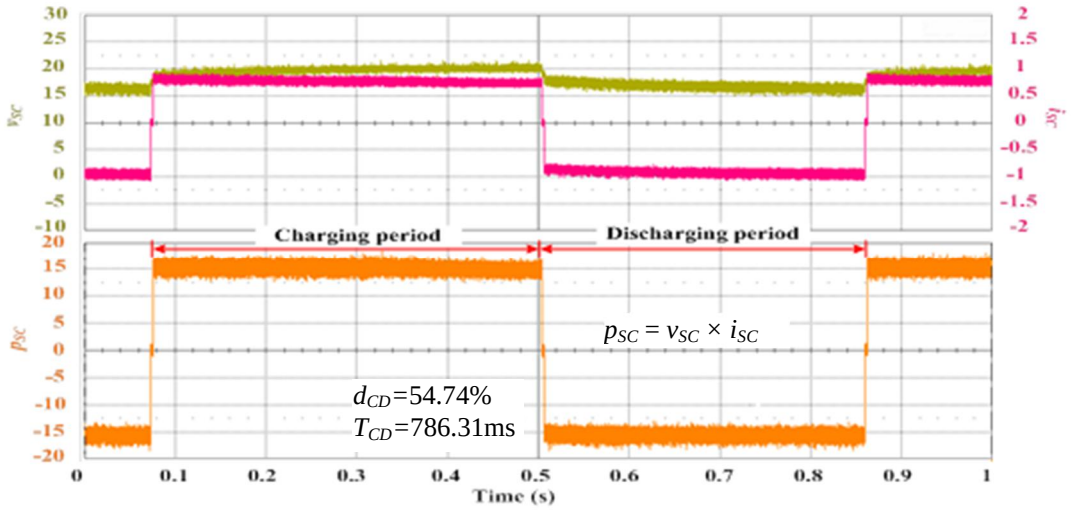


Figure 4.44 The voltage, current and power waveform of the Maxwell® PC5 stack I during the CPC tests at P = 15W, V_{SC_min} = 15V and V_{SC_max} = 20V

During the CPC mode, the SC stack is investigated under both natural cooling and forced cooling (i.e. using a small fan). The thermal imaging pictures for both cooling conditions are shown in Figure 4.45 when the power is at the maximum (15W). It can be seen that the inner SC cells get quite hot (47°C) in natural cooling condition. It is note that the SC temperature was observed on the paint black surface by using the Fluke® Ti25 thermal imager, which has accuracy of ±2°C.

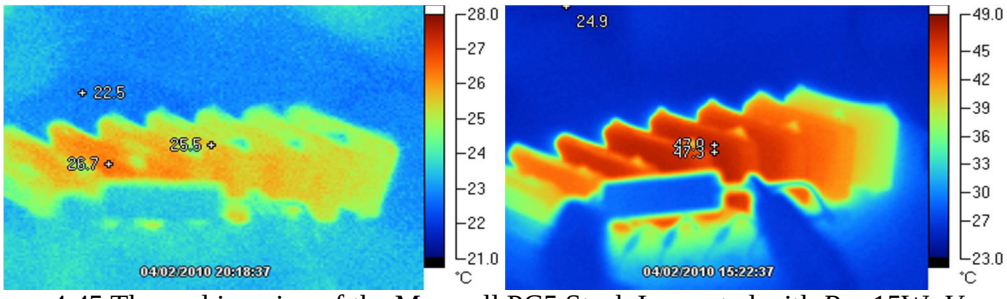


Figure 4.45 Thermal imaging of the Maxwell PC5 Stack I operated with P = 15W, V_{SC_min} = 15V and V_{SC_max} = 20V under forced cooling (left) and natural cooling (right) conditions

The experimental results including the cell temperature are presented in Table 4.12. The results are grouped under forced cooling and natural cooling conditions. The η_{RT} is estimated by using a charge-discharge duty cycle, d_{CD}, according to the duty cycle method as:

$$\eta_{EST\_Duty} = \frac{1}{d_{CD}} - 1 \tag{4.12}$$

Table 4.12 The estimated round-trip efficiency results from the d_{CD} of the Maxwell® PC5 stack I under the CPC method at various constant power level and min/max voltage settings

	P (W)	V_{SC_min}-V_{SC_max} (V)	T_{SC} (°C)	d_{CD} (%)	η_{EST_Duty} (%)
Forced Cooling	7	7-20	25	54.17	84.60
	7	10-20	25	53.14	88.18
	7	15-20	24	51.38	94.63
	10	10-20	25	55.12	81.42
	10	15-20	25	53.01	88.64
	15	15-20	26	55.37	80.60
Natural Cooling	7	7-20	35	53.93	85.43
	7	10-20	31	53.04	88.54
	7	15-20	32	51.47	94.29
	10	10-20	38	54.72	82.75
	10	15-20	37	52.42	90.77
	15	15-20	47	54.83	82.38

The test results show consistency with an increase of P and V_{SC_min}. Fixing the operating voltage range at 15-20V and increasing P from 7W to 10W or from 7W to 15W, reduces the η_{EST_Duty} further. However, fixing the P and increasing the V_{SC_min} (i.e. reducing the operating voltage range), increases the η_{EST_Duty} since the processed energy is reduced. At the lowest P level (7W) and at the smallest operating voltage range (15-20V), the SC has the highest η_{EST_Duty} for both cooling conditions. This is due to the low power and low energy being processed.

The overall η_{EST_Duty} under natural cooling is higher than under forced cooling. This η_{EST_Duty} improvement gives a reason to believe that there is the negative temperature coefficient (NTC) effect of the Maxwell® PC5 SC on its *ESR*. The NTC effect can be beneficial in providing thermal stabilization of a SC stack. As more power is processed, more losses heat up the device which then reduces its *ESR* slightly. Hence the losses reduce the temperature until the SC reaches a stable temperature operating point.

The CPC method is applied to the Maxwell® PC5 stack I and the estimated η_{RT} is observed during forced and natural cooling. Since the estimated η_{RT} based on the d_{CD} measurement is sensitive to the change of device temperature, the duty cycle method can track small changes in the overall SC stack *ESR* with any changes in environmental operating conditions.

4.3.2 The Maxwell® PC5 Stack II (8x2)

In this section, the Maxwell® PC5 stack II η_{RT} and E_{Loss_RT} are investigated to further study the NTC effect with the CPC method at a single power level and a single operating voltage range. The SC temperature, T_{SC}, is monitored for both the forced and the natural cooling conditions. The SC stack is tested at V_{SC_min}-V_{SC_max} between 15 to 20V and at P = 30W under both forced and natural cooling conditions continuously for approximately 80 minutes. Some CPC experimental results are presented in Figure 4.46 and Figure 4.47, under forced and natural cooling, respectively. The measurement results shown in Figure 4.46 and Figure 4.47 were recorded later in the work by using a high spec LeCroy® WaveRunner HRO 64Zi oscilloscope (12bit) with the T_{Samp} of 0.2µs. Two TENMA® 1:1 passive voltage probes configured to measure differential device voltage and a LEM® current probe

PR30 with 10 turns were used to capture voltage and current information. By increasing number of turns to 10 on the current probe, the probe sensitivity increases 10 times. The accuracy specified at the rated current of $20A_{RMS}$ can be applied to the current measurement in the 2-3A range. The voltage and current probes have accuracy of 0.2% and 0.4% when measuring the voltage between 15V to 20V and the current between 1A to 2A, so the measured power data may contain error of up to 0.6%. The efficiency and energy loss error can be less than 1.2%. For the accuracy validation of both voltage and current probes, a test procedure is detailed in Appendix C. For the cell temperature measurement and logging, the K-type thermocouple is used together with the PicoLog TC-08 data logger, which has the accuracy of 0.2% and the resolution of $\pm 0.1^0$C.

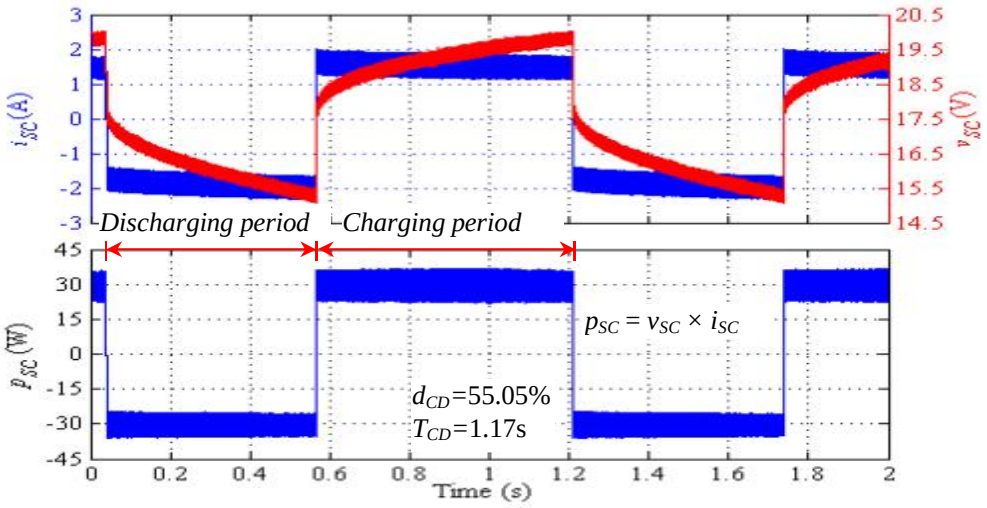


Figure 4.46 The voltage, current and power waveform of the Maxwell® PC5 stack II during the CPC tests under the forced cooling condition

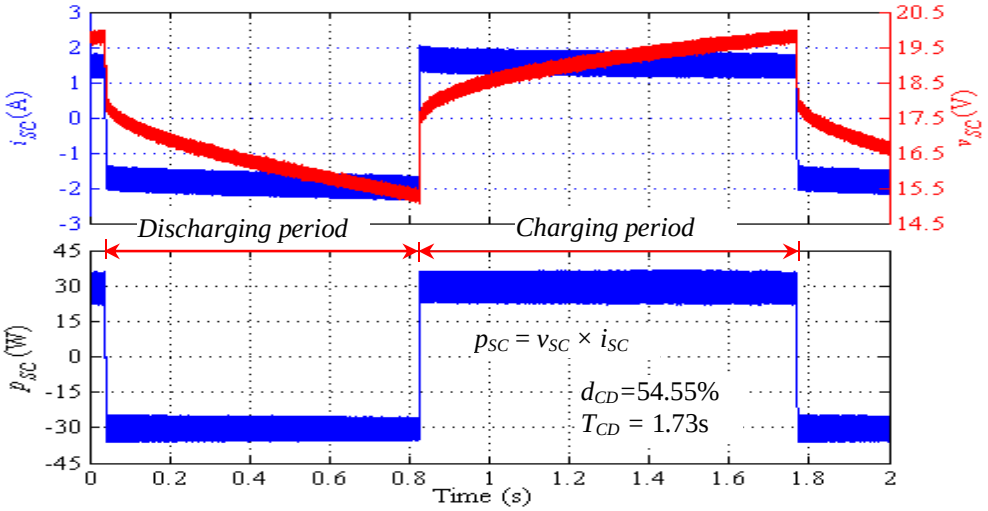


Figure 4.47 The voltage, current and power waveform of the Maxwell® PC5 stack II during the CPC tests under the natural cooling condition

Full experimental results including the cell temperature are presented in Table 4.13. By using (4.13) and (4.14), a round-trip efficiency and energy loss per charge-discharge cycle, η_{RT_EXP} and $E_{Loss\_RT\_EXP}$, are calculated for each operating point and are presented in Table 4.13.

$$\eta_{RT\_EXP} = \frac{-\int_0^{T_D} p_{SC}\,dt}{\int_0^{T_C} p_{SC}\,dt} = \frac{-P_{D\_avrg}T_D}{P_{C\_avrg}T_C} = \frac{-E_D}{E_C} \tag{4.13}$$

$$E_{Loss\_RT\_EXP} = E_C + E_D \tag{4.14}$$

In addition to (4.13), if p_{SC} is controlled constant during charging and discharging, the η_{RT_EXP} can be calculated easily from the average charging power, P_{C_avrg}, the average discharging power, P_{D_avrg}, charging period T_C and discharging period, T_D.

Table 4.13 The experimental results of 30W constant power cycling on Maxwell® PC5 stack II (20V 1F) (T_{Samp} equals to 0.2µs)

Condition	T_{SC} (°C)	T_{CD} (s)	V_{C_min} (V)	V_{C_max} (V)	P_{C_avrg} (W)	P_{D_avrg} (W)	η_{RT_EXP} (%)	$E_{Loss\_RT\_EXP}$ (J)
Forced cooling	26.5	1.089	16.61	18.99	29.42	30.47	82.7	3.09
	28	1.164	16.56	18.98	29.55	30.37	83.9	3.05
	28	1.158	16.57	18.99	29.49	30.39	83.9	3.03
	28	1.145	16.58	18.99	29.59	30.36	83.8	3.03
	28	1.145	16.58	19.01	29.57	30.37	83.9	3.01
	27.8	1.139	16.56	19	29.58	30.39	83.8	3.01
Natural cooling	55.5	1.726	16.40	19.08	29.54	30.40	85.5	4.05
	56	1.733	16.39	19.08	29.54	30.44	85.6	4.04
	56.3	1.734	16.40	19.08	29.59	30.43	85.5	4.07
	56.7	1.736	16.40	19.09	29.52	30.44	85.7	4.00
	56.8	1.734	16.39	19.07	29.56	30.43	85.5	4.06
	56.8	1.732	16.40	19.087	29.50	30.49	85.7	4.01

From Table 4.13, it can be seen that η_{RT_EXP} is increased by ≈2-3% as the test condition is changed from forced to natural cooling. Since the η_{RT_EXP} do not include the fan power, the η_{RT_EXP} improvement is explained by the decreased *ESR* when the

T_{SC} increases as discussed in the previous section. On the other hand, the SC stack $E_{Loss\_RT\_EXP}$ is increased by ≈30% (from ≈3J to ≈4J), which is due to an increase in the single charge-discharge period, T_{CD}, by 45% (from ≈1.1s to ≈1.7s). An increased in the T_{CD} at the same P level would result in higher energy loss. Note that from Table 4.13, the minimum and maximum ideal voltages, V_{C_min} and V_{C_max}, measured during the dead-time period, are also presented together with the P_{C_avrg} and P_{D_avrg}. These parameters are used in the round-trip efficiency and energy loss estimation process based on the SC voltage presented in Section 4.4.1.

The experimental result presented in this section will be used and compared with the round-trip efficiency and energy loss estimation results presented in Section 4.4.

4.4 Round-trip Efficiency and Energy Loss Estimation

In this section, the η_{RT} and E_{Loss_RT} estimation schemes presented in Section 2.6 are applied to the experimental data of the Maxwell® PC5 stack II shown in Section 4.3.2. The estimation schemes used are the Voltage-based, the Current-based and the Current-based with the FFT methods.

4.4.1 Estimation of η_{RT} and E_{Loss_RT} by the Voltage-based Method

To estimate η_{RT} and E_{Loss_RT}, the Electrochemical Impedance Spectroscopy (EIS) method is applied to the Maxwell® PC5 stack II again to determine the impedance-frequency information particularly at the DC bias voltage of 17.5V with the swept frequency from 10mHz to 10kHz. The 17.5V bias is chosen since it relates to the average voltage of the stack during the CPC testing (i.e. an operating voltage between 15V to 20V). The impedance result is represented by the simple RC model as the C and ESR versus frequency as shown in Figure 4.48.

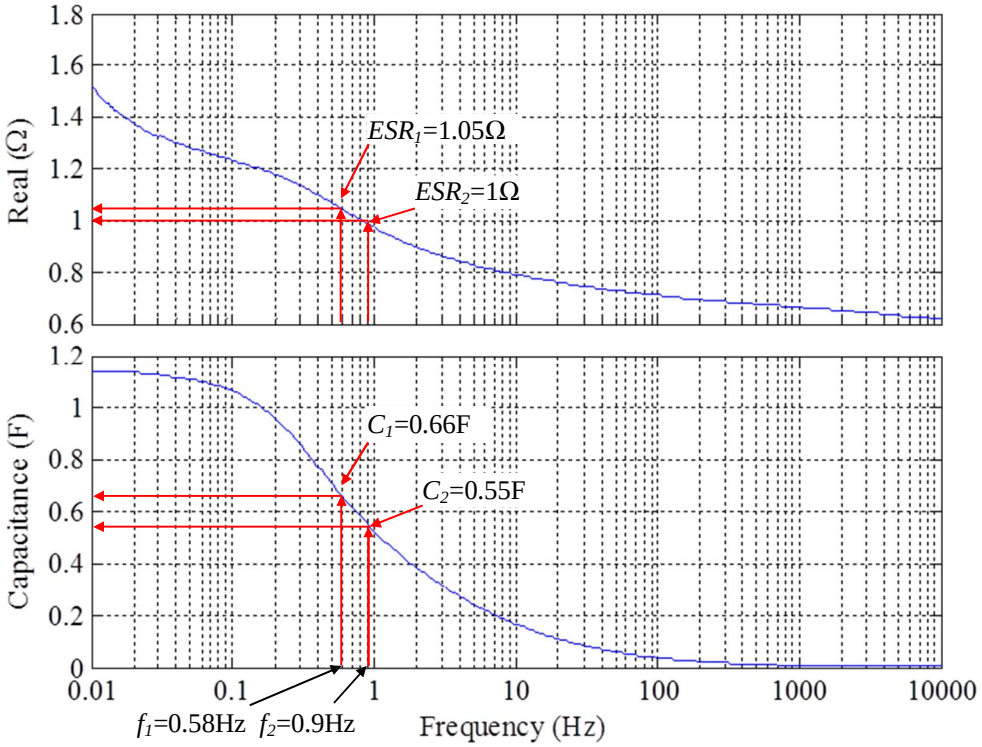


Figure 4.48 The *ESR* and the *C* versus frequency at 17.5V DC bias voltage of the Maxwell® PC5 stack II

From Figure 4.48, it can be seen that both the *ESR* and the *C* are reduced as frequency increases. This implies that the energy loss and the processed energy in the high frequency region are small. Choosing a frequency =1/T_{CD} (denoted as f_1 and f_2 for the forced and natural cooling conditions), an equivalent series resistance and capacitance, ESR_{Period} and C_{Period}, can be derived. They are presented in Table 4.14. The estimated round-trip efficiency and energy loss method are then calculated using the method of Section 2.6.1.2 and the ESR_{Period} and C_{Period}. Equations (2.30) and (2.31) are presented here again as (4.15) and (4.16):

$$\eta_{EST\_V} = \frac{-E_{D\_EST\_V}}{E_{C\_EST\_V}} \tag{4.15}$$

$$E_{Loss\_EST\_V} = E_{D\_EST\_V} + E_{C\_EST\_V} \tag{4.16}$$

For definition of the energy terms, see Section 2.6.1.2. This method is referred as 'Voltage-based'. It uses the V_{C_min}, V_{C_max}, P_{C_avrg} and P_{D_avrg} parameters (shown in Table 4.13) from the CPC experimental result to estimate round-trip efficiency $\eta_{RT\_EST\_V}$ and energy loss $E_{Loss\_EST\_V}$. The estimated results are presented in Table

4.14. It is noted that the charge-discharge cycling frequency f_{CD} is a reciprocal of T_{CD}.

Table 4.14 Data record of several charge-discharge cycles under the CPC of 30W of Maxwell® PC5 stack II showing the correlation of the η_{RT} and the E_{Loss_RT} between the experiment (from Table 4.13) and the Voltage-based estimation method

Condition	From the CPC test		From the EIS test		η_{RT} (%)	$\eta_{RT\_EST\_V}$ (%)	$\Delta\eta_{RT}$ (%)	E_{Loss_RT} (J)	$E_{Loss\_EST\_V}$ (J)	ΔE_{Loss} (%)
	T_{CD} (s)	f_{CD} (Hz)	ESR_{Period} (Ω)	C_{Period} (F)						
Forced cooling	1.089	0.918	1.005	0.540	82.7	82.09	-0.71	3.09	4.45	44.08
	1.164	0.859	1.013	0.559	83.9	81.89	-2.41	3.05	4.74	55.38
	1.158	0.864	1.012	0.557	83.9	81.92	-2.36	3.03	4.71	55.44
	1.145	0.873	1.011	0.547	83.8	81.93	-2.19	3.03	4.67	54.22
	1.145	0.874	1.011	0.555	83.9	81.97	-2.24	3.01	4.71	56.58
	1.139	0.878	1.010	0.553	83.8	81.93	-2.18	3.01	4.72	56.62
Natural cooling	1.726	0.579	1.067	0.664	85.5	80.87	-5.38	4.05	6.59	62.84
	1.733	0.577	1.068	0.665	85.6	80.83	-5.52	4.04	6.66	64.71
	1.734	0.577	1.068	0.666	85.5	80.84	-5.42	4.07	6.63	62.72
	1.736	0.576	1.068	0.665	85.7	80.85	-5.66	4.00	6.66	66.37
	1.734	0.577	1.068	0.666	85.5	80.82	-5.49	4.06	6.61	63.03
	1.732	0.577	1.068	0.665	85.7	80.84	-5.61	4.01	6.63	65.38

From Table 4.14, it can be seen that for the estimated efficiencies, the prediction falls to 2-3% error range during forced cooling and to with 5-6% during natural cooling. This seems to be acceptable. One possible explanation for the good efficiency estimation is that when applying (4.15), the C_{Period} parameters from both $E_{C\_EST\_V}$ and $E_{D\_EST\_V}$ terms cancel out, so the error depending on this capacitance change is minimized. However, the 2-3% and the 5-6% error in the η_{RT} estimation mean quite large errors in determining the actual energy loss, which are 44-57% for forced cooling and 62-67% for natural cooling. The estimation method needs to be refined further by focusing on reducing the error in the estimated E_{Loss_RT} rather than η_{RT}. This will be presented in the next section.

4.4.2 Estimation of η_{RT} and E_{Loss_RT} by the Current-based Method

In this section, the estimated round-trip and energy loss method presented in Section 2.6.1.3 is employed. The measured current i_j at each sampling point j and ESR_{Period} are used to calculate an instantaneous power loss P_j as (4.17).

$$P_j = i_j^2 ESR_{Period} \tag{4.17}$$

Indeed, by accumulating this power loss for N_{Samp} sample points over the T_{CD}, the total power loss is obtained. By multiplying this quantity with the sampling time, T_{Samp}, the energy loss $E_{Loss\_EST\_I}$ is estimated as (4.18).

$$E_{Loss\_EST\_I} = \sum_{j=1}^{N_{Samp}} \left(P_j\right) T_{Samp} \tag{4.18}$$

Since this method only employs the current information from the CPC experiment, it is referred as the 'Current-based' energy loss estimation. The estimated results are presented in Table 4.15 with the T_{Samp}=0.2µs. This is obtained from the experimental results presented in Figure 4.46 and Figure 4.47. The formula contains 0.8% error since it has a square of the measured current.

Table 4.15 Data record of several charge-discharge cycles under constant power 30W of Maxwell® PC5 stack II showing the correlation of the E_{Loss_RT} between the experiment (from Table 4.13) and the Current-based estimation method with T_{Samp} equals to 0.2µs.

Condition	From the CPC test		From the EIS test	E_{Loss_RT} (J)	$E_{Loss\_EST\_I}$ (J)	ΔE_{Loss} (%)
	T_{CD} (s)	f_{CD} (Hz)	ESR_{Period} (Ω)			
Forced cooling	1.089	0.918	1.005	3.09	3.22	4.19
	1.164	0.859	1.013	3.05	3.45	11.33
	1.158	0.864	1.012	3.03	3.43	12.70
	1.145	0.873	1.011	3.03	3.45	10.57
	1.145	0.874	1.011	3.01	3.45	10.80
	1.139	0.878	1.010	3.01	3.44	11.24
Natural cooling	1.726	0.579	1.067	4.05	5.71	41.04
	1.733	0.577	1.068	4.04	5.73	41.85
	1.734	0.577	1.068	4.07	5.74	40.84
	1.736	0.576	1.068	4.00	5.75	36.14
	1.734	0.577	1.068	4.06	5.74	43.41
	1.732	0.577	1.068	4.01	5.75	39.86

From Table 4.15, for the same operating points considered earlier in Table 4.13, the error between the experimental and the estimated results reduce from 44-57% to 4-13% for forced cooling and 62-67% to 36-44% for natural cooling. One of reasons for this improvement is the removal of the capacitance term from the loss estimation. In the low frequency range, the EIS result shows that the capacitance strongly depends on the DC bias voltage in a nonlinear fashion. Therefore, the equivalent capacitance read from a single DC bias voltage which is used in the Voltage-based loss estimation presented earlier is insufficient to account for this nonlinearity. This, in turn, causes large error output.

It can also be seen from the Current-based loss analysis, that the averaged power terms (i.e. P_{C_avrg} and P_{D_avrg}) are excluded. These power terms are most likely to contain the sum of error from both voltage and current measurements as the power is a product of current and voltage. Therefore, by excluding the averaged power terms, an energy loss estimation based on the current alone is better than that based on the Voltage-based method. Next, the Current-based with the FFT method is applied to the CPC experimental results to estimate the E_{Loss_RT}.

4.4.3 Estimation of η_{RT} and E_{Loss_RT} by the Current-based with the FFT Method

Instead of processing the measured SC current in the time domain, it can be processed in the frequency domain. The estimated round-trip and energy loss method presented in Section 2.6.1.4 is employed. By applying the Fast Fourier Transform (FFT), fundamental, harmonics and DC components of the current are obtained separately at a specific frequency. Using the fundamental and the harmonic currents I_k with the ESR_k extracted from EIS method at a matched frequency, a power loss, P_{IFFT_k}, of each k^{th} harmonic can be calculated by (4.19). Consequently, by accumulating this power loss for N_{Har} spectrums, the total power loss is obtained and by multiplying this quantity with T_{CD}, the energy loss, $E_{Loss\_EST\_IFFT}$, is estimated by (4.20).

$$P_{IFFT\_k} = I_k^2 ESR_k \tag{4.19}$$

$$E_{Loss\_EST\_IFFT} = \sum_{k=1}^{N_{Har}} \left(P_{IFFT\_k} \right) T_{CD} \tag{4.20}$$

The FFT algorithm is applied to all the experimental currents presented earlier in Table 4.13. Two sets of the harmonic spectrums of the SC currents are shown in Figure 4.49, which are taken under forced and natural cooling conditions. From Figure 4.49, the harmonic currents at the frequencies over 10Hz are very small when compared with the amplitude of the fundamental currents. Therefore, if the high frequency harmonics are calculated together with the *ESR* over at the same frequency range by (4.19), they contribute to an insignificant power loss. This is indicated in Figure 4.50, particularly beyond 10Hz. However, the loss estimation is calculated using up to 100 harmonics, and this should be sufficient to represent the majority of the energy loss within an SC device. The estimated results are presented in Table 4.16. The formula contains 0.8% error since it has a square of the measured current.

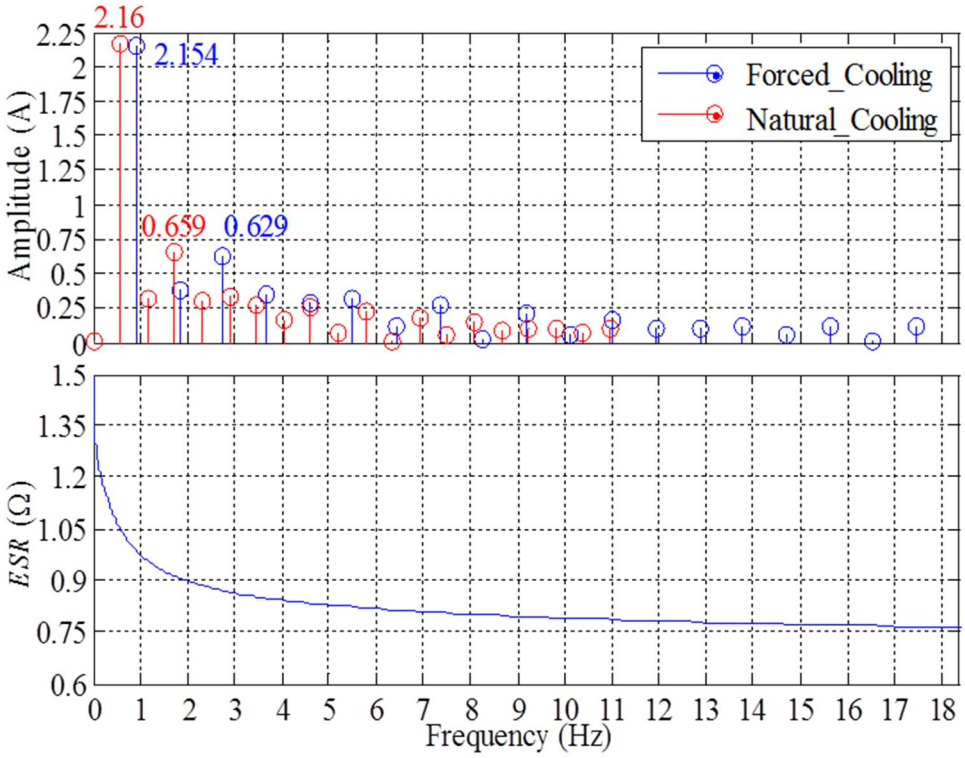


Figure 4.49 The FFT harmonic spectrums of the SC currents operated in the CPC mode during the forced and the natural cooling conditions (presented up to 20 harmonics) and the *ESR* versus frequency (Figure 4.48)

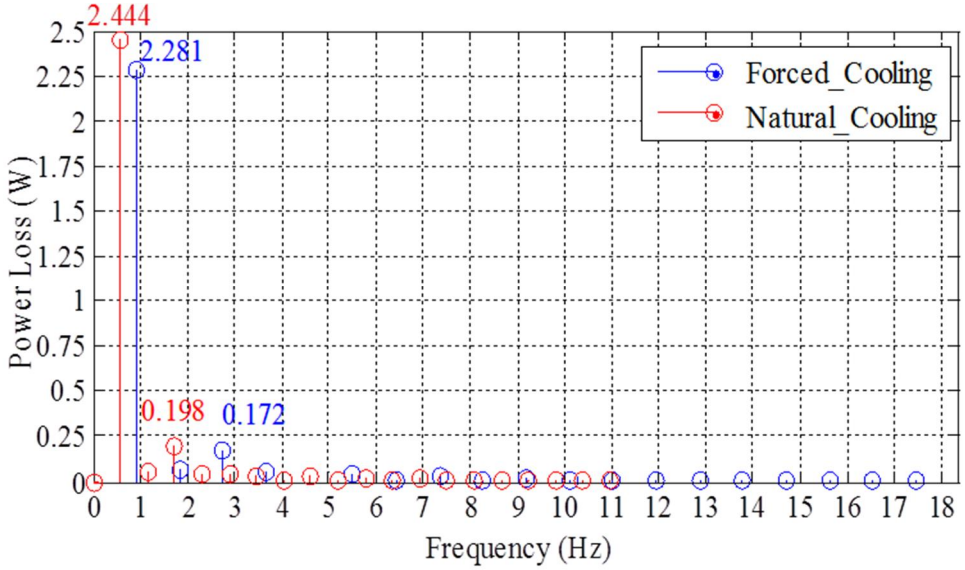


Figure 4.50 The power loss harmonic spectrums of the SC operated in the CPC mode during the forced and the natural cooling conditions (presented up to 20 harmonics)

Table 4.16 Data record of several charge-discharge cycles under constant power 30W of Maxwell® PC5 stack II showing the correlation between E_{Loss_RT} as given by the experiment (from Table 4.13) and the Current-based with the FFT method

Condition	T_{CD} (s)	E_{Loss_RT} (J)	$E_{Loss\_EST\_IFFT}$ (J)	ΔE_{Loss} (%)
Forced cooling	1.089	3.09	3.08	-0.37
	1.164	3.05	3.34	7.75
	1.158	3.03	3.32	9.09
	1.145	3.03	3.34	7.14
	1.145	3.01	3.35	7.64
	1.139	3.01	3.32	7.57
Natural cooling	1.726	4.05	5.17	27.67
	1.733	4.04	5.20	28.64
	1.734	4.07	5.20	27.78
	1.736	4.00	5.22	23.4
	1.734	4.06	5.20	29.94
	1.732	4.01	5.22	26.9

In Table 4.16, the Current-based method with the FFT processing is applied to estimate E_{Loss_RT} for the same operating points presented earlier in Table 4.13. The error between the experimental and the estimated results are reduced further to 0.3-9% for the forced cooling and 23-30% for the natural cooling. This improvement is because of the derivation of the *ESR*s from the measured impedances at a large number of frequency points so minimizing the effect of the error in the loss estimation. The difficulty of using this method is described in Section 2.6.1.4.

In summary, this E_{Loss_EST} method yields very precise estimated results during forced cooling as the average error is approximately 6.4%. However, if the testing condition is changed to natural cooling, the estimation results are poor as the average error is approximately 27.4%. In the next section this method is refined with a procedure to update the device *ESR* information to improve the estimation.

4.4.4 Refined Methodology to Improve the Estimated Energy Loss

4.4.4.1 Detecting Changes in Operating Conditions

During the constant power cycling tests, a temperature of one cell within the stack is monitored and recorded continuously for approximately 2.5 hours (Figure 4.51). Using this temperature to represent the overall stack temperature, it is shown that once the system reaches its steady-state condition, the average temperatures during forced cooling and natural cooling of the stack are ≈ 28°C and 57°C. During the test, the voltage and the current information of the stack are also taken at about 5-minute intervals, which results in 28 time (as denoted as a cross sign × in Figure 4.51). From (4.13) and (4.14), both η_{RT} and E_{Loss_RT} are calculated and presented in Figure 4.52. Consequently, by processing the recorded current and through (4.15)-(4.20), both the experimented and estimated E_{Loss_RT} can be plotted against the operating time as in Figure 4.53. These are in agreement with those presented in the previous section (Table 4.14, Table 4.15 and Table 4.16) and indicate that changes either in the efficiency or the energy loss error can be used for monitoring the environmental conditions and/or the health status of the SC module.

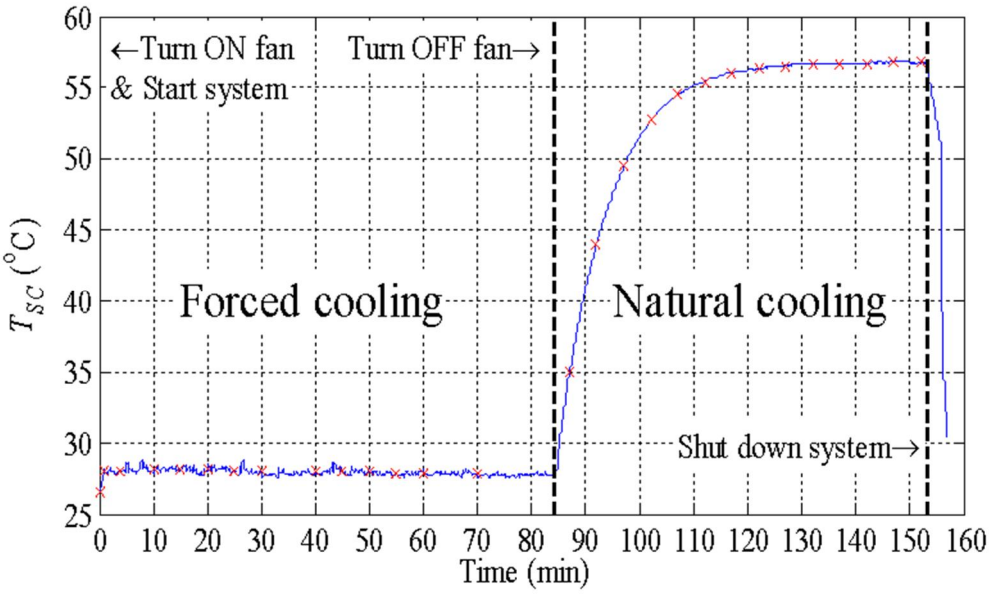


Figure 4.51 Temperature of one of cell within the stack during the CPC test and the numbers (×) on the curve represent data points recorded.

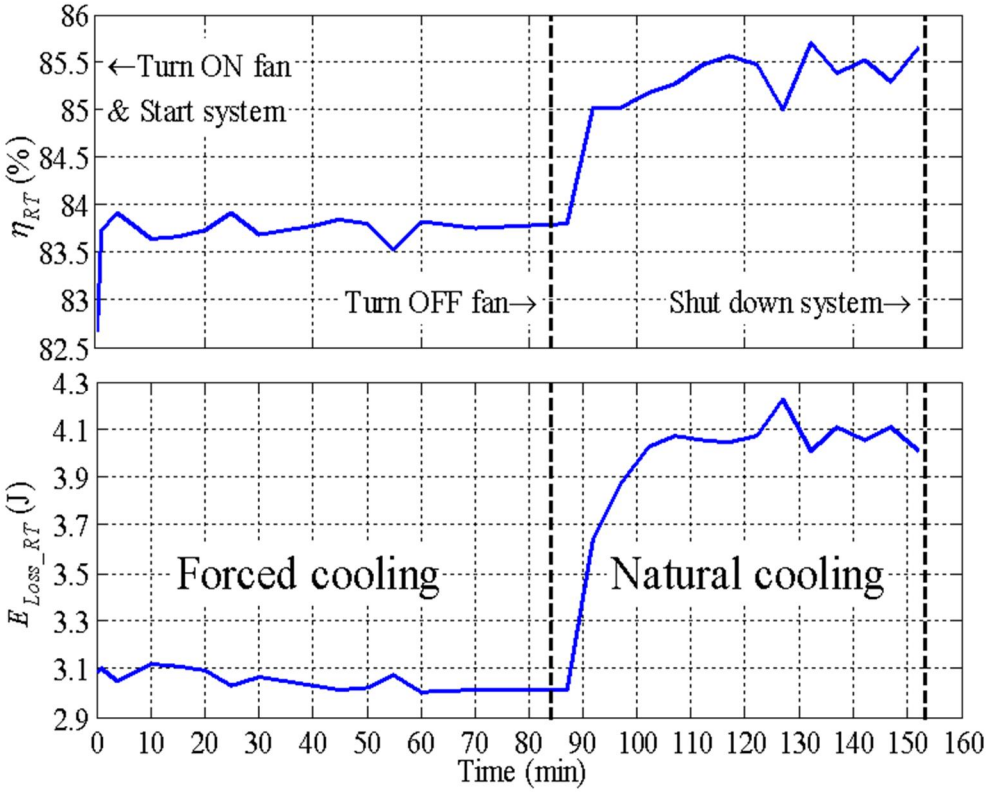


Figure 4.52 The experimental round-trip efficiency and the energy loss of the Maxwell® PC5 stack II versus the operating time

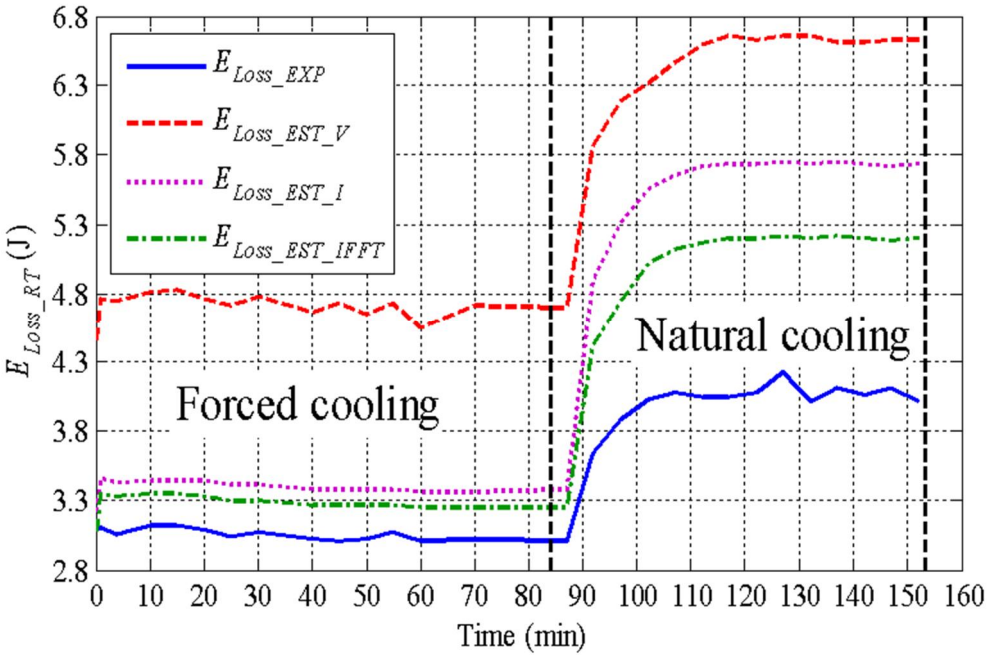


Figure 4.53 Energy loss during constant power cycling over 2 hours period (E_{Loss_RT} is experimental energy loss, $E_{Loss\_EST\_V}$ is the Voltage-based estimated energy loss, $E_{Loss\_EST\_I}$ is the Current-based estimated energy loss and $E_{Loss\_EST\_IFFT}$ is the Current-based with FFT estimated energy loss)

4.4.4.2 Method to Account for Changes in *ESR* Depending on Device Temperature

From Figure 4.53, the losses derived from the current-based method with and without the FFT processing are in good agreement with the experimental results only under forced cooling period. As the temperature of the stack increases under natural cooling, the error between the estimated and the experimental losses increases dramatically. This implies that the *ESR* used in the analysis during natural cooling is an overestimation. According to [51], the SC's nonlinear impedance characteristic is not only affected by applied frequency and DC-bias voltage, but also by operating temperature. Thus, all factors should be taken into account in order to estimate the energy loss accurately. Additionally from [51], in low frequency range (<10Hz), the *ESR* evolution of SCs is affected mostly by operating temperatures of >40°C. Meanwhile, the temperature has a small effect on the equivalent capacitance parameter, so this will not be taken into account. Indeed, it can be seen that in the power cycling experiment, the SC operating periods fall into this low frequency range (≈1Hz) for all presented operating points, so the estimated energy loss results presented earlier should be attenuated.

The voltage steps of the SC stack due to *ESR* are observed during the CPC testing. The diagram presented in Figure 4.54 is used to indicate different IR voltage step happens when the mode is changed from charging to discharging or vice versa. From Figure 4.54, V_{T_Cmin} and V_{T_Cmax} are the minimum and the maximum terminal voltage during charging, and V_{T_Dmin} and V_{T_Dmax} are the minimum and the maximum terminal voltage during discharging.

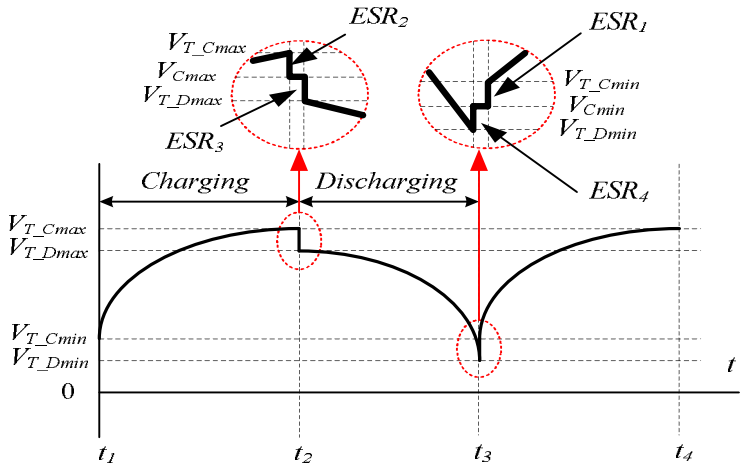


Figure 4.54 The *ESR* observation from the SC voltage curve when the mode toggling occurs

Since the amplitudes of transient current and voltage are known, the *ESR*s at each voltage step can be determined and are presented in Figure 4.55 versus time. Two schemes of attenuated resistance are applied in order to scale down estimated energy loss. There are '*ESR* group averaging' (using average *ESR*s observed during the forced cooling and natural cooling periods), and '*ESR* from each point' (using *ESR* at each point to do the attenuation). First, by using all ESR_1, ESR_2, ESR_3 and ESR_4, the average *ESR*s are calculated for all operating points and are presented as 'ESR_{avrg}' in Figure 4.56. Next, all averaged *ESR*s are re-averaged in groups for the forced cooling and the natural cooling conditions separately. These are denoted as 'ESR_{avrg_f}' and 'ESR_{avrg_n}' in Figure 4.56 and are 0.6388Ω and 0.5628Ω, respectively.

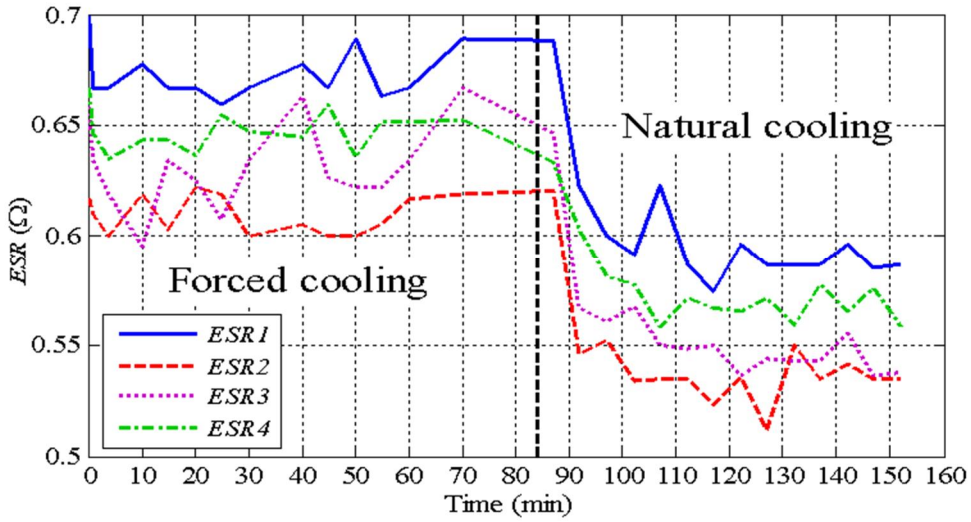


Figure 4.55 The *ESR*s derived from voltage step during mode change: ESR_1 at start charging; ESR_2 at stop charging; ESR_3 at start discharging; ESR_4 at stop discharging

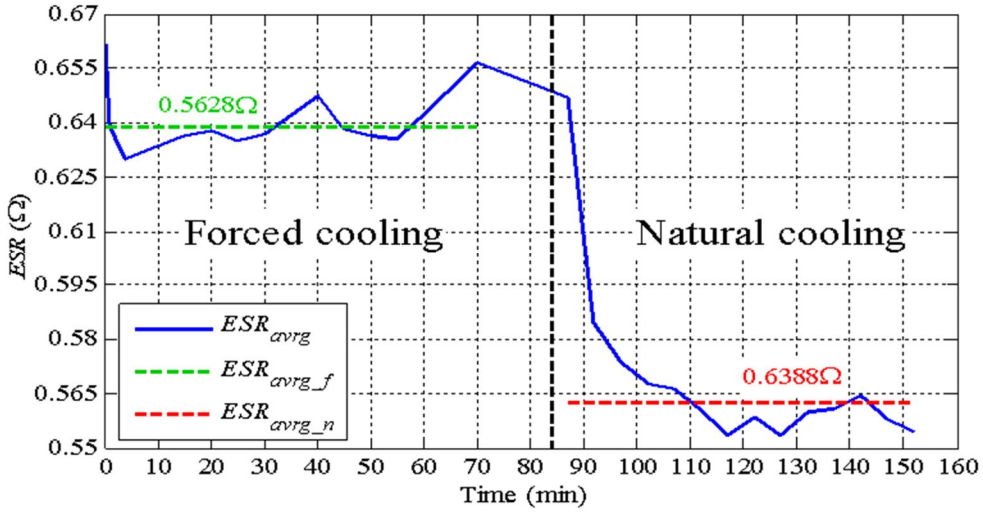


Figure 4.56 The averaged *ESR* calculated from each testing point covering both the forced and the natural cooling conditions and the average *ESR*s over forced cooling and natural cooling conditions (0.5628Ω and 0.6388Ω)

The estimated energy loss error between the experimental results and the estimated from the Current-based method with the FFT processing, with two schemes of *ESR* attenuation, are shown in Figure 4.57. The high discrepancies under the natural cooling are reduced dramatically to less than 10% for both the group average and the "each-point technique". The total average error over the test time is reduced to approximately 4.7% for both the group average and "each-point technique".

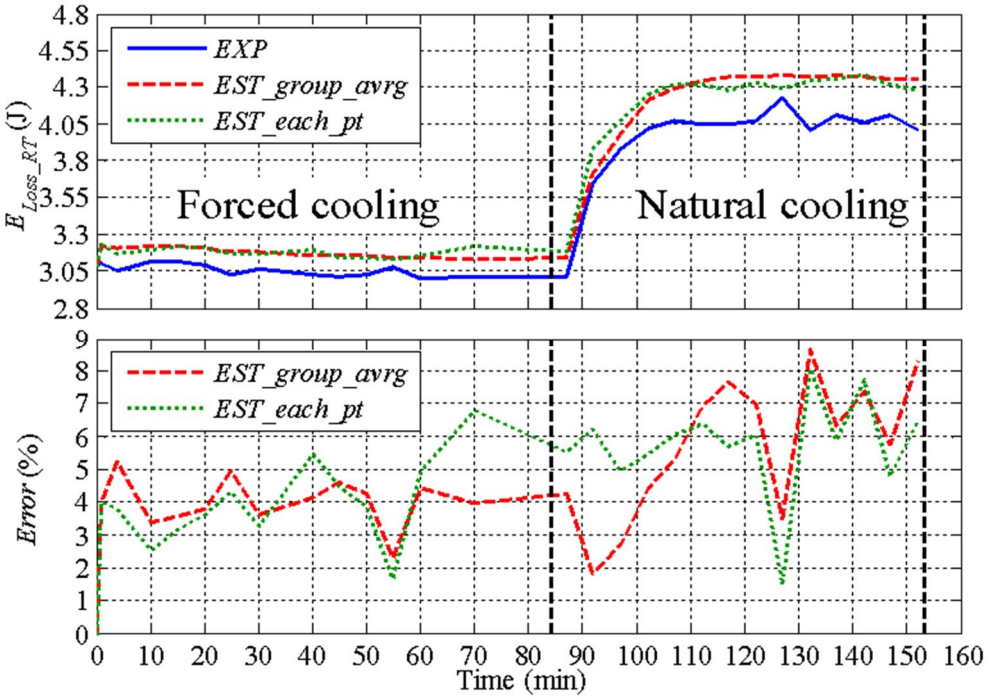


Figure 4.57 The energy loss error between the experimental and the estimated results

4.5 Conclusion

In this chapter characterization results have been presented according to three characterization objectives: to identify model parameters representing the short-term and long-term SC behavior, which can then be used to evaluate the round-trip efficiency and energy loss in relevant working conditions for any given constant power application. The experimental results representing the short-term behavior are used in the model identification process to derive the model parameters.

To identify the model parameters representing short-term behavior, the electrochemical impedance spectroscopy method (EIS) and the pulse constant current method (PCC) are used. Firstly, the EIS method is applied to a pool of available supercapacitor type devices each representing a different manufacturing technology. The impedance-frequency results represented by the assuming the single RC (complex impedance) model show that the applied DC-bias voltage has an effect on the model parameters of most devices. For the Maxwell® devices which are based on organic electrolyte, the applied DC-bias voltage has a positive effect on the device characteristics as the bias voltage helps reduce the *ESR* which is equivalent to making the energy extraction more efficient, and increase the *C* which means that as the device charges more energy can be stored at the same voltage. The reduced *ESR* and the increased *C* are in the tolerance range specified in the datasheet (±25% for the resistance and ±20% for the capacitance). On the other hand, for the supercapattery which is based on aqueous electrolyte, the applied DC-bias voltage has a negative effect to the device characteristics, either increasing the *ESR* or reducing the *C* or both. However, the changing effect (in %) of DC-bias voltage on the supercapattery stack device parameters is smaller than that for the Maxwell® devices.

Second step is to apply the PCC method to the Maxwell® PC5 stack II and the supercapattery stacks I and II. The PCC voltage response during the relaxation period is used to derive the model parameters. It was found that the voltage response of the PCC-derived models fit the experiment results very well.

Later, the EIS-derived models of the Maxwell® PC5 stack II and the supercapattery stack I and II are compared with the corresponding PCC-derived models. For the

Maxwell® PC5 stack II, the difference in frequency and pulse response of both the EIS-based and the PCC-based models yield very good matching with the corresponding experimental results providing that the results obtained with similar level of DC bias voltage are considered. For the supercapattery stack I, there is a small mismatch between the EIS-based and the PCC-based models as indicated in the frequency response testing. This small mismatch yields a large difference in voltage response to the large signal tests (i.e. PCC). For the supercapattery stack II, there is a large mismatch between the EIS-based and the PCC-based models. Some of the mismatch could be explain by the continuous changing in device property with time, which could have been caused by imperfect device sealing (electrolyte evaporation) and imperfect contact at the device terminals (crocodile clips) which would have impacted the *ESR* precision later addressed by fitting the device with standardized terminals.

To characterize the long-term behavior of the Maxwell® PC5 stack II and the supercapattery stack I, the constant voltage method (CV) is used. The results indicate that the energy retention capability of the Maxwell® technology is greater than the supercapattery technology as indicated by the higher derived *EPR* value (MΩ range in comparison with 10kΩ range), but the supercapattery device *EPR* was found to be consistent with other aqueous electrolyte supercapacitors (ELIT®, not shown in the thesis). The supercapattery device has been further investigated with the CV-with-floating-current-process. The results show lower *EPR* than those derived from the conventional CV method. It can be concluded that the high self-discharging characteristic of the supercapattery makes the device unsuitable for stand-by applications (e.g. UPS). Nevertheless, this high self-discharging characteristic which increases as voltage reaches the maximum allowed cell voltage has a positive effect providing an intrinsic nonlinear self-balancing cell voltage mechanism for a large supercapattery stack, which means a stack will not need any cell voltage balancing circuitry, keeping therefore the cost low.

Since real applications demand a given power to be processed, the constant power cycling method (CPC) was also assessed and its performance evaluated when used with the Maxwell® PC5 stack I. The experimental results indicate that the round-trip efficiency is increased if low power and low energy (i.e. reduce operating voltage

range) are processed. At higher power, as the testing condition is changed from the forced to natural cooling which results in higher device temperature, the efficiency increases for the same operating conditions. The reasons behind the efficiency incremental improvement required further investigations into the loss mechanism of the Maxwell® PC5 stack II. First the methods to estimate the energy loss in a single charge-discharge cycle of the SC stack under the CPC control are presented. The methods are divided into 3 approaches: voltage-based, current-based and current-based-with-FFT. The estimated energy losses are then compared with those obtained from the experiment. It is shown that the estimation based on current is more accurate than the voltage-based approach since only the real part of the SC impedance needs to be used, which was only slightly affected by the DC-voltage bias. In particular, the current-based-with-FFT estimation shows the most accurate result as it utilizes multi-frequency points to estimate the energy loss. However, all energy loss estimated methods show that the error increases significantly when the processed power increases which is consistent with a change/increase of the operating temperature of the SC stack. The error of the most accurate method increases to ≈27.4% average when changing from the forced to natural cooling. Therefore, two schemes of adjusting the device resistance (which is obviously changing compared to the one determined via EIS when device was at ambient temperature) are derived, based on the variation of voltage steps during device current steps at cycle change. These are referred as the '*ESR* group averaging' and '*ESR*-from-each-point'. The average error after adjusting the ESR is reduced to 6.3%. Indeed, the attenuation scheme seems to be very effective against temperature under natural cooling; the error is reduced by 17%, which proves clearly that the method counteracts the effect of temperature on *ESR* change. Note that the modeling research into the variation of parameters with temperature is out of the scope of this thesis as it requires more precise temperature control and sensor equipment such as climate chambers, calorimeters etc.

Chapter 5 Voltage Equalizing in Electrochemical Cell

5.1 Introduction

In this chapter the unbalanced cell voltage problem in series-connected supercapacitor stacks is discussed. A solution to this problem is to apply a voltage equalizer across the stack. Several voltage equalizer types have been proposed in literature, which are the passive-dissipative, the active-dissipative and the active-regenerative. These equalizer types are discussed in Section 5.3. Trade-offs in size, weight, efficiency, modularity and control complexity of each topology have been reported in literature. However, it is found that investigation of efficiency improvement versus increase of complexity/cost has not been sufficiently reported. Therefore, the aim of this chapter is to investigate the design and operation of a single-switch flyback voltage equalizer topology, which will be presented in Section 5.4 and 5.5. In Section 5.6, the trade-offs between the equalization time, the effectiveness of equalization (i.e. maximum voltage deviation) and the total energy loss of both the equalizer and stack are investigated. In Section 5.6.4, the performance comparison against an active-dissipative voltage equalizer is also investigated.

5.2 Factors that Causes an Unbalanced Cell Voltage Problem within a Series-connected Supercapacitor Stack

Any applications, for example, UPS [94] and electric transportation [95,96], require high voltage battery and supercapacitor systems consisting of small voltage units/cells. Due to the low voltage of small batteries and supercapacitors, cells must be connected in series. However, operating stacks of series-connected battery or supercapacitor cells over a long time causes an uneven change of behavior among the cells [96]. These changes will cause an unbalanced cell voltage condition, which leads to earlier degradation cell performance [53]. In particular, any cell that experiences the highest voltage and/or has smaller capacitance will have the degradation effect further amplified. In [97], three main parameters which cause cell voltage unbalance of supercapacitors are:

- Variation of capacitance, *C*
- Variation of equivalent series resistance, *ESR*
- Variation of equivalent parallel resistance, *EPR*, which is used to represent both a leakage current and self-discharging rate

To illustrate an uneven voltage distribution due to capacitance variation only, a simulation is done in PSIM®. Four ideal capacitors having capacitance values within a ±5% tolerance band (0.525F, 0.5F, 0.5F, 0.475F) are connected in series. The stack is charged with a constant current of 5A, starting from a completely discharged condition. The voltage deviation of each cell is presented in Figure 5.1. At the end of the charging process, the standard deviation (*STD*) of the cell voltage of the stack reaches 11% and the maximum cell voltage deviation ($\Delta V_{Max}=V_{Max}-V_{Min}$) is 0.271V while the average voltage, $V_{Average}$ is 2.7V, as presented in Table 5.1.

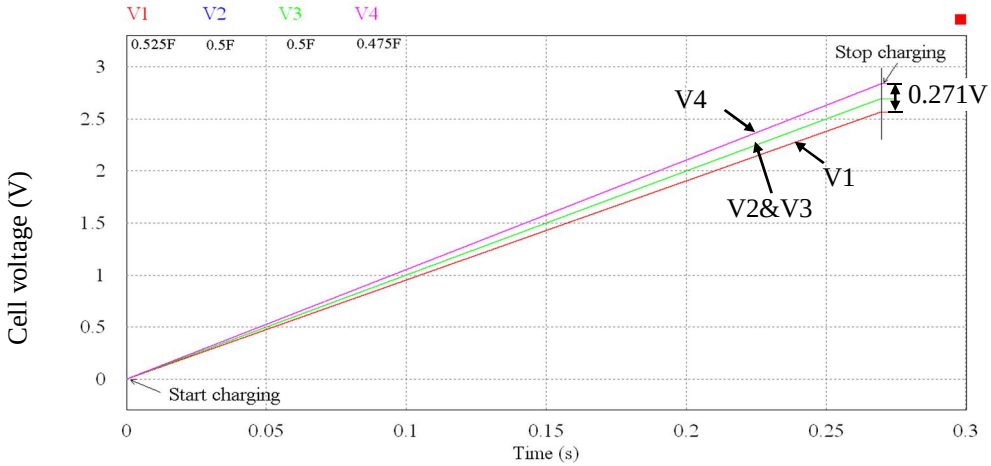


Figure 5.1 Cell voltage unbalance for 4 series-connected supercapacitors (0.525F, 0.5F, 0.5F and 0.475F)

Table 5.1 Individual cell voltage after constant current charging 5A without the equalizer

Parameter	Value
V1	2.568V
V2	2.697V
V3	2.697V
V4	2.839V
$V_{Average}$	2.700V
$\Delta V_{Max}=V_{Max}-V_{Min}$	0.271V
STD	11.04%

Cell voltage variation may be even more serious if there is high *ESR* deviation problem in the stacks when they are operating under constant power conditions (e.g. as in load-levelling application), where the current varies inversely proportional to stack voltage to maintain the power constant.

Different self-discharging characteristic of each cell of a series-connected supercapacitor stack is another factor that causes an unbalance cell voltage condition. In grid-interface applications where the voltage of the stack is maintained constant during stand-by mode (e.g. in an uninterruptible power system (UPS) [94]), the loss of charge due to self-discharging characteristic of devices is compensated by an external source. Each cell will be compensated with the same amount of charge (i.e. same charging current) since they are connected in series. However, the devices with higher leakage current will have their voltage slowly decreased while the devices with lower leakage current will have their voltage slowly increased to maintain the

overall stack voltage [95]. The self-discharging characteristic also affects the cell voltage deviation when the stack is left un-used (i.e. for a relaxation period).

Even though a cell characteristic matching process may be applied initially before the stack is assembled, a perfect matching is difficult to achieve due to limitation in manufacturing standards, and different aging and storage conditions of each cell [52]. An overvoltage condition will shorten a particular cell's life, which later will affect the life of whole stack. In order to counteract this problem, it is necessary to stop the charging process when the weakest cell reaches the maximum voltage level. Meanwhile, an under voltage condition occurring in the other cells within the same stack will reduce the energy storage capability of the whole stack. Therefore, to operate the energy storage stack safely and effectively, it is necessary to have a voltage equalizer attached to the stack.

In [94-96,98], the cell voltage variation of supercapacitor stacks have been observed and reported in different applications. In [94], the stack is used in a UPS application without any voltage equalizers attached. However, the maximum operating stack voltage should be reduced under the rated condition for safety reasons [94]. By doing this, the power capacity of the stack is decreased and the number of series-connected cell is increased which indicate poor use of devices and additional cost. In [95,96], the stack is tested in transportation applications. In [95], the cell voltage condition of the stack is not seriously unbalanced since it has gone through off-line balancing before using the stack. The voltage deviation of the stack after 19 months increased slightly, but cell voltage equalization is required to perform periodically. In [98], the authors use a statistical approach to analyze the impact of manufacturers' *EPR* and *C* tolerance on the life expectancy of supercapacitors. The results show that the life expectancy increases dramatically by applying voltage equalizers, which makes the influence of capacitor tolerance and self-discharge rate becomes negligible.

A voltage equalizer is required in order to the maintain stack condition and maximize its performance. Therefore, several voltage equalizer topologies and their trade-offs will be discussed in the next section.

5.3 Voltage Equalizers

5.3.1 Dissipative Voltage Equalizers

There are many types of voltage equalizers that have been proposed that can be categorized as dissipative and regenerative. In the dissipative type, the equalizers can be either passive or active. The passive-dissipative types rely on passive components such as resistors (or so called bleeding resistors) and Zener diodes connected in parallel to each cell [98,99], as presented in Figure 5.2(a)-(b). These equalizers dissipate all the excess energy and increase leakage current of each cell, but their advantage is simplicity. These voltage equalizers are, therefore, inapplicable to applications where efficiency is an important issue. More detailed analysis of selected value of bleeding resistors are presented in [98].

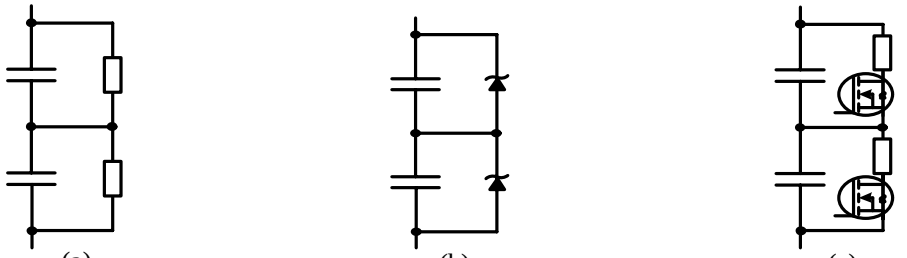


Figure 5.2 Dissipative voltage equalizers (a) shunt resistor (b) Zener diode (c) shunt resistor with active switches

On the other hand, active-dissipative equalizers rely on controlled switches. Figure 5.2(c) shows an active-dissipative example [100], as employed widely by many supercapacitor stack manufacturers. This equalizer burns the excess incoming energy into the resistor attached to the cell in order to limit the cell voltage to a predefined level. Comparing this equalizer with the passive ones, it is more accurate and versatile and slightly more efficient.

However, if dissipative voltage equalizers are employed in a large-number series-connected supercapacitors stack, the dissipated energy will cause thermal management problems. This problem, in turn, increases the cost, size, and cooling equipment design of the system. Therefore, active-regenerative voltage equalizers are introduced as an alternative option.

5.3.2 Regenerative Voltage Equalizers

Many regenerative voltage equalizers have been discussed in [101,102]. They are categorized as unidirectional and bi-directional energy flow types. These voltage equalizers employ intermediate energy storage components such as inductors, transformers and capacitors to transfer energy. In addition, trade-offs between circuit complexity, control complexity, and the cost and dynamic performance of some regenerative type voltage equalizers are discussed in [101,102]. The main issues of designing regenerative voltage equalizers are summarized as:

- Energy efficiency and balancing time
- Complexity and cost
- Modularity

The efficiency of a voltage equalizer is the highest concern of system design engineers designing an energy storage system. Since voltage equalizers increase the energy loss, it is preferable not to have them in the first place. However, due to the voltage unbalance problems reported in the last section, voltage equalizers are necessary for supercapacitor energy system.

Ideally, to achieve high efficiency in voltage equalizing, voltage equalizers should have a highly efficient and effective energy circulation when transferring energy from the highest voltage cell directly to the lowest voltage cells. In other words, it is preferable for energy transfer to bypass average or neutrally charged cells when an over voltage cell situation is detected within a stack. However, this is not always possible, and for this reason, portions of energy need to be circulated from the highest to the lowest voltage cells via the intermediary voltage cells. Getting this energy in and out of the intermediary cells causes additional losses, which affects the overall efficiency of the voltage equalizing process. This inefficient circulation of energy is indicated in the cell voltages reducing and increasing. In [103], energy transfer is presented as a Digraph which is very useful to indicate the direction of energy transfer. Note that the balancing time is also increased due to this inefficient energy circulation.

More flexible energy circulation, avoiding average charged/neutral cells can be achieved by increasing the complexity of the voltage equalizers. This can be done by

choosing topologies with a high number of switches, either using relays or semiconductor devices to provide multiple direct energy flow paths [104,105]. However, as the number of switches per cell increases, a complicated control algorithm/hardware and individual cell voltage measurement become crucial in order to manage the energy flow effectively. These additional requirements increase the cost of implementation of the voltage equalizer significantly.

Another main design issue is the modularity of voltage equalizers which is very important in grid-interface applications (i.e. 400-600V stack) where a large number of supercapacitors (i.e. 200-300 components) are required to be series-connected. In [101], the voltage equalizers are required at both cell and modular level in order to transfer energy among all cells within the same stack. It is also shown that the intermediate energy storage and switches used in the modular level voltage equalizers are rated at *n* times that used in the cell voltage equalizer for *n* cell voltage equalizers.

In this thesis, 3 main types of regenerative voltage equalizers are considered and discussed. These are the switch capacitor, inductive and single-switch types.

5.3.2.1 Switched-capacitor Voltage Equalizers

A switched-capacitor equalizer is used to balance cell voltage of either series-connected battery or supercapacitor stacks [106-109]. In Figure 5.3(a), a 4-cell switched-capacitor equalizer is presented where C_{T1}-C_{T3} are capacitors, Q_1-Q_4 are bi-directional switches, $Cell_1$-$Cell_4$ are either battery or supercapacitor cells. The concept is to use series-connected capacitors to transfer energy between each supercapacitor cells by toggling all switches up and down for the same period of time. However, the main drawbacks of this architecture are long equalizing time and inefficient energy transfer. The equalizing time is limited by low energy transfer rate due to small voltage differences between capacitors and cells, the contact resistances and the device *ESR*. Therefore, this equalizer is usually employed in batteries equalizing applications where charging and discharging periods are also long. Additionally, there is a risk of high peak current flow at the beginning of the equalizing operation (i.e. all capacitors are in completely discharge condition). This happens because the circuit relies only on small resistance and stray inductance from switches and device terminals to limit the current.

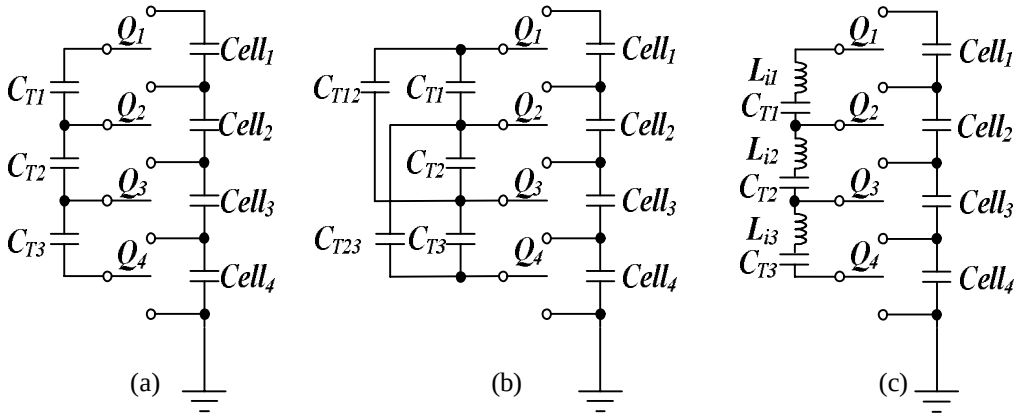


Figure 5.3 A switch-capacitor voltage equalizer (a) traditional topology (b) double-tiered topology (c) resonant topology

The circuit in Figure 5.3(a) is further developed by [107] with an introduction of a second row of series-connected capacitors, C_{T12} and C_{T23}, as shown in Figure 5.3(b). The second row of series-capacitors improves the speed of energy transfer among all cells. Unequal energy of each battery cell within the stack can transfer more quickly through this second capacitors row. In [107], the circuit parameter variation of this topology also is investigated through a numerical approach.

Alternative development of the circuit in Figure 5.3(a) with a resonant tank concept is presented in Figure 5.3(c) [108,109]. By including inductances, L_{i1}-L_{i3}, the high current spike problem is resolved and these inductors form a resonant tank with capacitors C_{T1}-C_{T3}. With a resonant concept (i.e. with zero-current switching in this case), the author of [108,109] claims that the efficiency of the equalizer is improved to 98%. However, this high efficiency is achieved from a 2-cell stack only so the problem of an inefficient energy circulation is absent.

5.3.2.2 Inductive Voltage Equalizers

Inductive type voltage equalizers utilize either inductors or transformers as the main intermediate energy storage to transfer energy and balance cell voltage. The mechanism of transferring energy can be from cell to cell (charge-discharge types), from cell to module (discharge types) and from module to cell (charge types) as summarized in [101]. The topologies used can be Forward [110], Fly-back [104,111-115] and Buck-boost [47,99,105,116-118].

Initially many voltage equalizers are developed with a centralized multi-winding secondary transformer [110] since the transformer can transfer energy to many cells

at once. However, modularity is a serious limitation of the topologies using centralized transformers as it is difficult to design and to construct a symmetrical winding transformer for large numbers of cells. An alternative scheme is to use a discrete transformer per cell to manage energy flow individually [112,113], but in doing this, a number of switches also increases with number of cells.

Another approach which relies on discrete inductors is a bi-directional buck-boost voltage equalizer [47,99,116-118] as presented in Figure 5.4(a) and Figure 5.4(b). The control design and implementation of this topology can be found in [118].

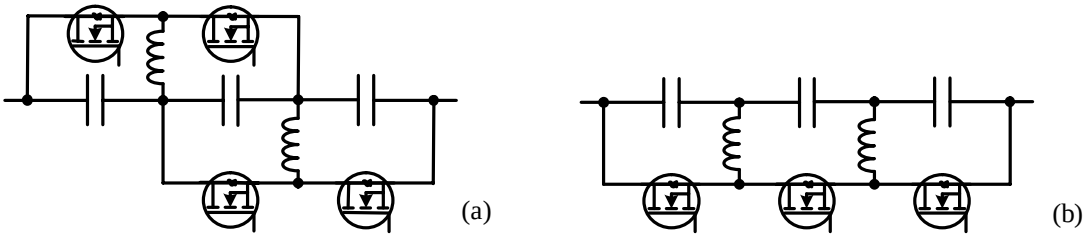


Figure 5.4 Bi-directional buck-boost voltage equalizers for 3 cells stack with (a) 2*N*-2 switch per *n* cell-stack [99,116] (b) *n* switch per *n* cell-stack [117,118]

To reduce weight of the multiple transformers or inductors, unidirectional or bi-directional types switching with a single transformer or a single inductor can be used [104,105,114].

Considering these inductive voltage equalizer topologies, as the number of cells grows, a number of switches also increases. Unlike the switched-capacitor topologies, these topologies with a higher number of switches require more highly complex control algorithm in order to manage energy efficiently. Therefore, the issue is to reduce the number of switches but still maintain the voltage equalizing functionality. These topologies are the single-switch voltage equalizers which will be presented in the next section.

5.3.2.3 A Single-switch Voltage Equalizer

Several single-switch voltage equalizers have been proposed in [119,120]. Their main advantages are simple control and a single driver circuitry for a switching device. The first single-switched equalizer is developed with a fly-back topology utilizing a centralized multi-winding secondary transformer as presented in Figure 5.6. The operation of this equalizer will be described in more detail in section 5.4. However, due to the problem of having a multi-winding transformer in a

symmetrical winding construction, a multi-stack buck-boost topology is proposed in [119] as presented in Figure 5.5. Figure 5.5 shows 4-cell SEPIC-based, Zeta-based and isolated Cuk-based voltage equalizers which utilize discrete inductors and capacitors. These circuits, C_{in} and L_{in} are the input capacitor and inductor, C_{T1}-C_{T4} are capacitors, L_{i1}-L_{i4} are inductors, Q is a switch, D_1-D_4 are diodes and $Cell_1$-$Cell_4$ are either battery or supercapacitor cells. For an isolated Cuk-based equalizer, a transformer with a turn ratio, N_a, connected with an auxiliary capacitor, C_a, is used.

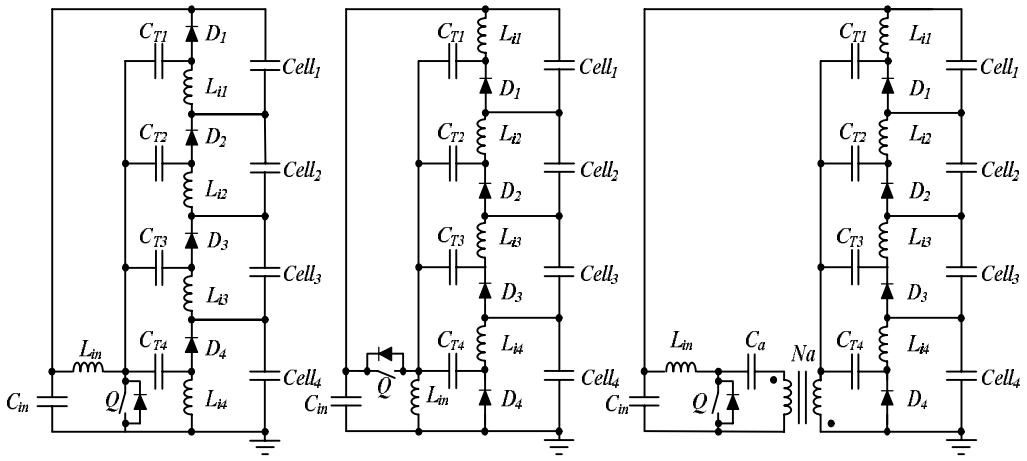


Figure 5.5 A single-switch cell voltage equalizer using multi-stack buck-boost converter (a) SEPIC-based equalizer (b) Zeta-based equalizer (c) Isolated Cuk-based equalizer [119]

A single-switch topology has a drawback of efficiency as the energy cannot be moved flexibly (i.e. from the most unwanted-energy to the most wanted-energy cells). These inefficient energy flow behaviours can be observed in both in short-term and long-term balancing periods. In the short-term period, some cell voltages are maintained constant since the same amount of energy is taken out and put in to the cells within the switching period [119,120]. The constant voltage cell condition does not mean the unwanted energy by-passing the constant voltage cells to the most wanted energy cell. For the long-term period, the effect is observed as the voltage levels of cells are charged and then discharged again or vice versa. These effects will be presented experimentally with a single-switch flyback-based topology in Section 5.5.

5.3.2.4 Summary of Regenerative Voltage Equalizers

Advantages and disadvantages of 3 types of voltage equalizers are summarized in Table 5.2.

Table 5.2 Summary of advantages and disadvantages of considered voltage equalizers

Specification	Switched-capacitor voltage equalizer topologies [106-109]	Inductive voltage equalizer topologies [47,99,104,105,110-118]	Single-switch voltage equalizer topologies [119,120]
Circuit complexity	High ☹	High ☹	Low ☺
Control	Simple ☺	Complex ☹	Simple ☺
Efficiency	Low ☹	High ☺	Medium ☺
Equalizing time	Long ☹	Short ☺	Medium ☺
Additional complexity	May have current spike problem at a starting period	Require energy management scheme	May require a multi-winding transformer

It can be seen that trade-offs in size, weight, efficiency, modularity and control complexity of each topologies have been reported in literature. However, it has been found that investigation on efficiency improvement versus increase of complexity/cost has not been sufficiently reported. Therefore, the aim of this chapter is to investigate the design and operation of a single-switch flyback voltage equalizer topology [52,102,121] shown in Figure 5.6. The investigation is focused on the trade-off between the equalization time, the effectiveness of equalization (i.e. maximum voltage deviation) and the total power losses of both equalizer and stack. In addition, the performance against an active-dissipative voltage equalizer is also investigated and used as a comparison to the performance of the flyback topology [58].

5.4 A Single-switch Fly-back Voltage Equalizer

A single-switch flyback-based voltage equalizer [115] is shown Figure 5.6. When the switch, *Q*, is turned ON, the energy from the entire stack is transferred into the flyback transformer, and when *Q* is turned OFF, energy is then returned mostly to the lower voltage cell, as illustrated in Figure 5.6(a) and (b). The circuit is working with a duty cycle, *d*, equal to or less than 0.5 to provide an optimum stress on both the transistor and diodes. By doing this, the circuit is operated in a discontinuous conduction mode (DCM), so a feedback control is not required. When the voltages of all cells are balanced with small deviation, the flyback converter can be disabled. This circuit utilizes the transformer to circulate some of the stack energy to equalize all cells voltages. The equalizer retrieves quantities of energy proportional to each cell voltage when the flyback transformer is "charged" and returns quantities of energy proportional to the voltage mismatch when it is "discharged".

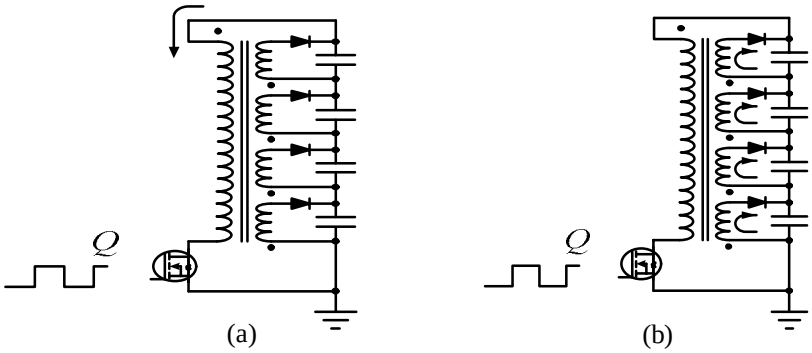


Figure 5.6 Current flowing direction of flyback voltage converter used as a voltage equalizer (a) when turn ON switch *Q* energy is taken from the whole stack (b) when turn OFF switch *Q*, energy is transferred to each cells but mostly to the lowest voltage cell.

5.5 Investigation of Cell Voltage Balancing Mechanism of the Flyback Voltage Equalizer

To validate the operation of the voltage equalizing mechanism of the flyback equalizer, a simple simulation and a simple experiment were performed.

The operation of the flyback voltage equalizer is simulated using the PSIM® as presented in Figure 5.7. To reduce simulation time, four supercapacitor cells of 0.1F capacitance with cell voltage 2.5 V are connected in series to build a 10V stack. All *ESR*s of the capacitors are ignored. The other circuit parameters used in simulation are: magnetizing inductance, L_m = 5mH, switching frequency, f_{sw} = 10 kHz with duty cycle, d = 0.5, diode forward voltage drops, V_{F1}-V_{F4} = 0.3V, transformer turn ratio (N_P:N_S) = 4:1.12 with four secondary windings. Leakage inductances and winding resistances of primary and secondary windings, L_{P_Leak} and L_{S_Leak}, are set to a low nominal value.

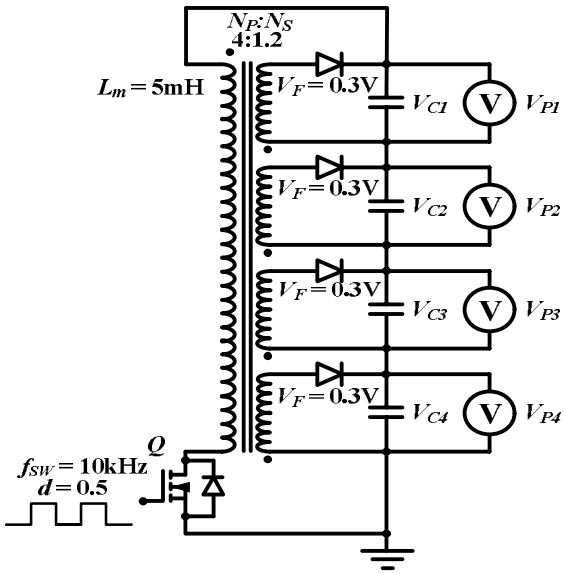


Figure 5.7 Simulation schematic diagram of flyback voltage equalizer.

The experimental investigation is also performed similarly to the simulation but using eight Maxwell® PC5 (4F/2.5V) supercapacitor cells connected in series and parallel to build a 2F/10V stack. In addition, since building an imbalanced stack is more difficult, different initial cell voltages have been considered to illustrate the operation of the flyback voltage equalizer circuit. The rate of energy being circulated and dissipated, and the total stack capacitance are different from the simulation, so different equalization times are expected.

Both the simulation and the experiment were carried out for two different initial capacitor voltages on V_{C1}-V_{C4}, settings as given in Table 5.3. These voltage settings are assigned such that the equalizing mechanism can be observed clearly. However, these settings may not represent the realistic unbalance cell voltage. The simulated and experimental operating voltages of all cells during the equalizing time are observed and are presented from Figure 5.8 to Figure 5.10. For the simulation, the values V_{C1}-V_{C4} are recorded and are presented as V_{P1}-V_{P4} in Figure 5.8 and Figure 5.9.

Table 5.3 Initial cell voltage of supercapacitors for both simulation and experimental set ups

Initial cell voltage (V)	Simulation		Experimental	
	Case 1	Case 2	Case 1	Case 2
V_{C1}	2.50	2.50	2.44	2.50
V_{C2}	2.00	2.00	2.06	2.02
V_{C3}	1.50	2.00	1.54	2.02
V_{C4}	1.00	1.50	1.00	1.54

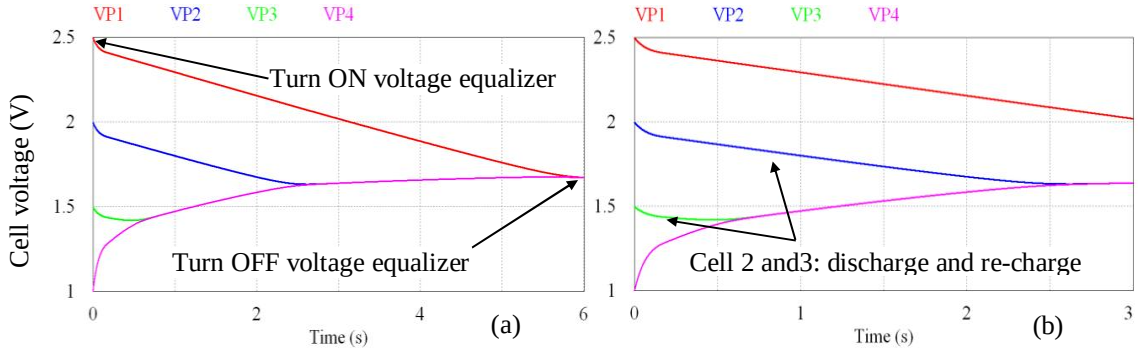


Figure 5.8 Simulation of the 4-cell stack with the flyback voltage equalizer case 1 (a) cells' voltages from time = 0 to 6s (b) cells' voltages zoom in from time = 0 to 3s

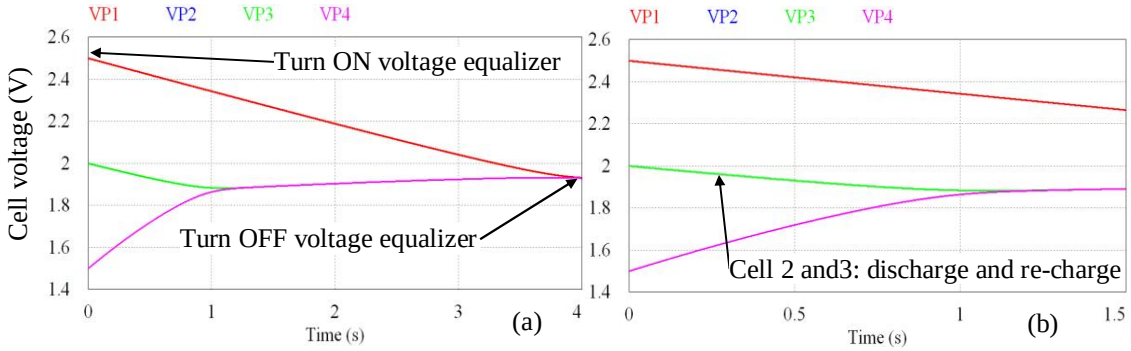


Figure 5.9 Simulation of the 4-cell stack with the flyback voltage equalizer case 2 (a) cells' voltage from time = 0 to 4s (b) cells' voltages zoom in from time = 0 to 1.5s

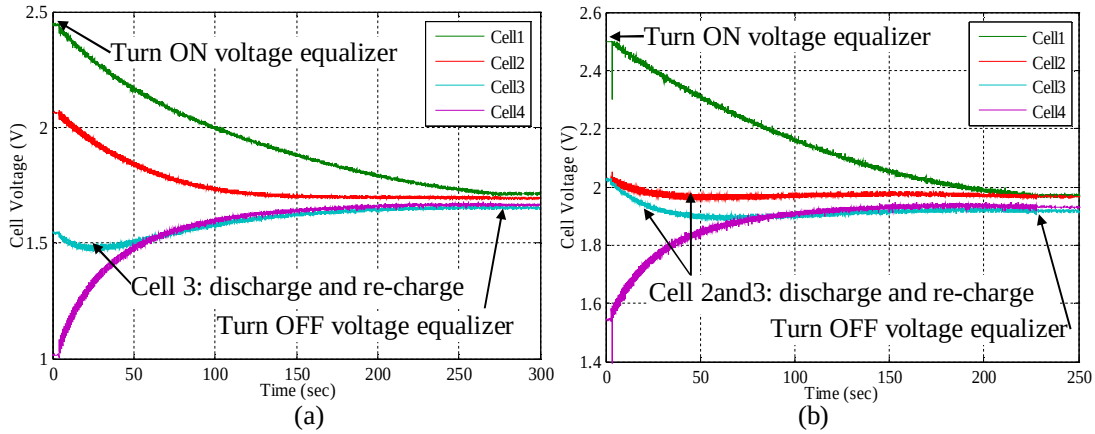


Figure 5.10 Experimental result of the 4-cell stack with the flyback voltage equalizer (a) case 1 (b) case 2

Both the simulation and the experimental results show clearly that there is an inefficient energy flow into cell 3 for case 1 (Figure 5.8(b) and Figure 5.10(a)) and both cell 2 and cell 3 for case 2 (Figure 5.9(b) and Figure 5.10(b)), as they are initially discharged and then re-charged later. This re-circulation of the energy causes losses and decreases the overall efficiency of the voltage equalizer and of the supercapacitor stack. Particularly, according to case 2, to achieve low energy loss in the voltage equalizing, the energy from the highest voltage cell (top) should be transferred directly to the lowest voltage cell (bottom) rather than being passed to/from the other cells to charge the bottom cell. This is a limitation of this simple flyback topology which utilizes a centralized multi-winding transformer as an intermediate energy storage to transfer energy among the capacitor cells. However, the question that will be addressed in the following section is how serious is the impact of this unwanted energy circulation on equalization efficiency.

5.6 Simulation Set up and Results

5.6.1 Simulation Parameters Selection

To investigate trade-offs between the total equalizing loss, *TEL* (represented in this thesis as a percentage of the charging energy loss, E_{Loss_charge}), the equalizing time, T_{Eq}, and the standard deviation of the cell voltage of the stack, *STD*, of the flyback topology, a simulation study is done in PSIM®. The *STD* is calculated by:

$$STD = \sqrt{\frac{\sum_{i=1}^{n}\left(V_i - V_{Average}\right)}{n-1}} \tag{5.1}$$

where n is number of cells, V_i is cell voltage and $V_{Average}$ is a mean value of cell voltages.

A similar simulation is also performed for the active-dissipative voltage equalizer (Figure 5.2(d)), and the results are used as a benchmark in comparison with the flyback type.

In this simulation, the charging stack voltage of series-connected supercapacitors is depicted in both Figure 5.11 and Figure 5.12. Figure 5.11 shows cell voltages equalized by the flyback equalizer, so the energy is regenerated. On the other hand, Figure 5.12 shows cell voltages equalized by the active-dissipative equalizer, so the energy is dissipated in the resistors. Figure 5.12 also shows the length of T_{Eq} that the cell dissipative currents, $I_{R\_dissipate}$, flow. The equalization mechanism of the active-dissipative equalizer is activated corresponding to the threshold over-voltage condition setting. The effect of *ESR* is indicated as 'IR voltage drop' in both Figure 5.11 and Figure 5.12 since the RC equivalent model (*ESR* and *C* connected in series) is used to represent the supercapacitor characteristic. In addition, the charger and the equalizer are set to stop at the same time, so the T_{Eq} period is defined in relative to the charging period, T_C, as an equalizing duty cycle, d_{Eq}. Note that the *STD* during charging is focused since an overvoltage problem occurs in this period. The *STD* during discharging is not included in this analysis.

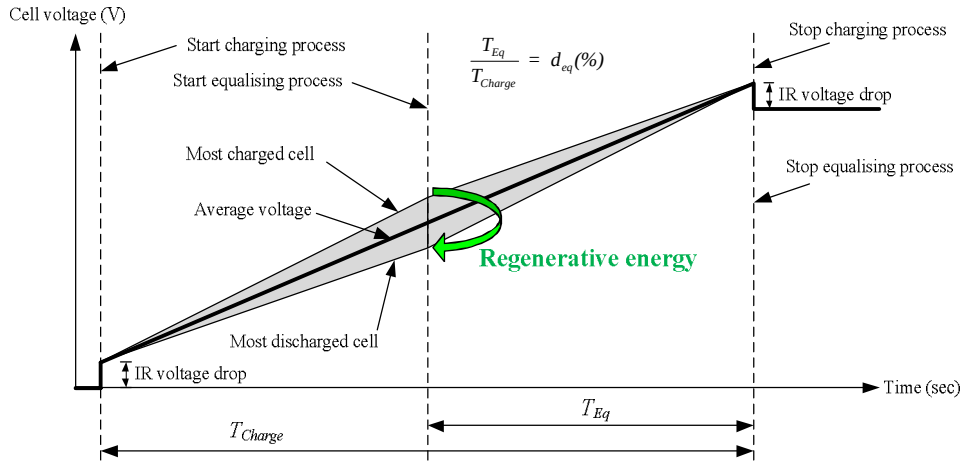


Figure 5.11 Definition of parameters for the flyback voltage equalization process of the series-connected supercapacitor stack under constant current charging

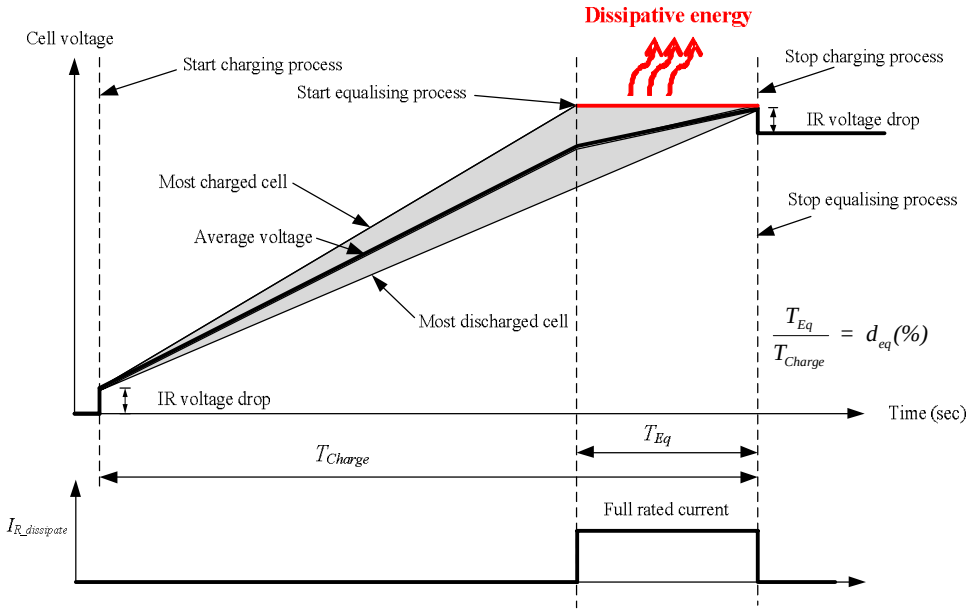


Figure 5.12 Definition of parameters for the active-dissipative voltage equalization process of the series-connected supercapacitor stack under constant current charging

The 4-cell stack of Figure 5.7 is considered again in this analysis, but this time all cells are starting from a completely discharged condition with uneven capacitances of ±5% assigned, where C_1 = 1.05pu, C_2 = C_3 = 1pu and C_4 = 0.95pu. The variation of devices' *ESR* is neglected in this study. Losses due to *ESR* and winding resistances, ESR_W, are calculated from an integration of $I_{RMS}^2 \times (ESR+ESR_W)$ over a conduction period. In addition, losses due to semiconductor devices (MOSFET and diode) are calculated by PSIM® thermal module as presented in Figure 5.13. For this study, modeling of the switching loss and transformer core loss has not been included.

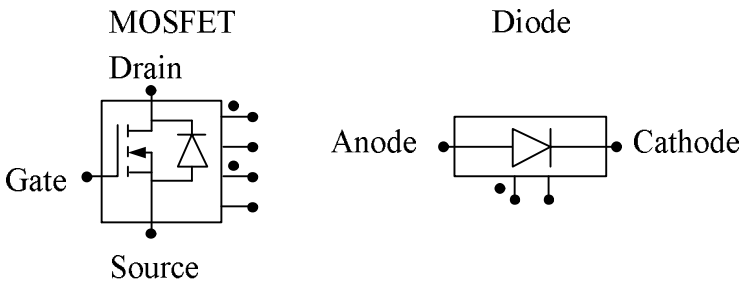


Figure 5.13 PSIM® Thermal module for MOSFETs and diodes

For this analysis, a set of simulation parameters are defined and are presented in Table 5.4. The transformer turns ratio is set to $N_P/N_S = n/1.2$ [101] to compensate for the forward diode voltage drop during commutation where n is the number of supercapacitor cells connected in series. The ESR_W is split into a primary, R_{Pri} and secondary, R_{Sec} winding resistances and they are chosen to be less than or equal to the supercapacitor ESR. Therefore, the conduction losses due to these windings during the T_{Eq} are comparable to those of the supercapacitors. The leakage inductances of the primary and the secondary windings, L_{P_Leak} and L_{S_Leak}, in this analysis are deliberately minimized so that the corresponding snubber losses and the snubber design can be neglected. In practice, the value of L_{S_Leak} is approximately 10% of the value of L_{P_Leak}, and this fact is also used in this simulation. Supercapacitor parameters, C = 0.5F and ESR = 50mΩ are used to minimize the charging/simulation time. However, the calculated energy loss can be scaled up for higher capacitances, where both charging and equalizing time will take longer, but this is not desired in a simulation study. For the switching devices, the on-state V-I characteristics are chosen to match devices with voltage and current ratings close to the operating condition so that the level of energy loss due to equalizing is realistic. The switching device parameters are taken from the datasheet of the VISHAY® MOSFET Si2302CDS (V_{ds_max} = 20V and I_{ds_max} = 2.9A) and the NXP Schottky diode PMEG3030EP (V_{r_max} = 30V, I_{F_max} = 3A). The duty cycle, d, is set to 0.45 to guarantee the total reset of the magnetizing inductance energy over a switching period. For the charging condition, the stack is charged with a constant current, I_{Charge}, of 5A until the whole stack voltage reaches 2.7V×4 = 10.8V. This results in a charging period, T_C, of 0.4696sec which is kept constant for all simulations. The simulation parameters are summarized in Table 5.4.

Table 5.4 Definition of model's parameters used in PSIM simulation

	Parameter	Value
Transformer	N_P	4
	N_S	1.2
	R_{Pri}	50mΩ
	R_{Sec}	4.5mΩ
	L_{P_Leak}	1µH
	L_{S_Leak}	0.09µH
	L_m	*testing parameter*
Super-capacitor	V_{cell_max}	2.7V
	V_{Stack}	2.7×4 = 10.8V
	ESR	50mΩ
	C	0.5F±5%
Semiconductor device	MOSFET	Si2302CDS
	V_{ds_max}	20V
	I_{ds_max}	2.9A
	Diode	PMEG3030EP
	V_{r_max}	30V
	I_{F_max}	3A
Timing and charging	f_{sw}	*testing parameter*
	d	0.45
	I_{ch}	5A
	T_C	0.4696s
	d_{Eq}	*testing parameter*

Figure 5.14 shows a simulation schematic diagram of the flyback voltage equalizer as implemented in PSIM®. The circuit topology presented in Figure 5.14 is the same as that of Figure 5.7 but with more detail of the simulation voltage, current probes and loss calculation probes as listed in Table 5.5. In Figure 5.14, the switching loss calculation probes (Q_{Sw}, QD_{Sw} and D_{Sw1}-D_{Sw4}) are connected here to make schematic complete and to let PSIM® run without error message, but they are not included in the loss calculation. The capacitor voltages, V_{C1}-V_{C4}, are used to calculate amount of supercapacitor stack stored energy, E_{Stored_Stack}. The cell voltages, V_{P1}-V_{P4}, are monitored for protection purposes.

Table 5.5 Symbols used in the simulation and their meaning

Symbol	Meaning
i_{TP}	A transformer primary winding current
i_{TS1}-i_{TS4}	Transformer secondary winding currents
i_{SC1}-i_{SC4}	Cell currents
v_{C1}-v_{C4}	Capacitor voltages
v_{SC1}-v_{SC4}	Cell voltages
v_{Stack}	A stack voltage
I_{Ch}	A main charger current
Q_{Cond} and Q_{Sw}	MOSFET conduction and switching losses
QD_{Cond} and QD_{Sw}	Anti-parallel diode conduction and switching losses
D_{Cond1}-D_{Cond4}	Cell diode conduction losses
D_{Sw1}-D_{Sw4}	Cell diode switching losses.

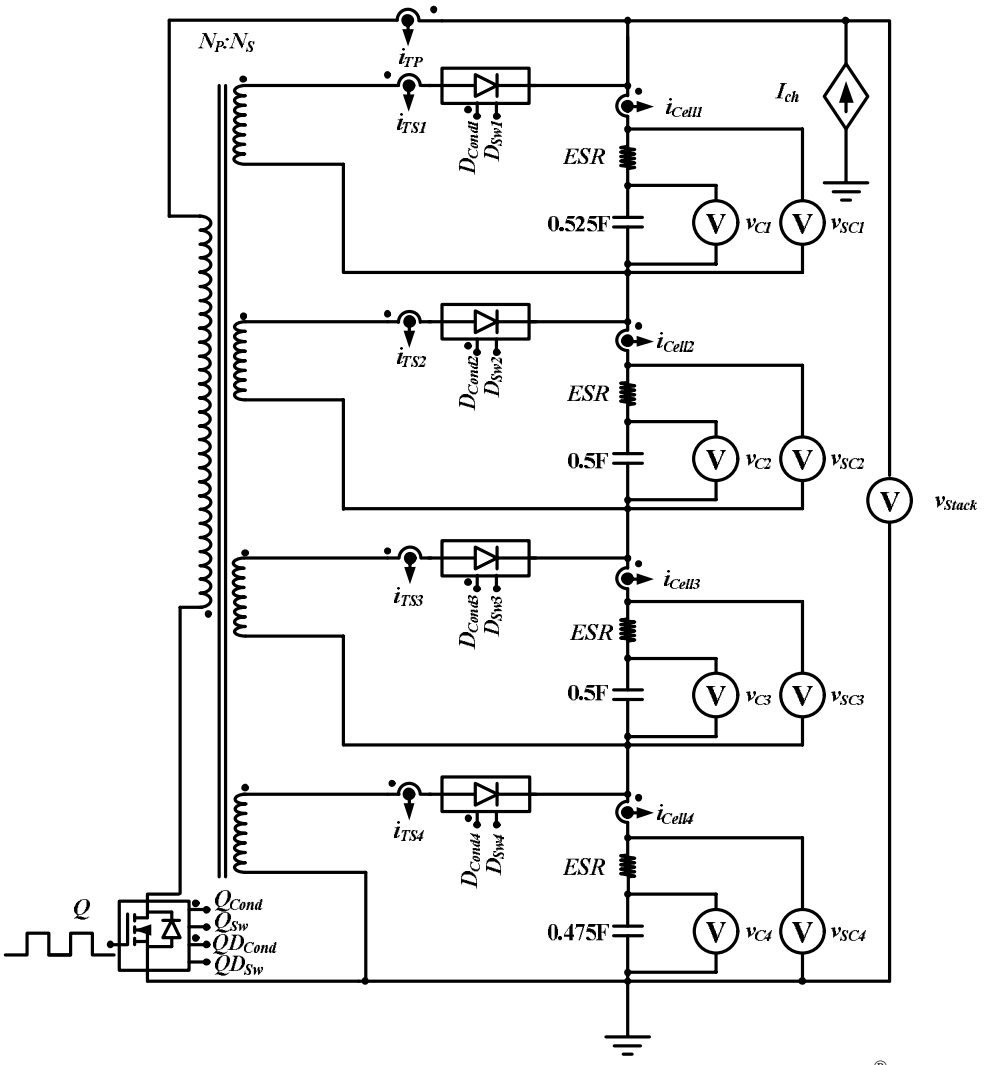


Figure 5.14 Simulation model of the flyback voltage equalizer and its PSIM® parameter settings

5.6.2 Flyback Voltage Equalizer Operating Modes

The possible operating modes of a flyback voltage equalizer are listed below, which range from a simple control algorithm requirement to a more complicated but more effective one.

- Mode I – constant switching frequency
- Mode II – constant primary winding peak current
- Mode III – constant power

The main difference between Mode I and Mode II can be seen clearly in the i_{TP} current as presented in Figure 5.15.

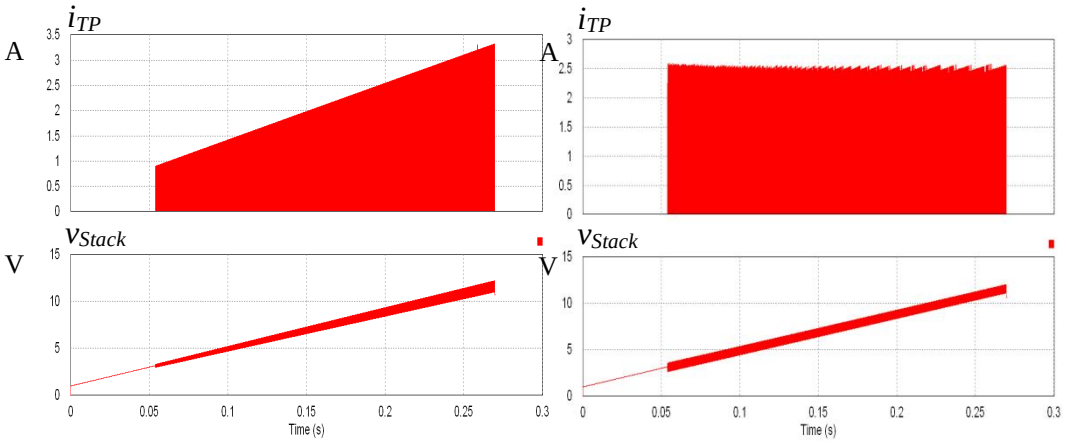


Figure 5.15 The primary winding current and the supercapacitor stack voltage of the flyback equalizer operating (a) in Mode I (b) in Mode II

For Mode III, in order to maintain power at constant level as a v_{Stack} reduces, a primary winding peak current need to be increased at the beginning of the equalization process. This action results in overrated devices compared with the other two modes. In addition, to calculate the current reference depending on the instantaneous stack voltage, a division operation, which is only available in the digital control platform, is needed. To keep the control as simple as the circuit topology, the digital control platform is avoided. Therefore, the constant power mode will not be considered in this analysis.

5.6.2.1 Mode I – Constant Switching Frequency

Constant switching frequency mode is considered as a conventional operating mode of this equalizer. Generally, in a flyback transformer, the maximum stored energy, E_{Stored} in the magnetizing inductance, L_m varies proportionally to the square of the peak i_{TP}, $\hat{i}_{TP}$, which is calculated from (5.2).

$$E_{Stored} = 0.5 L_m \hat{i}_{TP}^2 \tag{5.2}$$

However, when Q is ON, the voltage across the v_{Lm} is equal to v_{Stack}, and

$$v_{Lm} = L_m \frac{di_{TP}}{dt} = L_m \frac{\hat{i}_{TP} f_{sw}}{d} \tag{5.3}$$

which shows that if f_{sw} and d are kept constant, $\hat{i}_{TP}$ is depending on v_{Stack}.

Re-arranging (5.3) for $\hat{i}_{TP}$ and substituting it in (5.2) results in

$$E_{Stored} = 0.5 \frac{v_{Stack}^2 d^2}{L_m f_{sw}^2} \tag{5.4}$$

It can be seen that the E_{Stored} in L_m is dependent on v_{Stack} and it reaches a maximum when the stack is fully charged. The value of $\hat{i}_{TP}$ when v_{Stack} reaches its maximum has been recorded and the corresponding maximum E_{Stored} as a function of L_m are summarized in Figure 5.16 for different f_{sw} and L_m settings. This dependency seems to change significantly from a steep curve at low L_m (that would typically correspond to discontinuous conduction mode (DCM)) to a flatter one at high L_m, which is typical for continuous conduction mode (CCM). At around 0.35-0.5mH, there is a clear boundary between DCM and CCM. To make the equalizing process more effective, large quantities of energy need to be processed which means operation in DCM is desired. From (5.3), it is clear that if $\hat{i}_{TP}$ is to be kept constant throughout the entire T_{Eq}, it is necessary to adjust f_{sw} with v_{Stack} to ensure that the flyback operates in DCM all time. This operating mode is investigated the in next section.

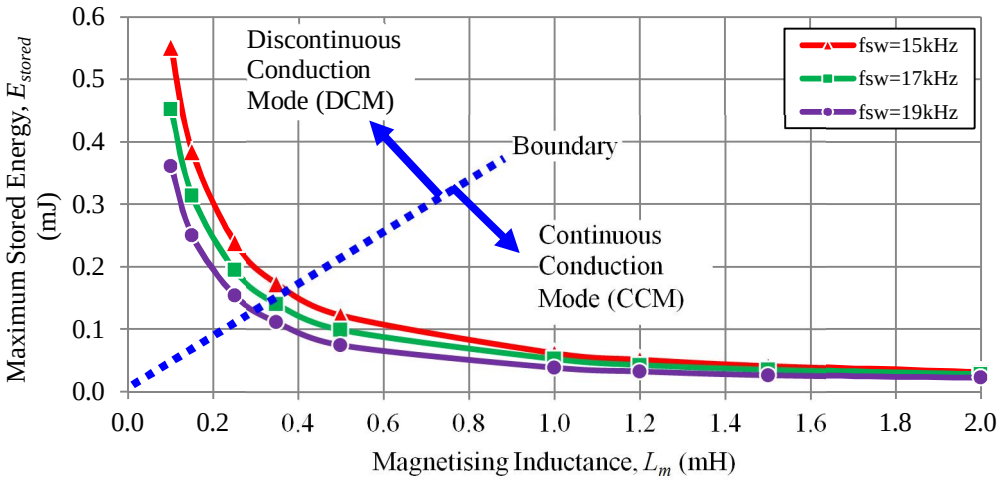


Figure 5.16 Maximum (corresponds to the end of charging) stored energy, E_{stored}, in the magnetizing inductance, L_m, of a flyback transformer versus the magnetizing inductance, L_m

The next step is to evaluate the efficiency and the effectiveness of the equalizing process by using the flyback voltage equalizer operating in Mode I. Three values for L_m: 0.1, 0.15 and 0.25mH are used in conjunction with a f_{sw} of 20kHz whilst for higher L_m values: 0.35, 0.5 and 1mH, a f_{sw} of 15kHz had to be used in order to avoid CCM. Figure 5.17 summarizes the total equalizing loss, *TEL*, as a percentage of the E_{Loss_charge}, at different starting moments of the equalizing process (i.e. different d_{Eq} setting). The *TEL* increases nonlinearly with increasing d_{Eq} since the equalizing circuit is operating for a longer amount of time.

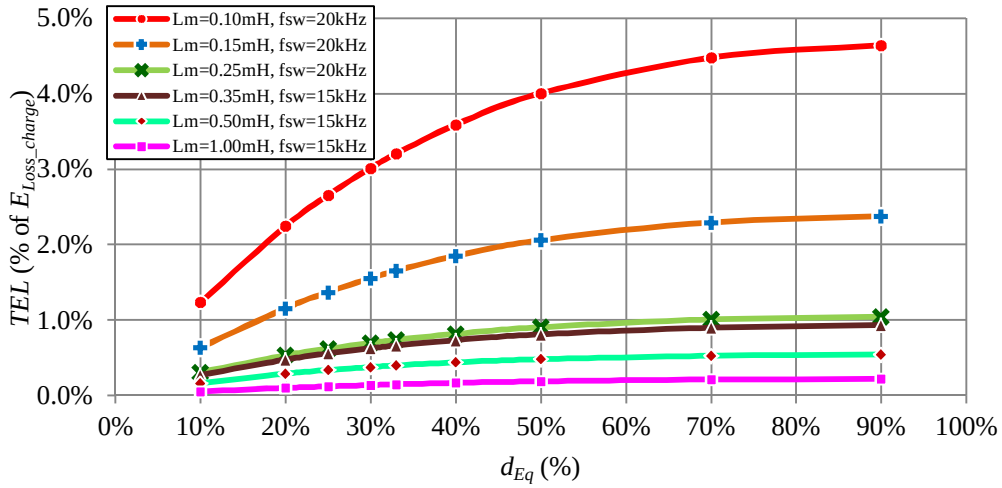


Figure 5.17 Total equalizing loss, *TEL*, versus duty equalizing, d_{Eq}, (% of charging time, T_C) at various magnetising inductance, L_m, and switching frequencies, f_{sw} (fixed duty cycle, fixed switching frequency condition)

The *TEL* is found to be very high when using lower L_m (0.1mH @20kHz) because the amount of energy processed already exceeds the minimum energy demand of the weakest cell, and a greater share of the excess energy is re-circulated through the

other cells. If the amount of energy processed is better matched to the cell's unbalance, the *TEL* will be reduced, as revealed by the curves corresponding to slightly higher L_m. Considering the *TEL* = 2% from two L_m curves (0.1mH and 0.15mH @20kHz) for the same *TEL* (2%), L_m = 0.1mH corresponds to the d_{Eq} of 18% and L_m = 0.15mH to 50%. However, at this point, it is not clear how effective the equalizing process is. For this reason the standard deviation of the cell voltages within the stack, *STD*, is also evaluated to establish the trade-off between *TEL* and *STD*. The results are summarized in Table 5.6 and shown in Figure 5.18.

Table 5.6 Simulation results of flyback voltage equalizer operating in Mode I

L_m (mH)	Point in Figure 5.18	d_{Eq} (%)	*TEL* (J)	E_{Loss_charge} (J)	*TEL* (% of E_{Loss_charge})	E_{Stored_Stack} (J)	v_{SC1} (V)	v_{SC2} (V)	v_{SC3} (V)	v_{SC4} (V)	$\Delta V_{Max} = V_{Max} - V_{Min}$	$V_{Average}$ (V)	*STD* (%)
0.1	*A*	62	0.0584	1.348	4.34	7.1906	2.6365	2.6798	2.6798	2.7340	0.0975	2.6825	3.99
	B	30	0.0406	1.348	3.02	7.2262	2.6218	2.6846	2.6846	2.7668	0.1450	2.6895	5.95
0.15	*C*	77	0.0315	1.348	2.34	7.2258	2.6448	2.6848	2.6848	2.7420	0.0972	2.6891	4.00
	D	36	0.0235	1.348	1.74	7.2463	2.6289	2.6851	2.6851	2.7737	0.1448	2.6932	5.99
0.25	*E*	58	0.0129	1.348	0.96	7.2574	2.6378	2.6817	2.6817	2.7798	0.1420	2.6952	6.01

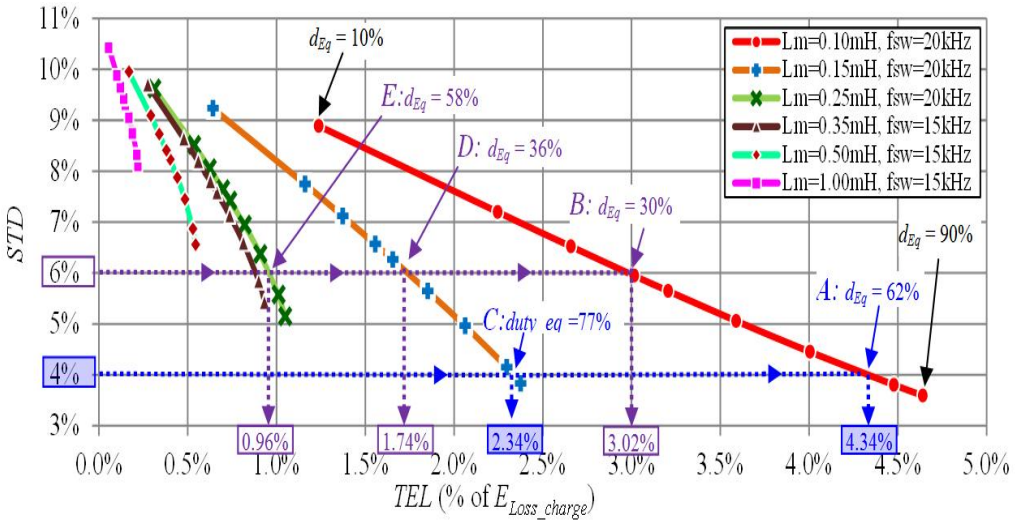


Figure 5.18 Standard deviation, *STD*, of cell voltages within the stack versus total equalizing loss, *TEL* (fixed duty cycle and switching frequency condition). The graph points correspond (from left to right) to the following duty equalizing, d_{Eq}: 10%, 20%, 25%, 30%, 33%, 40%, 50%, 70% and 90%.

From Table 5.6 and Figure 5.18, it can be seen that the same level of *STD* can be achieved with less *TEL* by using higher magnetising inductances and higher d_{Eq}. Two examples are highlighted in Figure 5.18.

- Example 1: *STD* = 4%, the 0.15mH *TEL* is 2.34% (point *C*) which is less than the 0.1mH *TEL* (point *A* = 4.34%). However, the 0.15mH d_{Eq} is 77% which is higher than the 0.1mH d_{Eq} (62%).
- Example 2: *STD* = 6%, the 0.25mH *TEL* is 0.96% (point *E*), which is the lowest when compared to the equalizing loss for 0.15mH (point *D* = 1.74%) and 0.1mH (point *B* = 3.02%) but the 0.25mH d_{Eq} (58%) will be higher compared to the the 0.15mH d_{Eq} (36%) and the 0.1mH d_{Eq} (30%).

However, since supercapacitor stacks are usually operated between half and full rated voltage, which corresponds to an extraction of 75% of total stored energy, a d_{Eq} > 50% may not be possible since the equalizing circuit needs to be continously ON when charging. Therefore, if the capacitance of the cells is highly unbalanced, it may be very inefficient or costly (high peak current means larger magnetics/high rated current switches) to achieve a very good voltage equalizing. This reason points to a necessary compromise between the effectiveness of equalizing and the maximising the stored energy in the stack.

5.6.2.2 Mode II – Constant Primary Winding Peak Current

Re-arranging (5.3) for $\hat{i}_p$ and substituting in (5.2) results in

$$E_{stored} = 0.5 \frac{v_{Stack}^2 d^2}{L_m f_{sw}^2} \tag{5.5}$$

From (5.5), f_{sw} can be extracted:

$$f_{sw} = \sqrt{\frac{d^2 v_{Stack}^2}{2 L_m E_{stored}}} = \frac{d v_{Stack}}{\sqrt{2 L_m E_{stored}}} \tag{5.6}$$

where d and E_{stored} are imposed and the only variable is v_{Stack}. In order to achieve constant $\hat{i}_{TP}$ during the whole charging period, f_{sw} has to be adjusted according to (5.6).

Again, the same set of L_m values used in Mode I is also used here. The variation of f_{sw} for each L_m follows (5.6) so that $\hat{i}_{TP}$, which will remain constant throughout the charging period, will match the maximum $\hat{i}_{TP}$ at the end of the charging period in Mode I. The simulation results are summarized in Figure 5.19 which shows the corresponding *TEL* as a percentage of the charging energy at different starting moments of the equalizing process (i.e. different d_{Eq}) with constant $\hat{i}_{TP}$. It can be noted that *TEL* becomes very high when using a lower L_m but compared to Mode I, it now increases linearly with d_{Eq}.

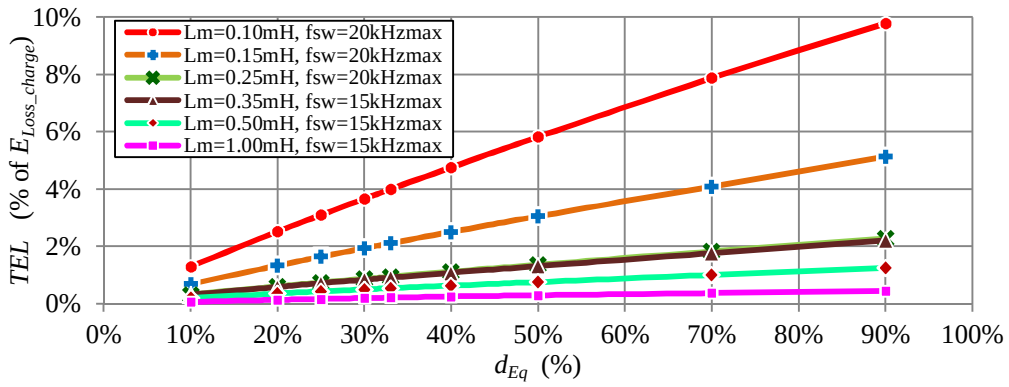


Figure 5.19 Total equalizing loss, *TEL*, versus duty equalizing, d_{Eq} (% of charging time) at various magnetising inductance, L_m and switching frequency, f_{sw} (fixed duty cycle, varying switching frequency condition)

The effectiveness of the equalizing process is evaluated by determining the *STD* for each set of simulation parameters and its variation versus *TEL* is shown in Figure 5.20. A few operating points highlighted in Table 5.7 are selected for discussion. From Table 5.7 and Figure 5.20, it can again be seen, that the same *STD* can be achieved with less *TEL* by using higher L_m and higher d_{Eq}. Two examples are highlighted in Figure 5.20.

- Example 1: *STD* = 4%, the 0.25mH *TEL* is 2.22% (point *E*) which is the lowest when compared to the 0.15mH *TEL* (point *C* = 3.74%) and the 0.1mH *TEL* (point *A* = 6.76%). The 0.25mH d_{Eq} will be the highest (87%) at compared to the 0.15mH d_{Eq} (63%) and the 0.1mH d_{Eq} (59%).
- Example 2: *STD* = 7%, the 0.25mH *TEL* is 0.95% (point *F*) which is the lowest when compared to the 0.15mH *TEL* (point *D* = 1.58%) and the 0.1mH *TEL* (point *B* = 2.64%) but the 0.25mH d_{Eq} is the highest (33%) compared to the 0.15mH d_{Eq} (24%) and the 0.1mH d_{Eq} (21%).

Table 5.7 Simulation results of flyback voltage equalizer operating in Mode II

Lm (mH)	Point in Figure 5.20	d_{Eq} (%)	TEL (J)	E_{Loss_charge} (J)	TEL (% of E_{Loss_charge})	E_{Stored_Stack} (J)	v_{SC1} (V)	v_{SC2} (V)	v_{SC3} (V)	v_{SC4} (V)	$\Delta V_{Max} = V_{Max}$-V_{Min}	$V_{Average}$ (V)	STD (%)
0.1	*A*	59	0.0912	1.3480	6.76	7.1416	2.6264	2.6714	2.6714	2.7243	0.0979	2.6734	4.00
	B	21	0.0356	1.3480	2.64	7.2352	2.6106	2.6865	2.6865	2.7816	0.1710	2.6913	7.00
0.15	*C*	63	0.0504	1.3480	3.74	7.1989	2.6382	2.6811	2.6811	2.7359	0.0977	2.6841	4.00
	D	24	0.0213	1.3480	1.58	7.2515	2.6161	2.6868	2.6868	2.7876	0.1715	2.6943	7.06
0.25	*E*	87	0.0299	1.3480	2.22	7.2155	2.6433	2.6825	2.6825	2.7404	0.0971	2.6872	4.00
	F	33	0.0128	1.3480	0.95	7.2608	2.6237	2.6835	2.6835	2.7933	0.1696	2.6960	7.07

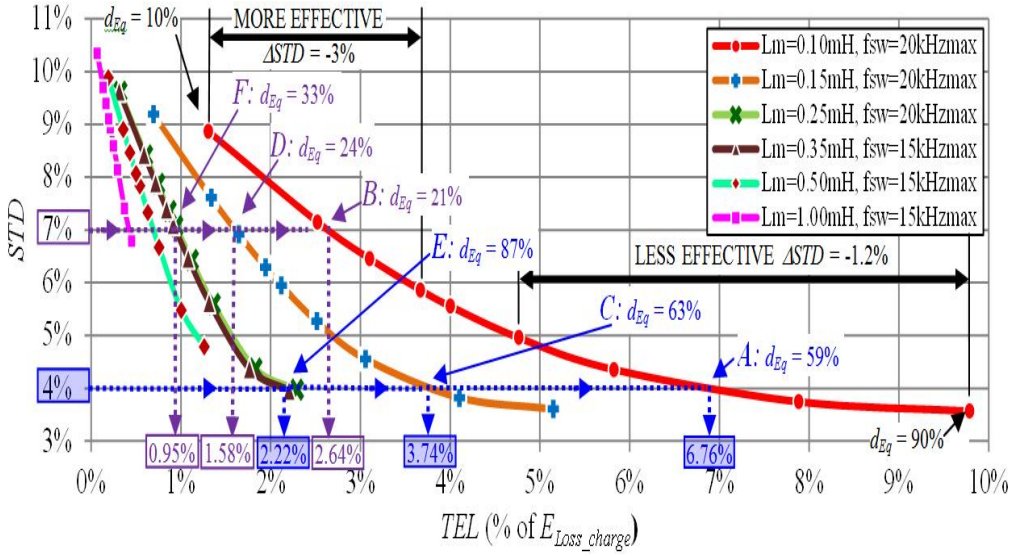


Figure 5.20 Standard deviation (*STD*) of cell voltage within the stack versus total equalizing loss (*TEL*) (fix duty cycle, varying switching frequency condition). The graph points correspond (from left to right) to the following d_{Eq}: 10%, 20%, 25%, 30%, 33%, 40%, 50%, 70% and 90%.

5.6.3 Comparison between Mode I and Mode II Flyback Voltage Equalizers

When comparing Mode I and II from the point of view of cell-volatge *STD* versus the time of equalizing, it can be noted that to provide the same level of losses (= 2% for example in Figure 5.17 and Figure 5.19), the voltage equalizer needs to operate for a shorter time in Mode II (d_{Eq} = 30% for 0.15mH@20kHz max) compared to Mode I (d_{Eq} = 50% for 0.15mH@20kHz). This may be desirable in situations when only a shorter operation of the equalizer near the full state of charge

is possible. However, this has a different impact on the effectiveness of equalizing, with Mode I achieving a better *STD* (5%) than Mode II (6%). The effectiveness of the equalizer versus its power losses for both Mode I and II is summarized in Figure 5.21 to allow an easier comparative assessment.

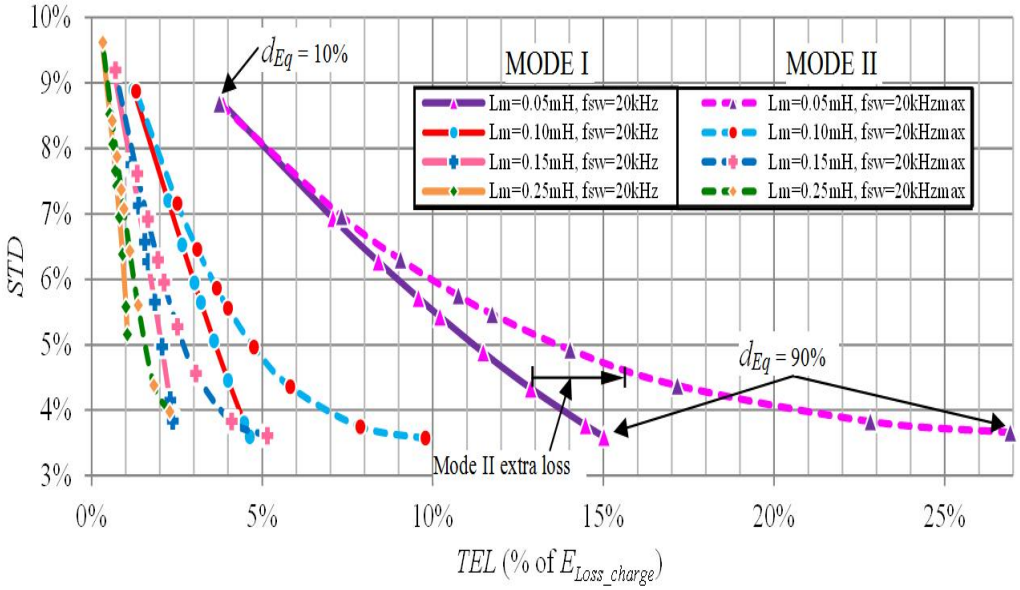


Figure 5.21 Comparison of standard deviation, *STD* of cell voltages within the stack versus total equalizing loss, *TEL* between Mode I (fix switching frequency) and Mode II (fix primary winding peak current). The graph points correspond (from left to right) to the following duty equalizing, d_{Eq}: 10%, 20%, 25%, 30%, 33%, 40%, 50%, 70% and 90%.

It can be seen that at reduced equalizing times, the two modes converge. However, as the equalizing time increases, differences appear in terms of additional losses that take place in Mode II, especially for small L_m (i.e. higher $\hat{i}_{TP}$), whilst the improvement in *STD* seems insignificant. When higher L_m (≥0.25mH)(i.e. smaller $\hat{i}_{TP}$) are used, the increase in power losses for Mode II reduces significantly whist a noticeable improvement in *STD* still exists. This can still make the choice of Mode II over Mode I acceptable. However, a detailed evaluation of the losses for a particular case of circuit parameters needs to be conducted before deciding which operating mode is more convenient.

5.6.4 Comparison between Flyback and Active Dissipative Voltage Equalizers

Another interesting situation to be analyzed is the comparison of the flyback voltage equalizer with an active-dissipative equalizer from the point of view of *STD* against *TEL*. The reason why this situation is of interest is that for the particular test conditions of this study (imbalance due to only one small capacitance cell), an active-dissipative voltage equalizer may end up bleeding the excess power from only that small cell. Let's consider the 4-cell stack of 0.525F, 0.5F, 0.5F and 0.475F capacitance again. If the charging process stops before 0.525F, 0.5F and 0.5F cells reach the threshold over-voltage, the energy losses are low compared to those of the losses in an active-regenerative voltage equalizer since the energy is dissipated from the 0.475F cell only. However, this equalization setting would result in high *STD* values, and in order to achieve lower a *STD*, activation of more than one cell's dissipative circuits and worsening of the losses would be unavoidable. For this reason, the results of an active-dissipative voltage equalizer Figure 5.2 (d) are added to the results already shown in Figure 5.21 and the cumulative results are shown in Figure 5.22.

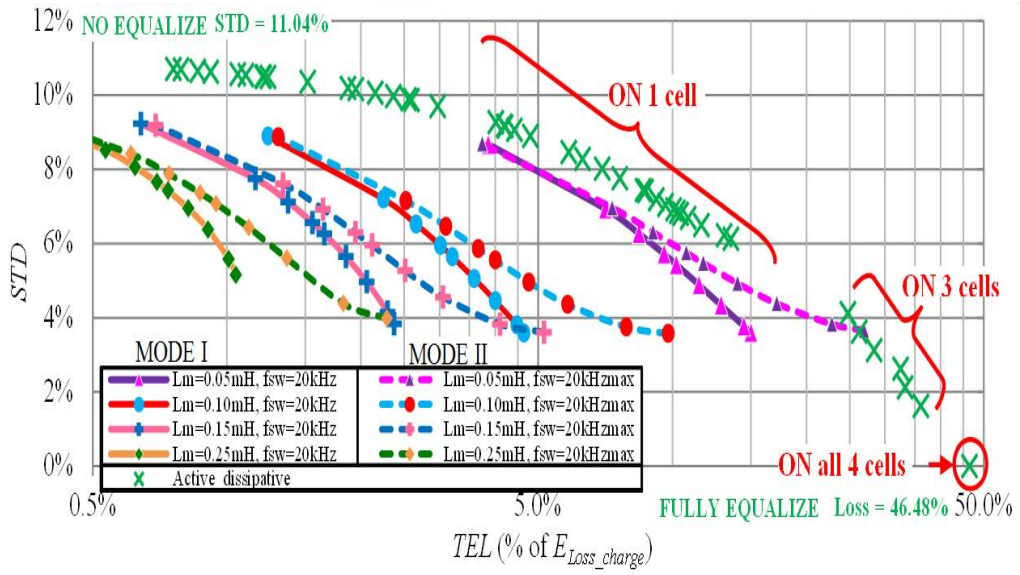


Figure 5.22 Comparison of standard deviation, *STD* of cell voltages within the stack versus total equalizing loss, *TEL* (in log scale) between the flyback voltage equalizer Mode I (fixed switching frequency), Mode II (fixed primary winding peak current) and an active-dissipative voltage equalizer. The testing duty equalizing, d_{Eq}, of testing conditions are 10%, 20%, 25%, 30%, 33%, 40%, 50%, 70% and 90%, plotted from left to right.

The active-dissipative equalizer cell is activated only when the corresponding cell voltage reaches its threshold setting, which in the situation considered will result in three distinctive regions:

- Turn ON 1 cell: the voltage equalizer for the 0.475F cell is turned on.
- Turn ON 3 cells: the voltage equalizers for the 0.475F, 0.5F and 0.5F are turned on.
- Turn ON all cells: the voltage equalizers for all cells are turned on.

When the voltage of weakest cell (0.475F) triggers the operation of its cell equalizer, it allows for that cell voltage to remain constant by bleeding all the incoming energy. It can be noted that depending on the moment the charging stops, this may result in slightly smaller *STD* than the 11% level that corresponds to charging without a voltage equalizer (Table 5.1). The longer the dissipation takes place, the more the other cells have the opportunity to catch up, but more losses are caused. The *STD* decreases until approximately 6.1% before the next two cells equal in capacitance (0.5F) reach the activation level, which correspond to a relative energy loss of 13%. Below this *STD* level, three active-dissipative circuits (0.475F, 0.5F, and 0.5F cells) will be operating which will reduce the *STD* below 2% but the losses will increase above 35% of the charging losses. This is obviously not an efficient way of maximizing the energy that can be stored by the stack. The benefit of this action is seen only as a measure to protect the cells from being overcharged. Furthermore, to eliminate the cell voltage variation of ±5% capacitance tolerance four-cell stack with the active dissipative type, the amount of energy loss is about 50% of the charging energy.

One interesting result is that the resulting curve represents an outer boundary beyond which the operation of a flyback voltage equalizer becomes also inefficient. This is the case only with the operating point of the flyback converter operating in Mode II with a very small L_m (0.05mH) or very high $\hat{i}_{TP}$ for a very long (90%) duration of the equalizing process, resulting in 27% loss. However, it can be noted that the same *STD* (3.8%) is possible with much smaller $\hat{i}_{TP}$ (i.e. L_m > 0.15mH) but causing significantly less losses (just below 2.4%). The other point is that the designer can always achieve a trade-off between the small cell-voltage *STD*, which impacts the

exploitation of the supercapacitor stack, the efficiency (small relative losses) and the size of magnetic and power semiconductors (value of L_m and $\hat{i}_{TP}$).

5.7 Conclusion

In this chapter, problems related to series-connected electrochemical cell are reported. It is shown that an over or under-voltage in one cell affects the life of the entire stack. For supercapacitors, three parameters which cause cell voltage unbalance are capacitance, equivalent series resistance and equivalent parallel resistance of the cells. The first two parameters affect cell voltages during charge-discharge operation while the last affects cell voltage during relaxation and during stand-by periods. Two ways to avoid the problem of voltage variation without employing voltage equalizers are proposed. These are matching cell characteristic before assembling the stack and decreasing rated maximum operating stack voltage while operating the stack. However, due to non-distributed temperature effects, aging and storing conditions, the problem will come back in the long term. Therefore, voltages equalizers are essential to the energy system.

Various voltage equalizer topologies have been introduced. Voltage equalizers can be categorized as passive-dissipative, active-dissipative and active-regenerative. The passive-dissipative types rely on passive components (i.e. bleeding resistors) to dissipate excess energy of overvoltage cells. Active-dissipative types employ switches to control dissipative energy by dissipating excess energy only when the cell voltage hits a predefined level. Compared the passive equalizer, it is more accurate and versatile and slightly more efficient. On the other hand, active-regenerative voltage equalizers utilize intermediate energy storage to regenerate the excess energy with the stack. Three active-regenerative voltage equalizer topologies, which are switched-capacitor, inductive, a single-switch, are discussed in comparison. Pros and cons of each topology are summarized.

Among research work in this area, trade-offs among efficiency improvement versus increase of complexity/cost have not been well reported. This chapter has addressed this shortfall by investigating the trade-offs for a common single-switch fly-back voltage equalizer. Thus, a simple fly-back voltage equalizer utilized only a single

switch is chosen for this investigation. The flyback voltage equalizer is briefly described. Two possible operating modes of the flyback voltage equalizer are studied: constant switching frequency (Mode I) and constant primary winding peak current (Mode II). Trade-offs between equalizing time and equalizing efficiency of each mode are shown. The simulation results show that for both operating modes, a reduction in the equalizing time, T_{Eq}, causes a reduction in the effectiveness, or *STD*, and the total equalizing loss, *TEL*. Operating the equalizer in Mode II can reduce *STD* slightly more than in Mode I for the same T_{Eq}, but the penalty is more energy dissipation. Depending on the design objectives, the design trade-off between cell-voltage *STD*, T_{Eq} and energy loss can be made. If maximizing efficiency is the main concern, the turn-on duration of the voltage equalizer should be as short as possible. However, if the efficiency issue can be compromised and a long operating period is possible, low level of cell voltage variation can be achieved with small amount of energy being dissipated.

Lastly, an active-dissipative voltage equalizer with resistive shunts are also studied and analyzed as a benchmark comparison with the flyback type. The results of both voltage equalizers show that the flyback type can minimize cell voltage variation with low amount of energy being dissipated than for the active-dissipative type.

Chapter 6 Supercapattery Emulators

6.1 Introduction

The prototyped Supercapattery device, as with any newly developed electrochemical energy storage devices from research laboratories, present difficulties in rapid-prototyping for large size and quantities needed for evaluation in high power applications such as hybrid electric vehicles and power grid-interface applications. Even if a manufacturing capability is available, the high cost of materials required at an initial phase impacts upon the development of larger devices and further affects system validation of the device in a real application. In addition, an environmental issue is the recycling problem of materials found in large prototypes. This is an important concern. Since some materials of the prototype are perhaps either toxic or non-environmental friendly, special decomposition schemes are required. Even though all the previously stated issues are resolved, doing practical work in electrical engineering labs with large electrochemical chemical devices which are not fully certified (from safety point of view) may raise additional restrictions.

A solution to the above problems is to implement a power electronic emulator, which mimics the electrical characteristics of the Supercapattery device with high accuracy and high speed performance. Hardware-in-loop (HIL) testing can be performed in order to verify the control design of a power electronic interface suitable for the newly developed energy storage device at a higher power level than the actual laboratory lab device can handle. However, it is noted that the artificial Supercapattery cannot behave as perfectly as the real Supercapattery since the temperature, regenerative and aging effects of the device itself cannot be emulated.

These characteristics require intensive testing with dedicated equipment. This requires long-term process control and monitoring, so it is out of scope of this thesis.

The emulator system consists of 3 parts as presented in Figure 6.1,

- Part I: a device characteristic
- Part II: a controller
- Part III: a power electronic converter

From Figure 6.1, the Signal Measurement unit receives a circuit or system variable signal and passes it to the device characteristic block as a low voltage measured signal. The Device Characteristic model block processes the measured signals and produces a reference signal either as a voltage or current reference through the modelling algorithm as happens in the real device to the Controller unit. Finally, the Controller senses the controlling parameter through its feedback loop and tries to control the Power Electronic Converter to output the model reference through PWM signals.

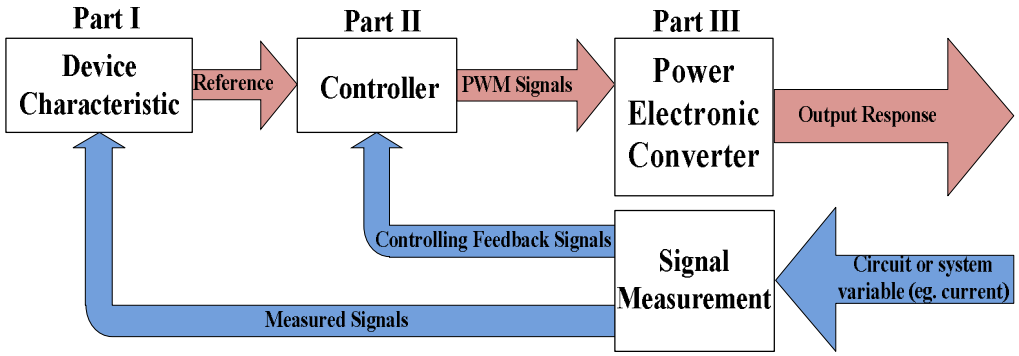


Figure 6.1 Emulator functional block diagram

In fact, Part II and III can be combined and considered as a power amplifier unit. For now, Part I and II are focused and Part III (Power electronic converter topologies) will be discussed in Section 6.2.

For Part I, either a real energy storage device or its model parameters can be used to reproduce the characteristic of the devices. The advantage of the first approach is its simplicity and is straightforward in implementation since no detailed model parameters are required. A real small supercapacitor/Supercapattery (e.g. 1-10F) can be used together with a power amplifier unit to scale up the device characteristic so as to appear as if the device is of 1000's of Farads. However, the complexity issue of

the device characteristic block is now shifted to the signal conditioning unit which interfaces between Part I and Part II&III. The interfacing circuitry must be carefully designed to handle the small rated current (<1A range) and the small rated voltage (2-3V) of the real device with good accuracy and speed. Existing measurement tools used in the power amplifier stage are designed for measuring high currents (>10 A range) and voltages (>100V range) so using these tools for low power level measurement and control would be inappropriate. Therefore, extra equipment designed for measuring the low power level with high precision is necessary. It is noted that no previous research has been done using a real device.

Alternatively, a supercapacitor/Supercapattery model obtained from the characterisation methods presented in Chapter 2 (either from a pulse constant current or an electrochemical impedance spectroscopy methods) can be implemented electronically. Use of a model approach has been reported in [122]. However, due to the nature of the model used, the output voltage equation involves differentiating the currents through the capacitor components in the model. The derivative algorithm should be avoided in a digital implementation since its accuracy is depending on a sampling time limitation. In this thesis, a voltage algorithm is developed in order to avoid derivative terms. This will be described in Section 6.5.1. The benefits of having a model of the devices and being able to implement them are scalability and safety. However, the characterizing process can be time consuming if the temperature-dependent characteristic of the device is considered. The advantages and disadvantages of using a real device approach and a model parameter approach are summarised in Table 6.1. It is shown that the model parameter main approach is better than the real device approach as scalability and flexibility of implementation are our concerns here.

Table 6.1 Comparison between using a real device and using model parameters

	Using real device	Using model parameters
Scalable flexibility	Scaling up requires more energy storage devices and/or adjustment in input/output signals. ☹	It is easy to scale up the system by duplicating equivalent models or modifying one equation. ☺
Fast prototyping	It is the quickest way to develop an emulator since there is no need to extract and implement device parameters. ☺	The characterization process to obtain model parameters takes time. ☹
Safety	Overvoltage and overcurrent conditions may occur. ☹	The system is free from overvoltage and overcurrent issues. ☺
Reproducibility	The device characteristic maybe affected by temperature and regenerative effects. ☹	The same model parameters results in the same output characteristics. ☺
Hardware complexity	Two sets of voltage and current sensors for measurement are required. ☹ - The first set is for accurately monitoring a real device voltage and current, which is also used in the protection. - The second set is for the high rated voltage and current measurement in the power amplifier stage.	Only a single set of voltage and current sensor is required (only in the power amplifier stage). ☺

The Device Characteristic block of the model parameter approach (Part I) can be implemented together with the controller (Part II) in an analogue or a digital platform. To decide which platform is more suitable for an emulator application, the design requirements of the emulator are considered:

- Response speed of the emulator during transients
- Flexibility of implementing both model and controller
- Complexity of both the model and controller structures

For the response speed during transients, the analogue platform possesses a higher bandwidth than the digital as the analogue signal is processed in a continuous domain, while the digital is performed in the discrete. This high bandwidth advantage improves the total response of the emulator in both the model and the controller parts which is recommended in an emulation of high specific-power (fast response) characteristic devices (i.e. supercapacitor/supercapattery). Additionally, using the analogue platform for the model implementation is easy since discrete

components (resistors and capacitors) can be put together exactly as the equivalent model describes.

However, flexibility of the model implementation is considered as the most important aspect. This is because different set of model parameters are obtained during the supercapattery prototype development. These parameters are implemented on the emulator and they may be disregarded as not useful after the final actual device is built. For this reason the digital platform is preferred over the analogue. Particularly, scalability is done easily in the digital by either re-programming or changing some parameters in the algorithm.

As shown in Chapter 4 the supercapacitor/supercapattery characteristics are voltage-dependent. To fully emulate this complex characteristic, different set of model parameters at each level of DC bias voltage are required. Implementing many sets of model parameters in the analogue platform would be complicated since the same equivalent models are constructed and connected together through an analogue multiplexer. On the other hand, in the digital domain, a look-up-table (LUT) algorithm can be used. In addition, using the digital platform is easy for implementing a complex controller to control a complex converter topology with many switches.

By considering all three aspects, the digital platform is preferred over the analogue as the digital platform possesses higher flexibility of both model and controller implementation and has a higher complexity handling capability. The advantages and disadvantages of using an analogue and a digital platform summarised in Table 6.2.

Table 6.2 Comparison between using analogue and digital platforms

	Using Analogue	Using Digital
Model implementing flexibility	Changing the parameters and structures of both the model and the controller require changing in all discrete component parameters. ☹	It is flexible in changing the parameters and structures of both the model and the controller. ☺
Complexity handling	The system has poor complexity handing so it is not suitable for implementing the complex equivalent model and the controller. ☹	More complex model of the device can be implemented easily by using LUT (DC bias voltage-dependent parameters).☺
Fast prototyping	It is simple to implement the equivalent model of devices with a single set of parameters. ☺	The conversion of device equivalent model into equations is required (discrete domains). ☹
Bandwidth	High bandwidth, which is necessary for emulating high power series of supercapacitors. ☺	Bandwidth depends on sampling and processing time limitations. ☹

6.2 Emulator Circuit Topology Selection

For a power electronic converter presented as Part III in Figure 6.1, both fast dynamic response and good accuracy are needed in order to replicate the behaviour of a fast response device like the supercapacitor/supercapattery.

A few research papers have been published on the emulation of electrochemical energy storage devices such as batteries and SCs [56,122,123]. In [123], an adjustable linear regulator based emulator is used since the application itself requires high accuracy and good dynamic response of both current and voltage. However, this topology is not suitable for high power and high voltage applications due to the poor efficiency of the circuits themselves; this leads to difficulty in managing the high amount of heat dissipation. For this reason, switching power electronics converter topologies have been used in order to fully emulate the characteristics of supercapacitors and batteries in [122] and [56], respectively.

The challenges of using switching converters are the selecting of the filter inductance, the filter capacitance and the switching frequency of the DC/DC converter in order to meet the demand design criteria. In fact, a high switching frequency with low values of passive components (inductance and capacitance) is essential to get fast dynamic response in both voltage and current. However, doing this will impact upon the ripple and the accuracy of both voltage and current outputs.

For these reasons, the interleaved operated bi-directional half-bridge inverters become an ideal candidate for such an application: it provides small equivalent inductance and has a high equivalent switching frequency. In [56] such a configuration based on non-coupled interleaved inductors is used. This is easier to control but for a given ripple level, it will require larger magnetics size. Increasing the number of channels may be a way to reduce ripple but as the number of interleaved channels is increased, the improvement in ripple attenuation becomes insignificant, as investigated in [124]. Therefore, an optimum number of channels should always be found for different applications. Alternatively, the other option of reducing ripple is to use coupled inductors or InterCell transformers [54,55].

In this thesis, a six-channel bi-directional half-bridge converter with interleaving connection of InterCell transformers is proposed [59] to create an emulator with high dynamic response and accurate output current and voltage waveforms. The converter was previously used in the characterisation as described and presented in Chapter 3 and it is adopt here with the emulator role, as shown in Figure 6.2. A constant voltage source, V_S is connected to the emulator input, and at the output of the emulator, the terminal voltage, v_{EMU}, is controlled to follow the real stack voltage characteristics according to the charger current, $i_{Charger}$. The InterCell transformers and the filtered capacitor, C_{EMU}, are used for filtering the switching ripple.

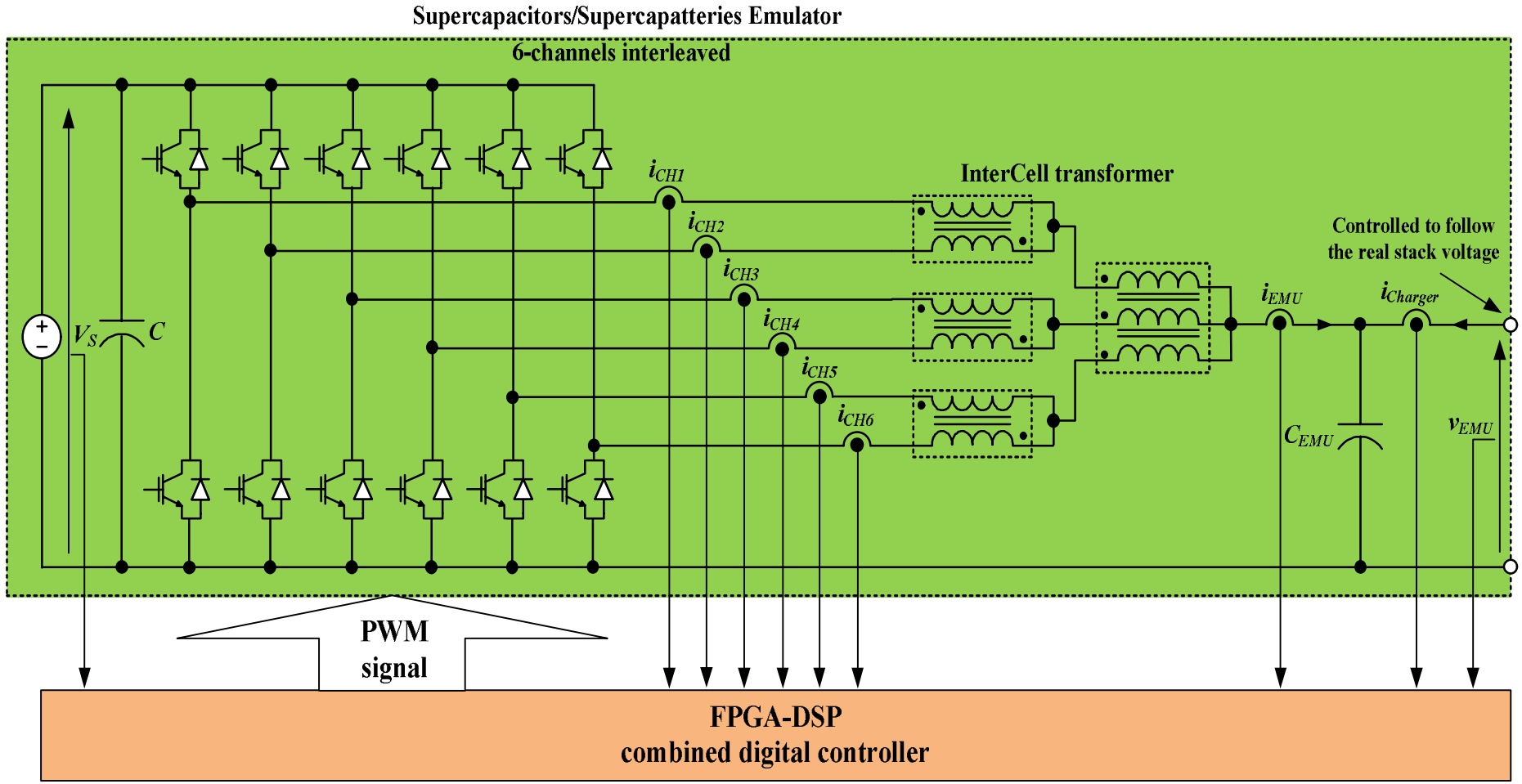


Figure 6.2 The supercapacitors/Supercapatteries emulator

6.3 Emulator Control Topology

According to Figure 6.1, the device characteristic (Part I) and the controller (Part II) are presented in more detail as the block diagram of Figure 6.3. Starting from the left side, the $i_{Charger}$ is used as the circuit or system variable of the emulator. It is measured and fed into the Model block (the Device Characteristic block in Figure 6.1). An emulator voltage reference, v_{EMU}*, is then produced and fed to the voltage controller. The model implementation will be described in Section 6.5.

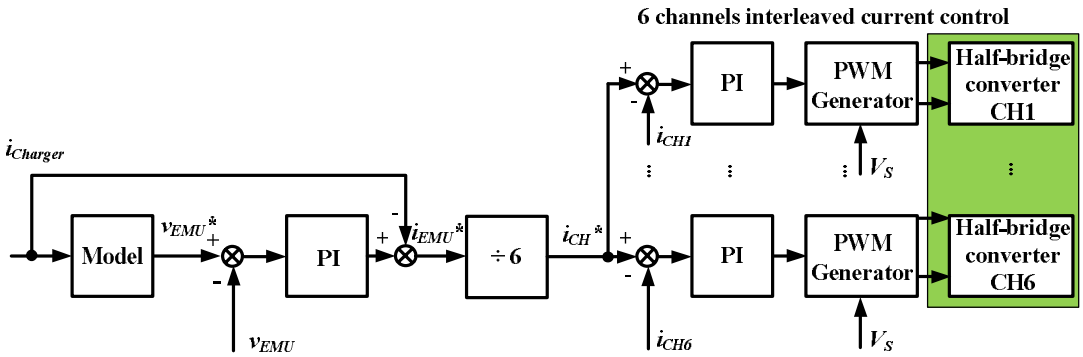


Figure 6.3 Separated channel current control

For the controller part, a proportional + integrator (PI) controller is employed in controlling both the current, i_{EMU} and the v_{EMU} of the emulator. All PI controllers are also implemented with anti-windup schemes (not shown in Figure) in order to prevent the controller saturation in the integral part. Two feedback control loops are used, the outer voltage loop and inner current loops. The current control loop is the inner loop since its controller is designed to be faster than the voltage as is usually done in the conventional control of bi-directional buck-boost converters. In addition, to improve dynamic response of the emulator, the $i_{Charger}$ signal is also used in calculating the total current control reference i_{EMU}* as a feedforward signal. This feedforward signal improves the speed of the emulator as extra information bypasses the current controller without passing through the slow voltage loop. Consequently, the i_{EMU}* is divided by 6 to give the channel current reference, i_{CH}*.

A six-channel interleaved half-bridge converter is employed so that the PWM generator units must generate six PWM signals with phase-shifted signals of $2\pi/N_{CH}$ ($2\pi/6 = 60°$) where N_{CH} is number of interleaved channels.

6.4 Emulator Control Design

From Figure 6.2, the equivalent circuit of the emulator output filter is depicted as in Figure 6.4 which includes the InterCell transformer winding resistances. It is noted that the three phase InterCell transformer is presented by three separate two-phase transformers as shown in right hand side of figure.

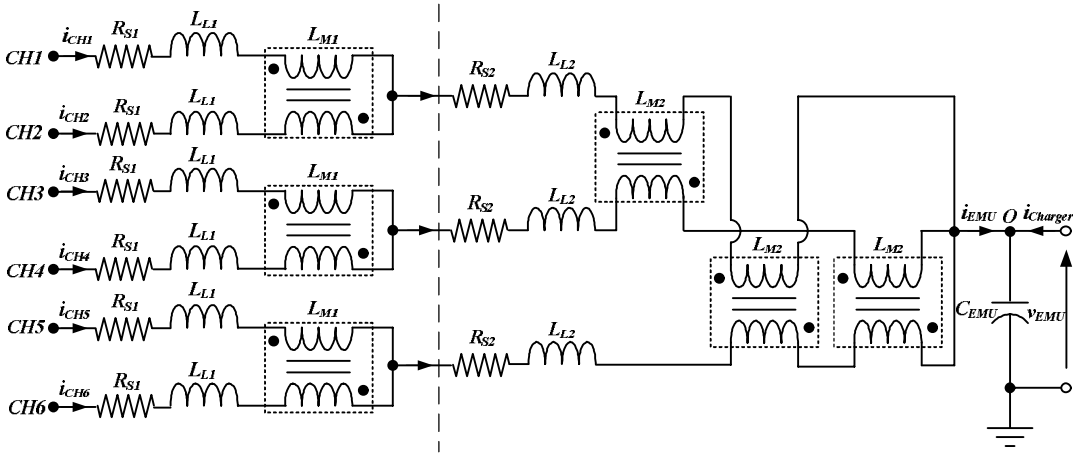


Figure 6.4 An equivalent circuit of the six-channel emulator InterCell transformer with an output capacitor

In Figure 6.4, i_{CH1} to i_{CH6} are the currents of channel 1 to 6, i_{EMU} is the emulator output current, v_{EMU} is the emulator output voltage, R_S is the winding series resistance, L_L is the leakage inductance, L_M is the magnetizing inductance and C_{EMU} is the emulator output capacitance. The subscribe number 1 and 2 represent parameters of the two-phase InterCell transformer and the three-phase InterCell transformer.

Since the i_{EMU} is divided into 6 channels equally, the duty cycle, d, for all channels is the same at steady-state. The emulator transfer functions in s-domain are:

$$\frac{I_{CH}}{V_{CH}} = \frac{1}{6}\frac{C_{EMU}s}{C_{EMU}\sum L_L s^2 + C_{EMU}\sum R_S + 6} \tag{6.1}$$

$$\frac{V_{EMU}}{I_{CH}} = \frac{6}{sC_{EMU}} \tag{6.2}$$

where I_{CH} is the emulator channel current, V_{CH} is the applied channel voltage, V_{EMU} is the emulator output voltage, $\sum R_S = R_{S1} + 2R_{S2}$ and $\sum L_L = L_{L1} + 2L_{L2}$. For full

detail of the emulator transfer function derivation, see Appendix E. It is noted that the InterCell transformer mathematic derivation is studied from [125].

The current controller with the emulator transfer function (plant) is shown in Figure 6.5 and the cascaded current and voltage controller with the plant is shown in Figure 6.6.

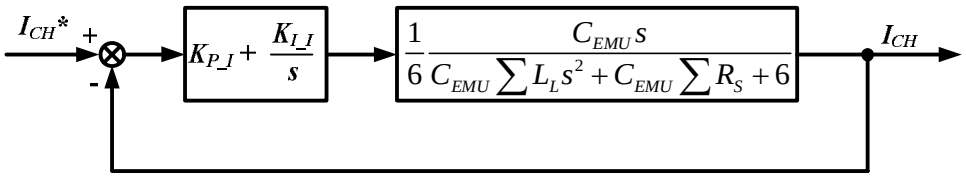


Figure 6.5 The emulator current controller plus the plant transfer function

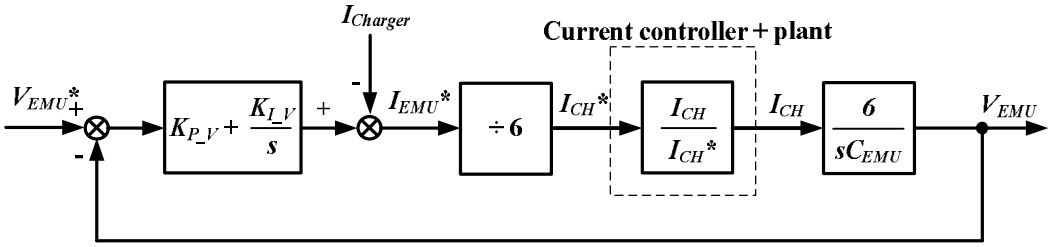


Figure 6.6 The emulator cascaded controller (voltage and current controller) plus the plant transfer function

From Figure 6.5 and Figure 6.6, I_{CH}^{*} and V_{EMU}^{*} are the emulator channel current reference and voltage reference, K_{P_I} and K_{I_I} are the current controller proportional and integral gains and K_{P_V} and K_{I_V} are the voltage controller proportional and integral gains. The plant parameters used in the controller design are presented in Section 6.6. The PI controller parameter K_P and K_I of the controllers used in Figure 6.5 and Figure 6.6 are shown in Table 6.3. The Bode plot of the close loop control is shown in Figure 6.7.

Table 6.3 Control parameters used in mode of operation

Parameters	Value
K_{P_I}	20
K_{I_I}	25000
K_{P_V}	0.3
K_{I_V}	100

From Figure 6.7, the close loop control bandwidth, BW, is limited to 200Hz, which is sufficient for emulating the supercapattery characteristic in power system applications. The gain margin, GM, is 55dB and the phase margin, PM, is 140^0. In practice, there is delay in computation and sampling processes, these high GM and PM are selected to ensure the stability of the emulator system. The experimental results with the designed control parameters are presented in Section 6.7.1.

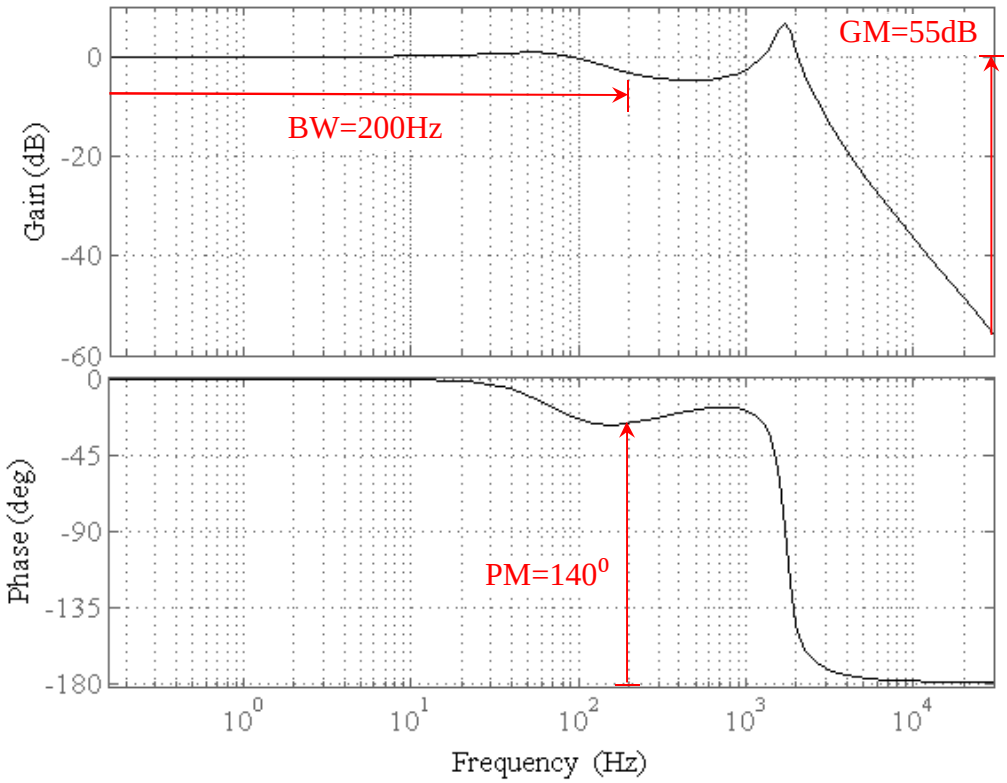


Figure 6.7 Bode plot of the emulator close loop transfer function

6.5 Model Selection and Scalability

6.5.1 Model Selection

In Chapter 2, several supercapacitor/supercapattery equivalent models and the corresponding model-derived characterizing methods are presented. Most of the proposed models in literature can be written directly in the time domain or s-domain. To implement these models into the FPGA-DSP digital platform, the models in the discrete z-domain are required. This can be done through a discretising process. In this thesis the 5th order series-parallel RC model proposed in Chapter 2 is used for the emulation as presented in Figure 6.8.

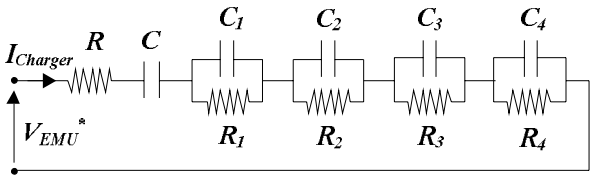


Figure 6.8 The 5th order series-parallel RC model

From Figure 6.8, the s-domain transfer function of the model can be written as

$$\frac{V_{EMU}^{*}(s)}{I_{Charger}(s)} = R + \frac{1}{sC} + \frac{R_1}{sR_1C_1+1} + \frac{R_2}{sR_2C_2+1} + \frac{R_3}{sR_3C_3+1} + \frac{R_4}{sR_4C_4+1} \tag{6.3}$$

where V_{EMU}* and $I_{Charger}$ are emulator voltage reference charging current either in s-domain or z-domain. Combining all terms in (6.3) gives a polynomial form:

$$\frac{V_{EMU}^{*}(s)}{I_{Charger}(s)} = \frac{A_0 + A_1 s + A_2 s^2 + A_3 s^3 + A_4 s^4 + A_5 s^5}{B_0 + B_1 s + B_2 s^2 + B_3 s^3 + B_4 s^4 + B_5 s^5} \tag{6.4}$$

where A_0 to A_5 and B_0 to B_5 are coefficients of nominator and denominator terms of the s-domain transfer function. The MATLAB command 'c2d' is used to convert (6.4) from the s-domain to z-domain so that the transfer function becomes

$$\frac{V_{EMU}^{*}(z)}{I_{Charger}(z)} = \frac{a_0 + a_1 z^{-1} + a_2 z^{-2} + a_3 z^{-3} + a_4 z^{-4} + a_5 z^{-5}}{b_0 + b_1 z^{-1} + b_2 z^{-2} + b_3 z^{-3} + b_4 z^{-4} + b_5 z^{-5}} \tag{6.5}$$

The z^{-1} means delay by one sample. The discrete transfer function (6.5) is presented in Figure 6.9, which is called canonical form in a digital filter design.

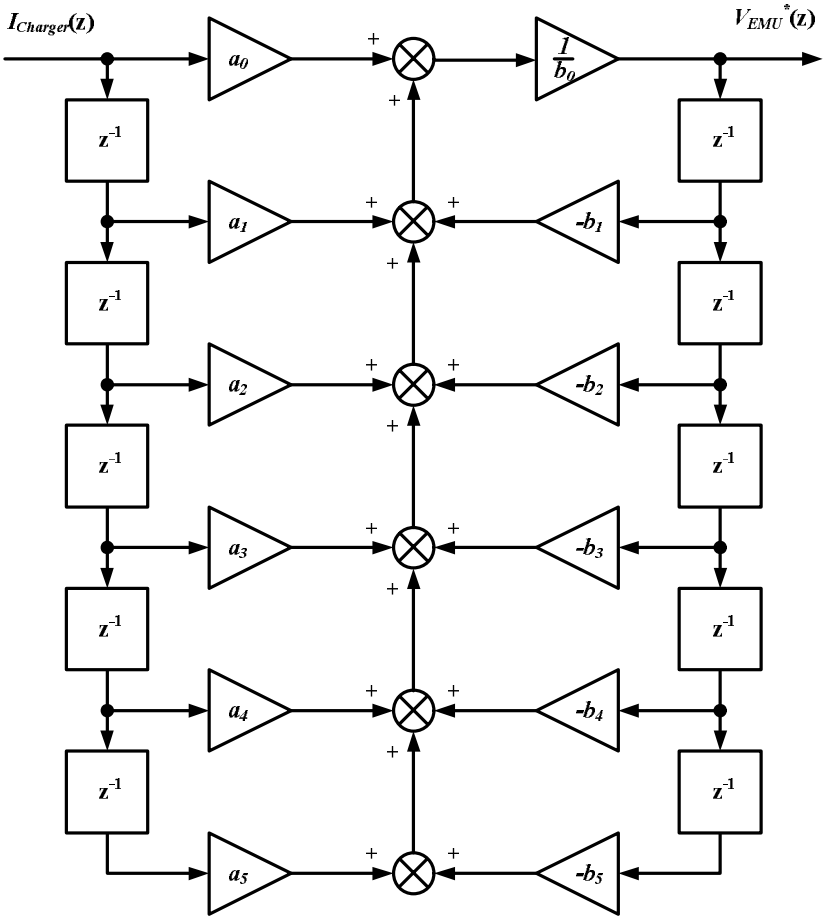


Figure 6.9 Canonical form of the model used for implementation into the digital platform

In fact, the discretisation of (6.4) may lead to oscillations in implementation. In particular, when emulating fast-response devices like supercapacitors/supercapatteries, the position of the poles in the discrete domain is near the unit-circle (only on unit circle if $R_i \rightarrow 0$, otherwise they are near it), which means that the emulated system is on the verge of being unstable. To implement (6.5) without oscillations, an additional knowledge of digital filter design is needed, but this is out of scope of this thesis.

To overcome the existence of under-damped poles arising from discretisation, an alternative implementation can be used. Here, V_{EMU}* is considered as a summation of voltage drops across each series connected component as presented in Figure 6.10 and described as:

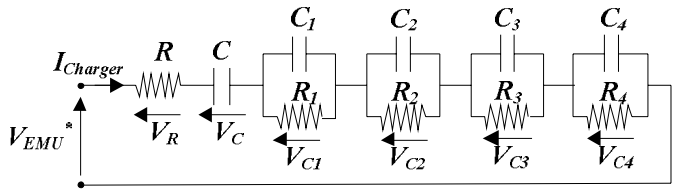


Figure 6.10 The 5th order series-parallel RC model with a summation of voltage drop calculation

$$V_{EMU}{}^{*} = V_R + V_C + V_{C1} + V_{C2} + V_{C3} + V_{C4} \tag{6.6}$$

Where V_R, V_C, V_{C1}, V_{C2}, V_{C3} and V_{C4} are calculated from (6.7) to (6.12) with a sampling frequency T_S that used in the digital platform. Using the Euler discretisation of $\dot{x} = \left[x(k) - x(k-1) \right] / T$:

$$V_R(k) = I_{Charger}(k) R \tag{6.7}$$

$$V_C(k) = V_C(k-1) + \left(I_{Charger}(k) \right) \frac{T_S}{C} \tag{6.8}$$

$$V_{C1}(k) = V_{C1}(k-1) + \left(I_{Charger}(k) - \frac{V_{C1}(k)}{R_1} \right) \frac{T_S}{C_1} \tag{6.9}$$

$$V_{C2}(k) = V_{C2}(k-1) + \left(I_{Charger}(k) - \frac{V_{C2}(k)}{R_2} \right) \frac{T_S}{C_2} \tag{6.10}$$

$$V_{C3}(k) = V_{C3}(k-1) + \left(I_{Charger}(k) - \frac{V_{C3}(k)}{R_3} \right) \frac{T_S}{C_3} \tag{6.11}$$

$$V_{C4}(k) = V_{C4}(k-1) + \left(I_{Charger}(k) - \frac{V_{C1}(k)}{R_4} \right) \frac{T_S}{C_4} \tag{6.12}$$

It can be seen that only 1st order equations are used in calculating V_{EMU}* so the oscillation problem has gone. In addition, from the concept of voltage drop summation, more parallel RC cells can be added to increase the total order of the model for better fitting.

6.5.2 Scalability of the Model

By considering the equivalent model presented in Figure 6.10 as a single impedance *Z*, standard impedance rules can be used to create series and parallel cell connections to build up bigger units. Figure 6.11 and Figure 6.12 show a series-connected configuration and a parallel-connected configuration, which yield equivalent impedances Z_S and Z_P.

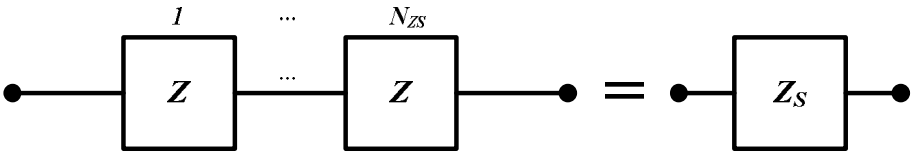


Figure 6.11 The series connection of the model blocks

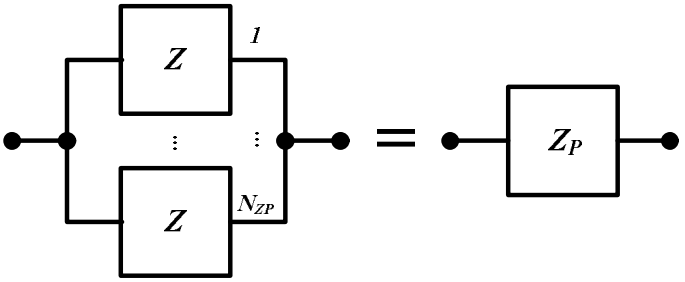


Figure 6.12 The parallel connection of the model blocks

From Figure 6.11, Z_S is

$$Z_S = N_{ZS} Z \tag{6.13}$$

$$Z_S = N_{ZS} R + \frac{N_{ZS}}{sC} + \frac{N_{ZS} R_1}{sR_1 C_1 + 1} + \frac{N_{ZS} R_2}{sR_2 C_2 + 1} + \frac{N_{ZS} R_3}{sR_3 C_3 + 1} + \frac{N_{ZS} R_4}{sR_4 C_4 + 1} \tag{6.14}$$

To comply with the equivalent model implementation proposed in Figure 6.10, (6.14) is modified with new parameters as:

$$Z_S = R_{NS} + \frac{1}{sC_{NS}} + \frac{R_{1S}}{sR_{1S} C_{1S} + 1} + \frac{R_{2S}}{sR_{2S} C_{2S} + 1} + \frac{R_{3S}}{sR_{3S} C_{3S} + 1} + \frac{R_{4S}}{sR_{4S} C_{4S} + 1} \tag{6.15}$$

Where $R_{NS} = N_{ZS}R$, $C_{NS} = C/N_{ZS}$, $R_{1S} = N_{ZS}R_1$, $C_{1S} = C_1/N_{ZS}$, $R_{2S} = N_{ZS}R_2$, $C_{2S} = C_2/N_S$, $R_{3S} = N_{ZS}R_3$, $C_{3S} = C_3/N_{ZS}$, $R_{4S} = N_{ZS}R_4$ and $C_{4S} = C_4/N_{ZS}$. Note that (6.15) is similar to (6.3). Therefore, from (6.15), the implementation for scaling-up a stack of N_{ZS} series-connected cells can be achieved by substituting, *R* with R_{NS}, *C* with C_{NS}, R_1

with R_{1S}, R_2 with R_{2S}, R_3 with R_{3S}, R_4 with R_{4S}, C_1 with C_{1S}, C_2 with C_{2S}, C_3 with C_{3S} andC_4 with C_{4S} in (6.7) to (6.12).

From Figure 6.12, Z_P is

$$Z_P = \frac{Z}{N_{ZP}} \tag{6.16}$$

$$Z_P = \frac{R}{N_{ZP}} + \frac{1/N_{ZP}}{sC} + \frac{R_1/N_{ZP}}{sR_1C_1+1} + \frac{R_2/N_{ZP}}{sR_2C_2+1} + \frac{R_3/N_{ZP}}{sR_3C_3+1} + \frac{R_4/N_{ZP}}{sR_4C_4+1} \tag{6.17}$$

$$Z_P = R_{NP} + \frac{1}{sC_{NP}} + \frac{R_{1P}}{sR_{1P}C_{1P}+1} + \frac{R_{2P}}{sR_{2P}C_{2P}+1} + \frac{R_{3P}}{sR_{3P}C_{3P}+1} + \frac{R_{4P}}{sR_{4P}C_{4P}+1} \tag{6.18}$$

Where $R_{NP} = R/N_{ZP}$, $C_{NP} = N_{ZP}C$, $R_{1P} = R_1/N_{ZP}$, $C_{1P} = N_{ZP}C_1$, $R_{2P} = R_2/N_{ZP}$, $C_{2P} = N_{ZP}C_2$, $R_{3P} = R_3/N_{ZP}$, $C_{3P} = N_{ZP}C_3$, $R_{4P} = R_4/N_{ZP}$ and$C_{4P} = N_{ZP}C_4$. Note that (6.18) is similar to (6.3). Therefore, from (6.18), the implementation for scaling-up a stack of N_P parallel-connected cells can be achieved by substituting, R with R_{NP}, C with C_{NP}, R_1 with R_{1P}, R_2 with R_{2P}, R_3 with R_{3P}, R_4 with R_{4P}, C_1 with C_{1P}, C_2 with C_{2P}, C_3 with C_{3P} and C_4 with C_{4P} in (6.7) to (6.12).

According to Figure 6.11 and Figure 6.12, the model can also scale up in a series-parallel pattern as presented in Figure 6.13, which results in a series-parallel connected equivalent impedance, Z_{SP} as described in (6.19).

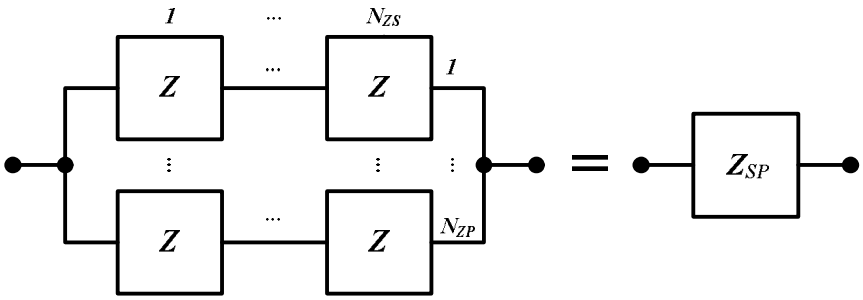


Figure 6.13 The series-parallel connection of the model blocks

$$Z_{SP} = \frac{N_{ZS}}{N_{ZP}} Z \tag{6.19}$$

$$Z_{SP} = \frac{N_{ZS}}{N_{ZP}} R + \frac{N_{ZS}/N_{ZP}}{sC} + \frac{R_1\left(N_{ZS}/N_{ZP}\right)}{sR_1C_1+1} + \frac{R_2\left(N_{ZS}/N_{ZP}\right)}{sR_2C_2+1} + \frac{R_3\left(N_S/N_P\right)}{sR_3C_3+1} + \frac{R_4\left(N_{ZS}/N_{ZP}\right)}{sR_4C_4+1} \quad (6.20)$$

$$Z_{SP} = R_{NSP} + \frac{1}{sC_{NSP}} + \frac{R_{1SP}}{sR_{1SP}C_{1SP}+1} + \frac{R_{2SP}}{sR_{2SP}C_{2SP}+1} + \frac{R_{3SP}}{sR_{3SP}C_{3SP}+1} + \frac{R_{4SP}}{sR_{4SP}C_{4SP}+1} \quad (6.21)$$

Where $R_{NSP} = (N_{ZS}/N_{ZP})R$, $C_{NSP} = (N_{ZP}/N_{ZS})C$, $R_{1SP} = (N_{ZS}/N_{ZP})R_1$, $C_{1SP} = (N_{ZP}/N_{ZS})C_1$, $R_{2SP} = (N_{ZS}/N_{ZP})R_2$, $C_{2SP} = (N_{ZP}/N_{ZS})C_2$, $R_{3SP} = (N_{ZS}/N_{ZP})R_3$, $C_{3SP} = (N_{ZP}/N_{ZS})C_3$, $R_{4SP} = (N_{ZS}/N_{ZP})R_4$ and $C_{4SP} = (N_{ZP}/N_{ZS})C_4$,

Again by using (6.7) to (6.12) with new parameters, the model presented in (6.21) is a scaled-up system using N_{ZS} series and N_{ZP} parallel connected cells to produce an $N_{ZS} \times N_{ZP}$ cell system. If $N_{ZS} = N_{ZP,}$ the model parameters of the scaled-up unit are the same as a model of a single unit, but the rated current and voltage are increased by N_{ZP} and N_{ZS}. For simplicity, the last approach is used in scaling up the model in the implementation.

6.6 Experimental Rig Setup

Figure 6.14 shows the schematic diagram of the test bench which comprises the supercapattery emulator and the charger typically associated with any energy storage device. The charger also employs a six-channel bi-directional half-bridge converter with interleaving connection of InterCell transformers. The C_{EMU} is a capacitor which helps in smoothing the output voltage ripple caused by the switching of the interleaved converter. The voltage across C_{EMU}, v_{EMU}, is monitored by the emulator which is acting as the real supercapattery device to the charger. The control algorithm of both the charger and the emulator are implemented separately in two FPGA-DSP platforms. Since the emulator must act corresponding to the charger action, the control of the charger and the emulator can be considered as master and slave.

To allow circulation of the power, the DC-links of the emulator V_{DC1} and the charger circuit V_{DC2} are connected to the same DC power supply unit in a back to back connection. Hence, the energy needed from the DC power supply is just for compensating the power losses.

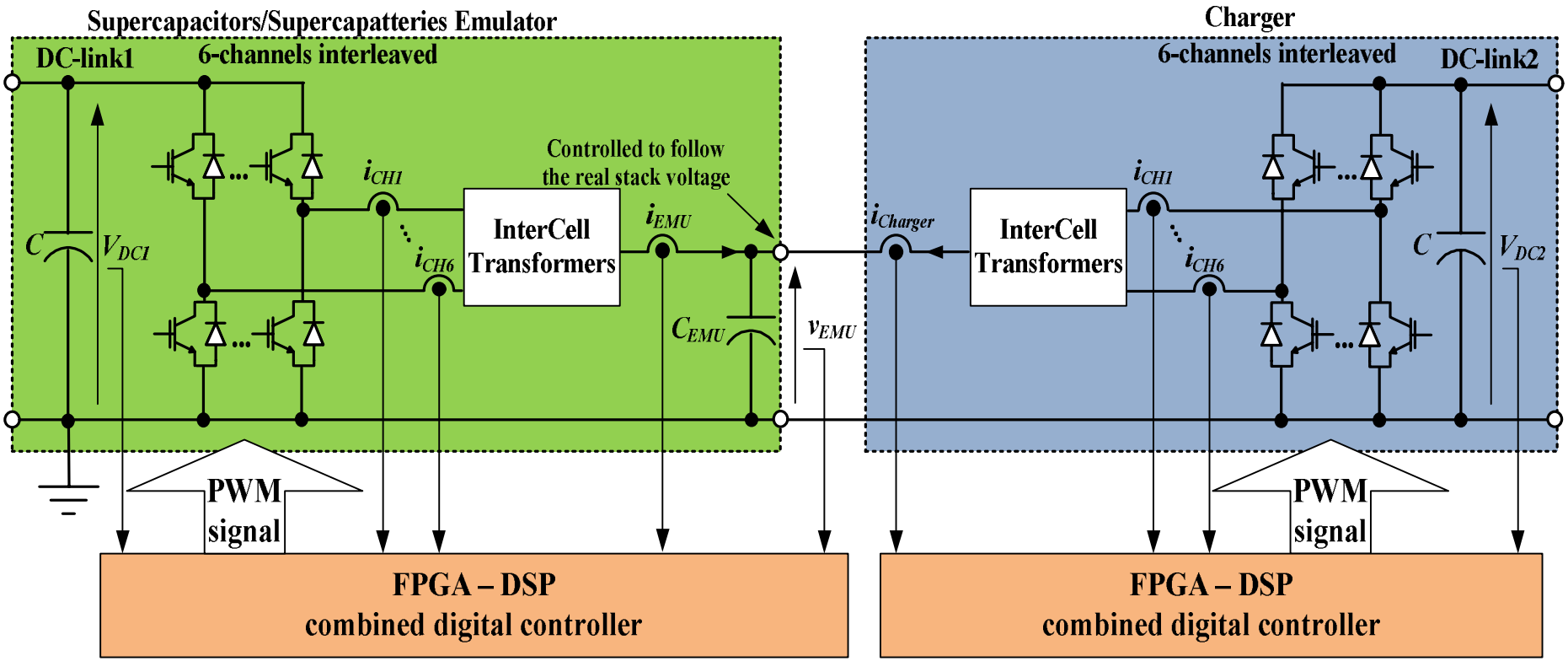


Figure 6.14 The six-channel interleaved bi-directional DC/DC half-bridge converter topology used as the supercapattery emulator (left side) and used as a charger circuit (right side)

For the InterCell transformers presented in Figure 6.14, four coupled inductors are used and are arranged as depicted in Figure 6.15. The coupled inductors consist of three two-phase InterCell transformers designed as in [55] and a three-phase InterCell transformer to accumulate the overall inductor current. The main reason for the three-phase InterCell transformer connected to the outputs of the two-phase transformers is to prevent a circulation current between them. Additional ripple cancellation is gained if the three-phase InterCell transformer is designed such that it has a high ratio of magnetising inductance, L_M, to leakage inductance, L_L.

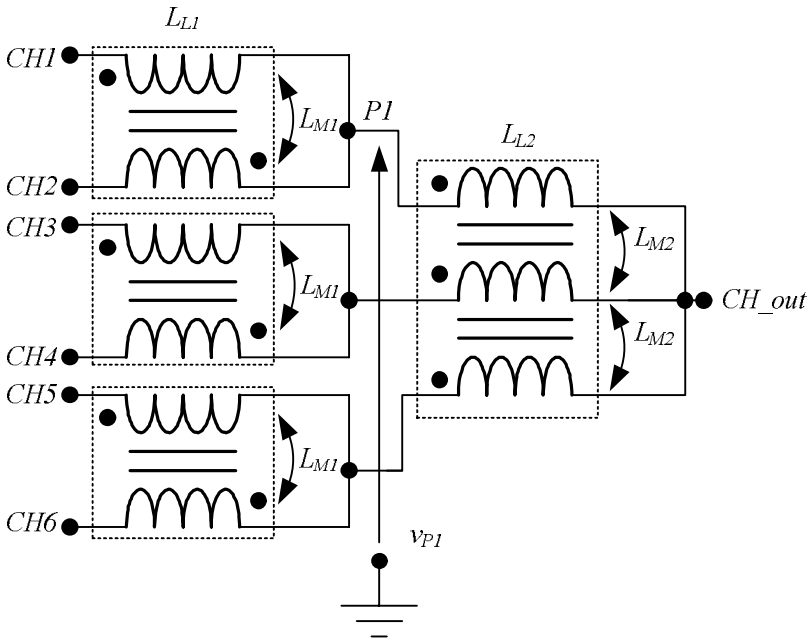


Figure 6.15 InterCell transformer used in Emulator

From Figure 6.15, the six channels of the interleaved converter, *CH1-CH6*, are switched using six PWM signals phase-shifted by 2π/6 (60°) which are generated by using a FPGA-DSP digital control platform as presented in Figure 6.14. The 6 channels are operated with the following phase shift sequence: *CH1*(0°) + *CH2*(180°), *CH3*(60°) + *CH4*(240°) and *CH5*(120°) + *CH6*(300°). The switching frequency of each channel is 10 kHz, so an effective switching frequency of 60 kHz at the output, *CH_out*, is achieved.

The inductance parameters of the InterCell transformers used in the emulator are listed in Table 6.4. The 100Hz inductance parameters are given for both the two-phase and the three-phase transformers and these parameters are matched with the parameters used in the control design in Section 6.4. In addition, the inductance parameters of the two-phase and the three-phase transformers are given at 10 kHz

and 20 kHz respectively since these are the frequencies of the current ripple of each transformer. It can be noted that the value of the inductances of the three-phase transformer is smaller as it deals with a current ripple of double the switching frequency of the DC/DC converter. The two-phase type is designed for a rated current of 15A per channel and the three-phase type is designed to handle 30A per channel. The two-phase type is constructed from Amorphous core (Metglas® AMCC100) whist the three-phase is a conventional 3-phase AC choke. It can be note that the inductance parameters of all windings within the same transformer type (i.e. either two-phase or three-phase types) are similar so only one is shown. In Table 6.4, the winding resistances of both InterCell transformers, R_S, are also included. Subscribe 1 and 2 represent parameters of two-phase and three-phase InterCell transformer.

Table 6.4 Parameters of InterCell transformer

Parameter	R_{S1} @100Hz (mΩ)	L_{L1} @100Hz (µH)	L_{L1} @10kHz (µH)	L_{M1} @10kHz (mH)	R_{S2} @100Hz (mΩ)	L_{L2} @100Hz (µH)	L_{L2} @20kHz (µH)	L_{M2} @20kHz (mH)	C_{EMU} @100Hz (µF)
Value	125	575	400	1.76	30.6	253	258	1	96

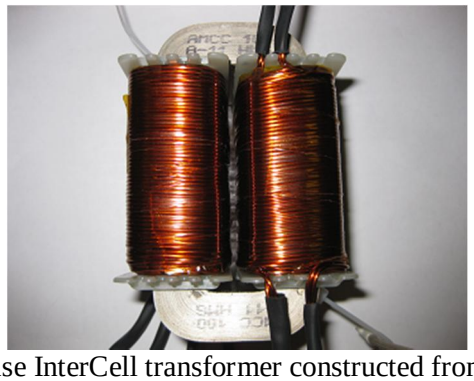


Figure 6.16 A two-phase InterCell transformer constructed from Amorphous material (Metglas® AMCC100)

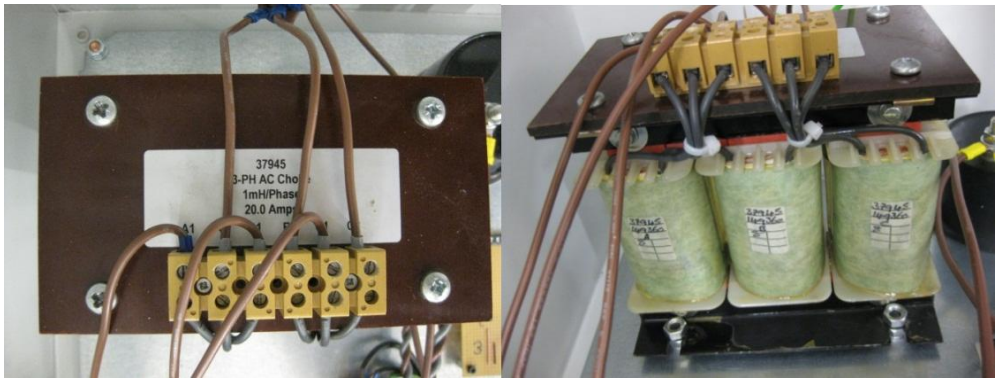


Figure 6.17 A three-phase InterCell transformer

6.7 Experimental Results

In this section, the steady state and the dynamic performance evaluation of the interleaved converter that is the core of the supercapattery emulator is presented first in Section 6.7.1. Then, in Section 6.7.2, the evaluation of the supercapattery emulator against the real device characteristics is shown in different operating modes typical for an energy storage device:

- discharge over a fixed value resistor (Section 6.7.2.1)
- pulse current (Section 6.7.2.2)
- constant current charge-discharge cycling (Section 6.7.2.3)
- constant power charge-discharge cycling (Section 6.7.2.4)

In all cases, the emulator is operated with the separated channel current control (see Figure 6.3).

6.7.1 Performance Evaluation of the Interleaved Converter

6.7.1.1 Steady State Performance of the Interleaved Converter

The emulator is operated in steady state to supply a constant $i_{Charger}$ (Figure 6.16). The test results are shown in Figure 6.18. In Figure 6.18, the converter is operated without feedforward current from the charger (Figure 6.3). The 6 channels interleaved are implemented successfully as the phase shift between i_{CH1}, i_{CH3} and i_{CH5} is seen to be 60°. The amount of overall ripple current of the interleaved converter output current i_{EMU} is very small (less than 500mA peak to peak when V_{DC1} = 50V). The currents also have a frequency six times higher than the switching frequency (10kHz), which means that the converter operates with a much higher virtual switching frequency. It can be concluded that the ripple current is small. However, due to a sampling frequency limitation of the FPGA-DSP platform and the processing time spent (25µs), the output cannot be controlled perfectly as designed.

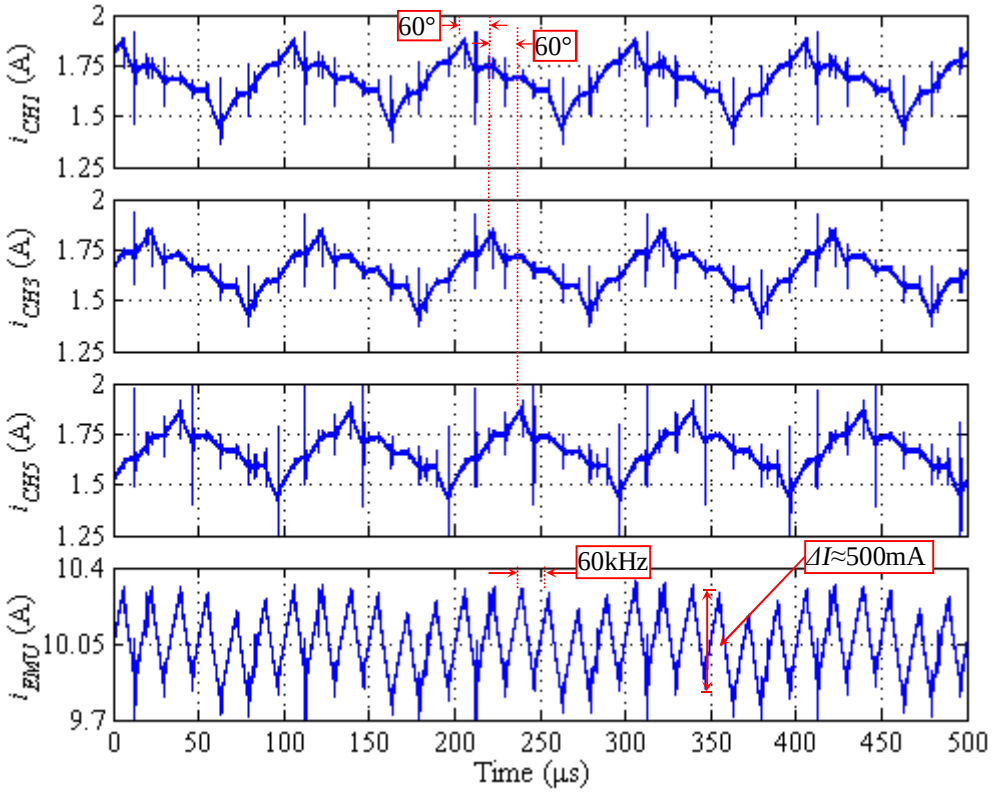


Figure 6.18 Channel currents *CH1*, *CH3* and *CH5* and total emulator current without feed-forward current from charger

6.7.1.2 The Current Controller Response Test with Step Current

The emulator output with C_{EMU} removed is suddenly connected to a resistive load, R_{Load}, as presented in Figure 6.19, so a step current is produced. With R_{Load} = 1.5Ω, an i_{EMU}* step change of 10A is applied and the result is shown in Figure 6.20. The dynamic response following a 10A current step is good, showing a 50μs rise time with the total current of the interleaved converter settling in less than 200 μs. In Figure 6.20, v_{P1} (depicted in Figure 6.15) is also measured in order to observe the output voltage of 2 interleaved channels.

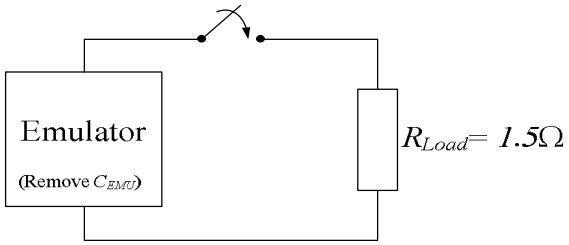


Figure 6.19 The emulator tested with a step current change produced by suddenly connecting to the resistive load

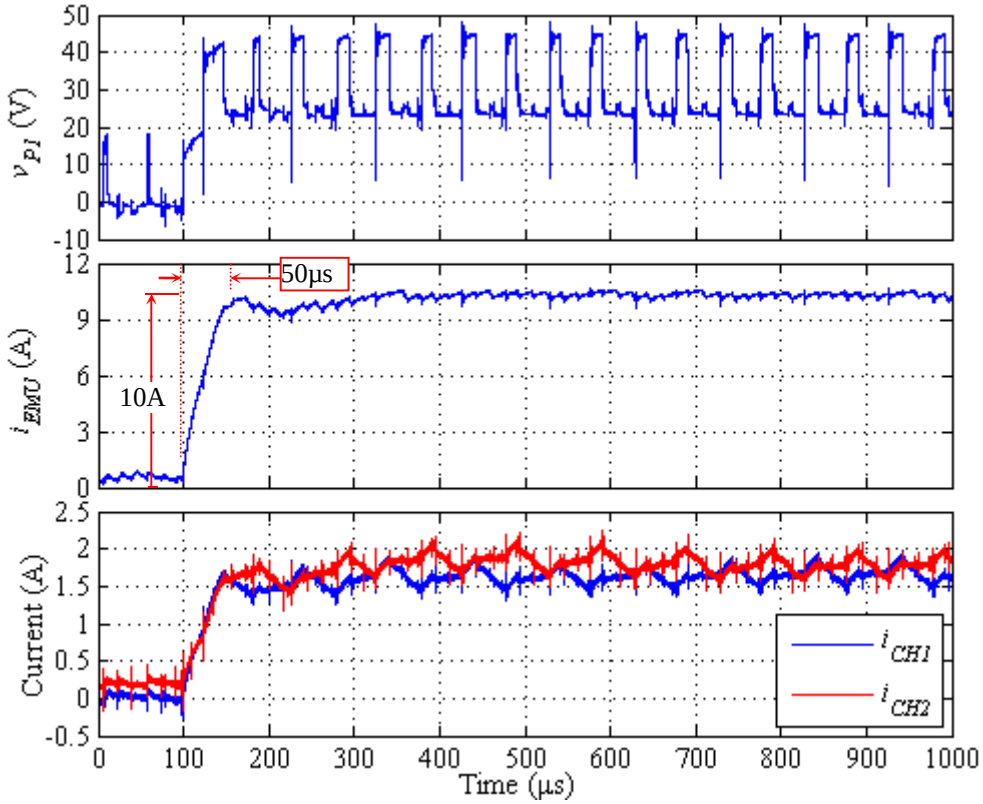


Figure 6.20 Testing transient response of the emulator with a step current of 10A under resistive loading.

6.7.1.3 Testing the Performance of the Voltage Controller

This test is done in the similar way as presented in Figure 6.19 but with the C_{EMU} connected. The performance of the voltage controller is tested with a 20V step change in the v_{EMU}* and the result is presented in Figure 6.21. Since the supercapattery stack voltage is rated at 19V, the emulator output voltage is chosen and tested at 20V. Due to the presence of a second order LC filter on the output of emulator (across C_{EMU} in Figure 6.14), the response has a small oscillatory overshoot. A fast voltage dynamic is desirable. To do this, C_{EMU} must be charged/discharged at a high rate and the converter must be rated for this peak current.

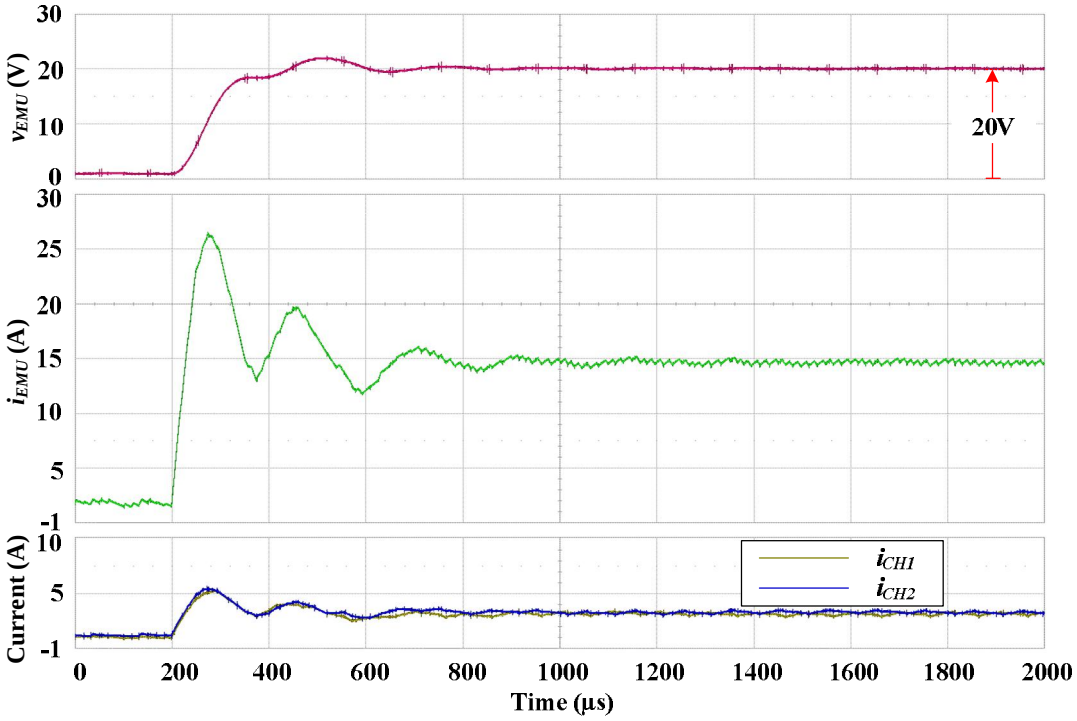


Figure 6.21 The emulator voltage control performance testing

6.7.2 Evaluation of the Supercapattery Emulator

6.7.2.1 Emulator Evaluation of a Fixed Resistor Discharge Test

In this section, the supercapattery equivalent model with the model parameters presented in Section 6.5.1 and Chapter 4 is used and is implemented in the DSP to replicate the behaviour of the supercapattery. The dependence of the model parameters C_1 to C_4 and R_1 to R_4 on the value of the DC bias voltage is considered in a simplified linear relationship. Initially, the Model block is disabled and in order to pre-charge C_{EMU}, the v_{EMU}* is set to 19V by the user directly, which is the maximum voltage of the real supercapattery stack. Then, suddenly an external load resistor of 1.5Ω is connected to the emulator output terminals (same as in the previous section), which causes the current to rise sharply to 12A as presented in Figure 6.22. The voltage step due to the series resistance R of the model depicted in Figure 6.10 is also indicated in Figure 6.22. Since the exponential decay of the emulator's voltage is not so obvious due to the time scale, a straight dashed line is added to Figure 6.22. The limitations of the emulator in terms of reaction speed, which affects its high frequency (kHz range) bandwidth, can be seen in Figure 6.23, which zoom in on the transition moment. The initial voltage drop momentarily

exceeds the expected level, which is caused by the delay of the emulator's current controller. It is corrected in 400 µs.

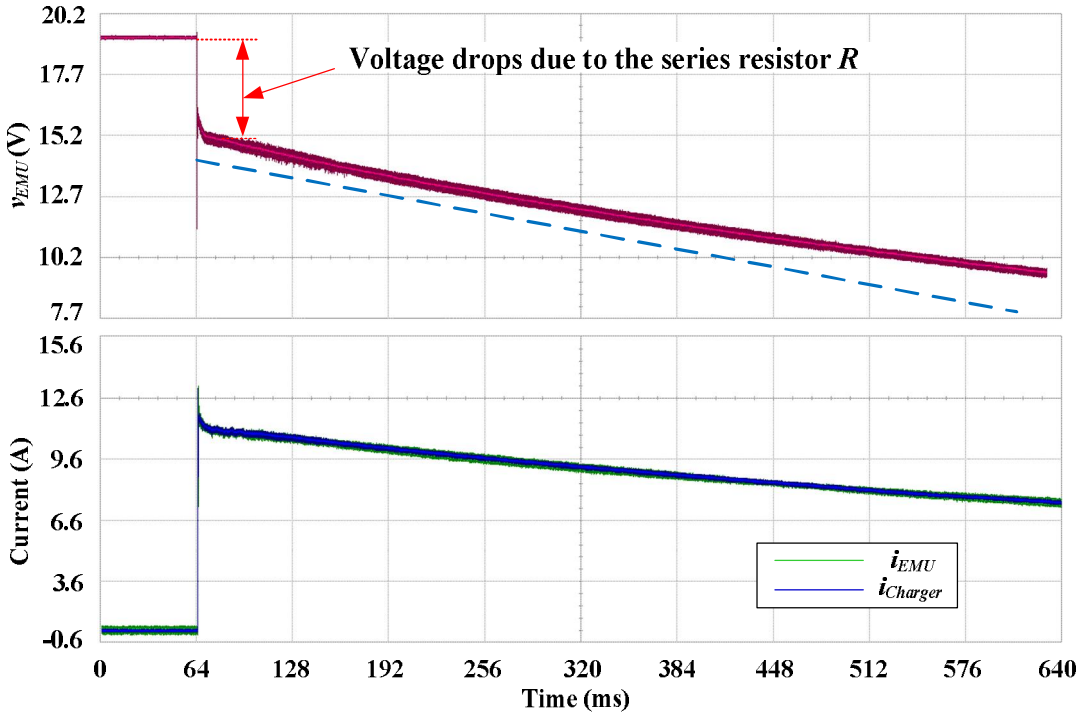


Figure 6.22 Supercapattery emulator discharge testing with a fixed value resistor 1.5Ω

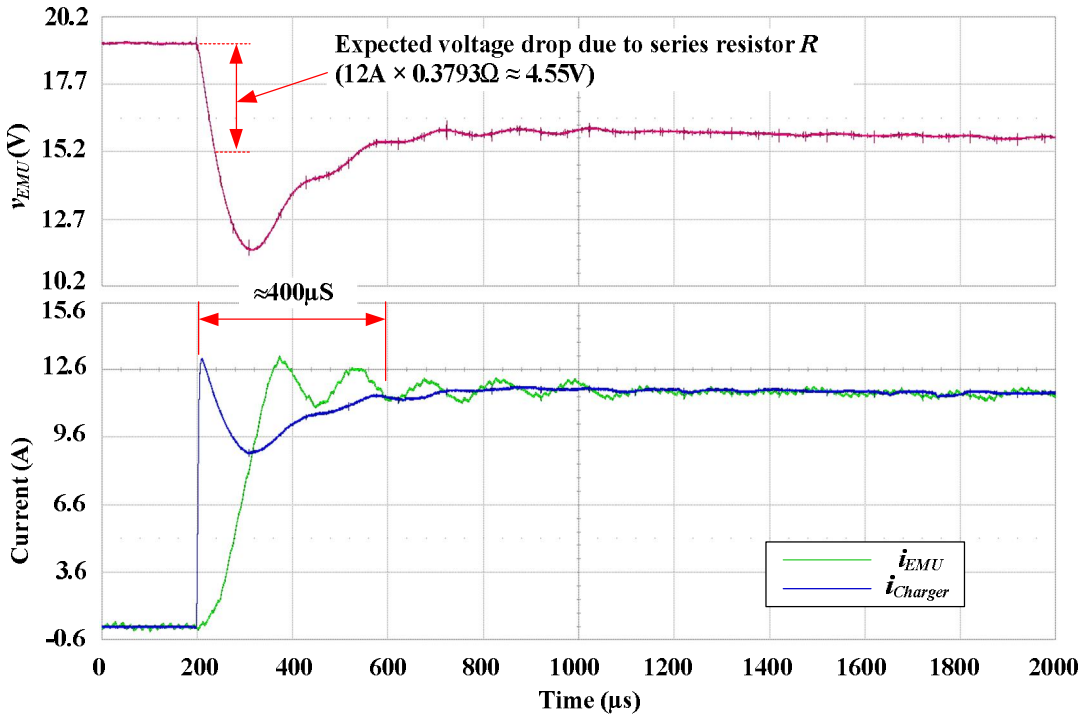


Figure 6.23 Zoom in during the transient period

6.7.2.2 Emulator Evaluation under a Current Pulse Test

The emulator is tested for a discharged current pulse as shown in Figure 6.24, which is the method presented and discussed in Chapter 2. Firstly, the v_{EMU} is controlled to 10.3V such that the emulator has the same initial condition as that of the test with the real stack. Then, an $i_{Charger}$ of -5.8A for 163.8ms (considered as a discharged pulse current) is applied to both the real device and the emulator. The emulator voltage response is found to fit very well with the experimental result of the supercapattery as shown in Chapter 4. This result was used to extract the equivalent parameters from the relaxation process.

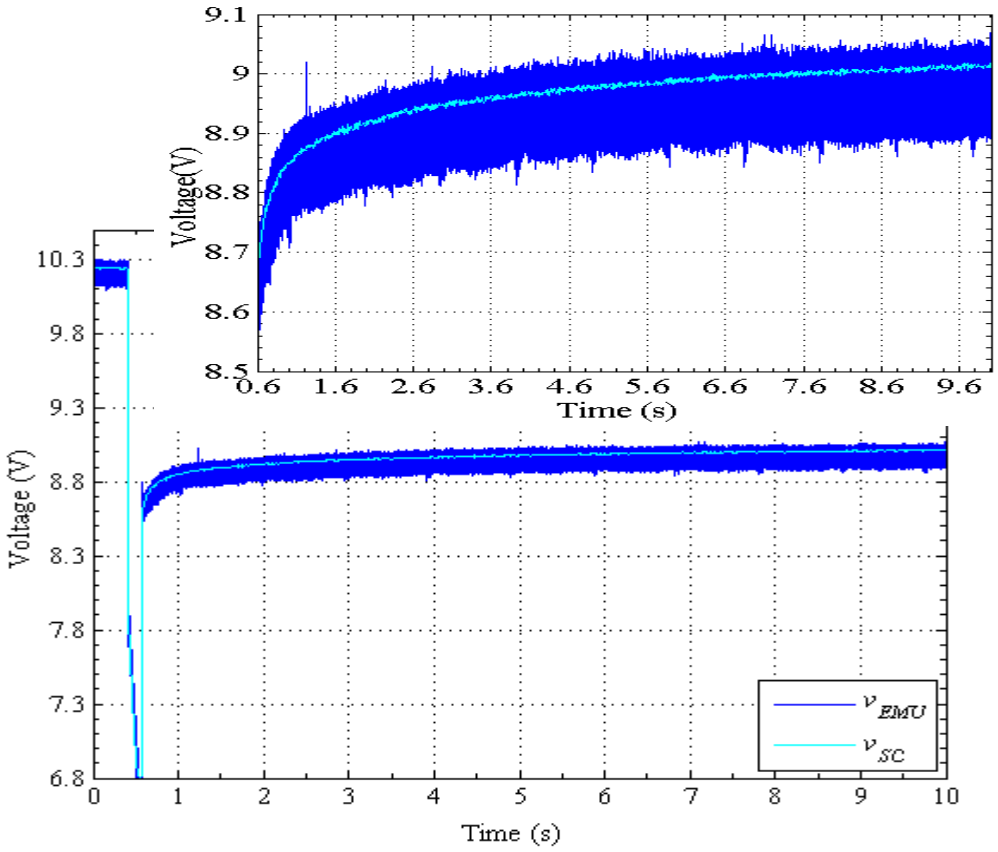


Figure 6.24 Supercapattery stack (Real) versus emulated replica (EMU) testing under constant pulse current control of -5.8A/163.8ms (upper subplot details the relaxation process).

Note that the tracking during the current pulse is acceptable. However, some small differences are seen during the relaxation process, which is highlighted in the zoom-in section added on the top of Figure 6.24.

6.7.2.3 Emulator Evaluation under Constant Current Cycling

A constant current control of ±6A square waveform is performed on both the real supercapattery and its emulated replica. This is done by setting $i_{Charger}$ equal to 6A. The minimum and maximum operating voltages are set to 5 and 19V for both cases, which results in minimum and maximum operating powers of 30W and 114W. The test results of the voltage and power of the real device, v_{SC} and p_{SC} and the voltage and power of the emulator, v_{EMU} and p_{EMU}, under similar $i_{Charger}$ are shown in Figure 6.25 and Figure 6.26. Since feed-forward of the charger current is implemented, tracking performance of the emulator current is excellent even during the transition from discharging to charging and vice versa as highlighted in the zoom as presented in Figure 6.27 (a) and (b). However, small differences exist in the charge-discharge duty cycle, d_{CD}, and the charge-discharge cycle period, T_{CD}: 49.17% and 1.81s for the real Supercapattery stack and 48.9% and 1.84s for the emulated replica. These d_{CD} and T_{CD} differences between the real stack and the emulator may be due to small difference in the applied switching current ripple between Figure 6.25 and Figure 6.26 since they were produced with different test rigs (Rig I and Rig II). Rig I uses Hysteresis current control while Rig II uses a PI current control and PWM. In addition, the emulator had a fairly large the capacitive filter/smooth inductor.

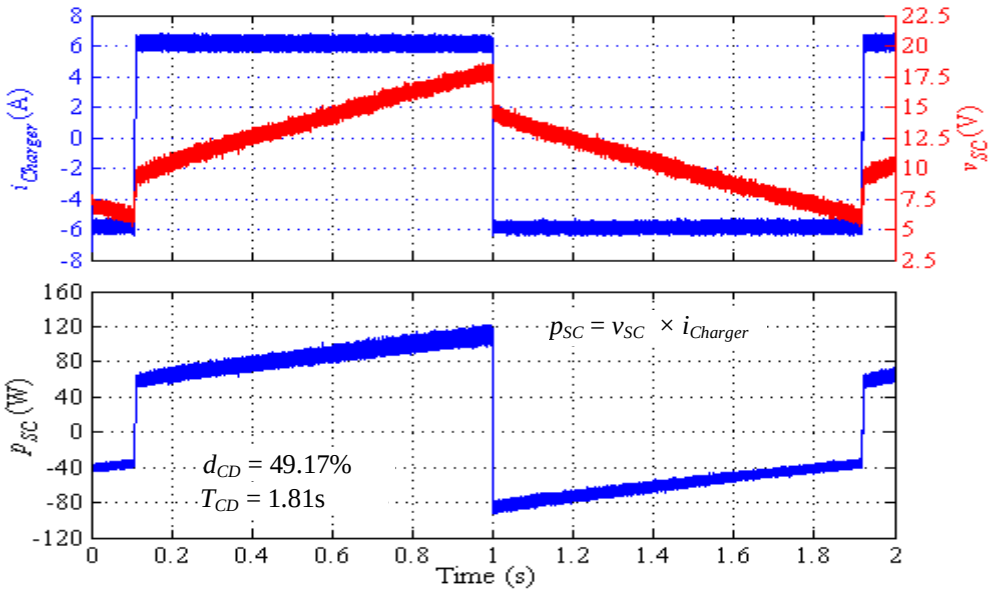


Figure 6.25 6A constant current charge-discharge cyclic test of the real Supercapattery stack

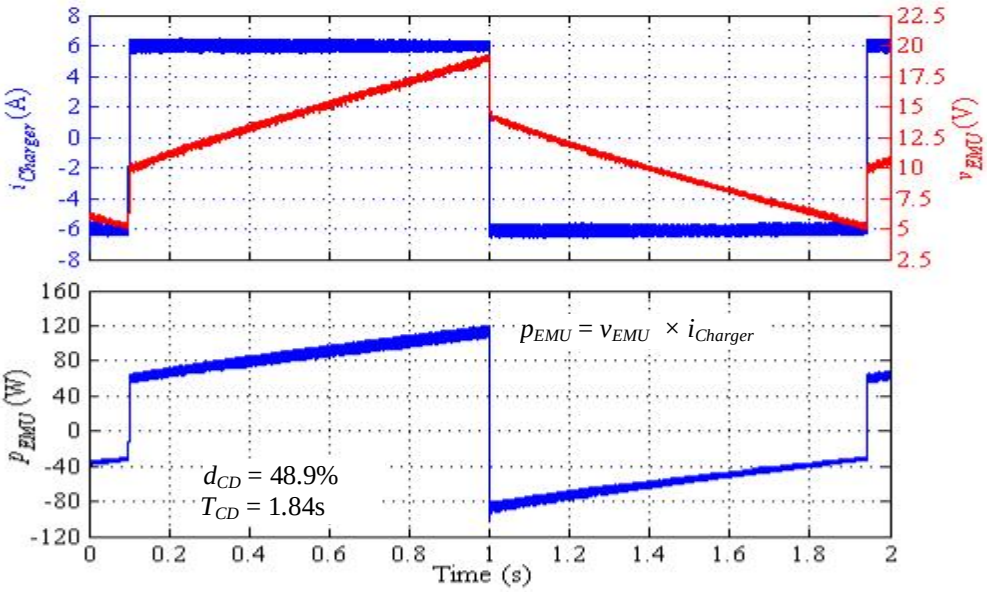
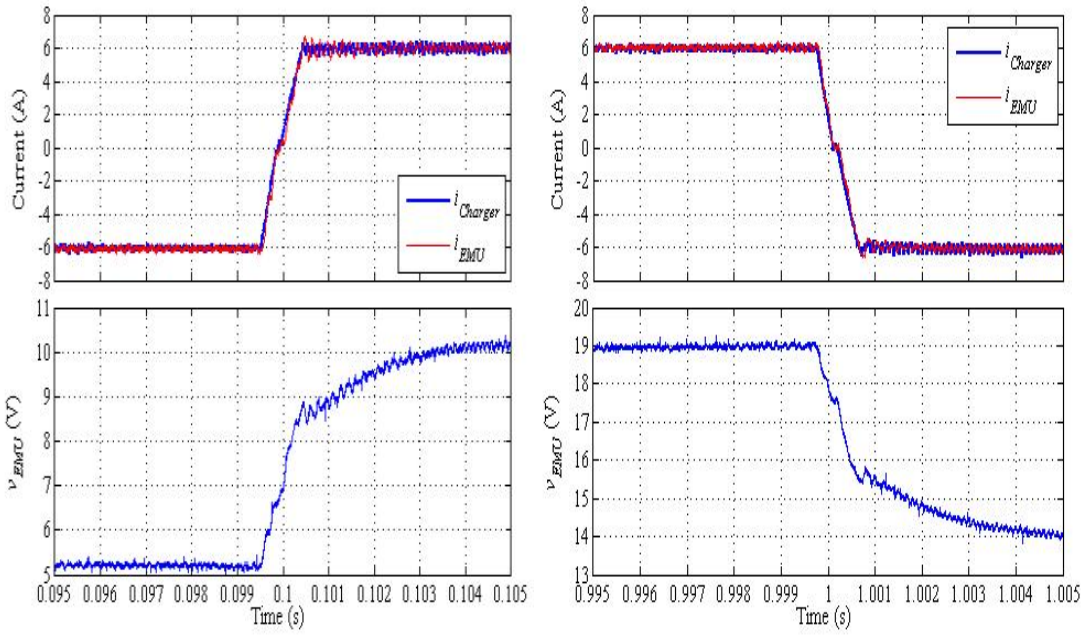


Figure 6.26 6A constant current charge-discharge cyclic test of the Supercapattery emulator



(a) (b)

Figure 6.27 Zoom-in to observe the tracking performance of the emulator under constant current operation: (a) transition from discharging to charging; (b) transition from charging to discharging.

6.7.2.4 Emulator Evaluation under Constant Power Cycling

A constant power cycling test of ±60W is performed with both the real supercapattery and its emulated replica. To control the power constant, the voltage across the real stack and the emulator are measured and are used in calculating $i_{Charger}$* as done in Chapter 4. The minimum and maximum operating voltages in this

case are set to 10 and 19V for both cases. The test results are shown in Figure 6.28 and Figure 6.29. The results show good agreement between the real Supercapattery stack (Figure 6.28) and its emulated replica (Figure 6.29): d_{CD} = 54.36% and T_{CD} = 1.54s for the real stack and d_{CD} = 55.48% and T_{CD} = 1.533s for the emulated one. Again the d_{CD} and T_{CD} differences between the real stack and the emulator may be due to small difference in the applied switching current ripple between Figure 6.28 and Figure 6.29.

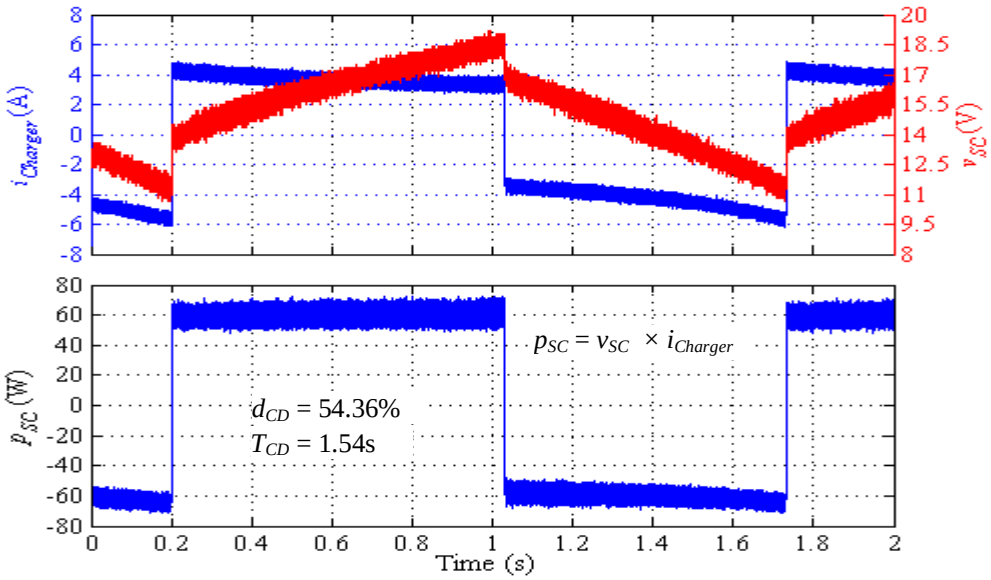


Figure 6.28 60W constant power cycling of the Supercapattery

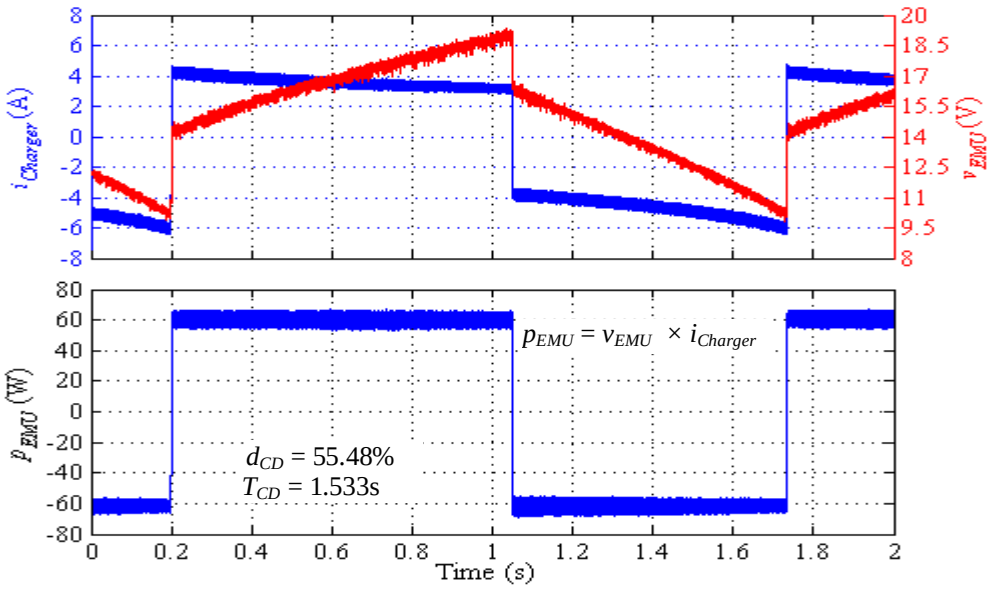


Figure 6.29 60W constant power cycling test of the Supercapattery emulator

6.7.2.5 Constant Power Cycling Emulation of a High Power Device

All the previous tests were conducted with low voltage and currents to be compared with the tests with the real supercapattery device. The emulator is designed to process a much higher voltage, current and power and is evaluated with the scaled-up model as presented in Section 6.5.2. It is assumed that the emulator emulates an energy storage device with similar equivalent circuit parameters as the supercapattery but with much higher voltage (130V) and current (15A) ratings. Since the rated voltage and rated current of the supercapattery are 19V 6A per stack, the model is connected as 7 in series and is expanded to 7 parallel branches, which yields a 133V 42A stack. Since $N_S = N_P$, the model parameters of single stack can be re-used to represent the parameters of this larger stack ($Z_{SP} = Z$). The DC-link voltage of the interleaved inverter was raised to 200V and a minimum discharge voltage of 70V was used.

The result is shown in Figure 6.30, where a constant power cycling test of ±1kW is performed. This illustrates the capability of the emulator to deliver meaningful power levels whilst remaining versatile in behaviour. A 1kW power level is not available from the real supercapattery prototype stack, so an experimental comparison of emulator versus true device cannot be carried out.

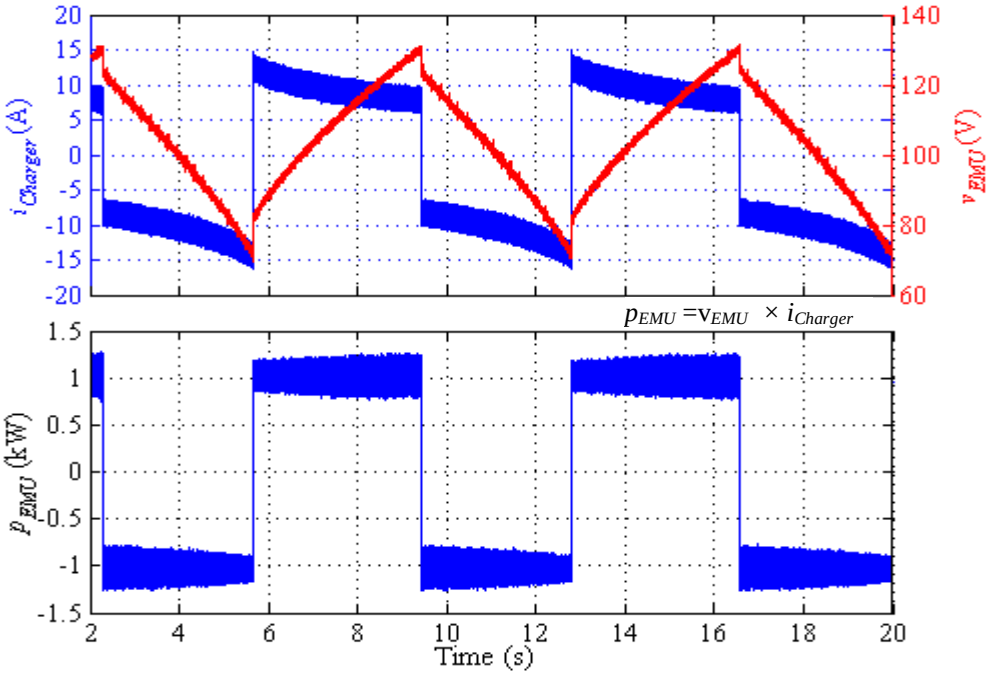


Figure 6.30 1kW constant power cycling test of the emulator

Ideally, the emulator concept has no limitation since it can emulate the SC characteristic as long as the SC model is available and V/I does not exceed the emulator rating. However, the emulator capability in practice is limited by:

- the accuracy and the rated voltage and rated current of the equipment that used to extract the SC model parameters, which is ±20V and ±20A for the Bio-Logic SP-150 with its current booster (Rig III).
- the rated voltage and the rated current of power electronic converter (Part III in Figure 6.1), which is 400V 60A.
- the bandwidth of the voltage controller of the emulator, which is 2kHz.

6.8 Conclusion

This chapter relates to the emulation of supercapattery. Emulation is very useful because it allows testing of equipment designed for large energy storage units which are not available, either because of size, cost, safety and so on. The emulator consists of three parts: the device characteristic model, the controller and the power electronic converter.

For the device characteristic model, the equivalent model and the model parameters extracted by the methods presented in Chapter 4 are used. It is concluded that the device characteristic model and the controller should be implemented in a digital platform since this offers greater flexibility in handling scalable and complex models. For the power converter, there is always a trade-off between speed and accuracy, particularly for emulating high power (both current and voltage) stacks. To overcome this trade-off, an interleaved topology is employed. It is found that increasing the number of interleaved converters reduces ripple. But as the number of interleaved channels is increased, the improvement in ripple attenuation becomes insignificant. Alternatively, the another way of reducing ripple is to use coupled inductors or InterCell transformers and a six-channel bi-directional half-bridge converter with interleaving connection of InterCell transformers has been constructed and evaluated.

A control topology for the emulator and tuning guidelines are presented. It is shown that the proposed equivalent model can be implemented directly on the digital platform. However, there is a risk of oscillation in the controller when implementing a high order model. On the other hand, considering the output voltage of the model as a summation of voltage drops across each series-connected component can minimize the oscillation problem. The model implementation is reduced to simple 1^{st} order components. In addition, the presented equivalent model can be scaled-up easily by combining cells in series, parallel and series-parallel configurations.

The voltage and current controllers of the interleaved converter are evaluated. The results show that the rise time of current and voltage are 50µs and 400µs, respectively, which is acceptable for the emulator application. The emulating performance is evaluated experimentally for a discharge into a resistor, for constant current pulsing and constant power cycling. The results indicate that the performance of the emulator is consistent with the real device. It was found that the emulation of high specific-power type energy storage is very challengeable during a transient period. This is due to nature of high specific power devices (i.e. supercapacitors) that respond faster than low specific power one (i.e. batteries).

Chapter 7 Conclusion and Discussion

7.1 Conclusion

In this PhD thesis, a wide range of technical problems relating to supercapacitors and the supercapatteries are addressed. The main contributions of the thesis can found in:

Chapter 2, the limitations of the single RC model included in the SC characterizing standards are presented. Several SC models are summarized and discussed in conjunction with the characterizing techniques as proposed in the literatures. The model characterizing techniques are grouped into small-signal and large-signal approaches. In this thesis, both the electrochemical impedance spectroscopy (small signal) and the proposed single pulse current (large-signal) techniques were used for modeling the dynamic SC characteristic. The results were used to obtain the parameters of a detailed series-parallel RC model. The models derived from both techniques are compared and the results are consistent with the real device response as presented in Chapter 4.

Chapter 4 deals with another interesting aspect of using SCs in energy storage applications, the round-trip efficiency. In this thesis a constant power cycling method realistic for most energy storage applications is proposed for evaluating SC round-trip efficiency. When the charging power is equal to the discharging power, the proposed method requires only the charge-discharge duty cycle to calculate the efficiency. Additionally, by monitoring online the efficiency changes, any changes within the device characteristic during exploitation due to temperature, parameter changes, etc., can be detected immediately. Furthermore, the methods to estimate energy loss in a single charge-discharge cycle of the SC stack under the CPC control

are also discussed. Three proposed approaches for estimating SC round-trip energy loss are described, which are voltage-based, current-based and current-based with the FFT algorithm. In the energy loss estimation, the latter method uses a frequency dependent and temperature SC resistance value, which changes during the constant power cycling. The errors were reduced to less than 10%.

Chapter 5, a design trade-off analysis for a single-switch fly-back voltage equalizer. Two possible control modes were proposed: a constant switching frequency mode and a constant peak current control mode. The trade-offs between the equalization time, T_{Eq}, the effectiveness of equalization, *STD*, (i.e. maximum voltage deviation) and the total energy loss of both the equalizer and stack, *TEL*, under the two different control modes were presented. Depending on the design objectives, the design trade-off between *STD*, T_{Eq} and *TEL* can be made. If maximizing efficiency is the main concern, the turn-on duration of the voltage equalizer should be as short as possible. However, if the efficiency issue can be compromised and a long operating period is possible, a low cell voltage variation can be achieved with a small amount of energy being dissipated. Lastly, an active-dissipative voltage equalizer with resistive shunts was studied and analyzed as a benchmark comparison with the flyback type. The results of both voltage equalizers showed that the flyback type can minimize cell voltage variation with less amount of energy being dissipated than for the active-dissipative type.

Chapter 6, the supercapattery emulator with the model presented in Chapter 4 was implemented in the digital platform (i.e. FPGA-DSP). The emulator employed an interleaved topology with InterCell transformers to overcome a trade-off between speed and accuracy, particularly for emulating high power (both current and voltage) stacks. By using the emulator, issues relating to cost of implementation, university laboratory safety regulations and inconsistency behavior of the device can be minimized. The voltage and current controllers of the interleaved converter were evaluated. The emulating performance was evaluated experimentally for a discharge into a resistor, for constant current pulsing and for constant power cycling. The results indicated that the performance of the emulator was consistent with the real device. Lastly, hardware-in-loop (HIL) testing was performed in order to verify the control design of a power electronic interface for the newly developed energy

storage device at a power level of 1kW. This power level was higher than the actual laboratory lab device can handle by 10 times. The result confirmed the capability of the emulator to deliver meaningful power levels whilst remaining versatile in behavior.

7.2 Future Work

The main future work that can be developed from the work presented in the thesis relate to the SC characterization, modeling and emulation and the fly-back voltage equalizer.

7.2.1 SC Characterization, Modeling and Emulation

1. In the SC model identification methods presented in Chapter 4, the series-parallel RC model was used. This model is limited to represent SC short-term characteristic only. To enhance this model so that it can also represent SC long-term characteristic (i.e. self-discharging), an equivalent parallel resistance, *EPR*, can be connected either in the positions I or II as presented in Figure 7.1. The reason for these two positions is based on the assumption that the self-discharging characteristic may affect the SC relaxation process (position I) or may not (position II).

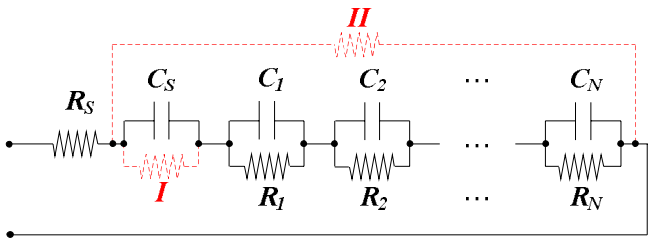


Figure 7.1 New series-parallel RC model with *EPR* at position I or II

2. The SC round-trip efficiency and energy loss evaluation under the constant power cycling method presented in Chapter 2 could be validated experimentally using a calorimeter.
3. From Chapter 2, the SCs have voltage-dependent and temperature-dependent characteristics. Thus, the testing voltage and temperature must be controlled in the characterization processes in order to have a complete SC model that behaves

closely to the actual device. To control the operating temperature precisely, a climate chamber is required. Thus, a full voltage range and full temperature range model could be constructed and used in the emulator, so that the emulator characteristic would be as close to that of the real device. The temperature-dependent, voltage-dependent and frequency-dependent SC impedance can be developed and derived as electrical model parameters and shown in a 3D plane as depicted in Figure 7.2.

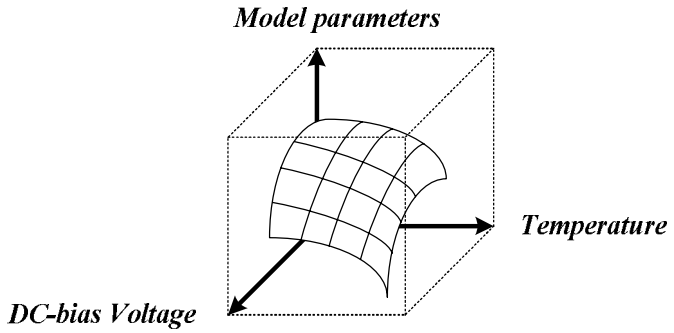


Figure 7.2 Simplistic 3D diagram of model parameters as a function of DC-bias voltage and temperature

4. In Chapter 6, the ADC sampling frequency, f_{samp}, used in the FPGA-DSP control platform is less than the equivalent switching frequency, f_{sw_eq}. Therefore, the control algorithm cannot update the control parameters and minimize the output steady-state error as it can when $f_{samp}=f_{sw\_eq}$. To increase f_{samp}, either the SC model or the converter control algorithm or both can be implemented on the FPGA platform. However, only the converter control algorithm is suggested to be implemented in the FPGA platform, so the fast and flexible model implementation advantage of the system is maintained.
5. The future work of the SC characterization, modeling and emulation development can be summarized as a flow chart presented in Figure 7.3. Three developing phases are presented as: (i) characterization and modeling phase (ii) model validation phase (iii) model implementation phase.

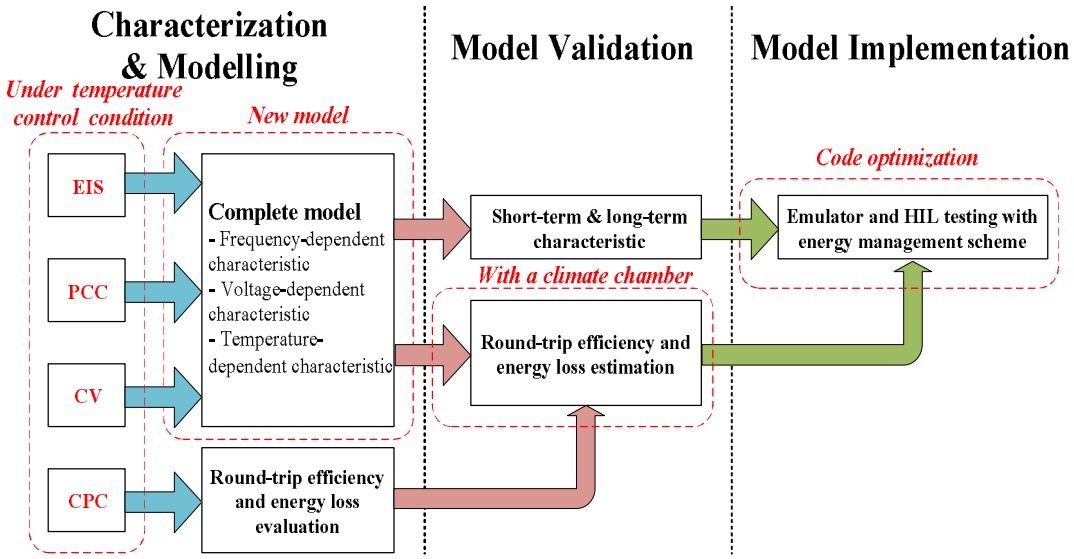


Figure 7.3 The SC characterization, modeling and emulation development chart (EIS = the electrochemical impedance spectroscopy method, PCC = the pulse constant current method, CV = the constant voltage method and CPC = the constant power cycling method)

7.2.2 The Fly-back Voltage Equalizer

The key component in a single-switch fly-back voltage equalizer is a multi-winding transformer. In practice, the unequal leakage inductances of the secondary windings prevent the circulated energy to be share equally among different cells. Therefore, a multi-winding transformer modeling is essential for further study since it can determine the realistic number of cell that can be equalized effectively in term of voltage and energy loss and time.

7.3 List of Publications

The work in this thesis has resulted in a number of publications. These are:

[i] P. Kulsangcharoen, C. Klumpner, M. Rashed, and G. Asher, "A new duty cycle based efficiency estimation method for a supercapacitor stack under constant power operation," in *Power Electronics, Machines and Drives (PEMD 2010), 5th IET International Conference on*, 2010, pp. 1-6

[ii] P. Kulsangcharoen, C. Klumpner, M. Rashed, and G. Asher, "Characterization of energy storage devices for constant power applications," in *IECON 2010 - 36th Annual Conference on IEEE Industrial Electronics Society*, 2010, pp. 1805-1810

[iii] P. Kulsangcharoen, C. Klumpner, X. H. Zhou, C. Peng, G. Z. Chen, M. Rashed, and G. Asher, "Efficiency Evaluation of a Novel Supercapattery Stack with a Power Electronic Interface for Energy Storage Systems," in *Power Conversion Intelligent Motion (PCIM)*, Nuremberg, Germany, 2010.

[iv] P. Kulsangcharoen, C. Klumpner, M. Rashed, and G. Asher, "Evaluation of a flyback regenerative voltage equalisation circuit for series-connected supercapacitor stacks," in *Power Electronics and Applications (EPE 2011), Proceedings of the 2011-14th European Conference on*, 2011, pp. 1-12.

[v] P. Kulsangcharoen, M. Rashed, C. Klumpner, D. De, C. Patel, G. Asher, and G. Z. Chen, "Evaluation of a digitally controlled power electronic emulator for Supercapattery," in *Power Electronics, Machines and Drives (PEMD 2012), 6th IET International Conference on*, 2012, pp. 1-6.

In addition, the author has involved in building the electrochemical testing facility, which has resulted in publications:

- D. De, C. Klumpner, M. Rashed, C. Patel, P. Kulsangcharoen, and G. Asher, "Achieving the desired transformer leakage inductance necessary in DC-DC converters for energy storage applications," in *Power Electronics, Machines and Drives (PEMD 2012), 6th IET International Conference on*, 2012, pp. 1-6.
- D. De, C. Klumpner, C. Patel, P. Kulsangcharoen, M. Rashed, and G. Asher, "Modelling and Control of a Multi-stage Interleaved DC-DC Converter with Coupled Inductors," *Power Electronics, IET Transactions on*, 2013. (accepted)

Appendix A : Standard Characterization Methods

In this section, published SC characterization standards (IEC62391:2006 [22,60] and IEC62576:2010 [61]), testing manuals [62,63], and manufacturing application notes [64-67] are discussed and compared in detail. To determine *ESR* and *C*, a constant current charge-discharge method (CC) presented in [22,60,61,64-67] is used. The CC consists of a charging, a voltage holding, and a discharging period, as depicted in Figure A.1. In each testing step, the following tasks are performed,

- Charging period: the cell is charged with a constant current of I_{ch} until the cell voltage reaches a cell rated voltage, V_{rated}.
- Voltage holding period: the cell voltage is maintained constant either at equal or slightly below V_{rated} for fixed period of time.
- Discharging period: the cell is discharged with a constant current of I_{disch} until the cell voltage reaches minimum or within a safety level.

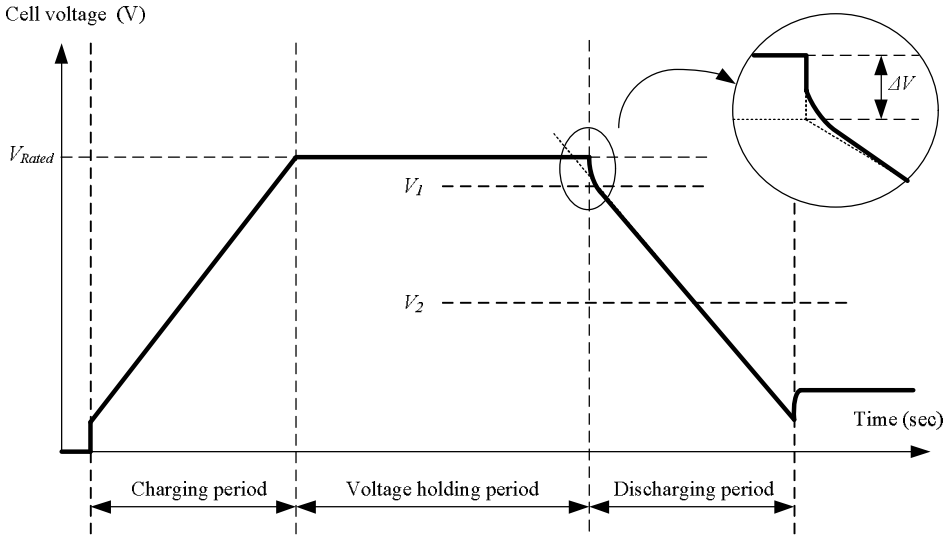


Figure A.1 Voltage-time characteristics of the constant current charge-discharge method used for determining *ESR* and *C* in IEC62391 and some manufacturers application notes

In the SC characterization standards [22,60,61], the term *ESR* has been differentiated into ESR_{AC} and ESR_{DC} which can be determined from the different method. ESR_{AC} is determined from the 'AC resistance method' [22], which is done by applying small AC current value of between 1 to 10mA at 1kHz frequency across the cell and measuring the voltage, so the ESR_{AC} is calculated by (A.1). The further study of ESR_{AC} was done with an electrochemical impedance spectroscopy presented in Section 2.5.1.

$$ESR_{AC} = \frac{V_{RMS}}{I_{RMS}} \tag{A.1}$$

Where V_{RMS} and I_{RMS} are the effective values of AC voltage and current

The detail of parameters setting of each testing procedure is discussed as four periods: (i) pre-conditioning period (ii) charging period (iii) holding period and (iv) discharging period. These differences are described and summarized in Table A.1

1. In the cell pre-conditioning period, there is no specified action stated in IEC62391 standard [22] and some manufacturing application notes since they assume that the testing cell is in a brand new condition. However, in Maxwell® application note, it is recommended to short-circuit for 1 hour prior to the characterization process. This is done to ensure consistency of testing result.

2. During the charging period, different document uses different amount of applied constant charging current. However, the aim is the same for all documents which is to charge the cell to its V_{rated} as quickly as possible but also minimizing the effect of the IR voltage drop before/after removing a constant current. Therefore, the constant charging current is defined by mA/F, and this rate depends on capacity of the test cell.
3. There is a holding period between charging and discharging periods. This gap time is provided for SCs' relaxation phenomena, which is due to their large RC time constant. This duration is between 10 to 60 minutes, and in [22,66,67], a constant voltage source is applied at V_{rated} to ensure that the test SCs are nearly or fully charged (ie. V_{cell} reaches V_{rated}).
4. For discharging period, different amount of discharging current is defined in different document. Similarly to the charging current, the discharging current is selected such that IR voltage drop is not large and it does not exceed pre-defined voltage levels used in the *C* determination. However, the amount of the discharging current is also not too small which causes too small IR voltage drop, and results in difficulty of accurate *ESR* determination. In IEC62391 standard [22], for SC used in power applications (Class3), the discharging current is selected to be 10 times higher for the *ESR* determination than the *C* determination. This discharging current is specified by mA per Farad Volt, so for 2.5V cell 4mA per Farad Volt will be 10mA per Farad, which is also the equivalent to the parameter specified in [66]. However, nowadays the cell voltage is increased beyond 2.5V already (eg. SCs available from NESSCAP® (2.7V), LS Mtron® (2.8V) and Maxwell® (2.7V)), so it is necessary to specify the discharging current with not only per Farad but also per rated voltage of the device under test as shown in IEC62391 standard [22].

From Table A.1, pre-defined voltage levels used in determining *C* is also different for all of the testing standards and manufacturing application notes. As will be shown later that *C* has nonlinear voltage-dependent characteristic, the selected voltage levels will affect the determination value of *C* directly as stated in Table A.1. The best practice is to calculate *C* from the voltage range that the SCs are used in particular application. Since in most application, the SC is operated between at V_{rated} and at a half of V_{rated} so that 75% of energy is utilized. Therefore, it is recommended

to choose V_1 and V_2 between voltage range of V_{rated} and at a half of V_{rated} as done in Maxwell manufacturer's datasheet [65]. Please note that the constant charge-discharge in Maxwell application note is slightly different from the testing pattern presented in Figure A.1, and it is called "six-step" process as presented in Figure A.2. The main difference from the previous testing pattern is there are two testing cycles where only the information of the 2nd cycle is used in the parameter determination.

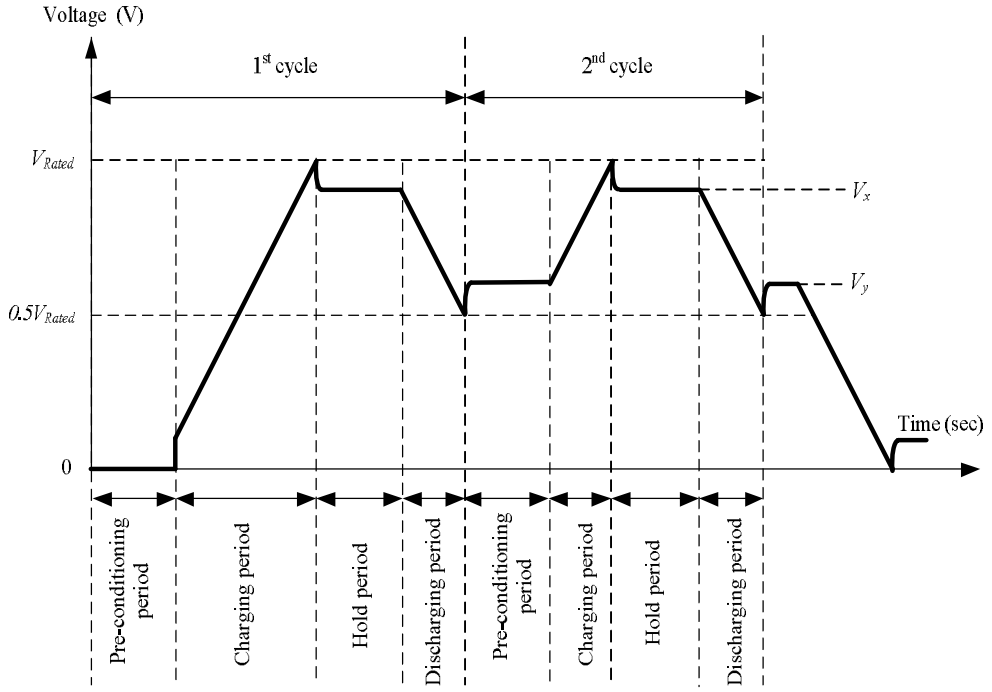


Figure A.2 Voltage-time characteristics of the constant current charge-discharge method used for determining *ESR* and *C* in Maxwell® application note so called "six-step" process

Table A.1 Comparison of process to determine capacitance, *C* and an equivalent series resistor, *ESR*

	Standards		Manufacturing application notes			
	IEC62391		LS Mtron®	NESSCAP®		Maxwell®
For determine	*C*	*ESR*	*C* and *ESR*	*C*	*ESR*	*C* and *ESR*
During pre-conditioning period	Not specified		Not specified	Not specified		For 1st cycle: Short-circuit cell for 1hr under temperature 23°±2°C For 2nd cycle: Open-circuit cell for 15s
During charging period (Applying I_{ch})	I_{rated} of device until V_{cell} reaches V_{rated}		10mA/F until V_{cell} reaches V_{rated}	I_{rated} of device until V_{cell} reaches V_{rated}		75mA/F until V_{cell} reaches V_{rated}
During hold period (Applying $V_{const} = V_{rated}$)	30mins		10mins	30mins	>60mins	Open-circuit cell for 15s
During discharging period (Applying I_{disch})	$4C_{rated}V_{rated}$ mA* until V_{cell} becomes insignificant	$40C_{rated}V_{rated}$ mA* until V_{cell} becomes insignificant	10 mA/F until V_{cell} reaches 0.1V	1mA/F until V_{cell} becomes insignificant		75mA/F until V_{cell} reaches 0.1V
V_1 and V_2 used in *C* calculation of Figure A.1	$V_1 = 0.8V_{rated}$ and $V_2 = 0.4V_{rated}$		Not specified	$V_1 = 0.7V_{rated}$ and $V_2 = 0.3V_{rated}$		$V_1 = V_x$ (see Figure A.2) and $V_2 = 0.5V_{rated}$
ΔV used in *ESR* calculation of Figure A.1	The difference between V_{rated} and an intersection of a back-projection line of slope of $(V_1-V_2)/(t_1-t_2)$.		IR drop during 10ms period after discharging	IR drop after discharging		The difference between $0.5V_{rated}$ and V_y (see Figure A.2)
Testing pattern	Figure A.1					Figure A.2

*Rated for Class 3 device defined in [22] which is used for power applications

Another SCs testing standard and manuals are IEC62576 [61], EUCAR [62] and FreedomCAR [63], which are written specially for hybrid electric vehicle (HEV) applications. The main differences of these standards from the previous standards are summarized as below,

- In the pre-conditioning period, the environmental testing temperature is concerned, so the temperature control equipment (ie. climate chambers) is warm-up with a given time period before performing the test. The testing cell is also strictly required to be short-circuit for a given time period, for example, more than 2hours for IEC62576 [61], and 12hours for EUCAR [62].
- During charging and discharging periods, the applied charging and discharging currents are limited under 95% efficiency condition [61]. The loss due to charging is minimized so the device temperature is not changed much from testing temperature. The formula used to calculate this current is also presented in [61].
- In the holding period, a short resting time is proposed since in HEV applications, the charge-discharge cycle period is very short as energy has to be transferred in-out instantaneously during accelerating and braking, for example, 5mins for IEC62576 [61].
- In FreedomCAR [63], the energy stored is a parameter of interest, so there is no procedure to determine the capacitance. The effective capacitance is used and can be derived from the discharging energy.

The presented testing standards are used for characterizing SCs and determining their simple RC equivalent model of SCs. Each standard procedure is designed in accordance with the way the SCs are used, so many testing parameters such as operating voltage range, working temperature, charge-discharge periods and so on, are defined differently. Therefore, the testing standards can be used only as a guideline on studying characteristic of SCs since there are many limitation of RC model.

Appendix B : Extra Experimental Results

The characterization results of each device are grouped and presented in separated sections. These devices are:

- The supercapattery stack I (re-do testing) (Section B.1)
- The supercapattery stack II (Section B.2)
- The Maxwell® BMOD0052 SC stack (Section B.3)
- The ELIT® SC stack (Section B.4)

For the supercapattery stack I and II, the results and the derived-models from the electrochemical impedance spectroscopy (EIS) and the pulse constant current (PCC) are presented. In addition, the constant power cycling (CPC) results of both devices are included. For the Maxwell BMOD0052 and the ELIT® SC, only the EIS results are presented.

B.1 The Supercapattery Stack I (Re-do Testing)

B.1.1 SC Characterization Results Using the Electrochemical Impedance Spectroscopy (EIS) Method and Model Parameters

The EIS method with the frequency sweep from 10mHz to 1kHz is applied on the supercapattery nineteen-cell stack with DC-bias voltages of 0V and 10V. The impedance result at zero-bias voltage is included for comparison. The experimental results based on the simple RC model are presented in Figure B.1 and Figure B.2.

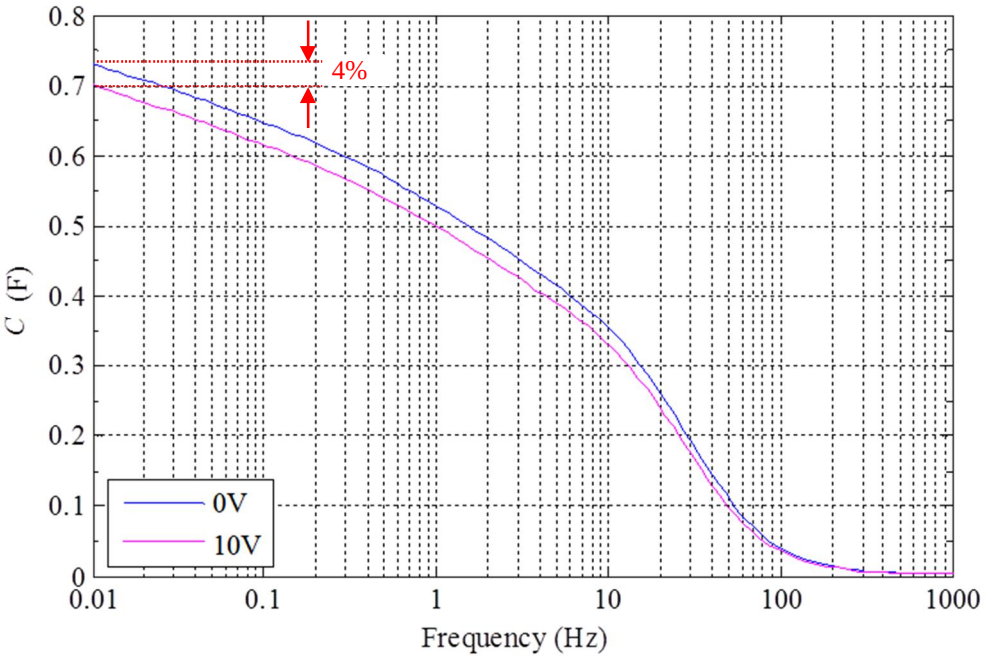


Figure B.1 Equivalent capacitance versus frequency range 10mHz to 1kHz of the nineteen-cell supercapattery stack at the applied voltages of 0V and 10V

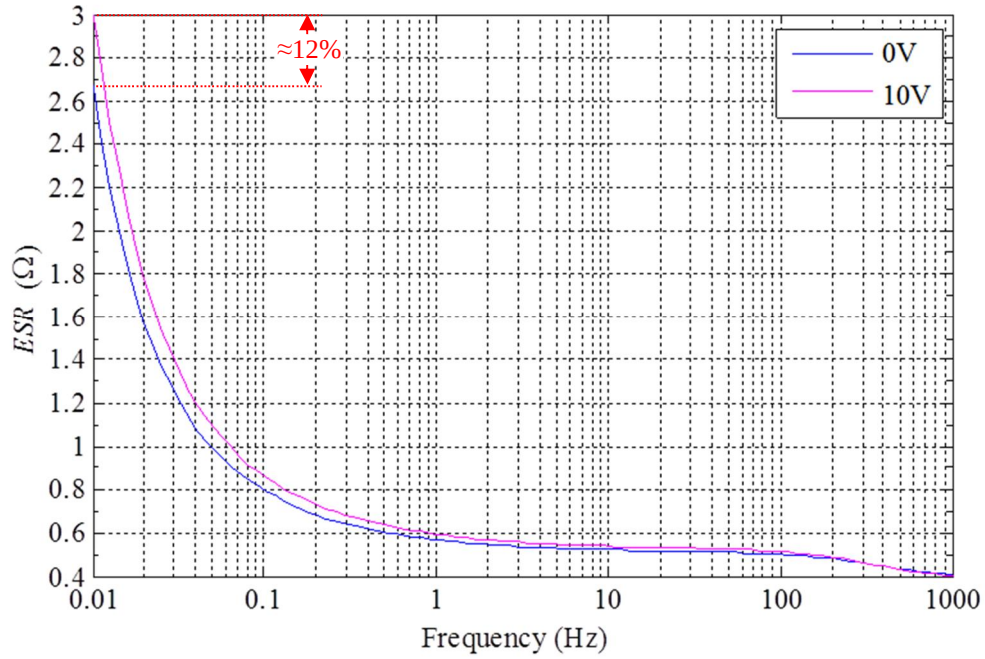


Figure B.2 Equivalent series resistor versus frequency range 10mHz to 1kHz of the supercapattery nineteen-cell stack at zero-bias and the applied voltage of 10V

From Figure B.1 and Figure B.2, due to the 10V bias effect, the equivalent series resistor, *ESR*, at 10mHz is increased by 12% and the capacitance, *C*, is reduced by 4% from that of zero-bias condition. The effect of DC-bias voltage on the *ESR* is smaller when the frequency increases toward 1kHz. These *ESR* and *C* values indicate

the device is already degraded since in Section 4.2.1.2, the *ESR* at 10mHz is 2.15Ω (28% lower) and the *C* is 0.76 (7.8% higher).

The identification process is applied to the experimental results obtained at 10V DC-bias voltage that presented in Figure B.1 and Figure B.2 to derive model parameters based on model IV_2 (Figure B.3). The 10V-bias result is chosen since it will be used for further evaluation and in comparison with the PCC result. The impedance results are shown in Figure B.4 and Figure B.5. The derived model parameters are presented in Table B.1.

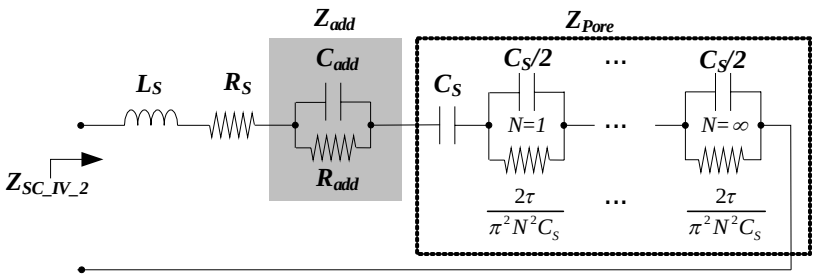


Figure B.3 Model IV_2: The *N* series-parallel RC model with an additional RC branch

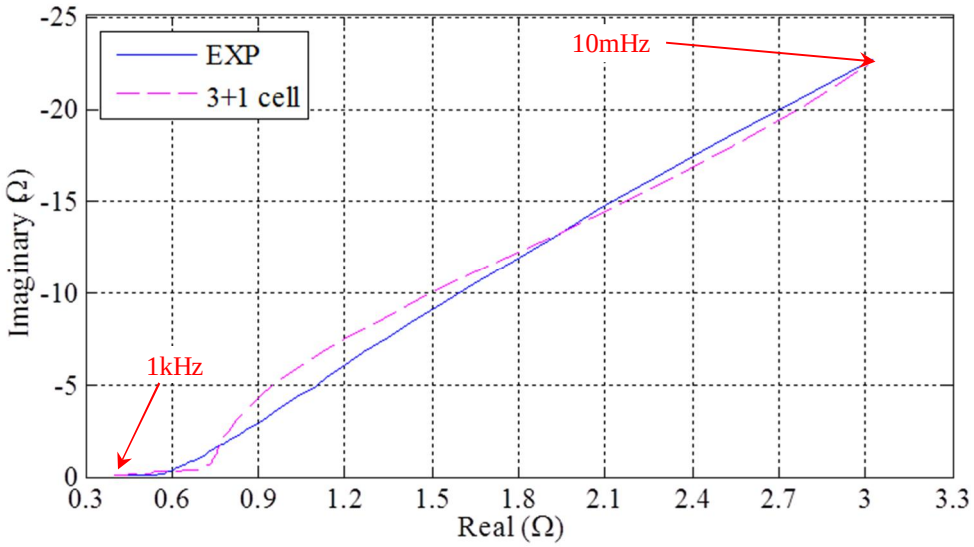


Figure B.4 Real and imaginary impedance terms versus frequency of the 10V-bias measured and model IV_2 (3+1 cells) of the supercapattery stack I

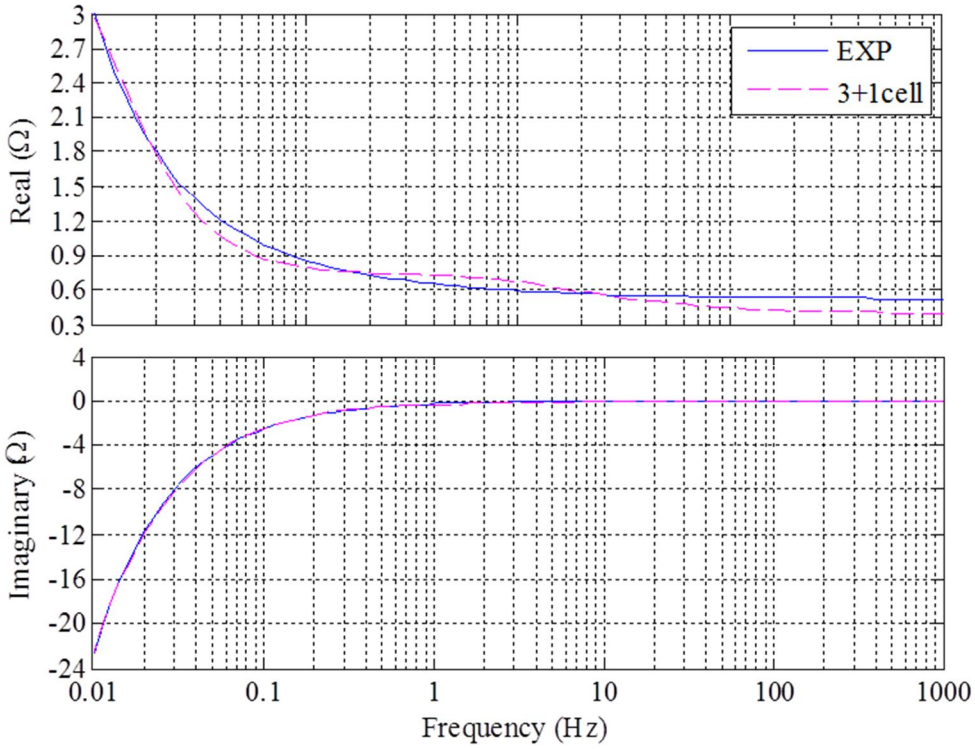


Figure B.5 Imaginary versus real impedance terms of the 10V-bias measured and model IV_2 (3+1 cells) of the supercapattery stack I

Table B.1 The model IV_2 parameters derived from the EIS experimental result of the supercapattery stack I at 10V-bias voltage

N	R_{add} (Ω)	C_{add} (F)	R_S (Ω)	L_S (nH)	C_S (F)	τ	Real *RMSE* (10^{-3})	Imaginary *RMSE* (10^{-3})	Real R^2 (max=1)	Imaginary R^2 (max=1)
3+1	3.80	3.45	0.4078	20	0.7756	0.941	80.5	78.7	0.9747	0.9997

From Figure B.4, it is seen clearly that the model fits the experimental result. The results are re-plotted as imaginary and real terms versus frequency in Figure B.5. The imaginary impedance term derived from the model fit correctly to the experimental imaginary impedance for all frequency range. However, the real impedance term derived from the model is fairly fit the experimental real impedance. The goodness of fitting is justified by *RMSE* and R^2 parameters presented in Section 4.2.2 and they are included in Table B.1. In addition, from Table B.1, the R_{add} and C_{add} are chosen by trial and error to minimize the real and the imaginary *RMSE*s.

B.1.2 SC Characterization Results using the Pulse Constant Current (PCC) Method and Its Model Identification Algorithm

The PCC is re-applied again on the supercapattery stack I with the discharged PCC, i_{SC}, at I_P = -5.8A for the period, T_P = 327.6ms. The SC voltage response, v_{SC}, is recorded as presented in Figure B.6. The initial SC stack voltage before applying the PCC, V_i, is 11.654V and the final SC stack voltage after removing the PCC, V_f, is 8.87V. Thus, the average voltage, V_{avrg}, is 10.262V.

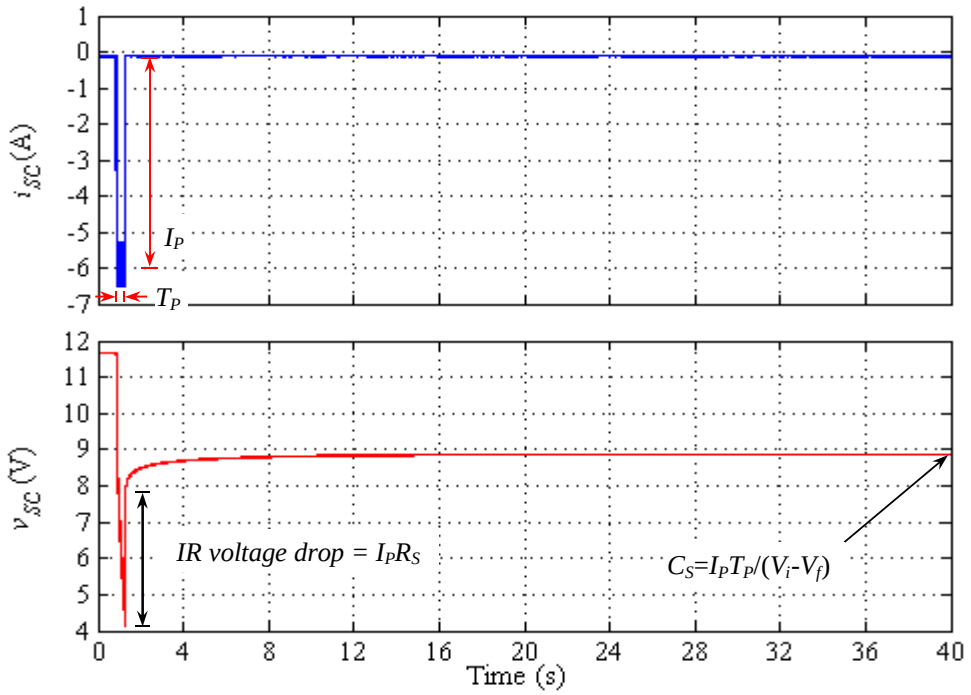


Figure B.6 Experimental result of the discharged PCC on the supercapattery stack I (I_P = –5.8A, T_P = 327.6ms, V_i = 11.654and V_f = 8.87V)

This time the v_{SC} is low noise and non-filtered. The fitting process is performed as same as before on the relaxation period, and the fitted coefficients and the model parameters are presented in Table B.2 and Table B.3.

Table B.2 The fitted coefficients and the error from the MATLAB® Curve Fitting Toolbox™ at various N

N	X_1	Y_1	X_2	Y_2	X_3	Y_3	X_4	Y_4	const	RMSE (10^{-3})	R^2 (max=1)
1	0.6074	0.461							8.859	32.51	0.9152
2	0.4068	0.274	0.7031	5.158					8.869	14.32	0.9832
3	0.3057	0.204	0.4505	1.690	0.9282	40.010			8.875	5.20	0.9978
4	0.2606	0.179	0.3422	1.031	0.3259	6.464	0.8587	64.440	8.877	3.75	0.9989

Table B.3 The RC parameters extracted from Table B.2 based on model IV_3 (expressed in Ω and F)

N	R_1	C_1	R_2	C_2	R_3	C_3	R_4	C_4	R_S	C_S
1	0.7470	2.9034							0.4655	0.6798
2	0.8175	4.4674	0.1487	1.3041					0.4655	0.6823
3	0.8142	6.0121	0.1827	3.2388	0.1600	0.1562			0.4655	0.6837
4	0.7898	7.0817	0.2058	4.7121	0.0639	2.4220	0.1481	0.1048	0.4655	0.6842

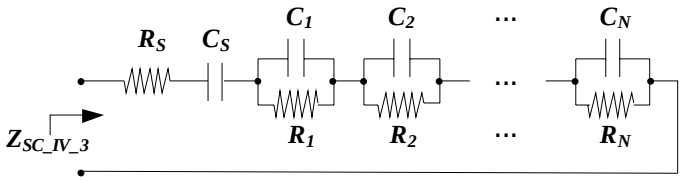


Figure B.7 Model IV_3: The N series-parallel RC model without L_S

From Figure B.7 and Table B.3, for the model order N = 4, the R_S has increased by 18.5% (from 0.3793Ω) and the C_S has reduced by 18.1% (from 0.8356F) comparing with the result presented in Section 4.2.3. The PCC results confirm the degradation of the supercapattery with the EIS result.

Model IV_2 with the parameters of Figure B.7 shown in Table B.3 is simulated. The comparison between the model and the experimental results both after the pulse period and during the pulse period are shown Figure B.8 and Figure B.9, respectively. For an order of N = 4, the fitting is very good in both the period after the PCC and during the pulse period. Therefore, the model N=4 is selected for further evaluation.

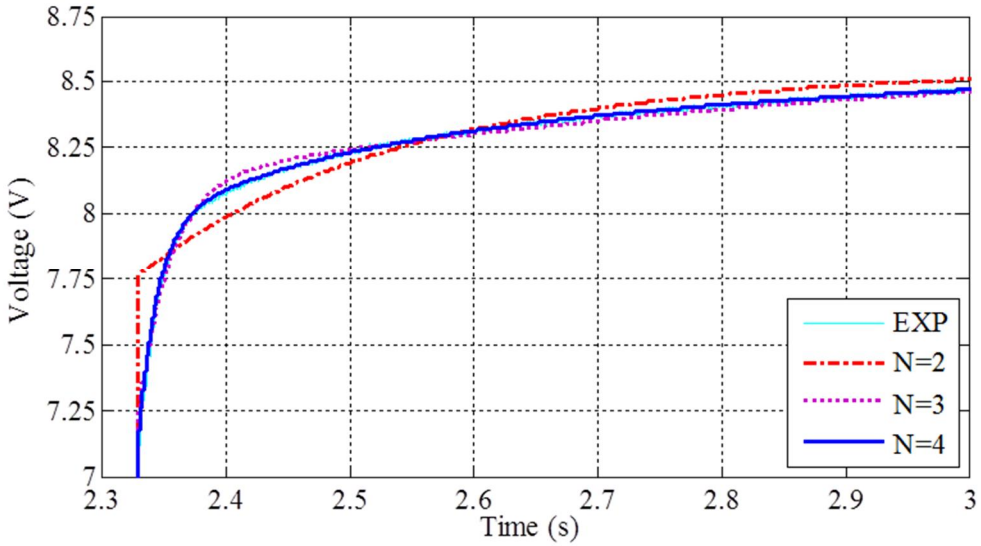


Figure B.8 The comparison of the voltage response after removing the PCC between the experimental result and the simulations with different model order N used

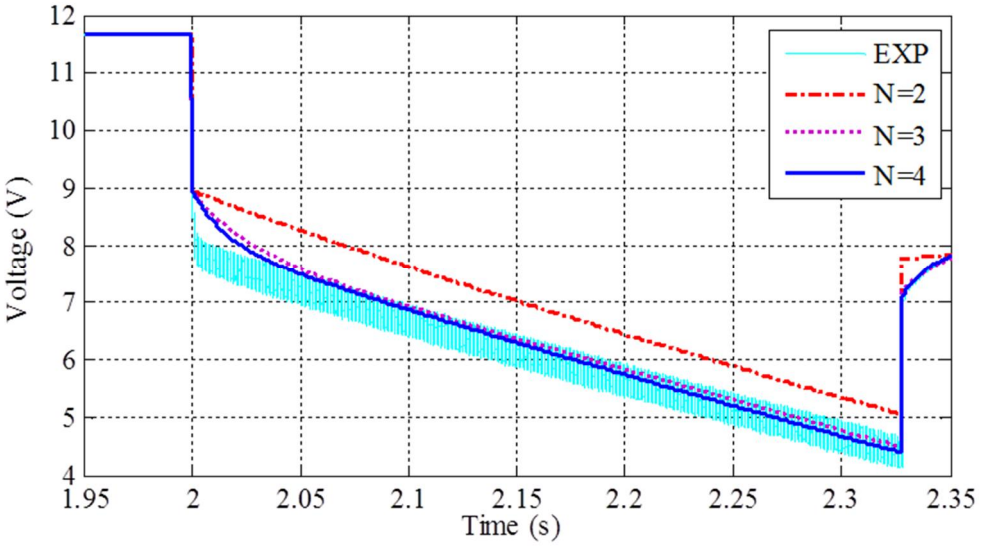


Figure B.9 The comparison of the voltage response during applying the PCC between the experimental result and the simulations with different model order *N* used

B.1.3 Evaluation of the Electrochemical-Impedance-Spectroscopy-based and the Pulse-Constant-Current-based models

Firstly, the frequency response of the PCC-based model presented of Figure B.7 is simulated, and the result (PCC) is compared with the experimental results (EIS-EXP) and with the EIS-based model (EIS) presented in Figure B.4. The comparison is shown in Figure B.10 and Figure B.11. Note that all results are either obtained or derived from nearly the same DC bias-voltage of 10V.

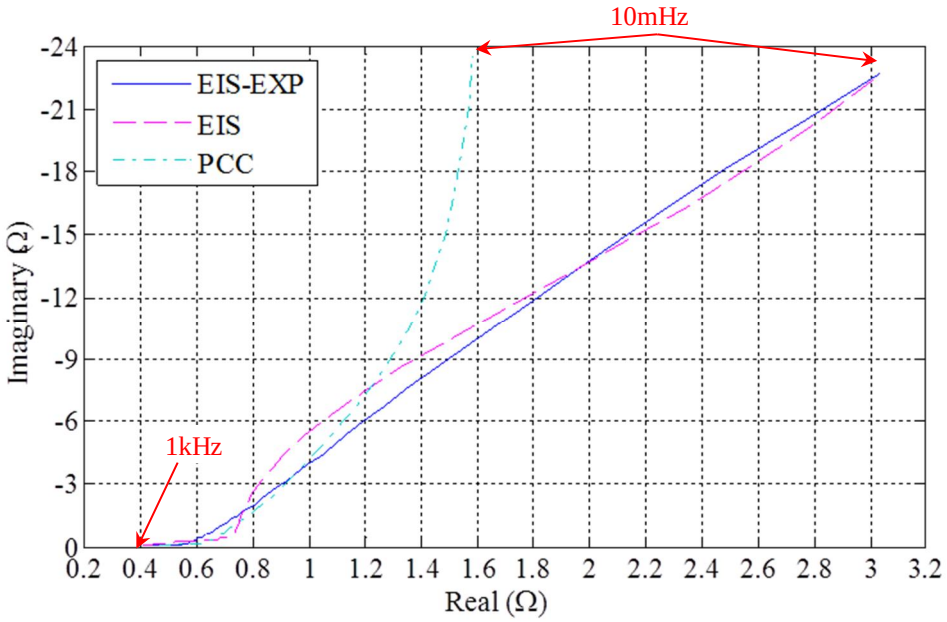


Figure B.10 Imaginary versus real impedance terms of the 10V-bias EIS experimental result, the EIS-derived and the PCC-derived results of the supercapattery stack I

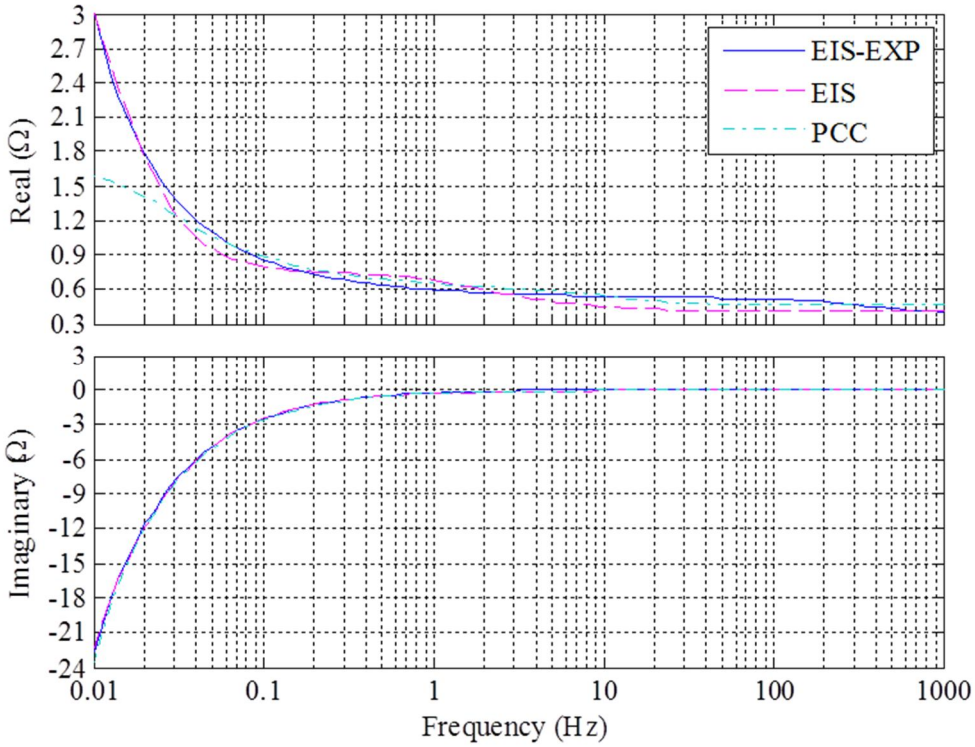


Figure B.11 Real and imaginary impedance terms versus frequency of the 10V-bias EIS experimental result, the EIS-derived and the PCC-derived results of the supercapattery stack I

The imaginary impedance part of the PCC fits the EIS-EXP very well. However, in the real impedance part, the PCC does not fit the EIS-EXP at the frequency <50mHz. Since the PCC is derived from the pulse period of 40s (≈25mHz), the response of the PCC model cannot fit the EIS-EXP at this low frequency range. In addition, from Figure B.11, it can be seen that the PCC real term at 1kHz is more than the EIS by 60mΩ. This difference is due to mismatch between the R_S component of the PCC and the EIS. This extra resistance derives probably from the lead cable and the plug connection that are used in the PCC measurement. To justify the goodness of fitting, the errors between the PCC and the EIS-EXP, and between the EIS and the EIS-EXP, are calculated and presented in Table B.4. The high discrepancy between the PCC and the EIS-EXP is confirmed with the higher real *RMSE* and the lower real R^2 than the EIS.

Table B.4 Error between the EIS and the PCC models and the EIS experimental result

Model from	Real *RMSE* (10^{-3})	Imaginary *RMSE* (10^{-3})	Real R^2 (max=1)	Imaginary R^2 (max=1)
EIS	80.521	78.71	0.9747	0.9997
PCC	246.133	147.64	0.7635	0.9989

Next, the EIS-based model is evaluated with the PCC simulation, and the result is compared with the PCC-based model and the PCC experimental result (denoted as PCC-EXP) as shown in Figure B.12 and Figure B.13.

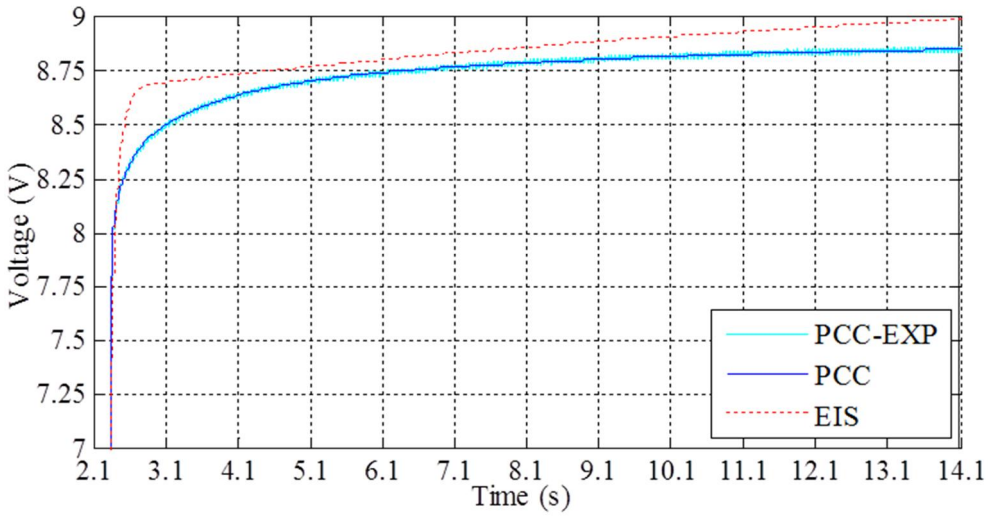


Figure B.12 The comparison of the voltage response after removing the PCC between the EIS-based model, the PCC-based model and the PCC experimental result

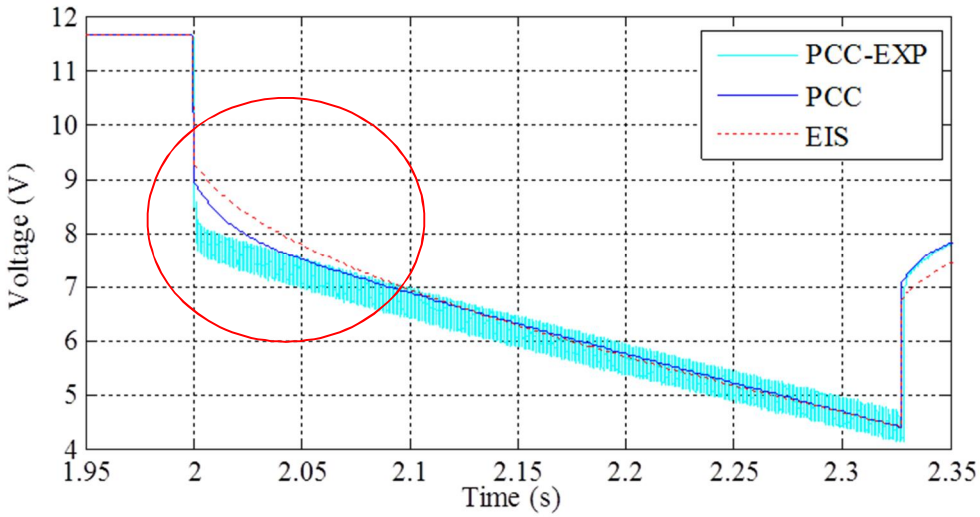


Figure B.13 The comparison of the voltage response during applying the PCC method between the EIS-based model, the PCC-based model and the PCC experimental result

From Figure B.12, considering the voltage response after removing the PCC (i.e. the relaxation period), the EIS has the final steady-state voltage and error higher than the PCC and the PCC-EXP. This discrepancy is explained by the difference in the C_S value used in each model. The EIS and the PCC C_S parameters are 0.7756F and 0.6842F, which cause the PCC bouncing voltage after discharge to become lower than that of the EIS.

Figure B.13 shows the voltage responses during the PCC period. The PCC voltage response fits the PCC-EXP better than the EIS even though their R_S parameters are slightly different (i.e. 60mΩ) as indicated in the frequency response testing. Thus, it can be concluded that a small mismatch in the model parameters between the EIS and the PCC as indicated in the frequency response testing can yield large discrepancies in the voltage response for the large signal test. In addition to Figure B.13, in the red circle, a step voltage error between the experimental result and the models are shown. Since the *ESR* at higher DC bias voltage is higher than at that of the lower DC bias voltage, the main *ESR* used in the both models determined from single DC bias voltage condition cannot account for this. Even though the *ESR* of pulse model obtained from pulse experimental result should fit perfectly but the model can only fit one value of main *ESR* since the model assumed that the main *ESR* does not changed with the DC bias voltage.

B.1.4 The Round-trip Efficiency Evaluation

In this section, the supercapattery stack I round-trip efficiency, η_{RT}, is tested with the constant power cycling method (CPC) at the constant power, P, of 40, 50 and 60W with the operating voltage range, V_{SC_min}-V_{SC_max}, of 8-19V, 10-19V and 12-19V. The testing is started from low to high power levels. The choice of testing conditions (i.e. P, V_{SC_min} and V_{SC_max}) is limited by the device rated current of 5A and the rated voltage of 19V. Thus, to test at higher power, the minimum voltage is increased in order not to exceed the maximum current of 5A that can be handled by the SC. Some experimental results of the CPC testing on the supercapattery stack I are presented in Figure B.14 (40W & 8-19V), Figure B.15 (50W & 10-19V) and Figure B.16 (60W & 12-19V). More results are included in Table B.5, which shows the test results in at the maximum current of 4A and 6A but the same votlage range and power level are maintained for comparison. The stack temperature is observed by using a thermal camera at the start and at the end of test as presented in Figure B.17 and Figure B.18. The center point stack temperature is changed by ≈2°C only. It is possible that slightly higher temperatures may develop inside the stack, but due to its flat and thin shape and quite thick metal end plates that provides good cooling, helps the heat to spread out well and prevents dangerous overheating.

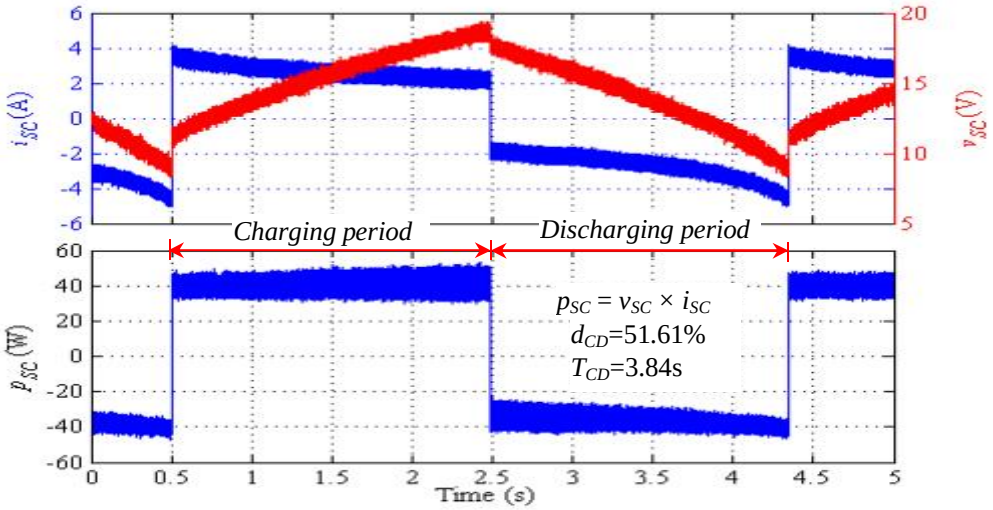


Figure B.14 Voltage, current and power waveform of the SC stack during the charge-discharge tests at P = 40W, V_{SC_min} = 8V and V_{SC_max} = 19V

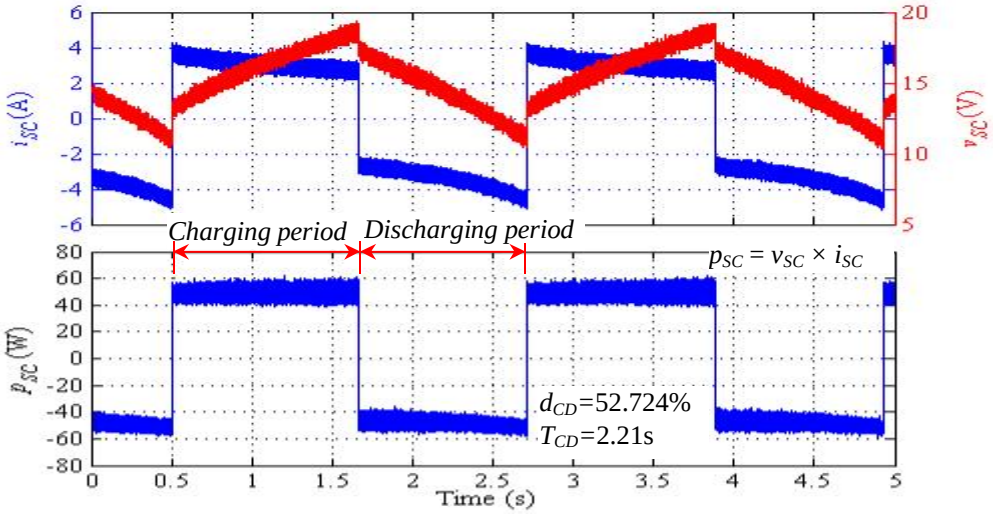


Figure B.15 Voltage, current and power waveform of the SC stack during the charge-discharge tests at P = 50W, V_{SC_min} = 10V and V_{SC_max} = 19V

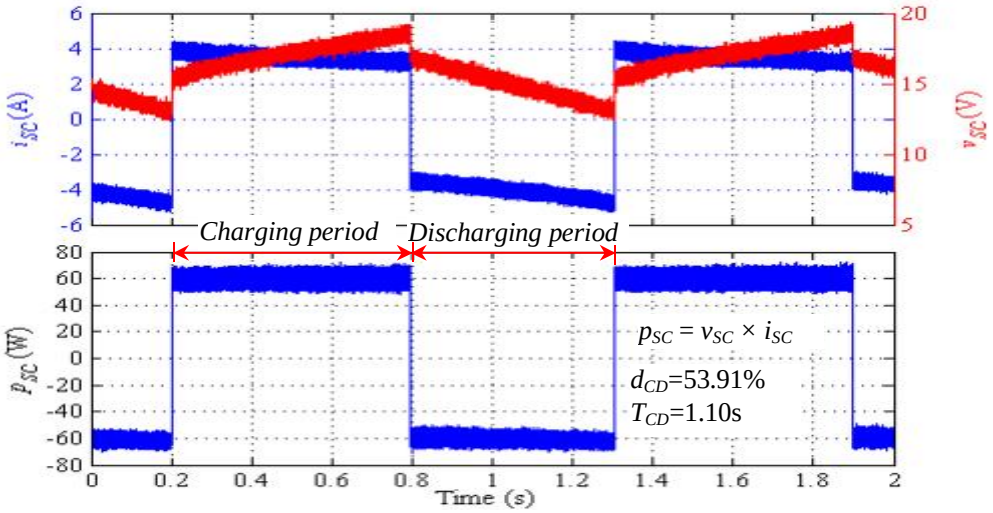


Figure B.16 Voltage, current and power waveform of the SC stack during the charge-discharge tests at P = 60W, V_{SC_min} = 12V and V_{SC_max} = 19V

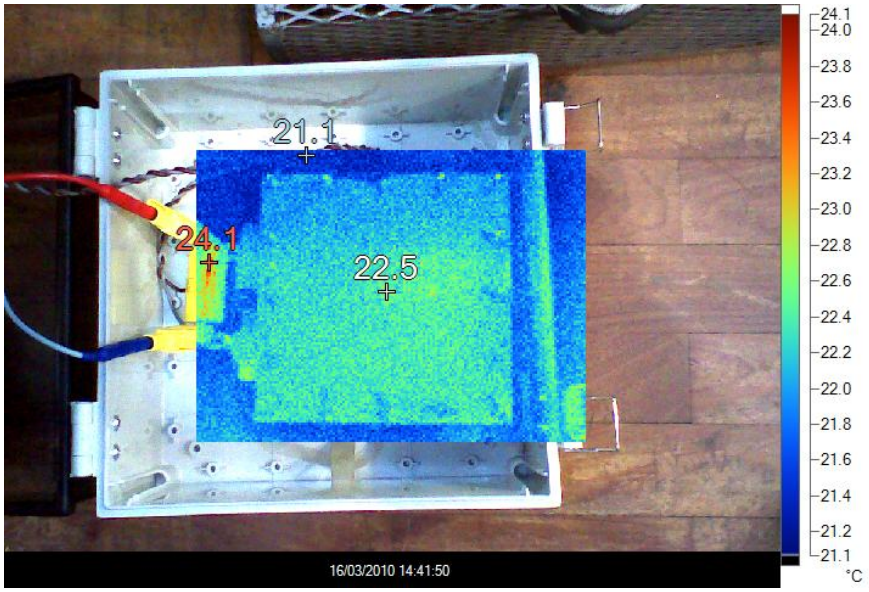


Figure B.17 The supercapattery stack I temperature at the start of the CPC testing

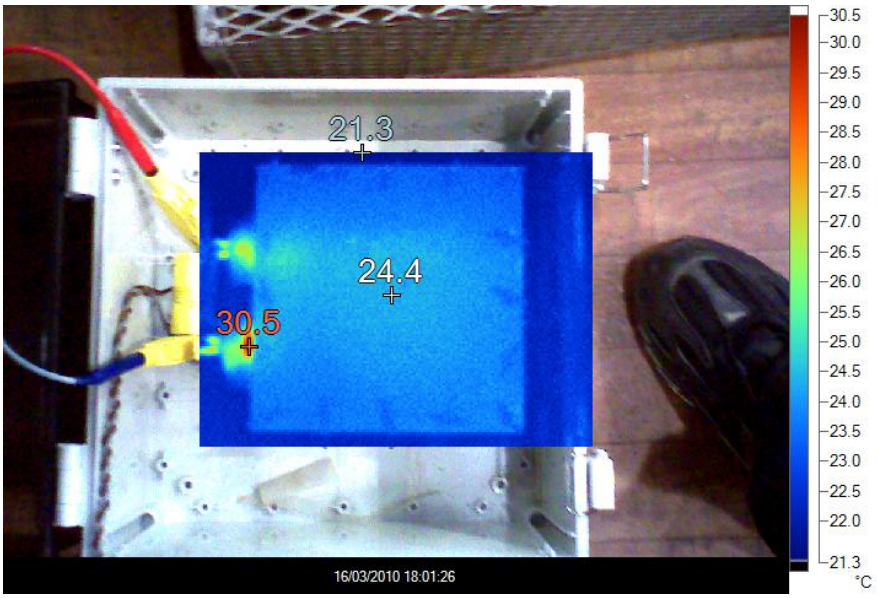


Figure B.18 The supercapattery stack I temperature at the end of the CPC testing

By using (B.2) and (B.3), a round-trip efficiency and energy loss per charge-discharge cycle, η_{RT_EXP} and $E_{Loss\_RT\_EXP}$, are calculated for each operating point. The results are included in Table B.5.

$$\eta_{RT\_EXP} = \frac{-\int_0^{T_D} p_{SC}\,dt}{\int_0^{T_C} p_{SC}\,dt} = \frac{-E_D}{E_C} \tag{B.2}$$

$$E_{Loss\_RT\_EXP} = E_C + E_D \tag{B.3}$$

Table B.5 The experimental results of the supercapattery stack I under the CPC method

V_{range} (V)	V_{cmin} (V)	V_{cmax} (V)	T_{CD} (s)	f_{CD} (mHz)	P_{C_avrg} (W)	P_{D_avrg} (W)	P_{avrg} (W)	η_{Exp} (%)	$E_{Loss\_RT\_EXP}$ (J)
8-19	10.1	18.3	3.84	260.2	40.68	36.23	38.45	83.46	13.35
	10.4	18.1	3.18	314.4	45.29	41.83	43.56	83.40	12.6
10-19	11.7	18.2	3.26	306.6	40.48	35.90	38.19	85.59	9.55
	12	18.2	2.68	373	45.19	41.74	43.47	85.99	8.8
	12.2	18	2.24	446	49.20	47.77	48.49	86.93	7.61
	12.7	17.7	1.57	639	59.43	56.16	57.80	83.29	8.52
12-19	13.4	18.3	2.45	408.9	40.61	37.05	38.83	89.46	5.28
	13.6	18.1	1.99	503	45.07	42.95	44.01	90.10	4.56
	13.7	18	1.63	613.1	49.96	48.64	49.30	88.88	4.83
	14.2	17.8	1.1	905.5	59.81	60.38	60.09	86.33	4.86

From Table B.5, for the same operating voltage range, the efficiency decreases when the power increases as shown in Figure B.19. This efficiency-power relationship is explained by the increase of the current in the circuit in the CPC test. In addition, at low voltage (8-19V range), only two operating points at lower power levels of 40W and 45W have been tested, which means that the losses are referred to a low processing power, resulting a lower efficiency. This may also be a potential explanation why the efficiency seems to increase with the power level up to a point, after which it starts to drop (probably due to the losses increasing exponentially with square the current, outpacing the increase of processing power).

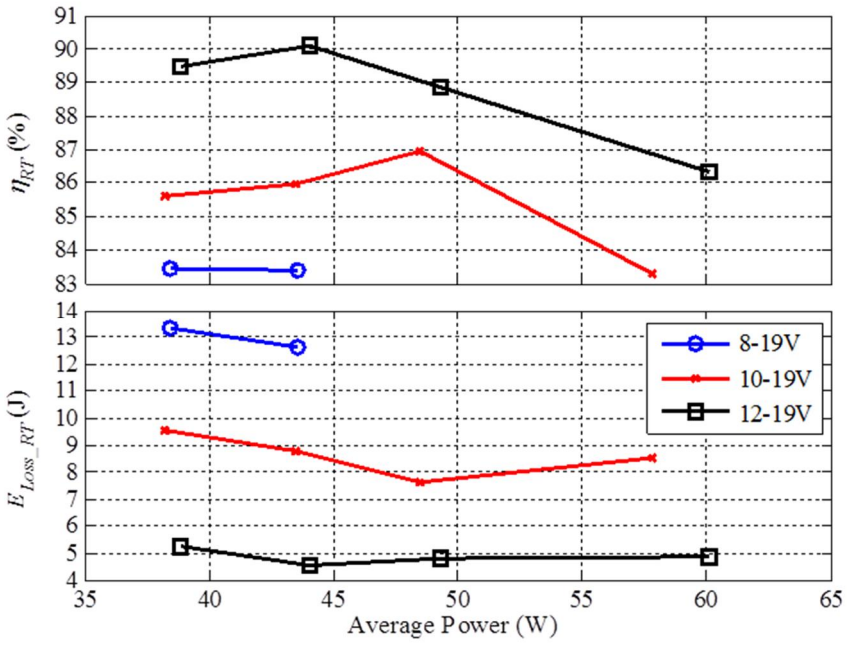


Figure B.19 Efficiency versus average power for different voltage ranges

In addition to Figure B.19, as the average processing power increases, the energy loss is slightly reduce. This small energy loss reduction effect is due to the charge-discharge period changes slightly as well as the corresponding *ESR* (see Figure B.2).

B.2 The supercapattery stack II

B.2.1 SC Characterization Results Using the Electrochemical Impedance Spectroscopy (EIS) Method and Model Parameters

The EIS method is applied to the three-cell supercapattery stack with the frequency sweep from 10mHz to 1kHz at zero-bias and 3V DC-bias voltage conditions. The experimental results based on the simple RC model are presented in Figure B.20 and Figure B.21.

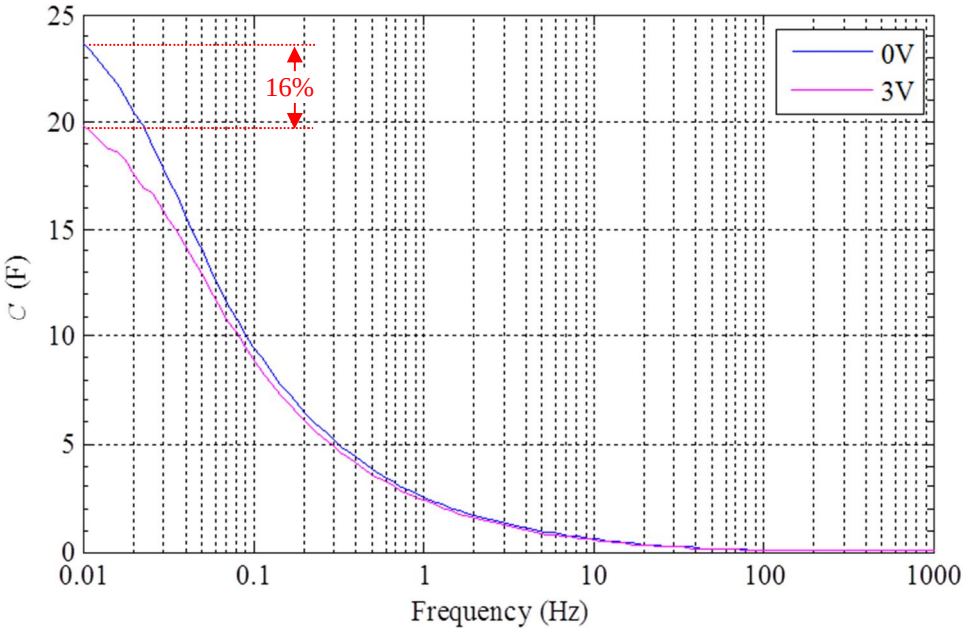


Figure B.20 Equivalent capacitance versus frequency range 10mHz to 1kHz of the three-cell supercapattery stack at the applied voltage 0V and 3V

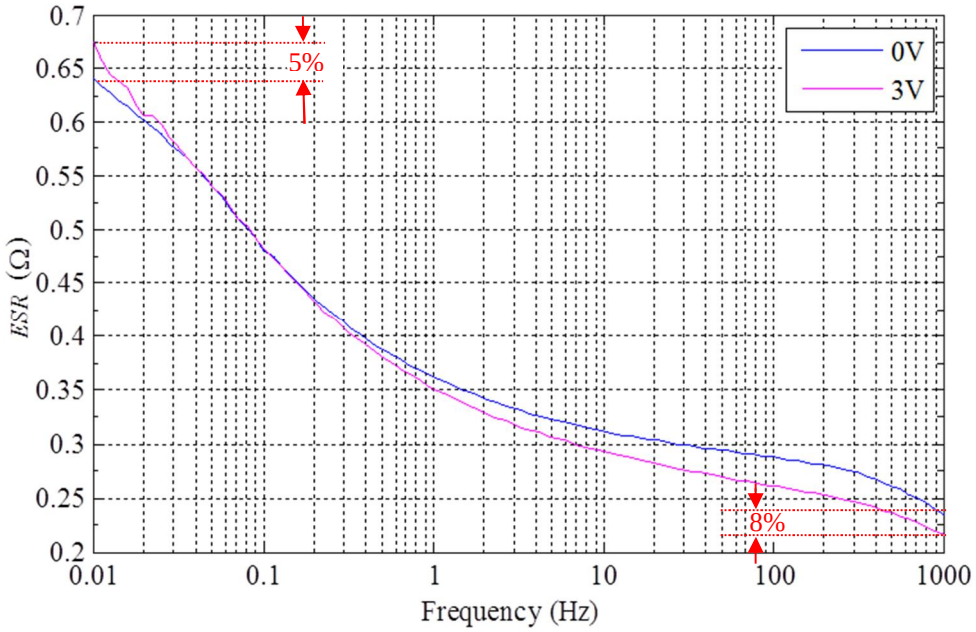


Figure B.21 Equivalent series resistor versus frequency range 10mHz to 1kHz of the three-cell supercapattery stack at the applied voltage 0V and 3V

As mention in Section 2.2, the three-cell supercapattery stack is developed differently from the nineteen-cell stack. On the electrode of this supercapattery stack, a thick-coated carbon-nanotube layer is used. Therefore, more charges can be stored, which increases the stack energy capacity than the nineteen-cell stack architecture as the experimental result presented in Figure B.20. The measurement result of Figure B.20 at 10mHz indicates that the capacitance is approximately 24F, which is less than the rated of 30F specified by the School of Chemical Engineering (Table 2.1). However, from the capacitance-frequency projection, the capacitance may reach 30F if the frequency is reduced further, but the investigate stops at 10mHz frequency setting due to accuracy limitation of the equipment at the low frequency region.

In fact, the thick carbon-nanotube layer increases the cell capacitance dramatically as well as the *ESR* as indicated in Figure B.21 For the DC-bias effect on the three-cell supercapattery stack, the capacitance at 10mHz is reduced by 16% when applying with 3V bias voltage as presented in Figure B.20. On the other hand, the 3V DC-bias voltage effect on the *ESR* is mild, which is approximately 5% at 10mHz and 8% at 1kHz as presented in Figure B.21. It can be seen that the effect of DC-bias voltage on the supercapattery stack I and II are different due the ways they are optimized and constructed, whether they are power or energy enhance.

The identification process is applied to the experimental results obtained at 3V DC-bias voltage that presented in Figure B.20 and Figure B.21 to derive model parameters based on model IV_2 (Figure B.3). The 3V result is chosen since it will be used for further evaluation and in comparison with the PCC result. The impedance results are shown in Figure B.22 and Figure B.23. The derived model parameters are presented in Table B.6.

From Figure B.22 and Figure B.23, it is clearly to see that the real impedance term derived from the model does not fit correctly to the experimental real impedance particularly at the high frequency region beyond 10Hz. This poor fitting is also indicated in Table B.6 as the real R^2 is diverged from 1. In addition, from Table B.6, the R_{add} and C_{add} used in the identification algorithm are chosen as small values compared with the R_S and C_S parameters. Thus, the role of additional RC branch in this case is to correct the model impedance at the high frequency range. The condition of the selected R_{add} and C_{add} parameter, in this case, is opposite to the fitting done with the Maxwell® PC5 stack II and the supercapattery stack I, in which the role of the additional branch is to correct the impedance in the low frequency region.

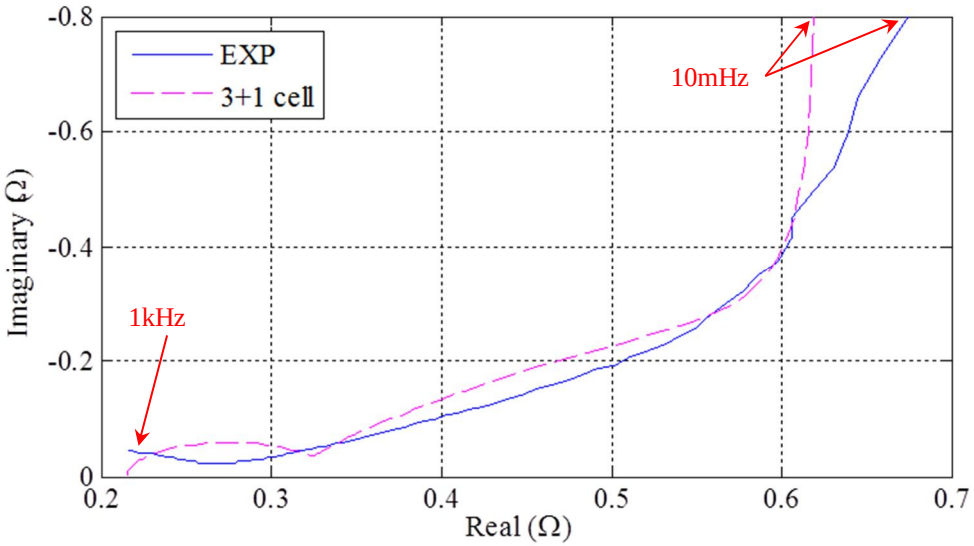


Figure B.22 Real and imaginary impedance terms versus frequency of the 3V-bias measured and model IV_2 (3+1 cells) of the supercapattery stack II

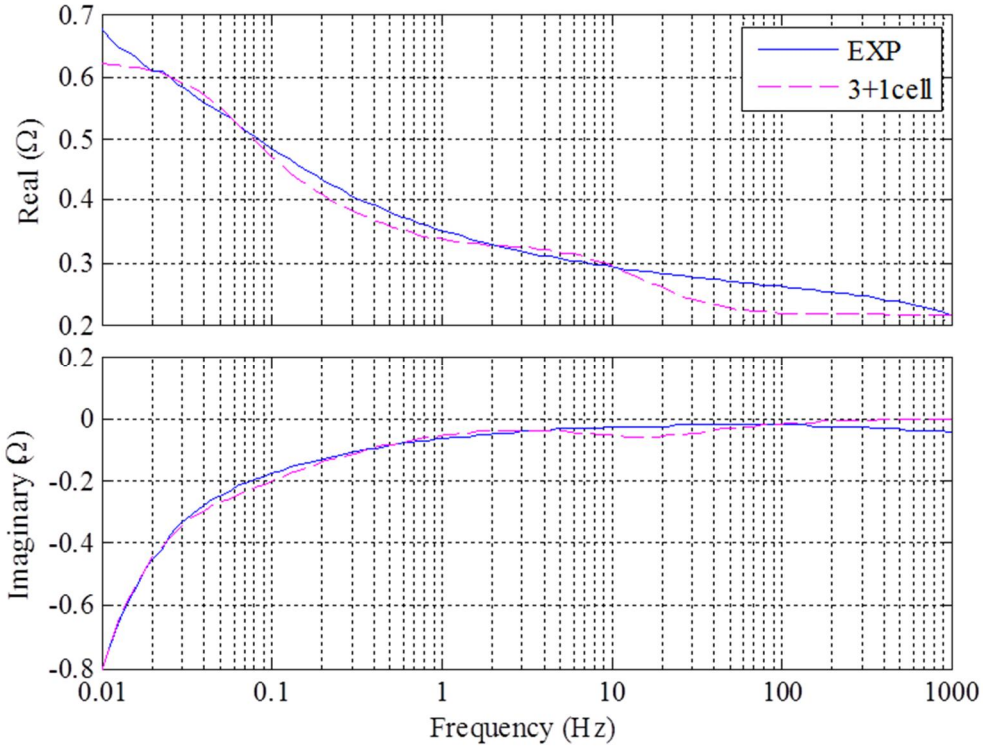


Figure B.23 Imaginary versus real impedance terms of the 3V-bias measured and model IV_2 (3+1 cells) of the supercapattery stack II

Table B.6 The model IV_2 parameters derived from the EIS experimental result of the supercapattery stack II at 3V-bias voltages

N	R_{add} (Ω)	C_{add} (F)	R_S (Ω)	L_S (nH)	C_S (F)	τ	Real *RMSE* (10^{-3})	Imaginary *RMSE* (10^{-3})	Real R^2 (max=1)	Imaginary R^2 (max=1)
3+1	0.11	0.09	0.2159	20	20.6393	22.3044	24	19.2	0.9635	0.9860

For the other model parameters, R_S and L_S are chosen based on the same criterion as done before with the Maxwell® PC5 stack II and the supercapattery stack I presented in Chapter 4. The derived C_S and τ values indicate that the fitting algorithm is done in the medium frequency region (ie. 0.44Hz). To improve, the fitting further, one more additional RC-branch with high time constant can be added to the identification algorithm optionally.

In the experimental result of Figure B.22, the supercapattery stack II impedance exhibits a half of semi-circle shape at the high frequency range. This is not happened with the Maxwell® PC5 stack and the supercapattery stack I. The half semi-circle shape is magnified as presented in Figure B.24. Also presented in Figure B.24, the selected R_{add} and C_{add} values affect the model algorithm that also tries to imitate the

SC impedance characteristic, which yields a semi-circle shape. In addition, this semi-circle behaviors is found in a battery impedance result typically [126], which is due to a charge-transfer characteristic. The charge-transfer characteristic can be described with the model proposed in [126], which is out of scope of this thesis.

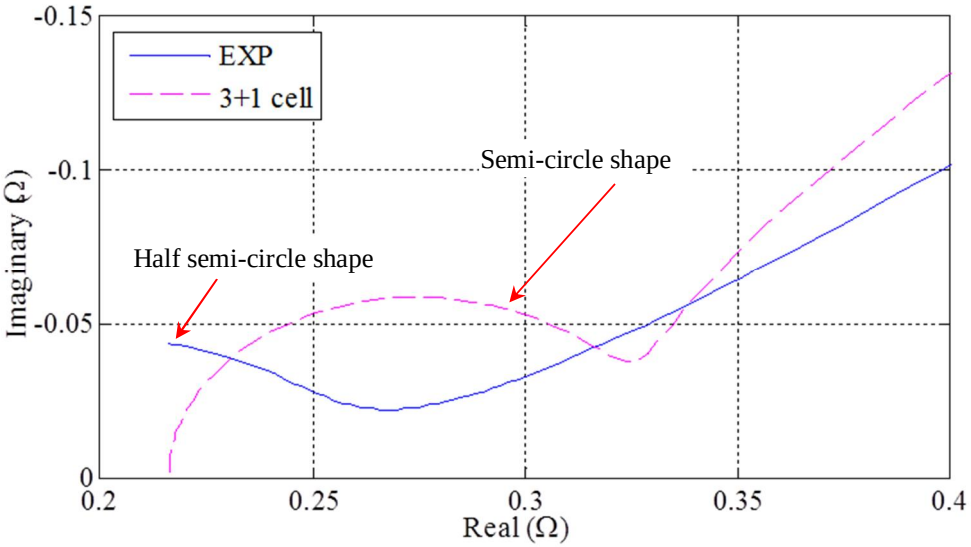


Figure B.24 The zoom-in version of Figure B.23 at the high frequency region

B.2.2 SC Characterization Results Using the Pulse Constant Current (PCC) Method and Its Model Identification Algorithm

The supercapattery stack II is also characterized by the PCC at I_P = -1.825A for T_P = 2.621s, and the v_{SC} is recorded as shown in Figure B.25. The V_i, V_f and V_{avrg} are 3.199V, 2.931V and 3.064V. Note that the v_{SC} is low noise and non-filtered. The fitting process is performed as same as before on the relaxation period, and the fitted coefficients and the model parameters are presented in Table B.7 and Table B.8. The model parameters presented in Table B.8 are constructed, simulated and compared with the experimental result as shown in Figure B.26 and Figure B.27.

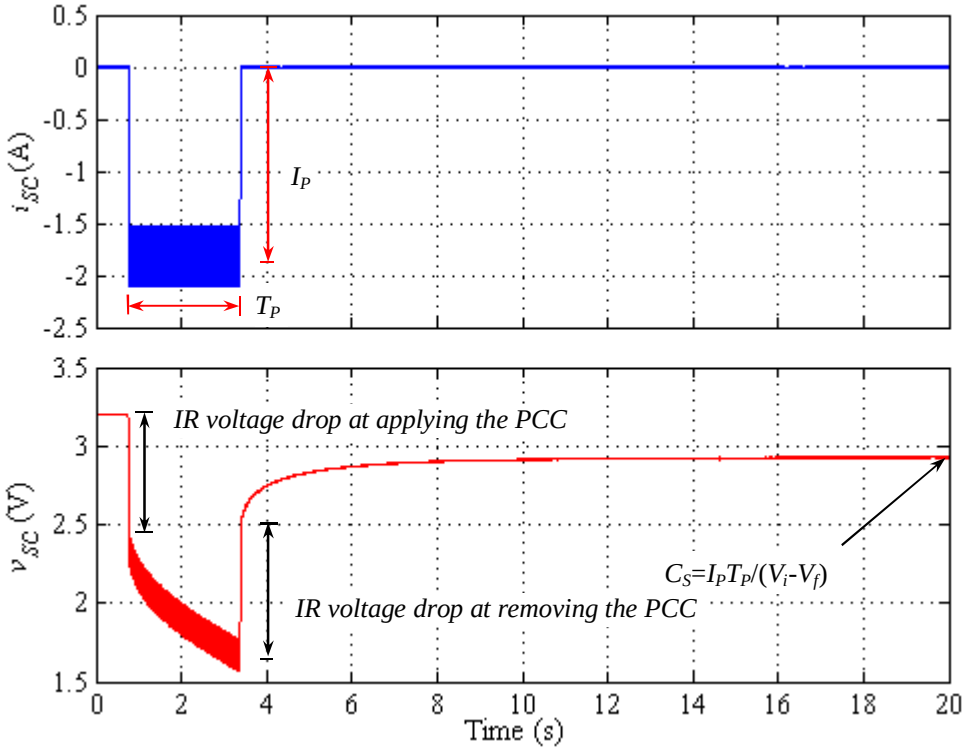


Figure B.25 Experimental result of a negative pulse current on the 30F 5V SCAP stack (I_P = –1.825A, V_i = 3.199V, V_f = 2.931V, V_{avrg} = 3.064V and T_P = 2.6214s)

The PCC result for this low voltage stack (ie. 5V) is interesting as the PCC has dramatically changed the DC-bias voltage level. The effect of DC-bias voltage is impacted directly on the model parameter R_S, which affects the fitting performance during applying the PCC. From Figure B.25, the IR voltage drops at applying and at removing the PCC are observed, and they are different, which are 0.678V and 0.833V. The average value is calculated as 0.7555V, which results in the R_S equals to

0.414Ω. If the IR voltage drop information at removing the PCC alone is used (ie. 0.833V), the R_S is 0.4564Ω, which is 9% higher. The high R_S causes the extra error in the model voltage response during applying pulse as presented in Figure B.26, but it is not affected the voltage response at the relaxation period as shown in Figure B.27.

Table B.7 The fitted coefficients and the error from the MATLAB® Curve Fitting Toolbox™ at N=4

X_1	Y_1	X_2	Y_2	X_3	Y_3	X_4	Y_4	*const*	*RMSE* (10^{-3})	R^2 (max=1)
0.061	0.196	0.199	0.801	0.135	4.359	0.096	47.750	2.931	0.7735	0.9998

Table B.8 The RC parameters extracted from Table B.7 based on model IV_3 expressed in Ω and F

R_1	C_1	R_2	C_2	R_3	C_3	R_4	C_4	R_S	C_S
0.0832	61.2939	0.1244	10.03	0.0738	3.1105	0.0525	0.399	0.414	17.831

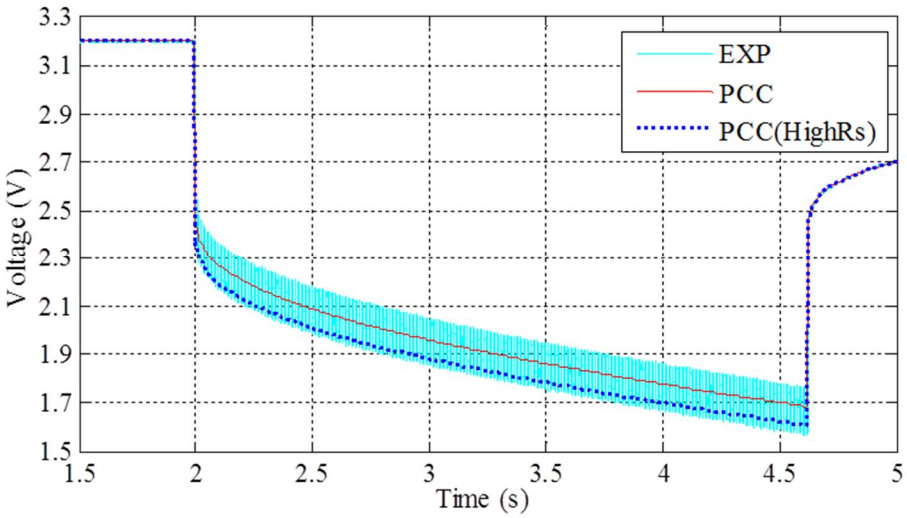


Figure B.26 The comparison of the voltage response during applying the PCC between the experimental result and the simulations with the N = 4

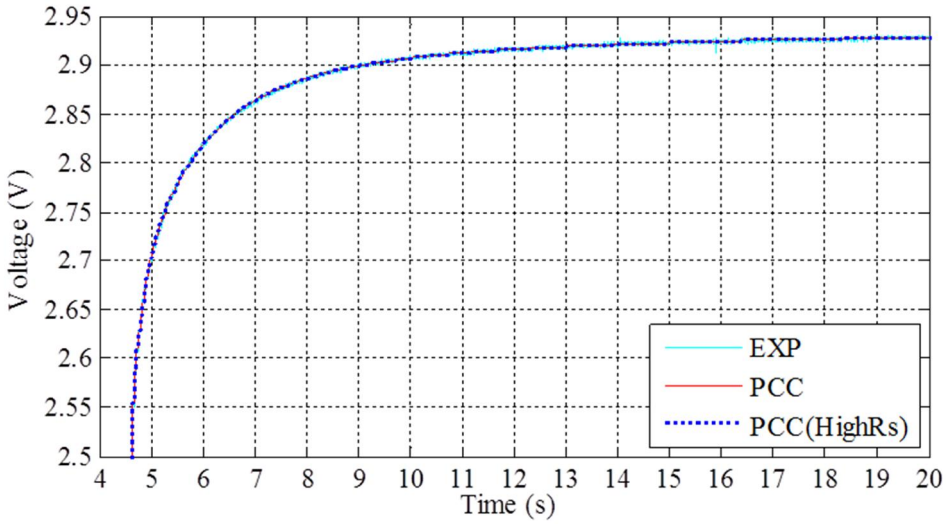


Figure B.27 The comparison of the voltage response after removing the PCC between the experimental result and the simulations with the $N = 4$

B.2.3 Evaluation of the Electrochemical-Impedance-Spectroscopy-based and the Pulse-Constant-Current-based models

Firstly, the frequency response of the PCC-based model presented of Figure B.7 is simulated, and the result (PCC) is compared with the experimental results (EIS-EXP) and with the EIS-based model (EIS) presented in Figure B.22. The comparison is shown in Figure B.28 and Figure B.29. Note that all results are either obtained or derived from nearly the same DC bias-voltage of 3V.

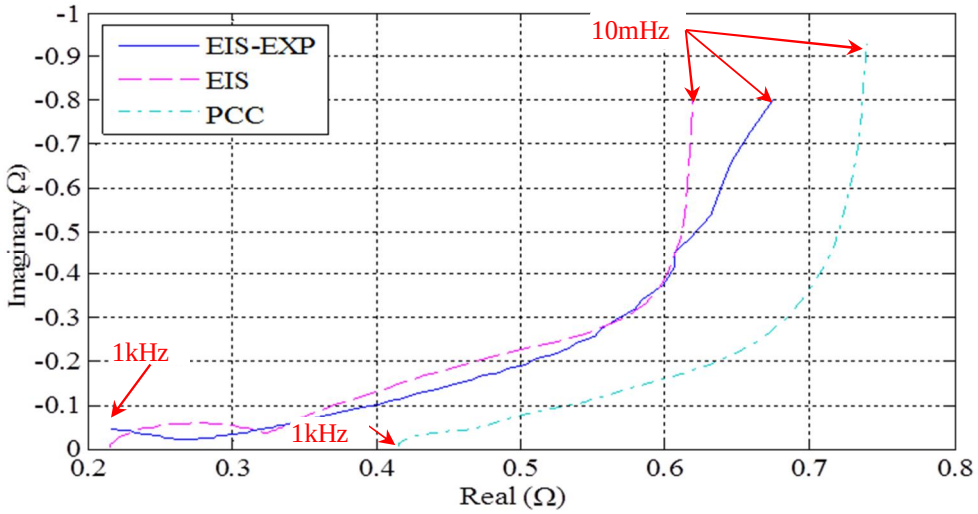


Figure B.28 Imaginary versus real impedance terms of the 3V-bias EIS experimental result, the EIS-derived and the PCC-derived results of the supercapattery stack II

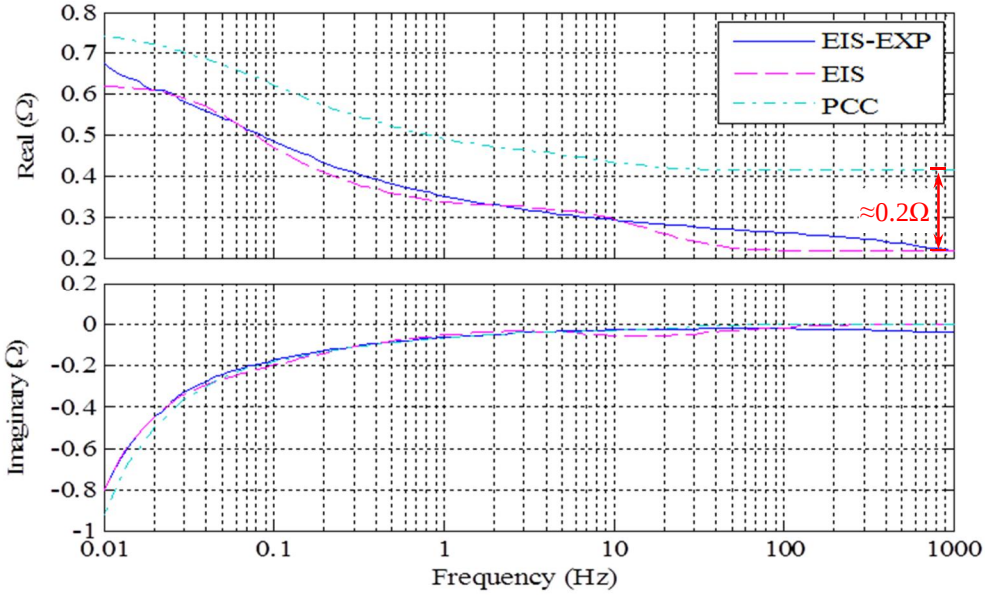


Figure B.29 Real and imaginary impedance terms versus frequency of the 3V-bias EIS experimental result, the EIS-derived and the PCC-derived results of the supercapattery stack II

Figure B.28 shows the imaginary versus the real impedance terms of the PCC, the EIS, and the EIS-EXP results. It is clearly seen that for the entire frequency range, the real impedance part of the PCC is more than both the EIS-EXP and the EIS. The results are re-plotted as the real and the imaginary impedance terms versus frequency as presented in Figure B.29. The overall fitting result between the imaginary impedance part of the PCC and the EIS-EXP is acceptable except at the low-end and the high-end frequency range <0.1Hz and >10Hz as the PCC term is diverged from the EIS-EXP. In addition, from Figure B.29, there is a large offset error in the real impedance part between the PCC and the EIS-EXP. The error is mainly due to the R_S used in the PCC-based model, which is higher than the EIS-based model by ≈0.2 Ω as also indicated in Figure B.29. The errors between the PCC and the EIS-EXP, and between the EIS and the EIS-EXP are presented in Table B.9. As expected, the imaginary *RMSE* and R^2 are small for both models, and the real *RMSE* of the PCC is large. The real R^2 of the PCC model is not available since the result is out of agreement with the EIS-EXP.

Table B.9 Error between the EIS and the PCC models and the EIS experimental result

Model from	Real *RMSE* (10^{-3})	Imaginary *RMSE* (10^{-3})	Real R^2 (max=1)	Imaginary R^2 (max=1)
EIS	24.032	19.16	0.9633	0.9859
PCC	144.062	29.45	-	0.9669

Next, the EIS-based model is evaluated with the PCC method, and the result is compared with both the PCC-based model and the PCC experimental result (denoted as PCC-EXP) as shown in Figure B.30 and Figure B.31.

From Figure B.30, considering the voltage response after removing the PCC (ie. the relaxation period), the EIS has the final steady-state voltage and error higher than the PCC and the PCC-EXP. This unequal steady-state voltage is explained by the difference in the C_S value used in each model. The EIS and the PCC C_S parameters are 20.6393F and 17.831F (ie. 13.6% less). The parameter difference cause the EIS bouncing voltage after discharge to become higher than that of the PCC even though both the imaginary terms analyzed from the frequency response (Figure B.29) are in very good agreement.

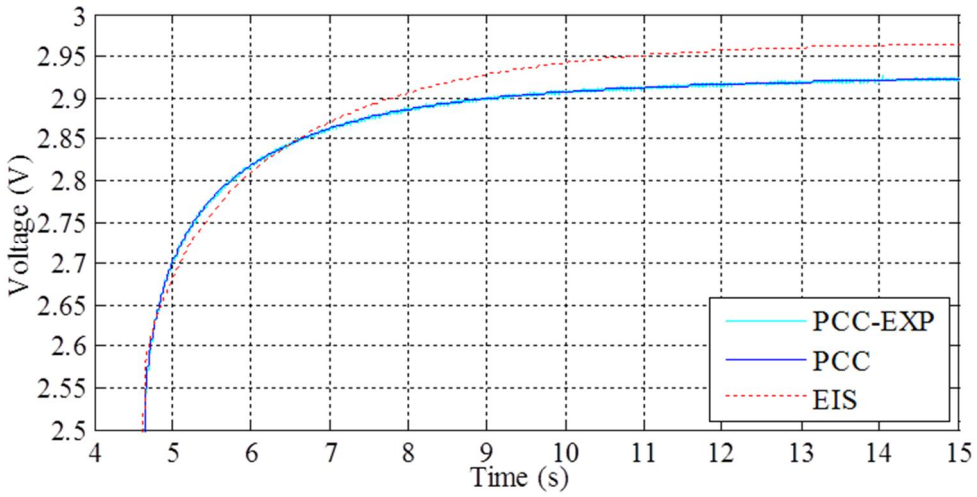


Figure B.30 The comparison of the voltage response after removing the PCC between the EIS-based model, the PCC-based model and the PCC experimental result

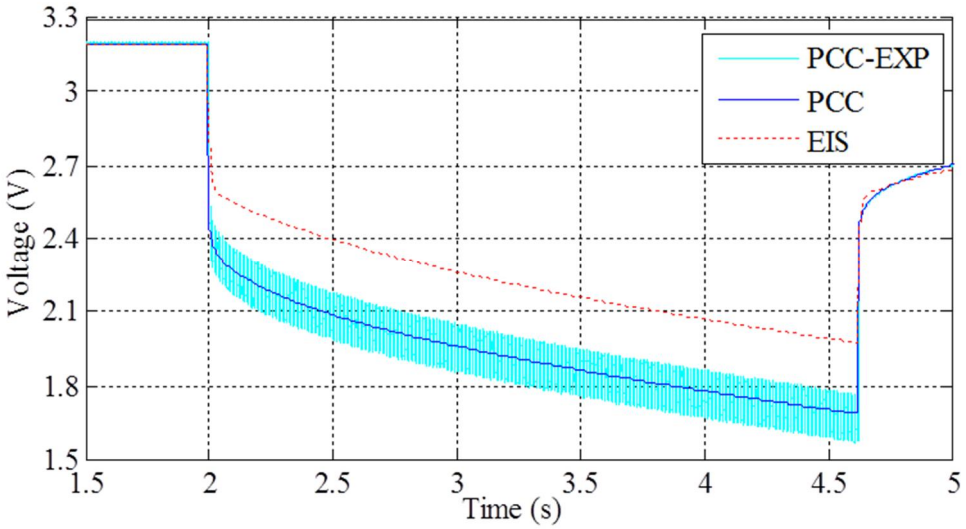


Figure B.31 The comparison of the voltage response during applying the PCC method between the EIS-based model, the PCC-based model and the PCC experimental result

During the applying PCC period, the EIS voltage response does not fit the PCC-EXP as indicated in Figure B.30. Since the EIS R_S value is smaller than the PCC as discussed in the frequency response evaluation, the EIS IR voltage drop is also smaller. However, if considering same R_S used in each model, the PCC and EIS voltage response waveform will be closely in agreement.

The difference in R_S and C_S parameters between the EIS and the PCC models is not caused by the mismatch in the DC-bias voltage conditions of each method. Since from the EIS result presented in Figure B.20 and Figure B.21, the effect of the DC-bias voltage changing from 0V to 3V on the 1kHz resistance is only 8%, so this effect cannot increase the R_S by 91% (from 0.2159 Ω to 0.414Ω). In addition, the sweeping DC-bias voltage effect on the 100Hz capacitance reduction is 16% from approximately 25F at 0V, but the C_S derived from the PCC at 3V bias is 17.831F, which is 28.6% smaller.

In conclusion, the supercapattery stack II when tested under large-signal testing, the device characteristic is different from when the device was tested with the small-signal experiment. Further investigation with this device is required as it exhibits battery-like characteristic, but unfortunately, the device is degraded, so the characterization is discontinued.

B.2.4 The Round-trip Efficiency Evaluation

In this section, the supercapattery stack II round-trip efficiency, η_{RT}, is tested with the CPC method at P of 2, 4 and 6W with V_{SC_min}-V_{SC_max} of 1-5V, 2.25-5V and 3-5V. The testing is started from low to high power levels. The choice of testing conditions (i.e. P, V_{SC_min} and V_{SC_max}) is limited by the device rated current of 2A and the rated voltage of 5V. Thus, to test at higher power, the minimum voltage is increased in order not to exceed the maximum current of 2A that can be handled by the SC. Some experimental results of the CPC testing on the supercapattery stack I are presented in Figure B.32 (2W & 1-5V), Figure B.33 (4W & 2.25-5V) and Figure B.34 (6W & 3-5V). The stack temperature is observed by using a thermal camera at the start and at the end of test as presented in Figure B.35 and Figure B.36. The center point stack temperature is changed by ≈4°C only. It is possible that slightly higher temperatures may develop inside the stack, but due to its flat and thin shape and quite thick metal end plates that provides good cooling, helps the heat to spread out well and prevents dangerous overheating.

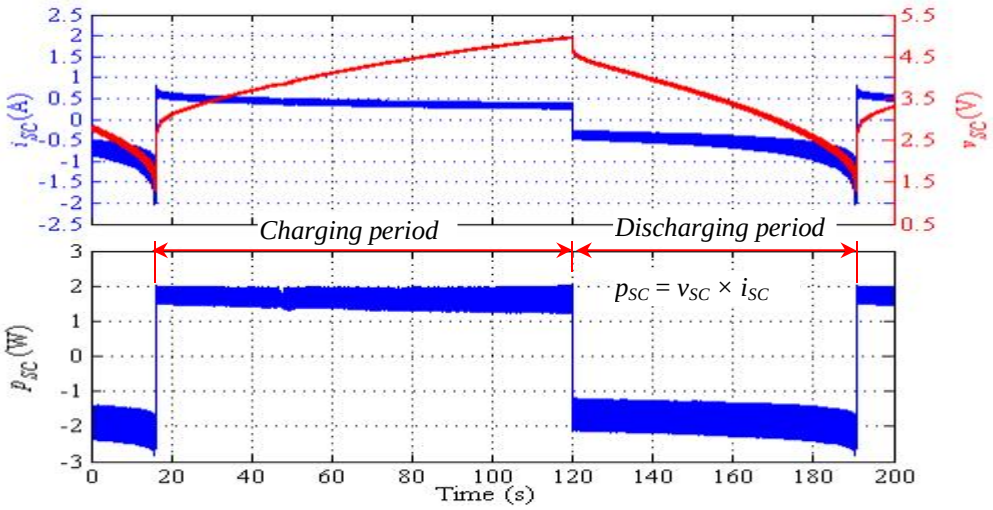


Figure B.32 Voltage, current and power waveform of the SC stack during the charge-discharge tests at P = 2W, V_{SC_min} = 1V and V_{SC_max} = 5V

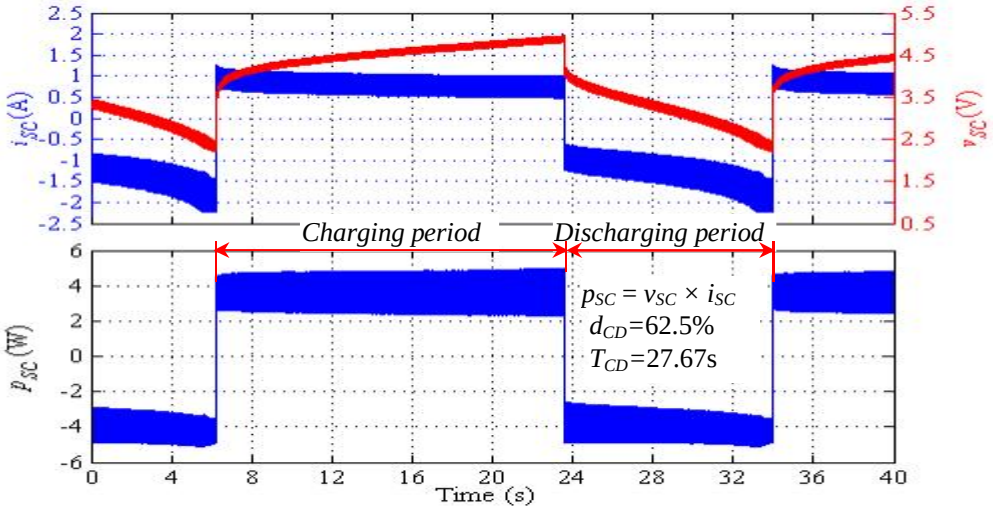


Figure B.33 Voltage, current and power waveform of the SC stack during the charge-discharge tests at P = 4.5W, V_{SC_min} = 2.25V and V_{SC_max} = 5V

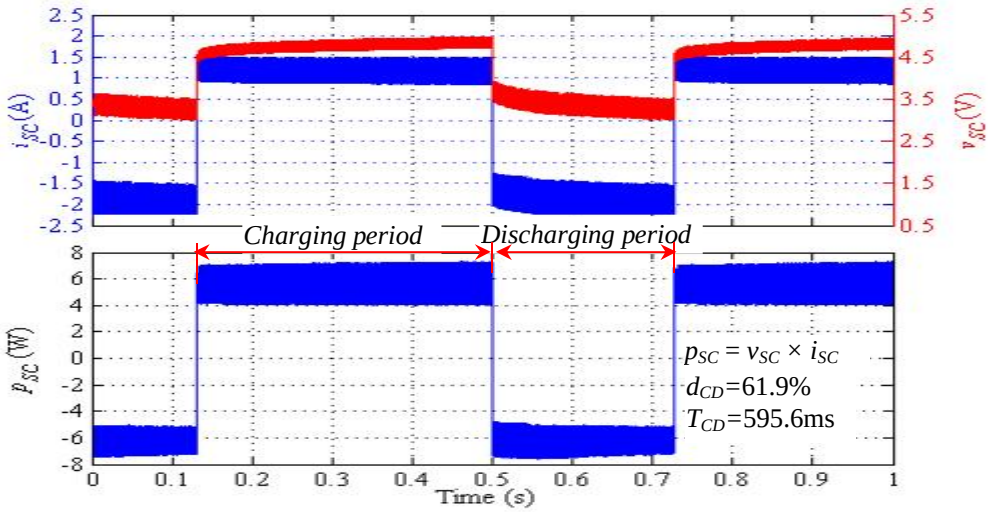


Figure B.34 Voltage, current and power waveform of the SC stack during the charge-discharge tests at P = 6W, V_{SC_min} = 3V and V_{SC_max} = 5V

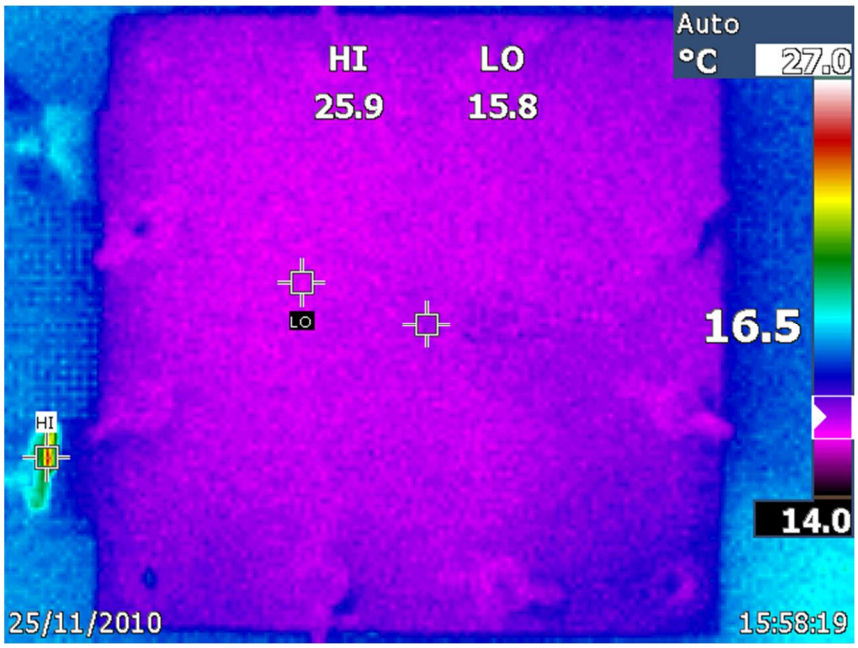


Figure B.35 The supercapattery stack II temperature at the start of the CPC testing

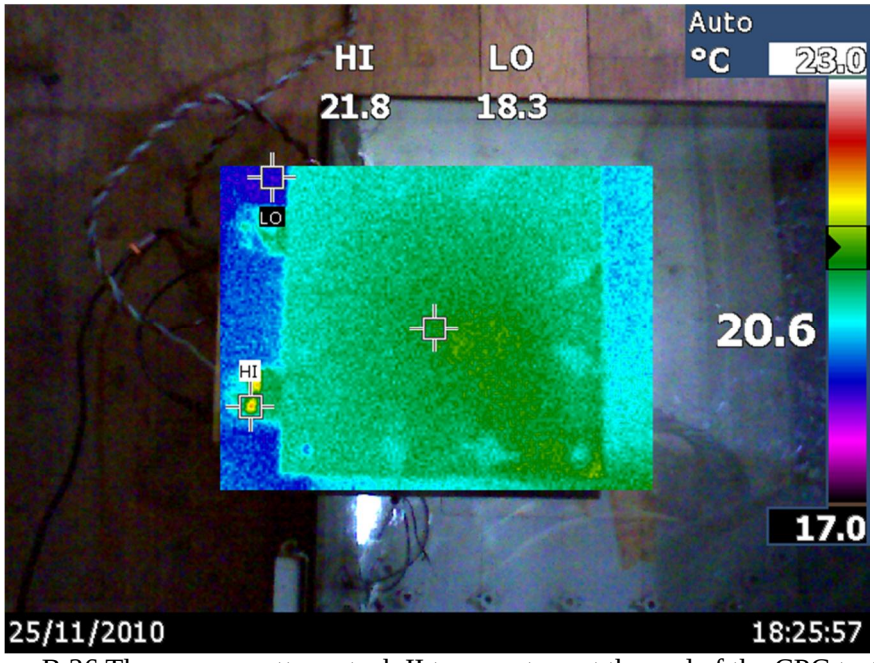


Figure B.36 The supercapattery stack II temperature at the end of the CPC testing

The full experimental results are presented in Table B.10. By using (B.2) and (B.3), a round-trip efficiency and energy loss per charge-discharge cycle, η_{RT_EXP} and $E_{Loss\_RT\_EXP}$, are calculated for each operating point.

Table B.10 The experimental results of the supercapattery stack II under the CPC method

V_{range} (V)	V_{cmin} (V)	V_{cmax} (V)	T_{CD} (s)	f_{CD} (mHz)	P_{C_avrg} (W)	P_{D_avrg} (W)	P_{avrg} (W)	η_{Exp} (%)	$E_{Loss\_RT\_EXP}$ (J)
1-5	2.214	4.842	183.1	5.463	1.6369	1.824	1.73	72.3	50.45
	2.110	4.841	174.6	5.728	1.6387	1.821	1.73	75.8	41.19
2.25-5	3.038	4.602	28.31	35.32	3.5837	4.056	3.82	67.1	20.99
	3.033	4.601	27.67	36.14	3.5933	4.05	3.82	67.6	20.11
	3.041	4.599	27.47	36.4	3.5865	4.052	3.82	67.7	19.91
3-5	3.995	4.393	0.612	1633	5.5766	6.281	5.93	68.2	0.68
	3.996	4.408	0.596	1679	5.5827	6.282	5.93	69.4	0.63

From Table B.10, as the minimum operating voltage is increased from 1V to 2.25V as well as the average power level changing from 1.7W to 3.8W, the efficiency reduces from 72-75% to 67%. However, as the minimum voltage increases further to 3V and the processing power increases to ≈6W, the efficiency is increased slightly from 67% to 68-69%. This nonlinear power-efficiency relationship is explained by an increase in processing energy and power is less than the energy loss reduction due to the corresponding *ESR* is reduced. As the processing power increases from 1.7W to 6W, the charge-discharge period decreases from ≈200 seconds (5mHz) to <1 second (>1Hz), which results in the *ESR* reduction by 50% according to Figure B.21. Note that the ESR 5mHz is not available, so the 10mHz *ESR* value is used in the calculation. The *ESR* reduction effect reduces the energy loss dramatically from 41-50J to <1J as the power level increases from 1.7W to 6W.

B.3 The Maxwell® BMOD0052 SC Stack

The EIS method is applied to the Maxwell® SC commercial stack BMOD0052 to inspect its impedance-frequency characteristic. The testing frequency is swept from 10mHz to 1kHz at 3V, 6V, 9V, 12V and 15V DC-bias voltages. In addition, in the experiment, the measurement is done carefully to minimise the contact resistance that may come from lead cable resistance and a loose connection problem since the specified *ESR* in the Maxwell® BMOD0052 datasheet is in mΩ range. Furthermore, to perform the EIS method on this large capacitance stack, the time required to let the stack voltage to reach its steady-state is longer than the small capacitance stack (ie. the PC5 stack). The 1-hour voltage holding period is applied as suggested in Section 2.2, after changing the DC-bias voltage to ensure the steady-state condition of the stack before performing the EIS method. Since the device has been used before conducting the EIS testing, the device is expected to be different from the specification defined in the datasheet. The capacitance is expected to be reduced within 20% from the rated value while the *ESR* is expected to increase within 100% from the rated value [90]. This is indicated in the experimental results based on the simple RC model as presented in Figure B.37 and Figure B.38.

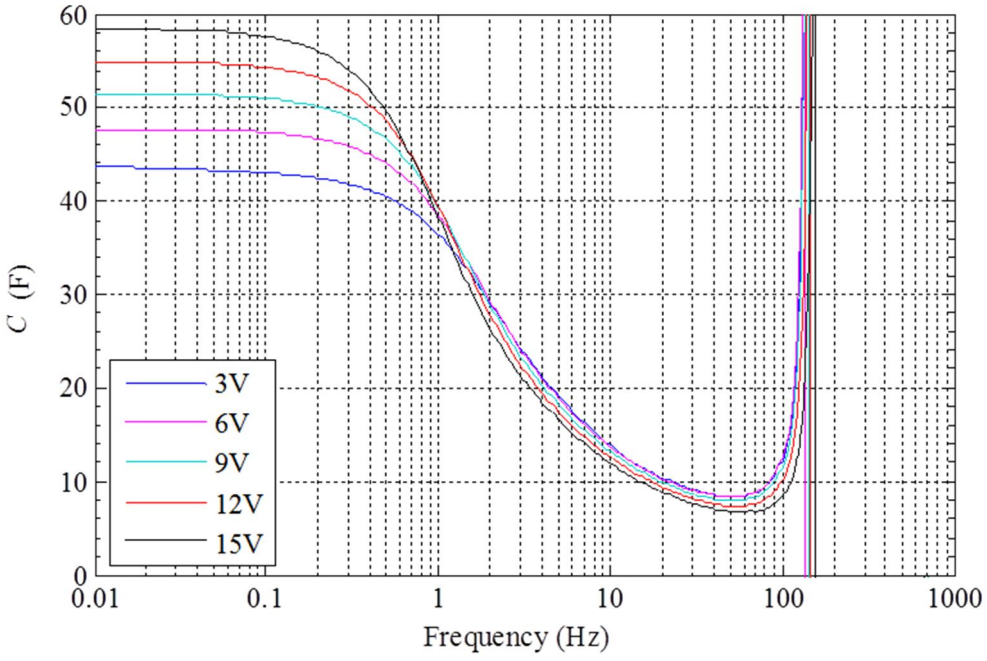


Figure B.37 Equivalent capacitance versus frequency range 10mHz to 1kHz of Maxwell BMOD 15V (Bio-Logic) at the applied voltage of 3V, 6V, 9V, 12V and 15V

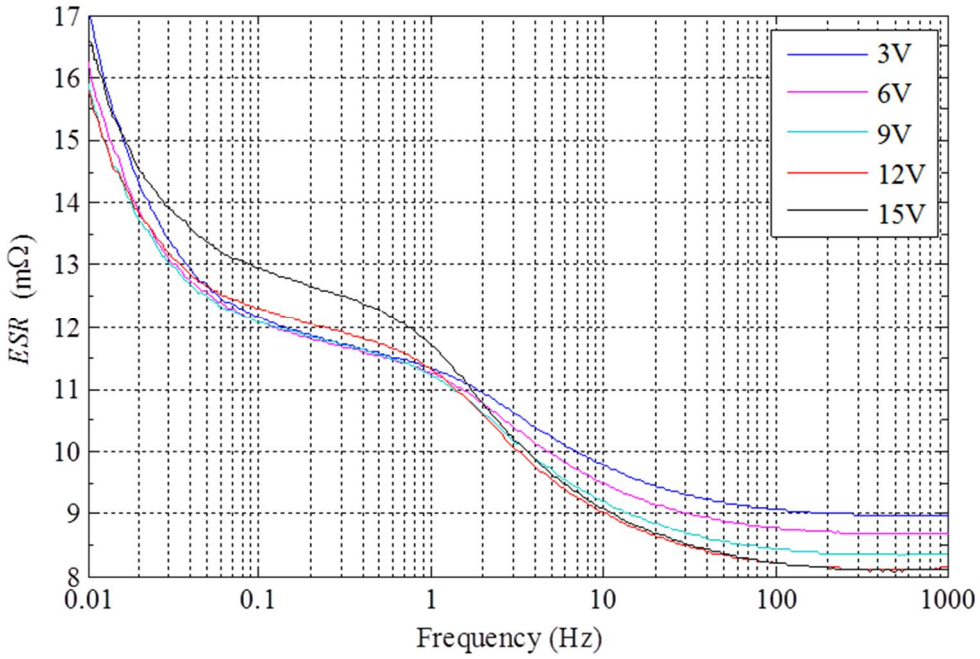


Figure B.38 Equivalent series resistor versus frequency range 10mHz to 1kHz of Maxwell BMOD 15V (Bio-Logic) at the applied voltage of 3V, 6V, 9V, 12V and 15V

From Figure B.37, the capacitance at 10mHz is increased when increasing the applied DC-bias voltage. This capacitance-voltage relationship is similar to the Maxwell® PC5 since the technology is the same. In addition, the 10mHz derived capacitance is increased linearly by 34% over the 12V DC-bias sweep as presented in Figure B.39. Using the 10mHz capacitances at 6V and 9V bias voltage conditions, the 10mHz capacitance at 7.5V is calculated as 49.48F. This 10mHz capacitance at 7.5V should be equal to the rated (52F), however, it is ≈5% less, which is due to the device degradation as expected.

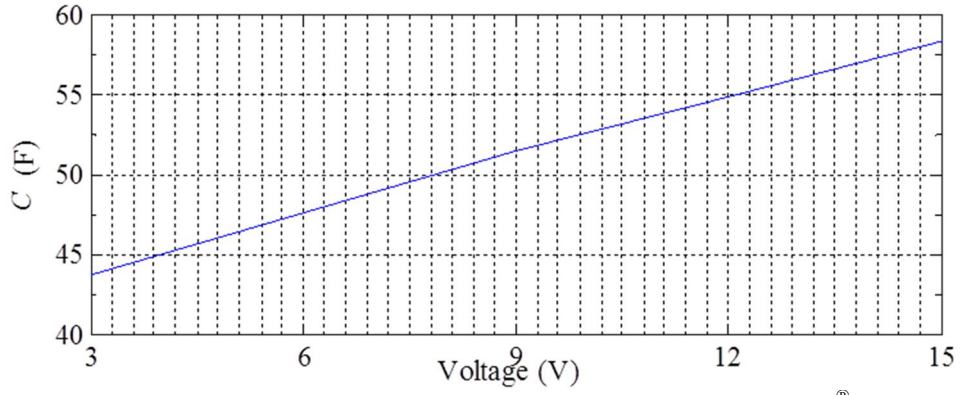


Figure B.39 Equivalent capacitance versus DC-bias voltage of the Maxwell® BMOD0052 at 10mHz

In Figure B.39, the capacitance-frequency results also reveal a resonant frequency at around 200Hz. This resonant characteristic is shown up in the low frequency region due to the module large capacitance and stray inductance. According to the datasheet, the Maxwell BMOD0052 physical size and volume is larger than the Maxwell PC5, so the Maxwell BMOD0052 stray inductance is expected to be larger than the Maxwell PC5 stacks. Therefore, the resonant frequency is shifted from the high frequency region (ie. beyond 1kHz) to 100's of Hz and can be calculated by a conventional formula:

$$\omega_{res} = \frac{1}{\sqrt{L_S C}} \tag{B.1}$$

where ω_{res} is a resonant frequency in rad/s and L_S series inductance. If using C = 52F, at 200Hz, L_S = 12nH, which is typical for large capacitance module.

From Figure B.38, the *ESR* versus frequency at various applied DC-bias voltages is presented. The *ESR* at 10mHz and at 1kHz are re-plotted against the applied DC-bias voltage and are presented in Figure B.40.

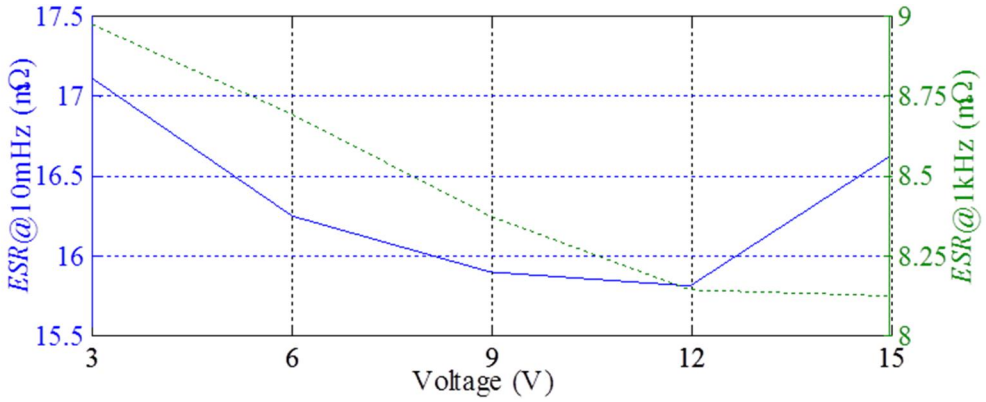


Figure B.40 Equivalent series resistance versus DC-bias voltage of the Maxwell® BMOD0052 at 10mHz and 100Hz

From Figure B.40, the averaged *ESR*@10mHz and *ESR*@1kHz from all presented DC-bias voltage points are 16.33mΩ and 8.1mΩ, which are higher than 14.5mΩ@DC and 8mΩ@1kHz as specified in the datasheet [90]. It can be seen that the degradation affects the *ESR*@10mHz (ie. low frequency *ESR*) more than the *ESR*@1kHz (ie. high frequency *ESR*). In addition, in Figure B.40, the *ESR* is decreased as the applied DC-bias voltage increases, which is similar to the PC5 stack. However, the *ESR*@10mHz at 15V is more than 12V, which is not followed

the pattern. Let's consider back in Figure B.38, the *ESR* at the frequency <1Hz also does not follow the pattern of reducing *ESR* as increasing the DC-bias voltage. This inconsistency results may be due to the self-discharging rate of the BMOD0052 stack, which is 50 times more than the PC5 stack according to the datasheets [90].

B.4 The ELIT® SC Stack

The ELIT® stack is built with an aqueous electrolyte type as well as the supercapattery, so it is interesting to observe its impedance characteristic and compare with the supercapattery. Therefore, the EIS method is applied to the ELIT® SC with the swept frequency from 10mHz to 100Hz and at 5V, 12V, 15V and 17.5V DC-bias voltage conditions. The experimental results based on the simple RC model are presented in Figure B.41, Figure B.42 and Figure B.43. Note that the measurement is done with extra lead cable, which results in additional stray inductance and *ESR* presented in the results.

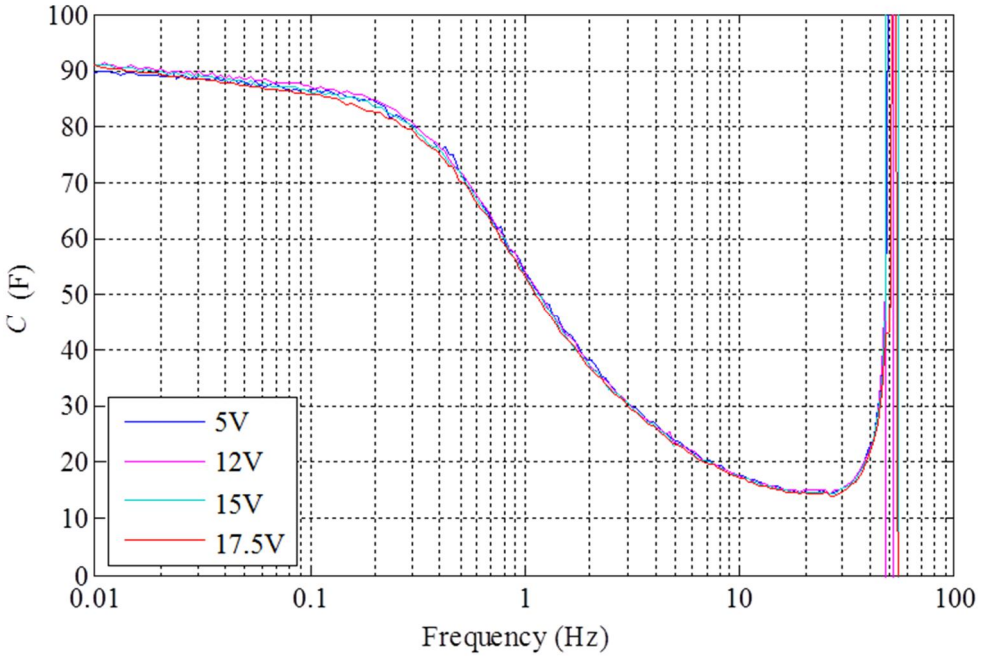


Figure B.41 Equivalent capacitance versus frequency range 10mHz to 100Hz of ELIT at the applied voltage of 5V, 12V, 15V, 17.5V

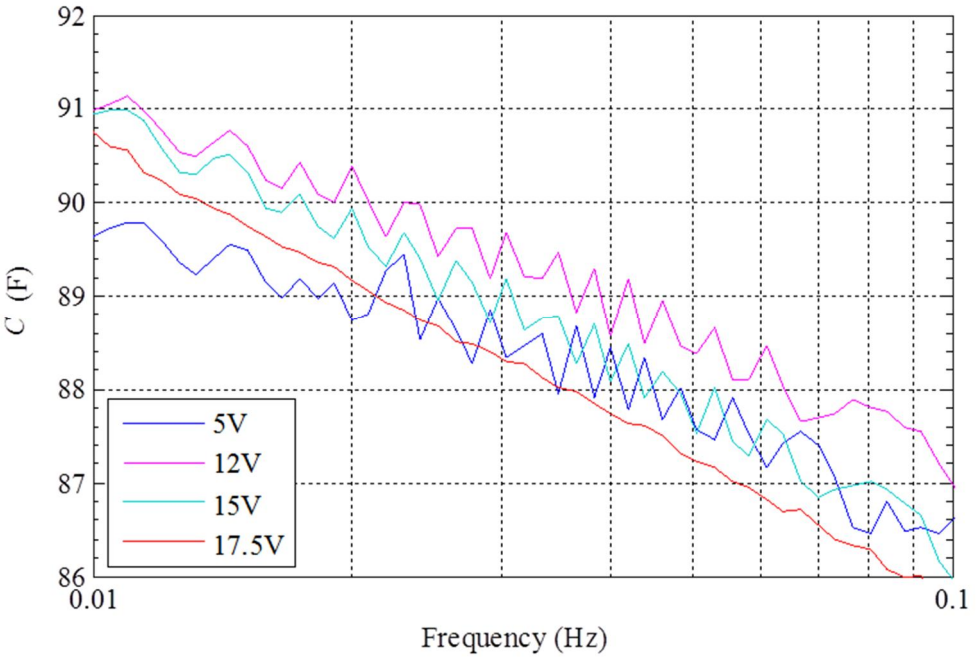


Figure B.42 Equivalent capacitance versus frequency range 10mHz to 100Hz of ELIT at the applied voltage of 5V, 12V, 15V, 17.5V (zoom-in)

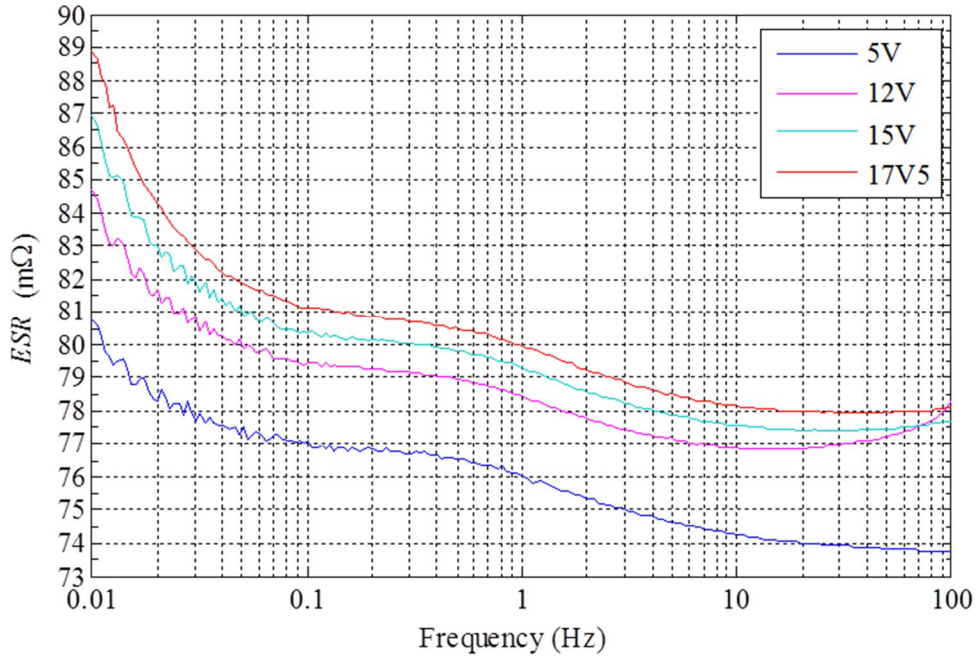


Figure B.43 Equivalent series resistor versus frequency range 10mHz to 100Hz of ELIT stack at the applied voltage of 5V, 12V, 15V, 17.5V

From Figure B.41, for all frequency range, the ELIT® capacitance is only slightly affected by the applied DC-bias voltage, and this characteristic is similar to the supercapattery stack I. The zoom-in capacitance values at the frequency between 10mHz and 100mHz are presented in Figure B.42 for inspecting the capacitance

variation due to the applied voltage. The capacitance is varied between 90 to 91F, which is more than the value described in the datasheet information (C > 85F).

In addition, from Figure B.41, the capacitance-frequency results also reveal a resonant frequency at ≈50Hz. This resonant characteristic is shown up in the low frequency region due to the large capacitance and stray inductance condition similar to the Maxwell BMOD0052 experimental result. If using (B.1) and let C = 90F, the L_S = 11µH. However, there is additional stray inductance from the lead cable, which alters the actual resonant frequency due to the device inductance. The actual L_S is expected to be within nH range.

From Figure B.43, the *ESR* versus frequency at various applied DC-bias voltages is presented. The *ESR*s at 10mHz and at 100Hz are re-plotted against the applied DC-bias voltage and are presented in Figure B.44.

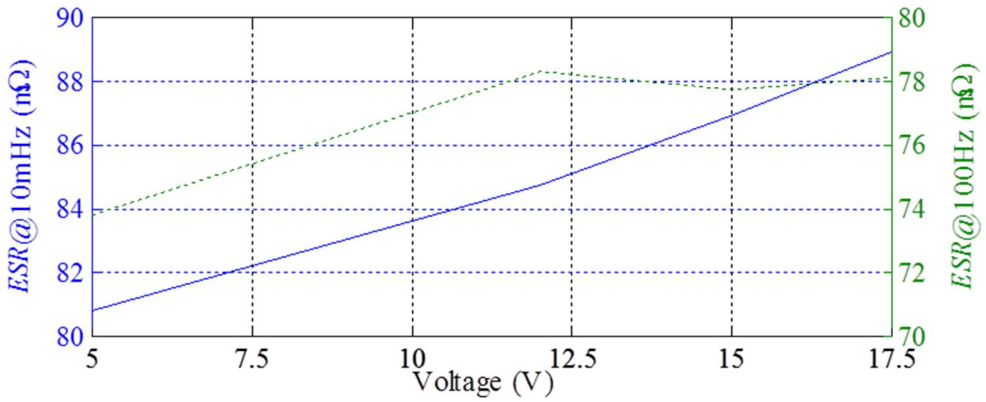


Figure B.44 Equivalent series resistance versus DC-bias voltage of the ELIT SC at 10mHz and 100Hz

Since the measurement was done with long lead cable in additional to the equipment cable, the absolute value of the measured *ESR* in this case is irrelevant to what is specified in the datasheet (*ESR*@DC <4.2mΩ). However, from the measurement result, the *ESR* is varied with the applied DC-bias voltage as it is increased with applied DC-bias voltage as presented in Figure B.44 for both the 10mHz and 100Hz *ESR*s.

Appendix C : Measurement Equipment Error Inspection

This appendix consists of three sections, where the precision of each of the components used in the measurements were evaluated. The current and the voltage probes connected to a LeCroy HRO 64Zi digital oscilloscope (12-bit vertical resolution) used in Chapter 4 experiment were tested using a calibrator to evaluate their accuracy. The current probe under test is the PR30 LEM® and the voltage probe under test is TENMA 1:1 passive type. These probes were tested in conjunction with a Ballatine® 1620A transconductance and a Datron® model 4705 multifunction calibrator that would output very precise levels of voltage and currents. The Ballatine® machine is a precision current source, which outputs an accurate current level according to the input voltage fed from the Datron® machine. The accuracy validations of both current and voltage probes are presented in Section C.1 and C.2.

The measured SC current and voltage data is processed internally by the digital oscilloscope to construct the SC power data, which is used in conjunction with the charging or discharging period to calculate the charging or discharging energy. However, evaluating the SC charging and discharging energy is a more complex task as the SC impedance is quite often not constant with the SC voltage. This non-linearity leads to additional errors in the energy loss calculation or estimation. Therefore, the methodology had to be improves by using a more accurate the LeCroy® current probe with the LeCroy® oscilloscope and using the Bio-Logic SP-150 impedance spectroscopy equipment with its 20A Booster equipment (Rig III in Chapter 3) as a mean to conduct additional low noise constant power tests and using its embedded 16bit A/D platform as a mean of checking the precision of the less accurate oscilloscope. The validation was carried out by applying the constant current cycling (CCC) test of the SP-150 machine to a 100W/1.5Ω resistive load.

The accuracy validations of both the LeCroy® and the Bio-Logic platforms are presented in Section C.3.

C.1 Current Probe

In Chapter 4, the PR30 LEM current probe was used to measure the experimental current in the range of ±2A with the switching ripple ≈0.5A at the frequency less than 20kHz. Based on the PR30 LEM current probe specification shown in Table C.1, it was decided that the probe bandwidth of 100kHz is sufficient for the measurement. However, the measuring current range is ±30A, which was 10 times higher than the expected level of the experimental current to be measured. Using this probe to measure the current straightaway would result in large error. Therefore, the SC connecting wire was used to wind 10 turns in the current probe window to increase the sensed magnetic field closer to the probe rating. By doing this, the probe sensitivity is increased well above what would have been achieved by measuring low current with a single turn. The probe output range and resolution have improved from 0.1V/A to 1V/A and from ±1mA to ±0.1mA. The output of the current probe was connected to the LeCroy® HRO 64Zi oscilloscope, which was set at the 1V/div range. This adjustment was done to match the setting used to obtain the results presented in Chapter 4.

One thing to note is that the offset calibration of the PR30 probe is done manually by adjusting its potentiometer knob, which is often considered not very precise. The offset can be removed by the way data is processed. When performing the FFT, the DC component present in the current is always removed and only the relevant harmonics are used. However, in case of large cycle period and/or low power test, the device leakage current cannot be neglected and has to be considered in loss estimation. The DC current component derived via the FFT is replaced with that of the device leakage current, which is identified via a separate leakage current test done at relevant bias voltage level as presented in Section 2.5.1.5.

Table C.1 The specification of the PR30 LEM current probe

Parameter	Value
Current range	$20A_{RMS}$
Measuring range	±30A
Output sensitivity	100mV/A
Resolution	±1mA
Accuracy	±1% of reading ±2mA error
Conductor position sensitivity in relative to center reading	±1%
Frequency range	DC to 100kHz (-0.5dB)

The current probe has been tested with the calibrator and the measured results are compared with the calibrator pre-set DC current as shown in Figure C.1. The results show that the error is smaller than 0.24% for the measured currents in the range of -2.5A to -0.4A, below which it increases significantly and remains below 0.35% for the whole positive current direction. From the results it can be concluded that if the offset button could have been further adjusted to cancel 0.1% of the offset seen in the measurement, the error would have been below +/- 0.15%. In addition, the range of the actual experimental current typical for constant current/power presented in Chapter 4 varies only between -2A to -1A during discharging and between 1A to 2A during charging, so the range affected by large error seen in Fig. C1 is not used and the measurement results in very small error (|Error| < 0.4%).

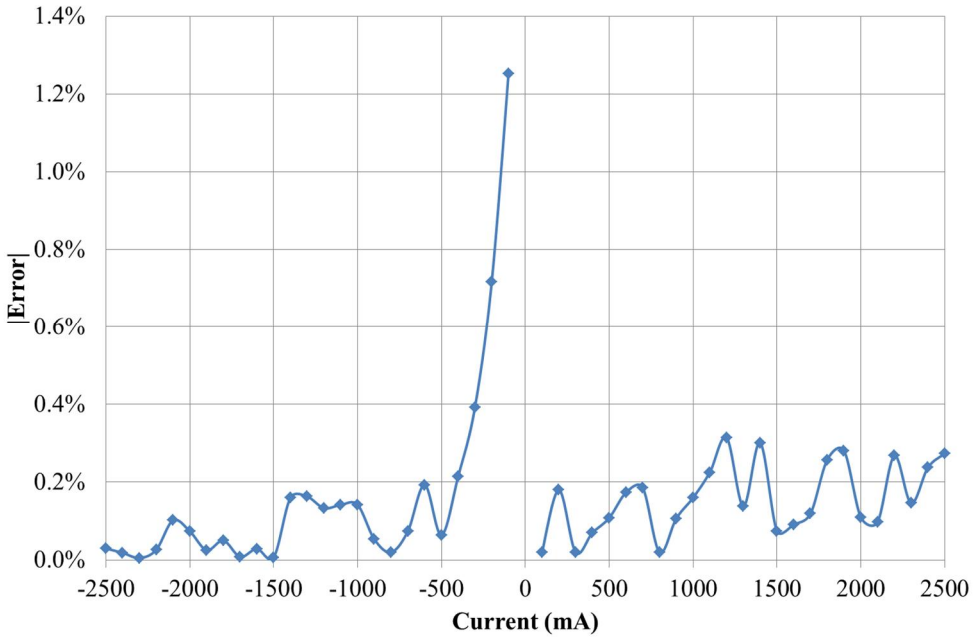


Figure C.1 The PR30 LEM current probe tested with the calibrator

C.2 Voltage probe

In Chapter 4, two of the TENMA 1:1 passive voltage probe were connected to implement a differential voltage measuring configuration, which is equivalent to connect the hot terminal (ground of probes was connected to the common ground) of each probe to each of the SC stack terminals. In this section, these probes are tested in the same configuration with the calibrator. The TENMA probe has the specification as shown in Table C.2.

Table C.2 The specification of the TENMA passive voltage probe

Parameter	Value
Attenuation ratio	1:1
Bandwidth	DC to 10MHz
Rise time	35ns
Input resistance	1MΩ
Input capacitance	90pF
Max input voltage	200V

Both voltage probes used in the power loss/efficiency tests had their precision tested by connecting them to the LeCroy® HRO 64Zi oscilloscope, which was set on the 5V/div range. This adjustment was done to match the setting used to obtain the results presented in Chapter 4. It is noted that during the efficiency tests in Chapter 4, the SC stack voltage was varied between 15V to 20V but both probes are tested with 5 to 35V DC level set from the calibrator. The measured results are compared with the calibrator pre-set DC voltage as shown in Figure C.2. The results show that the absolute error is smaller than 1% for the entire range and the error is smaller than 0.2% in absolute (but less than 0.1% in differential mode) for the relevant 15 to 20V voltage range.

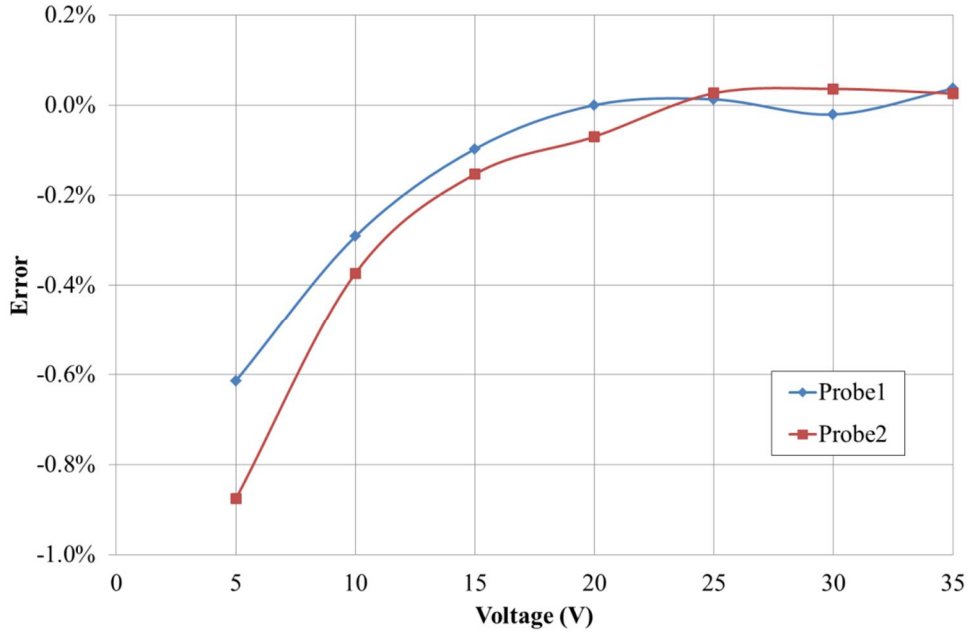


Figure C.2 Precision of the TENMA 1:1 passive voltage probe tested with the calibrator

C.3 Energy Measurement Validation of the LeCroy® Oscilloscope Scope versus the Bio-Logic machine

To validate the measurement accuracy of the LeCroy® HRO 64Zi oscilloscope versus the Bio-Logic SP-150 with its 20A Booster equipment (Rig III in Chapter 3) under the constant current cycling (CCC) test, the 100W/1.5Ω resistive load was used. In fact, the constant current cycling (CCC) test subjects the resistive load to a quasi-square wave current, which is equivalent to the constant power cycling (CPC) having the power level always positive (I^2*R) as shown in Figure C.3. It is noted that in Figure C.3, there is a deadtime of 0.1 second between the positive and the negative current periods.

The load resistance was measured using a 4-wire connection and the resistance measurement function of the Keithley® 2700 multi-meter before and after conducting the CPC test to check the resistance. Both the before and after CPC test results yield the same resistance of 1.497Ω, which confirms that the resistive change due to the temperature is very small. It should be noted that the Keithley® multi-meter was set at the smallest resistance measurement range of 100Ω, which results in a resistance measurement resolution of 0.1mΩ.

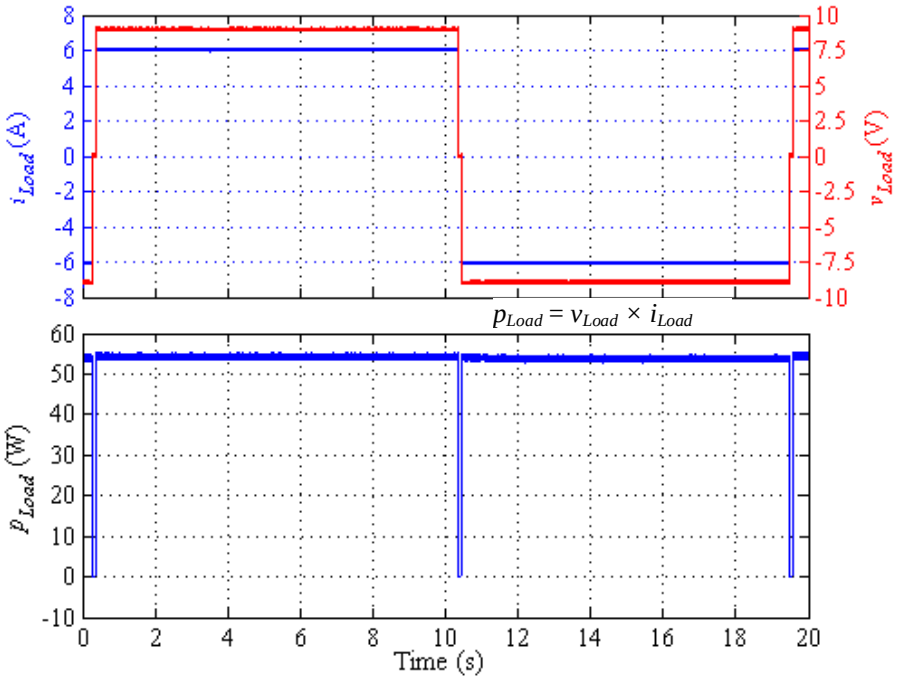


Figure C.3 The current, voltage and power of the resistive load during the CCC test captured by using the oscilloscope

The specifications and settings of both Bio-Logic and the LeCroy® platforms are shown in Table C.3.

Table C.3 Setting and Specification of the Bio-logic and the LeCroy® measurement platform

Parameter Settings	Bio-Logic	LeCroy®
Sampling frequency (kHz)	5	500
Sampling resolution (bit)	16	12
Voltage measurement resolution (mV)	0.305	10
Current measurement resolution (mA)	0.6	3.9
Voltage measurement setting	±10V range	±20V range (5V/div)
Current measurement setting	±20A range	±8A range (2A/div)
Voltage probe	internal	TENMA
Current probe	internal	LeCroy® AP015

From Table C.3, it can be seen that the Bio-Logic platform has a low sampling speed but high accuracy (16bit and 5kHz sampling) while the LeCroy® platform has high sampling speed but low accuracy (12bit and 500kHz sampling). Therefore, it can be concluded that the Bio-Logic has a far better voltage measurement resolution than that of the LeCroy®. The settings of both platforms were done to obtain the best measurement resolution. For the LeCroy® platform, the LeCroy® AP015 current probe was used rather the PR30 LEM® current probe since the AP015 probe has the

auto zero offset and the degaussing functions, which helps in minimizing the measurement offset error.

The CCC test was done at ±6A (resulting in 54W power loss equivalent to the CPC test) to demonstrate bidirectional power processing similar to charging and discharging SC. The load resistor temperature was control less than 60 ^{0}C by mounting it to a heat sink and using a fan to perform force cooling. The durations of the positive and negative current half waves were set to 10 and 9 seconds with the deadtime between half waves of 0.1 second, which is very similar to the SC tests conducted. This will have an effect of different energy loss levels caused by the positive and the negative half waves which allows better visibility of the comparative results. The positive current and the negative current half waves represent SC charging and discharging. The test was run for 100 cycles (each being less than 20s) and the results are shown in Figure C.4. The dissipated energy due to positive current and negative current is denoted as E_p and E_n.

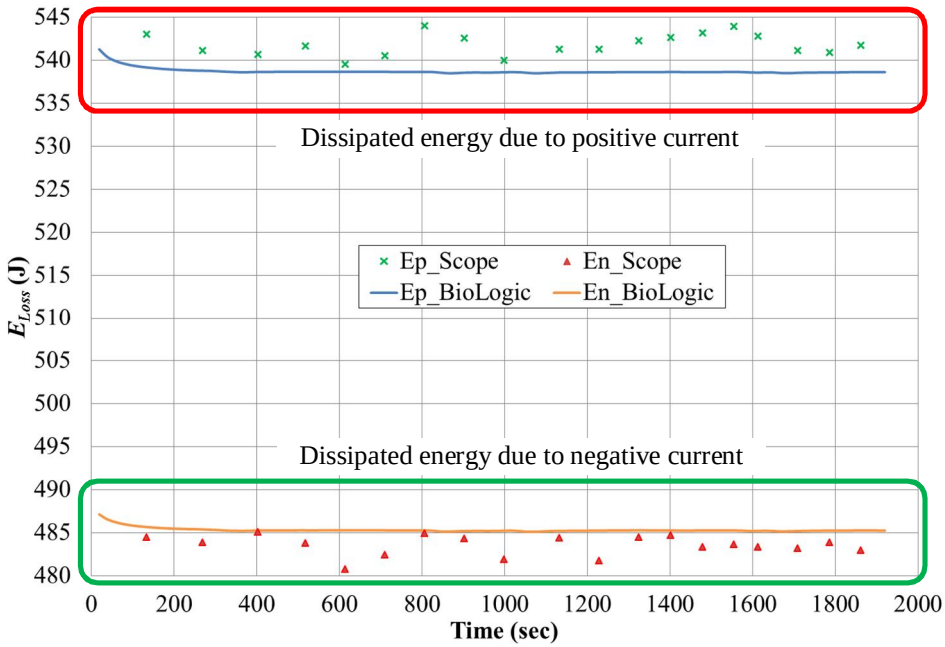


Figure C.4 The dissipated energy during the test

From Figure C.4, the LeCroy® measurement results show larger fluctuation whilst the Bio-Logic measurement results are very smooth/consistent. If the value of the load resistance is considered (1.497Ω), the calculated dissipated energy during the positive current and the negative current conditions should be 538.92J and 485.03J.

Assuming this is correct, the error between the calculated and the measured dissipated energy of both platforms is shown Figure C.5.

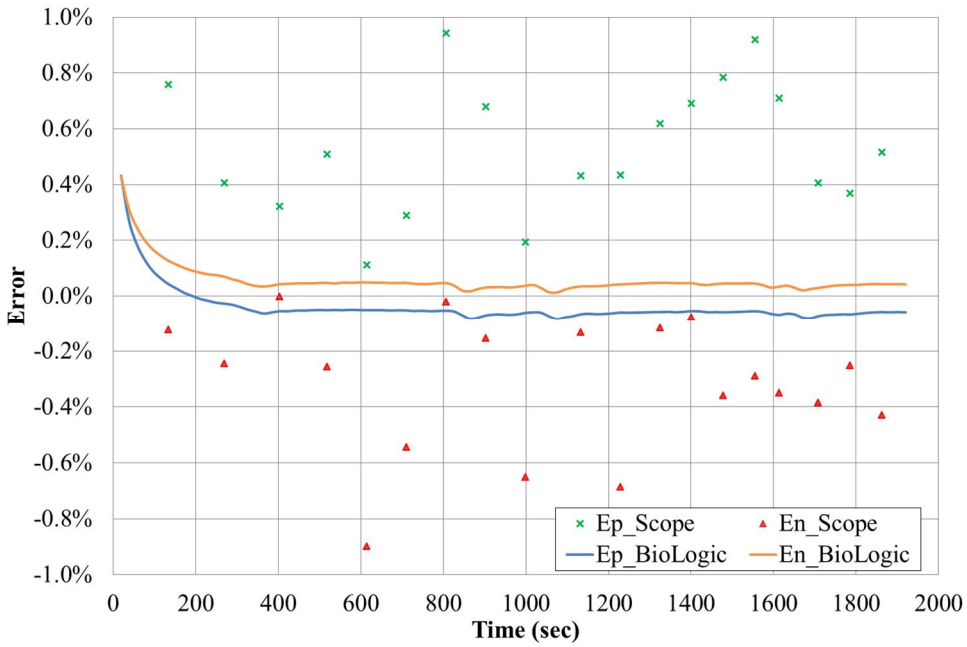


Figure C.5 The error between the calculated and the measured dissipated energy

From Figure C.5, the Bio-Logic platform has better accuracy in the energy measurement than the LeCroy® platform since the error is almost symmetrical and smaller. The average error is calculated for both platforms and is shown in Table C.4. The energy measurement accuracy of the LeCroy® platform is acceptable (< 1%).

Table C.4 Comparison the Bio-Logic and the LeCroy® measurement error during the positive and negative current conditions between

Average error	Bio-Logic	LeCroy®
positive current	< 0.1%	0.5%
negative current	< 0.1%	0.3%

Appendix D : Gauss-Newton Algorithm for the SC model Identification

The Gauss-Newton method is usually used to minimize a sum of squared function values. In this work, this method is employed to achieve the least square error fitting between the SC model and its actual impedance. The algorithm minimizes the error by iteration. In order to compromise with the algorithm complexity, the positive SC impedance information (i.e. the SC inductive behavior) is calculated separately without using the Gauss-Newton algorithm as presented in the fitting process in Section 2.5.1.1. Therefore, only the SC porous impedance, Z_{Pore}, is applied to the Gauss-Newton algorithm.

D.1 Using Gauss-Newton with Model IV

The Gauss-Newton method is applied to determine C_S and τ parameters, which represent the Z_{Pore} characteristic of model IV as shown in Figure D.1.

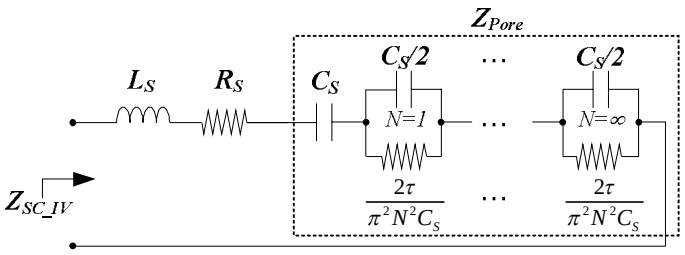


Figure D.1 Model IV: The *N* series-parallel RC model with an added inductance

From Figure D.1, Z_{Pore} can be described as:

$$Z_{Pore} = \frac{1}{j\omega C_S} + \sum_{i=1}^{N} Z_N \tag{D.1}$$

where $Z_N = \dfrac{\dfrac{2\tau}{\pi^2 N^2 C_S}}{1 + j\omega \dfrac{2\tau}{\pi^2 N^2 C_S} C_N}$

Substitute $\tau_{New} = \dfrac{2\tau}{\pi^2}$, Z_N becomes

$$Z_N = \frac{\dfrac{\tau_{New}}{N^2 C_S}}{1 + j\omega \dfrac{\tau_{New}}{N^2 C_S} C_N}$$

Since $C_N = \dfrac{C_S}{2}$, Z_N becomes

$$Z_N = \frac{2\tau_{New}}{2N^2 C_S + j\omega \tau_{New} C_S}$$

Multiply Z_N with $\dfrac{2N^2 C_S - j\omega \tau_{new} C_S}{2N^2 C_S - j\omega \tau_{new} C_S}$, then Z_N becomes

$$Z_N = \frac{2\tau_{New}\left(2N^2 C_S - j\omega \tau_{New} C_S\right)}{\left(4N^4 + \omega^2 \tau_{New}^2\right) C_S^2}$$

Let *den* = $\left(4N^4 + \omega^2 \tau_{New}^2\right)$, Z_N becomes

$$Z_N = \frac{4\tau_{New} N^2 - j2\omega \tau_{New}^2}{den C_S} \tag{D.2}$$

In the Gauss-Newton iteration algorithm, (D.3) to (D.5) are used, which output C_S and τ_{New} at the end of the process.

$$\begin{bmatrix} \tau_{New}(k+1) \\ C_S(k+1) \end{bmatrix} = \begin{bmatrix} \tau_{New}(k) \\ C_S(k) \end{bmatrix} + \alpha\Delta \tag{D.3}$$

$$\Delta = \left(J^T \times J\right)^{-1} \times J^T \times Error \tag{D.4}$$

$$Error = \begin{bmatrix} \mathrm{Re}(Z_{SC} - Z_{RL}) - \mathrm{Re}(Z_{Pore}) \\ \mathrm{Im}(Z_{SC} - Z_{RL}) - \mathrm{Im}(Z_{Pore}) \end{bmatrix} \tag{D.5}$$

where α is a learning factor, Δ is increment vector, J is a Jacobian matrix, Z_{SC} is the actual SC impedance and $Z_{RL} = j\omega L_S + R_S$. k and k+1 represent the current and the next iteration points.

Using (D.1) and (D.2) to construct J:

$$J = \begin{bmatrix} \mathrm{Re}\left(\frac{\partial Z_{Pore}}{\partial C_S}\right) & \mathrm{Re}\left(\frac{\partial Z_{Pore}}{\partial \tau_{New}}\right) \\ \mathrm{Im}\left(\frac{\partial Z_{Pore}}{\partial C_S}\right) & \mathrm{Im}\left(\frac{\partial Z_{Pore}}{\partial \tau_{New}}\right) \end{bmatrix} \tag{D.6}$$

Substitute (D.1) into (D.2) and perform a Jacobian derivative, $\frac{\partial Z_{Pore}}{\partial \tau_{New}}$ and $\frac{\partial Z_{Pore}}{\partial C_S}$, which results in

$$\frac{\partial Z_{Pore}}{\partial \tau_{New}} = \frac{4N^2 denC_S - 8N^2\tau_{New}^2\omega^2 C_S + j\left(4\omega^3\tau_{New}^3 C_S - 4\omega\tau_{New}C_S den\right)}{den^2 C_S^2} \tag{D.7}$$

$$\frac{\partial Z_{Pore}}{\partial C_S} = \frac{j}{\omega C_S^2} + \frac{-4\tau_{New}N^2 den + j2\omega\tau_{New}^2 den}{den^2 C_S^2} \tag{D.8}$$

Before start the iteration, the initial values of the fitted parameter is calculated first, so the initial values of C_S and τ_{New} are calculated from the lowest frequency information of the SC impedance. The initialized values are selected such that the iteration time is minimized. The output τ_{New} is converted back to τ before calculating R_N by $\tau = \frac{\tau_{New}\pi^2}{2}$.

D.2 Using Gauss-Newton with Model IV_2

In model IV_2, the RC parallel branch impedance, Z_{add}, is added to model IV as shown in Figure D.2. The Z_{add} can be described by (D.9).

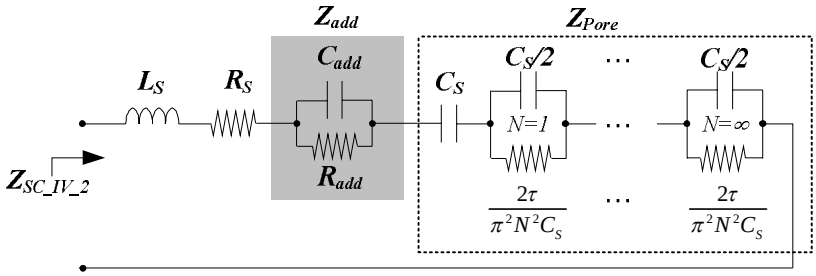


Figure D.2 Model IV_2: The *N* series-parallel RC model with an additional RC branch

$$Z_{add} = \frac{R_{add}}{1 + j\omega R_{add} C_{add}} \tag{D.9}$$

The Z_{add} is subtracted from the Z_{SC}. Then the iteration process is performed with (D.3), (D.4), (D.6) and (D.10) to output C_S and τ_{New}.

$$Error = \begin{bmatrix} \mathrm{Re}(Z_{SC} - Z_{RL} - Z_{add}) - \mathrm{Re}(Z_{Pore}) \\ \mathrm{Im}(Z_{SC} - Z_{RL} - Z_{add}) - \mathrm{Im}(Z_{Pore}) \end{bmatrix} \tag{D.10}$$

Appendix E : Modelling of Emulator System

In this section, the transfer function of the emulator system presented in Chapter 6 is derived. The transfer function is used in the current and voltage control design of the emulator. The emulator output filter comprises of three of two-phase InterCell transformers, a three-phase InterCell transformer and an output capacitor. The equivalent circuit of the filtering component is shown in Figure E.1.

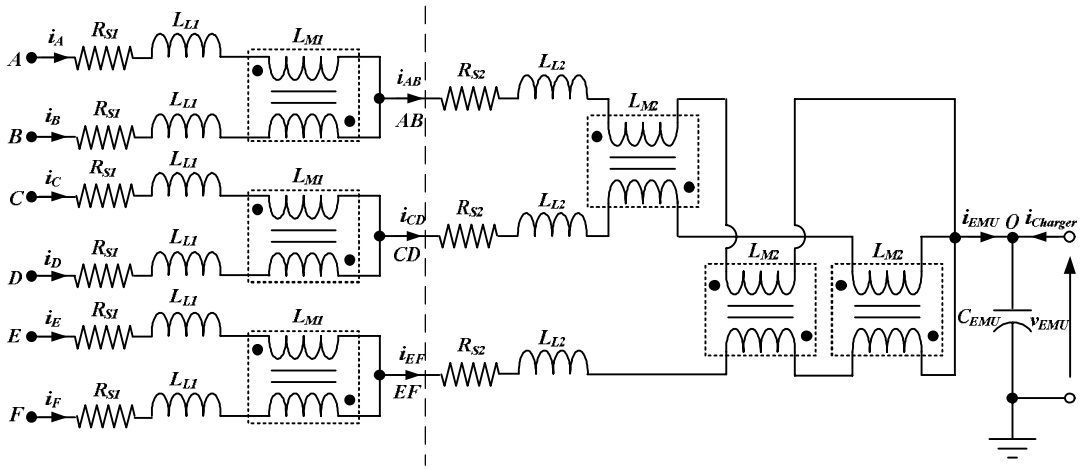


Figure E.1 An equivalent circuit of the six-channel emulator InterCell transformer with an output capacitor

From Figure E.1, i_A to i_F are the currents of channel A to F, i_{EMU} is the emulator output current, v_{EMU} is the emulator output voltage, R_S is the winding series resistance, L_L is the leakage inductance, L_M is the magnetizing inductance and C_{EMU} is the emulator output capacitor. It is noted that the subscribe number 1 and 2 represent parameters of the two-phase and the three-phase InterCell transformers. Based on KCL laws, the transfer function of each channel current and an output voltage can be written as:

$$v_A - v_{EMU} = L_{L2}\left(i'_A + i'_B\right) + R_{S2}(i_A + i_B) + L_{M2}(i'_A + i'_B - i'_C - i'_D) + L_{M2}(i'_A + i'_B - i'_E - i'_F) + L_{L1}i'_A + L_{M1}\left(i'_A - i'_B\right) + R_{S1}i_A \quad \text{(E.1)}$$

$$v_B - v_{EMU} = L_{L2}\left(i'_A + i'_B\right) + R_{S2}(i_A + i_B) + L_{M2}(i'_A + i'_B - i'_C - i'_D) + L_{M2}(i'_A + i'_B - i'_E - i'_F) + L_{L1}i'_B - L_{M1}\left(i'_A - i'_B\right) + R_{S1}i_B \quad \text{(E.2)}$$

$$v_C - v_{EMU} = L_{L2}\left(i'_C + i'_D\right) + R_{S2}(i_C + i_D) - L_{M2}(i'_A + i'_B - i'_C - i'_D) + L_{M2}(i'_C + i'_D - i'_E - i'_F) + L_{L1}i'_C + L_{M1}\left(i'_C - i'_D\right) + R_{S1}i_C \quad \text{(E.3)}$$

$$v_D - v_{EMU} = L_{L2}\left(i'_C + i'_D\right) + R_{S2}(i_C + i_D) - L_{M2}(i'_A + i'_B - i'_C - i'_D) + L_{M2}(i'_C + i'_D - i'_E - i'_F) + L_{L1}i'_D - L_{M1}\left(i'_C - i'_D\right) + R_{S1}i_D \quad \text{(E.4)}$$

$$v_E - v_{EMU} = L_{L2}\left(i'_E + i'_F\right) + R_{S2}(i_E + i_F) - L_{M2}(i'_A + i'_B - i'_E - i'_F) - L_{M2}(i'_C + i'_D - i'_E - i'_F) + L_{L1}i'_E + L_{M1}\left(i'_E - i'_F\right) + R_{S1}i_E \quad \text{(E.5)}$$

$$v_F - v_{EMU} = L_{L2}\left(i'_E + i'_F\right) + R_{S2}(i_E + i_F) - L_{M2}(i'_A + i'_B - i'_E - i'_F) - L_{M2}(i'_C + i'_D - i'_E - i'_F) + L_{L1}i'_F - L_{M1}\left(i'_E - i'_F\right) + R_{S1}i_F \quad \text{(E.6)}$$

$$v'_{EMU} = \frac{\left(i_A + i_B + i_C + i_D + i_E + i_F\right)}{C_{EMU}} \quad \text{(E.7)}$$

where v_A to v_F are the applied voltages of the interleaved channel A to F, i'_A, i'_B, i'_C, i'_D, i'_E, i'_F and v'_{EMU} represent derivative terms of i_A, i_B, i_C, i_D, i_E, i_F and v_{EMU}. MATLAB® Symbolic toolbox is used to solve (E.1) to (E.7) for i'_A, i'_B, i'_C, i'_D, i'_E, i'_F and v'_{EMU} and re-arrange them in the state-space form:

$$[x'] = [A][x] + [B][u] \quad \text{(E.8)}$$

where

$$[x'] = \begin{bmatrix} i'_A & i'_B & i'_C & i'_D & i'_E & i'_F & v'_{EMU} \end{bmatrix}^T, [x] = \begin{bmatrix} i_A & i_B & i_C & i_D & i_E & i_F & v_{EMU} \end{bmatrix}^T,$$

$$[x] = \begin{bmatrix} v_A & v_B & v_C & v_D & v_E & v_F \end{bmatrix}^T,$$

$$[A]=(-1)\begin{bmatrix} X_1 & X_2 & O_1 & O_1 & O_1 & O_1 & \frac{1}{\sum L_L} \\ X_2 & X_1 & O_1 & O_1 & O_1 & O_1 & \frac{1}{\sum L_L} \\ O_1 & O_1 & X_1 & X_2 & O_1 & O_1 & \frac{1}{\sum L_L} \\ O_1 & O_1 & X_2 & X_1 & O_1 & O_1 & \frac{1}{\sum L_L} \\ O_1 & O_1 & O_1 & O_1 & X_1 & X_2 & \frac{1}{\sum L_L} \\ O_1 & O_1 & O_1 & O_1 & X_2 & X_1 & \frac{1}{\sum L_L} \\ -\frac{1}{C_{EMU}} & -\frac{1}{C_{EMU}} & -\frac{1}{C_{EMU}} & -\frac{1}{C_{EMU}} & -\frac{1}{C_{EMU}} & -\frac{1}{C_{EMU}} & 0 \end{bmatrix} \text{ and}$$

$$[B]=\begin{bmatrix} X_3 & X_4 & O_2 & O_2 & O_2 & O_2 \\ X_4 & X_3 & O_2 & O_2 & O_2 & O_2 \\ O_2 & O_2 & X_3 & X_4 & O_2 & O_2 \\ O_2 & O_2 & X_4 & X_3 & O_2 & O_2 \\ O_2 & O_2 & O_2 & O_2 & X_3 & X_4 \\ O_2 & O_2 & O_2 & O_2 & X_4 & X_3 \\ 0 & 0 & 0 & 0 & 0 & 0 \end{bmatrix}$$

$$X_1=\frac{\sum R_S}{6\sum L_L}+\frac{R_{S1}}{2\left(L_{L1}+2L_{M1}\right)}+\frac{\sum R_S}{3\left(L_{L1}+2L_{L2}+6L_{M2}\right)}$$

$$X_2=\frac{\sum R_S}{6\sum L_L}-\frac{R_{S1}}{2\left(L_{L1}+2L_{M1}\right)}+\frac{\sum R_S}{3\left(L_{L1}+2L_{L2}+6L_{M2}\right)}$$

$$X_3=\frac{1}{6\sum L_L}+\frac{1}{2\left(L_{L1}+2L_{M1}\right)}+\frac{1}{3\left(L_{L1}+2L_{L2}+6L_{M2}\right)}$$

$$X_4=\frac{1}{6\sum L_L}-\frac{1}{2\left(L_{L1}+2L_{M1}\right)}+\frac{1}{3\left(L_{L1}+2L_{L2}+6L_{M2}\right)}$$

$$O_1=\frac{\sum R_S}{6\sum L_L}-\frac{\sum R_S}{6\left(L_{L1}+2L_{L2}+6L_{M2}\right)}$$

$$O_2=\frac{1}{6\sum L_L}-\frac{1}{6\left(L_{L1}+2L_{L2}+6L_{M2}\right)}$$

$\sum R_S = R_{S1} + 2R_{S2}$ and $\sum L_L = L_{L1} + 2L_{L2}$

From Figure E.1, the voltage inputs of channel *A* to *F*, v_A to v_F, can be expressed as $d_A V_{DC}$ to $d_F V_{DC}$ where d_A *to* d_F are the switching duty cycles of channel A to F and V_{DC} is the voltage of a constant voltage source. Since the i_{EMU} is divided into 6 channels equally, *d* of all channels is the same at steady-state. Performing linearization on (E.8) and the small signal model of the system is:

$$\left[\tilde{x}'\right] = \left[A\right]\left[\tilde{x}\right] + V_{DC}\left[B\right]\left[\tilde{d}\right]^T \tag{E.9}$$

where $\left[\tilde{d}\right] = \left[\tilde{d}_A \quad \tilde{d}_B \quad \tilde{d}_C \quad \tilde{d}_D \quad \tilde{d}_E \quad \tilde{d}_F\right]$.

Since the system leakage inductances are dictating to the dynamic of the system common state variables (emulator voltage and current), the emulator common transfer function is used as a plant model to simplify the current controller design. The simplified transfer function in s-domain of the plant model is reduced to:

$$\frac{I_{EMU}}{V_{CH}} = \frac{C_{EMU} s}{C_{EMU} \sum L_L s^2 + C_{EMU} \sum R_S + 6}$$

$$\frac{I_{CH}}{V_{CH}} = \frac{1}{6} \frac{C_{EMU} s}{C_{EMU} \sum L_L s^2 + C_{EMU} \sum R_S + 6} \tag{E.10}$$

where I_{EMU} is the emulator output current, I_{CH} and V_{CH} are the current and the applied voltage of single interleaved channel.

Since I_{EMU} is equal to $6I_{CH}$, from (E.7) the output current-to-voltage transfer function is:

$$\frac{V_{EMU}}{I_{CH}} = \frac{6}{sC_{EMU}} \tag{E.11}$$

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