The University of Nottingham
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Investigation of Structural, Electrical and Optical Properties of Advanced Wide Bandgap Semiconductor Materials And Devices

by

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M. Sc (Applied Physics)

Thesis submitted to the University of Nottingham

for the degree of Doctor of Philosophy

June 2023

ABSTRACT

This thesis reports an investigation of deep level defects in p-i-n $Al_{0.6}Ga_{0.4}N/Al_{0.5}Ga_{0.5}N$ multi quantum wells (MQWs) based deep ultraviolet light emitting diodes (DUV-LED), $In_{0.09}Ga_{0.91}N/GaN$ MQWs based ultraviolet photodetector (UV-PD) and NiO/β-Ga_2O_3 heterojunction diodes. Firstly, different analytical techniques were used to examine the structural, electrical, and optical properties of AlGaN-based on DUV LEDs with 50% Al content before and after electrical stress process at 100 mA over 150 hours. The cathodoluminescence (CL) intensity of the DUV LED after stress process decreased. Current-voltage (I-V) characteristics demonstrated that leakage current and ideality factor increased from 4.18×10^{-9} cm^{-3} to 4.50×10^{-9} A and 4.96 to 6.14, respectively ,following electric current stress. Capacitance-voltage (C-V) measurements indicated that the stress process causes the charge carriers to be redistributed in the active region of the MQWs. The Deep Level Transient Spectroscopy (DLTS) measurements at reverse bias V_R=-0.5V revealed two and one electron traps with higher concentration in fresh (not subjected to the electrical current process) and stressed (subjected to the electrical current process) LEDs, respectively. Scanning Transmission Electron Microscopy (STEM) images and Energy-Dispersive X-ray (EDX) Spectroscopy mapping showed that there are not many dislocations or defects in the MQWs before electrical stress is applied. As a result of the stress, two dislocation lines appeared and extended throughout the quantum wells.

The InGaN/GaN MQWs UV-PDs, which consisted of a thick passivation layer of Al_2O_3, were subjected to high electrical current stress of 200 mA over 340 hours

and investigated by employing different combined optical and electrical measurements. As a consequence of electrical stress, it was noticed that the Electroluminescence (EL) intensity decreased substantially (~ 48 %), suggesting that most of the charge carriers are captured by the newly induced defects in the active region. In addition, the parasitic current leakage paths increased significantly which in turn reduced the photocurrent generation process largely. Furthermore, within the temperature range of 100 K – 440 K, the values of the ideality factor and junction potential are found to be always higher and lower in treated PDs, respectively. This indicates the presence of generation recombination centres caused by defects. Two trap levels are identified in treated PDs via Laplace DLTS analysis. The obtained results indicate that degradation is mainly associated with the newly generated defects, mostly Mg-related shallow acceptors, including MgGa and Mg-H_2 complexes, which can form acceptor levels as a result of the breaking of Mg-H chemical complexes due to high heating levels during the stress treatment.

The effect of Rapid Thermal Annealing (RTA) at 225 ℃ in N_2 atmosphere for 15 minutes on the electrical and optical properties of NiO/β-Ga_2O_3 heterojunction diodes was investigated using Photoluminescence (PL) and micro-Raman spectroscopy, C-V, I-V, DLTS, L-DLTS, techniques, and SILVACO-TCAD numerical simulator. Micro-Raman results revealed no frequency shift, no linewidth variation, or relative intensity change. After RTA, the PL intensity was five times greater than that of the fresh sample as a result of an increase in the density of gallium and oxygen vacancies (V_{Ga} + V_O) in the annealed samples. A comparison of the I-V characteristics of annealed and fresh samples revealed that the ideality factor decreased from 2.33 to 1.74 and the junction potential increased from 0.68 eV to 0.76 eV after the thermal annealing process. DLTS measurements

showed that the number of electrically active traps differed between the two samples. In particular, three and one electron traps were detected in fresh and annealed samples, respectively. Additionally, the RTA process reduced the concentration of trap E_3 of more than two times. SILVACO-TCAD simulator achieved a fairly good agreement between simulation and measurements by considering a surface NiO acceptor density of about 1×10^{19} cm^{-3} and E_2 trap depth into the surface of β-Ga_2O_3 layer of about 0.220 μm. The results of the investigation of the NiO/β-Ga_2O_3 heterojunction diodes indicate that RTA improves their performance significantly. Specifically, RTA enhances the PL intensity by increasing gallium and oxygen vacancies, reduces the reverse leakage current and trap concentrations. These results confirm that RTA plays a critical role in improving the performance and functionality of NiO/β-Ga_2O_3 based devices.

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   Journal of Materials Today Electronics 4, 100042 (2023)

CONFERENCE PRESENTATIONS

ORAL TALK

- "Investigation of Electrically Active Defects in NiO/Ga_2O_3 p-n diode by Using Deep Level Transient Spectroscopy"
  Global Conference on Materials Science and engineering (GCME-2022)
  Valencia, Spain, Novamber 7^{th} -8^{th} (2022)

POSTER PRESENTATIONS

- "Investigation of Electrically Active Defects in InGaN/GaN Multi Quantum Wells Grown on Different Substrates by Using Deep Level Transient Spectroscopy"
  The UK Nitrides Consortium (UKNC) winter conference.
  United kingdom, January 7^{th} -8^{th} (2021)

- "Investigation on the effect of stress on electrically active defects in AlGaN multi quantum well"
  31st International Conference on Defects in Semiconductors.
  Oslo, Norway, July 26^{th} -30^{th} (2021)

ACKNOWLEDGEMENTS

First and foremost, I wish to express my gratitude to Allah Almighty for providing me with the strength, knowledge, and ability to complete this thesis successfully.

It has been an honor and a pleasure to express my gratitude to those who supported this thesis.

It is my pleasure to express my sincere gratitude to my supervisor, **Prof. Mohamed Henini**, for the continuous support that he has given me during my PhD studies and research, as well as for his patience, motivation, enthusiasm, and immense knowledge. I would like to thank him for his guidance and advice throughout the research and writing this thesis. In addition, I would like to express my deep gratitude to him for providing me with numerous opportunities during my PhD, including participating at international conferences where I presented my work and explored collaborations with a variety of groups from around the world independently and confidently.

It is my pleasure to thank **Taibah University** in Saudi Arabia for their financial support of my PhD program.

I would like to thank all my collaborators, namely, Prof. **Yara Gobato** (Federal University of São Carlos, Brazil) for PL and Raman characterization and for useful discussions, Dr. **Helder Galeti** (Federal University of São Carlos, Brazil) for his helpful support to learn PL technique, group of Dr **Lixia Zhao** (the Institute of Semiconductors, Chinese Academy of Sciences, Beijing, China) for providing p-i-n $Al_{0.6}Ga_{0.4}N/Al_{0.5}Ga_{0.5}N$ MQWs based DUV-LED devices, optical and structural

characterization, the group of **Dr Pradip Dalapati** (Nagoya Institute of Technology, Nagoya, Japan) for providing $In_{0.01}Ga_{0.99}N$/GaN MQWs based UV-PDs, optical and photovoltaic characterization, the group of **Dr Yuhao Zhang** (Center for Power Electronics Systems, Virginia Polytechnic Institute and State University, Blacksburg) for providing NiO/β-Ga_2O_3 heterojunction diodes, both **Dr Nouredine Sengouga** and **Dr Labed Madani (**Sejong University, 209 Neungdong-ro, Gwangjin-gu) for support SILVACO-TCAD simulator results and for useful discussions. My specials go also to all other collaborators named in the publications list.

I would also like to thank **Mr. Jasbinder Chauhan** for his assistance in processing the devices investigated in this thesis. Also, I would like to express my gratitude to all of my colleagues in the School of Physics for their support and friendship during my PhD studies.

I would like to present my deepest gratitude to my deceased soulful father **Ibrahim**, who passed away in 2018 and my beloved mother **Atoh** for their great role in my life and academic journey. Their love, guidance, and sacrifices have been the driving force behind my success, and I am forever grateful for their unwavering support. I am truly blessed to have such amazing parents who have sacrificed so much to provide me with the opportunities and resources to pursue my dreams. Thank you from the bottom of my heart. Also, I would like to express my heartfelt gratitude to my wife **Tahani** and daughter **Malk** for their unconditional love and support throughout my academic journey. Their unwavering belief in me has been a constant source of motivation and inspiration. Without their constant encouragement and understanding, I would not have been able to achieve the

success I have. They have been my biggest motivators and I am forever thankful for their unwavering support. Also, I would to thank my brothers **Khalil** and **Fawaz** for their support and for being truly brothers when needed. Many thanks as well for my sisters **Galliah**, **Fayzah**, **Fawzia**, **Siham** and **Amirah**. Without their precious support, it would not be possible to conduct this research.

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CHAPTER 1 : INTRODUCTION

Chapter 1 will give a brief introduction to the semiconductor materials and devices investigated as well as the motivations and structure of the thesis.

1.1 INTRODUCTION

In the last few years, several improvements have been made in the silicon material technology along with the design of new device structures. Currently, most of the high power systems (such as bipolar p-i-n diodes and MOSFET) are based on silicon technology. These Si-based systems, however, are approaching their theoretical limits of device performance [1]. By adopting alternative materials that exhibit enhanced switching performance, higher voltage capabilities, and greater power density, it is possible to improve the high power system significantly [2]. Thus, it becomes necessary to consider other semiconducting materials in order to improve device performance further, especially in the case of unipolar high-voltage power devices. Wide bandgap (WBG) semiconductors are an attractive alternative because they have larger bandgaps (> 2 eV) than conventional elemental semiconductors like silicon (1.12 eV) [3], and several inherent material advantages including high thermal conductivity, high breakdown voltage and comparable carrier mobility. Despite having a higher energy requirement, an excited electron is still capable of jumping from the valence band into the conduction band. There are various semiconductors with wide bandgap including III-Nitride compound semiconductors (such as GaN, $In_{(1-x)}Ga_xN$ and $Al_{(1-x)}Ga_xN$), Gallium Oxide (Ga_2O_3) and Nickel Oxide (NiO) which are also capable to operate at higher temperatures and frequencies than silicon-based technologies [4].

The wide-bandgap III-nitride semiconductors, such as $Al_{(1-x)}Ga_xN$ and GaN, have attracted tremendous attention due to their successful applications in optoelectronics, in particular visible - UV light-emitting diodes (LEDs), laser diodes (LDs), intersubband transition (ISBT)-based emitters and photodetectors (PD) [5], photovoltaics [6], nonlinear optics [7], and power electronics, including high electron mobility transistors (HEMTs) [8], p-n diodes [9], and Schottky barrier diodes (SBDs) [10].

1.1.1 Deep Ultraviolet Light Emitting Diodes (DUV LEDs)

One of the most important applications of wide-bandgap III-nitride semiconductors is deep ultraviolet (DUV) light sources, such as LEDs, with emitting wavelengths ranging from 220 nm to 350 nm. Over the past decade, considerable research has been devoted into the development of group III-nitrides-based DUV optoelectronics and recently, due to improvements in the crystalline quality of AlN and high Al-molar fraction AlGaN layers, and the optimization of p-type doping in AlGaN and LED structure design, the External Quantum Efficiency (EQE) and output power of AlGaN-based DUV LEDs have increased significantly. An EQE of over 3% and an output power of over 1 mW were reported in 2010 for flip-chip DUV LEDs with emission wavelengths between 255 nm and 280 nm [11]. In 2011, It was reported that a high Internal Quantum Efficiency (IQE) near 70% and EQE of 1.3% were achieved at 100 mA continuous wave (CW) current injection and emission wavelength of 260 nm using pseudomorphic UV LEDs grown on AlN substrates [12]. The maximum EQE of 10.4% and IQE of 60% for 278 nm DUV LEDs at 20 mA CW injection with a power output of 9.3 mW was achieved by

migration-enhanced metal organic chemical vapor deposition in order to reduce threading dislocations (TDs) and by utilizing a transparent p-type conduction layer, UV-reflecting Ohmic contacts, and an optimized chip encapsulation process [13]. Pandey et al. have reported EQE values of 11% for AlGaN/GaN/AlGaN tunnel junction LEDs at 265 nm emission wavelength [14]. A recent study of DUV LEDs based on AlGaN multi-quantum wells (MQWs) has achieved a maximum EQE of 20.3% to date. However, as compared with the excellent performance of group III-nitride based LEDs operating in the near UV [15] and blue [16] regions, the efficiency of DUV LEDs is still rather modest. The need to improve further EQE of DUV LEDs is crucial. It is important to note that EQE is dependent on both IQE and light extraction efficiency (LEE). The high IQE of InAlGaN MQWs can reach ~80% by reducing the densities of threading dislocations [17]and defects. Therefore, the deep level defects are a major concern.

1.1.2 Ultraviolet Photodetectors (UV PDs)

The UV PD is another device based on III-Nitride. In 1974, Pankove and Berkeyheiser began investigating the photoconductive properties of GaN [18]. During the 1990s, Khan et al. developed a GaN-based UV PD grown by metal-organic chemical vapor deposition (MOCVD) technique [19]. In the years that have followed, several teams have worked on exploring and developing a variety of photodetector structures, such as p-n and p-i-n junctions. InGaN films, which have been used in PD based p-i-n structures, have shown at zero-bias (a self-powered photoresponse) response values of 0.037 A/W at 426 nm, corresponding to an IQE of 15.5% [20]. Another study of $In_{(1-x)}Ga_xN$ based PD with an In-content of 11% has demonstrated of UV detection in the range 350-400 nm. It was found that the

highest spectral responsivity was 0.206 A/W at wavelength of 380 nm and EQE was about 67% with UV/visible rejection ratio of 10^3 [21]. In general, PDs based on $In_{(1-x)}Ga_xN$ alloys with $x<0.1$ show that the localized states and deep-level traps associated with the surface defects cause a persistent photoconductive effect, which results in unstable and slow photoresponses [22]. To overcome the technological limitations imposed by InGaN thin films, many groups used InGaN/GaN MQWs [23-25]. These MQWs structures offer impressive benefits like a lower noise level [23] and a more abrupt wavelength response cut-off [24]. Noise level refers to the amount of unwanted electrical fluctuations present in the output of photodetectors. According to Rivera et al., Schottky-type PDs have been demonstrated using InGaN/GaN MQWs where the In content is less than 14%. The devices showed a response of 1 A/W for different In composition and bias voltages as well as a rejection ratio of more than 10^4 between UV and visible light [24]. p-n junctions were also fabricated using MQWs. InGaN/GaN MQWs p-n junction PDs with semi-transparent Ni/Au electrodes were developed by Chiou et al [26, 27]. The device displayed a breakdown voltage of - 20 V and a UV-visible rejection ratio of more than 10^5. The maximum responsivity was 1.76 A/W at -3 V at around 380 nm. In terms of peak response wavelength, it ranged between 416 nm and 466 nm. However, the response decreased to 0.0035 A/W at 466 nm due to a degrading quality resulting from the increase of In content. By using 15-pair $In_{0.12}Ga_{0.88}N$ MQWs in a p-i-n structure, PDs fabricated using a typical LED epitaxial structure and surface texturing by using electron beam evaporation and selectively dry etching [28], achieved a peak responsivity of 0.24 A/W at 388 nm under a reverse bias voltage of -3 V with EQE of 78%. However, a recent study investigated the effects of In contents in $In_{(1-x)}Ga_xN$ MQW p-i-n PDs on the responsivity. It was

found that for In contents of 4.6%, 6.8%, and 8.8%, the values of responsivity increased from 0.175 A/W, 0.21 A/W, and 0.25 A/W, respectively. PDs with the highest In content of 8.8% have relatively superior performance compared to others due to its higher values of responsivity (0.25 A/W), detectivity, increase of peak responsivity with applied bias and superior light power-dependent photocurrent characteristics [29]. According to recent numerical simulation research, the maximum responsivity is 0.265 A/W at 380 nm under a reverse bias of -2 V for a 15 periods of $In_{0.1}Ga_{0.9}N$/GaN MQWs p-i-n PDs [30]. There are several reasons for the slow development of UV PDs due for example to the difficulties in reducing the threading dislocations [31] and the existence of highly sensitive defect states in the InGaN/GaN [24] interface, which can adversely affect their performance. Therefore, one of the most important factors to consider is the deep level defects present in these structures.

1.1.3 Ga_2O_3 Material

Ga_2O_3 is another WBG semiconductor material and belongs to the Transparent Conducting Oxides (TCOs) family. This material is known as an n-type semiconductor with relatively wide bandgap of ~4.6-4.9 eV [32]. Additionally, the high electron mobility and high breakdown voltage of Ga_2O_3 make it attractive for applications in high-power electronics [33], beyond the capabilities of current GaN and SiC platforms. Furthermore, Ga_2O_3 has been widely used in a variety of fields because of its unique properties in optics, photoelectric conversion, and electrical fields. These include UV detection [34], photocatalysis [35], flat panel displays [36], UV filters [37], gas sensors [38], and optoelectronic devices [39]. In addition Ga_2O_3 has been shown to be a promising material in biomedicine field where it can be applied as multifunctional drug carrier due to its penetration in the cell

membranes resulting in efficient luminescence emission [40, 41]. A wide range of p-type semiconductors, including Cu_2O [42], CuI [43] and NiO [44], were used to produce p-n heterojunctions with n-type β-Ga_2O_3.

1.1.4 NiO Material

NiO is amongst these high-performance p-type materials because it is easy to deposit by sputtering and to control the hole concentration [45]. The p-NiO/n-β-Ga_2O_3 heterojunction diodes (HJDs) have excellent voltage blocking capabilities, and a breakdown voltage of 2.41 kV has been demonstrated [46]. Despite the progress made on NiO/β-Ga_2O_3 HJDs, they still have serious leakage current problems and premature breakdown [44, 47]. In some cases, these problems may be a consequence of defects in β-Ga_2O_3 and at the NiO/β-Ga_2O_3 interface. The reverse leakage path in β-Ga_2O_3 SBDs appears to be caused by a deep energy level state below the conduction band (E_C) of E_C-0.72 eV [47]. Moreover, a defect with an activation energy of E_C-110 meV was found to affect power devices by increasing the ON-state resistance of unintentionally doped Ga_2O_3 and decreasing the breakdown voltage [48]. Defects with energy states within the bandgap of semiconductors have detrimental effects on the device's performance because they act as efficient recombination centres. A few studies have made efforts to reduce these defects. Rapid thermal annealing (RTA) has been used in order to improve film quality and reduce interface defects of NiO/β-Ga_2O_3 p-n HJDs [49]. A recent study compared a conventional single heterojunction p-NiO/β-Ga_2O_3 device containing single p-NiO layer with a new structure consisting of a vertical double-layered p-NiO/n-β-Ga_2O_3 heterojunction diodes consisting of two double-layer of p-type NiO films [50]. The results showed that the double-layered NiO device had

a significantly lower leakage current density and a higher rectification ratio than the conventional device. Additionally, this device exhibited excellent thermal stability and was able to operate effectively at high temperatures. Furthermore, the double-layered NiO design led to a reduction in hole concentration and an improvement in breakdown voltage. However, investigations of the effects of RTA on the optical properties and electrically active defects in NiO/β-Ga_2O_3 devices have not been reported yet. Therefore, a study of the effect of RTA is necessary.

In general, semiconductor structures possess a variety of different defects that alter their electrical and optical properties. It is possible to introduce defects into the semiconductor lattice intentionally, through doping, or unintentionally, during the fabrication and growth processes. As a consequence, many of these defects create deep levels within the bandgaps of semiconductor materials, which affect the performance of the devices. Therefore, it is crucial to assess and control the defects present in semiconductor materials and devices using a combination of techniques, namely, (i) deep level transient spectroscopy (DLTS), a powerful technique for investigating electrically active defects, (ii) luminescence and Raman spectroscopies for studying the optical properties (iii) photocurrent spectroscopy (PSC) for determining the photovoltaic properties, and transmission electron microscopy (TEM) and energy dispersive X-ray (EDX) spectroscopy for probing the structural properties.

1.2 Motivation

In semiconductor materials, deep defect states play an important role in the dynamics of carrier transport, electrical and optical properties, as well as the

performance of electronic and optoelectronic devices. Thus, the primary motivation of this thesis is to study the strutural, optical and electrical properties of p-i-n $Al_{0.6}Ga_{0.4}N/Al_{0.5}Ga_{0.5}N$ multi quantum wells (MQWs) based deep ultraviolet light emitting diode (DUV LED), p-i-n $In_{0.09}Ga_{0.91}N$/GaN MQWs UV-photodetectors and p-NiO/n-Ga_2O_3 heterojunction diodes.

The current-voltage (I-V), capacitance-voltage (C-V), DLTS, Laplace DLTS (L-DLTS), cathodoluminescence (CL), scanning transmission electron microscopy (STEM) and EDX characterisation techniques were employed to study the electrical, optical and structual properties of $Al_{o.6}Ga_{0.4}N/Al_{0.5}Ga_{0.5}N$ MQWs based DUV LED after electric current stress. The motivation of investigating the effect of electric current stress is to (i) identify the physical processes accountable for the degradation of DUV LEDs, (ii) understand how point defects and dislocations influence the device performance, (iii) determine the nature of these point defects and (iv) reduce the detrimental effects that hinder the novel development of such devices. Similarly, an investigation has been carried out on the effect of the electric current stress on the electrical and optical properties of InGaN/GaN MQWs UV-photodetectors by using I-V, C-V, DLTS, L-DLTS, electroluminescence (EL) and PSC characterisation techniques. This investigation was conducted to understand how defects penetrate different epilayers, their chemical nature, and their effects on devices. Moreover, I-V, C-V, DLTS, L-DLTS, Raman and Photoluminescence (PL) characterisation techniques, and Technology Computer-Aided Design (TCAD) simulator were employed to examine the effect of thermal annealing process on the electrical and optical properties of NiO/Ga_2O_3 heterojunction diodes (HJD). In addition, RTA process is investigated with the aim

to achieve a high performance NiO/β-Ga_2O_3 HJD and improve both bulk and heterointerface quality.

1.3 SCHEME OF THE THESIS

The struture of this thesis is organised as follows:

Chapter 1: discusses the research motivations and structure of the thesis.

Chapter 2: presents the fundamental concepts of semiconductors, crystal structure, energy bandgaps and the principles of heterostructure devices. This chapter also covers the properties of III-Nitride, Ga_2O_3 and NiO semiconductor materials, and describes the optical properties of semiconductors.

Chapter 3: provides details on the crystal defects as well as the theoretical background of carrier kinetics. The most well-known defects in III-Nitrides, Ga_2O_3 and NiO semiconductor materials are also discussed.

Chapter 4: describes the experimental techniques used in this thesis including DLTS, Laplace DLTS, luminescence (PL, EL, CL) and Raman spectroscopies, PSC and TEM. Furthermore, the hardware and software needed for implementing some of these methods are also presented.

Chapter 5: provides information on the samples studied in this thesis, as well as gives a brief description of the measurements setup.

Chapter 6: discusses the effect of electric current stress process on $Al_{0.6}Ga_{0.4}N/Al_{0.5}Ga_{0.5}N$ MQWs based DUV LEDs using I-V, C-V, DLTS, L-DLTS, CL, TEM and EDX.

Chapter 7: presents an investigation of the effects of electric current stress process on InGaN/GaN MQWs based UV photodetectors using I-V, C-V, DLTS, Laplace DLTS, EL and PSC techniques.

Chapter 8: reports on an investigation of the effects of thermal annealing process on the electrical and optical properties of NiO/Ga_2O_3 heterojunction diodes using I-V, C-V, DLTS, Laplace DLTS, Raman and PL measurement methods, and SILVACO-TCAD (Technology Computer-Aided Design) numerical simulator to model the heterojunction diodes.

Chapter 9: presents an overview of the research work done in this thesis and provides suggestions for future work.

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CHAPTER 2: FUNDAMENTAL CONCEPTS OF SEMICONDUCTORS

This chapter describes the basics and fundamental properties of semiconductors, such as doped and undoped semiconductors structures, crystal structures, density of states, natural energy bandgap, and temperature dependent energy gap. In addition, brief details of structural and electrical properties heterostructures materials such as lattice mismatch, atom size, atom electronegativity, and band alignment will be presented. The chapter will conclude by discussing the basic features of III nitride and oxide semiconductor materials, namely AlN, GaN, and InN, and NiO and Ga_2O_3. In addition, operation of LEDs and photodetector devices are covered.

2.1 Basic Of Semiconductors And Some Selected Devices

In the last few decades, semiconductors have become the core of modern electronic and optoelectronic industries since they are utilized to create numerous components and systems based on advanced electrical, optical and photovoltaic devices [1]. Among these devices are computers (memories, CPUs), optical storage media (lasers for CDs and DVDs), high efficiency solar cells, displays (thin film transistors, LEDs), projection (laser diodes), general lighting (LEDs) [2].

According to resistivity theory, a semiconductor is a material which has an electrical conductivity that lies between insulators and conductors. Normally, it is defined as a material with a resistivity ranging between 10^{-2} and 10^{9} Ω.cm.

Semiconductors can either be elementary, which are made of a single element, or compounds, which are made of two or more elements. The elementary semiconductor consists of only one element such as Si and Ge, which belong to the

group IV elements, but a compound semiconductor consists of two or more elements from the periodic table such as elements from the groups III and V, and II and VI. A compound semiconductor can be a binary compound if it consists of two elements, such as GaAs, and a ternary compound if it consists of three elements, such as InGaAs [3].

2.1.1 Undoped And Doped Semiconductors

Semiconductor materials can also be classified by the nature of their doping. As an example, a pure semiconductor is also known as an undoped semiconductor or an intrinsic semiconductor. Semiconductors of this type are generally composed of elementary (e.g. Si) or binary compound semiconductors (e.g. GaAs). Although intrinsic semiconductors are considered very pure, they still contain small amount of impurities that could not affect their electrical properties. It is also possible to define a pure semiconductor as one in which the number of electrons in the conduction band is equal to the number of holes in the valence band. At zero absolute temperature, an intrinsic semiconductor behaves as an insulator since the valence band is completely filled and the conduction band is completely empty, meaning that there are no charge carriers to contribute to the conductivity. On the other hand, in the presence of a thermal or photo excitation, the conductivity of this type of semiconductor will increase.

In semiconductor materials, doping refers to the addition of impurity atoms to a pure semiconductor. A semiconductor that is doped with other atoms is known as an extrinsic or impurity semiconductor. In particular, when an excess number of electrons are introduced by the dopant atoms, these create an n-type semiconductor. An example of an n-type doping is when a pentavalent impurity (group V in the

periodic table as shown in Figure 2.1) is added to pure Si. Si has four electrons in its outer electronic shell while arsenic has five electrons. Due to this, extra valence electrons are added since the four electrons in As are bound to the silicon atoms that surround them leaving only one electron for n type conduction. Similarly, when one of the trivalent impurities (Group III in the periodic table) such as boron is added to a pure Si atom, the three valence electrons of the boron atom form covalent bonds with the four surrounding Si atoms, leaving one hole free for p-type conduction. In a semiconductor with an excess number of holes created by the dopant atoms, the semiconductor is referred to as a p-type semiconductor [3, 4].

III	V	VI	VII
B Boron 10.81	**C** Carbon 12.01	**N** Nitrogen 14.01	**O** Oxygen 15.99
Al Aluminium 26.98	**Si** Silicon 28.09	**P** Phosphorus 30.97	**S** Sulfur 32.06
Ga Gallium 69.72	**Ge** Germanium 72.64	**As** Arsenic 74.92	**Se** Selenium 78.96
In Indium 114.8	**Sn** Tin 118.7	**Sb** Antimony 121.8	**Te** Tellurium 127.6
TI Thallium 204.38	**Pb** Lead 207.2	**Bi** Bismuth 209	**PO** Polonium 209
Nh Nihonium 248	**FI** Flerovium 289	**Mc** Moscovium 288	**LV** Livermorium 293

Figure 2.1:Periodic table for Group III to Group VII [5].

2.2 Crystal Structure And Properties

In semiconductor devices, the crystal structure plays an important role in their electrical and optical properties. In these materials the crystal structure is the arrangement of the atoms in the crystal.

2.2.1 Crystal Structure

The ideal crystal structures are formed by placing atoms or molecules in an arrangement to form a three-dimensional array structure without adding impurities either intentionally or unintentionally during the growth process. This crystal structure can be found in many forms. Figure 2.2 shows the three common examples of these structures, namely Simple Cubic (SC), Body-Centered Cubic (BCC), and Face-Centered Cubic (FCC). The simple or primitive cubic has atoms at each corner of the cubic. Furthermore, the BCC structure has an additional atom in the centre of cubic. For the FCC structure, additional atoms at each face of the cubic are present [6].

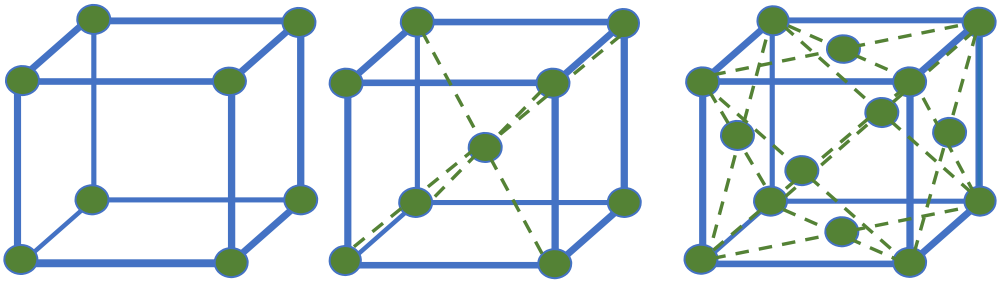

Figure 2.2: Crystal structure of (a) simple cubic lattice (b) body centred cubic lattice and (c) face centred cubic lattice.

In addition to the above structures, there are also common and essential crystal structure types in semiconductors such as diamond and zinc blende structures as shown in Figure 2.3. Both structures can be produced through the inter-pinning of

two FCC lattices offset by one-quarter diagonally. Furthermore, the atoms are arranged into a tetrahedron and each atom is covalently bonded to four neighbouring atoms. In contrast to diamond structure, zinc blende structure only has two different types of atoms (e.g. GaAs, GaSb, and InAs), while diamond structure has only one type of atom (e.g. Ge, Si, C) [3].

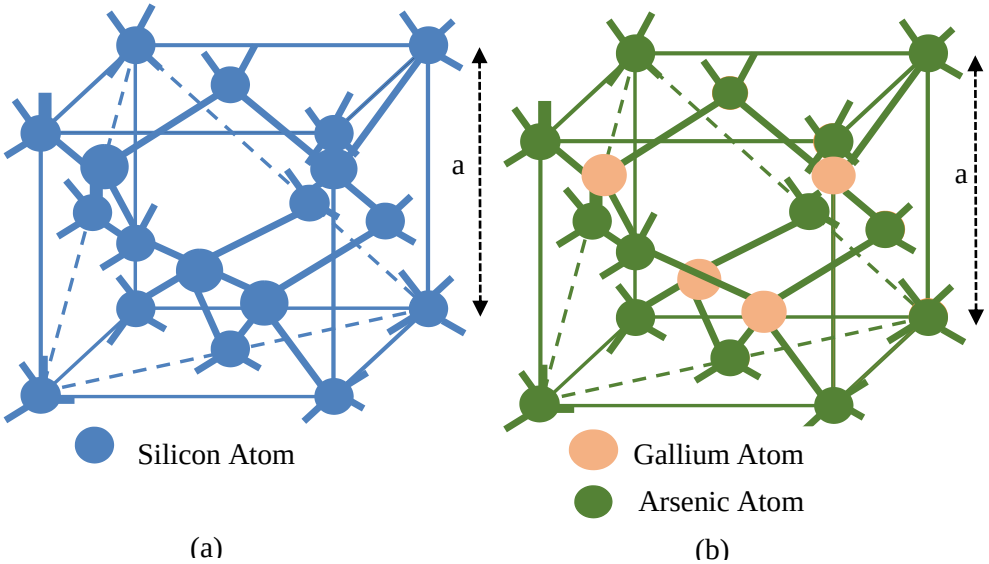

Figure 2.3: (a) Diamond structure for Si and (b) Zinc blende structure for GaAs [3] where a is the lattice constant.

The orientation of crystal planes has a significant role to play in the fabrication of semiconductor devices. In order to produce a device successfully, it is essential to know the plane on which it will be fabricated, as this can influence the device's electrical and optical properties. Typically, Miller indices are used to define the planes of a crystal. Miller indices (*hkl*) of a plane can be identified by finding the intercepts of the plane along the *x*, *y* and *z* directions, then taking the reciprocals of the intercepts and finally reducing them to the smallest integers [7]. Figure 2.4 shows the Miller indices of cubic crystals for low index planes such as (100), (110) and (111). Based on a set of parameters *h*, *k*, and *l*, a crystal surface's direction can be calculated as follows:

1. (hkl) for a plane that has intercepts at $\frac{1}{h}, \frac{1}{k}\ and\ \frac{1}{l}$ on the *x*, *y* and *z* axis, respectively.
2. $(\bar{h}kl)$ for a plane that intercepts the negative *x* axis.
3. $\{hkl\}$ for a full set of equivalent planes.
4. $[hkl]$ for a direction of a crystal such as [100] for the *x* axis.
5. $< hkl >$ for a full set of equivalent directions.

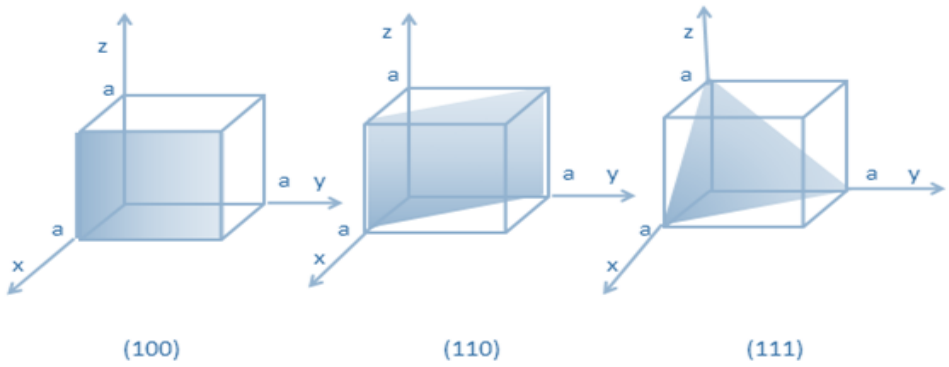

Figure 2.4: Miller indices of some planes in a cubic crystal.

The crystalline solid along the *x*, *y* and *z* directions can be easily described by using three primitive basis vectors (***a***, ***b*** and ***c***). A crystal structure will remain the same under any translation through a direct lattice vector (***R***), which is the sum of these primitive vectors as given by equation (2.1) [6].

$$\boldsymbol{R} = m\boldsymbol{a} + n\boldsymbol{b} + p\boldsymbol{c} \tag{2.1}$$

where *m*, *n* and *p* are integers.

The relation between the reciprocal lattice basis vectors ($\boldsymbol{a}^*$, $\boldsymbol{b}^*$, and $\boldsymbol{c}^*$) and the primitive vectors (***a***, ***b***, and ***c***) are given by the following equations [6].

$$\boldsymbol{a}^* = 2\pi \frac{\boldsymbol{b} \times \boldsymbol{c}}{\boldsymbol{a} \cdot (\boldsymbol{b} \times \boldsymbol{c})} \tag{2.2}$$

$$\boldsymbol{b}^* = 2\pi \frac{\boldsymbol{c} \times \boldsymbol{a}}{\boldsymbol{a} \cdot (\boldsymbol{b} \times \boldsymbol{c})} \tag{2.3}$$

$$\boldsymbol{c}^* = 2\pi \frac{\boldsymbol{a} \times \boldsymbol{b}}{\boldsymbol{a} \cdot (\boldsymbol{b} \times \boldsymbol{c})} \tag{2.4}$$

where $\boldsymbol{a}^* . \boldsymbol{a} = 2\pi$ and $\boldsymbol{a} . \boldsymbol{b}^* = 0$

It is important to note that the denominators in the above equations are equal since $\boldsymbol{a}.(\boldsymbol{b}\times\boldsymbol{c}) = \boldsymbol{b}.(\boldsymbol{c}\times\boldsymbol{a}) = \boldsymbol{c}.(\boldsymbol{a}\times\boldsymbol{b})$. They define the volume enclosed by these vectors (***a***, ***b***, *and* ***c***).

The reciprocal lattice vector, ***G*** can be defined by [6].

$$\boldsymbol{G} = h\boldsymbol{a}^* + k\boldsymbol{a}^* + l\boldsymbol{a}^* \tag{2.5}$$

where h, k and l are integers.

The relationship between reciprocal lattice (***G***) and direct lattice (***R***) is given by

$$\boldsymbol{G}.\boldsymbol{R} = 2\pi \text{ x integer.} \tag{2.6}$$

2.2.2 Energy Bandgap

The energy gap (E_g) or bandgap is defined in solid-state physics as the difference in energy between the top of the valence band (V_B) and the bottom of the conduction band (C_B). Based on their energy gap, materials are classified into three categories, namely insulators, semiconductors, and metals. Particularly in metals, E_g is equal to 0 eV. In semiconductors E_g ranges from 0.17 eV [e.g. Indium Antimonide (InSb)] to 6 eV [e.g. Aluminum Nitride (AlN)], while in insulators E_g is very high (e.g. E_g > 6 eV) [6] as seen in Figure 2.5. A semiconductor bandgap is represented by its energy-wave vector (*E*-*k*). The conduction band, as well as the valence band, near k = 0 have approximately parabolic shapes, and their energies are given by [8].

$$E_c = E_g + \frac{h^2k^2}{8\pi^2 m_e^*}, E_v = E_g - \frac{h^2k^2}{8\pi^2 m_h^*} \tag{2.7}$$

where h is the Planck's constant, m_h^* and m_e^* are the effective mass of hole and electron, respectively.

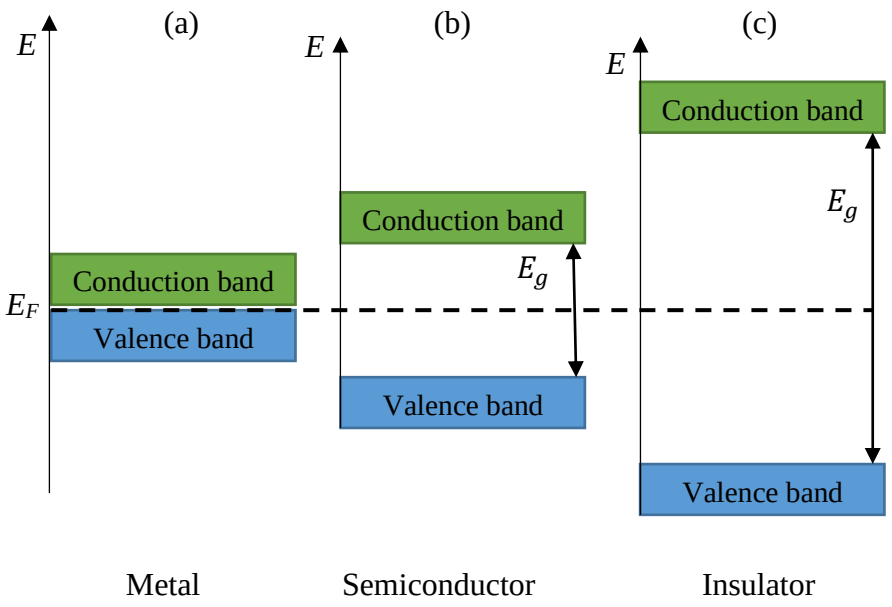

Figure 2.5: Schematic of the energy band diagrams of (a) metal, (b) intrinsic semiconductor, (c) insulator [9].

At a very low temperatures (at ~0 K), electrons are confined in the valence band because they are not able to overcome the bandgap to move to the conduction band due to insufficient energy. Thus, at such low temperatures, semiconductors behave as an insulating material [8].

2.2.3 Direct And Indirect Bandgap

Semiconductors can be grouped into direct and indirect bandgap semiconductors, based on the nature of their bandgaps. This classification is based on the location of the minimum energy of the conduction band and the maximum energy of the valence band with respect to the wave vector (k). When the minimum energy in the conduction band and the maximum energy in the valence band have the same k value, i.e. at $k = 0$ (Γ point), the semiconductor is called a direct bandgap semiconductor (for example, GaAs). On the other hand, for indirect bandgap

semiconductors (e.g. Si), the minimum of the conduction band and the maximum of the valence band are not at the same wave vector value [8]. Figure 2.6 illustrates the (*E-k*) relationship for the two most common semiconductors, GaAs and Si, respectively, with respect to their direct or indirect bandgaps [7].

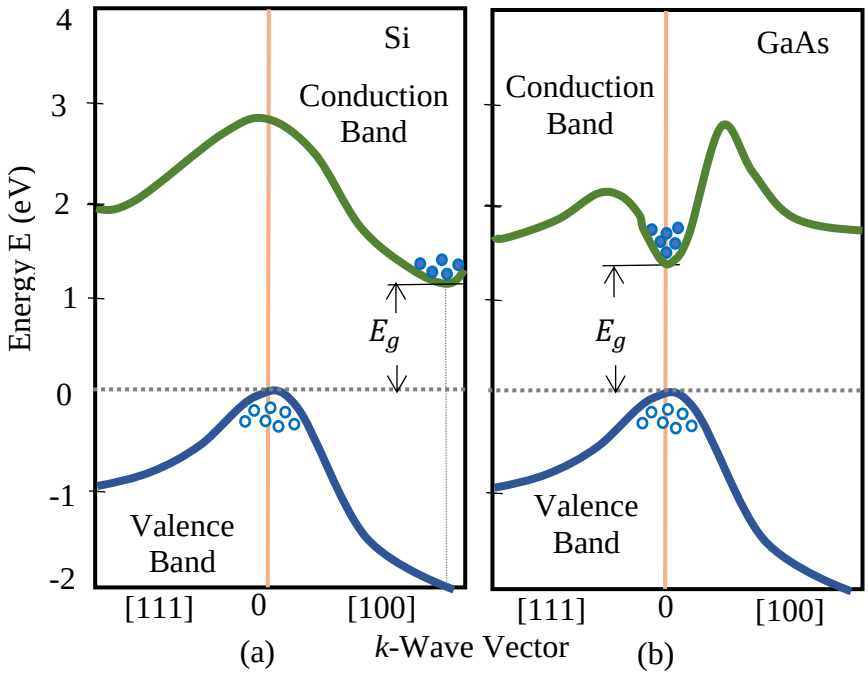

Figure 2.6: Energy-band structures of (a) Si that has an indirect band gap and (b) GaAs that has a direct band gap. The full and open circles represent the electrons and holes, respectively [3].

2.2.4 Effect Of Temperature On Energy Bandgap

The energy of the bandgap of semiconducting materials is temperature dependent. This dependence is related to the thermal vibrational energy, which results in an increase in the amplitude of the atomic vibrations due to the increase in temperature. When the temperature of a material increases, the kinetic energy of its atoms increases as well. This increase in the kinetic energy causes the amplitude of

atomic vibration to increase. The interatomic spacing is increased by this effect, which in turn reduces the electron potential experienced by the electrons in a semiconductor. The result is that the size of the energy gap is reduced. This behaviour can be better understood by taking GaAs and Si as examples as shown in Table 2.1. Si and GaAs have bandgap energies of 1.17 eV and 1.52 eV, respectively, at 0 K. At room temperature, these energies decrease to 1.12 eV and 1.42 eV, respectively, for Si and GaAs.

Table 2.1: temperature dependent energy bandgaps [7].

Semiconductor materials	Bandgap (E_g) at 0K	Bandgap (E_g) at 300K
GaAs	1.52 eV	1.42 eV
Si	1.17 eV	1.12 eV

The empirical relationship between the temperature (T) and the energy of bandgap (E_g) is formulated by Varshni law[10]

$$E_g(T) = E_g(0) - \frac{\alpha T^2}{T+\beta} \tag{2.8}$$

where $E_g(0)$ is the energy bandgap at 0 K, α and β represent the empirical parameters associated with the material e.g. α = 0.49 meV/K, and β = 655 K for silicon and α = 0.5 meV/K, and β = 220 K for GaAs

2.2.5 Quantum Confinement

Nanostructured materials possess unique electronic and optical properties compared to bulk materials. The unique properties of semiconductor nanomaterials are a result of a phenomenon known as the quantum size or quantum confinement

effect, which occurs when the system's size is smaller than the Bohr excitonic radius. Exciton Bohr radius can be defined as the separation distance between electron and hole [11].

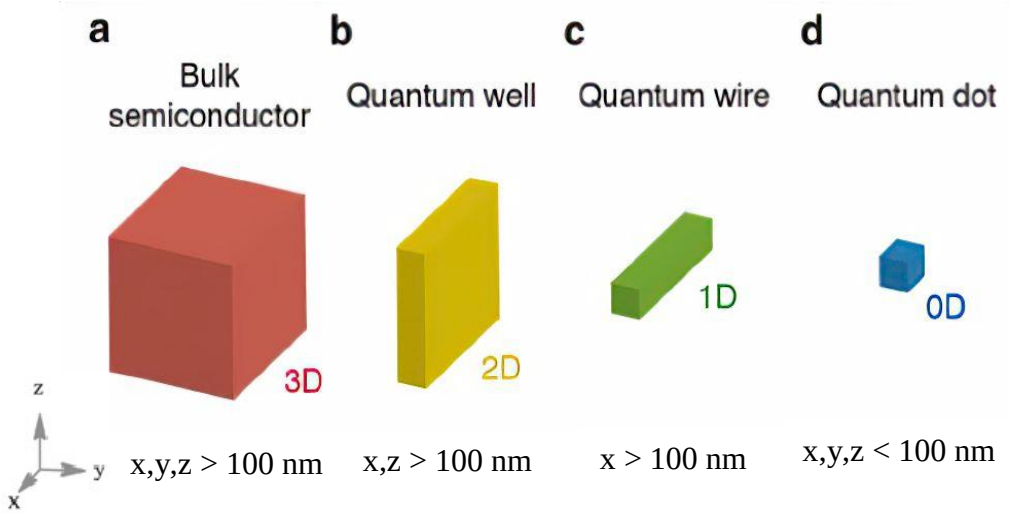

Figure 2.7: Schematic illustration of (a) a bulk semiconductor, (b) 2D quantum well, (c) 1D quantum wire, and (d) 0D quantum dot [12].

According to their dimensions, semiconductor material structures are grouped into four categories, namely, three-dimensional (3D) structures (bulk), two-dimensional (2D) structures (quantum wells), one-dimensional (1D) structures (quantum wires) and 0-dimensional (0D) structures (quantum dots) as shown in Figure 2.7. It is important to note that in bulk structures, particle motion is not quantized, therefore, particles can move freely in all dimensions. Quantum well structures involve the quantization of motion in one direction, leaving the particles free to move in the remaining two directions. Therefore, the continuous levels of energy found in bulk materials become discrete levels of energy within such layers. However, in quantum wires there is two-directional quantisation, resulting in only one direction of free movement. In quantum dot structures, quantisation occurs in all three

directions, i.e. the particle is confined in all three directions. Figure 2.8 illustrates a typical quantum well diagram, which is formed by growing a thin semiconductor layer between two layers of another semiconductor material with a larger band gap. GaAs/AlGaAs is an example of two materials that may be used to form a semiconductor quantum well, where the quantum well is formed in the thin GaAs layer sandwiched between two AlGaAs layers with a larger bandgap.

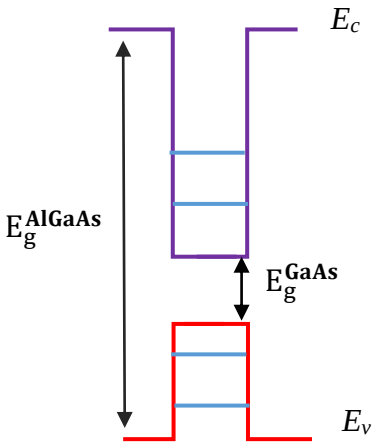

Figure 2.8: A typical diagram of a single quantum well. The blue lines represent the allowed energy levels for an electron and hole within the well.

2.2.6 Density Of States In Semiconductors

The density of states (DOS) is defined as the number of different states at a particular energy level that electrons or holes are allowed to occupy, i.e. carriers (electrons and holes) can occupy the following number of states per unit volume per unit energy. In a semiconductor, the distribution and concentration of carriers is crucial. Interactions between atoms in close proximity result in a splitting of quantized energy levels into a finite number of energy states [13].

Energy bands are created by electrons occupying all lower energy states available to them, which are in other words, valence and conduction bands. At 0 Kelvin, the

valence band is completely filled with electrons, while the electronic states in the conduction band are empty. The conduction and valence bands are separated by a bandgap, which is the range of energies where no allowed states can exist. During the conduction process, when electrons possess enough energy to overcome the bandgap, they are excited to the conduction band leaving vacancies (holes) in the valence band. These electrons tend to occupy available states in the conduction band. These allowed states at certain energy levels are defined as density of states. The density of states differs based on the degree of freedom of the carriers and their confinement. The degree of freedom of the carriers is dependent on the material structure as discussed in section 2.2.5.

Figure 2.9 illustrates the density of states for these materials as a function of energy. The density of states of a bulk material is proportional to the square root of energy, while it is a step-like function in the case of a 2D system (such as a quantum well). A 1D material such as a quantum wire has a density of states described by the function $(E)^{-1/2}$ while a 0D material (such as a quantum dot) has its density of states described by a delta function [14, 15].

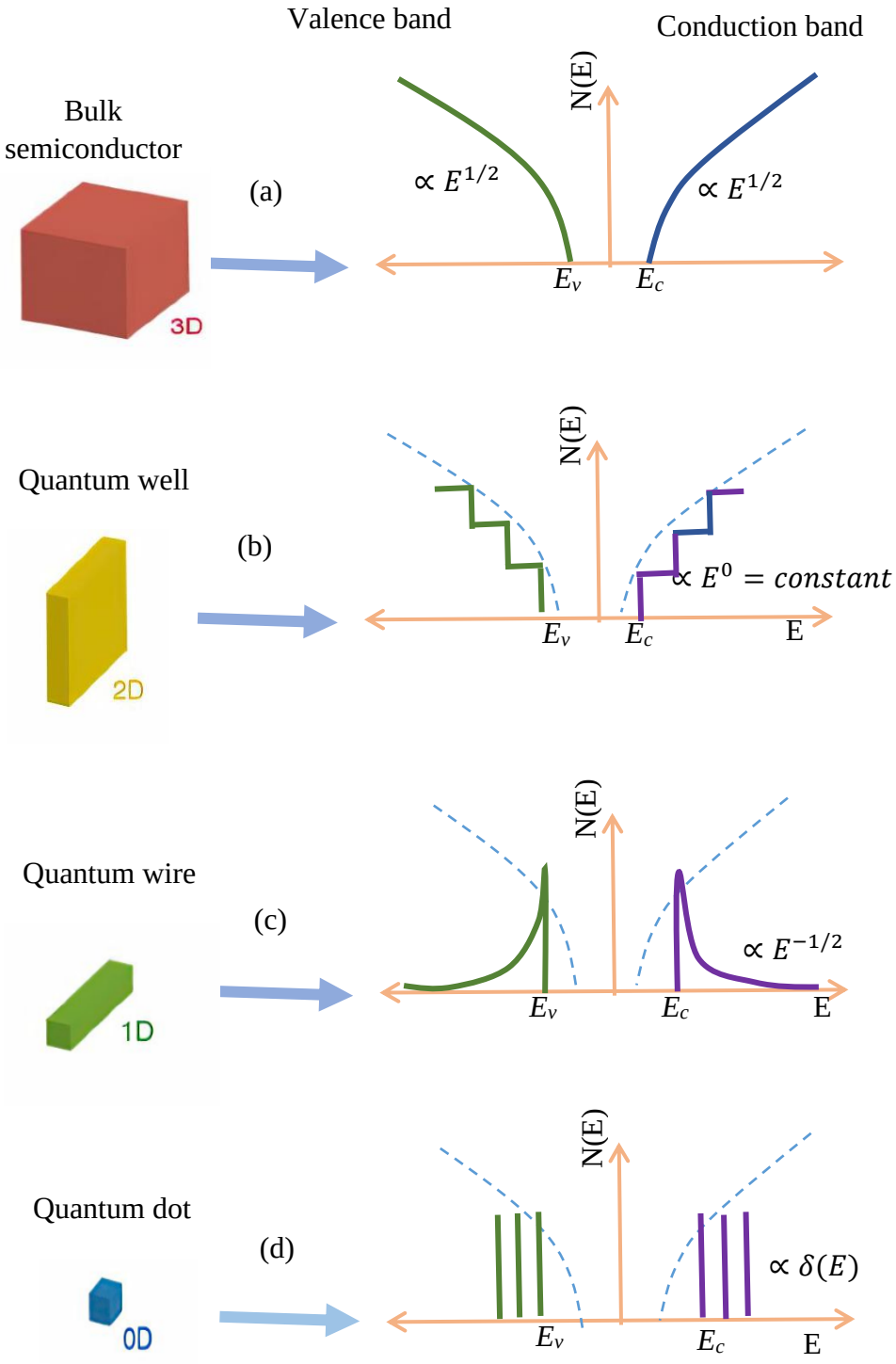

Figure 2.9: Density of states for (a) bulk semiconductor or three-dimensional system (3D), (b) two-dimensional systems (2D), (c) one-dimensional systems (1D), and zero-dimensional systems (0D). The dotted line represents the conduction and valence bands for a 3D system [16].

2.3 Heterojunction And Homojunction Structures

Semiconductor structures can either be homojunctions or heterojunctions. A homojunction structure is formed by growing layers of similar crystalline semiconductor materials on top of each other (e.g. p-n junction). Typically, these materials have the same bandgaps and lattice constants. A heterojunction is formed, however, when two different crystalline semiconductor materials with different properties are grown on top of each other [6].

2.3.1 Lattice Matching

The matching of lattice constants can be achieved by growing two layers of different materials on top of each other while both have the same lattice constant as shown in Figure 2.10 (a). On the other hand, if the two materials grown on top of each other have different lattice constants, the resulting structure is referred to as mismatched. The lattice mismatch is determined by [7]

$$\frac{\Delta a}{a} = \frac{a_{sub} - a_{layer}}{a_{sub}} \tag{2.9}$$

where a_{layer} and a_{sub} are the lattice constants of layer and substrate, respectively. There are two types of strain that can be encountered in a mismatched structure: compressive and tensile. A semiconductor layer with a large lattice constant (known as an epilayer) deposited on a substrate with a smaller lattice constant leads to compressive strain, as illustrated in Figure 2.10 (b). In contrast, tensile strain occurs when the lattice constant of the substrate is greater than that of the epilayer, as shown in Figure 2.10 (c).

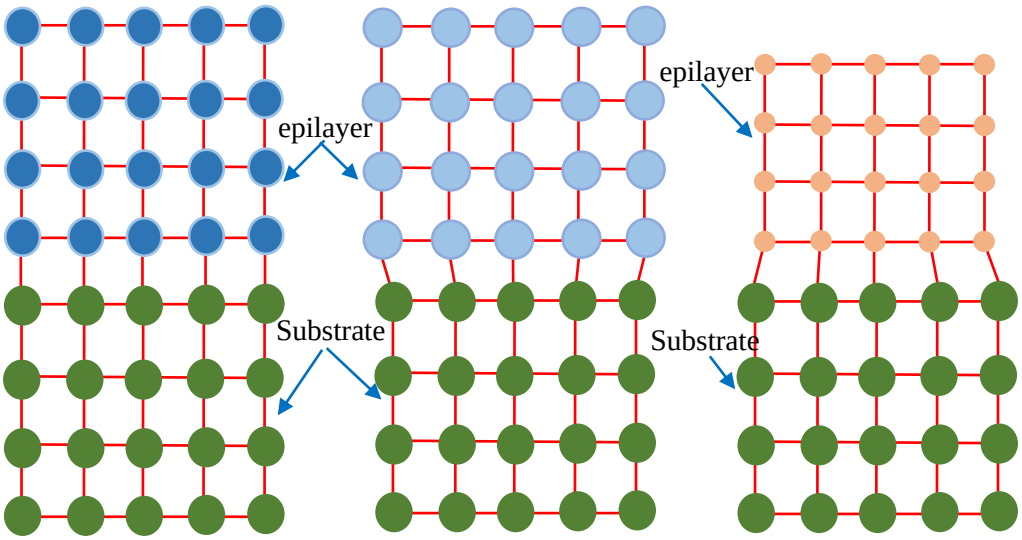

Figure 2.10: Schematic illustration of (a) lattice matched structure, (b) Compressive strain (lattice mismatched structure) and (c) Tensile strain (lattice mismatched structure).

2.3.2 Atomic Size And Electronegativity

There are a number of factors that contribute to the formation of heterojunction structures including the size of the atoms, electronegativity (χ) and alignment of energy bands in addition to the lattice match (mismatch). Electronegativity (χ), which refers to an atom's ability to attract electrons and form a chemical bond, also plays an important role in the process of growth [7]. χ is a unitless quantity but is generally referred to as Pauling scale. The first study of electronegativity was conducted by Linus Pauling in 1932 [17]. In accordance with Pauling's theory, if A and B are two different semiconductor materials used to form a heterostructure, the difference between their electronegativity (A and B) is given by

$$\chi_A - \chi_B = [(eV)^{-\frac{1}{2}}]\sqrt{E_D(AB) - \frac{[E_D(AA)+E_D(BB)]}{2}} \qquad (2.10)$$

where χ_A and χ_B are the electronegativity of material *A* and *B*, respectively. $E_D(AB)$, $E_D(AA)$ and $E_D(BB)$ are the dissociation energies in eV between the atoms *AB*, *AA* and *BB*, respectively. It is worth to mention that the electronegativity has no unit and the term $\left[(eV)^{-\frac{1}{2}}\right]$ is introduced to make the electronegativity unitless.

2.3.3 Band Alignment

The band alignment is crucial in controlling the behaviour of carriers in a heterojunction structure. According to Anderson's rule, the conduction and valence bands can be aligned between two semiconductor materials A and B. In Anderson's theory, the electron affinity of the materials that form the heterojunction drives the behaviour of the device [18]. A semiconductor A and another semiconductor B are used to form a heterojunction, and their vacuum levels have to line up as stated by Anderson's rule. When the vacuum levels are aligned, the difference in electron affinities between A and B (κ_A- κ_B) leads to the offset of both the conduction band (ΔE_c) and the valence band (ΔE_v) as given below [13].

$$\kappa_B - \Delta E_c - \kappa_A = 0 \tag{2.11}$$

$$\Delta E_c = \kappa_B - \kappa_A \text{ and } \Delta E_v = \Delta E_g - \Delta\kappa \tag{2.12}$$

Figure 2.11 depicts three different types of band alignments, namely, straddled alignment or type-I, staggered alignment or type-II, and broken gap alignment or type-III. In type-I alignment, a lower energy gap material (B) lies in the valence band of a material with higher energy gap (A) and a conduction band of the lower energy gap material (B) lies in the conduction band of the higher energy gap

material (A). Examples of such alignments include InGaAs/InP and AlGaAs/GaAs. When the conduction and valence band edges of a higher bandgap material (A) are higher than the relative band edges of the lower bandgap material (B) the alignment is known as a type II band alignment, for example GaSb/GaAs heterojunctions. In the case where the conduction band edge of one material (B) lies below the valence band edge of another material (A) then it is known as a type-III band alignment. This type of alignment can be seen in the GaSb/InAs heterostructure [13].

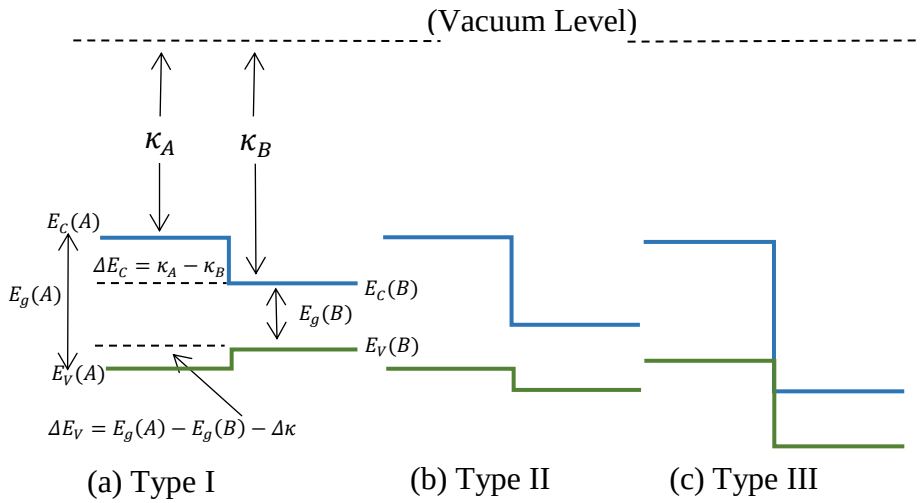

Figure 2.11: Types of energy bands alignments in heterojunctions, where E_c, E_v, E_g, ΔE_c, ΔE_v are the conduction band, valence band, energy gap, conduction band offset, and valence band offset, respectively. κ_A and κ_B are electron affinity of materials A and B, respectively.

2.4 General Properties Of Selected Semiconductors

This section contains the optical and electrical properties of semiconductor materials that have been investigated in this thesis. Among the recent advances in semiconductor research, Indium Nitride (InN) and Gallium Nitride (GaN) have attracted attention due to their tunable band gap energies, which can be used in a

wide variety of applications. The crystal structure has a significant effect on the optical and electrical properties of InN and GaN semiconductors. To better understand III-nitrides, this section provides a brief review of their structural, optical and electrical properties.

2.4.1 Properties Of III-Nitride Materials

A family of group III-V nitride materials consists of AlN, GaN, InN and their ternary and quaternary alloys. Typically, these semiconductors crystallize in zincblende or wurtzite forms, but wurtzite forms are the more stable polymorphs under ambient conditions [19]. The wurtzite crystal structure belongs to the $P6_3mc$ space group and has a hexagonal unit cell comprised of two interpenetrating hexagonal close-packed sublattices [20]. For the case of GaN, which has wurtzite structure, the electronic energy bands are the key determining factors of its optical and electrical properties. Figure 2.12 shows an energy band diagram of GaN with wurtzite crystal structure. The energy bandgap (E_g) in the Γ-valley is measured through the minima of the conduction band and maxima of the valence band at *k* (wave vector) = 0. E_A is an energy gap of 4.7-5.5 eV in A-valley. L-valley consists of an $E_{M\text{-}L}$ bandgap with a value of 4.5 to 5.3 eV. The value of E_{so} is 0.008 eV, and it is commonly referred to as the split-off band in the valence band.

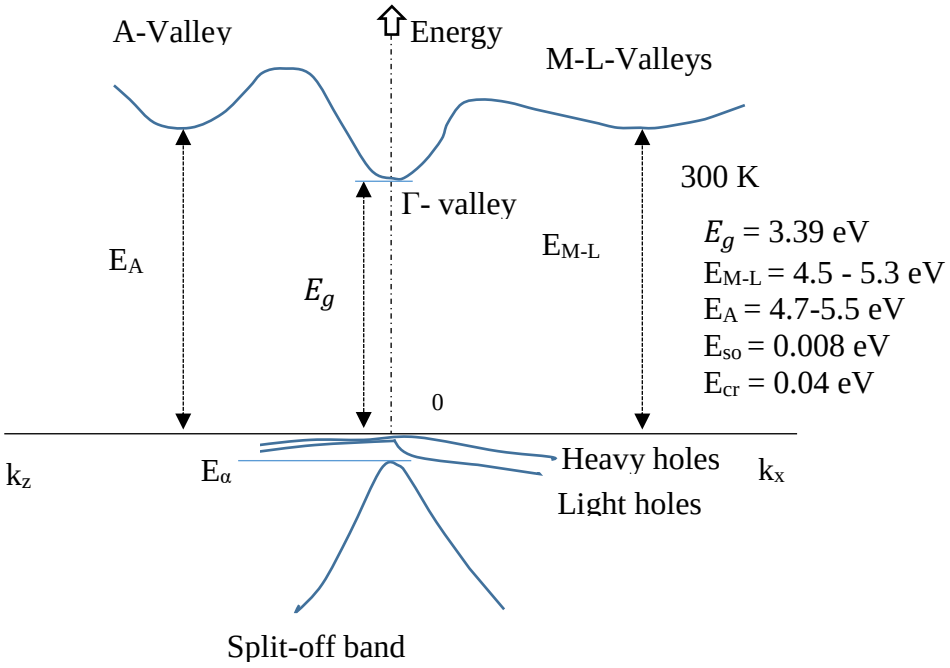

Figure 2.12: Energy band diagram of wurtzite GaN semiconductor [21].

The direct bandgap is one of the key determining factors of the optical and electrical properties of III-nitride materials. Figure 2.13 shows that the bandgaps of III-nitride semiconductors have a wide range of energies, extending from infrared (low energy) to ultraviolet (high energy) regions of the spectrum, ranging from 0.7 eV to 6.2 eV [22]. For the case of GaN, and AlN materials, which have wide bandgaps of 3.4 and 6.2 eV, respectively, and high thermal conductivities, devices based on these two materials are able to operate at high temperatures environment, as shown in Table 2.2. A significant advantage of III-V nitride materials is that they possess high electron velocity and mobility characteristics, which makes them suitable for high frequency applications as well. Additionally, III-V nitride materials have a high breakdown field that are required for high voltage applications. As a result of the advantages of III-V nitrides, they are excellent candidates for photonics and photonic integrated circuits as compared with conventional semiconductors such as III-arsenide and silicon [22].

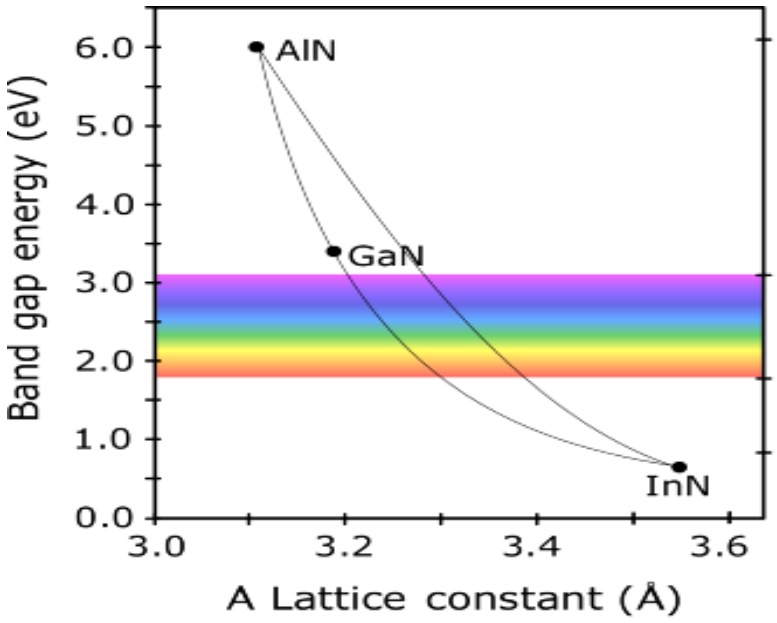

Figure 2.13: The band gap energy and lattice constant of III-nitride semiconductor [23].

Table 2.2: the optical and electronic properties of III-nitride semiconductors at room temperature [24, 25]

Parameters	**InN**	**GaN**	**AlN**
Band gap (eV)	0.64	3.39	6.2
Electron mobility (10^3 cm^2/(V.s))	3.0	1.2	1.1
Thermal conductivity (W/cm.K))	1.8	1.3	2.7
Thermal expansion coefficient (10^{-6}/K)	3.8	5.59	4.2
Saturated electron drift velocity (10^7 cm/s)	2.5	2.5	1.8
Breakdown field (MV/cm)	1.0	1.0	11.7

2.4.2 Gallium Oxide (Ga_2O_3)

Gallium oxide (Ga_2O_3) is a single crystal that possesses six polymorphs, namely α, β, γ, δ, ε and κ [26]. Amongst these, β is the most stable polymorph up to the melting point and is the only polymorph that can be grown by melting [27-30]. Ga_2O_3 is the most transparent semiconducting oxide (TSO) with a wide bandgap thus far known.

β-Ga_2O_3 has a direct bandgap of 4.9 eV [31] with high transparency in the ultraviolet spectrum [32]. This material exhibits unique properties, such as a wide bandgap, high transparency, chemical and thermal stability, which makes it suitable for use in electronic and optoelectronic applications.

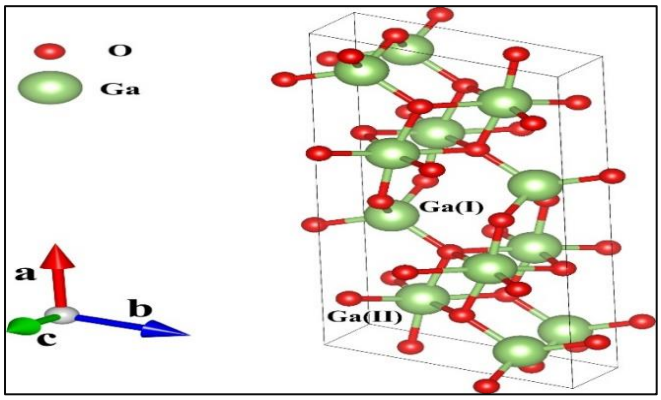

Figure 2.14: Crystal structure of Ga_2O_3 [33].

β-Ga_2O_3 has a monoclinic structure with lattice constants of a=12.23 Å, b=3.04 Å, and c=5.80 Å [34] as shown in Figure 2.14. Half of the gallium atoms, Ga (I), form tetrahedra, while the other half, Ga (II), form octahedra with neighboring oxygen atoms. Oxygen (I) atoms are threefold bonded with two Ga (II) atoms and one Ga (I) atom. Oxygen(II) atoms are also threefold bonded with one Ga(II) atom and two Ga(I) atoms [35].

β-Ga_2O_3 has recently attracted tremendous interest as a material for next generation power electronics due to (i) its high band gap of ~4.9 eV, high breakdown field of 8 MV/cm which is much larger than its GaN and SiC counterparts. In addition, the bandgap of β-Ga_2O_3 can be increased further by using ternary alloys such as β-$(Al_{1-x}Ga_x)_2O_3$ [36, 37]. This will open up new opportunities for next generation high power devices using β-$(Al_{1-x}Ga_x)_2O_3/Ga_2O_3$ heterojunctions.

The electrical breakdown value is empirically related to the semiconductor bandgap. Among the commonly quoted values of 8 MV/cm breakdown field value is that obtained by curve fitting, as shown in Figure 2.15 (a). In this Figure, the breakdown field for diamond is estimated to be 10 MV/cm and the bandgap of Ga_2O_3 was calculated as 4.9 eV. Figure 2.15 (b) shows a lower on-resistances of β-Ga_2O_3 compared to several contemporary wide bandgap and ultra wide bandgap semiconductors. Furthermore, β -Ga_2O_3 offers several higher power switch metrics such as Baliga figure of merit (BFOM), Johnson figure of merit (JFOM), and comparable saturation velocity, making it a prospective candidate for high power and high speed applications [36, 38]. Table 2.3 shows some of the important material properties of some wide bandgap semiconductors and those of β -Ga_2O_3.

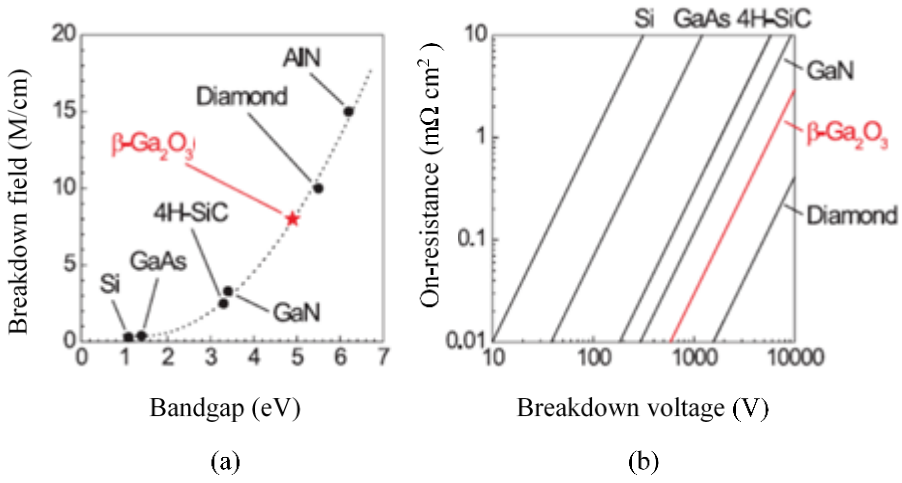

Figure 2.15: (a) Predicted breakdown field versus bandgap, and (b) theoretical limits of on-resistances as a function of breakdown voltage for several semiconductors [36].

Table 2.3: Comparison of key electronic properties of 4H-SiC, GaN, and β-Ga_2O_3 [36, 38]

Properties	**4H-SiC**	**GaN**	**β-Ga_2O_3**
Band gap (eV)	3.3	3.4	4.9
Electron mobility ($cm^2/(V.s)$)	1000	1200	300
Saturation velocity ($\times 10^7 cm.s^{-1}$)	2	2.5	2
Baliga	317	846	3214
JFOM/$JFOM_{Si}$	278	1089	2844
Breakdown field (MV/cm)	2.5	3.3	8
Substrate cost	High	High	Low

2.4.3 Nickel Oxide (NiO)

NiO, or Ni(II) oxide (NiO) is an excellent p-type semiconductor that is well known for its electrical and optical properties, as well as its chemical stability [39]. NiO semiconductors have high transparency in visible spectrums and bandgaps of between 3.6 and 3.8 eV [40]. In this material, antiferromagnetic behaviour can be observed up to 523 K, an unusually high Neel Temperature (T_N) for an anti-ferromagnet, while it becomes paramagnetic above T_N [41]. As a result of these desirable properties, anti-ferromagnetic materials are promising for a variety of applications in spin electronics because they have faster switching times than ferromagnetic materials [42]. In addition, it can be used in solar thermal absorber [43], fuel cells [44], electro-chromic display devices and gas sensors [45]. Figure 2.16 shows the atomic structure of NiO crystals. The structure of NiO is similar to rock salt structure which is face-centered cubic (FCC). Table 2.4 shows some of the important material properties of NiO.

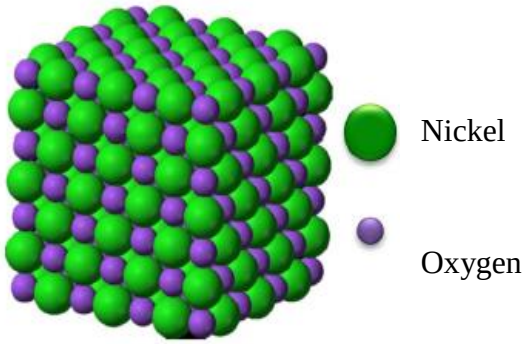

Figure 2.16: Face-centered cubic structure of NiO [46].

Table 2.4: important properties of NiO [47].

Molar Mass	74.69 g/mol
Mass density	6.67 g/cm^3
Crystal structure	Rock salt
Electronic configuration	3d^8
Melting point	1957 °C
Bandgap	3.6-4 eV
Type of semiconductor	p-type

2.5 Operation Of Light Emitting Diodes (LEDs) And Photodetectors (PDs)

2.5.1 Light Emitting Diodes (LEDs)

An LED consists of two elements of processed material called p-type semiconductor and n-type semiconductor. These two elements are placed in direct contact, forming a region called the p-n junction as can be seen in Figure 2.17. When the LED is forward biased, electrons from the conduction band and holes from the valence band recombine and emit a photon, enabling current to flow. When this occurs energy is released in the form of a photon [48].

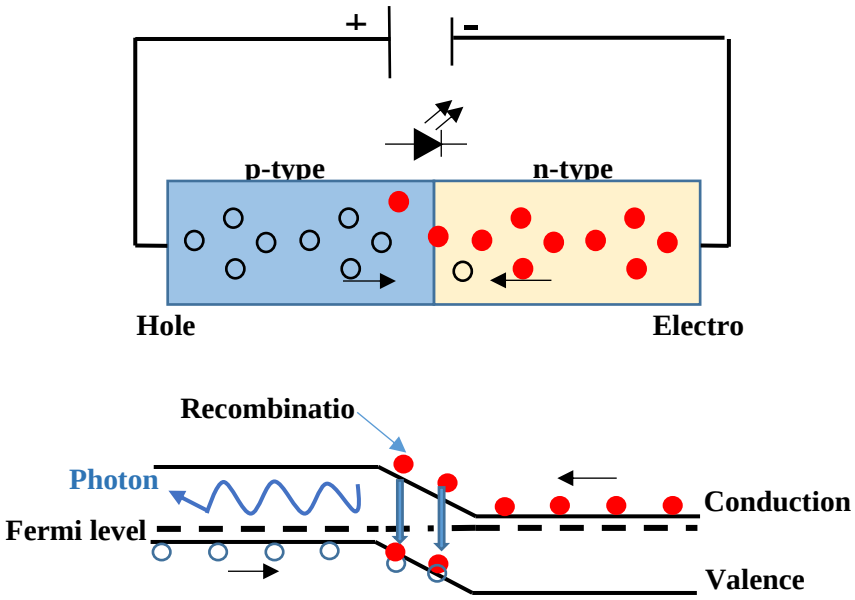

Figure 2.17: (a) Working principle of an LED; (b) Schematic energy band diagram of an LED [48].

2.5.2 Photodetectors (PDs)

Photodetectors are sensors that can convert the photon energy of light into electrical signal. Figure 2.18 illustrates a photodetector which consists of a p-n junction and operates in reverse bias, converting light photons into current. When the photon energy at a certain wavelength of light irradiation is equal to or greater than the bandgap of semiconductors, photons can excite the electrons from the valence band to the conduction band, resulting in conductive electron–hole pairs, increasing photodetector conductivity while generating electrical signals [49].

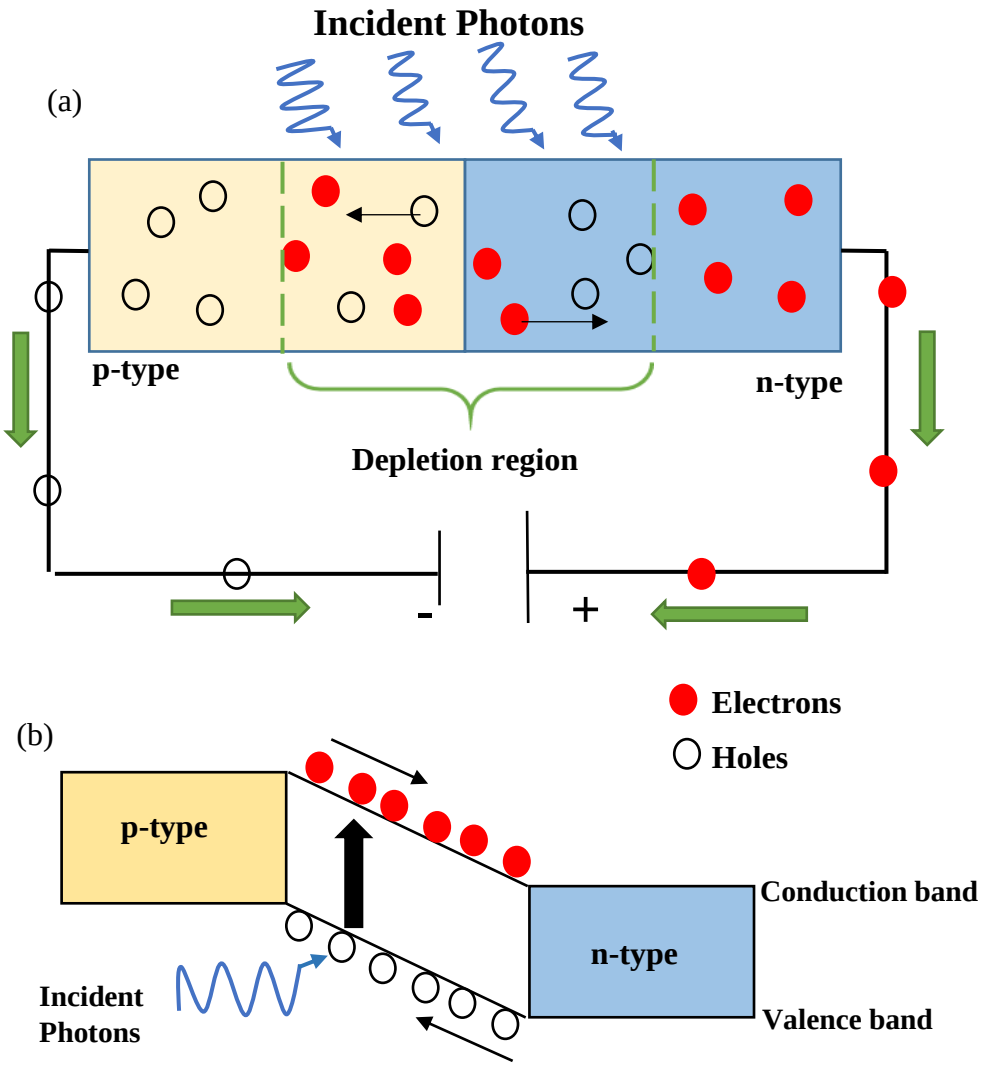

Figure 2.18: (a) Working principle of a photodetector; (b) Schematic energy band diagram of a PD.

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CHAPTER 3: SEMICONDUCTOR DEFECTS AND THEIR PROPERTIES

This chapter discusses the defects of semiconductors induced by foreign impurities and trapping centres. Also discussed is the theory of deep-level defects and their carrier kinetic processes. A brief review of defects in gallium nitride and related compounds, Ga_2O_3 and NiO semiconductor materials is presented.

3.1 Semiconductor Defects

A perfect crystal is formed by a periodic arrangement of unit cells along the crystal orientation. This type of crystal is called an ideal crystal [1]. However, in reality there are many types of defects ranging from point, complexes, and extended defects which make the crystal not perfect. A review of the most important defects will be discussed in this section.

3.1.1 Point Defects

A point defect refers to a structural defect caused by a single atom that has been located in an irregular position in the lattice. Due to the fact that point defects have zero dimensions, the disruption of the crystal structure resulting from these defects is localized. Defects of this type are present in different forms such as vacancy, substitutional, interstitial, and antisite impurities. As shown in Figure 3.1 (a), a vacancy defect is created when an atom is missing from a lattice site. There are cases where one of the basis atoms of a crystal structure is replaced by a foreign atom impurity. This form of defect is known as a substitutional defect, where an impurity atom is placed in a lattice site of the host semiconductor (Figure 3.1 (b)).

Whenever one of the host atoms is changed by a different host atom, this type of substitutional defect is known as an antisite defect. Figure 3.1 (c) illustrates the antisite defect observed in GaAs semiconductors, in which one As atom is replaced by one Ga atom (Ga_{As} antisite). When As occupies a Ga site, an As antisite (As_{Ga}) is formed. A further type of point defect is an interstitial impurity which can be seen in Figure 3.1 (d). A defect is generated by the presence of an atom in the space between two atomic sites. In the case where the atom is of the same type as the host material atoms, the defect is known as self-interstitial. In contrast, if the interstitial atoms are foreign to the regular crystal, the defect is called foreign-interstitial [2, 3].

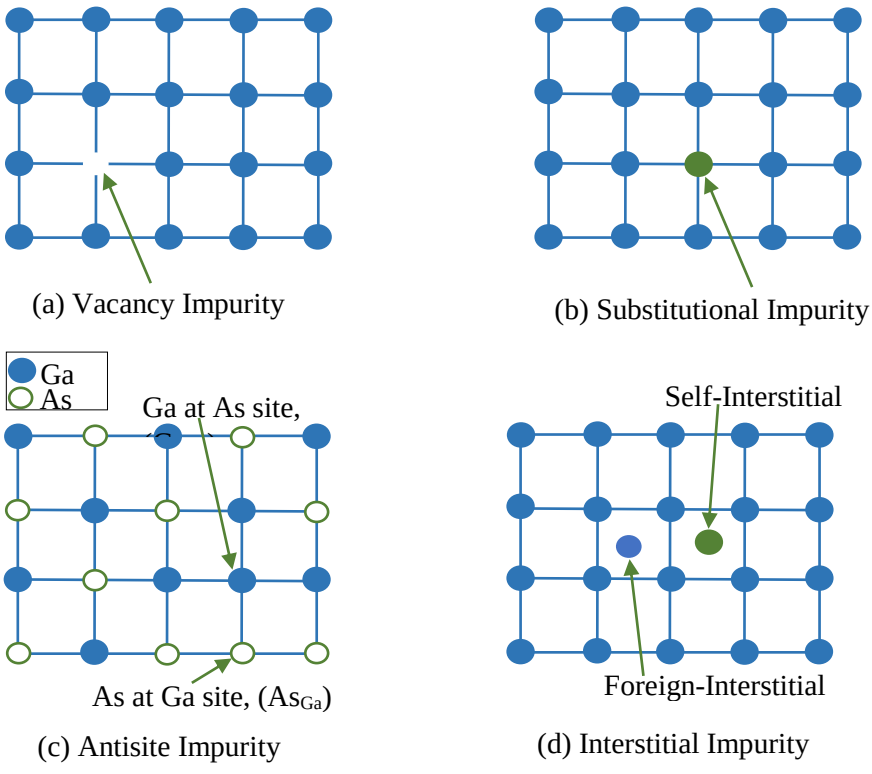


Figure 3.1: illustration of different forms of point defects in crystalline semiconductors: (a) Vacancy impurity; (b) Substitutional impurity; (c) Antisite impurity; and (d) Interstitial impurity

3.1.2 Complexes Of Point Defects

A point defect can be bound to another point defect like the atoms of a molecule are bound together. It is possible to have two or more point defects interact with each other, forming a pair known as a point complex defect [4]. Figure 3.2 (a) illustrates the split-interstitial defect that is created when two interstitial atoms form a pair. The defects are the result of either the interaction of two interstitial atoms of the same host material or of the interaction of two impurity interstitial atoms. Vacancy defects can also create different types of complexes within a crystalline system, as illustrated in Figure 3.2 (b). Particularly, when two vacancies form a pair, then the resulting complex is called the Di-vacancy. Moreover, the Frenkel defect is created when an atom forms a pair with itself in the interstitial space. Furthermore, vacancy-impurity complexes are formed when a vacancy and a foreign interstitial interact with each other. In addition, when two vacancies and an interstitial atom form a pair, a complex is formed known as a split vacancy. Figure 3.2 (c) illustrates another kind of complex defect, the impurity pair, which is created by a substitutional impurity atom forming a pair with an interstitial impurity atom.

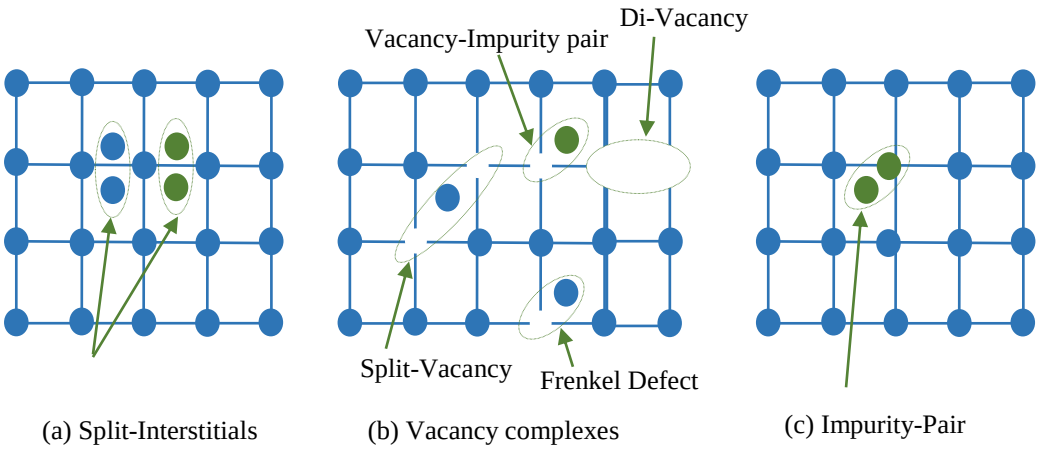
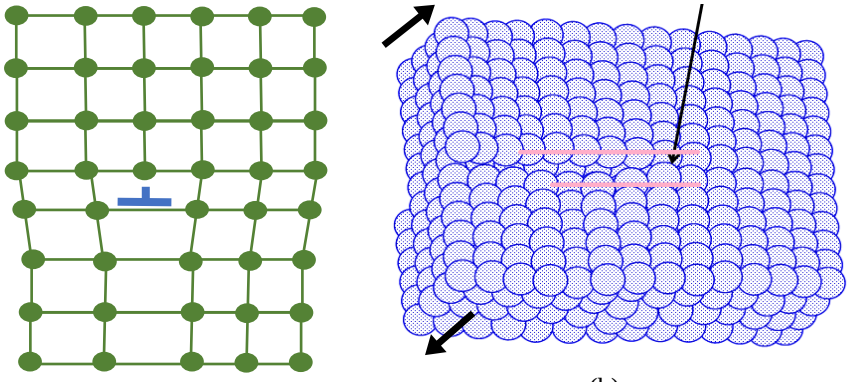


Figure 3.2: Illustration of different forms of complex defects: (a) split-interstitials, (b) vacancy complexes, and (c) complexes of impurity-pair.

3.1.3 Line Defects

The linear defect is also known as a dislocation defect or a one-dimensional defect that occur as a result of a line of atoms that are out of their regular positions in the crystal. The dislocation defect is a very common defect in semiconductors and is very much intertwined with the other kinds of defects [5]. The two most common types of dislocations are edge and screw dislocations. Edge dislocations occur when an extra half-plane of atoms exists in the middle of the crystal as shown in Figure 3.3 (a) [6]. In contrast, Figure 3.3 (b) shows screw dislocations which occur when one part of the crystal is displaced relative to the other [2].



(a) (b)

Figure 3.3: Illustration of different forms of linear defects: (a) edge dislocations and (b) screw dislocations.

3.2 Defects And Their Carrier Kinetics

This section discusses the classification of defects based on their energies. In addition, the mechanisms of recombination and generation processes will be discussed in detail.

3.2.1 Shallow And Deep Levels Impurities

The presence of any impurity can play a significant role in the electrical and optical properties of a semiconductor when it is within the bandgap range and its energy level falls inside it. As a result, defects are classified into shallow and deep levels according to their positions within the conduction and valence bands [7]. Shallow levels of impurities (dopant impurities) are defects that are located near the valence band or conduction band, as shown in Figure 3.4. Such defects, which are intentionally introduced as dopant atoms, are referred to as shallow donor levels if they contribute an electron to the conduction band (E_c) or shallow acceptor levels if they contribute a hole to the valence band (E_v) [8, 9]. Typically, shallow levels have a relatively low ionization energy of 5-10 meV and are easy ionized at room temperature, which enhances the electrical conductivity of semiconductors. Alternatively, defects with energy levels equal or greater than 0.1 eV below the conduction band or above the valence band are called deep-level impurities [10]. Since these defects cannot be ionized at room temperature, their contribution to the current flow is small. Therefore, the presence of deep level impurities could affect the electrical and optical properties of semiconductors. A discussion of the conduction mechanism involving impurities levels is provided in the following section.

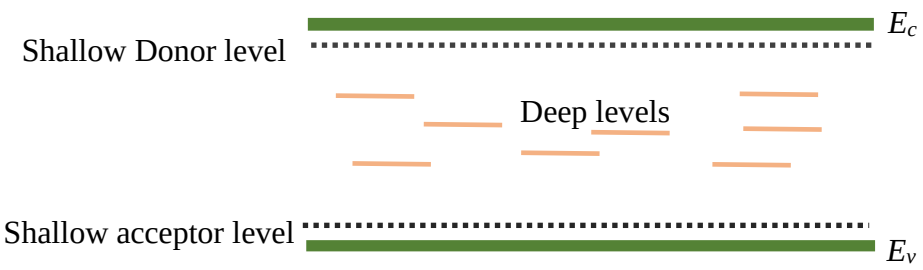


Figure 3.4: Schematic diagram showing deep and shallow defects within the bandgap of a semiconductor.

3.3 Generation And Recombination Processes (G-R Centres)

In semiconductors, deep-level impurities are also known as trap centres or Generation-Recombination Centres (GRCs). At equilibrium, the occupancy of a deep level is determined by the emission and capture rates of carriers. The recombination of electrons and holes in a semiconductor occurs in two different ways: direct and indirect recombination. A direct recombination, occurring between two bands, usually occurs in semiconductors, whereas an indirect recombination occurs between levels present within the bandgap of the material. The mechanism of the generation and recombination of charge carriers by deep levels has been described by Shockley and Read [1]. Additionally, it was described independently by R. N. Hall [11].

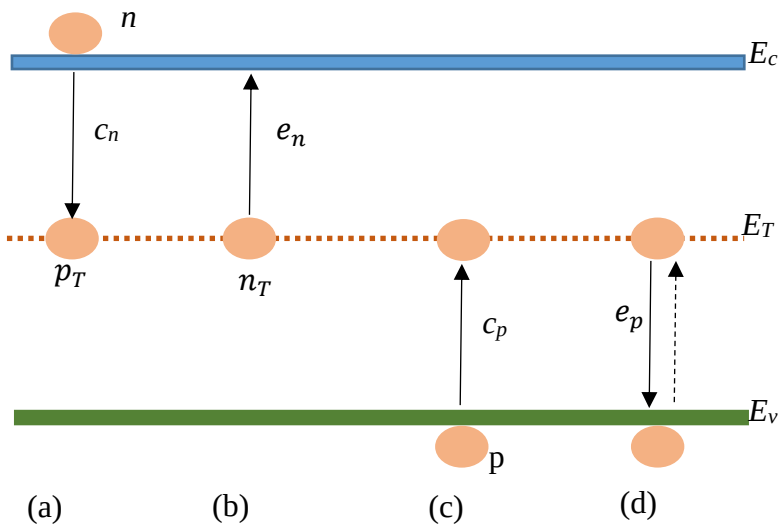


Figure 3.5: Schematic diagram of capture and emission processes: (a) capture of electron (b) emission of electron (c) capture of hole and (d) emission of hole.

The process of generation-recombination is illustrated in Figure 3.5. A deep-level impurity in the semiconductor has an energy E_T located within the forbidden gap

that is distributed throughout the semiconductor and has a concentration N_T. Consider, first, that an electron from the conduction band is captured by the centre (Figure 3.5 (a)), and this captured electron can be described by its electron capture coefficient (c_n). The electron at the centre may be emitted back into the conduction band (electron emission (e_n)), as shown in Figure 3.5 (b), or the hole from the valence band can be captured by the centre, which is called a hole capture (c_p) (Figure 3.5 (c)). As a result of either of these two processes, a hole will be formed in the deep centre, again with two possibilities. This means that the centre has the capability of emitting the hole back to the valence band (hole emission e_p), as shown in Figure 3.5 (d), or can even capture an electron from the conduction band (Figure 3.5 (a)). Process (d) can be viewed as electron emission from the valence band to the centre, as shown by the dashed arrow in Figure 3.5 (d). It is important to point out that these are the only four possible processes occurring between the conduction band, impurity levels, and valence band. A recombination occurs when electrons are captured (Figure 3.5 (a)) followed by holes being captured (Figure 3.5 (c)). In contrast, generation occurs when an electron is emitted to the conduction band (Figure 3.5 (b)) followed by the emission of a hole to the valence band (Figure 3.5 (d)). Furthermore, a third process is known as trapping, which is neither generation nor recombination. A trap centre is referred to as a deep level when a capture of an electron is followed by the emission of the electron back into the conduction band, or when a capture of a hole is followed by the emission of the hole back into the valence band. During the trapping process, the conduction band or valence band is the only band involved in the impurity level. In the recombination or generation process, both the conduction and valence bands, along with the level of impurity participate. The centres located in the lower half of the

bandgap generally have a hole emission rate much lower than the electron emission rate. Similarly, for the centres in the upper half, the electron emission rate is greater than the hole emission rate. Most centres have one dominant emission rate while the other can be neglected. The G-R centre can be either electron or hole occupied. An electron occupies the centre in a n_T state, while a hole occupies it in a p_T state. n_T is neutral, while p_T is positive charge in a donor G-R centre. For an acceptor centre, n_T is a negative charge and p_T is a neutral charge. The total density of G-R centres (N_T) filled by electrons (n_T) or holes (p_T) is given by equation (3.1). It is worth noting that a centre is either occupied by an electron or a hole [12].

$$N_T = n_T + p_T \tag{3.1}$$

The density of electrons in the conduction band (n), the density of holes in the valence band (p) and the state of the centre n_T or p_T change together with time. It is important to know the rate of change with time of these parameters. Emission of electrons increases the density of electrons in the conduction band (n) while electron capture decreases them. Therefore, the change of (n) with respect to time due to the *G-R* process can be written as

$$\frac{dn}{dt}|_{G-R} = (b) - (a) = e_n n_T - c_n n p_T \tag{3.2}$$

Generally, the emission rate e_n equals the number of electrons emitted per second by the G-R centre into the conduction band. The concentration of the trap occupied by electrons is given by n_T. According to equation (3.2), the only parameters that affect electron emission are e_n and n_T. In addition, from this equation, it is obvious

that the process of electron capture is governed by the presence of electrons in the conduction band n, the electron capture rate c_n, as well as the concentration of traps occupied by holes p_T. As in equation (3.2), the change in holes density per time is given by [12]:

$$\frac{dp}{dt}|_{G-R} = (d) - (c) = e_p p_T - c_p p n_T \tag{3.3}$$

The electron capture coefficient c_n is affected by the electron thermal velocity and the cross-sectional area of the *G-R* centre. The dependence can be expressed as follows [12]:

$$c_n = \upsilon_{th}\sigma_n \tag{3.4}$$

Similarly, the hole capture coefficient is given by

$$c_{\mathrm{p}} = \upsilon_{th}\sigma_{n\mathrm{p}} \tag{3.5}$$

The concentration of the *G-R* state changes as a function of time during the emission or capture process. Therefore, this rate change can only be calculated using Equations (3.2) and (3.3), and it is given by [12]:

$$\frac{dn_T}{dt}|_{G-R} = \frac{dp}{dt} - \frac{dn}{dt} = \left(c_n n + e_p\right)(N_T - n_T) - \left(c_p p + e_n\right)n_T \tag{3.6}$$

Under the steady state condition, the density is $\frac{dn_T}{dt} = 0$ and therefore equation (3.6) can be rewritten and rearranged as follows [12]:

$$n_T = \frac{e_p + c_n n}{e_n + c_n n + e_p + c_p p} N_T \tag{3.7}$$

In most cases, deep-level impurity measurements are based on equation 3.8. The detailed balance principle states that the rate of emission and the rate of capture are equal at thermal equilibrium. Consequently,

$$e_n n_T = c_n n p_T \tag{3.8}$$

Assuming Equation 3.4 is applied, Equation 3.8 is written as follows:

$$e_n n_T = \upsilon_{th} \sigma_n n p_T \tag{3.9}$$

Similarly, if holes exist,

$$e_p p_T = \upsilon_{th} \sigma_p p n_T \tag{3.10}$$

According to the Fermi-Dirac distribution, f, the total density of deep levels is given by

$$N_T = n_T + p_T = N_T f + N_T (1 - f) \tag{3.11}$$

Assuming that Fermi-Dirac distribution function (f) is the number of states occupied by electrons, the number of states occupied by holes is (1- f). Fermi-Dirac distribution function is defined as follows [3]:

$$f = \left[\frac{1}{1 + \exp\left(\frac{E_T - E_F}{k_B T}\right)} \right] \tag{3.12}$$

where E_F is the energy of the Fermi level, k_B is the Boltzmann constant and T is temperature. So, by using Equations (3.12) and (3.11) in Equation (3.8), this gives [12]:

$$e_n = \sigma_n \langle v_n \rangle_{th} n \exp\left(\frac{E_T - E_F}{k_B T}\right) \tag{3.13}$$

where *n* is the density of electron in conduction band and is given by

$$n = n_i \exp\left(\frac{E_F - E_i}{k_B T}\right) = N_c \exp\left(-\frac{E_c - E_F}{k_B T}\right) \tag{3.14}$$

where n_i is the intrinsic carrier concentration,

$$n_i = N_c \exp\left(\frac{E_i - E_c}{k_B T}\right) \tag{3.15}$$

Subsequently, by substituting equation (3.14) in equation (3.13), this gives:

$$e_n = \sigma_n \langle v_n \rangle_{th} N_c \exp\left(-\frac{E_c - E_T}{k_B T}\right) \tag{3.16}$$

where N_C is the density of states in the conduction band:

$$N_c = 2\left(\frac{2\pi m_e^* kT}{h^2}\right)^{\frac{3}{2}}$$

$$\langle v_n \rangle_{th} = \left(\frac{3kT}{m_e^*}\right)^{\frac{1}{2}}$$

where m_e^* is the effective mass of electrons.

Similarly, substituting $p = N_v\ exp\left(-\frac{E_F - E_v}{K_B T}\right)$ in Equation (4.10) gives:

$$e_p = \sigma_p \langle v_p \rangle_{th} N_v \exp\left(-\frac{E_T - E_v}{k_B T}\right) \tag{3.17}$$

where N_v and $\langle v_p \rangle_{th}$ are given by

$$N_v = 2\left(\frac{2\pi m_p^* kT}{h^2}\right)^{\frac{3}{2}}$$

$$\langle v_p \rangle_{th} = \left(\frac{3kT}{m_p^*}\right)^{\frac{1}{2}}$$

where m_p^* is the effective mass of holes.

Substituting the values of $\langle v_n \rangle_{th}$and Nc $\langle v_p \rangle_{th}$ N_v in Equations (3.16) and (3.17), respectively, equations (3.18) and (3.19) are obtained as follows:

$$e_n = AT^2 \sigma_n \exp\left(-\frac{E_c - E_T}{k_B T}\right) \tag{3.18}$$

$$e_p = AT^2 \sigma_p \exp\left(-\frac{E_T - E_v}{k_B T}\right) \tag{3.19}$$

where A is a constant, equal to:

$$A = 2\left(\frac{2\pi m_e^* k_B}{h^2}\right)^{3/2}\left(\frac{3k_B}{m_e^*}\right)^{1/2} = 4m_e^* \frac{\sqrt{6\pi^3}(k_B)^2}{h^3}$$

Moreover, the Arrhenius plot of $\left(\frac{e_{n,p}}{T^2}\right)$ versus $\frac{1000}{T}$ generates a straight-line graph. From the slope of that graph, the activation energy of the deep level can be extracted. This parameter is the most important parameter for characterisation of the deep levels because it shows the position of the deep level in the forbidden gap.

3.4 Defects In Some Semiconductor Materials

In almost every modern electronic device, semiconductor materials play an important role. Accordingly, the semiconductor industry has recently experienced highly significant growth. Among the major hurdles and difficulties encountered in these industries is the production of perfect crystals. As a matter of fact, all crystals have imperfections or defects because some atoms can enter the crystal structure or even be missing in some places in the structure or lattice of the crystal [8]. A defect in a device may alter its electrical or optical properties, thereby altering its performance. Due to this, it has become very important to identify and characterize the defects created during the growth and processing of materials and devices in order to better understand their functionality [13]. A brief review of the literature for defects in GaN and related compounds, Ga_2O_3 and NiO materials is presented in the following section.

3.4.1 Defects In Gallium Nitride And Related Compounds

The wide-bandgap compound semiconductor gallium nitride (GaN) is widely used in many applications such as Light Emitting Diode (LED), transistors and power integrated circuits and radar. In this III-V compound semiconductor, different types of crystalline defects can be created during the growth process, such as vacancies,

interstitials, and antisite defects. These defects play an important role in the optoelectronic and electronic properties of devices.

The most common defect in GaN samples is ET3 trap. This deep level defect typically has an energy level of 0.16 eV [14]. As a matter of debate, the character of this trap (donor or acceptor) remains unclear. Several studies suggested that it is a donor and is related to nitrogen vacancy V_N [15-17]. However, the traps are determined to be acceptors due to the fact that their activation energy is independent of the applied electric field in DLTS measurements [18]. Another common deep level trap in undoped n-GaN is D found in n-GaN film grown by hydride vapor-phase epitaxy [15] or ET5 [19] in GaN film grown by metalorganic chemical vapour deposition (MOCVD) with an activation energy of 0.25 eV and concentrations ranging from ~2×10^{13} cm^{-3} to ~8×10^{13} cm^{-3}. The DLTS spectra measurements of n-GaN grown by molecular beam epitaxy (MBE) under various N to Ga fluxes strongly suggest that conditions that are N-rich are conducive to the formation of these defects [20]. These centres are associated with nitrogen vacancies or their complexes [20, 21]. Another common trap in GaN grown by MBE, which was mainly detected by deep level optical spectroscopy (DLOS) and DLTS, has typically activation energies ranging from 1.28 to 1.35 eV. These traps were assigned to interstitial C donors [20-22].

Similarly, the most common traps in the wider bandgap AlGaN/GaN Schottky are Ec-0.57±0.03 eV [23]. According to Götz et al [24], the level found in $Al_{0.12}Ga_{0.88}N$ by using DLTS is probably the same as that found in GaN (E2= 0.58 eV [25], D2= 0.60 eV [26], ET10= 0.56 eV [14], B= 0.62 eV [27]), which was attributed to nitrogen antisite N_{Ga} [23, 26]. An additional common defect with activation energy of 0.11–0.14 eV was associated with Ga vacancy (V_{Ga}) related defects [25-28].

Another type of III-Nitride semiconductor material is InGaN which is affected by common defects. Among these defects is EN1 with activation energy of 0.26 eV below the conduction band edge and capture cross section of ~10−15 cm^2 [29]. The defect is a characteristic of point defects. Defects with such energy levels have been associated with nitrogen-vacancies (V_N) [30-33]. One of the most common and deep defects in InGaN/GaN is e_2. This deep level defect typically has an energy level 0.70 eV [34]. This trap was attributed to native defects (such as nitrogen-related defects or vacancies) [25, 35, 36], possibly arranged along dislocations [34]. The activation energies and origin of the above mentioned traps are summarised in Table 3.1.

Table 3.1: Properties and origin of traps reported in GaN and related compounds.

Trap and material	Activation energy (eV)	Origin	References
ET3 in GaN	0.16	V_N	[14-18]
D in GaN	0.25	associated with V_N	[14, 19-21]
Electron trap	1.28 to 1.35	interstitial C donors	[20-22]
E2, D2, ET10 and B in GaN	0.58 to 0.62	N_{Ga}	[14, 23-27]
Electron trap	0.11–0.14	associated with V_{Ga}	[25-28]
EN1 in InGaN	0.26	V_N	[29-33]
e_2 in InGaN	0.70	native defects	[25, 34-36]

3.4.2 Defects In Ga_2O_3

Ga_2O_3 has a wide bandgap and various intentional and unintentional trap levels have been reported. Therefore, investigation of electrically active defects is necessary due to the great potential of Ga_2O_3-based power electronics and optoelectronics in the future. Previously, several defect levels have been observed

in both single crystals and thin films of β-Ga_2O_3 using deep-level transient spectroscopy (DLTS), deep-level optical spectroscopy (DLOS), admittance spectroscopy, thermally stimulated current (TSC) spectroscopy, and thermally stimulated depolarization current (TSDC) [37-39]. An unintentional donor of 110 meV energy was observed in β-Ga_2O_3 single crystal grown by edge-defined film-fed growth (EFG) [37]. The origin of this donor level has been proposed to either a native interstitial or a Si substitution at the octahedral Ga site. Tadjer et al. reported the existence of a trap that is located at 0.23 eV below the conduction band in halide vapor phase epitaxial β-Ga_2O_3 which was doped with both Si and N impurities [40]. A study was also conducted on the effect of twin boundaries, which induce structural disorder, on homoepitaxial β-Ga_2O_3 thin films. An acceptor level with an activation energy of 0.34 eV was identified using DLTS. This trap was believed to originate from twin lamellae, which could be responsible for the observed electrical compensation and mobility reduction [41].

Titanium (Ti) is often used as Ohmic contact in β-Ga_2O_3. The contact between Ti in β -Ga_2O_3 may produce a defect with an activation energy of 0.95 eV, which originates from octahedral Ga substitution [42]. Irmscher et al. proposed that Co impurity may be responsible for trap levels at 0.55 eV and 1.04 eV in undoped β -Ga_2O_3 crystals grown by the Czochralski method from an iridium crucible under a carbon dioxide containing atmosphere [43]. Deep levels have been studied by Zhang et al. in β -Ga_2O_3 single crystal using both the DLTS and DLOS methods [39]. They observed traps at Ec =0.62 eV, 0.82 eV, 1.0 eV, 2.16 eV, and Ec =4.40 eV below the conduction band. Wang et al. investigated the traps in β-Ga_2O_3 thin films using TSC and TSDC [38]. The films used for the measurements were grown in oxygen, argon, and a mixture of both gases. It was found that the thin films grown

in an argon atmosphere possessed reduced traps compared to other growth conditions. The activation energies and origin of the above mentioned traps are summarised in Table 3.2.

Table 3.2: properties and origin of traps reported in β -Ga_2O_3

Activation energy (eV) of trap	**Origin**	**References**
0.23		[40]
0.34	twin lamellae	[41]
0.95	Octahedral Ga substitution	[42]
0.55 and 1.04	Co impurity	[43]
0.11-0.14, 0.62, 0.82, 1.0, 2.16, 4.40		[38-39]

3.4.3 Defects In NiO

The native defects of NiO influence its optoelectronic and transport properties significantly [44]. It has been demonstrated that Ni vacancy (V_{Ni}) defects in NiO lead to the enhancement of p-type conductivity. It has been shown by Lany et al [45] and Dawson et al [46] that when the growth condition is O-rich, the formation energies of V_{Ni} and oxygen vacancies (V_O) are low and high, respectively. The results of these studies are in agreement with the p-type conductivity observed in O-rich NiO materials [47, 48]. Furthermore, it has also been shown that native defects in NiO have a significant effect on the bandgap and optical properties of the material. The Ni-vacancy (V_{Ni}) state has been attributed to the degradation of its transparency to visible light. In their study, Newman and Chrenko [49] noted that NiO with excess oxygen appeared darker, which they attributed to background absorption in the range of 0.1 to 3.0 eV that is caused by defects with increasing O/Ni ratios. Among other findings, Ono et al [50] examined the relationship between transmittance and electrical properties of NiO thin films deposited by

sputtering, and concluded that dipole- forbidden charge transfer transitions induced by V_{Ni} may play a role in producing the darker colour.

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CHAPTER 4: EXPERIMENTAL TECHNIQUES

Semiconductor materials can be used to build a wide variety of electronic devices based on metal-semiconductors and p-n junctions. It is possible to obtain n-type and a p-type semiconductors by doping them in such a way that enables electrons and holes to be the majority carriers, respectively [1]. Alternatively, metal-semiconductor contacts or Schottky barrier diodes can be formed by the deposition of a metal on either n- or p-type semiconductor [2]. In general, the main difference between a p-n junction and a Schottky diode lies in the depletion region. Depletion occurs at the p-n junction when electrons in the n-type region move toward the p-type region and combine with the holes. A result of this process is that negative ions are formed in the p-type region and positive ions in the n-type region. A strong electric field results from the opposite polarity ions on the two sides of the junction, creating a depleted area that prevents transfer of carrier charges. In the case of a Schottky barrier, the entire depletion region is on the semiconductor side since the depletion on the metal side is so small that it can be neglected. Therefore, a discussion of the fundamental characteristics of a p-n junction is provided in this chapter. In this study, techniques such as current-voltage (I-V), capacitance-voltage (C-V), deep level transient spectroscopy (DLTS), Laplace DLTS, Photoluminescence (PL), Electroluminescence (EL), Cathodoluminescence (CL), Photocurrent and Scanning Transmission Electron Microscopy (STEM) techniques were employed to determine the electrical and optical properties of the samples investigated in this thesis. Their principles of operation will be discussed in this chapter.

4.1 P-N Junction

The junction between a p-type and an n-type semiconductor is called a p-n junction. In a p-n junction system, holes diffuse into the n-region and electrons diffuse into the p-region, leading to the creation of a depletion region [1]. This region acts as a barrier to prevent further diffusion of electrons and holes.

Figure 4.1 shows schematic illustrations of the energy band of a p-n junction before and after the formation of the junction under thermal equilibrium condition and in the absence of an applied bias. $q\chi_s$ is the work function of the semiconductor and χ_s represents the electron affinity of the semiconductor material. E_{Fn} and E_{Fp} represent electron and hole Fermi levels, respectively. qV_{bi} is the electrostatic potential differences (built-in potential) at thermal equilibrium between the n and p regions. The potential difference between the Fermi level and the intrinsic Fermi level in the p-region and n-region is represented as $V_p$and V_n, respectively. x_n and denote the depletion layer width in the n and p regions, respectively. E_c, E_v, and E_{Fi} are the conduction band energy, valence band energy and intrinsic Fermi level, respectively [3, 4]. Figure 4.1 (a) shows that for n-type semiconductor the Fermi level (E_{Fn}) is below the conduction band. However, for p-type semiconductor the Fermi level (E_{Fp}) is above the valence band (E_v). Figure 4.1 (b) indicates that the Fermi level (E_F) is constant at thermal equilibrium for the p-n junction. Additionally, as shown in Figure 4.1 (b), the n and p doped regions are considered to be uniformly doped, whereas the transition between the n and p regions is abrupt. Consequently, this results in the formation of an abrupt junction (also called a step junction, or a shallow diffused junction). In contrast, a linearly graded junction (or a deep diffused junction) is formed when doping concentrations are not uniform in the p-n junction regions. As a result, the doping change at the metallurgical junction

is graded. Figure 4.1 (c) shows that there are three distinct regions in a p-n junction. These are the quasi-neutral p and n regions (QNR) away from the metallurgical junction, and the space-charge (or depletion) region (SCR) that is occupied by the shallow ionized acceptors in the p-depletion region, and the shallow ionized donors in the n-depletion region.

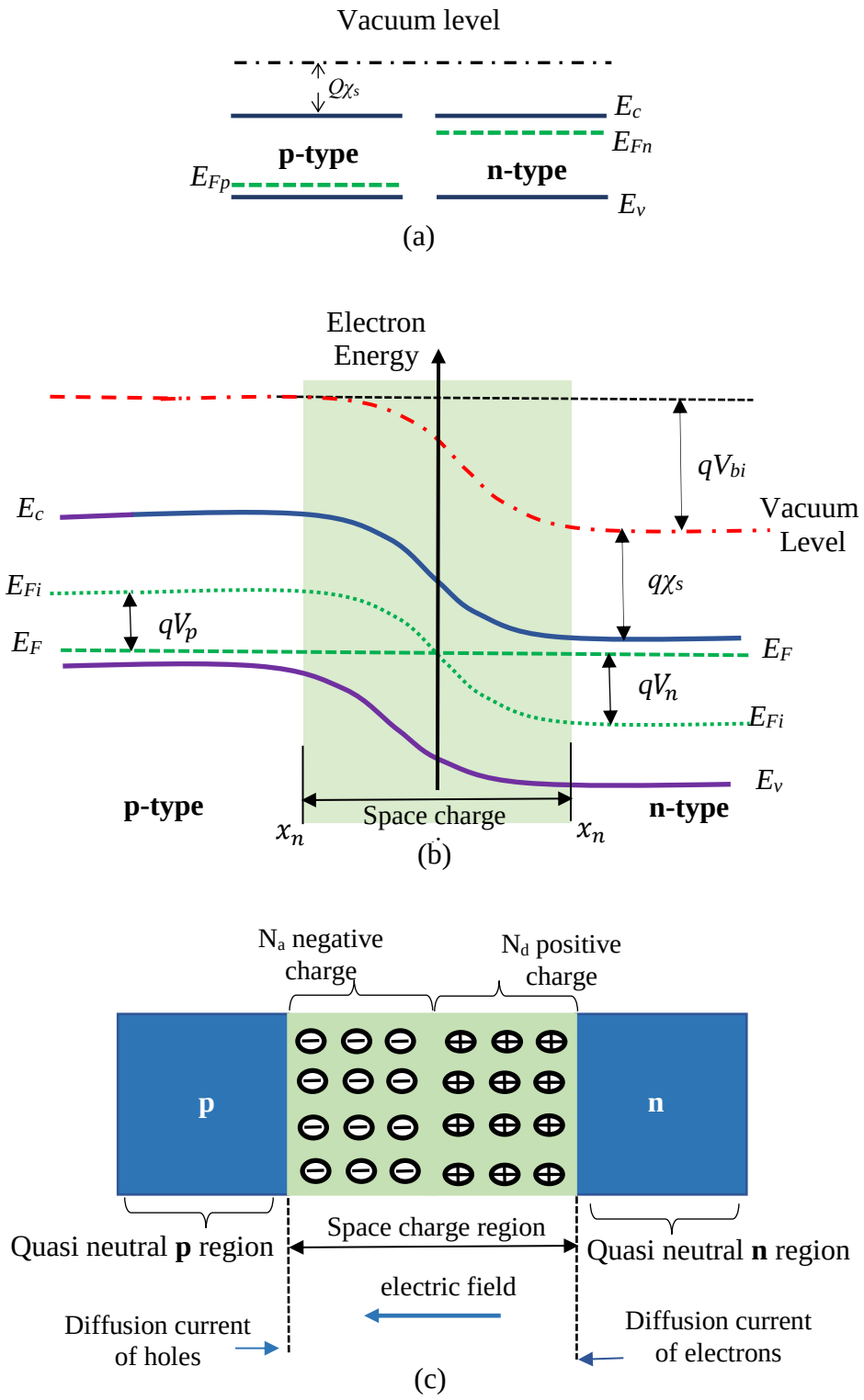


Figure 4.1: Schematic diagram of a p-n junction: (a) the energy band structure of a p-type and n-type semiconductor before forming the junction (b) the energy band structure after the formation of the junction (c) p-n junction showing the depletion region (or space charge region)

The concentration of electrons and holes in the p and n regions can be given by:

$$n = n_i exp\left(\frac{V_n}{V_T}\right) \tag{4.1}$$

$$p = n_i exp\left(\frac{-V_p}{V_T}\right), \tag{4.2}$$

where n_i is the density of the intrinsic carrier, V_T is the thermal voltage which is equal to the Boltzmann constant divided by electric charge $\frac{K_B T}{q}$

The built-in potential, carrier distribution, electric field, potential profile in the junction space-charge region for an abrupt p-n junction and a linear-graded p-n junction are derived from the continuity equation and Poisson's equation.

In general, at equilibrium, the relationship between the charge distribution and the potential *V* (or the electric field,) of these junctions is given by Poisson's equation:

$$\frac{d^2V}{dx^2} = \left(\frac{dE}{dx}\right) = \frac{\rho(x)}{\varepsilon_s} = \frac{q}{\varepsilon_s}[N_D^+(x) - n(x) - N_A^-(x) + p(x)] = 0 \tag{4.3}$$

where E is the electric field, ε_s is the permittivity of the semiconductor material, ρ is the density of charge, $n(x)\ and\ p(x)$ are the densities of the carrier at a distance x from the junction, and $N_A^-(x)\ and\ N_D^+(x)$ are uncompensated acceptor and donor ions, respectively.

Equation (4.3) can be solved by "depletion approximation". In this approximation it is assumed that (1) there are only ionized doping impurities $N_D^+(x)\ and\ N_A^-(x)$ in SCR, (2) the contribution of free carriers (n and p) to the local charge is negligible, (3) there are no free holes in the depletion region on the n-type side and the p-type side, respectively. Therefore, in the depletion regions, the charge densities are equal to those in the n-type and p-type materials (the metallurgical

junction is taken as the origin). By using appropriate boundary conditions and Equations 4.1 to 4.3, the electric field, built-in voltage and charge distribution in different regions of p-n junction can be obtained. It is known that the total charge density is equal to zero in the quasi-neutral p and n regions, consequently Eq. (4.3) becomes (assuming complete ionization):

$$[n - p - N_D - N_A] = 0 \tag{4.4}$$

where N_A and N_D are the holes and electrons density on the p- and n- side, respectively. By assuming N_A to be zero (or $N_A << N_D$), p << n and N_A=p=0, in the quasi-neutral n region, then the electrostatic potential (V_n) at the edge of the region can be obtained by substituting the above assumptions in Eq. (4.4) and Eq. (4.1), which yields:

$$n = N_D \tag{4.5}$$

$$N_D = n_i exp\left(\frac{\mathrm{V}_n}{V_T}\right) \tag{4.6}$$

Therefore, solving the potential can be obtained by taking the log for both sides of Equation (4.6), which yields to:

$$\mathrm{V}_n = V_T ln\left(\frac{N_D}{n_i}\right) \tag{4.7}$$

By applying similar assumptions for the p-region, the electrostatic potential (V_p) at the edge of the depletion layer can be written as:

$$V_p = -V_T ln\left(\frac{N_A}{n_i}\right) \tag{4.8}$$

The built-in potential (V_{bi}) can be calculated using Eq. (4.8) and Eq. (4.7). This gives the following:

$$V_{bi} = \mathrm{V}_n - \mathrm{V}_p = V_T ln\left(\frac{N_A N_D}{{n_i}^2}\right) \tag{4.9}$$

By assuming n = p = 0 and complete ionization in the depletion region, the Poisson equation (4.3) yields the following equation [1]:

$$\frac{d^2V}{dx^2} = \left(\frac{dE}{dx}\right) = \begin{cases} \dfrac{qN_A}{\varepsilon_s} & -x_p \le x \le 0 \\ -\dfrac{qN_D}{\varepsilon_s} & 0 \le x \le x_n \\ 0 & x \le x_n \; and \; x \ge \; x_n \end{cases} \tag{4.10}$$

where x_p and x_n represent the depletion layer widths in the p and n regions, respectively. By integrating Eq. (4.10), the electrical field can be written as [1].

$$E(x) = -\frac{qN_A(x_p + x)}{\varepsilon_s} \qquad for \; -x_p \le x \le 0 \tag{4.11}$$

$$E(x) = -\frac{qN_D(x_n - x)}{\varepsilon_s} \qquad for \; 0 \le x \le x_n \tag{4.12}$$

The relationship between the electric field and the potential *V* can be expressed as $E(x) = -\frac{dV}{dx}$. Therefore, integrating Eq. (4.11) and Eq. (4.12) yields [1]:

$$V(x) = \frac{qN_A}{2\varepsilon_s}\left(x_p + x\right)^2 \qquad for \; -x_p \le x \le 0 \tag{4.13}$$

$$V(x) = V(0) + \frac{qN_D}{\varepsilon_s}\left(x_n x - \frac{x^2}{2}\right) \quad for\ 0 \le x \le x_n \tag{4.14}$$

Therefore, from Equation (4.13), the potential across the p-region can be expressed as:

$$\mathrm{V}_p = \frac{qN_A {x_p}^2}{2\varepsilon_s} \tag{4.15}$$

and from Equation (4.14), the potential across n-region can be expressed as:

$$|\mathrm{V}_n| = \frac{qN_D {x_n}^2}{2\varepsilon_s} \tag{4.16}$$

Thus, the built-in voltage can be described as [1]:

$$V_{bi} = \mathrm{V}_p + |\mathrm{V}_n| = V(x_n) = \frac{E_m}{2}\left(x_p + x_n\right) \tag{4.17}$$

where

$$|E_m| = \sqrt{\frac{2qN_A \mathrm{V}_p}{\varepsilon_s}} = \sqrt{\frac{2qN_D|\mathrm{V}_n|}{\varepsilon_s}} \tag{4.18}$$

Owing to the continuity of the electrical field at the junction interface, the following should be noted:

$$N_A x_p = N_D x_n \tag{4.19}$$

By using Eq. (4.17) and (4.19), the depletion width on either side (x_p and x_n) can be calculated as follows [1]:

$$x_p = \left(\frac{2\varepsilon_s V_{bi}}{q}\frac{N_D}{N_A(N_A+N_D)}\right)^{\frac{1}{2}} \tag{4.20}$$

and

$$x_n = \left(\frac{2\varepsilon_s V_{bi}}{q}\frac{N_A}{N_D(N_A+N_D)}\right)^{\frac{1}{2}} \tag{4.21}$$

Hence, the width of the space charge (W) in the p-n junction can be written as [1]:

$$W = x_p + x_n = \left(\frac{2\varepsilon_s V_{bi}}{q}\frac{N_A+N_D}{N_A N_D}\right)^{\frac{1}{2}} \tag{4.22}$$

According to this equation, the depletion width relies on the doping density of the lightly doped side. For example, if $N_A >> N_D$, then $W = \left(\frac{2\varepsilon_s V_{bi}}{qN_D}\right)^{\frac{1}{2}}$. Therefore, it is concluded that a larger fraction of the depletion region is located on the side of the junction with lower doping (in this case, the n-side of the junction).Such a structure is known as a one-sided abrupt p–n junction [1, 4].

4.2 P-N Junction Under Bias Conditions

The equilibrium condition of a p-n junction may be disturbed if an external bias voltage is applied between the n and p regions. This allows charge carriers to flow through the junction. A current flow will be determined by the polarity of the

applied external biases, which can either be forward or reverse bias conditions. By applying a reverse bias voltage, charge carriers (electrons and holes) are pushed away from the junction, resulting in difficulty in crossing the depletion region. Figure 4.2 shows the differences in the band structure of a p-n junction in the absence and presence of external bias. Figure 4.2(a) illustrates that the Fermi energy at zero bias is constant across the junction. Applying a forward bias voltage to the junction as shown in Figure 4.2(b), the potential barrier across the junction decreases to $(V_{bi} - V)$ and the width of depletion decreases. Therefore, high current flows through the junction. Consequently, the Fermi level on the n side E_{Fn} is shifted down by half its value at equilibrium, while the Fermi level on the p side E_{Fp} does reverse. In the case of a reverse bias voltage, the Fermi level of the n region shifts lower than the Fermi level of the p region, as shown in Figure 4.2(c) Thus, the potential barrier $(V_{bi} + V)$ increases and the depletion width expands, resulting in a reduction of the flow of current through the junction, meaning that for a reverse-bias condition, the current flows only by thermal effects.

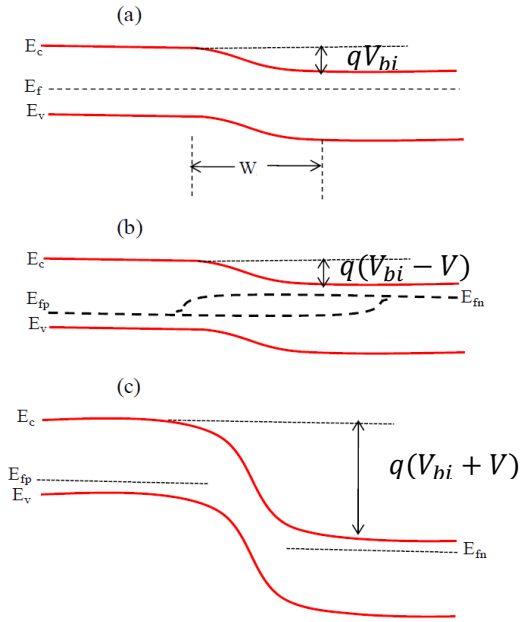


Figure 4.2: Schematic diagram of the energy band structure of a p-n junction under (a) zero-bias, (b) forward bias, and (c) reverse bias conditions.

By neglecting the voltage drop in p and n quasi-neutral regions, and modifying the solution of the Poisson's equation at zero bias given in Equation (4.22) by replacing V_{bi} with $(V_{bi} \pm V)$, one can obtain the depletion width for abrupt junction under bias condition as expressed by :

$$W = \left(\frac{2\varepsilon_s(N_A + N_D)}{qN_AN_D}(V_{bi} \pm V)\right)^{\frac{1}{2}} \tag{4.23}$$

4.2.1 Depletion Layer Capacitance

The depletion capacitance of the space charge region is one of the key parameters for studying and understanding p-n junctions. Measurements of capacitance as a function of reverse-bias voltages are used to determine the built-in potential of junctions. Additionally, the capacitance-voltage analysis is one of the most common methods used to estimate the carrier density profile in Schottky diodes and p-n junctions. In a p-n junction, there is a double layer of hole and electron charge carriers separated by a depletion region, so it is comparable to a parallel plate capacitor. Therefore, its associated capacitance is given by [5].

$$C = \frac{dQ}{dV} = \frac{d(qN_Ax_p)}{dV} = \frac{d(qN_Dx_n)}{dV} \tag{4.24}$$

where, dQ is the depletion region charge and dV is the applied voltage. Moreover, the capacitance may also be expressed as a function of the junction depletion width, W, as follows:

$$C = \frac{A\varepsilon_s}{W} \tag{4.25}$$

Here, A is the area of the diode, ε_s is permittivity and W is the depletion region width. Thus, by assuming $N_A \gg N_D$ and using Equations (4.24) and (4.25), the one side abrupt junction capacitance for a reverse bias condition can be written as follows:

$$C = \frac{dQ}{dV} = \frac{A}{2}\left[\frac{2\varepsilon_s q N_D}{V_{bi} \pm V}\right]^{1/2} \tag{4.26}$$

Based on Equation (4.26), it is apparent that the capacitance of the diode decreases as the reverse bias increases. As a result, if the inverse of the capacitance square, ($1/C^2$) is plotted as a function of the applied voltage, V, a linear relationship is found as shown in Figure 4.3. The doping concentration, N_D, in the lightly doped semiconductor can be obtained from the slope of the line and the x-intercept of the line (at $1/C^2 = 0$) indicates the built-in potential across the junction.

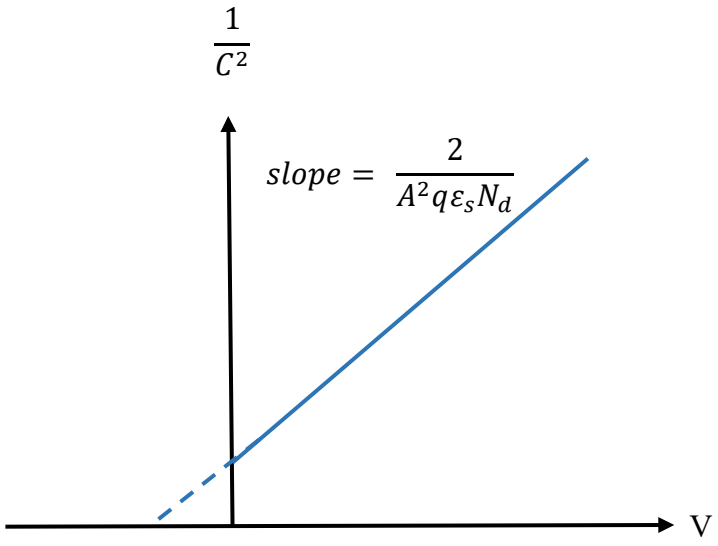


Figure 4.3: A typical plot of ($1/C^2$) versus applied reverse-bias voltage.

4.3 Current- Voltage Characterisation

The I-V characteristics of an ideal Schottky or p-n junction can be described by the thermionic emission model that includes series resistance (R_s) as follows:

$$I = I_s\left[exp\left(\frac{q(V - IR_s)}{nK_BT}\right) - 1\right] \tag{4.27}$$

In this equation, q is the electronic charge, V is the applied voltage, K_B is the Boltzmann constant, n is the ideality factor, I_s is the saturation current, and T is the absolute temperature in Kelvin. Experimental data is used to derive the values of n and I_s. In general, the saturation current I_s is expressed as:

$$I_s = AA^{**}T^2 exp\left(\frac{-qV_{bi}}{K_BT}\right) \tag{4.28}$$

where A is the diode area, A^{**} is the effective Richardson's constant for a semiconductor material, and V_{bi} is the junction potential. Under forward bias condition, for $V - IR_s >> K_BT$, the thermionic diode current is given by

$$I = I_s exp\left(\frac{q(V - IR_s)}{nK_BT}\right) \tag{4.29}$$

A first derivative of I with respect to V (Equation (4.29)) gives the following result:

$$\frac{dI}{dV} = I_s\left(\frac{q}{\boldsymbol{n}K_B\boldsymbol{T}} exp\left(\frac{q(V - IR_s)}{nK_BT}\right) - \frac{q}{nK_BT} exp\left(\frac{q(V - IR_s)}{nK_BT}\right) R_s \frac{dI}{dV}\right) \tag{4.30}$$

$$G = \frac{q}{nK_BT} I_0\, exp\left(\frac{q(V - IR_s)}{nK_BT}\right)(1 - G.R_s) = \frac{q}{nK_BT} I\,(1 - G.R_s) \tag{4.31}$$

Note that $dI/dV = G$ (the conductance) and rearranging the terms, the following form is obtained:

$$\frac{G}{I} = \frac{q}{nK_BT} - \frac{qR_s}{nK_BT}G \tag{4.32}$$

As shown in Figure 4.4, plotting G/I vs G, values of n and R_s can be determined from the y-intercept and slope, respectively. This experimental method for extracting n and R_s is known as Werner's method [6].

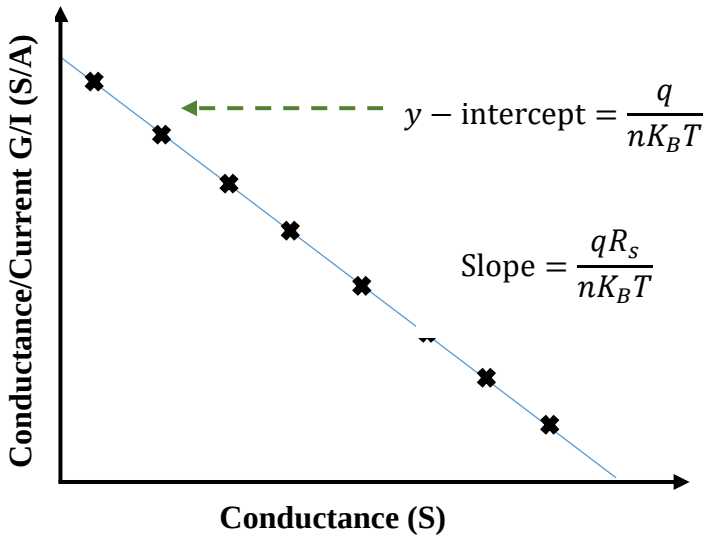


Figure 4.4: A typical plot of $G//$ versus G used for extracting the diode parameters using the I-V characteristics.

By taking the logarithm of Equation 4.27 and plotting $\ln(I)$ versus$(V - IR_s)$, I_s could be extracted from the y-intercept.

$$\ln(I) = \ln(I_s) + \frac{q(V - IR_s)}{nK_BT} \qquad (4.32)$$

Then, by substituting I_s value in Equation (4.28) where A, A^{**} and T are known, and V_{bi} can be calculated.

4.4 Deep Level Transient Spectroscopy Technique (DLTS)

There are a number of widely used techniques in the study of deep level defects in semiconductors, which are based on microscopic defect analysis [7]. A technique that is among these is Deep Level Transient Spectroscopy (DLTS). It is a powerful microscopic tool that can characterise the deep levels in semiconductors via the observation of the charge carriers emission from traps [8]. DLTS was discovered by Lang in 1974 [9]. This technique uses the concept of space charge capacitance to determine the activation energies of defects, based on the variation of depletion width as a function of temperature. It is employed to investigate defects, their activation energy, concentration, and consequential effects in semiconductor materials and devices.

4.4.1 Capacitance Transients

The DLTS method measures the capacitance transients resulting from a change in the space charge region, which requires a Schottky diode or a p-n junction device. Figure 4.5 shows the variation of the charge occupancy at a defect level in a Schottky diode under different bias conditions. The DLTS technique relies on applying a bias pulse periodically to the diode with a fixed frequency in order to disturb the occupancy of the defects and to improve the signal to noise ratio. In this work, the pulses are repeated between reverse bias V_R and filling bias V_P (where $V_P < V_R$) with a given filling pulse width t_p.

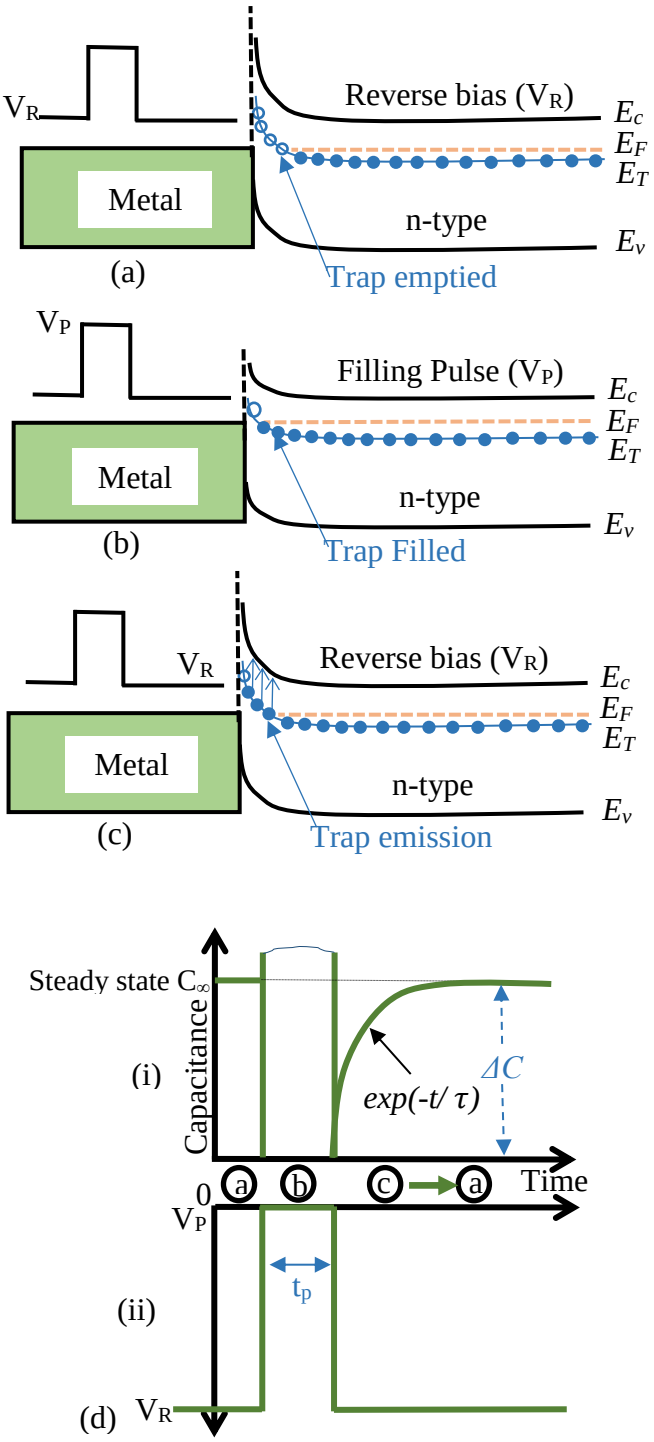


Figure 4.5: Energy band diagrams of a Schottky diode illustrating the charge occupancy changes of the defects level during (a) emptying of traps at $V=V_R$ bias condition, (b) filling of traps with filling pulse $V=V_P$, and (c) thermal emission of electrons due to the increase in the temperature at $V=V_R$. (d) DLTS pulse and the corresponding capacitance transient. t_p and E_T represent a pulse width and a trap energy level.

As illustrated in Figure 4.5, at a stage (a), the junction is initially exposed to a reverse bias V_R and a space charge region is formed. Traps above the Fermi level are empty of charge carriers. At stage (b), a filling pulse V_P is applied. This technique causes the depletion width to become smaller. Therefore, when the electrons leave the conduction band they will flow to the region that was previously depleted of carriers. Within this region, the traps will begin to capture these electrons (filled with carriers). In a pure capturing process (no emission of charge carriers) from the kinetics of capture (Equation 3.6, Chapter 3), the rate equation for the density of filled traps is as follows:

$$\frac{dn_T}{dt} = c_n(N_T - n_T) \tag{4.33}$$

where c_n, N_T and n_T represent the electron capture coefficient, the total number of trap states, and the number of trap states occupied by electrons, respectively. The electron capture coefficient is a mathematical function expressed as follows:

$$c_n = \sigma_n < v_{th} > n \tag{4.34}$$

where σ_n and $\langle v_{th} \rangle$ are the capture cross-section and thermal velocity of electrons. $n = N_d - N_T \cong N_d$ is the effective doping concentration.

When a long enough duration filling pulse (t_p) is applied, the traps will completely be filled by electrons so that $n_T = N_T$. However, at stage (c), after the reverse bias is re-established the depletion region moves back to its original width, and the filled

traps will start to emit the carriers. The corresponding emission rate can be given from the kinetics of emission process by:

$$\frac{dn_T}{dt} = e_p N_T - n_T(e_n + e_p) \tag{4.35}$$

where e_n and e_p represent electron emission and hole emission, respectively.

Assuming that the deep level is only an electron interacting centre, then the time dependences of n_T during the capture and emission processes (Equations (4.33 and 4.35)) can be calculated respectively as follows [2]:

$$n_T(t) = N_T\{1 - \exp(-c_n t)\}, \quad c_n \gg e_n, e_p, c_p \tag{4.36}$$

and

$$n_T(t) = N_T \exp\left(\frac{-t}{\tau}\right), \quad e_n \gg c_n, e_p, c_p \tag{4.37}$$

where c_p is the capture coefficient of holes and τ is the inverse of the electron emission rate, i.e. $\tau = \frac{1}{e_n}$.

According to the above equation, the reduction of the filled trap concentration is exponential with a time constant τ and gives rise to a capacitance transient as demonstrated schematically in Figure 4.5(d).

Indirectly, the variation of the occupancy of traps can be measured by monitoring the changes in capacitance at the junction. Therefore, Equation (4.26) can be rewritten with the added contribution of filled traps in the space charge region.

$$C = \frac{dQ}{dV_R} = \frac{A}{2}\left[\frac{2\varepsilon_s q N_D^*}{V_{bi} + V_R}\right]^{1/2} \tag{4.38}$$

where $N_D^* = N_D - n_T$. and $n_t \ll N_D$.

The steady state capacitance is defined as $C_\infty = \frac{A}{\sqrt{2}}\left[\frac{2\varepsilon_s q N_D}{V_{bi}+V_R}\right]^{1/2}$

Then, the amplitude of the capacitance transient can be expressed as:

$\Delta C = C - C_\infty$ which can be expanded as follows

$$\Delta C = C_\infty\left(1 - \frac{\mathrm{n}_T}{2N_D}\right) \tag{4.39}$$

The information about the time dependence of the capacitance for majority carrier traps emission can be obtained by substituting Equation (4.37) in Equation (4.39):

$$\Delta C = C_\infty\left[1 - \frac{N_T}{2N_D}\exp\left(-\frac{t}{\tau}\right)\right] \tag{4.40}$$

Therefore, it is possible to determine the deep level trap concentration and electron emission rate by measuring the amplitude of the capacitance transient and the time constant, respectively. The trap emission process and corresponding change in the capacitance in time scale is presented in Figure 4.5 (d). Moreover, it is worth noting that the sign of the capacitance transient in minority carrier traps is the opposite of that of majority carrier traps.

4.4.2 Conventional DLTS

The DLTS technique principle [9] relies on perturbing the occupancy of the deep states and measuring the change in capacitance ΔC between two points in time t_1

and t_2 ($t_2 > t_1$) due to carrier capture and emission. In the process, this transient is measured as a function of temperature, T, leading to the production of a DLTS spectrum, which provides information regarding trap parameters such as the activation energy, E_T, the cross section, σ, and density, N_T. According to Equation (4.40), the DLTS output signal, $S(T)$, can be expressed mathematically as follows:

$$S(T) = C(t_1) - C(t_2) = \Delta C_\circ \left[exp\left(-\frac{t_2}{\tau}\right) - exp\left(-\frac{t_1}{\tau}\right) \right] \qquad (4.41)$$

where $\Delta C_\circ$ is the change in the capacitance at time $t = 0$, and is given by:

$$\Delta C_\circ = \frac{C_\infty N_T}{2N_D} \qquad (4.42)$$

where N_T is the trap concentration and C_∞ is the capacitance at a maximum reverse bias (when the trap is empty). $S(T)$changes as the emission rate e_n changes with temperature as shown in Figure 4.6 (a). The DLTS signal will be small in the case of $\tau \ll (t_1 - t_2)$ and $\tau \gg (t_1 - t_2)$, whereas it will be maximum in the case of $\tau \approx (t_1 - t_2)$. The maximum signal can be obtained for $S(T)$ (maximum emission) by using $\frac{dS(T)}{d\tau} = 0$. This produces the equation for the rate window and is equal to the maximum amplitude of the DLTS signal.

$$\tau = \tau_{max} = \frac{(t_1 - t_2)}{ln\left(t_1/t_2\right)} \qquad (4.43)$$

Therefore, by changing the rate window value, τ, i.e. by changing the value of two measurement times t_1 and t_2, the DLTS peaks are shifted to higher temperatures as shown in Figure 4.6 (b). The Arrhenius plot of the emission rates as a function of temperature is used to determine the trap activation energy, as shown in Figure 4.6 (c). The activation energy, E_T, and apparent capture cross-section, σ_n, of the trap can be deduced from the slope and intercept of the Arrhenius plot, respectively. Additionally, the trap concentration, N_T, can be calculated through Equation (4.42), which is related to the conventional DLTS peak amplitude. As indicated by Equations (4.42) and (4.43), the maximum peak height of DLTS signal is independent of the absolute value of the time constants, t_1 and t_2 but is dependent upon the time constant ratio, (t_2/t_1). In the transient process, the change in capacitance is usually very small meaning that the DLTS measurements will be very sensitive to noise. Therefore, in order to improve the signal-to-noise ratio, the capacitance measurements are averaged over a large number of acquired capacitance transients. It is worth pointing out that by averaging a set of capacitance transients, the signal-to-noise ratio (SNR) will be increased, ideally in proportion to the square root of the number of measurements ($SNR=N^{1/2}$) .

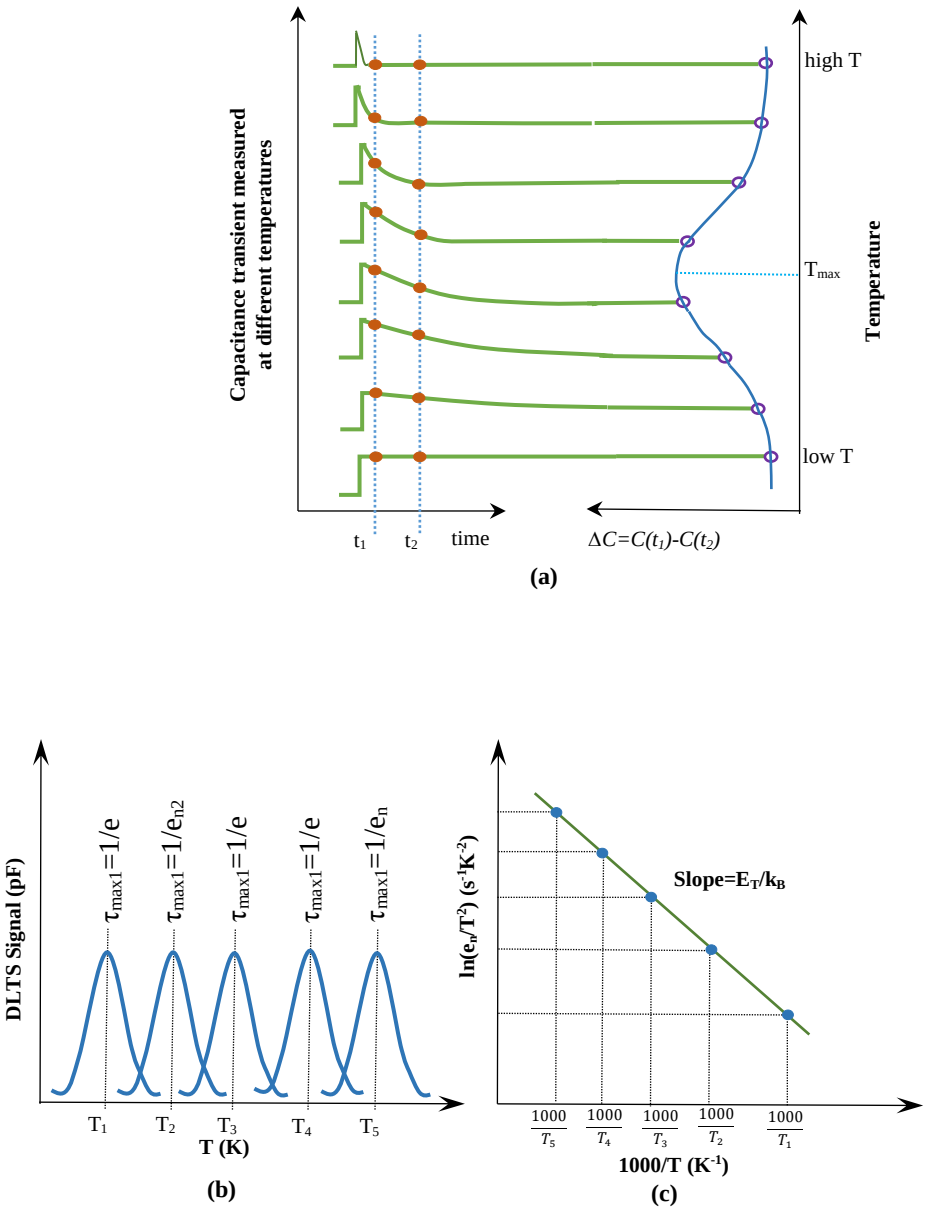


Figure 4.6: Schematic diagram of the DLTS signal generation process: (a) the right-hand side shows a consistent DLTS signal generated from the capacitance transient between two values of capacitance at t_1 and t_2 as a function of temperature; the left-hand side shows the capacitance transients as function of temperatures. (b) DLTS peaks for different rate windows. (c) Determination of activation energy of trap from Arrhenius plot.

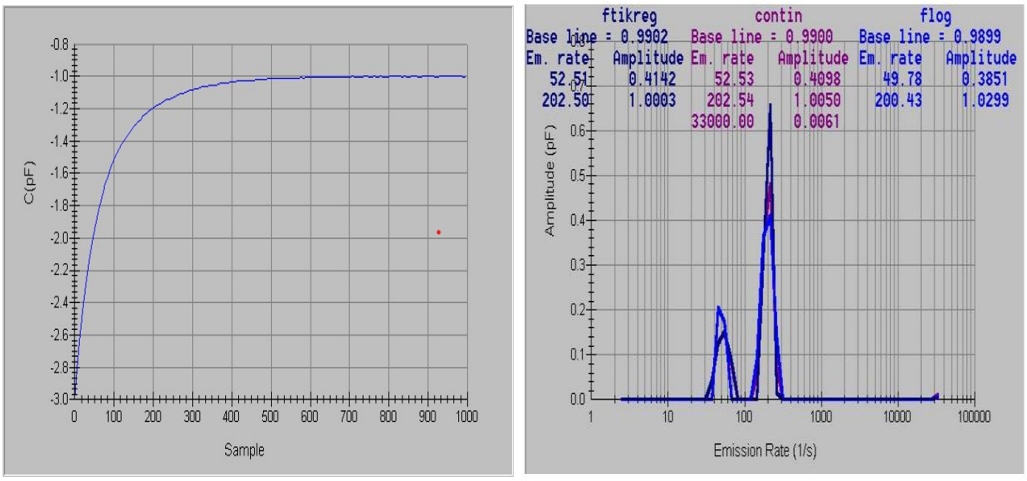
4.5 Laplace DLTS Spectroscopy

The conventional DLTS technique is commonly used to characterise the deep levels in semiconductor materials [9]. This technique is based on producing a sequence of peaks which depends on the temperature. These peaks are the result of the exponential behaviour of the emission transient from deep levels. Despite this, there are significant issues associated with the resolution of DLTS, which arise as a result of the scanning nature of the temperature. Among these challenges is the accuracy of the temperature measurements associated with thermal scanning, since the temperature of the diode changes continuously throughout the process. Thus, the ability to determine the activation energies will become less accurate. Furthermore, the difficulty of separating the time constants of exponential emission transients from different defect states leads to a broadening of the DLTS spectra peak [10].

For these reasons, to overcome the limitations of the conventional DLTS, a mathematical method called Laplace Inversion has been developed to extract the emission spectrum F(s) from a transient capacitance signal. The type of DLTS using these mathematical methods is known as Laplace DLTS (LDLTS). This technique is based on the fact that the transient capacitance is averaged and measured at a fixed temperature, meaning that LDLTS is an isothermal technique [10, 11]. A further advantage of this technique is that it converts the DLTS signal from a time domain to a frequency domain. In an attempt to increase the signal-to-noise ratio, different digital schemes are employed in order to digitize and average the analogue output of the capacitance meter during the emission process [12]. According to the Laplace equation, the LDLTS transient can be expressed mathematically as follows:

$$f(t) = \int_0^{\infty} F(s)e^{-st}ds \qquad (4.44)$$

where $f(t)$ is the recorded transient (time domain) and $F(s)$ is the spectral function (frequency domain). So $f(t)$ is the Laplace transform of the true spectral function $[F(s)]$. An example of a capacitance transient can be seen in Figure 4.7 (a). Using mathematical algorithms that apply the inverse Laplace transform for the function, it is possible to get a spectrum of emission rates, $f(t)$that determine the spectra of the emission rates. In the Laplace technique, three mathematical algorithms have been implemented for Laplace Inversion $f(t)$: FLOG, CONTIN, and FTIKREG. However, only one routine is employed for data processing. These algorithms all use the Tikhonov regularisation method. Each of them, however, uses a different principle to determine and define the regularisation parameters. The CONTIN [13] and FTIKREG) algorithms [14, 15] codes, generated by Queen's University of Belfast's Computer Physics Communication (CPC), were incorporated in the DLTS software (see section 4.6.6) developed by a joint project "Copernicus Project CIPA CT-94-0172 and the Foundation for Polish Science Serial No: C3.2.041". These two algorithms have been adapted for use in the Laplace DLTS system. However, the last algorithm (FLOG) has been specifically developed for the system. Additionally, it is important to note that the parallel implementation of three numerical algorithms increases the confidence level in the calculated spectra. Moreover, this technique produces very well-defined, delta-like peaks spectra for multi exponential transients as a function of emission rates, as shown in Figure 4.7 (b). Furthermore, the trap concentration can be found from the area under the peaks of LDLTS signal. Hence, the precision of the characterization of defects increases [11].



(a) (b)

Figure 4.7: (a) Diagram of the capacitance transient using Laplace DLTS at fixed temperature (time domain); (b) delta-like peaks spectra output (frequency domain) related to two emission rates obtained from the capacitance transient with the use of three numerical routines.

4.6 DLTS Hardware Setup

Details of the equipment used for the DLTS and I-V measurements are discussed in this section. The equipment involved in the DLTS system includes the following components: cryostat and temperature controller, capacitance meter, current-voltage source meter, data acquisition and BNC connector box for analogue Input (I)/Output (O). These apparatuses are all controlled by a computer with a GPIB interface over a network. Figure 4.8 shows an experimental photograph of the DLTS system. The block diagram of the DLTS configuration is shown in Figure 4.9.

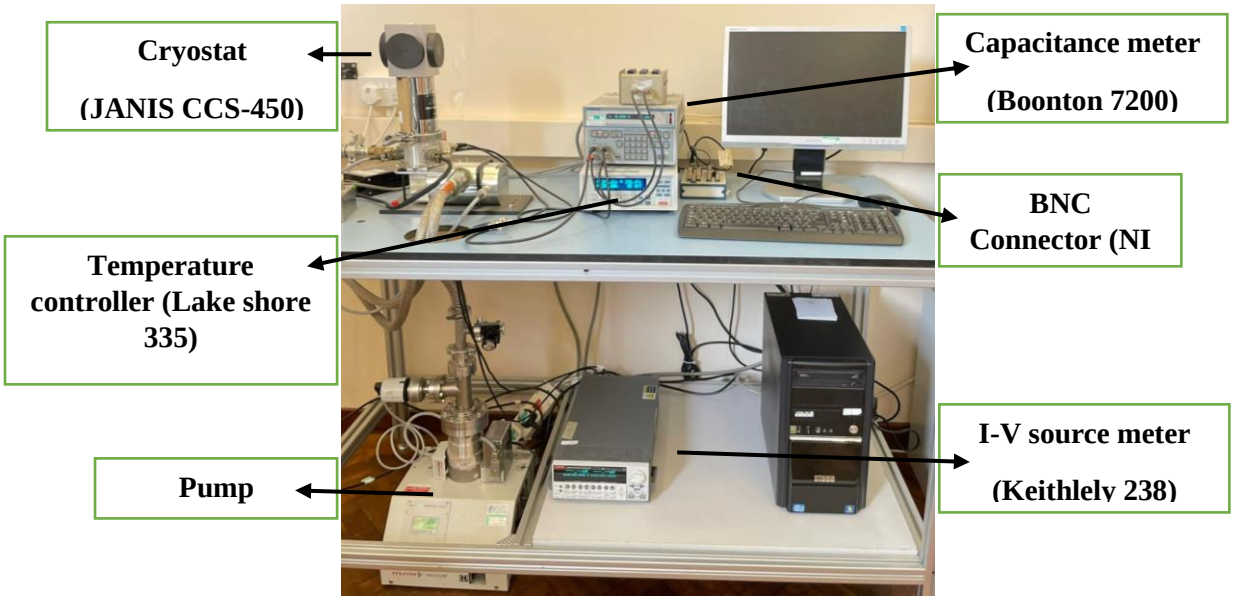


Figure 4.8: Photograph of the DLTS system.

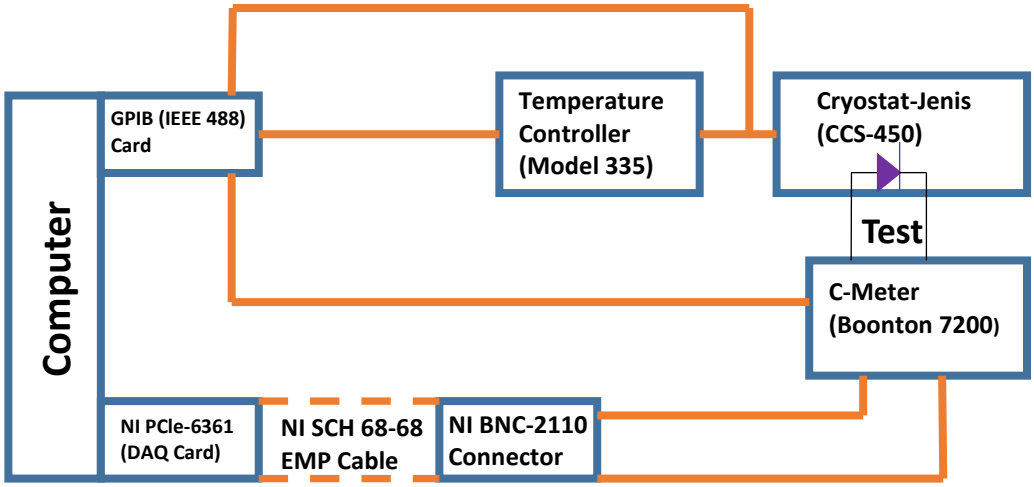


Figure 4.9: Schematic diagram of the DLTS system showing the different components which are discussed in sections 4.6.1 to 4.6.6.

4.6.1 Cryostat And Temperature Controller

Since the process of emitting charge carriers from the traps depends on the thermal energy, the DLTS and Laplace DLTS measurements are carried out using a cryostat (model Janis CCS-450) and a temperature controller (Model Lake Shore 335) to control the sample temperature. This temperature controller controls two temperature sensors, one of which is mounted very close to the sample for accurate temperature measurement. Figure 4.10 shows the internal structure of the cryostat. Specifically, this system includes a sample holder attached to a cold finger, thermal sensors, electrical ports, a radiation shield, and an aluminium vacuum shroud. The cryostat is powered by a compressor that is fitted with a closed-cycle refrigeration system that provides helium gas (He) through a flexible 6 feet long cryogen transfer line. This cryostat, which is controlled by Lake Shore 335, operates at temperatures ranging from 10 K to 450 K with a level of stability of 1 K.

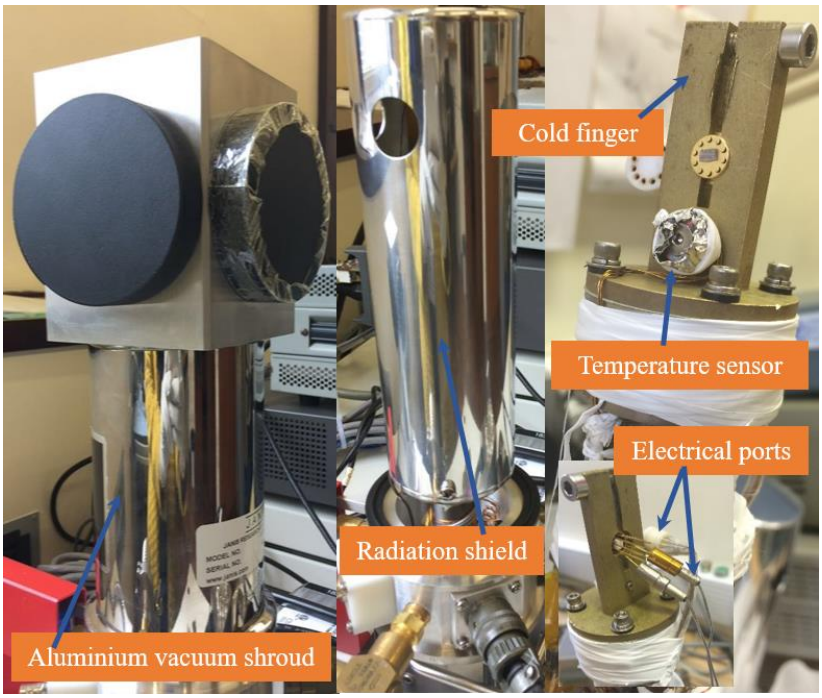


Figure 4.10: Photograph showing different components f the cryostat.

4.6.2 Capacitance Meter

Capacitance meters which have a fast response time are essential for the measurements of capacitance transients. In this work, the Boonton 7200 meter, which has a response time of ~120 μs, was employed. Moreover, it has a fixed sampling frequency of 1 MHz which is high enough to avoid parasitic effects but low enough to avoid the influence of surface states.

4.6.3 Current-Voltage Source Meter

The I-V measurements of each sample in this thesis were carried out at a variety of temperatures to determine the diode parameters such as ideality factor (n), junction potential (V_{bi}), and series resistance (R_s). Additionally, for DLTS and Laplace DLTS measurements, a low reverse current is required, and thus I-V measurements are performed to check the suitability of the devices. The I-V measurements were performed using a Keithley 2602A current source meter, which was connected to a computer using a GPIB interface in order to provide a source voltage in the range of 100 μV to 110 V with a sensitivity of ±10 μV and a source current in the range of 100 fA to 100 mA, with a sensitivity of 10 fA.

4.6.4 Data Acquisition And BNC-2100 Connector

The data acquisition card is a key element of the DLTS technique for biasing and pulsing the diodes. Data acquisition (DAQ) card from National Instruments (NI) is used. By using this card, input voltage can be applied up to ± 10.0 V and with pulse width from 0.5 μs. The SHC68-68-EPM adapter is used to interface the NI card with the BNC-2110 connector box. The BNC-2110 connector box transmits data from the diode to the computer for processing.

4.6.5 Computer Interface

General-purpose interface bus (GPIB) is used to connect all the equipment in the experimental setup with the computer and to control them remotely through software.

4.6.6 System Software

Laplace DLTS software was developed by a joint project "***Copernicus Project CIPA CT-94-0172 and The Foundation for Polish Science Serial No: C3.2.041***" between University of Manchester, Manchester, United Kingdom (Professor A. R. Peaker) and Institute of Physics of the Polish Academy of Sciences, Warsaw, Poland (the late Professor L. Dobaczewski). This purchased commercial software functions in two modes, namely conventional DLTS and Laplace Transient processing (Laplace DLTS) mode.

4.7 Conventional DLTS Mode

The conventional DLTS measurement mode, has three different types of procedures, which use the concept of a rate window, namely Multi-Rate Window, TrapView, and Exponential Fitting. The sample is scanned from a start to end points of temperatures with increasing steps (usually 2 K/minute) in each one of these three procedures.

In the "Multi-Rate" mode nine different rate windows can be used, namely 5 s^{-1}, 10 s^{-1}, 20 s^{-1}, 50 s^{-1}, 100 s^{-1}, 200 s^{-1}, 500 s^{-1}, 1000 s^{-1} and 2000 s^{-1}. In the "TrapView" mode, one pair out of 5 different pairs of rate windows can be selected at a time: (4, 10 s^{-1}), (20, 50 s^{-1}), (80, 200 s^{-1}), (400, 1000 s^{-1}) and (2000, 5000 s^{-1}). In contrast, only one rate window can be used with the "Exponential Fitting" mode. The

Arrhenius plot is obtained when the measurement is run in the "Exponential Fitting" mode. As a result, defects activation energies and capture cross-sections can be estimated. It is also possible to use this mode in lock-in mode, which has better resolution than the rate window mode. However, lock-in mode has a poor signal to noise ratio.

4.7.1 Laplace Transient Processing (Laplace DLTS) Mode

In this mode, the temperature of the sample is fixed during measurement. Generally, this mode is used to increase the signal to noise ratio. Three different algorithms are applied to generate Laplace DLTS peaks as discussed in section 4.5.

4.8 Luminescence Techniques: Photoluminescence (PL), Electroluminescence (EL) And Cathodoluminescence (CL)

Luminescence spectroscopy is one of the most powerful techniques for characterization of semiconductors, especially those that are suitable for optoelectronic devices. The technique is nondestructive and is capable of yielding information on the properties of semiconductors such as electronic structure, bandgap energy, defect states, and other properties. Additionally, it is sensitive to impurities and defects that affect the quality of materials and the performance of devices. Luminescence is the process of light emission after some energy was absorbed by the material. There are three ways to excite a sample to cause luminescence, namely Photoluminescence (PL), Electroluminescence (EL) and Cathodoluminescence (CL) techniques. PL is one of many types of luminescence which is the emission of light from a material that is not heated. Thus, PL is the emission of light caused by photon absorption. PL spectroscopy is a powerful and

non-destructive method which is commonly used for investigating optical properties of semiconductor materials [2]. During an optical investigation, a sample is exposed to an optical source, such as a laser, with an energy greater than that of the material bandgap ($hv > E_g$). The light from the laser source (photons) is absorbed and the excess energy is transferred to the material in a process known as photo-excitation. Then, the material will emit the excess energy in the form of light known as PL spectrum. The intensity and the spectral content of the PL spectrum are used to obtain important information about the material properties, such as the bandgap, impurity energy levels and the quality of the material. In the photo-excitation process, the electrons are excited to higher states and then relax back to their equilibrium states losing the difference in energy (between the excited and equilibrium states) in the form of light in a process called radiative recombination. However, a non-radiative process occurs when the difference in the energy is lost as heat. Figure 4.11 shows the excitation of electrons, where non-equilibrium electrons tend to relax back into the equilibrium state (inter-band relaxation to band edge) and finally this is followed by emission of light due to an electron-hole radiative recombination.

The luminescence processes occurring in CL and EL measurements are, in principle, the same as those present in standard PL measurements. However, CL results from the excess carriers generated by an electron beam (e-beam) and EL occurs from the excess carriers that are generated by current injection (electric current).

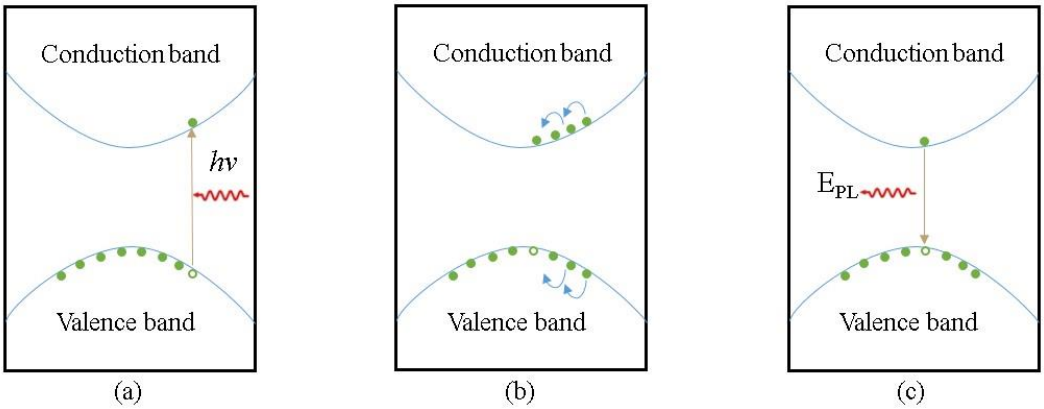


Figure 4.11: Illustration of the processes involved in PL (a) photo-excitation from the valence band to the conduction band, (b) inter-band relaxation and (c) recombination, which leads to PL emission.

4.9 Raman Spectroscopy

Raman spectroscopy technique is used in order to investigate various properties of materials, such as chemical structure and crystallinity. There are two processes involved in Raman spectroscopy, namely Rayleigh and Raman scattering. Rayleigh scattering is an elastic process where the incident photon is of the same energy as the scattered photon. Raman scattering is based on the inelastic scattering of light (Raman scattering) with the scattered light having a different wavelength from the incident light. Almost all of the scattered light from a semiconductor is unchanged in wavelength when illuminated by monochromatic light. However, only a small amount of the scattered light has a different wavelength than the incident wavelength. As the scattered light loses energy (has less energy than the incident light), the phenomenon is called Stokes scattering. It is, however, called anti-Stokes scattering if the scattered photon has a higher energy. As a result of the difference in energy, a change in vibrational energy occurs within the molecule that absorbs the light. The Raman spectrum is a plot of scattered light intensity versus frequency

that indicates at which energies the scattered light has been scattered. In this spectrum, peaks are generated where their position and intensity can be used to identify the material under investigation [16, 17]. The schematics of the Stokes and anti-Stokes Raman scattering are shown in Figure 4.12

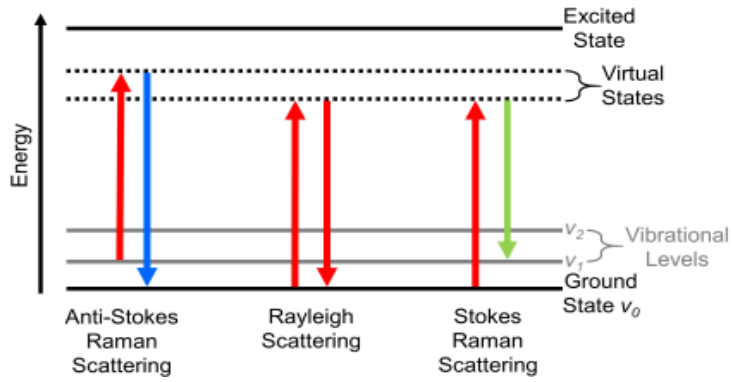


Figure 4.12: Schematic diagram of energetic transitions involved in Raman scattering. Rayleigh scattering, Stokes scattering and anti-Stokes scattering [18].

4.10 Photocurrent Spectroscopy

Photocurrent spectroscopy technique measures the photoexcited current in response to the incident photon energy, thus allowing the study of semiconductor electronic structures. In this technique, charge carriers are generated by an externally applied electric field in a photoconductor that is excited by a continuous stream of photons. The photocurrent is generated using a monochromatic light beam, where the incident light is modulated by a mechanical chopper. The modulated light is then focused onto the sample, generating a photocurrent signal, which is filtered and detected by a lock-in amplifier. By analysing this data, important information about the efficiency of the device in converting light into electrical energy, as well as its response to light of different energies can be obtained. The use of photocurrent spectroscopy provides a valuable tool for the

development and optimization of photovoltaic devices and contributes to understanding semiconductor physics and materials science [19].

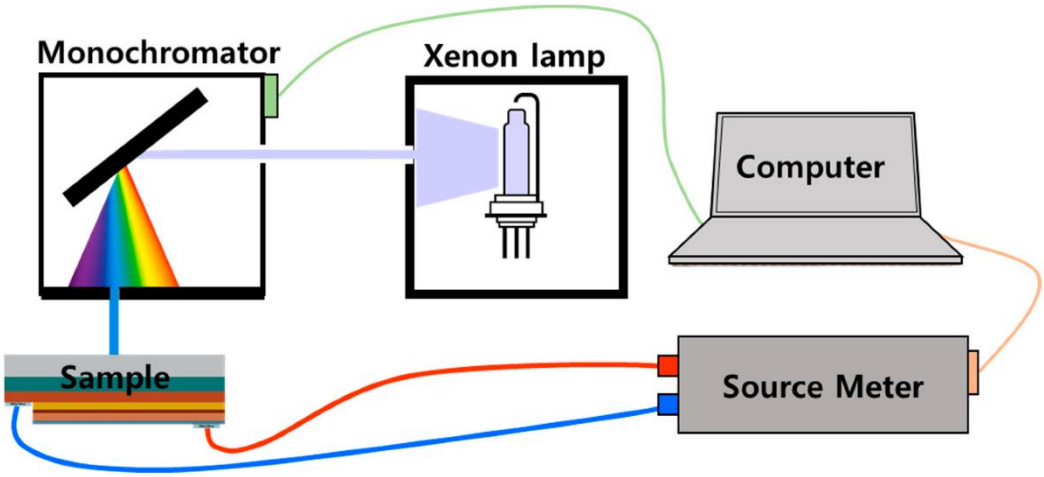


Figure 4.13: Schematic diagram of Photocurrent spectroscopy [20].

4.11 Scanning Transmission Electron Microscopy (STEM)

Scanning transmission electron microscopy (STEM) is a technique that provides imaging and morphological characterization at the atomic level. STEM systems use a beam of electrons that is converged (with a maximum convergence angle) to a small probe of electrons. The probe scans across the sample or specimen, producing an image in series, pixel by pixel, as a function of the probe's position on the sample. Due to the raster (scanning) of the probe, image acquisition is slower than in TEM. The resolution of images is governed by the size of the electron probe (smaller is better) and the beam current (higher is better) [21]. The High-Angle Annular Dark-Field (HAADF) imaging technique shown in Figure 4.14 detects electrons scattered by a sample at high angles after focusing STEM beam. During HAADF imaging, a beam of high-energy electrons is focused onto the sample, and the electrons that scatter at high angles are collected by HAADF detector positioned

at a high angle to the incident beam. By scanning the beam across the sample, a high-resolution image can be formed from the intensity variations in the collected electrons. HAADF imaging is particularly useful for imaging elements in a sample [22, 23]. STEM can be also combined with Energy-dispersive X-ray spectroscopy (EDX). EDX is the generation of X-rays from a sample through an electron beam. X-rays are generated by the characteristics and nature of the elements in the sample. In this way, X-ray energy can be measured. The EDX analysis uses an electron beam to bombard a sample, which emits characteristic X-rays [24]. X-ray data can be used to create an elemental map that shows the distribution of compounds or elements across a sample surface. The map is usually displayed as a false-colour image, with different colours representing different elemental intensities [24]. An EDX map can be used to identify specific areas of the sample containing high concentrations of a particular element or compound.

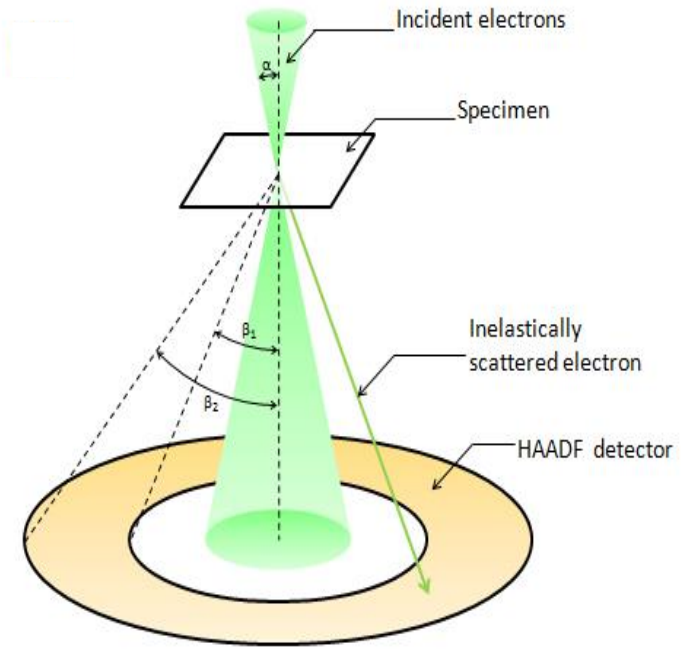


Figure 4.14: Schematic diagram of the HAADF- STEM technique [25].

4.12 Silvaco Technology Aided Design (TCAD) Simulation

Silvaco TCAD (technology computer aided design) software is generally used to model semiconductor devices under operating conditions and to understand the transport mechanisms. It works by solving a set of mathematical equations that describe the physical behaviour of electrons and holes in inorganic semiconductor and other charge carriers like polarons and excitons in an organic semiconductor. The simulation is typically performed in a step-by-step manner, where the device structure is first defined and the material optical, electrical and electronic properties are specified. After that, the electrical properties of the device are modelled using numerical solutions to fundamental partial differential equations. The simulator software uses three partial differential equations, the Poisson's equation and the holes and electrons equations of continuity. Once the device parameters are set, the simulation is run to calculate the electrical and physical behaviour of the device, such as the current and capacitance as a function of voltage and frequency, respectively. After that, the output data extraction can be achieved using two methods, the first is the extraction as data file and the other type is through Figures [26] depending on the transport mechanism investigated.

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CHAPTER 5: EXPERIMENTAL DETAILS

The purpose of this chapter is to present the experimental details of the research reported in the thesis. In addition, a description of the conditions and the procedure used in the preparation of the samples used in this study. Moreover, the measurement equipment and the methods which were used to characterise the AlGaN/GaN, InGaN/GaN Multi Quantum Wells (MQWs) and NiO/Ga_2O_3 semiconductor materials investigated in this work, are discussed in the sections below.

5.1 Samples

These studies used samples of three different types of materials, AlGaN/AlGaN, InGaN/GaN MQW and NiO/Ga_2O_3 heterojunctions. AlGaN/AlGaN and InGaN/GaN MQW samples are electrically stressed in a controlled environment to observe the effects of stress on the electrical and optical properties of these samples. Electrical stress is the process of applying an electrical field to a semiconductor device in order to test its reliability. The electrical stress process is used to determine the device's ability to withstand electrical stress and to identify any potential failure mechanisms. For the NiO/Ga_2O_3 heterojunctions, the samples were annealed at 200 K in Argon gas environment to study the impact of annealing on the optical and electrical properties of these devices. Briefly these investigations are summarised below.

i. The effect of stress on $Al_{0.6}Ga_{0.4}N/Al_{0.5}Ga_{0.5}N$ MQW based deep ultraviolet LEDs.
ii. The effect of stress on $In_{0.01}Ga_{0.99}N/GaN$ MQW based UV photodetectors.

iii. The effect of Rapid Thermal Annealing (RTA) on NiO/Ga_2O_3 heterojunction diodes.

5.2 Measurement Details

Several key details about the measurement methods utilized in this study are presented in the sections that follow.

5.2.1 Current-Voltage (I-V) Measurements

The I-V characteristics of p-n diodes are measured after fabrication in order to determine whether they are of good quality and suitable for LDLTS or DLTS measurements. A figure of merit for DLTS measurements is very low reverse currents (~1μA). The I-V measurements were conducted with a Keithley 236 current-voltage source meter. The current is measured from -4 V to + 4 V with voltage steps of 0.1 V. The experimental values of reverse current at -4 V in all samples selected for DLTS measurements are in the range of 10^{-9} A to 10^{-5}A at room temperature.

5.2.2 Capacitance-Voltage (C-V) Measurements

The C-V measurements are important for obtaining the background doping concentration of the diodes. In addition, this parameter is also crucial to DLTS analysis in order to determine the trap concentrations. C-V measurements were performed with a Boonton 7200 capacitance meter operating at a fixed frequency of 1MHz.

5.2.3 DLTS Measurements

In this thesis, the DLTS technique, which is described in detail in Chapter 4, was used in order to investigate the electrically active defects in the devices examined. The samples were first mounted and bonded onto TO5 headers, which were placed on a holder within a He closed-loop cycle cryostat (JANIS CCS-450). The samples were first cooled to 10K, and then the temperature was ramped up at a rate of 2K/min from 10K to 450K (depending on the quality of p-n diodes), with a reverse bias (V_R) set at a chosen value. A transient capacitance is monitored by a Boonton 7200 capacitance meter during the temperature scan by applying a train of electrical pulses to the sample with a chosen filling pulse (V_P) value generated by an interface card from National Instruments. The change in capacitance transient is monitored by a computer in the form of a DLTS signal as a function of temperature.

5.2.4 Laplace DLTS Measurements

Laplace DLTS measurements were performed in order to resolve the broad peaks detected in conventional DLTS. During the Laplace DLTS measurements, the temperature of the samples is fixed as the method is isothermal. A Laplace DLTS measurement is performed within the range of temperatures represented by the conventional DLTS peak. The details of these measurements are described in Chapter 4.

5.2.5 Luminescence Measurements: Photoluminescence (PL), Cathodoluminescence (CL) And Electroluminescence (EL) Measurements

Photoluminescence (PL) measurements were carried out on NiO/Ga_2O_3 heterojunction using a Linkam THMS600 cryostat and He–Cd Kimmon Koha laser (λ = 325 nm) as excitation source with a laser power of 30 mW. The spectra were recorded by an Andor Solis SR500 monochromator using 300 lines/mm diffraction grid and a S-20 photomultiplier. The PL measurements were performed on the samples investigated in Chapter 8 in collaboration with Prof. Yara Gobato's group at Federal University of Sao Carlos, Brazil.

Cathodoluminescence (CL) is a powerful technique for understanding the behaviour and performance of electronic devices. The CL measurements reported in Chapter 6 were carried out at 3kV, 5kV and 7kV on AlGaN/GaN multi quantum well based LEDs in collaboration with the group of Dr Lixia Zhao at the Institute of Semiconductors, Chinese Academy of Sciences, Beijing, China.

The room temperature Electroluminescence (EL) measurements discussed in Chapter 7 were carried out on InGaN/GaN multi quantum well based photodetectors before and after current stress at 100 mA in collaboration with the group of Dr Pradip Dalapati at Nagoya Institute of Technology, Nagoya, Japan.

5.2.6 Raman Measurements

Micro-Raman measurements were performed with a 633 nm laser excitation on NiO/Ga_2O_3 heterojunction. The Raman signal was measured in a Lab RAM HR Horiba John Yvon system with 50x objective with spectral resolution of about 1 cm^{-1}. The Raman measurements were carried out on the samples mentioned in

chapter 8 in collaboration with Prof. Yara Gobato's group at Federal University of Sao Carlos, Brazil.

5.2.7 Photovoltaic Measurements

Photovoltaic measurements were performed to determine the I–V characteristics under artificial solar light with a standard air-mass 1.5 global spectrum, i. e. standard one sun-intensity (power density: 100 mW/cm^2). The photovoltaic measurements were carried out on samples presented in Chapter 7 in collaboration with Dr Pradip Dalapati at Nagoya Institute of Technology, Nagoya, Japan.

5.2.8 Scanning Transmission Electron Microscopy (STEM)

The STEM LED chip specimens were prepared using a focused ion beam-scanning electron microscope system (Helios NanoLab 460 HP). STEM images and EDX mapping were recorded using a double aberration corrected transmission electron microscope (JEM-ARM300F, JEOL). This SEM-CL method was used on the samples mentioned in Chapter 6 in collaboration with the group of Dr Lixia Zhao at the Institute of Semiconductors, Chinese Academy of Sciences, Beijing, China.

5.2.9 Silvaco Technology Aided Design (TCAD) Simulation

TCAD of SILVACO was used to model the I-V characteristics, energy band diagram of the structures, transport mechanisms, free carriers' profile and potential and electric field profiles. This modelling was used for the samples investigated in Chapter 8 in collaboration with Dr Nouredine Sengouga (University of Biskra, Algeria) and Dr Labed Madani (Sejong University, Korea).

CHAPTER 6: INVESTIGATION OF THE EFFECTS OF ELECTRIC CURRENT STRESS PROCESS ON THE STRUCTURAL, OPTICAL AND ELECTRICAL PROPERTIES of $Al_{0.6}GA_{0.4}N/Al_{0.5}GA_{0.5}N$ MULTI-QUANTUM WELLS BASED LEDS

6.1 Introduction

In this Chapter, the effects of electric current stress of 100 mA over 150 hours on the structural, optical and electrical properties of $Al_{0.6}Ga_{0.4}N/Al_{0.5}Ga_{0.5}N$ multi-quantum wells (MQWs) based deep ultraviolet light-emitting diodes (DUV LEDs) grown on sapphire substrates have been investigated using different techniques. The Current-voltage (I-V) characteristics indicated that the leakage current and ideality factor increased after the electric current stress. The capacitance - voltage (C-V) measurements revealed that the stress process causes redistribution of the charge carriers in the MQWs active region. At a small reverse bias V_R= - 0.5 V, deep level transient spectroscopy (DLTS) measurements showed two electron traps in the fresh LEDs (i.e. not subjected to the electric current stress), and one electron trap and a small unresolved signal due to a hole trap in the stressed LEDs. The very small hole trap signal at V_R= - 0.5 V which was not resolved by Laplace DLTS became more pronounced at V_R= - 4 V, and this bias condition Laplace DLTS revealed the same number of electron traps and hole traps in both LEDs. Scanning transmission electron microscopy (STEM) images and Energy-Dispersive X-ray spectroscopy (EDX) mapping demonstrated clear evidence that there are not many dislocations or defects in the MQWs before the stress is applied. However, after the

stress has occurred, two dislocation lines have appeared and extended throughout the quantum wells region.

6.2 Background

Group III-V aluminium gallium nitride (AlxGa1-xN) semiconductors with high Al composition (x) are promising for harmless, high efficiency deep ultraviolet light-emitting diodes (DUV LEDs) [1-3]. Compared with conventional mercury gas-discharge lamps, AlGaN-based DUV LEDs with the emission in UV-C wavelength range (100-280 nm) have exceptional properties, such as tunable emission wavelength, low operating voltage, and environmental friendliness [4, 5], which have potential applications in air- or water-purification, high-density data storage, medical diagnostics and disinfection, etc [6-8]. Till now, due to the low internal quantum efficiency (IQE) and Light Extraction Efficiency (LEE), the maximum EQE of AlGaN-based DUV LEDs at 275 nm is just 20.3% [9] and the general EQE of DUV LEDs is only in the single-digit percentage, which is far less than InGaN-based blue LEDs (>80%) [6, 10-14]. Many efforts have been made to reduce the threading dislocations (TDs) during AlGaN epitaxial growth [15, 16]. With the reduction of the density of TDs in AlN template, the highest IQE of AlGaN quantum wells can reach ~80% with a dislocation density less than 3 ×108 cm2 [17, 18]. Recently, it has been reported that the dominant nonradiative recombination centre is mainly related to point defects instead of threading dislocations for AlGaN epilayers [19]. Chichibu et al. [20, 21] have suggested that the point defects (PDs) play an important role in AlxGa1-xN-based LEDs. PDs such as Al (VAl) and N (VN) vacancies or complexes in AlxGa1-xN would be generated and propagate in or around the active region during operation or stress

[22, 23]. These point defects can act as nonradiative recombination centres in the active layers and increase the Shockley-Read-Hall (SRH) recombination, resulting in a decrease of optical power of the LEDs [24, 25]. However, how point defects and dislocations influence the device performance and what is the real character of these point defects is still not clear. AlGaN and quaternary InAlGaN material systems are widely used to fabricate such DUV LEDs. However, the lifetime of the latest deep UV-C LEDs is still limited to a few thousand hours due to various technical difficulties, such as high densities of threading dislocations [26], which limit their market penetration. In addition, poor Ohmic contacts result in a high junction temperature of the LED devices during operation [24]. During the operation of AlGaN-based UV LEDs in various degradation studies, such as stress current of 100 mA after 2, 8, 16, 50, 516 and 1000 hours, point defects have been found to generate and propagate in or around the active region [27]. In the active layer of the LEDs, these point defects will act as non-radiative recombination centres, thereby decreasing the internal quantum efficiency of the LEDs [27, 28]. Numerous reasons have been suggested as being accountable for the degradation of AlGaN and (In)AlGaN-based DUV LEDs subjected to current/temperature stress. Glaab et al. [29] reported the generation of acceptor-like point defects in the active region of AlGaN-based DUV LEDs after the devices were exposed to stress at a constant current of 100 mA over 50, 250 and 1000 hours. It was found that concentration of non-radiative recombination centres increased with increasing the stress level. In another study of AlGaN-based UV-B LEDs after stress operation at 200 mA, it was explained that a possible mechanism for the change in acceptor concentration resulting from the breaking of Mg-H complexes could be responsible for the degradation [30]. M. Meneghini et al reported an extensive analysis of the

degradation of AlGaN-based DUV LEDs submitted to direct current stress tests at different current densities and periods of time using combined electrical and optical characterization techniques. [31]. They found that (i) the stress can induce a significant decrease in the optical power emitted by the devices; (ii) the optical power decrease is more prominent at low measuring current levels, which suggests that degradation is related to an increase in the concentration of defects; (iii) the stress causes a localized increase in the apparent charge distribution profiles in the active region of the devices. All these experimental evidences imply that degradation is due to an increase in the defectiveness in the active layer of the devices. However, the physical origin of different degradation processes under current stress is not well understood. Therefore, to get high-reliable DUV LEDs, information regarding the various degradation behaviours and identifying the physical processes accountable for degradation taking place within the device are necessary to increase the lifetime of DUV LEDs and reduce several detrimental effects that hinder the novel development of such devices.

In this study, an investigation is carried out to investigate the defects present in AlGaN-based DUV LEDs after the degradation caused by electric current stress using cathodoluminescence (CL), C-V, DLTS, Laplace DLTS, STEM and EDX characterisation techniques. The results show that high electric current stress can induce both dislocations and point defects within the active region, especially in the first QWs near the p-side of the AlGaN epitaxial structure. These findings are important to understand the role of the dislocations and point defects and further improve AlGaN-based DUV LEDs.

6.3 Sample Details

Figure 6.1 shows a schematic diagram of the 260 nm AlGaN deep ultraviolet LEDs fabricated on AlN template/sapphire substrate by employing an epitaxial lateral overgrowth (ELO) process which has the advantage of producing low threading dislocation density. The structure was grown commercially by metal organic chemical vapor deposition (MOCVD) technique. A 600 nm AlN buffer layer was first deposited. This was followed by a 1.2 µm n-type Si-doped $Al_{0.7}Ga_{0.3}N$ current spreading layer, three periods of $Al_{0.6}Ga_{0.4}N/Al_{0.5}Ga_{0.5}N$ MQWs, a p-type Mg-doped $Al_{0.8}Ga_{0.2}N$ electron blocking layer (EBL), a 50 nm p-type Mg-doped $Al_{0.7}Ga_{0.3}N$ layer and a 100 nm p-type Mg-doped GaN contact layer. LEDs typically require 10 mA of working current. The LEDs were stressed at a high current of 100 mA corresponding to a current density of 160 A/cm2. This was the maximum operating current, and this stress was sustained over a duration of 150 hours. This electrical stress process was performed at room temperature and in an open laboratory environment.

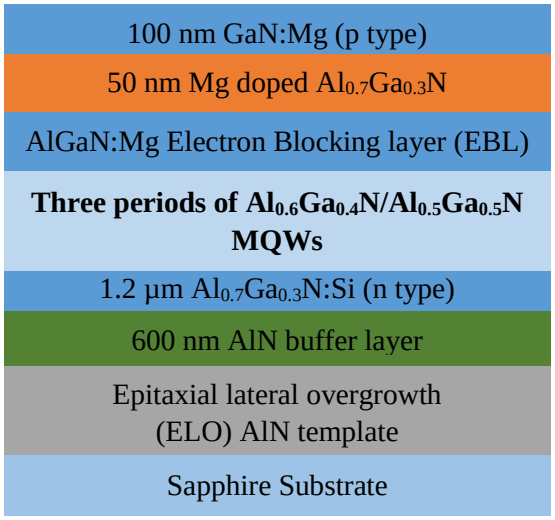

Figure 6.1: Schematic structure of the $Al_{0.6}Ga_{0.4}N/Al_{0.5}Ga_{0.5}N$ MQWs LEDs.

6.4 Optical Properties

Since the penetration depth of the electrons increases with increasing the electron beam energies [32] and in order to understand the distribution of the radiative and/or nonradiative recombination centres at different depths, CL spectra were measured using different electron accelerating voltages. In this case, the structural and optical properties of different layers in the multilayers structure can be identified. Figure 6.2 (a) shows the CL of the fresh (control sample which has not been subjected to current stress) DUV LEDs measured with different energies of the incident electrons, where the accelerating voltages were 3 kV, 5 kV and 7 kV. This allows the identification of the depth dependence of the radiative and non-radiative recombination centres distributions along the c-axis [0001].

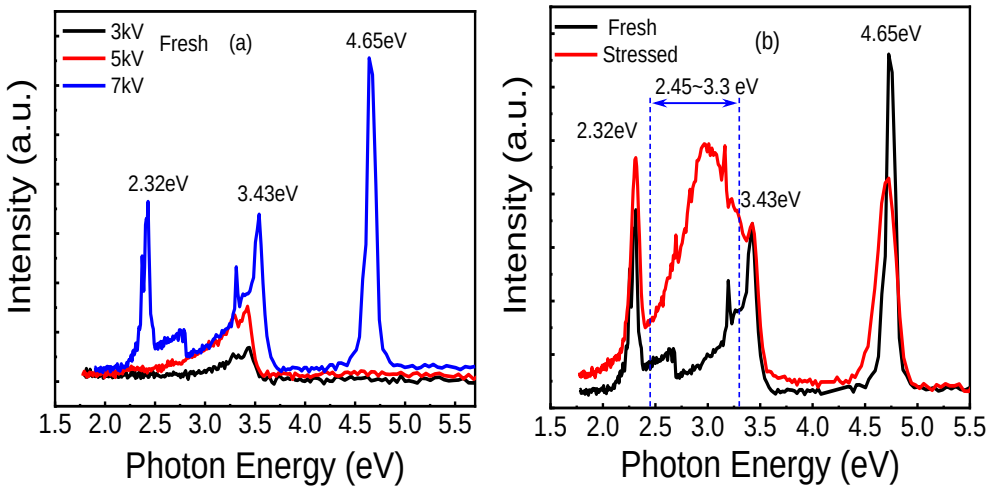

Figure 6.2: CL spectra of: (a) fresh DUV LED sample measured under different electron accelerating voltages of 3 kV, 5 kV and 7 kV; (b) DUV LEDs before and after degradation, measured under 7 kV electron accelerating voltage.

When the operation voltages are 3 kV and 5 kV, there is almost no emission from the QWs with the corresponding energy 4.65 eV (265 nm), indicating that the

majority of the collected CL signals are from the regions above the MQWs of the DUV LED chip. With increasing the operation voltage to 7 kV, the emission of AlGaN MQWs at 4.65 eV increases dramatically, suggesting that it is from the quantum well region. Using Monte Carlo simulations, the penetration depths of the electrons in the LED chip at 3 kV, 5 kV, and 7 kV are ~50 nm, 130 nm and 180-200 nm, respectively [33, 34]. Using the fresh LED chip as the control sample, the CL spectra of the stressed chip were investigated. Figure 6.2 (b) shows the CL spectra of the fresh and stressed LEDs measured at an electron accelerating voltage of 7 kV. As clearly seen in Figure 6.2, the intensity of the peak at 4.65 eV from the AlGaN MQWs decreases significantly after stress, similar to the previously reported results [35]. This suggests that some other defects may be generated inside the active region or p-type layers. The peaks at 3.43 eV and 2.32 eV correspond to the band edge emission of GaN and the second order diffraction of the main emission peak, respectively. Besides, an obvious broad emission in the energy range of 2.45-3.30 eV appears for the stressed sample compared with the control sample, which is related to the increased point defects in the quantum well area during the stress.

6.5 Electrical Investigations

6.5.1 Current-Voltage Measurements

I-V measurements as a function of temperature (200 - 440 K corresponding to -73.15 ^{0}C - 126.85 ^{0}C) with 20 K intervals) were performed for fresh and stressed samples in order to determine the diode parameters such as ideality factor (n), junction potential (V_{bi}) and series resistance (R_s). Figure 6.3 shows the semi-

logarithmic plot of I-V characteristics at room temperature. The I-V characteristic curves of the DUV LEDs show that the leakage current in the reverse bias region and the subthreshold region increase after the stress. In addition, the ideality factor calculated from the I-V curves also increases after stress, indicating the generation of point defects and/or dislocations [35].

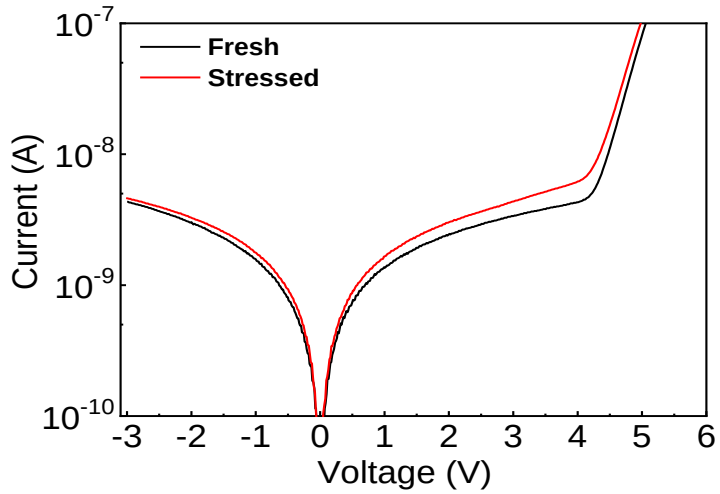

Figure 6.3: Semi-logarithmic I-V plots before and after electric current stress process.

The p-i-n junction current-voltage characteristics could be described by the thermionic emission model, as given by equation (6.1) below [36].

$$I = I_s \left[exp\left(\frac{q(V-IR_s)}{nK_BT}\right) - 1 \right] \tag{6.1}$$

where I_s is the saturation current and is given by [36]:

$$I_s = AA^{**}\, T^2\, exp\left(\frac{-qV_{bi}}{K_BT}\right) \tag{6.2}$$

where q is the elementary charge, n is the ideality factor, K_B is Boltzmann's constant, T is the temperature, V_{bi} is the Junction potential, R_s is the series resistance, A is the effective diode area (A= 0.00016 cm^2 for both devices) and A is the effective Richardson's constant (A^{**} = 34 A cm^{-2} K^{-2} for $Al_{0.3}GaN_{0.7}$). Werner's method was used to derive the diode parameters (n, V_{bi} and R_s) [36], which was discussed in Chapter 4, Section 4.3. Figure 6.4 shows the plots of G/I versus G and $ln\, I$ versus $(V - IR_s)$ for fresh LEDs. Similar procedure was used to extract the diode parameters of all samples investigated in this thesis.

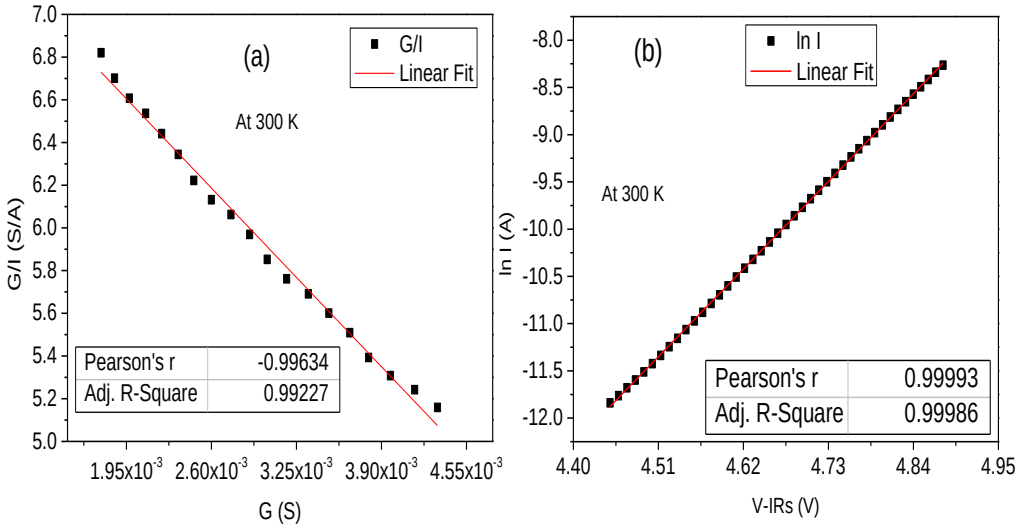

Figure 6.4: (a) plots of G/I versus G obtained from I-V curves at room temperature for forward bias conditions for Fresh sample. These plots were used to determine the ideality factors. (b) plots of ln (I) versus ($V-IRs$) for fresh sample are used to obtain V_{bi}.

These parameters (n, V_{bi} and R_s) before and after current stress at room temperature are shown in Table 6.1.

Table 6.1: Experimental data of ideality factor, junction potential and series resistance, obtained from I-V characteristics at room temperature for both samples.

Sample	n	V_{bi} (eV)	R_s (Ω)
Fresh	4.96 ± 0.20	0.99 ± 0.04	80.16 ± 0.40
Stressed	6.14 ± 0.30	0.90 ± 0.04	111.79 ± 5.50

As can be seen from Table 6.1 the ideality factor increased from 4.96 to 6.14 after the electric current stress. This increase, which was reported in UV LEDs devices after stress operation, was ascribed to the generation of point defects within or around the active region. These defects could be responsible for both Trap-Assisted Tunnelling (TAT) and nonradiative recombination [35, 37]. It is worth to mention that both devices demonstrated values of ideality factors greater than unity. This can be attributed to deep-level-assisted tunnelling [38]. Furthermore, fresh samples have a higher junction potential (0.99 ±0.04 eV) when compared to stressed samples (0.90 ± 0.04 eV). The higher value of junction potential and lower value of ideality factor of the fresh samples may indicate that the fresh samples possess better electrical properties. In addition, the fresh samples have lower series resistance (80.16 ± 0.40 Ω) compared to the stressed samples (111.79 ± 5.50 Ω).

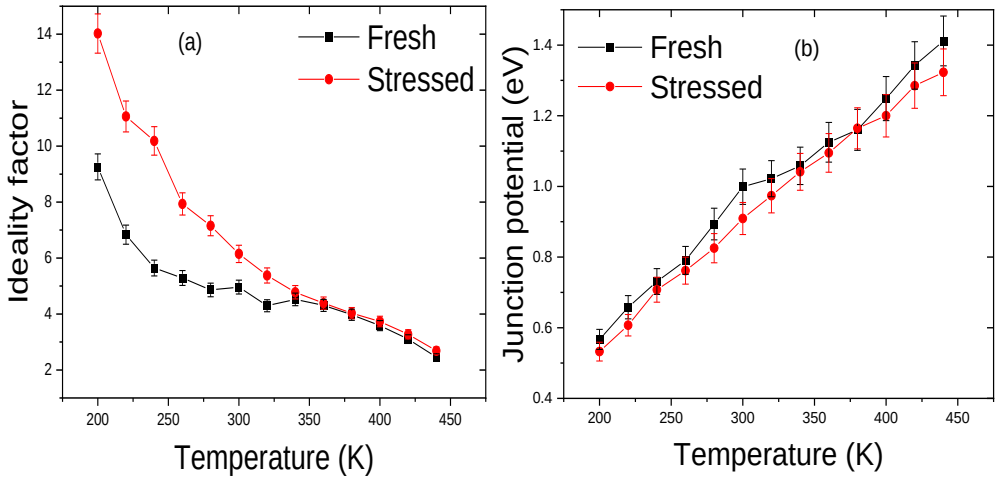

Figure 6.5: Temperature dependence of (a) the ideality factor, and (b) the junction potential, for both devices over a temperature range between 200 K and 440 K.

It is obvious, as shown in Figure 6.5 (a), that the ideality factor decreases with decreasing temperature. In the temperature range 200 K - 440 K, the ideality factor values for fresh and stressed devices ranged between 9.25 and 2.45, and 14.02 and 2.68, respectively. Similar trends and high ideality factors have been reported previously in $Al_{0.25}GaN_{0.75}$/GaN MQWs-based UV-LEDs, which were attributed to the presence of a tunnelling mechanism in these devices [39]. Tunnelling mechanism is a phenomenon when electrons pass through a barrier between p-type and n-type regions of a device when they have not sufficient energy to surmount the potential barrier. Figure 6.5 (b) shows the temperature dependence of junction potential for both devices. For both devices, the junction potential increases as the temperature increases. In contrast, the stressed device has a slightly lower junction potential than the fresh device, which is attributable to the current stress.

6.5.2 Capacitance -Voltage Characteristics

To investigate the carrier distribution in the active region of the DUV LEDs before and after the stress, C-V characteristics were measured at 1 MHz, as shown in the inset of Figure 6.6 (a).

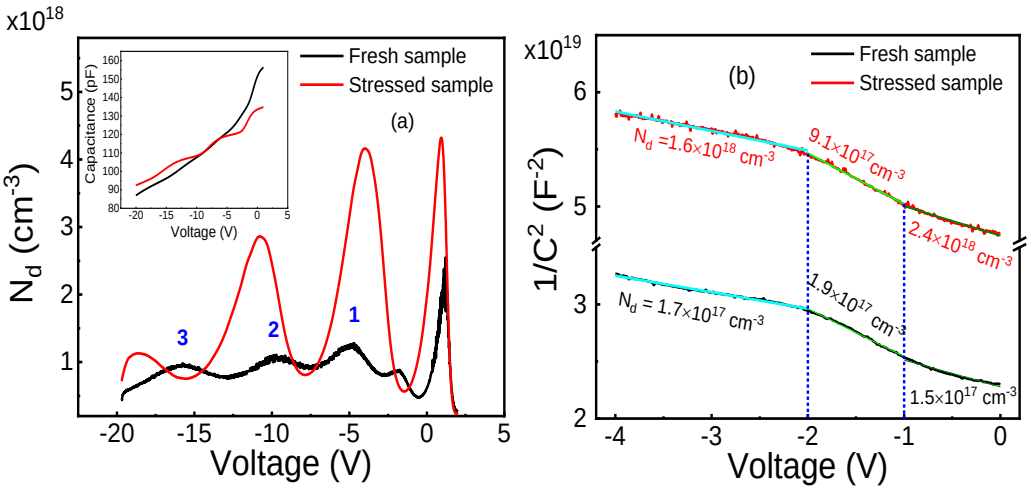

Figure 6.6: (a) the apparent carrier distribution (ACD) for the fresh and stressed DUV LEDs at various reverse biases obtained from C-V curves. The inset shows capacitance-voltage (C-V) curves of the fresh and stressed DUV LEDs measured at 1 MHz. (b) Relationship between the reciprocal of the square of the capacitance ($1/C^2$) and voltage (from -4 V to 0 V). Different colours are used for linear fitting to obtain the apparent carrier concentration.

The capacitance of the LEDs increases under a large reverse bias but decreases under a small reverse bias after stress. The three steps in the C-V curve in reverse bias become more obvious after stress (see inset of Figure 6.6 (a)). In addition, it the capacitance between -5 V and 0 V, is smaller after the electrical current stress, indicating that the effective negative charges in the p-region become less, which makes the space charge region move to the p-side. The different behaviour of capacitance change under reverse bias indicates the redistribution of the carriers in

the active region after stress. Figure 6.6 (a) shows the apparent carrier distribution (ACD) calculated from the C-V curves of DUV LEDs using the following equation [40],

$$\frac{\partial C_j(V_r)}{\partial V_r} = -\frac{C_j^3(V_r)}{q\varepsilon A^2}\frac{1}{N_d} \tag{6.1}$$

where ε represents the permittivity, A is the area of the junction, C_j is junction capacitance, V_r is the applied, reverse bias, and N_d denotes the apparent carrier concentration. The three peaks (marked by numbers 1-3) correspond to the three quantum wells of the LEDs. The ACD of the fresh LEDs is very uniform in the MQWs. But after stress, the carrier distribution in the MQWs becomes inhomogeneous, as shown Figure 6.6 (a) (red line). Furthermore, the change of N_d of the first quantum well near the p-region (the first QW, marked 1) for stressed LEDs is more significant than the other two quantum wells. The maximum value of the ACD for first QW changes from $1.20 \pm 0.06 \times 10^{18}$ cm^3 to $4.16 \pm 0.20 \times 10^{18}$ cm^3 after current stress. To further investigate the variation of the active area near the p-region, the relationship between the inverse of the square of the capacitance and voltage (from -4 V to 0 V) was extracted from C-V curves, which is plotted in Figure 6.6 (b). Since the active area (MQWs region) of the LEDs epitaxial structure is normally undoped, the apparent carrier concentration of the first QW area can be obtained by linear fitting $1/C^2$ - V curve in the reverse bias voltage range -4 V to 0 V as discussed in Chapter 4 and expressed below,

$$\partial\left(\frac{1}{C^2}\right)\Big/\partial V_r = \frac{2}{A^2\, q\varepsilon N_d} \tag{6.2}$$

The results show that the linear fitted average apparent carrier concentration N_d for both the fresh and stressed samples can be divided into three voltage regions, -4 V to -2 V, -2 V to -1 V and -1 V to 0 V, respectively. The apparent carrier concentrations in these three regions for the stressed LEDs are 9.4, 4.8, and 16 times greater than those of the fresh samples. Therefore, the ACD in the MQWs had a redistribution process after stress, showing an increase trend during the stress, and this behaviour is more significant in the top quantum well of the active area close to the p-type side. As reported previously, the electric current stress would cause the generation of defects in the AlGaN-based LED chips [24, 35], and these defects which are related to deep levels can capture electrons or holes [19], resulting in the increase of the ACD in the AlGaN MQWs.

6.5.3 DLTS And Laplace DLTS Characteristics

To further investigate the possible deep levels in the region near the p-region, DLTS spectra were obtained for the fresh and stressed samples. DLTS measurements were performed for the fresh and stressed LEDs under two different reverse bias conditions, namely, (i) a filling voltage (V_P) of 0 V and a reverse applied voltage (V_R) of -0.5 V (corresponding to a small depletion region near the interface), and (ii) V_P = 0 V and V_R = -4 V (corresponding to a depletion region extending away from the interface). Figure 6.7 shows the DLTS spectra for V_P = 0 V and V_R = -0.5 V before and after stress to evaluate the area adjacent to the p-region around MQWs. For the fresh device, two negative peaks are observed at 80 K and 265 K and labelled as $E_{1F(-0.5)}$ and $E_{2F(-0.5)}$, respectively. The subscripts “F” and “-0.5 refer to fresh sample and reverse applied voltage V_R, respectively. However, for the stressed LEDs, the $E_{2S(-0.5)}$ peak (subscript “S” refers to stressed sample) shifts

towards lower temperature of 233 K. In addition, a small positive peak (labelled as H_{1S}) appears at ~145 K for the stressed LEDs. In DLTS, a positive peak is related to minority-carriers trap levels, whereas a negative peak is related to majority-carriers trap levels [41, 42]. For the unintentionally doped AlGaN MQWs, the minority carriers are holes and the majority are electrons [41].

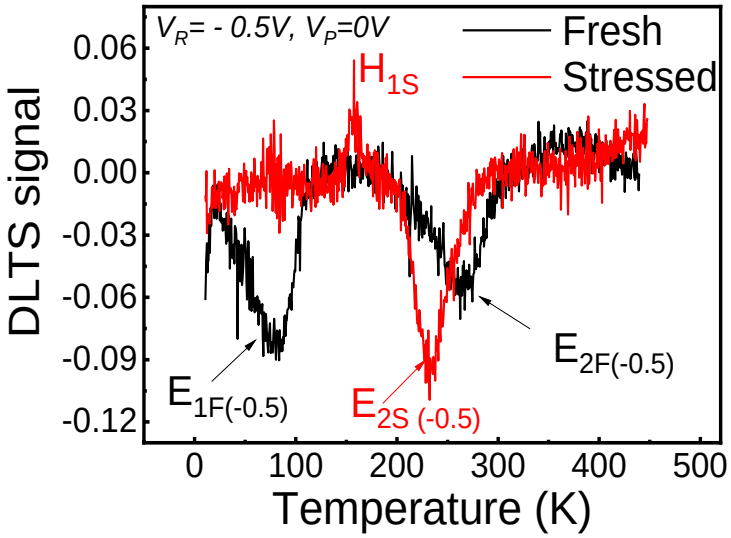

Figure 6.7: Typical DLTS spectra of the fresh and stressed DUV LEDs at V_R= -0.5 V.

Figure 6.8 shows the Arrhenius plots of the traps detected in the fresh and stressed samples for V_R = -0.5 V with their parameters listed in Table 6.2. The small activation energy of trap $E_{1F(-0.5)}$ of about 0.010 eV (corresponding to the peak at a temperature ~100 K) indicates that it has a shallow character [19], which may be related to the point defect P1 with activation energy 0.01 eV reported previously and which was suggested to be related to Al vacancies (V_{Al}) [19]. The disappearance of the negative peak E_{1F} and the emergence of the new positive peak H_{1S} indicates that there may be a donor-acceptor complex trap in the active area after the stress. This H_{1S} trap could not be resolved by using LDLTS at reverse bias

V_R = -0.5 V, but it has been resolved at reverse bias V_R= -4 V which will be discussed later. The activation energies of the traps $E_{2F(-0.5)}$ and $E_{2S(-0.5)}$ which are in the range 0.20 to 0.25 eV could indicate that they have the same origin and be related to N vacancies (labelled E1) with activation energy of 0.20 eV [43]. The trap $E_{2F(-0.5)}$ concentration increases by more than 20 times from 4.5 ×10^{13} cm^3 to 9.9×10^{14} cm^3 after electric current stress. The capture-cross section of $E_{2F(-0.5)}$ also increases from 4.6 × 10^{-20} cm^2 to 8.6 × 10^{-19} cm^2 after stress. In addition, the shift of the E_{2S} DLTS peak to lower temperature and the increase of the activation energy indicate that the trapping probability of electrons increases after the stress.

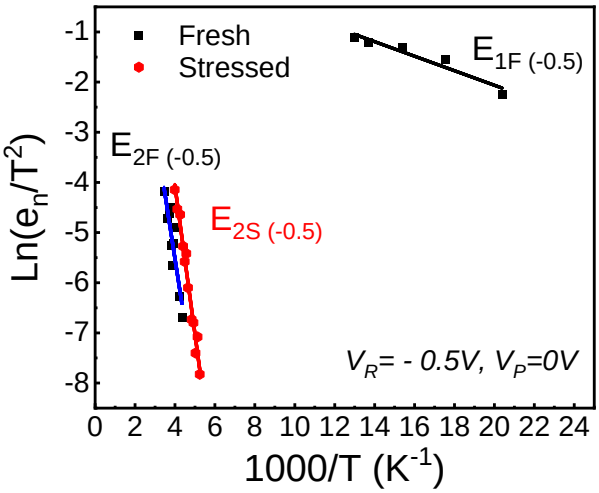

Figure 6.8: Arrhenius plots for fresh and stressed devices obtained from Laplace DLTS at V_R= -0.5 V.

Table 6.2: Apparent activation energy, capture cross section, and trap concentration of the defects observed in the fresh and stressed DUV LEDs devices. DLTS experimental conditions: V_R= - 0.5 V, V_P = 0 V and the duration of the filling pulse was tp = 1 ms.

Samples	Trap	Activation energy (eV)	Trap concentration (cm^{-3})	Capture Cross-Section (cm^2)
Fresh	$E_{1F(-0.5)}$	0.01	$7.4\pm0.4\times10^{13}$	$8.8\pm0.4\times10^{-22}$
	$E_{2F(-0.5)}$	0.20 ±0.04	$4.5\pm0.2\times10^{13}$	$4.6\pm0.2\times10^{-20}$
Stressed	$E_{2S(-0.5)}$	0.25 ±0.01	$9.9\pm0.5\times10^{14}$	$8.6\pm0.4\times10^{-19}$

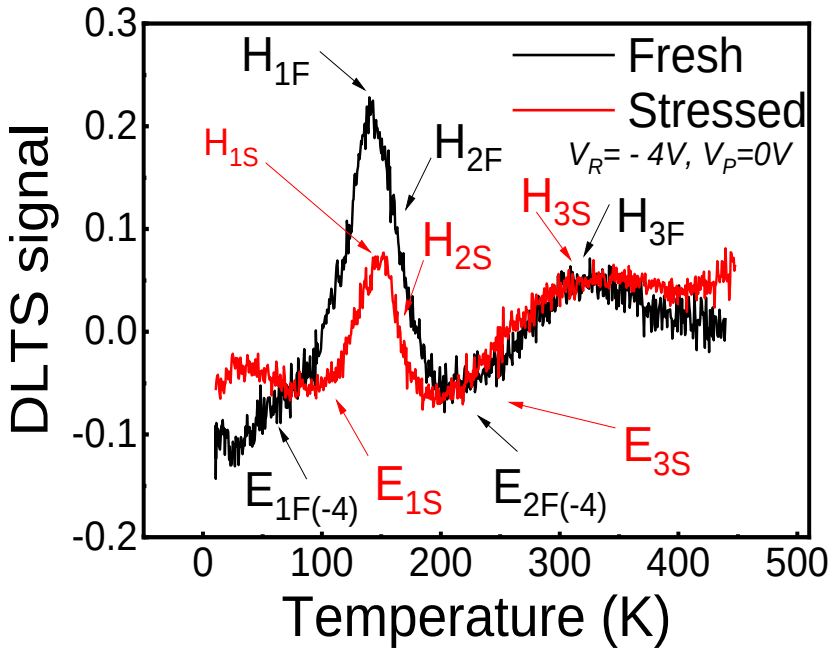

Figure 6.9: Typical DLTS spectra of both DUV LEDs at V_R= -4 V

Figure 6.9 shows the DLTS spectra before and after stress at V_R = -4 V (region probed by DLTS away from interface). The same number of traps were found in both LEDs. The following traps have been detected and labelled as $E_{1F\,(-4)}$, $E_{2F\,(-4)}$, H_{1F}, H_{2F}, and H_{3F} in fresh LEDs, and E_{1S}, E_{3S}, H_{1S}, H_{2S}, and H_{3S} in stressed LEDs.

It is worth mentioning that the amplitude of the H_{1S} peak is enhanced for fresh sample at V_R= -4 V and this peak is detected at the same temperature as for V_R= -0.5 V. The activation energies of these traps were calculated from the Arrhenius plots as shown in Figure 6.10 (a) and (b). The trap parameters, such as activation energies, trap concentrations and capture cross sections are summarised in Table 6.3. $E_{1F\,(-4)}$ and $E_{2F\,(-4)}$ traps have similar activation energies and concentrations to those of $E_{1F\,(-0.5)}$ and $E_{2F\,(-0.5)}$, respectively, indicating that these traps are close and far from the interface (i.e. uniformly distributed across the depletion layer). However, trap $E_{2F\,(-0.5)} = E_{2S\,(-0.5)}$ was not detected at V_R = -4 V, meaning it is located near the interface. Traps E_{1S} and E_{3S} may be related as they have almost the same activation energy at around 0.07 eV, but with different concentrations and capture cross-sections as shown in Table 6.2. The origin of these traps could be the same as the D trap with activation energy 0.075-0.085 eV reported in the study of AlGaN/AlGaN superlattice based on near-UV LEDs [44]. The D trap was attributed to nitrogen vacancy [44, 45]. Traps H_{1F}, $H_{2F,}$ H_{1S} and H_{2S} with activation energies in the 0.01eV to 0.07 eV narrow range, could be related and originate from a similar trap that could be assigned to nitrogen vacancy complexes as suggested by T. Kinoshita et al. [46] in their study of Mg-doped $Al_{0.7}Ga_{0.3}N$ thin films grown on sapphire substrates by MOCVD. In their investigation, magnesium (Mg) flux was increased (i.e. p-doping) during the growth process of AlGaN in order to prevent it from becoming less effective over time due to self-compensation. However, the magnesium forms complexes with nitrogen vacancies in AlGaN with activation energies of 0.047–0.072 eV at temperature below 500 K. This trap was found also in AlGaN quantum well heterostructures for mid-ultraviolet emitters having an activation energy of 0.060 eV. The H_{3S} with activation energy of 0.090 eV could

be assigned to Mg related acceptors (h1) with activation energy ranging from 0.1 to 0.2 eV [41]. The origin of H_{3F} trap could be related to Mg impurities that are used as p-type dopants in Mg-doped AlN epilayers grown by MOCVD [47]

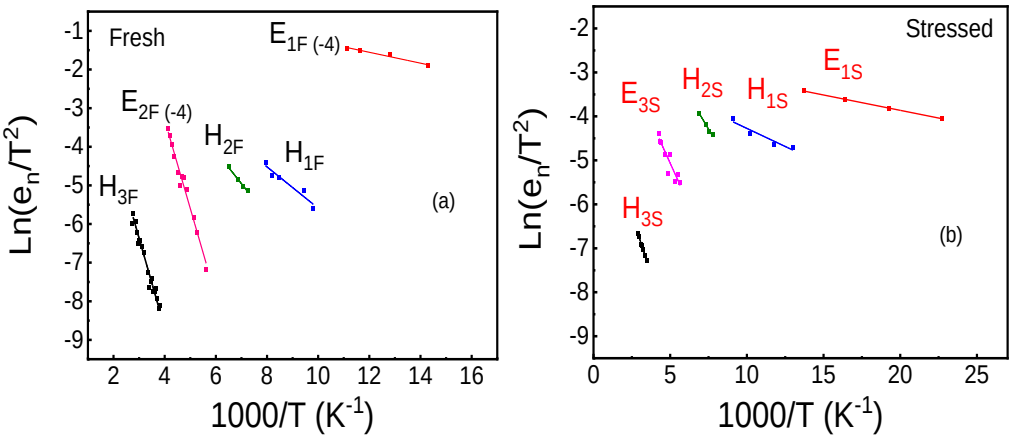

Figure 6.10: Arrhenius plots for fresh LEDs obtained from Laplace DLTS, and (b) Arrhenius plots for stressed LED obtained from Laplace DLTS.

Table 6.3: Apparent activation energy, capture cross section, and trap concentration of the defects observed in the fresh and stressed DUV LEDs devices. DLTS experimental conditions: V_R= - 4 V, V_P = 0 V and the duration of the filling pulse was tp = 1 ms.

Samples	Trap	Activation energy (eV)	Trap concentration (cm^{-3})	Capture Cross-Section (cm^2)
Fresh	$E_{1F\ (-4)}$	0.010	$6.1\pm0.3\times10^{13}$	$1.6\pm0.1\times10^{-23}$
	$E_{2F(-4)}$	0.20±0.01	$7.6\pm0.4\times10^{13}$	$5.3\pm0.3\times10^{-19}$
	H_{1F}	0.05±0.01	$6.1\pm0.2\times10^{13}$	$3\pm0.2\times10^{-22}$
	H_{2F}	0.07±0.01	$2.2\pm0.3\times10^{14}$	$9.5\pm0.5\times10^{-22}$
	H_{3F}	0.20±0.01	$6.1\pm0.2\times10^{13}$	$7.1\pm0.3\times10^{-22}$
Stressed	E_{1S}	0.070±0.01	$4.80\pm0.2\times10^{14}$	$1.3\pm0.1\times10^{-22}$
	E_{3S}	0.07±0.01	$9.6\pm0.5\times10^{14}$	$4.6\pm0.2\times10^{-22}$
	H_{1S}	0.010	$9.6\pm0.5\times10^{14}$	$2.8\pm0.1\times10^{-23}$
	H_{2S}	0.050	$9.6\pm0.5\times10^{14}$	$4.3\pm0.2\times10^{-22}$
	H_{3S}	0.090	$7.2\pm0.4\times10^{15}$	$1\pm0.1\times10^{-23}$

6.6 Structural Characterization

To further evaluate the DUV LED structure after degradation, especially the quantum well area, the samples were characterised by cross-sectional TEM imaging and EDX (Energy-dispersive X-ray spectroscopy) mapping.

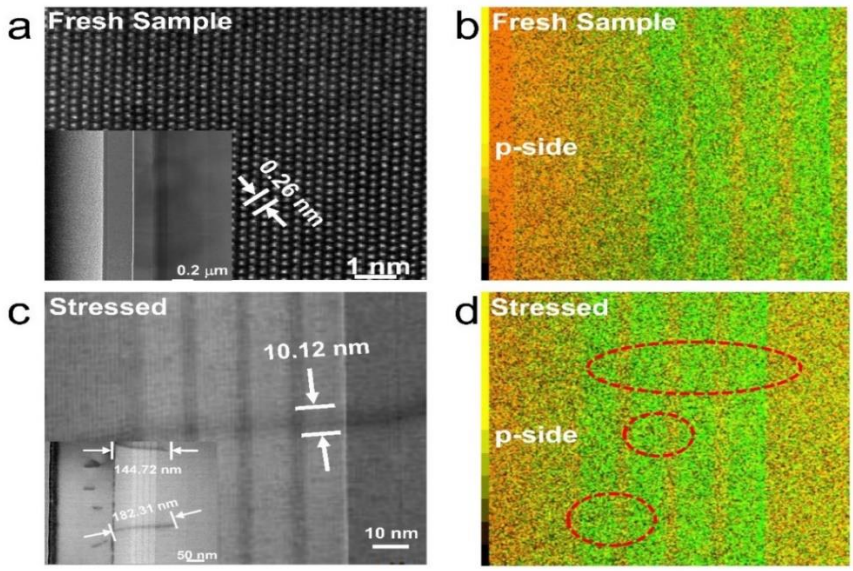

Figure 6.11: Cross-sectional aberration-corrected STEM image of the DUV LEDs devices (a) fresh sample; (c) stressed sample. EDX elemental mapping of the MQWs region shown as an overlay of Al, Ga and N signals for the fresh sample (b) and the stressed sample (d). The red circles in Fig. 6.10 (d) show some variation of the elements in the MQWs for the stressed sample.

Figure 6.11 (a) shows the aberration-corrected high angle annular dark field scanning transmission electron microscopy (HAADF-STEM) image of the MQWs region of the fresh LEDs, and the inset displays the TEM image of the epitaxial structure for the fresh LEDs. These images help to directly identify the depth dependence of the defects. There are little dislocations or defects in the MQWs before the stress. However, after the stress, two dislocation lines appear and extend through the whole quantum wells region, as shown in Figure 6.11 (c). To

investigate the effect of the threading dislocation on the MQWs, the EDX mapping of the MQWs region were measured by an overlay of Al (green), Ga (yellow) and N (orange) signals, as shown in Figure 6.11 (b) and (d). By comparing the EDX mapping images of the fresh and stressed samples, there are some variations of the composition in the first and second quantum wells and barriers near the p-region of the epitaxial structure. These variations suggest the occurrence of intermixing between the Al, Ga and N elements, indicating potential strain-induced diffusion and alloying effects in the active region under electrical stress conditions. The composition also changes along the dislocation, as marked with the red circles in Figure 6.11 (d). The TEM and EDX mapping results suggest that the MQWs of the LEDs epitaxial structure have been strongly affected after stress, especially close to the p-side. In general, threading dislocations (TDs) in InGaN/GaN MQWs active structures would act as nonradiative recombination centres and degrade the PL emission intensity [48, 49], which strongly contribute to the leakage current of forward and reverse I-V regions in LEDs [50, 51]. The electrical and optical properties of InGaN/GaN MQWs tend to deteriorate with increasing dislocation densities [52]. However, for AlGaN/GaN MQWs, the internal quantum efficiency (IQE) of the QWs grown on AlN bulk substrates with a low threading dislocation density (TDD) < 10^5 cm^2 is almost the same as that of QWs grown on sapphire substrates with a high TDD (approximately 10^9 - 10^{10} cm^2) [53]. The emission dark spots attributed to TDs were not observed in the CL images of AlGaN/AlN QWs in the entire temperature region [19]. The results reported in the literature suggest that TDs are not the dominant nonradiative recombination centres for AlGaN-based LEDs. However, in this work, the TEM results show that the dislocation lines did appear in the MQWs region after electric current stress, which may influence the

point defects due to Mg diffusion along the dislocation line and creating some Mg-related acceptor traps [54] and degrading the AlGaN-based LEDs [55] in terms of optical quality.

6.7 Conclusion

In this study, point defects and dislocations were investigated systematically by comparing the AlGaN-based DUV LEDs before and after degradation using several different analytical techniques, including cathodoluminescence, deep-level transient spectroscopy and transmission electron microscopy. The results show that the electrical current stress induced point defects are located within the multiple quantum wells region, especially in the first quantum well near the p-region of the p-i-n DUV LEDs. The increased point defects density during the stress caused a carrier redistribution process. In addition, the DLTS results showed two electron traps in the fresh LEDs and one electron trap and a small unresolved signal due to a hole trap in the stressed LEDs. The very small hole trap signal at V_R= - 0.5 V which was not resolved by Laplace DLTS became more pronounced at V_R= - 4 V, and this bias condition Laplace DLTS revealed the same number of electron traps and hole traps in both LEDs. Moreover, the TEM (EDX mapping) also provided some evidence of Mg diffusion along the dislocation line leading to Mg-related traps. By investigating the defects of the fresh and the electric current stressed DUV LEDs epitaxial structures, the failure mechanisms for the stressed sample with regards to the point defects and dislocations have been identified. The stressed sample exhibited a decreasing intensity of emission, an increase in leakage current, and a higher ideality factor compared to the fresh sample. This study is important to further improve the performance of AlGaN-based DUV LEDs.

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CHAPTER 7: CURRENT-INDUCED DEGRADATION BEHAVIOURS OF InGaN/GaN MULTIPLE-QUANTUM-WELLS UV PHOTODETECTORS: ROLE OF ELECTRICALLY ACTIVE DEFECTS

7.1 Introduction

To examine the critical role of electrically active defects and surface states in $In_{0.09}Ga_{0.91}N$/GaN multiple quantum wells (MQWs) ultraviolet photodetectors (UV-PDs), the study of degradation mechanisms in such devices is very important. This chapter reports the effects of the electric current stress process on the structural, electrical and optical properties of InGaN/GaN MQWs UV-PDs before and after electric current stress using electroluminescence (EL), Current-Voltage (I-V), Capacitance–Voltage (C-V), DLTS, Laplace-DLTS and Photocurrent Spectroscopy (PCS) techniques. By applying a high electrical current stress of 200 mA over 340 hours, it was found that InGaN/GaN MQWs UV-PDs degraded and their properties were affected. As a consequence of electric current stress, it was found that (i) the electroluminescence intensity decreases distinctly (~ 48 %), suggesting that more of the charge carriers are captured by the newly induced defects in the active region; (ii) the open-circuit voltage is mostly accountable for the degradation of photovoltaic properties in stressed PDs; (iii) the parasitic current leakage paths increased significantly which in turn reduce the photocurrent generation process largely; (iv) within the temperature range of 100–440 K, the values of the ideality factor and junction potential are found to be always higher and lower in stressed PDs, respectively, indicating the presence of generation-

recombination centres caused by defects; (v) two major trap levels are identified in stressed PDs via Laplace DLTS analysis; and (vi) the responsivity in stressed PDs decreases. The obtained results indicate that degradation is mainly associated with the newly generated defects, mostly Mg-related shallow acceptors, including Mg_{Ga} and Mg-H_2 complexes, which can form the acceptor levels as a result of the breaking of Mg-H chemical complexes due to high heating levels during the stress treatment.

7.2 Background

Nowadays, the advancement of wide bandgap semiconductors (GaN, AlGaInN, MgZnO, Ga_2O_3, $ZnGa_2O_4$, etc.) based ultraviolet photodetectors (UV-PDs) is one of the utmost in demand and extensively developed areas of optoelectronic devices because UV-PDs find widespread civilian, space, and military applications, including remote control systems, multispectral flame sensing, ozone monitoring, space communication systems, and missile warning systems [1-4]. However, several detrimental effects originating from native defects and surface states in such devices hinder the novel development of super-sensitive UV-PDs [5-8]. For the development of high-performance UV light detection devices with ultrafast response speed, InGaN/GaN MQWs structures have commonly been employed [9-12]. The InGaN/GaN MQWs structure can effectively decrease the thermodynamic and strain-induced structural instabilities as well as the formation of V-type defects, leading to surpassing the technical bottleneck in the usable high spectral responsivity [11, 13]. Furthermore, the technological difficulties for the production of low defects and large area GaN substrates, propel the use of other less lattice matched substrates, namely, Si and sapphire for the fabrication of PDs. Therefore,

the obvious lattice mismatch and the dissimilarity in thermal expansion coefficients between GaN and these substrates lead to the generation of high density defects in InGaN/GaN heterostructures [14]. Several defects and structural imperfections in InGaN/GaN MQWs PDs play many critical roles for various unfavorable effects which strongly affect the photoexcited charge carrier separation process in PDs. The practical applications of such devices in numerous fields demand highly reliable and stable PDs. Therefore, for the development of highly stable UV-PDs, the role of surface states and high defects density, including threading dislocations (TDs) and native point defects need to be studied rigorously. In earlier works [15, 16], the impact of constant current stress on the electrical and optical properties of similar PDs has been reported and it has been observed that the degradation processes are usually associated with the newly generated electrically active defects in the stressed devices. Based on X-ray diffraction (XRD) and X-ray photoelectron spectroscopy (XPS) results, Horng et al. [4] claimed that in $ZnGa_2O_4$-based deep ultra-violet (DUV) photodetectors, the main degradation is caused by the ozone compensation as well as the surface water adsorption. However, the defect-related degradation mechanisms in InGaN-based PDs are not well investigated until now. Several open questions remain unanswered: (i) where are the central defect levels situated, (ii) how do they penetrate in the different epilayers, (iii) what are their chemical natures and (iv) what are their activities in the devices. Thereby, to fabricate high-efficiency and high-reliable InGaN-based UV-PDs, an in-depth inspection of the location of defects and their activities in such devices is importantly required. This work aims to gain detailed information on the above issues by studying the degradation behaviours of the optical and electrical properties of InGaN/GaN MQWs UV-PDs at high constant current stress. Prior to

presenting the details of the study, it is necessary to describe some of the essential and novel aspects of the investigation. First, the $In_{0.09}Ga_{0.91}N$/GaN MQWs UV-PDs structure has been grown on a sapphire substrate and the fabricated devices included a 20-nm-thick Al_2O_3 passivation layer deposited on top which can reduce the surface states significantly. Second, the optical and electrical characteristics of fresh and stressed UV-PDs were obtained to understand the root mechanisms of the degradation. Third, Deep Level Transient Spectroscopy (DLTS) and Laplace-DLTS spectra have been acquired for the fresh and stressed UV-PDs in order to identify the location and nature of electrically active defects. The sensitization performance of the detector has been examined in relation to the effect of the electric current stress.

7.3 Device Fabrication

In the present work, an $In_{0.01}Ga_{0.99}N$/GaN MQWs UV-PDs structure was grown on the *c*-plane of a sapphire substrate by using a horizontal metal organic chemical vapor deposition (MOCVD) system. The cross-sectional view of the employed PDs structure is schematically displayed in Figure 7.1. Initially, the low-temperature GaN (LT-GaN) buffer layer of 30 nm was grown on top of the substrate at a substrate temperature < 650 ^{0}C and then, a thick Si-doped n-type GaN layer was deposited (growth temperature GT = 1160 °C, thickness = 2.5 μm, doping concentration ≈ 3×10^{18} cm^{-3}). This was followed by an active region consisting of a large number (42-period) of InGaN/GaN (3 nm / 3 nm) MQWs (GT = 825 °C). Finally, two Mg-doped p-type GaN layers were grown by a two-step growth process. During the growth of the first 100 nm p-GaN layer, the growth temperature was kept at 825 °C, whereas the remaining 150 nm p-GaN layer was grown at 875

°C. The Mg concentration for the p-GaN layers was about 5×10^{19} cm^{-3}. It is important to note that the two-step growth process of the p-GaN layers can improve the device performance significantly as observed in GaInN MQWs [17].

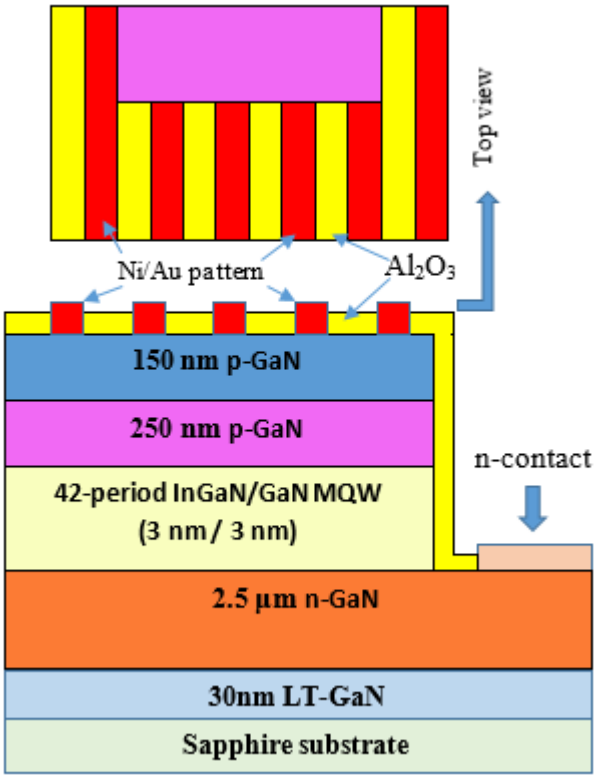

Figure 7.1: Schematic illustration (cross-sectional) of InGaN-based UV-PDs structure.

The UV-PDs were fabricated using standard techniques including photolithography, BCl_3 plasma reactive ion etching (RIE), electron beam metal evaporation (EBE), and subsequent annealing. The photolithographic method was used to imprint the device geometry of the grown structure, whereas RIE was employed to etch the contact regions (n-type) of the device. After that the etched sample was annealed at 750 °C for 30 minutes in N_2 atmosphere to activate the Mg acceptors in the p-GaN layers. Following the Mg acceptors activation process, the n-contact was formed by depositing Ti/Al/Ni/Au (15/60/12/60 nm) metals using

EBE process, whereas the finger-shaped p-contact was also deposited by the same process (EBE) with Ni/Au (5 nm / 60 nm) metals as seen in Figure 7.1. Next, a rapid (30 s) annealing treatment at 750 °C in N_2 atmosphere was performed to accomplish good n-type Ohmic contact layers. In addition, to attain p-type Ohmic contacts, the sample was annealed at 600 °C for 3 minutes in O_2 atmosphere. Before the finalization of PDs fabrication, a 20-nm thick Al_2O_3 passivation layer was deposited on top of the sample (without contact electrodes) to reduce the effect of surface states. The passivation film was deposited by an atomic layer deposition unit (Cambridge Nano-tech) [18]. During the atomic layer deposition, trimethylaluminum was used as an Al precursor, whereas purified H_2O and O_3 were considered as the O_2 precursors [11, 18].

7.4 Structural Characterization

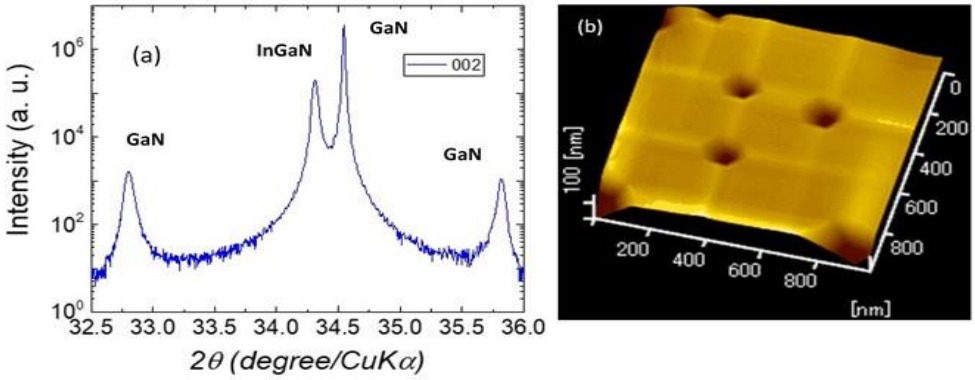

Figure 7.2: (a) Curve of XRD (2θ-ω scan) for (002) plane reflection, and (b) 1 × 1 μm^2 AFM image.

Figure 7.2 (a) shows the XRD linescan where the satellite peaks are clearly noticeable, demonstrating the high quality of the periodic multilayer structure of the sample with Indium incorporated into GaN. In addition, from this ω–2θ scan, the In composition in InGaN/GaN MQWs region was calculated to be about 9%.

Furthermore, the estimated value of the density of TDs was about 9.1×10^8 cm^{-2}. The surface morphology of the top GaN layer was analyzed by using Atomic Force Microscopy (AFM) before fabrication, as shown in Figure 7.2 (b). During the growth of the sample, the formation of threading dislocations (TDs) results in the creation of numerous pits (dark spots) on the surface, leading to changes in the surface topography as can be seen in Figure 7.2 (b). The size and shape of these pits are directly linked to the type of dislocations present [19]. Specifically, pits caused by screw-type dislocations tend to be larger than those caused by edge-type dislocations [20]. The atomic force microscopy is a widely employed technique to record the image of pits associated with TDs [14]. Furthermore, Figure 7.2 (b) shows that checkerboards which can often be caused by a number of factors, such as tip-sample interactions, surface roughness, or variations in material properties [21]. The obtained value of the root mean square (RMS) roughness in the areas not containing pits and checkboards was 11.66 nm.

The details of the various optical and electrical measurements (electroluminescence (EL), current-voltage (I–V), capacitance–voltage (C–V), DLTS, Laplace DLTS and photocurrent spectroscopy (PCS)) used in this investigation are described in Chapter 5. Furthermore, it is worth noting that in the present work, the constant high-current (200 mA) over 340 hours stress treatments of the un-encapsulated UV-PDs were performed at room temperature and in an open laboratory environment. On the other hand, the DLTS and LDLTS were carried out in the temperature range of 10 K - 450 K using a Boonton 7200 capacitance meter, a pulse generator, a Lake Shore 331 temperature controller and a data acquisition system. All the PDs samples (two fresh and three stressed) were mounted and wire-bonded onto TO5

headers and fitted in a Janis closed-loop helium cryostat for the temperature dependence measurements.

7.5 Optical Properties

7.5.1 Degradation Of Luminescence Property

The degradation of the luminescence property of the PDs devices which contain a 42-period of InGaN/GaN MQW in the active region was recorded. The EL intensity for a driving current of 100 mA decreased markedly (~ 48%) as depicted in Figure 7.3 . Ma et al. [22] suggested that in InGaN/GaN MQWs structures, the domination of TDs ruins the luminescence property of the active region because these TDs act as non-radiative recombination centres (NRCs). However, the obtained results shown in Figure 7.3 suggest that the degradation of EL intensity in the stressed PDs is closely related to the newly created defects in the active region of the device where numerous charge carriers can recombine non-radiatively. These defects, therefore, reduce the EL intensity substantially [15]. Furthermore, it is important to mention that throughout the stress treatment, the full width at half maximum (FWHM) does not change significantly, whereas the MQW emission peak in the stressed PDs is shifted slightly from 412.2 nm (fresh PDs) to 412.4 nm, as depicted Figure 7.3. This small red-shift could be due to the In content fluctuation as suggested in Ref. [15]. In addition, the In fluctuation can affect the NRCs in the device as well. Therefore, this In fluctuation in the stressed PDs can further reduce the EL intensity.

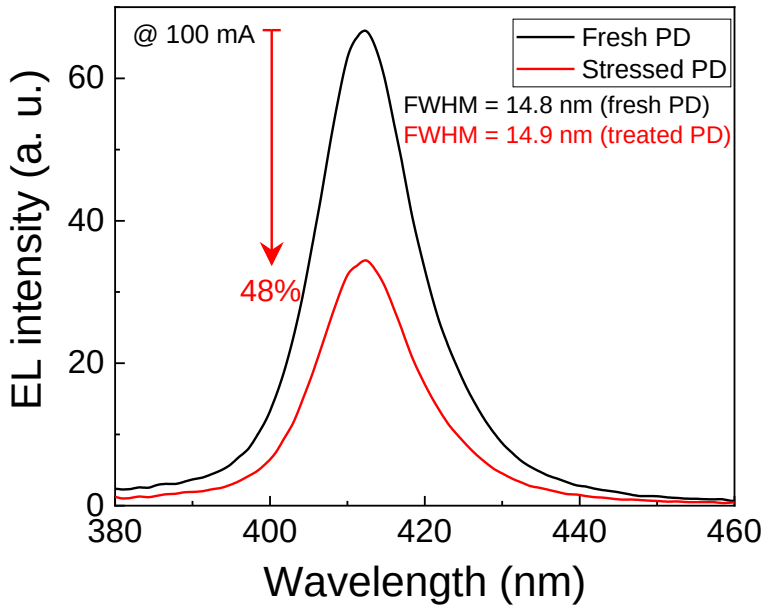

Figure 7.3: EL spectra at 100 mA acquired before (black line) and after 340 hours of stress treatment (red line). FWHM: 14.8 nm (fresh PDs), 14.9 nm (stressed PDs).

7.6 ELECTRICAL PROPERTIES

7.6.1 Degradation Of Photovoltaic Properties

It is important to note that studies on the degradation of photovoltaic properties, namely, short-circuit current (I_{SC}) and open-circuit voltage (V_{OC}) in InGaN/GaN MQWs PDs under different stress conditions are not widely available in the literature [16, 23, 24]. However, to get a deep perception into the degradation of photovoltaic properties of InGaN-based PDs, the I–V characteristics were measured under the artificial solar light with a standard air-mass 1.5 global spectrum i. e., standard 1 sun-intensity (power density: 100 mW/cm^2) before and after 340 hours of electric current stress treatment of 200 mA. The obtained results are illustrated in Figure 7.4. It can be noticed in Figure 7.4 that I_{SC} reduces slightly from 5.48×10^{-6} to 5.37×10^{-6} A (corresponding short-circuit current density J_{SC} from 0.55 to 0.54 mA/cm^2) due to stress treatment. On the other hand, V_{OC} decreases from 2.11 V (fresh PDs) to 1.1 V (stressed PDs), suggesting the defect-related

forward conduction processes are increased due to stress (more details are mentioned in the next section) [24]. In InGaN/GaN MQWs stressed solar cells, Caria et al. [24] observed that the reduction in V_{OC} is much higher than that of J_{SC}. In another work, Huang et al. [23] noticed the same trend of variation in V_{OC} and J_{SC} in similar stressed devices. These reports support the present observation in Figure 7.4. Furthermore, this noteworthy decrease in V_{OC} seems to be the foremost degradation mechanism in the stressed devices. P. Dalapati et al [16] noticed that due to the strong resistive effects in stressed PDs, the photovoltaic properties decreased significantly. To get additional information, the values of shunt resistance (R_{SH}) and series resistance (R_s) for fresh and stressed PDs were calculated from the obtained I–V characteristics (under light) using the following equations

$$R_{SH} = \frac{V_{sc}}{I_{sc}} \tag{7.1}$$

$$R_s = \frac{V_{oc}}{I_{oc}} \tag{7.2}$$

where V_{sc} and I_{oc} are short-circuit voltage and open-circuit current, respectively. Interestingly, the value of R_{SH} decreased from 6850± 342 kΩ (fresh PDs) to 1070± 53 kΩ (stressed PDs), whereas R_s increased from 62± 3.1 kΩ (fresh PDs) to 117± 5.85 kΩ (stressed PDs). The high resistive effects in the stressed PDs could be related to the activation of initially inactive defects [16]. Nevertheless, the strong reduction in R_{SH} as well as the increase in the magnitude of R_s during the stress

treatment might ruin the photovoltaic properties of the detector significantly as observed in Figure 7.4.

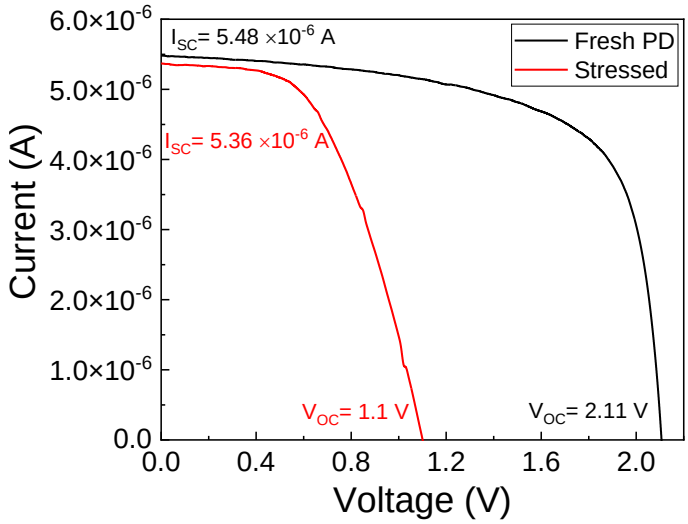

Figure 7.4: I–V characteristics of fresh and stressed PDs measured under standard 1 sun intensity at room temperature.

To evaluate the sensitization performance of the detector, responsivity (R_λ), external quantum efficiency (η), and detectivity (D^*) are often considered [11]. Therefore, to get further insight into the effect of current stress on the spectral sensitivity of the detectors, the values of R_λ, η, and D^* were estimated from the PCS results for fresh and stressed PDs using the following relations [11].

$$R_\lambda = \frac{I_p}{P_{in}} \tag{7.3}$$

$$\eta = \frac{hc \times R_\lambda}{q\lambda} \tag{7.4}$$

$$D^* = \frac{R_\lambda}{(2q \times J_d)^{\frac{1}{2}}} \tag{7.5}$$

where I_p is maximum photocurrent, P_{in} is the incident light power, h is Planck's constant, c is the speed of light, q is the electronic charge, λ is the wavelength of the incident photon, J_d is the dark current density.

It is important to note that the devices show the highest value of R_λ at 382 nm (power of the light used was 10 μW). Therefore, the values of R_λ, η, and D^* were calculated at 382 nm. The estimated values of R_λ, η, and D^* in the fresh PDs are 0.266 ± 0.010 A/W, 85.9%, and 4.32± 0.20 × 10^{11} Jones, respectively. Interestingly, as a consequence of high current stress, the values of R_λ, η, and D^* decrease to 0.257 ± 0.010 A/W, 82.6%, and 0.68± 0.03 × 10^{11} Jones, respectively, in the stressed PDs. These results suggest that the generated defects in the device during the stress treatment ruin the photodetection capability of the detector significantly.

7.6.2 I–V Characteristics

The I–V curves for fresh and stressed PDs were acquired at room temperature and the achieved results are presented in Figure 7.5. For the specific bias-dependent current transport analysis, three different regions, namely, I, II, and III are designated in Figure 7.5. When the devices have been subjected to the constant current stress, the reverse leakage current (region III) increases significantly, suggesting that the parasitic leakage routes, which are usually prompted by severe point defects within or around the MQWs, are activated strongly during the electric current stress treatment [15]. It can be noticed in Figure 7.5 that within 0 to 2 V (region II), the subturn-on forward leakage increases markedly in the stressed PDs, indicating the defect-assisted mechanisms play a paramount role in the carrier transport. In this bias region, the trap-assisted tunneling process can aid in the

motion of numerous electrons and hence, increases the carrier leakage in the device [15]. Region I indicates that both the ideality factor (n) as well as R_S are increased in the stressed PDs. It is interesting to note that in a high-forward bias (region I), the current flow through the stressed PDs at a fixed forward voltage decreases slightly. This decrease of current could be due to the effect of high series resistance in the stressed PDs. In addition, a very good rectification ratio was achieved in fresh PDs which is about 2.91×10^5 at ± 3.5 V. The rectification ratio at ± 3.5 V is defined as ratio between the diode currents measured at + 3.5 V and – 3.5 V, respectively. The value of rectification ratio reduces remarkably to 1.32×10^3 at ± 3.5 V due to long-time current stress treatment. These quantitative results further support the observation of leakage current in stressed PDs, as seen in Figure 7.5.

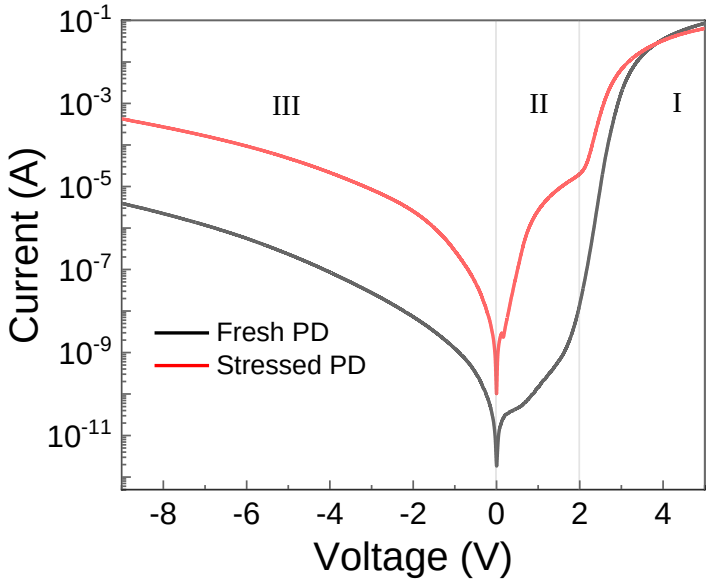

Figure 7.5: I–V characteristics acquired before and after 340 hours of current stress treatments.

Furthermore, the values of ideality factor (n) and junction potential (V_{bi}) were estimated at different temperatures for both PDs (fresh and stressed) to gain further insight into the device physics. The well-known Werner's method was used to

determine the diodes parameters (n, and V_{bi}). The current-voltage characteristics of p-n junctions can be described by thermionic emission, [25] as described in Chapter 4, Section (4.3).

$$I = I_s \left[exp\left(\frac{q(V-IR_s)}{nK_BT}\right) - 1 \right] \tag{7.1}$$

$$I_s = AA^{**}\, T^2\, exp\left(\frac{-qV_{bi}}{K_BT}\right) \tag{7.2}$$

where q is the elementary charge, K_B is Boltzmann's constant, T is the temperature, V_{bi} is the junction potential, A is the effective diode area, A^{**} is the effective Richardson's constant. The forward I– V characteristics for all samples are used to obtain the values of n and V_{bi}.

The estimated values of n and V_{bi} at different temperatures are plotted in Figure 7.6 a and b, respectively. It should be noted that the value of n at room temperature increases from 2.20 ± 0.01 (fresh PDs) to 3.87 ± 0.01 (stressed PDs), suggesting the generation of defects in or around the MQWs active region during the stressing process [26]. However, for both devices, it is evident that the ideality factor increases significantly due to lowering of temperature from 440 K to 100 K as shown in Figure 7.6 (a). In this temperature range, the value of n increases from 1.4 to 12.6 for the fresh PDs, whereas for stressed PDs, it rises from 2.71 to 20.86. Similar trends have also been reported previously [27-29]. This behaviour can be explained by a temperature-activated process due to the current transport across the junction interfaces [30, 31]. In the temperature range of 300-440 K, both devices demonstrated values of n greater than unity and close to 2. A variety of factors may

be responsible for this behaviour. These include generation-recombination mechanisms, interface states, series resistances, and junction potential inhomogeneities [32]. However, the fresh device has a lower value of n than the stressed device, suggesting that the fresh device is closer to ideal diodes than the stressed device. At low temperatures, the higher values of n indicate an additional mechanism to the pure thermionic emission that contributes to the current, namely the thermionic field emission [33]. Another possible reason for the deviation of n values from unity at low temperatures may be due to the presence of generation-recombination centres caused by defects in the GaN, such as deep levels in the forbidden gap [34]. Figure 7.6 b illustrates the temperature dependence of the junction potential for both devices. The junction potential increases linearly with increasing temperature, as seen the linear fits in Figure 7.6 b. However, the fresh device has a slightly larger junction potential than the stressed device which can be attributed to current stress. Junction potential at 100 K and 440 K for the fresh and stressed devices are 0.27 eV and 1.28 eV, and 0.23 eV and 1.24 eV, respectively. The lower value of V_{bi} in the stressed PDs suggests that numerous carriers might reach the defect states easily and enhance the non-radiative recombination mechanism rather than their separation, resulting in a poor photocurrent generation process [15, 16].

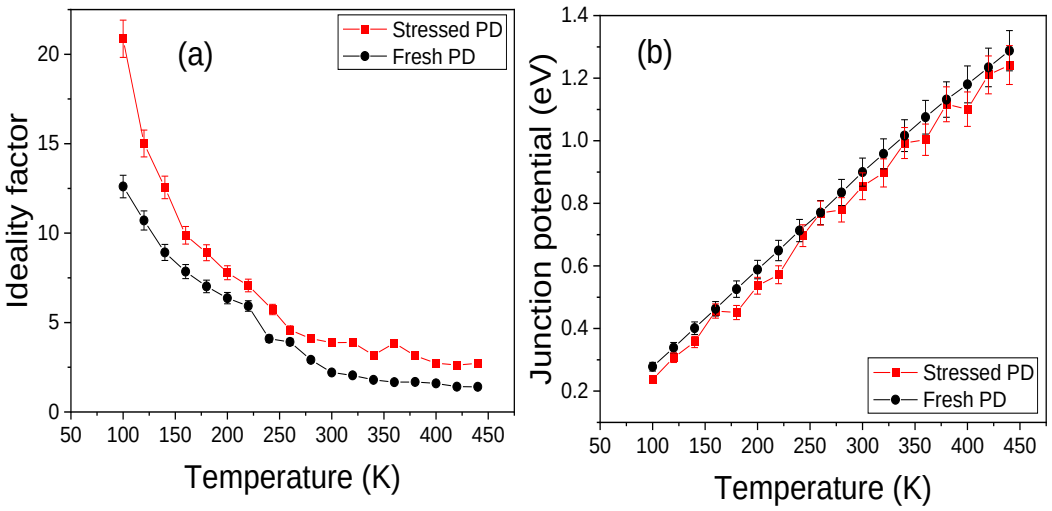

Figure 7.6: Temperature dependence of (a) ideality factor, and (b) junction potential, obtained from I–V characteristics for fresh and stressed PDs.

7.6.3 Analysis Of The C–V Characteristics

The change in the carrier concentration (N_d) during the stress can affect the degradation process strongly [15, 22]. Therefore, quantitative analysis in the change of N_d during the stress is required to understand its role. In this work, to determine the value of N_d, the C–V characteristics of both devices were measured at room temperature using a frequency of 1 MHz and the results are shown in Figure 7.7 (a).

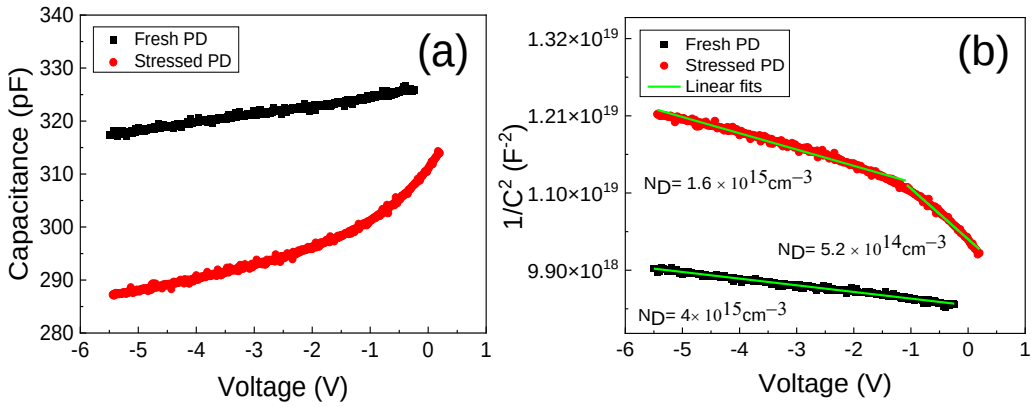

Figure 7.7: (a) C–V plots at room temperature for fresh and stressed PDs. (b) Plot of $1/C^2$ as a function of voltage.

The slope of the best fit of the $1/C^2$ versus reverse bias plot is used to calculate the free carrier concentrations as illustrated in Figure 7.7 b. For the fresh PDs, the free carrier concentration of $4.1 \pm 0.2 \times 10^{15}$ cm^{-3} is consistently uniform, as evidenced by the linear trend exhibited by the plot of $1/C^2$ versus applied bias. However, for the stressed PDs, two lines are fitted to the C–V data, confirming the presence of two different free carrier concentrations of $1.6 \pm 0.1 \times 10^{15}$ cm^{-3} and $5.2 \pm 0.3 \times 10^{14}$ cm^{-3}. This decrease in N_d is probably related to the increase of the number of defects after stress. This will be confirmed in the DLTS section. However, for the stressed PDs, a reduction of the capacitance can be observed, which indicates that one Space-Charges Region (SCR) is reduced and the other involved SCR is widened. This reduction after stress can be attributed to an increase in defect-induced acceptor states, which is most likely to be the cause of a reduction of charge states in p-n SCRs [15]. These defects can be generated during the stress leading to a carrier redistribution in the active region and the induced point defects generated during the degradation process are located within the MQWs region [22].

7.6.4 DLTS And Laplace DLTS Characteristics

To determine the presence and properties of defects in the investigated PDs structures that can affect their degradation, DLTS measurements for both fresh and stressed PDs were performed. DLTS technique has been previously employed to evaluate the effects of current stress on electrically active defects [35]. In the present work, the adopted experimental DLTS parameters are: a reverse bias V_R = -0.5 V and V_R = -5 V, a filling pulse height V_P = 0V, a filling pulse time t_P = 1 msec, and a rate window of 500 s^{-1}. As illustrated in Figure 7.8, the DLTS signals have been plotted against temperature for only the stressed PDs over the scanned

temperature range of 10-450 K. It is worth noting, no signals have been detected by DLTS in the fresh devices. This could be due to the fact that no defects are present in the fresh samples, or they have very low concentrations beyond the detection limit of DLTS. However, the stressed PDs exhibit only one negative peak at both reverse biases as shown in Figure 7.8. It is evident in Figure 7.8 that the amplitude of the DLTS signal increases with increasing reverse bias (away from the interface). This indicates that the concentration of the trap increases away from the interface.

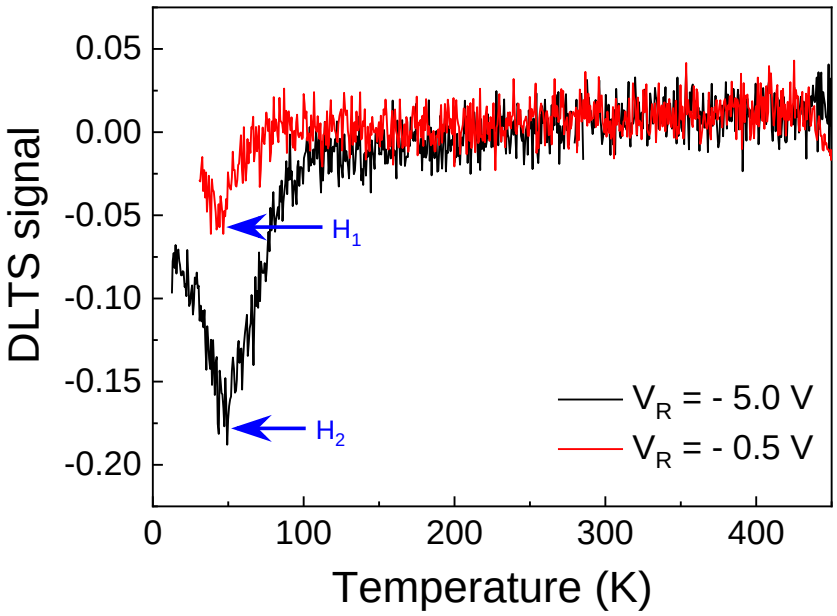

Figure 7.8: DLTS spectra for the stressed devices at V_R = -0.5 V and V_R = -5 V.

Since the DLTS peaks are broad, Laplace DLTS (LDLTS) measurements were carried out to resolve these peaks [36]. LDLTS measurements show only one hole trap (H_1) and two hole traps (H_1, H_2) at reverse biases V_R = -0.5 V and V_R = -5 V, respectively. The activation energies of these traps are determined from the Arrhenius plots as shown in Figure 7.9. A summary of these traps parameters,

including the activation energy, the trap concentrations, and the capture cross-section, is presented in Table 7.1.

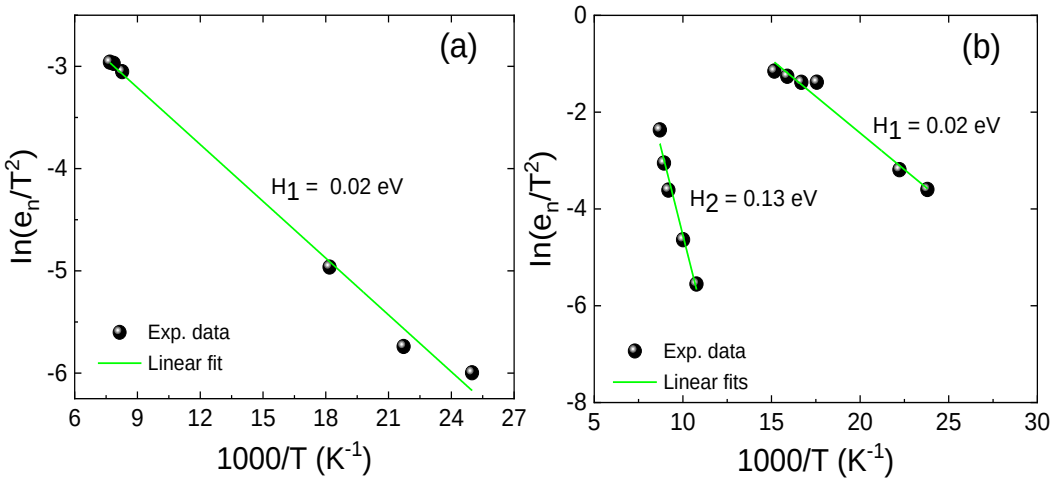

Figure 7.9: Arrhenius plots for the stressed device obtained from Laplace DLTS at (a) V_R= -0.5 V, and (b) V_R= -5 V.

Table 7.1: Traps parameters for the stressed device at V_R= -0.5 V and V_R = -5 V, V_P= 0 V, and t_P = 1 msec.

V_R (V)	**Trap**	**Activation energy (eV)**	**Trap concentration (cm^{-3})**	**Capture Cross-Section (cm^2)**
-0.5	H_1	0.020 ± 0.001	$5.5\pm0.3\times10^{11}$	$8.2\pm0.4\times10^{-23}$
-5	H_1	0.020 ± 0.001	$1.5\pm0.1\times10^{12}$	$1.4\pm0.1\times10^{-20}$
	H_2	0.13 ± 0.01	$1.8\pm0.1\times10^{18}$	$9\pm0.45\times10^{-18}$

As shown in Table 7.1, the trap H_1 with an activation energy of 0.02 eV is observed in the stressed device at both reverse biases (V_R = -0.5 V and -5 V), indicating that this trap exists near and away from the junction interface. A similar shallow trap (D1) with an activation energy of 0.07 eV has been reported in 100 mA stressed InGaN/GaN structure grown on SiC substrates [37]. This trap, which is found to be

the cause of the device degradation after current stress, may originate from the evolution of Mg complexes and the generation of NRCs during growth. This shallow trap has also been observed in AlGaN/InGaN/GaN heterostructures before current stress with similar activation energy (0.07 eV), however, no explanation was given regarding its possible origin [38]. In addition, the authors in Ref. [38] have not detected any deep traps in AlGaN/InGaN/GaN heterostructures. The capture cross-section of the H_1 trap at V_R = -0.5 V is 8.2 ± 0.4 × 10^{-23} cm^2, whereas it is higher (1.4 ± 0.1 × 10^{-20} cm^2) at V_R = -5 V. Its concentration at V_R = -0.5 V (near interface) and V_R = -5 V (away from interface) as determined from LDLTS is 5.5 ± 0.3 × 10^{11} cm^{-3} and 1.5 ± 0.1 × 10^{12} cm^{-3}, respectively. These results, which agree with the observed amplitude of the DLTS signal, confirm that the trap is more concentrated away from the interface of the junction. The additional H_2 trap with an activation energy of 0.13 ± 0.11 eV and concentration of 1.8± 0.1 × 10^{18} cm^{-3} is observed in stressed PDs only at a reverse base V_R = -5 V (away from the interface). A similar deep defect with activation energy of 0.12 eV, labeled as trap A, has been detected in unstressed and stressed devices at different direct currents of 50 mA and 100 mA [39]. It is consistent with the predictions of the presence of Mg-related shallow acceptors, including Mg_{Ga} and Mg-H_2 complexes, which can form p-type layers as a result of the breaking of the Mg-H chemical complexes due to high heating levels during the aging treatment [38]. This trap with activation energy in the range of 0.12-0.14 eV is observed in GaN/InGaN MQWs structures as well and was attributed to a freeze out of Mg acceptors [40, 41]. Moreover, the generation of these traps can be attributed to current stress. The induced stress generates point defects or dislocations, which can cause the sub-threshold region to increase and the ideality factor also to increase after stress, indicating the generation of point

defects or dislocations [26]. Furthermore, these defect induced acceptor states are most likely to be the cause of the reduction of the capacitance [15] and carrier redistribution [22].

7.7 Conclusions

In summary, InGaN/GaN MQWs UV-PDs were fabricated with an Al_2O_3 passivation layer and a systematic study was carried out to understand the root mechanisms that could account for the degradation of the device performances due to constant current stress by employing several combined optical and electrical measurements. The obtained EL spectra suggest that the EL intensity decreases by about 48% in the stressed PDs due to 200 mA of current stress over 340 hours. This indicates that more of the charge carriers are captured by the newly created defects in the active region. In the stressed PDs, the reduction in V_{OC} is much larger than J_{SC}, indicating that V_{OC} seems to be the leading degradation mechanism in devices. The strong reduction in V_{OC} can be ascribed to the enhancement of the defect-related forward conduction processes in the stressed PDs. The dark I–V measurements suggest that in the stressed PDs, the dramatic increase of the reverse and forward leakage currents suggests that the parasitic leakage routes, which are usually prompted by severe point defects within or around the MQW, are activated largely during the stress treatment. Furthermore, the temperature dependence of I–V characteristics in the stressed PDs suggests that within 100-440 K, the values of ideality factor (junction potential) are always higher (lower) than that of the fresh devices, indicating the existence of generation-recombination centres caused by the created defects. It is important to mention that the source of the leakage currents in the stressed PDs could be due to the two major trap levels observed in the LDLTS

spectra and having different activation energies. However, based on the obtained results, it is assumed that the degradation mechanisms in the stressed PDs are strongly associated with the activation of initially inactive defects, mainly Mg-related shallow acceptors, including Mg_{Ga} and Mg-H_2 complexes. The worsening of device performances is closely attributed to the activation of acceptor levels in stressed PDs as confirmed by LDLTS analysis. Finally, due to the stress treatment, the sensitization performance of the detector decreases significantly in stressed PDs, suggesting the generated defects in the device can ruin their photodetection performance largely.

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CHPTER 8: INVESTIGATION OF DEEP DEFECTS AND THEIR EFFECTS ON THE PROPERTIES OF NiO/β-Ga_2O_3 HETEROJUNCTION DIODES

8.1 Introduction

In this study, the effects of rapid thermal annealing (RTA) on the electrical and optical properties of NiO/β-Ga_2O_3 heterojunction diodes were investigated using capacitance-voltage, current-voltage, Deep Level Transient Spectroscopy (DLTS), Laplace DLTS, photoluminescence and micro-Raman spectroscopy techniques, and SILVACO-TCAD numerical simulator. The NiO/β-Ga_2O_3 structure, which was designed with NiO low-doped and fully depleted at zero bias, allowed the study of the properties of β-Ga_2O_3 and its interface with NiO. Micro-Raman results revealed good agreement with the theoretical and experimental results reported in the literature. The photoluminescence intensity of the sample after RTA is five times higher than the fresh sample due to a rise in the density of gallium and oxygen vacancies (V_{Ga} + V_O) in the annealed β-Ga_2O_3 samples. The current-voltage characteristics showed that the annealed devices exhibited a lower ideality factor at room temperature and higher junction potential compared with fresh samples. The DLTS measurements demonstrated that the number of electrically active traps were different for the fresh and annealed samples. In particular, three and one electron traps were detected in fresh samples and annealed samples, respectively. SILVACO-TCAD was used to understand the distribution of the detected electron trap E_2 (E_c-0.15 eV) in the fresh sample and the dominant transport mechanisms. A fairly good agreement between simulation and measurements was achieved by

considering a surface NiO acceptor density of about 1×10^{19} cm^{-3} and a uniformly distributed E_2 trap from the surface of β-Ga_2O_3 layer to about 0.220 μm. These results unveil comprehensive physics in NiO/β-Ga_2O_3 heterojunction and suggest that RTA is an essential process for realizing high-performance NiO/β-Ga_2O_3 devices.

8.2 Background

Ultra-wide bandgap (UWBG) semiconductor gallium oxide (Ga_2O_3) is an excellent candidate for the next generation power devices, owing to its very large bandgap of ~4.8 eV, high theoretical breakdown electric field of ~8 MV/cm, and availability of affordable native substrates [1-3]. By taking advantage of these superior physical properties, β-Ga_2O_3 power devices can potentially achieve higher switching frequency, smaller switching losses and higher operation temperatures compared with same current- and breakdown voltage- rated Si, SiC and GaN counterparts [4-6]. To enhance the performance of β-Ga_2O_3, various device structure innovations have been demonstrated in recent years to advance the device figure-of-merits (FOM) as well as pushing Ga_2O_3 towards circuit applications [7, 8]. Among device innovations, different edge termination structures were designed to reduce electric field crowding at the junction periphery. These include mesa, trench, field plate, guard ring, and ion-implanted terminations [9-13].

There are many attempts to develop a stable p-type β-Ga_2O_3 [14-17] in order to form heterojunctions with the well-established n-type β-Ga_2O_3. However, other p-type materials have been considered to form stable heterojunctions with β-Ga_2O_3 with the aim to achieve high breakdown voltage, lower leakage current and to potentially enhance ruggedness of β-Ga_2O_3 power devices [4, 18, 19]. Different p-

type semiconductors such as Cu_2O, Ir_2O_3, Ag_2O, CuI and NiO were employed to produce p-n heterojunctions with β-Ga_2O_3 [20-23]. Among these p-type materials, NiO is promising for achieving high performance NiO/β-Ga_2O_3 heterojunction diodes (HJDs) due to its easy deposition by sputtering and controllable hole concentration stemming from the nickel vacancy [24]. The NiO/β-Ga_2O_3 system has shown excellent voltage blocking capability. A high breakdown voltage of 1.86 kV and a specific on-resistance of 10.6 mΩcm^2 was reported by using a double-layer NiO [18]. Recently, an improved breakdown voltage of 2.41 kV has been demonstrated based on NiO/β-Ga_2O_3 HJDs with small-angle beveled field plate, achieving a record Baliga's FOM of 5.18 GW cm^{-2} [4].

Despite the progress made on NiO/β-Ga_2O_3 HJDs, they still suffer from serious leakage current and premature voltage breakdown [20, 25]. These problems may originate from defect states in β-Ga_2O_3 and the NiO/β-Ga_2O_3 interface. A deep energy level state below the conduction band (E_C) of E_C-0.72 eV was found to be responsible for reverse leakage path in β-Ga_2O_3 Schottky diodes (SBDs) [25]. Even an incomplete ionization of a 110 meV level defect state in unintentionally doped *β*-Ga_2O_3 may increase the ON-state resistance, decrease the breakdown voltage and cause instabilities of power devices [26]. Hence, it is of vital importance to identify the defect states in β-Ga_2O_3 and NiO/β-Ga_2O_3 interface, which is remarkably beneficial for unveiling voltage breakdown and transport mechanisms, as well as improving the reliability of β-Ga_2O_3 power devices. DLTS, as an efficient and powerful method used for observing and characterizing deep level impurities in semiconductors, was widely used in β-Ga_2O_3. Zhang *et al.* reported five majority traps spread throughout the Ga_2O_3 energy bandgap using DLTS and optical DLTS (ODLTS) in Ni/Ga_2O_3 SBDs [27]. A DLTS study of defects in Ga_2O_3:Zr crystals

has only shown relatively shallower deep levels [28]. While in β-Ga_2O_3 grown on two differently oriented substrates to realize SBDs, DLTS has identified two deep levels relatively close to the conduction band [29]. Most of the DLTS efforts are based on β-Ga_2O_3 SBDs. To reveal the defect states in NiO/β-Ga_2O_3 system, a p^+ NiO/n^- β-Ga_2O_3 HJD was fabricated to investigate the majority and minority carrier traps. Energy levels below the conduction band (E_C) and above the valence band (E_V) of E_C-(0.75–0.79) eV and E_V+0.14 eV were identified to be electron and hole traps, respectively [30]. However, the p^+ NiO/n^- β-Ga_2O_3 HJDs used in the aforementioned work has a very shallow depletion into NiO at reverse biases (i.e., unpunched-through NiO). Therefore, it is difficult to exclude the defect states in NiO measured by DLTS. On the other hand, to achieve a high performance NiO/β-Ga_2O_3 HJD, annealing is an effective way to improve both bulk and heterointerface quality, however, the relevant physics has not been fully understood.

To address these gaps, in this work, the structure of NiO/β-Ga_2O_3 HJDs was designed with a punched-through NiO layer to guarantee that the DLTS signals are detected only from β-Ga_2O_3 bulk and NiO/β-Ga_2O_3 interface. DLTS measurements were carried out on fresh and annealed HJDs devices. By combining experimental and modeling, this work aims at understanding NiO/β-Ga_2O_3 HJDs and revealing the dominant conduction mechanisms before and after annealing.

8.3 Samples Details

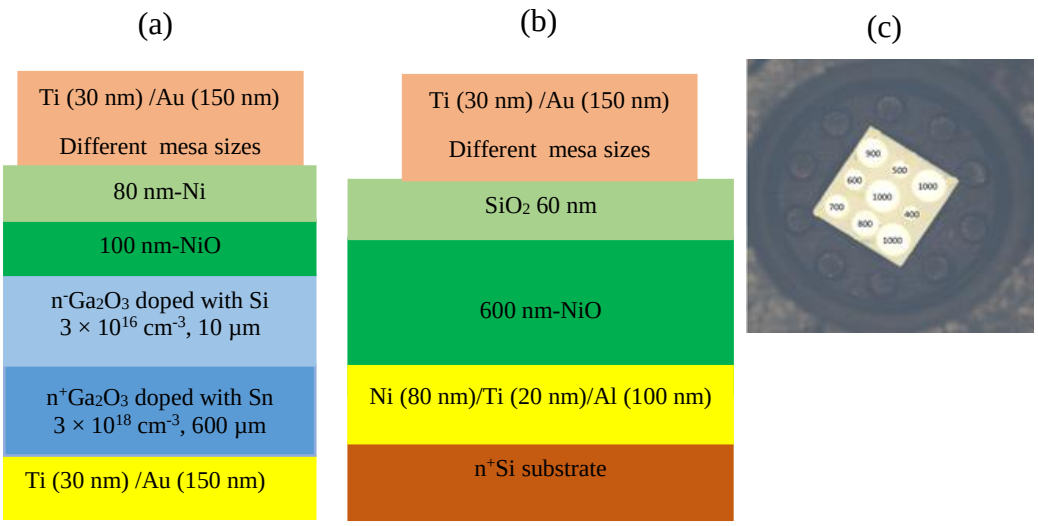

Figure 8.1: Schematic cross-section of (a) NiO/β-Ga_2O_3 HJD, (b) metal/SiO_2/NiO MOS (metal oxide semiconductor) structure for C-V tests, (c) top view of electrical mesas (top contacts) with different diameters.

Figure 8.1 (a) shows the cross-section schematics of the NiO/β-Ga_2O_3 HJD. The epitaxial structure consists of a 10-μm thick Si-doped n^- Ga_2O_3 drift layer (n^- = ~3×10^{16} cm^{-3}) grown by hydride vapor phase epitaxy (HVPE) on 600 μm (001) Sn-doped n^+ Ga_2O_3 substrate. The fabrication process of the NiO/β-Ga_2O_3 HJD was commenced by depositing the back Ohmic contact of Ti/Au (30/150 nm) using electron beam evaporation (EBE), followed by rapid thermal annealing (RTA) at 470 °C in N_2 atmosphere for 1 min. A 100 nm NiO layer was then sputtered on top of the β-Ga_2O_3 drift layer in pure Ar gas ambient with a flow rate of 60 sccm. This was followed by sputtering a 80 nm thick Ni layer. Finally, the sample was immediately transferred to an electron beam evaporator where a 30 nm/150 nm Ti/Au metal stack was deposited as the anode pad. Photolithography lift-off process was then used to define circular mesas with different sizes for electrical characterisation as shown in Figure 8.1 (c). RTA post-annealing was performed at

225 ℃ in N_2 atmosphere for 15 min to improve Ga_2O_3/NiO interface quality. In order to characterize the acceptor concentration (N_A) in NiO, a metal/SiO_2/NiO MOS (Metal Oxide Semiconductor) structure was fabricated, as shown in Figure 8.1 (b). Highly-doped n-type Si wafer was utilized as the substrate. Ni/Ti/Al metal stack with thickness of 80/20/100 nm was deposited by EBE. NiO layer was sputtered using the same process mentioned above. Then 60 nm SiO_2 was deposited by plasma enhanced chemical vapor deposition (PECVD), followed by deposition of Ti/Au (30/150 nm) electrode. The p-type doping of NiO originates from nickel vacancies [31]. Generally, the N_A value in NiO can be modulated by tuning the Ar/O_2 flow ratio during the sputtering process [32]. The lowest N_A value that can be achieved is when there is no O_2 gas flow during the sputtering process. In this work, the NiO was deposited in pure Ar atmosphere with the aim to obtain a very low N_A value which is required to achieve a fully depleted NiO layer.

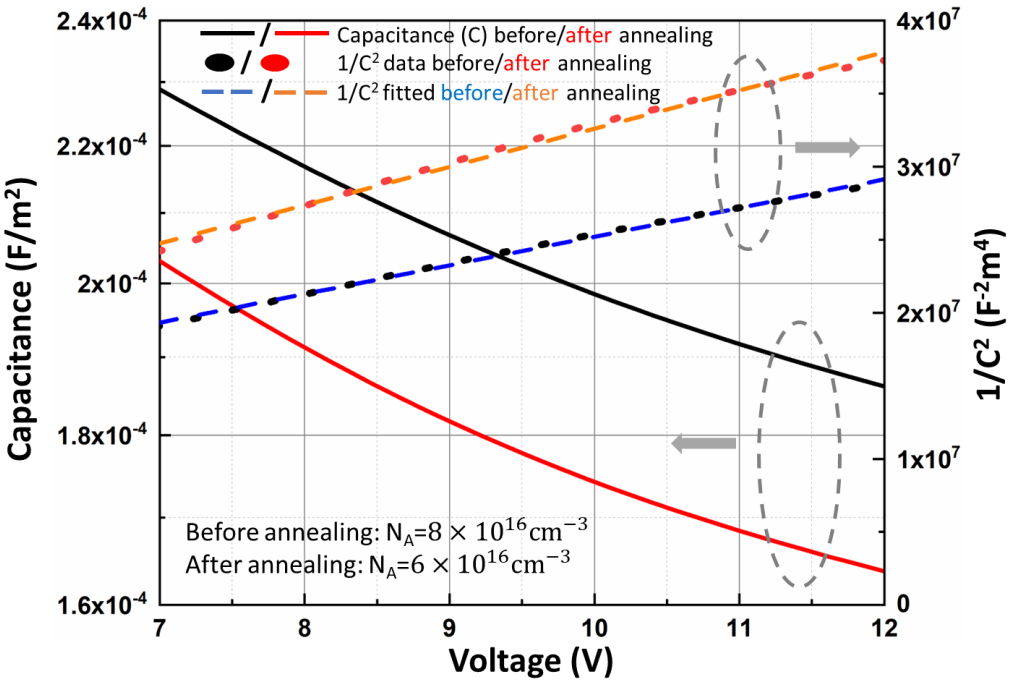

Figure 8.2: C-V, $1/C^2$-V data and fitted $1/C^2$-V plots of the metal/SiO_2/NiO MOS measured at 1 kHz for NiO before and after annealing.

Figure 8.2 (a) and (b) show the capacitance-voltage (C-V), $1/C^2$-V data and fitted $1/C^2$-V plots of the MOS structures measured at frequency of 1 kHz, before and after the RTA of NiO. The extracted N_A in the NiO before and after annealing is about $8.0 \pm 0.4 \times 10^{16}$ cm^{-3} and $6.0 \pm 0.3 \times 10^{16}$ cm^{-3}, respectively. Due to the low N_A and small thickness of NiO, the NiO is totally depleted at zero bias in the NiO/β-Ga_2O_3 HJD. Therefore, the defect states in NiO can be easily excluded for DLTS analysis.

8.4 Optical Characterization

8.4.1 Micro-Raman Spectroscopy

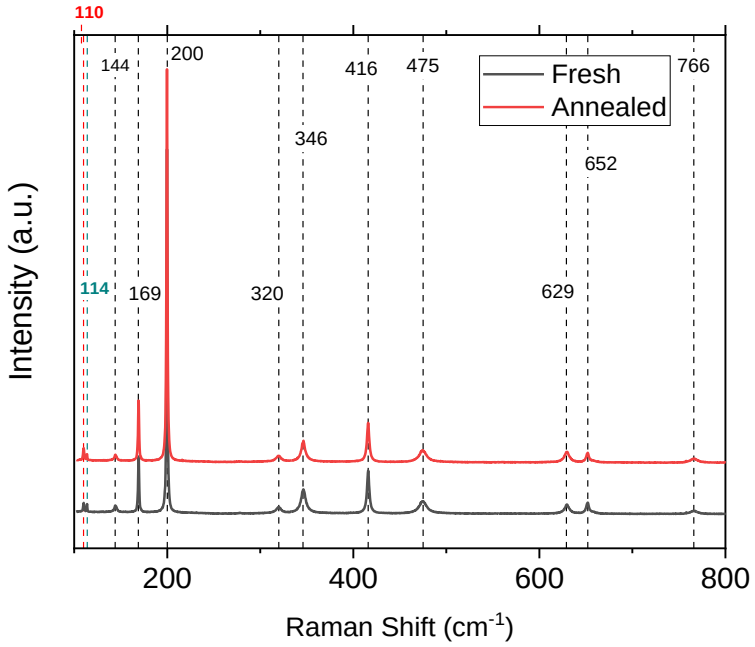

Figure 8.3: Raman spectra of fresh and annealed β-Ga_2O_3 samples.

The Raman spectra of the fresh and annealed Ga_2O_3 samples are similar (Figure 8.3). Comparing the spectra, no important frequency shift, linewidth variation, or

relative intensity change was observed. Particularly, Raman peaks at 110, 114,144, 169, 200, 320, 346, 416, 475, 629,652, and 766 cm^{-1} were observed. The wavenumbers and width of Raman peaks are in good agreement with the theoretical and experimental results reported in the literature for β-Ga_2O_3 phase, with a monoclinic structure and belongs to the C^3_{2h} space group [33-39]. The nature of the observed peaks depends on the frequency range [33, 35, 38, 39]: for $\omega < 210\ cm^{-1}$, they are associated with the low-frequency vibration and translation motion of tetrahedron (GaO_4)–octahedron (Ga_2O_6) chains; for $300\ cm^{-1} < \omega < 500\ cm^{-1}$, they are attributed to the deformation of tetrahedron and octahedron; finally, for $\omega > 500\ cm^{-1}$ region is related to the high-frequency stretching and bending of tetrahedra. The sharp and high-intensity Raman peaks indicate that both β-Ga_2O_3 samples (fresh and annealed) have high crystallinity. From Raman results, it is also possible to conclude that there is no appreciable change in the crystalline structure after thermal treatment.

8.4.2 Photoluminescence Spectroscopy

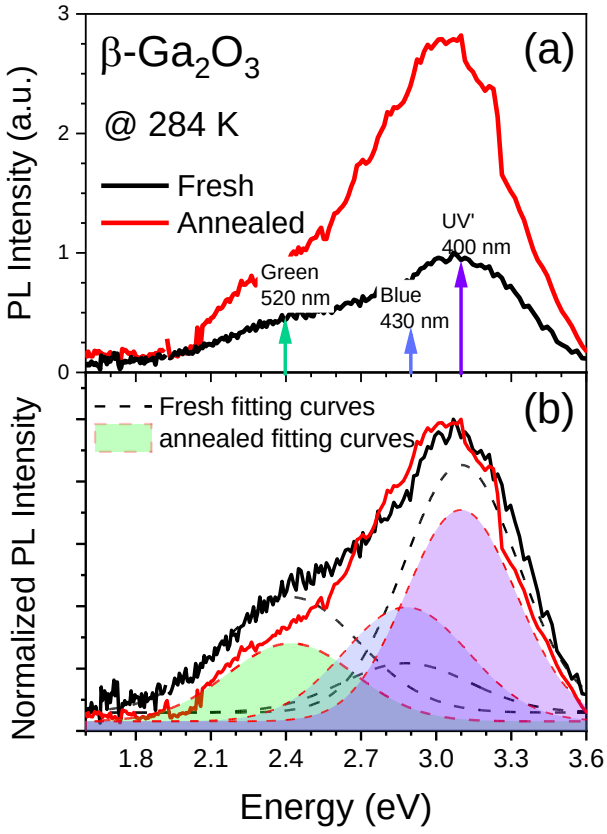

Figure 8.4: (a) PL spectra of fresh and annealed β-Ga_2O_3 samples at 284 K present a strong enhancement of intensity after annealing; (b) normalized PL spectra allow the visualization of the role of each defect complex.

Figure 8.4 (a) shows typical below bandgap excitation PL spectra of fresh and annealed β-Ga_2O_3 samples at a temperature of 284 K by using a UV laser (λ = 325 nm) as excitation source with a power of 30 mW. The broad spectra present a stronger blue band at around 3.0 eV with a weaker green tail at low energies characterized by a band centred at 2.48 eV. It is worth noting that the PL intensity increases about five times after RTA while the PL peak position did not show significant change with thermal annealing. In general, the PL spectrum of β-Ga_2O_3 samples presents several broad bands from UV to the visible region that depend on

the doping and different post-treatments [40]. The optical bandgap of single-crystal β-Ga_2O_3, usually measured by absorption techniques, is around 4.8 eV for undoped samples [41]. When excited above bandgap, there are four typical PL bands related to β-Ga_2O_3 at around 3.40 eV (UV), 3.10 eV (UV'), 2.95 eV (blue), and 2.48 eV (green) [40, 42]. The UV band at 3.4 eV (wavelength=360 nm), which is usually independent of the presence of impurities, decreases fast in intensity with increasing temperature, and has been attributed early on to electron recombination with a self-trapped hole (STH) [40].

The UV' (3.1 eV or wavelength =400 nm) and blue PL bands in undoped β-Ga_2O_3 samples were previously associated with the recombination of electrons and holes trapped at an acceptor site [35, 37]. The type of donors that contribute to the PL are not well understood but they are usually associated with shallow donors [35, 37]. such as unintentional doping or Ga_i (Ga interstitial). It is important to point out that samples in this study are doped intentionally using Si atoms, which are shallow donors in β-Ga_2O_3 semiconductor materials. The presence of Si increases further the total density of donors in samples. Gallium vacancy (V_{Ga}), divacancy ($V_{Ga} + V_O$) and interstitial oxygen (O_i) have been suggested as acceptor levels [40]. Recent studies have confirmed that transitions involving $V_{Ga} + V_O$ acceptor levels could explain the nature of the blue PL band [40]. In addition, deeper electronic levels in the bandgap are responsible for the lower energy emissions [40]. The green PL band at around 520 nm indicates the presence of oxygen-related defects originating from the recombination of electrons with holes trapped by interstitial oxygen (O_i) [40]. The energy positions of these three PL bands are indicated in Figure 8.4 (a) for clarity. A deconvolution of the spectra in UV', blue, and green regions by Gaussian curves (dashed lines) shows interesting features. In general, an increase

of PL intensity after thermal annealing is observed. Similar enhancements of PL intensity after annealing have been reported previously [43, 44]. In addition, the PL spectra in the UV' range exhibit a similar profile as compared to the PL of the fresh sample as evidenced in the normalized spectra shown in Figure 8.4 (b). Furthermore, a relative decrease in the lower energy tail is observed for the annealed sample. It is worth noting that the relative intensity of the blue increases after annealing. In contrast, the relative intensity of the green band decreases. As the blue PL band is associated with the recombination of holes trapped at an acceptor site (acceptors: gallium vacancy (V_{Ga})) or the divacancy ($V_{Ga} + V_O$) [40], the results would indicate an increase of such V_{Ga} vacancies, which is consistent with previous studies reported in the literature [45, 46]. On the other hand, as mentioned above the green PL band, which is correlated to holes trapped at Oi, has shown a decrease of the relative PL intensity after thermal annealing. The observed changes of relative intensity of these bands after thermal annealing and the details of the nature of these PL bands in β-Ga_2O_3 are not well understood yet. Further studies are needed to shed some light on their origins.

8.5 Electrical Characterization

8.5.1 Current-Voltage Characteristics

The current-voltage characteristics (I-V) as a function of temperature (200-340 K with 20 K intervals) were measured on fresh and annealed NiO/β-Ga_2O_3 p-n diodes in order to determine three key factors: ideality factor (n), junction potential (V_{bi}), and series resistance (R_s).

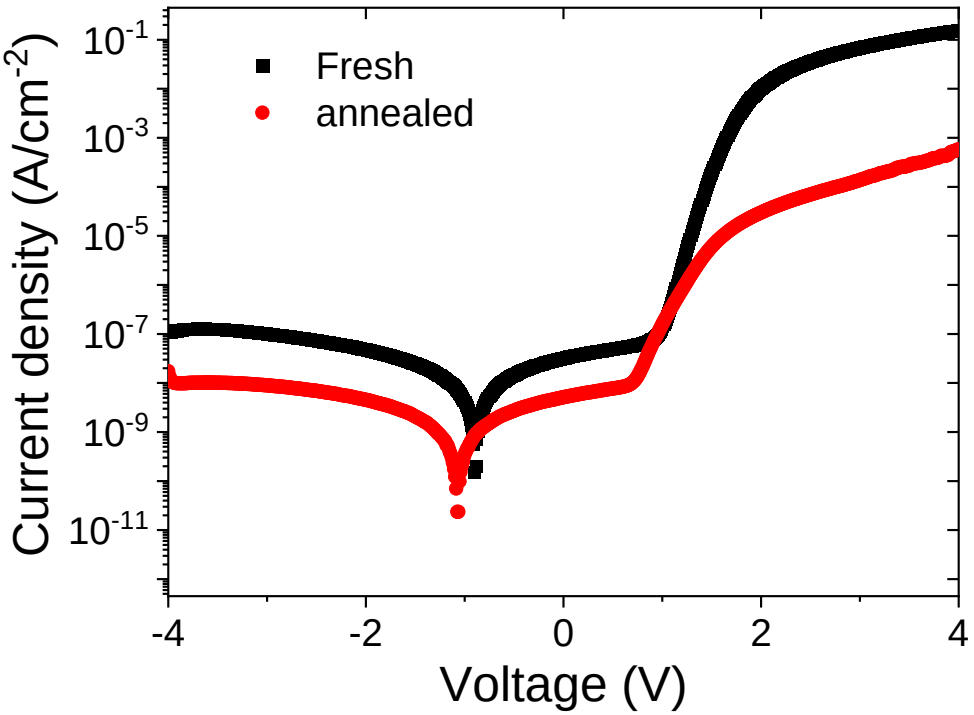

Figure 8.5: J-V plots for both fresh and annealed samples.

Figure 8.5 shows a semi-logarithmic current density versus voltage plot (J-V) for fresh and annealed samples at room temperature. Both samples have relatively low leakage current densities. Figure 8.5 shows that the annealed samples exhibit a lower reverse current density than the fresh samples. The reverse bias current densities at -4 V before annealing and after annealing are 1.17 x 10^{-7} A/cm^{-2} and 1.19 x 10^{-8} A/cm^{-2}, respectively. This reduction in reverse current density indicates improved electrical characteristics of the device as a result of the thermal annealing process. A similar behaviour has been observed in previous studies on NiO/β-Ga_2O_3 p-n diodes, where the reverse current was found to rapidly decrease after annealing the device in a nitrogen atmosphere for 3 minutes at 350 °C [47]. In addition, it is assumed that the lower reverse current observed in the annealed samples is due to a reduction of the number of deep defects or to their concentrations, which act as generation recombination centres [48]. The

assumptions will be further investigated using DLTS. In the heterojunction junction, thermionic current at the band discontinuity is very important. In fact, it is believed that the thermionic emission mechanism is usually predominant in metal-semiconductor Schottky contacts which can be regarded as a special case of heterojunctions [49].

Current-voltage characteristics of heterogeneous p-n junctions can be described by thermionic emission, as given below [49, 50] (see also Chapter 4, Section (4.3)):

$$I = I_s \left[exp\left(\frac{q(V - IR_s)}{nK_BT}\right) - 1 \right] \tag{8.1}$$

$$I_s = AA^* T^2 \, exp\left(\frac{-qV_{bi}}{K_BT}\right) \tag{8.2}$$

where q is the elementary charge, n is the ideality factor, K_B is Boltzmann's constant, T is the temperature, V_{bi} is junction potential, R_s is the series resistance, A is the effective diode area (A = 2.12 × 10^{-3} cm^2 and 8.1 × 10^{-3} cm^2 for fresh and annealed samples, respectively) and A^{**} is the effective Richardson's constant. The diode parameters (n, V_{bi} and R_s) were calculated as described in chapter 4 section (3.4) [51]. The forward I-V characteristics for all samples are used to obtain the series resistance, ideality factors (n), and junction potential (V_{bi}). These parameters are summarized in Table 8.1.

Table 8.1: Ideality factor (n), junction potential (V_{bi}) and series resistance (R_s) at room temperature for fresh and annealed devices.

Device	n	V_{bi} (eV)	R_s (Ω)
Fresh	2.33 ± 0.1	0.68 ± 0.03	0.30 ± 0.01
Annealed	1.74 ± 0.07	0.76 ± 0.03	130 ± 6.1

The ideality factor in forward bias for fresh and annealed samples, as shown in Table 8.1 , deviates from unity, but it is worth noting that the ideality factor value of annealed sample is much lower than that of fresh sample. This reduction of ideality factor was reported in NiO/β-Ga_2O_3 p-n diodes after annealing process, demonstrating that thermal treatment can significantly enhance the quality of NiO/Ga_2O_3 p-n interface and reduce the interface recombination caused by defects [47]. Additionally, if one considers that the ideality factor is around 2 in both samples, then this value is comparable to those obtained for NiO/β-Ga_2O_3 heterojunction diodes reported by Kokubun et al. [21] and Peter et al. [52]. This indicates that the current may be limited by recombination [53, 54]. The junction potential values of the annealed and fresh samples were calculated as 0.76 and 0.68 eV at room temperature, respectively. The junction potential value of annealed diodes is higher than fresh samples. This slight difference of junction potential after annealing could be due to the rapid thermal annealing process. R_s is dominated by the lightly-doped NiO. Its increase after annealing suggests a reduction of hole concentration.

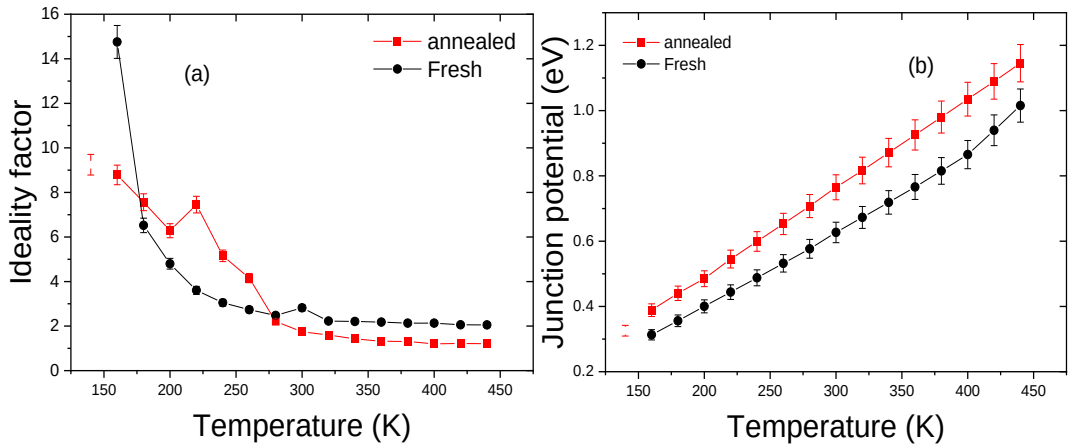

Figure 8.6: Temperature dependence of (a) Ideality factor; (b) junction potential, obtained from I-V characteristics.

Figure 8.6 (a) and (b) show the temperature dependence of the ideality factor and junction potential for fresh and annealed samples over the temperature range 100 K to 440 K, respectively. Interestingly, the ideality factor decreased with increasing temperature while the junction potential increased. It is worth pointing out that similar observations were reported both in β-Ga_2O_3 materials [55-57] and in the AlGaN MQW based LEDs and InGaN/GaN based UV-photodetectors discussed in Chapters 6 and 7. These changes as a function of temperature are related to inhomogeneous interfaces caused by interfacial traps. According to the inhomogeneity theory, the junction potential can be considered as a Gaussian distribution, and with increasing temperature it is expected that electrons located at high energies will dominate the transport mechanism and cause the barrier to become higher. The very high value of the ideality factor at low temperatures is related to the tunneling current domination, however, with increasing temperature the thermionic transport mechanism dominates [58]. At 225 K, the ideality factor does not follow the decaying behaviour as a function of temperature, i.e. increases,

indicating a possible change in the transport mechanism of charge carriers across the interface

8.5.2 Capacitance-Voltage Characteristics

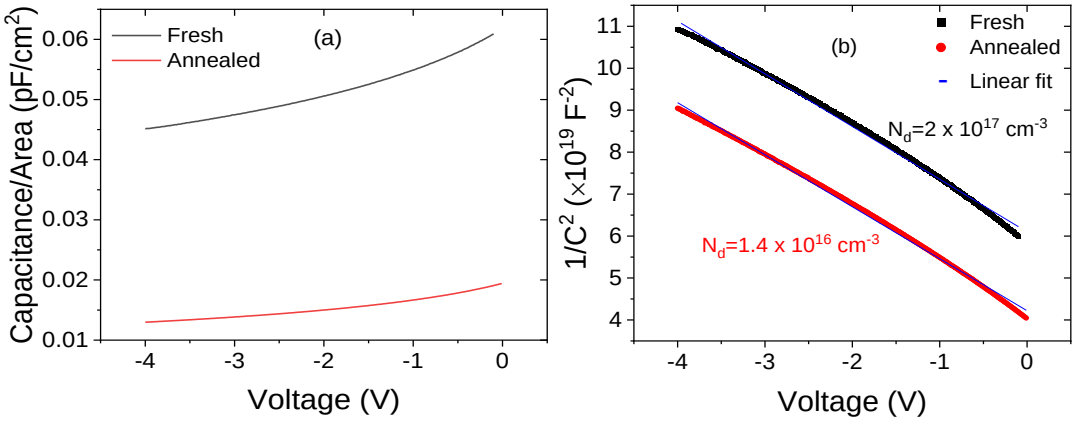

Figure 8.7: (a) Plots of C-V characteristics and (b) $1/C^2$ versus V plots for fresh and annealed samples at room temperature (RT).

Capacitance-voltage measurements were performed at room temperature with a frequency of 1 MHz for both samples and are presented in Figure 8.7 (a). As NiO is fully depleted at zero bias, the plot of $1/C^2$ vs V shown in Figure 8.7 (b) can be used to estimate the donor concentration (N_d) in Ga_2O_3. The straight line for both diodes indicates that the doping profiles are homogeneous. The N_d values were found to be $2.0 \pm 0.1 \times 10^{17}$ cm^{-3} and $1.4 \pm 0.1 \times 10^{16}$ cm^{-3} for the fresh and annealed samples, respectively. The annealed sample exhibits lower value of free carrier concentration as compared with the fresh sample. The high N_d in the fresh sample could be due to surface contamination or Si surface congregation that could have occurred during the epitaxial growth.

8.5.3 DLTS And L-DLTS Measurements

DLTS technique has been used to investigate the effects of post growth annealing on electrically active defects in Ga_2O_3 or near the Ga_2O_3/NiO interface [59]. The experimental DLTS parameters used were: a reverse bias V_R = -2 V, a filling pulse height V_P = 0V, a filling pulse time t_P = 1 msec, and a rate window of 500 s^{-1} as shown in Figure 8.8.

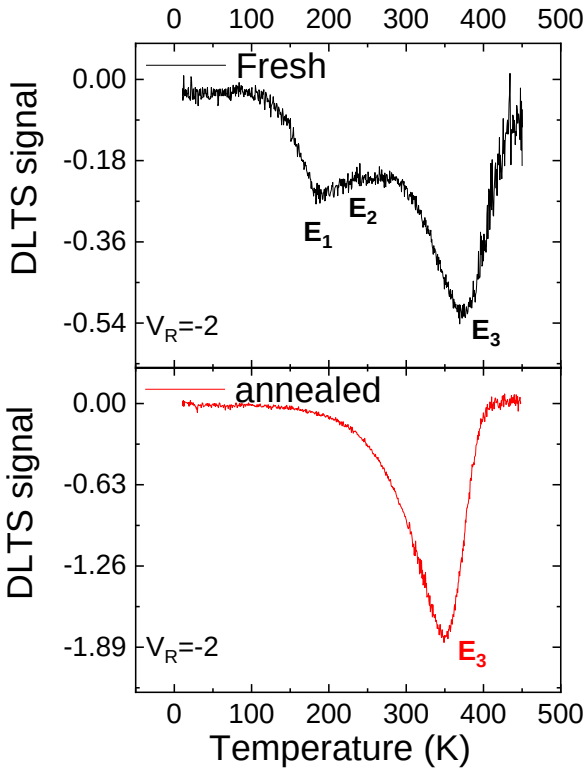

Figure 8.8: DLTS spectra for fresh and annealed devices V_R = -2 V.

Figure 8.8 illustrates a typical DLTS spectrum for both samples. In fresh sample, three negative peaks are detected in the temperature range 100 K - 400 K, which correspond to three electron traps labelled as E_1, E_2 and E_3. After annealing, it is clear from Figure 8.8 that the post-growth annealing process reduces the number of traps to only one electron trap E_3. To resolve the broad DLTS peaks, Laplace DLTS

(LDLTS) measurements [60] were carried out. The activation energies of these traps were determined from Arrhenius plots as shown in Figure 8.9. A summary of these trap parameters, including the activation energy, the trap concentrations, and the capture cross-section, is presented in Table 8.2.

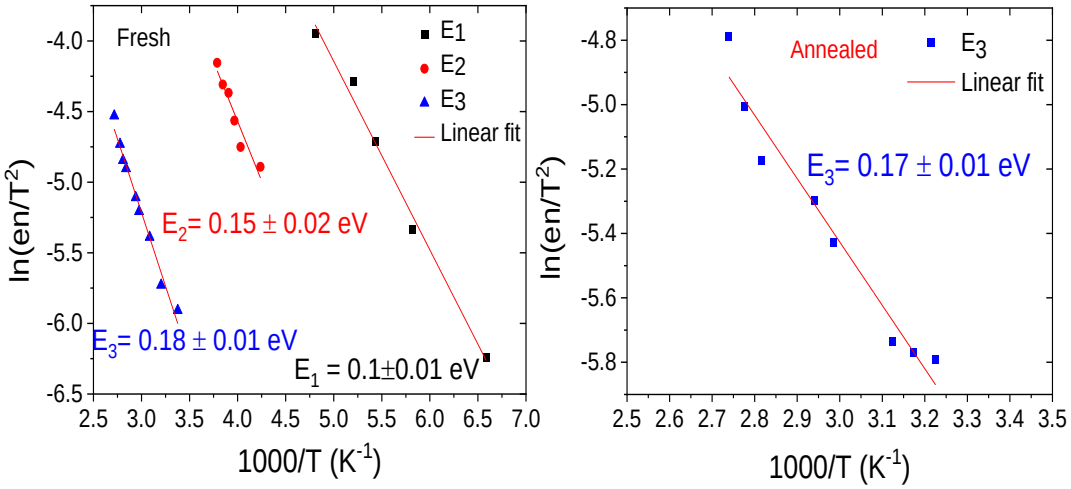

Figure 8.9: Arrhenius plots for fresh and annealed devices obtained from Laplace DLTS at V_R= -2 V.

Table 8.2: Traps parameters for both device at V_R= -2 V, V_P= 0V, and t_P = 1 msec.

sample	Trap	Activation energy (eV)	Trap concentration (cm^{-3})	Capture Cross-Section (cm^2)
Fresh	E_1	0.10 ±0.01	$5.5\pm0.3\times10^{17}$	$4\pm0.2\times10^{-20}$
	E_2	0.15 ±0.02	$9.4\pm0.5\times10^{16}$	$3\pm0.2\times10^{-20}$
	E_3	0.18 ±0.01	$2\pm0.1\times10^{17}$	$9.1\pm0.5\times10^{-21}$
Annealed	E_3	0.17 ±0.01	$4.3\pm0.2\times10^{14}$	$5.2\pm0.3\times10^{-21}$

As shown in Figure 8.9 and Table 8.2, the donor trap E_1 with an activation energy of 0.10 ± 0.01eV and concentration of 5.5×10^{17} cm^{-3} observed in β-Ga_2O_3 is likely to be the same trap detected by Neal et al [26] using temperature dependent Hall-effect measurements up to 1000 K and admittance spectroscopy (AS) technique.

They suggested that the presence of this centre is most likely related to a native defect, such as an antisite or interstitial [26] It is also possible that silicon on octahedrally coordinated Ga(II) of Ga_2O_3 could be responsible for the 110 meV donor [26]. However, this trap was annihilated after the annealing process. The trap E2 with activation energy of 0.15±0.02 eV and trap concentration of 9.4×10^{16} cm^{-3}, was observed in the fresh sample. A similar deep defect was detected in pulsed-laser-deposited epitaxial films of β-Ga_2O_3 using thermally stimulated current [61]. This trap was also detected using AS technique in β-$(Al_{0.14}\ Ga_{0.86})_2O_3/Ga_2O_3$ heterojunctions. It was suggested that E_2 could be due to trapping/detrapping of electrons by Sn donors in the substrate and the energy required to overcome the potential barrier between β-$(Al_{0.14}\ Ga_{0.86})_2O_3$ ternary and the Ga_2O_3 substrate, respectively. [62]. The trap E_3 was detected in both samples (fresh and annealed) with activation energy ranging from 0.16 eV to 0.19 eV. This defect level was detected in both ZCO/Ga_2O_3 and NiO/Ga_2O_3 heterojunctions with activation energies ranging from 0.18 to 0.23 eV using Thermal Admittance Spectroscopy (TAS) [52]. This defect level with similar activation energy was also found in homo-epitaxial β-Ga_2O_3 thin films fabricated by metal organic chemical vapor deposition or by plasma enhanced molecular beam epitaxy [63, 64]. This defect was also observed in Ga_2O_3 films grown by halide vapor phase epitaxy on p-type diamond substrates [65], and in Ge-doped (010) β-Ga_2O_3 layers grown by plasma-assisted molecular beam epitaxy using DLTS technique. It was suggested that this trap may be related to double donor Ge dopants [64]. This may indicate that this defect is common in epitaxial β-Ga_2O_3 thin films [52]. Furthermore, the results demonstrated that the RTA process reduce the concentration of E_3 trap from 2×10^{17} cm^{-3} to 4.3×10^{14} cm^{-3}, while E_1 and E_2 traps were annihilated.

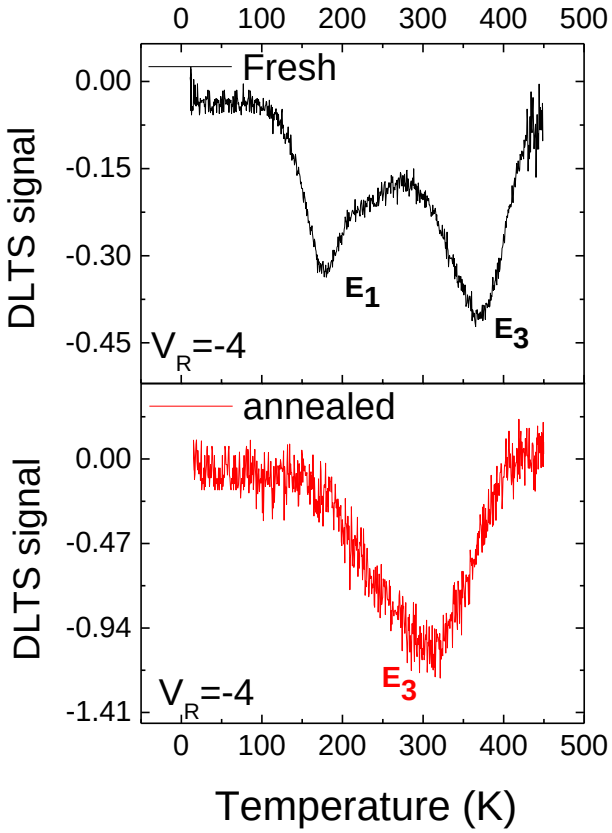

Figure 8.10: DLTS spectra for fresh and annealed devices at (a) V_R = -4 V .

Figure 8.10 shows that the electron traps E_1 and E_3 are also revealed by DLTS at V_R= - 4 V in the fresh sample. Similarly, electron trap E_3 is also detected in the annealed sample.

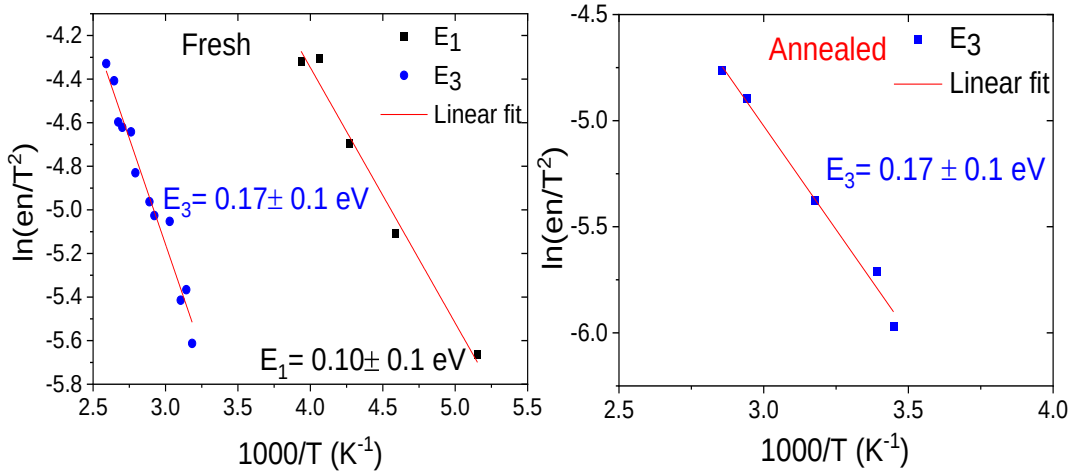

Figure 8.11: Arrhenius plots for fresh and annealed devices obtained from Laplace DLTS at V_R= -4 V.

Table 8.3: Traps parameters for both device at V_R= -4 V, V_P= 0V, and t_P = 1 msec.

sample	Trap	Activation energy (eV)	Trap concentration (cm^{-3})	Capture Cross-Section (cm^2)
Fresh	E_1	0.10 ±0.01	$1.6\pm0.1\times10^{17}$	$6.4\pm0.3\times10^{-21}$
	E_3	0.18 ±0.01	$1.8\pm0.1\times10^{16}$	$4.6\pm0.2\times10^{-22}$
Annealed	E_3	0.17 ±0.01	$3.1\pm0.2\times10^{16}$	$7.5\pm0.4\times10^{-21}$

The Arrhenius plots for both samples obtained from LDLTS measurements are shown in Figure 8.11. Electron traps E_1 and E_3 have lower concentrations as compared to the bias condition of -2V as can be seen in Table 8.3, indicating that both E_1 and E_3 are bulk traps in the Si-doped β-Ga_2O_3 epitaxial layer. This is in contrast to trap E_2 which was observed only at a reverse bias of -2 V while it was absent at -4 V suggesting that it is probably an interface trap. For the annealed sample, the electron trap E_3 is also observed but with higher concentration.

8.6 Modelling

TCAD of SILVACO was used to model the HJD with the aim of correlating trap dynamics to device characteristics. TCAD solves the basic drift-diffusion semiconductor equations, Poisson and continuity equations and include thermionic tunneling above and through the heterojunction, respectively [66-68]. Poisson equation is given by [66-68]:

$$div(\varepsilon\nabla\psi) = -q\left(p - n + N_D^+ - N_A^- \pm N_t^\pm\right) \tag{8.3}$$

where ψ is the electrostatic potential, ε is the permittivity, p and n are free holes and electrons concentrations, respectively, $N_D^+(N_A^-)$ is the ionized donor (acceptor) density and $N_t^\pm$ is the ionized traps density. For NiO and Ga_2O_3, $N_A^- = \frac{N_A}{1+\frac{1}{2}\exp(\frac{E_f - E_a}{KT})}$ and $N_d^+ = \frac{N_d}{1+\frac{1}{2}\exp(\frac{E_{d-E_f}}{KT})}$ the ionization energies of the dopants in each layer are presented in Table 8.5.

The continuity equations for electrons and holes defined in steady states are given by [66-68]:

$$0 = \frac{1}{q} div\overrightarrow{J_n} + G_n - R_n \tag{8.4}$$

$$0 = -\frac{1}{q} div\overrightarrow{J_p} + G_p - R_p \tag{8.5}$$

where G_n and G_p are the generation rates for electrons and holes, R_n and R_p are the recombination rate for electrons and holes. $\vec{J}_n$ and $\vec{J}_p$ are the electron and hole current density which are given in term of quasi-Fermi level (ϕ_n and ϕ_p) and mobility (μ_n and μ_p) as[66-68]:

$$\vec{J}_n = -q\mu_n n\nabla\phi_n \tag{8.6}$$

$$\vec{J}_p = -q\mu_p p\nabla\phi_p \tag{8.7}$$

Traps are represented by their ionized density $N_t^{\pm}$. The sign $\pm$ depends on whether the trap is a majority or a minority carrier so that $N_t^+ = fN_t$ and $N_t^- = (1-f)N_t$, f is the occupancy function given by $f = \frac{\sigma_n n+\sigma_p p}{\sigma_n(n+n_t)+\sigma_p(p+p_t)}$, $\sigma_{n(p)}$ is the trap capture cross-section for electrons (holes). Furthermore, the recombination rate is related to traps through the well-known Shockley-Read-Hall recombination (SRH) formula $R_{n,p} = \frac{pn-n_i^2}{\tau_{0n}(p+p_t)+\tau_{0p}(n+n_t)}$ with $n_t = n_i exp(-(E_i - E_t)/kT)$ and $p_t = n_i exp(-(E_t - E_i)/kT)$, τ_{0n} and τ_{0p} are the minority carrier lifetime which are also related to traps through $\tau_{0n(p)} = \frac{1}{v_{thn(p)}\sigma_{n(p)}N_t}$ where $v_{thn(p)}$ is the thermal velocity of electrons (holes).

In addition, thermionic emission (equation 8.1 and 8.2) and tunneling currents are taken into account since they might be present in heterojunctions. The tunnelling current is given by [69]:

$$J_T = J_T\ \frac{A^*T_L}{K_B}\int_{\epsilon}^{\infty}\Gamma(E')\ln(\frac{1+F_s(E')}{1+F_m(E')})dE' \tag{8.8}$$

where $A^*, T_L, K_B,\ \epsilon,\ F_s(E')$ and $F_m(E')$ are effective Richardson's coefficient (41.11 $Acm^{-2}K^{-2}$), lattice temperature, Boltzmann constant, electrons energy, and Maxwell- Boltzmann distribution in the semiconductor and metal, respectively, and $\Gamma(E')$ is the tunnelling probability given by [69]:

$$\Gamma(\epsilon) = \exp\left[-2\frac{\sqrt{2m^*}}{\hbar}\int_{x_1}^{x_2}\sqrt{E_c(x)-\epsilon}\,dx\right] \tag{8.9}$$

Here, $E_c(x)$ and (x_1, x_2) are the potential energy distribution of Schottky barrier diode and classical turning points, respectively. Furthermore, mobilities which are dependent on concentration and temperature are considered using an analytic model for each layer, which is given by [70]:

$$\mu_n(T, N_d) = \mu_{minn}\left(\frac{T}{300}\right)^{n1} + \frac{\mu_{maxn}\left(\frac{T}{300}\right)^{m1} - \mu_{minn}\left(\frac{T}{300}\right)^{n1}}{1+\left(\frac{T}{300}\right)^{\alpha 1}\left(\frac{Nd}{N_{d0}}\right)^{\gamma 1}} \tag{8.10}$$

$$\mu_p(T, N_a) = \mu_{minp}\left(\frac{T}{300}\right)^{n2} + \frac{\mu_{maxp}\left(\frac{T}{300}\right)^{m2} - \mu_{minp}\left(\frac{T}{300}\right)^{n2}}{1+\left(\frac{T}{300}\right)^{\alpha 2}\left(\frac{Na}{N_{a0}}\right)^{\gamma 2}} \tag{8.11}$$

where μ_{minn}, μ_{minp}, μ_{maxn}, μ_{maxp}, $n1$, $m1$, $\alpha 1$, $\gamma 1$, N_{d0}, $n2$, $m2$, $\alpha 2$, N_{a0} and $\gamma 2$ are fitting parameters presented in Table 8.4 for majority carriers at each layer. Figure 8.12 shows the used NiO hole mobility dependent acceptor density. In addition to SRH, Auger recombination and mobility dependent electric field are considered in this simulation.

Table 8.4: Fitting parameter for mobility dependant concentration and temperature model (Analytic model)

Parameters	**Sn:β-Ga_2O_3**	**Si:β-Ga_2O_3**	**NiO**
$\boldsymbol{\mu_{minn}}$	55.24± 2.70	55.24± 2.70	-
$\boldsymbol{\mu_{maxn}}$	172±0. 9	300± 15	-
$\boldsymbol{\mu_{minp}}$	-	-	0.181
$\boldsymbol{\mu_{maxp}}$	-	-	6.73± 0.30
$\boldsymbol{n1}$	1	1	-
$m1$	1	1	-
$\boldsymbol{\alpha 1}$	1	1	-
$\boldsymbol{\gamma 1}$	1/2	1/2	-
$\boldsymbol{n_0}$	5.0 ± 0.3×10^{18} cm^{-3}	3.0 ± 0.2×10^{16} cm^{-3}	-
$\boldsymbol{n2}$	-	-	1
$m2$	-	-	1
$\boldsymbol{\alpha 2}$	-	-	1
$\boldsymbol{\gamma 2}$	-	-	1/2
$\boldsymbol{p_0}$	-	-	1.0± 0.1×10^{15}

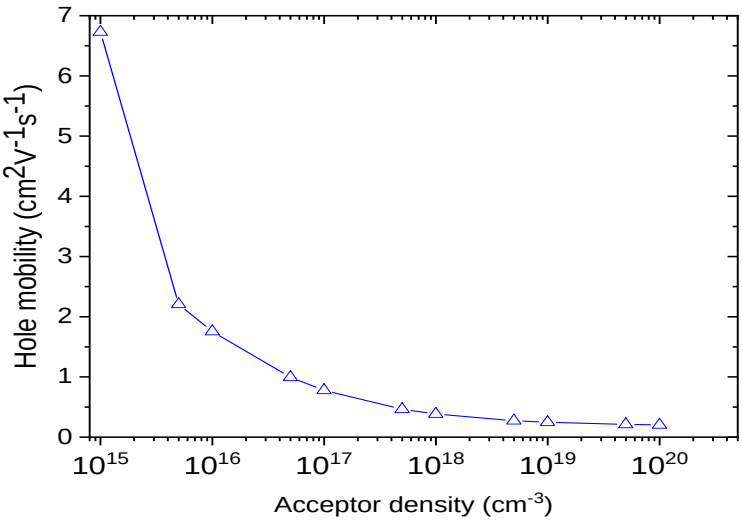

Figure 8.12: The simulation of NiO hole mobility dependent acceptor density is based on experimental results reported in the literature.

8.7 Modelling NiO/ β -Ga_2O_3 Heterojunction

In this section, fresh and annealed NiO/β-Ga_2O_3 heterojunction characteristics were modelled in order to understand conduction mechanisms as well as deep levels effects. The starting modeling parameters of each layer of the heterojunction are shown in Table 8.5**.** The difference between fresh and annealed samples is in their deep levels content.

Table 8.5: Properties of each layer of the studied NiO/β-Ga2O3 HJD.

Parameters	**Sn:β-Ga_2O_3 [63, 66, 71]**	**Si:β-Ga_2O_3 [26, 66, 71]**	**NiO [72-74]**
Thickness (µm)	600	10	0.1
Bandgap (eV)	4.8	4.8	3.71
Affinity (eV)	4	4	1.46
Hole mobility ($cm^2V^{-1}s^{-1}$)	10	10	1
Electron mobility ($cm^2V^{-1}s^{-1}$)	172	300	12
Doping density (N_a and N_d) (cm^{-3})	1×10^{18} (n-type)	1.4×10^{16}-2×10^{17} (n-type)	5×10^{15}-1×10^{19} (p-type)
Ionization energy (eV)	E_c-0.21	E_c-0.11	E_v+0.26
Relative permittivity	12.6	11	10.7
N_c (cm^{-3})	3.7×10^{18}	3.7×10^{18}	2.8×10^{19}
N_v (cm^{-3})	5×10^{18}	5×10^{18}	1×10^{19}
Minority carrier lifetime (ns)	0.21	0.21	260

8.7.1 Fresh NiO/β-Ga_2O_3 Heterojunction (FHJ)

In FHJ, the electron traps E_1 and E_3 are revealed by DLTS at -2V and -4V, which indicates that both E_1 and E_3 are bulk traps which are considered in epitaxial layer (Si-doped β-Ga_2O_3) in contrast to E_2, which was seen at -2 V while it was absent at -4 V indicating that it is probably an interface trap. The depletion region width for

the -2 V and -4 V reverse biases is roughly estimated to be 0.204 µm and 0.232 µm, respectively, for the effective doping density of 2×10^{17} cm^3 estimated from C-V characteristics. The 0.204 µm and 0.232 µm depletion region widths are initially considered the location limits of the interface and bulk traps, respectively. The N_A value in the p-type NiO is first assumed to be 8×10^{16} cm^{-3}.

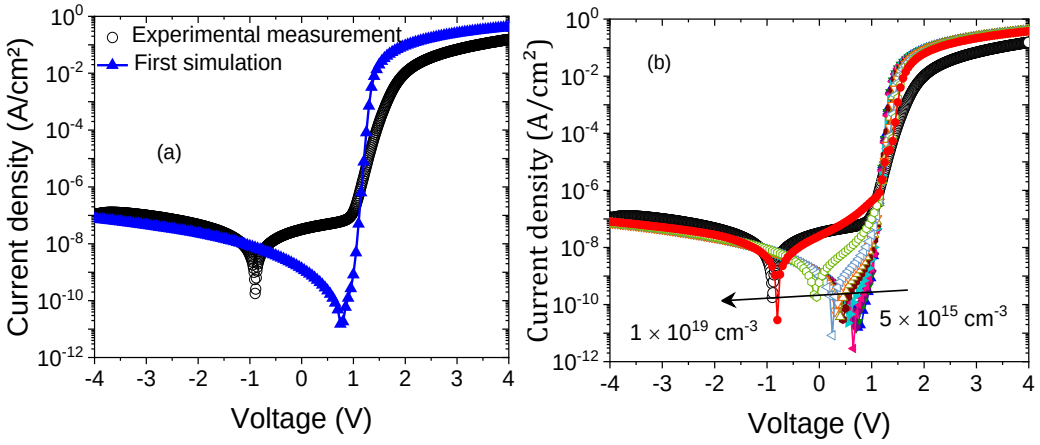

Figure 8.13: The simulated FHJ J-V characteristics for: (a) homogeneous NiO density (8×10^{16} cm^{-3}) and (b) variable NiO surface acceptor density.

The simulated J-V characteristics compared to measurements are presented in Figure 8.13 (a). The disagreement between simulation and measurement, especially the voltage position of the J-V curve at J=0, may be related to several reasons. The first possible reason could be due to the inhomogeneity of NiO acceptor density. For example, Lee el al. [75] have extracted Ni and oxygen profiles using energy dispersive X-ray spectroscopy (EDS) and they found that Ni and oxygen have inhomogeneity profiles, which will affect the acceptor density profile. Therefore, the effect of NiO surface acceptor density should be taken into account. In this work, the value of acceptor density in NiO was varied from 5×10^{15} cm^{-3} to 1×10^{19}

cm^{-3} and the obtained J-V characteristics, compared with measurements, are presented in Figure 8.13 (b).

The point where the current - voltage curve is most impacted is at J=0, i.e. where J changes sign. As the NiO surface acceptor density increases the peaks of the simulated and the measured currents get closer. This behaviour is related to the increase in the band-to-band tunneling current [76]. A good agreement is achieved for a surface acceptor density of 1×10^{19} cm^{-3}.

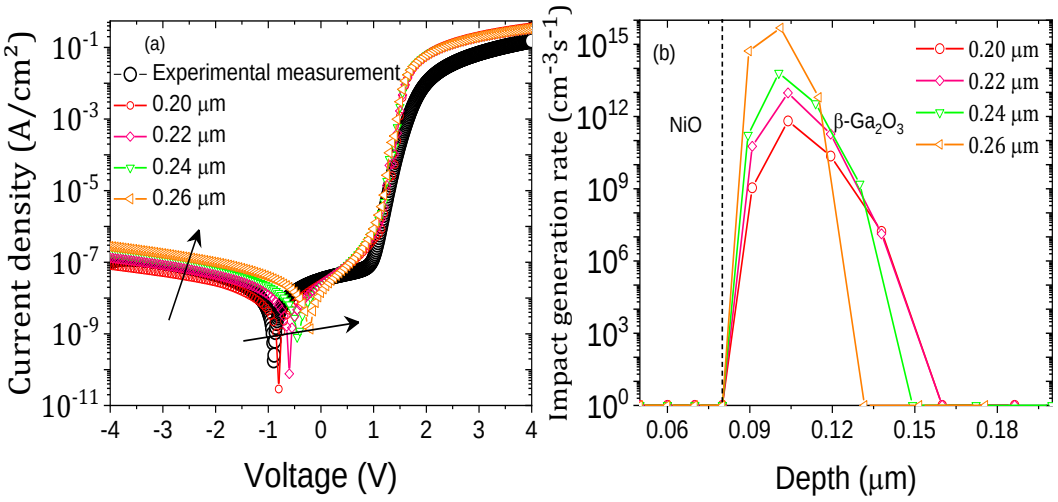

Figure 8.14: Effect of the E_2 trap location depth on (a) the simulated J-V characteristics and with acceptor density (1×10^{19} cm^{-3}) (b) impact generation rate at equilibrium.

The second plausible explanation is the E_2 trap location depth. Initially this interface trap is assumed to be located in the region between the interface and 0.204 µm (the depletion region limit corresponding to -2 V). This trap location may well be beyond this position. This probable limit is varied between 0.20 µm and 0.26 µm and the corresponding J-V characteristics are presented in Figure 8.14 (a). With increasing trap depth, the leakage current increased. This may be related to the increase in NiO/β-Ga_2O_3 interface generation of free carriers from this trap level as

shown in Figure 8.14 (b). A good agreement at reverse voltage was obtained for a depth of about 0.220 µm which is less than 0.234 µm (corresponding to -4V). This may well be the reason that the E_2 trap was absent in DLTS at -4 V. The series resistance region is not affected by the E_2 trap location depth. Therefore, a further investigation is required. The E_2^* trap (E_c-0.75) is one of the most observed traps in β-Ga_2O_3 [30, 77, 78] at a density of 10^{13}-10^{14} cm^{-3}. This trap is not observed in this study perhaps because of the fact that it is usually observed in bulk β-Ga_2O_3 and affects the forward current [30]. Therefore, this trap is considered in Sn-doped β-Ga_2O_3 substrate with density $4.1\times10^{13}cm^{-3}$ [30] and the modelling-measurement difference is reduced as presented in Figure 8.15.

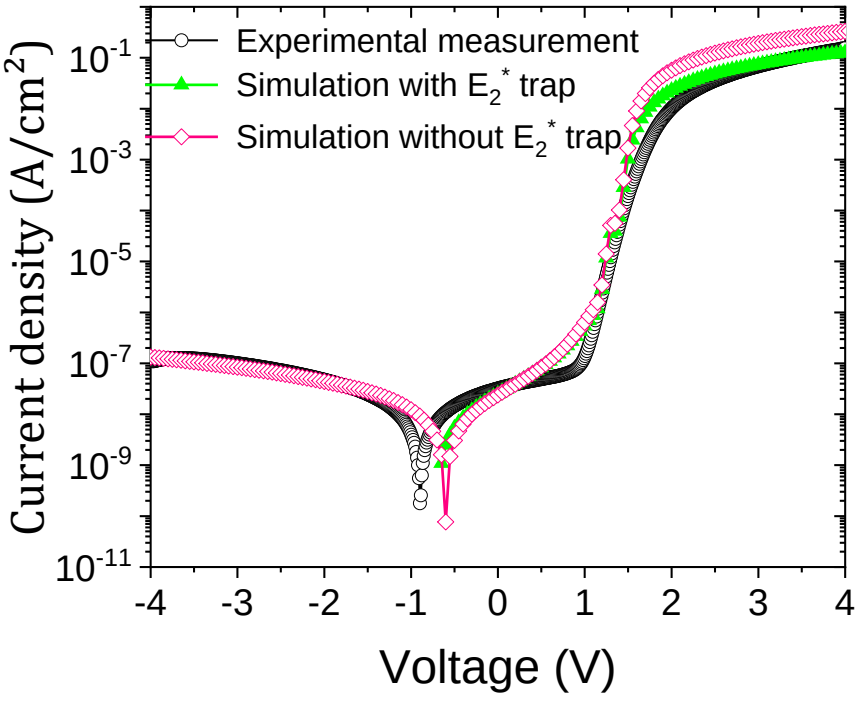

Figure 8.15: Effect of Ec-0.75 eV trap on J-V characteristics.

Now, after obtaining a fairly good agreement, the equilibrium band diagram, free carriers' profiles, electric field and potential profiles are extracted and are shown in Figure 8.16.

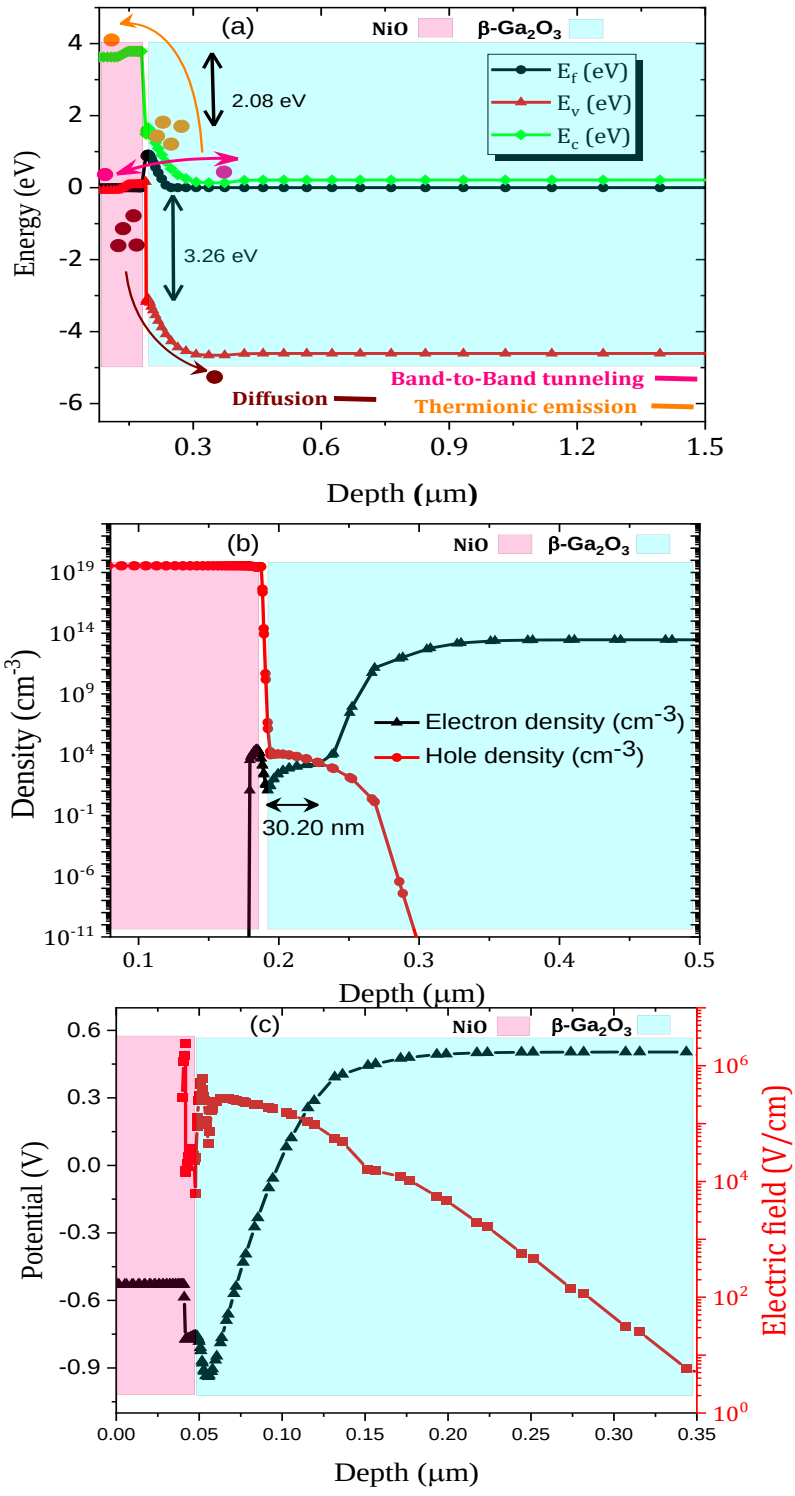

Figure 8.16: Equilibrium (0 V) band diagram and transport mechanisms (a), free carriers' profile (b), and potential and electric field profile (c).

A type-II NiO/β-Ga_2O_3 heterojunction as shown in Figure 8.16 was obtained which is in agreement with [24, 30]. In this work, three transport mechanisms are present: thermionic emission, diffusion and band-to-band tunneling as detailed in Figure 8.16

(a). Free holes diffuse from NiO to the surface of β-Ga_2O_3 with a diffusion length of about ~ 30 nm as shown in Figure 8.16 (b). Then, because of high NiO hole density, band-to-band tunneling plays an important role while the thermionic emission mechanism finds a suitable barrier to overcome. From the free carrier profile, the equilibrium depletion spreads mainly in β-Ga_2O_3 because of high NiO surface acceptor density and its width is ~ 0.182 μm which is obtained from the equilibrium potential profile (Figure 8.16 (c)). Furthermore, the built-in potential value (V_{bi}) extracted from the equilibrium potential profile is about 1.30 V, which is different from the turn-on voltage (V_{on}) of about 1.40 V for fresh HJ sample extracted from the simulated J-V characteristics shown in Figure 8.15. This small deviation of 0.1 V between the two values may be related to the effect of the considered interfacial traps. A high equilibrium electric field with unusual profile at the NiO/β-Ga_2O_3 interface may be due to hole diffusion and the considered surface Figure 8.16 (c)).

8.7.2 Annealed NiO/β-Ga_2O_3 Heterojunction (AHJ)

When the sample was annealed, only one trap was revealed by DLTS, namely E_3. The activation energy of this trap is E_c-0.17 eV and its density is 4.3×10^{14} cm^{-3} at -2 V but increased to 3.1×10^{16} cm^{-3} at -4 V. This indicates that this trap has a non-uniform distribution profile. Therefore, the AHJ was modelled using the same

established parameters for the FHJ except for the traps, NiO acceptor density, and the donor density in the Si-doped β-Ga_2O_3. Consequently, a simple presentation of the trap profile was proposed. This profile consists of two regions with different densities. The first starts from the interface and has a depth equal to the depletion region limit at -2V (0.685 μm for the AHJ) with a density of 3.1×10^{14} cm^{-3}. The second started from 0.685 μm to the rest of the active region (Si-doped β-Ga_2O_3) of the sample with a density of 3.1×10^{16} cm^{-3}. Furthermore, it was found that after annealing the sheet resistance increased from 3.99×10^7 Ω/cm^2 to 1.47×10^8 Ω/cm^2, indicating that the free hole density decreased after annealing. The extracted hole density from sheet resistance with the consideration of the proposed hole mobility model was about 2.35×10^{15} cm^{-3} (N_A= 6×10^{16} cm^{-3} because the free hole density is just 4.7 % of N_A). The N_A value is very close to the measured value of 6×10^{16} cm^{-3}. This decrease of hole density may be related to the decrease in oxygen vacancy in NiO layer. In addition, the donor density of the considered Si-doped β-Ga_2O_3 layer is 1.4×10^{16} cm^{-3}. The simulated J-V curves show good agreement with the experimental results as illustrated in Figure 8.17.

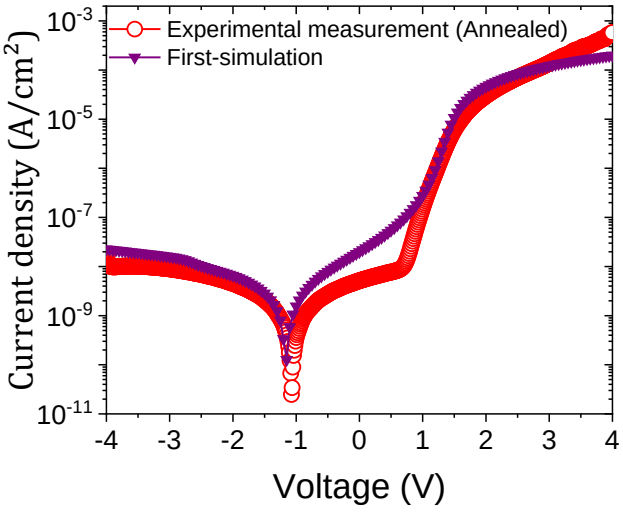

Figure 8.17: The simulated J-V characteristics compared to measurement for AHJ.

8.8 Conclusion

The effects of RTA on the electrical and optical properties of NiO/β-Ga_2O_3 heterojunction diodes have been investigated using Capacitance-Voltage, Current-Voltage, DLTS, Laplace DLTS, Photoluminescence, micro-Raman spectroscopy techniques, and SILVACO-TCAD numerical simulator. The heterojunction diode was designed to make NiO layer fully depleted at zero bias, thus allowing for the study of the properties of β-Ga_2O_3 and its interface with NiO. It was found that the annealed samples showed better diode performance. This was in agreement with the optical results which demonstrated an enhancement in the photoluminescence peak intensity after RTA. This enhancement is explained by a rise in the density of gallium and oxygen vacancies. In addition, the RTA resulted in an improvement of the electrical characteristics of the devices and a reduction of the number of electrically active traps. SILVACO TCAD was used to model different effects. Values of the E_2 trap depth from the β-Ga_2O_3 surface and the NiO surface hole density were determined, enabling a good agreement with experimental results for fresh and annealed samples. Furthermore, because of the high NiO surface hole density, it was demonstrated that band-to-band tunneling transport mechanism is dominant. Applying the RTA process on NiO/β-Ga_2O_3 heterojunction diodes resulted in superior optical and electrical properties than those of the fresh samples, which are required for potential applications in next generation power devices. The demonstrated NiO/β-Ga_2O_3 heterojunction can open up a route towards future bipolar devices such as heterojunction gate field-effect-transistors (HJ-FETs).

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CHAPTER 9: CONCLUSION AND FUTURE WORK

The purpose of this chapter is to summarize the results of the research carried out on the electrically active defects that are present in

1. $Al_{0.6}Ga_{0.4}N/Al_{0.5}Ga_{0.5}N$ multi quantum wells (MQWs) based deep ultraviolet light-emitting diodes (DUV LEDs),
2. $In_{0.09}Ga_{0.91}N$/GaN MQWs based ultraviolet Photodetector (UV PD)
3. p-NiO/n-β-Ga_2O_3 heterojunction diodes

using electrical (I-V, C-V, DLTS, Laplace DLTS), optical (CL, EL, PL), structural (TEM) and photovoltaic (PCS) characterization techniques. Future work suggestions are also covered in this chapter.

9.1 Conclusion

9.1.1 $Al_{0.6}Ga_{0.4}N/Al_{0.5}Ga_{0.5}N$ MQWs based DUV LEDs

In this study, point defects and dislocations were investigated systematically by comparing the properties of $Al_{1-x}Ga_xN/Al_{1-y}Ga_yN$ MQWs based DUV LEDs before and after degradation caused by electric current stress using several different analytical techniques, including CL, DLTS and TEM. The results show that the electrical current stress induced point defects are located within the MQWs region, especially in the first quantum well near the p-side of the LEDs devices. The increased point defects density during the stress caused a carrier redistribution process. At a small reverse bias V_R= - 0.5 V, DLTS measurements showed two electron traps in the fresh LEDs (i.e. not subjected to the electric current stress), and one electron trap and a small unresolved signal due to a hole trap in the stressed

LEDs. The very small hole trap signal at V_R= - 0.5 V which was not resolved by Laplace DLTS became more pronounced at V_R= - 4 V, and at this bias condition Laplace DLTS revealed the same number of electron traps and hole traps in both fresh and stressed LEDs. Moreover, TEM and EDX mapping provided some evidence of Mg diffusion along the dislocation line leading to Mg-related traps. By investigating the defects of the fresh and the stressed DUV LEDs epitaxial structures, the failure mechanisms for the stressed samples involving point defects and dislocations have been identified.

Comparison of these observed results with those of others concerning the degradation of AlGaN-based DUV LEDs confirms that new defects are generated within or around the active region as a result of electrical current stress process[1, 2]. Moreover, P Dalapati et al. [3] reported a similar carrier redistribution process in GaN-based LEDs, linking this phenomenon to stress-induced defects. Similar observations support the DLTS findings confirming that generated defects due to electrical stress lead to degradation of LEDs [1]. Furthermore, the observation of dislocations that occur after electrical current stress as evidenced by TEM and EDX mapping is in accordance with previous observations that have shown that dislocations penetrate deeper in the multiple quantum wells (MQWs) active region of UV-C LEDs [4]. This study, which aligns with these existing insights, strengthens the credibility of the findings reported in this thesis.

9.1.2 $In_{0.09}Ga_{0.91}N$/GaN MQWs UV-photodetectors

InGaN/GaN MQWs UV-photodetectors (PDs) were studied systematically to determine the root mechanisms that could account for the degradation of the devices' performances due to electrical current stress by employing several

combined optical and electrical measurements. The obtained EL spectra suggest that the EL intensity decreases by about 48 % in the stressed PDs due to 200 mA of current stress over 340 h. This degradation is due to more charge carriers in the active region being captured by newly created defects. From photovoltaic measurements, it was found that V_{OC} is reduced much more than I_{SC} in the stressed PDs, indicating that V_{OC} is the leading degradation mechanism. The dark I-V measurements showed that in the stressed PDs, the reverse and forward leakage currents increase significantly. This suggests that the parasitic leakage routes, which are usually prompted by severe point defects within or around the MQWs, are activated largely after electric current stress. Furthermore, the temperature dependence of I-V characteristics of the stressed PDs showed that the values of ideality factor (Junction potential) are always higher (lower) than those of the fresh devices, indicating the presence of generation-recombination centers caused by the created defects during the stress. It is important to note that the source of leakage currents in stressed PDs could be due to two major trap levels with different activation energies which were detected by Laplace DLTS. The degradation mechanisms in the stressed PDs, however, are strongly associated with the activation of initially inactive defects, mainly Mg-related shallow acceptors, such as Mg_{Ga} and Mg-H_2. According to Laplace DLTS analysis, the devices's performances are significantly worsened by activation of acceptor levels in stressed PDs. In addition, the sensitization performance of stressed PDs significantly decreases as a result of stress treatment, suggesting that the generated defects in the device can ruin their photodetection performance.

In comparing the observed results with previous studies on the degradation of InGaN-based UV PDs, these results confirm that electrical current stress generates new defects in the active region. A similar observation has been reported in MQWs-UV PDs, confirming that the reduction of EL intensity is due to the generation of new defects after electrical stress [5]. This EL intensity reduction was also observed in InGaN light-emitting diodes during the electrical stressing process [6]. Furthermore, Dalapati et al. [5] reported the same reduction in short-circuit current (I_{SC}) and open-circuit voltage (V_{OC}) of InGaN/GaN UV PDs. The significant increase in reverse and forward leakage currents found after the electrical stress procedure aligns with the findings reported in InGaN based on UV. Furthermore, DLTS findings confirm that electrical stress generates acceptor traps that lead to the degradation of PDs. In addition, there is strong correlation between these acceptor defects and the degradation of GaN-based devices under similar stress conditions [7]. The present study provided insights into the underlying mechanisms governing the degradation of InGaN/GaN MQWs UV-photodetectors under electrical current stress as well as established parallels with the existing literature. The comprehensive evidence gathered has led to a more profound understanding of PDs degradation processes.

9.1.3 p-NiO/ n-β-Ga_2O_3 heterojunction diodes

The effect of rapid thermal annealing (RTA) on the electrical and optical properties of p-NiO/n-β-Ga_2O_3 heterojunction diodes have been investigated using I-V, C-V, DLTS, Laplace DLTS, photoluminescence, micro-Raman spectroscopy techniques, and SILVACO-TCAD numerical simulator. The heterojunction diode structure was designed to make NiO fully depleted at zero bias, thus allowing for

study of the properties of n-β-Ga_2O_3 and its interface with NiO. Analyses showed that the performance of the diodes was better for the annealed samples. The optical results evidenced an enhancement in the β-Ga_2O_3 photoluminescence peak intensity after RTA process. This improvement is explained by an increase in the density of gallium and oxygen vacancies. Additionally, RTA improved the electrical characteristics of the devices and reduced the number of electrically active traps. SILVACO-TCAD numerical simulator was used to model different effects. The results obtained for the annealed samples were well in agreement with experimental results using the same values for both hole density and activation energy of trap E_3 (0.17 eV) that were obtained experimentally. However, for fresh samples, the agreement was obtained only by using the activation energy of the E_2 trap (0.15 eV) and a higher hole density (1×10^{19} cm^{-3}) than the experimentally determined value (8×10^{16} cm^{-3}) . Moreover, the high density of NiO surface holes demonstrates that tunneling transport mechanisms dominate. Applying RTA treatment on p-NiO/ n-β-Ga_2O_3 heterojunction diodes resulted in superior optical and electrical properties than those of the fresh samples, which are required for potential applications in next generation power devices.

These findings are consistent with those reported previously in studies conducted on similar semiconductor systems. For example, the observed increase in gallium and oxygen vacancy densities, resulting in an increase in PL intensity, is in agreement with those observed by Ohira et al. [8], where similar enhancements were attributed to vacancy-related processes. Similar results were reported in NiO/Ga_2O_3 heterostructures, demonstrating that the RTA process improves the electrical characteristics [9]. This is also supported by DLTS results, where the

RTA process was found to reduce the number and concentration of electrically active traps. DLTS findings also confirmed the presence of electron trap E3 with an activation ranging from 0.18 to 0.23 eV that was observed previously before and after RTA treatment [10].

9.2 Future Work Suggestions

As these material systems are comparatively new, it is very important to acquire further knowledge and deeper understanding about the effects that affect their remarkable electronic and optical properties in order to develop advanced devices. In addition, to significantly increase the performance of the devices investigated in this thesis, it is essential to understand and optimise the growth fabrication and processing processes in order to minimise the defects that affect their properties. According to the experimental results obtained in this thesis work, suggestions for further investigations are proposed in the following:

(i) In order to understand further the effects of electric current stress process on the properties of $Al_{1-x}Ga_xN/Al_{1-y}Ga_yN$ MQWs DUV LEDs, it is important to study different stress conditions, such as electric current levels and duration of stress. Thus, this will help determine the levels of electrical current and exposure times that cause minimal degradation of the LEDs. This information can then be used to optimize the design and operation of the LEDs in order to increase their lifetimes.

(ii) The number of quantum wells (QWs) in the active region of semiconductor devices is very important. It is well known that if this number is too large then the crystal quality degrades, the hole mobility as compared to electrons is reduced, and the potential barrier for the

transport of holes into the QWs from the electron blocking layer (EBL) becomes high. Therefore, it is proposed to investigate the effects of the number of QWs in the active region on the electrical, optical and structural properties of p-i-n InGaN/GaN MQWs UV PDs. The aim is to determine the optimum number of QWs for the enhancement of the LEDs performance.

(iii) Heat and hydrogenation treatment processes are well known to reduce the concentration of defects, annihilate and passivate completely defects. Therefore, it is proposed to investigate the effect of thermal annealing and hydrogen irradiation on the electrical, optical and structural properties of p-NiO/n-β-Ga_2O_3 heterojunction diodes with the aim to determine the optimum treatment conditions for the enhancement of their properties. For the heat treatment process two techniques could be explored, namely furnace annealing and RTA, using different temperatures and annealing time. For the hydrogenation process one could consider using different energies and doses of the ions.

(iv) Gamma radiation is a type of electromagnetic radiation that is highly energetic and can penetrate through materials. Due to its ability to modify the optical and electrical properties of semiconductor materials, it has become an important tool in the development of dosimeters and radiation detectors. However, in order to improve these devices, it is crucial to understand the effects of gamma radiation on different materials. This is particularly important for space applications, where the radiation environment can cause defects in semiconductors that may

degrade their performance and lifetime. By conducting systematic studies with different doses of gamma radiation, one can gain a better understanding of its effects on electrically active defects in wide bandgap materials. Such investigations are essential for assessing the suitability of wide bandgap semiconductors for use in satellite communications and other space applications.

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