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Hybrid Modular Multilevel Converter (MMC) applications under over-modulation

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To Isabel, who always encouraged me to pursue my dreams. To Mary and Pablo whose memories are always with me.

Abstract

The Modular Multilevel Converter (MMC) has become a prominent converter topology due to its several advantages: high modularity, high scalability, low harmonic distortion, and high efficiency. In particular, due to its modular structure, it is possible to increase its voltage rating by stacking extra cells. The MMC has been successfully applied to high voltage direct current (HVDC) transmission systems and drive applications.

Most MMC-based projects use the half-bridge sub-module (HBSM) as a building block to reduce semiconductor losses. Despite the MMC advantages, there are still open challenges regarding its control and operation. For instance, in the HBSM-based MMC, the minimum dc-port voltage cannot be lower than two times the AC output voltage. The over-modulation operation of the MMC, i.e. operation with reduced dc-link voltage, has shown some benefits. For instance, the MMC can operate with a reduced dc-port voltage in HVDC applications to avoid flashovers under extreme atmospheric conditions. In addition, for back-to-back MMC-based drive applications, it is possible to reduce the energy arm oscillations by controlling the dc-port voltage.

The operation with a reduced dc-port voltage can be accomplished by using full-bridge sub-modules (FBSM) instead of the HBSMs. However, this solution has higher semiconductor losses. A possible alternative is to use a hybrid MMC. In this case, each arm is composed of HBSMs and FBSMs. However, in the hybrid MMC, the capacitor voltages of the HBSMs and FBSMs may drift apart if the converter operates with reduced dc-port voltage because the arm current becomes unipolar, i.e. the arm currents do not have zero-crossing angles.

This thesis presents two control strategies to ensure the cell capacitor voltage balance of the hybrid MMC operating in over-modulation. A decoupled control is developed and shown to regulate the inner and outer converter variables independently. An optimisation problem is proposed to ensure the local balance between HBSMs and FBSMs. In addition, a closed-loop controller is considered to correct any mismatch between the control and actual system parameters. The proposed controller is validated through simulation and experimental results. In particular, a 5 kW hybrid MMC of 18 cells has been built to validate the proposed strategies.

Finally, this thesis presents the control systems and experimental evaluation of a hybrid back-to-back (BTB) modular multilevel converter (MMC) for drive applications. The grid-side converter is a hybrid MMC composed of half-bridge sub-modules (HBSMs) and full-bridge sub-modules (FBSMs), while the drive-side converter is an HBSM-based MMC. The proposed topology can operate with a variable dc-port voltage. By controlling the dc-port voltage as a function of the machine operational point, it is possible to reduce the high sub-module capacitor voltage oscillations in the machine-side MMC during low machine speed. An experimental rig composed of 36 cells was built and tested to validate the proposed control.

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II. Conference Papers

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8.23 Zoomed view during high-frequency operation for variable dc-link voltage. Upper arm current i_{2a}^{U} (green), lower arm current i_{2a}^{U} (yellow), circulating current i_{2a}^{Σ} (pink), sub-module capacitor voltage v_{C2a1}^{U} (blue), and machine phase current i_{2a} (red). 186

8.24 Machine-side operation with constant dc-link voltage E. (a) Machine speed, (b) dc-link voltage E, (c) sub-module capacitor voltages, (d) machine currents i_{2abc}, (e) circulating currents $\boldsymbol{i}_{2\alpha\beta}^{\Sigma}$, and (f) common-mode voltage applied to the machine. 187

8.25 Machine-side operation with variable dc-link voltage E. (a) Machine speed, (b) dc-link voltage E, (c) sub-module capacitor voltages, (d) machine currents i_{2abc}, (e) circulating currents $\boldsymbol{i}_{2\alpha\beta}^{\Sigma}$, and (f) common-mode voltage applied to the machine. 188

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Chapter 1

List of Abbreviations

M^2C	Modular Multilevel Converter
M^3C	Modular Multilevel Matrix Converter
PCC	Point of Common Coupling
HVDC	High-Voltage Direct Current
VSC	Voltage Source Converter
NPC	Neutral-Point Clamped
ANPC	Active Neutral-Point Clamped
CHB	Cascaded H-Bridge
FC	Flying Capacitor
PI	Proportional-Integral
RC	Resonant Control
LPF	Low-Pass Filter
NF	Notch Filter
PLL	Phase Locked Loop
SM	Sub-Module
HBSM	Half-bridge Sub-Module
FBSM	Full-bridge Sub-Module

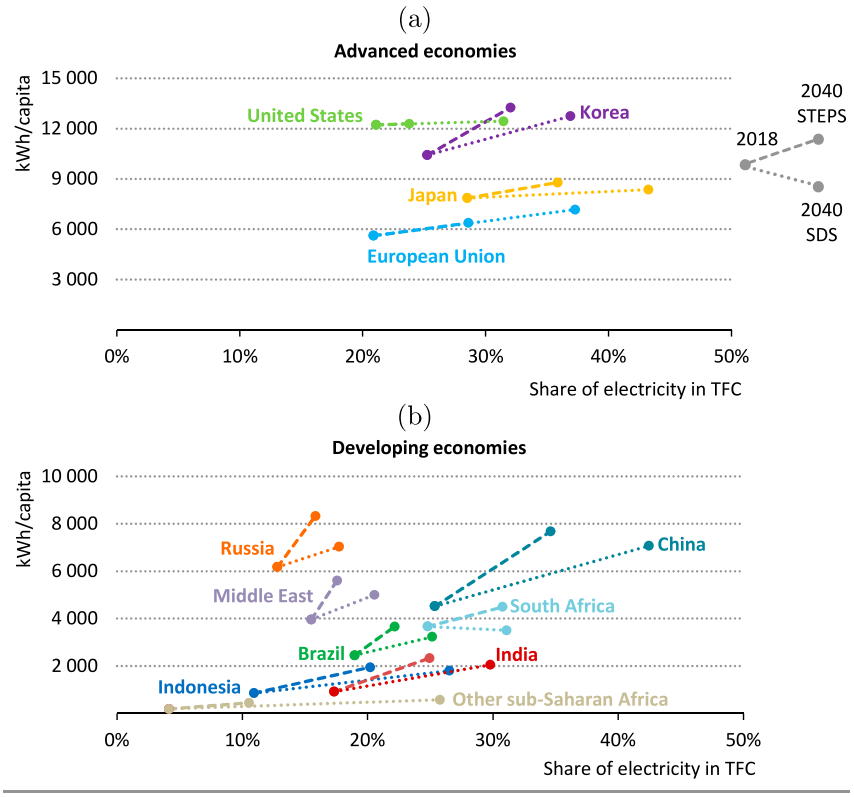
LV	Low Voltage
MV	Medium Voltage
HV	High Voltage
SHE	Selective Harmonic Elimination
NLM	Nearest Level Modulation
SVM	Space Vector Modulation
PWM	Pulse Width Modulation
PD	Phase Disposition
POD	Phase Opposite Disposition
APOD	Alternate Phase Opposite Disposition
EMI	Electromagnetic Interference
ESR	Equivalent Series Resistance
DSP	Digital Signal Processor
FPGA	Field-Programmable Gate Array
PCB	Printed Circuit Board

Chapter 2

Introduction

Over the last century, the technical development of electrical networks has been a significant boost to the quality of human life. As a consequence, electrical energy consumption has grown steadily to meet the demands of modern humanity. Electricity is at the heart of modern economies, powering communications, healthcare, industry, education, comfort and entertainment [10]. Furthermore, the application of power electronic converter to interface different electrical energy sources and loads has improved their performance and usability [11–13]. The per-capita electricity demand is depicted in figure 2.1 (a) and (b) for developed and developing economies [1] respectively. In this case, the per-capita consumption is shown for the years 2018 and 2040. To forecast the future consumption, two scenarios are considered: Stated Policies Scenario (STEPS) and Sustainable Development Scenario (SDS). The former predict the future demand assuming the current energy policies while the latter assume certain future outcomes, such as a better efficiency on industrial process, and then the equivalent per-capita consumption is calculated [1]. From fig. 2.1, it is clear that most countries are expected to increase their electricity consumption in the coming years.

The two largest electricity consumption sectors are buildings (space and water heating, cooling, lighting, among others) and industry with a consumption of 11800 TWh and 9300 TWh respectively [1]. Most of the industrial consump-



Notes: TFC = total final consumption; kWh = kilowatt-hour; STEPS = Stated Policies Scenario; SDS = Sustainable Development Scenario. Other sub-Saharan Africa excludes South Africa.

Figure 2.1: *Per-capita electricity demand in advanced and developing economies according to* World Energy Outlook 2019 *[1]*

tion is due to electric motors (pump, fans, compressors, conveyor belts, among others). In 2018, 30% of the global demand in electrical energy was for electric motors [1], this percentage is equivalent to 6930 TWh. These machines operate in the medium-voltage range to ensure a high efficiency is maintained. Currently, medium-voltage drives have a voltage rating between 2.3 and 13.8 kV and a nominal power from 0.2 to 40 MW [2]. The drives application market has grown continuously during recent years. It is forecast that the total electrical demand will increase up to 36453 TWh by 2040, where 11418 TWh is due to electrical machines [1]. There are several industries that require the use of high-power and medium voltage electrical machines within their process. For instance, oil and gas, petrochemical, mining, pulp/paper, cement, chemical, metal production, traction, and marine drive sectors [14].

In the last decade, the performance of voltage source converters has increased in several applications, in particular, in HVDC (High-voltage direct current)

applications [15] and drive converters [3]. Although, current-source converters are a mature technology, these solutions employ thyristors devices, the main drawbacks of these components are their slow switching speed and their inability to gate off the power switches [16]. In addition, there has been a considerable development in the field of power electronics. In particular, several multilevel and scalable converters has been proposed [17–19].

In 2003, the modular multilevel converter (MMC) was introduced by Prof. Marquardt [20]. These converters allow the distribution of voltage stress across lower voltage cells, thus eliminating the need for series connection of switching devices. The main advantages of the MMC are its low harmonic distortion, easy scalability, high voltage rating, and high modularity. Despite the fact that previous multilevel solutions were available in the market, such as, the neutral-point clamped (NPC) converter, the cascaded H-bridge (CHB), and the flying capacitor (FC) converter, these solutions have practical drawbacks [4, 21, 22]. In NPC converters, each switch has to withstand half of the dc-link voltage, consequently, these converter can only be used in the low and medium voltage range if individual 6.5 kV switches are considered. Although it is possible to increase its number of levels, an additional balance circuit for the floating capacitors is required [2]. The main issue with the CHB converter is the necessity of an isolated power supply for each H-bridge, it is common to feed each H-bridge with a multi-winding transformer, however, this is an expensive and bulky solution [3]. Finally, the flying capacitor converter hasn't reached a wide use on industry because a high switching frequency is required to ensure the capacitor voltage balance, and such frequencies are not feasible in high-power applications [23].

Recently there has been an increased interest in MMC based systems from both academia and industry. The term *modular* converters make reference to the fact that these topologies are composed of smaller units called *power electronics building block* (PEBB) or sub-modules. While the expression *multilevel* refers to the fact that these converters can modulate output voltages with more

than 2 levels. The MMC finds applications in HVDC projects [22], drive converters [24], flexible AC transmission systems (FACTSs) [25], dynamic braking chopper [26], distributed store energy systems [27], among others.

Various sub-modules (SMs) have been proposed to populate MMCs, such as the half-bridge sub-module (HBSM), the full-bridge sub-module (FBSM) and the neutral-point clamped (NPC) sub-module [28]. However, most MMC applications use the HBSM to reduce semiconductor power losses. In HVDC applications, the main drawback of the HBSM-based MMC is that it cannot control fault currents due to DC short circuits [29]. Consequently, for a pole-to-pole fault the freewheel diodes of each HBSM could be damaged [30, 31]. A possible solution, to block the DC short circuits, is to add DC breakers [32] or to change the cell type, for instance, to FBSMs [33]. Another disadvantage of the HBSM-based MMC solution is that it cannot operate with a reduced DC port voltage over a wide range. During bad weather conditions, it is a common practice to reduce the DC-port voltage to reduce the risk of pole-to-pole short circuits [34, 35].

For drive applications based on the MMC, large low-frequency voltage oscillations can occur in the capacitors of the sub modules at low mechanical speeds. Most of the proposed solutions involve the injection of high frequency circulating currents and common-mode voltage [36]. However, the circulating currents can lead to over sizing of the converter components and the high frequency common-mode voltage can reduce the lifespan of the machine bearings [37]. To decrease the large voltage oscillations a different approach is to reduce the dc-port voltage at low mechanical speed [38–41]. In [38], a back-to-back MMC composed entirely of FBSMs is proposed to regulate the dc-port voltage. Although this solution reduces the capacitor voltage oscillation at low speed, it doubles the number of switches and consequently the losses are significantly increased. In [39, 40], the dc-port voltage is modulated using series switches. In this case, the mean value of the dc-link is regulated. However, the additional switches have to withstand the rated dc-port voltage. In addition,

snubber filters have to be included to reduce the dv/dt introduced by the series switches.

The hybrid MMC, composed of both HBSMs and FBSMs, was proposed in [42]. The hybrid MMC is able to operate with a dc-port voltage lower than that achievable with a HBSM-based MMC and it has fewer components than the FBSM-based MMC. However, as demonstrated in [43], when the modulation index is large ($m \geq 2$) corresponding to a low dc-port voltage, the arm currents are unipolar (e.g. are always positive) and as a result the capacitor voltages cannot be balanced.

This thesis proposes two voltage balancing methodologies for the Hybrid MMC. The proposed strategies to ensure the local balance between the FBSMs and the HBSMs are named CLC-I and CLC-II. The former strategy guarantees the local balance by increasing the magnitude of the reactive current on the grid-side. The latter strategy ensures the local balance by injecting a circulating current component within the converter, i.e. this additional current does not appear in the AC port nor the DC port. The main advantage of this converter is that it can operate with a reduced dc-port voltage (over-modulation operation). In this thesis, the term *over-modulation* has a different meaning than the one commonly employed in the literature. For instance, for a two level inverter, the amplitude modulation index is defined as [2]:

$$m_a = \frac{\hat{V}_m}{\hat{V}_{\text{cr}}} \tag{2.1}$$

Where $\hat{V}_m$ and $\hat{V}_{\text{cr}}$ are the peak value of the phase voltage reference and the peak value of the PWM carrier respectively. In most application the value $\hat{V}_{\text{cr}}$ is kept constant. For instance, for a two-level inverter, the standard waveforms of the phase reference and the triangular carrier are shown in figure 2.2. In the previous example, the inverter is operating in over-modulation when $\hat{V}_m > \hat{V}_{\text{cr}}$. However, in this thesis the term over-modulation makes reference to an hybrid MMC that operates with a reduced dc-link voltage. In this thesis, the grid

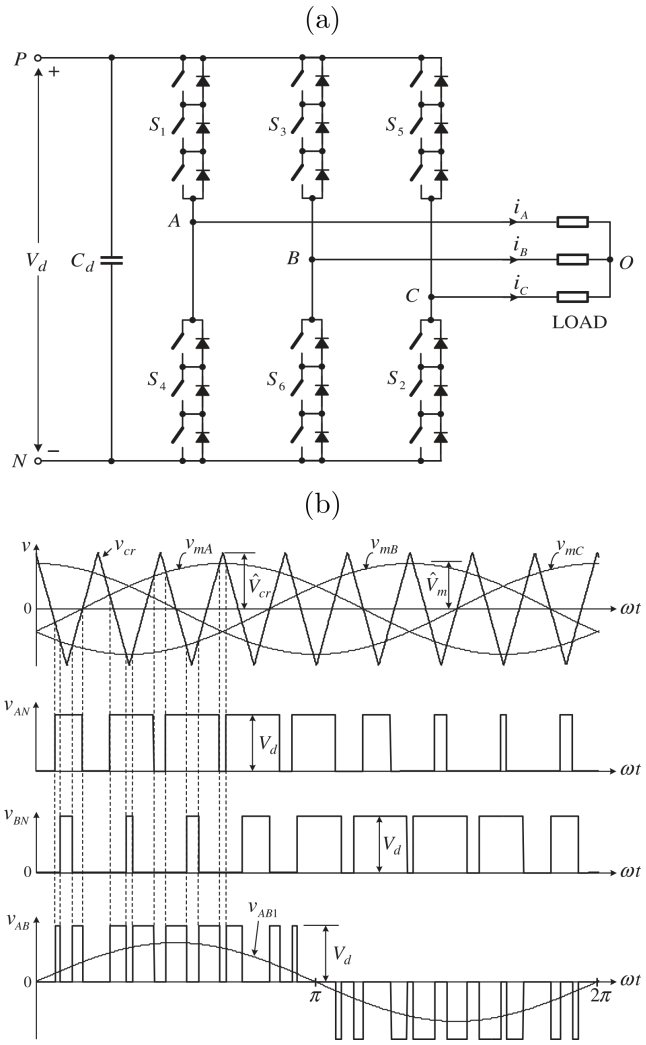


Figure 2.2: *(a) Two level inverter and (b) phase-voltage reference along with carrier waveform in a two level voltage source inverter [2]*

voltage magnitude is kept constant, while the dc-link voltage is reduced. In particular, the modulation index is defined as:

$$m = \frac{2V_g}{E} \tag{2.2}$$

Where V_g is the peak value of the grid voltage while E is the dc-link voltage. In this thesis, the converter operates in over-modulation when m>2. However, as previously noted in the literature [42], when the modulation index is higher than m>2, if no control action is taken, the arm currents become unipolar,i.e. they are strictly positive (or negative). In this scenario, the FBSMs and HBSMs capacitor voltages start to drift apart until the converter becomes

unstable. The proposed strategies ensure the local balance between these two cells types. In addition, an application of the hybrid MMC for MMC-based drive converters is presented. In this case, a back-to-back MMC solution is considered. The front-end converter is based on a hybrid MMC, while the machine-side converter is a HBSM-based MMC. In this case the hybrid MMC is used to produce a controllable dc-port voltage to reduce the capacitor voltage oscillation of the machine-side converter. An optimal value for the dc-link voltage is derived, in this case, the focus is to reduce the capacitor voltage oscillations in the machine-side MMC during low-mechanical speed. An advantage of operating the back-to-back hybrid MMC is that the required common-mode voltage injected in the machine stator is reduced.

From the previous discussion, it is concluded that the hybrid MMC can be applied in the following areas:

1. As a front-end converter in drive applications. In an MMC-based drive converter, the capacitor voltage oscillations are proportional to the dc-link voltage. Consequently, during machine start-up, operation with a lower dc-link voltage has benefits, such as the ability to operate with a reduced energy pulsation on the sub module capacitors of the drive-side MMC.

2. In HVDC applications where the dc-port voltage needs to be reduced to avoid flash-over due to bad weather conditions [30, 35, 44]. In this case, it has been proposed to reduced the dc-link voltage to avoid any short-circuit between lines. For HVDC projects installed in cold regions, a common problem is that ice can accumulate on the overhead transmission lines, if the ice weight exceeds the mechanical threshold of the transmission towers, they can collapse and consequently the power transmission will stop [45]. Currently, de-icing methods to prevent the collapse of HVDC systems are classified into three categories: mechanical, chemical and thermal [46]. The thermal method using a high DC current to

produce heat and melt the ice is simple to implement and it does not pollute the environment. For MMC-based HVDC projects, a possible solution to implement a thermal de-icer is to use an hybrid MMC. In this case, the rated power can be transfer with a reduced dc-link voltage and consequently the high dc-link current can be use to melt the ice layer [47]. Finally, the hybrid MMC can be used to interface AC grid utilities to a DC load with reduced DC voltage.

2.1 Hypotheses

The following hypotheses are stated for this research project:

1. It is possible to calculate the minimum compensating current (reactive current or circulating current) to ensure the local balance of the FBSMs and HBSMs when the hybrid MMC operates in over-modulation.

2. A closed-loop local balance control can be implemented to compensate any imbalance between the capacitor voltages of the HBSMs and FBSMs if the theoretical value is underestimated due to parameter mismatch between the theoretical model and the real system parameters.

3. A global capacitor balancing control can be developed to maintain the voltage balance in all 6 arms of the hybrid MMC.

4. It is possible to reduce the injected common-mode voltage by a HBSM-based MMC when it is driving an induction machine at low mechanical speed.

2.2 Objectives

This PhD research project aims to contribute to the state of the art of the hybrid MMC, in particular, to propose a control for the over-modulation operation of the hybrid MMC. Then, a drive application is presented, in this case

the hybrid MMC acts as a front-end converter to regulate the dc-link voltage of a HBSM-based MMC. Consequently, the objectives of this thesis are listed below:

1. To derive a decoupled model of the hybrid MMC. The main objective is to propose a decoupled control to ensure the arm energy balance, the cell balance between the FBSMs and HBSMs, and the current control of the AC and DC outer ports.

2. To propose a simple method to derive the minimum compensating currents to ensure the local balance of the hybrid MMC.

3. To add a closed-loop voltage control loop to correct any mismatch between the capacitor voltages of the FBSMs and HBSMs during overmodulation operation.

4. To design and build an experimental rig to validate the performance of the proposed control strategy for the hybrid MMC. In addition, the operation of the hybrid MMC (front-end) along with a HBSM-based (drive-converter) operating in a back-to-back configuration is tested.

2.3 Thesis outline

The remainder of this thesis is divided in the following chapters:

1. Chapter 2: A literature review of the most common multilevel solutions is presented, in particular their advantages and drawbacks are discussed to understand the relevance of modular and multilevel solutions. Next, the basic cell topologies, main control strategies, modulation schemes, and applications of the modular multilevel converter are explained. In particular, the challenges related to the drive applications are discussed and several solutions presented in the literature are shown. Finally, the application of the hybrid MMC to modify the dc-link voltage of a HBSM-based MMC is presented.

2. Chapter 3: The voltage-current decoupled model of the MMC is introduced. In addition, the energy model of the MMC is also explained. These two models are used to derive a closed-loop control of the MMC. In addition, the sizing of a general hybrid MMC (front-end converter) is presented. Finally, the sizing of a MMC for drive application is discussed. Due to the different output frequency of the grid- and machine-sides converters, the minimum cell capacitances are calculated differently for each case.

3. Chapter 4: This chapter explains the proposed control strategies to ensure the local balance of the hybrid MMC during over-modulation. The methods are called closed-loop control (CLC) I and II. In CLC-I, the reference of the reactive current is controlled to ensure the local balance of the hybrid MMC. Then, in CLC-II the local balance is accomplished by injecting a circulating current within the converter. The global control strategy of the hybrid MMC is also presented. Next, the control of a back-to-back MMC-based drive application is presented. The optimal value of the dc-link voltage is derived to reduce the capacitor voltage oscillations during over-modulation.

4. Chapter 5: The proposed controllers are validated through full-scaled simulation results. The unbalance problem between the FBSMs and HBSMs for a hybrid MMC operating in over-modulation is shown. Then 2 main cases are considered: Hybrid MMC operation and MMC-based drive application. First, the hybrid MMC controller is studied when the converter is feeding a 3 MW load and it is operating with a grid voltage equal to 6.9 kV. Second, the application of variable dc-link voltage is presented for an MMC based drive converter.

5. Chapter 6: The experimental rig used to validate both control strategies is presented. The main constructive aspects, such as, the control platform, modulation scheme implementation, measurement acquisition

boards are explained.

6. Chapter 7: The proposed controllers are validated using an experimental rig. Firstly, the operation of the hybrid MMC is shown. In this case, both control strategies are presented and tested. In addition, the proposed local balance controllers are compared with 2 strategies presented in the literature. Then, the operation of the closed-loop voltage controller is tested considering that the feed-forward term is miscalculated. The transient response for a load-step is also shown. Secondly, the back-to-back hybrid MMC converter is discussed, the grid-side converter is a hybrid MMC while the machine-side converter is an HBSM-based MMC. The hybrid MMC imposed a controllable dc-link voltage to reduce the capacitor voltage oscillations of the machine-side converter. The main advantage is the reduction of the common-mode voltage applied to the machine stator.

7. Chapter 8: The conclusions, main contributions and a perspective for further improvements are presented in this Chapter.

Chapter 3

Literature review of multilevel converter topologies

3.1 Introduction

In recent years, there have been significant advances in various fields which contribute to the development of power electronics: semiconductor switches technology, converter topologies, and control strategies, among others. In particular, the development of multilevel topologies has been encouraged for several reasons, such as: to reduce industrial process costs, to exploit new technological advantages, to implement actions against the global warming effects, among others. In many industrial processes, the overall operational costs are reduced by reaching economies of scale; the final goal of this idea is to reduce the total cost by increasing the scale of operation. For instance, economies of scale are obtained by increasing the power of the electrical machine driving these industrial processes. In most cases, the power is increased by using medium-voltage drives up to a voltage of 13.8 kV [3]. Some examples of these industrial applications are pipeline pumps in the petrochemical industry [48], fans in the cement industry [48], pumps in water pumping stations [49], traction applications in the transportation sector [50], steel rolling mills in the metals industry [51], among others.

Furthermore, in the last decade, there have been advances in the use of DC in applications, especially in high-voltage direct current (HVDC) projects. Most of the electrical grid infrastructure is based on AC systems. However, in some cases, the use of DC systems presents several advantages. Due to the global warming effect, several countries have adopted policies to increase electrical generation using renewable sources (solar, wind, among others). In the last years, offshore wind farm projects have been developed by several countries because stronger and steady winds are abundant in the sea, and the visual and audible noise impact is considerably reduced [52] in comparison with onshore solutions. It has been shown that for long-distance undersea transmission, HVDC systems have a lower cost than high-voltage alternate current (HVAC) systems. In [53], it is concluded that an HVDC solution has lower annual costs than the equivalent HVAC system for a 100 MW wind park.

Initially, the 2 level voltage source converter (VSC) was adopted to be used in medium voltage applications by connecting several switches in series to produce an equivalent switch with a higher voltage blocking capability. Although it is possible to scale this solution indefinitely, it has various practical disadvantages. Since the series switches and their gate drives are not exactly the same, the series switches will not be able to evenly share the total voltage in the blocking states or during transients. To solve this problem, snubber circuits are added [54]. However, the total efficiency is reduced and the required volume of the converter increases.

This chapter presents a review of multilevel converters (MC) developments, i.e. converters that can output voltages with more than two levels. In particular, multilevel converters are classified into two main areas: Classical Multilevel Converters and Modern Multilevel Converters. The most common and well established classical MCs are the neutral-point clamped (NPC) converter, flying capacitor (FL) converter, and the cascaded H-bridge sub-module (CHB) converter [55–57]. Conversely, in the modern MC family, converters such as the modular multilevel converter (M^2C), the modular multilevel matrix converter

(M^3C), and variations of these topologies are considered.

3.2 Classic Multilevel Converters

Before the introduction of multilevel converters, it was a common solution to connect several switches in series to increase the converter rated voltage [2] of the two level VSC. However, this approach has some practical problems. Besides the voltage equalization problem depicted before, the two level VSC has high harmonic distortion, high electromagnetic interference (EMI), and it requires bulky and expensive passive filters. Multilevel converters were proposed to overcome these problems. These converters have a better performance than the 2 level VSC: better current quality, higher voltage capability, lower switching losses, and lower dV/dt. The following three topologies become established in the industry: the 3 level neutral-point clamped (NPC) [55, 58, 59], the flying capacitor (FL) voltage source converter [60, 61], and the cascade H-bridge converter (CHB) [62–64]. The advancement in high-voltage insulated-gate bipolar transistors (IGBTs) and integrated-gate commuted thyristors (IGCTs) has led to an increase in voltage source converters (VSC) over current source converters in industrial applications.

3.2.1 Neutral-point clamped converter

The NPC converter was proposed by Nabae from the research group of Professor Akagi in the Tokyo Institute of Technology [65] in 1981. The diode clamped multilevel converter is a widely used topology for medium voltage and high power applications reaching several megawatts. It has been applied successfully in drive applications such as conveyors, pumps, fans, and mills for industries in the oil, metal, mining, and marine sector [66, 67].

The NPC converter uses clamping diodes and cascaded capacitors to produce a multilevel output voltage. The minimum realisation of this topology can produce three voltages levels. Although it is possible to produce more than

three levels, the control and circuit topology become impractical; consequently, most industrial applications use the 3-level NPC [3]. The main advantages of the NPC over the standard 2-level voltage source converter are: low dv/dt in the output voltage, low harmonic distortion in the output current, each switch withstand a maximum voltage equal to half of the dc-link voltage, and the 3-level NPC can be used in the medium-voltage range without connecting switching devices in series [2].

The circuit topology of a 3 level NPC is shown in Fig. 3.1; each leg is composed of 4 switches with 4 anti-parallel diodes. The dc-port capacitor is split in 2 series capacitor C_{d1} and C_{d2}. In addition, the neutral point Z is connected to the output port through 2 clamping diodes per leg.

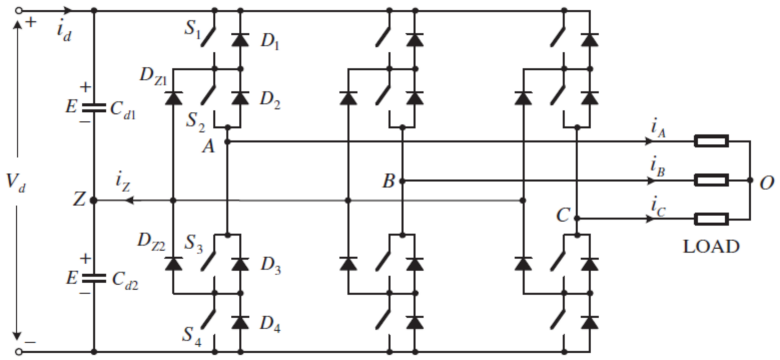


Figure 3.1: *Circuit topology of a neutral-point clamped (NPC) 3 level converter [2].*

Each leg has 3 valid switching states, as shown in Table 3.1. In this case, the output voltage is measured from the neutral point Z. In the following analysis, the floating capacitors are balanced, and each one has a voltage equal to E. In the state P, the 2 upper switches S_1 and S_2 turn on while the rest are off, the output voltage is E with respect to the middle point Z. If only the inner switches are turned on, the output port is connected to the middle point through one of the clamping diodes. Finally, if the lower 2 switches S_3 and S_4 are turned on, the output voltage is $-E$.

To reduce the switching losses and preserve a high quality output waveform, the transitions between the switching states **P** and **N** are forbidden, therefore

Switching state	S_1	S_2	S_3	S_4	Output voltage
P	ON	ON	OFF	OFF	E
O	OFF	ON	ON	OFF	0
N	OFF	OFF	ON	ON	$-E$

Table 3.1: Switching states of the 3 level NPC.

the only valid state changes are **P**↔**O** and **N**↔**O**. By avoiding the transition **P**↔**N**, each switch withstand a maximum voltage equal to E. Despite the advantages of the NPC converters over the 2 level VSC, it has some practical issues; for instance, it is necessary to balance the floating capacitors of the dc-side, and the semiconductor losses are unevenly shared among the switches [3].

For the 3L-NPC converter, there are 2 established solutions to ensure the balance of the floating capacitors. The first solution uses the redundant switching states of the converter to regulate the current that flows to the neutral point Z. The valid switching states, for a 3L-NPC, are shown in Fig. 3.2(a), notice that they can be classified in 4 groups according to their length: *zero* vectors, *small* vectors ($V_d/3$), *medium* vectors ($V_d/\sqrt{3}$), and *large* vectors ($2V_d/3$). The switching states to produce each vector are shown in Fig. 3.2(b). From this figure, notice that the zero and small vectors have redundant states. By using these redundant states, it is possible to change the direction of the injected current to Z and thus to balance the floating capacitors [58, 59, 68, 69]. In the second approach, the floating capacitor balance is accomplished by injecting a zero-sequence voltage in the modulation voltage reference [70, 71]. Nowadays, the balance problem is solved for the 3L-NPC. Although it is possible to increase the number of levels, in this case, an additional voltage balancing circuit is required to ensure a proper converter operation [72].

Finally, as stated before, the main disadvantage of the NPC converter is the uneven semiconductor loss distribution [73, 74]. The unequal semiconductor losses among switches will produce different junction temperatures; consequently, the maximum current will be limited by the switch that reaches

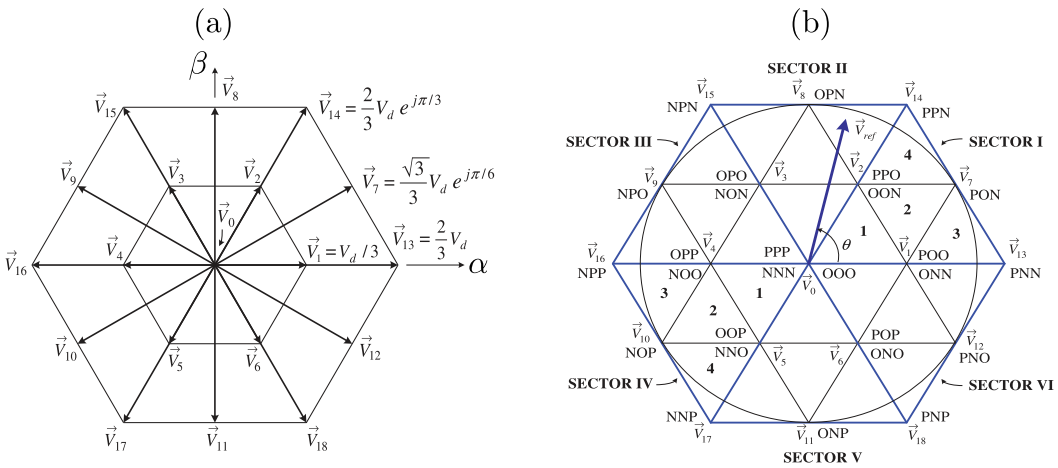


Figure 3.2: *(a) Space vector diagram of a 3L-NPC and (b) division of sectors and regions [2].*

the highest temperature. In 2001, Bruckner et. al. [75] proposed the active neutral-point clamped converter (ANPC) to improve the loss distribution. In this case, the clamping diodes are replaced by active switches, and as a consequence, each leg has four redundant states to output zero. In [76], the junction temperature of each switch is estimated online, and then a look-up table is used to select the least stressed switches to modulate the voltage reference. In drive applications, the 3L-NPC converter can reach an output voltage of 4.2 kV by using 6.6 kV devices. It is possible to increase the voltage range by adding more levels. However, for NPC converter with more than 3 levels, an additional balancing circuit is required to ensure the proper balance among the flying capacitors [2].

3.2.2 Flying capacitor converter and Cascaded H-bridge converter

In addition to the NPC converter, there are other 2 well established multilevel topologies for drive applications [3], the flying capacitor (FL) converter, and the cascaded H-bridge converter (CHB) that are shown in Fig. 3.3 (a) and (b) respectively.

The FL converter was firstly proposed in [77]. There is a commercial version of a 4-level FL converter for drive applications [17]. The 4L-FL converter

shown in Fig. 3.3.a has 64 valid switching states to produce the output voltage phase v_{xN}=$\{V_{dc}/2, V_{dc}/6, -V_{dc}/6, -V_{dc}/2\}$, the redundant switching states can be used to balance the floating capacitor voltages. The main disadvantage of this converter is the capacitor voltage balance of the flying capacitors; since the load current flows through them, a high switching frequency is required to minimise their oscillations. A phase shift modulator has been proposed to naturally balance the capacitor voltage of an FL converter [78]. Alstom developed a commercial 4 level flying capacitor converter, which is named *ALSPA VDM6000*. This converter has an output voltage of 3.3 kV, and its rated power is 4.6 MVA [79].

The cascaded H-bridge was proposed in 1988 [80]. Each phase consists of N H-bridges in series. By stacking more cells, this converter can achieve a higher output voltage. However, the main drawback of this converter is that a multi-pulse transformer is required to produce the N isolated dc power supplies, such a transformer is bulky and expensive, and it is the main limitation to increase the number of levels [81]. A possible solution to reduce the number of H-bridges is to have different voltages cells. However, in this case, it is not possible to cancel the input current harmonics, and each cell requires a unique design depending on its voltage level [82].

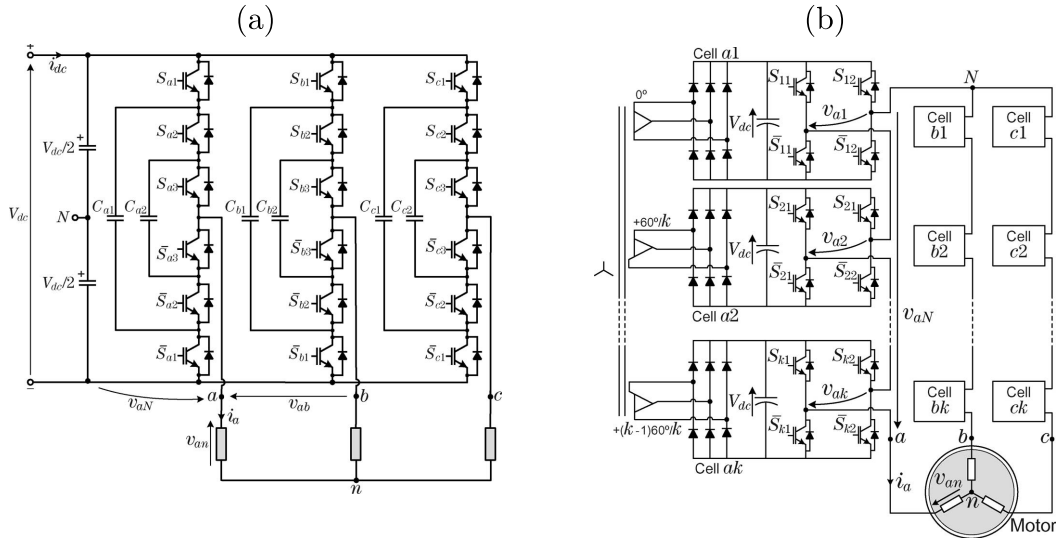


Figure 3.3: *(a) Flying capacitor converter and (b) cascaded H-bridge converter [3].*

3.3 Modern Multilevel Converters

The first multicellular converter capable of reaching a high number of levels without requiring isolated DC sources was proposed by Lesnicar et. al. in 2003 [20], it was called Modular Multilevel Converter (MMC). Unlike previous multilevel converters, the MMC is composed of small independent converters called sub-modules. Each sub-module does not require an isolated dc-power supply. Moreover, it is straightforward to increase its voltage rating by adding extra sub-modules due to its modular structure.

Since its introduction, more multilevel converters based on the MMC structure have been proposed. Initially, the MMC was intended to interface a three-phase AC system with a DC bus bar. The modular structure has also been applied to interface two three-phase systems. For instance, the modular multilevel matrix converter (M^3C) was proposed in [83], and it has the same structure as the standard matrix converter [84], except that each switch is replaced by an array of several FBSMs connected in series. Another modular converter that has gained attention is the hexverter [85]; this converter can also be used to interface two 3 phase AC systems, but it requires fewer sub-modules than the M^3C.

3.3.1 The Modular Multilevel Converter

The modular multilevel converter (MMC) is a prominent solution for high voltage direct current (HVDC) transmission systems [86, 87] and for medium voltage drive applications [88, 89]. The main benefits of the MMC are its modularity and scalability to reach high voltage requirements, high efficiency, low harmonic distortion, transformerless operation, and reduced dv/dt in each switch [90, 91].

The circuit topology of a standard MMC is shown in Fig. 3.4. It has the same structure as a 2-level VSC, but the main switches have been replaced by a series connection of N sub-modules, creating an *arm*. In addition, an inductor

L is connected to each arm. The inductor is used to filter high-order harmonics due to the switching frequency and to limit circulating currents resulting from the operation of the circuit. Each output phase is connected to an upper and lower arm, denoted as U and L. Several sub-modules have been proposed in the literature to use as a building block in the MMC [4]. For instance, the half-bridge sub-module [92], the full-bridge sub-module (FBSM) [87], the clamp-double cell [93], 3L neutral-point clamped [94], 3L flying-capacitor [95], and the 5L cross-connected cell [4]. The circuit topology of each cell is shown in Fig. 3.5. The cell type that requires the fewest switches is the HBSM; as a consequence, most of the MMC commercial projects employ the HBSM as a building block since it has lower semiconductor losses and only two gate signals are required. Despite the previous advantages, the main issue with the HBSM is that it cannot be used to limit currents resulting from a short circuit on the main dc bus. This feature is important in HVDC applications, where short circuits may occur. In the event of a dc-fault, the anti-parallel diodes of each cell will conduct the fault current, and in the process, they may be destroyed. The short-circuit can be mitigated if a cell type able to output negative voltages is used. For instance, the FBSM, the clamp-double cell, and the 5L cross-connected cell can output positive and negative voltage values. In addition, it is possible to use a cell with more voltage levels to further reduce the AC side harmonic distortion, for instance, the 3L NPC cell and the 3L FC cell. A comparison between these cell types is shown in Table 3.2.

Cell topology	Output voltage	DC-fault capability	Losses
Half-bridge	$0, v_C$	No	Low
Full-bridge	$0, \pm v_C$	Yes	High
Clamp-double	$0, v_{C1}, v_{C2}, v_{C1}+v_{C2}$	Yes	Moderate
3L FC	$0, v_{C1}, v_{C2}, v_{C1}-v_{C2}$	No	Low
3L NPC	$0, v_{C2}, v_{C1}+v_{C2}$	No	Moderate
5L Cross-connected	$0, v_{C1}, v_{C2}, v_{C1}+v_{C2}$	Yes	Moderate

Table 3.2: Comparison among several cell circuits for MMC applications.

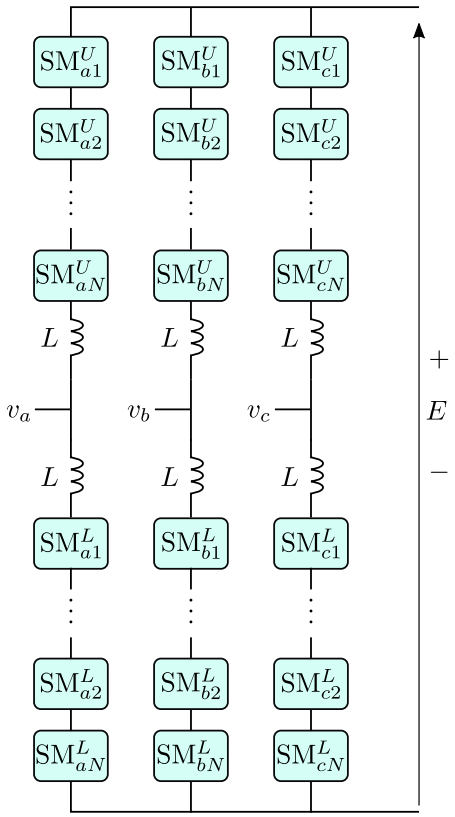


Figure 3.4: *General circuit topology of a modular multilevel converter (MMC).*

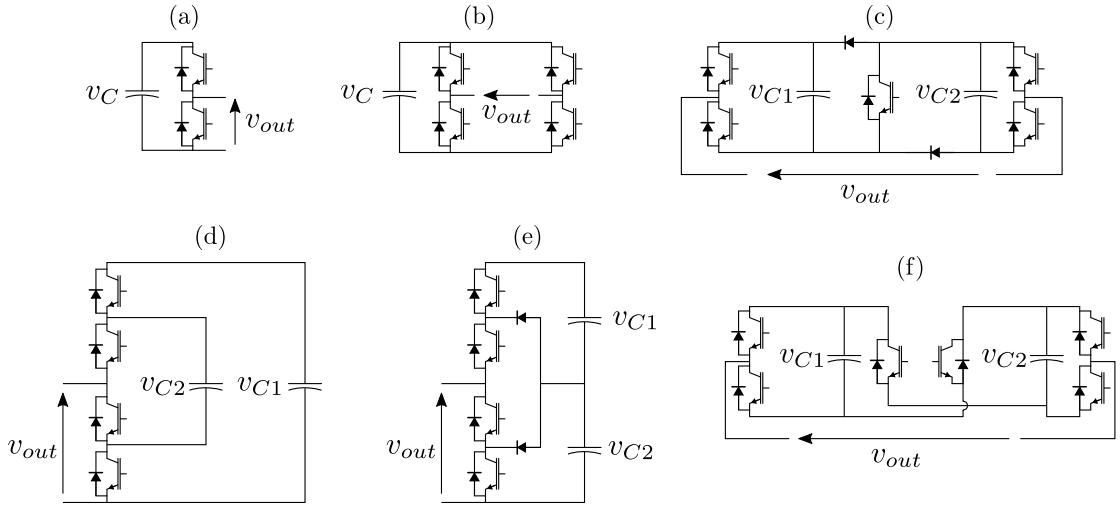


Figure 3.5: *(a) HBSM, (b) FBSM, (c) clamp-double cell, (d) 3L flying-capacitor cell, (e) 3L neutral-point clamped cell, and (f) 5L cross-connected cell.*

3.3.2 Modulation schemes for the MMC

Several modulation schemes have been proposed in the literature for the M^2C [4, 96–98]. They are classified according to the requirement for single or multiple reference waveforms. The most common modulation methods are explained next.

1. **Single reference waveform**:

   (a) **Carrier-disposition PWM techniques**: In this case, each sub-module has its triangular carrier displaced symmetrically. The switch state of each cell is obtained by comparing the voltage reference of each arm with the cell carrier waveform. Depending on the carrier phase-shift, these modulators are grouped in: phase disposition (PD), phase opposition disposition (POD), and alternate phase opposition disposition (APOD), as shown in Fig.3.6.a to Fig.3.6.c respectively. Although the implementation of these techniques is straightforward, its main disadvantage is the unequal sub-module utilisation which increases the AC voltage harmonic distortion and the circulating currents. In [99], a modified capacitor voltage balance control is proposed for PD-PWM; in this case, a sorting algorithm is introduced to assign which cells will be inserted at the end of each control period. In addition, a constant voltage offset multiplied with the cell switch state is added to each capacitor voltage measurement to reduce unnecessary switching actions. In [100], a new controller for the circulating current is proposed for a low cell count MMC; in this case, the arm-inductor voltage drop is not neglected, unlike in most HVDC applications. The second harmonic is considerably reduced without increasing the control complexity and the main advantage is the reduction of the semiconductor losses.

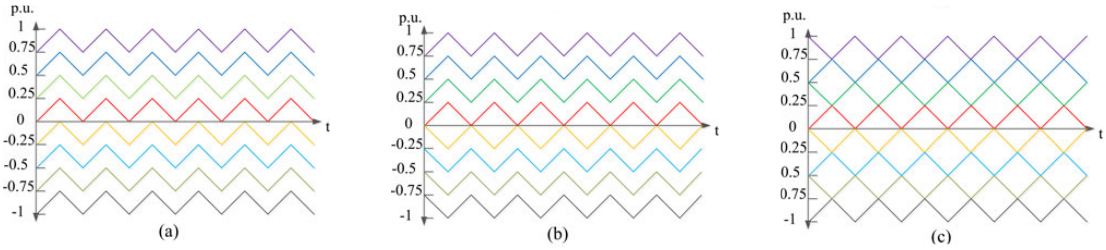


Figure 3.6: *Carrier-disposition modulation schemes: phase disposition (a), phase opposition disposition (b) and alternate phase opposition disposition (c) [4].*

   (b) **Sub-harmonic techniques**: In this case, the modulator uses 2N

identical carriers per phase-leg, where N is the number of sub-module in each arm, with a phase shift of $\frac{\pi}{N}$. The sub-harmonic technique has lower harmonic distortion than the carrier-disposition PWM [101].

2. **Multiple reference waveform**:

   (a) **Direct modulation**: In this case, the number of inserted cells for the upper and lower arm is calculated using (3.1)-(3.2) respectively, where $v_{\mathrm{j,ref}}$ is the output voltage reference and V_{DC} is the dc-port voltage. Due to its simplicity, most MMC applications employ direct modulation-based techniques. The main disadvantage of this technique is the presence of circulating current [102]. In addition, this method introduces a coupling between the output power and some internal variables, such as the sub-module capacitor voltage, dc-port current, and the circulating currents. In [103], a new closed-loop controller of the dc-port current is introduced to avoid this coupling issue.

$$n_{\mathrm{p,j,ref}} = N\frac{0.5V_{\mathrm{dc}} - v_{\mathrm{j,ref}}}{V_{\mathrm{dc}}} \tag{3.1}$$

$$n_{\mathrm{n,j,ref}} = N\frac{0.5V_{\mathrm{dc}} + v_{\mathrm{j,ref}}}{V_{\mathrm{dc}}} \tag{3.2}$$

   (b) **Indirect modulation**: In this case, the voltage reference for the upper and lower arm are calculated as in (3.3)-(3.4). The term $v^{\Sigma}_{\mathrm{reg,j}}$ is used to control the total energy in arm-j while $v^{\mathrm{circ}}_{\mathrm{reg,j}}$ balances the energy between arms. The indirect modulation technique can be implemented using a closed-loop control in which the terms $v^{\Sigma}_{\mathrm{reg,j}}$ and $v^{\mathrm{circ}}_{\mathrm{reg,j}}$ are the output of a controller [104], conversely, these terms

can be estimated (open-loop control) [105].

$$n_{\mathrm{p,j,ref}} = N\frac{0.5V_{\mathrm{dc}} - v_{\mathrm{j,ref}} - v^{\Sigma}_{\mathrm{reg,j}} - v^{\mathrm{circ}}_{\mathrm{reg,j}}}{\sum_{i=0}^{N} v_{\mathrm{cp,i,j}}} \tag{3.3}$$

$$n_{\mathrm{n,j,ref}} = N\frac{0.5V_{\mathrm{dc}} + v_{\mathrm{j,ref}} - v^{\Sigma}_{\mathrm{reg,j}} - v^{\mathrm{circ}}_{\mathrm{reg,j}}}{\sum_{i=0}^{N} v_{\mathrm{cn,i,j}}} \tag{3.4}$$

(c) **Phase-shifted carrier (PSC) based PWM technique [98, 106]**: In this case, the modulation index of each sub-module is calculated using (3.5)-(3.6) for the upper and lower arm respectively. The term $v_{\mathrm{a,j}}$ regulates the average capacitor voltage of arm-j while $v_{\mathrm{b,i,j}}$ regulates the individual capacitor voltage of module i-th of phase-j. In this case, each cell has its own carrier that is phase-shifted with respect to the next sub-module; by changing the carrier phase-shift, it is possible to minimize the harmonics in the circulating current or in the output voltage. The main advantages of PSC are the even distribution of losses among the sub-modules and its modularity and scalability analogous to the M^2C structure.

$$m_{p,i,j} = \frac{\frac{V_{\mathrm{dc}}}{2N} - \frac{v_{\mathrm{j,ref}}}{N} + v_{a,j} + v_{b,i,j}}{v_{\mathrm{cp,i,j}}} \tag{3.5}$$

$$m_{n,i,j} = \frac{\frac{V_{\mathrm{dc}}}{2N} + \frac{v_{\mathrm{j,ref}}}{N} + v_{a,j} + v_{b,i,j}}{v_{\mathrm{cn,i,j}}} \tag{3.6}$$

3.3.3 Capacitor voltage compensation strategies for the MMC-based drive converter

Originally, the M^2C was intended as an interface between power generation and transmission of electrical energy using HVDC (High Voltage Direct Current) converters [107, 108]. In HVDC applications during normal operation, the capacitor voltage control is well documented, and several strategies have been proposed. In this area, the research is focused currently on the operation of HVDC links under unbalanced grid conditions and the converter capability to operate under short circuits in the DC, and AC ports [22, 109, 110].

Some authors have proposed the use of the M^2C for medium-voltage drive applications over classical multilevel topologies such as the NPC converter, FL converter, and the CHB converter [111, 112]. However, the most difficult operation point for drive applications occurs when the electrical frequency of the machine is close to zero and the initial torque is high, since the magnitude of the capacitor voltage oscillations of an MMC are inversely proportional to the frequency of the AC port [36]. Several authors have presented strategies to overcome this issue, Korn *et al.* proposed a controller to drive induction machines with a quadratic torque profile [113] where the upper and lower power arms are grouped in a common $p_{\mathrm{x,cm}}$ and differential $p_{\mathrm{x,dm}}$ portion (3.7)-(3.8). A low-frequency mode (LFM) controller is defined in which the circulating current is calculated as $i_{\mathrm{cx}} = i_{\mathrm{cx,cm}} + i_{\mathrm{cx,dm}}$ for each phase. The common portion $i_{\mathrm{cx,cm}}$ regulates $p_{\mathrm{x,cm}}$ while $i_{\mathrm{dx,cm}}$ controls its differential part $i_{\mathrm{cx,dm}}$. The circulating current components are calculated using an algebraic equation [113]. A sinusoidal common-mode voltage v_0 is imposed to regulate some remaining arm power terms. Moreover, to shrink the speed range of the LFM, Korn *et al.* proposed a rotor flux optimization in which the magnitude of the machine current is proportional to the machine frequency.

$$p_x^P = p_{\mathrm{x,cm}} + p_{\mathrm{x,dm}} \tag{3.7}$$

$$p_x^N = p_{\mathrm{x,cm}} - p_{\mathrm{x,dm}} \tag{3.8}$$

Antonopoulus *et al.* proposed an open-loop system for a M^2C-based drive machine at rated torque for the whole speed range [114]. For low mechanical speed, two circulating current with frequencies $\omega_{\mathrm{cm}} + \omega_S$ (positive sequence) and $\omega_{\mathrm{cm}} - \omega_S$ (negative sequence) are injected, where ω_{cm} is the frequency of the injected sinusoidal common-mode voltage and ω_S is the electric machine frequency. The magnitude of the circulating currents and common-mode voltage, along with ω_{cm} are calculated using an off-line optimization. Although the capacitor balance is accomplished, for low frequencies, the arm current

is up to 3 times the rated machine current [114], therefore the SMs have to be overrated. Moreover, the open-loop performance depends on how accurate the estimated system parameters are, and in general, it does not have a good transient response.

Kolb *et al.* have proposed a decoupled model of the M^2C using a linear transformation to express the variable systems in terms of the average and difference of the upper and lower voltages and currents [115]. Using the DC part, the positive and negative sequence components of the circulating currents, the controller regulates the mean value of the arm power to zero to balance the capacitor voltages of each module. Espinoza *et al.* [116] use the $\Sigma\Delta\alpha\beta 0$ transformation to decouple the dynamic of the AC voltage and current with the dynamic of the inner converter variables. In this case, a nested controller is proposed to balance the capacitor voltage, and instead of using the negative sequence of the circulating current, a high-frequency component in the common-mode voltage and in the circulating current is injected to balance the voltage oscillations at low machine frequency.

Some authors have proposed the use of finite control set-model predictive control (FCS-MPC) to address the capacitor voltage balance problem. However, since the M^2C might possess a high number of sub-modules, for instance, over 100 modules per arm for HVDC applications, an exhaustive search of the state that minimizes a given cost function will be potentially unfeasible. In [117], an FCS-MPC strategy is proposed to control the ac-side currents, to balance the capacitor voltage and to minimize the circulating currents using a discrete-time model for a one-step forward prediction. The controller evaluates a cost function for every valid state. Although the simulation results of [117] shows a good steady-state and transient response, the number of valid states increase drastically with N; for instance, for $N = 50$ there are over $7 \cdot 10^{18}$ valid states. To reduce the number of evaluations, in [118] the control problem is solved by applying three MPC controllers to regulate different objectives; as a consequence, the number of evaluations decreases and additionally, there is no

requirement to tune weighting factors since each MPC has a single-objective cost function. The first MPC regulates the ac current, the second MPC regulates the current of the dc-port, and finally, the third MPC balances the capacitor voltage of each module. However, the approach of [117, 118] may produce a high dv/dt during transients since they consider all possible output voltages levels. A fast FCS-MPC is proposed in [119], in this strategy, only a reduced set of valid states is considered. Specifically, only the nearest voltage levels around the previous optimal voltage level are taken into account at every sampling time. In addition, in this case, the capacitor voltage balance is achieved by using a voltage sorting algorithm. However, these approaches require a high sampling time to ensure a proper tracking error, and in most cases, it is only feasible to predict a reduced number of steps due to the high computational burden of the algorithm.

3.3.4 Modular Multilevel Matrix Converter and Hexverter

Nowadays, the term *modular converters* (*MC*s) describes a varied family of converters that share the common feature of being composed of smaller converters called sub-modules. The most popular modular converter is the MMC; however, there are two additional modular topologies that are being studied by several research groups: the modular multilevel matrix converter (M^3C) and hexverter. These topologies are shown in Fig. 3.7 respectively, where each block represent a sub-module. A complete review of these topologies can be found in [120] that address the modelling, controller systems, modulation techniques, and principal applications.

The M^3C is an AC to AC power converter where each phase of one AC-side is connected to the 3 phases of the other AC-side by a stack of full-bridge sub-modules (FBSMs) in series with an inductor; therefore, the M^3C is composed of 9 arms. This converter makes bidirectional power transfer possible between the 2 AC systems and guarantees sinusoidal waveforms on both sides.

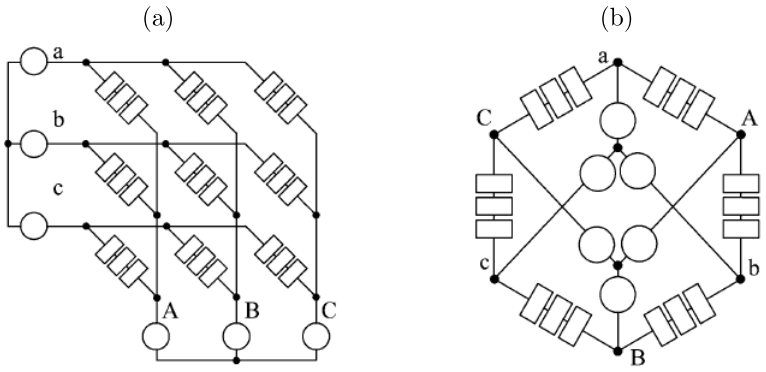


Figure 3.7: *(a) M^3C and (b) Hexverter.*

Besides regulating the input and output converter current, the controller has to balance the voltage of each floating capacitor. Experimental results for this converter have been achieved by using the double $\alpha\beta 0$ transformation to obtain a decoupled model of the converter [121–124]. The double $\alpha\beta 0$ transformation allows modelling the converter using four circulating currents to balance the capacitor voltages independently of the input and output ports. In [125], a different transformation is proposed to obtain a decoupled model of the M^3C; in this case, predictive control is implemented in the current control loops. The M^3C can be used in gear-less drives [113]. In [123], the M^3C is proposed to interface a wind generator with the grid. Recently, it has been proposed to use the M^3C to interface wind parks using low-frequency AC transmission systems[126].

The current challenge associated with the M^3C is to balance its flying capacitors during all operating conditions. The balancing task becomes difficult when the input and output AC port have the same frequency; this drawback limits the application of the M^3C to drive machines over the full speed operation range. The high voltage oscillations of the sub-modules are controlled by manipulating the circulating currents and injecting auxiliary signals such as common-mode voltage [127]. In [128], reactive power is injected in the input AC side to maintain the capacitor balance; however, some applications do not permit the injection of reactive power to the grid [127].

Recently a novel converter, called the *Hexverter*, has been proposed for in-

terfacing 2 AC systems [129–131]. According to Baruschka *et al.* [131] this converter has a good performance for low-frequency speed applications, such as wind energy. The hexverter is composed of 6 arms, and as in the M^3C, each branch is constituted exclusively of FBSMs plus an inductor in series. In this case, only one circulating current exists. The capacitor voltage control regulates the cells in one branch, and also the branches need to be balanced as well. However, for some operation points, it is necessary to work with a power factor lower than 1 to ensure the sub-module capacitor voltages balance [129]. A comparison between the M^3C, hexverter and the M^2C was carried out in [132, 133]. A systematic and fair comparison methodology was carried out to obtain meaningful results. In this respect, all converters are designed to have the same unit capacitance constant H, which is defined as the ratio between the energy stored in the converter and its nominal power [133]. The name of the H constant is associated with the unit inertia constant in synchronous rotary condensers [134]. For every multilevel converter topology, its capacitor voltage oscillations are inversely proportional to its H constant [135]. However, increasing H results in a more expensive converter.

Ilves *et al.* conducted a qualitative comparison of the M^3C, M^2C and *Hexverter* [132] to quantify the semiconductor requirements and pulsations of the stored energy in each topology. To obtain the device requirements, the normalized power rating n_{pr} is defined as in (3.9) where S_{conv} is the rated power of the converter, S_{sm} is the combined power rating of the semiconductor devices, n_{arm} is the number of arms, n_{sm} is the number of semiconductors per sub-module, and $\hat{V}_{\text{arm}}$ and $\hat{I}_{\text{arm}}$ are the peak-value of the voltage and current of one generic arm respectively.

$$n_{\text{pr}} = \frac{S_{\text{sm}}}{S_{\text{conv}}} = \frac{n_{\text{arm}} n_{\text{sm}} \hat{V}_{\text{arm}} \hat{I}_{\text{arm}}}{S_{\text{conv}}} \tag{3.9}$$

The value of n_{pr} for the previous converters depends on the implemented controller, however, assuming an equivalent circulating current method [132] the

n_{pr} for a back-to-back (BTB) half-bridge based M^2C, M^3C and the hexverter are depicted in Table 3.3, along with the rms and peak arm current. Therefore, the BTB M^2C stands out with a minimum combined power rating among the modular converters, and the hexverter has the highest rms and peak values, and thus requiring sub-modules with higher power ratings than the other topologies.

Converter Topology	n_{pr}	RMS current pu	Peak current pu
Back-to-back M^2C	24	0.433	0.75
M^3C	32	0.333	0.667
Hexverter	37	0.577	1.15

Table 3.3: Normalized currents and semiconductors ratings.

The voltage oscillations are studied by calculating the peak-to-peak value of the energy variation for each converter. Both the M^3C and the hexverter become unstable at synchronous frequency if no circulating currents are applied, while the BTB M^2C only presents oscillations in the capacitor voltage at low frequency if no circulating currents are applied. Moreover, in [132] it is concluded that both the M^3C and hexverter require the injection of reactive power to decrease the capacitor voltage oscillations and thus restrict its applications.

In [133] the voltage oscillations of the M^2C and M^3C produced when driving an induction machine are compared through simulations and experimental tests. In this case, H=50 ms for both converters. The authors of this work concluded that the M^2C is more suitable to drive quadratic torque profile loads such as fans, blowers, pumps and centrifugal compressors. In contrast, the M^3C is more appropriate to drive low-speed high torque motors such as mills, kilns, conveyors, and extruders. Moreover, the capacitor voltage oscillations as a function of the motor torque and frequency are calculated. In order to make a fair comparison, no mitigation scheme is employed. For an M^2C, the voltage oscillations are lower than 20% of the capacitor voltage reference for frequencies higher than 21 Hz independently of the motor torque. Concerning

the M^3C, the voltage oscillations are higher for frequencies above 42 Hz, and as the motor frequency approaches the synchronous frequency (50 Hz) the oscillations increase drastically.

3.4 Novel Modular topologies for drive applications

To solve some of the problems associated with the M^2C applied to drive machines, several authors have proposed new M^2C-based topologies. These new converters aim to maintain the capacitor voltage balance during low machine frequency without injecting auxiliary signals such as common-mode voltage or circulating currents. Although circulating currents do not affect the output or input port, their use should be minimal to avoid the overrating of semiconductor components and to increase the converter efficiency [136]. The use of common-mode voltage has been criticized [137] since it produces insulation damage and leakage currents in the machine bearings.

To avoid the problems associated with the auxiliary signals, some authors have proposed novel modular topologies [5–7, 138]. Du *et al.* introduced the active cross-connected M^2C (AC-M^2C) [5] that is shown in Fig. 3.8.a where the proposed circuit is characterized by the connection of the upper and lower arms middle points through a stack of series FBSMs. The power oscillations between the capacitor of the upper and lower arm are controlled by injecting a high-frequency circulating current in the new branch. A high-frequency voltage v_h is added in the four sub-arms as shown in Fig. 3.8.b to redistribute the power between the upper and lower arm; these voltages components are defined with opposite signs in each arm to cancel their effect in the AC and DC port. In the cross-connected branch, the voltage $\Delta v_{\mathrm{arm,x}}$ produces a high frequency current $i_{\mathrm{h,x}}$ that interacts with the voltages components v_h to generate an interchange of power between the upper and lower arm. The high-frequency current and

voltage are defined as square waveforms to reduce their amplitude. The main advantage of this topology is that the maximum peak current is the same in all the arms and branches. However, its control can not follow exactly the square reference. The work of [5] aims to avoid the use of a common-mode voltage v_0. Although the proposed control system does not use explicitly v_0, the experimental results show a voltage v_0 different from zero. Moreover, this converter requires three additional arms with the same power rating and number of sub-modules as an arm of a standard M^2C, increasing the number of required sub-modules with respect to the standard M^2C.

A new modulation scheme and controller was proposed for the Flying Capacitor-M^2C (FC-M^2C) in [138]. This topology is similar to the AC-M^2C; however, instead of connecting the upper and lower arm with a stack of series half-bridges, the FC-M^2C has a flying capacitor across the middle point of the upper and lower arm. The power in each phase is balanced using this cross-connected capacitor. Nevertheless, the flying capacitor has to tolerate half of the DC-port voltage. Although the FC-MMC overcomes the zero/low-fundamental-frequency issues of conventional MMC, it suffers from high current stress on the semiconductor switches and flying capacitor [138].

The star-channel M^2C and delta channel M^2C were proposed in [6] and [7] respectively. Although these topologies reduce the voltage oscillations without the injection of common-mode voltage, both controllers inject a square waveform current in the auxiliary circuits. In the star-channel M^2C (Fig. 3.9.a), the number of modules for each star-branch is a quarter of the sub-modules in a standard arm. The delta-channel M^2C (Fig. 3.9.b) injects only 40% current in its auxiliary circuit in comparison with the AC-M^2C. Moreover, both proposed M^2C auxiliary circuits are composed exclusively of full-bridge modules, increasing the number of semiconductor components, and the delta channel branch has to be designed to support a voltage of $\frac{\sqrt{3}V_d}{4}$, V_d being the dc-port voltage.

A different approach is to control the dc-port voltage to reduce the capaci-

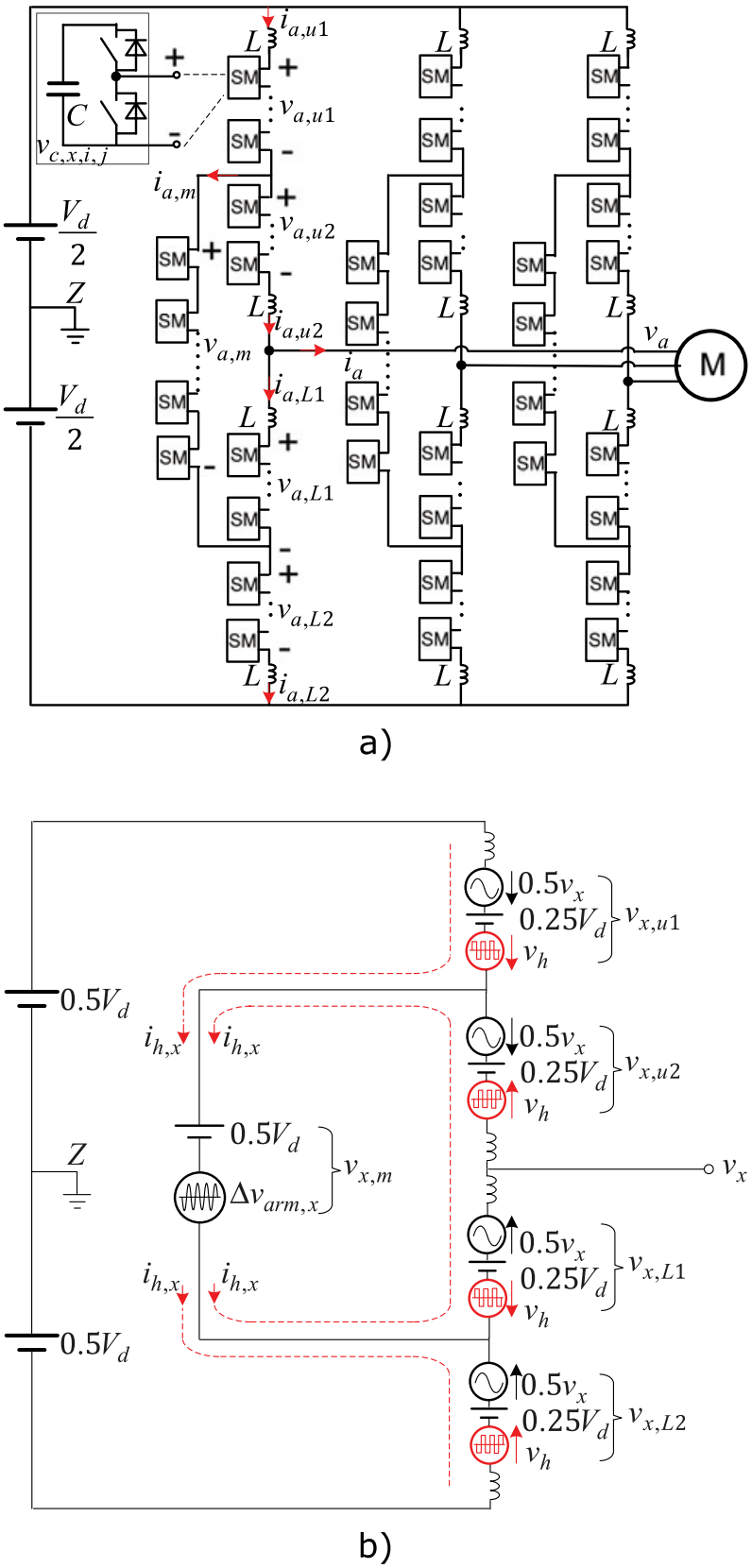


Figure 3.8: *Active cross-connected M^2C for medium-voltage motor drive [5].*

tor voltage oscillations [38–40, 139, 140]. In [38, 139], a back-to-back (BTB) FBSM-based MMC is proposed to reduce the oscillations of the floating ca-

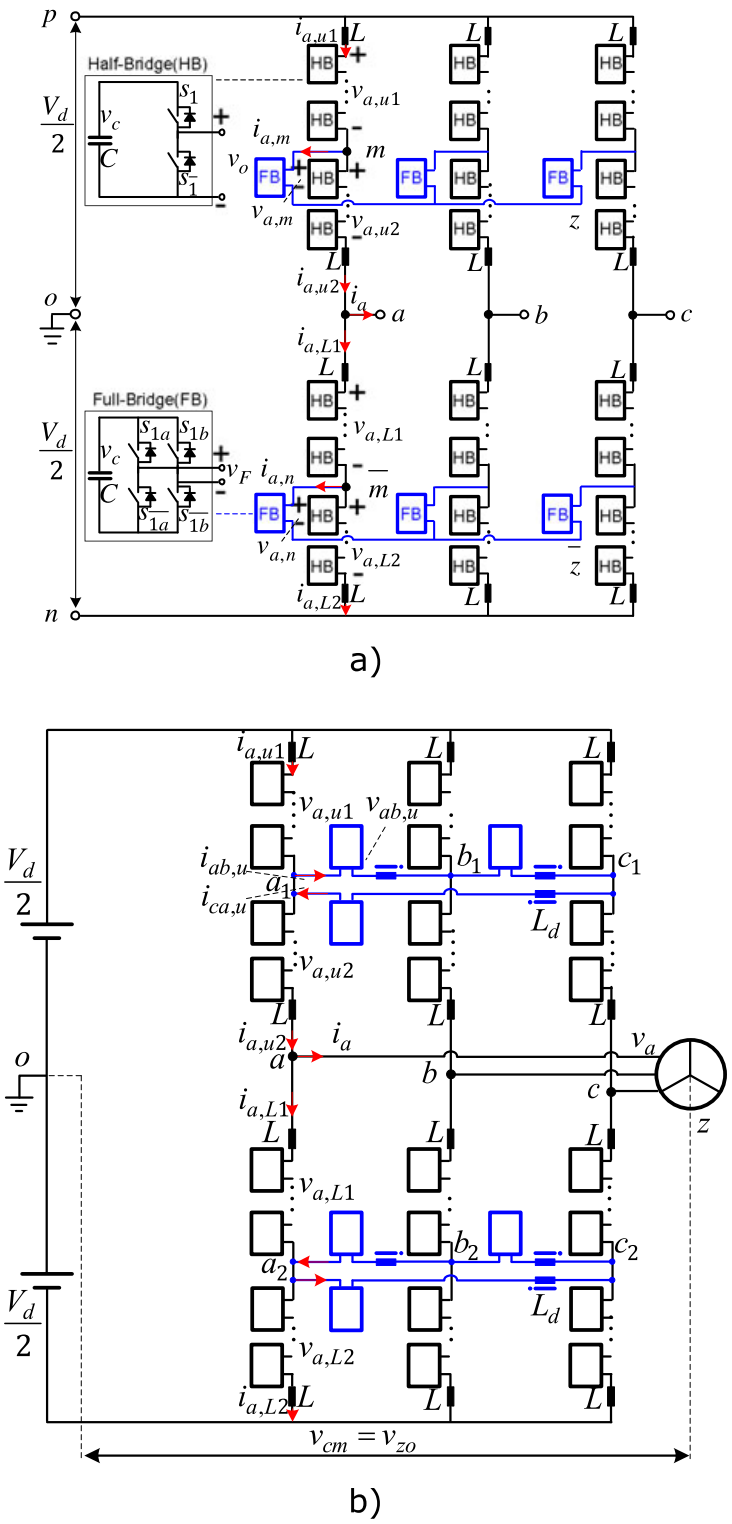


Figure 3.9: *Star-channel M^2C [6] and Delta-channel M^2C [7].*

pacitors for the whole operation range. In this case, the grid-side converter is regulated as a controllable current source that produces a constant dc-link current to feed the machine-side MMC. Although the capacitor voltage oscillations are reduced for the whole machine speed range, this solution doubles

the number of switches with respect to the standard HBSM-based MMC. In [140], the dc-port voltage is regulated using a modified 24-pulse rectifier. In this case, the dc-port voltage is controlled by changing the connection among the diode bridges belonging to the 24-pulse rectifier. However, this solution requires a multi-winding transformer that is expensive and bulky. In addition, only three discrete values of dc-link voltage can be employed in [140] (100%, 50%, and 25% of the rated dc-port voltage); therefore, the optimal value of the dc-port voltage cannot be applied for the full machine speed range.

In [39, 40], a series switch is added in the dc-link port to regulate the average value of the dc-port voltage. The series switch can modulate the dc-port voltage between its rated value and zero. However, this solution has a high value of $\frac{dV}{dt}$ in the dc-port and consequently, the EMI (electromagnetic interference) is higher than that of a standard MMC. Although in [39, 40] the injected common-mode voltage is reduced, the series switch has to withstand the full dc-port voltage, and a snubber filter needs to be added to smooth the input voltage of the drive-side MMC.

Guan *et al.* [8] proposes a hybrid M^2C converter for the grid-side while using a half-bridge based M^2C converter for the machine side as shown in Fig. 3.10. The dc-port voltage is proportional to the machine electric frequency; moreover, the machine operates under constant torque conditions, i.e., the dc current I_{dc} and the output AC current I_m are constant. However, this topology produces an asymmetrical current through the upper and lower arm, which yields an uneven distribution of losses and power requirements among the sub-modules.

Another approach was presented by Sau *et al.* [9] where the grid-side converter is a full-bridge based M^2C and the machine-side corresponds to a half-bridge based M^2C, this converter is shown in Fig. 3.11. The controlled dc-port voltage is regulated in a similar manner as in [8]. However, since the grid-side converter is composed of full-bridge modules only, the losses and semiconductor components are increased. The dc-port voltage regulation can be accomplished

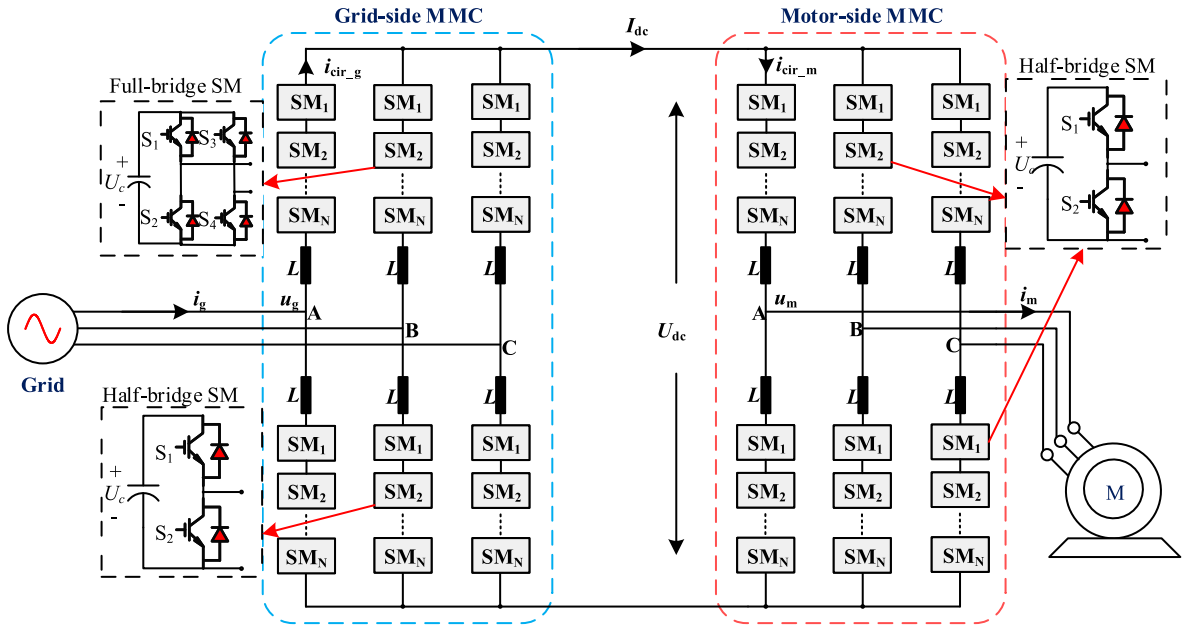


Figure 3.10: *Back-to-back hybrid modular multilevel converter [8].*

by using a combination of FBSMs and HBSMs.

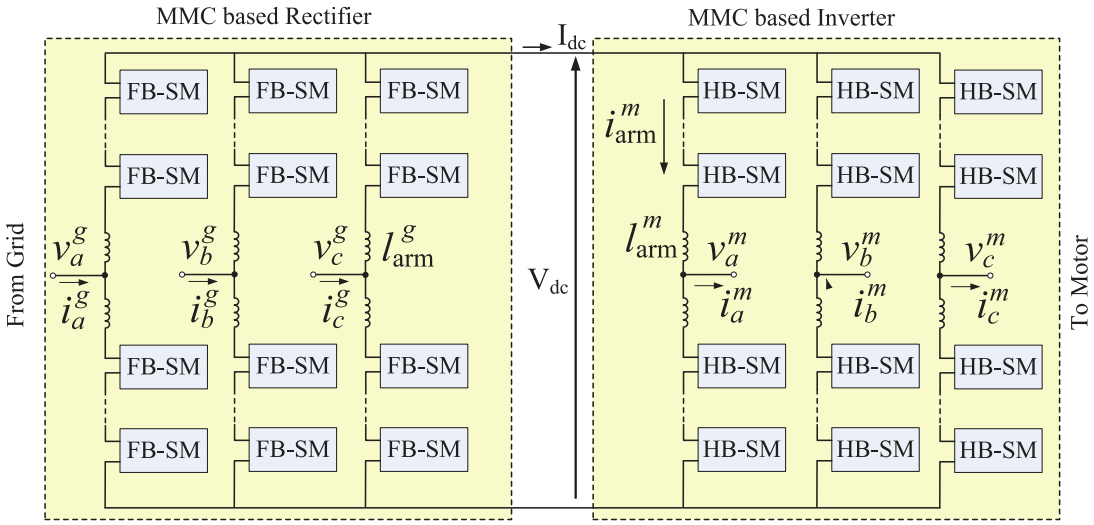


Figure 3.11: *Back-to-back hybrid modular multilevel converter [9].*

3.4.1 The Hybrid Modular Multilevel converter

The hybrid MMC, composed of both HBSMs and FBSMs, was proposed in [42]. In the event of a short-circuit in the dc-port, the FBSMs can block the grid voltage; otherwise, the sub-module free-wheeling diodes may be damaged due to the high fault currents. The hybrid MMC can operate with a dc-port

voltage lower than that achievable with an HBSM-based MMC, and it has fewer components than the FBSM-based MMC. However, when the modulation index is large ($m \geq 2$) corresponding to a low dc-port voltage, the arm currents are unipolar (e.g. always positive), and in this condition, the capacitor voltages of the HBSMs cannot be balanced [43].

The hybrid MMC is an intermediate solution between the HBSM-based MMC and the FBSM-based MMC. The HBSM-based MMC is preferred in most applications due to its lower semiconductor losses in comparison with the FBSM-based MMC. However, the FBSM-based has a broader output voltage range than that of the HBSM-based MMC, because each FBSM can output a negative voltage. For an HBSM-based MMC composed of N cells per arm and with a cell capacitor voltage reference v_C^*, the arm voltage is bounded between Nv_C^* and 0, while in a FBSM-based MMC the arm voltage is bounded between Nv_C^* and $-Nv_C^*$. In the hybrid MMC only a portion of the arm's cells are replaced by FBSMs. For a hybrid MMC composed of N_H HBSMs and N_F FBSMs, with $N=N_H+N_F$, the arm voltage is limited between Nv_C^* and $-N_F v_C^*$. One possible design solution is to reduce the proportion of FBSMs within each arm to decrease the semiconductor losses. The minimum number of FBSMs depends of each particular application, in particular, the hybrid MMC can be employed to block dc-fault conditions [141, 142], to reduce the cell capacitance in HVDC applications [143], or to produce a reduce dc-link voltage [144]. For instance, if the hybrid MMC is used for HVDC applications, the converter should be able to block dc-faults. The arm voltage v_x^y of an hybrid MMC is shown in figure 3.12, in this case M FBSMs are allowed to output a negative voltage in steady-state operation ($M \leq N_F$). As a consequence the arm voltage is limited between Nv_C^* and $-Mv_C^*$. In this case, the maximum value of the dc-link

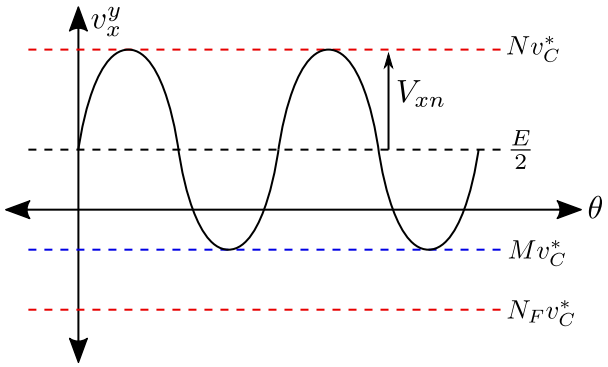


Figure 3.12: *Arm voltage of a hybrid MMC.*

voltage and the maximum phase-to-neutral voltage V_{xn} are:

$$E = (N - M)v_C^* \tag{3.10}$$

$$V_{xn} = \frac{N + M}{2} v_C^* \tag{3.11}$$

Figure 3.13 illustrates a fault-current path formed between the AC and DC sides [145]. In this case, the current provided by a grid phase will return through a different one. During the fault condition, all the FBSMs in the fault-

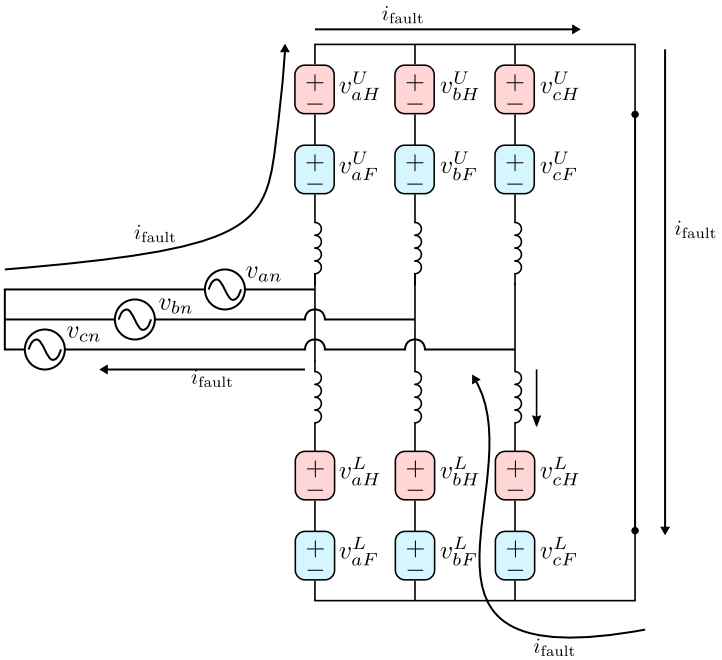


Figure 3.13: *Pole-to-pole short circuit in a hybrid MMC.*

current path are used to block the phase-to-phase grid voltage. Therefore, it is possible to derive the minimum number of FBSMs N_F required to block the

fault condition:

$$\sqrt{3}\frac{N+M}{2}v_C^* \leq 2N_F v_C^* \tag{3.12}$$

$$\frac{\sqrt{3}}{4} \leq \frac{N_F}{N+M} \tag{3.13}$$

A different criterion to choose the number of FBSMs and HBSMs is to reduce the cell capacitance. The reduction of the cell capacitance is a critical design goal to decrease the sub-module volume and cost. In [143], the optimal modulation index is derived to reduce the arm energy fluctuation. Then, the number of FBSMs that are required in steady-state can be calculated as a function of this optimal modulation index. Finally, in some applications the hybrid MMC is design to have a variable dc-link voltage in a wide range [144]. In this case, the number of FBSMs and HBSMs is calculated to output the minimum dc-link voltage.

Some control strategies have been proposed to compensate for the capacitor voltage imbalance between the HBSMs and FBSMs in a hybrid MMC. In [42], balancing is accomplished by forcing a polarity change in the arm current by reducing the power factor at the grid-side and increasing the magnitude of the ac component. In [146], the capacitor voltage balancing is realised by injecting a circulating current; however, [146] does not present explicit expressions to calculate the magnitude of the required current. Moreover, the magnitude of the required circulating currents is calculated offline, assuming that the MMC and grid parameters are constant.

A modified sorting modulation scheme was introduced in [34] to operate a hybrid MMC with a higher modulation index. In this case, a PI controller regulates the energy exchange between the HBSMs and FBSMs by changing the order in which the modulation scheme inserts the sub-modules. Although this method is more efficient than others proposed in the literature, it does not guarantee the change of polarity in the arm current required to balance the HBSMs at every possible operating point.

Some authors have proposed the use of circulating current to ensure the local balance in a hybrid MMC during over-modulation [34, 42, 146, 147]. The main drawback of these methods is that the feed-forward circulating currents are calculated off-line. Thus, the circulating currents are imposed without considering the degree of imbalance between the capacitor voltages of the FBSMs and HBSMs, i.e., there is no closed-loop control of the FBSM-HBSM capacitor voltage imbalance. Moreover, the controller cannot compensate for changes in the operating point and/or variations in the parameters of the hybrid MMC. Consequently, the off-line calculated feed-forward currents may not be totally effective in dealing with the imbalance between FBSMs and HBSMs in a hybrid MMC.

3.5 Summary

Classical multilevel converters have several disadvantages in medium-voltage applications. To increase the number of levels of a NPC converter over 3, it is necessary to add a balancing circuits to ensure the proper regulation of the floating capacitors. The flying capacitor converter has some industrial applications; however, its main disadvantages are the size of the floating capacitors and the required high switching frequency. Finally, the cascaded H-bridge converter needs to provide an isolated power supply to each H-bridge. Feeding each H-bridge through a multi-winding transformer is the standard solution, but such a transformer is expensive and bulky. The drawbacks discussed above explain the necessity of developing novel and better multilevel converters; particularly, modularity is a crucial aspect to consider.

Then, the family of modern multilevel converters is introduced. The MMC comprises several small converters (sub-modules) that work together; consequently, the MMC can withstand high-voltage using standard semiconductor switches. Several authors have worked in MMC-based drive applications because it is a promising solution for medium-voltage traction applications. How-

ever, the MMC presents high-voltage capacitor voltage oscillations while the machine operates at a reduced speed. The literature review concludes that for drive applications, the back-to-back MMC requires the minimum power rating devices compared to the M^3C and the Hexverter.

In a back-to-back MMC-based drive converter, the capacitor voltage on the machine-side MMC can be reduced by controlling the value of the dc-link voltage. Although some solutions have been presented, they have some practical drawbacks. An alternative is to use an hybrid MMC as a front-end converter to regulate the dc-link voltage. Some control strategies to ensure the local balance between the FBSMs and HBSMs in a hybrid MMC working in overmodulation has been presented. However, no simple expressions to calculate the minimum compensating currents are derived.

In the following chapters, the model and sizing of a modular multilevel converter are presented. Then, two strategies to ensure the local balance of a hybrid MMC are presented. In addition, a closed-loop controller is also proposed to compensate for any mismatch between the theoretical model used in the control platform and the actual system. Finally, this thesis explores the use of the hybrid MMC to regulate the dc-link voltage of an MMC-based drive converter. In this case, it is possible to regulate the dc-link voltage continuously rather than imposing a finite number of values. The optimal value of the dc-link voltage is derived as a function of the machine operational point.

Chapter 4

Modelling and sizing of the Modular Multilevel Converter

4.1 Introduction

This thesis considered two different MMC-based systems. Firstly, an individual hybrid MMC and secondly a back-to-back MMC-based drive converter. As explained in chapter 2 and 3, there are conditions in which working with a suppressed dc-link voltage has advantages in MMC-based applications. For instance, in HVDC transmission systems, it is a common practice to reduce its dc-link voltage during bad weather conditions to avoid short-circuits. In addition, in a back-to-back MMC drive converter, it is possible to reduce the common-mode voltage injected into the machine stator by reducing the dc-link voltage during low-mechanical speed. In drive applications, the grid-side converter is a hybrid MMC, while the machine-side converter is an HBSM-based MMC. The single hybrid MMC and the back-to-back hybrid MMC drive applications are shown in figure 4.1 and 4.2 respectively.

This chapter discusses the modelling of the MMC. Firstly, a dynamic model is derived, which is needed as the basis for energy management control. A transformation of the basic equations is introduced, which removes coupling and eases control design. The converter model is expressed in the $\Sigma\Delta\alpha\beta 0$ ref-

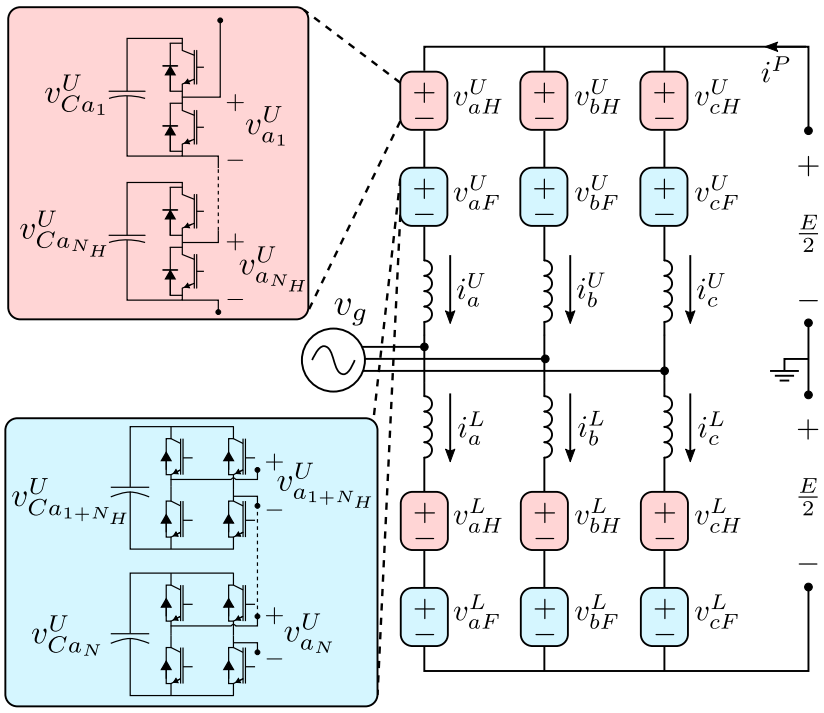


Figure 4.1: *Circuit diagram of the hybrid MMC.*

erence frame. Previous work in the literature usually consider the per-phase model of the MMC. However, when working with the natural reference frame, it is not easy to identify the effect of each current sequence component on the capacitor voltage balance. The MMC model can be used for the hybrid MMC and the HBSM-based MMC as well. Some issues specific to the hybrid converter regarding the inherent unbalancing of the capacitor energies are introduced, and their origins are explained. Finally, steady-state modelling of the MMC is undertaken to allow basic design and component sizing. The differences between the requirements for the grid and machine side converters are discussed, particularly in terms of capacitor voltage ripple and cell capacitor sizing.

4.2 Model of the MMC

This section presents a general model for the MMC. The MMC consists of six arms as depicted in Fig. 4.3. Each arm is composed of the cascade connection of N sub-modules and an inductor L. Notice that the hybrid MMC has the

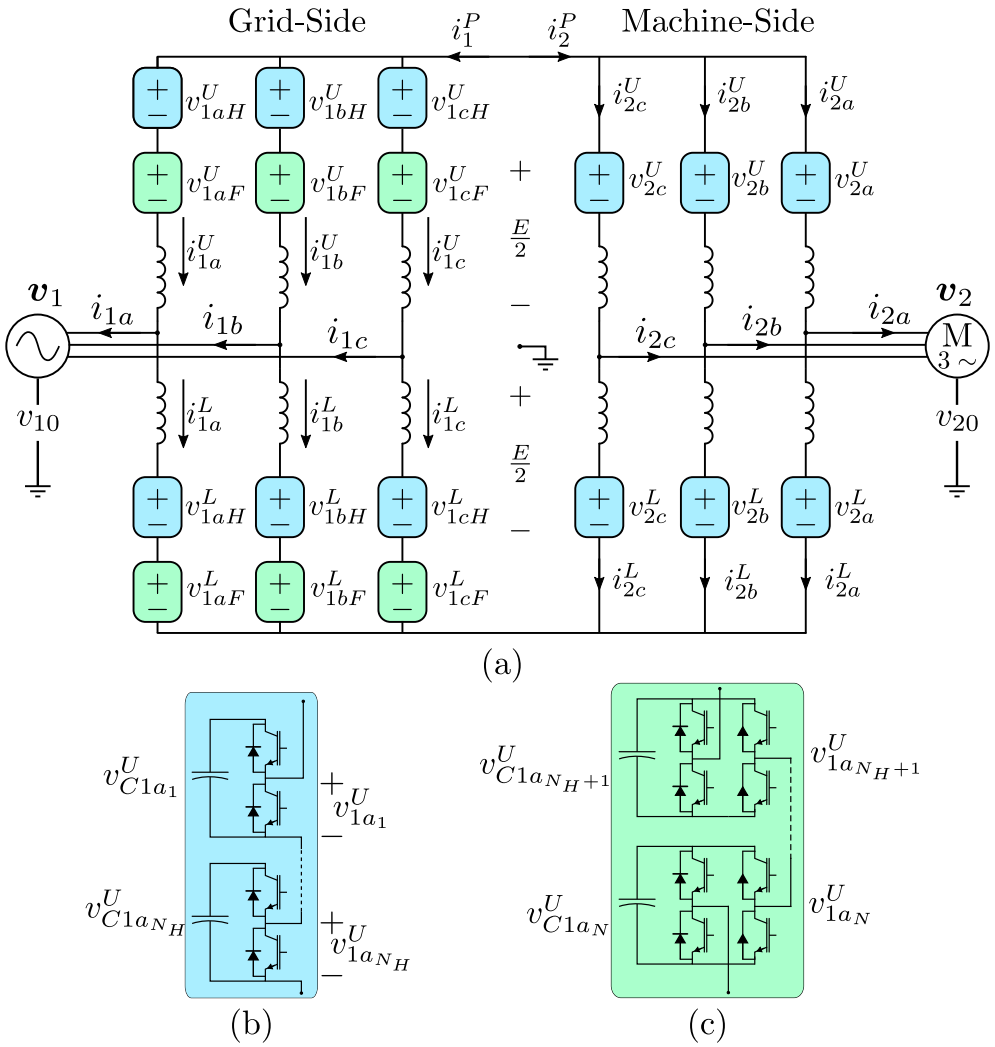


Figure 4.2: *Model of the hybrid BTB MMC for drive applications (a), cluster of HBSMs (b) and cluster of FBSMs (c).*

same structure, but each arm is composed of N_H HBSMs and N_F FBSMs as shown in Fig. 4.1.

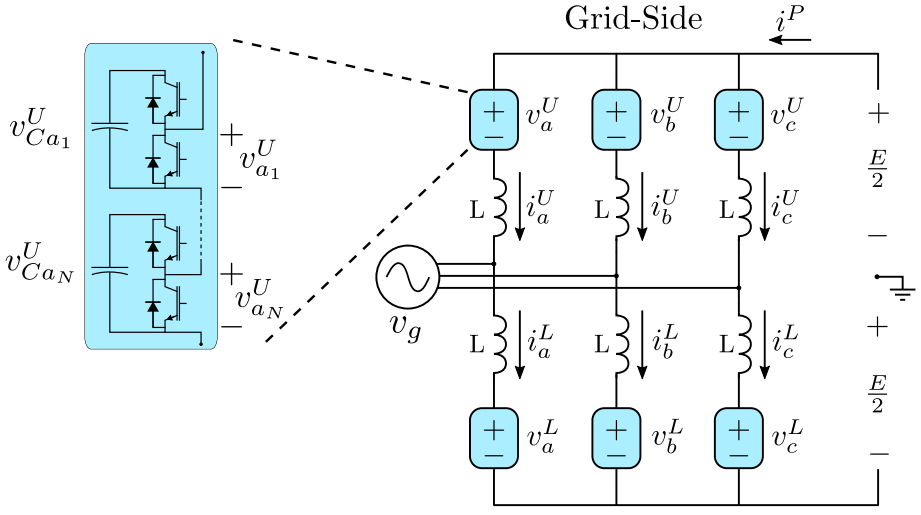


Figure 4.3: *Circuit diagram of a general MMC.*

For the MMC shown in Fig. 4.3, each output phase $x \in \{a, b, c\}$ is connected to an upper (U) and lower (L) arm designated as $y \in \{U, L\}$ respectively. The voltage modulated by each arm v_x^y is given in (4.1), where $S_{xHi}^y \in \{0, 1\}$ are the switching states for the HBSMs, and $v_{Cx_i}^y$ is the capacitor voltage of the i_{th} cell of phase x and arm y.

$$v_x^y = \sum_{i=1}^{N} v_{Cx_i}^y S_{xHi}^y \tag{4.1}$$

For the hybrid MMC, the arm voltage is given in eq. (4.2), where $S_{xFi}^y \in \{-1, 0, 1\}$ are the switching states for the FBSMs. The main difference is that the FBSMs can output a negative voltage while the HBSMs can only output zero or positive values.

$$v_x^y = v_{xH}^y + v_{xF}^y = \sum_{i=1}^{N_H} v_{Cx_i}^y S_{xHi}^y + \sum_{i=N_H+1}^{N} v_{Cx_i}^y S_{xFi}^y \tag{4.2}$$

The voltage-current relationships of the MMC are shown in (4.3) using natural coordinates, where E is the dc-port voltage, v_x^y and i_x^y are the arm voltages and currents respectively, and v_x is the grid voltage.

$$\frac{E}{2}\begin{pmatrix} 1 & 1 & 1 \\ 1 & 1 & 1 \end{pmatrix} = \begin{pmatrix} v_a^U & v_b^U & v_c^U \\ v_a^L & v_b^L & v_c^L \end{pmatrix} + \begin{pmatrix} v_a & v_b & v_c \\ -v_a & -v_b & -v_c \end{pmatrix} + L\frac{d}{dt}\begin{pmatrix} i_a^U & i_b^U & i_c^U \\ i_a^L & i_b^L & i_c^L \end{pmatrix} \tag{4.3}$$

Notice that in (4.3) the Thevenin inductance of the grid is considered negligible. It is not straightforward to independently control the outer and inner converter variables in this reference frame, because the variables in (4.3) are coupled. To overcome this problem, some authors have proposed the use of the $\Sigma\Delta\alpha\beta 0$ linear transformation [115, 116]. Given a matrix in the natural coordinates

X_{abc}^{UL}, its $\Sigma\Delta\alpha\beta 0$ transformation is obtained by pre-multiplying it by $T_{\Sigma\Delta}$ and post-multiplying it by $T_{\alpha\beta 0}$. For instance, the arm voltage $V_{\alpha\beta 0}^{\Sigma\Delta}$ is calculated as:

$$\underbrace{\begin{pmatrix} v_\alpha^\Sigma & v_\beta^\Sigma & v_0^\Sigma \\ v_\alpha^\Delta & v_\beta^\Delta & v_0^\Delta \end{pmatrix}}_{V_{\alpha\beta 0}^{\Sigma\Delta}} = T_{\Sigma\Delta} \underbrace{\begin{pmatrix} v_a^U & v_b^U & v_c^U \\ v_a^L & v_b^L & v_c^L \end{pmatrix}}_{V_{abc}^{UL}} T_{\alpha\beta 0} \tag{4.4}$$

Where the matrices $T_{\Sigma\Delta}$ and $T_{\alpha\beta 0}$ are defined by:

$$T_{\Sigma\Delta} = \frac{1}{2}\begin{pmatrix} 1 & 1 \\ 2 & -2 \end{pmatrix} \qquad T_{\alpha\beta 0} = \frac{1}{3}\begin{pmatrix} 2 & 0 & 1 \\ -1 & \sqrt{3} & 1 \\ -1 & -\sqrt{3} & 1 \end{pmatrix} \tag{4.5}$$

Analysing (4.4)-(4.5) can be concluded that the superscript Σ stands for terms that are proportional to the addition of the voltages synthesised by the upper and lower arm (see (4.4)). On the other hand, the superscript Δ stands for the terms which are proportional to the subtraction of the voltages synthesised by the upper and lower arms (see (4.4)). The subscripts α, β and 0 have the meanings conventionally associate with the Clarke transform [91, 115, 116]. Applying the $\Sigma\Delta\alpha\beta 0$ transformation to (4.3), the following decoupled model is obtained:

$$\frac{E}{2}\begin{pmatrix} 0 & 0 & 1 \\ 0 & 0 & 0 \end{pmatrix} = \begin{pmatrix} v_\alpha^\Sigma & v_\beta^\Sigma & v_0^\Sigma \\ v_\alpha^\Delta & v_\beta^\Delta & v_0^\Delta \end{pmatrix} + 2\begin{pmatrix} 0 & 0 & 0 \\ v_\alpha & v_\beta & v_0 \end{pmatrix} + L\frac{d}{dt}\begin{pmatrix} i_\alpha^\Sigma & i_\beta^\Sigma & \frac{1}{3}i^P \\ i_\alpha & i_\beta & 0 \end{pmatrix} \tag{4.6}$$

where instead of using the 6 arm currents i_x^y in natural coordinates, they are expressed in the $\Sigma\Delta\alpha\beta 0$ reference frame as the dc-port current i^P, the ac-port currents $\boldsymbol{i}_{\alpha\beta}$,which are the $\alpha-\beta$ components of the grid-current for the circuit depicted in Fig. 4.1, and the circulating currents $\boldsymbol{i}_{\alpha\beta}^\Sigma$ (internal to the converter).

According to (4.6), i^P, $\boldsymbol{i}_{\alpha\beta}$, and $\boldsymbol{i}^{\Sigma}_{\alpha\beta}$ can be controlled independently by the arm voltage terms v^{Σ}_0, $\boldsymbol{v}^{\Delta}_{\alpha\beta}$, and $\boldsymbol{v}^{\Sigma}_{\alpha\beta}$ respectively. Throughout this thesis, bold fonts are used to denote vectors. By regulating the arm voltage v^y_x it is possible to regulate the converter output voltage and currents. However, unlike the CHB converter, each cell in a standard or hybrid MMC is not fed by an external isolated power supply; on the contrary, each cell is connected to a floating capacitor, as shown in Fig. 4.1. Consequently, it is necessary to regulate the arm energy balance and the individual capacitor voltage within the MMC. In the following section, an energy-power model of the MMC is presented to provide the basis for developing capacitor voltage control strategies in Chapter 5.

4.2.1 Overall Approach to Energy Management of the MMC

Energy management of the MMC has been addressed in several publications [116, 120]. In this thesis, the energy storage of the six arms is indirectly regulated by controlling the total capacitor voltage of each arm:

$$v^y_{Cx} = \sum_{i=1}^{N} v^y_{Cxi} \qquad x \in \{a,b,c\}, y \in \{U,L\} \tag{4.7}$$

To regulate the total capacitor voltage v^y_{Cx} with $x{\in}\{a,b,c\}$ and $y{\in}\{U,L\}$, the instantaneous power of each arm P^{UP}_{abc} is controlled:

$$\underbrace{\frac{d}{dt}\begin{pmatrix} v^U_{Ca} & v^U_{Cb} & v^U_{Cc} \\ v^L_{Ca} & v^L_{Cb} & v^L_{Cc} \end{pmatrix}}_{V^{UL}_{Cabc}} \approx \frac{1}{Cv^*_C} \underbrace{\begin{pmatrix} p^U_a & p^U_b & p^U_c \\ p^L_a & p^L_b & p^L_c \end{pmatrix}}_{P^{UL}_{abc}} \tag{4.8}$$

where the instantaneous power of each arm is $p^y_x{=}i^y_x v^y_x$ $x{\in}\{a,b,c\}$ and $y{\in}\{U,L\}$, C is the cell capacitance, and v^*_C is the capacitor voltage reference of each sub-module. In eq. 4.8, it is assumed that the capacitor voltages present a small

ripple and its value is close to the capacitor voltage reference v_C^*. By expressing the converter power in the $\Sigma\Delta\alpha\beta 0$ reference frame, i.e. by pre-multiplying (4.8) by $T_{\Sigma\Delta}$ and post-multiplying by $T_{\alpha\beta 0}$ [see (4.4)-(4.5)], it is relatively simple to identify which current components can be used to balance the energy among the six arms:

$$\underbrace{\frac{d}{dt}\begin{pmatrix} v_{C\alpha}^{\Sigma} & v_{C\beta}^{\Sigma} & v_{C0}^{\Sigma} \\ v_{C\alpha}^{\Delta} & v_{C\beta}^{\Delta} & v_{C0}^{\Delta} \end{pmatrix}}_{V_{C\alpha\beta 0}^{\Sigma\Delta}} \approx \frac{1}{Cv_C^*} \underbrace{\begin{pmatrix} p_{\alpha}^{\Sigma} & p_{\beta}^{\Sigma} & p_{0}^{\Sigma} \\ p_{\alpha}^{\Delta} & p_{\beta}^{\Delta} & p_{0}^{\Delta} \end{pmatrix}}_{P_{\alpha\beta 0}^{\Sigma\Delta}} \tag{4.9}$$

If the energy is completely balanced in the MMC, then the six capacitor voltages in the matrix located at the left-hand side of (4.8) are identical (i.e. $v_{Ca}^U{=}v_{Ca}^L{=}v_{Cb}^U{=}\cdots{=}v_{Cc}^L{=}Nv_C^*$). Considering this and applying $T_{\Sigma\Delta}$ and $T_{\alpha\beta 0}$, it is straightforward to conclude that in a balanced converter the total capacitor voltages in the $\Sigma\Delta\alpha\beta 0$ reference frame are $v_{C\alpha}^{\Sigma}{=}v_{C\beta}^{\Sigma}{=}0$, $v_{C\alpha}^{\Delta}{=}v_{C\beta}^{\Delta}{=}0$, $v_{C0}^{\Delta}{=}0$, and $v_{C0}^{\Sigma}{=}Nv_C^*$. The capacitor voltage v_{C0}^{Σ} is related to the total energy stored in the converter and has to be regulated to a nonzero value, while the remaining 5 voltage terms regulate the balance among the converter arms. It can be shown that the power terms $P_{\alpha\beta 0}^{\Sigma\Delta}$ can be obtained as (see [115, 116]):

$$p_0^{\Sigma} = \frac{Ei^P}{6} - \frac{1}{4}\Re\{\boldsymbol{v}_{\alpha\beta}\boldsymbol{i}_{\alpha\beta}^c\} \tag{4.10}$$

$$\boldsymbol{p}_{\alpha\beta}^{\Sigma} = -\frac{1}{4}(\boldsymbol{v}_{\alpha\beta}\boldsymbol{i}_{\alpha\beta})^c + \frac{E}{2}\boldsymbol{i}_{\alpha\beta}^{\Sigma} - \frac{1}{2}v_0\boldsymbol{i}_{\alpha\beta} \tag{4.11}$$

$$\boldsymbol{p}_{\alpha\beta}^{\Delta} = -(\boldsymbol{v}_{\alpha\beta}\boldsymbol{i}_{\alpha\beta}^{\Sigma})^c + \frac{E\boldsymbol{i}_{\alpha\beta}}{2} - \frac{2}{3}i^P\boldsymbol{v}_{\alpha\beta} - 2v_0\boldsymbol{i}_{\alpha\beta}^{\Sigma} \tag{4.12}$$

$$p_0^{\Delta} = -\Re\{\boldsymbol{v}_{\alpha\beta}(\boldsymbol{i}_{\alpha\beta}^{\Sigma})^c\} - \frac{2}{3}i^P v_0 \tag{4.13}$$

where $\Re$ and $(\cdot)^c$ are the real part and complex conjugate operators respectively. The power terms $P_{\alpha\beta 0}^{\Sigma\Delta}$ are derived in Appendix A. In the power equations (4.10)-(4.13) the complex numbers are expressed as vectors to simplify their representation. For instance, the power vector $\boldsymbol{p}_{\alpha\beta}^{\Sigma}$ is defined to group the power terms p_{α}^{Σ} and p_{β}^{Σ}, in particular, $\boldsymbol{p}_{\alpha\beta}^{\Sigma}{=}p_{\alpha}^{\Sigma} + jp_{\beta}^{\Sigma}$. The power vec-

tors $\boldsymbol{p}^{\Sigma}_{\alpha\beta}$ and $\boldsymbol{p}^{\Delta}_{\alpha\beta}$ do not have the same physical interpretation of the complex power. In this thesis the vector notation was chosen to have more compact expressions for the arm power equations (4.10)-(4.13). The power term p^{Σ}_{0} is proportional to the difference between the ac power and the dc power of the MMC. The power terms $\boldsymbol{p}^{\Delta}_{\alpha\beta}$ and p^{Δ}_{0} represent the power difference between the upper and lower arms while the power terms $\boldsymbol{p}^{\Sigma}_{\alpha\beta}$ represent the power flow between the converter phases [115, 116]. Therefore, to regulate all the capacitor voltages $V^{\Sigma\Delta}_{C\alpha\beta0}$, different components of the circulating current $\boldsymbol{i}^{\Sigma}_{\alpha\beta}$ along with the dc port current are used. By inspecting the power terms $P^{\Sigma\Delta}_{\alpha\beta0}$ it is straightforward to choose current components (orthogonal between them) to produce controllable dc-power terms, to regulate $V^{\Sigma\Delta}_{C\alpha\beta0}$ of (4.9). The circulating current utilised in this thesis is shown in (4.14) where $\theta = \int \omega_g dt$ is the grid voltage angle and the grid voltage is $\boldsymbol{v}_{\alpha\beta} = V_g e^{j\theta}$.

$$\boldsymbol{i}^{\Sigma}_{\alpha\beta} = \overline{\boldsymbol{i}^{\Sigma}_{\alpha\beta}} + \boldsymbol{i}^{\Sigma+}_{dq}\mathrm{e}^{j\theta} + \boldsymbol{i}^{\Sigma-}_{dq}\mathrm{e}^{-j\theta} \tag{4.14}$$

To regulate the energy balance among the 6 arms, three balancing actions are considered[115]:

1. Total energy control: The power term p^{Σ}_{0} regulates the total energy stored in the converter. In this case, the current i^{P} is used to regulate p^{Σ}_{0} (4.10).

2. Vertical balance: To balance the energy between the upper and lower arms, the power terms $\boldsymbol{p}^{\Delta}_{\alpha\beta}$ and p^{Δ}_{0} are controlled. By replacing the circulating current $\boldsymbol{i}^{\Sigma}_{\alpha\beta}$ (4.14) in the power term $\boldsymbol{p}^{\Delta}_{\alpha\beta}$ (4.12) it can be noticed that only the negative sequence component $\boldsymbol{i}^{\Sigma-}_{dq}e^{-j\theta}$ produces a manipulable dc power term with the grid voltage $\boldsymbol{v}_{\alpha\beta} = V_g e^{j\theta}$, in this case, the controllable power term is $V_g \boldsymbol{i}^{\Sigma-}_{dq}$. Analogously, the positive sequence current component $i^{\Sigma+}_{d}$ produces a manipulable power term in p^{Δ}_{0} (4.13).

3. Horizontal balance: To balance the arm energy between all phases, the power term $\boldsymbol{p}^{\Sigma}_{\alpha\beta}$ is used. In this case, the second term of (4.11) is con-

trolled using the component $\overline{\boldsymbol{i}_{\alpha\beta}^{\Sigma}}$ of the circulating current (see (4.14)).

4.3 Balance between the HBSMs and FBSMs during low dc-port voltage

The capacitor voltage imbalance problems produced in a hybrid MMC operating with a high modulation index m have already been reported in [30, 43, 146, 147]. When a hybrid MMC operates with a reduced dc-port voltage E, the arm currents can become unipolar, i.e. the arm currents will not have zero crossing points. If this condition is not corrected, the capacitor voltages of the HBSMs and FBSMs will diverge continuously. Considering phase a for example, the same result holds for the other phases.

$$i_a^U = \frac{1}{2}i_a + \frac{i^P}{3} \qquad i_a^L = -\frac{1}{2}i_a + \frac{i^P}{3} \tag{4.15}$$

which, if the losses are neglected yields:

$$Ei^P = \frac{3}{2}V_g I_g \cos(\varphi) \tag{4.16}$$

where V_g and I_g stand for the moduli of the grid voltage and current respectively, and φ is the grid power factor angle. By defining the modulation index as $m{=}2V_g/E$ and by replacing (4.16) into (4.15), the arm currents i_a^U and i_a^L are calculated as:

$$i_a^U = \frac{1}{2}I_g\left(\cos(\omega_g t + \varphi) + \frac{m}{2}\cos(\varphi)\right) \tag{4.17}$$

$$i_a^L = -\frac{1}{2}I_g\left(\cos(\omega_g t + \varphi) - \frac{m}{2}\cos(\varphi)\right) \tag{4.18}$$

From (4.17)-(4.18), if the reactive current is zero (i.e. $\varphi{=}0$), the arm currents become unipolar for $m{>}2$. Considering that the voltage synthesised by the half-bridge power cells is also unipolar, it is simple to conclude that, when the

arm current is also unipolar, the HBSM power flow is unidirectional and the HBSM capacitors charge (or discharge) continuously each time the half-bridges synthesise a non-zero voltage.

Capacitor voltage imbalance between the HBSMs and FBSMs, due to the effect of unipolar arm current, is depicted in Fig. 4.4. In this case, a hybrid MMC, with N_F/N_H=0.5, feeds a constant load p_L=0.5 pu at the dc-port and the dc-port voltage is reduced down to 40% of its rated value (m reaching a value of 2.5).

As shown in Fig. 4.4(a), when the modulation index $m > 2$, the HBSM capacitor voltages discharge to zero while the FBSMs increase their capacitor voltages. In addition, Fig 4.4(b)-(d) show an amplified view (between t=0.9s to t=1.4s) of the capacitor voltages (b), and the arm voltage and current of phase a (c), and the modulation index m (d). Notice from Fig. 4.4(c) that after t=1.1s the current (in green) does not becomes positive again. If the capacitor voltage imbalance is not corrected, the over-voltage cell protection will eventually disconnect the MMC from the utility grid. In Fig 4.4(b), the capacitor voltage oscillations of the FBSMs are higher than that of the HBSMs, the main reason is as the modulation index is increased, the HBSMs remain bypassed for a bigger proportion of the fundamental period.

4.4 Steady state modelling of the MMC for design and sizing

Previously, a decoupled model of the MMC was explained. In this section, the main parameters of the MMC are designed, such as cell voltage, number of cells, cell capacitance, among others. For this analysis, it is assumed that the converter is working in a steady-state operation. The differences between the requirements for the grid and machine side converters are discussed, particularly in terms of capacitor voltage ripple and cell capacitor sizing.

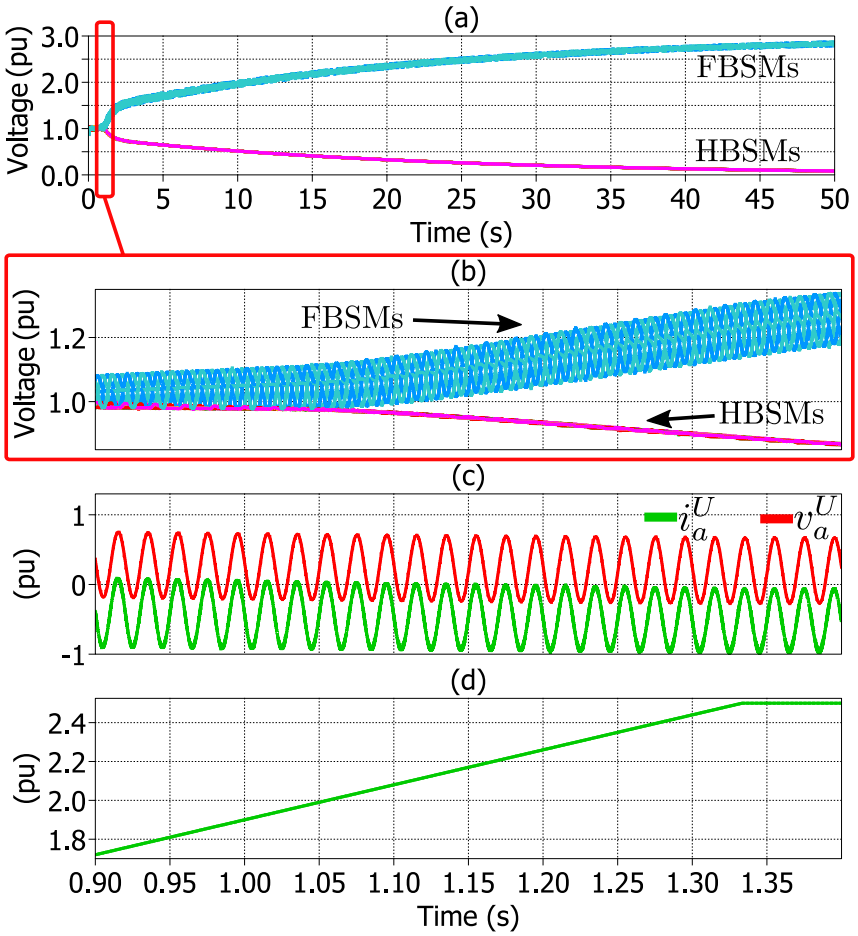


Figure 4.4: *Imbalance between HBSMs and FBSMs. (a) cell capacitor voltages, (b) zoom of capacitor voltages t=0.9→1.4 s, (c) arm current i_a^U (green) and arm voltage v_a^U (red), and (d) modulation index m.*

The main parameters of a modular multilevel converter are its cell capacitance C, arm inductor L, number of cells per arm N, and cell capacitor voltage reference v_C^*. Even though both converter sides of the back-to-back MMC are based on the modular multilevel converter, the parameter design optimisation process is different for both sides because the grid and machine do not operate at the same electrical frequency. In the machine-side converter, the arm energy has large energy oscillations during low mechanical speed. Conversely, the grid-side converter has a fixed frequency (50 or 60 Hz); consequently, the cell capacitors are chosen considering this operational point.

A critical component in an MMC application is its cell capacitance. Ideally, the voltage oscillations should be kept as reduced as possible for several reasons: (i) the voltage difference between the dc-bus voltage and the total voltage

across the upper and lower arms of any phase introduces circulating currents, that reduce the converter efficiency [148]; (ii) if the capacitor voltage oscillations are considerable, the MMC may not have enough voltage margin to modulate the output voltage, in this scenario the converter voltage harmonic distortion is increased; (iii) high voltage oscillation will reduce the lifespan of the cell capacitors, and finally (iv) for drive applications the capacitor voltage oscillations are inversely proportional to the machine speed. Therefore, it is necessary to choose the capacitance to limit these oscillations carefully; otherwise, the converter may become unstable. Although choosing a high cell capacitance value can reduce the voltage oscillations, it will increase the size and cost of the converter. Thus, there is a trade-off in the selection of the cell capacitance, in which the objective is to choose a reduced cell capacitance while having a reduced voltage ripple and a stable response. Considering the different output frequencies of the machine and grid sides MMC, the process to optimal choosing the cell capacitance is different.

4.4.1 Hybrid MMC case (grid-side converter)

The main parameters of the hybrid MMC are discussed, such as the cell capacitance, number of HBSMs and FBSMs, and voltage levels.

Cell capacitance

Although the hybrid MMC and the HBSM-based MMC shared a similar structure, their energy arm oscillations are different, i.e. a different methodology should be considered to choose the cell capacitance in the hybrid MMC. When the hybrid MMC operates with a modulation index lower than 2, it behaves as an HBSM-based MMC. However, when the hybrid MMC operates in overmodulation, the HBSMs and FBSMs within each arm no longer have the same charging/discharging process. In this case, the voltage oscillations are dominated by the energy variation between the FBSMs and the HBSMs. In partic-

ular, while the arm voltage reference is negative, the HBSMs remain bypassed, and the FBSMs produce the required voltage; if the converter losses are neglected, the HBSM sub-module capacitor voltages do not change during this interval. The net energy gained by the FBSMs, while the HBSMs are bypassed, is calculated by integrating the arm power while the voltage reference is negative:

$$\Delta W_{FB} = \int_{t_{v1}}^{t_{v2}} p_x^y(t)dt = \frac{i_d E(m^2-1)}{4\omega_g m} \qquad \forall \quad x\in\{a,b,c\}, y\in\{U,L\} \tag{4.19}$$

Where t_{v1} and t_{v2} are the zero crossing points of the arm voltage considered. In this case, the energy variation is shared evenly among the FBSMs within each arm:

$$\Delta W_{FB} = \frac{N_F C}{2}(V_{Cmax}^2 - V_{Cmin}^2) \tag{4.20}$$

By approximating the mean value between V_{Cmax} and V_{Cmin} by the cell reference voltage v_C.

$$\Delta W_{FB} \approx N_F C v_C^* \Delta V_{C1} \tag{4.21}$$

And finally, by equating the both expressions for the FBSMs energy variation (4.19)-(4.21), the sub-module voltage ripple can be expressed as:

$$C = \frac{i_d E(m^2-1)}{4N_F v_C^* \Delta V_{C1} \omega_g m} \tag{4.22}$$

From (4.22), the required cell capacitance for the hybrid MMC can be calculated.

Number of cells and voltage levels

The number of cells will affect several aspects of the MMC, such as the arm current ripple, the cell capacitor voltage ripple, and the semiconductor losses. In a hybrid MMC, it is also necessary to calculate the hybridisation ratio, i.e., the number of FBSMs (N_F) and HBSMs (N_H) per arm. The number of sub-modules is a function of the maximum and minimum arm voltage. From the voltage model of the hybrid MMC, the maximum and minimum v_x^y are calculated as:

$$v_{x\max}^y = \frac{E}{2} + V_1 = V_1\left(\frac{1}{m} + 1\right) \tag{4.23}$$

$$v_{x\min}^y = \frac{E}{2} - V_1 = V_1\left(\frac{1}{m} - 1\right) \tag{4.24}$$

The minimum capacitor voltage reference $v_{C\,\min}^*$ will be a function of the maximum arm voltage and the number of cells.

$$v_{C\,\min}^* = \frac{V_1}{N}\left(\frac{1}{m} + 1\right) \tag{4.25}$$

Once the total number of cells has been calculated, the minimum number of FBSMs is calculated by considering the minimum negative voltage that each arm has to modulate. As explained before, the minimum $v_{x\,\min}^y$ depends on the magnitude of the AC output voltage of the hybrid MMC and its maximum modulation index m, thus the minimum N_F is:

$$N_F = \left\lceil \frac{V_1}{v_{C\,\min}^*}\left(\frac{1}{m} - 1\right)\right\rceil \tag{4.26}$$

4.4.2 HBSM-based MMC case (machine-side converter)

The main parameters of the HBSM-based MMC are discussed below, in particular the cell capacitance and the number of cells per arm.

Cell capacitance

For the machine-side MMC, it is considered that there is a local controller associated with each arm that drives the mean voltage of all capacitors in the arm to be equal [116]. Accordingly, it is assumed that all capacitors have the same charging/discharging characteristic per arm for the analysis. The capacitor voltage oscillations are calculated considering phase a, which is shown in Fig. 4.5, the same analysis can be done for the remaining phases.

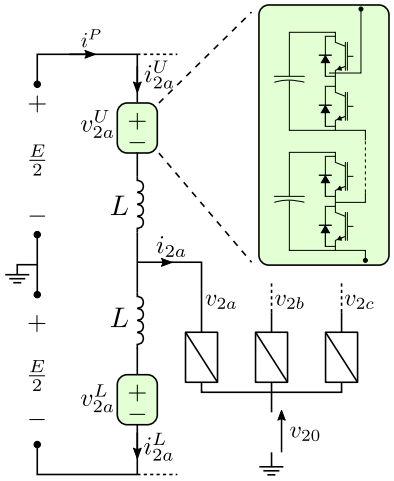


Figure 4.5: *Upper and lower arms of phase a of the machine-side converter.*

In this case, the instantaneous power of the upper arm p^U_{2a} is [149]:

$$p^U_{2a} = v^U_{2a} i^U_{2a} = \left(\frac{E}{2} - v_{2a} - v_{20}\right)\left(\frac{1}{2} i_{2a} + i^\Sigma_{2a}\right) \tag{4.27}$$

$$= \frac{E i_{2a}}{4} + \frac{E i^\Sigma_{2a}}{2} - \frac{i_{2a} v_{20}}{2} - \frac{i_{2a} v_{2a}}{2} - i^\Sigma_{2a} v_{20} - i^\Sigma_{2a} v_{2a} \tag{4.28}$$

Where v_{2a} and v_{20} are the machine output voltage of phase a and v_{20} is the common-mode voltage injected into the stator. The cell capacitance should be chosen for the worst-case scenario, i.e. when the machine operates at low mechanical speed [36]. In this case, as explained in the previous section, a high frequency circulating current and common-mode voltage are injected to reduce the capacitor voltage oscillations per phase. In particular, the circulating

current of phase a is:

$$i_{2a}^{\Sigma}(t) = \frac{i^P}{3} + I_{hf}^{\Sigma}\sin(\omega_{hf}t) \tag{4.29}$$

Where i^P is the dc-link current, I_{hf}^{Σ} is the magnitude of the high-frequency circulating current, and ω_{hf} is its frequency. As explained in chapter 2, a high-frequency circulating current and common-mode voltage are injected to control the cell capacitor unbalance. From the converter point of view, the maximum value of the frequency ω_{hf} depends on the carrier frequency; it is common to choose a frequency f_{hf} at most ten times slower than the carrier frequency [88]. In addition, different common-mode voltage waveforms have been proposed in the literature [150]. In this thesis, a square-wave common-mode voltage is considered to reduce the peak value of the circulating current. However, if a lower dV/dt is required, a sinusoidal common-mode voltage can be injected [151]. In this case, the machine-side MMC injects the following common-mode voltage:

$$v_{20} = V_{20}\text{sgn}(\sin(\omega_{hf}t)) \tag{4.30}$$

To avoid over-modulation problems, the peak value of the common-mode voltage is limited to:

$$V_{20} = \alpha\left(\frac{E}{2} - \|\boldsymbol{v}_{2dq}\|\right) \tag{4.31}$$

Where α=0.85 is a slack variable to ensure enough margin voltage during transient. Most of the low-frequency capacitor voltage oscillations are caused by the voltage term $\boldsymbol{v}_{C2\alpha\beta}^{\Delta}$ [89, 115, 116], the expression of $\boldsymbol{v}_{C2\alpha\beta}^{\Delta}$ is repeated below:

$$Cv_C^*\frac{d\boldsymbol{v}_{C2\alpha\beta}^{\Delta}}{dt} = -(\boldsymbol{v}_{2\alpha\beta}\boldsymbol{i}_{2\alpha\beta}^{\Sigma})^c + \frac{E\boldsymbol{i}_{2\alpha\beta}}{2} - \frac{2}{3}i^P\boldsymbol{v}_{2\alpha\beta} - 2v_{20}\boldsymbol{i}_{2\alpha\beta}^{\Sigma} \tag{4.32}$$

By expressing the previous expression in a rotary reference frame dq:

$$Cv_C^* \frac{d\boldsymbol{v}_{C2dq}^{\Delta}}{dt} = \frac{1}{2} E \boldsymbol{i}_{2dq} - \frac{2}{3} i^P \boldsymbol{v}_{2dq} - jCv_C^* \omega_{2e} \boldsymbol{v}_{C2dq}^{\Delta} - 2v_{20} \boldsymbol{i}_{2dq}^{\Sigma} \tag{4.33}$$

To reduce these oscillations, the derivative of $\boldsymbol{v}_{C2dq}^{\Delta}$ should be equal to zero in (4.33), in this case, the magnitude of the injected circulating current is:

$$I_{hf}^{\Sigma} = \frac{1}{2V_{20}} \left(\left\| \frac{1}{2} E \boldsymbol{i}_{2dq} - \frac{2}{3} i^P \boldsymbol{v}_{2dq} \right\| - Cv_C^* \omega_{2e} \left\| \boldsymbol{v}_{C2dq}^{\Delta} \right\| \right) \tag{4.34}$$

In the previous expression, $\boldsymbol{i}_{2dq}$ and $\boldsymbol{v}_{2dq}$ are the machine stator currents and voltages respectively, and E and i^P are the dc-port voltage and current. The second term depends on the capacitance C, the cell voltage reference v_C^*, the machine electrical frequency ω_{2e}, and the magnitude of the converter voltage vector $\boldsymbol{v}_{C2dq}^{\Delta}$. As shown by eq. 4.34, the magnitude of the circulating current can be reduced by imposing that $\boldsymbol{v}_{C2dq}^{\Delta}$ is in phase with $\frac{1}{2} E \boldsymbol{i}_{2dq} - \frac{2}{3} i^P \boldsymbol{v}_{2dq}$.
The voltage oscillations are caused by the energy oscillations in each arm, the instantaneous energy in the upper arm of phase a is calculated by integrating the instantaneous power p_{2a}^U from (4.27).

$$E_a^U(t) = \int p_{2a}^U(t) dt \qquad t \in [t_0, t_0 + T_{hf}] \tag{4.35}$$

The instantaneous energy E_a^U is calculated from (4.35). In this case, the machine voltage v_{2a} and current i_{2a} are given by:

$$v_{2a}(t) = V_m \cos(\omega_2 t) \tag{4.36}$$

$$i_{2a}(t) = I_m \cos(\omega_2 t + \varphi_2) \tag{4.37}$$

The energy oscillations are calculated by integrating the arm power (4.27) within one period of the common-mode voltage $T_{hf} = \frac{2\pi}{\omega_{hf}}$:

$$\max(\Delta E_a^U) = \max(E_a^U(t)) - \min(E_a^U(t)) \qquad t\in[t_0, t_0 + T_{hf}] \tag{4.38}$$

By neglecting the resistive losses of the MMC, the energy variation per arm can be expressed as a function of the voltage variation of the cell capacitors within this arm:
is equal to the cell capacitors of that arm:

$$\max(\Delta E_a^U) = \frac{1}{2}NC\left(V_{C\max}^2 - V_{C\min}^2\right) \tag{4.39}$$

$$= NC\frac{V_{C\max} + V_{C\min}}{2}(V_{C\max} - V_{C\min}) \tag{4.40}$$

$$\approx NCv_C^*\Delta V_{C2} \tag{4.41}$$

In the previous expressions, $V_{C\max}$ and $V_{C\min}$ are the maximum and minimum cell capacitor voltage. By equating both expressions of the arm energy variation, the cell capacitance C can be calculated as function of the desired ΔV_{C2}.

$$C = \frac{\max(E_a^U(t)) - \min(E_a^U(t))}{N\Delta V_{C2}v_C^*} \qquad t\in[t_0, t_0 + T_{hf}] \tag{4.42}$$

Number of cells and voltage levels

The machine-side MMC is composed of HBSMs, therefore the arm voltage is bounded by:

$$0 \leq v_{2x}^y \leq N_2 v_C^* \qquad x\in\{a,b,c\}, y\in\{U,L\} \tag{4.43}$$

Where v_{2x}^y is the arm voltage of phase $x\in\{a,b,c\}$ and $y\in\{U,L\}$, N_2 is the number of cells per arm and v_C^* is the cell capacitor voltage. According to [149], the minimum value of the dc-link voltage is given by:

$$E_{2\,\min} \geq \max(v_{2x}^y) + v_L \tag{4.44}$$

Where v_L is an additional voltage included for the current control of the dc-current i^P and the control of the circulating currents. In addition, the relation between the cell capacitor voltage and the dc-link voltage is given by (4.45) where the dc-link voltage E is chosen to be larger than the minimum required $E_{2\,\min}$.

$$v_C^* = \frac{E}{N_2} \tag{4.45}$$

The maximum and minimum cell capacitor voltage are given by $V_{C\max}$ and $V_{C\min}$. In [149], it is suggested to include a voltage reserve below and above of the voltage range in steady state operation of the cell capacitor voltages. The main goal is to provide enough voltage margin to improve the dynamic response. In this case, it is suggested to set the voltage reference equal to the maximum cell voltage variation in steady-state operation ΔV_{C2}. The cell capacitor voltage along with the voltage reserves are shown in figure 4.6, the allowed zone is shown in blue while the voltage reserve are shown in red.

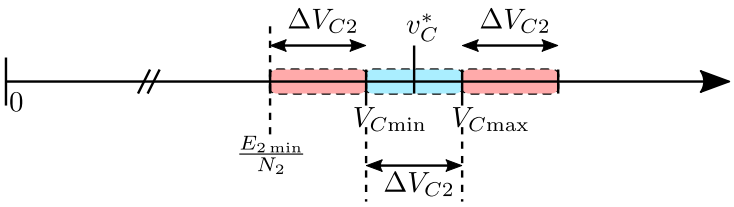


Figure 4.6: *Ranges of the capacitors voltages for the machine-side MMC.*

4.4.3 Arm inductance

Each arm is connected to an inductor L to compensate for any voltage mismatch due to the PWM output voltage of each arm; in addition, the arm inductance is used to control the circulating currents within each MMC. The arm inductance is calculated as a function of the maximum current ripple [152]. In HVDC applications, where each arm can have hundreds of cells, the arm voltage has already low harmonic distortion. Consequently, the arm inductance is chosen between 10% and 20% of the base reactance. The main

concern, in this case, is to choose an arm inductance high enough to limit the arm currents in the event of a short-circuit in the dc-port [153]. However, the number of cells is reduced; consequently, it is common to define a maximum current ripple to be considered in the parameter design process. The current ripple can be expressed as [152]:

$$\Delta i = \frac{v_c^* d_{\text{cell}}(1 - d_{\text{cell}})}{2N f_c L_a} \tag{4.46}$$

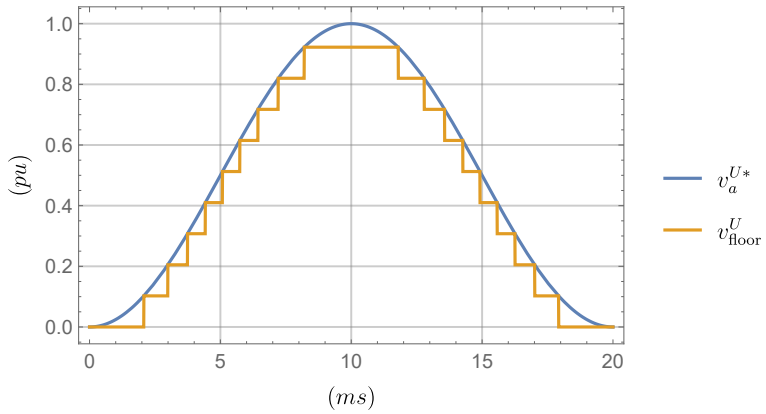
Where L_a is the arm inductance, N is the number of cells per arm, v_c^* is the capacitor voltage reference, f_c is the carrier frequency, and d_{cell} is the cell duty cycle of the output voltage per each voltage level. The value of d_{cell} is derived as the difference between the arm voltage reference and the floor value of multilevel voltage per voltage level. For instance, considering the upper arm of phase a, its voltage reference v_a^{U*} and its floor voltage v_{floor}^U is plotted in fig. 4.7a in per unit and considering N=10, and its equivalent cell duty cycle is depicted in fig. 4.7b.

From the expression of the current ripple (4.46), its maximum value is obtained for a duty cycle d_{cell}=0.5, therefore the minimum arm inductance can be expressed as a function of the maximum current ripple:

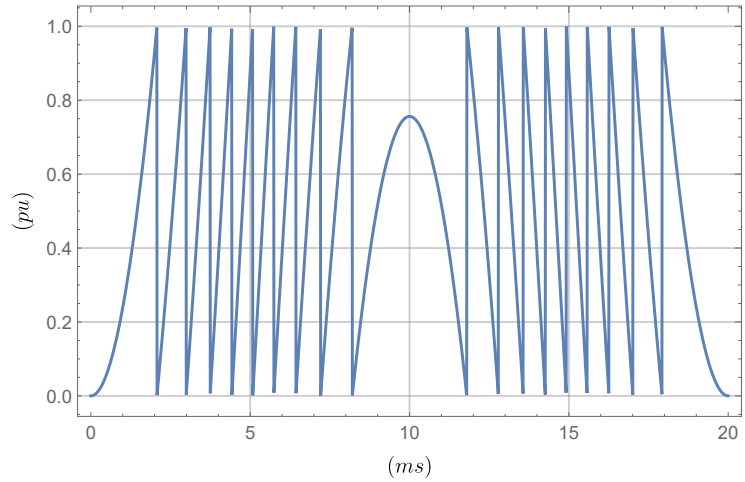
$$L_{\text{min}} = \frac{v_c^*}{8N f_c \Delta i} \tag{4.47}$$

4.5 Summary

This chapter presents the modelling of the modular multilevel converter. First, a decoupled voltage-current model of a generic MMC is derived. This model defines three different converter currents: AC output currents, DC output current, and inner circulating currents. One of the major differences between the MMC and previous multilevel topologies is that the MMC has an extra controllable current denominated as circulating currents. The circulating current



(a) *Voltage reference v_a^{U*} of the upper arm of phase a (blue) and lower voltage level per cell (yellow).*



(b) *Equivalent duty cycle of the output voltage level per cell.*

Figure 4.7: *(a) Voltage reference v_a^U (blue) and voltage level per cell (yellow). (b) Cell duty cycle per voltage level.*

is defined as the average between the upper and lower arm currents per phase. A model using the $\Sigma\Delta\alpha\beta 0$ transformation is presented [115]. The main advantage of this model is that the outer and inner variables are decoupled. Thus, it is possible to regulate the AC and DC output ports independently of the inner circulating currents. Then, a decoupled energy model for a general MMC is also presented; the main advantage of the energy model is that it allows identifying which current components causes unbalance among the MMC arms. Notice that the decoupled model for the MMC can also be applied to the hybrid MMC because it is used to ensure the energy balance among arms. Then, the imbalance problem typical of the hybrid MMC working in over-modulation is presented. When the currents become unipolar, the arm currents are always

positive (or negative); consequently, it is not possible to properly balance the HBSMs.

The decoupled model derived is used in the next chapter to develop a control for the hybrid MMC. In this case, the energy model is used to propose a control for the arm energy of the hybrid MMC. Then, the decoupled voltage model is the base of the inner current control. The same decouple model is considered for the machine-side control in the back-to-back application. In particular, the optimal value of the dc-link voltage is calculated as a function of the electrical machine point of operation.

Chapter 5

Proposed control strategies

5.1 Introduction

The decoupled model presented in the chapter 4 is now used to derive the control of the hybrid MMC and the HBSM-based MMC for drive applications. By using a rotary reference frame, it is possible to regulate the capacitor voltage balance among arms using independent components of the circulating currents. This chapter presents the proposed control of the hybrid MMC (grid-side) and the HBSM-based MMC (machine-side). The main goals are to maintain the voltage of the floating capacitor of each cell at a predefined target value and to control the output/input currents. Firstly, control of the hybrid MMC is presented. In this case, the capacitor voltage balance control is divided in global and local control. The global control is in charge of evenly distributing the energy among the six arms. Conversely, the local balance control ensures that the FBSMs and HBSMs are balanced. Secondly, the control of an hybrid back-to-back (BTB) MMC drive application is presented. In this case, the hybrid MMC uses the previous global and local control to ensure a stable operation. In addition, the hybrid MMC regulates the dc-link voltage of the BTB MMC. The optimal value of the dc-link voltage E_{opt} is calculated to minimise the capacitor voltage oscillations of the machine-side. As a consequence, the required common-mode voltage is reduced in the

machine-side MMC. Finally, the machine-side MMC control is explained, it is worth highlighting that for the machine side only the global control is required since this side is built using a HBSM-based MMC.

In both cases, a nested control structure is used to ensure the capacitor voltage balance and to regulate the output converter current. The general structure of the MMC control, applicable to either converter, is shown in Fig. 5.1. The inner current control loop has a natural frequency 10 times faster than that of the outer capacitor voltage control loop. In the following analysis, the subscripts 1 and 2 are used for the grid and machine side variables respectively.

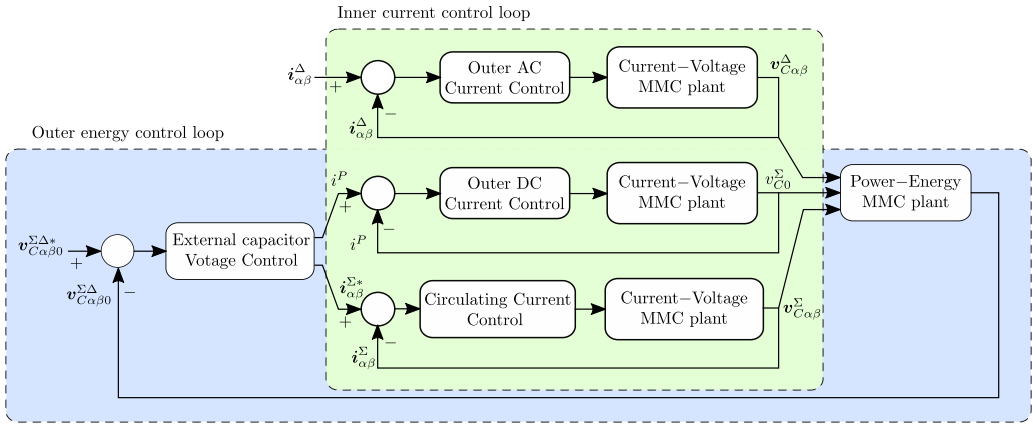


Figure 5.1: *General control structure of the MMC.*

5.2 Global capacitor voltage control of the hybrid MMC

Since the grid frequency is fixed to f_1=50 Hz the floating capacitors of the grid-side do not have considerable oscillations during normal operation. Consequently, in the global capacitor voltage control, the mean value of the total capacitor voltage is regulated. In addition, the global capacitor control is also in charge of ensuring the balance among the 6 arms.

To balance the energy among the six arms, the circulating current $\boldsymbol{i}^{\Sigma}_{1\alpha\beta}$ is used (5.2), by using different components of the circulating current it is possible to balance the arm energy. In addition, the total energy of the hybrid MMC

can be regulated by controlling the direct grid current or the dc-port current. In particular, in this case the total energy is regulated using the direct grid current.

To balance the capacitor voltages an outer control layer manipulates the references of the circulating current $\boldsymbol{i}^{*\Sigma}_{1\alpha\beta}$ and the direct grid current i^{*}_{1d}. By orienting the electric variables in a rotary reference frame along the grid voltage, the output converter variables $\boldsymbol{i}_{1\alpha\beta}$ and $\boldsymbol{v}_{1\alpha\beta}$ along with the circulating currents $\boldsymbol{i}^{\Sigma}_{1\alpha\beta}$ can be expressed as:

$$\boldsymbol{i}_{1\alpha\beta} = \boldsymbol{i}^{+}_{1dq} e^{j\theta_1} \tag{5.1}$$

$$\boldsymbol{i}^{\Sigma}_{1\alpha\beta} = \overline{\boldsymbol{i}^{\Sigma}_{1\alpha\beta}} + \boldsymbol{i}^{\Sigma+}_{1dq} e^{j\theta_1} + \boldsymbol{i}^{\Sigma-}_{1dq} e^{-j\theta_1} \tag{5.2}$$

$$\boldsymbol{v}_{1\alpha\beta} = v_{1d} e^{j\theta_1} \tag{5.3}$$

The voltage terms $\boldsymbol{v}^{\Sigma}_{C1\alpha\beta}$, $\boldsymbol{v}^{\Delta}_{C1\alpha\beta}$, and v^{Δ}_{C10} are related to the arm energy balance of the hybrid MMC. By using the $\Sigma\Delta\alpha\beta 0$ transformation it is straightforward to choose orthogonal components of the circulating current to balance these 5 voltage terms. For instance, the voltage vector $\boldsymbol{v}^{\Sigma}_{C1\alpha\beta}$ is regulated using the mean value of the circulating current $\overline{\boldsymbol{i}^{\Sigma}_{1\alpha\beta}}$. By replacing (5.1)-(5.3) into (4.11) yields:

$$Cv^{*}_{C}\frac{d\boldsymbol{v}^{\Sigma}_{C1\alpha\beta}}{dt} = -\frac{1}{4}(v_{1d} i^{+}_{1dq} e^{2j\theta_1})^{c} + \frac{E}{2}(\bar{i}^{\Sigma}_{1\alpha\beta} + i^{\Sigma+}_{1dq} e^{j\theta_1} + i^{\Sigma-}_{1dq} e^{-j\theta_1}) - \frac{1}{2} v_{10} (i^{+}_{1dq} e^{j\theta_1}) \tag{5.4}$$

From (5.4), the product between the dc-port voltage E and the dc-component of the circulating current has a mean value different from zero. Consequently, the current vector $\overline{\boldsymbol{i}^{\Sigma}_{\alpha\beta}}$ can be used to regulate the average value of $\boldsymbol{v}^{\Sigma}_{C1\alpha\beta}$ as shown in:

$$Cv^{*}_{C}\frac{d\overline{\boldsymbol{v}^{\Sigma}_{C1\alpha\beta}}}{dt} = \frac{E\overline{\boldsymbol{i}^{\Sigma}_{1\alpha\beta}}}{2} \tag{5.5}$$

By doing a similar analysis, it can be shown that the voltage vector $\boldsymbol{v}^{\Delta}_{1\alpha\beta}$ can

be regulated using the negative sequence component of the circulating current $\boldsymbol{i}_{1dq}^{\Sigma-}$. In this case, by replacing (5.1)-(5.3) into (4.12) yields:

$$Cv_C^* \frac{d\boldsymbol{v}_{C\alpha\beta}^{\Delta}}{dt} = -(v_{1d}e^{j\theta_1}(\bar{\boldsymbol{i}}_{1\alpha\beta}^{\Sigma} + \boldsymbol{i}_{1dq}^{\Sigma+}e^{j\theta_1} + \boldsymbol{i}_{1dq}^{\Sigma-}e^{-j\theta_1}))^c + \frac{E\boldsymbol{i}_{1dq}^{+}e^{j\theta_1}}{2} - \frac{2}{3}i^P v_{1d}e^{j\theta_1} \tag{5.6}$$

In the previous expression, notice that only the negative-sequence component $i_{1dq}^{\Sigma-}$ produce a dc controllable term along with the grid voltage. Consequently:

$$Cv_C^* \frac{\overline{d\boldsymbol{v}_{C1\alpha\beta}^{\Delta}}}{dt} = -v_{1d}(\boldsymbol{i}_{1dq}^{\Sigma-})^c \tag{5.7}$$

Finally, v_{C0}^{Δ} is controlled by injecting a positive sequence of the circulating current $i_d^{\Sigma+}$. Replacing (5.1)-(5.3) into (4.13) yields:

$$Cv_C^* \frac{dv_{C10}^{\Delta}}{dt} = -\mathbb{R}\left\{v_{1d}e^{j\theta_1}(\bar{\boldsymbol{i}}_{1\alpha\beta}^{\Sigma} + \boldsymbol{i}_{1dq}^{\Sigma+}e^{j\theta_1} + \boldsymbol{i}_{1dq}^{\Sigma-}e^{-j\theta_1})^c\right\} \tag{5.8}$$

In this case, to regulate the mean value of v_{C10}^{Δ} the direct component of the positive-sequence of the circulating current is employed:

$$Cv_C^* \frac{\overline{dv_{C10}^{\Delta}}}{dt} = -v_{1d}i_{1d}^{\Sigma+} \tag{5.9}$$

In addition to balance the energy between the six arms of the MMC, its total energy has to be controlled as well. In this case, the direct current i_{1d} is used. By replacing (5.1)-(5.3) into (4.10):

$$Cv_C^* \frac{\overline{dv_{C10}^{\Sigma}}}{dt} = \frac{Ei^P}{6} - \frac{v_{1d}i_{1d}}{4} \tag{5.10}$$

The global capacitor voltage control shown in Fig. 5.2 ensures balancing of the total energy among the six arms. It is composed of an outer voltage layer (green) and an inner current layer (blue). The floating capacitor voltages

within each arm are added to obtain the total capacitor voltage V_{Cabc}^{UL} which is then referred to the $\Sigma\Delta\alpha\beta 0$ reference frame. Notice that the term $\boldsymbol{v}_{C\alpha\beta}^{\Sigma}$ has a double frequency component $2\omega_g$ due to the term $0.25(\boldsymbol{v}_{\alpha\beta}\boldsymbol{i}_{\alpha\beta})^c$ [see (4.11)], while the term $\boldsymbol{v}_{C\alpha\beta}^{\Delta}$ has a frequency component ω_g (4.12). The oscillatory components of $\boldsymbol{v}_{C\alpha\beta}^{\Sigma}$ and $\boldsymbol{v}_{C\alpha\beta}^{\Delta}$ are removed using notch filters tuned at $2\omega_g$ and ω_g respectively. To ensure balance among the 6 arms, the voltage references in the $\Sigma\Delta\alpha\beta 0$ coordinate frame are:

$$v_{C0}^{\Sigma *} = N v_C^* \qquad v_{C\alpha}^{\Sigma *} = v_{C\beta}^{\Sigma *} = v_{C\alpha}^{\Delta *} = v_{C\beta}^{\Delta *} = v_{C0}^{\Delta *} = 0 \tag{5.11}$$

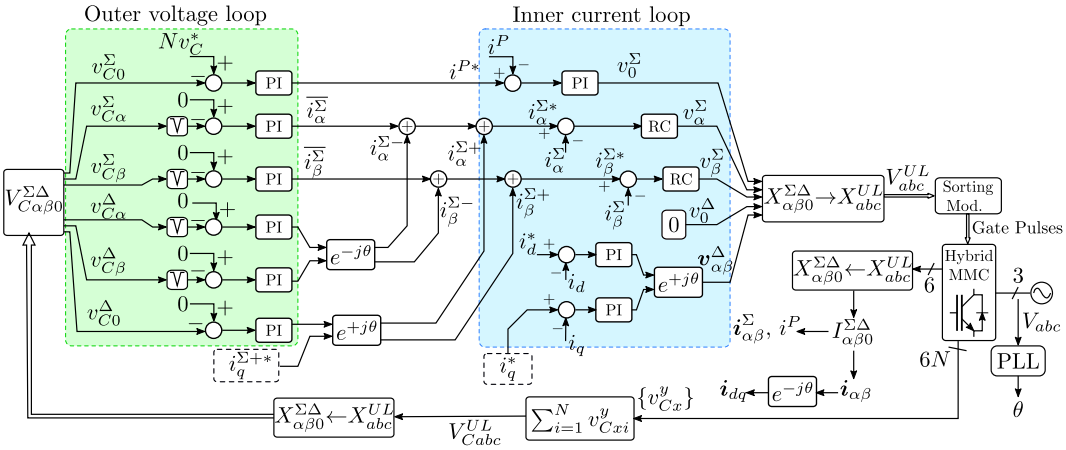


Figure 5.2: *Proposed global balance control.*

The transfer function of the outer voltage controller plants are shown in Table 5.1. To regulate the voltages, with zero steady-state error, PI controllers are utilised.

$$G_{PI} = K_p \frac{s + K_i}{s} \tag{5.12}$$

The column *Manipulated Current* in Table 5.1 is the current component regulated by the inner control loop to drive the respective voltage component to the reference value.

Regarding the inner current controllers, the transfer functions between the

Table 5.1: Plant model of the global and local capacitor voltage controllers.

Voltage comp.	Voltage-current Plant	Manipulated Current
v_{C0}^{Σ}	$\frac{E}{6Cv_C^*s}$	i^P
$v_{C\alpha}^{\Sigma}$, $v_{C\beta}^{\Sigma}$	$\frac{E}{2Cv_C^*s}$	$\overline{i_{\alpha}^{\Sigma}}$, $\overline{i_{\beta}^{\Sigma}}$
v_{C0}^{Δ}	$-\frac{v_d}{Cv_C^*s}$	$i_d^{\Sigma+}$
$v_{C\alpha}^{\Delta}$, $v_{C\beta}^{\Delta}$	$\frac{v_d}{Cv_C^*s}$	$i_d^{\Sigma-}$, $i_q^{\Sigma-}$
$\Delta v_F^{\Sigma} - \Delta v_H^{\Sigma}$	$[\frac{\partial(v_F^{\Sigma}-v_H^{\Sigma})}{\partial i_q}]_0$	Δi_q or $\Delta i_q^{\Sigma+}$

manipulable voltages $V_{\alpha\beta 0}^{\Sigma}$ and the converter currents $I_{\alpha\beta 0}^{\Sigma\Delta}$ are derived from (4.6) and shown in Table 5.2. To regulate the capacitor voltages $V_{C\alpha\beta 0}^{\Sigma\Delta}$, with

Table 5.2: Plant models for the current controllers.

Current comp.	Plant	Manipulated Voltage
i_{α}^{Σ} , i_{β}^{Σ}	$-\frac{1}{sL}$	v_{α}^{Σ}, v_{β}^{Σ}
i^P	$-\frac{3}{sL}$	v_0^{Σ}
i_d, i_q	$-\frac{1}{sL}$	v_d^{Δ}, v_q^{Δ}

zero steady-state error, PI controllers are utilised. The outer voltage controllers provide the circulating current $\boldsymbol{i}_{\alpha\beta}^{\Sigma *}$, reactive current i_q^* and dc-port i^{P*} current references to the inner control loops. The circulating currents $\boldsymbol{i}_{\alpha\beta}^{\Sigma}$ are regulated using proportional resonant controllers tuned at ω_g (see [123, 154]). The dc-port current i^P and grid currents $\boldsymbol{i}_{dq}$ are regulated using PI controllers.

The output of the inner current controllers provide the voltages references $V_{\alpha\beta 0}^{\Sigma\Delta}$ to be synthesised by the hybrid-MMC cells. The arm voltage references V_{abc}^{UL} are calculated using the inverse $\Sigma\Delta\alpha\beta 0$ transformation. Finally, a sorting modulator is used to generate the gate drive signals for each cell [155]. In the sorting modulator, the sub-module capacitor voltages are sorted ascending (descending) for a positive (negative) arm current. Next, if the reference arm voltage v_x^{y*} is positive both sub-modules types are allowed to operate and they are inserted according to the previous sorted list without exceeding v_x^{y*}, the remainder between v_x^{y*} and the capacitor voltage of the inserted sub-modules is synthesized using pulse width modulation (PWM). On the other hand, if $v_x^{y*} \leq 0$ only the FBSMs can operate while the HBSMs are bypassed. The sorting modulation algorithm also provides cell-balancing capability within

each arm. The sorting modulator for the phase $x \in \{a, b, c\}$ and arm $y \in \{U, L\}$ is explained in the algorithm 1.

Algorithm 1 Algorithm of the sorting modulator implemented for the MMC operation.

Require: $-N_F v_C^* \leq v_x^{y*} \leq N v_C^*$
Ensure: $\sum_{i=1}^{N_H} m_{xi}^y v_{Cxi}^y + \sum_{i=N_H+1}^{N} m_{xi}^y v_{Cxi}^y = v_x^{y*}$
$m_{xi}^y \leftarrow 0 \ \forall i \in \{1, \ldots, N\}$
$i \leftarrow 0$
partialS $\leftarrow 0$
if $v_{xi}^{y*} > 0$ **then**
    if $i_x^y > 0$ **then**
        Sort (descending) v_{Cxi}^y
    else
        Sort (ascending) v_{Cxi}^y
    while partialS $+ v_{Cxi}^y \leq v_{xi}^{y*}$ **do**
        partialS $\leftarrow$ partialS $+ v_{Cxi}^y$
        $m_{xi}^y = 1.0$
        $i \leftarrow i + 1$
    $m_{xi}^y = (v_{xi}^{y*} - \text{partialS})/v_{Cxi}^y$
else
    $i \leftarrow H + 1$
    while partialS $- v_{Cxi}^y \geq v_{xi}^{y*}$ **do**
        partialS $\leftarrow$ partialS $- v_{Cxi}^y$
        $m_{xi}^y = -1.0$
        $i \leftarrow i + 1$
    $m_{xi}^y = (v_x^{y*} - \text{partialS})/v_{Cxi}^y$

5.3 Local balance control of the hybrid MMC

As discussed in Section 4.3, an inherent unbalancing mechanism between the HBSMs and FBSMs of the hybrid MMC can exist for high modulation indexes, if the arm currents are unipolar. Here, two strategies are proposed for overcoming this problem. The objective of the work described in this section was to develop new strategies based on both reactive and circulating current to balance the FBSMs and HBSMs of an hybrid MMC working in over-modulation. It was recognised that previous solutions to this problem [30, 42, 146, 156] were sub-optimal in that the amount of extra current employed was greater than that required and no simple closed expressions were derived to calculate

their value. To address this a detailed analysis of the unbalancing phenomenon was undertaken. This has yielded new analytical expressions for the required currents and has led to the development of a new balancing methodology that intrinsically ensures that the minimum balancing current is used under all operating scenarios. The arm current can be made bipolar by injecting reactive current or circulating current. Both strategies aim to move energy from the FBSMs to the HBSM and vice versa. Optimal methodologies to minimise the required circulating or reactive currents have not been proposed before. This is achieved through an analysis which yields explicit equations for the compensating currents. This analysis has not been presented before.

For the analysis presented below, it is considered that the cascade connections of FBSMs and HBSMs of phase $x{\in}\{a,b,c\}$ and pole $y{\in}\{U,L\}$ are modelled as two equivalent sub-modules with a capacitor voltage equal to v^y_{Fx} and v^y_{Hx} [see (5.13)]. In the following analysis, the total capacitor voltage of the HBSMs and FBSMs is calculated as shown in (5.14). Finally, the voltage error between the FBSMs and HBSMs is the difference between the average value of the capacitor voltages of the FBSMs and HBSMs [see (5.15)].

$$v^y_{Hx}{=}\frac{1}{N_H}\sum_{i=1}^{N_H} v^y_{Cx_i} \qquad v^y_{Fx}{=}\frac{1}{N_F}\sum_{i=1+N_H}^{N} v^y_{Cx_i} \tag{5.13}$$

$$v^{\Sigma}_{H} = \sum_{x,y}\frac{v^y_{Hx}}{6} \qquad v^{\Sigma}_{F} = \sum_{x,y}\frac{v^y_{Fx}}{6} \tag{5.14}$$

$$e_{FH} = \overline{v}^{\Sigma}_{F} - \overline{v}^{\Sigma}_{H} \tag{5.15}$$

5.3.1 Reactive current injection method (CLC-I)

The arm current and voltage i^U_a and v^U_a in steady-state operation can be expressed as (5.16)-(5.17) where i_d and i_q are the active and reactive grid-current, and $\theta{=}\omega_g t$ with ω_g as the grid frequency. It is assumed that the voltages and currents are referred to a synchronous rotating reference frame orientated along

the grid voltage $\boldsymbol{v}_g$.

$$i_a^U = \frac{i_d}{2}\left(\cos(\theta) + \frac{m}{2}\right) - \frac{i_q}{2}\sin(\theta) \tag{5.16}$$

$$v_a^U = \frac{E}{2}\left(1 - m\cos(\theta)\right) \tag{5.17}$$

To illustrate the local balancing problem between the HBSMs and FBSMs for $m \geq 2$, the instantaneous and average value of the capacitor voltages for the HBSMs v_{Ha}^U and FBSMs v_{Fa}^U, along with the arm voltage v_a^U and arm current i_a^U are shown in Fig. 5.3, considering $i_d < 0$ and $i_q > 0$. A similar analysis can be performed for the other operating conditions.

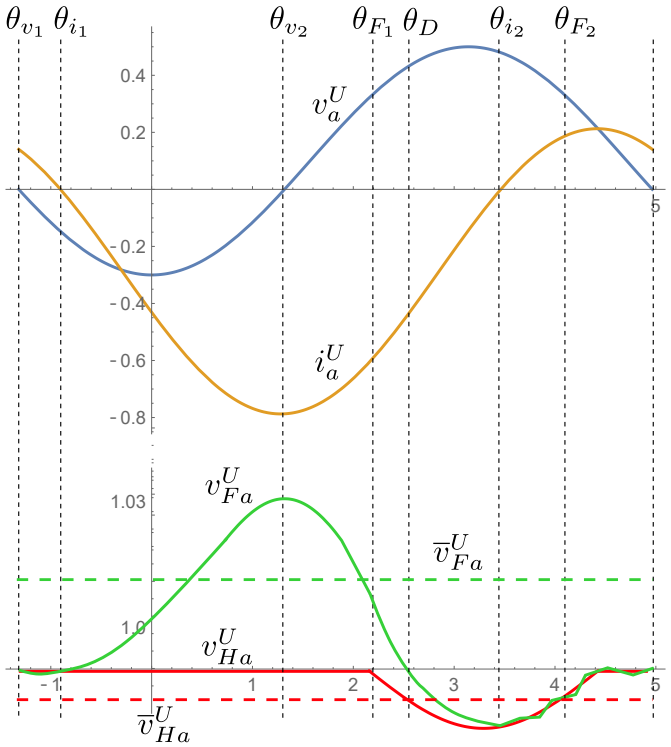


Figure 5.3: *Sub-module charging and discharging process for CLC-I. Arm voltage v_a^U (blue), arm current i_a^U (yellow), capacitor voltage of the equivalent FBSMs v_{Fa}^U (green) and HBSMs v_{Ha}^U (red).*

In Fig. 5.3, $\theta_{v_1} - \theta_{v_2}$ and $\theta_{i_1} - \theta_{i_2}$ are the zero-crossing angles of the arm voltage v_a^U and current i_a^U respectively. Additionally, θ_{F_1} and θ_{F_2} are the angles at which the arm voltage v_a^U is equal to the maximum synthesised voltage of the

FBSMs:

$$\theta_{v_1} = -\cos^{-1}\left(m^{-1}\right) \qquad \theta_{v_2} = -\theta_{v_1} \tag{5.18}$$

$$\theta_{i_1} = \cos^{-1}\left(-\frac{m i_d}{2\left\|\boldsymbol{i}_{dq}\right\|}\right) - \tan^{-1}(i_q, i_d) \tag{5.19}$$

$$\theta_{i_2} = 2\pi - \theta_{i_1} + 2\tan^{-1}(i_q, i_d) \tag{5.20}$$

$$\theta_{F_1} = \cos^{-1}\left(\frac{1}{m} - \frac{N_F v_C^*}{V_g}\right) \qquad \theta_{F_2} = 2\pi - \theta_{F_1} \tag{5.21}$$

In this case, the i_q required to guarantee balance between the HBSMs and FBSMs is calculated by considering that the ΔE energy incremented in the FBSMs (while the HBSMs synthesise 0V) is released during $\theta \leq \theta_{i_2}$.

1. Initially, between θ_{v_1} and θ_{v_2} the arm voltage is negative, and only the FBSMs generate voltage while the HBSMs produce 0V. In this case, the FBSMs increase their total energy W_F^+ (5.22). Although the HBSMs could be inserted, the FBSMs would then modulate an even lower negative voltage and consequently W_F^+ will be higher than the case when the HBSMs produce 0V.

$$W_F^{(+)} = \int_{\theta_{v_1}}^{\theta_{v_2}} v_a^U i_a^U d\theta = -\frac{i_d E}{4\omega_g}\frac{\left(m^2-1\right)^{3/2}}{m} \tag{5.22}$$

2. Next, in the interval between θ_{v_2} and θ_{F_1} the capacitors of the FBSMs will discharge while the HBSMs synthesise 0V since, in this period, the FBSMs have higher priority to be discharged. The energy exchange is $W_{F1}^{(-)}$ and it is calculated similarly to the previous case, see (5.23).

$$\begin{aligned} W_{F1}^{(-)} = \frac{0.25}{E V_g \omega_g}\Big(& i_d\sqrt{4V_g^2 - E^2}\left(V_g^2 - \tfrac{E^2}{4}\right) - E i_q (v_C^* N_F)^2 \\ & + 2 i_d \sqrt{V_g^2 - (v_C^* N_F - \tfrac{E}{2})^2}\left(\tfrac{E^2}{4} + \tfrac{E}{2} N_F v_C^* - V_g^2\right)\Big) \end{aligned} \tag{5.23}$$

3. Finally, from θ_{F1} and θ_D, the FBSMs alone are not able to synthesise the required voltage and both the FBSMs and the HBSMs have to be used. As depicted in Fig. 5.3, θ_D is the angle where the FBSMs have finally released the entire energy, W_F^+, incremented between θ_{v_1} and θ_{v_2}. Notice that $\theta_D \leq \theta_{i2}$. The energy released in this period, by the FBSMs, is $W_{F2}^{(-)}$ see (5.24).

$$\begin{aligned} W_{F2}^{(-)}=&\frac{N_F v_C^*}{2EV_g\omega_g}\Big(-\tfrac{E^2}{2}i_q+Ei_dV_g\sin(\theta_D)+Ei_qN_Fv_C^* \\ &+i_d\theta_DV_g^2-\tfrac{E}{2}i_d\sqrt{-E^2+4EN_Fv_C^*-4(v_C^*N_F)^2+4V_g^2} \\ &-i_dV_g^2\cos^{-1}\left(\frac{E-2N_Fv_C^*}{2V_g}\right)+Ei_qV_g\cos(\theta_D)\Big) \end{aligned} \tag{5.24}$$

To ensure the balance of the FBSMs, the total energy stored during θ_{i1} to θ_{v2} has to be released between θ_{v_2} and θ_D, i.e.:

$$W_F^{(+)} + W_{F1}^{(-)} + W_{F2}^{(-)} = 0 \tag{5.25}$$

Therefore, the required i_q can be calculated from (5.25) as a function of θ_D. As an example, a simple case is considered assuming m=2.6; N_F/N_H=0.5; and v_C^*=E/N. The required reactive current for this operating condition is shown in (5.26).

$$i_q(\theta_D) = \frac{i_d(-1.2987\theta_D - \sin(\theta_D) + 5.77691)}{\cos(\theta_D) - 0.0183333} \tag{5.26}$$

To inject the minimum reactive current that ensures the local balance (5.25), the following optimisation problem is proposed:

$$\begin{aligned} \underset{\theta_D}{\text{minimize}} \quad & i_q(\theta_D) \\ \text{subject to} \quad & W_F^{(+)} + W_{F1}^{(-)} + W_{F2}^{(-)} = 0, \\ & \theta_{F_1} < \theta_D < \theta_{i_2} \end{aligned} \tag{5.27}$$

which is numerically solved off-line (using the Nelder-Mead method [157]). The reactive grid-currents are calculated from the result of (5.27) and are stored in a look-up table as shown in Fig. 5.6(b).

5.3.2 Circulating current injection (CLC-II)

Bipolar arm current can also be forced by injecting a quadrature component in the circulating current. In this case, the extra component only appears in the converter arms and affects neither the ac nor the dc ports of the MMC. The currents components $i_d^{\Sigma+}$, $\boldsymbol{i}_{dq}^{\Sigma-}$ and $\overline{\boldsymbol{i}_{\alpha\beta}^{\Sigma}}$ are employed to balance energy among the 6 arms of the hybrid MMC as discussed before (global capacitor voltage balance). In the proposed method, a quadrature component of the circulating current ($i_q^{\Sigma+}$) is utilised as a degree of freedom to force a polarity change in the arm currents. The circulating current in natural coordinates i_{abc}^{Σ} can be expressed as:

$$\begin{pmatrix} i_a^{\Sigma} \\ i_b^{\Sigma} \\ i_c^{\Sigma} \end{pmatrix} = \begin{pmatrix} i_{GBa}^{\Sigma} \\ i_{GBb}^{\Sigma} \\ i_{GBc}^{\Sigma} \end{pmatrix} - i_q^{\Sigma+} \begin{pmatrix} \sin(\theta) \\ \sin(\theta - \frac{2\pi}{3}) \\ \sin(\theta + \frac{2\pi}{3}) \end{pmatrix} \tag{5.28}$$

where the terms i_{GBx}^{Σ} are the circulating currents used for the global balance, for instance, for phase a:

$$i_{GBa}^{\Sigma} = \overline{i_{\alpha}^{\Sigma}} + (i_d^{\Sigma+} + i_d^{\Sigma-})\cos(\theta) + i_q^{\Sigma-}\sin(\theta) \tag{5.29}$$

During steady-state operation the circulating current required to perform the global balance of the capacitor voltages becomes negligible, therefore $i_{GBx}^{\Sigma} \approx 0$. The circulating current $i_q^{\Sigma+}$ is added to both the upper and lower arm currents. For instance, if a circulating current component $i_q^{\Sigma+}$ is injected, the

arm currents i_a^y with $y \in \{U, L\}$ become:

$$i_a^y = \sqrt{0.25 i_d^2 + (\pm 0.5 i_q + i_q^{\Sigma+})^2} \cos\left(\omega t + \varphi_a^{U,L}\right) + \frac{i^P}{3} \tag{5.30}$$

$$\varphi_a^y = \text{atan2}\left(\pm 0.5 i_q + i_q^{\Sigma+}, \pm 0.5 i_d\right) \tag{5.31}$$

According to (5.30)-(5.31), the phase shift and magnitudes of the arm currents i_x^U and i_x^L could be different. Therefore, the charging/discharging behaviour of the HBSMs and FBSMs of the upper and lower arms is not the same when compensation utilising circulating current is applied. The minimum required current $i_q^{\Sigma+}$ to guarantee the balance between HBSMs and FBSMs can be calculated in a similar manner to that for the previous method CLC-I. However, due to the asymmetry between i_x^U and i_x^L, it is necessary to compute the minimum $i_q^{\Sigma+}$ for the upper and lower arms separately. For the operating point considered previously to derive (5.26), and i_q=0, the required circulating currents $i_{qU}^{\Sigma+}$ and $i_{qL}^{\Sigma+}$ for the upper and lower arms respectively are:

$$i_{qU}^{\Sigma+}(\theta_U) = \frac{i_d(-0.649351\theta_U - 0.5\sin(\theta_U) + 2.88846)}{\cos(\theta_U) - 0.0183333} \tag{5.32}$$

$$i_{qL}^{\Sigma+}(\theta_L) = \frac{i_d(-0.649351\theta_L + 0.5\sin(\theta_L) + 3.08257)}{\cos(\theta_L) - 0.226111} \tag{5.33}$$

Notice that $i_{qU}^{\Sigma+}(\theta_U) = 0.5 i_q(\theta_D)$ [see (5.16) and (5.30)] which is consistent with the fact that the contribution of the reactive current and circulating component in the upper arm current are $-0.5 i_q$ and $-i_q^{\Sigma+}$ respectively.

To obtain the feed-forward compensation current, a numerical off-line minimisation procedure is used to calculate the angles θ_U and θ_L that minimise $i_{qU}^{\Sigma+}$ and $i_{qL}^{\Sigma+}$ respectively. The optimisation problem is almost identical to that in (5.27), but using circulating currents instead of imposing a reactive current component in the grid. For the same operating point, the maximum of the pair ($i_{qU}^{\Sigma+}$, $i_{qL}^{\Sigma+}$) is used as the feed-forward compensating current and is stored in a look-up table. This is shown in Fig. 5.6(c).

5.3.3 Comparison between CLC-I and CLC-II

The main differences between CLC-I and CLC-II are the modulation margin and the power factor of the grid currents. The modulation margin is the unoccupied sub-module capacitor voltage per arm. When reactive current is utilised (see Section IV.A), it is relatively simple to demonstrate [from (4.6)] that the reactive current in steady state is:

$$0 = v_d^{\Delta} + 2V_g - \omega_g L i_q \rightarrow i_q = \frac{v_d^{\Delta} + 2V_g}{\omega_g L} \tag{5.34}$$

where the variables are oriented along the grid voltage, ω_g is the grid angular frequency, V_g is the grid voltage, v_d^{Δ} is the d-axis voltage synthesised by the hybrid-MMC and L is the arm inductance. From (5.34) it is concluded that in steady state operation when i_q=0, v_d^{Δ} is intrinsically negative with a value of $v_d^{\Delta} \approx -2V_g$. Therefore (5.34) can be written as:

$$i_q = \frac{V_g - (|v_d^{\Delta}|/2)}{\omega_g (L/2)} \tag{5.35}$$

where the voltage $|v_d^{\Delta}|/2$ is equivalent to a "converter voltage" (see [153]). Using (5.35), it is concluded that the magnitude of i_q, when the hybrid-MMC is supplying a lagging reactive power to the grid (i_q>0), is easy to increase by reducing the voltage $|v_d^{\Delta}|$ synthesised by the converter. Therefore there is a relatively large voltage (the full magnitude of the grid voltage vector) to produce this current. On the other hand, if it is required to supply leading reactive power to the grid (i.e. i_q<0), the voltage $|v_d^{\Delta}|$ synthesised by the converter has to be increased until the numerator of (5.35) becomes negative. Therefore, if the voltage margin in the capacitors is low, particularly in the time interval where only the FBSMs (e.g. for m>2) are operating, then it is concluded that there is less voltage margin available, i.e. without reaching over-modulation, to achieve operation with i_q<0. Moreover, if the hybrid

MMC is connected to a weak grid with a non-negligible Thevenin reactance, a larger value of $|v_d^{\Delta}|/2$ is required to regulate a reactive current i_q<0.

In summary, regarding CLC-I, it can be concluded that the main advantage of this strategy (for i_q>0) is the relatively large voltage margin available which can be used to improve the dynamic response and steady state operation of this method. This is further corroborated by the experimental results given in Section VI. The main disadvantage of CLC-I is that the grid has to operate with low power factor, and this could be infeasible for long-term operation.

To analyse CLC-II, the arm voltage v_a^U obtained from (4.4), is used:

$$v_a^U = v_\alpha^\Sigma + v_0^\Sigma + \frac{1}{2}v_\alpha^\Delta + \frac{1}{2}v_0^\Delta \tag{5.36}$$

Using (4.6) and neglecting the voltage drop in the inductance, the values of v_0^Σ, v_α^Δ and v_0^Δ can be replaced by their equivalents in natural coordinates as:

$$v_a^U \approx v_\alpha^\Sigma + \frac{E}{2} + v_{ga} + v_0 \tag{5.37}$$

where the voltage v_{ga} is the phase-a grid voltage, E is the dc-link voltage and v_0 is the common mode voltage, which is not considered in this application (i.e.$v_0 = 0$). Therefore the upper arm has to synthesise a peak v_a^U value approximately equal to the sum of the peak phase to neutral grid voltage, half of the dc-link voltage and the peak value of v_α^Σ.

Considering that a fraction of the voltage $v_{\alpha\beta}^\Sigma$ is required to regulate the current $i_q^{\Sigma+}$, utilised in CLC-II, the voltage margin (at a particular operating point) is provided by the maximum value of $|v_{\alpha\beta}^\Sigma|$ that can be synthesised without over-modulation resulting in in any of the submodules. However, it is not simple to determine this margin considering that the components of the circulating current required for balancing the energy in the hybrid-MMC [see (4.14)] are also regulated using $v_{\alpha\beta}^\Sigma$. Using the criterion reported in [158] the fraction of the capacitor voltage utilised for v_α^Σ could be set to $\approx$ 20% (for an HVDC

system). However this 20% of voltage margin is still well below that available in CLC-I when $i_q > 0$ [see (5.35)].

In summary, the strategy CLC-II has less voltage margin than that of CLC-I (for $i_q > 0$) and this affects the dynamic performance of this methodology and the maximum value of $i_q^{\Sigma+}$ which can be synthesised. However, the main advantage of this control methodology is that the grid can be operated with unity power factor.

The optimal values of the reactive current i_q (CLC-I) and circulating current $i_q^{\Sigma+}$ that guarantee the local balance between the HBSMs and FBSMs are shown in Figs. 5.4 and 5.5 respectively. These values have been obtained using the methodology discussed in sections 5.3.1 and 5.3.2. Notice that for determining Fig. 5.5 unity power factor operation at the grid side has been considered. The compensating currents required (i_q and $i_q^{\Sigma+}$) are shown as a function of the modulation index m and the direct grid-current i_d. In both cases, the required current increases as the modulation index or the direct current increases. Moreover, it has to be considered that the current $|i_q|$ is a grid current and the current $|i_q^{\Sigma+}|$ is the arm current. Therefore their magnitudes cannot be directly compared unless it is considered that the arm current produced by CLC-I is half of $|i_q|$ [see (5.16)]. Finally notice that the absolute values, i.e. $|i_q|$ and $|i_q^{\Sigma+}|$, are shown in Figs. 5.4 and 5.5 because equal balancing performance is obtained with $\pm i_q$ and $\pm i_q^{\Sigma+}$. As stated in Section IV.B, for CLC-II the optimisation problem has to be solved for the upper and lower arms independently. The currents for the upper and lower arms are shown in the yellow and blue plots of Fig. 5.5. For $i_d>0$ ($i_d<0$), the magnitude of the required current for the lower arms is higher (lower) than that of the upper arms.

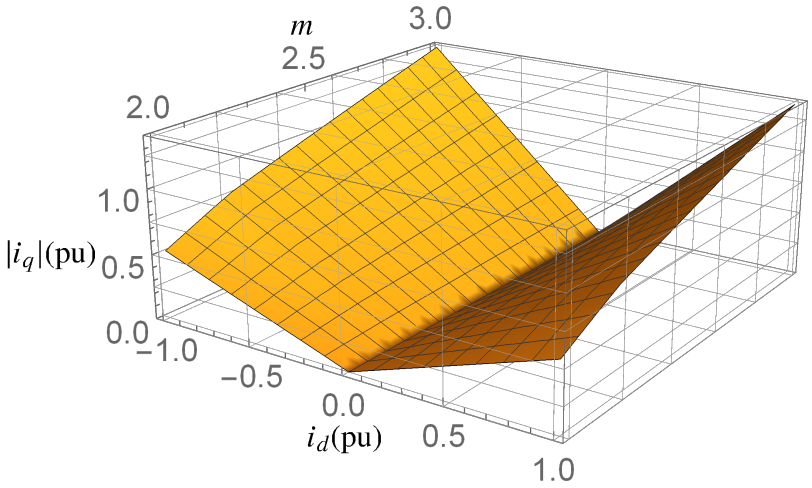


Figure 5.4: *Minimum $|i_q|$ (pu) as a function of the modulation index m and the direct current i_d (pu).*

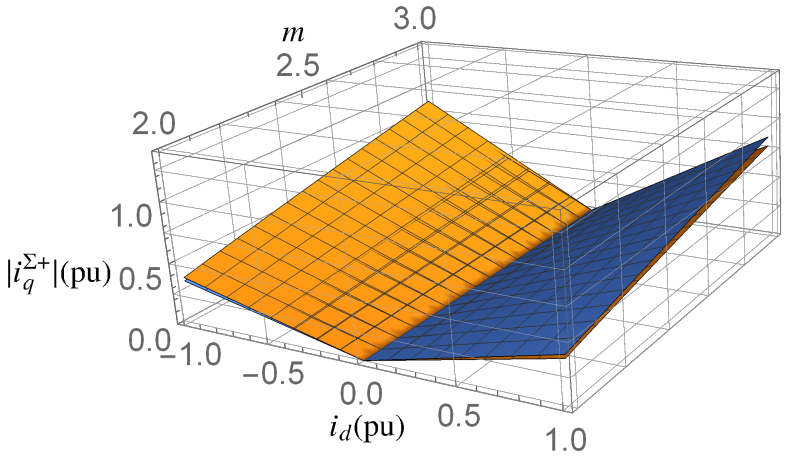


Figure 5.5: *Minimum $|i_q^{\Sigma+}|$ (pu) as a function of the modulation index m and the direct current i_d (pu).*

5.4 Local capacitor closed-loop voltage control

In the previous section, two mechanisms were identified for transporting energy between the FBSMs and HBSMs of an hybrid MMC operating at high modulation index. This section proposes closed loop control approaches, based on either mechanism, which enables capacitor balancing of the converter studied. Using the results of the analysis in the previous section, the proposed approaches always use the optimum solution at each operating point.

The local capacitor voltage control regulates the imbalance between the capacitor voltages of the FBSMs and HBSMs when the arm current becomes unipolar. The local balance control is shown in Fig. 5.6. In Fig. 5.6(a) the

outer control loop is shown, as well as a feed-forward current component stored in a look-up table. This feed-forward component can be obtained either from the CLC-I strategy [see Fig. 5.6(b)] or from the CLC-II control strategy [see Fig. 5.6(c)]. Outer control loop design is discussed below in Section 5.4.1.

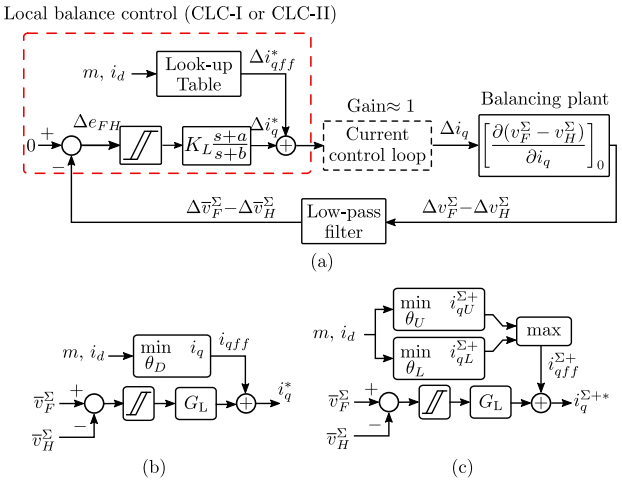


Figure 5.6: *Proposed local balance control. (a) general structure of the local balance control, (b) proposed control CLC-I, and (c) proposed control CLC-II.*

5.4.1 Design of the Outer Voltage control loop

As shown in Fig. 5.6(a), the voltage difference e_{FH} between the average capacitor voltages of the FBSMs $\overline{v}_F^{\Sigma}$ and the HBSMs $\overline{v}_H^{\Sigma}$ [see (5.13)-(5.15)] is filtered out and processed by a controller based on a lag network which can be designed to have a high rejection of the dc component of the error e_{FH}. An integrator is avoided in this application because, in steady state operation, the average capacitor voltages of the FBSMs and HBSMs could be slightly different even when the energies in the FBSMs and HBSMs are balanced. Therefore, the utilisation of a PI controller is not a suitable option to regulate Δe_{FH}.

For the design of the lag controller it is assumed that a slow dynamic is required for the outer voltage control loop, considering that a well-estimated feed-forward compensating current will compensate most of the error e_{FH} with the faster dynamic response typically produced by the inner control loops. Therefore, the transfer function between Δi_q^* and $\Delta v_{CF}^{\Sigma} - \Delta v_{CH}^{\Sigma}$ can be repre-

sented as a small signal gain evaluated at a quiescent point "0", i.e:

$$\Delta e_{FH} = \left[\frac{\partial\left(v_{CF}^{\Sigma} - v_{CH}^{\Sigma}\right)}{\partial i_q}\right]_0 \Delta i_q = K_{FH}\Delta i_q \tag{5.38}$$

A similar transfer function to that in (5.38) can be obtained for the CLC-II strategy. A voltage hysteresis band is utilised in the outer control loop, therefore if e_{FH} is greater than the upper threshold, $V_{C\mathrm{U}}$, then the lag compensator is activated, and will be deactivated when e_{FH} is below the lower threshold $V_{C\mathrm{L}}$. The transfer function of the lag-controller is:

$$G_L = K_L\frac{s+a}{s+b} \tag{5.39}$$

The dc-gain of the lag controller depicted in (5.39) is equal to $(a/b)K_L$. Therefore by adequately selecting the values of K_L, a and b a good rejection of the dc-component of e_{FH} is obtained. Design of the lag controller has been realised using the root locus method. The gain K_{FH} of (5.38) has been obtained using simulation work considering different modulation indexes, for a hybrid MMC with N_F/N_H=1/2. These results are shown in Fig. 5.7 and they are very similar for both the CLC-I and CLC-II strategies. In Fig. 5.7(a) the variation of the e_{FH} respect to the reactive current is shown, the voltage error is expressed in per unit and the base voltage is defined as the total capacitor voltage reference Nv_C^*. Notice that after the balancing is achieved, increasing the current i_q (or $i_q^{\Sigma+}$) does not produce any effect in the error e_{FH}.

The small signal gain K_{FH} [see (5.38)] is shown in Fig. 5.7(b). Using m=2.8 as an example, it is shown in Fig. 5.7(b) that for an i_q current below $\approx$ 0.15pu the gain K_{FH} is $\approx$ 0. This is because the arm current is unipolar and no balancing is possible. For i_q>0.15pu the gain K_{FH} is strongly non-linear until it return to zero when the balancing is achieved. Notice that after balancing the energy between the full and half bridge cells in the converter, the effects produced in e_{FH} by increasing the current i_q (or $i_q^{\Sigma+}$) are negligible. The gain

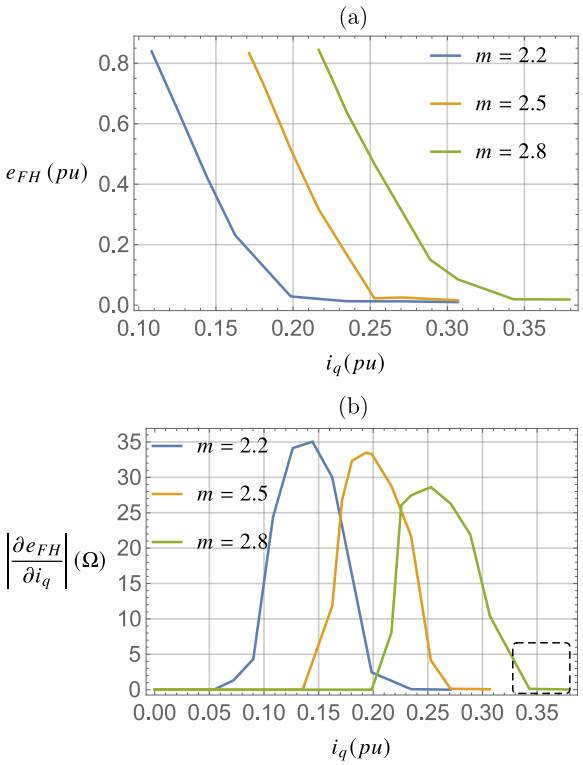


Figure 5.7: *Gain of the local balance plant for CLC-I.*

K_{FH} has units of Ohms and consequently is expressed in per unit considering the base impedance.

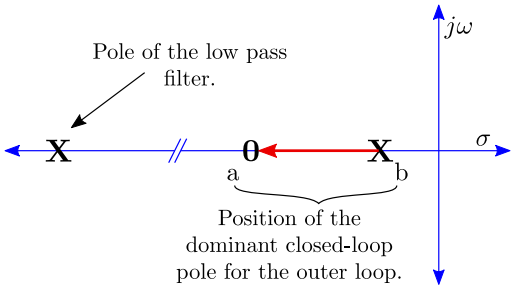


Figure 5.8: *Root locus for the design of the outer control loop.*

Using Fig. 5.7 the design of the lag controller [see (5.39)] is simple to realise using Root Locus or any other control-design methodology. From Fig. 5.6(a) it is concluded that the outer voltage control system has a closed loop transfer function with a single dominant pole whose location is between the zero "a" and the pole "b" (see Fig. 5.8). Therefore, the natural frequency of this dominant pole is limited. Moreover, even when the variation of the gain K_{FH} could be relatively high, as shown in Fig. 5.7, this gain variation is restricted when the feedforward compensating currents of CLC-I and CLC-II are relatively well

estimated. Therefore a good design of the lag controller is relatively simple to realise. As an example, the dotted box in Fig. 5.7(b) shows the limits of where the gain will be located when the feedforward compensating currents are well estimated - in this case for M=2.8 is considered.

5.5 Proposed control of the dc-port voltage

In the previous section, the global and local capacitor balance control of the hybrid MMC is explained. This section presents a drive application of the hybrid MMC converter in a back-to-back MMC-based system. In this case, the grid-side converter is an hybrid MMC while the machine-side converter is a HBSM-based MMC. The hybrid MMC regulates the dc-link voltage of the back-to-back converter. The dc-link voltage is imposed to reduced the capacitor voltage oscillations during low mechanical speed in the machine-side MMC. The main advantage of this application is the reduction in the injected common-mode voltage to the machine stator.

The cell capacitors of the drive-side MMC have high voltage oscillations when operating at low mechanical speed. These voltage oscillations are due to unwanted low frequency terms in the arm power. Most of the capacitor voltage oscillations are related to the power term $\boldsymbol{p}^{\Delta}_{2\alpha\beta}$ [see (4.12)]. In particular, the second and third terms at the right-hand side of equation (4.12) produce low frequency power components that are responsible for the capacitor voltage oscillations. From (4.9) and (4.12), the capacitor voltage oscillations $v^{\Delta}_{C2\alpha\beta}$ can be referred to a dq reference frame:

$$Cv^{*}_{C}\frac{d\boldsymbol{v}^{\Delta}_{C2dq}}{dt}=\underbrace{\frac{1}{2}E\boldsymbol{i}_{2dq}-\frac{2}{3}i^{P}\boldsymbol{v}_{2dq}}_{\boldsymbol{p}_{\text{osc}}}-\underbrace{jCv^{*}_{C}\omega_{2e}\boldsymbol{v}^{\Delta}_{C2dq}}_{\boldsymbol{p}_{m}}-\underbrace{2v_{20}\boldsymbol{i}^{\Sigma}_{2dq}}_{\boldsymbol{p}_{c}} \tag{5.40}$$

Notice that the term $(\boldsymbol{v}_{2\alpha\beta}\boldsymbol{i}^{\Sigma}_{2\alpha\beta})^{c}$ [see (4.12)] does not produce low frequency oscillations. Therefore, it has been neglected in (5.40). The capacitor voltages oscillations are caused by the term $\boldsymbol{p}_{\text{osc}}$. The term $\boldsymbol{p}_{m}$ is a degree of freedom

and $\boldsymbol{p}_c$ is a controllable power term employed to cancel $\boldsymbol{p}_{\text{osc}}$.

While $\|\boldsymbol{p}_{\text{osc}}\| > \|\boldsymbol{p}_m\|$, a high-frequency current is injected to produce a controllable power term $\boldsymbol{p}_c$. This operation region is named low-frequency mode (LFM) because it happens during low mechanical speed. Conversely, when $\|\boldsymbol{p}_{\text{osc}}\| < \|\boldsymbol{p}_m\|$, the capacitor voltage oscillations are reduced and it is not necessary to inject high-frequency circulating current. While $\|\boldsymbol{p}_{\text{osc}}\| < \|\boldsymbol{p}_m\|$, the MMC is operating in high-frequency mode (HFM).

The power component $\boldsymbol{p}_{\text{osc}}$ that causes voltage oscillations during LFM can be reduced by controlling the dc-port voltage E as a function of the machine operational point. In the general case, assuming a cage machine operating with a non-negligible reactive current, the conservation of active power between the ac- and dc-ports of the machine-side converter is:

$$Ei^P = \frac{3}{2}\boldsymbol{v}_{2dq} \cdot \boldsymbol{i}_{2dq} \tag{5.41}$$

Where $\cdot$ is the dot product. By replacing (5.41) in the expression of $\boldsymbol{p}_{\text{osc}}$ from (5.40):

$$\|\boldsymbol{p}_{\text{osc}}\|^2 = \frac{E^2}{4}\|\boldsymbol{i}_{2dq}\|^2 - (\boldsymbol{v}_{2dq} \cdot \boldsymbol{i}_{2dq})^2 \left(1 - \frac{\|\boldsymbol{v}_{2dq}\|^2}{E^2}\right) \tag{5.42}$$

The equation (5.42) is convex and can be solved analytically. The influence of the dc-port voltage E over the power term $\boldsymbol{p}_{\text{osc}}$ can be studied by calculating its small-signal model:

$$\Delta\|\boldsymbol{p}_{\text{osc}}\| = \frac{\partial\|\boldsymbol{p}_{\text{osc}}\|}{\partial E}\Delta E = G_0\Delta E \tag{5.43}$$

In the previous expression, the gain G_0 is:

$$G_0 = \frac{\|\boldsymbol{i}_{2dq}\|\left(E^4 - 4\|\boldsymbol{v}_{2dq}\|^4\cos^2(\varphi_2)\right)}{2E^2\sqrt{E^4 - 4\|\boldsymbol{v}_{2dq}\|^2\cos^2(\varphi_2)(E^2 - \|\boldsymbol{v}_{2dq}\|^2)}} \tag{5.44}$$

Where $\cos(\varphi_2)$ is the power factor of the machine. Since the machine-side

converter is a HBSM-based MMC, the dc-port voltage is bounded by:

$$E{>}2\,\|\boldsymbol{v}_{2dq}\| \tag{5.45}$$

By replacing (5.45) in (5.44) it is simple to show that $G_0{>}0$. Consequently, from (5.43) a reduction in E will produce a reduction in $\|\boldsymbol{p}_{\text{osc}}\|$ that is responsible of the capacitor voltage oscillations during low mechanical speed.

Regarding the other power terms in (5.40), it is concluded that $\boldsymbol{p}_m$ is not affected by ΔE. To analyse $\boldsymbol{p}_c$ it has to be considered that the machine-side MMC is built using HBSM. Therefore, the peak of the common-mode voltage v_{20} is limited by $|v_{20}|{=}(E/2{-}\,\|\boldsymbol{v}_{2dq}\|)$ and a reduction in the dc-link voltage produces a reduction in the maximum compensating power $\boldsymbol{p}_c$ which can be provided in a particular system operating point, i.e.:

$$\Delta\boldsymbol{p}_c{=}-\,\boldsymbol{i}^{\Sigma}_{2dq0}\Delta E \tag{5.46}$$

considering this reduction in $\Delta\boldsymbol{p}_c$ and analysing (5.40) it is concluded that it is difficult to eliminate completely the mitigating currents and common mode voltage to compensate the power oscillations at extremely low speed (i.e. when $\|\boldsymbol{v}_{2dq}\|{\approx}0$ and $\omega_{2e}{\approx}0$).

The dc-port voltage is calculated to minimize the power term $\boldsymbol{p}_{\text{osc}}$. Since $\|\boldsymbol{p}_{\text{osc}}\|$ is a convex function of E, a minimum can be found:

$$E_{\text{opt}} = \sqrt{\frac{2\,(\boldsymbol{v}_{2dq}\cdot\boldsymbol{i}_{2dq})\,\|\boldsymbol{v}_{2dq}\|}{\|\boldsymbol{i}_{2dq}\|}}{=}\sqrt{2\cos(\varphi_2)}\,\|\boldsymbol{v}_{2dq}\| \tag{5.47}$$

Although (5.47) minimises the magnitude $\boldsymbol{p}_{\text{osc}}$, this expression does not take into account that a minimum dc-port voltage E_{req} is required to modulate the machine stator voltage, and, if required, the necessary common mode voltage,

which can be obtained off-line:

$$E_{\text{req}} \geq 2(\|\boldsymbol{v}_{2dq}\| + V_{20}) \tag{5.48}$$

Therefore, the imposed dc-port voltage is:

$$E^* = \min\{E_{\text{opt}}, E_{\text{req}}\} \tag{5.49}$$

Finally, the minimum feasible dc-port voltage E_{min} that an hybrid MMC can output depends on the hybridisation ratio between the FBSMs and HBSMs N_F/N_H:

$$E_{\text{min}} = v_C^* N_H \left(1 - \frac{N_F}{N_H}\right) \tag{5.50}$$

Consequently, the dc-port voltage reference $E^* \geq E_{\text{min}}$. By imposing the dc-port voltage (5.49) the magnitude of $\boldsymbol{p}_{\text{osc}}$ is minimised. Two important advantages of working with a minimal E are the reduction of the magnitude of the common-mode voltage and the duration of the LFM. As highlighted by several publications, the injection of a high frequency common-mode voltage is a standard solution in MMC for drive applications. However, high-frequency common-mode voltage induces damaged in the machine bearings [137].

5.6 Overall control system of the BTB converter

In the previous section, the cell capacitor balance control for a hybrid MMC was explained. Then, the optimal value of the dc-link voltage in a BTB MMC-based drive application was derived. This section presents the general control structure of the BTB MMC converter. The grid-side converter is implementing using a hybrid MMC, the control of this converter was explained in sections 5.2

and 5.3 but it is shown briefly here in the general control of the back-to-back converter. Then, the control of the machine-side converter is explained, this control is based on [89, 115].

The general control of the hybrid BTB MMC is shown in Fig. 5.9. The grid-side control is shown in the blue area, while the machine-side control is depicted in the green area of Fig. 5.9. In both converter sides, nested closed-loop controllers ensure the arm energy balance. The outer control layer regulates the capacitor voltage terms $V_{j\alpha\beta0}^{\Sigma\Delta}$ for the grid (j=1) and machine (j= 2) sides. Then, the outer layer provides the circulating current references to ensure the energy balance among the arms of each MMC side. In addition, the machine-side control calculates the optimum value of the dc-link voltage E according to (5.49). Then, this value is sent to the grid-side controller through a Serial Peripheral Interface (SPI). The serial communication is programmed in each FPGA as explained in the Appendix. Each converter-side control is explained below.

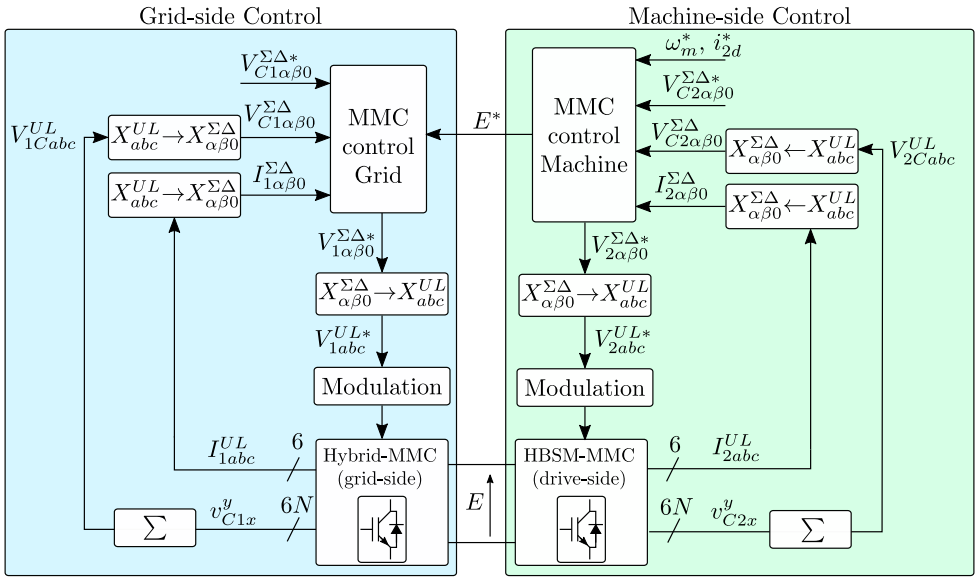


Figure 5.9: *General control of the hybrid MMC (grid-side).*

5.6.1 Control of the grid-side hybrid MMC

The global balance control of the grid-side converter is depicted in Fig. 5.10. The balance control is divided in an outer (orange area) and an inner (yellow

area) control layers. The outer voltage control regulates the total capacitor voltages $V^{\Sigma\Delta}_{C1\alpha\beta0}$ using different component of the circulating current $\boldsymbol{i}^{\Sigma}_{1\alpha\beta}$ and the direct current i_{1d}. The control of v^{Σ}_{C10} regulates the total energy of the grid-side MMC and it is controlled by adjusting the direct current i_{1d}. The remainder voltage terms of $V^{\Sigma\Delta}_{C1\alpha\beta0}$ regulate the energy balance among the six arms.

By replacing the imposed circulating current $\boldsymbol{i}^{\Sigma}_{\alpha\beta}$ in the arm power equations of the grid-side MMC it is straightforward to identify which circulating current components can be employed to regulate each total capacitor voltage terms $V^{\Sigma\Delta}_{C1\alpha\beta0}$. In particular, to regulate the capacitor voltages $\boldsymbol{v}^{\Sigma}_{C1\alpha\beta}$, $\boldsymbol{v}^{\Delta}_{C1\alpha\beta}$, and v^{Δ}_{C10} the following circulating current terms are employed $\overline{\boldsymbol{i}^{\Sigma}_{1\alpha\beta}}$, $\boldsymbol{i}^{\Sigma-}_{1dq}$, and $i^{\Sigma+}_{1d}$ respectively. The grid currents $\boldsymbol{i}_{1dq}$ are controlled in a dq reference frame using PI controllers. While the circulating currents $\boldsymbol{i}^{\Sigma}_{1\alpha\beta}$ are regulated using proportional-resonant controllers.

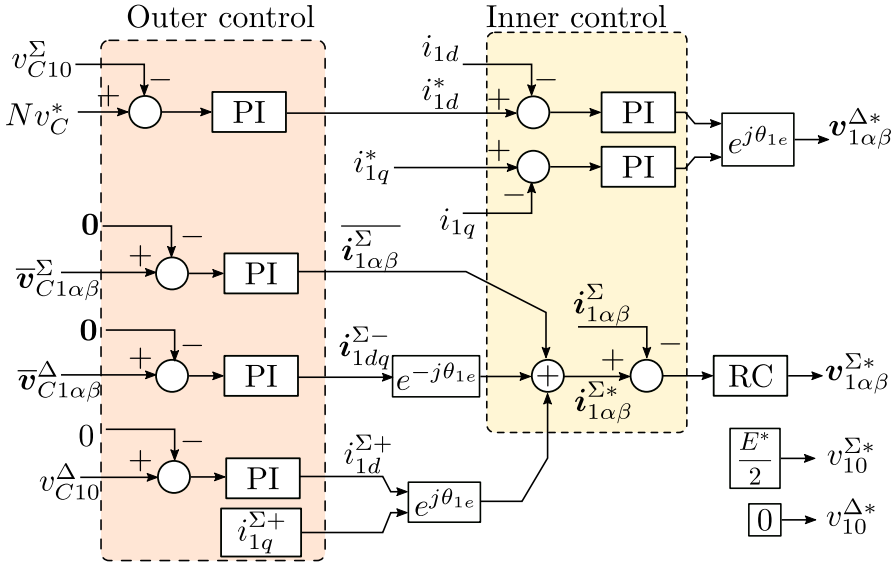


Figure 5.10: *Control of the hybrid MMC (grid-side).*

5.6.2 Control of the Machine-side MMC

The control of the machine-side converter is based on the methodology presented in [89]. The general structure of the machine control is shown in the green area of figure 5.9. As stated in the literature, high capacitor voltage os-

cillations appear during the machine start-up that are inversely proportional to the electrical frequency applied to the machine. To reduce these oscillations, a high-frequency circulating current along with a high-frequency common-mode voltage are injected.

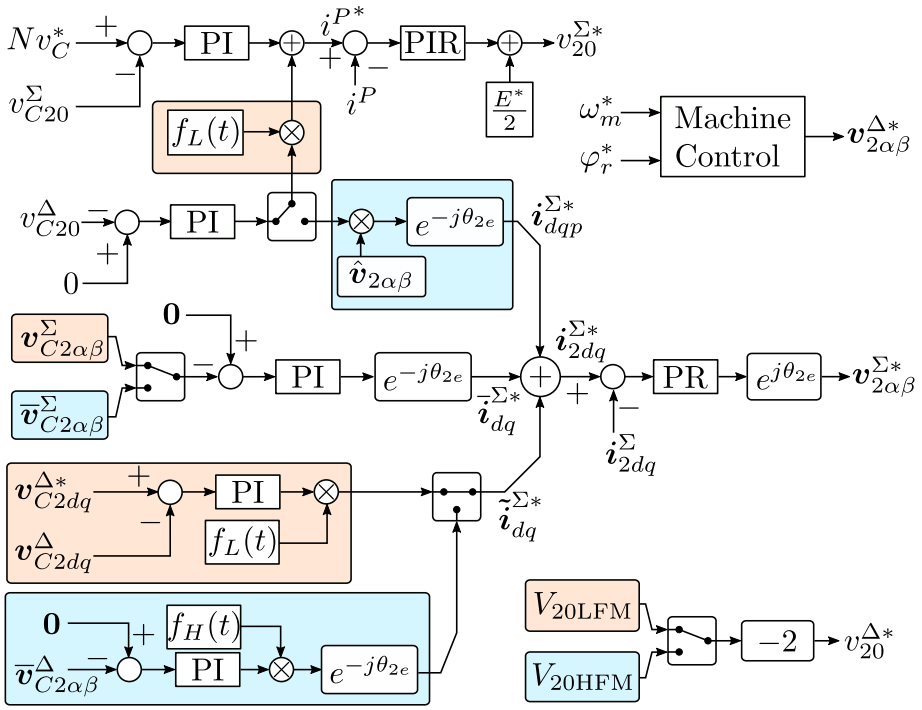


Figure 5.11: *Control of the machine-side MMC.*

To balance the MMC arms, the cell capacitor voltages are measured and the total capacitor voltages $V_{C2\alpha\beta0}^{\Sigma\Delta}$ are calculated. Then, the control shown in Fig. 5.11 regulates the arm balance and the induction machine using field oriented control. The control of $V_{C2\alpha\beta0}^{\Sigma\Delta}$ is accomplished by regulating different components of the circulating current $i_{2\alpha\beta}^{\Sigma}$ and the dc-port current i^P. The power oscillations for the machine-side MMC are:

$$\boldsymbol{p}_{2\alpha\beta}^{\Sigma} = -\frac{1}{4}(\boldsymbol{v}_{2\alpha\beta}\boldsymbol{i}_{2\alpha\beta})^c + \frac{E}{2}\boldsymbol{i}_{2\alpha\beta}^{\Sigma} - \frac{1}{2}v_{20}\boldsymbol{i}_{2\alpha\beta} \tag{5.51}$$

$$p_{20}^{\Sigma} = -\frac{1}{4}\Re\{\boldsymbol{v}_{2\alpha\beta}\boldsymbol{i}_{2\alpha\beta}^c\} + \frac{Ei^P}{6} \tag{5.52}$$

$$\boldsymbol{p}_{2\alpha\beta}^{\Delta} = -(\boldsymbol{v}_{2\alpha\beta}\boldsymbol{i}_{2\alpha\beta}^{\Sigma})^c + \frac{E\boldsymbol{i}_{2\alpha\beta}}{2} - \frac{2}{3}i^P\boldsymbol{v}_{2\alpha\beta} - 2v_{20}\boldsymbol{i}_{2\alpha\beta}^{\Sigma} \tag{5.53}$$

$$p_{20}^{\Delta} = -\Re\{\boldsymbol{v}_{2\alpha\beta}(\boldsymbol{i}_{2\alpha\beta}^{\Sigma})^c\} - \frac{2}{3}i^P v_{20} \tag{5.54}$$

It is possible to use the controllable power terms at the right-side of equations

(5.51)-(5.54), to control each voltage term of $V_{C2\alpha\beta 0}^{\Sigma\Delta}$. The machine control has 2 operational modes named as low-frequency mode (LFM) and high-frequency mode (HFM) that depend on the machine frequency. During low-mechanical speed (LFM), the MMC sub-modules have high capacitor voltage oscillations, to compensate these oscillations circulating currents along with common-mode voltage are injected. However, in HFM, the oscillations are lower and only the average value of the total capacitor voltage is regulated. During LFM, the controllers in orange boxes in Fig. 5.11 are activated. Conversely, during HFM the controllers in the blue boxes are activated. The control of each voltage term $V_{C2\alpha\beta 0}^{\Sigma\Delta}$ is explained below. These controllers are based on [89, 116].

Control of $\boldsymbol{v}_{C2\alpha\beta}^{\Delta}$

To reduce the voltage oscillations $\boldsymbol{v}_{C2\alpha\beta}^{\Delta}$, the last term of eq. (5.53) is controlled, this term is defined as $\boldsymbol{p}_{\text{control}}$:

$$\boldsymbol{p}_{\text{control}} = -2v_{20}\boldsymbol{i}_{\alpha\beta}^{\Sigma} \tag{5.55}$$

Most of the capacitor voltage oscillations are due to the power terms $\frac{1}{2}E\boldsymbol{i}_{2\alpha\beta}$ and $-\frac{2}{3}i^{P}\boldsymbol{v}_{2\alpha\beta}$, notice that the frequency of the capacitor voltage oscillations is ω_{2e}. In this work, a sinusoidal common-mode voltage and a circulating current with the same frequency are injected to regulate $\boldsymbol{p}_{\text{control}}$. Without loss of generality, the imposed common-mode voltage and circulating currents are [116]:

$$v_{20} = V_0 \sin(\omega_0 t) \tag{5.56}$$

$$\boldsymbol{i}_{\alpha\beta}^{\Sigma} = I_{\alpha\beta}^{\Sigma} e^{j(\theta_{2e}-\theta_0)} \sin(\omega_0 t) \tag{5.57}$$

The instantaneous power of the controllable term $\boldsymbol{p}_{\text{control}}$ is:

$$\boldsymbol{p}_{\text{control}} = -2v_{20}\boldsymbol{i}^{\Sigma}_{\alpha\beta} \tag{5.58}$$

$$= -2V_0 I^{\Sigma}_{\alpha\beta} e^{j(\theta_{2e}-\theta_0)} \sin^2(\omega_0 t) \tag{5.59}$$

$$= -V_0 I^{\Sigma}_{\alpha\beta} e^{j(\theta_{2e}-\theta_0)} + V_0 I^{\Sigma}_{\alpha\beta} e^{j(\theta_{2e}-\theta_0)} \cos(2\omega_0) \tag{5.60}$$

Notice that the first term $\boldsymbol{p}_{\text{control}}$ in (5.60) has a frequency equal to ω_{2e}, consequently it can be used to cancel the capacitor voltage oscillations $\boldsymbol{v}^{\Delta}_{C\alpha\beta}$. The second term has a frequency equal to $\omega_{2e}+2\omega_0$ and these oscillations are filtered out by the sub-modules capacitors.

The machine-side control has two operational modes named as low-frequency mode (LFM) and high-frequency mode (HFM). In these two operational modes, the control principle is the same than described above, i.e. the converter injected a sinusoidal common-mode voltage and a sinusoidal circulating current with the same frequency to produce a controllable power term. The only difference is the frequency and magnitude of the common-mode voltage used in each operational mode. The operational mode selected by the controller depends on the power terms $\boldsymbol{p}_{\text{osc}}$ and $\boldsymbol{p}_m$, these power terms were previously defined in (5.40) and they are shown below for clarity:

$$\boldsymbol{p}_{\text{osc}} = \frac{1}{2}E\boldsymbol{i}_{2dq} - \frac{2}{3}i^P\boldsymbol{v}_{2dq} \tag{5.61}$$

$$\boldsymbol{p}_m = jCv^*_C\omega_{2e}\boldsymbol{v}^{\Delta}_{C2dq} \tag{5.62}$$

The converter operational modes are described below:

1. **Low-frequency mode**: While $\|\boldsymbol{p}_{\text{osc}}\| > \|\boldsymbol{p}_m\|$, the converter is operating in Low-frequency mode (LFM). In this case, a sine wave common-mode voltage $v_{0\text{LFM}}$ is injected:

$$v_{20\text{LFM}} = V_{20\text{LFM}} f_L(t) \qquad f_L(t) = \sin(2\pi f_{hf} t) \tag{5.63}$$

Where f_{hf} is the frequency of the common-mode voltage. By increasing f_{hf}, the cell capacitance can be reduced [88]. However, if a high value of f_{hf} is used, the carrier frequency has to be increased accordingly to have an acceptable control accuracy over the circulating current. Consequently, if the common-mode voltage frequency is increased, the converter switching losses will increase as well. In most MMC drive applications that use standard Silicon-based MOSFET switches, the frequency f_{hf} is limited to $f_{hf}\leq$200 Hz: in [150] f_{hf}=45 Hz, in [115] f_{hf}=100 Hz, and in [159] f_{hf}=200 Hz. In this work f_{hf}=75 Hz, consequently during LFM a common-mode voltage and circulating current of frequency f_{hf}=75 Hz are injected to reduced the cell capacitor voltage oscillations.

2. **High-frequency mode**: While $\|\boldsymbol{p}_{\text{osc}}\| < \|\boldsymbol{p}_m\|$ the converter operates in HFM. During HFM, the required circulating currents and common-mode voltages are reduced in comparison with the required during LFM. In this case, the common-mode voltage is imposed as a third-harmonic of the machine voltage $\boldsymbol{v}^{\Delta}_{2\alpha\beta}$ to increase the modulation index of the machine-side MMC. By defining the electrical angle of $\boldsymbol{v}^{\Delta}_{2\alpha\beta}$ as $\theta^{\Delta}_{2\alpha\beta}$, the common-mode voltage during HFM is:

$$v_{20\text{HFM}}(t)=V_{20\text{HFM}}f_H(t) \qquad f_H(t)=\sin(3\theta^{\Delta}_{\alpha\beta}) \tag{5.64}$$

In most MMC-based drive control strategies, the capacitor voltage oscillations are driven to zero [36, 115, 116]. This is equivalent to set $v^{\Sigma*}_{2C0}=Nv^{*}_{C}$ and $v^{\Sigma*}_{2C\alpha}=v^{\Sigma*}_{2C\beta}=v^{\Delta*}_{2C\alpha}=v^{\Delta*}_{2C\beta}=v^{\Delta*}_{2C0}=0$. However, if a capacitor voltage band is permitted, the required circulating current will be lower. In this thesis, the same approach as [89] was adopted, during LFM the capacitor voltage reference $\boldsymbol{v}^{\Delta}_{C2dq}$ are calculated as (5.65), where $\tilde{v}_C$ is the allowed capacitor voltage

oscillations.

$$\left\|\boldsymbol{v}_{C2dq}^{\Delta*}\right\| = 2(\tilde{v}_C - \left\|\boldsymbol{v}_{C2\alpha\beta}^{\Sigma}\right\|) \tag{5.65}$$

Control of $\boldsymbol{v}_{C2\alpha\beta}^{\Sigma}$

Regardless of the operational mode, to regulate the voltage term $\boldsymbol{v}_{C2\alpha\beta}^{\Sigma}$, a dc-component of the circulating current $\overline{\boldsymbol{i}_{2\alpha\beta}^{\Sigma}}$ is employed [see eq. (5.51)]. The only difference is that during HFM, the total capacitor voltages $\boldsymbol{v}_{C2\alpha\beta}^{\Sigma}$ are filtered out to remove the oscillatory component.

Control of v_{C20}^{Σ} and v_{C20}^{Δ}

The voltage term v_{C20}^{Σ} regulates the total energy of the MMC. According to (5.52), by regulating the current $\overline{i^P}$ it is possible to modify p_{20}^{Σ}.
Regarding the control of v_{C20}^{Δ}, during LFM an oscillatory component of i^P is used to produce a controllable power term with the common-mode voltage [see (5.54)]. Conversely, during HFM a circulating current in phase with the machine voltage $\boldsymbol{v}_{2\alpha\beta}$ is used to regulate v_{C20}^{Δ}.

5.7 Summary

This chapter explains the proposed control of the hybrid MMC and the back-to-back system. The global capacitor control of a hybrid MMC and a HBSM-based MMC shares the same structure. In both cases, the energy of the 6 arms belonging to each MMC are controlled through the total voltages terms v_{C0}^{Σ}, v_{C0}^{Δ}, $\boldsymbol{v}_{C\alpha\beta}^{\Sigma}$, and $\boldsymbol{v}_{C\alpha\beta}^{\Delta}$. The total energy of the 6 arms is controlled through v_{C0}^{Σ}, while the balance between the converter arms is regulated using $\boldsymbol{v}_{C\alpha\beta}^{\Sigma}$, and $\boldsymbol{v}_{C\alpha\beta}^{\Delta}$. The outer control layer define the references for the circulating currents $\boldsymbol{i}_{\alpha\beta}^{\Sigma}$, in particular different components of the circulating current are use to

ensure the balance among arms. The total energy is controlled differently depending on the load connected. For the hybrid MMC working as a front-end converter, the control of the total energy regulates the direct current i_d. Whereas, for an MMC driving an electrical machine, the dc-link current i^P controls its total arm energy.

Next, this chapter discusses some critical aspects for each converter side. Regarding the hybrid MMC, the control must balance the capacitor voltage of the FBSMs and HBSMs while the converter operates in over-modulation. This thesis proposes two methods to ensure the local balance. In the first one (CLC-I), the local balance reduces the power factor to balance FBSMs and HBSMs. The minimum magnitude of the reactive current is calculated to ensure the capacitor voltage balance between the FBSMs and HBSMs. However, it is not allowed to operate with a low power factor in most industrial applications; consequently, a second strategy is presented. The second control strategy (CLC-II) injects a circulating current within the converter to ensure to have bipolar arm currents. In both cases, the minimum required compensating current is derived as a function of the cell capacitor voltage, the direct current i_d, and the hybridisation ratio of the hybrid MMC. Since it is possible to have parameters mismatch between the theoretical values and the actual ones in the real system, a closed-loop controller is derived to ensure the local balance. Finally, the control of the back-to-back MMC for a drive application is discussed. In this case, the optimal value for the dc-link voltage is derived. Moreover, the control of the machine-side converter is also explained. The machine-side control has 2 operational modes that depend on the machine speed named low-frequency and high-frequency modes. In low frequency mode, the controller injects common-mode voltage to the machine stator and high-frequency circulating currents to balance the flaoting capacitor. It is shown that the common-mode voltage along with the duration of the low-frequency mode is reduced when the optimal value of the dc-link voltage is used.

In the next chapter, the proposed controllers are evaluated through simulation

results of an hybrid MMC and a back-to-back MMC-based drive converter.

Chapter 6

Simulation results

This chapter presents full-scale simulations of a hybrid MMC working in the over-modulation region (m>2). The performance of the 2 proposed local balance strategies CLC-I and CLC-II is demonstrated for several cases. As explained before, the local balance control ensures that the arm energy is evenly shared between the HBSMs and the FBSMs within each arm. Firstly, the operation of an individual hybrid MMC is considered and then a back-to-back hybrid MMC is considered. The steady-state and transient responses are shown. In particular, the following tests are considered:

1. Unbalanced operation of the hybrid MMC: The aim of this test is to show the capacitor voltage unbalance between the HBSMs and the FBSMs that results when the hybrid MMC operates in over-modulation without any compensation strategy. In this case, only the standard global balance control is enabled.

2. Local balance control strategy: In this section, the operation of the local balance control is demonstrated. Both of the proposed control strategies CLC-I and CLC-II are validated.

3. Operation of the closed-loop local voltage control: In this case, the operation of the closed-loop voltage control is tested when the feed-forward compensating current is under-estimated. Since the feed-forward cur-

rents were derived using the converter model, in a real application some mismatch may exist due to the component tolerance and perturbations.

4. Step-load impact: The transient response of the control is tested for a step change in the load power for both the CLC-I and CLC-II strategies.

5. Drive application case I: In this case, a back-to-back system is considered to feed an induction machine. The front-end converter is a hybrid MMC while the machine-side converter is a HBSM-based MMC. In particular, it is shown that by regulating the dc-link voltage according to (5.49) it is possible to reduce the magnitude of the injected common-mode voltage in the machine stator. In addition, the duration of the low-frequency operation it is also reduced.

6. Drive application case II: In this case a back-to-back drive system is also considered. In particular it is shown that the cell capacitance of the machine-side MMC can be reduced by operating with a reduced dc-link voltage. As explained in the literature review, the cell capacitance of an MMC-based drive converter is considerably greater than that of an MMC for HVDC applications due to the energy pulsation produced in the MMC arms during low speed operation. [36, 89, 115, 116].

6.1 Unbalance between the HBSMs and FBSMs

Firstly, the imbalance problem between the HBSMs and FBSMs is shown. In this case, a resistive load is connected to the dc-port. Initially, the modulation index is m=1.7 and it is increased up to m=2.5 with the local balance control disabled. However, the arm energy balance control is activated and therefore the total arm energy is evenly shared. The hybrid MMC is feeding a resistive load with a power P_L=3MW for m=1.7. In this case, a medium-voltage grid is considered V_g=6.9 kV (rms). The number of cells along with the arm

inductance are chosen using method discussed in section 4.4.3. In particular, the THD in the output currents is lower than 1% under full-power operation. The sub-module capacitor voltage v_C^* is given by:

$$V_C^* = k_{\max} \frac{2V_g}{m_0} \tag{6.1}$$

In this case, m_0=1 and $k_{\max}$=1.25 to ensure enough voltage margin during the transient response, consequently, v_C^*=2084 V. In addition, the converter time constant τ_{MMC}, i.e. the ratio between its stored energy and its rated power is 76 ms, where the time constant is calculated as:

$$\tau_{\text{MMC}} = \frac{6 \cdot N \cdot \frac{1}{2} C \cdot v_C^2}{P_{\text{rated}}} \tag{6.2}$$

The main parameters of the hybrid MMC are shown in Table 6.1.

Table 6.1: Simulation parameters for the hybrid modular multilevel converter.

Parameter	Description	Value
P	Rated power	3 MW
E	Rated dc-link voltage	11.7 kV
N_H	Number of HBSMs per arm	4
N_F	Number of FBSMs per arm	3
N	Number of cells per arm	7
V_g	Grid voltage (line-to-line RMS)	6.9 kV
v_C^*	Sub-module voltage reference	2084V
f_c	Carrier frequency	5kHz
L	Arm inductance	3.5 mH
C	Sub-module capacitance	2.5 mF

The capacitor voltages of the upper arm of phase a are shown in Fig. 6.1(a), and the modulation index is shown in Fig. 6.1(b). In this case, once the modulation index reaches the threshold m=2, the capacitor voltages of the FBSMs and the HBSMs start to drift apart. In particular, the capacitor voltage of the FBSMs increase while the capacitor voltage of the HBSMs decrease. After t=6 s, the voltage difference between the FBSMs and the HBSMs is 997 V. Although it is possible to operate the converter with unbalanced cell voltages, if the arm currents remain unipolar, the FBSMs and HBSMs voltage difference

will continuously increase until the over-voltage protection is triggered. Consequently, it is necessary to ensure a balanced operation of the HBSMs and FBSMs. In addition, in this test, the FBSMs capacitor voltages increase while the HBSMs voltages decrease due to the sign of the power flow. If the hybrid MMC was working as an inverter, the opposite would happen.

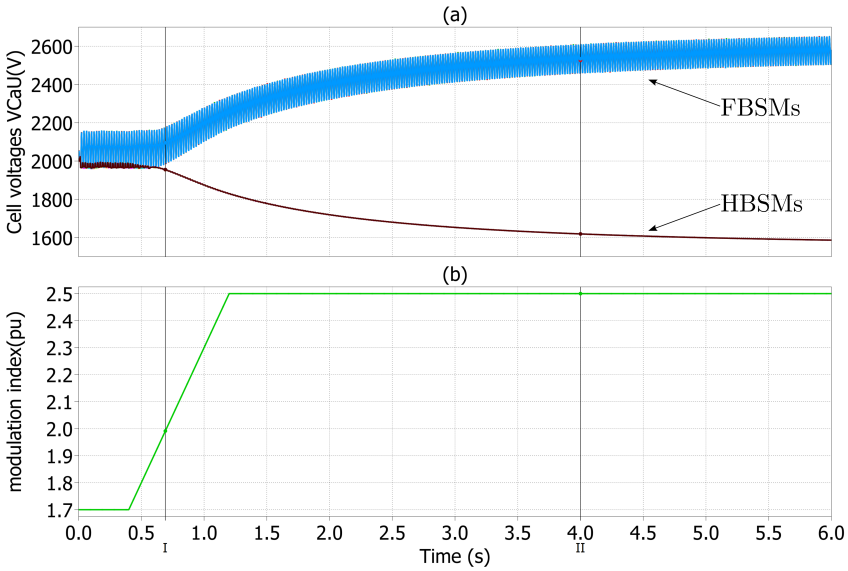
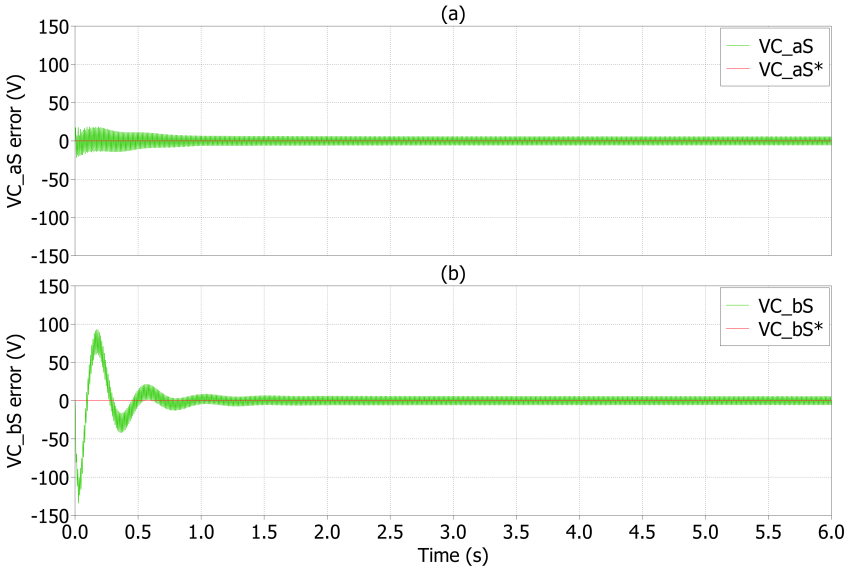


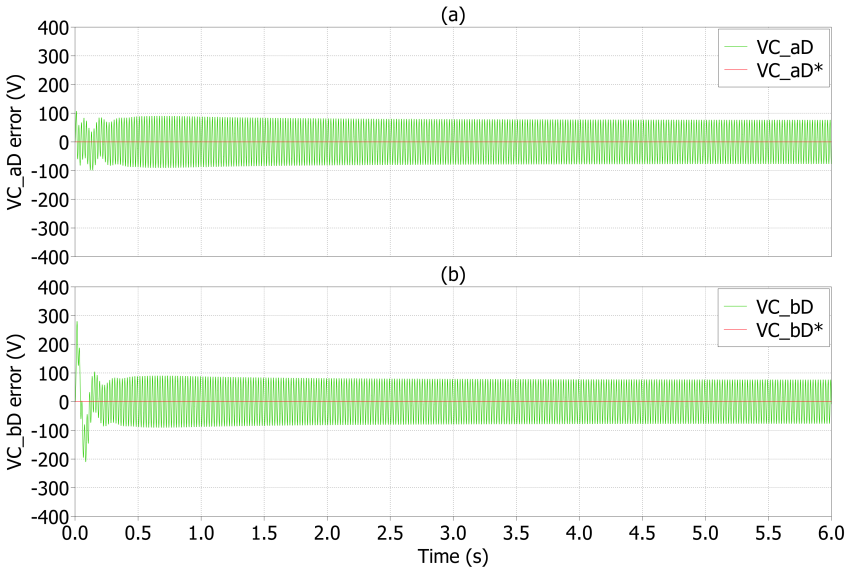
Figure 6.1: *(a) sub-module capacitor voltages of the upper arm of phase a. (b) modulation index m.*

In the test discussed above the arm energy balance control is activated. Consequently, during the entire test, the system is able to evenly balance the total arm energy of the hybrid MMC, even though the local balance control is not enabled. The capacitor voltage errors in the $\Sigma\Delta\alpha\beta 0$ reference frame are shown next. The capacitor voltage errors of the vectors $\boldsymbol{v}_{C\alpha\beta}^{\Sigma}$ and $\boldsymbol{v}_{C\alpha\beta}^{\Delta}$ are depicted in figures 6.2a and 6.2b respectively, and are shown to converge to zero. As explained in chapter 5, the total voltage references $\boldsymbol{v}_{C\alpha\beta}^{\Sigma}$, $\boldsymbol{v}_{C\alpha\beta}^{\Delta}$, and v_{C0}^{Δ} regulate the energy balance between the 6 arms and consequently they are set to zero. In steady-state operation, the capacitor voltage error is bounded by $\left\|\boldsymbol{v}_{C\alpha\beta}^{\Sigma}\right\|$ <6 V and $\left\|\boldsymbol{v}_{C\alpha\beta}^{\Sigma}\right\|$ <75 V. All the capacitor voltage terms $\boldsymbol{v}_{C\alpha\beta}^{\Sigma}$, $\boldsymbol{v}_{C\alpha\beta}^{\Delta}$, v_{C0}^{Δ} are negligible since the total energy per arm is balanced. As explained in chapter 4 [see section 4.2.1], the voltage terms $\boldsymbol{v}_{C\alpha\beta}^{\Delta}$ and v_{C0}^{Δ} are related with the balance between the upper and lower arms, while the voltage term $\boldsymbol{v}_{C\alpha\beta}^{\Sigma}$

regulates the arm balance between different phases.



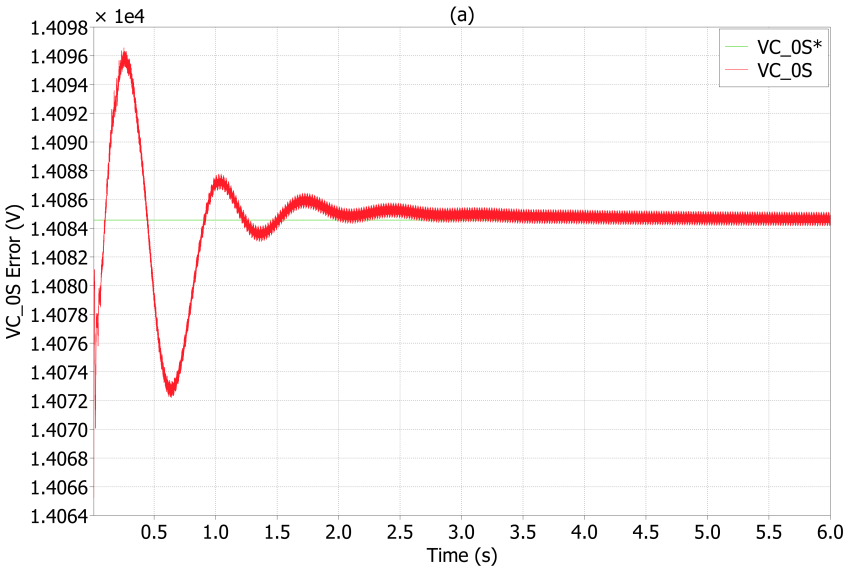
(a) *Capacitor voltage error* $v_{C\alpha}^{\Sigma}$.



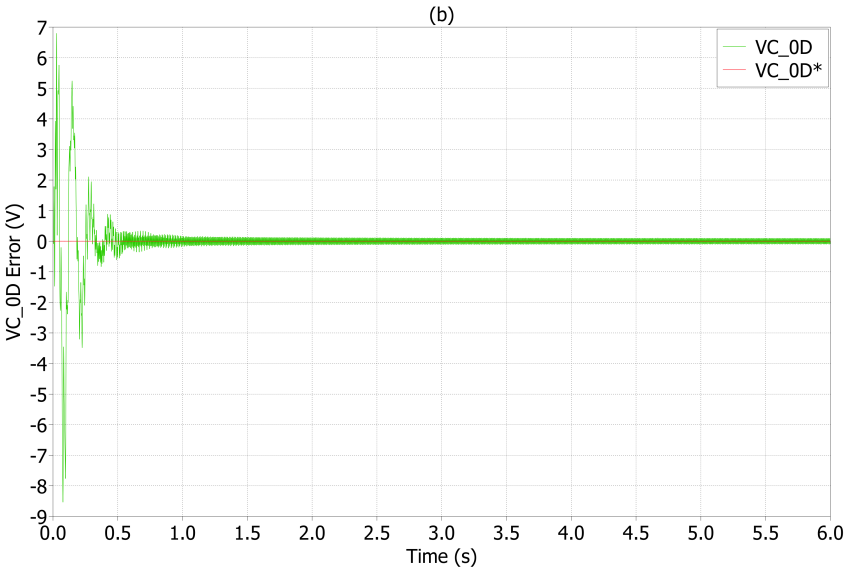
(b) *Capacitor voltage error* $v_{C\beta}^{\Sigma}$.

Figure 6.2: *Capacitor voltage error* $\boldsymbol{v}_{C\alpha\beta}$.

The capacitor voltage errors v_{C0}^{Σ} and v_{C0}^{Δ} are shown in figures 6.3a and 6.3b respectively. The voltage term v_{C0}^{Σ} regulates the average value of the total capacitor voltages of the 6 arms. In this case, a feed-forward term is added to the control of v_{C0}^{Σ} to take into account any load power change in the dc-port. In steady-state, the capacitor voltage errors are bounded by $|v_{C0}^{\Sigma}|$<11.2 V and $|v_{C0}^{\Delta}|$<0.11 V. So it is shown that even though the energy is evenly shared among the 6 arms, within each arm the FBSMs and HBSMs cells are unbalanced.



(a) *Capacitor voltage error* v_{C0}^{Σ}.



(b) *Capacitor voltage error* $v_{C\beta}^{\Sigma}$.

Figure 6.3: *Capacitor voltage error* v_{C0}^{Δ}.

The dc-link voltage E, along with the modulation index m for this test are shown in Fig. 6.4(a) and (b) respectively. The FBSMs and HBSMs capacitor voltages start to unbalance once the dc-link voltage is lower than E=5.6 kV. The unbalance problem is created because the arm currents become unipolar and do not cross zero. The arm current i_a^U is shown in Fig. 6.5. In this case, once the modulation index reaches the value m=2, it is clear that the arm current becomes unipolar. In particular, while m>2, the arm currents are strictly negative. If the converter was operating as a inverter, the arm currents would become strictly positive.

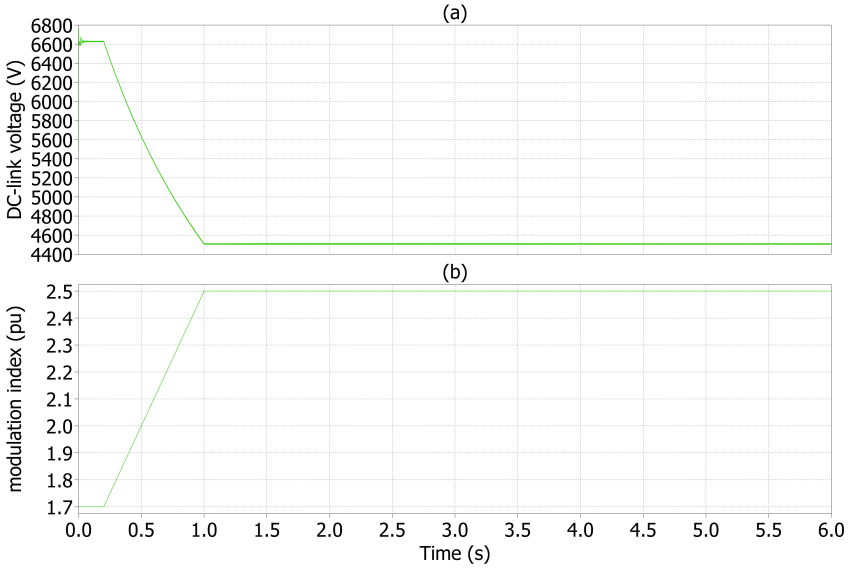


Figure 6.4: *(a) DC-link port voltage E. (b) modulation index m.*

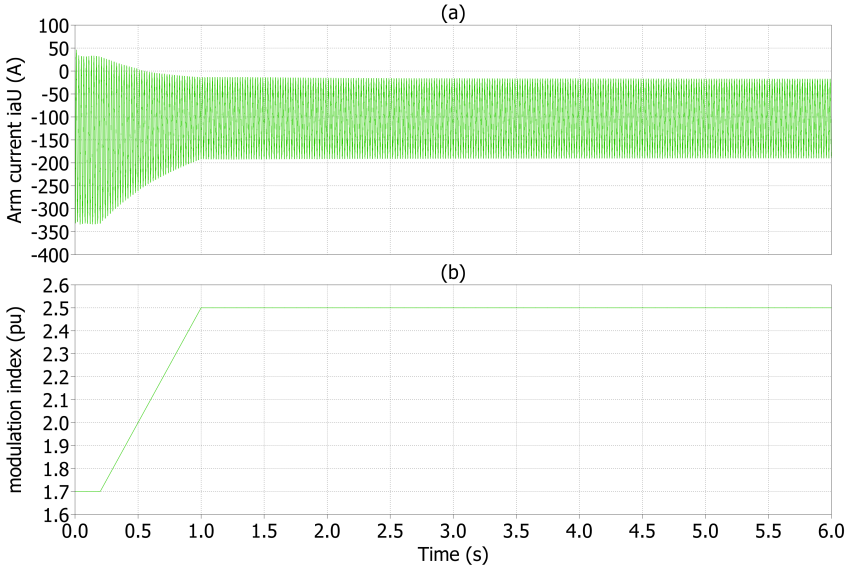


Figure 6.5: *(a) Arm current i_a^U (upper arm of phase a). (b) modulation index m.*

The grid currents in dq coordinates are shown in Fig.6.6. As explained before, the control system is able to properly regulate the direct and quadrature grid currents because the energy balance between the arms is still effective.

The circulating currents are shown in Fig.6.7. In steady-state they are negligible with a peak value of 4.3 A.

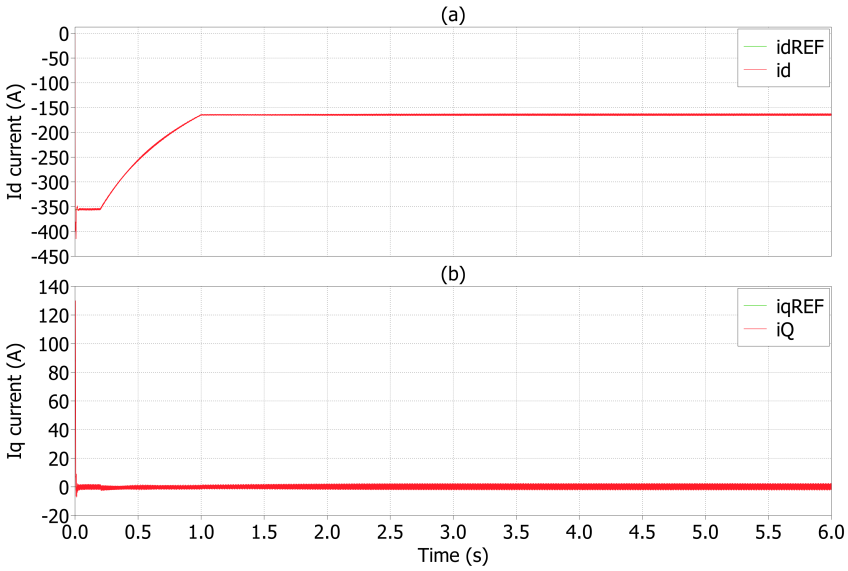


Figure 6.6: *(a) Grid direct current. (b) Grid quadrature current.*

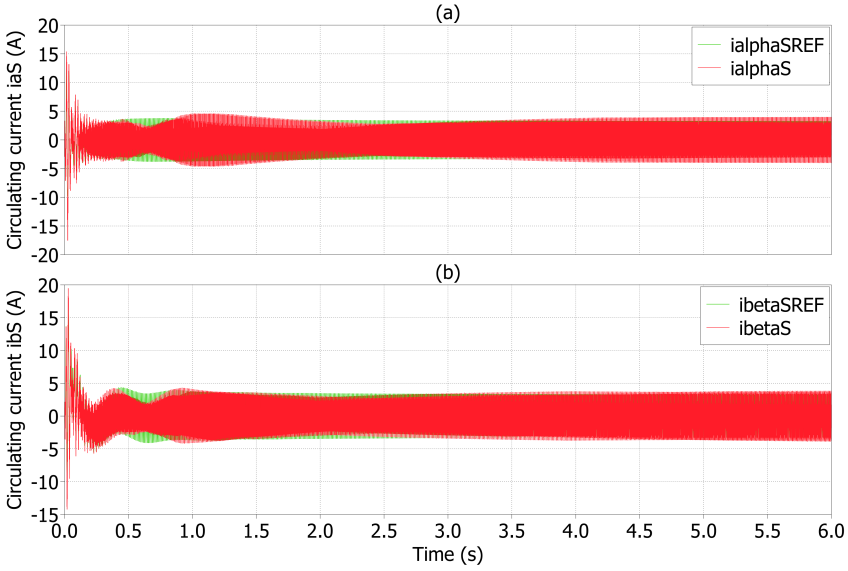


Figure 6.7: *Control of the circulating current in the $\alpha\beta$ reference frame (a) i_{α}^{Σ} and (b) i_{β}^{Σ}.*

6.2 Performance of local balance control strategies

This section demonstrates the operation of the 2 proposed strategies (CLC-I and CLC-II) to ensure the local balance between the HBSMs and the FBSMs. A resistive load is connected to the dc-link port, in this test the modulation index is ramped from m=1.7 to m=2.5. The load power is 3 MW for m=1.7. The capacitor voltages of the sub-modules of the hybrid MMC are shown in figure

6.8 when i_q>0 is considered, in this case CLC-I is employed. In steady-state operation, the capacitor voltage oscillations are less than 176 V. As explained in section 5.3.3, the same result is achieved if i_q<0 is considered. The main difference is that when a positive reactive current is employed the converter has a higher available voltage margin than that available with negative reactive current.

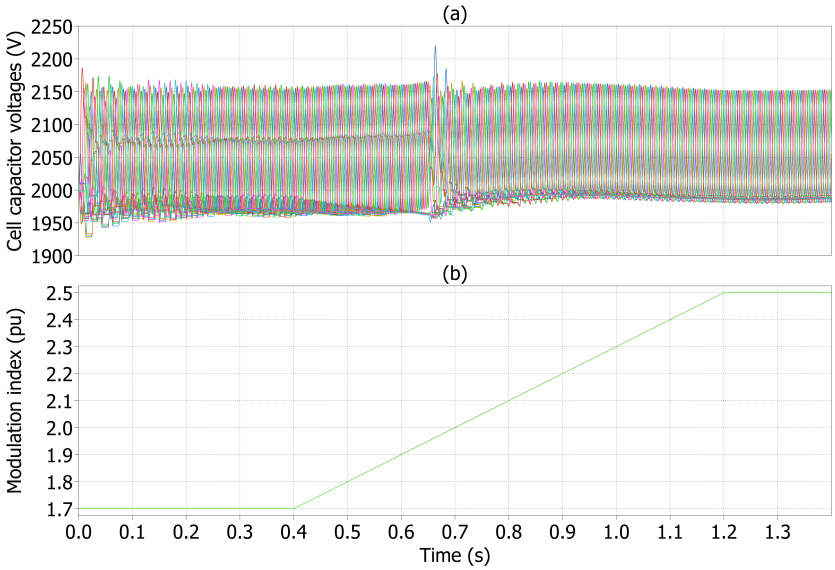


Figure 6.8: *Floating capacitors of the hybrid MMC when the modulation index is varied from* m=1.7 → 2.5 *using CLC-I.*

When i_q<0, the cell capacitor voltages are shown in Fig. 6.9. As expected, the control system is still able to balance both FBSMs and HBSMs. In this case, the capacitor voltage oscillations are 207 V in steady-state operation.

The previous results show that the proposed control strategy CLC-I is able to keep the capacitor voltage balance between the HBSMs and FBSMs during over-modulation.

In order to demonstrate the effectiveness of the optimisation to calculate the feed-forward current needed to ensure the capacitor voltage balance between FBSMs and HBSMs, the following results illustrate what happens if the feed-forward current is in error. For this illustration, the feed-forward current is artificially reduced to 90% of the calculated optimum value. As shown in Figure 6.10, the FBSM and HBSM capacitor voltages start to diverge when

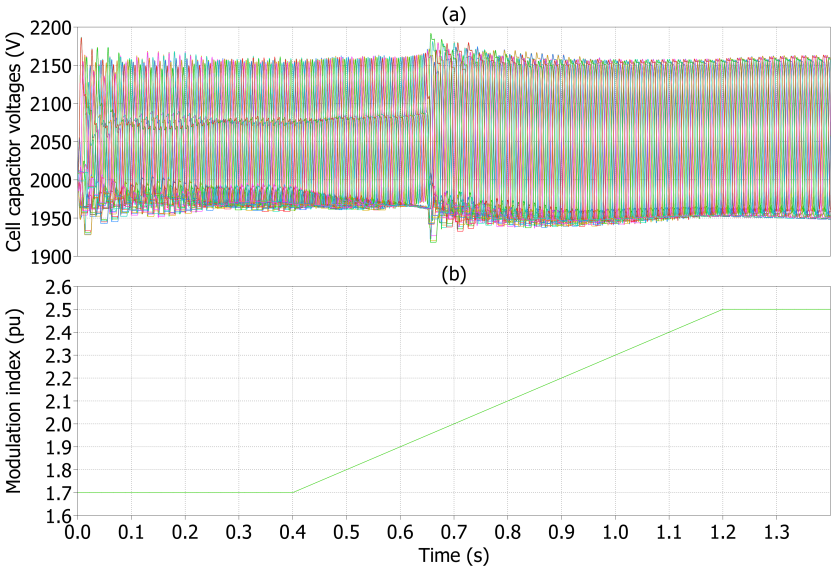


Figure 6.9: *Floating capacitors of the hybrid MMC when the converter operates in over-modulation with CLC-I and with a negative power factor.*

m=2.4 and operation over the entire range is not possible.

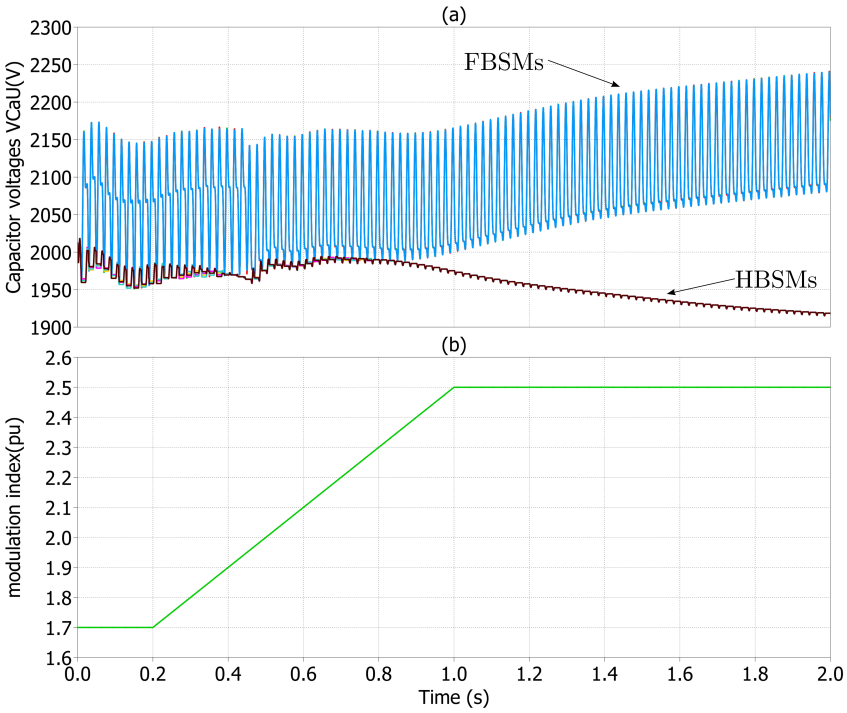


Figure 6.10: *Floating capacitors of the hybrid MMC when the converter operates in over-modulation with CLC-I and with a positive power factor. Only* 90% *of the theoretical feed-forward current is considered.*

The grid currents in the *dq* reference frame are shown in figure 6.11. As the modulation index increases, the power factor is reduced as shown in table 6.2. Despite the proposed CLC-1 strategy ensuring local balance, it results in a low

power factor. For instance, for a modulation index m=2.5 the power factor is only 0.71.

Table 6.2: Reactive current and power factor as a function of the modulation index and direct current when CLC-I is used.

Modulation index m	i_d (A)	i_q (A)	Power factor	Load power(MW)
2.1	233.8	160.7	0.82	2.0
2.2	212.2	162.2	0.8	1.8
2.3	193.1	162.0	0.77	1.6
2.4	177.0	161.5	0.73	1.5
2.5	164.1	160.7	0.71	1.4

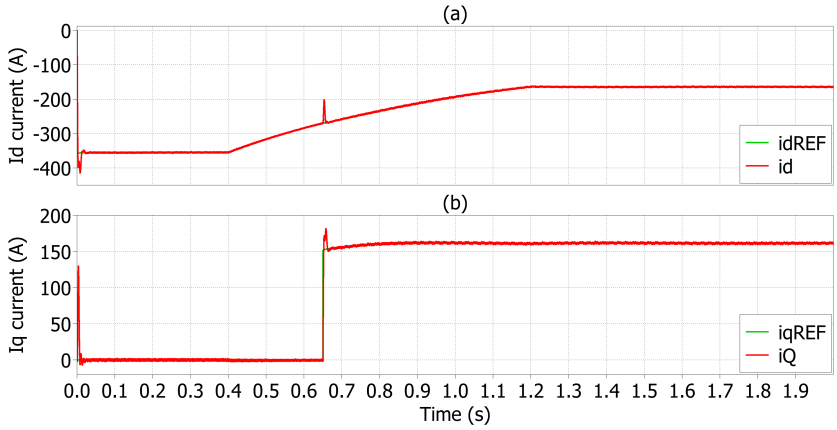


Figure 6.11: *Direct and quadrature grid currents when the modulation index is varied from m=1.7 to m=2.5 with CLC-I.*

The circulating currents are shown in figure 6.12. Once the steady-state is reached, the magnitudes of the circulating currents are 3.8 A. In this case, the circulating currents are used to ensure the energy balance between each arm. Since the grid frequency is high (f_1=50 Hz) and it remains constant, the arm energy pulsations are low and consequently the required circulating currents are small as well.

The arm currents are shown in figure 6.13, during the modulation index sweep, illustrating that the CLC-I strategy ensures bipolar arm currents. In steady-state operation, when the converter operates at m=2.5, the control system injects a reactive current equal to 160.7 A. In this case, the arm current has average and peak values equal to −102.6 A and 114.4 A respectively.

The grid currents in natural coordinates for different modulation indexes are

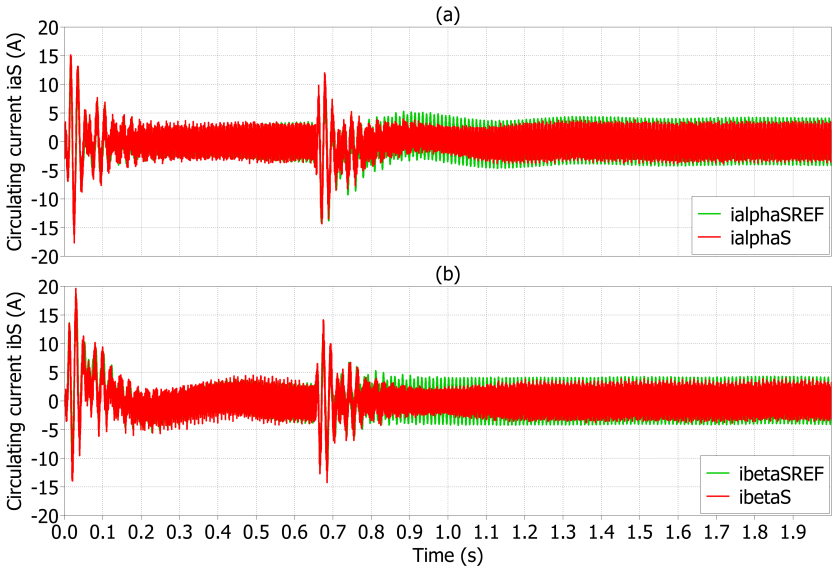


Figure 6.12: *Circulating currents* $i^{\Sigma}_{\alpha\beta}$ *when the modulation index is varied from* m=1.7 *to* m=2.5 *with CLC-I.*

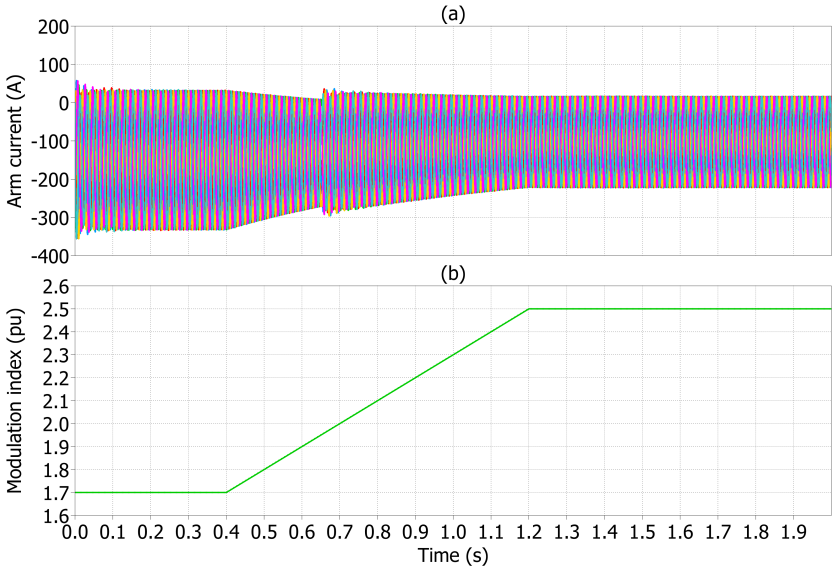


Figure 6.13: *Arm currents* i^{y}_{x} *with* $x\in\{a,b,c\}$ *and* $y\in\{U,P\}$ *when the modulation index is varied from* m=1.7 *to* m=2.5 *with CLC-I.*

shown next. The currents I_{abc} for the initial modulation index m=1.7 are plotted in figure 6.14, in this case the harmonic distortion is THD=0.3%. Once, the modulation index is greater than m=2, the control system increases the magnitude of the reactive current, as shown in figure 6.15. Finally, once the modulation index reaches m=2.5 the currents are shown in figure 6.16, the harmonic distortion of the grid current is THD=0.5%.

The performance of the hybrid MMC when the CLC-II strategy is employed is discussed next. In this case, the grid operates with unity power factor and

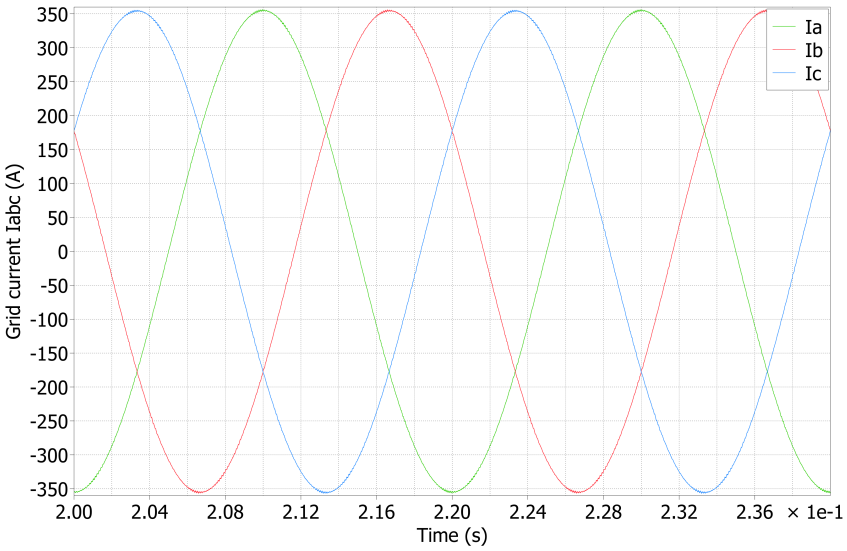


Figure 6.14: *Grid currents I_{abc} for the initial modulation index m=1.7 (CLC-I).*

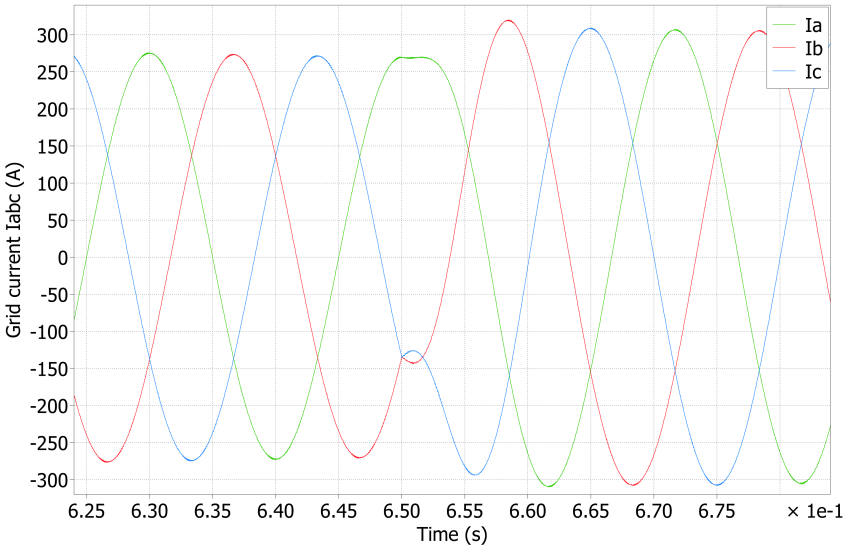


Figure 6.15: *Grid currents I_{abc} when the modulation index reaches m=2 (CLC-I).*

an additional circulating current component is injected to ensure the local balance between the FBSMs and HBSMs during over-modulation. The same modulation sweep as the previous test is considered. The capacitor voltages of all the sub-modules are shown in figure 6.17 when a negative polarity $i_q^{\Sigma+}$<0 is considered. As explained in section 5.3.2, the strategy CLC-II increase the magnitude of the circulating current to ensure the local balance. In particular, this is done by increasing the magnitude of $i_q^{\Sigma+}$. In this case, the capacitor voltage oscillations are less than 221 V.

If a positive value of $i_q^{\Sigma+}$ is used, the control performance is similar to that

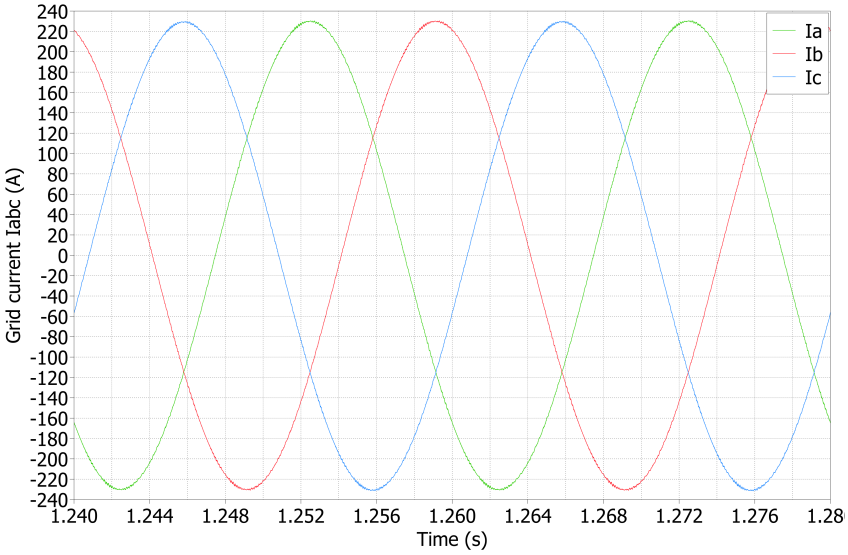


Figure 6.16: *Grid currents I_{abc} for a modulation index m=2.5 (CLC-I).*

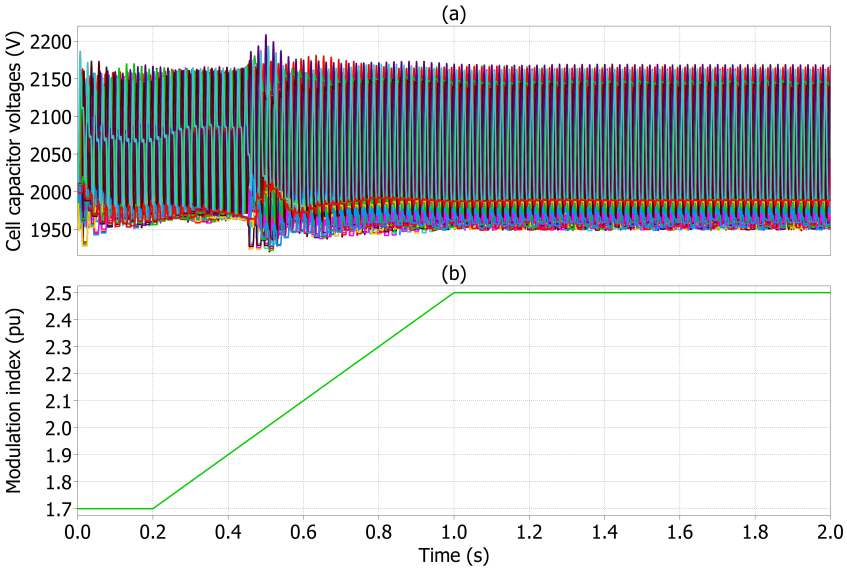


Figure 6.17: *Cell capacitor voltages for a modulation index sweep m=1.7 → 2.5 while CLC-II is used with $i_q^{\Sigma+}$<0.*

shown in the previous case. The capacitor voltages along with the modulation index are shown in Fig. 6.18(a) and (b) respectively for $i_q^{\Sigma+}$>0. In this case, the capacitor voltage oscillations are lower than 219 V.

In addition, to probe the accuracy of the proposed optimization method, an error is introduced in the feed-forward circulating current reference $i_q^{\Sigma+}$. The cell capacitor voltages of the upper arm of phase a are shown in figure 6.19 when the feed-forward term is reduced by 10%. Since the feed-forward current is less than that calculated to ensure the capacitor voltage balance, the FBSMs

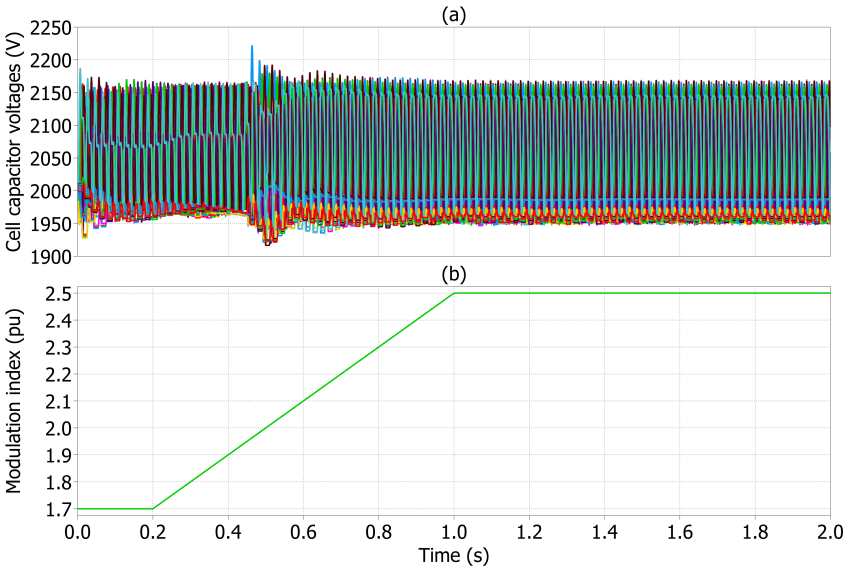


Figure 6.18: *Cell capacitor voltages for a modulation index sweep* m=1.7→2.5 *while CLC-II is used with* $i_q^{\Sigma+}$>0.

and HBSMs capacitor voltages drift apart.

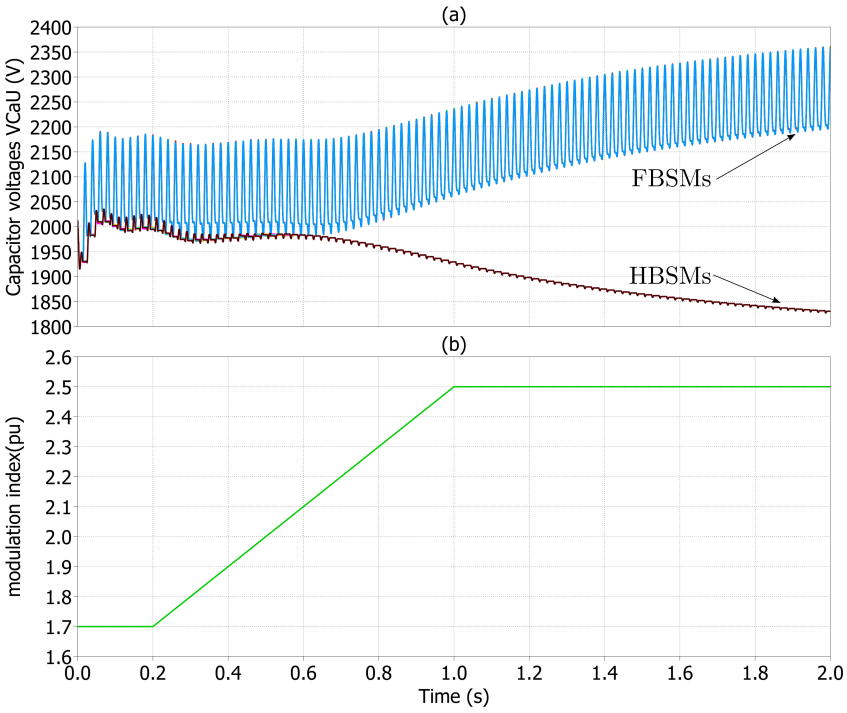


Figure 6.19: *Cell capacitor voltages if the feed-forward term is reduced by* 10% *of its theoretical value when CLC-II is used.*

The grid currents are shown in fig 6.20. Notice that the converter is able to operate with unity power factor, this is an important advantage with respect to CLC-I.

The circulating currents $\boldsymbol{i}_{\alpha\beta}^{\Sigma}$ are plotted in figure 6.21. Once the modulation

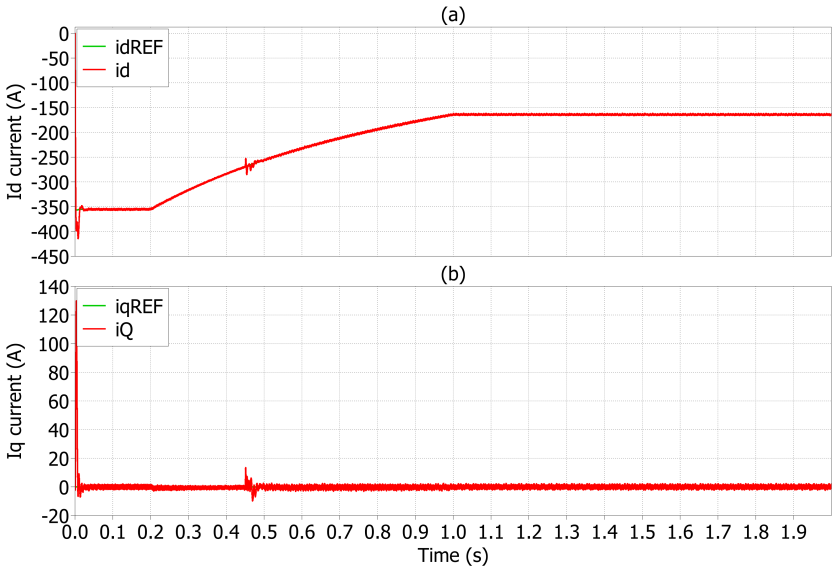


Figure 6.20: *Grid currents* $\boldsymbol{i}_{dq}$ *when the modulation index is swept from* m=1.7 *to* m=2.5 *and the local balance is accomplished by using CLC-II.*

index is higher than m>2, the reference of the circulating current component $i_q^{\Sigma+}$ is increased to maintain the local balance. Once the steady-state operation is reached, the magnitude of the circulating current component $i_q^{\Sigma+}$ is 89.3 A. In addition, the transient response of the resonant controller of the circulating currents is shown in fig. 6.22.

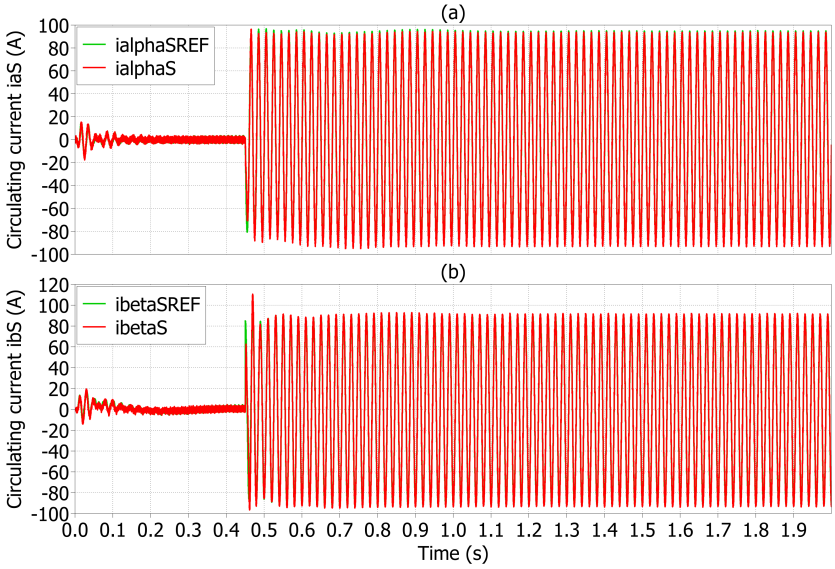


Figure 6.21: *Circulating currents* $\boldsymbol{i}_{\alpha\beta}^{\Sigma}$ *while the modulation index is swept from* m=1.7 *to* m=2.5 *using CLC-II.*

The arm currents are shown in figure 6.23. By imposing the circulating current component $i_q^{\Sigma+}$, the arm currents are bipolar during the whole test. In steady-

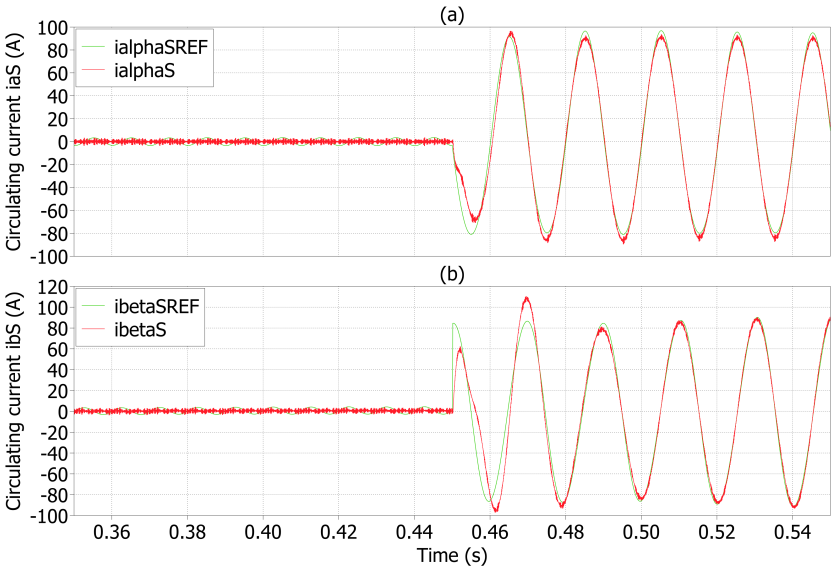


Figure 6.22: *Zoom view of* $\boldsymbol{i}_{\alpha\beta}^{\Sigma}$ *while the modulation index is swept from* m=1.7 *to* m=2.5 *using CLC-II.*

state for m=2.5, the mean and peak value of the arm currents are −102 A and 126.1 A respectively, consequently the maximum and minimum arm currents are 24.1 A and −228.1 A respectively.

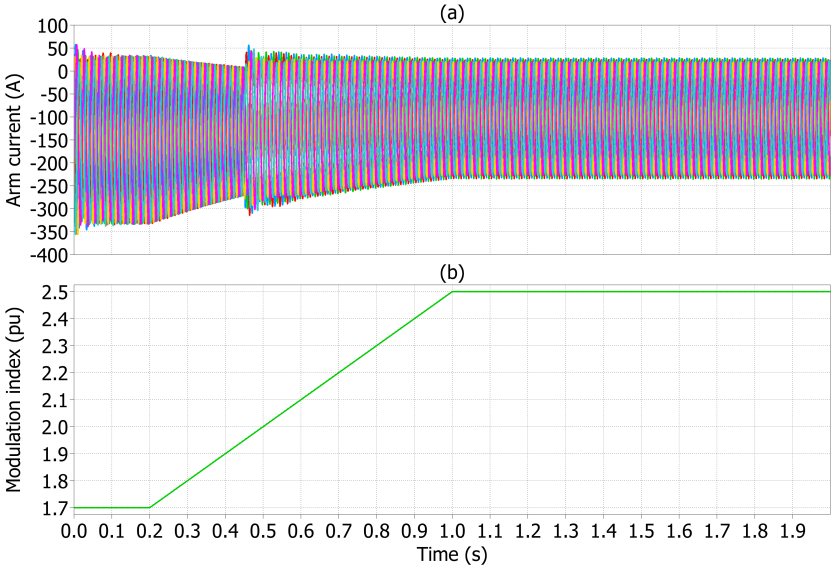


Figure 6.23: *Arm currents while the modulation index is swept from* m=1.7 *to* m=2.5 *using CLC-II.*

6.3 Performance of the closed loop HBSM/FBSM voltage difference controller

In this test, the performance of the closed-loop voltage controller is shown when the modulation index is m=2.5. The converter is operating in over-modulation and the feed-forward current term is reduced to half of its theoretical value at t_1=1 s. While the compensating current is lower than required, the FBSM and HBSM capacitor voltages start to drift apart. Then, after Δt=0.5 s, the outer local balance control is activated and the cells capacitor voltages balance again.

Figures 6.24-6.27 show the controller performance when CLC-I is used, i.e. the control reduces the grid power factor to ensure the voltage balance between the HBSMs and FBSMs. The sub-module capacitor voltages are shown in fig. 6.24. Once the reactive current reference is reduced to half of its original value, the FBSM capacitor voltages increase while the capacitor voltage of the HBSMs are reduced. After Δt=0.5 s, the average value of the FBSM capacitor voltage is 2.2 kV while for the HBSMs it is 1.8 kV. At t_2=1.5, the closed-loop control is activated and the FBSMs and HBSMs become balanced again. The floating capacitors of both sub-modules are balanced after Δt=160 ms. After balance is achieved, the capacitor voltage oscillations are the same as before the transient test at Δv_c=178 V.

The grid currents are shown in figure 6.25. Initially, the reactive current is i_q^*=161.6 A. Then, it is reduced to i_q^*=80.7 A and, as a consequence, the FBSMs and HBSMs capacitor voltages start to drift apart. The reactive current is limited to I_{qmax}=200 A, once in steady state, the reactive current reference is i_q^*=156.4 A. In steady-state, the power factor is 0.7 (capacitive).

The circulating currents $\boldsymbol{i}_{\alpha\beta}^{\Sigma}$ during the transient test are shown in fig. 6.26. As expected, the circulating currents are negligible, since CLC-I does not rely on them to ensure the local balance.

The error between the mean value of the HBSM and FBSM capacitor voltages,

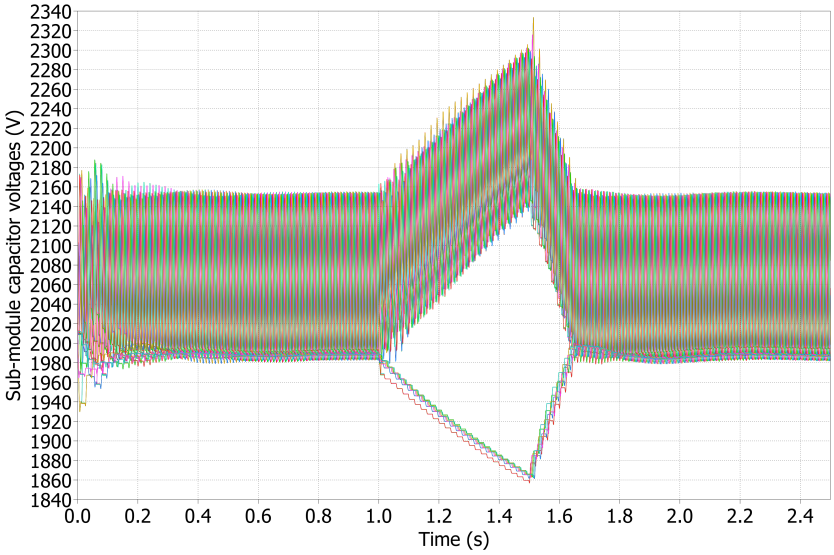


Figure 6.24: *Floating capacitor voltages of the FBSMs and HBSMs during the transient response of the outer local balance control using CLC-I.*

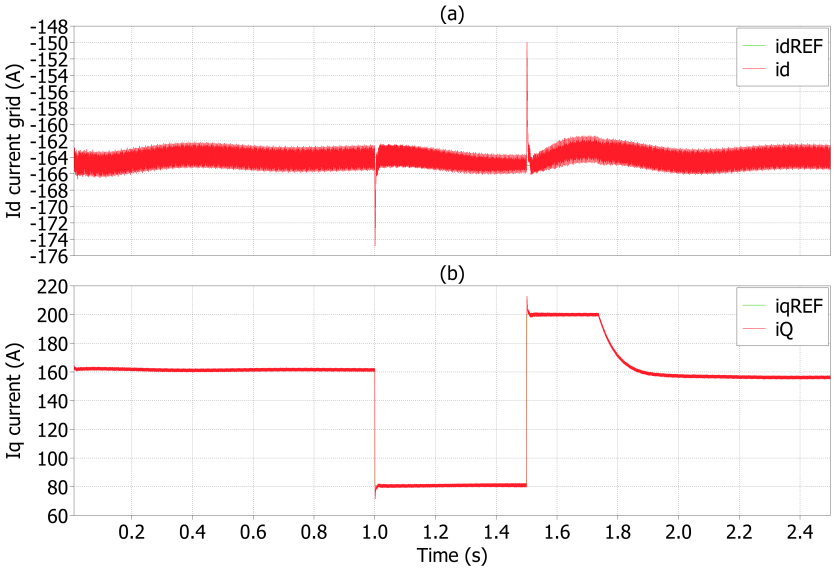


Figure 6.25: *Grid currents $\boldsymbol{i}_{dq}$ during the transient response of the outer local balance control using CLC-I.*

the output of the outer local voltage balance controller i_{qU}, and the feed-forward current reference i_{qff} are shown in fig. 6.27. In steady-state, the capacitor voltage error between the FBSMs and HBSMs is e_{FH}=56.9 V. When the feed-forward current is reduced, the voltage error between the FBSMs and HBSMs reaches e_{FH}=312.0 V. Finally, once the closed-loop voltage controller is activated, the voltage error is reduced to e_{FH}=58.2 V.

The same test is repeated using the second controller proposed CLC-II, where a circulating current component is injected to ensure the local balance. The

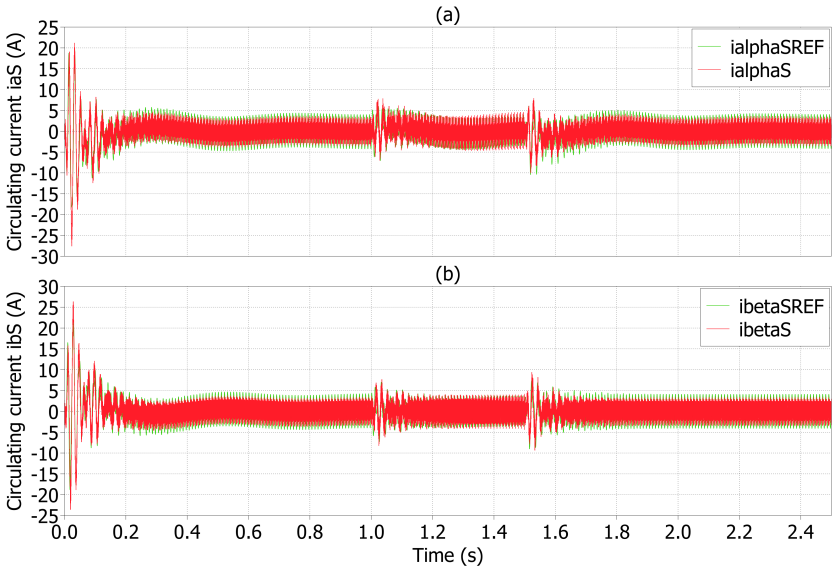


Figure 6.26: *Circulating currents $\boldsymbol{i}_{\alpha\beta}^{\Sigma}$ during the transient response of the outer local balance control using CLC-I.*

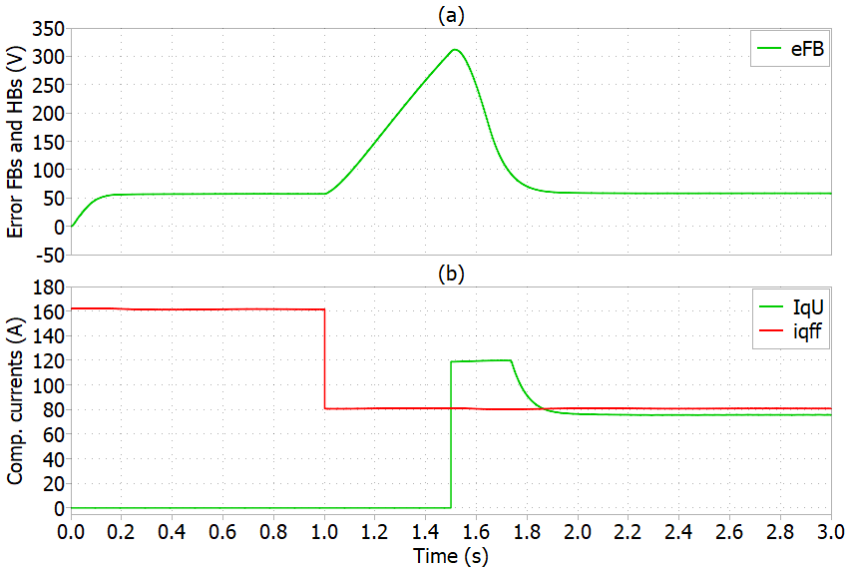


Figure 6.27: *Capacitor voltage error between the FBSMs and HBSMs e_{FH}, output of the outer local voltage balance controller i_{qU}, and the feed-forward current reference i_{qff} during the transient response of the outer local balance control using CLC-I.*

cell capacitor voltages are shown in figure 6.28. Initially, the capacitor voltage oscillations are 190 V. The feed-forward current $i_q^{\Sigma+}$ is reduced to half of its theoretical value at t=1 s, as a consequence the voltage error between the FBSMs and HBSMs increases. Then, the closed-loop voltage control is activated at t=1.5 s, and as a consequence, the capacitor unbalance is reduced in Δt=240 ms.

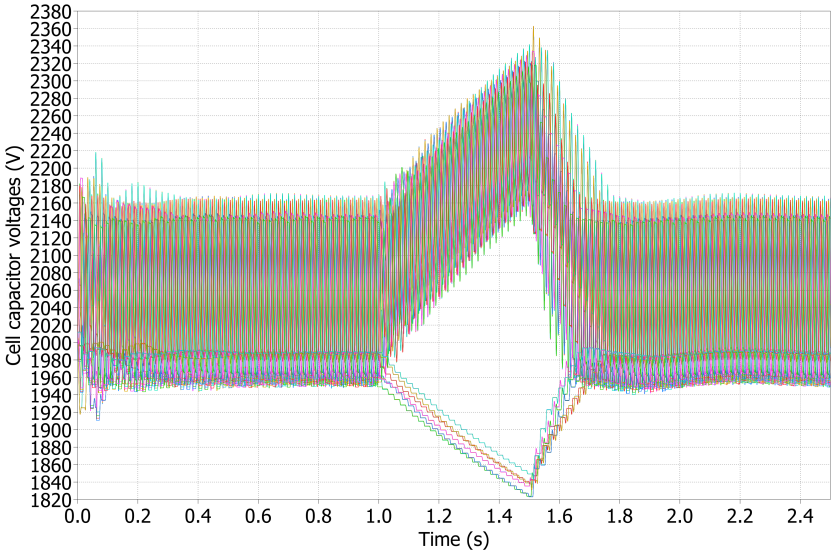


Figure 6.28: *Floating capacitor voltages of the FBSMs and HBSMs during the transient response of the outer local balance control using CLC-II.*

The grid currents are plotted in figure 6.29. In this case, the reactive current reference is zero during the whole operation and the direct current is $i_d = -164$ A. The main advantage of CLC-II is that it can operate at unity power factor.

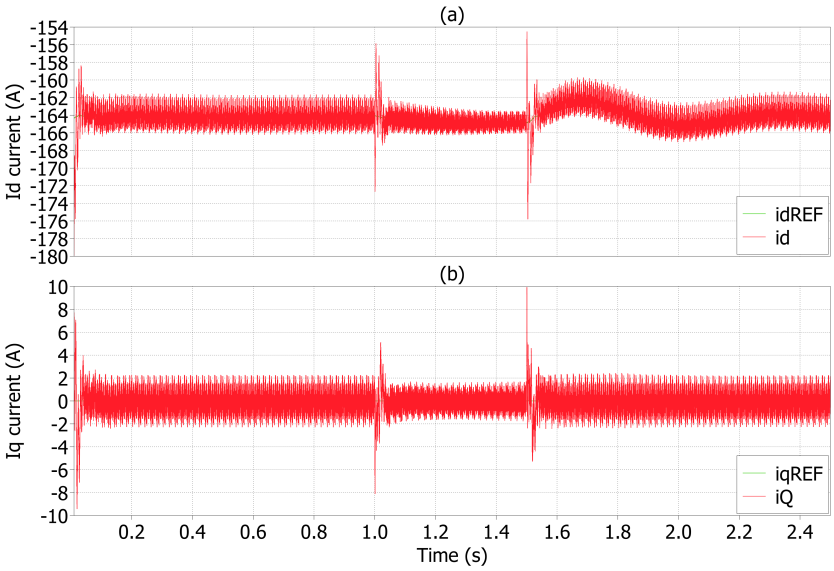


Figure 6.29: *Grid currents $\boldsymbol{i}_{dq}$ during the transient response of the outer local balance control using CLC-II.*

The circulating currents during the whole test are shown in Fig. 6.30. Initially, the magnitude of the circulating current component $i_q^{\Sigma+}$ is 89.2 A. At t=1, the feed-forward current is reduced by 50%, and the magnitude of $i_q^{\Sigma+}$ is reduced to

44.8 A. Finally, once the closed-loop voltage control is activated and the system reaches steady-state, the circulating current magnitude is 86.5 A. A zoomed view of the circulating current when the local balance control is enabled is shown in fig. 6.31.

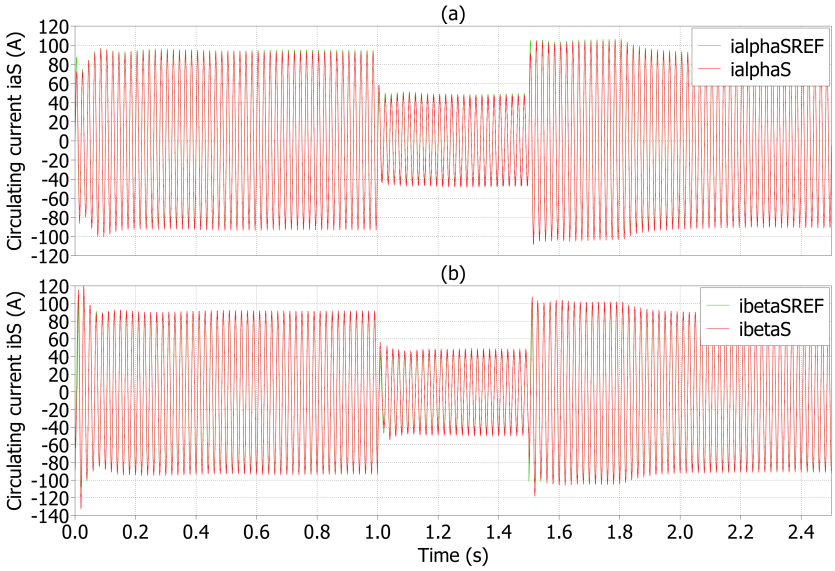


Figure 6.30: *Circulating currents* $\boldsymbol{i}^{\Sigma}_{\alpha\beta}$ *during the transient response of the outer local balance control using CLC-II.*

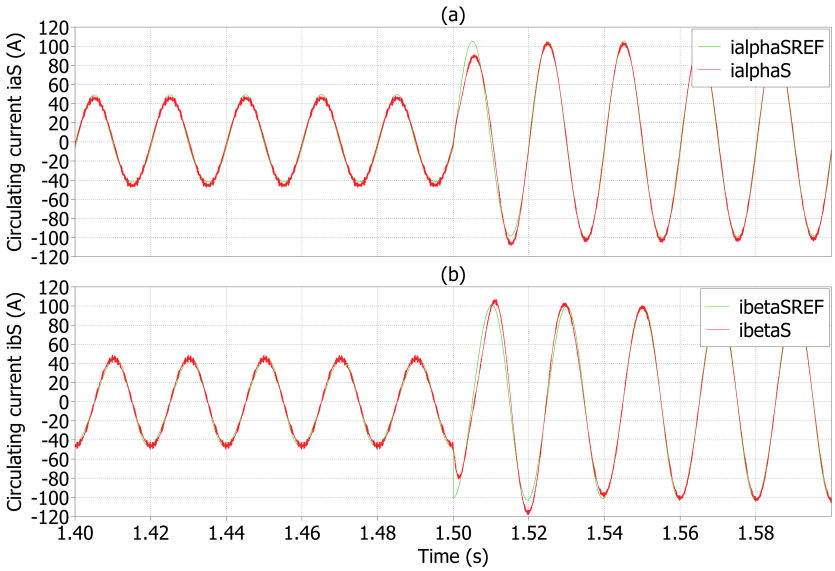


Figure 6.31: *Zoom of the circulating currents* $\boldsymbol{i}^{\Sigma}_{\alpha\beta}$ *between* t=1.4 *s and* t=1.6 *during the transient response of the outer local balance control using CLC-II.*

Finally, the average value of the capacitor voltage error between the FBSMs and HBSMs e_{FH}, the output of the outer local balance control and feed-forward circulating current are shown in figure 6.32. Before the feed-forward value of

the circulating current component $i_q^{\Sigma+}$ is decreased, the capacitor voltage error between the FBSMs and the HBSMs is 90.4 V. After the feed-forward current $i_q^{\Sigma+}$ is reduced, the capacitor voltage error increases up to 380 V. Finally, once the closed-loop local voltage control is enabled the voltage error is reduced to 90.9 V that is similar to its original value. The mean value of the floating capacitor per arm is closed to v_c^*, however, due to the different charging/discharging behaviour of the FBSMs and HBSMs while the hybrid MMC operates in over-modulation, there is a voltage error between the capacitor voltages of the HBSMs and FBSMs.

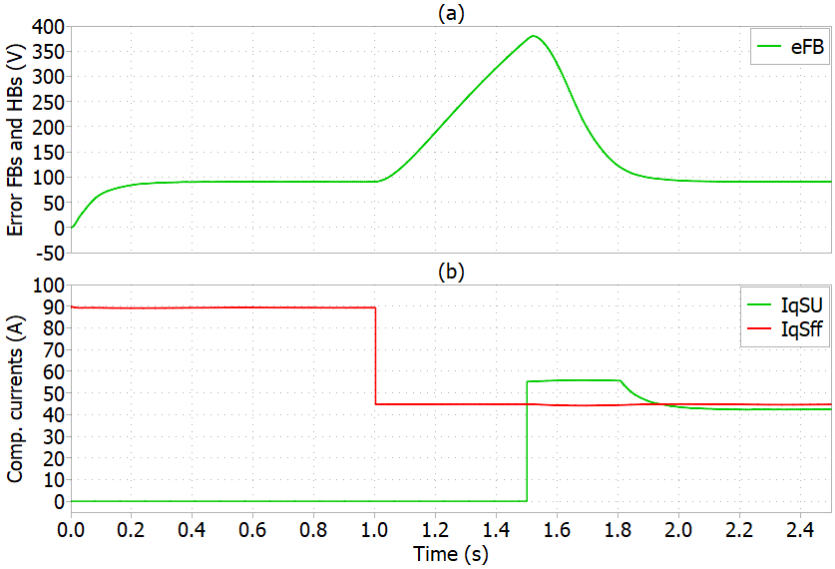


Figure 6.32: *Cell capacitor voltages if the feed-forward term is reduced by* 50% *of its theoretical value when CLC-II is used.*

6.4 Load step performance

In this case, the converter is operating in over-modulation m>2. Initially, the load power is 2 MW and the load power is increased by ΔP_{load}=0.5 MW at t=1 s, during the whole of the remaining operation the converter is working with m=2.5. The local balance control is able to ensure balance between the FBSMs and HBSMs during the transient response. The dc-link port voltage is shown in figure 6.33, the voltage ripple of the dc-port voltage is 0.25% of the nominal dc-link voltage. Once the additional load is connected, the dc-port

voltage decreases to 4355 V, this reduction is equivalent to 3.4% of the nominal dc-port voltage. In this test, the dc-link voltage error is less than 0.1% of the reference value after Δt=17 ms.

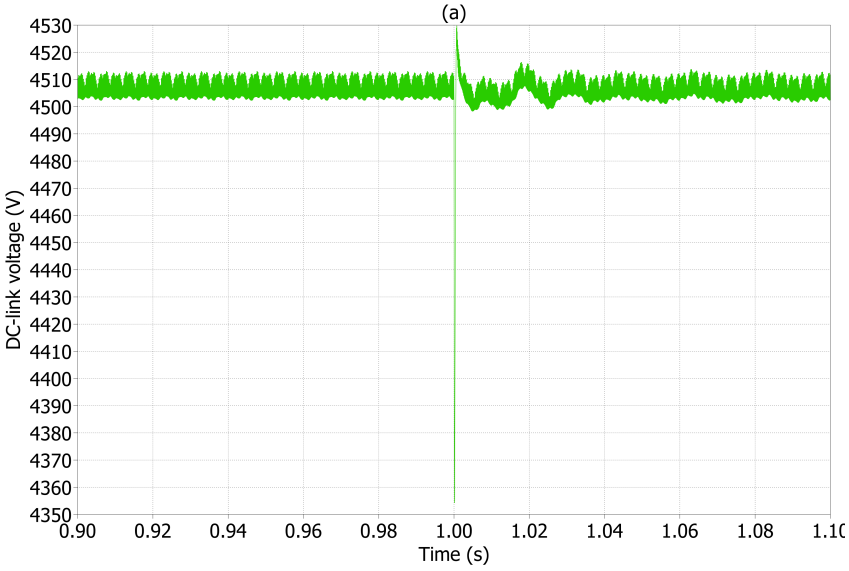


Figure 6.33: *DC-link voltage E during a load impact* ΔP_{load}=0.5 *MW using CLC-I.*

The capacitor voltages are shown are shown in figure 6.34. Before the load impact the capacitor voltage oscillations are 226 V and after they increase to 267 V. During the whole test, the cell capacitor voltages remain balanced.

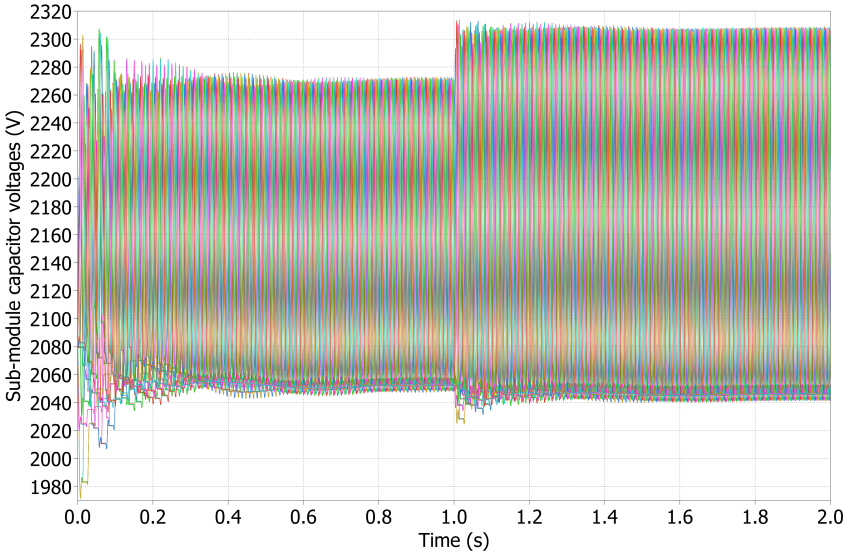


Figure 6.34: *Cell capacitor voltages during a load impact* ΔP_{load}=0.5 *MW using CLC-I.*

The grid currents $\boldsymbol{i}_{dq}$ and the circulating currents $i^{\Sigma}_{\alpha\beta}$ are shown in figures 6.35

and 6.36 respectively. After, the load impact, the magnitude of the direct and quadrature currents are $|i_d|$=295.8 A and $|i_q|$=291.1, i.e. the power factor is 0.71. Finally, the circulating currents are small and the effect of the load impact is negligible. In steady-state operation, after the load impact, the rms value of the circulating current is 1.2 A.

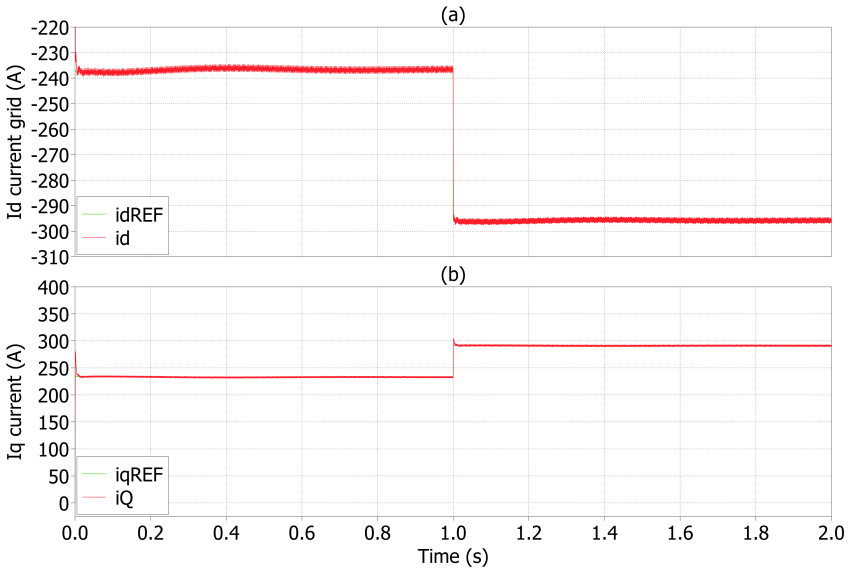


Figure 6.35: *Grid currents i_{dq} during a load impact ΔP_{load}=0.5 MW using CLC-I.*

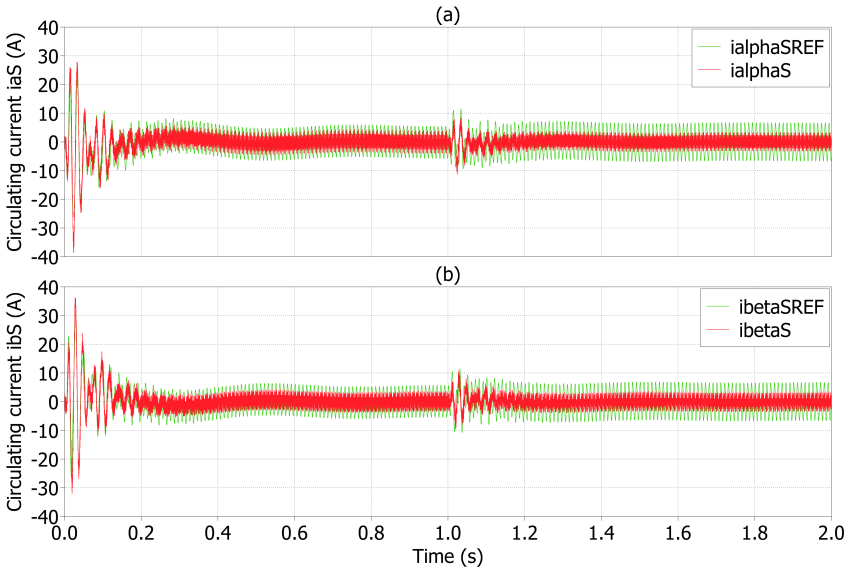


Figure 6.36: *Circulating currents $\boldsymbol{i}^{\Sigma}_{\alpha\beta}$ during a load impact ΔP_{load}=0.5 MW using CLC-I.*

The same impact load test is repeated but using CLC-II to ensure the local balance. The dc-link voltage is shown in figure 6.37. In this case, the transient response has an undershoot equal to 147.0 V, which is equivalent to

3.3%. However, in this case, the dc-link voltage error is lower than 0.1% of its reference value after 36 ms.

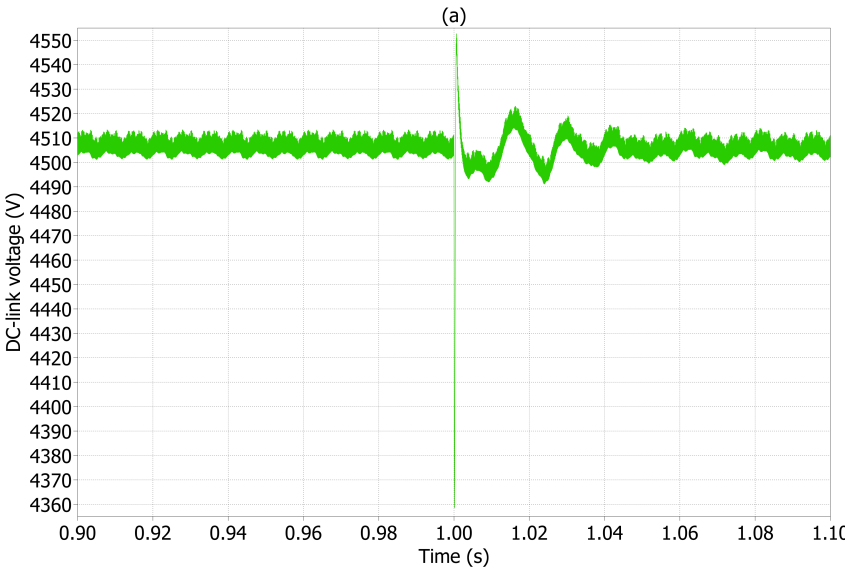


Figure 6.37: *DC-link voltage E during a load impact* ΔP_{load}=0.5 *MW using CLC-II.*

The capacitor voltages are shown in figure 6.38. Before the load step, the capacitor voltage oscillations are 309 V, and after the ΔP_{load} increment, the voltage oscillations increase to 380 V.

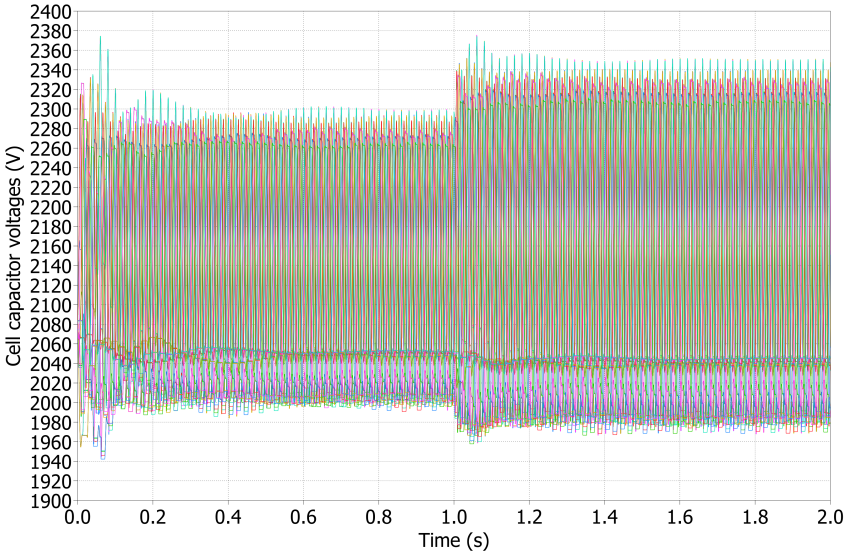


Figure 6.38: *Cell capacitor voltages during a load impact* ΔP_{load}=0.5 *MW using CLC-II.*

The grid currents $\boldsymbol{i}_{dq}$ and the circulating currents $\boldsymbol{i}^{\Sigma}_{\alpha\beta}$ are plotted in figures 6.39 and 6.40 respectively. During the whole test, the average value of the

reactive current is zero. Before the load impact, the circulating current peak value is 132.0 A and after the load power increment, the peak value is 162 A. The frequency of the circulating currents $\boldsymbol{i}_{\alpha\beta}^{\Sigma}$ is 50 Hz, therefore its frequency matches its theoretical value imposed when the negative sequence component $i_q^{\Sigma+}$ is injected.

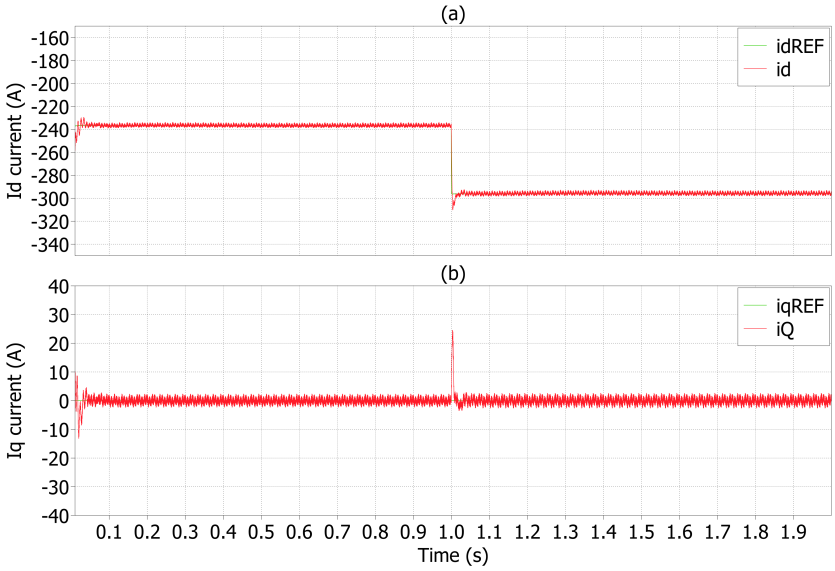


Figure 6.39: *Grid currents i_{dq} during a load impact ΔP_{load}=0.5 MW using CLC-II.*

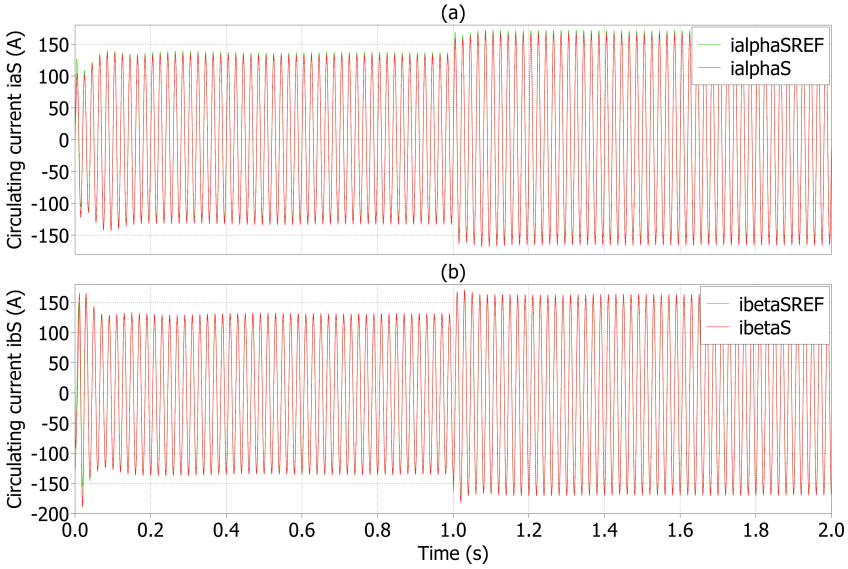


Figure 6.40: *Circulating currents $\boldsymbol{i}_{\alpha\beta}^{\Sigma}$ during a load impact ΔP_{load}=0.5 MW using CLC-II.*

6.5 Common-mode voltage reduction for a drive application

In this test, a back-to-back MMC is considered to drive an induction machine. The hybrid MMC is used to produce a controllable dc-link voltage. This is used to reduce the magnitude of the common-mode voltage needed to balance the floating capacitors of the machine-side converter when operating at low mechanical speeds. In addition, by imposing a controlled dc-link voltage equal to (5.49), the duration of the LFM is reduced in the same proportion as the ratio between the minimum dc-link voltage E_{min} and its rated value E_{rated}.

The converter operation with constant dc-link voltage is shown first. In this test the MMC drive is used to feed a quadratic-torque profile such as a fan application. Although it is possible to drive a constant load torque, the converter would have to be overrated due to the high arm current. For constant load torque profiles, the modular multilevel matrix converter is preferred if the electrical frequency of the load is lower than that of the grid-side port [26]. At rated speed the delivered power is 1 MW. The converter parameters of the HBSM-based MMC are shown in table 6.3. The simulations are made for a 1 MW induction machine [160] with the parameters shown in Table 6.4.

Table 6.3: Simulation parameters for the HBSM-based modular multilevel converter for the machine-side.

Parameter	Description	Value
P	Rated power	1 MW
E	Rated dc-link voltage	8525 V
N	Number of cells per arm	8
v_C^*	Sub-module voltage reference	1.23 kV
f_c	Carrier frequency	2.5kHz
L	Arm inductance	2.5 mH
C	Sub-module capacitance	3.5 mF

The machine speed along with its reference are shown in fig. 6.41. The machine starts from standstill and it accelerates up to rated speed N_r=1189 RPM.

The capacitor voltages of each sub-module are shown in fig. 6.42, the voltage

Table 6.4: Simulation parameters for the HBSM-based modular multilevel converter for the machine-side.

Parameter	Description	Value
R_s	Stator resistance	0.21 Ω
R_r	Rotor resistance	0.146 Ω
L_{ls}	Stator leakage inductance	5.2 mH
L_{lr}	Rotor leakage inductance	5.2 mH
L_m	Magnetizing Inductance	155 mH
J	Moment of inertia	10 kg-m^2
p	Pair of poles	3
N_r	Rated Speed	1189 RPM
f_s	Nominal stator frequency	60 Hz

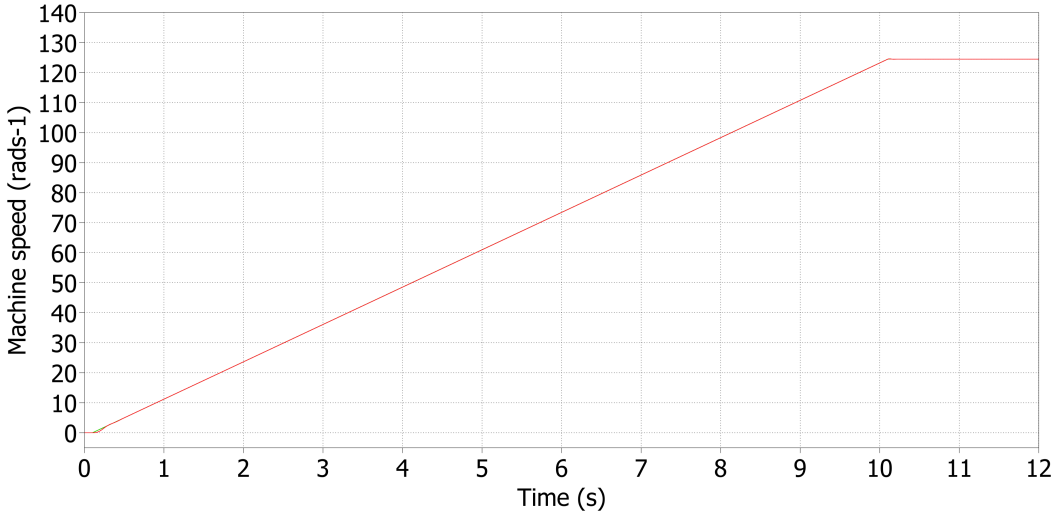


Figure 6.41: *Mechanical speed along with its reference.*

peak-to-peak ripple is 102 V and, as explained in section 5.5, the transition between low-frequency mode (LFM) and the high-frequency mode (HFM) happens when the power term $\boldsymbol{p}_m$ is greater or equal to the oscillatory component $\boldsymbol{p}_{\text{osc}}$. These power terms are defined in equation 5.40. In this case this transition occurs at t=4.18 s.

The capacitor voltages of the sub-modules of the upper arm of phase a during LFM and HFM are shown in figures 6.43a and 6.43b respectively. As the machine speed increases the capacitor voltage oscillations decrease. In steady-state operation, once the machine operates at rated speed, the capacitor voltage oscillations are 65 V.

The total capacitor voltage of each arm is shown in fig. 6.44 in the $\Sigma\Delta\alpha\beta 0$

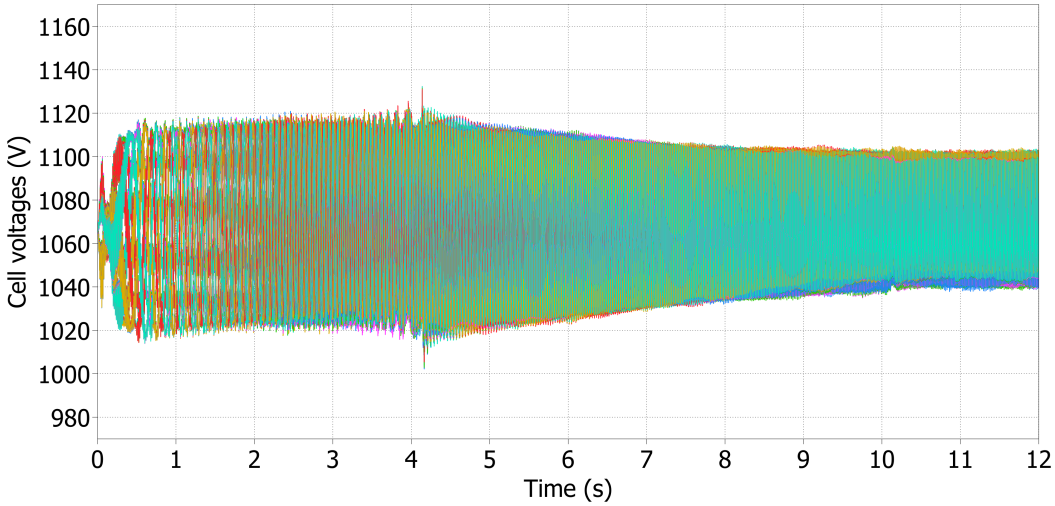
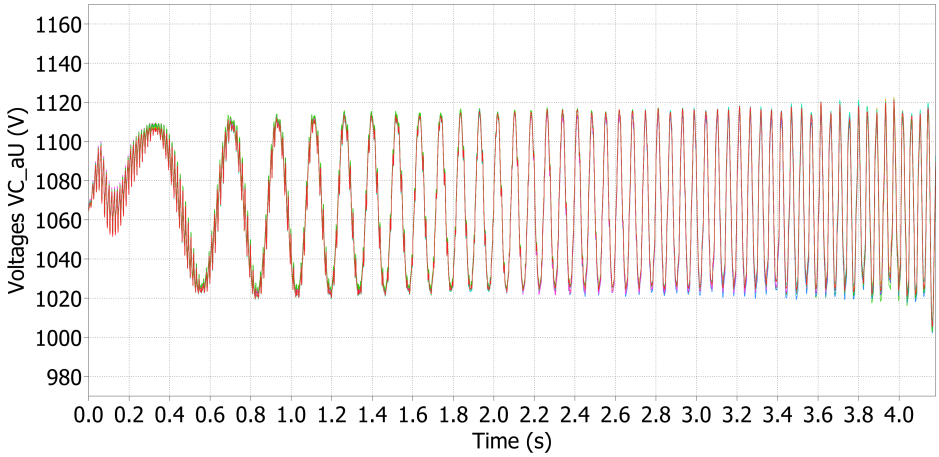
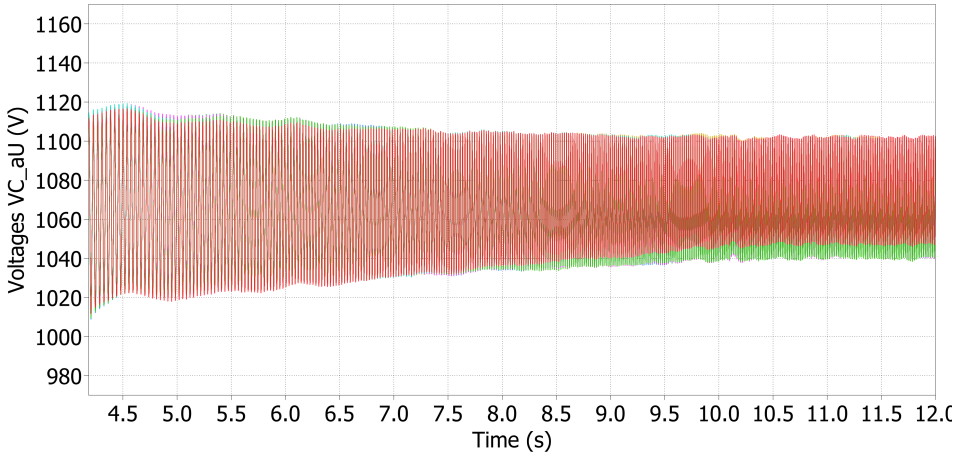


Figure 6.42: *Capacitor voltage of the HBSMs of the MMC-based drive converter with constant dc-link voltage.*



(a) *Capacitor voltage of the upper arm of phase a during LFM.*



(b) *Capacitor voltage of the upper arm of phase a during HFM.*

Figure 6.43: *Capacitor voltage of the HBSMs of the upper arm of phase a during LFM (a) and HFM (b).*

reference frame. The voltage term v_{C0}^{Σ} is depicted in Fig. 6.44(a), this term is equal to the average of the total capacitor voltage of the 6 arms, in steady-state v_{C0}^{Σ}=Nv_C^*. The voltages terms $\boldsymbol{v}_{C\alpha\beta}^{\Sigma}$, v_{C0}^{Δ}, and $\boldsymbol{v}_{C\alpha\beta}^{\Delta}$ are shown in Fig. 6.44(b)-(d) respectively, these 5 terms regulate the energy balance among the converter arms. The voltage ripples are mainly due to the voltage term $\boldsymbol{v}_{C\alpha\beta}^{\Delta}$, in this case the maximum value is 750 V, while the maximum values of v_{C0}^{Δ} and $\boldsymbol{v}_{C\alpha\beta}^{\Sigma}$ are 76 V and 120 V respectively.

The machine current during the whole speed ramp is shown in fig. 6.45a. A zoomed view of $\boldsymbol{i}_{abc}$ is shown in figure 6.45b, even though in the LFM the converter is injecting circulating currents, the machine currents have low distortion. The machine currents when the system reaches steady-state operation are shown in figure 6.45c, the peak value of the machine current is 202 A, in this case the load power is 1 MW.

During low-frequency operation, the capacitor voltage balance is accomplished by injecting a high-frequency circulating current along with a common-mode voltage. The circulating currents along with their references are shown in fig. 6.46(a)-(b). As expected these currents are higher during the machine start-up and then, once the mechanical speed increases, the magnitude of the circulating current is reduced considerably. During LFM the peak value of the circulating currents is 91 A. Conversely, during HFM, once the machine reaches the rated speed, the peak value of the circulating currents is 1.4 A, notice that at this operational point the converter is delivering 1 MW of active power. The common-mode voltage is shown in 6.46(c), the maximum common-mode voltage is produced for ω_m=0 rad/s and is equal to half the dc-link voltage, its magnitude decrease when the machine speed increases. During low-frequency mode a square-wave common-mode voltage is injected with frequency f_e=75 Hz. Once the machine operates in high-frequency mode, a sinusoidal common-mode voltage is injected to increase the modulation index and to balance the voltage terms $\boldsymbol{v}_{C\alpha\beta}^{\Delta}$. During LFM, the peak value of the common-mode voltage is 3595 V. Conversely, in HFM, the peak value of the common-mode voltage

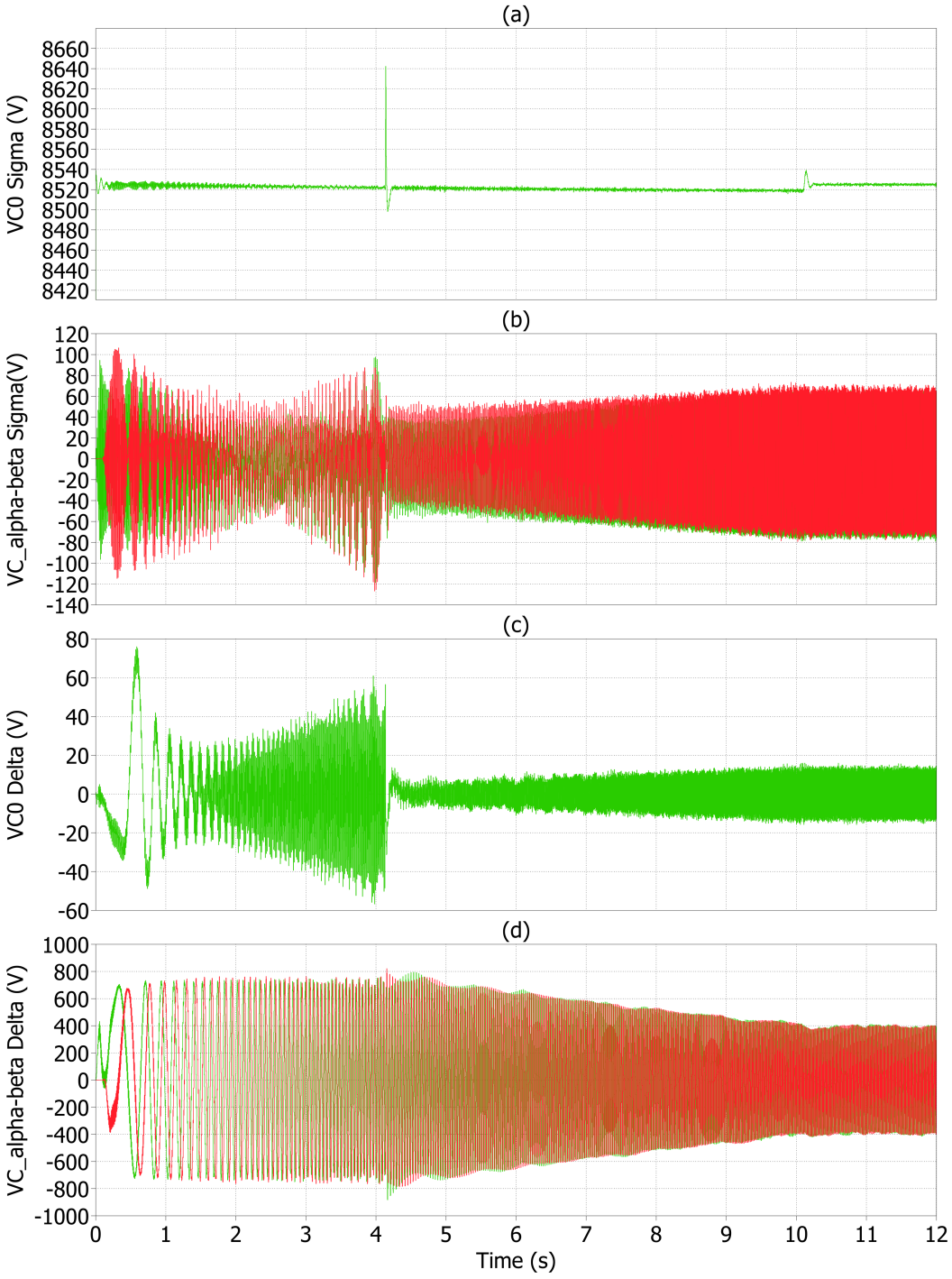
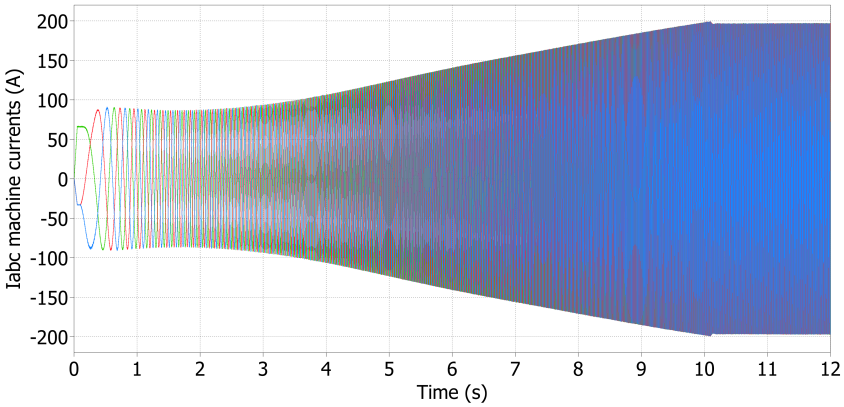


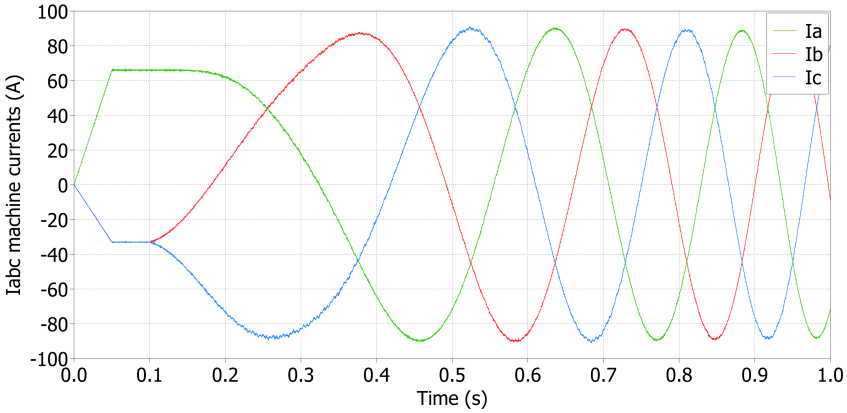
Figure 6.44: *Total capacitor voltage of the HBSMs in $\Sigma\Delta\alpha\beta 0$ coordinates: (a) total capacitor voltage v_{C0}^{Σ}, (b) unbalance voltage term $\boldsymbol{v}_{C\alpha\beta}^{\Sigma}$, (c) unbalance voltage term v_{C0}^{Δ}, and (d) unbalance voltage term $\boldsymbol{v}_{C\alpha\beta}^{\Delta}$.*

is 740 V.

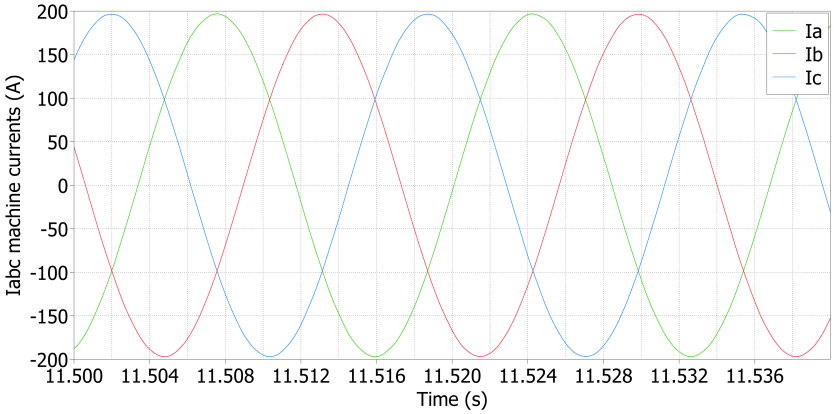
In the next test, the same speed profile and load are considered but a controlled dc-link voltage is imposed. In the previous analysis in section 5.5, it has been shown that the magnitude of the common-mode voltage and the duration of



(a) *Currents of the induction machine during the whole speed ramp.*



(b) *Currents of the induction machine during LFM.*



(c) *Currents of the induction machine in steady-state at* ω_m=124 *rad/s.*

Figure 6.45: *Currents of the induction machine: (a) during the speed ramp, (b) during LFM, and (c) during steady-state at rated speed.*

the LFM are proportional to the dc-port voltage. In the following test, the dc-link voltage is varied according to (5.47). From the previous analysis, the optimal dc-link voltage to reduce the energy oscillations in each arm were derived. In this case, the common-mode voltage is reduced down to 40% of its nominal value, i.e. initially the dc-port voltage is E_{min}=3410 V. The minimum

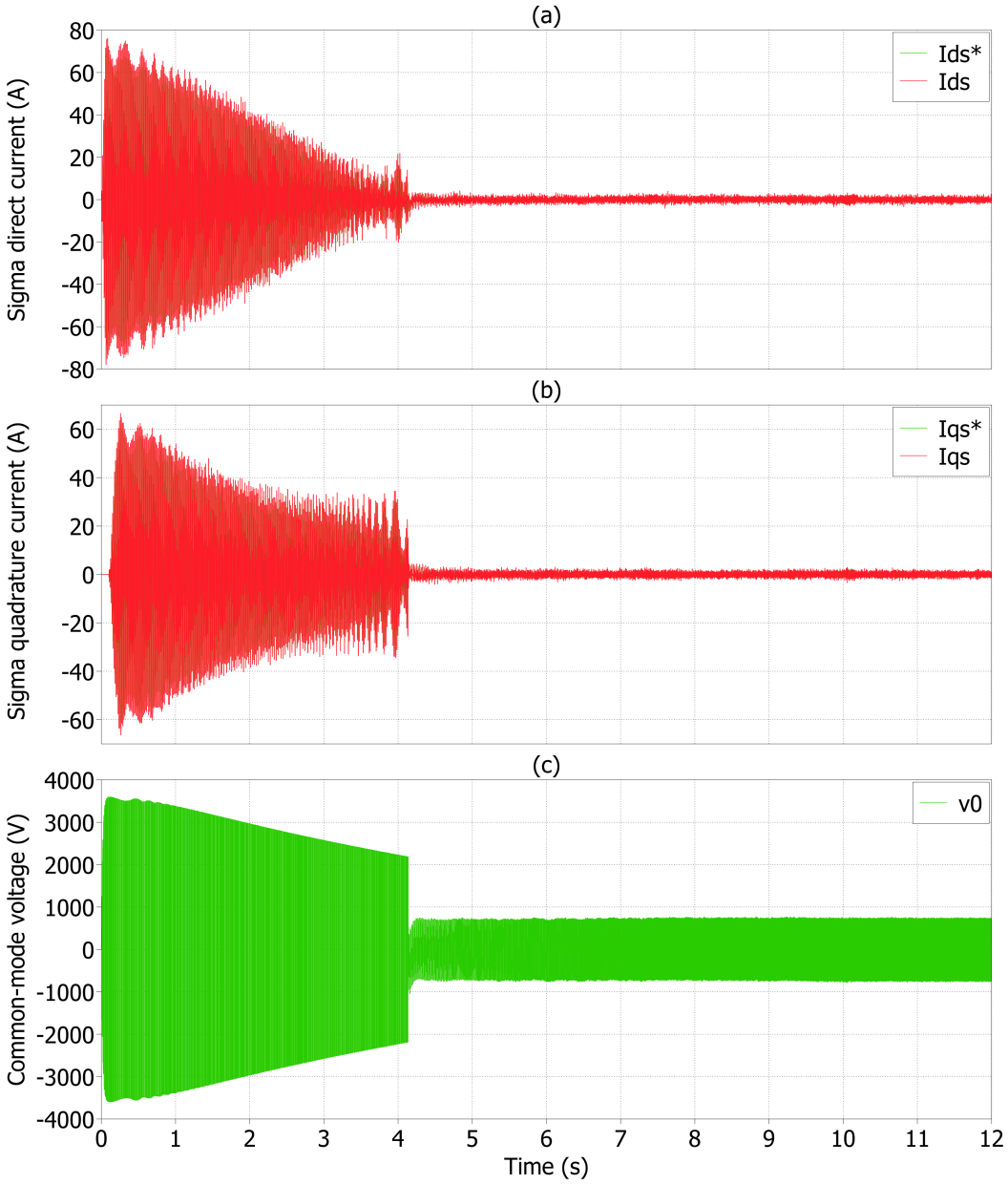


Figure 6.46: *(a) direct circulating current i_d^{Σ}, (b) quadrature circulating current i_q^{Σ}, and (c) common-mode voltage v_0.*

value of the dc-link has been chosen to avoid over-currents during LFM in the arm currents of the drive-side MMC and to have enough voltage margin to modulate the machine voltage. The cell capacitor voltages are shown in fig. 6.47.

The capacitor voltages of the upper arm of phase a are shown in figures 6.48a and 6.48b respectively. During LFM, the maximum capacitor voltage oscillation is 94 V and once the system reaches steady-state operation it is 65 V.

The circulating currents along with the common mode voltage are shown in

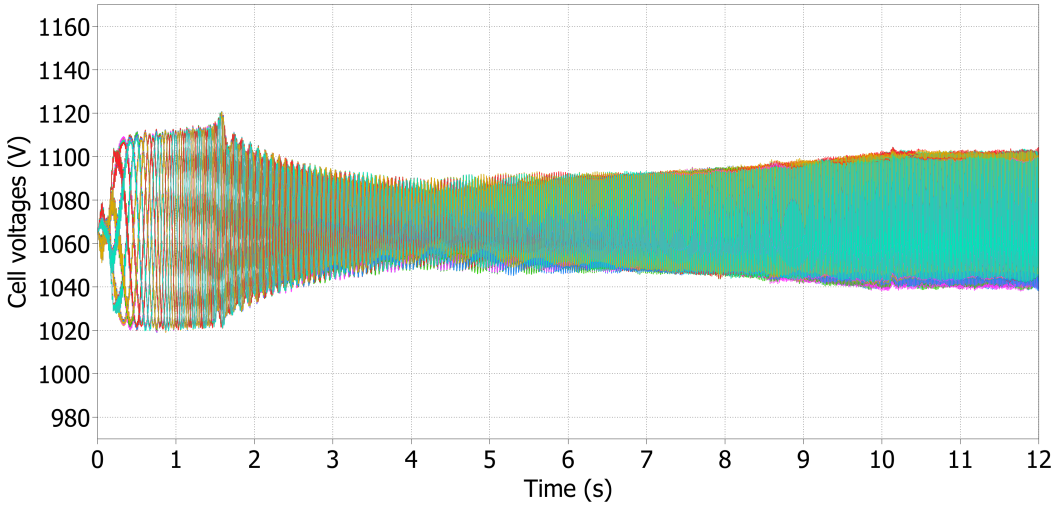
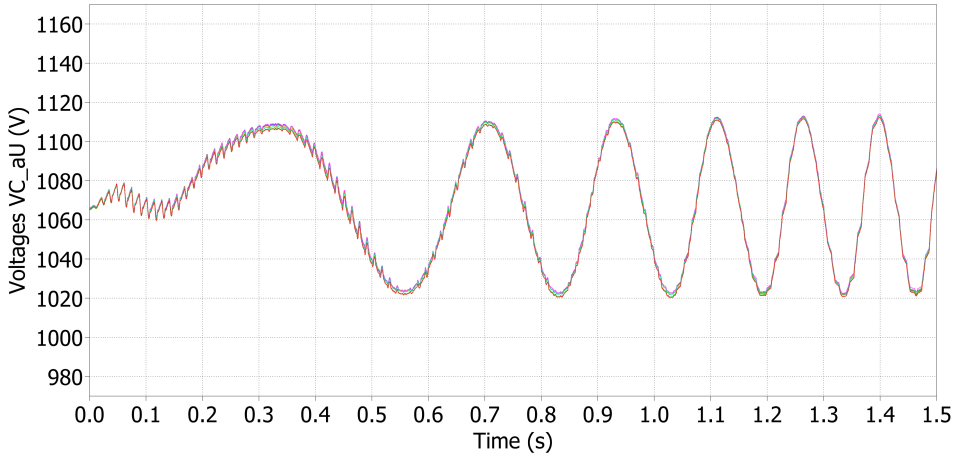
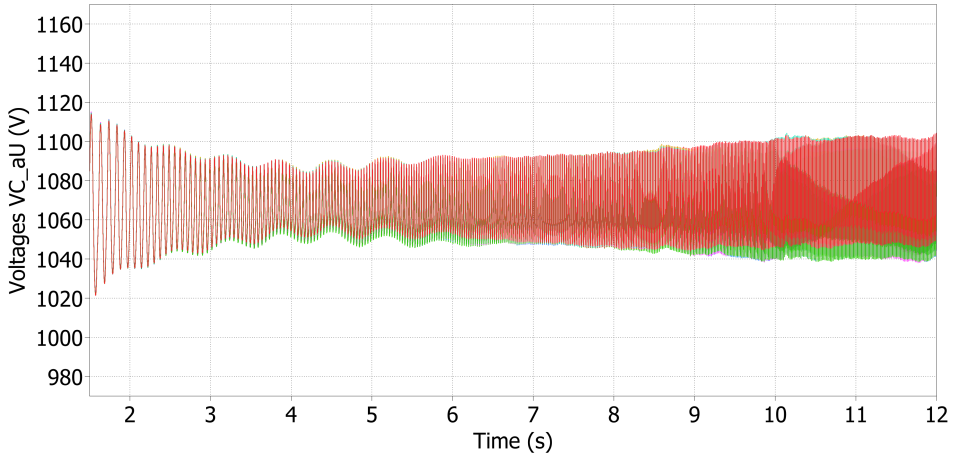


Figure 6.47: *Floating capacitor using a variable dc-port voltage ($E_{\min}$=3410 V).*



(a) *Capacitor voltage of the upper arm of phase a during LFM.*



(b) *Capacitor voltage of the upper arm of phase a during HFM.*

Figure 6.48: *Capacitor voltage of the HBSMs of the upper arm of phase a during LFM (a) and HFM (b).*

figure 6.49. In this case the peak value of the common-mode voltage is 1.5 kV, i.e. 39.6% of the maximum common-mode voltage injected with a fixed dc-link voltage. As expected, the duration of the low-frequency mode is also reduced to 34.8% of the LFM duration when the dc-link voltage is kept constant during the whole operation.

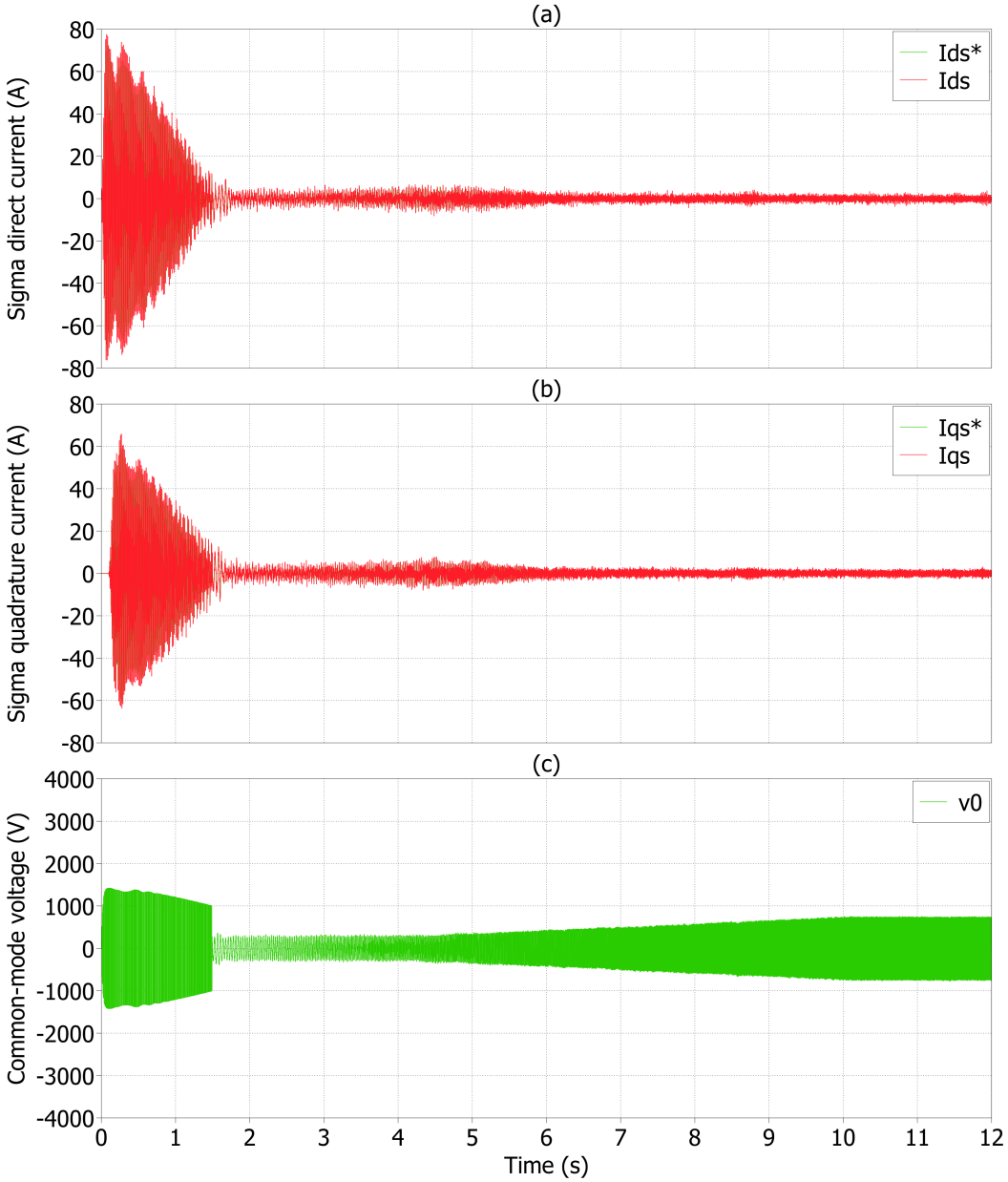
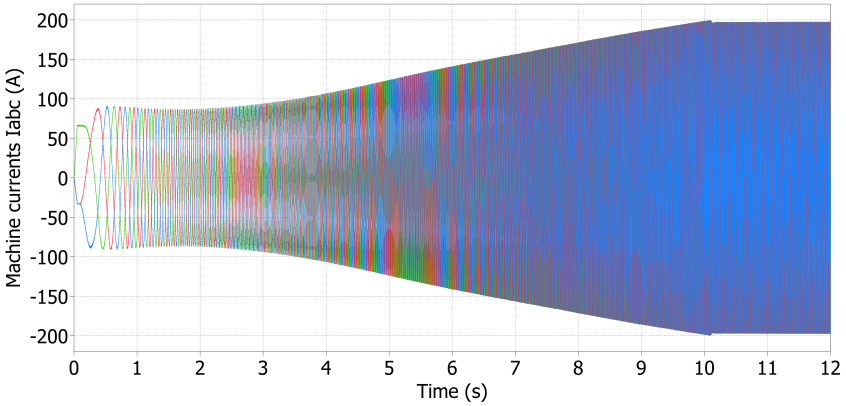


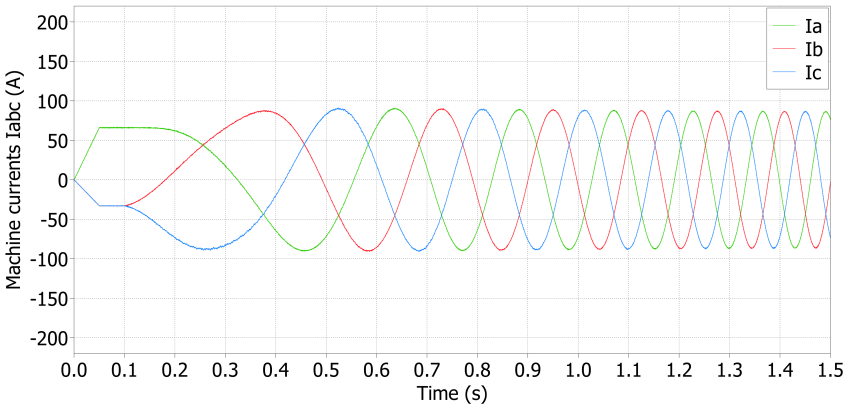
Figure 6.49: *Floating capacitor using a variable dc-port voltage ($E_{\min}$=3410 V).*

The machine current during the whole speed ramp is shown in fig. 6.50a when a variable dc-link voltage is used. A zoomed view of $\boldsymbol{i}_{abc}$, during LFM, is shown in figure 6.50b, even though in the LFM the converter is injecting circulating

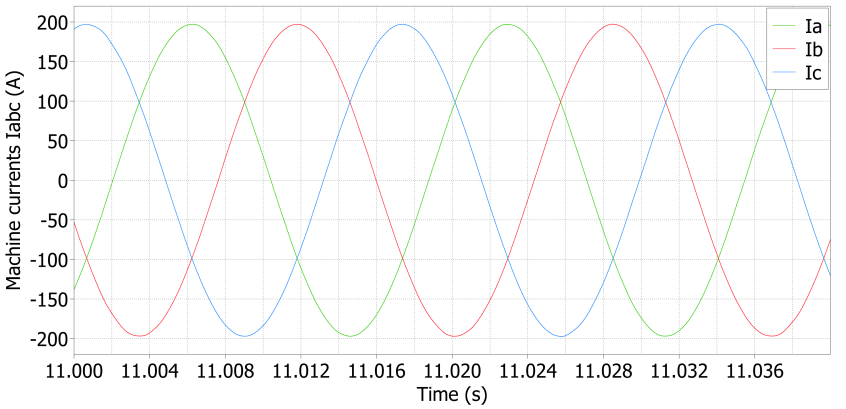
currents, the machine currents have low distortion. The machine currents when the system reaches steady-state operation are shown in figure 6.50c where the peak value of the machine current is 202 A and the load power is 1 MW. As expected the machine currents are not affected by the controlled dc-link voltage.



(a) *Currents of the induction machine during the whole speed ramp.*



(b) *Currents of the induction machine during LFM.*



(c) *Currents of the induction machine in steady-state at* ω_m=124 *rad/s.*

Figure 6.50: *Currents of the induction machine: (a) during the speed ramp, (b) during LFM, and (c) during steady-state at rated speed.*

Next, the performance of CLC-I and CLC-II is shown when producing a variable dc-link voltage for the drive-side MMC. In this case, the hybrid MMC is designed to provide a rated dc-link voltage equal to 8525 V. In addition, the hybridisation ratio is chosen to be able to modulate the minimum dc-link voltage defined in the previous test (40% of its rated value). The parameters of the hybrid MMC are shown in table 6.5.

Table 6.5: Simulation parameters for the hybrid modular multilevel converter for the drive application.

Parameter	Description	Value
P	Rated power	1 MW
E	Rated dc-link voltage	8525 V
N_H	Number of HBSMs per arm	3
N_F	Number of FBSMs per arm	2
N	Number of cells per arm	5
V_g	Grid voltage (line-to-line RMS)	5.5 kV
v_C^*	Sub-module voltage reference	2084V
f_c	Carrier frequency	5kHz
L	Arm inductance	5 mH
C	Sub-module capacitance	0.8 mF

First, the operation of the hybrid MMC when CLC-I is used is considered. The cell capacitor voltage is shown in Fig. 6.51. During the whole test, the cell capacitor voltages remain balance and the voltage oscillations are 8.5% of its rated value in steady-state operation.

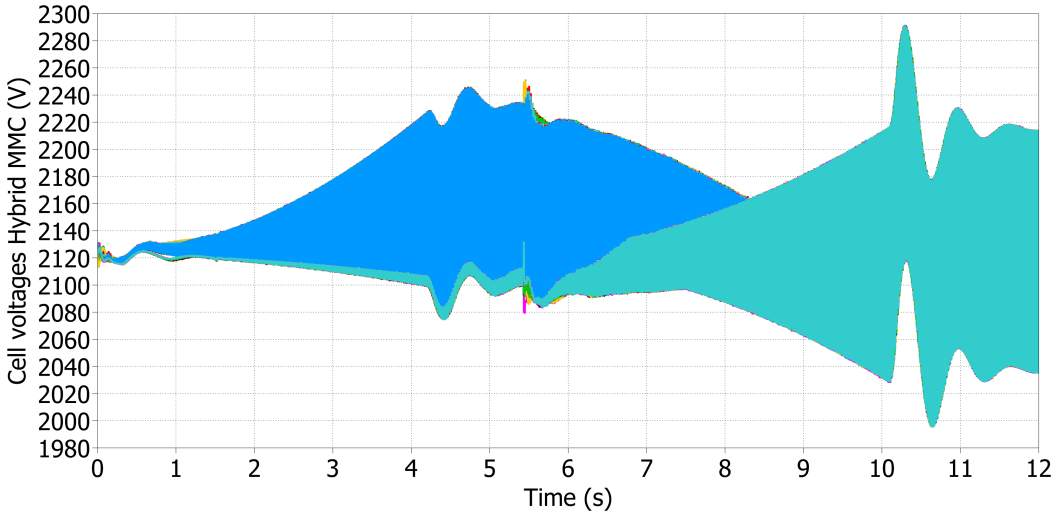


Figure 6.51: *Floating capacitor of the hybrid MMC for a variable dc-port voltage (CLC-I).*

The dc-link voltage is shown in Fig. 6.52. Initially, the dc-link voltage is 40% of its rated value $E_{\min}$=3410 V. Then, once the machine increase its speed, the dc-link voltage is calculated according to (5.49). Once, the machine reaches its rated speed, the dc-link voltage is equal to 8525 V.

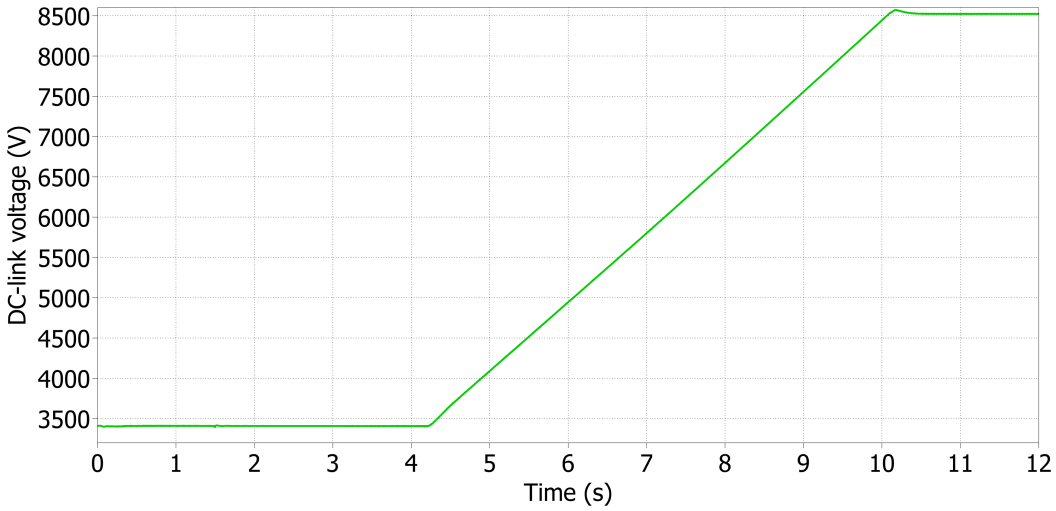


Figure 6.52: *DC-link voltage of the hybrid MMC for a variable dc-port voltage (CLC-I).*

The grid currents and circulating currents of the hybrid MMC are shown in figures 6.53 and 6.54 respectively. The direct current increases along with the load power and in steady-state operation the grid current is 170 A. During low-frequency operation, while the dc-link voltage is reduced, the maximum reactive current is 43 A. The circulating currents for this case are negligible, since CLC-I does not rely on the injection of circulating current to ensure the balance between HBSMs and FBSMs, and accordingly the circulating currents have a peak value lower than 2 A.

Finally, the control of the hybrid MMC with variable dc-link voltage is considered when the local balance is done using CLC-II. The cell capacitor voltages are shown in Fig. 6.55. In this case, the capacitor voltage oscillations are 8.5% at rated speed, this is similar to the previous case because at rated speed the hybrid MMC operates as a HBSM-based MMC, i.e. without an extra circulating current component or extra reactive current.

The grid currents of the hybrid MMC are shown in Fig. 6.56. The main

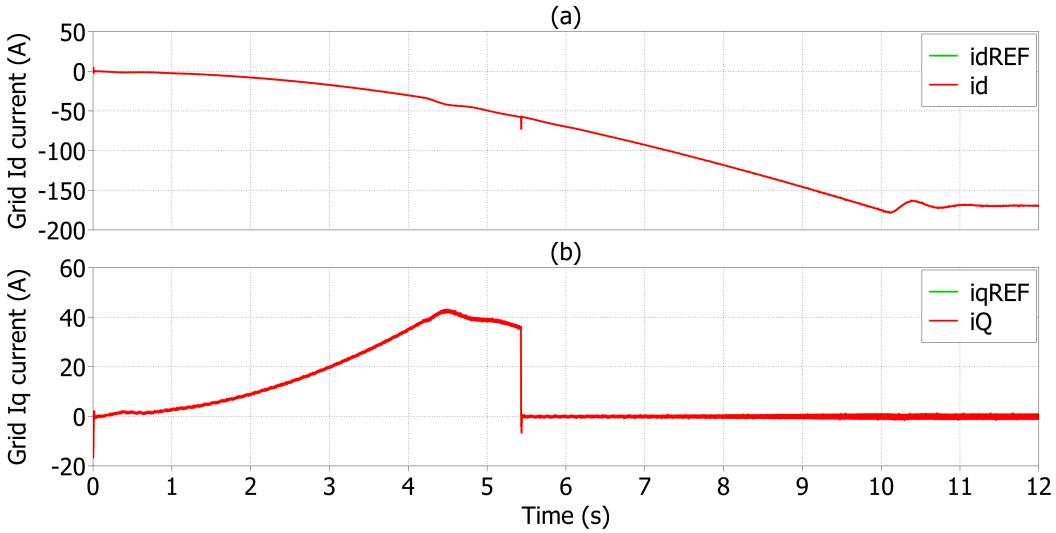


Figure 6.53: *Grid currents of the hybrid MMC for a variable dc-port voltage (CLC-I).*

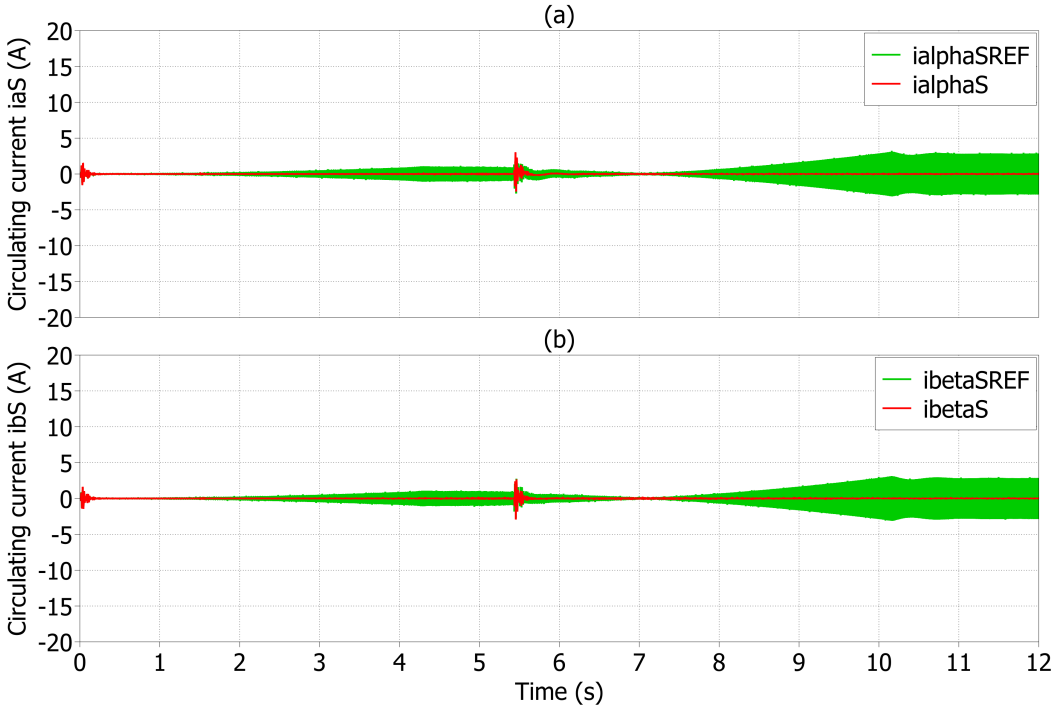


Figure 6.54: *Circulating currents of the hybrid MMC for a variable dc-port voltage (CLC-I).*

advantage of using CLC-II is that the reactive current is zero (unity power factor operation) during the whole operation. The direct current is similar to that for CLC-I.

Finally, the circulating currents when CLC-II is used to balance the FBSMs and HBSMs are shown in Fig. 6.57. The maximum peak value is 21 A while the dc-link voltage is reduced. In steady-state operation the circulating currents

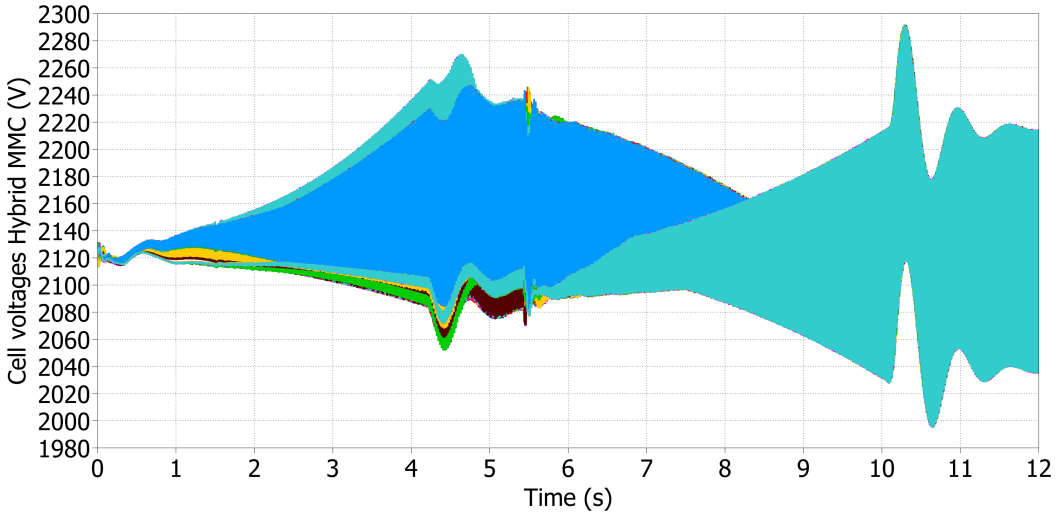


Figure 6.55: *Cell capacitor voltages of the hybrid MMC for a variable dc-port voltage (CLC-II).*

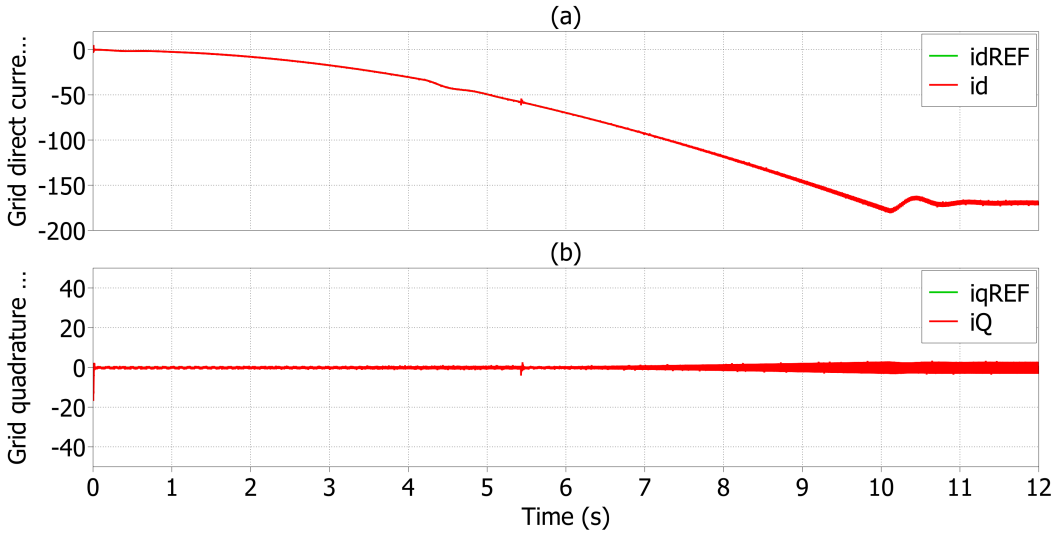


Figure 6.56: *Grid currents of the hybrid MMC for a variable dc-port voltage (CLC-II).*

are negligible.

6.6 Capacitance reduction for the drive side MMC

As explained in the previous section 5.5, by imposing a controllable dc-port voltage according to (5.49), the power oscillation term $\boldsymbol{p}_{\text{osc}}$ is minimised during LFM. As a consequence, another advantage of working with an optimal dc-port

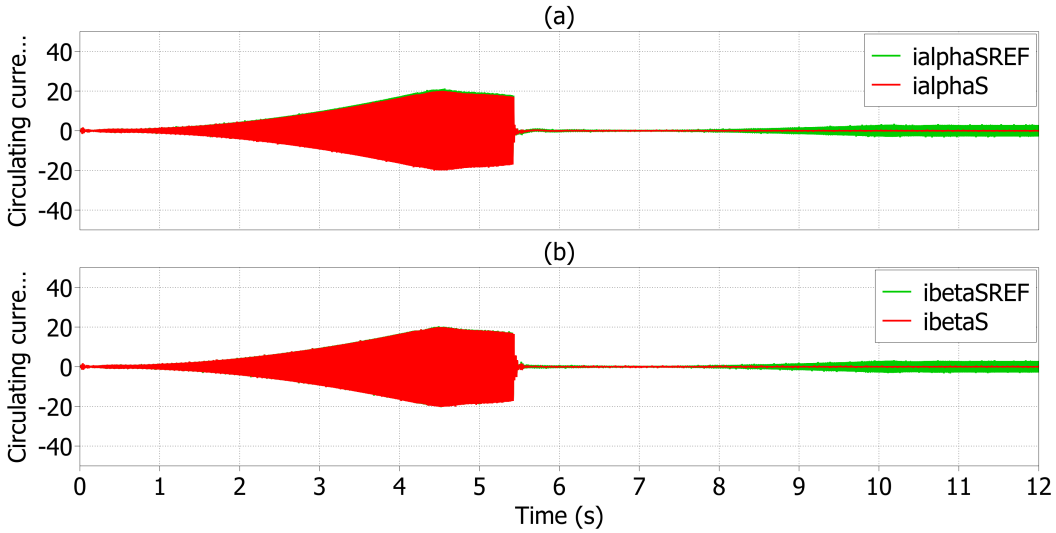
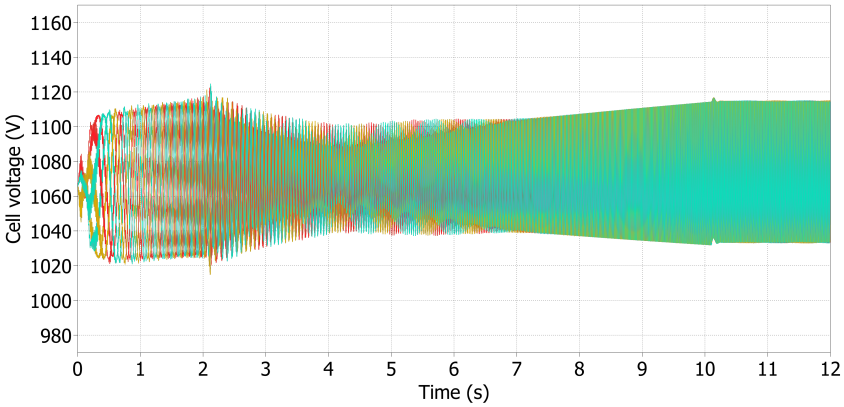
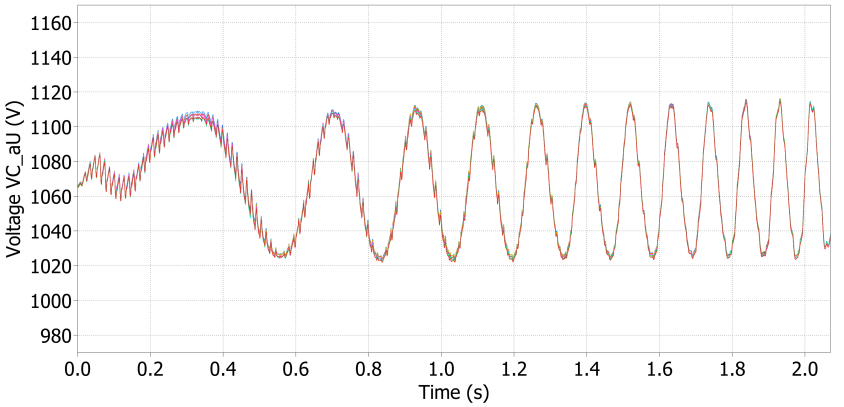


Figure 6.57: *Grid currents of the hybrid MMC for a variable dc-port voltage (CLC-II).*

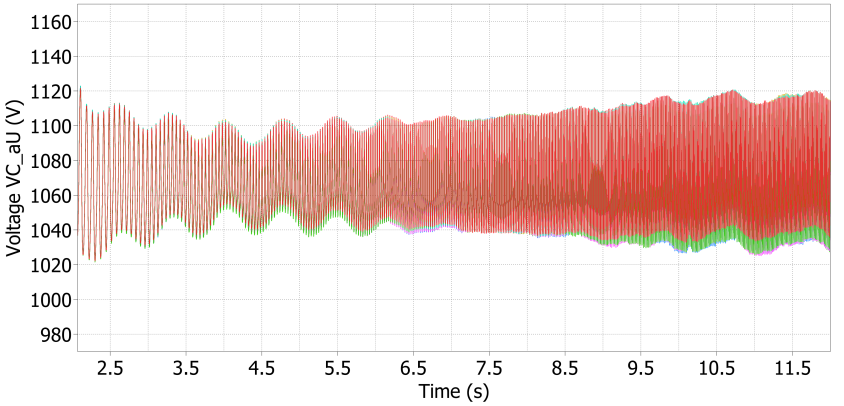
voltage is that during LFM the capacitor voltage oscillations are lower than the case when the rated dc-link voltage is used. Consequently, it is possible to reduce the cell capacitance and to keep the capacitor voltages bounded to the maximum oscillations reached during LFM. As an example, the previous drive converter is considered again. The dc-port voltage is controlled according to (5.49) but in this case the capacitance is reduced by 30% of the original case and the same load and speed references are considered. The cell capacitor voltages are shown in figure 6.58a. In LFM, the maximum value of the capacitor voltage oscillations is 94 V and during HFM, the capacitor voltage oscillations are less than 82 V. As expected, the voltage oscillations are greater when a reduced cell capacitance is used, but they are less than those reached during LFM. The circulating currents are shown in figures 6.59(a)-(b) and the common-mode voltage is shown in 6.59(c). In this case, the peak value of the common-mode voltage is 1.4 kV. In addition, the LFM duration increases by Δt=0.5 s. The peak value of the circulating currents is 91.1 A during LFM.



(a) *Cell capacitor voltages when a variable DC-link is used and the cell capacitance is reduced by* 30%.



(b) *Capacitor voltages* v_{Ca}^{U} *during LFM when a variable DC-link is used and the cell capacitance is reduced by* 30%.



(c) *Capacitor voltages* v_{Ca}^{U} *during HFM when a variable DC-link is used and the cell capacitance is reduced by* 30%.

Figure 6.58: *Capacitor voltages when a variable DC-link is used and the cell capacitance is reduced by* 30%.

6.7 Summary

This chapter presented simulation results to validate the proposed control system of chapter 5. First, the unbalance problem typical of the hybrid MMC

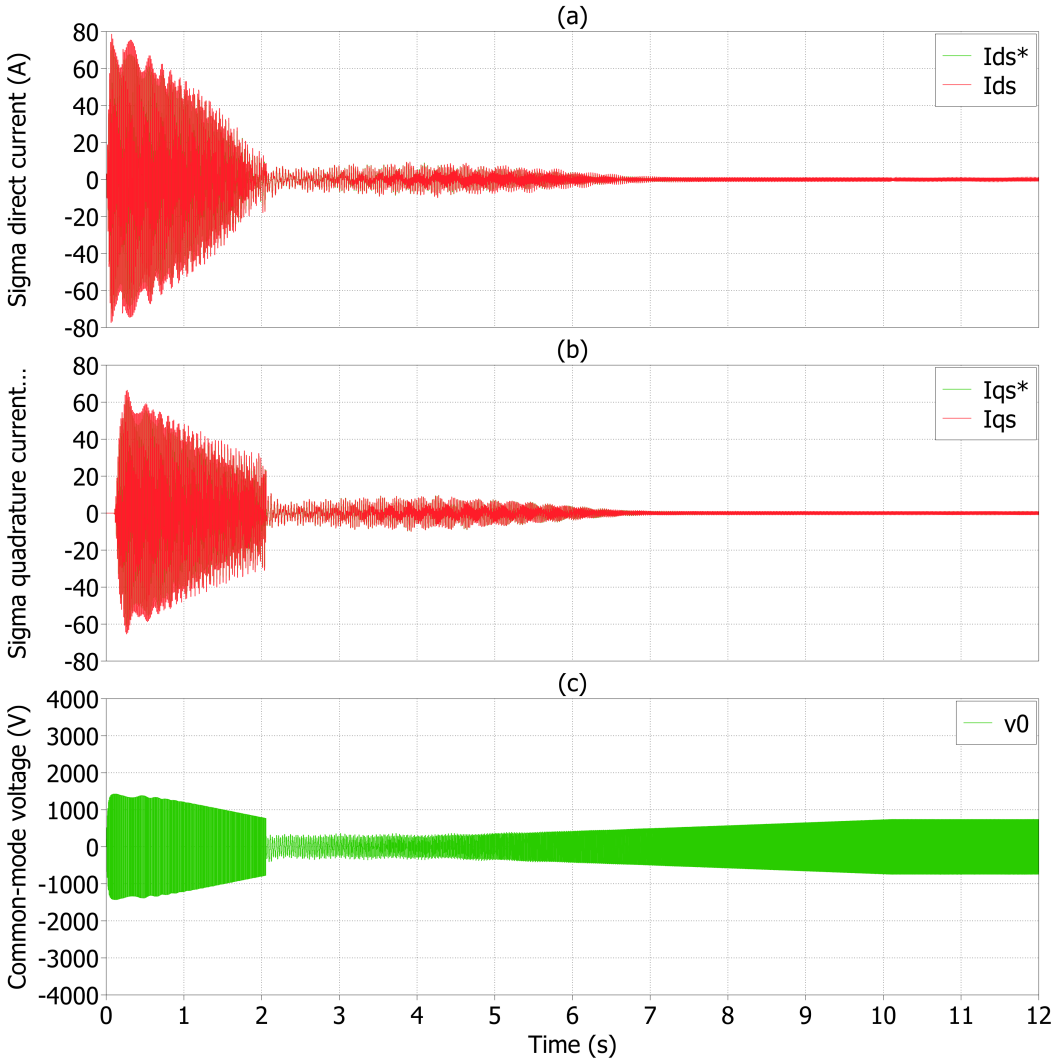


Figure 6.59: *Circulating currents i_d^{Σ} (a), i_q^{Σ} (b), and common-mode voltage (c) when a variable DC-link is used and the cell capacitance is reduced by* 30%.

operating in over-modulation was illustrated. It is worth pointing out that the global balance control, i.e. the control to regulate the total energy among the six arms, works appropriately even when the FBSMs and HBSMs are unbalanced. However, due to the increase in the cell voltages of one or other type of cell, the over-voltage protection will eventually trigger an alarm to disconnect the whole system and avoid damaging the switches. The performance of the two proposed local balance strategies, CLC-I and CLC-II, was tested when the hybrid MMC operates in over-modulation. The local balance control ensures that the arm energy is evenly shared between the HBSMs and the FBSMs within each arm. Both proposed strategies are compared when the modulation index is increased from m=1.7 up to m=2.5, and both controllers can ensure

the local balance between the FBSMs and HBSMs over the whole modulation index sweep. CLC-II is more likely to be used since it can operate with unity power factor. Next, the operation of the closed-loop controller was evaluated. It is concluded that CLC-I has a faster response than CLC-II to re-balance the FBSMs and HBSMs if the hybrid MMC is working in over-modulation. Finally, the performance of the control under a step-load is also considered. In this case, the control is able to ensure the local balance for CLC-I and CLC-II. In addition, two simulation tests were considered regarding the operation of the back-to-back MMC-based drive application. First, the operation of the drive converter was tested with a constant and a variable dc-link voltage. In the latter case, the length of the low-frequency mode and the common-mode voltage injected into the machine stator are reduced in the same proportion as the dc-link voltage. Finally, a second application of operation with a reduced dc-link voltage is shown. Reducing the dc-port voltage makes it possible to reduce the cell capacitance without increasing the capacitor voltage oscillations in the whole speed range.

A quadratic torque load profile was employed for the drive applications studied in this chapter. The selection of this particular load profile is based on the literature review, where it has been shown that the MMC should be preferred to drive quadratic-torque profile loads [24, 133, 161, 162]. For MMC-based drive converters, the most common solution is to injected a high-frequency common-mode voltage along with circulating current to reduce the capacitor voltage oscillations during low mechanical speed [36]. The practical limitation of the MMC for different torque load profiles is the high arm current required during low mechanical speed. Theoretically, it is possible to use an MMC for different loads, such as, constant torque loads. However, the sub-modules switches have to be oversized. In [24], it was possible to drive a load with 40% of its rated torque at the machine start-up without over-sizing the sub-modules switches.

The next chapter explains the experimental rig built to validate the proposed

control of the hybrid MMC and the drive application using a back-to-back MMC converter.

Chapter 7

Experimental rig

7.1 Introduction

This chapter presents the experimental rig used for the validation of the proposed strategies. First, the experimental rig used to validate the hybrid MMC is presented. Then the experimental rig used to validate the back-to-back MMC is described. Both systems used the same control platform based on a DSP board TMS320C6713 DSK by Texas Instrument and FPGA boards to produce the gate signals, read the A/D channels, manage the hardware protection, among other functions. In addition, this chapter depicts the measurement stage, the control system, and the interrupt routine that implements the proposed controllers.

7.2 Converter implementation

An experimental prototype of a 5kW-hybrid MMC was designed and implemented to validate the proposed control strategies. In this case, the hybrid MMC has a total number of 18 sub-modules. Fig. 7.1 shows the circuit diagram of the hybrid MMC, and Fig. 7.2 depicts its implementation in the laboratory. The parameters of the experimental system are listed in Table 7.1. The controller was programmed in a DSP Texas Instrument model TMS320C6713

platform augmented by 3 FPGA (Actel) boards (shown at the bottom right of Fig. 7.2). The FPGA boards were developed in the PEMC group [163]. The FPGA boards are used to read the analogue-to-digital converters (ADCs), implement the hardware protection system (over-currents and over-voltages), and generate each cell's pulse-width modulation (PWM) signals. The ADC used is the model *LTC1407* that can sample at 3Msps and it has two differential channels. The grid is emulated using a chroma 61511 programmable supply (shown at the bottom left of Fig. 7.2), and the load is composed of resistors connected to the dc-port side of the hybrid MMC (see Fig. 7.1). In this case, each arm is composed of 2 HBSMs and 1 FBSM.

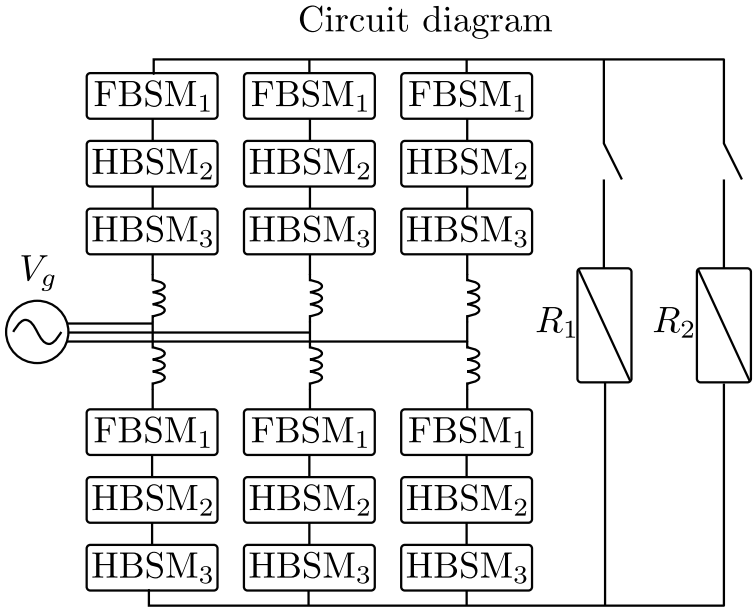


Figure 7.1: *Circuit diagram of the experimental MMC prototype composed of one FBSM and 2 HBSMs in each arm.*

The FBSMs and HBSMs are implemented using the IGBT Infineon model F4-50R06W1E3, its maximum current is 50 A. Figure 7.3.(a) and (b) depicts an HBSM and an FBSM respectively. In both cases, the same PCB is used, but for the HBSM cell, only one leg of the H-bridge has been populated. The sub-modules were inherited from a previous research project within the PEMC group at the University of Nottingham [163]. The pulse signals from the PWM are transmitted through an optical fibre link to avoid issues associated with electromagnetic noise.

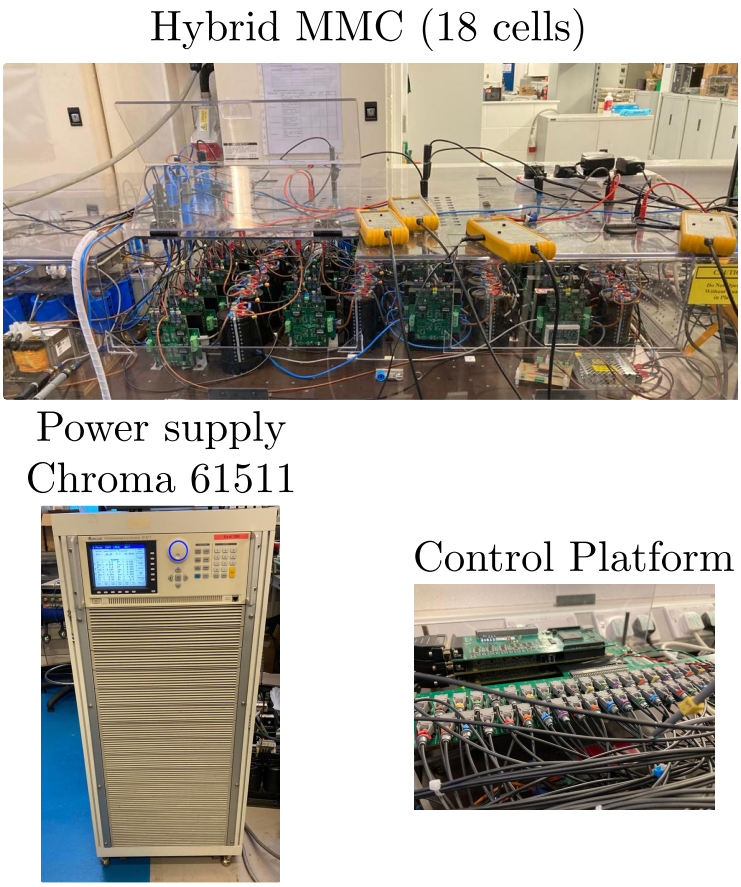


Figure 7.2: *Experimental System. At the top are the 18 FBSM and HBSM modules. Bottom left is the Chroma 61511 programmable power supply. Bottom right is the control platform.*

Table 7.1: Parameters of the hybrid MMC.

Parameter	Description	Value
N_H	HBSMs (IGBT (F4-50R06W1E3/ 50A) per arm	2
N_F	FBSMs (IGBT (F4-50R06W1E3/ 50A) per arm	1
$6N$	Total number of cells	18
V_g	Magnitude of the grid voltage	120V
v_C^*	Sub-module voltage reference	100V
f_c	Carrier frequency (PD-PWM modulation)	8kHz
L	Arm inductance	4.15 mH
C	Cell capacitor (B43564-D4338-M/ 350V)	3.3 mF
R_1	Resistive load	11 Ω
R_2	Resistive load	22 Ω

The gate-drive circuit of each IGBT is shown in Fig. 7.4. In this case, the gate-drive circuit has two options to implement the dead-time for each IGBT turn-on: analogue-based or software-based solution. In the first case, the dead-time is implemented analogically using an RC circuit with an anti-parallel

(a) (b)

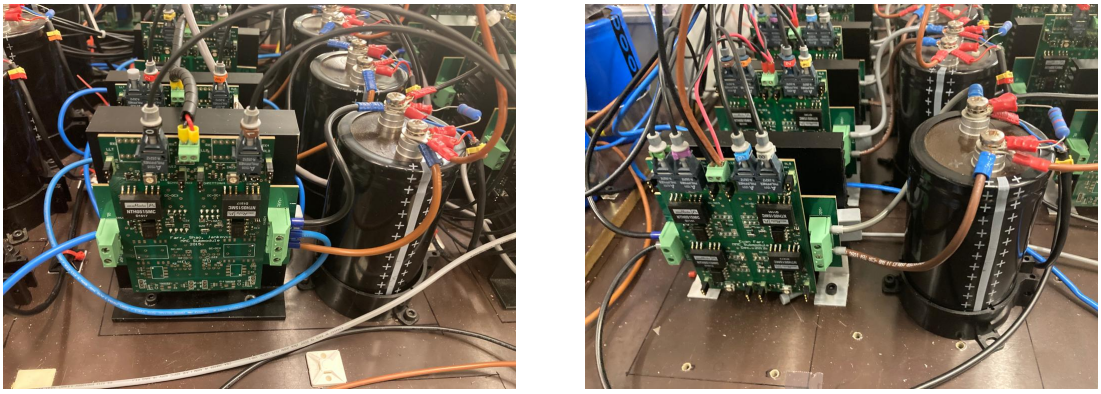


Figure 7.3: *Laboratory implementation of a HBSM (a) and FBSM (b).*

diode. When a turn-on signal is applied, it has to charge the capacitor C_{dt} before the signal changes the output of the Schmidt-trigger buffer of Fig. 7.4. Conversely, when a turn-off signal is applied, the anti-parallel diode discharge the capacitor voltage C_{dt} immediately; thus, the delay is only added when the IGBT is turned on. The dead-time is regulated by changing the resistance value of the trimmer of Fig. 7.4.

In the second case, the RC circuit is bypassed, and the dead-time is added in the FPGA firmware. The VHDL code of the dead-time function is depicted in the Appendix B.2. Regardless of how the dead-time is included, each IGBT is driven through an optocoupler (model Broadcom HCPL-3120); the optocoupler is added to provide galvanic isolation between the gate-emitter terminals of each IGBTs within one sub-module. In this case, the optocoupler is fed with an isolated ±15 V power supply. In addition, anti-parallel Zener diodes are connected in parallel between the gate-emitter terminals to limit the applied voltage V_{GE}; this is done to avoid damaging the IGBT isolation between the gate and emitter terminals.

In addition, a back-to-back hybrid MMC has been built to validate the proposed control of the dc-link voltage for drive applications. The grid-side converter is a hybrid MMC composed of 18 sub-modules (1 FBSM and 2 HBSM per arm), while the machine-side converter is an HBSM-based MMC composed of 18 cells. In this case, a controllable voltage source AMETEK model MX45

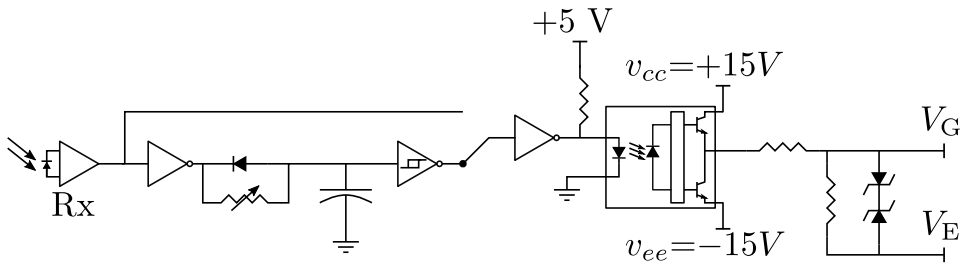


Figure 7.4: *Gate-drive circuit of each IGBT to generate the pulse signals.*

is used as the grid. The topology is shown in Fig. 7.5.

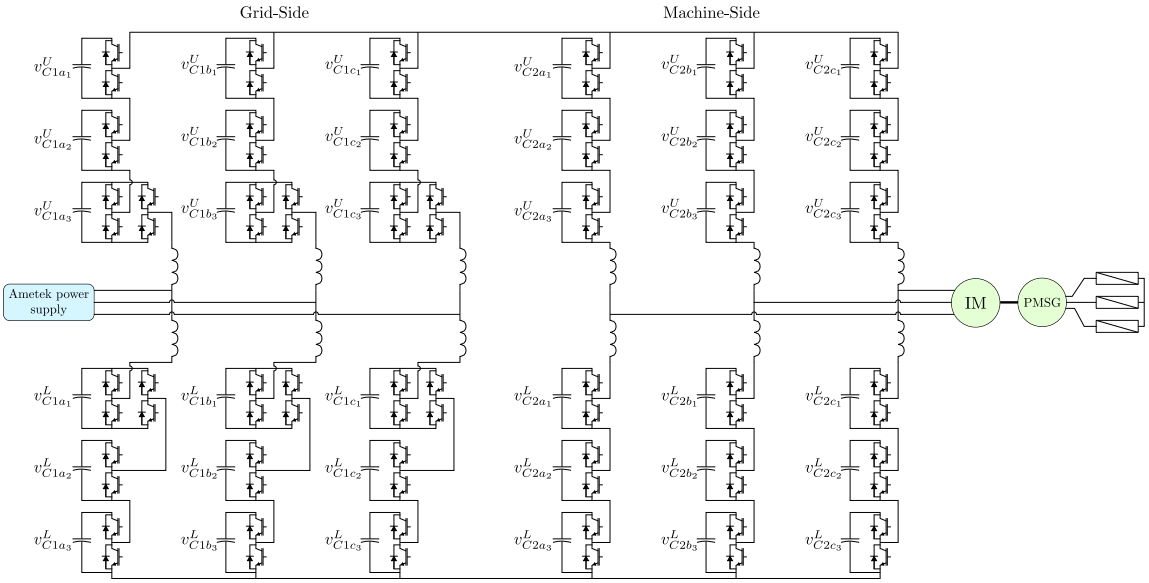


Figure 7.5: *Circuit diagram of the experimental back-to-back modular multilevel converters.*

The experimental setup of the back-to-back modular multilevel converter is shown in Fig. 7.6. In addition, the connection between both converter sides along with their control platform is depicted in Fig. 7.7. Both control platforms can communicate through a serial peripheral interface (SPI) between both master FPGA boards. The SPI link is implemented on each FPGA; its code is explained in the Appendix.

The parameters of the experimental rig for the back-to-back applications are shown in Table 7.2. In this case, each cell is built using the MOSFET Infeneon model IRFI4227PBF that has a maximum current equal to 47 A.

Each converter is controlled by a DSP *Texas Instrument* 6713 control platform. The machine-side control calculates the dc-port voltage reference E^* according

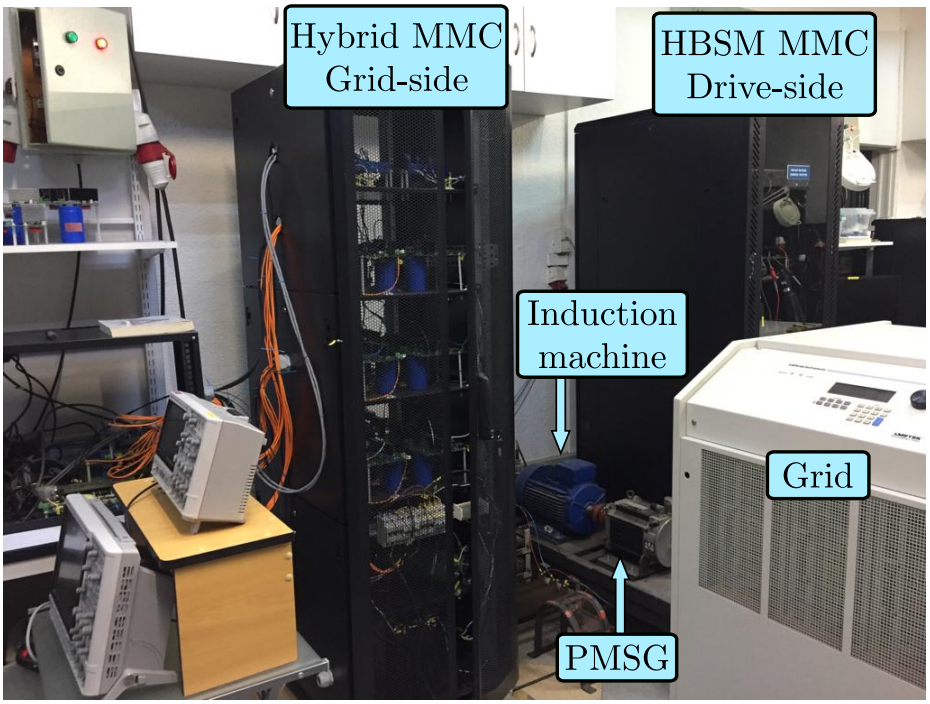


Figure 7.6: *Experimental setup of the hybrid back-to-back modular multilevel converter.*

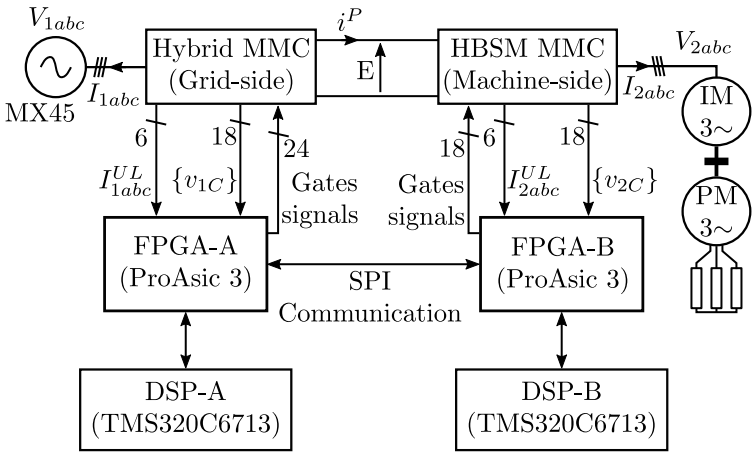


Figure 7.7: *Connection of the grid- and machine- sides converters along with their respective control platform.*

to (5.49) using the machine variables in each sampling period T_S. Then, the dc-link voltage reference E^* is sent to the grid-side control platform through a serial communication interface (SPI) implemented using optical fibre. The master and slave SPI interface are programmed in the machine-side and grid-side FPGA board; these VHDL codes are depicted in B.3. The induction machine is mechanically coupled to a permanent magnet generator (PMG) that feeds a resistive load. The parameters of the induction machine are listed

Table 7.2: Parameters of the hybrid MMC.

Parameter	Description	Value
N_H	HBSMs per arm (grid-side)	2
N_F	FBSMs per arm (grid-side)	1
N_2	HBSMs per arm (machine-side)	3
C_1	Cell capacitance (grid-side)	2200 μF
C_2	Cell capacitance (machine-side)	4700 μF
L_1	Arm inductance (grid-side)	5 mH
L_2	Arm inductance (machine-side)	2.5 mH
v_{C1}^*	Cell capacitor voltage reference (grid-side)	100 V
v_{C2}^*	Cell capacitor voltage reference (machine-side)	100 V
V_1	Grid voltage	150 V
f_1	Grid frequency	50 Hz
E	Dc-port voltage	130−300 V

in table 7.3.

Table 7.3: Parameters of the induction machine.

Parameter	Description	Value
R_s	stator resistance	0.66 Ω
R_r	rotor resistance	0.724 Ω
L_{ls}	stator leakage inductance	2.23 mH
L_{lr}	rotor leakage inductance	2.23 mH
L_m	magnetizing inductance	0.138 H
p	number of pole pairs	1

7.3 Voltage and current measurement board

The voltage sensor LEM model LV 25-P is used to measure the voltage across each sub-module, dc-link voltage, and the line-to-line grid voltages. The circuit diagram of this transducer is shown in Fig. 7.8. In this case, the voltage transducer is fed with ±15 V. The voltage sensor is based on a hall-effect closed-loop circuit to measure the input voltage; in addition, it provides galvanic isolation between the measured variable and the control platform. The measured voltage is transformed into a current through the measurement resistor R_m. Then, the transducer output current is sent to the FPGA board, where these currents are converter to voltages between 0 and 5 V through a burden resistor R_b. The FPGA board has ten analogue-to-digital channels

(ADCs); each ADC senses the voltage across a burden resistor R_b.

The measurement resistor is equal to R_m=20 kΩ, which gives a nominal input current (i_{PN} = 10 mA) when the measured voltage is equal to 200 V. On the FPGA board, the voltage across the burden resistors is limited between 0 and 5 V, in this case, the burden resistor is equal to R_b=100 Ω.

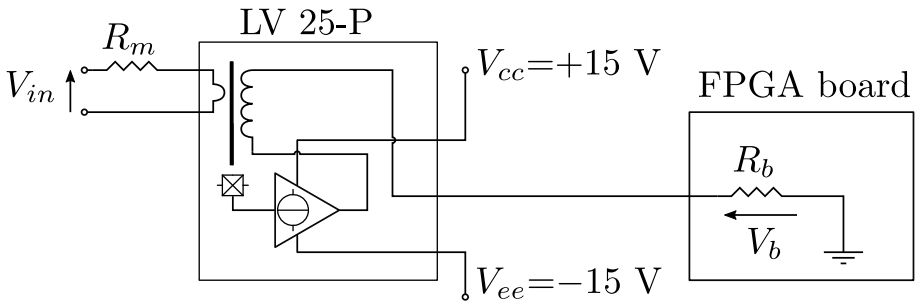


Figure 7.8: *Voltage transducer LEM LV 25-P circuit diagram.*

To measure the arm currents, the current sensor LEM LA 55-P is used. The circuit diagram of this sensor is shown in Fig. 7.9. In this case, the current is directly measured without a measurement resistor. A burden resistor is also required to measure the equivalent voltage on the FPGA board; in this case, a burden resistor equal to R_b=200 Ω is used. Each current transducer has two primary turns. The total current has to be lower than 50 mA to avoid damaging the current sensor.

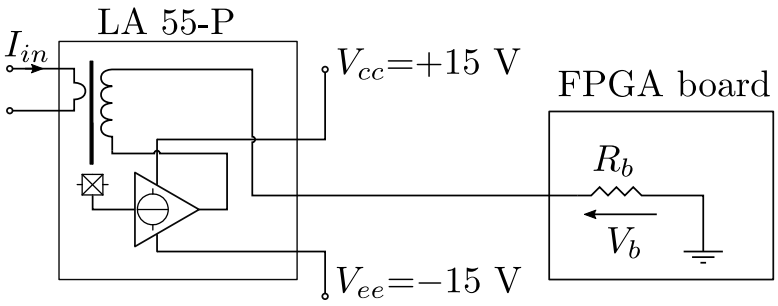


Figure 7.9: *Current transducer LEM LA 55-P circuit diagram.*

7.4 DSP and FPGA board

The control algorithm is implemented in a DSP *Texas Instrument* model TMS320C6713. The DSP operates along with the FPGA boards as an in-

terface between the control platform and the converter. The main functions of the FPGA boards are to interface the A/D converters; generate the interrupt pulse for synchronisation; implement the hardware protection system (over-currents and over-voltages), and generate the pulse-width modulation signals (PWM) of each cell. In particular, the FPGA board is based on the model ProAsic 3 by Actel. Both MMC sides have the following variables to be measured: 18 cell capacitor voltages, 6 arm currents, and 1 dc-link voltage. Notice that the output current in the AC and DC port can be calculated using the MMC arm currents. In addition, for the grid-side converter it is necessary to measure the grid voltages v_{ab}, v_{bc}, and v_{ca}. Since each FPGA board has ten analogue-to-digital channels, each MMC-side needs 3 FPGA boards to read all the required measurements in each sampling period. When more than one FPGA board is connected, one acts as a master while the rest are slaves. The Master FPGA board is in charge of generating the PWM pulse for each sub-module. In particular, at the end of the control routine, the modulation index of each cell is sent to the master FPGA board.

In the master FPGA board, a phase-shift modulation scheme has been implemented. In this case, three triangular carriers are defined for each cell within one arm, as shown in Fig. 7.10. Each cell has its modulation index. The modulation index for each cell is updated whenever its carrier reaches the maximum count C_{max}. In particular, C_{min}=0 and C_{max}=3125; consequently, the modulation index of each cell are scaled in this range. The phase shift between carriers is programmable through the DSP program.

The master FPGA board generates the interrupt signal to synchronise all the FPGA boards. The DSP routine is depicted in Fig. 7.11. First, in the main code of the DSP program, the converter variables and the gains of the A/D converters are initialised. Next, the FPGA registers are reset; this step is required to erase any error flag that could be activated by hardware or software protection. In addition, the DSP has to specify the interruption period; in this case, the interruption period is the same as that of the triangular carrier

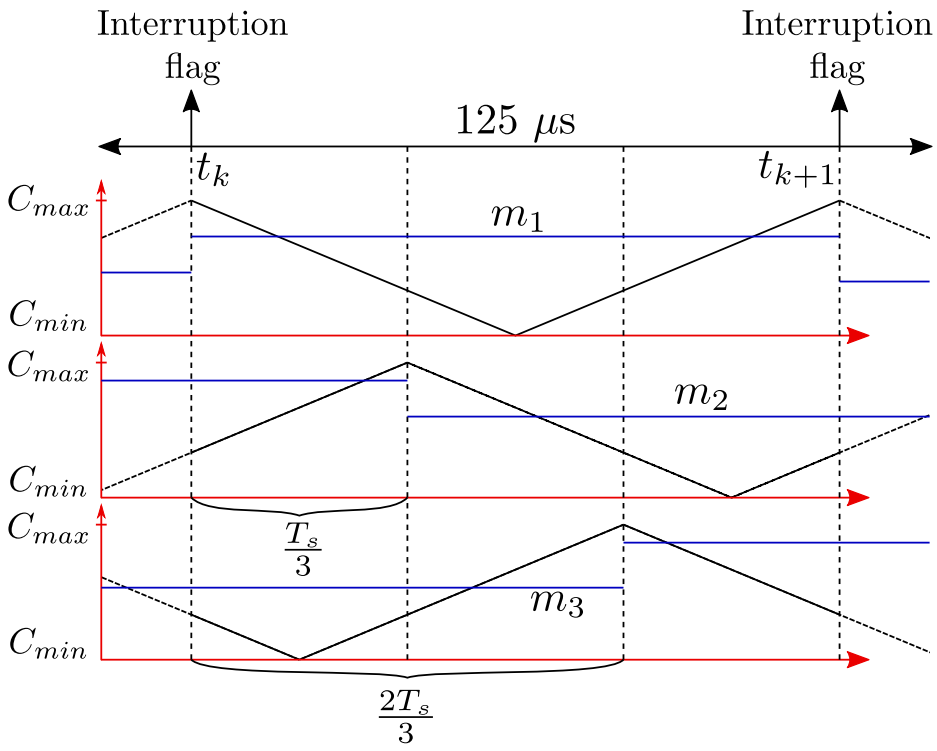


Figure 7.10: *Pulse width modulation per arm.*

period, in particular, T_s=125 μs. Next, the offset of each A/D channel is estimated by calculating the average of 1000 measurements in each channel with the converter out of operation, and then the offset is subtracted from each measurement. Finally, some protocols are activated, such as the hardware protections, the LED display within the master FPGA board, and the host client to read the converter through Matlab.

The hardware protection is implemented in the FPGA board to sense the output of the ADCs directly. Each one of the 10 A/D channels in each FPGA board has its hardware protection. The protection threshold of each channel is configurable from the DSP board.

The LED display is used to show the current converter state, namely: Operation condition, fault condition, or pre-charging. Finally, the host client is a MatLab script developed within the PEMC group to measure DSP variables in real-time.

The interruption routine for the hybrid MMC is depicted on the right side of Fig. 7.11; for the machine-side, the interruption routine is similar, but it does

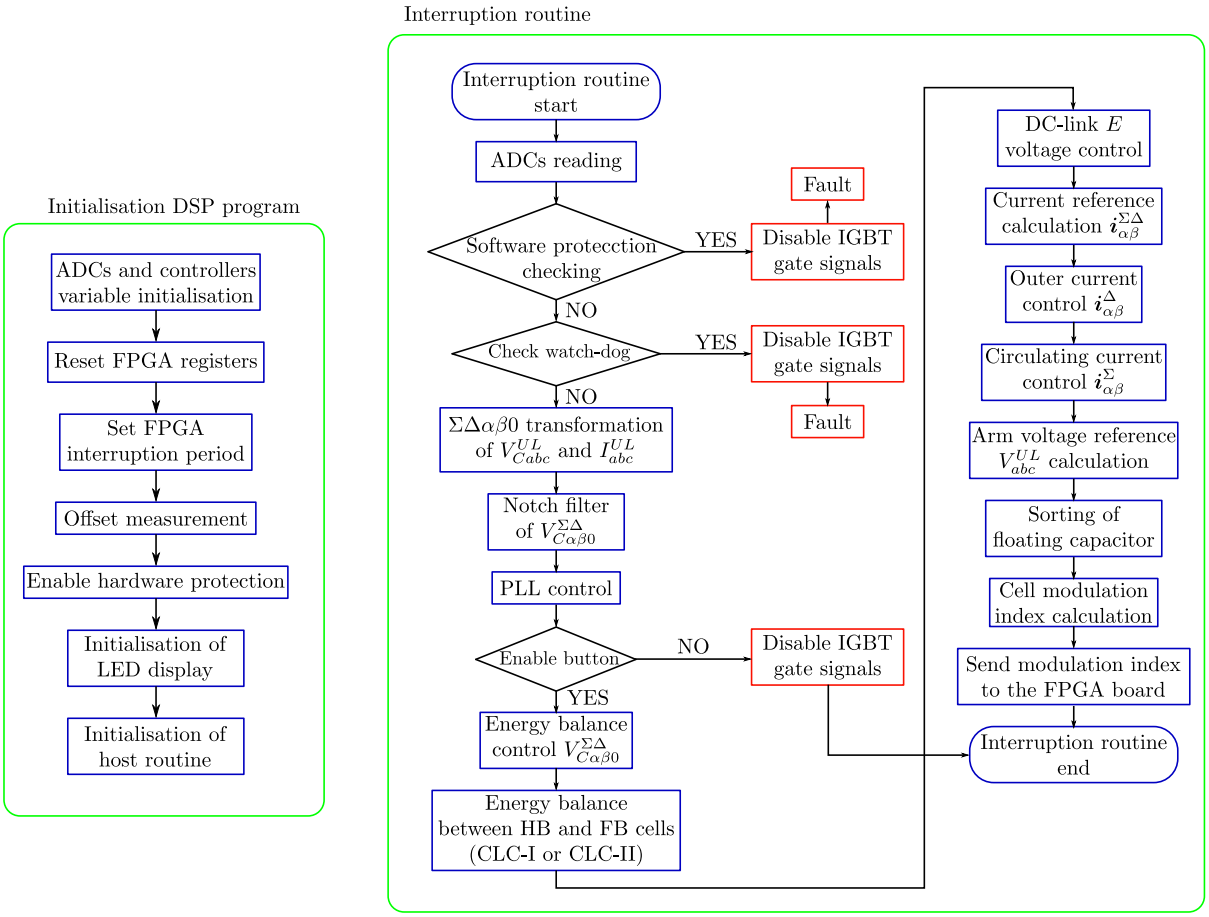


Figure 7.11: *Diagram block of the control routine.*

not have the voltage balance control between HBSMs and FBSMs. The master FPGA board generates an interruption pulse every 125 μs; this pulse launches the *Interruption routine*. Initially, all the A/D channels are read by each FPGA board and sent to the DSP board. If any value exceeds its maximum threshold, the software protection of that measurement is triggered, and the IGBT gate signals are disabled. The system state is locked in fault condition; therefore, the DSP program has to be uploaded again to restart its operation. Next, the watch-dog flag is checked; this flag indicates if the first-in-first-out (FIFO) list used to manage the phase-shift among carriers is empty; if this is the case, the interruption routine is terminated, and the converter state is set to a fault condition. If the system does not have any triggered protection flag, the rest of the DSP routine is executed.

Initially, the total capacitor voltage of each arm is calculated. Then, the converter variables are expressed in the $\Sigma\Delta\alpha\beta0$ reference frame. The total

capacitor voltages $V_{C\alpha\beta0}^{\Sigma\Delta}$ are then filtered using notch filters, and finally, a phase-lock loop (PLL) is used to estimate the voltage grid angle θ_1 that is required to connect the hybrid MMC with the grid.

To activate the closed-loop control, the enable button has to be switched on. First, the outer energy balance between arms is performed. Then, if the converter is operating in over-modulation, the energy balance between the HBSMs and FBSMs is done. The outer energy control produces the reference of the circulating currents and outer currents. Finally, the inner current control gives the arm voltage reference $V_{\alpha\beta0}^{\Sigma\Delta}$. The arm voltage reference $V_{\alpha\beta0}^{\Sigma\Delta}$ is expressed in the natural reference frame V_{abc}^{UL}. Then the voltage reference of each arm is sent to the modulation scheme.

7.5 Summary

This chapter presents the main characteristics of the experimental rig to validate the operation of the hybrid MMC and the operation of the back-to-back converter for drive applications. Both systems used the same control platform based on a DSP board TMS320C6713 DSK by Texas Instrument and FPGA boards to produce the gate signals, read the A/D channels, manage the hardware protections, among other functions. The measurements are taken through FPGA development boards, each one is able to measure up to 10 differential signals, consequently, each MMC requires 3 FPGA boards to measure all the relevant variables. LEM transducers are considered to measure the voltages and currents. The next chapter presents the experimental results used to validate the proposed control strategies. In particular, the local balance for a single hybrid MMC system is validated. To validate the operation of the hybrid MMC, a prototype composed of 18 sub-modules has been built, in this case each arm has 1 FBSM and 2 HBSMs. Then, the operation of a back-to-back converter for drive applications is also considered. In this case, the machine-side converter is composed of 18 HBSMs, and the grid and ma-

chine side converter control platforms are linked using an SPI communication link.

Chapter 8

Experimental results

8.1 Introduction

This chapter presents the experimental results to validate the control of the hybrid MMC in over-modulation (m>2) under different conditions, in this case a hybrid MMC composed of 18 cells (1 FBSM and 2 HBSM per arm) is considered. In addition, the operation of the back-to-back MMC for a drive application is also validated, in this case, the grid-side converter is an hybrid MMC composed of 18 cells (1 FBSM and 2 HBSM per arm) while the machine-side converter is a HBSM-based MMC composed of 18 cells. The experimental rigs discussed in chapter 7 are used to evaluate the proposed control for the hybrid MMC and for the back-to-back MMC case. The proposed strategies presented in chapter 5 are validated experimentally. The following experimental tests are considered:

1. Operation of an uncompensated Hybrid MMC in the over-modulation range: The aim of this test is to shown the imbalance in the capacitor voltages of the HBSMs and FBSMs when the hybrid MMC operates in over-modulation and the voltage control between the FBSMs and HBSMs is disabled.

2. Operation of CLC-I during over-modulation: In this section, the pro-

posed control strategy CLC-I is tested when the hybrid MMC operates in over-modulation. In this case, the power factor is decreased to ensure the change of sign of the arm current. Then, the proposed strategy CLC-I is compared with similar approaches found in the literature.

3. Operation of CLC-II during over-modulation: In this test, the proposed control strategy CLC-II is validated while the hybrid MMC operates in over-modulation. In this case, a circulating current component is injected to ensure the change of sign of the arm currents. Then, this strategy is compared with similar approaches presented in the literature.

4. Closed-loop local balance control: The operation of the closed-loop local balance control is tested. In this test, the feed-forward currents are underestimated and as a consequence the FBSMs and HBSMs capacitor voltages start to drift apart. Then, the closed-loop controller is enable to correct the capacitor voltage imbalance.

5. Dynamic response under load-step variation: The proposed capacitor voltage balance control are tested under step-load variation. In both cases, the balance between HBSMs and FBSMs is accomplished.

6. Steady-state operation of the proposed strategies: This experimental test shows the steady-state response of the cell capacitors of the FBSMs and HBSMs for the hybrid MMC when it operates in over-modulation. A higher second harmonic is produced when the system operates with CLC-II in comparison with the case in which CLC-I is used.

7. Back-to-back drive converter: In this experimental test, the operation of the back-to-back is shown. The grid-side converter is a hybrid MMC while the machine-side converter is a HBSM-based MMC. The operation with fix and variable dc-link voltage is shown. When the system operates with a reduced dc-link voltage, the duration of the low-frequency mode

is reduced. In addition, the peak value of the common-mode voltage is also reduced in the same proportion than the dc-link voltage.

8.2 Operation of an Uncompensated Hybrid MMC in the over-modulation range

When a hybrid MMC operates in over-modulation (m>2), the arm currents become unipolar if neither of the control systems depicted in Fig. 5.6 is enabled. This is experimentally demonstrated in Fig. 8.1. In this case the hybrid MMC is feeding a resistive load R_1=11 Ω at the dc-port side. Initially, the hybrid MMC operates with a modulation index m=1.7 equivalent to E=141V and then the modulation index is ramped from m=1.7 to m=2.55 (i.e. $E{\approx}94V$). Fig. 8.1(a) shows waveforms for the capacitor voltages of the upper arm v_{Ca1}^{U} (FBSM, yellow) and v_{Ca2}^{U} (HBSM, green), and those of the lower arm are v_{Ca1}^{L} (FBSM, blue) and v_{Ca2}^{L} (HBSM, red) for phase a. In addition, the grid current i_a, the arm currents i_a^U (upper) and i_a^L (lower), and the dc-port voltage E are shown in the scope waveforms in Fig. 8.1(b). An zoomed view of this figure is shown in Fig. 8.1(c) expanding the zone where the arm currents become negative. After t_1, the modulation index is m>2 and, as a consequence, the arm currents become unipolar and the capacitor voltages of the FBSMs and HBSMs start to unbalance. At t_2, the modulation index is m=2.55, and the FBSMs trigger the over-voltage protection $V_{\max}$ = 140V and the converter is shut down. Notice that for m>2, the capacitor voltages of the FBSMs increase while those of the HBSMs decrease.

8.3 Operation of the proposed control system (CLC-I) for over-modulation operation

In this section the operation of the control system labelled as CLC-I, discussed in Section 5.3 and depicted in Fig. 5.6(b), is presented. The currents

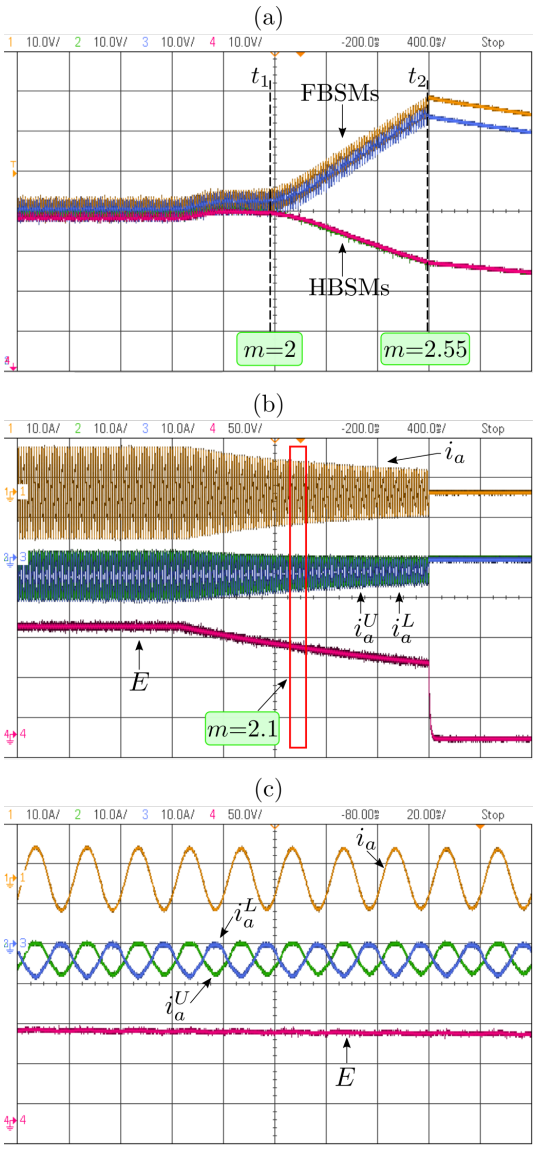


Figure 8.1: *(a) Capacitor voltages of v^U_{Ca1} (yellow), v^U_{Ca2} (green), v^L_{Ca1} (blue), and v^L_{Ca2} (red); (b) grid current i_a (yellow), arm currents i^U_a (green) and i^U_a (blue), and dc-port voltage E (red); (c) zoomed view of (b).*

and voltages produced by the converter when the modulation index is ramped from m=1.7 to m=2.5 are shown in Fig. 8.2. The minimum reactive current to ensure the local balance between FBSMs and HBSMs is derived by solving the optimization problem (5.27) along with the action of the closed-loop compensator [see Fig. 5.6]. Fig. 8.2(a) shows the cell capacitor voltages v^U_{Ca1} (FBSM, yellow), v^U_{Ca2} (HBSM, green), v^L_{Ca1} (FBSM, blue), and v^L_{Ca2} (HBSM, red). Notice that the FBSMs and HBSMs remain balanced during the whole modulation index sweep. The grid currents and dc-port voltage are shown in Fig. 8.2(b) with the grid current reaching a peak-to-peak value of ≈22.9A at

the beginning of the test and a final value of ≈14.7A at the end of the test. Notice that the grid current is increased by the CLC-I strategy when m>2. This is because reactive current is added to the grid current in order to produce a bipolar current in the arms. A zoomed view, when m=2, is shown in Fig. 8.2(c). Once m=2.5, the magnitude of the reactive current is i_q≈5.1A and the power factor is 0.7. In steady-state, the capacitor voltage oscillations are less than 6.2V.

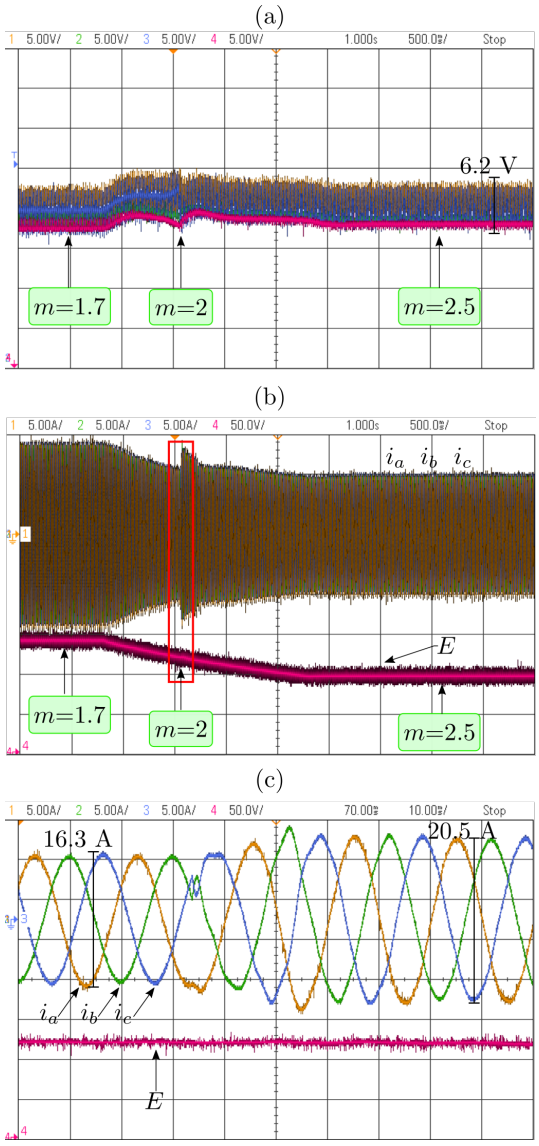


Figure 8.2: *Capacitor voltage balance using CLC-I for $m = 1.7 \rightarrow 2.5$. (a) capacitor voltages of v^U_{Ca1} (yellow), v^U_{Ca2} (green), v^L_{Ca1} (blue), and v^L_{Ca2} (red); (b) grid currents i_{abc} and dc-port voltage E; and (c) zoomed view of the (b).*

8.4 Performance Comparison Between CLC-I and similar strategies previously discussed in the literature

In [42, 156] among other works, the imbalance problem is also addressed by manipulating the reactive component of the grid currents, but without including the external voltage control loop shown in the nested control system shown in Fig. 5.6. In the previous publications, it is claimed that the power factor to ensure bipolar arm currents is given by:

$$m\cos(\varphi) < 2 \tag{8.1}$$

From (8.1), the reactive current (for m>2) is:

$$\frac{\sqrt{m^2-4}}{2}|i_d| \leq |i_q| \tag{8.2}$$

Notice that this expression only guarantees the change of sign of the arm currents. However, it does not necessarily ensure capacitor voltage balance among FBSMs and HBSMs. In addition, (8.2) only gives a lower bound for the reactive current magnitude. Therefore, a scaling factor has to be included in order to ensure capacitor voltage balance for the whole operating range of the modulation index. Consequently, (8.2) is rewritten as:

$$i_q = \alpha_1 \frac{\sqrt{m^2-4}}{2}|i_d| \tag{8.3}$$

Since there is no explicit expression given to calculate the required i_q^* (8.3), such as the one discussed in this thesis (see Section 5.3.1), the minimum reactive current (i.e. α_1) has to be obtained using simulation work and/or a methodology based on trial and error. In order to demonstrate the potential difficulties of this approach, a test was conducted on the experimental prototype. Follow-

ing several iterations of simulation and experimental tests and the use of trail and error, it was determined that α_1=1.33 ensures capacitor voltage balance between the FBSMs and the HBSMs for m=2.5. However, α_1=1.33 does not ensure capacitor voltage balance for lower modulation indexes. In Fig. 8.3(a)-(b), the modulation index reference is changed from m=1.7 to m=2.5 and, although the capacitor voltages are balanced once m=2.5, they drift apart for m=2.1 as shown in Fig. 8.3(b). If the modulation index is ramped from m=1.7 to m=2.1, the capacitor voltages remain unbalanced as shown in Fig. 8.3(c) with a capacitor voltage error of ≈7V. This problem is produced by the non-linearities of the system (see Fig. 5.7), and the non-linearities of the term $\sqrt{m^2-4}$ given in (8.3). Conversely, with the proposed CLC-I strategy, this problem is not apparent [see Fig. 8.2(a)]. This is because the minimum current to balance the capacitor voltage is obtained using an explicit expression (see Section 5.3.1), and the external voltage control loop, depicted in Fig. 5.6, ensures regulation even if the reactive current is slightly in error.

8.5 Operation of the proposed control system (CLC-II) for over-modulation operation

The same modulation index variation (m=1.7→2.5) considered in the experimental results presented in Fig. 8.2 is repeated but using the CLC-II strategy. In this case, the circulating current component $i_q^{\Sigma+}$, obtained using the methodology discussed in Section 5.3.2, is utilised to balance the FBSMs and HBSMs during over-modulation (m>2).

Fig. 8.4(a) shows the capacitor voltages v_{Ca1}^U (yellow), v_{Ca2}^U (green), v_{Ca1}^L (blue), and v_{Ca2}^L (red). As shown in Fig. 8.4, at the beginning of the test the grid current (peak-to-peak) is ≈22.9A (similar to that depicted in Fig. 8.2) while at the end it is ≈11.2A; this is less than the value obtained for the CLC-I case which was ≈14.7A. As discussed previously, the difference in magnitude

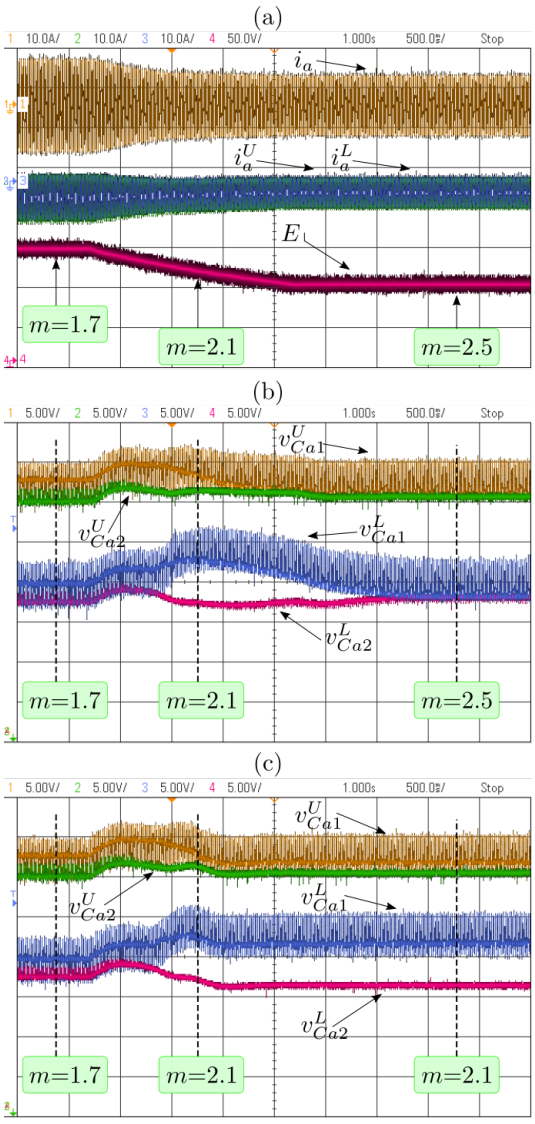


Figure 8.3: *(a) Grid current i_a (yellow), Arm currents i_a^U (green) and i_a^L (blue), dc-port voltage E (red). Capacitor voltages of v_{Ca1}^U (yellow), v_{Ca2}^U (green), v_{Ca1}^L (blue), and v_{Ca2}^L (red) when (a) $m = 1.7 \rightarrow 2.5$ and (b) $m = 1.7 \rightarrow 2.1$.*

is produced because the CLC-I strategy uses reactive grid-current to balance the HBSM-FBSM capacitor voltages.

In Fig. 8.4, circulating current is applied to the arm currents to balance the capacitor voltages. For m>2 a current $i_q^{\Sigma+}$ is injected, [see lower waveforms of Fig. 8.4(b) and (c)], with a peak-to-peak value of ≈7.5A. Notice that there is a small voltage difference increase ≈3V for m≈2.1 between the capacitor voltages of the upper and lower arms which becomes negligible after 0.15s. The maximum steady state voltage oscillation is 8.3V. A zoomed view of the grid current i_a, the arm currents i_a^U and i_a^L, the dc-port voltage E, and the

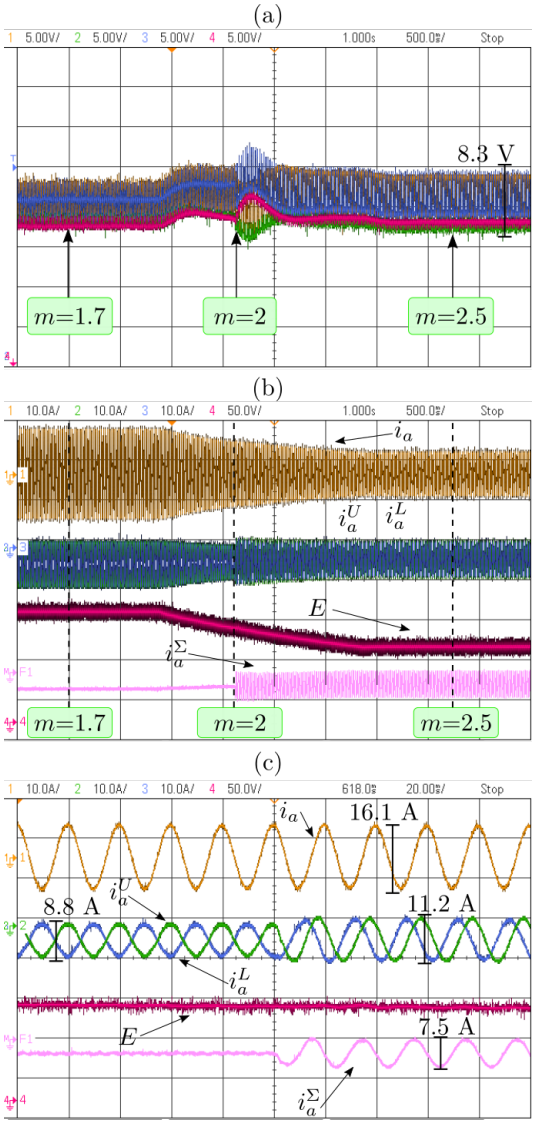


Figure 8.4: *(a) Capacitor voltages of v_{Ca1}^U (yellow), v_{Ca2}^U (green), v_{Ca1}^L (blue), and v_{Ca2}^L (red) . (b) Grid current i_a (yellow), arm currents i_a^U (green) and i_a^L (yellow), dc-port voltage E (red), and circulating current i_a^Σ (pink). (c) zoomed view of (b) when m=2.*

circulating current i_a^Σ are shown in Fig. 8.4(c) for the zone where $m\approx 2$.

As mentioned before, when CLC-II is applied, there is a reduced unbalance of ≈3V between the average voltages of the upper and lower arm. However, this variation is not permanent even if the system operates at $m\approx 2.1$ in steady state. To experimentally verify this, a ramp variation in the modulation index between m=1.7 to m=2.1 is realised. These results are shown in Fig. 8.5. Notice that the capacitor voltages v_{Ca1}^U, v_{Ca2}^U, v_{Ca1}^L, and v_{Ca2}^L remain balanced during the whole test as depicted in Fig. 8.5(a) with a capacitor voltage oscillation of ≈7.8V in steady state. The grid current i_a (yellow), arm currents

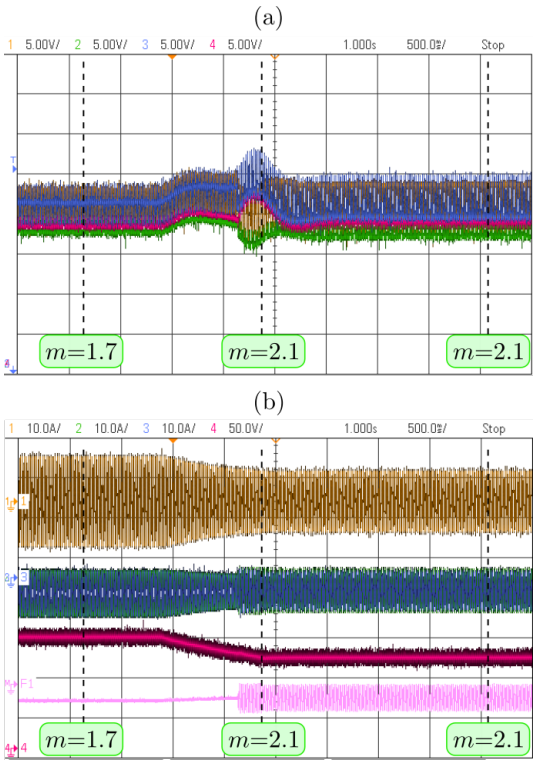


Figure 8.5: *(a) Capacitor voltages of v^U_{Ca1} (yellow), v^U_{Ca2} (green), v^L_{Ca1} (blue), and v^L_{Ca2} (red) . (b) Grid current i_a (yellow), arm currents i^U_a (green) and i^L_a (yellow), dc-port voltage E (red), and circulating current i^Σ_a (pink).*

i^U_a (green) and i^L_a (yellow), dc-port voltage E (red), and circulating current i^Σ_a (pink) are shown in Fig. 8.5(b).

8.6 Performance Comparison Between CLC-II and similar strategies previously discussed in the literature

In [30, 146], among other works, the utilisation of circulating current to avoid imbalance problems between the capacitor voltages of the HBSMs and FB-SMs, during over-modulation operation, is reported. Again an external voltage control loop was not considered in this previous work and a rigorous mathematical methodology to minimise the required circulating currents was neither proposed nor discussed. In [30], the injected reactive current is calculated to

ensure the bipolarity of the arm current. This is achieved using:

$$|i_q^{\Sigma+}| \geq \frac{i_d}{4}\sqrt{m^2-4} \tag{8.4}$$

However, the current required to balance the capacitor voltages of the HB-SMs and FBSMs is not necessarily equal to the minimum current required to achieved bipolarity. To ensure balancing for $m\approx 2.5$, (8.4) has to be multiplied by a constant $\alpha_2>1$ yielding:

$$i_q^{\Sigma+} = \alpha_2\frac{i_d}{4}\sqrt{m^2-4} \tag{8.5}$$

Similarly to the reactive current case discussed in Section 8.4, an explicit equation to calculate the value of α_2 which ensures the balance between the FBSMs and HBSMs was not given. Therefore, again, the value has to be obtained using simulation and/or experimental work combined with some heuristic procedures. Using this approach for the experimental prototype, the value that ensures capacitor voltage balancing for $m\approx 2.5$ is $\alpha_2=1.65$. Again, considering the strong non-linearities of the system [see Fig. 5.7 and (8.5)], this value is not necessarily appropriate for operating in steady state with smaller value of m.

To demonstrate the potential problems, Fig. 8.6(a)-(b) show the performance of the control strategy implied by (8.5), when the modulation index is changed from $m=1.7$ to $m=2.5$ and the required circulating current is calculated using (8.5) with $\alpha_2=1.65$. The grid current i_a, arm currents i_a^U and i_a^L, and the dc-port voltage E are also shown in Fig. 8.6(a). The capacitor voltages v_{Ca1}^U (FBSM, yellow), v_{Ca2}^U (HBSM, green), v_{Ca1}^L (FBSM, blue), and v_{Ca2}^L (HBSM, red) are shown in Fig. 8.6(b). Notice that for $m<2.5$ the capacitor voltages are unbalanced. If the modulation index reference is ramped from $m=1.7\rightarrow 2.1$ the capacitor voltages remain unbalanced as shown in Fig. 8.6(c). In this case, the capacitor voltage error is $\approx$15V which is a relatively large error considering

that the nominal voltage of each sub-module is 100V.

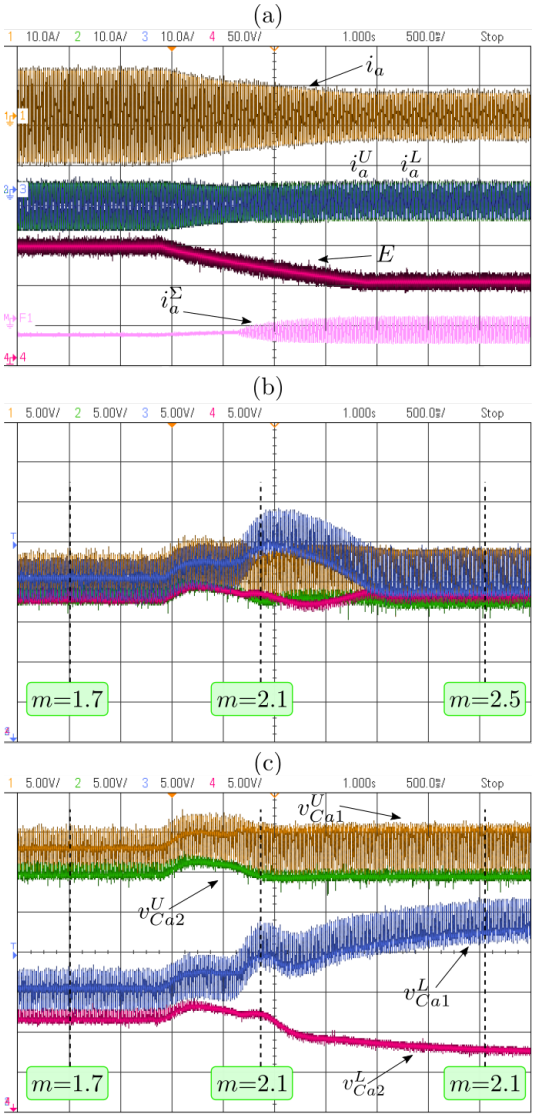


Figure 8.6: *(a) Grid current i_a (yellow), Arm currents i_a^U (green) and i_a^L (blue), dc-port voltage E (red), and circulating current i_a^Σ (pink). Capacitor voltages of v_{Ca1}^U (yellow), v_{Ca2}^U (green), v_{Ca1}^L (blue), and v_{Ca2}^L (red) when (a) $m = 1.7 \rightarrow 2.5$ and (b) $m = 1.7 \rightarrow 2.1$.*

As demonstrated in Sections 8.4 and 8.6, a single value of $\alpha_{1,2}$ in either (8.3) or (8.5) is not adequate to achieve capacitor voltage balancing between the HBSMs and FBSMs in the entire over-modulation range, particularly if the aim is to minimise the reactive or circulating currents which are required in the Hybrid MMC. Therefore, several values of $\alpha_{1,2}$ could be required to achieve good performance in a wide operating range. Moreover, extensive experimental and simulation work could be required to implement the previously reported approaches. Conversely, in the control systems proposed here, the explicit

equations can be used to minimise the required reactive or circulating current which is necessary to balance the HBSM-FBSM capacitor voltage for operating the hybrid MMC with any value of m. Moreover, there is an additional outer voltage control loop layer in the proposed approach. This additional loop [see Fig. 5.6(a)] is activated when the capacitor voltage balancing error $v_{CF}^{\Sigma} - v_{CH}^{\Sigma}$ is larger than a predefined hysteresis band.

8.7 Dynamic and steady state Performance of the outer control loop

This thesis proposes the use of a new outer voltage control loop layer to ensure the capacitor voltage balance between the HBSMs and FBSMs even if the feedforward currents have errors. This loop is depicted in Fig. 5.6(a) and it is designed using the methodology discussed in Section 5.4.1 and Fig. 5.8.

In the following results, to check the performance of the closed-loop compensator, an error is intentionally introduced in the feed-forward compensating current using a step change to reduce it to 50% of its correct value. Subsequently, after 200ms has elapsed, the closed-loop compensator is activated to regulate the capacitor voltage error e_{FH} between the FBSMs and the HBSMs. During the test the hybrid MMC operates in the over-modulation range with m=2.5 (E=96V) and it feeds a load R_L=7.3 Ω connected at the dc-side port. In Fig. 8.7 some internal variables utilised by the CLC-I algorithm implemented in the control platform (e.g. i_d and i_q) are obtained from the data acquisition system of the DSP. The cell capacitor voltages are shown in Fig. 8.7(a). The capacitor voltage error between the FBSMs and the HBSMs is shown in Fig. 8.7(b). Initially e_{FH}≈1.8V but once the feed-forward current is reduced the voltage error increases to e_{FH}≈9.6V. After the close-loop compensator is activated the voltage error is regulated with a settling time of ≈150 ms [see Fig. 8.7(a)]. The feed-forward current i_{ff} and the output of the close-loop

compensator i_{lag} are shown in Fig. 8.7(c). Initially, the magnitude of the feed-forward current is ≈7.6A and the output of the compensator is zero. At t_1, a step reduction of i_{ff} to 3.8A is introduced and, consequently, the error e_{FH} increases. After the outer control loop is activated at t_2, the reactive current reference is increased to i_q^*=8.4A by the close-loop compensator before falling back to the initial value i_q^*≈7.6A once e_{FH} is reduced in steady-state. Notice that the large error introduced artificially into i_{ff} is completely removed by the closed-loop compensator. In addition, the grid currents $\boldsymbol{i}_{dq}$ and their references are shown in Fig. 8.7(d). Finally, the circulating currents $\boldsymbol{i}_{\alpha\beta}^{\Sigma}$ and their references are shown in Fig. 8.7(e) notice that the circulating currents are negligible because the CLC-I strategy is based on manipulating the reactive grid-current.

The variables captured by the digital scope, corresponding to the experimental test depicted in Fig. 8.7 are shown in Fig. 8.8. The capacitor voltages v_{Ca1}^U (yellow, FBSM), v_{Ca2}^U (green, HBSM), v_{Ca1}^L (blue, FBSM), and v_{Ca2}^L (red, HBSM) are shown in Fig. 8.8(a). After the feed-forward current is reduced at t_1, the capacitor voltages of the FBSMs increase, while for the HBSMs the voltages decrease. The maximum voltage difference is 18.3V but, in steady state, after the outer control loop is enabled the voltage difference is 8.1V. The grid current i_a, the arm currents i_a^U and i_a^L, and the dc-port voltage are shown in Fig. 8.8(b). A zoomed view of Fig. 8.8(b) is shown in Fig. 8.8(c) corresponding to the zone where the close-loop compensator is activated. Before t_2, the peak-to-peak grid current is 16.4A which increases to 22.9A once the close-loop compensator is enabled.

The experimental tests are repeated, using identical conditions, for the CLC-II strategy. Again some of the internal variables (e.g $i_q^{\Sigma+}$) are obtained using the data acquisition system available in the DSP-based control platform. The cell capacitor voltages are shown in Fig. 8.9(a), the voltage error between the FBSMs and HBSMs e_{FH} is shown in Fig. 8.9(b). Initially, the capacitor voltage error is e_{FH}≈3.7V which increases to e_{FH}≈11.1V when the feed-forward

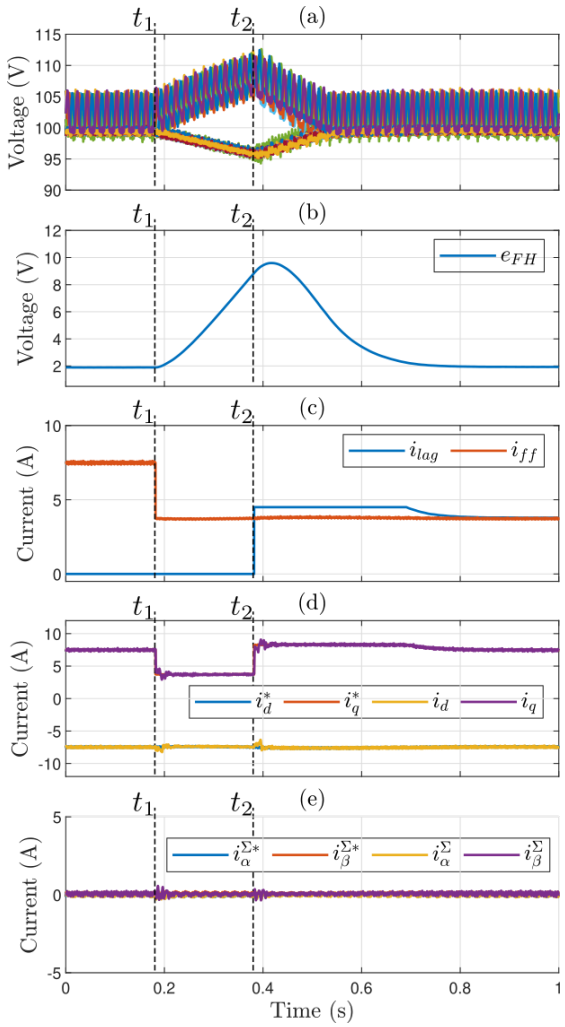


Figure 8.7: *Closed-loop compensator operation using CLC-I:(a) cell capacitor voltages, (b) voltage error e_{FH} between the FBSMs and the HBSMs, (c) feed-forward current and compensating current, (d) grid currents $\boldsymbol{i}_{dq}$ and $\boldsymbol{i}^*_{dq}$, and (e) circulating currents $\boldsymbol{i}^{\Sigma}_{\alpha\beta}$ and $\boldsymbol{i}^{\Sigma*}_{\alpha\beta}$.*

current is reduced (by 50%). However, when the outer control loop [shown in Fig. 5.6(a)] is activated, the voltage error is reduced back to its initial value. The feed-forward current and the current produced at the output of the closed-loop compensator are depicted in Fig. 8.9(c). Initially, the feed-forward current is 5.2A and the compensator is disabled. At t_1, the feed-forward current is reduced by ≈50% and the error e_{FH} increases. After the outer control loop is activated at t_2, the magnitude of $i_q^{\Sigma+}$ reaches 6.1A which is again reduced to $i_q^{\Sigma+}$≈5.2A when the error e_{FH} achieves steady state. Again, the large error introduced artificially into i_{ff} is completely removed by the closed-loop compensator. The grid currents $\boldsymbol{i}_{dq}$ and $\boldsymbol{i}^*_{dq}$ are shown in Fig. 8.9(d), notice

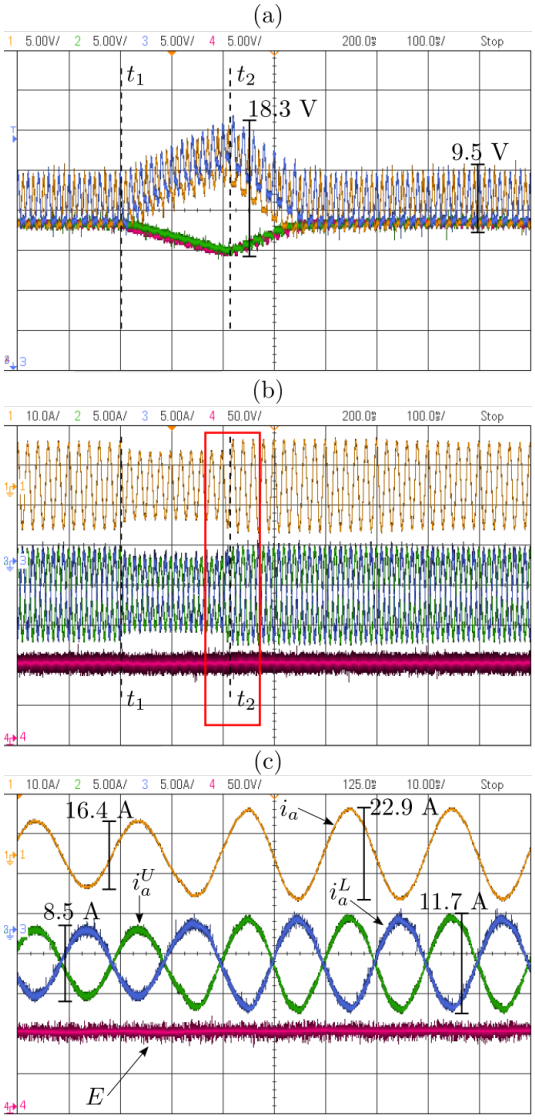


Figure 8.8: *Closed-loop compensator operation using CLC-I: (a) Capacitor voltages of v_{Ca1}^U (yellow), v_{Ca2}^U (green), v_{Ca1}^L (blue), and v_{Ca2}^L (red). (b) grid current i_a (yellow), the arm currents i_a^U (green) and i_a^L (blue), and the dc-port voltage E (red). (c) zoomed view of (b) once the compensator is activated.*

that the converter operates with unity power factor during the whole test, with i_d^*= − 7.9A (which is one of the advantages of the CLC-II strategy). Finally, the circulating currents $\boldsymbol{i}_{\alpha\beta}^{\Sigma}$ and their references are shown in Fig. 8.9(e). The settling time of the capacitor voltage regulation is ≈160ms, as shown in Fig. 8.9(a) and Fig. 8.10(a).

The variables captured by the digital scope, corresponding to the experimental test of Fig. 8.9 are shown in Fig. 8.10. In this case the capacitor voltages v_{Ca1}^U, v_{Ca2}^U, v_{Ca1}^L, and v_{Ca2}^L are shown in Fig. 8.10(a). After the feed-forward current is reduced the capacitor voltage difference increases to 22.7V, but once the

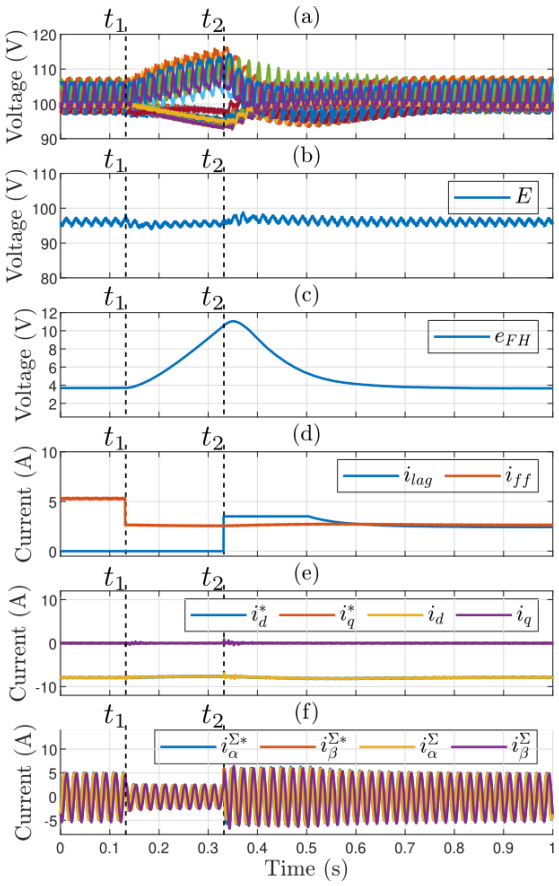


Figure 8.9: *Closed-loop compensator operation using CLC-II:(a) cell capacitor voltages, (b) voltage error e_{FH} between the FBSMs and the HBSMs, (c) feed-forward current and compensating current, (d) grid currents $\boldsymbol{i}_{dq}$ and $\boldsymbol{i}_{dq}^*$, and (e) circulating currents $\boldsymbol{i}_{\alpha\beta}^{\Sigma}$ and $\boldsymbol{i}_{\alpha\beta}^{\Sigma*}$.*

outer control loop is activated the original conditions are restored. Due to the asymmetry in the charging process between the upper and lower arm cells (see Section 5.3.2), the upper arm capacitor voltage balancing is faster ($\Delta t \approx 90$ ms) than that of the lower arm ($\Delta t \approx 160$ ms). The grid current i_a, arm currents i_a^U and i_a^L, dc-port voltage E, and circulating current i_a^{Σ} are shown in Fig. 8.10(b), a zoomed view of Fig. 8.10(b) is shown in Fig. 8.10(c), corresponding to the zone where the outer control loop is activated. When CLC-II is used the grid current is not affected and the converter operates with unity power factor. The peak-to-peak value of the grid current i_a is 15.6A.

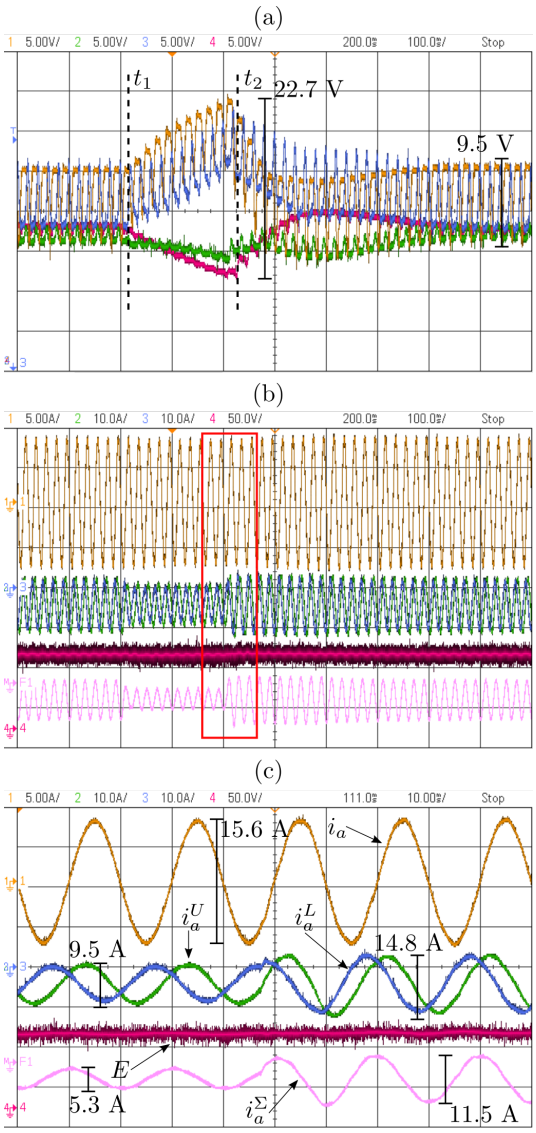


Figure 8.10: *Closed-loop compensator operation using CLC-II: (a) Capacitor voltages of v_{Ca1}^U (yellow), v_{Ca2}^U (green), v_{Ca1}^L (blue), and v_{Ca2}^L (red). (b) grid current i_a (yellow), the arm currents i_a^U (green) and i_a^L (blue), and the dc-port voltage E (red). (c) zoomed view of (b) once the compensator is activated.*

8.8 Dynamic Response for Step Variations in the Load

The control performance is tested considering a load impact at the dc-port side. The hybrid MMC is operating with m=2.5 feeding a resistive load R_L=11 Ω when an impact load occurs and the load resistance is reduced to R_L=7.3 Ω. The performance of both control strategies (CLC-I and CLC-II) is analysed and compared.

Fig. 8.11 shows the converter variables when CLC-I is used. The capacitor

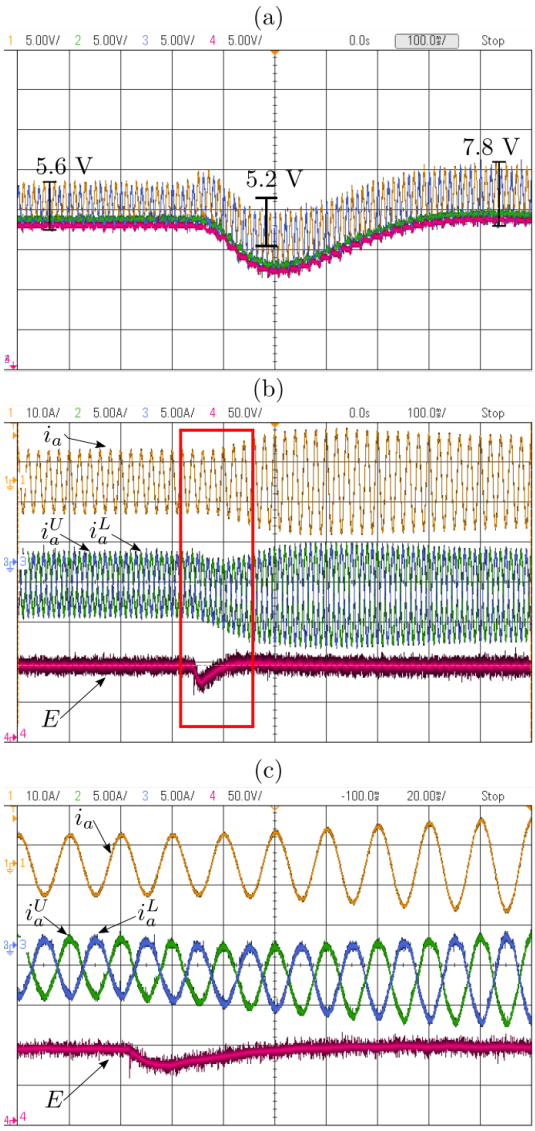


Figure 8.11: *Impact load using CLC-I: (a) Capacitor voltages of v_{Ca1}^U (yellow), v_{Ca2}^U (green), v_{Ca1}^L (blue), and v_{Ca2}^L (red). (b) grid current i_a, arm currents i_a^U and i_a^L and the dc-port voltage E. (c) zoomed view of (b).*

voltages v_{Ca1}^U, v_{Ca2}^U, v_{Ca1}^L, and v_{Ca2}^L are shown in Fig. 8.11(a). Initially, the capacitor voltage oscillations around the mean value are 5.6V and after the load impact they are slightly increased to 7.8V. During the whole test, the FBSMs and HBSMs remain balanced. Notice that, the average voltage of the upper and lower sub-modules have a dip of about 5.2V, due to the load impact, but the control of v_{C0}^{Σ} [see Fig. 5.2] is able to regulate the total capacitor voltage of each arm in about 400ms.

The grid current i_a, arm currents i_a^U and i_a^L and the dc-port voltage E are shown in Fig. 8.11(b) and (c). During the entire test the grid side operates

with a power factor of ≈0.7 because the CLC-I strategy is being used. The peak-to-peak value of the grid current i_a is 7.3A before the load impact and increases to 12.7A after the load impact before settling down to ≈10.9A in steady state. Immediately following the load impact the dc-port voltage has a dip of ≈25V and the control system is able to restore it to the reference value of E=96V in ≈60ms.

The experimental tests are repeated, using identical conditions, for the CLC-II strategy. The experimental results are shown in Fig. 8.12.

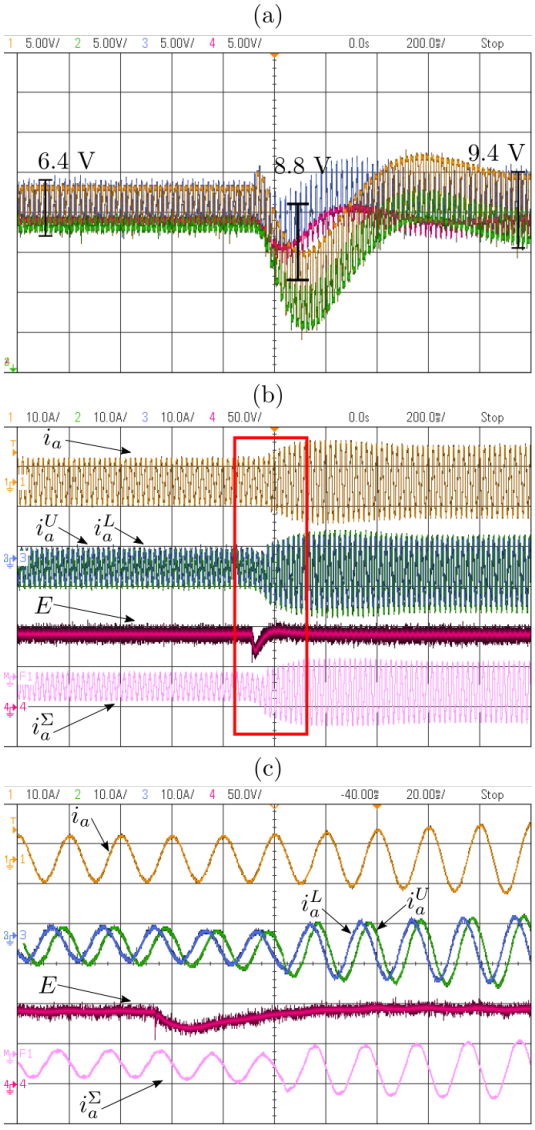


Figure 8.12: *Impact load using CLC-II: (a) Capacitor voltages of v_{Ca1}^U (yellow), v_{Ca2}^U (green), v_{Ca1}^L (blue), and v_{Ca2}^L (red). (b) grid current i_a, arm currents i_a^U and i_a^L and the dc-port voltage E. (c) zoomed view of (b).*

The capacitor voltages v_{Ca1}^U, v_{Ca2}^U, v_{Ca1}^L, and v_{Ca2}^L are shown in Fig. 8.12(a).

Initially, the capacitor voltage oscillations, around the mean value, are 6.4V. After the load impact, the capacitor voltage oscillations are ≈9.4V [see the green waveform in Fig. 8.12(a)]. Due to the load impact, the mean capacitor voltages decrease initially by 8.8V before the global capacitor voltage control system regulates them back to the reference value in 450ms. Fig. 8.12(b) and (c) show the grid current i_a, arm currents i_a^U and i_a^L and the dc-port voltage E. Before the perturbation, the peak value of the circulating current is 3.4A which increases to 7.6A after the load impact.

The main advantage of the CLC-II strategy with respect to CLC-I, is that the converter operates with unity power factor at the grid-side port. However, as discussed in detail in Section 5.3.3 [see also (5.34)-(5.35)], the CLC-II strategy has a smaller voltage margin to regulate the circulating currents used in the hybrid-MMC. Therefore its dynamic response is slower than that obtained with the CLC-I strategy (see Fig. 8.11). This is also confirmed by the response of the control system regulating the dc-link voltage. The dc-port voltage decreases by ≈25V and the control system regulates it back to E=96V in ≈95ms.

8.9 Steady-state Waveforms and capacitor voltage Spectrum for the proposed control strategies

The capacitor voltages v_{Ca1}^U (FBSM), v_{Ca2}^U (HBSM), v_{Ca1}^L (FBSM), and v_{Ca2}^L (HBSM) in steady-state operation are shown for both control strategies (CLC-I and CLC-II). For this test the converter is operating with a modulation index of m=2.5 and a resistive load of 11Ω is connected to the dc-link port. The steady state responses for the CLC-I and CLC-II strategies are shown in Figs. 8.13(a) and (b) respectively.

When CLC-II is used, the charging/discharging behaviour of the sub-modules of the upper and lower arms is no longer symmetric because the arm currents

are asymmetric, according to (5.30)-(5.31), and this is reflected in the waveforms depicted in Figs. 8.13(a) and (b). For both strategies, the capacitor voltage ripple is more significant for the FBSMs with peak to peak values of 6.2V and 8.3V for CLC-I and CLC-II respectively. The ripple in the HBSMs is much less because only the FBSMs contribute to the arm voltage when it is negative during over-modulation (the HBSMs are bypassed and produce zero contribution).

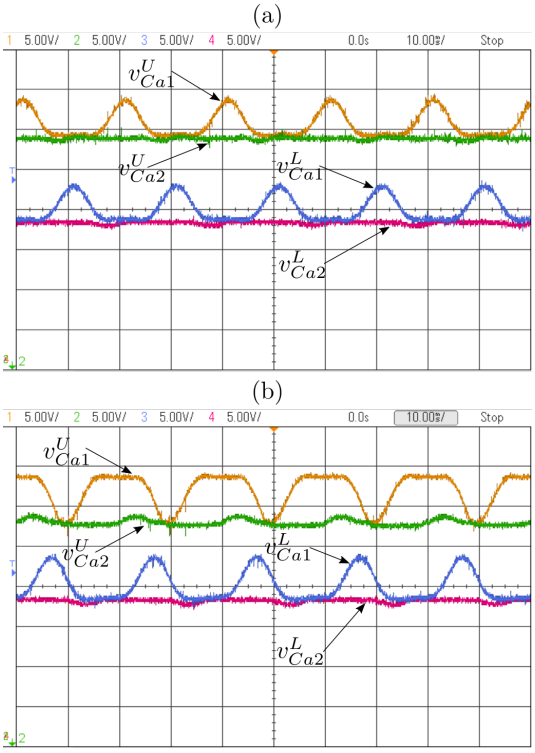


Figure 8.13: *Capacitor voltages of v^U_{Ca1} (yellow), v^U_{Ca2} (green), v^L_{Ca1} (blue), and v^L_{Ca2} (red) for CLC-I (a) and CLC-II (b).*

The spectra, obtained using the Discrete Fourier Transform (DFT), of the capacitor voltages v^U_{Ca1} (FBSM) and v^U_{Ca2} (HBSM) for CLC-I and CLC-II are shown in Fig. 8.14(a) and (b) respectively where the magnitudes are expressed as a percentage of the fundamental. Since the magnitude of the harmonic components are low (<3%), an expanded view of the spectrum is shown in Fig. 8.14. Notice that regardless of the strategy, the harmonic components of the FBSM capacitor voltages are greater than those of the HBSMs. For instance, for CLC-I, the second harmonic of v^U_{Ca1} (FBSM) and v^U_{Ca2} (HBSM) are 0.8% and 0.1% respectively while, for CLC-II, the second harmonic of v^U_{Ca1}

and v_{Ca2}^{U} are 1.2% and 0.2% respectively.

In Fig. 8.14, The DFTs corresponding to the upper arm capacitor voltages are shown. For CLC-I both the upper and the lower arm capacitor voltages have very similar, almost identical, spectra. For CLC-II, there are more asymmetries in the circulating currents of the upper and lower arms [see (5.32)-(5.33)]. Therefore, one of the arms can have a slightly higher or lower second order capacitor voltage harmonic magnitude (less than ≈0.3%).

The CLC-II strategy produces slightly greater harmonic components in the capacitor voltages than CLC-I . This fact is mainly due to the asymmetries in the upper/lower circulating currents, which were discussed in detail in chapter 5, section 3.2.

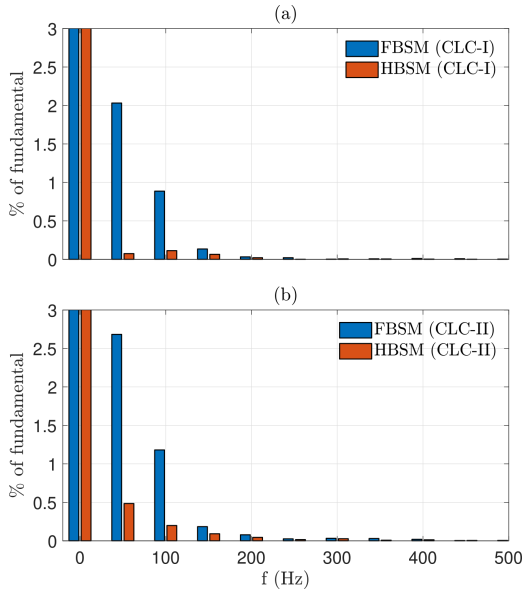


Figure 8.14: *Spectral estimation obtained using the Discrete Fourier Transform (DFT) of v_{Ca1}^{U} (FBSM) and v_{Ca2}^{U} (HBSM) for CLC-I (a) and CLC-II (b).*

Finally, the grid current i_a, the arm currents i_a^U and i_a^L, the dc-port voltage E are shown in steady-state when m=2.5 for CLC-I and CLC-II in Fig. 8.15(a) and (b) respectively. In steady-state, when CLC-I is considered, the magnitude of the reactive current is i_q^*≈5A which is equivalent to a power factor of 0.7. Conversely, when CLC-II is used the converter operates with unity power factor and the magnitude of the circulating current is i_q^{Σ}=3.8A.

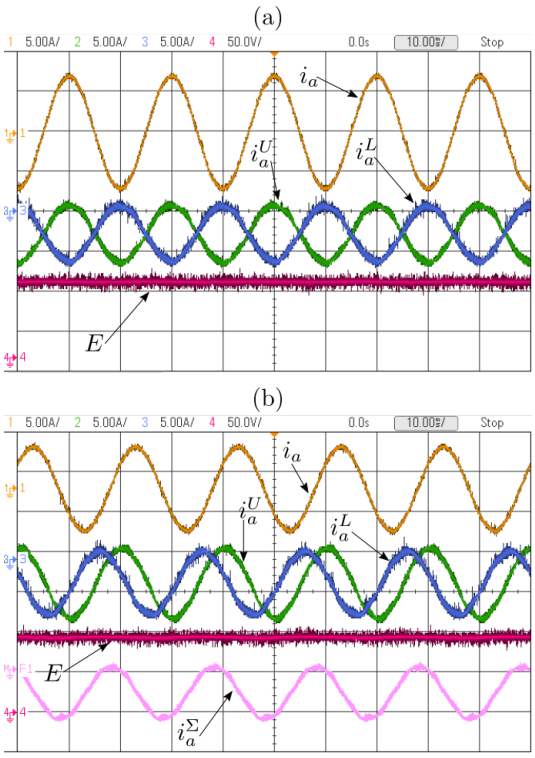


Figure 8.15: *Grid current i_a, the arm currents i_a^U and i_a^L, the dc-port voltage E are shown in steady-state when m=2.5 for: (a) CLC-I and (b) CLC-II.*

8.10 Variable dc-link operation for a BTB MMC-based converter

In this test, a back-to-back MMC is used to drive an induction machine. The grid-side converter is an hybrid MMC while the machine-side is a HBSM-based MMC. The operation with constant and variable dc-link is tested. In this test, the variable dc-link is calculated as 5.49. A ramp reference speed $\omega_2^* = 0 \rightarrow 147$ $rads^{-1}$ is applied to the machine control.

The arm currents i_{2a}^U (green) and i_{2a}^L (yellow), the circulating current i_{2a}^Σ (pink), the cell capacitor voltage v_{C2a1}^U (blue), and the machine current i_{2a} (red) are shown in Fig. 8.16 and Fig. 8.17 for a fixed dc-link voltage $E^* = 300$ V and for a variable dc-link respectively. For the variable dc-link voltage operation, E^* is calculated as (5.49), in addition, the minimum dc-port voltage modulated by the hybrid MMC is limited to $E_{\min}$=130 V. Notice that the voltage oscillation of the sub-module v_{C2a1}^U are higher for a fixed dc-port voltage operation ($\Delta Vc \approx 15.5$ V) than for a variable dc-port voltage operation ($\Delta Vc \approx 8.7$ V).

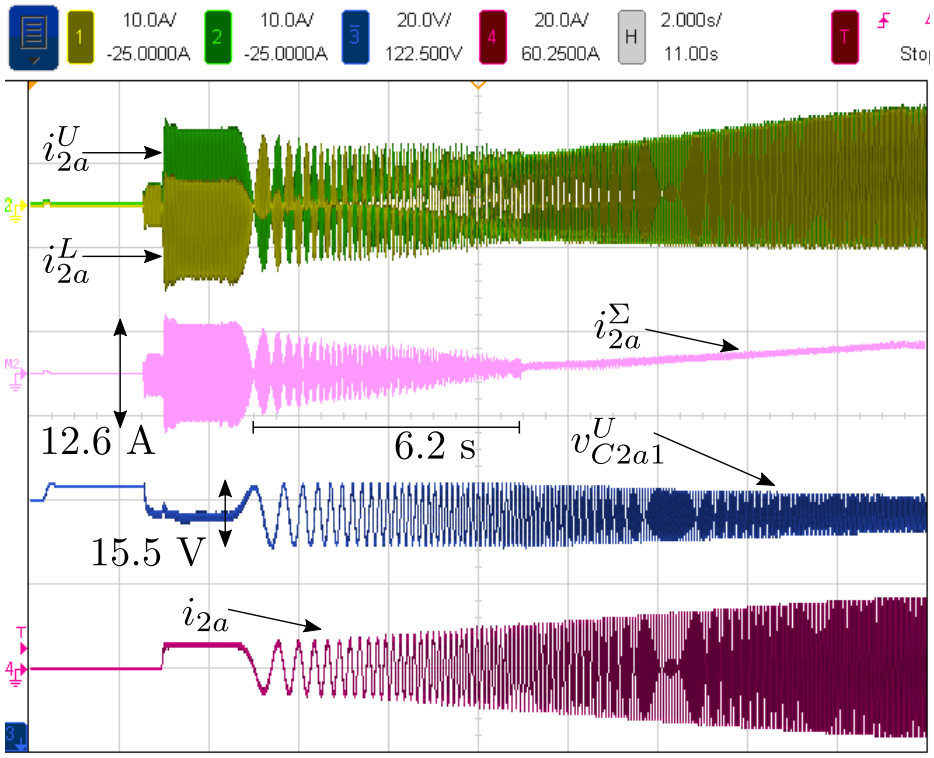


Figure 8.16: *Machine-side operation for constant dc-link operation. Upper arm current i_{2a}^{U} (green), lower arm current i_{2a}^{U} (yellow), circulating current i_{2a}^{Σ} (pink), sub-module capacitor voltage v_{C2a1}^{U} (blue), and machine phase current i_{2a} (red).*

In addition, the low frequency mode operation is applied for a longer duration when the dc-port voltage is fixed ($\Delta t \approx 6.2$ s) in comparison with a variable E operation ($\Delta t \approx 2.5$ s). In this case, when E is fixed, the LFM is applied in the machine speed range $0 \leq \omega_m \leq 282$ RPM, while for a variable E the LFM is only applied in $0 \leq \omega_m \leq 604$ RPM.

Figures 8.18 to 8.20 show a zoomed view of Fig. 8.16 for different operational mode, in all these figures the upper arm current i_{2a}^{U} (green), lower arm current i_{2a}^{U} (yellow), circulating current i_{2a}^{Σ} (pink), sub-module capacitor voltage v_{C2a1}^{U} (blue), and machine phase current i_{2a} (red) are shown for a constant dc-link voltage. Figure 8.18 shows the drive-side MMC variables during the stator magnetization ($i_{q2}=0$). Then, 8.19 and 8.20 show the drive-side MMC variables for low-frequency mode and high-frequency mode.

Figures 8.21 to 8.23 show a zoomed view of Fig. 8.17 for different operational mode, in all these figures the upper arm current i_{2a}^{U} (green), lower arm current i_{2a}^{U} (yellow), circulating current i_{2a}^{Σ} (pink), sub-module capacitor voltage v_{C2a1}^{U}

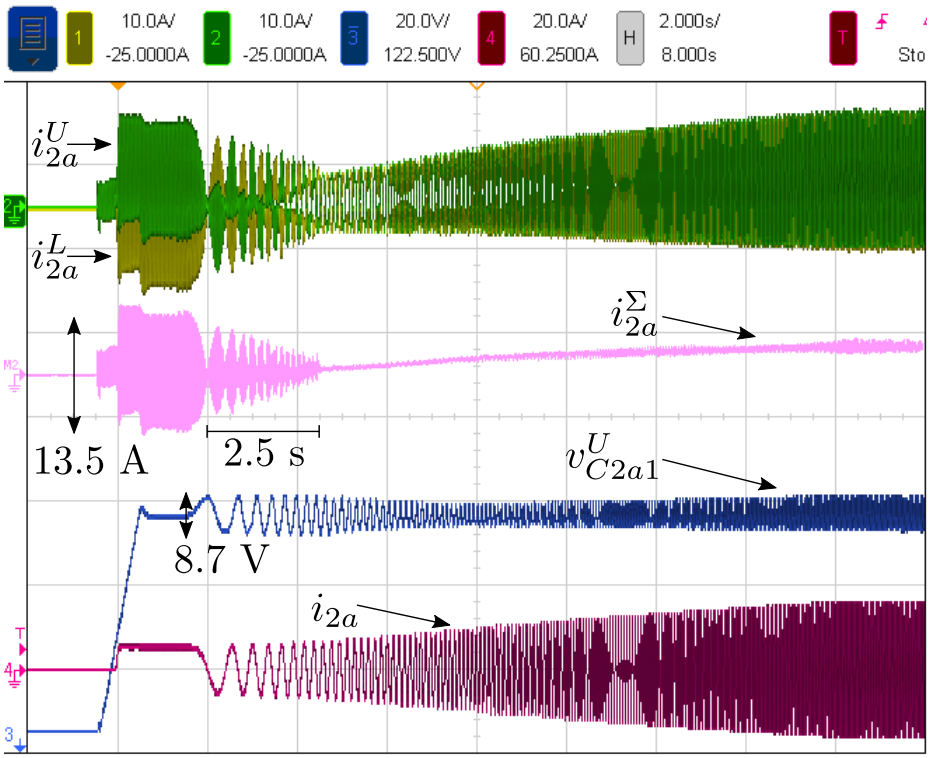


Figure 8.17: *Machine-side operation for variable dc-link operation. Upper arm current i_{2a}^{U} (green), lower arm current i_{2a}^{U} (yellow), circulating current i_{2a}^{Σ} (pink), sub-module capacitor voltage v_{C2a1}^{U} (blue), and machine phase current i_{2a} (red).*

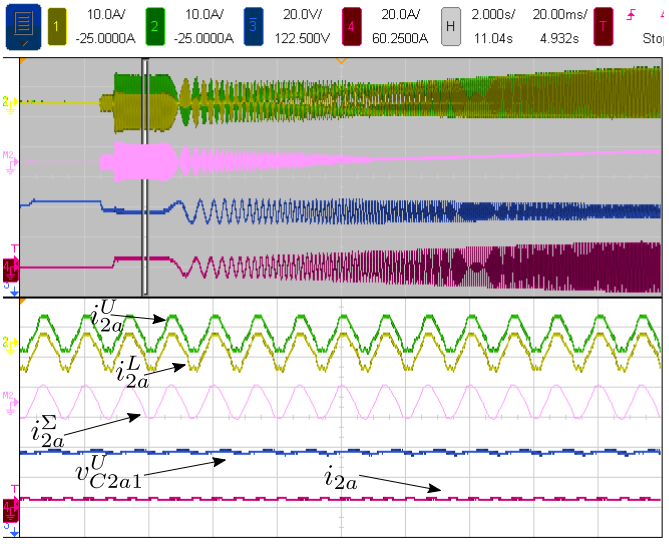


Figure 8.18: *Zoomed view during stator magnetization for constant dc-link operation. Upper arm current i_{2a}^{U} (green), lower arm current i_{2a}^{U} (yellow), circulating current i_{2a}^{Σ} (pink), sub-module capacitor voltage v_{C2a1}^{U} (blue), and machine phase current i_{2a} (red).*

(blue), and machine phase current i_{2a} (red) are shown for a variable dc-link voltage. Figure 8.21 shows the drive-side MMC variables during the stator magnetization (i_{q2}=0). Then, 8.22 and 8.23 show the drive-side MMC variables

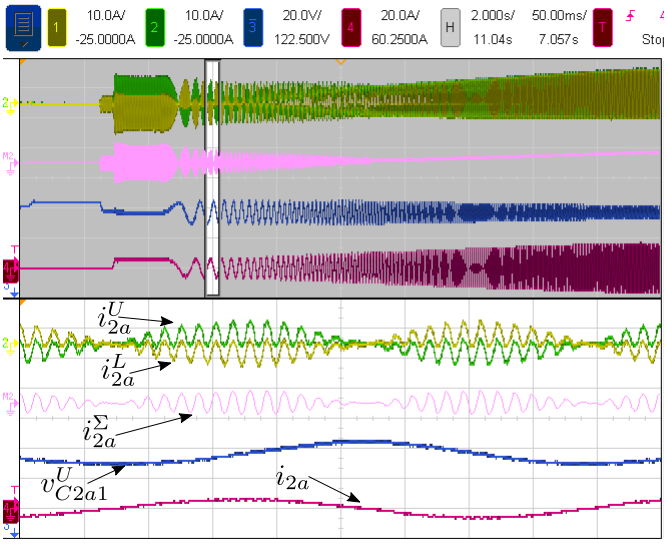


Figure 8.19: *Zoomed view during low-frequency operation for constant dc-link voltage. Upper arm current i^U_{2a} (green), lower arm current i^U_{2a} (yellow), circulating current i^Σ_{2a} (pink), sub-module capacitor voltage v^U_{C2a1} (blue), and machine phase current i_{2a} (red).*

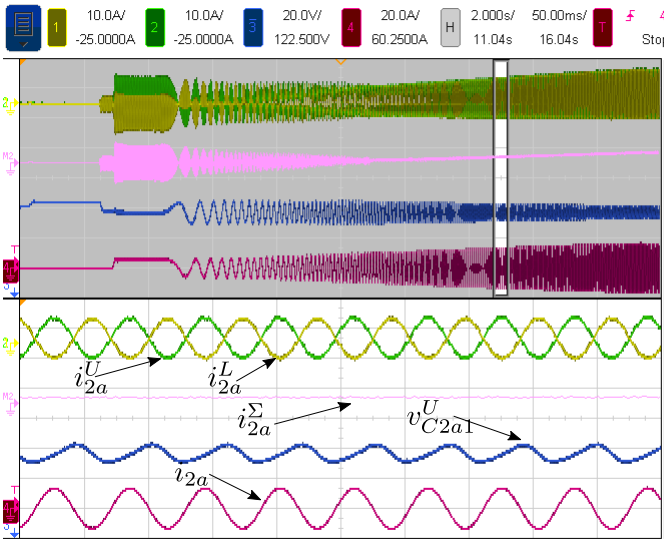


Figure 8.20: *Zoomed view during high-frequency operation for constant dc-link voltage. Upper arm current i^U_{2a} (green), lower arm current i^U_{2a} (yellow), circulating current i^Σ_{2a} (pink), sub-module capacitor voltage v^U_{C2a1} (blue), and machine phase current i_{2a} (red).*

for low-frequency mode and high-frequency mode.

Figure 8.24 depicts some relevant DSP variables of the speed ramp test with constant dc-port voltage E discussed previously of Fig. 8.16. The machine speed is shown in Fig. 8.24(a). In this case, the DC-link voltage remains constant and it is equal to E≈300 V as shown in Fig. 8.24(b). The capacitor voltages of each HBSM are shown in Fig. 8.24(c), in this case, the maximum

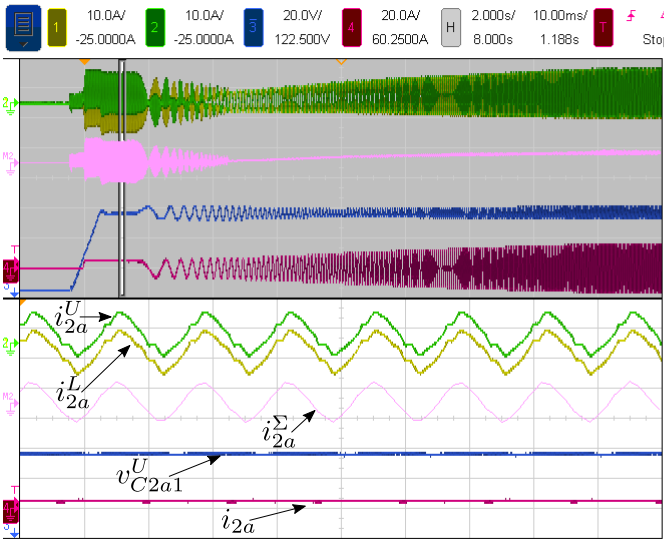


Figure 8.21: *Zoomed view during stator magnetization for variable dc-link operation. Upper arm current i^{U}_{2a} (green), lower arm current i^{U}_{2a} (yellow), circulating current i^{Σ}_{2a} (pink), sub-module capacitor voltage v^{U}_{C2a1} (blue), and machine phase current i_{2a} (red).*

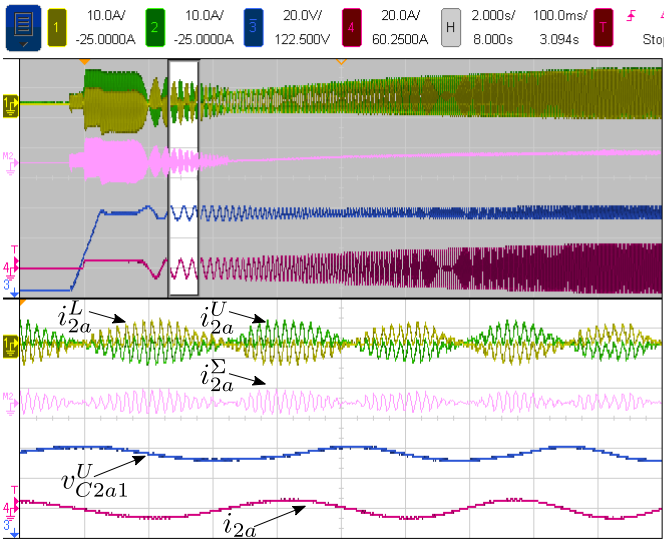


Figure 8.22: *Zoomed view during low-frequency operation for variable dc-link voltage. Upper arm current i^{U}_{2a} (green), lower arm current i^{U}_{2a} (yellow), circulating current i^{Σ}_{2a} (pink), sub-module capacitor voltage v^{U}_{C2a1} (blue), and machine phase current i_{2a} (red).*

peak-to-peak voltage oscillation is 16.7 V. The machine current i_{2abc} and the circulating currents $i^{\Sigma}_{2\alpha\beta}$ are shown in Fig. 8.24(d) and (e) respectively. Finally, the imposed common-mode voltage v_{20} is shown in Fig. 8.24(f), in this case, the maximum amplitude is reached during the machine start-up and it is equal to 120 V.

Regarding the variable dc-link voltage test, some internal DSP variables are

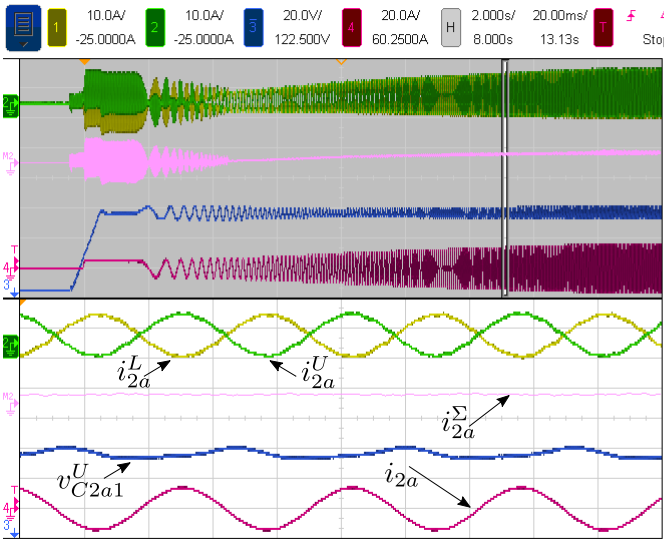


Figure 8.23: *Zoomed view during high-frequency operation for variable dc-link voltage. Upper arm current i^U_{2a} (green), lower arm current i^U_{2a} (yellow), circulating current i^Σ_{2a} (pink), sub-module capacitor voltage v^U_{C2a1} (blue), and machine phase current i_{2a} (red).*

shown in Fig. 8.25. The same speed profile reference than the previous test is applied as shown in Fig. 8.25(a). The variable dc-link voltage produced by the hybrid MMC is shown in Fig. 8.25(b), in this case E varies from 130 V to 300 V as a function of (5.49). The cell capacitor voltages are plotted in Fig. 8.25(c), in this case the maximum peak-to-peak voltages oscillations is 10.8 V. The sub-module voltage oscillations, for a variable E operation, are 35.3% lower than that of when the back-to-back converter operates with a constant E. In addition, the machine currents i_{2abc} and the circulating currents $\boldsymbol{i}^\Sigma_{\alpha\beta}$ are shown in Fig. 8.25(d) and (e) respectively, since the same speed profile is applied, the machine currents are the same than that of the previous test. However, as expected, the low-frequency mode is applied for a lower duration than that of the previous case. Finally, the peak value of the common-mode voltage is 48.2 V, i.e., the common-mode voltage v_{20} is reduced ≈40% with respect to the constant dc-link voltage case.

The operation of the hybrid MMC to produce a variable dc-link voltage (5.49) is depicted below. The local balance between the HBSMs and FBSMs is done by controlling the reactive current i_{1q} or the circulating current $i^{\Sigma+}_{1q}$.

The grid-side converter variables when a reactive current component is used

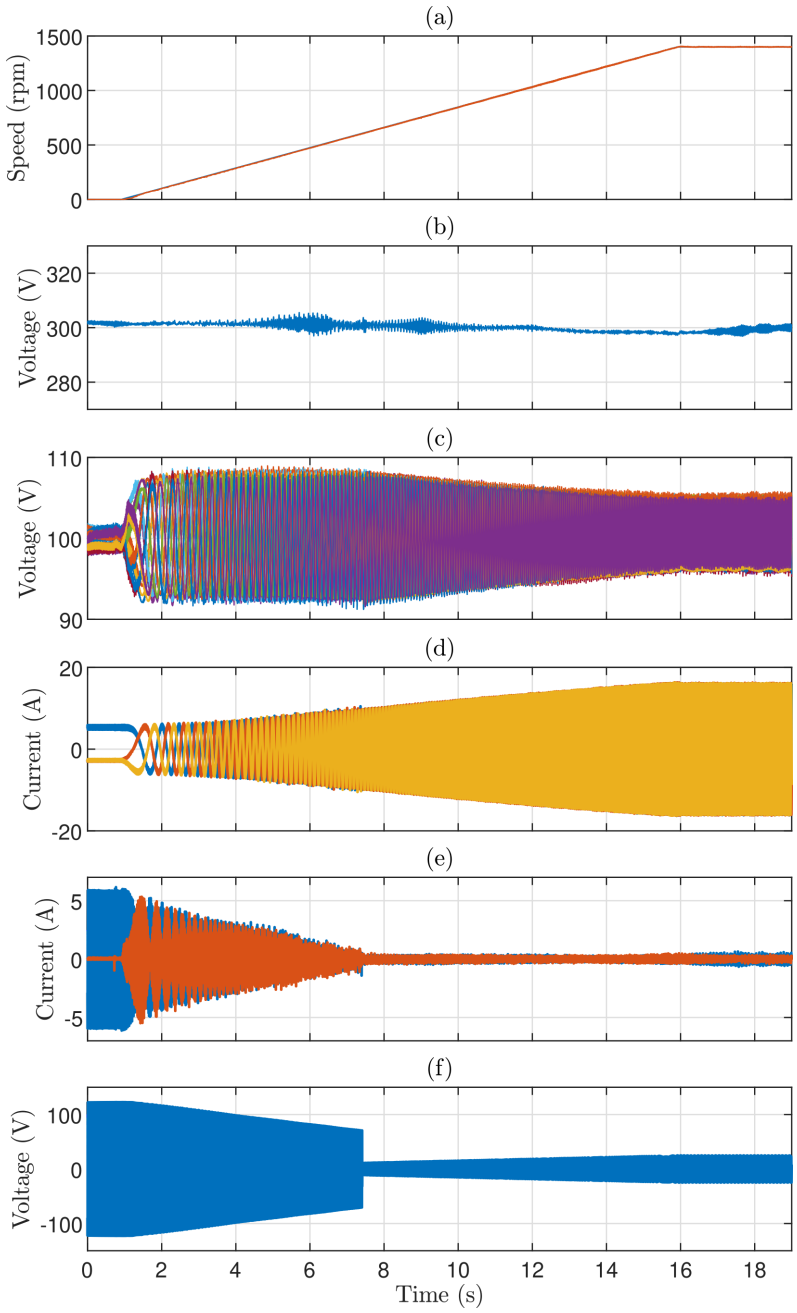


Figure 8.24: *Machine-side operation with constant dc-link voltage E. (a) Machine speed, (b) dc-link voltage E, (c) sub-module capacitor voltages, (d) machine currents i_{2abc}, (e) circulating currents $\boldsymbol{i}_{2\alpha\beta}^{\Sigma}$, and (f) common-mode voltage applied to the machine.*

to accomplish the local balance between HBSMs and FBSMs are shown in Fig. 8.26. The cell capacitor voltages are shown in Fig. 8.26(a), in this case the peak-to-peak capacitor voltage oscillations are lower than 14.6 V. The dc-port voltage is shown in Fig. 8.26(b). Next, the grid current is shown in Fig. 8.26(c), during this test the power factor is reduced down to 0.65. In addition, the circulating currents $\boldsymbol{i}_{\alpha\beta}^{\Sigma}$ are shown in Fig. 8.26(e), during the

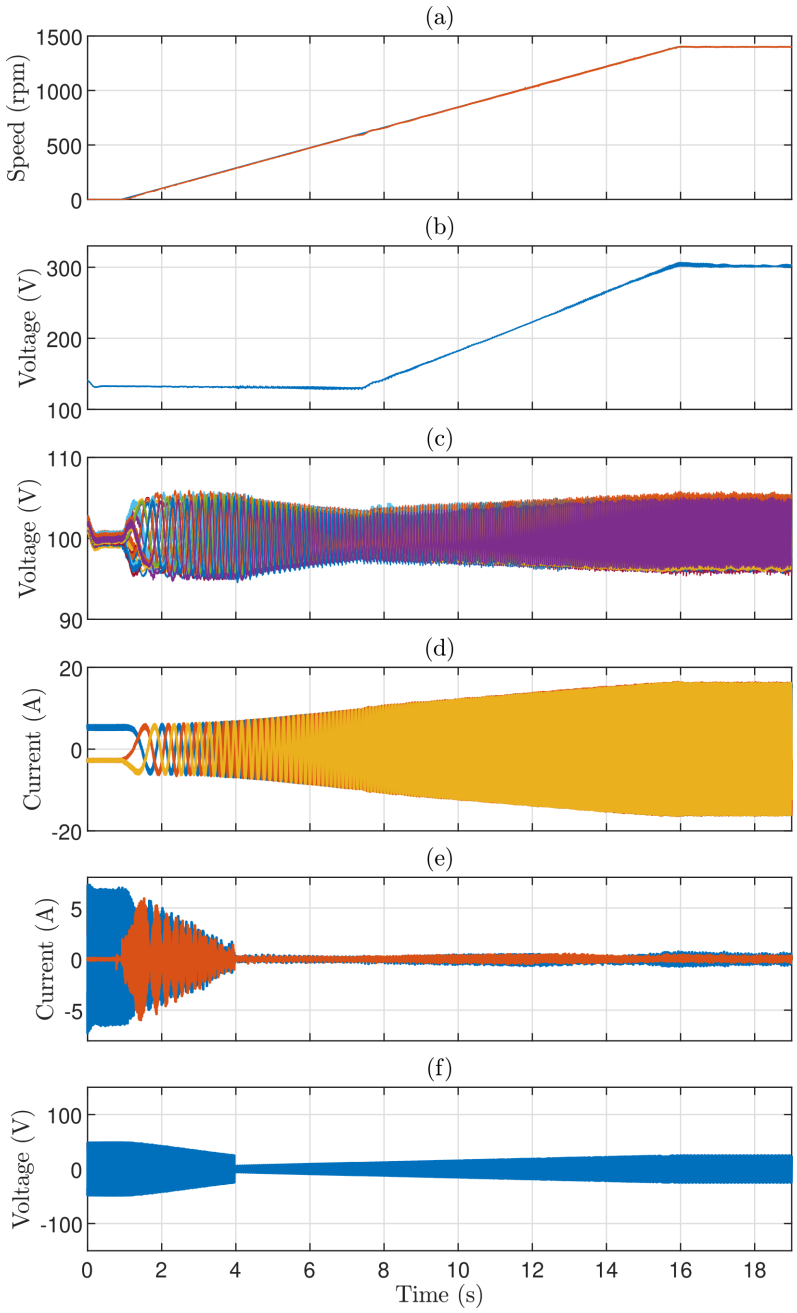


Figure 8.25: *Machine-side operation with variable dc-link voltage E. (a) Machine speed, (b) dc-link voltage E, (c) sub-module capacitor voltages, (d) machine currents i_{2abc}, (e) circulating currents $\boldsymbol{i}_{2\alpha\beta}^{\Sigma}$, and (f) common-mode voltage applied to the machine.*

whole test the circulating current has a peak value of 1.4 A that is negligible compared to the output grid currents. The magnitude of the injected reactive current is shown in Fig. 8.26(f).

Finally, the operation of the hybrid MMC using circulating current is shown in Fig. 8.27. In this case, the cell capacitor voltages are shown in Fig. 8.27(a), the peak-to-peak capacitor voltage oscillations are 15.5 V. The dc-link voltage

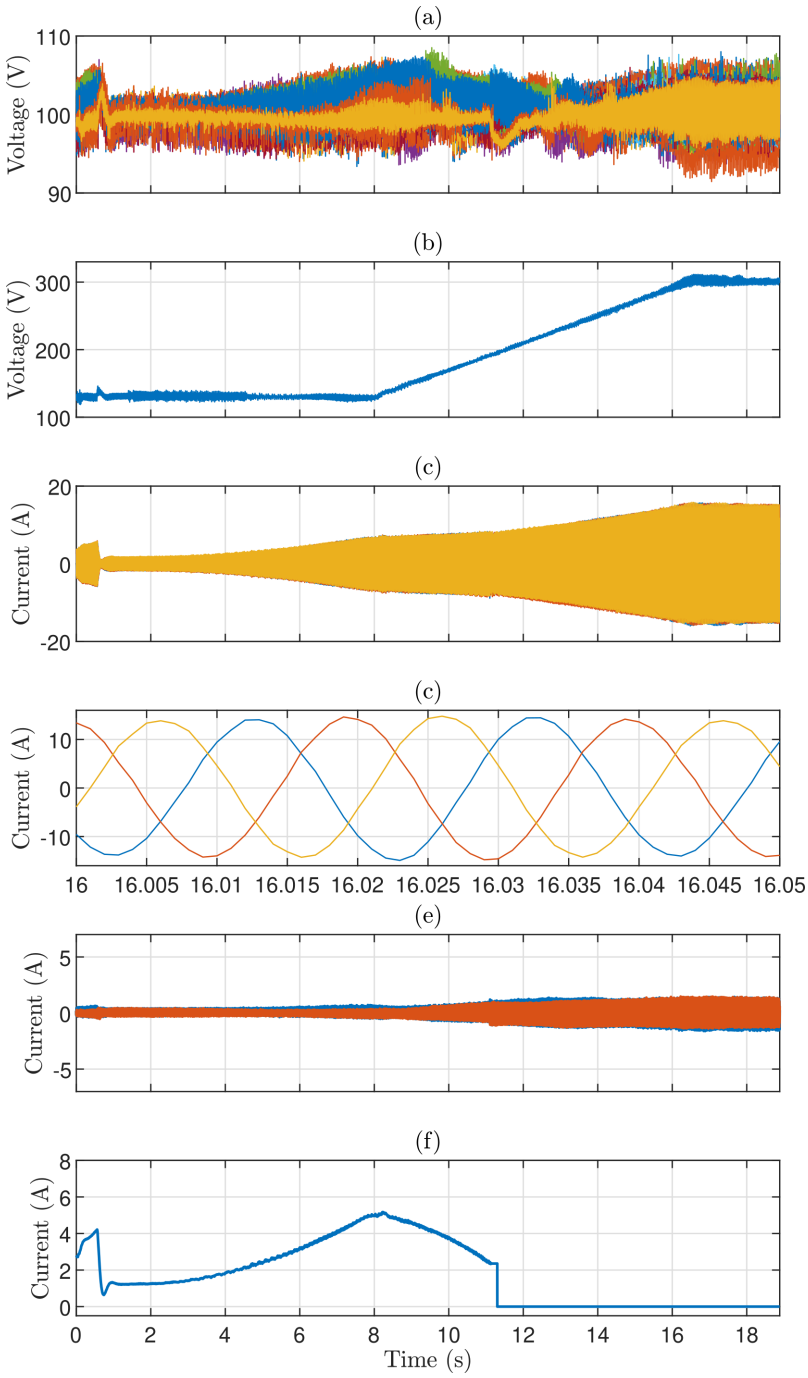


Figure 8.26: *Hybrid MMC operation with reactive current. (a) cell capacitor voltages, (b) dc-link voltage E, (c) grid currents i_{1abc}, (d) zoomed view of the machine currents, (e) circulating currents $\boldsymbol{i}_{1\alpha\beta}^{\Sigma}$, and (f) magnitude of the reactive current i_{1q}.*

is shown in Fig. 8.27(b). The grid current is shown in Fig. 8.27(c), and a zoomed view of the grid current between t=10 s and t=10.1 s is plotted in Fig. 8.27(d) while the converter is injecting a circulating current component $i_{1q}^{\Sigma+}$, the grid current has a low harmonic distortion. The circulating currents $\boldsymbol{i}_{1\alpha\beta}^{\Sigma}$ and the magnitude of the current reference $i_{1q}^{\Sigma+}$ are shown in Fig. 8.27(e)

and (f) respectively. In this case, the front-end converter operates with unity power factor.

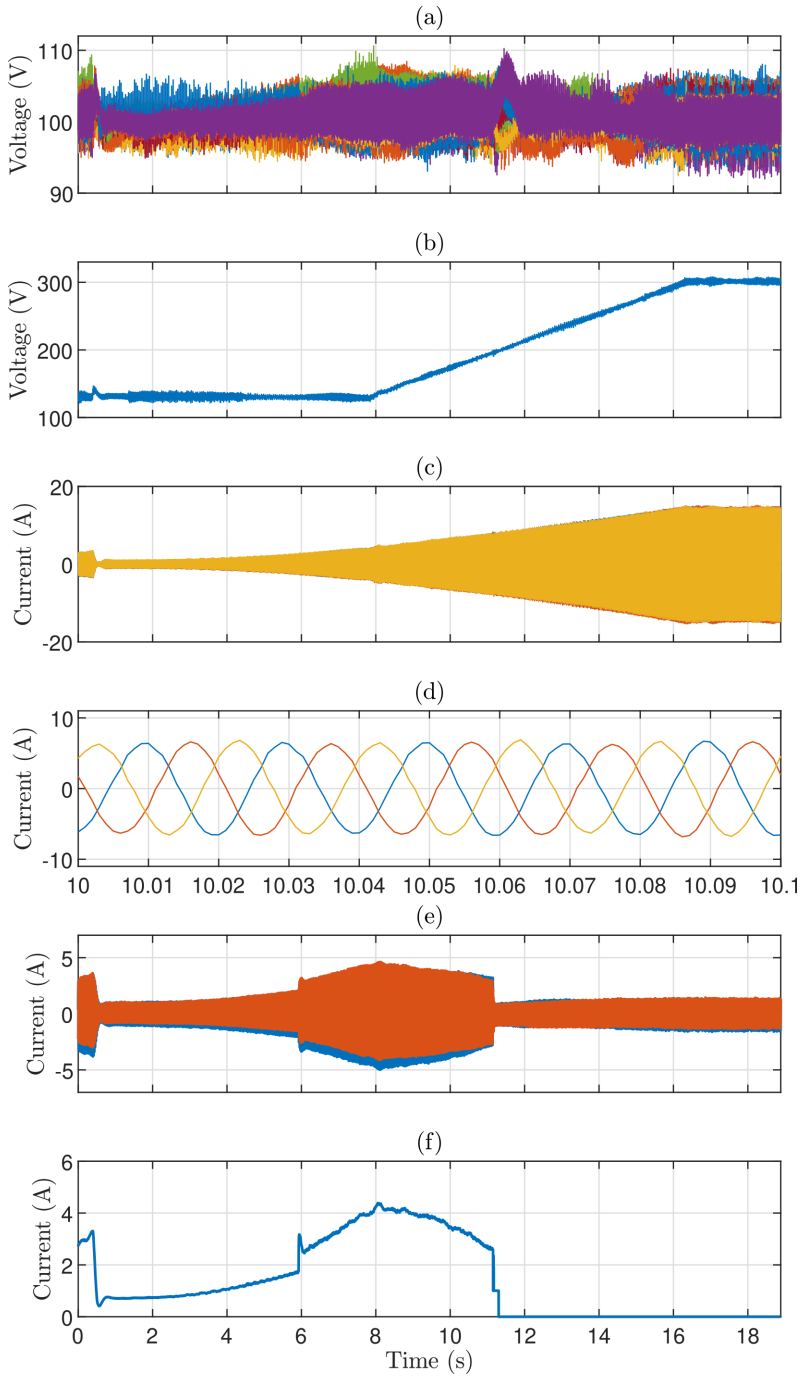


Figure 8.27: *Hybrid MMC operation with circulating current. (a) cell capacitor voltages, (b) dc-link voltage E, (c) grid currents i_{1abc}, (d) zoomed view of the machine currents, (e) circulating currents $\boldsymbol{i}^{\Sigma}_{1\alpha\beta}$, and (f) magnitude of the circulating current $i^{\Sigma+}_{1q}$.*

8.11 Summary

This chapter shows the experimental results to validate the proposed control strategies for the hybrid MMC and the back-to-back drive application.

First, the unbalance problem is shown when the hybrid MMC operates in over-modulation and the control does not inject any compensating currents (neither reactive current nor circulating current). Although the hybrid MMC can still operate while the FBSMs and HBSMs are unbalanced, if the imbalance is not corrected, the cell capacitor voltage of one cell type will keep increasing until the over-voltage protections trigger. The performance of both proposed strategies CLC-I and CLC-II, is shown during over-modulation. Both strategies can ensure the local balance of the hybrid MMC converter. However, CLC-I operates with a low power factor while CLC-II can balance the FBSMs and HBSMs at unity power factor. The proposed strategies CLC-I and CLC-II are also compared with similar approaches found in the literature. The main advantage over those works is that CLC-I and CLC-II calculate the minimum compensating current to ensure the local balance. Previous works only give lower bounds to ensure the arm currents' change of sign. However, these works do not give closed-expressions nor simple procedures to calculate the required compensating currents. Then, the operation of the closed-loop control is tested when the control miscalculates the feed-forward current . In this case, CLC-I is faster than CLC-II in balancing the cell capacitor voltages of the HBSMs and FBSMs. The transient response under step-load variation is also considered, and the proposed strategies can balance the FBSMs and HBSMs. Finally, relevant steady-state waveforms are depicted; one important difference between CLC-I and CLC-II is that the latter produces higher harmonics than the former. In both cases, the FBSMs have a higher first and second harmonic compared to the one of the HBSMs.

Second, the operation of the back-to-back MMC converter for drive applications is tested. It is shown that the operation with a variable dc-link voltage

requires injecting a reduced common-mode voltage with respect to the case with constant dc-link voltage. In addition, the duration of the low-frequency mode is reduced, and the capacitor voltage oscillations are also reduced when the dc-link voltage is variable. The next chapter presents the main conclusions of this research effort.

Chapter 9

Conclusions

Compared to a half-bridge based MMC, the hybrid MMC allows operation with a suppressed dc-side voltage, which can have significant advantages for many applications, such as HVDC converters and high power drive applications. However, the operation when the dc voltage is significantly reduced and is below the peak of the ac phase voltage (modulation index >2) is not possible without additional attention to the problem of energy balance between the full-bridge (FBSM) and half-bridge (HBSM) sub-modules. Under these conditions, the arm currents become unipolar, and it is not possible to achieve energy balance with conventional control approaches. Nevertheless, the ability to operate with a significantly depressed dc side voltage is essential to maximise the benefits of the hybrid MMC, and it is therefore important to develop control approaches that can achieve this.

This thesis has proposed two strategies to guarantee the capacitor voltages balance between the FBSMs and HBSMs in a hybrid MMC operating with a modulation index >2. The first strategy, CLC-I, uses an additional reactive grid-current, while the second strategy, CLC-II, uses an additional component in the circulating current that does not affect the overall arm energy balance. Both strategies use feed-forward terms to improve the transient response. A significant advantage of the proposed strategies is that an explicit methodology to calculate the feed-forward optimal currents is presented. In particular,

explicit expressions for the reactive current (CLC-I) and circulating current (CLC-II) are derived. This allows the additional current required in either method to be minimised at all operating conditions, which has not been possible with previous methods. In addition, a closed-loop control regulates the measured capacitor voltage error between the FBSMs and the HBSMs to compensate for parameter variations between the actual system and those used in the feed-forward current calculations. Furthermore, a decoupled model of the hybrid MMC has been applied to derive a simple control of the floating capacitor voltages.

The proposed controllers have been validated under steady-state and transient conditions using simulation results and experimental tests on a prototype converter. The dynamic and steady-state performance has been shown to be very good for all the experimental conditions studied. It has been concluded that the control approach based on reactive grid-current has a better dynamic response since a relatively high voltage margin is available to impose the required grid current. On the other hand, the compensating scheme based on internal circulating currents allows operation with unity power factor at the grid side.

In addition, this thesis presents a hybrid back-to-back MMC for drive applications. The grid-side converter is a hybrid MMC composed of HBSMs and FBSMs, while the machine-side converter is an HBSM-based MMC. It is possible to control the dc-port voltage to reduced the injected common-mode voltage to the machine stator and to reduce the arm energy pulsations of the drive-side MMC during low mechanical speed. Consequently, the stress over the machine insulation is reduced. An optimal value for the dc-link voltage has been derived, and then the operation with variable dc-link voltage has been validated through simulations and experimental results. Previous works have proposed different topologies to produce a variable dc-link voltage for drive applications. For instance, an FBSM-based modular multilevel converter in back-to-back configuration was proposed to drive an induction machine, but the switches count is doubled with respect to the HBSM-based MMC case.

Some authors have proposed to vary the dc-link voltage discretely. For instance, the modulate the dc-link voltage with a director switch in the dc-port or use a tapped transformer to produce different dc-link voltage levels. However, the former approach introduced harmonics to the converter, and the latter solution requires a special multi-winding transformer which is bulky.

9.1 Main Contributions

The achievements and contributions of the presented work are following:

1. The review of the multilevel topologies is discussed. The main models, sub-modules, control strategies are presented. Then, the advantages and disadvantages of the hybrid MMC are highlighted. In particular, the hybrid MMC can operate with a reduced dc-link voltage. As pointed out by several authors, the hybrid MMC can be useful in HVDC applications. For instance, the dc-link voltage can be reduced during bad weather conditions to reduce the risk of short-circuits. In addition, a second application of the hybrid MMC is presented, in particular, in a back-to-back MMC-based drive application. If the grid-side converter is implemented using a hybrid MMC, it is possible to regulate the dc-link voltage to reduce the arm energy oscillations during low mechanical speed in the drive-side MMC.

2. A decoupled model of the hybrid MMC is explained. The main advantage of working in the $\Sigma\Delta\alpha\beta 0$ reference frame is the simplification of the control design. By using the decoupled model, it is possible to regulate the sub-module cell capacitor using the different components of the positive and negative components of the circulating currents. Thus, the use of each component does not affect different errors terms. In addition, a procedure to size the hybrid MMC converter along with the HBSM-based MMC is presented. In particular, analytical expressions for the

main converter parameters are derived.

3. A nested closed-loop for the hybrid MMC is proposed. First, the general structure of the arm energy balance is presented. An outer voltage control loop composed of 6 PI controllers regulates the different components of the circulating current to ensure the energy balance among arms. In addition, the inner current control structure is explained. The circulating currents are controlled using resonant controllers, while the grid currents are regulated using PI controllers. This control does not introduce any extra harmonic to the grid-side.

4. Two control strategies to ensure the local balance of a hybrid MMC operating in over-modulation are presented. These strategies are named CLC-I and CLC-II. The former ensures the local balance by increasing the magnitude of the reactive current, while the latter increases the circulating current's magnitude.

5. The control of the back-to-back MMC is presented. In this case, the grid-side converter is a hybrid MMC, while the machine-side converter is an HBSM-based MMC. The machine operational point is considered to calculate the required dc-link voltage to reduce the energy arm oscillations of the machine-side MMC.

6. The proposed controllers are validated through simulation results. An MW application is considered to validate the hybrid MMC control. The proposed strategies CLC-I and CLC-II have a good steady-state and transient response. CLC-I has a better transient response to balance the FBSMs and the HBSMs than CLC-II. However, CLC-II can operate with unity power factor, while CLC-I imposes a poor PF when the hybrid MMC operates in over-modulation. Regarding the back-to-back application, it is shown that the arm energy pulsations are less when a variable dc-link voltage is used.

7. The proposed controllers are validated using the experimental rig in chapter 8. A hybrid MMC rig composed of 18 cells is implemented to validate the proposed controllers CLC-I and CLC-II. In this case, each arm is composed of 1 FBSM and 2 HBSMs. Finally, the operation of a back-to-back MMC for drive application is presented. In this case, a back-to-back system composed of 36 cells is considered.

9.2 Limitations and Suggestions for Further Improvements

The limitations and suggestions for further improvement are listed below:

1. In this thesis only quadratic torque profile loads have been considered for the machine-side MMC. According to several authors in the literature review, the MMC is best suited for quadratic torque load profiles [24, 36, 161, 162]. For instance, the MMC can be employed to drive industrial fans or centrifugal compressors [133]. Although different load profiles can be driven by an MMC, the arm current will be higher than its rated value at nominal speed. Therefore, different modular converters should be considered to avoid over-sizing the sub-module switches. In particular, the MMC is not suitable for constant torque profiles or quadratic torque profiles with an initial value at zero speed. For instance, the quadratic plus constant profile is found in hydro pumped storage centrals [164]. In this case, the M^3C is best suited to drive loads with a high initial torque at low mechanical speed [161]. Finally, the M^3C is more suitable for mills, kilns, and extruders [133].

2. Although, the proposed control strategy is able to ensure an stable operation of the hybrid MMC. The derivation of each control plant is a time-consuming process. In addition, considering that the processing power of micro-controllers and DSPs has increased considerably in the

last decade, the predictive control seems as an interesting approach to control an hybrid MMC. The main advantage of predictive control in power electronics is its fast transient response and intuitive implementation.

3. The addition of the FBSMs to the HBSMs increases the output voltage capability of the hybrid MMC. However, other hybrid MMC topologies has been proposed to enhanced the HBSM-based MMC. For instance, the cascaded hybrid MMC is a topology that has a stack of FBSMs in series to each output AC port. It seems interesting to study the possible applications of the hybrid MMC.

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Appendix A

MMC arm power in the $\Sigma\Delta\alpha\beta 0$ coordinates

The proposed control in this thesis is based in the $\Sigma\Delta\alpha\beta 0$ transformation. The main advantage of working with this linear transformation is that the MMC can be modelled as decoupled circuits. Therefore, it is possible to regulate independently the inner and outer converter variables. The voltages and currents of the converters are expressed in a matrix form in $\Re^{2\times 3}$. For instance, the arm voltages of an MMC are represented by the matrix V_{abc}^{UL}:

$$V_{abc}^{UL} = \begin{pmatrix} v_a^U & v_b^U & v_c^U \\ v_a^L & v_b^L & v_c^L \end{pmatrix} \tag{A.1}$$

To express the arm voltages of the MMC in the $\Sigma\Delta\alpha\beta 0$ reference, the matrix V_{abc}^{UL} is pre- and post- multiplied by the matrices $T_{\Sigma\Delta}$ and $T_{\alpha\beta}$. The transformation matrices $T_{\Sigma\Delta}$ and $T_{\alpha\beta}$ are defined below:

$$T_{\Sigma\Delta} = \frac{1}{2}\begin{pmatrix} 1 & 1 \\ 2 & -2 \end{pmatrix} \qquad T_{\alpha\beta 0} = \frac{1}{3}\begin{pmatrix} 2 & 0 & 1 \\ -1 & \sqrt{3} & 1 \\ -1 & -\sqrt{3} & 1 \end{pmatrix} \tag{A.2}$$

The voltage matrix V_{abc}^{UL} in $\Sigma\Delta\alpha\beta 0$ coordinates is defined as:

$$V_{\alpha\beta 0}^{\Sigma\Delta} = \frac{1}{2}\begin{pmatrix} 1 & 1 \\ 2 & -2 \end{pmatrix}\begin{pmatrix} v_a^U & v_b^U & v_c^U \\ v_a^L & v_b^L & v_c^L \end{pmatrix}\frac{1}{3}\begin{pmatrix} 2 & 0 & 1 \\ -1 & \sqrt{3} & 1 \\ -1 & -\sqrt{3} & 1 \end{pmatrix} \tag{A.3}$$

$$= \begin{pmatrix} v_\alpha^\Sigma & v_\beta^\Sigma & v_0^\Sigma \\ v_\alpha^\Delta & v_\beta^\Delta & v_0^\Delta \end{pmatrix} \tag{A.4}$$

The MMC arm power terms $P_{\alpha\beta 0}^{\Sigma\Delta}$ in the $\Sigma\Delta\alpha\beta 0$ reference frame is calculated from the instantaneous power per arm:

$$P_{\alpha\beta 0}^{\Sigma\Delta} = T_{\Sigma\Delta} P_{abc}^{UL} T_{\alpha\beta 0} \tag{A.5}$$

Where the instantaneous power is defined as the product between the arm current and the arm voltage:

$$P_{abc}^{UL} = \begin{pmatrix} v_a^U i_a^U & v_b^U i_b^U & v_c^U i_c^U \\ v_a^L i_a^L & v_b^L i_b^L & v_c^L i_c^L \end{pmatrix} \tag{A.6}$$

The instantaneous power can be defined using the Hadamard product ($\circ$ operator) as [165]:

$$P_{abc}^{UL} = V_{abc}^{UL} \circ I_{abc}^{UL} \tag{A.7}$$

By replacing the power expression P_{abc}^{UL} from (A.7) into (A.5), the arm power can be calculated as:

$$P_{\alpha\beta 0}^{\Sigma\Delta} = T_{\Sigma\Delta} \left(V_{abc}^{UL} \circ I_{abc}^{UL} \right) T_{\alpha\beta 0} \tag{A.8}$$

To express the arm power as a function of the converter voltages and currents in the $\Sigma\Delta\alpha\beta 0$ reference frame, the converter matrices V_{abc}^{UL} and I_{abc}^{UL} can be written as a function of $V_{\alpha\beta 0}^{\Sigma\Delta}$ and $I_{\alpha\beta 0}^{\Sigma\Delta}$ respectively:

$$V_{abc}^{UL} = T_{\Sigma\Delta}^{-1} V_{\alpha\beta 0}^{\Sigma\Delta} T_{\alpha\beta 0}^{-1} \tag{A.9}$$

$$I_{abc}^{UL} = T_{\Sigma\Delta}^{-1} I_{\alpha\beta 0}^{\Sigma\Delta} T_{\alpha\beta 0}^{-1} \tag{A.10}$$

Since a three-phase balanced load is considered, the γ component of the transformation matrix $T_{\alpha\beta 0}$ is null. Consequently, the arm currents $I_{\alpha\beta 0}^{\Sigma\Delta}$ are:

$$I_{\alpha\beta 0}^{\Sigma\Delta} = \begin{pmatrix} i_\alpha^\Sigma & i_\beta^\Sigma & \frac{i^P}{3} \\ i_\alpha & i_\beta & 0 \end{pmatrix} \tag{A.11}$$

In addition, if the inductor voltage drop in each arm is neglected, the converter voltage can be approximated by:

$$V_{\alpha\beta 0}^{\Sigma\Delta} \approx -2 \begin{pmatrix} 0 & 0 & -\frac{E}{4} \\ v_\alpha & v_\beta & v_0 \end{pmatrix} \tag{A.12}$$

By replacing expressions (A.9)-(A.12) into (A.8), the power terms in the $\Sigma\Delta\alpha\beta 0$ reference frame are derived:

$$p_\alpha^\Sigma = \frac{E}{2} i_\alpha^\Sigma - \frac{1}{4} i_\alpha v_\alpha + \frac{1}{4} i_\beta v_\beta - \frac{1}{2} i_\alpha v_0 \tag{A.13}$$

$$p_\beta^\Sigma = \frac{E}{2} i_\beta^\Sigma + \frac{1}{4} i_\beta v_\alpha + \frac{1}{4} i_\alpha v_\beta - \frac{1}{2} i_\beta v_0 \tag{A.14}$$

$$p_0^\Sigma = \frac{1}{6} E i^P - \frac{1}{4} i_\alpha v_\alpha - \frac{1}{4} i_\beta v_\beta \tag{A.15}$$

$$p_\alpha^\Delta = \frac{1}{2} E i_\alpha - \frac{2}{3} i^p v_\alpha - i_\alpha^\Sigma v_\alpha + i_\beta^\Sigma v_\beta - 2 i_\alpha^\Sigma v_0 \tag{A.16}$$

$$p_\beta^\Delta = \frac{1}{2} E i_\beta - \frac{2}{3} i^p v_\beta + i_\beta^\Sigma v_\alpha + i_\alpha^\Sigma v_\beta - 2 i_\beta^\Sigma v_0 \tag{A.17}$$

$$p_0^\Delta = -i_\alpha^\Sigma v_\alpha - i_\beta^\Sigma v_\beta - \frac{2}{3} i^P v_0 \tag{A.18}$$

To have more compact expressions for the arm power, it is possible to define the following complex voltage, current, and power terms:

$$\boldsymbol{v}_{\alpha\beta} = v_\alpha + jv_\beta \tag{A.19}$$
$$\boldsymbol{i}_{\alpha\beta} = i_\alpha + ji_\beta \tag{A.20}$$
$$\boldsymbol{i}^{\Sigma}_{\alpha\beta} = i^{\Sigma}_\alpha + ji^{\Sigma}_\beta \tag{A.21}$$
$$\boldsymbol{p}^{\Sigma}_{\alpha\beta} = p^{\Sigma}_\alpha + jp^{\Sigma}_\beta \tag{A.22}$$
$$\boldsymbol{p}^{\Delta}_{\alpha\beta} = p^{\Delta}_\alpha + jp^{\Delta}_\beta \tag{A.23}$$

The arm power equations $P^{\Sigma\Delta}_{\alpha\beta 0}$ can be written using the previous vector notation from equations (A.19)-(A.23):

$$p^{\Sigma}_0 = \frac{Ei^P}{6} - \frac{1}{4}\Re\{\boldsymbol{v}_{\alpha\beta}\boldsymbol{i}^{c}_{\alpha\beta}\} \tag{A.24}$$
$$\boldsymbol{p}^{\Sigma}_{\alpha\beta} = -\frac{1}{4}(\boldsymbol{v}_{\alpha\beta}\boldsymbol{i}_{\alpha\beta})^c + \frac{E}{2}\boldsymbol{i}^{\Sigma}_{\alpha\beta} - \frac{1}{2}v_0\boldsymbol{i}_{\alpha\beta} \tag{A.25}$$
$$\boldsymbol{p}^{\Delta}_{\alpha\beta} = -(\boldsymbol{v}_{\alpha\beta}\boldsymbol{i}^{\Sigma}_{\alpha\beta})^c + \frac{E\boldsymbol{i}_{\alpha\beta}}{2} - \frac{2}{3}i^P\boldsymbol{v}_{\alpha\beta} - 2v_0\boldsymbol{i}^{\Sigma}_{\alpha\beta} \tag{A.26}$$
$$p^{\Delta}_0 = -\Re\{\boldsymbol{v}_{\alpha\beta}(\boldsymbol{i}^{\Sigma}_{\alpha\beta})^c\} - \frac{2}{3}i^P v_0 \tag{A.27}$$

Appendix B

VHDL codes

B.1 Triangular carrier signal

```
library IEEE;
use IEEE.STD_LOGIC_1164.ALL;
use IEEE.STD_LOGIC_ARITH.ALL;
use IEEE.STD_LOGIC_UNSIGNED.ALL;
--use IEEE.NUMERIC_STD.all;

entity TRIANGULAR_PIPE is
port (CLK : in STD_LOGIC;
      WAVE_OUT : out STD_LOGIC_VECTOR(13 downto 0);
          MAX_C : in STD_LOGIC_VECTOR(13 downto 0);
      RESET :in STD_LOGIC);
end TRIANGULAR_PIPE;

architecture Behavioral of TRIANGULAR_PIPE is

signal count,count1 : UNSIGNED (13 DOWNTO 0);

begin

process(CLK,RESET)
begin
if(RESET = '1') then
    count <= 0;
    count1 <= UNSIGNED(MAX_c);--5000;
elsif(rising_edge(CLK)) then
    --"direction" signal determines the sense of counting (up or down)
        if(count>=0 AND count<UNSIGNED(MAX_c)) then
                count1 <= count1 - 1;
        else
                count1 <= count1 + 1;
        end if;

        if(count<UNSIGNED(MAX_c)+UNSIGNED(MAX_c)) then
                count <= count + 1;
```

```
        else
                count <= 0;
                count1 <= UNSIGNED(MAX_c);
        end if;

end if;
end process;

WAVE_OUT <= conv_std_logic_vector(count1,14);

end Behavioral;
```

B.2 Programmable dead-time

```
library IEEE;
use IEEE.STD_LOGIC_1164.ALL;
use IEEE.NUMERIC_STD.ALL;


entity DT_PIPE is
Port(PATRON_IN: IN STD_LOGIC;
          PATRON_OUT: OUT STD_LOGIC;
          CLK, RESET: IN STD_LOGIC);
end DT_PIPE;

architecture Behavioral of DT_PIPE is

Signal contador: INTEGER RANGE 0 TO 80;
Signal Patron_TEMP1: STD_LOGIC;

begin

Process(CLK, RESET, PATRON_IN)

Begin

if(RESET = '0') then
        contador <= 0;
        Patron_TEMP1 <= '0';
elsif(CLK'EVENT and CLK='1') then
        if(PATRON_IN = '0') then
                Patron_TEMP1 <= '0';
                contador <= 0;
        else
                if(contador < 75) then
                        contador <= contador + 1;
                        Patron_TEMP1 <= '0';
                else
                        Patron_TEMP1 <= '1';
```

```
                End if;
        End if;
End if;

End Process;

PATRON_OUT <= PATRON_TEMP1;

end Behavioral;
```

B.3 Serial communication (Master)

```
----------------------------------------------------------------------------------
--
--   FileName:         spi_master.vhd
--   Dependencies:     none
--   Design Software:  Quartus II Version 9.0 Build 132 SJ Full Version
--
--   HDL CODE IS PROVIDED "AS IS."  DIGI-KEY EXPRESSLY DISCLAIMS ANY
--   WARRANTY OF ANY KIND, WHETHER EXPRESS OR IMPLIED, INCLUDING BUT NOT
--   LIMITED TO, THE IMPLIED WARRANTIES OF MERCHANTABILITY, FITNESS FOR A
--   PARTICULAR PURPOSE, OR NON-INFRINGEMENT. IN NO EVENT SHALL DIGI-KEY
--   BE LIABLE FOR ANY INCIDENTAL, SPECIAL, INDIRECT OR CONSEQUENTIAL
--   DAMAGES, LOST PROFITS OR LOST DATA, HARM TO YOUR EQUIPMENT, COST OF
--   PROCUREMENT OF SUBSTITUTE GOODS, TECHNOLOGY OR SERVICES, ANY CLAIMS
--   BY THIRD PARTIES (INCLUDING BUT NOT LIMITED TO ANY DEFENSE THEREOF),
--   ANY CLAIMS FOR INDEMNITY OR CONTRIBUTION, OR OTHER SIMILAR COSTS.
--
--
----------------------------------------------------------------------------------

LIBRARY ieee;
USE ieee.std_logic_1164.all;
USE ieee.std_logic_arith.all;
USE ieee.std_logic_unsigned.all;

ENTITY spi_master IS
  GENERIC(
    slaves  : INTEGER := 1;  --number of spi slaves
    cpol    : STD_LOGIC := '0';     --spi clock polarity
    cpha    : STD_LOGIC := '0';     --spi clock phase
    d_width : INTEGER := 32); --data bus width
  PORT(
    clock   : IN     STD_LOGIC;     --system clock
    reset_n : IN     STD_LOGIC;     --asynchronous reset
    enable  : IN     STD_LOGIC;     --initiate transaction
    int_m   : IN     STD_LOGIC;
    tx_data : IN     STD_LOGIC_VECTOR(d_width-1 DOWNTO 0);
                                    --data to transmit
```

```
    miso     : IN     STD_LOGIC;      --master in, slave out
    sclk     : BUFFER STD_LOGIC;      --spi clock
    ss_n     : BUFFER STD_LOGIC;      --slave select
    mosi     : OUT    STD_LOGIC;      --master out, slave in
    busy     : OUT    STD_LOGIC;      --busy / data ready signal
    rx_data  : OUT    STD_LOGIC_VECTOR(d_width-1 DOWNTO 0));
                                       --data received
END spi_master;

ARCHITECTURE logic OF spi_master IS
  TYPE machine IS(ready, execute);  --state machine data type
  SIGNAL state       : machine;     --current state
  SIGNAL slave       : INTEGER;
  --slave selected for current transaction
  SIGNAL clk_div     : INTEGER RANGE 0 TO 50;
  SIGNAL addr        : INTEGER RANGE 0 TO 10;
  SIGNAL clk_ratio   : INTEGER;     --current clk_div
  SIGNAL count       : INTEGER;
  --counter to trigger sclk from system clock
  SIGNAL clk_toggles : INTEGER RANGE 0 TO d_width*2 + 1;
  --count spi clock toggles
  SIGNAL assert_data : STD_LOGIC;
  --'1' is tx sclk toggle, '0' is rx sclk toggle
  SIGNAL rx_buffer   : STD_LOGIC_VECTOR(d_width-1 DOWNTO 0);
  --receive data buffer
  SIGNAL tx_buffer   : STD_LOGIC_VECTOR(d_width-1 DOWNTO 0);
  --transmit data buffer
  SIGNAL last_bit_rx : INTEGER RANGE 0 TO d_width*2;
  --last rx data bit location
  SIGNAL flag1       : STD_LOGIC;
  SIGNAL flag2       : STD_LOGIC;
  SIGNAL enable_f    : STD_LOGIC;
BEGIN

  PROCESS(int_m, enable)
  BEGIN
  IF(int_m = '1') THEN
    flag1 <= '0';
  ELSIF(rising_edge(enable)) THEN
    flag1 <= '1';
  END IF;
  END PROCESS;

  PROCESS(int_m, enable)
  BEGIN
  IF(int_m = '1') THEN
    flag2 <= '1';
  ELSIF(falling_edge(enable)) THEN
    flag2 <= '0';
```

```
END IF;
END PROCESS;

enable_f <= flag1 AND flag2;

PROCESS(clock, reset_n)
BEGIN

  IF(reset_n = '0') THEN  --reset system
    busy <= '1';  --set busy signal
    ss_n <= '1';  --deassert all slave select lines
    mosi <= 'Z';  --set master out to high impedance
    rx_data <= (OTHERS => '0'); --clear receive data port
    state <= ready;  --go to ready state when reset is exited
    clk_div <= 25;
    addr <= 0;

  ELSIF(clock'EVENT AND clock = '1') THEN
    CASE state IS    --state machine

      WHEN ready =>
        busy <= '0'; --clock out not busy signal
        ss_n <= '1'; --set all slave select outputs high
        mosi <= 'Z'; --set mosi output high impedance

        --user input to initiate transaction
        IF(enable_f = '1') THEN
          busy <= '1';    --set busy signal
          IF(addr < slaves) THEN
          --check for valid slave address
            slave <= addr;
          --clock in current slave selection if valid
          ELSE
            slave <= 0; --set to first slave if not valid
          END IF;
          IF(clk_div = 0) THEN
          --check for valid spi speed
            clk_ratio <= 1;
            --set to maximum speed if zero
            count <= 1;
            --initiate system-to-spi clock counter
          ELSE
            clk_ratio <= clk_div;
            --set to input selection if valid
            count <= clk_div;
            --initiate system-to-spi clock counter
          END IF;
          sclk <= cpol;
          --set spi clock polarity
```

```
            assert_data <= NOT cpha;
            --set spi clock phase
            tx_buffer <= tx_data;
            --clock in data for transmit into buffer
            clk_toggles <= 0;
            --initiate clock toggle counter
            last_bit_rx <= d_width*2 + conv_integer(cpha) - 1;
            --set last rx data bit
            state <= execute;
            --proceed to execute state
          ELSE
            state <= ready;
            --remain in ready state
          END IF;

        WHEN execute =>
          busy <= '1';
          --set busy signal
          ss_n <= '0';
          --set proper slave select output

          --system clock to sclk ratio is met
          IF(count = clk_ratio) THEN
            count <= 1;  --reset system-to-spi clock counter
            assert_data <= NOT assert_data;
            --switch transmit/receive indicator
            IF(clk_toggles = d_width*2 + 1) THEN
              clk_toggles <= 0;
            --reset spi clock toggles counter
            ELSE
              clk_toggles <= clk_toggles + 1;
             --increment spi clock toggles counter
            END IF;

            --spi clock toggle needed
            IF(clk_toggles <= d_width*2 AND ss_n = '0') THEN
              sclk <= NOT sclk; --toggle spi clock
            END IF;

            --receive spi clock toggle
    IF(assert_data = '0' AND clk_toggles < last_bit_rx + 1 AND ss_n = '0')
    THEN
             rx_buffer <= rx_buffer(d_width-2 DOWNTO 0) & miso;
             --shift in received bit
            END IF;

            --transmit spi clock toggle
            IF(assert_data = '1' AND clk_toggles < last_bit_rx) THEN
              mosi <= tx_buffer(d_width-1);
```

```
              --clock out data bit
              tx_buffer <= tx_buffer(d_width-2 DOWNTO 0) & '0';
              --shift data transmit buffer
            END IF;

            --end of transaction
            IF(clk_toggles = d_width*2 + 1) THEN
              busy <= '0'; --clock out not busy signal
              ss_n <= '1'; --set all slave selects high
              mosi <= 'Z'; --set mosi output high impedance
              rx_data <= rx_buffer;
              --clock out received data to output port
              state <= ready; --return to ready state
            ELSE              --not end of transaction
              state <= execute;   --remain in execute state
            END IF;

          ELSE --system clock to sclk ratio not met
            count <= count + 1; --increment counter
            state <= execute;   --remain in execute state
          END IF;

      END CASE;
    END IF;
  END PROCESS;
END logic;
```

B.4 Serial communication (Slave)

```
library IEEE;
use IEEE.STD_LOGIC_1164.ALL;
use IEEE.NUMERIC_STD.ALL;

entity SPI_Slave is
    Generic ( breite: natural := 32);
    Port ( SCLK : in  STD_LOGIC;
           SS   : in  STD_LOGIC;
           MOSI : in  STD_LOGIC;
           MISO : out STD_LOGIC;
           Dout : out STD_LOGIC_VECTOR (breite-1 downto 0);
           Din  : in  STD_LOGIC_VECTOR (breite-1 downto 0));
end SPI_Slave;

architecture Behavioral of SPI_Slave is
signal dinsr  : STD_LOGIC_VECTOR (breite-1 downto 0);
signal counter : INTEGER RANGE 0 TO 32;
signal doutsr : STD_LOGIC_VECTOR (breite-1 downto 0) := (others => '0');
begin
```

```
  process (SS, Din, SCLK)
  begin
     if (SS='1') then
        dinsr <= Din;
     elsif falling_edge(SCLK) then
        dinsr <= dinsr(dinsr'left-1 downto 0) & '0';
     end if;
  end process;
  MISO <= dinsr(dinsr'left) when SS='0' else 'Z';

process (SS, SCLK)
begin
    if(SS='1') then
        counter <= 0;
        Dout <= doutsr;
    elsif(rising_edge(SCLK)) then
        if(counter>=0 AND counter<32) then
            doutsr(31-counter) <= MOSI;
            counter <= counter + 1;
        end if;
    end if;
end process;

end Behavioral;
```