Analysis, Design and Evaluation of Quasi Z-Source Modular Multilevel Converter

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Abstract

The deployment of renewable energy production capability needs to increase significantly in the near future to be able to meaningfully reduce emissions caused by current electrical power generation. Also, the electrical energy and power generation will have to increase due to the need to decarbonize the transport which currently runs on fossil fuels.

Recently, newly installed renewable energy production capabilities such as wind turbines and photovoltaics outpaced newly built fossil fuels generation capabilities. The voltage generated by these renewable energy sources often fluctuates in accordance with the weather conditions. Therefore, power converters are required to regulate the output voltage and maximize the available generated power. Technically speaking, available power converter solutions with both voltage step-down and step-up capability are indispensable to maximise the capturing of renewable power. For this reason, the development of novel power converter topologies that could bring additional advantages to existing solutions is still under the scope.

A new breed of multilevel converters, which is modular multilevel converter (MMC) which is able to be connected directly in medium and high voltage DC and AC networks, has been proposed and gained much attention. The MMC based on half-bridge sub-modules (HBSMs) is the simplest configuration but provides only voltage-step-down conversion which is not sufficient for effective interfacing with many renewable energy sources.

This thesis proposes the integration of the impedance networks especially quasi Z-source (qZS) network with the HBSM based modular multilevel converter

(MMC). This integration has not previously been reported. The proposed quasi Z-source modular multilevel converter (qZS-MMC) has the advantages of not only performing the commonly used voltage step down function but also voltage step up function. In addition, it was found that the proposed converter has an inherent capability to block the fault current during a DC side fault.

The proposed qZS-MMC consists of two quasi Z-source networks inserted between the terminals of the input DC source and the DC-link terminals of a modular multilevel converter. The operation of the qZS-network requires the introduction of a short circuit at its output terminals in order to increase the energy stored in the qZS-network inductors. This increase in the stored energy provides the converter's voltage boosting capability. To provide the short circuit current path, each qZS-network is connected to a chain-link of series connected switches at its end-terminals. By gating only one of these chain-links, the generated output voltage will be highly distorted. Therefore, two modulation techniques named simultaneously shorted (SS) and reduced inserted cells (RICs), are proposed to avoid any distortion in the output voltage. These techniques are analysed and compared based on a mathematical derivation for the converter internal voltages and currents. Based on these, guidelines for sizing the different passive components and a procedure for estimating the semiconductor losses are presented for each modulation technique. The DC-fault blocking capability of the proposed converter is investigated, where the converter behavior is illustrated for pole-to-pole and pole-to-ground DC side faults. The proposed qZS-MMC is compared with the full-bridge based MMC (FB-MMC) and quasi Z-source cascaded multilevel converter (qZS-CMI) in order to validate its feasibility. The comparison accounts for the required number of the passive and active components, voltage and current stresses, the semiconductor power losses and output voltage waveform quality.

The performance of the proposed converter is evaluated through simulation using PLECs software and different test cases were considered. The simulation results demonstrate the ability of the converter to perform buck-boost operation using the proposed modulation techniques and to block the DC-fault current. A laboratory scaled prototype is built and is used to experimentally validate the operation of the converter and the DC-fault blocking capability.

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Contents

List of Figures

List of Tables

Nomenclature

B	Boost factor
C_{N1}, C_{N2}	Lower qZS-capacitance
C_{U1}, C_{U2}	Upper qZS-capacitance
C_1	Parallel qZS-capacitances
C_2	Series qZS-capacitances
cos φ	Power factor
C_{SM}	SM capacitance
D_{sh}	Shoot-through duty ratio
D_{U1}, D_{N1}	Upper and lower qZS-networks series diodes
E_{CU1}, E_{CU2}	Maximum energy variations of capacitors C_{U1}, and C_{U2}
e_{off}	Turn-off energy of one IGBT
e_{on}	Turn-on energy of one IGBT
e_{rec}	Reverse recovery energy of one diode
f_c	Carrier frequency
f_o	Fundamental output frequency
f_{sort}	Sorting frequency
G	Converter gain
G_{PR}	Open loop transfer function PR controller
i_{Ao}	Instantaneous AC output current
i_{CU1}	Upper qZS-capacitor current
i_{LU1} , i_{LU2}	Upper qZS-inductor currents
i_{LN1} , i_{LN2}	Lower qZS-inductor currents
i_{UA}, i_{AN}	Upper and lower arm currents

i_{2f}	Second order harmonic component in the arm current
i_{cir}	Circulating current
I_L	Average value of qZS-inductor currents
I_m	Peak value of the fundamental phase current
i_{SU}	Instantaneous current in the chain-link devices
i_{SU1}	Instantaneous current in the series devices
I_{UA}, I_{NA}	Peak value of the upper and lower arm currents
I_{UN}	DC component in the arm current
$k_{i\text{-}arm\text{-}SS}$	Arm current ripple factor when using SS technique
$k_{i\text{-}arm\text{-}RICs}$	Arm current ripple factor when using RICs technique
$k_{i\text{-}qZS\text{-}SS}$	qZS-inductor current ripple factor when using SS technique
$k_{i\text{-}qZS\text{-}RICs}$	qZS-inductor current ripple factor when using RICs technique
k_v	Capacitor voltage ripple factor
L_O	Arm inductance
L_S	Source qZS-inductance
L_{N1}, L_{N2}	Lower qZS-inductances
L_{U1}, L_{U2}	Upper qZS-inductances
m	Converter modulation index
N_{ch}	Number of series devices in the chain-link switch
N_U	Number of inserted SMs in the upper arm
N_N	Number of inserted SMs in the lower arm
N_{SM}	Number of SMs in each arm
N_{UA}, N_{UB}, N_{UC}	Number of inserted SMs in the upper arms in phases *A*, *B*, and *C*
$P(\omega.t)$	Instantaneous arm power
P_C (t)	Conduction power losses
$P_{C\text{-}arm}$ (t)	Instantaneous arm conduction losses
$P_{C\text{-}diode}$ (t)	Instantaneous diode conduction power losses
$P_{C\text{-}IGBT}$ (t)	Instantaneous IGBT conduction power losses
$P_{C\text{-}qZS}$ (t)	Instantaneous qZS-network conduction losses
P_{DC}	Input power
$P_{SW\text{-}arm\text{-}RICs}$	Total arm switching power losses when using the RICs technique

$P_{SW\text{-}arm\text{-}SS}$	Total arm switching power losses when using the SS technique
$P_{SW\text{-}fc}$	Instantaneous arm switching dissipated power losses during a carrier frequency cycle
$P_{SW\text{-}fsort}$	Instantaneous arm switching dissipated power losses due to sorting
$P_{SW\text{-}qZS}$	Instantaneous switching power losses for each switch in the chain-link switches
P_{UN}	DC-link active power
R_f	Switching device equivalent resistance
r_O	Equivalent parasitic resistance
S	Apparent power
S_U , S_N	Upper and lower chain-link switches
S_{U1} , S_{N1}	Upper and lower series switches
T	Carrier frequency cycle
T_n	Non-shoot-through interval
T_{sh}	Shoot-through interval
T_{U1}, T_{N1}	Upper and lower qZS-networks series antiparallel switches
v_{Ao}	Instantaneous AC output voltage
v_{LU1} , v_{LU2}	Upper qZS-inductor voltages
v_{LN1} , v_{LN2}	Lower qZS-inductor voltages
v_{LO}	Arm inductor voltage
v_U	Upper arm voltage
v_N	Lower arm voltage
v_{UO}	Upper DC-bus voltages
v_{ON}	Lower DC-bus voltages
v_{UN}	DC-bus voltages
V_{CSM}	SM capacitor voltage
V_{C1}	Average value of parallel qZS-capacitor voltage
V_{C2}	Average value of series qZS-capacitor voltage
v_{cir}	Voltage across the arm inductor due to circulating current
V_{CN1}, V_{CN2},	Average value of the lower qZS-capacitor voltages
v_{CN1}, v_{CN2}	Instantaneous lower qZS-capacitor voltages
V_{CU1}, V_{CU2},	Average value of the upper qZS-capacitor voltages
v_{CU1}, v_{CU2}	Instantaneous upper qZS-capacitor voltages

V_C^*	Reference of the average SMs capacitor voltage
V_{DC}	DC source voltage
V_m	Peak value of the fundamental phase voltage
V_n	Semiconductor device test voltage
V_{UN}	Peak value of the DC-link voltage
V_{UO}	Peak value of the upper DC-link voltage
V_{ON}	Peak value of the lower DC-link voltage
$v_{sh\text{-}N}$	Lower shoot-through modulating signal
$v_{sh\text{-}U}$	Upper shoot-through modulating signal
v_t	Total voltage drop on semiconductor device
V_f	Forward voltage drop of semiconductor device
ΔE	Energy variation of the upper arm
ΔE_{PP}	Peak to peak energy variation
Δi_{cir}	Peak to peak ripple of circulating current i_{cir}
Δv_{CU1}	Instantaneous value of the qZS-capacitor voltage ripple
φ	Phase shift between the output voltage v_{AO} and output current i_{AO}
ω	Fundamental output angular frequency
ω_c	Cutoff frequency

Abbreviations

AC	Alternating Current
ADC	Analogue Digital Converter
ANPC	Active Neutral Point Clamped
APOD-PWM	Alternate Phase Opposition Disposition Pulse Width Modulation
CDSMs	Clamp-Diode Sub-Modules
CHB	Cascaded H-Bridge
CMC	Cascaded Matrix Converter
CMI	Common Mode Inductance
DC	Direct Current
DMI	Differential Mode Inductance
DSP	Digital Signal Processor
FB-MMC	Full Bridge Based Modular Multilevel Converter
FBSMs	Full-Bridge Sub-Modules
FC	Flying Capacitor
FPGA	Field Programable Gate Array
GUI	Graphics User Interface
HBSM	Half-Bridge Sub-Module
HMMC	Hybrid Modular Multilevel Converter
HNPC	H-Bridge Neutral Point Clamped
HPI	Host Port Interface
HPZSI	High-Performance Z-Source Inverter
IGBTs	Insulated Gate Bipolar Transistors
ISN-VSI	Impedance-Source Network Voltage Source Inverter

ISNs	Impedance-Source Networks
IZSI	Improved Z-Source Inverter
MMC	Modular Multilevel Converter
MqZS-CHI	Modified quasi Z-Source Cascaded Hybrid Inverter
MqZS-NPC	Modified quasi Z-Source Neutral Point Clamped
NLC	Nearest Level Control
NPC	Neutral Point Clamped
NST	Non-Shoot-Through
PD-PWM	Phase Disposition Pulse Width Modulation
PEMC	Power Electronics, Machines and Control
PI	Proportional Integral
PMSG	Permanent Magnet Synchronous Generator
POD-PWM	Phase Opposition Disposition Pulse Width Modulation
PR	Proportional Resonant
PS-PWM	Phase-Shift Pulse Width Modulation
PWM	Pulse Width Modulation
qZS-CMI	quasi Z-Source Cascaded Multilevel Converter
qZSI	quasi Z-Source Inverter
qZS-MMC	quasi Z-Source Modular Multilevel Converter
RESs	Renewable Energy Sources
RICs	Reduced Inserted Cells
SHE	Selective Harmonics Elimination
SMs	Sub-Modules
SS	Simultaneously Shorted
ST	Shoot-Through
SVM	Space Vector Modulation
SZSI	Series Z-Source Inverter
THD	Total Harmonic Distortion
UNIFLEX-PM	Universal Flexible Power Management System
VSI	Voltage Source Inverter
WES	Wind Energy System
ZSI	Z-Source Inverter
ZS-MMC	Z-Source Modular Multilevel Converter

Chapter 1
Introduction

1.1 Motivation for the project

The world demand to use more renewable energy is continuously growing. To fulfil this demand, the installation of new and powerful wind turbines (WT) and photovoltaic (PV) systems has become necessary. Often, these renewable energy sources are connected to the main power grid through power converters. The output voltage of most renewable energy sources fluctuates in a wide range with changes in the operating conditions e.g. wind speed and solar irradiance. Therefore, having a power converter that can compensate for these fluctuations by being able not only to perform a voltage step-down, but also to step-up the voltage may be quite useful. For example, the power converter presented in [1] can provide voltage step-up function with a gain range up to 1:4, to enable interfacing wind turbine system to medium voltage AC grid. Whilst in [2], the power converter with a gain range of 1:10 is used to connect photovoltaic system to low voltage grid.

Multilevel converters are considered the best candidate converters for renewable energy applications due to their good output voltage waveform quality formed by using small voltage steps. Among multilevel converters, the modular multilevel converter (MMC) has received a lot of attention.

The half-bridge submodule (HBSM) based MMC is considered as the simplest configuration of a MMC [3]. However, it faces some critical drawbacks of being a voltage step-down converter where the output voltage is limited to one half of the DC-link voltage and consequently it becomes inappropriate for the grid interfacing of many renewable energy sources. Also, it has no ability to deal with faults at the DC terminals of the converter. Using full-bridge submodule (FBSM) instead of half-bridge submodule has been recommended to overcome these shortcomings [4]. Due to the capability of the FBSM to provide negative voltage state beside to zero and positive voltage states, the FBSM based MMC has an inherent DC-fault blocking capability and can block the overcurrent caused by short-circuiting the DC bus powered by the AC source. In addition, various studies have used the negative voltage state from the FBSM to increase the modulation index and the AC output voltage [5-7]. Under constant DC source voltage and SMs voltage rating, the FBSM based MMC requires more SMs in order to increase the modulation index and consequently the AC output voltage can be boosted [6]. However, the FBSM based MMC requires more active switches (e.g. IGBTs) twice as many HBSM based MMC, which not only increases the converter cost, but increase the total power losses.

Therefore, how to improve the HBSM based MMC to achieve these features is an interesting point to study. Impedance networks have been integrated with other multilevel converters, cascaded H-bridge and neutral point clamped converters, to provide a voltage-boost function. Since the impedance networks have not been adopted with the MMC before, it is suggested to integrate them with the HBSM based MMC to provide a voltage-boost function. Thus, this thesis aims to integrate an impedance networks with the HBSM based MMC, including designing proper modulation techniques and identifying its features and limitations.

1.2 Project objectives

The research described in this thesis aims to investigate using an impedance network in conjunction with modular multilevel converter as a solution for medium voltage applications. To achieve this aim, the main project objectives are defined as:

- Reviewing existing multilevel converter topologies considering their benefits, drawbacks, and applications.
- Reviewing impedance networks based multilevel converters.
- Investigating the impedance network concept to add voltage-boost function to the half-bridge submodule based modular multilevel converter.
- Proposing a novel impedance network based MMC topology and the corresponding modulation techniques to effectively provide proper operation for the resulting power converter.
- Developing guidelines for sizing different passive components for the converter design.
- Presenting a procedure for losses estimation for the proposed converter to estimate the converter efficiency.
- Investigating the ability of the proposed converter to block DC-side faults.
- Comparing the proposed converter with other existing topologies, identifying its advantages and disadvantages.
- Validating the proposed converter through simulation and experimental studies.

1.3 Thesis outline

The thesis is organized into eight chapters.

Chapter 2 presents a review of the common multilevel converter topologies considering their benefits, drawbacks and applications. The ability of multilevel converters to provide buck or/and boost functions is reported and accordingly the suitably for renewable energy sources integration with the electric grid is defined. The review also investigates the integration of impedance networks with multilevel converter topologies to highlight the main features and limitations for these topologies.

Chapter 3 presents the MMC operation principles. The circuit structure, the features of the MMC, sub-modules configurations, DC-fault blocking capability,

mathematical model, modulation techniques and the SMs capacitor voltage balance are all discussed.

In **Chapter 4**, a novel impedance network based MMC is proposed. The proposed converter integrates the Qis-network with the HBSM based MMC. The proposed converter can provide a voltage-boost function and has an inherent DC-fault blocking capability. The operating principles of the quasi Z-source MMC (Qis-MMC) is introduced. Two modulation techniques are proposed, which are the simultaneously shorted (SS) and reduced inserted cells (RICs) methods, in order to achieve a voltage boost function without any distortion in the output voltage. The advantages and disadvantages of these two modulation techniques are highlighted. A scheme to suppress the low order even harmonic components in the circulating current and provide stable operation under components asymmetry due to tolerances is presented.

Chapter 5 provides systematic design guidelines for sizing the passive components of the converter. A procedure for estimating the semiconductor losses is presented for each modulation technique. Simulation studies are presented to demonstrate the feasibility and validity of the voltage-buck and voltage-boost functions. Finally, potential applications are suggested.

Chapter 6 provides a comparison between the proposed qZS-MMC, the full-bridge based MMC and the quasi Z source cascaded multilevel converter. The proposed so-MMC under DC-side fault conditions is also analysed. The converter behavior is illustrated for pole-to-pole and pole-to-ground DC-faults. The converter response to faults is validated through simulation studies in this chapter.

Chapter 7 introduces the design of the laboratory rig which is used to validate the performance of the proposed qZS-MMC. A single-phase converter is designed with a 5-level output voltage waveform, output power of 2 kW and output voltage of 170 V. The measurement circuits and PWM vector generation are also described. The experimental results are presented. The operation principle, modulation techniques and DC-fault blocking capability, presented in Chapter 4 and Chapter 6 and validated by simulation, are experimentally validated in this chapter.

In **Chapter 8,** the three-phase qZS hybrid MMC (qZS-HMMC) is proposed. The operation principle of the proposed configuration with the RICs technique is presented. The work in this chapter is considered as an initial study for the qZS-HMMC and this topology still needs further investigation.

Chapter 9 concludes the presented work in this thesis, summarizes the contributions and also proposes the potential directions for the future work.

Chapter 2

Literature Review

Renewable energy sources (RESs) such as wind turbines and photovoltaics are being widely adopted to help reduce greenhouse gas emissions [8]. These energy sources are connected to the electrical grid through power converters, which are used to accommodate and regulate the variations of the generated output voltage [8, 9] . Multilevel converters are often considered as the best candidate for renewable energy applications due to their feature of improved output waveform quality [10]. Moreover, multilevel converters can be combined with an impedance network topology to enhance the operation with RESs [11, 12].

This chapter provides a literature review on the different topologies of multilevel converters. The following section will also give a review of the main common impedance network topologies and the operation principles for the basic topology. Then, the previously reported impedance network based multilevel converter topologies are presented. Finally, the chapter is concluded, highlighting the motivation for this thesis.

2.1 Multilevel topologies

The operating principle of the multilevel converter depends on dividing the DC-link voltage directly or indirectly to get a number of voltage levels in the AC output voltage, leading to better AC waveform quality. Multilevel converters have many advantages compared to two-level converters for example better

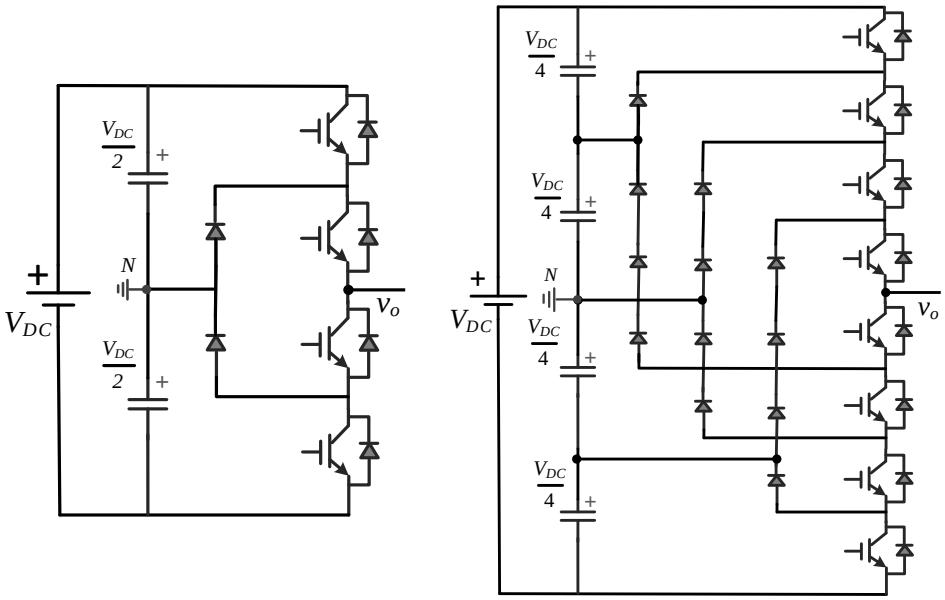
power quality, lower THD, lower *dv*/*dt*, higher operating voltage capability, and reduced voltage stress applied on each switch [10, 13-15]. The most common multilevel converters topologies are the neutral point clamped (NPC) [16], flying capacitor (FC) [17], and cascaded H-bridge (CHB) [18] converters.

The neutral point clamped (NPC) converter uses clamped diodes and cascaded capacitors to produce multiple levels in the output voltage [19]. The clamping diodes clamp the switches to one capacitor voltage level. For higher number of levels, voltage balancing between DC-link capacitors is required. This topology suffers from unequal distribution of power losses among the inner and outer switches. The number of clamping diodes increases rapidly with increasing the number of levels. Single-phase 3-level and 5-level circuits are shown in Fig. 2.1. The 3-level NPC back-to-back configuration has already been applied in wind energy systems [12]. The NPC converter in a 3-level configuration has also found industrial applications such as medium-voltage motor drives [19, 20].

The flying capacitor (FC) converter configuration shown in Fig. 2.2 is similar to that of the NPC converter, where instead of using clamping diodes, the FC converter uses flying capacitors to clamp the switches to one capacitor voltage level [13]. For this converter, as the number of AC output voltage levels (n) increases, the number of capacitors increases rapidly as $(n-1)\cdot(n-2)/2$. In addition, balancing the FC voltages issue should be considered, the complexity increases with increasing number of levels. Due to the aforementioned balancing issue, applications of the FC converter are restricted to 3-level and 4-level circuits [10, 13, 21], particularly in medium voltage drives applications.

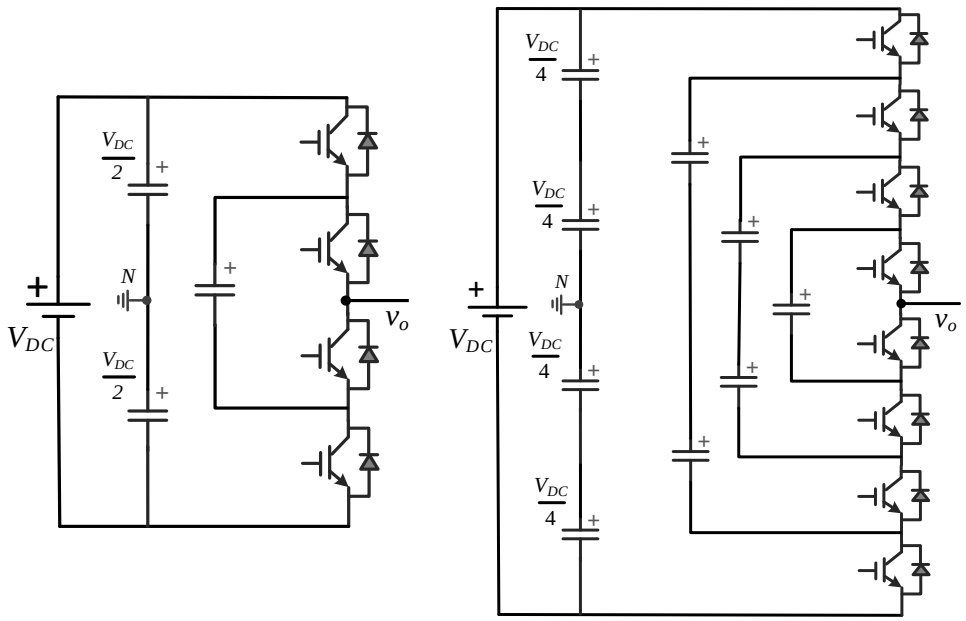
The cascaded H-bridge (CHB) converter [14], which has a modular structure, composed of cascaded full-bridge units can be applicable in high voltage applications. This arrangement is shown in Fig. 2.3 for a 5-level circuit. The CHB converter requires multiple isolated DC sources which can be obtained from separate DC sources or isolated multi-pulse diode rectifiers. The major drawback of this topology is the high number of isolated DC sources, which equals to the number of H-bridge units. The cascaded units need to be balanced especially if their components are asymmetric [13]. This converter can be suitable for power system applications such as FACTs devices [13, 22]. The

CHB converter has been reported for photovoltaic power conversion, which can easily be configured to provide separated DC sources [11, 23]. Based on the CHB converter, the Universal Flexible Power Management system (UNIFLEX-PM) is presented, which has the capability of interconnecting different electrical grids [24-26].



(a) (b)

Fig. 2.1: NPC multilevel converter for, a) 3-level and b) 5-level



(a) (b)

Fig. 2.2: FC multilevel converter for, a) 3-level and b) 5-level

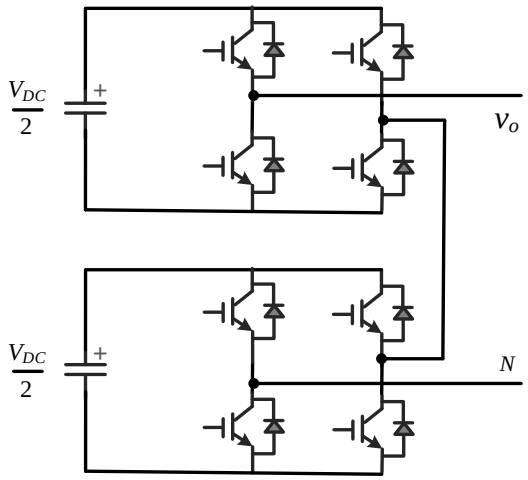


Fig. 2.3: Cascaded H-bridge 5-level converter

The development of multilevel converters has not been stopped at the traditional converters. Other topologies have been proposed, which are a result of introducing some upgrades to the traditional converters or hybrid of the traditional circuits. Among these converters are the active NPC (ANPC), the H-bridge NPC (HNPC) and the cascaded matrix (CM) converters [13].

The modular multilevel converter (MMC) has drawn significant attention due to its attractive features such as modularity, scalability and failure management [27]. The idea of the MMC comes from the traditional two-level voltage source converter where there are two switches per leg, as shown in Fig. 2.4a. By replacing each switch with the so-called “arm” or “chain-link” with the series connection of two-level half-bridge sub-modules, the MMC was formed as shown in Fig. 2.4b. The chain-link concept is obtained from [28] and depends on distributed energy storage. An inductor is required in each arm to limit the current ripple caused by the instantaneous voltage difference which is naturally produced between the DC-link voltage and the two arm voltages [27]. The MMC can work as inverter, rectifier, DC-DC converter, and AC-AC converter [27].

The MMC was firstly proposed with half-bridge sub-module (HBSM), considered as the simplest and the cheapest configuration [3] as shown in Fig. 2.4c. However, using HBSM limits the converter output voltage to half of the DC-link voltage (V_{DC}/2) and is therefore considered inappropriate for interfacing many renewable energy sources to the AC grid systems as it only works as a step-down converter. In addition, it has no ability to deal with the DC-faults [3].

Therefore, the MMC with HBSM must be upgraded with additional hardware to withstand the DC-fault currents and provide voltage step-up function.

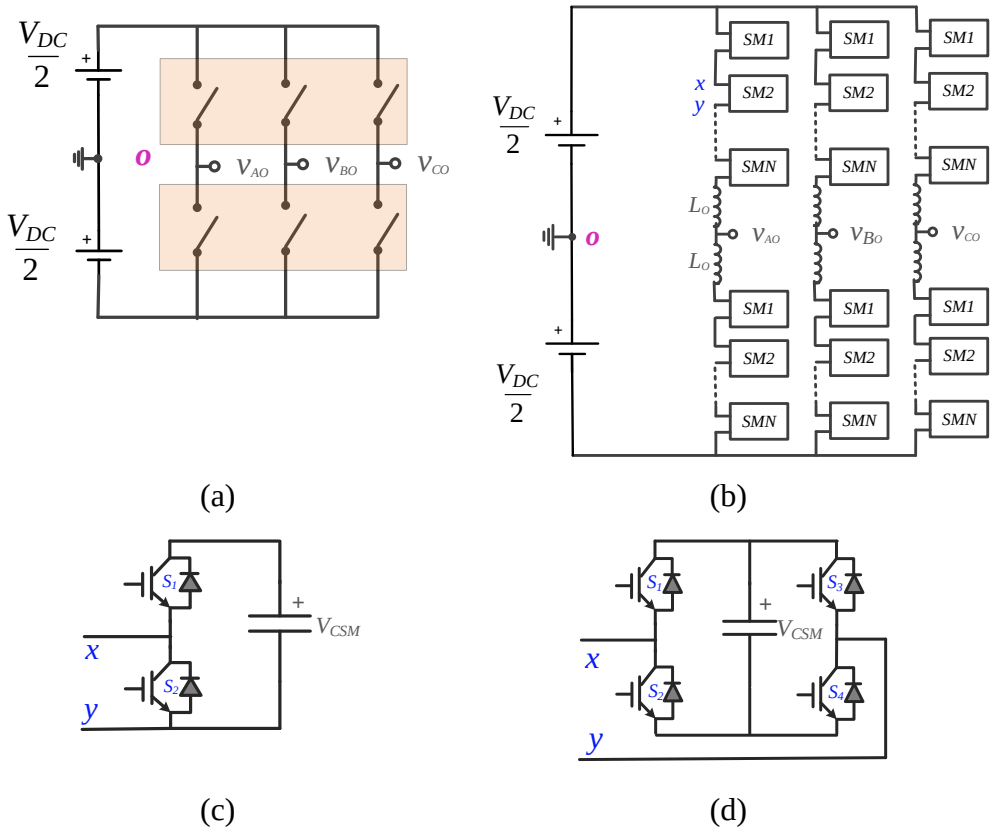


Fig. 2.4: MMC concept realization and its sub-module topologies

Another configuration of the MMC uses full-bridge sub-module (FBSM) [4], as shown in Fig. 2.4d. The FBSM based MMC can provide DC-fault blocking capability and also allows the converter to work in boost mode, which allows the output voltage to exceed half of the DC-link voltage. By increasing the modulation index (which defines the ratio between the AC output voltage and half of the DC-link voltage) to be greater than 1, the MMC operates in boosting mode. This can be achieved depending on the capability of the FBSM to generate the negative voltage states [6]. However, under constant DC source voltage and SMs voltage rating, the FBSM based MMC requires more SMs in order to increase the modulation index and consequently the AC output voltage can be boosted [6]. The FBSM based MMC is suitable for interfacing many renewable energy sources to the electrical grid. For example, a wind turbine generation system which employs a FBSM based MMC is presented in [4]. However, the

FBSM based MMC requires two semiconductor switches in the conduction path, which not only increases the converter cost, but also can increase the power losses. The work described in [6] showed that when a FBSM based MMC operates with a voltage step-up function, the SM capacitor (storage) requirements will be decreased, especially at a boost gain of 1.414.

An interesting solution can be achieved by combining half-bridge and full-bridge sub-modules, where the number of semiconductor switches is reduced compared to the FBSM based MMC. Depending on the ratio of the number of FBSM to the number of HBSM, the DC-fault blocking capability and the voltage step-up capability can be ensured [29]. For ratio that are equal to or higher than 2 (the number of FBSM equals the number of HBSM), the converter can block the DC-faults [30]. While the ratio should be equal or higher than 0.5 (the number of FBSM is twice the number of HBSM) to provide voltage step-up function for the hybrid MMC [29]. A detailed design has been given in [31] for all modulation indices, which illustrates the fluctuation waveforms (charging and discharging) of both the HBSM and FBSM capacitors.

This hybrid MMC (HMMC) has a limitation in its operation where the boosted output voltage should not exceed a specific value as this causes a capacitor voltage imbalance problem between the HBSMs and FBSMs [31]. The FBSMs can charge or discharge regardless of the arm current direction, while HBSMs can charge (discharge) only during positive (negative) states of the arm current. At a specific operating point, the negative current becomes insufficient to allow the half-bridge sub-module to discharge, which will lead to a steady voltage increase of the SMs capacitors of the half-bridge sub-module. The theoretically and experimentally investigations given in [29] show that the maximum output voltage is restricted to about 1.63 times of half of the DC-link voltage at unity power factor, otherwise half-bridge and full-bridge sub-modules will be unbalanced.

The classical multilevel converters (NPC, FC and CHB) are incapable of performing the voltage boost function when working in an inversion mode. These converters can be improved with additional hardware to provide a voltage step-up capability and then will be appropriate for interfacing renewable energy sources (such as photovoltaic and wind energy systems) to an AC electrical grid.

Recently, the impedance-source networks (ISN) were integrated at the DC-link terminals of the 2-level voltage source inverter (2L-VSI) to provide a voltage boost capability [32, 33]. This concept has been used to extend the advantages of ISN to multilevel converters, this is briefly discussed in the following sections.

2.2 Impedance network topologies

In the last two decades there has been a trend to consider impedance-source network VSI (ISN-VSI) topologies. The first ISN-VSI was suggested by F. Z. Peng in 2002 and was referred to as Z-source inverter (ZSI) [33] as shown in Fig. 2.5. The ISN-VSI topologies are one of the promising topologies in power converters in applications where there is a need to operate in either buck or boost modes with only one power conversion stage. These converters typically have a two-port network connected between the DC source and the traditional VSI circuit, composed of inductors, capacitors and diodes or/and switches, as shown in Fig. 2.5 for a basic ZSI example circuit.

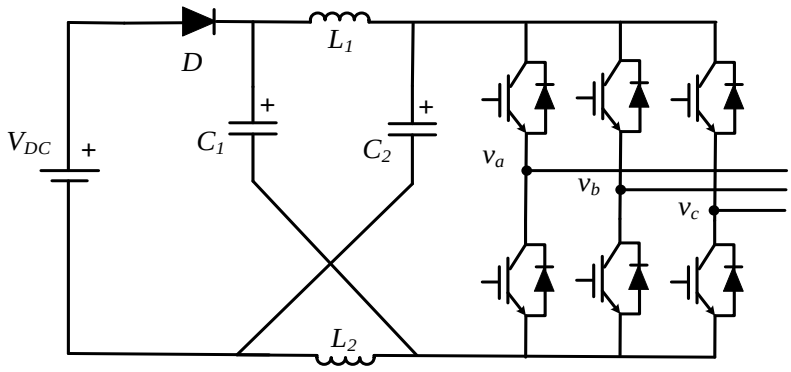


Fig. 2.5: Z-source inverter topology

Generally, the voltage boost capability of the ISN-VSI requires the introduction of a short circuit (shoot-through) at the impedance network output terminals in order to increase the energy stored in the impedance network inductors which is later transferred to the impedance network capacitors. The shoot-through states are inserted during the zero voltage states of the switching pattern [33]. The shoot-through states are formed by gating both the upper and lower devices of at least one inverter leg.

Impedance network topologies have been emerged in applications such as power generation wind turbines [34] , photovoltaic system [35, 36], and fuel cells [37]. Other examples include automotive applications [37, 38] and adjustable speed motor drives [39, 40].

2.2.1 Basics of Z-source inverter

The unique feature of the basic Z-source inverter is that the fundamental peak output voltage can be theoretically regulated for any values between zero and infinity [32]. The ZSI consists of two inductors (L_1, L_2), two capacitors (C_1, C_2) and a diode as shown in Fig. 2.5. The diode is required to guarantee unidirectional current flow. To provide bidirectional current flow, an IGBT can be connected in antiparallel to the diode.

In a traditional voltage source inverter (VSI) there are eight switching states [41]. Six of the states are active states where the load is connected directly to the supply voltage. The remaining two states are null states where either all upper or lower switches are conducted simultaneously to the same voltage. The null states achieve zero line-voltage across the load terminals. For a ZSI there is an additional state called the shoot-through state where the DC-link terminals are shorted by gating both the upper and lower switches of at least one inverter leg [33]. Both the null and shoot-though states achieve zero line-voltage across the load terminals. Therefore, the shoot-through states are inserted within the null states without affecting the active states or the line-voltage across the load. The main difference is that the shoot-through states enable the boosting of the DC-link voltage through the impedance network, where the DC-link voltage V_{UN} can be expressed by (2.1) and consequently the peak value of the phase voltage V_m can be expressed by (2.2) [33, 42].

$$V_{UN} = \frac{V_{DC}}{1 - 2 \cdot T_{sh} / T} = BV_{DC} \tag{2.1}$$

$$V_m = \frac{mV_{UN}}{2} = \frac{mV_{DC} / 2}{1 - 2 \cdot T_{sh} / T} \tag{2.2}$$

where T_{sh} and T are the shoot-through interval and switching period, B is the boost factor and m is the converter modulation index. From (2.1) and (2.2), the output voltage V_m can be controlled from 0 to half the DC source voltage $V_{DC}/2$ by altering m ($0 < m < 1$) and setting $T_{sh} = 0$. Therefore, the output voltage is stepped down (buck mode). To step up the voltage (work in the boost mode), T_{sh} is selected such that $T_{sh} > 0$, while m is given by:

$$m = 1 - T_{sh} / T \tag{2.3}$$

The ZSI faces some drawbacks, such as discontinuous source current, high inrush current, unidirectional power flow, light load operation, and high voltage stress on switches [32]. Therefore, researchers are interested in improving the performance of the original circuit and to mitigate the limitations associated with the ZSI [33, 43-48]. The quasi Z-source inverter (qZSI) can provide continuous source current and reduce voltage rating for one of the network capacitors [43]. The improved ZSI (IZSI) and the series ZSI (SZSI) were proposed in [46, 49] to limit the inrush current value and reduce the capacitor voltage stress. For a wide load range, the high performance ZSI (HPZSI) was proposed to solve the light load operation problem [50].

All these topologies produce the same DC-link voltage V_{UN} but have a high voltage stress on the inverter switches. For a high boost factor B, a high value of shoot-through interval T_{sh} is required and consequently the maximum modulation index m decreases according to (2.3). Therefore, the output voltage will be a smaller fraction of the DC-link voltage (2.2), which means that the DC-link voltage will not fully be utilised to generate the output voltage and a high voltage stress is seen by the inverter switches. In addition, operating at low values of m will affect the output power quality and lead to a poorer harmonic spectrum of the output voltage (higher THD).

Recent research had considered improving the dependency between the modulation index m and the boost factor B. This can be achieved by obtaining a high boost factor while maintaining a high modulation index value. This is considered as the main inspiration for the development of the other impedance network categories [51-56].

Various modifications have been proposed for the main ZSI circuit, such as adding or removing switches, capacitors and/or coupled inductors [32]. According to [32], there are four categories which are switched inductor [51, 57, 58], cascaded quasi Z-source [59], tapped inductors [52, 60] and magnetically coupled inductors [53-56, 61-64].

Researchers have also considered merging the impedance-source network topologies with the multilevel converters to combine the advantages of both [65-68]. The Z-source and quasi Z-source have received a lot of attention with multilevel converters. Therefore, the next section discusses multilevel converters with impedance network topologies.

2.2.2 Impedance network multilevel converter

As discussed in section 2.1, multilevel converters have some advantages in terms of better harmonic performance compared to 2-level VSIs for different applications, such as for medium voltage motor drives and interface between renewable energy sources and the main electric grid [13, 19]. However, most multilevel converters are unable to provide a voltage-boost function [69]. Therefore, the combination of the impedance networks with multilevel converters provides not only a voltage-buck but also a voltage-boost function whilst with distributing the voltage stress between the switches. From the overview, the neutral point clamped (NPC) inverter and cascade H-bridge (CHB) inverter can be integrated to impedance networks [69].

A Z-source impedance network has been integrated with a 3L-NPC, with two Z-source impedance networks attached between the two isolated DC sources and the conventional 3L-NPC inverter, as shown in Fig. 2.6 [70]. The DC-link voltage and the converter output voltage can be determined in a similar way to the two-level ZSI using (2.1) and (2.2). To achieve the shoot-through state, both the Z-source networks can be fully or partially shorted [70, 71], and both should be boosted by equal time intervals to avoid voltage balancing problems. Practically, using two Z-source networks is not cost effective, since it uses two isolated DC sources and two impedance networks, increasing the cost and weight of the converter [69]. In addition, this topology requires a modulator for boosting balance of the two networks [71].

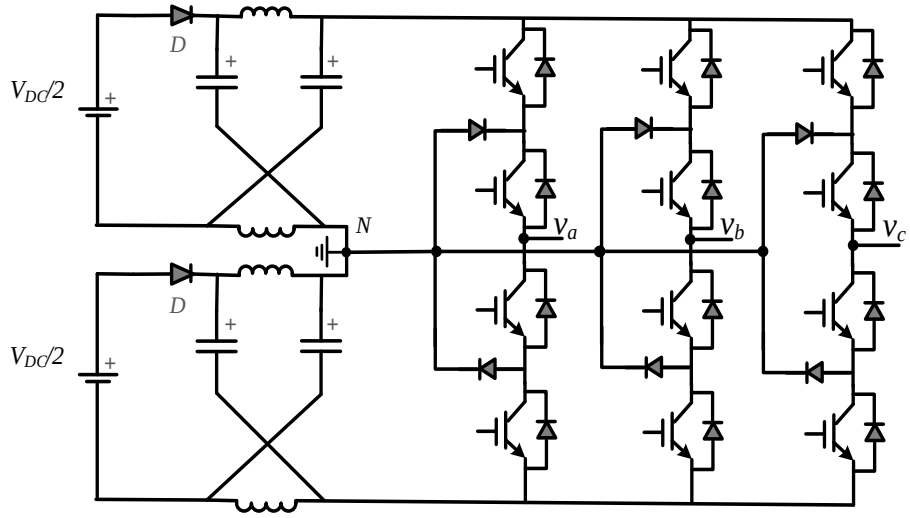


Fig. 2.6: Three-level NPC with two Z-source networks

To reduce the passive component count, a single Z-source impedance has been proposed [70]. This circuit uses a split-DC source (two non-isolated supplies) and a single Z-source network as shown in Fig. 2.7. Although the voltage rating of the Z-source capacitors is doubled, this topology is considered as an optimized topology in terms component count.

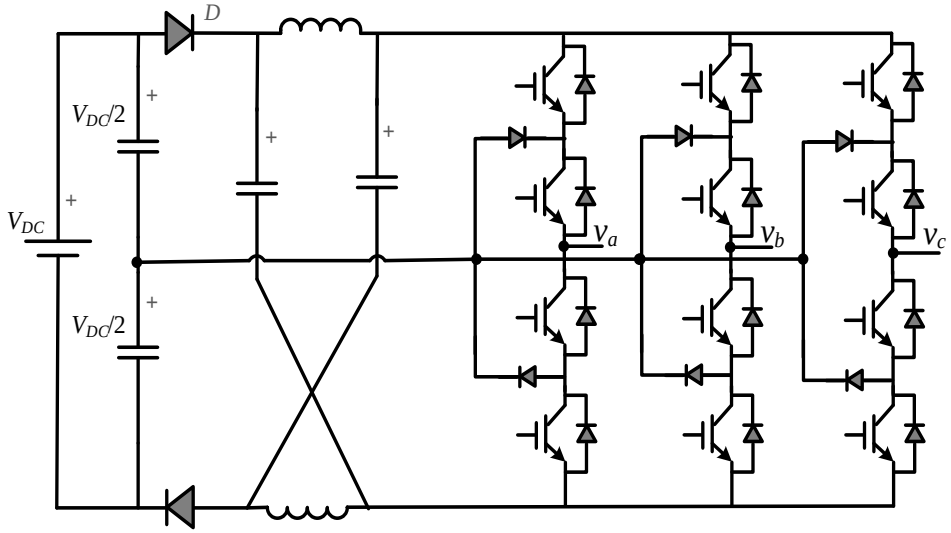


Fig. 2.7: Three-level NPC with single Z-source network

The quasi Z-source (qZS) network, which has the feature of continuous source current, has been integrated with a 3L-NPC inverter in single-phase [72] and three-phase [73] configurations. Fig. 2.8 shows the quasi Z-source 3L-NPC

inverter with two qZS circuits and a single source. Although the number of required passive components is the same as the3L-NPC with two Z-source networks, the 3L-NPC with the qZS-networks only uses one DC source and reduces voltage rating of two capacitors compared with the 3L-NPC with two Z-source networks [32, 69].

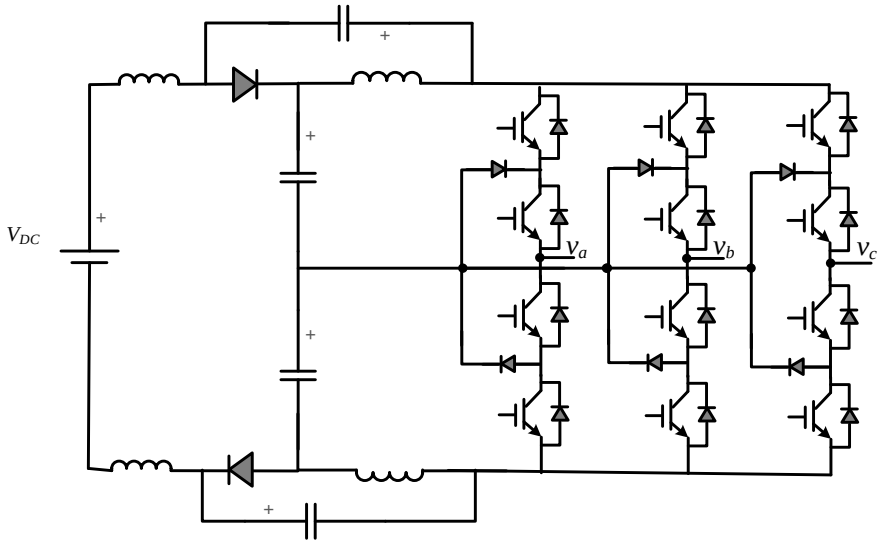


Fig. 2.8: Three-level NPC with quasi Z-source network

Other impedance-source networks have been integrated with the 3L-NPC, such as T-source, Γ-source [66], transformer Z-source (transformer-based impedance network) achieve high gain at high modulation index. Using these networks achieves lower components stress voltages compared with Z-source and quasi Z-source networks particularly at high gain value [66].

To extend the impedance-source networks for combination with a five-level NPC inverter, the Z-source 5L-NPC has been proposed [68]. This topology has two Z-source networks attached between the two isolated DC sources and the conventional 5L-NPC converter, as shown in Fig. 2.9. Each supply needs to be split using two capacitors. [68] identified partial shoot-through states instead of using a full DC-link shoot-through. In this circuit only the upper part of the upper Z-source network circuit and lower part of lower Z-source network are shorted. It is hard to short the lower part of the upper Z-source network circuit and upper part of lower Z-source network as this will cause drop in the output voltage level.

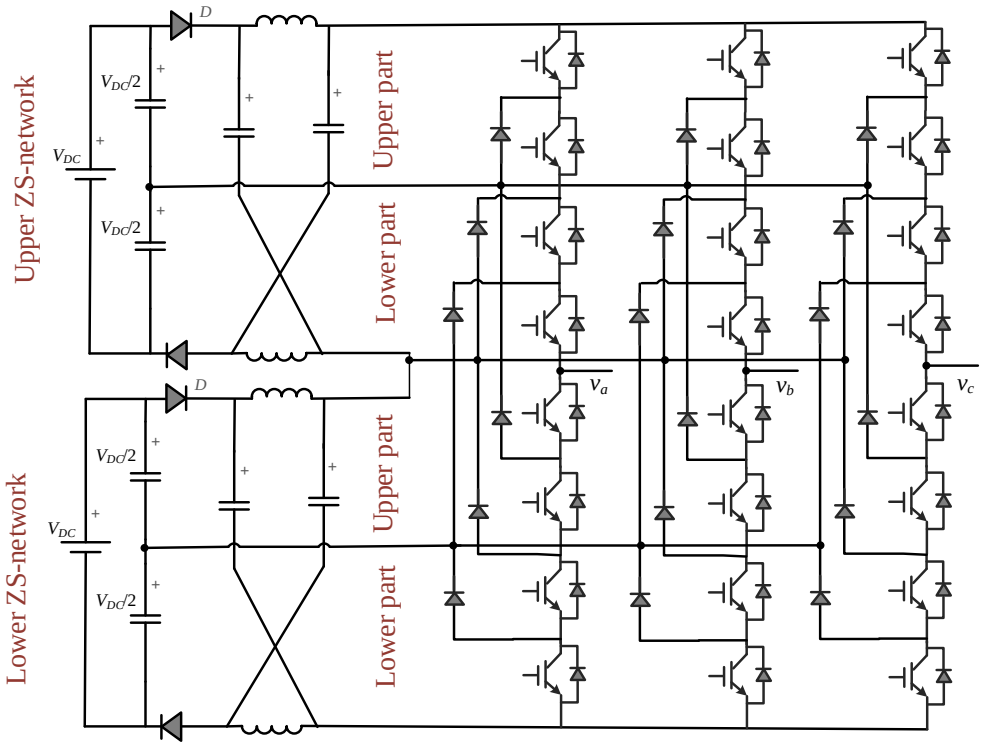


Fig. 2.9: Five-level NPC with two Z-source networks

Recently, a three-phase modified qZS-network with three-level NPC inverter (MqZS-NPC) [74] and a single-phase modified qZS five-level hybrid cascaded inverter (MqZS-CHI) have been proposed in [75]. Both topologies use two qZS-networks, removing the source inductors and implementing diode between the DC source and upper qZS-network. The two topologies can provide higher gain and boost factor, but the source DC current is discontinuous.

The cascaded H-bridge (CHB) multilevel converter with a qZS-network has been studied [65, 76]. The qZS-network is introduced in each module in the CHB, as shown in Fig. 2.10. This converter requires multiple isolated DC sources, which can be obtained from photovoltaic (PV) panels for example. The research for this integration focused on photovoltaic applications for single-phase and three-phase electrical systems [67, 77]. The number of output voltage levels can be increased by cascading more modules of the CHB based qZS-networks [68]. However, more qZS-networks are required with an increase in the number of sub-modules because each sub-module requires a qZS-network.

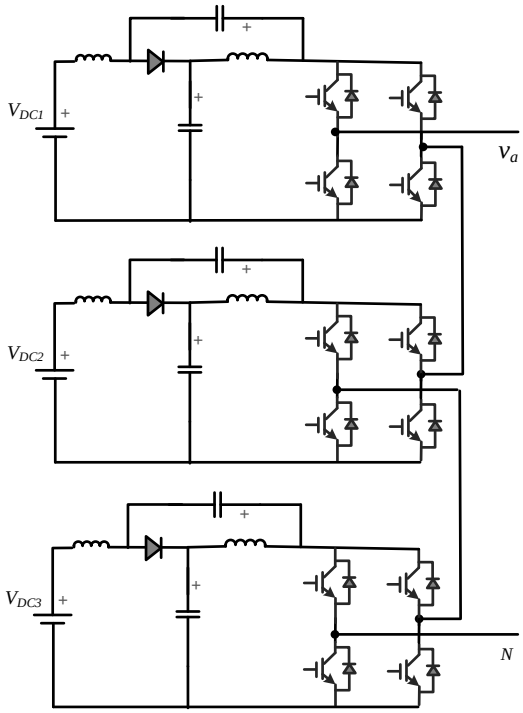


Fig. 2.10: Phase-a seven-level cascaded H-bridge converter

2.3 Conclusions

This chapter has presented a brief survey of multilevel converter topologies, which have been integrated with renewable energy sources. Multilevel converters can provide a good AC waveform quality and harmonic performance. Since most of the multilevel topologies operate in buck mode, the impedance networks can be integrated with the multilevel topologies to achieve a voltage-boost function in order to be suitable as an interface between renewable energy sources and the electric grid. Examples of this integration have been reviewed.

The previously reported impedance network based multilevel topologies have some limitations. For example, the integration of Z-source networks with NPC multilevel converter is only practically realizable with three-level and five-level NPC. On the other hand, other impedance networks (qZS, TZ and transformer Z-source) are restricted to three-level NPC multilevel converters. For a higher number of output voltage levels, more impedance networks are required and it becomes impossible to introduce the shoot-through state for all these impedance-source networks [68] without distorting the output voltage. Instead,

the CHB multilevel converter based on quasi Z-source (qZS) network can be extended to a higher number of output voltage levels by cascading more modules. However, a higher number of isolated DC sources and qZS-networks are required when increasing the number of modules.

The MMC, which has attractive features such as modularity, scalability, and failure management capability, was briefly presented. HBSM based MMC, which is considered the simplest configuration, can always generate output voltage lower than half of the DC-link voltage, and also has no ability to deal with the DC-fault. These limitations are solved by replacing HBSMs by FBSMs, but the number of semiconductor switches are doubled. The hybrid MMC mixes between HBSMs and FBSMs to reduce the switches count but the voltages unbalance problem between sub-modules may appear. Therefore, the HBSM, FBSM, and hybrid based MMC circuits face some difficulties in providing voltage-boost function, components counts and voltage balancing problem.

Interesting findings from this literature review are that the currently reported multilevel converters with impedance network have limitations and the impedance networks have not yet been adopted with the MMC. The integration of the impedance network concept to the MMC may become a competitor to NPC and CHB based qZS-network topologies in terms of the number of output voltage levels and number of required isolated DC sources and qZS-networks. Therefore, this thesis will study the integration of the impedance network with the MMC to cover this gap in the literature and to understand the advantages and disadvantages of this integration compared with some other impedance networks based multilevel topologies.

Chapter 3
Operation Principles of Modular Multilevel Converter

This chapter introduces the operation principles of the modular multilevel converter (MMC) on which the development of the proposed converter relies. MMC circuit and sub-modules configurations, features, a mathematical model of the MMC and modulation techniques are covered in this chapter. Also, a capacitor voltage balancing mechanism to ensure equal voltage of the sub-module capacitors is presented.

3.1 Operation principles of the MMC

The structure of a single-phase MMC is shown in Fig. 3.1. The MMC leg consists of an upper and a lower arm. Each arm is formed by N_{SM} series-connected identical inverter sub-modules (SMs), and an arm inductor (L_O). Each SM is usually an independent VSC with a floating DC capacitor which means is only receiving power from the MMC arm (no additional power supply). Each SM can generate either a positive or zero voltage (sometimes negative voltage level with specific SMs) into the corresponding arm to help synthesize the desired arm voltage [78]. The larger the number of SMs that are used for the same DC-link voltage, the smaller the DC link SM voltage is needed which also leads to smaller voltage steps. This leads to a better quality of the AC output

voltage and consequently smaller THD. Using a suitable modulation strategy, the arm voltage is composed of the AC fundamental voltage and a DC voltage component equal to half of the DC-link voltage, where v_U is the upper arm voltage while v_N is the lower arm voltage. The AC output voltage v_{Ao} is formed co-operatively by combining the upper and the lower arms. The arm inductor L_O is used to limit the current surge caused by the instantaneous voltage difference between the two arms which is naturally produced due to the instantaneous state of the SMs in each arm. The upper and lower arm inductors may be noncoupled or coupled in which case the size can be reduced by making sure the magnetization of the core can be achieved only by the circulating current and not by the main load current which can be equally split between the two arms [4, 79].

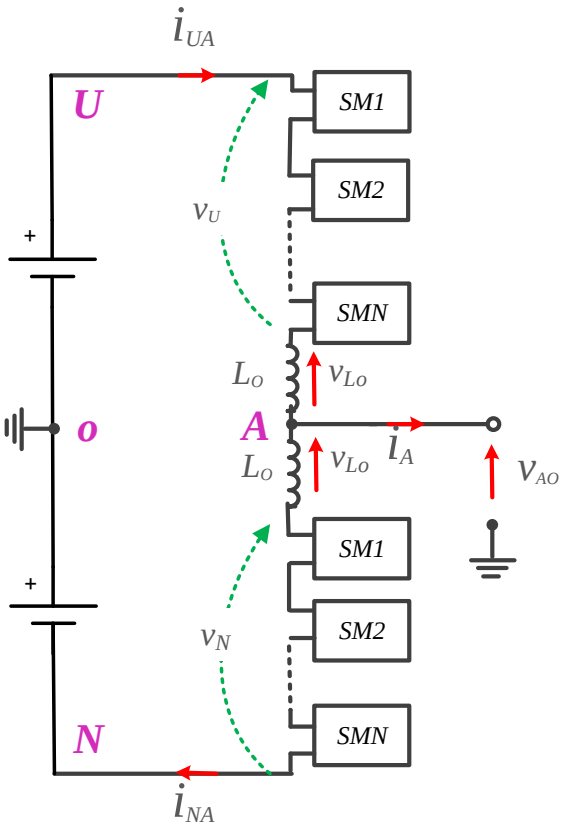


Fig. 3.1: The structure of a modular multilevel converter in a single-phase/half bridge configuration.

A main feature of the MMC is its modular design that uses series connection of the sub-module inverters. The basic building block of the MMC is the inverter sub-module (SM). Different SM inverter configurations can be used [80, 81].

The most frequently used SM inverters are the half-bridge inverter SM (HBSM), the full-bridge inverter SMs (FBSM), and the clamp-diode inverter SM (CDSM). A more detailed description of the topologies is given below.

a) Half-bridge SM (HBSM)

The HBSM is the most popular SM configuration for the MMC due to requirement of only two switches per SM leading to a cheaper and simpler design and control complexity. Fig. 3.2a shows the HBSM configuration. The two switches T_1 and T_2 in the SM are controlled in opposition by a single signal and its complement. The switching states of the HBSM are listed in Table 3.1. When T_2 is on, T_1 has to be off and the SM capacitor is bypassed, and the SM output terminals XY voltage inserted in the arm is zero. If T_2 is off, T_1 is on, therefore the voltage inserted by the SM in the arm is equal to the SM capacitor voltage V_{CSM}. Only during this latter active state, the capacitor gets charged or discharged according to the direction of the arm current. The third state occurs when both T_1 and, T_2 are off and consequently the SM is blocked, and the current can flow only through the freewheeling diodes. In this case the SM output voltage depend on the direction of the arm current, but this state is only used when shutting down the MMC.

HBSM can only generate zero or positive voltage which mean that the HBSM based MMC is unable to deal with a DC-fault (short-circuit between the DC terminals of the MMC's DC-link) [82, 83]. Therefore, fast circuit breakers able to clear DC currents are necessary to isolate the DC-fault. Another limitation is that the peak value of the fundamental output of MMC phase voltage is limited to one half of the total DC-link voltage (step-down operation).

b) Full-bridge SM (FBSM)

The FBSM configuration is shown in Fig. 3.2b, which is built by two legs and each leg has two switches. The two switches on the same leg are controlled in opposition by a single signal and its complement. Therefore, it is required two command signals, one for each leg. The output terminal voltage of the FBSM has three voltage values, positive DC-link voltage $+V_{CSM}$, negative DC-link voltage $-V_{CSM}$ or zero voltage. As the FBSMs can insert both voltage polarities in the arm, the FBSM based MMC has an inherent DC-fault blocking capability

and can block the overcurrent caused by short-circuiting the DC bus powered by the AC source [82, 83]. The FBSM require four IGBTs which is twice compared to the HBSM, which not only increases the converter cost, but also significantly increases the conduction power losses because the SM current flows through two IGBTs instead of only one with the HBSM.

c) Clamp-diode SM

In [82, 84], the use of a clamp-diode SM (CDSM) has been investigated to provide DC-fault blocking capability. The CDSM is formed of two HBSMs, an IGBT and two diodes as shown in Fig. 3.2c. Normally, the switch T_5 is always on and the CDSM is equivalent to two series connected HBSMs. The output voltage states of the CDSM are zero or positive (0, V_{CSM}, and $2V_{CSM}$). Compared with HBSM and FBSM, the CDSM has higher conduction losses than the HBSM and lower than the FBSM and can provide DC-fault blocking capability.

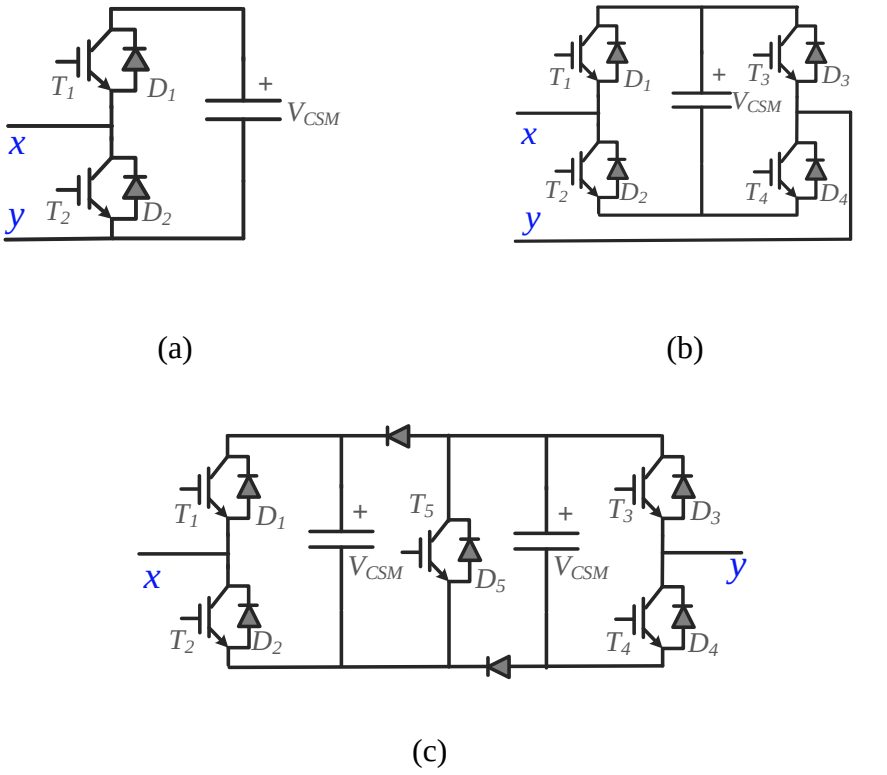


Fig. 3.2: Available SMs configurations: a) HBSM, b) FBSM, and c) CDSM

Table 3.1: Available switching states of the HBSM

SM status	Switching states		V_{XY}	I	Conducting device	Capacitor state
	T_1	T_2				
Bypassed	0	1	0	$+\ X \to Y$	T_2	Bypassed
				$-\ Y \to X$	D_2	Bypassed
Inserted	1	*0*	V_{CSM}	$+\ X \to Y$	D_1	Charging
				$-\ Y \to X$	T_1	discharging
Blocked	0	0	V_{CSM}	$+\ X \to Y$	D_1	Charging
			0	$-\ Y \to X$	D_2	Bypassed

3.2 Features of MMC

The concept and the basic operating principles of the MMC were first proposed by Marquardt *et.al.* [27] in 2003. Since 2010, the MMC has received a significant attention and became one of the most attractive multilevel converter topologies for both medium and high voltage applications [3, 80, 85, 86] due to the ability to extend to any voltage level with low or medium voltage semiconductor devices. The distinct features of the MMC can be summarized as follows:

- Modularity construction and scalability: the converter uses identical inverter sub-modules (SMs). Therefore, more SMs can be added to increase the number of the output voltage levels. Higher voltage and power levels requirements could be achieved by adding additional SMs. Also, the higher the number of SMs, the greater the number of output voltage levels leading to a better output voltage waveform quality. However, this increases the control complexity. Increasing the number of SMs requires more sensors that are necessary to measure the SMs voltages in order to ensure voltage balance between all SMs to make sure operation conditions remain stable. In [87, 88], methods to estimate the SMs voltages have been reported to help reducing the number of required voltage sensors.

- Improved redundancy for SM failure management: the converter redundancy increases with adding spare SMs, where in case of any sub-module failure, a faulty SM can be bypassed and its operation replaced by the spare SM without disrupting the circuit operation [89].
- Lower SM average switching frequency can be used because same PWM voltage quality can be maintained with higher number of voltage levels thanks to increasing the number of SMs within each arm, which results in reduced switching losses due to lower switching voltage and average switching frequency [80].
- Reduced size of the passive filters at the AC side due to enhanced harmonic performance by increasing the number of levels. Elimination of a separate output filter can also be obtained due to the presence of inductors in each arm, needed mostly to limit circulation currents which also limits the output switching current ripple.
- The arms currents are not chopped as they are in a standard voltage source inverter (two-level VSI, NPC, etc): they are flowing continuously (being chopped only inside the SM) and they do not change from positive or negative to zero depending on switching states [80] which helps with reducing EMI and overvoltage that would be generated in long converter arms with significant stray inductance.

3.3 Mathematical model of MMC

Fig. 3.1 illustrates the structure of a single-phase MMC. It is assumed that each SM is based on the half-bridge inverter configuration. In order to simplify the analysis, the series connected SMs in the upper and lower arm are replaced by the controllable voltage sources v_U and v_N respectively.

By applying Kirchhoff's voltage law in Fig. 3.1, the voltage relations of both the upper and lower arm are given by:

$$v_{AO} = v_{UO} - v_U - L_O \frac{di_{UA}}{dt} - r_O i_{UA} \tag{3.1}$$

$$v_{AO} = -v_{ON} + v_N + L_O \frac{di_{NA}}{dt} + r_O i_{NA} \tag{3.2}$$

where i_{UA} and i_{NA} denote the upper and lower arm currents respectively. r_O is the equivalent parasitic resistance of the arm semiconductor devices, cables, and the corresponding arm inductor. v_{Ao} is the AC output voltage, and v_{UO} and v_{ON} are the upper and lower DC-link voltages respectively, all relative to the DC-link mid-point.

Assuming that the direction of the currents is as shown in Fig. 3.1, the AC output current i_{Ao} and the upper and lower arm currents i_{UA} and i_{NA} can be given by:

$$\begin{aligned} i_{AO}(t) &= i_{UA}(t) - i_{NA}(t) \\ i_{UA}(t) &= i_{AO}(t)/2 + i_{cir}(t) \\ i_{NA}(t) &= -i_{AO}(t)/2 + i_{cir}(t) \end{aligned} \tag{3.3}$$

Equation (3.3) indicates that the output current is split simultaneously by the two arms. The arm currents (i_{UA} and i_{NA}) are composed of the AC output current i_{Ao} and the circulating current i_{cir} which flows through the upper and lower arm without affecting the output current. The circulating current i_{cir} contains a DC component I_{UN} that supports the actual power transfer from the MMC's DC source and the DC-links of the SMs and AC components which usually contain low order even harmonics, with the second order harmonic (twice the fundamental frequency) being the dominant one. The large value of the 2nd order harmonic current component will add further current stress and arm losses, which needs to be suppressed. The circulating current i_{cir} and the second order harmonic component i_{2f} can be calculated by:

$$\begin{aligned} i_{cir} &= \frac{i_{UA}(t) + i_{NA}(t)}{2} \\ i_{2f}(t) &= \frac{i_{UA}(t) + i_{NA}(t)}{2} - I_{UN} \end{aligned} \tag{3.4}$$

Adding (3.1) into (3.2) and using (3.3), the AC output voltage is given by:

$$v_{AO}(t) = \frac{v_{UO}(t) - v_{ON}(t)}{2} - \frac{v_U(t) - v_N(t)}{2} - \frac{L_O}{2} \cdot \frac{di_{AO}}{dt} - \frac{r_O}{2} \cdot i_{AO} \tag{3.5}$$

From (3.5), it can be seen that the output AC voltage can be influenced by the difference between the upper and lower DC-link voltages, the difference

between the upper and lower arm voltages and also by the output current that causes a voltage drop on the arm inductance. The voltage drop across the arm inductance will cause a slight variation in the output voltage levels where this part can be completely ignored or removed by using coupled arm inductor configuration [3]. Since L_O and r_O are small, the effect of i_{Ao} on the output voltage can be ignored. Therefore, the AC output voltage v_{Ao} is expressed by:

$$v_{AO}(t) = \frac{v_{UO}(t) - v_{ON}(t)}{2} - \frac{v_U(t) - v_N(t)}{2} \tag{3.6}$$

The DC-link voltages $v_{UO}(t)$ and $v_{ON}(t)$ are generally equal to half of the DC-bus voltage. Therefore, the first term in (3.6) is always zero.

During carrier frequency cycle, the average number of the inserted SMs in MMC leg equals N_{SM} [29]. The average value of the SM capacitor voltage V_{CSM} has to be equal to the DC-link voltage V_{UN} divided by N_{SM} and the voltage in each arm is ranged between 0 and $N_{SM} \cdot V_{CSM}$. Therefore, the peak value of the output voltage is given as:

$$V_m = N_{SM} \cdot V_{CSM} / 2 = V_{UN} / 2 \tag{3.7}$$

From (3.7), the output voltage is limited to half of the DC-link voltage and can only achieve voltage step-down functionality.

Subtracting (3.1) from (3.2) , the voltage across the arm inductor v_{cir}, due to the circulating current i_{cir}, is defined as:

$$v_{cir} = L_o \frac{di_{cir}}{dt} + r_o i_{cir} = \frac{v_{UN}(t)}{2} - \frac{v_U(t) + v_N(t)}{2} \tag{3.8}$$

From (3.8) the voltage across the arm inductor v_{cir} depends on the voltage difference between the DC-link voltage and the sum of the arm voltages and will not affect on the AC output voltage. Therefore, controlling the circulating current in the arm can be implemented by adding or subtracting a voltage v_{cir} to/from both arms. Based on (3.1), (3.2), and (3.8), the upper and lower arm voltages can be defined by:

$$v_U = V_{UO} - v_{AO} - v_{cir} \tag{3.9}$$

$$v_N = V_{ON} + v_{AO} - v_{cir} \tag{3.10}$$

where v_{cir} is used to control the circulating current. Otherwise it is set to zero.

3.4 Modulation techniques for the MMC

Suitable modulation techniques are defined in relation to the required number of SMs for each arm to produce the required arm voltage and consequently the desired output voltage. Modulation techniques that are applicable for multilevel topologies can be applied also to MMC [14, 18, 90]. When the MMC was proposed, the space vector modulation (SVM) technique was used [27]. However, this technique is not normally used with the MMC because its complexity grows with increasing the number of SMs [91, 92]. A review on the used modulation techniques in MMCs has been presented in [78], where the techniques are categorized into low switching frequency and high frequency carrier-based PWM techniques.

Nearest level control (NLC) and selective harmonics elimination (SHE) are low switching frequency techniques that can reduce the switching losses [78, 93]. In the NLC technique, the level index has been taken as the number of inserted SMs in the arm. This technique is simple especially with increasing the number of SMs. However, low order harmonics are generated in the output voltage waveform. The SHE technique can be applied to the MMC and it depends on a predetermined set of turn-on angle of the pulse signals to eliminate the low order harmonics in the output voltage waveform and also to provide capacitor voltage balance.

PWM techniques based on high frequency triangle-wave carrier signals have been adopted for use also with the MMC such as the phase-shifted and level-shifted carrier which are shown in Fig. 3.3 with considering N_{SM} = 4 and the upper and the lower reference signals are normalized and ranged from 0 to N_{SM}. The phase-shifted carrier technique [94] considers N_{SM} phase-shifted carrier signals with a phase displacement between two adjacent carriers of T/N_{SM} (where T is the carrier period) and amplitude of N_{SM}. Using this technique does not

provide a natural balancing between the voltages of the SMs capacitors and a balancing algorithm is required.

The level-shifted carrier technique [95] uses N_{SM} carrier signals which are symmetrically level shifted with respect to y-axis and each carrier signal has amplitude of unity. For the same switching frequency of the phase-shifted technique, the level-shifted technique should have N_{SM} times higher carrier frequency. Depending on the phase shift between the level-shift carriers, the level-shifted carrier technique can be further categorized into:

(1) Phase disposition PWM (PD-PWM)
(2) Phase opposition disposition PWM (POD-PWM)
(3) Alternate phase opposition disposition PWM (APOD-PWM)

The level-shifted technique has some interesting finding when applied with the MMC with using two reference signals for the upper and lower arms [96, 97]. In the case of POD-PWM and APOD-PWM, the total number of inserted SMs in both arms are always equal to N_{SM}. This is leading to N_{SM} + 1 levels in the output voltage waveform with voltage step of V_{DC}/N_{SM}. In the case of PD-PWM, the total number of inserted SMs in both arms are changed between N_{SM} -1, N_{SM} and N_{SM} +1, leading to $2N_{SM}$ + 1 levels in the output voltage waveform with voltage step of $V_{DC}/2N_{SM}$. Hence, the PD-PWM improves the output voltage quality, but it leads to a larger harmonic component in the circulating current. The level shifted-carrier technique produces unequal distribution of switching pulses between sub-modules, which results in SMs capacitor voltage imbalance and a SM capacitor voltage balancing algorithm is required which will be discussed in the next section.

The principle of level-shifted PWM is referred as NLC with PWM (NLC+PWM) which is presented in [98, 99]. In this case, the reference signal is normalized and ranged from 0 to N_{SM}. The integer value of the reference signal is used to indicate the number of SMs that should be inserted, while the fractional value of the reference signal indicates the duty ratio of the SM that performs PWM. In this thesis, the phase-disposition carrier-based PWM (or called NLC+PWM) is applied.

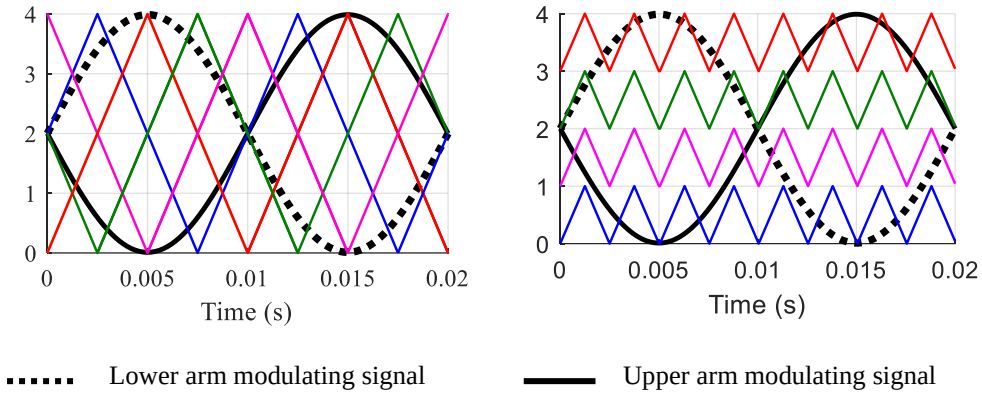


Fig. 3.3: Illustration of how the carrier based modulation techniques with N_{SM} = 4 are implemented for: a) the phase-shifted (PS) and b) the level shifted (PD) techniques

3.5 SMs capacitor voltage balancing mechanism

The MMC requires a voltage balancing strategy to balance and keep the all the sub-modules capacitor voltages at their desired average values. The implementation of voltage balancing strategies depends on the availability of redundant states within the MMC arm [100]. The MMC arm capacitors balancing can be achieved by different strategies [78, 81].

For the level-shift technique, the most widely used balancing strategy is based on the sorting method [95]. The redundant switching state with the strongest effect in facilitating voltage balancing is always selected. Assuming the number of inserted SMs in the upper and lower arm are N_U and N_N respectively, the sorting method can be summarized in four steps as follows:

1) Measure and sort the upper and lower all individual SMs capacitor voltages.
2) If the upper (lower) arm current is positive where current direction shown in Fig. 3.1 is considered as positive, choose the N_U (N_N) SMs with the lowest voltages to be inserted. Therefore, the corresponding cell capacitor is charged, and the voltage increases contributing to reducing the imbalance.
3) If the upper (lower) arm current is negative, choose the N_U (N_N) cell with the highest voltages to be inserted. Therefore, the corresponding cell

capacitor is discharged and the voltage decreases contributing to reducing the imbalance.

It must be mentioned that this sorting method may lead to unnecessary switching transition between the SMs and an increase of the overall switching frequency. If the number of required SMs to be inserted for two consecutive control cycles are the same, the sorting algorithm may choose different SMs to be inserted for the second control period. This results in increased switching transitions and consequently of the switching losses. Various methods have been proposed to reduce the unnecessary switching when using the sorting algorithm, such as a dual sorting algorithm [94].

In order to reduce the unnecessary additional switching, the sorting process is executed every N_{SM} carrier frequency cycles, therefore the sorting frequency is reduced to $f_{sort} = f_c/N_{SM}$. This matches with the equivalent switching frequency for the level-shifted technique. The practical implementation of the sorting algorithm is simple.

3.6 Conclusions

This chapter reviewed operation principles of the MMC and the features as presented in the research literature. The common submodule configurations, which are half-bridge, full-bridge, and clamp-diode inverter SMs were presented with highlighting the advantages and disadvantages of each configuration. The half-bridge SMs based MMC is considered the simplest configuration, but it suffers from the inability to achieve voltage step-up functionality as the output voltage is limited to the DC pole voltage, and the inability to deal with a DC-fault, which require some modifications to the main circuit to overcome these limitations.

The applicable modulation techniques for the MMC were briefly discussed. From the carrier based PWM techniques family, the phase disposition PWM (PD-PWM) has been selected for the work in this thesis due to the high quality of the AC output voltage. To ensure capacitor voltage balance between the sub-modules in each arm, a sorting-based mechanism has been explained. The capacitor voltages in each arm are sorted in ascending or descending order and

based on the arm current polarity and the number of inserted sub-modules needed to generate the desired output voltage, the most charged/discharged SM capacitors are selected to be inserted or bypassed to reduce the voltage imbalance.

Chapter 4
Proposed MMC with Impedance Network

This chapter proposes the integration of the impedance network concept to the HBSM based MMC. The proposed converter has the capability to step-up the voltage (i.e., the output voltage can be more than DC pole voltage). Firstly, the operating principles of the proposed single-phase converter are discussed. Then, two modulation techniques are proposed to operate the converter and are explained in detail. Simulation studies are presented to validate the proposed concepts and show the effectiveness of the proposed modulation techniques in allowing the converter to operate in both voltage buck and voltage boost modes with excellent harmonic performance.

4.1 Impedance network integrated with MMC

The particularities of impedance network based multilevel converters were previously summarized in section 2.2.2. From the different impedance network topologies available, the Z-source and quasi Z-source networks are commonly combined with the multilevel converters [32, 69]. Therefore, these networks are also used in this project to illustrate their integration with the MMC and the other impedance network configurations can be studied in a similar way.

The impedance network with the MMC can be generalized as having two or/and three input terminals and two or/and three output terminals. Fig. 4.1 shows the initial structure of a single-phase Z-source MMC. The Z-source networks (ZS) can be integrated using two networks, as shown in Fig. 4.1 where two ZS networks are inserted with each of the two separate DC input sources, or using a single ZS network as shown in Fig. 4.2.

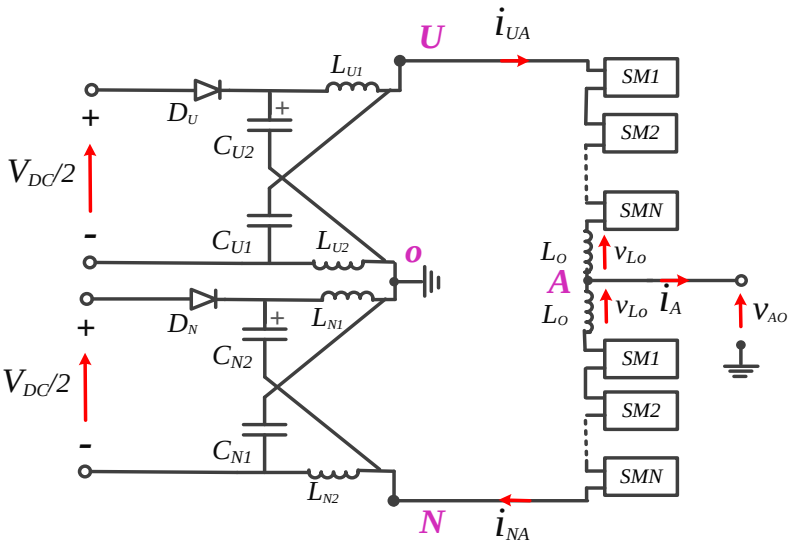


Fig. 4.1: The structure of a Z-source MMC using two ZS-networks

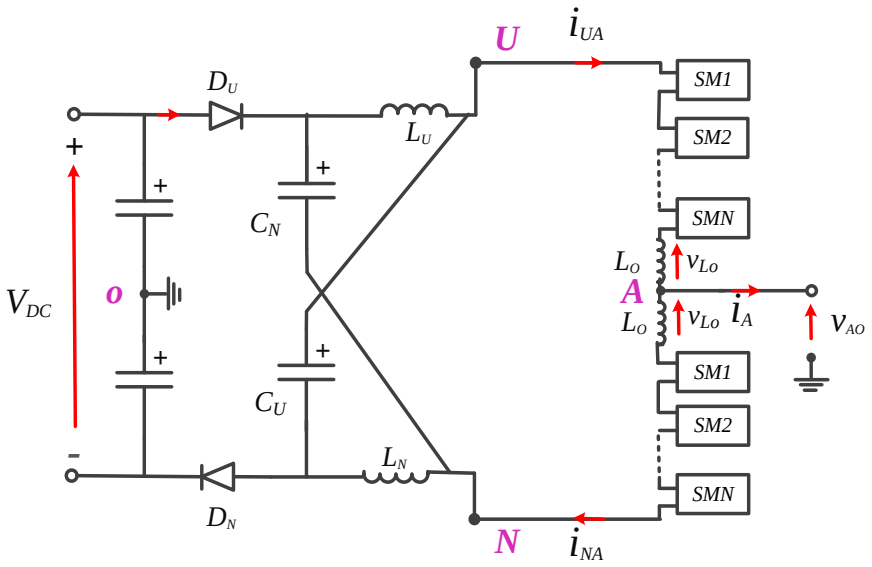


Fig. 4.2: The structure of a Z-source MMC using a single ZS-network

The structure of the quasi Z-source with the MMC is shown in Fig. 4.3. The quasi Z-source (qZS) stage consists of two identical qZS-networks with a single DC input source. The qZS-MMC requires two impedance networks with a single input DC source. The ZS-MMC requires two isolated DC-supplies when using two separate ZS networks or requires one supply with two decoupled capacitors when using a single ZS network as shown in Fig. 4.1 and Fig. 4.2 respectively. The qZS-MMC and ZS-MMC with two ZS networks use the same quantity of passive components but one of the qZS capacitors has a lower voltage stress. The ZS-MMC with one ZS-network requires smaller passive components counts, but their voltage ratings are higher.

Since the qZS impedance network draws a continuous input current [43] and therefore lowering the source current stress and filtering requirements, the qZS-network is applicable for various applications [38, 67] such as renewable power and electric vehicles. As a result, this chapter investigates the operation of the MMC when integrated with the qZS-network.

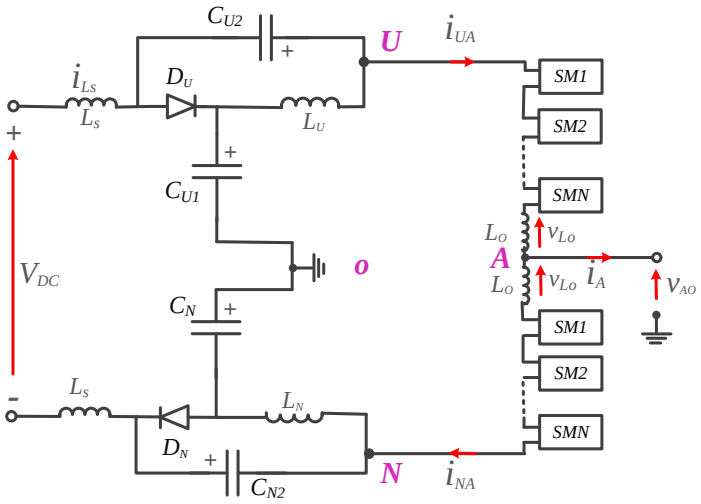


Fig. 4.3: The initial structure of a quasi Z-source MMC network

4.2 The quasi Z-source MMC

The proposed structure for a single-phase qZS-MMC is shown in Fig. 4.4. The MMC leg consists of the upper and the lower arms. Each arm is formed by N_{SM} series-connected identical sub-modules (SMs), and an arm inductor (L_O). Each SM is based on a half-bridge inverter configuration with one DC-link floating capacitor. The quasi Z-source (qZS) stage consists of two identical qZS-networks which are inserted between the DC source (V_{DC}) and the MMC leg. The two networks share a midpoint node "*O*" between the two capacitors C_{U1}, C_{N1} that can be used as a reference point for the definition of the output voltage v_{Ao} and also a return point for the load current.

Similar to impedance-network circuits, the operation of the qZS-network requires the introduction of a short circuit (shoot-through) at its output terminals in order to increase currents and consequently the energy stored in the qZS-network inductors which is later transferred to the qZS-network capacitors. This increase in the stored energy provides the converter's voltage boosting capability [32, 43].

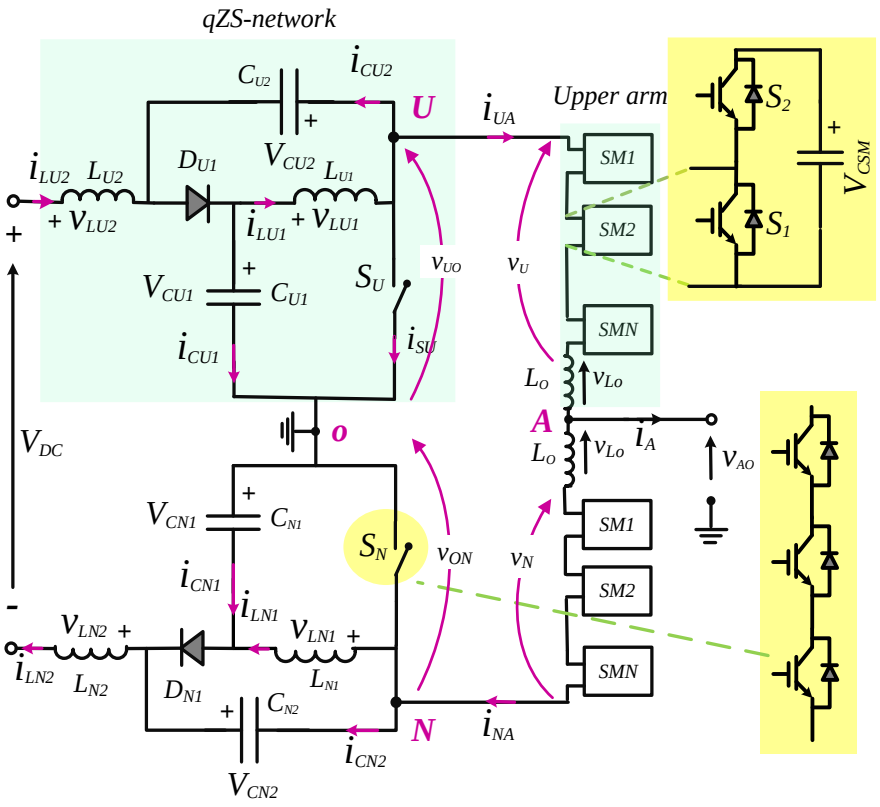


Fig. 4.4: The structure of a single-phase quasi Z-source MMC

It is not possible to use the MMC leg to produce the shoot-through by bypassing all the SMs in both the upper and lower arm due to presence of the arm inductors in the path of shoot-through current as the shoot-through path should have a low inductance. Even with the assumption that the arm inductors could be removed, bypassing all the SMs would lead to a drop in upper and lower arm voltage levels to zero, which would cause a significant temporary loss of voltage leading to high distortion in the output voltage and the benefit of having a multilevel functionality will be compromised. To avoid this problem, two chain-links of series connected switches S_U and S_N each able to handle half the DC-link voltage are connected at the upper and lower qZS-networks end-terminals respectively to provide shoot-through current path to the DC-link midpoint "*O*" as shown in Fig. 4.4. The number of the series switches in each chain-link is at least equal to half the number of SMs in each arm, assuming an equal voltage rating with the SMs switches. The actual number of the series switches needed in each chain-link will be discussed later.

Generally, there are two operation modes for the qZS-network. Considering the upper qZS-network which is shown in Fig. 4.5a, the operation modes are:

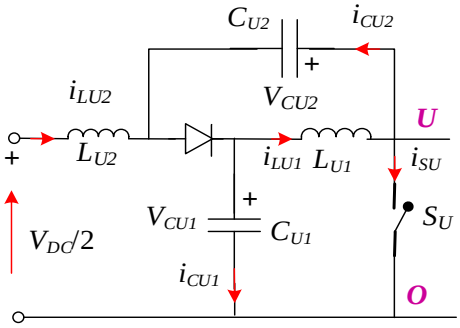
1) Shoot-through (ST) mode: The upper DC-link terminals are shorted, which forces the series diode to become reverse biased as shown in Fig. 4.5b. Therefore, the stored energy in the capacitors begins to transfer to the inductors causing the capacitor voltage to decrease and the inductor current to increase. The equations for the upper and the lower qZS networks during ST mode are:

$$\left.\begin{aligned} v_{LU1}(t) &= V_{CU1} \\ v_{UO}(t) &= 0 \end{aligned}\right\} \quad @\ S_U \text{ ON}$$
$$\left.\begin{aligned} v_{LN1}(t) &= V_{CN1} \\ v_{NO}(t) &= 0 \end{aligned}\right\} \quad @\ S_N \text{ ON} \qquad (4.1)$$

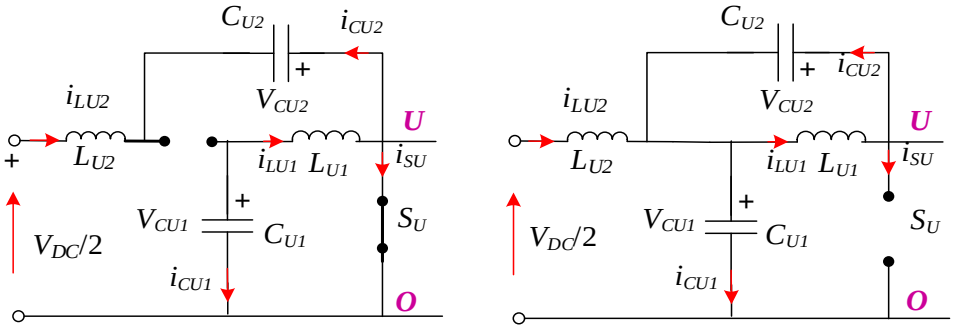
2) Non-shoot-through (NST) mode: The qZS-network is connected to an inversion stage. Therefore, the series diode will be forward biased as shown in Fig. 4.5c. The stored energy in the inductors begins to transfer to the load,

and the qZS capacitors begin to charge causing the capacitor voltage to increase and inductor current to decrease.

$$\left.\begin{aligned} v_{LU1}(t) &= -V_{CU2} \\ v_{UO}(t) &= V_{CU1} + V_{CU2} \end{aligned}\right\} \quad @\ S_U \text{ OFF}$$
$$\left.\begin{aligned} v_{LN1}(t) &= -V_{CN2} \\ v_{NO}(t) &= V_{CN1} + V_{CN2} \end{aligned}\right\} \quad @\ S_N \text{ OFF} \qquad (4.2)$$



(a)



(b) (c)

Fig. 4.5: Upper qZS-network operation modes: a) upper qZS-network, b) shoot-through mode and c) non-shoot-through mode

The source inductors' voltages (v_{LU2} for upper qZS-network and v_{LN2} for lower qZS-network) depend on the state of the upper and lower chain-link switches S_U and S_N, where there are four different cases which are defined by (4.3).

$$v_{LU2}(t) = v_{LN2}(t) = \begin{cases} (V_{DC} + V_{CU2} + V_{CN2})/2 & S_U \text{ ON}, \ S_N \text{ ON} \\ (V_{DC} + V_{CU2} - V_{CN1})/2 & S_U \text{ ON}, \ S_N \text{ OFF} \\ (V_{DC} - V_{CU1} + V_{CN2})/2 & S_U \text{ OFF}, \ S_N \text{ ON} \\ (V_{DC} - V_{CU1} - V_{CN1})/2 & S_U \text{ OFF}, \ S_N \text{ OFF} \end{cases} \quad (4.3)$$

The converter switching period T can be expressed by $T=T_{sh}+T_n$, where T_{sh} is the shoot-through interval, and T_n is the non-shoot-through interval. Let D_{sh} and D_n are the ST and NST duty ratios respectively defined by:

$$D_{sh} = T_{sh}/T \qquad D_n = T_n/T \quad (4.4)$$

Since the upper and lower sections of the qZS network is symmetric, the following pairs of passive components are assumed identical: $C_{U1} = C_{N1} = C_1$, $C_{U2} = C_{N2} = C_2$, $L_{U1} = L_{N1} = L_{U2} = L_{N2} = L$ and consequently the capacitor voltages and inductor currents have their average value where $v_{CU1} = v_{CN1} = V_{C1}$, $v_{CU2} = v_{CN2} = V_{C2}$ and $i_{LU1} = i_{LU2} = i_{LN1} = i_{LN2} = I_L$. At steady state, the average value of the inductors voltage over one switching period equals to zero. The qZS-network capacitor average voltages V_{C1} and V_{C2} are given by (4.5). The peak value of the DC-link voltages during NST mode, V_{UO}, V_{ON} and V_{UN} are given by (4.6).

$$V_{C1} = \frac{1 - D_{sh}}{1 - 2D_{sh}} V_{DC}/2$$
$$V_{C2} = \frac{D_{sh}}{1 - 2D_{sh}} V_{DC}/2 \quad (4.5)$$

$$V_{UO} = V_{ON} = V_{UN}/2 = \frac{1}{1 - 2D_{sh}} V_{DC}/2 \quad (4.6)$$

As previously explained, in the ST mode, the stored energy in the qZS-capacitors begins to transfer to inductors which causes the inductor currents to increase and capacitor voltages to decrease. Whereas in the NST mode, the capacitors are not only charging but also, they may be discharging depending on the value of the corresponding arm current relative to the inductor current. To illustrate this, let's consider the current direction as shown in Fig. 4.4 and that the qZS-inductor

currents have their average value I_L, the qZS capacitor current i_{CU1} during ST and NST modes is defined by (4.7) and (4.8) respectively. During NST mode, the capacitors are charging/discharging if the instantaneous value of i_{UA} is higher/lower than I_L.

$$i_{CU1}(t) = I_L \tag{4.7}$$

$$i_{CU1}(t) = i_{UA}(t) - I_L \tag{4.8}$$

It is worth noting that during these switching modes of ST or NST, the SM capacitors are charging or discharging depending only on the polarity of arm current, where the SMs capacitor voltage decreases/increases when the corresponding arm current is negative/positive regardless of the switching modes [86].

4.3 Modulation techniques for qZS-MMC

This section describes the proposed modulation schemes for the single-phase qZS-MMC. The following assumptions were made when analysing the operating principles of the qZS-MMC:

- The qZS-MMC operates in inversion mode.
- The SMs capacitor voltages in each arm are well balanced using the sorting algorithm discussed in section 3.5.
- The AC-circulating current is suppressed at a negligible level, which will be discussed later in this chapter.
- The power losses of the converter are ignored, and the voltage drop across the resistance of the inductors and semiconductor devices are neglected.

In this study, the phase disposition (PD) carrier technique is employed for the MMC [95] with two opposite reference modulating signals for both the upper and the lower arm SMs. Assuming N_{SM} sub-modules are used per arm, N_{SM} level-shifted carriers are required and consequently, a ($2N_{SM}$ +1) level waveform is generated on the output. Each carrier signal is responsible for producing the gating signals of two SMs, one from upper arm and one from lower arm, which

are chosen according to a capacitor voltage balance algorithm (section 3.5). The PWM level shifted modulation technique (i.e. PD-PWM) at N_{SM} = 4 is shown in Fig. 4.6.

Through a switching (i.e. carrier) frequency period, the total number of inserted SMs in the phase-leg are changed between N_{SM} -1, N_{SM} and N_{SM} +1 with total average of N_{SM}, hence:

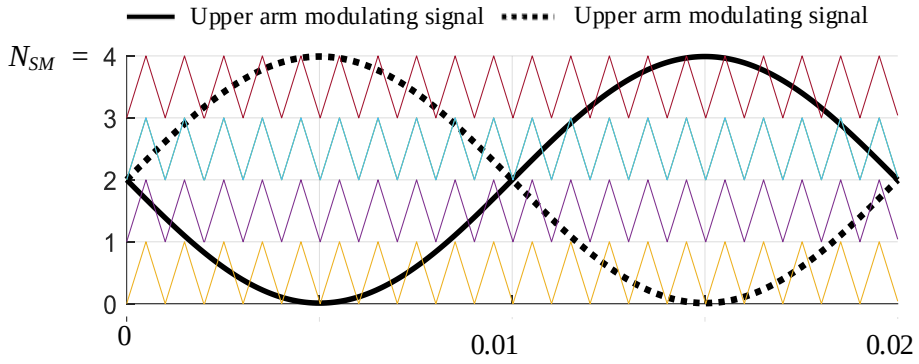


Fig. 4.6: PWM level shifted modulation technique: the upper and lower modulating signals with level-shifted carriers at N_{SM} = 4

$$v_U(t) + v_N(t) = N_{SM} \cdot V_{CSM} \tag{4.9}$$

From (3.6), the instantaneous value of the output voltage potential $v_{AO}$with reference to midpoint "O" is reliant on the upper and lower DC-link voltage potentials (v_{UO} and v_{ON}) and the voltage generated by each arm (v_U and v_N). In traditional MMC, the DC-link voltage potentials v_{UO} and v_{ON} are generally equal to half the DC source voltage V_{DC}/2, which means that the first term in (3.6), is always zero. In a qZS-MMC, the operation of each of the chain-link switches (S_U and S_N) alone will cause the first term in (3.6) having a value of equals to half the DC-link voltage V_{UN}/2, that will seriously disturb the output voltage v_{AO}. One way to avoid this disturbance is by firing both chain-link switches simultaneously (S_U and S_N). Therefore, the first term in (3.6) becomes zero. In the thesis, the proposed modulation based on this mechanism is referred to as the "simultaneously shorted (SS)" modulation technique and is explained in detail in the section 4.3.1.

Another option to compensate for the disturbance caused by turning on one of the chain-links is by having the arm generating an adapted voltage to compensate for the disturbance in the output voltage as suggested in (3.6). This principle can be implemented by changing the number of the inserted SMs in the corresponding arm and the proposed modulation that uses this technique is referred to as the "reduced inserted cells (RICs)" modulation technique.

4.3.1 Simultaneously shorted (SS) modulation technique

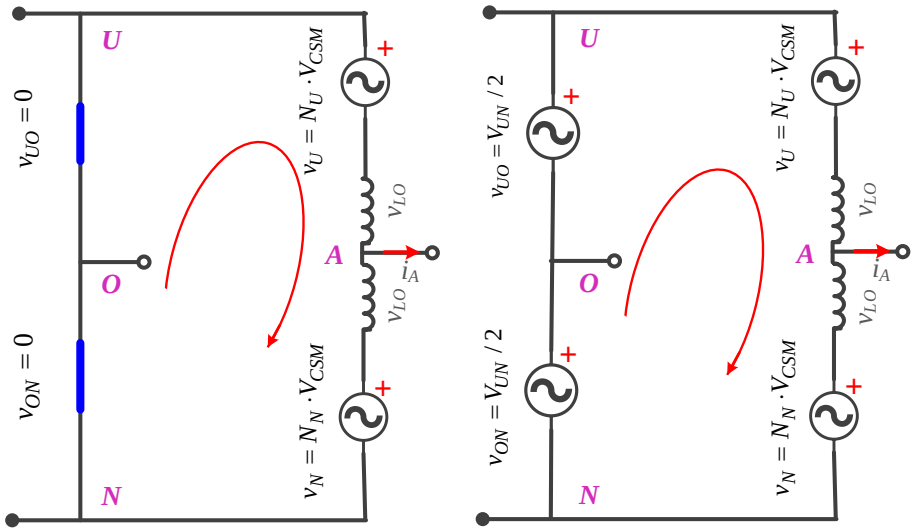
If only one of the chain-link switches (S_U , S_N) is turned on alone, the first term in (3.6) will become high having a value of half the DC-link voltage and then the output voltage v_{AO} will be extremely disturbed. One way to avoid this disturbance is for both chain-links switches to be fired simultaneously, resulting in zero voltage of the first term in (3.6).

In this technique, the upper and lower chain-links S_U and S_N are simultaneously fired and both the upper and lower qZS-networks operate in full ST mode. Consequently, the upper and the lower DC-link voltages v_{UO} and v_{ON} have a zero potential $v_{UO} = v_{ON} = 0$, leading to a zero dc-link seen by the inversion stage, that lowers the maximum voltage that can be produced on the output. Also, considering that both upper and lower qZS-networks operate in NST mode, the upper DC-link voltage v_{UO} will be equal to the lower DC-link voltage v_{ON} and both equal to $v_{UN} / 2$ as given in (4.6). This means that the first term in (3.6) in both ST and NST modes is zero. The equivalent circuits seen from the MMC side during ST and NST modes for this particular case are shown in Fig. 4.7a and Fig. 4.7b respectively.

The switching signals can be simply achieved by comparing the triangle carrier signal with an upper and lower shoot-through modulating signals $v_{sh\text{-}U}$ and $v_{sh\text{-}N}$ of level D_{sh} proportional with the desired ST duty cycle as shown in Fig. 4.8 where the upper and the lower chain-link switches S_U and S_N are gated by using identical pulse signals. The upper and lower arm inductor voltages in ST and NST modes respectively can be expressed by:

$$v_{LO}(t) = \begin{cases} -\dfrac{v_U(t)+v_N(t)}{2} & \text{if } S_U \ \& \ S_N \quad \text{ON} \\ \dfrac{v_{UO}(t)+v_{ON}(t)}{2} - \dfrac{v_U(t)+v_N(t)}{2} & \text{if } S_U \ \& \ S_N \quad \text{OFF} \end{cases} \tag{4.10}$$

Due to the assumption that the average current in the inductor remains the same, the average voltage across the arm inductor over the switching period is equal to zero and is given by (4.11).



(a) (b)

Fig. 4.7: Equivalent circuit when using simultaneously shorted (SS) technique during the: (a) ST and (b) NST modes

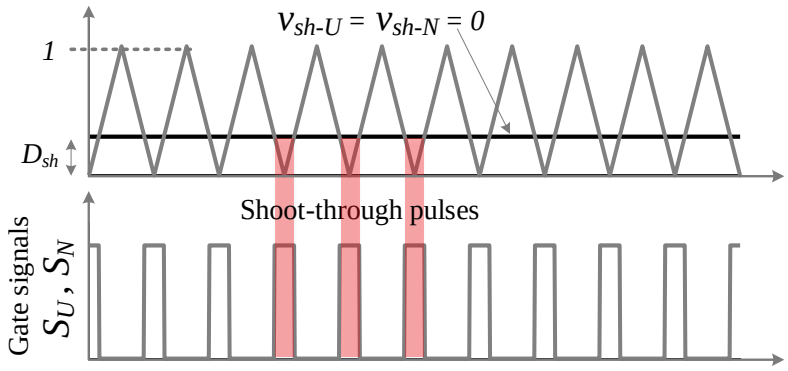


Fig. 4.8: Generation of switching signals for the simultaneously shorted (SS) technique

$$\begin{aligned} v_{LO}(t) = & -\frac{v_U(t)+v_N(t)}{2}\cdot D_{sh} \\ & +\left[\frac{v_{UO}(t)+v_{ON}(t)}{2}-\frac{v_U(t)+v_N(t)}{2}\right]\cdot(1-D_{sh})=0 \end{aligned} \tag{4.11}$$

Substituting by (4.6) and (4.9) into (4.11), the SMs capacitor voltage is given by (4.12).

$$V_{CSM} = (1-D_{sh})\times\frac{V_{UN}}{N_{SM}} = \frac{(1-D_{sh})}{(1-2D_{sh})}\times\frac{V_{DC}}{N_{SM}} \tag{4.12}$$

From (4.12), it is noted that the SM capacitor voltage V_{CSM} has to be equal to the average value of the DC-link voltage divided by N_{SM}. Consequently, the peak of the fundamental phase voltage V_m can be expressed by:

$$\begin{aligned} V_m = & \frac{m\cdot N_{SM}\cdot V_{CSM}}{2} \\ & = \frac{m\cdot(1-D_{sh})}{(1-2D_{sh})}\times\frac{V_{DC}}{2} = m\cdot G\times\frac{V_{DC}}{2} \end{aligned} \tag{4.13}$$

where m is converter modulation index and G is the converter voltage gain which is the ratio of V_m to $V_{DC}/2$ at $m = 1$ and is defined by (4.14) when using the SS technique:

$$G = \frac{(1-D_{sh})}{(1-2D_{sh})} \tag{4.14}$$

Assuming that the converter is able to generate a sinusoidal voltage that results in a sinusoidal current, the AC output voltage and current can be expressed by:

$$\begin{aligned} v_{AO}(t) &= V_m \sin\omega\cdot t \\ i_{AO}(t) &= I_m \sin(\omega\cdot t-\varphi) \end{aligned} \tag{4.15}$$

where φ is the phase shift between the output voltage waveform v_{AO} and current waveform i_{AO}, I_m is the peak value of the fundamental phase current, and $\omega = 2\cdot\pi\cdot f$ is the fundamental output angular frequency, corresponding to the output frequency f.

The actual upper and lower arm voltages consist of a DC voltage component (which equals to one half of the average value of the DC-link voltage) and AC voltage component (which equals to peak fundamental voltage), can be expressed by (4.16).

$$v_U(t) = \frac{(1-D_{sh})\cdot V_{UN}}{2}\cdot(1-m\cdot\sin\omega\cdot t)$$
$$v_N(t) = \frac{(1-D_{sh})\cdot V_{UN}}{2}\cdot(1+m\cdot\sin\omega\cdot t) \quad (4.16)$$

Neglecting the converter power losses, the input power $P_{DC} = V_{DC}\, I_L$ equals to the DC-link power which is the product of the DC component in the DC-link current (i.e., arm current) I_{UN} and the DC component in the DC-link voltage (1-D_{sh}) V_{UN}, and also equal to the load active power.

$$P_{DC} = V_{DC}\cdot I_L = (1-D_{sh})\cdot V_{UN}\cdot I_{UN} = \frac{V_m\cdot I_m}{2}\times\cos\varphi \quad (4.17)$$

Substituting from (4.6) and (4.13) into (4.17), the DC component in the arm current I_{UN} and the average value of the qZS-inductor current I_L can be expressed by:

$$I_{UN} = \frac{m\cdot\cos\varphi\cdot I_m}{4}$$
$$I_L = \frac{m\cdot(1-D_{sh})\cdot\cos\varphi\cdot I_m}{4\cdot(1-2D_{sh})} \quad (4.18)$$

Assuming that a suitable controller is used that is able to make sure that the low order even harmonic in the circulating current is kept at negligible level. Substituting (3.4) and (4.18) into (3.3), the current through the upper and lower arm can be expressed by:

$$i_{UA}(t) = \frac{m\cdot\cos(\varphi)\cdot I_m}{4} + \frac{I_m}{2}\cdot\sin(\omega\cdot t-\varphi)$$
$$i_{NA}(t) = \frac{m\cdot\cos(\varphi)\cdot I_m}{4} - \frac{I_m}{2}\cdot\sin(\omega\cdot t-\varphi) \quad (4.19)$$

Based on voltage and current relations deduced in this section for the SS technique and in the next section for the RICs technique, the components sizing, and converter losses will be estimated later in this chapter. Using the SS technique, the chain-link switches are subjected to a high voltage stress especially with increasing the converter voltage gain. The reason is that the SMs capacitor voltages which is defined in (4.12) have to be charged according to the average value of the DC-link voltage. Consequently, using (3.6) results in the output voltage is also generated according to the average value of the DC-link voltage and does not depends on the peak value of the DC-link voltage as given in (4.20). This means that a high voltage stress results across the chain-link switches for a given output voltage level.

$$V_m = m \cdot (1 - D_{sh}) \cdot \frac{V_{UN}}{2} \tag{4.20}$$

4.3.2 Reduced inserted cells (RICs) modulation technique

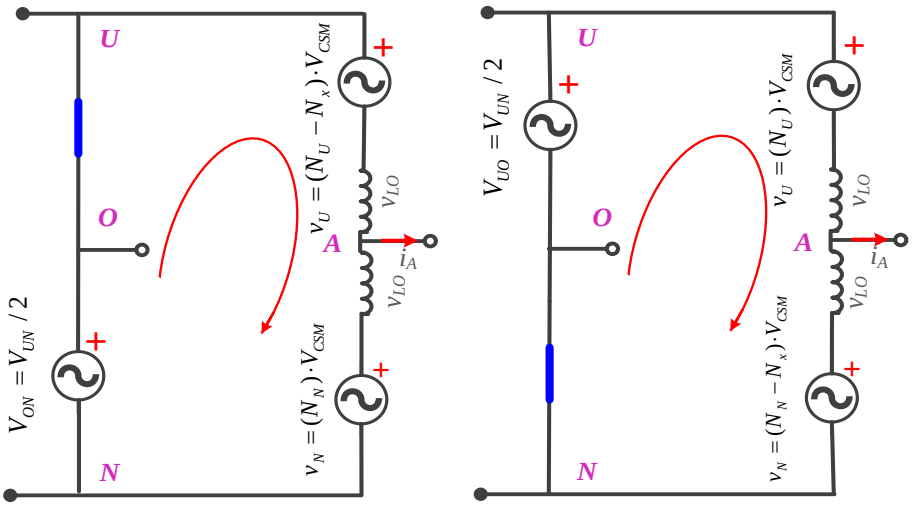
The previous section illustrated the SS technique that is ST simultaneously by turning on the upper and lower chain-link switches together. However, a high voltage stress of the chain-link switches appears. The concept of introducing individual shoot-through by gating only one of the upper or the lower chain-links will create a significant change in the output voltage where its magnitude will change by value of half of the DC-link voltage, which reflects on the corresponding level number to change by N_{SM} /2 step. To compensate for this, the corresponding arm voltage needs to be simultaneously changed to compensate for the asymmetric shorting of half of the DC-link voltage.

Firstly, the analysis can be derived by realizing that the SMs capacitors are charged according to the peak value of the DC-link voltage V_{UN} / N_{SM}.

$$V_{CSM} = V_{UN} / N_{SM} \tag{4.21}$$

This can be explained by considering the case of turning on the upper chain-link switches which will cause the overall DC-link voltage to drop to half. To compensate for the change in the output voltage, the number of inserted SMs in

the upper arm needs to be changed by N_X where N_X is the number of SMs that should be bypassed from the arm. The corresponding equivalent circuits during a partial ST shown for both cases of ST in both the upper and lower qZS-networks are shown in Fig. 4.9a and Fig. 4.9b respectively, while Fig. 4.7b shows the equivalent circuit during NST mode.



(a) (b)

Fig. 4.9: Equivalent circuit when using reduced inserted cells (RICs) technique during ST mode for, (a) upper and (b) lower qZS-networks

Applying Kirchhoff's voltage law, the arm inductor voltage v_{LO} in ST and NST modes can be expressed by:

$$v_{LO}(t) = \begin{cases} -(N_U + N_N - N_X)\cdot V_{CSM} + \dfrac{V_{UN}}{2} & \text{if } S_U \text{ or } S_N \quad \text{ON} \\ \dfrac{v_{UO}(t) + v_{ON}(t)}{2} - \dfrac{v_U(t) + v_N(t)}{2} & \text{if } S_U \ \&\ S_N \quad \text{OFF} \end{cases} \tag{4.22}$$

where N_U and N_N are the number of inserted SMs in the upper and the lower arms respectively with $N_U + N_N = N_{SM}$. Considering that the average inductor voltage over the switching period is equal to zero and is given by:

$$\begin{aligned} v_{LO}(t) = &\left[(N_U + N_N - N_X)\cdot V_{CSM} - \frac{V_{UN}}{2}\right]\cdot D_{sh} \\ &+ \left[\frac{v_{UO}(t) + v_{ON}(t)}{2} - \frac{v_U(t) + v_N(t)}{2}\right]\cdot(1 - D_{sh}) = 0 \end{aligned} \tag{4.23}$$

Using (4.9) and (4.23), the number of SMs N_X that should be bypassed from the upper arm or the lower arm to compensate for the asymmetry caused by a partial ST, is given by:

$$N_X = N_{SM} / 2 \tag{4.24}$$

As the available DC-link voltage halves, the number of inserted SMs per leg should also be reduced by $N_{SM}/2$ during upper or lower DC-link ST mode, which makes the SMs capacitor to charge according to the peak value of the available DC-link voltage V_{UN} / N_{SM} as identified previously. To avoid distortion of the output voltage, if the upper chain-link switches are performing a shooting-through, $N_{SM}/2$ SMs that were initially turned on from the upper arm, should be selected to be bypassed and similarly, a same number needs to be bypassed in case of shooting-through the lower chain-link switches. Therefore, in order to introduce the ST signals to either the upper or lower qZS-network, the upper or lower arm should have at least $N_{SM}/2$ inserted SMs.

As shown in Fig. 4.10, for N_{SM} = 4 sub-modules per arm, 4 level-shifted carriers are required and consequently, a 5-level waveform is generated on the upper and lower arm and a 9-level waveform is generated on the output voltage [78].

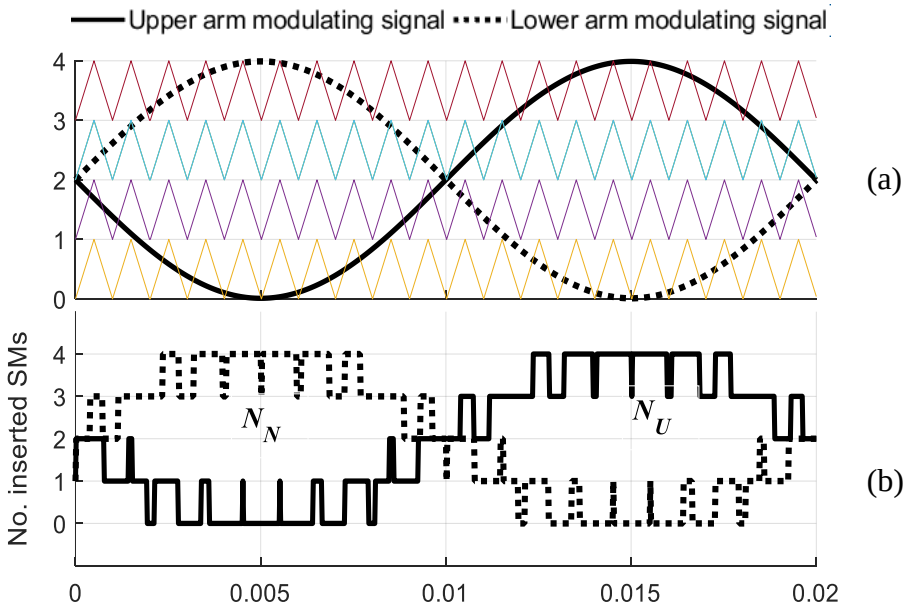


Fig. 4.10: Illustrating the PWM level shifted modulation technique: a) the upper and lower modulating signals with level-shifted triangles and b) the number of inserted cell for the upper and lower arm (bottom)

It is clear that, during the second half-cycle of the upper arm modulating signal (i.e. the negative half cycle of the output voltage), the number of upper inserted SMs N_U is greater than or equal to N_{SM} /2. While during the first half-cycle of the lower arm modulating signal (i.e. the positive half cycle of the output voltage), the number of lower inserted cells N_N is greater than or equal to N_{SM} /2. Hence, the upper chain-link switches can be turned on during the negative half cycle of the output voltage, and the lower chain-link switches can be turned on during the positive half cycle of the output voltage.

Considering that the ST carrier has a unity height and is in-phase with level-shifted carriers as shown in Fig. 4.11a, the ST reference signals for the upper and the lower arms ($v_{sh\text{-}U}$ and $v_{sh\text{-}N}$) can be defined by:

$$v_{sh-U} = \begin{cases} 0 & \rightarrow \quad 0:\pi \\ 2D_{sh} & \rightarrow \quad \pi:2\pi \end{cases}$$
$$v_{sh-N} = \begin{cases} 2D_{sh} & \rightarrow \quad 0:\pi \\ 0 & \rightarrow \quad \pi:2\pi \end{cases} \tag{4.25}$$

To avoid any distortion in the output voltage, the ST modulating signal for the upper chain-link switches is set to zero in the first half cycle, while the ST modulating signal for the lower chain-link switches is set to zero in the second half cycle, as illustrated in (4.25). In addition, to attain the average ST duty ratio over one output frequency period to be D_{sh}, the height of ST modulating signals should be equal to $2D_{sh}$. The ST modulating signals, and the resultant ST pulses are shown in Fig. 4.11a, and Fig. 4.11b. The modified upper and lower arm modulation signals are shown in Fig. 4.11c where during the ST intervals, the amplitude of original modulating signals is level-shifted by N_{SM} /2 units of the SMs carrier.

As a result, the upper and the lower arm voltages have DC and fundamental frequency components. By using Fourier series, the upper and the lower arm voltages can be expressed by (4.26). The upper and the lower DC-link voltages shown in Fig. 4.11d have DC and AC fundamental components. The DC-link voltage can be expressed by (4.27).

$$v_U = (1-D_{sh})\cdot\frac{V_{UN}}{2} - (m-\frac{4\cdot D_{sh}}{\pi})\cdot\frac{V_{UN}}{2}\cdot\sin\omega\cdot t \tag{4.26}$$

$$v_N = (1-D_{sh})\cdot\frac{V_{UN}}{2} + (m-\frac{4\cdot D_{sh}}{\pi})\cdot\frac{V_{UN}}{2}\cdot\sin\omega\cdot t$$

$$v_{UO} = (1-D_{sh})\cdot\frac{V_{UN}}{2} + \frac{4\cdot D_{sh}}{\pi}\cdot\frac{V_{UN}}{2}\cdot\sin\omega\cdot t \tag{4.27}$$

$$v_{ON} = (1-D_{sh})\cdot\frac{V_{UN}}{2} - \frac{4\cdot D_{sh}}{\pi}\cdot\frac{V_{UN}}{2}\cdot\sin\omega\cdot t$$

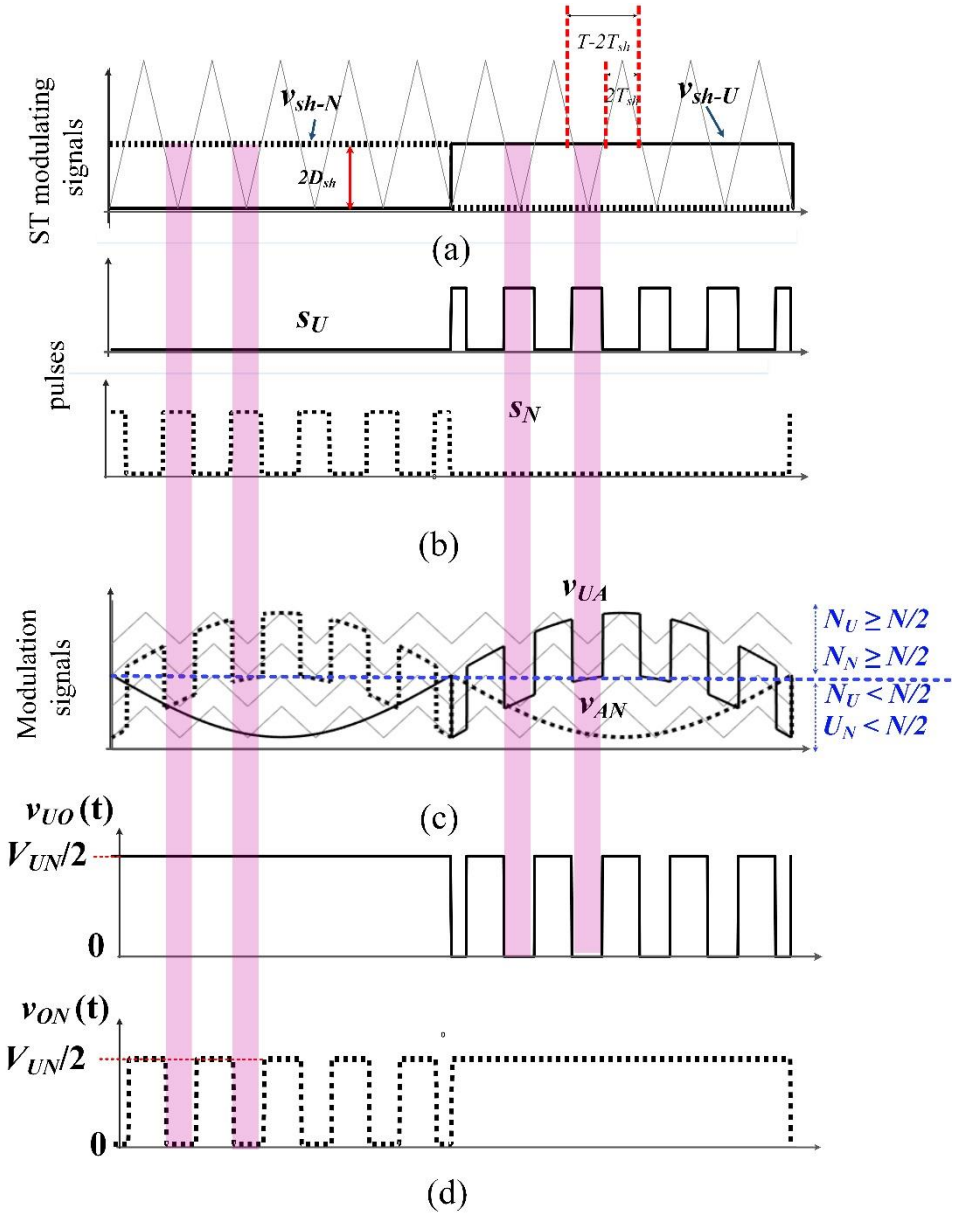


Fig. 4.11: Illustration of how the RICs modulation technique waveforms regenerated: a) shoot-through modulation signals, b) modified modulation signal, c) chain-link switches pulses, and d) the upper and the lower DC-link voltages

The Fourier series of the upper and the lower arm voltages in (4.26) and the DC-link voltages in (4.27) have been derived in Appendix A and only the final equations are presented here.

From (4.6), (4.26) and (4.27) and also applying Kirchhoff's voltage law, the peak value of the fundamental output phase voltage can be expressed by:

$$V_m = m \cdot \frac{V_{UN}}{2} = \frac{m}{(1-2 \cdot D_{sh})} \cdot \frac{V_{DC}}{2} = m \cdot G \cdot \frac{V_{DC}}{2} \tag{4.28}$$

where G is the converter gain and is defined by (4.29) in case of using the RICs technique:

$$G = \frac{1}{(1-2D_{sh})} \tag{4.29}$$

From (4.28), the peak value of the fundamental output phase voltage is equal to half of the peak value of the DC-link voltage $V_{UN}/2$ at m = 1. From (3.3) and (4.27), it is found that the upper and the lower DC-link voltages and the upper and the lower arm currents have a constant DC component and also an AC component at the fundamental frequency. Therefore, the DC-link active power is given by:

$$P_{UN} = (1-D_{sh}) \cdot V_{UN} \cdot I_{UN} + \frac{D_{sh}}{\pi} \cdot V_{UN} \cdot I_m \cdot \cos(\varphi) \tag{4.30}$$

where the first term in (4.30) is generated from the product of the DC components of the DC-link current (arm current) I_{UN} and the average of the total DC-link voltage. The second term is the product of the fundamental component of the arm current (3.3) and the fundamental component of DC-link voltage in both upper and lower DC-link voltages (4.27). According to the power conservation law, the input power from the DC-source $P_{DC} = V_{DC} \cdot I_L$ equals the DC-link power P_{UN} (4.30) and both are equal to the load active power when ignoring the converter losses, as illustrated in (4.31).

$$P_{DC} = P_{UN} = \frac{V_m \cdot I_m}{2} \cdot \cos(\varphi) \tag{4.31}$$

From (4.6), (4.30) and (4.31), the DC component in the arm current I_{UN} and the average value of the qZS-inductor current I_L when using the RICs technique are determined as:

$$I_{UN} = \frac{m_{RIC} \cdot \cos(\varphi) \cdot I_m}{4}$$
$$I_L = \frac{m \cdot \cos(\varphi) \cdot I_m}{4 \cdot (1 - 2D_{sh})} \tag{4.32}$$

where

$$m_{RIC} = \frac{m - 4 \cdot D_{sh} / \pi}{1 - D_{sh}} = \frac{2 \cdot m \cdot G - 4 \cdot (G-1) / \pi}{G+1} \tag{4.33}$$

Assuming that the low order even harmonic in the circulating current is kept at negligible level and substituting (3.4) and (4.32) into (3.3), the current through the upper and lower arm can be expressed by:

$$i_{UA}(t) = \frac{m_{RIC} \cdot \cos(\varphi) \cdot I_m}{4} + \frac{I_m}{2} \cdot \sin(\omega \cdot t - \varphi)$$
$$i_{NA}(t) = \frac{m_{RIC} \cdot \cos(\varphi) \cdot I_m}{4} - \frac{I_m}{2} \cdot \sin(\omega \cdot t - \varphi) \tag{4.34}$$

In this modulation technique, the SMs capacitors (4.21) are charged according to the peak value of the DC-link voltage, while they are charged according to the average value when using SS technique (4.12). Using (4.6), (4.14), and (4.29), the peak value of the DC-link voltage V_{UN} is defined for the SS and the RICs techniques by (4.35) and (4.36) respectively.

$$V_{UN} = (2G - 1) \cdot \frac{V_{DC}}{2} \tag{4.35}$$

$$V_{UN} = G \cdot \frac{V_{DC}}{2} \tag{4.36}$$

The peak value of the DC-link voltage V_{UN} presents the voltage stress V_S seen by the chain-link switches. Fig. 4.12 shows the normalized voltage stress $V_S/(V_{DC}/2)$ versus the gain G. It is noted that the voltage stress is increasing when increasing

the gain and becomes lower when using the RICs technique compared to the SS technique for the same gain *G*.

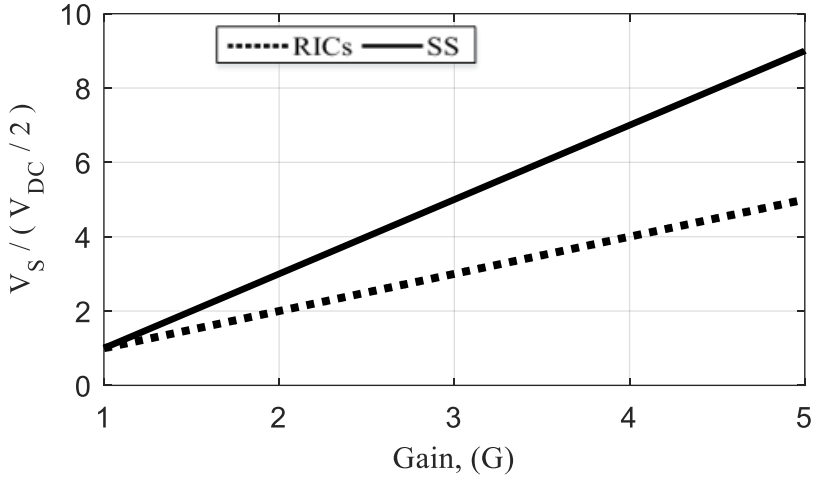


Fig. 4.12: The normalized voltage stress versus the gain

4.4 Operation constraints

In this study, it is assumed that the values of inductances and capacitances are sufficiently large so that the inductor currents and capacitor voltages have low ripple. As stated previously, during the ST mode, the diodes are always reverse biased. However, during the NST mode, the two qZ network diodes D_{U1} and D_{N1} are required to conduct, which can be achieved according to the conditions in (4.37).

$$\begin{aligned} i_{LU2} + i_{LU1} &> i_{UA} \\ i_{LN2} + i_{LN1} &> i_{NA} \end{aligned} \tag{4.37}$$

where i_{LU1}, i_{LU2}, i_{LN1} and i_{LN2} are the upper and the lower qZS-inductor currents as depicted in Fig. 4.3 and each of these currents is assumed to be equal to its average value of I_L. From (4.37), the condition for the diodes to conduct current is the instantaneous value of i_{UA} (or i_{NA}) becomes lower than $2I_L$ in the NST mode. Otherwise, the diodes will not be conducting which leads to a reduction in the peak value of the DC-link voltage to be V_{C1} instead of V_{C1}+V_{C2} and consequently this causes a higher disturbance in the output voltage. For

simplicity, assuming that the low order even harmonic in the circulating current is kept at a negligible level, and using (3.3), the maximum value of the upper and lower arm currents is given by:

$$I_{UA} = I_{NA} = I_{UN} + I_m / 2 \tag{4.38}$$

Using (4.18), (4.37), and (4.38) for the SS technique, the condition for the diodes to conduct during NST intervals is given by:

$$D_{sh} > \frac{1}{2} - \frac{m \cos \varphi}{4} \tag{4.39}$$

Equation (4.39) shows that the minimum limit for the shoot-through duty ratio D_{sh} depends on the power factor cos φ and modulation index m. At unity power factor and modulation index, D_{sh} should be higher than 0.25 and this value increases when supplying a more inductive load. The limitations accompanied with this configuration, when using series diodes, are:

- For a gain value less than or equal to one ($G \leq 1$) in the buck mode, and a range in the boost mode of $1 < G < 1.5$ (@ $D_{sh} = 0.25$), the diodes are not able to conduct during the whole NST mode interval causing drop in DC-link voltage.
- However, the DC-link voltage decreased during a part of NST intervals, the average voltage on the circuit components increases depending on the load condition and the circuit design parameters.
- Overcharge of all converter capacitors which may lead to converter elements damage.
- The output voltage will be highly distorted.

The reasons for these limitations in qZS-MMC are the two uncontrolled diodes (D_{U1} and D_{N1}) where their states are dependent on the circuit operating conditions such as, ST duty ratio D_{sh}, modulation index m, and cos φ. These two diodes play a dominant role in the DC voltage boosting process and cannot be removed. To overcome this issue, a pair of active switches is added in anti-parallel with the series diodes (D_{U1} and D_{N1}) to provide a controllable path

for the current in the reverse direction as shown in Fig. 4.13. The two switches T_{U1} and T_{N1} are gated by complementary gating signals to S_N and S_U respectively.

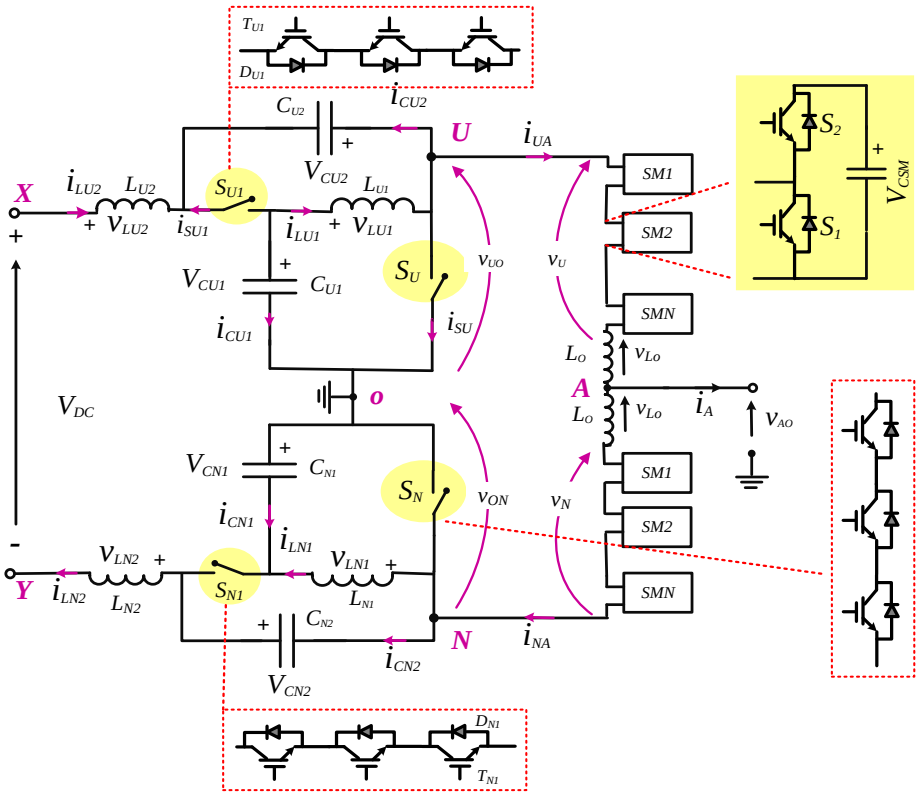


Fig. 4.13: The modified structure of the proposed quasi Z-source MMC

4.5 Deriving the three-phase configuration

The previous discussion regarding the proposed modulation techniques applied to a single-phase qZS-MMC. For a three-phase converter, the RICs technique is not applicable. To clarify that, let us assume that the three-phase MMC legs are sharing the same DC-link connection points *U* and *N* as shown in Fig. 4.13. The ST modulating signals for S_U and S_N depend on the polarity of the output phase voltage as shown in Fig. 4.11 when using RICs technique. Therefore, if the upper/lower chain-link switches are turned on, at least one of the upper/lower arms in the three-phase legs will not be able to compensate the effects of shorting the upper/lower DC-link terminals as that causes the number of the output voltage levels of that particular leg(s) to decrease by a maximum of N_{SM} /2 voltage levels. Consequently, a significant distortion in the corresponding output phase voltage will be generated.

For a detailed illustration, the three-phase upper arm modulating signals have been drawn in Fig. 4.14 where the number of inserted SMs in the upper arms in phases *A*, *B*, and *C* are N_{UA}, N_{UB}, and N_{UC} respectively. In the region R_1, the N_{UB} is higher than $N_{SM}/2$ while both the N_{UA} and N_{UC} are lower than $N_{SM}/2$, leading to distortion in the phases *A* and *C*. Phase *A* output voltage will be distorted in regions from R_1 to R_3, and phase *B* will be distorted from R_3 to R_5, while during R_1, R_5, and R_6 phase *C* will be affected, as shown in Fig. 4.14.

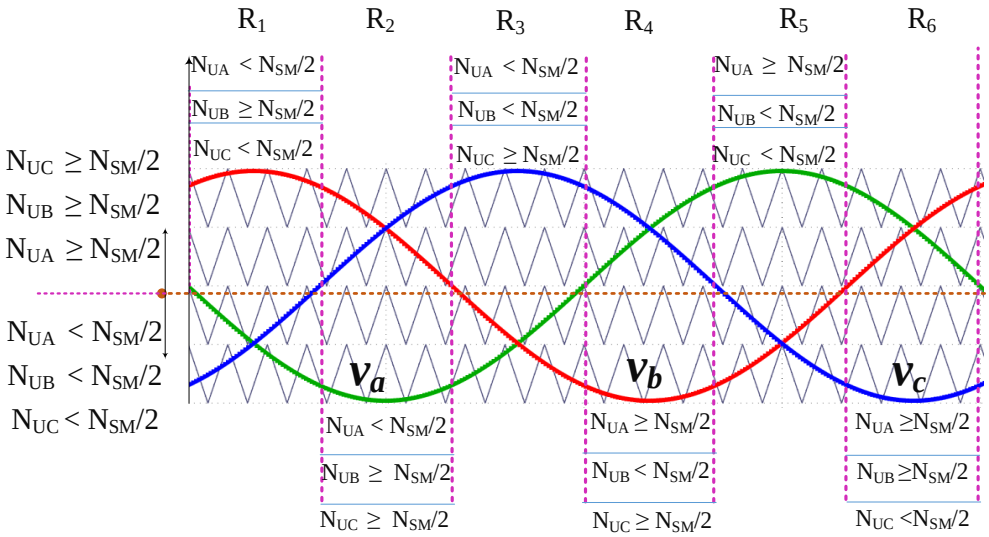


Fig. 4.14: The three-phase upper arm modulating signals

To avoid causing any distortion in the three-phase output voltages when using the RICs technique, two qZS-networks are required for each phase-leg and these can be connected to the same DC source terminals as shown in Fig. 4.15. However, using 6 qZS-networks with a high number of components is not a cost-effective design.

On the other hand, the operation of S_U and S_N are independent of the reference output phase voltages when using the SS technique for the single-phase converter, where the ST pulses are continuously introduced through the output frequency cycle. Therefore, for the three-phase converter, the SS technique can be applied while using only two qZS-networks or only one qZS-network circuit if the DC-side mid-point is not required in connection with the load (delta or star connection with floating neutral). The three-phase converter configuration is shown in Fig. 4.16.

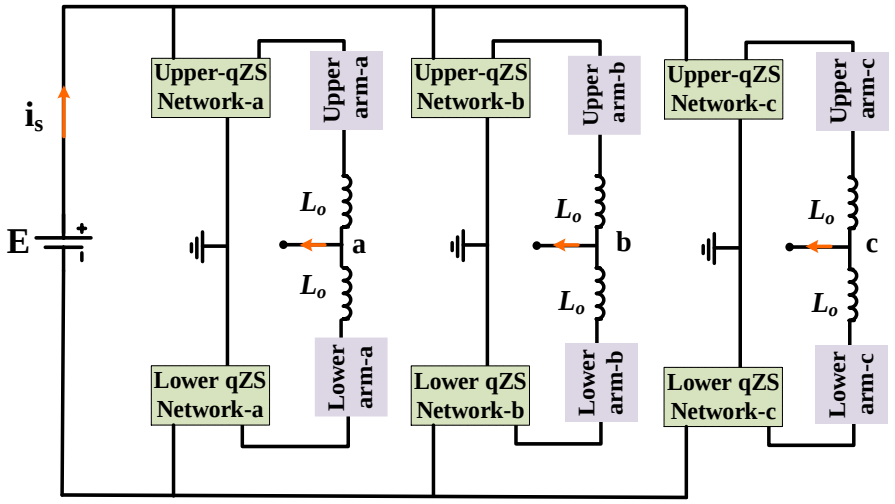


Fig. 4.15: The configuration of non-optimized three-phase qZS-MMC

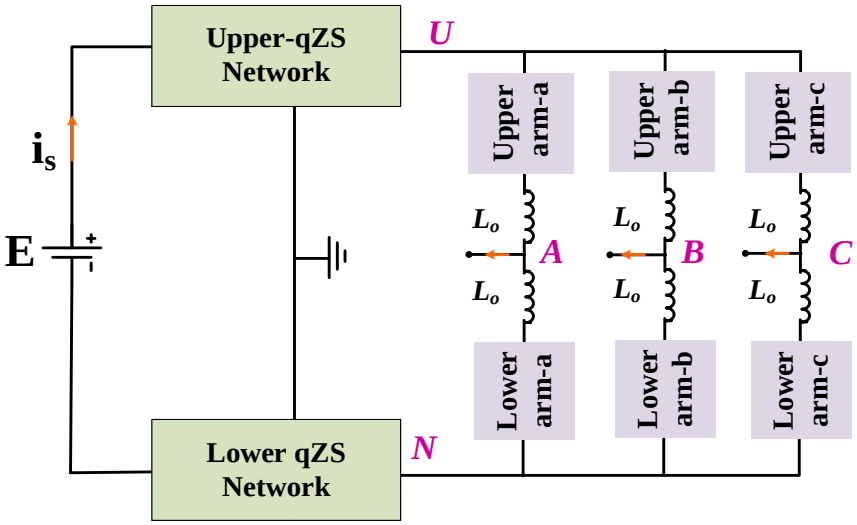


Fig. 4.16: The configuration of three-phase qZS-MMC

4.6 Control objectives

The essential objective is to keep the SMs capacitor voltages in balance, otherwise the MMC may be unstable due to imbalance problem between the SMs [3]. Based on the level-shift PWM technique, the total number of inserted SMs in the MMC leg are changed between N_{SM} -1, N_{SM} and N_{SM} +1 with total average of N_{SM} during a switching frequency cycle, which can ensure that the sum of the upper and lower arm voltage equals $N_{SM}V_C$. In order to ensure that the average

SM voltage is well distributed among all SM capacitors, the capacitor voltage balance strategy given in section 3.5 is implemented here, which is based on the sorting algorithm method reported in [95]. The implementation of this method depends on the sorting of the SM capacitor voltage and the direction of the arm current. For positive (negative) values of the arm current, the algorithm selects the SMs with lower (higher) voltages to be inserted for charging (discharging).

There are inherent low order even harmonics, with the 2nd order harmonic being the dominant component, in the circulating current, which would make additional losses and current stress on the circuit. These harmonics need to be suppressed or well-regulated to a small value particularly when the arm inductance is small [101].

Moreover, due to the presence of some sources of imbalance, such as asymmetry between the two qZS-networks and also between the two MMC arms (manufacturing tolerance), the AC fundamental current will be unequally distributed between both arms. This will appear as a fundamental frequency current component in the circulating current, which will provide a difference in the DC voltages produced by the two arms and the qZS-networks [102, 103].

Therefore, the controller target is to suppress the second order harmonic using the second order harmonic circulating current control, and also eliminate the fundamental component in the circulating current using fundamental frequency circulating current control. Using (3.9) and (3.10), the upper and lower arm voltage references can be given as:

$$v_U = v_{UN}/2 - v_{AO} - v_{cir} \tag{4.40}$$

$$v_N = v_{UN}/2 + v_{AO} - v_{cir} \tag{4.41}$$

The variable v_{cir} is used to control the circulating current, otherwise it is set to zero. The upper and lower arm currents are measured to get the circulating current i_{cir} using (3.4). i_{cir} are required to suppress the second order harmonic and the fundamental components in the circulating current.

A. 2nd order harmonic circulating current control

There may be significant 2nd order harmonic components in the circulating current i_{cir}, particularly when the arm inductor size is small. Allowing for a large second order component would add additional losses in the converter. Therefore, it is advantageous to suppress this component.

For AC circulating current controller, a proportional resonant (PR) controller is considered in [104], which is widely applied for single-phase converter [101]. This controller is used to detect and eliminate the undesired harmonics. The PR controller is able to achieve a high gain at the selected frequency and then eliminate the steady state error. The open loop transfer functions of an ideal PR controller and a non-ideal PR controller are given by (4.42) and (4.43) respectively.

$$G_{PR}(s) = K_{PR} + \frac{2K_{iR}s}{s^2 + (2\omega_o)^2} \tag{4.42}$$

$$G_{PR}(s) = K_{PR1} + \frac{2\omega_c K_{iR}s}{s^2 + 2\omega_c s + (2\omega_o)^2} \tag{4.43}$$

where ω_o is the angular fundamental output frequency, $2\omega_o$ is the angular 2nd order harmonic frequency to be eliminated, and $\omega_c << \omega_o$ represents the cutoff frequency. In an ideal PR controller, the gain is infinite at the selected harmonic frequency ($2\omega_o$), whilst at other frequency gain is zero. Practically, non-ideal PR controller is preferred as the bandwidth can be set and widen by ω_c compared to the ideal controller, which can be helpful for reducing sensitivity of slight frequency variation [105].

The circulating current can be obtained by (3.4). $G_{PR}(s)$ needs to be adjusted such that the gain at selected harmonic frequency $2\omega_o$ is high. The gain is chosen to be 50 at $2\omega_o$ and 1 at zero frequency. Using (4.43), the controller coefficients K_{PR} and K_{iR} are designed as 1 and 50 respectively. The bandwidth can be selected by using ω_c. In practice, ω_c values of 5-10 rad/s have been found to provide a good compromise [105]. ω_c of 5 rad/s is used in this work. Fig. 4.17 shows the bode diagram of the $G_{PR}(s)$.

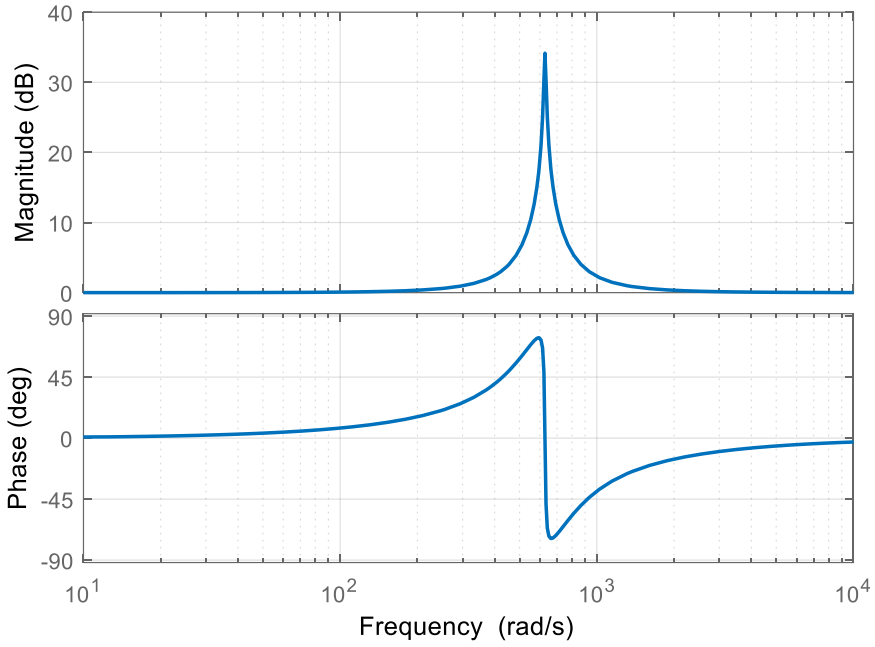


Fig. 4.17: Bode diagram of the PR controller for filtering 2nd order harmonic component in the circulating current

B. Fundamental frequency circulating current control

Imbalance in the values of the passive components of the two qZS-networks, upper and lower arm and within HBSMs, which unless compensated, causes a circulating fundamental frequency component current. This leads to imbalance in voltages produced by the qZS-networks and the two MMC arms and consequently low order harmonic components appear in the output voltage.

To correct this, another proportional resonant controller is applied to minimize the fundamental frequency component in the circulating current caused by circuit components imbalance. Another term is added to (4.43) to filter out the fundamental frequency component in the circulating current. The modified transfer function is (4.44).

$$G_{PR}(s) = K_{PR1} + \frac{2\omega_c \cdot K_{iR1} \cdot s}{s^2 + 2\omega_c s + (\omega_o)^2} + K_{PR2} + \frac{2\omega_c \cdot K_{iR2} \cdot s}{s^2 + 2\omega_c s + (2\omega_o)^2} \quad (4.44)$$

Fig. 4.18 shows the control block diagram for the two circulating current controllers. Fig. 4.19 shows the bode diagram of the two PR controllers together with the following set of parameters: ω_c = 5 rad/s, K_{PR1} = *0.5*, K_{PR2} = 0.5, K_{iR1} = 50, and K_{iR2} = 50. It is seen that this controller achieves the expected high gain

peaks at the selected frequencies 2π×50 rad/s and 2π×100 rad/s and small gain for the other frequencies.

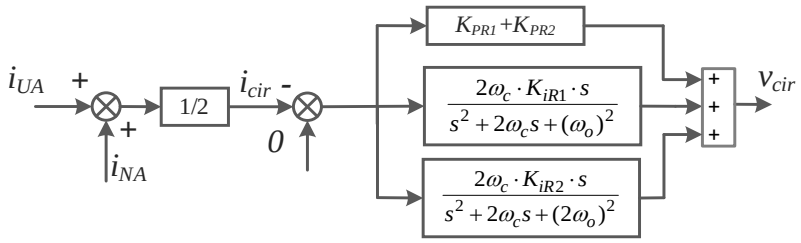


Fig. 4.18: The control diagram for suppressing the 2nd order harmonic and fundamental frequency components in the circulating current

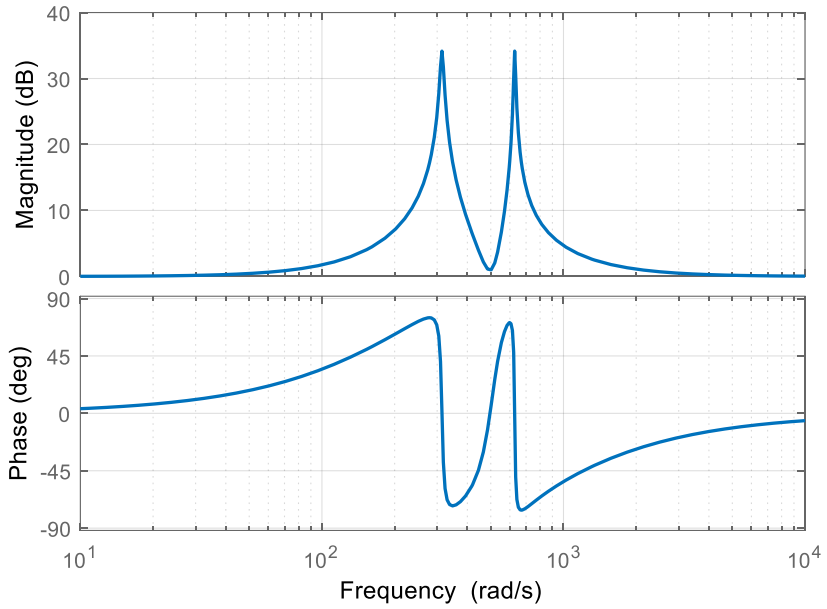


Fig. 4.19: Bode diagram of the PR control for filtering 2nd order harmonic and fundamental components in the circulating current

4.7 Simulation results

To verify the operation principles and show the validity of the proposed modulation techniques and control scheme, relevant models were implemented in PLECS for the proposed converter configuration shown in Fig. 4.13. The parameters used in the simulation models are given in Table 4.1. The simulation study has been carried out using a passive inductive AC load (R+L) and considering that all system components and switches are ideal.

Firstly, the requirement for using antiparallel active switches to avoid the limitations identified in Section 4.4 is investigated. The second test is to verify the performance of the proposed modulation techniques (SS and RICs). Operation considering components asymmetry and the corresponding control algorithm is explored using unequal component parameters.

Table 4.1: Parameters of the simulation model

Parameter	Value
Peak output voltage (V_m)	5.5 kV
DC source voltage (V_{DC})	5.5 kV to 11 kV
SM capacitor voltage (V_{CSM})	1.36 kV
Number of SMs per arm (N_{SM})	8
Arm inductance (L_o)	5 mH
SMs capacitances (C_{SM})	3.3 mF
qZS inductances ($L_{U1} = L_{U2} = L_{N1} = L_{N2}$)	10 mH
qZS capacitances ($C_{U1} = C_{N1}$)	3.3 mF
qZS capacitances ($C_{U2} = C_{N2}$)	3.3 mF
Load resistance	10 Ω
Load inductance	10 mH
Carrier frequency (f_c)	4 kHz
Sorting frequency (f_{sort})	0.5 kHz
Arm equivalent resistance	0.05 Ω
L_{U1}, L_{U2}, L_{N1}, L_{N2} equivalent resistance	0.05 Ω

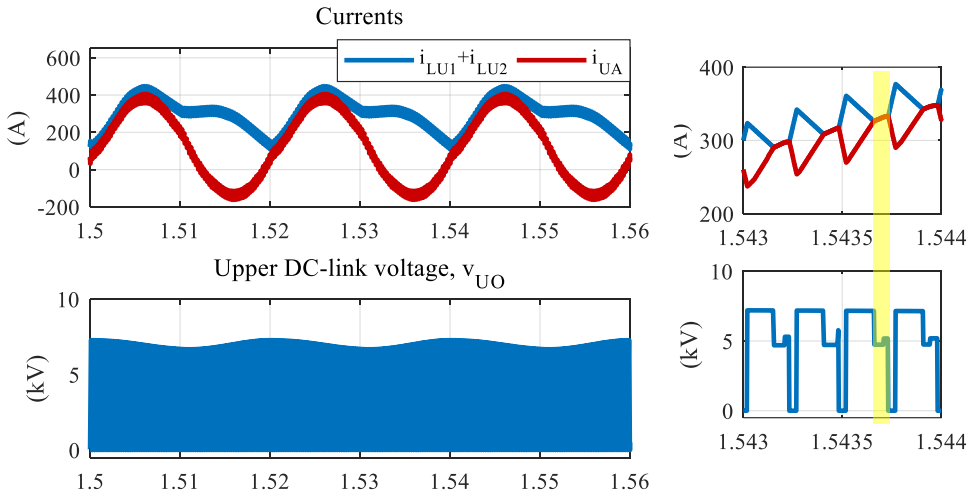
4.7.1 Test 1: Verifying the operation constraints

The first test demonstrates the necessity of using the antiparallel active switches in qZS-networks (T_{U1} and T_{N1}) when operating at low D_{sh}. According to the relation given in (4.39), the D_{sh} should be higher than 0.26 at $\cos \varphi = 0.95$ and $m = 1$, otherwise the diodes will not be conducting during NST mode causing a reduction in the DC-link voltage, therefore, to avoid this, the antiparallel active switches T_{U1} and T_{N1} are required.

4.7.1.1 Case 1: D_{sh} does not satisfy (4.39)

The first part assumes no antiparallel switches where D_{sh} is set to 0.15 (< 0.26), m = 1 and giving G = 1.21, and consequently if the DC source voltage is 9.1 kV, a peak value for the fundamental component of output voltage of 5.5 kV is achieved according to (4.14) when using the SS technique.

Fig. 4.20 shows the upper arm current i_{UA} , the sum of upper qZS-inductor currents $i_{LU1} + i_{LU2}$ and the upper DC-link voltage v_{UO} when using series diode only. It is clear that when the upper arm current waveform i_{UA} exceeds the sum $i_{LU1} + i_{LU2}$, a negative current will be expected to flow through the diode D_{U1} which is impossible and therefore the arm current i_{UA} equal to $i_{LU1} + i_{LU2}$, which will cause a reduction in the DC-link voltage. The DC-link voltage is not remaining constant in NST mode where it is dropped from 7.5 kV to 5 kV as highlighted in Fig. 4.20b. On the other hand, Fig. 4.21 shows that the arm current can be higher than $i_{LU1} + i_{LU2}$ without a drop of the DC-link voltage as a result of using active switches in antiparallel with the series diodes to provide a controlled reverse conduction path.



(a) (b)

Fig. 4.20: Simulation results at D_{sh} = 0.15 when using series diode only: a) upper arm current i_{UA}, and the sum of qZS inductor currents i_{LU1}+i_{LU2} (top), upper DC-link voltage (bottom), and b) zoomed view

Fig. 4.22 shows the parallel qZS capacitor voltages v_{CU1} and v_{CN1}, the series qZS capacitor voltages v_{CU2} and v_{CN2}, and the upper and lower arm SMs capacitor voltages when using series diode only.

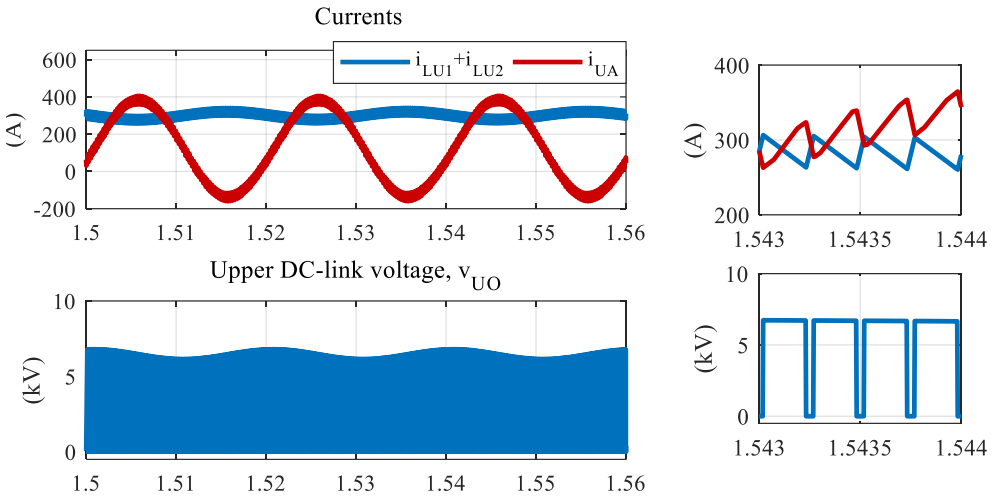


Fig. 4.21: Simulation results at D_{sh} = 0.15 when using controlled antiparallel switches: a) upper arm current i_{UA}, and the sum of qZS inductor currents i_{LU1}+i_{LU2} (top), upper DC-link voltage (bottom), and b) zoomed view

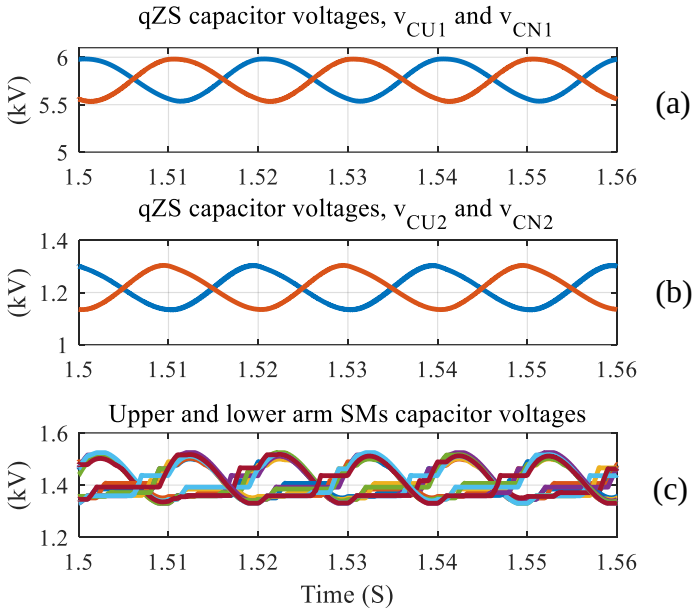


Fig. 4.22: Simulation results at D_{sh} = 0.15 when using series diode only: a) parallel qZS capacitor voltages v_{CU1} and v_{CN1}, b) the series qZS capacitor voltages v_{CU2} and v_{CN2}, and c) the upper and lower arm SMs capacitor voltages

The expected average values of network capacitor voltages v_{CU1} (or v_{CN1}), v_{CU2} (or v_{CN2}), and SMs capacitor voltages defined by (4.5) and (4.12) are 5.5 kV, 0.97 kV, and 1.375 kV respectively. However, the actual simulation values of capacitor voltages are 5.75 kV, 1.22 kV, and 1.42 kV respectively as shown in Fig. 4.22. The increase in the actual values is depending on the load condition and the circuit design parameters.

This means that the circuit capacitors are exposed to overcharge if any of the series diodes D_{U1} and D_{N1} stop conducting in NST mode. However, using the active switches in antiparallel T_{U1} and T_{N1} with the series diodes makes all the capacitor voltages to be at their calculated values as explained previously and as shown in Fig. 4.23.

Fig. 4.24 and Fig. 4.25 show the output voltage and current and their harmonic spectrum when using series diode only and in Fig. 4.26 and Fig. 4.27 when adding the antiparallel switches.

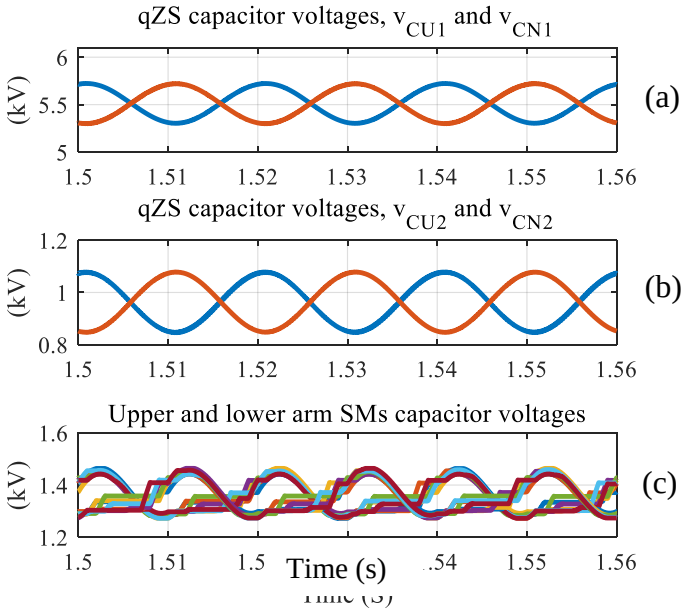


Fig. 4.23: Simulation results at D_{sh} = 0.15 when using controlled antiparallel switches: a) parallel qZS capacitor voltages v_{CU1} and v_{CN1}, b) the series qZS capacitor voltages v_{CU2} and v_{CN2}, and c) the upper and lower arm SMs capacitor voltages

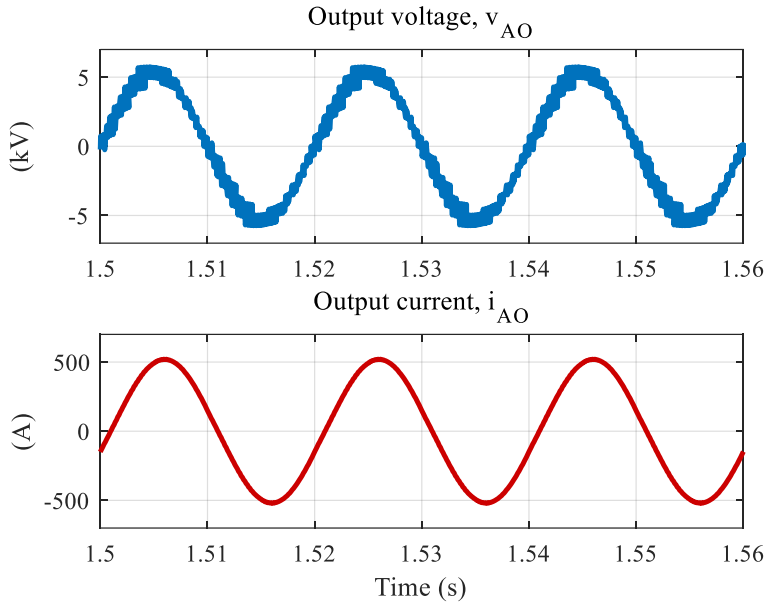


Fig. 4.24: Output voltage and output current at D_{sh} = 0.15 when using series diode only

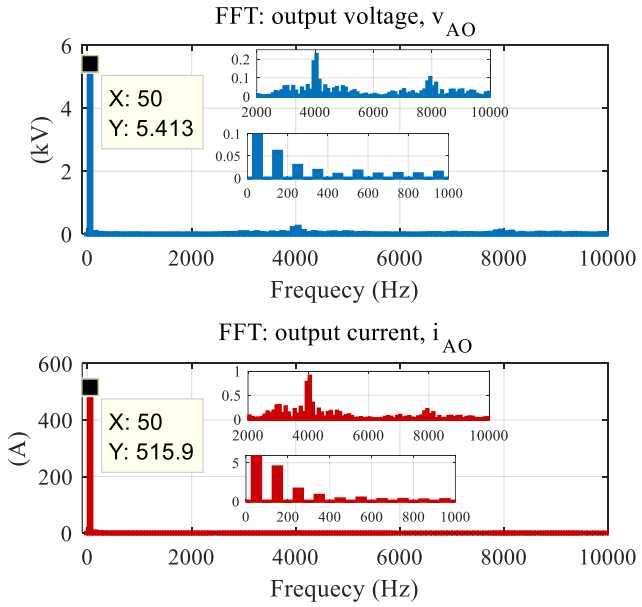


Fig. 4.25: Harmonic spectrum of the output voltage (zoom in component are shown in kV) and output current at D_{sh} = 0.15 when using series diode only

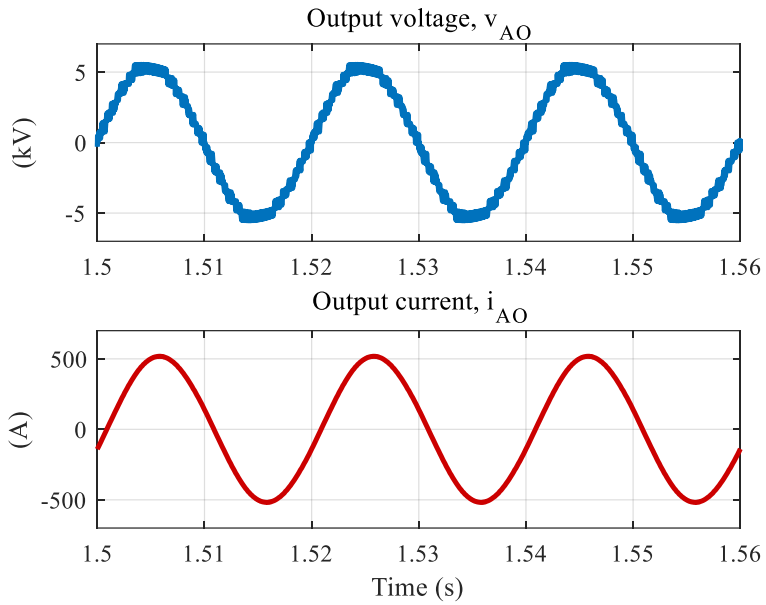


Fig. 4.26: Output voltage and output current at D_{sh} = 0.15 when using controlled antiparallel switches

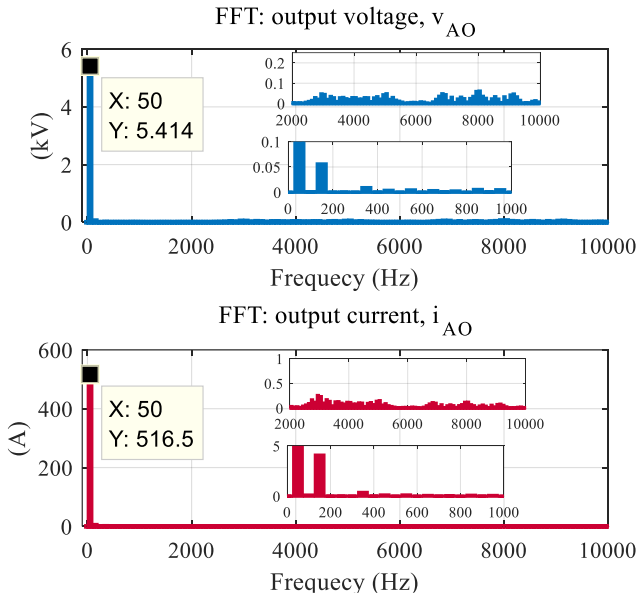


Fig. 4.27: Harmonic spectrum of the output voltage (zoom in component are shown in kV) and output current at D_{sh} = 0.15 when using controlled antiparallel switches

Even though the converter delivers approximately the same fundamental voltage and current (in amplitude) in both cases, using only the series diodes resulted in a slightly higher level of low order harmonics (5^{th} and 7^{th}) and a significant higher level of switching frequency harmonics. This distortion is also revealed by the difference in the total harmonic distortion (THD) values for the output voltage and current that are 8.7% and 1% respectively when using only the series diodes compared to 5.7% and 0.8% respectively when using the antiparallel switches.

4.7.1.2 Case 2: D_{sh} satisfies (4.39)

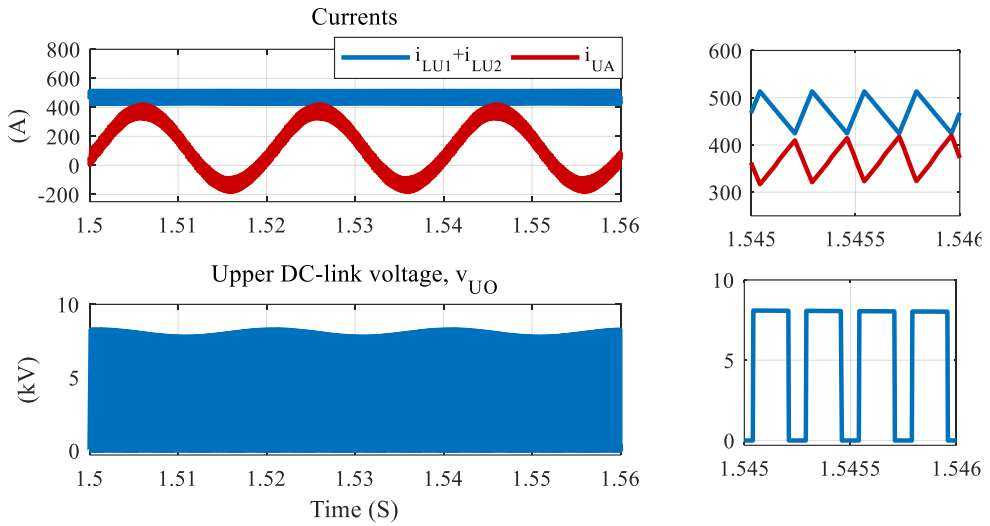
The second case has been carried at D_{sh} = 0.333 (> 0.26), giving a voltage gain of G = 2 and consequently, for a DC source voltage of 5.5 kV, the peak fundamental output voltage reaches 5.5 kV. According to (4.39), at cos φ = 0.95 and m = 1, no current will flow through the antiparallel switches at D_{sh} values higher than 0.26. Fig. 4.28 shows the upper arm current i_{UA} , the sum of upper qZS-inductor currents $i_{LU1} + i_{LU2}$ and the upper DC-link voltage v_{UO} when using series diode only. It is clear that the waveform of the upper arm current i_{UA} is always lower than the sum $i_{LU1} + i_{LU2}$, and consequently there is no need for using controlled antiparallel switches. Fig. 4.29 shows the output voltage and current without distortion in the output waveforms.

These two test cases verify the analysis explained previously and show the condition where using antiparallel active switches is necessary for better operation of the proposed qZS-MMC.

4.7.2 Test 2: Verifying the proposed modulation techniques

In this section, the performance of the SS and RICs technique has been compared. The test has been carried considering that the available DC source voltage is 7.3kV and the desired peak of the fundamental output voltage is 5.5 kV. Therefore, $G*m$ = (2*5.5kV) / 7.3kV which should result in a converter voltage gain G= 1.5 and modulation index m=1.

From (4.14) and (4.29), the required shoot-through duty ratios D_{sh} are 0.25 for the SS technique and 0.17 for RICs technique.



(a) (b)

Fig. 4.28: Simulation results at D_{sh} = 0.333: a) upper arm current i_{UA}, and the sum of qZS inductor currents i_{LU1}+i_{LU2} (top), upper DC-link voltage (bottom), and b) their zooming

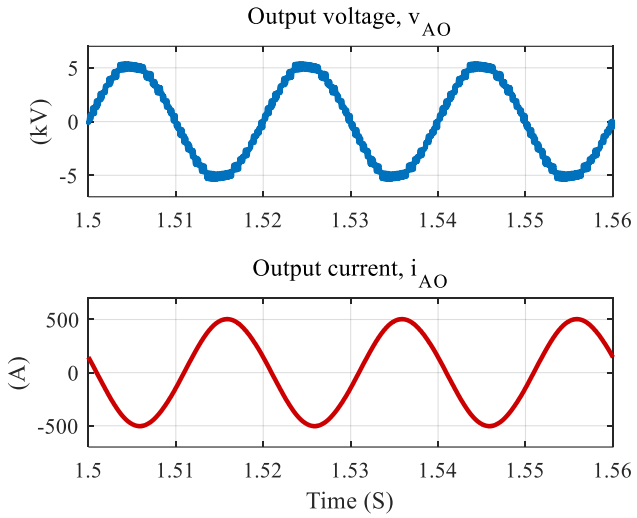
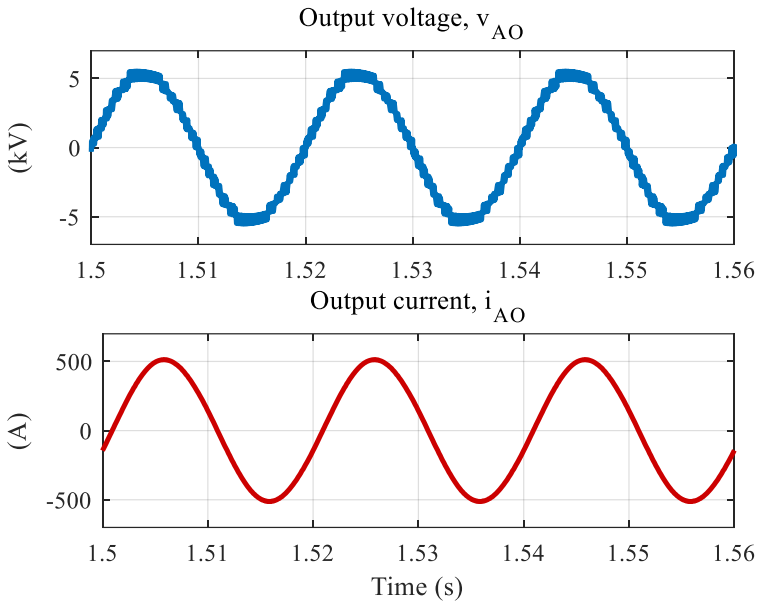


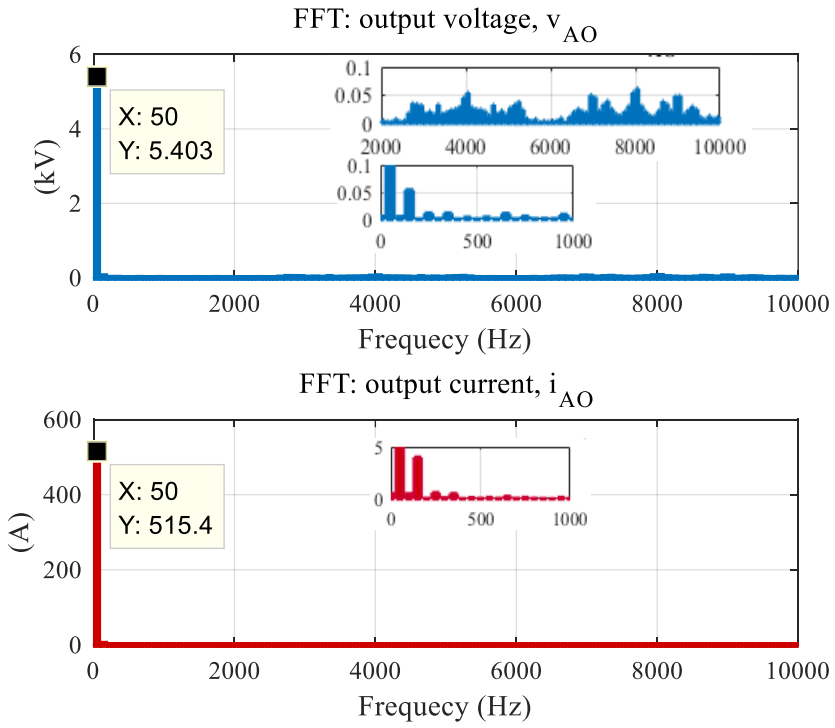
Fig. 4.29: Output voltage and output current at D_{sh} = 0.333

The output voltage and current and their harmonic spectrum for the SS and RICs techniques are shown in Fig. 4.30 and Fig. 4.31 respectively. The peak value of the fundamental output voltage as revealed by the FFT is 5.41 kV for both techniques. The difference between the expected peak value of the fundamental output voltage (5.5 kV) and the actual simulated one is caused by having some parasitic resistance in the components of the circuit. The voltage and current

harmonic spectrums show irrelevant values of low order harmonic components, where the most significant one is the 3rd order harmonic with a peak value of less than 1% of the fundamental component.

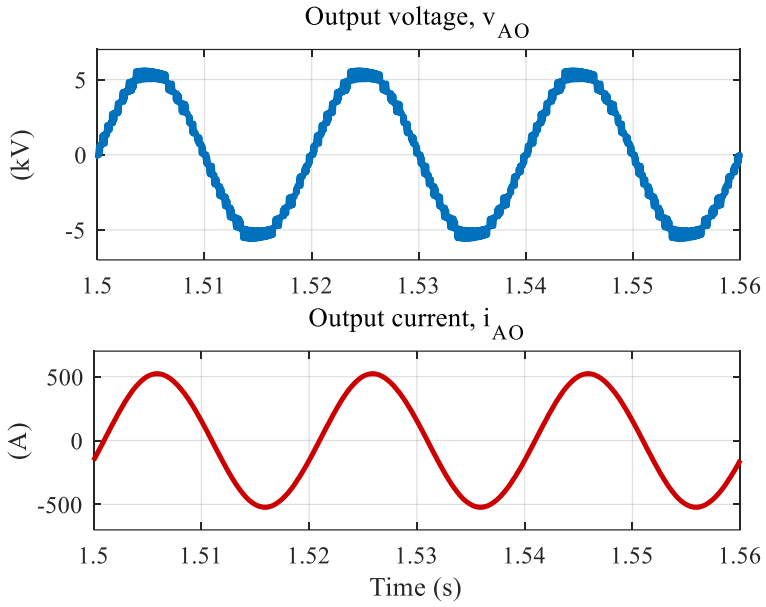


(a)

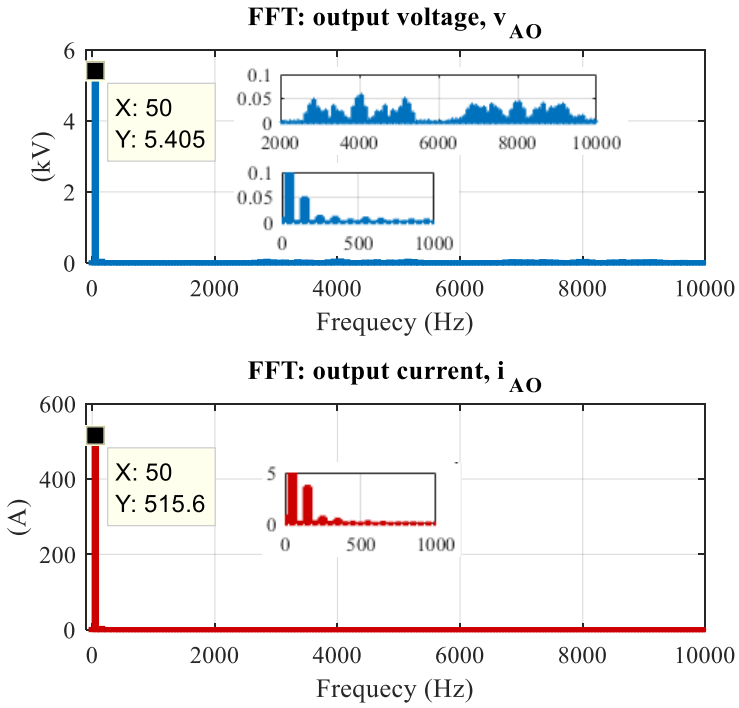


(b)

Fig. 4.30: Simulation results for the SS technique, a) output voltage and current waveforms, and b) harmonic spectrum (zoom in voltage component are shown in kV)



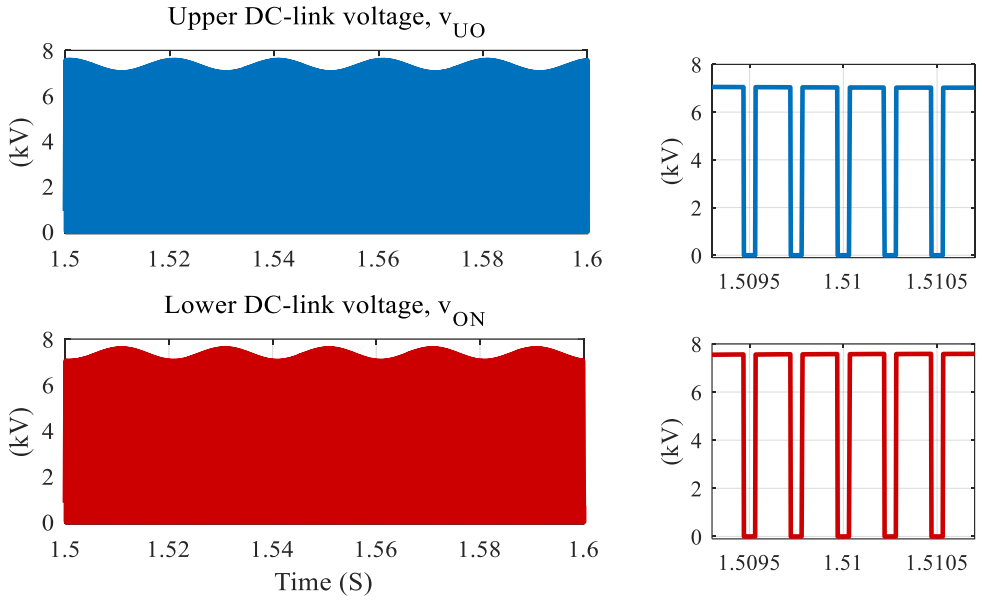
(a)



(b)

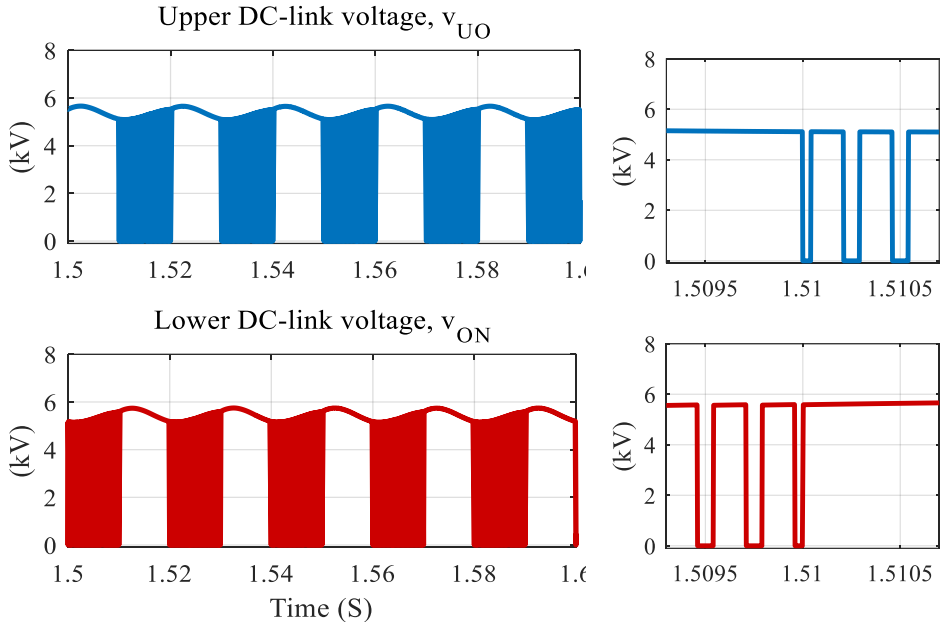
Fig. 4.31: Simulation results for the RICs technique, a) output voltage and current waveforms, and b) harmonic spectrum (zoom in voltage component are shown in kV)

The upper and the lower DC-link voltages v_{UO} and v_{ON} are shown in Fig. 4.32 and Fig. 4.33, where the peak values experienced in the DC-link voltages for the SS and the RICs techniques are 7.3 kV and 5.45 kV respectively.



(a) (b)

Fig. 4.32: Simulation results for the SS technique, a) upper and lower DC-link voltages waveforms, and b) zoomed view

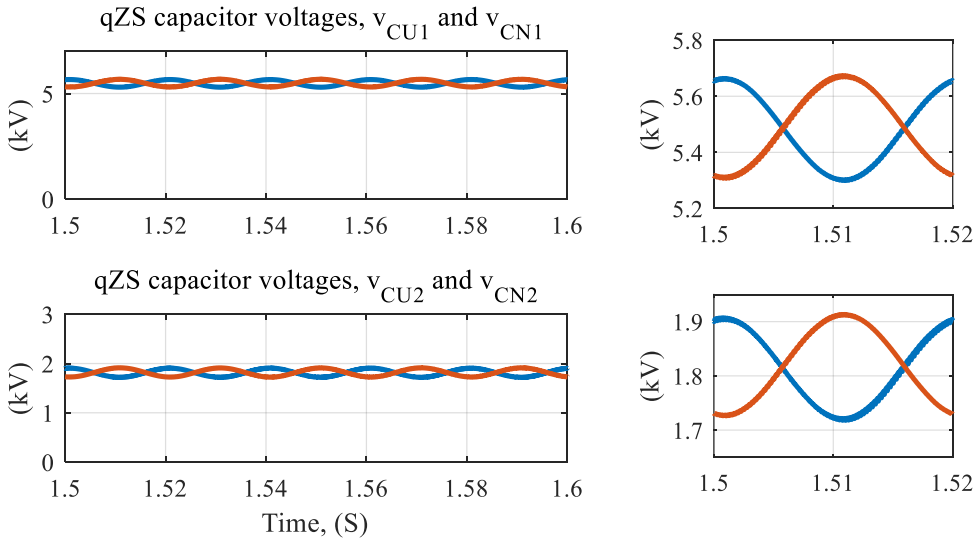


(a) (b)

Fig. 4.33: Simulation results for the RICs technique, a) upper and lower DC-link voltages waveforms, and b) zoomed view

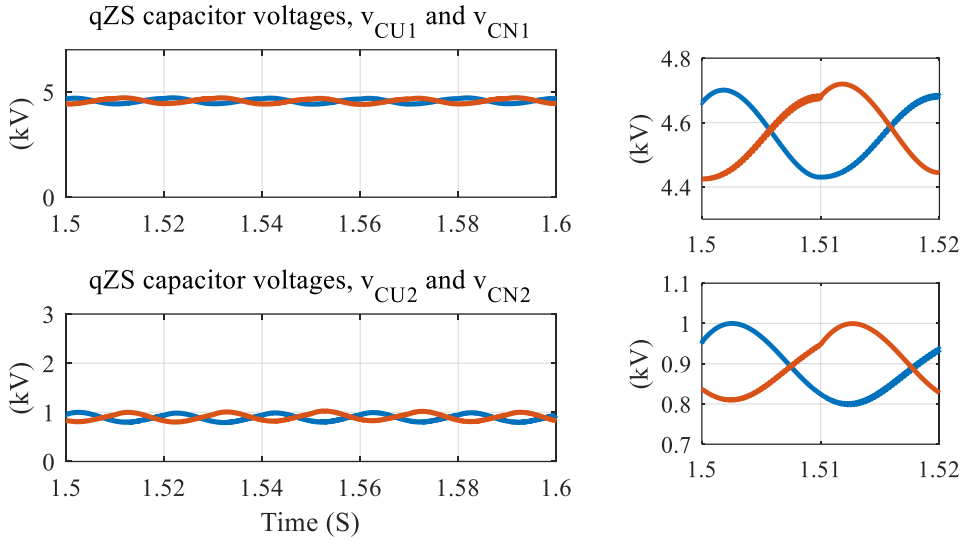
Therefore, it is demonstrated that the voltage stress of the chain-link switches is significantly higher for the SS technique (by 34 %) compared to the RICs technique. It is worth to mention that the upper qZS-network can be shorted during the negative half of output voltage, while the lower qZS-network can be shorted during the positive half of the output voltage, when using RICs technique.

The qZS-capacitor voltages (v_{CU1}, v_{CN1}, v_{CU2} and v_{CN2}) are shown in Fig. 4.34 and Fig. 4.35. The qZS-capacitor average voltages v_{CU1}= v_{CN1}=V_{C1} and v_{CU1} = v_{CN1} = V_{C2} are 5.47 kV and 1.83 kV when using the SS technique, while they are 4.5 kV and 0.9 kV when using the RICs technique as shown in Fig. 4.34 and Fig. 4.35. Therefore, the SS technique requires a higher voltage rating for qZS-capacitor than the RICs technique. The ripple for V_{C1} is the same for both modulation methods, at 7% (0.39 kV / 5.47 kV for the SS technique and 0.32 kV / 4.58 kV for RICs technique). Therefore, the required qZS capacitances C_{U1} and C_{N1} for the SS and RICs techniques are the same. On the other hand, the ripple for V_{C2} is 11% (0.2 kV/1.8 kV) for the SS technique and 21% (0.19 kV / 0.9 kV) for the RICs technique, leading to RICs technique required a larger capacitances C_{U2} and C_{N2} than SS technique. A detailed qZS capacitor design will be given in section 5.1.1.1.



(a) (b)

Fig. 4.34: Simulation results for the SS technique, a) qZS capacitor voltages waveforms, and b) zoomed view



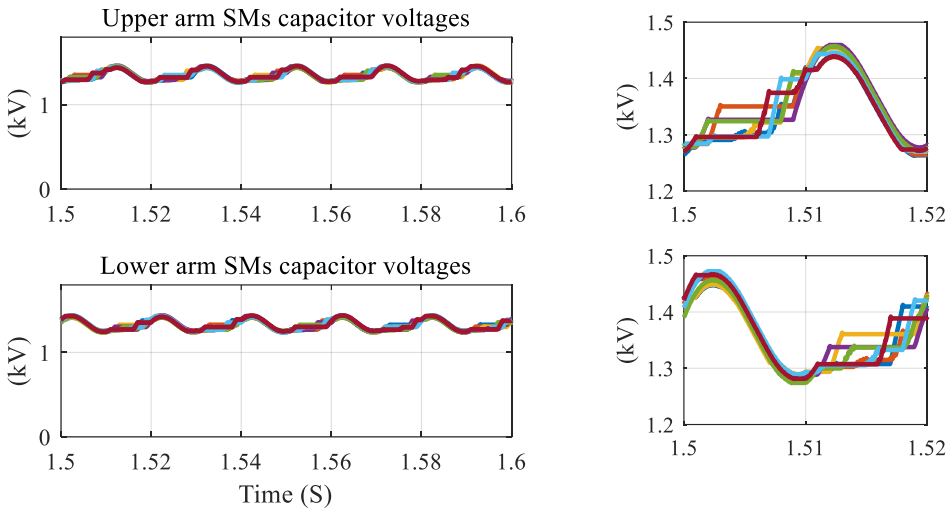
(a) (b)

Fig. 4.35: Simulation results for the RICs technique, a) qZS capacitor voltages waveforms, and b) zoomed view

Fig. 4.36 and Fig. 4.37 show the upper and lower arm SMs capacitor voltages for the SS and RICs techniques respectively. At the same voltage gain, the SMs average capacitor voltages for the two techniques are 1.365 kV despite different DC-link peak voltages. The average SMs capacitor voltages are calculated according to the peak value of the total DC-link voltage (2*5.45 kV) divided by N_{SM} when using RICs technique, while they are calculated according to the average value of the total DC-link voltage (2*5.4 kV) divided by N_{SM} when using SS techniques. The two techniques provide different SMs capacitor voltage ripples which will be estimated in the next section.

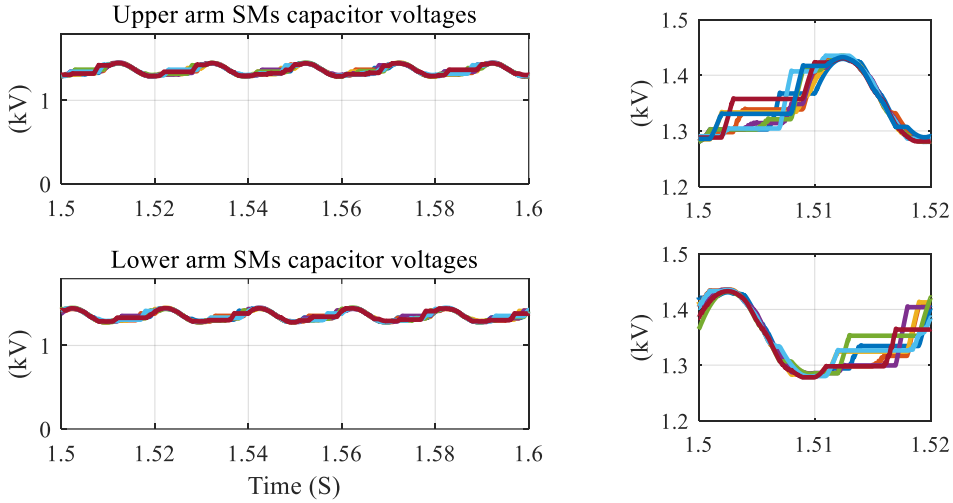
The upper and lower qZS-inductor currents are shown in Fig. 4.38 and Fig. 4.39 for the SS and RICs techniques. When comparing the low frequency current components, the inductor currents i_{LU1} and i_{LN1} have low ripples at the fundamental frequency in case of using SS technique as shown in Fig. 4.38, whereas the same currents have high level of fundamental frequency ripples when using the RICs technique where their peak value equals three times of the average value as shown in Fig. 4.39. When comparing the switching current ripple stress, the inductor currents i_{LU2} and i_{LN2} have switching frequency ripples as revealed in Fig. 4.38b and Fig. 4.39b, where the peak to peak switching ripples in case of using RICs technique is half of that in case of using the SS technique mainly because of

switching only half the DC-link voltage during the ST. Noting that the previous test results have been illustrated while suppressing the 2nd order harmonic component in the arm current.



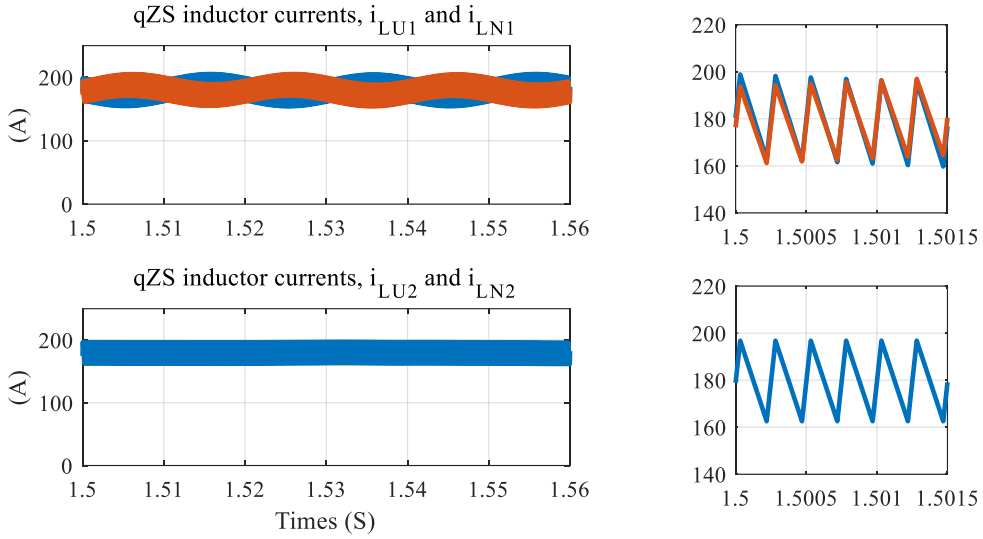
(a) (b)

Fig. 4.36: Simulation results for the SS technique, a) SMs capacitor voltages, and b) zoomed view



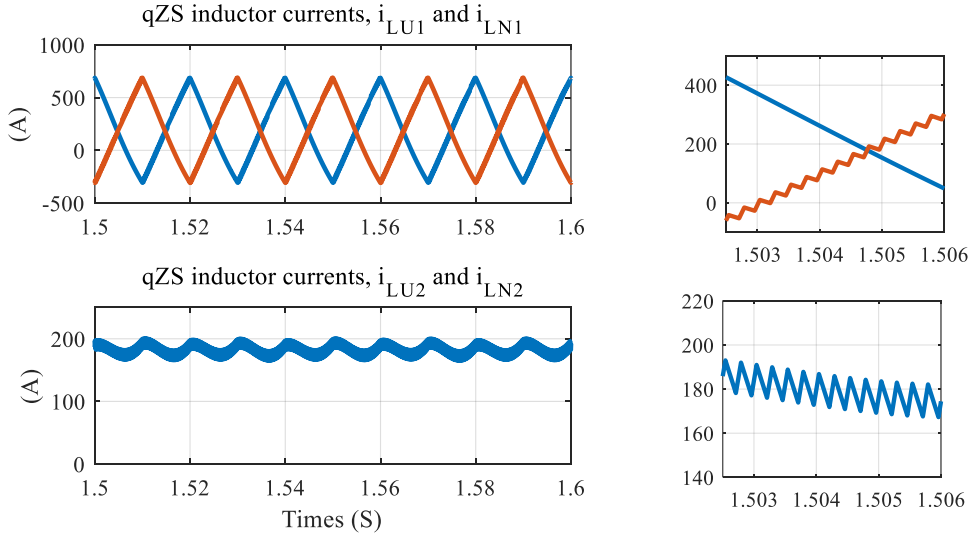
(a) (b)

Fig. 4.37: Simulation results for the RICs technique, a) SMs capacitor voltages, and b) zoomed view



(a) (b)

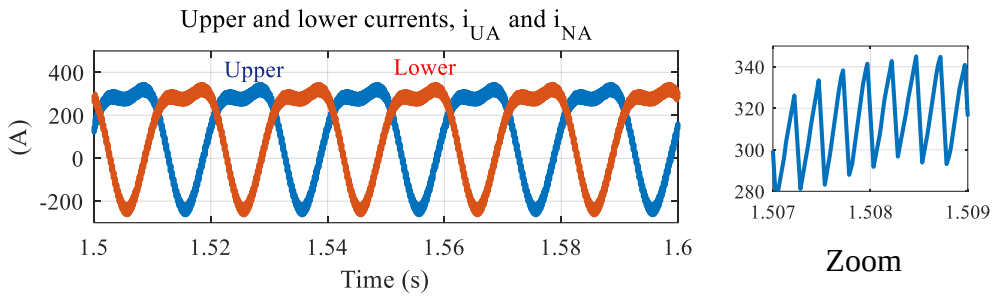
Fig. 4.38: Simulation results for the SS technique, a) qZS inductor currents, and b) zoomed view showing the switching ripple



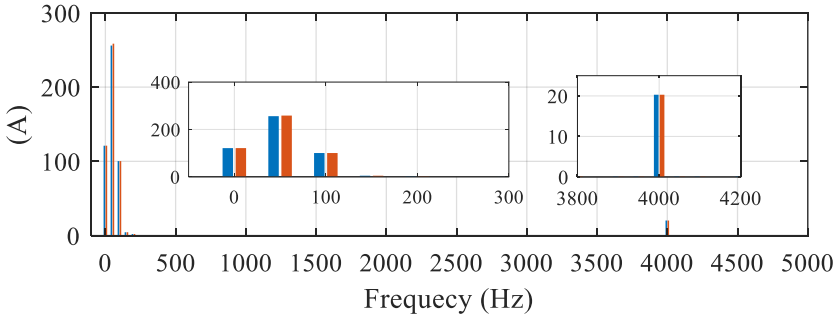
(a) (b)

Fig. 4.39: Simulation results for the RICs technique, a) qZS inductor currents, and b) zoomed view showing the switching ripple

It is important to clarify the effect of employing the 2nd order harmonic circulating current controller on the arm currents. To illustrate this, the upper and lower arm currents and their harmonic spectrum are presented in Fig. 4.40 and Fig. 4.41 for the SS and RICs techniques showing the 2nd order harmonic component in the arm current.

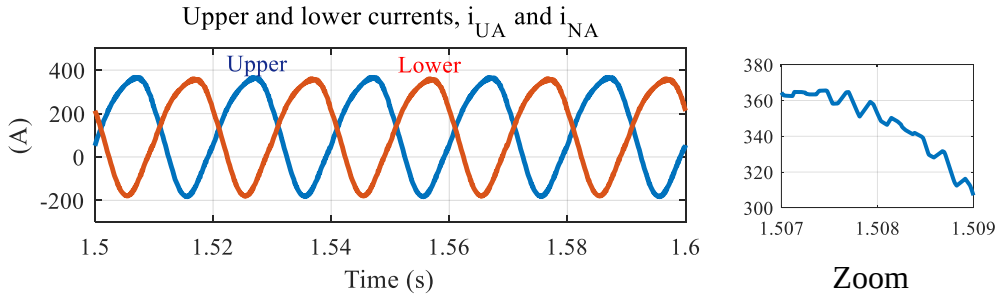


(a)

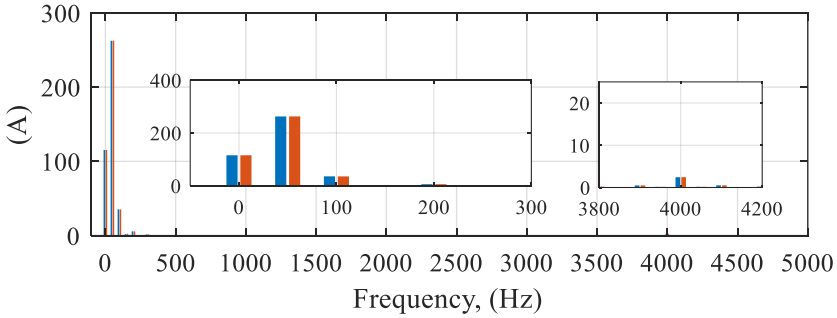


(b)

Fig. 4.40: The SS technique simulation results showing the 2nd order harmonic component in the circulating current, a) upper and lower arm currents, and b) harmonic spectrum



(a)



(b)

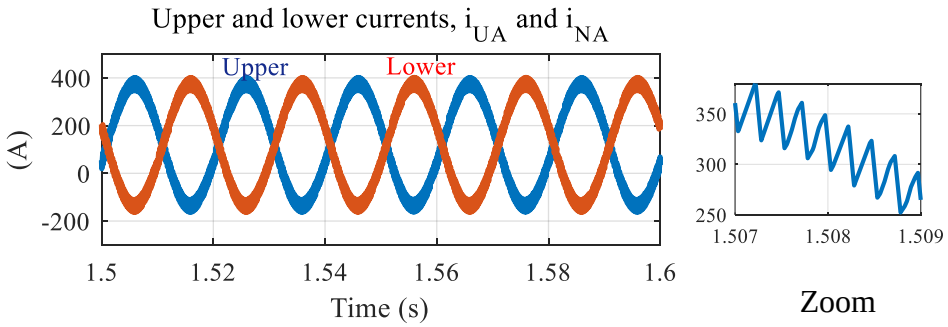
Fig. 4.41: The RICs technique simulation results showing the 2nd order harmonic component in the circulating current, a) upper and lower arm currents, and b) harmonic spectrum

It is noted that the 2nd order harmonic component is generated, and this has a significant value when using the SS technique compared with the RICs technique.

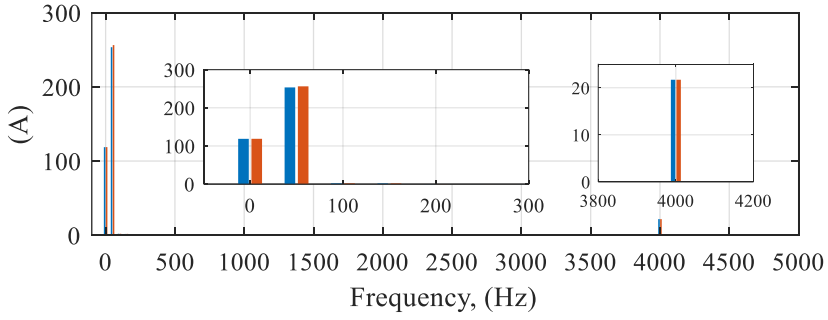
By employing the 2nd order harmonic circulating current control, the 2nd order harmonic circulating current can be well suppressed to be almost zero as shown in Fig. 4.42 and Fig. 4.43 for the SS and RICs techniques respectively. This allows using a much smaller arm inductance value.

The arm inductor has also a role to limit the switching frequency components in the arm current. The switching frequency ripples in the arm currents are high in case of using the SS technique which is around six times the ripples in case of using the RICs technique at the same arm inductance value, as highlighted in the zoom part and also the harmonic spectrum in Fig. 4.42 and Fig. 4.43. A detailed arm inductor design will be given in section 4.8.

Table 4.2 summarizes the key simulation results for the two modulation techniques with the important values of circuit voltage.

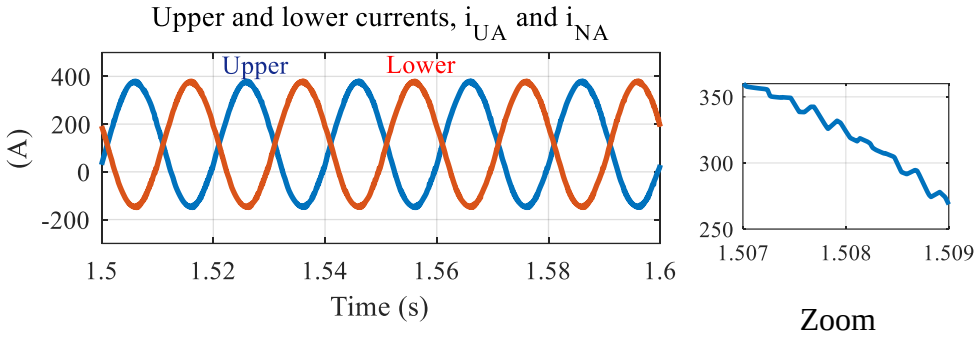


(a)

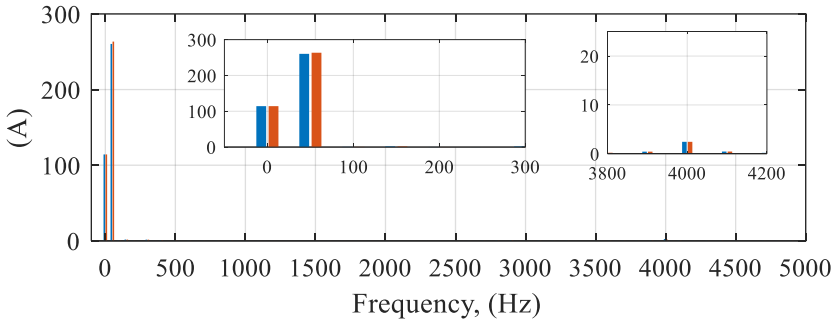


(b)

Fig. 4.42: The SS technique simulation results with employing the 2nd order harmonic circulating current controller, a) upper and lower arm currents, and b) harmonic spectrum



(a)



(b)

Fig. 4.43: The RICs technique simulation results with employing the 2nd order harmonic circulating current controller, a) upper and lower arm currents, and b) harmonic spectrum

Table 4.2: Simulation results for SS and RICs techniques

Modulation technique	SS	RICs
Desired peak output voltage	5.5 kV	
DC source voltage	7.33 kV	
Desired voltage gain G	1.5	1.5
D_{sh}	0.25	0.167
m	1	1
SMs capacitor voltage	1.36 kV	1.36 kV
Peak of upper/lower DC-link voltage	7.35 kV	5.5 kV
V_{C1}	5.47 kV	4.6 kV
V_{C2}	1.8 kV	0.9 kV

4.7.3 Test 3: Operation considering components asymmetry

Manufacturing tolerance in passive elements may cause asymmetry between the two qZS-networks and also between the two MMC arms. To study its effect on the operation, intentional error in values of capacitors and inductors are added in the simulation. The tolerance in passive components is usually within ±1%, ±5% or ±10% [106]. Two simulation cases have been considered using the SS technique.

4.7.3.1 $C_{U1} = 0.8C_{N1}$

In this study, the worst case for the ±10% tolerance range is simulated. For this purpose, it is assumed that the capacitance C_{U1} in the upper qZS-network has an error of -10% and the capacitance C_{N1} in the lower qZS-network has an error of +10% in their values. Therefore, the capacitance values of the two qZS-networks are mismatched such that $C_{U1} = 0.8C_{N1}$. Fig. 4.44 shows the qZS capacitor voltages v_{CU1} and v_{CN1}, and the upper and lower SMs capacitor voltages.

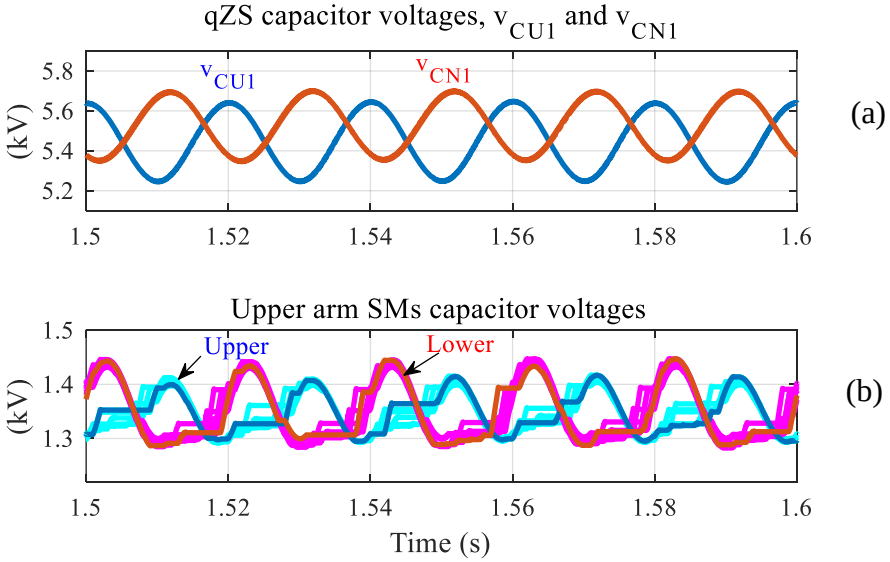


Fig. 4.44: Simulation results using SS technique in case of C_{U1}= $0.8C_{N1}$: a) the qZS capacitor voltages v_{CU1} and v_{CN1}, and b) the upper (blue) and lower (red) arm SMs capacitor voltages at N_{SM} = 8

It is noted that there is an imbalance between the qZS capacitor voltages, where their average values are not equal leading to a slight difference between the average value of both the upper and lower SMs capacitor voltages as shown in Fig. 4.44. It is obvious that the change in capacitance affects the corresponding voltage ripple (decreasing capacitance increases the ripples).

In addition, the fundamental frequency component of the upper and the lower arm currents are not equal, as illustrated from their FFT shown in Fig. 4.45a. The fundamental frequency component appears in the circulating current as shown in Fig. 4.45b.

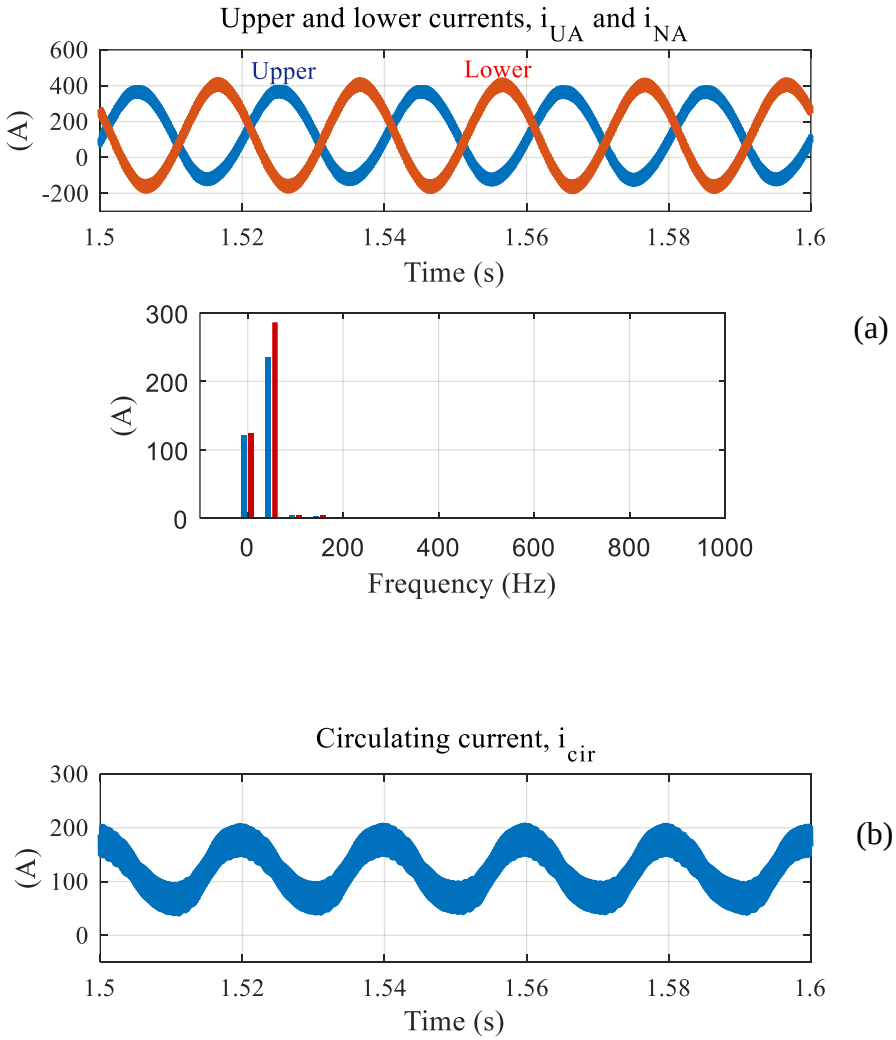


Fig. 4.45: Simulation results using SS technique in case of C_{U1}= 0.8C_{N1}: a) the upper and lower arm currents and their harmonic spectrum, and b) the circulating current.

The output voltage and current waveform are shown in Fig. 4.46 and are highlighted by the FFT spectrum shown in Fig. 4.47, where the fundamental voltage and current components are not affected and at their expected values and no distortion is observed their waveforms, only insignificant 2nd order harmonic component has appeared in the harmonic spectrum.

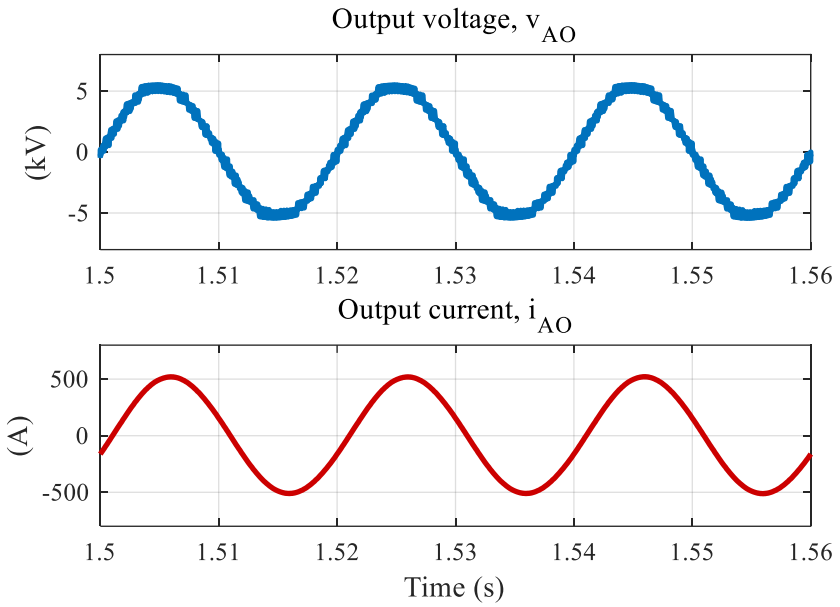


Fig. 4.46: The output voltage and current when using SS technique in case of C_{U1}= 0.8C_{N1}.

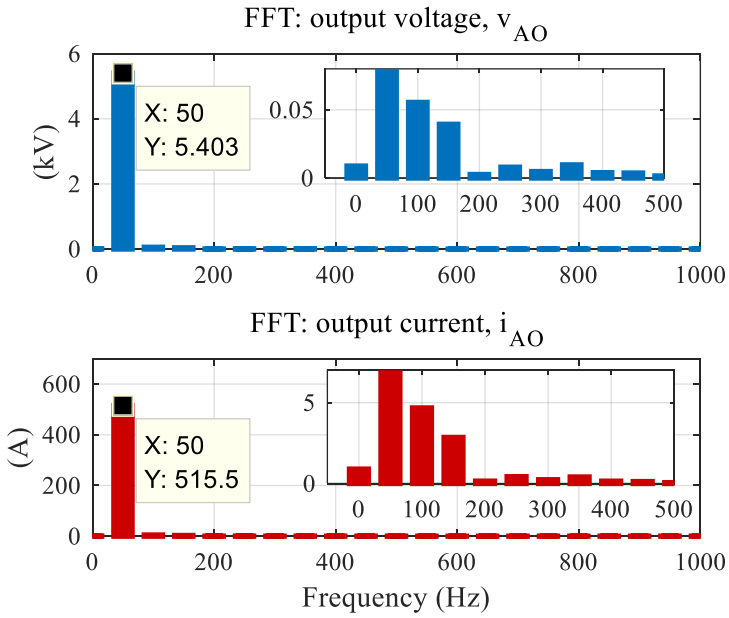


Fig. 4.47: Harmonic spectrum of the output voltage and current when using SS technique in case of C_{U1}= 0.8C_{N1}.

For the same asymmetry in capacitance, Fig. 4.48 shows the simulation results of the qZS-MMC with employing the fundamental circulating current controller. Both the upper and lower qZS capacitor voltages, and the upper and the lower SMs capacitor voltages are well balanced. It is noted that, the peak to peak ripple of v_{CN1} is 80% of that of v_{CU1}.

The fundamental component of the upper and the lower arm currents are equal as shown in Fig. 4.49a and the fundamental frequency component in the circulating current is approximately zero as shown in Fig. 4.49b.

The output voltage and current waveform and their FFT spectrum are shown in Fig. 4.50 and Fig. 4.51 respectively, where the fundamental voltage and current components are not affected and at their expected values, and the harmonic spectrum is free from the 2nd order harmonic component as shown in Fig. 4.51.

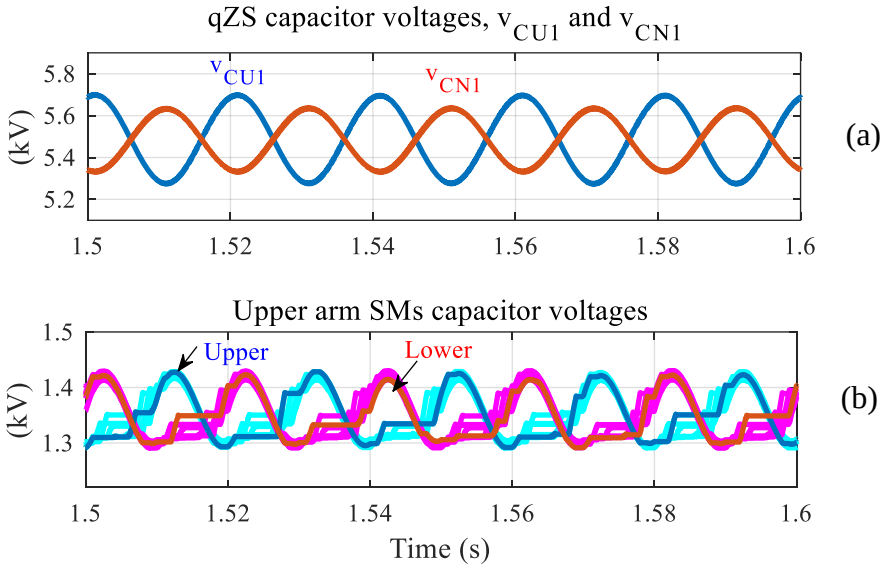


Fig. 4.48: Simulation results using SS technique in case of C_{U1}= 0.8C_{N1} when employing the fundamental frequency circulating current controller: a) the qZS capacitor voltages v_{CU1} and v_{CN1}, and b) the upper (blue) and lower (red) arm SMs capacitor voltages at N_{SM} = 8

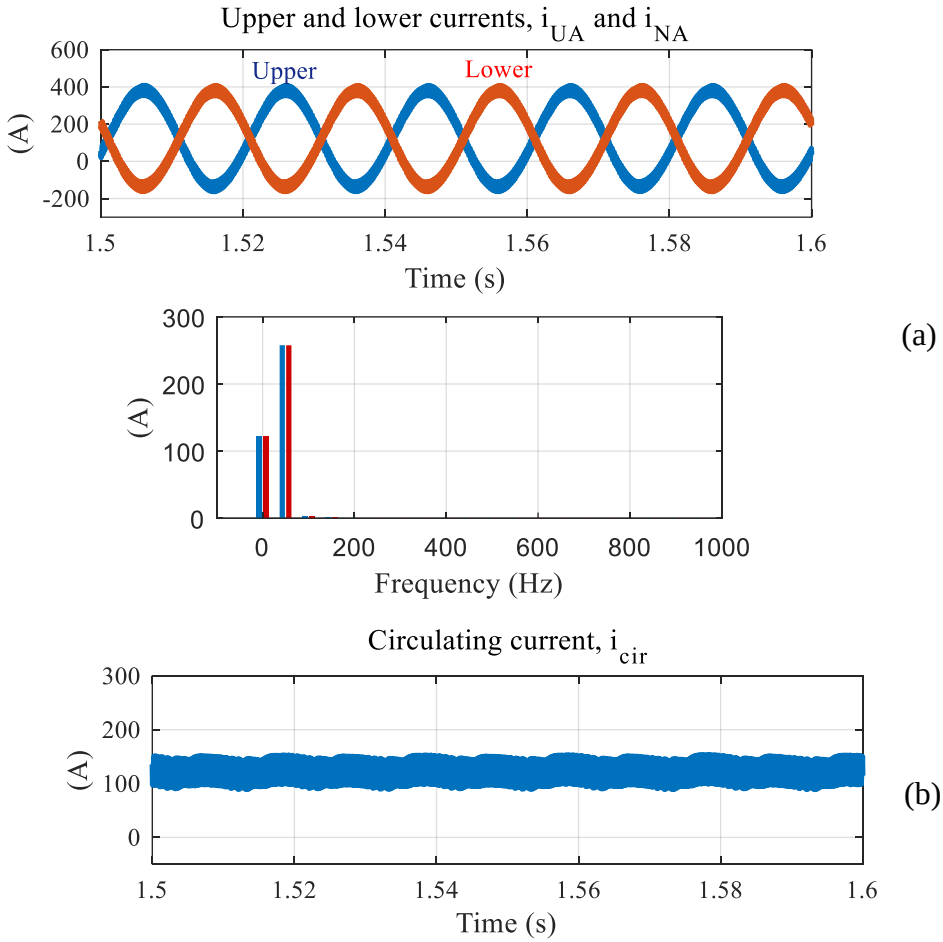


Fig. 4.49: Simulation results using SS technique in case of C_{U1}= 0.8C_{N1} when employing the fundamental frequency circulating current controller: a) the upper and lower arm currents and their spectrum, and b) the circulating current.

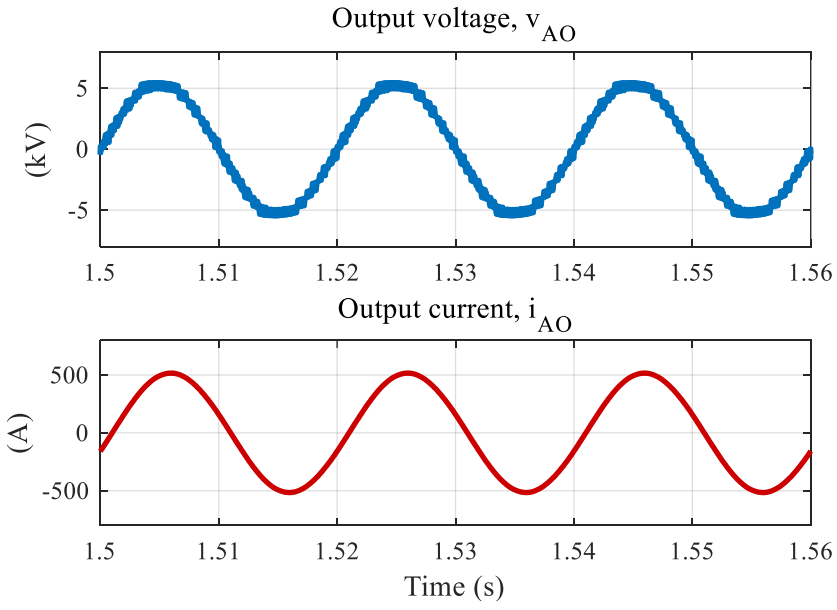


Fig. 4.50: The output voltage and current when using SS technique in case of C_{U1}= 0.8C_{N1} when employing the fundamental frequency circulating current controller.

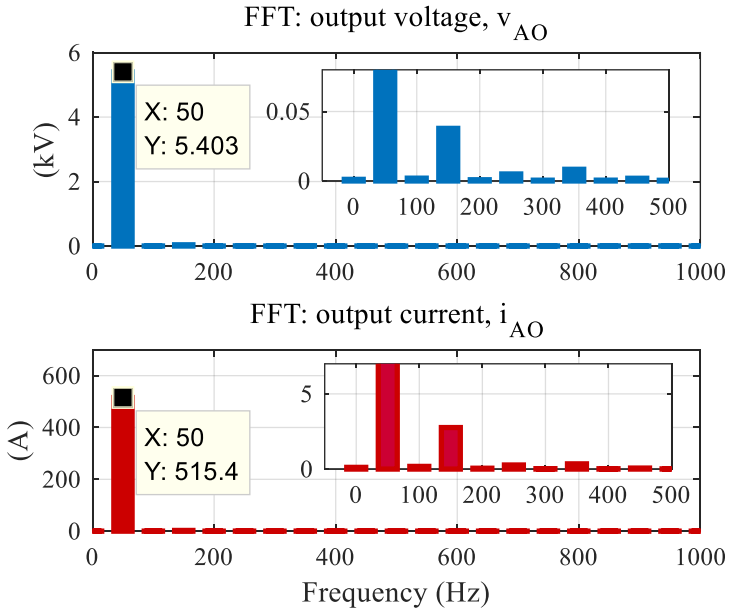


Fig. 4.51: Harmonic spectrum of the output voltage and current when using SS technique in case of C_{U1}= 0.8C_{N1} when employing the fundamental frequency circulating current controller.

4.7.3.2 C_{SM} (upper) = 0.8C_{SM} (lower)

In the second simulation case, it is assumed that each SM capacitance in the upper arm has an error of -10% in their values, while those of the lower arm has an error of +10%. Therefore, the upper and lower arm capacitances are mismatched such that C_{SM} (upper) = 0.8 C_{SM} (lowers). Fig. 4.52 shows the qZS capacitor voltages v_{CU1} and v_{CN1} and the upper and lower SMs capacitor voltages, where it is observed that there is an imbalance between them.

In addition, there is a fundamental frequency component error between the upper and the lower arm currents as indicated by their FFT, which are shown in the Fig. 4.53a. The fundamental frequency component appears in the circulating current as shown in Fig. 4.53b.

By employing the fundamental frequency circulating current controller, the qZS capacitor voltages and the upper and lower SMs capacitor voltages are well balanced as shown in Fig. 4.54. The fundamental component in the upper and the lower arm currents are equal and the fundamental frequency component in the circulating current is approximately zero as shown in Fig. 4.55.

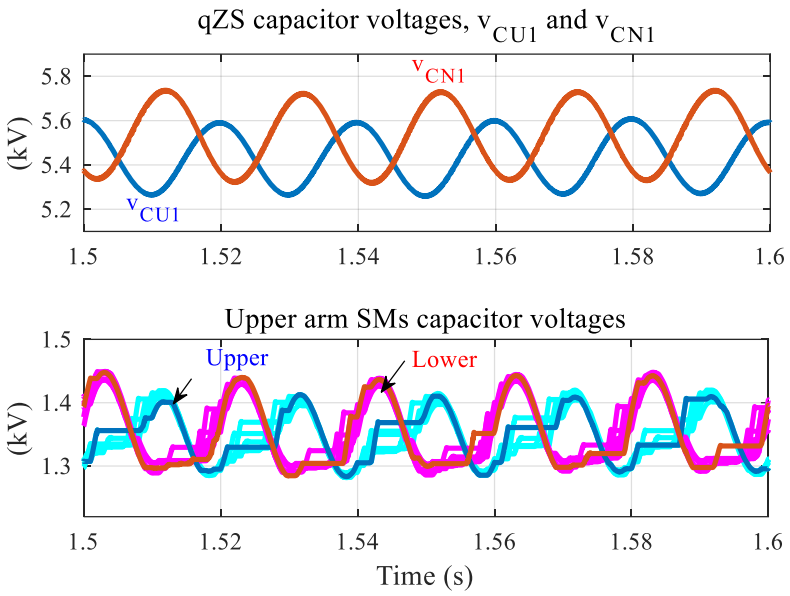


Fig. 4.52: Simulation results using SS technique in case of C_{SM} (upper) = 0.8C_{SM} (lower): a) the qZS capacitor voltages v_{CU1} and v_{CN1}, and b) the upper (blue) and lower (red) arm SMs capacitor voltages at N_{SM} = 8

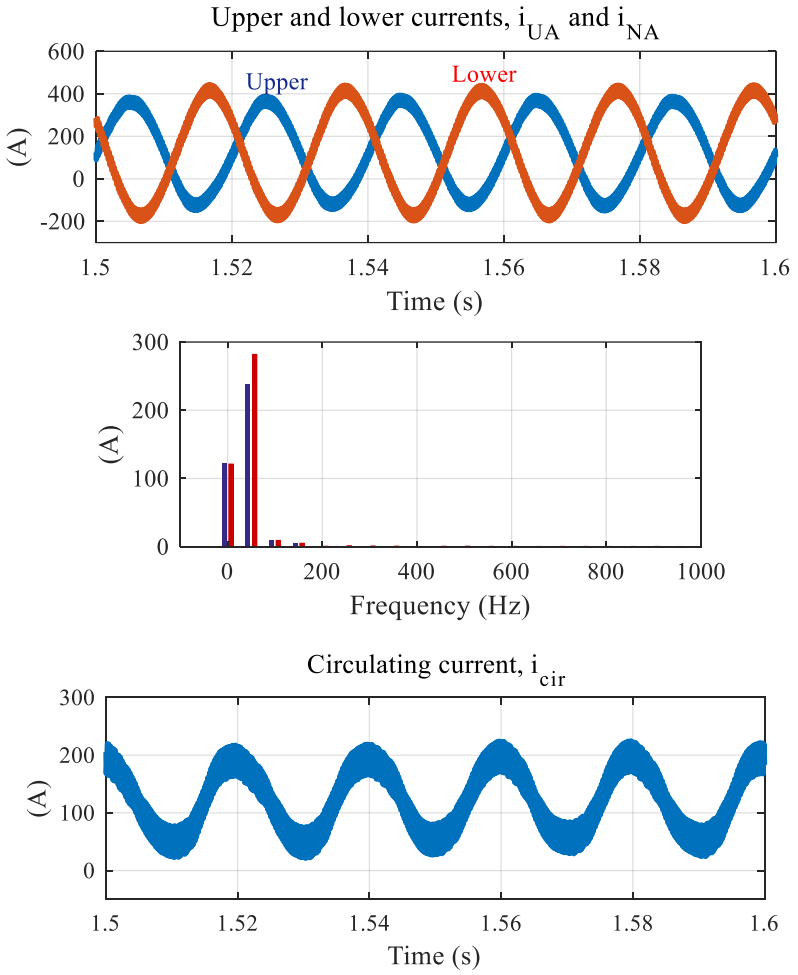


Fig. 4.53: Simulation results using SS technique in case of C_{SM} (upper) = 0.8C_{SM} (lower): a) the upper and lower arm currents and their harmonic spectrum, and b) the circulating current.

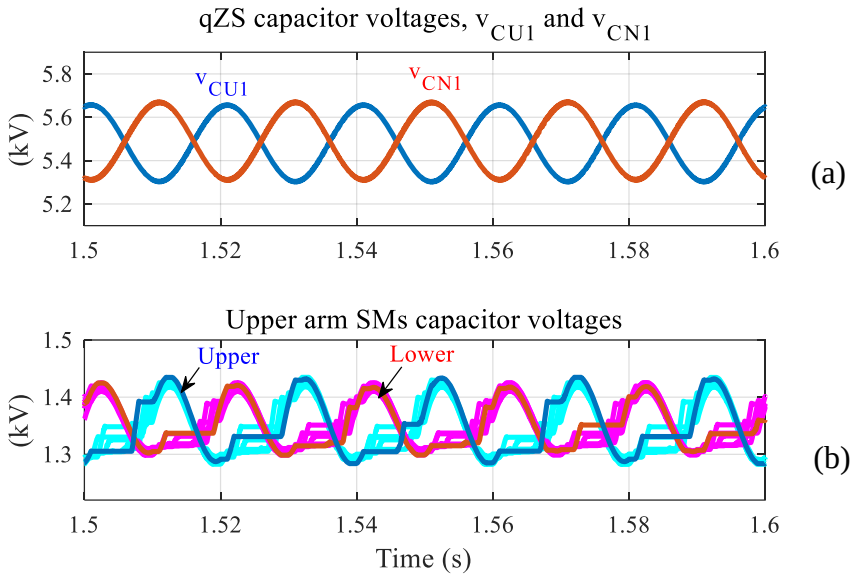


Fig. 4.54: Simulation results using SS technique with C_{SM} (upper) = 0.8C_{SM} (lower) when employing fundamental frequency circulating current controller: a) the qZS capacitor voltages v_{CU1} and v_{CN1}, and b) the upper (blue) and lower (red) arm SMs capacitor voltages at N_{SM} = 8

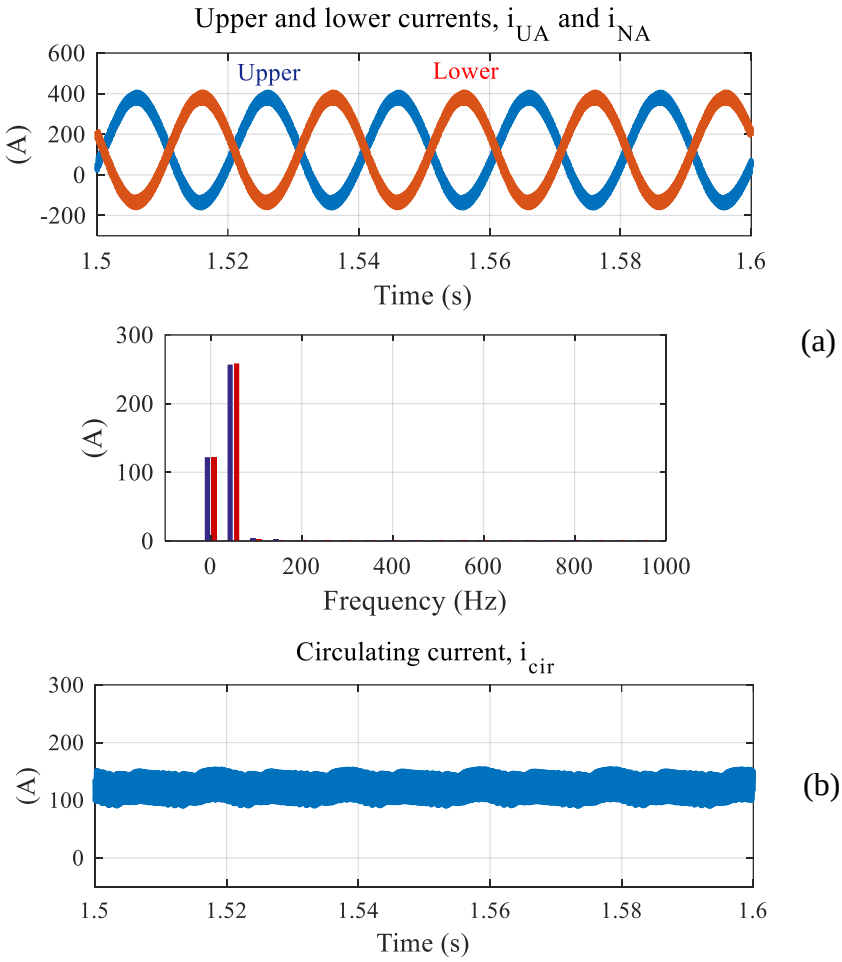


Fig. 4.55: Simulation results using SS technique with C_{SM} (upper) = 0.8C_{SM} (lower) when employing fundamental frequency circulating current controller: a) the upper and lower arm currents and their spectrum, b) the circulating current.

4.8 Conclusions

The HBSM based MMC can generate AC output voltage with a peak fundamental amplitude limited to the half of the DC-link voltage. In this chapter, the impedance network concept has been integrated with the HBSM based MMC in order to extend the output voltage range beyond the half of the DC-link voltage i.e. allowing operation in voltage boosting mode. The operation principle of the quasi Z-source MMC has been presented. Two modulation techniques, the simultaneously shorted (SS) and the reduced inserted cells (RICs) have been proposed and compared with each other. The relation between the ST duty ratio and converter gain, has been deduced for both techniques with illustrating the SMs capacitor voltage relation according to the DC-link voltage.

In addition, it has been proved that using series diode in the qZS-network, causes an undesired mode to appear, where the diode will not be conducting during the whole NST mode interval. This leads to a reduction in the peak value of the DC-link voltage and consequently this causes a disturbance in the output voltage. This problem has been solved by connecting an antiparallel IGBT with the series diode and this was validated by simulation results.

The circulating current in qZS-MMC may contain 2^{nd} order harmonic component, which may bring additional losses and current stress on the arm switches. Thus, a control scheme is presented to suppress this component in the circulating current. Due to asymmetry between passive components in the upper and lower arm of the MMC and the qZS-networks, a fundamental frequency error current component appeared in the circulating current. By adding a suitable controller, this has been also well controlled/minimised to maintain stable operation.

Relevant simulation cases have been presented to validate the proposed concepts and show the effectiveness of the proposed modulation techniques in allowing the converter to operate in both voltage buck and voltage boost modes.

Chapter 5
Converter Sizing and Losses Estimation

In this chapter, systematic design guidelines for sizing the passive elements (capacitors and inductors) used in the proposed topology are provided for the two modulation techniques described in Chapter 4. Also, analytical expressions for estimating the semiconductor losses that include the conduction and switching losses, are presented. Simulation studies are presented to validate the effectiveness of the proposed analytical analysis. Finally, the use of this converter in a typical industrial application is investigated.

5.1 Sizing of the qZS-MMC components

The proposed topology relies on a large number of passive components, which may affect the power density: the qZS-network inductors and capacitors, the MMC arm inductors, and the SMs capacitors. For this reason, sizing appropriately the inductors and capacitors is an important task in the design of the converter that requires in depth investigations. Relevant studies were identified for the individual parts of the qZS-MMC including qZS-network sizing [72, 107] and MMC side sizing [6, 108]. These studies have been considered as the initial steps toward sizing of the proposed qZS-MMC.

A detailed analysis to enable derivation of analytical formulae to estimate the needed size of the different components is presented in this section.

5.1.1 Capacitors

The capacitors account for a large fraction of the overall volume and weight of both the SMs and the qZS-networks. In this section, the expressions for determining the capacitance requirements for the SMs and for the qZS-network are derived analytically to ensure an acceptable capacitor voltage ripple. To simplify the analysis, it is assumed that the power losses of the converter are considered insignificant.

5.1.1.1 SMs capacitors sizing

Due to symmetrical structure of the upper and lower arm, the capacitor ripple voltage is similar for both arms and for this reason, only the upper arm is considered in the analysis. The energy variation of the arms needs to be firstly deduced and consequently a quantitative design of the SM capacitance can be provided for each technique.

A. Sizing SM capacitors when using the SS technique

The passive component size calculation starts by analyzing the instantaneous power in the arm that can be calculated as a product of the arm voltage and arm current. By using (4.16) and (4.19) for the SS technique, the instantaneous arm power can be expressed as (5.1).

$$\begin{aligned} P(\omega\cdot t) &= v_{UA}(\omega\cdot t)\cdot i_{UA}(\omega\cdot t) \\ &= S\cdot\left[\sin(\omega\cdot t-\varphi)-\frac{m^2}{2}\cos\varphi\cdot\sin\omega\cdot t+\frac{m}{2}\cos(2\omega\cdot t-\varphi)\right] \end{aligned} \tag{5.1}$$

where $S = V_m \cdot I_m / 2$, is the apparent power. By integrating (5.1), the energy variation of the upper arm can be expressed by:

$$\begin{aligned} &\Delta E(\omega\cdot t) = \\ &\frac{S}{\omega}\cdot\left[-\cos(\omega\cdot t-\varphi)+\frac{m^2}{2}\cdot\cos\varphi\cdot\cos(\omega\cdot t)+\frac{m}{4}\cdot\sin(2\omega\cdot t-\varphi)\right] \end{aligned} \tag{5.2}$$

To calculate the peak to peak energy ΔE_{PP}, the zero crossing points of the arm power should be calculated. There are only two zero crossing points at θ_1 and θ_2 which are the same as the upper arm current zero-crossing points. Using (4.19) for i_{UA}, θ_1 and θ_2 are given by:

$$\begin{aligned}\theta_1 &= \pi + \sin^{-1}(m \cdot \cos\varphi / 2) - \varphi \\ \theta_2 &= 2\pi - \sin^{-1}(m \cdot \cos\varphi / 2) - \varphi\end{aligned} \tag{5.3}$$

By substituting (5.3) into (5.2), ΔE_{PP} can be derived as:

$$\Delta E_{PP} = \int_{\theta_2}^{\theta_1} \Delta E(\omega \cdot t) = \frac{2 \cdot S}{\omega} \sqrt[3/2]{1 - (\frac{m \cdot \cos\varphi}{2})^2} \tag{5.4}$$

Assume k_v is the capacitor voltage ripple factor, the SMs capacitor voltage is varying from (1+ k_v/2) V_{CSM} to (1- k_v/2) V_{CSM}. The relation between the minimum capacitance value and the upper arm energy ΔE_{pp} can be expressed by:

$$C_{SM} = \frac{\Delta E_{PP}}{k_v \cdot N_{SM} \cdot V_{CSM}^2} \tag{5.5}$$

From (4.12), (4.14), (5.4) and (5.5), the SM capacitance value when using the SS technique can be derived as:

$$C_{SM} = \frac{2 \cdot N_{SM} \cdot S}{k_v \cdot \omega \cdot G^2 \cdot V_{DC}^2} \sqrt[3/2]{1 - (\frac{m \cdot \cos\varphi}{2})^2} \tag{5.6}$$

B. Sizing SM capacitors when using the RICs technique

Using (4.26) and (4.34), the instantaneous arm power and the arm energy variation when using the RICs technique can be derived as (5.7) and (5.8).

$$\begin{aligned}P(\omega t) = {} & v_{UA}(\omega \cdot t) \cdot i_{UA}(\omega \cdot t) = \\ & S \cdot \left[(1 - D_{sh}) \cdot \sin(\omega \cdot t - \varphi) - m_{RIC} \cdot (m - \frac{4 \cdot D_{sh}}{\pi}) \cdot \frac{\cos\varphi \cdot \sin\omega \cdot t}{2} \right. \\ & \left. + (m - \frac{4 \cdot D_{sh}}{\pi}) \cdot \frac{\cos(2 \cdot \omega t - \varphi)}{2} \right]\end{aligned} \tag{5.7}$$

$$\Delta E(\omega \cdot t) = \frac{S}{\omega} \cdot \left[-(1-D_{sh}) \cdot \cos(\omega \cdot t - \varphi) + m_{RIC} \cdot (m - \frac{4D_{sh}}{\pi}) \cdot \frac{\cos\varphi \cdot \cos\omega \cdot t}{2} + (m - \frac{4 \cdot D_{sh}}{\pi}) \cdot \frac{\sin(2 \cdot \omega \cdot t - \varphi)}{4} \right] \quad (5.8)$$

The zero crossing points of the arm power are the same as the upper arm current zero-crossing points. Using (4.34) for i_{UA}, θ_1 and θ_2 are given by:

$$\theta_1 = \pi + \sin^{-1}(m_{RIC} \cdot \cos\varphi / 2) - \varphi$$
$$\theta_2 = 2\pi - \sin^{-1}(m_{RIC} \cdot \cos\varphi / 2) - \varphi \quad (5.9)$$

where m_{RIC} is defined by (4.33). By substituting (5.9) into (5.8), ΔE_{PP} can be derived as (5.10) and expressed as a function of the gain G given in (4.29) by (5.11).

$$\Delta E_{pp} = \frac{2S(1-D_{sh})}{\omega} \sqrt[3/2]{1-(\frac{m_{RIC}\cos\varphi}{2})^2} \quad (5.10)$$

$$\Delta E_{PP} = \frac{S(G+1)}{\omega G} \sqrt[3/2]{1-(\frac{m_{RIC}\cos\varphi}{2})^2} \quad (5.11)$$

From (5.5) and (5.11), the minimum SM capacitance value when using the RICs technique can be derived as (5.12).

$$C_{SM} = \frac{N_{SM}(G+1)S}{k_v \omega G^3 V_{DC}^2} \sqrt[3/2]{1-(\frac{m_{RIC}\cos\varphi}{2})^2} \quad (5.12)$$

C. Comparing size of SMs capacitors for SS and RIC

The MMC arm normalized energy variation waveform $\Delta E(\omega \cdot t) \cdot \omega / 2S$, which are defined by (5.2) and (5.8) when using the SS and RICs technique respectively, is shown in Fig. 5.1a and Fig. 5.1b for SS and RICs respectively at m = 1, cos φ = 1. It is noted that the energy variation waveform is only dependent on the modulation index m and the power factor cos φ for the SS technique whilst for the RICs, it depends also on the converter ST duty ratio D_{sh}.

The peak value of energy variation decreases with increasing D_{sh} when using the RICs technique. The normalized energy variation waveform is redrawn at m = 1, cos φ = 0.6 in Fig. 5.2a and Fig. 5.2b for SS and RICs techniques respectively. Comparing Fig. 5.1 to Fig. 5.2, the peak value of energy variation decreases with increasing cos φ for both modulation techniques and consequently smaller capacitor size is needed.

Fig. 5.3 shows the normalized maximum energy ΔE_{PP}*(ω/2S) versus the gain for both techniques at three values of cos φ of 0.6, 0.8 and 1 and unity m. It is noted that using the RICs technique with increasing the converter gain, a reduced maximum energy ΔE_{PP} and consequently smaller capacitor size is needed. The maximum energy ΔE_{PP} when using the RICs technique is reduced by 18% compared to the SS technique at G equals 2 and unity cos φ.

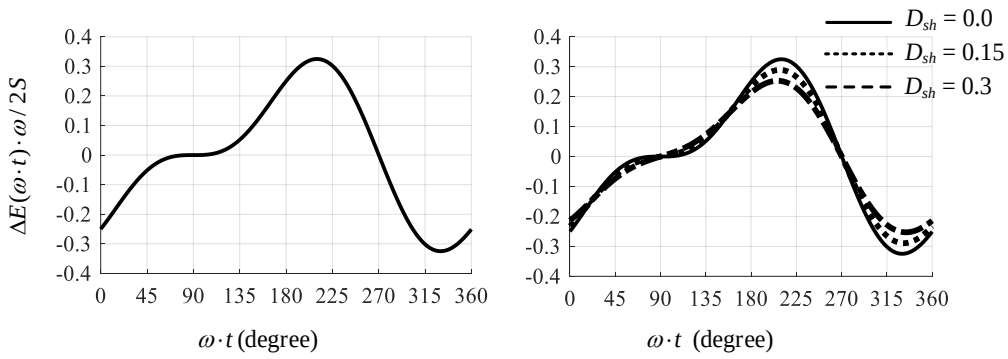


Fig. 5.1: The normalized energy variation ΔE_{PP} for a) the SS technique and b) the RICs technique at m = 1 and cos φ = 1

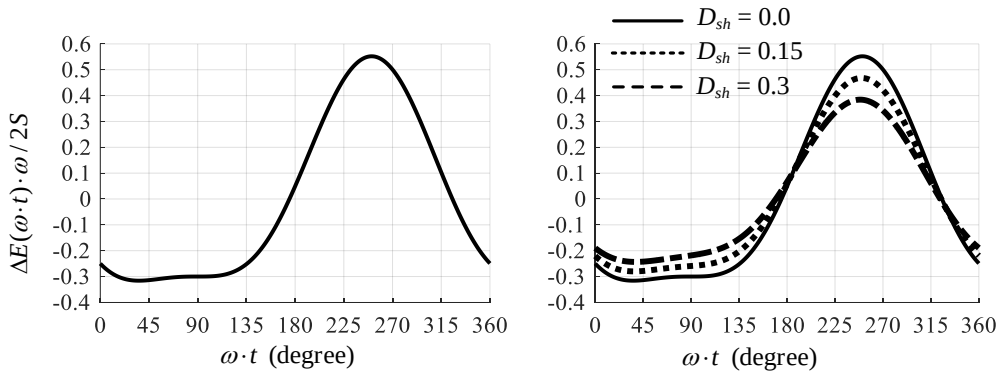


Fig. 5.2: The normalized energy variation ΔE_{PP} for a) the SS technique and b) the RICs technique at m = 1 and cos φ = 0.6

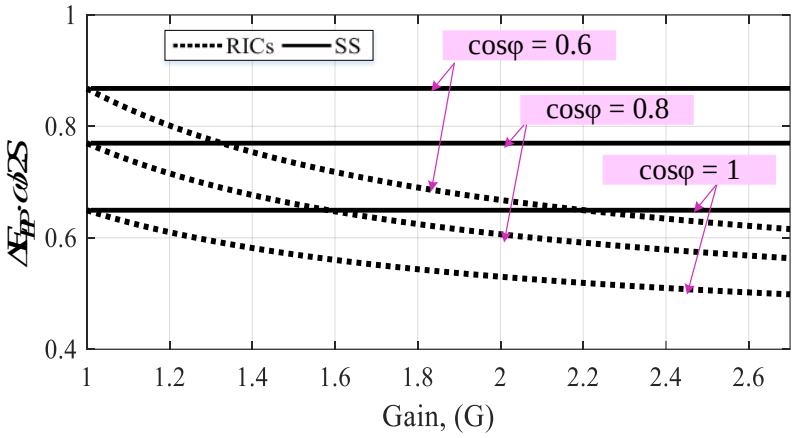


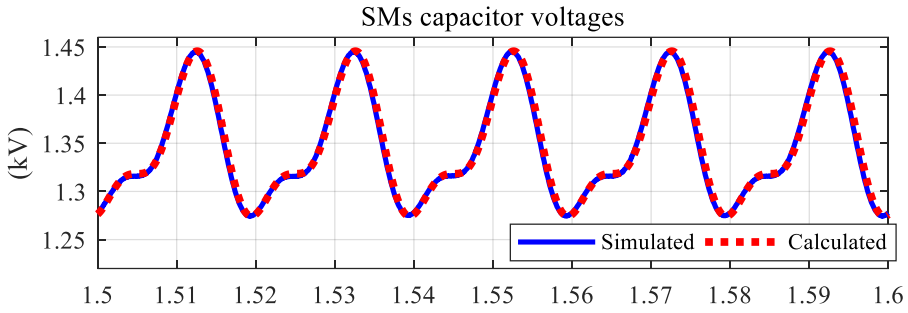
Fig. 5.3: Comparison of the normalized maximum energy ΔE_{PP} versus gain G for the SS and RICs techniques at cos φ = 0.6, 0.8, and 1

According to $\Delta E(\omega t) = N_{SM}(C_{SM} \cdot v_{CSM}^2(\omega t) - C_{SM} \cdot V_{CSM}^2)/2$ and using (4.12) and (5.2) for the SS technique, and (4.21) and (5.8) for the RICs technique, the SMs capacitor voltage waveform can be obtained using (5.13).

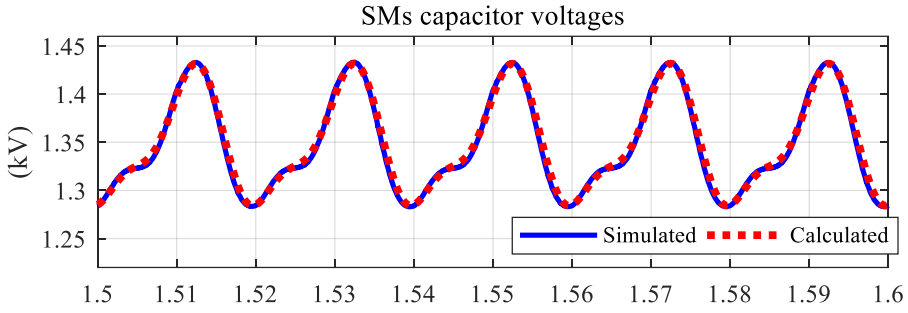
$$v_{CSM}(\omega t) = \sqrt{\frac{2\Delta E(\omega t)}{N_{SM} C_{SM}} + V_{CSM}^2} \tag{5.13}$$

where V_{CSM} is the average value of the SMs capacitor voltage.

To verify the above analytical model, the simulation model used in section 4.7 is used with a G = 1.5, N_{SM} = 8, C_{SM} = 3.3 mF, S = 1.5 MVA, and cos φ = 0.95. Fig. 5.4a and Fig. 5.4b compare the calculated capacitor voltage obtained by (5.13) and the SM capacitor voltage resulted from the simulation model for the SS and RICs techniques respectively. The average SM capacitor voltage value is 1.36 kV. It can be noted that the calculated and simulated waveforms are well matched and that the RICs technique introduced a lower ripple in SM capacitor voltage compared with the SS technique as predicted by the analytical model.



(a)



(b)

Fig. 5.4: Simulated and calculated SMs capacitor voltage for a) SS technique, and b) RICs technique

5.1.1.2 qZS-network capacitors sizing

The upper and lower qZS-network components are identical. Therefore, only the upper qZS-network is considered to estimate the capacitance requirements for the qZS-networks.

A. Sizing qZS capacitors when using the SS technique

The upper qZS capacitor current i_{CUI} waveform is shown in Fig. 5.5 where capacitor current equals to (4.7) during ST mode and equals to (4.8) during NST mode. Using (4.7) and (4.8), the average value of the capacitor current over a switching period is given by (5.14).

$$i_{CU1}(t) = D_{sh} \cdot I_L + (1 - D_{sh}) \cdot (i_{UA}(t) - I_L) \tag{5.14}$$

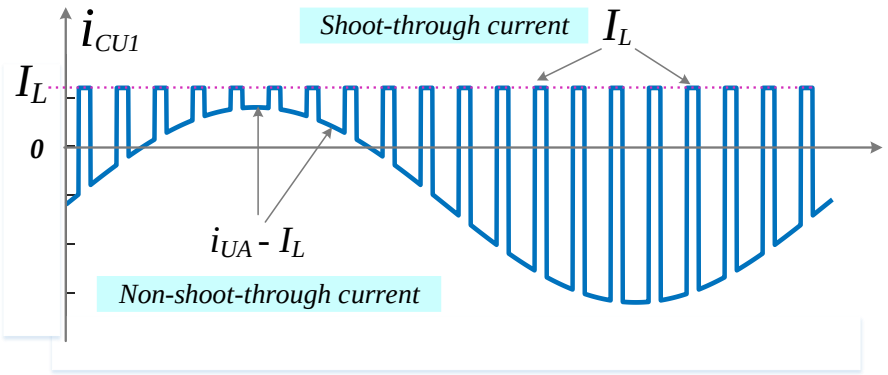


Fig. 5.5: The capacitor current waveform i_{CU1} when using the SS technique

Substituting from (4.18) into (5.14), the capacitor current i_{CU1} over a switching period is given by:

$$i_{CU1}(t) = (1 - D_{sh}) \cdot \frac{I_m}{2} \cdot \sin(\omega \cdot t - \varphi) \tag{5.15}$$

By integrating and using the capacitor current in (5.15), the instantaneous value of the qZS-capacitor voltage ripple Δv_{CU1} is determined:

$$\Delta v_{CU1} = \frac{1}{C_{U1}} \int i_{CU1}(t) \cdot dt = \frac{-(1 - D_{sh}) \cdot I_m}{2 \cdot \omega \cdot C_{U1}} \cos(\omega \cdot t - \varphi) \tag{5.16}$$

To calculate the peak to peak capacitor voltage ripple, the zero crossing points of the capacitor current should be calculated. From (5.15), the upper qZS-network capacitor current zero crossing points θ_1 and θ_2 are identified as:

$$\theta_1 = \varphi \qquad \theta_2 = \pi + \varphi \tag{5.17}$$

Substituting from (4.14), (5.17), into (5.16), the minimum required qZS-capacitance C_{U1} as a function of the gain G is:

$$C_{U1} = \frac{8S}{\omega \cdot k_{v-qZS-SS} \cdot m \cdot G \cdot (2G - 1) \cdot V_{DC}^2} \tag{5.18}$$

Also, the capacitance C_{U2} is given by:

$$C_{U2} = \frac{G}{G - 1} C_{U1} = \frac{8S}{\omega \cdot k_{v-qZS-SS} \cdot m \cdot (G - 1) \cdot (2G - 1) \cdot V_{DC}^2} \tag{5.19}$$

B. Sizing qZS capacitors when using the RICs technique

As discussed earlier in section 4.3.2, the upper/lower qZS-network works only during the NST mode in the positive/negative half cycle of the output voltage waveform where the capacitor current i_{CU1} during this part of the cycle is defined by (4.8). The upper qZS capacitor current i_{CU1} is shown in Fig. 5.6 to illustrate its operation.

By using Fourier series for the capacitor current shown in Fig. 5.6 which contains fundamental, low order harmonic components and switching frequency components, with the fundamental one being the lowest frequency, causes most of the capacitor voltage ripple. The fundamental component of the capacitor current i_{CU1} is derived by (5.20).

$$i_{CU1}(t) = \left[\frac{I_m}{2}\cdot(1-D_{sh}) - \frac{4D_{sh}}{\pi}\cdot(2I_L - I_{UN})\right]\cdot\sin(\omega t - \varphi) \qquad (5.20)$$

Using (4.29), (4.32) and (5.20), the instantaneous value of the qZS-capacitor voltage ripple Δv_{CU1} can be expressed by:

$$\begin{aligned}\Delta v_{CU1} &= \frac{1}{C_{U1}}\int i_{CU1}(t)dt \\ &= \frac{-I_m}{2\omega\cdot C_{U1}}\left(\frac{G+1}{2G} - \frac{G-1}{\pi\cdot G}\cdot(2G\cdot m - m_{RIC}).\cos\varphi\right)\cdot\cos(\omega\cdot t - \varphi)\end{aligned} \qquad (5.21)$$

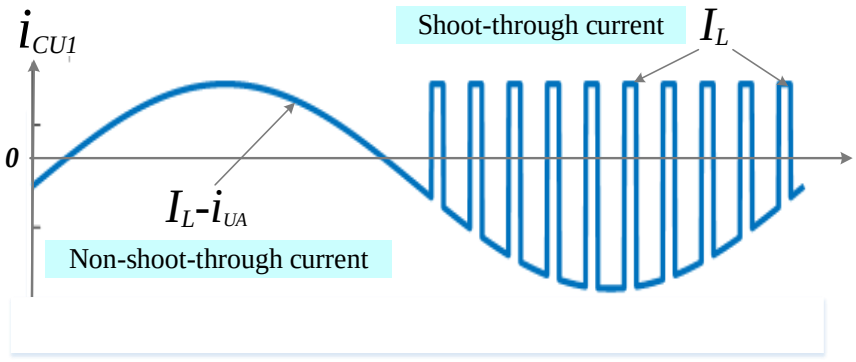


Fig. 5.6: The capacitor current waveform i_{CU1} when using the RICs technique

Substituting from (4.29), (5.17) into (5.21), the minimum qZS-capacitance C_{U1} as a function of the gain G is:

$$C_{U1} = \frac{16S}{\omega \cdot k_{v-qZS-RICs} \cdot G \cdot (G+1) \cdot V_{DC}^2} \times \left(\frac{G+1}{2G} - \frac{G-1}{4\pi \cdot G} \cdot \left(2G \cdot m - m_{RIC}\right).\cos\varphi \right) \tag{5.22}$$

Also, the capacitance C_{U2} is given by:

$$C_{U2} = \frac{G+1}{G-1} C_{U1} = \frac{V_{C1}}{V_{C2}} C_{U1} = \frac{16S}{\omega \cdot k_{v-qZS-RICs} \cdot G \cdot (G-1) \cdot V_{DC}^2} \times \left(\frac{G+1}{2G} - \frac{G-1}{4\pi \cdot G} \cdot \left(2G \cdot m - m_{RIC}\right).\cos\varphi \right) \tag{5.23}$$

In (5.20), it is assumed that the qZS-inductor current is constant and equal to its average value I_L which makes the relations deduced to calculate the qZS-capacitance values for the RICs technique not very accurate due to the presence of the fundamental frequency component in the inductor currents. Therefore, these relations are used as an indicator to approximate the size of the capacitances required.

C. Comparing size of qZS capacitors for SS and RIC

These analytical models allow comparing the capacitance for both modulation techniques and this is drawn versus the gain G and is shown in Fig. 5.7a and Fig. 5.7b for C_{U1} and C_{U2} respectively. The capacitance values have been normalized by dividing (5.18), (5.19), (5.22), (5.23) by $8S / \omega \cdot k_v \cdot V_{DC}^2$, as noted in Fig. 5.7. It can be seen that the required qZS capacitance C_{U2} value for the RICs technique is higher than that for the SS technique. However, the required capacitance C_{U1} value is approximately the same for both modulation techniques.

However, due to different operating voltages that result in different voltage peaks for the capacitors in both techniques, the stored energy in each capacitor should be derived to have a fair comparison. The maximum energy E_{CU1} and E_{CU2} in the qZS capacitors C_{U1} and C_{U2} are determined by (5.24) for SS technique and by (5.25) for RICs technique.

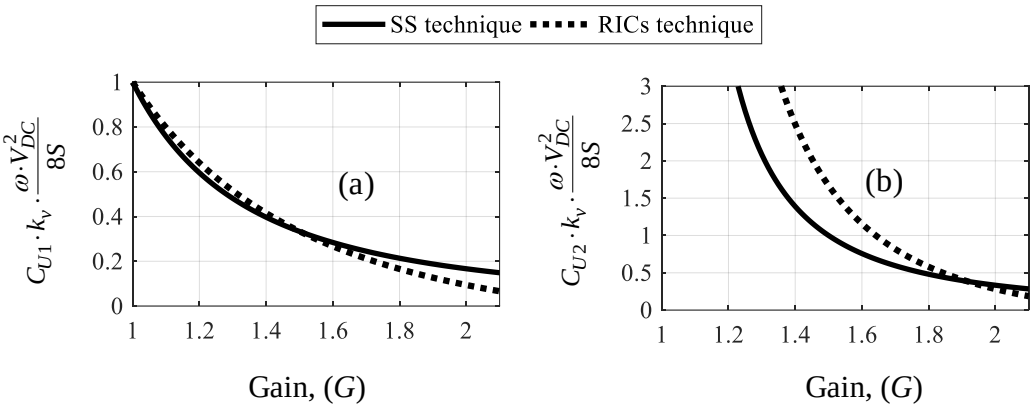


Fig. 5.7: The variation of qZS normalized capacitances C_{U1} and C_{U2} at cos φ = 1 and m = 1.

$$E_{CU1} = C_{U1} \cdot k_v \cdot V_{C1}^2 = \frac{2 \cdot S \cdot G}{\omega \cdot m \cdot (2G-1)}$$
$$E_{CU2} = C_{U2} \cdot k_v \cdot V_{C2}^2 = \frac{2 \cdot S \cdot (G-1)}{\omega \cdot m \cdot (2G-1)} \tag{5.24}$$

$$E_{CU1} = C_{U1} k_v V_{C1}^2$$
$$= \frac{S \cdot (G+1)}{\omega \cdot G}\left(\frac{G+1}{2G} - \frac{G-1}{4\pi G} \cdot \left(4G - m_{RIC}\right).\cos\varphi\right) \tag{5.25}$$
$$E_{CU2} = C_{U2} k_v V_{C2}^2$$
$$= \frac{S \cdot (G-1)}{\omega \cdot G}\left(\frac{G+1}{2G} - \frac{G-1}{4\pi G} \cdot \left(4G - m_{RIC}\right).\cos\varphi\right)$$

The maximum energy variations for the two qZS capacitors E_{CU1} and E_{CU2} are drawn versus the gain G at $m=1$ and cos φ =1 and are shown in Fig. 5.8a and Fig. 5.8b respectively. It is noted that, the energy E_{CU1} and E_{CU2} are lower for RICs technique compared to SS technique for the whole gain range.

The total maximum energy for the qZS-network can be estimated by direct summation of $E_{CU1} + E_{CU2}$ which is shown in Fig. 5.9. For the SS technique, the total maximum capacitor energy is independent on the power factor cos φ and gain G whilst for the RICs technique, the total maximum capacitor energy is

smaller and decreases when increasing the gain G and increasing the power factor cos φ.

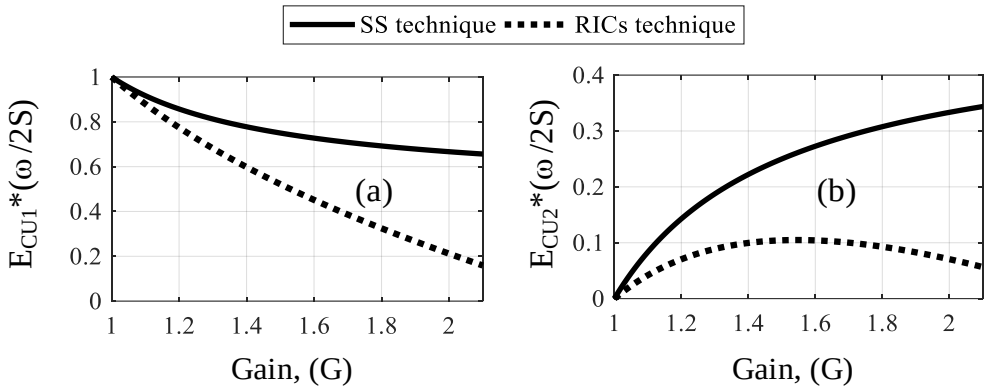


Fig. 5.8: The variation of normalized energy E_{CU1} and E_{CU2} at cos φ = 1 and m = 1

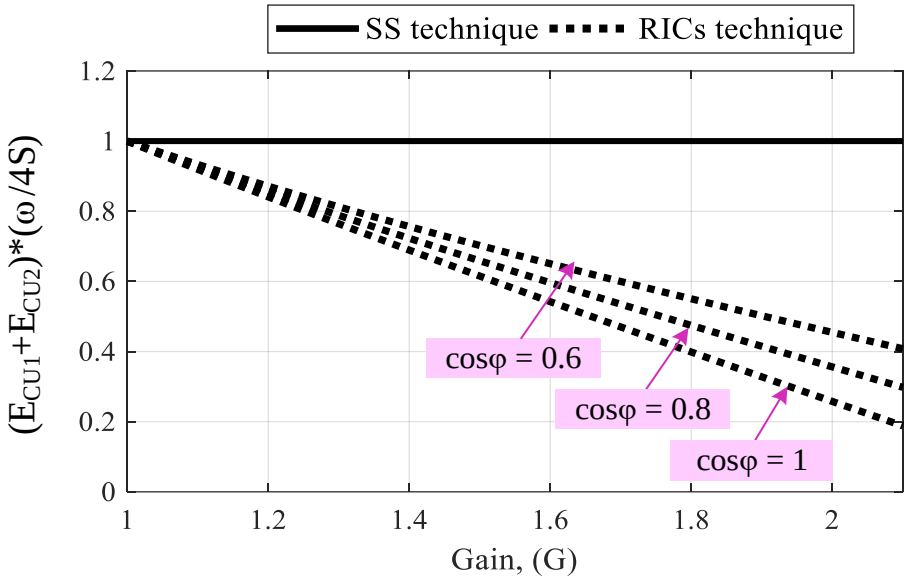


Fig. 5.9: The variation of the total normalized capacitor energy E_{CU1} + E_{CU2} versus gain G at cos φ = 0.6, 0.8, and 1 for both modulation techniques

According to the simulation model presented in section 4.7, which used N_{SM} =8, G = 1 (the SMs capacitance decreases when increasing the gain), V_{DC} = 11 kV, S = 1.5 MVA, K_v = 15%, cos φ = 0.95 and m = 1, therefore based on (5.6) and (5.18) for SS technique, and (5.12) and (5.22) for RICs technique, C_{SM} and C_{U1} need to satisfy:

$$\begin{aligned} C_{SM} &> 2.75\ \text{mF} \\ C_{U1} &> 2.02\ \text{mF} \end{aligned} \tag{5.26}$$

Therefore, the value of capacitances C_{SM} and C_{U1} of 3.3 mF has been selected and were used in all the simulations from Section 4.7.

Referring to the simulation results for qZS capacitor voltages given in Fig. 4.34 and Fig. 4.35 at gain value of 1.5, 8 SMs per arm and 0.95 power factor, the peak to peak capacitor voltage ripple factor k_v can be calculated that used 3.3 mF SM capacitance. Using the same qZS capacitance of 3.3 mF, the ripple factor for V_{CU1} (or V_{CN1}) is the same for both modulation methods, at 7% (0.39 kV/5.47 kV for the SS technique and 0.32 kV/4.58 kV for RICs technique), which matches the analytical curve given in Fig. 5.7a at G = 1.5. On the other hand, the ripple factor for V_{CU2} (or V_{CN2}) is $k_{v\text{-}qZS\text{-}SS}$ = 0.2 kV/1.8 kV = 0.11 and $k_{v\text{-}qZS\text{-}RICs}$ = 0.19 kV / 0.9 kV = 0.21 for the SS and RICs techniques respectively, with a ratio of $k_{v\text{-}qZS\text{-}SS}$ / $k_{v\text{-}qZS\text{-}RICs}$ = 0.11/0.21 = 0.52, which is slightly lower than the ratio 1/1.7 = 0.58 calculated theoretically from Fig. 5.7b at the same qZS capacitances.

5.1.2 Inductors

5.1.2.1 Arm inductor sizing

The arm inductors, which are connected in series with the SMs in each arm, are used to limit the circulating current that can be generated as a result of the instantaneous voltage difference between the DC-link voltage and the two arms voltages [109]. In addition, the arm inductors are used to limit the fault current in case of a DC-link fault [110].

This circulating current normally contains, besides switching frequency components which are easily limited by the high corresponding impedance of the inductance, also 2nd order harmonic components which circulate through the upper and lower arm and are not so easy to limit due to the lower impedance (frequency). The circulating current controller can be employed to suppress the 2nd order harmonic in the circulating current to a negligible level. The suppression control that is being employed was discussed in section 4.5. Therefore, the arm inductors are selected to reduce the switching ripple of the circulating current caused by the switching of the power semiconductor devices [109]. So, the main criteria for choosing the arm inductance is to limit the

switching ripple that circulate through the two arms. Referring to (3.8), the fluctuation and switching in the upper and lower arm voltages cause ripple in the circulating current i_{cir} and does not effect on the output voltage.

According to (3.8) for traditional MMC [111], the maximum voltage applied across the two arm inductors equals to V_{CSM} as a result of switching on/off one SMs at each switching frequency cycle. In this work, according to (4.10), shooting through the upper and the lower DC-links together when using the SS technique results in the maximum voltage applied across the arm inductors equals (N_{SM} +1) V_{CSM}. However, using the RICs technique results in maximum arm inductor voltages similar to the case of traditional MMC and equals to V_{CSM} according to (4.22).

A. Sizing arm inductors when using the SS technique

In order to estimate the required arm inductance, it is important to calculate the voltage applied across the arm inductor during ST or NST modes. According to (4.10) and Fig. 4.7, the DC-link voltages are set to zero and the voltage across the arm inductor during ST mode is given by:

$$v_{LO}(t) = -\left(v_U(t) + v_N(t)\right)/2 \tag{5.27}$$

Since the total number of inserted SMs in the phase leg are changed between N_{SM} -1, N_{SM} and N_{SM} +1 with total average of N_{SM} utilized through a carrier frequency period, the maximum value of the arm inductor voltage that is produced during the ST mode is given by (5.28) and it is used to estimate the required arm inductance.

$$v_{LO} = (N_{SM} + 1) \cdot V_{CSM} / 2 \tag{5.28}$$

Based on (3.8) and (5.28), and neglecting the arm equivalent resistance r_o, and considering that V_{UN} equals zero during ST mode, the switching ripple of the circulating current i_{cir} can be estimated based on:

$$L_O \frac{di_{cir}}{dt} = L_O \frac{\Delta i_{cir}}{\Delta t} = -\frac{v_U(t) + v_N(t)}{2} \simeq (N_{SM} + 1) \cdot V_{CSM} / 2 \tag{5.29}$$

Therefore, over the ST interval of $D_{sh}*T$, a voltage of (5.28) is put on each arm inductor. Therefore, the peak to peak ripple of i_{cir} is given by:

$$\Delta i_{cir} = \frac{D_{sh} \cdot (N_{SM} + 1) \cdot V_{CSM}}{2 f_c \cdot L_o} \tag{5.30}$$

Let's define $k_{i\text{-}arm\text{-}SS}$ as the ratio of arm current ripple when using SS technique. The arm inductance can be calculated by:

$$L_O = \frac{D_{sh} \cdot (N_{SM} + 1) \cdot V_{CSM}}{2 f_c \cdot k_{i-arm-SS} \cdot I_{UN}} \tag{5.31}$$

Substituting from (4.12), (4.14), and (4.18) into (5.31), the arm inductance as a function of the gain G, when using the SS technique, is given by:

$$L_O = \frac{m.(G-1) \cdot G^2 \cdot (N_{SM} + 1) \cdot V_{DC}^2}{2 f_c \cdot k_{i-arm-SS} \cdot (2G-1) \cdot \cos\varphi \cdot N_{SM} \cdot S} \tag{5.32}$$

B. Sizing arm inductors when using the RICs technique

This technique depends on gating only one of the upper or the lower chain-link switches with reducing the number of inserted SMs by $N_{SM}/2$ in the corresponding arm during the ST mode. As a result and according to (4.22), (4.26), and (4.27), the maximum arm inductor voltage always equals V_{CSM} during ST mode and also during NST mode (which is similar to traditional MMC [111]). For simplification, the switching states of the MMC leg change twice every carrier frequency cycle T, which are due to inserting and bypassing one SM from each arm. Accordingly, a voltage of $V_{CSM}/2$ is put on each arm inductor over an interval of $T/2$. Therefore, the peak to peak ripple of i_{cir} is given by:

$$\Delta i_{cir} = \frac{V_{CSM}}{4 f_c \cdot L_O} \tag{5.33}$$

The arm inductance can be calculated by:

$$L_O = \frac{V_{CSM}}{4 f_c \cdot k_{i-arm-RICs} \cdot I_{UN}} \tag{5.34}$$

Where $k_{i\text{-}arm\text{-}RICs}$ as the ratio of arm current ripple when using RICs technique. Substituting from (4.29) and (4.31) into (5.34), the arm inductance as a function of the gain G when using RICs technique, is given by:

$$L_O = \frac{G^2 \cdot m \cdot V_{DC}^2}{4 f_c \cdot k_{i-arm-RICs} \cdot m_{ric} \cdot \cos\varphi \cdot N_{SM} \cdot S} \tag{5.35}$$

C. Comparing size of arm inductors

From (5.32) and (5.35), for 8 SMs per arm and unity m, the arm inductance for both SS and RICs techniques are normalized, and shown in Fig. 5.10. It is noted that the arm inductance when using the SS technique is higher than the RICs technique at the same ripple factor, especially when operating at increased voltage gain.

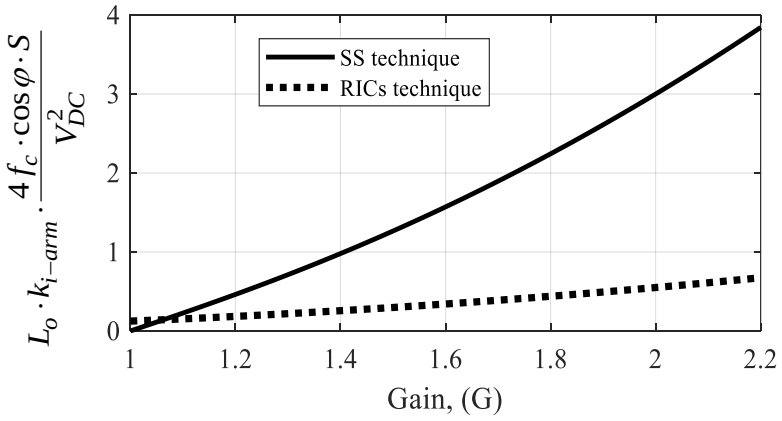


Fig. 5.10: Variation of normalized arm inductance versus gain G at N_{SM} = 8

Referring to the simulation results for the upper and lower arm inductor currents given in Fig. 4.42 and Fig. 4.43 at a gain value of 1.5 and 8 SMs per arm, which used identical value for the arm inductance of 5 mH for both modulation methods, the current ripple factor when using the SS technique is $k_{i\text{-}arm\text{-}SS}$ = 45A/121A = 0.37, while the ripple factor when using the RICs technique is $k_{i\text{-}arm\text{-}RICs}$= 9A/115A = 0.078 leading to a relative ratio of current ripple of $k_{i\text{-}qZS\text{-}SS}/k_{i\text{-}arm\text{-}RICs}$ = 0.37/0.078 = 4.7 between the SS and RICs techniques arm current ripples.

According to the curve given in Fig. 5.10 and the theoretical analysis, consider the same arm inductance for both modulation techniques and G = 1.5, the ratio

of the current ripple factor of SS technique to the current ripple factor of RICs technique is equal to 1.35/0.3 = 4.5, which is identical to the calculated ratio obtained from the simulation study.

According to the simulation data used in section 4.7, N_{SM} = 8, G = 2 (the arm inductance increases when increasing the gain), V_{DC} = 5.5 kV, S = 1.5 MVA, K_i = 30%, cos φ = 0.95 and m = 1, therefore, L_O needs to satisfy (5.36) and (5.37) for SS and RICs techniques respectively.

$$L_O > 13.8\,mH \tag{5.36}$$

$$L_O > 2.3\,mH \tag{5.37}$$

It is worth to mention that the arm inductors can be non-coupled [78] or coupled inductors [4]. In term of current flow direction, the arm current contains two components which are common-mode (circulation current) and differential-mode (output current) [79]. Using non-coupled arm inductors creates equal common mode inductance (CMI) and differential-mode inductance (DMI). The CMI is useful to limit the low order even harmonics and the switching ripple components in the circulating current. While the DMI is effective at suppressing the switching ripples in the output current which can improve THD due to load filtering action [111]. To reduce the size of the magnetic components, [3, 4] proposed to apply a single core very well coupled inductors (with a connection shown in Fig. 5.11) with CMI inductance employed only to limit the circulating current. However, the DMI became very small because the magnetic fluxes produced by the output current component in the upper and lower arm cancel each other, and consequently the switching ripples in the load current was not suppressed leading to a high THD in the output voltage and current. In order to combine the magnetic components used for circulating current limitation and also for suppressing the switching ripples in the output current (filter action), the integrated core EE design has been proposed in [79], where the DMI is sufficiently large.

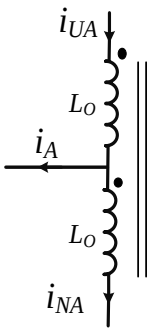


Fig. 5.11: Coupled arm inductor

One limiting aspect when using coupled inductances is that any fault or mismatch in the control of sharing equally the load current through the two arms, can lead to saturation of the coupled inductance core which will cause significant reduction in CMI and also a significant increase of circulating current. This is the reason why in the thesis, non-coupled arm inductors have been considered.

5.1.2.2 qZS-network inductor sizing

The qZS components for the upper and the lower section are assumed to be identical where $C_{U1} = C_{N1} = C_1$, $C_{U2} = C_{N2} = C_2$, and consequently the capacitor voltages and inductor currents have their average value where $v_{CU1} = v_{CN1} = V_{C1}$ and $v_{CU2} = v_{CN2} = V_{C2}$.

A. Sizing qZS inductors when using the SS technique

Fig. 5.12a shows the voltages and currents waveforms of the qZS-MMC inductors L_{U1}, L_{N1}, L_{U2}, and L_{N2} when using the SS technique. From Fig. 4.5 and (4.1)-(4.3), the qZS-inductor voltages v_{LU1}, v_{LN1}, v_{LU2} and v_{LN2} during ST mode are given by:

$$v_{LU1} = v_{LN1} = V_{C1} \tag{5.38}$$

$$v_{LU2} = v_{LN2} = (V_{DC} + 2V_{C2}) / 2 = V_{C1} \tag{5.39}$$

The inductance can be obtained by:

$$L = \frac{v_L \cdot \Delta t}{\Delta i_L} \tag{5.40}$$

where

$$\Delta t = D_{sh} / f_c \tag{5.41}$$

where $k_{i\text{-}qZS\text{-}SS}$ is the qZS-inductor current ripple factor when using SS technique.

Using (4.5), (4.14), (5.38), (5.39) and (5.41) into (5.40), the qZS-inductances have been calculated as a function of gain and carrier frequency f_c.

$$L_{U1} = L_{N1} = L_{U2} = L_{N2} = \frac{G \cdot (G-1) \cdot V_{DC}^2}{2 \cdot f_c \cdot k_{i-qZS-SS} \cdot (2G-1) \cdot P_{DC}} \tag{5.42}$$

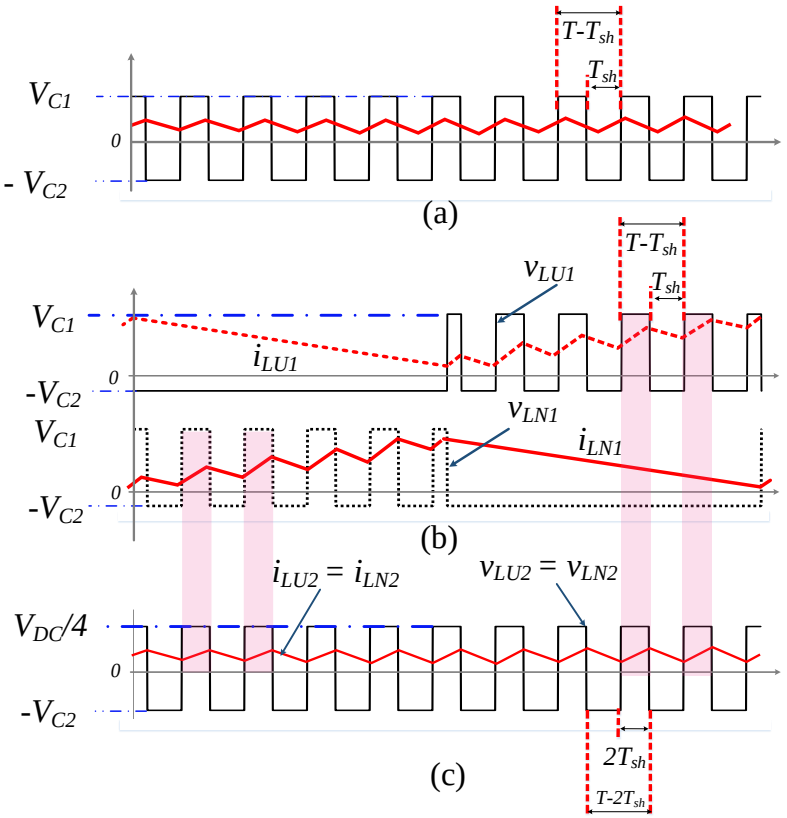


Fig. 5.12: Relevant waveforms used in determining the inductor size: a) inductor voltage and current when using SS technique, b) inductor L_{U1}, L_{N1} and c) inductor L_{U2}, L_{N2} voltage and current when using RICs technique

B. Sizing qZS inductors when using the RICs technique

This technique depends on using the partial shoot-though concept, where the upper chain-link switches can perform a shooting through of half the DC-link voltage during one half of the fundamental frequency cycle while the lower chain-link switches can perform the partial ST in the other half of the cycle.

The voltage and current waveforms of the qZS-MMC inductors L_{U1}, L_{N1}, L_{U2}, and L_{N2} when using the RICs technique are shown in Fig. 5.12b and Fig. 5.12c.

During the first half of fundamental frequency cycle, the upper (lower) qZS-network is working in the NST mode, where inductor voltage v_{LU1} (v_{LN1}) equals $-V_{C2}$. So, Δt is redefined as (5.43), where f_o is the output fundamental frequency.

$$\Delta t = 1/(2f_o) \tag{5.43}$$

Because the ST mode is used partially only for the upper (lower) chain-link switches through half the interval of the output voltage duty cycle (when N_U or N_N are lower than N_{SM} /2 as shown in Fig. 4.11), it makes the qZS-inductor currents hold AC component at the fundamental frequency f_o**.** Using (4.5), (4.29), and (5.43), the qZS inductances (L_{U1}, and L_{N1}) are calculated by:

$$\begin{aligned} L_{U1} = L_{N1} &= \frac{D_{sh} \cdot V_{DC}^2}{4 \cdot k_{i-qZS-RICs} \cdot (1-2D_{sh}) \cdot f_o \cdot P_{DC}} \\ &= \frac{(G-1) \cdot V_{DC}^2}{8 \cdot f_o \cdot k_{i-qZS-RICs} \cdot P_{DC}} \end{aligned} \tag{5.44}$$

where $k_{i\text{-}qZS\text{-}RICs}$ is the qZS-inductor current ripple factor when using RICs technique. As shown in Fig. 5.12c, the source inductors are charging in both the upper and lower qZS-networks ST modes with a duty ratio equals to $2D_{sh}$ and discharging in NST mode, producing inductor current ripple only at the carrier frequency (no low order frequency components). Therefore, the time interval in (5.40) is given by:

$$\Delta t = 2D_{sh} / f_c \tag{5.45}$$

The source inductor voltages during upper or lower ST modes are defined by (5.46).

$$v_{LU2} = v_{LU2} = (V_{DC} + V_{C2} - V_{C1})/2 = V_{DC}/4 \tag{5.46}$$

Using (4.5), (4.29), (5.45), and (5.46), the qZS inductances (L_{U2}, and L_{N2}) are calculated by (5.47).

$$L_{U2} = L_{N2} = \frac{D_{sh} \cdot V_{DC}^2}{2 \cdot k_{i-qZS-RICs} \cdot f_c \cdot P_{DC}} = \frac{(G-1) \cdot V_{DC}^2}{4 \cdot k_{i-qZS-RICs} \cdot f_c \cdot G \cdot P_{DC}} \tag{5.47}$$

C. Comparing size of qZS inductors

Comparing the formula in (5.42), when using the SS technique, to the result in (5.47), for the RICs technique, and for the same current ripple factor in the source inductor, the required source inductance ($L_{U2} = L_{N2}$) when using SS technique is higher than that with the RICs technique where the inductance ratio reaches to 2.25 times at gain value G equals 1.5.

The inductance L_{U1} and L_{N1} depends on the switching (carrier) frequency f_s (5.42) only for the SS technique and on the output frequency f_o (5.44) for the RICs technique. Dividing (5.42) by (5.44), the ratio between the inductances required for SS technique to RICs technique is given by:

$$\frac{L_{U1}(SS) \cdot k_{i-qZS-SS}}{L_{U1}(RICs) \cdot k_{i-qZS-RICs}} = \frac{4 f_o G}{f_c \cdot (2G-1)} \tag{5.48}$$

$$\frac{L_{U2}(SS) \cdot k_{i-qZS-SS}}{L_{U2}(RICs) \cdot k_{i-qZS-RICs}} = \frac{2G^2}{(2G-1)} \tag{5.49}$$

Due to a much larger inductance needed to limit the output frequency ripple, it can be noted that the current ripple when using the SS technique (switching ripple) in much lower compared to RICs technique (output frequency ripple) with a ratio of $k_{i\text{-}qZS\text{-}SS}/k_{i\text{-}qZS\text{-}RICs}$=1/27 at f_c = 4 kHz, f_o = 50 Hz and G = 1.5 at the same qZS inductance for both modulation methods.

Referring to the simulation results for the qZS-network inductor currents given in Fig. 4.38 and Fig. 4.39 at the same qZS inductance of 10 mH for both modulation techniques and at a gain value of 1.5 and f_c = 4kHz, the inductors L_{U1} and L_{N1} current ripple factor is $k_{i\text{-}qZS\text{-}SS}$ =37 A / 180 A = 0.2 (switching ripple) when using the SS technique, while the ripple factor when using the RICs technique is $k_{i\text{-}qZS\text{-}RICs}$ = 1000 A / 180 A = 5.5 (output frequency ripple) leading

to a ratio of $k_{i\text{-}qZS\text{-}SS}/k_{i\text{-}qZS\text{-}RICs}$= 0.2/5.5 = 1/27 between SS and RICs techniques which is identical to the ratio estimated by the previously derived equation (5.48).

Also, the source inductors L_{U2} and L_{N2} current ripple factor when using the SS technique is $k_{i\text{-}qZS\text{-}SS}$ = 37 A / 180 A = 0.2, while the ripple factor when using RICs technique is $k_{i\text{-}qZS\text{-}RICs}$ =17 A / 180 A = 0.09, leading to a ratio of $k_{i\text{-}qZS\text{-}SS}/k_{i\text{-}qZS\text{-}RICs}$= 0.2/0.09 = 2.22 between SS and RICs techniques which is also identical to the ratio estimated by the previously derived equation (5.49).

According to the simulation data used in section 4.7, N_{SM} = 8, G = 2, V_{DC}=5.5 kV, S = 1.5 MVA, $k_{i\text{-}qZS\text{-}SS}$ = 20%, f_c = 4 kHz, cos φ = 0.95 and m = 1, therefore, L_{U1}, L_{N1}, L_{U2} , and L_{N2} needs to satisfy (5.50) for the SS technique.

$$L_{U1} = L_{U2} = L_{N1} = L_{N2} > 8.75\ \text{mH} \tag{5.50}$$

For RICs technique, considering L_{U1}, and L_{N1} have a ripple factor $K_{i\text{-}qZS\text{-}RICs}$ of 500%, while L_{U2}, and L_{N2} have a ripple factor $k_{i\text{-}qZS\text{-}RICs}$ of 20%, therefore, L_{U1}, L_{N1}, L_{U2} , and L_{N2} needs to satisfy (5.51) and (5.52) for the RICs technique.

$$L_{U1} = L_{N1} > 10.5\ \text{mH} \tag{5.51}$$

$$L_{U2} = L_{N2} > 3.3\ \text{mH} \tag{5.52}$$

Therefore, the value of all qZS inductances L_{U1}, L_{N1}, L_{U2}, and L_{N2} of 10 mH has been selected and was used in all the simulations from Section 4.7.

5.2 Losses estimation

Power losses of the converter can be divided into losses in the passive components (due to resistance of inductors and capacitors of the qZS-MMC) and losses due to semiconductor devices (IGBTs and diodes). It is fair to assume that the semiconductor device losses are dominant compared to the passive

component losses. The semiconductor device losses are an important factor that determines the converter efficiency and are analyzed in detail in this section.

The semiconductor device power losses consist of conduction and switching losses, and both are due to non-ideal performance of the devices. The conduction losses are because of the interaction of the conducting current through the device and the forward voltage of the device when the device conducts and is turned fully on. The switching losses are determined by the dissipated energy during the turn on and turn off switching which results of overlap of the device current and blocking voltage of the controllable devices (IGBTs) and the reverse recovery mechanism of the fast recovery diodes.

In [112], the semiconductor losses have been estimated depending on the average value of the semiconductor device currents, which reduced the precision of the losses estimation. Another approach given in [113] uses the simulated current waveforms and loss specifications from the semiconductor device datasheets to calculate the semiconductor losses for specific operating conditions. In [114], the instantaneous current value of the semiconductor devices has been theoretically estimated and used to calculate the losses and this approach is adopted also in this thesis. Therefore, the analytical comparison of the loss estimation is presented in the following section and this model is validated by the simulation model.

Due to symmetrical circuit parts, the conduction and switching power losses have been derived only for the upper qZS-network and the upper arm of the MMC leg. The lower part of the qZS-MMC is assumed to provide the same losses as the upper part.

5.2.1 Conduction losses analysis

The conduction power losses are the losses that occur when the power semiconductor devices are turned on and conducting a given current. The conduction power losses in a single device are defined by:

$$P_C(t) = v_t(i_c(t)) \,.\, i_c(t) \tag{5.53}$$

where $v_t\,(i_c(t))$ is the total on-state voltage drop on the semiconductor device during the conduction of the device current $i_c(t)$, which can be approximated by:

$$v_t(t) = V_{f_0} + R_f \,.\, i_c(t) \tag{5.54}$$

where V_{f0} is the device opening forward voltage drop at zero current and R_f is the device equivalent resistance. These parameters can be easily obtained from the device characteristic curve from the datasheets by approximating a linear voltage drop with a given device opening voltage.

5.2.1.1 SMs conduction losses

In our study, it important to review the operation states of the SMs according to the arm current direction and SM output voltage. With reference to Fig. 5.13, the switching states of the HBSM are summarized in the Table 5.1 according to the arm current direction and the SM output voltage.

Table 5.1: Switching states of HBSM

SM status	V_{XY}	states		Current direction	Conducting device
		T_1	T_2		
Inserted	V_{CSM}	1	*0*	+ $X \rightarrow Y$	Diode D_1
				- $Y \rightarrow X$	IGBT T_1
Bypassed	0	0	1	+ $X \rightarrow Y$	IGBT T_2
				- $Y \rightarrow X$	Diode D_2

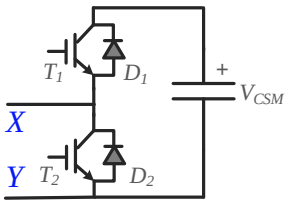


Fig. 5.13: HBSM configuration

When N_U of the upper arm SMs are inserted in the arm, the diode D_1 conducts if the arm current is positive, and the current flows through T_1 if the arm current is negative. The remaining $N_{SM} - N_U$ SMs in the arm are bypassed where the diode D_2 conducts if the arm current is negative and the current flows through T_2 if the arm current is positive. Therefore, the instantaneous conduction losses can be expressed as:

$$P_{C-arm}(t) = \begin{cases} N_U \cdot P_{C-diode}\left(i_{UA}(t)\right) + \left[N_{SM} - N_U\right] \cdot P_{C-IGBT}\left(i_{UA}(t)\right) \\ \qquad @ \quad i_{UA}(t) \geq 0 \\ \left[N_{SM} - N_U\right] \cdot P_{C-diode}\left(i_{UA}(t)\right) + N_U \cdot P_{C-IGBT}\left(i_{UA}(t)\right) \\ \qquad @ \quad i_{UA}(t) < 0 \end{cases} \tag{5.55}$$

where N_U is the number of inserted SMs in the upper arm and can be defined by $N_U = v_{UA}(t)/V_{SM}$. The current i_{UA} is defined respectively in (4.19) and (4.34) for the SS and RICs techniques. $P_{C\text{-}diode}$ and $P_{C\text{-}IGBT}$ are the instantaneous diode and IGBT conduction power losses which can be estimated using (5.53), (5.54) with the relevant parameters extracted from manufacturer datasheet. From the voltage drop and conducting current characteristics for both the diode and the IGBT, the formulae for $P_{C\text{-}diode}$ and $P_{C\text{-}IGBT}$ can be obtained as given in Appendix B.

5.2.1.2 qZS-network conduction losses

In this thesis, chain-link and series switches consist of IGBTs connected in antiparallel to the diodes as illustrated in the schematic shown in Fig. 4.13 for reasons explained in section 4.4. The instantaneous conduction losses of the chain-link and series switches can be expressed as:

$$P_{C-qZS}(t) = \begin{cases} N_{ch} \cdot P_{c-IGBT}\left(i(t)\right); & i(t) \geq 0 \\ N_{ch} \cdot P_{c-diode}\left(i(t)\right); & i(t) < 0 \end{cases} \tag{5.56}$$

where $i(t)$ represents the instantaneous current i_{SU} and i_{SU1} for the chain-link and series switches which are defined by (5.57) and (5.58) respectively. N_{ch} is the number of series devices in the chain-link switch, which depends on the modulation technique, which will be determined in the next chapter.

$$i_{SU}(t) = \left(2I_L - i_{UA}\right) g_{SU}(t) \tag{5.57}$$

$$i_{SU1}(t) = -\left(2I_L - i_{UA}\right) g_{SU1}(t) \tag{5.58}$$

where $g_{SU}(t)$ and $g_{SU1}(t)$ are the pulse signals of switches S_U and S_{U1} respectively, with the pulse amplitude is equal to '1' which represent their conduction state. These signals are illustrated in Fig. 4.8 for the SS technique and Fig. 4.11 for the RICs technique. According to the instantaneous value of the arm current i_{UA} and the inductor current I_L, the qZS-network conduction losses can be estimated for both SS and RICs techniques.

The average value of the upper arm SMs and upper qZS-network conduction power losses over a fundamental frequency period has been executed by integrating (5.55) and (5.56) respectively using a MATLAB script.

5.2.2 Switching losses analysis

The switching losses are related to the voltage and current of each device, which are estimated during the on and off transition states of the semiconductor devices. The switching energies include e_{on} and e_{off} for turn on and turn off energies of the IGBT and e_{rec} for reverse recovery energy of the diode [113].

5.2.2.1 SMs switching losses

By considering a simplified assumption that the SM capacitor voltage is constant at its average value V_{CSM}, the voltage across each switch is V_{CSM}. The current of the IGBTs and diodes in SMs is equal to the arm current. In each SM, which is a half-bridge SMs configuration, there are always two transitions generating switching loss which are: (1) the conducting IGBT turns off and the diode taking over conduction of the arm current turns on, with e_{off} dissipated energy, (2) the conducting diode turns off and the IGBT taking over conduction of the arm current turns on, with e_{rec} and e_{on} dissipated energies.

The switching characteristic curves and formulae for turn on loss of one IGBT e_{on}, turn off loss of one IGBT e_{off} and recovery loss of one diode e_{rec} are given and illustrated in Appendix B.

A. SM switching losses for the SS technique

Depending on the level-shift carrier based algorithm, only one SM is bypassed/inserted from each arm during a carrier frequency cycle f_c. As previously illustrated in the converter operation principles, a sorting algorithm

is required to provide SMs capacitor voltage balancing, where some or all of the SMs are switched during this sorting process. In order to reduce unnecessary switching, the sorting process is executed every N_{SM} carrier frequency cycle, $f_{sort} = f_c / N_{SM}$. Therefore, there are two groups of transitions, one at the carrier frequency f_c and the other at the sorting frequency f_{sort}.

According to Table 5.1 and Fig. 5.13, if the SM is inserted and the arm current i_{UA} is positive (or the SM is bypassed and the arm current is negative), the IGBT turns off and diode turns on leading to energy loss of e_{off}. Also, if the SM is bypassed and the arm current is positive (or if the SM is inserted and the arm current is negative), the conducting IGBT turns on and diode turns off leading to e_{on} and e_{rec}. The generated switching loss energies at each transition are listed in Table 5.2.

Therefore, during carrier frequency f_c cycle, one of the SMs is inserted (bypassed) and then one of SMs is bypassed (inserted). Therefore, the total arm switching dissipated power losses during a carrier frequency cycle is defined by:

$$P_{SW-f_c}(t) = f_c \cdot \left(e_{off}\left(i_{UA}(t)\right) + e_{on}\left(i_{UA}(t)\right) + e_{rec}\left(i_{UA}(t)\right) \right) \times \frac{V_{CSM}}{V_n} \qquad (5.59)$$

where V_n is the SMs semiconductor device test voltage (which equals to 1650 V in the datasheet of the MITSUBISHI CM800HA-66A IGBT power module for the test system ratings used in the simulation studies). The switching characteristic curves and formulas for e_{on}, e_{off}, and e_{rec} are given in Appendix B.

Table 5.2: Generated switching energies at each transition

Transition condition		Semiconductor devices				Switching energies
SM state	Arm current	T_1	D_1	T_2	D_2	
Inserted	+ *ve*	0	$0 \rightarrow 1$	$1 \rightarrow 0$	0	e_{off}
Bypassed	+ *ve*	0	$1 \rightarrow 0$	$0 \rightarrow 1$	0	e_{on}+ e_{rec}
Inserted	− *ve*	$0 \rightarrow 1$	0	0	$1 \rightarrow 0$	e_{on}+ e_{rec}
Bypassed	− *ve*	$1 \rightarrow 0$	0	0	$0 \rightarrow 1$	e_{off}

In addition, the switching dissipated energy due to the sorting mechanism needs to be considered. Assuming the sorting process is performed every N_{SM} carrier frequency cycle, the sorting frequency f_{sort} equals f_c /N_{SM}. The number of SMs that are included in the sorting depends on the number of inserted SMs in the corresponding arm.

Firstly, if the number of inserted SMs N_U is less than N_{SM}/2, it is assumed that all the inserted SMs N_U are bypassed during the sorting process, and then N_U of SMs will be selected using the balancing algorithm, to be inserted. If the arm current is positive, the N_U inserted SMs will be bypassed and their switching losses become N_U of e_{on} + e_{rec} (while e_{off} for negative arm current). Then, instant, the N_U SMs will be selected to be inserted and their switching energies become N_U of e_{off} (while e_{on} + e_{rec} for negative arm current). Therefore, the resultant switching energy loss during this sorting instant is equal to N_U of e_{on} + e_{rec}+ e_{rec} regardless of the arm current direction.

If the number of inserted SMs N_U is higher than or equal to N_{SM}/2, it is assumed that only $N_{SM} - N_U$ of inserted SMs will be selected using the balancing algorithm to be bypassed, and then $N_{SM} - N_U$ of all bypassed SMs (which are $2N_{SM} - 2N_U$) will be selected to be inserted. If the arm current is positive, $N_{SM} - N_U$ of inserted SMs will be bypassed and their switching energies are e_{on}+ e_{rec} (while e_{off} for negative arm current). Then, the $N_{SM} - N_U$ of bypassed SMs will be inserted and their switching loss will be e_{off} in case of positive arm current (while e_{on} + e_{rec} for negative arm current). Therefore, the resultant switching energy loss is equal to $N_{SM} - N_U$ of (e_{on} + e_{rec}+ e_{rec}) regardless of the arm current direction.

Finally, the arm dissipated switching power losses due to sorting algorithm is defined by (5.60). The total arm switching power losses when using the SS technique is defined by (5.61).

B. SM switching losses for the RICs technique

According to the polarity of the fundamental output voltage, the number of SMs that change states can be estimated.

$$P_{SW-sort}(t) = \tag{5.60}$$

$$\begin{cases} = \left[f_{sort} \cdot N_U(t) \right] \\ \qquad \times \left[e_{off}\left(i_{UA}(t)\right) + e_{on}\left(i_{UA}(t)\right) + e_{rec}\left(i_{UA}(t)\right) \right] \times \dfrac{V_{CSM}}{V_n} \\ \qquad\qquad if \qquad N_U(t) < N_{SM}/2 \\ = \left[f_c + f_{sort} \cdot \left(N_{SM} - N_U(t)\right) \right] \\ \qquad \times \left[e_{off}\left(i_{UA}(t)\right) + e_{on}\left(i_{UA}(t)\right) + e_{rec}\left(i_{UA}(t)\right) \right] \times \dfrac{V_{CSM}}{V_n} \\ \qquad\qquad if \qquad N_U(t) \geq N_{SM}/2 \end{cases}$$

$$P_{SW-arm-SS}(t) = P_{SW-fc}(t) + P_{SW-sort}(t) \tag{5.61}$$

During the positive half cycle of the fundamental period when the upper qZS-network works in NST mode, one of the SMs is inserted (bypassed) and then one of SMs is bypassed (inserted). This case is similar to the SS technique where, the arm switching dissipated power losses during the carrier frequency cycle f_c is defined by (5.59). However, during the negative half cycle of the fundamental period, the upper qZS-network works in both ST and NST modes during one carrier frequency cycle leading to $N_{SM}/2$ of the inserted SMs are switched during ST mode while only one of the SMs is switched during NST mode. As a result, $N_{SM}/2+1$ of the SMs are switched when considering that the ST carrier frequency is the same as the SMs carrier frequency.

The dissipated switching energy due to the sorting mechanism is similar to the SS technique. Therefore, according to the polarity of the fundamental output voltage and number of inserted SMs, the total switching power losses when using the RICs technique can be calculated by (5.62).

$$P_{SW-arm-RICs}(t) \tag{5.62}$$

$$\begin{cases} = \left[f_c + f_{sort} \cdot N_U(t) \right] \times e_t \times \dfrac{V_{CSM}}{V_n} \\ \qquad\qquad if \quad V_m \geq 0 \quad \& \quad N_U(t) < N_{SM}/2 \\ = \left[f_c + f_{sort} \cdot \left(N_{SM} - N_U(t) \right) \right] \times e_t \times \dfrac{V_{CSM}}{V_n} \\ \qquad\qquad if \quad V_m \geq 0 \quad \& \quad N_U(t) \geq N_{SM}/2 \\ = \left[f_c \cdot \left(1 + N_{SM}/2 \right) + f_{sort} \cdot N_U(t) \right] \times e_t \times \dfrac{V_{CSM}}{V_n} \\ \qquad\qquad if \quad V_m < 0 \quad \& \quad N_U(t) < N_{SM}/2 \\ = \left[f_c \cdot \left(1 + N_{SM}/2 \right) + f_{sort} \cdot \left(N_{SM} - N_U(t) \right) \right] \times e_t \times \dfrac{V_{CSM}}{V_n} \\ \qquad\qquad if \quad V_m < 0 \quad \& \quad N_U(t) \geq N_{SM}/2 \end{cases}$$

Where $e_t = e_{off}\left(i_{UA}(t)\right) + e_{on}\left(i_{UA}(t)\right) + e_{rec}\left(i_{UA}(t)\right)$

5.2.2.2 qZS-network switching losses

According to current direction given in Fig. 4.13, the chain-link switches can conduct current during ST mode while series switches can conduct current during NST mode, where these currents are defined by (5.63) and (5.64) respectively. Otherwise, these switches are off and holding zero current value.

$$i_{SU}(t) = 2I_L - i_{UA} \tag{5.63}$$

$$i_{SU1}(t) = -\left[2I_L - i_{UA} \right] \tag{5.64}$$

If the current of the chain-link (or series) switches has positive value, the IGBT holds this current where this IGBT turns on and off during one carrier frequency cycle leading to e_{on} and e_{off}. While if this current has negative polarity, the diode conducts the current; when this diode turns off during one carrier frequency cycle, it produces reverse recovery loss e_{rec}. The instantaneous switching power losses for each switch in the chain-link switches at $i(t) = i_{SU}(t)$ (or series switches at $i(t) = i_{SU1}(t)$) is defined by (5.65).

$$P_{SW-qZS}(t)=\begin{cases} f_c\left[e_{off}\left(i(t)\right)+e_{on}\left(i(t)\right)\right]\times\dfrac{V_{UN}}{2\cdot V_n\cdot N_{ch}} & i(t)>0 \\ f_c\times e_{rec}\left(i(t)\right)\dfrac{V_{UN}}{2\cdot V_n\cdot N_{ch}} & i(t)<0 \end{cases} \quad (5.65)$$

where V_{UN} is the peak value of the DC-link voltage which are defined by (4.35) and (4.36) and $i(t)$ denotes the current i_{SU} for the chain-link switches or i_{SUI} for series switches and defined by (5.63) and (5.64) respectively.

For RICs technique, as the ST pulses for upper qZS-network are not introduced over the positive half of output voltage fundamental cycle, there is no switching losses in the positive half cycle which should be considered in calculation.

The presented analytical expressions have been used to evaluate the conduction and switching power losses for both the MMC arm and the qZS-network where the integration has been executed over one fundamental frequency period to estimate average over a cycle loss.

5.2.3 Analysis of the power losses

For comparison purpose between the two proposed modulation schemes, the output voltage is set to 5.5 kV with output power of 1.4 MW, where only a single-phase converter has been investigated via detailed simulations. The peak value of output phase voltage was fixed to 5.5 kV and the source voltage is considered to be variable in a wide range, varying from 22 kV to 5.5 kV and causing to a change in the voltage gain value from 0.5 to 2. The modulation index *m* is set to 1 in the boost mode, while it is set to *G* value in the buck mode. Considering a topology consisting of eight SMs per arm, each SMs needs to have an average capacitor voltage equal 1.35 kV in boost mode. Therefore, MITSUBISHI CM800HA-66A IGBT, rated at 3.3kV and 800A can be used for the SMs [115].

To determine the qZS-network switches rating, it is considered that the maximum operating gain is ‘2’. According to (4.14) and (4.29), the duty ratio needs to be set to 0.33 and 0.25 for the SS and RICs techniques respectively. As a result, the maximum DC-link voltage is 16.2 kV and 11 kV at a gain value

equals 2 when using the SS and RICs techniques respectively. Considering the same switches rating for both SMs and qZS-networks devices, 4 switches per chain-link (which equals $N_{SM}/2$) are required when using the RICs technique while 6 switches per chain-link (which equals $2N_{SM}/3$) are required for the SS technique. The conduction and switching characteristics as specified in the manufacturer's datasheet of the MITSUBISHI CM800HA-66A IGBT are provided in Appendix B.

The previously explained losses estimation procedure provides information about the expected losses in the qZS-MMC when using either of the two modulation techniques. Fig. 5.14 shows the conduction losses in qZS-networks for each of the proposed modulation techniques, SS and RICs, versus the active output power at different gain values. The output voltage is fixed at 5.4 kV while the input voltage is varying to 22, 14.6, 11, 8.8, 7.3 and 5.5 kV at gain values equal to 0.5, 0.75, 1, 1.25 1.5, and 2 respectively. As expected, the SS technique adds more conduction losses in qZS-networks which is a result of having a higher number of qZS chain-link switches compared to the RICs technique. The conduction losses of the series switches S_{U1} are higher than that of the chain-link switches S_U due to a higher duty ratio of S_{U1}. With decreasing the DC source voltage from 22 kV to 5.5 kV, the source and inductor currents increase and consequently, there is more dissipated conduction losses.

Fig. 5.15 shows the SMs conduction losses for all gain values in the considered range. The two techniques give approximately equal SMs conduction losses. For a certain output power, the arm current is the same at any gain value, with a slight change in the DC component I_{UN} between the two techniques, leading to approximately equal SMs conduction losses at any gain value.

Regarding the switching losses, the frequency of the triangular carrier signal f_c is chosen to be 4 kHz. As a result of switching only one SM per arm during the carrier frequency cycle f_c, the actual average number of commutations per second per SMs (i.e. equivalent switching frequency f_s) is $f_s = f_c/N_{SM} = 0.5$ kHz. The sorting frequency f_{sort} is set to be at the average switching frequency $f_{sort} = f_s = 0.5$ kHz.

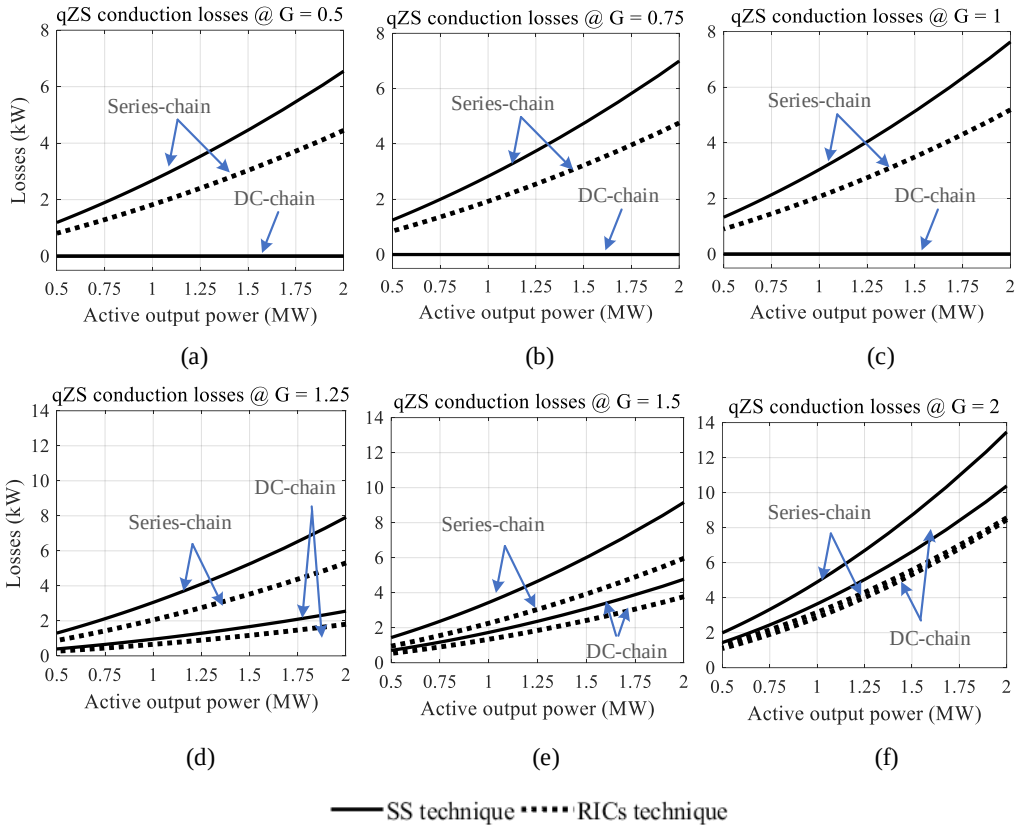


Fig. 5.14: qZS-networks conduction losses at a) G = 0.5, b) G = 0.75, c) G = 1 d) G = 1.25, e) 1.5 and f) G = 2.

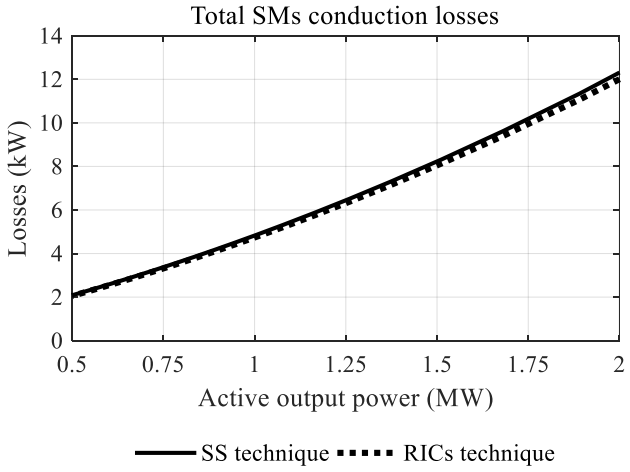


Fig. 5.15: SMs conduction losses at any gain value

In boost mode (at gain values 1.25, 1.5 and 2), the RICs technique adds more SMs switching losses compared to the SS technique. This is a result of having to turn on/off N_{SM} /2 of SMs during ST intervals that leads to an average switching frequency $3f_c/ N_{SM}$ which is three times higher than in the case of using the SS technique (f_c/ N_{SM}). However, the voltage stress on the series and chain-link switches is higher in the case of using the SS technique compared to RICs technique and by applying only partial ST intervals of RICs, the qZS-networks switching losses are higher when using the SS technique especially when increasing the gain. Fig. 5.16 shows the switching losses for the switches in the chain-link switches, the series switches and SMs switches for each of the proposed modulation techniques versus the active output power at different gain values. In the buck mode, the two techniques become identical and the SMs losses are equal. By decreasing the converter gain from 1 to 0.5, the SMs switching losses increases due to increase in the SMs capacitor voltage.

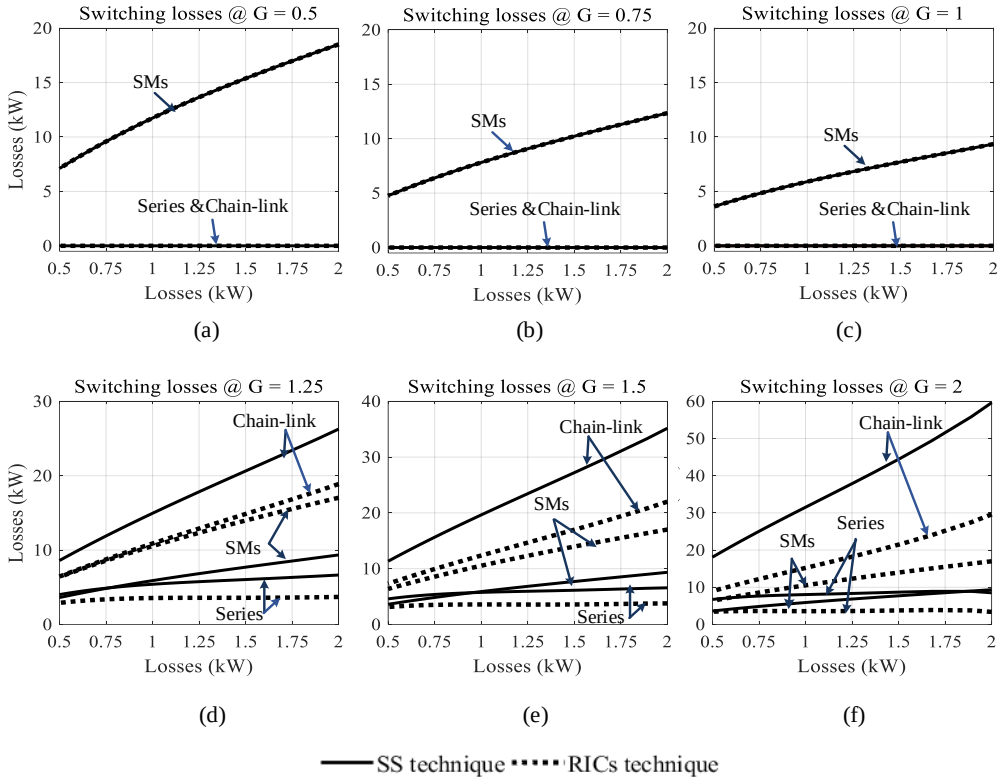


Fig. 5.16: Switching losses for chain-link, series and SMs switches when using SS and RICs techniques at a) G = 0.5, b) G = 0.75, c) G = 1 d) G = 1.25, e) G = 1.5 and f) G = 2.

Fig. 5.17 shows the percentage of total losses to the active output power versus the active output power when using the RICs and SS techniques. In buck mode, the total losses decrease when increasing the gain from 0.5 to 1, while the losses increase when increasing the gain from 1 to 2. In addition, using the RICs technique achieves lower total converter losses and then a higher overall efficiency.

The conduction and switching losses estimation procedure for each technique have been validated using simulation models for each technique at output power of 1.4MW and different values of gains 0.75, 1, 1.5, and 2 as listed in Table 5.3. The qZS-MMC model with the SS and RICs techniques have been built using PLECS. Each device can have its turn-on, turn-off and recovery switching energy matched with the one in the chosen datasheet where look-up tables can be extracted and inserted to PLECS thermal library. Comparing the simulation results given in Table 5.3 with those expected by the analytical models shows a high degree of matching.

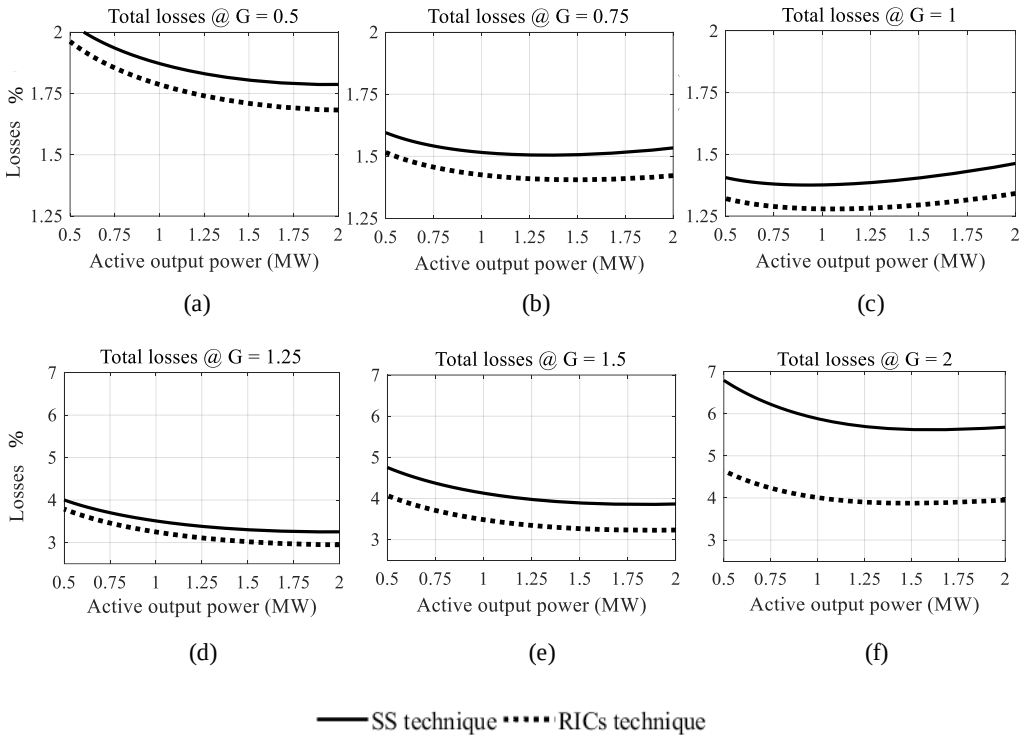


Fig. 5.17: Total losses when using SS and RICs techniques at a) G = 0.75, b) G = 1, c) G = 1.25 d) G = 1.5, and e) G = 2.

Table 5.3: The simulation result of conduction, switching and total losses

		SMs losses (kW)			qZS-losses (kW)			Total losses (kW)
		Con.	Sw.	Total	Con.	Sw.	Total	
G = 0.75	**A**	8.1	10.1	18.2	3.5	0	3.5	21.7
	B	8.1	10.1	18.2	5.3	0	5.3	23.5
G = 1	**A**	8.1	7.3	15.4	3.8	0	3.8	19.2
	B	8.1	7.3	15.4	5.6	0	5.6	21
G = 1.5	**A**	8.2	14	22.2	6.5	19.4	25.9	48.1
	B	8	7.8	15.8	9.4	32.4	41.8	56.6
G = 2	**A**	8	13.8	21.8	10.2	23.1	33.3	55.1
	B	7.8	7.5	15.3	14.1	48.7	62.8	78.1

A: RICs technique **B:** SS technique

5.3 Application of qZS-MMC to interfacing a wind turbine system with the medium voltage grid

Green energy sources are attracting a great attention worldwide in an attempt to reduce the CO_2 emissions [8]. The wind energy system (WES) is one of the fastest growing renewable energy sources in the world [116] . Among various generator types used with WES, the permanent magnet synchronous generator (PMSG) has gained a significant interest due to absence of the gear box which consequently leads to a reduced system failure, improved efficiency and higher system reliability [117].

Configuration of the WES using direct drive PMSG is shown in Fig. 5.18, where there is no gearbox. Due to the variation of the generator output frequency with the wind speed, a back-to-back (BTB) converter is required to interface the WES to the electric grid. The BTB converter comprises of a controlled PWM rectifier which generates a regulated DC voltage at the DC-link terminals and a PWM

inverter which produces an AC voltage synchronized to match with the grid. The typical BTB converter configurations are the two-level voltage source converter (2L-VSC) [118], the NPC [118], and the MMC [78]. BTB configurations of NPC and MMC are the most promising due to the salient features of the multilevel converter of low harmonic distortion and better handling of the medium and high voltage/power [10]. However, using two forced commutated converters leads to a high cost and low efficiency [4].

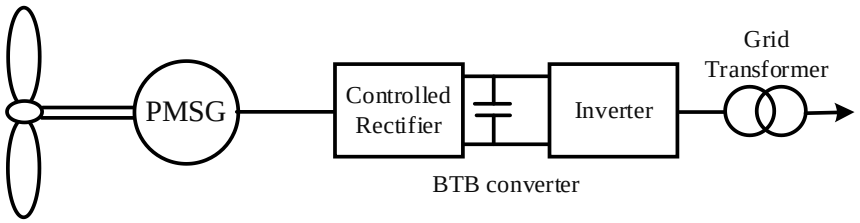


Fig. 5.18: Configuration of wind energy system with multipole PMSG using BTB converter

In [4], it has been suggested to use a full-bridge SMs based MMC (FB-MMC) to interface the WES (with a rating of 6.6 kV, 5 MW [4]) to the electric grid. This integration has been implemented using a simple three-phase uncontrolled diode rectifier in-between the AC output terminals of the PMSG and the DC input terminals of the FB-MMC. This circuit has an advantage over the BTB configuration which is replacing the controlled rectifier stage (which may be one of the 2L-VSC, NPC, or MMC) with a three-phase diode rectifier, which results in a lower cost, higher reliability and improved efficiency [4].

The proposed qZS-MMC can achieve the same function of the FB-MMC converter with a fluctuating DC voltage. Fig. 5.19 shows a feasible configuration for the WES based on qZS-MMC and using a multipole PMSG with no gear box. The AC voltage from the generator is converted to a variable DC voltage using a three-phase diode rectifier. The DC voltage is varying in proportion to rotational speed, as resulting from the momentarily available wind power. The qZS-MMC uses the varying DC voltage and can generate a constant AC output voltage by adjusting the converter parameters.

The work published in [119, 120] have describe the maximum point power tacking method for a wind turbine generation system using uncontrolled diode rectifier, which can be applied here.

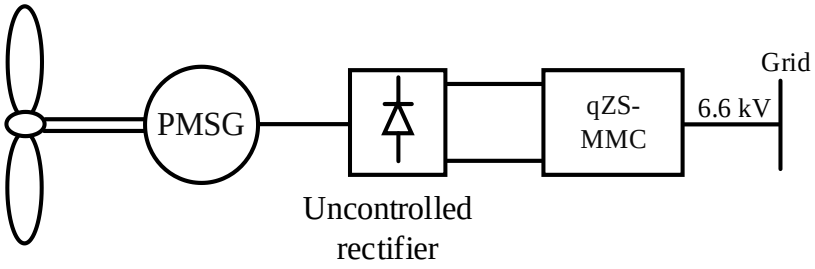


Fig. 5.19: Wind energy system based on qZS-MMC

5.4 Conclusions

In this chapter, the capacitor voltage and inductor current ripples in the qZS-networks and the MMC arms have been analysed and compared for the two modulation techniques which allows an estimation of the required capacitor and inductor sizes. Guidelines for sizing different passive components have been developed. Using the RICs technique requires lower qZS capacitor sizes compared to the SS technique and also slightly lower SMs capacitor sizes especially when increasing the gain. However, for the same current ripple factor, the required source inductance ($L_{U2} = L_{N2}$) when using RICs technique is lower than that with the SS technique. While the RICs technique requires a much higher qZS inductance (L_{U1} and L_{N1}) in order to limit the fundamental frequency current component that appeared in the qZS inductor currents. Also, the RICs technique requires a much lower arm inductance in order to limit the switching ripples.

Relevant simulation cases have been presented to validate the analysis given in this chapter. A particular attention has been given to the power losses with deriving the analytical expressions of the semiconductor losses, comprising of conduction and switching losses that have been presented for each modulation technique. The SS technique adds more conduction losses in qZS-networks which is a result of having a higher number of qZS chain-link switches compared

to the RICs technique. The two techniques give approximately equal SMs conduction losses. Since the voltage stress on the chain-link switches is higher in case of using the SS technique compared to RICs technique and by applying only partial ST intervals of RICs, the qZS-networks switching losses are higher when using the SS technique especially when increasing the gain. On the other hand, the RICs technique adds more SMs switching losses compared to the SS technique. To conclude, using the SS technique resulted in higher total converter losses and then lower efficiency compared with the RICs technique.

Wind turbine generation system is a potential application for the proposed qZS-MMC. Instead of using traditional back-to-back converters such as BTB-MMC, the qZS-MMC is a good candidate for PMSG based wind turbine generation system due to using three-phase diode-rectifier with the qZS-MMC instead of using the controlled rectifier in BTB converters which results in lower cost and improved efficiency.

Chapter 6
Topologies Comparison and Investigating the Fault Blocking Capability

This chapter includes a comparison between the proposed qZS-MMC and other two power converters, that able to provide voltage buck and boost capabilities, which are the FBSMs based MMC (FB-MMC) and the quasi Z source cascaded multilevel converter (qZS-CMI). The comparison is carried out in terms of the required number of passive and active components, conduction and switching power losses and output voltage quality.

The traditional HBSM based MMC is unable to block the fault current during fault at the DC terminals (hereafter referred to as DC-fault) due to presence of the freewheeling diodes in the upper and lower arms that allow the current to pass from AC side to feed the DC-fault. This current may reach high levels which may damage the converter devices.

The proposed qZS-MMC can block the AC grid current during the DC-fault, when the qZS capacitor voltages in the fault current path is higher than the grid voltage. Therefore, this chapter investigates the converter behavior under DC-fault conditions. A simulation model is developed and is used to demonstrate the validity of the proposed converter and its capability to handle the pole-to-pole

and pole-to-ground DC-faults. Section 7.3 will present the experimental results for the converter operation under DC-fault.

6.1 Topologies comparison

The attractive features of the proposed qZS-MMC that have been showcased in the simulation results shown before makes it suitable for use in the interface with a medium voltage/power system such as multi wind turbines and photovoltaic generation systems. Since other power conversion options are available, it would be interesting to compare the proposed converter with the MMC based on FBSMs (FB-MMC) [4] and the quasi Z-source cascaded multilevel converter (qZS-CMI) [65, 77] as all these are able to provide voltage boosting capability. The comparison has been carried out in terms of:

1. Number of active and passive components
2. Voltage and current stresses
3. Conduction and switching losses
4. Output voltage waveform quality

6.1.1 Number of active and passive components

The proposed comparison is carried out in terms of the required number of semiconductor devices, inductors, capacitors and DC voltage sources for the same number of levels and magnitude of the output AC voltage where the gain G is required to reach 2. Regarding the proposed qZS-MMC and the FB-MMC, N_{SM} SMs per arm are required working with a modulation index that is fixed to "1" for all boost gain ranges for these converters leading to $2N_{SM}$ + 1 output voltage levels. For the qZS-CMI, in order to increase the gain (i.e. increase the ST duty ratio), the modulation index should decrease with increasing the ST duty ratio, leading to a drop in the number of the output voltage levels [65]. As a result, the number of SMs for the qZS-CMI is changed to $3N_{SM}$ /2 to attain $2N_{SM}$ +1 levels in the output voltage at G = 2.

Considering the same switches voltage rating for both SMs and qZS-networks devices in the proposed qZS-MMC, N_{SM}/2 devices per chain-link are required when using the RICs technique while $2N_{SM}$/3 devices per chain-link are required

for the SS technique. The series devices in the qZS-networks that are considered are the IGBTs with antiparallel diodes in both qZS-MMC and qZS-CMI.

Table 6.1 shows the power semiconductor requirements for different topologies. Taking the number of the IGBTs in the FB-MMC as a reference, the total number of IGBTs required by the qZS-MMC with RICs and SS techniques decreases to 75 % and 87.5 %, respectively, and to 93.7 % for the qZS-CMI in case of the single-phase converter.

Regarding the passive components, the qZS-MMC uses four more inductors and two more capacitors compared to the FB-MMC, while the qZS-CMI requires more inductors and capacitors especially with increasing N_{SM}. The qZS-MMC and the FB-MMC require one DC source and the qZS-CMI requires more isolated DC sources depending on N_{SM}.

For a three-phase converter implementation, due to the fact that the qZS switches are shared with the other two phases, the number of IGBTs required by the qZS-MMC controlled by the SS technique decreases to 62.5% compared to the FB-MMC, which is considered a significant reduction in terms of number of semiconductor power devices while it is 93.7% for qZS-CMI.

Table 6.1: Comparison of active and passive component requirements

	qZS-MMC with RICs	qZS-MMC with SS	FB-MMC	qZS-CMI
No. SMs/phase	2 N_{SM}	2 N_{SM}	2 N_{SM}	3 N_{SM}/2
No. IGBTs/phase	4 N_{SM}	4 N_{SM}	8 N_{SM}	6 N_{SM}
No. qZS IGBTs	2 N_{SM}	3 N_{SM}	0	3 N_{SM} / 2
Single-phase converters				
Total IGBTs	6 N_{SM}	7 N_{SM}	8 N_{SM}	7.5 N_{SM}
Inductors	6	6	2	3 N_{SM}
Capacitors	2 N_{SM} +4	2 N_{SM} +4	2 N_{SM} + 2 split Caps	3 N_{SM}
DC voltage sources	1	1	1	3 N_{SM} / 2
Three-phase converters				
Total IGBTs	*N/A*	15N_{SM}	24 N_{SM}	22.5 N_{SM}
Inductors	*N/A*	10	6	9 N_{SM}
Capacitors	*N/A*	6N_{SM} + 4	6N_{SM} + 2	9 N_{SM}
DC voltage sources	*N/A*	1	1	9 N_{SM}/2

It should be noted that a convenient three-phase implementation is possible for the qZS-MMC with RICs, but it is considered non-optimized configuration as illustrated in section 4.5. Table 6.1 summarizes the requirements of the power semiconductor devices, inductors and capacitors and DC voltage sources.

6.1.2 Voltage and current stresses

Table 6.2 describes the ratio of voltage stress of the switching devices and the capacitor voltages relative to the peak value of the fundamental output phase AC voltage for the three topologies which is assumed to remain constant. The relations in Table 6.2 have been derived to provide the output voltage level. The voltage stress of the series and the chain-link switches of the qZS-MMC when using the RICs technique are lower than that of the qZS-MMC when using the SS technique and both are higher than that of the qZS-CMI. Therefore, for the same switches rating of SMs, $N_{SM}/2$ switches per chain-link are required when using the RICs technique while $2N_{SM}/3$ switches per chain-link are required for the SS technique operating at $G = 2$. The SM switches stress voltages are equal for the qZS-MMC and FB-MMC, and both are higher than that of the qZS-CMI.

In conclusion, although the qZS-CMI switches are subject to the lowest voltage stress, it requires a higher number of switches than the proposed qZS-MMC as explained and summarized in Table 6.1. Also, the qZS capacitor voltage of the qZS-CMI is lower than the qZS capacitor voltage of the qZS-MMC.

Regarding the current stress, Table 6.3 describes the ratio of the current stress of the switching devices and the inductors relative to the peak value of the output AC current. The current stress of the series and chain-link switches are slightly higher when using the RICs compared to the SS technique, where $m_{RIC} = 0.91$ at $G = 2$. The current stress of the series switch of the qZS-CMI is higher than that of the qZS-MMC with a ratio of 1.6 times at $G = 2$ at $m = 1$ and $\cos(\varphi) = 1$. The qZS-CMI gets a higher SMs current stress than the FB-MMC and both are higher than the qZS-MMC. The current stress of the qZS inductor of the proposed converter qZS-MMC are half of the qZS-CMI. Also, the FB-MMC gets a higher current stress on the arm inductor compared to the qZS-MMC.

It can be concluded that the proposed converter has the lowest current stresses among the three topologies.

Table 6.2: Comparison of voltage stresses relative to the peak output AC voltage

		qZS-MMC with RICs	qZS-MMC with SS	FB-MMC	qZS-CMI
Switches	Series	1	$\frac{(2G-1)}{G}$	-	$\frac{(2G-1)}{N_{SM}G}$
	DC-link	1	$\frac{(2G-1)}{G}$	-	-
	SMs	$\frac{2}{N_{SM}}$	$\frac{2}{N_{SM}}$	$\frac{2}{N_{SM}}$	$\frac{(2G-1)}{N_{SM}G}$
Caps.	qZS	C1 $\frac{G+1}{2G}$ C2 $\frac{G-1}{2G}$	C1 1 C2 $\frac{G-1}{G}$	-	C1 $\frac{1}{N_{SM}}$ C2 $\frac{(G-1)}{N_{SM}G}$
	SMs	$\frac{2}{N_{SM}}$	$\frac{2}{N_{SM}}$	$\frac{2}{N_{SM}}$	-

Table 6.3: Comparison of current stresses relative to the peak output AC current

		qZS-MMC with RICs	qZS-MMC with SS	FB-MMC	qZS-CMI
Switches	Series	$(\frac{mG}{2}-\frac{m_{ric}}{4})\cdot\cos\varphi+\frac{1}{2}$	$(\frac{mG}{2}-\frac{m}{4})\cdot\cos\varphi+\frac{1}{2}$	-	G
	DC-link	$(\frac{mG}{2}-\frac{m_{ric}}{4})\cdot\cos\varphi+\frac{1}{2}$	$(\frac{mG}{2}-\frac{m}{4})\cdot\cos\varphi+\frac{1}{2}$	-	-
	SMs	$\frac{m_{ric}}{4}\cdot\cos\varphi+\frac{1}{2}$	$\frac{m}{4}\cdot\cos\varphi+\frac{1}{2}$	$\frac{m\cdot G}{4}\cdot\cos\varphi+\frac{1}{2}$	$\frac{G+1}{2}$
Inductors	qZS	$\frac{m\cdot G}{4}\cdot\cos\varphi$	$\frac{m\cdot G}{4}\cdot\cos\varphi$	-	$G/2$
	Arm	$\frac{m_{ric}}{4}\cdot\cos\varphi+\frac{1}{2}$	$\frac{m}{4}\cdot\cos\varphi+\frac{1}{2}$	$\frac{m\cdot G}{4}\cdot\cos\varphi+\frac{1}{2}$	-

6.1.3 Conduction and switching losses

The analytical expressions of the conduction and the switching losses of the proposed converter have been previously given in section 5.1.2 for the SS and RICs techniques. In addition, the conduction and switching losses expressions have been considered also for the FB-MMC and the qZS-CMI, and are detailed in Appendix C.

These analytical expressions have been used to compare the converter losses for the three topologies where the integration of power losses has been executed over a duration equal to the fundamental period to be able to calculate the average losses. The case study employed in section 5.1.2 has been used here for comparison purpose. The switch type which has been previously used in section 5.1.2, which was the MITSUBISHI CM800HA-66A IGBT, 3.3kV and 800A, is also employed in this section to make the results of the comparison compatible. The conduction and switching characteristics of the IGBT module used, that have been determined by the manufacturer, are summarised in Appendix B.

The qZS-MMC is modulated using the SS and RICs techniques, and the FB-MMC is modulated using the phase disposition PWM (PD-PWM) [4], while the qZS-CMI is modulated using the phase-shift PWM (PS-PWM) technique [76]. The frequency of the triangular carrier signal f_c is chosen to be 4 kHz for the qZS-MMC and the FB-MMC. To ensure a fair comparison, the PS-PWM technique used for the qZS-CMI is adjusted to achieve the same number of switch transitions as the PD-PWM, by setting the carrier frequency to f_c / N_{SM} = 4 kHz/8 = 500 Hz for the cascaded units in this case. It is worth to mention that the resulting shooting-through frequency is 1 kHz for the qZS-CMI due to shooting-through two times during one switching frequency cycle, while it is 4 kHz for the qZS-MMC.

The percentage ratio of the conduction, switching and overall losses relative to the active output power for the three topologies (but two cases are considered for the proposed qZS-MMC) are shown in Fig. 6.1 for buck operating mode at gain values of 0.75 and 1.0 and Fig. 6.2 for boost operating mode at gain values of 1.5, 1.75 and 2.0. These curves have been drawn using the analytical

expressions corresponding to each topology, which have also been validated using the simulation models for each topology.

From the two figures, it can be concluded that:

- The qZS-CMI causes the highest conduction losses, and the conduction losses of FB-MMC is higher than the proposed qZS-MMC.
- The qZS-MMC and the FB-MMC have equal switching losses in buck mode. Also, both topologies mentioned have switching losses higher than the qZS-CMI. While in boost mode, the qZS-MMC with RICs technique has switching losses lower than the qZS-MMC with SS technique (as illustrated previously in section 5.1.2) and both are higher than qZS-CMI, and FB-MMC has the lowest switching losses.

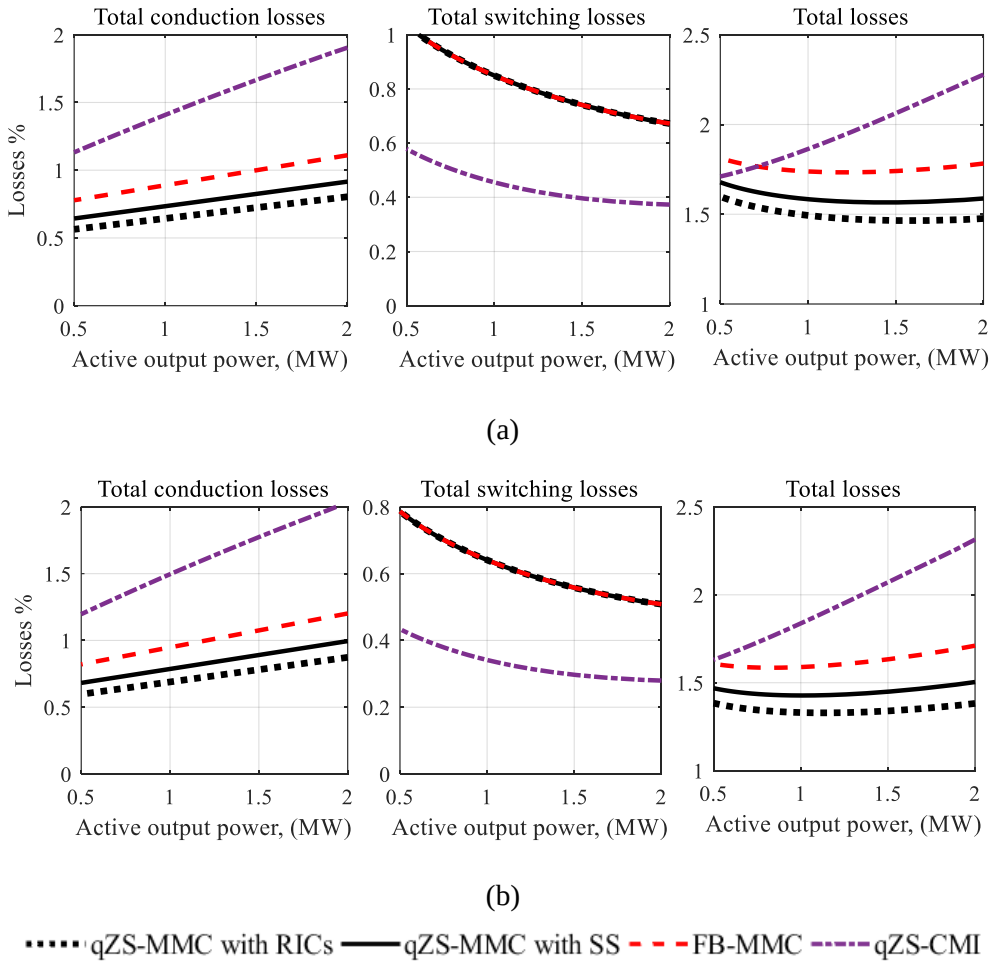


Fig. 6.1: Summarised conduction, switching, and total power losses percentage of the qZS-MMC with RICs technique, qZS-MMC with SS technique, qZS-CMI and FB-MMC in buck mode for gain values of: a) 0.75, and b) 1.0

- With respect to the total losses (conduction and switching), the proposed qZS-MMC has the lowest total losses in buck mode. On the other hand, the FB-MMC has the lowest total losses in boost mode. The qZS-MMC with SS technique causes total losses higher than the qZS-CMI, and both of them are higher than the qZS-MMC with RICs.

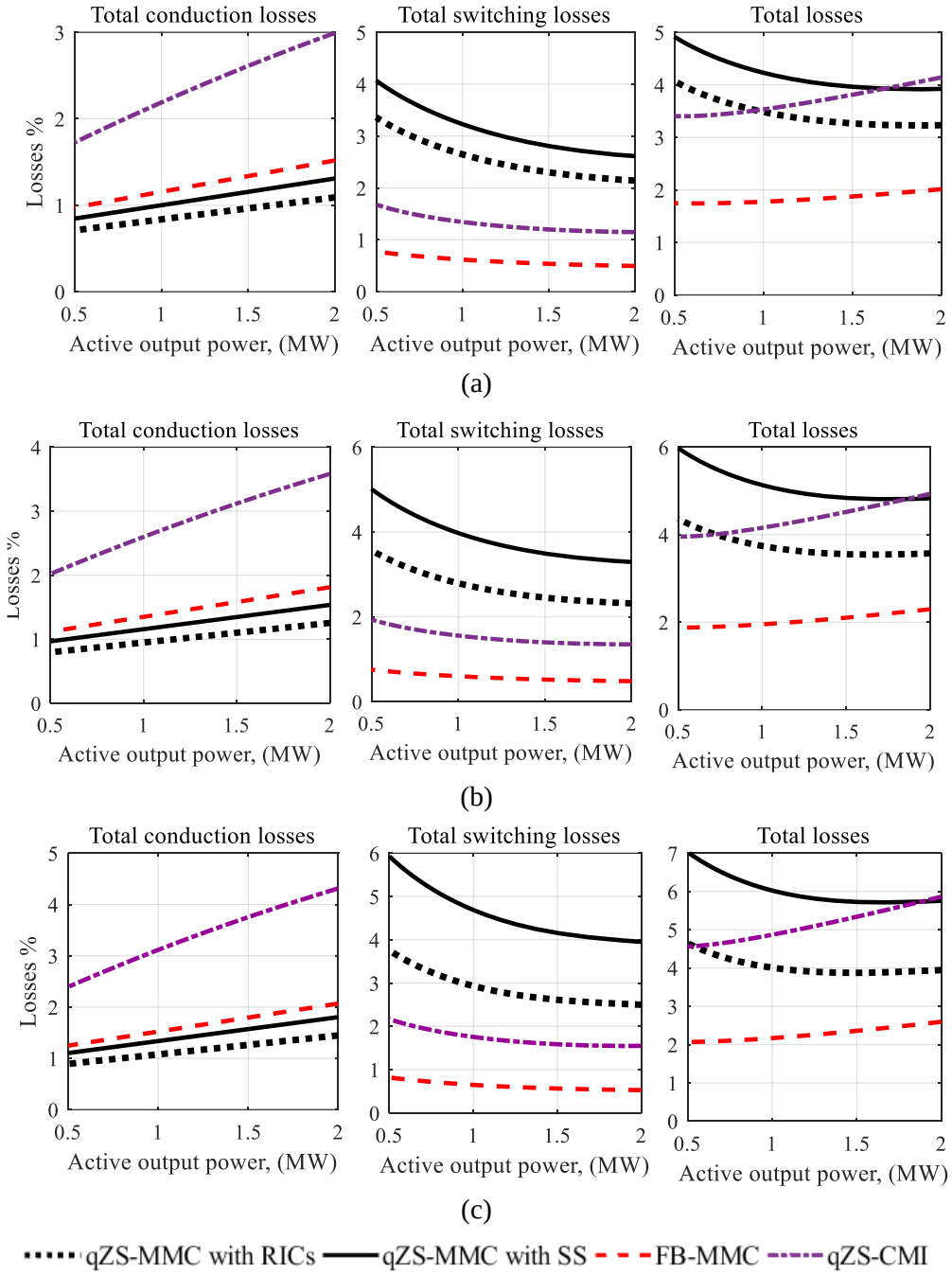


Fig. 6.2: Summarised conduction, switching, and total power losses percentage of the qZS-MMC with RICs technique, qZS-MMC with SS technique, qZS-CMI and FB-MMC in boost mode for gain values of: a) 1.5, b) 1.75 and c) 2.0

In this case, the shooting-through frequency was 1 kHz for the qZS-CMI and 4 kHz for the qZS-MMC. However, if the shooting through frequency for the qZS-MMC is adjusted to be 1 kHz, the same shooting through frequency as of the qZS-CMI, then the qZS-MMC will be more efficient compared to the qZS-CMI as shown in Fig. 6.3 at gain values of 1.5 and 2.0.

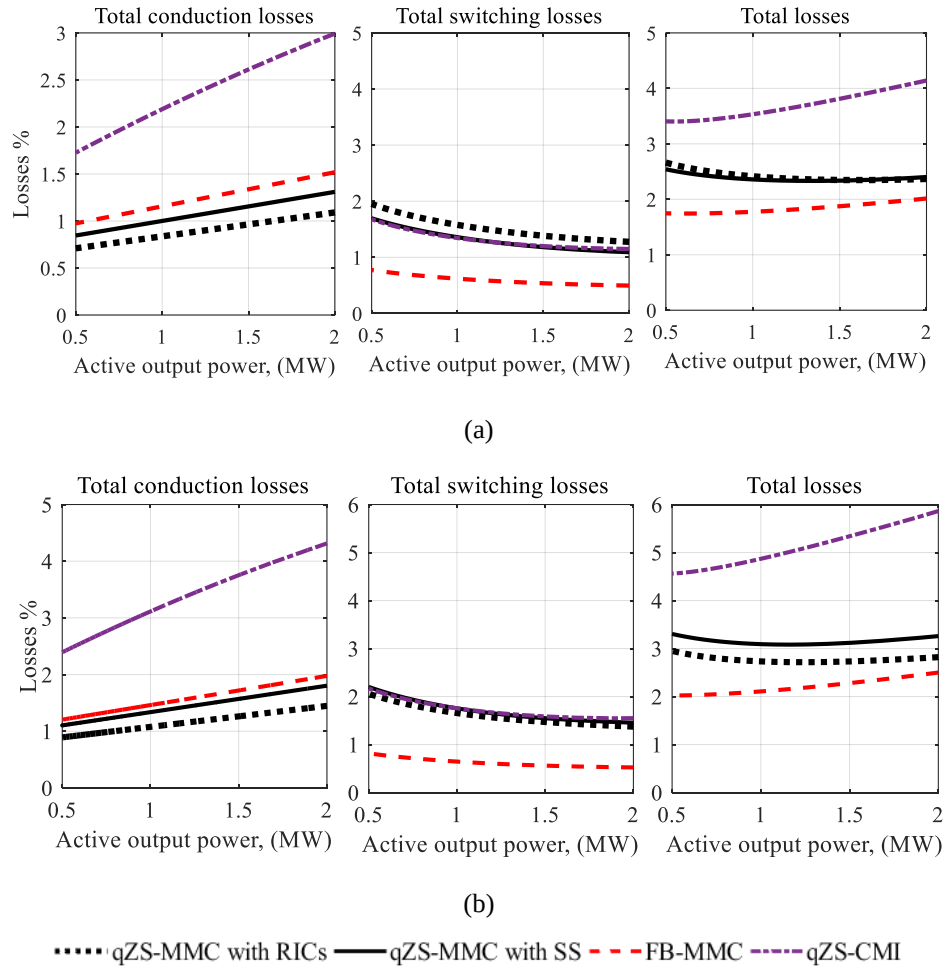


Fig. 6.3: Summarised conduction, switching, and total power losses percentage of the qZS-MMC with RICs technique, qZS-MMC with SS technique, qZS-CMI and FB-MMC at 1 kHz shooting through frequency in boost mode for gain values of: a) 1.5, and b) 2.0

The analytical evaluation of the conduction and switching losses for each topology has been validated using simulation models for each case at an output active power of 1.4 MW and voltage gain values of 0.75, 1, 1.5, and 2.0. The models have been built using PLECS software, where for each device, a loss model can be assigned, characterized by the turn-on, turn-off and recovery switching energy and by the forward voltage and current relation.

Depending on the datasheet parameters of the selected devices, formulas or look-up tables can be extracted and inserted into the PLECS thermal library. As previously mentioned, the MITSUBISHI CM800HA-66A IGBT, with power loss characteristics given in Appendix B, has been used for all topologies for comparison purpose. The simulation results are given in Table 6.4. Comparing these results with those expected by the analytical models shows a high degree of matching. For instance, in the simulation results at G = 1, the proposed qZS-MMC when using RICs and SS techniques, the FB-MMC and the qZS-CMI have total loss of 1.38%, 1.5%, 1.8% and 2.2% respectively which are slightly higher than the values obtained from the analytical models, which are 1.35%, 1.45%, 1.7% and 2.1% respectively (refer to Fig. 6.1). While for G = 2, the total loss is 3.9 %, 5.5 %, 2.6 %, 5.2% for the four topologies, respectively, which are slightly different from the values obtained from the analytical models, which are 3.9%, 5.3%, 2.4% and 5.5% respectively (refer to Fig. 6.2).

Table 6.4: Simulation result of conduction, switching and total losses

	Losses in kW (and % of 1.4MW)					
	Con.	Sw.	Total	Con.	Sw.	Total
	G = 0.75			G = 1.5		
A	14.5	10.8	25.3 (1.8%)	19.8	7.5	27.3 (1.9%)
B	23.4	5.6	28.6 (2.4%)	38	18.1	56.1 (4%)
C	11.6	10.1	21.7 (1.46%)	14.7	33.4	48.1 (3.4%)
D	13.4	10.1	23.5 (1.6%)	17.4	40.2	57.6 (4.1%)
	G = 1.0			G = 2.0		
A	16.8	8.6	25.4(1.8%)	28.1	7.6	35.7 (2.6%)
B	26	4.3	30.4 (2.2%)	57	23.5	72.1 (5.2%)
C	11.9	7.3	19.4 (1.38%)	18.2	36.9	55.1 (3.9%)
D	13.7	7.3	21 (1.5%)	21.9	56.2	78.1 (5.5%)

A: FB-MMC **B:** qZS-CMI **C:** qZS-MMC with RICs **D:** qZS-MMC with SS

6.1.4 PWM harmonics profile

The harmonic spectrum of the output voltage produced by the single phase circuit of FB-MMC, the qZS-CMI and the qZS-MMC are compared and shown in Fig. 6.4 for gain values of 1.0, 1.5, 1.75, and 2.0. The SS and RICs techniques produce similar harmonic profile, therefore, the harmonic profile has been shown only for the RICs technique.

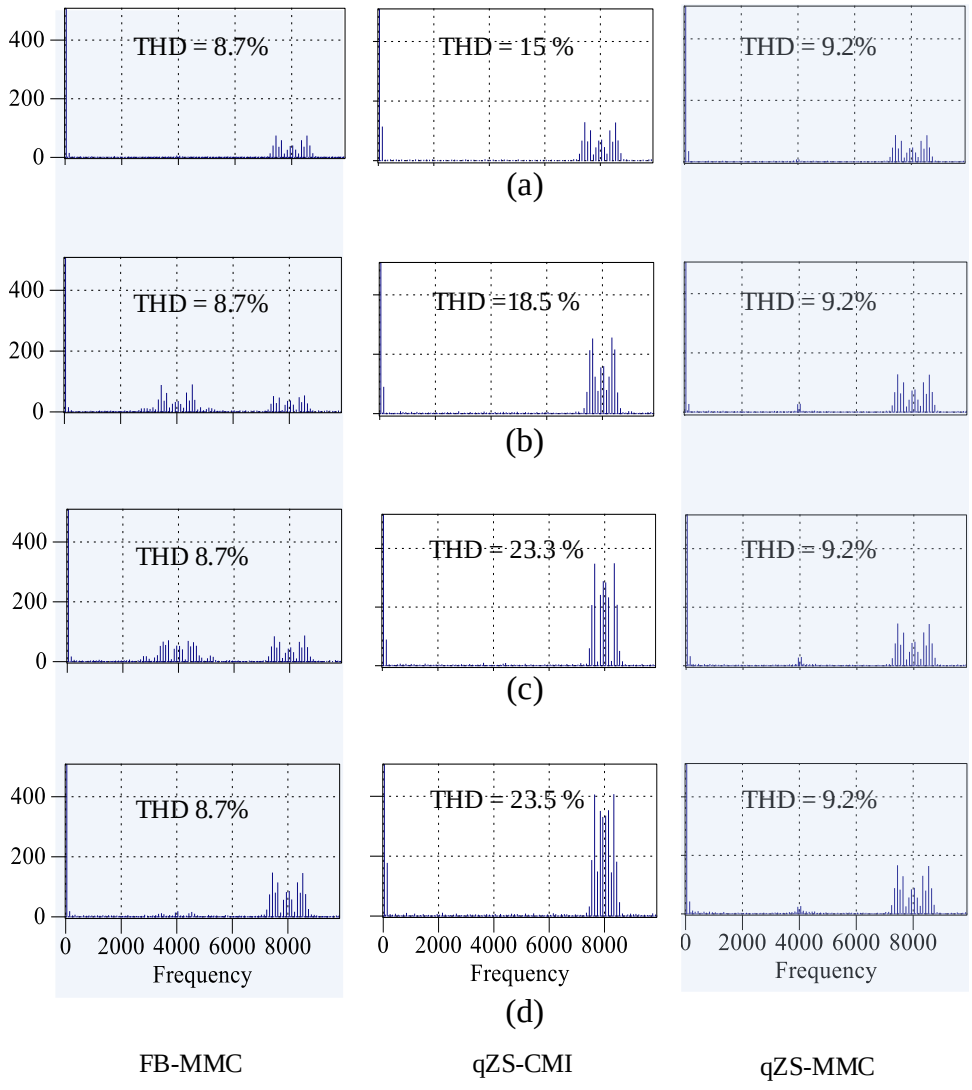


Fig. 6.4: The FFT analysis of the output AC voltage when the converters work at: a) G = 1.0, b) G = 1.5, c) G = 1.75, and d) G = 2.0

It is noted that the switching harmonics of the qZS-MMC appear as sideband clusters at the carrier frequency where the most dominant harmonic cluster is located at twice the carrier frequency ($2f_c$ = 8 kHz) for all gain values.

The harmonic profile of the FB-MMC at gain equals 1.0 and 2.0 is similar to the qZS-MMC. However, at intermediary gain values, an additional dominant harmonic cluster appears for the FB-MMC at the carrier frequency. This is an important finding since a larger harmonic cluster at lower frequency will require an increased size for the output AC filter. The switching harmonics of the qZS-CMI appear as sideband cluster at 8 kHz for all gain values.

The total harmonic distortion THD of the output voltage of the qZS-MMC and FB-MMC is approximately equal to 9.2% and 8.7% for all gain values respectively. For the qZS-CMI, the THD is higher and equals to 15%, 18.2%, 23.3%, and 23.5% for the gain values of 1.0, 1.5, 1.75, and 2.0 respectively. To increase the gain of the qZS-CMI, the modulation index should decrease with increasing the shoot through duty ratio [65] which leads to a drop in the output voltage level, while the modulation index could be maintained fixed for all gain values for the other two converters.

In the previous comparison, the proposed converter has been compared with one of the MMC family (FB-MMC) and with one of impedance network based CMI (qZS-CMI). It is worth to mention that the proposed converter can be also compared with the traditional boost converter based MMC (hereafter named as Boost-MMC), but it is not included in this thesis. However, through a simple analysis, for the same voltage stress, the proposed qZS-MMC using RICs technique requires the same number of semiconductor devices when compared with the Boost-MMC. Both qZS-MMC using RICs technique and Boost-MMC approximately have equal total losses. The proposed converter requires smaller SM capacitor size, while it requires slightly larger size of the other passive components.

6.2 DC-fault blocking

During DC-side faults, the traditional MMC with HBSM does not provide fault current blocking and a high current flows from the AC grid into the fault [83].

This is a result of the presence of freewheeling diodes that provide an uncontrolled current path for the DC-fault to be fed from the AC grid through the upper and lower arm. This current may reach high levels and damage the switching devices if not detected and isolated by dedicated fast acting protection devices such as circuit breakers.

Several modifications have been carried on the SMs to overcome these issues such as:

1. Thyristors [121, 122]: Adding thyristors in parallel connection to the output terminals of the HBSM has been applied to hold the fault current and consequently protect the freewheeling diodes of the SMs. However, the fault is still not isolated and further devices like circuit breakers are still required.
2. Full-Bridge SMs (FBSMs) [83]: The output terminal voltage of the FBSM has zero, positive and negative voltage values. Since the capacitors of all FBSMs appear as a series connected DC sources (of negative voltage value) in each arm with total arm voltage higher than the peak value of the AC voltage, the DC-faults can be blocked. The FBSMs require twice as many IGBTs as the HBSM, which not only increases the converter cost, but also significantly increases the conduction power losses since the arm current passes through two devices instead of only one for the HBSM.
3. Hybrid connected SMs [29]: by combining FBSMs and HBSMs, sufficient negative arm voltage may be produced that can provide DC-fault blocking capability. The ratio of FBSMs to HBSMs should be at least 1:1.

6.2.1 qZS-MMC DC-fault blocking principles

The proposed qZS-MMC has an inherent DC-side fault blocking capability feature when the fault occurs at the DC-terminals (between *X* and *Y* terminals, as shown in Fig. 6.5) of the converter. The fault blocking principle requires the injection of a negative voltage in the path of the fault which is equal to or higher than the peak value of the AC grid voltage, which is the voltage source powering

the short-circuit current. In this converter, the qZS capacitors can be used to block the AC grid current during the fault. This happens when the voltage of the qZS capacitor, that are in the path of the fault, is higher than the grid voltage. Once the over-current is detected, the switches of the HBSM of the MMC leg and the qZS-networks are blocked. The scenarios of pole-to-pole and pole-to-ground DC-faults have been considered separately.

6.2.1.1 Pole-to-pole fault

This fault occurs between the positive and negative terminals of the DC source as shown in Fig. 6.5. After detecting the fault and blocking all converter switches, a resonant current will flow through the qZS-inductors and capacitors where the resonant path and the current direction are highlighted in Fig. 6.5. This current makes the qZS-capacitor of voltage V_{CU1} to discharge and the qZS-capacitor of voltage V_{CU2} to charge until capacitor voltages V_{CU1}, and V_{CU2} become equal, assuming they have the same capacitance. Considering $V_{CU1} = V_{CN1} = V_{C1}$ and $V_{CU2} = V_{CN2} = V_{C2}$, the qZS-capacitor voltages V_{C1} and V_{C2} are:

$$V_{C1} = \left(V_{C1}(0) + V_{C2}(0)\right) \times \frac{C_2}{(C_1 + C_2)}$$
$$V_{C2} = \left(V_{C1}(0) + V_{C2}(0)\right) \times \frac{C_1}{(C_1 + C_2)} \tag{6.1}$$

where $C_{U1} = C_{N1} = C_1$, $C_{U2} = C_{N2} = C_2$. $V_{C1}(0)$ and $V_{C2}(0)$ are the values of qZS-capacitor voltages before the fault happens. The resonant current flows only through the passive components in the qZS-network and does not flow through the semiconductor devices of the qZS-network and SMs.

The AC grid can feed the fault through the antiparallel diodes D_1 in both arms. The positive polarity of the AC grid current flows through D_1 in the upper arm, while the negative polarity of the AC grid current flows through the lower arm as shown in the Fig. 6.6. In both paths, the qZS-capacitors, with an equivalent voltage of $2V_{C2}$-V_{C1}, are in the fault path and can be used to block the AC grid current.

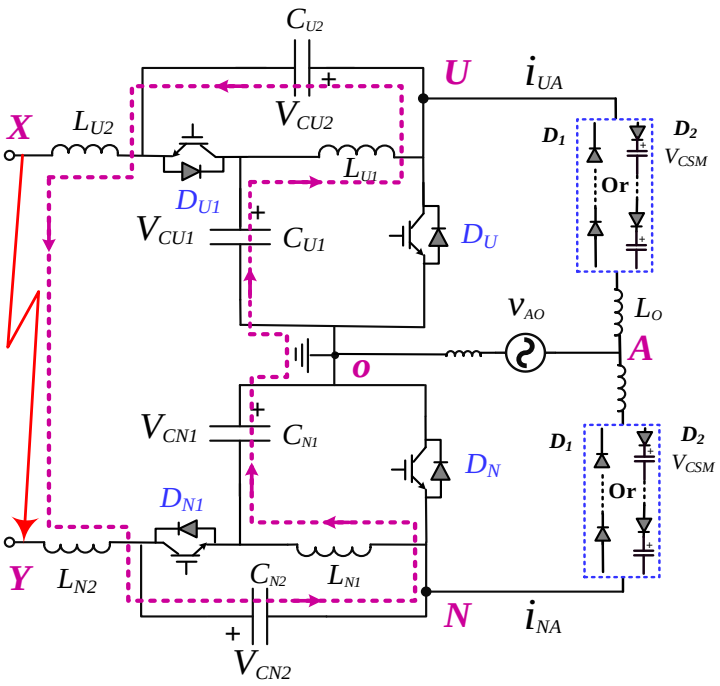


Fig. 6.5: Schematic of the DC-fault resonant current path after blocking IGBTs under pole-to-pole DC-fault

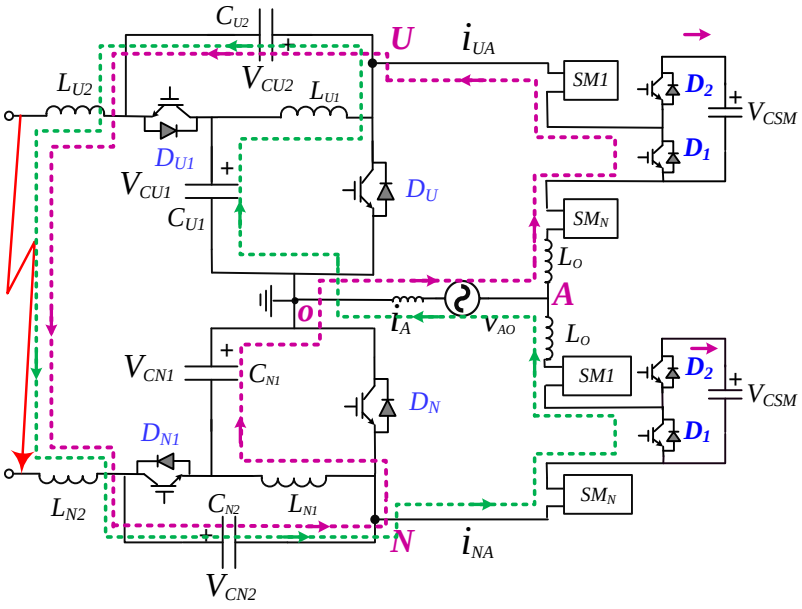


Fig. 6.6: DC-fault current path pole-to-pole DC-fault

There are two possibilities of fault blocking, if the equivalent qZS-capacitor voltage $2V_{C2}$-V_{C1} are equal to or larger than the peak value of the AC voltage, the remaining voltage in the loop will be negative, making the arm current to decrease to zero and then this negative voltage will keep these diodes turned off and the fault turned into an open circuit. On the other hand, if the equivalent

voltage $2V_{C2}$-V_{C1} are smaller than the peak value of the AC voltage, a current will flow from the grid into the DC side fault causing a charge of the qZS-capacitors. Once the qZS-capacitor voltages exceed the peak value of the AC voltage, the AC grid current and the arm currents will start to decrease towards zero and the DC-fault can be completely blocked as explained earlier.

6.2.1.2 Pole-to-ground fault

This fault occurs between the positive (or negative) terminal of the DC source and the ground terminal '*O*' as shown in Fig. 6.7. In this case, the upper and the lower qZS-networks show different behaviors. Considering the fault is imposed between the positive and the ground terminals, after detecting the fault and blocking all converter switches, a resonant current will flow through the upper qZS-network. The resonant path and the current direction are highlighted in the Fig. 6.7. This current makes the qZS-capacitor of voltage V_{CU1} to discharge and the qZS-capacitor of voltage V_{CU2} to charge until capacitor voltages V_{CU1}, and V_{CU2} become equal (assuming they have the same capacitance) and can be determined by (6.2).

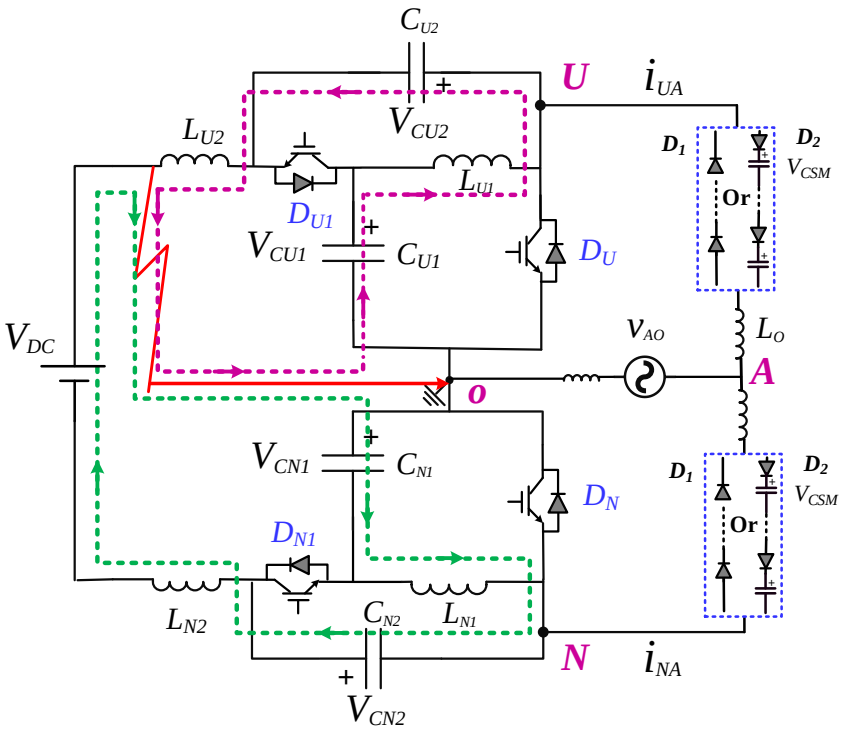


Fig. 6.7: DC-fault resonant current path in the upper and lower qZS-networks after blocking IGBTs under pole-to-ground DC-fault

$$V_{CU1} = V_{CU2} = \frac{V_{CU1}(0) + V_{CU2}(0)}{2} \tag{6.2}$$

where $V_{CU1}(0)$ and $V_{CU2}(0)$ are the values of qZS-capacitor voltages before the fault occurrence.

Another transient current will flow through the lower qZS-network as highlighted in the Fig. 6.7. This current makes the qZS-capacitor C_{N1} to charge and the C_{N2} to discharge where the qZS-capacitor voltages V_{CN1}, and V_{CN2}, at the end of the oscillation are:

$$\begin{aligned} V_{CN1} &= \frac{V_{CN1}(0) + V_{CN2}(0)}{2} + \frac{V_{DC}}{2} \\ V_{CN2} &= \frac{V_{CN1}(0) + V_{CN2}(0)}{2} - \frac{V_{DC}}{2} \end{aligned} \tag{6.3}$$

where $V_{CN1}(0)$ and $V_{CN2}(0)$ are the values of qZS-capacitor voltages before the fault occurrence.

The AC grid can feed the fault through the antiparallel diodes D_1 in the upper arm as shown in the Fig. 6.8. In this path, the qZS-capacitor of voltage of V_{CU2}, is connected with opposite polarity which helps to block the AC grid current. There are two possibilities of fault blocking as follows. If the qZS-capacitor voltage V_{CU2} is equal to or larger than the peak value of the AC voltage, the voltage in the loop will be negative, making the antiparallel diodes turned off. while, if the qZS-capacitor voltage V_{CU2} is smaller than the peak value of the AC voltage, a current will flow from the AC grid to the DC fault causing the qZS-capacitor C_{U2} to charge. Once the qZS-capacitor voltage V_{CU2} exceeds the peak value of the AC voltage, the AC grid current and the arm currents will start to decrease towards zero and the DC-fault can be completely blocked.

There is another path for the AC grid current to feed the fault, which is through the diode D_2 and SM capacitor of the lower arm, as shown in Fig. 6.8. The equivalent loop voltage in the path of the fault is $v_{AO} + V_{DC} + V_{CN2} - N_{SM}.V_{CSM}$, where V_{CN2} is defined by (6.3).

If $v_{AO} + V_{DC} + V_{CN2} \leq N_{SM}.V_{CSM}$, the loop voltage will be negative, which makes the loop diodes turned off. If $v_{AO} + V_{DC} + V_{CN2} > N_{SM}.V_{CSM}$, a current will flow from the grid to the DC fault causing the lower arm SM capacitors to charge. Once the lower arm total SM capacitors voltage $N_{SM}.V_{CSM}$ exceeds $v_{AO} + V_{DC} + V_{CN2}$, the loop voltage will be negative which will allow all the diodes in the fault path to become reverse biased.

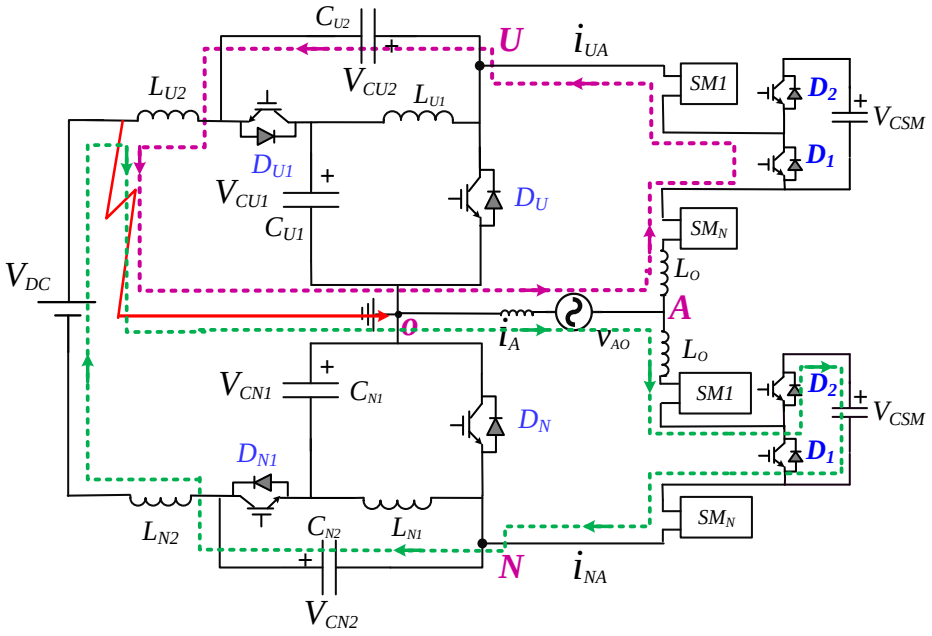


Fig. 6.8: DC-fault current path under pole-to-ground DC-fault

6.2.2 Simulation results

To assess the response of the proposed qZS-MMC to a pole-to-pole and pole-to-ground DC-side faults, an AC voltage source has been added at the AC output terminals of the qZS-MMC that is able to source and sustain a faulty current in the circuit. The simultaneously shorted modulation technique presented in Section 4.3.1 is used. The test has been carried out considering that the DC source voltage is 7.3 kV and peak AC grid voltage is 5.5 kV. The parameters used for the simulation model are presented in Table 6.5.

Table 6.5: Parameters of the simulation model

Parameter	Value
DC source voltage (V_{DC})	7.3 kV
Peak output voltage (V_m)	5.5 kV
SM capacitor voltage (V_{CSM})	1.36 kV
Power rating	1.4 MW
Number of SMs per arm (N_{SM})	8
Arm inductance (L_o)	5 mH
SMs capacitances (C_{SM})	3.3 mF
qZS inductances ($L_{U1} = L_{U2} = L_{N1} = L_{N2}$)	10 mH
qZS capacitances ($C_{U1} = C_{N1}$)	3.3 mF
qZS capacitances ($C_{U2} = C_{N2}$)	3.3 mF
Carrier frequency (f_c)	4 kHz

6.2.2.1 Pole-to-pole DC-fault

The DC-fault has been imposed at t =1.5 s by using an ideal switch in series with a 1 Ω resistor between points X and Y as shown in Fig. 4.13. The DC source voltage, which is set initially to 7.3 kV, reduces quickly to small value level as shown in Fig. 6.9a.

Once the fault is detected, where the controller detects the fault by monitoring the DC-side current (i_{LU2}) such that this current increases exceeding an overcurrent of -2I_L, all converter IGBTs are turned off. After the IGBTs are blocked, the qZS-capacitors C_{U1}, C_{N1} (which initially have been charged to larger voltages) start to discharge and C_{U2}, C_{N2} (which initially are charged to smaller voltages) start to charge until their voltages become approximately equal as illustrated in Fig. 6.9b. The upper and lower SM capacitor voltages remain mostly unchanged after SMs switches blocking as shown in Fig. 6.9c and Fig. 6.9d.

As is shown in Fig. 6.10, the grid current and the upper and lower arm currents dropped significantly when all the IGBTs have been blocked and their values approach zero.

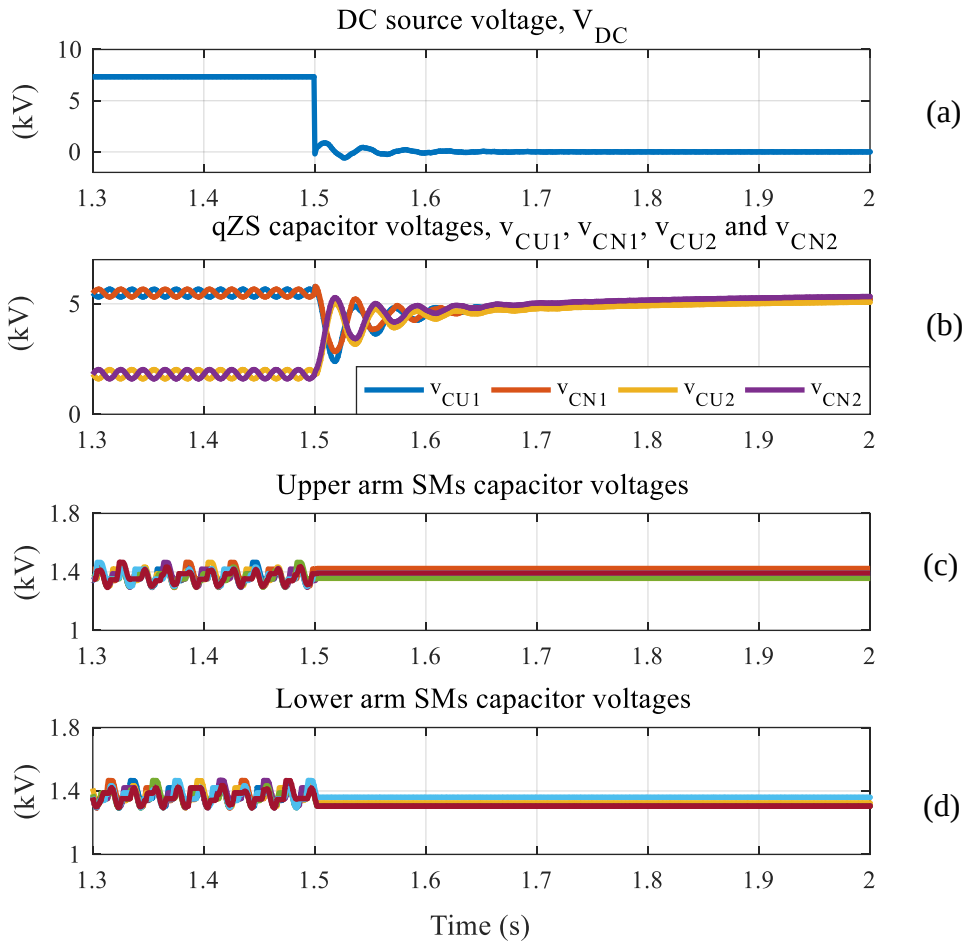


Fig. 6.9: Pole-to-pole DC-fault simulation: a) DC source voltage, b) qZS capacitor voltages, c) and d) upper and lower SMs capacitor voltages.

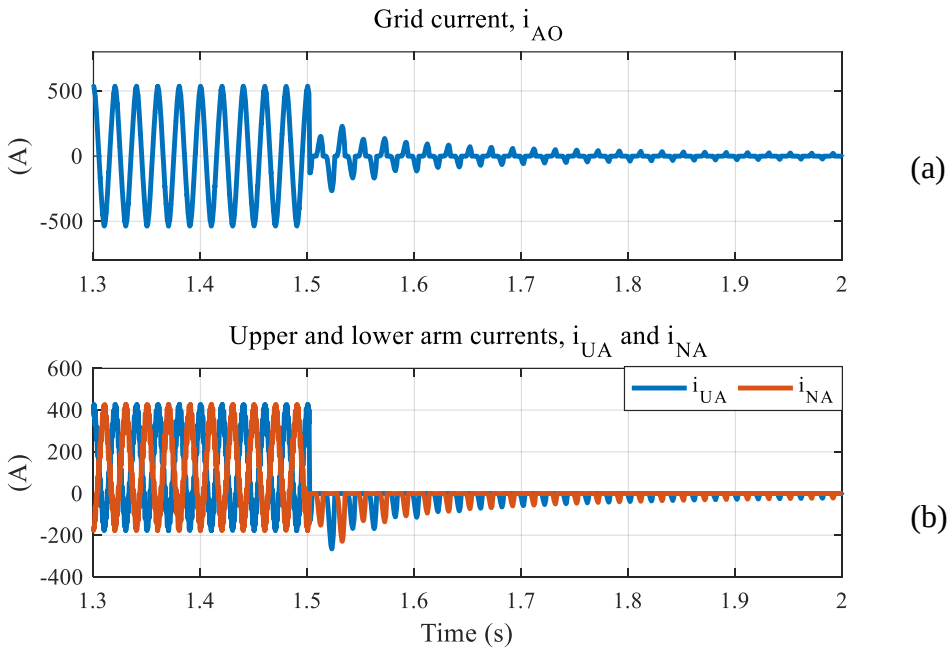


Fig. 6.10: Pole-to-pole DC-fault simulation: a) grid current and b) upper and lower arm currents.

It is worth noting that the grid and arm currents do not reach zero immediately after blocking the IGBTs, where a small current continues to flow through the freewheeling diodes D_1 in both the upper and lower arm. This happens when the instantaneous value of the grid voltage is higher than the qZS capacitors voltages, resulting in charging of the qZS-capacitors.

The full and continuous faulty current blocking requires additional time and occurs when the residual current causes the qZS-capacitors voltages to increase above the peak value of grid voltage, which will then produce a negative residual voltage in the faulty circuit and will allow all the diodes to become reverse biased.

The inductor currents i_{LU1}, i_{LU2}, i_{LN1}, and i_{LN2} fluctuate following a natural resonance as shown in Fig. 6.11a until they settle to zero which coincides with an absolute peak overshoot current of approximately 4.1 times the operating current from the pre-fault condition. This over-shoot current may lead to saturation of the inductor core, if iron core is used, during this short period of over-shoot. This saturation will not affect the fault detection and isolating the converter as the fault detection threshold level is only $2I_L$. It is worth to mention that, it should be noted that the resonant current only flows through the inductors and the capacitors of the qZS-networks and this current does not flow through the qZS switches S_U, S_N, S_{U1} and S_{N1} as discussed and shown in Fig. 6.5. The currents i_{SU} and i_{SU1} are shown in Fig. 6.11b and Fig. 6.11c (the current has been measured in the same direction of the diode positive current).

6.2.2.2 Pole-to-ground DC-fault

The DC-fault is imposed between the positive and the ground terminals at t =1.5 s by using an ideal switch in series with a 1 Ω resistor between points X and O, as shown in Fig. 4.13.

Once the fault is detected, all converter IGBTs are turned off. The capacitors of the upper network C_{U1} and C_{U2} start to discharge and charge respectively until their voltages become approximately equal (according to (6.2)) as shown in Fig. 6.12a. The qZS-capacitor C_{N1} charges and the qZS-capacitor C_{N2} discharges as shown in Fig. 6.12a where their voltages reach to V_{DC} and zero respectively according to (6.3) for this case. On the other hand, the upper arm SMs capacitor voltages remain mostly unchanged as shown in Fig. 6.12b.

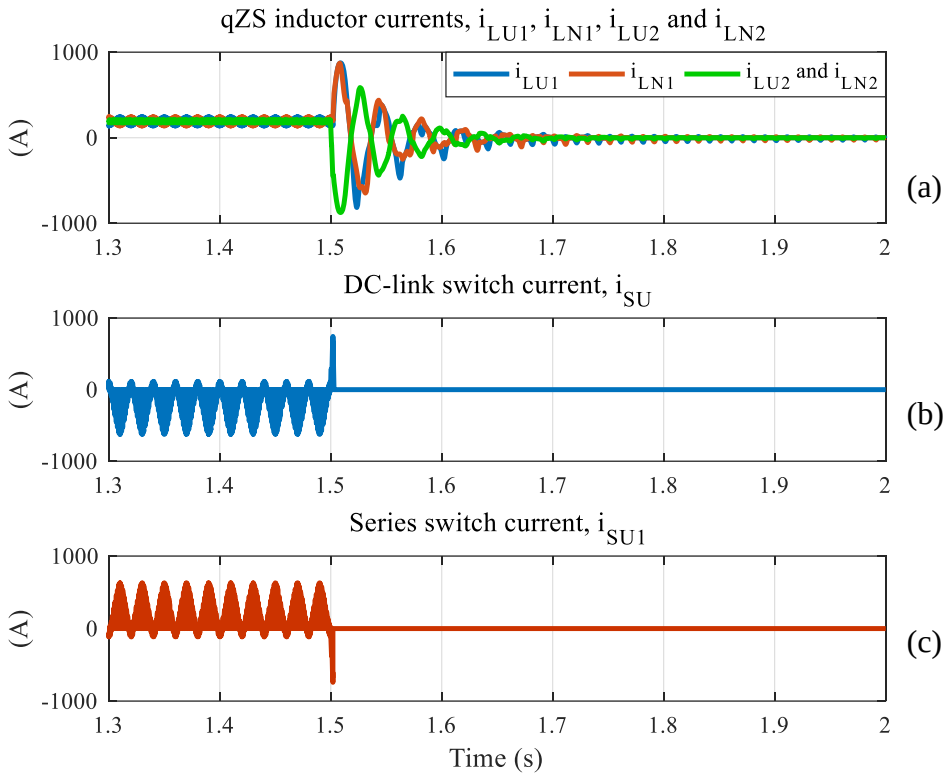


Fig. 6.11: Pole-to-pole DC-fault simulation: a) qZS inductor currents, b) DC-link switch current i_{SU} and c) series switch current i_{SU1}

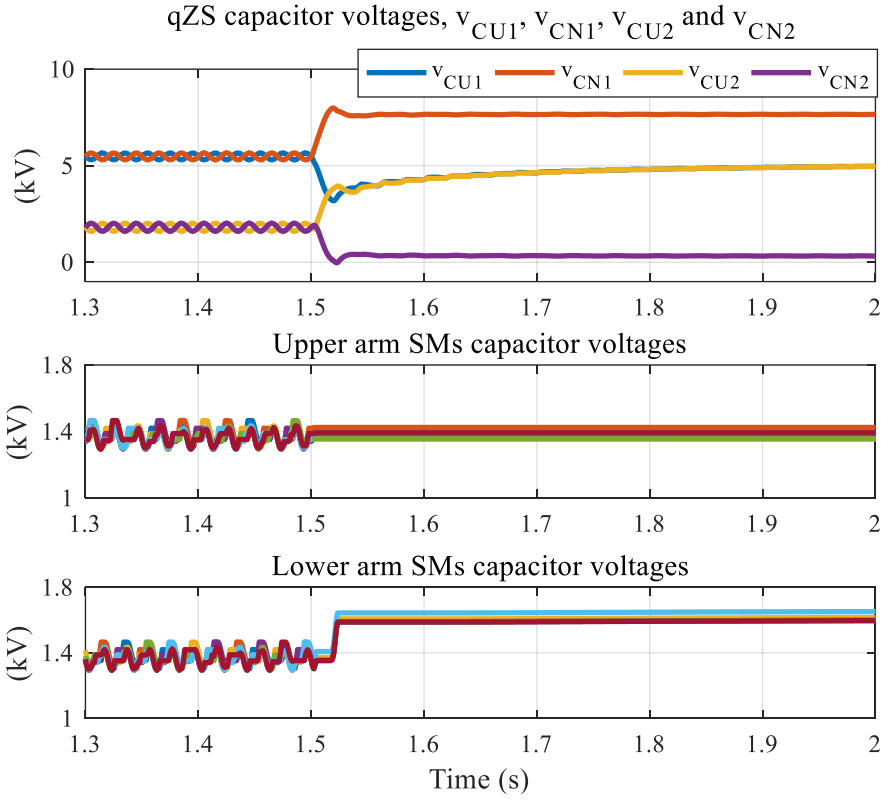


Fig. 6.12: Pole-to-ground DC-fault simulation: a) qZS capacitor voltages b) and c) upper and lower SMs capacitor voltages respectively.

Whereas a current (as explained in Section 6.2.1.2) will flow through the lower arm series SMs capacitors causing a charge of all capacitors until their total voltage ($N_{SM}.V_{CSM}$) becomes equal to the summation voltage ($v_{AO} + V_{DC} + V_{CN2}$) and then the voltages remain mostly unchanged, as shown in Fig. 6.12c.

Fig. 6.13 shows the grid current and the upper and lower arm currents. The upper arm current i_{UA} does not reach zero immediately after blocking the IGBTs, where a small current continues to flow through the freewheeling diodes D_1 in the upper arm, which causes the upper qZS-capacitors to charge. The complete upper arm current blocking requires additional time and occurs when the upper capacitor voltages increase above the peak value of grid voltage, which will allow all the diodes to become reverse biased. On the other hand, the lower arm current i_{NA} reaches zero within a short period, and faster than the upper arm current i_{UA}.

After blocking the IGBTs, the inductor currents i_{LU1}, i_{LU2}, i_{LN1}, and i_{LN2} fluctuate as shown in Fig. 6.14a until they settle to zero with an absolute peak overshoot current of approximately 2.7 times the operating current peak from the pre-fault condition. However, this current does not flow through the chain-link switches S_U, S_N, S_{U1} and S_{N1} as discussed and shown in Fig. 6.7 and therefore has no impact on the need to oversize the semiconductor devices to withstand a DC-fault. The series and DC-link switch currents i_{SU} and i_{SU1} are illustrated in Fig. 6.14b and Fig. 6.14c.

To conclude, these results verify the DC-fault blocking capability of the proposed qZS-MMC under pole-to-pole and pole-to-ground faults. The qZS switches and capacitors that are already present in the converter are utilized to also block the DC-fault, where the current peaks can be successfully limited at a safe level that depends on how fast the fault is detected and consequently the short-circuit DC-link current can be cleared quickly. The overcurrent affects only the passive components in the qZS-network stage and therefore do not require oversizing of the semiconductor devices of the qZS-network and SMs.

6.3 Conclusions

In this chapter, a comprehensive comparison of the qZS-MMC, the FBSMs based MMC (FB-MMC) and quasi Z source cascaded multilevel converter (qZS-CMI) has been carried out.

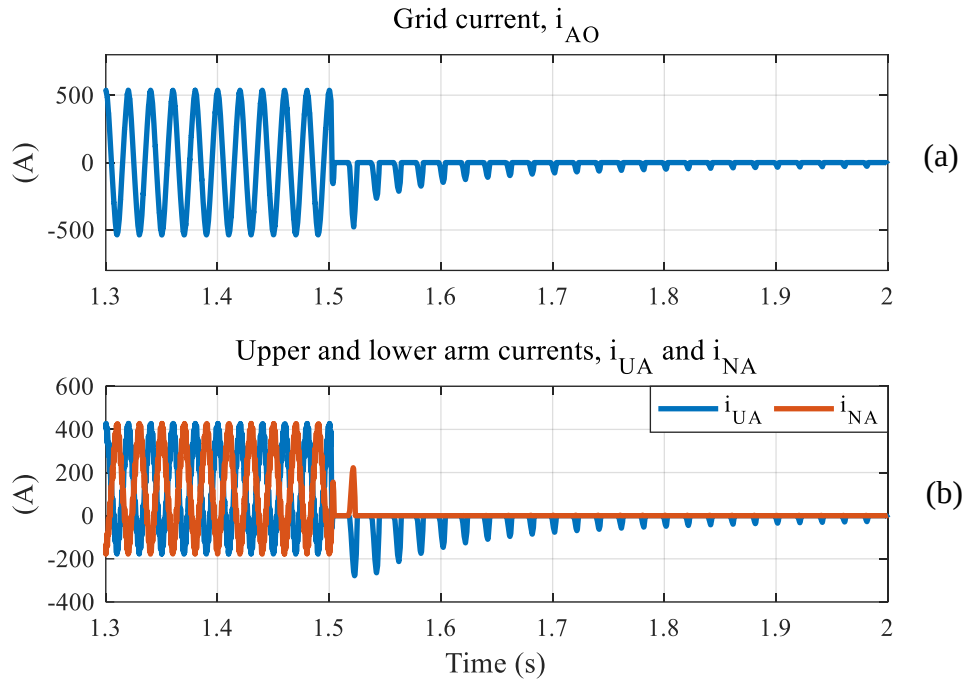


Fig. 6.13: Pole-to-ground DC-fault simulation: a) grid current and b) upper and lower arm currents.

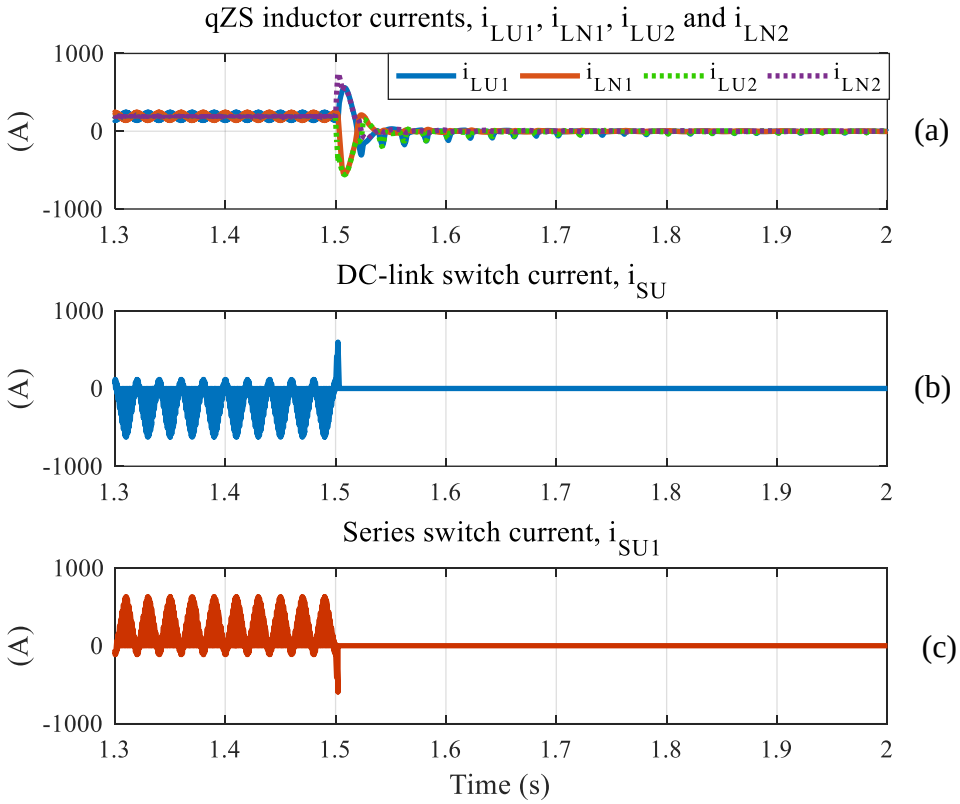


Fig. 6.14: Pole-to-ground DC-fault simulation: a) qZS inductor currents, b) DC-link switch current i_{SU} and c) series switch current i_{SU1}

Firstly, the number of IGBTs necessary to build the proposed qZS-MMC controlled by the RICs and SS technique are found to be only 75 % and 87.5 % of that required for the FB-MMC in the case of single-phase converter, which is a significant reduction. Regarding the passive elements, the qZS-MMC uses four more inductors and two more capacitors compared to FB-MMC, while the qZS-CMI requires more inductors, capacitors and isolated DC sources depending on the number of sub-modules.

Another aspect of the comparison considered also the voltage and current stresses. The voltage stresses of the series and the chain-link switches of the qZS-MMC when using RICs technique are lower than those of the qZS-MMC when using SS technique and both are higher than those of the qZS-CMI at the same output voltage. The SM switches stress voltages are equal for qZS-MMC and FB-MMC, and both are higher than those of the qZS-CMI. The qZS-CMI has the lowest voltage stress on SMs and qZS-switches. The qZS capacitor voltage of the qZS-CMI is lower than of that of the qZS-MMC. Although the qZS-CMI switches get the lowest voltage stress, the number of the required switches is higher. Regarding the current stresses, the proposed converter has the lowest current stresses among the three topologies in terms of SMs current, arm inductor current and qZS inductor current. The FB-MMC gets a higher current stress for the arm inductor compared with the qZS-MMC. The current stress of the qZS inductor of the proposed qZS-MMC are half the value of the qZS-CMI.

The following aspect of the comparison was in terms of semiconductor device losses, where the proposed qZS-MMC is the most efficient in buck mode. However, the FB-MMC is the most efficient in boost mode, especially with increasing the converter gain.

Finally, when comparing the performance from harmonic content in the output voltage point of view, the FB-MMC has a significant harmonic cluster in the output voltage at the switching frequency compared to the qZS-MMC which will either require increasing the output AC filter size or doubling the switching frequency. In the latter case, the losses may increase to the point where the MMC becomes less efficient than the proposed qZS-MMC. The THD of the output voltage of the qZS-MMC and FB-MMC are quite close and both are lower than that for the qZS-CMI.

The proposed qZS-MMC was found to be better than the FB-MMC in terms of, a) number of semiconductor devices, b) conduction losses, c) overall losses in buck mode, and d) arm inductor and SMs current stress. However, the qZS-MMC has shortcomings in terms of a) number of passive components (four more inductors and two more capacitors), b) switching losses in boost mode, and c) overall losses in boost mode. When it is compared to the qZS-CMI, the proposed converter was found to be superior in terms of, a) number of semiconductor devices, passive components and isolated DC sources, b) conduction and overall losses in both buck and boost modes, c) THD of the output voltage and d) current stress of passive components and semiconductor devices. On the other hand, the qZS-MMC has higher voltage stress on passive components and semiconductor devices.

Also, in this chapter, the DC-fault blocking capability of the proposed converter has been discussed. The qZS-MMC can provide blocking capability feature where the qZS capacitor, that are in the path of the fault, can facilitate blocking the free-wheeling diodes and therefore remove any DC fault currents. The proposed converter has been tested under pole-to-pole and pole-to-ground DC-faults. Once the fault is detected by the controller, all converter switches are blocked. The arm currents dropped to negligible levels and the qZS-inductor currents fluctuated following a natural resonance until they settle to zero without affecting the qZS switches because the inductor current doesn’t pass through them.

Chapter 7
Experimental Rig and Evaluation

The design of a small-scale laboratory prototype power converter is presented in this chapter. This prototype has been built for the purpose of validating the behavior and the performance of the proposed qZS-MMC. This prototype has been used to assess the two modulation techniques described in this thesis and the circuit capability of blocking DC-faults.

The parameters of the prototype power converter and the control platform, which consists of TMS320C6713 DSP, an FPGA board, and host port interface (HPI) daughter card, are presented. The measurements have been obtained via voltage and current transducers which are connected to the FPGA board. The software used to obtain the experimental results, also discussed.

The experimental results are presented in this chapter using the proposed two modulation techniques: the simultaneously shorted (SS) and the reduced inserted cells (RICs). The operation limitations corresponding to using the series diodes of the qZS-networks are presented in both buck and boost modes and then the effect of using antiparallel switches with the series diodes to solve these limitations is presented. The response of the proposed qZS-MMC to a DC-fault is checked while connecting the AC output terminals of the qZS-MMC to the AC main electrical grid.

7.1 Design consideration for the experimental rig

This section focuses on the design of the prototype to validate the theoretical analysis and the simulation results. The simulation results have been based on a converter with 8 SMs per arm, a peak output phase voltage of 5.5 kV, and a rated power of 1.4 MW. A reduced scale laboratory prototype has 2 SMs per arm, 170 V peak fundamental output voltage and a rated power of 2 kW. For the purpose of proving the converter principles, 2 SMs per arm are sufficient to evaluate the operation principles, the two modulation techniques and the DC-fault blocking capability. A schematic diagram of the prototype is shown in Fig. 7.1

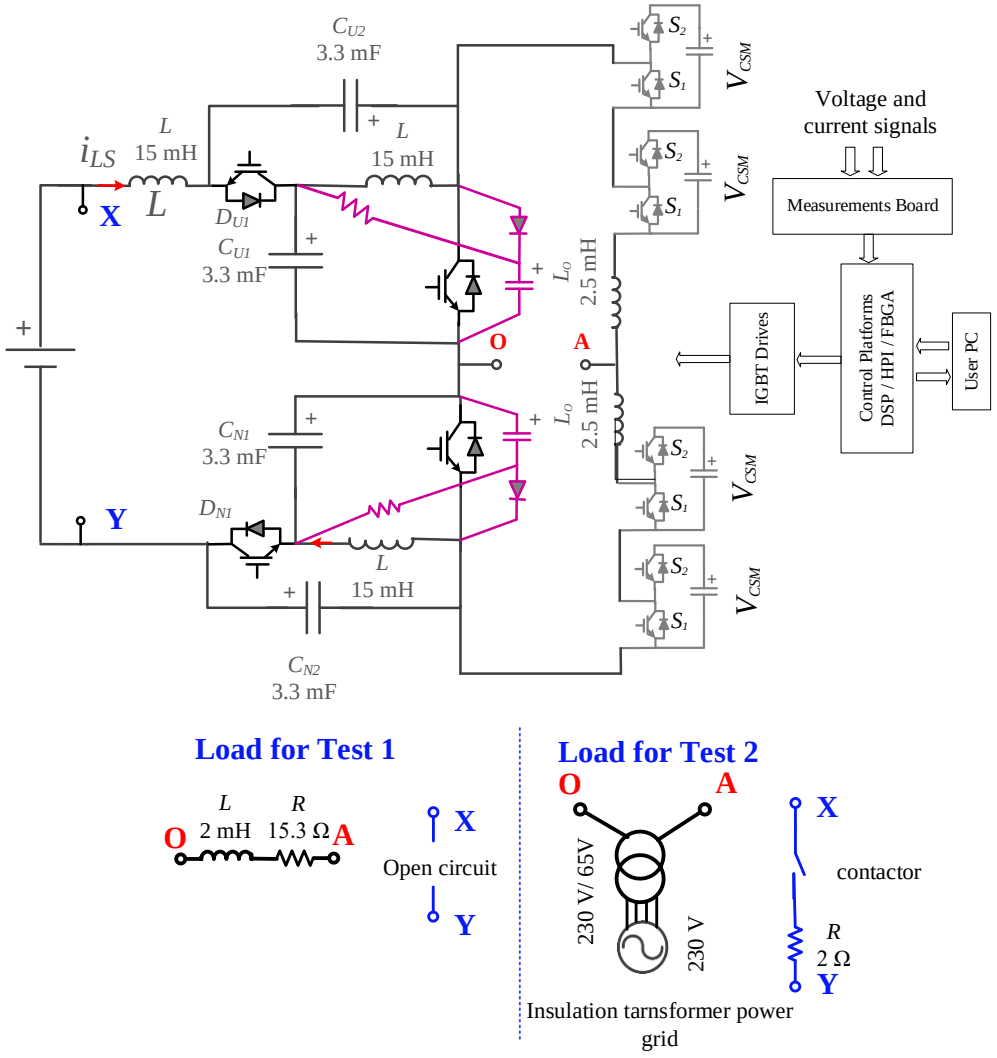


Fig. 7.1: Schematic diagram of the experimental system prototype

Firstly, the operating principles described by the mathematical analysis is verified using an RL load which is shown as “Load for Test 1” sub-circuit in Fig. 7.1. The second test is to check the capability of the proposed converter to provide DC-fault blocking. For the latter test, an AC grid is connected at the output terminals of the converter which is shown as “Load for Test 2” sub-circuit in Fig. 7.1. A photograph for the converter setup is shown in Fig. 7.2.

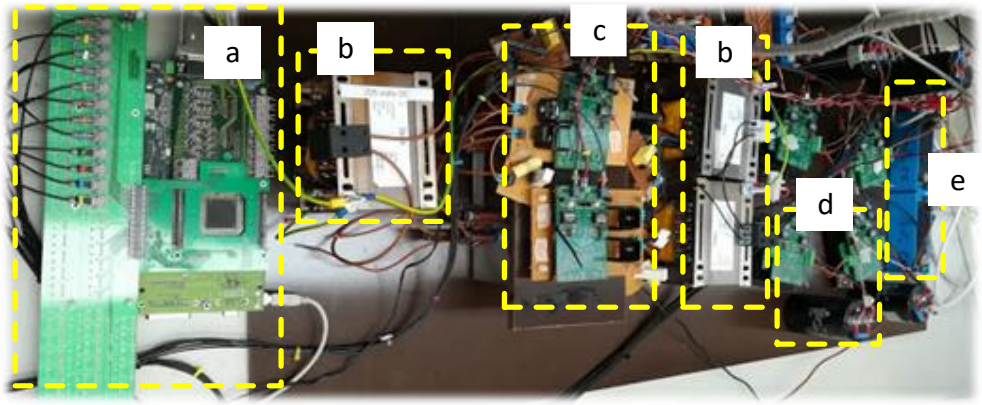


Fig. 7.2: Photograph of the experimental prototype: a) TMS320C6713 DSP and FPGA platform, b) qZS-inductors, c) qZS-capacitors and switches, d) SMs, and e) arm inductors

7.1.1 Power converter design

For 2 SMs per arm and a peak value of the output voltage of 170 V, a SM capacitor voltage of 170 V is required. The SM PCB design has been obtained from previous work within the PEMC Research Group at the University of Nottingham. An Infineon power semi-conductor module, F4-30R06W1E3 [123], was used in the design of this converter. This module is a full-bridge converter which comprises four IGBTs rated at 600 V/30 A, the rating is higher than the required level. Only one branch is used for each SM as the circuit is half-bridge converter. A photograph of the power SM is shown in Fig. 7.3.

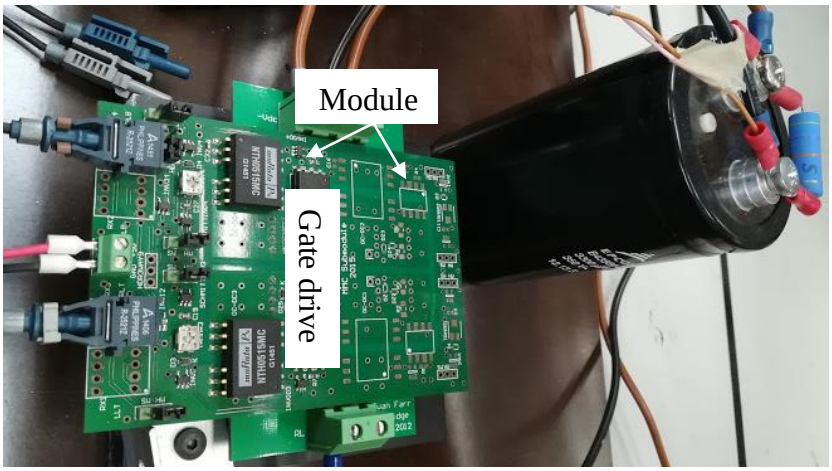


Fig. 7.3: A photograph of the power SM with the gate driver circuit

The qZS-network stage uses IKW50N60H3 (600 V /50 A) [124] switches for the series and chain-link switches, built using Veroboard. Aluminum electrolytic capacitors have been used for the SMs and qZS-network.

For each SM, a 100 nF snubber capacitor has been connected across the SM DC-terminals to reduce the overvoltage that may be generated due to effect of stray inductance. For the qZS-networks, there is a high frequency power loop through C_{U1}, C_{U2}, and D_{U1} for the upper qZS-network and through C_{N1}, C_{N2}, and D_{N1} for the lower qZS-network as shown in Fig. 7.1. The stray inductance of these loops may cause high voltage spikes over the DC-link switches during transition from ST state to NST state, which may damage the switches. The stray inductance could be reduced by shortening the connection wires. However, reducing the loop length may not be enough for reducing the voltage spikes to an acceptable level. Therefore, a snubber circuit at the terminals of the DC-link switch is still required [125]. The RCD snubber circuit, proposed in [126], has been connected at the terminals of the DC-link switch in order to reduce the DC-link voltage spikes as shown in Fig. 7.1. The snubber capacitor and resistor are selected according to [125] as 0.47 µF and 200 Ω, in order to limit the voltage spikes to be less than 10% of the peak value of the DC-link voltage.

A photograph of the power sub-module with the gate driver circuit and the heat sink is shown in Fig. 7.3. A schematic diagram of the gate driver circuit is shown in Fig. 7.4. The gate drive signal is obtained from the FPGA board via a fiber

optic cable. The signal from fiber optic cable is taken through resistor R_D, capacitor C_D and diode D_D (RCD) circuit to add a deadtime. The RCD circuit adds a delay in the rising edge of the signal related to the value of the resistor R_D. An optocoupler HCPL-3120 is used to isolate the driving signal from the 5V power supply. In addition, an isolated power supply (±15V) NTM0515MC is used to achieve the required voltage level for the IGBT. Two Zener diodes are used to prevent transient over-voltage in the IGBT gate signal. Table 7.1 summarises the system design parameters and component values.

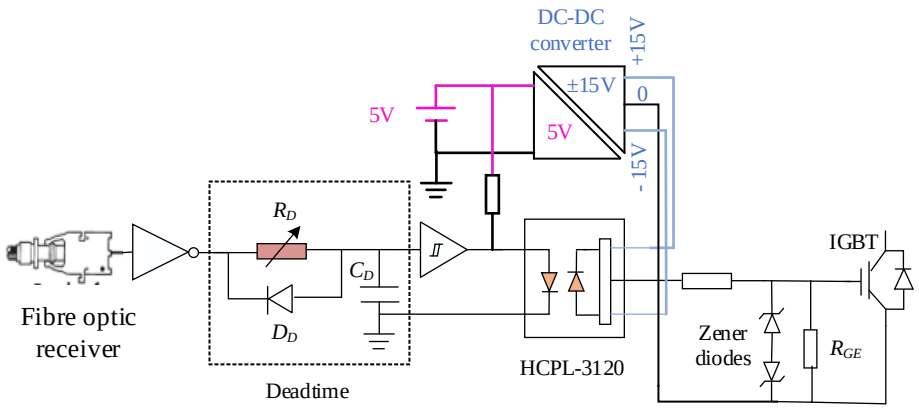


Fig. 7.4: A schematic diagram of the gate driver circuit

Table 7.1: Parameters of the experimental model

Parameter	Value
Peak output voltage (V_m)	170 V
DC source voltage (V_{DC})	340 V, 280 V 225 V
SM capacitor voltage	170 V
Number of SMs per arm (N_{SM})	2
Arm inductance (L_o)	2.5 mH
SMs capacitances (C_{SM})	3.3 mF
qZS inductances ($L_{U1} = L_{U2} = L_{N1} = L_{N2}$)	15 mH
qZS capacitances ($C_{U1} = C_{U2} = C_{N1} = C_{N2}$)	3.3 mF
Load resistance	15.3 Ω
Load inductance	2 mH
Carrier frequency (f_c)	10 kHz

The converter is tested in both buck and boost modes with different values of DC source voltage (of 340 V, 280 V and 225 V) in order to get 170 V. The SMs and qZS-network capacitances are selected according to (5.6), (5.12) and (5.18), as given in section 5.1.1. For the experimental design, 2 SMs per arm, rated power of 2 kW, V_{DC} of 340V (in order to get 170 V of peak output voltage), G = 1, cos φ = 0.98 and m = 1, 3.3 mF for the SMs and qZS-network capacitances C_{SM} and C_{U1} can be used corresponding to 5% and 15 % voltage ripple factor respectively. The discharging resistor are connected in parallel to the SM capacitors where it is value controls the discharging time of the capacitor. For 60 second time constant, the required discharging resistor is 20 kΩ.

The arm inductance value is selected according to (5.32) or (5.35). For the experimental design, V_{DC} of 225 V and G = 1.5, 2.5 mH of arm inductance is used corresponding to 40% current ripple factor when using the SS and RICs technique.

The qZS inductance values are selected according to (5.44) when using the RICs technique as shown in section 5.1.2.2. For V_{DC} = 225 V and G = 1.5, 15 mH of qZS inductance can be used, corresponding to a 200% current ripple factor.

7.1.2 Measurement board

The SM capacitor voltages and the upper and lower arm currents should be measured in order to apply the sorting algorithm and the SM capacitor balancing. Further signals for the DC voltage, source current and AC output voltage are measured for the DC-fault blocking test. A photograph of the measurement boards (voltage and current transducers) is shown in Fig. 7.5.

LA 55-P [127] and LV 25-P [128] sensors are used for the current and voltage measurements, as shown in Fig. 7.6 and Fig. 7.7. These two transducers are equipped with Hall effect closed loop current sensors and are selected due to good linearity and excellent accuracy. Both current and voltage transducers require a +15/0/-15 V voltage supply.

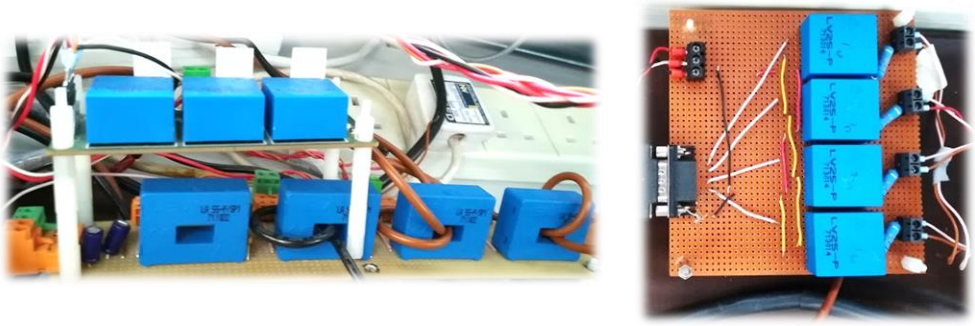


Fig. 7.5: Photograph of current and voltage transducers

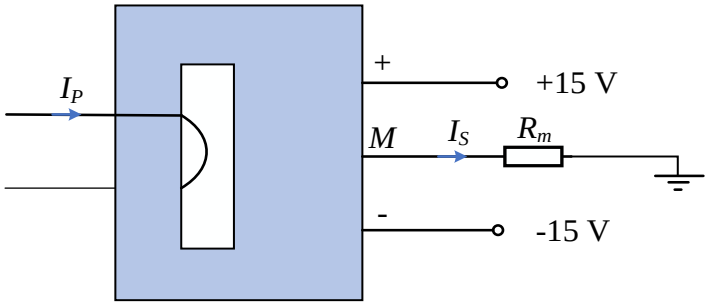


Fig. 7.6: LA 55-P current transducer circuit diagram

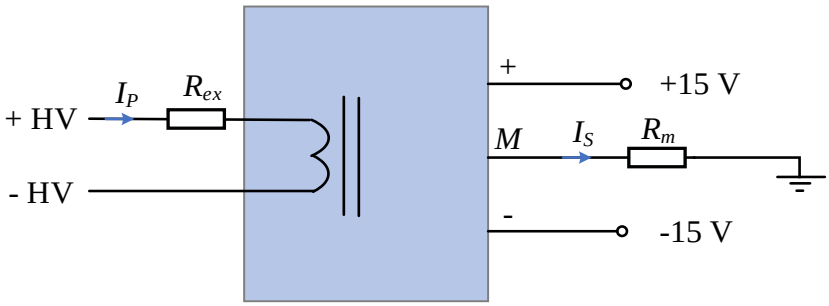


Fig. 7.7: LV 25-P voltage transducer circuit diagram

The concept of current sensor LA 55-P is shown in Fig. 7.6. The cable carrying the current to be measured is passed through the hole of the transducer making one or more turns. The nominal primary current is up to 50 A for this type, leading to a secondary current of ±50 mA (a conversion ratio of 1/1000). The FPGA burden resistor R_m limits the voltage on the board to ±5 V. For example, if the cable carries a measuring current of 20 A with two turns through the hole, which makes a total of 40 A in the primary side and then 40 mA in secondary side giving a burden resistor of 5 V/ 40 mA = 125 Ω.

The voltage transducer LV 25-P shown in Fig. 7.7 is based on the same principle as the current transducer and is recommended to measure voltages up to 500 V. The measured voltage is transferred to a current and an output signal is delivered by the voltage transducer using an external resistor R_{ex}. The external resistor R_{ex} is selected depending on the maximum measured voltage and the datasheet nominal input current. The nominal maximum current at the primary side is 10 mA. The external resistor R_{ex} can be calculated by the measured voltage / 10 mA. For example, the SMs capacitor voltage is 170 V, the external resistor R_{ex} = 170/10 mA = 17 kΩ. Therefore, 20 kΩ is selected for R_{ex}. The maximum secondary current is at 25 mA, which leads to a burden resistor of 5 V/ 25 mA = 200 Ω. Therefore, 150 Ω is selected for R_m.

The transducers need to be calibrated using dedicated sources to scale the relation between the ADC reading and the actual measured signals. The calibration procedure can be repeated at every time of the operation to compensate any deviation in the readings due to the temperature effect of the transducer and the resistors.

7.2 Control platform

The control platform consists of a Texas instruments C6713 DSK DSP board, an FPGA board, and a host port interface (HPI). A photograph of this control platform is shown in Fig. 7.8.

The DSP is clocked at a frequency of 225 MHz and uses a 32-bit wide External Memory Interface which is shared with the FPGA, as well as an HPI daughtercard. The DSP can be programmed using the Code Composer Studio (CCS) from Texas Instruments. The DSP main function is to calculate the switching signal requirements for the converter modulation.

The HPI daughtercard provides an interface to the HPI on the DSP and downloads the code to the DSP. In addition, this daughtercard allows data transfer between the host PC and the DSP. The daughtercard used is a Graphics User Interface (GUI) to interface the host PC and enables the on-line monitoring and plotting of the DSP program variables.

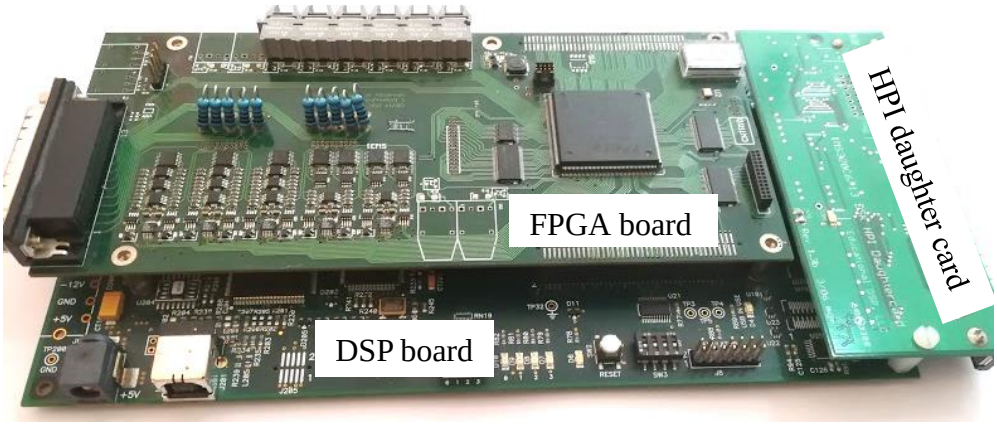


Fig. 7.8: A photograph of the control platform including the FPGA board and the HPI daughtercard mounted on the DSP board

The FPGA board has been developed by the Power Electronics, Machines and Control Group (PEMC) Research Group at the University of Nottingham, and it uses ProASIC3 chip. The FPGA card contains connectors which are used for data transmission between the FPGA and DSP, analogue digital converter (ADC) reading channels (up to ten channels), optical transmitters for PWM signals, interrupt period and trip monitoring.

In this circuit, only one FPGA board is used as the number of measurements required from the system is nine (less than the ten available ADC channels). The trip limits for the ADC channels can be used to trip the FPGA by setting the threshold value for each ADC channel. If one or more of the measured values are beyond their threshold level, the trip signal is sent to the FPGA and consequently the PWM signals will be disabled (‘0’).

The FPGA is responsible for the interrupt signal generation, which is required for the control platform operation. Once the DSP receives the interrupt signal, the modulating signals will be updated at beginning of each sample frequency period and the sequence of the switching signals will be transmitted via the optical transmitters to the gate drive circuits. The interrupt routine can be described as follows.

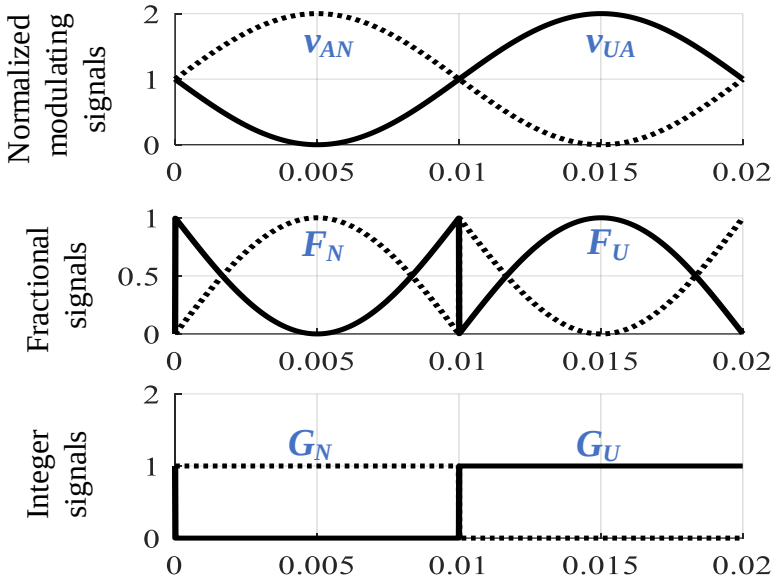
The PWM vectors for gating the SMs can be represented by a hexadecimal vector of 8 digits (0000 0000), with the 4 left digits for the data part and the 4 right digits for the time part. The time part indicates how many of the clock cycle every vector should be applied. Each digit in the data part can be represented by

4 binary bits, where each bit indicates the SM status. For instance, if the data part vector is 0001, the first hexadecimal digit which is '1' is converted to '0001' binary which means that the first SM in the upper arm should be inserted. If the data part vector is 0003, the first hexadecimal digit which is '3' is converted to '0011' binary which means that the first and the second SMs in the upper arm should be inserted. The complementary (inverse) signal can be produced which allows the SM to be bypassed.

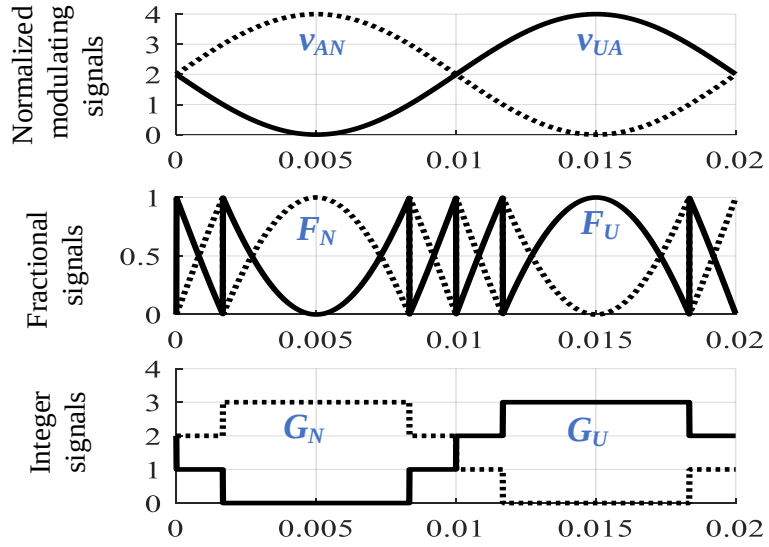
There are two options to provide the complementary signal. The gate drive circuit can receive one signal via the fiber optic cable and then uses the inverting gate to provide the complementary signal. The second option is to make the complementary signal in the FPGA and consequently the gate drive will receive two signals for the two switches of the SM. The latter option is implemented in this project in order to be able to block all the converter switches under DC-fault conditions, which cannot be achieved with the first option. Therefore, the required pulse signals are 12, where 8 are for the SM switches and 4 are for the qZS switches. As a result of having only 10 fiber optic transmitters for the FPGA board, an extension board is used which can provide up to 48 transmitters.

The reference signals v_U and v_N of the upper and the lower arms are normalized to the range from 0 to N_{SM}. The integer value of the modulation signals G_U and G_N indicates how many of the SMs are inserted in the upper and lower arm respectively, while the fractional values F_U and F_N mean the duty ratio of just one SM that achieves PWM in the upper and lower arm respectively. This means that one SM in the upper arm and one SM in the lower arms performs PWM during the switching frequency cycle with duty ratio of F_U and F_N. Fig. 7.9a and Fig. 7.9b show the normalized modulating signals, fractional and integer signals that are required to generate pulse signals for $N_{SM} = 4$ and $N_{SM} = 2$ respectively.

For more details at $N_{SM} = 2$, during an interrupt period (sampling frequency cycle), in case of an upper modulation signal v_U of 1.3, one SM is inserted in the current path while the other SM performs PWM with a duty ratio F_U of 30 % of the switching cycle. Simultaneously, the lower modulation signal v_N is 0.7, one SM performs PWM with a duty ratio F_N of 70% and the other SM is bypassed.



(a)



(b)

Fig. 7.9: Modulating signals, the fractional signals and the integer signals at a) N_{SM} = 4 and, b) N_{SM} = 2

In this case, five vectors (v_1 to v_5) can be used at each interrupt period as illustrated in Fig. 7.10. The mechanism used to generate the PWM signals is shown in Fig. 7.11. The upper and lower modulating signals are normalized within the range (0 : N_{SM}). Then, the fraction and integer values are obtained. From the sorting mechanism, the index of the SM that should be inserted or

bypassed is determined. Consequently, the PWM vectors can be generated according to the fraction and integer values.

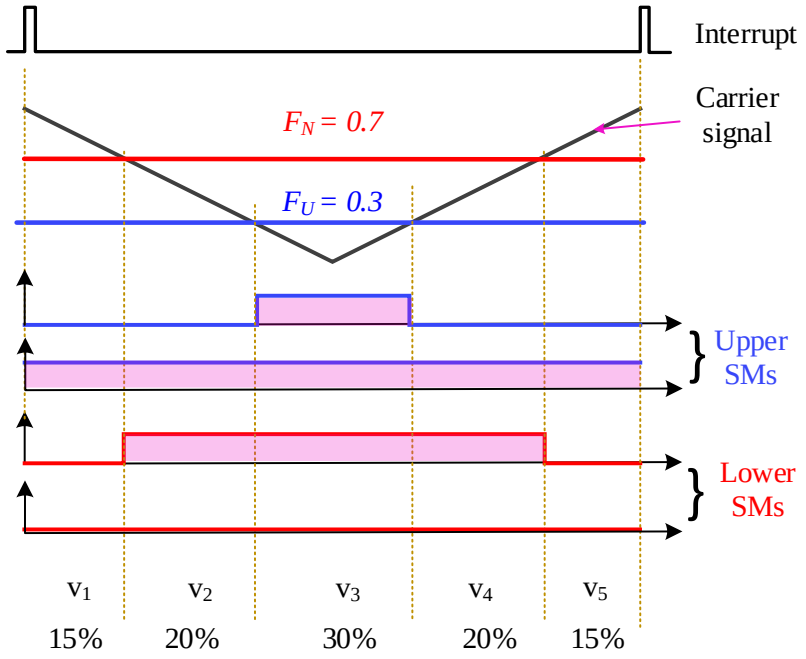


Fig. 7.10: PWM vector generation at N_{SM} = 2, in case of v_U = 1.3 (F_U = 0.3) and v_N = 0.7 (F_N = 0.7)

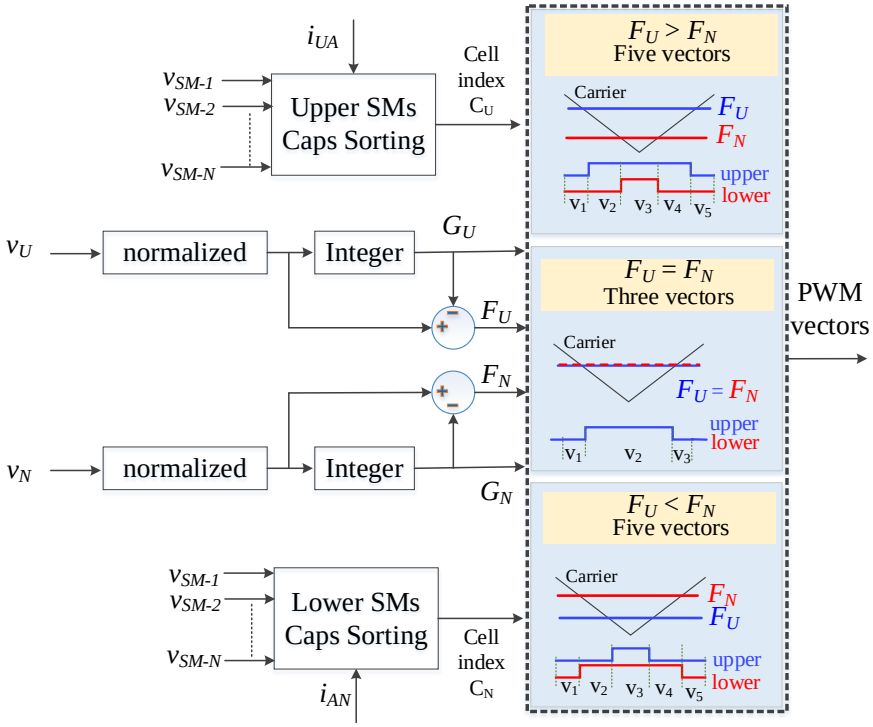


Fig. 7.11: The PWM signals generation mechanism for SMs

This mechanism is suitable for the qZS-MMC when using the SS technique, while more vectors have to be identified when using the RICs technique. In addition to the F_U and F_N signals, the shoot-through modulating signal needs to be considered. During the ST interval, the number of inserted SMs in the corresponding arm needs to be reduced by $N_{SM}/2$. Referring to section 4.4.2 and Fig. 4.11, the upper (lower) qZS-network can perform ST mode if the amplitude of the upper (lower) arm modulating signal is higher than $N_{SM}/2$.

Consider the upper and the lower modulation signals v_U and v_N are 1.3 and 0.7 respectively. Therefore, one of the upper SMs and one of the lower SMs perform PWM with duty ratios F_U of 30% and F_N of 70% respectively. In addition, in order to get average D_{sh} of 0.2, the upper ST modulating signal $v_{sh\text{-}U}$ has a height of 0.4 as discussed in section 4.3.2. The number of inserted SMs in the upper arm needs to be reduced by '1' (= $N_{SM}/2$) during the ST interval. Using the two fraction signals (F_U and F_N) and the ST signal, seven vectors should be applied during an interrupt period. Fig. 7.12 shows the PWM vector generation in case of $F_N > v_{sh\text{-}U} > F_U$, while Fig. 7.13 shows the PWM vector generation in case of $F_N > F_U > v_{sh\text{-}U}$. The remaining switching vectors can then be generated.

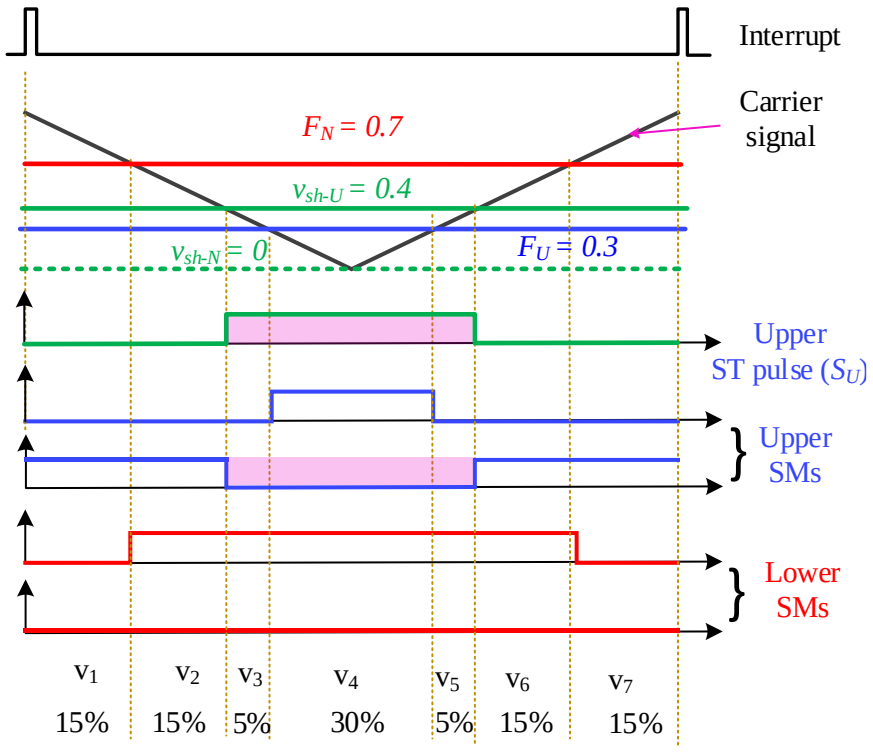


Fig. 7.12: PWM vector generation in case of $F_N > v_{sh\text{-}U} > F_U$ when using RICs technique

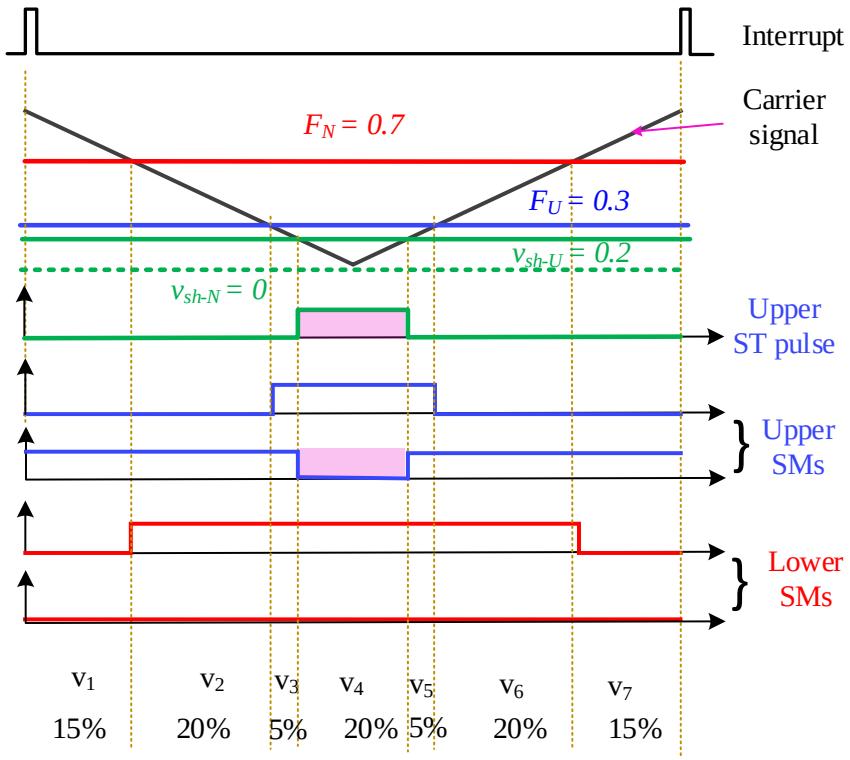


Fig. 7.13: PWM vector generation in case of $F_N > F_U > v_{sh\text{-}U}$ when using RICs technique

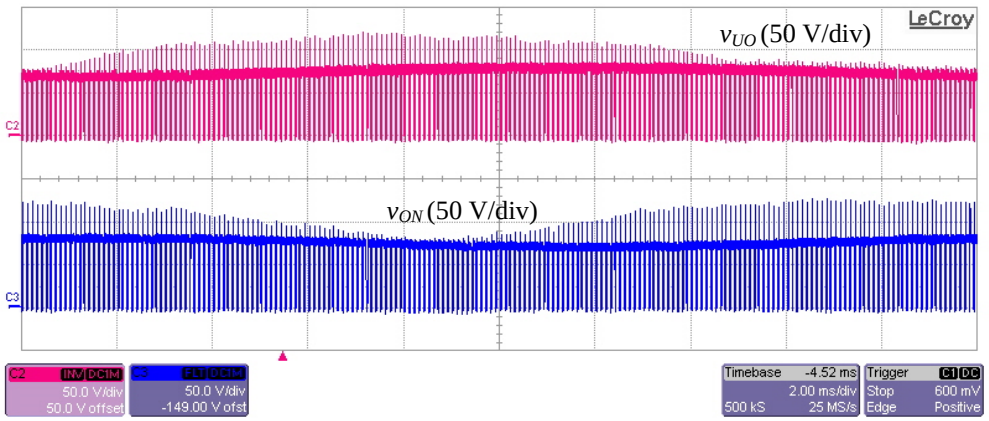
7.3 Experimental Evaluation

To experimentally verify the theoretical analysis and confirm the simulation studies given in this thesis, a low voltage and power rated scaled down prototype of a 5-level quasi Z-source modular multilevel converter (qZS-MMC) described in section 7.1 and section 7.2 is implemented to obtain the experimental results.

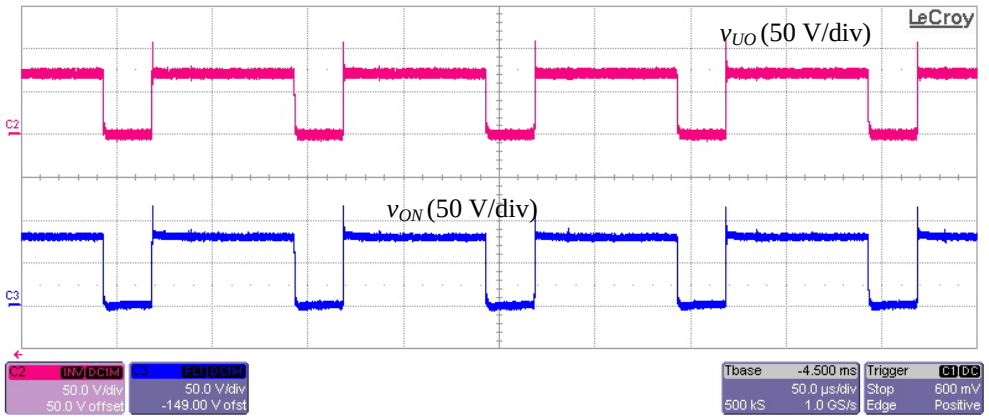
For data recording purposes, some of the experimental waveforms are captured by using a 200-MHz LeCroy oscilloscope using a combination of differential voltage probs and current probs. The other experimental results presented in this chapter are recorded by using MATLAB through the HPI graphical interface. The waveforms taken through the HPI are sampled at 10 kHz, which is the DSP switching and sampling frequency. Therefore, this part of results, obtained by HPI, is free from the switching ripple.

7.4 Snubber circuit effect

To illustrate the effectiveness of the snubber circuit on reducing voltage spikes, the DC-link voltages v_{UO} and v_{ON} have been compared with and without using the snubber circuit. The results in this case have been taken when operating with a small DC source voltage in order to avoid generating large voltage spikes, which may destroy the chain-link switches. The DC source voltage V_{DC} is set to 80 V, ST duty ratio D_{sh} is 0.25 and consequently the gain G will be 1.5 when using the SS technique. The upper and lower DC-link voltages and their zoomed view are shown in Fig. 7.14 without connecting the snubber circuit. It is noted that the voltage spikes are high and are approximately equal to 50% of the peak value of the DC-link voltage for this test case.



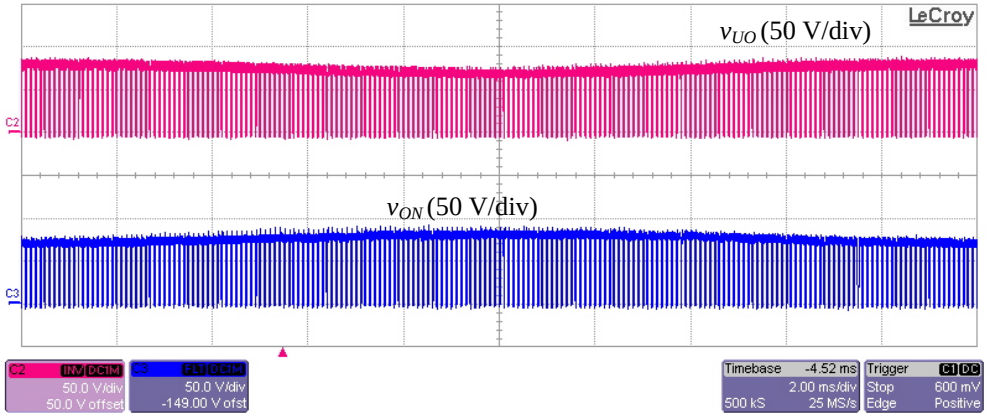
(a)



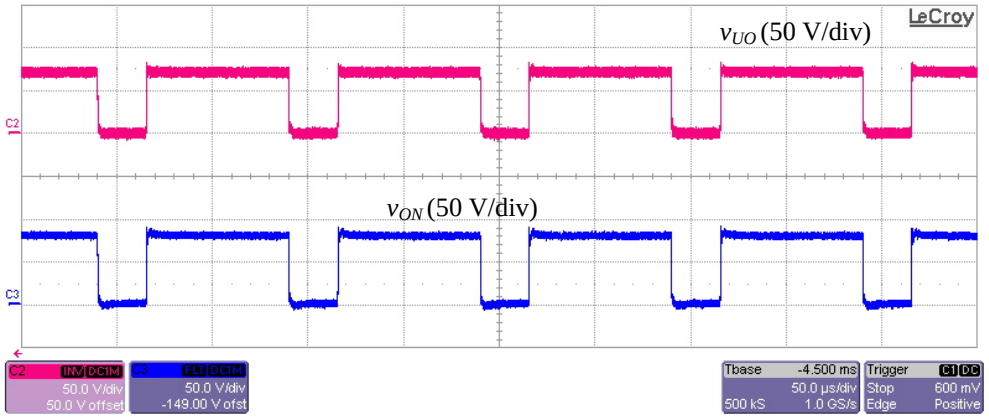
(b)

Fig. 7.14: Experimental results showing a) the upper (top) and the lower (bottom) DC-link voltages v_{UO} and v_{ON} without having the snubber circuit connected at V_{DC} = 80 V, D_{sh} = 0.25 and G = 1.5, b) their zooming.

Using the snubber circuit at the terminals of the chain-link switches reduces the voltage spikes to less than 10% of the peak value of the DC-link voltage as illustrated in Fig. 7.15.



a)



(b)

Fig. 7.15: Experimental results showing a) the upper (top) and the lower (bottom) DC-link voltages v_{UO} and v_{ON} when using the snubber circuit at V_{DC} = 80 V, D_{sh} = 0.25 and G = 1.5, b) their zooming.

7.5 Verifying the operation constraint

To validate the importance of using the antiparallel switches and verify experimentally the theoretical and simulation studies, experiments have been conducted in both buck and boost modes with and without using the antiparallel IGBTs. The protype has been constructed using IGBTs connected in antiparallel to the diodes. Therefore, the case of using series diodes only is achieved by turning off the IGBT gate drive signals.

This test demonstrates the necessity of using the antiparallel active switches in the qZS-networks (T_{U1} and T_{N1}) to preserve performance, as explained in section 4.4. According to the relation given in (4.39), if the D_{sh} is less than 0.25 (at cos φ = 1 and m = 1), the series diodes will become reverse biased during NST mode causing a significant drop in the DC-link voltages v_{UO} and v_{ON}. Therefore, the antiparallel active switches T_{U1} and T_{N1} are required.

7.5.1 Buck mode

The qZS-MMC is first operated in buck mode by setting ST duty ratio to D_{sh} = 0 and modulation index to m = 0.98. The DC source voltage used is set to V_{DC} = 340 V in order to get 167 V of peak fundamental of output voltage according to (4.14) for SS technique (Note: 170 V peak is theoretically obtained at m = 1).

Fig. 7.16 shows the upper arm current i_{UA} , the sum of upper qZS-inductor currents $i_{LU1} + i_{LU2}$ and the upper DC-link voltage v_{UO} when using series diode only and their zooming view. It is clear that when the upper arm current waveform i_{UA} exceeds the sum of $i_{LU1} + i_{LU2}$, a negative current will be expected to flow through the series diode D_{U1} which is not possible and leading to the blocking of the series diode and a drop in the corresponding DC-link voltage waveform (circuit connection is shown in Fig. 4.13). Therefore, the arm current i_{UA} equal to $i_{LU1}+i_{LU2}$. In addition, the average value of the DC-link voltage equals to 220V, which is higher than the expected value which is 170V (half of the DC source voltage V_{DC}/2). In contrast, Fig. 7.17 shows that the arm current can be higher than $i_{LU1} + i_{LU2}$ without resulting in a drop in the DC-link voltage as a result of using the active switches T_{U1} and T_{N1} in antiparallel with the series diodes to provide a controlled reverse conduction path. Also, the average value of the DC-link voltage is at its expected value.

Fig. 7.18 and Fig. 7.19 show the output voltage and current and their harmonic spectrum when using the series diode only and Fig. 7.20 and Fig. 7.21 show the results when using the IGBT in antiparallel to the series diode. Although in both cases the converter achieves on the output the same peak fundamental voltage and current, when using only the series diodes resulted in a significantly higher level of low order harmonics 3rd, 5th and 7th (with a percentage (relative to

fundamental component value) of 6%, 3.3% and 2% respectively) and switching frequency harmonics. This distortion is also revealed by the differences in the total harmonic distortion (THD) values for the output voltage and current that are 18.5% and 8.9% respectively when using the series diodes only compared to 12.7% and 3.5% respectively when using the IGBT in antiparallel to the series diode.

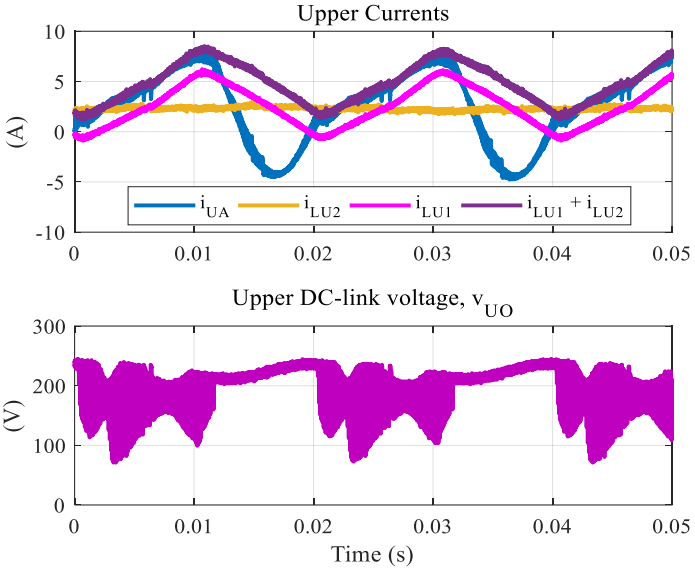
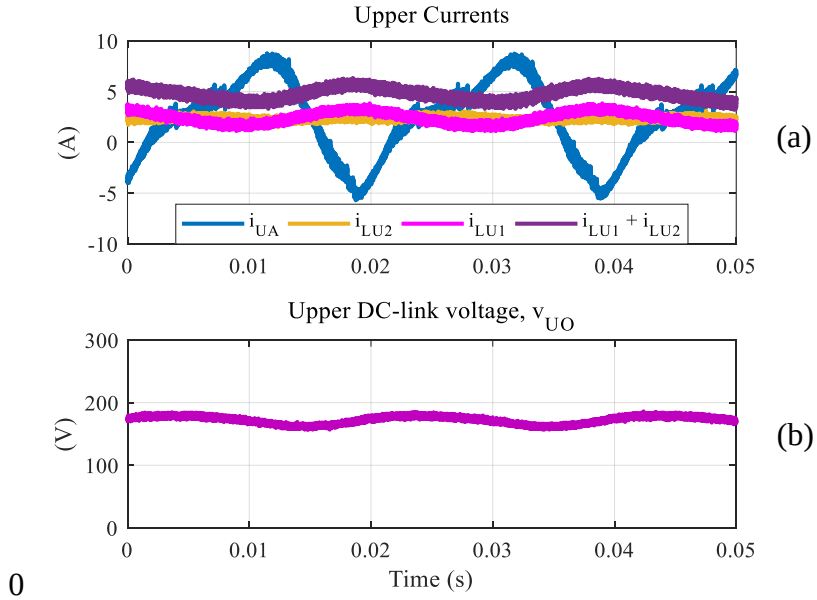


Fig. 7.16: Experimental results when using only series diode at D_{sh}=0, m = 0.98, and V_{DC} = 340 V: a) upper arm current i_{UA}, the qZS inductor currents i_{LU1}, i_{LU2} and i_{LU1}+i_{LU2}, and b) upper DC-link voltage v_{UO}



0

Fig. 7.17: Experimental results when using IGBT antiparallel to the series diode at D_{sh} = 0, m = 0.98, and V_{DC} = 340 V: a) the upper arm current i_{UA}, the qZS inductor currents i_{LU1}, i_{LU2} and i_{LU1}+i_{LU2}, and b) the upper DC-link voltage v_{UO}

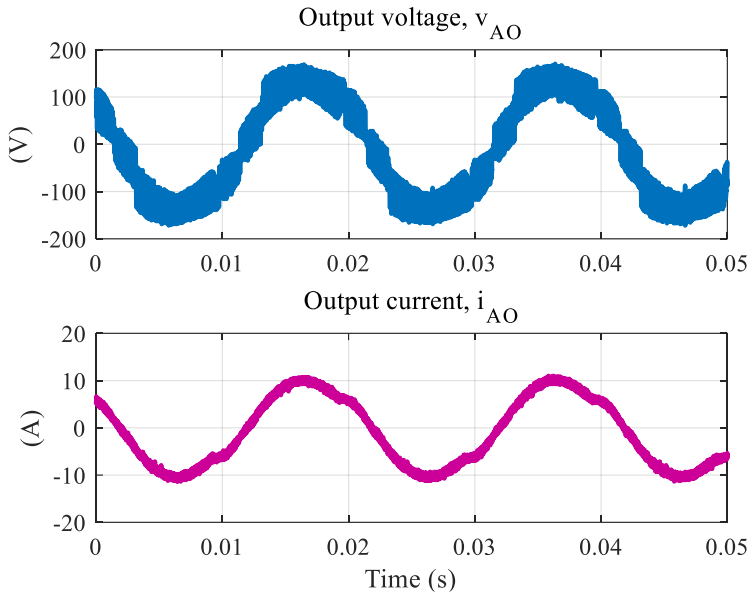


Fig. 7.18: Output voltage and current when using only the series diode at D_{sh} = 0, m = 0.98, and V_{DC} = 340 V

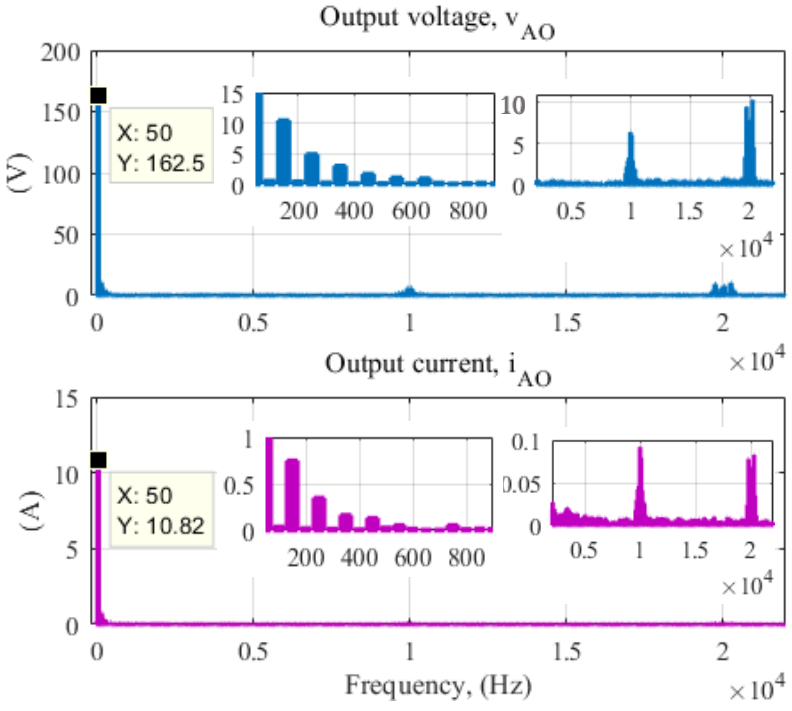


Fig. 7.19: Harmonic spectrum of the output voltage and current when using only the series diode at D_{sh} = 0, m = 0.98, and V_{DC} = 340 V

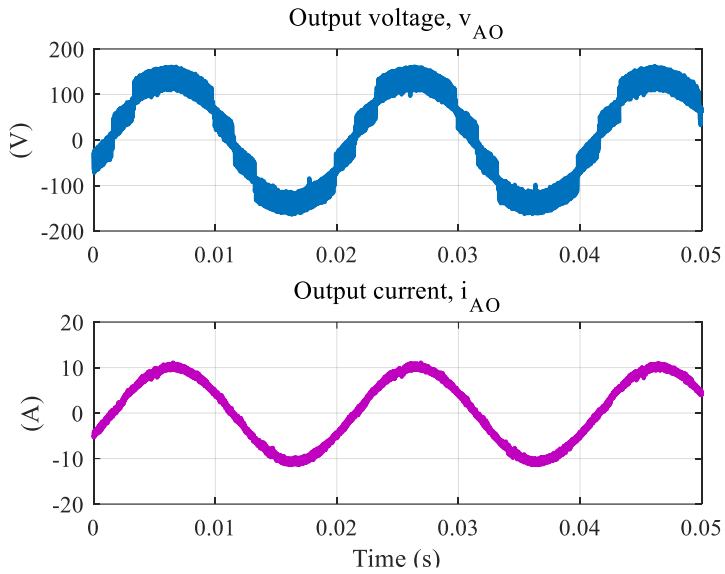


Fig. 7.20: Output voltage and current when using IGBT in antiparallel to the series diodes at D_{sh} = 0, m = 0.98, and V_{DC} = 340 V

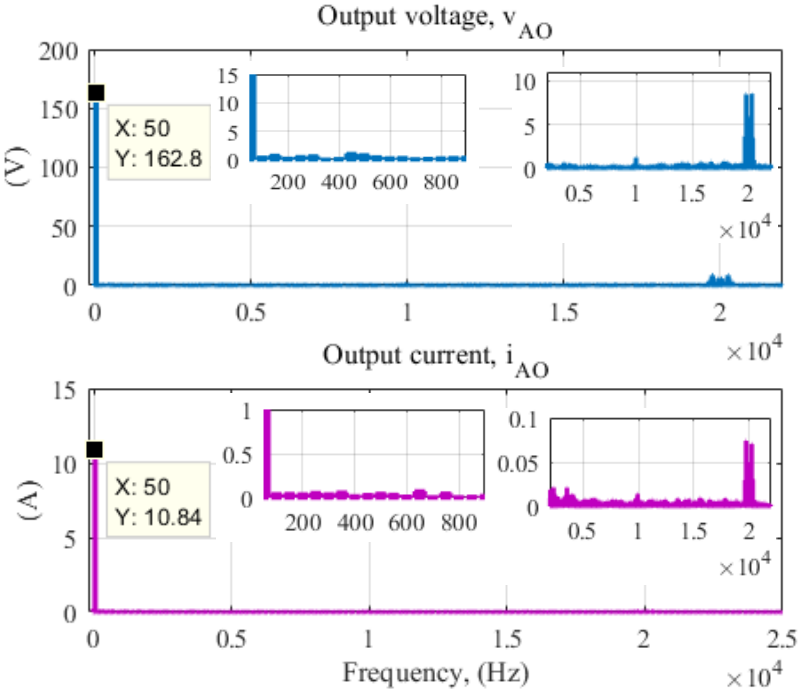
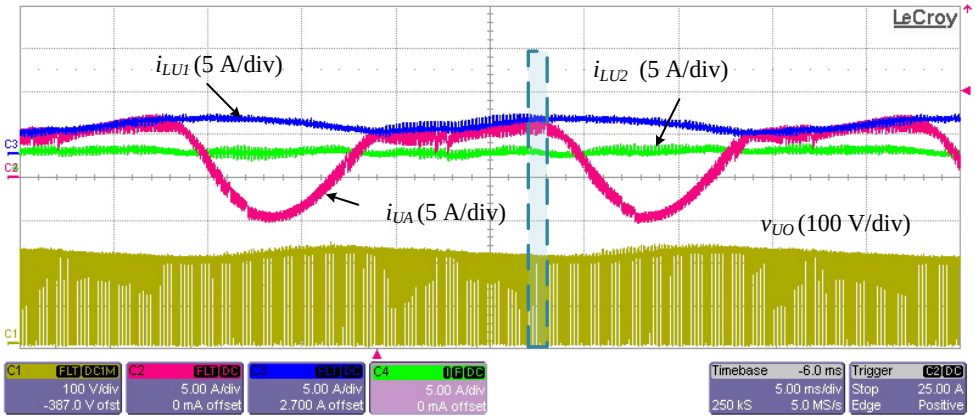


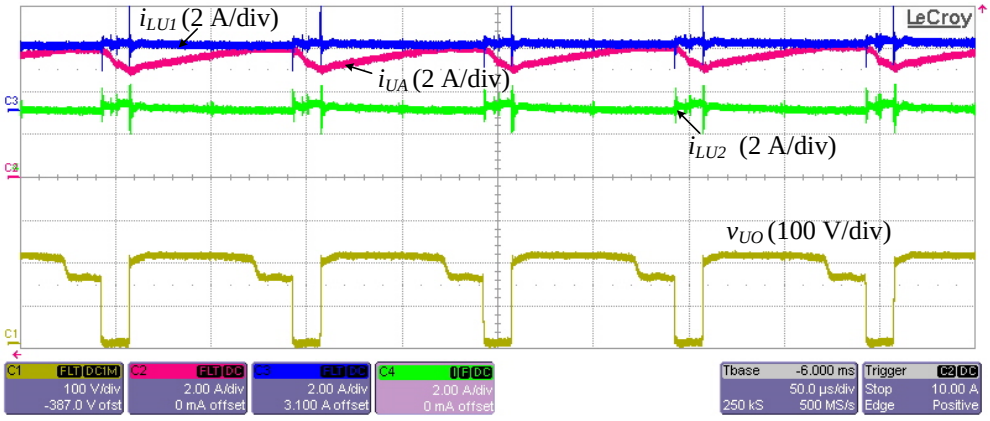
Fig. 7.21: Harmonic spectrum of the output voltage and current when using IGBT in antiparallel to the series diodes at D_{sh} =0, m=0.98, and V_{DC}=340 V

7.5.2 Boost mode

The test is repeated in boost mode at D_{sh} = 0.15, G = 1.2 and m = 0.98, where it is shown that the IGBT in antiparallel to the series diode is still required to avoid the undesired limitations in performance. To achieve the same peak fundamental of the output voltage of 167 V, the DC source voltage V_{DC} was set to 280 V. The upper arm current i_{UA} , the upper qZS-inductor currents i_{LU1}, i_{LU2} and the upper DC-link voltage v_{UO} and their zooming view when using the series diode only are shown in Fig. 7.22.



(a)

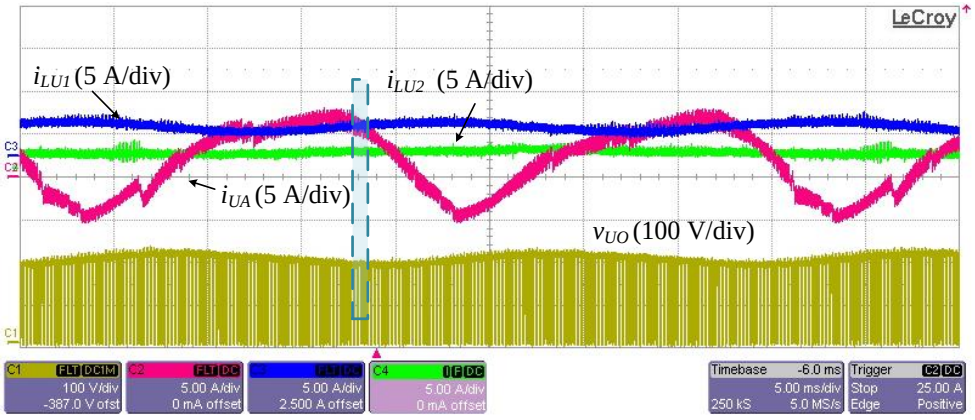


(b)

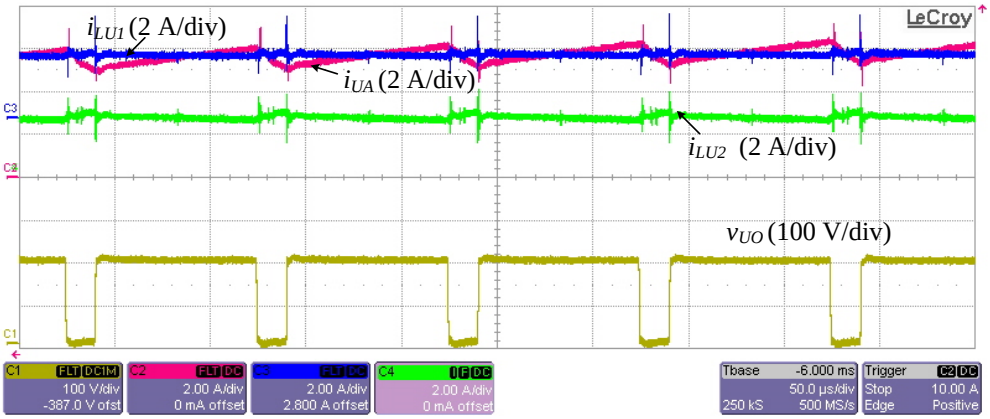
Fig. 7.22: Experimental results at D_{sh} = 0.15, m = 0.98 and V_{DC} = 280 V when using only series diodes: a) inductor currents i_{LU1}, i_{LU2}, upper arm current i_{UA} and upper DC-link voltage v_{UO}, and b) their zooming

To prove that equation (4.37) is satisfied, the summation of the two inductors currents ($i_{LU1} + i_{LU2}$) should be compared to the arm current i_{UA}. Fig. 7.22 shows that the zero crossing points of channel Ch4 (i_{LU2}) and channel Ch2 (i_{UA}) are the same and that the zero crossing of Ch3 (i_{LU1}) is set at the average value of the Ch4 (in order to obtain $i_{LU1} + i_{LU2}$). It is therefore clear that when the waveforms of the arm current exceed the sum of $i_{LU1} + i_{LU2}$, the series diode will be blocked leading to a drop in the DC-link voltage as highlighted in Fig. 7.22.

Fig. 7.23 shows that when using IGBT in antiparallel to the series diode, the arm current can be higher than ($i_{LU1} + i_{LU2}$) without a drop of the DC-link voltage.



(a)



(b)

Fig. 7.23: Experimental results at $D_{sh} = 0.15$, $m = 0.98$ and $V_{DC} = 280$ V when using IGBT in antiparallel to the series diode: a) inductor currents i_{LU1}, i_{LU2}, upper arm current i_{UA} and upper DC-link voltage v_{UO}, and b) their zooming

Fig. 7.24 and Fig. 7.25 show the output voltage and current and their harmonic spectrum when using the series diode only and Fig. 7.26 and Fig. 7.27 show the output when using the IGBT in antiparallel to the series diode. In both cases, the peak value of the fundamental output voltage as revealed by the FFT is 162 V. The difference between the expected peak value of the fundamental output voltage (167 V) and the actual measured one (162 V) is caused by voltage drops across the qZS inductors and the power semiconductor devices.

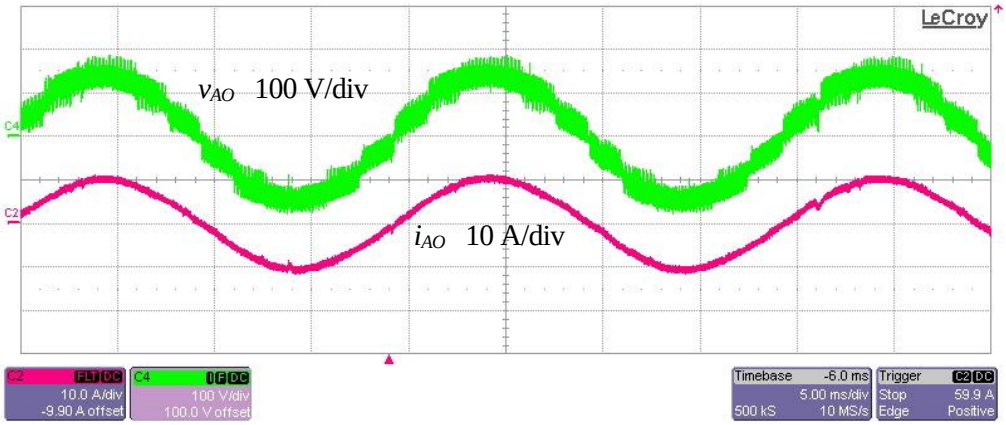


Fig. 7.24: Output voltage and current when using series diode at D_{sh} = 0.15, m = 0.98, and V_{DC} = 280 V

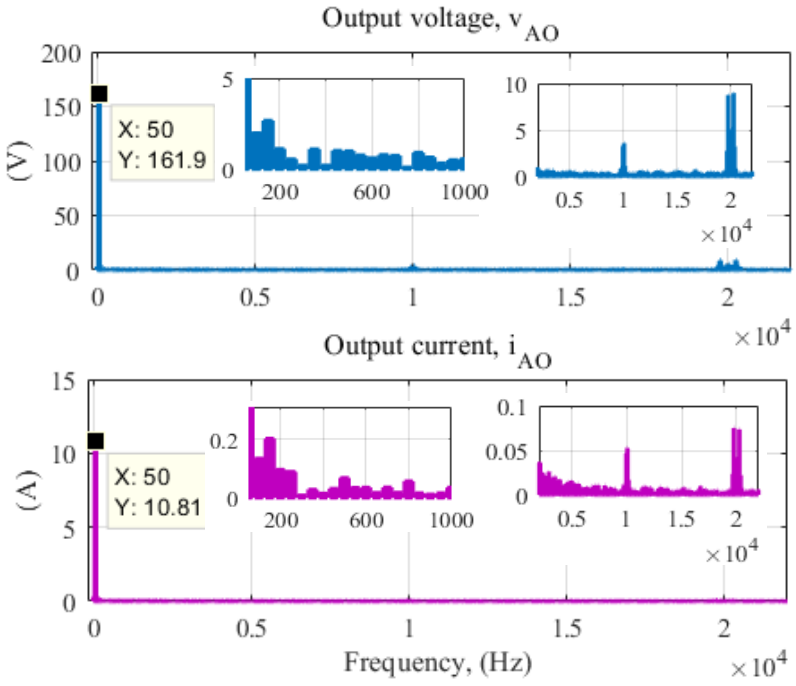


Fig. 7.25: Harmonic spectrum of the output voltage and current when using series diode at D_{sh} = 0.15, m = 0.98, and V_{DC} = 280 V

Using the series diode only resulted in a significantly higher level of low order harmonics and also switching frequency harmonics. The THD values for the output voltage and current are 14.1% and 4.9% respectively when using the series diode only compared to 13.2% and 3.8% respectively when using the IGBT.

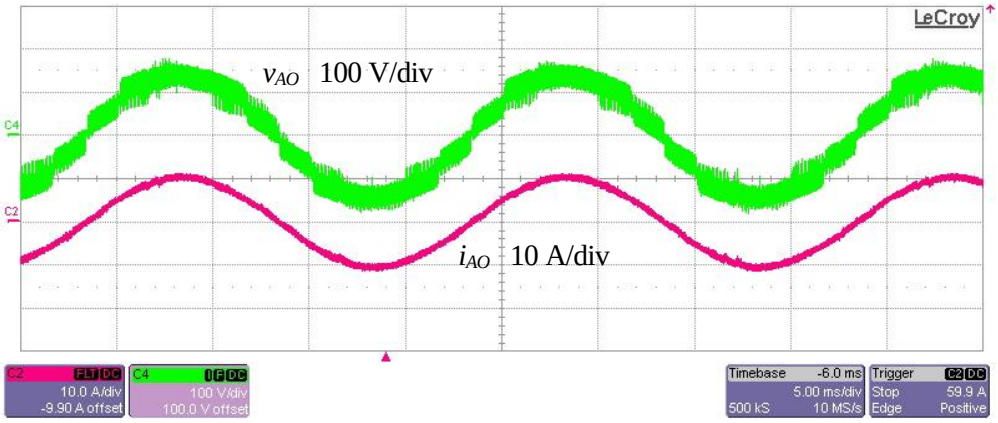


Fig. 7.26: Output voltage and current when using IGBT in antiparallel to the series diode at D_{sh} = 0.15, m = 0.98, and V_{DC} = 280 V

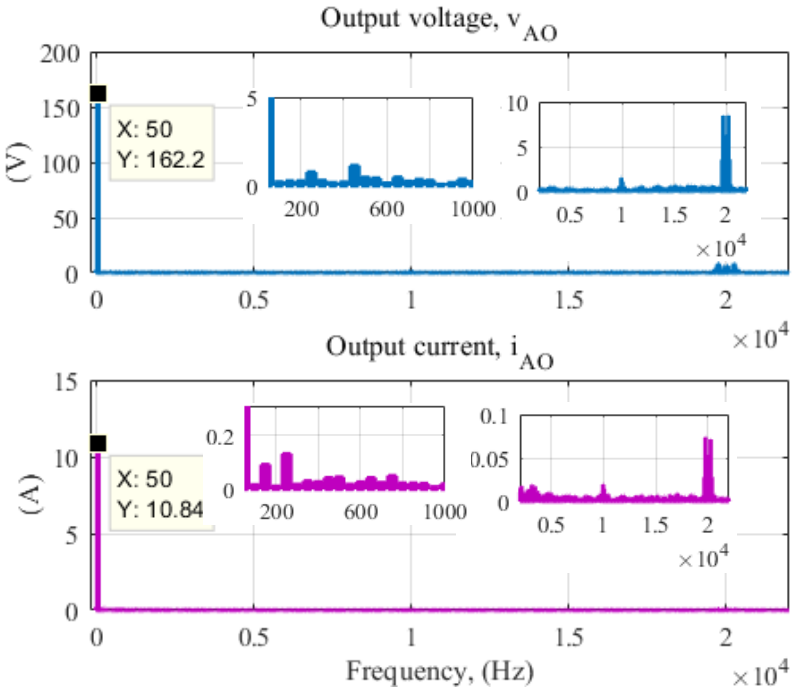


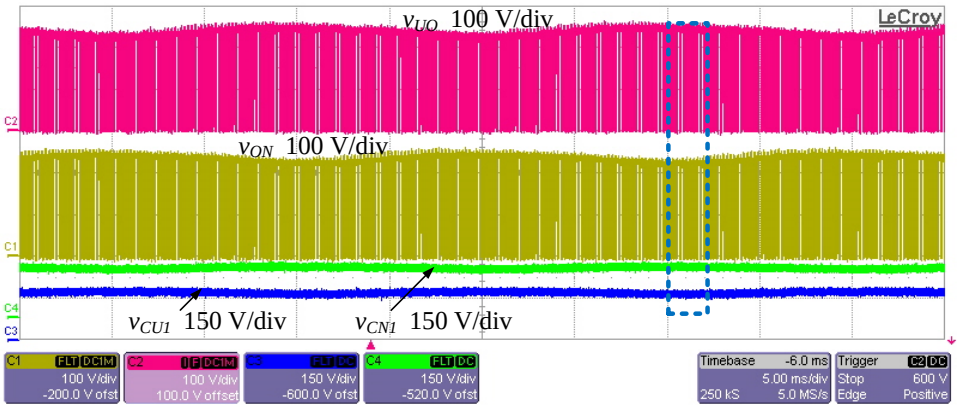
Fig. 7.27: Harmonic spectrum of the output voltage and current when using IGBT in antiparallel to the series diode at D_{sh} = 0.15, m = 0.98, V_{DC} = 280 V

7.6 Verifying the proposed modulation techniques

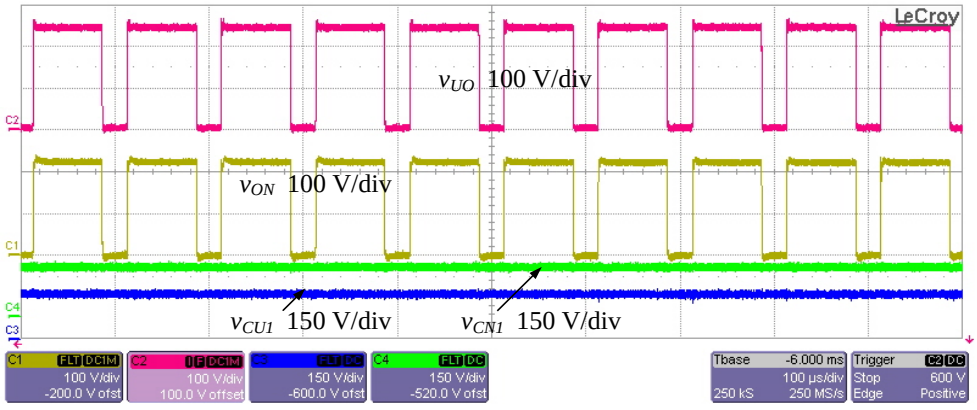
Performance of the two proposed modulation techniques (SS and RICs) has been compared in this section. The DC source voltage was set to 225 V with converter modulation index of 0.98 and a ST duty ratio of 0.25 and 0.17 was used with the SS and RICs respectively to obtain the same voltage gain value of G = 1.5 that lead to the same expected peak of the fundamental output voltage of 167 V.

7.6.1 Comparison of DC-link and qZS-capacitor voltages

The upper and the lower DC-link voltages (v_{UO} and v_{ON}), and qZS-capacitor voltages (v_{CU1} and v_{CU2}) are shown in Fig. 7.28 and Fig. 7.29 for the SS and RICs respectively.

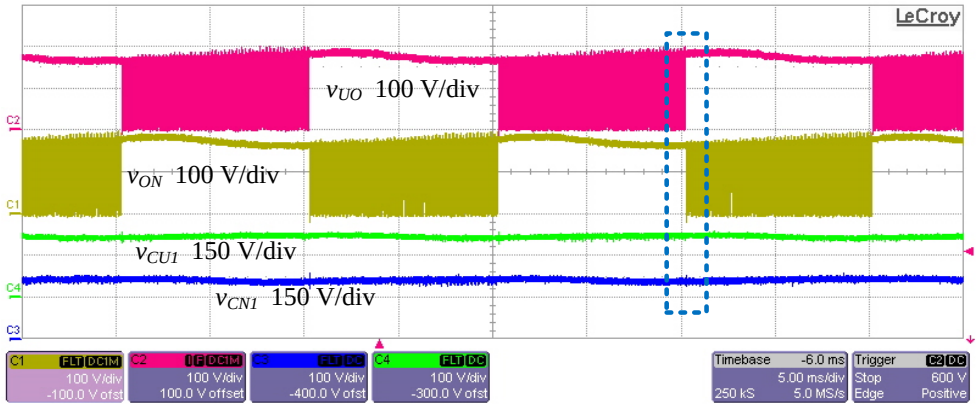


(a)

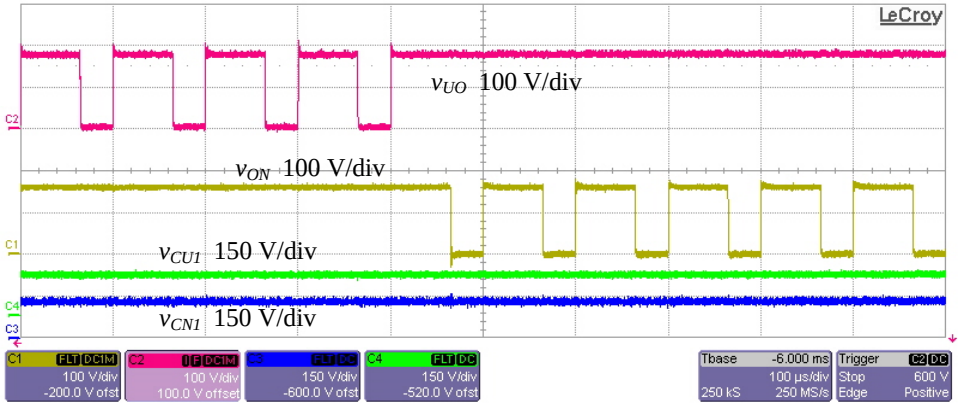


(b)

Fig. 7.28: Experimental results for SS technique: a) the upper and the lower DC-link voltages v_{UO} and v_{ON}, and qZS-capacitor voltages v_{CU1} and v_{CN1} and, b) their zooming at m = 0.98, and V_{DC} = 225 V, D_{sh} = 0.25.



(a)



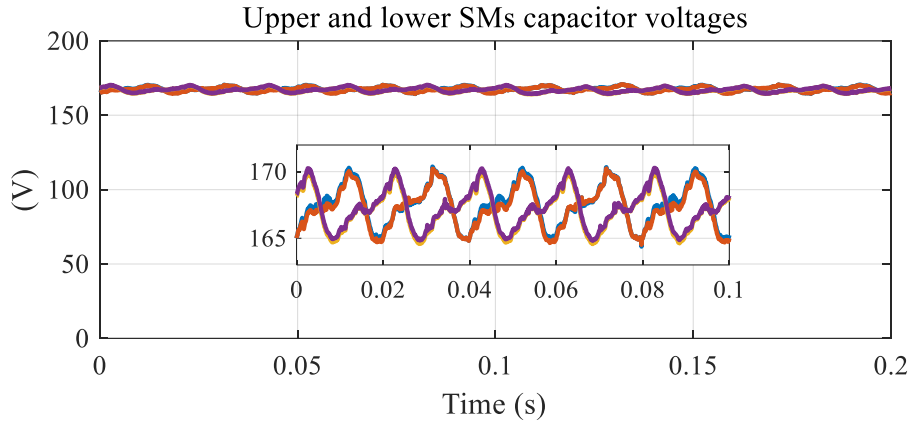
(b)

Fig. 7.29: Experimental results for RICs technique: a) the upper and the lower DC-link voltages v_{UO} and v_{ON}, and qZS-capacitor voltages v_{CU1} and v_{CN1} and, b) their zooming at m = 0.98, V_{DC} = 225 V, and D_{sh} = 0.17.

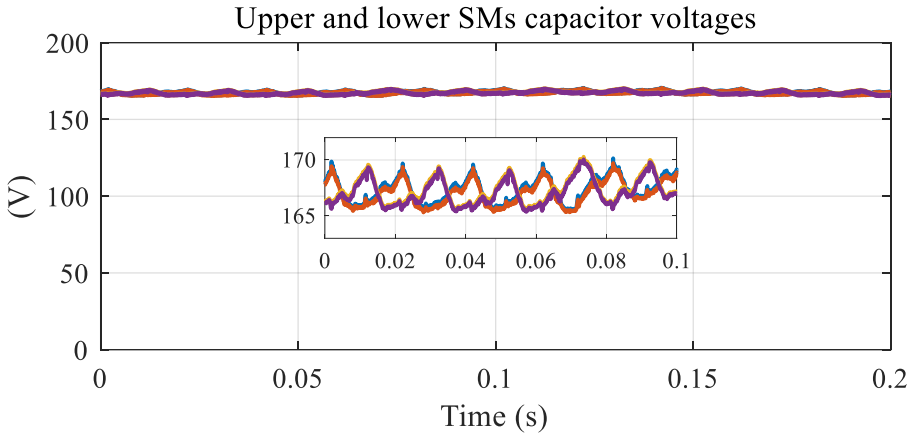
The peak values experienced in the DC-link voltages (v_{UO} and v_{ON}) for the SS and RICs techniques are 225 V and 169 V respectively, and the qZS-capacitor average voltages of 169 V and 140 V respectively. Therefore, it is demonstrated that the stress voltage on the chain-link switches and the qZS-capacitor voltage are high for the SS technique compared to the RICs technique.

7.6.2 Comparison of the SMs capacitor voltages

Due to the high number of measurements needed, the upper and lower arm SMs capacitor voltages have been captured from the DSP memory by using MATLAB through the HPI and are shown in Fig. 7.30a and Fig. 7.30b for the SS and RICs techniques respectively. It is noted that both techniques have the same average SM capacitor voltage which is 167.5 V despite different DC-link peak voltages.



(a)



(b)

Fig. 7.30: Experimental results of the upper and lower arm SMs capacitor voltages captured by MATLAB via the HPI at m = 0.98, and V_{DC} = 225 V for, a) SS technique at D_{sh} = 0.25 and, b) RICs technique at D_{sh} = 0.17

It should be noted that the SMs capacitors are charging according to the average value of the DC-link voltage when using the SS technique, while they are charging according to the peak value of the DC-link voltage when using the RICs technique. The peak to peak SM capacitor voltage ripple in case of the RICs technique is 80% of that for the SS technique (SM capacitor remains the same) which agrees with the design prediction described in section 5.1.1.1 for a gain value of 1.5.

7.6.3 Comparison of the qZS-inductor currents

The upper and lower qZS-inductor currents are shown in Fig. 7.31 for the SS technique and in Fig. 7.32 for the RICs technique.

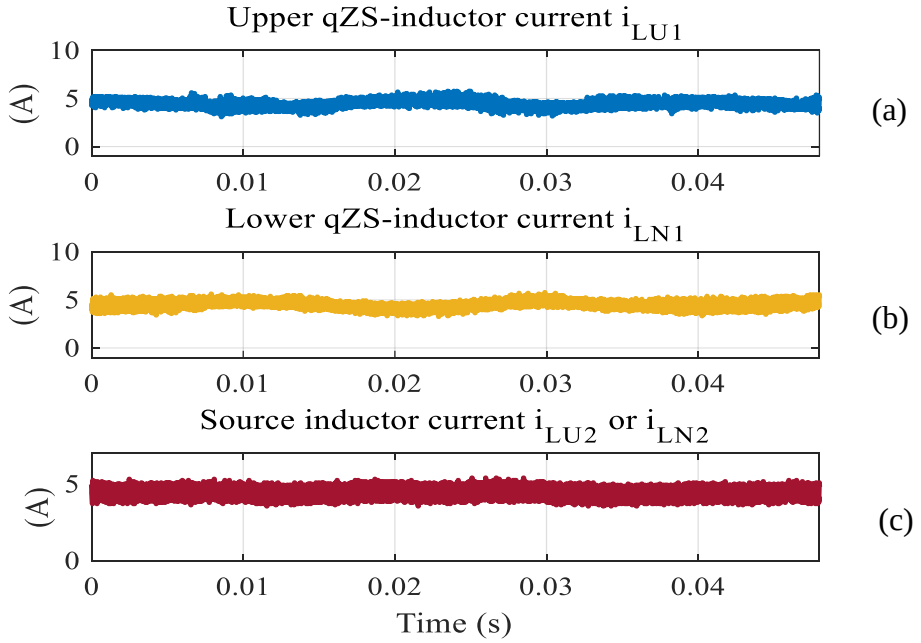


Fig. 7.31: Experimental results for SS technique: a) qZS-inductor currents i_{LU1}, and b) i_{LN1} and c) the source current i_{LU2} (or i_{LN2}) at m = 0.98, V_{DC} = 225 V, and D_{sh} = 0.25

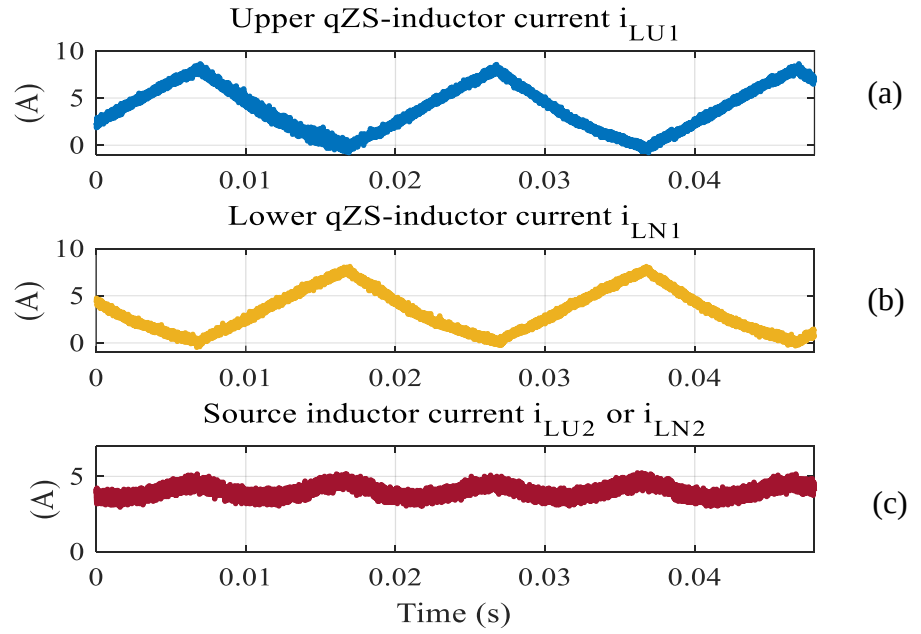


Fig. 7.32: Experimental results for RICs technique: a) qZS-inductor currents i_{LU1}, and b) i_{LN1} and c) the source current i_{LU2} (or i_{LN2}) at m = 0.98, V_{DC} = 225 V, and D_{sh} = 0.17

It is noted that the inductor currents i_{LU1} and i_{LN1} have a high ripple at the fundamental frequency in case of using the RICs technique where their peak equals twice of the average value, whereas these currents are approximately free from the low order fundamental frequency ripple when using the SS technique.

The source current (i_{LU2} or i_{LN2}) has switching frequency ripples where the peak to peak ripple in case of using the RICs is found to be half of that in case of using the SS technique as shown in Fig. 7.31 and Fig. 7.32. These results agree with the design prediction described in section 5.1.2.2.

7.6.4 Comparison of the harmonic spectrum

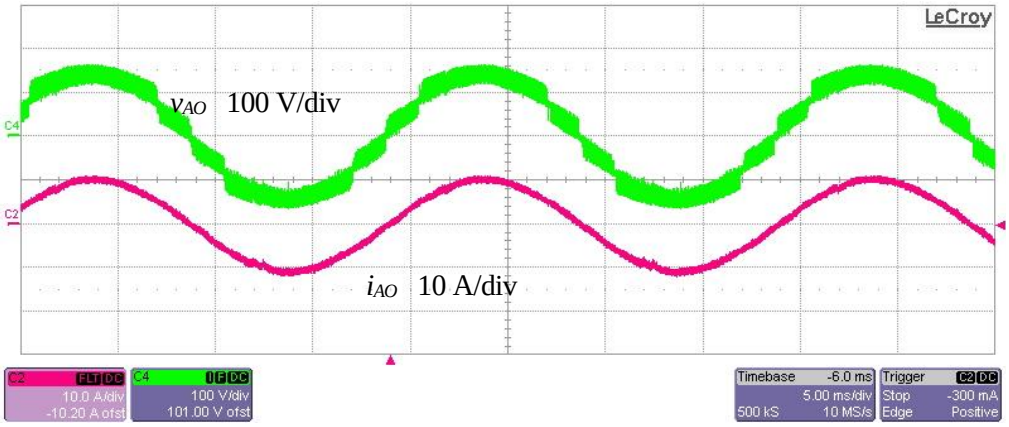
The output voltage and current and their harmonic spectrum for the SS and RICs techniques are shown in Fig. 7.33 and Fig. 7.34 respectively. The peak value of the fundamental output voltage as revealed by the FFT is 159.4 V and 161.4 V for the SS and RICs techniques respectively. The difference between the expected peak value of the fundamental output voltage (167 V) and the actual measured one (159.4 V for SS technique and 161.4 V for the RICs technique) is caused by voltage drops across the circuit components.

The qZS-MMC output voltage produces a slightly higher value of low order harmonics when using RICs technique compared with SS technique, while the switching frequency components are the same for both techniques. The THD values for the output voltage and current are 12.7% and 3.9% respectively when using the SS technique compared to 12.8% and 4% respectively when using the RICs technique.

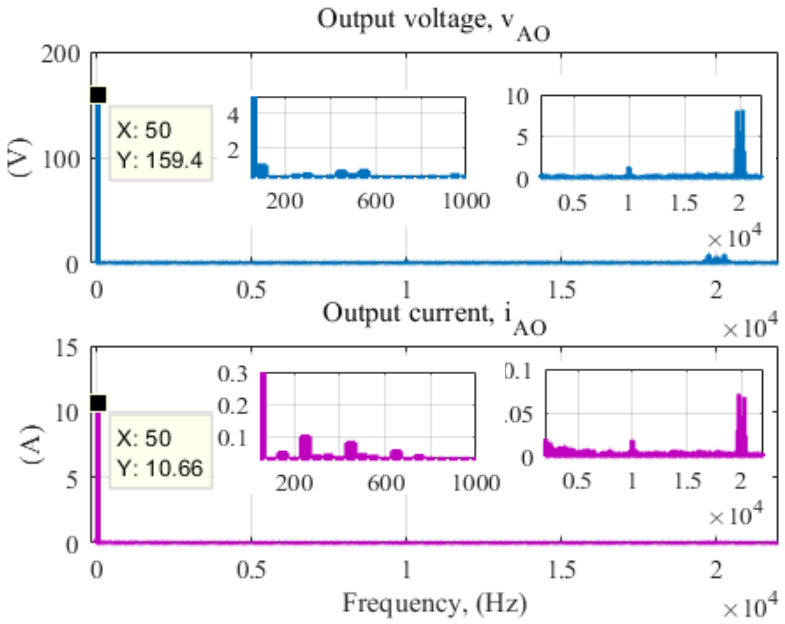
7.6.5 Comparison of the efficiency curves

Fig. 7.35 indicates the experimental efficiency curves of the reduced scale qZS-MMC prototype when using RICs and SS techniques with different output power at gain value equals 1.5 and under DC source voltage V_{DC} = 225 V. The way the efficiency has been determined is as follows: The different value of output power is obtained by changing the load resistance value while the output voltage is kept constant. The input power was measured by reading the voltage and current readings delivered by the power supply whilst the output power was calculated

by measuring the load current and then using the I^2R power relation. Using the RICs technique makes the converter more efficient compared to SS technique. The efficiency at highest tested load power reaches 93.5% at a load power of 920 W when using RICs technique compared to 91.5% for the SS technique respectively.

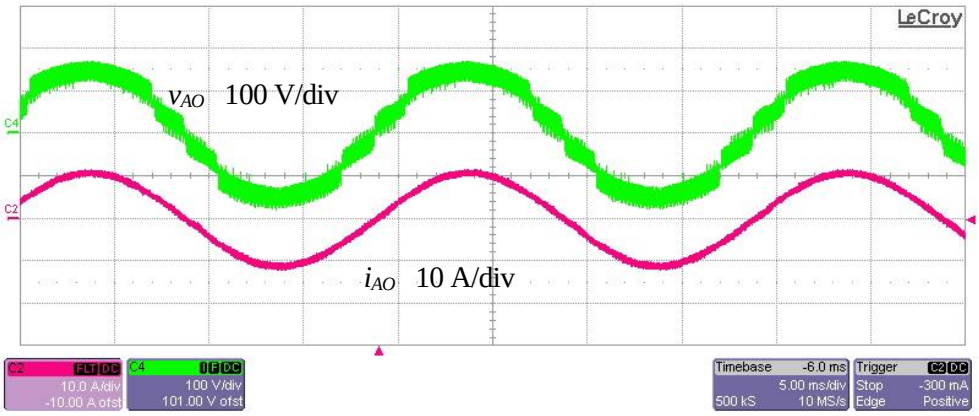


(a)

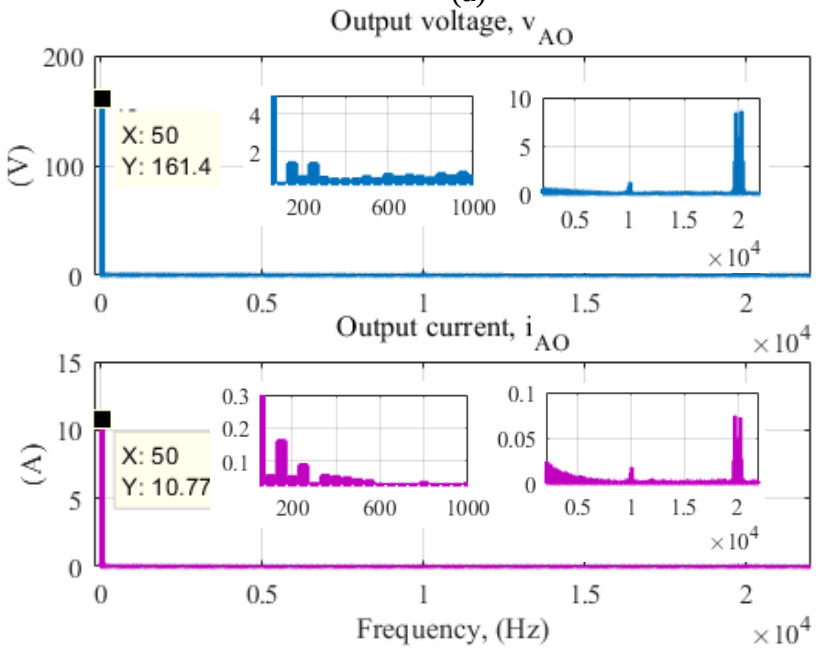


(b)

Fig. 7.33: Experimental results when using SS technique at D_{sh} = 0.25, m = 0.98, and V_{DC} = 225 V: a) the output voltage and current, and b) their harmonic spectrum



(a)



(b)

Fig. 7.34: Experimental results when using RICs technique at D_{sh} = 0.17, m = 0.98, and V_{DC} = 225 V: a) the output voltage and current, and b) their harmonic spectrum

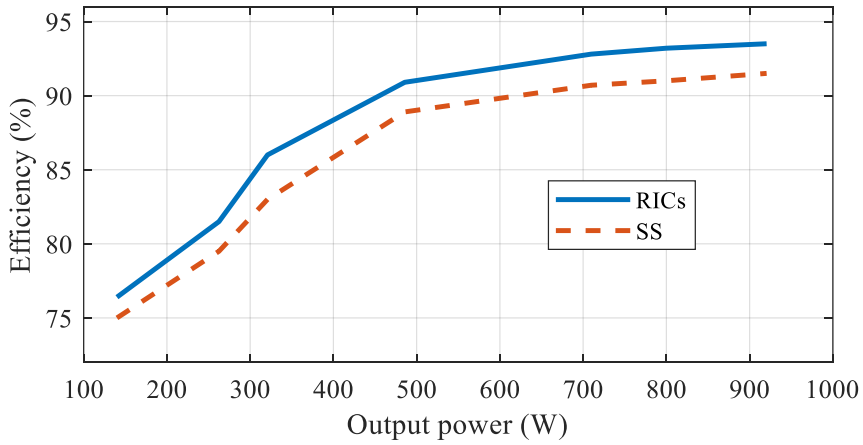


Fig. 7.35: Efficiency comparison of the experimental prototype with both modulation methods for constant output voltage (variable load current)

7.7 Operation under a DC-fault

In this section, the response of the proposed qZS-MMC to the DC-fault that has been described in Chapter 5, is experimentally validated. A pole-to-pole DC-fault has been imposed at the DC source terminals between points X and Y as shown in Fig. 7.1. The main AC grid has been connected to the AC output terminals of the qZS-MMC. The DC-fault has been implemented by using a contactor in series with a 2 Ω resistor to limit the fault current to a relevant but not dangerous level. The circuit parameters for this test are given in Table 7.2.

Table 7.2: Parameters of the experimental setup used in the DC-fault test

Parameter	Value
Converter peak output voltage (V_m)	65 Vpk
Transformer voltage ratio	$220\sqrt{2}$ / 65 V
DC source voltage	100 V
SM capacitor voltage	65 V
Fault resistance	2 Ω
Grid inductance	2 mH
Number of SMs per arm (N_{SM})	2

The inductances and capacitances are the same as given in Table 7.1. The DC source voltage is set initially at 100 V and reduces quickly to around 10% once the fault occurred due to maximum current limitation of the DC voltage supply.

Initially the converter operates in inverter mode. The controller detects the fault by monitoring the DC-side current ($i_{LS} = i_{LU2} = i_{LN2}$). When a fault occurs, this current is reversed and rapidly increases exceeding a predefined threshold current level. In this study, the threshold value is set to $-I_L$ = -1.2. Once the fault is detected, all converter IGBTs are turned off and consequently the DC-side current settles to zero.

The DC-side fault has been imposed many times, where two different fault cases illustrating the DC-side current which look very similar, are shown in Fig. 7.36. It is noted that, the DC-side current oscillates following a natural resonance then it settles to zero which results in an absolute peak overshoot current of approximately 2.5 times the operating DC link current from the pre-fault condition.

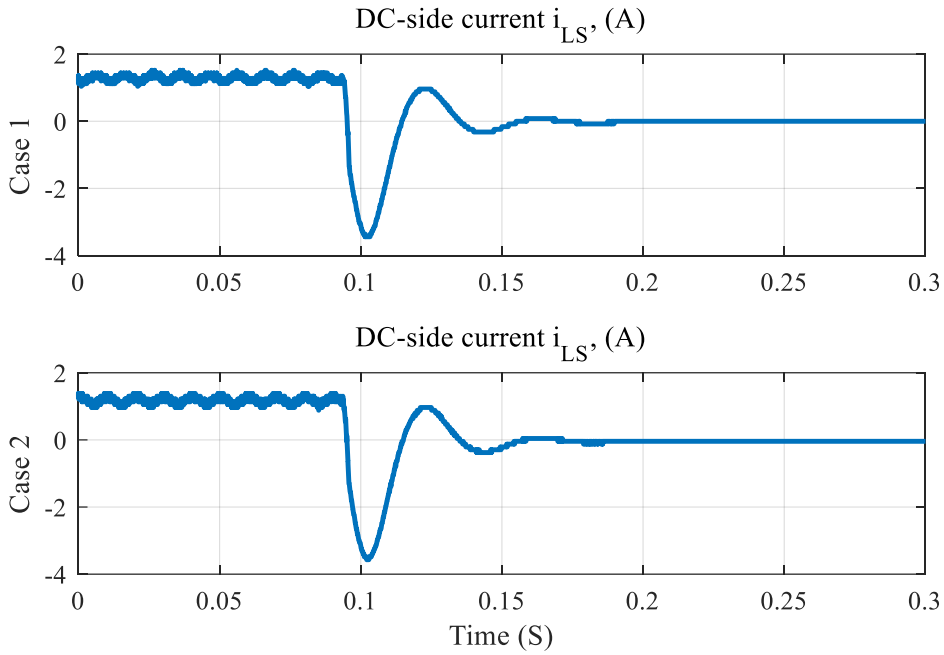


Fig. 7.36: Experimental results showing DC-side current for two different fault cases

Although this value may be considered high, it should be noted that the resonant current only flows through the inductors and the capacitors of the qZS-networks and this current does not flow through the qZS-switches S_U, S_N, S_{U1} and S_{N1} posing therefore no danger for the power semiconductors as discussed in section 6.2.1. To illustrate this, the DC-side current i_{LS} and one of the chain-link switch current i_{SU} are shown in Fig. 7.37.

The supply voltage V_{DC}, the grid voltage v_{AO}, the grid current i_{AO} and the lower arm current i_{NA} are shown in Fig. 7.38. After all the IGBTs are blocked, the grid current and the lower arm current reduce to zero. It is worth noting that a small current still flows in the lower arm and the grid as shown in Fig. 7.38 and discussed previously in section 6.2.1. The complete blocking needs additional time and occurs when the qZS-capacitors voltages increase above the peak value of grid voltage, which will allow all the diodes to become completely reverse biased.

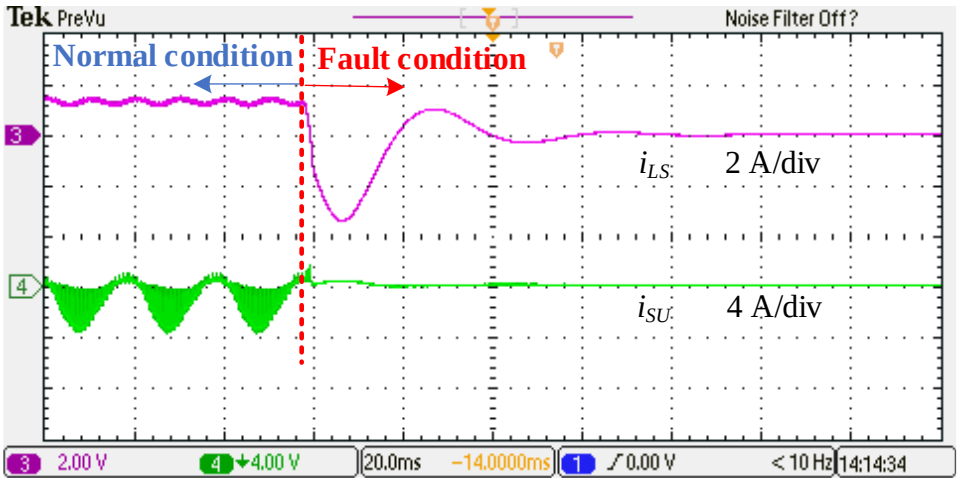


Fig. 7.37: Experimental results of the DC-fault showing the source inductor current i_{LS} (2 A/div) and the qZS switch current i_{SU} (4 A/div)

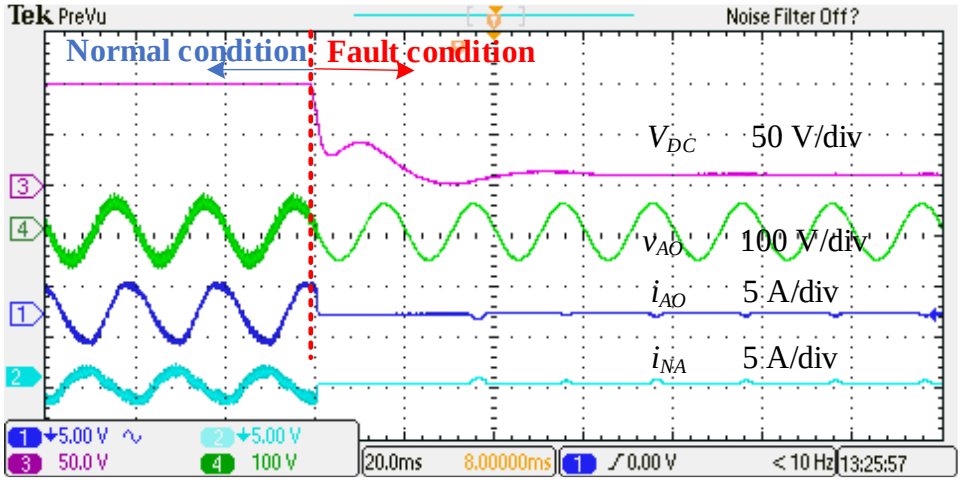


Fig. 7.38: Experimental results of the DC-fault showing DC-voltage V_{DC} (50 V/div), grid voltage v_{AO} (100 V/div), grid current i_{AO} (5 A/div), and arm current i_{NA} (5 A/div)

The qZS-capacitors C_{U1} and C_{U2} start to discharge and charge respectively until their voltages become approximately equal as illustrated in Fig. 7.39 (Ch2 and Ch3 have the same reference position), whereas the SMs capacitor voltages remain mostly unchanged.

The experimental results delivered in this section verify the theoretical analysis and the simulation studies regarding the DC-fault blocking capability of the proposed qZS-MMC as discussed in Chapter 5.

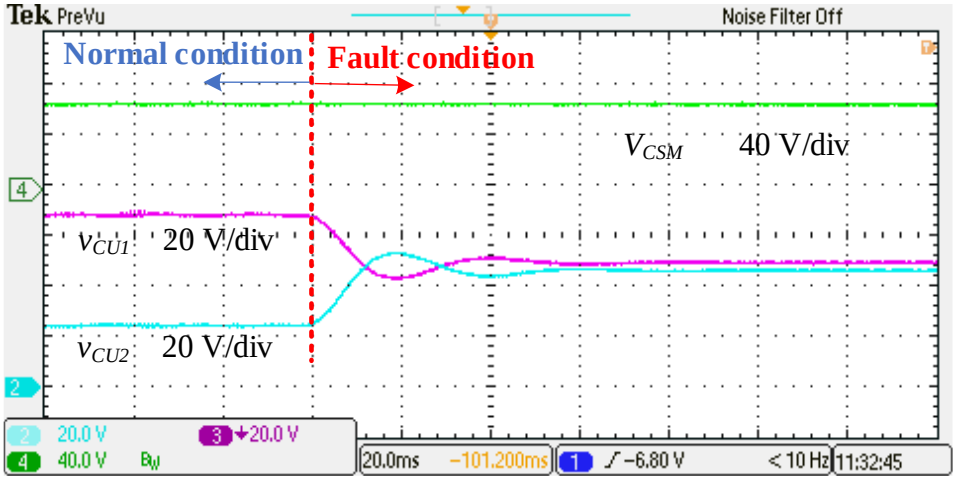


Fig. 7.39: Experimental results of the DC-fault showing the SM capacitor voltage v_{CSM} (40 V/div), qZS capacitor voltages v_{CU1} and v_{CU2} (20 V/div)

7.8 Conclusions

The design of a reduced scale laboratory rig has been presented. This prototype can be used to assess the performance of the proposed qZS-MMC. A single-phase converter has been provided with 2 SMs per arm and consequently it can output a 5-level voltage waveform. The converter hardware including passive and active components and gate driving circuit is given in detail at output power of 2 KW and fundamental peak of the output voltage of 170 V. In addition, the control platform (DSP and FPGA), voltage and current measurement circuits and PWM vectors generation have been described.

This chapter has also presented the experimental results conducted on the described test rig. The outcomes of the experiments validate the ability of the proposed converter to perform voltage buck-boost operation while maintaining multilevel function. Firstly, the negative effect of using only the series diode in the qZS-network has been experimentally tested in buck and boost modes. It has been proved that the undesired mode has appeared, which leads to a distortion in the output voltage and current. This problem has been solved by connecting an IGBT in antiparallel to the series diode and the improvement has been experimentally validated.

To reduce the voltage spikes on the DC-link switches, a snubber circuit has been used, which decreases the spikes in the DC-link voltages to a negligible level.

The proposed two modulation techniques namely the SS and the RICs have been compared and validated experimentally. Compared with the SS technique, the RICs technique achieves smaller stress voltages on the chain-link switches and the qZS capacitors, at the same voltage gain. In addition, for the same source side inductances, the switching ripple in the source current when using the RICs technique is approximately half of that when using the SS technique. For the same SMs capacitance, the SMs capacitor voltage has a smaller ripple when using the RICs compared with the SS technique. The peak to peak SM capacitor voltage ripple in case of RICs technique is about 85% of that for the SS technique which means a smaller capacitor could be used in a converter controlled by RICs technique. However, using the RICs technique provides high ripple at the fundamental frequency component in the qZS-inductor currents, which requires larger inductors compared with the SS technique. Finally, both modulation techniques resulted in a similar harmonic profile with a negligible value of low order harmonics in the converter output voltage and current. The THD values using both modulation techniques were about 13% for the output voltage and 4% for the output current at the experiment design conditions used.

The ability of the proposed converter to block the DC-fault current has been experimentally investigated for a pole-to-pole fault. The fault has been imposed using a mechanical contactor in series with a resistor to limit the fault current to a relevant but safe level. The converter controller has detected the DC-fault and blocked all IGBTs to block the fault and prevent damaging the converter components.

It can be finally concluded that the experimental results obtained support fully the theoretical analysis and simulation results.

Chapter 8

Novel quasi Z-Source Hybrid MMC

8.1 Introduction

In this chapter, the three-phase qZS hybrid MMC (qZS-HMMC) has been proposed. The work in this chapter is considered as an initial study for the qZS-HMMC and this topology still needs further investigation. The operation principle of the proposed configuration with the RICs technique is presented. Chapter 4 and Chapter 5 indicate that RICs is more advantageous than SS technique in terms of voltage stress on the chain-link switches, overall losses and capacitors size. Using RICs with qZS-MMC has a disadvantage where qZS-inductors of large size are required. This problem is due to the inability to introduce ST mode during a half cycle of the output frequency. Using hybrid configuration of MMC, HBSMs and FBSMs, allows to insert ST mode during the whole interval of the output frequency cycle, consequently small inductors size can be used. Also, this hybrid connection allows the converter to be simply extended to three-phase configuration.

The capacitor sorting algorithm discussed in section 3.5, needs to be modified in order to ensure SMs capacitor voltages balancing between HBSMs and FBSMs is presented. The operation and analysis of the proposed converter is validated using simulation model.

8.2 qZS Hybrid MMC: circuit configuration and operation principles

The structure of the three-phase qZS hybrid MMC (qZS-HMMC) is shown in Fig. 8.1. The MMC leg consists of the upper and lower arm. Each arm is formed by N_{SM} series-connected sub-modules (SMs) comprising $N_{SM}/2$ FBSMs and $N_{SM}/2$ HBSMs, and an arm inductor (L_O). The HBSMs and FBSMs are well balanced with average voltage of V_{CSM}. HBSM can generate two voltage levels (zero, $+V_{CSM}$) while FBSM can generate three voltage levels (zero, $+V_{CSM}$, and $-V_{CSM}$). It is worth to mention that the charging or discharging of HBSMs capacitors are depending on the direction of the arm current, while FBSMs capacitors get charged or discharged according to the polarity of both the arm current and SMs injected voltage.

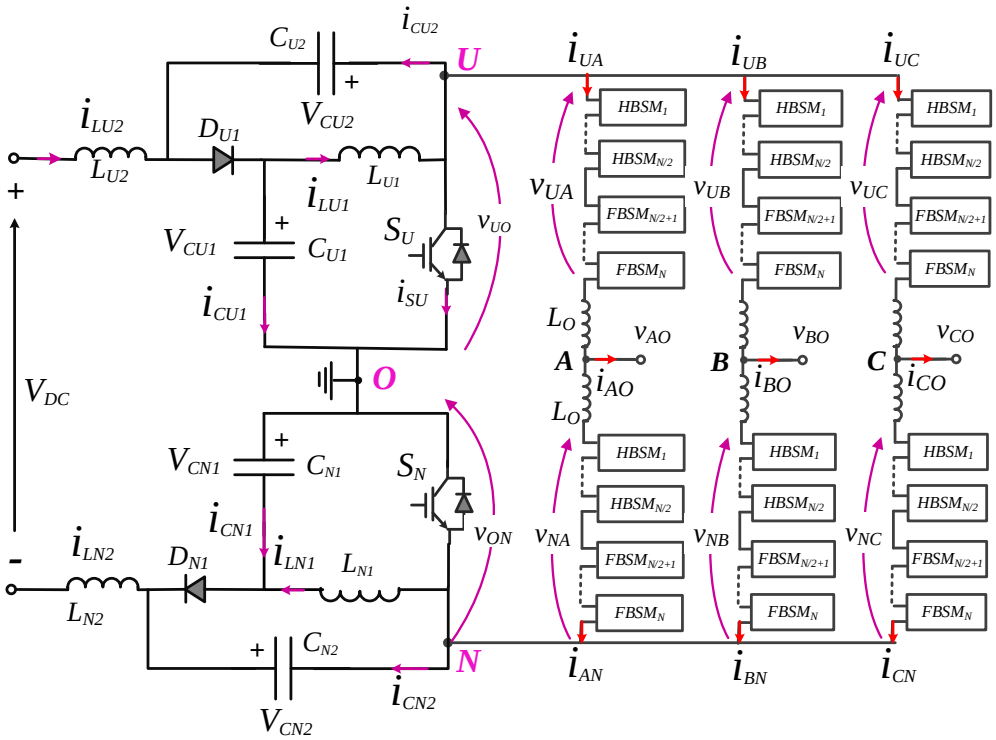


Fig. 8.1: Structure of a quasi Z-source hybrid modular multilevel converter qZS-HMMC

The two qZS-networks are introduced between the DC source (V_{DC}) and the DC-link terminals of the three-phase legs as shown in Fig. 8.1. The two networks share a midpoint node "*O*" between the two capacitors C_{U1}, C_{N1} that can be used

as a reference point for the output voltages.

The instantaneous voltage of the upper and the lower arms in phase *j*, where *j* = *A*, *B*, *C*, are represented by v_{Uj}, and v_{Nj} and the upper and lower DC-link voltages are denoted by v_{UO}, and v_{ON} respectively. By applying Kirchhoff's voltage law in Fig. 8.1, the three-phase output voltages are given by:

$$v_{jO}(t) = \frac{v_{UO}(t) - v_{ON}(t)}{2} - \frac{v_{Uj}(t) - v_{Nj}(t)}{2} \tag{8.1}$$

The three-phase upper and lower arm currents i_{Uj}, and i_{Nj} can be expressed by:

$$\begin{aligned} i_{Uj}(t) &= i_{cir-j} + \frac{i_{jO}(t)}{2} \\ i_{Nj}(t) &= i_{cir-j} - \frac{i_{jO}(t)}{2} \end{aligned} \tag{8.2}$$

where i_{jO} represents the three-phase output currents in phases *A*, *B*, and *C*. $i_{cir\text{-}j}$ is the circulating current in phase *j*. This current $i_{cir\text{-}j}$ contains a DC component $I_{UN}/3$, which is one-third of the DC-link current that provides the actual power transfer and AC components i_{zj} which usually contain second order harmonic. The circulating current $i_{cir\text{-}j}$ and the second order harmonic component i_{zj} can be calculated by:

$$\begin{aligned} i_{cir-j}(t) &= i_{zj}(t) + I_{UN}/3 \\ i_{zj}(t) &= \left(i_{Uj}(t) + i_{Nj}(t)\right)/2 - I_{UN}/3 \end{aligned} \tag{8.3}$$

8.3 Modulation technique: RICs technique

As previously illustrated in section 4.3.2 for a single-phase qZS-MMC, if the upper DC-link switches are performing a shooting-through, $N_{SM}/2$ SMs that are initially on, should be selected from the upper arm in each phase to be bypassed. The number of upper (lower) arm inserted cells greater than or equal to $N_{SM}/2$ can only be realized during the negative (positive) half-cycle of the output voltage waveform.

By extending this concept to the three-phase configuration, if the upper (lower) chain-link switches are turned on, at least one of the upper (lower) arms in the

three-phase legs will not be able to compensate the shorting of the upper (lower) DC-link terminals and that causes the number of the output voltage levels of that particular legs to change by maximum N_{SM} /2 voltage levels. Consequently, a significant distortion in the corresponding output phase voltage will be produced.

For more illustration, the three-phase upper arm modulating signals have been drawn as shown in Fig. 4.14 where the number of inserted SMs in the upper arms in phases *A*, *B*, and *C* are N_{UA}, N_{UB}, and N_{UC} respectively. In the region R_1, the N_{UB} is higher than $N_{SM}/2$ while both the N_{UA} and N_{UC} are lower than $N_{SM}/2$, leading to distortion in the phases *A* and *C* during shooting-through of the upper DC-link terminals. Phase *A* output voltage will be distorted in regions from R_1 to R_3, and phase *B* will be distorted from R_3 to R_5, while R_1, R_5, and R_6 will be affected for phase *C*, as shown in Fig. 4.14.

To solve this, a half number of the SMs needs to be replaced by FBSMs with a ratio 1:1 for HBSMs and FBSMs as shown in Fig. 8.1. The negative voltage states of the FBSMs have been used to compensate the voltage drop in the DC-link, especially when the number of inserted SMs is lower than N_{SM} /2. Considering phase *A*, during ST intervals of upper qZS-network and the regions R_1 to R_3 (where $N_{UA} < N_{SM}$ /2), the N_{UA} that are initially inserted will be bypassed and N_{SM} /2-N_{UA} of FBSMs will be inserted with their negative voltage polarities (-V_{CSM}). While during ST intervals and the regions R_4 to R_6 ($N_{UA} \geq N_{SM}$ /2), the N_{SM} /2 that are initially inserted will be bypassed.

The ST reference signals of the upper and the lower chain-link switches can be simply achieved by comparing the triangle carrier signal with a level D_{sh} proportional with the desired ST duty cycle. Fig. 8.2 shows the upper and the lower chain-link gating signals and the modulating signals of the upper and lower arm of the phase *A*. During the ST intervals, the amplitude of modulating signals is dropped by $N_{SM}/2$ units of SMs carrier. As shown in Fig. 8.2, the chain-link gating signals are interleaved which is beneficial in reducing the switching ripples in the source and arm currents compared to non-interleaved one.

To calculate the average value of the SMs capacitor voltage, the upper and lower arm inductor voltages in NST mode (where S_U and S_N are off) for any phase, can be expressed by (8.4).

$$v_{LO-j}(t) = \frac{v_{UO}(t) + v_{ON}(t)}{2} - \frac{v_{Uj}(t) + v_{Nj}(t)}{2} \tag{8.4}$$

The equivalent circuit of the qZS-HMMC during the ST mode of the upper qZS-network in region R_1 is shown in Fig. 8.3. In region R_1, $N_{UB} \geq N_{SM}/2$ and N_{UA} & $N_{UC} < N_{SM}/2$, thus the number of inserted SMs in the phase B decreased by $N_{SM}/2$ to be $N_{UB} - N_{SM}/2$ with positive capacitor polarities. While the SMs, that are already inserted in phase A and C are bypassed and $N_{SM}/2$-N_{UA} and $N_{SM}/2$-N_{UC} of FBSMs will be inserted with negative voltage polarities as shown in Fig. 8.3. The upper and lower arm inductor voltages for phase j during ST mode can be expressed by:

$$v_{LO-j}(t) = \frac{v_{ON}(t)}{2} - (N_{Uj} + N_{Nj} - \frac{N_{SM}}{2}).\frac{V_{CSM}}{2} \tag{8.5}$$

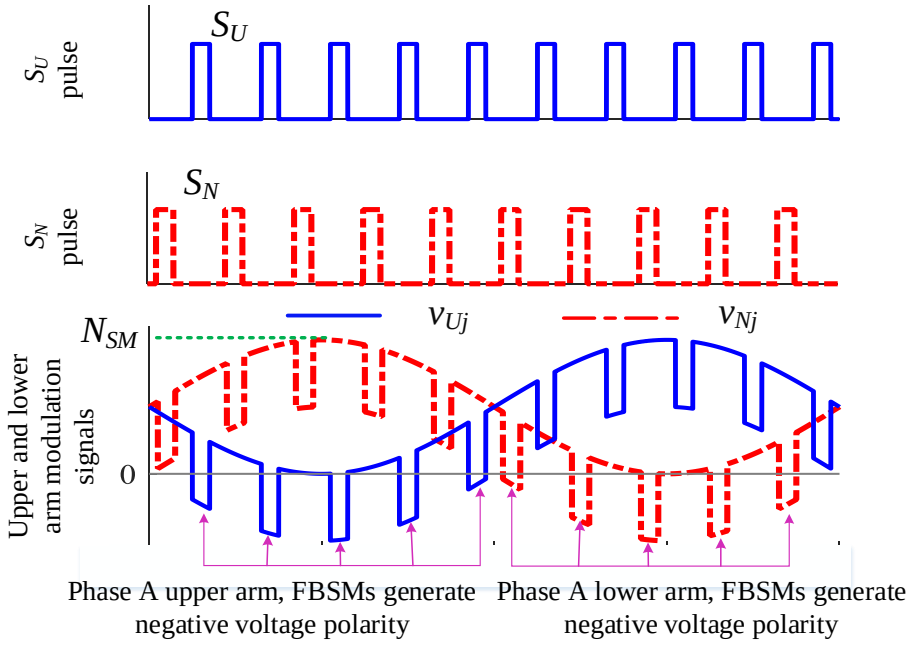


Fig. 8.2: RICs technique waveforms: a) upper, b) lower chain-link switches pulses, and c) upper and lower arm modulating signals

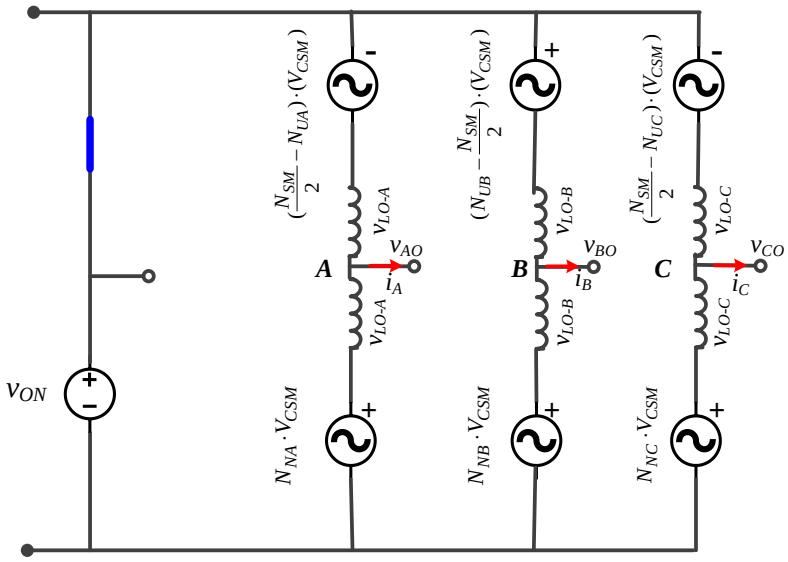


Fig. 8.3: Equivalent circuit for the qZS-HMMC when operating in region R_1 and upper DC-link switch S_U is turned on

where N_{Uj} and N_{Nj} are the number of inserted SMs in the upper and the lower arms respectively in phase j with $N_{Uj}+N_{Nj} = N_{SM}$. For a stable operation, the average voltage across the arm inductor over the switching period is equal to zero. Using (8.4) and (8.5), the arm inductor voltage is:

$$v_{LO-j}(t) = (1-D_{sh}) \cdot \left[\frac{v_{UO}(t) + v_{ON}(t)}{2} - \frac{v_{Uj}(t) + v_{Nj}(t)}{2} \right] + D_{sh} \cdot \left[\frac{v_{ON}(t)}{2} - (N_{Uj} + N_{Nj} - \frac{N_{SM}}{2}) \cdot \frac{V_{CSM}}{2} \right] = 0 \quad (8.6)$$

Consequently, the SMs average capacitor voltage is given by:

$$V_{CSM} = \frac{1}{N_{SM}(1-2D_{sh})} V_{DC} = V_{UN} / N_{SM} \quad (8.7)$$

The SMs capacitors V_{CSM} will be charged according to the peak value of the DC-link voltage divided by N_{SM}. As a result, the number of the series switches in each chain-link will be equal to half the number of SMs in each arm, assuming an equal voltage rating with the SMs switches. The peak of fundamental phase voltage V_m can be expressed by (8.8), where m is modulation index and G is the converter voltage gain defined by (4.29).

$$V_m = \frac{mN_{SM}V_{CSM}}{2} = \frac{m}{(1-2D_{sh})} \times \frac{V_{DC}}{2} = \frac{mGV_{DC}}{2} \tag{8.8}$$

It is necessary to ensure that the SMs capacitor voltage in both HBSMs and FBSMs are well balanced. The HBSMs capacitor can be charged only when the arm current is positive and discharged when the arm current is negative. Thus, it is important to analyse the effect of using the negative voltage polarity of the FBSMs on the charging and discharging of the HBSMs. Neglecting the converter power losses, the input power $P_{DC} = V_{DC} \cdot I_L$ equals to the DC-link power which is the product of the DC component in the DC-link current I_{UN} and the DC component in the DC-link voltage $(1-D_{sh}) \cdot V_{UN}$, and also equal to the load active power.

$$P_{DC} = (1-D_{sh}) \cdot V_{UN} \cdot I_{UN} = \frac{3 \cdot V_m \cdot I_m}{2} \times \cos\varphi \tag{8.9}$$

The DC component in the arm current can be expressed by:

$$I_{UN} = \frac{3 \cdot m \cdot \cos\varphi \cdot I_m}{4 \cdot (1-D_{sh})} \tag{8.10}$$

Substituting from (8.10) into (8.2) and considering AC-circulating current is suppressed to a negligible level, the arm currents are:

$$\begin{aligned} i_{Uj}(t) &= \frac{m \cdot \cos\varphi \cdot I_m}{4 \cdot (1-D_{sh})} + \frac{i_{jO}(t)}{2} \\ i_{Nj}(t) &= \frac{m \cdot \cos\varphi \cdot I_m}{4 \cdot (1-D_{sh})} - \frac{i_{jO}(t)}{2} \end{aligned} \tag{8.11}$$

As noted, the DC component in the arm current is increasing with increasing D_{sh} (more gain G) leading to a reduction in the negative interval of the arm current. The negative interval of the arm current should be enough to discharge the HBSMs capacitor. Therefore, the following condition must be satisfied.

$$I_{UN} < \frac{I_m}{2} \Rightarrow D_{sh} < 1 - \frac{m\cos\varphi}{2} \tag{8.12}$$

At unity modulation index m and cos φ, D_{sh} should be lower than 0.5, which is already the maximum limit for stable operation as deduced in (8.7). Otherwise, the arm current will be always positive and the HBSMs capacitor can only charge

causing unbalance operation. However, practically the maximum D_{sh} is ranged between 0.35 to 0.4 depending on circuit voltage drop on the passive and active components. With reducing the DC supply voltage, the duty ratio D_{sh} increases to compensate for the change in the supply voltage and the interval needed for FBSMs to generate negative voltage polarity increases. This leads to a difference in the duty ratios of the FBSMs and HBSMs and causes slightly difference between average capacitor voltage of FBSMs and HBSMs particularly at high values of D_{sh}, but they are still balanced.

8.4 SMs capacitor voltage balancing algorithm

The sorting method given in section 3.5 has been adopted and applied to ensure SM capacitor voltages balancing for qZS-HMMC. The steps of sorting and selection algorithm for the upper arm (the lower arm will be similar) are shown in Fig. 8.4 and are summarized as follows:

1. Measure and sort all upper and lower capacitor voltages in each phase and also, sort FBSMs capacitor voltages.
2. The modulation scheme will determine the number of inserted SM capacitors N_{Uj} and N_{Nj} in each phase.
3. If the upper qZS-network works in NST mode:
    - If the upper arm current is positive, choose the N_{Uj} SMs with the lowest voltage to be inserted. Therefore, the corresponding SMs capacitors are charged.
    - If the upper (lower) arm current is negative, choose the N_{Uj} SMs with the highest voltage to be inserted. Therefore, the corresponding SMs capacitors are discharged.
4. If the upper qZS-network works in ST mode, and $N_{Uj} \geq N_{SM}/2$: N_{Uj} should be reduced by $N_{SM}/2$. The new number of inserted cells N_{Uj} - $N_{SM}/2$ in each arm should be selected according to step 3 regardless of the SMs configuration.
5. If the upper (lower) qZS-network works in ST mode, and $N_{Uj} < N_{SM}/2$: all the inserted SMs N_{Uj} should be bypassed. In addition, $N_{SM}/2$ - N_{Uj} of FBSMs should be inserted by their negative voltage polarity.

- If the upper arm current is positive, choose $N_{SM}/2$ - N_{Uj} FBSMs with the highest voltage to be inserted. Therefore, the corresponding FBSMs capacitors are discharged.
- If the upper arm current is negative, choose the $N_{SM}/2$ - N_{Uj} FBSMs with the lowest voltage to be inserted. Therefore, the corresponding FBSMs capacitors are charged.

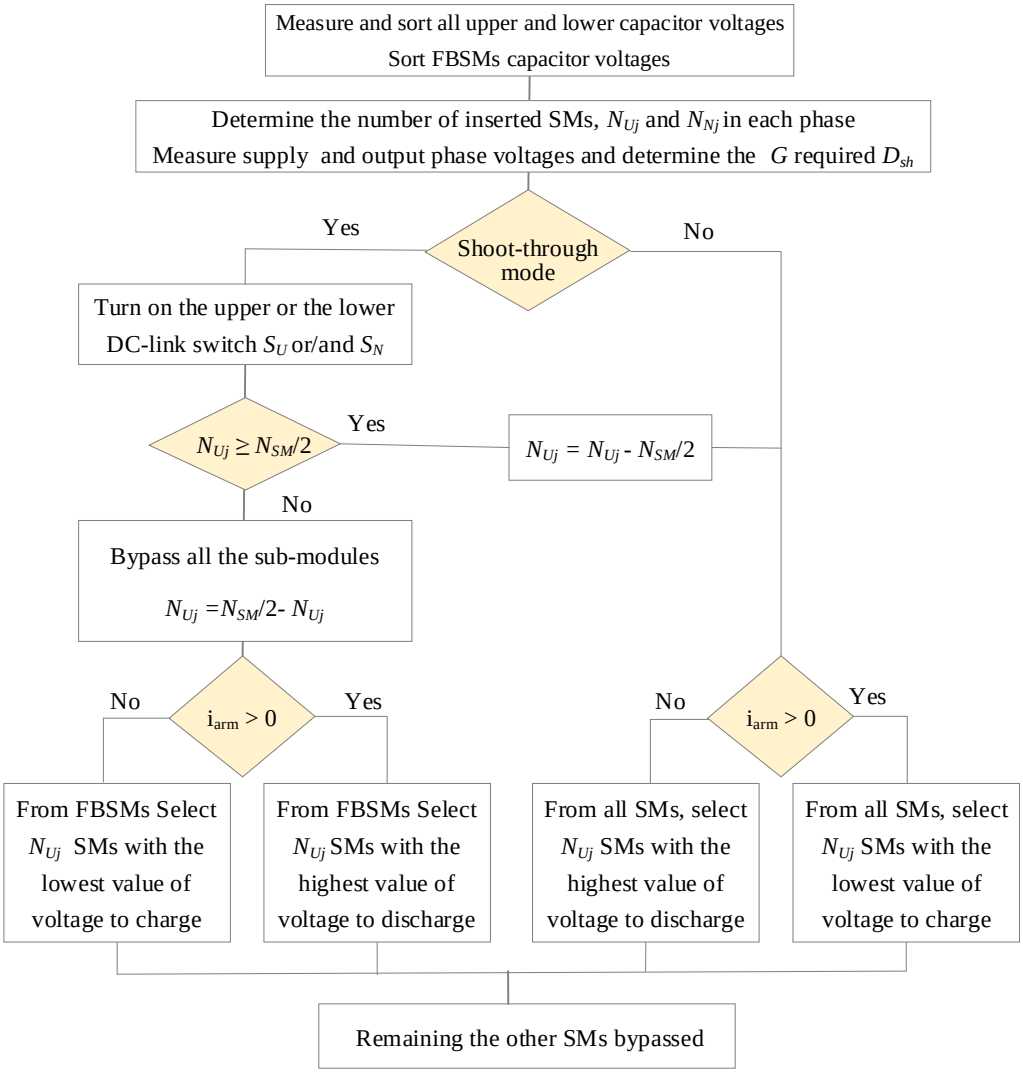


Fig. 8.4: Flow chart of sorting and selection algorithm

8.5 Simulation results

To verify the validity of the proposed qZS-HMMC, relevant simulations model was implemented in PLECs software for the proposed configuration shown in Fig. 8.1. The parameters used in the simulation models are given in Table 8.1.

Table 8.1: Parameters of the qZS-HMMC simulation model

Parameter	Value
Line-line RMS voltage	6.6 kV
Number of SMs per arm (N_{SM})	4
DC source voltage (V_{DC})	6.6 kV
SM capacitor voltage (V_{CSM})	2.75 kV
Arm inductance (L_o)	5 mH
SMs capacitances (C_{SM})	3.3 mF
qZS inductances ($L_{U1} = L_{U2} = L_{N1} = L_{N2}$)	10 mH
qZS capacitances ($C_{U1} = C_{N1}$)	3.3 mF
qZS capacitances ($C_{U2} = C_{N2}$)	3.3 mF
Load resistance and inductance	10 Ω, 10 mH
Carrier frequency (f_c)	2 kHz

The simulation study has been carried out using a passive inductive load (R+L) and considering that all system components and switches are ideal.

Firstly, D_{sh} and m are set at 0.2 and 1 respectively. According to (4.29), the gain value is 1.67. To attain 6.6 kV line-line RMS voltage, the source voltage needs to be 6.6 kV. Fig. 8.5 shows that the upper and the lower DC-link voltages which have a peak value of 5.5 kV and the zero notches are interleaved as shown in Fig. 8.5b which helps with DC source current and arm current ripple filtering.

The upper arm SM capacitor voltages of the three phases shown in Fig. 8.6 are charged equally and their voltages are calculated according to the peak value of the total DC-link voltage divided by N_{SM} as derived in (8.7).

The RICs technique, which has been implemented here, provides a proper operation for the converter without any distortion in the output voltages and currents. The three-phase output voltages and currents and their harmonic spectrums are shown in Fig. 8.7 and Fig. 8.8 respectively. It is noted that, the peak value of the fundamental output phase voltages is equal to 5.36 kV, which is approximately equal to the peak value of the half DC-link voltage at $m = 1$.

It is noted that the switching harmonics of the output voltages appear as sideband clusters of the carrier frequency where the most dominant harmonic cluster is located at twice the carrier frequency (4 kHz). The low order harmonics of the output voltages and currents are insignificant with the 3rd harmonic being the largest at 0.74% and 0.5% of the fundamental voltage and current components, respectively.

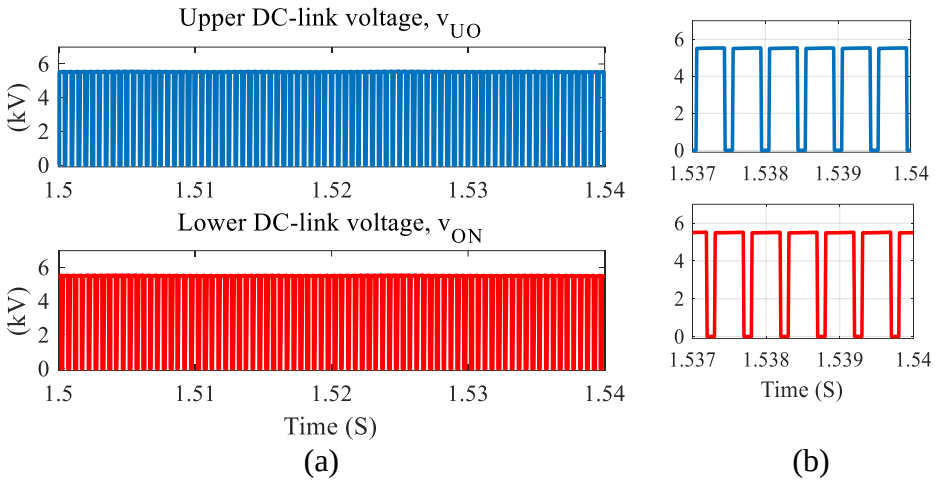


Fig. 8.5: qZS-HMMC simulation results, a) the upper and the lower DC-link voltages, and b) zoomed view

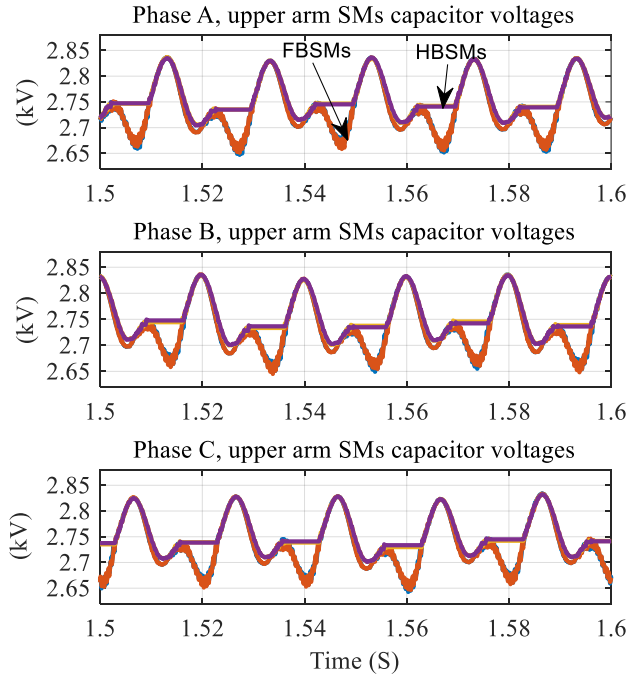


Fig. 8.6: Upper arm SMs capacitor voltages in the three phases

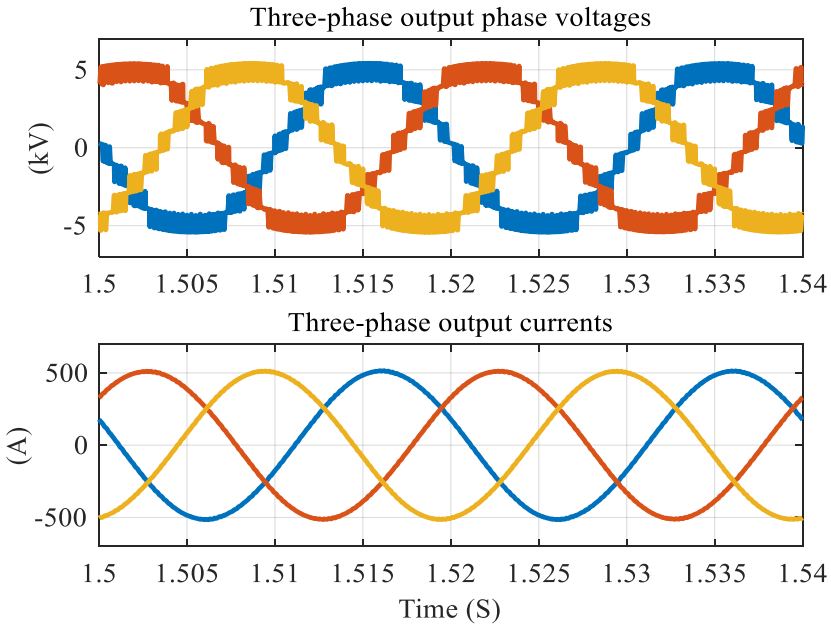


Fig. 8.7: Three-phase output voltages and currents

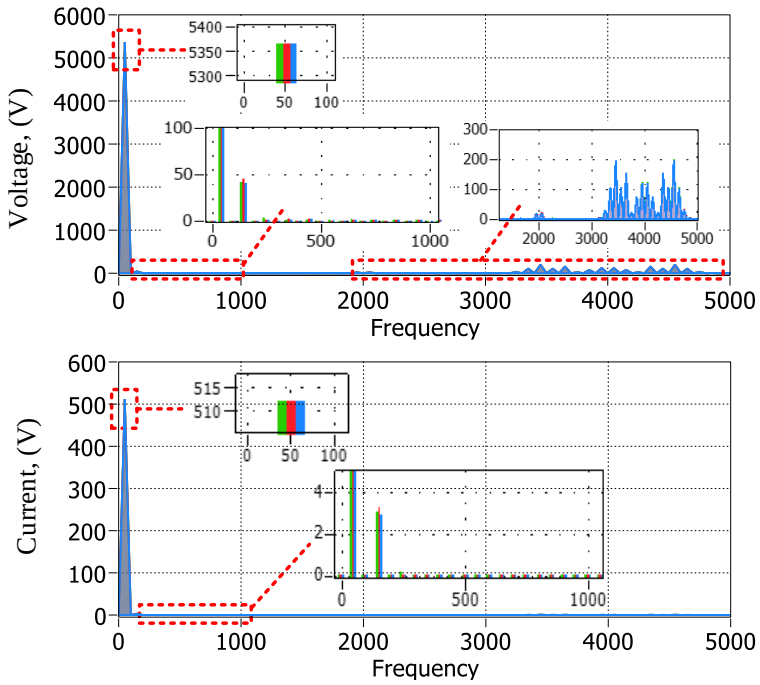


Fig. 8.8: Harmonic spectrum of phase voltages and currents

To attain a fixed output phase voltage of 5.5 kV at different values of the supply voltage, the duty ratio D_{sh} should be adjusted to compensate for the change in supply voltage. When reducing the DC source voltage, the duty ratio D_{sh} increases and the interval needed for FBSMs to generate negative voltage polarity increases. This will lead to a difference in the duty ratios of the FBSMs

and HBSMs and may cause unbalance between FBSMs and HBSMs. Fig. 8.9 shows the phase A upper arm SMs capacitor voltages at different values of the D_{sh}, which are 0.1. 0.2, 0.25 and 0.33 and consequently according to (4.29) the gain values become 1.25, 1.66, 2 and 3 respectively. With increasing the gain, the difference between the average values of FBSMs and HBSMs capacitor voltages are increasing, but they are still balanced.

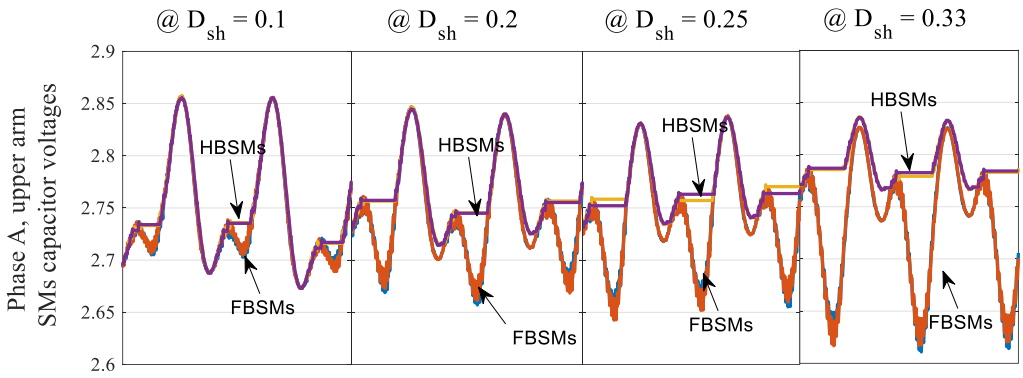


Fig. 8.9: Phase A upper arm SMs capacitor voltages at different duty ratios

8.6 Conclusions

This chapter proposed a novel three-phase quasi Z-source hybrid modular multilevel converter (qZS-HMMC) topology consisting of an equal number of HBSMs and FBSMs powered via two quasi Z-source networks. This converter can operate not only step down (buck) mode, but also has voltage boost capabilities. The reduced inserted cells (RICs) modulation technique has been modified to suit the particularities of the proposed converter and implemented in a simulation model. The sorting and selection algorithm to ensure capacitor voltages balancing between FBSMs and HBSMs is adopted. The work in this chapter only shows the proof of concept of the qZS-HMMC and this topology still needs further investigation.

Chapter 9

Conclusions and Future Work

This chapter presents the core findings of the work presented in this PhD thesis. Proposals for future research work are also provided.

9.1 Conclusions

Due to increased penetration of embedded generation systems, especially renewable energy resources such as wind turbines and photovoltaics in the electric power systems, the need has increased to design power converters which can successfully operate with these sources. The output voltage of most renewable energy sources fluctuates in a wide range with changes in the operating conditions. Therefore, having power converters that can compensate for these fluctuations is desirable. Multilevel converters are often considered the best candidate topology due to their improved waveform quality. However, most multilevel converters suffer from the drawback that they only operate in buck mode (the peak output voltage cannot be higher than half the DC input source voltage). Among multilevel converters, the modular multilevel converter (MMC) is an interesting type, it provides several features such as modularity, voltage and power scalability and the potential for redundancy. The MMC based on half-bridge sub-module (HBSM), which is considered the simplest structure, only provides a buck function. Thus, instead of HBSM, a full-bridge sub-module (FBSM) based MMC has been recommended to provides voltage boost function.

However, this configuration requires twice as many IGBTs as the half-bridge sub-modules, which is reflected in the cost and the total converter losses.

Impedance networks have been used at the DC terminals of two-level voltage source inverters to increase the input DC voltage to higher levels which allows the converter to operate in boost mode. This integration has also been extended to the multilevel converters (the neutral point clamped (NPC) and cascade H-bridge (CHB) converters) to provide a voltage-boost function. The integration of the impedance network to the MMC had not been reported in the literature, which encouraged the work presented in this thesis.

Therefore, a novel quasi Z-source modular multilevel converter (qZS-MMC) has been presented in this thesis. The proposed topology takes the advantages of not only performing the common voltage-buck function but also a voltage-boost function. In addition, the proposed qZS-MMC has an intrinsic capability to block fault current during a DC side fault. The scope of this thesis focused on the operation principles, suitable modulation techniques, converter design, and converter losses estimation of this novel topology.

Firstly, a review of the common multilevel converters regarding their advantages, disadvantages, and applications, has been presented. The ability of the multilevel converters to be integrated with variable voltage sources in renewable energy systems such as wind and photovoltaic has been reported. Since most multilevel converters provide a buck function only, they cannot always be directly integrated with these renewable sources. These converters can be improved with additional hardware to provide a voltage-boost capability and then become appropriate for integrating the renewable energy sources. For example, a MMC and NPC converters has been used in back-to-back configurations in order to integrate wind turbines, and also impedance-networks have been recently used with NPC and CHB multilevel converters to integrate wind turbine and photovoltaic systems. Furthermore, an MMC has been built with FBSMs instead of HBSMs in order to provide a voltage-boost function, but the number of semiconductor switches is doubled. Also, the hybrid MMC that consists of half-bridge and full-bridge SMs was developed to reduce the switches

count, but the boost factor is limited due to voltage unbalance problem between the sub-modules.

The review of impedance network based multilevel converters showed that the impedance networks have not been implemented with the MMC yet. The concept of integrating the impedance network with a MMC may become a good addition to the family power converter topologies and become a competitor to the NPC and CHB based impedance network topologies in terms of obtained a number of output voltage levels, number of required isolated DC sources and number of qZS-networks. Therefore, this thesis presented the integration of the impedance network with the MMC to understand the advantages and disadvantages of this integration compared with some other multilevel converter topologies with voltage-boost function.

Among impedance network topologies, the quasi Z-source (qZS) network has received more attention with CHB and NPC converters, consequently this thesis investigated the operation of the HBSM based MMC when integrated with the qZS-network. The MMC features and operation principles have been reviewed. The common submodule configurations were presented with highlighting the advantages and disadvantages of each configuration. The applicable modulation techniques for the MMC were briefly discussed. The SMs capacitor voltage balance has been explained, where the capacitors in each arm are sorted in ascending or descending order based on the arm current polarity and the number of inserted sub-modules, specific SM capacitors are selected to be inserted or bypassed.

The proposed qZS-MMC has been configured by connecting two qZS-networks at the DC-link terminals of the MMC. The boost action has been attained by the introduction of a short circuit (shoot-through) at the output terminals of the qZS-networks in order to increase the energy stored in the qZS-network inductors which is later transferred to the qZS-network capacitors. This stored energy provides the voltage boosting capability. To provide the shoot-through action, a chain-link switch has been connected to the end-terminals of each qZS-network, where the shoot-through action cannot be attained depending on the SMs in both the upper and lower arm due to losing the benefit of having multilevel

functionality. Moreover, it has been shown that the series diode in the qZS-network should connected to antiparallel IGBTs in order to avoid the appearance of any undesired operating modes.

A significant part of the project has focused on how to properly design the modulation techniques with the boost function and without affecting the number of levels in the output voltage. Two carrier-based modulation techniques, simultaneously shorted (SS) and reduced inserted cells (RICs) have been proposed and compared with each other. Phase disposition PWM (PD-PWM) has been selected for the work in this thesis due to the high quality of the AC output voltage waveform. The difference between the modulation techniques is how to compensate for the shoot through action and avoid a large disturbance in the output voltage.

The SS technique depends on introducing the shoot-through mode to the two qZS-networks at the same time. While the RICs technique depends on compensation of shooting through of one qZS-network by having an adapted voltage by the corresponding arm. The implementation of each technique has been described in detailed. The relationship between the shoot-through duty ratio and converter gain has been deduced for both techniques with illustrating the SMs capacitor voltage relation according to the DC-link voltage. Moreover, guideline for sizing the passive components has been developed. The RICs achieves smaller stress voltages on the qZS switches and the qZS capacitors. In addition, the SMs and qZS-network capacitor voltage has a smaller ripple when using the RICs technique compared with the SS technique. For the same switching ripple in the source current, the required source side inductance of the qZS-networks when using the RICs technique is approximately half of required inductance when using the SS technique. However, using the RICs technique provided a much higher ripple value of the fundamental frequency component in the qZS-inductor currents (inner inductors L_{U1} and L_{N1}), which requires inductors with large inductance compared with SS technique, while it requires a much lower arm inductance in order to limit the switching ripples.

The semiconductor power loss estimation procedure has been presented for each modulation technique. The SS technique causes more conduction losses in qZS-

networks while the two techniques give approximately equal arm conduction losses. Since the voltage stress on the chain-link switches is higher in the case of using the SS technique, the qZS-networks switching losses are higher when using the SS technique than the RICs technique especially with higher gains. On the other hand, the RICs technique causes more SMs switching losses compared to the SS technique due to higher number of commutations during one carrier frequency cycle. The total losses when using the SS technique are higher when compared with the RICs technique.

Similar to the traditional MMC, the circulating current in the qZS-MMC may contain low order even components (especially 2^{nd} order component), which may bring additional losses and current stress on the arm switches. Thus, a control scheme has been presented to suppress these components in the circulating current. In addition, a control scheme to maintain stable operation under components asymmetry (due to component tolerance) has been presented.

A significant advantage of the proposed qZS-MMC is providing a DC side fault blocking capability. The qZS-MMC can block DC-faults when the qZS capacitor voltages in the fault current path is higher than the grid voltage connecting the qZS capacitors by the negative polarity in the path of the fault. The converter performance has been investigated under pole-to-pole and pole-to-ground faults.

To evaluate the feasibility of the new solution, the qZS-MMC has been compared with the FBSM based MMC (FB-MMC) and quasi Z source cascaded multilevel converter (qZS-CMI) in terms of the required number of the passive and active components, voltage and current stresses, the semiconductor power losses and output voltage waveform quality. The number of IGBTs required for the proposed qZS-MMC modulated with the RICs and SS technique in the case of the single-phase converter are 75 % and 87.5 % of that required for the FB-MMC, and are 80 % and 93.3 % of that required for the qZS-CMI, which is considered a significant reduction. The qZS-MMC uses four more inductors and two more capacitors compared to the FB-MMC, while the qZS-CMI requires more inductors, capacitors and isolated DC sources depending on the number of sub-modules.

The stress voltages of the SM switches are equal for the proposed qZS-MMC and the FB-MMC, and both converters are higher than the qZS-CMI. The voltage stress of the series switches of the qZS-MMC is higher than that of the qZS-CMI. So, the qZS-CMI has the lowest voltage stress on SMs and qZS-switches, and also smaller qZS capacitor voltage. The qZS-MMC has lower current stress (approximately half value) through the SMs and qZS inductors when compared with the qZS-CMI, and also the qZS-MMC has a slightly lower current stress through the SMs and arm inductors when compared with the FB-MMC.

Concerning the power losses comparison, the qZS-MMC has the lowest conduction losses, and the conduction losses of FB-MMC is lower than of qZS-CMI, in both buck and boost modes. The qZS-MMC and FB-MMC have equal switching losses in buck mode, and both of them have switching losses higher than the qZS-CMI. While in boost mode, switching losses of the qZS-MMC is higher than the qZS-CMI, and FB-MMC has the lowest switching losses. Therefore, the FB-MMC has the lowest total losses (conduction and switching losses) in boost mode, while the qZS-MMC has lowest total losses in buck mode.

Regarding the output voltage waveform quality, the SS and RICs techniques produce similar harmonic spectrum and approximately equal THD. The switching harmonics of the qZS-MMC and the qZS-CMI appear as sideband clusters at the carrier frequency where the most dominant harmonic cluster is located at twice the carrier frequency. However, the harmonic profile of the FB-MMC has harmonics cluster at the carrier frequency, which may require a larger filter. The total harmonic distortion THD for the qZS-CMI is higher than the qZS-MMC and FB-MMC.

The proposed topology has been simulated in the PLECs software and different test cases were considered. The simulation results demonstrate the ability of the converter to perform buck-boost operation and generate multilevel output voltage waveform using both SS and RICs techniques. Comparison between the topologies (FB-MMC, qZS-CMI and proposed converter) has been verified by simulation. In addition, the converter has been examined under DC side faults by imposing pole-to-pole and pole-to-ground DC-faults in the simulation models.

In order to experimentally validate the proposed converter, a scaled down prototype of the single-phase qZS-MMC has been designed. The experimental system is rated at 2 kW and used 2 SMs per arm. The prototype has been controlled with the SS and RICs modulation techniques. The experimental results have been presented to validate the converter operation principles. Also, the converter performance under pole-to-pole DC-fault has been examined. The fault has been imposed using a contactor in series with a resistor to limit the fault current. The converter successfully blocked the fault current as explained in the theoretical analysis and the simulation studies. The results captured from the different experiments prove the validity of the concept proposed in this work.

9.2 Author's contributions

The achievements of the presented work are summarized in the following points:

- A new multilevel converter topology (qZS-MMC) has been proposed with the aim to provide voltage-boost function in addition to the voltage-buck function.
- Two carrier-based modulation techniques (SS and RICs) have been designed to effectively provide a proper operation for the converter and the two techniques have been compared with each other.
- DC-fault blocking capability of the proposed converter has been investigated.
- A comparison between the proposed converter, the full-bridge based MMC and the qZS-CMI has been presented. The comparison was in terms of, 1) the number of active and passive components, 2) voltage and current stresses, 3) semiconductor losses, and 4) output voltage waveform quality.
- It has been demonstrated that the proposed converter reduces the number of required active switches to be 75 % or 87.5% (depending on the used modulation technique) of that required for the FB-MMC and also it reduces the number of required isolated DC sources and passive components when it is compared with the qZS-CMI.

- Loss estimation procedure has been presented for the proposed converter with the proposed modulation techniques and also for the FB-MMC and the qZS-CMI.
- Guidelines for sizing different passive components have been developed under the proposed modulation techniques.
- Simulation studies have been performed to validate the performance of the proposed novel converter.
- A laboratory prototype has been designed and built.
- Experimental tests of the novel converter have effectively been performed.
- DC side fault blocking capability of the converter has been experimentally validated.

9.3 Future work

The work presented in this thesis can be considered as a first step toward integrating impedance networks to the modular multilevel converters. More work is required to further investigate this integration and to achieve full implementation of this converter topology. Some of areas where the future work can be directed are listed as:

- The investigation of other impedance networks will be studied in detail. As the qZS-network has received an increasing attention with the multilevel converters due to drawing continuous source current and reducing voltage rating for one of the network capacitors compared with traditional Z-source network, the qZS-network has been integrated with the MMC in this project. Other impedance networks need to be integrated and compared with the used one to optimize the converter size, losses … etc. This point has been initiated by integrating the Z-source network with the MMC. The initial proposed Z-source MMC reduces the required number of inductors and their size compared to the proposed qZS-MMC. This work has been analysed and simulated and as illustrated in [129]. Further work for this point can be directed to the three-phase implementation using hybrid sub-modules.

- The three-phase converter will be investigated and implemented with the feasible control strategy, and consequently the converter performance under unbalanced AC load and the corresponding control strategy can be analysed.
- Other multilevel modulation techniques such as, phase-shift carrier-based technique and space vector PWM with the concept of RICs will be analysed. This may result in improving the converter performance.
- The converter dynamics should be analysed in detail to investigate the converter variables interaction.
- The implementation of the proposed converter to the wind turbine system and feasible control strategy will be researched.
- The converter ability to block DC-faults has been considered in this project. Therefore, the performance of the proposed converter under AC fault conditions is an interesting point to be investigated in future work.
- The integration of the qZS with the hybrid MMC will need further study such as partial shoot-through concept can be studied which may reduce the switching losses for the converter.

9.4 List of publications

The following three international conference papers and two journal papers related to the research presented in this thesis have been peer reviewed and published. Also, one journal paper is currently under review.

1. F. A. Khera, C. Klumpner and P. Wheeler, "Experimental Validation of a quasi Z-Source Modular Multilevel Converter with DC Fault Blocking Capability," in IEEE Journal of Emerging and Selected Topics in Power Electronics, vol. 9, no. 2, pp. 1951-1965, April 2021, doi: 10.1109/JESTPE.2019.2955859.

2. F. A. Khera, C. Klumpner and P. W. Wheeler, "New modulation scheme for bidirectional qZS modular multi-level converters," in The Journal of Engineering, vol. 2019, no. 17, pp. 3836-3841, 2019, doi: 0.1049/joe.2018.8020.

3. F. A. Khera, C. Klumpner and P. W. Wheeler, "Integrating a Single Z-Source Network with a Modular Multilevel Converter for Voltage Boosting," 2019 IEEE 15th Brazilian Power Electronics Conference and 5th IEEE Southern Power Electronics Conference (COBEP/SPEC), Santos, Brazil, 2019.

4. F. A. Khera, C. Klumpner, and P. W. Wheeler, "A Comparison of Modulation Techniques for Three-phase quasi Z-Source Modular Multilevel Converter Able to Provide DC-link Fault Blocking Capability," in 2018 20th European Conference on Power Electronics and Applications (EPE'18 ECCE Europe), 2018

5. F. A. Khera, C. Klumpner, and P. W. Wheeler, "Operation Principles of Quasi Z-Source Modular Multilevel Converters" In 2017 IEEE 3rd Annual Southern Power Electronics Conference (SPEC), 2017.

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Appendix A

Fourier series of upper and lower DC-link and arm voltage

A.1 DC-link voltage

The upper and the lower DC-link voltage waveforms, which are illustrated in Fig. A.1, have two voltage components which are a DC voltage component and an AC fundamental frequency component.

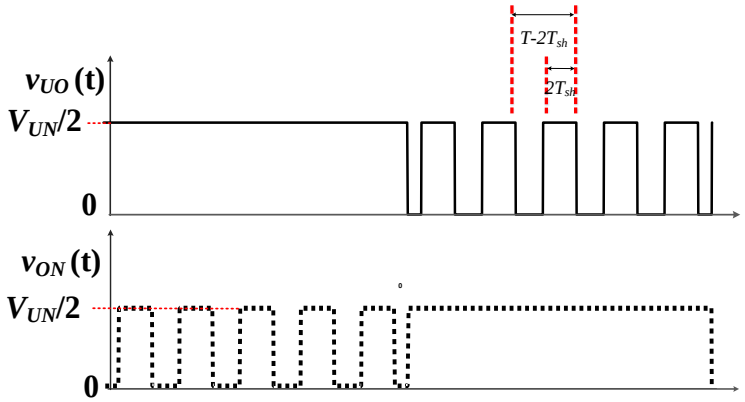


Fig. A.1: The upper and the lower DC-link voltage waveforms when using RICs modulation technique

It is noted that, one half cycle has a constant voltage value at $V_{UN}/2$, while the other half is a pulsated voltage that can be approximated to its average value, which is equal to $(1\text{-}2D_{sh})$ * $V_{UN}/2$. Therefore, the waveforms can be

approximated to square wave and the DC voltage components can be calculated by (A.1).

$$\begin{aligned} v_{UO}(DC) = v_{ON}(DC) = \\ &= \frac{1}{2\pi}\left[\pi \cdot \frac{V_{UN}}{2} + \pi \cdot \frac{V_{UN}}{2} \cdot (1 - 2 \cdot D_{sh})\right] \\ &= \frac{V_{UN}}{2} \cdot (1 - D_{sh}) \end{aligned} \quad \text{(A.1)}$$

Due to an equal width of the pulses, the fundamental component can be calculated using Fourier formulas of the square waveform.

$$\begin{aligned} v_{UO} &= \frac{4}{\pi} \cdot D_{sh} \cdot \frac{V_{UN}}{2} . \sin \omega \cdot t \\ v_{ON} &= -\frac{4}{\pi} \cdot D_{sh} \cdot \frac{V_{UN}}{2} . \sin \omega \cdot t \end{aligned} \quad \text{(A.2)}$$

From (A.1) and (A.2), the upper and the lower DC-link voltages are given by:

$$\begin{aligned} v_{UO} &= (1 - D_{sh}) \cdot \frac{V_{UN}}{2} + \frac{4 \cdot D_{sh}}{\pi} \cdot \frac{V_{UN}}{2} \cdot \sin \omega \cdot t \\ v_{ON} &= (1 - D_{sh}) \cdot \frac{V_{UN}}{2} - \frac{4 \cdot D_{sh}}{\pi} \cdot \frac{V_{UN}}{2} \cdot \sin \omega \cdot t \end{aligned} \quad \text{(A.3)}$$

A.2 Arm voltage

The modified modulating signal for the upper arm, shown in Fig. A.2a, consists of two components which are the original modulating signal shown in Fig. A.2b and the compensating signal shown in Fig. A.2c. Fig. A.3 shows the lower arm modified modulating signal, the original modulating signal and the compensating signal. The upper and lower arm original modulating signals can be expressed by:

$$\begin{aligned} v_U &= \frac{V_{UN}}{2} - V_m \cdot \sin \omega t \\ v_N &= \frac{V_{UN}}{2} + V_m \cdot \sin \omega t \end{aligned} \quad \text{(A.4)}$$

where $V_m = m \cdot V_{UN} / 2$, and m is the converter modulation index. By using Fourier Transformation, the compensating signals for the upper and the lower arms consist of a DC voltage component and an AC fundamental component which are given by (A.5) and (A.6) respectively.

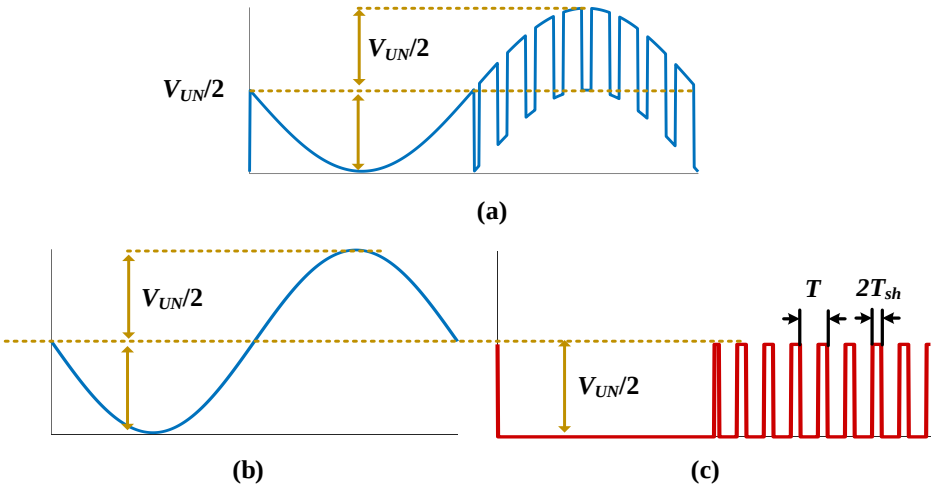


Fig. A.2: Upper arm modulating signal a) modified modulation signal, b) original modulation signal, and c) compensating signal

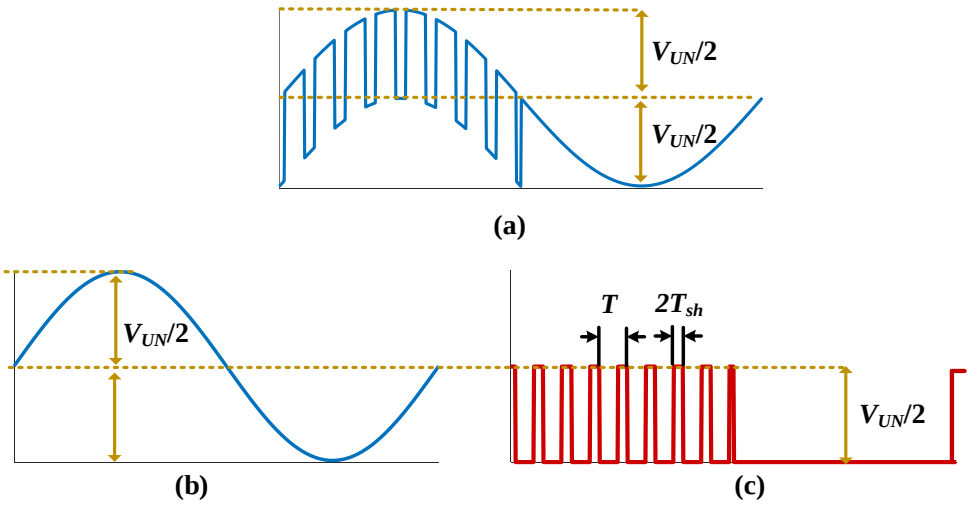


Fig. A.3: Lower arm modulating signal a) modified modulation signal, b) original modulation signal, and c) compensating signal

$$v_{DC} = D_{sh} \cdot \frac{V_{UN}}{2} \tag{A.5}$$

$$\begin{aligned} v_{Fund-up} &= -\frac{4 \cdot D_{sh}}{\pi} \cdot \frac{V_{UN}}{2} . \sin \omega \cdot t \\ v_{Fund-low} &= \frac{4 \cdot D_{sh}}{\pi} \cdot \frac{V_{UN}}{2} . \sin \omega \cdot t \end{aligned} \tag{A.6}$$

Using (A.5) and (A.6), the upper and the lower arm compensating signals are given by:

$$\begin{aligned} v_{Comp-Up} &= D_{sh} \cdot \frac{V_{UN}}{2} - \frac{4 \cdot D_{sh}}{\pi} \cdot \frac{V_{UN}}{2} . \sin \omega \cdot t \\ v_{Comp-Low} &= D_{sh} \cdot \frac{V_{UN}}{2} + \frac{4 \cdot D_{sh}}{\pi} \cdot \frac{V_{UN}}{2} . \sin \omega \cdot t \end{aligned} \tag{A.7}$$

Subtracting the compensating signals (A.7) from the original modulating signals given in (A.4), the modified modulating signals for both the upper and the lower arms are given by:

$$\begin{aligned} v_U &= \left(1 - D_{sh}\right) \cdot \frac{V_{UN}}{2} - (m - \frac{4 \cdot D_{sh}}{\pi}) \cdot \frac{V_{UN}}{2} \cdot \sin \omega \cdot t \\ v_N &= \left(1 - D_{sh}\right) \cdot \frac{V_{UN}}{2} + (m - \frac{4 \cdot D_{sh}}{\pi}) \cdot \frac{V_{UN}}{2} \cdot \sin \omega \cdot t \end{aligned} \tag{A.8}$$

Appendix B

Characteristics of the IGBT module used in the theoretical analysis

Fig. B.1 and Fig. B.2 show the conduction and switching characteristics of the IGBT and diode in the MITSUBISHI CM800HA-66A module [115]. The conduction loss of the IGBT from Fig. B.1a, the conduction loss of the diode from Fig. B.1b, and switching loss energy (the turn on, off and reverse recovery) from Fig. B.2 are the curves which need to be transferred to formulas utilizing a curve fitting method. Values of IGBT voltage drop are given in Fig. B.1a which are based on the V_{GE} = 15 V, T_j = 25^o C curve. Therefore, the diode voltage drop values are selected based on the T_j = 25^o C curve. The results of the curve fitting are given, and the conduction loss formulas are:

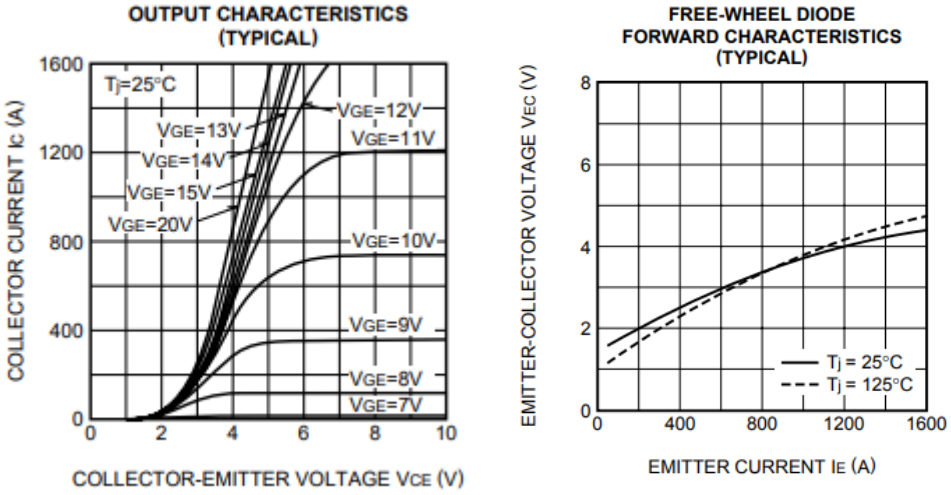
$$\begin{aligned} P_{C-diode}(i) &= |i| \times \left(-85 \times 10^{-8} |i|^2 + 0.0032 \times |i| + 1.4 \right) \\ P_{C-IGBT}(i) &= |i| \times \left(-75 \times 10^{-8} |i|^2 + 0.0032 \times |i| + 2.4 \right) \end{aligned} \tag{B.1}$$

The switching energy loss formulas are:

$$e_{on}(i) = \left(93\times10^{-8}\,|i|^2 + 0.0011\times|i| + 0.13\right)$$

$$e_{off}(i) = \left(77\times10^{-9}\,|i|^2 + 0.00079\times|i| + 0.12\right) \qquad \text{(B.2)}$$

$$e_{rec}(i) = \left(8.3\times10^{-10}\,|i|^3 - 1.3\times10^{-6}\,|i|^2 + 0.0007\times|i| + 0.12\right)$$



(a) (b)

Fig. B.1: MITSUBISHI CM800HA-66A module characteristic from the datasheet: a) IGBT output characteristics, and b) Diode forward characteristics

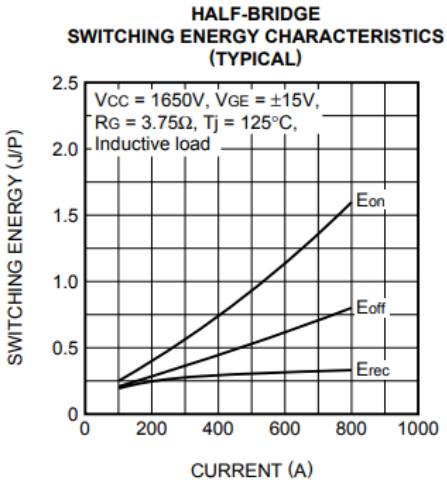


Fig. B.2: MITSUBISHI CM800HA-66A module switching energy characteristics

Appendix C

FB-MMC and qZS-CMI Losses Evaluation

A. MMC based FBSMs (FB-MMC)

The configuration of the FB-MMC is shown in Fig. C.1. The switching states of the FBSM are summarized in Table C.1 according to the current direction and the SM output voltage.

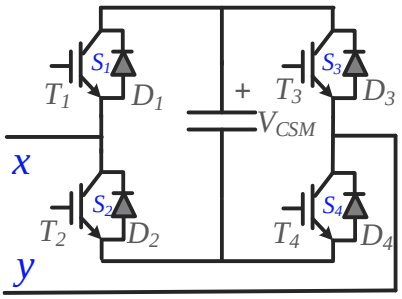


Fig. C.1: FBSM configuration

Table C.1: Switching states of FBSMs

state	Conducting devices					Conducting switches (Diodes, IGBTs)	
	S_1	S_2	S_3	S_4	V_{XY}	(+) $X \rightarrow Y$	(-) $Y \rightarrow X$
1	1	0	0	1	V_{CSM}	D_1, D_4	T_1, T_4
2	1	0	1	0	0	D_1, T_3	T_1, D_3
3	0	1	0	1	0	T_2, D_4	D_2, T_4
4	0	1	1	0	$-V_{CSM}$	T_2, T_3	D_2, D_3

1. Conduction losses

From Table C.1, the number and the type of the conducting devices can be seen based on the arm current direction and arm voltage sign. The instantaneous conduction loss can be expressed as:

$$P_{C-arm}(t) = \tag{C.1}$$

$$\begin{cases} 2N_U^{FB}(t) \times P_{C-diode}\left(i_{UA}(t)\right) + \\ +\left[N_{SM} - N_U^{FB}(t)\right] \times \left[P_{C-IGBT}\left(i_{UA}(t)\right) + P_{C-diode}\left(i_{UA}(t)\right)\right] \\ \qquad @ \quad i_{UA}(t) \times v_{UA}(t) \geq 0 \\ 2N_U^{FB}(t) \times P_{C-IGBT}\left(i_{UA}(t)\right) + \\ +\left[N_{SM} - N_U^{FB}(t)\right] \times \left[P_{C-IGBT}\left(i_{UA}(t)\right) + P_{C-diode}\left(i_{UA}(t)\right)\right] \\ \qquad @ \quad i_{UA}(t) \times v_{UA}(t) < 0 \end{cases}$$

where $N_U^{FB}(t)$ is the number of inserted SMs in each arm.

2. Switching losses

As a result of implementing PD-PWM technique for the MMC based on FBSMs [95], only one SM is inserted, and another/same SM is bypassed during a carrier frequency f_c cycle. Based on Table C.1, considering the SM is switched from state 1 to state 2 and the arm current has a positive polarity, D_4 is turned off and the T_3 is turned on leading to e_{on} and e_{rec} energy for the IGBT and the diode respectively. During the same frequency cycle, the same/another SM is switched from state 2 to state 1 and the arm current still has a positive polarity, D_4 is turned on and T_3 is turned off leading to e_{off} energy for the IGBT. Therefore, the arm dissipated switching power loss during a carrier frequency cycle is defined by:

$$P_{SW-fc}(t) = f_c \cdot \left(e_{off}\left(i_{UA}(t)\right) + e_{on}\left(i_{UA}(t)\right) + e_{rec}\left(i_{UA}(t)\right)\right) \times \frac{V_{CSM}}{V_n} \tag{C.2}$$

Similar to the qZS-MMC, the sorting is performed every N_{SM} carrier frequency cycle where the sorting frequency f_{sort} equals to f_c/N_{SM}, the arm dissipated switching power loss due to sorting is defined by:

$$P_{SW-sort}(t) = \tag{C.3}$$

$$\begin{cases} = \left[f_{sort} \cdot N_U(t) \right] \\ \qquad \times \left[e_{off}\left(i_{UA}(t)\right) + e_{on}\left(i_{UA}(t)\right) + e_{rec}\left(i_{UA}(t)\right) \right] \times \dfrac{V_{CSM}}{V_n} \\ \qquad\qquad @ \quad N_U(t) < N_{SM}/2 \\ = \left[f_{sort} \cdot \left(N_{SM} - N_U(t)\right) \right] \\ \qquad \times \left[e_{off}\left(i_{UA}(t)\right) + e_{on}\left(i_{UA}(t)\right) + e_{rec}\left(i_{UA}(t)\right) \right] \times \dfrac{V_{CSM}}{V_n} \\ \qquad\qquad @ \quad N_U(t) \geq N_{SM}/2 \end{cases}$$

The total arm dissipated switching power loss is defined by:

$$P_{SW-arm}(t) = P_{SW-fc}(t) + P_{SW-sort}(t) \tag{C.4}$$

B. qZS cascaded multilevel inverter (qZS-CMI)

The configuration of qZS-CMI is shown in Fig. C.2. The modules can be only modulated using the phase-shift PWM (PS-PWM) technique. According to [65], each module requires two ST reference signals which are represented by a straight line, one of them is equal to the positive peak of the modulating signal and the other is equal to the negative peak. The shoot-through mode is introduced only during the zero-voltage mode of the corresponding module.

The ST duty ratio is defined as a function of modulation index *m* by:

$$D_{sh-CMLI} = 1 - m \tag{C.5}$$

As a result, the peak value of the DC-link voltage at the DC terminals of the module is defined by:

$$V_{AB} = 1/(1-2D_{sh}) \times V_{DC} / N_{SM-CAS} \tag{C.6}$$

The peak of fundamental output phase voltage V_m can be expressed by:

$$V_m = m\ N_{SM-CAS} V_{UN} = m\ /(1-2D_{sh}) \times V_{DC} = GV_{DC} \tag{C.7}$$

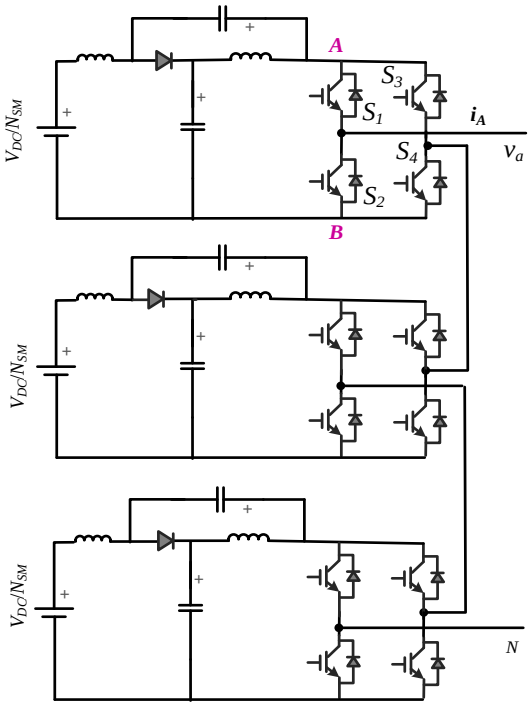


Fig. C.2: Phase-a seven-level cascaded H-bridge converter

1. Conduction losses

The shoot-through mode can be introduced by turning on all switches of the corresponding module. Therefore, each switch of the module holds on the load current during its NST mode (active or zero states). In addition, during the ST mode, each switch of the module holds the ST current, which equals to half of

the summation of the two qZS inductor currents $\left(i_{L1}(t)+i_{L2}(t)\right)/2 = I_L$ in each network and half of the load current. The current of the switch S_1 is defined as:

$$i_{S1}(t) = \begin{cases} i_A \times v_{S1} & \rightarrow \text{NST} \\ I_L + i_A/2 & \rightarrow \text{ST} \end{cases} \tag{C.8}$$

where v_{S1} is the pulse signals of switches S_1. The instantaneous conduction losses of S_1 can be expressed as (C.9) and the other switches in this module will be identical.

$$P_C(t) = \begin{cases} P_{c-IGBT}\left(i_{S1}(t)\right) & i_{S1}(t) \geq 0 \\ P_{c-diode}\left(i_{S1}(t)\right); & i_{S1}(t) < 0 \end{cases} \tag{C.9}$$

The current of the qZS diode switch during NST mode is:

$$i_{d-qZS}(t) = 2I_L - i_A(v_{S1} - v_{S3}) \tag{C.10}$$

where v_{S1} and v_{S3} are the pulse signals of the upper switches S_1 and S_3. Using (C.9), the conduction power losses can be estimated.

2. Switching losses

The qZS-CMI can be only modulated using phase-shift PWM (PS-PWM) technique [26]. During the NST mode, the module holds the load current using two switches, one of each leg. Therefore, the load current is used to calculate the dissipated switching energy. During a carrier frequency f_c cycle, there are two transitions for each leg of the module which are: (1) the IGBT turns off and diode turns on and (2) the diode turns off and the IGBT turns on. Therefore, the module dissipated switching power loss is defined by:

$$P_{SW-NST}(t) = 2f_c \cdot \left(e_{off}\left(i_{AO}(t)\right) + e_{on}\left(i_{AO}(t)\right) + e_{rec}\left(i_{AO}(t)\right)\right) \times \frac{V_{AB}}{V_n} \tag{C.11}$$

During the ST mode, the two legs are used to makes short circuit and as a result, the current is equally distributed between the two legs in the ST mode which is

previously defined by (C.8). Since two switches from the module are already on from the previous NST states and they are holding current, only two more switches (IGBTs) are turned on during ST mode and then turned off. Also, the shoot-through mode is introduced twice through the switching frequency f_c cycle. Therefore, the dissipated switching power loss is defined by:

$$P_{SW-ST}(t) = 2 f_c \cdot \left(2 \times e_{off}\left(i_{S1}(t)\right) + 2 \times e_{on}\left(i_{S1}(t)\right)\right) \times \frac{V_{AB}}{V_n} \tag{C.12}$$

The module total dissipated switching power loss is defined by:

$$P_{SW}(t) = P_{SW-NST}(t) + P_{SW-ST}(t) \tag{C.13}$$

During the ST mode, the series diode in any of the qZS networks, that was holding the summation of the two qZS-inductor currents $i_{L1}(t) + i_{L2}(t) = 2I_L$, is turned off. Therefore, the dissipated switching power is a result of switching recovery energy and defined by:

$$P_{SW}(t) = 2 f_c \times \left[e_{rec}\left(2I_L\right)\right] \times \frac{V_{AB}}{V_n} \tag{C.14}$$