A New Modular Multilevel Converter for HVDC Applications

Zain Hassan

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Everything you possess of skill, and wealth, and handicraft, wasn't it first merely a thought and a quest?

- Rumi

Abstract

In the coming years, due to an increasing shift towards electric mobility and further industrialisation, a rapid growth in the demand for electricity is expected. At the same time, this energy demand must be met in a clean and sustainable manner, to reduce climate change as well as to ensure security of supply. It is predicted that the High Voltage Direct Current (HVDC) transmission technology will play a key role in the future power systems which are expected to feature higher levels of interconnection and more renewable-based generation. HVDC transmission is preferred over AC transmission in applications such as power transmission over long distances and from offshore wind sources, and interconnection of asynchronous systems. The main elements of an HVDC system are the AC/DC converters that take up the majority of the initial set up cost, and therefore, there has been a huge focus lately on improving these converters in terms of functionality, cost and efficiency.

Today, the state-of-the-art converter topology for Voltage Source Converters (VSC) based HVDC transmission is the Modular Multilevel Converter (MMC), which replaced the earlier two- and three-level VSC topologies. Recently, a new breed of VSC converters, known as the 'hybrid VSCs' are introduced, that combine the aspects of two- and three-level VSCs with the modular multilevel structure of the MMC.

In this work, a new hybrid VSC, the Switched Mid-Point Converter (SMPC), has been proposed. While maintaining the same efficiency as the MMC, the energy storage requirement of the SMPC is shown to be less than half of that of the MMC. The operating principle and the particular voltage waveshaping of the chainlinks of the submodules is investigated. For effective operation of the SMPC, suitable control strategies are proposed. The converter concept and the developed control schemes are verified both using computer simulations and a lab-scaled experimental prototype.

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Chapter 1

Introduction

1.1 Background

The idea of using direct current (DC) for electric power transmission dates back to the late nineteenth century when the world's first DC transmission system was built in 1882 by Thomas Edison. Around the same time, George Westinghouse joined with Nikola Tesla and developed what he believed was a safer and better way of generating and transmitting electricity on a larger scale: alternating current (AC). What followed was a fierce competition between the two that history remembers as the "war of the currents", eventually won by Westinghouse on account of the performance advantages of transformers and induction motors. AC transmission became the standard and has since dominated the electric power industry.

However, DC transmission enjoyed a revival after the development of mercury arc valves in the 1930s. Dr Uno Lamm of ASEA, regarded as the "father of HVDC", led the efforts to incorporate the mercury arc technology into a manufacturable converter valve. After two decades of development when the converter technology was close to being commercially feasible, ASEA acquired the first commercial order for a HVDC system based on sub-sea cables from Vattenfall in 1950. This HVDC link, finally commissioned in 1954, was designed to transmit 20 MW of power between Sweden

and Gotland at a DC voltage of 100 kV.

In the later half of the twentieth century, the prospects of HVDC becoming an integral part of the transmission system flourished with the advancement in power semiconductor technology. The thyristor was invented in the 1950s and in 1970, ASEA made the first commercial use of thyristor-based converters, adding 10 MW of power to the existing Gotland link. Owing to the high current-carrying capability of thyristors, thyristor-based HVDC technology found applications in bulk power transfer at high voltages over long distances. In the 1980s, another significant breakthrough in the field of power semiconductors led to the invention of Insulated Gate Bipolar Transistors (IGBTs). In the field of HVDC, the IGBTs were first utilised in ABB's (formerly ASEA) HVDC Light Technology, and the first commercial project was the 50 MW sub-sea HVDC link between the southern and northern parts of the Gotland island, put into operation in 1999.

Today, HVDC is a significantly mature technology and there are well over 200 HVDC links in operation worldwide. Although AC technology still dominates the transmission industry, HVDC has gained a central role in the future energy scenario. In recent years, the global drive towards decarbonisation has motivated a paradigm shift from dependence on fossil-fuel-based power generation to cleaner and more sustainable renewable energy sources. Consequently, the power system industry also has to undergo radical changes to improve power generation and transmission technologies and to ensure smooth integration of renewable-based power.

From a power transmission point of view, the impact of the aforementioned energy revolution is that HVDC systems are being increasingly preferred over AC transmission for a variety of applications, such as offshore wind and continent-wide grid interconnection. Generally, HVDC has a higher set up cost due to expensive converter stations but the line costs in HVDC are lower compared to those in AC. This is because HVDC transmission uses two power-carrying conductors for transferring the same amount of power for which an AC transmission system needs three for

three phases [6]. Moreover, in AC transmission, the reactance of the line increases with length, causing it to consume more reactive power, and thus puts limits on the transmission length. On the other hand, a DC line has no reactance and hence there are no limits on the transmission distance [6]. The break-even distance, after which HVDC transmission becomes cheaper than AC transmission, in case of overhead DC lines ranges between 500 km and 800 km depending on factors such as cost of right of way and other country-specific costs [7]. In addition to cost benefits, a HVDC system allows better regulation of power flow and can be connected in a back-to-back configuration to interconnect two asynchronous AC networks, achieving a more reliable overall grid operation.

In the present era, HVDC transmission systems are classified into two major technologies: the Line Commutated Converters (LCC) that are formed using thyristors, and the Voltage Source Converters (VSC) that are mainly based on IGBTs. LCC systems can easily reach very high power ratings due to high current ratings of thyristors, and hence, are the technology of choice for bulk power transmission over long distances. The drawbacks associated with LCCs are high reactive power compensation requirement, large AC harmonic filters and dependence on AC system strength. In comparison, the VSC technology employs self-commutated devices, such as IGBTs, and hence, the output voltage of the VSCs can be fully controlled. This allows an independent regulation of the active and reactive power, thereby overcoming the drawbacks of the LCC systems. VSC technology has applications in offshore wind connections and in the overlay DC grids of the future.

The earliest VSC topology is the two-level converter, which has the drawback of higher semiconductor losses compared to LCCs. Multilevel VSCs were then introduced which offer better harmonic performance and lower $\mathrm{d}v/\mathrm{d}t$, as a result of their ability to produce multiple output levels. Some of the prominent multilevel topologies are the Neutral (and Active Neutral) Point Clamped Converter, Flying Capacitor Converter and the Cascaded Full-Bridge Converter.

Although some of the multilevel VSC topologies are modular, their structural complexity increases with the number of output levels. The first truly modular converter for HVDC applications is the Modular Multilevel Converter (MMC), introduced in 2001. In addition to modularity, the MMC also features low switching losses, low $\mathrm{d}v/\mathrm{d}t$ and high quality output waveforms. As a result, the MMC is a significant improvement compared to the earlier two-level and multilevel VSCs, and is being commercially employed by all major HVDC vendors. The conventional MMC is based on the series connection of half-bridge submodules, which renders it incapable of handling DC side faults. Several alternative submodule configurations have been proposed for the MMC to enable DC fault blocking at the expense of higher losses, notably the full-bridge submodule, the clamped-double submodule and the hybrid MMC that employs both half-bridge and full-bridge submodules, and is a variant of the original MMC.

The latest breed of VSC converters are the hybrid VSCs that combine the features of the earlier two- and three- level converters with modular multilevel converters. Hybrid VSCs offer different benefits over the MMC, such as DC fault blocking without sacrificing efficiency, lesser number of submodules with smaller capacitors, and a lower volume and footprint for the converter station. The most prominent hybrid VSC topologies are the Alternate Arm Converter, the Hybrid Multilevel Converter with AC-side cascaded H-bridges, the Parallel Hybrid Modular Multilevel Converter and the Series Bridge Converter. Hybrid VSCs are attractive substitutes to the MMC in space-constrained applications and in applications where DC fault blocking is required. This has led to an increased research interest in various aspects of the hybrid VSC topologies in the last few years. The efforts are also directed towards the introduction of a hybrid VSC topology that can challenge the MMC as the state-of-the-art for HVDC, and forms the next generation of commercial VSC converters.

1.2 Project Objectives

In continuation of the previous research efforts on hybrid VSCs, this research work introduces a novel hybrid VSC topology, titled as 'the Switched Mid-Point Converter' (SMPC) for HVDC applications. Prior to arriving at the main topology in this thesis, two intermediate topologies, that paved the way for the main topology, are also conceptualised and theoretically discussed. These intermediate topologies are titled as 'the Parallel H-Bridge Converter' (PHBC) and 'the Parallel Connected multilevel converter with Unfolding Bridges' (PCUB).

The main objectives of this project are to:

- review different VSC topologies, especially focusing on the modular multilevel converter (MMC) and hybrid VSCs
- formulate the concepts of the PHBC and the PCUB, identify the drawbacks of both topologies, and propose structural changes
- derive the SMPC topology and perform an in-depth analysis of its operation
- perform a detailed comparative analysis between the SMPC and the MMC for given system ratings
- develop a control strategy to ensure the correct operation of the SMPC
- verify the proposed control strategy through a switching simulation model
- validate the converter operation practically using a three-phase lab-scaled experimental prototype

1.3 Thesis Outline

The outline of the thesis is as follows.

Chapter 2 provides an overview of the HVDC technology, its applications and future scope. In addition, the various converter topologies are presented, with an emphasis on the recent modular multilevel and hybrid VSC converters.

Chapter 3 investigates the two intermediate topologies i.e. the PHBC and the PCUB. The discussion on the topologies presented in this chapter is mainly theoretical, allowing more focus on the structural aspects of the topologies and their drawbacks. It is shown that the main topology of this thesis, the SMPC, is derived by restructuring the PCUB topology.

Chapter 4 introduces the SMPC. The operating principle of the topology, along with the basic wave-shaping of its chainlink voltages, is described in detail. Utilising the mathematical expressions for chainlink voltages and currents, the issue of arm energy management is investigated in depth. As a solution to the energy management problem, a method for balancing the arm energies based on second harmonic injection is proposed. After that, sizing of different parameters in the SMPC is evaluated, followed by a method for optimising the modulation index of the converter. An analysis on the challenges associated with the use of hybrid chainlinks (formed using two types of cells) in the SMPC is also included. As is important with novel VSC modular multilevel converters, a detailed comparison of the SMPC with the MMC is presented. Lastly, the performance of the SMPC under AC and DC fault conditions is theoretically discussed.

Chapter 5 focuses on the control strategy development and simulation modelling of the SMPC. First, the overall control scheme is described, and then the design of the individual control loops is explained in detail. Furthermore, the implementation of the final wave-shaping and the modulation scheme is also addressed. Finally, results from a switching simulation model of the SMPC are presented for different operating conditions to verify the proposed wave-shaping and the control scheme.

Chapter 6 covers a brief description of the experimental prototype used for practical

validation of the SMPC. Different aspects related to both the hardware design and the software implementation are included.

Chapter 7 presents the results obtained from the experimental work. The converter operation described in Chapter 4 and the devised control scheme in Chapter 5 are practically validated for the down-scaled ratings of the prototype.

Chapter 8 summarises the main conclusions of the thesis and suggests ideas for future work.

1.4 Contributions of the thesis work

The original contributions of this thesis include:

- An investigation of the operating principles and limitations of the PHBC and the PCUB i.e. two new voltage-source converters for HVDC
- The conceptualisation, definition of the operating principle and wave-shaping selection of the SMPC i.e. a novel voltage-source converter for HVDC, considered as the "main" topology of this thesis
- The formulation of the mathematical basis for the energy management problem of the SMPC, along with a proposed solution
- A comparative analysis of the SMPC against the MMC in terms of energy storage, number of submodules, capacitor size and converter losses
- A proposed technique for DC current ripple removal in the SMPC during AC single-phase fault conditions
- The development of the control strategy for the SMPC as well as the simulation and experimental validation of the control scheme and the SMPC converter operation

Chapter 2

Literature review

2.1 Introduction

HVDC transmission is a key enabling technology for the large-scale integration of renewables and for the pan-continental DC grids of the future. Although its central role in the energy scenario has been acknowledged fairly recently, HVDC systems have existed since the 1950s. Pioneering development of the HVDC technology took place with the invention of the mercury arc valves and the first commercial HVDC transmission link was commissioned between Gotland and the Swedish mainland in 1954. More than sixty years on, HVDC technology has significantly matured and its evolution has been closely linked with the advancement of semiconductor power devices. With the advent of thyristors in 1950s and IGBTs in 1980s, the two major HVDC technologies, the Line Commutated Converter HVDC (LCC-HVDC) and the Voltage-Source Converter HVDC (VSC-HVDC), emerged that have enabled HVDC to become a vital part of the existing transmission system.

In this chapter, the applications and future scope of HVDC are initially discussed, and then a detailed review of the converter topologies for HVDC are presented. The basic operation and configurations of both LCC and VSC converters are first discussed

along with a comparison between the two technologies. This is followed by an in-depth review of both the conventional two-level and multilevel VSC topologies and the contemporary modular multilevel converter (MMC) and hybrid VSC topologies.

2.2 HVDC: Applications and Future Scope

HVDC is a system that uses power electronics technology to convert electrical power from AC to DC at the sending end and from DC to AC at the receiving end, thereby interconnecting two AC systems. On the DC network, the power can either be transmitted over long distances using overhead lines or subsea cables, or both the sending-end and the receiving-end converters may be located at the same site, resulting in a back-to-back HVDC scheme. These HVDC schemes are depicted in Figure (2.1).

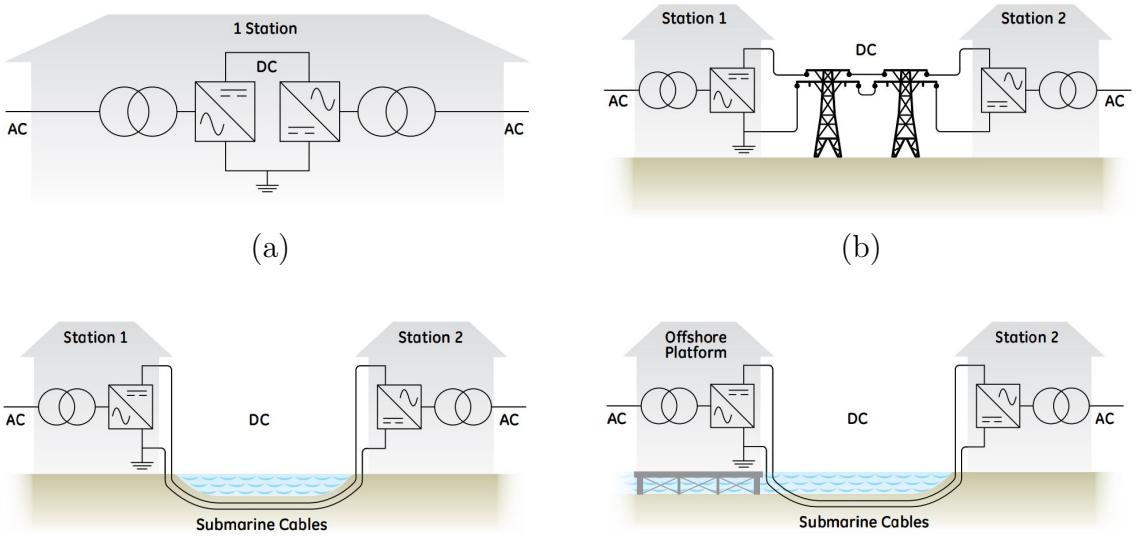


Figure 2.1: Possible HVDC schemes [1] (a) Back-to-back HVDC (b) Bulk power transmission using overhead lines (c) Bulk power transmission using subsea cables (d) Bulk power transmission from offshore platform to on-shore grid

A back-to-back HVDC scheme is suitable for interconnecting two adjacent and asynchronous AC systems without applying any operational restrictions to either system

[8]. Even in cases where the two AC networks operate at the same frequency, a back-to-back HVDC interconnection is preferred over an AC interconnection to improve system flexibility and to limit the spread of cascading faults [8] [1]. Examples of this are back-to-back HVDC connections in North America and India in which both terminals of the scheme are located on the same site [8].

HVDC schemes with overhead lines provide economical means of transmitting bulk power over long distances on land. DC lines have lower losses than AC lines and do not carry reactive power and hence much longer transmission distances can be achieved [9]. In addition, only two conductors are required in a DC line compared to three in an AC line which leads to smaller right-of-way requirements and a reduction in the environmental impact [10]. A good example of this type of HVDC scheme is the Madeira HVDC link in Brazil which is the longest HVDC transmission line at 2,386 km and transports hydropower resources of the Amazon River basin into the Sao Paulo region [11].

HVDC schemes with subsea cables are useful for providing interconnections where power transmission crosses water and in particular, transporting power from offshore wind farms to the mainland. Long, high power HVDC subsea cables are technically and economically viable, which is not the case for AC cables where the capacitive charging current dominates the cable's overall current carrying capability. Several examples of interconnections between countries across the Baltic Sea utilise HVDC schemes with subsea cables e.g. Estlink (between Estonia and Finland) and NordBalt (between Sweden and Lithuania) [12]. Also, several HVDC schemes transporting offshore wind power to the mainland are operational in the UK and Europe e.g. Hornsea, Borwin and DoggerBank, amongst others.

The discussion above has outlined the existing application areas of HVDC, in which numerous commercial installations are successfully operational, which are:

- Bulk power transmission over long distances

- Interconnection of asynchronous systems
- Sub-sea connections and power transmission from offshore wind farms

All the HVDC schemes in the aforementioned application areas are point-to-point (P2P) schemes. With a huge increase in the number of P2P HVDC links, it becomes possible to interconnect them to form DC grids [13]. An overlay DC grid, such as the future "supergrid" in Europe, is seen as a promising solution for integrating massive amounts of renewables and to ensure security of energy supply [14].

Recently, there has been significant interest in the interconnection of P2P HVDC links driven by the need for DC grid development. As compared to the traditional P2P connection, a meshed DC grid provides multiple inter-connection paths between two converter terminals [15]. This leads to security of power transfer since a trip on a single DC line may not affect the power flow between two DC grid terminals. Other benefits achieved with DC grids are operational flexibility and enhanced power trading [16]. Furthermore, the variability of renewable sources can be reduced as the weather systems at different renewable energy sites have limited correlation [14].

Several technical challenges need to be overcome before the vision of DC grids can become a reality. Suitable DC protection technology will be required to isolate the faulty lines allowing power flow on the rest of the grid [16]. DC grid control is challenging as the dynamics are faster than those of AC systems and there is an absence of inertia. Moreover, multiple manufacturers will be involved in the development of DC grids and hence a regulatory framework and standard DC grid codes have to be developed to ensure interoperability.

2.3 HVDC converters

The two distinct HVDC converter technologies are the Line-Commutated Converter (LCC) HVDC and the Voltage Source Converter (VSC) HVDC. LCC-HVDC has

applications in bulk power transfer over long distances whereas VSC-HVDC is a more recent development and has applications in offshore wind connections and the future DC grids. In the following sections, a brief overview of the two technologies is presented along with a comparison between them.

2.3.1 Line Commutated Converters

Line-commutated converter (LCC) HVDC is built using thyristors and is a well-established technology. It has been in use since the 1950s for long-distance bulk-power transmission and for back-to-back connection of asynchronous systems.

The thyristor is a semiconductor device in which the start of the conduction can be controlled by a firing pulse, but the end of the conduction occurs when the current passes through zero. A thyristor press-pack package manufactured by ABB is shown in Figure (2.2). They have high power ratings and are very efficient. Single devices can have up to 8500 V, 4500 A capability and in order to reach the high voltages in an HVDC system, several thyristors are connected in series to form an equivalent "valve".

Figure 2.2: Press-pack thyristor package (Source: ABB)

The basic circuit of a LCC-HVDC connection with thyristors is a six-pulse thyristor bridge connected to an AC system via a converter transformer as shown in Figure (2.3) [17]. The DC voltage has a six-pulse ripple and hence, DC reactors are used to smooth the DC current. They also serve as buffers between the converters and the

DC line [18]. In addition, LCCs generate AC harmonics and AC filters are shunt-connected to provide low impedance paths for harmonic currents [18].

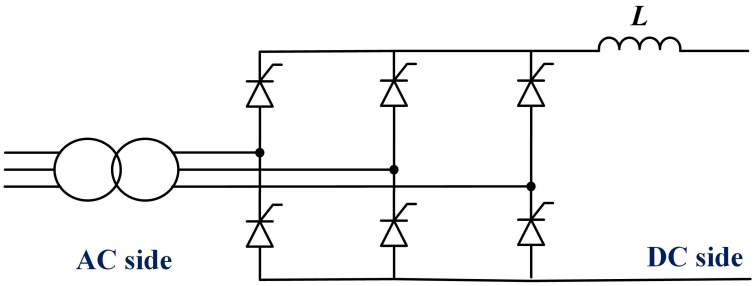


Figure 2.3: LCC converter based on six-pulse thyristor bridge

In order to reduce some of the low-order harmonics and to achieve higher ratings, two six-pulse bridges can be series connected on the DC side through separate 30° phase-shifted transformers on the AC side. This results in the 12-pulse thyristor bridge converter configuration as depicted in Figure (2.4) which is employed in most of the commercial LCC-HVDC systems [19]. The transformer arrangement for the desired phase-shift is Y-Δ on one bridge and Y-Y on the other bridge and the 5th, 7th, 17th and 19th harmonics are cancelled out on the AC network [18].

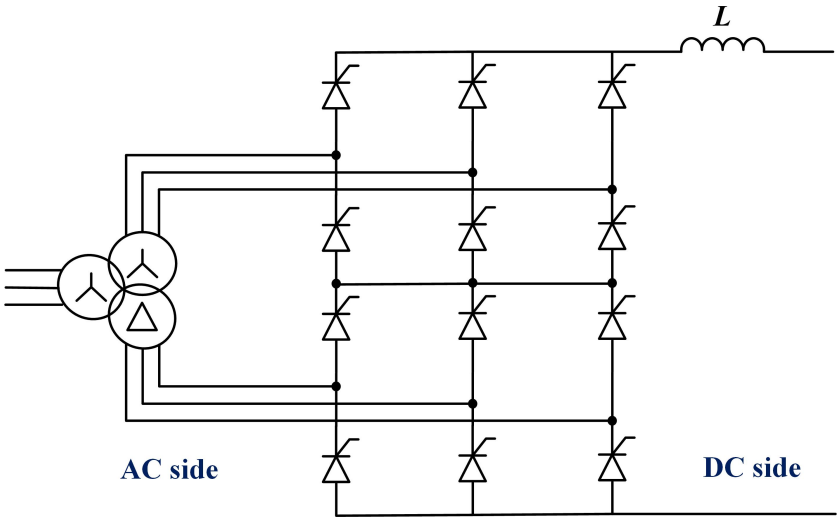
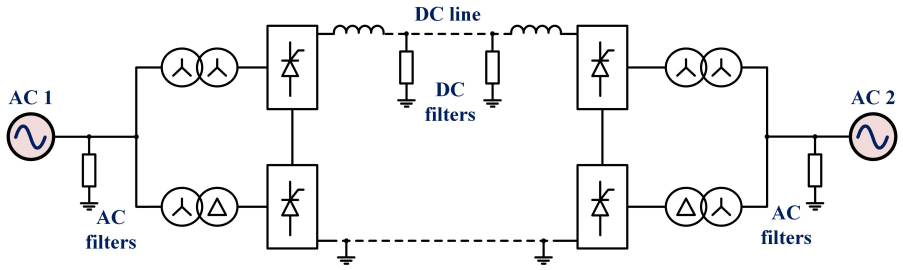


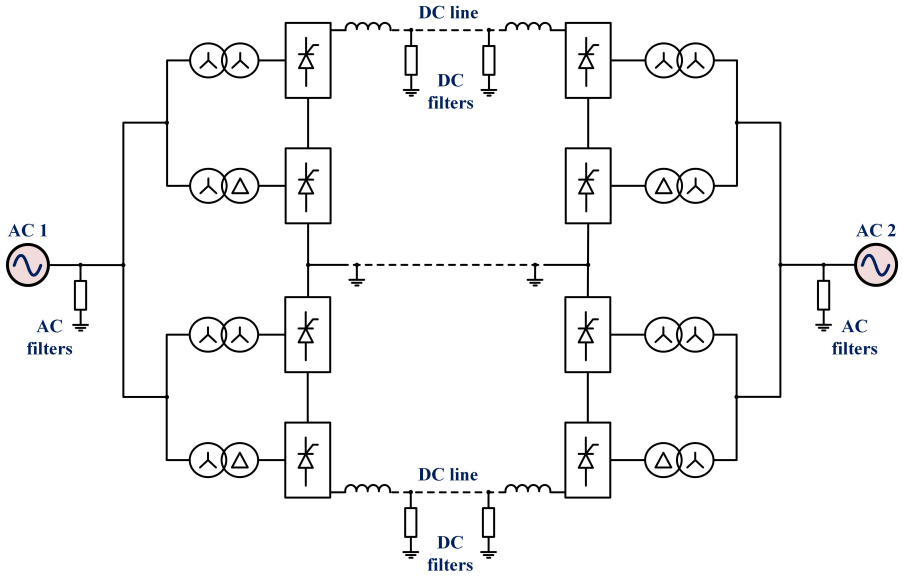
Figure 2.4: LCC converter based on twelve-pulse thyristor bridge

The possible configurations for HVDC systems are monopolar links and bi-polar links, shown in Figure (2.5). Monopolar HVDC systems consist of one or more 12-pulse

converter units at each end and a single conductor at a high DC voltage. The return path can either be through the ground, seawater or a metallic return wire. Bipolar HVDC systems, which are the most common configuration for HVDC connections, have two poles and two converters of equal rating. The midpoint of the converters can be grounded on one or both ends. Compared to monopolar systems, bipolar systems require lower voltage ratings for a similar power transfer [18] [17]. Another advantage is that in case of outage of a pole during a fault or maintenance, the system can be continuously operated at half the capacity using the other pole with ground return.



(a)



(b)

Figure 2.5: (a) Monopolar LCC-HVDC system (b) Bipolar LCC-HVDC system

2.3.2 Voltage Source Converters

Voltage Source Converters (VSC) are based mainly on insulated gate bipolar transistors (IGBTs), which are devices that combine the reliability and power handling capacity of BJTs and the controllability of the MOSFETs [17]. IGBTs are fully controllable devices which can be turned on by applying a positive voltage on the gate, and the turn-off can be achieved with either a null or a negative gate voltage. Commercially available IGBT modules have voltage blocking capability of up to 6.5 kV and a current rating of over 2 kA [20]. In HVDC applications, IGBTs are used with an anti-parallel free-wheeling diode to provide bidirectional current flow. A typical IGBT module manufactured by Infineon is shown in Figure 2.6.

Figure 2.6: A typical IGBT module rated at 4.5 kV and 1.2 kA (Source: Infineon [2])

Since the current in a VSC can be switched on and off by controlling the semiconductor switches (mostly IGBTs), there is no dependence on the strength of the AC network for commutation [21] and hence, VSCs offer black-start capability. Because of the fast switching capability of IGBTs, Pulse Width Modulation (PWM) can be used to fully control the amplitude and phase angle, which allows independent regulation of active and reactive power flow.

The most basic VSC circuit is the three-phase two-level VSC, which was commercially applied in the early generations of ABB's HVDC Light technology [22]. Further innovations in VSC-HVDC have led to the introduction of multilevel VSC converters which have more output voltage steps producing a staircase waveform and thereby

reducing the harmonic distortion and filtering requirements. The first multilevel converter was the three-level neutral-point clamped (NPC) converter [23]. In the last decade, modular-type multilevel converters, in which individual module capacitors are distributed throughout the converter, have shown great promise for VSC-HVDC transmission. The capacitors act as discrete voltage sources, each generating a voltage level, which allows production of a nearly sinusoidal AC voltage at the output [24].

The first commercial VSC for HVDC was built in 1997 on the island of Gotland, which was rated at 50 MW, ± 80 kV, and was based on the two-level VSCs. Since then, there has been a steady increase in the voltage and power ratings of VSCs; ratings of up to 2 GW and ± 500 kV are currently available. VSC-HVDC has been the only viable choice for connecting offshore wind, since the LCC-HVDC stations have larger footprints and various outdoor equipment, making them impractical for an offshore installation. The first offshore wind connection using VSC-HVDC was commissioned in 2010 for the Borwin wind farm [17].

2.3.3 Comparison between LCCs and VSCs

Both LCC and VSC technologies are widely used for HVDC applications, with LCC-HVDC being the technology of choice for bulk-power transmission using overhead lines and VSC-HVDC being preferred in offshore wind connections and the future DC grid connections. Since LCCs have been around for more than six decades, they are a reliable and mature technology with less room for innovation. Alternatively, VSCs are a relatively recent technology and although the technology has been used in numerous commercial projects to date, many of its application areas are still being widely researched and developed.

As mentioned before, LCC-HVDC transmission provides a reliable solution for bulk power transmission, owing to the high voltage and current ratings of thyristors. In addition, thyristors have good overcurrent capability and LCC-HVDC systems are

resilient to DC side faults [16]. However, the disadvantages of LCC based HVDC transmission systems which have driven the development of VSCs are [24] [16]:

- LCCs require significant reactive power compensation which is about 50% - 60% of the active power under normal operating conditions. Hence, switched capacitor banks and passive filters are needed on the AC side to supply the reactive power.
- They generate high magnitude low-order harmonics on the AC side which must be removed by the use of large harmonic filters. These harmonic filters, together with reactive power compensation devices, result in large station footprints for LCC HVDC systems. This makes them potentially impractical for use in space-constrained applications like offshore connections.
- Since they are line-commutated, there is a dependence on the AC system "strength". To ensure stable operation, a minimum short circuit ratio (SCR) of the AC system, typically larger than 2, is needed.
- Power flow reversal is achieved by reversing the DC link voltage. This introduces certain limitations such as the low-cost cross-linked polyethylene (XLPE) cables cannot be used.

In comparison, since VSCs are based on forced-commutating switches and are able to synthesise a fully controllable voltage, the active and reactive power can be independently controlled. Therefore, unlike LCC systems, VSC systems not only have no reactive power compensation requirement, but they can also provide voltage support to the local AC network by supplying reactive power. In addition, the PWM switching is at a high frequency (1-2 kHz) [16] and thus, the harmonic filters are at higher frequencies which are much lower in size and cost. The removal of reactive compensation devices, along with smaller harmonic filters, significantly reduces the station footprints of VSC HVDC stations.

Since the commutation of the switches in a VSC system is forced, there is no SCR requirement of the AC network. Thus, VSC-HVDCs can be connected to weak systems where they can contribute to the system stability [24]. VSCs also offer black-start capability, which is the ability to restore power without an external power source [17]. This feature is useful for applications where space is critical as start-up generators are not needed to bring the system online. Furthermore, the power reversal in VSCs is very fast (50-100 ms) [16] and is achieved by only reversing the DC current. Since the DC voltage polarity is constant, VSCs are the preferred option for paralleling on the DC side to develop multiterminal HVDC and DC grids.

On the downside, VSCs are still a more expensive technology than LCCs and the overall semiconductor requirement in VSCs is higher than in LCCs. Moreover, DC short-circuit faults are a serious problem in overhead lines, since during a DC fault, VSCs without DC-fault handling capability behave as an uncontrolled diode bridge which feeds the DC fault from the AC side. The fault is transferred to the AC side potentially resulting in the collapse of the AC voltage [16]. Faults are cleared by tripping the AC breakers and system restoration may take a long time. Because of the absence of a zero-crossing, DC current is difficult to break and hence, DC circuit breakers are complex technologies. In fact, one of the biggest challenges in fully utilising VSCs for future DC grids is the need for very fast and reliable DC circuit breakers [16].

2.4 VSC-HVDC topologies

In this section, a detailed review of VSC converter topologies intended for HVDC transmission applications is presented. Since the development of the basic two-level VSC more than two decades ago, many VSC-HVDC topologies have been introduced, that can be broadly categorised into non-modular VSCs and modular VSCs. A few of these topologies are limited only to literature, while others have found industrial

acceptance and have been used in various commercial VSC projects. The most recent breed of VSCs i.e. hybrid VSCs, that combine the aspects of non-modular and modular VSCs, are still in the technology development phase and offer promising solutions to the technical challenges faced in the contemporary application areas of VSC-HVDC transmission.

2.4.1 2-level VSC

The most basic form of a VSC is the half-bridge VSC shown in Figure (2.7). In this configuration, two distinct voltage levels per phase with respect to the DC midpoint can be produced at the output terminal. One voltage level is $\frac{V_{dc}}{2}$ when the upper device is conducting, and the other level is $-\frac{V_{dc}}{2}$ when the lower device is conducting.

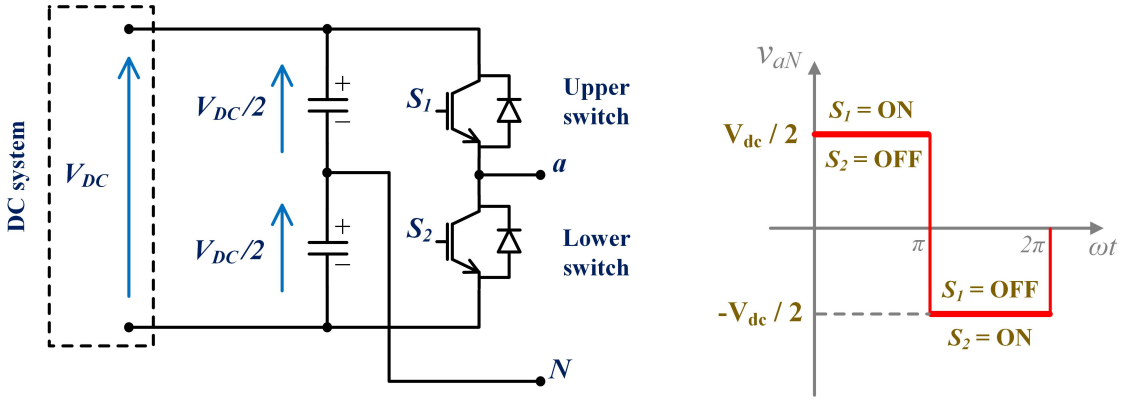


Figure 2.7: Half-bridge VSC configuration and output waveform

The connection of three half-bridge VSCs in parallel leads to the three-phase two-level VSC shown in Figure (2.8). The output voltages of the three-phase VSC are 120° apart and are interfaced to an AC system through a transformer. The conduction states of the devices can be electronically controlled using Pulse-Width Modulation (PWM) which makes it possible to vary the r.m.s. of the fundamental component of the output voltage. Moreover, the use of PWM also shifts the output harmonics to higher order frequencies, thereby reducing the filtering requirements. The reduction or elimination of the low order harmonics is linked to the switching frequency of the PWM. At higher PWM switching frequencies, a higher reduction of the low-order

harmonics is achieved but at the expense of increased switching power losses. Due to this trade-off, a balance between the levels of harmonic distortion and the cost incurring from additional power losses has to be achieved.

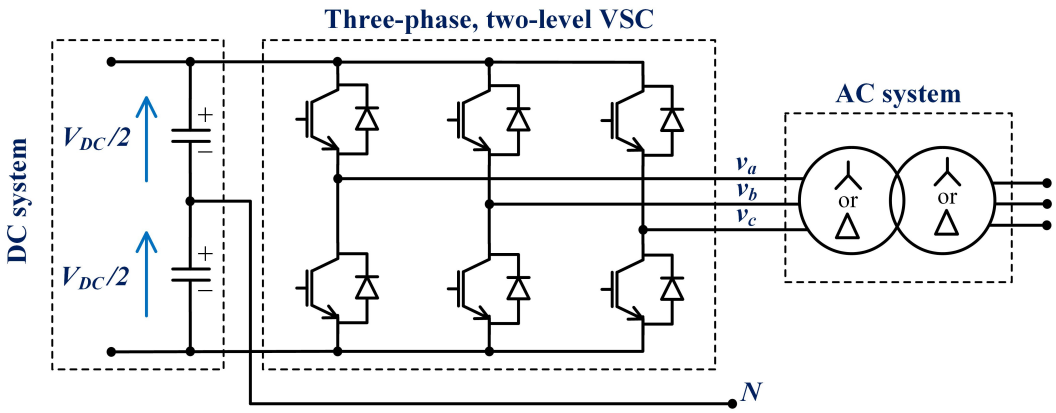


Figure 2.8: Three-phase two-level VSC

IGBTs only allow current in one direction and hence, a free-wheeling diode is connected in anti-parallel to the IGBT to allow bi-direcitonal current flow. In HVDC applications, several of these IGBT-diode modules are stringed together in each switch position to achieve an equivalent "valve" for high voltage levels. Dynamic balancing of the switch voltages between the series-connected IGBTs during switching transients is a critical issue which requires the use of snubber circuits [16].

The drawbacks of the 2-level VSC are higher switching losses and relatively high filtering requirements (although much smaller than with LCC). Moreover, the high $\mathrm{d}v/\mathrm{d}t$ of the output voltage imposes increased insulation requirements on the interfacing transformers.

2.4.2 Multilevel VSCs

The second generation of the VSCs are the multilevel VSCs which were developed to address the shortcomings of the 2-level VSC. The concept of "multilevel" is associated with three output levels or higher in the output waveform. With the help of multiple output levels, multilevel VSCs are able to reduce the effective switching frequency per

device, resulting in lower switching losses, and achieve lower harmonic distortion and dv/dt in the output voltage, leading to reduced filtering and insulation requirements.

In the following paragraphs, an overview of some of the prominent multilevel VSCs is presented.

2.4.2.1 Neutral Point Clamped Converter (NPC)

The Neutral Point Clamped (NPC) converter was first introduced in 1981 [23] for medium-voltage drive applications and first used for HVDC applications in 2000 in the Eagle Pass project in the USA [25]. The basic NPC converter is a three-level VSC, which is capable of producing a '0' state at the output, in addition to a positive and a negative level.

The basic circuit of a three-phase three-level NPC is shown in Figure (2.9). The DC bus voltage is split into three voltage levels by two series connected capacitors, C_1 and C_2, with their mid-point connection defined as the zero voltage or neutral point [26]. Structurally, the NPC is formed by connecting together two half-bridge VSCs. The AC output is taken from the connection point of the two half-bridge VSCs whereas their original outputs are clamped to the neutral point through clamping diodes.

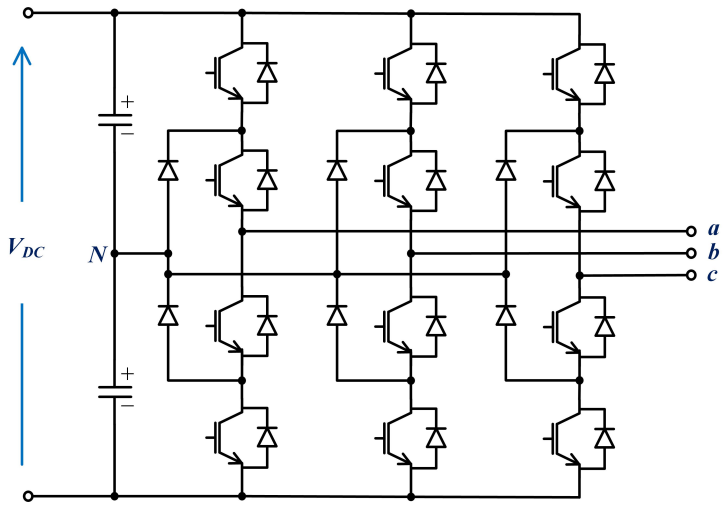


Figure 2.9: Three-phase Neutral Point Clamped (NPC) converter

In the NPC converter, the two clamping diodes are the distinguishable feature that allow the output of the converter to access the zero potential of the neutral point, thus enabling the generation of the '0' output level along with $\frac{+V_{dc}}{2}$ and $\frac{-V_{dc}}{2}$. Although the number of switch positions in the NPC are twice that of the 2-level VSC, each string of IGBTs is rated for $\frac{V_{dc}}{2}$, effectively resulting in the same IGBT count for the two converters. Hence, just with the use of additional clamping diodes, the waveform quality of the AC voltage in the NPC is substantially improved compared to the 2-level VSC.

The NPC topology can be extended to a higher number of output levels by increasing the number of DC-link capacitors and using additional power switches and clamping diodes. A 5-level NPC is shown in Figure (2.10). Although a higher number of switches is needed if the output levels of the NPC are to be increased, the voltage stresses on each switching device reduces [16]. However, for NPCs with higher output levels, there is a dramatic increase in the number of clamping diodes needed to share the voltage [27], and in addition, the complexity of the dc-link capacitor balance control increases. As a result, the industrial applications of the NPC have been limited mainly to three levels only [27].

2.4.2.2 Active Neutral Point Clamped Converter (ANPC)

The Active Neutral Point Clamped Converter (ANPC) is a variation of the original NPC which uses additional IGBTs in parallel with the clamping diodes, first introduced for HVDC applications in [28]. A 3-level ANPC is shown in Figure (2.11).

In this configuration, a more equal distribution of the semiconductor losses is achieved, leading to a higher output power capability due to better switch utilisation [29]. An example of the 3-level ANPC in HVDC is the ±150 kV, 330 MW Cross-Sound Cable Project in the US that interconnects the energy markets of New England and New York [30].

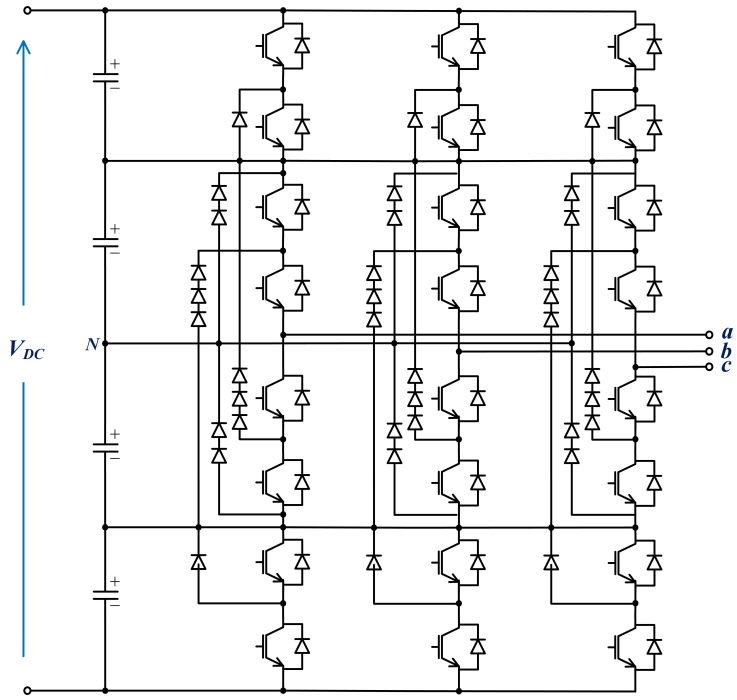


Figure 2.10: Three-phase five-level Neutral Point Clamped (NPC) converter

2.4.2.3 Flying Capacitor Converter (FCC)

The Flying-Capacitor Converter (FCC) topology, first introduced in [31], is structurally quite similar to the NPC topology, with the main difference being that floating capacitors replace the clamping diodes [27]. A 3-level FCC is shown in Figure (2.12).

Unlike the NPC, the output in the FCC cannot be connected to the neutral point to generate the '0' voltage level. Instead, the '0' voltage level is obtained by controlling the switches such that the output is connected to the DC link through the flying capacitor with opposite polarity with respect to the DC link [24]. For the '0' voltage level generation, redundant switching combinations are available that can be utilised to balance the floating capacitor voltages.

The FCC topology can be considered "modular" since the addition of a pair of switches and a capacitor provides an additional voltage level to the output. Thus, it can easily be scaled to higher voltages required in HVDC transmission applications.

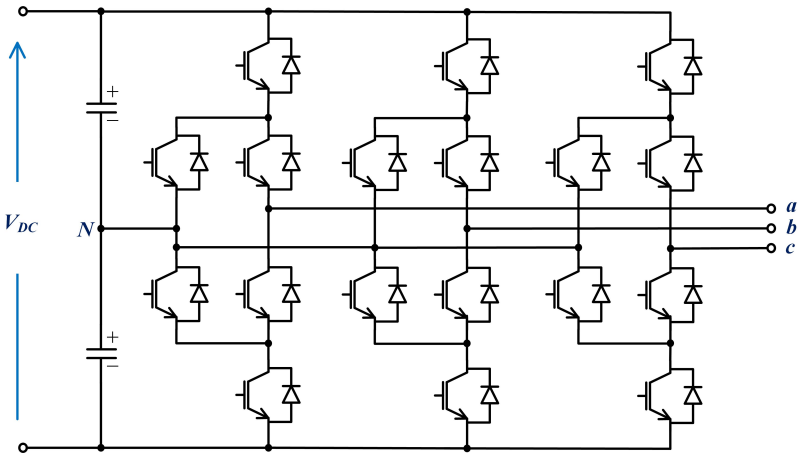


Figure 2.11: Three-level Active Neutral Point Clamped (ANPC) converter

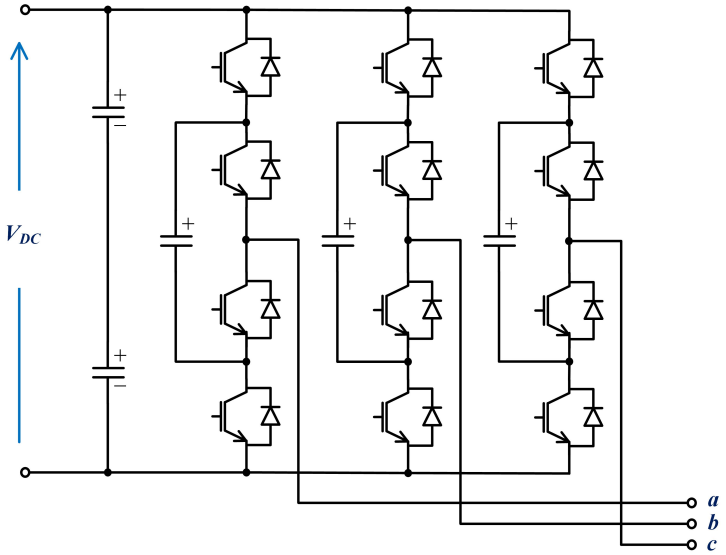


Figure 2.12: Three-level Flying Capacitor Converter (FCC)

The drawback of the FCC is the large converter footprint due to the bulky floating capacitors.

2.4.2.4 Cascaded Full-Bridge Converter (CFB)

A full-bridge module, which is a parallel connection of two half-bridge legs shown in Figure (2.13), is capable of producing three output levels i.e. $+V_{dc}$, $-V_{dc}$ and 0. Stringing together two or more full-bridge modules leads to the Cascaded Full-Bridge Converter (CFB) topology. A three-phase CFB is depicted in Figure (2.14).

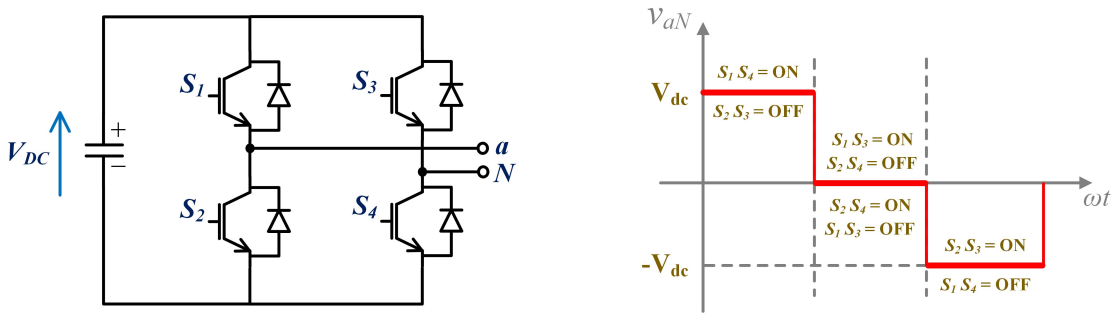


Figure 2.13: A full-bridge module and its output waveform

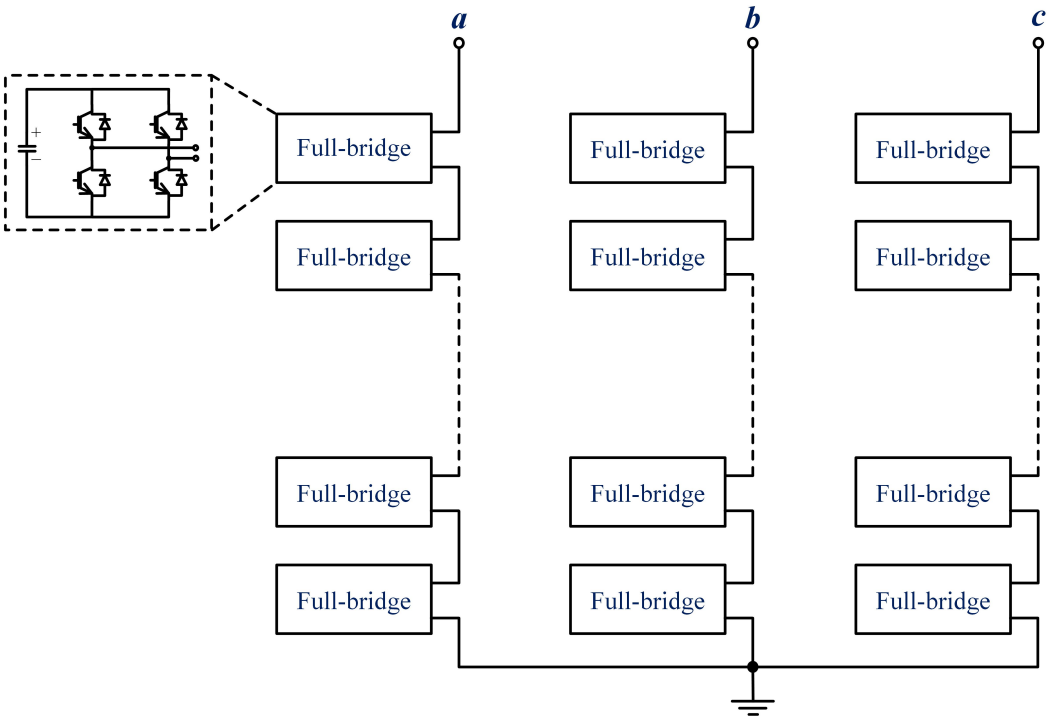


Figure 2.14: Cascaded Full-Bridge (CFB) Converter

The CFB topology was first introduced in [32]. In the CFB converter, the output voltages of the full-bridges are combined to form a multilevel waveform at the output. For N full-bridges connected in series, a total of $2N+1$ different voltage levels can be produced, and hence the CFB is a modular topology.

A major drawback of the CFB topology is the need for isolated DC bus voltage for each full-bridge, especially in case of real power exchange [33]. The separate

DC sources are usually supplied by a three-phase rectifier fed by a transformer [27], which adds significantly to the cost of the converter. Hence, the CFB is more suited to specific applications, for example, the STATCOM, where the objective is to exchange reactive power only [24].

2.4.3 Modular Multilevel Converter - MMC

As discussed above, several multilevel VSC topologies have been proposed for HVDC applications which offer better output quality and reduced losses compared to the two-level VSC. Although some of these multilevel topologies are modular, their structural complexity increases with the number of output levels [34] which inhibits their extensive utilisation in commercial HVDC transmission applications.

The Modular Multilevel Converter (MMC), first introduced by Prof. Marquardt in 2001 [35], offers a completely modular design and is easily scalable to the high voltage levels required in HVDC applications. In addition to modularity, the MMC also features low switching losses, low $\mathrm{d}v/\mathrm{d}t$ leading to reduced insulation requirements, and high quality output waveforms, resulting in little to no filtering requirements.

Due to its comparative benefits over other multilevel converters, the MMC has been widely accepted by the industry, with applications in HVDC, medium-voltage drives and power quality regulation. Major HVDC manufacturers like ABB, Siemens and General Electric all have their own MMC-based HVDC converter solutions under different brand names, e.g. HVDC Light (ABB) and HVDC Plus (Siemens). The first commercial usage of the MMC in HVDC applications was in the Trans Bay Cable project in the US, commissioned by Siemens in 2010 [36].

2.4.3.1 Basic structure and operation

The basic structure of the MMC is shown in Figure (2.15). The distinctive feature of the MMC is the series connection of identical submodules, termed as a ChainLink (CL) in this thesis. This feature allows for a modular structure that makes the MMC superior to the earlier multilevel topologies for HVDC applications, as the MMC can be easily scaled to high voltage and power levels by adding submodules in each CL.

The three-phase MMC of Figure (2.15) has three phase-legs connected in parallel to the DC bus. The three-phase AC outputs are taken from the midpoint of the phase-legs. Each phase-leg has two arms; the upper arm, which is connected between the positive DC bus bar and the AC output, and the lower arm, which is connected between the negative DC bus bar and the AC output. Each arm is made up of a CL and an arm reactor. The submodules in the CLs consist of a capacitor and IGBTs connected in different configurations, out of which the Half-Bridge configuration is the most common.

A half-bridge submodule, that is formed by two IGBTs and a capacitor, can either present the capacitor voltage at its output or a zero voltage depending on whether the upper or the lower switch is on. In the context of the MMC, this essentially means that a half-bridge submodule can either be inserted (capacitor voltage at the output) or by-passed (zero voltage at the output). Thus, by appropriately controlling the switching of the devices in the submodules, each CL can be configured to operate as a controllable voltage source, given that no net power is exchanged with a CL in steady-state and the energy balance between the submodules is maintained. In the MMC, the CL voltages can be synthesised such that the combination of the CL voltages within the arms and the phase-legs result in the desired voltages at the AC and DC outputs of the converter [37]. Thus, the MMC can act as a controllable voltage source on both the AC and DC sides, which is different from two-level and multilevel converters that behave as a current source behind a capacitor when seen

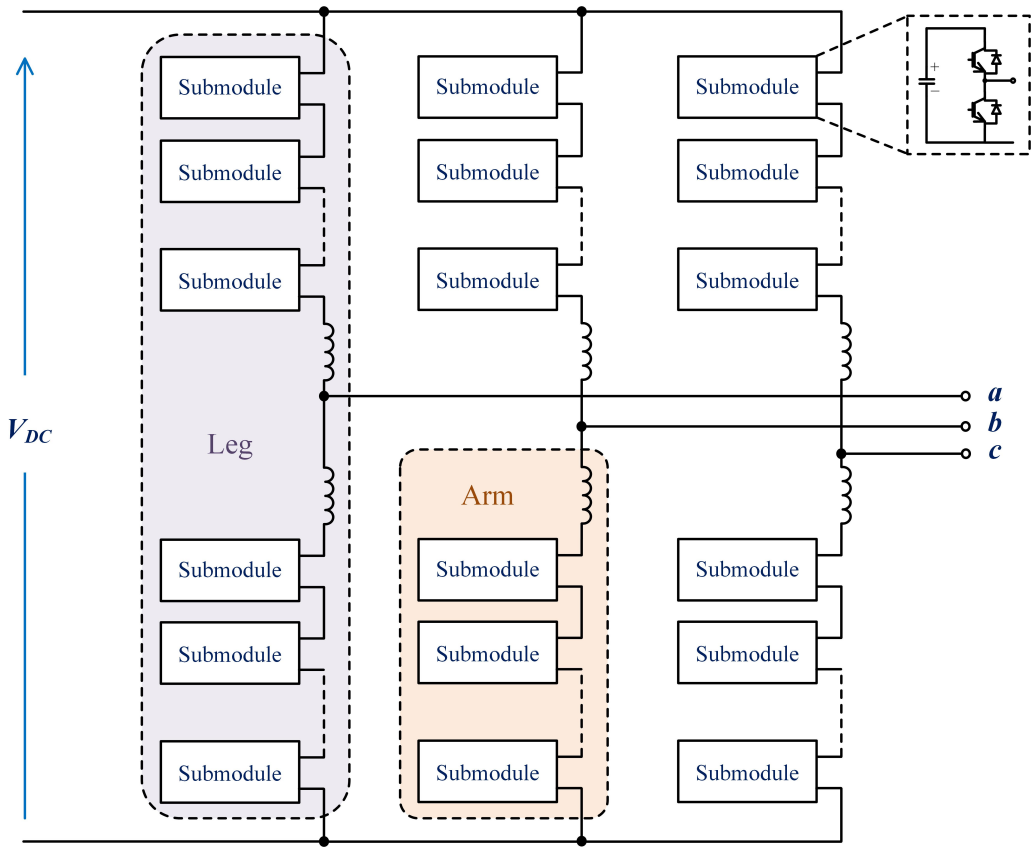


Figure 2.15: Basic structure of the Modular Multilevel Converter

from the DC side [37].

2.4.3.2 Control and Modulation

The primary control objectives in the MMC, that are needed to ensure stable operation are the output current control and cell capacitor voltage control. Moreover, secondary control objectives, such as the circulating current control, can also be employed to influence the size, efficiency and reliability of the MMC [38]. A block diagram of an MMC control structure is shown in Figure (2.16).

The control of the output current in the MMC employed in HVDC applications is similar to that in other multilevel converters, i.e. a closed-loop controller calculates the output AC voltage reference based on the error between the output AC current and its reference. The output AC current reference is usually obtained from an outer

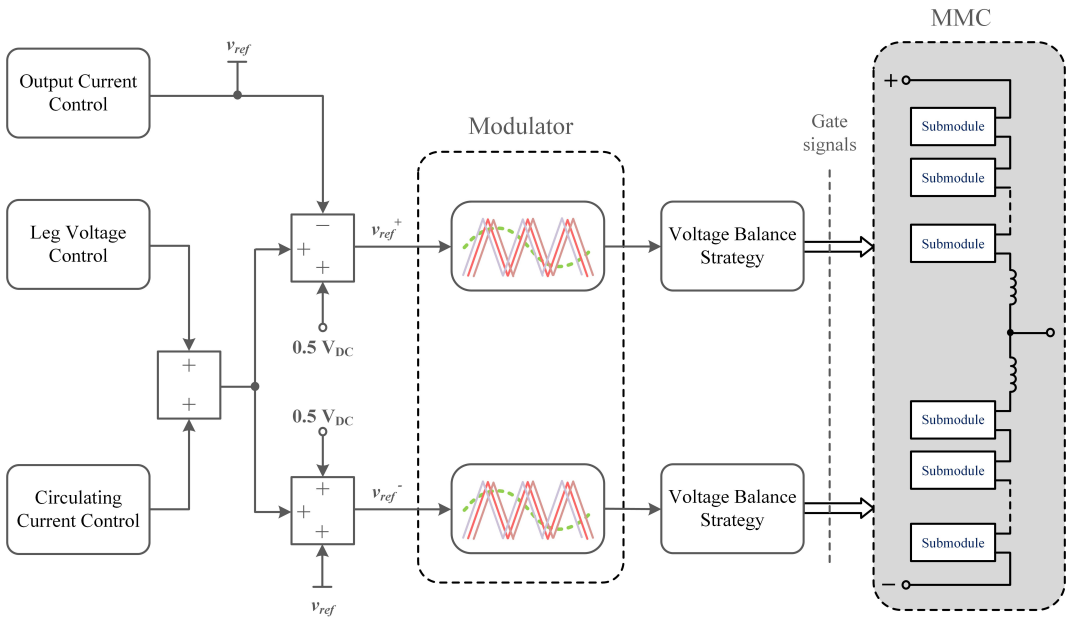


Figure 2.16: Block diagram of MMC control

DC voltage/power controller which regulates either the DC voltage or the active power flow.

The feature of the MMC that makes its control more complicated than the earlier VSC converters is the presence of a large number of floating SM capacitors, distributed across the arms and phase-legs of the MMC. The first challenge is to regulate the capacitor voltages such that the average voltage of all cells is controlled to a reference level. In terms of control strategy development, this can be achieved by maintaining power balance between the AC and DC sides (in steady-state), so that zero net energy is exchanged with the cells over a period. The second challenge is to balance the cell voltages between the arms, as well as between the cells in each arm. The arm balancing can be integrated into the control strategy by redistributing the energy between the arms. The cell voltage balancing is usually implemented directly on the modulation signals by reallocating the switching patterns amongst the cells using sorting techniques.

The circulating currents in the MMC are second-harmonic currents that flow internally within the converter phase-legs but do not appear in the AC and DC side

currents. If left unregulated, the circulating currents can increase the peak/RMS value of the arm currents, thereby increasing the losses [39]. Thus, a circulating current controller is usually added to the MMC control strategy to suppress the circulating current. The same controller can also be used to maintain the circulating current at a reference value for the purpose of reducing cell capacitance [40].

The modulation techniques employed for the MMC include carrier-based modulation, which includes the phase-shifted PWM and level-shifted PWM. In these techniques, the modulation reference is compared with higher frequency triangular carrier waves. Thus, the resulting switchings are at a higher frequency, which leads to higher switching losses. For high voltage applications, where hundreds of sub-modules are connected in series, low-frequency modulation is favourable to reduce the switching losses. Such modulation techniques include the selective harmonic elimination (SHE) and the nearest level modulation (NLM) [38].

2.4.3.3 Operational Issues and Challenges

In the field of HVDC, the MMC has been considered a massive step forward compared to the two-level converters. Although the MMC eliminates the need for AC side filters and a large DC-link capacitance and thus provides cost-saving, the converter arrangement itself is more costly and occupies more volume than the two-level converter. This is because the number of switching devices required in the MMC is at least twice compared to two-level converters, and in addition, the MMC employs hundreds of bulky sub-module capacitors in high voltage applications. Moreover, arm reactors are also required in the MMC to suppress the circulating currents and to reduce the rate of surge current during DC faults. Hence, there have been numerous efforts to reduce the cost and volume of the MMC to make it more attractive for space-critical applications e.g. offshore wind.

The MMC has the potential capability to ride through different types of AC faults,

making it favourable for applications subjected to strict grid code requirements [16]. In case of asymmetrical faults, the healthy phases will operate unaffected, and potentially at high per-phase power [16].

In MMC-HVDC applications, DC-side faults are challenging for the most commonly used half bridge configuration of the MMC. At the instant of the DC-side fault, the IGBTs are blocked to prevent them from damage due to over-current. Hence, the HB-MMC behaves like an uncontrolled diode rectifier, and the AC side feeds into the DC fault. However, one advantage compared with two-level converters is that the cell capacitors do not discharge into the fault, making the post-fault recovery easier. Nonetheless, DC faults are a challenging issue in the MMC, and several alternative submodule configurations and alternative circuit arrangements have been proposed to tackle the issue [41][42][43][44][45][46].

2.4.4 Alternative Modular Multilevel Converters

2.4.4.1 Alternative Submodule Configurations

The half-bridge configuration is the dominant type of submodule for HVDC applications because of the lowest losses and the lowest cost [47]. Several other submodule configurations have been proposed to improve certain aspects of the MMC.

The most obvious alternative is the *full-bridge (FB) submodule*, shown in Figure (2.13). With the use of FB submodules in the arms of the MMC, during a DC fault, a counter voltage can be produced which blocks the flow of the fault current from the AC side into the DC fault. This is achieved at the expense of twice the number of IGBTs and approximately 70% to 80% higher losses [48].

Other alternative submodule topologies that provide DC fault blocking are the *clamped single-submodule (CSSM)* [41] and the *clamped double-submodule (CDSM)* [42], shown in Figure (2.17). Compared to the HB submodule, the CSSM employs an additional

IGBT and two additional diodes [41]. Moreover, the submodule capacitor is split into two capacitors and their midpoint is connected to submodule's lower terminal through diode D4. During normal operation, S3 is always on. When all the IGBTs are blocked in the event of a DC fault, the CSSM arrangement presents either one or both of the SM capacitors in the fault current path, depending on the current direction.

The CDSM is essentially a series connection of two HB submodules during normal operation, realised by means of the IGBT S5 and its anti-parallel diode D5 and two additional diodes D6 and D7 [48]. During a pole-to-pole DC fault, for a positive arm current, diodes D2, D3 and D5 conduct due to which both capacitors are in series, thereby presenting twice the DC voltage against the AC line-to-line voltage. If the current direction is negative, the diodes in conduction are D1, D4, D6 and D7 which results in a parallel connection of the capacitors, and the whole DC voltage is available for blocking the fault current from the AC side.

When compared with HB and FB submodules, both the CSSM and the CDSM are intermediate solutions in terms of losses and semiconductor requirement. Between the CSSM and CDSM, the CSSM has a slightly lower semiconductor requirement and slightly higher losses than the CDSM [49].

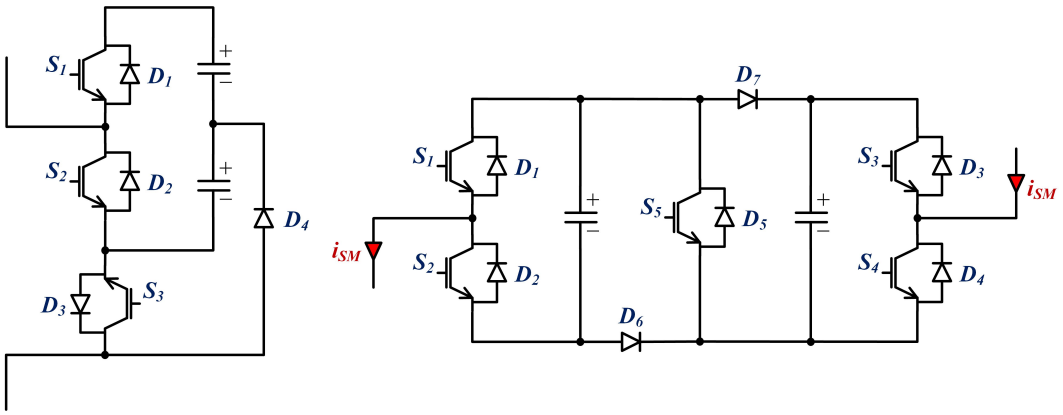


Figure 2.17: Clamped Single-Submodule (left) and Clamped Double-Submodule (right)

Other alternative submodule configurations are the cross-connected submodules,

namely the *five-level cross-connected submodule (5L-CCSM)* [43] and the *three-level cross-connected submodule (3L-CCSM)* [44], shown in Figure (2.18). As the name suggests, the 5L-CCSM consists of two back to back half-bridge cells cross-connected through two IGBT-diode pairs, S6-D6 and S5-D5. The 3L-CCSM also has the same structure, with the difference that one of the IGBTs (S6) has been omitted. Both the 5L-CCSM and the 3L-CCSM provide DC fault blocking, and both configurations insert the same negative blocking voltage during DC faults. According to [43], for the 5L-CCSM, composing an MMC arm with 25% 5L-CCSM submodules fulfills the DC fault blocking criteria, with the rest of the submodules being the HB configuration.

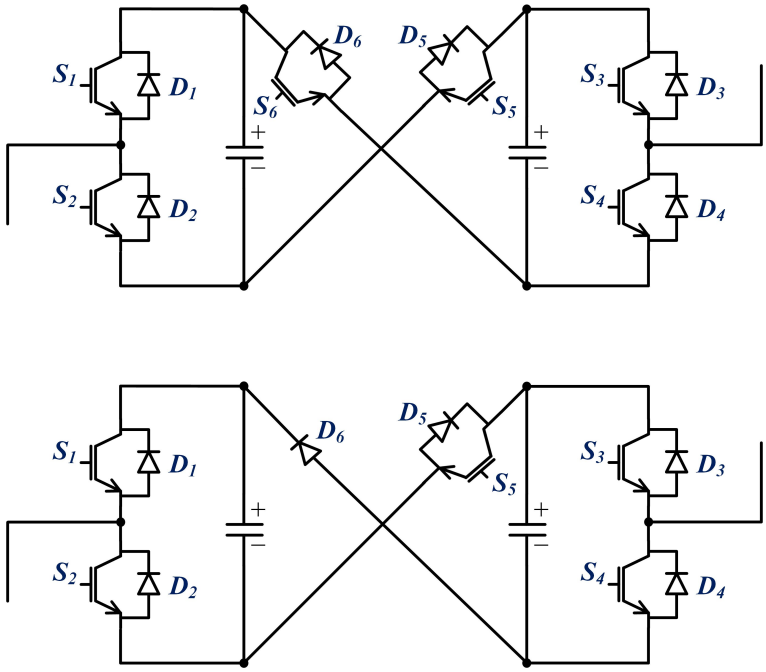


Figure 2.18: Five-level cross-connected submodule (top) and three-level cross-connected submodule (bottom)

Lastly, the submodule configuration that also deserves a mention is the *semi-full-bridge submodule (SFB-SM)* [45], which is an extension of the CDSM and also provides DC fault tolerance. The SFB-SM, shown in Figure (2.19), is derived by replacing the two diodes in the CDSM with IGBT-diode pairs. With the SFB-SM configuration, two positive voltage levels and one negative voltage level can be obtained at the output. Since the SFB-SM uses two capacitors which can be bypassed, connected in series, or in parallel, it can replace two conventional HB submodules.

According to [45], with some switching constraints, the semiconductor requirement in the SFB-SM is 50% higher compared to the HB submodule, and 25% lower compared to the FB submodule. Furthermore, by using the negative voltage levels to increase the modulation index above unity, a 59% reduction in the capacitor voltage ripple can be achieved.

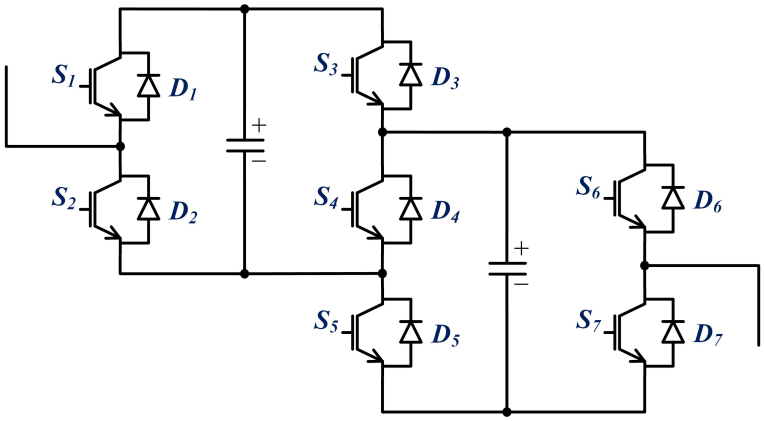


Figure 2.19: Semi-Full-Bridge submodule

2.4.4.2 Hybrid MMC

In the previous section, alternative SM configurations for the MMC that provide DC fault blocking capability were discussed. In the MMC, each arm is rated for the whole DC voltage. This means that employing only a portion of "DC-fault tolerant" SMs (about 50% for a modulation index close to unity) in the arms can present sufficient blocking voltage against the AC line-to-line voltage during DC faults. The remaining SMs in the arm can be the more efficient, less expensive HB submodules. In this manner, each arm of the MMC is composed of a hybrid design with two types of SMs i.e. HB SMs and "DC-fault tolerant" SMs. In [44], hybrid MMC configurations based on different types of DC-fault tolerant SMs in combination with the HB SMs are proposed along with comparisons between the configurations. However, in [46], the term "hybrid MMC" is used to only represent a combination of HB SMs and FB SMs in an MMC arm, which is also the definition adopted in this thesis.

The basic structure of the hybrid MMC is depicted in Figure (2.20). As mentioned

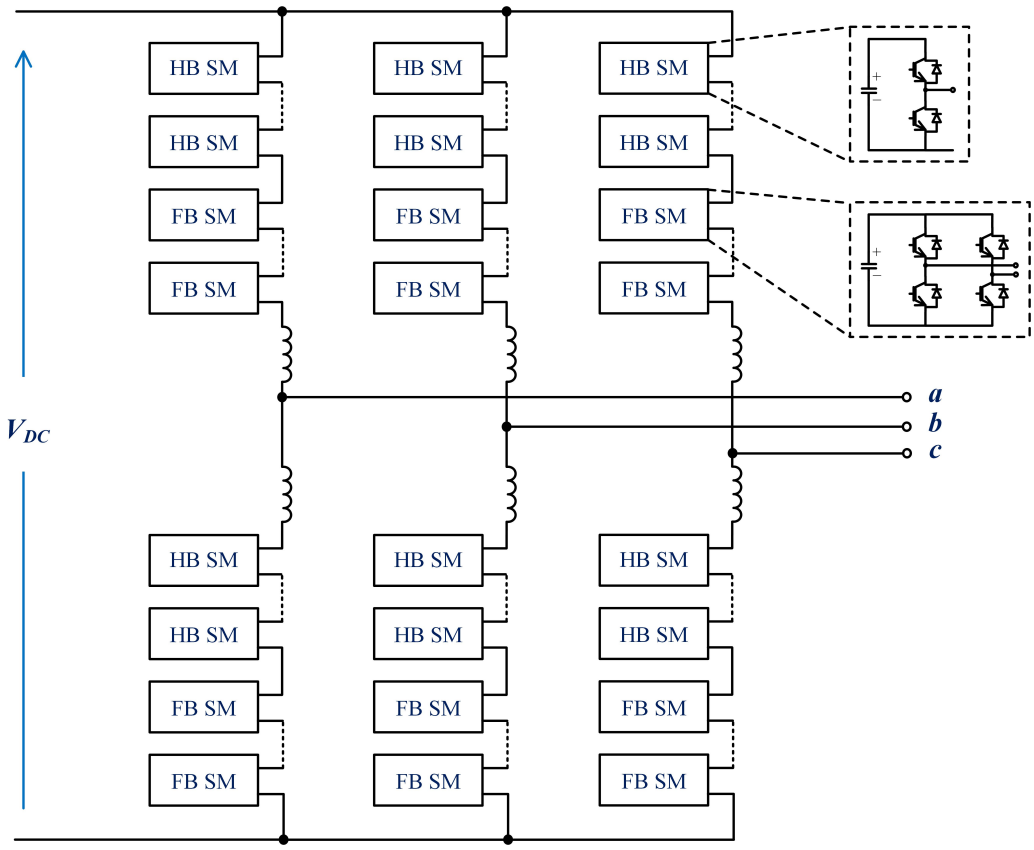


Figure 2.20: Basic structure of the hybrid MMC

above, each arm is composed of a series connection of both HB submodules and FB submodules. During normal operation, there are no operational differences between the standard HB-MMC and the hybrid MMC.

Generally, for DC fault handling, the blocking voltage formed by a series connection of SM capacitors in two arms (one upper arm and one lower arm in different legs) should be greater than the peak line-to-line converter AC voltage. Hence, the number of FBs required in the hybrid MMC for DC fault blocking are:

$$N_{FB}^{H-MMC} \geq \frac{\hat{V}_{LL}}{2V_c^{nom}}$$

where V_c^{nom} is the nominal value of the SM capacitor voltage.

For normal operation of the hybrid MMC, the conventional control strategy of the HB-MMC can be employed. However, due to the presence of FBs in the hybrid MMC,

there is a possibility to utilise the negative voltage state of the FBs to extend the AC output voltage range beyond the limits imposed by the DC voltage, thereby increasing the power transmission capability. This idea is explored in detail in [46], in which the authors conclude that in order to ensure sufficient charging and discharging times for the HB submodules in a hybrid MMC arm to balance their capacitor voltages, the number of FB submodules generating the negative voltage state must not exceed one-third of the total number of submodules in the arm [46]. Furthermore, in this type of operation of the hybrid MMC, the conventional cell sorting strategy of the HB-MMC needs to be modified to account for the fact that the HBs in an arm have to be bypassed during the periods when the arm voltage is negative.

The hybrid MMC is a promising alternative to the FB-MMC for HVDC transmission applications where DC fault handling capability is critical. With the hybrid MMC, the same objectives as the FB-MMC are achieved at a lower semiconductor cost and with lower losses.

2.4.4.3 Series-Connected MMC

A disadvantage of the MMC is the high station cost. In a conventional MMC, the three phase-legs are connected in parallel with the DC bus, and the semiconductor rating of each arm should be enough to block the whole DC voltage. To reduce station cost, one option is to employ a series connection of converter phases, resulting in the Series-Connected MMC (SC-MMC) topology. Compared to the conventional MMC, a one-third reduction in the number of semiconductor switches is achieved for withstanding the same DC voltage. The concept of the SC-MMC was first introduced in [50] for HVDC tapping applications. HVDC tapping is the supply of power to the rural or small urban communities that are in close proximity to an HVDC line. Usually, the power "tapped" is only a small portion of the rated power, and hence, the standard (and expensive) converter stations are not viable.

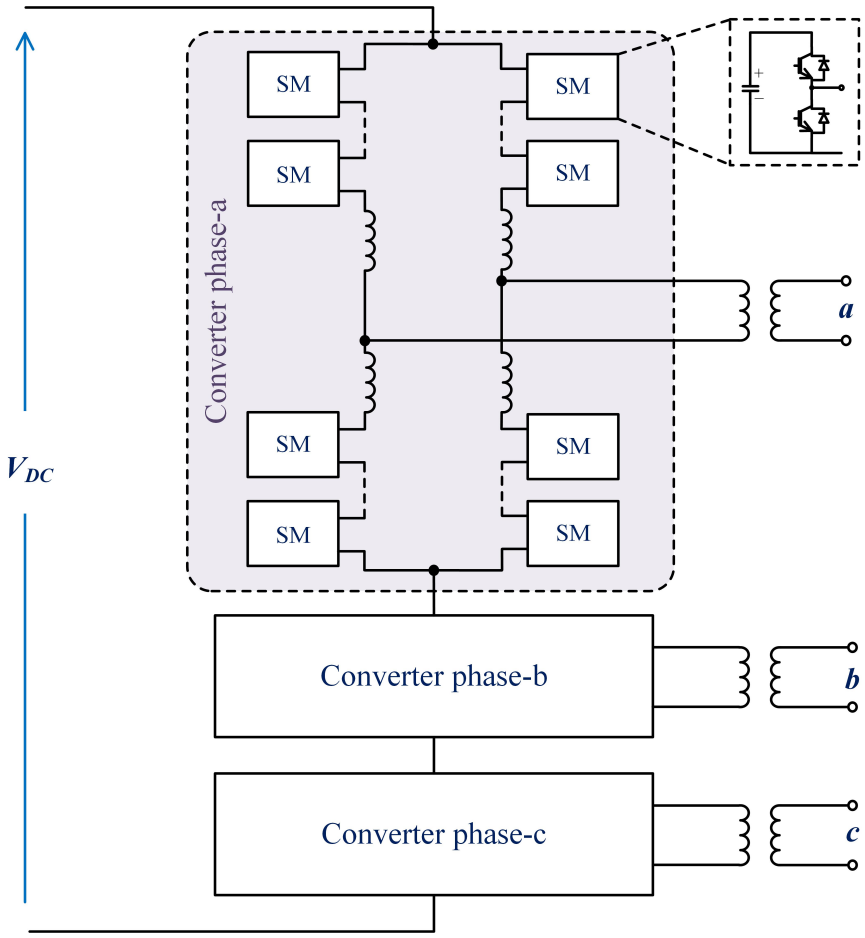


Figure 2.21: Basic structure of a series-connected MMC

Further details of the SC-MMC operation and control have been presented in [51]. The basic structure of the SC-MMC is shown in Figure (2.21). The three converter phases are connected in series across the DC side. Each converter phase is composed of four arms connected in an H-bridge configuration. The AC outputs of the three converter phases are connected to the secondary windings of three single-phase transformer, and the primary windings of the transformers are delta-connected to the AC grid. In the SC-MMC, the full DC current flows through each converter phase, and hence, due to the IGBT current limits, the P/Q capability of the converter is lower than the conventional MMC.

2.4.5 Hybrid VSCs

Over the past two decades, there has been rapid innovation in converter topologies for VSC-HVDC. Since the industrial acceptance of the MMC, extensive research efforts globally have led to the introduction of various alternative MMC configurations with improved features and lower cost and size of the converter. Furthermore, as a result of these efforts, in recent years, a new breed of VSC topologies have come to light that combine the characteristics of both modular multilevel converters and the conventional two- and three-level converters. These are termed as 'Hybrid VSC topologies'.

The basic concept of the Hybrid VSC topologies is to use the multilevel converter chainlinks to provide a voltage wave-shaping function which is then 'directed' to the appropriate AC or DC network using the semiconductor switches arranged in two- or three-level configuration [52]. The multilevel chainlinks providing the wave-shaping function are referred to as 'waveshaping circuits' and the two- or three-level switch arrangements are termed as 'director switches'. Due to the design flexibility, several topologies can be derived by considering either series or parallel connections of the waveshaping circuits and the director switches, and by choosing to place the waveshaping circuits either on the AC or the DC side [53].

In this section, some of the recently proposed hybrid VSCs are reviewed. At the time of writing, none of these topologies have yet been commercially used in any HVDC projects. However, out of the topologies discussed, the Alternate Arm Converter and the Series Bridge Converter are being researched and developed by General Electric, and may form the next generation of commercial VSC-HVDC converters.

2.4.5.1 Alternate Arm Converter

The Alternate Arm Converter (AAC) [54] [55] is a hybrid VSC topology that is intended to provide DC fault blocking capability without compromising the efficiency and the semiconductor requirements of the converter. The basic structure of the AAC is depicted in Figure (2.22). Structurally, it is similar to the MMC, except with the difference that an additional director switch is employed in each arm. Moreover, the cells in the arms are FB submodules to allow for DC fault handling.

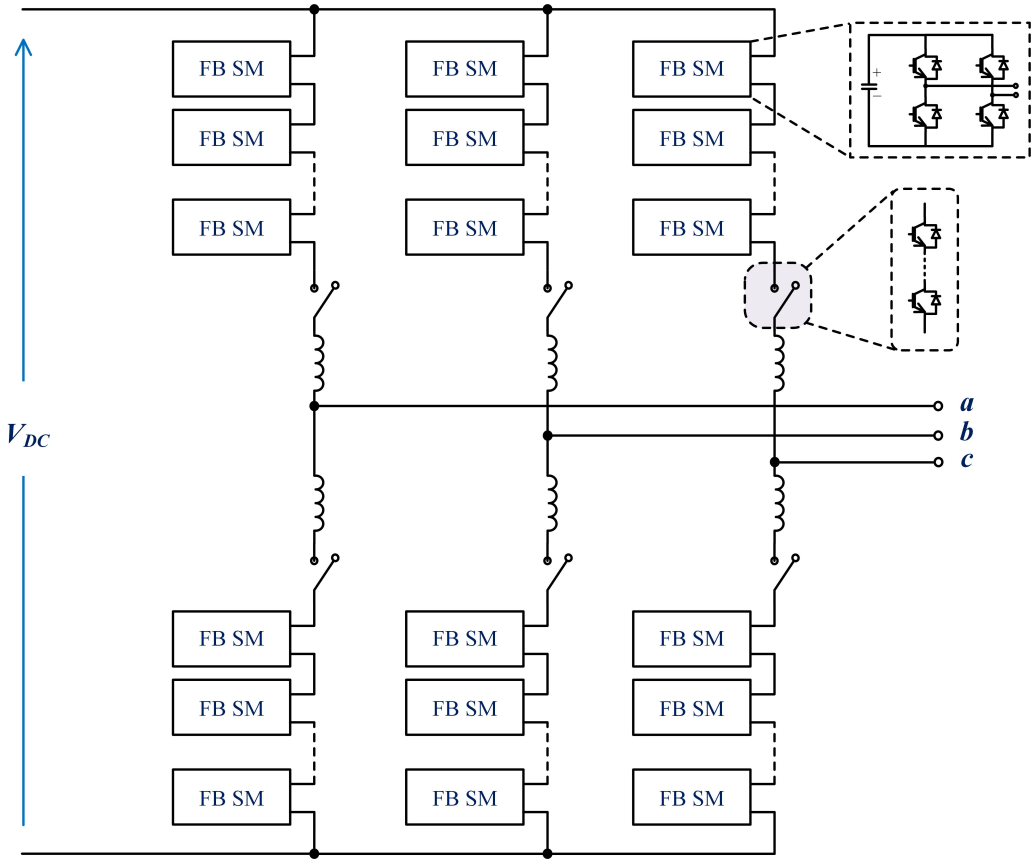


Figure 2.22: Basic structure of the Alternate Arm Converter

In the AAC, each of the director switches in a phase-leg conducts during half of the fundamental cycle, thereby resulting in alternate conduction of the two arms in a phase-leg. Each arm constructs only one half-cycle of the AC voltage, as illustrated in Figure (2.23), and the maximum voltage that the arm has to produce is equal to half of the DC bus voltage. Hence, the voltage rating, and consequently the number

of submodules, of each arm is one-half of that in the MMC [55].

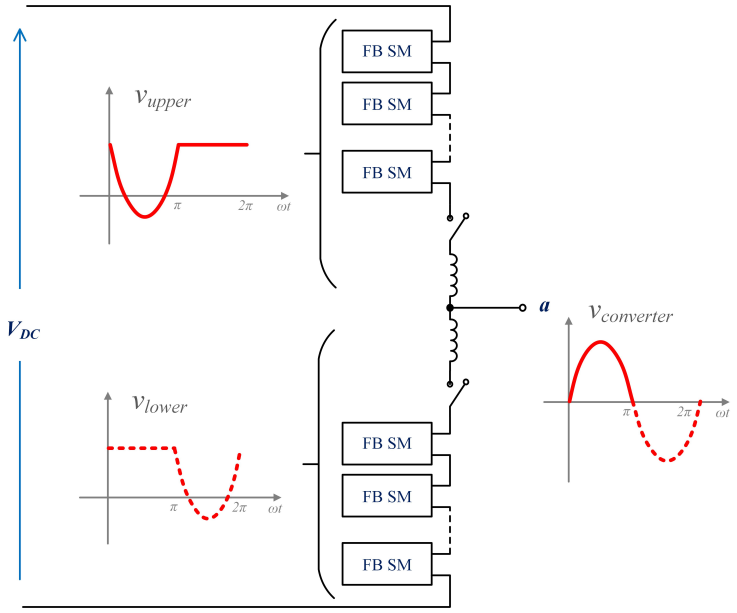


Figure 2.23: Theoretical arm voltages of a single-phase of the AAC

One other difference between the MMC and the AAC is that unlike the MMC that is a voltage source towards the DC side, the AAC acts as a current source as seen from the DC terminal. This is because each phase-leg of the AAC injects one half-cycle of the AC waveform into the positive DC pole, and the other half-cycle into the negative DC pole. Since the sum of the AC half-cycles injected into the DC poles by the three phase-legs of the AAC is composed of 6n harmonics, the AAC requires a rather large DC filter to smoothen the DC voltage.

Furthermore, as a consequence of the AC half-cycle injection into the DC poles, the AC and the DC sides in the AAC are directly coupled. This means that in order to achieve power balance between the AC and DC sides, a fixed ratio between the AC-side and DC side voltages need to be maintained. In [55], by equating the AC-side and DC-side energies and then performing some arithmetic manipulation, this ratio is defined as:

$$\hat{V}_{AC} = \frac{2}{\pi} V_{DC} \tag{2.1}$$

This specific ratio between the AC and DC voltage magnitudes corresponds to a

modulation index of $\frac{4}{\pi}$. Hence, the AAC is required to operate in over-modulation, which is possible due to presence of full-bridge cells in the converter arms. In practical HVDC applications, where the DC voltage levels are usually specified and in addition, the converters are interfaced to the AC network through transformers, the turns ratio of the transformer can be selected to obtain the AC voltage according to Eq. (2.1).

In order to compensate for AC and DC voltage variations and to facilitate reactive power exchange between the converter and the AC grid, a certain flexibility in the modulation index of the converters is usually required in grid-connected applications. To be able to operate the AAC at modulation indexes different than $\frac{4}{\pi}$, a short overlap period is introduced when passing the conduction from one arm to the other in a phase-leg. During this period, a current flows in both the arms of a phase-leg simultaneously that can be used to exchange energy between the two arms and the DC terminal. It must be noted that the required overlap period increases as the modulation index moves farther from $\frac{4}{\pi}$, and a larger overlap period leads to higher losses in the converter.

When compared with the MMC, the AAC has lower arm energy fluctuations, and the capacitor voltage ripple is reduced [37]. In [56], it has been concluded that the cell capacitor of the AAC is slightly less than half the size and the capacitive energy storage of the converter arms is about a third of that of the MMC. However, the disadvantage of the AAC is the need for a large DC bus filter. In addition, the director switches in the AAC need to withstand the peak AC voltage, which leads to a higher semiconductor expenditure in the AAC compared to the MMC.

In order to address some of the shortcomings of the AAC, a new mode of operation of the AAC called “Extended Overlap” has been introduced in [57]. The EO-AAC extends the overlap period to 60° which decouples its DC current path from the AC current paths. This feature of the EO-AAC eliminates the need for the DC smoothing filters and frees the constraint on the operating modulation index, thereby improving the original AAC topology.

2.4.5.2 Hybrid Multilevel Converter with AC side cascaded H-bridges

The hybrid multilevel converter with AC side cascaded H-bridges [58] (shown in Figure (2.24)) is another hybrid VSC topology that uses the basic two-level converter circuit along with waveshaping circuits on the AC side. In this topology, the two-level converter is the main power stage that produces a square wave output at its AC terminal. The H-bridge cascaded cells in each phase (i.e. waveshaping circuits) are controlled to produce the voltage difference between the desired fundamental AC voltage and the two-level converter output voltage, thereby acting as series active filters. This configuration allows the two-level converter to be switched at a much lower frequency than would be possible without the AC-side waveshaping circuits.

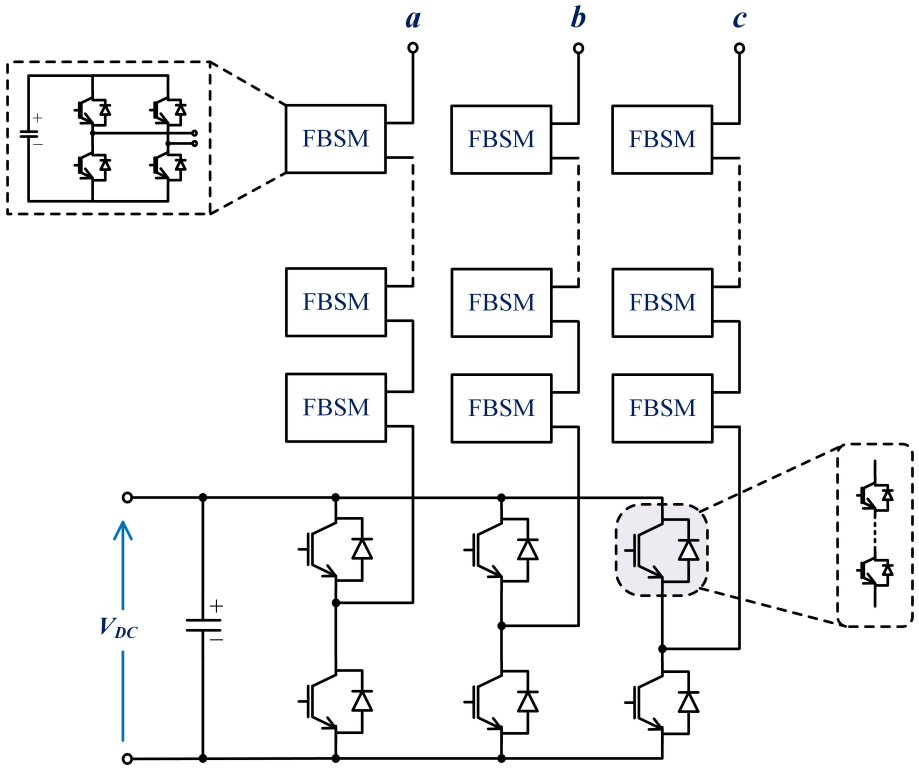


Figure 2.24: Schematic of the Hybrid Multilevel converter with AC side cascaded H-bridges

The voltage waveform of the H-bridge cascaded cells does not contain a fundamental voltage component as they only compensate for the residual harmonic voltages generated by the two-level converter. Therefore, the average power exchanged with

the H-bridge cascaded cells is nominally zero, even though they are in the fundamental current path [53][59]. The voltage waveforms of the H-bridge cascaded cells is symmetrical, and hence, FB cells are employed. The use of FB cells also makes this topology capable of blocking DC faults.

The hybrid multilevel converter with AC side cascaded H-bridges requires a quarter of the submodules compared to the MMC and half of the submodules compared to the AAC [59]. On the downside, the losses in the hybrid converter with AC side cascaded H-bridges are higher than both the MMC and the AAC. Moreover, this topology also faces some of the issues associated with the two-level converter, such as the dynamic voltage balancing of the series-connected IGBTs.

2.4.5.3 Parallel-Hybrid Modular Multilevel Converter

The hybrid VSC topologies discussed so far employ a series connection of director switches and waveshaping circuits. Naturally, it is also possible to connect the waveshaping circuits and the director switches in parallel, which was first realised in the case of the Parallel Hybrid Modular Multilevel Converter (PH-MMC) [60] [61].

Depicted in Figure (2.25), each converter phase of the PH-MMC is composed of a parallel connection of an H-bridge based three-level director switch configuration and a waveshaping circuit based on a series connection of HB submodules. On the AC side, the converter phase units are interfaced to the AC network through three single-phase transformers, while on the DC side, the three phase units are connected in series to feed the DC transmission line.

The H-bridges in the PH-MMC are switched at the fundamental frequency. The string of HB cells are controlled to synthesise rectified AC voltages that are unfolded by the H-bridges to produce the sinusoidal, non-rectified AC output voltages. The rectified voltages produced by the three strings of HB cells are 120° displaced, resulting in a 6n ripple in the DC voltage, and hence, some filtering on the DC side

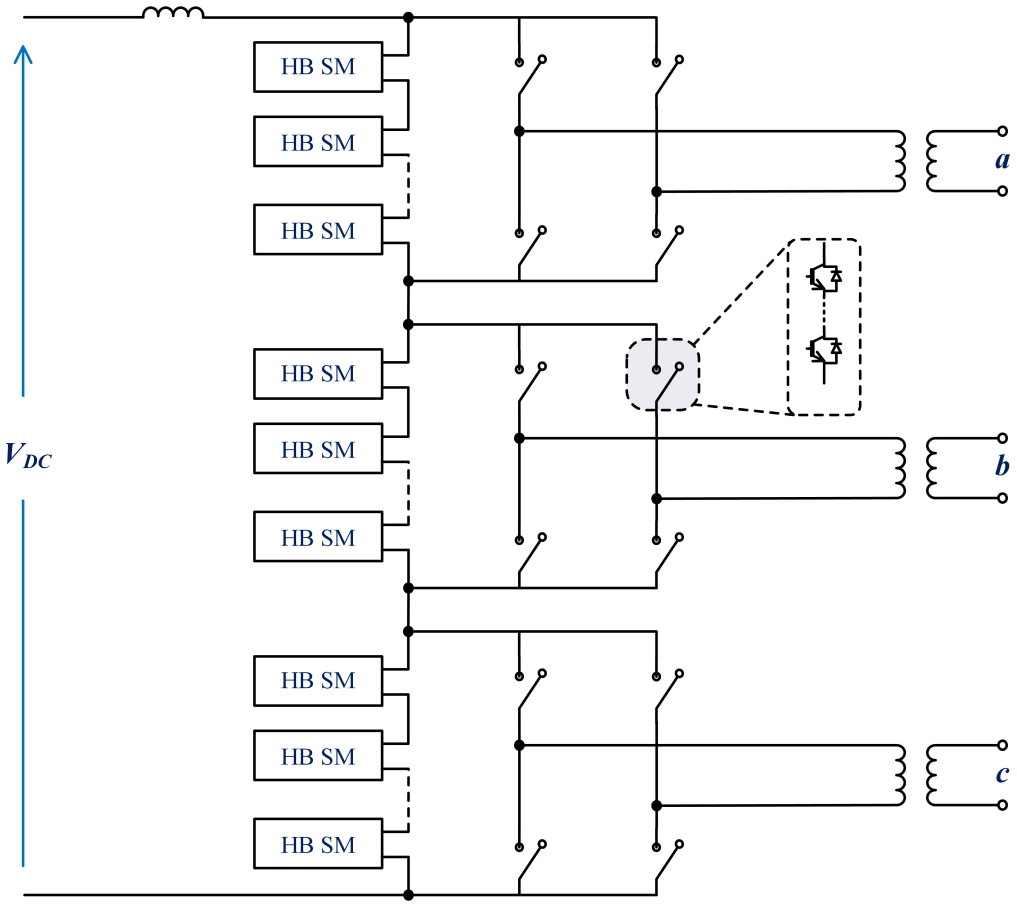


Figure 2.25: Schematic of the Parallel Hybrid Modular Multilevel Converter

is required. Another limitation of the PH-MMC is that the AC and DC voltages are coupled and the converter has a fixed modulation index of 1.05 [60]. Hence, for practical applications, the control of the AC output voltage is achieved by adding third harmonic components in the reference voltages [60].

In the PH-MMC, the series strings of HB cells sit outside of the main current path. This fact, combined with the fundamental frequency switching of the H-bridges, results in lower semiconductor losses. Moreover, compared with the MMC, only half the number of submodules are required in the PH-MMC, thus reducing the size and volume requirements of the converter. The drawback is the additional switches in the series-connected IGBTs that increase the overall semiconductor expenditure.

2.4.5.4 Series Bridge Converter

Another hybrid VSC, which is the extension of the PH-MMC, is the Series Bridge Converter (SBC) [62] [63]. The SBC, shown in Figure (2.26), has a similar structure as the PH-MMC, except with the difference of the use of an array of FB cells in series (termed as Series Full Bridges (SFBs)) between the string of HB cells (termed as Chainlink (CL)) and the "unfolding" H-bridge in each converter phase. The SFBs provide the function of decoupling the AC- and DC-side voltages and, in addition, are also utilised to obtain a ripple-free DC voltage. The theoretical voltage waveshaping of the CLs in the SBC can be seen in Figure (3.1).

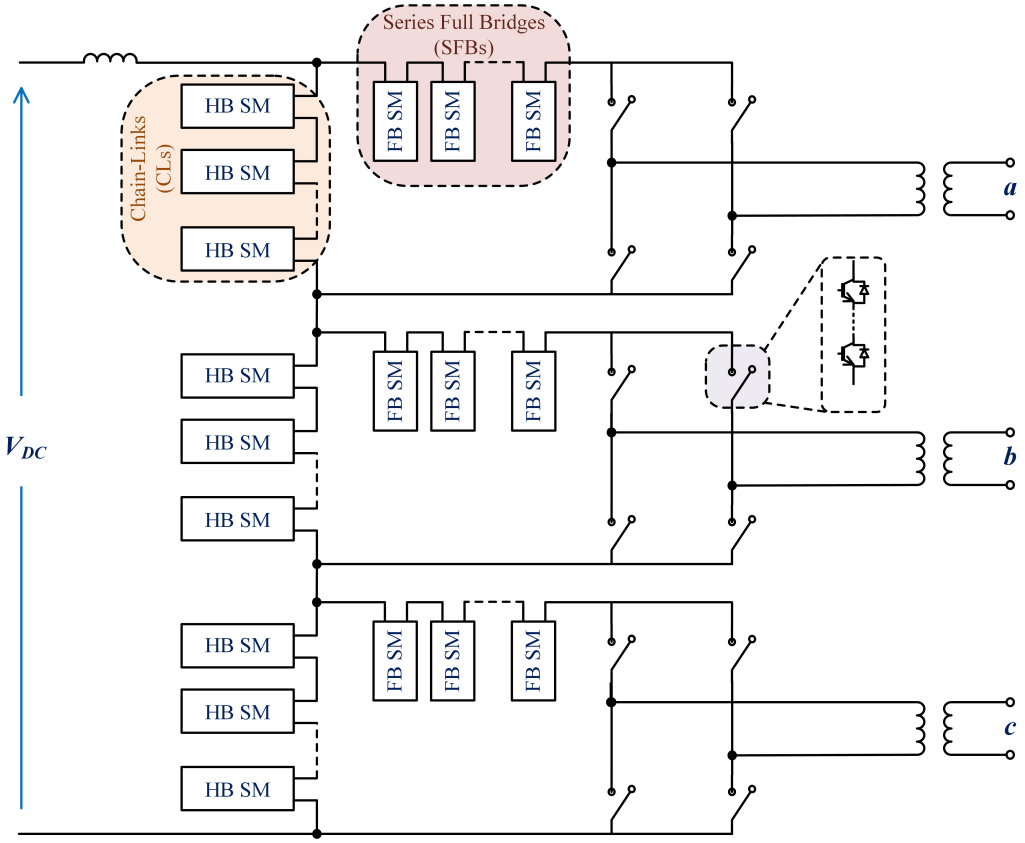


Figure 2.26: Schematic of the Series Bridge Converter

The addition of the SFBs in the SBC makes the internal energy control of the converter more challenging. The steady state average powers of the CL and the SFB in each converter phase are inherently non-zero, even when the converter losses and

component asymmetries are neglected [63]. Therefore, in order to ensure correct operation of the converter, a mechanism based on the addition of a second harmonic voltage component in the SFB voltage and the subtraction of the same component from the CL voltage is employed. The interaction of the added second harmonic voltage components with the second harmonic current components, that are common between the CL and the SFB, results in DC power terms that can be adjusted to drive the overall steady-state powers of the CL and the SFB individually to zero.

The SBC is an attractive topology for HVDC applications, especially in space-critical applications, such as offshore wind and city center infeed. In [64], a detailed comparison of the SBC and the MMC has been presented. It has been concluded that an SBC converter station will have a 51% smaller footprint, 62% lower volume and 22% smaller weight compared to an MMC converter station. These reduced figures in the SBC are a result of the need for much smaller capacitors and lesser number of submodules compared to the MMC.

2.5 Summary

In this chapter, a review of the HVDC transmission technology, its applications and future scope, basic classification of HVDC transmission technologies and a detailed review of major VSC topologies for HVDC transmission applications are presented.

The two distinct HVDC transmission technologies, LCC and VSC, are discussed, along with a comparison between the two. Since the new contribution of this thesis is in the area of novel VSC converters, the major part of this chapter is devoted to the discussion of different VSC topologies. The earlier two-level and multilevel converters are described, along with their drawbacks. The introduction of the MMC, as a topology that address the shortcomings of the earlier VSC topologies, is then highlighted, followed by the control of MMC and its operational challenges. Identifying the challenges of the MMC as the basis for further research in VSC topologies, the conception

of alternative submodule configurations and hybrid VSCs is then discussed. Finally, some of the most prominent hybrid VSCs are explained in detail including the AAC, the Hybrid Multilevel Converter with AC-side cascaded H-bridges, the PH-MMC and the SBC.

Chapter 3

Initially proposed topologies: PHBC & PCUB

3.1 Introduction

In the previous chapter, a brief overview of a few prominent existing hybrid VSCs was presented. In this chapter, the concepts for two new hybrid VSCs are derived and their drawbacks are discussed. To address these drawbacks, minor structural changes are proposed that lead to the "main" topology of this thesis. Hence, the conception of the main topology of this thesis, the Switched Mid-Point Converter (SMPC), is shown as a multi-staged process.

To avoid repetition of common concepts relevant to all the topologies, such as converter internal energy management and optimisation of certain parameters, the initial topologies presented in this chapter are only conceptually discussed emphasising the circuit design considerations. Although complete switching models with closed-loop control have been successfully developed to validate the ideas for all intermediate topologies, their details have been omitted from this thesis.

3.2 Motivation from the Series Bridge Converter (SBC)

The Series Bridge Converter (SBC) is an attractive hybrid VSC topology (discussed in Section (2.4.5.4)) which allows for a compact HVDC converter. However, one drawback, as discussed in [65], is that the AC fault performance of the SBC is relatively inferior when compared with other parallel-connected topologies like the MMC.

Since the SBC topology is still in its early stages of development, to the best of author's knowledge, the study in [65] is the only research work so far on its AC fault operation. According to this study, the required reduction in the converter AC-side voltages during AC faults in the SBC is difficult to achieve. In the SBC, the DC voltage is formed by the summation of the rectified three-phase CL (shunt-connected Chain-Link) voltages and hence, relies on their 'symmetricity' to produce a ripple-free DC voltage, given that other appropriate techniques are employed to remove the 6n ripple. Since the mean value and the amplitude of a rectified waveform are linked, a reduction in the CL voltage amplitude will affect its ability to generate its share of the DC voltage. Hence, if the same CL voltages as normal operation are synthesised during AC faults to keep the three-phase CL voltages symmetric, the voltage ratings of the Series Full-Bridges (SFBs), which are typically rated at $\frac{V_{DC}}{4}$ [64], will have to be increased to be able to handle AC voltage depressions, as depicted in Figure (3.1). Thus, the attractive benefits of the topology will be lost.

Also in the study in [65], a method that uses trapezoidal alternating components in the CLs during AC faults is proposed and the voltage distribution between the converter phases is managed based on the AC fault type while making sure that they sum up to the DC network voltage. Even with this solution, the power transfer capabilities are limited and in extreme cases such as a severe single-phase fault, the only option is to isolate the faulty phase from the DC side [65].

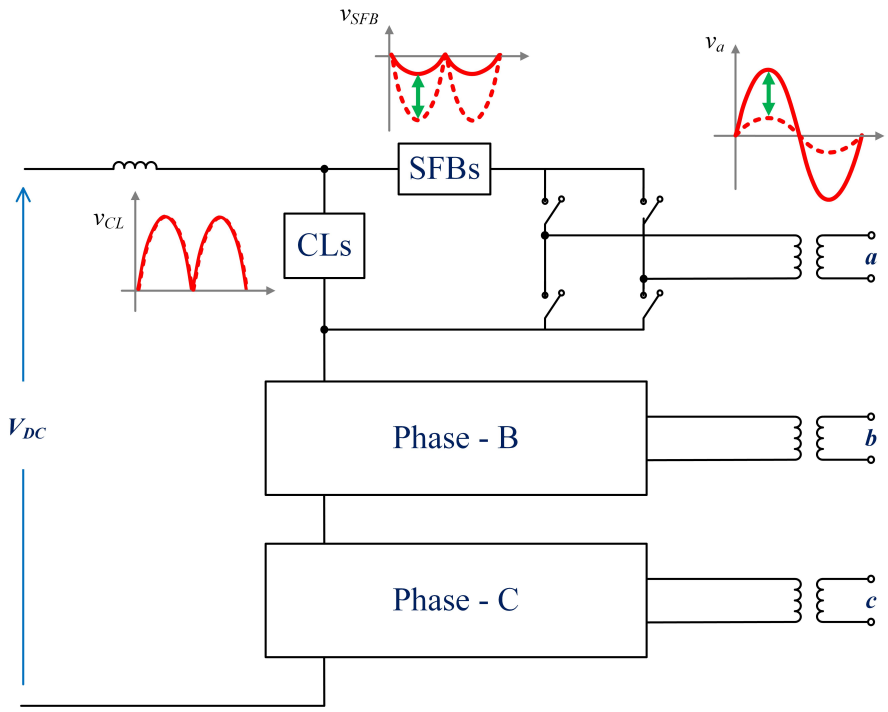


Figure 3.1: Illustration of the requirement to over-rate SFBs to handle AC voltage depressions in the SBC

The rectified waveforms of the chainlinks in the SBC lead to smaller submodule capacitances since the fundamental frequency of the instantaneous power ripple in the CL/SFB is twice the AC fundamental frequency [63]. In order to retain this benefit and considering that a parallel connection of converter phases across the DC side may provide better AC fault performance (from the experience of the MMC and other parallel-connected topologies), the starting point of the investigation undertaken in this thesis is based on deriving a new topology that uses the SBC structure, except with the difference of a parallel connection of converter phases across the DC side. The resulting topology is titled the 'Parallel H-Bridge Converter (PHBC)'.

3.3 Parallel H-Bridge Converter (PHBC)

Similar to the SBC, the PHBC topology is a hybrid circuit that employs a three-level converter along with wave shaping circuits. The three-phase configuration of the

converter is presented in Figure (3.2). Like the MMC and AAC, the three phases of the PHBC are connected in parallel across the DC side voltage. Each phase consists of a DC-side reactor, two chainlink (CL) arms and an 'unfolding' H-bridge configuration which is interfaced to the AC network through a transformer arrangement. The shunt-connected CLs, termed 'Longitudinal Chainlinks (LCs)', are based on a series connection of half-bridge (HB) SMs and the series-connected CLs, named 'Transverse Chainlinks (TCs)', are formed using a series connection of full-bridge (FB) SMs. Both the LCs and TCs are responsible for synthesising a variable amplitude, full wave rectified, multilevel voltage waveform that is 'unfolded' by the H-bridge at the zero crossings to generate the AC side voltage. The switches in the unfolding H-bridge are formed by a series string of IGBTs.

The concept of operation of the PHBC is to synthesise multilevel voltage waveforms at the output using an H-bridge arrangement. A conventional three-level H-bridge arrangement using a DC voltage source, shown in Figure (3.3a), has three output levels: V_{DC}, 0 and $-V_{DC}$. If the DC voltage source is replaced by a full-wave rectified multilevel DC waveform source, as depicted in Figure (3.3b), the output of the H-bridge arrangement is a multilevel AC waveform that closely approximates a sinusoidal waveform. In the PHBC, the rectified multilevel DC waveform source is a combination of the LCs and the TCs.

Since the LCs are responsible for supporting the full DC voltage, the mean value of the LC voltage is imposed by the DC side. Given that the LCs are required to synthesise a full-wave rectified voltage, the amplitude of the LC voltage, $\hat{V}_{LC}$, is fixed at $\frac{\pi V_{DC}}{2}$. Hence, the TCs serve the purpose of decoupling the converter AC output voltage from v_{LC} by providing appropriate attenuation such that the voltage generated at the DC side terminals of the H-bridge arrangement is in accordance with the required converter output at the transformer secondary (converter side). The attenuation demanded from the TCs can be adjusted to facilitate reactive power exchange.

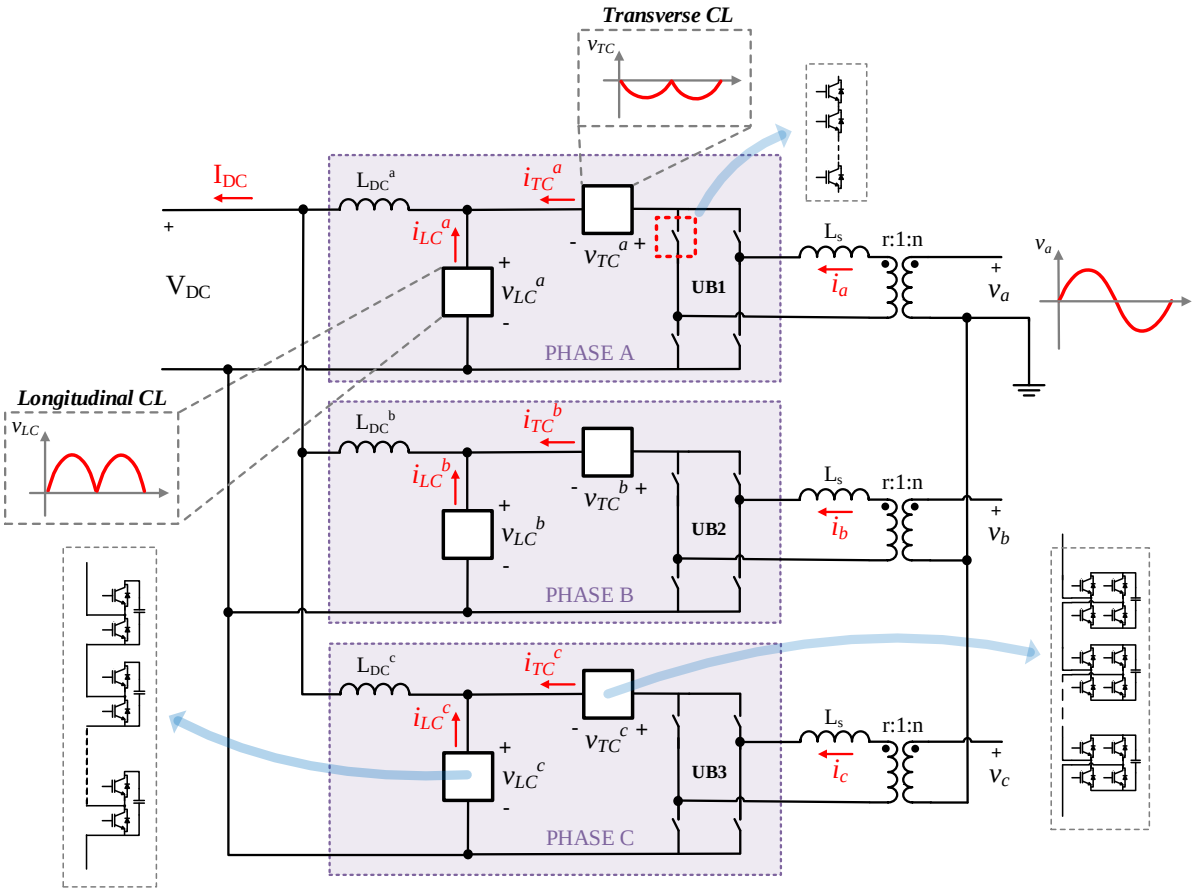


Figure 3.2: PHBC converter topology

Considering a hypothetical case in which the TCs are removed, the peak converter AC voltage will be $\frac{\pi V_{DC}}{2}$. Using the general definition of modulation index (MI) as the ratio between peak converter AC voltage and half of the DC voltage, the MI in the case of PHBC is equal to π. This means that considerable voltage attenuation is required to interface the converter to the AC grid as the AC and DC voltage levels in practice are chosen such that the MI is close to 1. The TCs should ideally only provide attenuation to regulate power flow since they are in the main current path and are formed of FBs. Rating them to provide full attenuation will lead to a massive increase in losses and device count. Hence, the ratio of transformer turns i.e $\frac{r}{n}$ in Figure (3.2) is selected as π to make the interface possible with the AC grid. However, the drawback is that the voltage ratings of the unfolding H-bridges are high resulting in high conduction losses and device count there.

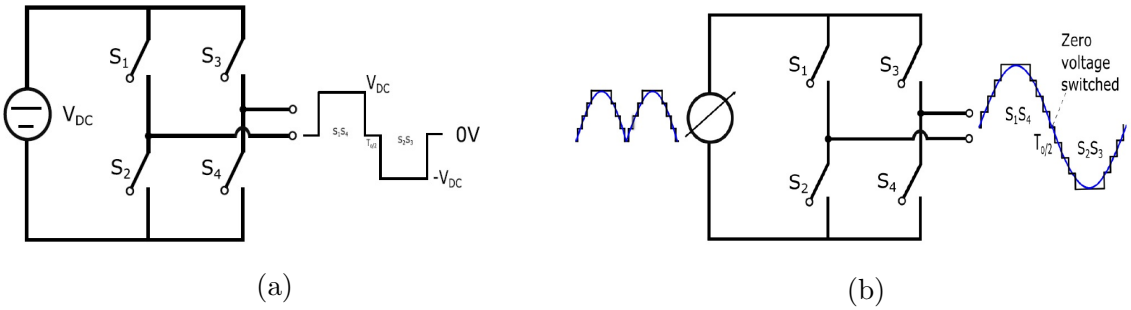


Figure 3.3: (a) H-bridge with a constant DC source (b) H-bridge with a multilevel DC source [3]

The idealised voltage synthesised by the LCs, a full-wave rectified waveform, is composed of even harmonics of quadratically decaying amplitudes with the 2nd harmonic being the largest. The equivalent circuit on the DC side, considering only the harmonics, can be imagined as a connection of multiple even harmonic voltage sources with the DC smoothing inductor, L_{DC}, in each phase as depicted in Figure (3.4). In this figure, the appearance of a short-circuit on the DC side is due to the omission of both the DC voltage and the DC terms of the CLs to illustrate only the effect of CL even harmonics on the sizing of the smoothing reactor. Hence, the circuit in Figure (3.4) cannot be directly used for rating the reactors.

In Figure (3.4), although all the even harmonics, with the exception of the 6n harmonics, cancel out on the DC network in a balanced three-phase system, they are present in the current that flows inside the converter phases. The magnitudes of the harmonics in this current are dependent on the value of L_{DC} and impact the current rating of the devices and capacitor sizes in the LC. Using an averaged model of the converter for a 20 MW, 20 kV DC - 11kV AC system, it has been estimated that in order to keep the LC current within margins that are practically feasible in terms of device ratings and capacitor sizes, the value of L_{DC} has to be between 30 mH - 40 mH. In comparison, for the MMC, the arm reactor values reported in [66] from a survey of multiple references are between 1 mH - 5 mH. The requirement of large DC

smoothing reactors in each converter phase renders the PHBC topology ineffective for HVDC applications in comparison with existing multilevel topologies.

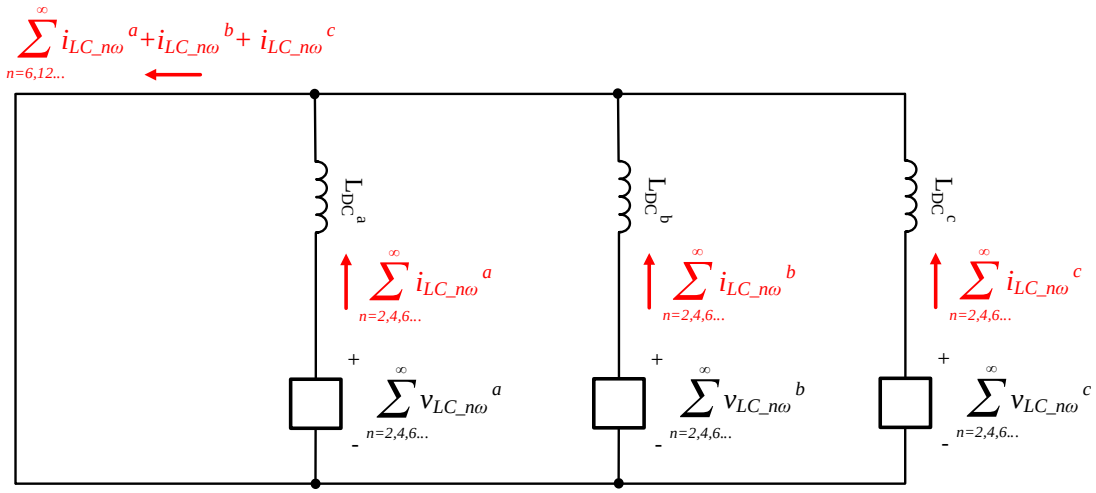


Figure 3.4: DC side equivalent circuit considering harmonics only

Moreover, there are insignificant benefits achieved over the SBC under AC fault conditions. Achieving the required reduction in the converter AC-side voltage during AC under-voltage conditions without over-sizing the TCs is also still difficult. However, due to the parallel connection of the converter phases across the DC side, if the faulty phase is to be isolated, the LCs in the healthy phases do not need to be over-rated.

The main drawbacks of the PHBC topology are summarised below:

- High voltage ratings of the unfolding H-bridges
- Massive size of the DC smoothing reactors
- Difficulty in achieving output voltage reduction during AC faults

In order to reduce the size of the DC smoothing reactor, a possible solution considered is the use of an additional transverse CL in series with the DC reactor. This CL behaves like an 'electronic inductor' and thus, is named the 'Electronic Inductor CL'

(ELC). The function of the ELC is to cancel out selective harmonic components produced by the LC on the DC side. Firstly, the 2nd harmonic is removed as it is the largest in size and removing it lowers the DC reactor value considerably. Secondly, the 6th harmonic is cancelled out since it is zero-sequence and appears in the summation of a balanced three-phase system if not removed. The concept is illustrated for a single-phase PHBC circuit in Figure (3.5). The voltage to be synthesised by the ELC is an addition of the 2nd and 6th harmonic voltages whose magnitude and phase angles have to be carefully chosen to match those in the LC voltage. Since the ELC generates AC components with equal positive and negative voltage levels, it is composed of series-connected FBs.

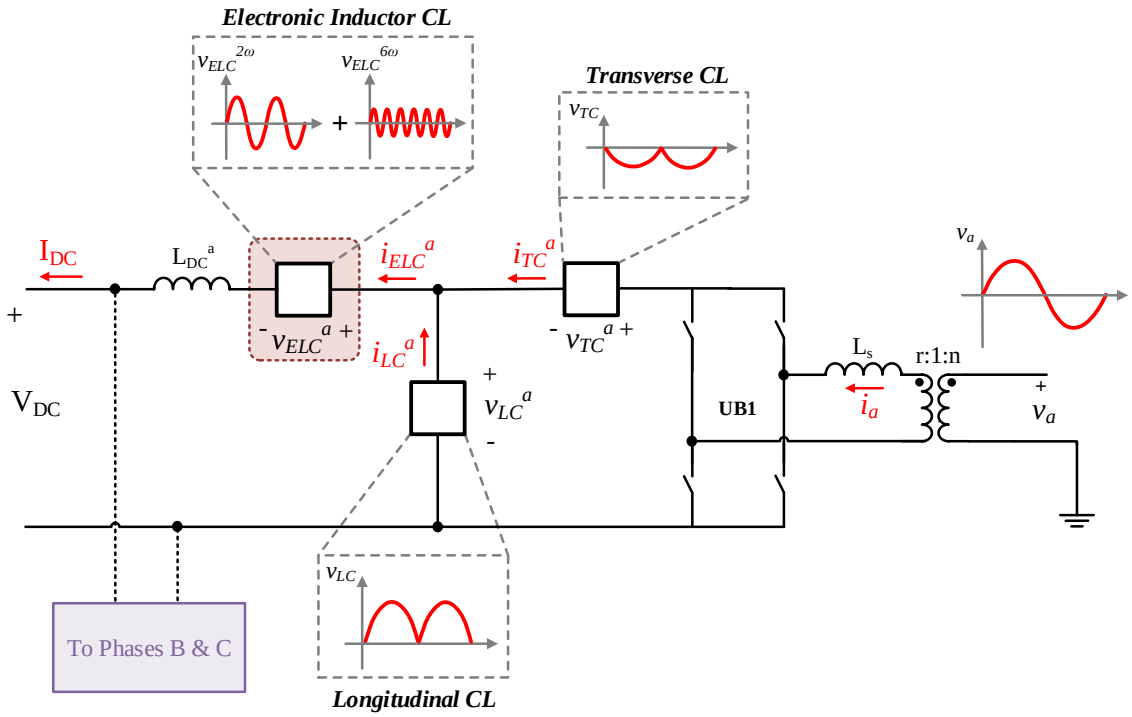


Figure 3.5: Single-phase PHBC circuit with the ELC

The inclusion of the ELC in the PHBC topology reduces the required DC smoothing reactor value, for ensuring practically feasible margins of the LC current, to around 2 mH - 5 mH. The obvious downside, however, is the extra number of FB SMs in the ELC resulting in a higher device count and higher conduction losses. In fact, the

number of SMs per phase are increased by around 40% compared to the case of the PHBC without the ELC.

As mentioned earlier, the ELC in Figure (3.5) produces purely AC components. However, it is possible to assign a different function to the ELCs by utilising them to produce some DC voltage and, in addition, eliminate all the harmonics presented by the LC on the DC side. This new function of the ELC results in the following changes:

- The LC voltage is no longer imposed by the DC side voltage. This means that the LC voltage can be freely synthesised according to the AC operating point requirements. As a result, the TCs are no longer needed to obtain the control of the AC output voltage, and hence, the TCs can be removed from the circuit.
- There is more control over the MI and it becomes possible to operate at MIs lower than π, leading to relatively smaller ratings of the unfolding H-bridges
- Achieving the required reduction in the converter AC-side voltage during AC faults becomes possible, given again that the ELCs are appropriately rated.

Moreover, the benefit of a reduced DC smoothing reactor is retained since the even harmonics are completely eliminated by the ELC. The aforementioned change in the utilisation of the ELC leads to a new intermediate topology that is called the 'Parallel-connected Converter with Unfolding Bridges (PCUB)' and is the subject of the next subsection.

3.4 Parallel-connected Converter with Unfolding Bridges (PCUB)

The PCUB circuit is shown in Figure (3.6). Since the ELCs now do not just behave as an 'electronic inductor' but rather produce some DC voltage too, the name for these

CLs is changed to Transverse CLs (TCs). Similar to the PHBC, the converter phases connect in parallel across the DC side and each phase has its own DC reactor and 'unfolding' H-bridge, interfaced to the AC side through a single-phase transformer and two waveshaping CLs, the LC and the TC. The LC is formed of series-connected HBs whereas the TC is composed of a series connection of FBs. As mentioned before, the position of the TC is the main difference between the PHBC and the PCUB.

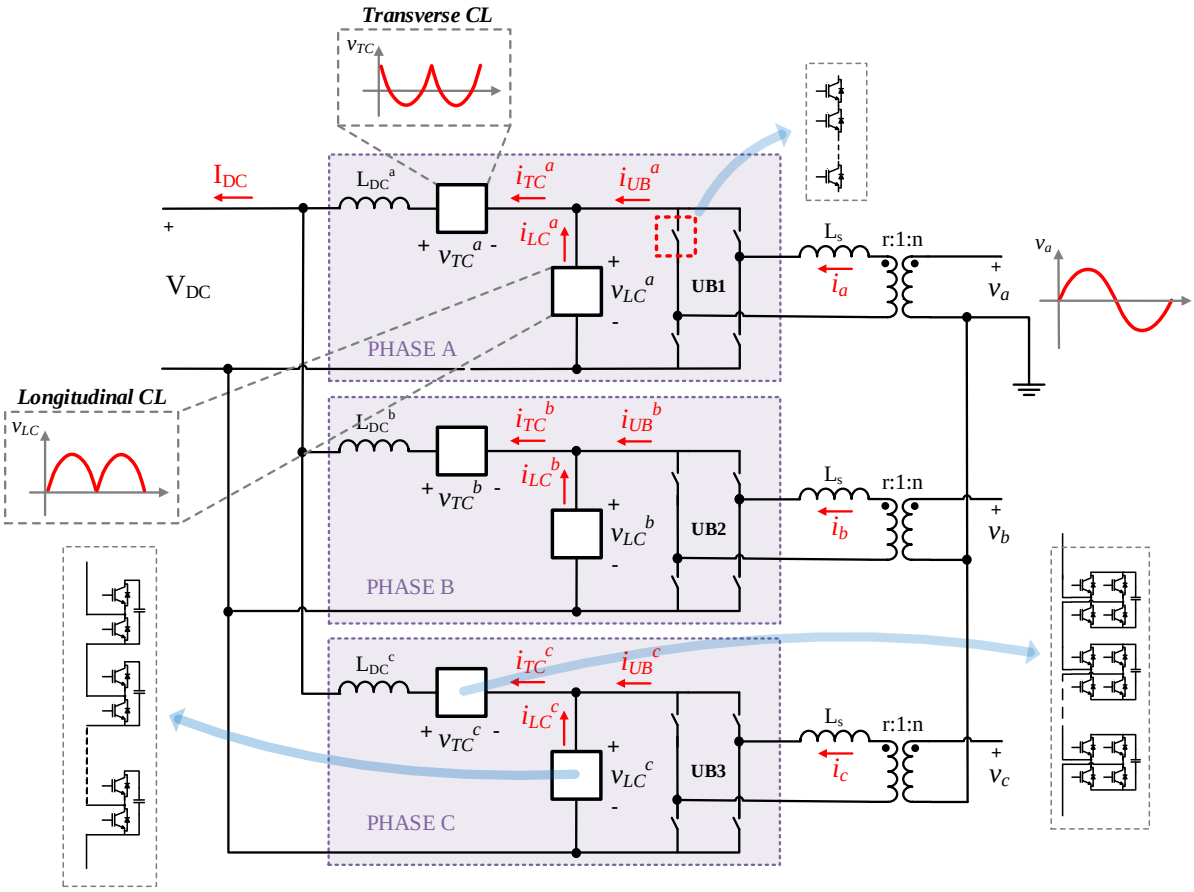


Figure 3.6: PCUB converter topology

In terms of operation of the converter, the LCs are used to synthesise a full-wave rectified multilevel voltage waveform, the peak value of which is imposed by the AC side P-Q operating point. This rectified multilevel waveform is 'unfolded' by the H-bridge at the zero crossings to generate the AC side voltage. The LC voltage can

thus be expressed generically for an arbitrary phase 'x' as:

$$v_{LC}^{x} = r \cdot |v_x|$$
$$v_{LC}^{x} = \frac{2r\hat{V}}{\pi} + \sum_{n=2,4,6..}^{\infty} v_{LC_{n\omega}}^{x}$$

where v_x and $\hat{V}$ are the instantaneous and peak AC voltages respectively at the network side of the transformer (primary) and 'r' is the turns ratio of the transformer (n=1 in Figure (3.6)).

The TC voltage is thus synthesised such that the remaining portion of the DC voltage is supported and all the AC components in the LC are cancelled out. Thus, it can be generically expressed as:

$$v_{TC}^{x} = \underbrace{\left(V_{DC} - \frac{2r\hat{V}}{\pi}\right)}_{\substack{\text{Remainder DC} \\ \text{voltage support}}} - \overbrace{\sum_{n=2,4,6..}^{\infty} v_{LC_{n\omega}}^{x}}^{\substack{\text{Full AC} \\ \text{cancellation}}}$$

Due to the parallel connection of converter phases across the DC side, one-third of the DC current flows in each phase. Since the TC aims to cancel out all the AC voltage components of the LC, only DC current flows in the TC. Because of the unfolding action, the current at the input of the UB, i_{UB}, is the full-wave rectification of the AC current on the transformer secondary with the required phase-shift in case of reactive power. The current through the LC is then the difference between i_{UB} and the TC current. The currents can be expressed generically as follows:

$$i_{LC}^{x} = \begin{cases} \frac{i_x}{r} - \frac{I_{DC}}{3} & 0 \leq t \leq \frac{\pi}{\omega} \\ -\frac{i_x}{r} - \frac{I_{DC}}{3} & \frac{-\pi}{\omega} \leq t \leq 0 \end{cases}$$

$$i_{TC}^{x} = \frac{I_{DC}}{3}$$

where i_x is the instantaneous AC current at the network side of the transformer.

As a result of the full-wave rectification stage at the UB which causes DC and even harmonics to flow inside the converter CLs, the average powers in the CLs are not inherently zero. Non-zero average CL powers will result in uncontrolled capacitor charging/discharging. Thus, in order to operate the converter successfully, the CL average powers have to be regulated to zero by injecting a common control variable in both the TC and the LC that transfers energy between the two CLs. In the PCUB, identifying that the even harmonic voltages in the LC and the TC are in phase opposition, driving common even harmonic currents through the two CLs will dissipate equal and opposite mean powers in them, achieving the desired effect. As mentioned earlier, in the interest of avoiding duplication, the concept of energy management and second harmonic injection for the PCUB is only briefly discussed here. For more details on the subject, the reader can refer to [67] or Section (4.4) of this thesis.

For the PCUB, only the injection of a second harmonic current, $i_{2\omega}$, is proposed. Since the LC voltage is imposed by the AC side and no additions can be made to it, $i_{2\omega}$ is driven by adding 2ω components only in the TC voltage. Thus, the TC voltage can be re-expressed as:

$$v_{TC}^{x} = \left(V_{DC} - \frac{2r\hat{V}_c}{\pi} \right) - \sum_{n=2,4,6..}^{\infty} v_{LC_{n\omega}}^{x} + v_{2\omega}^{bal}$$

In terms of CL ratings, the LCs should be rated for the peak AC voltage multiplied by 'r'. For the TCs, although the balancing 2ω voltage addition will modify the appearance of the waveforms, the maximum voltage that these CLs need to produce will always be the full DC voltage, hence they are rated for V_{DC}. Since any value for the MI of the converter (between a certain range) is achievable theoretically, the turn ratio 'r' can be optimised to achieve minimisation of certain parameters. In the case of the PCUB, selection of 'r' based on the minimisation of the converter's stored energy is proposed. Again, the details of the turn ratio optimisation method are omitted here, but can found in [67] or Section (4.5.4) of this thesis (where the relevant discussion is framed in terms of the optimisation of the modulation index).

However, the result of the analysis is presented in Figure (3.7) which shows that the stored energy inside the converter minimises at a turns ratio value of 2.44 (which corresponds to a modulation index value of 2.19 for the 20kV DC - 11kV AC voltage ratings used for the analysis). At this turns ratio, the stored energy inside the converter for a 20 MW system is 131.3 kJ and the H-constant (H_c) can be calculated as follows:

$$H_c = \frac{E_{stored}}{P_{rated}} = 6.6 \text{ kJ/MW}$$

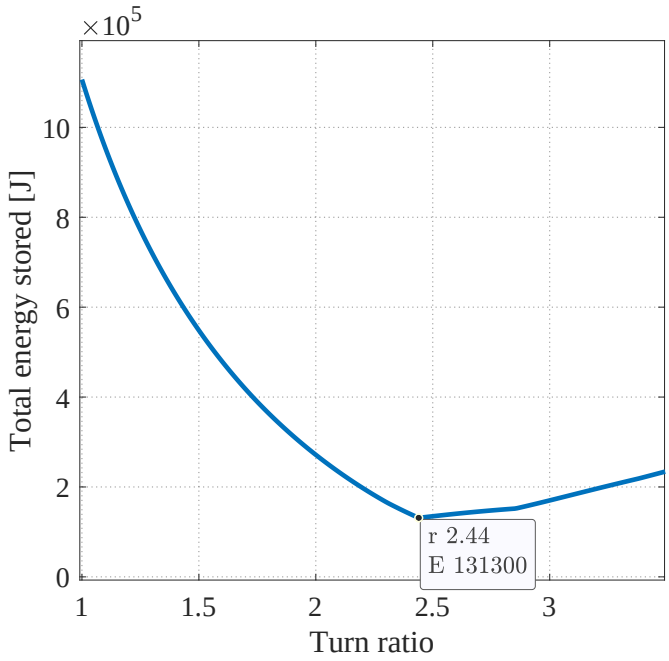


Figure 3.7: Worst-case stored energy for varying turns ratios

More detailed comments on the H-constant can be found in Section (4.5.4) of this thesis. The value of H-constant calculated above for the PCUB is 4-5 times smaller than that of the MMC. Although the number of total SMs needed per phase in the PCUB are comparable to that in the MMC, the smaller energy storage is due to small SM capacitors in the PCUB. In [67], it has been noted that the SM capacitances, for a 20 MW, 20kV DC - 11 KV AC system with a 20% peak-to-peak ripple factor, are 1.9 mF and 0.8 mF for the LC and the TC respectively. In fact, the SM capacitor sizes in the PCUB, when operated at the optimum '$r = 2.44$', are even smaller than those in the SBC (between 3 mF - 4 mF are reported in [62] for similar voltage

and power ratings) which explains why the PCUB has a comparable energy storage requirement to the SBC, even with a higher number of SMs needed in its CLs.

The drawback of the PCUB is that the minimised energy storage requirement is tied to the optimum turns ratio operation. As mentioned before in the case of the PHBC, a high turns ratio (effectively a higher modulation index) results in high voltage ratings of the UBs, leading to higher semiconductor requirement. If 'r' is reduced (thereby lowering the modulation index) to enable lower voltage ratings of the UBs, the stored energy requirement will rise, as can be seen from Figure (3.7), and the attractive benefit of smaller capacitor sizes will be lost, which in turn will be a compromise on the compactness of the converter.

It is important here to make some comments on the fault performance of the PCUB. In the case of AC faults, the converter is capable of reducing the AC output voltage since the LC voltage can be synthesised according to the required reduction. The TCs are capable of supporting the DC voltage on their own since they are rated for V_{DC}, and can also easily provide the desired AC harmonic cancellation under reduced AC converter voltage. In the case of severe single-phase AC faults, continued operation can be achieved without isolating the faulty phase. Moreover, the PCUB can potentially provide DC fault blocking because of the presence of FBs in the TCs, which will typically be rated high enough to counter the AC side voltage during a DC fault. A detailed investigation of the fault performance of the PCUB is the subject of future work.

Although the PCUB itself is an attractive topology for HVDC, particulary because of the lower energy storage requirement and better fault performance, the high voltage ratings of the UBs limit its practical use as they result in higher losses and a higher semiconductor expenditure. Hence, it is imperative to keep the voltage ratings of the UBs low and that is the driving factor behind the conception of the final topology presented in this thesis, the SMPC.

A minor restructuring of the PCUB topology is proposed based on the idea of replacing the H-bridge in the UB with a half-bridge. Since the half bridge has only one output terminal, the converter has a floating output in this case, similar to the MMC, which can be referred to a fictitious mid-point on the DC voltage as shown in the single-phase representation of the restructured topology in Figure (3.8). Moreover, the TCs are split into two CLs, one connected to the positive DC terminal and the other to the negative DC terminal through separate reactors in both cases.

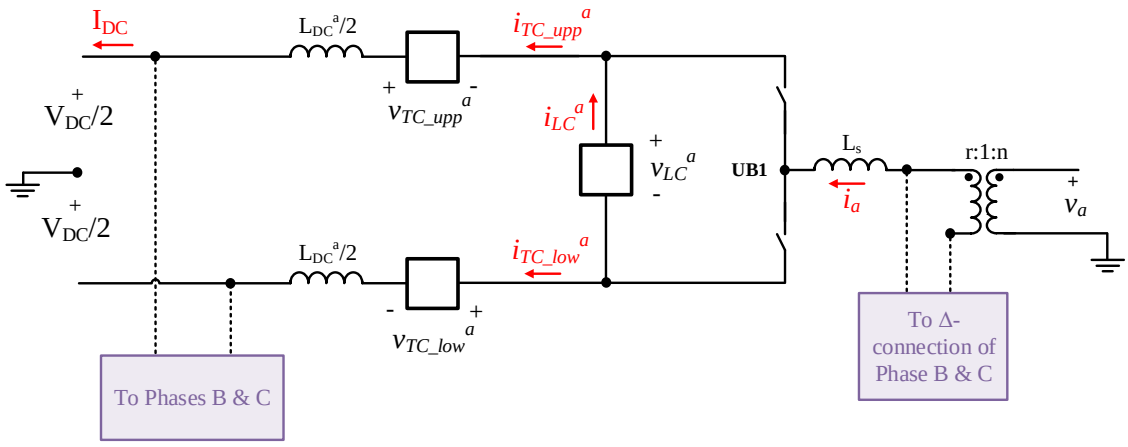


Figure 3.8: Single-phase representation of the restructured topology

Despite the structural similarity to the PCUB, the working principle of the restructured topology in Figure (3.8) is quite different and hence, the voltage waveshaping of the CLs needs to be reconsidered. The topology based on the single-phase structure in Figure (3.8) is titled the 'Switched Mid-Point Multilevel Converter (SMPC)' which is the main and final topology proposed in this thesis.

3.5 Summary

In this brief chapter, two topologies developed in the initial stages of this PhD work, the PHBC and the PCUB are introduced. To avoid taking the focus away from the main/final topology explained in Chapter 4, both the topologies presented in this

chapter are only theoretically discussed. Emphasis has been placed on identifying the key problems with the topologies and proposing structural changes to alleviate these issues.

The discussion in this chapter starts with highlighting the comparatively inferior AC fault performance of the SBC. This is established as the primary motivation for investigating a new circuit configuration using the SBC single-phase structure in a parallel connection of converter phases across the DC side. This circuit, named the PHBC, is discovered to have a number of drawbacks - namely the massive size of the DC smoothing reactors in each phase, high voltage ratings of the UBs and unsatisfactory AC fault performance. To reduce the DC reactor size, the addition of the ELC is then proposed, in series with the reactor, to cancel out the 2nd and 6th voltage harmonics produced by the LC on the DC side. This brings the value of L_{DC} to an acceptable range but at the cost of higher device count and conduction losses.

The idea of utilising the ELC to support some part of the DC voltage is then proposed, which leads to the PCUB topology. In addition, all the even harmonics presented by the LC on the DC side are also cancelled. The TCs from the original PHBC circuit are no longer needed in the PCUB. It is shown that the PCUB is an attractive topology for HVDC applications, thanks to the small energy storage requirement at an optimised transformer turns ratio, and better fault performance. The H-constant is calculated to be 4-5 times smaller than that of the MMC and roughly similar to that of the SBC. A limitation of the PCUB in terms of the minimised energy storage being linked with the optimum turn ratio operation is identified. Due to the optimum turns ratio being a high value (2.44), it leads to high voltage ratings of the UBs that limit the practical use of the PCUB. As a solution, the final proposal is to replace the H-bridge in the UB with a half-bridge and split the TC into two CLs resulting in a new topology named the SMPC. The SMPC is the main topology proposed in this thesis and is the subject of the rest of the thesis.

Chapter 4

Switched Mid-Point Converter (SMPC): Basic Operation and Analysis

4.1 Introduction

Hybrid VSC topologies have shown promise in meeting emerging needs of the HVDC market. Topologies such as the Parallel Hybrid Modular Multilevel Converter [60] and the Series Bridge Converter [62] require only half the number of submodules compared to the MMC which makes them very attractive for applications where smaller footprints are essential, such as offshore converter platforms. Other topologies like the Alternate Arm Converter [55] and the Hybrid Multilevel Converter with AC-side cascaded H-bridges [68] provide the benefit of DC fault-ride through without much compromise on the efficiency or on the volume/size of the converter. During DC faults, they are able to stay connected and provide reactive power support to the grid.

In the previous chapter, two hybrid VSC topologies proposed as part of this PhD work, namely the PHBC and the PCUB were discussed. Moreover, a brief account of the process of arriving at the main topology, the SMPC, was given. In this chapter,

the SMPC is explained in detail and a complete analysis of the converter during ideal grid conditions as well as during fault scenarios is presented. Initially, the basic structure of the topology and the operating principle is described. Then, the mathematical equations for the electrical quantities are derived and the issue of energy management, along with a proposed solution, is discussed. Following that, the sizing of converter parameters is presented and a methodology for optimising the converter operation is developed. A comparison of the SMPC with MMC in terms of the number of SMs, capacitor sizes, energy storage and losses is then detailed. Finally, the behaviour of the converter under AC and DC fault conditions is discussed.

4.2 Description of the topology

The SMPC incorporates features of both two-level and multilevel converter topologies and hence, can be classified as a Hybrid VSC. As shown in Figure (4.1), each converter phase in the SMPC is connected in parallel across the DC side.

Each phase consists of a two-level director switch (DS) configuration, two arm reactors and three waveshaping chainlinks, namely upper (UPP), middle (MID) and lower (LOW) chainlinks (CLs). The DSs are switched at AC line frequency and the waveshaping CLs generate multilevel voltage waveforms such that in each phase-leg, (1) the AC side voltage is produced at the centre point of the DS configuration and (2) all the AC components are cancelled on the DC side. In order to achieve sufficient voltage ratings, the DSs are composed of a series string of IGBTs. To avoid a short-circuit through the anti-parallel diodes of the DSs, the voltage across the MID CL terminals must never be negative. Thus, the MID CLs are required to produce positive voltage levels only and are formed by a series connection of half-bridge (HB) cells. As will be shown in the subsequent sections, for the internal energy of the converter to naturally balance, the modulation index, i.e. the ratio of the peak AC voltage to half the DC voltage, is $\frac{\pi}{2}$ which requires the converter to operate in

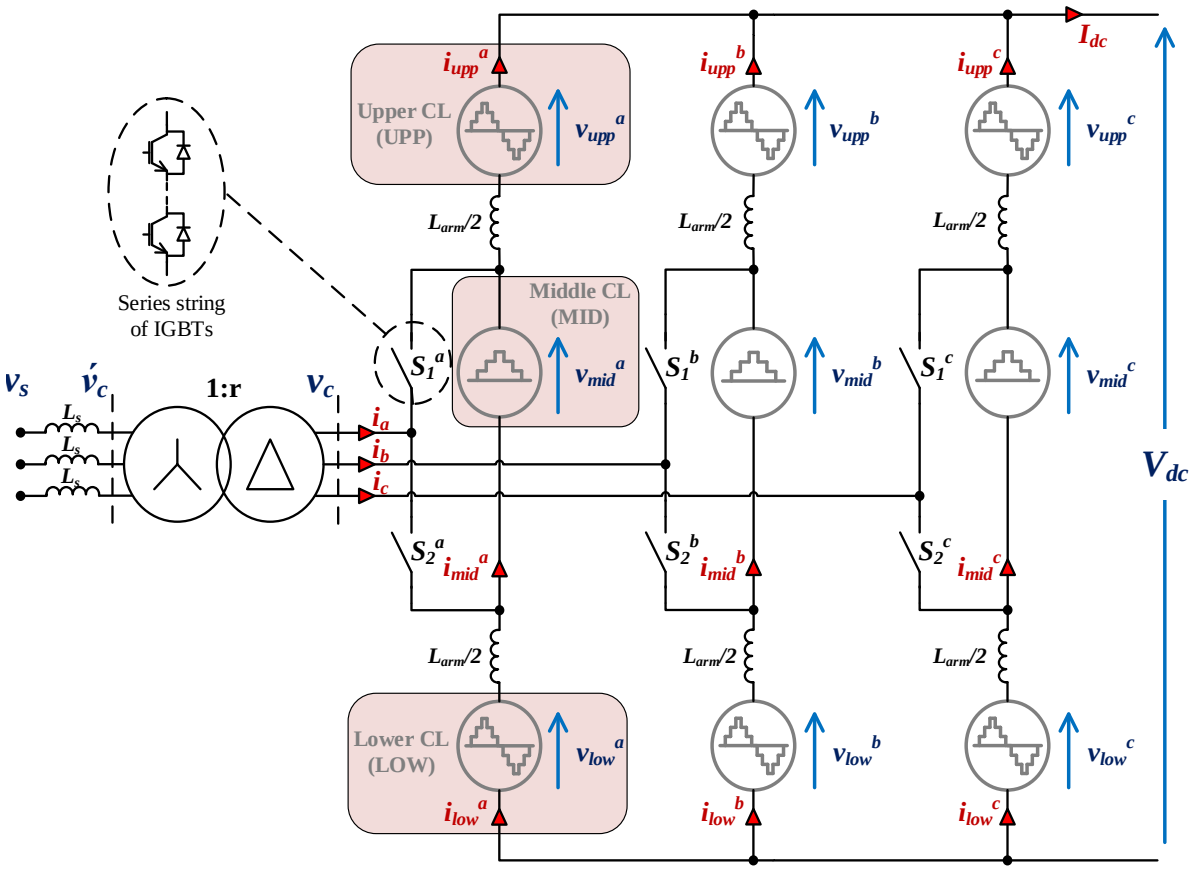


Figure 4.1: SMPC converter topology

over-modulation. For this reason, the UPP and LOW CLs are required to synthesise both positive and negative voltage levels. Two possible formations for UPP and LOW CLs are considered - (1) a series connection of full-bridge (FB) cells and (2) *'hybrid chainlinks'* that are formed by connecting both HBs and FBs in series in the same chainlink. In this thesis, the use of hybrid chainlinks in UPP/LOW CLs is proposed for the converter as a general recommendation because of reasons discussed later in Section (4.6) whereas for the experimental work, only FB cells are used in UPP/LOW CLs due to practical limitations. However, the basic waveshaping analysis and control design is based on the averaged waveforms (no switching considered) synthesised by the UPP/LOW CL as a whole and hence, is independent of the choice of cell formation. The electrical schematics of the symbols used to represent the CLs are illustrated in Figure (4.2).

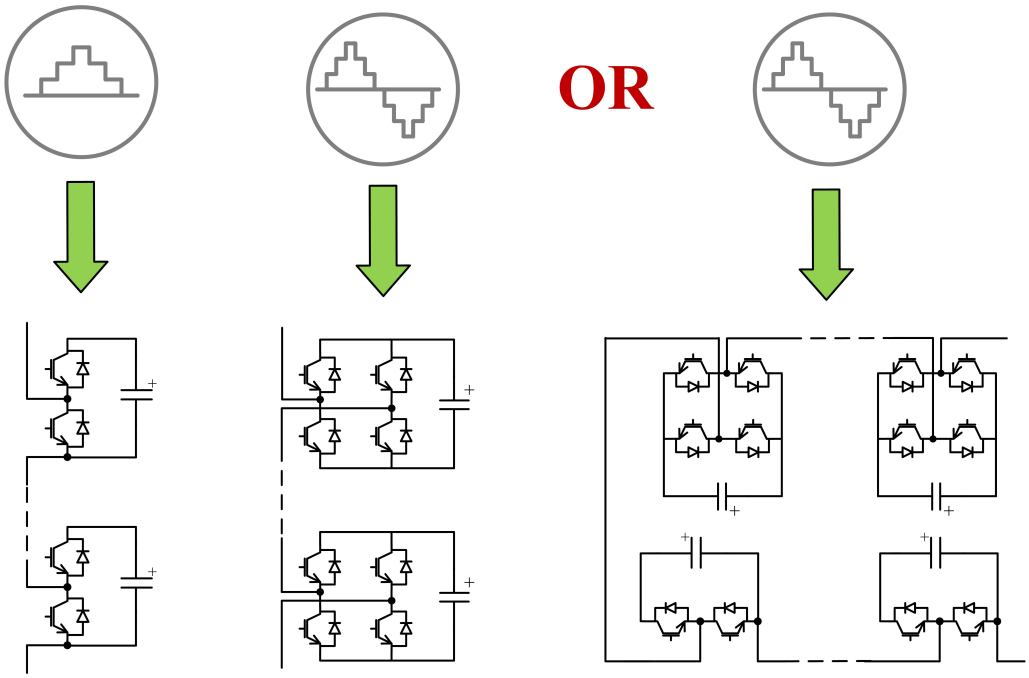


Figure 4.2: Electrical schematics of MID CL and UPP/LOW CL

On the AC side, the converter is interfaced to the AC system through a star-delta transformer with a generic turns-ratio value *'r'*. It is worth mentioning here that in principle, the SMPC, like the MMC, is a transformer-less topology as the transformer is not essentially needed to operate the circuit. However, in practice, a transformer is needed in most HVDC applications to meet system requirements and to provide isolation [69]. In the analysis part of this thesis, the turns-ratio of the transformer is used to adjust the AC voltage on the converter side. The AC line/transformer leakage reactance L_s in Figure (4.1) is neglected for the theoretical analysis presented in this chapter as the variations in v_c' for a given P-Q range are small in normal operation. Hence, it is assumed that v_c' is constant and equal to v_s. Operation at different P-Q points is modelled by setting the amplitude and phase of the supply currents with respect to the converter terminal voltage.

4.3 Operating Principle

Although each phase of the SMPC is composed of three waveshaping CLs, the operation of the converter can be more intuitively understood by considering a two-arm operation with each phase-leg divided into upper and lower arms (not to be confused with 'UPP' and 'LOW' that are used to refer to the CLs in the text), quite similar to a standard MMC. The two strings of IGBTs in the DS configuration (S_1 *and* S_2) switch the placement of the MID CL between upper and lower arms alternately over one fundamental cycle. This means that in the positive AC half cycle, when the devices in S_1 in Figure (4.1) are turned on, MID and LOW CLs constitute the lower arm while the UPP CL forms the upper arm. Alternatively, in the negative AC half cycle, the MID and UPP CLs constitute the upper arm while the LOW CL forms the lower arm. This is illustrated in Figures (4.3a) and (4.3b) using single-phase representations of the topology where the DS configuration is omitted intentionally for a better visualisation of the two-arm operation.

For the case when switch S_1 in Figure (4.1) is on, the voltage equations for the positive and negative poles of the DC circuit in Figure (4.3a) can be written as:

$$-v_c + \frac{L_{arm}}{2}\frac{d}{dt}i_{upp} - v_{upp} + \frac{V_{dc}}{2} = 0 \tag{4.1}$$

$$-v_c - \frac{L_{arm}}{2}\frac{d}{dt}i_{low} + v_{low} + v_{mid} - \frac{V_{dc}}{2} = 0 \tag{4.2}$$

For the purpose of determining the basic voltage wave-shaping of the CLs in each phase-leg of the SMPC, the voltage drops due to the arm inductances are ignored. This is a fair assumption since an accurate design of the AC and DC side control loops will ensure the generation of correct voltage references for the CLs that take this drop into account. Therefore, from an observation of Eqs (4.1) and (4.2), the following equations, relating the CL voltages to the converter AC voltage and the DC voltage, can be derived for the positive half cycle:

$$v_{upp} = \frac{V_{dc}}{2} - v_c \tag{4.3}$$

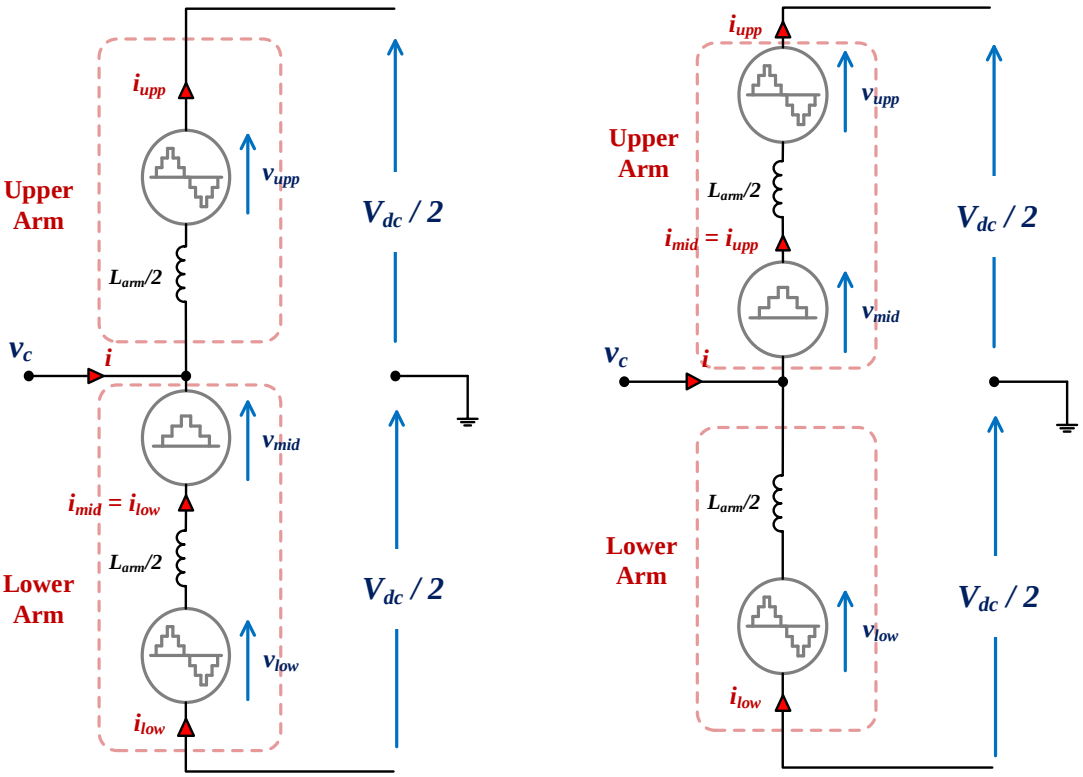


Figure 4.3: Equivalent single phase operation when (a) S_1 is on (b) S_2 is on

$$v_{mid} + v_{low} = v_c + \frac{V_{dc}}{2} \tag{4.4}$$

Similarly, for the case when switch S_2 in Figure (4.1) is turned on, the voltage equations for the positive and negative poles of the DC circuit in Figure (4.3b) can be written as:

$$-v_c + \frac{L_{arm}}{2}\frac{d}{dt}i_{upp} - v_{upp} - v_{mid} + \frac{V_{dc}}{2} = 0 \tag{4.5}$$

$$-v_c - \frac{L_{arm}}{2}\frac{d}{dt}i_{low} + v_{low} - \frac{V_{dc}}{2} = 0 \tag{4.6}$$

Neglecting the voltage drop in the inductors again, the following voltage equations

can be derived for the negative AC half cycle:

$$v_{mid} + v_{upp} = -v_c + \frac{V_{dc}}{2} \tag{4.7}$$

$$v_{low} = \frac{V_{dc}}{2} + v_c \tag{4.8}$$

From Eqs. (4.3), (4.4), (4.7) and (4.8), it can be deduced that for the positive AC half cycle, the voltage waveshaping of the UPP CL is unique whereas the voltage waveshaping of the MID CL and the LOW CL is not unique. Alternatively, in the negative AC half cycle, the LOW CL has a unique voltage waveshape while the MID CL and the UPP CL have non-unique voltage waveshapes. Therefore, due to the existence of non-unique voltage waveshapes in both half-cycles, several voltage waveshaping solutions are possible. In this thesis, the voltage waveshaping is selected to achieve symmetry in the waveforms and to avoid any sharp voltage transitions at the AC zero-crossing. Hence, the following voltage waveshaping of the CLs is selected:

Positive AC half-cycle:

$$v_{upp} = \frac{V_{dc}}{2} - v_c, \quad v_{mid} = v_c, \quad v_{low} = \frac{V_{dc}}{2} \tag{4.9}$$

Negative AC half-cycle:

$$v_{upp} = \frac{V_{dc}}{2}, \quad v_{mid} = -v_c, \quad v_{low} = \frac{V_{dc}}{2} + v_c \tag{4.10}$$

From observation of Figures (4.3a) and (4.3b), the voltages produced at the common terminals of the upper and lower arms can be expressed as:

$$v_{comm}(S_1on) = \frac{1}{2}[(v_{mid} + v_{low}) - v_{upp}] = v_c$$
$$v_{comm}(S_2on) = \frac{1}{2}[v_{low} - (v_{mid} + v_{upp})] = v_c$$

Also, the voltages produced at the differential terminals of the upper and lower arms is the same for both positive and negative half-cycles and can be expressed as:

$$v_{diff} = v_{mid} + v_{low} + v_{upp} = V_{dc}$$

Hence, the proposed voltage waveshaping ensures the ability of the converter phase-leg to produce only AC voltage at the common terminal of the DS configuration and only DC voltage at the differential terminals of the converter phase.

The idealised voltage waveshaping of the CLs is illustrated in Figure (4.4) for the converter operating in over-modulation mode. It needs to be mentioned, however, that the finalised waveshapes for the CL voltages will be slightly different than the ones presented here since additional voltage components will be added to the UPP and LOW CLs to transfer energy between arms, as discussed in the subsequent sections. The following observations can be made about the voltages that need to be synthesized by the CLs:

- **UPP CL:** Inverted half-wave rectification of the converter AC voltage with an offset of $\frac{V_{dc}}{2}$
- **MID CL:** Full-wave rectification of the converter AC output voltage
- **LOW CL:** Inverted half-wave rectification of the converter AC voltage with an offset of $\frac{V_{dc}}{2}$ and shifted by π *rads*

In the rest of this section, the voltages and currents of the converter CLs are mathematically expressed. Figure (4.1) is used as a reference for the converter model and it is assumed that the converter CLs are made up of a large number of cells and produce high-quality waveforms and hence, the switching effects are ignored.

Referring to the three-phase circuit of the SMPC in Figure (4.1), under ideal AC grid conditions, the balanced set of three-phase voltages that the converter needs to

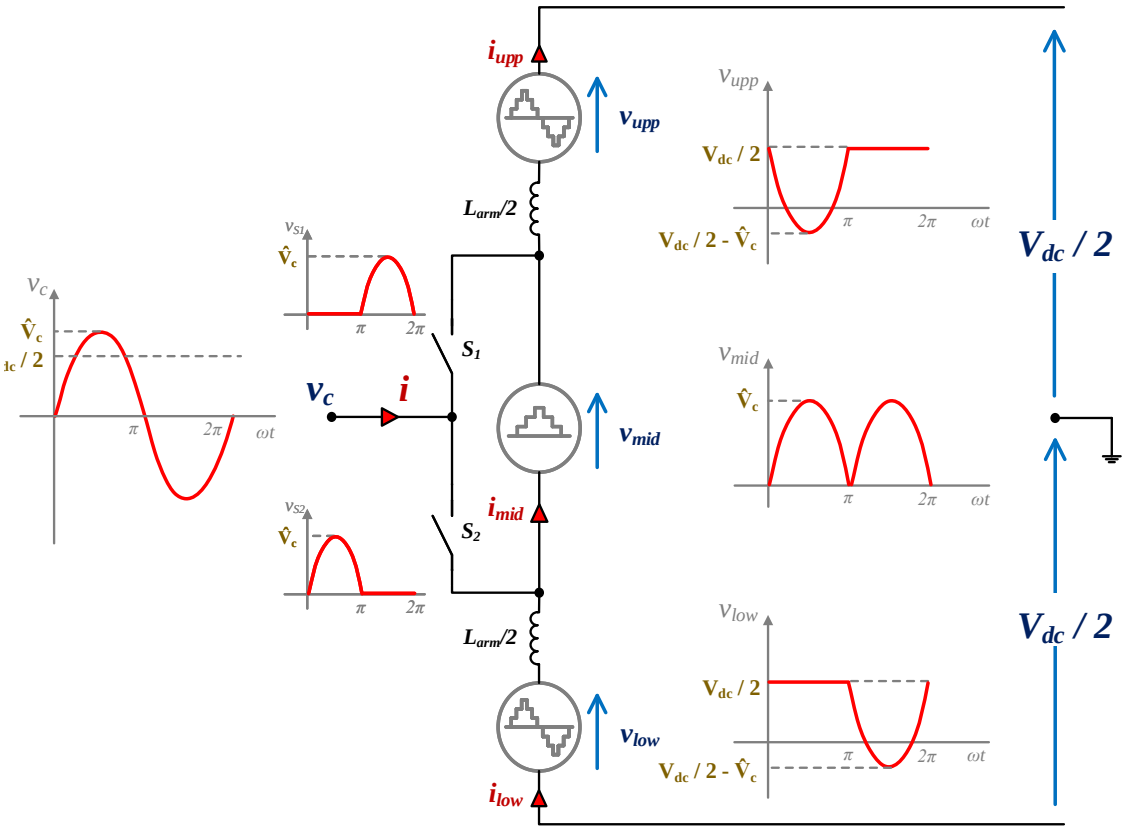


Figure 4.4: Idealized voltage waveshaping of the chainlinks assuming operation in overmodulation mode

generate at its AC output are:

$$\begin{aligned} v_c^a &= r\hat{V}_c \sin(\omega t) \\ v_c^b &= r\hat{V}_c \sin\left(\omega t - \frac{2\pi}{3}\right) \\ v_c^c &= r\hat{V}_c \sin\left(\omega t - \frac{4\pi}{3}\right) \end{aligned} \tag{4.11}$$

where $\hat{V}_c$ is the peak per-phase voltage at the transformer primary (grid-side).

Since the three converter phases in the SMPC are connected in parallel across the DC side and assuming that the phases are balanced and identical, the following analysis is conducted for phase a only.

Using the wave-shaping presented in Eqs (4.9) and (4.10) and the waveforms from

Figure (4.4), the voltages that need to be synthesised by the CLs can be expressed as:

$$v^a_{upp} = \begin{cases} -r\hat{V_c}\sin(\omega t) + \frac{V_{dc}}{2} & 0 < \omega t \leq \pi \\ \frac{V_{dc}}{2} & \pi < \omega t \leq 2\pi \end{cases} \tag{4.12}$$

$$v^a_{mid} = |r\hat{V_c}\sin(\omega t)| \tag{4.13}$$

$$v^a_{low} = \begin{cases} \frac{V_{dc}}{2} & 0 < \omega t \leq \pi \\ r\hat{V_c}\sin(\omega t) + \frac{V_{dc}}{2} & \pi < \omega t \leq 2\pi \end{cases} \tag{4.14}$$

As will be evident in the next section, the derivation of the average powers exchanged with the CLs in steady state will make use of the Fourier series expressions of the CL voltages and currents. Hence, the Fourier series representations of the expressions in Eqs (4.12)-(4.14) are computed and are given as:

$$v^a_{upp} = \frac{V_{dc}}{2} - r\hat{V_c}\left[\frac{1}{\pi} + \frac{1}{2}\sin(\omega t) - \frac{2}{\pi}\sum_{n=2,4,6..}^{\infty}\frac{1}{n^2-1}\cos(n\omega t)\right] \tag{4.15}$$

$$v^a_{mid} = r\hat{V_c}\left[\frac{2}{\pi} - \frac{4}{\pi}\sum_{n=2,4,6..}^{\infty}\frac{1}{n^2-1}\cos(n\omega t)\right] \tag{4.16}$$

$$v^a_{low} = \frac{V_{dc}}{2} - r\hat{V_c}\left[\frac{1}{\pi} - \frac{1}{2}\sin(\omega t) - \frac{2}{\pi}\sum_{n=2,4,6..}^{\infty}\frac{1}{n^2-1}\cos(n\omega t)\right] \tag{4.17}$$

As is expected from a full-wave rectified voltage synthesis by MID CL, Eq (4.16) shows that v^a_{mid} has a DC component and even harmonics of decaying amplitudes. Eqs (4.15) and (4.17) show that the UPP and LOW CLs each synthesise one-half of the converter AC voltage and combinedly block the remaining portion of the DC voltage and cancel out all the even harmonics in the MID CL voltage. Also from Eqs (4.15) - (4.17), the operational flexibility of the converter for a given P-Q range can be appreciated since all three CL voltages are a function of the AC operating point.

Considering ideal AC grid conditions again in Figure (4.1) and an arbitrary phase shift ϕ, the balanced set of three-phase currents at the converter side of the transfomer can be expressed as:

$$\begin{aligned} i_a &= \frac{1}{r}\hat{I}\sin(\omega t - \phi) \\ i_b &= \frac{1}{r}\hat{I}\sin\left(\omega t - \frac{2\pi}{3} - \phi\right) \\ i_c &= \frac{1}{r}\hat{I}\sin\left(\omega t - \frac{4\pi}{3} - \phi\right) \end{aligned} \tag{4.18}$$

Recalling the two-arm operation of each converter phase from Figures (4.3a) and (4.3b), the AC current will split equally between the upper and lower arms. Also, since the converter phases are in parallel across the DC side, one-third of the DC current flows through each converter phase. However, since the placement of the MID CL switches between upper and lower arms in each half-cycle, so does the current in the MID CL. It equates to the LOW CL current in the positive AC half-cycle and is the same as the UPP CL current in the negative AC half-cycle. Therefore, the chainlink currents for phase a can be expressed as:

$$i^a_{upp} = \frac{1}{2r}\hat{I}\sin(\omega t - \phi) + \frac{I_{dc}}{3} \tag{4.19}$$

$$i^a_{mid} = \begin{cases} -\frac{1}{2r}\hat{I}\sin(\omega t - \phi) + \frac{I_{dc}}{3} & 0 < \omega t \leq \pi \\ \frac{1}{2r}\hat{I}\sin(\omega t - \phi) + \frac{I_{dc}}{3} & \pi < \omega t \leq 2\pi \end{cases} \tag{4.20}$$

$$i^a_{low} = -\frac{1}{2r}\hat{I}\sin(\omega t - \phi) + \frac{I_{dc}}{3} \tag{4.21}$$

Computing the Fourier series representation for the expression in Eq. (4.20), i^a_{mid} can be re-expressed as:

$$\begin{aligned} i^a_{mid} = \frac{I_{dc}}{3} - \frac{\hat{I}}{r\pi}\cos\phi + \frac{2\hat{I}}{r\pi}\cos\phi \sum_{n=2,4,6..}^{\infty} \frac{1}{n^2-1}\cos(n\omega t) \\ + \frac{2\hat{I}}{r\pi}\sin\phi \sum_{n=2,4,6..}^{\infty} \frac{n}{n^2-1}\sin(n\omega t) \end{aligned} \tag{4.22}$$

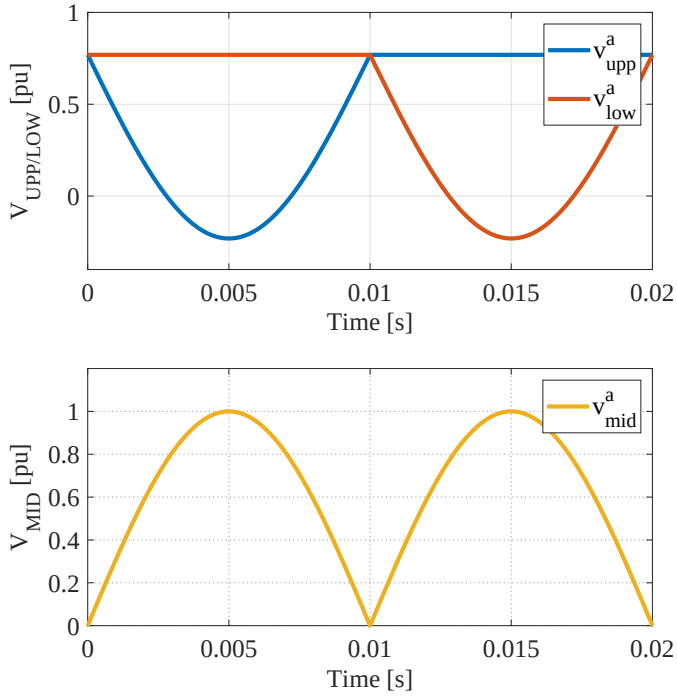


Figure 4.5: Idealised per-unit UPP/LOW CL voltages (top) and MID CL voltage (bottom)

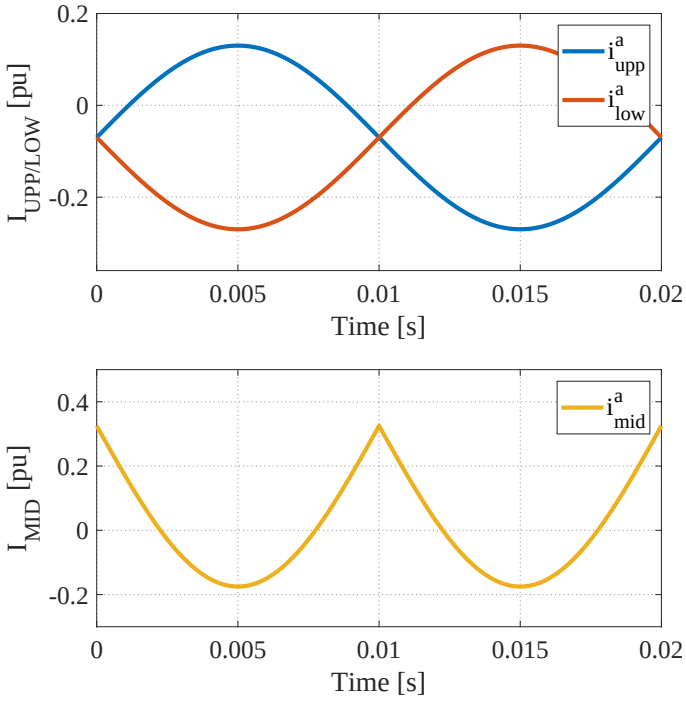


Figure 4.6: Idealised per-unit UPP/LOW CL currents (top) and MID CL current (bottom)

Figures (4.5) and (4.6) show idealised per-unit CL voltage and CL current waveforms at unity power factor. The waveforms implement the expressions in (4.12) - (4.14) and (4.19) - (4.21) in a MATLAB script.

4.4 Energy management

The key to multilevel operation and generation of waveforms that closely approximate the sinusoidal AC is the ability of multilevel converters to switch in and out cells containing charged capacitors at different instants over a period. To operate a multilevel converter successfully, the cell capacitor voltages should be stable within a pre-defined ripple margin around the nominal value. This is achieved by: (a) employing rotation mechanisms that sort the virtual positions of the cells based on whether their voltages are above or below the nominal value and the current direction and (b) ensuring that zero net energy is exchanged with the converter CLs over a period in steady-state [55].

In this thesis, the global power balance between the AC and DC side for the SMPC is maintained separately in each phase by per-phase global controllers. The global controllers control the overall stored energy in each phase-leg by regulating the difference between the per-phase AC and DC side powers. In addition, there are two local energy controllers that transfer energy between the CLs in a phase to ensure that zero average power is exchanged with all the CLs in steady-state. The two local energy controllers are:

- *Inter-arm energy controllers*, that transfer energy between the MID CLs and the UPP/LOW CLs to control their energy difference to a reference value.
- *Inter-CL energy controllers*, that transfer energy between the UPP CLs and the LOW CLs to maintain their energy difference to zero.

The analysis presented in this section relates to the Inter-arm energy controllers, establishing a mathematical basis for the need of transferring energy between the MID CL and the UPP/LOW CLs. The analysis can also be extended to the study and design of the Inter-CL energy controllers which is discussed in Chapter 5 where the control scheme designed for a particular application is presented.

The assumption made for the analysis is that the global power balance exists in each phase which means that in practice, the global controllers will be designed to act more quickly than the local controllers. Using this assumption, an expression for I_{dc} can be computed as:

$$\begin{aligned} P_{dc} &= \bar{P}_c \\ V_{dc} I_{dc} &= \frac{3}{2} r \hat{V}_c \frac{\hat{I}}{r} \cos\phi \\ I_{dc} &= \frac{3\hat{V}_c}{2V_{dc}} \hat{I} \cos\phi \end{aligned} \tag{4.23}$$

In order to define the CL average powers in terms of the operating point, instantaneous powers of UPP, MID and LOW CLs are first computed as given below. Note that in the CL current expressions of Eqs. (4.19) - (4.22), I_{dc} is defined as in Eq. (4.23).

$$p^a_{upp} = v^a_{upp} \times i^a_{upp}$$

$$\begin{aligned} p^a_{upp} = \overbrace{\frac{\hat{V}_c \hat{I}}{4}\cos\phi - \frac{r\hat{V}_c^{\,2}\hat{I}}{2\pi V_{dc}}\cos\phi}^{\text{DC terms}} - \frac{r\hat{V}_c^{\,2}\hat{I}}{4V_{dc}}\cos\phi\sin(\omega t) + \frac{r\hat{V}_c^{\,2}\hat{I}}{\pi V_{dc}}\cos\phi \sum_{n=2,4,6..}^{\infty} \frac{1}{n^2-1}\cos(n\omega t) \\ \underbrace{-\frac{\hat{V}_c\hat{I}}{4}\sin(\omega t)\sin(\omega t - \phi)}_{\substack{\text{contains an implicit DC term} \\ \text{(product of sines)}}} + \left(\frac{V_{dc}\hat{I}}{4r} - \frac{\hat{V}_c\hat{I}}{2\pi} + \frac{\hat{V}_c\hat{I}}{\pi}\sum_{n=2,4,6..}^{\infty}\frac{1}{n^2-1}\cos(n\omega t)\right)\sin(\omega t - \phi) \end{aligned} \tag{4.24}$$

$$p^a_{mid} = v^a_{mid} \times i^a_{mid}$$

$$p^a_{mid} = \overbrace{\frac{r\hat{V_c}^2\hat{I}}{\pi V_{dc}}\cos\phi - \frac{2\hat{V_c}\hat{I}}{\pi^2}\cos\phi}^{\text{DC terms}} + \left(\frac{8\hat{V_c}\hat{I}}{\pi^2} - \frac{2r\hat{V_c}^2\hat{I}}{\pi V_{dc}}\right)\cos\phi \sum_{n=2,4,6..}^{\infty}\frac{1}{n^2-1}\cos(n\omega t) + \frac{4\hat{V_c}\hat{I}}{\pi^2}\sin\phi \sum_{n=2,4,6..}^{\infty}\frac{n}{n^2-1}\sin(n\omega t) - \underbrace{\frac{8\hat{V_c}\hat{I}}{\pi^2}\cos\phi\left(\sum_{n=2,4,6..}^{\infty}\frac{1}{n^2-1}\cos(n\omega t)\right)^2}_{\text{contains an implicit DC term (product of cosines)}} - \frac{8\hat{V_c}\hat{I}}{\pi^2}\cos\phi\left(\sum_{n=2,4,6..}^{\infty}\frac{1}{n^2-1}\cos(n\omega t)\sum_{n=2,4,6..}^{\infty}\frac{n}{n^2-1}\sin(n\omega t)\right) \tag{4.25}$$

$$p^a_{low} = v^a_{low} \times i^a_{low}$$

$$p^a_{low} = \overbrace{\frac{\hat{V_c}\hat{I}}{4}\cos\phi - \frac{r\hat{V_c}^2\hat{I}}{2\pi V_{dc}}\cos\phi}^{\text{DC terms}} + \frac{r\hat{V_c}^2\hat{I}}{4V_{dc}}\cos\phi\sin(\omega t) + \frac{r\hat{V_c}^2\hat{I}}{\pi V_{dc}}\cos\phi\sum_{n=2,4,6..}^{\infty}\frac{1}{n^2-1}\cos(n\omega t) - \underbrace{\frac{\hat{V_c}\hat{I}}{4}\sin(\omega t)\sin(\omega t-\phi)}_{\substack{\text{contains an implicit DC term}\\ \text{(product of sines)}}} - \left(\frac{V_{dc}\hat{I}}{4r} - \frac{\hat{V_c}\hat{I}}{2\pi} + \frac{\hat{V_c}\hat{I}}{\pi}\sum_{n=2,4,6..}^{\infty}\frac{1}{n^2-1}\cos(n\omega t)\right)\sin(\omega t-\phi) \tag{4.26}$$

In Eqs. (4.24) - (4.26), ignoring the terms that are purely AC and collecting the obvious DC terms plus the terms containing implicit DC terms, the following can be written:

$$p^{a^{DCterms}}_{upp/low} = \frac{\hat{V_c}\hat{I}}{4}\cos\phi - \frac{r\hat{V_c}^2\hat{I}}{2\pi V_{dc}}\cos\phi - \frac{\hat{V_c}\hat{I}}{4}\sin(\omega t)\sin(\omega t-\phi)$$

$$p^{a^{DCterms}}_{upp/low} = \frac{\hat{V_c}\hat{I}}{4}\cos\phi - \frac{r\hat{V_c}^2\hat{I}}{2\pi V_{dc}}\cos\phi - \frac{\hat{V_c}\hat{I}}{8}\cos\phi + \underbrace{\frac{\hat{V_c}\hat{I}}{8}\sin(2\omega t) + \frac{\hat{V_c}\hat{I}}{4}\sin\phi\cos(\omega t)\sin(\omega t)}_{\text{AC terms ignored}} \tag{4.27}$$

$$p^{a^{DCterms}}_{mid} = \frac{r\hat{V_c}^2\hat{I}}{\pi V_{dc}}\cos\phi - \frac{2\hat{V_c}\hat{I}}{\pi^2}\cos\phi - \frac{8\hat{V_c}\hat{I}}{\pi^2}\cos\phi\left(\sum_{n=2,4,6..}^{\infty}\frac{1}{n^2-1}\cos(n\omega t)\right)^2 \tag{4.28}$$

The final term in Eq. (4.28) contains square of a cosine series. When it is expanded, a cosine-squared series will result in only DC terms and the remaining terms will be

purely AC. Extracting only the DC terms out of the cosine-squared series, Eq. (4.28) can be rewritten as:

$$p_{mid}^{a^{DCterms}} = \frac{r\hat{V_c}^2\hat{I}}{\pi V_{dc}}\cos\phi - \frac{2\hat{V_c}\hat{I}}{\pi^2}\cos\phi - \frac{8\hat{V_c}\hat{I}}{\pi^2}\cos\phi \sum_{n=2,4,6..}^{\infty} \frac{1}{2\left(n^2-1\right)^2} \tag{4.29}$$

In the last term in Eq. (4.29), $\sum_{n=2,4,6..}^{\infty} \frac{1}{2(n^2-1)^2} = 0.05845$. Finally, after some manipulation, the average powers in the CLs are given as:

$$\bar{P}_{upp}^{a} = -\frac{1}{2}\hat{V_c}\hat{I}\cos\phi\left(\frac{r\hat{V_c}}{\pi V_{dc}} - \frac{1}{4}\right) \tag{4.30}$$

$$\bar{P}_{mid}^{a} = \hat{V_c}\hat{I}\cos\phi\left(\frac{r\hat{V_c}}{\pi V_{dc}} - \frac{1}{4}\right) \tag{4.31}$$

$$\bar{P}_{low}^{a} = -\frac{1}{2}\hat{V_c}\hat{I}\cos\phi\left(\frac{r\hat{V_c}}{\pi V_{dc}} - \frac{1}{4}\right) \tag{4.32}$$

It can be observed from Eqs. (4.30) - (4.32) that in order for the mean powers exchanged with the CLs in steady-state to be zero, the following should be true:

$$\frac{r\hat{V_c}}{\pi V_{dc}} - \frac{1}{4} = 0 \tag{4.33}$$

The modulation index M of the converter is defined as the ratio of the peak converter AC output voltage to half of the DC voltage:

$$M = \frac{2r\hat{V_c}}{V_{dc}} \tag{4.34}$$

Substituting Eq. (4.34) into Eq. (4.33), the following is derived:

$$M_{ss} = \frac{\pi}{2} \tag{4.35}$$

This suggests that a 'sweet-spot' exists for the converter at the specific modulation index value of $\frac{\pi}{2} \approx 1.57$ where the steady-state average power exchanged with each CL is naturally zero without further control. Theoretically, this modulation index

can be set by choosing the transformer turns-ratio according to Eq. (4.34) for any set of AC and DC voltage levels.

Despite the existence of a 'sweet-spot', an active energy management controller is needed because the discrepancies between the theoretical model and the practical converter and asymmetries between converter arms will lead to a small average power exchange with the CLs in steady state. In addition, the active energy management controller will enable the converter to operate away from the 'sweet-spot' and free the aforementioned constraint on the modulation index, that can be optimised to provide other benefits such as reduced energy storage requirements (shown later in Section (4.5.4)).

It can be observed from Eqs. (4.30) - (4.32) that the following holds true:

$$\bar{P}^a_{mid} = -(\bar{P}^a_{upp} + \bar{P}^a_{low}) \tag{4.36}$$

Eq. (4.36) shows that the average powers of UPP and LOW CLs combined are equal and opposite to the average power in the MID CL. This means that when moving away from the 'sweet-spot', according to Eqs. (4.30) - (4.32), there will be a surplus of average power in the MID CL and an equal deficit in the UPP/LOW CLs combined, or vice-versa. To restore the equilibrium position of zero average power in all CLs, it is necessary to implement a mechanism for continually transferring energy between the MID CL and the UPP/LOW CLs in either direction as needed.

The task of continually transferring energy between the UPP/LOW CLs and the MID CL in the SMPC is slightly challenging because of the following two limitations:

- Observing the CL current expressions in Eqs. (4.19) - (4.22), it can be noticed that i^a_{upp}/i^a_{low} only have DC and fundamental frequency components whereas i^a_{mid} has DC and even harmonic components. This means that there exist no common frequency components in i^a_{upp}/i^a_{low} and i^a_{mid} and hence, energy cannot

be continually transferred between the CLs just by adding voltage correction terms to the CL voltages.

- The MID CL switches between the upper and lower arms each half cycle, and hence any balancing voltage components added in v^a_{mid} will not cancel on the AC side. That leaves only v^a_{low}/v^a_{upp} as possible degrees of freedom to transfer energy between the CLs.

In light of these limitations, the method proposed to tackle the problem of energy management is to add a control variable that is common to all the CLs in a phase-leg and can be injected just by acting on the UPP/LOW CL voltages.

From Eqs. (4.15) - (4.17), it can be observed that the second harmonic components in the CL voltage expressions are:

$$v^a_{upp_{2\omega}} = \frac{2r\hat{V}_c}{3\pi}\cos(2\omega t) \tag{4.37}$$

$$v^a_{mid2\omega} = -\frac{4r\hat{V}_c}{3\pi}\cos(2\omega t) \tag{4.38}$$

$$v^a_{low2\omega} = \frac{2r\hat{V}_c}{3\pi}\cos(2\omega t) \tag{4.39}$$

And the following relationship holds:

$$v^a_{mid2\omega} = -(v^a_{upp_{2\omega}} + v^a_{low2\omega}) \tag{4.40}$$

From Eq. (4.40), it can be deduced that a common second harmonic (2ω) current through all the CLs in a phase-leg would successfully achieve the desired effect of transferring energy between UPP/LOW and MID CLs. This 2ω current will be a circulating current on the DC side and can be driven by adding 2ω components with the same polarity in UPP and LOW CL voltages only. Hence, by accurately choosing the amount of 2ω current injection, the average powers of the CLs can be driven to zero in steady-state. Since the added 2ω current components will form a balanced 3-phase set, they will cancel at the DC side.

The 2ω current that needs to be injected has to be in phase with the 2ω components in the CL voltages shown in Eqs. (4.37) - (4.39). It is defined as:

$$i^a_{2\omega} = k_{2\omega 0}\cos(2\omega t) \tag{4.41}$$

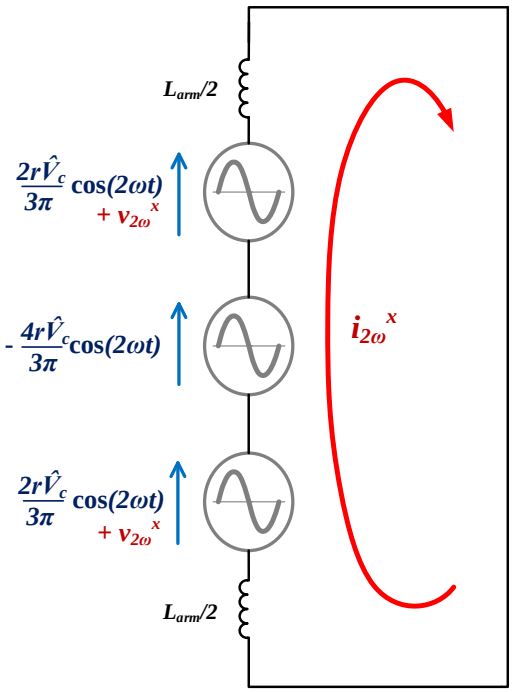


Figure 4.7: Equivalent 2nd harmonic circuit on the DC side

The equivalent second harmonic circuit on the DC side is presented in Figure (4.7). As mentioned above, v^a_{mid} is not available for any addition of balancing voltage components, and $i^a_{2\omega}$ is driven by adding 2ω voltage components ($v^a_{2\omega}$) only in v^a_{upp} and v^a_{low}. Hence, the 2ω voltage equation on the converter DC side can be expressed as:

$$v^a_{upp_{2\omega}} + v^a_{mid2\omega} + v^a_{low2\omega} = L_{arm}\frac{d}{dt}i^a_{2\omega}$$

$$\left(\frac{2r\hat{V}_c}{3\pi}\cos(2\omega t) + v^a_{2\omega}\right) - \frac{4r\hat{V}_c}{3\pi}\cos(2\omega t) + \left(\frac{2r\hat{V}_c}{3\pi}\cos(2\omega t) + v^a_{2\omega}\right) = L_{arm}\frac{d}{dt}(k_{2\omega 0}cos(2\omega t))$$

$v^a_{2\omega}$ is hence given as:

$$v^a_{2\omega} = -\frac{k_{2\omega}}{2}\sin(2\omega t) \tag{4.42}$$

where $k_{2\omega} = 2\omega L_{arm} k_{2\omega 0}$.

The 2ω average powers resulting from the interaction of the original 2ω voltage components in the CLs and $i^a_{2\omega}$ are determined as:

$$\begin{aligned} \bar{P}^a_{upp_{2\omega}} &= \frac{r k_{2\omega} \hat{V}_c}{6\pi\omega L_{arm}} \\ \bar{P}^a_{mid_{2\omega}} &= -\frac{r k_{2\omega} \hat{V}_c}{3\pi\omega L_{arm}} \\ \bar{P}^a_{low_{2\omega}} &= \frac{r k_{2\omega} \hat{V}_c}{6\pi\omega L_{arm}} \end{aligned} \tag{4.43}$$

Average power expressions of the CLs expressed earlier in Eqs. (4.30) - (4.32) can be re-written to include the effect of the energy management action as:

$$\bar{P}^a_{upp} = -\frac{1}{2}\hat{V}_c \hat{I} \cos\phi \left(\frac{r\hat{V}_c}{\pi V_{dc}} - \frac{1}{4} \right) + \frac{r k_{2\omega} \hat{V}_c}{6\pi\omega L_{arm}} \tag{4.44}$$

$$\bar{P}^a_{mid} = \hat{V}_c \hat{I} \cos\phi \left(\frac{r\hat{V}_c}{\pi V_{dc}} - \frac{1}{4} \right) - \frac{r k_{2\omega} \hat{V}_c}{3\pi\omega L_{arm}} \tag{4.45}$$

$$\bar{P}^a_{low} = -\frac{1}{2}\hat{V}_c \hat{I} \cos\phi \left(\frac{r\hat{V}_c}{\pi V_{dc}} - \frac{1}{4} \right) + \frac{r k_{2\omega} \hat{V}_c}{6\pi\omega L_{arm}} \tag{4.46}$$

Eqs. (4.44) - (4.46) can be equated to zero to develop an expression for $k_{2\omega}$, which is the 2ω balancing voltage amplitude:

$$k_{2\omega} = 3\omega L_{arm} \hat{I} \cos\phi \left(\frac{\hat{V}_c}{V_{dc}} - \frac{\pi}{4r} \right) \tag{4.47}$$

Expressing the turns-ratio r in terms of the modulation index M using Eq. (4.34), Eq. (4.47) can be re-written as:

$$k_{2\omega} = 3\omega L_{arm} \hat{I} \cos\phi \left(\frac{\hat{V}_c}{V_{dc}} - \frac{\pi\hat{V}_c}{2MV_{dc}} \right) \tag{4.48}$$

It is obvious from Eq. (4.48) that if $M = M_{ss} = \frac{\pi}{2}$, then $k_{2\omega} = 0$, verifying that no balancing second harmonic is required at the 'sweet-spot'. Also, the amount of

balancing second harmonic required depends on how far away M is from M_{ss} and the P-Q operating point of the converter (assuming a fixed L_{arm}). The variation of $k_{2\omega}$ for an arbitrary $M = 0.83M_{ss}$ with changing P-Q operating points is depicted in Figure (4.8) where a 20 kV DC - 11 kV AC system is considered with an active power capability of ± 20 MW and a reactive power capability of ± 8 MVAr. In this figure, absolute values of $k_{2\omega}$ normalised to $\frac{V_{dc}}{2}$ are plotted over the complete P-Q operating region. It can be noticed that the largest balancing second harmonic required is at the extreme points of the P-Q operating region.

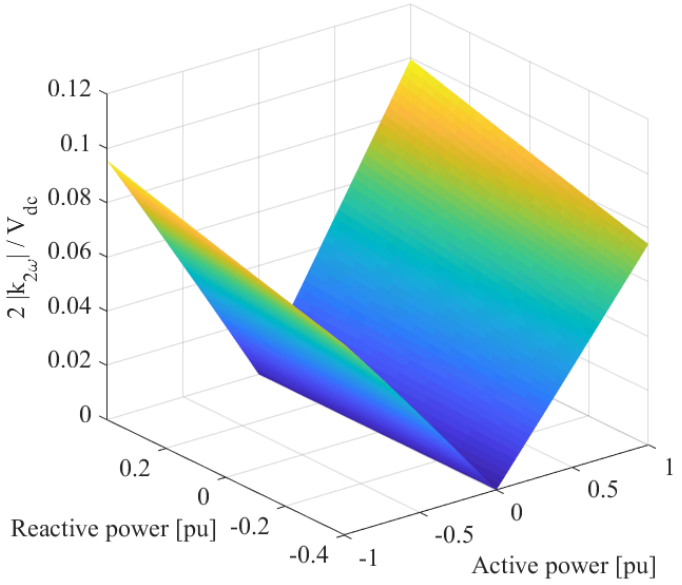


Figure 4.8: Absolute values of $k_{2\omega}$ normalised to $\frac{V_{dc}}{2}$ plotted over the P-Q operating region

To demonstrate the effect of changing M on $k_{2\omega}$, a polar plot is presented in Figure (4.9) assuming a fixed apparent power of 21.56 MVAr. The angle values are a sweep of the power factor angle from 0 to 2π and the radius of the plot is $\frac{2|k_{2\omega}|}{V_{dc}}$ that is plotted for different M values on either side of the 'sweet-spot'. The plot illustrates that the farther M is from M_{ss}, the higher is the required balancing second harmonic.

The expressions for UPP and LOW CL voltages after the addition of the balancing second harmonic are given in (4.49) and (4.50). The expression for MID CL voltage

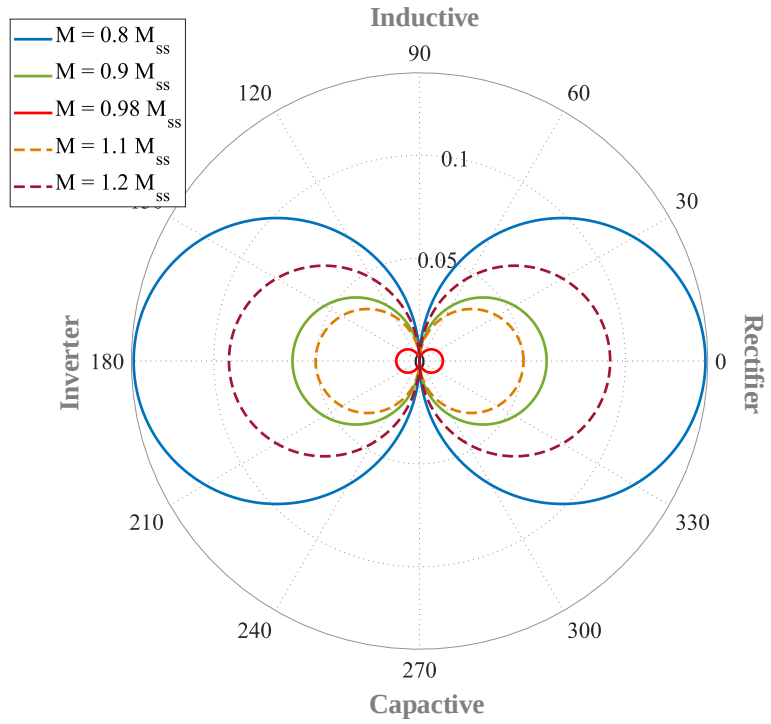


Figure 4.9: $\frac{2|k_{2\omega}|}{V_{dc}}$ plotted for different M values relative to M_{ss}

stays unchanged.

$$v^a_{upp} = \frac{V_{dc}}{2} - r\hat{V}_c\left[\frac{1}{\pi} + \frac{1}{2}\sin(\omega t) - \frac{2}{\pi}\sum_{n=2,4,6..}^{\infty}\frac{1}{n^2-1}\cos(n\omega t)\right] - \frac{k_{2\omega}}{2}\sin(2\omega t) \tag{4.49}$$

$$v^a_{low} = \frac{V_{dc}}{2} - r\hat{V}_c\left[\frac{1}{\pi} - \frac{1}{2}\sin(\omega t) - \frac{2}{\pi}\sum_{n=2,4,6..}^{\infty}\frac{1}{n^2-1}\cos(n\omega t)\right] - \frac{k_{2\omega}}{2}\sin(2\omega t) \tag{4.50}$$

The expressions for CL currents after the addition of balancing second harmonic are presented in (4.51) - (4.53).

$$i^a_{upp} = \frac{1}{2r}\hat{I}\sin(\omega t - \phi) + \frac{I_{dc}}{3} + \frac{k_{2\omega}}{2\omega L_{arm}}\cos(2\omega t) \tag{4.51}$$

$$i^a_{mid} = \frac{I_{dc}}{3} - \frac{I}{r\pi}\cos\phi + \frac{2I}{r\pi}\cos\phi \sum_{n=2,4,6..}^{\infty} \frac{1}{n^2-1}\cos(n\omega t) + \frac{2I}{r\pi}\sin\phi \sum_{n=2,4,6..}^{\infty} \frac{n}{n^2-1}\sin(n\omega t) + \frac{k_{2\omega}}{2\omega L_{arm}}\cos(2\omega t) \tag{4.52}$$

$$i^a_{low} = -\frac{1}{2r}\hat{I}\sin(\omega t - \phi) + \frac{I_{dc}}{3} + \frac{k_{2\omega}}{2\omega L_{arm}}\cos(2\omega t) \tag{4.53}$$

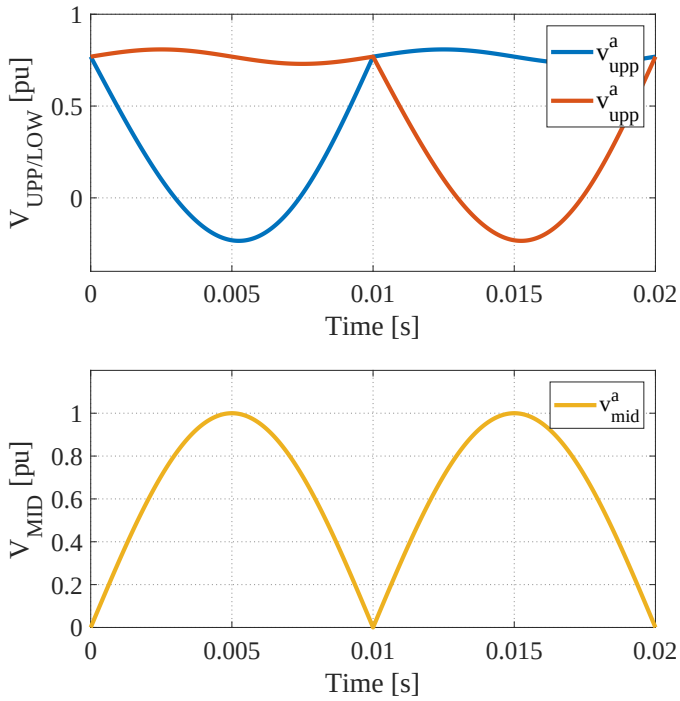


Figure 4.10: Idealised per-unit UPP/LOW CL voltages (top) and MID CL voltage (bottom) after energy management action

Figures (4.10) and (4.11) show idealised per-unit CL voltage and CL current waveforms after energy management for an arbitrary $M = 0.83M_{ss}$ at unity power factor. The effect of the balancing second harmonic on the voltage and current waveshapes can be observed.

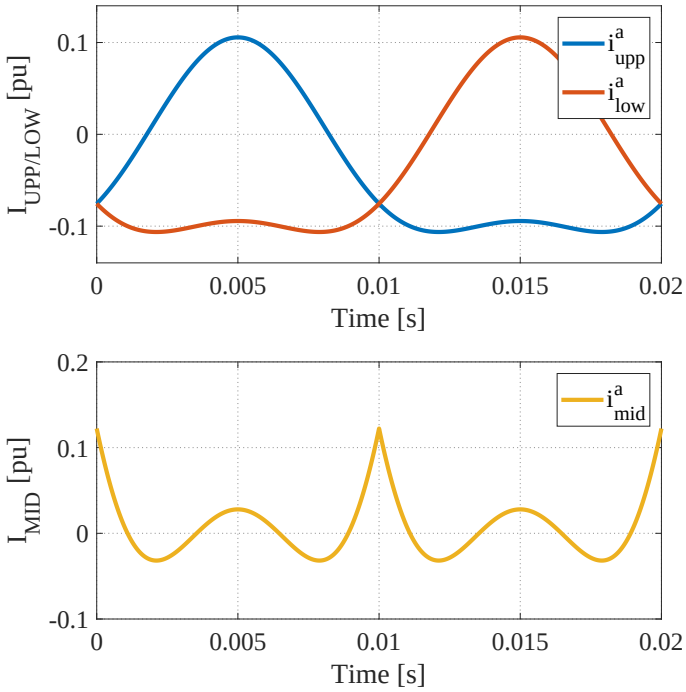


Figure 4.11: Idealised per-unit UPP/LOW CL currents (top) and MID CL current (bottom) after energy management action

4.5 Converter sizing and optimisation

Due to the differences in waveshaping and internal energy distribution in the CLs/arms of various multilevel VSC converters, the method of sizing the converter parameters for any given system ratings may vary considerably. Sizing of the converter generally involves the determination of the number of cells (referred to as 'Sub-Modules' (SMs) from here onwards) in the CLs/arms, dimensioning of the SM capacitors and the arm reactors and the selection of the nominal voltage to be maintained on the capacitors.

Multilevel converters generate an AC current that is very close to a sine wave and hence, AC filters are not needed. However, an absence of AC filters means that the SMs in a multilevel converter are one of the bulkiest components of the converter station [55]. Inside an SM, the capacitor size may take over 50% of the total size and 80% of the weight of the SM [70]. Recent efforts in proposing novel multilevel

HVDC topologies that are more compact than the MMC have focused on reducing the size of the capacitor and/or the overall number of SMs for any specified system rating.

For the sizing analysis of the SMPC, general expressions for CL ratings and for the calculation of the number of SMs are presented. For the SM capacitor sizing, numerical solutions are computed instead of finding symbolic solutions. This is because the energy functions derived from the integration of the CL power expressions would be too complicated to attain tractable results. Also, the modulation index of the converter is optimised, establishing a general solution for a given reactive power to active power ratio.

4.5.1 Voltage ratings of the CLs and the DS configuration

To evaluate the general voltage ratings of the CLs and the DS configuration, the maximum voltages produced by the CLs are first determined. It is assumed that the peak converter AC output voltage, $\hat{V}_c$ is fixed for any fixed M. Also, it needs to be declared that $\hat{V}_c$ is at the converter side of the AC transformer and hence, already incorporates the turns-ratio multiplication factor. Moreover, the expressions presented only provide the minimal requirement under normal operation and extra margins may need to be added under different operating conditions e.g. faults.

In Figure (4.12), the idealised voltage wave-shaping of the converter taking into account the modifications resulting from the energy management action has been shown. As can be seen from the figure, the MID CLs need to be rated for $\hat{V}_c$ and the UPP/LOW CLs need to be rated for $\frac{1}{2}(V_{dc} + |k_{2\omega}^{wc}|)$.

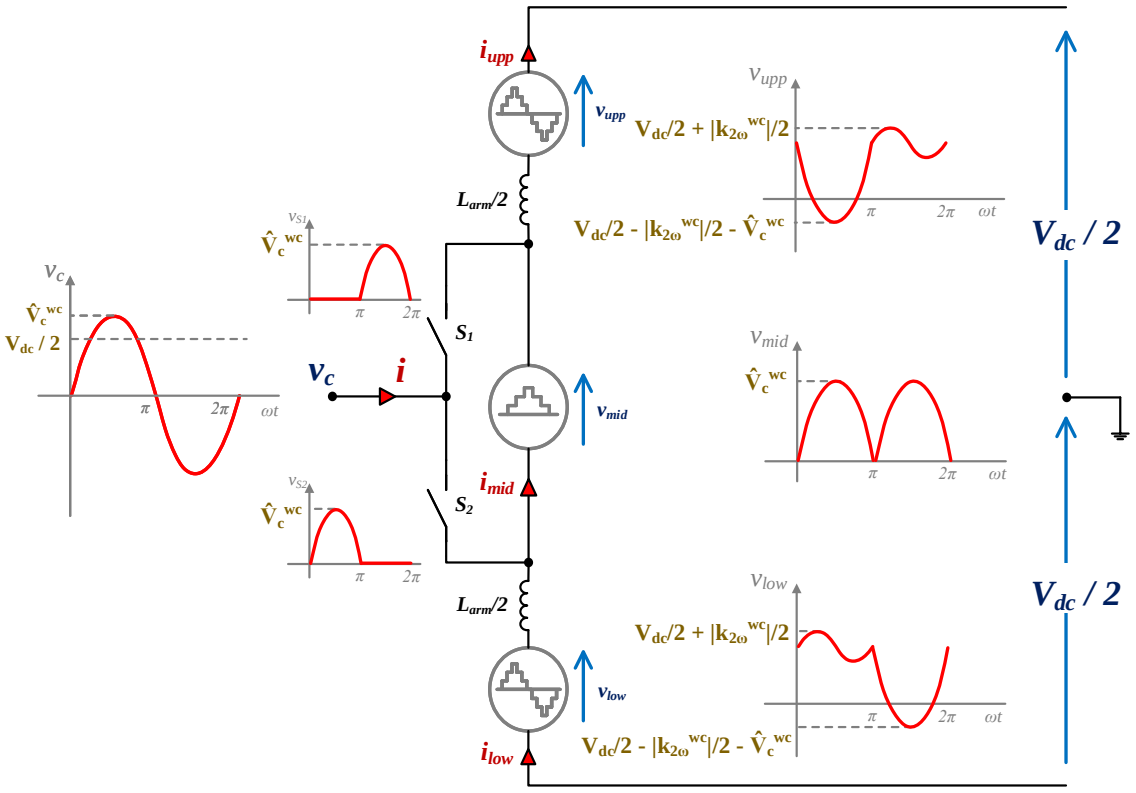


Figure 4.12: Idealised voltage waveshaping of the CLs after energy management assuming operation in over-modulation mode

Thus, the number of SMs required in the CLs can generically be expressed as:

$$\begin{aligned} N_{SM}^{upp} &= \frac{\frac{1}{2}(V_{dc} + |k_{2\omega}^{wc}|)}{V_{nom}} \\ N_{SM}^{mid} &= \frac{\hat{V}_c}{V_{nom}} \\ N_{SM}^{low} &= \frac{\frac{1}{2}(V_{dc} + |k_{2\omega}^{wc}|)}{V_{nom}} \end{aligned} \tag{4.54}$$

where V_{nom} is the nominal voltage maintained on the SM capacitors.

Both the switches in the DS configuration conduct alternately over a fundamental cycle and hence, should be rated to block the maximum voltage applied across them i.e. $\hat{V}_c$. Assuming that the maximum voltage applied to a single IGBT in a DS is the same as V_{nom}, the required number of IGBTs in each switch position of the DS

configuration can be obtained by:

$$N_{IGBT}^{DS} = \frac{\hat{V}_c}{V_{nom}} \tag{4.55}$$

For the case that 'hybrid chainlinks' are employed in UPP/LOW CLs, the number of SMs there can be expressed as:

$$N_{SM}^{upp/low} = N_{SM_{HB}}^{upp/low} + N_{SM_{FB}}^{upp/low}$$

where $N_{SM_{HB}}^{upp/low}$ and $N_{SM_{FB}}^{upp/low}$ are the number of half-bridge and full-bridge SMs respectively in UPP/LOW CLs.

To determine the minimum $N_{SM_{FB}}^{upp/low}$, the worst-case lowest voltage produced by the UPP/LOW CLs in the negative voltage region is used. Without the energy management action, it can be expressed as $\left(\frac{V_{dc}}{2} - \hat{V}_c\right)$ and the effect of $k_{2\omega}^{wc}$ on the voltage shape in the positive half-cycle in UPP CL and in the negative half-cycle in LOW CL is such that the lowest voltages of the CLs will not be lower than the value of $\left(\frac{V_{dc}}{2} - \hat{V}_c - \frac{|k_{2\omega}^{wc}|}{2}\right)$. Hence, it is safe to rate the minimum $N_{SM_{FB}}^{upp/low}$ as:

$$N_{SM_{FB}}^{upp/low} = \frac{\left|\frac{1}{2}(V_{dc} - |k_{2\omega}^{wc}|) - \hat{V}_c\right|}{V_{nom}} \tag{4.56}$$

The number of half-bridge SMs in UPP/LOW CLs can then be calculated as:

$$N_{SM_{HB}}^{upp/low} = N_{SM}^{upp/low} - N_{SM_{FB}}^{upp/low} \tag{4.57}$$

It is important here to mention that $N_{SM_{FB}}^{upp/low}$ is the minimum number of FB SMs required in UPP/LOW CLs to be able to produce the negative voltage of the CLs for a known modulation index (over-modulation considered). However, as presented later in Section (4.6), the actual $N_{SM_{FB}}^{upp/low}$ may be different than the one calculated in Eq. (4.56) to prevent their voltages to deviate away from the nominal voltage value.

4.5.2 System ratings for analysis

The sizing and optimisation analysis of the SMPC presented in the subsequent sections is based on the voltage and power ratings of a scaled-down industrial HVDC demonstrator [71] presented in Table (4.1). The SM nominal voltage has been fixed at 1500 V and the maximum allowed peak-to-peak voltage ripple in the SM capacitors is set to 20% of the nominal SM voltage. Using these fixed parameters, the capacitor size, number of SMs and the energy storage requirement are all solved for the specified system ratings.

System ratings	
Active power (P_{rated})	20 MW
Reactive power (Q_{rated})	± 8 MVAr
Line-to-line AC rms voltage (V_{AC})	11 kV
DC voltage (V_{dc})	20 kV
SM nominal votlage (V_{nom})	1500 V
SM capacitor voltage ripple (ρ_{pk-pk})	20% pk-to-pk

Table 4.1: System ratings for SMPC analysis

The P-Q envelope based on the above ratings is shown in Figure (4.13). The converter parameters should be sized for the worst-case operating conditions which occur at the extreme points of the operating region. Hence, only the points that exist on the outer boundaries of the P-Q envelope are of interest. For the sake of clarity, it should be noted that although the rated apparent power (S_{rated}) is 21.54 MVA, the maximum reactive power capability limit of ± 8 MVAr is respected in cases where there is no active power transfer. Hence, $|S|$ is not fixed on the boundaries of the P-Q envelope giving it a rectangular shape, rather than a circular one.

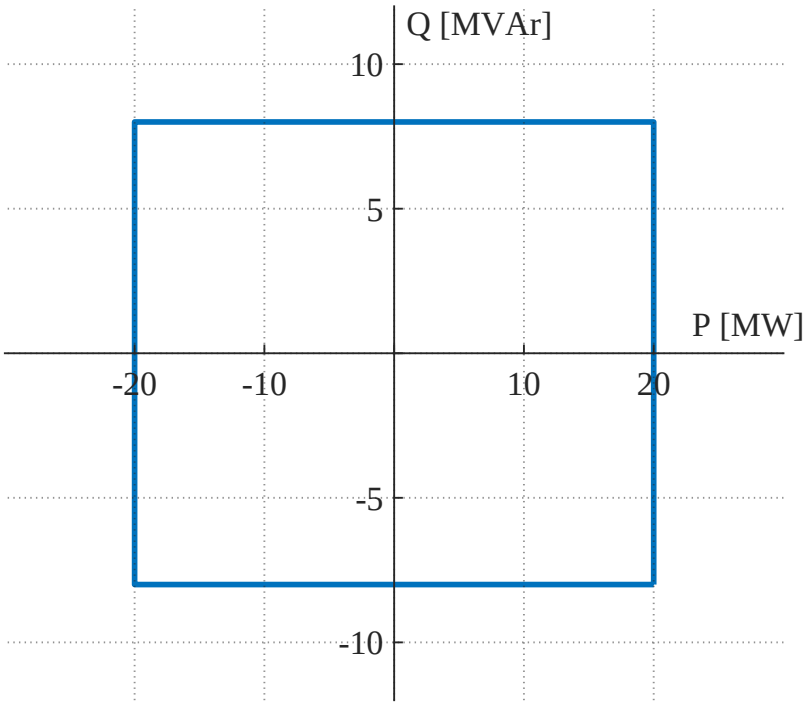


Figure 4.13: P-Q envelope considered for SMPC analysis

4.5.3 SM capacitor sizing

The principle of SM capacitor sizing in modular multilevel converters is to evaluate the minimum size for which the worst-case voltage ripple on the capacitors is within a pre-defined range of the SM nominal voltage. In this thesis, a well-established method, also discussed in [55],[72],[73],[74],[75] for other multilevel converters, is used. In this method, the energy pulsations of the CLs/arms are used to determine the SM capacitor sizes. It is implicitly assumed that the energy pulsations in each CL are equally distributed amongst the SM capacitors by the cell rotation mechanism.

The maximum and minimum energy in an SM capacitor can be expressed as:

$$E_{cap}^{max} = \frac{1}{2} C_{SM} \left(V_{nom} + \rho_{peak} V_{nom}\right)^2$$
$$E_{cap}^{min} = \frac{1}{2} C_{SM} \left(V_{nom} - \rho_{peak} V_{nom}\right)^2$$

where C_{SM} is the SM capacitance, ρ_{peak} is the peak ripple factor and V_{nom} is the

nominal SM voltage.

The peak-to-peak energy deviation in an SM capacitor can then be computed as:

$$\Delta E_{cap} = E_{cap}^{max} - E_{cap}^{min}$$

$$\Delta E_{cap} = 2C_{SM}\rho_{peak}V_{nom}^2 \tag{4.58}$$

Assuming that the insertion indices of the SMs are perfectly distributed between them and that all the SM capacitors in a CL equally share the CL voltage, the expression in Eq. (4.58) can be extended to develop the peak-to-peak energy deviation equation of a CL with N_{SM} SMs as follows:

$$\Delta E_{CL} = 2N_{SM}C_{SM}\rho_{peak}V_{nom}^2 \tag{4.59}$$

Expressing the peak-to-peak ripple factor, $\rho_{pk-pk} = 2\rho_{peak}$ and re-arranging Eq. (4.59), a generic expression for the minimum required SM capacitor size is presented as:

$$C_{SM} \geq \frac{\Delta E_{CL}}{\rho_{pk-pk}N_{SM}V_{nom}^2} \tag{4.60}$$

Considering that the effect of switching is negligible, ΔE_{CL} can be estimated with reasonable accuracy by first integrating the theoretical CL power expressions and then sizing the energy deviation between the extreme points of the instantaneous energy function (IEF) for the worst-case operating conditions. Then, if N_{SM} in a CL is known and V_{nom} and ρ_{pk-pk} are fixed, a fair estimation of the minimum capacitor size can be made.

In the case of the SMPC, the UPP/LOW CLs are identical and although the IEFs for both CLs would slightly differ, the peak-to-peak energy ripple and hence, the capacitor sizes are the same. However, MID CLs have an entirely different IEF which means that the capacitors in this CL should be sized separately from the other two. The IEFs for UPP/LOW and MID CLs, plotted for $M = M_{ss}$ and normalized

to $\frac{P_{rated}}{3\omega}$, are shown in Figures (4.14) and (4.15) respectively for $\phi = 0$ and $\phi = \frac{\pi}{2}$. As expected, the lowest frequency component in the MID CL energy ripple is at twice the fundamental frequency.

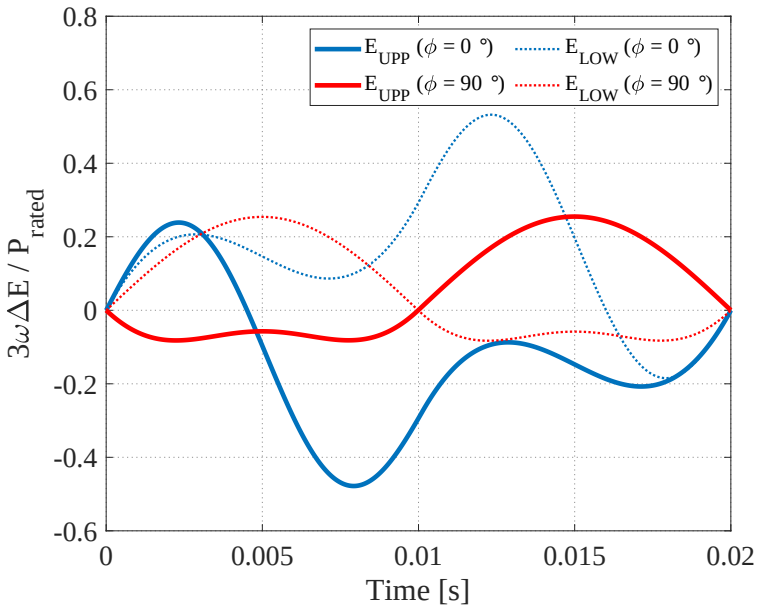


Figure 4.14: Energy functions for UPP/LOW CLs normalised to $\frac{P_{rated}}{3\omega}$ plotted for active power only (blue) and reactive power only (red)

To illustrate the variation in ΔE_{CL} over the P-Q operating region and for different modulation indexes, polar plots are presented in Figures (4.16) and (4.17) for a single UPP/LOW CL and a single MID CL respectively. The radii on these polar plots represent $\frac{3\omega\Delta E_{CL}}{P_{rated}}$ against the angle ϕ considering only the boundary points on the P-Q envelope for three different M values with the following significance:

- **M=0.9** is generally used in the case of a half-bridge MMC.
- **M=1.57** is the 'sweet-spot' modulation index of the SMPC
- **M=2.0** refers to the maximum achievable modulation index of the SMPC in the case when SMs in UPP/LOW CLs are only composed of FBs

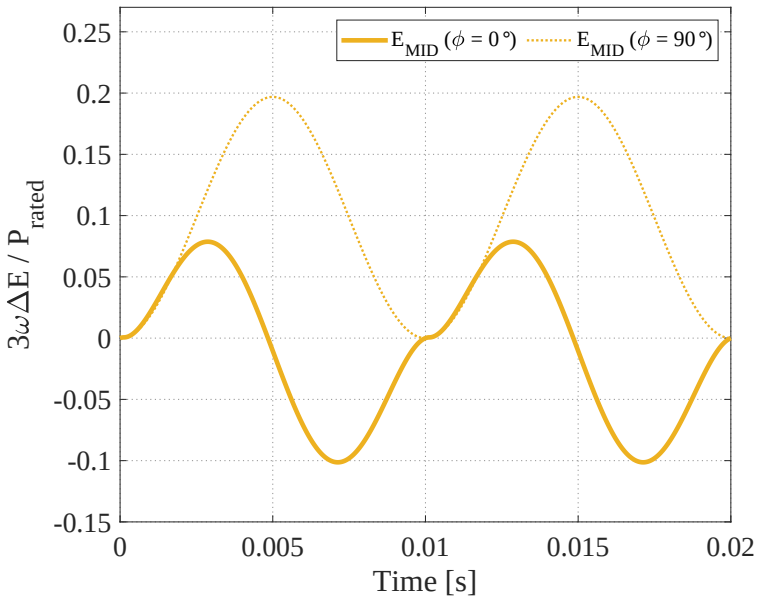


Figure 4.15: Energy functions for MID CLs normalised to $\frac{P_{rated}}{3\omega}$ plotted for active power only (solid yellow) and reactive power only (dotted yellow)

The minimum sizes for the UPP/LOW and MID CL capacitors can then be calculated using the worst-case energy deviation values (ΔE_{CL}^{wc}) from their respective plots and substituting them in Eq. (4.60). For the sake of an example, at $M = M_{ss} = 1.57$, $\frac{3\omega\Delta E_{CL}}{P_{rated}}$ takes the most extreme values of 0.7728 and 0.2871 for UPP/LOW and MID CLs respectively, both occuring at $\phi = -158.2°$, and the minimum capacitor size can be expressed as:

$$C_{SM}^{upp/low} \geq \frac{0.78 P_{rated}}{3\omega\rho_{pk-pk} N_{SM}^{upp/low} V_{nom}^2}$$

$$C_{SM}^{mid} \geq \frac{0.29 P_{rated}}{3\omega\rho_{pk-pk} N_{SM}^{mid} V_{nom}^2}$$

An observation that can be made from Figures (4.16) and (4.17) is that ΔE_{CL}^{wc} at $M = M_{ss} = 1.57$ is lower than ΔE_{CL}^{wc} at the other two M values (one higher than M_{ss} and the other lower than M_{ss}) for both UPP/LOW and MID CLs. Although it cannot be established that ΔE_{CL}^{wc} takes the smallest value at $M = M_{ss}$ from this

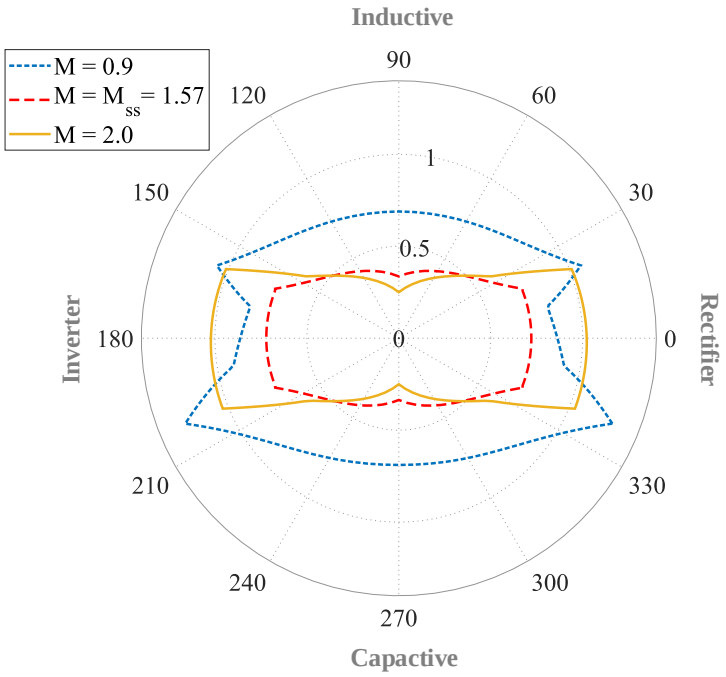


Figure 4.16: $\frac{3\omega\Delta E_{CL}}{P_{rated}}$ against ϕ for UPP/LOW CLs considering only the boundary points on the P-Q envelope for different modulation index values

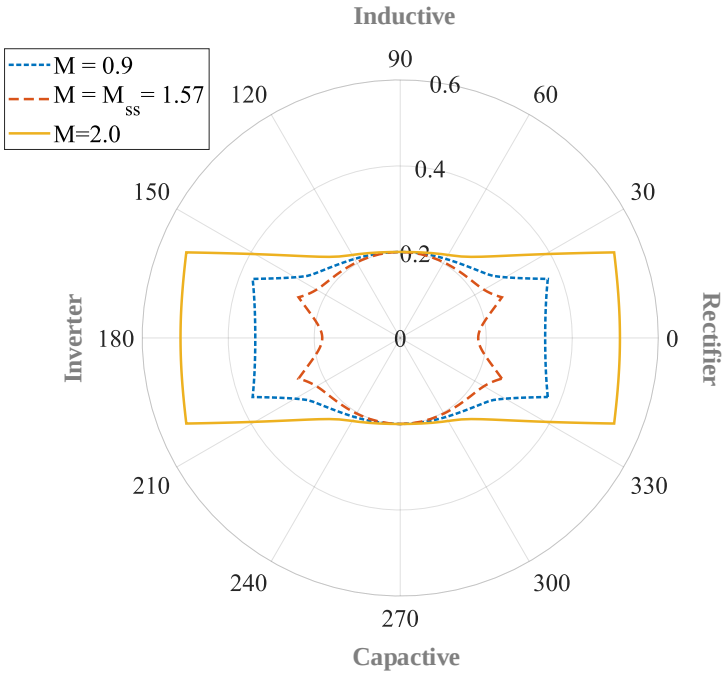


Figure 4.17: $\frac{3\omega\Delta E_{CL}}{P_{rated}}$ against ϕ for MID CLs conidering only the boundary points on the P-Q envelope for different modulation index values

observation alone, it can be deduced that ΔE_{CL}^{wc} varies non-linearly with the changes in M values, and may potentially minimise at a certain M value close to M_{ss}. In fact, this observation provides the motivation to study the optimisation of the modulation index which is the subject of the next sub-section.

4.5.4 Modulation index optimisation

In the SMPC, the nominal modulation index of the converter can be chosen between the range $0.9 \leq M \leq 2.0$ for the system specified in Table (4.1) by accordingly setting the transformer turns-ratio, assuming that the choice of cell formation in UPP/LOW CLs (either FBs or hybrid CLs) is made accordingly.

It has been established thus far that a smaller ΔE_{CL}^{wc} in a CL will result in smaller SM capacitor sizes if N_{SM}, V_{nom} and ρ_{pk-pk} are fixed and hence, minimising ΔE_{CL}^{wc} may lead to a reduction of the converter size. However, it must be noted that in the SMPC, the following quantities are also a function of M:

- Peak converter output voltage that dictates the N_{SM} needed in the MID CLs
- Balancing second harmonic required for energy management that can impact the N_{SM} required in the UPP/LOW CLs

Thus, it can be concluded that in order to allow the smallest possible converter size, the parameter chosen for minimisation should incorporate both the SM capacitor size and the number of SMs in the whole converter, and hence, an optimisation of the modulation index based on the minimisation of the energy storage in the converter is proposed.

The energy storage requirement of a multilevel converter is generally expressed as a fraction of the rated active or apparent power and has the units of 'kJ/MW' or 'ms', and is used as an approximate measure of the converter size. For the SMPC, the

energy storage requirement (called H_c in this thesis) can be expressed as:

$$H_c = 3 \times \left(\frac{10^3}{P_{rated}}\right)\left(N_{SM}^{upp/low} C_{SM}^{upp/low} V_{nom}^2 + \frac{1}{2} N_{SM}^{mid} C_{SM}^{mid} V_{nom}^2\right) \tag{4.61}$$

Mathematically, the optimisation function for the modulation index for a given system is expressed as:

$$M_{opt} = \min_{M\in[0.9,2.0]}\left(\max_{\phi\in[0,2\pi]}\left(H_{c_{(P_{rated},Q_{rated})}}(\phi)\right)\right) \tag{4.62}$$

This function translates to finding the M value at which the worst-case H_c for given system ratings is the lowest. In this thesis, this optimisation is performed for the system specifications in Table (4.1) by stepping M from 0.9 to 2.0 in increments of 0.01 and for every M value, the following is performed:

- ϕ is swept from 0 to 2π considering only the points on the P-Q envelope in Figure (4.13) and H_c is computed for every ϕ value to obtain the array H_c^{arr}
- $\max(H_c^{arr})$ is computed to obtain the worst-case H_c^{wc}
- H_c^{wc} is plotted against the corresponding M value relative to M_{ss}

The results from this analysis are presented in Figure (4.18). As expected, H_c^{wc} varies non-linearly with changing M and a minima occurs at $M = 0.84M_{ss}$. This M value is regarded as the optimum modulation index value M_{opt} that results in the smallest energy storage of the converter with $H_c^{wc} = 12.08$ kJ/MW.

It is worth mentioning here that despite the fact that the solution for M_{opt} presented here is for a specific set of system ratings, $M_{opt} = 0.84M_{ss}$ is a general solution for converter size optimisation for any set of system ratings, provided that the ratio of reactive power capability to active power capability $\left(\frac{Q_{rated}}{P_{rated}} = 0.4\right)$ is respected.

In this thesis, the SMPC is optimised for converter size reduction and hence, the converter is always operated at the optimum M value. $M_{opt} = 0.84M_{ss} \approx 1.32$ refers

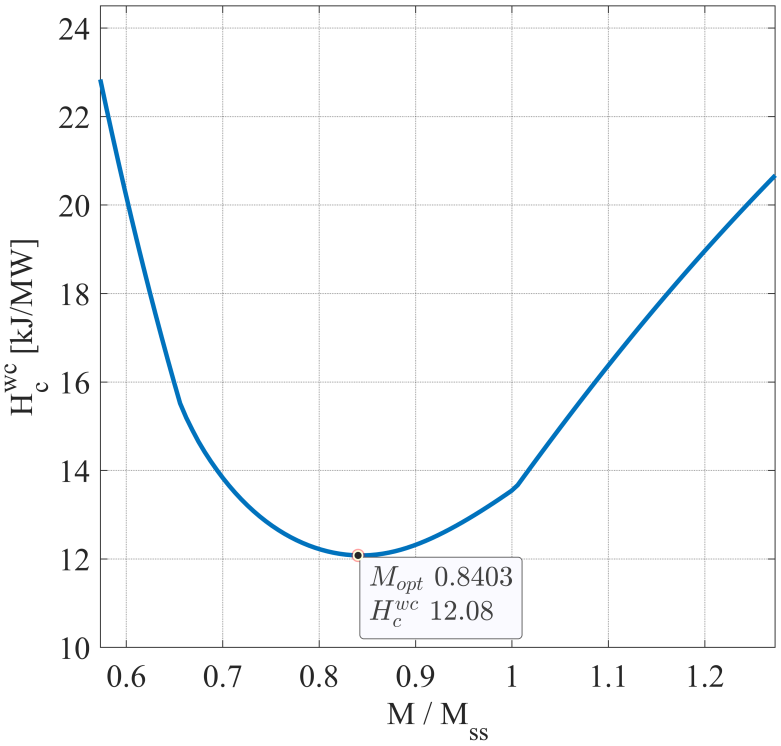


Figure 4.18: Optimisation of M based on energy storage minimisation

to over-modulation and hence, the choice of all or partial FBs in UPP/LOW CLs proposed in Section (4.2) is justified.

4.5.5 Solving converter parameters for M_{opt}

In this sub-section, the numerical solutions for converter parameters for the system ratings of Table (4.1) are presented. The reason for finding numerical solutions is to facilitate a quantitative comparison with the MMC later on in this chapter. The number of SMs, capacitor sizes and the energy storage values are computed for the SMPC operating at a modulation index of $M_{opt} = 1.32$.

From the plot of $\frac{2|k_{2\omega}|}{V_{dc}}$ against ϕ in Figure (4.19), the worst-case balancing second harmonic required is $k_{2\omega}^{wc} = 0.0608V_{dc}$ at $\phi = 21.8°$. Substituting this in Eq. (4.54),

the number of SMs in UPP/LOW CLs are calculated as:

$$N_{SM}^{upp/low} = \frac{0.53V_{dc}}{V_{nom}} = 7.07 \Rightarrow \mathbf{8\ SMs}$$

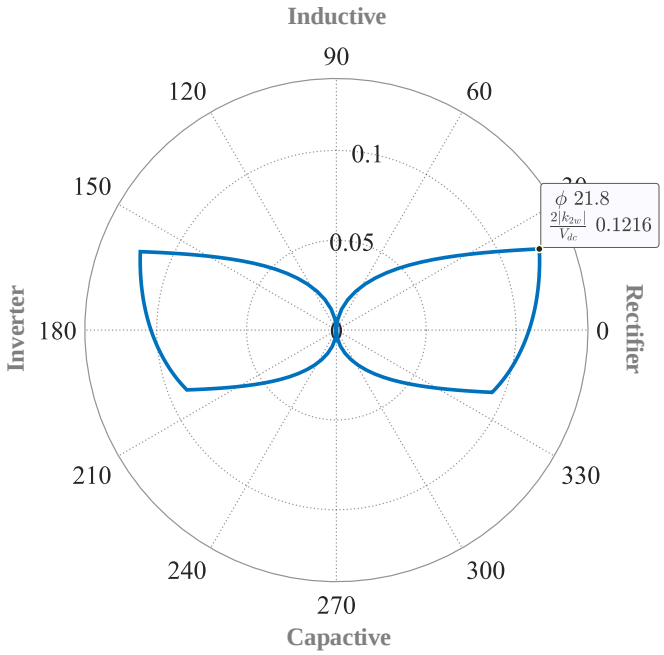


Figure 4.19: $\frac{2|k_{2\omega}|}{V_{dc}}$ against ϕ considering only the boundary points on the P-Q envelope for M_{opt}

The peak converter AC output voltage at $M_{opt} = 0.84M_{ss}$ is $\hat{V}_c = 13.19kV$. The number of SMs in MID CL are then evaluated as:

$$N_{SM}^{mid} = \frac{\hat{V}_c}{V_{nom}} = 8.79 \Rightarrow \mathbf{9\ SMs}$$

Because of over-modulation, the minimum number of FBs required in UPP/LOW CLs to produce the negative portion of the CL voltage are computed using Eq. (4.56) as:

$$N_{SM_{FB}}^{upp/low} = \frac{\left|0.47V_{dc} - \hat{V}_c\right|}{V_{nom}} = 2.43 \Rightarrow \mathbf{3\ FB\ SMs}$$

And the number of HBs as:

$$N_{SM_{HB}}^{upp/low} = N_{SM}^{upp/low} - N_{SM_{FB}}^{upp/low} \Rightarrow \mathbf{5\ HB\ SMs}$$

Lastly, the number of IGBTs at each DS switch position can be obtained by:

$$N_{IGBT}^{DS} = \frac{\hat{V}_c}{V_{nom}} \Rightarrow \mathbf{9\ IGBTs}$$

Thus, in total, the SMPC for the given system ratings has **25 SMs** in one converter phase, out of which **6** are **FB SMs** and **19** are **HB SMs**. In addition, there are a total of **18 IGBTs** in the DS configuration. The total IGBT count of the whole converter is calculated as:

$$N_{IGBT}^{tot} = 3 \times \left(4 \times N_{SM_{HB}}^{upp/low} + 2 \times N_{SM}^{mid} + 8 \times N_{SM_{FB}}^{upp/low} + 2 \times N_{IGBT}^{DS}\right) = 240$$

It is worth mentioning here that any comparison of the total IGBT count in the SMPC with other multilevel topologies must take into account the fact that the current in the MID CL is considerably smaller than the UPP/LOW CL currents. A quick analysis of the worst-case RMS currents at M_{opt} suggests a ratio of $\frac{I_{UPP/LOW_{rms}}^{wc}}{I_{MID_{rms}}^{wc}} = 3.39$. This effectively means that IGBTs that are rated for a much less current than the ones in UPP/LOW CLs, can be employed in the MID CLs.

The SM capacitor sizes are computed at M_{opt} using the method discussed in Section (4.5.3). Normalised energy deviation for a single UPP/LOW and a single MID CL are shown in Figure (4.20). $\frac{3\omega\Delta E_{CL}}{P_{rated}}$ takes the most extreme values of 0.6583 at $\phi = -21.8°$ and 0.2016 at $\phi = 158.2°$ for UPP/LOW CL and MID CL respectively. The minimum capacitor sizes are calculated as:

$$C_{SM}^{upp/low} \geq \frac{0.6583 P_{rated}}{3\omega\rho_{pk-pk} N_{SM}^{upp/low} V_{nom}^2}$$
$$C_{SM}^{upp/low} \geq \mathbf{3.88\ mF}$$

$$C_{SM}^{mid} \geq \frac{0.2016 P_{rated}}{3\omega\rho_{pk-pk} N_{SM}^{mid} V_{nom}^2}$$
$$C_{SM}^{mid} \geq \mathbf{1.06\ mF}$$

Sizing calculations for the SMPC are summarised in Table (4.2).

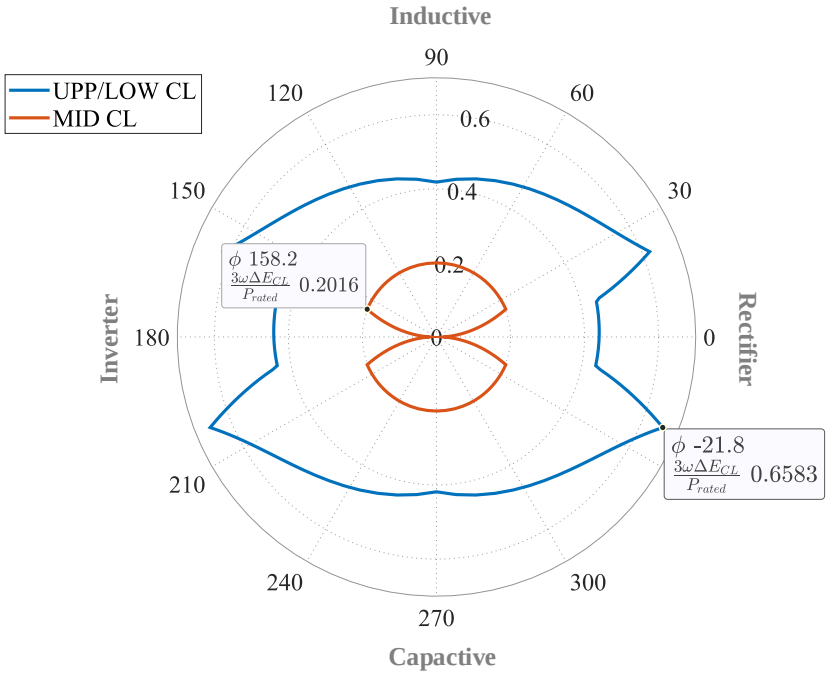


Figure 4.20: $\frac{3\omega\Delta E_{CL}}{P_{rated}}$ against ϕ for UPP/LOW CLs (blue) and MID CLs (red) considering only the boundary points on the P-Q envelope for M_{opt} values

Calculated parameters for the SMPC	
M	$0.84M_{ss}$
Number of SMs	
$N_{SM}^{upp/low}$	8 (5 HBs + 3 FBs)
N_{SM}^{mid}	9 HBs
N_{IGBT}^{DS}	9 IGBTs per DS
N_{IGBT}^{tot}	240 IGBTs
Capacitor sizes	
$C_{SM}^{upp/low}$	3.88 mF
C_{SM}^{mid}	1.06 mF
Energy storage	
H_c	12.08 kJ/MW

Table 4.2: Parameter sizing of the SMPC for the system ratings in Table 4.1

4.6 Hybrid Chainlinks

Optimization of the SMPC for energy storage reduction requires the converter to operate with a modulation index of $M_{opt} \approx 1.32$ and as a consequence of the chosen CL wave-shaping, the UPP/LOW CLs are required to synthesise negative voltages during normal operation. The ratio of the worst-case peak negative voltage to the worst-case peak positive voltage generated by the UPP/LOW CLs ($NPR^{wc}_{upp/low}$) is given as:

$$NPR^{wc}_{upp/low} = \frac{\left|\frac{1}{2}(V_{dc} - |k^{wc}_{2\omega}|) - \hat{V}^{wc}_{c}\right|}{\frac{1}{2}(V_{dc} + |k^{wc}_{2\omega}|)}$$

At M_{opt}, $NPR^{wc}_{upp/low} = 0.38$ which means that the required negative voltage can be generated if only 38% of the total SMs in UPP/LOW CLs are FBs. Hence, for the case of optimising the converter for the lowest energy storage by operating at M_{opt}, using all FBs will increase conduction losses unnecessarily and using Hybrid Chainlinks (H-CLs) is a better solution.

4.6.1 Capacitor voltage balancing with H-CL

Generally, in multilevel CLs that are composed of only one type of cells, the principle of SM capacitor voltage balancing is to sort the insertion priority of the SMs based on whether their voltages are above or below the nominal value, the direction of the current and, additionally in the case of FBs, whether the generated voltage state is positive or negative. Since, in single cell-type CLs, there is no restriction on the number of SMs that can take part in the construction of the CL output voltage at any given point over a fundamental cycle due to all being the same type (either HBs or FBs), the sorting mechanism can naturally ensure that all SMs in a CL experience roughly a similar deviation in their energy content with time.

However, this does not remain the case when an H-CL is required to produce a voltage

at its output that takes both positive and negative values under normal steady-state operation. The method of voltage synthesis with an H-CL when the CL peak negative voltage is smaller than the CL peak positive voltage ($NPR < 0.5$), which is the case for the UPP/LOW CLs in the SMPC operating at M_{opt}, is to employ both HBs and FBs in the positive voltage region and to utilise only FBs and bypass HBs in the negative voltage region. The consequence of this action is that for the negative voltage region, the HBs will maintain their energy while the FBs will see their energy deviate away from the mean value. This will result in dissimilar deviation in the energy content with time of the two types of SMs. However, it is not a problem in itself as long as the energies of both SM types at the start and end of the cycle are the same in steady-state i.e. the net energy difference in each cycle is zero. The voltage sharing and sorting mechanism for an H-CL is illustrated in Figure (4.21) using a flow diagram. The positive current direction is assumed as current entering the H-CL from its negative terminal to maintain consistency with the current convention assumed in Figure (4.1) for the SMPC.

4.6.2 Full-Bridges balanceability analysis

In order for H-CLs to successfully operate, the mean energies of both types of SMs in an H-CL taken over each cycle should be constant from one cycle to the next. For HBs, this can usually be ensured if the current through the H-CL is bi-directional. However, since only FBs can be utilised in the negative voltage period, their energy content may see either only a sharp increase or only a sharp decrease if there is no change in the current sign during that period which is the case for the UPP/LOW CLs in the SMPC, as can be seen from Figures (4.10) and (4.11) presented earlier assuming unity power factor operation. This means that in some operating conditions, the sorting mechanism may not be able to balance the energy of the FBs.

Hence, a FB 'balanceability' analysis is proposed in this thesis that is based on investigating whether the energy lost/gained by the FBs in the negative voltage

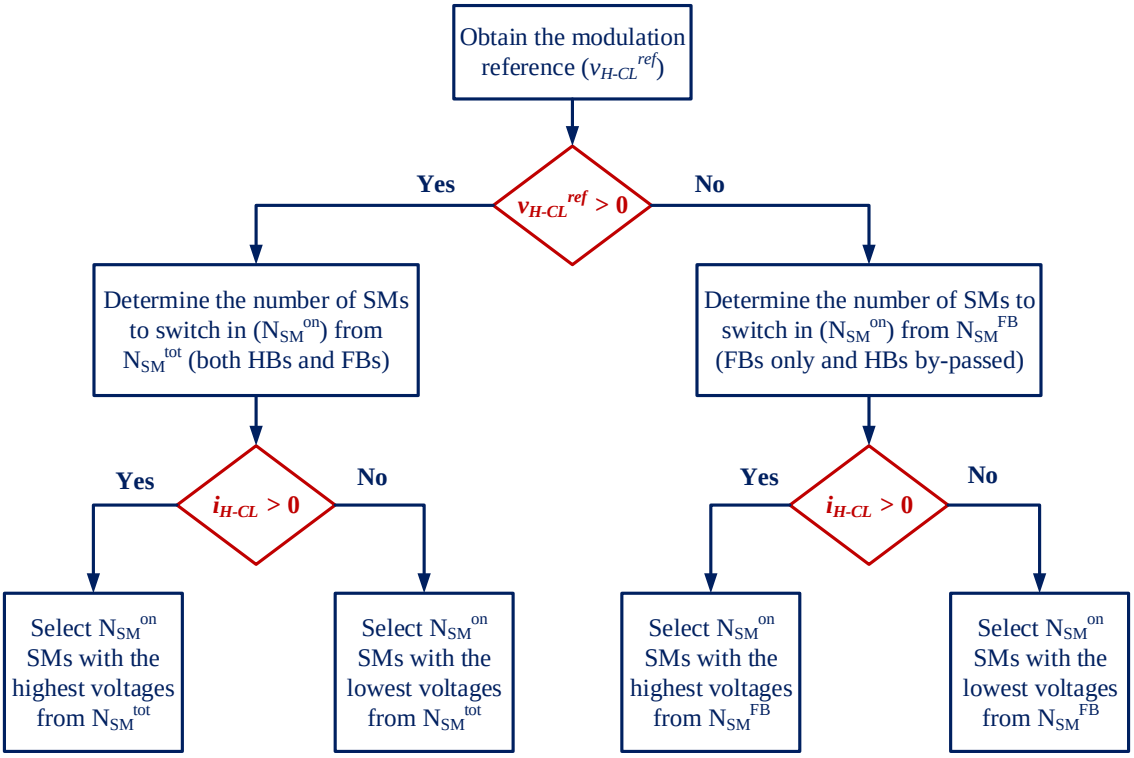


Figure 4.21: Voltage sharing and sorting mechanism for H-CL

region is recovered/released in the positive voltage region for a given operating point. To explain the concept, idealised UPP/LOW CL voltages and currents for full rated power and unity power factor at M_{opt} are taken as example in Figure (4.22) with regions marked from A-E. In Region A which is the negative voltage region, energy is lost/gained by the FBs ($E_{FB}^{loss/gain}$). Assuming that the sorting algorithm will take care of the appropriate switching durations of FBs, the analysis checks whether $E_{FB}^{loss/gain}$ in Region A can be recovered/released ($E_{FB}^{rec/rel}$) in Regions B,C,D and E combined. It should be noted that for different P-Q operating points, the CL current will have a different shape because of different oscillatory components which means:

- In Region A, the current will peak at some P-Q points and will not peak at other, so $E_{FB}^{loss/gain}$ will vary
- The Regions B/C/D/E will have different widths (or there may be less or more

'recovered/released' regions) and hence $E_{FB}^{rec/rel}$ will vary

This explains why the energy of the FBs will not be balanceable for some operating points with the absence of Q being the worst-case scenario.

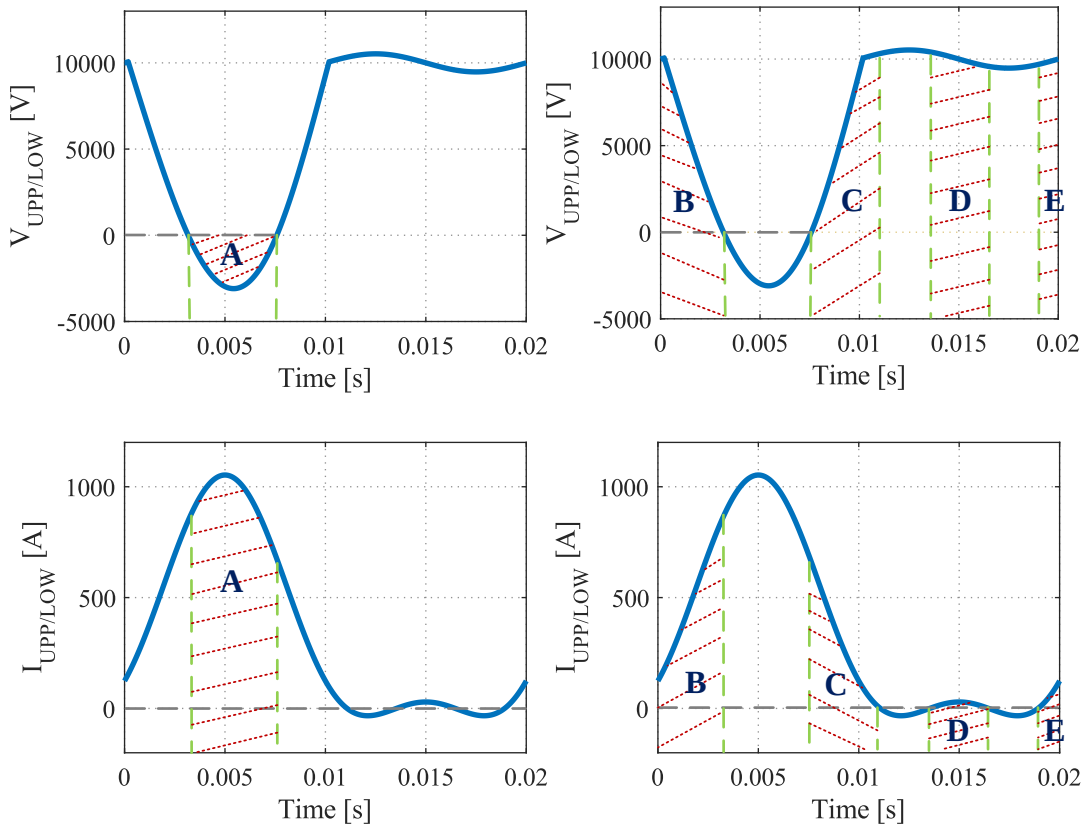


Figure 4.22: - (Left): Idealised UPP/LOW voltage (top) and current (bottom) showing Region A where energy is lost/gained by the FBs - (Right): Idealised UPP/LOW voltage (top) and current (bottom) showing Regions B,C,D and E where energy lost in Region A is recovered/released by the FBs

To conduct this analysis, the idealised FB instantaneous function is approximated as shown in Figure (4.23). The assumption made for the approximation is that within the positive voltage region, the sorting algorithm will naturally ensure maximum usage of FBs in Regions B,C,D and E to balance their energy and minimum usage elsewhere. The regions within the positive voltage region that are outside of B,C,D and E are ignored in the calculation of $E_{FB}^{rec/rel}$. The net FB energy (E_{FB}^{net}) is calculated

as follows:

$$E_{FB}^{net} = \left|E_{FB}^{loss/gain}\right| - \left|E_{FB}^{rec/rel}\right|$$

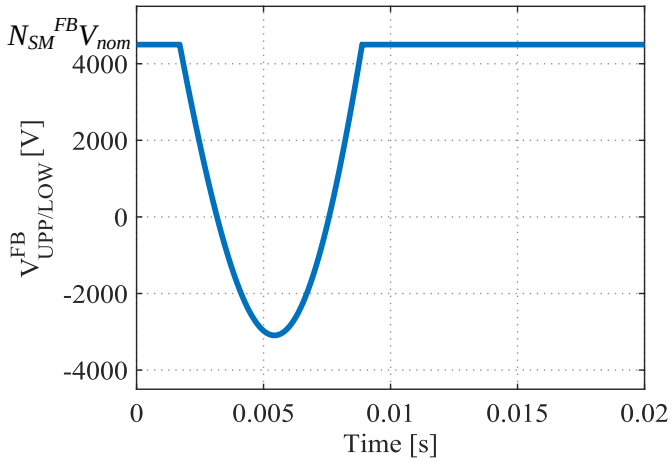
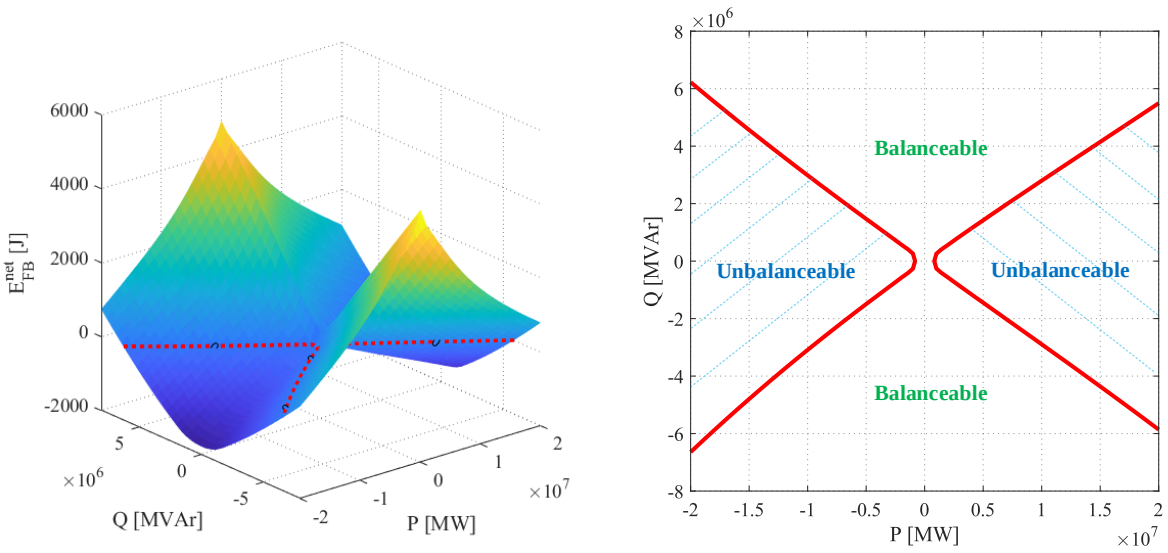


Figure 4.23: Approximation for idealised FB instantaneous voltage function

E_{FB}^{net} is calculated for a sweep of the P-Q operating region and shown in a 3D-plot in Figure (4.24a). A positive E_{FB}^{net} means that the region is balanceable whereas a negative E_{FB}^{net} means it is unbalanceable. The $E_{FB}^{net} = 0$ contours are then extracted and shown on a P-Q plot in Figure (4.24b). These contours serve as lines of demarcation between the balanceable and unbalanceable regions. It can be observed that for M_{opt}, operation at P_{rated} with unity power factor lies in the unbalanceable region but with the addition of rated Q, it becomes possible to balance the FBs which validates the hypothesis about the absence of Q being the worst-case scenario for FB balanceability. In order to identify what possible changes can result in the FBs being balanceable over the complete P-Q region, the following two scenarios are considered:

- **Increasing the number of FBs**: Keeping the same NPR, an increase in the number of FBs will impact the FB instantaneous function in Fig (4.23) which, in turn, will impact $E_{FB}^{rec/rel}$ and hence, the balanceability of FB energies. Intuitively, having a total number of FBs larger than ones generating negative voltage states will improve the ability of the sorting mechanism to balance their energies. A term $\frac{F}{N}$ is defined, as the ratio of FBs to the total number of SMs



(a) (b)

Figure 4.24: (a) E^{net}_{FB} shown as a function of the P-Q operating region with the contour $E^{net}_{FB} = 0$ marked (b) $E^{net}_{FB} = 0$ contour shown on the P-Q plane

in the CL, to study this effect.

- **Changing the modulation index**: Recalling the effect of modulation index M on the CL energies in the converter from previous sections, the effect of changing M on the FB balanceability is also considered.

To investigate these two scenarios, it is proposed that the minimum value of the E^{net}_{FB} function is looked at for every incremental step of the independent variables i.e. $\frac{F}{N}$ and M. On the resulting plots, the point where $\min(E^{net}_{FB})$ crosses zero will be the point of critical balanceability (PoCB). The result of the analyses are presented in Figures (4.25) and (4.26). From Figure (4.25), it is observed that for $NPR = 0.38$ and operating at $M_{opt} = 0.84 M_{ss}$, the PoCB occurs at $\frac{F}{N} = 0.59$ which implies that more than 59% of the SMs have to be FBs in order for them to be balanceable over the complete P-Q region. This is not desirable since it would increase the losses and will almost defeat the purpose of using H-CLs.

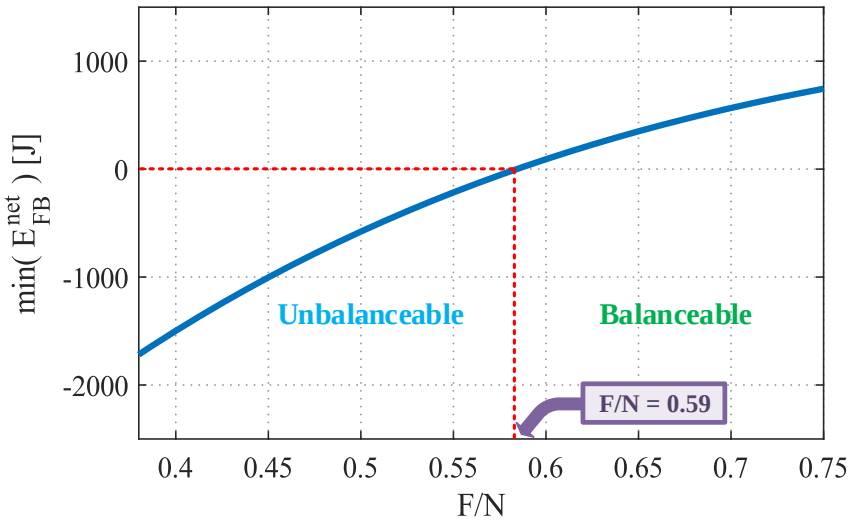


Figure 4.25: Effect on min (E_{FB}^{net}) of increasing the number of FBs

On the other hand, when the impact of M is considered, for $NPR = \frac{F}{N} = 0.38$, the PoCB occurs at $M = 0.79M_{ss}$ which is only a 5% change from $M_{opt} = 0.84M_{ss}$. Hence, reducing the optimum operational modulation index to $M_{opt}^{H-CL} < 0.79M_{ss}$ is a better choice since the compromise on the converter's energy storage will be small because of the H_c^{wc} vs M curve of Figure (4.18) being relatively flat around M_{opt}.

It is important here to mention that the analysis presented above only approximates the influence of different operating conditions (P-Q values, $\frac{F}{N}$ and M) on FB balanceability since it considers theoretical waveforms and estimates the action of the sorting algorithm. However, the trends in FB balanceability with varying operational set-points are accurate. Hence, the values of $\frac{F}{N}$ and M_{opt}^{H-CL} where PoCB occurs are used with an error margin between $\pm 5\%$ and $\pm 10\%$. Respecting this error margin and choosing the change in M to allow the FBs to be balanceable over the complete P-Q region, M_{opt}^{H-CL} is selected as $\mathbf{0.75M_{ss}}$ for the SMPC with UPP/LOW CLs composed of H-CLs. However, if all FBs are used, $M_{opt} = 0.84M_{ss}$ will hold.

The converter parameters are re-sized for M_{opt}^{H-CL} and are presented in Table (4.3). It can be noticed that H_c is now 12.8 kJ/MW which is only a 6% increase compared to the $M_{opt} = 0.84M_{ss}$ case.

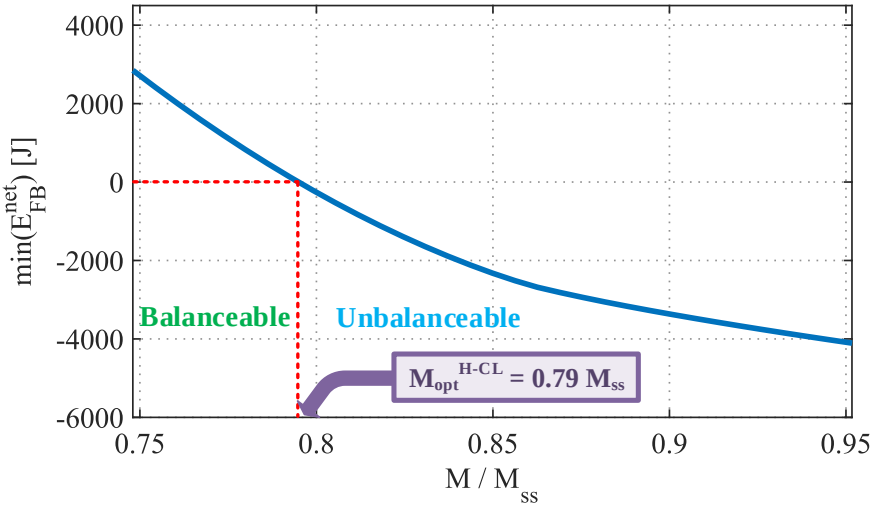


Figure 4.26: Effect on $\min\left(E_{FB}^{net}\right)$ of changing the modulation index M

Parameters for the SMPC with H-CLs	
M	$0.75M_{ss}$
Number of SMs	
$N_{SM}^{upp/low}$	8 (5 HBs + 3 FBs)
N_{SM}^{mid}	9 HBs
N_{IGBT}^{DS}	9 IGBTs per DS
N_{IGBT}^{tot}	210 IGBTs
Capacitor sizes	
$C_{SM}^{upp/low}$	4.05 mF
C_{SM}^{mid}	1.2 mF
Energy storage	
H_c	12.8 kJ/MW

Table 4.3: Parameter sizing of the SMPC with H-CLs in UPP/LOW CLs for the system ratings in Table 4.1

4.7 Comparison with the MMC

In order to present the benefits of the SMPC for HVDC converters, a comparative study using a standard MMC with HB SMs as the benchmark is conducted in this thesis. Although a comparison with a range of other multilevel converter topologies would be interesting, it is limited to only the MMC so that a detailed and fair comparative analysis can be made while keeping the same assumptions and margins that were used for the sizing of the SMPC parameters.

The study in this thesis will compare the number of SMs, capacitor sizes, energy storage requirements, IGBT/device count, semiconductor requirements and power losses between the two converters. The number of SMs have an effect on the overall system complexity as more auxiliary control systems will be needed for a higher number of SMs. The capacitor size impacts the size of the SMs. Energy storage of the converter gauges the combined effect of the number of SMs and capacitor size and serves as a useful measure of the overall size, volume and weight of the converter. The IGBT/device count and ratings determine the fixed setup cost and power losses influence the operating cost of a plant.

The fixed set of system ratings used for the comparison are listed in Table (4.1) that are based on the parameters of an existing MMC demonstrator built by Alstom Grid (now GE) in Stafford, UK [76]. All power/voltage ratings are kept the same for the two converters. Note that the AC line/transformer leakage inductance is ignored to maintain consistency with the analyses in previous sections. The SMPC, with its UPP/LOW CLs formed of H-CLs, is operated at the optimum modulation index $M_{opt}^{H-CL} = 0.75M_{ss} \approx 1.18$. For the MMC, the commonly used modulation index of 0.9 is selected, which is not optimised since a change in M does not affect much the energy storage of the half-bridge MMC, in which M cannot go higher than 1.

4.7.1 Number of SMs, capacitor sizes and energy storage

The number of SMs required in the CLs, sizes of the capacitors and energy storage requirement of the SMPC were computed for the given system ratings in Section (4.5). Following the same procedures, these parameters are now calculated for the MMC.

Recalling the operation of the MMC presented in the literature review section of this thesis, the CL voltages and currents for phase a (considering identical and balanced phases) of the MMC can be expressed as:

$$\begin{aligned} v^{a}_{upp/low_{MMC}} &= \frac{V_{dc}}{2} \mp \hat{V}_c \sin(\omega t) \\ i^{a}_{upp/low_{MMC}} &= \pm \frac{\hat{I}}{2} \sin(\omega t - \phi) + \frac{I_{dc}}{3} \end{aligned} \tag{4.63}$$

where only theoretical waveforms are considered and it is assumed that the circulating current of the MMC is suppressed. Moreover, no third harmonic is added in the modulation of the MMC which does not affect the comparative analysis as in theory, the third harmonic could also be added to the SMPC for the same reasons as in the MMC.

Without considering any redundancy margins in order to keep consistency with the case of the SMPC, the CLs in the MMC need to be rated as follows:

$$N_{SM}^{MMC} = \frac{\frac{1}{2}V_{dc} + \hat{V}_c}{V_{nom}} \tag{4.64}$$

By calculation, $\hat{V}_c = 9kV$ and hence $N_{SM}^{MMC} = 12.67 \Rightarrow \mathbf{13}$.

For the estimation of energy deviation in MMC CLs, similar to the case of the SMPC, a script is implemented. Inside the script, the outer boundaries of the P-Q envelope in Fig. (4.13) are swept and the IEF is computed by integrating the product of voltage and current equations in Eq. (4.63). The extreme values of IEF over a cycle is the peak-to-peak energy deviation (ΔE_{CL}^{MMC}) that is normalised to $\frac{P_{rated}}{3\omega}$ and

plotted against ϕ in Figure (4.27). $\frac{3\omega\Delta E_{CL}}{P_{rated}}$ takes the most extreme value of 1.801 at $\phi = 21.8°$ and hence, assuming the same ρ_{pk-pk} and V_{nom} as in the case of the SMPC, the minimum SM capacitor size in the MMC is calculated as:

$$C_{SM}^{MMC} \geq \frac{1.801 P_{rated}}{3\omega\rho_{pk-pk} N_{SM}^{MMC} V_{nom}^2}$$

$$C_{SM}^{MMC} \geq \mathbf{6.53\ mF}$$

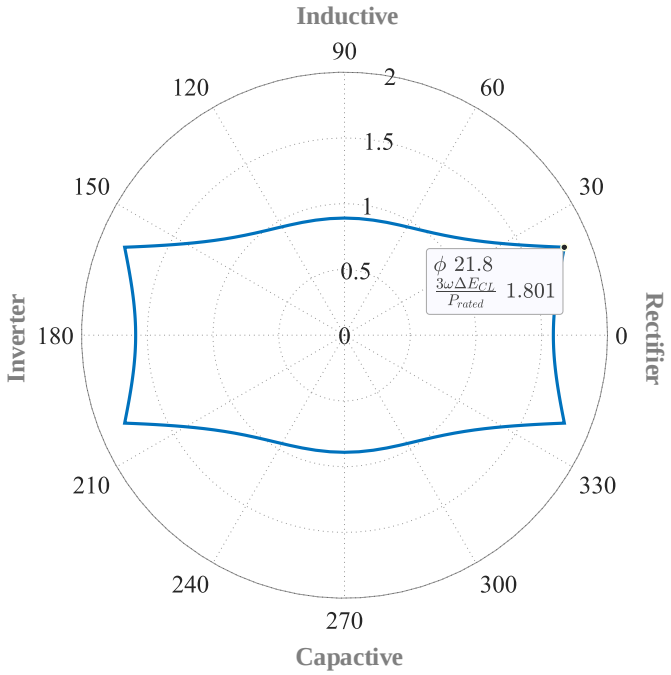


Figure 4.27: $\frac{3\omega\Delta E_{CL}}{P_{rated}}$ against ϕ for MMC CLs considering only the boundary points on the P-Q envelope

Energy storage requirement for the MMC is computed as:

$$H_c^{MMC} = \left(\frac{3 \times 10^3}{P_{rated}}\right)\left(N_{SM}^{MMC} C_{SM}^{MMC} V_{nom}^2\right) = \mathbf{28.7\ kJ/MW}$$

Thus, it can be concluded that the energy storage requirement of the SMPC (i.e. 12.8 kJ/MW) is **45%** of that of the MMC. This means that an SMPC converter will be considerably smaller in size compared to an MMC converter.

A visual comparison of the energy storage requirements between the two converters for different operational P-Q points is shown in Figure (4.28). An obvious observation

that can be made is that H_c^{SMPC} is smaller than H_c^{MMC} for the complete P-Q envelope boundary. In addition, it can also be noted that in case of only active power exchange, H_c^{SMPC} is 22 % of H_c^{MMC} whereas that figure is 66 % when only reactive power exchange takes place. However, in practice, the converter needs to be sized according to the worst-case values in order to supply both the rated P and Q without breaching any pre-set limits such as the voltage ripple in the SM capacitors. For this reason, a comparison of the worst-case H_c between the two converters makes the most sense and has already been respected in the comparisons presented earlier.

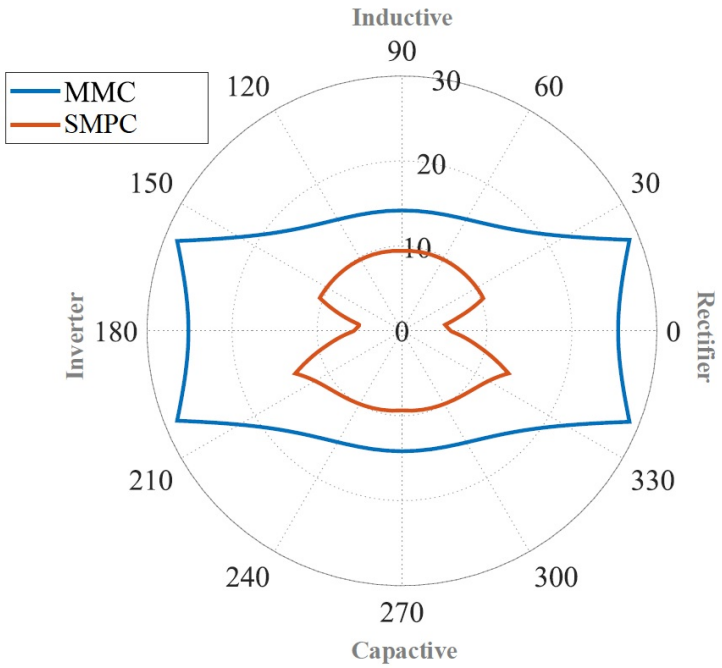


Figure 4.28: H_c against ϕ for the MMC (blue) and the SMPC (red) considering only the boundary points on the P-Q envelope

A summary of the comparison between the SMPC and the MMC is reported in Table (4.4). Compared to the MMC, the SMPC has a roughly similar number of SMs per phase (25 in the SMPC and 26 in the MMC), smaller capacitor sizes and, as presented above, a smaller energy storage requirement. On the other hand, the obvious disadvantage is that the overall number of IGBTs in the SMPC is 54% higher than in the MMC because of the additional devices in the DS configuration and the use of FBs in UPP/LOW CLs. However, in the SMPC, the rms current in MID CLs is

less than one-third of that in UPP/LOW CLs requiring the use of smaller current rated IGBTs in the former. The cost and size of an IGBT will be lower for a lower current rating and for this reason, a better approach is to compare the overall semiconductor requirements. In the interest of avoiding complexity and obtaining a quick analytical estimate, a method that expresses the overall semiconductor requirements as the product of the IGBT voltage rating, rms CL current and the total number of IGBTs is used in this thesis. It is assumed that all other variables are fixed for the two converters with only the CL current ratings impacting the semiconductor requirements and the actual conduction states within an SM are ignored. A term 'Total Device Power (TDP)' is defined that is expressed as follows for both the MMC and the SMPC:

$$TDP_{MMC} = \frac{1}{P_{rated}} \left(N^{tot}_{IGBT_{MMC}} V^{nom}_{SM} I^{rms^{wc}}_{MMC-CL} \right)$$

$$TDP_{SMPC} = \frac{1}{P_{rated}} \Big[\Big(3 \times 2 \times \left(N^{upp/low}_{SM_{FB}} \times 4 + N^{upp/low}_{SM_{HB}} \times 2 \right) \times V^{nom}_{SM} I^{rms^{wc}}_{upp/low} \Big) + \Big(3 \times 2 \times N^{mid}_{SM} V^{nom}_{SM} I^{rms^{wc}}_{mid} \Big) + \Big(3 \times 2 \times N^{DS}_{IGBT} V^{nom}_{SM} I^{rms^{wc}}_{DS} \Big) \Big]$$

By calculation for the system ratings under review, for the MMC, $I^{rms^{wc}}_{MMC-CL} = 654.6$ A and for the SMPC, $I^{rms^{wc}}_{upp/low} = 607.9$ A, $I^{rms^{wc}}_{mid} = 195.9$ A and $I^{rms^{wc}}_{DS} = 614.9$ A. For the DS configuration, devices with the same voltage ratings of those assumed in the rest of the converter are used. The TDP values calculated are $TDP_{MMC} = 7.66$ and $TDP_{SMPC} = 9.3$. Thus, it can be concluded that despite a 54% higher IGBT count, the semiconductor requirement for the SMPC is estimated to be only 21% -22% higher than that of the MMC.

	MMC	**SMPC**
M	0.9	1.178
Number of SMs		
$N_{SM}^{upp/low}$	13 HBs	8 (5 HBs + 3 FBs)
N_{SM}^{mid}	N/A	9 HBs
N_{IGBT}^{DS}	N/A	9 IGBTs per DS
N_{IGBT}^{tot}	156 IGBTs	240 IGBTs
Capacitor sizes		
$C_{SM}^{upp/low}$	6.53 mF	4.05 mF
C_{SM}^{mid}	N/A	1.2 mF
Energy storage		
H_c	28.7 kJ/MW	12.8 kJ/MW

Table 4.4: Comparison between the MMC and the SMPC for system ratings of Table 4.1

4.7.2 Converter losses

Once a VSC converter is analytically modelled, it becomes possible to determine the semiconductor losses in the converter using data supplied by device manufacturers. In this thesis, loss estimation of both the MMC and the SMPC is performed using both a script-based analytical approach and a switching simulation model. Ratings for the HVDC demonstrator listed in Table (4.1) are used for both converters to ensure consistency in the comparison.

In general, the converter semiconductor losses can be subdivided into conduction losses and switching losses. For multilevel converters, switching frequency is usually low and hence, conduction losses in the IGBTs and the anti-parallel diodes make a dominant contribution. Conduction losses are the result of the interaction of the

voltage drop across the device (applies to both IGBTs and diodes) during conduction and the current flowing through the device. Switching losses are caused because the transitions from on-state to off-state and vice versa do not occur instantly and the voltage across and current through the device are both non-zero during the transition period [77]. They can be further classified into turn-on switching losses and turn-off switching losses for IGBTs and reverse recovery loss for freewheeling diodes when they switch from the conduction to the blocking state (diode turn-off). Turn-on losses for the diodes are generally ignored as the transition from the blocking to the conduction state is much faster.

A derivation of the expressions to evaluate both conduction and switching power losses is now presented, first for a single IGBT/diode which is then extended to loss expressions for full CLs for the two separate cases of series-connected HBs and H-CLs. Starting with conduction losses, the instantaneous power loss in a device (IGBT/diode) in the on-state is given as:

$$p_{cond}^{device}(t) = v_{device}(t) \cdot i_{device}(t) \tag{4.65}$$

The voltage across the device is a time-varying function dependent on the device current that can be linearly approximated as:

$$v_{device}(t) = V_F + R_F \cdot i_{device}(t)$$

where V_F is the forward voltage of the device at zero current and R_F is the slope resistance for the device's output characteristics curve.

Before the instantaneous conduction loss can be expressed for a full CL, the conduction states of the basic building blocks, HB SMs and FB SMs, are considered based on the required SM output voltage and the direction of current flow. Figure (4.29) shows the structure of HB and FB SMs and also indicates the assumed positive current convention. All possible conduction states and the on-devices for each of these states are presented in Tables (4.5) and (4.6) for HB and FB SMs respectively.

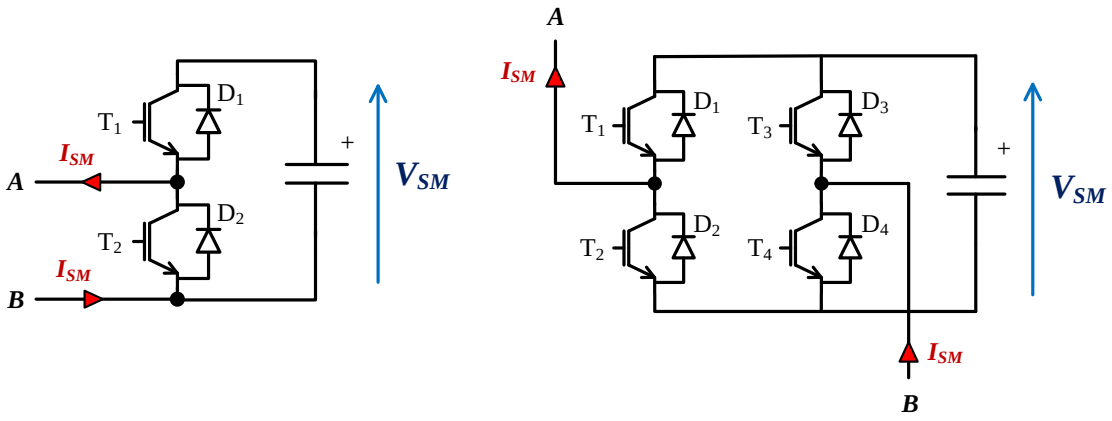


Figure 4.29: Half-Bridge SM (left) and Full-Bridge SM (right) indicating the current convention

$\mathbf{I_{SM}}$	$\mathbf{V_{AB}}$	**On-device**
$B \rightarrow A(+)$	$+V_{SM}$	T_1
$B \rightarrow A(+)$	0	D_2
$A \rightarrow B(-)$	$+V_{SM}$	D_1
$A \rightarrow B(-)$	0	T_2

Table 4.5: Half-Bridge conduction states

$\mathbf{I_{SM}}$	$\mathbf{V_{AB}}$	**On-device**
$B \rightarrow A(+)$	$+V_{SM}$	T_1&T_4
$B \rightarrow A(+)$	$-V_{SM}$	D_2&D_3
$B \rightarrow A(+)$	0	D_3&T_1 or T_4&D_2
$A \rightarrow B(-)$	$+V_{SM}$	D_1&D_4
$A \rightarrow B(-)$	$-V_{SM}$	T_2&T_3
$A \rightarrow B(-)$	0	D_1&T_3 or T_2&D_4

Table 4.6: Full-Bridge conduction states

The CLs in the MMC and the MID CLs in the SMPC are composed of series-connected HBs. The instantaneous functions for number of on-SMs and off-SMs are expressed as:

$$N_{ON}^{HB}(t) = \frac{v_{CL}(t)}{V_{nom}}$$
$$N_{OFF}^{HB}(t) = N_{SM}^{HB} - N_{ON}^{HB}(t)$$

where $v_{CL}(t)$ is the instantaneous CL voltage, V_{nom} is the nominal SM voltage and N_{HB}^{SM} is the total number of SMs in the HB CL.

The instantaneous conduction losses can then be expressed as:

$$p_{cond}^{HB}(t) = \begin{cases} N_{ON}^{HB}(t)P_{IGBT}\left(|i_{CL}(t)|\right) + N_{OFF}^{HB}(t)P_{diode}\left(|i_{CL}(t)|\right) & \text{if } (i_{CL}(t) > 0) \\ N_{OFF}^{HB}(t)P_{IGBT}\left(|i_{CL}(t)|\right) + N_{ON}^{HB}(t)P_{diode}\left(|i_{CL}(t)|\right) & \text{if } (i_{CL}(t) < 0) \end{cases}$$

For the UPP/LOW CLs in the SMPC, the recommendation in this thesis is to use hybrid CLs to keep the losses low without compromising the CL's ability to generate the necessary negative voltage. Hence, the loss estimation for H-CLs should take into account the durations for which both types of SMs will take part in the CL voltage construction. As it is very difficult to predict the actual SM selection and sorting action, especially in the positive voltage region, the FB instantaneous function is approximated as shown in Figure (4.23) for the reasons discussed in Section (4.6.2). With that approximation, the instantaneous functions for the number of on-SMs and off-SMs for both FBs and HBs in the H-CLs are expressed as:

$$N_{ON}^{FB^{H-CL}}(t) = \begin{cases} \dfrac{|v_{CL}(t)|}{V_{nom}} & \text{if } \left(v_{CL}(t) < N_{SM}^{FB^{H-CL}} V_{nom}\right) \\ N_{SM}^{FB^{H-CL}} & \text{if } \left(v_{CL}(t) \geq N_{SM}^{FB^{H-CL}} V_{nom}\right) \end{cases}$$

$$N_{OFF}^{FB^{H-CL}}(t) = N_{SM}^{FB^{H-CL}} - N_{ON}^{FB^{H-CL}}(t)$$

$$N_{ON}^{HB^{H-CL}}(t) = \begin{cases} 0 & \text{if } \left(v_{CL}(t) < N_{SM}^{FB^{H-CL}} V_{nom}\right) \\ \dfrac{\left|v_{CL}(t) - N_{SM}^{FB^{H-CL}} V_{nom}\right|}{V_{nom}} & \text{if } \left(v_{CL}(t) \geq N_{SM}^{FB^{H-CL}} V_{nom}\right) \end{cases}$$

$$N_{OFF}^{HB^{H-CL}}(t) = N_{SM}^{HB^{H-CL}} - N_{ON}^{HB^{H-CL}}(t)$$

where $v_{CL}(t)$ is the instantaneous voltage of the H-CL, V_{nom} is the nominal SM voltage and $N_{SM}^{HB^{H-CL}}$ and $N_{SM}^{FB^{H-CL}}$ are the total number of HB SMs and FB SMs in the H-CL respectively.

The instantaneous conduction losses in the H-CL are given as:

$$p_{cond}^{H-CL}(t)=\begin{cases} N_{ON}^{HB^{H-CL}}(t)P_{IGBT}(|i_{CL}(t)|)+N_{OFF}^{HB^{H-CL}}(t)P_{diode}(|i_{CL}(t)|)+2{\cdot}N_{ON}^{FB^{H-CL}}(t)P_{IGBT}(|i_{CL}(t)|), \\ \quad \text{if } \left(v_{CL}(t){\geq}N_{SM}^{FB}V_{nom} \,\&\&\, i_{CL}(t){>}0\right) \\ N_{OFF}^{HB^{H-CL}}(t)P_{IGBT}(|i_{CL}(t)|)+N_{ON}^{HB^{H-CL}}(t)P_{diode}(|i_{CL}(t)|)+2{\cdot}N_{ON}^{FB^{H-CL}}(t)P_{diode}(|i_{CL}(t)|), \\ \quad \text{if } \left(v_{CL}(t){\geq}N_{SM}^{FB}V_{nom} \,\&\&\, i_{CL}(t){<}0\right) \\ 2{\cdot}N_{ON}^{FB^{H-CL}}P_{IGBT}(|i_{CL}(t)|)+N_{OFF}^{FB^{H-CL}}\left(P_{diode}(|i_{CL}(t)|)+P_{IGBT}(|i_{CL}(t)|)\right)+N_{OFF}^{HB^{H-CL}}P_{diode}(|i_{CL}(t)|), \\ \quad \text{if } \left(v_{CL}(t){<}N_{SM}^{FB}V_{nom} \,\&\&\, \text{sgn}(v_{CL}(t)){>}0 \,\&\&\, i_{CL}(t){>}0\right) \\ 2{\cdot}N_{ON}^{FB^{H-CL}}P_{diode}(|i_{CL}(t)|)+N_{OFF}^{FB^{H-CL}}\left(P_{diode}(|i_{CL}(t)|)+P_{IGBT}(|i_{CL}(t)|)\right)+N_{OFF}^{HB^{H-CL}}P_{IGBT}(|i_{CL}(t)|), \\ \quad \text{if } \left(v_{CL}(t){<}N_{SM}^{FB}V_{nom} \,\&\&\, \text{sgn}(v_{CL}(t)){>}0 \,\&\&\, i_{CL}(t){<}0\right) \\ 2{\cdot}N_{ON}^{FB^{H-CL}}P_{diode}(|i_{CL}(t)|)+N_{OFF}^{FB^{H-CL}}\left(P_{diode}(|i_{CL}(t)|)+P_{IGBT}(|i_{CL}(t)|)\right)+N_{OFF}^{HB^{H-CL}}P_{diode}(|i_{CL}(t)|), \\ \quad \text{if } \left(v_{CL}(t){<}N_{SM}^{FB}V_{nom} \,\&\&\, \text{sgn}(v_{CL}(t)){<}0 \,\&\&\, i_{CL}(t){>}0\right) \\ 2{\cdot}N_{ON}^{FB^{H-CL}}P_{IGBT}(|i_{CL}(t)|)+N_{OFF}^{FB^{H-CL}}\left(P_{diode}(|i_{CL}(t)|)+P_{IGBT}(|i_{CL}(t)|)\right)+N_{OFF}^{HB^{H-CL}}P_{IGBT}(|i_{CL}(t)|), \\ \quad \text{if } \left(v_{CL}(t){<}N_{SM}^{FB}V_{nom} \,\&\&\, \text{sgn}(v_{CL}(t)){<}0 \,\&\&\, i_{CL}(t){<}0\right) \end{cases}$$

The instantaneous functions $p_{cond}^{HB}(t)$ and $p_{cond}^{H-CL}(t)$ can then be averaged over a fundamental period to obtain the conduction loss values for the respective CL.

Moreover, the conduction loss in the DS configuration in the SMPC also forms a considerable share of the total conduction loss of the converter. To obtain its expression, it is considered that S_1 is turned on during the positive AC half-cycle and S_2 in the negative AC half-cycle. The instantaneous conduction loss expression for the

DS configuration is presented as:

$$p_{cond}^{DS} = \begin{cases} N_{IGBT}^{DS^{S1}} P_{diode}\left(|i(t)|\right) & \text{if } (S_1 \text{ is on } \&\& \ i(t) > 0) \\ N_{IGBT}^{DS^{S1}} P_{IGBT}\left(|i(t)|\right) & \text{if } (S_1 \text{ is on } \&\& \ i(t) < 0) \\ N_{IGBT}^{DS^{S2}} P_{IGBT}\left(|i(t)|\right) & \text{if } (S_2 \text{ is on } \&\& \ i(t) > 0) \\ N_{IGBT}^{DS^{S2}} P_{diode}\left(|i(t)|\right) & \text{if } (S_2 \text{ is on } \&\& \ i(t) < 0) \end{cases}$$

where $i(t)$ is the AC side current.

In case of switching losses, as has been mentioned earlier, turn-on and turn-off losses for the IGBTs and only turn-off (reverse recovery) losses for the diodes are of relevance. Pre-determined information about turn-on, -off and reverse recovery energies for a single switching event at certain device current and voltage test points, can be used to estimate the switching loss function. The energies vary with the device current and hence, normalisation to the test values is necessary.

The instantaneous switching loss functions for both HB CL and H-CL are expressed below.

$$p_{sw}^{HB}(t) = f_{sw} N_{ON}^{HB}(t) \left(\frac{(E_{OFF} + E_{ON} + E_{REC})|i_{CL}(t)|V_{nom}}{V_{test} I_{test}} \right)$$

$$p_{sw}^{H-CL}(t) = \begin{cases} f_{sw} N_{ON}^{HB^{H-CL}}(t) \left(\frac{(E_{OFF} + E_{ON} + E_{REC})|i_{CL}(t)|V_{nom}}{V_{test} I_{test}} \right) \\ +2 \cdot f_{sw} N_{ON}^{FB^{H-CL}}(t) \left(\frac{(E_{OFF} + E_{ON} + E_{REC})|i_{CL}(t)|V_{nom}}{V_{test} I_{test}} \right), \\ \quad \text{if } \left(v_{CL}(t) \geq N_{SM}^{FB^{H-CL}} V_{nom} \right) \\ \\ 2 \cdot f_{sw} N_{ON}^{FB^{H-CL}}(t) \left(\frac{(E_{OFF} + E_{ON} + E_{REC})|i_{CL}(t)|V_{nom}}{V_{test} I_{test}} \right), \\ \quad \text{if } \left(v_{CL}(t) < N_{SM}^{FB^{H-CL}} V_{nom} \right) \end{cases}$$

where E_{OFF}, E_{ON} and E_{REC} are the turn-on, turn-off and reverse recovery energies that are usually provided by the device manufacturer in the datasheet and f_{sw} is the

switching frequency. Same as in the case of conduction losses, taking the average of these functions over a fundamental period gives the switching loss value for a CL. It must be noted that the DS configuration is switched at the AC line frequency and hence, the switching losses are negligible and are ignored in the calculations.

As mentioned above, loss estimation of VSC converters uses pre-determined device data and hence, device selection is an important step, particularly in a comparative study between two converters with different current ratings in their CLs. In the interest of ensuring fairness in the comparison, current ratings of the devices have been chosen to ensure that the current margin factor, i.e. the ratio of the rated device current to the rms current in the CL, is consistent for all CLs of both converters. The devices considered are 3.3kV HVIGBT modules with built-in anti-parallel diodes from Mitsubishi Electric because of an availability of a good range of current ratings for the same voltage rating. The worst-case rms currents for the CLs in the converters for the ratings of the HVDC demonstrator in Table (4.1) and the respective chosen devices are reported in Table (4.7).

Use	**Worst-case RMS Current**	**Manufacturer & Model**	**Rated Voltage**	**Rated Current**
MMC CLs	654.6 A	Mitsubishi Electric CM1200HC-66H	3.3 kV	1200 A
SMPC UPP/LOW CLs	607.9 A	Mitsubishi Electric CM1200HC-66H	3.3 kV	1200 A
SMPC MID CLs	195.9 A	Mitsubishi Electric CM400HG-66H	3.3 kV	400 A
SMPC DS	614.9 A	Mitsubishi Electric CM1200HC-66H	3.3 kV	1200 A

Table 4.7: Selected power devices for the analytical and simulation-based power loss comparison

The analytical expressions for losses derived above are implemented in Matlab and the results are presented in Figure (4.30) and Table (4.8) for the case when both converters are operating with rectifying active power and unity power factor. A switching frequency of 1 kHz is assumed for both converters. It can be observed that both converters have fairly similar overall losses with the SMPC losses being only 1.5% lower than those of the MMC. Conduction losses in the SMPC are 13.6% higher than in the MMC because of the additional losses in the DSs which are in the main current path. In fact, almost 39% of the conduction losses in the SMPC come from the DSs. It needs to noted here that for a practical HVDC system where hundreds of IGBTs will need to be stringed together to form each DS, ignoring the SM voltage ripple when applying the voltage derating factor to determine the ratings of the DSs, may result in a reduction in the conduction loss percentage in the DSs. On the other hand, the switching losses in the SMPC are 36% lower than in the MMC. This is because (a) the over-modulation operation in the SMPC results in a smaller main current than in the MMC and (b) the number of IGBTs switching the smaller main current (with an added balancing 2nd harmonic) in UPP/LOW CLs of the SMPC are 22% lower than in the MMC and the rest of the IGBTs in the MID CLs switch one-third of the smaller main current.

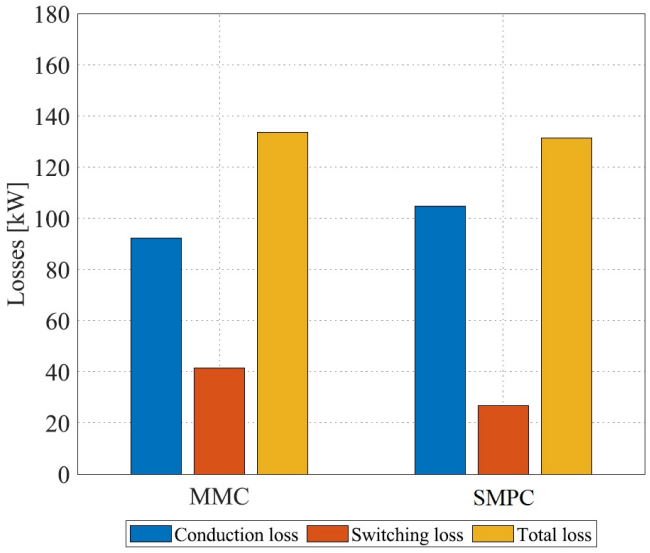


Figure 4.30: Analytical comparison of conduction, switching and total losses between MMC and SMPC at unity power factor

	Conduction loss(CLs)	Conduction Loss(DS)	Switching Loss	Total Loss	Loss percentage
MMC	92.2 kW	N/A	41.6 kW	133.8 kW	0.67 %
SMPC	64.1 kW	40.7 kW	26.7 kW	131.5 kW	0.66 %

Table 4.8: Analytical loss breakdown of MMC and SMPC at unity power factor

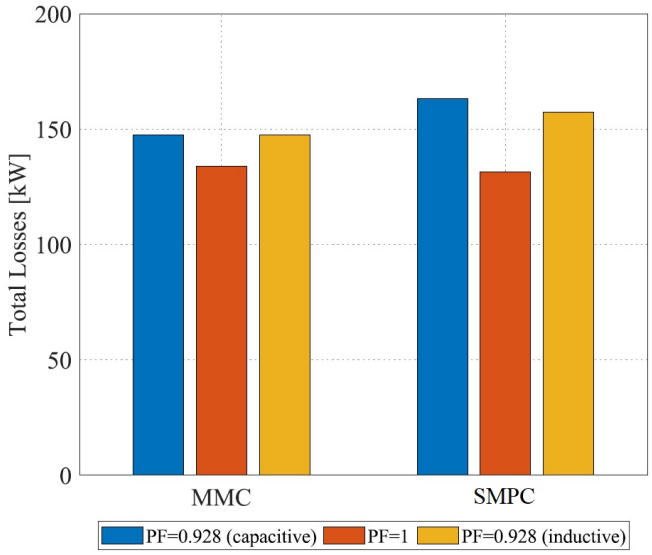


Figure 4.31: Analytical comparison of total losses between MMC and SMPC at different power factors

When rated Q is added, losses in the SMPC slightly exceed the losses in the MMC - 7.3% higher in case of −Q (capacitive) and 3.3% higher with +Q (inductive). This is depicted in Figure (4.31).

Because of the assumptions in the analytical loss computation above, it is subject to some percentage of error. For the purpose of verification, an additional PLECS® simulation model based approach is adopted for loss calculations. Although the switching transitions in PLECS are instantaneous to enable high-speed simulations, the software offers a parallel mechanism for semiconductor loss calculations. In this method, all the relevant device data such as switching energies and on-state voltage and current characteristics can be supplied in the form of look-up tables. The software uses linear interpolation to instantaneously calculate the losses based on the CL

current value [78] which are then averaged over a fundamental period.

To reduce control and modulation complexity, resulting CL currents from an averaged PLECS model for the converters (no switching involved) are sourced to a switching model of a single CL (HB for the MMC and HB, H-CL and DS for the SMPC) with a simple energy control loop that ensures that the capacitor voltages are balanced around the nominal value. The loss values for the single CL are then multiplied by the appropriate factors to obtain the conduction, switching and total converter losses. The results are reported in Table (4.9) for the case of unity power factor. It can be observed that the percentage difference between the total loss values of the two converters from the simulation is the same as in the analysis. However, the actual total loss values from the simulation are within a 5% error margin of the analytical values.

	Conduction loss(CLs)	**Conduction Loss(DS)**	**Switching Loss**	**Total Loss**	**Loss percentage**
MMC	95.7 kW	N/A	44.7 kW	140.4 kW	0.7 %
SMPC	64.5 kW	45.1 kW	27.4 kW	137 kW	0.69 %

Table 4.9: Simulation-based loss breakdown of the MMC and the SMPC at unity power factor

4.8 Fault considerations

The analysis presented thus far assumes that the AC and DC grid conditions are ideal. The study is extended to grid fault conditions in this section and the challenges that arise in the SMPC and the techniques incorporated to enable the converter to deal with them are discussed. However, a detailed investigation of all possible fault scenarios is out of scope for this thesis and the study is limited to AC voltage sag on one phase and a discussion on DC faults.

4.8.1 Unbalanced AC voltage sag

Due to short-circuits and other faults propagating in the electrical network to which an HVDC converter is connected, the AC voltage at the PCC may experience a sag [79][80]. Without implementing additional control, a sudden reduction in the AC voltage can lead to an increase in the current in an attempt to maintain the power transferred to the DC side, which can activate the trips and disconnect the converter from the grid [80]. This is undesirable since the Grid Code requires HVDC converters to stay connected to the grid during fault conditions [81]. In addition, a fault in one side of the system should not reflect on the other side. Hence, the fault currents arising on the AC side should not be transferred to the DC network [79].

The study presented in this thesis for the SMPC considers the case when an AC voltage sag occurs only in one phase. As the grid is unbalanced, the three-phase voltages and currents can be expressed by the sum of their positive, negative and zero sequence components. As is generally the case in VSC-HVDC systems, a Y-Δ transformer, with the Δ-connection on the converter side, is assumed between the SMPC converter and the grid which excludes the zero sequence components from the converter [82] [79]. During the fault, only the exchange of positive sequence current between the SMPC converter and the grid is considered and the negative sequence current is controlled to zero using the control strategy described in [83]. Further explanation of incorporation of this control method in the overall control strategy devised for the SMPC, and other assumptions related to a simulated case study of a single-phase AC voltage sag, are presented in Chapter 5. They are omitted here to narrow the focus to the particular challenge that the SMPC faces under unbalanced AC faults.

As explained in detail in Section (4.4), a balancing 2ω current is injected in the converter phase-legs to ensure zero steady-state average powers in the CLs of the SMPC. The size of the balancing 2ω current required in each phase-leg is a function

of the power of that converter phase-leg as can be deduced from Eq. (4.47). Thus, under normal operation when the per-phase-leg powers are equal, a symmetric set of 2ω currents is needed which cancel out on the DC side.

In case of unbalanced faults, when only positive sequence current is exchanged with the grid, the total power transferred from the AC to DC side is determined by the interaction of the positive sequence current and the positive sequence voltage. However, the individual per-phase-leg powers are not equal because the interaction of the positive sequence current with the negative sequence voltage results in different power contributions in each phase-leg. Although they sum up to zero and do not contribute to the total power transferred, they do result in an asymmetric set of balancing 2ω currents due to unequal per-phase-leg powers. The consequence is a 2ω ripple in the DC current, the size of which will be determined by the depth of the AC voltage sag.

Mathematically, the 2ω balancing currents under unbalanced fault conditions can be expressed as:

$$\begin{aligned} i_{2\omega}^{a} &= \frac{k_{2\omega}^{a}}{2\omega L_{arm}} \cos(2\omega t) \\ i_{2\omega}^{b} &= \frac{k_{2\omega}^{b}}{2\omega L_{arm}} \cos\left(2\omega t + \frac{2\pi}{3}\right) \\ i_{2\omega}^{c} &= \frac{k_{2\omega}^{c}}{2\omega L_{arm}} \cos\left(2\omega t - \frac{2\pi}{3}\right) \end{aligned} \tag{4.66}$$

where $k_{2\omega}^{a}$, $k_{2\omega}^{b}$ and $k_{2\omega}^{c}$ are the amplitudes of 2ω voltage required to circulate the desired 2ω current on the DC side and $k_{2\omega}^{a} \neq k_{2\omega}^{a} \neq k_{2\omega}^{c}$. Then, the ripple on the DC current can be written as:

$$I_{2\omega}^{DC} = i_{2\omega}^{a} + i_{2\omega}^{b} + i_{2\omega}^{c}$$

The resulting $I_{2\omega}^{DC}$ can be expressed as a phasor in the 2ω plane as shown in Figure (4.32) and hence, $I_{2\omega}^{DC} = |I_{2\omega}^{DC}| \angle \beta_{2\omega}$.

The method proposed in this thesis to remove the 2ω current ripple in the DC current

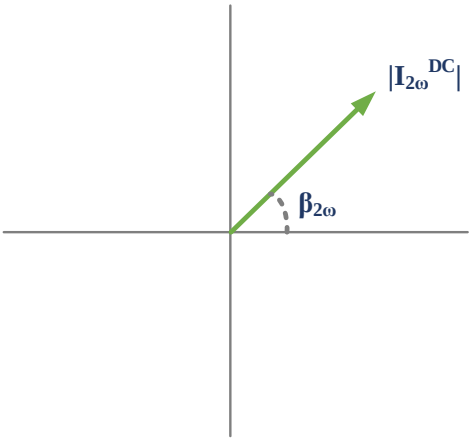


Figure 4.32: Phasor representation of the 2ω DC current ripple under unbalanced faults

(named 'quadrature compensation') is to inject additional 2ω currents in each phase that are in quadrature with the original balancing 2ω components given in Eq. (4.66). The quadrature currents are given in Eq. (4.67) and a balanced set is shown in the 2ω plane in Figure (4.33).

$$\begin{aligned} i_{2\omega}^{a^Q} &= \frac{k_{2\omega}^{a^Q}}{2\omega L_{arm}} \cos\left(2\omega t + \frac{\pi}{2}\right) \\ i_{2\omega}^{b^Q} &= \frac{k_{2\omega}^{b^Q}}{2\omega L_{arm}} \cos\left(2\omega t + \frac{2\pi}{3} + \frac{\pi}{2}\right) \\ i_{2\omega}^{c^Q} &= \frac{k_{2\omega}^{c^Q}}{2\omega L_{arm}} \cos\left(2\omega t - \frac{2\pi}{3} + \frac{\pi}{2}\right) \end{aligned} \tag{4.67}$$

Since $I_{2\omega}^{DC}$ is a known quantity (can be calculated in real-time), by a careful selection of the quadrature 2ω current amplitudes namely $k_{2\omega}^{a^Q}$, $k_{2\omega}^{b^Q}$ and $k_{2\omega}^{c^Q}$, the resultant $I_{2\omega}^{DC^Q}$ is generated such that it opposes $I_{2\omega}^{DC}$. The concept is illustrated in Figures (4.34a) and (4.34b). It must be noted that the quadrature currents do not affect the energy balance in the phase-legs.

In this thesis, quadrature compensation in AC unbalanced faults is implemented using open-loop calculations of the required quadrature components. These components may slightly increase the voltage ripple in the SM capacitors and hence, it is important to optimise their selection by decomposing the required $I_{2\omega}^{DC^Q}$ on the two

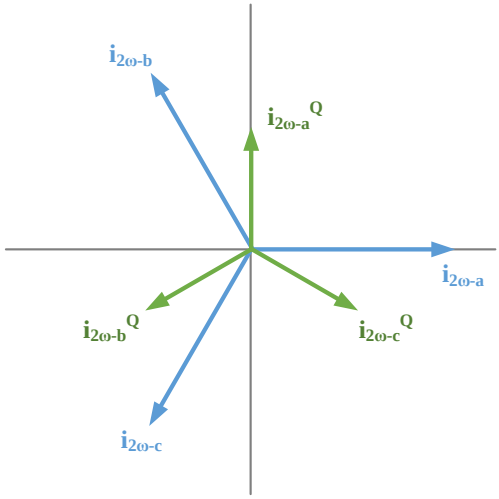


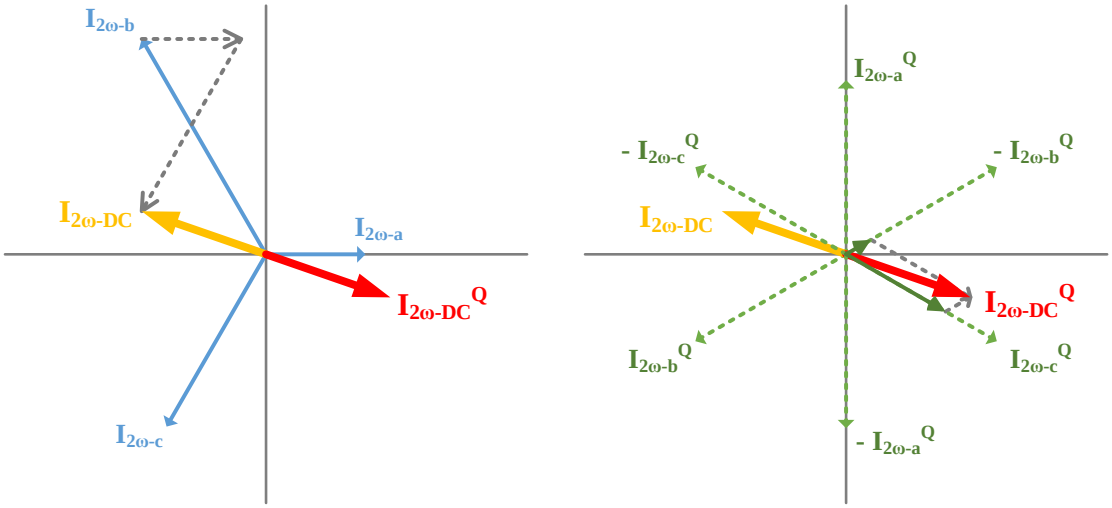
Figure 4.33: Balanced sets of $i_{2\omega}$ and $i_{2\omega}^{Q}$ currents

nearest neighbouring quadrature axes as depicted in Figure (4.34b). An algorithm is employed that identifies these axes and performs the decomposition using the simple method of sine rule.

4.8.2 Discussion on DC faults

Non-permanent DC faults in HVDC systems with overhead line transmission systems are a frequent occurrence caused by lightning strikes, pollution and broken tree branches [84] [85]. In multilevel converters, a short-circuit DC fault results in huge AC and DC fault currents capable of damaging the converter [86]. The protection schemes generally used to avoid the damage are AC or DC circuit breakers (CBs) that isolate the fault. AC CBs have a slow mechanical response time during which the devices still endure a high current stress [87]. Solid-state DC CBs have a fast response but the cost and semiconductor losses are significant in addition to the technology still being under development for high-power applications [88]. Furthermore, tripping of the CBs shuts down the system with no active/reactive power exchange and impacts the recovery time of the system after the fault is cleared [85].

Another approach to deal with DC faults is to utilize the inherent fault-ride through



(a) (b)

Figure 4.34: (a) Resultant $I_{2\omega}^{DC}$ under unbalanced AC faults and the required $I_{2\omega}^{DC^Q}$ (b) Required $I_{2\omega}^{DC^Q}$ decomposed on the nearest neighbouring quadrature axes

property of multilevel converters given that suitable SMs are used in the circuit. Hence, the MMC topologies with full-bridge SMs and clamp-double SMs and alternative topologies like the AAC are capable of handling DC faults [88]. This is because the SMs in these circuits can generate reverse voltages which allows control of the AC current during DC faults. The system can be kept in service continuously by exchanging reactive power with the grid which assists in recovering the normal operation after fault clearance [88] [85].

As explained in the previous sections, the focus in this thesis has been restricted to the optimisation of the SMPC for volume reduction and loss minimisation. For that reason, the DC fault handling capability of the converter is only conceptually discussed in this thesis and detailed simulation studies and experimental validation of DC fault scenarios are objectives for future work. For the discussion, the converter is considered to be capable of riding through the DC fault while compensating reactive

power and not just blocking the fault. This implies that at the instant when the fault is detected, instead of blocking all IGBTs, it is considered that the converter switches to fault-tolerant operation mode and retains active control of the AC current.

For DC fault-ride through (FRT) of a converter, the necessary condition is that the CLs are capable of generating bipolar voltages that becomes possible with the use of FB SMs. With enough FB SMs in the CLs, the converter is able to produce an output voltage large enough to counter the AC side voltage and regulate the current flow between the converter and the grid [89]. In previous sections, the proposed number of FB SMs in UPP/LOW CLs in the SMPC without fault considerations are not enough to enable the converter to ride through DC faults. Hence, this will now be revisited along with the waveshaping of the CLs.

In the DC FRT mode of the SMPC, the UPP/LOW CLs will be actively used for voltage synthesis whereas the HB SMs in the MID CL will be bypassed by turning on the lower switch in the HB configuration and the IGBTs in the DS configuration are blocked. The equivalent circuit is shown in Figure (4.35). Due to SMs by-passed in the MID CL, the CL outputs a zero voltage and a short-circuit across its terminals enables the UPP and LOW CLs to conduct simultaneously in parallel connection which doubles the reactive power compensation capacity. Moreover, it also ensures that the DC current during FRT is kept at zero. The UPP/LOW voltages in a generic phase x can be expressed as:

$$v^x_{upp} = -v_c$$

$$v^x_{low} = v_c$$

This implies that for successful DC FRT of the converter, the UPP/LOW CLs need to be rated for the peak converter AC voltage, $\hat{V_c}$, using all FB SMs. It should be noted that in the case that the SMPC is designed to ride through DC faults, since the UPP/LOW CLs are not composed of H-CLs, the original optimum modulation index value of $M_{opt} = 0.84M_{ss}$ can be chosen to obtain the lowest energy storage.

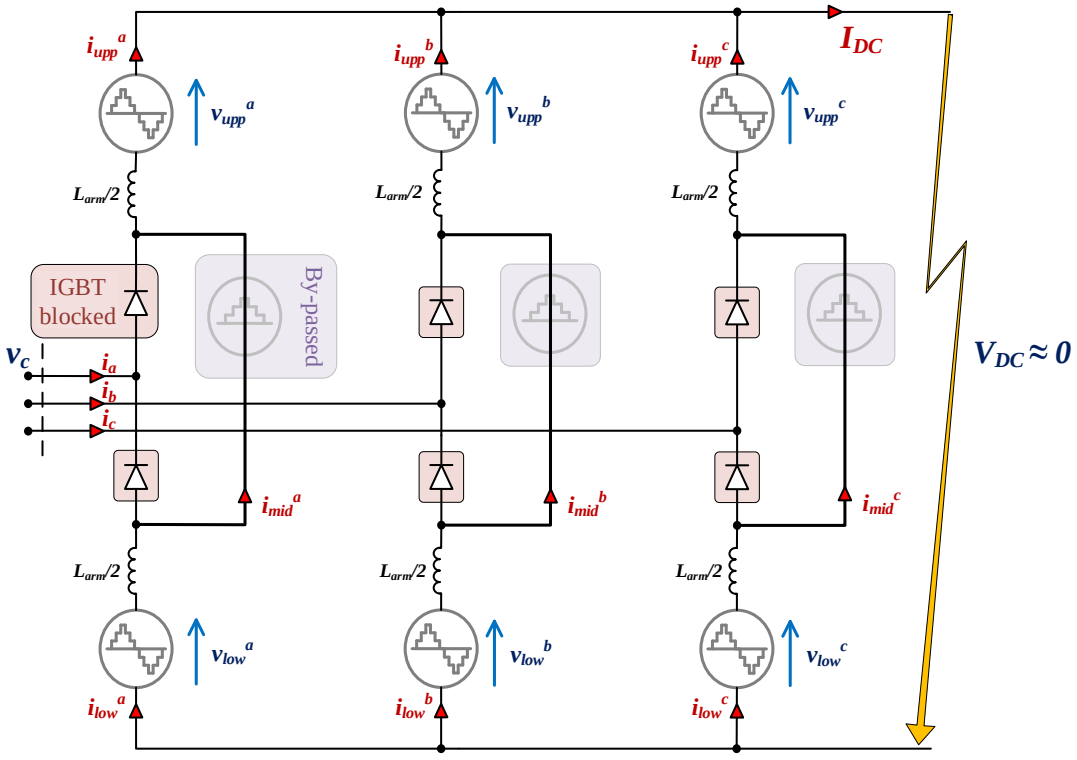


Figure 4.35: Equivalent circuit of SMPC in DC-fault ride through mode

For the DC-fault tolerant design scenario, the energy storage of the SMPC is fairly similar to the case without fault tolerance. However, because of the additional conducting devices resulting from the use of more FBs, the power losses are higher. Loss values from a switching model of the SMPC with DC FRT capability are presented in Table (4.10). Compared to a standard HB MMC, the losses for the SMPC with DC FRT are around 11% higher at unity power factor and roughly 27% - 28% higher at both inductive and capacitive power factors of 0.928. Thus, the benefit of DC FRT in the SMPC comes with a penalty on power loss that is more significant with the addition of rated Q. However, in comparison to the DC-fault tolerant FB-MMC that has 1.7-1.8 times higher power losses compared to a HB MMC, the SMPC with DC FRT offers the same functionality with around 25% - 30% lesser losses. Furthermore, a detailed power loss comparison with other multilevel topologies with DC fault handling capabilities e.g. Hybrid MMC [46], Hybrid Cascaded MMC [87] and AAC [55] is another interesting study that is considered a future scope of this work.

	Conduction loss(CLs)	Conduction Loss(DS)	Switching Loss	Total Loss	Loss percentage
PF = 1	90.3 kW	38.2 kW	26.9	155.4 kW	0.78 %
PF = 0.928 (inductive)	108.1 kW	41.8 kW	37.6 kW	187.5 kW	0.94 %
PF = 0.928 (capacitive)	104.7 kW	42.3 kW	40.8 kW	187.9 kW	0.94 %

Table 4.10: Simulation-based loss breakdown of the SMPC with DC FRT capability at different power factors

4.9 Summary

In this chapter, the operating principles and a complete theoretical analysis of a new hybrid multilevel VSC topology, titled the SMPC, is presented. Basic voltage waveshaping of the CLs is explained and the instantaneous voltages/currents/powers of the CLs are mathematically expressed using the Fourier series representation. It is shown that a 'sweet-spot' in terms of the AC and DC voltage levels exists for the converter where all its internal energies are balanced. Operating away from the 'sweet-spot' results in non-zero steady-state average powers of the CLs and hence, an active energy management strategy, based on second harmonic current injection, is proposed for the correct operation of the converter.

With the use of an active energy management strategy, the constraint imposed by the 'sweet-spot' modulation index is lifted. Since the SMPC can operate in over-modulation due to the presence of FBs in its CLs and, in addition, since there are no constraints on the choice of the modulation index within a certain range, a method for optimising the modulation index is proposed that minimises the energy storage of the converter. The optimum modulation index value is found to be 84% of the 'sweet-spot' modulation index. However, since the use of H-CLs in UPP/LOW CLs is proposed (instead of all FBs) to keep the losses low, the optimum modulation index

is adjusted to 75% of the 'sweet-spot' modulation index to ensure that the energies of both the HBs and the FBs in the H-CLs are balanced.

A detailed comparative analysis of the SMPC against the MMC is conducted for a fixed set of system ratings. It is shown that the SMPC has 10% less SMs per phase and considerably smaller capacitor sizes (29% smaller in UPP/LOW CLs and 78% smaller in MID CLs). Overall, the energy storage of the SMPC is half of that of the MMC. Thus, an SMPC converter can be expected to have a smaller volume than an MMC converter. The downside is that the number of IGBTs required is 54% higher, although it is shown that as a result of the MID CLs being out of the main current path, the actual semiconductor requirement is only 21-22 % higher. A detailed comparative loss analysis is also presented, further validated by switching loss models of both converters. Overall, the losses for both converters are comparable, with losses in SMPC being slightly higher (3% - 7%) with the addition of rated reactive power.

Performance of the SMPC in AC and DC fault conditions is also analysed. In case of unbalanced AC faults, a second harmonic ripple in the DC current appears. To remove the ripple, a method based on injection of quadrature second harmonic currents in the phase-legs is proposed. For DC faults, it is remarked that because of the presence of FBs in the UPP/LOW CLs, the converter is capable of providing DC fault-ride through given that the CLs are appropriately rated. However, the benefit of DC FRT comes with a small penalty on the power losses.

Chapter 5

Control strategy development and simulation studies

5.1 Introduction

In HVDC systems, a modular multilevel VSC converter acts as an energy interface between the AC system and the DC network using cell capacitors as energy storage elements [38]. Hence, the control objectives in these converters involve the control of voltages and currents at the converter terminals, control of the internal energies of the converter and their correct distribution amongst the converter phases and arms, and control of the internal circulating currents.

The control architecture depends on the application of the converter and the desired objectives [90]. Generally, converter stations at both ends of a VSC-HVDC link are controlled in a coordinated manner and it is crucial to ensure that power flow at the sending end (rectifier) matches that at the receiving end (inverter) minus the losses in the DC cable. To achieve this, in a point-to-point HVDC connection, one station is responsible for controlling the DC link voltage while the other controls the power flow. In addition, on their respective AC sides, both converter stations can control their reactive powers independently, either using direct orders or indirectly by controlling the AC voltages [91]. In the case of interconnection of two AC systems,

the DC voltage control and the power control functions are interchangeable between converters. In other specific applications where the power flow is mostly unidirectional, the converter stations usually have set control functions. For instance, when connecting offshore wind farms to an AC grid, the rectifier side generally controls the power flow and coordinates the AC voltage and frequency control with the generators and the inverter side is normally controlled to regulate the DC voltage. In another application scenario of supplying power to an islanded AC load, the inverter typically controls the frequency and the AC voltage of the load while the rectifier connected to the main grid controls the DC voltage [92].

In this thesis, a general control scheme for the SMPC is developed for the inverter side converter in the application scenario of a point-to-point HVDC connection between two AC systems. Hence, it is assumed that the DC network voltage is controlled by the other station and a stiff DC voltage is assumed. The control scheme is then designed to regulate the active power flow between the AC and the DC networks and the reactive power exchange between the converter and the AC grid, tracking both to set references. Other control scenarios are also possible with the scheme proposed. This flexibility is exploited later in the experimental investigations.

In this chapter, the basic principles of active and reactive power control on the AC side are first explained which form the basis of the AC current control. After that, the design of the control scheme for the SMPC is presented, starting with the overall control structure and then moving on to the detailed design of each control loop. Next, the simulation model developed to simulate the SMPC converter is introduced. Finally, simulation results for ideal AC grid conditions and for the unbalanced AC voltage sag case are presented to validate the control concepts developed.

5.2 Principle of Active and Reactive Power Control

VSCs are capable of controlling the active and reactive powers independently at their connection to the grid. To understand the basic principle of power transfer, a simplified circuit of a single-phase VSC connected to a single-phase grid through a lossless inductive line is shown in Figure (5.1). The VSC is considered as a controllable voltage source capable of generating an AC voltage with the desired magnitude and phase angle relative to the grid voltage.

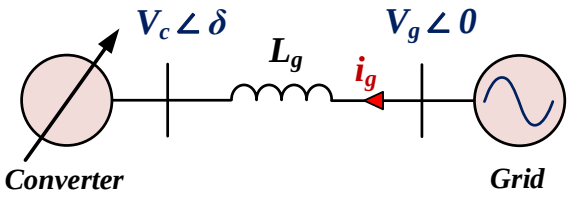


Figure 5.1: VSC modelled a controllable voltage source connected to the grid

The active and reactive powers exchanged between the converter and the grid can be expressed as [92]:

$$P_g = \frac{V_c \cdot V_g}{X_g} \sin \delta \tag{5.1}$$

$$Q_g = \frac{V_g^2}{X_g} - \frac{V_g \cdot V_c}{X_g} \cos \delta \tag{5.2}$$

where X_g is the reactance of the inductor L_g.

It can be concluded from Eq. (5.1) that the active power can be regulated by controlling the voltage angle δ between V_c and V_g. A change in sign of δ results in power flow reversal. If V_c lags V_g, the converter absorbs active power from the grid and operates as a rectifier. Conversely, if V_c leads V_g, the converter injects active power into the grid and operates as an inverter. From Eq. (5.2), it can be deduced that when V_c is lower than V_g, the converter absorbs reactive power from the grid and

operates in inductive mode. On the other hand, when V_c is greater than V_g, the converter supplies reactive power to the grid and operates in capacitive mode.

Therefore, a VSC has the ability to provide four-quadrant P-Q operation as shown in Figure (5.2). This is achieved by controlling the magnitude and the phase of the fundamental frequency AC voltage component generated at the output of the converter. In practice, this control is implemented in a closed loop in which the desired P-Q operating point is achieved by tracking the resulting current reference. The output of the control loop is the fundamental frequency component of the converter voltage with the correct magnitude and phase shift to enable the required power flow.

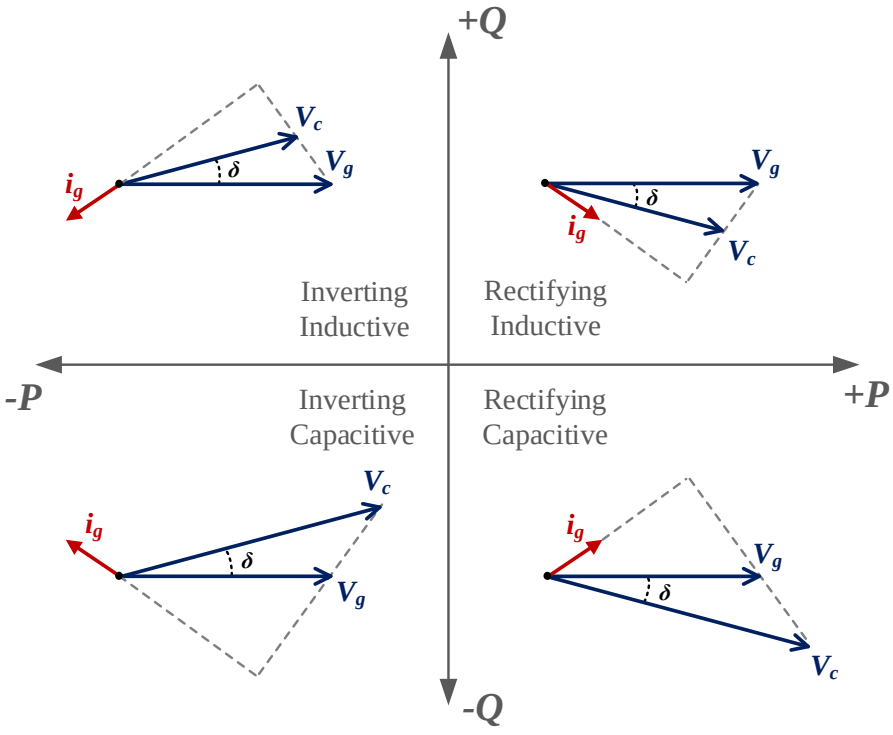


Figure 5.2: Four-quadrant P-Q operation of a VSC

5.3 Control Scheme

The converter arrangement considered for designing the control scheme is depicted in Figure (5.3). In the application considered, the AC power demand is imposed. Set references for the active and reactive power exchange between the converter and the AC grid are provided which dictate the AC current reference signal. Since the DC voltage is assumed to be stiff, the DC current also needs to be controlled in order to push the power to the DC network. The converter acts as an energy interface between the AC and DC sides and therefore, it is important to maintain the average total internal energy of the converter at a constant value. This can be achieved by ensuring overall power balance i.e. the AC and DC powers are equal if the converter losses are ignored. Since the AC power demand is imposed, the overall energy stored in the converter is maintained through regulation of the DC power by acting on the DC current.

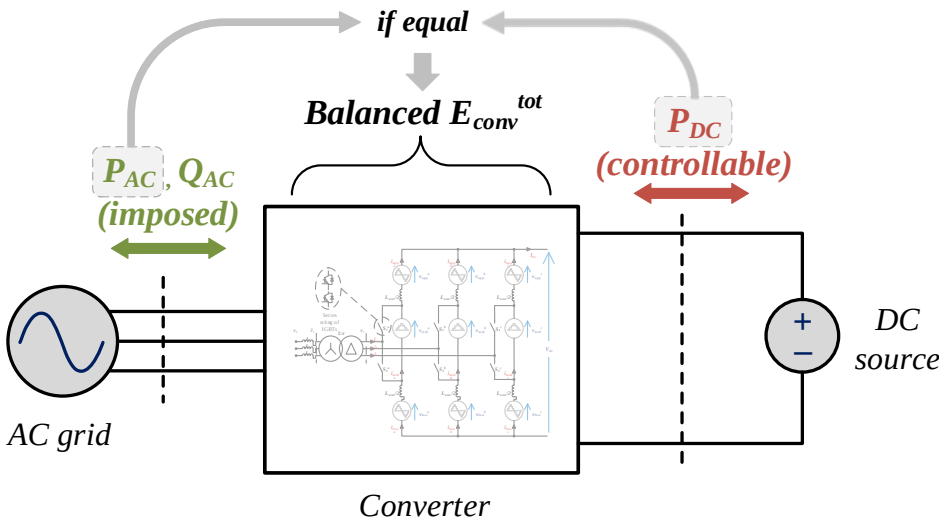


Figure 5.3: Converter arrangement considered for control scheme design

A block diagram of the overall control scheme for the SMPC converter, which is decoupled on the AC and DC sides, is presented in Figure (5.4). On the AC side,

the *abc* three-phase coordinate system is transformed into α-β coordinates to implement the control. On the DC side, a per-phase-leg control is implemented i.e. the total energy of each phase leg is regulated separately by generating the required DC current contribution independently to maintain power balance in that particular leg. Moreover, the energy stored in each phase leg should also be correctly distributed amongst the arms/CLs of the respective leg. This is achieved by injecting harmonic components in the circulating current on the DC side. As discussed in Section (4.4) and explained further later in this chapter, the harmonic components injected are the second harmonic that transfers energy between UPP/LOW CLs and MID CLs, plus a fundamental component that transfers energy between UPP and LOW CLs. The presented control automatically regulates the magnitudes of both the oscillatory components of the circulating current, which is needed as the energy imbalances amongst the three CLs in a phase leg vary with the operating point. The output of the circulating current control is the "DC part" of the modulation reference which, along with the AC reference signal, is the input to the wave-shaping block. This block generates the final modulation references for the UPP, MID and LOW CLs by implementing the chosen wave-shaping discussed in Section (4.3).

As highlighted in Figure (5.4), the main control loops are the AC current control, energy control and the circulating current control. The design of these individual control loops is now discussed at length in the following subsections.

5.3.1 AC current control

As mentioned before, the active and reactive power exchange between the converter and the AC system can be controlled by acting on the AC current.

AC side current control can be implemented in a number of ways that have been widely discussed in literature. In this work, AC current control is implemented in the α-β stationary reference frame, and proportional-resonant (PR) controllers are

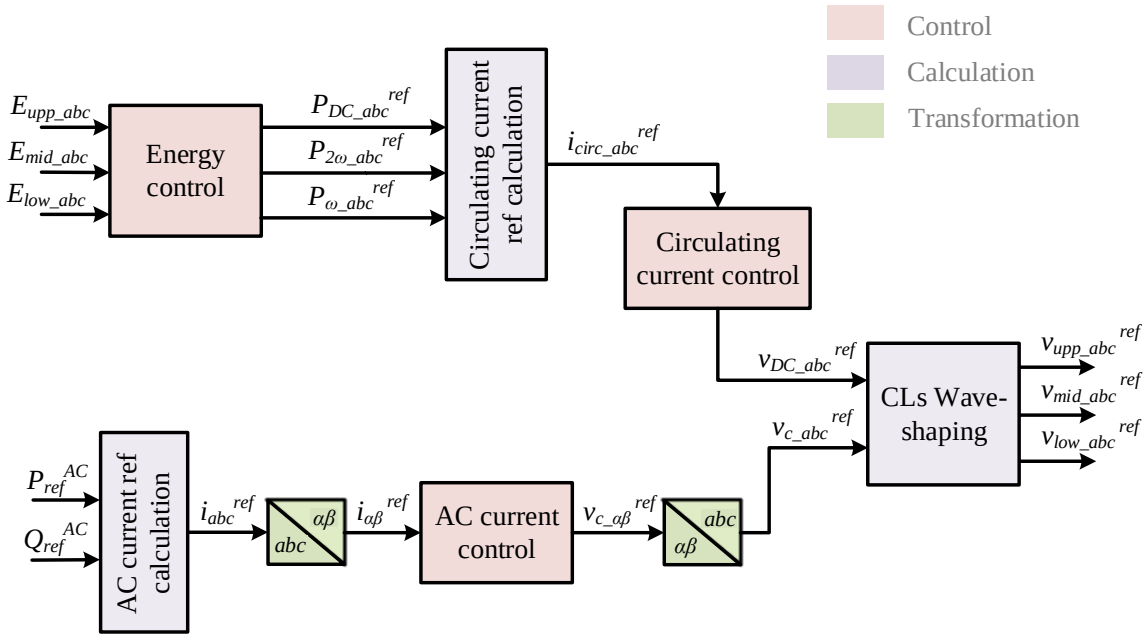


Figure 5.4: Overall per-phase-leg control scheme of the SMPC

used for tracking the reference with minimum steady state error.

A block diagram of the AC current control loop is shown in Figure (5.5). The PR controller structure used is based on [93] and given in Eq. (5.3) where ω_s is the AC frequency which is tracked by the controller with negligible steady-state error as the gain at ω_s is very high, and ω_c is the controller bandwidth. This structure is chosen because of its tuning simplicity as the control gains can be calculated solely based on the desired controller bandwidth and plant parameters.

$$C_{i_{AC}}(s) = \frac{(L_s s + R_s)(2\omega_c s + \omega_c^2)}{s^2 + \omega_s^2} \tag{5.3}$$

The AC current references for the individual phases are calculated from the P and Q set-points as shown in Figure (5.6) where $\hat{V}_s$ is the grid voltage amplitude and θ_{abc} are the angular positions of the grid phases measured using the single-phase PLL structure depicted in Figure (5.7) [4]. The first part of the PLL is the Phase Detector (PD) in which the Quadrature Signal Generator (QSG) first generates a $\frac{\pi}{2}$ rads time-shifted signal from the single-phase input and the two orthogonal components are

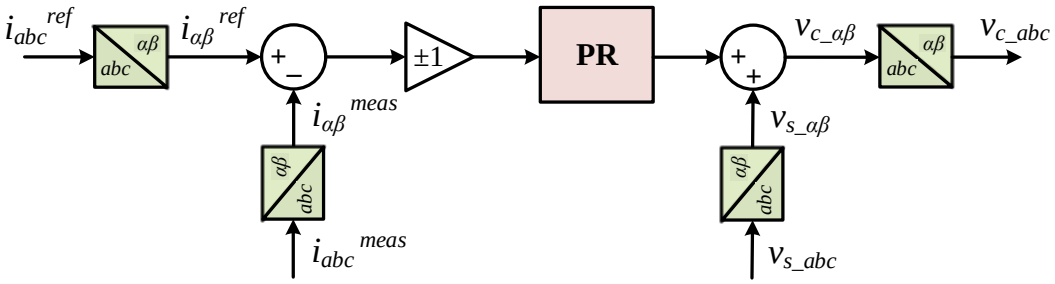


Figure 5.5: AC current control block diagram

converted into *d-q* quantities using Park transform. The second part is the Loop Filter (LF), realised by a PI controller, that attenuates high-frequency AC components from the PD output. The third part is the Frequency/Phase-angle Generator (FPG) in which the output of the LF is supplied with the target angular frequency as a feed-forward term followed by an integrator to acquire the angle. The QSG in the PD is a first-order all-pass filter based on [94] with the transfer function given in Eq. (5.4) which provides unit gain for all frequencies and shifts the input signal by 90 degrees at ω_s, the frequency of the AC system.

$$QSG = \frac{s - \omega_s}{s + \omega_s} \tag{5.4}$$

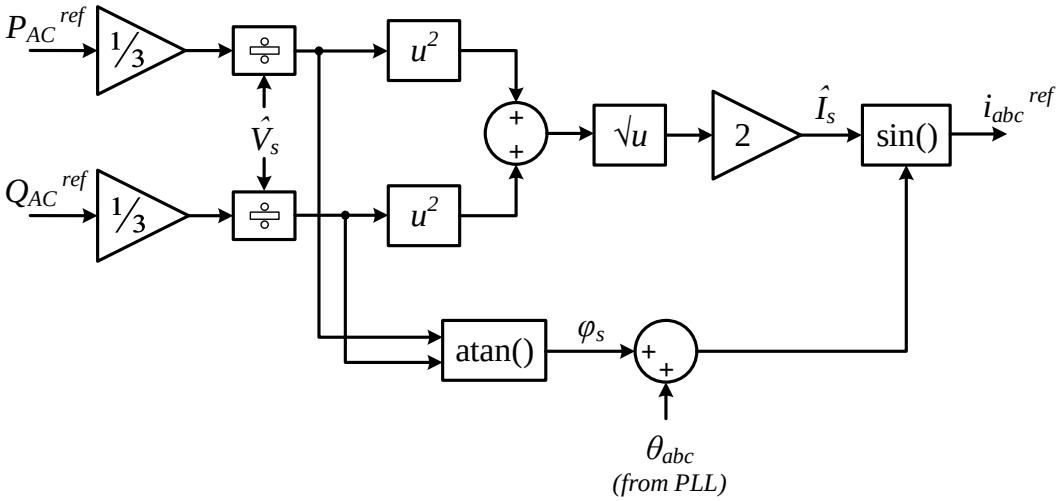


Figure 5.6: AC current reference calculation

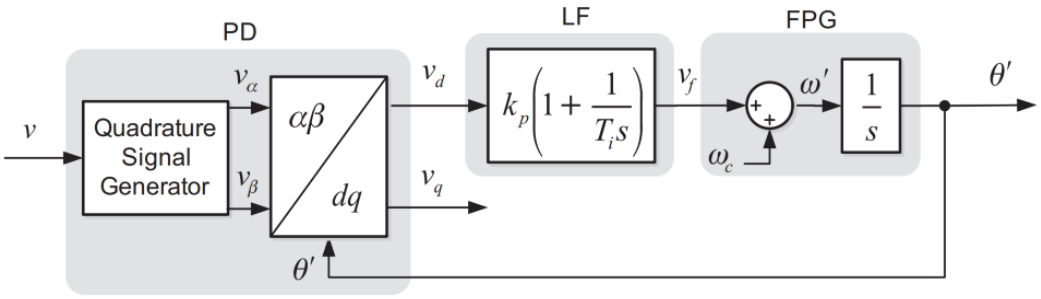


Figure 5.7: Single-phase PLL structure [4]

5.3.2 Energy Control

The objective of the energy control is to ensure that the total energy stored in the converter phase-legs is regulated at a set value. In addition, this energy should be shared between the CLs in such a manner that the individual CL energies are also maintained at their desired reference values. The energy control of the SMPC is subdivided into three parallel control loops, each of which contribute to the circulating current reference on the DC side. These control loops are the Total Energy Control, Inter-Arm Energy Control and Inter-Chainlink Energy Control and are discussed in detail in this section.

5.3.2.1 Total Energy Control

The Total Energy Control (TEC) is in charge of maintaining the per-phase average total energy at the reference value E_{TOT}^{ref}. E_{TOT}^{ref} corresponds to a desired nominal SM voltage of the capacitors. By regulating the total energy stored in the capacitors, the balance between the net DC power (P_{DC}) and the AC active power (P_{AC}) is ensured. In the application under study, P_{AC} is imposed and cannot be used a control variable. Hence, P_{DC} is the variable available to regulate the total energy.

For a generalised CL shown in Figure (5.8) with N number of SMs, the equivalent

stored energy of the CL can be written as:

$$E_{CL} = \frac{1}{2}\frac{C_{SM}}{N_{SM}}\left(\sum_{n=1}^{N_{SM}} v_{SM}^{n}\right)^{2} \tag{5.5}$$

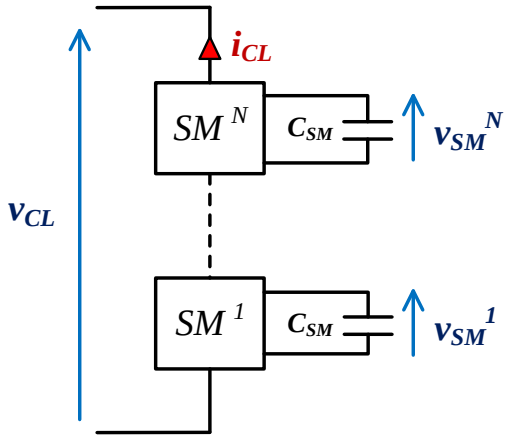


Figure 5.8: General schematic of a CL

Eq. (5.5) shows that the equivalent stored energy of a CL is proportional to the square of the sum-capacitor-voltage, which is measurable. E_{CL} generally has a mean value and an AC ripple. Since the control objective is to control the average value of CL energy, the AC ripple is generally removed using filters before feeding into the controllers.

The SMPC is composed of three CLs in a single phase-leg and the number of SMs and the capacitor sizes are different between MID CLs and UPP/LOW CLs. Hence, the total stored energy in any one arbitrary phase-leg can be expressed as:

$$E_{TOT}^{x} = \frac{1}{2}\left[\frac{C_{SM}^{upp}}{N_{SM}^{upp}}\left(\sum_{n=1}^{N_{SM}^{upp}} v_{SM}^{n}\right)^{2} + \frac{C_{SM}^{mid}}{N_{SM}^{mid}}\left(\sum_{n=1}^{N_{SM}^{mid}} v_{SM}^{n}\right)^{2} + \frac{C_{SM}^{low}}{N_{SM}^{low}}\left(\sum_{n=1}^{N_{SM}^{low}} v_{SM}^{n}\right)^{2}\right]$$

in which the sum-capacitor-voltages are measured quantities and N_{SM} and C_{SM} are fixed for all three CLs.

A block diagram of the TEC is presented in Figure (5.9). The error between the actual stored energy and the reference value includes the AC ripple which is removed

using a Moving Average Filter (MAF) with an averaging window at 50 Hz. The per-phase AC power is added as a feed-forward term to the output of the PI controller to improve the transient behaviour. Finally, the output of the controller is divided by V_{DC} to obtain the DC current reference of that particular phase leg. The plant gain is thus $\frac{1}{V_{DC}}$ and the plant used to design the PI controller is:

$$G_{TEC}(s) = \frac{1}{s}$$

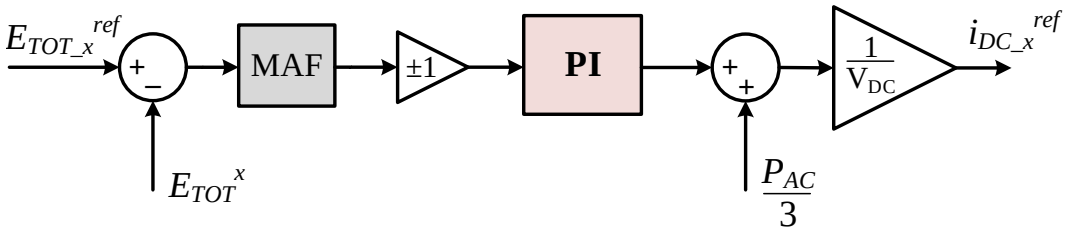


Figure 5.9: TEC block diagram

5.3.2.2 Inter-Arm Energy Control

The Inter-Arm Energy Controller (IAEC) is responsible for managing the energy transfer between MID CL and UPP/LOW CLs in each converter phase-leg. The design of the IAEC assumes that the converter is operating with global energy balance. Hence the TEC must be faster than the IAEC. As discussed in detail in Section (4.4), the average powers in the CLs are naturally non-zero in steady state even if the global power balance exists. Subsequently, in the same section, it has been explained that injecting a circulating second harmonic current through the DC side provides the means for exchanging power between the MID CL and the UPP/LOW CLs.

As mentioned above, a faster TEC loop ensures global power balance and hence, makes valid the energy management analysis of Section (4.4). Remembering from the analysis that the average powers of UPP and LOW CLs combined are equal and opposite to the average power in the MID CL, the IAEC can be designed to regulate the energy difference between UPP/LOW CLs and MID CLs to a constant reference,

E^{ref}_{DIFF}. It should be noted that E^{ref}_{DIFF} is generally different from zero since the number of SMs in the UPP/LOW and MID CLs are usually different. Recalling Eqs. (4.44)-(4.46), the final average power expressions of the CLs including the power contributions due to the circulating second harmonic current ($i^x_{2\omega}$) in an arbitrary phase x are:

$$\bar{P}^{FIN}_{upp_x} = -\frac{1}{2}\hat{V}_c\hat{I}\cos\phi\left(\frac{r\hat{V}_c}{\pi V_{dc}} - \frac{1}{4}\right) + \frac{rk_{2\omega}\hat{V}_c}{6\pi\omega L_{arm}}$$

$$\bar{P}^{FIN}_{mid_x} = \hat{V}_c\hat{I}\cos\phi\left(\frac{r\hat{V}_c}{\pi V_{dc}} - \frac{1}{4}\right) - \frac{rk_{2\omega}\hat{V}_c}{3\pi\omega L_{arm}}$$

$$\bar{P}^{FIN}_{low_x} = -\frac{1}{2}\hat{V}_c\hat{I}\cos\phi\left(\frac{r\hat{V}_c}{\pi V_{dc}} - \frac{1}{4}\right) + \frac{rk_{2\omega}\hat{V}_c}{6\pi\omega L_{arm}}$$

Thus, it can be said that the total average power 'exchanged' between the MID CL and UPP/LOW CLs during the energy management action is:

$$\bar{P}^x_{2\omega} = \frac{rk_{2\omega}\hat{V}_c}{3\pi\omega L_{arm}} \tag{5.6}$$

Let us define $\bar{P}^x_{orig}$ as:

$$\bar{P}^x_{orig} = -\hat{V}_c\hat{I}\cos\phi\left(\frac{r\hat{V}_c}{\pi V_{dc}} - \frac{1}{4}\right)$$

The final CL average power expressions can then be written as:

$$\bar{P}^{FIN}_{upp_x} = \frac{\bar{P}^x_{orig}}{2} + \frac{\bar{P}^x_{2\omega}}{2}$$

$$\bar{P}^{FIN}_{mid_x} = -\bar{P}^x_{orig} - \bar{P}^x_{2\omega}$$

$$\bar{P}^{FIN}_{low_x} = \frac{\bar{P}^x_{orig}}{2} + \frac{\bar{P}^x_{2\omega}}{2}$$

The stored energy in the individual CLs can be expressed as follows:

$$E^x_{UPP} = \frac{1}{2}\frac{C^{upp}_{SM}}{N^{upp}_{SM}}\left(\sum_{n=1}^{N^{upp}_{SM}} v^n_{SM}\right)^2$$

$$E^x_{MID} = \frac{1}{2}\frac{C^{mid}_{SM}}{N^{mid}_{SM}}\left(\sum_{n=1}^{N^{mid}_{SM}} v^n_{SM}\right)^2$$

$$E^x_{LOW} = \frac{1}{2}\frac{C^{low}_{SM}}{N^{low}_{SM}}\left(\sum_{n=1}^{N^{low}_{SM}} v^n_{SM}\right)^2$$

The actual differential energy E^x_{DIFF}, that is the difference between the UPP/LOW CL and MID CL energies, can then be written as:

$$E^x_{DIFF} = (E^x_{UPP} + E^x_{LOW}) - E^x_{MID}$$

Alternatively, in terms of the average CL powers, E^x_{DIFF} is defined as:

$$\begin{aligned} E^x_{DIFF} &= \frac{1}{s}\left[\left(\bar{P}^{FIN}_{upp_x} + \bar{P}^{FIN}_{low_x}\right) - \bar{P}^{FIN}_{mid_x}\right] \\ &= \frac{1}{s}\left[\frac{\bar{P}^x_{orig}}{2} + \frac{\bar{P}^x_{2\omega}}{2} + \frac{\bar{P}^x_{orig}}{2} + \frac{\bar{P}^x_{2\omega}}{2} + \bar{P}^x_{orig} + \bar{P}^x_{2\omega}\right] \\ &= \frac{2}{s}\left[\bar{P}^x_{2\omega} + \bar{P}^x_{orig}\right] \end{aligned}$$

Based on the derivation above, the basic control structure of the IAEC loop is shown in Figure (5.10). $\bar{P}^x_{2\omega}$ is the output of the IAEC controller and $\bar{P}^x_{orig}$ can be considered as an external perturbation that is linked to the AC active power reference. The plant used to design the PI controllers in the IAEC is:

$$G_{IAEC}(s) = \frac{2}{s}$$

A block diagram of the IAEC is depicted in Figure (5.11). The error is passed through an MAF to remove the AC ripple. The output of the PI controller is the total second harmonic power exchanged, $\bar{P}^x_{2\omega}$. To drive the circulating current that results in this

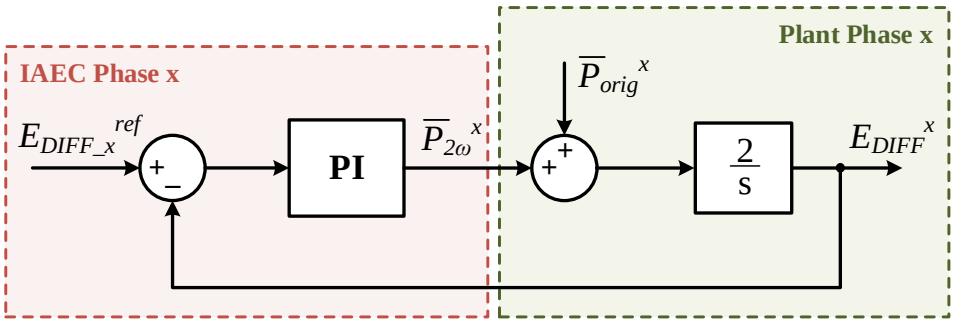


Figure 5.10: Basic structure of the IAEC

power exchange, the desired second harmonic required is then computed. Hence, using Eq. (5.6), the plant gain is:

$$\frac{k_{2\omega}^{a}}{\bar{P}_{2\omega}^{a}} = \frac{3\pi\omega L_{arm}}{r\hat{V}_c}$$

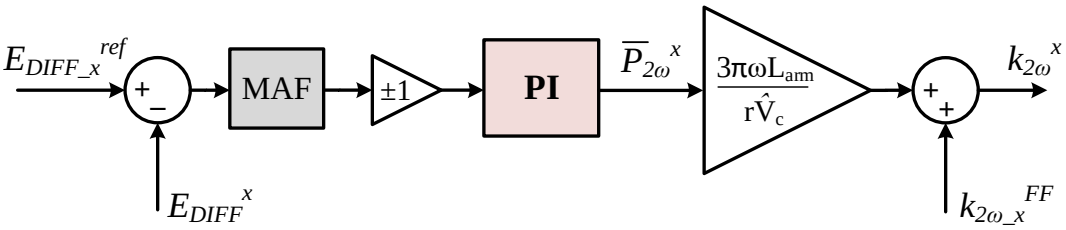


Figure 5.11: IAEC block diagram

It can be noticed that the plant gain of the IAEC includes the peak AC converter voltage $\hat{V}_c$, which is a function of the P-Q operating point. However, the non-linearity caused by $\hat{V}_c$ is considered mild, as the variations for a given P-Q range are small. Hence, it is reasonable to replace $\hat{V}_c$ by the AC grid peak voltage.

The output of the IAEC is the required amplitude of the second harmonic voltage. A feed-forward term, i.e. the estimated second harmonic voltage amplitude for the given operating conditions, is also added to the output to compensate for the external perturbation $\bar{P}_{orig}^{x}$ shown in Figure (5.10) resulting in faster error correction. The feed-forward calculation is based on Eq. (4.47) and is given in terms of the operational

set-points ($P^{ref}_{AC_x}$ & $\hat{V}_c$) as:

$$k^{FF}_{2\omega_x} = 6\omega L_{arm} P^{ref}_{AC_x} \left(\frac{1}{V_{DC}} - \frac{\pi}{4r\hat{V}_c} \right)$$

5.3.2.3 Inter-Chainlink Energy Control

The IAEC ensures that the energy difference between the UPP/LOW and MID CLs is maintained at a desired constant value. However, due to parameter differences and power loss differences due to different device characteristics between CLs, the individual energies of the UPP and LOW CLs will naturally drift away from the reference value in the absence of any control. Hence, the Inter-Chainlink Energy Control (ICEC) is added to regulate the individual UPP and LOW CL energies at their desired set-points.

The ICEC can be designed to remove any difference between the UPP and LOW CL energies i.e. ($E^a_{UPP} - E^a_{LOW}$) should be zero. Recalling Eqs. (4.15) and (4.17) from Section (4.3), the instantaneous CL voltages in phase a are:

$$v^a_{upp} = \frac{V_{dc}}{2} - r\hat{V}_c \left[\frac{1}{\pi} + \frac{1}{2}\sin(\omega t) - \frac{2}{\pi} \sum_{n=2,4,6..}^{\infty} \frac{1}{n^2-1} \cos(n\omega t) \right]$$

$$v^a_{mid} = r\hat{V}_c \left[\frac{2}{\pi} - \frac{4}{\pi} \sum_{n=2,4,6..}^{\infty} \frac{1}{n^2-1} \cos(n\omega t) \right]$$

$$v^a_{low} = \frac{V_{dc}}{2} - r\hat{V}_c \left[\frac{1}{\pi} - \frac{1}{2}\sin(\omega t) - \frac{2}{\pi} \sum_{n=2,4,6..}^{\infty} \frac{1}{n^2-1} \cos(n\omega t) \right]$$

It can be observed that the fundamental frequency components in the UPP and LOW voltages have the following relation:

$$v^a_{upp_\omega} = -v^a_{low_\omega}$$

Hence, the addition of a fundamental frequency current component (i^a_ω) in the circulating current can achieve the effect of transferring energy between UPP and LOW CLs until both CL average powers are driven to zero. It is worth mentioning that i^a_ω will not dissipate any average power in the MID CL as there are no fundamental frequency voltage components there and will have no effect on the energy balance in the MID CL. i^a_ω has to be in phase with $v^a_{upp_\omega}/v^a_{low_\omega}$ and hence can be defined as:

$$i^a_\omega = m_{\omega 0}\sin(\omega t)$$

The fundamental frequency voltage component (v^a_ω) that needs to be added in both UPP and LOW CLs to drive i^a_ω on the DC side can be expressed as:

$$\begin{aligned} 2v^a_\omega &= L_{arm}\frac{d}{dt}i^a_\omega \\ v^a_\omega &= \frac{m_\omega}{2}\cos(\omega t) \end{aligned}$$

where $m_\omega = \omega L_{arm} m_{\omega 0}$.

The average power 'exchanged' between the UPP CL and the LOW CL to ensure zero net average energy difference between the two CLs is given in Eq. (5.7). The subscript 'x' has been used instead of 'a' to represent an arbitrary phase.

$$\bar{P}^x_\omega = \frac{r m_\omega \hat{V}_c}{4\omega L_{arm}} \tag{5.7}$$

A term 'correction energy E^x_{CORR}' is defined as the difference between the UPP and LOW CL energies which can be written as:

$$E^x_{CORR} = E^x_{UPP} - E^x_{LOW}$$

In terms of the average CL powers, E^x_{CORR} is defined below. The definitions of $\bar{P}^{FIN}_{upp_x}$ and $\bar{P}^{FIN}_{low_x}$ follow from Section (5.3.2.2).

$$\begin{aligned} E^x_{CORR} &= \frac{1}{s}\left[\left(\bar{P}^{FIN}_{upp_x} + \bar{P}^x_\omega\right) - \left(\bar{P}^{FIN}_{low_x} - \bar{P}^x_\omega\right)\right] \\ &= \frac{2}{s}\left[\bar{P}^x_\omega\right] \end{aligned}$$

Thus, the plant used to design the PI controllers in the ICEC is:

$$G_{ICEC}(s) = \frac{2}{s}$$

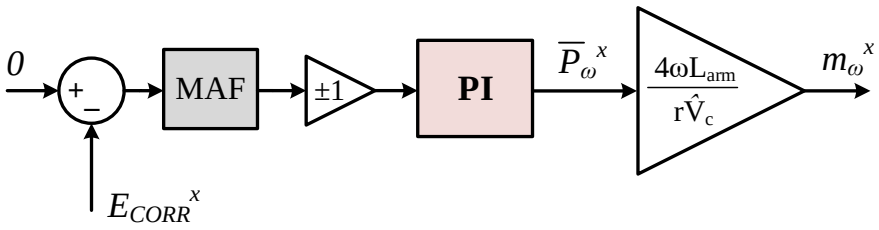


Figure 5.12: ICEC block diagram

A block diagram of the ICEC is shown in Figure (5.12). Similar to the previous energy loops, the AC ripple is eliminated using an MAF. The output of the PI controller is $\bar{P}_\omega^x$. To generate the fundamental frequency circulating current component that results in a power exchange of $\bar{P}_\omega^x$ between UPP and LOW CL, the amplitude of the required v_ω^x is then computed from $\bar{P}_\omega^x$. Hence, using Eq. (5.7), the plant gain is:

$$\frac{m_\omega^x}{\bar{P}_\omega^x} = \frac{4\omega L_{arm}}{r\hat{V}_c}$$

5.3.3 Circulating Current Control

In the SMPC, active control of the circulating current is essential since it serves as a carrier of energy between the CLs of a phase-leg. The circulating current in each phase leg 'x' is composed of the following components:

- *DC component (i_{DC}^x):* Enables power flow on the DC side and maintains total stored energy in each phase
- *Fundamental frequency AC component (i_ω^x):* Manages the correction energy between UPP and LOW CLs
- *Second harmonic AC component ($i_{2\omega}^x$):* Regulates the differential energy between UPP/LOW CLs and MID CL

The i^x_{DC} components in the circulating currents of each phase leg add up to form the DC network current whereas the i^x_{ω} and $i^x_{2\omega}$ components sum up to zero on the DC network in a balanced three-phase system. i^x_{ω} corrects any energy imbalances between UPP and LOW CLs arising from parameter/power-loss differences. Thus, in steady state, i^x_{ω} in each phase leg is a small current which does not significantly contribute to the current wave-shapes of the CLs. Contrarily, $i^x_{2\omega}$ continually transfers energy between MID CL and UPP/LOW CLs to maintain the equilibrium position of zero steady-state average power in the CLs (as discussed in detail in Section (4.4)), and hence, $i^x_{2\omega}$ usually has a sizeable magnitude in steady state. Its effect on the CL current wave-shapes depends on the operating point and becomes significant when operating away from the 'sweet-spot' (refer to Section (4.4) for the definition of 'sweet-spot').

In the case of parameter/power-loss differences between the three phase legs of the converter, both i^x_{ω} and $i^x_{2\omega}$ may not cancel out to zero on the DC side, leaving a small ripple in the DC current. If the SMPC converter is employed for HVDC schemes with strict specifications on the DC side ripple, both the 'ω' and '2ω' ripple can be removed by the quadrature injection technique presented earlier in Section (4.8.1). This is not explored further in this thesis due to time limitations.

The actual circulating current in each phase leg is based on the measurements of UPP and LOW CL currents. It can be calculated as follows:

$$i^x_{circ} = \frac{i^x_{upp} + i^x_{low}}{2}$$

Since the circulating current includes both DC and AC components (out of which $i^a_{2\omega}$ is a sustained component in steady state), the circulating current control is realised using PR controller to achieve negligible steady-state tracking error. A parallel-cascaded P+2R control structure with one proportional controller and two resonant controllers is adopted. One resonant controller is tuned at the fundamental AC frequency while the other is tuned at the second harmonic AC frequency. The ideal

P+2R controller is represented by:

$$G_{P+2R}(s) = K_P + \frac{2K_{R_\omega}s}{s^2+\omega_0^2} + \frac{2K_{R_{2\omega}}s}{s^2+(2\omega_0)^2}$$

where K_P, K_{R_ω} and $K_{R_{2\omega}}$ are gain constants and ω_0 is the fundamental AC system frequency.

The two resonant terms in the P+2R controller provide infinite gains at ω_0 and $2\omega_0$ and no phase shift and gain at other frequencies. The proportional term determines the dynamics of the system in terms of bandwidth, phase and gain margins [95]. In practice, the infinite resonant gains can cause stability problems and hence, a non-ideal P+2R controller is adopted as follows:

$$G_{P+2R}(s) = K_P + \frac{2K_{R_\omega}\omega_{c_\omega}s}{s^2+2\omega_{c_\omega}s+\omega_0^2} + \frac{2K_{R_{2\omega}}\omega_{c_{2\omega}}s}{s^2+2\omega_{c_{2\omega}}s+(2\omega_0)^2}$$

where ω_{c_ω} and $\omega_{c_{2\omega}}$ represent the cut-off frequencies around the two resonant frequencies which determine the sensitivity to frequency variations around the resonant peaks.

A block diagram of the circulating current control is presented in Figure (5.13). The output of the controller is the component of the modulation reference contributed by the DC side control loops, $v^x_{DC_{mod}}$. The DC voltage is not added as a feed-forward term to the output as it gets included later in the CLs waveshaping. The circulating current is driven through the arm inductors and hence, the plant of the control loop can be expressed as (note that each of the upper and lower arm inductors are $\frac{L_{arm}}{2}$):

$$G_{CIRC}(s) = \frac{1}{sL_{arm}}$$

The circulating current reference is calculated from the outputs of the energy controllers as shown in Figure (5.14). The outputs of the IAEC and ICEC ($k^x_{2\omega}$ & m^x_ω) are applied the appropriate gains to obtain the amplitudes of the 2ω and ω circulating current components, which are then multiplied by the appropriate sinusoidal

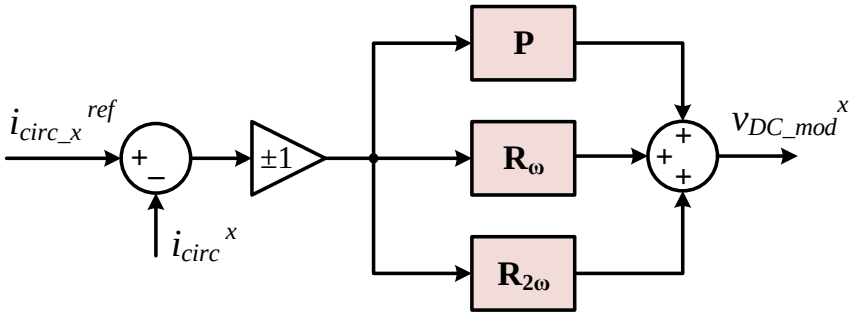


Figure 5.13: Circulating current control block diagram

functions. The angle arguments of these sinusoidal functions are obtained using the grid voltage angle from the single-phase PLL of the respective phase. It should be noted that the second-harmonic circulating current is negative-sequence but due to the use of single-phase PLLs, simply multiplying the PLL angle by 2 automatically takes care of the correct sequence in a three-phase system. Also, the output of the TEC (i_{DC}^{x}) is directly added to the circulating current reference.

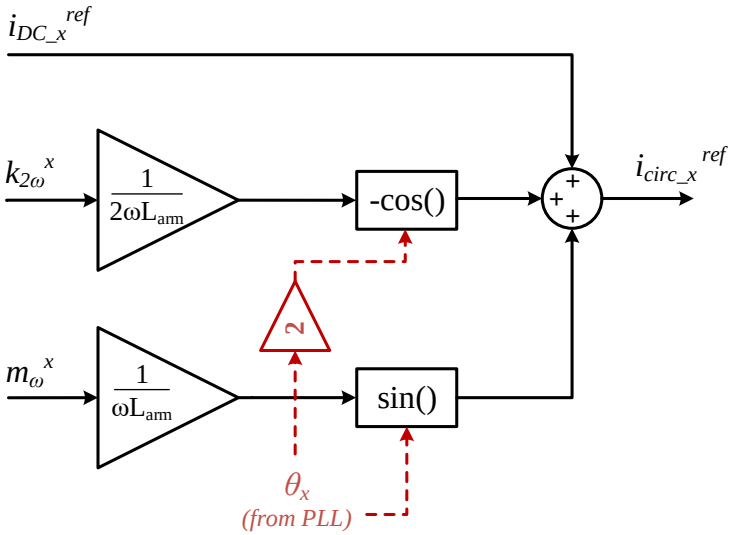


Figure 5.14: Circulating current reference calculation

5.3.4 CLs Waveshaping and Modulation

For the application specified prior to developing the control strategy presented thus far, in each phase-leg of the SMPC, the AC current control generates the first component of the modulation reference i.e. 'v_c^x'. In addition, a nested control on the DC side in which the energy controllers form the outer loop and the circulating current control forms the inner loop, produces the second component of the modulation reference i.e. '$v_{DC_{mod}}^x$'. The final modulation references for the CLs are then calculated as shown in Figure (5.15) where the final modulation references are marked in green.

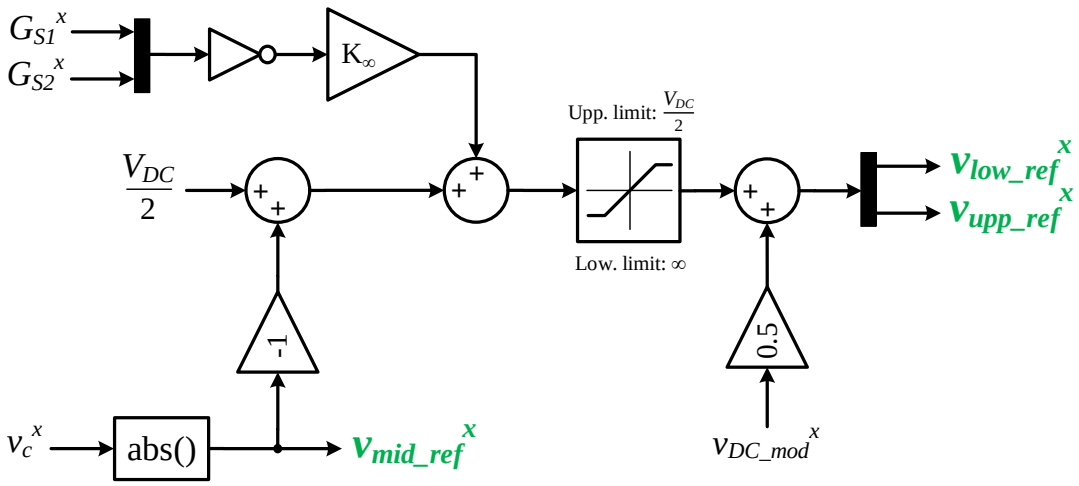


Figure 5.15: CLs waveshaping block diagram

The chosen CLs waveshaping has been explained in Section (4.3). Recalling from Figure (4.12) that the MID CL voltage is the full-wave rectification of the converter AC output voltage, the MID CL modulation reference ($v_{mid_{ref}}^x$) is then obtained by simply passing v_c^x through an 'absolute value' function.

For the UPP/LOW CLs, remembering that the DSs effectively modify the circuit connections each AC half cycle, the UPP and LOW CLs provide the function of full AC cancellation alternately over a fundamental cycle. Hence, it can be concluded

that their waveshaping is linked to the gating signals of the two series strings of IGBTs in the DS configuration i.e. S_1 and S_2. The gating signals for S_1 and S_2 (G^x_{S1} & G^x_{S2}) are defined as:

$$G^x_{S1} = \begin{cases} 1 & \text{if } v^x_c > 0 \\ 0 & \text{otherwise.} \end{cases}$$

$$G^x_{S2} = \overline{G^x_{S1}}$$

It should be noted that G^x_{S1} is associated with the LOW CL modulation reference ($v^x_{low_{ref}}$) while G^x_{S2} is associated with the UPP CL modulation reference ($v^x_{upp_{ref}}$).

It can also be recalled from Section (4.3) that the UPP and LOW CLs together block the remaining portion of the DC voltage. Hence, $\frac{V_{DC}}{2}$ is added to the inverse of $v^x_{mid_{ref}}$ followed by the addition of inverted outputs of G^x_{S1} & G^x_{S2} multiplied by a very high gain K_∞ ($K_\infty \gg \frac{V_{DC}}{2}$). The output is passed through a saturation block with the upper limit as $\frac{V_{DC}}{2}$ and lower limit as ∞. The K_∞ and the saturation block together implement the action of alternating half-cycle AC cancellation. Finally, one-half of the component of the modulation reference contributed by the DC side control loops ($v^x_{DC_{mod}}$) is added and the generated outputs are the UPP and LOW modulation references.

To modulate the CLs, the well-known Phase-Disposition Pulse Width Modulation (PD-PWM) technique is used. PD-PWM is a carrier-based modulation technique where the switching signal sequence is obtained by a simple comparison of the CL reference signals with level-shifted triangular carrier waves. Voltage transitions corresponding to each triangular carrier are associated with a particular SM [96]. To distribute the switchings evenly between the SMs over a fundamental period, SM selection methods called sorting are used.

The CLs modulation scheme is illustrated in Figure (5.16). To compensate for the cell voltage ripple, the modulation reference signal is first normalised with the sum of cell voltages of the CL. The "compensated" reference signal is then sub-divided into

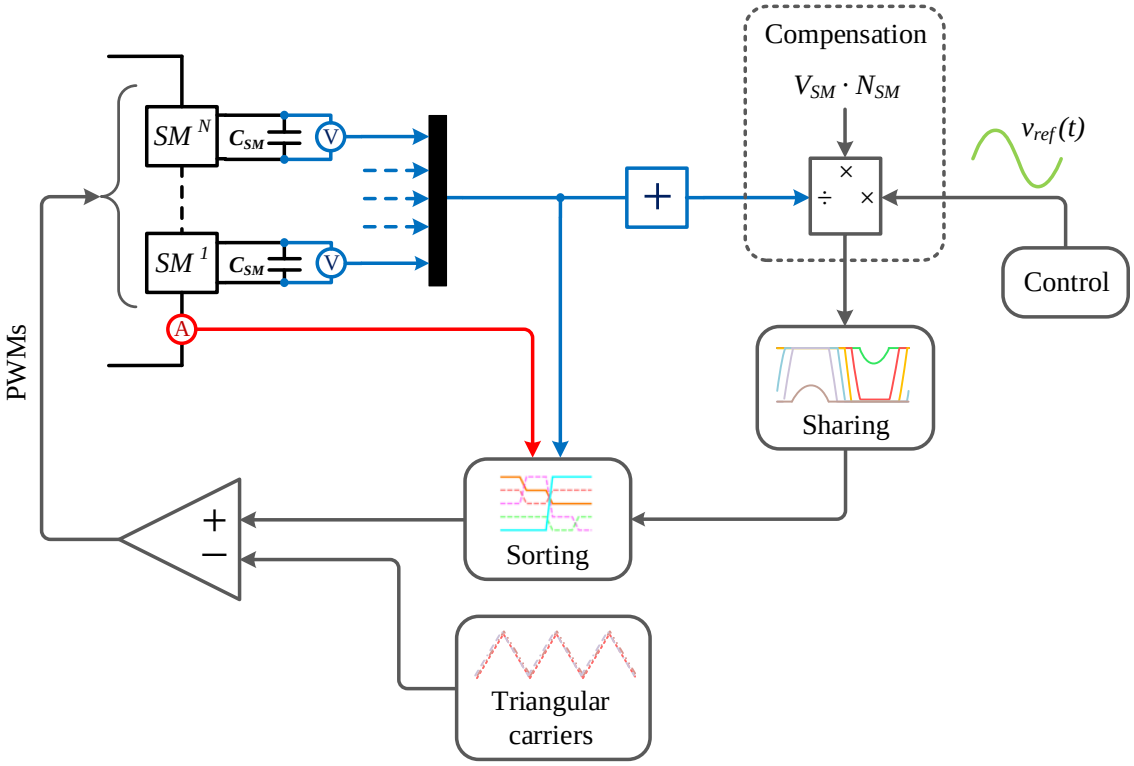


Figure 5.16: CLs modulation scheme

N_{SM} sub-modulation reference signals in the 'sharing' block. The sub-modulation signals are then sorted using a simple bubble sort algorithm that works though a data array comparing and swapping (when required) adjacent values until the array is fully sorted [97]. Note that the UPP/LOW CLs are formed of hybrid CLs and thus, the sorting mechanism depicted in Figure (4.21) is implemented. Finally, the sorted sub-modulation signals are compared with the triangular carriers that vary between 0 and the maximum value to generate the PWMs.

5.3.5 Controllers tuning

Correct tuning of the controller gains is essential to operate the converter successfully and to achieve the desired dynamic performance. Following are the two most important considerations when tuning the energy and current controllers in the SMPC:

- A cascaded control structure is employed in which the energy controllers form the outer loop and generate the reference for the inner circulating current controllers. While designing the energy control architecture, the dynamics of the circulating current controller are neglected as the latter is assumed to be much faster than the former. Thus, this assumption needs to be respected when selecting the controller bandwidths.

- Within the energy control, in order to make the energy management analysis valid, the TEC has to be designed for a bandwidth higher than the IAEC and ICEC.

Starting with the AC current controller, it is designed for a high bandwidth of $\omega_c = 2\pi \cdot 300$ rad/s in order to quickly respond to changes in grid current demand. In the PR transfer function used for this controller given in Eq. (5.3), ω_c dictates the time-constant of the first-order envelope of the grid current amplitude in response to a current reference amplitude step [93]. The open-loop bode plot of the AC current controller is shown in Figure (5.17) where it can be observed that the gain is highest at the resonant frequency ω_s which results in effective signal tracking at that given frequency. Moreover, the phase margin is $PM_{AC} = 76.4°$, indicating that the closed-loop control is stable.

Because of the approach taken to formulate the control loop models in Section (5.3.2), the plants for energy controllers are simply integral. The TEC, IAEC and ICEC use PI controllers that are designed to give appropriate bandwidths and transient responses according to the requirements for the cascaded loops. The inputs to the design process of the energy controllers are the natural frequency ω_n which majorly controls the response speed, and the damping ratio ζ which controls the oscillations. Remembering that the energy control forms the much slower outer control loop and that the TEC should act quicker than the IAEC and the ICEC, the natural frequencies chosen for the energy controllers are: $\omega_{n_{TEC}} = 2\pi \cdot 7$ rad/s, $\omega_{n_{IAEC}} = 2\pi \cdot 2.33$ rad/s, $\omega_{n_{ICEC}} = 2\pi \cdot 2.33$ rad/s. A damping ratio of $\zeta = 1$ has been used for all three

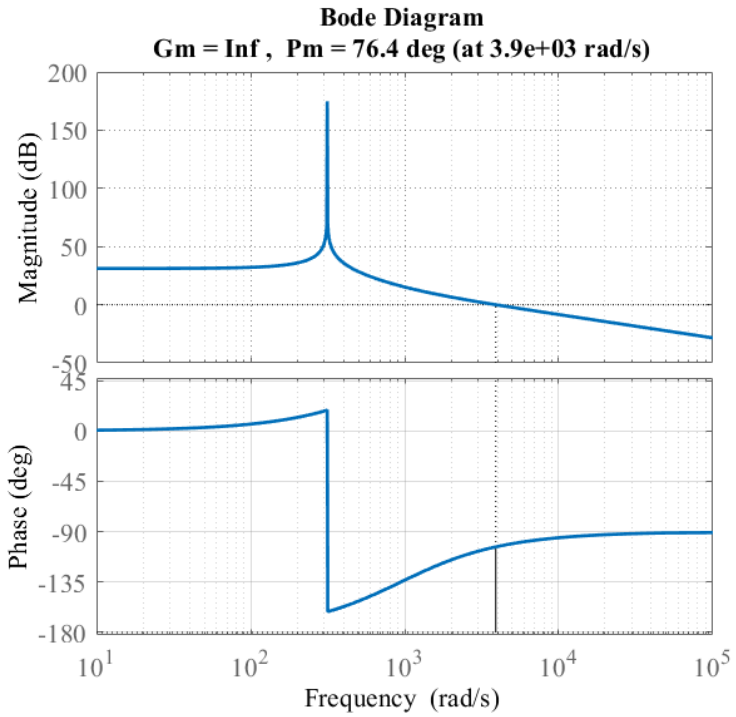


Figure 5.17: AC current control bode plot

controllers. The proportional and integral gains of the PI controllers are designed according to these specifications considering the respective plants for all energy loops. The step responses of the energy controllers are presented in Figure (5.18).

Finally, the inner circulating current control loop is designed for a faster bandwidth of $\omega_c = 2\pi \cdot 300$ rad/s. The cut-off frequencies around the resonant frequencies are selected as $\omega_{c_\omega} = \omega_{c_{2\omega}} = 2\pi$ to achieve a good compromise between the controller selectivity (narrower resonant peaks) and sensitivity (frequency variations around resonant peaks). High resonant gains are selected to achieve zero steady-state error with $K_{R_{2\omega}}$ twice as much as K_{R_ω} to achieve overall similar gains at the resonant peaks. The open-loop bode plot of the circulating current controller is given in Figure (5.19). The phase margin is $PM_{CIRC} = 56.5°$, indicating that the closed-loop control is stable.

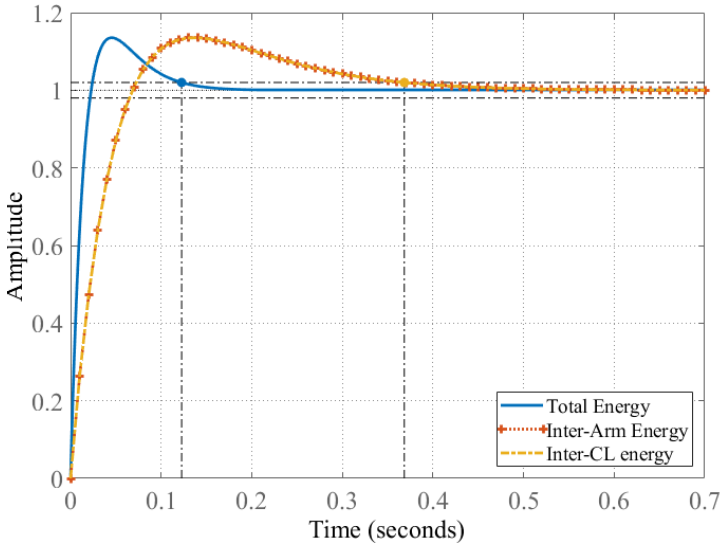


Figure 5.18: Step responses of the energy controllers

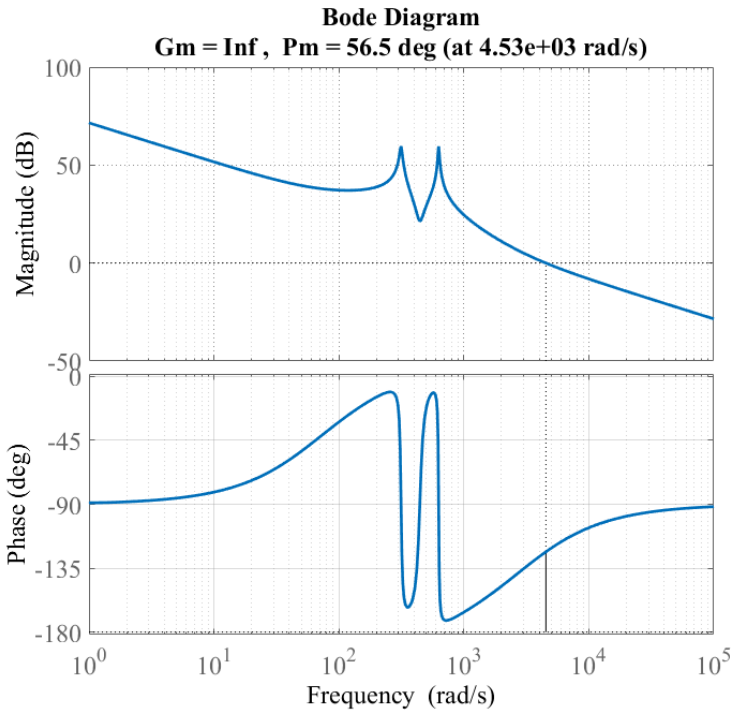


Figure 5.19: Circulating current control bode plot

5.4 Simulation Results

In order to validate the converter concept and the proposed control scheme, computer simulations have been performed using the PLECS® simulation package. The converter arrangement of Figure (5.3) is considered for the simulation study using the system ratings defined in Section (4.5.2). Table (5.1) reports the simulation model parameters and includes the system, converter and control parameters.

System parameters	
Line-to-line AC rms voltage (V_{AC})	11 kV
DC voltage (V_{dc})	20 kV
Transformer turns ratio (r)	1.3
AC side inductor (L_s)	2.3 mH
AC side resistance (R_s)	50 mΩ
AC system frequency (f_s)	50 Hz
Converter parameters	
Number of UPP/LOW CL SMs ($N_{SM}^{upp/low}$)	5 HBs + 3 FBs
Number of MID CL SMs (N_{SM}^{mid})	9 HBs
UPP/LOW CLs SM capacitance ($C_{SM}^{upp/low}$)	4.18 mF
MID CL SM capacitance (C_{SM}^{mid})	1.1 mF
Arm inductance ($\frac{L_{arm}}{2}$)	4 mH
SM nominal voltage (V_{SM})	1500 V
Switching frequency (f_{PWM})	5 kHz
Controllers parameters	
AC current control bandwidth ($\omega_{c_{AC}}$)	1885 rad/s
TEC natural frequency ($\omega_{n_{TEC}}$)	44 rad/s
IAEC natural frequency ($\omega_{n_{IAEC}}$)	14.64 rad/s
ICEC natural frequency ($\omega_{n_{ICEC}}$)	14.64 rad/s
CIRC current control bandwidth ($\omega_{c_{CIRC}}$)	1885 rad/s

Table 5.1: SMPC simulation model parameters

The model developed is a complete switching model with ideal semiconductor devices

that toggle instantaneously between the on-state and the off-state. Ideal devices are used to allow ease of use and improved simulation speed and they are sufficient to investigate all aspects of control and thermal management [98]. Moreover, single-phase AC side transformers used in the model are also considered ideal.

The results of the simulation are first presented for the steady-state converter operation considering both rated active and reactive power exchange under balanced grid conditions. The transient response of the converter as dictated by the designed control loops is also validated by changing the active and reactive power references. Finally, the unbalanced AC voltage sag case is simulated to demonstrate the open-loop implementation of the quadrature current injection method proposed in Section (4.8.1) for DC ripple removal.

5.4.1 Steady-state operation

The steady-state results for the SMPC operation are presented in Figure (5.20) for rated rectifying active power (P=+20 MW) and rated inductive reactive power (Q=+8MVAr). The transformer turn ratio given in Table (5.1) is appropriately selected to operate the converter at a modulation index of $M = 0.75M_{ss}$, which is the value of the optimum modulation index adjusted for operation with hybrid CLs in UPP/LOW CLs as discussed in Section (4.6). The results confirm operation as expected from the analysis. In Figure (5.20), the voltages generated by the UPP/LOW CLs and the MID CL for phase a verify the correct implementation of the chosen waveshaping presented in Section (4.3) since the CL voltages from the simulation match the theoretical waveforms presented in Figure (4.10). The value of the modulation index is $M = 0.75M_{ss} = 1.178$ and thus, as expected with over-modulation operation, UPP/LOW CL voltages generate a small negative voltage justifying the use of a few FBs (hybrid CLs). It can also be seen that the MID CL voltage is the full-wave rectification of the converter AC output voltage as dictated by the waveshaping.

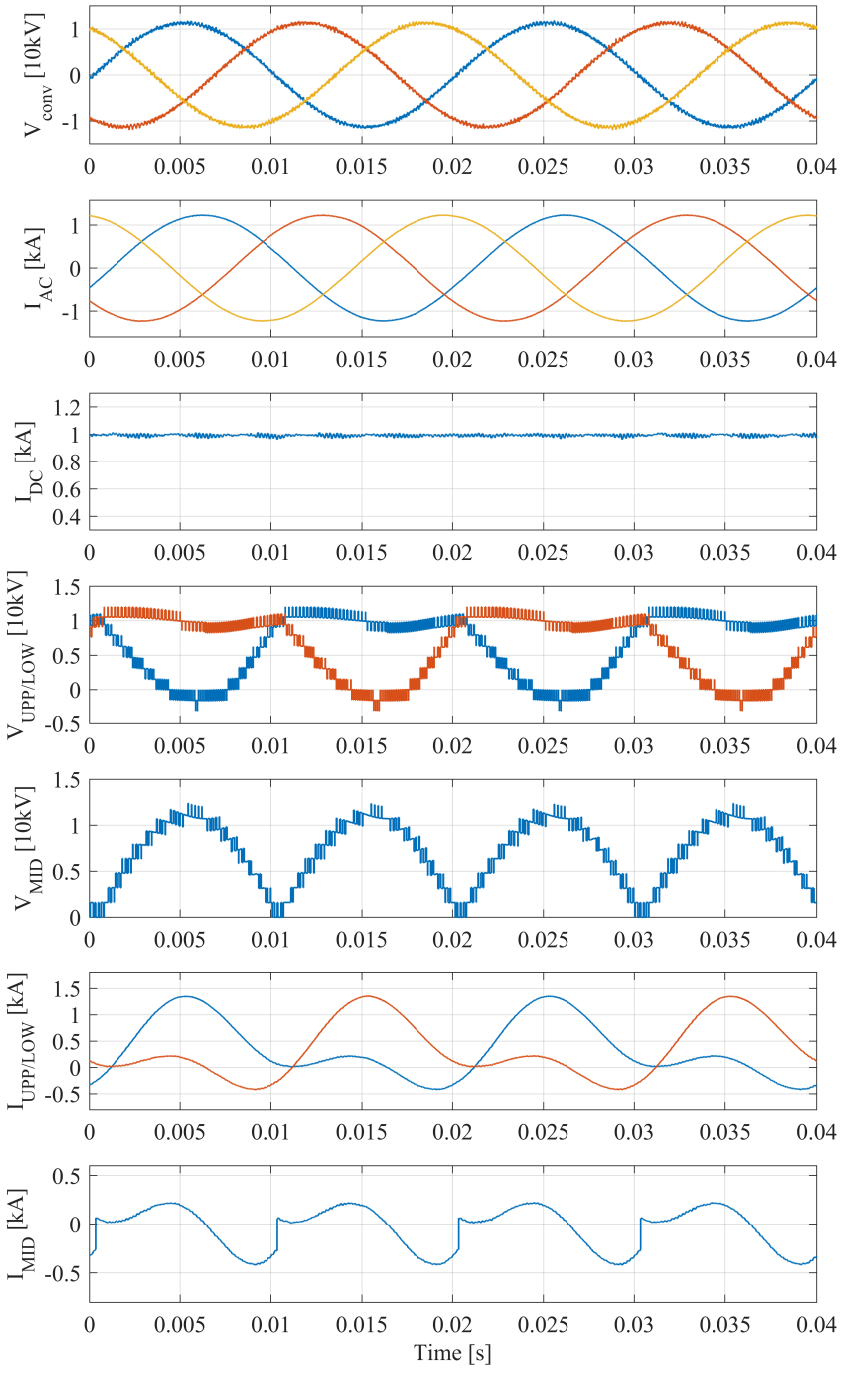


Figure 5.20: SMPC simulation results for P=20MW & Q=8MVAr. Counting from top to bottom: (1) Converter output voltages (2) AC side currents (3) DC side current (4) UPP/LOW CL voltages (phase a) (5) MID CL voltage (phase a) (6) UPP/LOW CL currents (phase a) (7) MID CL current (phase a)

Phase a CL currents from the simulation are also presented in Figure (5.20), demonstrating the basic two-arm operating principle of the converter with the MID CL switched between upper and lower arms every half cycle. It can be seen that in the positive half cycle, the MID CL current equals the LOW CL current while in the negative half cycle, it is the same as the UPP CL current. This behaviour is in accordance with the converter operation discussed in Section (4.3).

Since the converter is operated away from the 'sweet-spot', the second harmonic is injected in the circulating current for energy balancing as discussed in Section (4.4). The effect of the second harmonic on the CL voltages and currents wave-shapes can be observed. Moreover, as expected under balanced conditions, the second harmonic components in the phase legs of the converter cancel on the DC side as it can be seen that there are no low frequency components present in the DC side current.

The SM voltages for phase a are presented in Figure (5.21). It can be observed that they are stable around the nominal set-point of 1.5 kV and the ripple margin of 20% peak-to-peak is respected. As expected, the MID CL SM voltages oscillate at twice the AC fundamental frequency. In the UPP/LOW CL SM voltages, periods of no change in some SM voltages can be noticed when the HBs in the hybrid CLs are by-passed in the negative voltage region.

5.4.2 Transient response

This section presents simulation results showing the dynamic response of the controllers to changes in system set-points. First, the case of a reduction in the active power reference is simulated. The results are shown in Figure (5.22). A step reduction in P_{ref} from 20 MW to 10 MW is applied at 0.16s. The AC current controller that is designed for a high bandwidth (300 Hz) tracks the new reference in less than half a cycle. The SM voltage dynamics are dictated by the slowest energy loops i.e. IAEC and ICEC, and the step responses for these loops, shown earlier in Figure

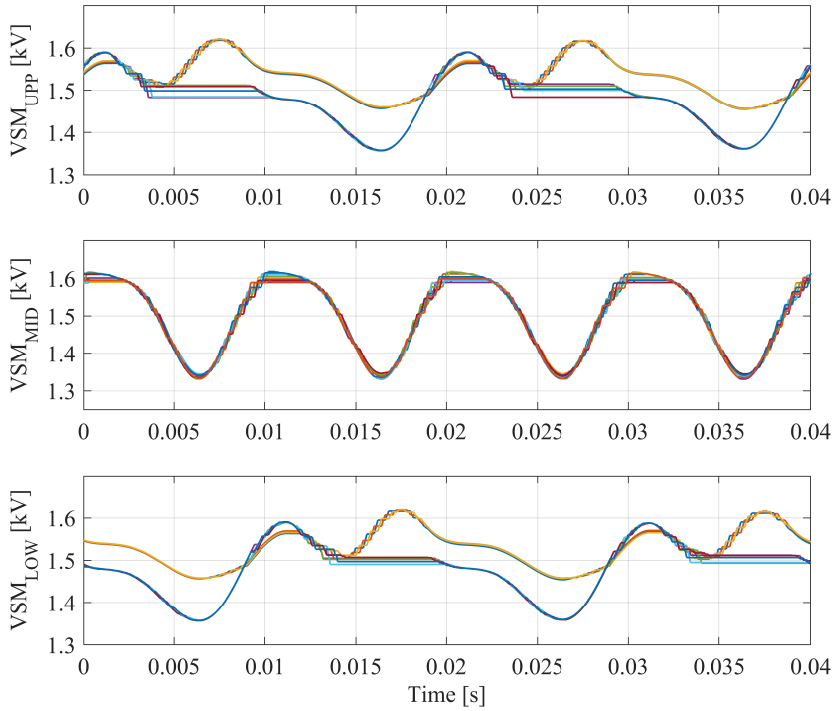


Figure 5.21: Ph. *a* UPP SM voltages (top), ph. *a* MID SM voltages (middle) and ph. *a* LOW SM voltages (bottom)

(5.18), settle in 0.4s-0.5s. Thus, as expected, the SM voltages in Figure (5.22) also return to the nominal value within 0.4s-0.5s.

Figure (5.23) shows the averaged energy transients (AC ripple removed) of each of the individual energy controllers where E_{TOT} corresponds to TEC, E_{DIFF} corresponds to IAEC and E_{CORR} corresponds to ICEC. The results verify the different bandwidth selections for the energy controllers. As can be observed, the TEC is the fastest to respond, with a three times lower settling time than the IAEC and ICEC responses. Individually, the TEC response settles within 0.1s-0.2s and the IAEC & ICEC responses settle within 0.4s-0.5s which matches the step-response behaviour shown earlier in Figure (5.18). The oscillations in the TEC response is a result of its interaction with the IAEC and ICEC loops. These oscillations can be reduced by further decreasing the bandwidths of IAEC and ICEC which in turn, lowers the coupling between TEC and IAEC/ICEC and lessens the interaction between them. The

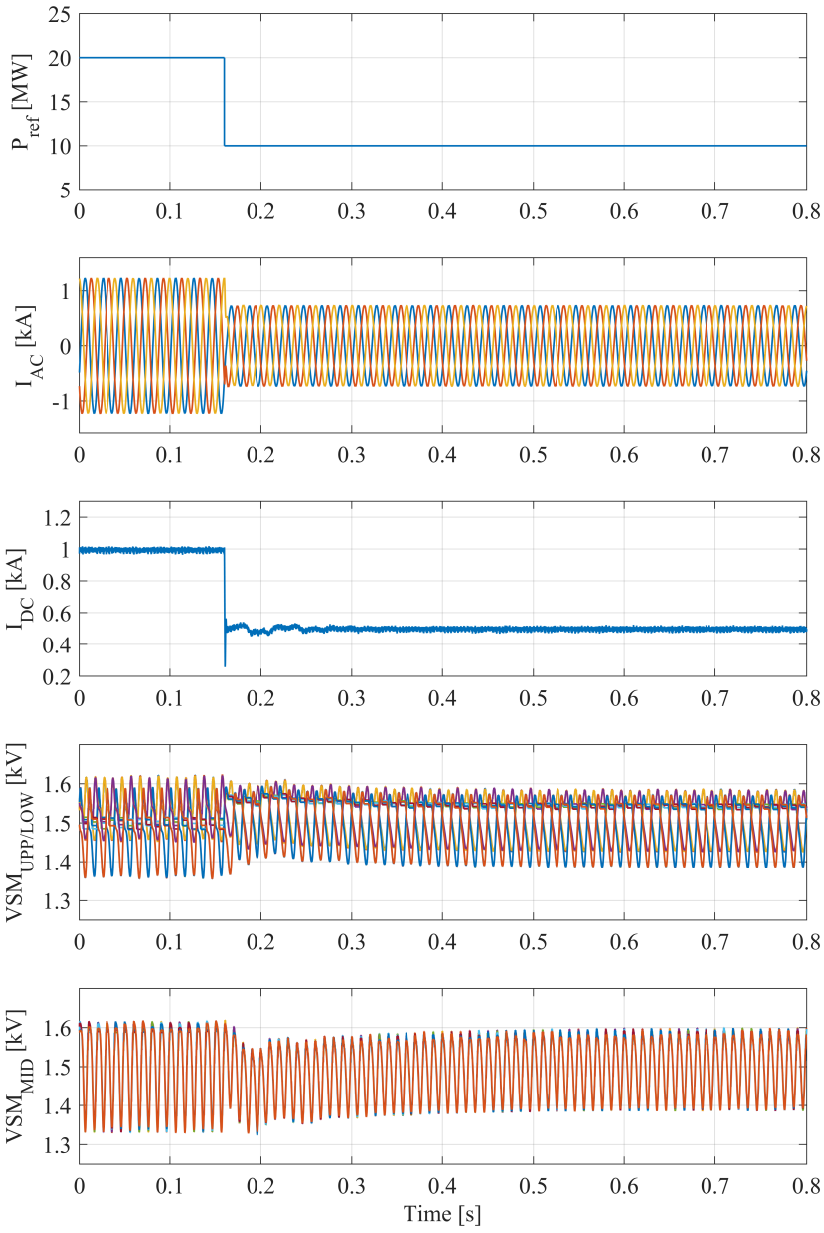


Figure 5.22: Transient results for a step reduction in P_{ref} from 20 MW to 10 MW. Counting from top to bottom: (1) Active power reference (2) AC side currents (3) DC side current (4) UPP/LOW SM voltages (phase a) (5) MID SM voltages (phase a)

downside is a larger time taken for the capacitor voltages to return to the nominal value.

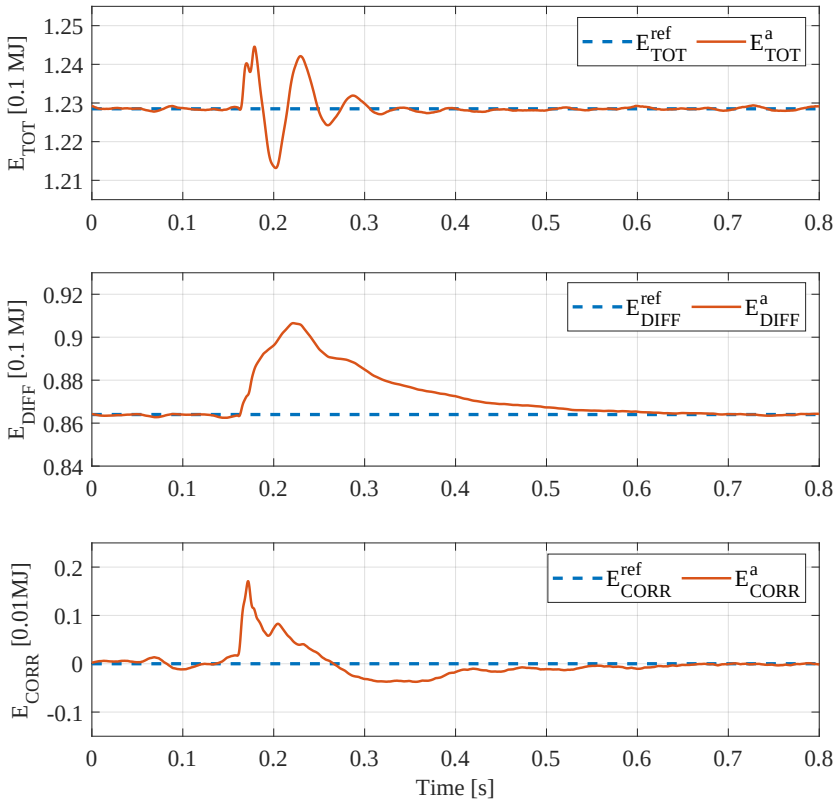


Figure 5.23: Averaged energy transients of Phase a for a step reduction in P_{ref}. Counting from top to bottom: (1) Total energy transient (TEC) (2) Differential energy transient (IAEC) (3) Correctional energy transient (ICEC)

The dynamic response of the controllers is further simulated for a step change in the reactive power reference from rated inductive Q (+8 MVAr) to rated capacitive Q (-8 MVAr). The results are presented in Figure (5.24) where the step is applied at 0.1s. The fast response of the AC and DC current controllers can again be noticed and the SM voltages also become stable within 0.4s-0.5s as expected. The ability of the converter to successfully supply rated Q to and absorb rated Q from the AC system without breaching the design limit of 20% peak-to-peak ripple in the SM voltages can be appreciated. The DC current has a small transient ripple at 50 Hz before it settles which is due to the differences in energy controller outputs between the three phase legs during transients which results in slightly unbalanced circulating currents.

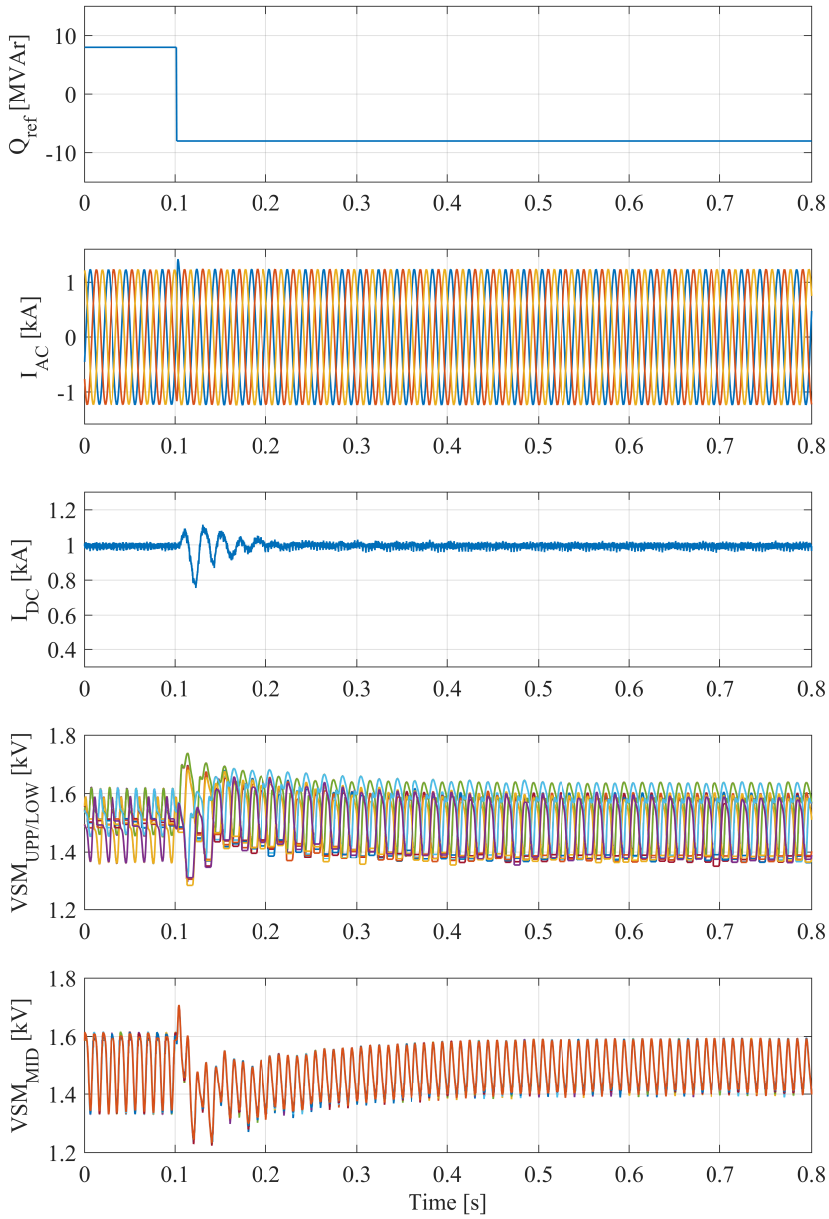


Figure 5.24: Transient results for a step reduction in Q_{ref} from +8 MVAr to -8 MVAr. Counting from top to bottom: (1) Active power reference (2) AC side currents (3) DC side current (4) UPP/LOW SM voltages (phase a) (5) MID SM voltages (phase a)

The averaged energy transients are displayed in Figure (5.25), verifying again that the response speeds for which the energy controllers are designed are respected even when the step change is in a different system set-point (Q in this case).

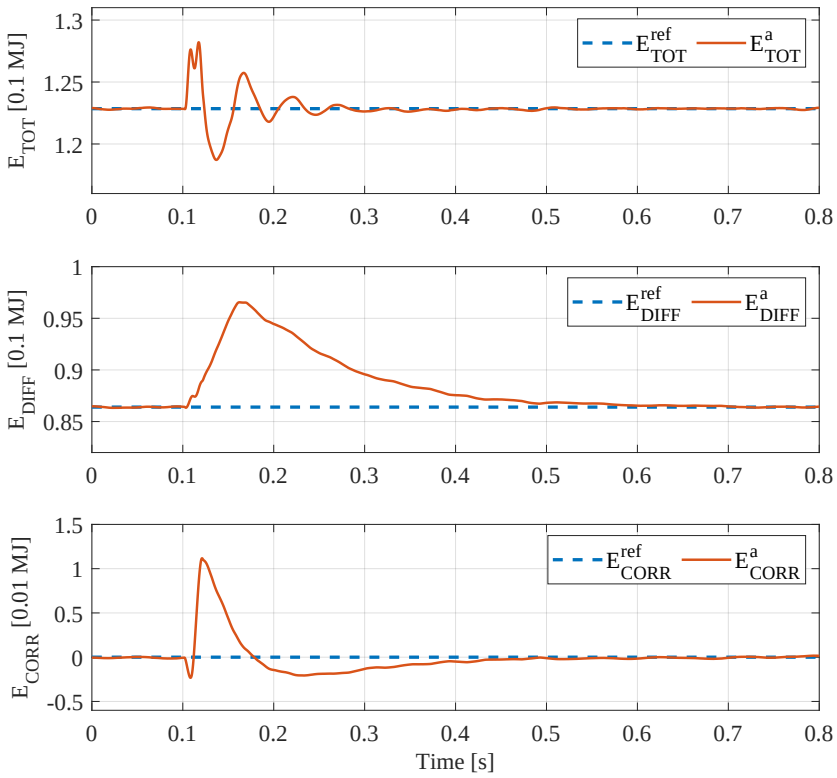


Figure 5.25: Averaged energy transients of Phase a for a step change in Q_{ref}. Counting from top to bottom: (1) Total energy transient (TEC) (2) Differential energy transient (IAEC) (3) Correctional energy transient (ICEC)

5.4.3 AC voltage sag

As discussed in Section (4.8.1), in case of an unbalanced fault on the AC system, a 2ω ripple appears in the DC current. Subsequently, a method called 'quadrature compensation' based on injection of quadrature 2ω current components in the CLs was proposed in which the sum of the quadrature currents opposes the 2ω ripple in the DC current during a DC fault.

In this section, results from a simulation study that considers the case when a 50% AC voltage sag occurs in one phase alone are presented. During the fault, only positive sequence current is exchanged between the converter and the grid. Moreover, the pre-fault active power levels are maintained for the duration of the fault. It is worth mentioning here that the goal of simulating AC faults is to demonstrate the open-loop implementation of the quadrature compensation method. Hence, the investigation of AC fault behaviour in the SMPC is limited only to simulation studies in this thesis and experimental validation of the subject is considered out of scope.

Some minor changes to the previously presented AC current control strategy are necessary to deal with AC unbalanced faults. The AC current reference calculation function of Section (5.3.1) is modified to control the negative sequence current to zero. This requires extraction of the positive-sequence PLL angle (θ^{+}_{PLL}) and the amplitude of the positive-sequence grid voltage ($\hat{V}^{+}_{s}$). If the AC current reference calculation in Figure (5.6) is performed using θ^{+}_{PLL} and $\hat{V}^{+}_{s}$, then the resulting AC current will be composed of only positive sequence components as the PR controller ensures accurate reference tracking.

For the AC fault simulation study, the general single-phase PLL structure presented in Figure (5.7) (which is used for the balanced case as well as in the experimental work) is replaced with an alternative three-phase PLL structure that allows the extraction of θ^{+}_{PLL} and $\hat{V}^{+}_{s}$. This PLL structure is introduced in [5] and enables fast detection of the grid voltage positive sequence (or negative sequence if needed) within one grid voltage cycle. The structure is illustrated in Figure (5.26) in which the grid voltage vector is first transformed to dq voltages using a rotating reference frame at fundamental frequency and with an arbitrary angular position (θ_f). In the next stage, the dq voltages are passed through moving average filters (MAFs) to filter any oscillations due to harmonics and negative sequence components. The filtered dq outputs are then transformed back into *abc* components using the same θ_f to obtain undistorted fundamental positive sequence voltages ($\bar{v}_a$,$\bar{v}_b$,$\bar{v}_c$ in the figure). These variables are finally fed into a conventional PLL to obtain the positive-sequence PLL

angle.

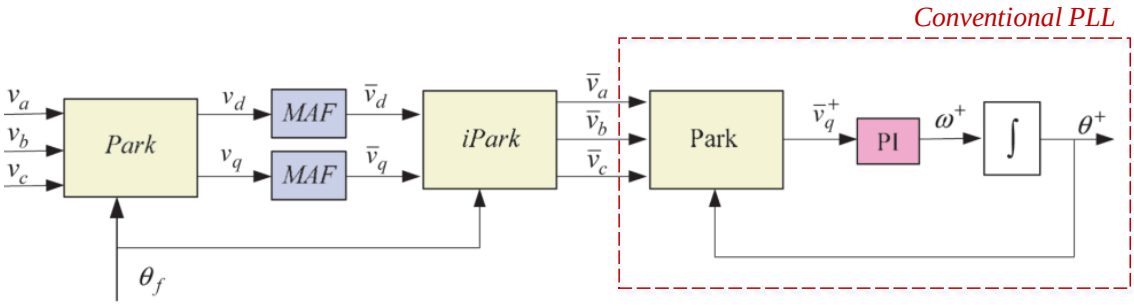


Figure 5.26: PLL structure for positive-sequence extraction [5]

In Section (4.8.1), it was discussed that in order to remove the 2ω ripple in the DC current ($I_{2\omega}^{DC}$ in Figure (4.34a)) during a DC fault, the required resultant 2ω quadrature DC current ($I_{2\omega}^{DC^Q}$ in Figure (4.34a)) should be equal to $-I_{2\omega}^{DC}$. It was further explained using Figure (4.34b) that $I_{2\omega}^{DC^Q}$ should be optimally decomposed on the nearest neighouring quadrature axes using an algorithm. In PLECS, this algorithm is implemented using its built-in 'C-script' block. At the output of the 'C-script' block, the desired 2ω quadrature currents for the three phase legs are generated, which are eventually added to the circulating current reference calculation depicted in Figure (5.14). The simulation results for a 50% AC voltage sag in Phase a are presented in Figure (5.27). The system is operated at full rated active power and unity power factor. After the fault is applied at 0.11s, the AC current stays balanced and increases in magnitude to maintain pre-fault active power, since the positive sequence of the grid voltage is reduced.

The 2ω ripple in the DC current during the fault can be observed between the fault application at 0.11s and 0.3s. At 0.3s, the open-loop 'quadrature compensation' is activated which completely removes the fault DC ripple. There is no noticeable increase in the SM voltage ripples after quadrature compensation is implemented, verifying that the optimal quadrature axes are selected as discussed previously in Section (4.8.1). Finally, when the Phase a voltage is restored to 100% at 0.6s, the system smoothly returns to normal operation. Overall, the results demonstrate the

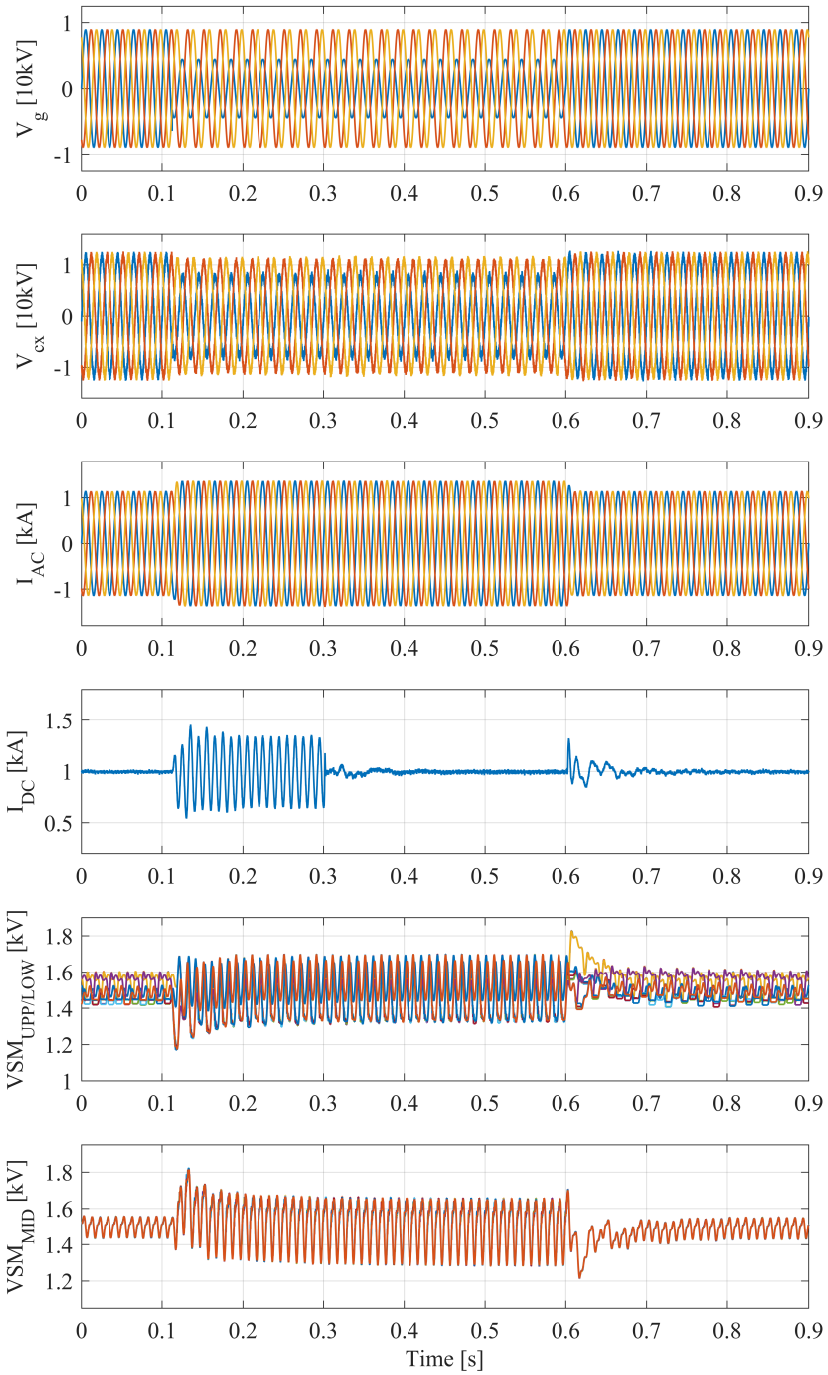


Figure 5.27: Simulation results for a 50% AC voltage sag in Phase *a*. Counting from top to bottom: (1) Grid voltages (2) Converter output voltages referred to a fictitious DC mid-point x (3) AC side currents (4) DC side current (5) UPP/LOW SM voltages (phase *a*) (6) MID SM voltages (phase *a*)

ability of the converter to uninterruptedly supply the rated active power in a single-phase AC fault, meanwhile keeping the DC side ripple-free using an effective method of 2ω quadrature current injection.

5.5 Summary

In this chapter, the overall control analysis and design for steady-state, transient and AC fault operation of the SMPC are presented. A comprehensive simulation study using PLECS was also undertaken to validate the control analysis, the proposed control approach and the resulting control design. In the application considered, the AC power demand is assumed to be imposed by the application and the DC power is regulated to implement internal energy management of the converter.

Initially, an overall control scheme that is decoupled on the AC and DC sides is devised. The main control loops identified are the AC current control, energy control and the circulating current control. The energy control is further divided into three parallel control loops - (1) TEC that controls the global power balance in each phase (2) IAEC that controls the differential energy between the UPP/LOW CLs and MID CL and (3) ICEC that regulates the correction energy between the UPP CL and the LOW CL. The three energy control loops together produce the reference for the circulating current controller. Block diagrams for all control loops are presented including the plant gains and in addition, the plants for controller design are also derived. In order to compute the modulation references from the control outputs, the selected waveshaping of the CLs is implemented. For modulation of the CLs, the PD-PWM technique is employed. The modulation references are normalised with the sum of the cell voltages, split into sub-signals, sorted and then compared with triangular carriers to generate the PWMs for the switches.

To verify the converter concept and the proposed control strategy, PLECS simulations for a medium-voltage 20 kV DC - 11 kV AC system are performed. Results

for the steady-state operation at P=20MW & Q=8MVAr show the ability of the converter to produce low-distortion AC current waveforms, meanwhile keeping the DC current free from any major lower-order harmonic ripple, eliminating the need for any DC side filters. Morever, the two-arm operating principle of the converter is also demonstrated through the CL current waveforms. For the purpose of validating the dynamic response of the controllers, step changes in the system set-points (P_{ref} & Q_{ref}) are simulated. The results validate the fast response of the AC and DC current controllers to changes in operating point and in addition, verify the different bandwidth selections for the three energy controllers. Finally, a fault scenario of 50% voltage sag on one of the AC phases is simulated. It has been shown that the converter is able to supply the rated active power during the fault without interruption, meanwhile maintaining the DC side ripple-free using an innovative approach based on injection of 2ω quadrature current components to deal with unbalanced operation.

Chapter 6

Experimental setup

6.1 Introduction

Experimental work is a critical step in validating the operation of novel multilevel VSC circuits. Considering the difficulty in testing at high voltages, laboratory prototypes are generally scaled down to lower voltages. They enable the use of a reduced number of series-connected modules and are sufficient to prove the converter concept.

The experimental rig used for this project is a down-scaled flexible modular multilevel converter laboratory prototype, designed and constructed by Dr. Francesco Tardelli and Dr. Alessandro Costabeber at the University of Nottingham PEMC Research Group lab facility. Details of the prototype were first reported in [99] and another prototype construction based on the same design was discussed in [100]. Flexibility in the connection configuration of the SMs was one of the main design aims of this prototype, making it possible to test different multilevel converter circuits with the same hardware equipment. However, to adapt the prototype to the SMPC operation, some hardware particular to the topology has been added, notably the arm inductors, additional current sensors, signal conditioning circuits and an implementation of the DS configuration, named as the "Front-End" Half Bridge (FEHB) in this chapter.

Initially in this chapter, a brief description of the experimental setup is given. First, the hardware structure is explained including the design of the Sub-Modules (SMs) and the FEHB configuration. Afterwards, the control structure of the prototype is discussed that includes the description of the control architecture and the control interface boards employed in the experimental setup.

6.2 Description of the Experimental Setup

6.2.1 Overview

The experimental rig is a three-phase converter with a nominal power rating of 4.5 kW. Each phase is composed of a total of 8 SMs that can be flexibly configured to form the desired number of CLs and SMs per CL in each converter phase, depending on the topology. The SMs are designed to operate as FBs but can be easily adjusted to operate as HBs by excluding one of the FB leg using a selectable hardware option.

The overall schematic of the experimental setup is illustrated in Figure (6.1) which shows the positions of the external voltage and current sensors. Taking into consideration the practical limitations, the following differences in the practical setup in comparison to the converter configurations proposed in the previous chapters can be highlighted:

- *The DC side is connected to a resistor instead of a DC voltage source:* The load on the DC side imposes the DC power demand. This operating mode can be referred to as a DC grid forming converter since the converter forms a constant DC voltage on the load. The power flow is unidirectional (AC to DC) with the converter acting as a rectifier.

- *AC side transformers are not used:* As the SMPC circuit can be operated without a transformer, the transformer is omitted for cost reasons. A variable

AC power supply is used to adjust the AC voltage in relation to the specified DC voltage in order to ensure optimum modulation index operation.

- *Only FBs are used instead of Hybrid CLs in UPP/LOW CLs:* In the interest of distributing the available HB and FB SMs adequately amongst the three CLs, it is found best to compose UPP/LOW CLs with FBs only. This also reduces complexity in code implementation. Experimental validation using hybrid CLs in UPP/LOW CLs is the subject of future work and can be undertaken by adding a few more SMs in each phase.

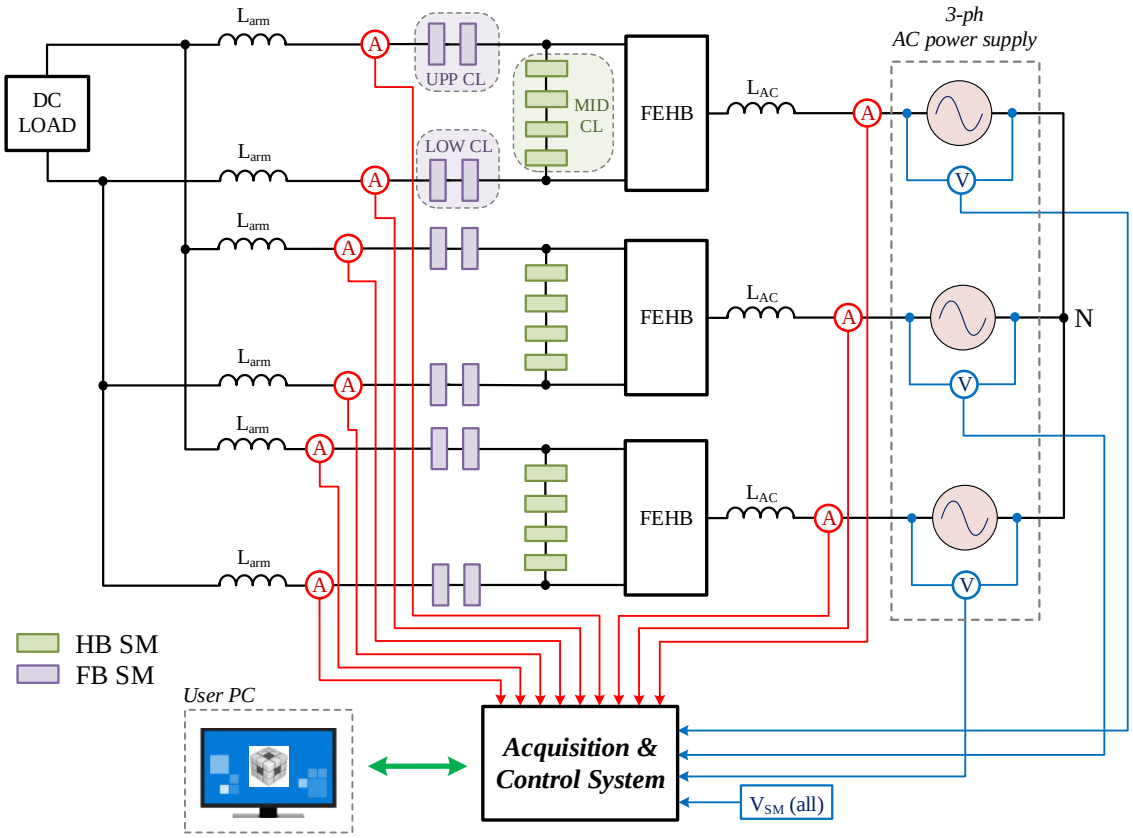


Figure 6.1: Schematic of the experimental setup

For the SMPC, the prototype is operated for a lower power rating of 1.5 kW, which is due to the unavailability of the DC side loads, at the time of the experiment, suitable for a higher power dissipation. The prototype is rated for 175 V DC voltage and a nominal SM voltage of 50 V is assumed. In each phase, out of the 8 SMs, 4 SMs are

used as HBs to form the MID CL and 2 SMs each are employed as FBs for both UPP and LOW CLs. This distribution ensures that the maximum voltage ratings of the CLs are respected i.e. 10% - 15% above half the DC voltage for the UPP/LOW CLs and peak AC voltage for the MID CL. In order to enable the power flow on the AC side, phase inductors are required. In addition, each phase has two arm inductors which are necessary for the circulation of the second harmonic balancing current for energy management.

The main experimental rig enclosure is shown in Figure (6.2) along with the FEHB on the right. The three vertical stacks of 8 SMs each are clearly visible. The SM stacks are interfaced to their respective controllers through the backplane PCB. AC phase inductors are placed next to each stack and the 6 arm inductors are placed behind the enclosure. SM inter-connections are configured on the rear frame of the enclosure. The primary (master) controller sits on top of the enclosure and communication links have been established between the controllers through optical fibres.

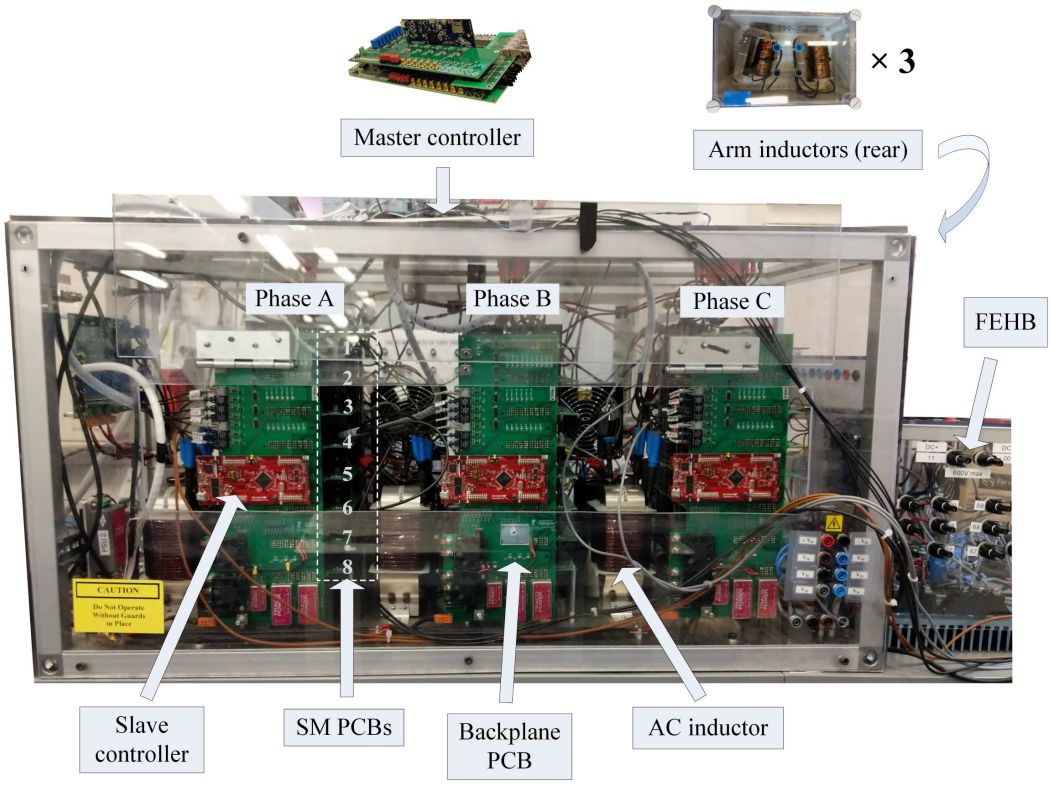


Figure 6.2: Experimental rig enclosure and the FEHB

A more detailed account of the components of the hardware and control structure of the prototype is now presented in the following sections.

6.2.2 Prototype Hardware Structure

6.2.2.1 Sub-Modules

The Sub-Module (SM) is the most critical component in multilevel converters. The salient features of the SM PCB design are low-cost build and compactness, achieved by the use of discrete low voltage MOSFETs and general purpose electrolytic capacitors. The SM PCB is shown in Figure (6.3) and can be broadly divided into four separate sections: the power circuit, the control circuit, a built-in pre-charge circuit and a voltage sensing circuit. In addition, there are 3 DC/DC converters that supply ±15 V to power the gate drivers, power terminals that connect the SM to the adjacent SM or the AC/DC terminal and a connector that plugs into the backplane PCB.

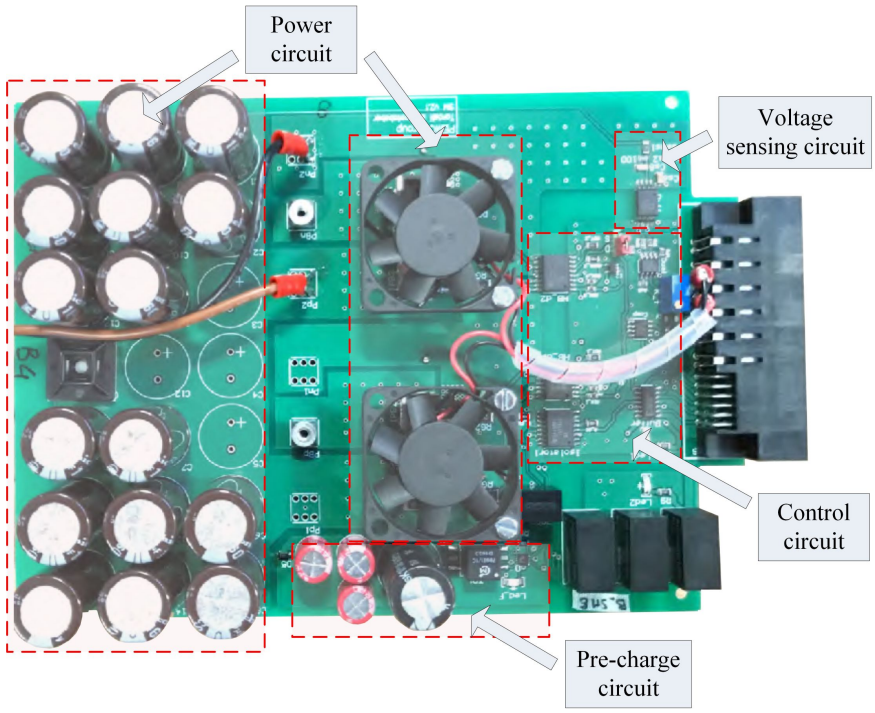


Figure 6.3: SM PCB

Power Circuit: In the power circuit, the switching devices used are the low on-state resistance and fast-switching IPB072N15N3 MOSFETs, rated for 150 V and 100 A. Since the general purpose electrolytic capacitors used have a low current rating, 16 capacitors of 330 μF are connected in parallel to form the local DC link, thereby ensuring safe operation. The combined capacitance of the SM is 5.28 mF. The electrical output terminals of the SM are located between the MOSFETs and the capacitors. Cooling fans are mounted above the MOSFETs that operate with 12 V.

Control Circuit: The functions of the control circuit are to drive the SMs and to isolate the power side from the control platform. Hence, the components used in this section of the SM PCB are the gate drivers and the digital isolator which creates isolation between the pre-charge circuit and the control side. The inputs to the control circuit from the backplane PCB through the connector are 2 PWM signals for the two legs of the FB (1 PWM signal if the SM is operated as a HB), a disable signal to either block or unblock the SM as desired and an enable signal for the pre-charge circuit. The outputs of the SM control circuit to the local controller are the over-voltage trip signal and the measured SM voltage.

The gate driver is the Texas Instrument UCC21520, which is a dual-channel gate driver with a 5.7 kV_{rms} reinforced insulation barrier between the input and the output. The gate driver circuit is shown in Figure (6.9). 3.3 V are supplied to the input side while the outputs are supplied with two independent 15 V sources (from the two DC/DC converters). When a logic '1' is applied at the input, the gate driver outputs +15 V, and 0 V when logic '0' is applied. The two devices in each leg can be controlled complementarily. Hence, the main PWM signal is for the high side MOSFET, and is inverted to generate the low side signal. To reduce the ringing caused by the non-ideal PCB layout, both the PWM signals are filtered by an RC network before routing to the gate driver inputs.

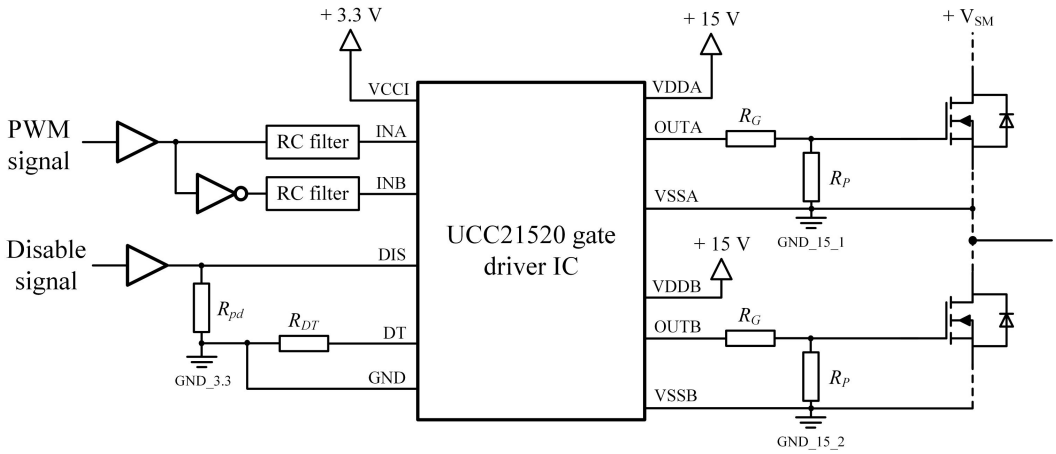


Figure 6.4: Gate driver circuit

The disable signal coming from the control board that blocks/unblock the SM operation is connected to the 'disable' pin of the driver IC through a buffer. The dead-time (DT) is a critical parameter that avoids shoot-through between the two MOSFETs in a leg and can be selected by appropriately choosing R_{DT}. The relation between the DT in [ns] and the resistance value in [kΩ] is: $DT = 10 \cdot R_{DT}$. To guarantee safe turn-on and -off margins, a DT of 1 μs is selected. Note that the impact of DT on the CL voltage waveform is limited as the operating PWM period is much larger (125 μs). On the output side, the gate resistor is 20 Ω. In addition, a 10 kΩ resistor is placed between the MOSFET's gate and source to avoid any undesired turn-on of the device when the driving signal is not present.

Pre-charge circuit: The built-in pre-charge circuit charges the SM capacitors to the desired voltage level at the start-up to ensure correct operation. The circuit is derived from the Cockcroft-Walton generator (CWG) [101] which is a voltage multiplier with diodes and capacitors arranged in such a manner that the capacitor charging occurs in multiple stages until the last capacitor is charged to the sum of all single capacitor voltages in the circuit.

The schematic of the pre-charge circuit is depicted in Figure (6.5). Using 15 V from one of the DC/DC converters and a transformer driver MAX 13256 IC, a 50% duty cycle ±15 V square wave voltage is obtained. A transformer isolates the CWG

from the power supply side. Current limiting resistors are placed to provide over-current protection for the MAX 13256 IC. The capacitors used are general purpose electrolytic. C_2, C_3 and C_4 have a value of 150 μF while C_1 has a higher value of 2200 μF to prevent damage due to reverse polarisation in case V_b is positive at the start-up. The diode D_5 is added to prevent current flow from the SM capacitor to the pre-charge circuit during normal operation. The enable signal for the pre-charge circuit is software-controlled, allowing the SM capacitors to charge to any desired voltage level between 0 and the 60 V theoretical maximum.

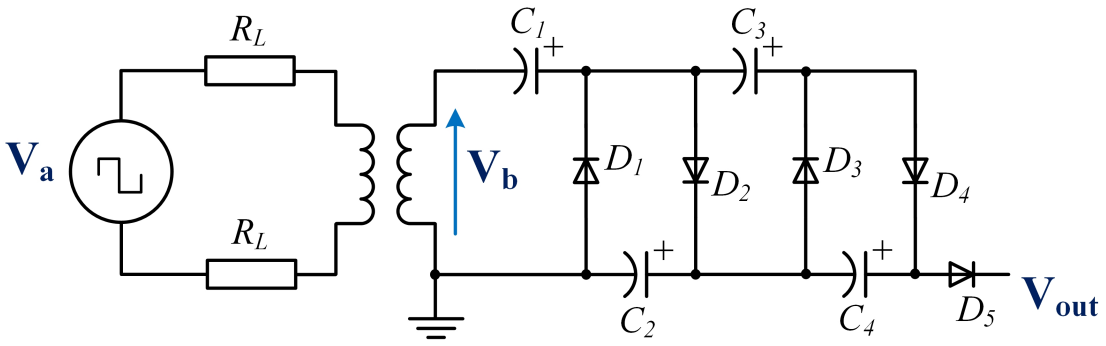


Figure 6.5: Built-in SM capacitor pre-charge circuit

Voltage sensing circuit: SM capacitor voltage measurement is necessary to determine the stored energy in the CLs and to implement the sorting algorithm. The SM PCB includes the low-cost built-in voltage sensing circuit shown in Figure (6.6), that uses a simple voltage divider circuit and a TI AMC1301 isolation amplifier with an input voltage range of $\pm$250 mV and a fixed amplifier gain of 8.2. The output of the amplifier is also compared to a predefined threshold to detect over-voltages in the SM. When an over-voltage occurs, a trip signal is transmitted to the local controller.

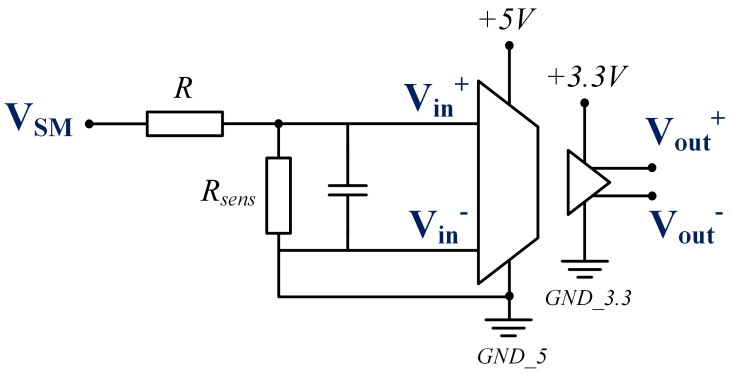


Figure 6.6: SM voltage sensing circuit based on the TI AMC1301 iso-amplifier

6.2.2.2 "Front-End" Half Bridge

In the SMPC, each converter phase-leg has director switches that are switched at the AC line frequency. In the experimental work, the implementation of these director switches is termed the "'Front-End" Half Bridge (FEHB)'. For the hardware implementation of the FEHB, the Dynex DIM400WHS17-A000 half-bridge IGBT module (Figure (6.7)) is used. Only one module per switch position of the FEHB is required because of the relatively low voltage and current ratings of the experimental prototype compared to the nominal rating of the half-bridge modules (1700V, 400A). However, in high-voltage implementations, multiple devices must be series connected to share the voltage.

Figure 6.7: Dynex DIM400WHS17-A000 half-bridge module

Three half-bridge modules are placed on an extruded aluminium heat sink inside an

enclosure as shown in Figure (6.8). Metal-oxide varistors (MOVs) are placed across each IGBT to protect them from damage in case of over-voltage events. The AC voltage is plugged into the FEHB through a three-phase socket at the rear side of the enclosure and the half-bridge terminals are connected to the front of the enclosure through H4 connectors.

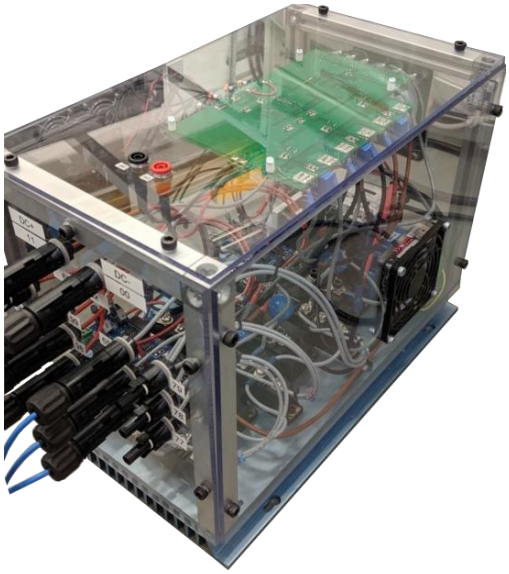


Figure 6.8: FEHB enclosure

In order to drive the IGBTs in the half-bridge modules, the gate driver circuit shown in Figure (6.9) is implemented. Each Dynex module has two switching devices and hence, the gate driver PCB includes two independent and isolated gate driver circuits. In total, three gate driver PCBs of Figure (6.11b) are employed in the FEHB. The digital signals received by the HFBR-2521 optical fibre receiver is passed through a Schmitt trigger buffer to obtain a signal between 0 V and 5 V depending on whether the digital signal is 0 or 1. The output of the Schmitt trigger is connected to the HCPL-3150 optocoupler to provide extra isolation between the signal circuit and the power circuit. A 390 Ω resistor is used to limit the current flow into the primary side LED of the optocoupler. The output of the optocoupler, that is connected between ± 15V, is then passed on to the IXDN609PI gate driver which is a high-speed high

current output driver that supplies a gate signal of ±15 V to the IGBT. 5 V are supplied from an external source to power the circuit, and the ± 15 V are obtained from the 5 V using the 2W Murata MGJ2D051515SC DC/DC converters.

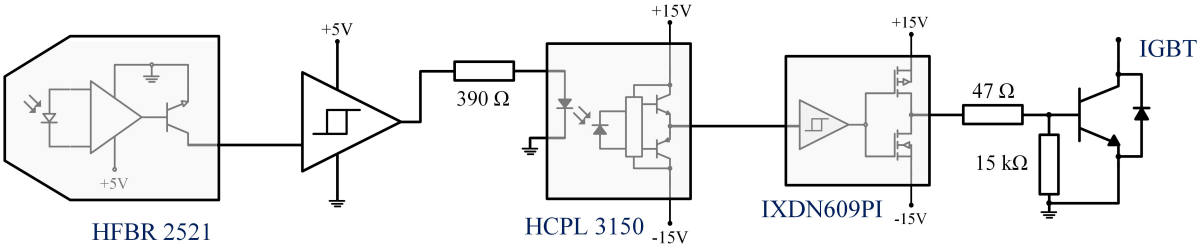


Figure 6.9: IGBT gate driver circuit

Only the digital signals for the high-side IGBTs in the half-bridge modules are sent from the controller along with a trip signal. A gate logic signal generator circuit depicted in Figure (6.10) is added that inverts the input gating signal to generate the gating signal for the low-side IGBTs, and in addition, implements the trip. Furthermore, it adds a delay to the rising edges of the gate signals using an RC circuit which is then shaped by a Schmitt trigger buffer to add dead-time between the upper and lower IGBTs of one half-bridge module. Figure (6.11a) shows the PCB that implements three gate logic signal generators of Figure (6.10). The outputs of this PCB are the inputs to the three gate driver PCBs of Figure (6.11b).

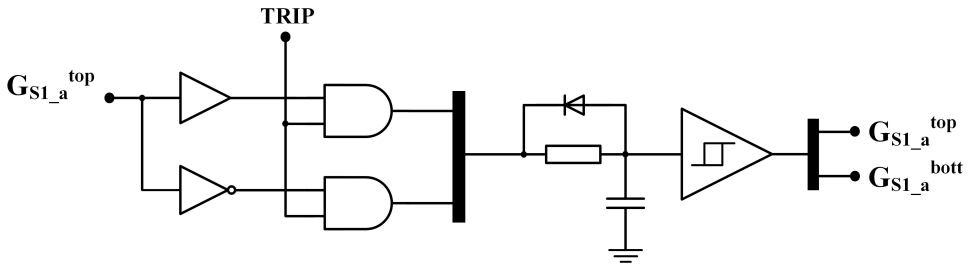
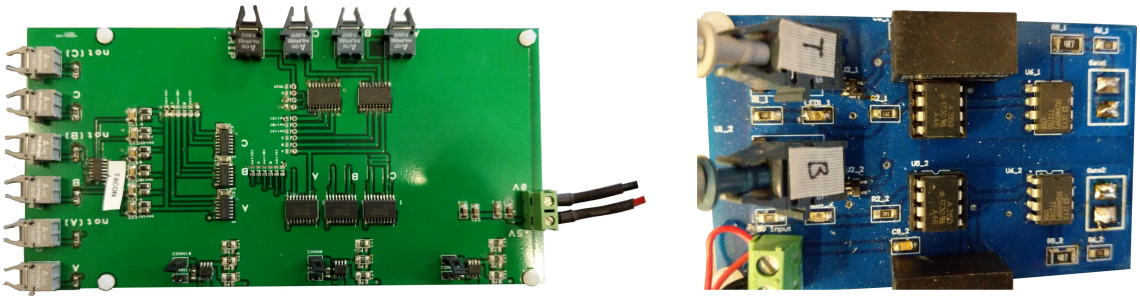


Figure 6.10: Gate logic signal generator



(a) (b)

Figure 6.11: (a) Gate logic signal generator PCB (b) FEHB gate driver PCB

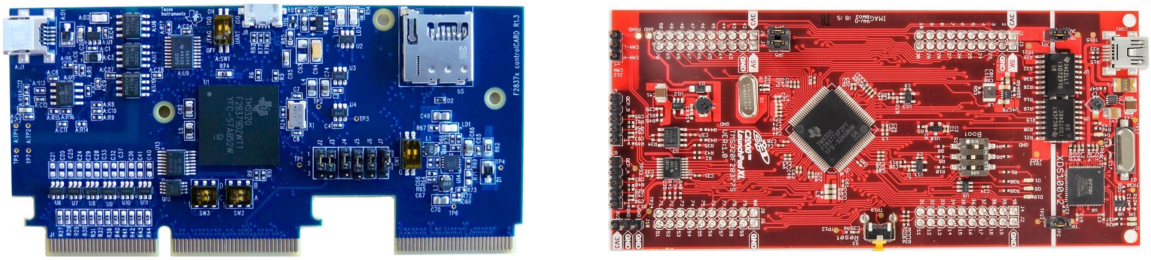
6.2.3 Prototype Control Structure

6.2.3.1 Control architecture

The control system in the prototype is based on low cost off-the-shelf micro-controller units (MCUs). In modular multilevel converters, the quantity of real time signals that need to be measured are significant (all SM voltages, plus converter terminal voltages and currents and arm currents etc.) and hence, the number of ADC channels in the control platform should be accordingly sufficient. However, it is difficult to find DSPs with more than 16 ADC channels. Therefore, a control structure based on a master-slave configuration is employed, where the slave controllers monitor all the SM voltages locally in each phase and only communicate the sum of the UPP, MID and LOW CL voltages to the master controllers, as they are sufficient for calculating the respective CL energies.

The MCUs used are the Texas Instruments F28379D and the F28377S for the master controller and the slave controllers respectively. The development boards housing the MCUs are the Delfino TMS320F28379D controlCARD for the master controller (shown in Figure (6.12a)) and the LAUNCHXL-F28377S LaunchPad for the slave controller (shown in Figure (6.12b)). The selections are based on the fulfillment of the following criteria:

- The slave controller should have at least eight ADC channels to monitor all of the SM voltages in a phase, a minimum of 12 PWM channels (4 for the HBs in the MID CL and 8 for the FBs in the UPP and LOW CLs) and a communication peripheral compatible with the master controller.
- The master controller should include at least 12 ADC channels (to monitor the three-phase AC currents and voltages and 6 arm currents) and 3 communication peripherals suitable for interfacing with the slave controllers.



(a) (b)

Figure 6.12: (a) TMS320F28379D controlCARD (b) LAUNCHXL-F28377S LaunchPad

Both the development boards include a XDS100 USB JTAG emulator that allows programming and debugging via USB. The USB interface also offers a serial connection between the MCU and the PC. The CPU core can run up to 200 MHz and on account of the additional Control Law Accelerator, the device is capable of achieving 400 MIPS (single core F28377S) and 800 MIPS (dual core F28379D).

The two MCUs feature a large number of individually programmable general-purpose input/output pins (GPIOs), communication peripherals such as three high-speed (up to 50MHz) serial peripheral interface (SPI) ports, four analog-to-digital converters (ADCs) in which up to 16 channels can be multiplexed in total and 24 PWM modules that can be operated synchronously. For detailed information about the available peripherals, the MCU datasheets ([102] [103]) and the technical reference manuals ([104][105]) can be referred.

The SPI is a synchronous data bus that establishes communication in full-duplex mode between two devices, using a master-slave architecture. In the experimental prototype, the SPI port is operated at 10 MHz. The master controller uses three separate SPI ports to communicate and each slave controller has its own dedicated communication link. In each communication, three 12-bit data streams are transmitted between the slave controllers and the master controller. The ADC module supports 12-bit or 16-bit resolution and comprises a sample & hold circuit. In this application, the 12-bit resolution has been selected and a software source enables the conversion. Each of the 24 enhanced PWM modules of the MCUs has a dedicated 16-bit counter with programmable period and source frequency control, which is configured in up-down mode for triangular carriers. Each module counter is continuously compared with the compare register of two channels A & B, producing two PWM outputs. In this application, the ePWM modules are used only in the slave controller MCUs and each SM is associated with an ePWM module.

The master-slave control structure employed in the experimental prototype is shown in Figure (6.13). The user can communicate with the master controller through the PC interface to specify system set-points. The task of the master controller is to implement the main control algorithms that use information acquired from the measurement boards (terminal voltages, currents and arm currents) via the ADCs and from the slave control boards (available CL voltages) to define the modulation references for the converter phases. It also handles the over-current and over-voltage system trips and controls the start of the interrupt routine of the slave controllers which is kept in reset status during start up. In addition, the gate signals for the FEHBs are directly sent by the master control board using appropriately configured GPIOs.

In the slave controller, during the interrupt routine, repetitive operations are performed which include the conversion of the local SM voltages, current sign detection in the CLs (using a sign detection circuit on the control platform) and calculation of the available CL voltages. In addition, the received modulation references from the

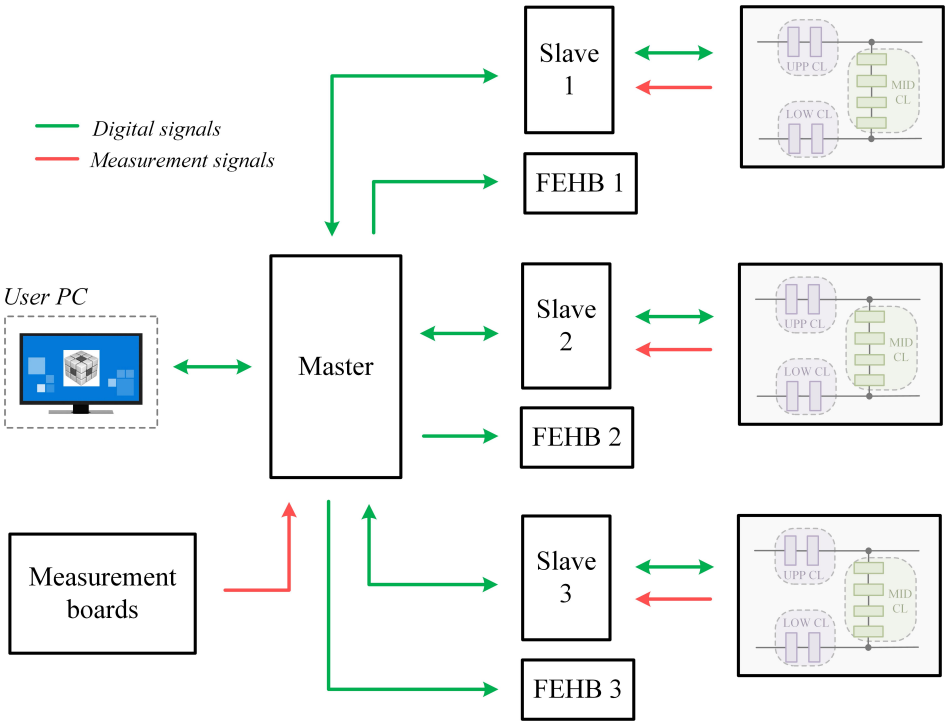


Figure 6.13: Master-slave control architecture

master controller are normalised according to the available CL voltages and shared among the SMs. Finally, within the same interrupt routine, the sorting of the SM insertion order is carried out and the PWM signals are generated.

6.2.3.2 Control interface boards

The control interface boards include the master interface PCB that houses the F28379D controlCARD, the backplane PCB that interfaces the SMs in the converter phase with the F28377S LaunchPad and the voltage and current measurement boards.

Master interface PCB: The master control board PCB with an expansion board mounted on top is shown in Figure (6.14). The controlCARD is connected to the board via a 180-pin edge connector. Twelve high-speed (up to 50 Mbd) AVAGO AFBR-1624 optic transmitters and AFBR-2624 receivers establish the SPI communication link with the slave controllers. In addition, the activation signal for the slave

controller interrupt routine and the trip communication from/to the master are also realised via optical transmitters/receivers, with the difference of the receiver in the trip communication being the inverting AFBR-2521. The current signals received from the measurement boards are first converted into voltages using a resistor and are then amplified via signal conditioning circuits, before then being connected to the input of the ADC channels. Trip circuits are implemented to check if the measured currents and voltages are within the acceptable margins and any trips are visually indicated by corresponding LEDs. A latch circuit keeps the LEDs on after a trip event until they are manually reset to help identify the cause of the trip. The expansion board, which is mounted on top of the master control board, is added to interface additional measurement inputs to the ADCs. The expansion board implements the same signal conditioning and trip circuits as the master control board. Lastly, an auxiliary board, which is also mounted on top of the master control board and is visible on the right corner in Figure (6.14), sends the gating and trip signals for the FEHBs using optic transmitters.

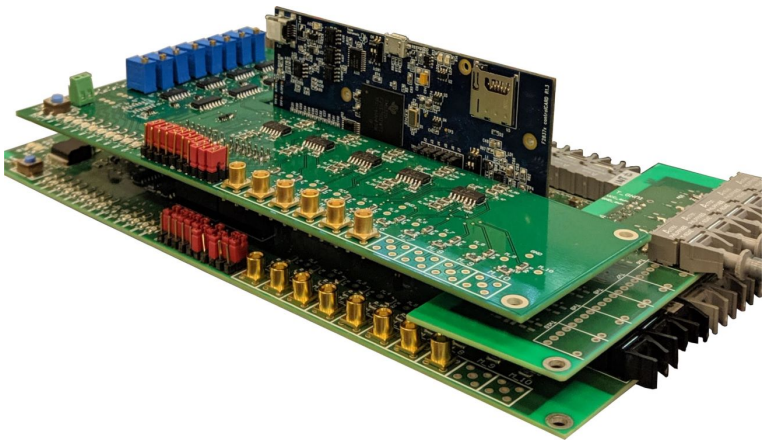


Figure 6.14: Master interface PCB with the expansion board mounted on top

Backplane PCB: The backplane PCB (shown in Figure (6.15)) mainly provides an interface between the F28377S LaunchPad and the SMs. The connectors on the SMs are plugged in at the rear of the backplane PCB enabling data transmission between the SMs and the local MCU. SM capacitor voltage measurements received

by the backplane are routed to the ADC channels through ADC filters. Further, the over-voltage trip signals from the SMs are fed into an AND logic gate, which outputs a digital '0' if at least one SM is in over-voltage. The output of the AND gate is connected to the RESET pin of the MCU, causing the slave controller MCU to automatically reset in an over-voltage event. The optical transmitters and receivers provide the optical communication link with the master controller, enabling the SPI communication. Moreover, the optical transmitters/receivers also allow the communication of other necessary information between the master controller and the slave controllers, such as the activation signal for the slave controller interrupt routine and the information on SM over-voltage trips.

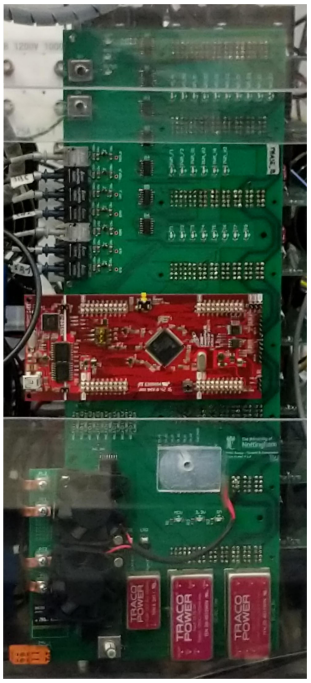


Figure 6.15: Backplane PCB

Information of the arm/CL current direction is essential for sorting the SM insertion indices in modular multilevel converters. A sign detection system is implemented directly on the backplane using a simple circuit shown in Figure (6.16). Two anti-parallel Schottky diodes are connected at the inputs of a comparator in a way that the conducting diodes alternate with the change in the current direction. When the current is positive, the lower diode conducts and the voltage drop across the diode is

sensed by the comparator, producing a '0' logic signal at the output. For a reverse current, a '1' logic is produced as the upper diode conducts. The output of the comparator is further connected to a dedicated GPIO of the MCU.

It needs to be mentioned that the SMPC has three CLs in a converter phase and the original backplane PCB had only two sign detection circuits. However, in the UPP/LOW CLs, it was observed that the effect of the balancing second harmonic addition on the CLs current is such that they are unidirectional for the major portion of the fundamental period and the current reversal occurs only for a very short duration. Since the power flow in the experimental application is unidirectional, it was concluded that sign detection for UPP/LOW CL currents is not required and only one sign detection circuit is used for the MID CL current. In practice, however, where the power flow is bidirectional and the P-Q operating range and system voltage levels are different, current sign detection for all the CLs would be required.

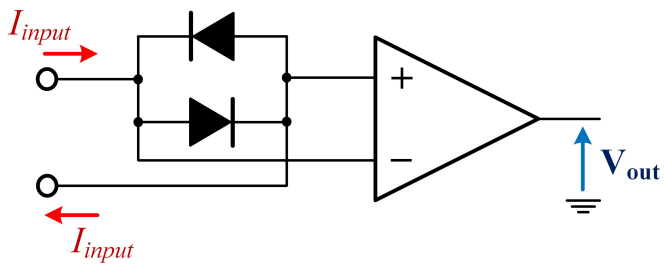


Figure 6.16: Sign detection circuit

Measurement boards: The external sensor requirements for the SMPC are 3 voltage sensors for the grid voltages and 9 current sensors for AC phase and arm currents. The pre-existing measurement board could host up to 10 voltage and 4 current transducers. For the arm current measurements, an additional measurement board with the capacity of measuring 8 currents has been constructed.

The sensors used are the Hall-effect based LEM LA 55-P current transducers and LEM LV 25-P voltage transducers. The LA 55-P has a nominal current of 50 A and outputs a current within a ± 50 mA range. The LV 25-P converts the measured

voltage into an input current using an internal resistor which is selected to keep the input current within the ±14 mA range. The input current is multiplied internally by a sensor gain of 2.5 to obtain the output current of the LV 25-P with a nominal value of 25 mA. The output currents of the transducers are converted into voltages via burden resistors on the master interface board, which are passed through signal conditioning circuits and then connected to the ADC channels of the master MCU.

6.2.3.3 Control software

For the correct operation of the converter prototype, it is essential to coordinate the execution of software instructions in both the master controller and the slave controllers. Hence, the interrupt routines of the two controllers should be synchronised and the code should be executed within the selected sample time ($T_s = 125\ \mu$s). The timing diagram of the master and slave interrupt routines is shown in Figure (6.17). The main steps are described below.

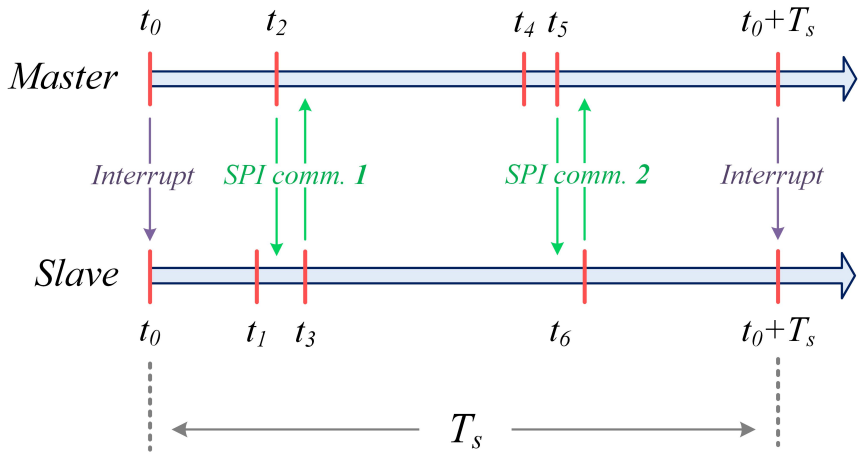


Figure 6.17: Master-slave code execution timing diagram

⇒ At t_0, the timer interrupt is initiated and the master controller transmits the interrupt routine activation signal to the slave controllers to synchronise the start of both interrupt routines. At this point, the slave controllers start the ADC conversion of the SM voltages. The master controller waits for the duration required for the slave

controllers to complete the conversion (t_1).

⇒ After the SM voltage conversion finishes at t_1, the master controller enables the SPI communication at t_2 to acquire the SM voltages. Also in the same communication, the master controller also sends the signals to enable the PWMs and the pre-charge circuit.

⇒ At t_3, the master controller receives the SM voltages from the slave controllers and obtains the readings from its ADC channels, after which the control algorithms are applied.

⇒ At t_4, the control implementation completes and the modulation references for the CLs are ready.

⇒ The second SPI communication starts at t_5 where the master controller sends the modulation references to the slave controllers.

⇒ After the slave controllers have received the modulation references at t_6, they implement the cell voltage ripple compensation, sharing, sorting and PWM generation. Since the SPI communication is always bi-directional, the slave controllers may be required by the master controller to send additional data in the second communication such as the SM voltage readings.

6.3 Control scheme modifications

As a result of using a resistive load instead of a voltage source on the DC side in the experimental setup, the original control scheme discussed in Chapter 5 has to be accordingly modified. The power flow is now unidirectional (AC to DC) with the converter acting as a rectifier.

The power demanded by the DC load is fixed as the converter is expected to source a

constant DC voltage on the load. Consequently, the DC side power can no longer be used as a control variable and the variable used to maintain global power balance in each phase is the AC power of the respective phase. Hence, the overall control scheme of the SMPC can be reconfigured such that instead of supplying an active power set-point externally, the active power reference is obtained from the output of the total energy controller. The modified control scheme, implemented in the experimental work, is shown in Figure (6.18). The control structures for the individual control loops are implemented in the same manner as discussed in Chapter 5.

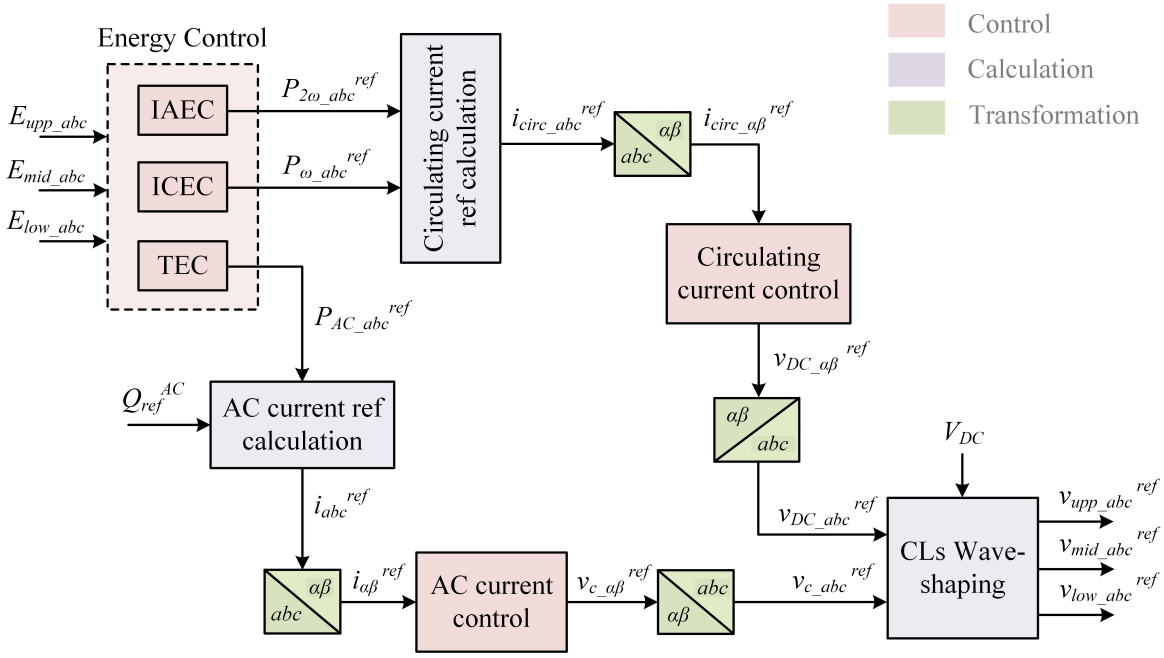


Figure 6.18: Control scheme for the SMPC experimental validation

Another slight change is the implementation of the circulating current loop in the α-β reference frame. This is because the measured circulating current in each phase-leg of the converter includes the DC current contribution of the respective phase-leg (in addition to the oscillatory components), but the controllers should not act on the DC current as it is drawn according to the load requirements. Therefore, the circulating current control is implemented in the α-β reference frame neglecting the zero-sequence component so that only the AC parts of the circulating current are

acted on by the control.

6.4 Summary

In this chapter, the experimental setup of a down-scaled laboratory prototype is presented. The prototype is a 3-phase converter with 8 SMs per phase, that can be flexibly configured to form different multilevel converter topologies. In addition, the FEHB enclosure, that implements the director switches of the SMPC, is also described. The design of the prototype control architecture based on the master-slave architecture is also presented, including an explanation of the interface boards for the master controller and the slave controllers. Moreover, the control software that interfaces the master controller and the slave controllers has also been discussed. Finally, some changes in the control strategy developed for the converter in Chapter 5 have been proposed to adapt it to the control needs of the experimental setup.

Chapter 7

Experimental results

7.1 Introduction

In this chapter, results from the experiment are presented with the prototype configured for the SMPC operation as a rectifier with a resistive load on the DC side, as explained in Chapter 6. Results from the experiment are presented to show the converter's performance both during steady-state and system transients.

The experimental tests are conducted to achieve the following goals:

- To validate the converter concept by presenting waveforms for steady-state operation of the converter
- To verify the proposed control scheme by showing results for the transient performance when the system is subjected to load and energy reference step changes
- To prove the optimum modulation index analysis of Section (4.5.4) by varying the operating modulation index of the converter and observing the change in the SM voltage ripple

7.2 Experimental system parameters

The parameters of the experimental system are summarised in Table (7.1). The converter is operated for 1.5 kW of active power transfer to a resistive load of 20 Ω on the DC side and a reactive power exchange of ± 600 VAr with the AC grid. It should be noted that the same ratio for $\frac{Q}{P} = 0.4$ is selected to maintain consistency with the initial medium-voltage system ratings defined for the converter analysis in Chapter 4. This ensures that the optimum modulation index analysis of Section (4.5.4) remains valid for the experimental work.

Experimental system parameters	
Active power	1.5 kW
Reactive power	± 600 VAr
AC voltage	140 V
DC voltage	175 V
SM nominal voltage	50 V
Number of cells (UPP CL)	2
Number of cells (MID CL)	4
Number of cells (LOW CL)	2
AC side inductor	1.69 mH
Arm inductor	4 mH
DC load	20 Ω
SM capacitance	5.28 mF
Control parameters	
PLL bandwidth	125 rad s^{-1}
AC current control bandwidth	2500 rad s^{-1}
TEC bandwidth	40 rad s^{-1}
IAEC bandwidth	13 rad s^{-1}
ICEC bandwidth	13 rad s^{-1}
CIRC current control bandwidth	2500 rad s^{-1}

Table 7.1: Experimental system and controller parameters

The constant DC voltage imposed across the load is 175 V. The AC grid voltage is

generated using a Chroma 61511 programmable three-phase AC power source. This allows the AC voltage to be precisely adjusted according to the optimum modulation index of $M = 0.84M_{ss} \approx 1.32$. Hence, the AC voltage level of the system is 140 V.

A simulation model for the same ratings as the experimental prototype is also implemented using the PLECS simulation package. The results from the simulation are the expected results against which the experimental results are compared. The simulation is built using ideal devices which leads to slight observable differences between the simulated and experimental waveforms, such as the less pronounced high-frequency switching noise in the simulation results when compared to the experimental results.

For recording the experimental data, two oscilloscopes have been used, namely the Tektronix MSO4054 with a 500 MHz bandwidth and the Tektronix MSO3014 with a 100MHz bandwidth. Both the oscilloscopes have a sample rate of 2.5 GS/s. In addition, for the acquisition of the SM voltages and the energy transients, the relevant data is stored in the RAM of the master MCU which is sampled at 2 kHz - a quarter of the switching frequency (8 kHz).

7.3 Steady-state results

Experimental results for the converter operation during steady state are presented in this section. Two sets of results are taken, one for the converter exchanging inductive reactive power with the AC source (Q =+600 VAr) and the other for the case of capacitive reactive power exchange (Q = -600 VAr). The active power transferred from the AC source to the load in both cases is 1.5 kW.

7.3.1 P = 1.5 kW, Q = 600 VAr

Figures (7.1) - (7.10) show the experimental results when the converter is operated at P = 1.5 kW, Q = +600 VAr, along with the simulation results for each set of

waveforms. It may be noted that the currents drawn from the AC supply in the experimental tests are slightly higher, when compared to AC side currents from the simulations, due to the converter losses that are not modelled in the simulation.

The converter AC output voltages (measured with respect to the AC grid neutral), AC side currents, DC voltage and DC current from the experiment are presented in Figures (7.1) and (7.3) and the same plots from the simulation are shown in Figures (7.2) and (7.4). It can be seen that the results from the experiment match those from the simulations. As expected, there is no observable lower order harmonic ripple in the DC current, demonstrating that the injected balancing second harmonic current, as discussed in Section (4.4), forms a balanced three-phase set (in ideal AC grid conditions) that cancels out on the DC side. Hence, the SMPC does not require bulky DC side filters.

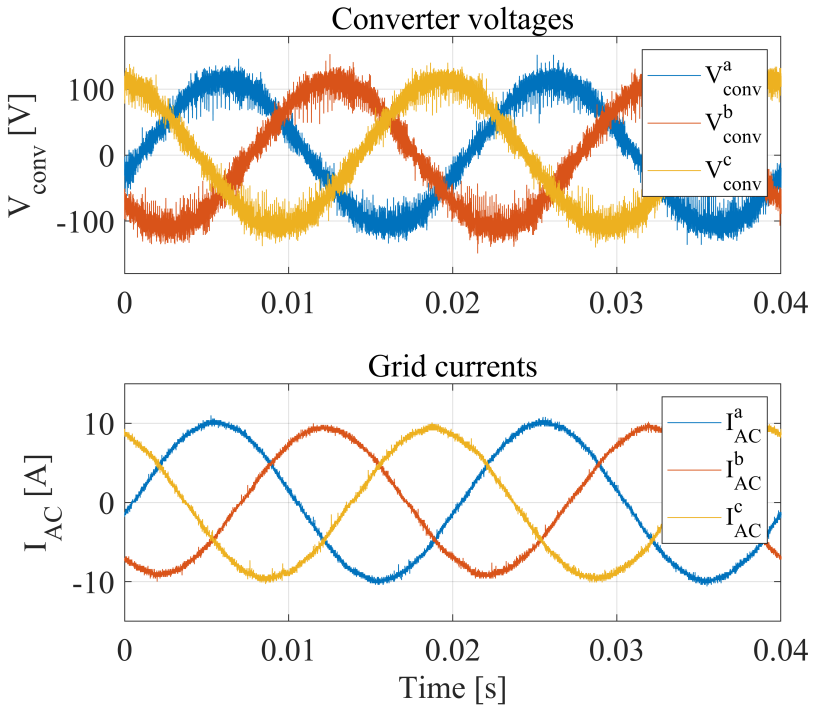


Figure 7.1: Experimental results for converter AC output voltages (top - data acquired using Tektronix MSO4054) and AC currents (bottom - data acquired using Tektronix MSO3014) at P = 1.5 kW, Q = 600 VAr

Figures (7.5) and (7.7) present the CL output voltages and the CL currents from

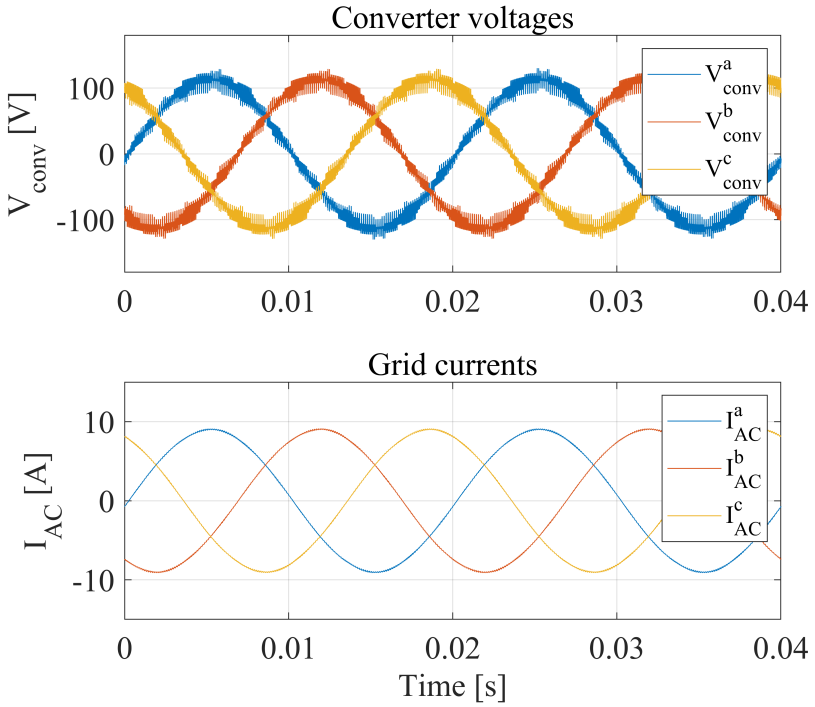


Figure 7.2: Simulation results for converter AC output voltages (top) and AC currents (bottom) at P = 1.5 kW, Q = 600 VAr

the experiment and Figures (7.6) and (7.8) show the same plots from the simulation. In addition to a good match between the simulated waveforms and the experimental waveforms, the results also confirm operation as expected from the analysis presented in Chapter 4 of this thesis. Figure (7.5) (LOW CL voltages are not included as they have the same waveforms as the UPP CL, except with a phase difference of π rads) verify the correct implementation of the selected waveshaping presented in Section (4.3). Looking at Phase a CL voltages (blue), it can be observed that the MID CL voltages are full-wave rectification of the converter AC voltages and the UPP CL voltages are inverted half-wave rectification of the converter AC voltages with an offset of $\frac{V_{dc}}{2}$. These voltage profiles are in accordance with the waveshaping discussion of Section (4.3).

In Figures (7.7) (LOW CL currents omitted for the same reason discussed above), the effect of the balancing second harmonic current can be seen in the UPP CL current waveshape. Moreover, the MID CL current can be noticed to have a fundamental

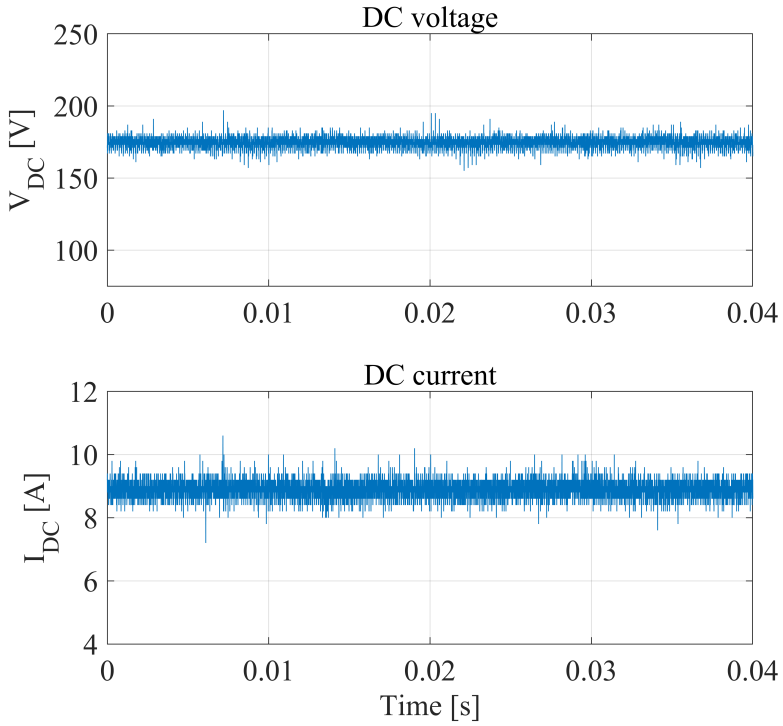


Figure 7.3: Experimental results for DC voltage (top - data acquired using Tektronix MSO4054) and DC current (bottom - data acquired using Tektronix MSO3014) at P = 1.5 kW, Q = 600 VAr

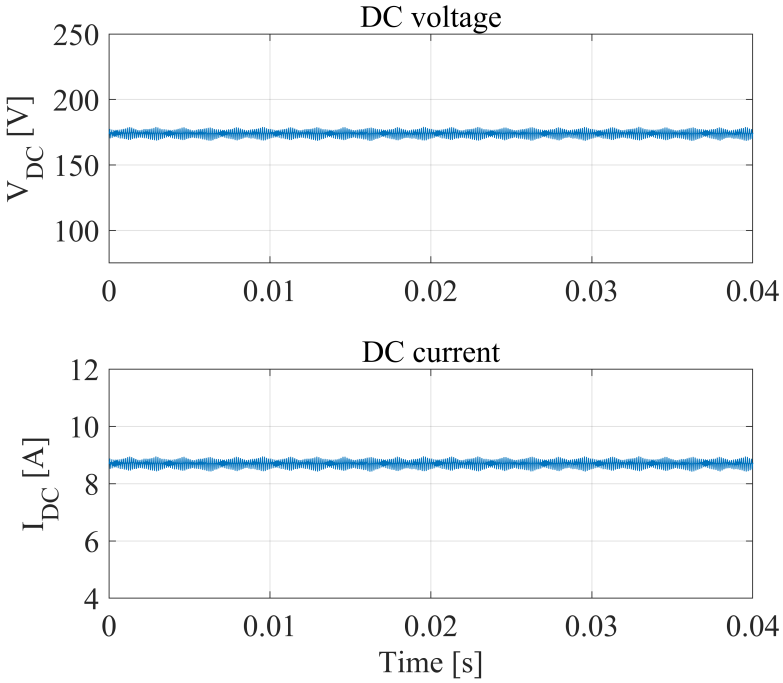


Figure 7.4: Simulation results for DC voltage (top) and DC current (bottom) at P = 1.5 kW, Q = 600 VAr

component at twice the AC frequency. This is also in accordance with the converter operation described in Chapter 4.

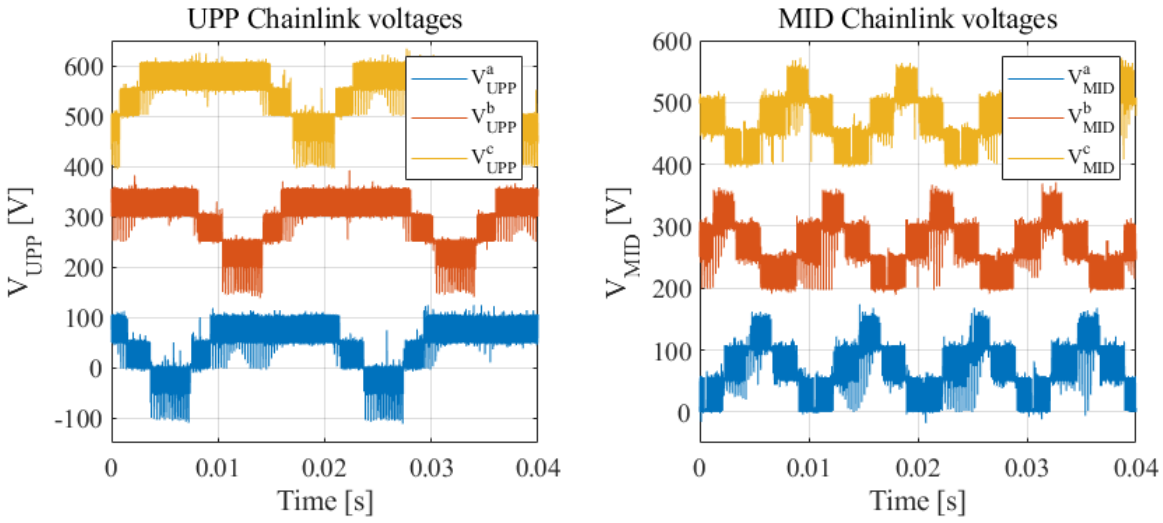


Figure 7.5: Experimental results for UPP CL voltages with offsets in Phases B & C (left) and MID CL voltages with offsets in Phases B & C (right) at P = 1.5 kW, Q = 600 VAr (Data acquired using Tektronix MSO4054)

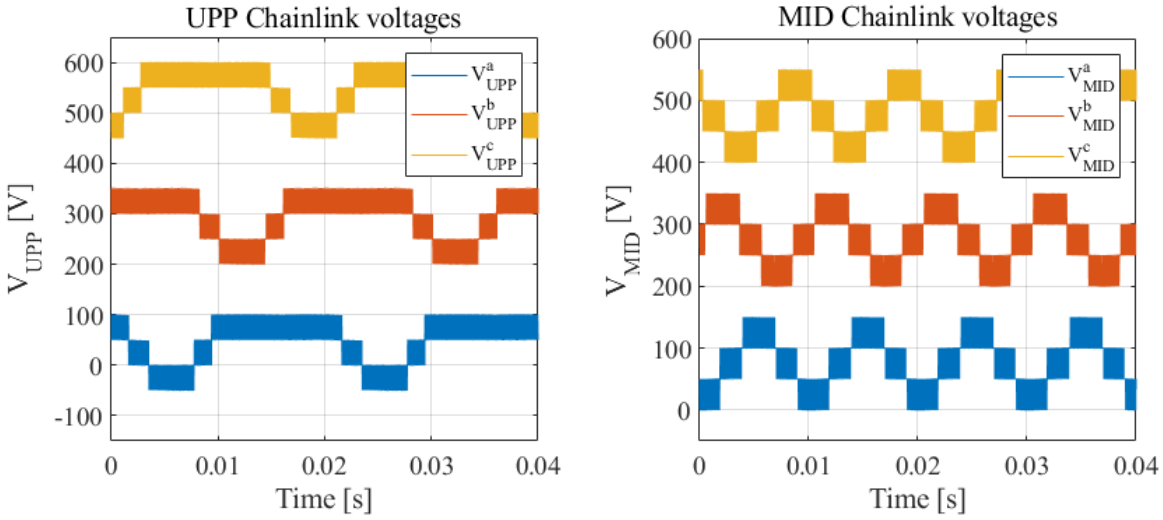


Figure 7.6: Simulation results for UPP CL voltage with offset in Phase B & C (left) and MID CL voltage with offset in Phase B & C (right) at P = 1.5 kW, Q = 600 VAr

Finally, to demonstrate the steady-state behaviour of the energy control loops, the SM voltages of Phase A from the experiment and the simulation are shown in Figures (7.9) and (7.10) respectively. The data for the experimental SM voltages is stored

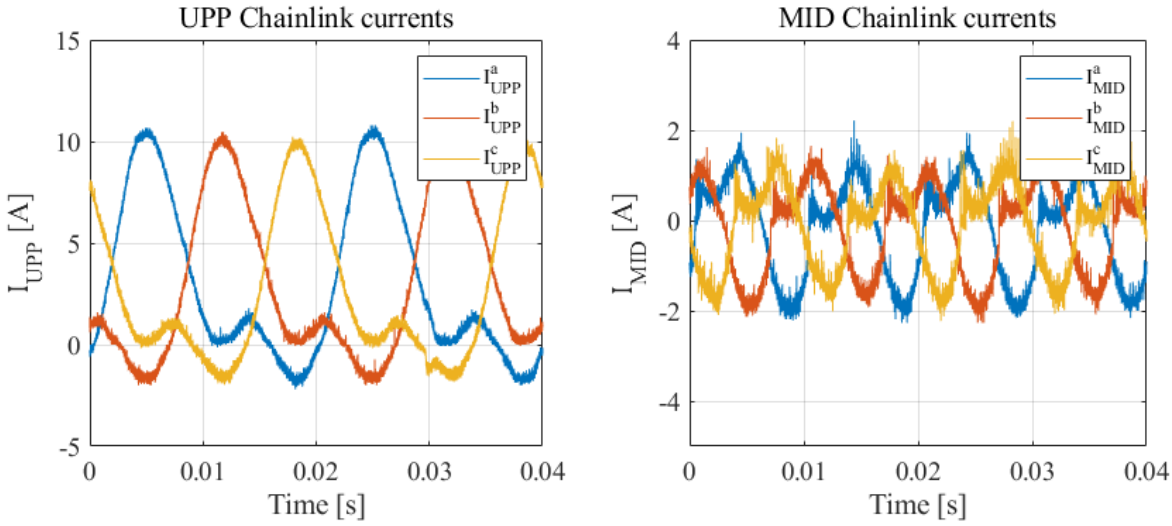


Figure 7.7: Experimental results for UPP CL current (left) and MID CL current (right) at P = 1.5 kW, Q = 600 VAr (Data acquired using Tektronix MSO3014)

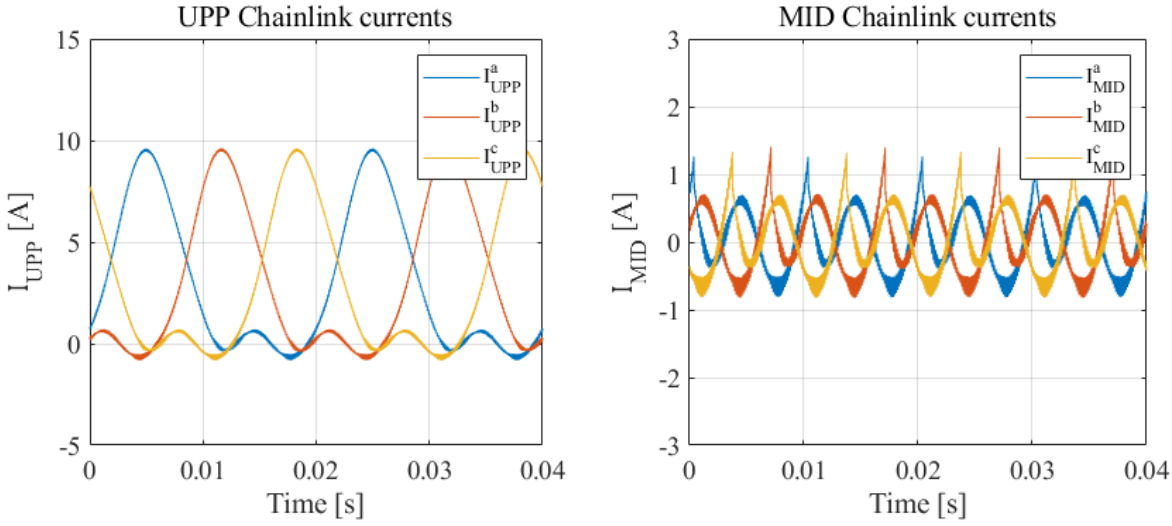


Figure 7.8: Simulation results for UPP CL current (left) and MID CL current (right) at P = 1.5 kW, Q = 600 VAr

in the RAM of the master controller MCU. It can be observed that the SM voltages are stable around the nominal SM voltage of 50 V.

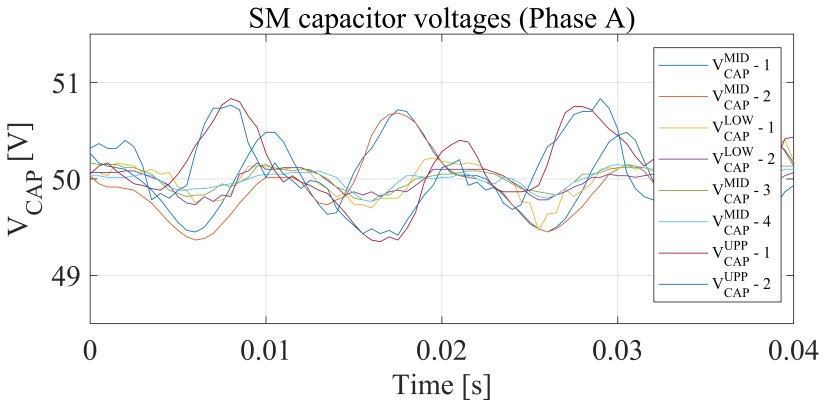


Figure 7.9: Experimental results for SM capacitor voltages in Phase A at P = 1.5 kW, Q = 600 VAr (Data stored in the master controller RAM)

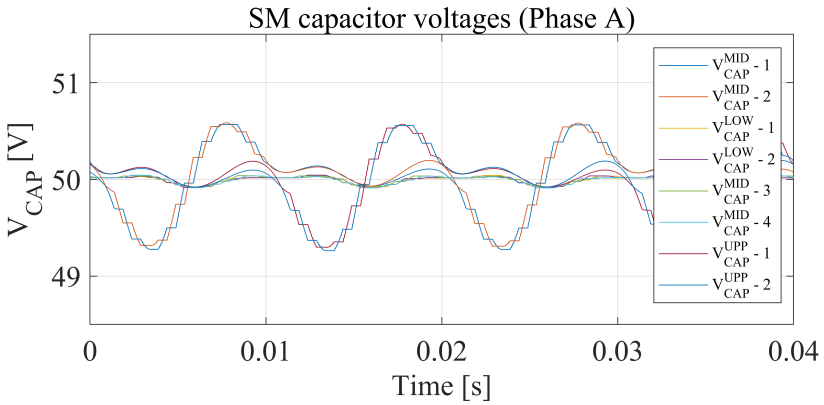


Figure 7.10: Simulation results for SM capacitor voltages in Phase A at P = 1.5 kW, Q = 600 VAr

Before the rest of the experimental results are presented, it should be mentioned that the purpose of presenting simulation results in this section is to provide references against which the experimental results can be compared. As can be seen from the above graphs, the experimental and simulation results match well. Therefore, in the rest of the chapter, the simulation results are omitted to avoid cluttering and only experimental results are shown.

7.3.2 P = 1.5 kW, Q= -600 VAr

Results from the experiment are now presented for a different operating point with the same active power transfer to the DC load, but with capacitive reactive power exchange with the AC source.

Similar to the previous sub-section, the converter AC output voltages, AC side currents, DC voltage and DC current from the experiment are presented in Figures (7.11) and (7.12). Figures (7.13) and (7.14) present the CL output voltages and the CL currents. Lastly, the SM voltages for Phase A are shown in Figure (7.15). The graphs show that the converter operation at a different operating point is again as expected from the analysis. The implementation of the CL voltage waveshaping is correct also in this case. The CL current wave profiles match those from the previous case with inductive reactive power, except with different oscillatory components due to the reactive power being capacitive. Finally, the SM voltages can be seen to be stable around the nominal value.

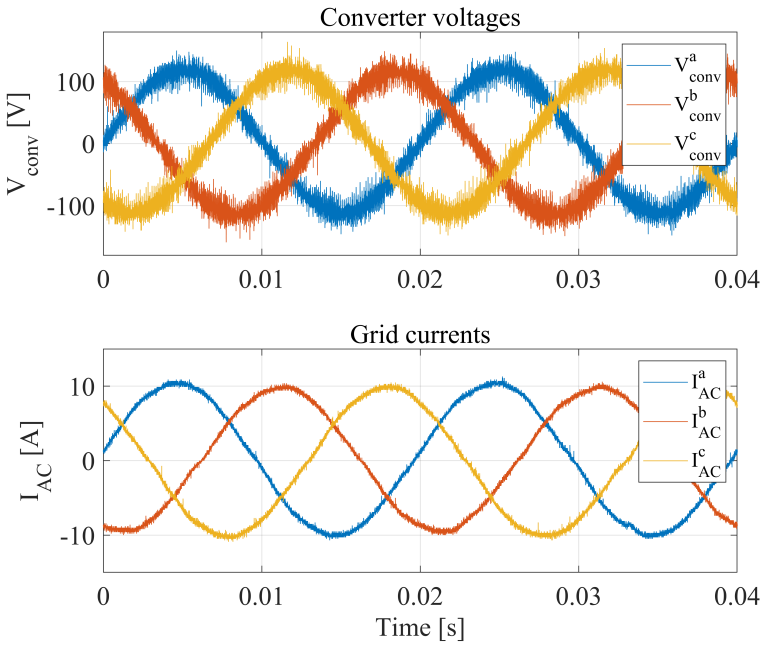


Figure 7.11: Experimental results for converter AC output voltages (top - data acquired using Tektronix MSO4054) and AC currents (bottom - data acquired using Tektronix MSO3014) at P = 1.5 kW, Q = -600 VAr

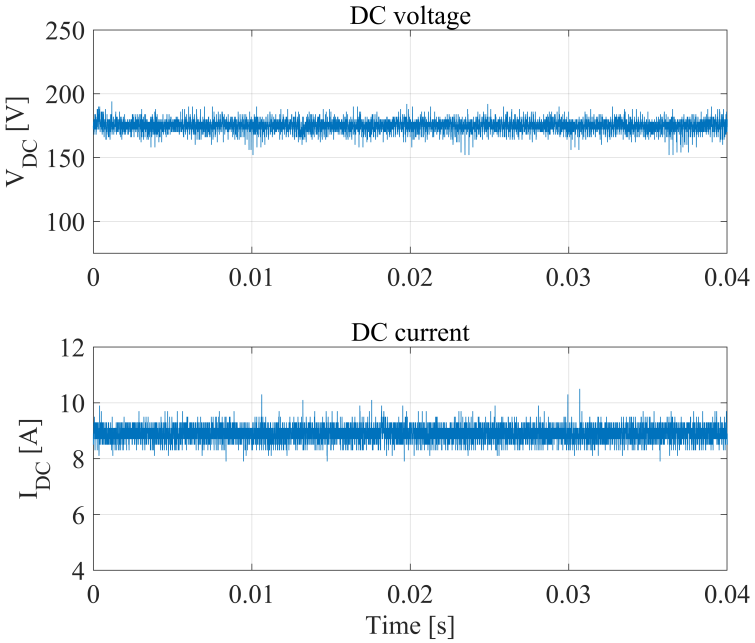


Figure 7.12: Experimental results for DC voltage (top - data acquired using Tektronix MSO4054) and DC current (bottom - data acquired using Tektronix MSO3014) at P = 1.5 kW, Q = -600 VAr

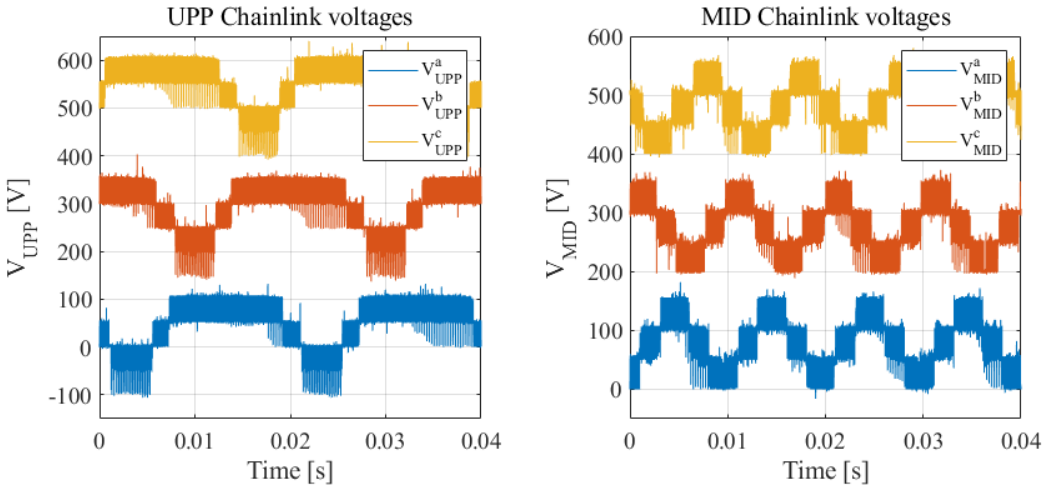


Figure 7.13: Experimental results for UPP CL voltages with offsets in Phases B & C (left) and MID CL voltages with offsets in Phases B & C (right) at P = 1.5 kW, Q = -600 VAr (Data acquired using Tektronix MSO4054)

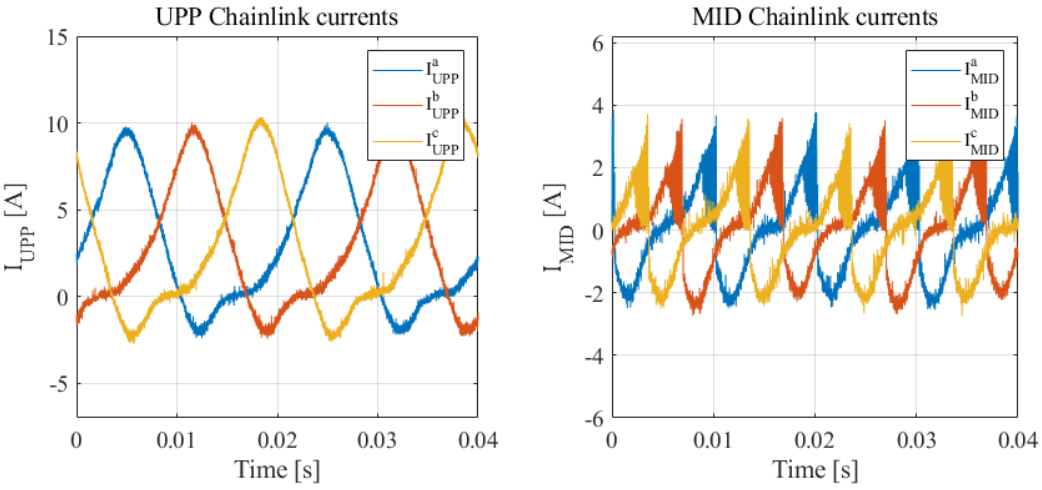


Figure 7.14: Experimental results for UPP CL current (left) and MID CL current (right) at P = 1.5 kW, Q = -600 VAr (Data acquired using Tektronix MSO3014)

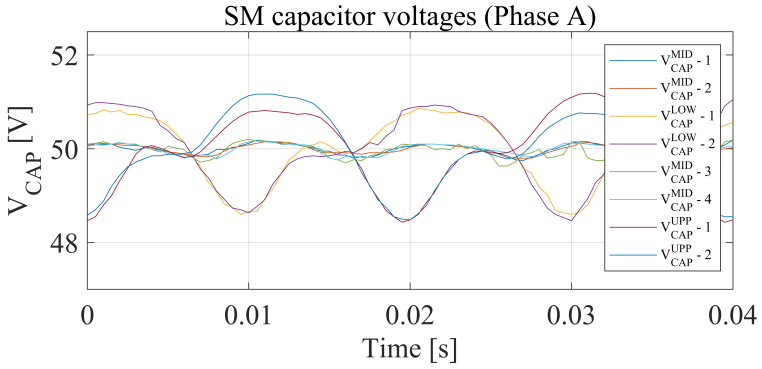


Figure 7.15: Experimental results for SM capacitor voltages in Phase A at P = 1.5 kW, Q = -600 VAr (Data stored in the master controller RAM)

7.4 Transient response

Experimental results for the transient response of the controllers are shown in this section. The tests performed include step variations in the DC load and the nominal energy reference of the CLs.

7.4.1 Load step response

For the load step response test, an electronically switched resistor bench is used that is optically controlled by the master MCU. The desired resistance can be formed by connecting or disconnecting resistors via optic signals, thereby achieving the required load configuration.

During the test, a 50 % step increase in the load is made. The initial DC load of 20 Ω, resulting in an active power transfer of 1.5 kW, is stepped up to 30 Ω reducing the active power to 1 kW. Two sets of results are taken for Q = 600 VAr and Q = -600 VAr.

For the load step test for positive Q, Figures (7.16) and (7.18) show the response of the AC current control loop and the DC current response respectively. A zoom of the AC current loop response is shown in Figure (7.17) around the time instants when the step is applied. In Figure (7.19), the individual CL energies are shown. Similarly, the results from the load power test for negative Q are presented in Figures (7.20), (7.21) and (7.22) showing the response of the AC current loop, DC current response and the CL energies respectively.

By observing the figures, it can be appreciated that the AC current control effectively tracks any changes in the current demand. Moreover, the response of the energy controllers matches with the energy control design of Chapter 5, showing that the individual CL energies return to their reference values within 0.4s-0.5s.

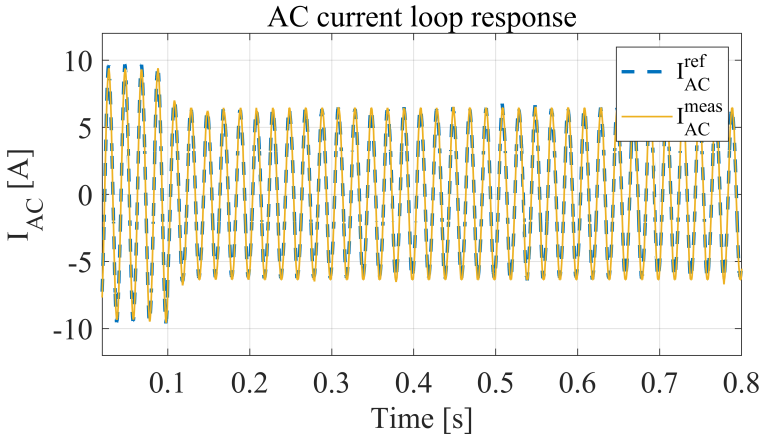


Figure 7.16: AC current loop response for a load step increase of 50 % at Q = 600 VAr (Data acquired using Tektronix MSO3014)

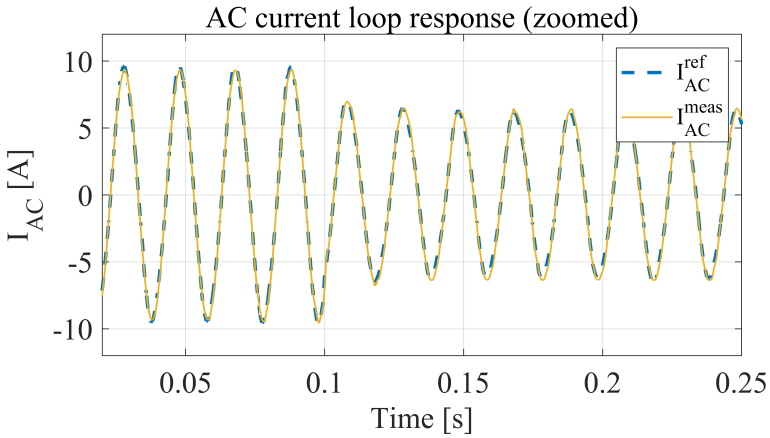


Figure 7.17: Zoom of the AC current loop response of Figure (7.16) around the time instants when the step is applied

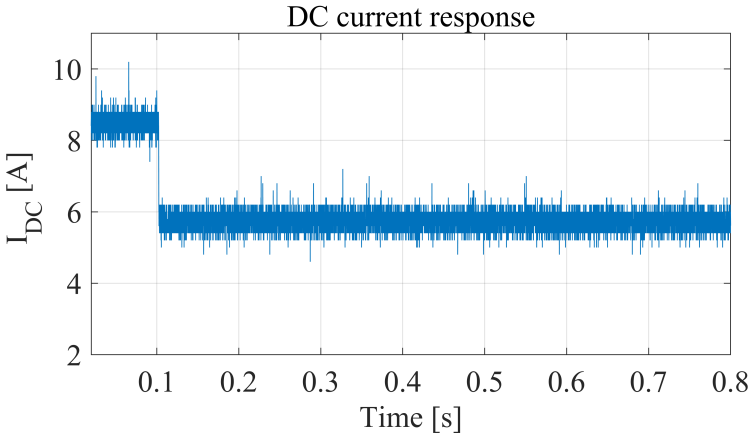


Figure 7.18: DC current response for a load step increase of 50 % at Q = 600 VAr (Data acquired using Tektronix MSO3014)

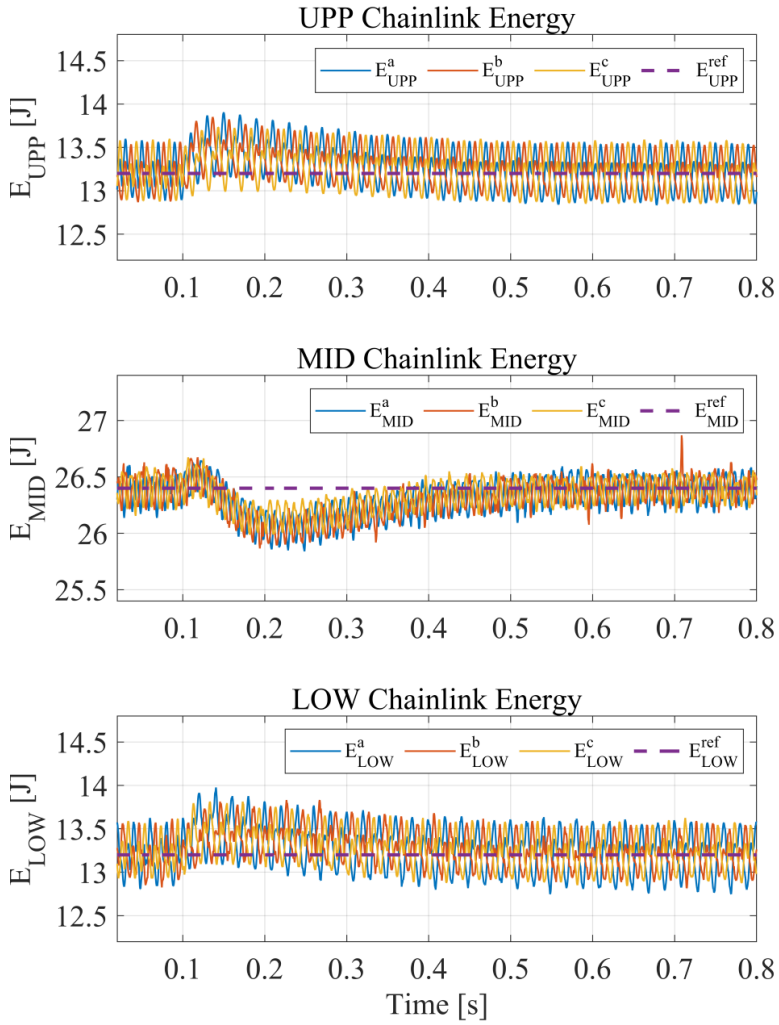


Figure 7.19: Individual CL energies demonstrating the response of the energy controller for a load step increase of 50 % at Q = 600 VAr (Data stored in the master MCU)

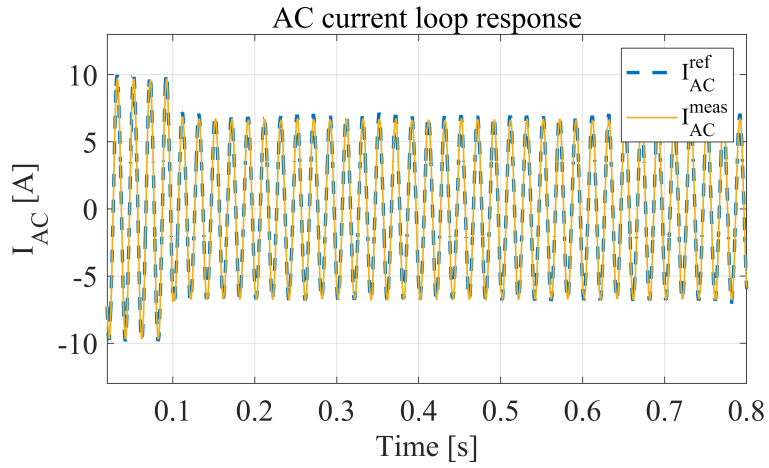


Figure 7.20: AC current loop response for a load step increase of 50 % at Q = -600 VAr (Data acquired using Tektronix MSO3014)

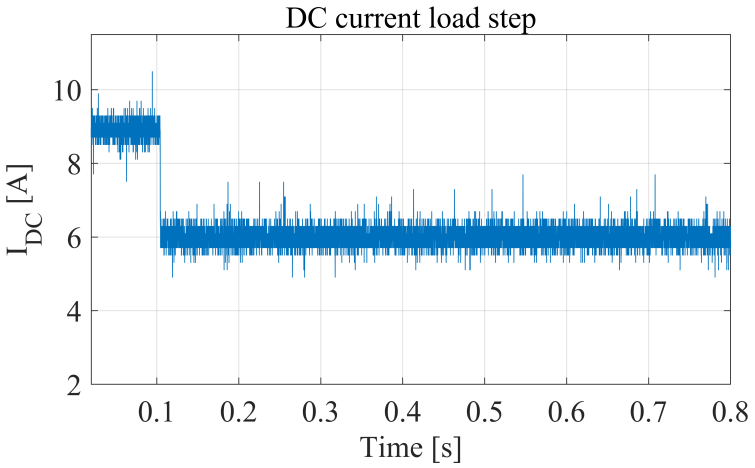


Figure 7.21: DC current response for a load step increase of 50 % at Q = -600 VAr (Data acquired using Tektronix MSO3014)

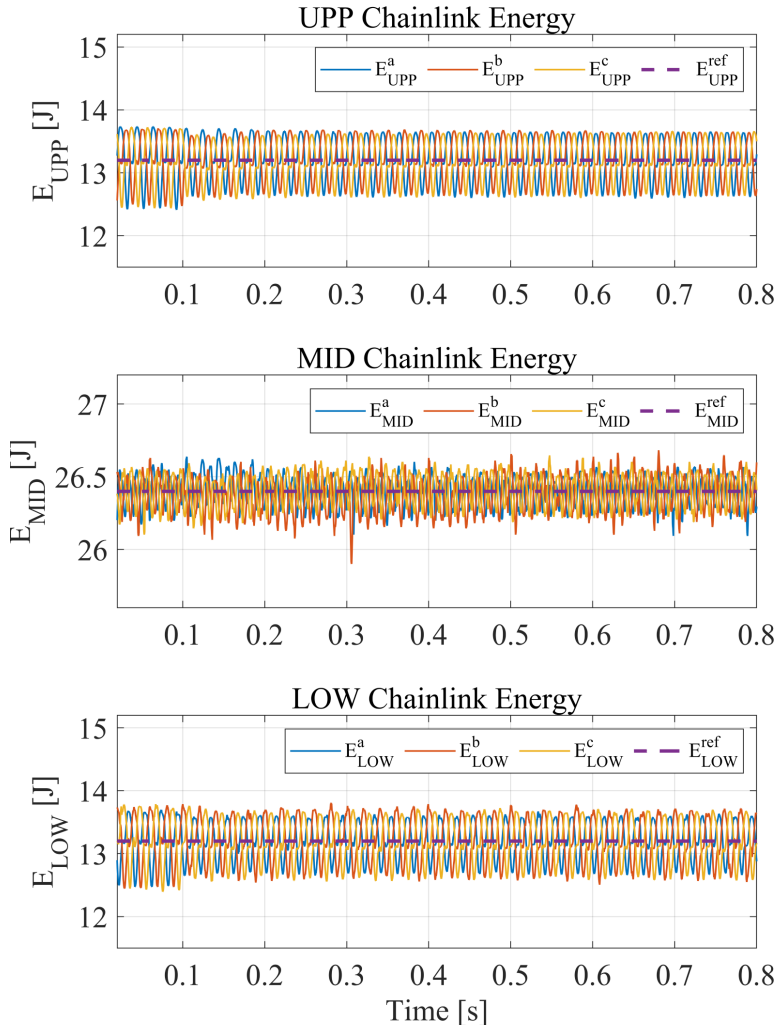


Figure 7.22: Individual CL energies demonstrating the response of the energy controller for a load step increase of 50 % at Q = -600 VAr (Data stored in the master MCU)

7.4.2 Energy step response

To further show the performance of the controllers, tests are performed for a 6 % step variation in the energy references of the CLs. In practice, this is implemented by changing the nominal SM voltage value from 50 V to 53 V. Two sets of results are taken for P =1.5 kW, Q = 600 VAr & P = 1.5 kW, Q = -600 VAr. These results are shown in Figures (7.23) and (7.24). The results show that the individual CL energies become stable around the new respective reference energy values within 0.4s-0.5 s.

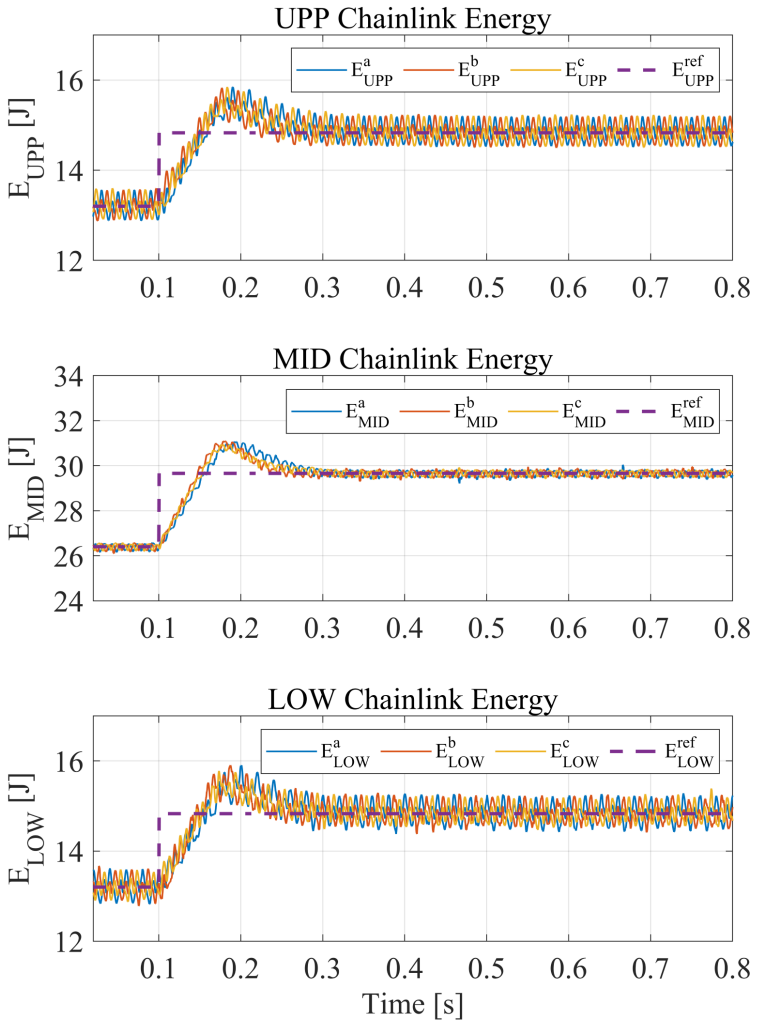


Figure 7.23: Individual CL energies demonstrating the response of the energy controller for an energy reference step increase of 6 % at P = 1.5 kW, Q = 600 VAr (Data stored in the master MCU)

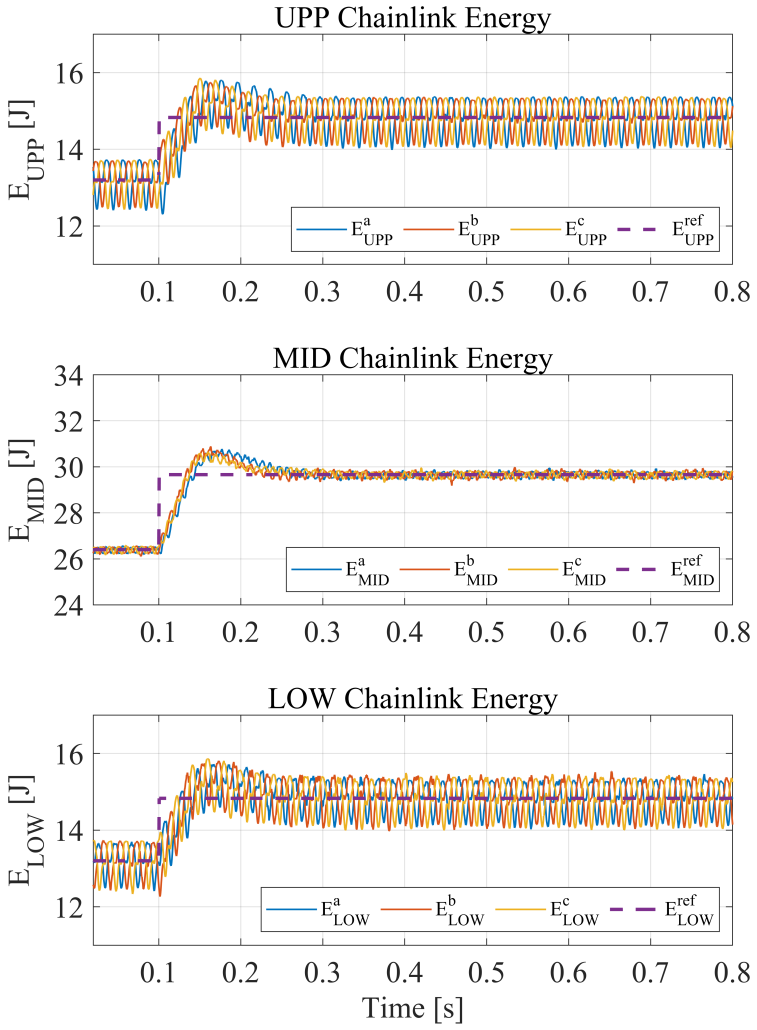


Figure 7.24: Individual CL energies demonstrating the response of the energy controller for an energy reference step increase of 6 % at P = 1.5 kW, Q = -600 VAr (Data stored in the master MCU)

7.5 Modulation index variation

In this section, experimental results for variations in the modulation index of the converter are presented with the goal of verifying the modulation index optimisation method introduced in Section (4.5.4). It can be recalled that the optimum modulation index is $M_{opt} = 0.84M_{ss} \approx 1.32$ when all FBs are used in the UPP/LOW CLs and the ratio of reactive power to active power ($\frac{Q}{P}$) is 0.4, which are the cases in the

experiment. At M_{opt}, the converter has the lowest energy storage value.

Experimental tests are conducted for different modulation index values, both below and above M_{opt}. The capacitor sizes and the number of SMs in the experimental setup are fixed, resulting in a fixed energy storage. With a fixed energy storage, it can be assumed that any changes in the energy pulsation of the CLs will manifest in the SM voltage ripple. Thus, the variation in the SM voltage ripple at different modulation indexes is used as an alternative to energy storage to verify the results of the optimum modulation index analysis with reasonable accuracy. The tests conducted are only for a single P-Q operating point i.e. P = 1.5 kW, Q = -600 VAr (capacitive).

Figures (7.25) - (7.33) show experimental results for operation at modulation indexes away from M_{opt} followed by the SM voltages for all cases with the ripple measurements marked. The results have been taken for four different M values i.e. $M = 1.16M_{opt} \approx 1.54$, $M = 1.38M_{opt} \approx 1.82$, $M = 0.84M_{opt} \approx 1.11$ and $M = 0.75M_{opt} \approx 1.0$. Two of the M values are above M_{opt} and the other two are below M_{opt}. Differences in the CL voltages and CL currents between results for different M values can be observed in Figures (7.25) - (7.28).

The SM voltage ripple in Phase a for the converter operating at the optimum modulation index M_{opt}, is presented in Figure (7.29) and shows a voltage ripple of 2.67 V. For the other M values away from M_{opt}, the SM voltage ripple in Phase A are shown in Figures (7.30) - (7.33). It is obvious from these figures that the lowest SM voltage ripple is at M_{opt} and operating away from M_{opt} on either side leads to an increase in the SM voltage ripple.

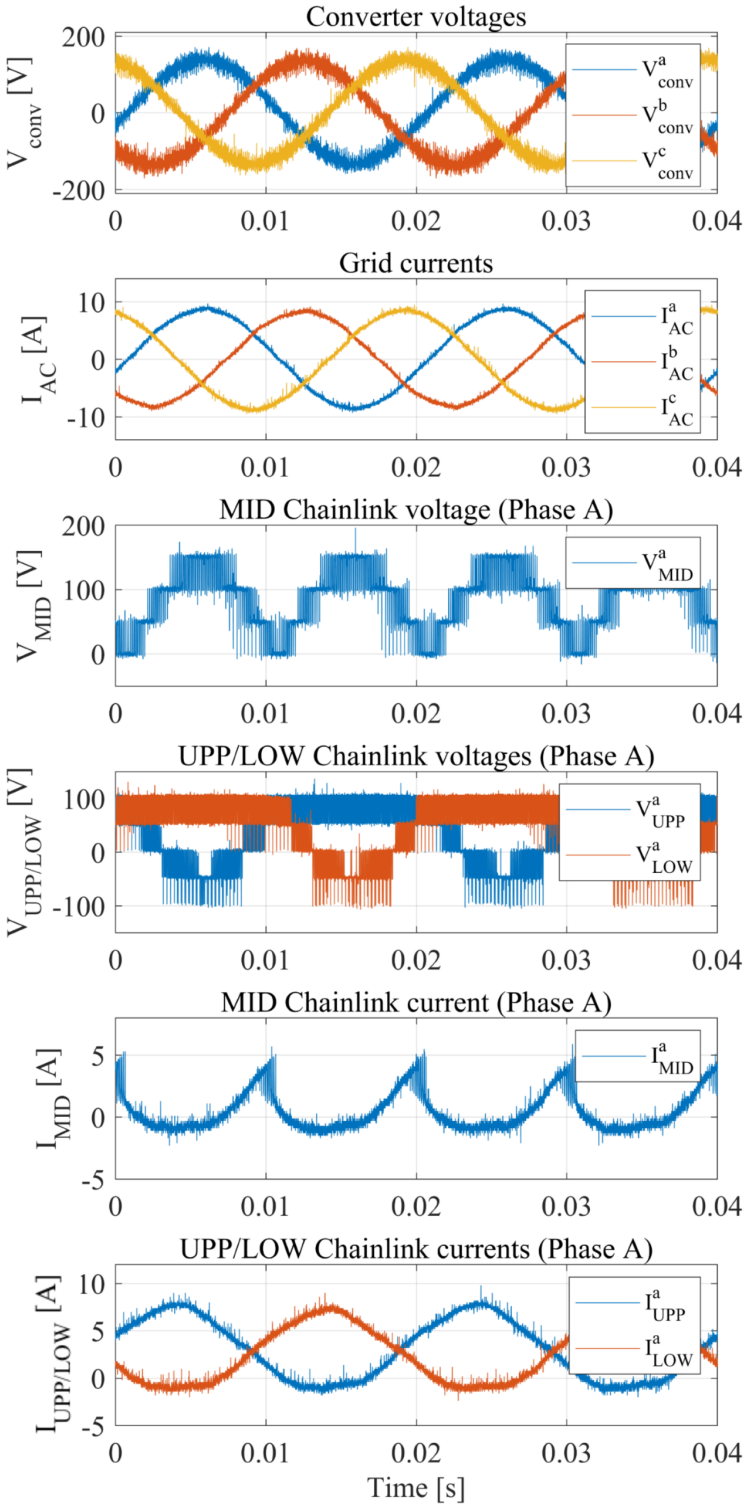


Figure 7.25: Experimental results at P = 1.5 kW, Q = -600 VAr operating at $\boldsymbol{M = 1.16 M_{opt} \approx 1.54}$ (Voltages data acquired using Tektronix MSO 4054, currents data acquired using Tektronix MSO 3014). Counting from top to bottom: (1) Converter AC output voltages (2) AC grid currents (3) MID CL voltage (Phase A) (4) UPP/LOW CL voltages (Phase A) (5) MID CL current (Phase A) (6) UPP/LOW CL currents (Phase A)

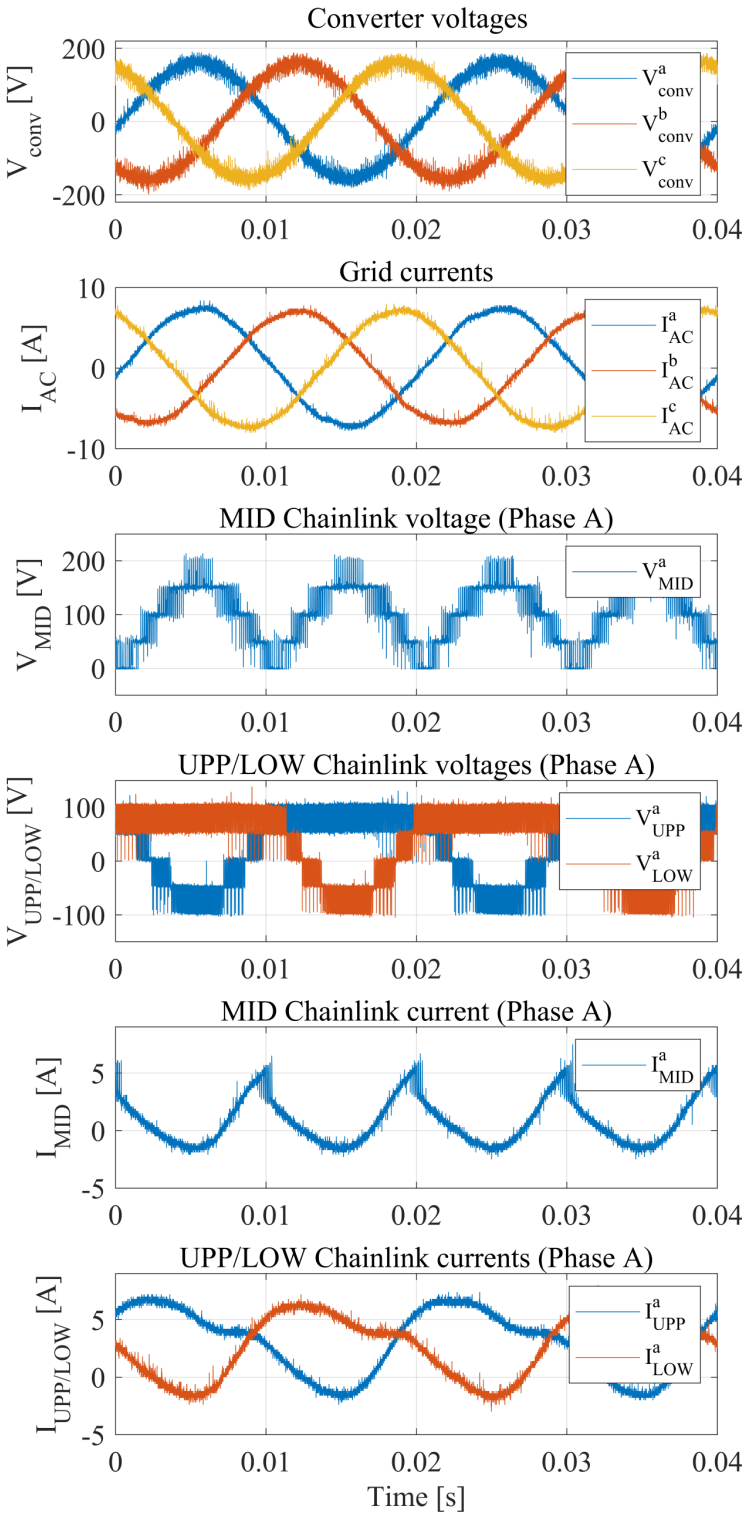


Figure 7.26: Experimental results at P = 1.5 kW, Q = -600 VAr operating at $\boldsymbol{M = 1.38 M_{opt} \approx 1.82}$ (Voltages data acquired using Tektronix MSO 4054, currents data acquired using Tektronix MSO 3014). Counting from top to bottom: (1) Converter AC output voltages (2) AC grid currents (3) MID CL voltage (Phase A) (4) UPP/LOW CL voltages (Phase A) (5) MID CL current (Phase A) (6) UPP/LOW CL currents (Phase A)

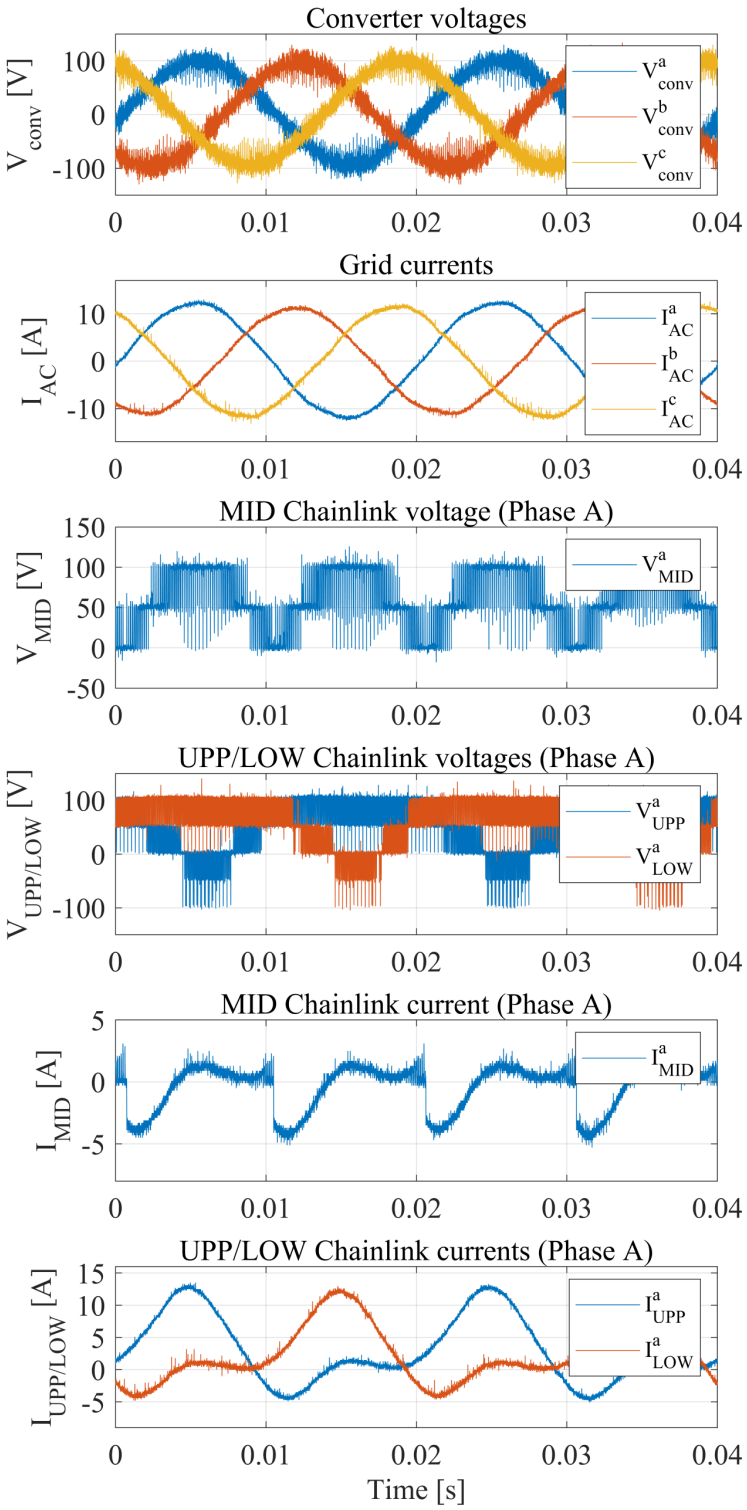


Figure 7.27: Experimental results at P = 1.5 kW, Q = -600 VAr operating at $\boldsymbol{M = 0.84M_{opt} \approx 1.11}$ (Voltages data acquired using Tektronix MSO 4054, currents data acquired using Tektronix MSO 3014). Counting from top to bottom: (1) Converter AC output voltages (2) AC grid currents (3) MID CL voltage (Phase A) (4) UPP/LOW CL voltages (Phase A) (5) MID CL current (Phase A) (6) UPP/LOW CL currents (Phase A)

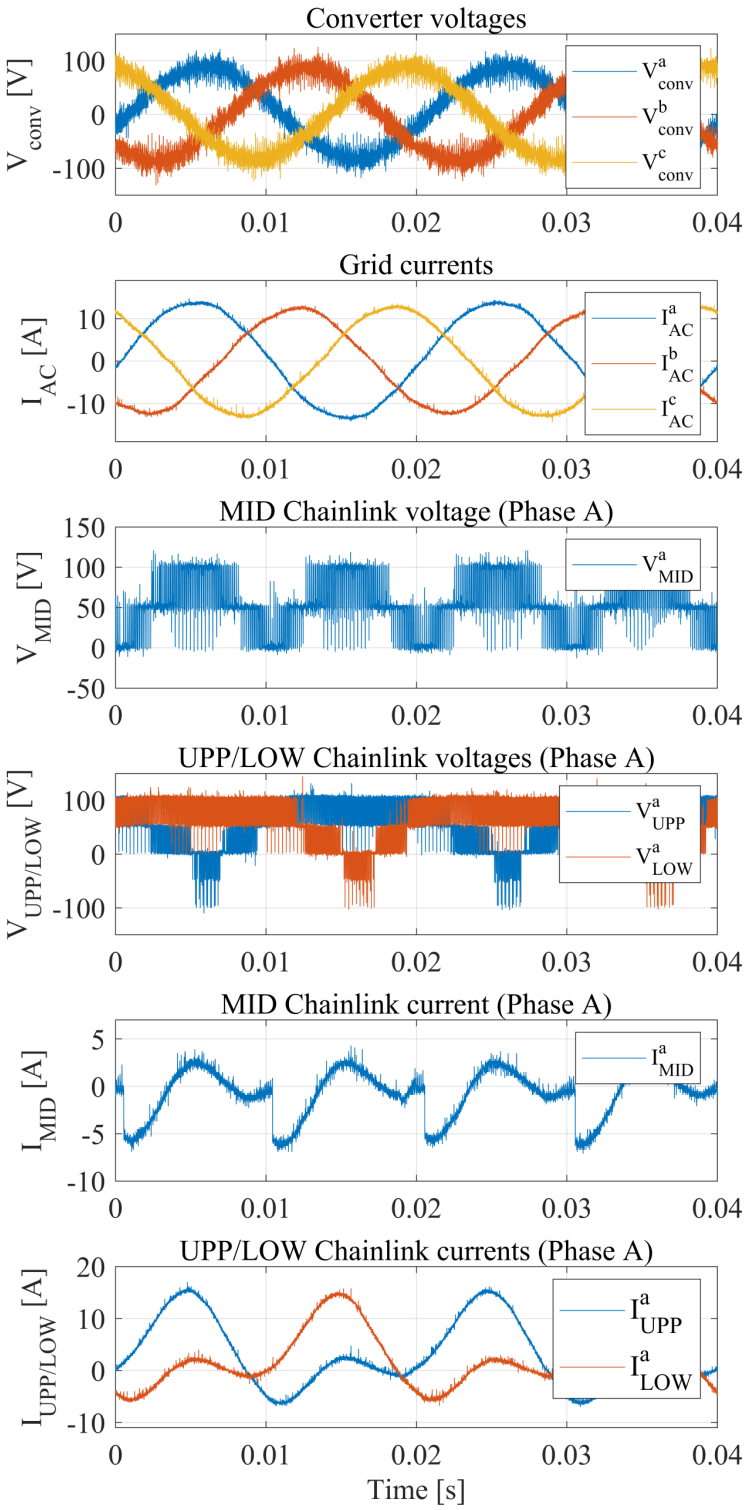


Figure 7.28: Experimental results at P = 1.5 kW, Q = -600 VAr operating at $\boldsymbol{M = 0.75M_{opt} \approx 1.0}$ (Voltages data acquired using Tektronix MSO 4054, currents data acquired using Tektronix MSO 3014). Counting from top to bottom: (1) Converter AC output voltages (2) AC grid currents (3) MID CL voltage (Phase A) (4) UPP/LOW CL voltages (Phase A) (5) MID CL current (Phase A) (6) UPP/LOW CL currents (Phase A)

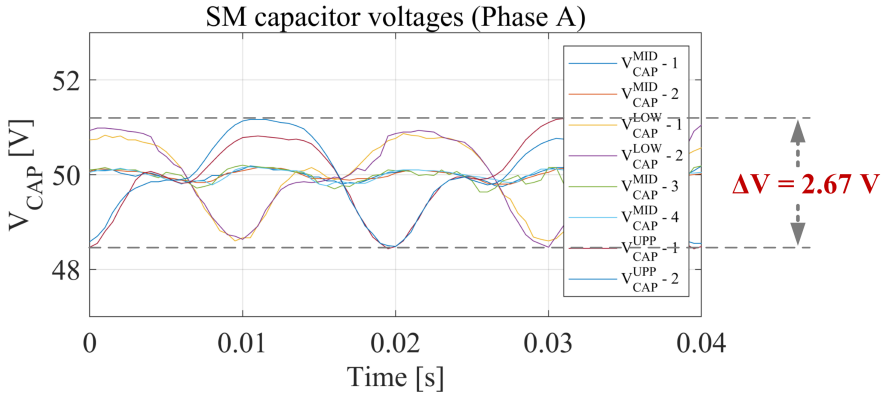


Figure 7.29: SM capacitor voltages in Phase A at P = 1.5 kW, Q = -600 VAr operating at $\boldsymbol{M = M_{opt} \approx 1.32}$ (Data stored in the master controller RAM)

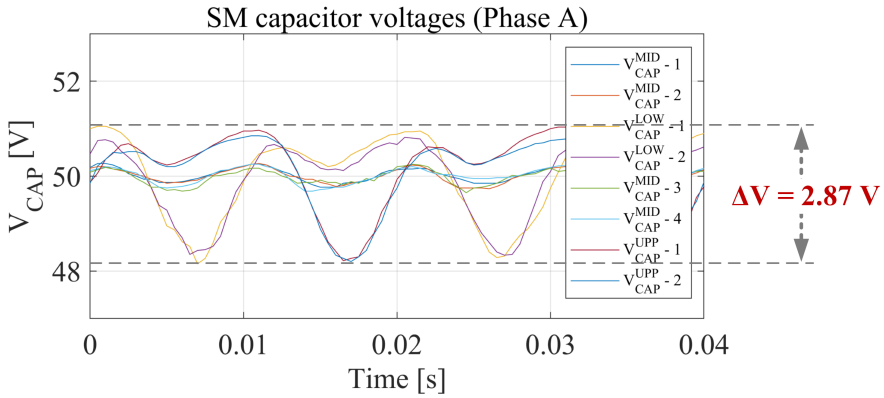


Figure 7.30: SM capacitor voltages in Phase A at P = 1.5 kW, Q = -600 VAr operating at $\boldsymbol{M = 1.16 M_{opt} \approx 1.54}$ (Data stored in the master controller RAM)

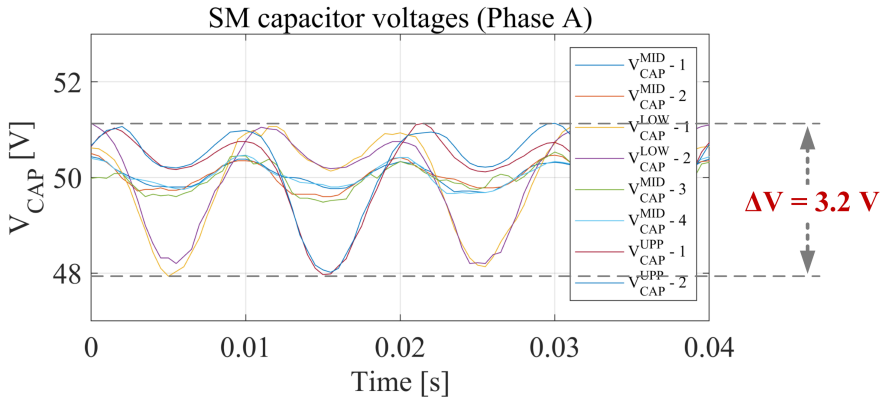


Figure 7.31: SM capacitor voltages in Phase A at P = 1.5 kW, Q = -600 VAr operating at $\boldsymbol{M = 1.38 M_{opt} \approx 1.82}$ (Data stored in the master controller RAM)

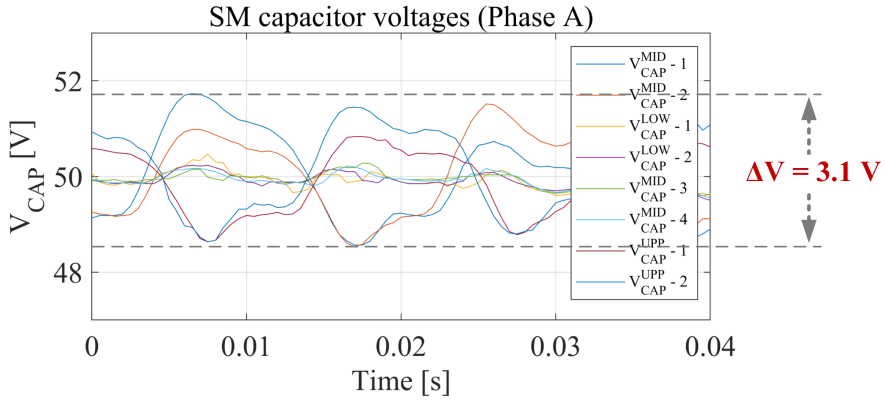


Figure 7.32: SM capacitor voltages in Phase A at P = 1.5 kW, Q = -600 VAr operating at $\boldsymbol{M = 0.84 M_{opt} \approx 1.11}$ (Data stored in the master controller RAM)

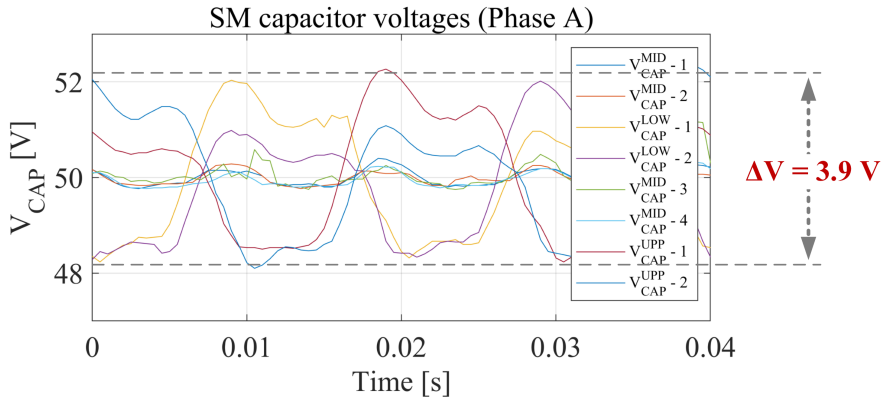


Figure 7.33: SM capacitor voltages in Phase A at P = 1.5 kW, Q = -600 VAr operating at $\boldsymbol{M = 0.75 M_{opt} \approx 1.0}$ (Data stored in the master controller RAM)

7.6 Summary

In this chapter, results from the experiment are presented to validate the converter operation. The experimental prototype is operated at an active power rating of 1.5 kW, rectifying into a resistive load of 20 Ω on the DC side.

The experimental steady state results are presented for two different P-Q operating points (P = 1.5 kW, Q = 600 VAr & P = 1.5 kW, Q = -600 VAr). For comparison, simulation results from a PLECS® simulation of the converter using the experimental system ratings are also included. Next, the transient response of the converter

is demonstrated to verify the control loops. Test conducted for the transient response are load step variation and energy reference step variation. Finally, results are presented for converter operation at different modulation indexes to verify the modulation index optimisation analysis presented earlier in Chapter 4. Overall, the results from the experimental match with the simulation results, and also validate the converter waveshaping and operation discussed in Chapter 4.

Chapter 8

Conclusions

Hybrid VSCs have attracted research interest in recent years due to their ability to meet emerging needs of the HVDC market. Based on the combination of the two- and three-level converters with the modular multilevel converters, hybrid VSCs offer several advantages such as weight, volume and cost reduction of the converter stations for offshore applications and DC fault handling capability in DC overhead lines and multi-terminal systems. The University of Nottingham, in collaboration with industry, has been actively involved in research on new hybrid VSC topologies. As an outcome of this research, two new hybrid VSC converters suitable for HVDC applications were introduced. The first was the Parallel-Hybrid Modular Multilevel Converter (PH-MMC) and the other was the Series Bridge Converter (SBC), which is a variant of the PH-MMC. Both the PH-MMC and the SBC, which were based on a series connection of converter phases across the DC side, provide significant volume and weight reduction compared to the MMC, thanks to the lesser number of submodules and smaller capacitors.

Building on the available knowledge on hybrid VSCs in the Power Electronics, Machines and Controls (PEMC) research group, this research work introduced three new hybrid VSC topologies, titled the Parallel H-bridge Converter (PHBC), the Parallel-Connected converter with Unfolding Bridges (PCUB), and the Switched Mid-Point

Converter (SMPC). The SMPC is regarded as the "main" topology of the thesis. The main chapters of this thesis investigated the SMPC topology in detail, covering the operating principle, mathematical analysis, comparison with the MMC, control strategy development and simulation and experimental validation of the topology and the control scheme.

Structurally, the SMPC is similar to the MMC in terms of the parallel connection of converter phase-legs. Each phase-leg of the SMPC is composed of three chainlinks and a director switch arrangement based on the two-level configuration. The SMPC operates by switching the middle chainlink between the upper and lower arms every AC half cycle. By expressing the chainlink voltages, currents and powers mathematically, it has been shown that the internal energy of the converter naturally balances at a specific modulation index of $\frac{\pi}{2}$, regarded as the 'sweet-spot' modulation index, M_{ss}. If the modulation index is different from M_{ss}, the result will be a surplus of average power in the middle chainlink and an equal deficit in the upper and lower chainlinks combined, or vice-versa. To restore the equilibrium position of zero average power in all chainlinks, a technique based on injection of second harmonic components in the circulating current is proposed. The balancing second harmonic transfers energy between the chainlinks, and its amplitude is a function of the operating point and the modulation index.

A method for finding the optimum value of the modulation index based on the minimisation of the energy storage of the converter is presented. It has been found that the energy storage of the SMPC varies non-linearly with a change in modulation index, and minimises at a value of $0.84M_{ss}$ for a $\frac{Q}{P}$ ratio of 0.4. Furthermore, it is also shown that if hybrid chainlinks (composed of both half-bridge and full-bridge cells) are employed in the upper and lower chainlinks, the optimum modulation index needs to be taken down to $0.75M_{ss}$ to ensure that the cell voltages of both types of cells remain stable around the nominal value.

As is important with all new modular multilevel VSC converter topologies, a comparative analysis against the half-bridge MMC is conducted. The upper and lower chainlinks in the SMPC are considered to be formed of hybrid chainlinks and the optimum modulation index of $0.75M_{ss}$ is used. For the MMC, a modulation index of 0.9 is assumed, which is the value generally used for its half-bridge version. The analysis is quantitative and uses a fixed set of system ratings. The results of the analysis showed that the although the number of cells are comparable between the SMPC and the MMC, the cell capacitors in the SMPC are smaller. Overall, the energy storage of the SMPC is 45% of that of the MMC. Hence, a SMPC converter can have a smaller overall volume and weight compared to a MMC converter. Moreover, the semiconductor losses of the converters are also comparable. The drawback is that the SMPC has a 20% higher semiconductor requirement than that of the MMC. A comparison of the SMPC with full-bridge MMC and other hybrid VSCs is an interesting study, but one that is out of scope of this thesis and a part of the future work.

Some theoretical discussions on the AC and DC fault performance of the SMPC are also included. During asymmetrical AC faults, the difference in per-phase powers results in an asymmetric set of balancing second-harmonics for the three phase-legs of the SMPC, causing a ripple in the DC-side current. For the removal of this ripple, a method is proposed in which additional second harmonic components that are in quadrature with the original balancing second harmonic components are injected in the phase-legs. The amplitude and phase of the quadrature second harmonic components are selected such that their sum opposes the DC current ripple. In addition, the SMPC can also be designed to provide DC fault blocking by forming the upper and lower chainlinks entirely using full-bridge cells and rating the chainlinks appropriately.

The control strategy for the SMPC is developed assuming a fixed DC source and imposed AC-side power demand. The main control loops in the SMPC are the AC

current control, energy control and the circulating current control. The energy control is further sub-divided into three separate control loops i.e. the total energy control, the inter-arm energy control and the inter-chainlink energy control. The final modulation references for the chainlinks are obtained by applying the selected waveshaping on the control outputs. The correct converter operation and the effectiveness of the control scheme are verified through computer simulations performed using the PLECS software package.

Eventually, for practical validation of the SMPC converter and the devised control strategy, experimental work is conducted on an existing small-scale laboratory prototype. The hardware implementation of the director switch, which is particular to the SMPC, is added to the prototype. On the AC side, the converter is connected to a programmable AC power supply, and the AC voltage is adjusted to obtain the optimum modulation index of $0.84M_{ss}$. The DC side is modelled by a resistive load, allowing only for rectification operation. The results from the experiment prove the validity of the converter concept and the control scheme, and also verify the optimum modulation index operation.

8.1 Summary of achievements

Achievements of the research work reported in this thesis include:

- Proposal and analysis of two new hybrid VSC topologies, the PHBC and the PCUB
- Invention of a new hybrid VSC topology, the SMPC, that has been proposed to reduce the converter energy storage compared to the half-bridge MMC
- Proposed solutions for the energy management problem of the SMPC, based on a detailed mathematical analysis

- Recognising the potential to optimise the SMPC in terms of energy storage and developing the analysis to find the optimum
- Analysis of the SMPC during AC and DC fault conditions, and a proposed solution for the second-harmonic DC current ripple problem in the SMPC under asymmetrical AC fault conditions
- Development of a novel energy control approach for the SMPC to ensure the correct distribution of the internal energy of the converter
- Development of the overall control strategy of the SMPC
- Verification of the converter operation and the control scheme using computer simulations
- Validation of the SMPC topology by successfully performing experimental tests

8.2 Future Work

To further advance the work presented in this thesis, the possible areas for future work include:

- Detailed investigation of the DC fault blocking capability of the SMPC, including comparisons with other DC fault tolerant VSC topologies in terms of losses, semiconductor requirement and the need for additional filtering
- Analysis of the performance of the SMPC under all possible types of symmetrical and asymmetrical AC faults, and converter bus faults
- Utilisation of multiple series-connected IGBTs used for the director switches in the experimental setup to test dynamic balancing

- Experimental testing using hybrid chainlinks for the upper and lower chainlinks of the SMPC. This will also practically validate the modified sorting algorithm and the cell voltage balance-ability analysis of Section (4.6).
- Exploring the possibility of replacing the IGBTs in the director switches with thyristors
- Analysis of the SMPC with third harmonic injection for better DC voltage utilisation and comparison against MMC with third harmonic injection

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