Individual device active cooling for enhanced system-level power density and more uniform temperature distribution

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***Abstract*—This paper provides a method of individual device active cooling system to balance the temperature distribution of system-level power density. 3L-ANPC GaN inverter was used to test and prove the feasibility of it in using multi-level systems.**

Keywords—Individual active cooling system, GaN HEMT, 3L-ANPC inverter

I. INTRODUCTION

Progress in semiconductor device technology evolution has not been matched by corresponding advancements in packaging, passives and cooling. The result is that system integration levels and performance optimization (efficiency and reliability) cannot quite realize the full potential offered by the active device technology and characteristics in terms of heat-generation rate and temperature withstand capability. The issue is particularly sensitive in the case of wide-band-gap devices (SiC, GaN), which find great favor in the implementation of multi-level inverter topologies, in which non-uniform power dissipation conditions among the chips are common. While bespoke packaging solutions are being looked at and filter size reduction is made possible by higher switching frequencies, deeper studies into cooling options are still wanting. This paper presents an original approach, based on the replacement of a common multi-chip cooler with an individual one, to yield: flexible cooling parameter setting based on individual chip dissipation; elimination of thermal cross-coupling effects; reduced overall volume.

II. CHARACTERISTICS OF THE SYSTEM

2.1 Individual coolers

As a case study, reference is made to a 2 kW 3-level GaN inverter intended for photo-voltaic applications [1]. The inverter uses 6 x 600V rated transistors, in TO220 discrete package shown in Fig.1; its power density is mainly determined by input/output filter elements and heatsink, which is shared by all devices, according to common thermal management design practice. In this work we replaced the single heat-sink with individual ones for each transistor (Fig.2): the design involves the use of a square ceramic heatsink interposed between device and fan. The HEMT is mounted onto the heatsink by a built-in bi-adhesive tape. The fan with the same as size as the heatsink is mounted onto the ceramic heatsink using adhesive tape wound around, so that no drilling or other mechanical work is needed. It is very compact and easy to mount solution.

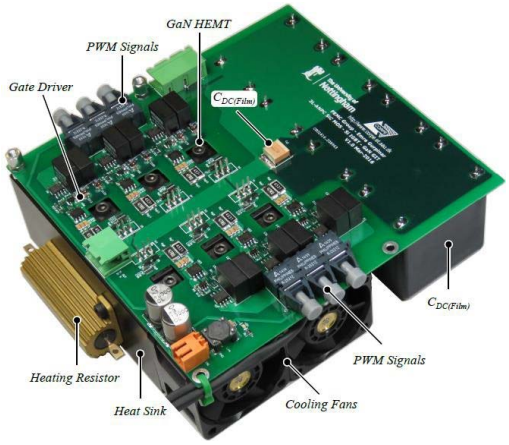

Fig. 1: 3-Level ANPC inverter assembly with indication of functional parts.

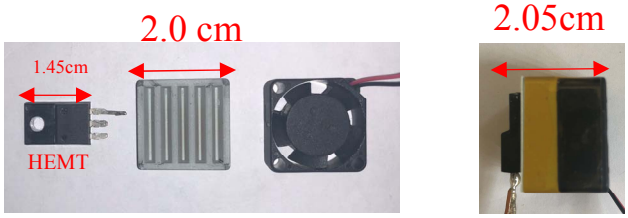

Fig. 2: Individual transistor cooling approach pursued in this study: transistor mounted on ceramic heatsink, mounted on mini-fan.

The Parameters of ceramic heatsink and fans are summarized in Table I. It is clear that the whole volume and weight significantly decrease.

TABLE I. HEAT-SINK AND FAN PARAMETERS

Ceramic Heatsink	Fan
Weight < 8.784g	Rated Voltage = 5V Rated Current = 135mA
Thermal Conductivity = 41-50 W/m.k.	Operating range = 2.5-6VDC Operating Temp. = -10-70deg Air flow = 1.6CFM Weight = 4.64g Acoustic Noise = 23.0dB (A)

Fig. 3 shows the 3L-ANPC inverter after mounting with individual coolers

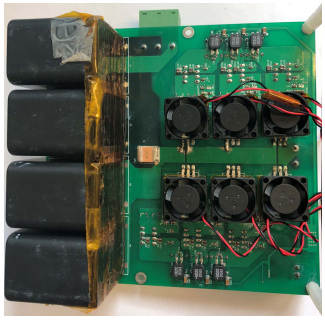

Fig. 3 The back view of 3L-ANPC inverter after mounting with new coolers.

2.2 Thermal analysis

The thermal network for one of devices of this ANPC inverter are illustrated in Fig. 4 where T_j is junction temperature, T_h is heat sink temperature, T_a is room temperature (22℃), P_loss is power loss across a single device, R_{jc} is junction-to-case thermal resistance, R_{ch} is case-to-heat sink thermal resistance and R_{hr} is required thermal resistance of the heatsink. R_{fan} is the thermal resistance of fan. X represents one of six switches. Table 2 shows known parameters of this model.

2.3 Control method of 3L-ANPC inverter

The topology of the above 3L-ANPC GaN inverter is shown in Fig. 5

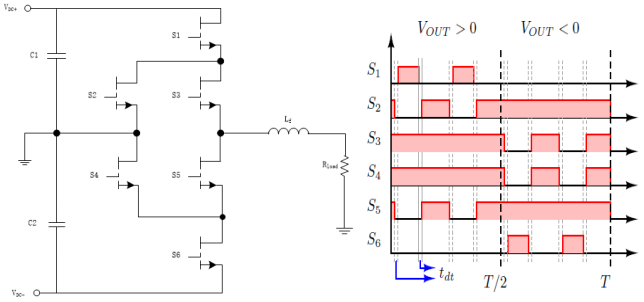

Fig. 5 The topology of 3L-ANPC GaN inverter (left); PWM control method in this case study [2] (right).

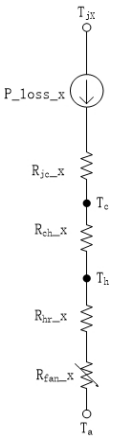

TABLE II. THERMAL MODEL PARAMETERS

T_{jX} (max) = 150℃
R_{jc}_x = 1.5℃/W
R_{ch}_x could be ignored if good mounting
R_{hr}_x = c (constant)
$R_{fan}x \propto V_{fan}$

R_{fan} could be calculated as following:

$$R_{fan}\text{\_x} = \frac{T_h - T_a}{P\_loss\_x} - c \text{ or } R_{fan}\text{\_x} = \frac{T_c - T_a}{P\_loss\_x} - c \quad (1)$$

Fig. 4 The thermal model for individual device of 3L-ANPC inverter

Because GaN HEMT has capability of reverse conduction, no parallel diodes needed. One PWM control method described in [2] was used to control this 3L-ANPC inverter. Synchronous rectification applied to decrease the conduction loss. The PWM sequence is shown in Fig. 6.

III. EXPERIMENTAL RESULTS AND DISCUSSIONS

The aim of the experiment is to prove that this individual cooler is able to balance the temperature without at the expense of volume and weight.

3.1 Thermal resistance of the fan

The case temperature at the steady state of GaN HEMT was measured by thermal couple during the experiment and thermal resistance of fan could be calculated using equation (1). The measured temperature and thermal resistance are summarized in Table 3.

TABLE III. MEASURED TEMPERATURES

P_loss (W)	Fan Voltage (V)				
	No fan	3V	4.5V	5V	6V
0.05	25.6	24.8	24.6	24.6	24.7
0.3	27.1	26.3	26.2	26.2	26.1
0.6	30.2	28.6	28.2	28.1	28
1.2	35.3	32.4	31.6	31.4	31.2
2	44.4	38.5	36.5	36.4	35.6
2.7		45.5	42.1	42	41.4
3.85		55.6	51.3	50.2	49.2
5.2		66.2	61.3	60.6	59.1

When power loss is greater than 2W, the temperature will increase dramatically, the device will face with more possibility of breaking down. Therefore, if only heatsink works, we stopped at when the power loss is 2W. It should also be noted that the case temperature varies a lot at low power. Also, fig. 7 shows the temperature changes due to the power loss under different biased voltage of the fan.

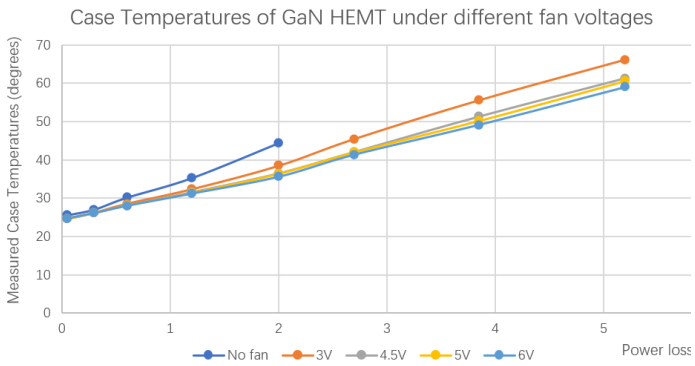

Fig. 7 The trend of the change of case temperatures due to power loss

From the above figure, these trends could be linearly interpolated. The interpolated equations are summarized in Table 4.

TABLE IV. INTERPOLATED EQUATIONS

Fan Voltage (V)	Equations
No fan (0V)	9.6944x + 24.474
3	8.1682x + 23.503
4.5	7.125x + 23.564
5	6.6592x + 23.677
6	6.6592x + 23.677

When fan voltage is 5V or 6V, the interpolated equations are the same because the air flow (speed of the fan) are almost the same even if the biased voltage increases. However, the measured case temperature shows the possibility of decreasing by at least 0.5℃ when increasing the biased voltage to 5V to 6V if the power loss is greater than 2W.

The thermal resistance could be calculated using Table 3 and equation (1). Assume R_{hr} is a small value, by approximately calculating the surface area of the heatsink, and apply equation

$R_{hr} = \frac{L}{\sigma A}$ (2), where σ is thermal conductivity, the value of R_{hr} is 0.35℃/W. Therefore, thermal resistances of the fan are summarized in Table 5 and the curve (Fig. 8) based on this shows the trend of change

TABLE V. FAN THERMAL RESISTANCE

P_loss (W)	Fan Voltage (V)				
	No fan	3V	4.5V	5V	6V
0.05	72	55.65	51.65	51.65	53.65
0.3	17	13.98	13.65	13.65	13.32
0.6	13.67	10.65	9.98	9.82	9.65
1.2	11.08	8.32	7.65	7.48	7.32
2	11.2	7.90	6.90	6.85	6.45
2.7		8.35	7.09	7.06	6.84
3.85		8.37	7.26	6.97	6.71
5.2		8.15	7.21	7.07	6.78

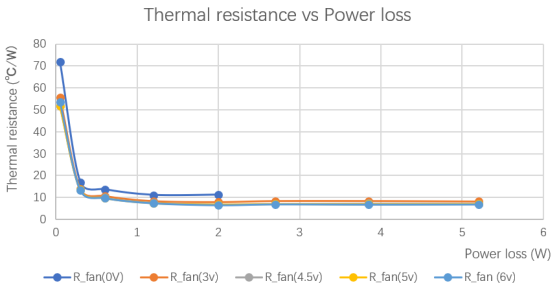

Fig. 8 Thermal resistances changes with fan voltage

It is clear that the thermal resistance decreases with the increase of the fan voltage. At low power, the temperature measurement might cause more error in calculating the thermal resistance which explain the significant thermal resistance at low power. When power loss is greater 2W, the value of fan thermal resistance is more accurate.

Also, the thermal resistance of fan does not change remarkably due to the limitation of the fan when increase the voltage which affect the effectiveness of this individual cooler.

3.2 Case study

The power loss of each device in this 3L-ANPC inverter was simulated using Plecs. Simulation parameters are summarized in Table 6.

TABLE VI. SIMULATION PARAMETERS

DC link Voltage (V)	700
Output RMS Voltages(V)	220
Output Power (W)	1K, 1.25K, 1.5K
Carrier Frequency (KHz)	100
Output Filter Inductance (mH)	1.6
Dead time (ns)	500
Modulation Index	0.95

Simulation results were illustrated in Table 7. Due to the symmetry of ANPC inverter, only power loss of the upper side switches loss.

TABLE VII. POWER LOSS OF HIGH-SIDE DEVICES

Output Power (W)	Power loss on each device (W)		
	S1	S2	S3
1000	1.67	1.61	2.15
1250	2.43	1.99	2.92
1500	3.28	2.48	3.9

From Table 7, S3 and S5 are the most stressed by power loss.

Therefore, we attempt to control the temperature of S3 by changing the fan voltage to make it more balanced. Under normal condition, we used rated 5V. At this time, the corresponding temperature of S3 could be interpolated using the equation in Table 4. To balance the temperature, we could turn off the fan when P_loss is 2.15W use 3V when P_loss is 2.92W and use 6V. The results could be seen in Table 8 and Fig. 9.

TABLE VIII. CASE TEMP. FOR 5V FAN BIAS

Power Loss (W)	Case Temperature (degrees) Rated Voltage 5V	Varied fan voltage
2.15	38	45 (0V)
2.92	43	47 (3V)
3.9	50	49 (6V)

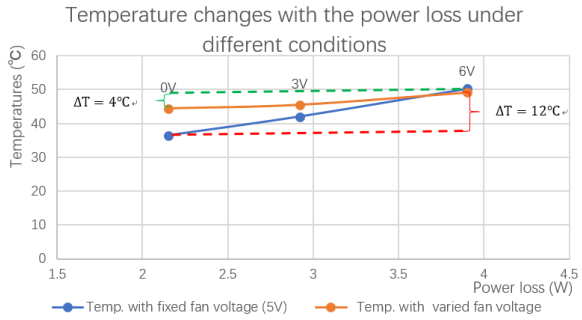

Fig. 9 The case temperatures when keeping the rated voltage and changing the fan voltage

It is clear that the temperature difference when the power loss increase from 2.15W to 3.9W decrease 8℃ using varying fan voltage method rather than keeping at 5V.

Furthermore, we could balance the temperatures between two devices. From Table 7, the power loss difference between S2 and S3 are the maximum. (Fig. 10)

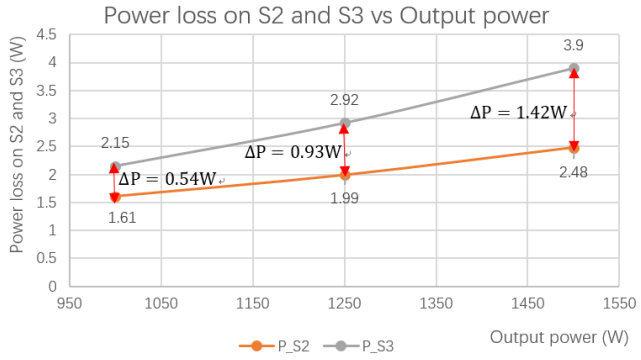

Fig. 10 Power loss and its difference between S2 and S3

The case temperatures for both S2 and S3 could be interpolated using equations in Table 4. Assume the constant fan voltage (5V). The temperatures for fixed fan voltage are summarized in Table 9. Then control the temperature by adjusting the fan voltage, the results are summarized in Table 10.

TABLE IX. CASE TEMPERATURE OF S2 AND S3 AT 5V FAN BIAS

Power Loss (W)	Case Temperature (degrees) S3	S2	Difference
2.15	38	34	4
2.92	43	37	6
3.9	50	40	10

From Table 9, the temperature difference will increase with the power loss increase.

TABLE X. CASE TEMPERATURE OF S2 AND S3 WITH REGULATED FAN BIAS

Power Loss (W)	Case Temperature (degrees) S3	S2	Difference
2.15	38 (5V)	37 (3V)	1
2.92	43 (5V)	44 (0V)	1
3.9	49 (6V)	48 (0V)	1

Table 10 shows the possibility that the time difference could be the same even the power loss increases.

IV. CONCLUSION

These individual active cooling systems have capability of balancing the temperatures of the fan when increasing or decreasing the power loss of each device. Also, the noise of the system is acceptable. However, the effectiveness is restricted by the characteristics of the fan and the ceramic heatsink. Firstly, the speed of the fan does not change significantly when we increase the biased voltage which causes the small change of thermal resistances. This kind of small fan is the minority number of fan which are available and suitable for this case study in the market even though they have some disadvantages.

Secondly, there are some limitations of the ceramic heatsink. We expect heatsinks with higher thermal conductivity (smaller thermal resistivity) and as the similar size as the device itself. The heat conductivity of ceramic material is worse than metal but it has the advantage of light weight lower thermal expansion coefficient. To improve the feasibility of the individual coolers, new material heatsink could be attempted.

Thirdly, the mounting method, in the case study, the ceramic heatsink has built-in thermal tape and we could use it to mount HEMT onto the heatsink. In the case study illustrated above, we were faced with a problem of not good stickiness for one or two heatsinks, which fell off during the experiment. This proves using thermal tape is not perfect. Furthermore, for the heatsink we used in the experiment, although it is very thin, it has very high thermal resistance which will decrease the effectiveness of The heatsink. To improve this, new method of mounting should be used.

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