Rapid Faults Detection for Controlling Multi-terminal High Voltage DC Grids under AC Grid Contingencies

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Abstract

To control power flow for integration of distributed energy onto urban power grids, rapid and accurate detection of the amplitude, phase-angle, and frequency offset of the grid voltage's positive and negative sequence components especially under grid fault conditions are more significant. This paper presents a new faults detection method that is capable of tracking signal deviations on the grid-voltage accurately and rapidly even in the case that bus-voltage contains high order harmonics and random noises. The experimental results verify the validity of the proposed method under various grid-fault conditions.

1. Introduction

Offshore wind farms have been identified as one of the solutions to low carbon and global warming. However, integrating offshore wind farms to urban power grids over distance of tens or hundreds kilometers is a challenge for power networks [1]. To deal with this issue, multi-terminal High Voltage DC transmission systems (MTDC) have been utilized with the development of power electronics. The focuses of current research trends are on investigating the control strategy of MTDC transmission for offshore wind power systems.

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Phase lock loops (PLL) [2-7] play a significant role in achieving good transient performance of the Voltage Source Converters (VSC) under grid faults scenarios due to the fact that the control of energy conversion highly relies on transformations of synchronous reference frame. At the Point of Common Connection (PCC), the rotating angle of the AC voltage vector must be accurately tracked at a fast rate. Fig.1 shows the closed-loop structure of a widely-adopted synchronous reference frame (SRF) PLL where the three-phase voltages of AC grids are transformed to d-q quantities by using the tracked angle. A Proportional plus Integral controller is employed to produce the rotating speed of the voltage vector on the basis of the error of the q-axis PCC bus voltage. The q-axis component of the PCC bus voltage makes its way towards zero in order to minimize the interaction between the active and reactive power control.
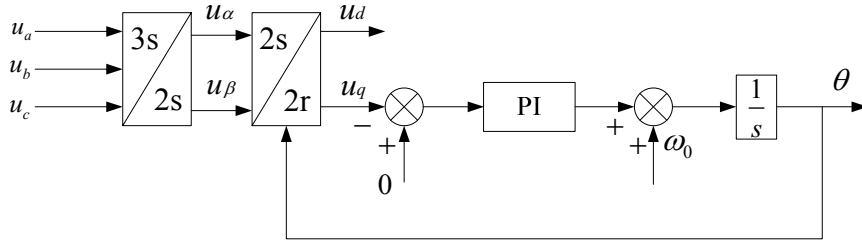

Fig. 1. Closed-loop structure for SRF-PLL

When AC grid contingencies happen, the grid voltage has to be tracked in between the time instants of the occurrence and clearance of a balanced or even unbalanced fault at the PCC bus. A low-bandwidth PLL may not be capable to track the angle of the PCC voltage sufficiently fast. This may deviate q-axis voltage and therefore deteriorate the control performance of the active and reactive power control. Nevertheless, a PLL with increased bandwidth may not be robust to high frequency distortions and cause unwanted interference with other control loops [4-7]. The linearization of the closed-loop PLL system illustrates that the loop gain has been significantly influenced by the grid voltage that is to be tracked. This implies that the speed response is decreased and disturbance rejection is worse in low-voltage conditions.

In general, the techniques of grid-voltage vector detection can be divided into the following categories:
1) Detection methods based on various coordinate transformation and a variety of filters [8-9].
2) Voltage-vector detection methods using improved PLLs [10-11].
3) The state space estimation methods [12].

The existing techniques can only detect partial fault information and are not able to deal with various contingencies simultaneously. An effective PLL is proposed in this paper that has been analytically tuned.

2. Decoupled Double Synchronous Reference Frame (D2SRF) PLL

Considering only the positive and negative components of the fundamental grids voltage, the voltage vector equation in the stationary reference frame is:

$$E_s = E_{dq}{}^P e^{j\omega t} + E_{dq}{}^N e^{-j\omega t} \tag{1}$$

where E_s --- Grid voltage vector, $E_s = 2/3\left(e_a + e_b e^{j2\pi/3} + e_c e^{-j2\pi/3}\right)$;

$E_{dq}{}^P e^{j\omega t}$ --- Positive sequence component of the fundamental bus voltage where $E_{dq}{}^P = E_d{}^P + jE_q{}^P$.

$E_{dq}{}^N e^{-j\omega t}$ --- Negtive sequence component of the fundamental bus voltage where $E_{dq}{}^N = E_d{}^N + jE_q{}^N$.

ω ---Angular frequency of the bus voltage.

The current vector equations:

$$I_s = I_{dq}{}^P e^{j\omega t} + I_{dq}{}^N e^{-j\omega t} \tag{2}$$

For the grid-side converter, the voltage equation in the stationary reference frame is:

$$L\frac{dI_s}{dt} = -RI_s + E_s - U_s \tag{3}$$

where U_s is the voltage vector of the AC grid.

Transforming (3) into d-q rotating reference frame and splitting positive and negative components yields the mathematical model for grid-side power converter in the positive and negative rotating frames. P represents positive and N negative.

When asymmetrical faults happen to the power grid, the output power of the converter is:

$$S = E_s I_s{}^* = \frac{3}{2}\left(E_{dq}{}^P e^{j\omega t} + E_{dq}{}^N e^{-j\omega t}\right)\left(I_{dq}{}^{P*} e^{-j\omega t} + I_{dq}{}^{N*} e^{j\omega t}\right) \tag{4}$$

Decoupled Double Synchronous Reference Frame (D2SRF) PLL is capable of detecting the voltage vector at a relatively fast rate. Double Synchronous Reference Frames consist of the positive frame dq^{+1} with angular frequency $\hat{\omega}$ and position $\hat{\theta}$ that rotates anti-clockwise and the negative frame dq^{-1} with $-\hat{\omega}$ and $-\hat{\theta}$ that goes round clockwise. As shown in Fig. 2, the voltage vector U_s can be split into positive sequence component U_s^{+1} and negative component U_s^{-1}. ϕ^{-1} is the initial phase angle of the fundamental negative sequence voltage. U_s expression in the double Synchronous Reference Frames is:

$$u_{s_{(dq^{+1})}} = \begin{bmatrix} u_{sd^{+1}} \\ u_{sq^{+1}} \end{bmatrix} = \left[T_{dq^{+1}}\right] u_{s\alpha\beta} = U_s^{+1}\begin{bmatrix} \cos\left(\omega t - \hat{\theta}\right) \\ \sin\left(\omega t - \hat{\theta}\right) \end{bmatrix} + U_s^{-1}\begin{bmatrix} \cos\left(-\omega t + \phi^{-1} - \hat{\theta}\right) \\ \sin\left(-\omega t + \phi^{-1} - \hat{\theta}\right) \end{bmatrix} \tag{5}$$

$$u_{s_{(dq^{-1})}} = \begin{bmatrix} u_{sd^{-1}} \\ u_{sq^{-1}} \end{bmatrix} = \left[T_{dq^{-1}}\right] u_{s\alpha\beta} = U_s^{+1}\begin{bmatrix} \cos\left(\omega t + \hat{\theta}\right) \\ \sin\left(\omega t + \hat{\theta}\right) \end{bmatrix} + U_s^{-1}\begin{bmatrix} \cos\left(-\omega t + \phi^{-1} + \hat{\theta}\right) \\ \sin\left(-\omega t + \phi^{-1} + \hat{\theta}\right) \end{bmatrix} \tag{6}$$

where $\left[T_{dq^{+1}}\right] = \left[T_{dq^{-1}}\right]^T = \begin{bmatrix} \cos(\hat{\theta}) & \sin(\hat{\theta}) \\ -\sin(\hat{\theta}) & \cos(\hat{\theta}) \end{bmatrix}$

dq^{+1} reference frame can be made roughly synchronized with the positive sequence voltage. Then $\hat{\theta} \approx \omega t$. Set $\sin(\omega t - \hat{\theta}) \approx (\omega t - \hat{\theta})$, $\cos(\omega t - \hat{\theta}) \approx 1 - ((\omega t - \hat{\theta})^2/2)$ and $(-\omega t - \hat{\theta}) \approx -2\omega t$. Linearizing (5) and (6) yields:

$$u_{s_{(dq^{+1})}} \approx U_s^{+1}\begin{bmatrix} 1 - ((\omega t - \hat{\theta})^2/2) \\ \omega t - \hat{\theta} \end{bmatrix} + U_s^{-1}\begin{bmatrix} \cos(-2\omega t + \phi^{-1}) \\ \sin(-2\omega t + \phi^{-1}) \end{bmatrix} \tag{7}$$

$$u_{s_{(dq^{-1})}} \approx U_s^{+1}\begin{bmatrix} \cos(2\omega t) \\ \sin(2\omega t) \end{bmatrix} + U_s^{-1}\begin{bmatrix} \cos(\phi^{-1}) \\ \sin(\phi^{-1}) \end{bmatrix} \tag{8}$$
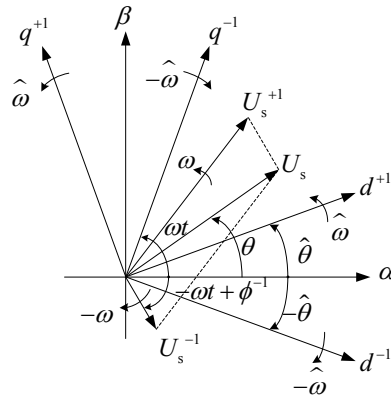
Fig. 2. The double Synchronous Reference Frames and voltage vectors.

It can be found from (7) and (8) that the magnitudes of the positive and negative sequence voltages are contaminated with DC components and second order harmonics. Traditional PLL may become oscillatory dealing with this situation. To depress the potential oscillation, a decoupling network is introduced to follow the phase trajectory of the fundamental positive sequence voltage, i.e. $\hat{\theta} = \omega t$.

$$
u_{s_{(dq^{+1})}} = \begin{bmatrix} u_{sd^{+1}} \\ u_{sq^{+1}} \end{bmatrix}
$$

$$
= U_s^{+1} \begin{bmatrix} \cos(\phi^{+1}) \\ \sin(\phi^{+1}) \end{bmatrix} + U_s^{-1} \cos(\phi^{-1}) \begin{bmatrix} \cos(2\omega t) \\ -\sin(2\omega t) \end{bmatrix} + U_s^{-1} \sin(\phi^{-1}) \begin{bmatrix} \sin(2\omega t) \\ \cos(2\omega t) \end{bmatrix} \tag{9}
$$

$$
u_{s_{(dq^{-1})}} = \begin{bmatrix} u_{sd^{-1}} \\ u_{sq^{-1}} \end{bmatrix}
$$

$$
= U_s^{+1} \begin{bmatrix} \cos(\phi^{+1}) \\ \sin(\phi^{+1}) \end{bmatrix} + U_s^{-1} \cos(\phi^{+1}) \begin{bmatrix} \cos(2\omega t) \\ \sin(2\omega t) \end{bmatrix} + U_s^{-1} \sin(\phi^{-1}) \begin{bmatrix} -\sin(2\omega t) \\ \cos(2\omega t) \end{bmatrix} \tag{10}
$$

The working process of the D2SRF PLL is to extract the positive and negative components, pass them through low pass filters then feedback to the relevant decoupling units. The structure forms a closed-loop correction process for the purpose of depressing the oscillations. The decoupling network for dq^{+1} and dq^{-1} reference frames is illustrated in Fig. 3 where the input angle of the dq^{-1} decoupling is $-2\hat{\theta}$. $\bar{u}_{sd^{+1}}$, $\bar{u}_{sq^{+1}}$, $\bar{u}_{sd^{-1}}$ and $\bar{u}_{sq^{-1}}$ are filtered mean values of the voltages, respectively.

The expression of the low pass filter is:

$$
\text{LPF}(s) = \frac{\omega_f}{s + \omega_f} \tag{11}
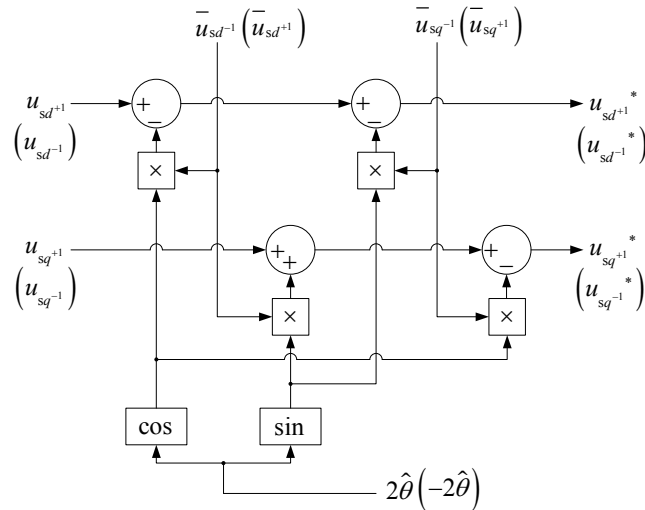$$

where ω_f ---cutoff frequency

Fig. 3. Decoupling network

After the filtering and decoupling, the influence of negative sequence quantities can be alleviated. The phase angle of the fundamental positive sequence voltage can be accurately tracked by setting the $u_{sq^{+1}}$ reference value and utilizing the control strategy of the traditional PLL.
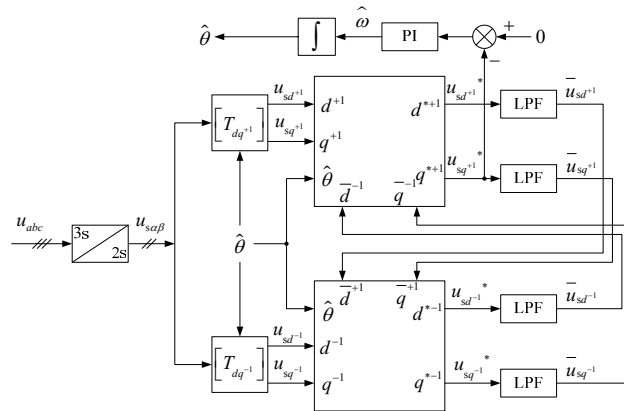

Fig. 4. D2SRF PLL structure

3. Experimental Results

To experimentally verify the capabilities of tracking faulty bus voltages for the D2SRF PLL, various grid voltage faults was emulated by Chroma 61705, a high performance three-phase programmable AC source device that is programed to generate temporary voltage surge and dips, phase angle jumps, harmonics superimpositions, three-phase unbalancing, frequency deviations and classical faulty conditions. A digital signal processing board TMS320F2812 serves as the real-time platform.

As shown by Fig. 5-a, at the time instant of 0.29 second, the grid voltage is programmed to consist of 100% positive components and 10% negative component. At the time instant of 0.29 second, the amplitude of positive component drops by 50%, the phase angle jumped by $\pi/2$, negative component suddenly changes to 50% and the frequency jumps from 50Hz to 60Hz. Those sudden changes to the grid voltage are considered to be a rather worse case of power quality.

As shown by Fig. 5-a, 5th harmonic with the amplitude of 10% and 7th harmonic with amplitude of 2.5% were superimposed onto the voltage. It can be seen that before the faults happen, the grid-voltage is only composed of three-phase positive sequence components. When the contingency occurs, the amplitude, phase angle, frequency of the voltage suddenly change and contain negative sequence components. This is a more serious situation.
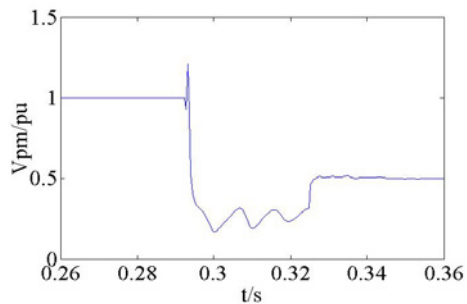
Fig 5-b) to f) demonstrates that it takes less than 0.01seconds for tracking of the amplitude, phase angle and frequency of the grid voltage. The phase angle estimation converges faster than the magnitude estimation and has smaller overshoot.
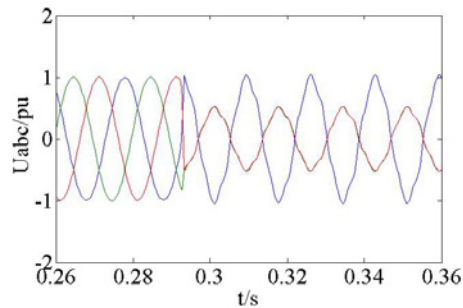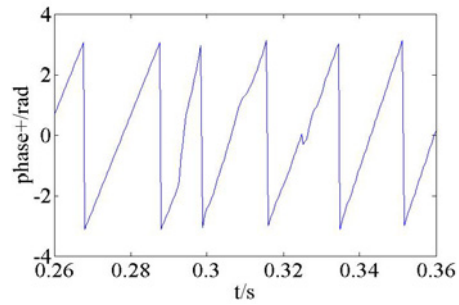

a) Unbalanced three phase grid voltages with harmonics added---experimental results.
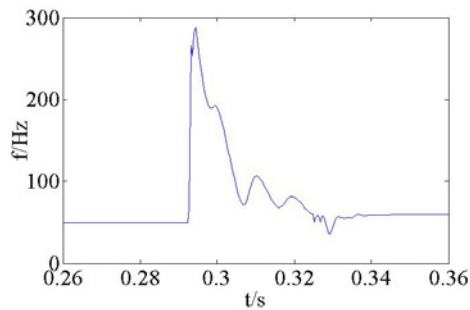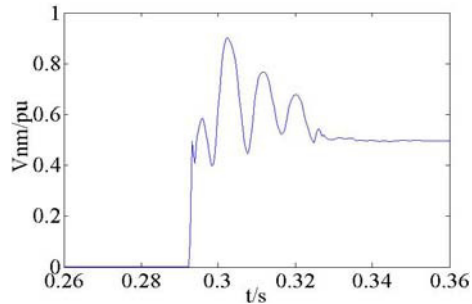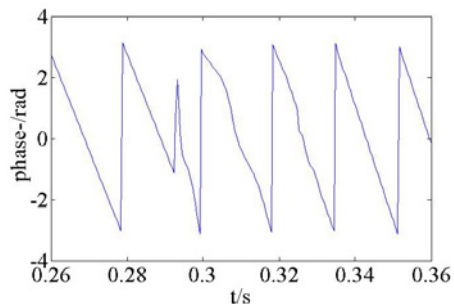

b) Frequency estimation

c) Estimation of the amplitude of positive component.

d) Estimation of the angle of positive component

e) Estimation of the amplitude of negative component.

f) Estimation of the angle of negative component

Fig.5. Detection results under unbalanced three phase grid voltages with harmonics added---experimental results.

Conclusions

The method overcomes the disadvantages of using existing methods which can only detect partial fault information on power grids and exhibit poor effectiveness. The D2SRF PLL can detect the amplitude, phase angle and frequency offset for the positive and negative sequence components. It is robust to high harmonics and random noises. The D2SRF PLL has been implemented and tested on the laboratory platform based on TMS320F2812 digital signal processor. A variety of fault conditions were emulated by using a programmable AC source device. The correctness of the suggested method has been verified.

Acknowledgements

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Biography

Dr Zhuang Xu works with the University of Nottingham Ningbo China. Zhuang Xu received his Ph.D. degree in electrical engineering from the University of New South Wales, Sydney, Australia. His research has been focused on power electronics and high-performance electrical drives.