Development of Phase Change Memory Cell Electrical Circuit Model for Non-volatile Multistate Memory Device

Nemat Hassan Ahmed ElHassan, BSc.

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Abstract

Phase change memory (PCM) is an emerging non-volatile memory technology that demonstrates promising performance characteristics. The presented research aims to study the feasibility of using resistive non-volatile PCM in embedded memory applications, and in bridging the performance gap in traditional memory hierarchy between volatile and non-volatile memories.

The research studies the operation dynamics of PCM, including its electrical, thermal and physical properties; in order to determine its behaviour. A PCM cell circuit model is designed and simulated with the aid of SPICE tools (LTSPICE IV). The first step in the modelling process was to design a single-level PCM (SLPCM) cell circuit model that stores a single bit of data. To design the PCM circuit model; crystallization theory and heat transfer equation were utilized. The developed electrical circuit model evaluates the physical transformations that a PCM cell undergoes in response to an input pulse. Furthermore, the developed model accurately simulated the temperature profile, the crystalline fraction, and the resistance of the cell as a function of the programming pulse.

The circuit model is then upgraded into a multilevel phase change memory (MLPCM) cell circuit model. The upgraded MLPCM circuit model stores two bits of data, and incorporates resistance drift with time. The multiple resistance levels were achieved by controlling the programming pulse width in the range of 10ns to 200ns. Additionally, the drift behaviour was precisely evaluated; by using statistical data of drift exponents, and evaluating the exact drift duration.

Moreover, the simulation results for the designed SLPCM and MLPCM cell models were found to be in close agreement with experimental data. The simulated I-

V characteristics for both SLPCM and MLPCM mimicked the experimentally produced I-V curves. Furthermore, the simulated drift resistance levels matched the experimental data for drift durations up to 10^3 seconds; which is the available experimental data duration in technical literature. Furthermore, the simulation results of MLPCM showed that the deviation between the programmed and drifted resistance can reach $6x10^6\Omega$ in less than 10^{10} seconds. This resistance deviation leads to reading failures in less than 100 seconds after programming, if standard fixed sensing thresholds method was used.

Therefore, to overcome drift reliability issues, and retain the density advantage offered by multilevel operation; a time-aware sensing scheme is developed. The designed sensing scheme compensates for the drift caused resistance deviation; by using statistical data of drift coefficients to forecast adaptive sensing thresholds. The simulation results showed that the use of adaptive time-aware sensing thresholds completely eliminated drift reliability issues and read errors.

Furthermore, PCM based nanocrossbar memory structure performance in terms of delay and energy consumption is studied in simulation environment. The nanocrossbar is constructed with a grid of connecting wires; and the designed PCM cell circuit model is used as memory element and placed at junction points of the grid. Then the effect of connecting nanowires resistance in PCM nanocrossbar performance is studied in passive crossbars. The resistance of a connecting wire segment was evaluated with physical formulas that calculate nanoscaled conductors' resistance. Then a resistor that is equivalent to each wire segment resistance is placed in the tested crossbar structure.

Simulation results showed that due to connecting wires resistance; the PCM cells are not truly biased to programming voltage and ground. This leads to 40% deviation

in the programed low resistive state from the targeted levels. Thus, affecting PCM reliability and decreasing the high to low resistance ratio by 90%.

Therefore, programming and architectural solutions to wire resistance related reliability issue are presented. Where dissipated power across wire resistance is compensated for; by controlling programming pulse duration. The programming solution retained reliability however; it increased programming energy consumption and delay by an average of 40pJ and 60ns respectively per operation.

Additionally, the effects of leakage energy in PCM based nanocrossbars were studied in simulation environment. Then, a structural solution was developed and designed. In the designed structure; leakage sneak paths are eliminated by introducing individual word lines to each memory element. This method led to 30% reduction in reading delay, and consumed only about sixth the leakage energy consumed by the standard structure.

Moreover, a sensing scheme that aims to reduce energy consumption in PCM based nanocrossbars during reading process was explored. The sensing method is developed using AC current in contrast to the standard DC current reading circuits. In the designed sensing circuit, a low pass filter is utilized. Accordingly, the filter attenuation of the applied AC reading signal indicates the stored state. The proposed circuit design of the AC sensing scheme was constructed and studied in simulation environment. Simulation results showed that AC sensing has reduced reading energy consumption by over 50%; compared to standard DC sensing scheme.

Furthermore, the use of SLPCM and MLPCM in memory applications as crossbar memory elements, and in logic applications i.e. PCM based LUTs was explored and tested in simulation environment. The PCM performance in crossbar memory was then compared to current Static Random Access Memory (SRAM)

technology and against one of the main emerging resistive non-volatile memory technologies i.e. Memristors.

Simulation results showed that programming and reading energy consumption of PCM based crossbars were five orders of magnitude more than SRAM based crossbars. And reading delay of SRAM based crossbars was only 38% of reading delay of PCM based counterparts. However, PCM cells occupies less than 60% of the area required by SRAM and can store multiple bit in a single cell.

Moreover, Memristor based nanocrossbars outperformed PCM based ones; in terms of delay and energy consumption. With PCM consuming 2 orders of magnitude more energy during programming and reading. PCM also required 10 times the programming delay. However, PCM crossbars offered higher switching resistance range i.e. 170kΩ compared to the 20kΩ offered by memristors; which support PCM multibit storage capability and higher density.

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3. **Nemat H. El-Hassan**, Ong Ming Hong, T. Nandha Kumar, and Haider Abbas F. Almurib, "Phase Change Memory Cell Emulator Circuit Design", *Elsevier Microelectronic Journal,* 2016.

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Glossary

VM	-	Volatile Memory
NVM	-	Non-Volatile Memory
SCM	-	Storage Class Memory
CPU	-	Central Processing Unit
RAM	-	Random Access Memory
SRAM	-	Static Random Access Memory
DRAM	-	Dynamic Random Access Memory
CMOS	-	Complementary metal oxide semiconductor
ReRAM	-	Resistive Random Access Memory
PCM	-	Phase Change Memory
MRAM	-	Magnetic Random Access Memory
MTJ	-	Magnetic Tunnelling Junction
GST	-	Germanium Antimony Telluride ($Ge_2Sb_2Te_5$)
PCRAM	-	Phase-change Random Access Memory
CBRAM	-	Conductive Bridge Random Access Memory
$V_{threshold}$	-	Threshold voltage
OUM	-	Ovonic Unified Memory
FCC	-	Face Centered Cubic
JMAK	-	Johnson-Mehl-Avrami-Kolmogorov
R_{PCM}	-	Cell resistance
R_{drift}	-	Drifted cell resistance
V_{Tdrift}	-	Drifted cell threshold voltage
t_{off}	-	Drift duration
VCR	-	Voltage controlled resistor

VCVS	-	Voltage Controlled Voltage Source
V_C	-	Crystalline fraction
$R_{crystalline}$ / R_{SET}	-	Crystalline state resistance
$R_{amorphous}$ / R_{RESET} / R_{OFF}	-	Amorphous state resistance
R_{ON}	-	Dynamic ON_state resistance
V_{cell}	-	Voltage across PCM cell
T_{cell}	-	Temperature across PCM cell
T_{cryt}	-	GST Crystallization temperature
T_{melt}	-	GST Melting temperature
V_{Tmax}	-	Maximum threshold voltage
V_{Tmin}	-	Minimum threshold voltage
opamp	-	operational amplifier
AC	-	Alternate Current
R_W	-	Connecting wire segment electrical resistance
MSB	-	Most Significant Bit
LSB	-	Least Significant Bit

CHAPTER 1

INTRODUCTION

1.1 Background

The phase change memory (PCM) also known as the Ovonic Unified Memory (OUM) [1] was first proposed by Ovshinsky in the early 1960's; based on $Ge_2Sb_2Te_5$ (GST) chalcogenide alloy. In its early development, GST was implemented on rewritable optical CD/DVD disks. However, as PCM technology substantially advanced, it became possible to integrate GST in today's ICs where manufacturing costs have been considerably reduced [2].

The operation concept of PCM relies on the fact that the phase change material can exist in at least two phases and can undergo a thermally induced phase change. The phase change is typically from highly resistive phase to low resistive phase or vice versa. The high resistive state is a disordered amorphous phase with short range atomic order and low free electron density. The low resistive state is at crystalline phase, with long range atomic order and high free electron density. The resistance of the two phases is read to distinguish two different states equivalent to binary 1 and 0.

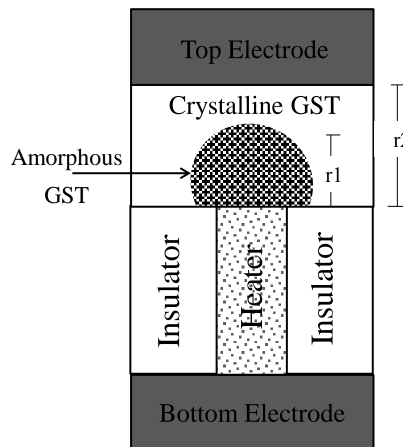

Figure 1.1: Cross section of PCM cell mushroom structure

The basic schematic cross section of PCM cell structure shown in Figure 1.1 is referred to as a mushroom cell. It is constituted of a thin film of chalcogenide material (GST in this work) with thickness of r2 in contact with a metallic heater; the

heater is surrounded by an insulator material. The programmable region referred to as active region in Figure 1.1 is the part that undergoes the phase change process which has the thickness of r1. The overall resistance of the cell is the series resistance of the bottom electrode, the heater, the phase change active region (GST layer) and the top electrode.

The PCM significance resides in its non-volatility among other properties that make it one of the most promising candidates for next generation mainstream Non-volatile Memory (NVM). PCM desirable properties include endurance, retention, and high density compared to other competing NVM technologies [3]–[8]. Furthermore, PCM properties make the technology a strong and desirable candidate in applications other than memories such as processors [9], space applications [10], and as electronic synaptic elements for building brain-like systems [11].

The high density offered by PCM is achieved by utilizing multilevel operation. In multilevel operation; each cell can be programmed to up to 2^N resistance levels and store N bits; leading to lower cost [12], [13]operation is essential for PCM to fulfil its potential as replacement for Flash memory; and it enhances PCM competitiveness in the market [14]. However, experimental results suggest that resistance drift with time, thermal disturbance and noise [15] are critical reliability issues in multilevel [12], [13].

To assess the undesirable resistance drift effects from design perspective; an accurate predictive electrical circuit model of PCM cell is required. It is also needed to realize a straightforward and timely implementation of PCM in an integrated circuit IC [16]. Such model can help in mitigating the resulting reliability drawbacks in multilevel operation. The model can be used in design, testing and implementation of PCM applications. Several such Spice based simulation models are found in technical literature. These models demonstrate the basic characteristics and operational features of PCM. However, these models failed to simulate key aspects in

PCM operation; such as the impact of time and the stochastic nature of drift at different resistive levels.

Additionally to utilize the high density offered by PCM, it is placed in a crossbar structure. Crossbar memory arrays provide efficient means to facilitate large scale geometry which in turn enables ultra-high densities [17]. Crossbars are constructed of a mesh of intersecting conducting wires; with memory elements placed at each intersection point. Due to increasing demand for denser and faster memory devices; researchers have moved to replace standard SRAM based crossbars with non-volatile memory (NVM) devices based nanocrossbars [18], [19]. However, nanocrossbar structures have multiple performance issues. These issues lead to an increase in consumed energy and can affect the programming performance. Including leakage [17], [20], [21] stray capacitances caused by memory peripheral circuitry , thermal crosstalk [22], and connecting wire resistance [23], [24].

These nanocrossbar performance issues have been addressed in technical literature. A number of methods have been proposed in attempts to eliminate the leakage currents; yet most of the proposed techniques aimed to reduce the reliability issues caused by leakage and not the energy loss due to leakage currents. The leakage mitigation methods included partial biasing [3], crossbar architecture designs [4], and AC sensing [5] which was targeted towards Memristors.

Furthermore, connecting wire resistance at nanoscaled crossbars increases with decreasing dimensions. This resistance increase leads to additional voltage drop across the connecting wires. Which affects the final programmed state of the PCM cell since the power delivered to the cell is reduced. The effects of connecting wire resistances has been addressed in technical literature [23]–[28]. However, all the works were targeted at general NVM crossbars and not the particular case of PCM based nanocrossbars. Furthermore, these works have used less than accurate estimations that did not consider the nanoscale effect on connecting wires resistance.

1.2 Aims

The general purpose of this research is to study, model, simulate and verify a realistic phase change memory (PCM) circuit model with the aid of Spice tools (LTSPICE). The model is expected to realistically simulate the temperature profile across the cell, calculate the crystalline fraction, measure the resistance of the cell and successfully generate the I-V characteristics of a PCM cell. The PCM cell model is designed with the purpose of understanding the PCM characteristics, study its failure modes, develop solutions, and evaluate the feasibility of PCM as a non-volatile random access memory technology for embedded memory applications.

The purpose of designing, testing, and verifying the PCM cell model against experimental data; is to use it as a building block to design and further test PCM performance in nanocrossbar memory arrays. The memory array performance is tested after designing and introducing the proper programming and read circuitry to the PCM crossbar structure. The aim of testing is to identify PCM array operational behaviour, determine its operational failures, their origins, and ways to avoid them in order to utilize PCM technology to its fullest potential and exploit multilevel storage property offered by PCM.

1.3 Objectives

- ❖ Design and implement an accurate circuit model for single and multibit storing PCM cell using crystallization theory and heat transfer governing equations. Then verify the circuit model behaviour by comparing against experimental data.
- ❖ Accurately evaluate drift phenomenon based on statistical data, and evaluate its effect on reliability. Then develop a drift prediction and mitigation method.
- ❖ Use the designed PCM circuit model to test performance of PCM elements in memory crossbar structure. Including the effects of leakage currents and

nanoscaled connecting wires resistance on energy dissipation and operation delay in crossbars.

- ❖ Develop an embedded memory and logic applications utilizing PCM properties, and the designed circuit model.
- ❖ Compare performance of PCM, SRAM, and NVM based crossbars in terms of programming and reading energy consumption, operation delay, and density.

1.4 Contribution of the research

This work develops a PCM cell model that overcomes all accuracy issues demonstrated by previous PCM models in technical literature. The designed model evaluates drift phenomenon and accurately accounts for variability in drift exponents thus evaluating drift effects at multilevel operation mode. Based on that model a sensing scheme that overcomes the reliability issue arising from drift is developed. That scheme minimizes the area over head and programming complexity encountered in previously proposed drift solutions.

Furthermore, the designed PCM cell circuit model is used as a building block to evaluate PCM based memory crossbars performance, an area that is not thoroughly explored in technical literature. Additionally, there is no research in literature that has conducted detailed comparison between PCM and other memory technologies using the same crossbar architecture. In this work, SRAM, memristor and PCM based crossbars performance is compared in simulation environment using the exact same crossbar architecture; thus providing a fair comparison medium in which the performance characteristics of each memory technology are accurately calculated and advantages highlighted to be further utilized in more proper applications. Finally, this work studied the feasibility of using PCM in memory and logic applications and successfully implemented MLPCM based LUTs and embedded memory structures.

1.5 Thesis outline

The layout of the rest of this thesis is as follows; Chapter 2 starts with an overview of current memory architecture and performance metrics used in evaluating memory performance. The most prominent emerging NVM technologies are briefly introduced. A detailed review of physical properties, operation concepts and reliability issues of PCM is presented. Chapter 3 is the chapter of literature review that highlights PCM behaviour governing equations, available PCM models, issues with PCM based crossbars, and how they are addressed in technical literature. The chapter also describes the methodology adopted in this work.

The designed PCM cell model is presented in Chapter 4 of this thesis. It describes in detail the circuit designs of the modules constituting the designed cell model, and the physical equations governing the model behaviour. It elaborates on the simulation patterns that are tested and compares the obtained results of simulations against experimental data. The work moves on to upgrade the single bit PCM cell design into multilevel PCM cell design. Moreover, the drift behaviour of amorphous and intermediate resistance levels of GST is simulated using experimental statistical data as reference. And a drift mitigation sensing method is presented.

Chapter 5 studies the performance issues facing memory crossbars in general and PCM based nanocrossbars in particular. Namely; connecting wire resistance energy consumption and energy dissipation due to leakage currents. Furthermore, the work elaborates on proposing solution to these performance drawbacks. The proposed solutions are designed and tested in simulation environment.

The use of PCM based nanocrossbar in memory and logic applications is presented in Chapter 6. Where both single and multibit storage using PCM based crossbars was explored. And a performance comparison in terms of delay, energy consumption and leakage energy in simulation environment is studied in detail. Additionally, the use of PCM memory cells in LUTs is explored. Then the

performance of PCM based memories is compared to currently used SRAMs and Memristors. Finally, this work is concluded in Chapter 7; with concluding remarks and proposed future work.

CHAPTER 2

PRELIMINARIES

2.1 Overview

In this chapter basic information that describe the current status of computer memory hierarchy are provided. The chapter starts in section 2.2 with main performance characteristics considered when evaluating a memory technology and structure. The current computer memory hierarchy and used memory technologies are explained in section 2.3. The most prominent emerging non-volatile memory technologies and their operation concepts are stated in section 2.4. Then a detailed description of PCM characteristics is provided in section 2.5.

2.2 Memory Performance Characteristics

The memory is an essential and integral part of modern computer systems architecture, which is used to store both data and software programs, for it to be later used by the processor [29]. There are different categories and classifications of memory types; that are often used within a single system. The main electronic memories categories are Volatile Memories (VM) and Non-Volatile Memories (NVM). As the name indicates; volatile memories lose stored data when the system is powered off, in contrast to their non-volatile counterparts which retain stored data for extended periods of time after the system is powered [29], [30]. However the volatility is not the only defining characteristic of a memory type, as the memory hierarchy in the computer system shown in Figure 2.1 is constructed of several layers of memories. Each memory layer has specific properties i.e. performance indices in accordance to the requirements of that layer.

The performance metrics used to describe a memory type are listed and defined as following:

a) <u>Retention Time</u>: The period during which the memory retains data stored in it after the system is powered off.

b) Read/Write energy: The energy required to read/write a single bit of data, it could be defined as the memory consumed per chip area.

c) Idle power: The energy consumed by the memory when it's not used i.e. idle.

d) Endurance: The number of program cycles that can be applied to the memory before the storage media becomes unreliable.

e) Access time: The time interval between the read/write request and the availability of data.

f) Read/Write latency: Time delay between the application of address and the availability of stable and accurate data on the data lines/memory cells.

g) Density (Capacity): The volume of information (in bits) that the memory can store

h) Cell size: The physical volume occupied by a single memory cell.

i) Temperature range: The range of temperature at which the memory can operate reliably.

j) Multilevel operation: The ability of a single memory cell to store more than a single bit of data.

It should be noted that a memory type does not possess all the desired performance characteristic; therefore trade-offs are made to support the main requirement of a specific system or memory type, e.g. some memories have longer retention times and higher capacities yet they require longer access times, while other memories trade the capacity for shorter access times [29]. Making the later suitable to be built in the processor; as it can keep up with its high operating speed; while the former is more suitable for external data storage system. Throughout this work read/write latency, read/write energy, and density will be the used metrics for performance comparison.

2.3 Traditional memory hierarchy

The depiction of modern memory hierarchy in Figure 2.1 shows how memory performance metrics i.e. latency, energy consumption and capacity are traded off at each level depending on the system requirements. For example, short access time and latency are needed in level 1 cache memory; since it is integrated in the Central Processing Unit (CPU) chip and must work at processor's speed. However, slightly longer latency and access time, and higher capacity are the performance metrics exhibited by caches at level 2.

The main memory is used to store programmes and data when they are active and used by the processor. The main memory copies its contents from the non-volatile archive memory residing at the bottom of the memory hierarchy, and loses the contents once the system's power goes off. As the main memory acts as a link between the two ends of the memory hierarchy it possess intermediate characteristics as well in terms of latency, density and energy consumption. The latency increases as we go towards the base of the memory hierarchy pyramid as seen in Figure 2.1, and the capacity increases and energy consumption decreases at the cost of increased latency towards the base where the archival storage containing software programmes and stored data [30]. In the following the characteristics of Static Random Access Memory (SRAM) used in cache memory, Dynamic Random Access Memory (DRAM) used in Main memory, and the Flash memory used as storage memory are discussed.

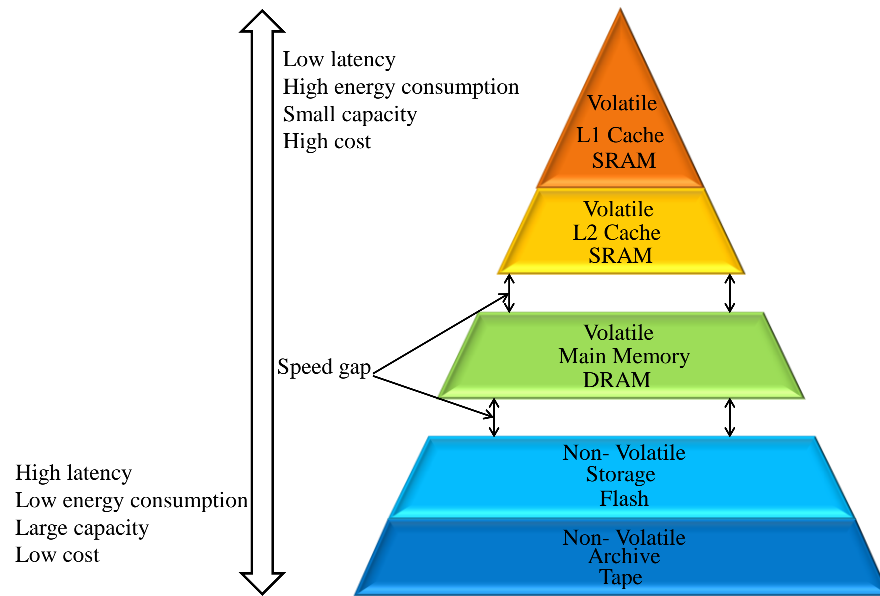

Figure 2.1: Traditional computer memory hierarchy [30]

2.3.1 SRAM

The SRAM is a high performance semiconductor memory constructed of six transistors. It is used for storing instructions in registers and caches of processors; due to its low latency as indicated in Figure 2.1. Thus SRAM low latency stated in Table 2.1, makes it suitable to provide data immediately to the CPU at its operating speed [30].Yet despite the high speed, it requires larger area per cell due to the six CMOS transistors constructing it.

2.3.2 DRAM

DRAM is a fast, power efficient semiconductor random access memory, with high endurance as indicated to in Table 2.1. DRAM is constructed of a single access transistor and a capacitor, and is used as main memory in computer systems. But since the main memory is separated from the CPU, an interface is required causing the DRAM energy consumption and delay to increase in comparison to SRAM [30], as seen in Table 2.1.

2.3.3 Flash memory

Flash memory is a non-volatile, highly scalable, and inexpensive semiconductor memory technology that is used at storage level. Flash memories have longer latency

and less endurance compared to SRAM and DRAM as noted from Table 2.1, but its high density makes it suitable to be used as external storage [30], [31]. The core concept of the traditional memory hierarchy shown in Figure 2.1 has evolved from the fact that high performance directly correlates with extra cost [30]. Therefore, the expensive high performance memories use is confined to places where it is critical for overall system performance. Moreover, critical computing applications are becoming more data-centric than compute-centric [32], which means they require larger memory space than ever. This leads to two key issues with the current memory hierarchy; i.e. the speed gap between memory hierarchy levels, and the increased power consumption due to increased memory density [31].

Table 2.1: Current memory hierarchy performance comparison [30]

Property	SRAM	DRAM	Flash
Read energy	-	0.8 J/GB	1.5 J/GB
Write energy	0.32µW [33]	1.2 J/GB	17.5 J/GB
Idle power	Cell leakage	Refresh power~100 mW/GB	1-10 mW/GB
Endurance	10^{16}[32]	10^{15}	10^4 - 10^5
Retention [34]	-	64 ms	>10 years
Read latency	1.23ns [35]	20-50 ns	~25 µs
Write latency	0.85ns [35]	capacitor charging time 20-50 ns	~500 µs
Density	-	1x	4 x
Power consumption	10.37 mW	10uA capacitor charging current	-
Cell size	>100F^2 [36]	6-8 F^2 [36]	10 F^2 [34]
Temperature range[34]	-	-40 – 85 ˚C	-40 – 150 ˚C
Multilevel	N/A	N/A	Available

From the issues faced by the traditional memory hierarchy, arose the need for a high-performance, high-density, and low-cost NVM technology; in order to improve overall system performance, and meet the demands of future storage server systems and consumer electronics market in terms of density and power. A class of memory that combines high speed and endurance of solid state memory such as SRAM, and archival memory low cost and high density, this class is called Storage Class Memory (SCM). SCM would bridge the speed gap in the memory hierarchy and solve the power consumption limitations [32]. Furthermore, having SCM will eliminate the need to store programs in non-volatile NAND then transferring them to volatile DRAM upon execution; by having the programs stored in non-volatile high speed SCM, hence providing high performance, low cost single chip solution [30].

2.4 Emerging resistive NVM

Emerging resistive switching memory technologies that can overcome the issues of traditional memory hierarchy, replace flash memories, and be the technology for storage class memory, are widely studied in technical literature [19], [31], [32], [34], [37]–[39]. These emerging NVM technologies possess desired properties as they offer low power consumptions, high operating speeds, long data retention, and high scalability leading to high density as indicated in Table 2.2.

The operating concept of resistive switching memories relies on the fact that the equivalent resistance of the memory cell can be controlled by applying external potential, leading to either chemically, magnetically, or thermally induced change of the cell resistance. The memory cell therefore can be in at least two resistive states. The resistive state of the memory cell can then be used to store binary data, where the relatively high resistive state corresponds to binary zero, and the relatively low resistive state represents binary one. Resistive switching memories include but are not limited to; Magneto-resistive RAM (MRAM), Phase change RAM (PCRAM),

Conductive Bridge RAM (CBRAM), Bi-Stable organic memory, Ferroelectric RAM (FeRAM), and Memristors. In the following the most prominent of these resistive switching memory technologies are described.

2.4.1 Resistive RAM (ReRAM) "Memristor"

Memristor is a two terminal non-volatile resistive memory structure that changes its instantaneous resistance known as memristance. The memristance changes according to the amount and direction of applied programming pulse. Where applied current controls oxygen ions and the formation of oxygen vacancies that lines up to create a conducting channel thus lowering the resistance of the memristor cell. Reversing the direction of applied current causes the oxygen vacancies conducting channel to collapse leading to increased resistance [40] as depicted in Figure 2.2.

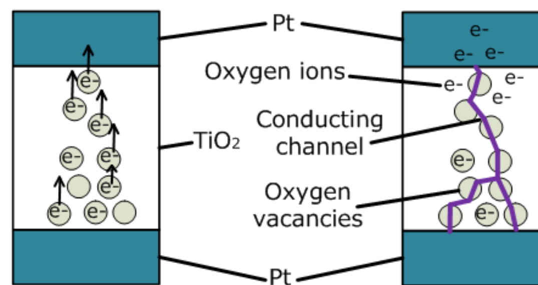

Figure 2.2: Cross section of memristor cell structure (high resistance "left", and low resistance "right")

2.4.2 Phase change memory (PCM)

PCM also referred to as PCRAM is a two terminal memory structure that is a promising SCM candidate. The operation concept of PCM relies on the material's thermally induced phase change property; in which the material changes its atomic structure from highly disordered, highly resistive amorphous structure to ordered low resistive crystalline state. Typical phase change materials are chalcogenides, such as $Ge_2Sb_2Te_5$ (GST) [30]. The phase change material layer is sandwiched between two electrodes as shown in Figure 2.3; and when current passes through the heater it

generates heat due to the Joule effect, this heat transfers to the phase change layer inducing the structure change [41].

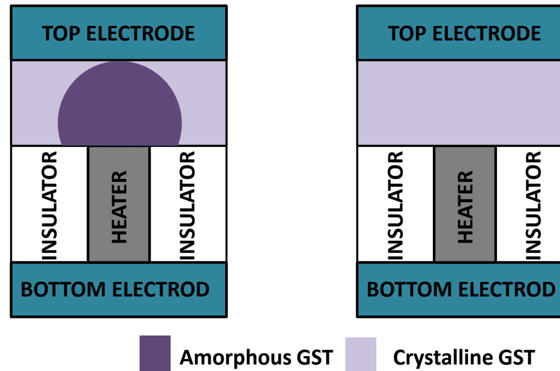

Figure 2.3: Cross section of PCM cell structure (high resistance “left”, and low resistance “right”)

2.4.3 Magnetic Tunnel Junction (MTJ)

A traditional Ferro Electric Random Access Memory (FeRAM) cell is a two terminal structure that consists of two ferromagnetic plates separated by a thin insulating layer as illustrated in Figure 2.4. This structure is known as a Magnetic Tunnel Junction (MTJ). The lower plate is set to a fixed polarity, while the polarity of the upper plate is free and can be switched by controlling the applied programming pulse. The electrical resistance of the memory cell changes depending on whether or not the polarity is aligned between the two plates [19]. If the magnetic polarization of the two layers is aligned, the resistance through the MTJ is low relative to the resistance when they are misaligned [30].

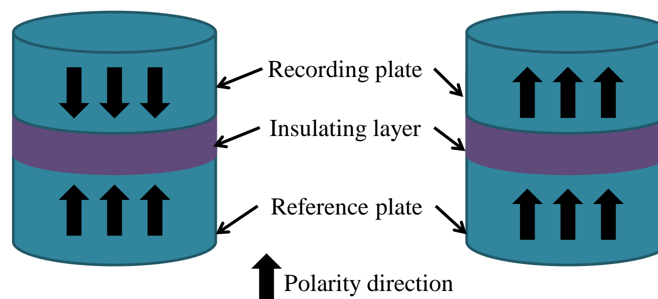

Figure 2.4: MRAM cell structure (high resistance “left”, and low resistance “right”)

2.4.4 Emerging NVMs performance comparison

The above discussed emerging resistive NVM share the storage mechanism concept i.e. resistive storage concept, which leads to non-volatility, in contrast to charge storage in volatile transistor based Random Access Memories (RAM). However resistive NVM technologies demonstrate different performance characteristics which are outlined in Table 2.2.

Table 2.2: Emerging resistive NVM technologies performance comparison [31]

Performance index	PCM	FeRAM	ReRAM
Cell size	4- 19 F^2	15- 35 F^2	6-10 F^2
Operation voltage	1.5 – 1.8 V	1.8V	3.3 – 6.5 V
Write current	10^{-4} A	10^{-6} A	10^{-4} A
Write latency	100ns	<10ns	50ns
Read latency	<5ns	<5ns	<5ns
Retention	>10 years	>10 years	>10 years
Endurance	10^9 - 10^{12}	10^{13}	10^6

As noted from Table 2.2, PCRAM shows better performance in comparison to ReRAM in all performance metrics excluding write latency. It is due to the fact that in PCRAM, the resistive change depends on thermally induced structural change in the material used. This requires longer delay compared to magnetic and chemical changes in FeRAM and ReRAM respectively. Furthermore, looking at PCM performance characteristics from Table 2.2 and comparing it to traditional memory structures i.e. SRAM, DRAM, and Flash memory from Table 2.1, it is noted that PCM shows superior performance characteristics. PCM performance surpasses Flash memory in all performance metrics, and only lags in comparison to DRAM and

SRAM in terms of writing latency; an issue that is addressed in technical research. Moreover, when comparing the PCM specifications to the targeted specification of storage class memory listed in [32], it is noted that it fulfils the requirements making it a strong candidate to fill in as the technology for storage class memory.

2.5 PCM characteristics

2.5.1 Materials

PCM technology relies on the phase change process displayed by chalcogenide materials; which are chemical compounds consisting of at least one chalcogen element, i.e. sulphur (S), selenium (Se), or tellurium (Te), in combination with other elements. In this research the focus is on germanium antimony telluride ($Ge_2Sb_2Te_5$) referred to as GST.

Most phase-change materials are chalcogenides, containing at least one element from group VI of the periodic table. This due to the fact that group VI elements form pre-dominantly twofold-coordinated covalent chemical bonds that can produce linear, tangled, polymer like clusters in the melt. These clusters lead to an increase the viscosity of the liquid, inhibiting the atomic motion necessary for crystallization [42]; thus preventing the amorphous phase from spontaneously crystalizing, a necessary feature in using PCM as resistive storage system.

GST is the most commonly used and most widely studied phase change material, due to its more established previous application in optical storage systems. Yet it should be noted that the properties required in materials used in optical storage differ from the properties required in resistive storage systems. Possessing desirable properties for optical storage does not necessary make the material suitable for resistive storage. For resistive storage applications, phase change materials are desired to have fast crystallization speeds to minimize programming delays, crystallization temperatures that are well above the operating medium temperature to

insure reliability, and relatively low melting temperature to minimize programming power consumption. A large $R_{amorphous}/R_{crystalline}$ ratio is also desired to facilitate a reliable read process and permit multilevel operation in order to increase density. High cyclability, endurance, and CMOS compatibility are as well much desired properties in resistive storage phase change materials. With all these requirements in mind phase change materials are studied and their properties are evaluated to decide the most suitable materials for resistive non-volatile memory application [42].

Experimental studies [43] showed that within the class of GeSbTe ternary alloys; compound materials along the pseudo-binary GeTe-Sb_2Te_3 tie-line (e.g. $Ge_2Sb_2Te_5$, $Ge_1Sb_2Te_4$, $Ge_1Sb_4Te_7$), as shown in Figure 2.5, have fast crystallization properties. While GeSbTe materials demonstrated nucleation dominated crystallization process; silicon antimony telluride (SiSbTe) showed growth dominated crystallization making it faster in terms of programming delay. In addition SiSbTe demonstrates better data retention in comparison with GeSbTe. With archive lifetime of SiSbTe being about twice as long as that of GeSbTe [44].

Many other compounds have been developed, tested, analysed and further improved by doping, thus widening the array of materials that can be used as phase change materials in resistive memories. The developed materials include Ge-Te, AgSbSe2, Sb-Se, Ag-In-Sb-Te, and other Sb-Te variants. Along with a wide variety of dopants including elements of the 13th and 14th columns of the periodic table e.g. carbon (C), tin (Sn), indium (In), aluminium (Al), silicon (Si), germanium (Ge), nitrogen (N), and oxygen (O); because they enhance the operation characteristics, i.e. melting temperature, crystallizing temperature [42].

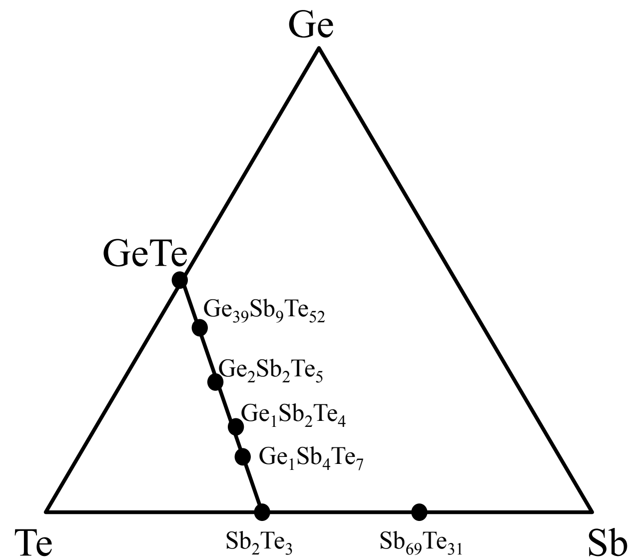

Figure 2.5: Phase diagram of the Ge-Sb-Te ternary alloy system

Adding dopants was experimentally studied [43], [45], [46], to evaluate the effect of adding nitrogen (N) and oxygen (O) on phase change properties. It was found that when adding oxygen to GeSbTe thin films, the oxygen acts as nucleation centre in crystallization process, minimizing the nucleation time in comparison to undoped GeSbTe films [45]. Moreover, it was noted that when doping $Ge_2Sb_2Te_5$ with nitrogen; the material endurance is improved as a result of increased activation energy [46]. Furthermore, different capping materials were tested [47], including silicon oxide (SiO_2) , aluminium oxide (Al_2O_3), germanium oxide (GeO_x), antimony oxide (SbO_x), titanium nitride (TiN) and Al. It was concluded that the use of SiO_2 and GeO_x as capping materials accelerates the recrystallization rate of GeSbTe substantially and increases crystallization temperature.

2.5.2 Operating principles of PCM

Data storage in PCM depends on the thermally induced phase change property in Chalcogenides (GST in this work); the material can exist in at least two phases; highly resistive amorphous and low resistive crystalline, where the latter phase represent (one) and the former represent (zero) in binary system.

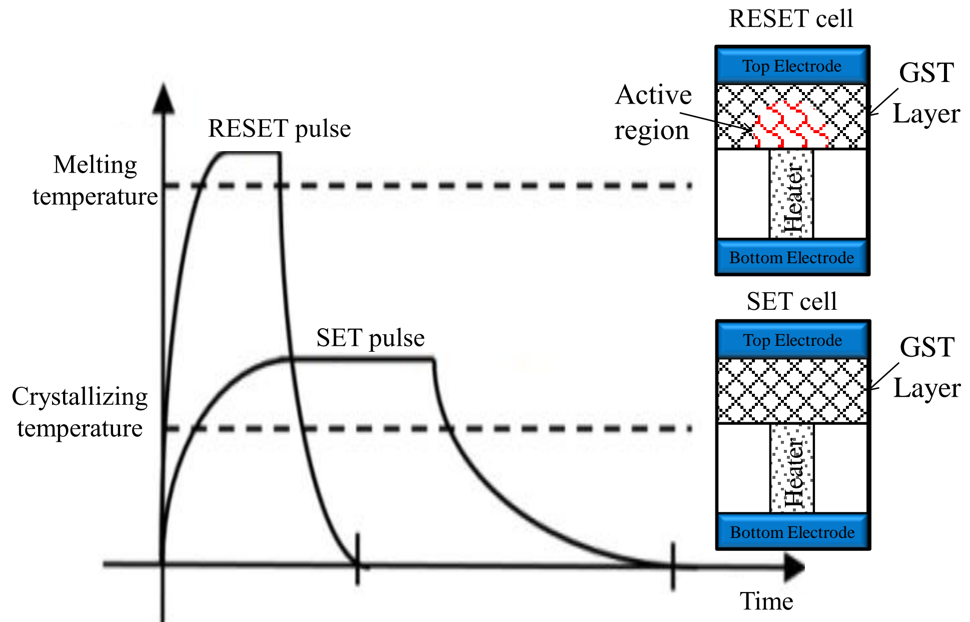

Figure 2.6: Temperature dependence of the phase change process

The material phase change from crystalline to amorphous is referred to as RESET process. During RESET process the PCM cell is heated by a current pulse above GST melting temperature (600˚C) utilizing the Joule effect. The material is then rapidly quenched before it rearranges back to crystalline state, hence keeping it at a distorted amorphous phase. Similarly, the phase change from amorphous to crystalline is referred to as SET process. In the SET process the PCM cell is heated slightly above GST crystallization temperature (≈200˚C) and well below its melting temperature as seen in Figure 2.6, for duration sufficient for the phase change material in active region to rearrange its atoms back to crystalline ordered state.

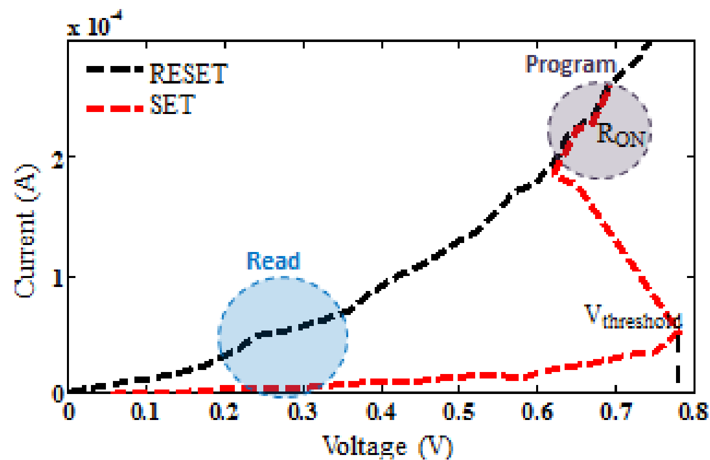

Figure 2.7: I-V characteristics of PCM cell

I-V characteristics shown in Figure 2.7 display the steady state response of a PCM cell. The steady state response gives an insight into the atomic transitions the PCM cell goes into when it is being programmed, i.e. SET from initial amorphous state into crystalline state, and RESET from initial crystalline state into amorphous state. After a RESET process the cell goes into a recovery stage before it reaches the final high resistance state. In the following the programming of PCM cells i.e. RESET and SET processes and the accompanying recovery transient are explained, along with the subthreshold regime and the characteristic snap back behaviour of PCM cell I-V characteristics as seen in Figure 2.7.

2.5.2.1 RESET process

When the material is initially crystalline as seen in crystalline curve in Figure 2.7, its resistance is relatively small and the current passing through the cell leads the temperature increase due to Joule effect. To programme the cell into the amorphous state i.e. to RESET the cell, a high steep programming current pulse is applied; causing an excessive presence of charge carriers. This creates a highly conductive dynamic ON state with even lower resistance (R_{ON}) as shown in Figure 2.7. This allows sufficient current to heat the cell above melting temperature and program the cell.

2.5.2.2 Recovery behaviour

It is noted from experimental results in technical literature [48], [49] that when a PCM cell is RESET i.e. programmed into amorphous highly resistive state, it does not immediately reach the targeted resistance level after programming. Rather a transient resistance that is lower than the targeted value appears directly after programming. The cell resistance then exponentially increases to reach the targeted resistance as seen in Figure 2.8. This transient behaviour is referred to as the recovery behaviour, and it was experimentally calculated in [48] by measuring the I-V characteristics at several points in time after programming as depicted in Figure 2.9. The corresponding cell resistance and threshold voltage are extracted from the

captured recovery behaviour. The experimentally observed recovery time for the cell's resistance to increase from R_{ON} (typically few KΩ) up to the targeted amorphous resistance was found to be about 30ns [48]–[50].

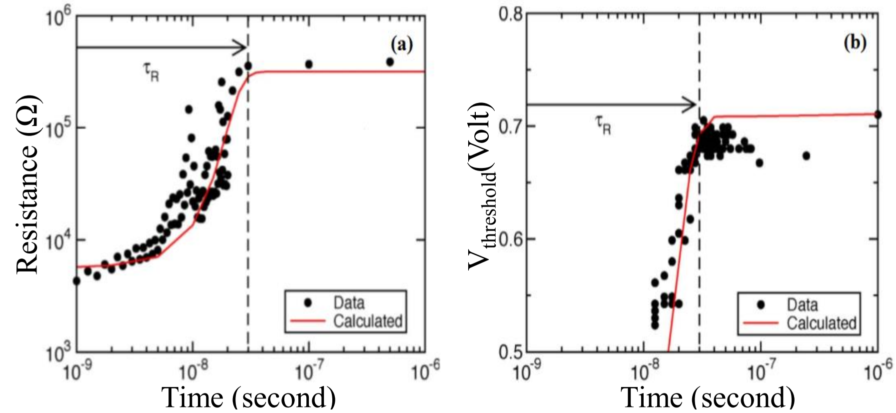

Figure 2.8: Cell (a) resistance and (b) threshold voltage as a function of time after programming [48]

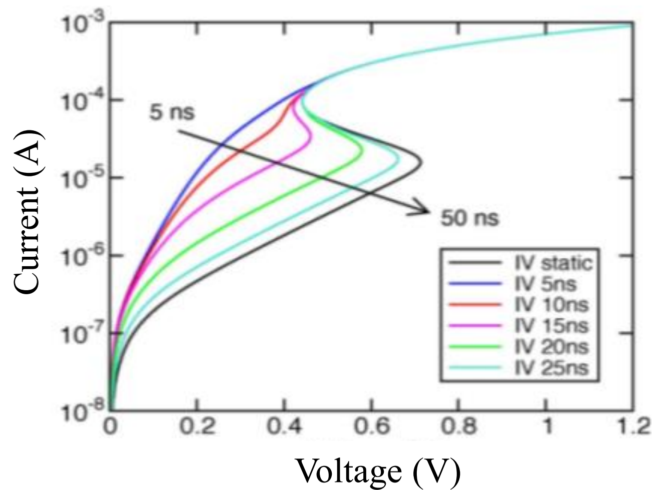

Figure 2.9: Calculated I–V curves for PCM devices at increasing time after reset, indicating the recovery dynamics[48]

The recovery behaviour is explained by the substantial concentration of excited carriers that are still at high energy states and elevated temperature within the cell immediately after programming. Thus resulting in lowered resistance, which gradually increase during the electronic relaxation time of carriers relaxing to low energy states, and the thermalization time needed for the excess thermal energy to diffuse [48], [50].

The impact of the recovery effect on device operation is significant in terms of reading speed [48], [51], as equilibrium must take place before reading can be carried out; in order to read accurate data. And if reading bias is applied before the equilibrium is achieved i.e. when the threshold voltage is substantially smaller; unintended programming may take place. Furthermore, read failures may occur due to lowered cell resistance, therefore the recovery time should be considered as the minimum waiting time after programming, to perform reading process.

2.5.2.3 SET process

The transition from amorphous to crystalline phase i.e. the SET process requires increasing the temperature of GST layer in the cell to its crystallizing temperature as shown in Figure 2.6. This is done by utilizing Joule heat effect; where the programming current that passes through the resistive material generates heat. It should be noted that at the amorphous phase, the resistance is considerably high. Therefore, to allow programming currents to flow and elevate the temperature to crystallization temperature; the resistance needs to be lowered. This lowering of resistance is an intrinsic property of GST chalcogenide alloy and is referred to as the Ovonic threshold switching as it was first proposed by Ovshinsky in the early 1960's [1], and the PCM at the time was also known as Ovonic Unified Memory (OUM).

The ovonic threshold switching takes place when a voltage higher than the threshold voltage ($V_{Threshold}$) is applied across the cell. Causing the resistance of the amorphous material to drop to a highly conductive state referred to as the dynamic ON state seen in Figure 2.7, while maintaining the amorphous structure. This allows sufficient current to pass through the cell, and cause the snapback behavior depicted in Figure 2.7 and Figure 2.9. If this current is maintained for a duration that allows the crystallization process to take place the ovonic memory switching occurs; which is the change of the material from amorphous to crystalline phase. The ovonic

memory switching is a structural change in contrast to the ovonic threshold switching which is mainly an electronic state of excess carriers which will be explained in the coming section.

2.5.2.4 Subthreshold regime in SET process

The subthreshold segment of initially amorphous cell I-V curve as shown in Figure 2.10 shows three distinct voltage dependencies on current. It begins with a linear ohmic relationships, then progresses into exponential dependency with increasing voltage, and finally becomes super exponential before threshold switching occurs [52].

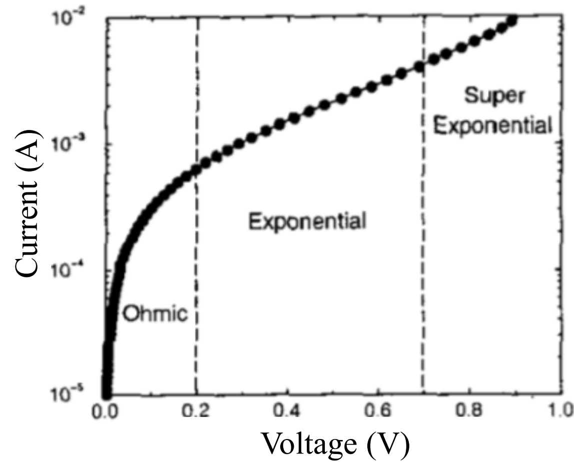

Figure 2.10: Subthreshold I-V characteristic of amorphous phase [52]

Poole-Frenkel analytical model of conduction was used to explain this subthreshold behaviour of amorphous GST [53], [54]. Where the current through the cell in the reset state is given by (2-1), where N_{tot} is the total trap density in the mobility gap above the Fermi level E_F. A is the contact area; τ_0 is the characteristic electronic attempt-to-escape time. Δz is the average distance among Coulombic traps. E_C is the mobility edge for the conduction band. V is the voltage across the amorphous chalcogenide region, and u_a is the thickness of the amorphous region.

$$I = 2qAN_{tot}\frac{\Delta z}{\tau_0}e^{-\frac{E_C-E_F}{k_BT}}\sinh\left(\frac{qV}{k_BT}\frac{\Delta z}{2u_a}\right) \tag{2-1}$$

The Poole Frenkel conduction equation (2-1) if used, can justify the voltage dependence of the subthreshold current in both the linear and exponential parts of the I-V curve due to the hyperbolic-sine term, however, it does not explain the threshold switching phenomenon [54].

2.5.2.5 Threshold Switching (Snapback)

The voltage snapback behaviour in the amorphous to crystalline transition; was attributed to the occurrence of various physical models including Impact Ionization, Field-assisted electron hopping, and Competing generation and recombination rates to reach equilibrium [55]–[57]. The competing behaviour of impact ionization, and generation and recombination of carriers, was depicted by [52], [55], explaining that at low field in amorphous phase, the conduction is ohmic as seen in Figure 2.10. But with increasing bias beyond a critical value; the impact ionization takes place, where electrons excited by bias fill up the acceptor like traps i.e. recombination takes place.

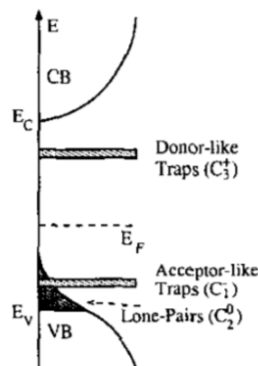

Figure 2.11: Amorphous GST band model [52]

The traps are a result of structural defects in tellurium (Te-Te) chains in GST amorphous hemisphere leading to acceptor/donor pairs of traps [58] as shown in Figure 2.11. With impact ionization taking place; current across the cell increases exponentially. With further increased bias; the structural defect spawned traps are filled with increasing free electron density, hence moving the Fermi level closer to the conduction band, and eventually the excited electrons fill up all the traps and the

carriers' recombination ceases leading to snapback behaviour. At snapback point, a lesser voltage lead to higher current flow due to increased free carriers' density, translating in a lower resistance state referred to as the dynamic ON state.

The lowered resistance at this point is attributed to an electronic mechanism, and is not a result of a structural change. The programming can only occur after this point, i.e. if the applied bias is maintained at sufficient amplitude for an adequate duration, a structural transformation i.e. crystallization will take place. This crystallization process is referred to as the Ovonic Memory [8], [56], [58].

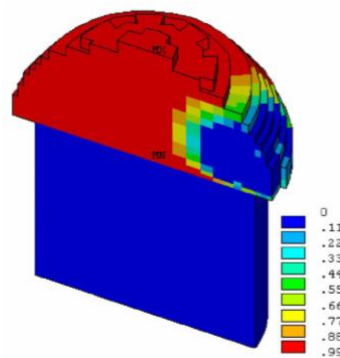

Figure 2.12: Hot filament formation in amorphous GST

Other works attributed the snapback behaviour to thermal effects rather than electronic ones. As suggested in [59] that the snapback is a result of thermal run away. It is assumed that a defective amorphous cap (active region) residing within a crystalline layer can provide through the defects a crystalline filament "tunnel". This tunnel forms through the shortest possible current path between the bottom electrode and the crystalline GST as shown in Figure 2.12. Thus leading to high current density, and elevated temperature at the defected area. With such elevated temperature, and due to negative temperature coefficient; lower resistivity and higher current density are demonstrated leading to the characteristic snapback effect. But given that the threshold switching speed is faster than the thermal time constant, electronic mechanisms are favoured over purely thermal mechanisms [41].

2.5.2.6 Multilevel programming

In multilevel (ML) phase change memory operation; each cell can be programmed up to N resistance levels (including fully set, fully reset and intermediate states) and store $\log_2 N$ bits, allowing an increased storage density, hence lower cost-per-bit. The multilevel operation mode is the most attractive feature of PCM [12], [13], [60], [61] and is essential for enhancing PCM technology competitiveness in the market [14].

Multilevel operation is achieved by programming the phase change material into intermediate states between the two corner (fully crystalline and fully amorphous) states. To program into intermediate levels two general approaches are used; i.e. partial crystallization and partial amorphization; in the former method the intermediate levels are reached by crystalizing a fully amorphous volume with varying pulse durations, given that the crystalline part is actually percolation paths that increase in diameter with longer pulses; thus pulses with longer durations result in smaller resistances. While in the former approach a fully crystalline material is partially amorphized by controlling the programming pulse amplitude, given that pulses with higher amplitudes melt amorphous caps with larger radiuses, thus higher resistance [62], [63]. The partial crystallization approach was adopted in this work.

2.5.2.7 Read process

To read the data in a PCM cell storage, a reading voltage pulse with small amplitude is applied across the electrodes of the cell and the amount current that passes across the cell defines the cell's resistance hence bit value. However, it should be taken into consideration that the reading voltage must be well below the threshold voltage to avoid read disturbs, and well after programming taking into account the recovery time; to avoid any read errors.

2.5.3 Crystallization of PCM

2.5.3.1 Nucleation and growth (Classical nucleation theory)

GST alloys experimentally displayed multiple phase transitions [64], [65], i.e. at 120-170˚C a transition from amorphous to metastable rock salt structure occur. Continuous heating to 200-250˚C causes transformation to a stable hexagonal crystalline phase; while at temperatures of 593-630 ˚C melting occurs. The two crystalline phases coexist during crystallization process [64]. Below crystallization temperature the material is identified as the crystalline $Ge_1Sb_4Te_7$ and above that temperature it transforms to face centered cubic (FCC) $Ge_2Sb_2Te_5$ crystals, as seen in Figure 2.13. This is derived from experimentally obtained impedance of the tested sample and using Bruggeman model. Bruggeman model is a model that states that the microscopic properties of a composite can be derived by averaging the values of the properties of the constituting elements [65].

The coexistence of the two phases thus indicates that the crystallization process follows subsequent nucleation "the generation of crystallization centers" and growth "of crystal clusters" mechanisms, following the classical nucleation theory. Where $Ge_1Sb_4Te_7$ nuclei form at lower temperatures, and the nuclei fraction decreases with increasing temperature at which growth of stable $Ge_2Sb_2Te_5$ crystals takes place as seen in Figure 2.13. A maximum nucleation rate is predicted at a temperature between the glass transition and the melting point, as stated by the classical nucleation theory [65].

The phase change materials can be classified into: nucleation dominated or growth dominated material depending on the nucleation and growth rates. If the nucleation rate of a material is higher than its growth rate, the material is considered nucleation-dominated material. And if the nucleation rate of a material is lower than its growth rate, the material is considered growth-dominated material. GST was found to exhibit nucleation dominated crystallization process [44], [66]–[68]. Moreover, the

established temperature dependence of nucleation and growth rates, i.e. I and V_g respectively, was found to be governed by (2-2) and (2-3) [69], [70].

$$I = \alpha_1 \exp\left(\frac{-Q_1}{RT}\right) \exp\left(\frac{-\Delta g^*}{RT}\right) \quad (2\text{-}2)$$

$$V_g = \alpha_2 \exp\left(\frac{-Q_2}{RT}\right) \left[1 - \exp\left(\frac{-\Delta g}{RT}\right)\right] \quad (2\text{-}3)$$

Where *Q1* and Q2 are activation energies for nucleation and growth respectively, Δg is the formation energy of crystallization, Δg* is the free energy required to form a critical nucleus. And *α1,* α2 are constants.

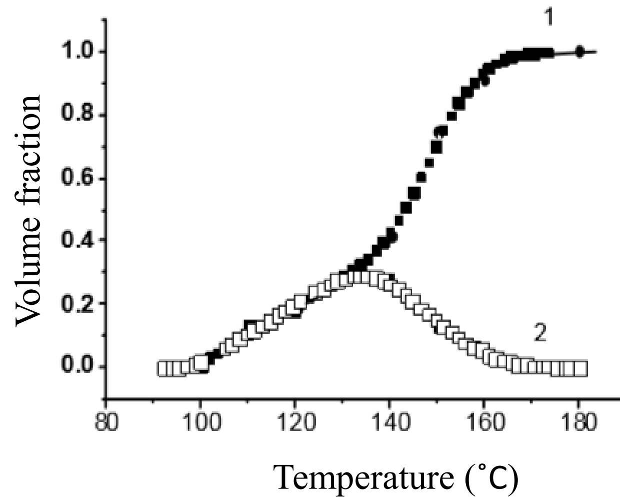

Figure 2.13: Crystalline volume fraction (Solid) and the nuclei volume fraction as a function of temperature [65]

2.5.3.2 Wright's theory

Wright et.al developed a theory of the crystallization process of GST based on the nucleation theory of liquid droplets "crystalline material" from supersaturated vapor "amorphous material" [71]. Given that when the amorphous material is heated the GST film relaxes via atomic reordering creating crystalline embryos with less free energy. These embryos then condense or evaporate creating crystalline clusters. Once these clusters exceed the critical radius r_c they will not dissolve by removing the heating pulse.

To overcome the energy barrier between amorphous and crystalline states in order to create the crystalline clusters; the concentration of embryos has to be larger than the supersaturation concentration based on this theory [71]. The supersaturation S from (2-5) physically quantifies the ratio of the density of basic embryos (N_1) normalized to the value at saturation ($N_{1,sat}$). When the basic embryo density exceeds the saturated value i.e. S>1, crystallization becomes possible. The free energy barrier between amorphous and crystalline is given by (2-4)

$$\Delta F = 4\pi r^2 \sigma - \frac{4\pi r^3}{3} \rho R ln(S) \tag{2-4}$$

where σ, ρ, R and S; are the surface free energy, crystalline density, gas constant and supersaturation respectively. Given that

$$S = (\frac{N_1}{N_{1,sat}}) \tag{2-5}$$

To achieve crystallisation; the energy barrier needs to be lowered, i.e. S>1 nuclei with radius $r>r_c$ are energetically favoured to grow and produce crystallites. While nuclei with $r<r_c$ will tend to reduce in size. On the other hand, if $S\leq 1$; free-energy increases with radius and stable nuclei cannot form, the crystallization is therefore impossible. The critical radius r_c is given by (2-6).

$$r_c = 2\sigma/\rho RT ln(S) \tag{2-6}$$

The rates at which the crystalline clusters condense and evaporate are both temperature (T) dependent as stated by the classical nucleation theory. Both rates competing behaviour can be described by the master equation from nucleation theory using numerical simulation [71].

2.5.3.3 The Johnson-Mehl-Avrami-Kolmogorov equation

JMAK equation was derived by Kolmogorov [72] and later by Johnson and Mehl [73] and Avrami [74], hence their initials were used when referring to the equation in literature. The equation describes how solids transform from one phase (state of

matter) to another at constant temperature. JMAK equation is based on three assumptions:(1) a random distribution of potential sites of nucleation, (2) instantaneous nucleation, and (3) interface-controlled grain growth and time independent growth rate [75]. This equation is frequently used in PCM models to calculate the crystalline fraction, given that the fraction transformed is the ratio of the crystalline volume to the total volume of phase change material.

The derivation of JMAK starts with the assumption that the nuclei are randomly distributed in space; and the volume that each crystallite can grow into is decreased from the total in proportion to the fraction that has already transformed. The JMAK equation facilitates a quantitative relation between the impingement influenced transformed volume f (2-7), and the extended impingement free volume f^{ext} (2-8). The extended impingement free volume f^{ext} includes the overlapping areas, thus the equation compensates for the impinged areas overlooked in extended volume as seen in Figure 2.14.

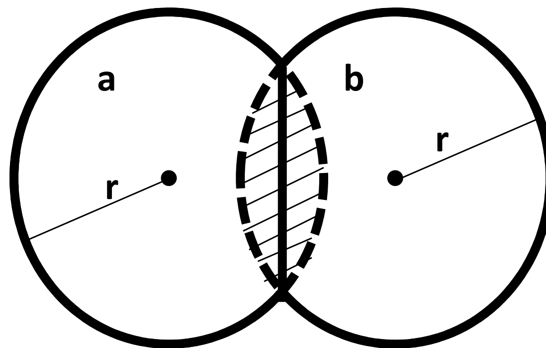

Figure 2.14: impingement influenced growing crystallite "solid line", and impingement free extended volume "dotted line"

The full derivation of the JMAK equation (2-9) can be found in Appendix 2-1.

$$f = \frac{V_a \cup V_b}{V_{total}} \qquad (2\text{-}7)$$

$$f^{ext} = \frac{V_a + V_b}{V_{total}} \qquad (2\text{-}8)$$

$$f = Kt^n \quad (2\text{-}9)$$

Where f is the transformed fraction, t is time, n is the Avrami coefficient, and K is the pre-exponential factor that is described by Meyer-Neldel rule in the following section.

2.5.3.4 Meyer-Neldel (MN) rule

The Meyer-Neldel rule is an empirical law that evaluates the dependence of the conduction activation energy on various conduction parameters, including but not limited to pressure, bias, and temperature [76]. The rule applies to a wide range of materials including inorganic semiconductors along with chalcogenides which are the materials of interest in this work. Therefore, the pre-exponential factor in (2-9) K can be evaluated based on Meyer-Neldel rule as a temperature dependent value [75]. Meyer-Neldel equation (2-10) describes the linear relation between the pre-exponential factor K and the temperature dependent activation energy E_A [77].

$$K(T) = v\exp(-\frac{E_A}{k_B T}) \quad (2\text{-}10)$$

$$v = v_0\exp(\frac{E_A}{E_{MN}}) \quad (2\text{-}11)$$

Where E_{MN} is the Meyer-Neldel energy, v is the frequency factor and v_0 is a true constant and k_B is the Boltzmann constant.

JMAK equation has been criticized by researchers due to the inconsistent values of the equations constants reported in literature; i.e. Avrami coefficient n values found in the range of (1 –5.8), E_A in the range of (0.8–2.9 eV), and v in the range of (10^{17}-10^{24}). This reported discrepancy was attributed to different deposition methods and crystallization processes, it was also suggested that for the same cell the Avrami exponent n does not remain constant during the crystallization process [64], [75].

Moreover, the reported non-integer values of the Avrami coefficient n where attributed to violations of the assumptions upon which the theory was based; where the Avrami coefficient represents Euclid dimensions (n = 1, 2, 3) [75]. Based on that it was concluded that the equation overcorrects for the extended volume as referred to in [78]. Yet the work in [78] derived the JMAK equation without relying on the concept of extended volume; proving the validity of the equation by considering only the time-dependent untransformed volume rather than the questioned extended volume. Furthermore, the work in [75] presented an extended version of JMAK where a fractal concept on space dimension was introduced; attributing the non-integer values of the Avrami coefficient to the expected complex fractal shapes of the crystalline grain surfaces.

The JMAK equation can be further used to describe the nucleation and growth theory; if the incubation time was included in the equation. The incubation time τ is the time needed for crystalline nuclei to reach critical radius r_c at which it cannot dissolve if the heat was removed. The incubation time was included in JMAK in [69] by subtracting the incubation period from the time of growth; hence making the actual crystal volume grow after the nucleation process has completed, in agreement with the theory. Hence the time dependent volume of the crystallite V(t) (2-12) becomes V(t- τ) (2-13); where v is the growth rate (speed).

$$V = \frac{4\pi}{3}(vt)^3 \tag{2-12}$$

$$V(t-\tau) = \frac{4\pi}{3}v^3(t-\tau)^3 \tag{2-13}$$

It was also suggested that at the beginning of the growth process the growth is three dimensional [69]. And once the crystal reaches the interfaces; the growth cease in one of the dimensions making it two dimensional growth processes, at which the volume can be described by (2-14), where h is the thickness of the film.

$$V(t-\tau) = \pi h v^2 (t-\tau)^2 - \frac{\pi}{12} h^3 \quad \text{(2-14)}$$

Incubation time can be calculated empirically; according to [75] when the annealing temperature is high the incubation time would be short and it becomes reasonable to ignore the incubation time.

2.5.3.5 Parameters affecting crystallization process

Material physical and chemical properties along with fabrication methods affect the crystallization process in terms of crystallization duration needed. In the following these parameters and their effects are listed.

a) Thickness: Incubation time dependence on thickness of the material relies on the deposition method. It is found to be proportionally related to the thickness of the as deposited amorphous GST, while it is inversely proportional to the thickness of melt quenched GST [47].
b) Doping: Doping GST by oxygen decrease the nucleation time and increase the crystallization rate compared to pure GST films. While doping with Nitrogen decreases the crystallization rate; [46] additionally the crystallization ability increases when the concentration of the metallic element (Sb) increases [45].
c) History/priming: The recrystallization of melt quenched material takes less time and temperature than that of as deposited amorphous material. An initial priming pulse would generate embryos that work as crystallization centres for subsequent crystallization processes by other pulses.
d) Programming pulses: Based on experimental results [71], there is a peak temperature at which embryo generation reaches a maximum. Programming the cell with a sequence of pulses rather than a single pulse means that the material will reach the peak temperature more than once increasing the number of embryos generated thus speeding the crystallization process [19], [79].
e) Capping layer: Capping materials can act as crystallization promoters. The effect of different interfaces on the crystallization process was studied in [47]. It was

found that using Al_2O_3 in 30 nm thick GST acted as a crystallization promoter leading to the short crystallization periods compared to other capping materials i.e. (GeO_x, SbO_x, SiO_2, Al and TiN).

2.5.4 PCM device optimization

The PCM device design is continuously optimised in order to increase density and reduce power consumption of the device i.e. programming current [11], [80]–[84]. Design optimisation goals are achieved by both (1) scaling the phase change material active volume, and (2) scaling the heater and electrodes diameter in the cell structure by controlling the structure design. Scaling on memory array level has further effects which include lowered cost per bit due to increased density. And the reduction of thermal disturbs due to cell to cell pitch in the array [85] that increases the stability in terms of interface reliability.

2.5.4.1 Scaled material behaviour

In order to fully utilize scaling benefits, the behaviour of the scaled material should be thoroughly considered when attempting to scale PCM material volume. Given that scaled particles - especially nano scaled ones- behave differently from bulk material and demonstrate different physical properties. In the case of scaled down PCM cells, the properties that needs to be verified are the crystallization and melting temperatures [42], which effect the individual cell behaviour and the reliability of its operation in an array structure.

Scaled material properties were tested ; to insure that phase change behaviour still occurs at minimized [11], [42]. Thin films i.e. one dimensional (1D) scaling “down to 18-nm”, nanowires i.e. two dimensional (2D) scaling “with diameters ranging from 20nm to 200 nm”, and nanoparticles i.e. three dimensional (3D) scaling “of diameters ranging from 1.8nm – 3.4nm were tested.

In terms of scaling the material volume, no fundamental limitations of phase change and electrical properties were exhibited, and the nanoparticles were found to be stable in amorphous states at room temperature [11]. Furthermore, experimental results [42] showed that the melting temperature for 2D scaled nanowires was less than that of bulk material, while the crystallization temperature of 1D scaled thin films was more than that of the bulk material.

2.5.4.2 PCM cell structures

PCM cell structures design optimization aims to reduce programming current by (a) controlling the heater and electrode contact area [41], and (b) thermal confinement of the heat generated by programming current [81] to increase its efficiency.

The cell structures that utilize contact area reduction include the mushroom cell, µ Trench structure [80], [86], ring-shaped contact [87], and the bridge cell [88]. However, the contact area is limited by the lithography and fabrication process; therefore lithography independent structures such as pore structure [89] are explored as well. Confined cell structures [81] were as well explored where the phase change material is thermally confined to minimize loss of heat and decrease required programming current by increasing its efficiency.

Among all available PCM cell structures in technical literature, the mushroom cell structure demonstrate favourable scaling because the effective thermal resistance scales inversely with contact area even though it is limited by lithography and process capability [41].

2.5.4.3 Mushroom cell scaling optimization

In technical literature [42], [84], [85] two methods of scaling mushroom cells were found; i.e. isotropic and non-isotropic scaling. The scaling process usually optimizes the heater/contact diameter (Φ) and thickness (L_h), and the thickness of the phase change layer (L_c) in order to maximize the temperature provided by a given

programming current, thus minimizing the required programming current. The optimum scaling corresponds to that geometry where the electrical and thermal resistances of the heater and of the chalcogenide layer are almost comparable to each other. At that optimum the temperature maximum is located at the bottom contact interface as shown in Figure 2.15 (b), thus utilizing the applied programming current to the fullest [85].

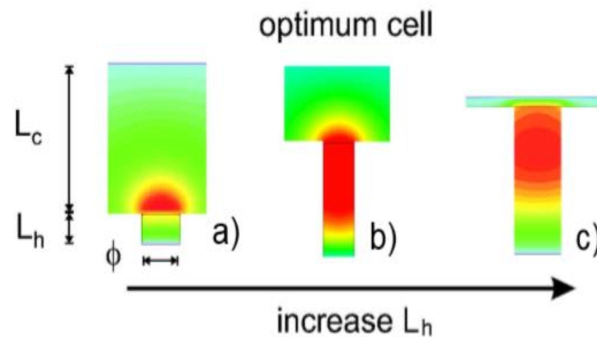

Figure 2.15: scaling optimization

It was found that isotropic scaling of all dimensions offers reliability in terms of thermal crosstalk in memory cells array since the temperature profile is also scaled. On the other hand non-isotropic scaling provides a faster decrease in programming current hence minimizing energy consumption, but it also causes and increase in programmed resistance thus degrading the readout reliability [85].

An optimization of scaling has been studied in [85] in which a hybrid of both types of scaling is applied. The cell is first non-isotropically scaled down to the point where further scaling may cause thermal disturbance. This first non-isotropic scaling allows for maximum current reduction, still complying with the program-disturb reliability requirements. Then, the cell is further scaled down according to the isotropic procedure, which guarantees the absence of thermal disturbance.

Another approach in enhancing energy consumption and density was scaling the electrodes size by the use of carbon nanotubes as electrodes; with this approach a remarkable reduction of programming current was achieved [42].

2.5.5 Reliability issues of PCM

Reliability issues of phase change memory array studied in technical literature are associated with retention and endurance issues. Retention is defined as the PCM cell ability to maintain originally stored data, without any unintentional alterations in its value. Endurance is defined as the ability of the PCM cell to retain its operational characteristics and avoid degradation with repetitive cycles of use. Endurance related reliability failures in PCM include permanent low resistive state which is referred to as stuck set, and permanent high resistive state referred to as stuck reset. While retention related reliability failures range from read disturb and thermal crosstalk to drift issues. In the following each of these is discussed.

2.5.5.1 Endurance associated reliability issues

a) Stuck set: occurs when GST based PCM cell is stuck at a low resistance crystalline state referred to as set state. The applied current fails to program the cell to the amorphous phase; due to either elemental segregation or material contamination. Elemental segregation lead to agglomeration of Antimony (Sb) atoms near the electrode contact interface; thus increasing contact area resulting in a decrease of resistance with cycling. Stuck set failure can be avoided by fabrication process, interface quality and write algorithm optimization [34], [38], [90], [91].

b) Stuck reset: occurs when the PCM cell is stuck at a high resistance amorphous state i.e. reset state. The applied current fails to program the cell to the crystalline phase; due to void formation in the GST material separating it from the heater and making its resistance very high. According to measurements by [92] the “stuck reset” error is the dominant type of errors that is significantly impacted by cycling “increase linearly with cycling”. this type of failure can be

mended by applying high current pulses that can melt the material and remove the voids [38], [90].

c) Early fails: result from pre-existing nucleation sites arranged in a configuration where a percolation path is created with minimum growth, hence they demonstrate unreliable behaviour. Experimental data from [90] suggest that early fails in reset cells are not permanent defects related to the individual cell itself, rather they are related to the amorphous material structure of this specific reset state. This failure mode can be suppressed by optimizing the fabrication process or the programming algorithm.

2.5.5.2 Retention related associated reliability issues

a) Read disturb: occurs when a reading process overheats the material due to bad isolation [92], leading to programming of the cell. However, read disturb depend on the applied reading current. Repetitive reading with current below 1 μA allows for a 10 years continuous reading preservation of the high-resistance state [79]. Therefore, reading disturb is not considered a major reliability issue for PCM.

b) Thermal cross talk: also referred to as “Program disturb” occurs when the heat of a programming process of a cell crosses to neighbouring cells causing them to change state. Thermal crosstalk takes place in poorly isolated structures, however reported data indicate no detectable phase degradation up to 10^{10} programming cycles, confirming the program disturb immunity for at least the 180-nm technological node [79].

c) Drift: is a gradual increase in amorphous material resistance in RESET state and threshold voltage with time due to structural relaxation and stress release in the amorphous material.

2.6 Summary

In this chapter an overview of performance metrics used in evaluating memory performance is presented. The status of current memory technologies in computer memory hierarchy is discussed in terms of these performance metrics. The issues facing the current memory systems are pointed out, and the most prominent emerging NVM technologies that aim to overcome these issues are introduced. The general operation concepts of the emerging NVM technologies are explained. Then a narrowed down specific description of PCM memory technology is presented. A detailed review of physical properties, operation concepts and reliability issues of PCM is presented.

CHAPTER 3

LITERATURE REVIEW

3.1 Overview

In this chapter, a review of PCM models available in technical literature up to date is presented in section 3.2. Furthermore, the drift phenomenon physical origins, governing lows, and methods presented in literature to mitigate its reliability effects are described in section 3.3. The application of PCM cells in memory crossbars and their performance issues are highlighted in section 3.4. Finally, the methodology adopted to carry this research work is outlined in section 3.5.

3.2 PCM modelling review

In technical literature there has been several proposed PCM cell models for both single bit [5], [93]–[96] and multibit storage [2], [4], [16], [97]–[100]. These PCM cell simulation models are found to be generally composed of interconnected basic modules that simulate the electrical and thermal behaviour of a PCM cell. A PCM cell model is expected to simulate the behaviour of the PCM cell in terms of resistive state, i.e. binary stored value, and generate the standard I-V characteristics. Additionally, a PCM model is expected to accurately calculate the temperature profile across the cell, and the crystalline ratio of the phase change material layer throughout the operation time.

A block diagram of the four basic modules constituting the general PCM cell model structure is depicted in Figure 3.1, and a summary of the physical laws and parameters used in each module is listed in Table 3.1. The specific modules behaviour is as follows:

1) <u>The electrical module:</u> represents the PCM cell equivalent circuit, and is responsible of generating the cell resistive state at all times i.e. the stored bit value.

2) The thermal module: calculates the temperature within the active region using heat transfer equation; based on the cell's resistive state and according to the applied external voltage.
3) The crystalline module: utilizes JMAK equation (2-9) described in Chapter 2 to calculate the crystalline ratio in the phase change material layer; using the temperature calculated in the thermal module.
4) The drift module: calculates the drifted parameters i.e. the resistance and threshold voltage based on the empirical laws and drift coefficients extracted from experimental statistical data. Drift phenomenon will be discussed in detail in section 3.3.

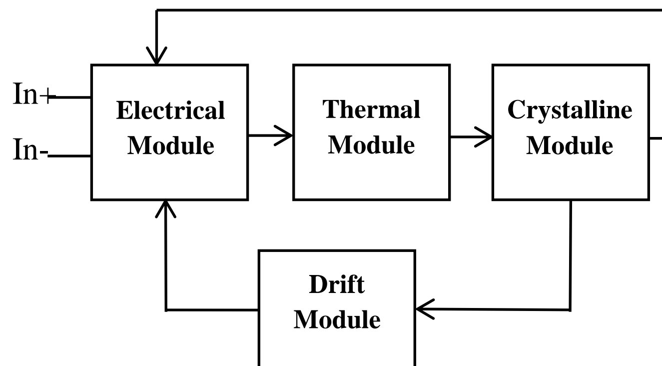

Figure 3.1: PCM cell model block diagram.

In technical literature there are several models for PCM cell [2], [4], [5], [16], [93]–[100].These models used the general interconnected model structure described in Figure 3.1. However, these models suffered from limitations that decreased the accuracy of their results, and rendered them unsuitable for use as testing baseline for PCM behaviour. Moreover, not all of them supported multilevel operation as an actual PCM element would. In the following a review of PCM models available in literature for both SLPCM and MLPCM, along with their drawbacks is presented.

Table 3.1: PCM cell model summary

Model's Block	Physical property	Equations & laws	Parameters	Source
Electrical Module	Resistance Cell's Voltage I-V Curves	Threshold switching	Crystalline resistance Amorphous resistance Dynamic resistance	[2], [4], [5], [63], [95]
Thermal Module	Cell's Temperature	Heat transfer and energy conservation	Cell dimensions Thermal capacity Thermal conductivity Crystallizing point Melting point	[2], [4], [16], [93], [96], [98]
Crystalline Module	Crystalline Ratio	Nucleation theory (JMAK equation)	Avrami constant Activation energy Meyer-Neldel energy pre-exponential factor	[16], [75], [98]
Drift Module	Drifted resistance and threshold voltage	Drift empirical laws	Normalized resistance Drift Coefficients	[4], [49], [50], [100], [101]

3.2.1 SLPCM modelling in literature

The SLPCM cell models found in [5], [93]–[96] addressed the issue of resistance drift when the cell is at amorphous phase, which is an intrinsic phenomenon of the PCM device behaviour. The model presented in [93] provided a spice based SLPCM cell model. The model was successful in generating different resistance levels based on the programming pulse; by calculating temperature and crystalline fraction resulting from that pulse. Yet the models did not demonstrate the I-V characteristics or the continuous change of resistance as the cell is being programmed. Instead, discrete resistance values were modeled with constant resistors. The model suggested by [94] provided both DC and transient simulations for the PCM device. The model succeeded in generating the PCM cell standard I-V characteristics. However, it did

not provide a thermal profile simulation. Similarly to the model in [93], the SLPCM model presented in [5] suggested HSpice circuit based model that used constant resistors to represent the two programmable resistance values of the PCM cell. Therefore, failing to model the continuous change in cell resistance as it occurs physically. Furthermore, the Verilog-A based models provided in [95], [96] did not include the snapback behaviour when programming into low resistive crystalline state. Consequently, the models failed to generate the I-V characteristics of a PCM cell.

3.2.2 MLPCM modelling in literature

The models found in technical literature that entertained the multilevel operation concept [2], [4], [16], [97]–[100] inherited the draw backs of the previously discussed PCM models. The model presented in [16] offered an upgrade to the model in [93], by including multilevel operation concept. The HSpice circuit based model [16] was successful in generating different resistance levels based on the programming pulse. However the model maintained the constant resistance representation. This led to model's failure in simulating the continuous resistance change, and failure to generate the standard I-V characteristics. The model designed in [97] offered a further improvement on the concept of [16]. It simplified the circuit design, by minimizing the number of circuit elements required in the circuit model of the PCM device. Furthermore, the models presented in [98] and [2] accounted for the continuous nature of resistance transition and modeled it properly. The models were successful in generating the I-V characteristics. In contrast to minimizing circuit element practiced in [97]. The model in [99] offered improving the pre-existing model [16]. This is done by including extra circuitry that evaluates the impact of amorphization on crystalline fraction. The enhanced model however still did not generate the I-V characteristics; nor did it account for the continuous nature of resistance transition.

Despite the fact that drift is an intrinsic phenomenon of the PCM device behaviour; all the previously discussed models including the ones that account for multilevel [2], [4], [5], [16], [93]–[100] has not addressed the drift issue. Not simulating the drift behaviour in MLPCM models is considered an enormous draw back; particularly that the drift effect impacts multilevel operation reliability profoundly. However, the work in [4] proposed an HSpice model that includes the continuous resistance change and the drift effect. Yet the presented model failed to accurately model the impact of programing time and the value of drifted parameters (amorphous resistance and threshold voltage). Because it did not calculate the programming specific duration; rather it calculated the overall simulation duration. Furthermore, the model did not retune the drifted parameters in the event of crystallization. Moreover, none of the reviewed PCM models have included the recovery transient behaviour when modelling the amorphous high resistive state immediately after programming. A summary of simulated characteristics in currently available MPLCM models is listed in Table 3.2.

Table 3.2: MLPCM models summary

Model	I-V characteristics	Multilevel operation	Drift phenomenon
[102]	✓	✓	✓
[100]	✓	✓	✓
[5]	✓	×	×
[2]	✓	✓	×
[99]	✓	✓	×
[98]	✓	✓	×
[95]	✓	✓	×

3.3 Drift phenomenon in amorphous phase

3.3.1 Drift origins

The drift phenomenon is one of the main reliability issues facing PCM technology and MLPCM in particular. The drift phenomenon affects the electrical properties of chalcogenide materials i.e. resistance and threshold voltage due to the interrelation between atomic structure and electrical properties [101], [103]. Drift is described as a gradual increase in amorphous material resistance and threshold voltage with time, as depicted in Figure 3.2. Drift behaviour has been attributed to structural relaxation and stress release in the amorphous material [13]. The structural relaxation process that leads to drift phenomenon is defined as "A thermally activated local atomistic scale rearrangement of the amorphous structure, minimizing the internal energy by annealing defects (e.g., dangling bonds, distorted bonds, and vacancies) in which the density of localized state can change significantly, thus resulting in an increase of resistance" [101], [103]–[105].

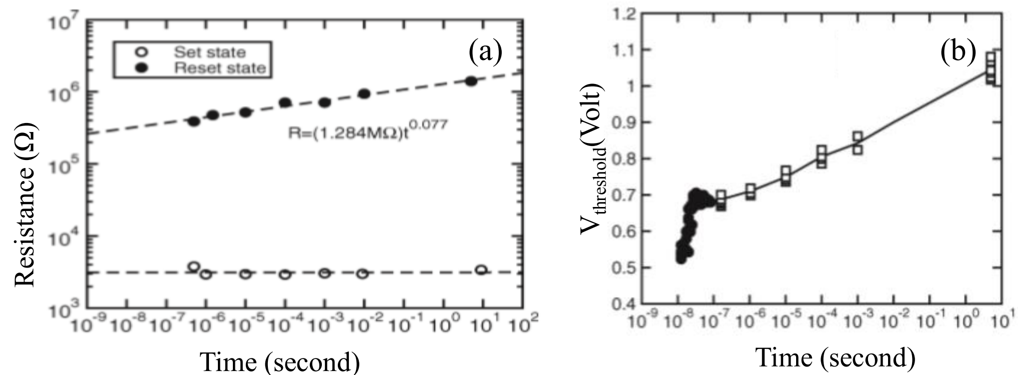

Figure 3.2: Drift in amorphous phase (a) resistance, and (b) threshold voltage ($V_{threshold}$) [49]

The drift is physically attributed to a short-range ordering process of distorted metastable chalcogenide amorphous structure, where a substantial disorder is still kept on the long range. This reordering is caused by rearrangement at atomistic-level i.e. defect annihilation of the disordered structure, and change in density of localized states accompanied by an energy release when phonons overcome energy barriers

[101], [105], [106]; causing the material to evolve into a thermodynamically stable state with less free energy.

The drifted parameters i.e. the resistance and threshold voltage, can be calculated based on the empirical laws (3-1) and (3-2) provided in literature [101]. Where R(t) is the resistance at time t, $R(t_0)$ is the initial resistance at time t_0, v_r and v_t are the resistance and threshold voltage drift coefficients respectively, and ΔV_T is a constant.

$$R(t) = R(t_0)\left(\frac{t}{t_0}\right)^{v_r} \tag{3-1}$$

$$V_T = V_{t_0} + \Delta V_T\left(\frac{t}{t_0}\right)^{v_t} \tag{3-2}$$

Drift coefficients v_r and v_t are found to be proportional to temperature, material thickness and initial amorphous resistance. Indicating that there will be different drift rates at each resistance level of the same PCM cell [101], [104]. Moreover, the values of drift coefficients v_r and v_t are extracted from statistical experiments. However, drift coefficient for the same cell at the same resistance can display different values; and completely different behaviours. This random behaviour is not related to geometry and material parameters; rather it is a result of intrinsic defects at the specific amorphous structure. Different structures in the same cell may in fact display different atomic defects and bonds as a result of random quenching of amorphous material leading to different structural relaxation process [101], [105].

Drifting of amorphous state parameters does not pose reliability threat in a single bit PCM cell. This is due to the fact that the crystalline state maintains its low resistance while the amorphous state drifts to higher values insuring that no overlap occurs. However, experimental results and simulations suggest that time-dependent resistance drift effects are undesirable for multilevel operation from design perspective; as the presence of drift imposes level boundary overlapping. Additionally, the resistance levels of intermediate and fully amorphous states shift

with time as depicted in Figure 3.3 . Therefore, drift of programmed resistive state jeopardizes the integrity of the stored and read bit values [12], [13].

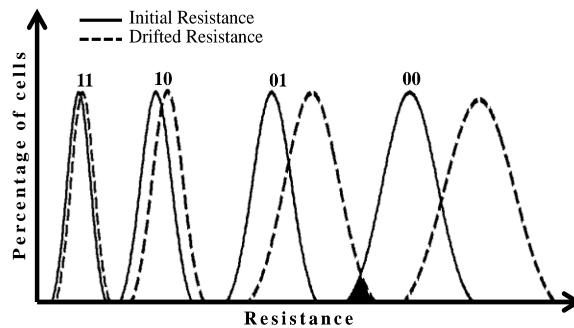

Figure 3.3: Initial programmed and drifted resistance distribution at different PCM resistance levels.

3.3.2 Drift mitigation in literature

Due to the serious reliability issue caused by drift; extensive research work was aimed to mitigate and minimize its effect. One of the conventional solutions was to increase the resistance margin between adjacent states. But it comes at the cost of limited resistance range and thus lower number of states (lower density). Even with an increased margin with time passage drift will lead to resistance levels overlapping. Another approach is Program and Verify algorithms [15]; in which the cell is programmed by applying consecutive programming and reading pulses until the resistance reaches the required value. This approach does not eliminate the drift effect, but it enhances the reliability of the resistance state immediately after programming. Moreover, the increased precision comes at a trade-off with programming delay, power consumption and wearing the PCM cell.

The reference cells scheme [107] was used as well, where specific cells are programmed at intermediate levels between the identified programming levels and are used as direct references during the read process. These reference cells are programmed simultaneously with data cells and hence drift accordingly. The issue with this approach is the programming overhead required, along with the fact that each resistance level drifts in a distinctive manner. Another method was inspired from

Dynamic Random Access Memory (DRAM) scrubbing technique [108], i.e. rewriting the entire physical memory block after a certain time or when an error is detected. The drawbacks of scrubbing is that the programming overhead required is not viable according to [109], the memory block being scrubbed cannot be accessed, and scrubbing requires energy overhead. Error Correction Codes (ECC) are often used along with scrubbing [108]; and they require computing power and delay overheads, design complexity and extra chip area hence, extra cost.

According to [110] all the above mentioned drift mitigation and correction mechanisms do not match the reliability requirements offered by DRAM. The suggested technique in [109] mitigates drift by removing the most error prone state and having a three resistance levels instead of four as the standard two bit cell. Thus eliminating the error caused by the drifting of that state. The main issue with that method is that the cell density decreases and the fact that the approach requires ternary to binary conversion and vice versa which mandates programming overhead.

Another drift mitigation method was the time-aware sensing scheme proposed by [111]. In time-aware sensing; dynamic sensing thresholds are calculated in contrast to the standard fixed sensing threshold method. The work in [111] integrated time-aware sensing with error correction codes; which leads back to the programming complexity and overhead. Time-aware sensing was also suggested in [110], where it was targeted at 3D PCM structures including thermal effects.

3.4 Crossbars

A crossbar is a memory structure that integrates memory devices (PCM cells in this work) in large arrays. Crossbar arrays provide efficient means to facilitate large scale geometry which in turn enables ultra-high densities [17]. Crossbar structures are constructed of a mesh of intersecting rows (Word lines) and columns (Bit lines) of conducting wires; with memory elements placed at each intersection point as shown

in Figure 3.4. Memory elements in the array are accessed by activating the proper row and column in the array; by using address decoders. The memory element at the intersection point of the addressed row and column is thus accessed and can be programmed or read based on the amount of voltage or current supplied through Word/Bit lines.

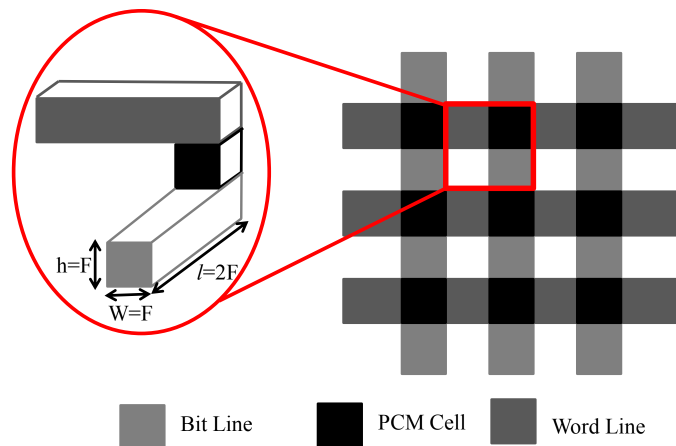

Figure 3.4 Passive PCM based nanocrossbar structure, "inset" lateral view of PCM cell in nanocrossbar.

Crossbars can either be passive or active. In passive crossbars no access device or selection transistors are connected to the memory element or connecting wires. On the other hand, active crossbars utilize selection devices such as diodes. With appropriate voltage configurations, passive PCM based crossbar arrays can be accessed without selection devices. However, sensing margin and power efficiency decreases significantly in large arrays [20]. The presence of selection device limits the flow of current to unselected wires and elements. Therefore, selection devices minimize leakage currents and related power dissipation [17], [20], [21]. Nonetheless, the magnitudes to which leakage currents affect the memory crossbar performance depend on the memory element used.

Until recently, crossbars have been designed with SRAM using CMOS technology. But with increasing demand for denser and faster memory devices, researchers have moved towards non-volatile memory (NVM) devices. NVM based crossbars have been proposed [18], [19]. Such as Memristors, PCM, Magnetic Tunnel

Junction (MTJ), Ferro Electric RAM (FeRAM), and Spin Transfer Torque Magnetic RAM (STTMRAM) among other NVM technologies [112], [113].

3.4.1 Performance issues in crossbars

Nanocrossbar memory structures have multiple performance issues. Including stray capacitances caused by memory peripheral circuitry [114], thermal crosstalk [22], disturb currents [79], and connecting wire resistance [23], [24] that consume energy and can affect reliability. However, the magnitude to which these performance issues affect the performance of the crossbar depends on the used underlying memory element technology.

Leakage currents do not affect PCM cell performance in particular as these currents are not sufficient to program PCM cells; since PCM requires relatively longer pulses with high power in order to be programmed. A PCM cell will maintain the integrity of the data stored in it for over 10 years, if it was continuously subjected to 1μA current. Nonetheless, leakage currents affect PCM based nanocrossbar performance in general, since it imposes energy loss in the grid. Furthermore, according to previous studies [79], PCM cells in crossbar structures are immune to thermal crosstalk. Given that thermal disturb between adjacent cells (100nm apart) never reaches programming temperature levels i.e. 200°C. On the other hand, the power loss across connecting wire resistance at nanoscaled crossbars affects the performance of the PCM cells, particularly the programmed low resistance state.

3.4.2 Connecting wires resistance

Resistive memory crossbars success relies on their high density, which is a result of reducing memory elements and crossbar connecting wires dimensions to nanoscale. However, the physical properties of conductors at nanoscale differ from that of bulk material. And among other physical resistivity; the electrical resistivity of conductors at nanoscale differs from the bulk material properties. This is due to the

increase of resistance when the geometrical dimension of connecting wires becomes comparable to the mean free path of electrons in the conducting materials. The increase of resistance with decreasing dimension is a result of electron scattering effects along surfaces and interfaces [115]. This should be taken into consideration when designing nanocrossbar memory structures, especially with technology nods being reduced down to 45nm. With connecting wires geometrical dimensions becoming comparable to the mean free path of electrons in the conducting materials as listed in Table 3.3.

Table 3.3: Ideal values for the mean free path of conductors [115]

Material	Mean free path
Silver Ag	52 nm
Copper Cu	39 nm
Titanium Ti	29 nm
Platinum Pt	23 nm
Aluminium Al	15 nm

When the lateral dimensions of the wire are comparable to the material electron mean free path, the electrons scatter at the surface of the wire mainly in a diffusive manner according to Fuchs model [115]. It states that “If the body is limited by surfaces, electrons are reflected back into the material” i.e. the electron scatter into the material in the opposite direction of the current.

The reflection of electrons can be either diffusive or specular in nature as depicted in Figure 3.5. In specular reflection depicted in Figure 3.5 (a); electrons retain their momentum parallel to the field, and their contribution to the effective current is unchanged. On the other hand, diffusive reflection seen in Figure 3.5 (b) leads the electrons to loose part or all of their impulse in field direction. And as a result resistance increase and the total current passing through the conductor wire decreases.

The ratio of these reflection modes is governed by the properties of the surface and grain boundaries [115], [116].

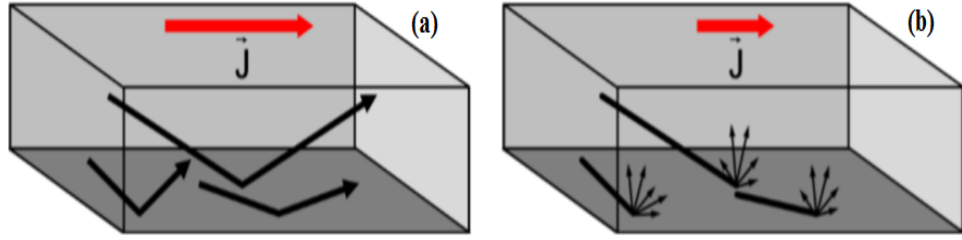

Figure 3.5: (a) Specular reflection of electrons at a conductor surfaces (b) Diffuse reflection of electrons at a conductor surface [115]

3.4.2.1 Connecting wires resistance calculation

The increase of electrical resistivity (ρ) due to surface scattering is described by (3-3), while (3-4) governs the increase of resistivity due to grain boundary scattering, and the overall resistivity increase is evaluated by (3-5) [115]. Where ρ_0 the bulk resistivity, λ is the electron mean free path, p is specularity factor i.e. the probability of an electron being scattered elastically at the side surface of the wire. C is a constant, h and w are the wire thickness and height respectively as shown in Figure 3.4. d is the average grain size, and *R* is the grain boundary reflection parameter.

$$\rho = \rho_0[1 + 2C(1-p)\left(\frac{1}{h}+\frac{1}{w}\right)\lambda] \tag{3-3}$$

$$\rho = \rho_0/3.\left(\frac{1}{3}-\frac{\alpha}{2}+\alpha^2-\alpha^3\ln(1+\frac{1}{\alpha})\right), \qquad \alpha = \frac{\lambda}{d}.\frac{R}{1-R} \tag{3-4}$$

$$\rho = \rho_0(2C\lambda(1-p)\left(\frac{1}{h}+\frac{1}{w}\right)+\frac{1}{1-\frac{3\alpha}{2}+3\alpha^2-3\alpha^3\ln(1+\frac{1}{\alpha})}) \tag{3-5}$$

3.4.2.2 Connecting wires resistance effects mitigation in literature

The power drop across connecting wires affects the performance of PCM based nanocrossbars. The nanocrossbars connecting wires resistance issue has been addressed in technical literature [23]–[28]. One of the early works addressing connecting wires resistance issue was presented in [23], where a bulk resistor was

used to represent each Word/Bit line equivalent resistance rather than representing each segment of the wire with an individual resistance as it physically is. The work in [23] then presented an equivalent circuit of the nanocrossbar to evaluate its performance, yet the initial bulk resistor assumption jeopardized its accuracy. Moreover, the work presented in [24] used a similar equivalent circuit approach to that used in [23]. Each wire segment was represented with a resistor to create an optimization frame work. Furthermore, [25]–[27] considered the effect of wire resistance in voltage and current decay in nanocrossbars among other factors based on matrix algebra. However, these works were targeted generally at nonlinear ReRAM based nanocrossbars and not the particular case of PCM based nanocrossbars.

3.4.3 Leakage currents

Leakage currents are unwanted currents that arise due to the potential difference between two points in a crossbar array and jeopardize the integrity of the data read . Leakage is one of the main issues facing crossbar memory structures. Leakage occurs when a memory element is targeted for either programming or reading; and currents pass through other untargeted elements as depicted in Figure 3.6. The blue line indicates the current passing through the targeted cell (shaded), while the red line is a possible leakage current path leading to power loss, programming delays, and read errors.

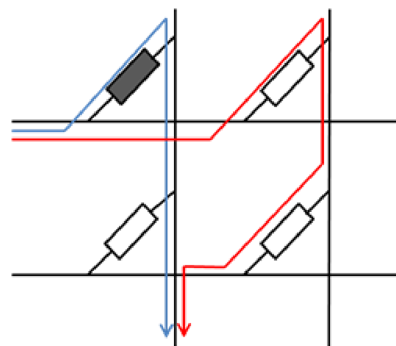

Figure 3.6: Leakage currents in standard crossbar architecture

The reading errors come from the fact the sensed current during the read operation is not the current passing through the targeted element only; but it also includes sneak currents coming from alternate paths. These sneak path currents are difficult to rule out; due to that fact that the exact amount of sneak current is dependent on the resistive state of elements on alternate paths.

3.4.3.1 Leakage currents mitigation in literature

A number of methods have been proposed in attempts to eliminate the sneak path currents in resistive memory based crossbars. Including but not limited to, partial biasing [117], crossbar architecture designs [118], and use of AC sensing instead of DC sensing [119].

3.4.3.1.1 *Leakage currents mitigation by using access device*

The most common practice to eliminate alternate currents is to connect an access device as demonstrated in Figure 3.7 to each element i.e. an active crossbar [20], [120], [121]. The presence of the access device enforces better control on the path of the current flow. The use of access devices minimizes reading errors and power consumption. However, it comes with the disadvantage of limiting the size of the memory to that of the selection device instead of the memory element, hence leading to decreased density in comparison to passive crossbars with no selection devices. As in passive crossbars the memory array can be packed to ultra-high density with memory element area of just $4F^2$ where F is the minimum feature size depicted in Figure 3.4.

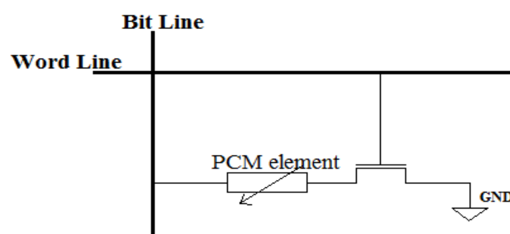

Figure 3.7: PCM element with access transistor

3.4.3.1.2 *Leakage mitigation by AC sensing*

An AC sensing technique is developed and tested with the aim of reducing the consumed and leaked energy in Memristor based nanocrossbar memory [119]. The method relied on using AC source for reading process. Where a low pass filter as depicted in Figure 3.8: Low pass filter circuit is utilized and the level of attenuation of the signal indicates the stored state. The AC sense reading technique is based on the concept of a first order low pass filter. The filter is implemented by coupling the memory cell with a capacitor.

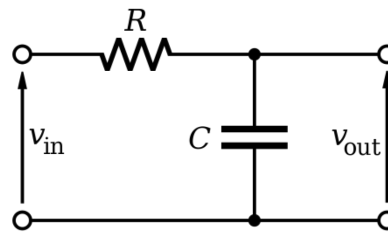

Figure 3.8: Low pass filter circuit

This low pass filter acts as a filtering circuit that will allow signals within a certain cutoff frequency; and attenuate any signal that exceeds the cutoff frequency. The cutoff frequency (f_c) of the low pass RC filter depends on the resistance and the capacitance of the circuit as stated in (3-6). When the capacitance is set to a constant, the cutoff frequency will only depend on the resistance of the circuit. And the two extreme resistive states will have different cutoff frequencies. Hence, the filters ability to differentiate between programmed resistive states i.e. sensing.

$$f_c = \frac{1}{2\pi \mathrm{RC}} \tag{3-6}$$

3.5 Methodology

3.5.1 PCM cell and memory crossbar design flow chart

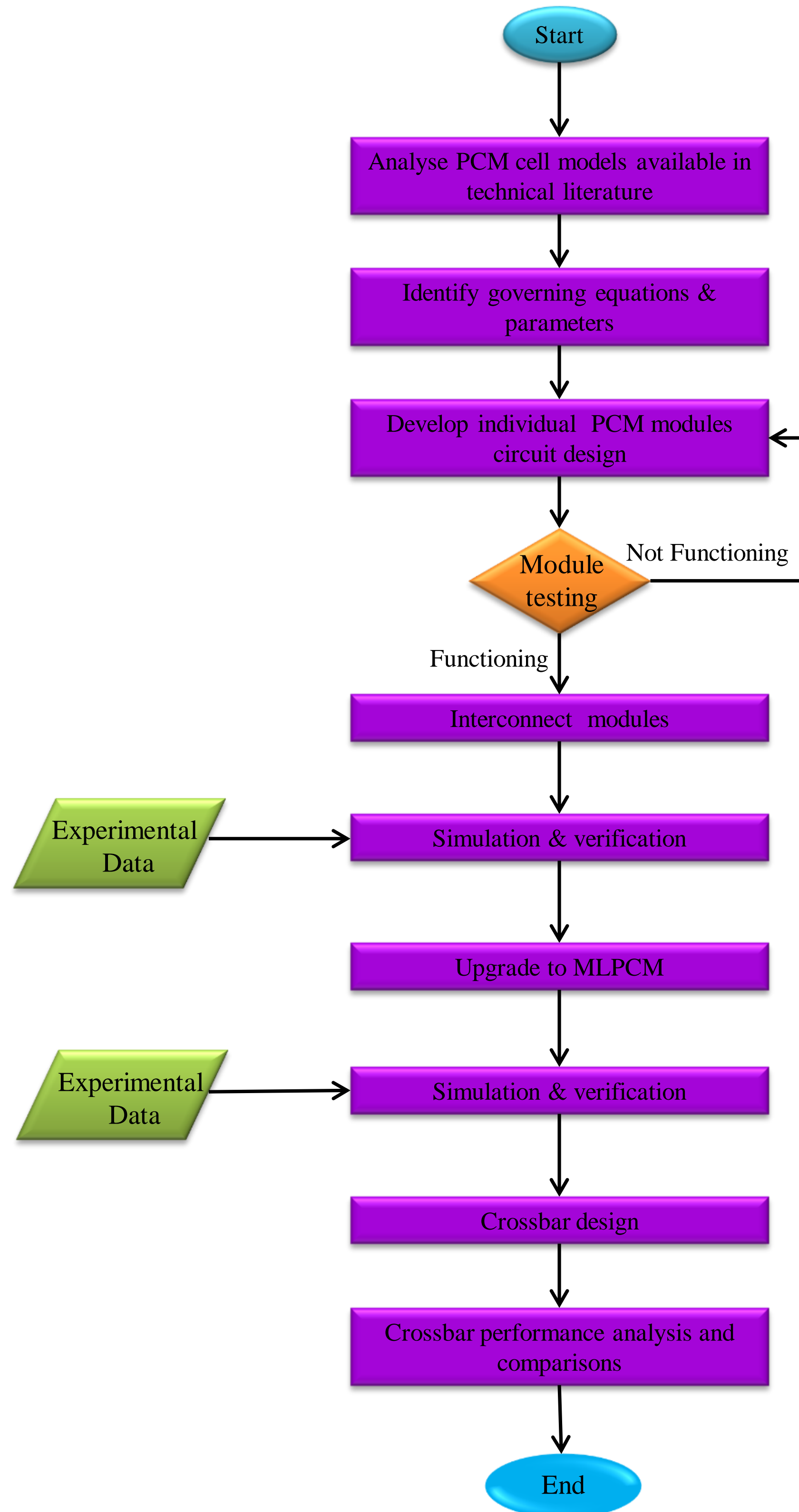

Figure 3.9: PCM cell circuit model design flow chart.

3.5.2 Design process

To design PCM cell circuit model the steps described by the flow chart in Figure 3.9 were applied. Initially, PCM models available in technical literature were collected, analysed and verified to identify physical equations and parameters governing SLPCM cell operation as described in Table 3.1. Once the governing equations of physical properties are verified; modules that calculate each property are designed and tested individually following the interconnected blocks format used in PCM models designs in most of the models in technical literature. Then the modules are connected and the overall model is tested in simulation environment using LTSpice.

The choice of Spice based circuit modelling is made to accommodate the subsequent usage of the designed cell circuit model in crossbar memory structure design and testing. To verify and validate the designed SLPCM cell circuit model, the simulation results are compared to experimental data found in technical literature; the compared metrics include the programmed resistance, I-V characteristics, and drifted parameters.

After the SLPCM model is verified it is upgraded into MLPCM cell circuit model. The upgrade is done by modifying some of the modules in the SLPCM model as will be described in detail in Chapter 4. The MLPCM cell circuit model is similarly verified by comparing simulation results to experimental data from technical literature. After both SLPCM and MLPCM cell circuit models are verified, they are further used as memory elements in memory crossbars to identify operational characteristics of PCM based memory crossbars.

3.5.3 Testing and verification

To test the behaviour and performance of the designed PCM cell models the design is subjected to a sequence of programming and reading pulses based on the crystallization and melting durations of the used GST material, and the physical

parameters of the cell are monitored. Additionally certain physical properties i.e. cell's resistance, I-V curves [4], [63], and drift parameters [4], [50], [100], [101] are compared to experimentally obtained values from actual PCM elements found in technical literature. The test procedures are explained in detail in Chapter 4.

Furthermore, the developed PCM models are used to analyse PCM based memory crossbar structures. The performance metrics used to characterise the crossbars on this work are area, density, energy consumption, and delay. The choice of these metrics is based on the fact that they are the bottleneck of memory systems. As area and density have direct correlation with cost per Bit, and along with delay and energy consumption these metrics can be used to compare the PCM based memory structure to other memory structures. Furthermore, delay and energy consumption are the main performance metrics used to identify PCM possible applications based on application requirements.

3.6 Summary

In the light of the drawbacks found in current PCM modelling in technical literature, an accurate PCM model that precisely evaluates the impact of time, simulates the thermal profile, resistance transitions and successfully generates the standard I-V characteristics and evaluates the drift phenomenon is needed. Such a model will serve as valuable design tool for PCM study and applications design.

Additionally, the drift phenomenon effects on the reliability of MLPCM operation has not been addressed in PCM models. Therefore, drift must be studied and addressed, and an efficient solution to enable the usage of multibit storage in PCM and utilize its high density possibility is called for.

Furthermore, the degradation in performance of PCM based memory nanocrossbars due to leakage and power loss across connecting wires resistance has to be studied and addressed. Given that the current work in technical literature is

general and does not specifically address PCM structures, nor does it consider PCM's physical properties.

CHAPTER 4

PCM ELECTRICAL CIRCUIT MODEL

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- *Elsevier Microelectronic Journal*

  (http://dx.doi.org/10.1016/j.mejo.2016.08.007)

4.1 Overview

In this chapter, SPICE based models of PCM cells for both single bit (SLPCM) and multibit (MLPCM) operation modes are presented. The chapter starts in section 4.2 with an overview of PCM models general module structure, the contribution of the designed circuit model, and detailed modules description. Simulation results are presented and discussed in section 4.3. Finally a drift mitigating reading circuit design is presented, simulated, and discussed in section 4.4.

4.2 PCM cell model design

PCM cell models are generally composed of interconnected basic modules that simulate the electrical and thermal behaviour of a PCM cell as previously mentioned in Chapter 3. The block diagram of the basic modules constituting the proposed PCM cell circuit model is depicted in Figure 4.1. The figure shows how the basic modules are connected along with the main signals that flow between the modules. Furthermore, the signals flowing in and out of each of the interconnected modules along with constants, parameters, signals and their initial values on simulation are listed in Table 4.1, each of which will be explained in their respective module description.

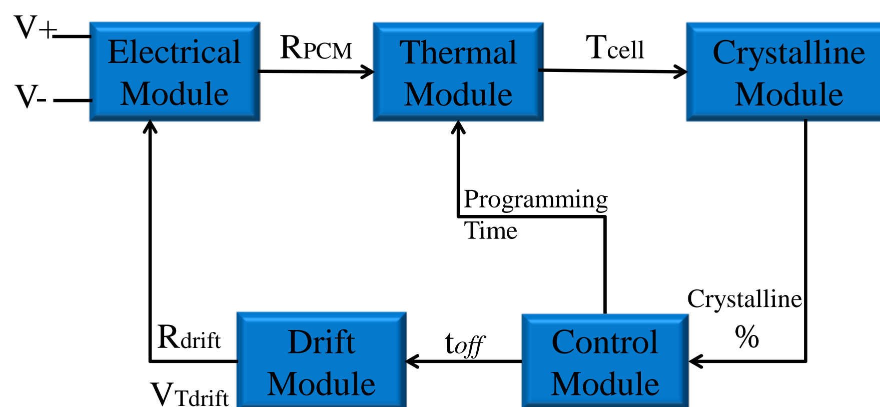


Figure 4.1: PCM cell model basic modules.

Table 4.1: Signals flow summary

Module	Inputs	Initial values	Constants	Outputs
Electrical module	$V_{inexternal}$ V_C PC $V_{threshold}$ t_{off}	- 0% 0 V_{Tmax} -	R_{ON} $R_{crystalline}$ $R_{amorphous}$	R_{PCM} V_{cell}
Thermal module	t_P V_{cell}	- -	r1 r2 k C	T_{cell}
Crystalline module	T_{cell}	-	E_A E_{MN} k_B	V_C
Control module	$V_{inexternal}$ V_C t_P PC IC	- - - - 1	V_{Tmax} V_{Tmin}	$V_{threshold}$ t_{off} t_P PC IC
Drift module SLPCM	t_{off} R_{Prog}	- -	R_0 V_{t0} ΔV_t v_r v_t	R_{drift} V_{Tdrift}
MLPCM	t_{off} R_{Prog}	- -	$R_0(R_{Prog})$ $v\ (R_{prog})$	R_{drift}

The electrical module represents an equivalent circuit for the PCM cell resistance and is responsible of generating the cell resistive state (R_{PCM}) during programming, reading, and when the cell is idle. According to the applied bias and R_{PCM}; the thermal module calculates the temperature within the active region. The thermal module uses the equation of heat transfer to calculate cell's temperature (T_{cell}). Subsequently, the crystalline module calculates the crystalline fraction in the cell as a function of the cell's temperature and applied pulse amplitude and duration. Moreover, the drift module calculates the drifted cell resistance (R_{drift}) and threshold voltage (V_{Tdrift}) based on the empirical laws provided in literature and according to the drift duration (t_{off}). Lastly, the control module orchestrates the flow of signals between the modules, and provides vital signals to the model including the duration of the programming pulse and the drift duration t_{off}.

The model presented in this work insures the reliability and physical accuracy of the representation of changes a PCM cell undergoes during operation. The designed circuit model improves on currently available simulation models in technical literature in four major aspects. These aspects are:

1. The evaluation of the applied pulse duration: The accurate evaluation of pulse duration has implications on both temperature profile and crystalline fraction calculations. In this work the exact duration is calculated in contrast to using the overall simulation duration as the time.
2. The evaluation of drift duration and crystallization implications on drift evaluation: The designed circuit model accurately evaluates the drift duration and additionally reset the drifted parameters in the event of crystallization as it physically occurs.
3. Thermal conductivity: The thermal conductivity “k” is temperature dependent. In the presented circuit model, the value of k corresponding to operating temperature was used.
4. Drift parameters evaluation: Statistical experimental data for drift parameters are used in the MLPCM circuit model. And the variability in drift parameters at different initial resistance level (R_{PCM}) and drift durations was accounted for; rather than using fixed values.

In the following sections, each module and connecting signal in both single and multibit PCM cells i.e. SLPCM and MLPCM circuit model will be described in detail. It should be noted that the model is designed to simulate GST based PCM element in a mushroom cell structure as the one depicted in Figure 1.1. Additionally, all the used constants and parameters in the designed circuit models are for a GST based mushroom cell structure with specific dimensions, and are listed in Appendix 4.1. The specific choice of material, cell structure, and dimensions is in accordance with available experimental data for results verification purpose.

4.2.1 SLPCM cell model description

4.2.1.1 Electrical/ Resistance module

A. Basic resistance modelling

The PCM cell resistance module equivalent circuit depicted in Figure 4.2 simulates the resistance of the PCM cell during programming and reading processes. Moreover, the electrical module is the module responsible for generating the I-V characteristics of the PCM cell; as the current passing through the cell depends on R_{PCM}.

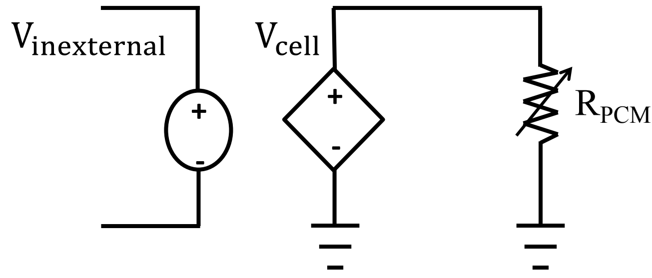


Figure 4.2: PCM cell resistance module equivalent circuit

The resistance across the cell R_{PCM} is modeled using Voltage Controlled resistor (VCR) as seen in Figure 4.2, and is a function of the crystalline fraction (V_C) as shown in (4-1). Given that $R_{crystalline}$ is the resistance of the PCM cell when the active region is completely crystalline i.e. V_C=1, and $R_{amorphous}$ is the resistance of the PCM cell when the active region is completely amorphous i.e. V_C=0. PC represents the programming condition i.e. if the cell is being programmed PC=1 and the resistance of the cell is the dynamic ON resistance (R_{ON}). On the other hand, if the cell is being read then PC=0, and the resistance of the cell depends on the crystalline fraction. V_C and PC are generated by the crystalline module and control module respectively.

$$R_{PCM} = (1 - PC)\left[V_C \times R_{crystalline} + (1 - V_c) \times R_{amorphous}\right] + PC \times R_{ON} \quad (4\text{-}1)$$

The cell equivalent resistance R_{PCM} is connected in series to a Voltage Controlled Voltage Source (VCVS) V_{cell} that represents the voltage input to the cell. V_{cell} is essential for the I-V characteristics simulation; as it represents the voltage across the PCM cell as a function of the applied external bias ($V_{inexternal}$). The cell experiences threshold switching phenomenon, where the voltage across the cell V_{cell} drops regardless of the external bias $V_{inexternal}$.

Therefore, at specific conditions a drop of ($V_{threshold}$-V_X) is introduced to V_{cell}; in order to simulate the snapback behaviour in the amorphous to crystalline transition. Specifically, when the input voltage is higher than the threshold voltage ($V_{threshold}$) and the cell is initially amorphous i.e. IC=1. Where IC is a signal generated by control module that indicates the cells initial state. And V_x is the intersection point of the ON and OFF states in the I-V characteristics seen in Figure 2.7. Otherwise, V_{cell} retains the same value of the external voltage. The value assigned to V_{cell} is calculated using the conditional equation (4-2).

$$\begin{aligned} V_{cell} &= V_{inexternal} - (V_{threshold} - V_x), \quad PC = 1 \& IC = 1 \\ V_{cell} &= V_{inexternal}, \quad \text{otherwise} \end{aligned} \tag{4-2}$$

B. Recovery transient resistance modelling

In order to model the transient recovery behaviour in the resistance module; experimental data from [48] were used along with curve fitting. An exponential equation (4-3) describing the transient resistance as a function of time after programming (t_{off}), and R_{ON} was developed. After the experimentally verified transient period i.e. 20ns, the programmed amorphous resistance starts drifting following the empirical drift equation evaluated in the drift module. Once the transient state conditions are met, R_{PCM} value is calculated using (4-3) accordingly instead of (4-1). It should be noted that the drifting and transient recovery behaviour affects the amorphous high resistance state. Therefore when the cell is programmed into low resistance state, equation (4-1) is solely used.

$$R_{PCM} = R_{ON} \times e^{2\times10^{8}\times t_{off}} \quad , \quad t_{off} < 20\text{ns} \tag{4-3}$$

4.2.1.2 Thermal module

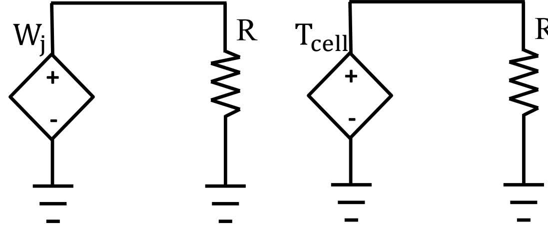


Figure 4.3: Temperature calculation module equivalent circuit

The temperature of the cell (T_{cell}) is calculated using the energy conservation equation (4-4). Given that the generated energy due to joule heating (W_j) is calculated by (4-5). The heat dissipating through the electrodes and the isolating layers (W_d) is calculated by heat transfer equation (4-6), given that I_{cell} is the current passing through the PCM cell, and k is the thermal conductivity of the phase change material. Where r_1 and r_2 are the radii of the active region and the PCM cell respectively, k is the thermal conductivity, and c is the heat capacity. By substituting (4-5) and (4-6) in (4-4) and solving the integration assuming that 30% of generated heat is dissipated we get the temperature in the programming region in the cell (4-7). The equation (4-7) is modeled using a VCVS connected in series with 1Ω resistors - for LTSpice simulation purposes as depicted in Figure 4.3.

$$T_{cell} = \int \frac{W_j - W_d}{C \times V} dt \tag{4-4}$$

$$W_j = I_{cell} \times V_{cell} \tag{4-5}$$

$$W_d = \sum k\nabla T \tag{4-6}$$

$$T_{cell} = \frac{0.7W_j(r_2 - r_1)}{2\pi k r_2 r_1}\left[1 - \exp\left(-\frac{3kr_2}{(r_2 - r_1)r_1^2 C} t_p\right)\right] + 300 \tag{4-7}$$

It should be noted that the thermal conductivity "k" is temperature dependent [122] as seen in Figure 4.4. Therefore, the value of k was chosen to correspond to the operating temperature i.e.400˚C.

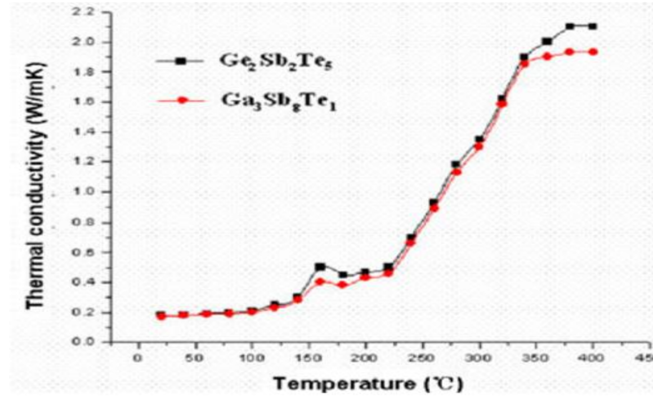


Figure 4.4: Thermal conductivity as a function of temperature [122]

4.2.1.3 Crystalline module

The crystalline module equivalent circuit depicted in Figure 4.5 was modeled based on JMAK equation (4-8) to evaluate the crystalline fraction (V_C). The JMAK equation describes how solids transform from one phase to another as a function of temperature (T_{cell}) and time. Where n is the Avrami coefficient, and t_p is programming time which is generated by the control module. In a similar fashion to the previous modules, VCVS's in series with1Ω resistors were used to model the crystalline module as shown in Figure 4.5.

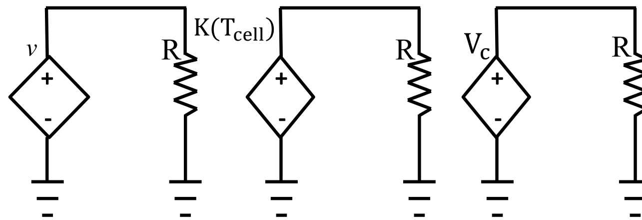


Figure 4.5: Crystalline fraction module equivalent circuit

$$V_c = k(T_{cell}).t_p{}^n \quad (4\text{-}8)$$

The pre-exponential factor in (4-8) "k" is given by the Meyer-Neldel rule (4-9), where E_A is the activation energy of GST. K_B is the Boltzmann constant. The pre-

exponential factor in (4-9) is evaluated according to the Meyer-Neldel rule with (4-10) given that E_{MN} is Meyer-Neldel energy, and v_0 is a constant listed in Appendix 4-1.

$$k(T_{cell}) = v \exp\left(-\frac{E_A}{k_B T_{cell}}\right) \tag{4-9}$$

$$v = v_0 \exp\left(\frac{E_A}{E_{MN}}\right) \tag{4-10}$$

4.2.1.4 Drift module

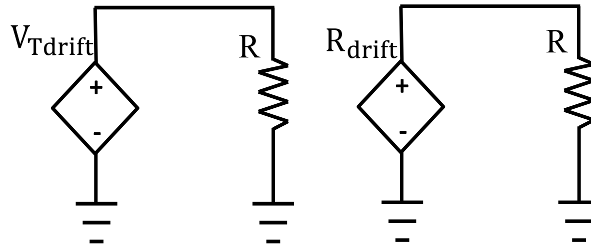


Figure 4.6: Drift module equivalent circuit

The drift module depicted in Figure 4.6 evaluates the drift phenomena of resistance and threshold voltage at amorphous phase. The equivalent circuit for the drift module is constructed using VCVSs in series with 1Ω resistors in a similar manner to the previous modules. The circuit calculates the drifted amorphous resistance R_{drift}, and threshold voltage V_{Tdrift} based on the empirical laws (4-11) and (4-12). Where t_{off} is the time at which the resistance and threshold voltage drift i.e. the time at which the cell is idle after being programmed into amorphous state. R_0 is the amorphous resistance at time t_0. v_r, and v_t are the resistance and threshold voltage drift exponents respectively, and V_{t0} and ΔV_T are constants. Once drift conditions are met R_{PCM} becomes R_{drift} i.e. if the cell was amorphous and idle for duration longer than the transient recovery time (t_{off}>20ns); the cell resistance in (4-1) is replaced by drifted resistance from (4-11). The drift coefficients (v_r , v_t) used in the model are taken from experimental results of GST based PCM cells, and all the used parameters are listed in Appendix 4-1.

$$R_{drift} = R_0 \left(\frac{t_{off}}{t_0}\right)^{v_r} \quad (4\text{-}11)$$

$$V_{Tdrift} = V_{t0} + \Delta V_T (\frac{t_{off}}{t_0})^{v_t} \quad (4\text{-}12)$$

4.2.1.5 Control module

The main task of the control module is to provide signals that connect other modules and insure proper operation of the PCM cell model. The module is responsible of identifying whether a cell is being programmed and to what state, or if it is being read based on the external input. The control module generates two basic control signals and three physical values equivalents, namely the threshold voltage $V_{threshold}$, the programming duration t_p, and the idle time t_{off}. These signals are generated by VCVS's connected in series with 1Ω resistors R in a similar fashion to the previous modules as seen in Figure 4.7, and are described in the following.

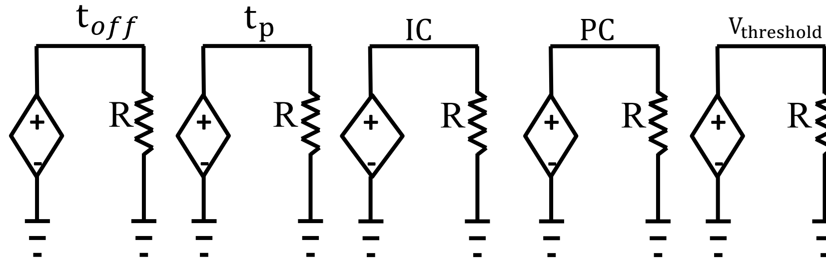


Figure 4.7: Control module equivalent circuit

A. Threshold voltage ($V_{Threshold}$): is the minimum input pulse amplitude at which programming can take place. It is calculated based on equation (4-13), where V_{Tmax} and V_{Tmin} correspond to $V_{threshold}$ when the cell is completely amorphous and completely crystalline respectively.

$$V_{threshold} = V_{Tmax} + (1 - IC) \times V_{Tmin} \quad (4\text{-}13)$$

B. Programming condition (PC): evaluates whether cell is being programmed or not by comparing the external input to the threshold voltage. The PC signal is evaluated using the comparator like equation (4-14). When the external input is higher than the

threshold voltage, PC=1 indicating that the cell is being programmed. Otherwise, PC=0 indicating that the input is not sufficient to program the cell, thus indicating a read process. The programming condition signal is essential in the calculation of R_{PCM} in (4-1) and the voltage across the cell (V_{cell}) (4-2) in the PCM equivalent circuit.

$$\begin{aligned} &\mathrm{PC} = 1\,, \quad V_{\mathrm{threshold}} > V_{\mathrm{inexternal}} \\ &\mathrm{PC} = 0\,, \quad \text{otherwise} \end{aligned} \tag{4-14}$$

<u>C. Initial condition (IC):</u> is the signal indicating the state of the cell prior to programming. If the cell is not at fully crystalline phase (V_C<1) during the first 5ns of programming pulse, then the cell is considered initially amorphous and (IC′=1). Otherwise, the cell is considered initially crystalline and (IC′=0) as indicated in (4-15). IC′ is then integrated in (4-16) to retain the value of the initial condition. The initial condition IC signal uses the resistance module equation (4-2).

$$\begin{aligned} &\mathrm{IC}' = 1\,, \qquad (t_P < 5\mathrm{ns})\&(V_C < 1) \\ &\mathrm{IC}' = 0\,, \qquad \text{otherwise} \end{aligned} \tag{4-15}$$

$$\mathrm{IC} = \int \mathrm{IC}'\, \mathrm{dt} \tag{4-16}$$

<u>D. Programming duration (t_P):</u> represents the exact duration of each programming pulse. By integrating the PC signal with respect to time (4-17). t_P is set to zero at the end of each programming pulse (PC=0) to eliminate accumulation of tp with successive programming pulses. This signal is used by both temperature and crystalline modules in (4-7) and (4-8) respectively.

$$\mathrm{tp} = \int \mathrm{PC}\, dt \tag{4-17}$$

<u>E. Idle/ Drifting time (t_{off}):</u> represents the time at which the resistance and threshold voltage drift i.e. the time at which the cell is idle after being programmed into amorphous state. This timing signal is calculated in a manner similar to the calculation of the programming time, except that the duration integrated is the time at which the cell is idle (PC=0) while in amorphous phase (V_C=0) as indicated in (4-18).

Once these two conditions are met $t_{off'}$ is triggered to 1, and is integrated in (4-19) to evaluate t_{off}. It should be noted that t_{off} is as well reset to zero once a crystallizing pulse is applied; thus resetting the drift process. Evaluated t_{off} value is used in the drift module to calculate drifting resistance and threshold voltage in (4-11) and (4-12) respectively.

$$t_{off}' = 1\,, \qquad (PC = 0)\&(V_C = 0)$$

$$t_{off}' = 0\,, \qquad \text{otherwise} \tag{4-18}$$

$$t_{off} = \int t_{off}'\, dt \tag{4-19}$$

4.2.2 MLPCM cell model upgrade

Multilevel operation allows the cell to store more than a single bit per cell leading to an increased density. The multilevel operation is achieved in this work by manipulating the applied programming pulses duration. This leads to programming the phase change material into intermediate states between the two corner states i.e. the fully crystalline and fully amorphous states. In order to incorporate multilevel functionality to the existing SLPCM model, modifications to control module and drift module are included.

4.2.2.1 Upgraded drift module

It is noted from experimental results that the drift coefficients v_r and v_t are proportional to the initial resistance value with v_r values ranging from 0.01to 0.11 in correspondence to resistance ranges of (10k - 1MΩ) [104], [105], [123]. Accordingly R_0 and ΔV_T demonstrate proportional increase with the programmed resistance level. This behaviour is seen in experimental data depicted in Figure 4.8, and is due to the fact that the drift process itself is stochastic in nature.

To account for this variability in the model; experimentally extracted values of v_r and R_0 [100] are recorded as a function of the initial cell resistance R_{PCM} using curve

fitting to generate (4-20) and (4-21). These values were then substituted in (4-11) and (4-12), making each resistance level generate a distinct drift behaviour tendency similar to the experimentally observed behaviour.

$$v_r = 0.0067 \times R_{prog}^{0.2123} \quad (4\text{-}20)$$

$$R_0 = 0.1621 \times R_{prog}^{1.3021} \quad (4\text{-}21)$$

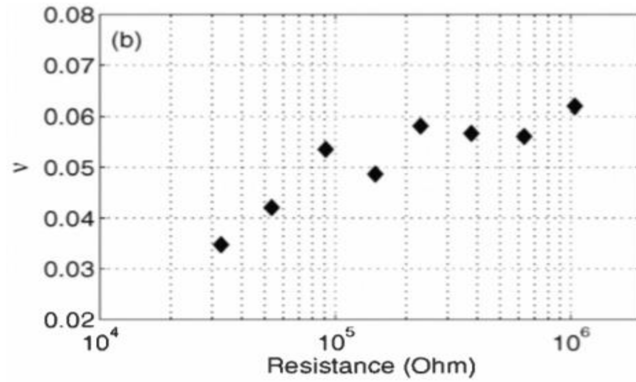


Figure 4.8:Average drift exponent as a function of the programmed resistance level [100]

Furthermore, to model the threshold voltage drift it is assumed that resistance and threshold voltage have the same drift coefficient. This is due to the lack of experimental data of v_t as a function of R_{PCM}. The assumption was made based on the experimental proximity of the two exponents for GST. Where at fully amorphous phase v_r=0.077 and v_t=0.074, with only 0.003 difference.

4.2.2.2 Upgraded control module

The threshold voltage calculating equation in the control module (4-13) is modified to accommodate multilevel operation. Given that $V_{threshold}$ is a function of crystalline fraction and is inversely proportional to it. Therefore $V_{threshold}$=V_{Tmin} when the cell is 100% crystalline, and $V_{threshold}$=V_{Tmax} when the cell is fully amorphous i.e. 0% crystalline. However, $V_{threshold}$ takes values between V_{Tmin} and V_{Tmax} in intermediate resistance levels according to the crystalline ration in active region as defined in (4-22). (4-13) is replaced by (4-22)in the upgraded MLPCM cell model.

$$V_{threshold} = V_{Tmax} + (V_{Tmin} - V_{Tmax})\, V_C \quad (4\text{-}22)$$

4.3 Simulation results

4.3.1 SLPCM simulation results and discussion

The test set shown in Figure 4.9 was used with constants and parameters listed in Appendix 4-1 to simulate and verify the behaviour of the SLPCM cell model. A 1.2V 200ns long crystallizing pulse, followed by a 10ns long 1.6V amorphizing pulse was applied to verify the behaviour of the proposed PCM cell model, given that the cell was initially amorphous. In the following, simulation results showing the behaviour of each module in response to the input pulse sequence are presented.

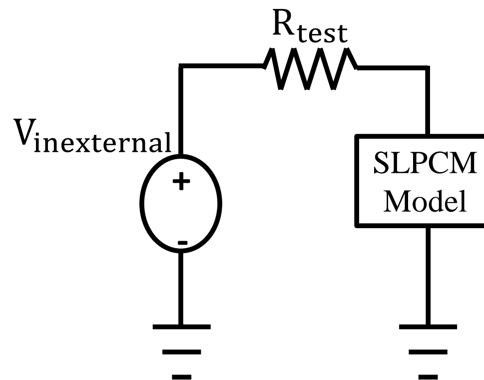


Figure 4.9: Test set for SLPCM cell model simulation

4.3.1.1 Resistance/ Electrical module

A. Applied sequence ($V_{inexternal}$) and Voltage across the cell (V_{cell})

From Figure 4.10 it is noted that when the programming pulse is applied on an initially amorphous cell; the voltage across the cell (V_{cell}) drops as expected during the snapback behaviour. While when a programming pulse is applied on a crystallized cell -as the second pulse in the testing sequence- V_{cell} retains $V_{inexternal}$ Value. Thus, the electrical module is able to simulate the dynamic ON state and the snapback behaviour. During snapback the resistance across the cell drops due to the excess

carriers. This drop in V_{cell} during programming is essential to simulate the I-V characteristics and particularly the snapback behaviour.

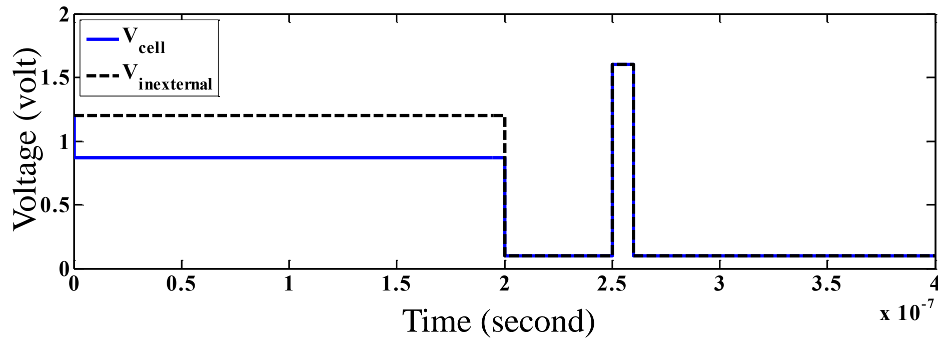


Figure 4.10: Voltage across the cell V_{cell} as a function of external input pulse sequence $V_{inexternal}$

B. Resistive state (R_{PCM})

To measure the resistance across the cell in response to the applied pulse; the current passing through the test resistor R_{test} depicted in Figure 4.9 is measured. Then the voltage across the cell V_{cell} is divided by that current value to calculate R_{PCM}. The simulated and measured R_{PCM} value in response to the input pulse is shown in Figure 4.11. It is noted from Figure 4.11 that the cell during a programming pulse attains the resistive value corresponding to the dynamic ON resistance R_{ON}, which is 1kΩ in this work. On the other hand, when the applied input pulse is a reading pulse R_{PCM} correlates with the previous programming pulse. I.e. the cell attains the low resistive state ($R_{crystalline}$=7kΩ) correlated with crystalline active region, after the first programming crystallizing pulse. Alternatively, the cell is found to be at high resistive state after the application of an amorphizing pulse, with R_{PCM} being equal to $R_{amorphous}$ which is 200kΩ in this work.

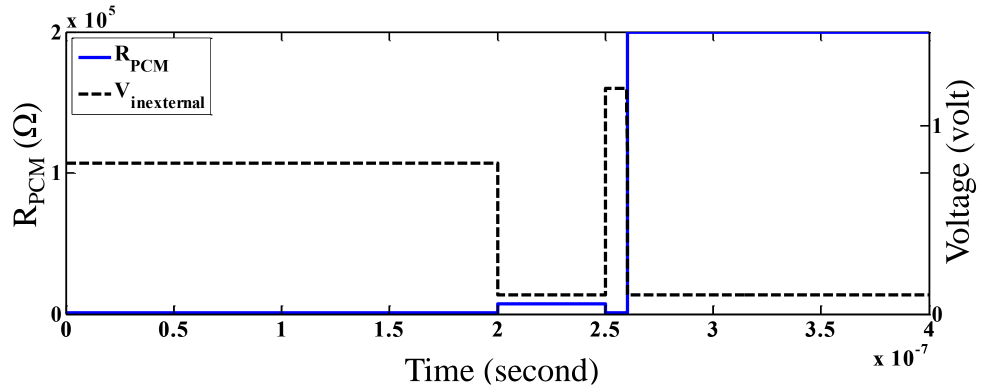


Figure 4.11: R_{PCM} as a function of external input pulse sequence $V_{inexternal}$

C. Recovery Behaviour

The transient resistance state subsequent to programming the cell into reset state was simulated and verified against the experimental data[50] as seen in Figure 4.12. It is noted that the experimental data indicate R_{ON} =3.5KΩ in contrast to the 1kΩ used in previous simulations. This value was calibrated in accordance to experimental data from [50]; in order to carry an accurate comparison. The simulated transient behaviour mimicked the experimental results with high accuracy as seen in Figure 4.12.

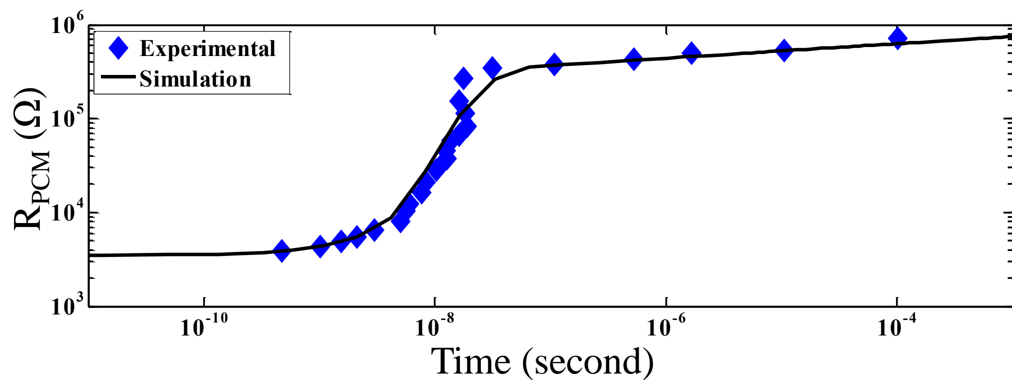


Figure 4.12: Simulated and experimental [50] resistance as a function of time after programming.

D. I-V Characteristics

To generate the I-V plot seen in Figure 4.13; two sequences of pulses were applied in order to test both SET and RESET curves. Initially, the SET curve was simulated

i.e. programming the cell into low resistive crystalline state. To simulate the SET curve; a series of 200ns long pulses with amplitudes increasing by 0.1V step was applied to the cell. Given that the cell is initially and before each pulse at amorphous state. Then the current passing through R_{test} corresponding to each 200ns pulse is recorded. While to simulate the RESET curve; 10ns pulses with escalating amplitudes by a step of 0.1V were applied to the cell. With an initial crystallizing pulse before each 10ns pulse, then in a similar manner the current passing through R_{test} corresponding to each 10ns pulse is recorded.

From the simulation results shown at Figure 4.13 it is noted that at the subthreshold region; simulation results are in close agreement with experimental data [4]. Threshold voltages of both simulated and experimental results were (~1.2V) and currents of simulated and experimental (~200µA). However, at the dynamic on state the simulated curves are not identical to experimental results. The reason behind this slight discrepancy is that in the model the cell maintains a constant resistance R_{ON}, while the experimental data of R_{ON} shows a slight exponential increase.

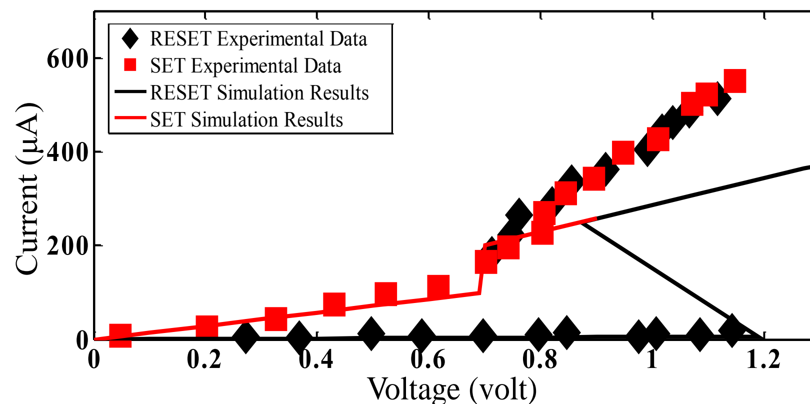


Figure 4.13: Simulated and experimentally obtained [4] PCM cell I-V characteristics

4.3.1.2 Crystalline module

The simulation result of the crystalline module shown in Figure 4.14 is consistent with the crystallization theory. As it is noted that the crystalline ratio V_C increases exponentially during the crystallizing pulse; indicating the growth of crystalline

nuclei. Furthermore, V_C maintains its value post programming and retains it as long as no programming pulse is applied. Thus, the model mimics the physical behaviour of GST material in the PCM element, where it does not spontaneously change state unless programmed. It is also noted from Figure 4.14 that when the cell is fully crystalline V_C =100%, while when the cell is amorphized V_C =0% as expected.

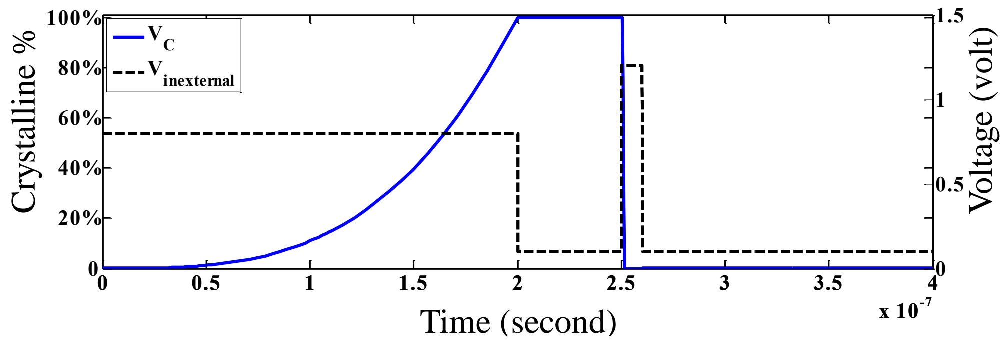


Figure 4.14: V_C as a function of external input pulse sequence $V_{inexternal}$

4.3.1.3 Thermal module

The simulation results of the thermal model with a thermal conductivity of "1.5 W/m/K" are shown in Figure 4.15. It is noted that the applied crystallizing pulse raises the temperature above the crystallizing temperature of GST (473Kelvin), yet well below its melting temperature (873Kelvin). Moreover, the amorphizing pulse raised the temperature across the cell above the melting temperature of GST. This indicates that the used thermal conductivity value along with the amplitudes of programming pulses create the proper thermal condition for PCM cell operation.

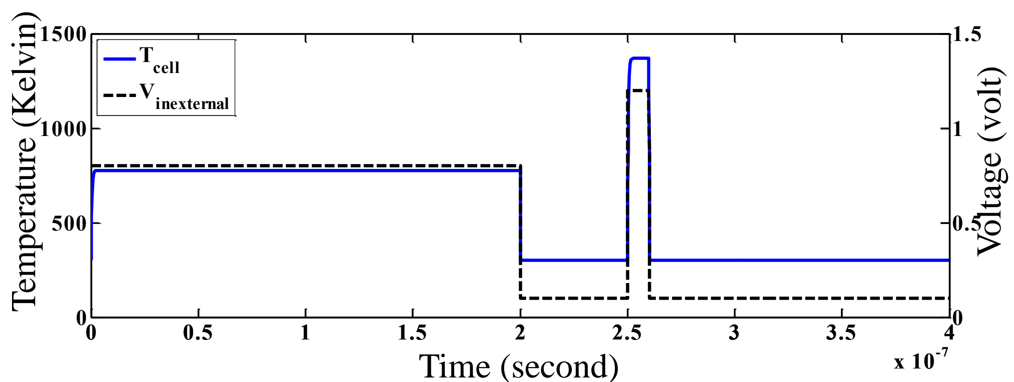


Figure 4.15: T_{cell} as a function of external input pulse sequence $V_{inexternal}$

4.3.1.4 Drift module

The drift module behaviour was tested by measuring R_{drift} after the application of an amorphizing pulse as depicted in Figure 4.16. It is noted from the simulation result that R_{drift} remains zero as long as the drifting conditions are not met; in compliance to the theory behind drift. I.e. drift only occur when the cell is idle and at amorphous phase. Furthermore, simulation results in Figure 4.16 show that R_{drift} calculation starts after the 20ns recovery transient period. And it follows an exponential behaviour in accordance to experimentally obtained drift equation (4-11).

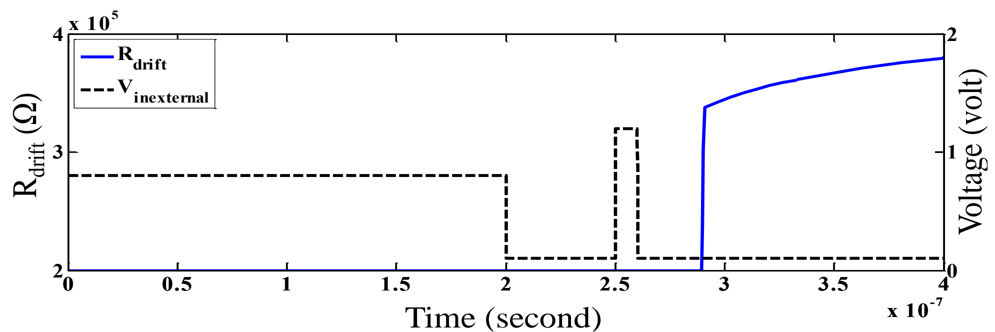


Figure 4.16: R_{drift} as a function of external input pulse sequence $V_{inexternal}$

Moreover, simulated R_{drift} is compared to experimentally obtained data by running simulations for extended t_{off} duration. It was noted from the comparison of simulation results and experimentally obtained data [4] shown in Figure 4.17; that the model depicted an accurate reproduction of drift behaviour at fully amorphous state over time.

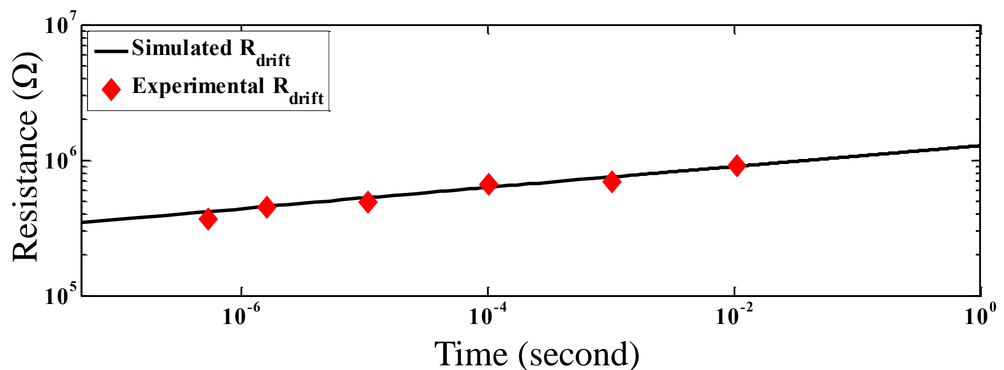


Figure 4.17: Simulation and Experimentally [4] obtained R_{drift} for extended drifting time t_{off}

4.3.1.5 Control module

A. Threshold Voltage ($V_{threshold}$)

The simulation results of the threshold voltage calculation part of the control module are shown in Figure 4.18. From the results it is noted that $V_{threshold}$ depends on the external input and subsequently V_C. I.e. $V_{threshold}$ decreases after a crystallizing pulse and when the crystalline fraction is 100% $V_{threshold}$ takes V_{Tmin} value. Subsequently, $V_{threshold}$ increases after an amorphizing pulse with 0% crystalline ratio and acquires V_{Tmax} Value, as stated in equation (4-13).It should be mentioned that the proper functionality of the $V_{threshold}$ part of control module is essential to obtain proper I-V characteristics.

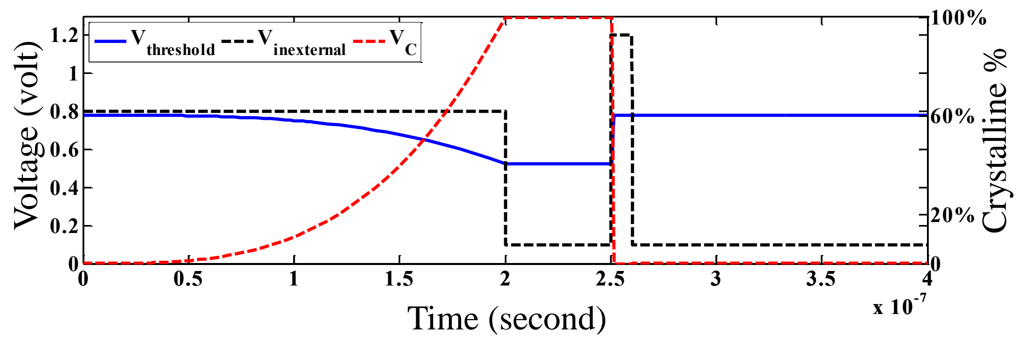


Figure 4.18: $V_{threshold}$ as a function of external input pulse sequence $V_{inexternal}$

B. Programming condition (PC)

Figure 4.19 displays PC signal state during the application of test pulse sequence. The result in Figure 4.19 show that PC=1 as long as the input $V_{inexternal}$ is larger than the threshold voltage which can be seen in Figure 4.18. Otherwise, PC= 0 indicating that the module follows the comparator equation (4-14) describing its behavior. The proper operation of this unit in the control module is essential to the proper behaviour of the electrical module.

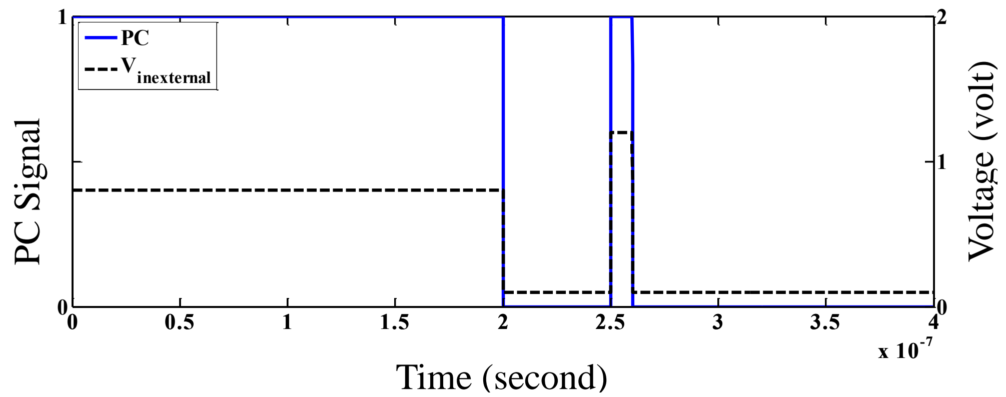


Figure 4.19: PC signal corresponding to external input $V_{inexternal}$

C. Initial Condition (IC)

The initial condition IC identifies the state of the cell prior to programming, by using the crystalline ratio in the first 5ns of programming as stated in (4-15). In a similar manner to PC, the control module depends on the crystalline ratio to identify the state of IC. From the simulation results in Figure 4.20 and looking at the crystalline ratio from Figure 4.14; it is noted that when V_C=0% IC=1 indicating that the cell was amorphous prior to the programming pulse in progress. On the other hand, IC=0 if V_C was 100%, indicating that the cell was initially crystalline prior to the programming pulse in progress. The proper estimation of IC is vital to the proper evaluation of V_{cell} in Figure 4.10 and subsequently the generation of the I-V characteristics depicted in Figure 4.13.

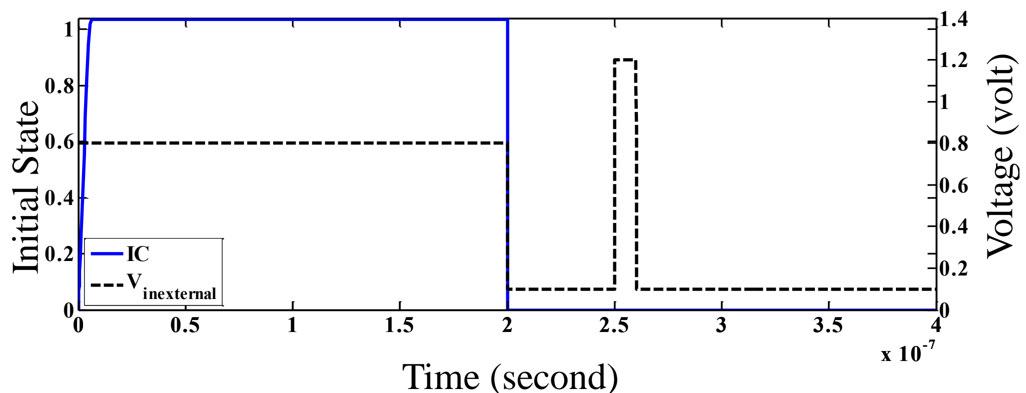


Figure 4.20: IC signal corresponding to external input $V_{inexternal}$

D. Programming Duration (t_P)

One of the main advantages of the proposed SLPCM model is the accurate evaluation of the programming pulse duration t_P. Figure 4.21 shows the evaluated t_P in accordance to the applied pulse. It is noted from the figure that once a programing pulse ends; t_P is set to zero. Hence, the model maintains a precise evaluation of programming pulse duration. An accurate t_P evaluation is important for obtaining accurate calculation of the impact of time in both crystalline ratio (4-8) and the temperature across the cell (4-7).

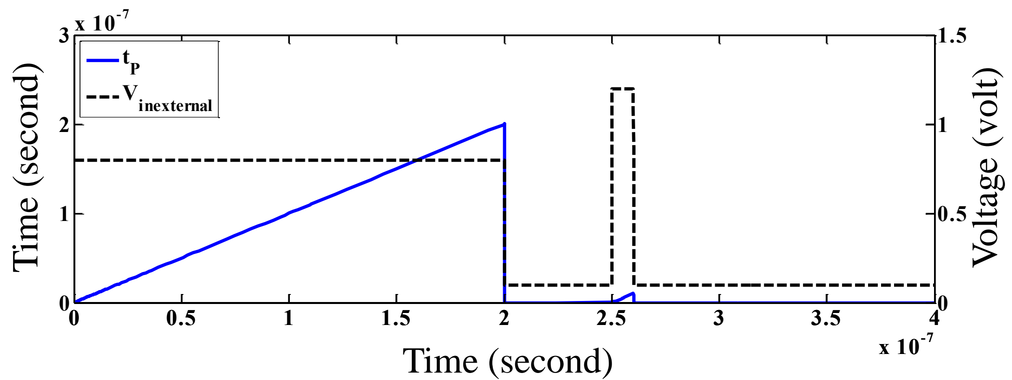


Figure 4.21: Simulation result of t_P evaluation in accordance to applied $V_{inexternal}$

E. Drifting time (t_{off})

The control module evaluates the time during which drift takes place (t_{off}). The evaluation of t_{off} depends on the presence of drift conditions i.e. if the cell is in amorphous phase and idle as indicated in Figure 4.22. From the simulation results in Figure 4.22 it is noted that the main feature of the control module is that it provides an accurate evaluation of t_{off}.

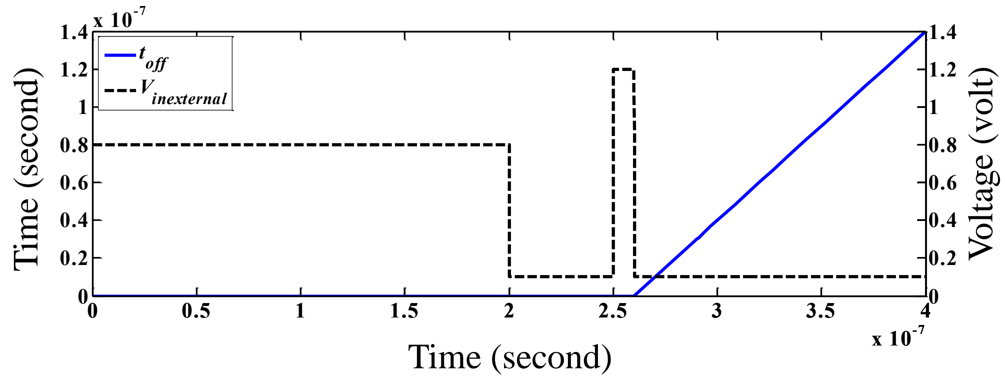


Figure 4.22: Simulation result for evaluation of t_{off} in accordance to applied $V_{inexternal}$

The model resets t_{off} value to zero once a crystallizing pulse is applied. Given that the drift is correlated to amorphous states only and once the material crystallizes it ceases drifting. This is in contrast to what was suggested by previous models [4] which does not account for the drift resetting after a crystallizing pulse as seen in Figure 4.23. Such failure to evaluate actual drift time renders PCM model to be less flexible and difficult to upgrade it to accommodate multilevel operation. Furthermore, it leads to erroneous evaluation of drifted parameters i.e. R_{drift} and V_{Tdrift}.

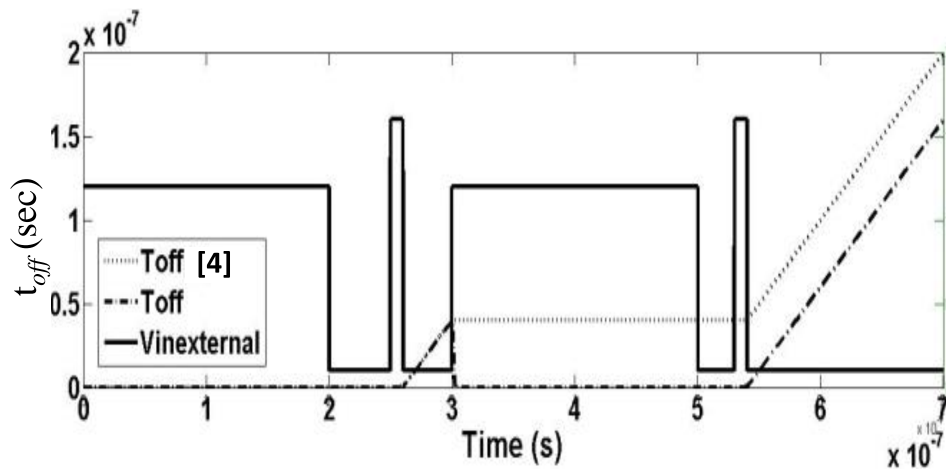


Figure 4.23: Comparison of t_{off} evaluation in suggested model and previous PCM model

4.3.1.6 Standalone cell Programming/Reading delay

The programming delay was based on experimental results in technical literature. I.e. 200ns to program into low resistance state and 10ns to program into high resistance state as stated in Appendix 4-1. On the other hand the reading delay is

dependent on the read circuit design used. In this work, a standard DC sensing circuit with a fixed reference value as the one depicted in Figure 4.24 was used. The cell is first programmed by applying the proper programming pulse amplitude and duration. Programming is performed while the write enable signal (WE) is activated and the read enable (RE) signal is deactivated. The write and read enable signals are inverts at all times.

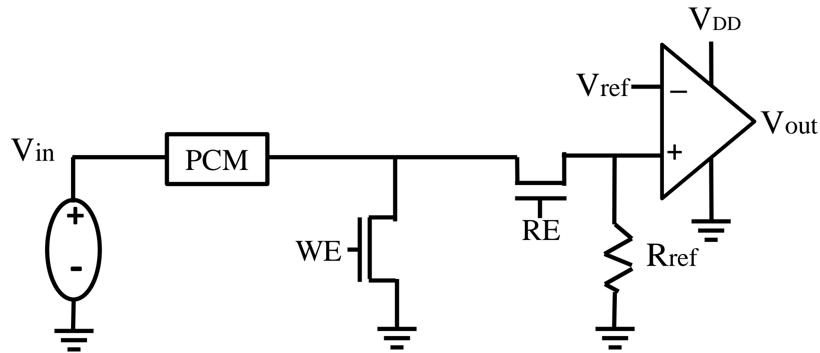


Figure 4.24: Standalone cell delay testing setup

To perform the reading operation; the read enable (RE) signal is activated. And a reading pulse is applied at V_{in}. The resistance of the cell will control the positive input to the opamp comparator, while V_{ref} is set to value between the outputs of a stored “0” and “1”. Accordingly the output (V_{out}) will swing to either V_{DD} or GND indicating a stored “1” or “0” respectively. The simulation result in Figure 4.25 showed the reading delay of a stored “1” is (1.13354μs), while the reading delay of a stored “0” is (698.758ns). It should be noted that the reading delay is sensitive to the change in reading circuit parameters i.e. R_{ref} and V_{ref}.

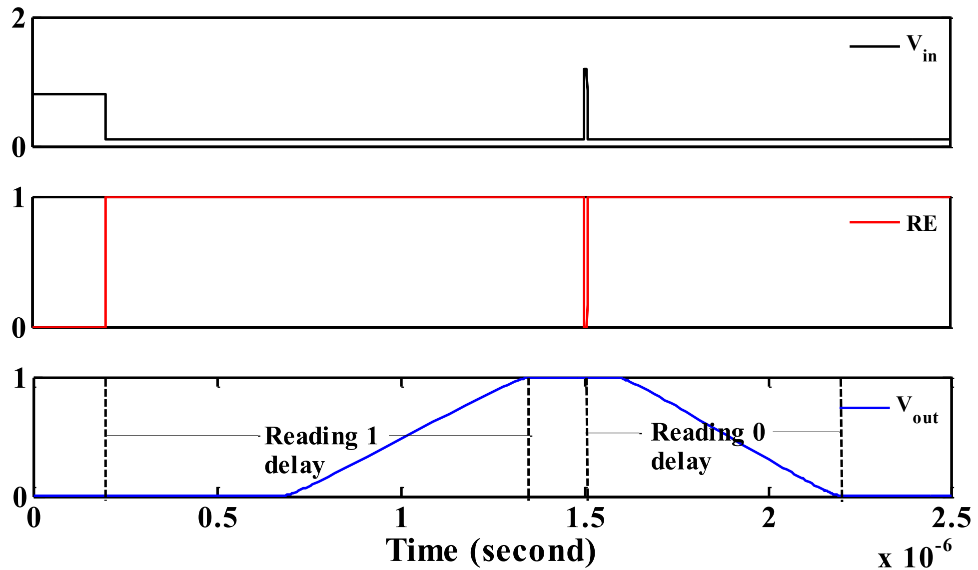


Figure 4.25: Reading delay of a standalone cell simulation result

4.3.2 MLPCM simulation results and discussion

The functionality of the proposed MLPCM model is validated using the test set shown in Figure 4.26 using parameters from Appendix 4-1. The behaviour of individual modules in the model was tested first. And then the I-V characteristics based on simulations were compared to experimental data [63] to validate the proposed MLPCM model. Furthermore, the drifting behaviour is simulated and compared against experimental results from technical literature [101].

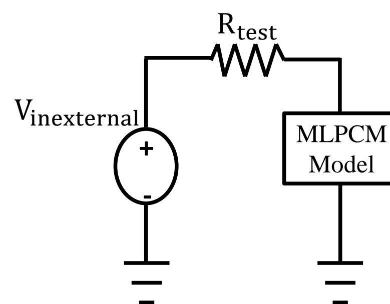


Figure 4.26: Test set for MLPCM cell model simulation

To accomplish multiple resistance levels crystallizing pulses with variable durations followed by amorphizing pulses to reset the cell to high resistive state are used. The corner levels of completely crystalline state and completely amorphous state are achieved by applying 0.8V and 1.2V, for 200ns and 10ns respectively. On the other hand to achieve intermediate levels, crystallizing pulses (0.8V) for 188ns

and 163ns were applied to achieve crystalline fractions of 80% and 50% respectively as described in Table 4.2.

Table 4.2: The drift exponents and corresponding resistances and binary mapping

Resistance level	Binary Equivalent	Resistance value (kΩ)	Vc%	Pulse duration (ns)
R4	00	200	0%	10
R3	01	100	50%	162 (t3)
R2	10	40	80%	188 (t2)
R1	11	1	100%	200 (t1)

Moreover, the programmable resistance levels of the proposed two bit MLPCM model in this work were mapped into equivalent binary values specified in Table 4.2. Furthermore, Table 4.2 shows the crystalline ratio and resistance of each of the programmable four levels tested in this work.

4.3.2.1 Electrical, Thermal and Crystalline modules behaviour in MLPCM model

Three of the basic modules of SLPCM are retained when upgrading the model to MLPCM cell model; namely electrical, thermal, and crystalline modules. However these modules were tested under multilevel operating conditions, i.e. multilevel programming pulses along with upgraded modules. From the simulation results in Figure 4.27(a) it is noted that T_{cell} is directly dependent on the applied pulse. In addition, partially and fully crystallizing pulses t1, t2, and t3 result in temperatures well below GST melting temperature and above crystallizing temperature. This is due to the programming approach used to program into intermediate levels. The cell is partially crystallized by applying pulses with durations shorter than that of a fully crystalizing pulse; in contrast to partially amorphizing the cell.

Furthermore, the crystalline ratio V_C increases exponentially when a crystallizing pulse is applied. As a subsequent to the increase in the temperature across the cell to crystallizing temperature as seen in Figure 4.27(b). It is also noted that V_C is directly

proportional of the duration of the pulse from Figure 4.27(b). The first 200ns crystallizing pulse (t1) resulted in 100% V_C, while the subsequent crystallizing pulses t2 and t3 of 188ns and 162ns resulted in crystalline fractions of 80% and 50% respectively. It is also noted from the results in Figure 4.27(b) that the application of an amorphizing pulse directly results in a drop of V_C to 0%; due to the increase of temperature across the cell above melting temperature. Rendering the behaviour of the model to be in line with JMAK equation used to calculate V_C.

Additionally, the resistive state of the cell immediately after programming is depicted in Figure 4.27(b). It shows that R_{PCM} increases with decreasing crystalline ratio, in accordance to the physical behaviour of an actual PCM element.

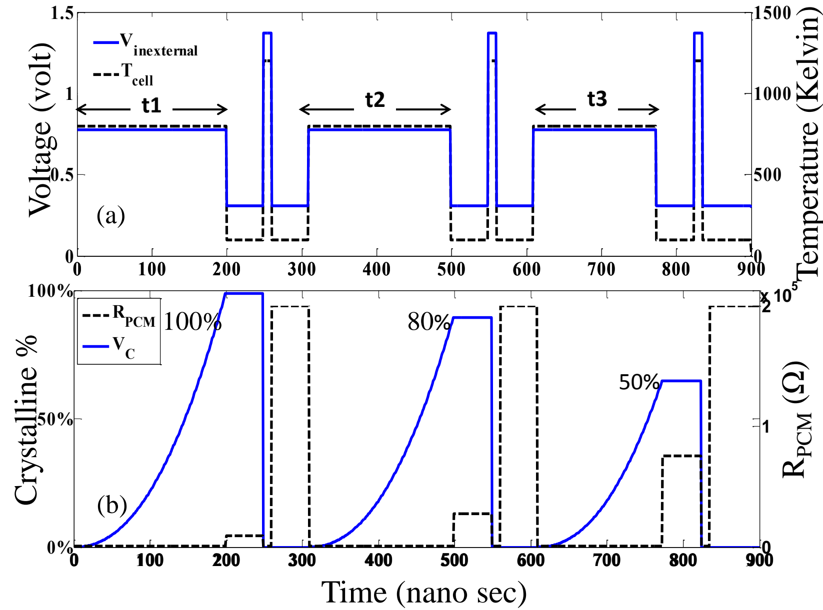


Figure 4.27: (a) Temperature across the cell T_{cell}, and (b) Crystalline fraction V_C and cell resistance R_{PCM} in response to external input $Vin_{external}$

4.3.2.2 Control module ($V_{threshold}$)

The behaviour of $V_{threshold}$ calculating unit in the control module was as well tested in multilevel operation conditions. It was noted from the simulation result in Figure 4.28 that $V_{threshold}$ changes as a function of crystalline ratio V_C and subsequently the resistance of the cell where with increasing resistance $V_{threshold}$ increases. The module follows equation (4-22) as designed. The proper operation of this module is essential

for the MLPCM model to accurately produce the I-V characteristics at various initial resistance levels. Given that the snapback behaviour occurs when the applied input exceeds the specific level's threshold voltage.

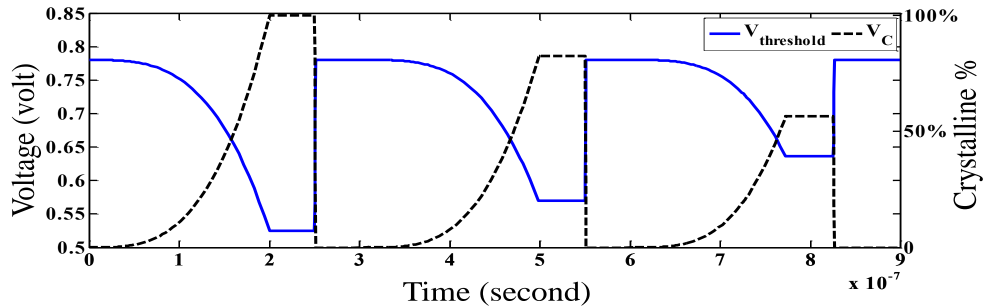


Figure 4.28: Threshold voltage $V_{threshold}$ of corner and intermediate resistance levels in accordance to V_C

4.3.2.3 Drift module

The main feature of the drift module in the designed MLPCM model is that it adapts with all initial resistance levels by using the drift parameters that correspond to each programmed resistive levels. As seen in Figure 4.29; the calculated values for drift coefficient and normalized resistance R_0 used in the evaluation of R_{drift} match the experimental values from which they were extrapolated [100].

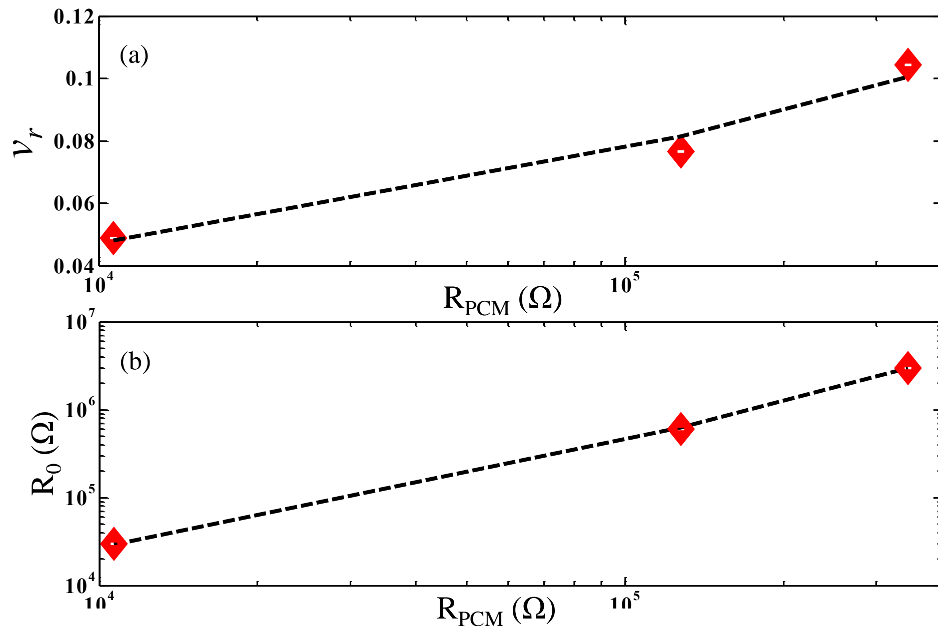


Figure 4.29: (a) Drift exponent v_r, and (b) Normalized resistanceR_0 at t_0=1sec as a function of programmed R_{PCM} "dotted line = simulation, points=experimental data [100]"

Furthermore, the models ability to accurately evaluate R_{drift} as a function of t_{off} is tested and compared against experimental data as shown in Figure 4.30. The simulation result show that the drift of resistance levels with higher initial values exhibit higher drift exponents. The results are found to be in close agreement with experimental data [100]. Additionally, it is noted that with higher initial resistance levels the deviation from the targeted level becomes larger as noted in Figure 4.31. This behaviour leads to reliability issues in multilevel operation which is addressed in section 4.4.

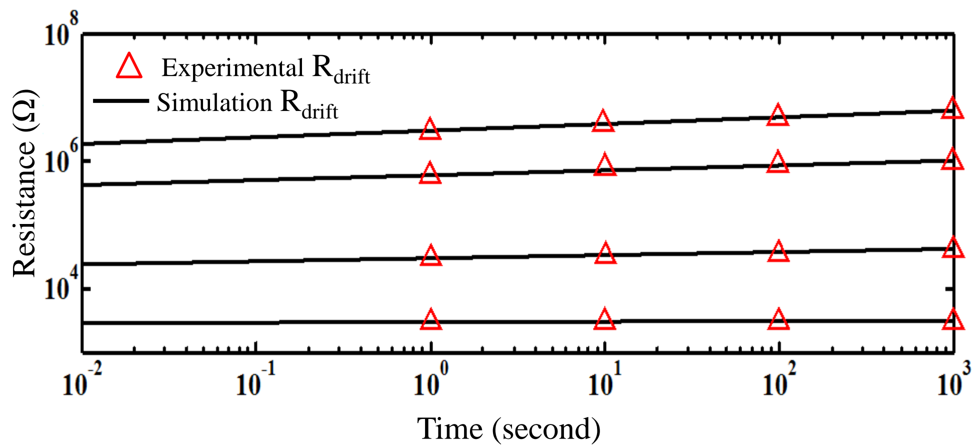


Figure 4.30: Simulation and experimentally extracted [100] R_{drift} at various initial R_{PCM} levels

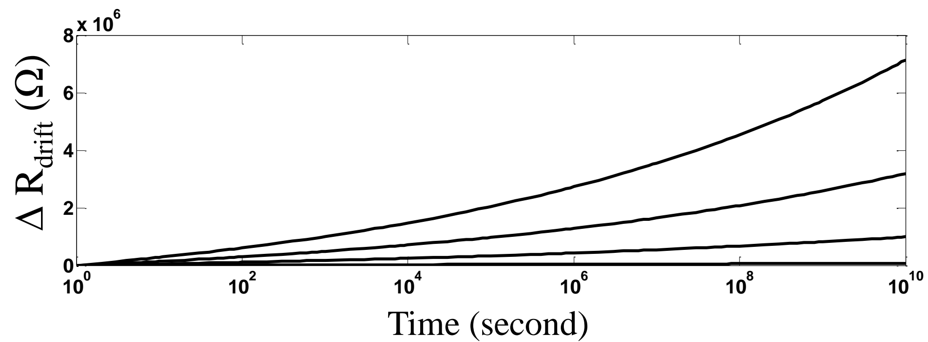


Figure 4.31: Drift deviation from targeted resistance ($\Delta R_{drift}= R_{drift}(t_{off})-R_{drift}(t_0)$)

4.3.2.4 I-V Characteristics

In a similar manner to that used in SLPCM model, MLPCM model I-V characteristics were simulated by applying a series of increasing voltage pulses with step of 0.1 V. The model's I-V plots were generated for different initial crystalline fractions (0%, 7.5%, 75% & 100%). The current through the cell for the

corresponding applied voltage was measured and used to generate the simulated I-V characteristics shown in Figure 4.32. The simulations show that the threshold value depends directly on the crystalline fraction i.e. the threshold voltage is proportional to the initial resistance level. Moreover, the simulated I-V curves from Figure 4.32 demonstrate the characteristic snapback behaviour in intermediate and fully amorphous resistance levels. And when compared to experimental results [63]; it is noted that the simulated snapback behaviour is similar to the experimental data.

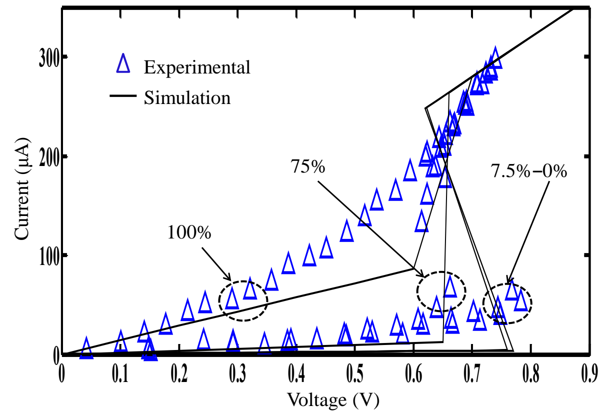


Figure 4.32: Simulated and experimentally extracted [63] I-V characteristics at various R_{PCM} levels

Although simulated curves are not identical to experimental results at all points; threshold voltages of both simulated and experimental results are in the range (0.62-0.8V), and currents of simulated and experimental results fall in the same range (150-250μA). In addition at reading voltage ranges ($V<V_{Threshold}$) the current difference between different resistance levels is recognizable as seen in Figure 4.32. The reason behind this slight discrepancy is that in the model the cell maintains a constant resistance unless it is being programmed, but for the experimental data it shows slight decrease in resistance in sub programming voltage ranges.

4.4 Drift mitigation by time-aware sensing

In this section a dynamic time-aware sensing scheme is presented to overcome reliability issues arising from resistance drift. The presented method eliminates the

effect of drift instead of merely minimizing it, by reconfiguring the reference threshold value as a function of drifting. Hence, allowing the PCM to tolerate the errors dynamically. This scheme was first proposed by [111] but it integrated time-aware sensing with error correction codes; which leads to programming complexity and overhead. It was also suggested in [110], however it was targeted at 3D PCM structures including thermal effects. In this work a circuit is designed to implement and test this method in simulation environment. The generated sensing thresholds are compared with the most recent experimental data [100] to prove that the computed sensing thresholds provide level boundaries that eliminate drift caused reading errors.

4.4.1 Proposed time-aware sensing

The proposed time-aware sensing scheme delivers a method to calculate the threshold between intermediate resistance levels. It adapts sensing levels with time by utilizing the experimental statistical data of drift behaviour at various initial resistance levels. Starting with the assumption that both R_0 and v_r follow Gaussian distributions; the time-aware sensing scheme is modeled, by taking the resistance drift equation (4-11) with t_0=1 and rewriting it in the logarithmic domain to get (4-23).

$$\log R_{drift} = \log R_0 + v_r \log(t_{off}) \quad (4\text{-}23)$$

$$\mu_l = \mu_R + \mu_v . log t_{off} \quad (4\text{-}24)$$

$$\sigma_l^2 = \sigma_R^2 + \sigma_v^2 . log t_{off}{}^2 \quad (4\text{-}25)$$

With both R_0 and v_r following Gaussian distributions; R_{drift} will also follow such distribution as stated by (4-24) and (4-25). μ_l, μ_R, and μ_v are the mean values of the resistance sensing threshold of level l, the initial resistance, and the drift exponent respectively. And σ_l, σ_R, and σ_v are the standard deviations of the resistance sensing threshold of level l, the initial resistance and the drift exponent respectively.

The Q-function of normal distribution calculates the error rate. This is the probability of having the drifted cell resistance of a targeted level in a certain point of time (t_{off}) beyond the boundaries of the programmed resistance level, as shown in Figure 4.33.

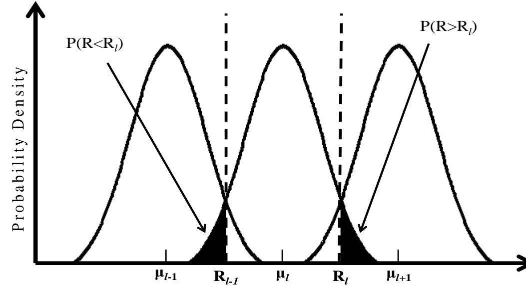


Figure 4.33: Gaussian probability density function of resistance levels overlapping.

Assuming that all resistance levels have equal probabilities [107], then using rules (4-26) and (4-27), where R_{sens} is the sensing threshold; the Q function of resistance level can be evaluated in (4-28) where R_l is level l boundary. he probability of the resistance drifting to the next level ($P(R_{sens} \geq R_l)$) is evaluated in (4-29), while the probability of resistance overlapping with the previous level ($P(R_{sens} < R_{l-1})$) is given by (4-30). Adding (4-29) and (4-30) the total reading error rate (4-31) is calculated in (4-32).

$$Q(-X) = 1 - Q(X) \tag{4-26}$$

$$R_L = \frac{R_{SENS} - \mu_l}{\sigma_l} \tag{4-27}$$

$$Q(R_{sens}) = P(R_{sens} \geq R_l) = \int_{R_l}^{\infty} \frac{1}{\sigma_l\sqrt{2\pi}} e^{\frac{-(R_{sens}-\mu_l)^2}{2\sigma_l^2}} dR_{sens} \tag{4-28}$$

$$P(R_{sens} \geq R_l) = P\left(y \geq \frac{R_{sens} - \mu_l}{\sigma_l}\right) = Q(\frac{R_{sens} - \mu_l}{\sigma_l}) \tag{4-29}$$

$$P(R_{sens} < R_{l-1}) = 1 - Q(\frac{R_{l-1} - \mu_l}{\sigma_l}) \tag{4-30}$$

$$P(R_{l-1} > R_{sens} \geq R_l) = 1 - Q\left(\frac{R_{sens} - \mu_{l+1}}{\sigma_{l+1}}\right) + Q\left(\frac{R_{sens} - \mu_l}{\sigma_l}\right) \tag{4-31}$$

$$error\,rate = \frac{1}{l}\sum 1 - Q\left(\frac{R_{sens} - \mu_{l+1}}{\sigma_{l+1}}\right) + Q\left(\frac{R_{sens} - \mu_l}{\sigma_l}\right) \tag{4-32}$$

To calculate R_{sens} that generates the minimum reading errors, the minima of equation (4-32) is calculated by differentiating it and equating the result to zero (4-33).

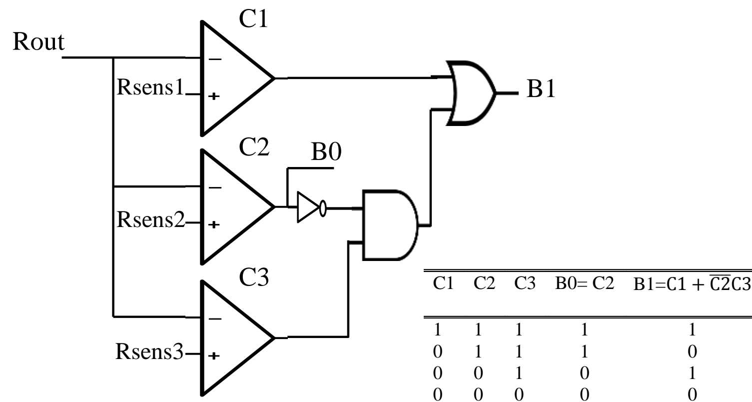
$$\delta\left(1 - Q\left(\frac{R_{sens}-\mu_{l+1}}{\sigma_{l+1}}\right) + Q\left(\frac{R_{sens}-\mu_l}{\sigma_l}\right)\right)/\delta R_{sens} = 0 \tag{4-33}$$

$$R_{sens} = (\mu_{l+1}\sigma_l + \mu_l\sigma_{l+1})/(\sigma_{l+1} + \sigma_l) \tag{4-34}$$

By solving (4-33) we obtain an adaptive time-aware resistance threshold level that generates the minimum reading errors in (4-34). It is then used as a reference for comparison during reading process; giving the value of the quantized reference resistance between any levels *l* and *l*+1 with respect to time according to the Gaussian distribution [111].

4.4.2 Time-aware sensing implementation

To implement time-aware sensing for N bit MLPCM; a minimum of 2N-1 time-aware sensing thresholds R_{sens} are needed as reference when reading the stored data. The current resistive state of MLPCM element is compared against the calculated sensing thresholds at the time of reading. Comparators that compare the cell's resistive state and the time adaptive threshold R_{sens} calculated by (4-34) as depicted in Figure 4.34 are used.



C1	C2	C3	B0= C2	$B1=C1+\overline{C2}C3$
1	1	1	1	1
0	1	1	1	0
0	0	1	0	1
0	0	0	0	0

Figure 4.34: 2-Bit MLPCM sensing circuit design, inset: truth table used to design the combinational circuit.

The MSB of the output B0, can be directly determined from the output of the second comparator C2. While the LSB B1 is determined by the output of comparators C1 and C3, along with the combinational circuit shown in Figure 4.34. The logic to generate the LSB is constructed using the truth table shown in the inset Figure 4.34.

4.4.3 Simulation results

The designed time-aware sensing method was tested by utilizing the MLPCM model presented in section 4.2.2.The proposed adaptive time-aware sense scheme was modeled using mean and standard deviation values for both resistance and drift coefficient that best suit the existing model. The method was tested using values that generate sensing thresholds that fall between the pre-designed resistance levels. The tuned values used are listed in Table 4.3, with (σ_R=0.08) and (σ_v=0.2) [111].

Table 4.3: Mean values of resistance and drift exponent

Resistance / Binary Equivalent Level	μ_{logR}	μ_v
L1(11)	4	0.02
L2 (10)	5	0.06
L3 (01)	5.5	0.08
L4 (00)	6.5	0.12

4.4.3.1 MLPCM without time-aware sensing

Simulations were carried to evaluate time at which resistance level boundaries overlap. This level overlapping can lead to reading errors if constant thresholds were used to evaluate the stored value. It should be noted that a constant sensing threshold can be used in a single bit cell since the drift will not cause levels to overlap. However, at multibit storage the drift of adjacent levels jeopardizes PCM integrity. Therefore, the standard reading method with fixed sensing thresholds limit PCM application as multibit storage element. The times at which this method fails and

level boundaries overlap are evaluated in simulation environment and listed in Figure 4.35.

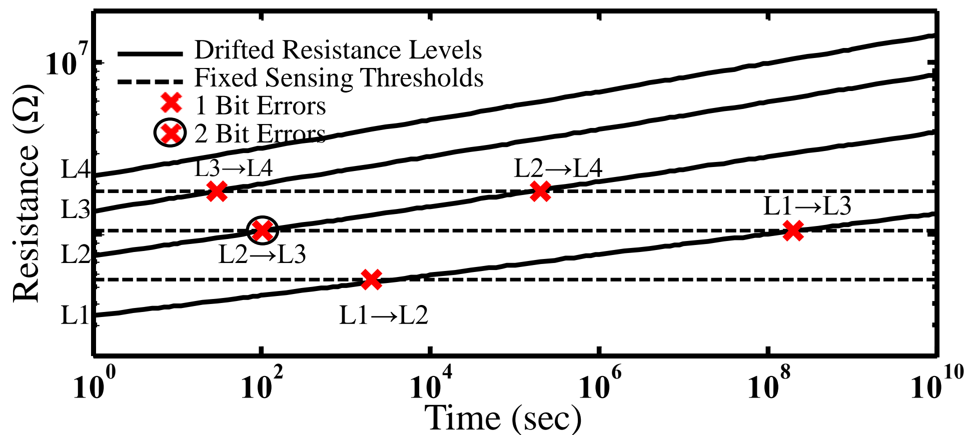


Figure 4.35: 2-Bit MLPCM sensing with fixed sensing threshold

From the results in Figure 4.35 it was noted that the third level (L3) is the quickest to cross level boundaries in less than 100 seconds. While both L1 and L2 take longer time to demonstrate bit errors. It was also noted that the errors caused by drift are proportional to the resistance level; since with higher resistance levels the reference boundary is crossed sooner. This is due to the increased drift coefficient. It is also noted that with time; drift leads to not only single bit errors but also to multibit errors, as the case of L2 (10) drifting to L3 (01).

4.4.3.2 MLPCM with time-aware sensing

In contrast the use of fixed sensing levels; the use of time-aware sensing allows generating sensing thresholds that adapt with resistive levels boundaries drift as seen in Figure 4.36. The adjustable reference levels compensate for the drifted programmed cell resistance and retain the integrity of the read level value. Thus, maintaining the density advantage of MLPCMs with read data remaining accurate and steady at all times. From simulation results in Figure 4.36; it can be noted that the sensing thresholds provided precise level boundaries that can be used for accurate reading of stored data despite programmed resistance drift.

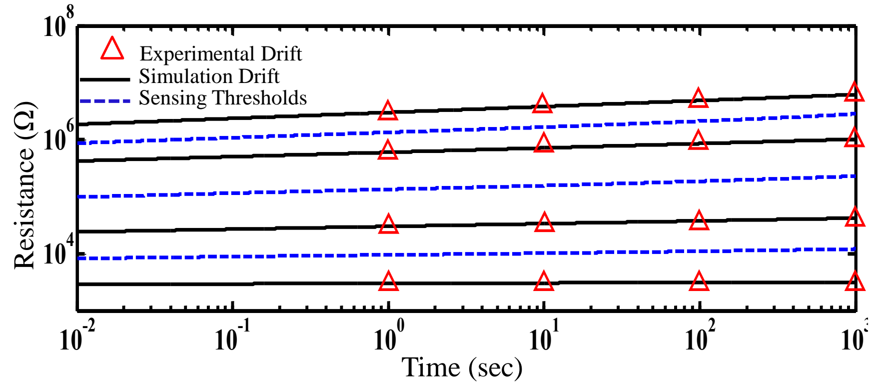


Figure 4.36: Simulation and experimental [100] resistance drift at various initial levels, and adaptive sensing thresholds.

4.5 Summary

In this chapter, SPICE based circuit models of PCM cells for both SLPCM and MLPCM operation modes are presented. These models are to be used as building blocks to design and further test PCM performance in nanocrossbar memory arrays as will be discussed in Chapter 5 and Chapter 6.

The proposed models are designed to accurately simulate the temperature profile, the crystalline fraction and the resistance of the cell at all times as a function of the input pulse; based on physical theories. The parameters used in the models were calibrated with experimental data, and the exact duration of the programming pulse and drifting time are calculated to accurately assess the impact of time.

The simulation results of the proposed PCM model were compared against experimental data and it was observed that the simulation results were in close agreement with experimental results. Furthermore, the designed models were capable of generating the I-V characteristics of a PCM cell, and precisely simulate the drift phenomenon of resistance and threshold voltage at the fully and partially amorphous states.

Additionally the simulated drift resistance levels matched the experimental data for drift durations up to 10^3 seconds; which is the available experimental data

duration in technical literature. Moreover, the simulation results of MLPCM showed that the deviation between the programmed and drifted resistance can reach $6x10^6\Omega$ in less than 10^{10} seconds. This resistance deviation leads to reading failures at drift durations less than 100 seconds, if standard fixed sensing thresholds method is used.

Furthermore, the drift problem that limits MLPCM operation was addressed. An adaptive sensing threshold scheme, that uses statistical data to predict the behaviour of MLPCM, was presented. The simulation results of the sensing thresholds compared to drifting resistance confirmed that the time-aware sensing scheme is reliable. The reading margins did not overlap as the case with standard sensing schemes that use fixed sensing thresholds.

CHAPTER 5

PCM BASED MEMORY CROSSBARS

Parts of the work presented in this chapter have been published in:

- *IEEE student conference on research and development*
  (DOI: 10.1109/SCORED.2015.7449367)
- *IET Journal of Engineering*
  (DOI: 10.1049/joe.2016.0212)
- *The International Nanotech and Nanoscience Conference and Exhibition.*

5.1 Overview

In this chapter passive PCM based nanocrossbars are tested to evaluate connecting nanowires resistance, and leakage effects on PCM performance in nanocrossbar memory architecture. The power drop due to leakage currents and across connecting wires affects the performance of PCM cells in the nanocrossbar memory. As it minimizes the power delivered to program the PCM cell, and increase the energy loss in the memory structure. Therefore, in this chapter PCM performance degradation due to energy loss across connecting wires resistance is evaluated in section 5.2. Structural and programming solutions to performance degradation due to nanowires resistance are presented in section 5.3.

Furthermore, section 5.4 addresses energy dissipation in PCM based nanocrossbars due to leakage currents. The work presents and tests structural and reading circuit solutions to mitigate leakage effects. It should be noted that the PCM cell circuit models presented in Chapter 4 are used as the memory element in the tested nanocrossbar structure.

5.2 Nanocrossbar connecting wires modelling

The Passive nanocrossbar depicted in Figure 5.1 shows the structure used in testing connecting wires resistance (R_W) effects on the performance of PCM cells in nanocrossbar memories. The PCM cell model presented in Chapter 4 was used as the memory element in the structure. Each connecting wire segment along Bit/Word lines is represented by an equivalent resistance (R_W) as depicted in Figure 5.1. This is in order to insure accurate evaluation of the power drop across each segment and its effect on each cell separately, according to its position (m,n) in the nanocrossbar. Where m and n represent the Word line and Bit line at which the cell resides respectively.

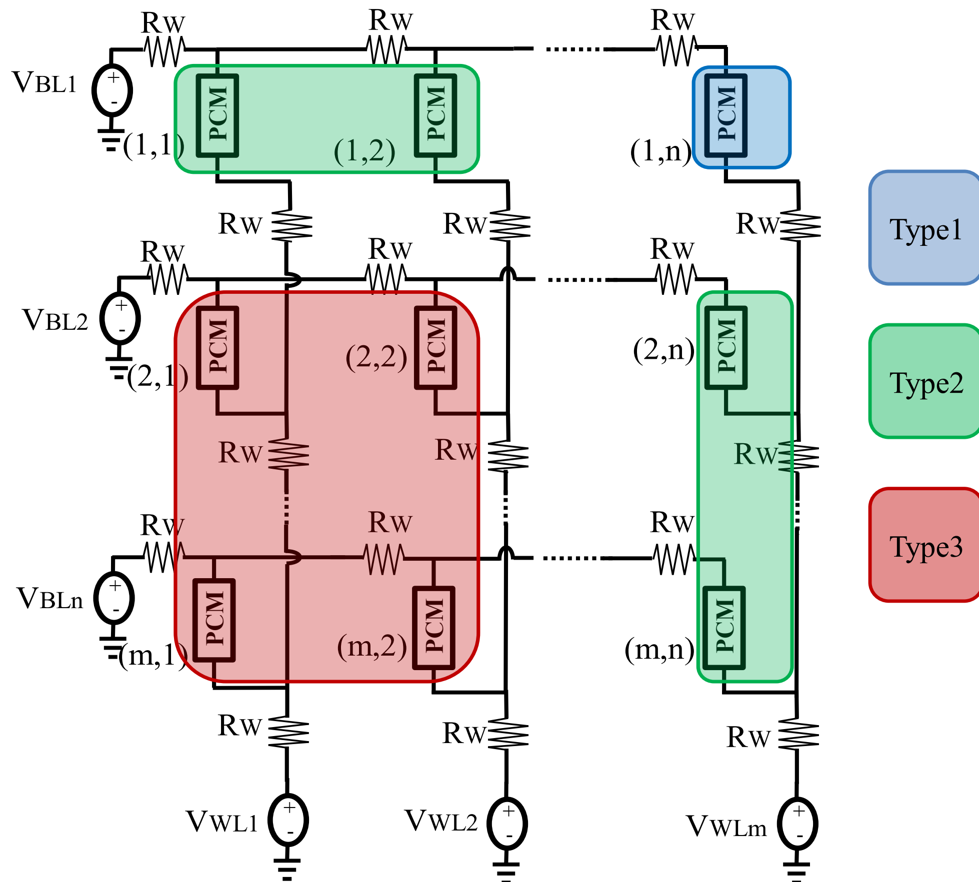


Figure 5.1: PCM based nanocrossbar test structure

To program a targeted cell partial biasing scheme [124] described in

Table 5.1 was adopted. The voltages of the word line (V_{WL}) and bit line (V_{BL}) at which the cell is positioned are probed to V_{prog} and ground respectively. On the other hand, untargeted cells are subjected to half the programming voltage $V_{prog/2}$. Therefore, the partial biasing scheme described in

Table 5.1 insures that the bias across untargeted cells is never sufficient to program them.

Table 5.1: Partial biasing scheme

Selected BL	0V
Selected WL	V_{prog} = 0.8 V, 1.2V
Unselected BL / WL	$V_{prog/2}$= 0.4V, 0.6V

5.2.1 Connecting wires resistance R_W evaluation

In this work Copper (Cu) was the adopted connecting wires material. The resistivity as a function of feature size was measured using two approaches; i.e. (a) Calculating using (3-3) to evaluate surface scattering effect with parameters from Table 5.2. And (b) extracting experimental data from [125]; which include both surface and grain boundary scattering contributions (3-5). The effect of surface scattering is evaluated individually. Since it was considered the sole contributor to resistivity increase at nanoscale in [125]; in contrast to the overall scattering effects considered in [115], [116]. Once the resistivity is evaluated, the connecting wire segment resistance (R_W) is calculated by (5-1). Given that the dimensions of the wire are dependent on the feature size (F) as shown in Figure 3.4.

$$R_W = \rho \frac{L}{A^2} = \rho \frac{2F}{F^2} = \rho \frac{2}{F} \quad (5\text{-}1)$$

Table 5.2: Summary of parameters of equation (3-3) [116], [125]

Parameter	Value in Cu
ρ0	1.7 μΩ.cm
C	1.2
λ	45nm (at room temperature)
p	0.5

5.2.2 Nanocrossbar equivalent circuit

Cells in the crossbar can be separated into three types illustrated in Figure 5.1. Type 1 is the targeted cell, while type 2 cells are the ones sharing Bit/Word Line with the targeted cell. Type 3 includes all non-targeted cells with no common Bit/Word Line with the targeted cell. Assuming that the corner cell (1,n) is the targeted cell; it

was noted that the current passing through cells of type 3 is 10^{-6}% of the current passing through cell type 1 i.e. targeted cell.

Furthermore, from Figure 5.1 structure it is noted that current passing through type 2 cells is 0.25% of the current passing through type 1. The current passing through wire segments connected to type 3 is 0.25% of the current passing through type 1. Moreover, current passing through wire segments connected to type 2 cells that are in the same selected word/bit line is the same as the targeted cell. While current passing through segments connected to type 2 cells; but not on a selected word/bit line, and segments connected to type 3 cells is (0.25)% of the current passing through type 1.

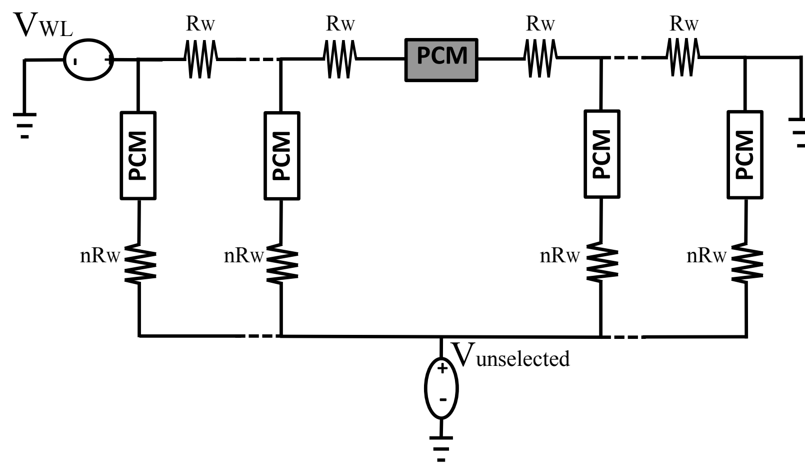


Figure 5.2: Equivalent circuit for passive crossbar structure when targeting corner mostly affected cell

Based on these current values it is found that there are certain branches of the crossbar that can be eliminated to build an equivalent circuit, i.e. branches with current being (10^{-6})% of the programming current. This eliminates all branches containing cells of type3, and simplifies the crossbar structure to the equivalent circuit is shown in Figure 5.2. The crossbar equivalent circuit was then used to evaluate the programmed resistance of the corner cell in square crossbars of different sizes up to 1kBit. The corner cells at low resistance $R_{crystalline}$ are tested with all the untargeted cells at high resistance state $R_{amorphous}$. This assumption is made in order to

create a worst case scenario; in which the maximum energy is lost in connecting wires and the targeted cell is the most affected cell in the nanocrossbar.

5.2.3 Simulation results and discussion

When programming cells to $R_{amorphous}$; the supplied power was sufficient to program the cells into fully amorphous state. This is due to the use of high amplitude steep pulses, which are capable of elevating the cell's temperature to programming boundary even with power dissipating across wires. On the other hand, the power drop across connecting wires affects low resistance state $R_{crystalline}$. This is due to the relatively low programming voltage of $R_{crystalline}$ compared to the programming voltage of $R_{amorphous}$, which makes $R_{crystalline}$ more sensitive to power loss. Therefore the low resistive state $R_{crystalline}$ was tested, in order to evaluate PCM performance in passive nanocrossbars with nanoscaled resistive connecting wires.

The effect of feature size (F) in programmed $R_{crystalline}$ is tested by changing R_W according to tested feature size in a 2x2 passive crossbar as depicted in Figure 5.1. While to test the effect of crossbar size in the final programmed state; the mostly effected cell i.e. the corner cell (1,n) is programmed in square nanocrossbars (n,n). Furthermore, the effect of the position of the cell in the array on its final programmed state is tested by programming cells in a square crossbar. The final programmed $R_{crystalline}$ was measured, and the deviation from targeted level is evaluated. To measure the programmed resistance of the cell; the voltage drop between Word and Bit lines at which the cell resides is measured and divided by the current passing through the cell.

A. *Resistivity and connecting wire resistance (R_W) calculation*

The resistivity of copper nanowires was calculated as a function of feature size (F) using equation (3-3) with parameters from Table 5.2. The calculated resistivity is then compared to the experimental data [16], as depicted in Figure 5.3(a). It was noted

from the comparison in Figure 5.3 (a) that there is a discrepancy at a maximum of 0.5μ.Ω.cm between experimental and calculated results when F=180nm. This difference is expected given that the experimental data includes the increase of resistivity due to both surface boundary scattering and grain boundary scattering. In contrast to the calculated resistivity that accounts only for surface scattering effect. Moreover, surface boundary scattering effect increases proportionally with dimensions. Since the wire length becomes much larger than the grains distance; leading to an increase in surface boundary contribution. However, the variance between calculated and experimentally obtained resistivity on the connecting wire resistance (R_W) is negligible as seen in Figure 5.3 (b).

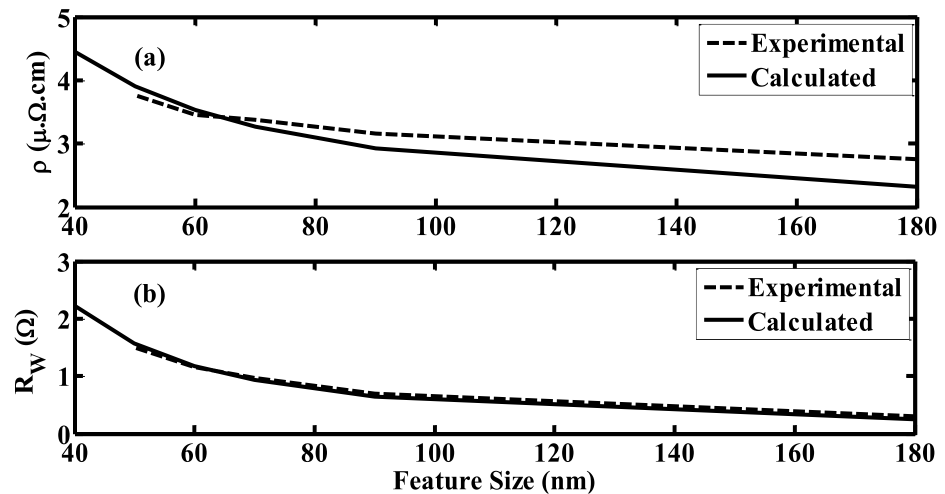


Figure 5.3: Experimentally obtained and calculated connecting wire (a) electrical resistivity, and (b) resistance as a function of feature size

B. Feature size effect on programmed $R_{crystalline}$

As noted from Figure 5.3; with decreasing feature size the resistivity increases resulting in higher wire resistance. Increasing wire resistance results in an increasing power drop across connecting wires; and accordingly an increase in programmed $R_{crystalline}$ as shown in Figure 5.4. To obtain the result depicted in Figure 5.4; the crossbar size was maintained constant i.e. 2x2, while R_W was varied according to

feature size; based on both calculated (3-3) and experimentally extracted [116] electrical resistivity ρ.

The cells were programmed into $R_{crystalline}$ and the deviation of programmed $R_{crystalline}$ from standalone cell i.e. 7kΩ [126] was measured. It was also noted that with increasing feature size the effect of wire resistance on $R_{crystalline}$ is less pronounced. Confirming that with increasing feature size; wire resistance decrease leading to reduced power drop across wires.

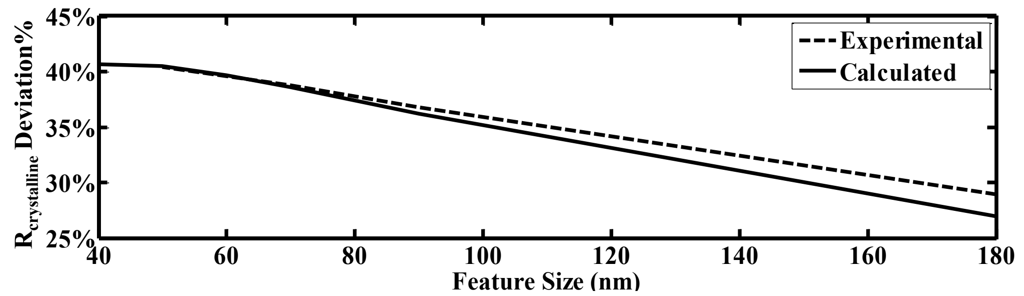


Figure 5.4: Programmed $R_{crystalline}$ deviation percentage from standalone cell as a function of feature size (F) in 2x2 crossbar

C. Crossbar size effect on programmed $R_{crystalline}$

The effect of the crossbar size on programmed $R_{crystalline}$ was tested using R_W extracted from experimental data for F=180nm. The most affected cell in the crossbar i.e. the corner cell (1,n) in Figure 5.1 was programmed to $R_{crystalline}$, while the rest of the cells were at $R_{amorphous}$, i.e. 200kΩ [126]. When programming the corner cell to $R_{crystalline}$, with all untargeted cells being at $R_{amorphous}$; the programmed cell resistance was found higher compared to the standalone cell as seen in Figure 5.5. With $R_{amorphous}/R_{crystalline}$ ratio dropping to almost 2 from the targeted 28 at 1Kbit crossbars; which is more than 90% decrease in $R_{amorphous}/R_{crystalline}$ ratio. Furthermore, the resistance of targeted cells was directly proportional to the size of the crossbar.

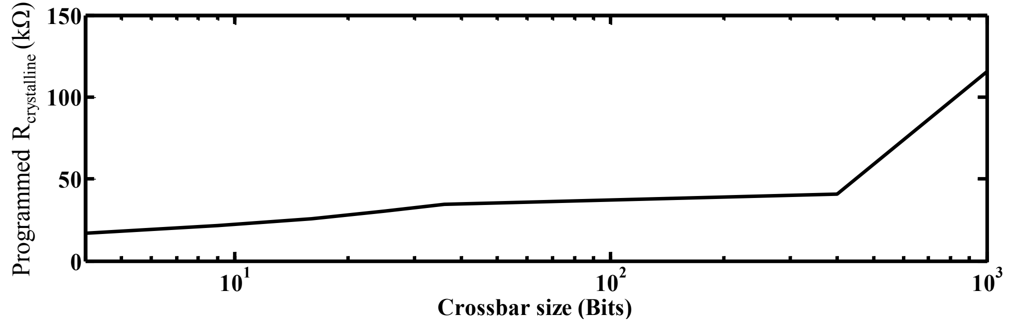


Figure 5.5: Programmed crystalline resistance as a function of crossbar size

The increase in programmed $R_{crystalline}$ noted in Figure5.5 indicates that the power supplied to the cell was not sufficient to crystallize it to a 100% crystalline state. This is derived from the direct link between the crystalline fraction and the resistance level i.e. lower resistances are achieved by higher crystalline fractions. The power loss across connecting wires "leading to the increase in programmed $R_{crystalline}$" increases with increasing number of wire segments i.e. larger crossbar size. Moreover, it was noted that all untargeted cells maintained their initial highly resistive state, indicating that the leakage currents are not sufficient to program unselected memory cells, and that PCM cells are resilient to leakage.

D. Cell position effect on programmed $R_{crystalline}$

To study the effect of cell position, the cells at all positions (n,m) of 1kBit nanocrossbar were programmed into low resistive state i.e. the state showing sensitivity to power loss across R_W. Then the programmed $R_{crystalline}$ was measured. It was noticed that cells that are further away from the voltage sources were the most effected by wire resistance. Additionally, programmed $R_{crystalline}$ was higher compared the targeted level, and to cells on the same row or column that are closer to the voltage source as seen in Figure 5.6, this is in correlation with number of segments across which energy is dissipated.

Furthermore, it was noted that cells in the same diagonal line show the exact deviation from targeted R_{ON} level as seen in Figure 5.6. This is due to the constant

number of wire segments (W_{NO}) in series with the PCM element, between the voltage source and ground during the programming process. Hence, cells experiencing the largest number of wires segments between the cell and voltage source suffer the most as shown in the worst case cell in Figure 5.6. On the contrary, cells positioned closest to the voltage sources and ground suffer the least from energy loss in connecting wires as shown in the best case cell in Figure 5.6.

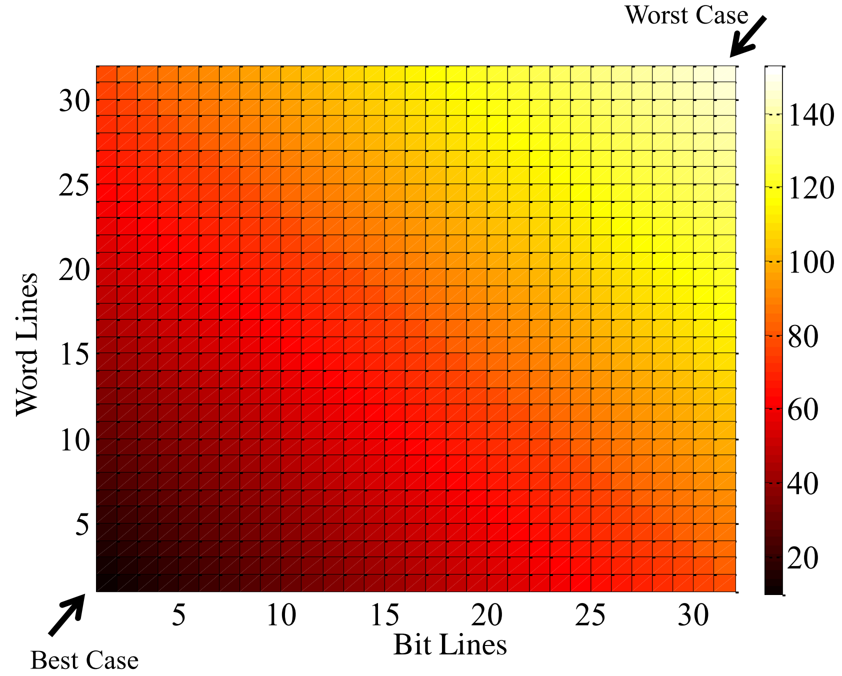


Figure 5.6: Bitmap of programmed resistance in kΩ crossbar at the end of 200ns programming pulse

Based on the cell's position on the crossbar i.e. W_{NO}; the effect of the wire resistance on the programmed cell $R_{crystalline}$ and the expected deviation from the targeted resistance level can be evaluated. By extracting simulation results and fitting $R_{crystalline}$ and the deviation percentage as a function of the cells position i.e. W_{NO} as defined in equations (5-2) and (5-3) respectively.

$$R_{ON} = 2311.9 \times W_{NO} + 5188.9 \quad (5\text{-}2)$$

$$\%\text{Deviation} = 0.2447 \times W_{NO} - 0.4506 \quad (5\text{-}3)$$

E. Energy dissipation in R_W

Simulation results in Figure 5.7 show that the amount of energy dissipation across crossbars during programming to $R_{crystalline}$ is directly proportional to the size of the array. This is due to the inherent increase of supply sources and wire segments in the entire structure. Moreover, it is noted that wire segments closer to voltage sources demonstrate higher power consumption. While the power drop across wire segments in same word line decreases while moving away from the source. This is due to the decrease of propagating power along the connecting wires, as voltage drops at each wire segment and current branches to multiple word lines. Nonetheless, wire segments in direct connection to targeted cell exhibited three orders of magnitude more power dissipation. This is due to the direct path from programming source and ground across the targeted cell, thus maximizing the power drop across the wire segments directly attached to it.

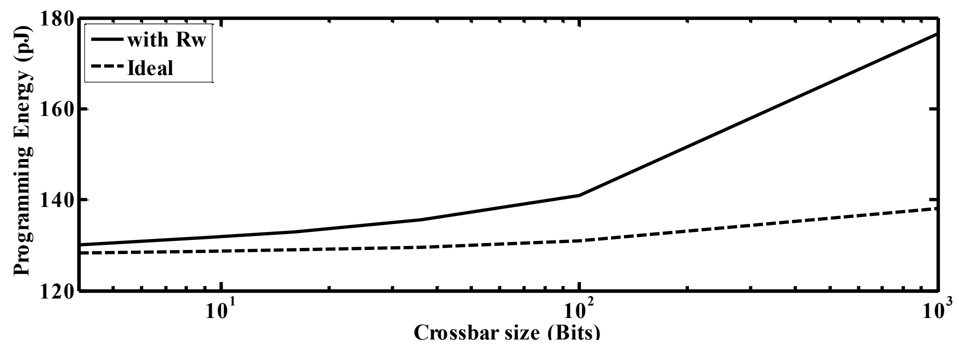


Figure 5.7: Energy consumed during programming in ideal and realistic nanocrossbars

Furthermore, it is noted from Figure 5.7 that the energy consumed in the realistic crossbar "with resistive connecting wires" was higher than the energy consumed in an ideal crossbar as expected. Additionally, with increasing crossbar size the deviation between an ideal crossbar and realistic one is more prominent. This is due to the increased dissipation of power across connecting wires.

5.3 Wire resistance effects mitigation

The presence of resistive connecting wires affects the amount of power supplied to program the memory cell. The cells will not be truly biased to V_{prog} or ground, thus resulting in programmed resistance levels different from the targeted ones. This affects the reliability of the read process depending on the resolution of the sense amplifier. Moreover, the connecting wire resistance does not only jeopardize the integrity of the read process, but it also decreases $R_{amorphous}/R_{crystalline}$ limiting the multilevel potential of PCM cell. Multilevel operation is the main advantage of the technology among emerging non-volatile memory technologies. In the following solutions to avoid wire resistance drawbacks are presented.

5.3.1 Programming Solution

In order to overcome partially crystallized programmed $R_{crystalline}$ levels and subsequent reading errors; the increase of wires energy consumption must be considered in programming schemes. It was noted that to achieve 100% crystallization i.e. targeted $R_{crystalline}$ level, the programming duration must be increased with increasing crossbar size as shown in Figure 5.8. This is in order to compensate for the decline in delivered energy. The added programming duration on the other hand, results in extra energy consumption, as seen in Figure 5.8.

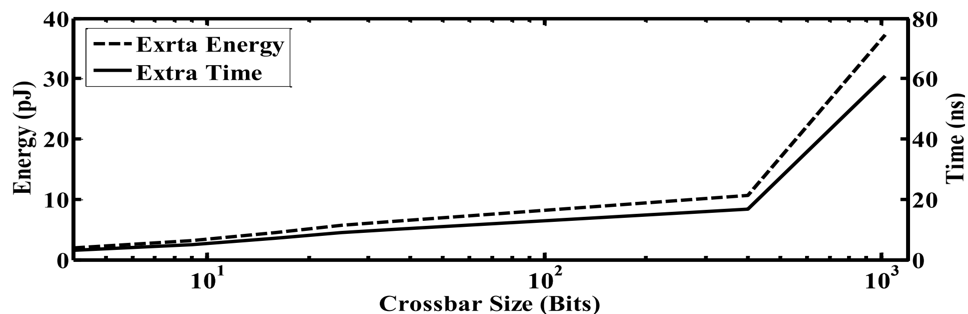


Figure 5.8: Added programming duration and energy required to program to targeted $R_{crystalline}$ level

5.3.2 Structural solution

The power drop across R_W leads to relatively high $R_{crystalline}$, thus jeopardizing the integrity of reading stored data and limiting crossbar size for reliable operation. Given that the degree of deviation of $R_{crystalline}$ from targeted level is directly linked to the position of the cell and distance from the voltage sources, a structural solution to minimize R_W effects can be adopted. In which, the memory array is segmented into smaller blocks that are accessible via address decoders as shown in Figure 5.9. And independent power rails are used to supply these blocks, in a similar concept to what is suggested in [25]. With the structure shown in Figure 5.9; the block size controls the worst case corner in contrast to the overall memory array size of the structure in Figure 5.1. This will allow building larger memory arrays with more reliability.

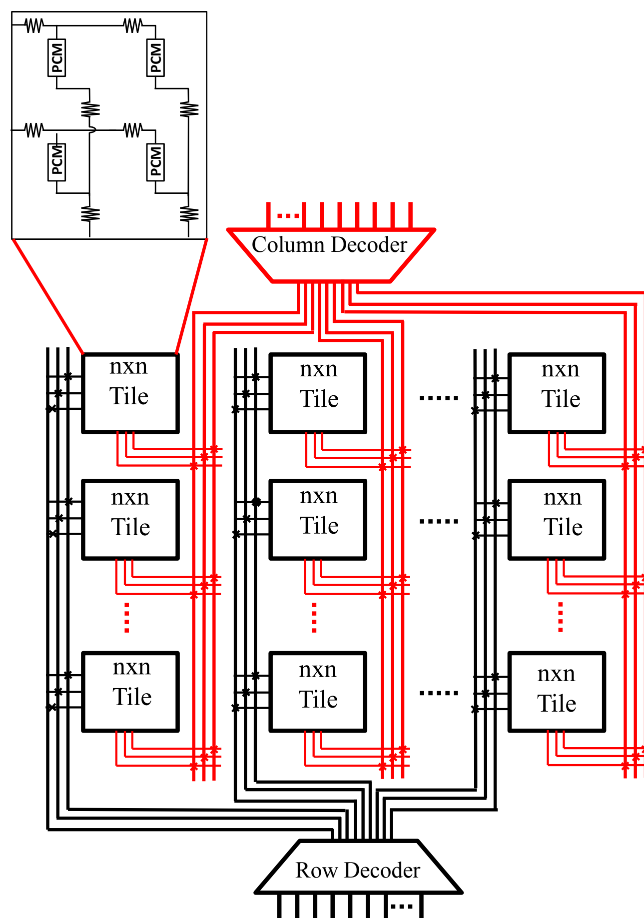


Figure 5.9: Block segmented nanocrossbar structure

Furthermore, when combining the programming solution with the structural solution; an optimization framework can be created. This is done by assessing the extra programming time required to minimize the deviation from the targeted level, and maximizing $R_{amorphous}/R_{crystalline}$ for a given tile size. Such a framework was outlined and tested for three different square tile sizes i.e. 2x2, 4x4, and 6x6 as shown in Table 5.3. It is derivative that with increasing tile size more programming time would be required to achieve the maximum $R_{amorphous}/R_{crystalline}$ i.e. 28 for the PCM model presented in Chapter 4. It should be noted that the bigger tile size, the less power rails required which implies less area overhead.

The trade-off between programming delay and area overhead is application oriented. I.e. for a given required $R_{amorphous}/R_{crystalline}$ (e.g. $R_{amorphous}/R_{crystalline}$ =12) in an application where speed is the limiting factor the optimization would be to choose smaller tiles for the least possible programming delay i.e. 4x4 would be a better choice according to Table 5.3. While for area critical applications, a bigger tile size can be chosen i.e. 6x6 to minimize the area taken by the power rails.

Table 5.3: Memory system optimization outline

Tile Size nxn	$R_{amorphous}/R_{crystalline}$	Extra Programming Time (ns)
2x2	28	3
4x4	11.46	3
	28	7
6x6	7.5	3
	13	7
	28	10

5.4 Leakage effects mitigation

5.4.1 Structural solution

In this section a structural solution to prevent the performance degradation related to energy dissipation caused by leakage current is presented. The standard crossbar structure is simulated and tested to be used as comparison reference. The developed leakage minimizing structure is then designed, simulated and compared to the standard structure. By comparing the performance of the developed crossbar structure, its efficiency and competence are validated.

5.4.1.1 Standard structure

The standard crossbar structure is constructed of an intersecting grid of Word lines (WL) and Bit lines (BL). A memory element is placed at each intersection point as depicted in Figure 5.10. In order to access a cell for either programming or reading; the address lines A0 and A1 are used. The address bits provided at the input of the controller will decide which row i.e. WL and column i.e. BL to be activated accordingly.

The write enable signal $WE/\overline{RE}$ dictates whether the cell is to be programmed or read. If the cell is to be programmed; DATA controller input decides the programming voltage applied, i.e. V_{P0} or V_{P1} program into logic 0 or 1 respectively as described by Table 5.4. E.g. if the PCM cell M0 in Figure 5.10 is to be programmed to logic 0 i.e. $R_{amorphous}$; A0A1 must be propped to “00”.This will activate WL1 and BL1, M0 resides in that intersection. While other Word/Bit lines will be floating i.e. unselected.

Furthermore, $WE/\overline{RE}$ signal will be high indicating that a writing operation is taking place. While DATA signal is set to zero, indicating that the cell is to be programmed into high resistance state that is equivalent to binary 0. Once these signals are activated; D0 will supply V_{P0} to M0 and hence programming it. All of the

addressing and programming signals are provided by the memory controller seen in Figure 5.10. The truth table of the controller unit in a standard crossbar structure Table 5.4, displays all possible programming and reading scenarios.

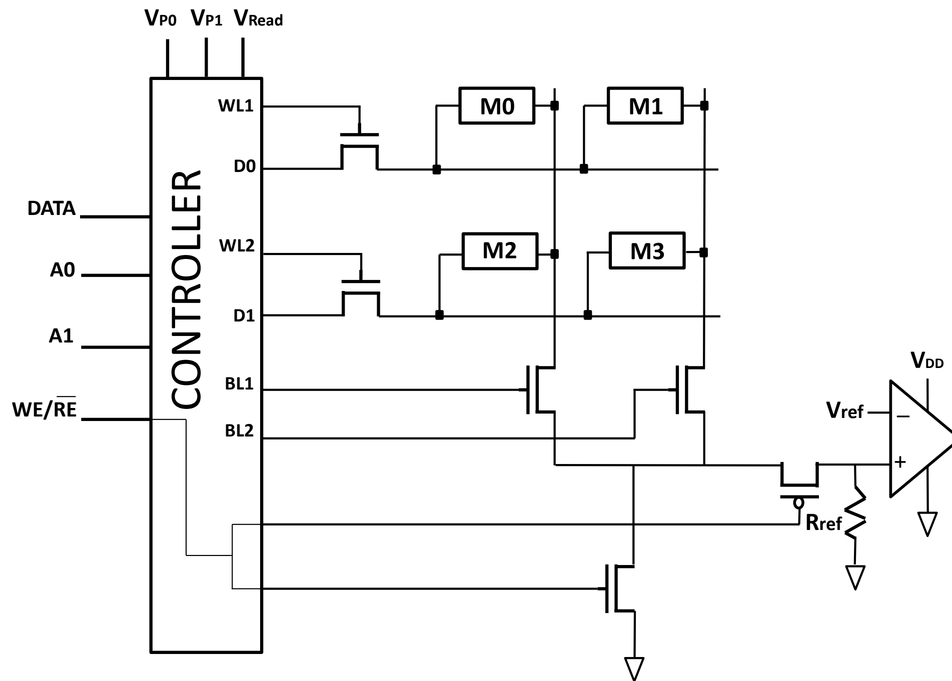


Figure 5.10: Standard crossbar structure

On the other hand, to perform reading operation; WE/$\overline{RE}$ is propped to zero and the reading voltage V_{Read} is supplied to the selected cell. The reading circuit is consisted of a comparator opamp, and a reference resistance R_{ref} that forms a voltage divider with the PCM cell, as seen in Figure 5.10. The voltage at the positive input of the comparator depends on the stored state on the PCM memory element. Accordingly, the evaluated output depends on the value stored on the PCM cell. When the accessed cell is at low resistive state $R_{crystalline}$; the voltage at the positive input of the comparator is higher than the reference voltage V_{ref}. Therefore, the comparators output swing to V_{DD} indicating a stored binary 1.

On the other hand, if the cell is at high resistive state $R_{amorphous}$; then the voltage at the positive input of the comparator is expected to be lower than the reference voltage $V_{ref.}$ The reference resistor R_{ref} and voltage V_{ref} must be selected properly; to insure

that V_{ref} falls between the output of low and high resistive states. This is in order for the comparator's output to fully swing between GND and V_{DD} (1V) and accurately evaluate the stored bit value. The selected values for R_{ref} and V_{ref} are listed in Appendix 5-1.

Table 5.4: Truth table of standard structure controller unit (x = don't care)

Operation	$WE/\overline{RE}$	A_0	A_1	DATA	D_0	D_1	WL_1	WL_2	BL_1	BL_2
Write	1	0	0	0/1	V_{P0}/V_{P1}	*Float*	1	0	1	0
	1	0	1	0/1	V_{P0}/V_{P1}	*Float*	1	0	0	1
	1	1	0	0/1	*Float*	V_{P0}/V_{P1}	0	1	1	0
	1	1	1	0/1	*Float*	V_{P0}/V_{P1}	0	1	0	1
Read	0	0	0	x	V_{Read}	*Float*	1	0	1	0
	0	0	1	x	V_{Read}	*Float*	1	0	0	1
	0	1	0	x	*Float*	V_{Read}	0	1	1	0
	0	1	1	x	*Float*	V_{Read}	0	1	0	1

5.4.1.2 Proposed structure

In order to minimize the energy loss in crossbars due to leakage current; without having to implement additional access devices which limit the scaling advantage offered by PCM elements; a structural solution is attempted. The proposed structure illustrated in Figure 5.11 limits leakage currents by removing sneak paths in the crossbar structure. In contrast to cells in the same row sharing Word lines; each cell is provided with an individual Word line. Therefore, this structure limits the stray currents that pass through shared Word line when a single cell in the row is addressed.

Furthermore, this structure offers simultaneous programming of multiple cells that share a Bit line in the crossbar. A similar concept was previously suggested for memristor based crossbars [118]. It aimed to avoid accidental programing of memristor cells and the subsequent reliability effects. However the design presented here is adapted for PCM based crossbars and aim to minimize power dissipation, since the PCM cells require programming energy levels relatively higher than what leakage generates.

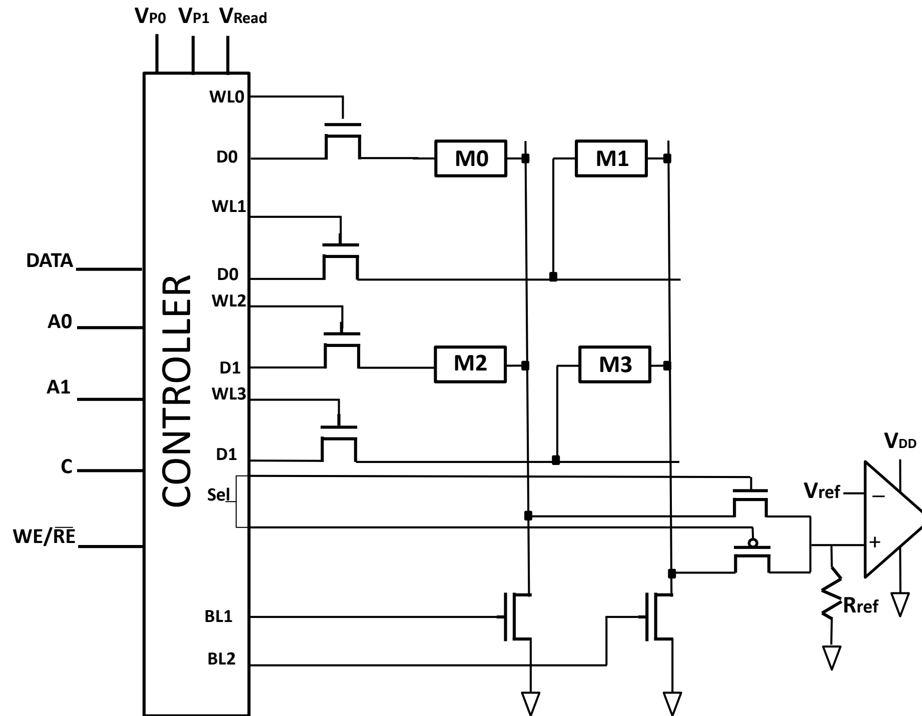


Figure 5.11: Adapted new crossbar structure

To perform a programming operation; all PCM cells sharing a Bit line can be programmed simultaneously. The addressed bit line can be accessed according to the address signal C. Moreover, the write enable signal $WE/\overline{RE}$ is set to high, and regardless of the value at the address lines; the cells at the selected Bit line according to C will be programmed. On the other hand, the read operation is performed in cells individually. Therefore, each cell is accessed during a read operation by activating the address line A0 and A1, in a similar fashion to that of the standard crossbar structure. The addressed cell is then supplied with V_{Read}, and a similar comparator assembly as the one described in the standard structure is used. However, a selection signal "Sel" indicates which Bit line is to be connected to the positive input of the read circuit opamp comparator. The "Sel" signal is activated by the memory controller according to the provided address in A0 and A1.

For example, if the PCM cells M0 and M2 in Figure 5.11 are both to be programmed to 0; then BL1 is selected by propping C to 0. As the cells are addressed;

$WE/\overline{RE}$ signal will be high indicating that a writing operation is taking place. Then by setting DATA to 0, D0 and D1 supply V_{P0} to both WL0 and WL2. Furthermore, to read the stored bit value in either of the programmed cells; address lines A0 and A1 are propped. For example to read M2; A0 and A1 are set to 1 and 0 respectively to activate WL2 and BL1 in which M2 resides. Then $WE/\overline{RE}$ signal will be low indicating a reading operation is in progress. Finally, V_{Read} will pass through the selected cell and the output of the opamp comparator will swing to 0 indicating the stored bit value as described.

In the same way of standard crossbars; all of the addressing and programming signals are provided by the memory controller as depicted in Figure 5.11. Truth table of the controller unit of the proposed crossbar structure Table 5.5 displays all possible programming and reading scenarios.

Table 5.5: Truth table of novel structure controller unit (x = don't care)

Operation	$WE/\overline{RE}$	A_0	A_1	C	DATA	D_0	D_1	WL_0	WL_1	WL_2	WL_3	BL_1	BL_2	Sel
Write	1	x	x	0	0/1	V_{P0}/V_{P1}	V_{P0}/V_{P1}	1	0	1	0	1	0	*Float*
	1	x	x	1	0/1	V_{P0}/V_{P1}	V_{P0}/V_{P1}	0	1	0	1	0	1	*Float*
Read	0	0	0	x	x	V_{Read}	*Float*	1	0	0	0	1	0	1
	0	0	1	x	x	V_{Read}	*Float*	0	1	0	0	0	1	0
	0	1	0	x	x	*Float*	V_{Read}	0	0	1	0	1	0	1
	0	1	1	x	x	*Float*	V_{Read}	0	0	0	1	0	1	0

5.4.1.3 Standard and proposed crossbar structures performance comparison

The standard and proposed crossbar structures depicted in Figure 5.10 and Figure 5.11 respectively; are simulated in LTSpice IV, using signal and parameters stated in Appendix 5-1. The simulations are carried with the purpose of testing the feasibility of the proposed structure to improve the memory crossbar performance, and its ability to mitigate energy loss due to leakage currents. The standard crossbar structure is used as a baseline for comparison, and the structures were tested for both reading and

writing processes for both high resistive and low resistive states i.e. binary 0 and 1 respectively.

A. Energy consumption in the crossbar

The dissipated energy during programming pulse i.e. the energy dissipated in all memory cells (M0 – M3) is the same in both structures, as seen in Figure 5.12 This is explained by the fact that the voltage applied to the grid during programming operation is the same regardless of the structure. While for the reading process; the proposed structure demonstrated superior performance as expected. With more than an order of magnitude improvement in consumed energy of reading a stored 0, and almost six times less energy when reading a stored 1. This was due to the elimination of leakage paths; which resulted in most of the applied current to pass through the targeted cell rather than untargeted ones.

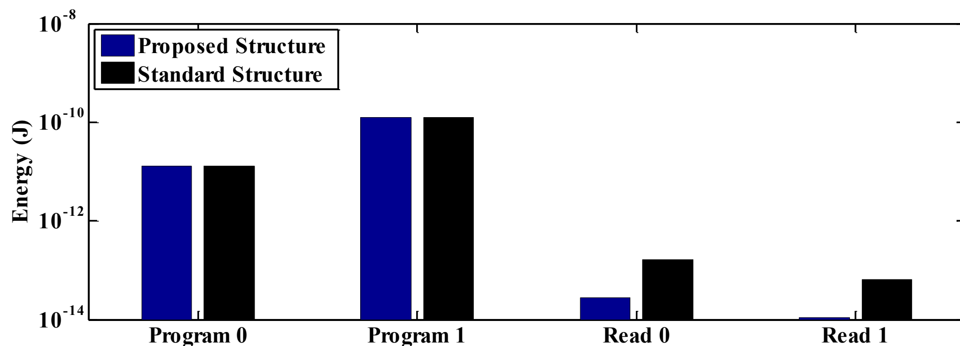


Figure 5.12: Summary of simulation results of dissipated energy during reading and programming

B. Energy dissipation due to leakage currents

The simulation results seen in Figure 5.13 are of leaked energy during the programming and reading. The results of the energy dissipated in untargeted cells showed a great variation between the two structures as expected. The proposed structure showed two and six orders of magnitude less leaked energy during programming to 0 and 1 respectively. This is directly tied to the elimination of

leakage paths in this structure by utilizing separate Word lines for each memory cell. Moreover, the proposed structure demonstrated more that thirteen orders of magnitude less leakage energy during the reading process as noted from Figure 5.13. Furthermore, it was noted that the leakage of reading process in the novel structure is the least of all. This is due to the fact that in addition to eliminating leakage paths, reading voltage V_{Read} is much smaller than programming voltage V_P, along with shorter reading delays in the novel structure.

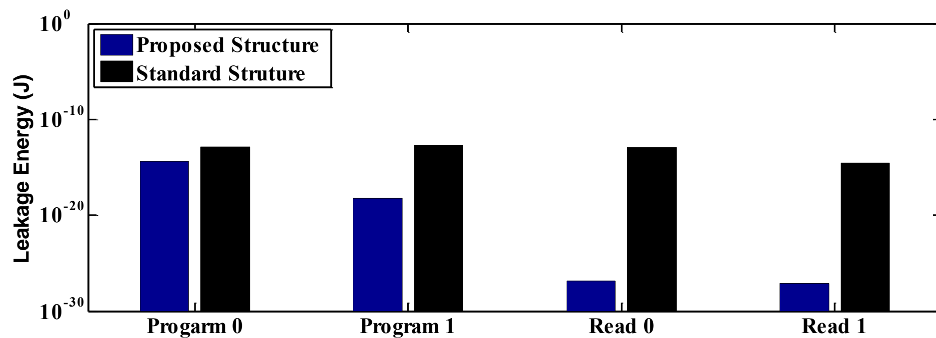


Figure 5.13: Summary of simulation results of leaked energy during reading and programming.

C. <u>Programming and reading delays & programmed $R_{crystalline}$</u>

The programming duration for both structures was set to a constant value in order to evaluate the effect of underlying structure on the programmed resistance state. However, the built in capability to program all cells sharing a Bit line in the novel structure, gave it a superior performance in terms of programming delay per cell as shown in Table 5.6. This particular improvement in programming time is an additional architectural advantage along with leakage elimination.

Furthermore, the reading delay was measured as the time for the output to fully swing to 0 or 1 from the moment the address lines and the read signal were propped. It was found that the proposed structure demonstrated almost three times less delay to read a stored 0. Also, it showed more than an order of magnitude less time to read a stored 1 as seen from simulation results outlined in Table 5.6. This is due to larger

current supplied to the comparator due to less leakage, resulting in a faster voltage swing.

Table 5.6: Delay and programmed level simulation results summary

Operation	**Novel Structure**	**Standard Structure**
Programming 0 Delay (s)	10 n/N*	10 n/cell
Programming 1 Delay (s)	200 n/N*	200 n
Reading 0 Delay (s)	1.23μ	3.31 μ
Reading 1 Delay (s)	0.929 μ	1.41 μ
Programmed $R_{crystalline}$ (Ω)	16.3213K	30 K
Programmed $R_{amorphous}$ (Ω)	200 K	200 K

*(N≈ No. of cells in a Bit line)

The last tested metric was the programmed state. It was found that when programming to high resistive state i.e. storing binary 0; both structures cells were fully programmed to 100% amorphous phase of 200KΩ. While when programming to low resistive state; the standard structure demonstrated higher programmed resistance compared to the novel structure as shown in Table 5.6. This is a direct result of leakage, since less energy is delivered to the targeted cell. This results in partially crystallized cells, and accordingly a higher programmed $R_{crystalline}$. This particular leakage effect in standard structure jeopardizes the reliability of memory operation, and furthermore limits multilevel operation.

5.4.2 AC sensing

During read process; leakage currents in PCM based crossbars cause unnecessary energy loss. Therefore, in this section we explore a leakage minimizing sensing method that was first suggested in [119]. The sensing scheme was targeted to minimize reliability issues in Memristors as leakage currents are sufficient to program Memristor cell. However, the AC reading technique in [119] is considered compatible for PCM operation after certain modifications. Even though it will serve to a different

purpose, i.e. energy saving rather than read disturbs avoidance. The AC reading circuit is designed and tested in PCM based crossbar memories in simulation environment. Then it was compared to the standard DC sensing method. The comparison was carried out in order to accurately evaluate the improvement offered by the AC reading technique.

5.4.2.1 Proposed AC Sense Circuit

The AC sensing circuit depicted in Figure 5.14 was constructed with the PCM cell acting as the resistive element in the low pass filter. According to the cell resistance level; the input AC signal will be attenuated to different levels as seen in Figure 5.15. The output of the filter at point A is then rectified in the second stage of the filter circuit. The signal at point B smoothed by the capacitor C2; is then used as an input to the comparator operational amplifier. That is the last stage of the reading process. In this last stage the output at point B is compared against a reference value V_{ref2}. The output at point C swings to either 0V or 1V according to the voltage at point B.

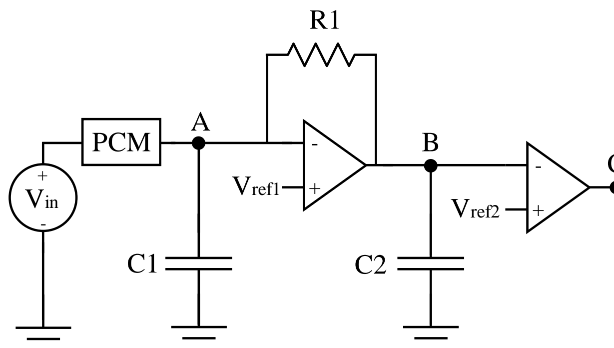


Figure 5.14: AC sense circuit.

The values of the sense circuit parameters i.e. resistor, capacitors, operating frequency and signal amplitude, are listed in Appendix 5-2. They were adapted to the used SLPCM model described in Chapter 4. As the parameters values have significant effect on the signal attenuation and the operation of the AC reading circuit. The circuit is sensitive to parameters change, e.g. with all other parameters

values fixed if C2 is increased above 1.12pF; the circuit fails in reading the stored Bit. Similarly the circuit fails if R1 exceeds the range (90.04-1MΩ).

5.4.2.2 AC sensing and DC sensing performance comparison

The proposed AC reading circuit was first tested in a standalone cell to insure its reliability. It was tested for both binary states 0 and 1 i.e. $R_{amorphous}$ and $R_{crystalline}$ respectively. The simulation results displayed in Figure 5.15 showed how the designed sense circuit responds to the applied reading voltage (V_{Read}) at each stage of sensing. The applied V_{Read} was kept well below programming voltage to avoid programming the cell.

The designed circuit successfully produced two distinguishable outputs corresponding to $R_{crystalline}$ and $R_{amorphous.}$ That distinguishable output is a result of each stage in the designed circuit in Figure 5.14 operating properly. The attenuation of V_{Read} at the output of the designed low pass filter in point A showed clearly different attenuation levels as seen in Figure 5.15. It is noted that the voltage at point A when reading a cell at $R_{crystalline}$ is identical to the input voltage i.e. non-attenuated. A slight phase shift due to the capacitor is noted. While for cells at $R_{amorphous}$; the filter attenuated the applied V_{Read} to almost 50%.

Moreover, for both resistive states the voltage at point A showed a DC offset compared to the input. This is due to V_{ref1} at the non-inverting input of the amplifier shown in Figure 5.14. The voltage at the second stage of the sensing circuit i.e. point B, is the amplified and slightly rectified output of the first stage. It was noted that a clear difference between the resistive states is well maintained and amplified at this stage. The final stage of the sensing circuitry is a standard comparator with a selected reference voltage that falls between the two possible outputs at point B. And based on the sensed voltage the comparator output fully swings to 0 or 1; indicating the stored bit in the cell according to its resistive state.

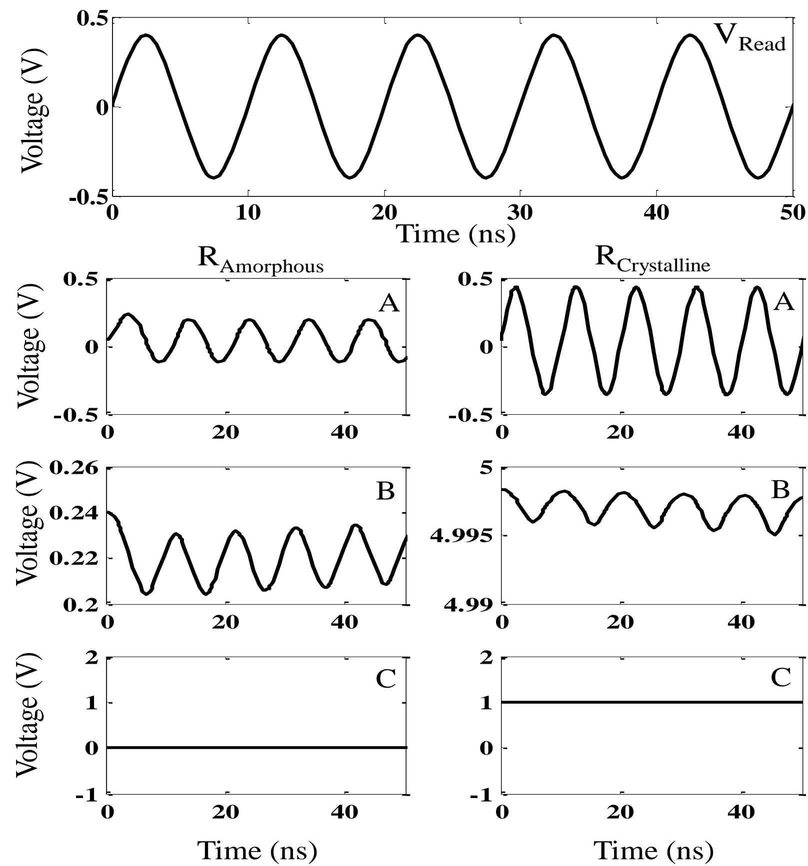


Figure 5.15: The AC sense circuit reading input and signals at points A, B, and C

Furthermore, the designed sensing circuit was tested in PCM based crossbar structure seen in Figure 5.10. The energy and accordingly the power loss due to leakage during reading are then measured. The performance of the proposed AC sensing circuit was compared against the conventional DC sensing depicted in Figure 4.24.

The proposed AC sensing method functioned properly in crossbar structure and it showed superior performance compared to a standard DC sensing method. The simulation and comparison results listed in Table 5.7 were measured for 10μ seconds long reading pulses. From the simulation results it is noted that the dissipated energy due to leakage is reduced as expected by 48% and 99% for a stored 0 and 1 respectively. Accordingly the dissipated power due to leakage was reduced by 48% and 46% to read a stored 0 and 1 respectively.

However it should be noted that despite the fact that the AC sensing circuit offers better energy consumption, it requires additional area overhead compared to DC scheme. Since the proposed sensing method requires more components, which calls for a trade-off between area overhead and energy consumption. Moreover, the simulation results obtained for the 2x2 crossbar is a base line that can be further extended to larger sizes of memory crossbars, knowing that leakage is proportional to the size of the crossbar, so leakage can be predicted.

Table 5.7: AC Sense circuit performance comparison summary

Process	AC Sensing	DC Sensing
Reading 0 leakage energy	29.6pJ	57.6pJ
Reading 1 leakage energy	0.177pJ	66.4pJ
Reading 0 leakage power	2.96μW	5.76μW
Reading 1 leakage power	3.54μW	6.64μW

5.5 Summary

In this chapter, PCM based crossbar memory structures were implemented and studied in simulation environment. The PCM cell model designed in Chapter 4 was used as the memory element in the modelled PCM based nanocrossbar memories, and performance issues facing PCM based nanocrossbars were addressed.

The energy loss across wire segments was simulated and studied. It was noted that it leads to almost 40% deviation in the programed low resistive state from the targeted levels. This effect compromises the integrity of the stored data and decrease the high to low resistance ratio by 90%. Therefore, a programming solution was proposed and tested. The programming solution retained reliability however; it increased programming energy consumption and delay by 40pJ and 60ns respectively per operation. Moreover, a structural solution was proposed, where the memory

crossbar is segmented into smaller units that are less affected by energy loss across connecting wires.

Moreover, a structural solution and a reading circuit were designed and tested to minimize leakage currents effects. The structural solution led to more than six orders of magnitude reduction in leakage energy. Additionally, it offered up to N time's improvement in programming delay where N is a metric proportional to the size of the architecture. And lead to more than an order of magnitude improvement in reading delay.

The second method proposed to reduce leakage during reading was the use of AC sources in contrast to the standard DC reading method. From simulation results it is noted that the dissipated energy due to leakage is reduced as expected by 48% and 99% for a stored 0 and 1 respectively. While the dissipated power due to leakage was reduced by 48% and 46%; to read a stored 0 and 1 respectively.

CHAPTER 6

SLPCM AND MPLCM IN MEMORY AND LOGIC APPLICATIONS

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6.1 Overview

In this chapter the use of PCM element in memory and logic applications is explored. In section 6.2, SLPCM and MLPCM circuit models presented in Chapter 4 are utilized as memory elements in an active crossbar memory structure. The proposed memory application is tested for crossbars at different sizes, and a performance comparison between SLPCM and MLPCM based memories in terms of delay, energy, and area was conducted. In section 6.3, a logic application of time-aware sensing coupled with MLPCM was implemented, where MPLCM is used as memory element in a Look Up Table (LUT). The suggested MLPCM based LUT was constructed with the MLPCM circuit model designed in Chapter 4. Then it was tested with and without the use of time-aware sensing proposed in Chapter 4. Finally in section 6.4, the performance of PCM based memory is compared to that of the emerging Memristor based NVM technology and to the currently used SRAM memory technology. The comparison was in terms of energy, delay, and area.

6.2 SLPCM and MLPCM based memory crossbar architecture

The standard crossbar architecture described in Figure 6.1 was utilised to construct PCM based memory structure. In this structure a PCM cell is placed at each intersection point of connecting wire mesh grid. Precisely, square grids with the number of columns i.e. Bit lines being equal to the number of rows i.e. Word lines as shown in Figure 6.1. The designed memory contained a memory controller and a reading circuit. The memory controller is responsible for both addressing e memory cells and signalling the proper operation to be executed. The reading circuit intuitively performs the reading operation whenever the memory controller props the reading signals.

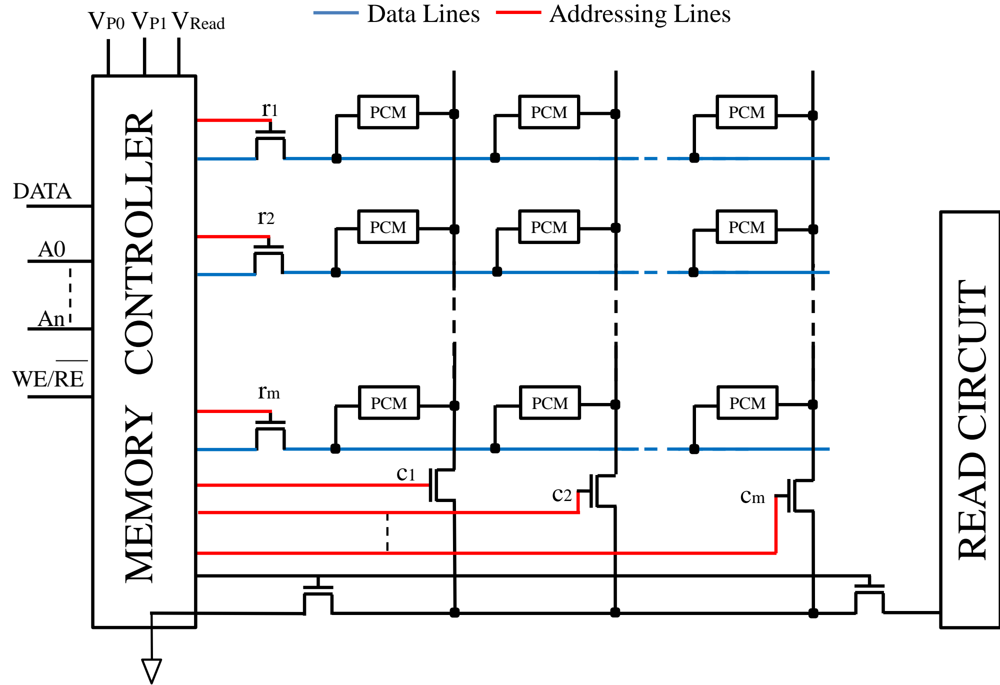

Figure 6.1: PCM based crossbar memory structure

6.2.1 Memory controller

The memory controller tasks include providing addressing signals to select memory cells, and propping the appropriate operation signal, i.e. either reading or writing. To address cells in a 2^n sized crossbar, n address lines are required. An address decoder built in the memory controller as shown in Figure 6.2(a) was used. The address decoder activates the proper selection switches (r_m,c_m) of the Word and Bit lines depicted in Figure 6.1 corresponding to the addressed cell. While switches connected to non-addressed cells are turned off.

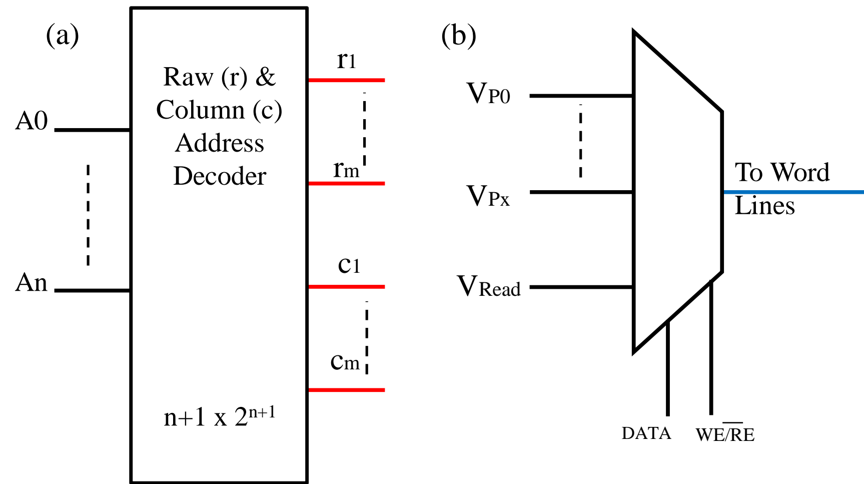

Figure 6.2: Memory controller's (a) Address decoder, and (b) Operation selector.

The other part of the memory controller is the read and write signal selectors. Based on an external enable signals (i.e. $WE/\overline{RE}$ & DATA) the controller decides which operation is to be executed. The write and read enable signal ($WE/\overline{RE}$) decides if the executed operation was a write or read operation. If it was a write operation; (DATA) signal dictates the written binary value i.e. 0 or 1. Based on these control signals; one of the predetermined programming or reading voltage levels (V_{Px}, V_{Read}) is selected to be applied to the targeted memory cell through the selected Word line. The operation selector behaviour for SLPCM and MLPCM is described in Table 6.1 and Table 6.2 respectively. It is noted that when the reading enable signal is propped i.e. "$WE/\overline{RE}$=0" regardless of DATA, V_{Read} is selected as the source supplied to the addressed memory cell. Alternatively, when the writing signal is propped "$WE/\overline{RE}$=1", DATA signal dictates which of the programming voltage sources (V_{P0}-V_{Px}) is to be selected and supplied to the addressed memory cell.

Table 6.1: Truth table of SLPCM Memory controller's operation selector unit

DATA	$WE/\overline{RE}$	Output to Word lines
*X	0	V_{Read}
0	1	V_{P0}
1	1	V_{P1}

Table 6.2: Truth table of MLPCM Memory controller's operation selector unit

DATA Bits		$WE/\overline{RE}$	Output to Word lines
D0	D1		
*X	*X	0	V_{Read}
0	0	1	V_{P00}
0	1	1	V_{P01}
1	0	1	V_{P10}
1	1	1	V_{P11}

*(X ≈ don't care)

6.2.2 Read circuit

Along with the memory controller, the read circuit is an essential part of the crossbar memory structure. In this work, a DC reading scheme as shown in Figure 6.3 is adopted. An opamp comparator is used to compare the state of the selected memory cell against a predefined reference value. This is done by applying a small DC read voltage V_{Read} that is well below the lowest applicable programming voltage V_P. This is to avoid altering the state of the cell after reading and thus jeopardizing the integrity of the stored data post reading.

Intuitively the read circuit structure is different for SLPCM and MLPCM. SLPCM requires a single reference value and thus a single comparator. In contrast; in MLPCM at least n-1 reference levels are required for a cell that can be programmed to n possible levels. In this work four possible resistive levels can be achieved to store two binary bits of data. Therefore, three reference levels are required and subsequently three comparators are required. Thus, making the MLPCM read circuit more complicated than the SLPCM which effects both the reading delay and read circuit area as will be discussed in section 6.2.3.2. The time-aware sensing scheme described in Chapter 4 was utilised in MLPCM based crossbar test structure. While

the standard reading circuit is used for SLPCM based crossbar test structure, as shown in Figure 6.3.

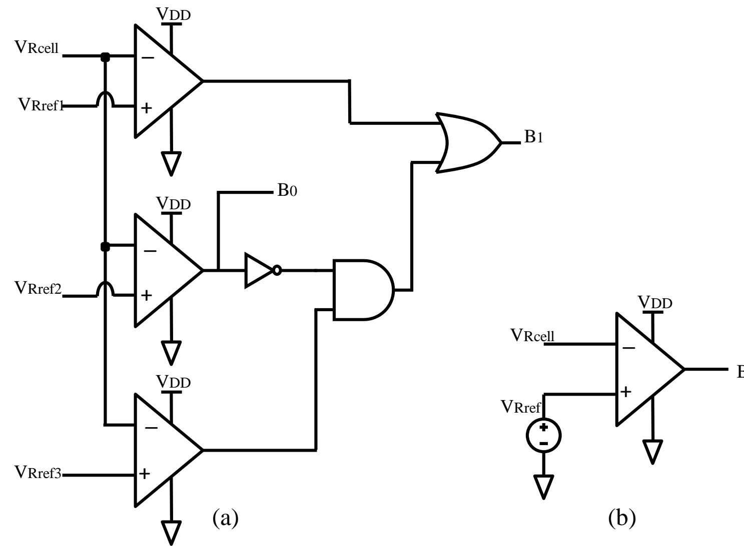

Figure 6.3: Read Circuit Design for (a) MLPCM and (b) SLPCM cells

6.2.3 Simulation results and discussion

Both SLPCM and MLPCM based memory crossbars were tested at three different sizes of crossbars namely 16, 64 and 256 Bits i.e. 4x4, 8x8, and 16x16. Square crossbars were tested in simulation environment to evaluate the effect of array size on the operational characteristics. I.e. the delay and energy consumed during programming and reading a single memory element on the crossbar array.

6.2.3.1 Energy consumption

6.2.3.1.1 Test procedure

The energy was measured for programming and reading a single memory cell at all possible binary states, i.e. “0” and “1” for SLPCM and “00”, “01”, “10” and “11” for MLPCM. To evaluate the programming energy; the energy consumed within the entire crossbar during the programming pulse duration was measured. That way the measured programming energy included both the efficiently used energy to program the cell, and the leakage energy in non-targeted PCM cells. Similarly, the reading

energy is measured as the energy consumed by the crossbar during the application of a reading pulse.

6.2.3.1.2 Simulation results

A. Corner levels write/read energy SLPCM and MLPCM consumption

The energy consumed to write into and read corner resistive levels for both SLPCM and MLPCM was measured and compared. The corner levels are binary "0" and "1" for SLPCM, and "00" and "11" for MLPCM. The measurement of a 4x4 crossbar are initially carried and analysed. Then 8x8 and 16x16 crossbars are tested to evaluate the effect of crossbar size.

It was noted from simulation results shown in Figure 6.4 that MLPCM consumes about two times the energy consumed by SLPCM to perform a write operation. On the other hand, the energy consumed during read process of a stored "1" in MLPCM was over an order of magnitude more energy compared to SLPCM. This is due to MLPCM longer reading delay that will be discussed in section 6.2.3.2.

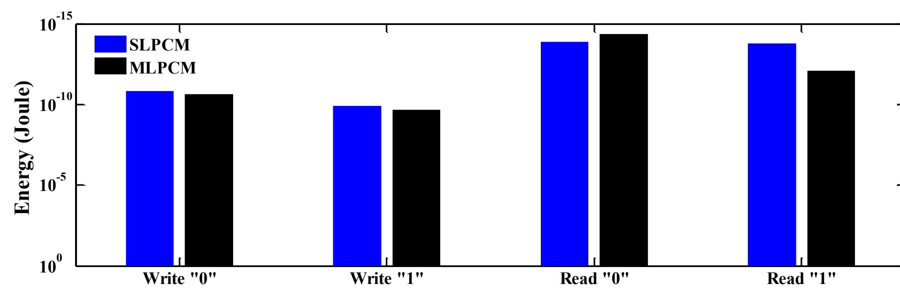

Figure 6.4: 4x4 SLPCM and MLPCM based crossbars energy comparison

Conversely, MPLCM consumed considerably less energy "3.5 times less" than that consumed in SLPCM when reading a stored "0".The reading delay of a stored "0" is the only operation where SLPCM consumes more energy than MLPCM. The reason behind the out of character reading delay is the different reading circuit setup used for SLPCM and MLPCM as described in section 6.2.2. SLPCM uses the fixed reference approach. On the other hand the MLPCM uses the adaptive time-aware sensing scheme presented in Chapter 4.

MLPCM model accounts for the drifting behaviour resulting in an increasing difference with time between the evaluated resistance and the predesigned reference value. Despite the fact that the reference resistance is time adapting as well, but the rate of change of the reference resistance in time is very small compared to the rate of programmed resistance change. With such increasing difference; less time is required by the reading circuit comparators, particularly the second comparator responsible for generation B_0 as shown in Figure 6.3 to fully swing the output to zero volts. This behaviour is not evident when comparing the reading energy of a stored binary “1” due to the lack of resistance drift phenomena in the corner low resistance level.

B. <u>Crossbar size effect</u>

It was noted that MLPCM maintains the trend of consuming more energy than SLPCM for larger crossbars i.e. 8x8 and 16x16. It was noted that the consumed energy increased proportionally with increasing crossbar size. MLPCM consumed roughly four and five times more writing energy compared to SLPMC in 8x8 and 16x16 crossbars respectively, as seen in Figure 6.5 and Figure 6.6. Furthermore, MLPCM consumed more than two orders of magnitude more energy while reading a stored “1”. Additionally, the trend of requiring less energy to read a stored binary “0” is as well maintained. Additionally, for all tested crossbar sizes, MLPCM consumed 3.5 times less energy reading a “0” compared to SLPCM.

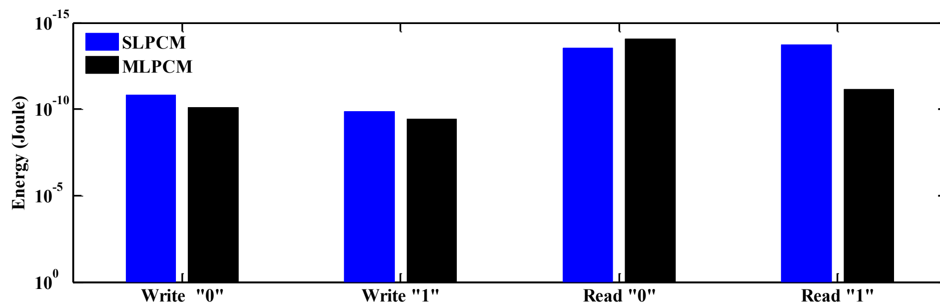

Figure 6.5: 8x8 SLPCM and MLPCM based crossbars energy comparison

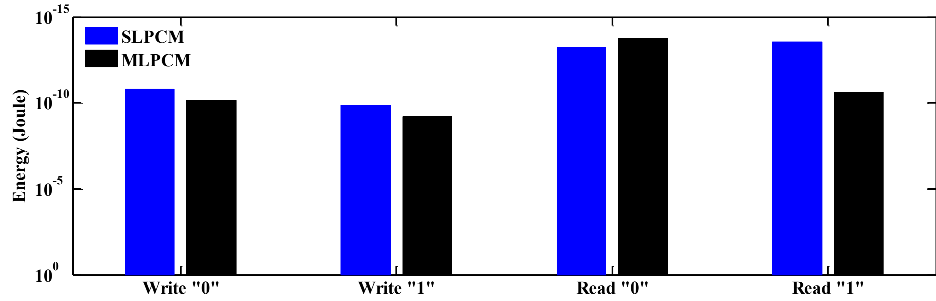

Figure 6.6: 16x16 SLPCM and MLPCM based crossbars energy comparison

C. Intermediate and corner levels MLPCM write/read energy consumption

Beyond the comparison of corner levels in SLPCM and MLPCM, the performance of all possible programmable states in MLPCM was compared. The simulation results showed a pattern of increasing consumed energy with increasing stored binary value and crossbar size, for both programming and reading as seen in Figure 6.7 and Figure 6.8 respectively.

The increase of consumption with increasing stored binary value is tied to the increase in both reading and writing delay as will be discussed in section 6.2.3.2. However, the increase of the consumed energy with increasing crossbar size is linked to the increase of leakage energy effect. Given that with larger crossbars more leakage energy is consumed as evident by simulation results.

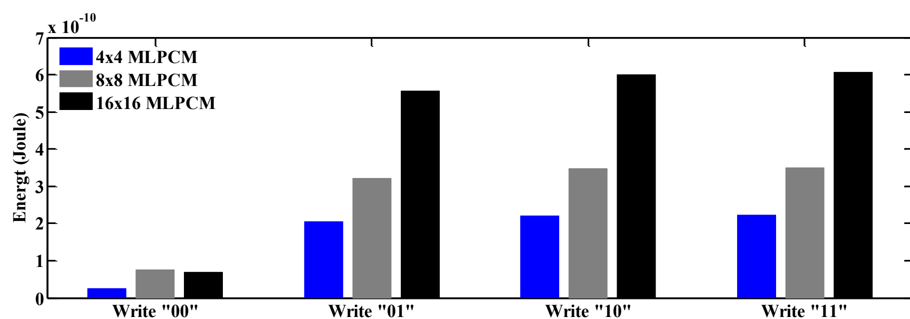

Figure 6.7: MLPCM writing energy comparison

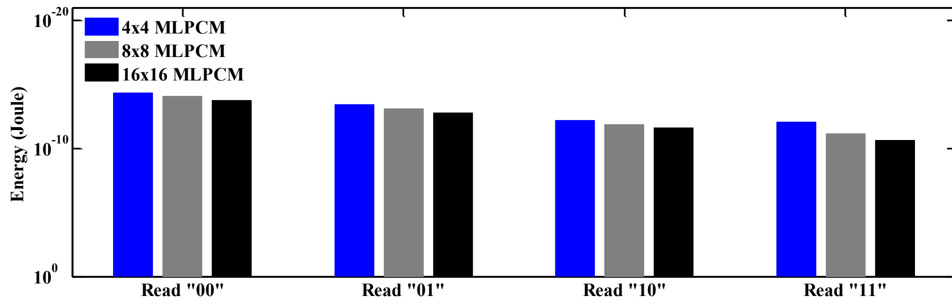

Figure 6.8: MLPCM reading energy comparison

D. Leakage energy consumption

It is noted that the energy leakage during writing increases from 36% to 63% of overall consumed energy, when the crossbar size increase from 8x8 to 16x16. Energy leakage during the reading process was even more prominent, with an increase from 50% to 75% of overall consumed energy, corresponding to an increase of size from 8x8 to 16x16.

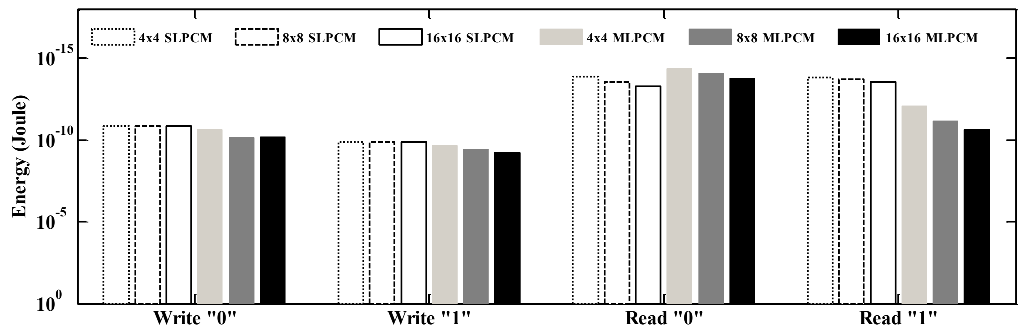

Figure 6.9: SLPCM and MLPCM energy consumption

Overall it can be concluded that MLPCM generally consumes more energy when compared to SLPCM as can be seen in Figure 6.9. The numeric values of simulation results for delay and energy consumption in SLPCM and MLPCM based crossbar memories can be found in Appendix 6-1 and Appendix 6-2 respectively.

6.2.3.2 Delay

6.2.3.2.1 Test procedure

Multilevel storage is achieved by controlling the programming pulse duration rather than controlling the amplitude as presented in the MLPCM cell model in Chapter 4. Therefore, the writing delay is measured as the minimum time required programming the targeted cell into the resistive level corresponding to stored data binary value. On the other hand, the reading delay is measured as the time from activating read signal until the output of the reading circuit fully swings to the expected voltage state with an accuracy of 10^{-3} i.e. "<1mV" for binary "0" and ">999mV" for binary "1".

6.2.3.2.2 Simulation results

A. <u>Programming delay</u>

The average writing delays is persistent for all crossbar sizes of both SLPCM and MLPCM, as the crystallizing time is independent of the memory structure and more correlated with the cell material properties. Thus the writing delay is dependent on the targeted resistance level. The shortest programming delay is that of the highest resistive state "00" as seen in Figure 6.10, since it is achieved by applying a high steep pulse.

On the other hand, the longest programming delay is that of the lowest 100% crystalline resistive state "11". This is due to that fact that the length of the crystallizing pulse is directly proportional to the targeted crystalline ratio. The intermediate levels are achieved by applying a pulse with the 100% crystallizing pulse amplitude but for durations needed to achieve only partial crystallization (97% and 63%) as depicted in Figure 6.10.

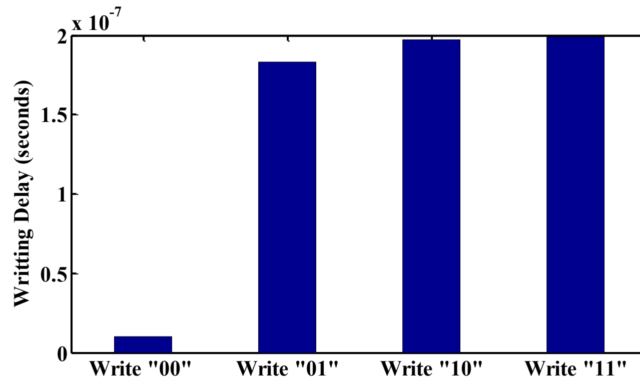

Figure 6.10: Average writing delay for all programmable states

B. Reading delay

The reading delay is dependent on both the programmed resistive state, and the design of the used reading circuit. The comparison of the reading delay in SLPCM and MLPCM was carried for the programmed corner resistive states. The simulation results in Figure 6.11 show that for the low resistance level "11"; MLPCM requires 10 times the reading delay of SLPCM. This is due to the simple structure of the read circuit of SLPCM that utilizes a single opamp comparator. While reading delay of "00" in MLPCM is slightly less than that of SLPCM. This is due to the resistance drift effect encountered in the MPLCM model. The drift leads to an increase of the comparators inputs difference; thus resulting in a faster swinging of the output as noted from Figure 6.12.

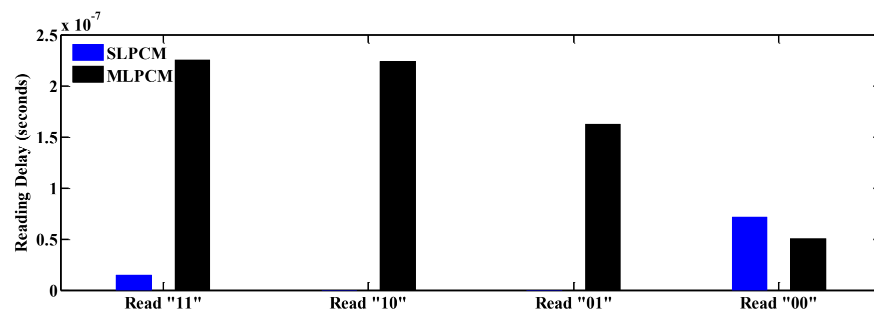

Figure 6.11: Average reading delay for all programmable states

The simulation results of reading delays at intermediate resistive states are shown in Figure 6.11 and Figure 6.13. From these results it was noted that longer reading delays are encountered with lower resistive levels.

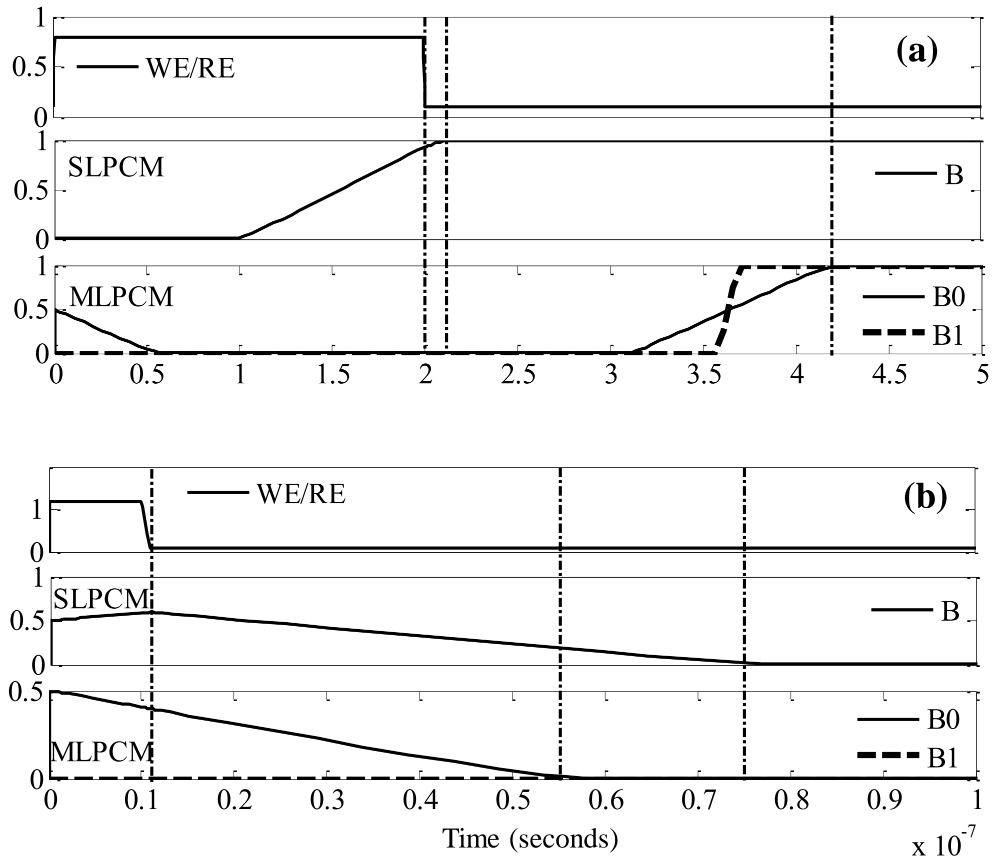

Figure 6.12: Reading delay for programmed (a) “11” and (b) “00” in SLPCM and MLPCM

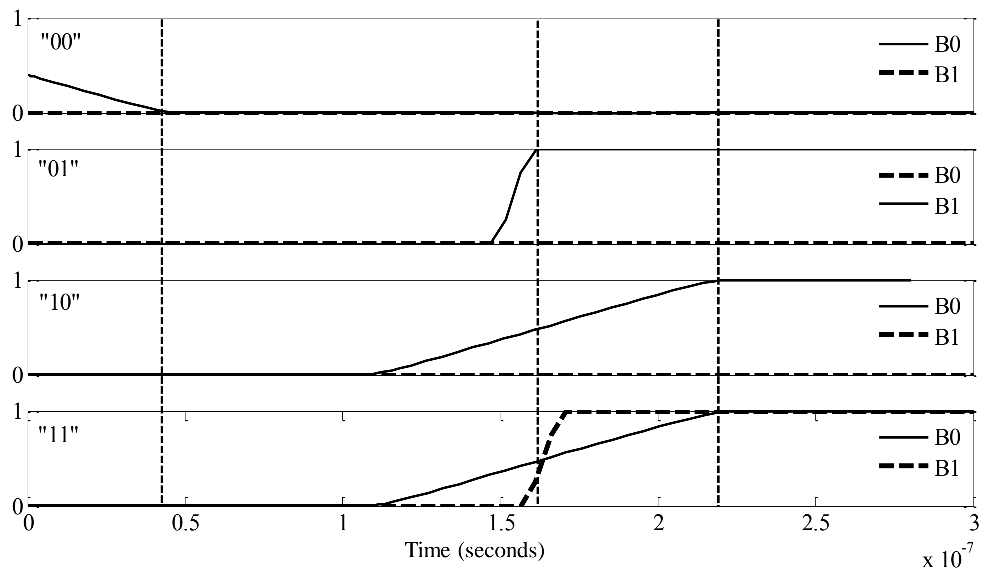

Figure 6.13: Measuring reading delay of all programmable states in MLPCM

6.2.3.3 Density

When performing a density comparison MLPCM have the advantage; as MLPCM offers high density achieved by multibit storage in a single memory cell. In the current comparison a four level cell that stores two Bits per cell is compared against a single Bit storing cell. This allows the tested MLPCM to offer double the density of SLPCM. It should also be noted that up to 16 resistive levels per cell can be achieved making a possibility of four folds of density increase.

However, the reading circuit of MLPCM occupies more surface area compared to SLPCM reading circuit. This is due to its complexity and added number of components, as can be noted from Figure 6.3. Given that the number of required comparators is proportional to the number of possible resistive levels. This is in contrast to the simple DC sense circuit scheme adopted in SLPCM reading circuit, where a single opamp comparator is used. Thus, making the two Bits per cell MLPCM sense circuit at least three folds larger in surface area compared to SLPCM; a ratio that is expected to increase with increased MLPCM density.

6.3 MLPCM based LUT

LUTs are equivalents to truth tables of logic functions, and are used to configure combinational logic functions in SRAM based FPGAs. But such SRAM based LUTs inherit the drawbacks of SRAM cells, i.e. they are volatile and consume energy and area; as the single SRAM cell is constructed of six transistors and stores a single bit. Therefore, the merits of MLPCM such as non-volatility and high density makes it an attractive alternative to SRAM in LUTs [18], [127]. As an application of MLPCM; this work presents two inputs MLPCM based LUT. The proposed two inputs LUT utilizes four MLPCMs (M0-M3) as shown in Figure 6.14(a). The MLPCMs are connected at the junctions of a 2x2 nanocrossbar as depicted in the inset of Figure 6.14(a). The input to the LUT is provided through a two inputs address decoder that

decodes the four possible inputs to a corresponding memory location i.e. MLPCM cells.

6.3.1 LUT half adder configuration

To explore MLPCM potential as LUT memory element; a half adder depicted in Figure 6.14(b) was configured in a two bit MLPCM based LUT. With A and B considered as the inputs of the half adder, and sum and carry the outputs as indicated in Figure 6.14(c). Each MLPCM in the LUT can store two bits by being programmed into one of the four resistive levels designated in Table 4.2 in Chapter 4. Therefore in each MLPCM, the sum and carry values of their corresponding inputs are stored. For example if the inputs of the half adder are "01", then sum and carry are "1" and "0" respectively. The input "01" refers to M1, which is programmed to L2 with 75% crystalline fraction as indicated in Table 4.2. In a similar fashion when M0, M2, and M3 are addressed; they are programmed to L4, L2, and L3 respectively. Thus the MLPCM based two inputs LUT is successfully configured to a half adder circuit.

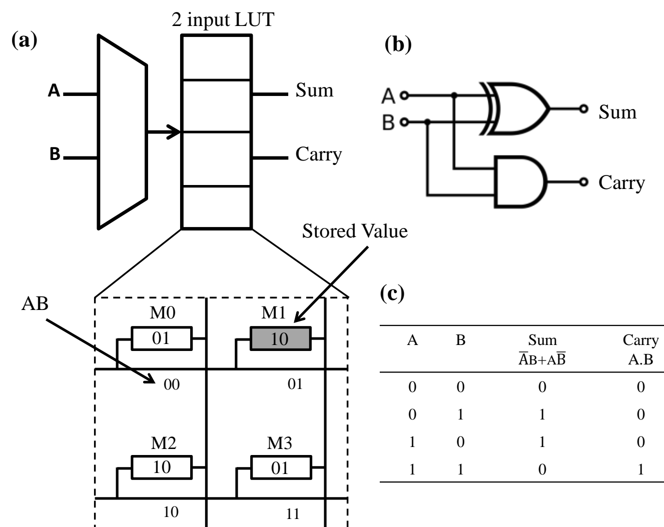

Figure 6.14: (a) 2 inputs MLPCM based LUT representation, (b) Half adder circuit, and (c) its Truth table.

6.3.2 Simulation results and discussion

Despite the logic density offered by MLPCM; the reliability of the MLPCM based LUT output deteriorates if fixed sensing thresholds are used, due to resistance drift as shown in Figure 4.35 in Chapter 4. In the following the reading reliability of MLPCM based LUT at both standard reading method with fixed sensing thresholds, and time-aware sensing is demonstrated.

For the presented half adder example the stored bits are in L2, L3 and L4 with 75%, 7.5%, and 0% crystalline fractions respectively taken from [100]. Indicating that three stages of failure will take place, according to simulation results in Figure 6.15, which used model parameters from [126].

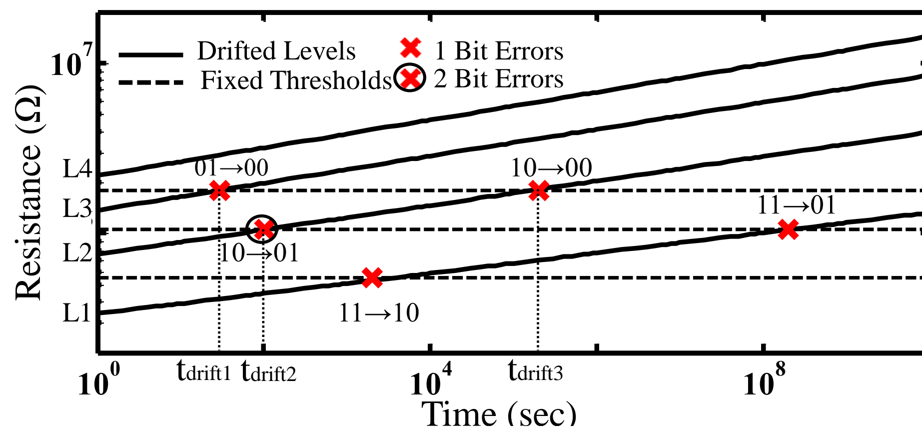

Figure 6.15: Single and multibit reading failure with fixed sensing thresholds

The stages of bit errors are specified in Table 6.3, given that the MLPCMs are programmed at t_0 and the stored Most Significant Bit (MSB) refers to the sum, while the Least Significant Bit (LSB) refers to the carry. The first stage at t_{drift1} effects M3; where a single bit error occurs when the resistance drifts from L3 to L4. In the second stage at t_{drift2}, two bit errors occur in both M1 and M2, where programmed resistance drifts from L2 to L3. Finally at the last stage of drift at t_{drift3}, M1 and M2 drift further to L4, correcting one of the bit errors at the second stage but leaving the cells with a remaining one bit error as indicated in Table 6.3.

Table 6.3: MLPCM based LUT drifted outputs

Inputs		t_0		tdrift1		tdrift2		tdrift3	
A	B	Sum	Carry	Sum	Carry	Sum	Carry	Sum	Carry
0	0	0	0	0	0	0	0	0	0
0	1	1	0	1	0	0	1	0	0
1	0	1	0	1	0	0	1	0	0
1	1	0	1	0	0	0	0	0	0

The time-aware sensing presented is Chapter 4 and depicted in Figure 4.34 can be used with this LUT to eliminate the effect of resistance drift. Where the MSB of the output B0 which represents the sum, and the LSB B1 representing the carry. Despite the fact that time-aware sensing implementation could lead to area and delay overhead; its significance is reduced since the LUT memory elements share the sense circuit.

6.4 PCM, Memristor and SRAM Performance comparison

In technical literature several comparisons are made to test the performance of resistive NVM in terms of area, energy, and delay in both simulation and experimental environment [18], [19], [128]–[130]. However, these performance comparisons are limited to either comparing emerging NVM technologies against each other and existing SRAM, DRAM and FLASH [128], [129]. Or only comparing one specific NVM technology to SRAM in specific purpose structure such as FPGA switch boxes[18], [19], [130]. The comparisons either did not use the same underlying crossbar architecture [128], [129]; or only compared each technology against SRAM [18], [19], [130]. Hence, not providing a fair comparison platform to estimate the advantages of these emerging memories over each other and the existing SRAM based memory crossbars. In this section a comparison between PCM,

Memristors and SRAM is conducted using the same underlying crossbar test structure.

6.4.1 Comparison test structure

The active crossbar architecture depicted in Figure 6.16 was the used test structure for both PCM and Memristor based memories. The memory elements M0–M3 are addressed using address lines A0 and A1. To perform programming and reading operations; the enable signals WE (write enable) and RE (read enable) are activated respectively. Moreover, the signals DATA and $\overline{\text{DATA}}$ indicate if the cell is to be programmed to logic 1 or 0 respectively.

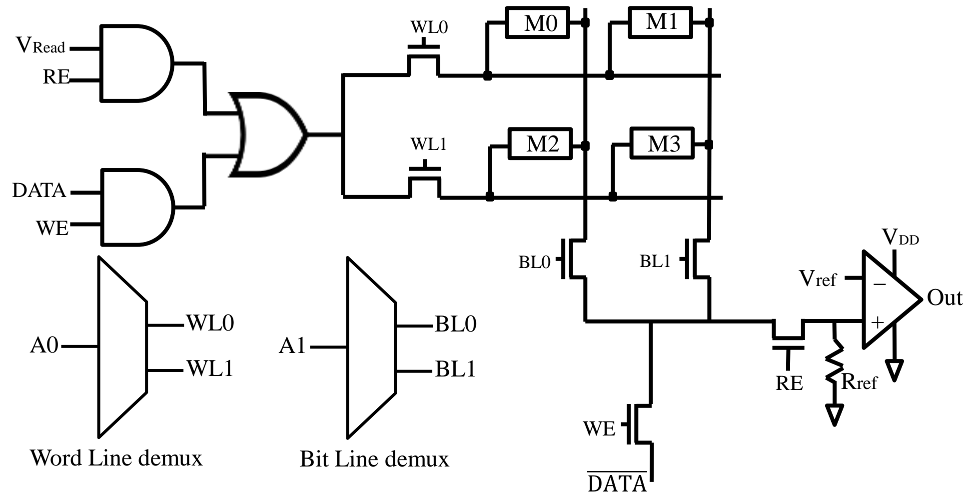

Figure 6.16: Schematic diagram of used crossbar architecture

6.4.1.1 Write operation

To access memory cells in the used active crossbar structure; pass-transistors are used as access devices. The Word line (WL) and Bit line (BL) pass-transistors connecting to the targeted cell are enabled by address lines using demultiplexers, as seen in Figure 6.16. The number of address lines depends on the size of the crossbar i.e. the number of memory elements.

To program i.e. write on a memory cell; write enable WE signal is activated. This allows current to flow between DATA and $\overline{\text{DATA}}$ through the selected memory cell.

However, PCM and Memristors are programmed by different voltage levels. Due to that difference, the programming "writing" circuit is slightly modified to accommodate the programming operation of each underlying technology as shown in Figure 6.17.

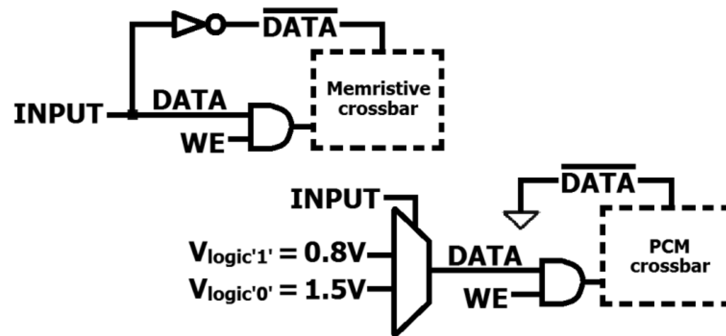

Figure 6.17: Write circuit of Memristor and PCM based crossbars.

To program a Memristor cell to logic 0 or 1; the applied programming voltage is maintained at 1V. However its direction through the Memristor is reversed. Thus, DATA and $\overline{\text{DATA}}$ are complementary of each other in the Memristive crossbar write circuit as seen in Figure 6.17. For example, if INPUT was 1V then DATA is 1V and $\overline{\text{DATA}}$ is 0V. Therefore, the selected Memristor will be programmed to logic '1' due to current flowing into the positive terminal of the Memristors in the crossbar.

On the other hand, to program PCM cells to logic 0 or 1; different levels of programming voltage are applied, while the current direction is maintained. Thus, in the write circuit of PCM crossbar, $\overline{\text{DATA}}$ is grounded (0V), while DATA is connected to a selector. The selector decides the appropriate programming voltage to be applied to DATA depending on the required logic i.e. INPUT. If logic '1' is to be written into the PCM, the selector applies 200ns pulse with 0.8V amplitude to DATA. Conversely, it applies 10ns pulse with 1.5V amplitude to DATA if logic '0' is to be written as shown in Figure 6.17.

6.4.1.2 Read operation

The read circuitry depicted in Figure 6.16 was used on Memristor, PCM, and SRAM based crossbars. In the read circuit an opamp is used as comparator. The read enable RE signal is charged to V_{DD}; to enable V_{READ} (0.5V) to pass through the memory cell and into the read circuitry, while V_{ref} is channelled into the inverting input of the amplifier as reference voltage. The parameters of the designed active crossbar test structure are listed in Appendix 6.3.

The opamp comparator swings to V_{DD} or GND to indicate the stored Bit in the memory element. If logic ‘1’ i.e. low resistance state was stored; the voltage at the non-inverting input of the amplifier will be higher than V_{ref}. This is due to the potential difference between the memory cell resistance and R_{ref}. The output of the opamp (OUT) will swing to V_{DD} indicating that the stored Bit is 1. Conversely, when the cell is at logic ‘0’ i.e. high resistance state; the non-inverting input of the amplifier will be at lower voltage than V_{ref}. Thus, OUT will swing to GND indicating a stored 0.

6.4.2 Simulation results and discussion

To evaluate the performance of PCM and Memristive crossbars; the PCM cell model presented in Chapter 4 was used as PCM element. While the Memristor model from [131] was used to represent the Memristive element. Moreover, when performing a read operation; the worst case scenario was tested. I.e. setting all untargeted memory cells to logic 1; allowing maximum leakage. To evaluate the average performance characteristics of each tested memory technology; all four memory cells (M0-M3) where programmed to levels 0 and 1 and read respectively, then the extracted values are averaged. The evaluated performance metrics include programming and reading delay, programming and reading energy, and leakage energy.

6.4.2.1 Programming delay

From the simulation results shown in Figure 6.18, it is noted that PCM based crossbars require longer programming durations compared to Memristor based ones. This is due to the operation mechanism of each memory. Memristor relay on carriers' movement; which requires less time compared to the thermally induced phase change mechanism of PCM. Moreover, Figure 6.18 shows the programmed resistive levels of PCM and Memristive crossbar. It clearly shows that PCM offers larger margin between high to low resistance states, i.e. almost 9 times of the margin offered by Memristors. This property makes PCM suitable for multibit storage.

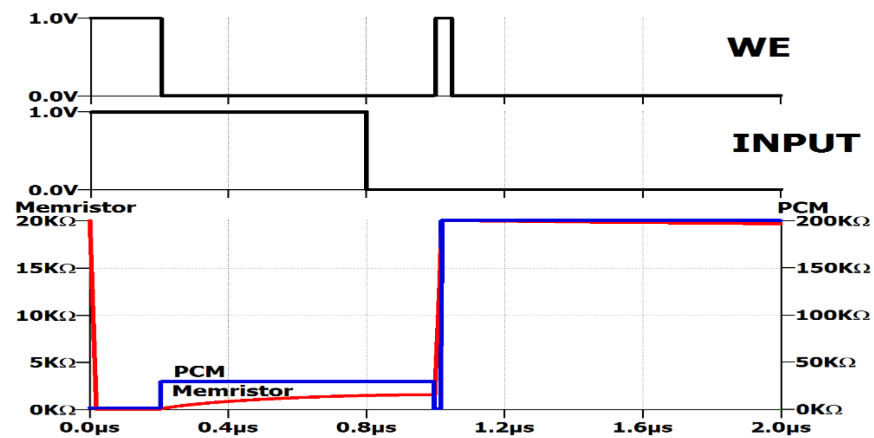

Figure 6.18: Programing delay and resistance levels of Memristor and PCM based crossbars

6.4.2.2 Reading delay

Figure 6.19 shows reading delay of both Memristor and PCM based crossbars. From the obtained simulation results shown in Figure 6.19 it is noticeable that PCM based crossbar requires longer reading delays for both stored 0 and 1 Bits. This a drawback resulting from the high resistivity accomplished by PCM cells. With such high resistances the reading current passing through the cell is much smaller than that passing through a Memristor cell. With smaller reading currents the opamp comparator in the reading circuit requires longer time to fully switch to indicate the stored Bit.

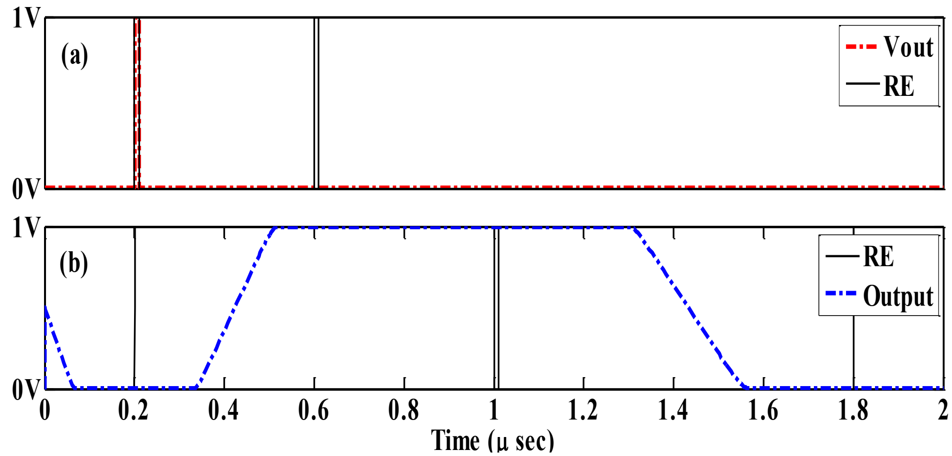

Figure 6.19: Simulation of Reading delay of (a) Memristive and (b) PCM based crossbars

6.4.2.3 *Energy consumption*

In order to evaluate the energy dissipated due to leakage in the crossbar; the energy consumption of all the unselected cells in the crossbar during reading and writing operations was measured. The obtained results are summarized in Figure 6.20. From these results it is noted that leakage energy of both PCM and Memristive crossbars showed more than 3 orders of magnitude improvement compared to SRAM crossbar. This is due to the fact that PCM and Memristor are resistive memories; and the presence of resistance in the leakage paths limits the flow of leakage currents. Furthermore, it is noted that PCM underwent higher leakage during programming compared to Memristors. This is due to PCM higher programming voltage.

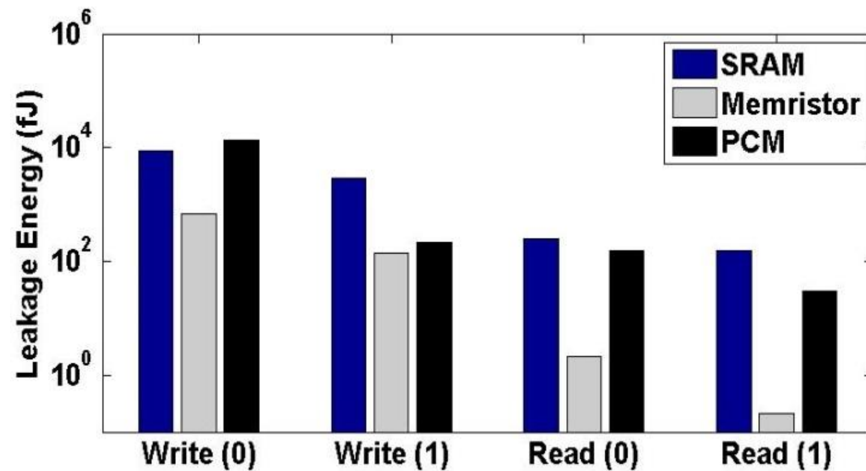

Figure 6.20: Leakage Energy in SRAM, Memristive, and PCM based crossbars

6.4.2.4 Comparison to SRAM

The performance of PCM and Memristor based crossbars was further compared to the current SRAM memory technology. The simulation results in Table 6.4 show that the programming delay for both Memristive and PCM crossbars was worse than that of SRAM crossbar by 2 and 3 orders of magnitude respectively. However, the read delay of the Memristive crossbar is about 3 orders of magnitude faster than the reading process of SRAM crossbar. The reason for the longer read delay is that the SRAM cells have high capacitive attributes. These capacitive attributes are a result of the large amount of transistors used to build an SRAM cell compared to NVM cells. Thus, it takes a longer time to charge or discharge output load in the SRAM crossbar.

Moreover, the programming energy of Memristive and PCM based crossbars were found to be 3 and 5 orders of magnitude higher than SRAM programming energy, and 2 and 3 orders of magnitudes for reading energy respectively. This is due to the higher resistance in the NVM cells of memristor and PCM. Since PCM has the highest resistance range compared to memristor and SRAM cells; the energy lost for read and write in PCM cells is the largest. The long programming and reading delays of PCM cells also contribute to the high amounts of energy lost.

In addition, NVM based crossbars offer higher density compared to SRAM technology; as an SRAM cell occupies an area of 6T i.e. the area of the 6 transistors consisting and SRAM cell. While the PCM and Memristors cell area takes up only is $4F^2$ in the crossbar as depicted in Figure 3.4 To put that comparison in perspective; an SRAM cell occupies a surface area of 0.4µm2 for a 65nm technology node [132], while a PCM based cell occupies only 0.26µm2. Therefore, NVM based crossbars prove to be superior to SRAM in term of area; as they require less area and offer higher density provided by multibit storage in a single cell. PCM has the evident advantage of PCM scaling capability, and it is established that in terms of scaling the

material volume no fundamental limitations of phase change properties are exhibited [11].

Table 6.4: PCM, Memristor and SRAM based memory crossbars comparison summary

Performance Metric	Memristor [131]	PCM	SRAM
Programming Delay (ns)	27.06	200	0.101
Read Delay (ns)	0.346821	636.826	391.926
Programming Energy (pJ)	1.752	126.73	0.00227
Read Energy (fJ)	23.1125	1369	0.7099
R_{ON} (Ω)	100	30 k	<10 k
R_{OFF}(Ω)	20 k	200 k	>10 M
Cell size	$4F^2$	$4F^2$	$6F^2$

6.5 Summary

In this chapter the application of SLPCM and MLPCM as memory elements in crossbar based memory application is studied. Then a performance comparison between SLPCM and MLPCM based memories was conducted. The comparison was in terms of writing delay, reading delay, writing energy, reading energy and area. From the comparison it is concluded that the reading delays and energy are closely tied to the reading circuitry used and the programmed level. With higher resistance levels requiring less programming/reading time and subsequently less energy.

Moreover, a half adder circuit configured with MLPCM based LUT was presented to demonstrate the capabilities of MLPCM paired with time-aware sensing. The pair of MLPCM and time-aware sensing can be further utilized to configure more complex functions with larger LUTs, as MLPCM will hold its advantage in terms of both reliability and density.

Additionally, a performance comparison was conducted between PCM and Memristor NVM based crossbars. The performance of the two NVM technologies was compared to the currently used SRAM technology. From the simulation results it

was concluded that the Memristor based crossbars showed superior performance compared to PCM based ones it terms of delay and leakage. However PCM crossbars offered higher resistance range, making it more efficient for applications in which operating speed is the limiting factor. While PCM crossbars are more efficient in applications that require denser memory storage; due to PCM cells having wider resistance range that allows multilevel switching and multibit storage.

The studied PCM material, and cell structure lags in terms of delay and energy consumption in comparison to Memristor and the current SRAM technology. However, it offers higher density due to both cell area and multilevel operation.

CHAPTER 7

CONCLUSION AND FUTURE WORK

7.1 Conclusion

The presented work studied the feasibility of using PCM based memory structure. To do so, an electrical circuit model of PCM cell was designed and tested. The designed cell behaviour was modelled to simulate both single and multibit storage. The simulation results were compared against experimental data obtained from an actual PCM element. This was in order to insure the reliability of performance tests based on the designed PCM cell. The developed circuit model successfully simulated the temperature profile, the crystalline fraction, and the resistance of the cell as a function of the programming pulse. Furthermore, the model generated I-V characteristics of PCM element that was in close agreement with experimental data.

In addition, drift behaviour in MLPCM was modelled, and simulated. The simulation results were verified by comparing them to experimental results for drift durations up to 10^3 seconds, as available in technical literature. It was deductive and clear from simulation results that the drift problem limits MLPCM operation and abolishes integrity of stored data. With failures occurring in less than 100 seconds after programming, and deviation between the programmed and drifted resistance reaching $6x10^6\Omega$ in less than 10^{10} seconds.

Therefore, an adaptive sensing threshold scheme that uses statistical data to predict the behaviour of MLPCM was presented. The obtained simulation results of the proposed drift sensitive reading circuit confirmed its reliability. The reading margins did not overlap as the case with standard sensing schemes that used fixed sensing thresholds. This solution successfully eliminated the drawback of drift, and sustained the desirable multibit storage capability of PCM based memory arrays.

Furthermore, the designed PCM circuit model was used to conduct performance tests and to study PCM based memory crossbars in simulation environment. Starting with the performance degradation of PCM based memories due to power loss across

wire segments. The simulation results showed that power consumed by connecting wires compromises the programmed resistive levels; specifically the low resistive state. It was noted that it was significantly higher with 40% deviation from the targeted levels. This jeopardized the integrity of stored data and led to 90% decrease in the high to low resistance ratio.

To overcome energy loss in connecting wires; the dissipated energy was compensated for by increasing the programming pulse duration. However, this solution imposed a trade-off in reliability, energy consumption, and delay; as programming energy consumption and delay increased by 40pJ and 60ns respectively. Therefore, a second solution was proposed; where the memory crossbar is segmented into smaller units that are less affected by energy loss across connecting wires.

In addition, the effects of leakage energy in PCM based nanocrossbars were studied. Simulation results of PCM based memory performance tests showed that the PCM element is resilient to leakage currents. Given that the programmed information was not compromised due to leakage. However, leakage currents did consume considerable energy across the memory system. A structural solution was proposed and successfully reduced the leakage by more than six orders of magnitude. Moreover, it led to an order of magnitude decrease in reading delay, and a significant improvement in programming delay that was proportional to the memory size.

Moreover, a second solution at reading circuit level was proposed and designed, in order to reduce leakage during reading process. Where an AC based reading circuit was used instead of standard DC reading method. This approach led to more than 50% reduction in leaked energy and reading energy as well.

Moreover, Memory and logic applications of PCM were explored using the designed PCM circuit models. SLPCM and MLPCM were used as memory elements in crossbar memory, and PCM based LUT was explored and tested in simulation

environment. Then, the performance of PCM based crossbars was compared to their SRAM and Memristors counterparts.

Simulation results showed that programming and reading energy consumption of PCM based crossbars were five orders of magnitude more than SRAM based crossbars. And reading delay of PCM based crossbars was two times longer than their SRAM based counterparts. However, the large resistance of PCM lead to two orders of magnitude reduction in leakage energy and higher density. Given that a PCM cell occupies two thirds of the area required by SRAM and can store multiple bit in a single cell.

Moreover, Memristor based nanocrossbars outperformed PCM based ones; in terms of delay and energy consumption. With PCM consuming 2 orders of magnitude more energy during programming and reading. PCM also required one order of magnitude longer programming delay. However, PCM crossbars offered higher switching resistance range i.e. 170kΩ compared to the 20kΩ offered by memristors; which support PCM multibit storage capability and higher density.

From all the above mentioned results, it is concluded that in order for PCM based memories to be a suitable replacement for the current SRAM technology; it must prove to be practical, and overcome few obstacles. As they still require more programming energy and longer delays compared to current technology. However, they do demonstrate desired density, non-volatility and reliability, and offer a promising future.

7.2 Future work

In this thesis, the performance of PCM element in memory crossbars is evaluated and compared to other memory technologies. The restrictions and drawback that face PCM elements in particular i.e. resistance drift and PCM based arrays in general i.e.

leakage and energy loss across connecting wires, are studied and addressed separately.

This work can be extended to evaluate the combined effects of crossbars resistive wires and resistance drift in PCM cells at array-level. And include the proposed performance optimization techniques i.e. time-aware sensing and architectural improvements; to test overall performance of PCM based memory system.

At the moment, the size of memory crossbars tested in simulation environment is restricted due to the convergence issue that arises with increasing crossbar sizes. Therefore, the use of a different software platform that allows testing larger memory crossbars to accurately evaluate the effect of crossbar sizes in PCM performance improvement is proposed to be future work.

In addition to designing a circuit model for a PCM cell, an emulator circuit can be a strong design tool. An emulator is an electrical circuit that would mimic the behaviour of PCM component. This circuit can then be used as a learning tool to design and develop applications of PCM without the cost of fabricating PCM device; due to the cost and technical difficulties in fabricating nanoscaled devices. In technical literature, there have been several emulator models for other NVM technologies such as Memristors [133]–[136], and NAND flash [137], but non for PCM. Therefore the design and implementation of a PCM cell emulator circuit, using commercially available discrete electronic components, is encouraged in future works to explore PCM possible applications.

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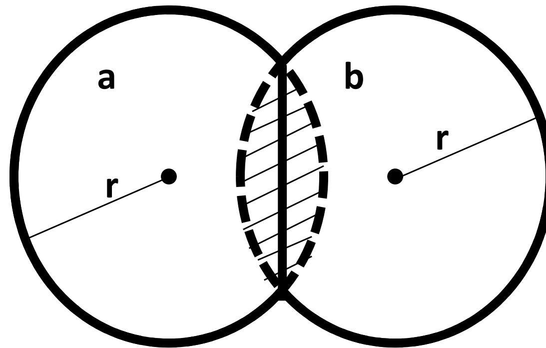
APPENDICES

APPENDIX 2-1

JMAK Equation Derivation



$f = \frac{V_a \cup V_b}{V_{total}}$

$f^{ext} = \frac{V_a + V_b}{V_{total}}$

$df = df^{ext}(1 - f)$

Given the volume V

$$V = \frac{4\pi}{3} r^3(t) = \frac{4\pi}{3}(vt)^3$$

Then multiplying the individual volume by the number density of nuclei, N we get:

$$f^{ext} = \sum V_i / V_{total} = \frac{4\pi}{3} N(vt)^3$$

Obtaining the extended fraction increment:

$$df^{ext} = V/V_{total} = 4\pi N(vt)^2 dt$$

Inserting the extended fraction increment into the differential equation:

$$df = df^{ext}(1 - f)$$

$$df = 4\pi N(vt)^2 dt(1 - f)$$

$$df/(1 - f) = 4\pi N(vt)^2 dt$$

Putting the nucleation and growth terms into a constant:

$$k = \frac{4\pi}{3} N v^2$$

Solving the differential equation gives:

$$\ln(1-f) = \frac{(4\pi N v^2)t^3}{3}$$

By rearranging and putting all constants into one term "k" we get JMAK equation:

$$f = 1 - \exp\{kt^n\}$$

Where

$f \equiv$ fraction transformed

$t \equiv$ time

$r \equiv$ radius

$V \equiv$ volume

$v \equiv$ growth rate (speed)

$N \equiv$ rate of nucleation, or, density of nuclei per unit volume

$n \equiv$ Avrami coefficient, in general, the exponent n in the equation is related to the geometry of the transformation.

Expending JMAK equation by the Taylor series expansion [49] and ignoring the second and higher order parts due to short programming pulses (<1µsec) we get;

$$f = Kt^n.$$

APPENDIX 4-1

Models parameters and constants used values [4], [49], [75], [122]

Module	Constant	Value
PCM cell	Crystalline resistance “$R_{crystalline}$”	7kΩ
	Amorphous resistance “$R_{amorphous}$”	200Ω
	Dynamic ON “R_{ON}”	1KΩ
	Set Programming Current I_{SET}	500µA
	Reset Programming Current I_{RESET}	1mA
	Programming time of Set	200ns
	Programming time of Reset	10ns
Switch control module	Holding voltage “V_x”Vmin	0.62V
	Threshold Voltage (Vth) Vmax	0.78 V
Temperature module	Radius of active region (r1)	50 nm
	Radius of PCM cell (r2)	100 nm
	Thermal capacity of GST (C)	1.25 $J.cm^{-3}K^{-1}$
	Thermal conductivity of GST (k)	1.5W/mK
	Glass Transition Point (Tx)	200˚C
	Melting Point (Tm)	600˚C
Crystalline module	Avrami const. “n”	2.2
	Activation energy “E_A”	2.3 eV
	Meyer-Neldel energy “E_{MN}”	66meV
	v_0	10^6 - 10^7
Drift module	R_0	1.28M
	V_{T0}	0.55
	Δv_t	0.46
	v_r	0.077
	v_t	0.074
Read circuit	V_{ref}	50mV
	R_{ref}	50kΩ

APPENDIX 5-1

Circuit Parameters of tested crossbar structures

Parameter	Value
R_{ref}	100kΩ in proposed structure 50 kΩ in standard structure
V_{ref}	50mV
V_{DD}	1V
V_{P0}	1.2V
V_{P1}	0.8V
V_{Read}	0.1V
DATA (High/Low)	1V/0V
A0	1V/0V
A1	1V/0V
$WE/\overline{RE}$	1V/0V
C	1V/0V

APPENDIX 5-2

AC sense circuit parameter values

Parameter	Value
PCM resistance range	7kΩ – 200kΩ
R1	1MΩ
C1	16F
C2	10fF
Frequency	100MHz
V_{read}	0.4V

APPENDIX 6-1

SLPCM Crossbar Based Memory Architecture performance simulation results

SLPCM	**1**			
	Write		Read	
	Delay (nsec)	Energy (pJoule)	Delay (nsec)	Energy (fJoule)
4x4	199	128.32	13.6581	16.289
8x8	199	129.5936	13.745	19.142
16x16	199	132.3592	16.09	29.201
32x32	199	137	14.654	36.4828

SLPCM	**0**			
	Write		Read	
	Delay (nsec)	Energy (pJoule)	Delay (nsec)	Energy (fJoule)
4x4	10	14.508	70.9145	14.183
8x8	10	14.652	71.0529	28.372
16x16	10	14.94	71.213	56.972
32x32	10	1.55E	71.9333	115

APPENDIX 6-2

MLPCM Crossbar Based Memory Architecture performance simulation results

MLPCM	11			
	Write		Read	
	Delay (nsec)	Energy (pJoule)	Delay (nsec)	Energy (fJoule)
4x4	199	223.06	225.785	868.25
8x8	199	351	225.847	6861.4
16x16	199	605.85304	224.903	23915.5

MLPCM	10			
	Write		Read	
	Delay (nsec)	Energy (pJoule)	Delay (nsec)	Energy (fJoule)
4x4	197	220.82	224.719	663.4
8x8	197	347.13554	224.489	1325.5
16x16	197	599.76662	223.428	2632.64

MLPCM	01			
	Write		Read	
	Delay (nsec)	Energy (pJoule)	Delay (nsec)	Energy (fJoule)
4x4	183	205.13	162.19	38.754
8x8	183	322.47052	161.411	77.33
16x16	183	557.15156	163.208	155.916

MLPCM	00			
	Write		Read	
	Delay (nsec)	Energy (pJoule)	Delay (nsec)	Energy (fJoule)
4x4	10	25.227	49.9872	4.2836
8x8	10	76.374	50.1205	8.587
16x16	10	68.537241	49.9916	17.1344

APPENDIX 6-3

Active crossbar test structure parameters

Parameter	Value
R_{ref}	50kΩ PCM based crossbar 10 kΩ Memristor based crossbar
V_{ref}	0.2V PCM based crossbar 0.25V Memristor based crossbar
V_{DD}	1V
V_{Read}	0.5V
DATA (High/Low)	1V/0V
A0 (High/Low)	1V/0V
A1 (High/Low)	1V/0V
WE (High/Low)	1V/0V
RE (High/Low)	1V/0V