

A New Class of Hybrid AC/AC Direct Power Converters

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Abstract- Variable voltage and variable frequency conversion of electrical energy from an AC source to an AC load is done in traditional power converters via a DC-link where an energy storage element (electrolytic capacitors) is situated. Despite its well-known benefits, it has the disadvantage of being bulky and to limit the converter lifetime. On the other hand, Direct Power Conversion (DPC) is an attractive concept, which doesn't need an energy storage buffer, but has two main disadvantages: reduced voltage transfer ratio (<0.86) and low immunity to voltage supply disturbances. This paper proposes a new approach to perform the power conversion by mixing various standard topologies of well-known power converters in order to improve their performance/behavior. Simulation and experimental results prove that the hybrid structures are able to boost the output voltage capability (some above unity) and/or to fully compensate unbalanced voltage supply.

Keywords- Direct AC/AC power conversion, hybrid converter, supply unbalance compensation, unitary voltage transfer ratio.

I. INTRODUCTION

Standard topologies of power converters have been investigated extensively for many years, which enabled the researchers to identify most of their advantages and disadvantages. Each topology consists of basic building blocks (DC/AC conversion stages), which may use a voltage DC-source or a current DC-source in the DC-link. Considering the characteristics of the semiconductor switches, we may say that voltage source type inverters benefit the most due to a reduced number of power devices and low conduction losses while Current Source Inverters (CSIs) would need switches with reverse blocking behaviour, currently implemented as a series connection of an IGBT and a diode. In depth semiconductor loss investigation showed that CSIs, offer smaller switching losses and that the conduction losses may be reduced by using the newly developed reverse blocking IGBTs.

The AC/DC/AC power conversion topologies that offer sinusoidal input current and bidirectional power flow are a result of a back-to-back connection of two identical inverters which in order to work properly, need an input filter consisting of a boost inductance (Fig. 1a) or an LC input filter (Fig. 1b). Both types of power converters rely heavily on the presence of reactive components on the DC-link in order to emulate the constant voltage/current source. So far, the voltage source converters seem to benefit from the fact that unipolar DC-link voltage allows the utilization of electrolytic capacitors, which

offer a very good energy storage density compared to magnetic storage, but their reliability is currently a major factor in limiting the life-time of any power electronic equipment.

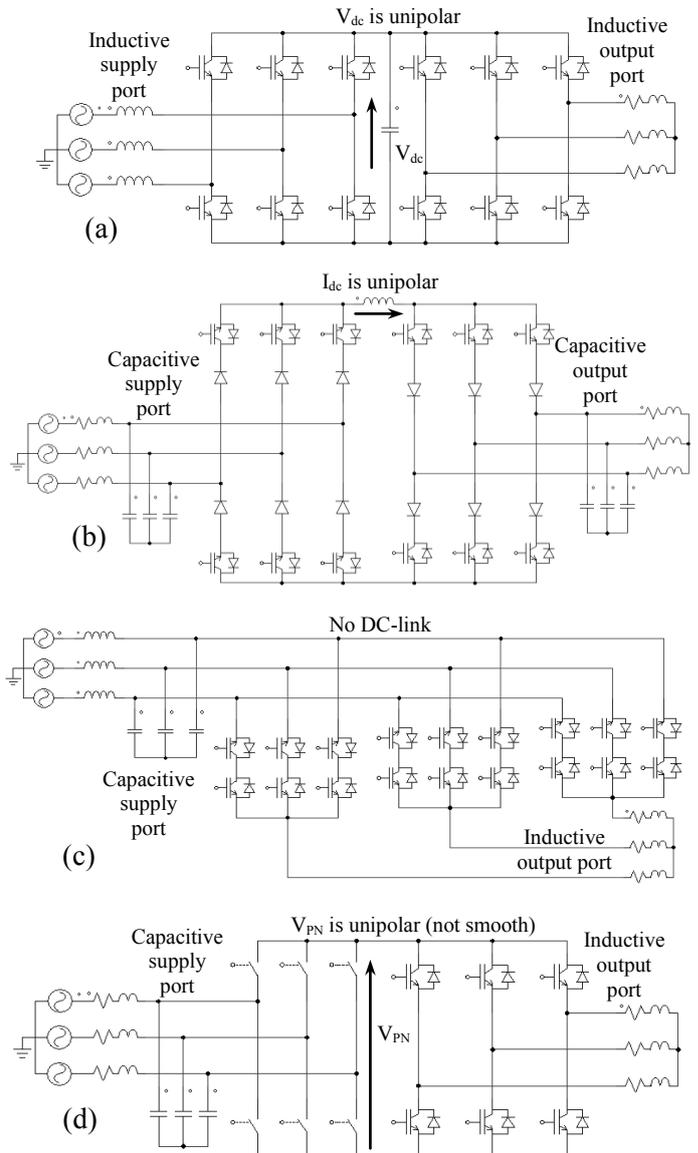


Fig. 1. Different classes of AC/AC power converters: a) AC/DC/AC Voltage Source Converter; d) AC/DC/AC Current Source Converter; e) AC/AC Single Stage Matrix Converter; f) AC/AC Two Stage Indirect Matrix Converter.

These disadvantages can be avoided in a class of power converters that have no energy storage, the so-called Direct Power Converters (DPCs): the single stage matrix converter shown in Fig. 1c [1]-[5] or its two-stage companion [6]-[11] shown in Fig. 1d, which in some particular applications requires less power devices [11].

Besides the high amount of semiconductor devices needed to build a DPC, it has two main disadvantages: the voltage transfer ratio is limited to 0.86 which means that it cannot compete directly with the back-to-back voltage source converter and also cannot be used to replace a standard converter equipped with a diode rectifier (retrofit applications) and it has low immunity to power-grid disturbances, which causes a further decrease of the output voltage capability [5].

In this paper, few novel hybrid DPC topologies [13], [14] that successfully solve the two most important drawbacks of the two-stage DPC are proposed. They consist in connecting an auxiliary voltage supply in the intermediary link of the two-stage DPC, with the purpose of compensating the deficit of voltage, which is characteristic to the two-stage DPC both in normal and unbalanced supply conditions. In §.II the standard modulation for a DPC is presented, while in §.III the concept of hybrid DPC is introduced and the different solutions are classified depending on how they are connected into the dc-link and if they have auxiliary means of supplying the necessary energy or based on energy storage. Finally, simulation and experimental results of two hybrid topologies are presented, confirming the superiority of the hybrid over standard DPC concept

II. SPACE VECTOR MODULATION FOR A TWO-STAGE DPC

Before presenting how the proposed hybrid topology works, it is necessary to present how the standard indirect matrix converter, also referred in the literature as “dual-bridge MC” [10] or “two-stage direct power converter” [12]-[13], works.

In [10], it has been shown that the implementation of Space Vector Modulation (SVM) for a two-stage DPC is identical to the case of a matrix converter controlled by an indirect SVM [2]-[4], therefore only the final equations are presented here. SVM produces a combination of two adjacent active vectors and a zero-vector to synthesize a reference vector of variable amplitude and angle. The proportion between the duty-cycles of the two adjacent vectors gives the direction and the duty-cycle of the zero-vector determines the magnitude of the reference vector. The input current vector I_{in} (only its angle) is

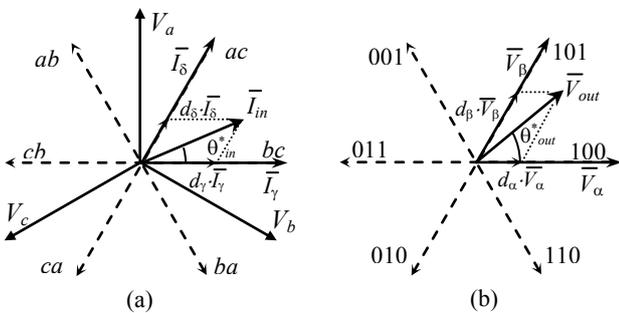


Fig. 2. Generation of the reference vectors in a two-stage Direct Power Converter using SVM: (a) rectification stage; (b) inversion stage.

the reference of the rectification stage (Fig. 2a) and the output voltage vector V_{out} is the reference of the inversion stage (Fig. 2b). The duty-cycles of the active switching vectors for the rectification stage, I_γ, I_δ are given by (1) and the duty-cycles of active switching vectors for the inversion stage, V_α, V_β are given by (2).

$$d_\gamma = m_I \cdot \sin(\pi/3 - \theta_{in}^*) \quad d_\delta = m_I \cdot \sin \theta_{in}^* \quad (1)$$

$$d_\alpha = m_U \cdot \sin(\pi/3 - \theta_{out}^*) \quad d_\beta = m_U \cdot \sin \theta_{out}^* \quad (2)$$

where $m_I = 1$ and m_U are the rectification and inversion stage modulation indexes, θ_{in}^* and θ_{out}^* are the angles within their respective sectors of the input current and output voltage reference vectors.

In the rectification stage, the zero-vector is eliminated due to redundancy with inversion stage and the switching sequence consists only of the two adjacent current vectors (line-to-line voltages). The zero-vector is applied by the inversion stage according to its need. By using (1), the adjusted rectification stage duty-cycles are found (3), where the modulation index of the rectification stage $m_I = 1$.

$$d_\gamma^R = \frac{d_\gamma}{d_\gamma + d_\delta} \quad d_\delta^R = \frac{d_\delta}{d_\gamma + d_\delta} \quad (3)$$

These duty-cycles multiply with the switching period and the resulting ON-times directly drive the rectification stage switches. Since the average voltage in the DC-link is not constant anymore due to the cancellation of the zero-vector in the rectification stage, it is necessary to calculate its value to compensate the modulation index of the inversion stage:

$$V_{PN-avg} = d_\gamma^R \cdot V_{line-\gamma} + d_\delta^R \cdot V_{line-\delta} \quad (4)$$

It can be seen that in the case $\theta_{in}^* = \pi/6$, $d_\gamma = d_\delta = 0.5$ and because the two line-to-line voltages are equal to their peak value multiplied to $\cos(\pi/6)$, it makes the average voltage over a switching period delivered by the rectifier stage to reach a minimum of 0.86 of the peak line-to-line voltage.

The inverter stage may use a double-sided asymmetric PWM switching sequence $0_\gamma - \alpha_\gamma - \beta_{\gamma+\delta} - \alpha_\delta - 0_\delta$, but with unequal sides because each side corresponds to a rectification switching sequence which uses a different DC-link voltage. Therefore, the value of the modulation index m_U used in (2) has to be corrected with the momentary average DC-link voltage V_{PN-avg} (4), which takes into account this variation (5). The inversion stage duty-cycles are given in (6).

$$m_U = \sqrt{2} \cdot V_{out} / V_{PN-avg} \quad (5)$$

$$d_1 = \frac{d_\gamma \cdot [1 - (d_\gamma + d_\delta) \cdot (d_\alpha + d_\beta)]}{d_\gamma + d_\delta} \quad d_2 = d_\gamma \cdot d_\alpha \quad (6)$$

$$d_3 = (d_\gamma + d_\delta) \cdot d_\beta \quad d_4 = d_\delta \cdot d_\alpha$$

By applying the previously presented control algorithm, sine-wave in sine-wave out operation is achieved as demonstrated in Fig. 3, where the input phase voltages (top) and current (second) and the output phase voltage (third) and load currents (bottom) are shown.

Fig. 4 shows the variation of the dc-link voltage delivered by the rectifier stage and its average over a switching period when

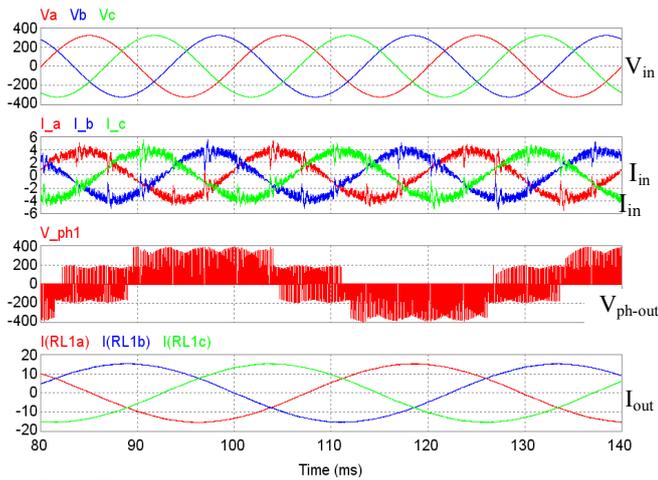


Fig. 3. Typical input and output voltage and current waveforms for a Direct Power Converter.

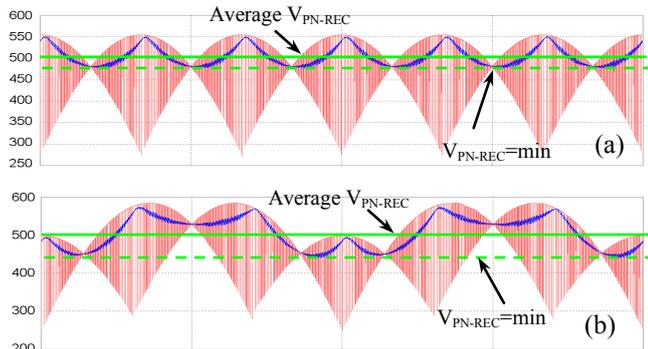


Fig. 4. The instantaneous dc-link voltage delivered by the rectifier stage and its average value for a two-stage DPC when the supply is a) balanced and b) 10 % unbalanced voltage supply, showing where the peak output voltage is limited at: a) 480 V and b) 450 V.

the supply voltage is sinusoidal and balanced (Fig. 4a) or has 10 % unbalance (Fig. 4b). The minimum average dc-link voltage is marked with dotted line while its mean value over a period of the input voltage fundamental (20 ms) is marked with continuous line. Two things are obvious: first, that the maximum voltage transfer ratio is limited when the average dc-link voltage reaches its minimum, and that this is further decreased when the input voltage supply becomes unbalanced. This led to the following idea: because there is a certain difference between the minimum and the mean level, one way of compensating the unbalance effect, and to increase the voltage transfer ratio as well, is to insert an AC source in the dc-link between the rectifier and the inverter stages and to inject a voltage that will cancel the normal variation of the

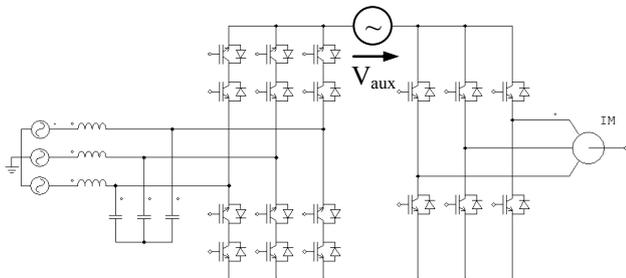


Fig. 5. Two-stage Matrix Converter with auxiliary voltage supply connected in the intermediary link.

average dc-link voltage, stabilizing its level at the mean value, as shown in Fig. 5. This solution enables also to reach unitary (or higher) voltage transfer ratio, by actually injecting an always-positive auxiliary voltage to compensate the required difference.

III. PROPOSED HYBRID TOPOLOGIES OF DPCs

In order to overcome the main drawbacks of DPCs, a few solution based on a hybrid approach are proposed below, all having in common the insertion of a controllable voltage source in the intermediary circuit [14],[15], which can be classified into two categories, consisting of using:

- an independent high-voltage DC source available in the DC-link as shown in Fig. 6a, which can be used as a third supply besides the two highest in magnitude rectified line-to-line voltages, which due to the fact that is higher in magnitude than any of the line-to-line voltages, will increase the average of the DC-link voltage seen by the inversion stage and therefore the voltage transfer ratio:

$$V_{PN-INV} = (1-d_c) \cdot V_{PN-REC} + d_c \cdot V_C = \sqrt{2} \cdot V_{out} \quad (7)$$

- a low-voltage DC source that may be introduced in series with the voltage delivered by the rectifier stage, whenever needed as shown in Fig. 6b, inherently boosting the average DC-link voltage seen by the inversion stage and therefore the voltage transfer ratio:

$$V_{PN-INV} = V_{PN-REC} + d_c \cdot V_C = \sqrt{2} \cdot V_{out} \quad (8)$$

Higher voltage transfer ratios, previously limited at 0.866 are possible (even higher than unity!), provided that the level of V_C is sufficient. Finding the optimum level for the auxiliary voltage supply is a tradeoff: if chosen low, it will not require higher blocking voltage capability for the semiconductors, but the power processed by the auxiliary supply is higher, as shown in Fig. 7. If chosen high, the processed power decreases, but due to higher blocking voltage capability needed in the switches, the installed power cannot decrease.

The second classification of these hybrid DPCs topologies is made depending on how the auxiliary voltage source is controlled. Normally, a capacitor is a basic circuit component

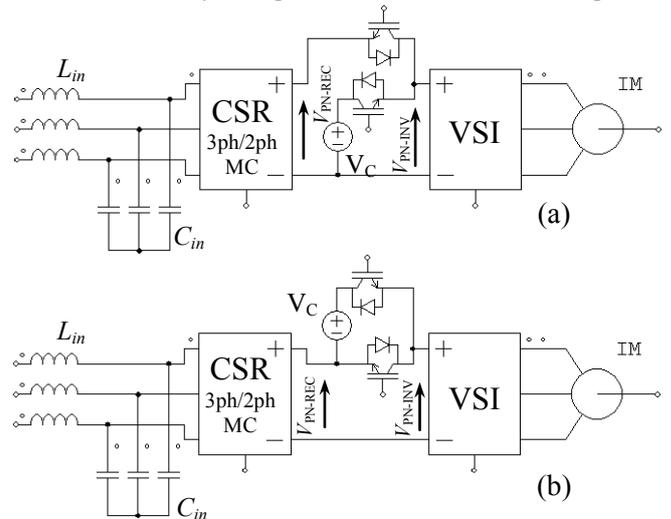


Fig. 6. Categories of hybrid DPC topologies employing: a) an auxiliary high-voltage DC source; b) low-voltage DC source.

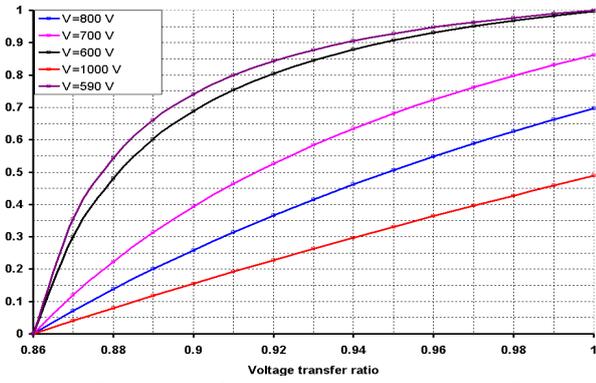


Fig. 7. Dependence of the peak power as a percentage of power delivered to the load versus the desired voltage transfer ratio and variable auxiliary supply voltage. ($V_{in} = 415V_{rms}$)

that has a voltage source behavior. One alternative is to supply its energy requirement by an auxiliary converter (boost/buck/fly-back etc) fed from an independent source. Then, as only a certain auxiliary converter topology will match the best each of the hybrid arrangement shown in Fig. 6, two topologies of hybrid power converters emerge utilizing:

- a reversible boost converter for the topology in Fig. 6a
- a reversible flyback converter for the topology in Fig.6b

There are many ways of connecting the auxiliary reversible converters to the same power grid, one may be to supply the boost converter from the input filter capacitors, but if using diodes, the power flow will be restricted. The simpler and most efficient way found, was to actually connect the boost converter at the dc-side of the rectifier stage, as both the boost and the flyback converters act as current sources on the supply port. The resulting hybrid DPC topologies that correspond to Fig. 6a and b are shown in Fig. 8a and b. Another possibility is not to have an auxiliary converter to supply unrestrictedly the energy needed by the auxiliary voltage source, but to use the fact that the average DC-link voltage delivered by the rectifier stage is not smooth, but varies between 0.866 and 1.00 the peak input-line-to-line voltage six times a cycle, or in case of voltage supply unbalance, within wider range. The resulting topology is presented in Fig. 8c, which uses an H-bridge inverter to allow a bipolar insertion of the capacitor.

It is clear that all three topologies actively use the capacitor that gives the voltage source behavior of the auxiliary voltage source, which may also store energy, arising the question if these topologies are still behaving as DPCs. The answer can be found in the way each of them is controlled. First of all, it is desired that the input currents to remain sinusoidal and one of the conditions for achieving that is to maintain accurate balance of input/output power over a switching period of the main converter:

$$P_{INV \rightarrow OUT} = P_{REC \rightarrow INV} + P_{C \rightarrow INV} = V_{INV_avg} \cdot I_{INV_avg} = const \quad (9)$$

$$P_{REC} = P_{REC \rightarrow INV} + P_{REC \rightarrow C} = V_{INV_avg} \cdot I_{INV_avg} = const \quad (10)$$

$$P_{REC \rightarrow INV} = V_{REC_avg} \cdot I_{INV_avg} \quad (11)$$

This means that for the first two topologies, the power flow into the capacitor, which is controlled by the boost/flyback converter, has to be maintained equal to the power delivered

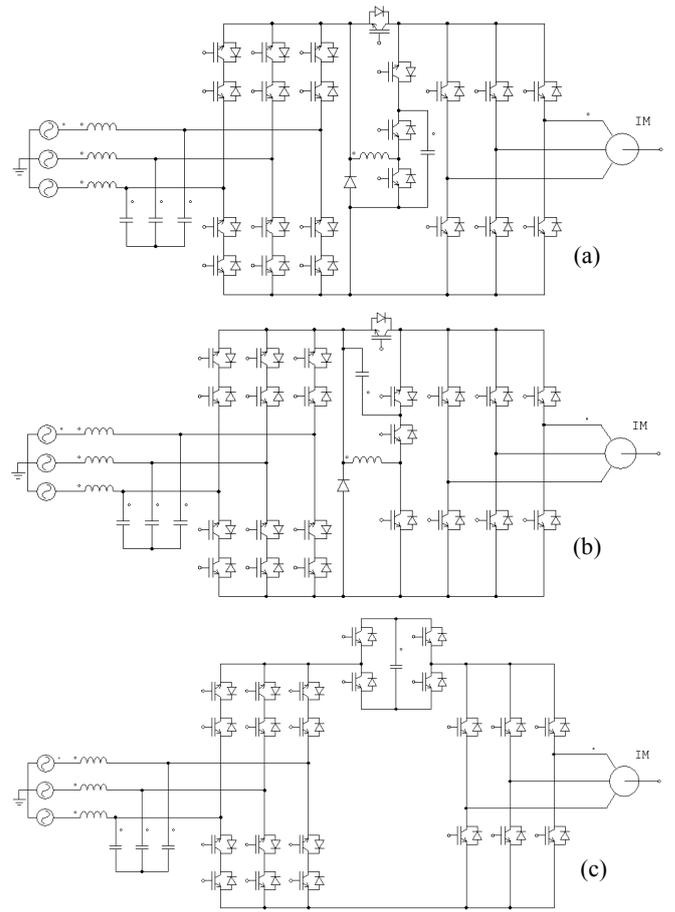


Fig. 8. ASD based on hybrid structures of two-stage DPC: a) with high-voltage auxiliary voltage source and reversible boost converter; b) with low-voltage auxiliary voltage source and reversible flyback converter; c) with capacitive storage inside an H-bridge inverter.

from the auxiliary voltage source to the inversion stage, operating as quasi direct power converters:

$$P_{C \rightarrow INV} = P_{REC \rightarrow C} \Rightarrow d_c \cdot V_C \cdot I_{INV_avg} = V_{REC_avg} \cdot I_{ref_inC} \quad (12)$$

which is accomplished if the current reference through the inductor follows (13) for the boost converter and (14) for the flyback converter, both being actually a product of the output power (dc-link inverter current) and a custom shape:

$$I_{ref_inC} = \frac{d_c \cdot V_C}{V_{PN-REC}} \cdot I_{INV_avg} = \frac{\sqrt{2} \cdot V_{out} / V_{REC_avg} - 1}{1 - V_{PN-REC} / V_C} \cdot I_{INV_avg} \quad (13)$$

$$I_{ref_inC} = \frac{d_c \cdot V_C}{V_{PN-REC}} \cdot I_{INV_avg} = \left(\frac{\sqrt{2} \cdot V_{out} - 1}{V_{PN-REC}} \right) \cdot I_{INV_avg} \quad (14)$$

This makes both topologies behave as quasi DPCs. Another converter in the same class is the back-to-back PWM Voltage Source Converter (VSC) with reduced dc-link capacitor, but as the two auxiliary converters process only a small fraction of the power delivered to the load (typically peak power below 30% for the boost and 13% for the flyback), it means that the typical energy storage, compared with a back-to-back VSC which processes its entire power delivered to the load via the dc-link, is insignificant, maintaining the DPC characteristic of the two hybrid configurations.

the output of this PI controller will give the peak value which needs to be multiplied by the custom shape in order to provide accurate input-output power balance (12). As the inductor current reference is not smooth, a fast PI controller for the current would probably not be able to force the actual inductor current to follow the reference accurately, and this is why a bang/bang with high sampling frequency or a hysteresis controller was employed.

The control system that ensures the proper operation of the H-bridge inverter within the hybrid converter is shown in Fig. 12. The capacitor voltage is monitored by a PI controller in respect to its reference value and its output generates an offset which is added to the target average voltage seen by the inverter stage. This allows the hybrid converter to adapt to supply voltage changes. The average voltage delivered by the rectifier is calculated each switching period and subtracted from the target, which produces the reference voltage to be generated by the H-bridge inverter. By dividing this value to the actual capacitor voltage, the duty-cycle of the nonzero voltage state of the H-bridge inverter is found, while its sign gives the combination of transistors that needs to be gated.

V. SIMULATION RESULTS

In order to evaluate how the proposed hybrid DPCs perform and to which extent they fulfill the expectation, two simulation models have been implemented in Saber and also one prototype has been built.

First simulation results that are presented correspond to the hybrid DPC shown in Fig. 8a, which operates with unitary voltage transfer ratio. This topology has been chosen as it has a smaller capacitor size, which anyway is used in the same place for protection purpose (clamp circuit), which means that the only passive component actually needed is the boost inductor. The parameters of the simulation model are presented in Appendix A. The DC-link voltage seen by the inversion stage is shown in Fig. 13a, which denotes the fact that two rectified line-to-line input voltages are mixed with a constant voltage of higher magnitude (800 V), which increases its average value and therefore the voltage transfer ratio. The load currents are illustrated in Fig. 13b, being sinusoidal and balanced which normally happens when the power delivered to the load is constant. Fig. 13c shows the filtered line-to-line output voltages, done by employing an RC low-pass filter to remove the PWM ripple and to reveal their peak value, which is needed to estimate the voltage transfer ratio. The RMS value of the line voltage is 412.8 V, close to the 415 V supply voltage. The three input currents are presented in Fig. 13d, revealing sinusoidal and balanced shapes which is the result of proper distribution of the load power in the input lines. The quality of the input currents is further investigated by showing the FFT of the input currents (Fig. 13 e-g), which shows a low content in low order harmonics ($< 2\%$) and a calculated THD of 5.2-5.5%. One aspect which is important when determining the installed power in semiconductors and the effect of choosing the level of the high-voltage auxiliary supply is illustrated in Fig. 14, where the average DC-link current drawn by the inversion stage (Fig. 14a and d) which is constant, the

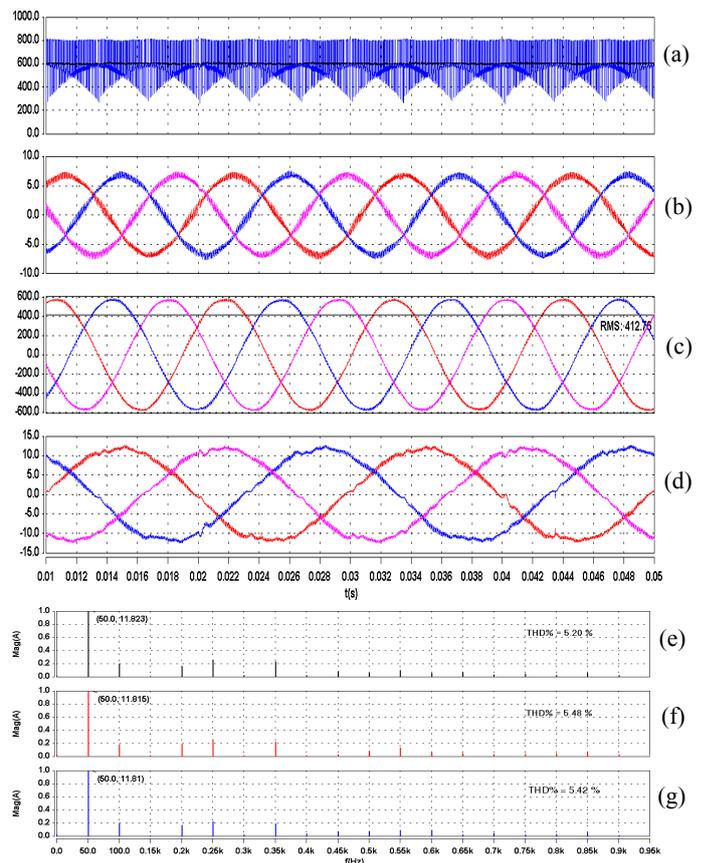


Fig. 13. Simulation of the hybrid DPC with high voltage auxiliary supply operating with unitary voltage transfer ratio: a) the DC-link voltage seen by the inversion stage; b) the load currents; c) the filtered line-to-line output voltages; d) the input currents; e)-g) the FFT of the three input currents.

current directly delivered to the inverter stage by the rectifier (Fig. 14b and e) and the one delivered by the auxiliary supply to the inverter stage (Fig. 14c and f) which is very similar to the reference current in the boost inductance. These waveforms are shown in two situations, when the auxiliary voltage is 700

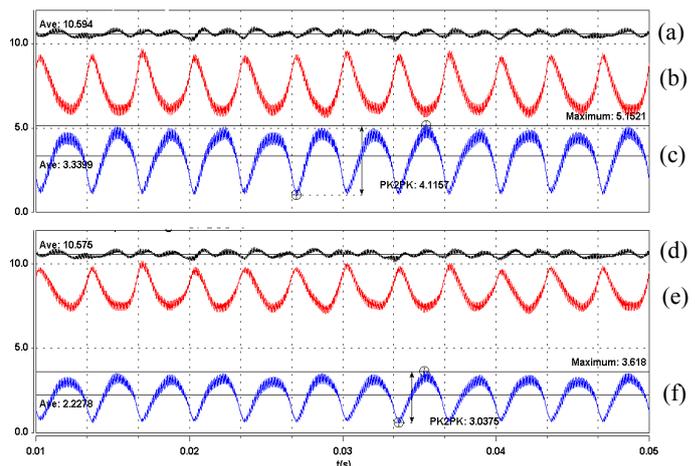


Fig. 14. Simulation of the hybrid DPC with high voltage auxiliary supply operating with unitary voltage transfer ratio in two situations: a)-c) $V_c = 700V$; d)-f) $V_c = 800V$. Waveforms: a), d) the average DC-link current drawn by the inversion stage; b), e) the average DC-link current delivered from the rectifier stage directly to the inversion stage; c), f) the average DC-link current delivered from the rectifier stage to the auxiliary supply.

V requiring a peak power processed by the auxiliary voltage supply of 3.6 kW and an mean value of 1.8 kW, and when the auxiliary voltage supply is increased to 800 V, which decreases the peak power through the auxiliary voltage supply to 2.9 kW and a mean value of 1.8 kW, while the voltage transfer ratio was maintained unity and the output power was 6 kW. This confirms the estimations from Fig. 7, where for 800 V, the ratio between the peak power through the auxiliary voltage supply and the output power was 0.5, compared to 0.48 here.

In order to prove the capability of the topology presented in Fig. 8c to compensate a 10 % input voltage unbalance, another simulation model has been implemented in Saber and the results are shown in Fig. 15. The parameters of the model are mentioned in Appendix B.

Fig. 15a shows the waveforms of the input currents, which are slightly distorted (flat top) but well balanced. By utilizing the H-bridge inverter it is possible to deliver sinusoidal and balanced output voltage near the maximum voltage transfer ratio. This can be seen in the shape of the load currents (Fig. 15b) and in the shape of the filtered output voltage (Fig. 15c). A low-pass RC filter with high cut-off frequency was used to extract the fundamental from the PWM output voltage in order to clearly show that the voltages are not only sinusoidal and balanced, but they are not decreased due to the fact that momentarily, due to unbalance, the input voltages cannot allow 0.86 voltage transfer ratio. Fig. 15d shows that both

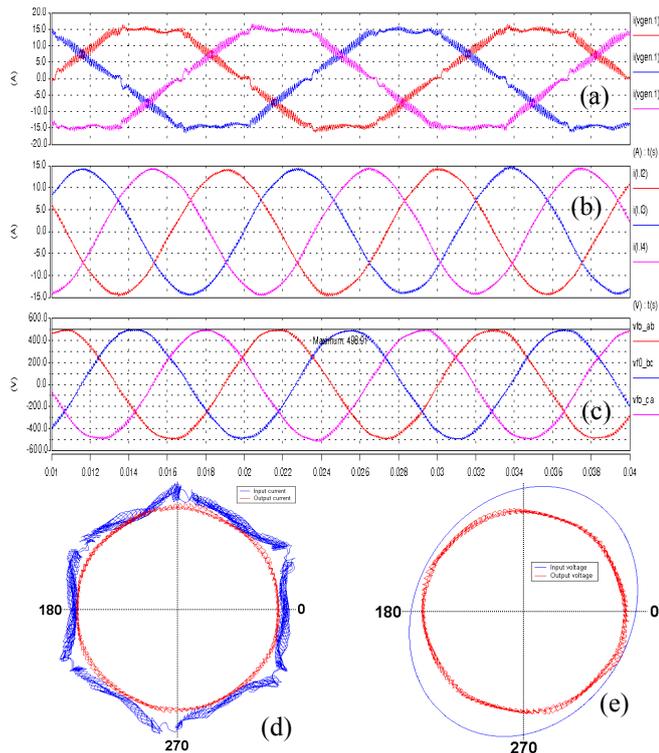


Fig. 15. Operation near maximum voltage transfer ratio (0.86) of the hybrid DPC under 10 % voltage unbalance: a) the input currents; b) the load currents; c) the filtered (RC low pass) output line-to-line voltages which proves that the waveforms are sinusoidal and balanced ($V_{line-pk} = 499V$); d) the locus of the input and output currents; e) the locus of the input (ellipse) and filtered output voltages.

input and output currents are balanced, even though only the output current is sinusoidal. Balanced input currents in the circumstances of unbalanced supply voltage are obtained by circulating most of the power ripple drawn from the input side with the H-bridge capacitor. The input and output voltage locus are shown in Fig. 15e. It is clear that the input voltage is unbalanced. The hybrid converter operates near 0.86 voltage transfer ratio, which is denoted by the fact that the two waveforms are almost tangent.

VI. EXPERIMENTAL RESULTS

The hybrid DPC topology using a high-voltage auxiliary supply has been practically implemented and preliminary experimental results carried out with reduced input voltage and higher than unity voltage transfer ratio are presented in Fig. 16. The parameters of the circuit are presented in Appendix C.

Fig. 16a shows the three line-to-line filtered (using three RC-star connected low pass filters) output voltages which denote clearly a peak value of 200 V, while the input line-to-line voltage (Fig. 16b) is only 150 V peak which results in a voltage transfer ratio of 1.33. This is possible because the reference of the auxiliary supply voltage is set at 400 V and

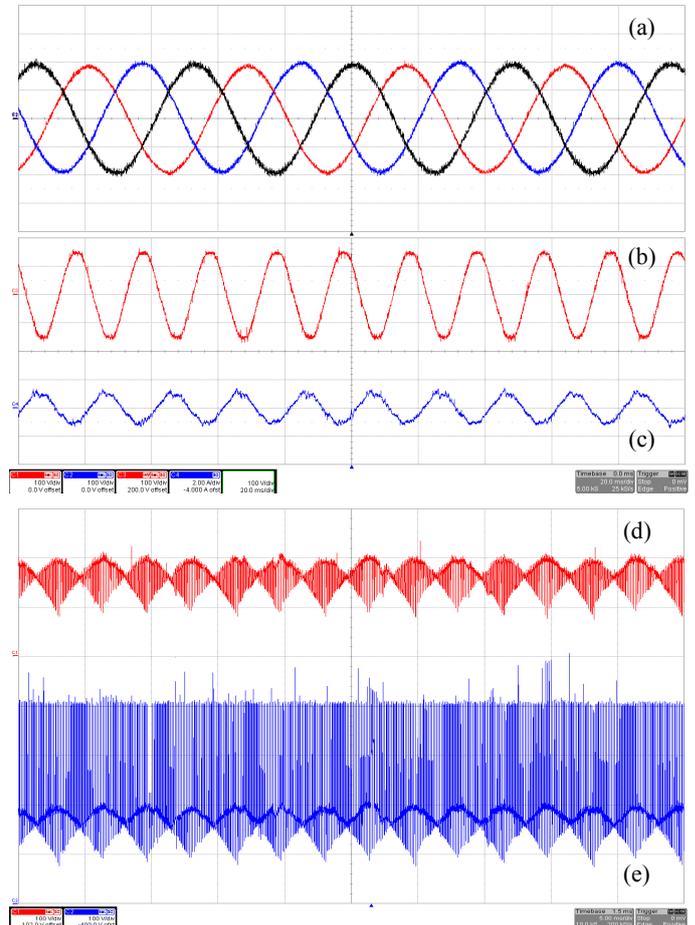


Fig. 16. Experimental results of the hybrid DPC with high voltage auxiliary supply operating with higher than unitary (133%) voltage transfer ratio: a) the three line-to-line output voltages filtered by small RC-filter (100 V/div); b) line-to-line input voltage (100 V/div); c) input current (2 A/div); d) rectifier and e) inverter side DC-link voltage.

this can be seen by comparing the waveforms of the DC-link voltage seen at the rectifier side (Fig. 16d) and inverter side (Fig. 16e) where the additional presence of the high-voltage auxiliary supply is present. The input current (Fig. 16c) is more distorted than expected mainly because the hysteresis controller for the boost inductance current cannot accurately follow the reference at reduced input voltage/output power.

VII. CONCLUSION

In this paper, a new approach on solving the two most significant disadvantages of Direct Power Converters (DPCs), the lower than unity voltage transfer ratio and the high sensitivity to unbalanced voltage supply, is proposed by using hybrid structures. Three hybrid DPC topologies are proposed: one based on a high-voltage auxiliary voltage source available in the DC-link controlled by a boost converter; the second one is based on a low-voltage auxiliary voltage supply available for insertion in the DC-link between the rectifier and inverter stages and controlled by a flyback converter and the third one is based on an H-bridge inverter and resembling the second topology, with the only difference that it does not need a charger to control the voltage, but it stabilizes the 300 Hz voltage ripple normally present in the average DC-link voltage delivered by the rectifier. First two hybrid DPCs provide unity voltage transfer ratio (or higher) and have very small energy storage component (small capacitors) as the auxiliary voltage chargers are controlled such that it would balance at any time the energy delivered from the auxiliary DC-source to the inverter stage. This indirectly maintains near sinusoidal input currents. The third topology needs energy storage capability, which is useful during unbalanced supply, but requires large size of the capacitor, which is rated at reduced voltage though.

Simulation results of the first and the third topologies and experimental results of the first topology at reduced voltage prove that they deliver the expected benefits, which enable now these converter topologies to compete with more success the more classical topologies for standard motor drives applications (including retrofit).

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APPENDIX A

The parameters in the simulation model for the results shown in Fig 13-14 are: $V_{\text{line-in}} = 415 \text{ V}_{\text{rms}}$, $L_{\text{in}} = 1 \text{ mH}$, $C_{\text{in}} = 4.5 \text{ }\mu\text{F/phase}$, $V_{\text{out}}/V_{\text{in}} = 1.0$; $f_{\text{out}} = 90 \text{ Hz}$, $f_{\text{sw}} = 10 \text{ kHz}$; $C = 10 \text{ }\mu\text{F/800 V}$, $L_{\text{aux}} = 1 \text{ mH}$, $f_{\text{s-aux}} = 100 \text{ kHz}$ and the load consist of $R_{\text{load}} = 50 \text{ }\Omega$, $L_{\text{load}} = 5 \text{ mH}$ star connected.

APPENDIX B

The parameters in the simulation model for the results shown in Fig 15 are: $V_{\text{line-in}} = 400 \text{ V}_{\text{rms}}$, $L_{\text{in}} = 2 \text{ mH}$, $C_{\text{in}} = 4.5 \text{ }\mu\text{F/phase}$, $V_{\text{out}}/V_{\text{in}} = 0.9$; $f_{\text{out}} = 90 \text{ Hz}$; $f_{\text{sw}} = 10 \text{ kHz}$; $C = 6,800 \text{ }\mu\text{F/100 V}$ and the load consist of $R_{\text{load}} = 20 \text{ }\Omega$, $L_{\text{load}} = 10 \text{ mH}$ star connected.

APPENDIX C

The parameters for the experimental results presented in Fig. 16 are: $V_{\text{in-ph}} = 61.5 \text{ V}_{\text{rms}}$; $V_{\text{out-ph}} = 82 \text{ V}_{\text{rms}}$; $f_{\text{out}} = 21 \text{ Hz}$; $V_{\text{c}} = 400 \text{ V}$; $L_{\text{in}} = 1 \text{ mH}$; $C_{\text{in}} = 9.2 \text{ }\mu\text{F/phase}$; $L_{\text{boost}} = 0.9 \text{ mH}$; $R_{\text{load}} = 120 \text{ }\Omega$; $L_{\text{load}} = 3 \text{ mH/phase}$; $f_{\text{sw}} = 8 \text{ kHz}$.

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