INVESTIGATION INTO STABLE FAILURE TO SHORT CIRCUIT IN IGBT POWER MODULES

BY

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ABSTRACT

This doctoral thesis investigates modes of failure of the IGBT power module and how these modes can be coerced from an open circuit failure mode (OCFM) to a stable short circuit failure mode (SCFM) by using different interconnect technologies and material systems. SCFM is of great importance for a number of applications where IGBT power modules are connected in series string e.g. high voltage modular multi-level converters (M^2LC) where one module failing to an OCFM can shut down the whole converter.

The failure modes of IGBT samples based on wirebond, flexible PCB, sandwich and press pack structured interconnect technologies have been investigated. Destructive Type-II failure test were performed which concluded that the SCFM is dependent on the energy level dissipating in the power module and the interconnect technology. The higher thermal mass and stronger mechanical constraint of the interconnect enables module to withstand higher energy dissipation.

The cross-sections of the tested samples have been characterised with the scanning electron microscope and three dimensional X-ray computed tomography imaging. It was observed that the networked conductive phases within the solidification structure and the Sn-3.5Ag filled in cracks of the residual Si IGBT are responsible for low resistance conduction paths. The best networked conductive phase with lowest electrical resistance and high stability was offered by Ag if used as an intermediate interconnect material on emitter side of an IGBT.

To offer a stable SCFM, a module has to be custom designed for a particular application. Hence for the applications which demand a stable SCFM, the IGBT module design becomes an integrated part of the complete power electronics system design.

"To my loving parents Mr. M. Yaqub & Mrs. Razia Sultana"

"To my beloved wife Ayesha and my daughter Zara"

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1 INTRODUCTION

1.1 Motivation

IGBT power modules are a workhorse of modern industry where they are used as switching devices in various applications such as modular multi-level converters (M^2LC), traction motor drives, renewable energy, pulse power systems (PPS), switch mode power supplies (SMPS), uninterruptable power supplies (UPS) and aerospace applications. Recently, modular multi-level converters or M^2LC have gained popularity particularly for their use in high voltage direct current (HVDC) transmission systems. They offer higher efficiency and very low level of the harmonic distortion which eliminates requirement of the harmonic filters in the HVDC system. Figure 1 shows the circuit diagram of the power stage of a modular multi-level converter in which 'n' numbers of sub modules are connected in series in each leg to support high voltage. Each sub module consists of an IGBT power module in half-bridge configuration along with a local DC storage capacitor [1].

Although the converters are designed with extreme care and consideration enabling them to deal with various kind of fault scenarios e.g. over current, over voltage etc. still it is highly likely that they will fail by experiencing a fault condition which it was not designed to tolerate, either because this was overlooked by the designer, or because it was not commercially viable to design for such a condition. The fault condition can be caused by various reasons e.g. gate drive fault, control system fault or short/open circuit at load etc.

In a converter, there are other components besides IGBT power modules: for example control system, gate drives and passive components such as filter capacitors and reactors. When the fault occurs, depending on the fault type and current that flows

through the circuit during fault condition, filter capacitors and reactors usually survive as they are quite robust and are capable to withstand instantaneous large peak currents. IGBT power modules on the other hand have limited capacity to withstand large peak currents, hence resulting in their failure. Therefore the weakest link in power circuit of a converter is the IGBT power module [2, 3].

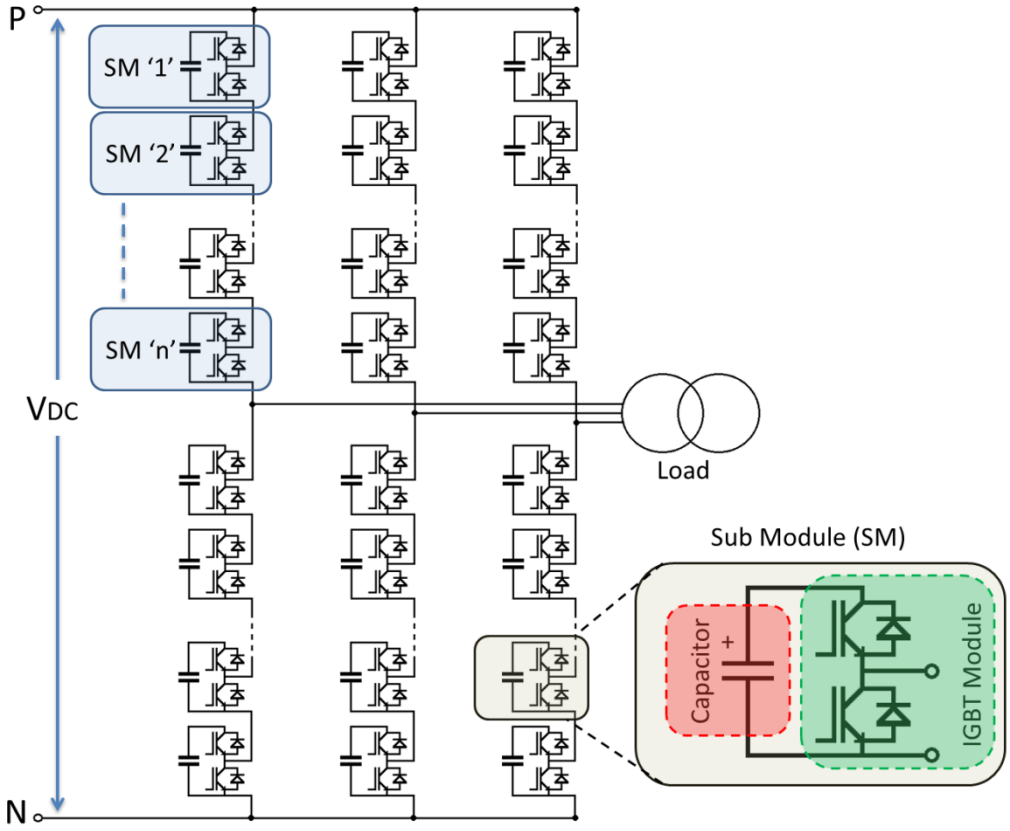


Figure 1: Modular multi-level converter [1].

Figure 1 shows that each sub module has a local DC storage capacitor which acts as a DC voltage divider and also protects the IGBT from unwanted voltage spikes caused by the parasitic inductance of DC bus when IGBT devices are switched. In a sub module, if the capacitance of the capacitor is 24mF and is charged up to 1300V, the energy stored in capacitor would be 20.3 kJ and if an IGBT power module fails, this local stored energy can dissipated inside the IGBT power module causing a massive explosion and possibility of emission of shrapnel [4].

After the failure of the IGBT power module, the workability of the converter is dependent on the failure mode of IGBT power module. If the module has achieved an open circuit failure mode (OCFM), there will be no current passing through the leg where the failure has occurred; hence the converter will stop working. Whereas, if the module has achieved the short circuit failure mode (SCFM), current can still pass through the failed sub module and if the rest of the sub modules in the converter leg can block the V_{DC} safely, the converter would continue its operation in spite of the sub module failure. This implies that if the converter is designed with additional or redundant sub modules, having failure to short circuit ability, the operational life span of the converter can be increased.

The large operational life span of the converter is especially important for the systems which are installed very remotely, at places which are not easy to excess or where the cost of unscheduled maintenance is very high [3]. The failed sub module can be replaced later during the scheduled maintenance. This implies that once an IGBT power module achieves SCFM, the life time of the SCFM or stability of SCFM is also equally important, and the module has to offer a stable current conduction path for at least the time period equal to the time period of the scheduled maintenance.

This raises a series of interesting questions, for example: what is the mode of failure of a conventional IGBT module? What are the factors that cause an IGBT module to fail to open or short circuit? Can the design of an IGBT module, the materials used in its construction, or the techniques used to provide interconnects to the semiconductor die within, influence the likelihood of a module failing to short-circuit, and what factors contribute to the stability of SCFM?

The aim of this thesis is to find answers to these questions and to understand the conditions which are necessary to facilitate and form a stable failure to short circuit in IGBT power modules.

1.2 Conventional Packaging and its Problems

A typical power IGBT module can be seen in Figure 2. In a conventional power IGBT module, the IGBT dies are attached to the metalized ceramic substrate. The latter consists of a ceramic layer (aluminium nitride, alumina) sandwiched between two copper layers.

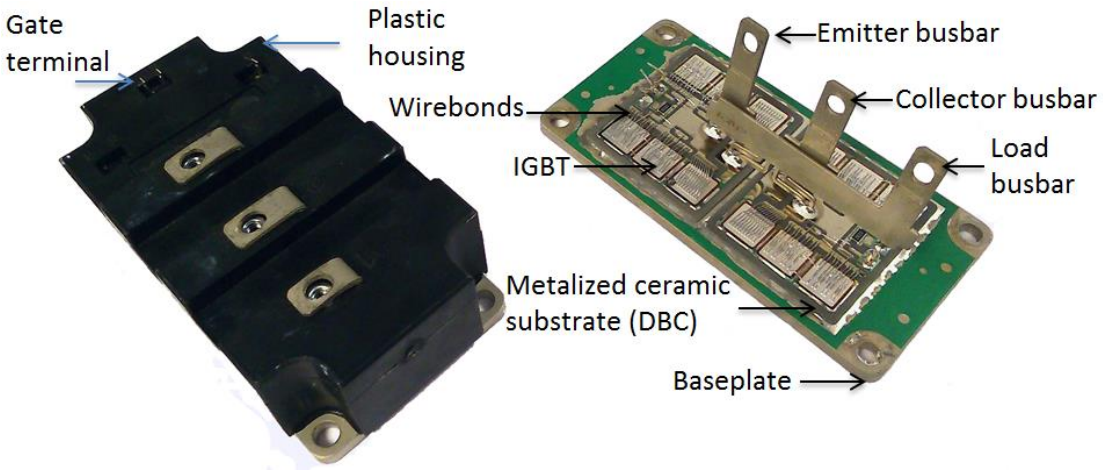


Figure 2: IGBT power module

The top copper layer of substrate provides copper tracks of customised design for different circuit configuration e.g. chopper or half bridge etc. The interconnections between the emitter and gate and the copper tracks of substrate is done by using ultrasonically bonded/welded Al wires. The collector, emitter and gate terminals of the device are finally taken out of module using busbars which are also soldered on to the top copper tracks of the substrate. The middle ceramic layer has high thermal conductivity and dielectric strength hence it provides electrical isolation from top

metallization to the bottom metallization and offers a channel to the heat losses incurred in the junction of the devices during their normal operation. The bottom metallization of the substrate is soldered on the baseplate which is normally made of AlSiC and is slightly curved i.e. either plano-convex or plano-concave shape to enhance the thermal contact when it is fixed by screws on the mounting. A small layer of Thermal interface Material (TIM) is applied between the heat sink and baseplate interface which improves the thermal contact between the heat sink and baseplate. Silicone dielectric gel which has high dielectric strength is used to encapsulate the components which further enhances the breakdown voltage of the module hence enabling it to be operated at high voltages. The module is then covered with a plastic housing which provides electrical insulation between the electrical terminals, a large creepage distance and mechanical stability under elevated temperature and polluted environmental conditions.

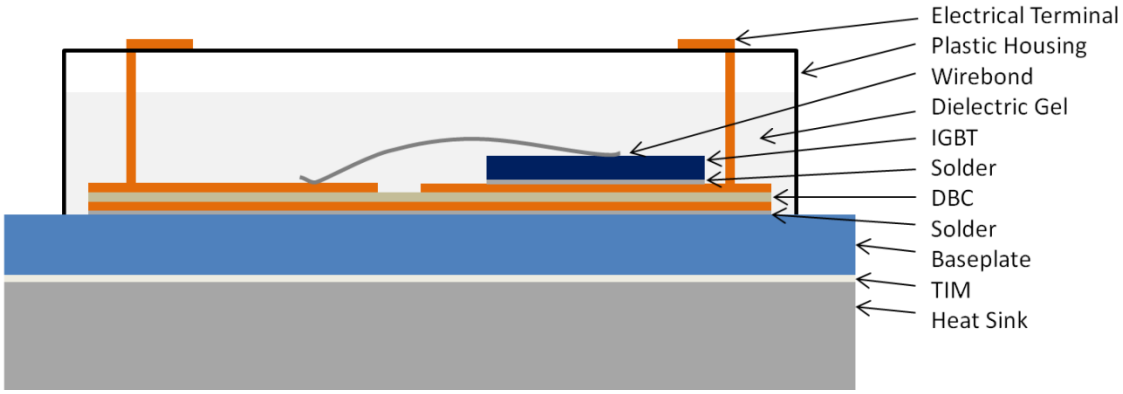


Figure 3: Cross-section of conventional power IGBT module

The analysis of the IGBT market suggests that it is dominated by the classic wirebonded IGBT modules and its variants. It is possibly because of the fact that this packaging technology was introduced in the 80's and was originally applied to packaging of metal oxide semiconductor field effect transistors (MOSFET) and

bipolar junction transistors (BJT). After the invention of IGBT, similar packaging technology was used for IGBT power modules.

Since the introduction of the first commercially available power IGBT module the emphasis was more inclined towards solving the problems related to the power semiconductor device. Lot of research was carried out to make the devices more reliable, efficient and rugged. Unfortunately packaging on the other hand was not given much emphasis possibly because it was fulfilling the requirements of the applications with slight compromises or because at that time applications were not as challenging as they are now. Figure 4 shows the comparison of an old module with a new one, where it can be seen that both old and the new module have same external appearance.

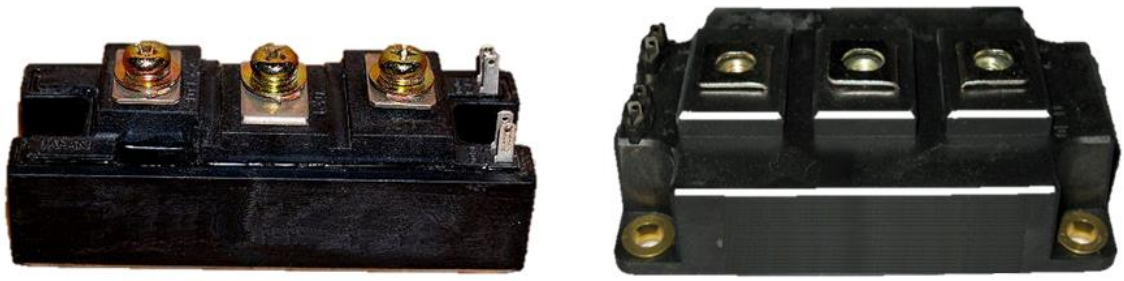


Figure 4: IGBT modules (left) from 80's, (right) latest IGBT module.

On the other hand, due to the ongoing technological developments in power electronics, industrial applications are evolving and becoming more demanding. Industrial applications require IGBT modules with SCFM capability, low inductance, high surge current rating, high current density, high operating temperature and high reliability. The parasitic inductance offered by the packaging of a conventional wirebonded IGBT module is more or less adequate enough to switch the Si based semiconductor devices because they only switch at a few kHz. On the other hand for SiC based semiconductor devices which operate few hundreds of kHz, even a small

parasitic inductance offered by the packaging would result into a massive voltage overshoot during the turn off period, hence SiC based semiconductor devices cannot be packaged in the same packaging. Likewise, single sided cooling offered by the conventional IGBT module is adequate enough to remove thermal losses produced by Si based semiconductor devices because their current density is less as compared to SiC based semiconductor devices which has high current density. Hence it needs double sided cooling which unfortunately is not possible to achieve by using conventional packaging technology.

In summary modern and future industrial applications require the development of an IGBT power module with high current density, SCFM capability, double side cooling, low inductance, high surge current, low loss and reduced cost. All these industrial application demands cannot be completed by using conventionally packaged power IGBT modules hence research in advance packaging techniques is of great importance to develop an alternative packaging technology which can make power modules more compatible with modern industrial applications.

1.3 Problems addressed in this Thesis

This thesis will address the problems associated with the existing solutions to achieve SCFM in IGBT power modules, which include the high costs incurred with achieving extremely flat surfaces of different components, the complicated structure and the complex manufacture procedure. Therefore, the main objective of this research work is to understand the failure mechanism of the IGBT power module by investigation into the interconnect structures and its relation to energy absorption and how to achieve low and stable contact resistance in the failed module. The results obtained are expected to provide guidance for further investigation and development of IGBT

power modules featuring SCFM with the possibility of a simple structure and a low manufacturing cost.

To achieve the above specified objectives, the first challenge of the research work is to develop an understanding about the **modes of failure** of a conventional IGBT power module. The second is to find out the effect on failure modes of using different **interconnect technology**. The third task is to find out the **structure** of the power module which facilitates SCFM. The final task is to find out the **material system and minimum thickness** which enables a stable SCFM.

1.4 Research Contributions

The main contribution of this work is the investigation and the identification of a relatively simple and cost effective solution for design and manufacturing of IGBT modules which feature failure to short circuit behaviour. The specific contributions include:

- The failure behaviours of the IGBT modules constructed with four interconnect technologies including conventional aluminium wirebond, flexible PCB, sandwich structure and press pack structure have been investigated;
- The ability of featuring failure to short circuit behaviour for the sandwich structure IGBT module under realistic energy levels in the event of IGBT destruction has been demonstrated;
- The microstructures of the tested IGBT modules with both failure to open circuit behaviour and failure to short circuit behaviour have been characterised;

- The phase changes of the component materials in the IGBT modules during overcurrent testing have been looked into;
- The material systems which result into stable SCFM have been investigated along with the identification of the most suitable material;
- The minimum thickness of intermediate layer for achieving the stable SCFM has been quantified.

1.5 Application of the Project

1.5.1 Modular Multi-level Converters

High voltage modular multi-level (M^2LC) converters will be used in high voltage direct current transmission networks. In this application several low voltage IGBT modules are connected in a series string to achieve the required voltage rating [1, 5]. If one of the series connected modules fails to open circuit, the whole converter can no longer be functional as there would be no current path. The outcome of this research can be used to make modules which can achieve a stable SCFM and hence can enable the converter to continue its operation even if modules have failed as long as the rest of the modules can withstand the overall input DC rail voltage.

1.5.2 High Speed switching Devices

Another potential application of this research is in the area of high speed switching device packaging. In comparison to Si based devices, Silicon Carbide (SiC) devices operate at quite high switching frequencies. If SiC devices are packaged in the conventional way, at higher switching frequencies, the rate of change of current di/dt becomes high and if there is even a very small parasitic inductance in the current commutation loop, it will result in a high voltage overshoot which can destroy the

device [6, 7]. In other words SiC devices are capable of operating at a high switching frequency but the current packaging technology is limiting it. By using the physical layout of the packaging which enables the achievement of SCFM, the parasitic inductance can be decreased significantly hence enabling the operation of SiC devices at higher frequencies and higher voltages.

1.5.3 Explosion Proof Packaging

In a typical voltage source converter application, the energy from the supply is temporarily stored locally in a large capacitor before being fed to the IGBT power module. If the module fails short circuit, all of the energy from the capacitor gets dissipated inside the module which leads to a massive destruction to not only the module itself but to the area surrounding it [4].

The reason for this explosion is as the device goes short circuit, a very large current passes through it which causes the meltdown of the wire bonds, hence initiating arcing. The arcing then produces high temperature plasma. This rise in temperature causes the materials inside the conventional IGBT module to vaporise and as the structure of the module is not confined, metallic shrapnel escapes the packaging at very high velocities. These high velocity shrapnel along with other debris can damage the delicate control circuitry and injure or harm nearby personnel.

The outcome of this research can be utilised to make explosion proof packaging because unlike the conventional IGBT module where the packaging is not confined, the new layout is based on the confined structure which will not permit any debris to escape the packaging hence not only saving the rest of the converter from the debris of failed device but also reduce the risk of personnel injury.

1.5.4 High Reliability

The IGBT devices by themselves are very reliable as long as they are operated within the limits defined in their datasheet. The weakest link is the interconnect technology i.e. the wirebonds and the soldering of the device on the substrate in which failure can easily take place when the module is subjected to the electro-thermal stress [8, 9]. The outcome of this research has led to the wirebond less silver sintered interconnect technique which can extend the operational lifespan of the module.

1.5.5 New Manufacturing Approach

The conventional IGBT module packaging process is quite slow labour intensive, expensive and inefficient. The emitter contact of each IGBT die involves at least 25 ultrasonic bonds and if there is a 200A module, it will require approximately 300 individual bonds which is a very slow process and often results in a low yield.

As there are no wirebonds involved in manufacturing of a module which can achieve SCFM, it can open a doorway to explore the new possibilities of more efficient and high yield manufacturing processes which might have potential to reduce the manufacturing cost and this needs to be investigated.

1.5.6 Double Sided Cooling

When the device turns on, it conducts current and dissipates heat. This heat causes the junction temperature of the device to rise and if the temperature exceeds the maximum junction temperature of the device, the device fails. Power modules must extract this heat as efficiently as possible. Conventional IGBT modules are single sided cooled because of their construction, this means that the heat goes out of the system in one direction, only normally through baseplate and the heat sink. The physical layout of

the module which achieves SCFM allows cooling from both sides which can help in more efficient cooling of the devices.

1.6 Overview of the Thesis

This thesis consists of eight chapters. Chapter 1 highlights the impact of this research work i.e. the applications which can benefit from the outcomes of this research. It also provides summary of existing packaging technologies their advantages and shortfalls. The current problems and challenges faced by the application industry have been identified which is basically the motivation behind this research work.

Chapter 2 is the literature review of the existing packaging technologies. In Chapter 3 tests were carried out on a simple wirebonded test vehicle to understand whether it fails to open or short circuit and relationship of the failure mode with the input energy is also discussed. Chapter 4 presents the experimental results of failure mode of flexible PCB based interconnect technology. The failure mode of sandwich structure is explored in Chapter 5.

In chapter 6 a simplified press pack IGBT (PPI) test vehicle is constructed and tested for its abilities for the failure to short circuit. Chapter 7 deals with the investigation into the most suitable material which could facilitate a failure to stable short circuit along with finding out its minimum thickness. Finally Chapter 8 contains the conclusions of the research and contribution of this research towards the packaging technology to develop a SCFM capable module.

2 LITERATURE REVIEW

Interconnect in IGBT power modules is the use of materials and technologies to electrically and mechanically connect the collector, emitter and gate of the device to the internal/external circuit for forming the intended electrically conductive paths while ensuring mechanical stability. It is the important part of the packaging process for achieving stable failure to short circuit behaviour of the power module. This is because the failure in IGBT power modules is in general caused by extremely rapid electric-thermal energy dissipation, while both the mechanical structure and the thermal and electric conducting paths of the power module during the operation heavily depend on the interconnect technology. Destructive testing of IGBTs is an essential part of this research therefore different electrical short circuit failure types encountered by IGBTs will be reviewed in sub-section 2.1. Then conventional aluminium wirebond technology along with all the interconnect technologies under investigation and development for overcoming the thermal and electric limits of aluminium wirebond will be reviewed. They include ribbon bond, embedded chip technology, metal post-interconnect parallel-plate structure, dimple array interconnect, planar interconnect technology, pressure contact technology, flexible PCB based packaging technology and press pack IGBT. Despite the fact that the majority of these interconnect technologies have not directly been intended for achieving failure to short circuit behaviour, analysis and understanding of them can be useful and closely associated with the present work. This is because a systematic review of these interconnect technologies can gain knowledge and clues on how to design the mechanical structure and select interconnect materials for obtaining the desirable electric-thermal energy dissipation to favour failure to short circuit behaviour of the

power module. Therefore, the interconnect technologies not directly intended for achieving failure to short circuit behaviour, together with conventional aluminium wirebond technology, will be reviewed in sub-section 2.2. On the other hand, two of the IGBT power modules using the press pack interconnect technology have been proposed and developed for achieving failure to short circuit behaviour of the power module. They are more closely related to the present work, and hence a more detailed review of them will be given in a separate sub-section (2.3).

2.1 Electrical Failure modes of an IGBT

Generally the electrical failure modes of IGBT power modules can be classified as open circuit failure and short circuit failure. Open circuit failure can be caused by an external loose electrical connection, rupture of wire due to passage of high current or wirebonds lift off. This can lead to discontinuous, reduced or intermittent flow of current, which consequently may lead to secondary failure which can be catastrophic. The electrical short circuit failure of an IGBT module involves the flow of uncontrolled surge current in a converter which can lead to potential destruction to not only the failed device but the other components as well [10, 11].

2.1.1 Open circuit failure

The open circuit failure can be further classified into two types

2.1.1.1 Wirebond Lift-off

Aluminium wirebond is an interconnect technology which is used to make electrical connections with the gate and emitter side of IGBTs. During the normal operation of the device, the IGBTs are subjected to the power/thermal cycling which causes the wirebond lift off. The lift off is due to the mismatch in the coefficient of thermal expansion (CTE) between the Al wirebond and the Si device. The thermal cycling

causes the initiation of cracks in the periphery of the bond and finally results in lift off [12].

2.1.1.2 Gate Drive Failure

The gate drive failure can be due to damaged device or disconnected/loose wires between gate drive and IGBT module [13]. This may lead to intermittent misfiring which can initiate secondary failure which can be catastrophic. If gate terminal goes open circuit i.e. become floating, it can possibly result in thermal runaway or high power dissipation [14].

2.1.2 Short Circuit Failure

The short circuit failure can be classified into the following types:

2.1.2.1 High Voltage Breakdown

It is caused by the high voltage overshoot which is induced by high di/dt of the collector current and stray inductance during the device turn off switching transient. If the voltage overshoot is high, the electric field can reach the critical region which will initially result in breakdown of a few cells in the IGBT first. This will result in high leakage current which will rise local temperature forming hotspots. Subsequently, this leads to the heat diffusion from the hot spots to the neighbouring cells eventually resulting in catastrophic failure [15]. The high voltage breakdown can also happen due to high value of collector to emitter voltage Vce and gate to emitter voltage Vge. It results into abrupt destruction followed by a surge of current during turn on of the device [16].

2.1.2.2 Static and Dynamic Latch-up

In IGBTs, latch-up occurs when collector current (Ic) can no longer be controlled by the gate. The equivalent circuit of an IGBT is shown in Figure 5. Latch-up happens

due to the turn on of the parasitic NPN transistor which causes the main PNP transistor to act as a thyristor and hence control over the collector current can no longer be established by using the gate terminal. The latch-up is of two types, static and dynamic latch-up [17]

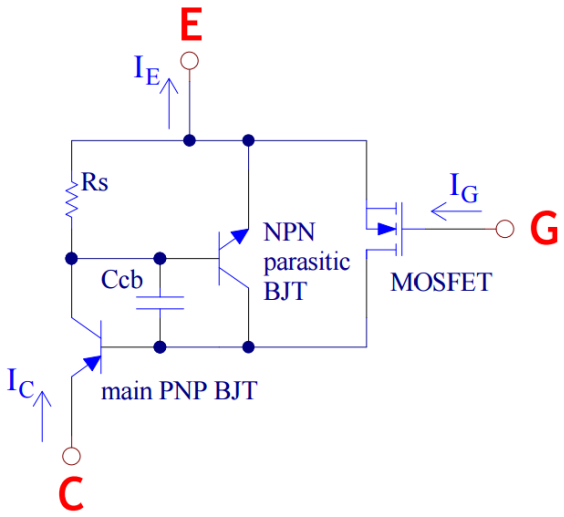


Figure 5: The equivalent circuit of IGBT [17]

Static latch-up happens due to high Ic which causes a high voltage drop across the parasitic resistance Rs resulting in turn on of the NPN parasitic bipolar junction transistor (BJT). The dynamic latch-up happens normally during the turn off of the IGBT when the NPN parasitic BJT is biased by the junction capacitance Ccb. Both types of latch-up result into catastrophic failure as the control over the gate is lost. The latest generation of IGBT devices having a trench gate structure and the heavily doped P-base region under N-emitter have demonstrated good latch-up immunity and is not considered as a common failure in modern IGBT devices [18].

2.1.2.3 Second Breakdown

It is a thermal breakdown of the device due to high stress current. The sequence of events for second breakdown is as follows: the increase in collector current causes increase in collector-base junction space-charge density. This decreases the

breakdown voltage which in return further increases the current density. The process continues until the high current density region reduces to the minimum area of a stable current filament. This results in the rapid rise in temperature and collapse of voltage across IGBT [11, 19].

2.1.2.4 Energy Shocks

When an IGBT encounters a short circuit during its normal operation, high power is dissipated in the module which can result in the failure of the device. The energy shock is the dissipation of high power in the device in a short time interval. This results in the flow of short circuit current which rapidly rises temperature[20, 21]. During the energy shock, the device does not fail until the heat generated due to the power dissipation exceeds the Intrinsic Temperature (250°C) of the Si. The intrinsic temperature is dependent on the voltage rating of the device and it normally decreases with the increase in operating voltage of the device. Once the device reaches its intrinsic temperature, any further rise in junction temperature would increase the charge carriers exponentially resulting in thermal runaway.

Type-I and Type-II short circuit failure can both be classified as energy shock failure. Type-I failure happens when the already turned ‘on’ device encounters a short circuit. It is also known as fault under load [21].

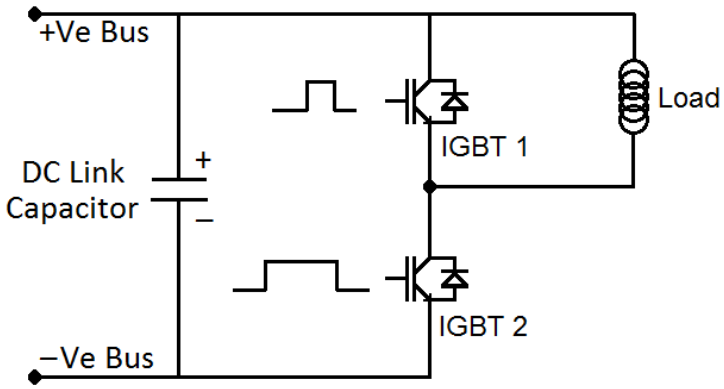


Figure 6: Test circuit to perform short circuit [21]

Figure 6 shows the test circuit to perform the short circuit test. The idealised waveforms of the type-I test can be seen in Figure 7 (a). Here Ic is the collector current and Vce is the voltage across the device. During time interval T1, the IGBT2 is in 'on' state and is working normally and it can be seen that Vce level is low. During time interval T2, the IGBT 1 erroneously turns 'on', this will cause a huge rise in current which can be seen in time interval T2. The IGBT2 leaves from the conduction state and enters the active region. This will result in high power dissipation in the device causing the thermal overload and hence eventually failure of the device.

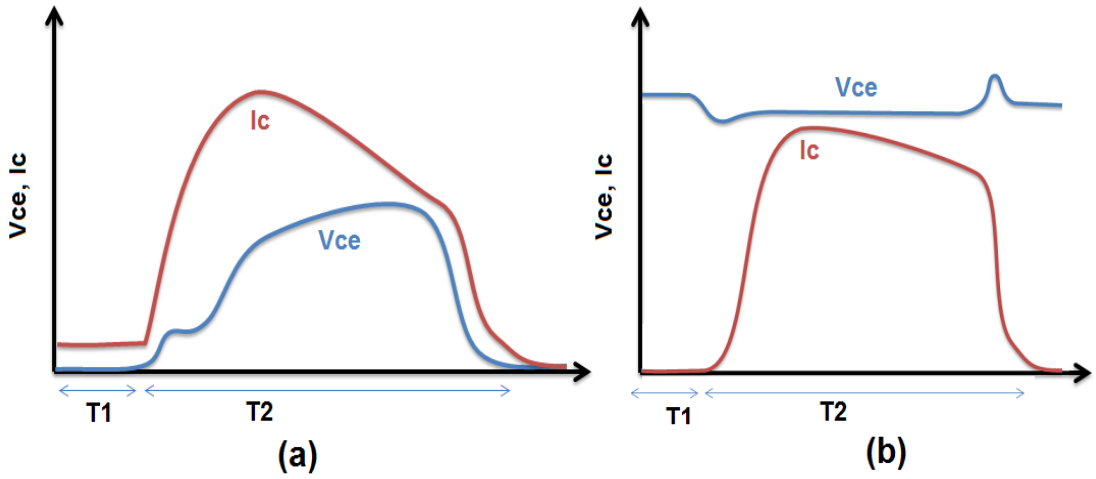


Figure 7: Idealised voltage and current waveforms of (a) Type-I and (b) Type-II test.

A Type-II short circuit happens when the device is turned 'on' into an already existing short circuit. Type II failure is also known as the hard switch fault [21]. This type of short circuit fault can be created by putting a short circuit across the load and turning on IGBT2. This will turn 'on' the IGBT straight into a short circuit. The idealised voltage and current waveforms can be seen in Figure 7(b). In time interval T1, the device is off and Vce is equal to the DC input voltage. In time interval T2, the device is switched 'on' which will basically put a short circuit across the DC link capacitor

resulting in flow of short circuit current through the device. This will result in dissipation of all the energy stored in the DC link capacitor to dissipate in the device resulting in thermal overload and catastrophic failure of the device.

The method used to achieve destructive failure of IGBTs in this research work resembles the Type-II method which results in thermal overload failure. It involves turning on of the IGBT into a short circuit which cause an uncontrolled flow of current through the device resulting in thermally overloading the device and hence its failure.

2.2 Interconnect Technologies

2.2.1 Wirebond

Wirebond is the most common interconnect technology which is widely employed in power IGBT modules. Figure 8 shows an IGBT module in which wirebond on top of the IGBTs provides an electrical connection with the emitter and gate terminal of the device. The bond is made by a tool which vibrates from 40 to 100 kHz to bond the wire [22, 23].

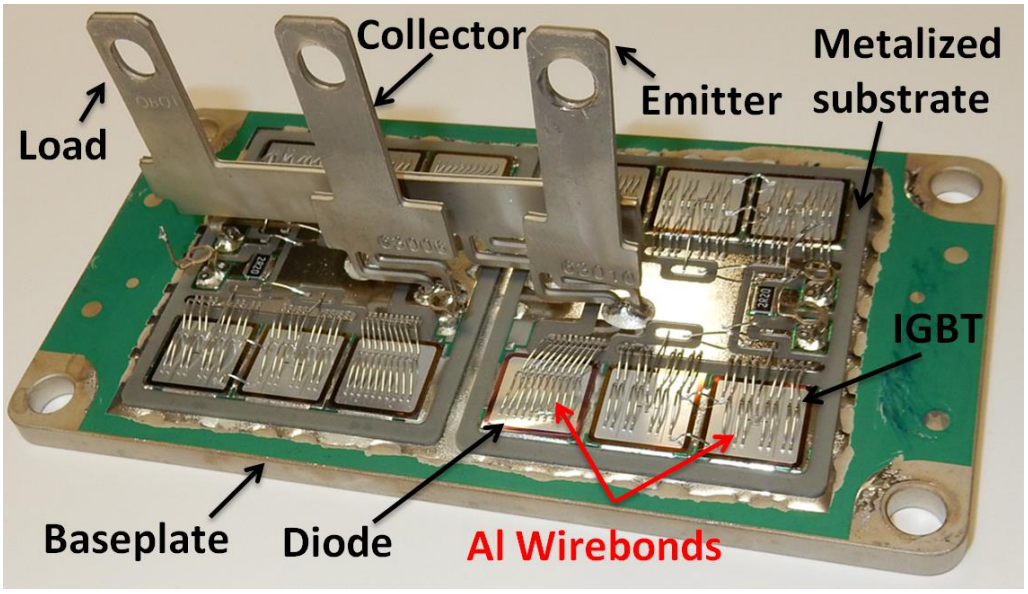


Figure 8: Wirebonds interconnection in IGBT module

The most common wire used for bonding is aluminium but copper wire is appearing to be used by few manufacturers for high power modules[24, 25]. The main reasons for the popularity of aluminium wirebonding are the established manufacturing process and the availability of support in the form of both infrastructure and literature from industry. The bonding process itself is highly flexible especially for handling complex geometries of substrates and dies and the bonding equipment is easy to program for automated manufacturing. However, wirebonding is a slow process and its disadvantages include reduced electrical performance, parasitic inductance, non-

uniform current distribution which results into poor transient current sharing [26]. It is also prone to fatigue which causes it to lift off during power/thermal cycling [12, 27].

2.2.2 Ribbon Bonding

Ribbon bonding has been developed to replace wire bonding for improving electrical performance and reliability [28]. Figure 9 shows a ribbon bond. Instead of bonding a large number of wires, a few thick Al ribbons are bonded. For example if eight 15mils diameter Al wires are bonded on the IGBT, these can be replaced by using three 70mil x 8mils Al ribbons. The bonding process is similar to that of wires except that a special tool is required to perform the bonding. Its advantages are a large area of electrical contact resulting in better electrical performance and reduction in parasitic inductance.

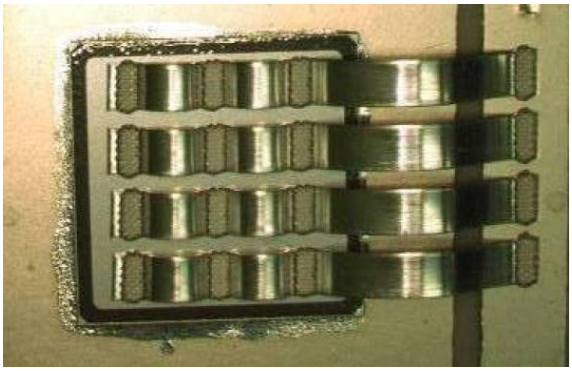


Figure 9: Ribbon Bonding[28]

It was reported that when subjected to temperature cycling from -60°C to 170°C for 2000 cycles, it resulted in exceptional bond strength and reliability as compared to the wirebonds [28]. As compared to the wirebonds, the bonding of thick ribbon requires high pressure on the die and to compensate for that a thick metallisation is required on the die to avoid cracking and the problem can get worse if bonding is performed on a thin device [29].

2.2.3 Embedded Chip Technology

The embedded chip technology (ECT) has been developed to not only eliminate the use of die attachment and wire bonds, but also achieve high temperature operation, reduction in parasitic inductance and increase in power density [30]. Figure 10 shows the cross-section of an embedded chip module which has been built using ECT [30]. It consists of a ceramic substrate containing openings to hold the device; the power semiconductor die is placed in the opening and is fixed with adhesive. A dielectric layer is printed on the top of device which contains a via. Seed layers are sputtered on both the top side and bottom side of the device, and interconnects are achieved with further electroplated Cu [30].

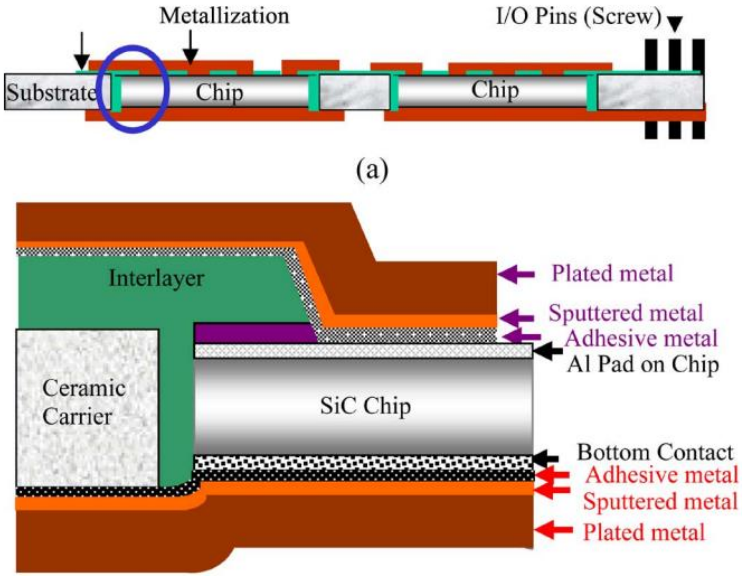


Figure 10: Embedded Chip Module [30]

The experimental results show that the module can be operated at 200°C. In order to operate at high temperature, a close matching of coefficient of thermal expansion (CTE) between different layers of module has been achieved by placing a chromium layer between the chip and the top copper interface. It has also been highlighted that a power density of $284 W/in^3$ under forced convection at room temperature has been

achieved which is 5 times the power density of a Si based module under similar conditions[30]. However, no reliability study has been carried out. Although the authors claim that the mechanical stresses generated by the CTE mismatch has been reduced, but the thermal stress analysis performed by Lee Pik *et al.* suggests the mechanical stress of an embedded chip module increases with thickness of the device [31].

2.2.4 Metal Post-Interconnected Parallel-Plate Structure

The metal post-interconnected parallel-plate structure (MPIPPS) is another packaging technology which uses metal posts instead of wirebonds to make connections with the emitter and gate of the device [32, 33]. As shown in Figure 11, in a MPIPPS module, the IGBT die is soldered on the direct bonded copper (DBC) substrate which can be directly mounted on a heat sink. The copper posts are bonded to the top side of the die by soldering and a specially manufactured DBC is then soldered on top of the metal posts creating a sandwich structure [32, 33].

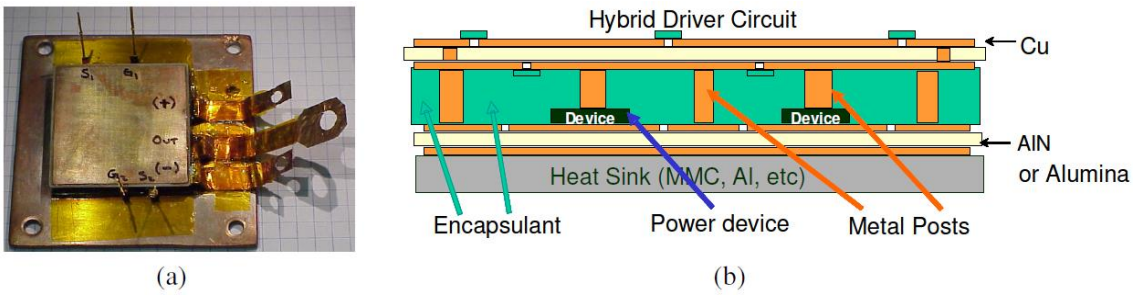


Figure 11: Metal Post Interconnect Parallel Plate Structure module (a) Photograph (b) cross-section [33].

The MPIPPS offers low DC resistance, reduced parasitic inductance and capacitance, better thermal management, easy integration of passive components, easy manufacturability and robustness [32, 33]. The electrical performance data of the packaged device shows that an air cooled 15 kW inverter operating from a 400V dc

bus at 20kHz switching frequency can be constructed by using three MPIPPS module which is almost twice the power that can be achieved using commercially packaged devices with similar ratings [32].

However, the authors have not highlighted any reliability issues arising from the CTE mismatch between the copper post and the silicon die. Soldering the copper posts on the device requires the top metallization of the device to be changed from aluminium to silver or copper which is a difficult process and can result into high contact resistance if the metallization is not done properly [34].

MPIPPS has also been used to develop an integrated power electronic module (IPEM) which offers superior thermal performance and high power density as it has integrated gate drives, decoupling capacitors and cooling mechanism[35].

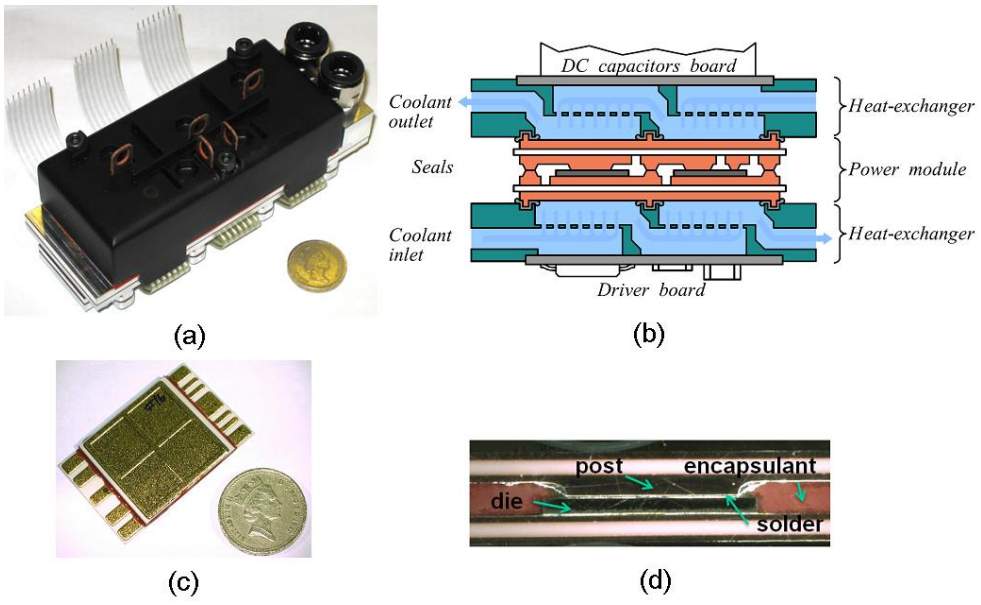


Figure 12: Integrated power electronic module [35] (a) module, (b) cross-section, (c) power module, (d) cross-section of power module.

Figure 12 shows a 600V 10kW three phase IPEM inverter where the metal posts are formed on the specially designed substrates by etching. It requires two reflow steps for assembly, first die and bottom substrate attachment is done using high temperature

solder e.g. AuSn, secondly bottom DBC, the top DBC attachment is done by low temperature solder e.g. SnAg hence resulting in a sandwich structure. It does not have any baseplate which implies that it has a shorter heat transfer path and lower stress levels during thermal cycling. The module is double side cooled by direct water impingement which provides more efficient cooling[35].

The complete module is quite compact in size with volumetric power density $30W/cm^3$and gravimetric power density of 17kW/kg [35]. The turn on/off electrical test results shows that there was no noticeable voltage overshoot which indicates that the module has very low parasitic inductance. The pressure drop vs flowrate curve suggests that the pressure drop in the cooling system was very low and can be further adapted to requirements by series/parallel combination of impingement cells [36]. The junction to case thermal resistance is 1.2 °C/W which enables it to dissipate three times more heat to reach the same junction temperature as in conventional wirebonded module [36]. However, the active power cycling from +45°C to 105°C performed on the module shows the premature failure of the module after 500 cycles which could be attributed to the poor quality of nickel layer on top of the devices which can be improved [36]. From the perspective of thermal conductivity, power density and low parasitic inductance, the module has very good performance, however the manufacturing is very difficult and time consuming especially etching of the substrates which can result in higher manufacturing cost.

2.2.5 Dimple Array Interconnect

Dimple array interconnect technology has been investigated to improve the thermal conductance and reduce the electrical resistance and parasitic capacitance and inductance [37]. In this interconnect technique, the electrical connections with the device are made using dimpled metal sheet and solder bumps. Figure 13 shows one

module made using dimple array interconnect technology. This structure has better thermal conductance as compared to the wirebonded module due to large area of contact and thermal conductivity of flexible copper sheet on the top. It also offers low electrical resistance and parasitic capacitance and inductance.

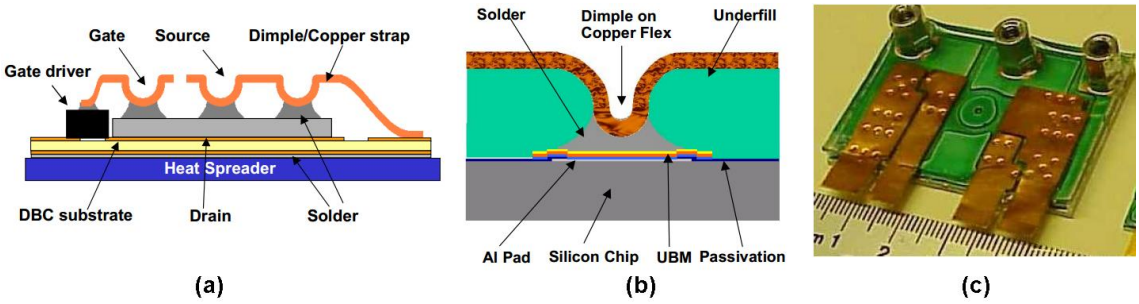


Figure 13: Dimple array interconnect technology [37] (a) cross-section, (b) structure, (c) module.

The test results from turn on/off tests performed on a 600V 50A module shows 60V overshoot during turn off of the device which is considerably lower than the commercially available wirebonded module of similar specifications. This shows the lower parasitic inductance of the module [38]. In this structure, a large amount of mechanical stress concentrates between the die to solder and solder to dimple interface if bonding is done using controlled collapse barrel shaped solder joints [37]. Results from thermal and power cycling test shows that fatigue resistance can be improved if hour glass shaped solder joints are used instead controlled collapse barrel shaped solder joints [38]. However, the authors have not devised any method to control the CTE mismatch issue. Also its reliability relies on the shape of the solder joints which is very hard to control.

2.2.6 Planar Interconnect Technology

A planar interconnect technology, thin film power overlay technology has been introduced for high voltage, high current, low parasitic inductance, decreased

packaging volume, high reliability due to absence of wirebonds and easy adaptability to accommodate different device types in the packaging [39]. Figure 14 shows the cross-section of power overlay technology which was introduced by General Electric. In this technology, the top side of power devices (which is normally aluminium) used are first sputtered with a titanium layer and then a copper layer. The Ti layer acts as an adhesive layer between Cu and Al. The power devices are then soldered on top of the DBC. Polyamide film is attached on top of the soldered devices which is ablated using a laser to expose the electrical connection pads of the devices on which the thick Cu layer is grown using an electroplating process[39, 40].

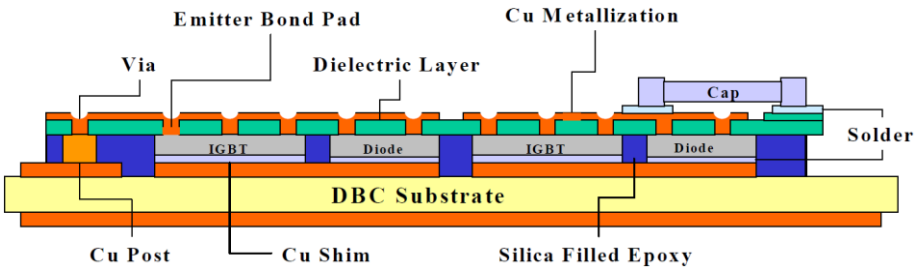


Figure 14: Cross-section of Power Overlay Technology [39]

The key advantages of this technology are increase in electrical contact area, decrease in the parasitic inductance, lower weight and size, higher packaging density and efficient removal of heat from both sides of the device. Although the authors have made some demonstrator modules using this technology e.g. 1200V 400A IGBT based module and 150V 1-2 kW 6.78MHz class-D power amplifier using MOSFETs where they have reduced the height profile of module by 50% compared with wirebonded module but no thermal and electrical test results have been discussed. The issues related to the CTE mismatch between Si and thick Cu metallization in this design have not been completely investigated and there is no published data available regarding its reliability studies.

Similar planar interconnect technology has also been employed by Siemens to develop its planar power module called Siemens planar interconnect technology (SiPLIT). Its salient features are low package induced electrical impedance, reduced electromagnetic interference, and reduced thermal resistance [41]. Figure 15 shows a SiPLIT module, the manufacturing involves soldering of chips on the DBC substrate and depositing a 200 micron thick insulating film on top. Specific areas of the film are then ablated by using a laser. 150μm of copper is electroplated on top of the exposed areas to make the electrical connections [41]. This interconnect technique has better electrical and thermal performance; it has been reported that there has been approximately 20% reduction in on-state resistance and 50% reduction in stray inductance whereas, junction to ambient thermal resistance was 20% less if compared with wirebonded module. Its reliability study shows 600V 100A module has passed over 1000 thermal shocks from -40°C to 150°C whereas it passed 230000 cycles when subjected to 95°C-175°C ΔT power cycling consequently resulting into module failure because of solder die attach fatigue [40, 41].

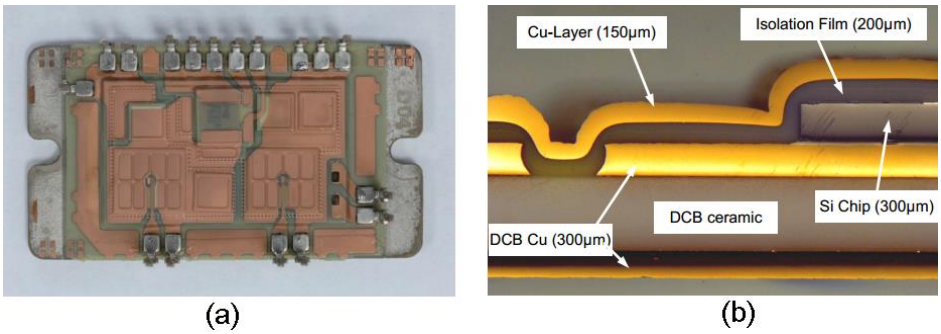


Figure 15: (a) SiPLIT module by Siemens[42], (b) Cross-section of SiPLIT module[41]

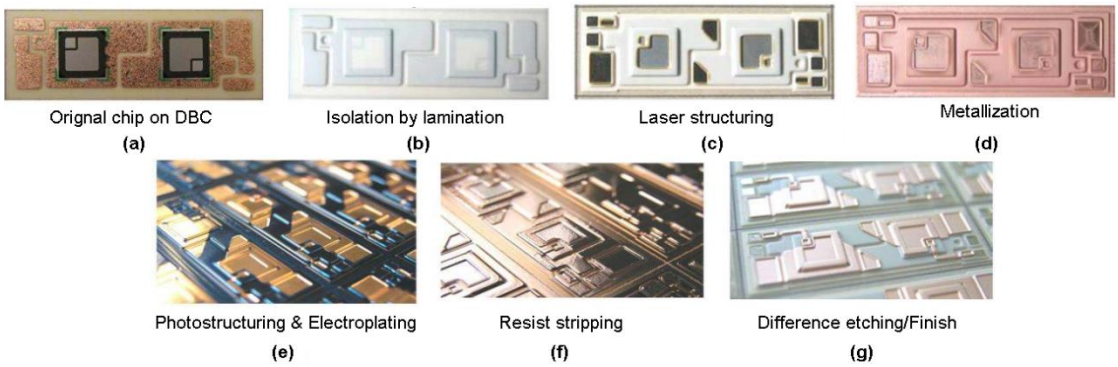


Figure 16: SiPLIT module by Siemens [41], (a) to (g) shows manufacturing process flow

Figure 16 shows the manufacturing process which involves numerous precise and laborious steps which can result into high manufacturing cost also the module cannot be worked back if some manufacturing fault occurs which can result in poor yield.

2.2.7 Wirebonded Module with Pressure Contact Technology (SKiiP)

The distinctive feature offered by pressure contact technology is the sintered devices, high temperature operation, high reliability and absence of solder joints and baseplate. Figure 17 shows the latest SKiiP-4 module; the devices are first sintered on the substrate and then wirebonded. The electrical/auxiliary contacts are made by using different kinds of springs depending upon application. The metalized substrate is directly mounted on the heat sink because of the absence of a baseplate which reduces the thermal resistance hence resulting in an increase in power density. The design of the module is 100% solder free which enables it to eliminate reliability problems related to solder joints [43]. It has been reported that the SKiiP-4 sintered module passed more than 90000 cycles during power cycling test based on IEC60749-34 specifications which is 3 times more than SKM45 module [43].

However, as the devices are wirebonded, the reliability problems related to wirebond still exists.

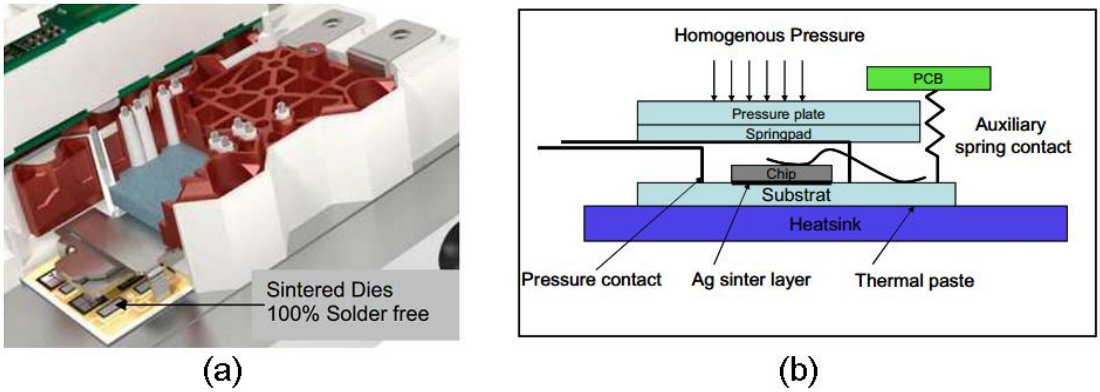


Figure 17: Semikron SKiiP 4 [43], (a) Module, (b) Cross-section

2.2.8 Flexible PCB based Packaging Technology (SKiN)

The unique attribute of flexible PCB based packaging technologies is free from both wirebonds and solder joints, low parasitic inductance, high surge current improved thermal conduction and high reliability [44]. In this technology, the devices are first sintered on to the DBC and instead of wirebonding; a flexible PCB is attached to the top side of the device by sintering which eliminates the reliability issues related to both soldering and wirebonds. The electrical connections are also sintered on the DBC and the DBC is sintered directly on top of the heat sink eliminating the baseplate and thermal interface material. It has been reported that the elimination of the thermal material interface results in the reduction of thermal resistance by 25% as compared to the benchmark conventional module [44]. The large electrical contact area achieved by sintering a flexible PCB also resulted in an increase of 27% in surge current rating as compared to the benchmark conventional module. In passive temperature cycling (-50 to 150°C), the SKiN module passed several hundred cycles before the delamination of DBC to heat sink interface whereas during active power cycling (40 to 150°C), the

SKiN module proved itself to be 10 times more reliable than the Al wirebond based modules[45].

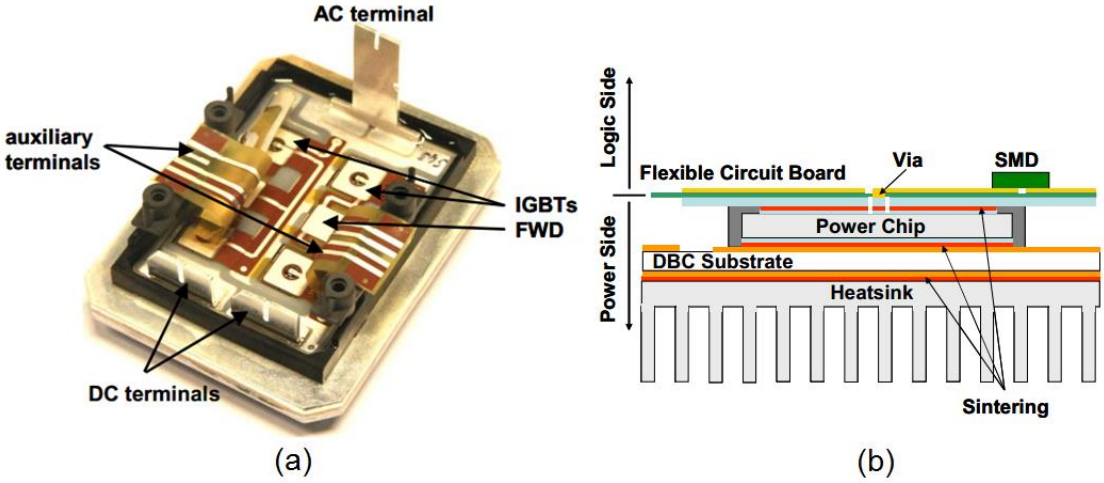


Figure 18: SKiN by Semikron[46](a) Module, (b) Cross-section

In summary, all the interconnect technologies mentioned above offer several advantages over the conventional packaging where they offer reduction in electrical contact resistance, reduction in parasitic capacitance and inductance, improved thermal conduction, double side cooling and increased operational lifetime of module. They are achieved by means of increasing the contact/conducting areas, thermal mass for heat dissipation and mechanical constraint, reducing electrical conducting length, and selecting suitable interconnect materials. Therefore, the mechanical structure and interconnect materials used in these interconnect technologies may be referred to and adopted in the present work to investigate and develop the IGBT power modules with desirable electric-thermal energy dissipation for favouring failure to short circuit behaviour.

2.3 IGBT Modules Favouring Failure to Short Circuit

2.2.1 Press Pack IGBT module

The first commercially available IGBT module (called press pack IGBT (PPI)) which is claimed to have the ability to fail to short circuit was introduced by IXYS UK Westcode Ltd. Figure 19 shows an IXYS UK Westcode Ltd PPI [47]. Its design consists of two parts i.e. the cassette and the ceramic housing. As it would be very difficult to make a pressure contact with a device whose gate is located in the centre therefore, a specially designed IGBT die with gate located at corner has been used. The cassette consists of a plastic housing in which a metallic shim is placed along with a corner gate IGBT die sandwiched between two floating Mo shims. The Mo shims serve two purposes, first they homogenise the pressure distribution on the die to avoid shattering of the die due to pressure peaks. Secondly as the Mo has CTE closer to Si, that makes it the most suitable conductive material to be placed next to the die. The cassette also offers a pogo pin gate contact which when mounted on the copper post located on the pole face of the ceramic housing, gets in contact with the PCB which connects all the gates of the IGBT dies together making a single gate terminal with very low inductance. This configuration completely eliminates all the bonded and soldered interfaces [48]. The number of cassettes is dependent on the current capability of the module. After testing each cassette externally especially for forward voltage blocking capability, the cassettes are carefully mounted on the Cu posts offered by the pole face of the ceramic housing and finally the module is hermetically sealed. One of the advantages of using the ceramic housing is retrofitting of these PPI with the existing designed assemblies based on thyristors and gate turn off thyristors without any modification of the clamping structure. The ceramic housing also reduces

the chances of rupture after catastrophic failure of module which exists with the conventional IGBT module [4, 49].

In contrast to a conventional IGBT module, it has been reported that the low inductance (< 4nH) due to internal structure of PPI and the presence of large thermal mass on the devices makes it very suitable for the pulse power applications with high repetition rates [50]. The ceramic housing normally contains large numbers of individual IGBT cassettes connected in parallel along with diode cassettes which collectively act as a single IGBT along with an antiparallel diode. The low inductance which has been reported is measured from pole to pole of the PPI. However, the parasitic inductance which is responsible for voltage overshoot at the device turn-off event is not the pole to pole inductance; rather it is the commutation loop inductance which depending upon the physical size of the commutation loop path, can be larger in the case of the PPI as compared to a conventional IGBT module.

Some reliability studies have been carried out by the manufacturer where it has been claimed that the components are an order of magnitude better than the conventional thyristors during power cycling [49].

As the whole module is bond free i.e. floating and the module contains several cassettes, the uniform distribution of pressure is very important both for current and thermal conduction and even a slight uneven distribution of pressure can lead to the difference in thermal resistance amongst cassettes during its normal operation [51].

The close examination of the press pack IGBT module shows that the mechanism of pressure distribution relies on the compliance offered by the Cu posts and the metal shim which is placed under the emitter side Mo shim. Nevertheless, in order for this packaging to achieve uniform pressure distribution and to avoid breaking the fragile

cassettes, everything has to be very flat and precise which makes it very complex and expensive to manufacture.

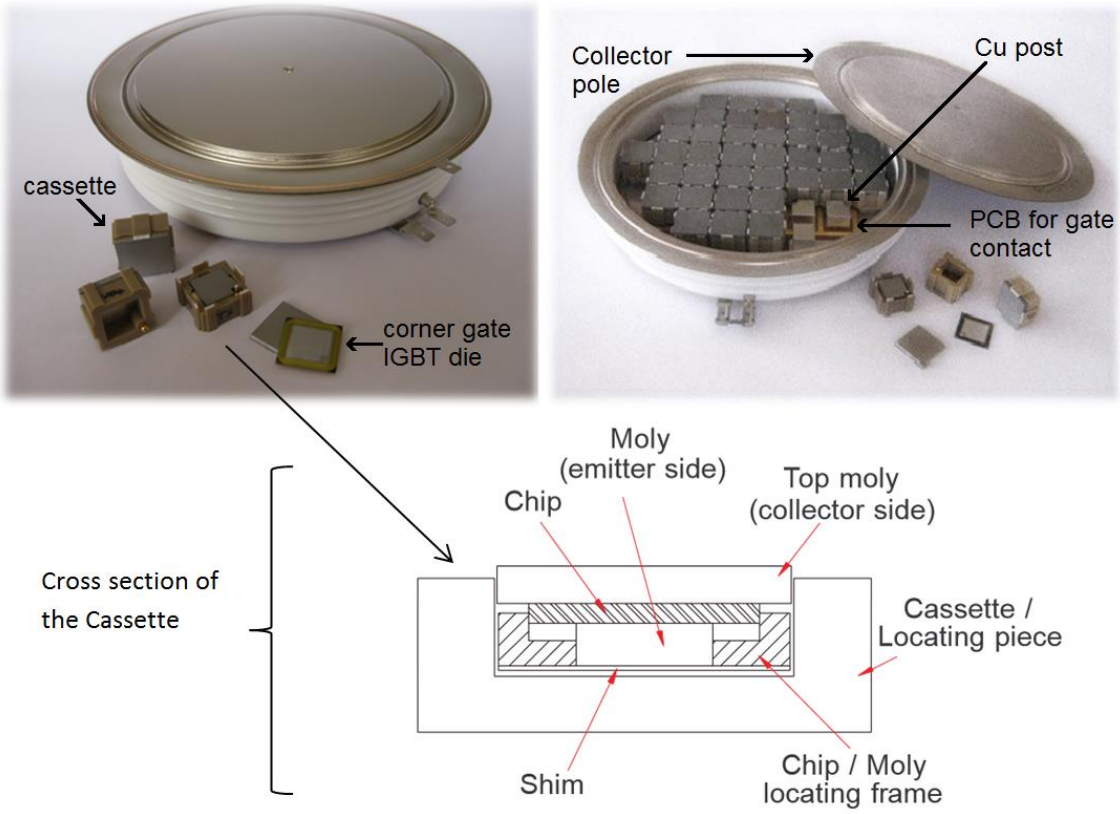


Figure 19: Press-Pack IGBT introduced by IXYS UK Westcode Ltd [47, 52].

Regarding its abilities for a failure to stable short circuit there is no published literature except, the manufacturer claims that in the press pack thyristor and GTO the failure mechanism is a failure to short circuit and as the PPI also utilises the same packaging therefore it is highly likely that it will also fail to short circuit but does not give a guarantee that the contact resistance of the failed device will be comparable to the device in normal operation [53]. Besides that there is no publication from the manufacturer where it has been investigated. A study was carried out by ABB for which they have filed a patent [54]. This indicates that in the case of press pack thyristor, the large Si disc is normally sandwiched between two Mo discs and when failure happens, the Si melts first as its melting point is less than Mo and as current

continues to pass, Si melts forming a conducting channel which spreads throughout the cross-section. In the absence of the oxygen (in a hermetically sealed package), the Si reacts with Mo to form a type of non-conductive powder and the process continues until all Si has been consumed which may last for years [54].

It should be noticed that in thyristors, the physical size of the Si disc is much larger than the physical size of an IGBT die. Hence there is a fair chance that the PPI would not last too long before all the Si is consumed to form powder after reacting with the Mo shims.

2.3.1 StakPak IGBT module

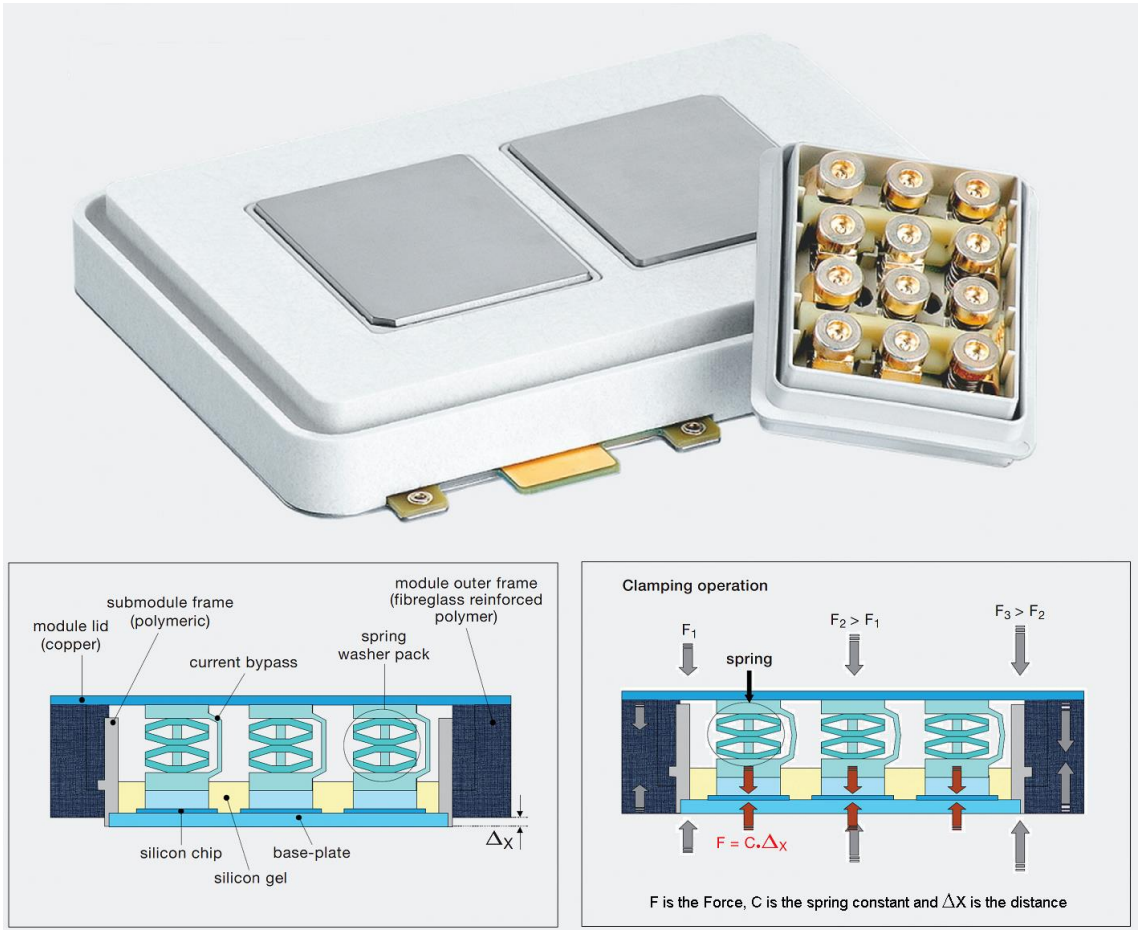


Figure 20: StakPak IGBT manufactured by ABB [55].

Another packaging technology for PPI was introduced by ABB called StakPak. Figure 20 shows the StakPak IGBT module in which the individual dies are packaged with a spring on top called the "press pin". When the module is clamped, each press pin experiences a force $F = c.\Delta x$ where c is spring constant and Δx is the distance travelled by the spring. The non-uniform distribution of the force on different press pins will result in different distances travelled by the spring and any surplus force exceeding the sum of all the forces on individual press pins will be absorbed by the rigid frame. Hence any asymmetry in the design can be normalised by the press pins resulting in a uniform distribution of pressure on an individual die without worrying about the flatness and tolerance issues [55].

Figure 21 presents the cross-section of one single chip. The construction of the module starts with soldering the die on the Mo baseplate on top of which an Al/Ag platelet is placed and then a bevel washer based spring is placed on top of it. The baseplate offers the collector connection to the device whereas the electrical connection of the emitter is not through the spring rather a current bypass is used (Figure 20) to ensure the rigid connectivity. The gate connection is made by a spring contact which is placed on top of gate terminal of each chip [55].

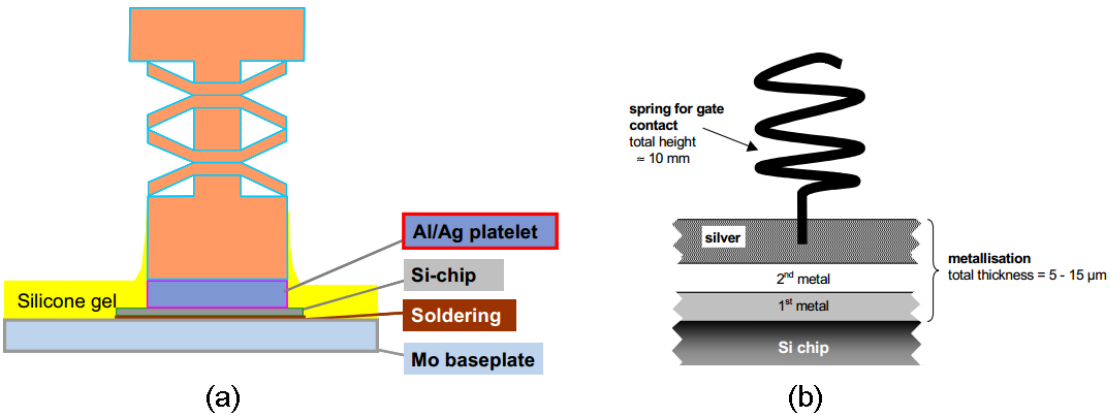


Figure 21: (a) Contact system for one single chip, (b) Direct pressure contact on gate [55].

As the module offers SCFM, it has been reported that there are two reliability issues associated with it. One is the reliability of module in the normal operation or intermittent operation life (IOL) and the other is the reliability/stability of the short circuit after the device has failed (SCFM life). These two requirements are detrimental to each other i.e. the module can either have improved power cycling capability or ability to sustain a low contact resistance after failure for a long time. It has been proposed that these two reliability issues can be tailored by selection of appropriate material in the press pin depending on different applications [56, 57].

The materials which facilitate the SCFM also have CTE larger than the Si. Hence, during the normal operation of the device, the temperature cycling causes thermo-mechanical fatigue and causes fretting due to CTE mismatch between Si and the intermediate material platelet which decreases the normal operational lifespan of the module [54]. From a reliability perspective the module can be customized for applications which require SCFM ability or longer IOL life. It has been reported that during the power cycling of a module designed for long SCFM life, the numbers of cycles in IOL were 100,000 when the module was subjected to cyclic junction temperature range of 40°C. On the other hand, the module which was tailored to achieve high IOL (reduced SCFM life) could achieve about one million cycles for similar conditions [56]. However, it should be noted that it is still less than a wirebonded module where over two million cycles can be easily achieved for similar conditions [58].

Experiments were conducted on StakPak modules by the manufacturer to further investigate the mechanism of SCFM where a single chip in the module was first subjected to over voltage breakdown followed by 1000-1500A which was passed through the sub-module for several hundred hours to observe the stability of the

SCFM. The voltage drop across the sub-modules was in the region of 300 – 700mV @ 1500A for majority of its lifetime until it fails to open circuit. However, the time it takes to become an open circuit has not been mentioned. The cross-section of the failed to short circuit sub-module indicated the formation of a conducting alloy between the Mo, Al, Si and PbSn. The samples which were observed during the early stage of current passage test indicated the formation of a hyper-eutectic alloy between Al-Si (16 wt. % Si in Al). In the intermediate stage of current passage test, the major portion of the conducting channel was composed of Mo 32%, Si 53% and Al 15%. The sample also indicated the formation of long cracks in the Mo baseplate due to the reaction of molten Al with Mo, which further increased the electrical contact resistance resulting in more heat dissipation and oxidation which further accelerated the crack formation and finally resulted into an open circuit [57].

The procedure adopted to conduct the abovementioned experiments for SCFM analysis does not account for the presence of a decoupling capacitor or DC link capacitor in the circuit which is almost always present in real industrial applications and can play a vital part in achieving SCFM. When the module fails, all the energy stored in the capacitor is dissipated in the module in a very short time interval causing the formation of arcing/plasma consequently leading to formation of very high temperature which causes vaporisation of various materials forming gases which eventually results in explosion of the module. Therefore, the way the module failures have been simulated, is actually quite different from what the module faces in a real industrial application.

Another mechanism of open circuit failure which has been reported is due to the silicone gel. In order to support high voltages, these modules are filled with the dielectric silicone gel which creeps slowly into the interface between the Si die and

spring contact. When a high temperature is generated during the SCFM, the silicone gel is converted into silica due to oxidation and high temperature. This formation of a hard layer of silica further increases the contact resistance and eventual failure to an open circuit [56].

Although it has been reported that the stable SCFM is highly likely to be achieved by using soft metals like Al but no detail has been published about the effect of using other materials on SCFM. Hence there is a need to explore different material systems which can find even better trade-off between extended life after SCFM and IOL.

In addition to the above problems associated with performance and reliability, it is reasonable to say that the manufacturing process is quite complicated and expensive. Another possible problem can arise during potting of silicone gel in unclamped module. After potting silicone gel, the module is normally placed in vacuum to extract the air bubbles out. As in the unclamped state, there can be low pressure exerted by the spring over the device. This can allow the penetration of small amount of gel into the contact interface causing increased contact resistance. Also the thermal path on the top side of the module shows that the thermal conduction is the complex function of displacement of the spring through which the thermal path is established. This implies that the thermal design would be complicated to compute and accurately estimate the junction temperature of the device.

2.4 Summary

Several interconnect technologies have been proposed and investigated to improve the electro-thermal performance who offer various advantages amongst each other. As a whole increasing the contact/conducting areas, thermal mass and introducing mechanical constraint in the interconnect technology can increase the ability of a

power module to handle higher power density and dissipate more heating. This may provide guidance or clues for the development of an innovative IGBT power module to favour SCFM.

There are only two commercially available IGBT power modules which claimed to have SCFM. Both of them are very complicated in mechanical structure and in manufacturing process. Except for the SCFM which has not been fully verified, the reliability of both of them needed to be improved and the selection of materials and the failure mechanism and its dependence on the pressure constraint needs to be further investigated

3 FAILURE MODES OF WIREBONDED IGBT TEST VEHICLE

3.1 Introduction

To determine how to design an IGBT module with a dominant stable SCFM, the starting point is to investigate the modes of failure of a conventionally packaged power IGBT module. For a better understanding of this investigation and instead of destroying the whole IGBT module which has a very complex structure, a simplified version of a conventional IGBT module has been implemented called the test vehicle which is shown in Figure 22. The test vehicle comprises of a single IGBT device attached to a direct bonded copper (DBC) substrate and wirebonds. Whereas in a conventional IGBT module there can be several substrates containing multiple devices connected in parallel using wirebonds.

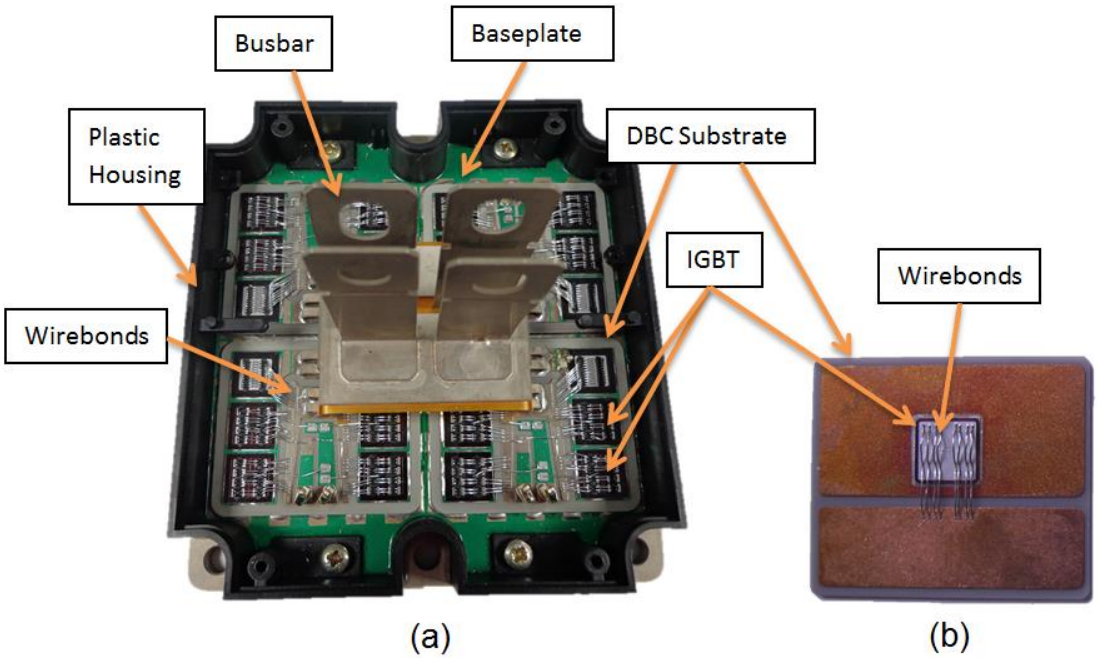


Figure 22: (a) shows the full IGBT module (b) Simplified wirebonded IGBT test vehicle

3.2 Experiment

The Type-II short circuit failure test is carried to evaluate the failure mode of the test vehicle. It is a destructive test in which a test vehicle is connected across a pre-charged capacitor bank whose stored energy can be varied by charging it to various voltage levels. The test vehicle is triggered by using a gate drive which turns on an IGBT. After turn on, the IGBT goes into saturation region, where the collector current reaches its maximum value and stays there until the junction temperature of the device exceeds its intrinsic or thermal limits after which the device brakes down followed by a sudden influx of current from the capacitor bank. The current through and the voltage across the device are recorded on the oscilloscope by using rogowski coil and high voltage differential probe respectively. Once the device fails, the judgement on OCFM or SCFM is made by measuring the collector to emitter contact resistance of the failed device by using high current power supply. The first step of the experiment is the sample preparation which is discussed in the following section.

3.2.1 Sample Preparation

The test vehicles were constructed using Alumina based Direct Bonded Copper or DBC substrate. The substrate had two copper islands on one side and which can be seen in Figure 23 (a). The power semiconductor devices used in the preparation of the samples were the 13.5mm X 13.5mm 1700V/50A centre gate IGBT having Al metallization on the emitter side (top side) and ~0.1/1/1 μm Ti/Ni/Ag finish on the collector side. These IGBT were made by Dynex Semiconductor Ltd.

In total, 10 test vehicles were constructed to study the failure mode in the wirebonded IGBTs. The test vehicles were constructed using the following steps:

1. The DBC substrates were cleaned first by using plasma cleaner to get rid of any organic coatings and oxides.
2. A mask was made out of 100um thick Aluminium foil to deposit solder paste as shown in Figure 23(b).

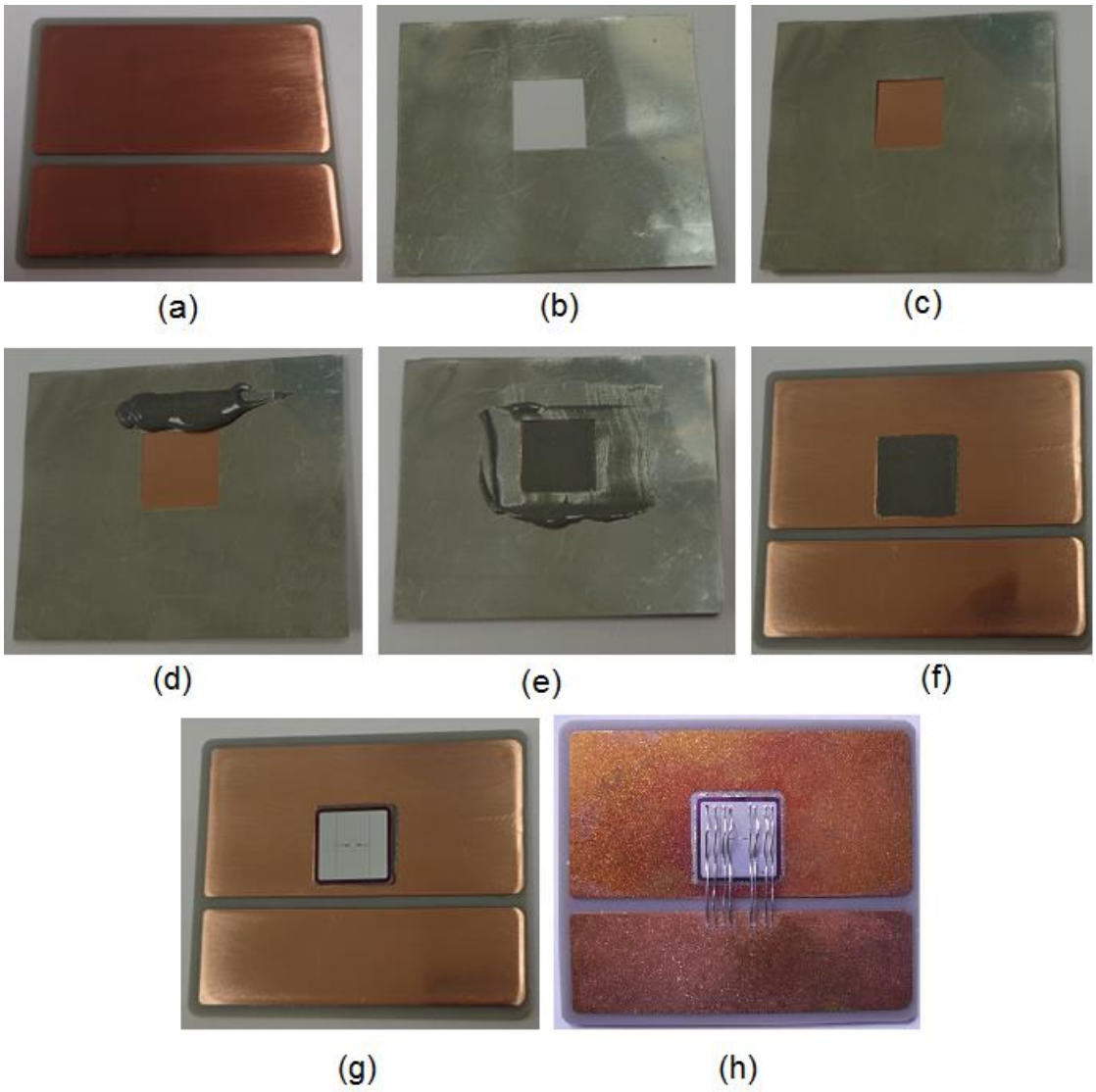


Figure 23: Sample preparation (a) two island DBC substrate (b) Aluminium mask (c) Mask placed on the substrate (d) Solder paste applied to the mask (e) Solder paste spread using squeegee (f) mask removed from the substrate (g) IGBT placed over the solder paste (h) finished test vehicle after passing through reflow oven and wirebonding process.

3. The mask was placed on the DBC substrate and the solder paste was applied to the DBC by using a squeegee as shown in Figure 23 (c), (d), (e) and (f).
4. The IGBT die was placed on top of the solder paste (Figure 23 g) and then was placed in the reflow oven. As the reflow was done in the presence of air, it caused oxidation of the DBC which was later removed by slightly warming the DBC to about 60°C and then applying the flux. This removal of the oxidation layer was essential for the next step which was wirebonding.
5. Wirebonding was done by using a standard 99.999% pure 375um diameter Al wire. Initially the parameters of the wirebonding equipment were slightly adjusted to get good bonds and then the wirebonding was performed on all 5 test vehicles using those parameters. A total of 17 bond pads on each die were implemented: 16 bond pads on the emitter area and one bond pad on the gate.

There were only two islands on the DBC, one island was used for the electrical contact to the collector of IGBT and one for the electrical contact of emitter of an IGBT. Therefore, the gate contact was taken out of the test vehicle using the same wire which was used to bond the gate of an IGBT. This wire was later connected to the gate drive unit. The finished test vehicle can be seen in the Figure 23 (h).

3.2.2 Setting up Test Rig

The schematic diagram and the actual test rig can be seen in the Figure 24 and the Figure 25 respectively.

The test rig was created by using a 0 to 400V variable power supply the output of which was connected to a capacitor bank which contained 9 X 6800uF 400V aluminium electrolyte capacitors connected in parallel. An anti-parallel diode was connected across it as a free wheel diode. The positive terminal of the capacitor bank was connected to the collector terminal of the test vehicle while the negative terminal

of the capacitor bank was connected to the emitter terminal. The test rig except the power supply was placed inside polycarbonate enclosure for safety reasons during destructive testing.

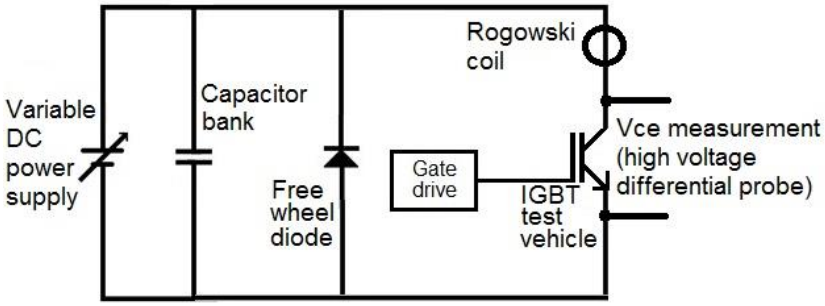


Figure 24: Schematic diagram of test rig

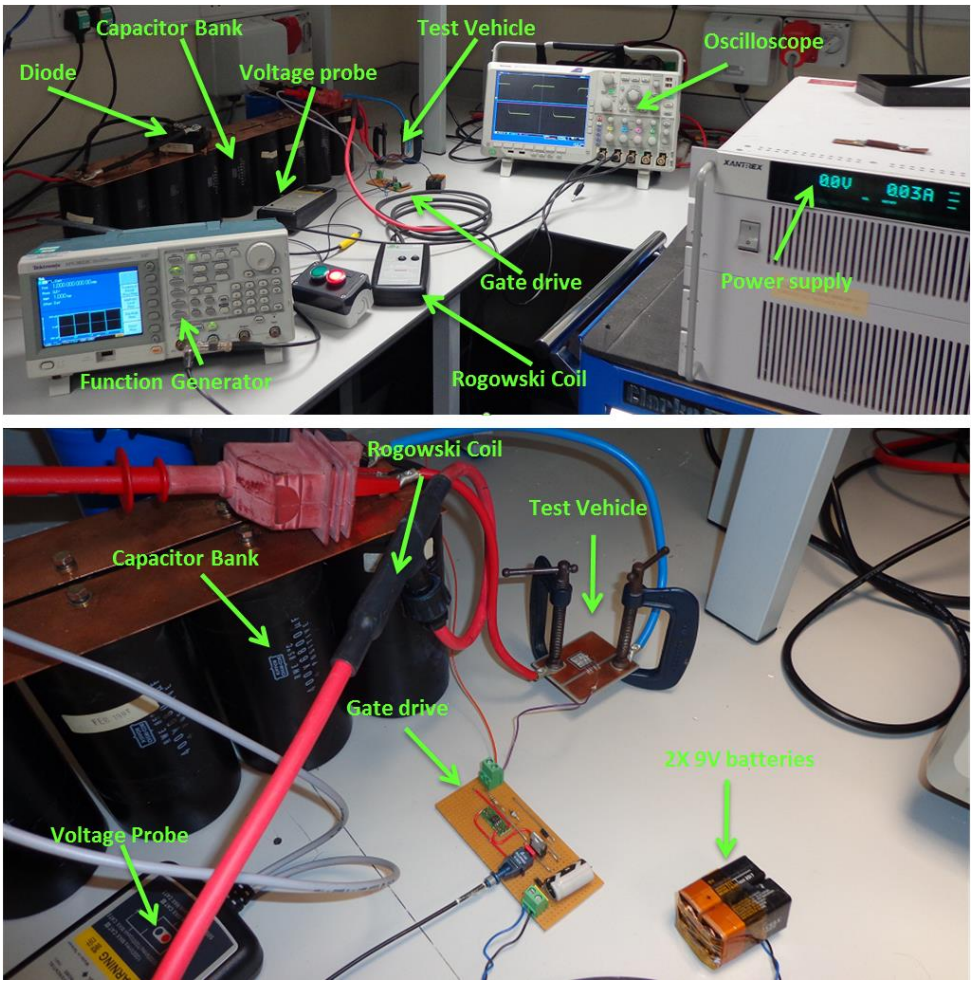


Figure 25: The Test Rig

To turn on the IGBT, a robust gate drive unit was also designed. Its schematic diagram can be seen in Figure 26. The presence of the diode on the output to the gate terminal actually protects the gate drive unit from destruction during the device failure. The gate drive receives its power from two series connected 9V batteries. The IR4426 is an H-Bridge driver which produces +18V at OUTA terminal when the fibre optic receiver receives light signal otherwise it outputs -18V. A function generator has been used to generate a square shaped pulse which is converted to a light signal by using the fibre optic transmitter. The fibre optic cable has been used to connect the output of the transmitter to the input of the gate drive receiver.

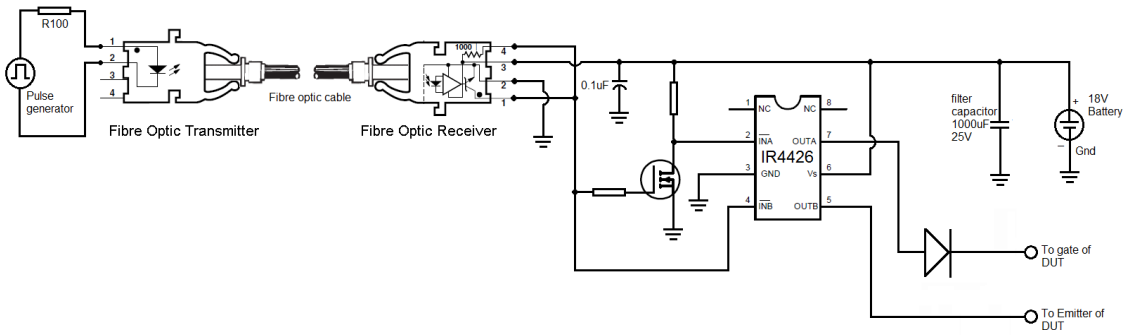


Figure 26: Gate Drive Unit

3.2.3 Principal of Testing

3.2.3.1 Estimation of Realistic Energy Levels Involved in the Explosion

In a typical real industrial application say a voltage source dc to dc converter, the energy from the mains is stored locally in the capacitor bank before delivering it to the IGBT. This capacitor is commonly known as a filter, line or DC link capacitor. The value of this capacitor depends upon the application and can be in range starting from a few μF to Farads. For an inverter, operating at 1300V having a DC link capacitor of 24 mF, the total energy stored in the system would be

$$E = {}^{1}/_{2}\, CV^2 = {}^{1}/_{2}\, 24e^{-3}1300^2 = 20.3\ kJoules.$$

This amount of energy can be considered as a realistic amount of energy that the IGBT power module will face in real industrial applications. If this amount of energy gets dissipated in IGBT power module, it can cause explosion of the module with ejection of shrapnel [4]. If an IGBT power module is of 1500A containing 30 IGBT dies (50A each) connected in parallel this implies that there would be about 680 Joules of energy per device if the module fails uniformly. Hence for our test vehicle which contains only one IGBT device, the stored energy of about 750 J can be safely advised as a benchmark for the destructive testing. This value has been increased from 680 J to 750 J to compensate for the energy dissipation in the equivalent series resistance (ESR) and in copper busbar connections.

3.2.3.2 Test Procedure

The test vehicle was connected to the test rig. A high voltage differential probe was connected across the device to measure the voltage across it and a rogowski current probe was also connected to measure the current. The oscilloscope was triggered by using an auxiliary output of the function generator. The 61.2mF capacitor bank was charged at different voltage levels to produce different level of energy pulses which started from 10 J up to 750 J for different test vehicles.

For example, to carry out test at 750 J, the capacitor bank was charged up to 156V, after charging the capacitor bank, the square shaped pulse was applied to the gate of the IGBT, the device turned on and it stayed on until all the energy from the capacitor bank passed through the device which induced the thermal overload failure. The same procedure was repeated for all the test vehicles but at different energy levels.

Due to the nature of this experiment the explosion causes the emission of shrapnel and a loud bang. To deal with these issues, further to putting a polycarbonate enclosure

around the test rig, ear defenders and the safety glasses were also used to protect against personal injury.

3.3 Experimental Results

3.3.1 Electrical Testing

The first test vehicle was tested at 750 Joules which resulted in the evaporation of all wirebonds i.e. OCFM. For the rest of the test vehicles, the energy level was subsequently reduced from previous experimental value until SCFM was observed.

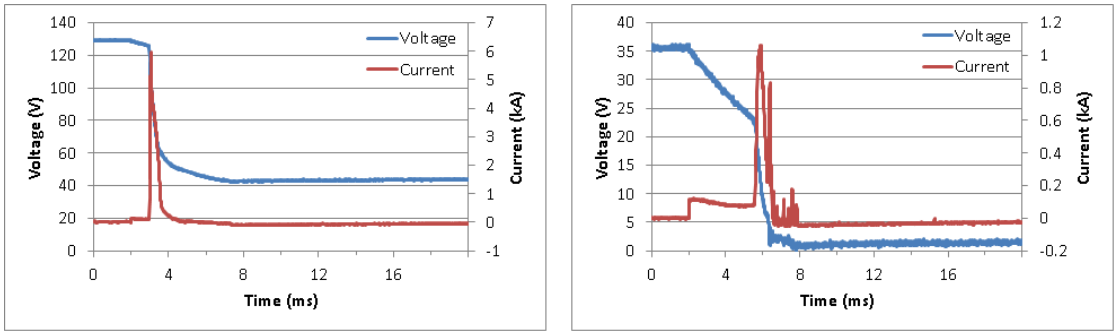


Figure 27: Voltage and current waveforms of wirebond based test vehicle (a) achieved OCFM at 500J (b) achieved SCFM at 62.5 J.

The electric current and voltage through and across the device respectively can be seen in Figure 27. The graph on the left hand side is of the test vehicle which resulted in the OCFM at 500J whereas the graph on the right hand side corresponds to the test vehicle which achieved SCFM at 62.5J. The results from the explosion testing of wirebonded test sample can be summarised in Table 1.

Energy (J)	Voltage (V)	Peak Current (A)	Saturation time (ms)	Failure Mode	Number of Samples tested
750	156	-	-	OCFM	1
500	128	6000	1	OCFM	1
250	90	1800	5	OCFM	3
125	63	600	7.5	OCFM	2
62.5	45	1100	2.8	SCFM	3

Table 1: Summary of results from wirebond based test samples.

3.3.1.1 High Speed Imaging

To develop understanding about dynamics of mechanical deformation of wirebonds and structure of IGBT die during explosion testing, a high speed camera (PHANTOM v12.1) was used. The setup can be seen in Figure 28. To save the lens of camera from the shrapnel of exploding IGBT, an enclosure made of polycarbonate was used.

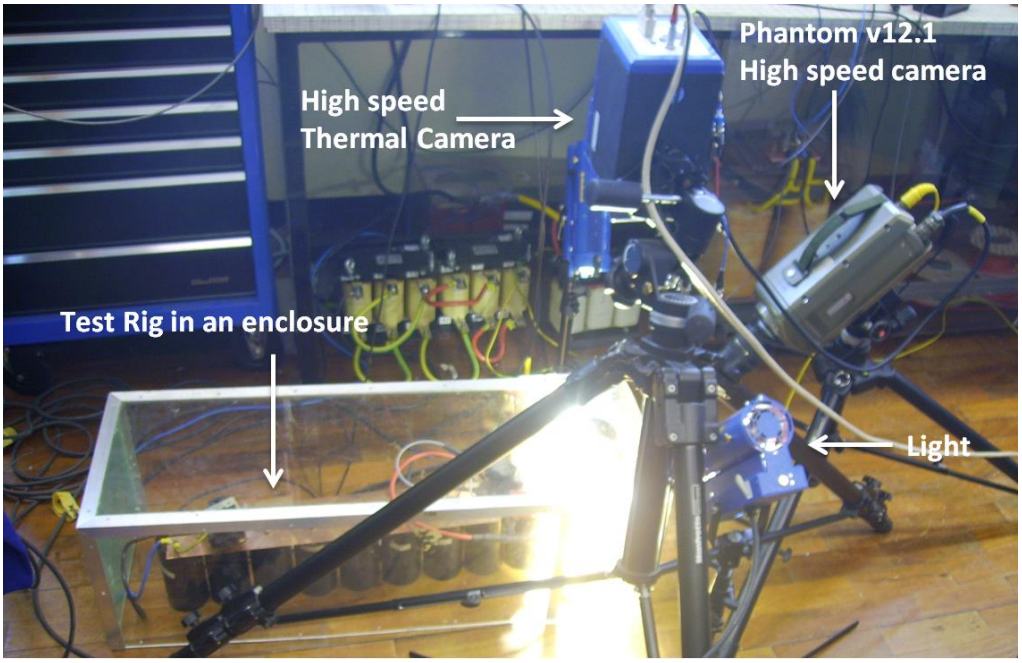


Figure 28: Setup for high speed camera

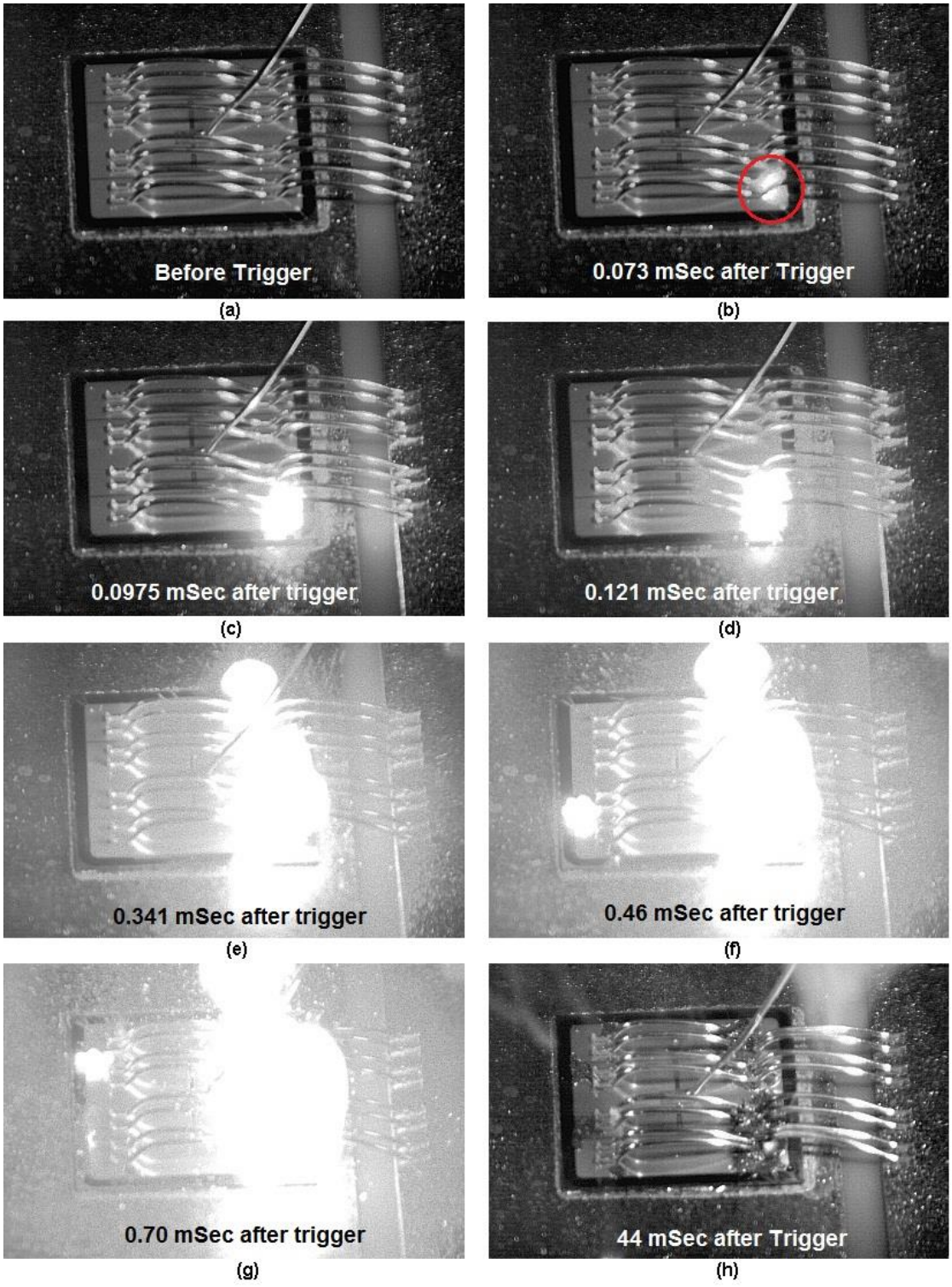


Figure 29: High speed imaging of exploding IGBT die in a sequence from (a) to (h)

To overcome the saturation problem, both the auto exposure and Extreme Dynamic Range (EDR) functions of the camera were used. The camera was triggered synchronously with the gate signal of the IGBT. Several test vehicles were destroyed at different energy levels (starting at 750J) to capture the exploding device at high speed but unfortunately resulted in the saturation of CMOS sensor of the camera. At 62.5J the intensity of the light during explosion was low enough to capture the high speed video. The video was recorded with 41.025kFPS (kilo frames per second). The most important frames of the video can be seen in Figure 29.

Initiation of an arc can be seen in Figure 29(b) underneath the wirebond highlighted inside the red circle which suggests that the wirebond was initially disconnected by melting. This single wirebond i.e. wirebond no. 1 is presumed to carry maximum current as it offers lowest impedance to current path, shown in Figure 30.

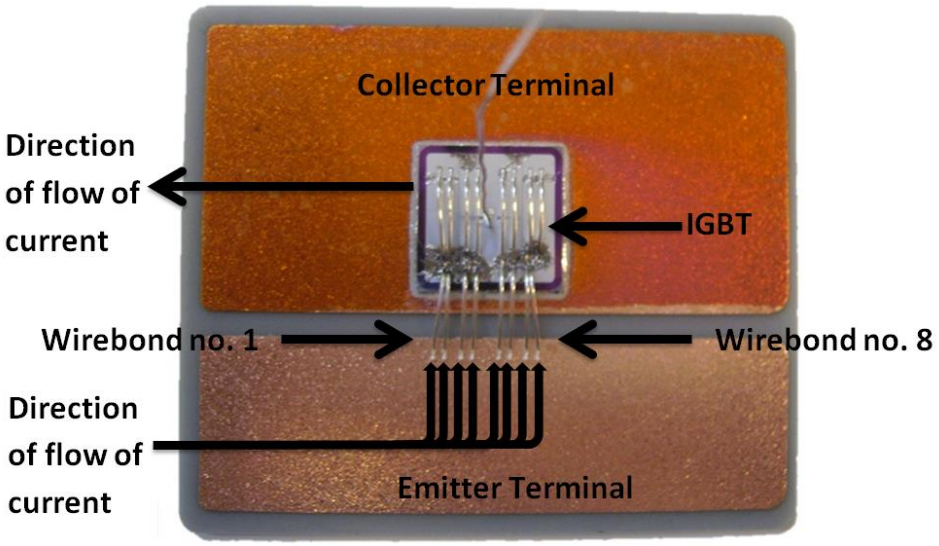


Figure 30: Current path on DBC

3.3.1.2 Maxwell Simulation for Current Density

The simulation was carried out using the Ansoft Maxwell 3D software to plot the current density in the wirebonded test vehicle. A simplified model of the test vehicle

was made using SolidWorks software and its geometry was imported into Ansoft Maxwell 3D, the model can be seen in Figure 31.

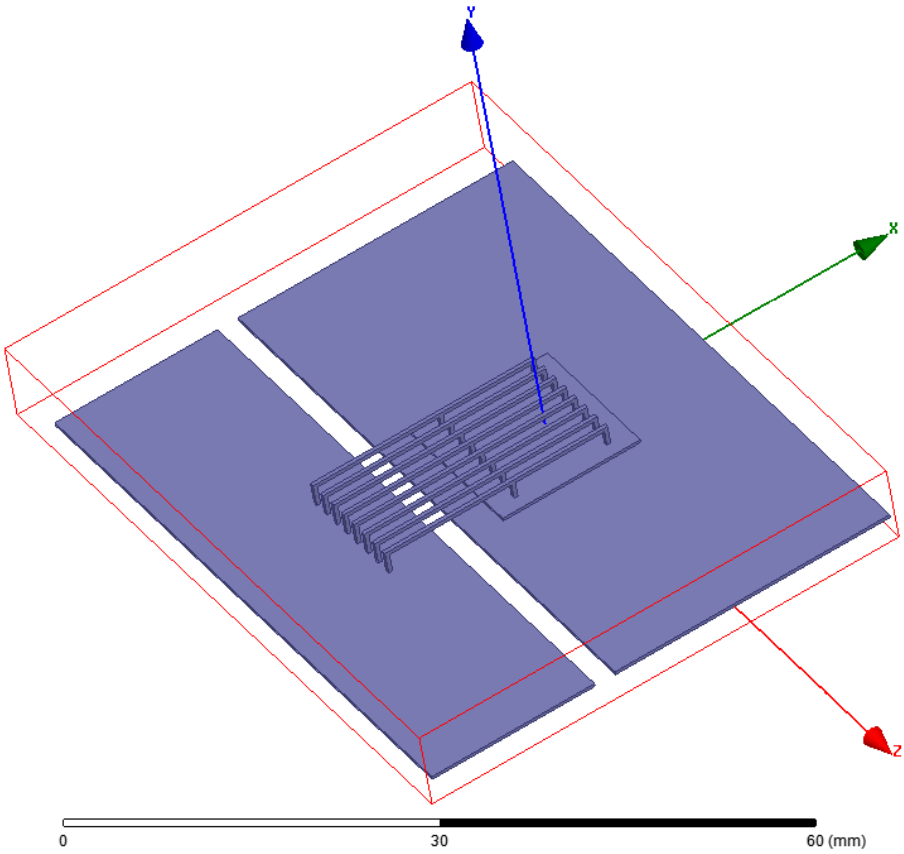


Figure 31: Simplified model of wirebonded test vehicle

Material	Bulk Conductivity (Siemens/meter)	Relative Permeability
Aluminium (wirebonds)	38000000	1.000021
Copper (substrate)	58000000	0.999991
Silicon to conductor (IGBT Die)	57000000	1
Vacuum	0	1

Table 2: List and property of materials used in the simulation

The list of the materials used in the simulation are presented in Table 2. Current conducting IGBT has been represented with Silicon to conductor. The mesh and the excitation faces are shown in Figure 32. 6000A of current signal was applied and the direction of the current flow is presented with the direction of arrows where the "Current 1" represents current going into the substrate and the "Current 2" represents current coming out of the substrate.

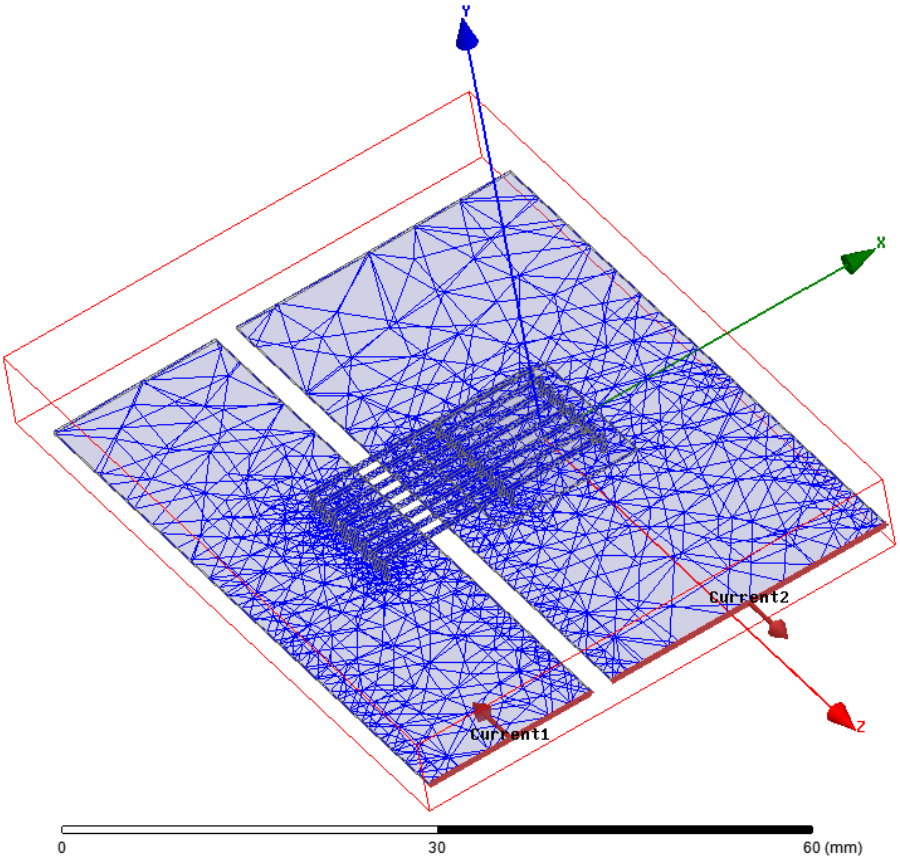


Figure 32: Mesh plot along with faces where current signal is applied

Figure 33 shows the current density plot whereas enlarged view of wirebonds is shown in circle. It should be noticed here that the wirebond no. 1 has carried most of the current as compared to the others resulted in the rapid rise of its temperature causing it to melt at the points where contact resistance was higher. This disrupted the path of the current flow causing formation of arc. The emergence of an arc can be seen under wirebond no. 1 shown in Figure 29(b) i.e. in the frame captured by high

speed camera. Then the rest of the wirebonds failed sequentially causing formation of an arc in a sequence from wirebond no.2 to wirebond no. 8 i.e. following the current density gradient calculated by the simulation. Hence the simulation result agrees with the experimental results.

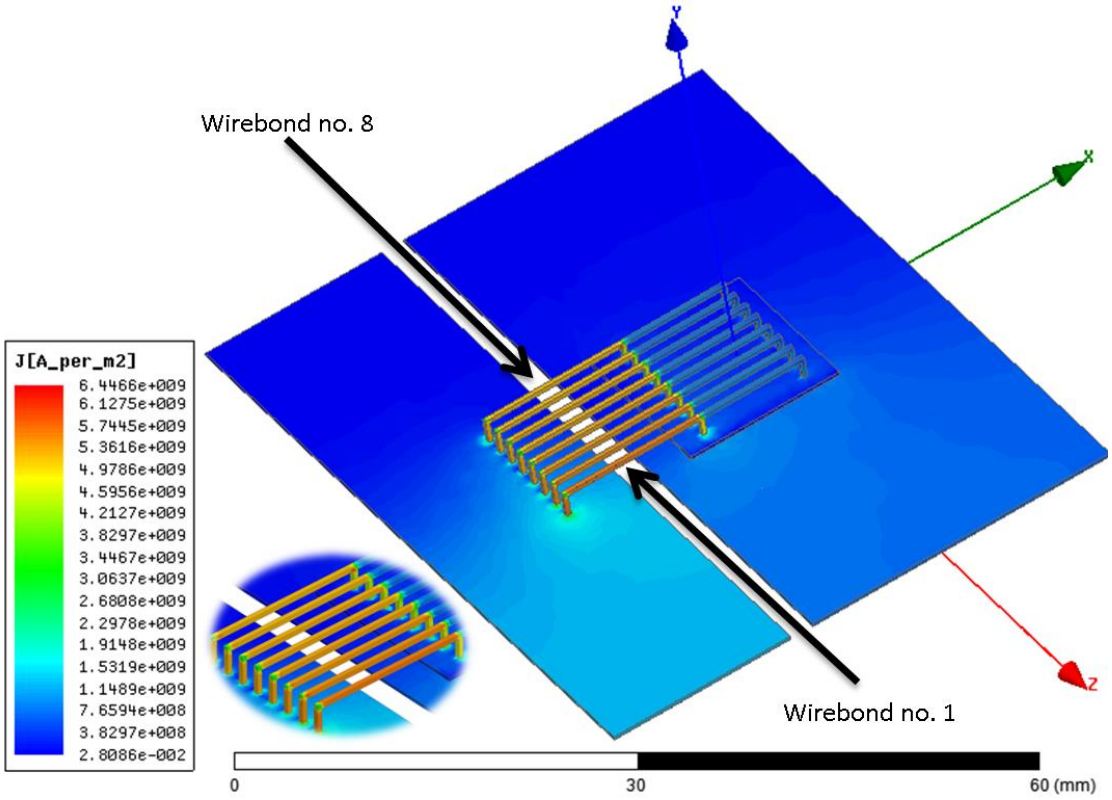


Figure 33: Current density plot

3.3.2 Microstructural Observation

For the microstructural observations, the failed samples were analysed under the scanning electron microscope (SEM) which had the built in stage for energy dispersive X-ray spectroscopy (EDX) to identify different materials. First, the test vehicles were analysed under the SEM to observe the topography and distribution of different materials on the surface of the device. The area of interest on the test samples was identified using initial topographical analysis and for further analysis of

the areas of interest, the test samples were cut using diamond saw and cross-sections and then they were moulded in an epoxy resin which was later grinded and polished using first 600 grit size SiC paper down to 1μm diamond suspension. These cross-sections were later analysed under the SEM.

Figure 34 shows the test vehicle after the explosion testing. Figure 34(a) is of the test vehicle which went OCFM at 500 Joules of energy whereas Figure 34 (b) is of test vehicle which went SCFM at 62.5 Joules.

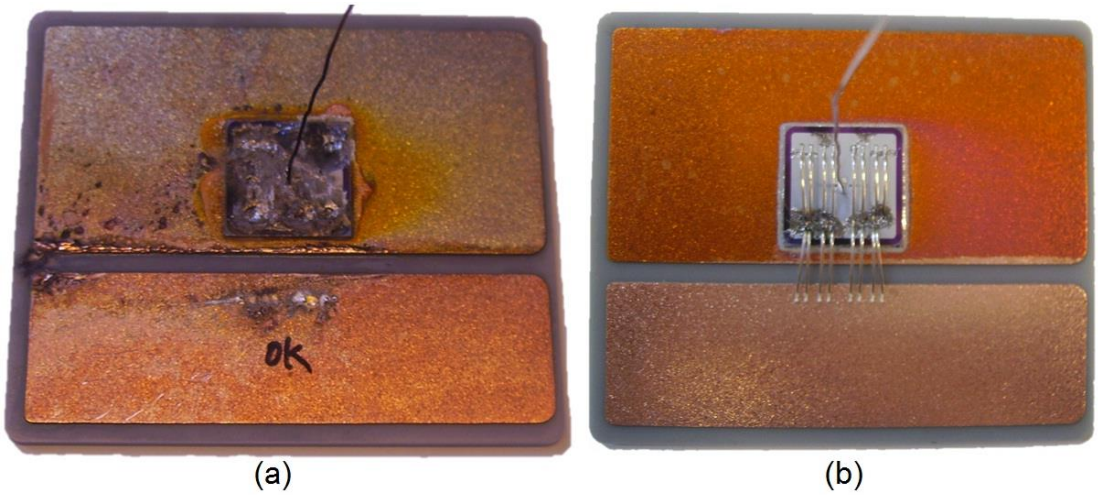


Figure 34: Test vehicles (a) achieved OCFM at 500J (b) achieved SCFM at 62.5J

3.3.2.1 Microstructural Observation of Failed to Open Circuit Test Vehicle

The cross section of the test vehicle that exploded at 500J was prepared and was observed under the Hitachi TM3000 Scanning Electron Microscope. The SEM images can be seen in Figure 35.

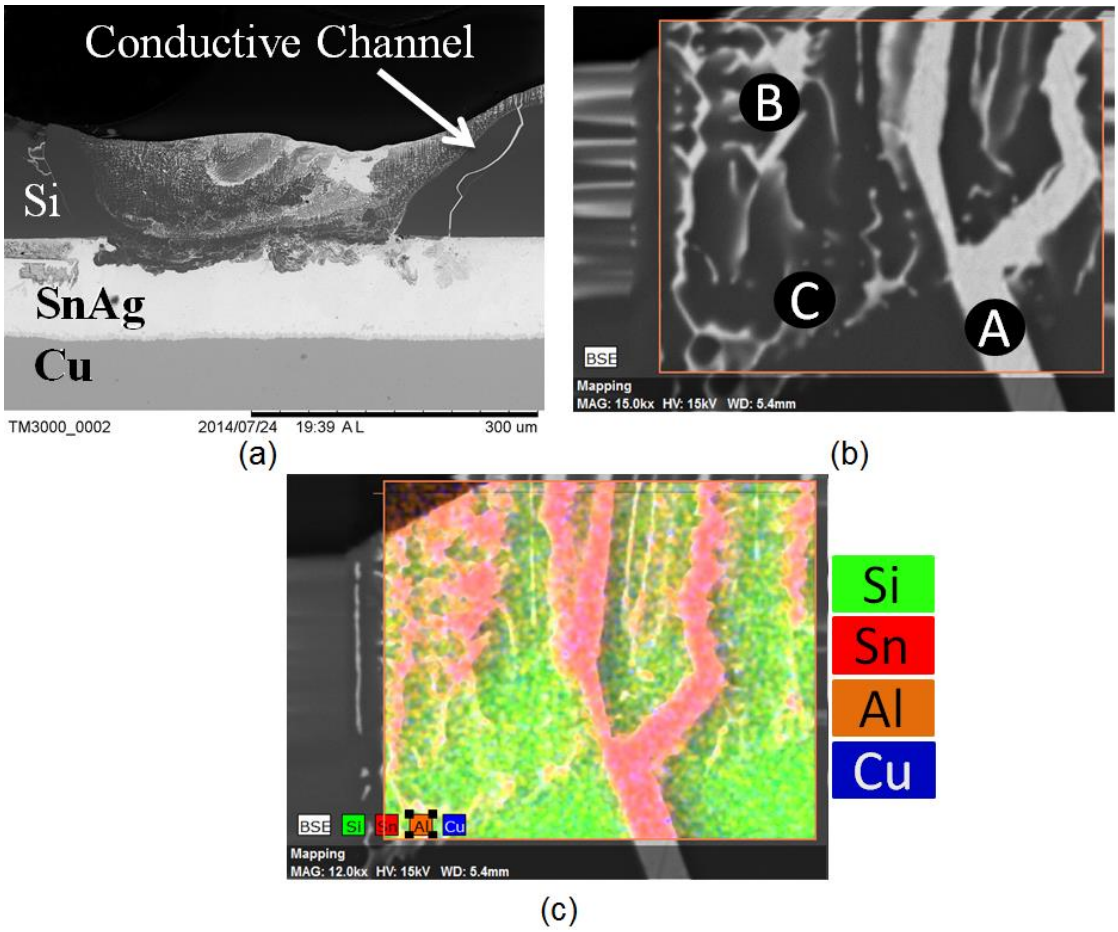


Figure 35: SEM images of cross-section of the test vehicle which achieved OCFM (a) conductive channel, (b) EDX points and (c) EDX element map.

Figure 35 shows the solidification structure, which resulted from the rapid solidification of the molten mixture of various materials such as Si, Al, Sn and Cu. The composition of the material is presented in atomic percentage (at%). The composition of the materials at point A is Sn 37 at%, Si 53 at%, Al 6 at% and Cu 2 at%. The composition of the materials at point B is Sn 22 at%, Si 71 at%, Al 4 at% and Cu 1 at%. The composition of the materials at point C is Sn 5 at%, Si 90 at%, Al 1 at% and Cu 1 at%. The dark phase in Figure 35 (a) and (b) is Si which has low electrical conductivity compared to the bright phase e.g. Sn and Al which has higher electrical conductivity. Hence the bright phase shows the conductive channels which in this case are largely tin based.

3.3.2.2 Microstructural Observation of Failed to Short Circuit Test Vehicle

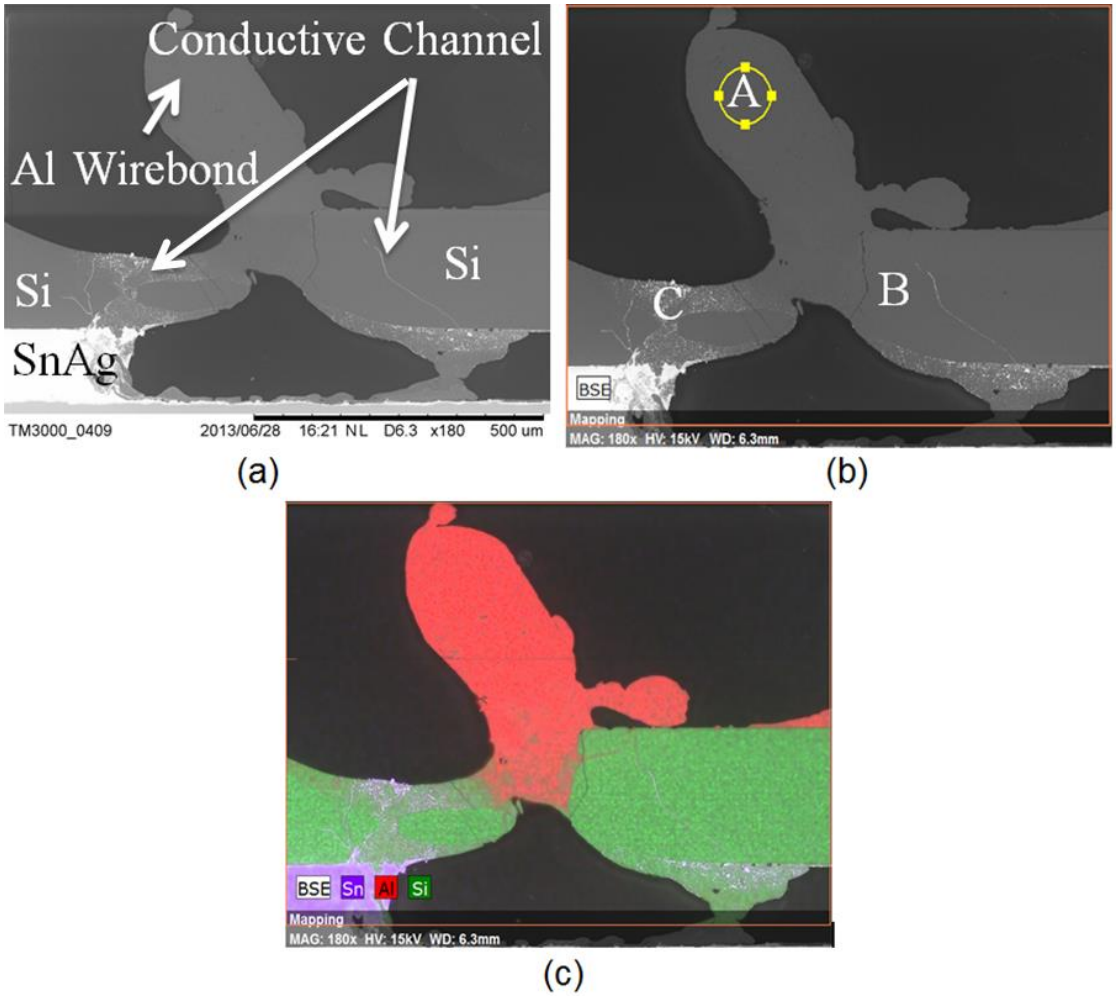


Figure 36: SEM images of cross-section of the test vehicle which achieved SCFM (a) shows the conductive channel (b) shows location of EDX points A B & C (c) EDX element map

The cross section of the test vehicle that exploded at 62.5J was prepared and observed. The SEM images can be shown in Figure 36. In Figure 36 we can see that wirebond is still in contact with the top of the device and underneath the wirebond we can see the formation of solidification structure (bright phase) which is electrically conductive. The composition of the materials at point A is Al 96 at% and Si 4 at%. The

composition of the materials at point B is Si 97 at% and Al 3 at%. The composition of the materials at point C is Si 90 at%, Al 7 at% and Sn 3 at%.

3.4 Discussion

From these experiments it can be concluded that the amount of energy involved during the failure of the device plays a vital role in defining whether the device is going to OCFM or SCFM. The threshold level of the energy has been identified which is in the region from 62.5 J to < 125 J that causes the test vehicle to achieve SCFM. The lower energy threshold level i.e. 62.5J which resulted in SCFM has been verified by repeating the experiment three times. The upper threshold level was identified by repeating the experiment two times. This wide error range could be reduced by performing the test at various energy levels in between said range but as it is very time/resource consuming process to carry out test, therefore it has not been investigated. Beyond 125 J of energy the wirebonds act as fuse wires and hence they vaporise achieving OCFM which has been verified by three times repetition of experiment at 250 J.

From the cross-section microstructural observation it has been identified that there was formation of conductive channels during the test. From the EDX of these channels it was identified that these channels which are bright phases were conductive because of the presence of high percentage of Sn which came from the SnAg solder used to attach the IGBT die to the substrate. These conductive channels were present both in the test vehicle which failed to open circuit and short circuit. The only difference between the two test vehicles was that the wirebonds stayed in contact in the test vehicle which achieved SCFM during the test carried out at low energy

whereas it vaporised in the test vehicle which achieved OCFM during the test carried out at high energy.

In the case of test vehicle which achieved SCFM, the conductive white phase in the test vehicle had good contact with the residual wire bond and the solder under the Si device. They together form the conductive path to carry the current after the failure test.

3.5 Summary

The wirebonded devices can fail both into a short or open circuit. The SCFM can only be achieved at relatively low energy level which in this case was 62.5J. In the real industrial applications it is highly unlikely that the IGBT module will be subject to low level of energy, per device, during failure. Therefore, it is highly likely that it will fail into an OCFM.

For wirebonded test vehicles, the failure to a short circuit happens only at low energy level, the next question that arises is what can be done to increase that energy level? One possible solution is to increase the thermal mass on the device because if the thermal mass is high, it will take a larger amount of energy to raise the temperature of the device and interconnects to the temperature at which materials undergo bulk vaporisation. The thermal mass of the interconnect can be increased by putting more wirebonds on the device or by using a different interconnect technology. This is what has been investigated in the next chapter.

4 Failure Modes of Flexible PCB Interconnected IGBT Test Vehicles

4.1 Introduction

In the previous chapter tests were performed on the wirebonded IGBT test vehicles and it was noted that they fail to both open and short circuit depending upon energy level. In this chapter wirebonds have been replaced with a different interconnect technology i.e. flexible PCB and its short circuit performance have been tested at different energy levels.

4.2 Experiment

4.2.1 Flexible PCB

The top side of the device i.e. emitter contact has been connected to the electrical terminals by using a flexible printed circuit board which can be seen in Figure 37.

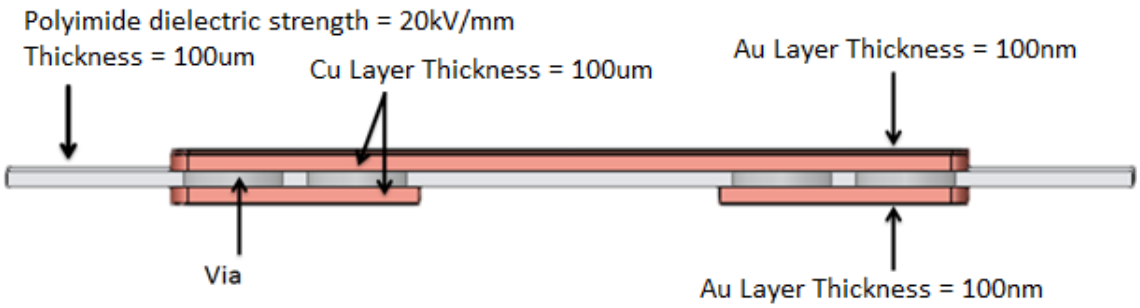


Figure 37: Flexible PCB

The flexible PCB contains three layers, the top layer is a 100um copper layer coated with 100nm Gold, the middle layer is polyimide, a flexible polymer with the thickness

of 100um and the bottom layer is again 100um Cu with 100nm Au coating. The thin Gold layer helps to produce a reliable sintered joint. As the dielectric strength of the polyimide is 20kV/mm, 100um thickness has been selected to support voltage up to approximately 2kV. One interesting feature is the "via" which connects the top side conductor with the bottom side conductor which can helps to provide a more degree of freedom to design the layout of power module.

Figure 38 shows a sheet of flexible PCB which contains different design patterns to accommodate a range of power semiconductor devices from different vendors.

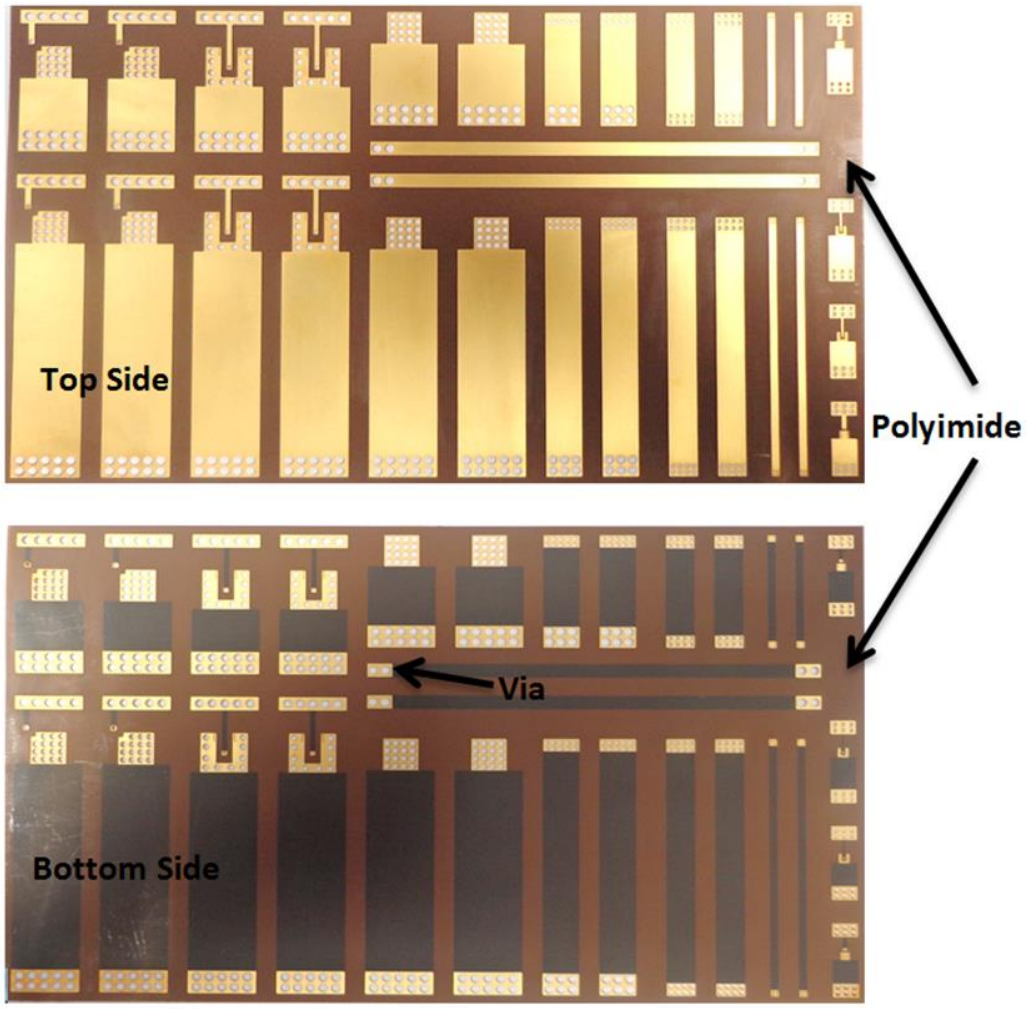


Figure 38: Flexible PCB for different type of devices

4.2.2 Sample Preparation

The top/emitter side metallization on the IGBT dies is normally aluminium alloy. The reason for that is to facilitate the wirebonding process by which Al wire is welded with the top Al layer of the device using ultrasonic bonding [59]. The presence of Al on the top also suggests that the device is not solder-able on the top because Al gets oxidised very quickly and hence always retains a thin layer of Aluminium Oxide which does not permit any other kind of bonding except ultrasonic bonding or welding.

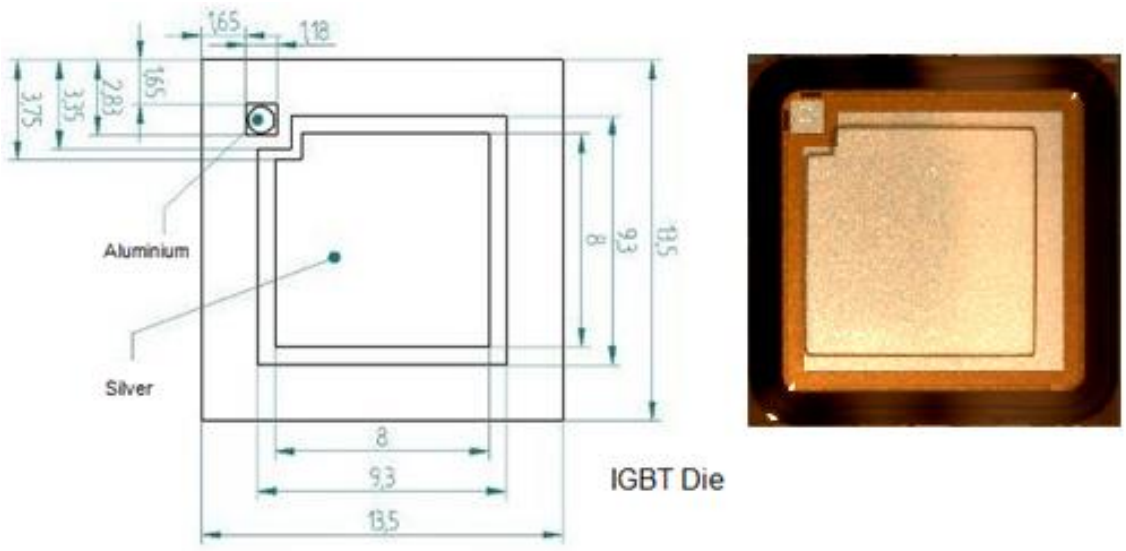


Figure 39: Silver top corner gate IGBT die (used in chapter 4 and chapter 5)

This implies that to change the interconnect technology from wirebonds to flexible PCB the top side metallisation has to be changed on the IGBT dies. Hence, the power semiconductor devices used in the preparation of the samples were the 13.5mm X 13.5mm 2500V/50A corner gate IGBT having ~0.5/0.1/1/1 μm Al/Ti/Ni/Ag metallization on the emitter side, ~0.5 μm Al metallization on gate pad and ~0.1/1/1 μm Ti/Ni/Ag metallization on the collector side. These IGBT were obtained from Dynex Semiconductor Ltd and can be seen in Figure 39 .

The test vehicles were constructed using Alumina based Direct Bonded Copper or DBC substrate i.e. the same substrate which has been used to construct wirebonded test vehicles. In total, five test vehicles were made to study the failure mode. The schematic diagram of the test vehicle can be seen in Figure 40.

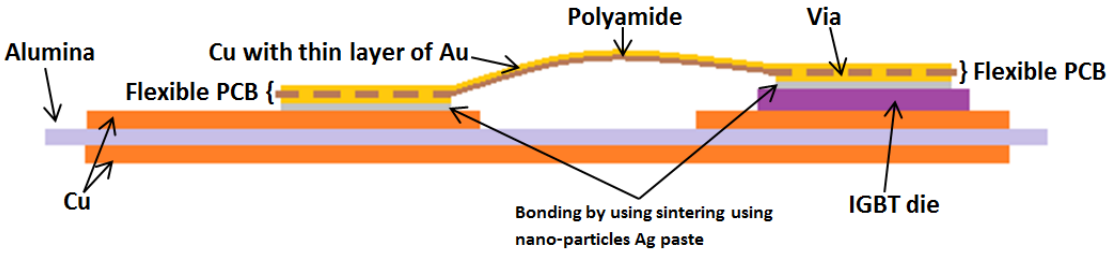


Figure 40: schematic diagram of the flexible PCB based test vehicle

The construction of the test vehicles was done using the following steps:

1. The DBC substrates were cleaned first by using plasma cleaners to get rid of any organic coatings and oxides.
2. A mask was made out of 100um thick Aluminium foil to deposit silver nano particle paste as shown in Figure 41 (b).
3. The mask was placed on the DBC substrate and the paste was applied to the DBC by using a squeegee as shown in Figure 41 (c), (d), (e).
4. The flexible PCB can be shown in Figure 41 (f). The silver paste was applied on its bottom side.
5. The substrate and flexible PCB was placed in an oven for about 30 minutes at 130 degree C to get rid of organic material inside the paste leaving a preform of pure silver nano particles.
6. The IGBT die was placed on top of the preform Figure 41 (g) and then flexible PCB was placed on top of the die Figure 41 (h).

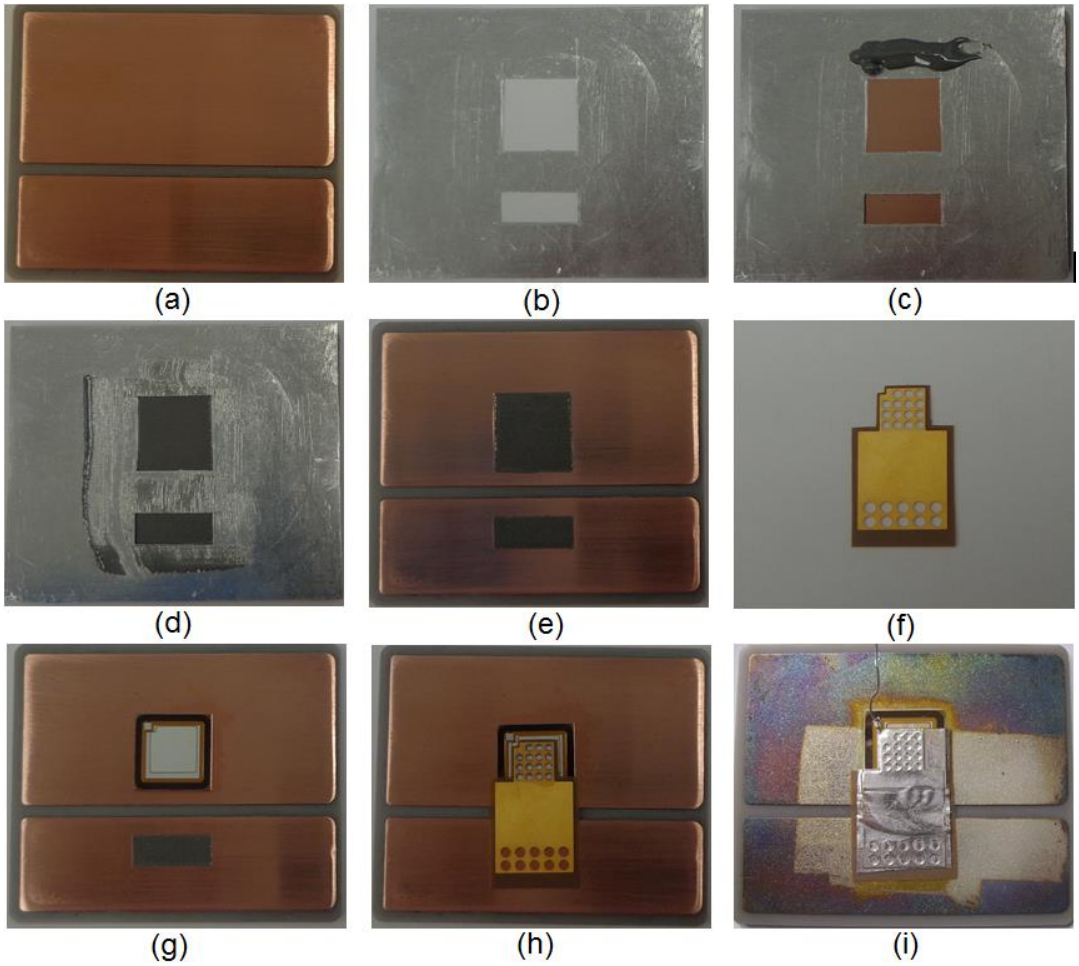


Figure 41: Sample preparation (a) two island DBC substrate (b) Aluminium mask (c) Mask placed on the substrate with silver paste applied to the mask (d) silver paste spread using squeegee (e) mask removed from the substrate (f) Flexible PCB (g) IGBT placed over the silver paste (h) flexible PCB placed on the IGBT and substrate (i) Final test vehicle after sintering and wirebonding gate contact.

7. The Al foil was placed on top of the flexible PCB to add some compliance during sintering process which can be seen in Figure 41 (i). A high temperature adhesive tape was applied on top of the Al foil to keep everything intact before placing it in the hydraulic press to simultaneously apply pressure and heat for sintering. The pressure, temperature and time profile for sintering process was recommended by

the silver paste manufacturer. Hence, the pressure applied was 5 MPa, temperature was 250 °C and time was 5 minutes to carry out sintering process.

8. After wirebonding the gate pad, the finished test vehicle can be seen in Figure 41 (i).

4.2.3 Test Procedure

It should be noted that the test rig was set up similarly to that described in section 3.2.2 and the test procedure was similar to the one being followed in section 3.2.3.2, except the first test vehicle was tested at 500 J; the others were tested at different energy levels depending upon the mode of failure. To find out the threshold energy level to attain SCFM, a simple procedure was adapted i.e. to keep reducing the energy level if the test resulted in OCFM, until it achieves SCFM.

4.3 Experimental Results

4.3.1 Electrical Testing

The first test vehicle was tested at 500 J which resulted in an OCFM. For the second test vehicle, the energy level was reduced to half the value at which first test vehicle was tested i.e. 250 J and was noticed that the test vehicle achieved SCFM. To find the threshold energy level to have an SCFM, the third test vehicle was tested at 375 J and it was noted that the test vehicle achieved OCFM. This implies that the energy required to have a SCFM was between 250 J and 375 J. The last test vehicle was tested at half way between 250 J and 350 J i.e. 312.5 J and it was noted that the test vehicle achieved SCFM.

The electric current and voltage through and across the device respectively can be seen in Figure 42. The graph on the left hand side is of the test vehicle which resulted

in OCFM at 500J whereas the graph on the right hand side corresponds to the test vehicle which achieved SCFM at 312.5 J. The double peak in current waveform is due to the intermittent electrical connection between the interconnect and the device top during the testing.

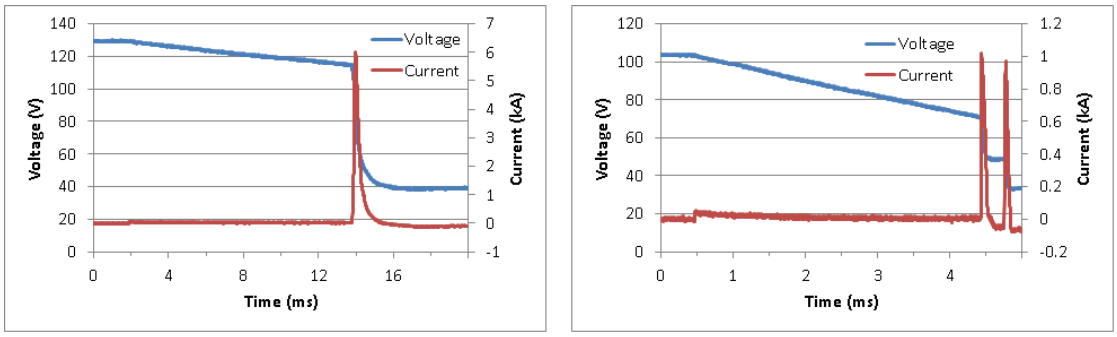


Figure 42: Voltage and current waveforms of flexible PCB bases test vehicles (a) achieved OCFM at 500 J (b) achieved SCFM at 312.5 J.

The summary of the results from flexible PCB based test vehicles can be seen in Table 3

Energy (J)	**Voltage (V)**	**Peak Current (A)**	**Saturation time (ms)**	**Failure Mode**	**Numbers of samples tested**
500	128	6000	10.8	OCFM	1
375	110	4600	14.75	OCFM	1
312.5	101	1100	39	SCFM	2
250	90	-	-	SCFM	1

Table 3: Summary of the results from flexible PCB based test vehicles

4.3.2 Microstructural Observation

Figure 43 shows the test vehicles after testing. Figure 43 (a) is of the test vehicle which resulted in OCFM at 500 Joules of energy whereas the Figure 43 (b) is of test vehicle which achieved SCFM at 312.5 Joules.

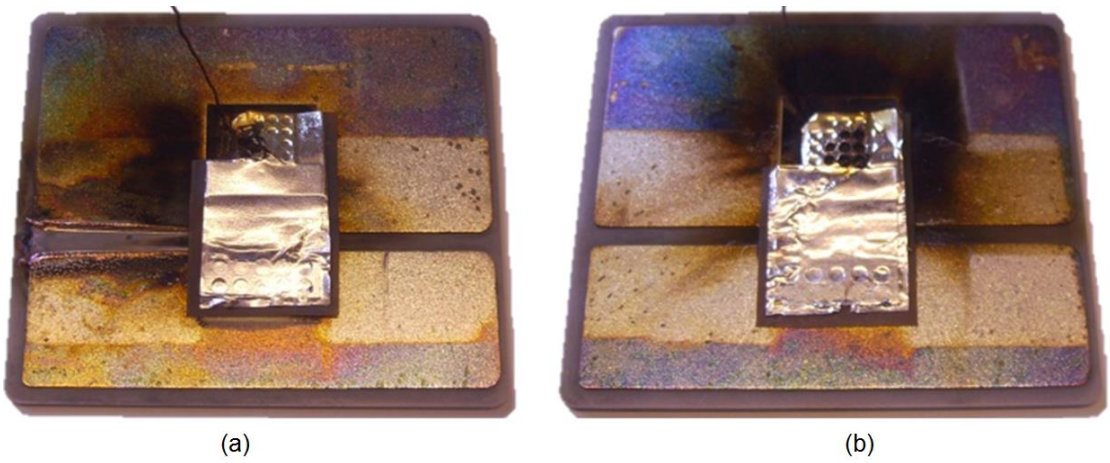


Figure 43: Test vehicles (a) achieved OCFM at 500 J, (b) achieved SCFM at 312.5 J

4.3.2.1 Microstructural Observation of Failed to Open Circuit Test Vehicle

The surface of the IGBT of the test vehicle which was tested at 500 J was scanned under the SEM and is shown in Figure 44. The Figure 44 (a) shows the crater which was formed during the test. The Figure 44 (b) shows the EDX element map of the Figure 44 (a). The EDX stage of the SEM was not able to resolve the bottom of the crater because of the topography of the sample. However, by using an optical microscope, it was observed that the bottom of the crater was the Cu metal of the DBC substrate. It can be clearly seen that the whole surface especially the walls of the crater were covered with a layer of intermetallic compound forming a solidification structure.. In Figure 44 (c) and (d), the dark phase represents Si and the bright

represents Ag, Cu and Al. The fine particle size (Figure 44 c) of Si also suggests that the cooling rate was very rapid. It can be seen In Figure 44 (d) that the composition of the materials at point A is Si 64 at%, Ag 20 at%, Cu 11 at% and Al 4 at%, the composition of the materials at point B is Si 87 at%, Ag 6 at%, Cu 6 at% and Al 1 at% and the composition of the materials at point C is Si 54 at%, Ag 32 at%, Cu 11 at% and Al 3 at%. Areas with high percentage of Si are less conductive whereas the areas with high Cu, Ag and Al are more conductive and these conductive interconnected channels are desirable for SCFM.

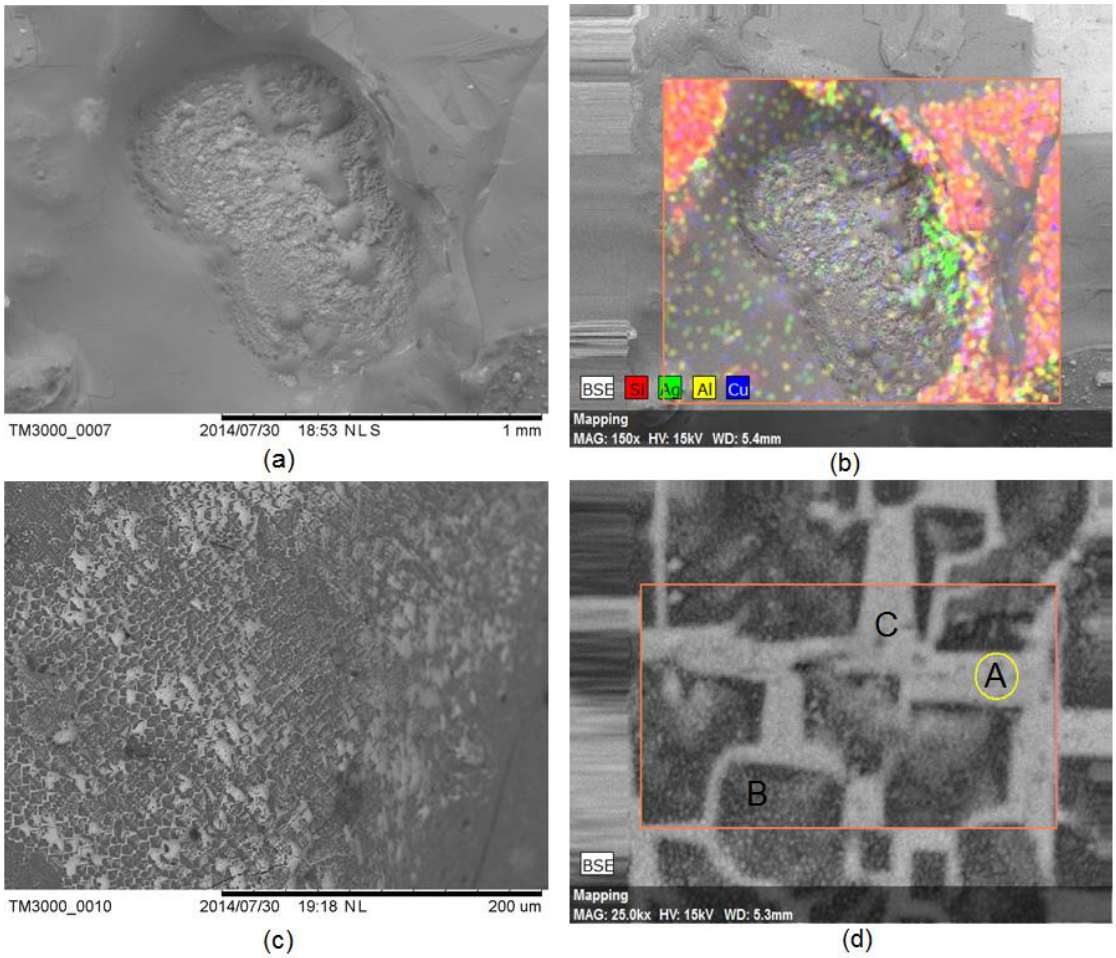


Figure 44: SEM image of the surface of an IGBT failed to open circuit, (a) conductive crater, (b) EDX element map, (c) side wall of crater and (d) EDX points.

The cross-section of the sample was prepared which can be seen in Figure 45. The bright phase is the conductive and the dark phase is the non-conductive Si. In Figure 45 (b) the composition of the materials at point A is Si 54 at%, Ag 40 at%, Cu 2 at% and Al 4 at%, the composition of the materials at point B is Si 90 at%, Ag 9 at%, Cu 0 at% and Al 1 at% and the composition of the materials at point C is Si 97 at%, Ag 3 at%, Cu 0 at% and Al 0 at%.

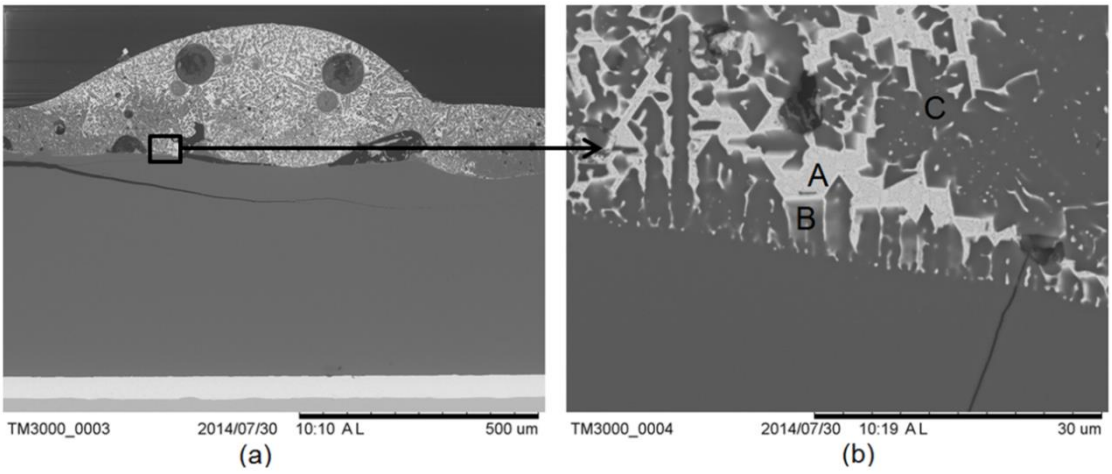


Figure 45: (a) Cross-section of test vehicle which achieved OCFM at 500 J, (b) EDX points.

4.3.2.2 Microstructural Observation of Failed to Short Circuit Test Vehicle

Figure 46 shows the surface analysis of the test vehicle under SEM. The flexible PCB was removed to perform the surface scan. The explosion caused the formation of crater which can be seen in Figure 46 (a). In Figure 46 (c), it can be observed that the walls of the crater are composed of intermetallic compounds which solidified very rapidly resulting in the formation of very fine particle of Si entangled in conductive base. The dark phase in Figure 46 (c) and (d) represents nonconductive Si whereas the

bright phase is conductive and represents Cu, Ag and Al. In Figure 46 (d) The composition of the materials at point A is Si 70 at%, Ag 28 at%, Cu 1 at% and Al 1 at%, the composition of the materials at point B is Si 96 at%, Ag 2 at%, Cu 0 at% and Al 1 at% and The composition of the materials at point C is Si 79 at%, Ag 19 at%, Cu 1 at% and Al 1 at%.

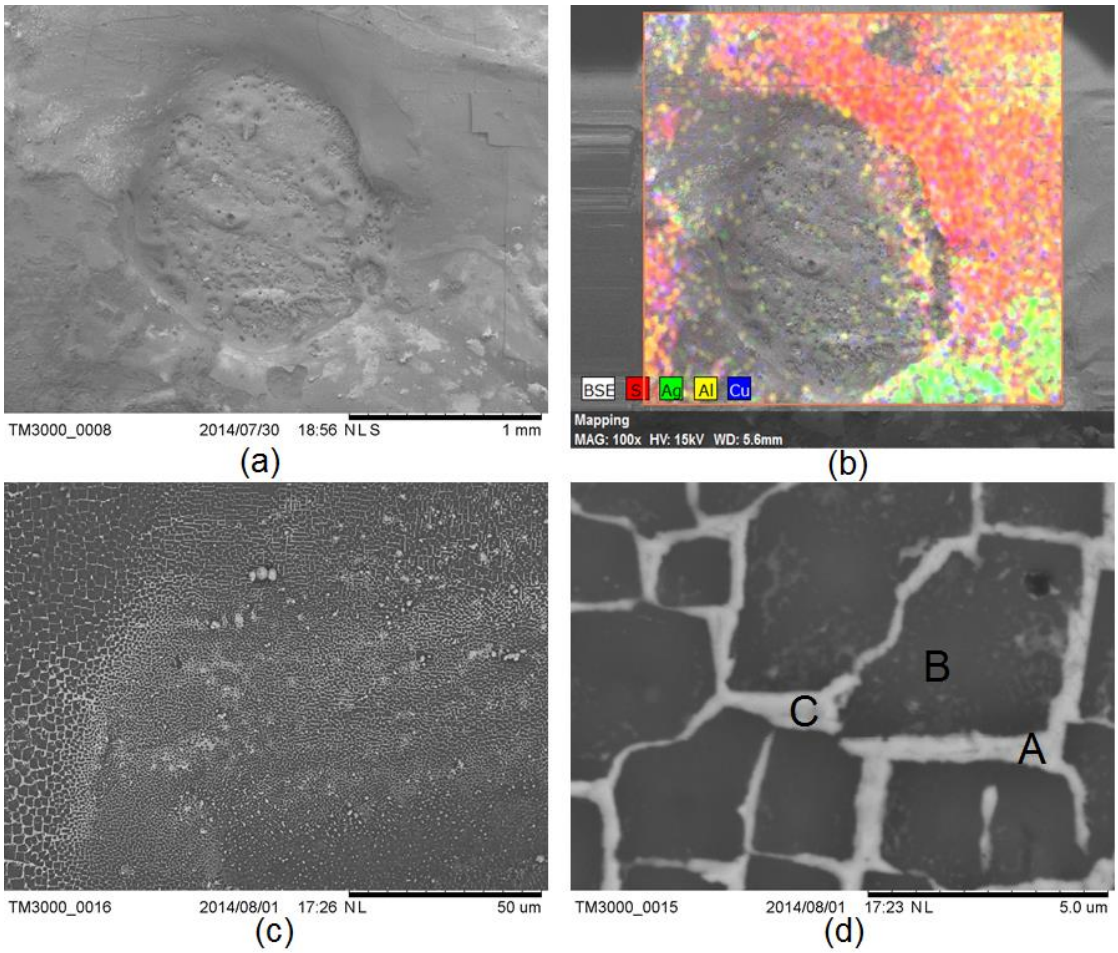


Figure 46: SEM image of the surface of an IGBT failed to short circuit, (a) conductive crater, (b) EDX element map, (c) side wall of crater and (d) EDX points.

The cross-section of the sample was prepared which can be seen in Figure 47. The bright phase in Figure 47 (a) is conductive Cu, Ag and Al whereas the dark phase is

Si. It can be seen that the flexible PCB is still in contact with the top side of the device to make a low resistance conduction path.

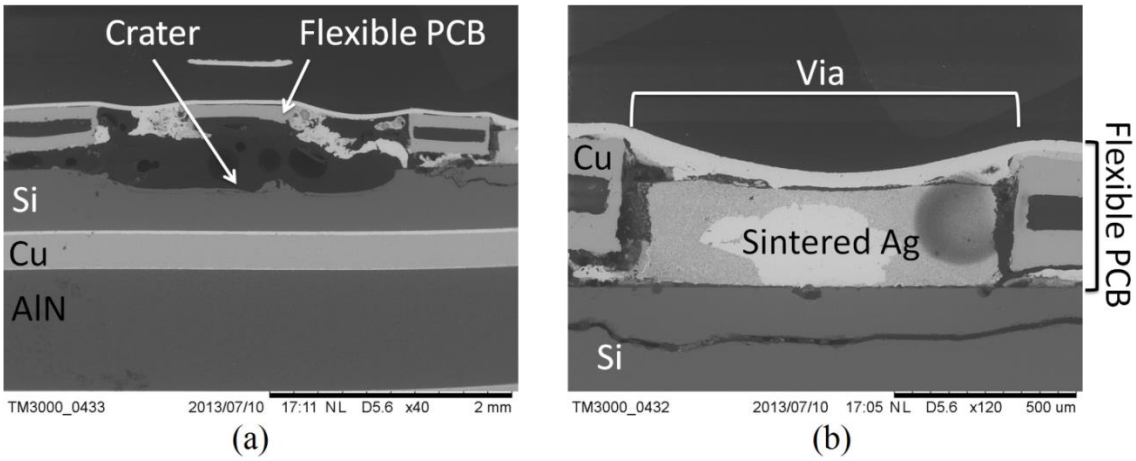


Figure 47: SEM of the test vehicle which attained SCFM at 312.5 J (a) the cross-section showing crater (b) contact interface between Si die top and flexible PCB.

4.4 Discussion

From these experiments, it has been observed that the flexible PCB based test vehicles fail to both open circuit and short circuit depending upon the energy level involved during the test. In the test vehicle that failed to open circuit at 500 J, it was observed that the flexible PCB blew off during the explosion which caused OCFM. On the other hand the flexible PCB stayed in contact with the top of the device in the test vehicle that was tested at 312.5 J causing SCFM.

From the surface microscopy of all the test vehicles it was observed that the metals on the top of the IGBT especially Silver and Aluminium melted and formed a thin coating of the conductive layer. This conductive layer was found making electrical contact with the copper of the substrate through the craters that were formed during the testing; this can be shown in Figure 44 (a) and Figure 46 (a). This implies that

during testing of all test vehicles, if the flexible PCB had stayed in contact with the device, the result would possibly have been failure to short circuit.

In the previous experiments, it was observed that for the wirebonded test vehicles the amount of energy required for a failure to short circuit was in the range from 62.5 J to < 125 J. This wide error range could be reduced by performing the test at various energy levels in between said range but as it is very time/resource consuming process to carry out test, therefore it has not been investigated. If we compare the energy level at which SCFM happened in wirebonded test samples i.e. 62.5 J with the energy level at which flexible PCB based test vehicle achieved SCFM i.e. 312.5 J, it is nearly 5 times increase in the energy level.

Another advantage of the flexible PCB interconnect is the increase in the saturation time of the device. It can be seen from the Table 1 that the saturation time for the wirebonded test vehicle was 2.8ms whereas in flexible PCB it was 39ms which is nearly 14 times increase. This increase in the saturation time is due to the increase in the overall contact area and thermal mass on the device which was achieved by bonding flexible PCB on top of the device. This increase in the saturation time implies that the flexible PCB is well suited for applications that involve high surge currents.

Instead of using SnAg solder, silver sintering has been used to bond both the IGBT to the substrate and the flexible PCB to emitter side of the IGBT. Silver has higher melting temperature (961°C) as compared to SnAg solder (221 °C) which implies that it can be used for the high temperature applications.

4.5 Summary

The flexible PCB based test vehicles can fail to either a short or an open circuit. The energy level required to get failure to short circuit has been increased from 62.5 J in case of wirebonds, to 312.5 J in case of flexible PCB. However, the energy level is still below target. Therefore both wirebonded samples and flexible PCB based samples are most likely to fail into an open circuit.

Beside the most apparent advantage which is the increase in energy level to have a failure to short circuit, other advantages have been found by replacing wirebonds with a flexible PCB. Some of these advantages are e.g. large contact area which led to low contact resistance and increased I^2t rating of the interconnect and device.

As the OCFM is caused by the high energy which physically detaches the flexible PCB from the top of the device therefore, the next question that arises is what can be done to keep the flexible PCB interconnect to stay in contact with the conductive phase of device. One possible solution is to reinforce the flexible PCB to device top interface by soldering another DBC on top of the flexible PCB so that the flexible PCB stays and keep contact with the conductive path during the test. This is what will be investigated in the next chapter.

5 Failure Modes of Sandwich Structure IGBT Test Vehicles

5.1 Introduction

In the previous chapter, tests were carried out on the Flexible PCB based test vehicles and it was found that they fail to both open and short circuit depending upon the energy level. It was further observed that the failure to open circuit was caused by the physical lift off of the flexible PCB during explosion because of the thermo-mechanical forces. In this chapter this problem will be addressed by construction of a new type of test vehicle which will confine the flexible PCB between two DBCs.

5.2 Experiment

5.2.1 Sample Preparation

In total two test vehicles were prepared because of the limited availability of silver top power IGBT dies. The preparation of samples started by using the flexible PCB test vehicles i.e. by following the steps mentioned in section 4.2.2. A DBC equal to the size of the flexible PCB was then soldered on top of the flexible PCB. The schematic can be seen in Figure 48.

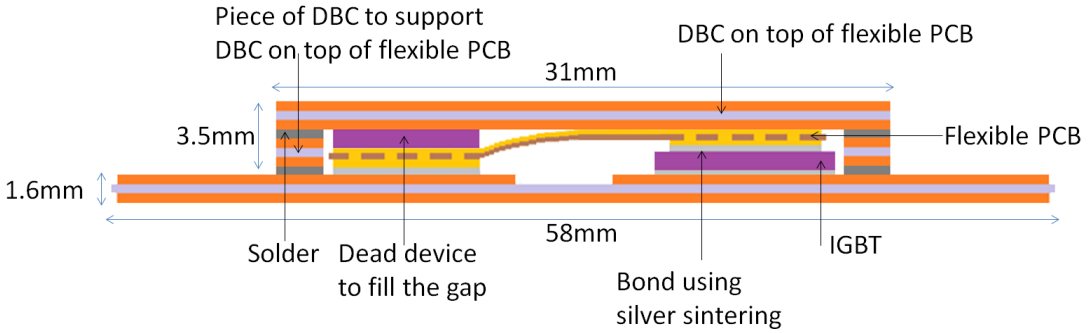


Figure 48: Schematic of sandwich test vehicle

5.2.2 Test Procedure

It should be noted that the test rig was set up similarly to that described in section 3.2.2. The estimation of amount of energy required to cause the failure to short circuit in the new test vehicle was difficult. From the previous experimental conclusions, it was expected that the energy level to achieve SCFM would be greater than 312.5 J (which was the amount of energy required to cause SCFM in flexible PCB based test samples) due to the presence of more thermal mass on the device and confined sandwich structure. As there were only two samples it was therefore decided to test the first sample at 750 J which is considered to be a moderate realistic mount of energy that a device would face in real industrial scenario.

5.3 Experimental Results

5.3.1 Electrical Testing

The first test vehicle was tested at 750 J and it was observed that it achieved SCFM. The second test vehicle was tested at double the amount of that energy i.e. 1500 J and it was noted that the test vehicle acquired OCFM as the integrity of the structure was lost.

The electric current and voltage through and across the device respectively can be seen in the Figure 49. Figure 49 (a) is of the test vehicle which resulted in SCFM at 750 J whereas the Figure 49 (b) corresponds to the test vehicle which achieved OCFM at 1500 J.

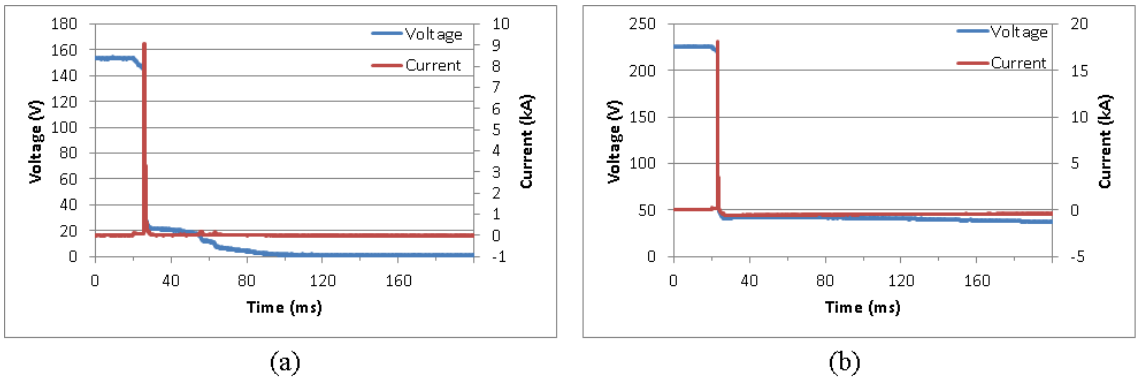


Figure 49: Voltage and current waveforms of sandwich structure based test vehicles (a) achieved SCFM at 750 J (b) achieved OCFM at 1500 J.

The summary of the results from flexible PCB based sandwich structure test vehicles can be seen in Table 3.

Energy (J)	**Voltage (V)**	**Peak Current (A)**	**Saturation time (ms)**	**Failure Mode**	**Numbers of samples tested**
1500	221	17500	2	OCFM	1
750	156	9000	3	SCFM	1

Table 4: Summary of results from sandwich structure based test vehicles.

5.3.2 3D Microstructural Observations

Figure 50 shows the sandwich type test vehicle after the explosion testing. Figure 50 (a) is of the test vehicle which achieved SCFM at 750 Joules of energy whereas Figure 50 (b) is of test vehicle which achieved OCFM at 1500 Joules. In Figure 50 (b) it can be seen that the test was very catastrophic as it disintegrated the whole structure.

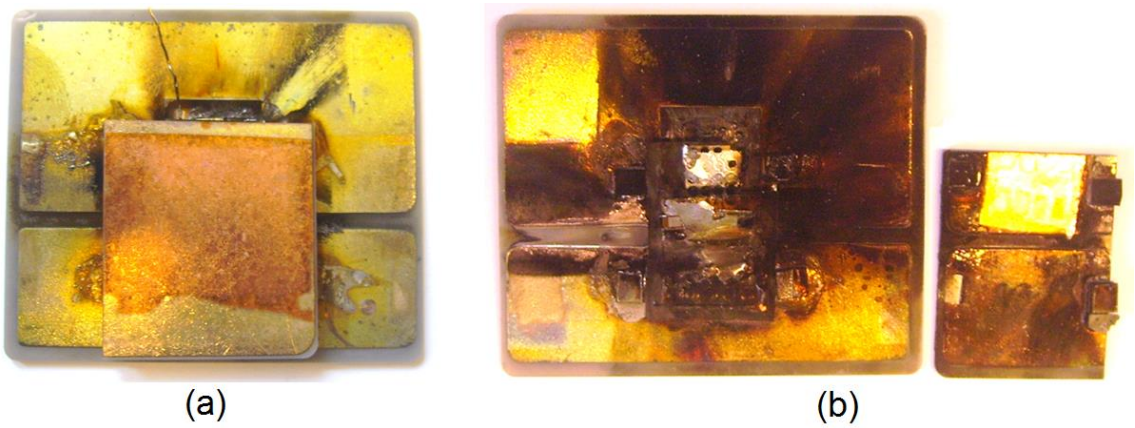


Figure 50: Test vehicle (a) achieved SCFM 750 J (b) achieved OCFM at 1500 J

In the previous experiments, the samples after performing the test were cross sectioned and characterised with SEM. Their results revealed the formation of conductive intermetallic compound comprising of Sn, Ag, Al and Cu which covered the surface of Si die. They were necessary for providing the conductive path between emitter and collector of the device in the cases where the sample failed to short circuit during explosion test. This was the microstructural mechanism for achieving SCFM.

In the present section the emphasis will be placed on the coordination of supplied energy with the phase change of failure site and estimate of possible maximum temperature during the explosion test. For this purpose the accurate estimation of the volume of failure site is very important. If the SEM images are used for volume calculation, lots of cross sections need to be performed which is extremely time consuming and the sample will be destroyed. Therefore, 3D X-Ray Microscopic Computed Tomography Images have been used to estimate the amount of the material that has be melted or possibly vaporised during the explosion. Figure 51 shows the one representative 2D image extracted from 3D image in which failure site has been shown. The equipment that has been used to do the 3D scanning was Xradia Versa XRM-500 which creates 3D image by scanning 2D images and then reconstruct them into 3D.

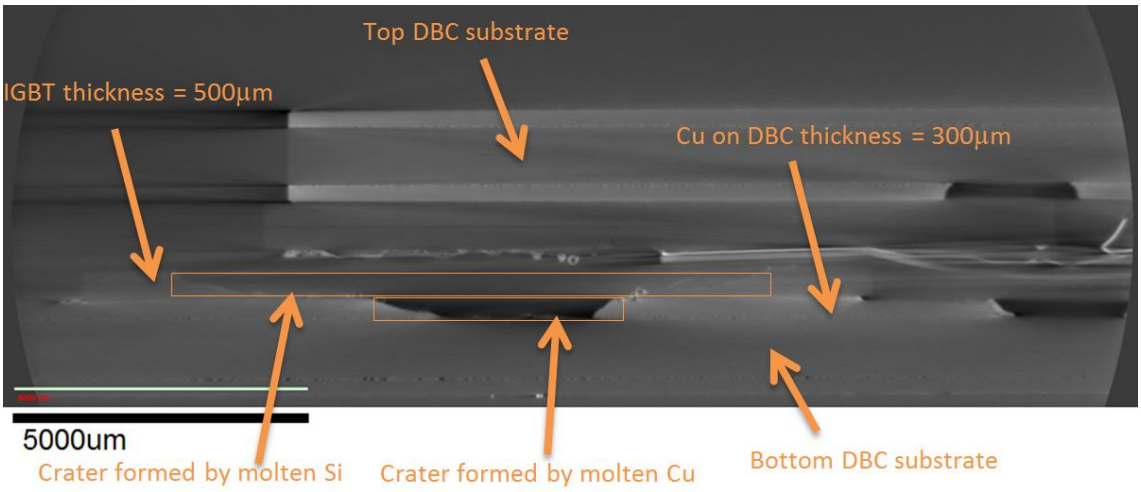
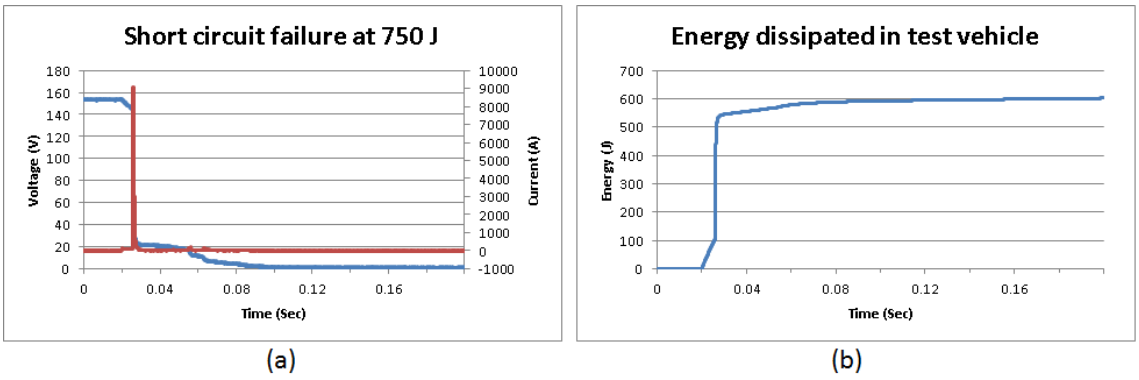


Figure 51: Cross-sectional view taken from reconstructed 3D X-ray CT images of sample which failed to short circuit

5.4 Phase change of metals and its correlation with input energy

The energy stored in the capacitor bank at which the explosion test was performed was 750 J but to calculate the actual energy that dissipated in an IGBT device, voltage and current waveforms were multiplied and integrated over the time yielding the input energy Q_{input} to be 600 J which can be seen in Figure 52 (b), rest of the energy has been dissipated in the equivalent series resistance (ESR) of the capacitor and the copper busbar.



(a) (b)

Figure 52: (a) Current pulse (b) Energy

The heating source is the current pulse which passed through the silicon device and from Figure 52 it can be seen that the duration of the current pulse was approximately 44ms. This implies that all the energy has been dissipated in 44ms. Assuming that all the energy has been dissipated in the silicon die, the heat zone distance can be estimated by using the following equation [60]:

$$X = \sqrt{\frac{K_{Si}t}{\rho_{Si}C_{Si}}} \qquad \textbf{5.1}$$

Where the heat zone distance in m is$X$, K_{Si} is the thermal conductivity of Si, t is the time in Sec, ρ_{Si} is the density of Si and C_{Si} is the specific heat capacity of Si.

Putting the values:

$$X = \sqrt{\frac{130 \times 44e^{-3}}{2329 \times 750}} = 1.8e^{-3}m$$

As the heat zone size is 1.8mm and the duration of the current pulse was very short, therefore it is safe to assume that most of the energy was dissipated in the heat zone causing temperature rise in Si and close contact materials.

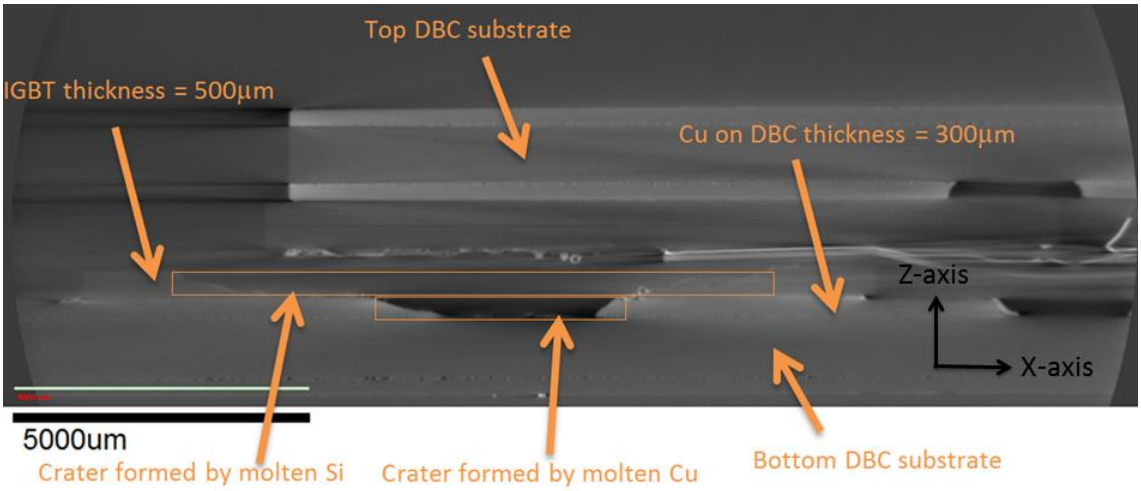


Figure 53: Image in XZ plane showing the crater

Figure 53 shows the crater which was formed during the explosion. It can be seen that the crater was formed by molten Copper and Silicon. The volume of the Cu and Si was calculated separately by using the ImageJ software.

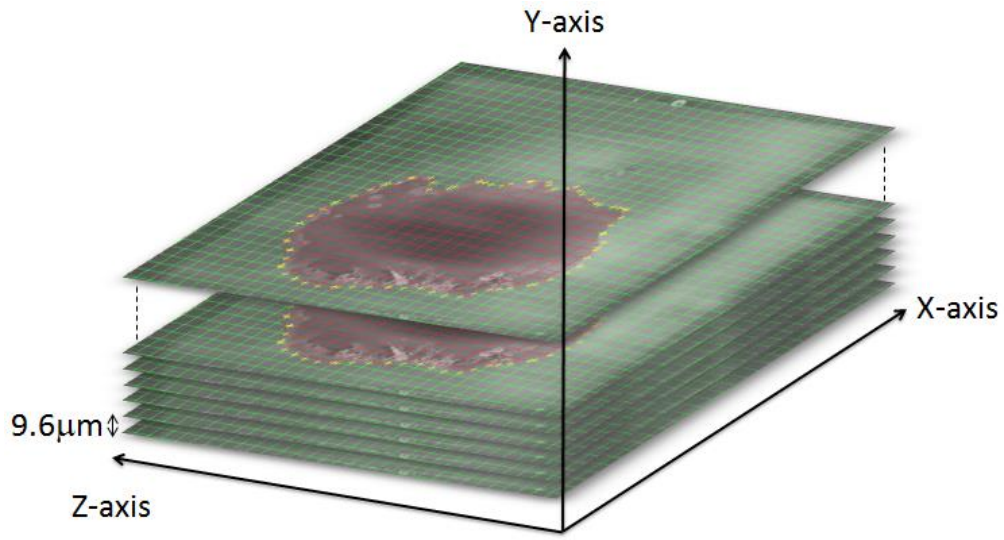


Figure 54 Images in XY plane showing crater area enclosed in yellow circle

The X-ray scanning of test sample in the XY plane was performed with the step wise increment of 9.6µm in Y-axis direction and as the thickness of the Cu on DBC was 300µm therefore, the volume occupied by the crater in 31 images (starting above the alumina ceramic) was calculated manually using ImageJ which turned out to be:

$$Volume\ of\ the\ Cu = \ 4.4592e^{-9}m^3$$

Similarly volume of the Si was calculated from 53 images as IGBT device was 0.5mm thick which is:

$$Volume\ of\ the\ Si = \ 23.988e^{-9}m^3$$

To find out the phase change of the metals i.e. whether they have melted or vaporised leaving crater behind, it is essential to find out the amount of energy required for the phase change of metals involved in the explosion.

From the volume, the mass of the Cu can be calculated as:

$$m_{Cu} = d_{Cu}V_{Cu} \qquad \textbf{5.2}$$

Where the mass of Cu is m_{Cu}, d_{Cu} is the density of Cu and V_{Cu} is the volume of Cu. As the density of d_{Cu} is $8960^{kg}/_{m^3}$therefore the mass becomes:

$$m_{Cu} = 8960\,{}^{kg}/_{m^3} \times 4.4592e^{-9}m^3 = 39.95e^{-6}kg$$

Similarly the mass of the Si can be calculated as:

$$m_{Si} = d_{Si}V_{Si} \qquad \textbf{5.3}$$

Where the mass of Si is m_{Si}, d_{Si} is the density of Si and V_{Si} is the volume of Si. As the density of d_{Cu} is $2329^{kg}/_{m^3}$therefore the mass becomes:

$$m_{Si} = 2329\,{}^{kg}/_{m^3} \times 23.988e^{-9}m^3 = 55.86e^{-6}kg$$

The number of moles of Si can be given as:

$$N_{Si} = \frac{m_{Si}}{A_r^{Si}} = \frac{55.86e^{-6}}{28.085} = 1.988e^{-6}$$

Where N_{Si} is the number of moles of Si and A_r^{Si} is the relative atomic mass of Si

Similarly the number of moles of Cu can be given as:

$$N_{Cu} = \frac{m_{Cu}}{A_r^{Cu}} = \frac{39.95e^{-6}}{63.546} = 0.628e^{-6}$$

Where N_{Cu} is the number of moles of Cu and A_r^{Cu} is the relative atomic mass of Cu

The molar ratio can be given as:

$$molar\ ratio = \frac{N_{Si}}{N_{Si} + N_{Cu}} = \frac{1.988e^{-6}}{1.988e^{-6} + 0.628e^{-6}} = 75.4\%$$

The binary phase diagram of Cu and Si can be shown in Figure 55.

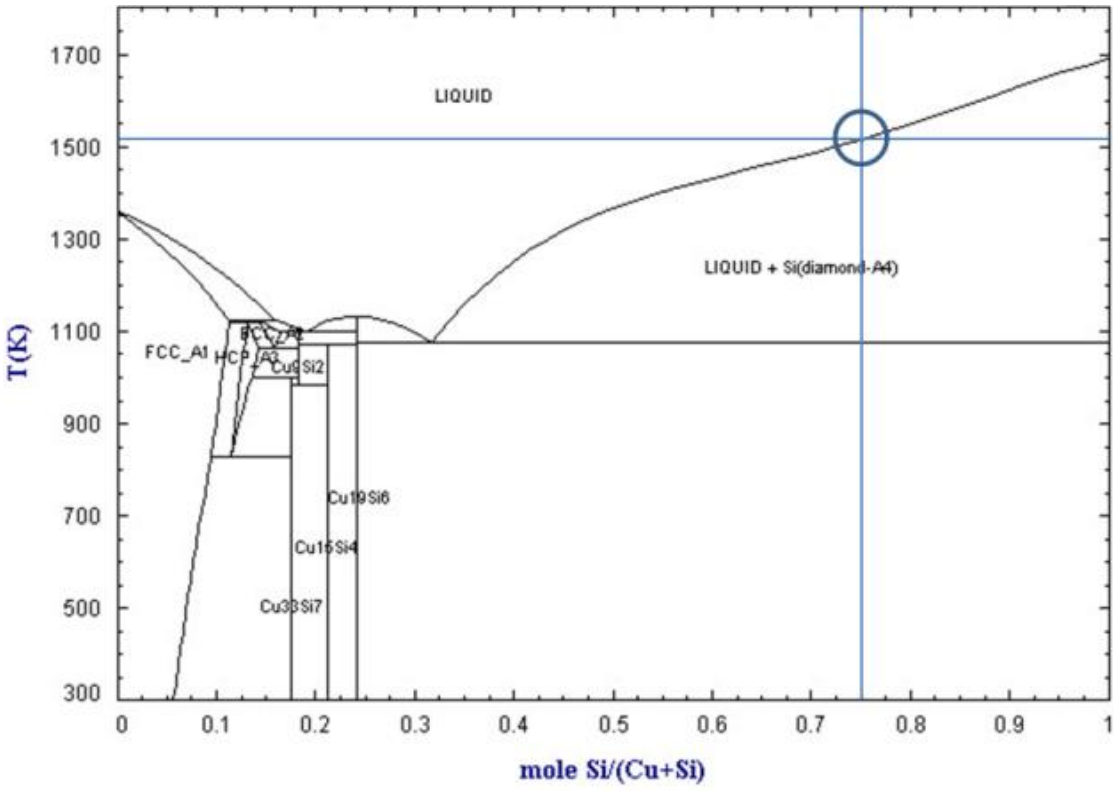


Figure 55: Binary phase diagram of Cu-Si [61]

It can be seen from the phase diagram that for molar ratio of 75% the temperature required is about 1505 K or 1232°C.

The amount of energy required to melt Cu can be given by the following equation:

$$Q_{Cu}^{1} = m_{Cu} \int_{T_r}^{T_{min}} C_{Cu} dT + m_{Cu} \Delta H_{Cu} \qquad \textbf{5.4}$$

Where $Q_{Cu}^{1}$is the amount of energy required to change the phase of Cu from solid to liquid, T_{min} is the minimum temperature required for the molar ratio of Si and Cu to be in liquid phase which is 1232°C, $T_r$is the room temperature, $C_{Cu}$is the specific heat capacity of Cu which is $385 {}^{J}/_{kg}\,^{\circ}C$ and $\Delta H_{Cu}$is the latent heat of fusion for Cu which is $205 {}^{kJ}/_{kg}$

The above equation can be simplified to:

$$Q_{Cu}^{1} = m_{Cu}C_{Cu}(T_{min} - T_r) + m_{Cu}\Delta H_{Cu} \qquad \textbf{5.5}$$

By putting the values:

$$Q_{Cu}^{1} = 39.95e^{-6} \times 385(1232 - 25) + 39.95e^{-6} \times 205000 = 18.56 + 8.189$$
$$= 26.74\,J$$

Similarly:

The amount of energy required to melt Si can be given by the following equation:

$$Q_{Si}^{1} = m_{Si}\int_{T_r}^{T_{min}} C_{Si}dT + m_{Si}\Delta H_{Si} \qquad \textbf{5.6}$$

Where $Q_{Si}^{1}$is the amount of energy required to change the phase of Si from solid to liquid, T_{min} is the minimum temperature required for the molar ratio of Si and Cu to be in liquid phase which is 1232°C, $T_r$is the room temperature, $C_{Si}$is the specific heat capacity of Si which is $750\,{}^{J}/_{kg}\,^{\circ}C$ and $\Delta H_{Si}$is the latent heat of fusion for Si which is $1926\,{}^{kJ}/_{kg}$

The above equation can be simplified to:

$$Q_{Si}^{1} = m_{Si}C_{Si}(T_{min} - T_r) + m_{Si}\Delta H_{Si} \qquad \textbf{5.7}$$

By putting the values:

$$Q_{Si}^{1} = 55.86e^{-6} \times 750(1232 - 25) + 55.86e^{-6} \times 1926000 = 50.56 + 107.58$$
$$= 158.14\,J$$

Now the total energy required for the formation of the liquid is:

$$Q^{1} = Q_{Cu}^{1} + Q_{Si}^{1} = 26.74 + 158.14 = 184.88\,J$$

As was calculated earlier the energy input to the test vehicle i.e. Q_{input} was 600 J and the energy utilised to melt both Cu and Si i.e. Q^{1} was 184.88 J which is far less than

the input energy therefore there is the possibility that the molten Cu and Si has reached quite high temperature.

(5.8) can be used to calculate if the energy was enough to take Cu to its boiling point.

$$Q_{Cu}^{2} = m_{Cu}C_{Cu}\left(T_{Cu}^{b} - T_{min}\right) \qquad \textbf{5.8}$$

Where Q_{Cu}^{2} is the amount of energy required to raise the temperature of copper to the boiling point, $T_{Cu}^{b}$is the temperature at which the Cu boils i.e. 2562°C and T_{min} is the minimum temperature required for the molar ratio of Si and Cu to be in liquid phase which is 1232°C.

Putting the values:

$$Q_{Cu}^{2} = 39.95e^{-6} \times 385(2562 - 1232) = 20.45\,J$$

Similarly the amount of energy required by Si to reach the similar temperature is:

$$Q_{Si}^{2} = m_{Si}C_{Si}\left(T_{Cu}^{b} - T_{min}\right) \qquad \textbf{5.9}$$

Where Q_{Si}^{2} is amount of energy required to raise temperature of Si to the boiling point of Cu

Putting the values:

$$Q_{Si}^{2} = 55.86e^{-6} \times 750(2562 - 1232) = 55.72\,J$$

Therefore the total amount of energy Q^{2} required to raise the temperature of both metals upto the boiling point of copper can be given as:

$$Q^{2} = Q^{1} + Q_{Cu}^{2} + Q_{Si}^{2} = 184.88\,J + 20.45\,J + 55.72\,J = 261.05\,J$$

From the above calculation it can be seen that Q_{input} which is 600 J is still greater than the amount of energy required to raise the temperature of both Cu and Si to the boiling point of Cu. Therefore it is quite possible that Cu has reached the gas phase.

The amount of energy Q^3 required to change the phase of Cu from solid to gas can be calculated by:

$$Q^3 = Q^2 + m_{Cu}\Delta H^e_{Cu} \qquad \textbf{5.10}$$

Where ΔH^e_{Cu} is the latent heat of vaporisation for Cu which is $4730^{kJ}/_{kg}$

Putting the values:

$$Q^3 = 261.05\,J + 39.95e^{-6} \times 4730000 = 450.01\,J$$

As Q^3 is still less than Q_{input} therefore it is quite possible that the silicon has reached its boiling point. The amount of energy Q^4 required to raise the temperature of Si to its boiling point can be given by:

$$Q^4 = Q^3 + m_{Si}\int_{T^b_{Cu}}^{T^b_{Si}} C_{Si}dT \qquad \textbf{5.11}$$

Where T^b_{Si} is the boiling point of Si which is 3265°C, and T^b_{Cu} is the boiling point of Cu which is 2562°C. The above equation can be simplified as:

$$Q^4 = Q^3 + m_{Si}C_{Si}\left(T^b_{Si} - T^b_{Cu}\right) \qquad \textbf{5.12}$$

By putting values:

$$Q^4 = 450.01 + 55.86e^{-6} \times 750(3265 - 2562) = 479.46\,J$$

As Q^4 is still less than Q_{input} therefore, it is possible that the Si has reached the gas phase. The amount of energy Q^5 required to raise the temperature of Si to change its phase from liquid to gas can be calculated by using the following equation:

$$Q^5 = Q^4 + m_{Si}\Delta H^e_{Si} \qquad \textbf{5.13}$$

Where ΔH^e_{Si} is latent heat of vaporisation of Si and its value is $12800^{kJ}/_{kg}$

Putting values:

$$Q^5 = 479.46\,J + 55.86e^{-6} \times 12.8e^{6} = 479.46\,J + 715\,J = 1194.46\,J$$

As Q^5 is much greater than the Q_{input} (600 J) therefore, it is reasonable to conclude that the energy was enough only to vaporise a small amount of Si.

5.5 Stability of SCFM

The IGBT that has been used in this study is capable to pass maximum continuous current of 50 A and that would be the maximum current the device will ever face in the normally operating industrial application. After the failure of the device, it is therefore required that the device should be able to pass 50 Amperes of current through it for a specific period of time.

From the literature review it was noted that one author has mentioned about this specific period of time to be several hundred hours [57]. Hence, it was decided to pass the current through the device and measure the voltage across the device to calculate the contact resistance of the short circuit and to observe the trend of change in resistance over time. Now if the resistance of the failed device does not change much over time from its initial low value then it would be called stable short circuit whereas if it changes significantly over time then it would be called unstable short circuit.

Therefore, 50 Amperes of current was passed through the test sample which achieved SCFM by using a high current low voltage power supply (50 A/10 V) to determine whether the failure to short circuit was stable or not. The voltage drop across the device was noted to calculate the resistance. The forced air was used to cool the test sample during the current passage test. It was observed that the initial resistance was 21 mΩ but after only 12 hours of continuously passing current the value of the resistance went up to 200 mΩ. As there was a significant change in the resistance therefore, it was considered as an unstable short circuit.

5.6 Discussion

In the case of flexible PCB test vehicles, the energy required to have a failure to short circuit was 312.5 J whereas, it can be seen that the amount of energy has been increased to 750 J by using sandwich structure. If both structures are compared, the only difference is the presence of more thermal mass on the device and confinement of the device between two DBCs. This implies that the energy required to achieve SCFM has got a direct relationship with the thermal mass on the device, interconnection type and the structure of the test vehicle.

Figure 52 (a) shows the current and voltage waveforms of test vehicle which resulted in SCFM. The stored energy in the capacitor bank was 750 J whereas only 600 J of energy was dissipated in the test vehicle in 44ms; rest of the energy was dissipated in the ESR and contact resistance of the test rig. By using the heat equations it was calculated that the amount of energy was sufficient to raise the temperature of the silicon to its boiling point which is 3265°C and as the boiling temperature of Cu is 2562°C it caused Cu to vaporise first leaving the crater behind which can be seen in Figure 53.

When the device fails, it tries to interrupt the current flowing through it causing the generation of electric arc which depending upon the input energy can reach high temperature. This electric arc causes the Si to change its phase from solid to gas which expands and escapes the test vehicle very rapidly; hence putting a lot of thermo-mechanical stress on the test vehicle results of which can be seen in Figure 50 (b).

5.7 Summary

Sandwich structure test vehicles can both fail to short circuit and open circuit depending upon the input energy level. However, with the sandwich structured test vehicle the amount of the energy required to achieve SCFM has been increased to

750 J which can be considered as a moderate realistic energy level that a device can face in the actual industrial application. Although the test vehicle failed to the short circuit but it was not stable as its resistance crept up with passage of current over the time. It has also been verified by using heat equations that during the failure the amount of energy required to melt/vaporise the total amount of materials which left crater in the test vehicle was well within the range of input energy.

To further test the argument that if the confined structure can yield a failure to short circuit, a new confined packaging structure called the press pack IGBT will be tested in the next chapter.

6 FAILURE MODES OF PRESS PACK IGBT TEST VEHICLE

6.1 Introduction

In the previous chapter, the sandwich structure based test vehicles were tested and it was observed that they fail to both open and short circuit depending upon the energy level. One of the most important outcomes of the last chapter was that the energy level at which SCFM could be sustained was increased by using sandwich structure to 750 J which was the target energy level.

It was also learned from the previous experiments that during the explosion craters are formed which create a physical gap between the failed die and the emitter contact. In order to get a failure to short circuit, that gap has to be filled by some conducting material. One way of doing that is by using a spring loaded mechanism which applies pressure and bring the emitter electrode back in contact with the failed device.

In this chapter spring loaded mechanism based test vehicle called press pack IGBT will be prepared and tested for its abilities of failure to short circuit.

6.2 Experiment

6.2.1 Test Vehicle Preparation

The test vehicle in this experiment contains two parts i.e. the frame which provides the spring loaded contact and the actual sample. The frame has been designed so that it can be re-used to accommodate different test samples. The frame can be seen in the Figure 56. It consists of three parts; a baseplate, a “C” shaped steel frame and a steel bolt. The baseplate is made up of GPO3 which is composite sheet made up from glass

matt and polyester resin. GPO3 exhibits an excellent combination of high strength and good flame resistance. A “C” shaped steel frame is fitted on top of the baseplate. The “C” shaped steel frame contains a threaded hole to accommodate a steel bolt. The steel bolt is specially designed with a spring loaded steel ball on one end. The steel bolt can be moved up and down by turning it anticlockwise and clockwise respectively. This steel bolt also act as the electrical contact for the emitter terminal of the IGBT.

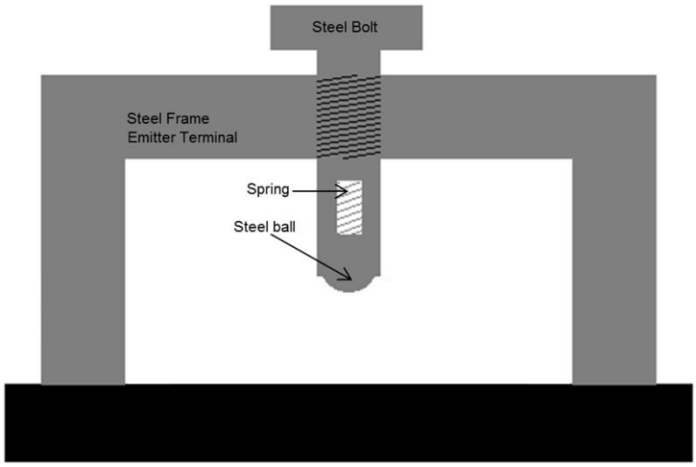


Figure 56: The re-usable frame of the test vehicle

The power semiconductor devices used in the preparation of the samples were the 13.5mm X 13.5mm 2500V/50A corner gate IGBT having Al metallization on both the emitter and gate pad and ~0.1/1/1 μm Ti/Ni/Ag metallization on the collector side. These IGBT were made by Dynex Semiconductor Ltd. The construction of the test sample was done using the following steps:

1. The DBC substrate was cleaned first by using plasma cleaners to get rid of any organic coatings and oxides.
2. A mask was made out of 100um thick Aluminium foil to deposit solder paste as shown in Figure 57 (b).

3. The mask was placed on the DBC substrate and the paste was applied to the DBC by using a squeegee as shown in Figure 57 (c) and (d).
4. The IGBT die was placed on top of the solder paste Figure 57 (e) and then was placed in the reflow oven. As the reflow was done in the presence of the air, it caused the oxidation of the DBC which was later removed by slightly warming the DBC to about 60C and then applying the flux. This removal of the oxidation layer was essential for the next step which is wirebonding.

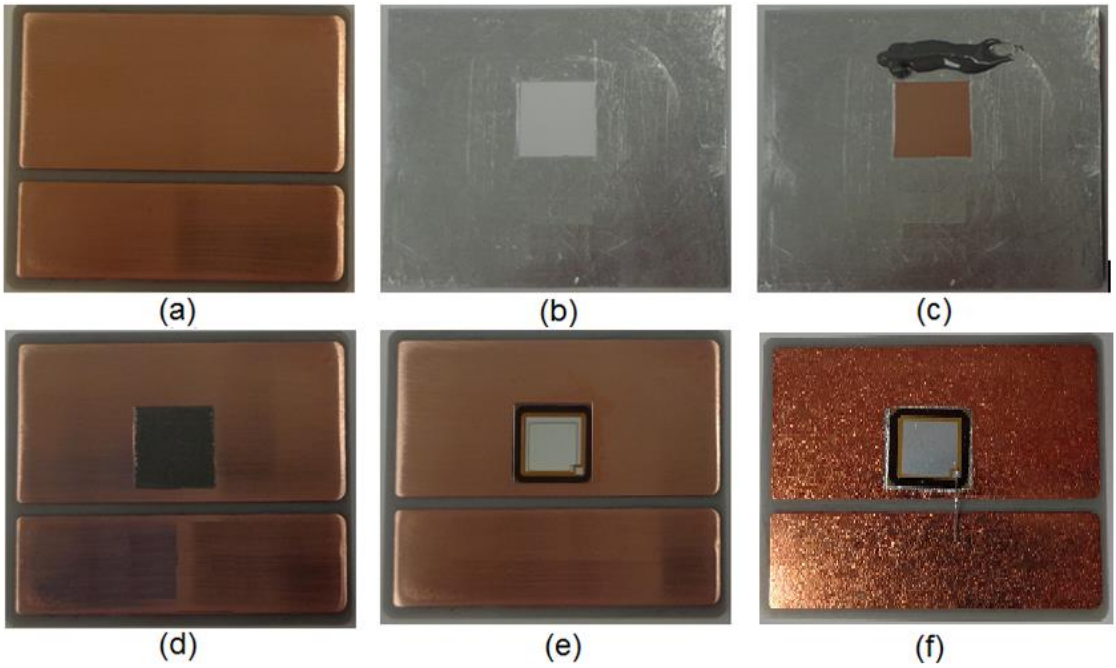


Figure 57: Preparation of test sample (a) two island DBC substrate (b) Aluminium mask (c) Mask placed on the substrate with solder paste applied to the mask (d) Solder paste spread using squeegee (e) IGBT placed over the solder paste (f) finished test vehicle after passing through reflow oven and wirebonding process.

5. For the preparation of this test vehicle only one wirebond was needed to connect the gate terminal of the IGBT to one of the island of the substrate. It was done by

using the standard 99.999% pure 375um diameter Al wire. The finished test vehicle can be seen in Figure 57 (f)

The schematic diagram of test vehicle can be shown in Figure 58. To prepare the test vehicle, the test sample is loaded under the steel bolt; the bolt is lowered until the steel ball touches the emitter of the IGBT and then the bolt is tightened by using calibrated torque wrench to achieve the specified pressure.

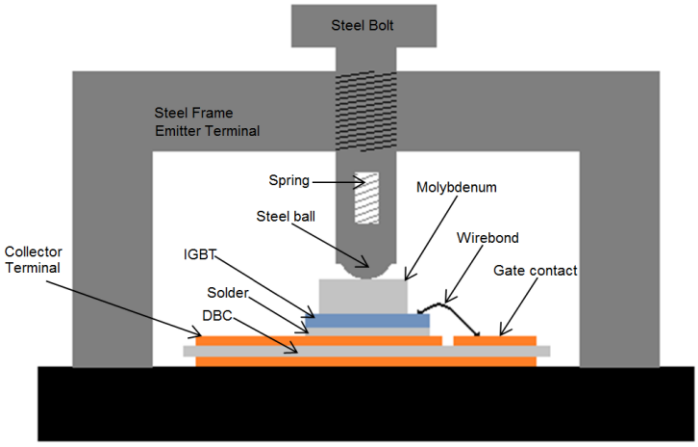


Figure 58: Schematic diagram of press pack IGBT test vehicle

A small 8×8mm wide and 2mm thick Molybdenum shim has been used to distribute the pressure evenly over the IGBT die. Molybdenum has been used because it has low resistivity and its CTE is very close to Silicon, hence that makes it the most suitable candidate.

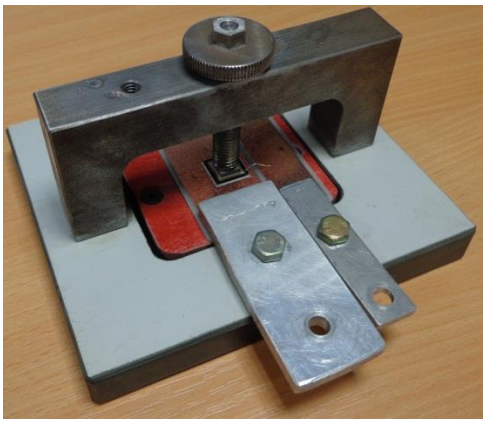


Figure 59: The complete test vehicle.

The complete test vehicle which comprises the frame and the test sample can be seen in Figure 59.

6.2.2 Test Procedure

It should be noted that the test rig was set up similarly to that described in section 3.2.2. After preparation, the test vehicle was connected to the test rig as shown in Figure 60.

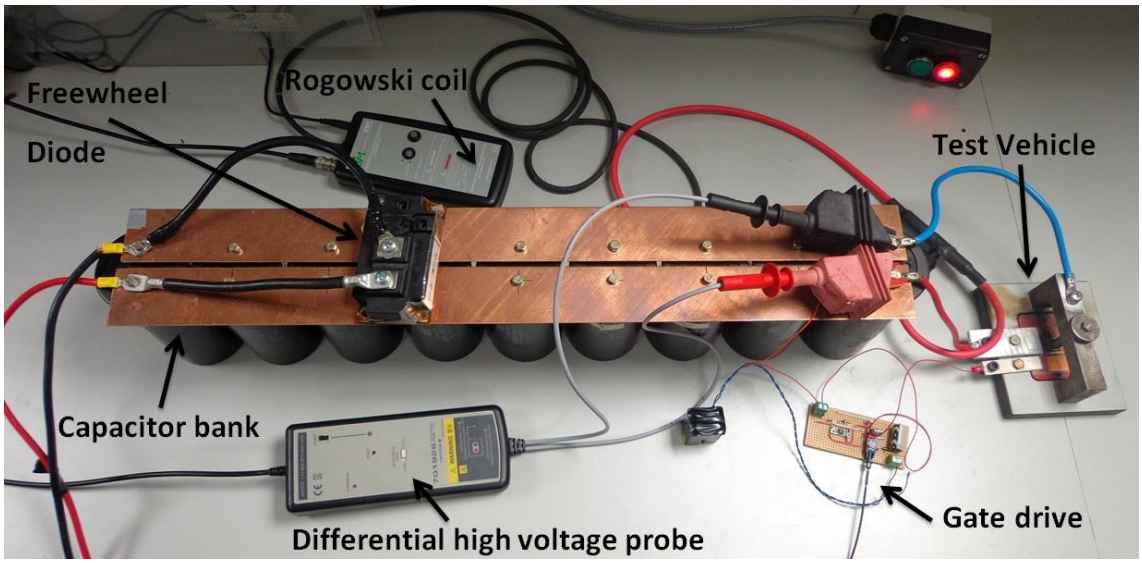


Figure 60: Test vehicle connected to test rig

2MPa pressure was applied on the IGBT die by rotating the bolt clockwise using a torque wrench which was calibrated by using the load cell. The capacitor bank was charged up to 156V yielding 750 J of stored energy. After charging the capacitor bank, the IGBT was turned on by using the gate drive which was triggered using the function generator to discharge all the energy stored in the capacitor through the IGBT.

To test whether the test sample failed to a stable or unstable short circuit, after the explosion test, collector and emitter terminal of the test vehicle were connected to

50A/10V power supply. 50 A of current was selected to pass through the device because it is the maximum average current that can be passed through the single IGBT die under normal conditions. Hence, the current was passed through the failed device and the voltage drop across the device was measured to calculate the contact resistance.

6.3 Experimental Results

6.3.1 Electrical Testing

The test vehicle was tested at 750 J and the electric current and voltage through and across the device respectively can be seen in Figure 61. From the waveforms it can be seen that the test vehicle failed to short circuit because voltage across the device collapsed to zero after explosion. To determine if the failure to short circuit was stable or not, 50 A of current was passed through the device. The voltage drop across the device was measured and resistance was calculated.

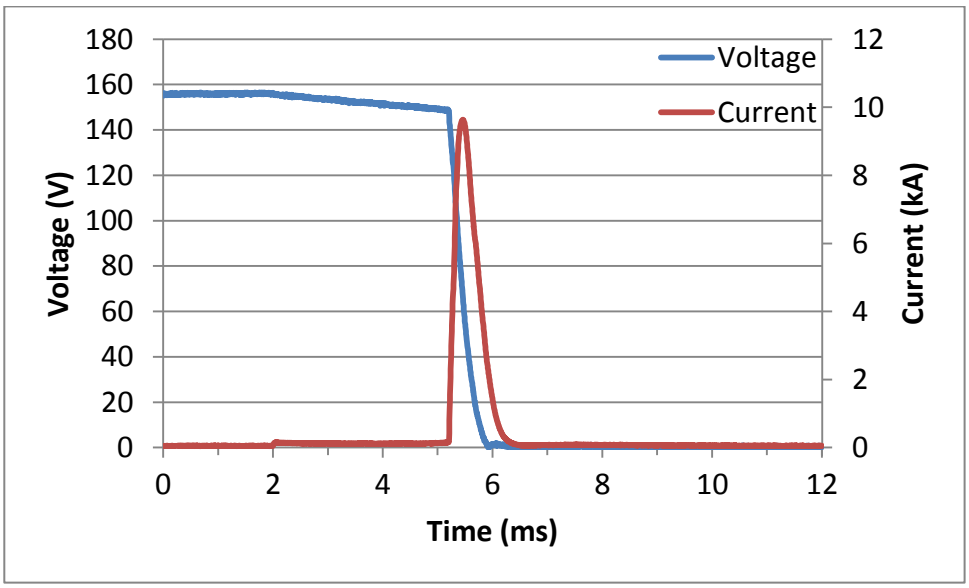


Figure 61: Voltage and current waveforms of Mo based test sample exploded at 750 J

Figure 62 shows the resistance profile of Mo based test sample. It was observed that the initial resistance of the short circuit was very low i.e. 5.4mΩ which went on increasing with the passage of time and reached to 200mΩ in 33 hours which implies that it was not a stable short circuit.

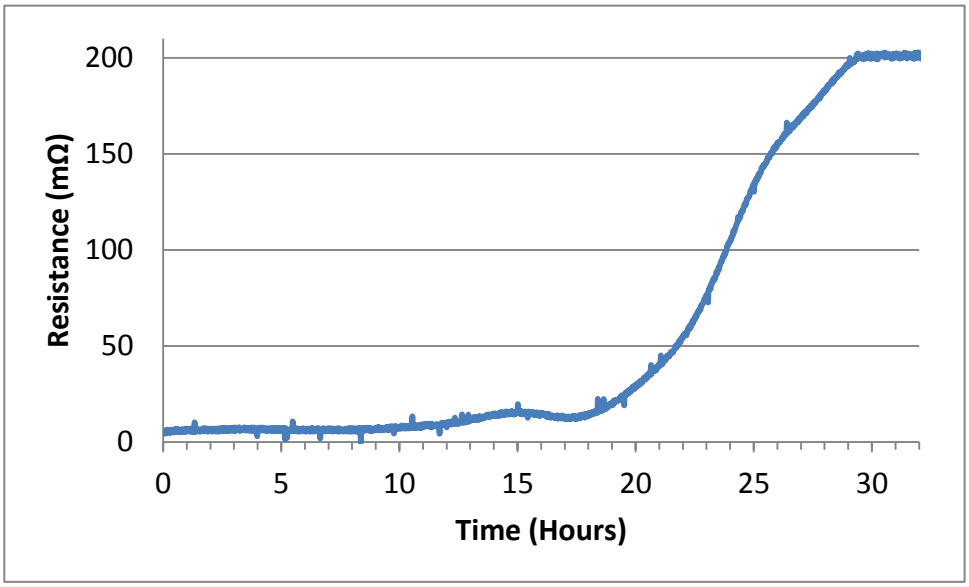


Figure 62: Resistance profile of Mo based test sample

6.3.2 Microstructural Observations

The test sample after being removed from the frame can be seen in Figure 63. It can be seen that the explosion test was quite intense resulting in the shattering of Si die.

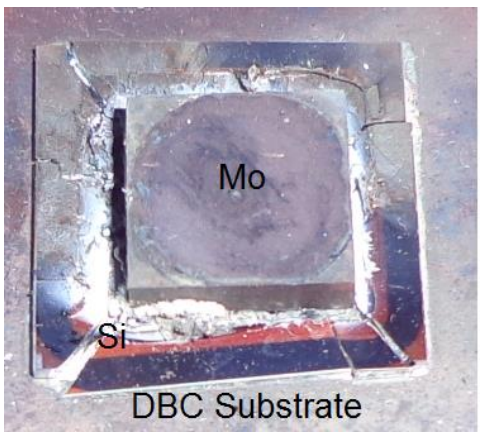


Figure 63: Mo based test sample after passing 50A for 33 Hours.

It should be noted here that the Mo shim was floating as there was no bonding between the Mo shim and the top surface of Si die.

A cross-section of the test sample was prepared and investigated under the SEM and the overall view can be shown in the Figure 64. It can be seen that there is a big void underneath the Mo shim along with some indication of molten Cu, Si, SnAg and Mo. Figure 65 shows SEM images of different areas of cross-section. Figure 65 (a) shows the entire cross-section where area enclosed by red, green and blue rectangles have been further magnified in Figure 65 (b), Figure 65 (d) and Figure 65 (f) respectively. Figure 65 (b) shows a broken piece of Si die underneath which the solidification structure has been formed i.e. Cu has been melted and formed an intermetallic compound with SnAg which can be seen in in detail in Figure 65 (c).

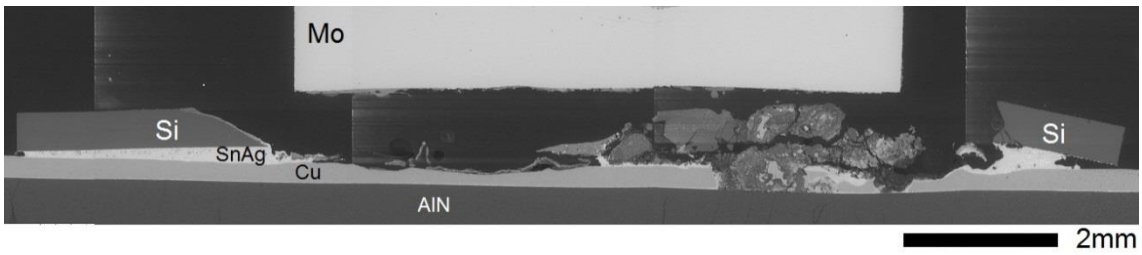


Figure 64: Overview of cross-section of Mo based test sample under SEM

Figure 65 (d) shows another location where solidification structure has been formed with very small pieces of broken Si embedded in the intermetallic compound of Cu and SnAg, whereas Figure 65 (e) is the enlarged view of Figure 65 (d).

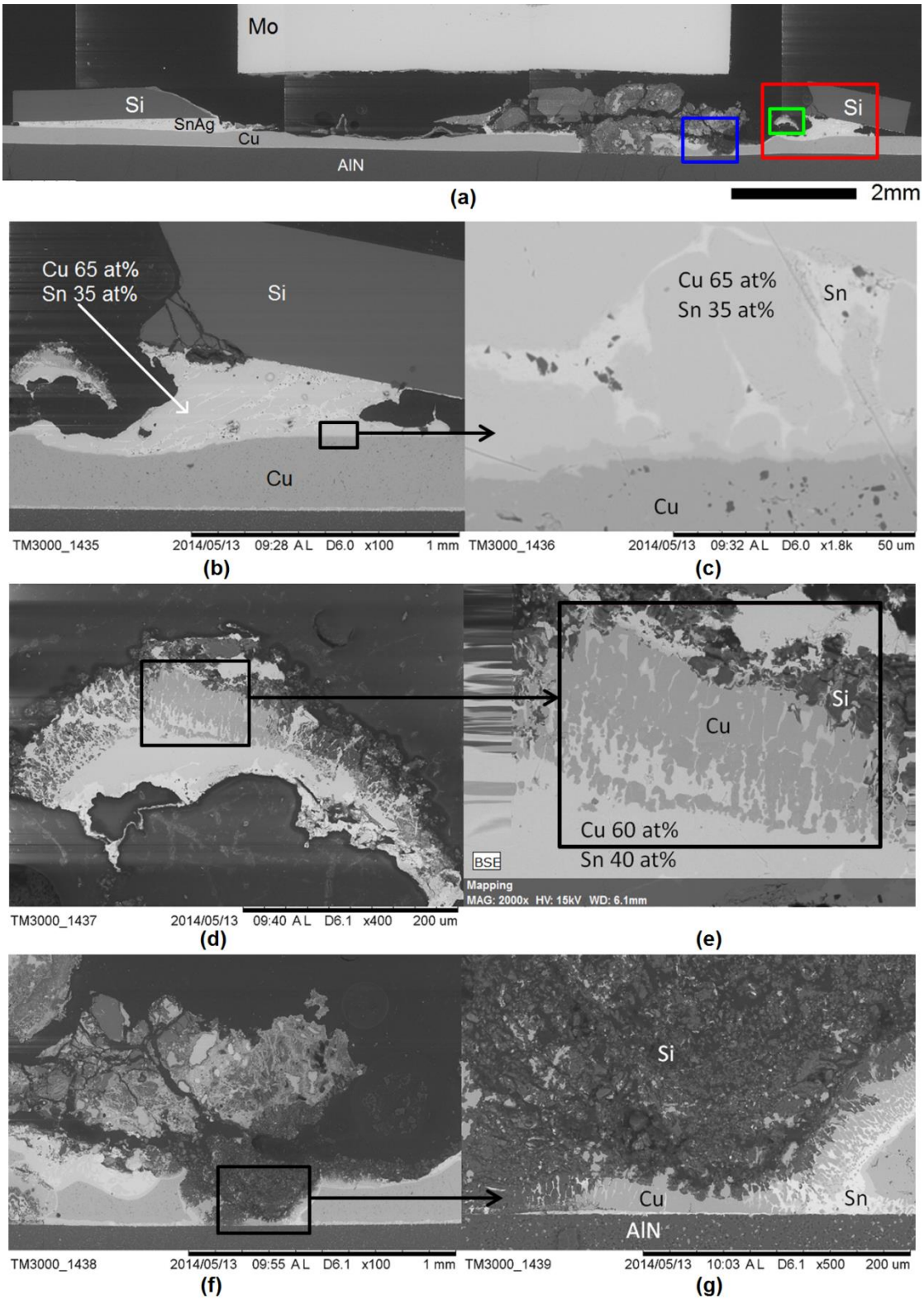


Figure 65: Image showing cross-section of Mo based test vehicle under SEM

Figure 65 (f) also shows very small particles of broken Si at a different location mixed with the complex intermetallic compound resulted from the explosion. Figure 65 (g) is the enlarged view of Figure 65 (f).

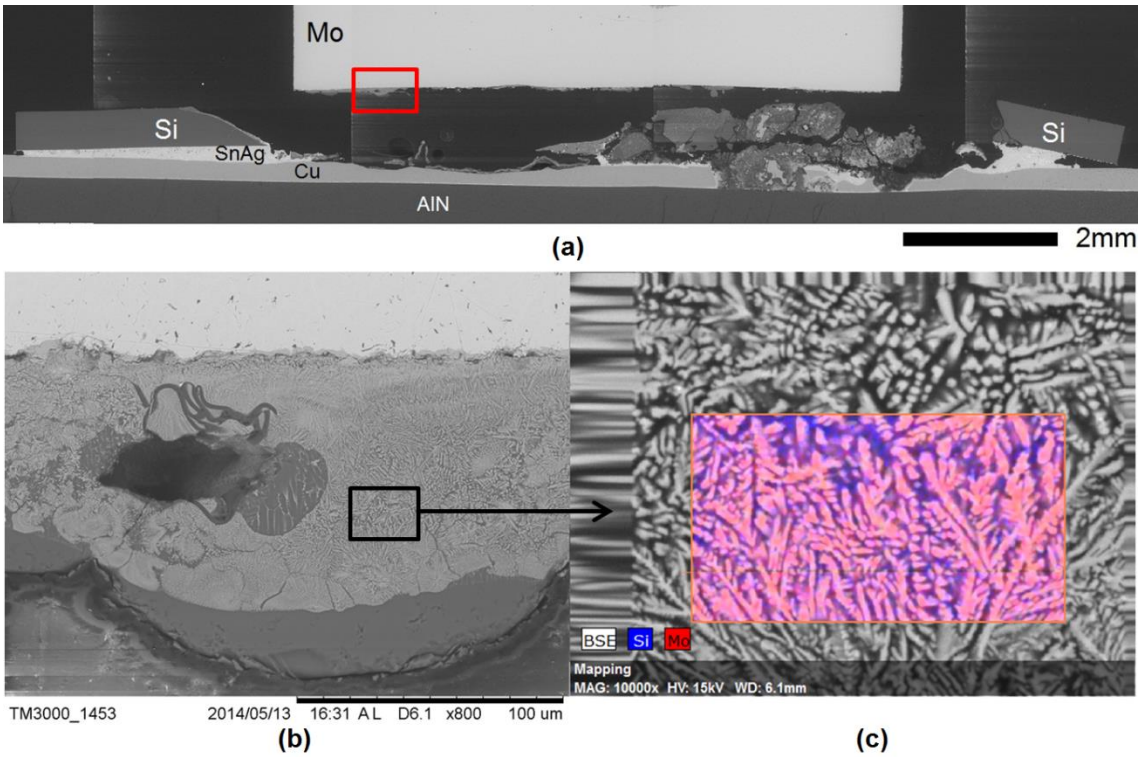


Figure 66: SEM images showing evidence of the intermetallic compound between the Mo and Si

Figure 66 shows the formation of $MoSi_2$ an intermetallic compound with dendritic microstructure between Mo and Si located at the IGBT top and Mo shim interface. Figure 66 (a) shows the whole cross-section, Figure 66 (b) shows the magnified SEM image of the area enclosed by red rectangle in Figure 66 (a) and Figure 66 (c) is further magnification of Figure 66 (b) which clearly shows the EDX element map along with the dendritic microstructure achieved by Mo and Si.

6.4 Discussion

The resistance from the collector to the emitter terminal of the failed test sample is proportional to the contact area between the Mo shim and the emitter side of the device. The more the contact area the lower will be the resistance and vice versa. From the investigation carried out in the previous chapter it was learned that during the explosion test there was production of gas i.e. Cu and some portion of Si changing from solid to gas phase. During this explosion test, the shattering of Si created a void underneath Mo shim as can be seen in Figure 64 and Figure 65 further confirms the rapid formation and release of gas. Despite the formation of the void there was still some contact between the Mo shim and top side of device, resulting in initial resistance of about 5.4mΩ. During the test of passing 50A current through the sample, the area of true contact was further reduced. This resulted in increased contact resistance and heating of the sample, consequently led to local growth of the complex intermetallic compound hence further disturbing the alignment of the Mo shim and as the IMC was very brittle and could not realign itself during the passage of current, finally resulted in the unstable short circuit having 200mΩ resistance. This experiment was repeated two times and the results were similar.

SCFM could not be achieved using Mo shim because it was not compliant i.e. very stiff and could not form suitable intermetallic compounds. One possible solution to address this problem was suggested by the literature review to put an intermediate layer of a compliant and conductive material between Mo shim and the top side of an IGBT e.g. Al or Ag [56, 57]. However, the literature does not provide the comprehensive understanding of the relevant mechanisms and does not include the effect of using other materials besides using Al and Ag. For example the effect of

using Cu as an intermediate metal is very important as there is growing interests in Cu based interconnect technologies in modern power IGBT modules.

The work done in the next chapter tries to develop an understanding of the effect of using various materials which can be used to transform an unstable SCFM to stable SCFM.

6.5 Summary

The Mo based press pack IGBT failed to short circuit with initial contact resistance of 5.4mΩ but it was not stable as its resistance kept on increasing and finally reached 200mΩ after passing 50 A current for 33 hours. The reason for unstable short circuit was formation of brittle intermetallic compound MoSi2 and reduction of the active contact area between Mo shim and the top side of the device. The current passage test caused heat generation which changed the structure/arrangement of the different conductive paths and as the intermetallic was brittle, it could not realign itself and resulted in further reduction in contact area.

7 INVESTIGATION OF SUITABLE MATERIALS FOR ACHIEVING SCFM

7.1 Introduction

In the previous chapter the press pack IGBT structure based test vehicles were tested and it was observed that if Mo shim is used directly in contact with the top side of the IGBT, it results in an unstable short circuit. This issue of the unstable short circuit is addressed in this chapter by placing small foils of different materials which are more compliant between the Mo shim and the top side of the IGBT. After finding out the most suitable material, the minimum required thickness of that material has also been investigated.

7.2 Experiment

7.2.1 Test Vehicle preparation

In this study the method of preparation of samples was similar as described in section 6.2.1 except a small change which is the introduction of a foil of different material between the Mo shim and top of an IGBT. The size of the foil was 8mm × 8mm ×0.5mm (L×B×H). This foil has been introduced to see the relationship between the failure to a stable short circuit and compliance of material. The schematic of the complete test vehicle showing physical location of the material sheet is shown in Figure 67.

Although in theory this test could be conducted with any electrically conductive materials that is more compliant compared to Mo, experimental work was carried out on just four materials Cu, SnAg, Al and Ag. They were selected because their high

electrical conductivity, compliance, low melting temperature and were already being used in the conventional IGBT manufacturing process. For example SnAg has been selected because it is already being used in attaching IGBT die to the substrate, Al is selected because the top metallization layer of most of the IGBT is Al, Cu is selected because in some IGBT modules Cu posts are bonded on top side of an IGBT to make emitter contact and some manufactures have already developed some devices with top metallization layer of Cu. Ag has been used because of its high electrical conductivity, compliance, low melting temperature and some manufacturers have started using Ag nano particle sintering as it is being considered as a more reliable die to substrate bonding medium as compared to soldering.

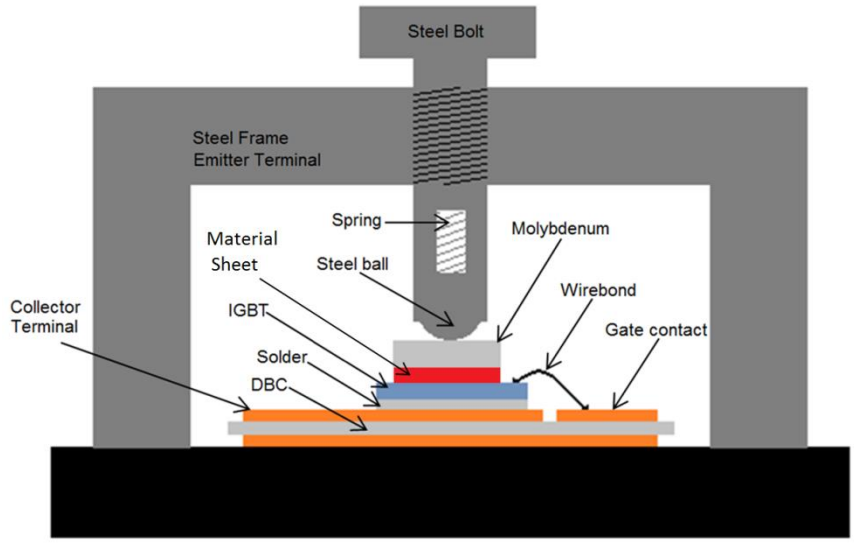


Figure 67: Schematic of test vehicle showing physical location of metal sheet

7.2.2 Test Procedure

7.2.2.1 Explosion Testing

The explosion testing for all of the test samples was carried out at 750J by using a 61.2mF capacitor bank which was charged to 156V. The test samples with different material systems were connected across the capacitor bank and the gate of the IGBT

was triggered enabling all the energy that was stored in the capacitor bank to discharge through the device inducing thermal overload failure to the device.

7.2.2.2 Current Passage Test

After explosion testing, the test samples were subjected to a current passage test. The current was passed through the test samples to see the stability of the short circuit. In this test, a continuous current of 50A was passed through the test sample until it failed to high contact resistance or reached 150 hours i.e. which ever happened first. For samples which resulted in unstable failure to short circuit, the experiments were carried out three times to confirm the test result repeatability.

7.2.3 Sample Cross-section & Analysis

After performing the current passage test, the test samples were removed from the frame. The quick fix glue was applied to the test samples to stop the movement of the Mo shim which was floating (i.e. was not bonded/ attached to the top side of an IGBT). The DBC on which the IGBT was attached was cut by using a diamond saw to the size of the IGBT so that it could be inserted in the resin mould to prepare the cross-section. Each sample was placed inside the resin mould by using a clip and a mixture of resin and hardener was poured on it and moulds were then left overnight to cure. The resin mounted samples were then cut near the approximate location of the failure to make them ready for the grinding. The grinding started off by using the coarser SiC sand paper with the grit size of 400 and gradually moving to 1200 grit size paper. After grinding, the samples were polished first by using 3μm diamond solution and later by using 1μm diamond solution.

The prepared cross sections of the test samples were then analysed by using a Hitachi TM3000 Scanning Electron Microscope (SEM) which had a built in stage of Energy

Dispersive X-ray Spectroscopy (EDX). The EDX was used to identify elemental composition at various positions of interest within the sample.

7.3 Experimental Results

7.3.1 Cu as intermediate material

7.3.1.1 Electrical Results

The Cu based sample was tested at 750 J and the electric current and voltage through and across the device respectively are shown in Figure 68. From the waveforms it can be observed that the test vehicle failed to short circuit because voltage across the device collapsed to zero after explosion.

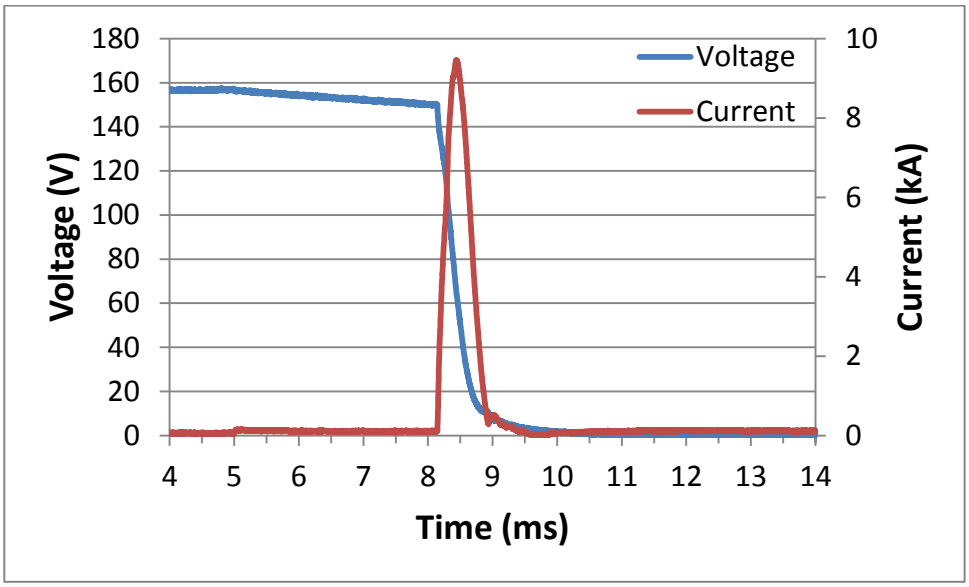


Figure 68: Voltage and current waveforms of Cu based test sample exploded at 750 J

From the Figure 68 it can be seen that the gate signal was applied at 5ms which caused the device to saturate which continued for about 3.142ms and can be seen in the figure as a small blip starting at 5ms. After the saturation region, at approximately

8.142ms the device exploded and the peak current during the explosion reached 9468A at 8.438ms.

Figure 69 shows the electrical contact resistance profile of the failed to short circuit device. During the current passage test, it was observed that the initial resistance of the short circuit was very low i.e. 5.2mΩ which increased with the passage of time reaching 200mΩ in 29 hours which confirmed that it was not a stable short circuit.

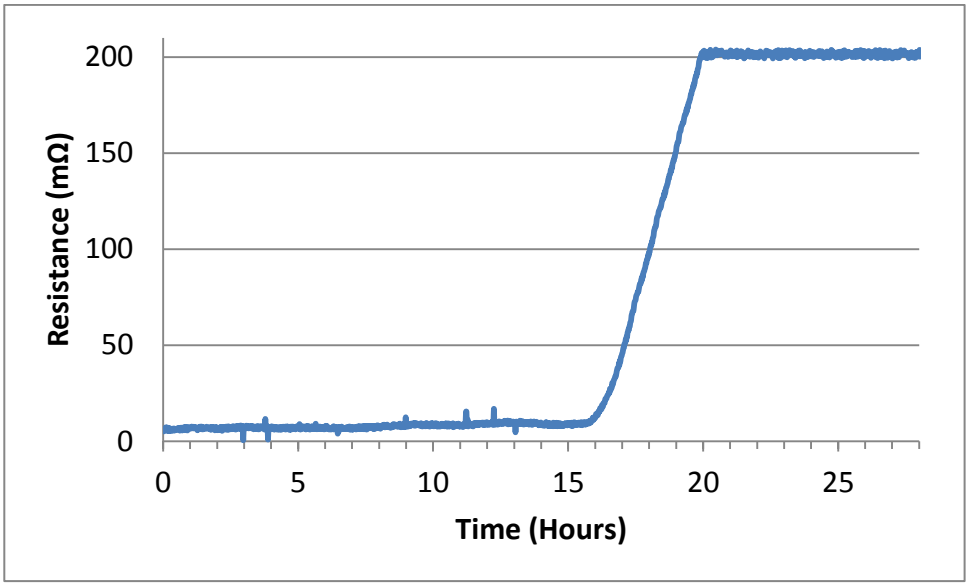


Figure 69: Contact resistance of Cu based test sample

7.3.1.2 Microstructural Observation

Figure 70 shows the photograph taken from the sample. It can be seen that the explosion test was quite intense resulting in the shattering of Si die. It should be noted here that the Mo shim was floating as there was no bonding between the Mo shim and the Cu sheet, similarly there was no bonding between Cu sheet and the top side of the device. During the current passage test, the temperature of the test vehicle went quite high causing oxidation of the Cu sheet which can be seen in Figure 70.

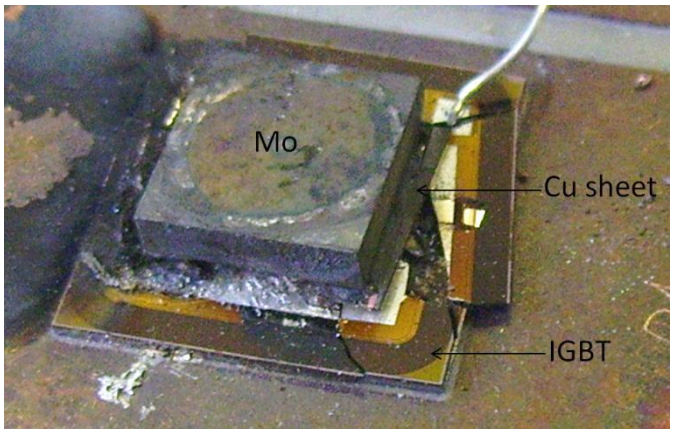


Figure 70: Cu based test sample after passing 50A for 29 Hours

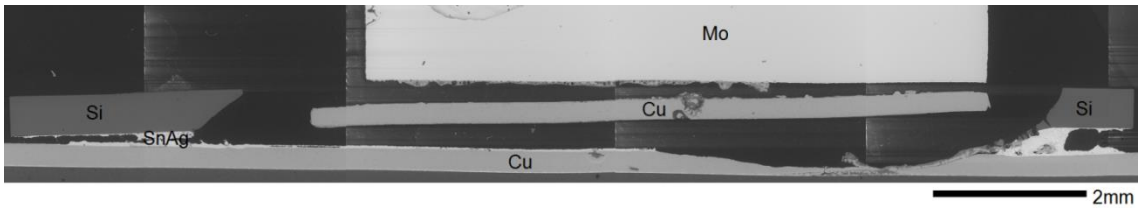


Figure 71: Overview of cross-section of Cu based test sample under SEM

From Figure 71 it can be seen that a large volume of Si die underneath the Cu sheet has been broken and vaporised by the high temperature and the mechanical forces caused by the explosion. It can also be seen that using the Cu as intermediate metal resulted in a poor electrical contact area with the top side of the die. This poor contact area resulted in excess heat generation which caused oxidation of the Cu therefore further reducing the electrical contact area hence further increased the electrical contact resistance.

Figure 72 shows different areas of the cross-section analysed under the SEM. Figure 72 (a) shows the complexity of the heterogeneous solidification structure which was formed after the explosion. It contains broken Si particles mixed with the Si-Cu hypereutectic structure where the Cu is 55 atomic percentage (at%) and Si is 45at% as pointed at by the arrow. Figure 72 (b) is the enlarged view of one portion of Figure 72

(a) where it shows the formation of a rapid solidification structure [62] and Cu-enriched dendrites. The Cu-enriched dendrites have composition approximately of Cu 67at%, Si 28 at% and Sn 3 at%. Based on the Cu-Si phase diagram [61], these dendrites probably are IMC $Cu_{19}Si_6$. The traces of Sn detected here can possibly come from the background noise. The dark phase is pure Si which was formed at the same time as the surrounding $Cu_{19}Si_6$ after the liquid reached the eutectic point. The composition of the brightest phase is close to that of Cu_3Sn while the Si detected there probably comes from the background $Cu_{19}Si_6$ dendrites.

Figure 72 (c) shows a different area of cross-section of the test sample where it shows the Cu sheet which was used as intermediate metal between the Mo shim and the device top. The formation of complex intermetallic compounds at the interface between Mo and Cu sheet can be seen in Figure 72 (d) which is the enlarged view of Figure 72 (c). It was found that there was no formation of any intermetallic compound between Mo and Cu. The Al came from the tri-metal layer on top of the device, and is present in different concentrations at different locations. Based on the Al-Cu-Si ternary phase diagram [63], these intermetallic compounds (IMCS) could possibly be $\theta - AlCu$ and $\eta_2 - AlCu$.

Figure 72 (e) shows a different area of cross-section where different micro-structures formed at the interface between the Mo and the Cu. Figure 72 (f) is the enlarged view of Figure 72 (e) where the solidification structure mixed with original structure in the Cu sheet and some Si particles can be seen. The Si probably came here after the explosion which occurred at a different location causing ejection of broken small pieces of Si into the molten Cu. It can also be seen that the Cu reacted only with the boundary of the Si crystal to form the solidification structure. This is a kind of

dendritic structure consists of a columnar zone next to the Cu side and an equiaxed zone at the edges of the Si particles [63].

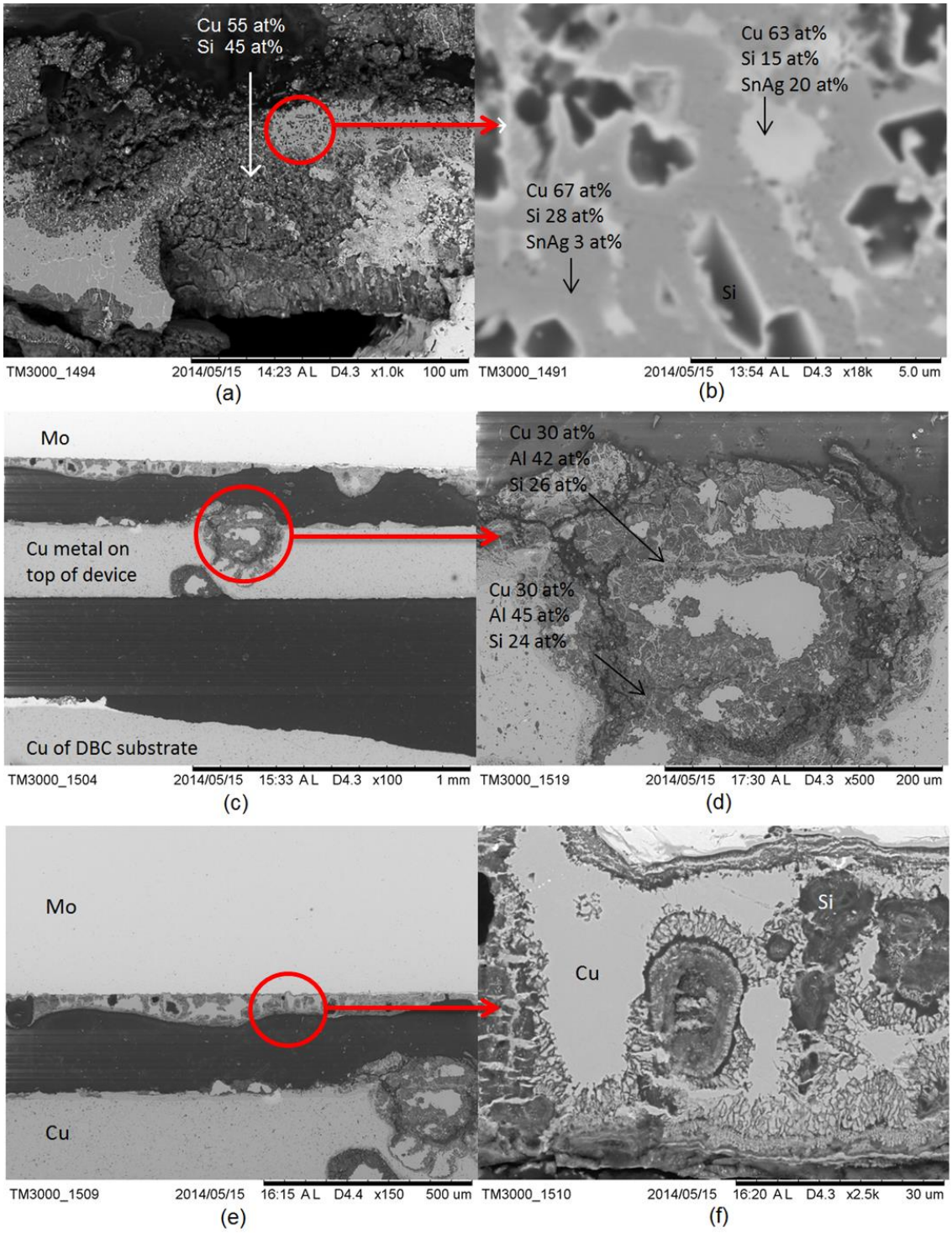


Figure 72: Image showing cross-section of Cu based test vehicle analysed using the SEM

7.3.2 SnAg as intermediate material

7.3.2.1 Electrical Results

Figure 73 shows the electric current and voltage waveforms of SnAg based test sample which was tested at 750 J. From the waveforms it can be observed that the test vehicle failed to short circuit because voltage across the device went to zero after test. The gate signal was applied to the device at 5ms which caused the device to go into the saturation region which persisted for approximately 3.136ms after which the device failed causing the flow of huge current which reached its peak value 6230A at 8.424ms.

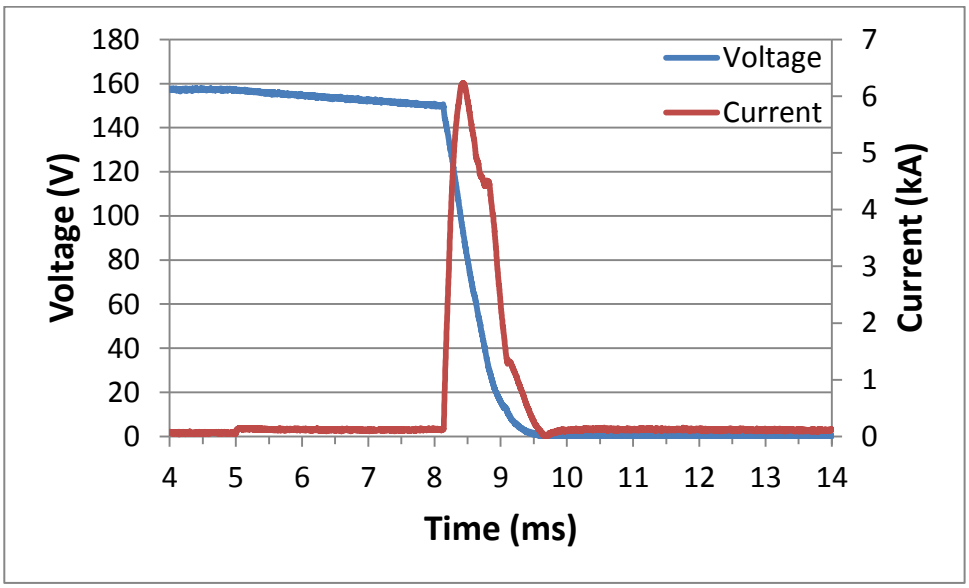


Figure 73: Voltage and current waveforms of SnAg based test sample exploded at 750 J

Figure 74 shows the electrical contact resistance of test sample. It shows that the initial resistance of the short circuit was 16mΩ which decreased to 14.15 mΩ after 150 hours which implies that it was a stable short circuit.

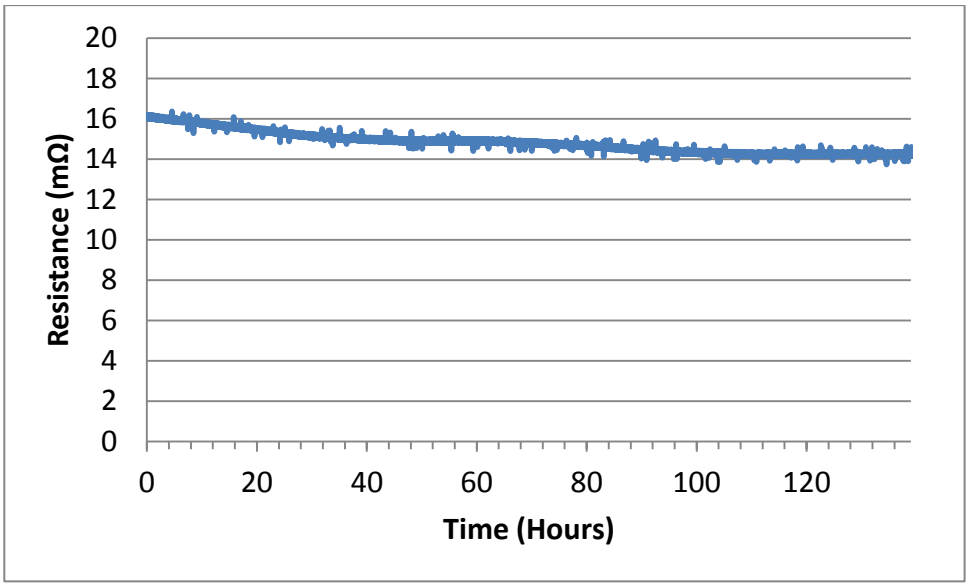


Figure 74: Contact resistance of SnAg based test sample

7.3.2.2 Microstructural Observation

Figure 75 shows the SnAg based test sample after the current passage test. The explosion test was quite extreme and broke the Si die. The SnAg sheet which is under the Mo shim has re-solidified which shows that it has reached at least 221°C temperature. It can also be seen that the explosion emitted some molten mixture of different metals in the form of a splash which can be seen on DBC.

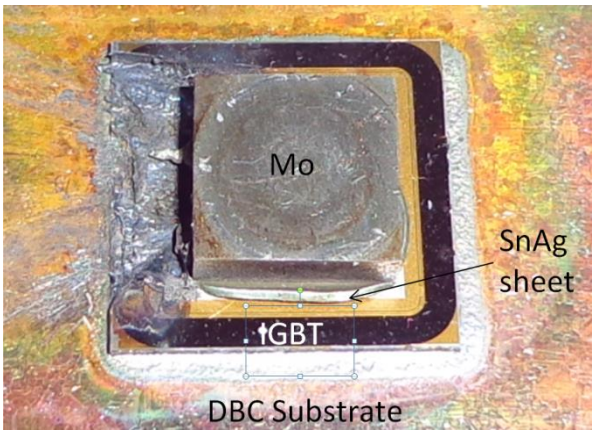


Figure 75: SnAg based test sample after passing 50A for 140 Hours

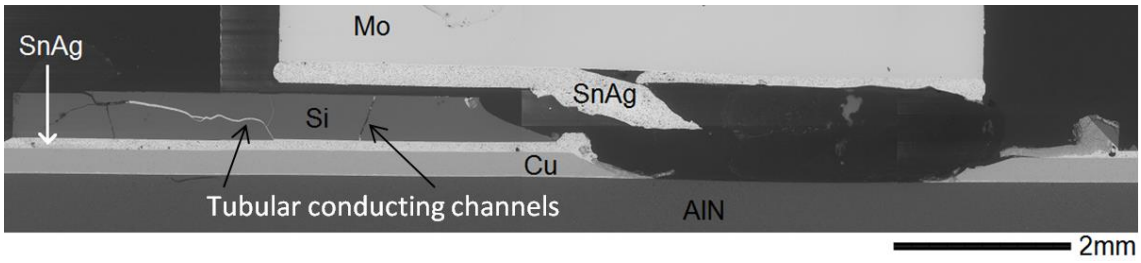


Figure 76: Overview of cross-section of SnAg based test sample under SEM

Figure 76 shows the cross-section view of the test sample. It can also be seen that half of the IGBT device has disappeared due to the explosion. The formation of a small tubular conducting channel can also be seen here which electrically connects the top of the device i.e. emitter to the bottom of the device i.e. collector. These features are probably formed by the capillary action of the molten SnAg which filled the gap between the broken pieces of Si during explosion.

Figure 77 shows different areas of cross-section under the SEM. Figure 77(a) shows the interface between the Sn and the Cu of the DBC substrate. The Cu reacted with the Sn to form intermetallic compounds. The most likely sequence of events here was; first the Cu reacted with the molten Sn to form a supersaturated solution of Cu in Sn which led to the formation of a scallop type Cu_6Sn_5structure at the interface which can be seen in Figure 77(b) and Cu_3Sn was formed between the Cu_6Sn_5 and Cu due to the diffusion and reaction type growth.

Figure 77(c) shows another area of cross section of the test sample where large needle like Si particles can be seen on the top side which becomes finer and finer as it moves along towards the bottom. The gradient of the particle size distribution shows that the bottom part of the structure cooled very rapidly resulting in formation of fine particles of Si as compared to the relatively slow cooling on the top resulting in large particles. The rapid cooling of the bottom side was due to the thermal conduction i.e. heat transfer towards the DBC as compared to air conduction on the top side which caused

slow cooling. The composition at point A is around Si 65 atomic percentage (at%), Cu 30 at% and Sn is 5at% and Point 'B' is a broken piece of the pure Si.

Figure 77(d) is the enlarged view of Figure 77(c) which shows the microstructure in detail. Here, during the solidification process the dark phase of Si crystals shown in point 'C' in Figure 77(d) solidified first. Once the residual liquid reached to the eutectic point, Si-Cu eutectic consisting of $Cu_{19}Si_6$ intermetallic compound shown in point 'A' in Figure 77(d) and the small Si crystals (point 'D') surrounding the large Si crystals were formed.

Figure 77(e) shows a different cross section area of the test sample which highlights the formation of the Sn rich conducting channels which connects the top side of the device i.e. emitter electrode to the bottom side of the device i.e. collector electrode. The size of these channels is very small hence their contribution towards low resistance might not be appreciable. However, the formation of such channels probably suggests that the liquid Sn or liquid Cu-Sn mixture wetted the walls of the crater in a better way with this material system as compared to the Mo and Cu based test samples where the crater formed after the explosion was less conductive.

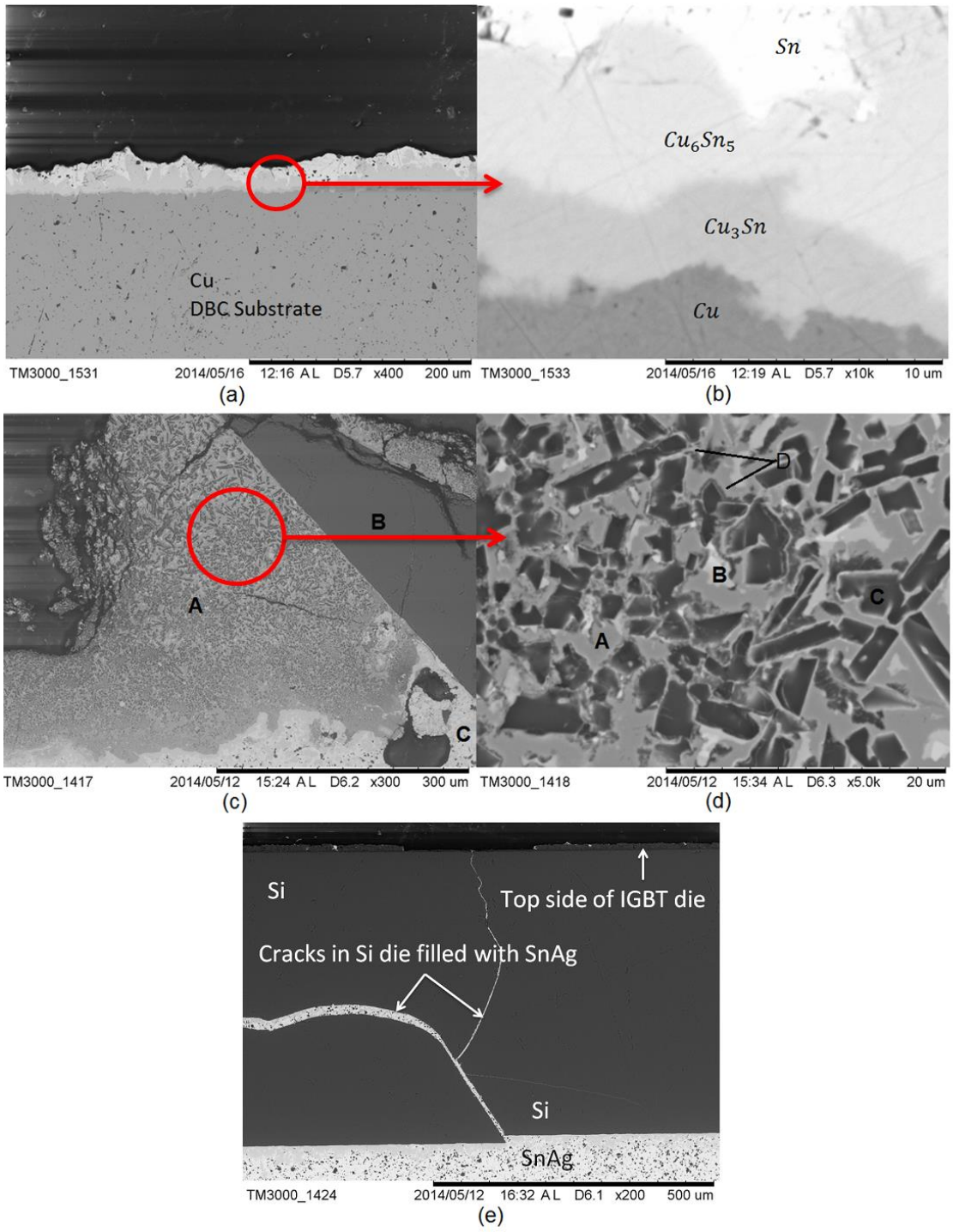


Figure 77: SEM images showing cross-section of SnAg based test vehicle

7.3.3 Al as intermediate material

7.3.3.1 Electrical Results

The Al based sample was tested at 750 J and the electric current and voltage through and across the device respectively are shown in Figure 78. From the waveforms it can be observed that the test sample failed to short circuit because voltage across the device collapsed to zero after explosion. From the Figure 78 it can be seen that the gate signal was applied at 5ms which caused the device to saturate which persisted for about 3.176ms. After saturation, at approximately 8.176ms the device exploded and the peak current during the explosion reached approximately 7876A at 8.44ms.

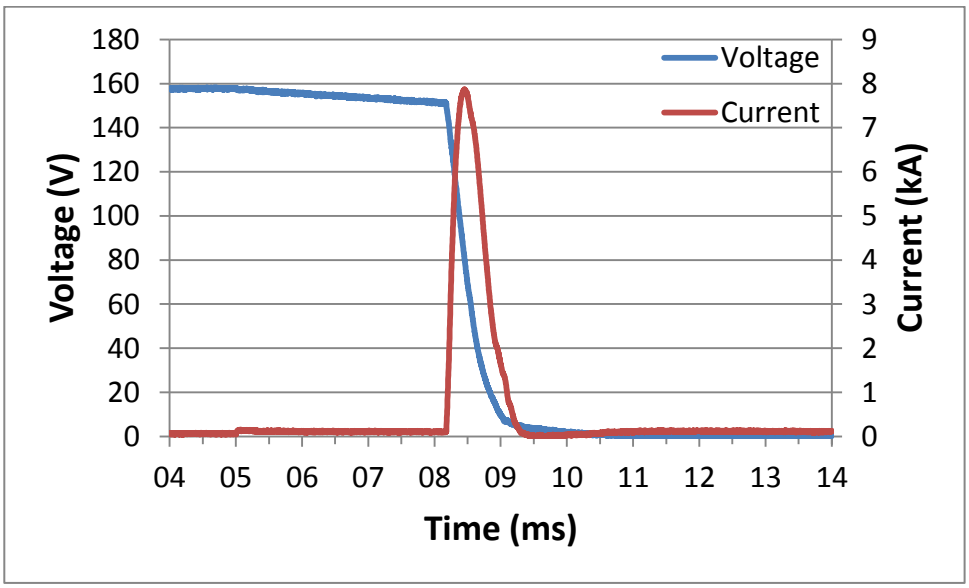


Figure 78: Voltage and current waveforms of Al based test sample exploded at 750 J

Figure 79 shows the electrical resistance profile of the failed to short circuit device. During the current passage test, it was observed that the initial resistance of the short circuit was 30mΩ which decreased to 23 mΩ after 150 hours which implies that it was a stable short circuit.

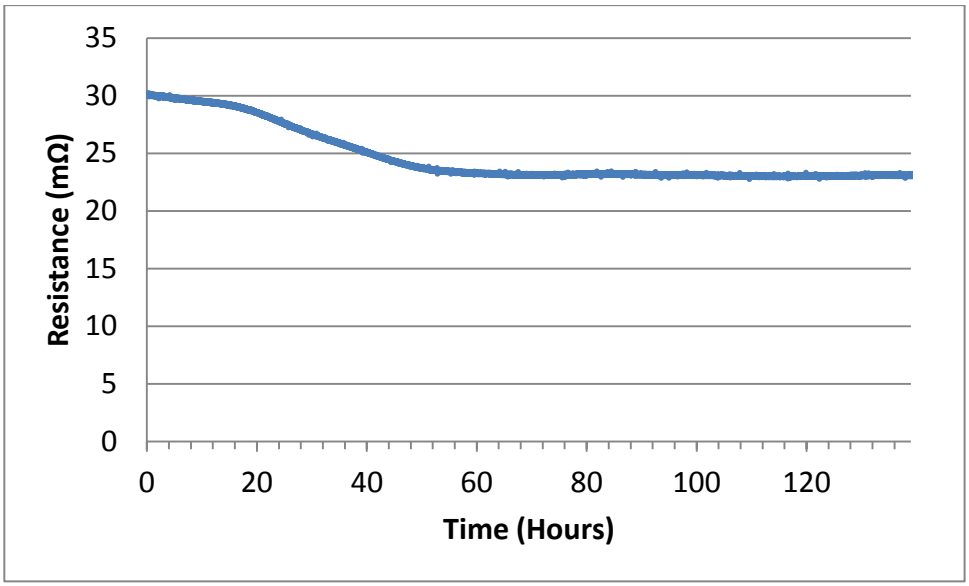


Figure 79: Contact resistance of Al based test sample

7.3.3.2 Microstructural Observation

Figure 80 shows the photograph of the test sample after the current passage test. It can be seen that the explosion test was quite intense resulted in the emission of molten Si and Al which coated the DBC with a greyish black powder which can be seen at the top. It should be noted here that both the Mo shim and the Al sheet were floating as there was no bonding between the Mo shim, Al sheet and the top surface of Si die. It can also be seen that the SnAg solder has been squeezed out from under the IGBT due to the pressure and temperature.

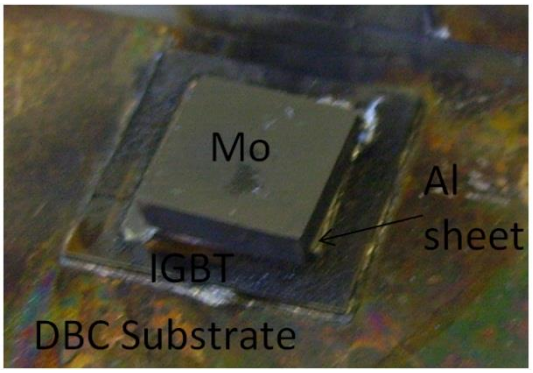


Figure 80: Al based test sample after passing 50A for 150 Hours

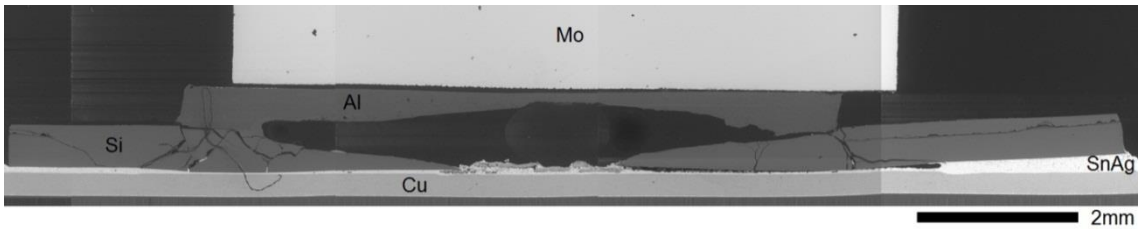


Figure 81: Overview of cross-section of Al based test sample under SEM

From Figure 81 it can be seen that a fair portion of the Si underneath the Al sheet has been broken and ejected out of the test sample by the mechanical force caused by the explosion. Overall it can be seen that there is a good contact area of the Al sheet with the top side of the device. The small tubular conducting channels can also be seen throughout the structure.

Figure 82 shows different areas of the cross-section of the test sample. Figure 82(a) shows the solidification structure at the interface between the Al and the Si seen under the SEM. In the top left corner is the pure Al, bottom left is the pure Si and on the middle right is the intermetallic compound of Al & Si where the composition varies from Al 70 atomic percentage (at%) Si 30 at% to Al 60 at% Si 40 at%. It is very hard to produce high contrast images with the elements separated by a unit of atomic number and it is similar in the case of this SEM image as the Al and the Si are next to each other on the periodic table. Figure 82(b) shows the same area of cross-section under the optical microscope where the solidification structure can be seen more easily as compared to the SEM image.

To develop further understanding of the microstructure and to get a better contrast between the Al and the Si, the cross-section was analysed using focused ion beam (FIB) equipment. Figure 82(c) shows the FIB images of the Al & Si solidification site whereas, Figure 82(d) is the enlarged view of Figure 82(c) in which the eutectic structure between Al & Si can be seen.

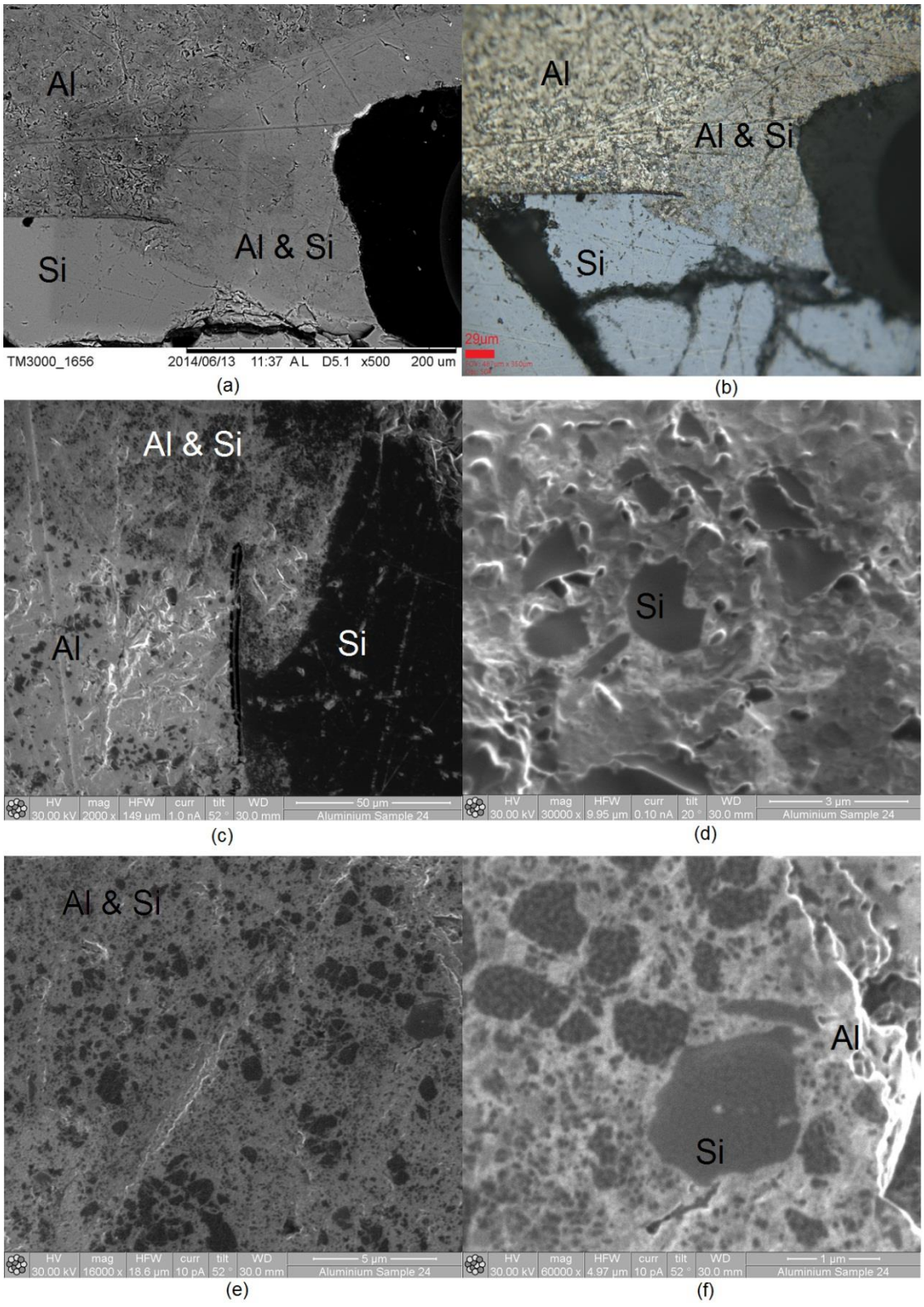


Figure 82: Image showing cross-section of Al based test vehicle under (a) SEM, (b) Optical microscope, (c), (d), (e) and (f) under FIB

To reveal the microstructure and to make it clearer, ion milling was performed which cleared the smudge that occurred on the surface of the moulded sample during the polishing phase. The FIB image taken after the ion milling can be shown in the Figure 82(e) whereas, Figure 82(f) is the enlarged view of the Figure 82(e) in which the eutectic structure between the Al and Si can be clearly seen.

7.3.4 Ag as intermediate material

7.3.4.1 Electrical Results

Figure 83 shows the electric current and voltage waveforms of Ag based test sample which was tested at 750 J. From the waveforms it can be observed that the test vehicle failed to short circuit because voltage across the device collapsed to zero after test. The gate signal was applied to the device at 5ms which caused the device to go into saturation region which persisted for approximately 3.42ms after which the device failed followed by a huge current passing through the failed device which reached its peak value of 10334A at 8.76ms.

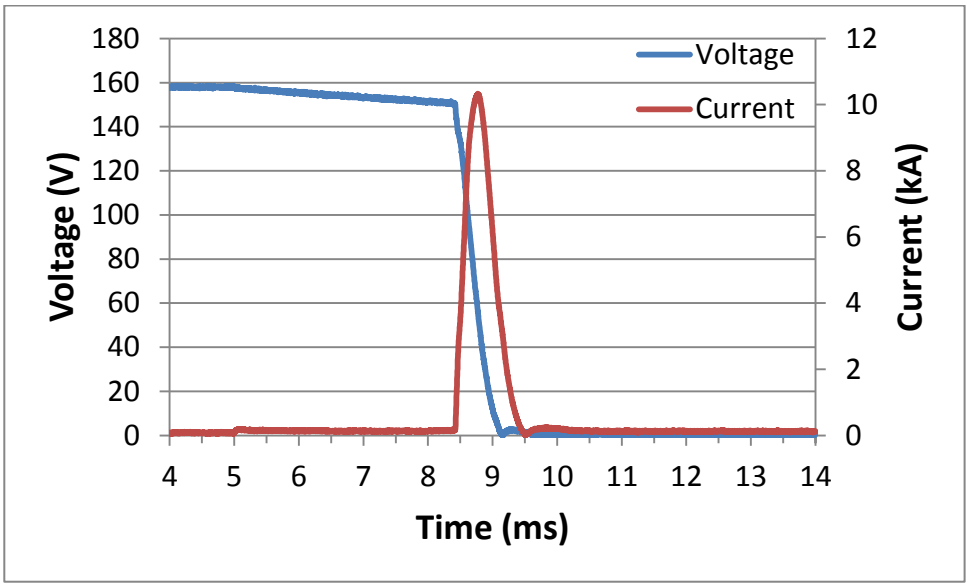


Figure 83: Voltage and current waveforms of Ag based test sample exploded at 750 J

Figure 84 shows the electrical contact resistance profile of the test sample where the initial resistance of the short circuit was 1.5mΩ which increased to 1.76 mΩ after 150 hours which implies that it was a stable short circuit.

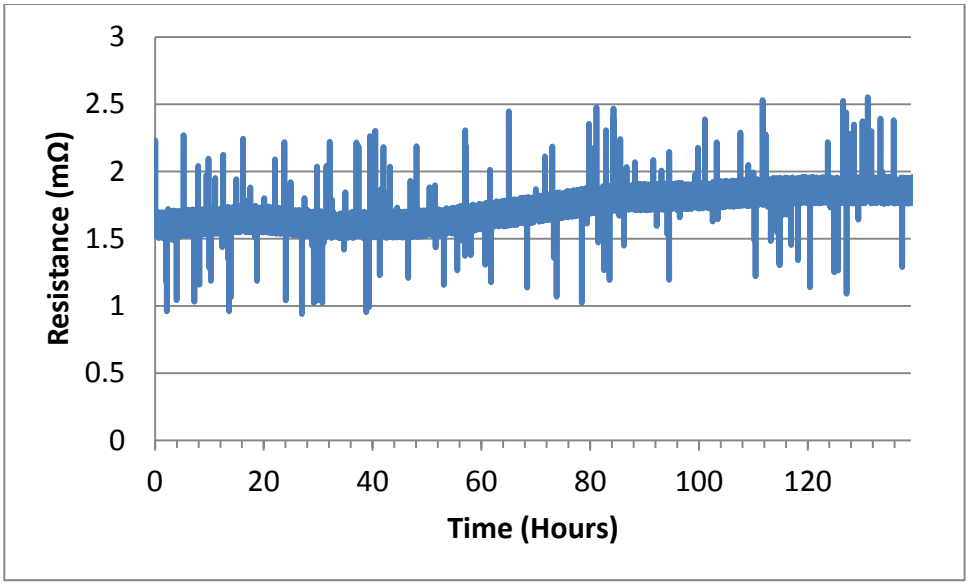


Figure 84: Contact resistance of Ag based test sample

7.3.4.2 Microstructural Observation

Figure 85 shows the photograph of the Ag based test sample. It can be seen that the explosion test was quite powerful resulting in the shattering of the Si die. It can also be seen that the explosion emitted a molten mixture of different metals in the form of a splash which can be seen on the DBC.

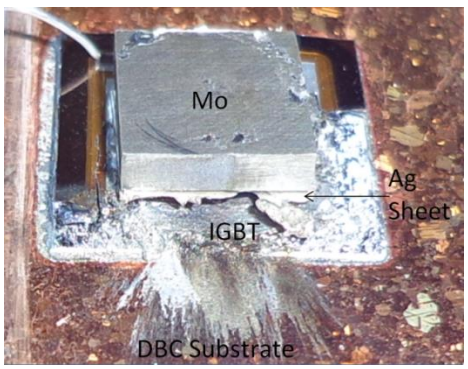


Figure 85: Ag based test sample after passing 50A for 150 Hours

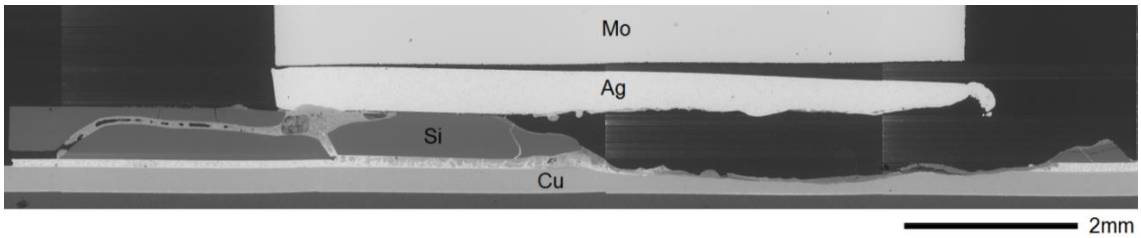


Figure 86: Overview of cross-section of Ag based test sample under SEM

Figure 86 shows the overall cross sectional view of the test sample. It can be seen that half of the IGBT device and some Cu from the DBC has disappeared due to the high temperature and mechanical force involved in the explosion. A solidification structure can be seen at the interface between the Ag sheet and the top side of the device i.e. the bottom left corner of the Ag sheet has melted along with the Si resulting in a formation of a large conducting channel which electrically connects the top of the device i.e. emitter to the bottom of the device i.e. collector.

Figure 87 shows different areas of cross-section under the SEM. Figure 87(a) shows the solidification structure formed at the interface between the Ag sheet and device top. Figure 87(b) shows the enlarged view of Figure 87(a), particularly the area near the Ag-Si interface where the eutectic structure between Ag & Si can be clearly seen. It also clearly shows the dendritic structure of Si which is a dark phase whereas between the Si dendrites the bright silver phase formed a connective network. Some very small grains of Si can also be seen from which it can be inferred that the cooling time was very rapid.

Figure 87(c) shows a different location of the cross section where the Ag-Si eutectic structure can also be seen. Figure 87(d) is the enlarged view of Figure 87(c) where the Si dendrites can be seen. This area has a higher percentage of Si but still the Ag is providing a connective network.

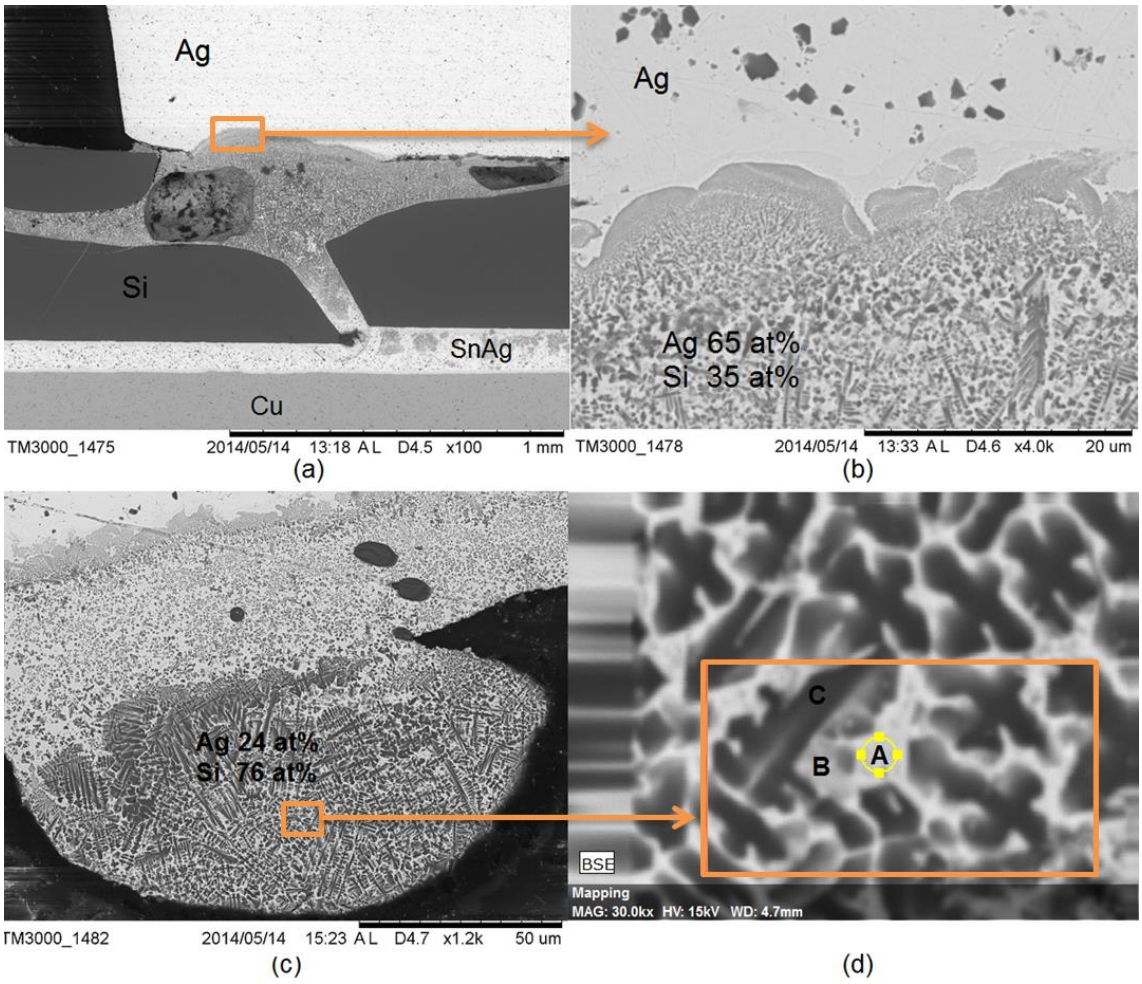


Figure 87: Image showing cross-section of Ag based test vehicle under SEM

7.4 Discussion

7.4.1 Comparison of the Electrical Test Results

Table 5 shows a comparison of the peak current and saturation time of test samples using different kinds of intermediate metals. It can be seen that during the explosion, the highest peak current of 10.33 kA was achieved by using Ag as the intermediate metal. The lowest peak current of 6.23 kA was achieved by using a SnAg preform. The saturation times of all the test samples were very close to each other and were in the range of 3.15ms to 3.4ms. One possible reason for this is that all the experiments

were very similar and the only difference was the use of different kind of intermediate metals.

Intermediate Metal	Thermal Conductivity $W.m^{-1}.K^{-1}$	Electrical Resistivity nΩ.m [64]	Saturation time (ms)	Peak current (kA)
Mo	137 [64]	53	3.20	9.63
Cu	397 [64]	15.8	3.14	9.46
SnAg	86.6 [65]	123	3.13	6.23
Al	238 [64]	26.1	3.17	7.87
Ag	425 [64]	14.7	3.42	10.33

Table 5: Saturation time and peak current of test samples

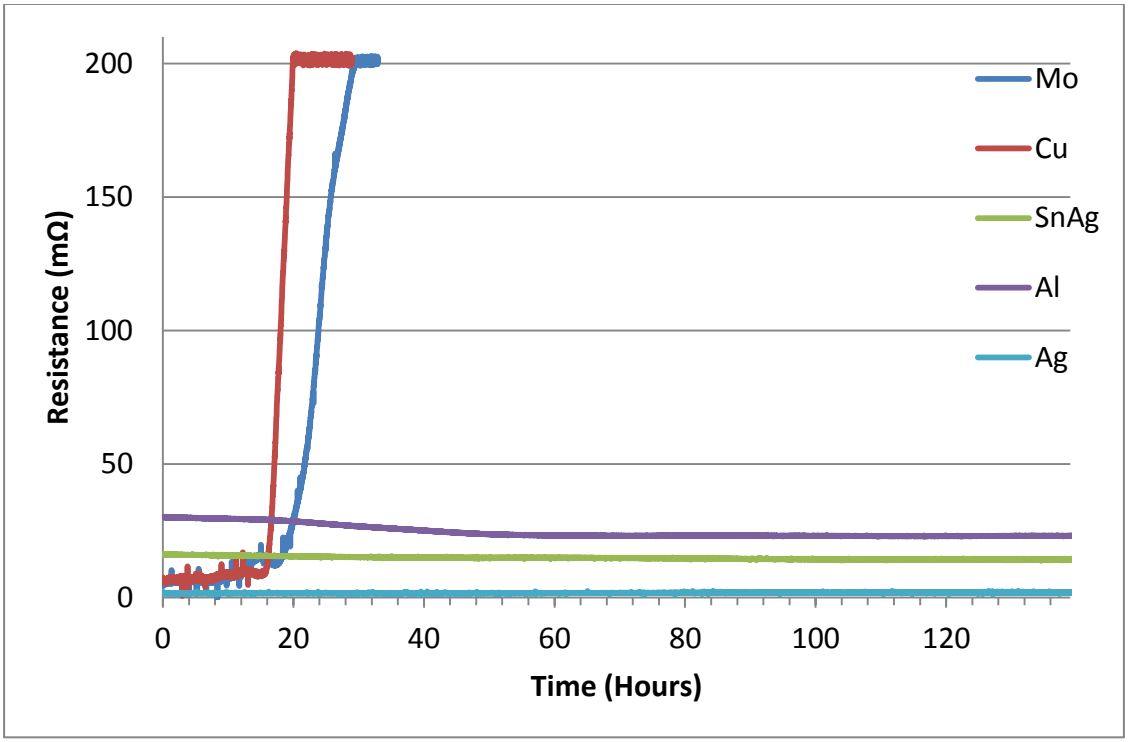


Figure 88: Resistance profile of Mo, Cu, SnAg, Al and Ag.

Figure 88 shows the comparison of the electrical contact resistance profile of the test samples made by using different intermediate metals. After failure to short circuit, the Mo based test sample had an initial resistance of 5.4mΩ but it went on increasing until it reached 200mΩ after 33 hours of the current passage test. The actual final resistance could be much more but the high current power supply that was used was configured to deliver 50A @ 10V so by the time it reached 200 mΩ, it took the power supply into constant voltage mode and hence ended up with the maximum measurable resistance of 200mΩ. From the resistance profile of Mo it can be seen that the contact resistance was stable for first 17 hours but after that it increased swiftly and reached the highest value of 200mΩ after 28 hours and resided there for 5 hours after which it was decided to stop the current passage test because the contact resistance was too high.

The Cu based test sample failed to short circuit with quite low initial resistance i.e. 5.2 mΩ but during the current passage test it eventually reached 200 mΩ after 18 hours resulting in an unstable short circuit. The resistance was stable for 15 hours but then it exponentially increased reaching 200mΩ in 4 hours and then it stayed there for 10 hours with no change hence it was decided to stop the current passage test. The use of Cu as intermediate metal was of great interest because copper bumps are being used in manufacturing planer power IGBT modules hence to further confirm the result, this experiment was repeated three times and each time it failed to initial low resistance short circuit which transformed to unstable short circuit after performing a current passage test.

The SnAg preform based test sample failed to a stable short circuit. The resistance of the SnAg based test sample was very stable with an initial start of 16mΩ which finally reached 14.15mΩ after 120 hours and stayed there unchanging for another 20 hours. It

can be seen that the resistance of the sample slowly and gradually decreased indicating that it was quite stable.

The Al based test sample resulted in the initial contact resistance of 30mΩ which was relatively higher than the rest of the intermediate materials used. It was expected to have lower contact resistance at least compared to SnAg because of the difference in the electrical resistivity of both of them. However, because the Al is very reactive, there is always a very thin and dense layer of Alumina (around 10μm) once Al is exposed to air. The Alumina which is a very good insulator even if it is very thin may have contributed to the increase in contact resistance. Another possibility is the poor wettability of liquid aluminium because of surface oxides which resulted in reduction in the true contact area between Al and device top. Figure 88 shows that the contact resistance was stable for the initial 17 hours and then it started decreasing and reached 23mΩ after 58 hours and then it stayed unchanged for 92 hours indicating its stability.

The lowest initial contact resistance was with Ag which started at 1.5mΩ and slightly increased to 1.76mΩ after 150 hours. It can be seen in Figure 88 that there was a very slight change in the resistance throughout 150 hours which indicates that it was very stable. Ag resulted in the lowest contact resistance because it is the best electrical conductor, less reactive and very compliant. Therefore, Ag fulfilled all criteria that were required to have a stable SCFM.

Intermediate Metal	Time (Hrs)	Initial Resistance (mΩ)	Final Resistance (mΩ)	Electrical Resistivity nΩ.m [64]	Result Stable/unstable short circuit
Mo	33	5.4	200	53	Unstable
Cu	29	5.2	200	15.8	Unstable
SnAg	150	16	14.15	123	Stable
Al	150	30	23	26.1	Stable
Ag	150	1.5	1.76	14.7	Stable

Table 6: Summary of contact resistance profile using different intermediate metals

Table 6 shows the summary of the contact resistance profile using different materials. From the analysis of experimental data it can be very safely said that from the point of view of the material SnAg, Al and Ag all resulted in a stable failure to short circuit but amongst all, Ag was the best candidate as it resulted into most stable failure to short circuit with the minimum electrical contact resistance.

7.4.2 Comparison of Material Properties

Table 7 shows a comparison of the physical properties of the materials. The materials which failed to unstable short circuit i.e. Mo and Cu had a high Young's modulus, Yield strength, Hardness and Melting point as compared to the materials which failed to stable short circuit. The Yield strength or proof strength is the minimum stress value which causes the plastic deformation in a given material. Now during the explosion test, these intermediate materials undergo a large amount of stress which plastically deforms the intermediate material and if its yield strength is high, it would be very difficult to deform it as compared to the intermediate material which has a low

yield strength and that is highly likely to be one of the reasons which caused stable failure to short circuit by using SnAg, Al, and Ag.

Intermediate Material	Young's Modulus (GPa)	Yield Strength (MPa) @ 25°C	Hardness Vickers HV	Melting point °C
Mo	325 [66]	415 [66]	200 [66]	2621 [66]
Cu	129.8 [66]	69 [66]	51.5 [66]	1084 [66]
SnAg	37 [67]	48.8 [68]	15.7 [66]	221 [66]
Al	69 [66]	12 [66]	20 [66]	660 [66]
Ag	82.7 [66]	54 [66]	25 [66]	961.7 [66]

Table 7: Physical properties of annealed materials

It is not surprising to also correlate the stability of the failure with melting point of the intermediate material. This is because generally the higher the melting point, the more stable will be the structure of the material which generally corresponds to higher Young's modulus, Yield strength and hardness of the material.

In the case of Ag, all the right properties of the material were there which resulted in the most stable failure to short circuit mode.

7.4.3 Comparison of Microstructural Observations

In the microstructural observation of all the test samples, the formation of rapid solidification microstructures was very common. This includes the broken small pieces of silicon embedded into the matrix which consists of intermetallic compounds (IMC) of Mo, Cu, Cu-Sn, Al and Ag, dendritic structures of Mo-Si, Cu-Si and eutectic structures of Mo-Si, Cu-Si, Ag-Si, Al-Si.

In the case of the Mo, formation of the IMC between Mo & Si can be seen in Figure 66. When EDX was performed, it suggested that the composition of the eutectic was Si 80 atomic percentage (at%) and Mo 20at%. Referring to the phase diagram (shown in Figure 89), It can be inferred that Mo & Si reached a phase called Molybdenum di-silicide ($MoSi_2$) which is a hypo-eutectic structure where the molten Mo solidified

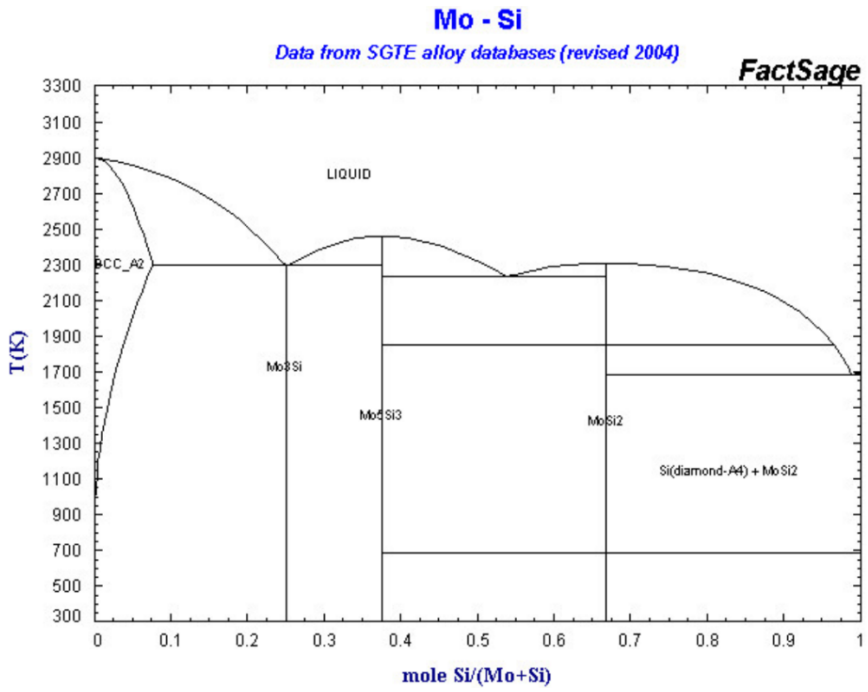


Figure 89: Phase diagram of Mo-Si [61]

first to form the Mo dendrites and then Si solidified between the Mo dendrites. $MoSi_2$ is a conductive alloy with very high Young's Modulus [66]. It can also be seen on the phase diagram that a temperature of approximately 2200 K was achieved during explosion causing the phase change from the solidus to the liquidus of both materials.

The microstructural analysis of Cu revealed the formation of an IMC between Cu-Si and their random quantitative distribution throughout the sample. The EDX of the different areas of the cross-section shows that the Cu-Si structures have composition ranging from Cu 55 atomic percentage (at%) Si 45at% (Figure 72(a)) to Cu 83at% Si

16at% (Figure 72(f)). The phase diagram of Cu-Si (Figure 90) suggests the possibility of the formation of different phases e.g.$Cu_{33}Si_7$, $Cu_{15}Si_4$, $Cu_{19}Si_6$ and $Cu_{19}Si_6 + Si$. It can also be seen on the phase diagram that a minimum temperature of approximately 1400 K was achieved during the explosion for the formation of Si 55at% Cu 45at%.

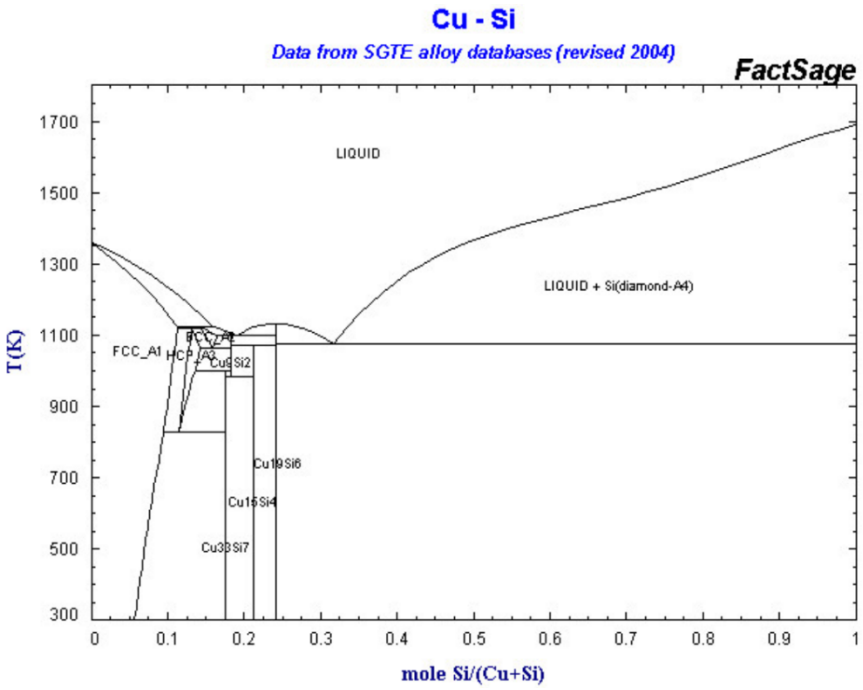


Figure 90: Phase diagram of Cu-Si [61]

In the SnAg based sample, if the microstructure at the interface between the SnAg and the Cu layer of the DBC substrate is examined, the formation of classic Cu-Sn intermetallic compounds e.g. Cu_6Sn_5 Cu_3Sn which can be seen as shown in Figure 77(b). Besides that, the formation of the Cu-Si intermetallic compound observed in Figure 77(c), the composition at point A is around Si 65 atomic percentage (at%), Cu 30 at% and Sn is 5at% and according to the phase diagram of Cu-Si which is shown in Figure 90 it is a hyper-eutectic Cu-Si structure in which the large black Si crystals started to solidify approximately at 1450 K.

The cross-section of the Al based sample is shown in Figure 82, where the formation of a eutectic structure between Al & Si can be seen. The composition of the eutectic structure was Al 60 at% Si 40 at%. The formation of some very small grains whose size is in the range of nano-meters can also be seen in Figure 82(f) which suggests that the cooling rate in the case of Al was extremely rapid.

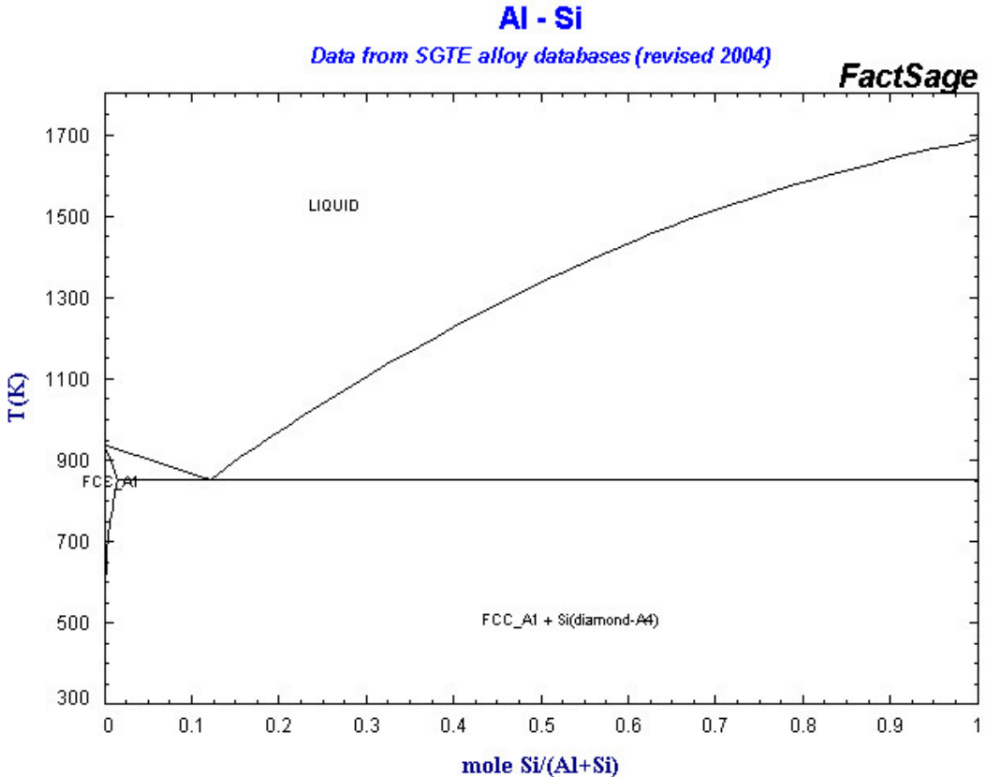


Figure 91: Phase diagram of Al-Si [61]

Phase diagram of Al-Si (Figure 91) suggests that it is a hyper-eutectic structure in which the Si solidified first to form black phase Si crystals (Figure 82(f)) and then it finally reached the eutectic point with the decrease in temperature. From the phase diagram, it can be seen that Si in Si 60 at% Al 40 at% started to solidify at approximately 1420 K.

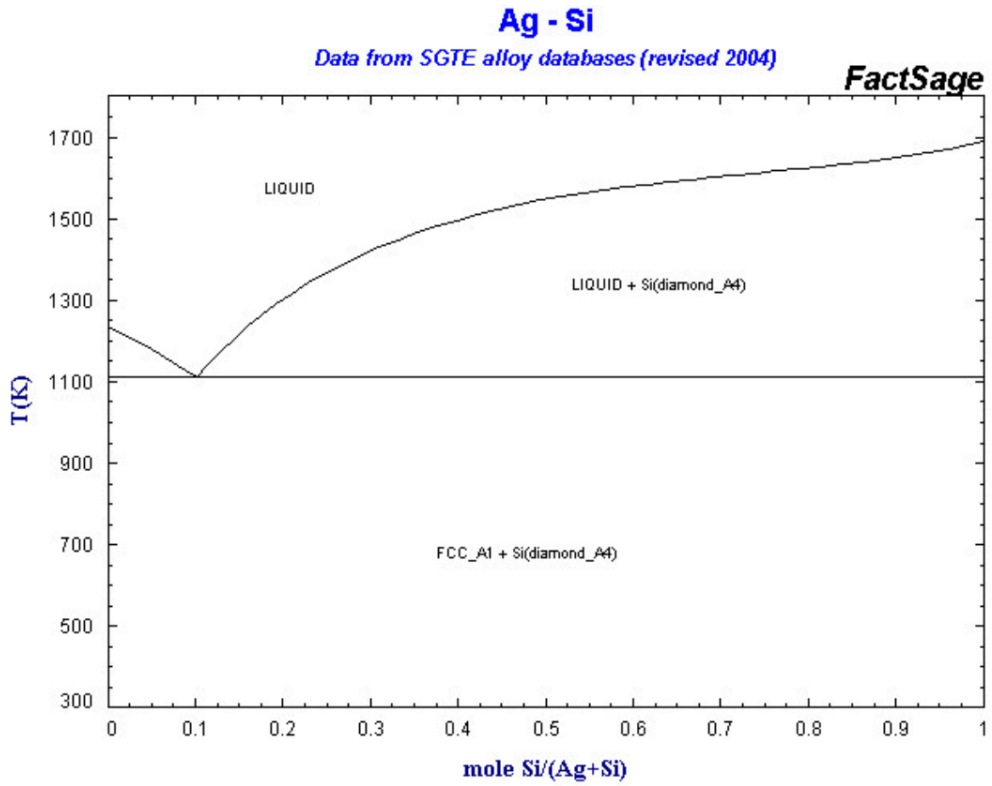


Figure 92: Phase diagram of Ag-Si [61]

The cross-sectional analysis of Ag shows the formation of a Ag-Si hyper eutectic structure at the interface between the Ag sheet and the top side of the device which can be seen in Figure 87(b). It also shows the formation of a dendritic structure having a composition of Ag 24 at% and Si 76 at%. Figure 92 shows the phase diagram of Ag-Si which suggests that in the Ag-Si hyper-eutectic alloy, Si started solidifying at approximately 1585 K.

The summary of the microstructural observations can be seen in Table 8 which shows the formation of different IMC and eutectic structures at the interface between the IGBT top and the intermediate material.

Intermediate Metal	Intermetallic compounds	Alloys	Minimum Temperature (K) From phase diagrams
Mo	$MoSi_2$	-	2220
Cu	$Cu_{33}Si_7$, $Cu_{15}Si_4$, $Cu_{19}Si_6$	-	1400
SnAg	-	Small Si particles in SnAg	1450
Al	-	Al 60 at% Si 40 at%	1420
Ag	-	Ag 65 at% Si 35 at%	1585

Table 8: Summary of different intermetallic compounds and alloys which are directly in contact with intermediate metal residual.

In the samples where Mo and Cu were used as the intermediate layer, broken pieces of Si without inclusion of any conductive metal i.e. Cu or Sn were observed. This probably implies that during the explosion period, the mating between the device and the intermediate layer was relatively poor and for the molten metal it was difficult to enter into the gaps between the broken particles of Si. Such an arrangement leads to the development of small and localized conductive/contact paths which resulted in low initial contact resistance value i.e. right after the explosion. Later during the current passage test, these small conductive channels were unable to support 50A of current for a long time and hence this resulted in an unstable short circuit.

In the case of Cu, which is very reactive, the surface oxidation was also observed as shown in Figure 70. This also contributed to the increase in the electrical resistivity which increased the probability of an unstable short circuit.

By contrast, the samples where SnAg, Al and Ag was used as the intermediate layer, there was the formation of Sn /SnAg channels through the micro cracks within the residual Si device. There was also less probability for the formation of the broken pieces of Si without any conductive material between them. From both these observations it can be inferred that the active contact area between the intermediate layer and the device was much better than those in the samples where the Mo and Cu was used. Because of the large contact area, the overall contact resistance was small which resulted in lower power dissipation both during the explosion test and during the current passage test therefore, the chances of the formation of local hotspots were low which helped in the stability of the low resistance throughout the test.

7.5 Effect of Thickness

After experimental verification that Ag is the most suitable material for a failure to short circuit, the next objective was to find the minimum thickness of Ag which can result in a stable failure to short circuit. In order to accomplish that, all the other parameters were kept the same to carry out the explosion test i.e. the input energy was kept at 750 J and the pressure on the device was kept at 2 MPa. The only thing that was varied was the thickness of the Ag sheet.

To find the minimum thickness, the first test sample was made by using a 25μm thick (8mm x 8mm) Ag sheet which was sandwiched between the Mo and the top of the device. The explosion test was performed on the test sample and it was found that the sample failed to short circuit. After the explosion test, the current passage test was

performed on the test sample which resulted in the initial contact resistance of 1.7mΩ and at remained almost unchanged for 150 hours confirming that it was a stable failure to short circuit. The SEM image of the cross-section can be seen in Figure 93 which shows the presence of conductive channels

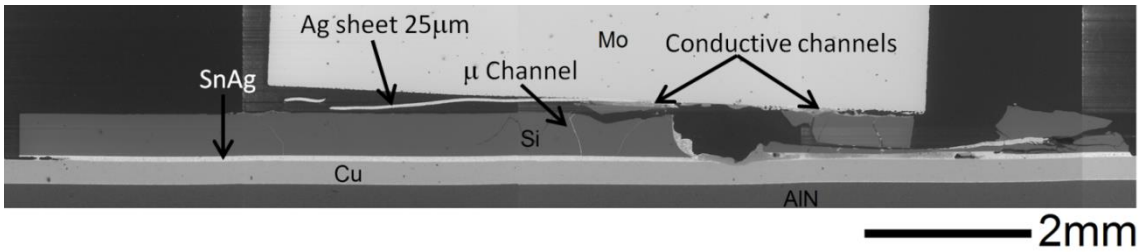


Figure 93: SEM image showing cross section of 25µm Ag sheet based test sample.

The second test sample was made by using 50µm thick un-sintered Ag nano particles preform placed between the Mo shim and the device top. It was decided to use the Ag nano particles preform because its sintering is a promising bonding technology for future IGBT modules.

It was experimentally found that the 50µm thick silver nano particle preform yields approximately a 20µm thick Ag layer after sintering and as the explosion test involves both high temperature and pressure, it converts the preform into 20µm thick bulk Ag sheet. The short circuit test was performed which resulted into an initial short circuit failure. Afterwards, current passage test was performed and it was found that the initial short circuit resistance was 0.7mΩ which increased to 8.4mΩ after 150 hours indicating that it was a stable failure to short circuit. The SEM of the cross section can be seen in Figure 94 which shows the formation of the conducting channels.

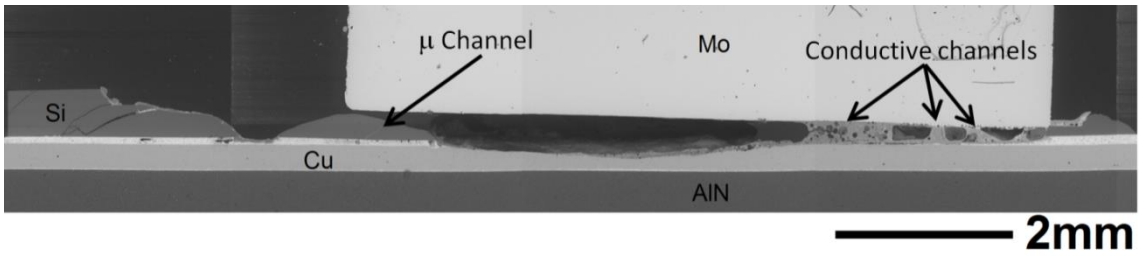


Figure 94: SEM image showing cross section of Mo coated with 50μm Ag nano particles preform.

The third test sample was made by using 5μm thick Ag sheet between the Mo shim and the top of the device. The explosion test was performed which resulted in initial failure to short circuit. Subsequently, the current passage test was performed and it was observed that the initial short circuit resistance was 100mΩ which after 5 minutes settled down to 2.3mΩ. The test was carried out for 150 hours in which it changed very slightly to 2.8mΩ.

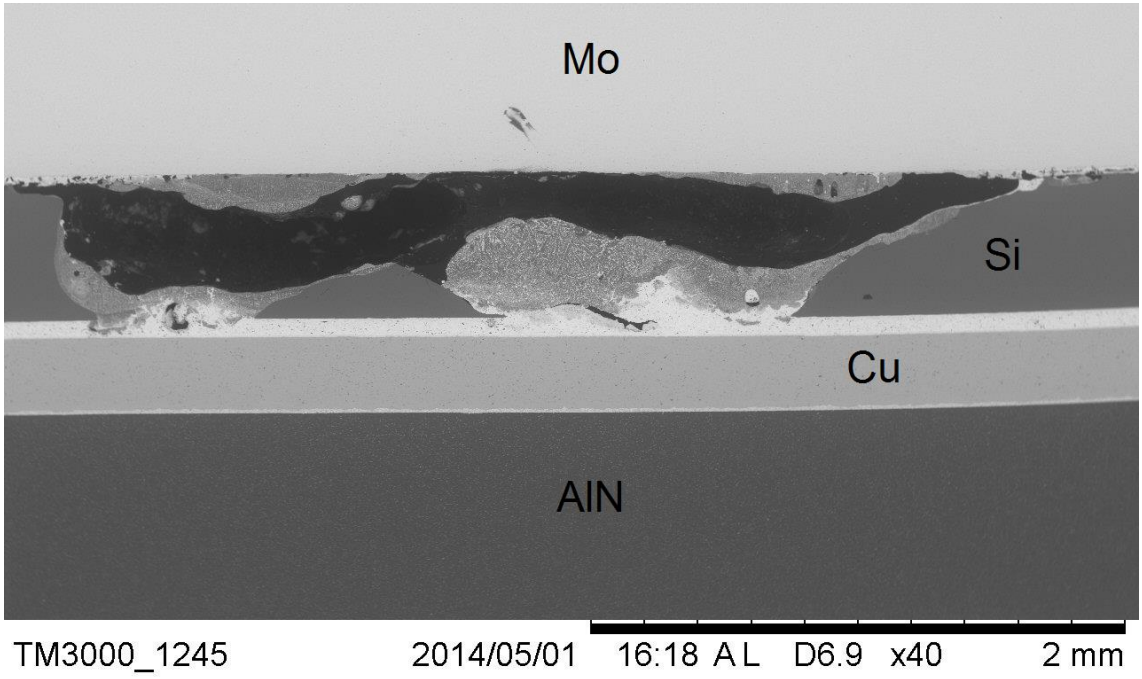


Figure 95: SEM image showing cross section of 5μm Ag sheet based test sample.

The high initial contact resistance caused the sample to overheat which probably melted/realigned the conductive channels and formed a low resistance stable conductive path.

To confirm the test result, this experiment was repeated two times. The first experiment resulted in a stable short circuit and the second experiment resulted in an unstable short circuit. Because repeatability was poor, 5μm think Ag sheet was deemed too thin to yield a stable short circuit.

Through these experiments, it can be concluded that the minimum thickness of the intermediate layer of Ag to cause a stable failure to short circuit should be greater than 25μm.

7.6 Summary

In this chapter two things have been evaluated, first the effect of using an intermediate layer of different kind of metals on the performance of the short circuit was experimentally studied. The experiments were performed by using different intermediate layer of metals e.g. Cu, SnAg, Al, and Ag. Cu as an intermediate metal failed to an unstable short circuit while SnAg, Al and Ag failed to a stable short circuit. Amongst SnAg, Al and Ag, the minimum short circuit contact resistance was achieved by using Ag; therefore it is the most suitable material which results in a stable SCFM. The possible reasons for Ag to be the best candidate are its compliance i.e. very suitable Young's Modulus, high electrical conductivity, high thermal conductivity and lower reactivity compared to the Cu, SnAg and Al. Secondly the minimum thickness of the intermediate layer of Ag to achieve a stable failure to short circuit was experimentally evaluated and it should be at least 25μm.

8 CONCLUSION AND FUTURE WORK

8.1 Conclusion

This thesis mainly deals with understanding the failure modes and development of the relevant technologies for achieving a stable short circuit failure mode for IGBT power module. The IGBT samples constructed with classical wirebond technology, flexible PCB interconnection, sandwich structure and press pack IGBT structure have been tested, and material systems including Mo, Cu, SnAg, Al and Ag served as intermediate metal in press pack type structure have been considered.

The failure modes of classic wirebonded IGBT power module have been investigated by constructing and performing tests on simplified, single die based wirebonded IGBT test vehicles. It achieved both OCFM and SCFM depending on the amount of energy which dissipated in test vehicle. If the energy level was higher than 125 J, the wirebonds acted like a fuse and melted away resulting in OCFM, whereas if the energy level was between 62.5 J and 125 J, the wirebonds stayed in contact with the top/emitter side of the IGBT resulting in SCFM. This energy level which resulted in SCFM was lower than the target energy level of 750 J which is considered to be a realistic amount of energy that a single die would face in a power IGBT module when it fails in a real industrial scenario. Therefore, it is highly likely that the wirebonded IGBT power modules would achieve OCFM in actual industrial scenarios.

To increase the energy level and to observe the effect of different interconnect technologies on failure modes, flexible PCB based test vehicles were constructed and tested. For similar reasons described above, they achieved both OCFM and SCFM. However, the flexible PCB based test samples were able to withstand energy

dissipation up to 312.5 J while maintaining SCFM. The SCFM at a higher energy level was contributed to more thermal mass and the large contact area on the emitter side of the device offered by flexible PCB interconnect technology.

A surface and cross-sectional scan was performed under SEM for both wirebonded and flexible PCB based test vehicles which achieved both OCFM and SCFM. It revealed that the top side of the IGBT of all test samples were covered with a layer of conductive eutectic structure having very small Si particles suspended in electrically conductive base composed of SnAg, Cu, Al and Ag. The samples which achieved SCFM have had their interconnect in contact with the top/emitter side of the IGBT, whereas they were either evaporated or destroyed in the test samples which achieved OCFM. The comparison of test results from using two different interconnect technologies led to the conclusion that the energy withstand ability of the power module can be increased by using interconnect technologies which can increase thermal mass and contact area on the top side of the power devices.

To further increase the ability of the test vehicle to sustain SCFM at 750J (the target energy level), sandwich structure based IGBT test vehicles were constructed and tested for their failure mode abilities. The sandwich structure based test vehicles were able to offer SCFM at a target energy level of 750 J. It was observed that testing caused energy dissipation in a small area which resulted in phase change of various metals e.g. Si, Cu, SnAg, Al and Ag from solid to gas, rapid expansion and ejection which caused formation of craters coated with the conductive eutectic structure. The eutectic structure contained very small broken pieces of nonconductive Si entangled in a conductive mixture of SnAg, Cu, Al and Ag.

A detailed analysis was carried out to correlate the amount of energy dissipated in the test vehicle with the phase change of the volume of metals which melted/evaporated

leaving the crater behind. The volume of different materials was calculated by 3d X-ray CT scanning of the test sample and it was concluded that the amount of energy required to melt the total amount of materials and vaporise part of them was well within the range of input energy.

Although the SCFM was achieved at the targeted energy dissipation level, it was not stable because of lack of compliance and microstructural realignment as the electrical contact resistance between the collector and emitter started increasing within few hours during the current passage test which was used to evaluate the life time of SCFM. From this experiment it was also concluded that the structure of the test vehicle should be such that it facilitate some conductive material to reoccupy the crater or void and form a low resistance contact to establish a stable SCFM.

This led to the development of a test vehicle structured like press pack IGBT module. A Mo shim was used on top side of the IGBT (because of its CTE close to Si) and the tests were carried out at the targeted energy level and it was observed that the test vehicle achieved SCFM with very low initial electrical contact resistance. Later during the current passage test it was observed that the short circuit was unstable. From the cross-sectional analysis the formation of MoSi2 was observed at the interface between the IGBT top and Mo shim which is evidence that high temperature was achieved during the test (2220 K). The initial low resistance contact which turned to high contact resistance was probably due to the fact that the IMC was very brittle and could not realign itself during the current conduction test. This resulted into poor contact between the device top and the Mo shim which further deteriorated with the temperature rise during the current passage test.

To find the most suitable intermetallic compound and the effect of compliance on the lifetime/stability of SCFM, foils of different materials e.g. Cu, SnAg, Al and Ag were

placed on top of the device and tests were carried out. It was found that the Cu based test vehicles were unable to achieve a stable SCFM as the contact resistance increased after few hours of the current passage test. The test vehicles based on SnAg, Al and Ag all passed the current conduction test when 50A was passed through the failed IGBT for 150 hours, indicating that the SCFM was stable. Amongst all test samples, the lowest electrical contact resistance was exhibited by Ag based test vehicles.

Cross-sections were prepared for all the test vehicles and were analysed under the SEM with integrated EDX stage. From the cross-sectional analysis, the common thing which was observed in all test samples was the formation of IMCs between Cu and Sn e.g. Cu_6Sn_5 Cu_3Sn located near the solder and DBC substrate interface. In Mo and Cu based samples, the formation of IMCs between Mo-Si and Cu-Si was observed located at the interface between the device top and the intermediate metal. In the case of SnAg, Al and Ag, the eutectic structure between Sn-Si, Al-Si and Ag-Si were observed. Although the thermal overload test was carried out on all test samples at the same energy level, it caused formation of large craters in Mo and Cu based test samples compared to the others. One possible reason could be the poor contact area between the device top and the intermediate metal due to the high Young's Modulus and hardness. This poor contact area resulted in high contact resistance as compared to the other soft metals, hence resulting in high energy dissipation which generated a large void under the intermediate metal. The formations of MoSi2, $Cu_{33}Si_7$, $Cu_{15}Si_4$ and $Cu_{19}Si_6$ IMCs at that interface were very brittle and scarcely connected to the device top. Therefore, during the current passage test, the initial contact resistance was low but as soon as the test sample started heating up, the IMCs being hard, could not realign hence resulted in an unstable SCFM. In the case of SnAg, Al and Ag based test samples, the eutectic structure formed at the interface between device top and the

intermediate metal had a good contact and during the current passage test, it was able to realign ensuring a stable SCFM. After the evaluation of the most suitable material i.e. Ag, its minimum required thickness has also been experimentally evaluated which should at least 25μm.

From all the experimental results it is safe to conclude that:

1. The wirebonded samples can be used to achieve SCFM at lower energy level.
2. Suitable interconnect technology can be used to increase the energy level.
3. Suitable material systems can be used to ensure stable SCFM.

8.2 Future Work

The work presented in this thesis can be used to understand and develop IGBT power modules capable of achieving stable SCFM. To extend this work, an essential step would be to look at the behaviour of multiple die modules first. It could be further extended to see how the SCFM capable IGBT module fails in an actual industrial application, where modules are connected in series. SCFM performance can be tested by inducing failure to one of the series connected modules and by observing if the converter continues its operation.

This research can also be extended to SiC based power semiconductor devices. At present the usage of SiC based power semiconductor devices e.g. JFET and MOSFET is gaining momentum and is being implemented in power electronics applications, where it offers superior voltage blocking, high current density and faster switching frequency compared to Si based power semiconductor devices. This research can be extended to find out the failure modes of SiC based power semiconductor devices.

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