# Impact of Silicon Carbide Device Technologies on Matrix Converter Design and Performance

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## Abstract

The development of high power density power converters has become an important topic in power electronics because of increasing demand in transportation applications including marine, aviation and vehicle system. The possibility for greater power densities due to absence of a DC link is made matrix converter topologies more attractive for these applications. Additionally, with the emerging SiC device technology, the operating switching frequency and temperature of the converter can be potentially increased. The extended switching frequency and temperature range provide opportunities to further improve the power density of the power converters.

The aim of this thesis is to understand how SiC devices are different from the conventional Si devices and the effect these differences have on the design and performance of a matrix converter. Specific gate drive circuits are designed and implemented to fully utilize the high speed switching capabilities of these emerging semiconductor devices. A method to evaluate the conduction and switching losses and performance of Si and SiC power devices in the matrix converter circuit is developed. The developed method is used to compare power losses of matrix converters designed with different Si and SiC devices for a range of operating temperatures and switching frequencies. A design procedure for matrix converter input filters is proposed to fulfil power quality standard requirements and maximize the filter power density. The impact of the switching frequency on the input filter volume has also been considered in this work. The output waveform distortion due to commutation time in high switching frequency SiC matrix converters is also investigated and a three-step current commutation strategy is used to minimize the problem. Finally the influence of parasitic inductance on the behaviour of SiC power MOSFET matrix converters is investigated to highlight the challenges of high speed power devices.

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# Introduction

## 1.1 Introduction

Power electronic converters have become widely used in many applications with the rapid development of power semiconductor devices due to improving the converter efficiency and more flexible control of applications. One application of power electronic converters is in motor drives for transportation systems including marine, aviation and vehicle transportation system [1].

Reducing the volume and weight of power converters is an important goal for applications in transportation systems because of the limited space and carrier capability [2]. Additionally, the efficiency of power electronic converters is also important for power density improvement because high efficiency means less cooling which usually increases the power density of power converters.

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The development of power electronic converters has been closely related to the development of power semiconductor device technologies that capable of handling higher powers [3]. The rapid development of power semiconductor devices in terms of voltage and current rating, improved performance, cost and size has accelerated the utilization of power electronic converters in a variety of electrical applications in industrial, aerospace, utility, communication and transportation systems [3].

Power electronic converters are being developed for more electric aircraft (MEA) applications [4]. The electrical power for the aircraft is provided by generators which are driven by the jet engines of the aircraft. For powering an AC system, the electrical energy which is generated by a variable speed generator is converted to a fixed frequency voltage through an AC/AC power electronic converter [5]. The AC/AC conversion can be achieved by AC/DC/AC converter or direct AC to AC converter such as matrix converter. One of the key benefits claimed for the matrix converter approach is the possibility of greater power density due to the absence of a DC link when compared with a AC/DC/AC converter which is very important for aerospace applications [6, 7].

## 1.2 Matrix Converter Technology

AC/AC converter topologies without any energy storage in the intermediate link are referred to as matrix converters. They can provide simultaneous amplitude and frequency transformation of voltage and current [8].

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The conventional direct matrix converter performs the power conversion in one stage. Alternatively, the indirect matrix converter topology features a two-stage power conversion. In the indirect matrix converter circuit, separate stages are provided for the power conversion similar to the AC/DC/AC converters. However, no energy storage element is implemented in the intermediate link [9]. Regarding their basic functionality, both matrix converter topologies are equivalent. Their different physical implementation only results in different operating characteristics.

Due to the absence of intermediate energy storage, matrix converters are often termed as “all silicon AC/AC converters”. However, it should be pointed out that matrix converters require also reactive components for a practical implementation. Those include the input capacitors to provide a voltage impressed input and additional passive components for the input filter to meet the electromagnetic compatibility (EMC) standards [8].

The complexity of the matrix converter topology makes the study and the determination of suitable modulation strategies a complex task. Different modulation techniques were introduced and compared in literature [10-14]. These different modulation strategies give different voltage conversion ratios and the number of commutations employed in each modulation strategy is different with implication on switching losses and waveform quality.

Matrix converter features a lower dependency of their overall semiconductor losses on the switching frequency compared with standard converter concepts [15]. This allows for increased converter efficiency if

higher switching frequencies are needed. However, it should be noted that matrix converter also require more semiconductor devices.

The matrix converter topology requires a bidirectional switch capable of blocking voltage and conducting current in both directions [7]. Discrete devices must be used to construct suitable bidirectional cells due to unavailability to date of a discrete semiconductor device that can fulfill this requirement. Different semiconductor technologies have been utilized for the implementing the bidirectional switches of the matrix converters such as the reverse blocking-IGBT technology [16, 17] and the silicon carbide device technology [18-20].

### 1.3 Research Motivation

One of the major requirements for aerospace applications which is fulfilled by the matrix converter, is to minimize the volume and weight [2]. It has been stated that an essential component to be minimized is the volume and weight of the passive components in order to maximize the power density of the matrix converter [21]. These passive components are used in the matrix converter to form the input filter. Hence, the part of the minimization of volume and weight of the matrix converter translates into maintaining the input current waveform ripple without increasing the passive components values. One of the approaches to minimize the magnitude of the input current ripple is to increase the switching frequency [22]. Therefore, the increase of power density of the matrix converter is mainly achieved by increasing the switching frequency, enabled by faster and lower loss power semiconductor devices.

# Chapter 1: Introduction

Using high switching frequencies and high power devices such as Insulated Gate Bipolar Transistor (IGBT) and Metal Oxide Semiconductor Field Effect Transistor (MOSFET), the power density of power electronics converter has increased since the 1990s [23]. Further improvement is expected in the near future with the implementation of wide band gap semiconductor devices such as Silicon Carbide (SiC) and Gallium Nitride (GaN) because of their even faster switching characteristics which bring benefits in some applications [24].

Among the wide band gap devices, the SiC devices can provide good performance in applications which demand high switching frequencies [25]. SiC devices can also sustain high operating temperatures, thus making them attractive candidates for aerospace applications [26], where the high temperature operation can reduce the weight and volume of the cooling system. Also, the use of SiC devices in applications requiring more than 400V can help in the design of power converters with higher efficiencies due to lower switching losses compared to conventional Silicon (Si) based devices [27].

To fully utilize the SiC power devices and further improve the power density, evaluation of the technology and power converter design approaches should be considered, and this is the basis of this work.

Although the approach for development a high power density power converters seems to be common, the relationship between the overall system performance in terms of efficiency and waveform quality is far from well-understood, especially in the extended frequency range offered by different SiC power devices. Furthermore, due to lack of experience and the different

characteristics of the SiC power devices, implementation of SiC power devices in a matrix converter remains a challenge in terms of EMI and lack of suitable capacitance developed for high voltage and high switching. Hence there is a clear need for a systematic performance analysis and design approach for the high power density matrix converter using SiC power devices.

## 1.4 Research Objectives

The objective of this work is to investigate the impact of SiC power devices on the design and performance of highly energy efficient matrix converters with high power density.

In this process the following aspects are considered:

- Design of suitable gate drive circuits for the different SiC power devices considered.
- Evaluation and characterization of a range of Si (benchmark) and SiC power devices which may be suitable for high switching frequency converters. This characterization includes comparing the driving, conduction and switching losses in matrix converter circuit for each device to enable the formation of a device loss model.
- Design of matrix converter input filter for obtaining minimum volume filters and achieving high power density converter by taking to account power quality standard requirements.
- Matrix converter performance in terms of output waveforms quality and the relationship with the switching frequency and the commutation time.

- The influence of parasitic circuit inductance on the SiC power MOSFET' performance in a matrix converter power circuit to highlight the challenges involved in the application of faster switching speed power electronic devices.

## 1.5 Thesis Outline

The remainder of this thesis is organised as follow:

In chapter 2 the most important power semiconductor devices used in typical motor drives are discussed in terms of their structure and fundamental characteristics.

In chapter 3 the matrix converter concept is introduced and a brief description of the chosen modulation strategy is given. The practical implementation issues of the matrix converter such as bidirectional switch structure, current commutation, input filter and need for a clamp circuit are explained. Simulation results of a matrix converter system for different switching frequencies are also presented.

In chapter 4 the design and implementation of a 2-phase to 1-phase matrix converter using different Si and SiC power devices is described. These circuits are used for measurement of switching phenomena and practically evaluating performance of the devices.

In chapter 5 the conduction and switching performance of a range of Si and SiC power devices are evaluated. The analytical power loss modelling of the matrix converter is presented and the impact of the switching frequency and

temperature on the matrix converter power loss is evaluated for a range of operating points.

In chapter 6 the design of the input filter is described in order to obtain minimum volume filters by taking into account the power quality standard requirements. Then the influence of the switching frequency on the input filter volume of the matrix converter is evaluated by considering converter power loss.

In chapter 7 the matrix converter performance in terms of output voltage and current in relation to the switching frequency and the commutation time is presented to highlight the effect of the commutation time limitations in high switching frequency matrix converters. Furthermore, analytical and experimental investigations into the influence of parasitic circuit inductance on the performance of SiC power MOSFETs in matrix converters are presented.

In chapter 8 the thesis conclusion and an outlook for possible future work are presented.

# Chapter 2
# Power Semiconductor Devices

There has been a surge of interest in the development of power semiconductor devices to meet the demands of compact and more efficient power converters in recent years. The power devices should have low on-state voltage drop and on-state resistance to reduce the conduction losses. They also should be capable to conduct high current and to block high voltage. They should have low switching losses. Additionally, to ensure long term reliability, to enable safe transient device overloading and be insensitive to high irradiation levels the semiconductor material should have minimal degradation effects and withstand elevated temperature levels.

The advancement of semiconductor switching devices is a key driving force for the development of power electronic technology. Therefore, significant efforts have been undertaken in the research and further development of

existing and new power semiconductor technologies such as the SiC technology for the past decades. In this Chapter, the potential benefits of SiC semiconductor materials compared with the Si material are summarized. Then an overview of adequate Si and SiC power semiconductor devices for low voltage power converters that are commercially available or close to commercialization have been expressed.

## 2.1 Silicon and Silicon Carbide

Recently, Si and SiC are two main semiconductor materials that are used to fabricate power semiconductor devices. There are various silicon carbide structures such as 3C-SiC, 4H-SiC and 6H-SiC [28], but only the last two structures are used in commercial devices and will be considered in this study. Some properties of Si and different structures of SiC are summarized in Table 2.1.

| Property | Unit | Si | 4H-SiC | 6H-SiC |
|---|---|---|---|---|
| Band Gap Energy $E_G$ | *eV* | 1.12 | 3.26 | 3.02 |
| Critical Electric Field $U_{crit} \approx E_{BD}$ | *MV/cm* | 0.3 | 2.8 | 2.5 |
| Intrinsic Carrier Concentration $n_i$ | $1/cm^3$ | $1.4\times10^{10}$ | $5\times10^{-9}$ | $1.6\times10^{-6}$ |
| Saturation Carrier Drift Velocity $v_{sat,n}$ | *cm/s* | $1\times10^{7}$ | $2\times10^{7}$ | $2\times10^{7}$ |
| Thermal Conductivity $\lambda_{th}$ | *W/(Kcm)* | 1.5 | 3.9 | 4.9 |

Table 2.1: Material properties of Si and 4H and 6H SiC at 25°C [28-30]

It can be noted from Table 2.1 that the largest differences between 4H-SiC and Si are the high critical electric field and the low intrinsic carrier density

which enable the implementation of power devices with high blocking voltage and small on-state resistance [31]. Additionally, a higher saturation carrier drift velocity allows for higher operating frequencies suitable for high switching frequency applications. The SiC also has superior thermal conductivity compared with Si which making the SiC power device attractive for operation at high temperatures. Therefore, SiC features excellent material properties for the implementation of high voltage, high switching frequency and high temperature power semiconductor devices. Among various structures of SiC materials, 4H-SiC is the preferred material due to its two times higher electron mobility ($\mu_n$) compared with 6H-SiC [32].

## 2.2 Suitable Devices for AC/AC Converters

Power semiconductor devices for an industrial, three-phase, low voltage AC/AC converter for drive application with nominal input voltage of 400V (rms) needs to have a blocking voltage capability of 1200V.

Due to band gap energy and critical electric field of Si, unipolar Si power switches have beneficial properties compared to bipolar devices for blocking voltage of up to 600V [33]. As the appropriate blocking voltage cannot be provided by Si high voltage MOSFETs, therefore they are not used for motor drive converters and bipolar devices are utilized primarily which have a blocking voltage capability of 1200 V. For this reason, Si IGBTs and Si PiN freewheeling diodes are mainly used in implementing state of the art low voltage motor drive converter systems. Also recently the Si PiN diode has been replaced by a SiC Schottky Barrier Diode (SBD) which provides a hybrid configuration of a Si transistor and a SiC freewheeling diode [34]. This

combination would generally allow for significantly reducing the dynamic losses in the power devices, particularly the turn on loss of the IGBT and the turn off loss of the diode.

To assess the potential of SiC semiconductor devices and performance of SiC AC/AC converter systems, a range of Si and SiC devices are considered in this work. In the following sections a details regarding the structure and operation of the most important Si and SiC power semiconductor devices will be presented. Also the reliable operation requirements of them are identified.

## 2.3 Si IGBT

IGBT is a monolithic combination of power Bipolar Junction Transistor (BJT) and MOSFET. It provides attractive characteristics of high input impedance of the voltage controlled MOSFET as well as low forward voltage drop at high current densities. There are different kinds of IGBTs in terms of semiconductor structure, properties and processing technology. The two traditional IGBTs are Punch-Through (PT) and Non-Punch-Through (NPT). The PT IGBT has lower on-state voltage drop and turn-off time than the NPT IGBT, whereas the NPT IGBT has higher blocking voltage and is less sensitive to temperature variations [35].

There is an IGBT based device with extended reverse blocking functionality which is named Reverse Blocking IGBT (RB-IGBT). The forward and reverse voltages can be blocked by the RB-IGBT and hence allows replacement of a serial connection of an IGBT and a diode with a single chip. It has been used

where bidirectional or reverse blocking power switches are needed such as current source converter or matrix converter [36].

Trench and Field-Stop (T&FS) is one of the main technological trends which provides further development in fabrication of IGBT devices [37]. The structure of T&FS IGBT which is mainly used by the manufacturer Infineon is shown in Figure 2.1. In the structure of T&FS IGBT, an $N^+$ buffer layer has been added below the $N^-$ substrate as a field stop layer in comparison with NPT IGBT. Due to the narrow $N^-$ layer, lower on-state resistance and switching losses can be achieved compared to an NPT IGBT. T&FS IGBT has lower saturation voltage and chip area due to combining a deep trench gate with back side emitter [38, 39].

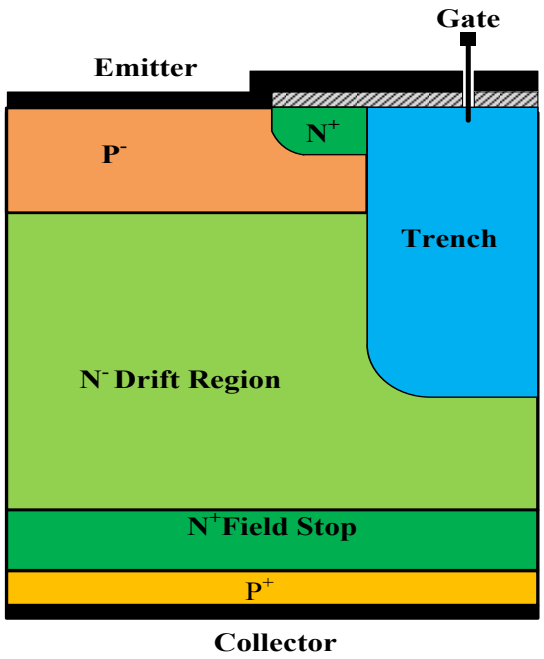



Figure 2.1: Schematic structure of T&FS IGBT [23]

## 2.4 SiC Diode

The advantages of SiC have accelerated the commercialization of SiC Junction Barrier Schottky (JBS) diodes with blocking voltages over 600 V by Infineon and Cree, which feature ultra-fast turn-on speed and almost zero reverse recovery effect compared to regular Si PiN diodes [40, 41]. The SiC JBS diode is a result of combining the properties of the PiN diode and Schottky diodes. The JBS diode is a Schottky diode with an integrated $P^+$-N junction grid into the drift region [42]. The structure of the SiC JBS diode is presented in Figure 2.2 which is mainly used by Cree.

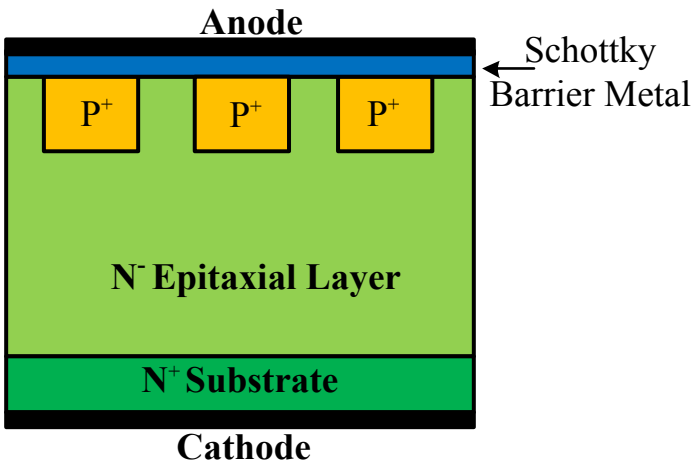



Figure 2.2: Schematic structure of JBS SiC diode [26]

## 2.5 SiC Power MOSFET

MOSFET switches are present nowadays in the majority of power conversion applications. Such popularity against other devices has been mainly justified by the simple and low loss driving requirements along with robust and reliable operation. Regarding the Si based technologies; MOSFETs are

normally applied below 600V due to the very large chip resistance at higher voltage levels [34].

The use of SiC material allows a significant extension of the blocking voltage range, due to reduction of the specific chip resistance. For instance, devices rated at 10kV have similar values of specific chip resistance as their 600V Si based counterparts [43].

### 2.5.1 Device Structure and Properties of SiC Power MOSFET

Vertical Depletion MOSFET (DMOSFET) is one of the main structures which provide further development in fabrication of SiC MOSFET device. The SiC DMOSFET structure which is mainly used by the manufacturer Cree is illustrated in Figure 2.3 [44]. It is a vertically structured device that can block very high voltages and conduct very large currents.

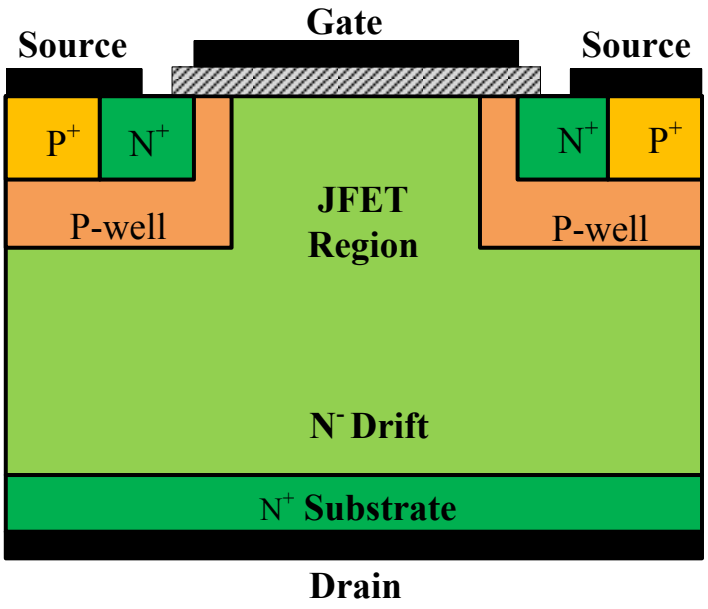



Figure 2.3: Schematic structure of SiC DMOSFET [28]

The direction of electron flow during forward operation is from the source via the inverted P-well and within the Junction Field Effect Transistor (JFET) region laterally and then within the drift layer and out via the drain contact vertically. On the other hand, when the gate of SiC MOSFET is turned on while the drain voltage polarity is negative with respect to the source, the reverse current conduction is possible. The direction of electron flow during reverse conduction is from drain to source through the same path as explained for forward conduction [45]. Reverse conduction property becomes interesting when considering synchronous rectification is needed in applications. The current will then be shared between the MOSFET structure and through the intrinsic diode, which cause reduction in the total loss.

The P-N junction of the P-well and the $N^-$ drift layer in SiC DMOSFET structure form an intrinsic body diode. It is forward biased and conducts current when the drain voltage polarity with respect to the source is negative. The on-state voltage drop of intrinsic PiN diode is around 2.5 to 2.7V. Due to such high voltage drop, an antiparallel Schottky can be used in order to attain optimal switching performance. Caution needs to be taken at higher temperatures and higher current values, when the intrinsic diode may enter in conduction before the external Schottky diode [46]. However in comparison with Si MOSFET, the reverse recovery characteristics for the body diode in a SiC MOSFET is negligible, which is comparable to the SiC diode [47].

In general, the total resistance of a MOSFET is the summation of the individual values from the channel, JFET region and drift region. While, in silicon designs, the drift region becomes dominant at higher voltage levels, the

same is not valid for SiC devices due to the thinner width and higher doping concentrations [48].

Regarding the temperature dependence, the channel resistance displays a negative coefficient, while the other two components have a positive coefficient. Therefore, in the SiC MOSFET a lower temperature dependence of the total device resistance can be observed [33].

SiC MOSFETs display a significantly less clear threshold limit and saturation regions in contrast with their Si based counterparts [49]. As a consequence, the device resistance can strongly be affected by the gate voltage. SiC MOSFETs are characterized by an output capacitance density approximately ten times higher than Si devices, due to the very thin drift region and higher doping concentrations. Such characteristic affects the turn on under hard switching conditions, as the output capacitance needs to be discharge through the MOSFET channel. The channel current density may reach very high values in case of high values of *dv/dt* [50]. The input capacitance is also larger due to the tight cell geometry for achieving higher channel density [51].

### 2.5.2 Operation and Driving of SiC MOSFET

Control of the SiC MOSFET is the same as the one valid for Si MOSFET. The difference is that the plateau on the gate voltage cannot be completely observed in some SiC MOSFET designs [52]. An important consequence of the low transconductance and threshold voltage of SiC MOSFETs is that these devices may be more susceptible to gate ringing effect [52].

Due to importance of the modest transconductance and short channel effects in SiC MOSFET, it is needed to be driven with higher gate voltage swing in comparison with Si IGBT [52].

## 2.6 SiC JFET

In fact of the referred challenges from the SiC MOSFET, JFETs have regained significant attention due to their simple and robust structure. In contrast with the MOSFET, the JFET is not controlled by an insulated gate structure but rather by a reverse biased PN junction. Hence the structure presents no interface problems related to gate oxide, increasing the reliability and ruggedness since no aging or parameter drift may be observed, making the device attractive for operation at high temperatures [53]. Additionally punch-through of the gate junction happens only at higher voltages in comparison with Si devices due to the wider band gap of SiC giving a broader gate voltage range capability [53]. Another feature is that most JFET devices have a symmetric channel structure, enabling operation as a synchronous rectifier in the reverse direction. This enables an additional reduction on the conduction losses during freewheeling [54].

### 2.6.1 Device Structure and Properties of SiC JFET

Two main constructive approaches can be identified for JFETs that are named the vertical and lateral structures [55]. In comparison with the lateral channel devices, the vertical approach have simple fabrication steps and also attains lower chip resistance [55].

The enhanced mode vertical JFETs structure, which is shown in Figure 2.4, is used by the manufacturer Semisouth. In this structure, the channel is formed between the two P-layers from the buried gate structures. The intrinsic PN-diode in such structure is connected from the gate to drain and source terminals. Moreover, the Miller capacitance which is defined as the gate to drain capacitance of the device is considerably high in such structure due to the large gate region overlapping the drain contact. By means of special doping profile and tight cell pitch design it is possible to obtain depletion of the channel at $V_{gs}$ equal to 0V, leading to a normally-off operation [56, 57] . A certain temperature dependence of the threshold voltage is possible to be observed in the presented structure [55]. Meanwhile a high value of transconductance is necessary in order to attain the nominal current capability before reaching the built-in voltage of the gate source diode [56].

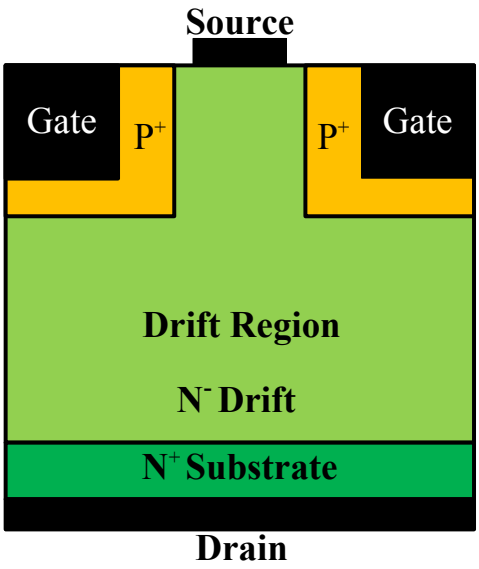



Figure 2.4: Schematic structure of SiC enhanced-mode vertical JFET [38]

### 2.6.2 Operation and Driving of SiC JFETs

By considering the basic JFET structure, the most significant drawback of it is the normally-on behaviour, as the channel will block only with continuous negative gate voltage leading to the formation of the depletion region. Due to the normally-on behaviour represents an inherent reliability problem for most circuits, especial gate driving circuits and supply strategies were proposed in the literature but still end up increasing the costs and complexity [18, 58-64]. Another possibility to solve this issue is the use of cascode structures that are nowadays seen as the most promising alternative for the referred problem [65]. In this configuration a low voltage Si MOSFET is connected in series with the SiC JFET. The voltage rating of the MOSFET is chosen to be higher than the maximum absolute value of the JFET pinch-off voltage. The driving of the JFET is indirectly performed by the MOSFET [66].

On the other hand, normally-off devices can be obtained by relying on the potential barrier formed by the grounded gate junction ($V_{gs}$=0V). In order to obtain such capability, the channel region needs to be very narrow with low doping concentration that results in a higher channel resistance. Another critical issue related to these devices is the reduction of the threshold voltage with increasing temperature values, that leads to the requirement of bipolar gate voltage driving to attain certain immunity against Electromagnetic Interference (EMI) [67].

In normally-off SiC JFET, conduction occurs only when a positive voltage higher than the threshold value is applied across the gate-source terminals.

Such level is very low, normally below 1.5V that makes the device especially susceptible to EMI induced voltages [68].

As it is mentioned a especial requirement of normally-off SiC JFET device from Semisouth is that the operation with direct polarization of the gate-source diode is advised by the manufacturer in order to attain the nominal values of forward resistance [69]. Thus a higher value of gate current starts to flow during conduction, as is presented in Figure 2.5 [70]. As it is obvious form Figure 2.5, the temperature dependence is significant and needs to be considered when designing the driver in order to avoid higher losses.

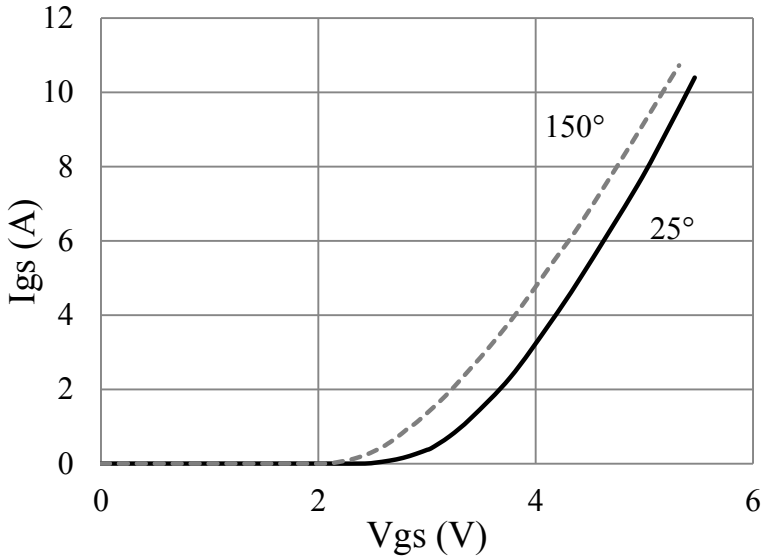



Figure 2.5: Gate-source current of normally-off SiC JFET as a function of gate-source voltage [45]

Therefore, it becomes mandatory to use a driver solution with gate current limitation. [71] proposed a simple drive circuit with bipolar voltage and gate current limiting resistor. The current limiting resistor can be calculated as:

$$R_g = \frac{(V_{cc} - V_{gs})}{I_{g\,(@V_{gs})}} \qquad (2.1)$$

where $V_{cc}$ represents the positive voltage of the driver, $V_{gs}$ and $I_g$ are the gate-source voltage drop and gate current value respectively.

The use of charge pumps is also utilized in a majority of configurations to provide demand peaks on the gate source current, enabling faster charge/discharge of the device parasitic capacitances and thus faster switching speed [53, 58]. The choice of the capacitance value needs to take into consideration not only the desired pump effect but also the inherent charge/discharge dynamic since the capacitor needs to be fully charged before the next transient. If the capacitor charges less than desirable value, it will cause a slight increase in the turn-on losses [72]. Advised is either a value at least 10 times larger than the device Miller capacitance or calculated by the following equation [73]:

$$\frac{2Q_{Miller}}{V_{CC}-V_{EE}-V_{gs}} \leq C_c \leq \frac{4Q_{Miller}}{V_{CC}-V_{EE}-V_{gs}} \quad (2.2)$$

Also an additional low resistance in series with the charge pump capacitor allows damping of any observed gate ringing. A simple parallel connection of the pump charge capacitor, damping resistor and gate resistor as gate drive circuit for normally-off SiC JFET is presented in Figure 2.6. In [74] a Schottky diode was also added in parallel with the gate resistor in order to enable fast turn-off.

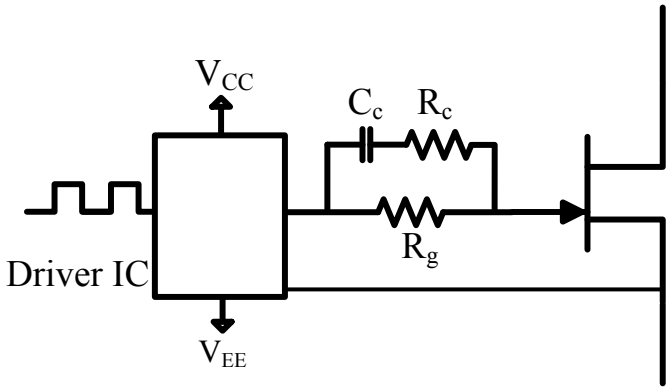



Figure 2.6: Simplified schematic diagram of the gate drive circuit for normally-off SiC JFET based on the charge pump circuit

## 2.7 SiC BJT

Many years ago, Si BJT was replaced by Si power MOSFETs and IGBTs due to its low current gain and small safe operating area which was caused by the unique second breakdown problem [75]. Indeed, there is almost no significant Si BJT research activity in the past 20 years, but the emergence of SiC as new material for power semiconductor devices has led to consider power BJTs as a possible candidate for high power and high voltage applications. This is due to some advantages of SiC BJTs when compared with other different SiC power devices which are normally-off device, very low specific on-state resistance, positive coefficient of the on-state resistance, fast switching speed, free from any gate oxide. Due to the junction voltage cancellation (base-emitter voltage is equal to base-collector voltage); the device resistance can be mainly summarized by contact/bond resistance plus substrate and collector layer resistances [75]. The SiC BJT as a bipolar device has a behaviour practically identical to a unipolar device at voltage levels around 1kV, due to the outstanding properties of the SiC material [76].

### 2.7.1 Device Structure and Properties of SiC BJT

The basic structure of BJT as shown in Figure 2.7 is normally obtained with a complete epitaxial construction [77]. Due to the absence of intrinsic diode function, an external freewheeling diode is necessary.

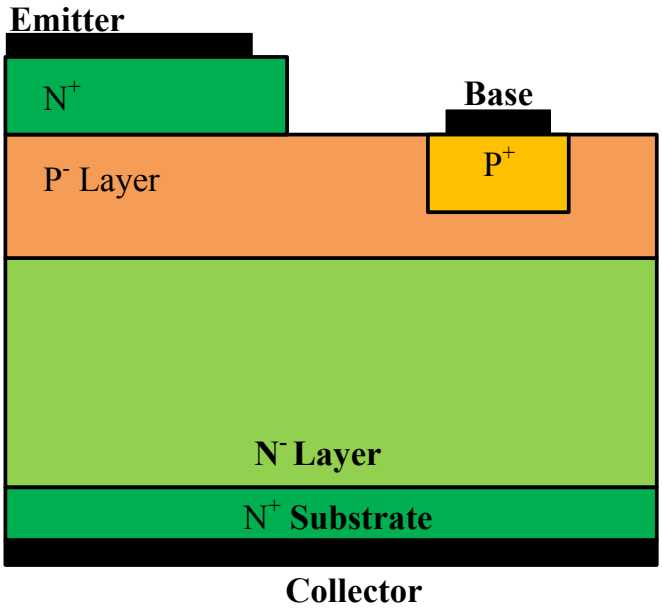



Figure 2.7: Schematic structure of SiC BJT [53]

The BJT structure itself is known for several decades but the application based on Si was so far limited due to some critical drawbacks like low current gain, poor switching performance, limited safe operation area with possible first and secondary breakdown effects.

Practically all of the referred drawbacks were overcome by use of SiC. The possible reduction of the drift thickness allows lower excess of charges during conduction, thus enabling considerably faster switching behaviour [78]. In comparison with other unipolar structures like MOSFETs, the BJT offers in

fact the possibility of reaching one of the lowest specific chip resistance values. Due to the voltage cancellation of both junction voltage ($V_{be,sat}$-$V_{bc,sat}$=0.1…0.2V), the most significant components are the resistances of the drift region and emitter/base contacts [76].

The gain obtained with SiC BJTs is more than three times higher than their best Si counterparts and is mainly achievable by optimizations related to constructive aspects [79-82].

The first breakdown is practically non-existent with SiC devices, so the current gain presents a negative thermal coefficient. Meanwhile, the second breakdown is also much less critical with SiC based BJTs, since the superior doping concentration moves the referred phenomenon to much higher current density levels [82].

### 2.7.2 Operation and Driving of SiC BJT

A vast multitude of driving circuits for Si BJTs can be found in the literature [75, 83]. Although such topologies are also applicable for their Si counterparts in principle, an important difference is the lower required value of base current.

The optimal driving conditions relay on a high peak of the base current at turn-on to minimize the delay and switching. The required peak current, $I_{bp}$, depends on the base-collector capacitance, $C_{bc}$, and on the expected charging time, $T_{ch}$, to charge such capacitor, being calculated by:

$$I_{bp} = \frac{Q_{C_{bc}}}{T_{ch}} \tag{2.3}$$

A well-known base drive arrangement that improves the switching transients is based on a charge pump circuit which is illustrated in Figure 2.8 [75]. It is consists of a base resistor and a speed up capacitor in parallel with resistor. The capacitor is charged up to a voltage level equal to the voltage difference between $V_{CC}$ and $V_{be(sat)}$ during the turn on transition of SiC BJT and so creating a low impedance path for the base current. In addition, the capacitor provides a negative voltage which applied across the base emitter terminals during the turn off transition of the SiC BJT. This causes improvement in the turn off transient.

Although the presented SiC BJT drive circuit is simple and cost effective, it has some critical drawbacks. The worst of them is that, the injected base current $I_b$ depends on the value of base-emitter junction voltage $V_{be}$ as demonstrated in the following equation.

$$I_b = \frac{V_{CC} - V_{be}}{R_b} \tag{2.4}$$

Under increasing values of collector current or at higher temperatures, $V_{be}$ will increase correspondently. This will lead to a certain reduction of the base current and thus to higher conduction losses. By increasing the supply voltage of drive circuit it is possible to avoid the above drawback, although in turn it causes increasing the driving losses [75].

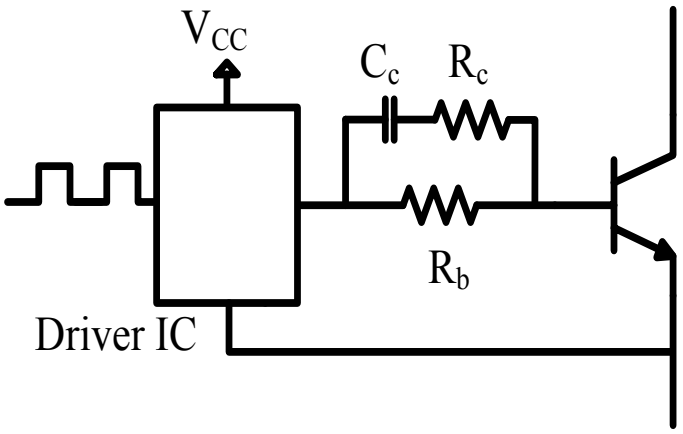



Figure 2.8: Simplified schematic diagram of base drive circuit for SiC BJT

## 2.8 Summary

The SiC power semiconductors are very attractive in high frequency, high voltage and high temperature application areas. An overview of Si and SiC material properties has been presented firstly in this chapter. Then details regarding the structure and operation of the most important Si and SiC semiconductor devices have been reviewed. The comparison of the four power semiconductor technologies commercially available with respect to different parameters is presented in Table 2.2. It is clear that the SiC power devices have the capability of operation at higher switching frequency with lower switching losses in comparison with the Si IGBT. Additionally, drive requirements of the Si IGBT and the SiC MOSFET are low and they have simple drive circuit in comparison with the SiC JFET and the SiC BJT. Compared to the Si IGBT, the cost to manufacture the power SiC devices can be high, due to manufacturing process.

| | Si IGBT | SiC MOSFET | SiC JFET | SiC BJT |
|---|---|---|---|---|
| Voltage Blocking | moderate | moderate | moderate | moderate |
| Switching Frequency | moderate | high | high | high |
| On-state Loss | high | high | low | low |
| Switching Loss | high | low | low | low |
| Gate or Base Current | pulses for turn on/off | pulses for turn on/off | pulses for turn on/off & on-state continuous current | pulses for turn on/off & on-state continuous current |
| Drive Requirements | low | low | moderate | moderate |
| Cost | low | high | high | high |

Table 2.2: Comparison of the power semiconductor devices commercially available

# Chapter 3
# The Matrix Converter Concept

The electrical power conversion from an input AC power line at a given frequency to an output AC power line at a different frequency can be achieved with different power converter structures. The available structures can be divided into direct and indirect power conversion schemes. Indirect power conversion scheme consists of two or more stages of conversion. The diode bridge rectifier inverter structure is an example of two stage indirect AC/DC/AC electrical energy conversion. In this indirect converter, an AC power is converted to a DC power by a rectifier stage firstly, and then converted again to AC at variable frequency by an inverter stage. On the other hand, AC/AC power conversion in direct conversion schemes is carried out by a single stage. The matrix converter is an example of single stage direct AC/AC electrical power converter. Each power conversion structure has

particular benefit and drawbacks, the choice, therefore, depends on the requirements of the application.

This Chapter gives an introduction to the matrix converter and briefly discusses its advantages and disadvantages when compared to the AC/DC/AC electrical converter. The fundamental of matrix converter operation are discussed and a brief description of the space vector modulation and the commutation schemes are then given. Practical implementation problems are discussed and solutions proposed in literatures are reviewed.

## 3.1 Matrix Converter Topology

Matrix converter as a direct power conversion scheme is a bidirectional direct power electronic converters and is able to provide amplitude and frequency conversion in AC electrical system. It consists of an array of controlled bidirectional switches; therefore, it is possible to connect an m-phase voltage source to an n-phase load directly.

One of the interesting features of matrix converters is sinusoidal input and output currents, so the high frequency components can be removed by means of a small filter. Depending on the modulation technique used, operation at unity input displacement factor can also be achieved. They are able to generate load voltages with arbitrary amplitude and frequency, therefore operation under abnormal input voltage conditions is possible for them [84].

In comparison with indirect AC/DC/AC electrical converters, there is no energy storage element in the matrix converter topology so it is called an all

silicon solution in power conversion. The elimination of bulky electrolytic capacitors, which are intolerant to high temperatures and have a relatively short life time [85], provides a potential for designing compact power conversion system. In fact, the weight and volume of the matrix converter due to lack of DC link capacitor is decreased in comparison with another kind of AC power converter which has energy storage elements [86]. However, due to lack of energy storage element, voltage transfer ratio of matrix converter is limited to 0.866 and the converter is more exposed to supply distortions and these are the main disadvantage of matrix converter.

Among different possible configurations for a matrix converter, an array of 3×3 bidirectional switches is of more interest for the industry because it connects a three-phase source to a three-phase load as shown in Figure 3.1 [6]. Each bidirectional switch can block voltage and conduct current in both directions, so the arrangement of bidirectional switches in the matrix converter enables any input line to be connected to any output line at any time.

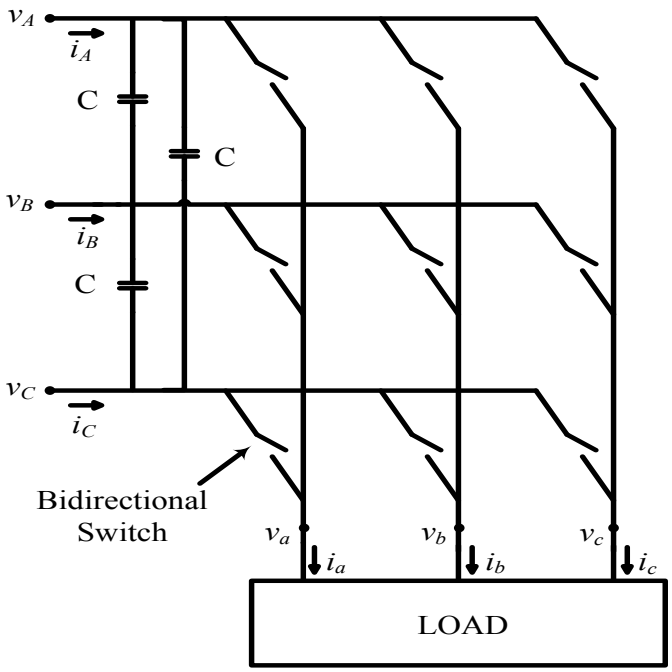



Figure 3.1: Basic 3×3 matrix converter circuit

In this structure, each output phase of the converter can be connected to any input phase voltage for a period of time, depending on which switch is on. Thus, the relationship between the input and output voltages along with the states of the nine bidirectional switches can be expressed in matrix form as given by:

$$\begin{bmatrix} v_a \\ v_b \\ v_c \end{bmatrix} = \begin{bmatrix} S_{aA} & S_{aB} & S_{aC} \\ S_{bA} & S_{bB} & S_{bC} \\ S_{cA} & S_{cB} & S_{cC} \end{bmatrix} \begin{bmatrix} v_A \\ v_B \\ v_C \end{bmatrix} \tag{3.1}$$

where $v_a$, $v_b$, $v_c$ and $v_A$, $v_B$, $v_C$ are the output voltages and the input voltages, respectively. $S_{jk}$ (j=a, b, c and k= A, B, C) which is defined as ‘1’or ‘0’ when switch is turned on and off respectively presents the switching state of each bidirectional switch connected between the input phase ‘k’ and output phase ‘j’ of the matrix converter.

Furthermore, the input currents of the matrix converter can be written in terms of the output currents and the switching states of nine bidirectional switches as given by:

$$\begin{bmatrix} i_A \\ i_B \\ i_C \end{bmatrix} = \begin{bmatrix} S_{aA} & S_{bA} & S_{cA} \\ S_{aB} & S_{bB} & S_{cB} \\ S_{aC} & S_{bC} & S_{cC} \end{bmatrix} \begin{bmatrix} i_a \\ i_b \\ i_c \end{bmatrix} \tag{3.2}$$

where $i_a$, $i_b$, $i_c$ and $i_A$, $i_B$, $i_C$ are the output currents and the input currents, respectively.

To ensure safe operation of the matrix converter, it is needed to consider two rules in analysing it. Firstly to avoid the extremely high current circulating through the converter, the voltage source at the input terminals must never be shorted. Secondly, to avoid the damage of the power switches caused by overvoltage, the naturally inductive load at the output terminals of the converter must not be opened. By these constraints, only one switch in one output phase can conduct at any instant. This basic operating principle of the converter can be written as given by:

$$S_{jA} + S_{jB} + S_{jC} = 1 \tag{3.3}$$

## 3.2 Space Vector Modulation for Matrix Converters

Study and determination of suitable modulation strategies for matrix converter is a hard task due to complexity of its topology. To provide a strong mathematical foundation for matrix converter theory, the first approach of modulation has been proposed by Alesina and Venturini [87]. It is based on the modulation duty cycle matrix approach. It allows the full control of the output

voltages and the input power factor, but the maximum voltage transfer ratio is limited to 0.5 and the input power factor control requires the knowledge of the output power factor [87].

In [88], the fictitious DC link algorithm has been presented and a noticeable increase of maximum voltage transfer ratio up to 1.053 has been achieved. This strategy divides the modulation to the rectification and inversion. It should be noted that by employing this kind of modulation technique, the waveform quality of the input and output variables decreases alongside the higher voltage transfer ratio.

The space vector modulation approach for the matrix converter as a well-known and established modulation technique has been addressed in [11, 13, 89-91]. The space vector modulation approach allows controlling the input power factor regardless the output power factor, reducing the number of switch commutations in each cycle period and fully utilizing the input voltages. The space vector modulation is a well-known solution for modulation strategy problem and is based on the instantaneous space vector representation of output reference voltages and input reference currents.

Due to the two constraints for the safe operation of the matrix converter, among twenty seven switching combinations for a three-phase matrix converter, only twenty one feasible switching configurations which is illustrated in Table 3.1 can be suitably used in the space vector modulation algorithm. The desirable output voltages and the input currents can be obtained by controlling the state of each bidirectional switch.

The first eighteen switching configurations, so called active configurations, determine an output voltage vector, $v_o$, and an input current vector, $i_i$, having fixed directions. The magnitude of these vectors depends on the instantaneous values of the input line to line voltages and output line currents. The last three switching configurations, namely zero configurations, are used to determine zero input current and output voltage vectors.

The representation of the input and output voltage vectors can be written based on the space vector approach respectively as given by:

$$\overrightarrow{v_i} = \frac{2}{3}\left(v_A + v_B e^{j2\pi/3} + v_C e^{j4\pi/3}\right) = V_i e^{j\alpha_i} \tag{3.4}$$

$$\overrightarrow{v_o} = \frac{2}{3}\left(v_a + v_b e^{j2\pi/3} + v_c e^{j4\pi/3}\right) = V_o e^{j\alpha_o} \tag{3.5}$$

The magnitudes, $V_i$ and $V_o$, and the phase angles, $\alpha_i$ and $\alpha_o$, of these voltage vectors depend on the instantaneous value of the input phase voltages and the output phase voltages respectively. The input voltage vector is provided from the measured three-phase input voltages, $v_A$, $v_B$ and $v_C$ whereas the output voltage vector is generated from the three-phase reference output voltages, $v_a$, $v_b$ and $v_c$.

Additionally, the space vector representation of the input and output current vectors can be given as:

$$\overrightarrow{i_i} = \frac{2}{3}\left(i_A + i_B e^{j2\pi/3} + i_C e^{j4\pi/3}\right) = I_i e^{j\beta_i} \tag{3.6}$$

$$\overrightarrow{i_o} = \frac{2}{3}\left(i_a + i_b e^{j2\pi/3} + i_c e^{j4\pi/3}\right) = I_o e^{j\beta_o} \tag{3.7}$$

where $i_A$, $i_B$, $i_C$ and $i_a$, $i_b$, $i_c$ are the input phase currents and the output phase currents, respectively. $I_i$ and $\beta_i$ are the magnitude and phase angle of the input current vector. $I_o$ and $\beta_o$ are the magnitude and phase angle of the output current vector.

| Switching configuration | Enabled switches | | | $V_o$ | $\alpha_o$ | $I_i$ | $\beta_i$ |
|---|---|---|---|---|---|---|---|
| +1 | $S_{aA}$ | $S_{bB}$ | $S_{cB}$ | $\frac{2}{3}v_{AB}$ | 0 | $\frac{2}{\sqrt{3}}i_a$ | $-\frac{\pi}{6}$ |
| -1 | $S_{aB}$ | $S_{bA}$ | $S_{cA}$ | $-\frac{2}{3}v_{AB}$ | 0 | $-\frac{2}{\sqrt{3}}i_a$ | $-\frac{\pi}{6}$ |
| +2 | $S_{aB}$ | $S_{bC}$ | $S_{cC}$ | $\frac{2}{3}v_{BC}$ | 0 | $\frac{2}{\sqrt{3}}i_a$ | $\frac{\pi}{2}$ |
| -2 | $S_{aC}$ | $S_{bB}$ | $S_{cB}$ | $-\frac{2}{3}v_{BC}$ | 0 | $-\frac{2}{\sqrt{3}}i_a$ | $\frac{\pi}{2}$ |
| +3 | $S_{aC}$ | $S_{bA}$ | $S_{cA}$ | $\frac{2}{3}v_{CA}$ | 0 | $-\frac{2}{\sqrt{3}}i_a$ | $\frac{7\pi}{6}$ |
| -3 | $S_{aA}$ | $S_{bC}$ | $S_{cC}$ | $-\frac{2}{3}v_{CA}$ | 0 | $-\frac{2}{\sqrt{3}}i_a$ | $\frac{7\pi}{6}$ |
| +4 | $S_{aB}$ | $S_{bA}$ | $S_{cB}$ | $\frac{2}{3}v_{AB}$ | $\frac{2\pi}{3}$ | $\frac{2}{\sqrt{3}}i_b$ | $-\frac{\pi}{6}$ |
| -4 | $S_{aA}$ | $S_{bB}$ | $S_{cA}$ | $-\frac{2}{3}v_{AB}$ | $\frac{2\pi}{3}$ | $-\frac{2}{\sqrt{3}}i_b$ | $-\frac{\pi}{6}$ |
| +5 | $S_{aC}$ | $S_{bB}$ | $S_{cC}$ | $\frac{2}{3}v_{BC}$ | $\frac{2\pi}{3}$ | $\frac{2}{\sqrt{3}}i_b$ | $\frac{\pi}{2}$ |
| -5 | $S_{aB}$ | $S_{bC}$ | $S_{cB}$ | $-\frac{2}{3}v_{BC}$ | $\frac{2\pi}{3}$ | $-\frac{2}{\sqrt{3}}i_b$ | $\frac{\pi}{2}$ |
| +6 | $S_{aA}$ | $S_{bC}$ | $S_{cC}$ | $\frac{2}{3}v_{CA}$ | $\frac{2\pi}{3}$ | $\frac{2}{\sqrt{3}}i_b$ | $\frac{7\pi}{6}$ |
| -6 | $S_{aC}$ | $S_{bA}$ | $S_{cC}$ | $-\frac{2}{3}v_{CA}$ | $\frac{2\pi}{3}$ | $-\frac{2}{\sqrt{3}}i_b$ | $\frac{7\pi}{6}$ |
| +7 | $S_{aB}$ | $S_{bB}$ | $S_{cA}$ | $\frac{2}{3}v_{AB}$ | $\frac{4\pi}{3}$ | $\frac{2}{\sqrt{3}}i_c$ | $-\frac{\pi}{6}$ |
| -7 | $S_{aA}$ | $S_{bA}$ | $S_{cB}$ | $-\frac{2}{3}v_{AB}$ | $\frac{4\pi}{3}$ | $-\frac{2}{\sqrt{3}}i_c$ | $-\frac{\pi}{6}$ |
| +8 | $S_{aC}$ | $S_{bC}$ | $S_{cB}$ | $\frac{2}{3}v_{BC}$ | $\frac{4\pi}{3}$ | $\frac{2}{\sqrt{3}}i_c$ | $\frac{\pi}{2}$ |
| -8 | $S_{aB}$ | $S_{bB}$ | $S_{cC}$ | $-\frac{2}{3}v_{BC}$ | $\frac{4\pi}{3}$ | $-\frac{2}{\sqrt{3}}i_c$ | $\frac{\pi}{2}$ |
| +9 | $S_{aA}$ | $S_{bA}$ | $S_{cC}$ | $\frac{2}{3}v_{CA}$ | $\frac{4\pi}{3}$ | $\frac{2}{\sqrt{3}}i_c$ | $\frac{7\pi}{6}$ |
| -9 | $S_{aC}$ | $S_{bC}$ | $S_{cA}$ | $-\frac{2}{3}v_{CA}$ | $\frac{4\pi}{3}$ | $-\frac{2}{\sqrt{3}}i_c$ | $\frac{7\pi}{6}$ |
| $0_1$ | $S_{aA}$ | $S_{bA}$ | $S_{cA}$ | 0 | - | 0 | - |
| $0_2$ | $S_{aB}$ | $S_{bB}$ | $S_{cB}$ | 0 | - | 0 | - |
| $0_3$ | $S_{aC}$ | $S_{bC}$ | $S_{cC}$ | 0 | - | 0 | - |

Table 3.1: Switching configurations for three-phase matrix converter [69]

The space vector modulation strategy for the matrix converter is based on a synthesis of the output reference voltage and the input reference current vectors by using a combination of the eighteen active and the three zero switching configurations which are detailed in Table 3.1 and shown in Figure 3.2. The capability to synthesize the output voltages of the converter and the input currents drawn from source voltages are provided simultaneously by this modulation technique. Additionally, by controlling the phase angle $\beta_i$ of the input current, the unity input displacement factor can be obtained.

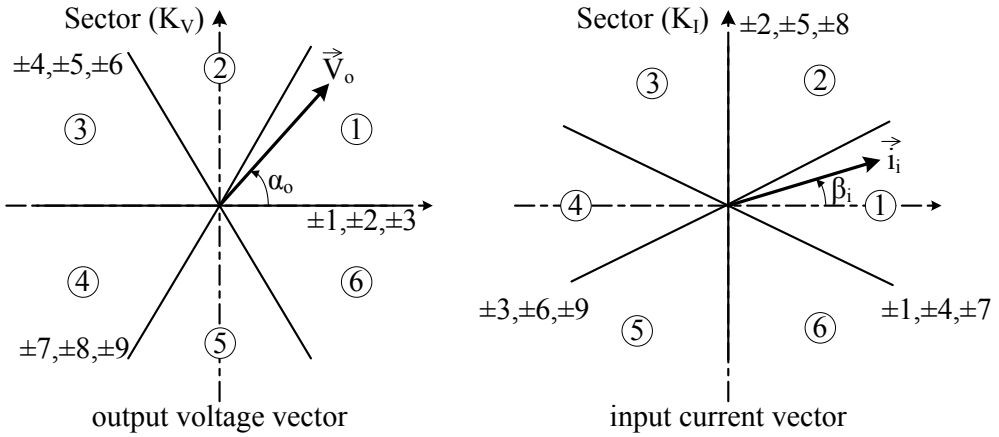



Figure 3.2: Space vector of output voltage and input current generated by the active configurations

It can be noted from Figure 3.2 that, the output voltage vector and the input current vector lie in one of the six output voltage and input current sectors. Four active switching configurations required to be identified for combination of the adjacent output voltage and input current vectors to achieve the desired output voltage vector and control input current phase angle. Additionally, in order to complete the switching cycle, the three zero switching configurations are considered in the space vector modulation algorithm. Therefore, the

switching states of the nine bidirectional switches can be produced. For instance, consider both the reference output voltage vector and the reference input current vector are placed in sector 1 as indicated in Figure 3.2 due to the phase angle of the input voltage vector, $\alpha_i$, cannot be controlled by the space vector modulation technique, the phase angle of the input current vector, $\beta_i$, has to be controlled for achieving zero input current phase displacement angle $\varphi_i$. The result of this is the unity displacement factor of the converter input. The possible active switching configurations are chosen initially to synthesize simultaneously the reference output voltage and input current vectors. Four of them only are needed from these configurations.

The selection of the switching configurations for each combination of the output voltage and input current sectors can be obtained by considering Table 3.2. When both the output voltage and input current vectors are placed in sector 1 the four selected switching configuration are +9, -7, -3 and +1.

To identify the four general switching configurations which are valid for any combination of input and output sectors, four symbols (I, II, III, IV) are also introduced in the Table 3.2. Any possible combination of output voltage and input current sectors can be determined by these four switching configuration. $K_V$ and $K_I$ present the sector of the output voltage vector and the input current vector respectively.

| $K_V$ \ $K_I$ | 1 | 2 | 3 | 4 | 5 | 6 | |
|---|---|---|---|---|---|---|---|
| 1 | +9 | -8 | +7 | -9 | +8 | -7 | I |
| | -7 | +9 | -8 | +7 | -9 | +8 | II |
| | -3 | +2 | -1 | +3 | -2 | +1 | III |
| | +1 | -3 | +2 | -1 | +3 | -2 | IV |
| 2 | -6 | +5 | -4 | +6 | -5 | +4 | I |
| | +4 | -6 | +5 | -4 | +6 | -5 | II |
| | +9 | -8 | +7 | -9 | +8 | -7 | III |
| | -7 | +9 | -8 | +7 | -9 | +8 | IV |
| 3 | +3 | -2 | +1 | -3 | +2 | -1 | I |
| | -1 | +3 | -2 | +1 | -3 | +2 | II |
| | -6 | +5 | -4 | +6 | -5 | +4 | III |
| | +4 | -6 | +5 | -4 | +6 | -5 | IV |
| 4 | -9 | +8 | -7 | +9 | -8 | +7 | I |
| | +7 | -9 | +8 | -7 | +9 | -8 | II |
| | +3 | -2 | +1 | -3 | +2 | -1 | III |
| | -1 | +3 | -2 | +1 | -3 | +2 | IV |
| 5 | +6 | -5 | +4 | -6 | +5 | -4 | I |
| | -4 | +6 | -5 | +4 | -6 | +5 | II |
| | -9 | +8 | -7 | +9 | -8 | +7 | III |
| | +7 | -9 | +8 | -7 | +9 | -8 | IV |
| 6 | -3 | +2 | -1 | +3 | -2 | +1 | I |
| | +1 | -3 | +2 | -1 | +3 | -2 | II |
| | +6 | -5 | +4 | -6 | +5 | -4 | III |
| | -4 | +6 | -5 | +4 | -6 | +5 | IV |

Table 3.2: Selection of switching configurations for each combination of output voltage and input current sectors [69]

The suitable duty cycle needs to be applied to each switching configuration at any switching period to provide the desired output voltage vector and the input displacement factor. The determination of the duty cycles for the selected four active switching configurations can be presented using:

$$d_I = \frac{2}{\sqrt{3}} q \frac{\cos(\tilde{\alpha}_0 - \frac{\pi}{3}) \cos(\tilde{\beta}_i - \frac{\pi}{3})}{\cos(\varphi_i)} \quad (3.8)$$

$$d_{II} = \frac{2}{\sqrt{3}} q \frac{\cos(\tilde{\alpha}_0 - \frac{\pi}{3}) \cos(\tilde{\beta}_i + \frac{\pi}{3})}{\cos(\varphi_i)} \quad (3.9)$$

$$d_{III} = \frac{2}{\sqrt{3}} q \frac{\cos(\tilde{\alpha}_0 + \frac{\pi}{3}) \cos(\tilde{\beta}_i - \frac{\pi}{3})}{\cos(\varphi_i)} \quad (3.10)$$

$$d_{IV} = \frac{2}{\sqrt{3}} q \frac{\cos(\tilde{\alpha}_0 + \frac{\pi}{3}) \cos(\tilde{\beta}_i + \frac{\pi}{3})}{\cos(\varphi_i)} \quad (3.11)$$

where $d_I$, $d_{II}$, $d_{III}$ and $d_{IV}$ present the related duty cycles of the four active switch configurations. $q$ as the voltage transfer ratio is equal $V_o/V_i$. $\varphi_i$ as the input phase displacement angle is the phase angle between the input current vector and the input voltage vector. Moreover, $\tilde{\alpha}_o$ and $\tilde{\beta}_i$ are the angles of the output reference voltage and input reference current vectors respectively which are measured from the bisecting line of the corresponding sectors as they are shown in Figure 3.3. The boundary limits of these phase angles are given by:

$$-\frac{\pi}{6} < \tilde{\alpha}_o < +\frac{\pi}{6} \quad , \quad -\frac{\pi}{6} < \tilde{\beta}_i < +\frac{\pi}{6} \quad (3.12)$$

The input phase displacement angle, $\varphi_i$, is controlled to keep the input current vector in phase with the input voltage vector and thus the unity input displacement factor is obtained. The maximum voltage transfer ratio of the matrix converter is 0.866 for the unity displacement factor operation [11].

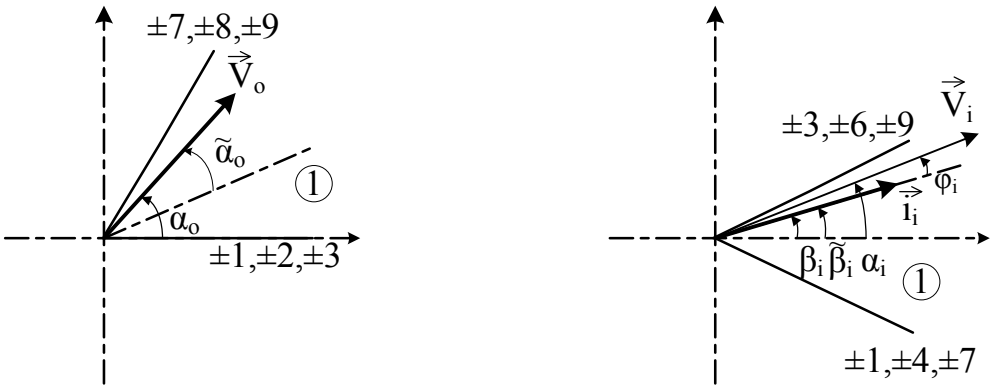



Figure 3.3: The synthesis of reference vectors in a given sector

For unity displacement factor operation and the voltage transfer ratio less or equal 0.866, it is needed to apply:

$$d_I + d_{II} + d_{III} + d_{IV} \leq 1 \tag{3.13}$$

Then the duty cycle for the zero switching configurations is applied to complete the sampling period, as it is shown by:

$$d_o = 1 - (d_I + d_{II} + d_{III} + d_{IV}) \tag{3.14}$$

In the space vector modulation technique, the zero switching configurations are distributed in the switching period. The duty cycle for each zero configuration, $0_1$, $0_2$, and $0_3$ can be determined by:

$$d_{01} = d_{02} = d_{03} = \frac{d_0}{3} \tag{3.15}$$

After obtaining the duty cycles for the active and zero switching configurations, to define the turn-on and turn-off sequence of the switches, determination of the switching pattern is considered subsequently. The double

sided switching pattern [11] was adopted in the implementation. The double sided, three zero vector switching pattern for nine bidirectional switches in one switching period when the four active switching configurations are +9, -7, -3 and +1 is shown in Figure 3.4.

$t_I$, $t_{II}$, $t_{III}$, $t_{IV}$, $t_{01}$, $t_{02}$ and $t_{03}$ as the time interval of the switching configuration can be defined by:

$$t_n = d_n T_{seq} \tag{3.16}$$

where $T_{seq}$ is the switching period and $n$ stands for $I$, $II$, $III$, $IV$, $01$, $02$ and $03$. It is clear that there are twelve combinations between the nine bidirectional switches in each switching period. It should be mentioned that the matrix converter performance in terms of ripple in the input and output waveforms is affected by the different switching patterns [92].

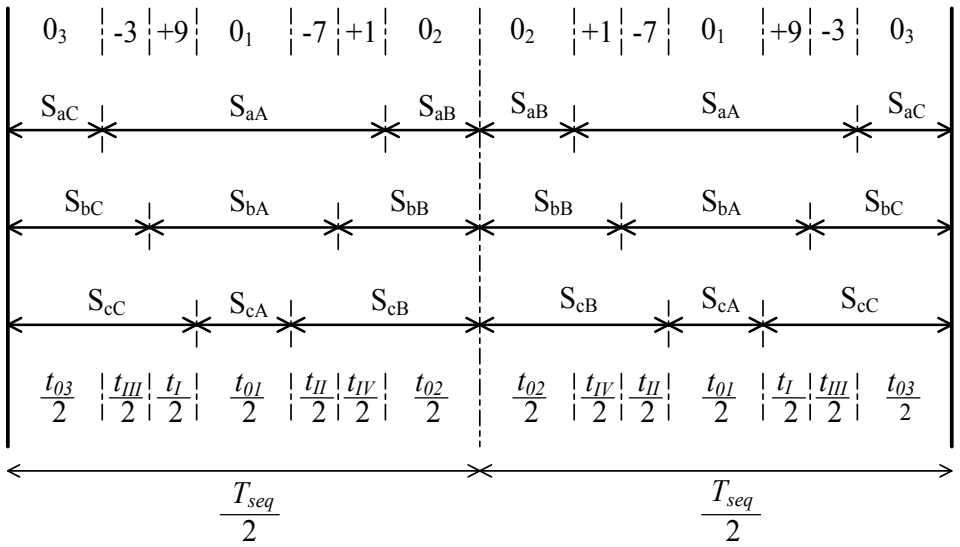



Figure 3.4: Double sided switching pattern of the space vector modulation in a switching period $T_{seq}$

## 3.3 Bidirectional Switch Structures

To implement a matrix converter, a bidirectional switch which is able to block voltage and conduct current in both directions is needed. Due to lack of such power electronic devices in market currently, it is needed to employ discrete devices to provide proper bidirectional switch. Additionally, the choice of bidirectional switches dictates which commutation methods can be used. In this section, some possible bidirectional switch configurations and the benefits and drawbacks of each arrangement are summarized. Also, it has been assumed that the switching device would be an IGBT, but other devices such as MOSFETs, JFETs and BJTs can be employed in the same way.

### 3.3.1 Diode Bridge Embedded Bidirectional Switch

The most simple bidirectional switch configuration is an IGBT at the centre of a single phase diode bridge as shown in Figure 3.5 and named diode bridge embedded bidirectional switch [93]. The main advantage of this configuration is that only one gate drive is needed per switch cell because both current directions flow through the same switching device so reducing the cost of the power circuit and complexity of the control and gate drive circuits. However the direction of current through the switch cell cannot be controlled which is a disadvantage of this configuration as most advanced commutation techniques rely on independent control of the current in each direction. Furthermore, due to the presence of three devices in each conduction path, the conduction losses of device are high [93].

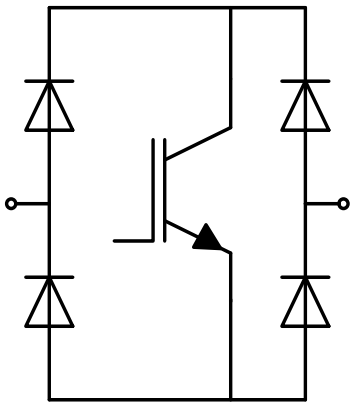


Figure 3.5: Diode bridge embedded bidirectional switch configuration

### 3.3.2 Anti-series IGBT with Antiparallel Diode Configurations

There are two kinds of these configurations as bidirectional switch, namely the common emitter configuration and the common collector configuration as illustrated in Figure 3.6.

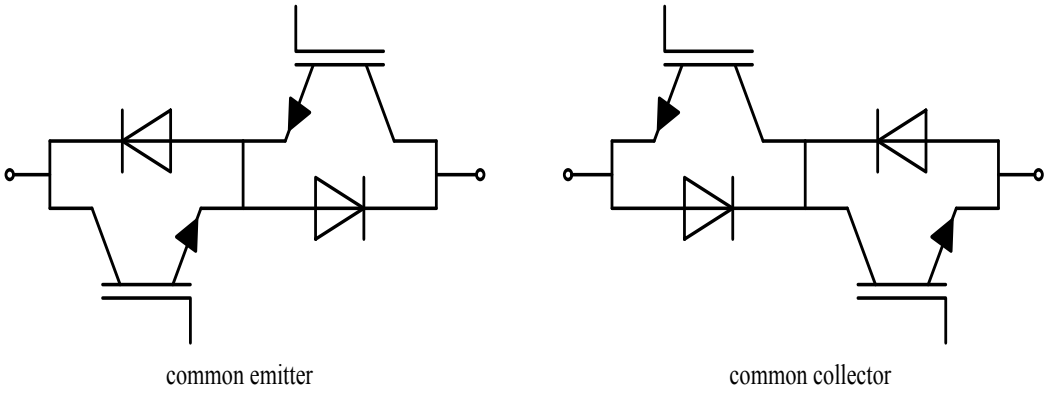



Figure 3.6: Anti-series IGBT with antiparallel diode configurations

The common emitter bidirectional switch consists of two IGBTs with antiparallel diodes, connected in a common emitter configuration. The diode provides the reverse blocking capability for the bidirectional switch. In this

configuration, one isolated power supply is needed to drive active bidirectional switch due to the common emitter point is considered as a local ground for each gate drive circuit. Thus nine isolated power supplies are needed for the eighteen switches of the three-phase to three-phase matrix converter.

The common collector bidirectional switch consists of two IGBTs with antiparallel diodes, connected in a common collector configuration. The main benefit of this configuration in comparison with the common emitter bidirectional switch is that only six isolated power supplies are needed for the eighteen switches of the three-phase to three-phase matrix converter as the eighteen IGBTs have the emitter connected to one of the six inputs and outputs. However, the drawback of this configuration is that the operation of the matrix converter in a large practical system can be affected due to difficulty in minimizing the parasitic inductance in the power converter circuit [94].

Additionally, in comparison with the diode bridge embedded bidirectional switch, the advantages of the ant-series IGBT with antiparallel diode configurations are possibility to control the direction of current independently and also the conduction losses of the converter is less due to only two devices that carry the load current at any time per switch.

### 3.3.3 Antiparallel RB-IGBTs

The implementation effort of a bidirectional switch can be reduced significantly by using RB-IGBTs. Due to reverse voltage blocking capability of RB-IGBTs, it is possible to replace the antiparallel wiring of two series connections of an IGBT and diode by two antiparallel connected RB-IGBTs as

shown in Figure 3.7. This configuration allows lowering the number of semiconductor dies for a bidirectional switch from four to two which leads to a very compact converter.

The on-state losses of a RB-IGBT are lower compared to an IGBT and a diode with an equivalent current rating that are connected in series as described in [95]. Therefore, it is generally believed that using RB-IGBTs instead of discrete series connections of IGBTs and diodes would not only simplify the power circuit layout but also decreases the semiconductor losses. However, due to large tail currents during RB-IGBT device turn-off as reported in [96] and poor reverse recovery characteristics, widespread use of this configuration has been limited.

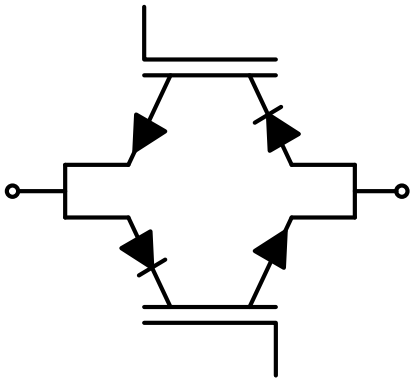


Figure 3.7: RB-IGBT bidirectional switch configuration

## 3.4 Commutation Strategies

Reliable current commutation between bidirectional switches cannot be achieved automatically due to the lack of natural freewheeling paths. It is necessary to control these switches to turn-on and turn-off in such a way to

satisfy the two fundamental rules of the matrix converter. To avoid the destruction of the converter due to the over currents and over voltages, these rules state that there can only be one input phase connected to the same output phase and that all the switches in any output phase cannot be open.

Some simple commutation strategies such as dead-time commutation and overlap commutation have been introduced for the matrix converters over the years. However, they need to add extra components to the bidirectional switch to satisfy the two fundamental rules which cause increasing converter losses [7].

The most common and reliable solution is four-step commutation which obeys the rules and controls the direction of current flow through the commutation cells. The two basic methods of implementing the four-step commutation are explained in this section. The first one is according to output current direction information and the second one to input voltage sign.

### 3.4.1 Four-Step Commutation Based on Output Current Direction

The four-step current commutation technique based on output current direction is a well-know and is a very reliable commutation scheme. To describe the principle of the four-step commutation technique, a simplified 2-phase to 1-phase matrix converter with two common emitter bidirectional switches is considered as illustrated in Figure 3.8.

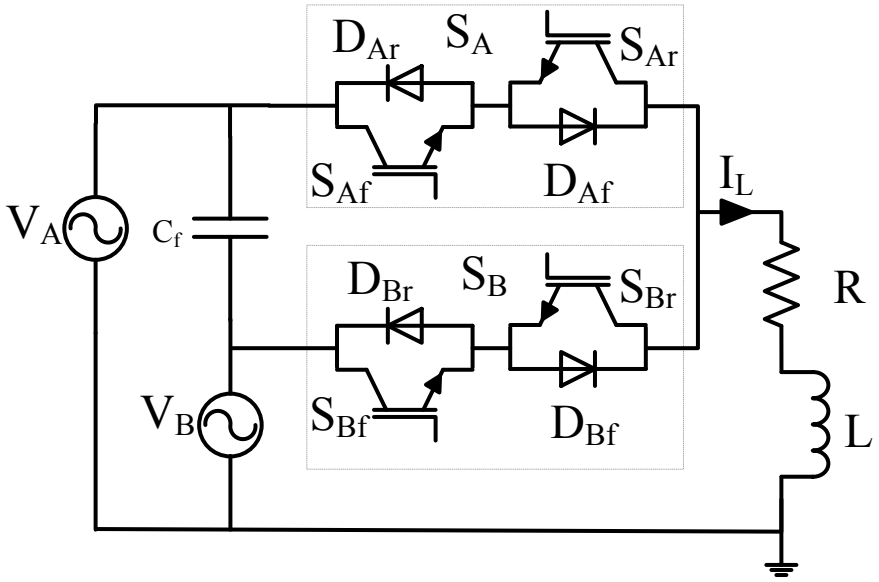



Figure 3.8: Two-phase to one-phase matrix converter

The timing diagram and sequence of the four-step current commutation for commutation from bidirectional switch $S_A$ to bidirectional switch $S_B$ where the direction of the output current, $I_L$, is positive is presented in Figure 3.9. It should be noted that the letters 'f' and 'r' in each bidirectional switch present the forward and reverse current direction devices, respectively.

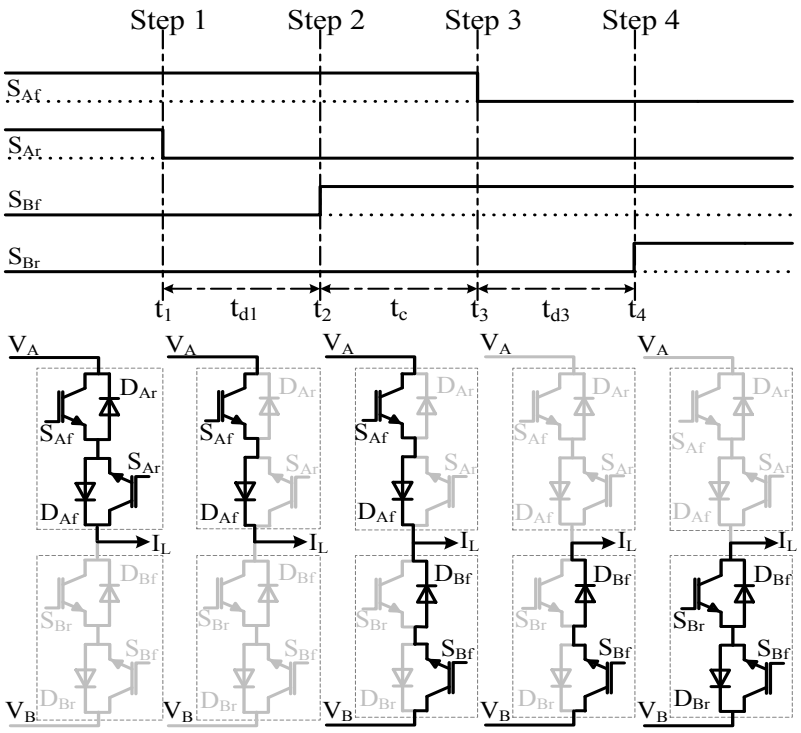



Figure 3.9: Timing diagram and sequence of four-step current commutation when the output current is positive and constant

The following explanation assumes that the output current is constant and in the direction illustrated in Figure 3.8 and both devices of the bidirectional switch $S_A$ are enabled. When a commutation to $S_B$ is required, the current direction is used to determine which device in the active switch is not conducting. The switching state sequence to follow is:

Step 1 consists in turning off the device that is not conducting the output current within the outgoing bidirectional switch; in this case, the device $S_{Ar}$ is disabled.

Step 2 consists in turning on the device that will conduct the positive output current within the incoming bidirectional switch; in this case, the $S_{Bf}$ is activated.

Step 3 consists in turning off the device that is conducting the output current within the outgoing bidirectional switch; in this case, the $S_{Af}$ is disabled.

Step 4 consists in turning on the device that will not conduct the output current within the incoming bidirectional switch; in this case, the $S_{Br}$ is activated.

For the case when the output current is in the opposite direction, the same procedure can be considered to determine the commutation sequence.

In commutation procedure, the devices cannot be enabled instantaneously due to the finite switching times of the power semiconductor devices as well as the propagation time delays of their gate signals. Therefore, referring to the timing diagram, short time gaps, $t_{d1}$, $t_c$, $t_{d3}$, which are determined by the device characteristics, needs to be introduced to the commutation processes between each step of the sequence. It should be noted that to avoid the short circuit between two input phases, the commutation time has to be long enough for the incoming device to turn on before the outgoing device is turned off. It is important also to note that the commutation time needs to be minimized to avoid waveform distortion [6].

Furthermore, due to the finite time of switching for the power device, a power loss is produced by the switching of power device. If the switching of the device occurs when the current through the devices or the voltage across the device is nearly zero, the switching loss is negligible and is referred to as ‘soft switching’. Conversely, if the current through the device and the voltage

across the device is non-zero, the switching loss can be significant and is referred to as 'hard switching'.

In the four-step current commutation, the type of switching depends on the direction of the load current and the relative potentials of the input voltages. If $V_A - V_B > 0$, commutation will occur at $t_3$ resulting a hard turn-off switching in $S_{Af}$ and a soft turn-on switching in $S_{Bf}$. Conversely, if $V_A - V_B < 0$, commutation takes place at $t_2$ resulting in a hard turn-on switching in $S_{Bf}$ , a soft turn-off switching in $S_{Af}$ and a hard turn-off switching in $D_{Af}$. It should be noted that there is no switching loss at all in $S_{Ar}$ and $S_{Br}$ for either situation, since neither conduct current when load current is positive. A similar, but different sequence of events to that above occurs for negative load current. All the possible commutation scenarios and associated switching types for the 2-phase to 1-phase matrix converter are summarised in Table 3.1.

| Commutation | $V_A$-$V_B$ | $I_L$ | $S_A$ | $S_B$ |
|---|---|---|---|---|
| A→B | + | + | Hard turn-off ($S_{Af}$) | Soft turn-on ($S_{Bf}$) |
| A→B | + | - | Soft turn-off ($S_{Ar}$) & Hard turn-off ($D_{Ar}$) | Hard turn-on($S_{Br}$) |
| A→B | - | + | Soft turn-off ($S_{Af}$) & Hard turn-off ($D_{Af}$) | Hard turn-on($S_{Bf}$) |
| A→B | - | - | Hard turn-off ($S_{Ar}$) | Soft turn-on ($S_{Br}$) |
| B→A | + | + | Hard turn-on($S_{Af}$) | Soft turn-off ($S_{Bf}$) & Hard turn-off ($D_{Bf}$) |
| B→A | + | - | Soft turn-on ($S_{Ar}$) | Hard turn-off ($S_{Br}$) |
| B→A | - | + | Soft turn-on ($S_{Af}$) | Hard turn-off ($S_{Bf}$) |
| B→A | - | - | Hard turn-on($S_{Ar}$) | Soft turn-off ($S_{Br}$) & Hard turn-off ($D_{Br}$) |

Table 3.3: Possible commutation scenarios and associated switching types in 2-phase to 1-phase matrix converter

### 3.4.2 Four-Step Commutation Based on the Sign of the Input line-to-line Voltage

The four-step commutation using the input voltage sign is another commutation scheme that can be used to ensure safe operation of bidirectional switch in the matrix converter. In this method, the commutation sequence between bidirectional switches in each output phase of matrix converter is determined based on the measuring input phase voltages. The basic concept of this strategy is to reproduce a freewheeling path in each bidirectional switch involved in the commutation process. Both power devices of the corresponding bidirectional switch have to be turned on when an output phase is connected to an input phase.

The timing diagram and the sequences of the four-step commutation technique using the input voltage sign when output current commutated from the bidirectional switch '$S_A$' to '$S_B$' and $V_A - V_B > 0$ is presented in Figure 3.11. When compared with the four-step commutation based on the output current, in this scheme the power devices are controlled to be turned on and turned off in different sequence.

Referring to Figure 3.10, once the diode that is reverse biased has been identified, the commutation strategy takes place in the following sequential steps:

Step 1 consists in turning on the device that is connected to the reverse biased diode of the incoming switch; in this case, the '$S_{Bf}$' is enabled.

Step 2 consists in turning off the device that is connected to the non-reverse biased diode of the outgoing switch; in this case, the '$S_{Af}$' is disabled.

Step 3 consists in turning on the device that is connected to the non-reverse biased diode of the incoming switch; in this case, the '$S_{Br}$' is enabled.

Step 4 consists in turning off the device that is connected to the reversed biased diode of the outgoing switch; in this case, the '$S_{Ar}$' is disabled.

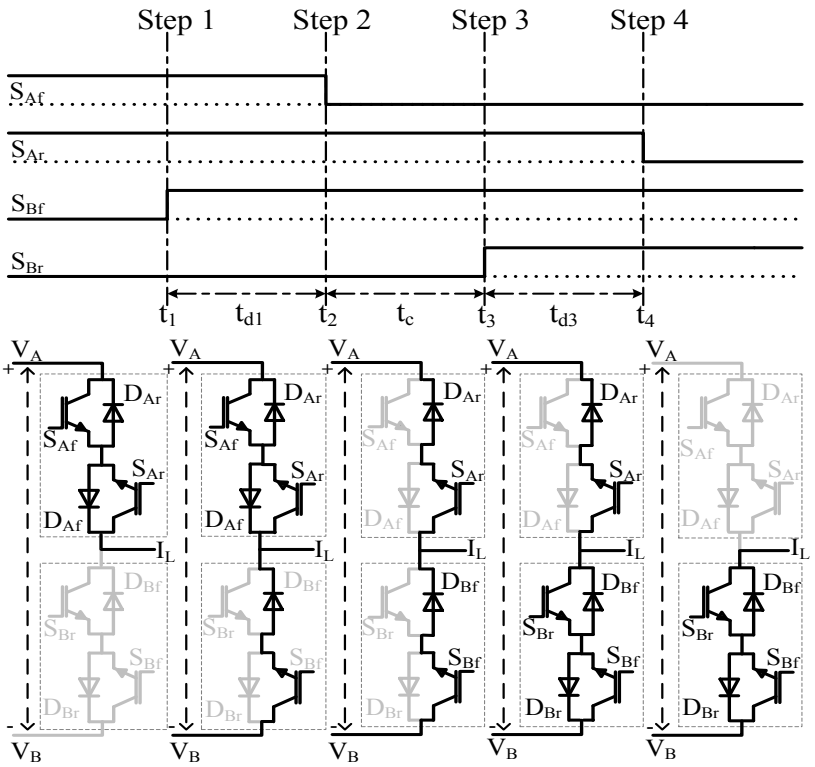



Figure 3.10: Timing diagram and sequence of four-step commutation based on input voltage magnitude when $V_A - V_B > 0$

In order to guarantee the above desired four-step switching sequence short time gaps, $t_{d1}$, $t_c$, $t_{d3}$, have to be inserted between the steps to ensure that the outgoing switch is completely disabled before the incoming device is enabled. Furthermore, the commutation time delay has to be optimized to prevent short

circuit in the matrix converter and also to avoid the undesirable waveform distortions which result from long commutation time delays.

It should be noted that for implementing the successful four-step commutation based on the input voltage, the accurate and reliable measurements of the input voltages is necessary. A short circuit can occur during the commutation process and destroying the matrix converter, if the sign of the input line-to-line voltage is not measured correctly.

For the case when the $V_A$ is less than $V_B$, the similar procedures can be used to determine the appropriate commutation sequence between bidirectional switches, $S_A$ and $S_B$.

## 3.5 Input Filter

The input filter is a significant component for matrix converter as it eliminates the high frequency distortions in the input current waveforms, which are generated by the PWM operation of the matrix converter at high switching frequencies. The input filter can also help to satisfy the electromagnetic interferences requirements [97].

The matrix converter input filter design has been addressed in a number of papers [98, 99] . Different configurations have been proposed for the matrix converter input filter. Such differences are a result of different design criteria, switching frequencies and modulation strategies. Three most common input filter configurations used in the matrix converter are the delta or star-

connection capacitors; second order LC filter and second order LC filter with damping resistor as shown in Figure 3.11.

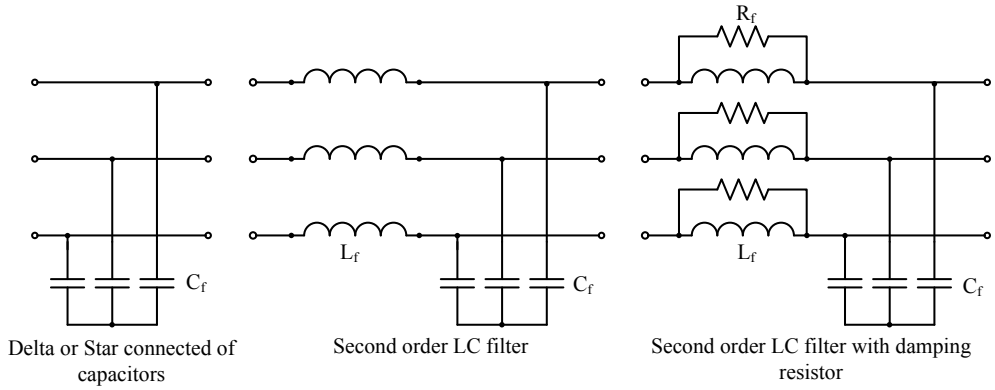



Figure 3.11: Input filter configurations for matrix converter

The design of the input filter is based on the switching frequency of the matrix converter to eliminate the frequency components around multiples of the switching frequency. The cut-off frequency of the input filter is lower than the switching frequency of the converter. The selection of an input filter components are based on the chosen cut-off frequency which is depended on the desired attenuation of the input current ripple.

## 3.6 Clamp Circuit

The matrix converter protection during faults is difficult due to the lack of energy storage elements in the matrix converter configuration, it is not possible to store energy that transfers from the inductive load. The fault condition in the matrix converter can be categorized as overcurrent and overvoltage [100]. The overcurrent in the matrix converter could occur due to a supply fault, converter commutation failure or abnormal operation of the load. Also if the two fundamental rules of the matrix converter are not satisfied,

extremely high fault currents can occur. An input overvoltage results from reasons such as the disturbance on the grid or improper start-up of the converter. An output overvoltage could occur due to the absence of a path for inductive load current in sudden turning off the converter. Additionally, the parasitic inductance among the bidirectional switches can be produce overvoltage at both sides of the matrix converter due to high *di/dt*.

Therefore, to protect the matrix converter during faults which could destroy the power semiconductor devices, a clamp circuit is needed. A typical clamp circuit provides a connection between the three-phase input supply and the load terminals of the converter as shown in Figure 3.12. This clamp circuit consists of two fast diode rectifier bridges, a clamp capacitor and a dissipation resistor. The load current path can be provided in the event of transient operations, suddenly shutdown converter or commutation failures. During a fault, the reactive energy stored in the load or supply inductance is transferred to the clamp capacitor.

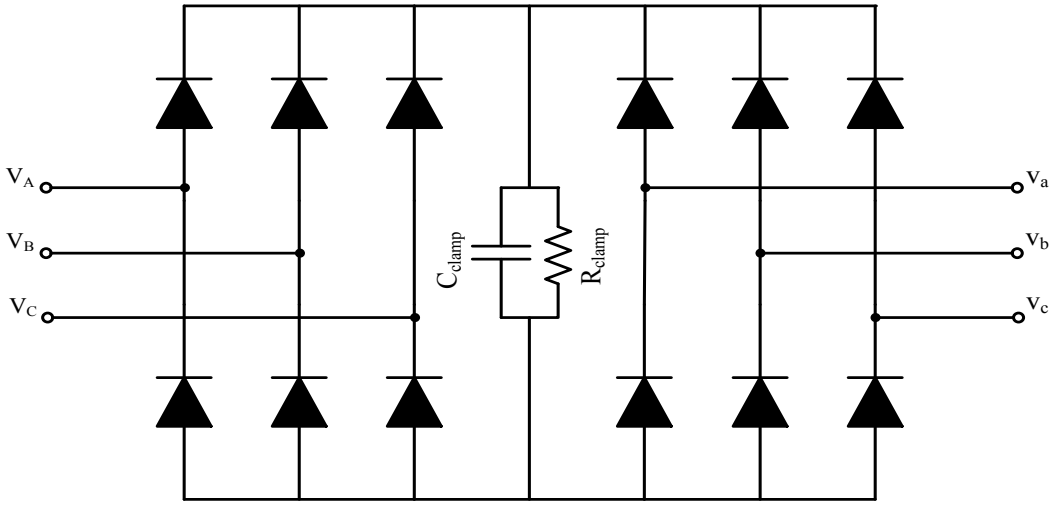



Figure 3.12: Clamp circuit for the matrix converter

The clamp capacitor must be designed to avoid an overvoltage risk to the semiconductor devices when the stored energy in the inductive load is transferred to the clamp capacitor during fault situations automatically. The value of the capacitor and its maximum voltage must be determined from the maximum energy stored in the inductive load and the maximum blocking voltage of used semiconductor devices. The maximum energy can be obtained from the load inductance at the time when the maximum current limit has been reached, as presented in [101]:

$$W_L = \frac{1}{2}L(i_a^2 + i_b^2 + i_c^2) = \frac{3}{4}L\hat{I}^2 \qquad (3.17)$$

where $W_L$ is the maximum energy stored in the load inductance; $L$. $i_a$, $i_b$ and $i_c$ are the three-phase load current. $\hat{I}$ is the overload current level which causes the matrix converter to shut down.

The maximum absorbed energy by the clamp circuit capacitor can be written in term of the change in energy of the capacitor from its initial voltage during normal operating condition to its maximum acceptable voltage as presented by:

$$W_C = \frac{1}{2}C_{clamp}(V_{max}^2 - V_{int}^2) \qquad (3.18)$$

where $C_{clamp}$ is the value of the clamp circuit capacitor, $V_{max}$ is the maximum permissible clamp voltage and $V_{int}$ as the initial voltage of the clamp capacitor, which is equal to the peak value of the input line voltage supplied to the matrix converter. The size of the clamp capacitor can be determined by taking into account (3.17) and (3.18) as presented by:

$$C_{clamp} = \frac{3}{2}\frac{L\hat{I}^2}{(V_{max}^2 - V_{int}^2)} \quad (3.19)$$

It should be considered in the selection of clamp circuit capacitor that the electrolytic capacitor type provides a greater amount of stored energy whereas the polypropylene capacitors have a better behaviour during transient operation [98].

## 3.7 Simulation Results

The three-phase matrix converter without input filter supplying a three-phase passive load has been simulated by Saber Software to demonstrate the performance of the matrix converter. Also simulation has been done for two different switching frequencies, 10 kHz and 80 kHz, to demonstrate some benefits of high switching frequency converter. The specifications of the converter are as follows:

- Rated input voltage and frequency: three-phase 230V (rms, phase voltage) and 50Hz mains supply.
- Rated output voltage and frequency: three-phase 117V (rms, phase voltage) and 400Hz.
- Rated apparent output power: three-phase 4.2kVA
- Displacement power factor ($\cos\varphi_i$): 0.92

Based on the given value for rated apparent output power, the apparent output power per phase can be determined by:

$$S_{ph} = \frac{4200}{3} = 1400\ VA \quad (3.20)$$

Load impedance can be calculated by:

$$Z = \frac{V^2}{S_{ph}} = \frac{117^2}{1400} = 9.78\Omega \quad (3.21)$$

Based on the given power factor, the load resistance and inductance can be calculated by:

$$R_L = Z \times \cos\varphi_i = 9.78 * 0.92 = 8.99\Omega \quad (3.22)$$

$$X = Z \times \sin\varphi_i = 9.78 * 0.39 = 3.82\Omega \quad (3.23)$$

$$L_L = \frac{X}{2\pi f_s} = \frac{3.82}{2*\pi*400} = 1.51mH \quad (3.24)$$

The converter is controlled using the space vector modulation strategy. A realistic model of the four-step commutation based on the output current direction is used to provide the safe current commutation between switching devices. The small time delays, $t_{d1}$, $t_c$ and $t_{d3}$ are used in the four-step current commutation and set equal to 100 nsec. The sampling frequency and simulation time step are set up based on the switching frequency of matrix converter.

The first simulation which has been run was the matrix converter with 10 kHz switching frequency. The three-phase output current of matrix converter is shown in Figure 3.13 while Figure 3.14 presents harmonic spectrum of output phase *a*. It can be noted that balanced and sinusoidal three phase output current waveforms are produced with output frequency of 400Hz. But as it is clear the output current waveforms are distorted and there are some high frequency harmonics presented in the output current spectrum.

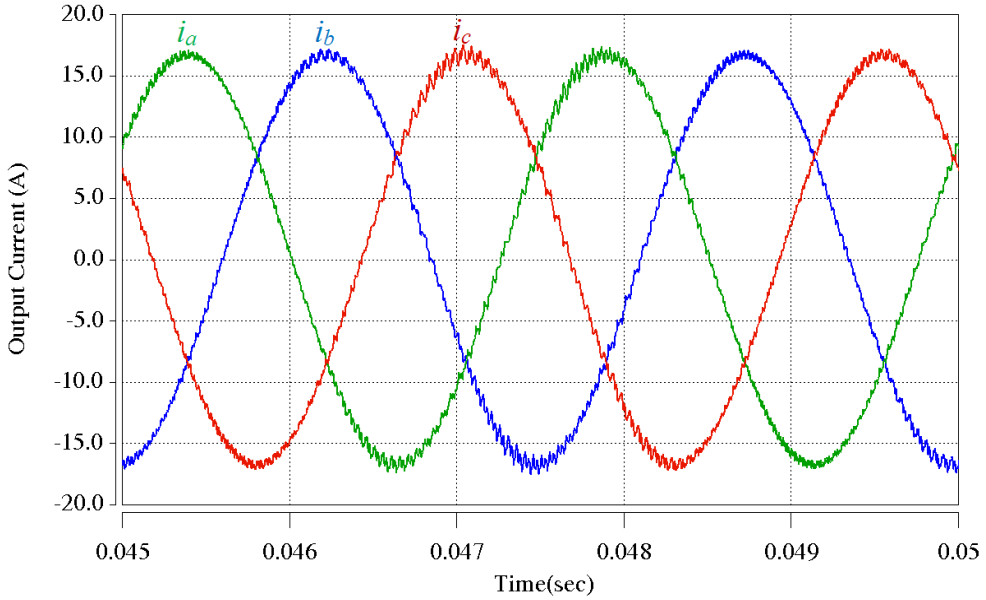



Figure 3.13: The three-phase output currents of matrix converter when the switching frequency is 10 kHz

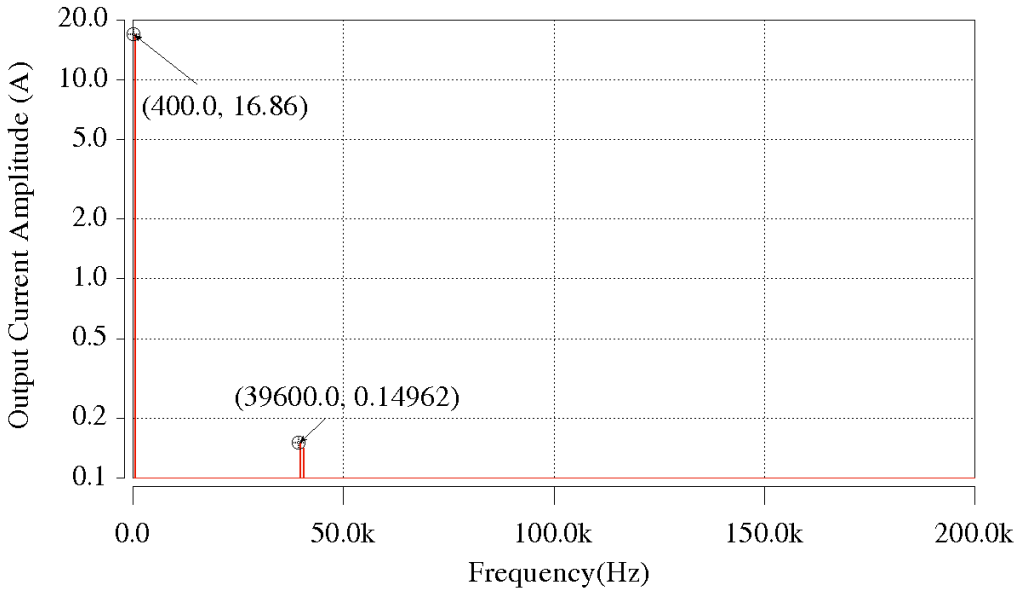



Figure 3.14: Harmonic spectrum of matrix converter output current, $i_a$, when the switching frequency is 10 kHz

The output current waveforms obtained when the switching frequency of matrix converter is 80 kHz are shown in Figure 3.15. The output phase *a* harmonic spectrum is shown in Figure 3.16. As it is clear, the output current waveforms are perfectly balanced and sinusoidal with output frequency of

400Hz. Also there is no significant distortion and high frequency harmonic in output current waveforms.

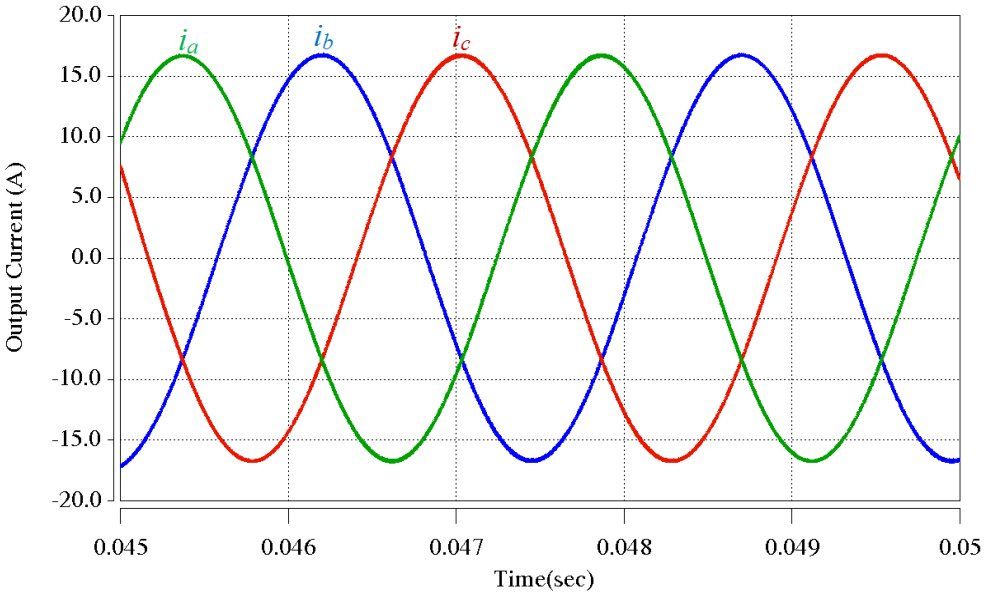



Figure 3.15: The three-phase output currents of matrix converter when the switching frequency is 80 kHz

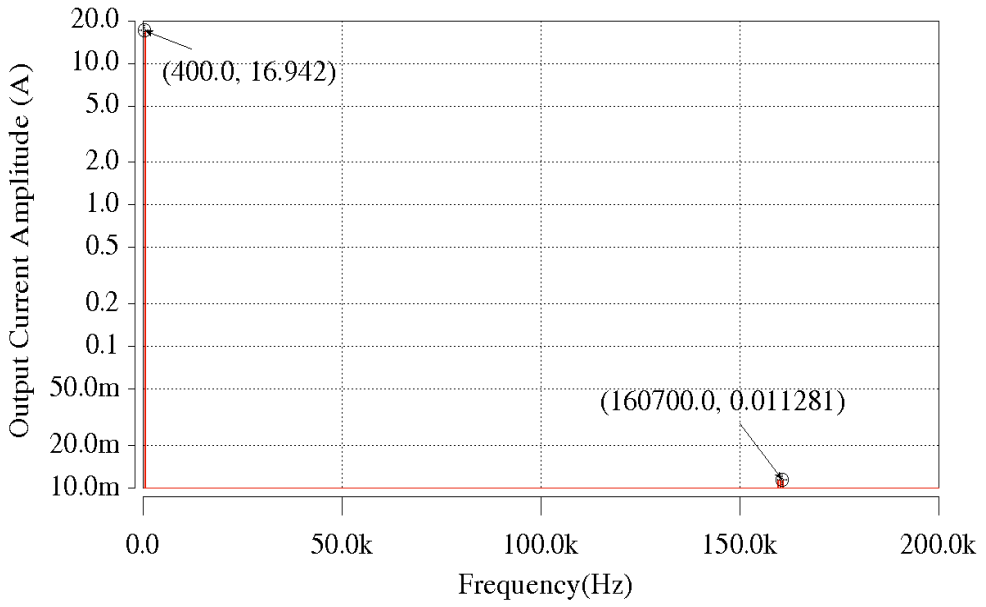



Figure 3.16: Harmonic spectrum of matrix converter output current, $i_a$, when the switching frequency is 80 kHz

The unfiltered input current spectrums of matrix converter for two switching frequencies have been obtained and presented in Figure 3.17. It is clear that the frequency of the first highest spike in the spectrums has increased by increasing switching frequency even though the amplitude of the ripples is the same. As the cut-off frequency of the matrix converter input filter is determined based on the first highest noise spike, so by increasing the switching frequency, the required attenuation is increased which result to higher cut-off frequency and lower value for passive components of the matrix converter input filter.

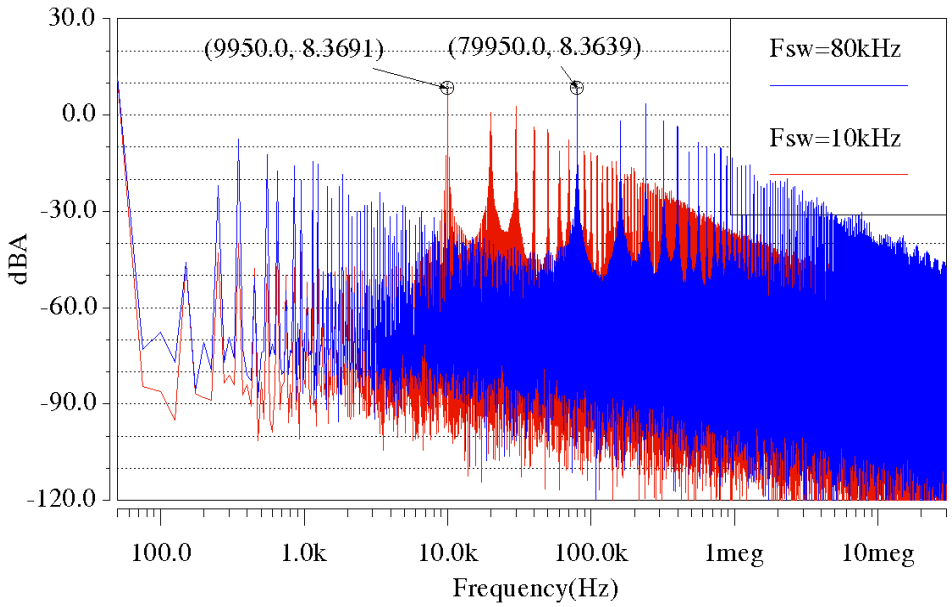



Figure 3.17: Spectrum of matrix converter unfiltered input current for different switching frequencies

## 3.8 Summary

In this chapter the three-phase to three-phase matrix converter topology has been reviewed. The matrix converter is a single power conversion stage using nine bidirectional switches. The matrix converter topology provides the

advantage of eliminating the request for any large energy storage elements. In order to demonstrate the relationship between the input and output voltages and currents using the switching states, the mathematical representation of the matrix converter is presented.

In order to maintain satisfactory system performance, the modulation schemes for the matrix converter based on the space vector modulation has been presented. The direct space vector modulation technique for matrix converter has been described.

The bidirectional switch configurations which are needed to implement matrix converter are explained in detail. The discrete power semiconductor switches and the diodes are arranged for each bidirectional switch because an ideal bidirectional switch is not available.

In order to avoid matrix converter damage due to a short circuit or an open circuit, the proper switching commutation sequence of the power devices has to be determined for safe current commutation from one bidirectional switch to another. The four-step current commutation strategies based on the output current direction and the input voltage sign have been described.

Additionally, in order to obtain good input current quality and to ensure the effective protection of the matrix converter from over voltages, the design of input filter and clamp circuit are presented.

Finally, to show the effectiveness of matrix converter, the simulation models of the matrix converter feeding a three-phase passive load for different switching frequencies have been presented. The simulation results show that

the matrix converter produces balanced, sinusoidal output current waveforms with controllable frequency of the output currents for the load. Also it has been shown that by increasing the switching frequency, it is possible to decrease the output current waveform distortion and increase the cut-off frequency for achieving lower value and volume for passive components of input filter of matrix converter.

# Chapter 4
# Hardware Prototype Implementation

In order to identify the switching phenomena and evaluate experimentally the switching losses of different SiC and Si devices within matrix converter, a laboratory prototype should be considered for implementation. Therefore, due to the need to evaluate four different semiconductor devices, four 2-phase to 1-phase matrix converters with same power circuit and different drive circuits have been implemented. The experimental rig is designed to be flexible with easy access to measure device currents and voltages.

In this chapter the overall structure of the 2-phase to 1-phase matrix converter prototype is presented. The design and the functionality of the power circuits including the clamp circuit, the drive circuit, the current direction detection and the measurement circuits are described in details. Finally, the

matrix converter control implementation based on a digital signal processor (DSP) and a field programmable gate array (FPGA) is explained.

## 4.1 Matrix Converter Power Circuit

The power circuit of matrix converter houses the matrix converter switches, diodes, clamp circuit, input filter capacitor, current direction detection circuit and measuring circuit. A schematic of the experimental rig which consists of clamp circuit, input filter and two bidirectional switches is shown in Figure 4.1. This forms the basis of the hardware of the 2-phase to 1-phase matrix converter which is a custom design for this project. The laboratory prototype of the 2-phase to 1-phase matrix converter is shown in Figure 4.2.

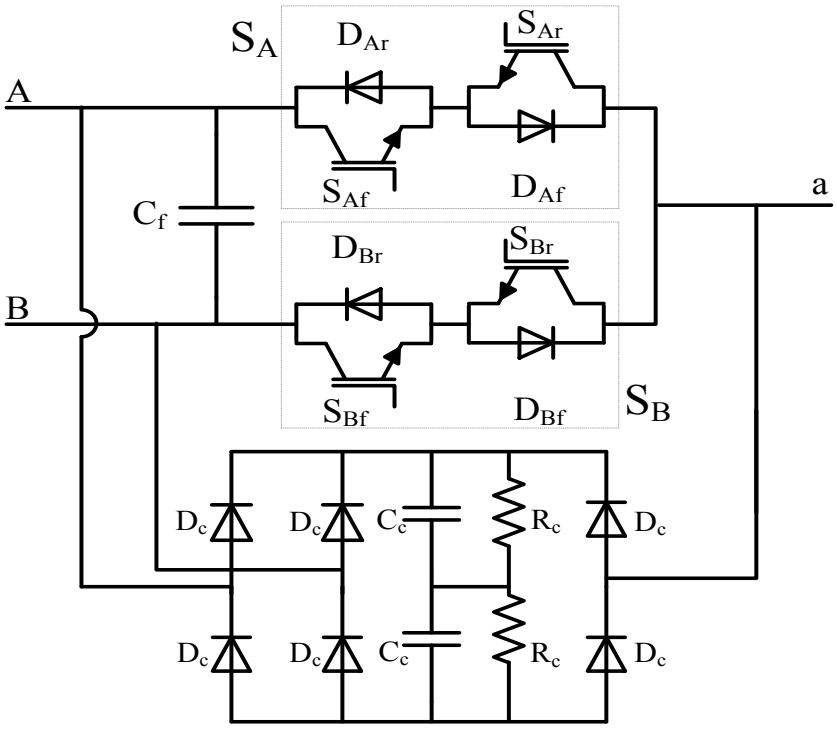



Figure 4.1: Schematic diagram of experimental rig

# Chapter 4: Hardware Prototype Implementation

A Printed Circuit Board (PCB) has been used for implementing the power circuit of matrix converter. The PCB of the matrix converter power circuit can be separated into two main areas which are High Current, high voltage conduction areas and Low voltage measurement signal areas; each of them needs different design considerations. The PCB of the matrix converter power circuit can be seen in Appendix B.

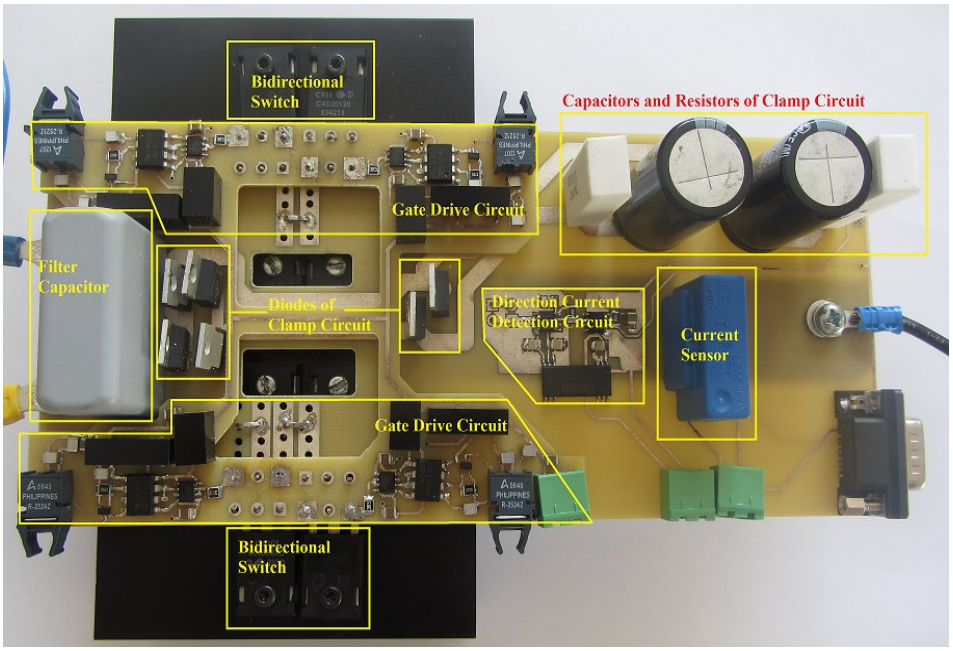



Figure 4.2: 2-phase to 1-phase matrix converter laboratory prototype

Different power devices switches and diode which are used in this work are listed in Table 4.1. The Package of the all switches and diodes is TO-247-3. Therefore, the four 2-phase to 1-phase matrix converters have the same PCB power circuit layout.

| Device | Model | Manufacturer | Package |
|---|---|---|---|
| Si IGBT+Diode | IKW15N120 | Infineon | TO-247-3 |
| SiC JFET | SJEP120R063 | SemiSouth | TO-247-3 |
| SiC MOSFET | CMF10120D | Cree | TO-247-3 |
| SiC BJT | BT1215AC | TranSic | TO-247-3 |
| SiC Diode | C4D20120D | Cree | TO-247-3 |

Table 4.1: Power devices are used in this work

### 4.1.1 High Current, High Voltage Conduction Areas

It is important to minimise any parasitic inductance when a circuit layout is designed for the high current, high voltage areas of the matrix converter. Due to high turn-off speed of the used switching devices, any inductance between the power switches, input filter capacitors and clamp diodes would lead to significant voltage spikes being generated at each commutation. The spikes of tens or even hundreds of volts which is greater than the voltage device ratings could be generated by the inductance of a short length of wire.

Laminated power planes are used for interconnections to ensure the parasitic inductance within the power circuit was minimised. The laminated power planes consist of a two layer PCB. The top layer of PCB is used for the clamp circuit, current direction detection circuit and current measuring circuit whereas the PCB bottom layer is used for the power circuit and input filter.

#### 4.1.1.1 High Voltage Implications

Adequate separation between layers and planes within layers is required to prevent occurrence of insulation breakdown due to the high voltage differences present within matrix converter power circuit. Dielectric strength of FR4 insulating material used within the PCBs is 20kV/mm approximately. The two layers PCB used has a FR4 thickness of 1.6 mm between layers, therefore the safe operating voltage between PCB layers is 32kV.

There is no material in the space between planes on individual layers so the air provides electric separation. The dielectric strength of air is 3kV/mm approximately. So to ensure the safe operating, a minimum separation between plane areas of 12 mm was allowed.

#### 4.1.1.2 High Current Implications

The required current capability is determined based on the current rating of switching devices. Due to the copper thickness is fixed by PCB manufacturer; the width of the planes is adjusted to obtain the desirable current capability. Also the amount of current has a significant effect on the temperature rise of the PCB which needs to be considered when designing the PCB power circuit.

The Institute for Interconnecting and Packaging Electronic Circuits (IPC) has provided a generic standard IPC-2221 for printed boards design [102]. Therefore based on the IPC-2221 standard, the width of copper required for a known copper thickness and acceptable temperature increase of the PCB and carry the required current is determined by equation (4.1) and (4.2).

$$A = \left[\frac{I}{(0.048 \times (\Delta T)^{0.44}}\right]^{0.725} \quad (4.1)$$

$$w = \frac{A}{1.378 \times \epsilon} \quad (4.2)$$

where $\Delta T$ is acceptable temperature increase (°C), $A$ is required cross sectional area of copper (mils$^2$), $\varepsilon$ is PCB copper thickness in (oz) as specified by IPC-2221 standard and $w$ is the required track width (mils).

Using the above equations, Table 4.2 is produced which shows the width of the copper plane required to carry the known current when the acceptable temperature increase is 10°C. These values are taken into account when the PCB power circuit of the matrix converter is designed.

| Current rating (A) | 5 | 10 | 15 | 20 | 25 |
|---|---|---|---|---|---|
| Required trace width (mm) | 10.10 | 16.70 | 22.41 | 27.61 | 32.46 |

Table 4.2: The required PCB copper widths for different currents

### 4.1.2 Low Voltage Measurement Signal

The power circuit PCB of matrix converter carries both low and high voltages. The drive circuit is implemented in separate board to ensure that the low voltage signals are as noise immune as possible, and protected from interference generated by the large voltage transitions presented in the high voltage areas. The output current measurement signal is a low voltage signal which is transmitted from the PCB power circuit as current. Due to being an

analogue signal, noise immunity is important. Therefore, the current measurement signal is shielded individually.

## 4.2 Drive Circuit

The switching signals generated from the control platform cannot be used to directly turn on and off the power devices of the matrix converter. Therefore, a drive circuit is needed to amplify and isolate these signals to drive the power switches. The drive circuit needs to provide specific voltage or current when the switching command state is sent from the FPGA. Additionally, the drive circuit provides electrical isolation between the low control platform and power devices.

A schematic diagram of the drive circuit for each bidirectional switch is presented in Figure 4.3. It consists of the buffer, the opto-coupler, the driver and the isolated power supply. Two switching signals generated from the FPGA are transmitted via optical fibres through the drive circuit to drive the forward and reverse direction devices in the bidirectional switch. The optical fibres provide both voltage isolation and good noise immunity.

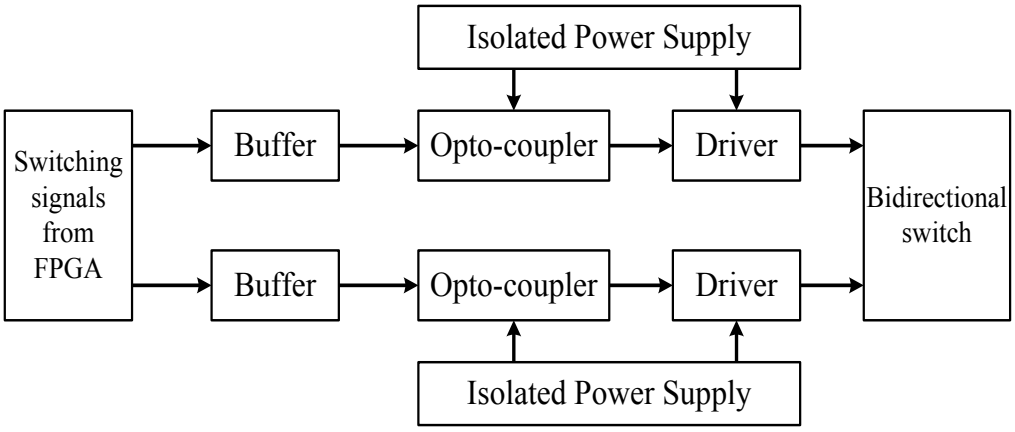



Figure 4.3: A schematic diagram of the drive circuit for each bidirectional switch

A single buffer (SN74LVC1G07DBR) is used to buffer each input signal. The open-drain output of the buffer together with a 270Ω pull-up resistor is used to provide the current required by an opto-coupler.

In order to place the drive circuit very close to its bidirectional switch, it has been made in different PCB. The power circuit PCB of matrix converter is plugged in the drive circuit PCB, so by this method the distance between power circuit board and drive board has been minimized and parasitic effects have been reduced. For instance, the drive circuit PCB of the SiC BJT can be seen in Appendix B.

The need to develop suitable drive circuit in pursue of full utilization of the power semiconductor devices high speed capabilities has hence become apparent, where the major obstacle faced has been the different specifications of components. In the following section, different specifications for driving

power devices and gate or base drives which are developed and used for implementation within a bidirectional switch of matrix converter are presented.

### 4.2.1 Si IGBT Gate Drive

The Si IGBT is a voltage controlled switching device that needs very small current during the switching period. To charge and discharge the internal capacitances of IGBT during switching operations, the gate drive circuit must have the source and sink capabilities. The schematic diagram of the gate drive circuit for the IGBT bidirectional switch is shown in Figure 4.4.

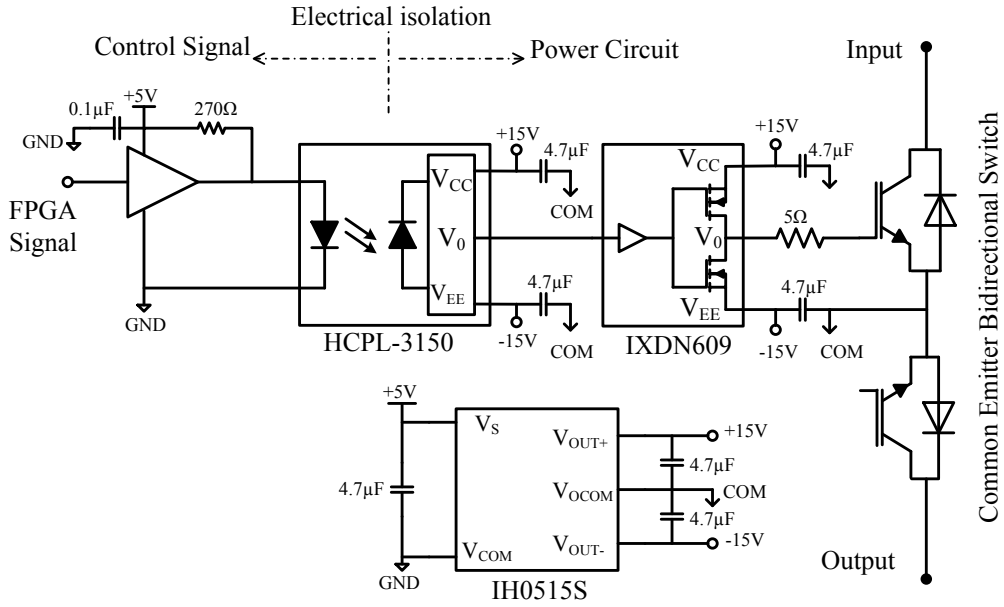



Figure 4.4: Schematic diagram of the gate drive circuit for the Si IGBT bidirectional switch

Due to the high voltage operating range of the bidirectional switch, the opto-coupler (HCPL-3150) is needed to provide the electrical isolation between the control circuitry ground and the bidirectional switch local ground. The opto-coupler (HCPL-3150) has high common mode transient immunity

(15kV/μsec) and can operate from 15 to 30V. In order to achieve the lowest turn on and off time for the IGBT switch, the driver (IXDN609) is used to enhance the source and sink capabilities of the gate drive circuit. The driver (IXDN609) provides 30V swing and up to 9A. The output of this driver is fed to the gate of each IGBT through the gate resistor. The gate resistor used has the same value as recommended by the device manufacturer and was determined to optimize the turn on and off time of the devices.

The gate drive circuit is powered by a 2W isolated DC/DC converter (IH0515S) which generates the dual voltage supply ±15V from a 5V supply for the output of the opto-coupler and the driver.

### 4.2.2 SiC MOSFET Gate Drive

The SiC MOSFET requires very small current during the switching period due to it is a voltage controlled switching device same as Si IGBT. The gate drive circuit must have the sink and source capability to charge and discharge the internal capacitance of SiC MOSFET during the switching period. Figure 4.5 shows the schematic diagram of the gate drive circuit for the common source SiC MOSFET bidirectional switch.

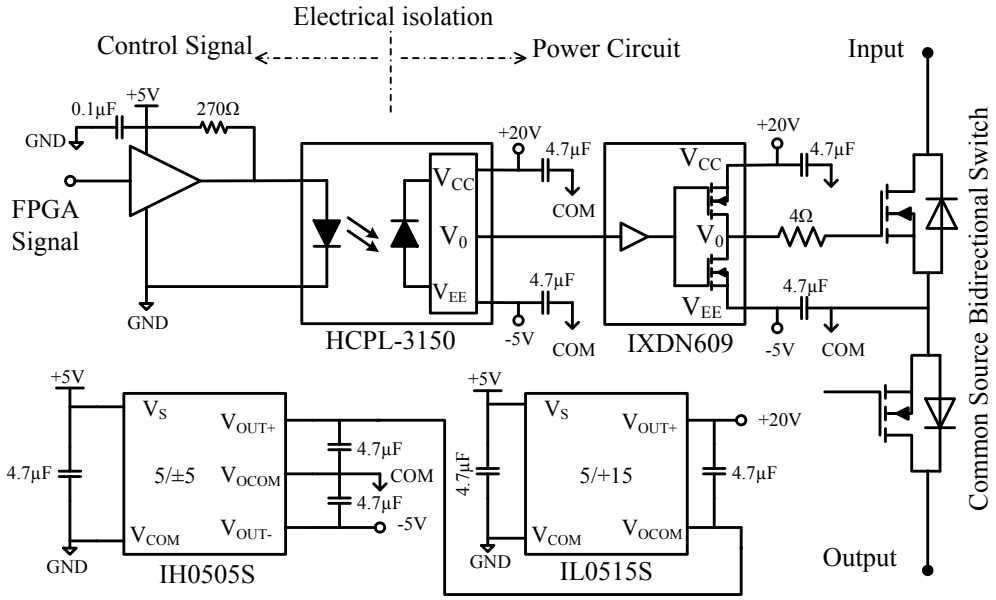



Figure 4.5: Schematic diagram of the gate drive circuit for the SiC MOSFET bidirectional switch

The gate drive circuit provides +20V between gate and source of the SiC MOSFETs to switch device on when the digital signal from FPGA is high and -5V between gate and source of the SiC MOSFETs to switch device off when the digital signal from FPGA is low. The on and off state driving voltages of SiC MOSFET have been recommended by the manufacturer of device (Cree). This is achieved through the use of opto-coupler (HCPL-3150) and driver (IXDN609). The opto-coupler which has high common mode transient immunity provides electrical isolation for the control signal. Moreover, driver which has a fast drive capability provides 25V swing between gate and source of SiC MOSFET. The output of drive is fed to the gate of the SiC MOSFET through the gate resistor. To minimize the turn on and off time of the SiC MOSFET, the recommended gate resistor by the device manufacturer is selected.

Two 2W isolated DC/DC converter (IH0505S and IL0515S) which generates the dual voltage supply ±5V and +15V from a 5V respectively are used to provide +20V and -5V and power the gate dive circuit.

### 4.2.3 Normally-off SiC JFET Gate Drive

Normally-off SiC JFET makes special demands on the gate driver circuit compared to other unipolar SiC or Si devices. To fully exploit the potential of normally-off SiC JFETs, conventional gate driver circuits for unipolar switches need to be adapted for use with these switches. During on-state of the normally-off SiC JFET the gate-source voltage must not exceed 3 V, while a current of around 150 mA (depending on the desired on-state resistance) must be fed into the gate. Additionally, during switching operation of the device the transient gate voltage should be from -15V (off) to +15V (on). Also the low threshold voltage of less than 0.7 V of normally-off SiC JFET requires high noise immunity. A gate drive circuit is developed in order to overcome the current limitations while still having a low circuit complexity. In the developed gate drive as shown in Figure 4.6 is based on AC coupling circuit. It is consist of a gate resistor ($R_g$) and a speed up capacitor ($C_c$). The gate resistor is used to set the DC operating point in the on-state by dropping the potential difference between the high level output of the driver and the required gate source voltage of the SiC JFET at a specified gate current. The speed up capacitor is used to rapidly deliver or remove the dynamic gate charge for a fast turn on and off. When the input capacitor of SiC JFET is fully charged steady state conditions will be regulated by the gate resistor. An additional low resistance ($R_c$) is

included in series with the speed up capacitor to dampen any observed gate ringing.

The proposed gate drive circuit is designed to control the 1.2kV-30A normally-off SiC JFET (SJEP120R063) from SemiSouth. Based on the main drive technical specifications of the normally-off SiC JFET which are listed in Table 4.3, the components value of the gate drive circuit can be determined by (4.3)-(4.5).

| Gate-source voltage ($V_{ge}$) | Gate current ($I_g$) | Peak gate current ($I_{gp}$) | Gate charging time ($T_{ch}$) | Supply voltage ($V_{cc}$) |
|---|---|---|---|---|
| 2.5 V | 0.15 A | 2 A | 100 nsec | 3.3 V |

Table 4.3: The main drive technical specifications of the SiC JFET

$$R_g = \frac{V_{cc}-V_{ge}}{I_g} = \frac{3.3-2.5}{0.15} = 5.3 \cong 5.6\ \Omega \qquad (4.3)$$

$$R_c = \frac{V_{cc}}{I_{gp}-\frac{V_{cc}}{R_g}} = \frac{3.3}{2-\frac{3.3}{5.3}} = 2.39 \cong 2.4\ \Omega \qquad (4.4)$$

$$C_c = \frac{I_{gp}T_{ch}}{V_{cc}} = \frac{2*100\times10^{-9}}{3.3} = 60\times10^{-9} \cong 68\,nF \qquad (4.5)$$

The other components of the drive circuit are similar to drive circuit of Si IGBT and SiC MOSFET which provides 18.3V output swing and up to 9A of current. The gate drive circuit is powered by two 2W isolated DC/DC

converters (IL0503S and IL0515S) which generates the voltage supply +3.3V and +15V respectively.

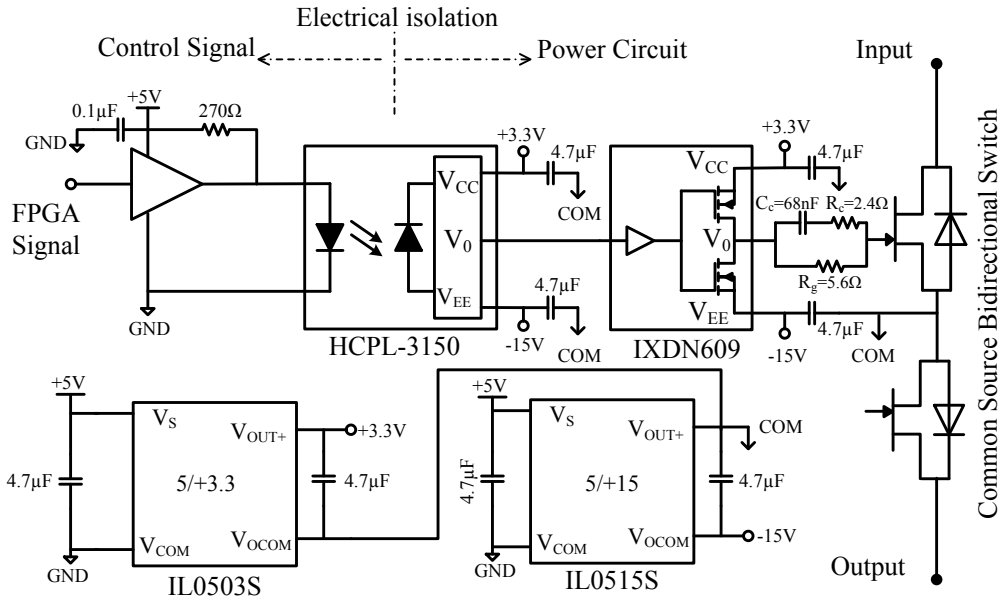



Figure 4.6: Schematic diagram of the gate drive circuit for the normally-off SiC JFET bidirectional switch

### 4.2.4 SiC BJT Base Drive

The base drive requirements of SiC BJTs are totally different from Si BJTs due to the SiC BJT does not rely on high injection and there is no problems with storage times at turn off. Also if the reverse base current during the turn off is too high, the SiC BJT does not have problem with trapped charge. Thus, these features make it clear that the design criteria of SiC BJT are different from Si BJT.

The main argument against the SiC BJT is the base current when it is in the on-state due to it must be produced by the base drive circuit and the amount of required base current is not negligible. Typical values of the common emitter

gain are of the order 60, which mean that a 30A SiC BJT would need a base current of the order of 0.5A. A well-known base drive circuit that improves the switching transients is an AC coupling circuit as illustrated in Figure 4.7. It is consists of a base resistor ($R_b$) and a speed up capacitor in parallel with resistor. The capacitor is charged up to a voltage level equal to the voltage difference between $V_{CC}$ and $V_{BE(SAT)}$ during the turn on transition of SiC BJT and so creating a low impedance path for the base current. In addition, the capacitor provides a negative voltage which applied across the base emitter terminals during the turn off transition of the SiC BJT. This causes improvement in the turn off transient.

The proposed base drive circuit is designed to control the 1.2 kV- 20A SiC BJT (BT1215AC) from TranSiC. Based on the main drive technical specifications of the SiC BJT which are listed in Table 4.4, the components value of the base drive circuit can be determined by:

| Base-emitter voltage ($V_{BE}$) | Base current ($I_b$) | Peak base current ($I_{bp}$) | Base charging time ($T_{ch}$) | Supply voltage ($V_{cc}$) |
|---|---|---|---|---|
| 3.1 V | 0.3 A | 3 A | 100 nsec | 5 V |

Table 4.4: The main drive technical specifications of the SiC BJT

$$R_b = \frac{V_{cc} - V_{BE}}{I_b} = \frac{5-3.1}{0.3} = 6.3 \cong 6.8\,\Omega \qquad (4.6)$$

$$R_c = \frac{V_{cc}}{I_{bp} - \frac{V_{cc}}{R_b}} = \frac{5}{3 - \frac{5}{6.3}} = 2.26 \cong 2.2\,\Omega \qquad (4.7)$$

$$C_c = \frac{I_{bp}T_{ch}}{V_{cc}} = \frac{3*100\times10^{-9}}{5} = 60 \times 10^{-9} \cong 68\,nF \qquad (4.8)$$

The other main components of the drive circuit are opto-coupler and driver. The opto-coupler (HCPL-7721) which has high common mode transient immunity (10kV/μsec) and operates from 4.5 to 5.5V provides electrical isolation for the control signal. Additionally, driver (IXDN609) provides 5V output swing and up to 9A of current. A 3W isolated DC/DC converters (IZ0505SA) which generates the voltage supply +5V is used to power the opto-coupler and driver.

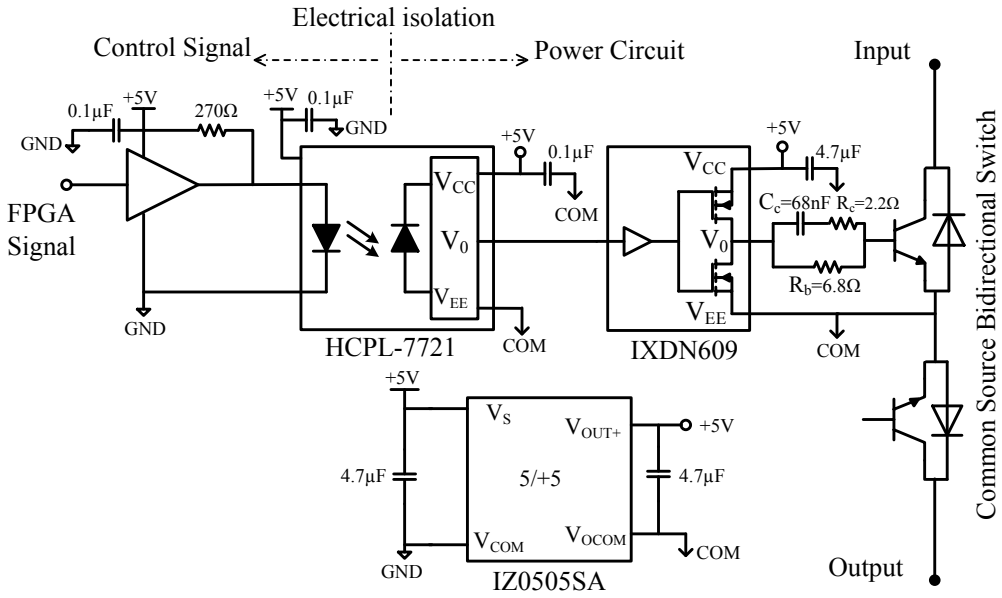



Figure 4.7: Schematic diagram of the gate drive circuit for the SiC BJT bidirectional switch

## 4.3 Clamp Circuit

The matrix converter has no large storage element in its structure in compare to the traditional DC-link voltage source inverter. The clamp circuit is

needed to protect the matrix converter. The schematic diagram of the clamp circuit connected between the input and output phases of the 2-phase to 1-phase matrix converter is presented in Figure 4.1.

It can be seen that the clamp circuit consists of a diode rectifier bridge with the clamp capacitors connected in parallel to their corresponding bleed resistors. SiC didoes (C2D10120A) are employed to construct the rectifier circuit which are populated on the top layer of the PCB power circuit. Theses SiC diodes are rated at 1200V and 8A and provide the desired characteristics of short reverser recovery time and the low forward voltage drop. Two 150μF, 450V electrolytic capacitors are connected in series connection and their dissipated resistor of 47kΩ are mounted on the top layer of the PCB power circuit of this laboratory prototype.

To protect the matrix converter under unhealthy operating conditions, the reactive energy stored in the load inductance is transferred to the clamp capacitor. A current path is provided by the diodes turning on in the clamp circuit in the fault situation such as the commutation failure between switches or open-circuit faults in the power switches. All of the inductive load energy can be safely transferred to the clamp capacitor and then dissipated in the paralleled resistor.

## 4.4 Current Direction Detection Circuit

The four-step current commutation strategy described in Chapter 3 is used to satisfy the safe current commutation requirements of the bidirectional switches. This commutation technique relies on knowledge of the current

direction in output phase of matrix converter. Therefore, the accurate detection of the output current direction plays a significant role in the correct switching operation of the power devices.

The schematic diagram of the current direction detection circuit is shown in Figure 4.8. A pair of anti-parallel SiC Schottky diodes is connected to the output phase of the matrix converter. These diodes have a current rating of 20A. They provide the preferred characteristics of a very low forward voltage drop and high frequency operation which are required for the accurate of the output current detection.

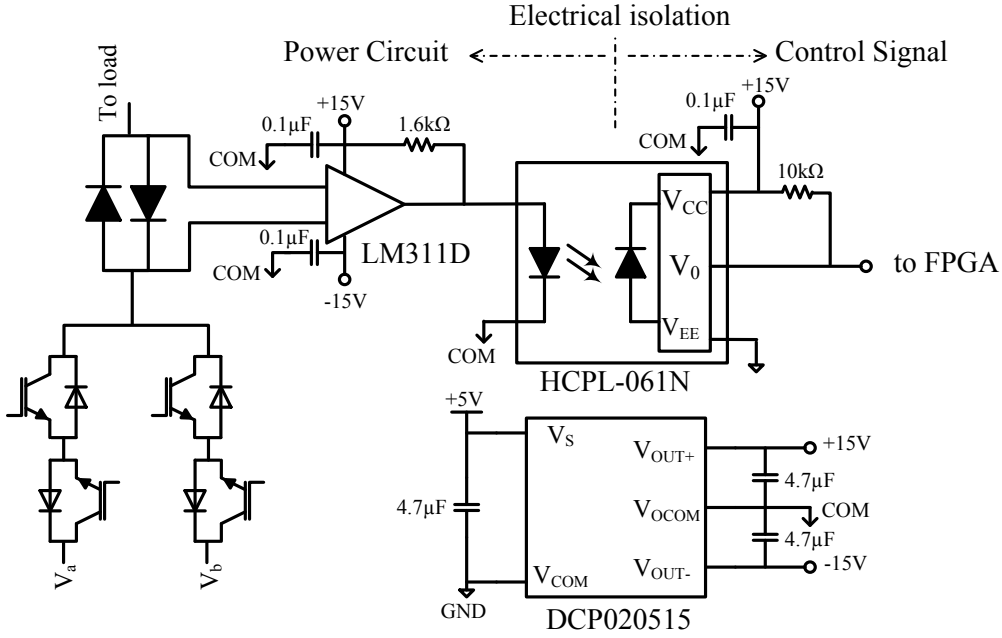



Figure 4.8: The schematic diagram of the current direction detection circuit

LM311D as voltage comparator is used to compare the voltage across the two antiparallel diodes, providing the logic signal for the output of the current direction circuit. The comparator output drives a high speed opto-coupler

(HCLP-061N). This opto-coupler is suitable as the high speed logic interface to achieve the logic signal compatibility and to obtain the electrical isolation between the power circuit and control signal transmitted to the FPGA.

The isolated DC/DC power converter (DCP020515) is needed to supply the current direction circuit. The control platform ground is separate from the circuit local ground.

## 4.5 Measurement Circuit and Techniques

The transient voltage and current waveforms for each switch and output current of matrix converter are needed to record and measure.

A current transducer used to measure the output current of the matrix converter is Hall effect LAH 25-NP manufactured by LEM. This current transducer has many features such as excellent accuracy, a wide frequency bandwidth of 200 kHz and high immunity to external interference while information is being transferred to the control platform. This transducer provides a galvanic isolation between the power circuit and control platform.

A schematic diagram of the current measurement circuit used to measure output phase current is shown in Figure 4.9. The primary terminals of the transducer are connected in series with the output phase. The measured current generates a secondary current in the transducer with a conversion ratio of 1:1000. The secondary output current flowing through a measurement resistor, $R_m$, produces a voltage signal which is sent to the A/D channel on the FPGA board.

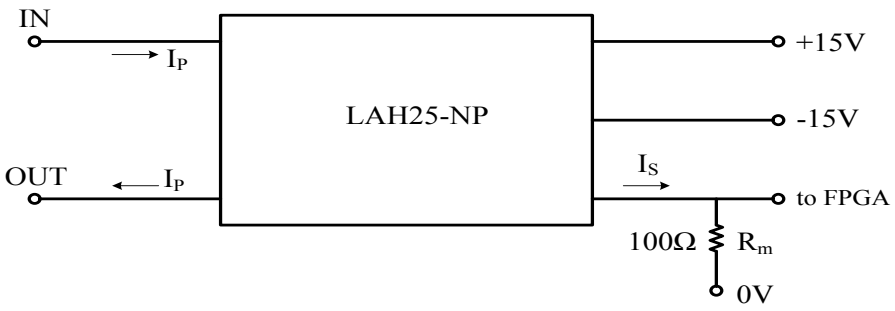



Figure 4.9: Schematic diagram of the current measurement circuit

Switching current waveform of devices in matrix converter is measured using a Rogowski current transducer. The CWT 03B Ultra Mini Rogowski current transducer provided by PEM consists of a coil, an electronic integrator unit and a BNC-BNC output cable. The clip around Rogowski coil is thin enough to insert into a leg of the power device switch with TO-247-3 package without increasing the parasitic inductance. The integrator provides a conversion of the measured current to a voltage signal. So, the integrator output can be connected to an oscilloscope directly.

The Rogowski current transducer provides several desirable features such as a very high frequency bandwidth (up to 20MHz), a high sensitivity of 100mV/A and a thin-flexible coil current probe which can insert in the confined spaces easily.

Voltage measurements are made using differential voltage probe with a bandwidth of 100MHz. The delay in the current and voltage measurements due to the signal processing and cabling are taken into account.

## 4.6 Control Board

This section describes the control implementation for the matrix converter based on a digital signal processor (DSP) and a field programmable gate array (FPGA). An interface cards (HPI daughter card) is incorporated into the control platform. By interfacing the HPI daughter card with the DSP board a bidirectional data transfer between the host PC and the DSP can be achieved to control the matrix converter and download the capture system data.

The overall structure of the control implementation for the matrix converter is shown in Figure 4.10. The voltage and current signals provided by the measurement circuits are transferred to a bank of A/D channels on the FPGA card. The current direction detection circuits provide information for the four-step current commutation technique which is implemented in the FPGA. Switching signals for safe commutation of the bidirectional switches are then transmitted to the gate drive circuit. The modulation technique used to control the matrix converter is implemented on the DSP.

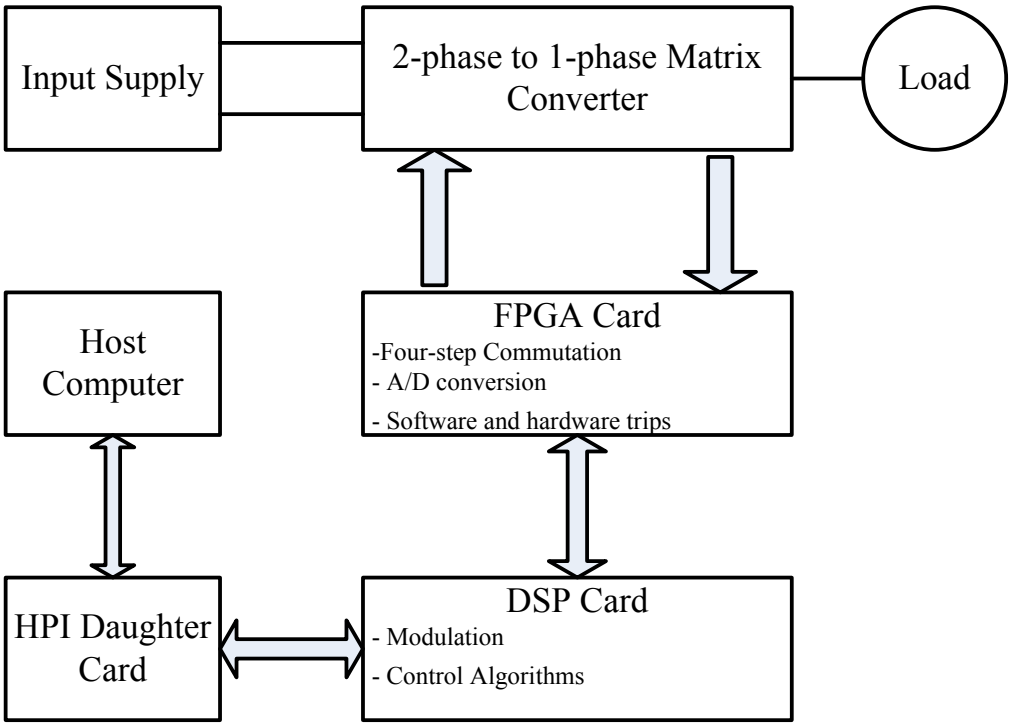



Figure 4.10: Diagram of overall matrix converter control implementation

### 4.6.1 Digital Signal Processor (DSP)

A high performance Texas Instruments TMS320C6713 floating-point signal processor with the DSP Start Kit (DSK) is employed to provide fast and effective control of the matrix converter. This device operates with a clock frequency of 255MHz and is able to deliver up to 1800 million instructions per second. The DSP source code for the control of the matrix converter was developed in the C language for previous project at the PEMC group of the University of Nottingham. The existed DSP source code is modified based on the requirements for controlling the2-phase to 1-phase matrix converter. The Code Composer Studio (CCS), an Integrated Development Environment (IDE)

for the host PC, communicates with the DSK using a USB host interface for DSP code creation, debugging and analysis for the real time applications.

All the calculation for the modulation technique is performed in the DSP. This process is executed at every interrupt interval, corresponding to the switching frequency. The voltage signals which represent the measured voltages and currents are simultaneously transmitted from the FPGA to the DSP through the resistor memory map. These signals are reconverted to the actual analogue values by scaling with their multiplicative factors.

### 4.6.2 Field Programmable Gate Array (FPGA)

A high performance Actel ProASIS3 FPGA card which has been designed and developed at the PEMC group of the University of Nottingham is used in control board [103]. This very flexible and versatile FPGA card is interfaced with the high speed TMS320C6713 DSP to control the matrix converter. The ten 12-bit A/D conversion channels and their individually software-configurable trip circuit are included on the FPGA card. The switching signals are transmitted to the gate drive circuits through fibre optic cable interfaced with the appropriate transmitters and receivers to provide both voltage isolation and good noise immunity.

To protect the matrix converter, the FPGA can turn off the power switches automatically when a trip signal is observed. Several types of trip are taken into consideration to ensure the safe operation of the matrix converter. There are two switches, a push button switch and a toggle switch, connected to the

FPGA card in order to reset the trips and enable/disable the matrix converter, respectively.

## 4.7 Summary

In this Chapter the experimental implementation of the laboratory prototype 2-phase to 1-phase matrix converter has been described. The matrix converter PCB power circuit implementation consists of the power devices and diodes, the input filter, the clamp circuit, the current direction detection circuit and the measurement circuit. The drive circuit has been implemented in separate PCB which was plugged in the PCB power circuit. The design of the PCB power circuit and drive circuit board have been described in details. The explanation of the functionality and construction of the components used in each circuit has also been given. The control implementation of the matrix converter has been achieved using the high performance DSP and FPGA platform.

# Chapter 5
# Power Losses Evaluation

Accurate semiconductor loss data is required to assess different power semiconductor device technologies for AC/AC converter applications. The semiconductor losses can be subdivided into conduction and switching losses. Conduction losses depend on the forward and reverse characteristics or static characteristic of the power semiconductor device. The switching losses are typically calculated in terms of the device turn-on and turn-off switching energies.

This Chapter concentrates on the static and dynamic characterization of some sample power semiconductor devices from different technologies in controlled condition in the 2-phase to 1-phase matrix converter to allow a fair comparison between them. Then based on the obtained data, the power loss performance of the matrix converter which is built by SiC and Si power

semiconductor devices have been compared in different conditions. The power devices under investigation in this Chapter are listed in Table 5.1.

| Power device | Model | Manufacturer | Voltage(V) | Current(A) |
|---|---|---|---|---|
| Si IGBT+diode | IKW15N120 | Infineon | 1200 | 30 |
| SiC JFET | SJEP120R063 | SemiSouth | 1200 | 30 |
| SiC MOSFET | CMF10120D | Cree | 1200 | 24 |
| SiC BJT | BT1215AC | TranSiC | 1200 | 20 |
| SiC Diode | C4D20120D | Cree | 1200 | 16 |

Table 5.1: Different power devices under static and dynamic characterizations

## 5.1 Power Losses of the Si IGBT

A third generation of Si IGBTs which are named T&FS IGBT and are suitable for operation in switching frequency range of 20 kHz and 100 kHz and offering very low collector-emitter saturation voltage ($V_{CEsat}$) and fast switching are chosen for comparing with other available SiC power semiconductor devices. The selected Si IGBT device is IKW15N120H manufactured by Infineon technology with current rating and blocking voltage of 30A and 1200V at temperature of 25°C, respectively. Also a fast recovery diode is connected antiparallel with the IGBT inside the package.

### 5.1.1 On-state Performance of the Si IGBT

The on-state performance of a Si IGBT is described by the forward output characteristic, on-state resistance and antiparallel diode forward characteristic. The IGBT forward output and its antiparallel diode forward characteristics are measured with a curve tracer. Figure 5.1 shows the IGBT forward output characteristic when its gate-emitter voltage is 15V for different temperatures. The antiparallel diode forward characteristic for different temperatures also is shown in Figure 5.2. It is clear that the curve slope and on-state voltage are decreased slightly by increasing temperature. So it can be stated that the on-state performance of the Si IGBT is slightly temperature dependent.

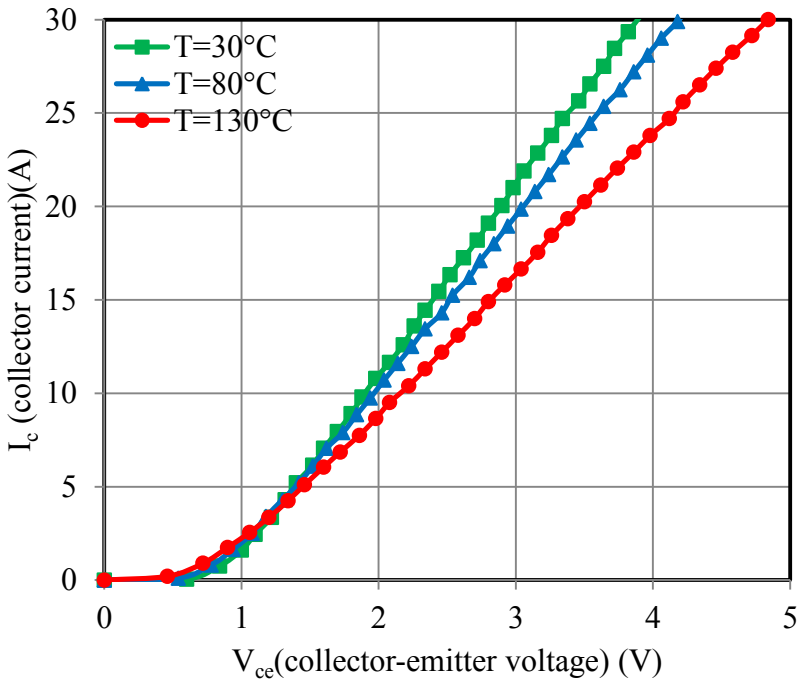



Figure 5.1: Forward output characteristic of the Si IGBT

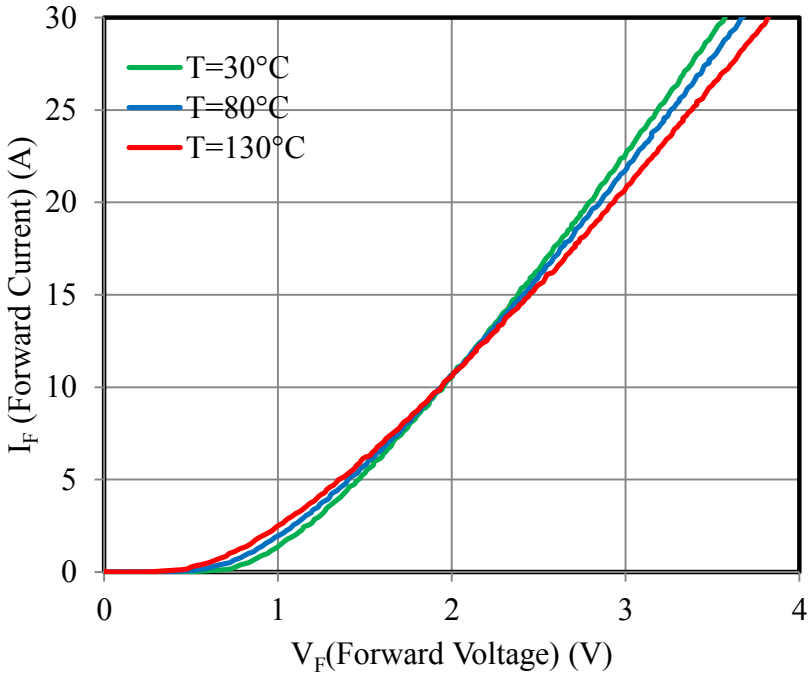



Figure 5.2: The forward characteristic of the IGBT antiparallel diode

The on-state voltage of the IGBT and diode are defined as on-state zero current collector-emitter voltage of IGBT and on-state zero current forward voltage of diode. The on-state voltage of the IGBT and diode for different temperatures are presented in Figure 5.3. It can be noted that the on-state voltages have reduced slightly by increasing temperature.

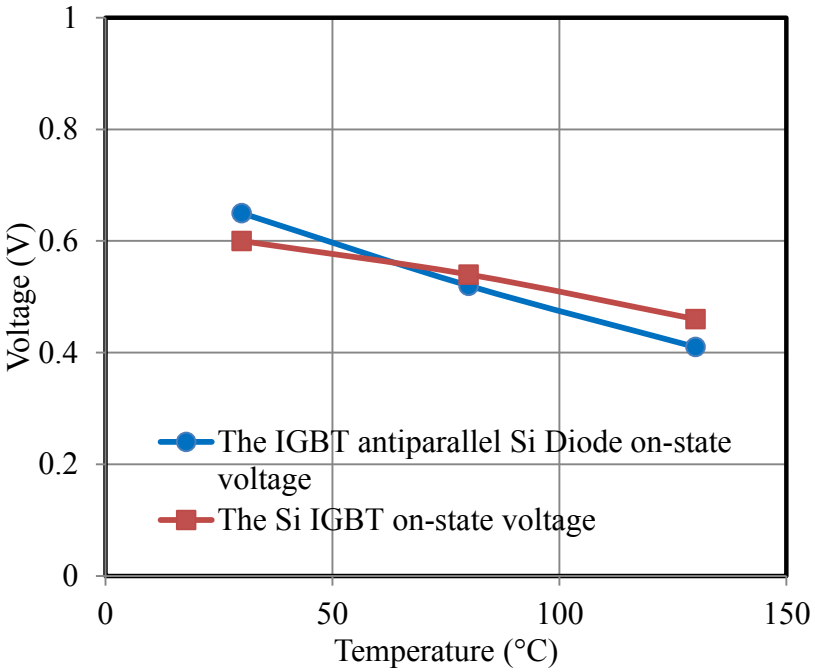



Figure 5.3: The Si IGBT and its antiparallel diode on-state voltages for different temperatures

The on-state resistance of the Si IGBT and its antiparallel diode can be determined by calculating the slope of their forward characteristics in the linear region. Figure 5.4 shows the calculated on-state resistance of the Si IGBT and its antiparallel diode for different temperatures. It is obvious that the on-state resistances have increased slightly by increasing temperature.

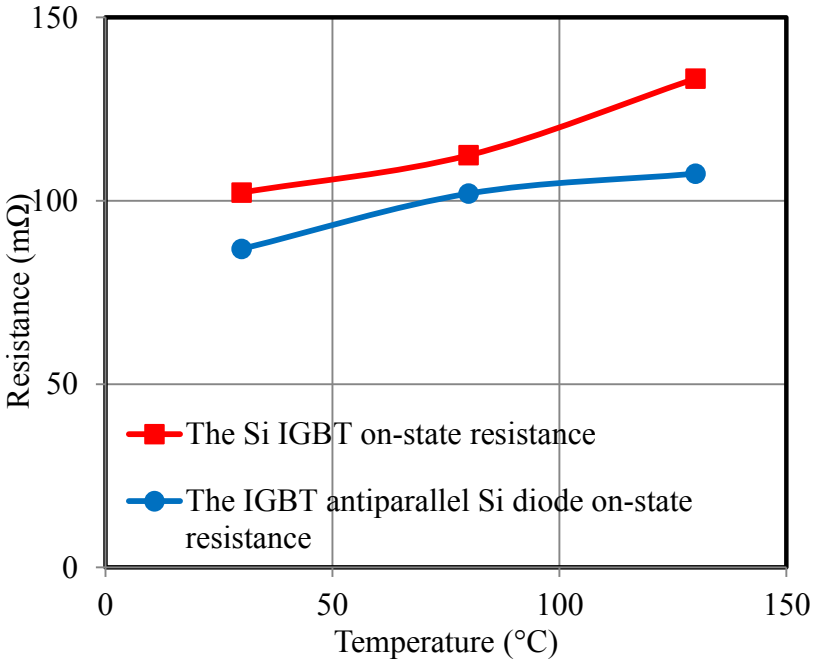



Figure 5.4: The Si IGBT and its antiparallel diode on-state resistances for different temperatures

The Si IGBT can be modelled with a voltage source which representing the IGBT on-state zero current collector-emitter voltage and the IGBT on-state resistance during conduction mode based on its on-state performance. Also the IGBT antiparallel diode can be modelled with a voltage source which representing the forward voltage of diode and the diode on-state resistance. Therefore the IGBT and diode forward characteristics can be linearized into the form:

$$V_{ce}(I_c, T) = V_{ce-on}(T) + R_{ce-IGBT}(T) \times I_c \qquad (5.1)$$

$$V_{diode}(I_{diode}, T) = V_F(T) + R_{diode}(T) \times I_{diode} \qquad (5.2)$$

where $V_{ce\text{-}on}$ is on-state zero current collector-emitter voltage of the IGBT and $R_{ce\text{-}IGBT}$ is the on-state resistance slope. Also $V_F$ is the forward voltage drop across the diode and $R_{diode}$ is the on-state resistance slope of the diode forward

characteristic. Figure 5.5 shows the electrical schematic of the IGBT and its antiparallel diode electrical models during conduction mode.

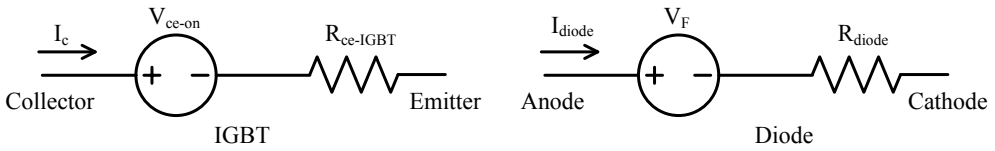



Figure 5.5: The electrical models of the IGBT and diode during conduction

### 5.1.2 Dynamic Performance of the Si IGBT

The dynamic characterization of Si IGBT is evaluated by the developed 2-phase to 1-phase Si IGBT matrix converter. The dynamic characterization of the Si IGBT is described based on the hard turn-on and turn-off switching of power semiconductor device in the matrix converter and then calculating the associated switching energy losses.

The voltage and current hard turn-on and turn-off switching waveforms of the Si IGBT have been measured at 30°C, 80°C and 130°C when the input voltage is 200V, 300V and 400V and the load current is 6A, 9A and 14A. The measured collector-emitter voltage and collector current waveforms of hard turn-on and turn-off switching of Si IGBT in a bidirectional switch of the matrix converter when the input voltage is 400V and the load current is 14A for different temperatures are shown in Figure 5.6 and Figure 5.7 respectively. It can be noted that the gradients of current and voltage waveforms are decreased slightly by increasing the temperature of power semiconductor device.

The turn-on time ($t_{on}$) is defined as the time from the current rising to 10% of its peak value until the voltage falls to 10% of the blocking voltage value. Similarly, the turn-off time ($t_{off}$) is defined as the time from the current falls to 90% of its peak value until the voltage rise to 90% of the blocking voltage value. Therefore, the turn-on and turn-off switching time of the Si IGBT at 400V is about 210ns and 345ns which are increased slightly by increasing power device temperature. It can be seen form Figure 5.6 that there is a voltage drop across the collector-emitter of the Si IGBT during current rising which is due to the parasitic inductance of the circuit. Also the reverse recovery current of the diode causes a current overshoot in the collector current of the Si IGBT during the turn-on switching. Additionally the parasitic inductance of the circuit causes a voltage overshoot across the collector-emitter of the Si IGBT during the turn-off switching which is obvious in Figure 5.7.

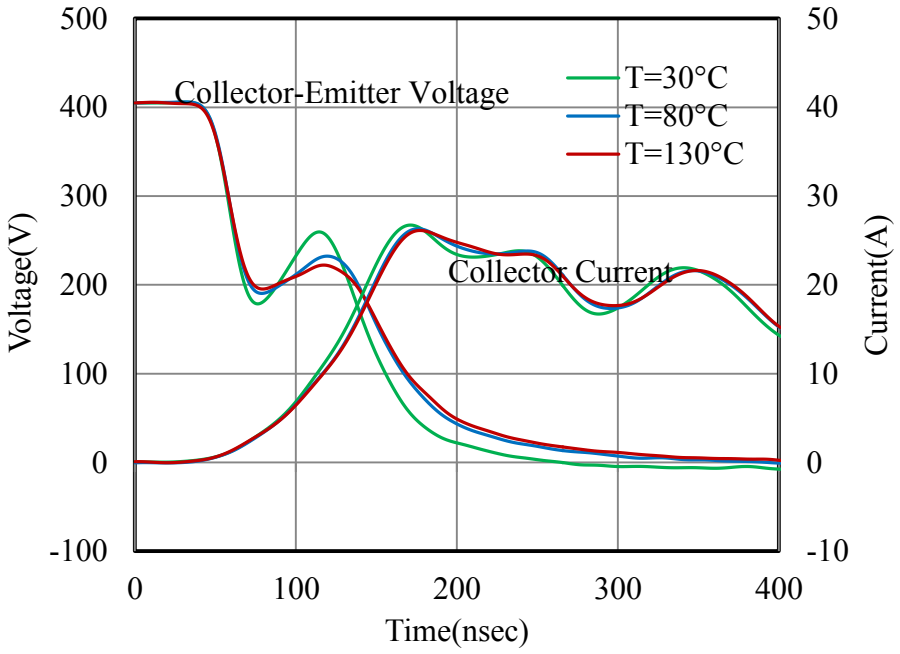



Figure 5.6: Experimentally measured hard turn-on switching waveforms of Si IGBT in a bidirectional switch of the matrix converter

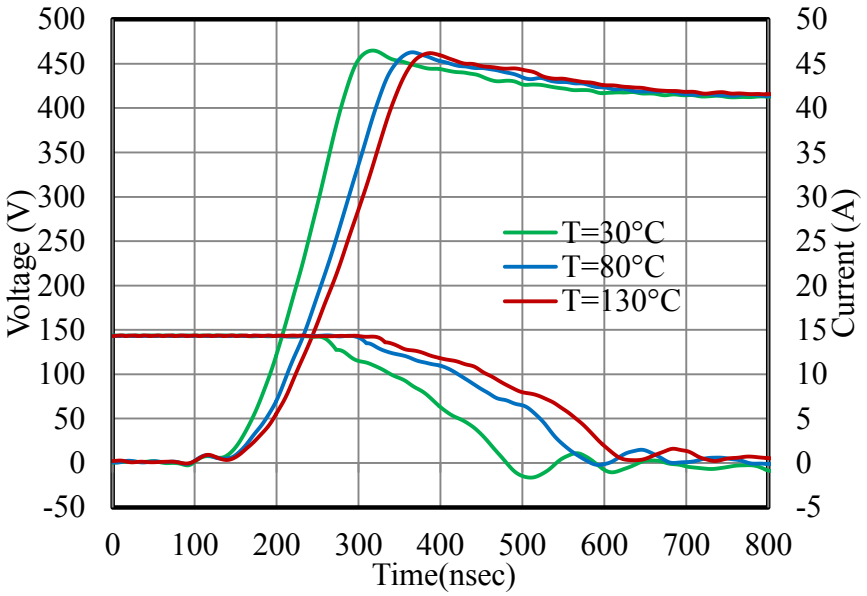



Figure 5.7: Experimentally measured hard turn-off switching waveforms of Si IGBT in bidirectional switch

The turn-on and turn-off switching energy losses of Si IGBT have been calculated based on the methodology introduced in Appendix C, for different measured switching waveforms. Figure 5.8 shows the calculated turn-on and turn-off switching energy losses of the Si IGBT when it is employed in the matrix converter as function of current for different voltages and temperatures. It can be seen that the Si IGBT turn-on switching energy losses varies about 200% in the considered temperature range of 30°C and 130° when the load current is 6 A for different voltages but as the load increases and reach to 14A the turn-on switching energy losses varies by about 25% for the same temperature and voltage domains. The variation with temperature in the Si IGBT turn-off switching energy losses is slightly more than turn-on switching energy losses in the considered temperature range of 30°C and 130°C.

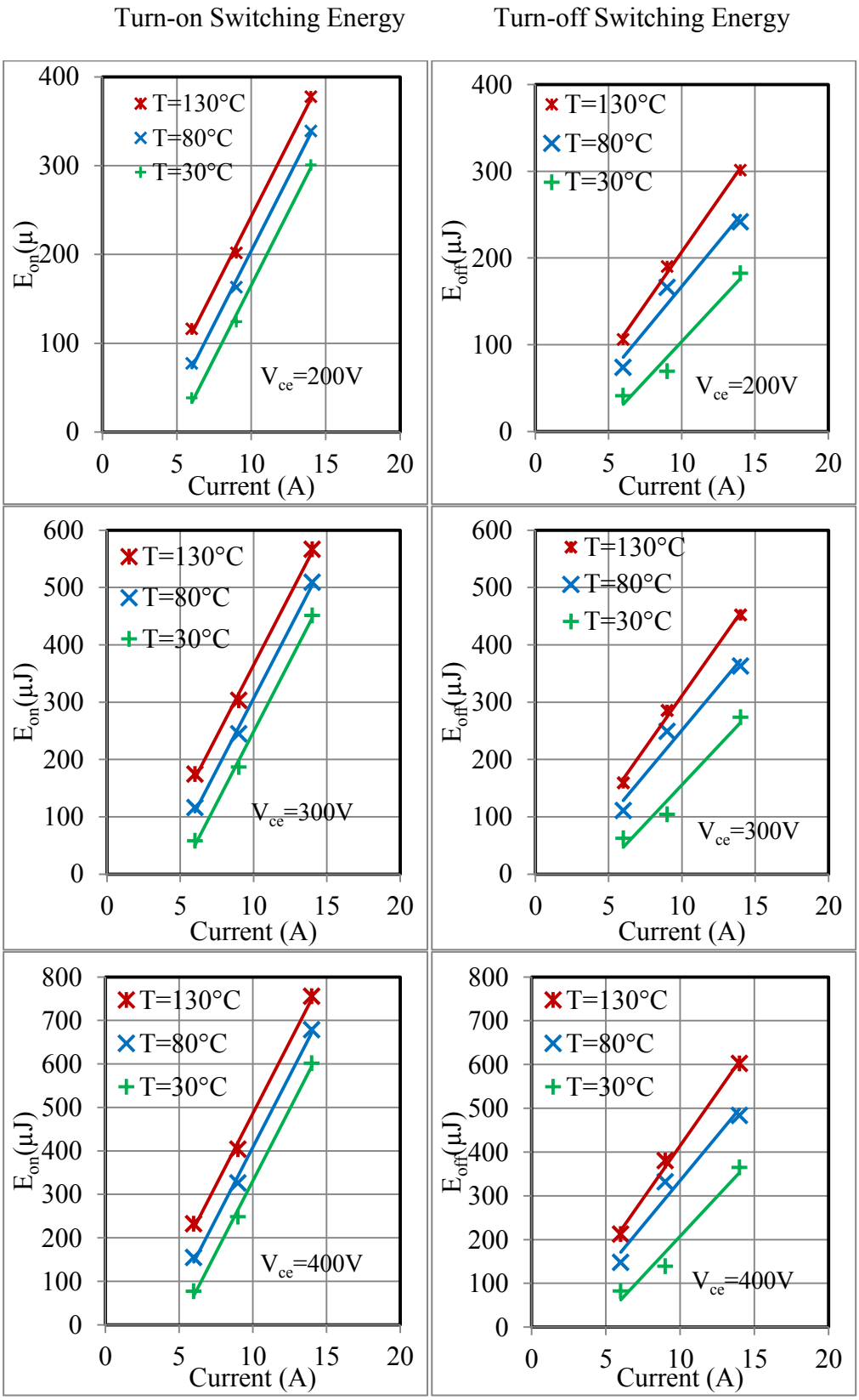



Figure 5.8: Switching energy losses of Si IGBT devices in different voltages, load currents and temperatures

## 5.2 Power Losses of the SiC MOSFET

The SiC MOSFET as mentioned in Chapter 2 is one of the new wide band gap power devices that because of its higher breakdown voltage, lower on-state resistance and better high temperature operation capability is promising to replace Si devices in high voltage and high frequency applications. Therefore, in order to evaluate SiC MOSFET potential performance in converter systems, it is required to fully characterize it. In this section, a 1.2kV, 24A SiC MOSFET manufactured by Cree is investigated.

### 5.2.1 On-state Performance of the SiC MOSFET

The on-state performance of the SiC MOSFET is described by the forward and reverse output characteristics, the on-state forward and reverse resistances and the body diode forward characteristic.

The forward output characteristic of the SiC MOSEFT is measured by curve tracer in various temperatures. The forward output characteristic of the SiC MOSFET for different temperatures when the gate-source voltage is 20V is presented in Figure 5.9. It can be seen from Figure 5.9 that the slope of the forward characteristic has decreased as the temperature has increased.

Additionally, the reverse output characteristic of SiC MOSFET at various temperatures is measured and presented in Figure 5.10 when gate-source voltage is 20 and -5V. It can be noted that when a negative gate voltage is applied the PN body diode of SiC MOSFET conducts and provides a reverse conduction property for the SiC MOSFET. But the forward voltage drop of body diode is high due to a wide band gap PN junction. Also by applying a

positive gate voltage, the majority carrier current flows through the MOSFET channel, thus the MOSFET channel starts to conduct. Therefore, these results show that the SiC MOSFET have a reverse conducting characteristic and also reverse voltage drop can be decreased significantly by simply turning on the SiC MOSFET. This means that using the SiC MOSFET in its synchronous rectification mode is possible and it brings significant on-state voltage reduction.

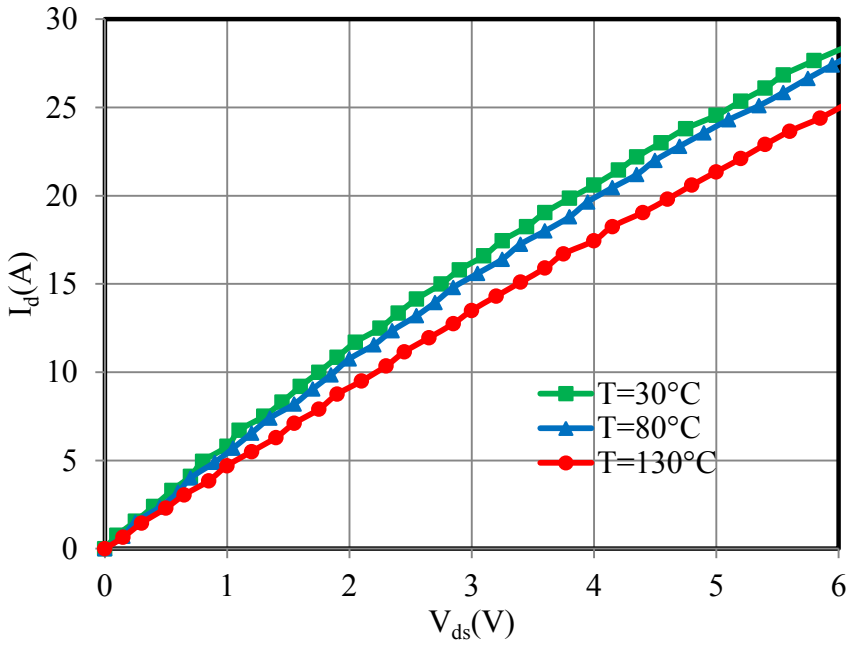



Figure 5.9: The forward output characteristic of the SiC MOSFET at 25ºC

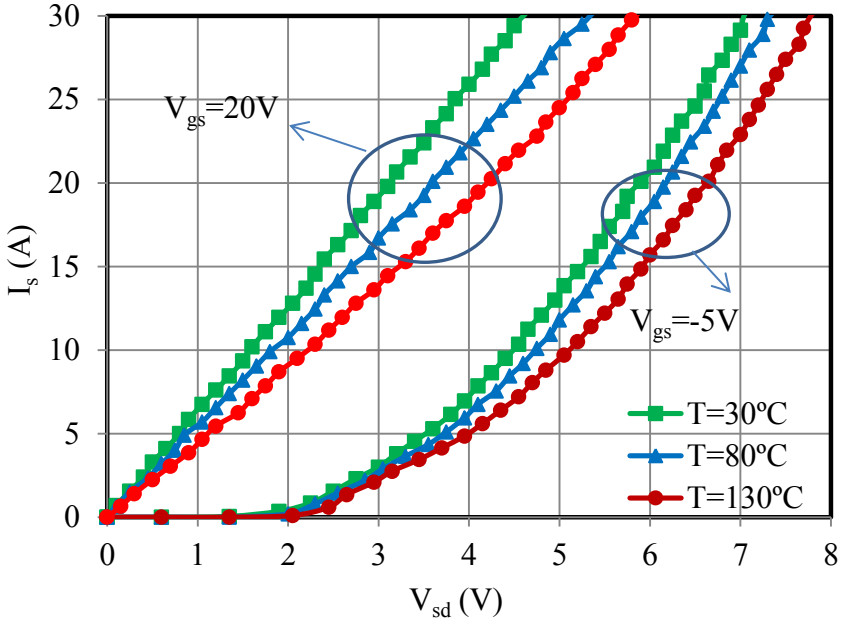



Figure 5.10: Reverse conduction characteristics of the SiC MOSFET at on and off gate-source voltage for different temperatures

The forward and reverse output characteristics of the SiC MOSFET are approximately linear, proving that in both direction the JFET channel can be treated as resistor. The equivalent on-state resistance of the SiC MOSFET in the forward and reverse conduction mode and also resistance of its body diode can be determined by calculating the slope of the forward and reverse output characteristics. Figure 5.11 shows the drain-source or forward and source-drain or reverse equivalent on-state resistances of the SiC MOSFET and resistance of its body diode at different temperatures when the gate-source voltage is 20V. It can be noted that there is no significant difference between the on-state resistances in forward and reverse directions and both of them increase slightly as the temperature increases. Also the body diode on-state resistance of SiC MOSFET is slightly more than the forward and reverse on-state resistance of the SiC MOSFET and it is increased by increasing the temperature. Thus, it should be noted that the forward, reverse and body diode

resistance of the SiC MOSFET have a positive temperature coefficient, which is benefited in paralleling operation devices.

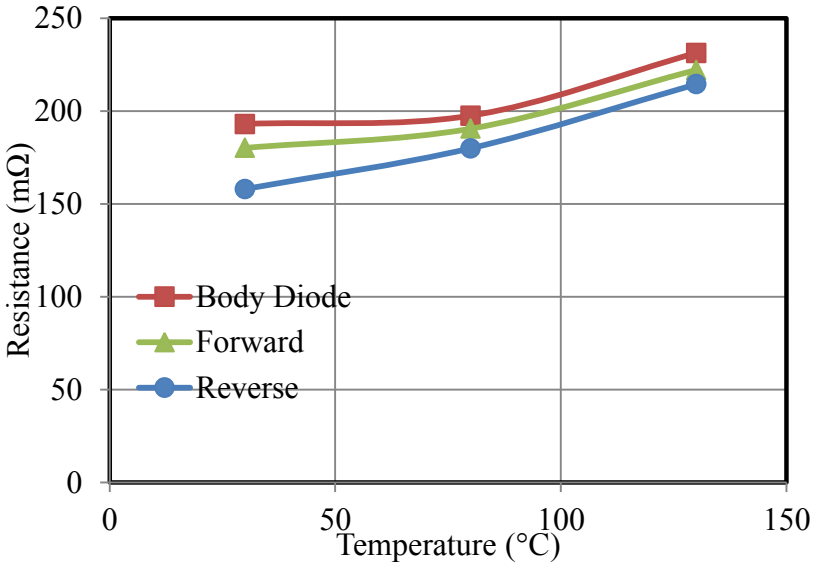



Figure 5.11: SiC MOSFET on-state resistance in forward and reverse conduction modes and the on-state resistance of its body diode

The SiC MOSFET during forward conduction mode can be modelled with a resistance which representing the SiC MOSFET forward on-state resistance ($R_{ds}$). In the reverse conduction mode of the SiC MOSFET, the current conduction path depends on the value of current, when current is smaller than a threshold value which is $\frac{V_F}{R_{sd-MOSFET}}$, only the MOSFET conducts, and when the current exceeds this threshold value, both the MOSFET and its body diode will conduct current. So the equivalent model of the SiC MOSFET in reverse conduction mode is a parallel circuit consists of the SiC MOSFET reverse on-state resistance and a model of the body diode which is a voltage source representing the forward voltage of diode and the diode on-state resistance. Therefore the SiC MOSFET can be linearized into the form:

$$V_{ds}(t) = R_{ds-MOSFET}(T) I_d \qquad (5.4)$$

$$V_{sd}(I,T) = \begin{cases} R_{sd-MOSFET}(T)I_s(t), & I_s \leq \frac{V_F}{R_{sd-MOSFET}} \\ \frac{R_{sd-MOSFET}(T)R_{diode}(T)I_s(t)+R_{diode}(T)V_F(T)}{R_{sd-MOSFET}(T)+R_{diode}(T)}, & I_s > \frac{V_F}{R_{sd-MOSFET}} \end{cases} \quad (5.5)$$

where $R_{ds\text{-}MOSFET}$ and $R_{sd\text{-}MOSFET}$ are the forward and reverse on-state resistances of the SiC MOSFET respectively. Also $V_F$ is the forward voltage drop across the SiC MOSFET body diode and $R_{diode}$ is the on-state resistance of the body diode. Figure 5.12 shows the electrical schematic of the SiC MOSFET model during forward and reverse conduction mode.

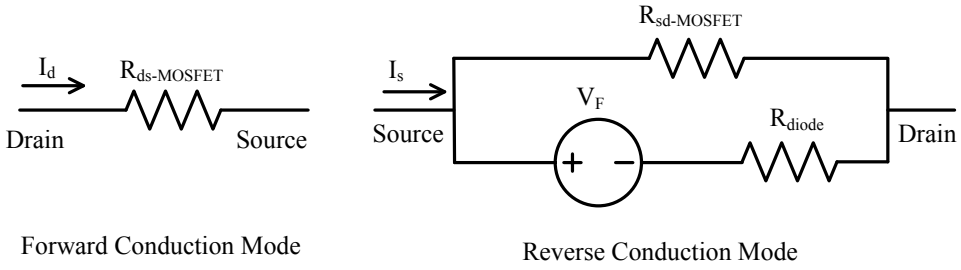



Figure 5.12: Electrical schematic of the SiC MOSFET model during forward and reverse conduction mode

### 5.2.2 Dynamic Performance of the SiC MOSFET

The dynamic characterization of SiC MOSFET is based on its application in matrix converter. Therefore, dynamic characterization of SiC MOSFET in this work is described based on the hard turn-on and hard turn-off switching in the matrix converter and then calculating the associated switching energies.

The voltage and current hard turn-on and turn-off switching waveforms of the SiC MOSFET used in matrix converter have been measured at 30°C, 80°C

and 130°C when the input voltage is 200V, 300V and 400V and the load current is 6A, 9A and 14A. The measured drain-source voltage and drain current hard turn-on and turn-off waveforms of SiC MOSFET when the input voltage is 400V and the load current is 14A are shown in Figure 5.13 and Figure 5.14 respectively. The average switching speed over the consider temperature range at 400V is in the range of 40ns to 50ns. It can be noted that by rising temperature of SiC MOSFET, there is no significant increasing in the turn-on and turn-off time of devices. This is one of the advantages of SiC MOSFET for high temperature applications due to performance of power device will not decrease noticeably. It should also be noted that due to the parasitc inductance of the circuit and high $di_d/dt$, there is a voltage drop and a voltage overshoot across the drain-source of the SiC MOSFET during turn-on and off switching respectively.

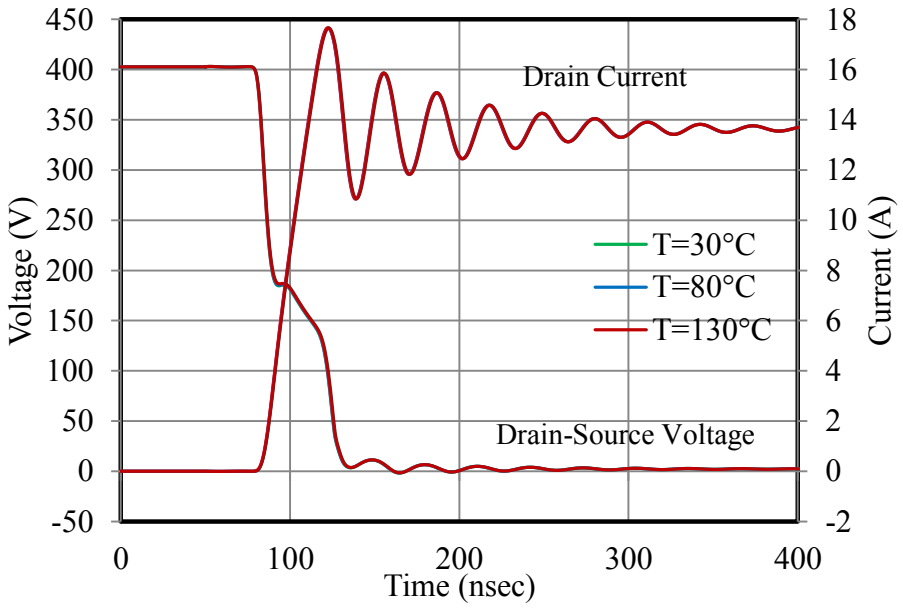



Figure 5.13: Experimentally measured hard turn-on switching waveforms of SiC MOSFET in bidirectional switch

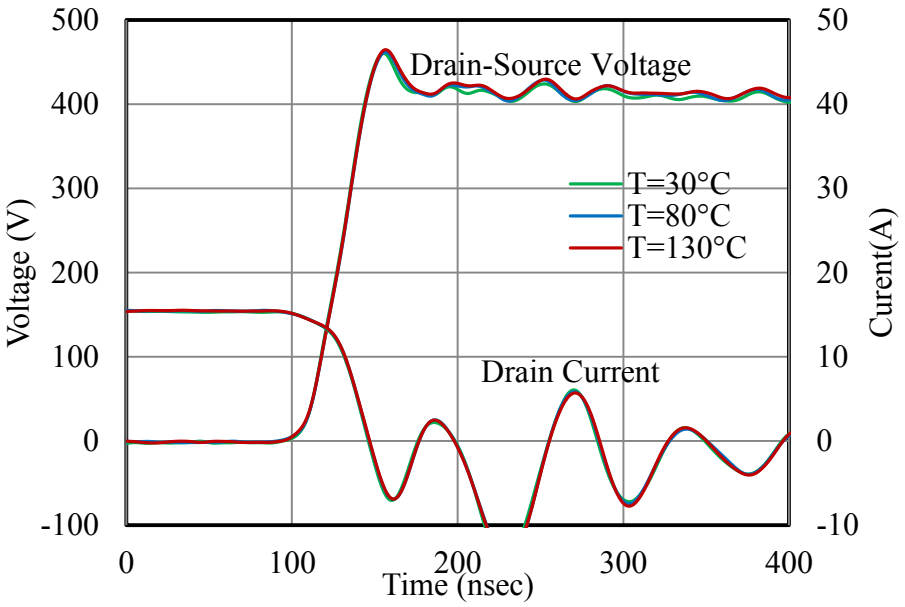



Figure 5.14: Experimentally measured hard turn-off switching waveforms of SiC MOSFET in bidirectional switch

The turn-on and turn-off switching energy losses of SiC MOSFET have been calculated based on the equation (C.1) for the different measured switching waveforms. Figure 5.15 shows the calculated turn-on and turn-off switching energy losses of the SiC MOSFET when it is used in the matrix converter as the function of the current for different voltages and temperatures. It can be noted that the SiC MOSFET turn-on and off switching loss energies varies less than 1% in the considered temperature range of 30°C and 130°C. By comparing the turn-on and turn-off switching loss energies at different voltages and currents, it reveals that the increase rate of them is linear with load current and blocking voltage, but the increase rate of the turn-off switching energy is twice of the turn-on switching energy.

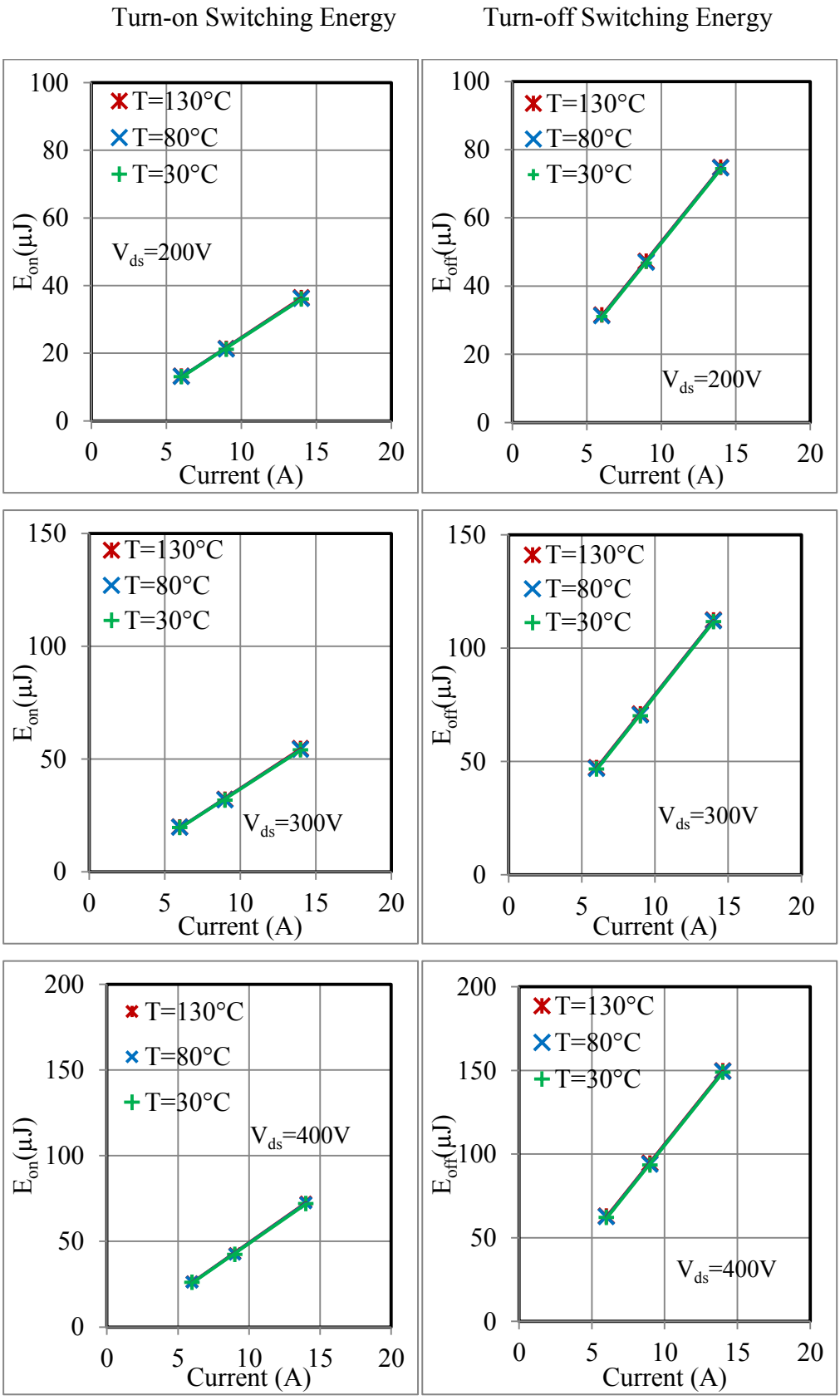



Figure 5.15: Switching energy losses of SiC MOSFET devices in different voltages, load currents and temperatures

## 5.3 Power Losses of the SiC JFET

The SiC JFET as the simplest electronic switching device that is based on the field effect to change its conduction state is another power semiconductor devices which is evaluated for power conduction and switching losses in this Chapter. As it has been mentioned the chosen SiC JFET is SJEP120R063 manufactured by SemiSouth Company. Due to inherent reliability problem of normally-on device, the selected SiC JFET is a normally-off power switch with 1200V blocking voltage and 30A current rating.

### 5.3.1 On-state Performance of the SiC JFET

As it has been stated in Chapter 2, the SiC JFET has reverse conduction capability, so the on-state performance of the SiC JFET is described by the forward and reverse output characteristics and forward and reverse on-state resistances. There is no body diode with this SiC JFET which is used in this study.

The forward output characteristic of the SiC JFET for different temperatures when the gate-source voltage of it is 2.5V has been measured by curve tracer and shown in Figure 5.16. Also the reverse output characteristic of the SiC JFET for different temperatures when the gate-source voltage is 2.5V has been measured and illustrated in Figure 5.17. It can be stated that the slope of curve in forward and reverse output characteristic of SiC JFET is decreased by increasing temperature.

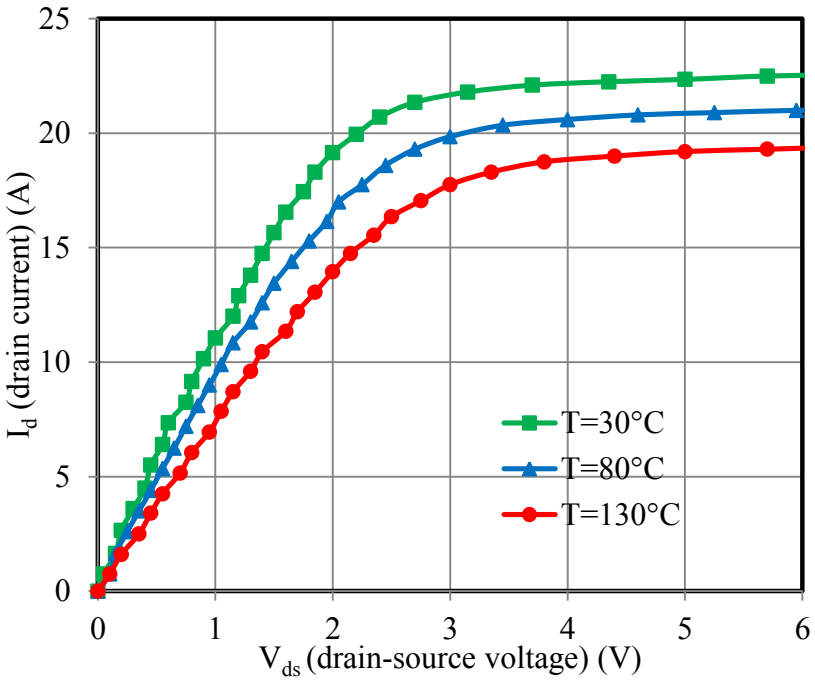



Figure 5.16: Forward output characteristics of SiC JFET for different temperatures when gate-source voltage is 2.5V

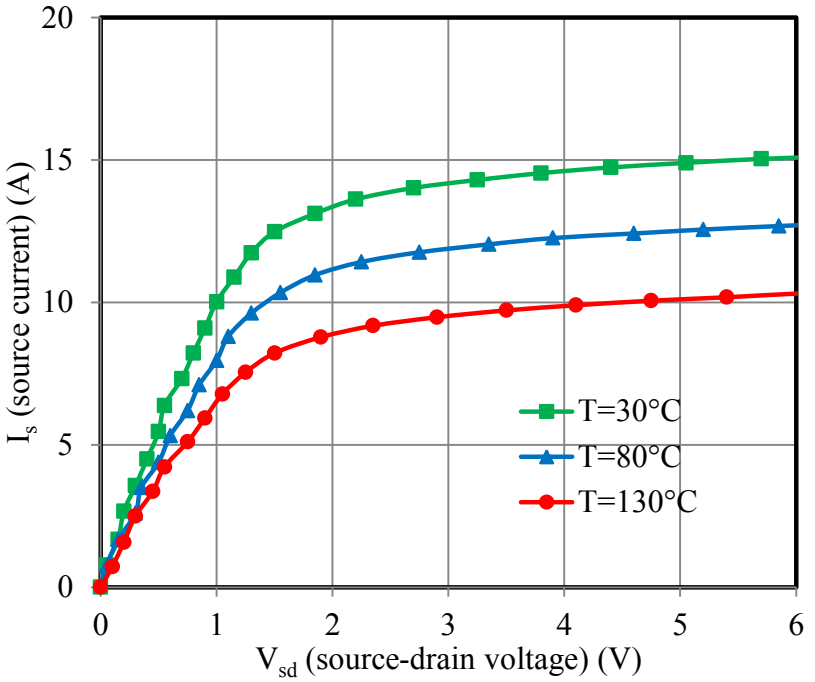



Figure 5.17: Reverse conduction characteristics of SiC JFET for different temperatures when the gate-source voltage is 2.5V

Furthermore, from Figure 5.16 and Figure 5.17, the device forward and reverse conduction on-state resistances can be extracted to be 94.91 mΩ and 98.90 mΩ at temperature of 30°C when $V_{gs}$ is biased at 2.5V. Also the device current saturates at 20.70A when $V_{gs}$ is biased at 2.5V in forward conduction at temperature of 30°C, whereas the reverse conduction current saturates at 13.12A. Additionally, Figure 5.18 shows the forward and reverse on-state resistances of the SiC JFET at different temperatures when the gate-source voltage is 2.5V. It can be noted that the on-state resistances in both directions increases as the temperature increases. Also the SiC JFET has very close forward and reverse on-state resistance. This means that using the SiC JFET in its synchronous rectification mode is possible and it brings significant on-state voltage reduction similar to the SiC MOSFET.

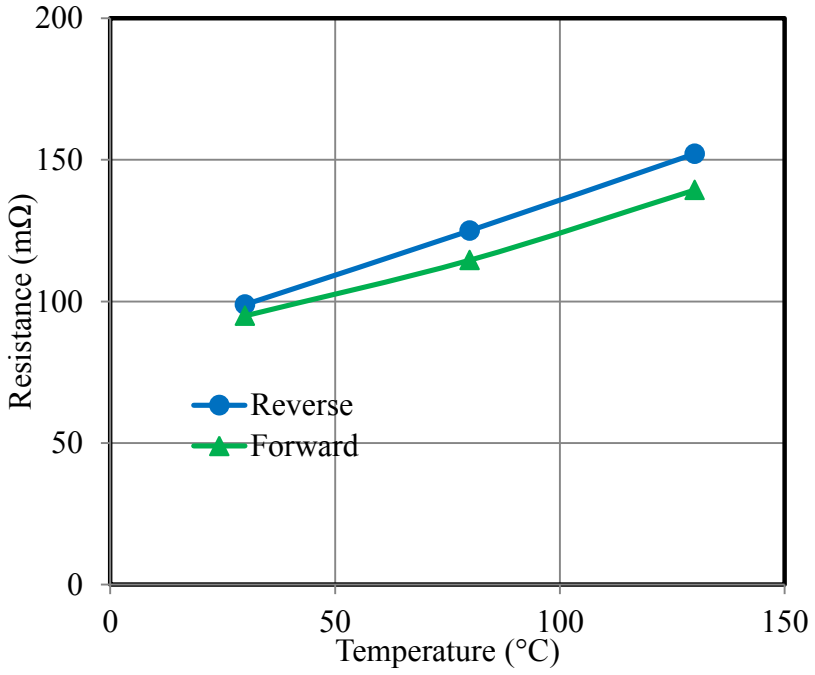



Figure 5.18: Forward and reverse on-state resistance of the SiC JFET at different temperatures

For normally-off SiC JFET, when current flows through drain-source direction, only forward on-state resistance, $R_{ds}$, conducts the current, so the normally-off SiC JFET can be modelled as a resistor. Also when current flows through source-drain direction, only the reverse on-state resistance, $R_{sd}$ conducts the current, thus the normally-off SiC JFET can be modelled as a resistor during reverse conduction. Therefore, the normally-off SiC JFET in forward and reverse conduction modes can be linearized into the form:

$$V_{ds}(I,T) = R_{ds-JFET}(T) \times I_d \qquad I_d \leq 15A \qquad (5.6)$$

$$V_{sd}(I,T) = R_{sd-JFET}(T) \times I_s \qquad I_s \leq 7A \qquad (5.7)$$

The electrical equivalent model of the normally-off SiC JFET in the forward and reverse conduction modes is presented in Figure 5.19.


Forward Conduction Mode  Reverse Conduction Mode

Figure 5.19: Electrical equivalent model of the normally-off SiC JFET in the forward and reverse conduction modes

### 5.3.2 Dynamic Characterization of the SiC JFET

The switching behaviours of the normally-off SiC are evaluated by the implemented 2-phase to 1-phase matrix converter where the used diode in the bidirectional switch is a SiC diode at different voltages, currents and temperatures. Figure 5.20 and Figure 5.21 show the measured drain-source voltage and drain current hard turn-on and turn-off switching waveforms of the

normally-off SiC JFET when the input voltage is 400V and the load current is 14A and temperature varies from 30°C to 130°C respectively. The turn-on overshoot current of the normally-off SiC JFET is not significant in compare with the SiC MOSFET. Also from the comparison of the switching waveforms at 30°C, 80°C and 130°C, it is observed that there is no significant increasing in the turn-on and turn-off time by rising temperature of SiC JFET. The averages over temperature of turn-on and turn-off switching speed achieved at 400V are about of 91ns and 60ns respectively. It should be noted that due to parasitic inductance of the circuit, there is a voltage drop and overshot across the SiC JFET during turn-on and off transient respectively.

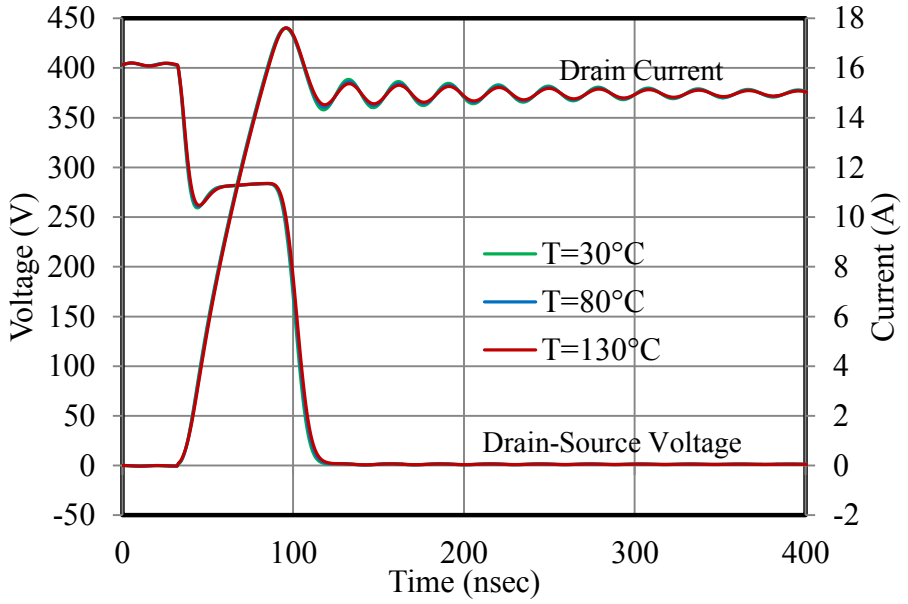



Figure 5.20: Measured hard turn-on switching waveforms of SiC JFET in bidirectional switch

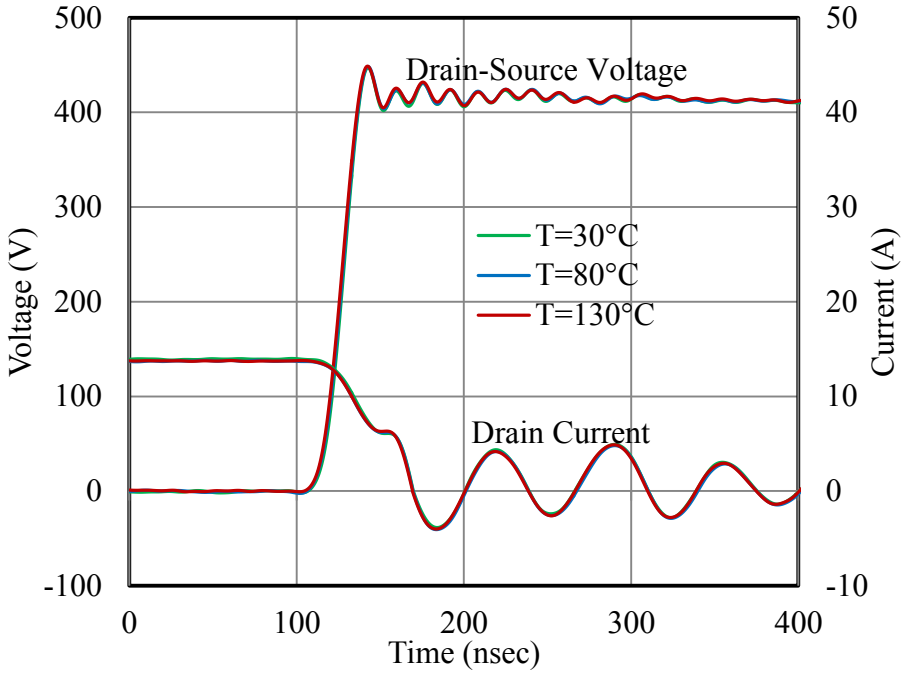



Figure 5.21: Measured hard turn-off switching waveforms of SiC JFET in bidirectional switch

The turn-on and turn-off switching energy losses of the normally-off SiC JFET have been calculated based on the equation (C.1) for different measured switching waveforms. The calculated turn-on and turn-off switching energy losses of the normally-off SiC JFET when it is employed in the matrix converter as function of current for different voltages and temperatures are illustrated in Figure 5.22. It can be noted that the normally-off SiC JFET turn-on switching energy losses varies about 10% in the considered temperature range of 30°C and 130°C. Also the variation in the SiC MOSFET turn-off switching energy losses is less than 3% in the considered temperature range of 30°C and 130°C. Also by comparing the turn-on and turn-off energy losses, it reveals that the increasing rate of the turn-on energy losses is less than the turn-off energy losses in the normally-off SiC JFET for different voltages and temperatures.

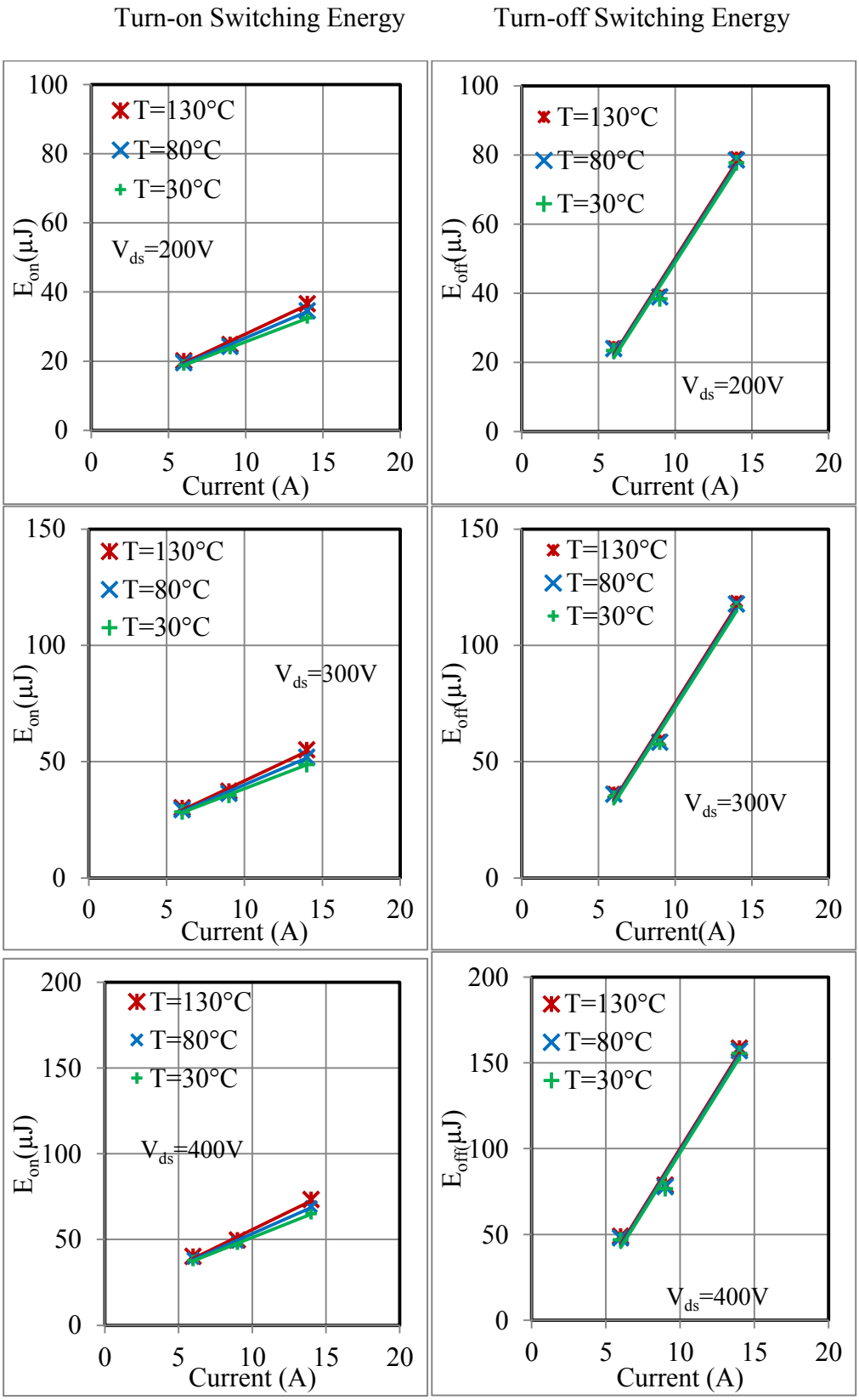



Figure 5.22: Switching energy losses of SiC JFET devices in different voltages, load currents and temperatures

## 5.4 Power Losses of the SiC BJT

The SiC BJT is another semiconductor power devices which is evaluted for power conduction and switching losses in this Chapter. As it has been mentioned the chosen SiC BJT is BT1215AC manufactured by TranSiC Company. The blocking voltage and current rating of it are 1200V and 20A respectively.

### 5.4.1 Static Characterization of the SiC BJT

The output forward charactristics of the used SiC BJT in this work has been measured by a curve tracer. The SiC BJT output charactristic at different temperatures when the base current is 250mA is shown in Figure 5.23. It is clear that the SiC BJT has a near zero collector-emitter offset voltage which is indicted that it can be modeled same as unipolar power device such as MOSFET and JFET in compare with Si IGBT. The equivalent on-state resistance, $R_{ce\text{-}BJT}$ of the SiC BJT in the forward conduction mode can be determined by calculating the slope of the forward output characteristics. Figure 5.24 shows the equivalent on-state resistance of the SiC BJT at different temperatures when the base current is 250 mA. It is clear that by increasing temperature, the on-state resistance of SiC BJT is increased which is advantage in terms of paralleling operation device.

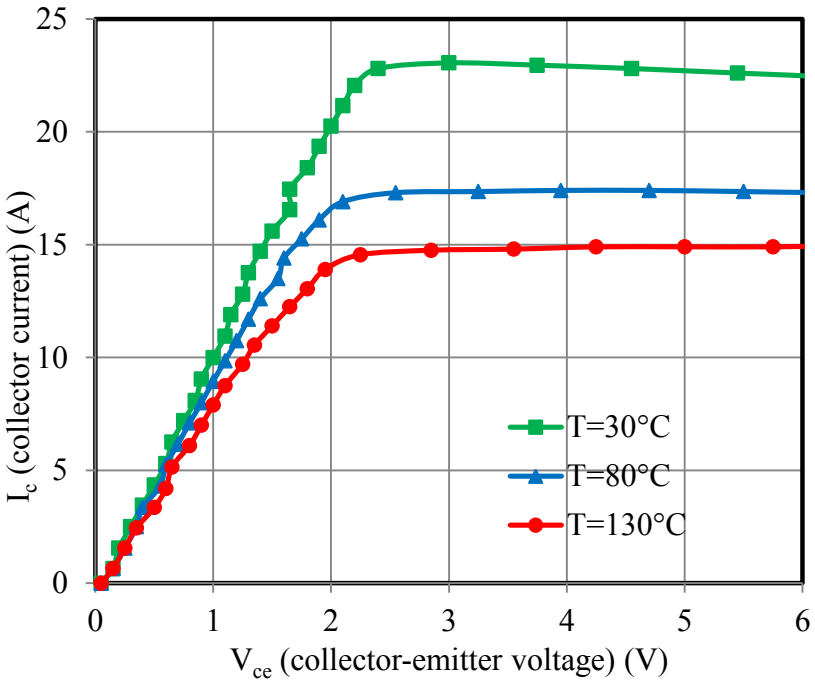



Figure 5.23: Forward output characteristics of SiC BJT at different temperatures when the base current is 250mA

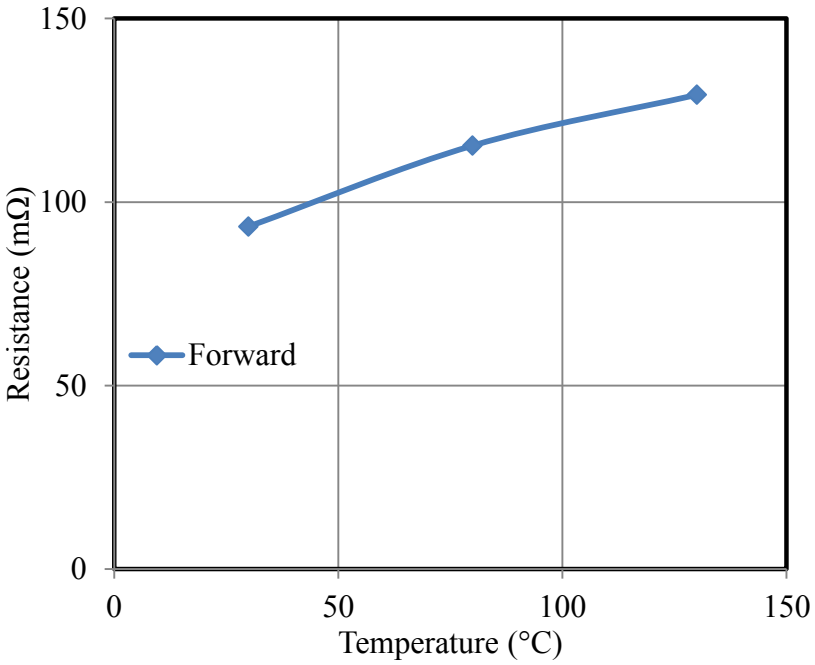



Figure 5.24: On-state resistances of the SiC BJT at different temperatures

The SiC BJT can be modelled with resistor which representing the SiC BJT on-state resistance during conduction mode based on its static characteristic. Thus the SiC BJT characteristic can be linearized into the form:

$$V_{ce}(I,T) = R_{ce-BJT}(T) \times I_c \qquad I_c \leq 15A \qquad (5.8)$$

The schematic of electrical equivalent model of the SiC BJT in the forward conduction mode is presented in Figure 5.25.

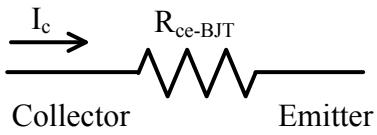



Figure 5.25: Schematic of electrical model of the SiC BJT during conduction mode

### 5.4.2 Dynamic Characterization of the SiC BJT

The dynamic characterization of SiC BJT is evaluated by the developed 2-phase to 1-phase SiC BJT matrix converter where the used diode in the bidirectional switch is a SiC diode. The dynamic characterization of SiC BJT is described based on the hard turn-on and turn-off switchings of power semiconductor device in the matrix converter and then calculating the associated switching energy losses.

The voltage and current hard turn-on and turn-off switching waveforms of the SiC BJT have been measured at 30°C, 80°C and 130°C when the input voltage is 200V, 300V and 400V and the load current is 6A, 9A and 14A. The measured collector-emitter voltage and collector current hard turn-on and turn-

off waveforms of SiC BJT in a bidirectional switch of the matrix converter when the input voltage is 400V and the load current is 14A for different temperatures are shown in Figure 5.26 and Figure 5.27 respectively. It can be noted that the current rise time and fall time during turn-on and turn-off transient are 35 ns and 71 ns respectively whereas the turn-on time is 185 ns and turn-off time is 83 ns. There is no significant increase in the gradients of current and voltage waveforms by increasing the temperature of power semiconductor device during switching. Due to the circuit parasitic inductance and high $di_c/dt$, there is a voltage drop during turn-on and an overshoot during turn-off across the SiC BJT. Also as a SiC diode is used in implementing the bidirectional switch, there is no significant current overshoot through the collector of the SiC BJT during turn-on switching transient.

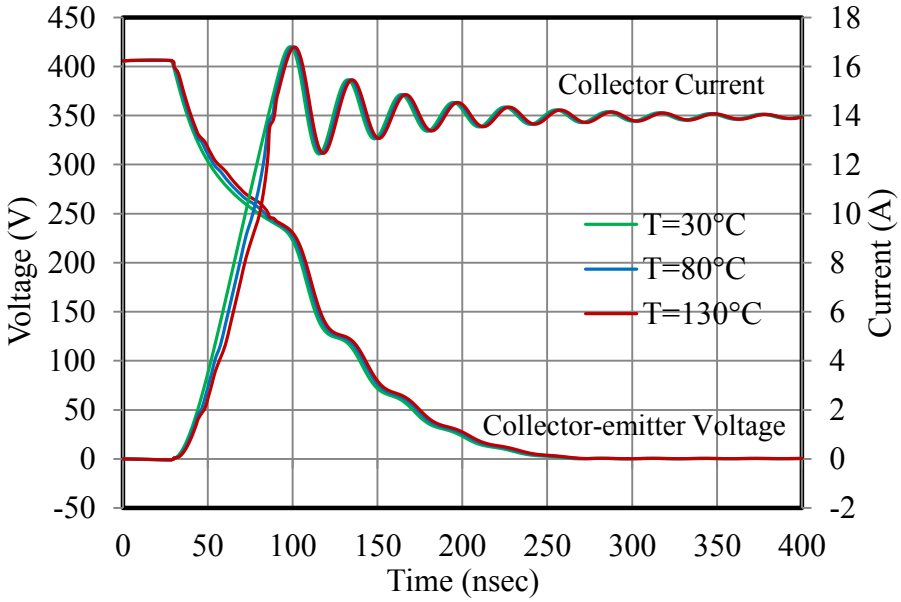



Figure 5.26: Measured hard turn-on switching waveforms of SiC BJT in bidirectional switch

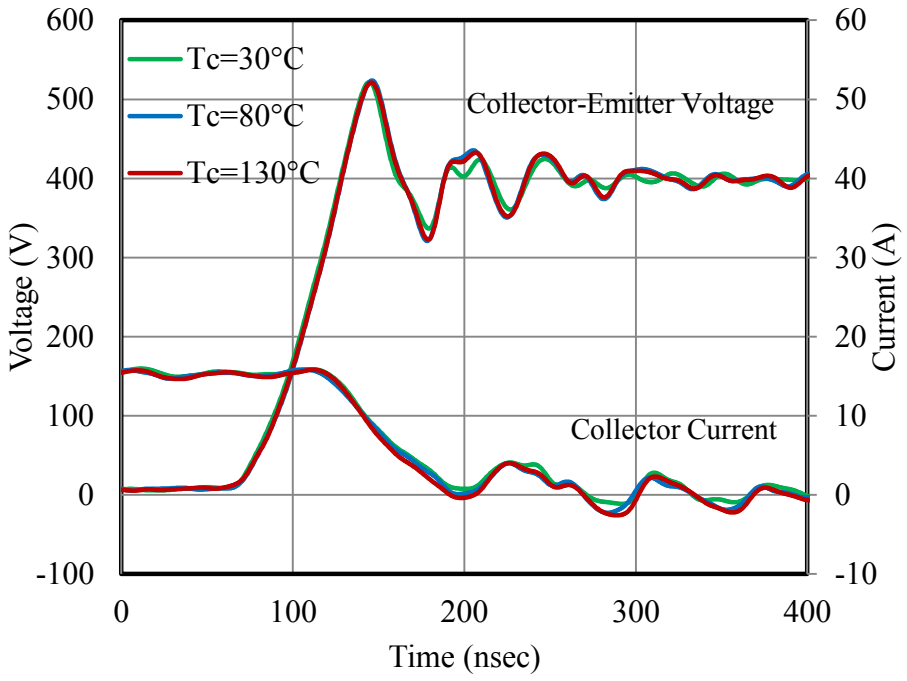



Figure 5.27: Measured hard turn-off switching waveforms of SiC BJT in bidirectional switch

Based on the measured switching waveforms, the SiC BJT switching energy losses can be calculated using equation (C.1). Figure 5.28 presents the calculated turn-on and turn-off switching energy losses of the SiC BJT when it is employed in the matrix converter as function of current for different voltages and temperatures. The test results show that the turn-on switching loss of the SiC BJT is more than the turn-off switching energy at the same voltage and current. It should be noted that there is no significant increasing in switching energy losses of the SiC BJT by increasing temperature in the considered range. Also the increase rates of both switching energies are linear with the voltage and current.

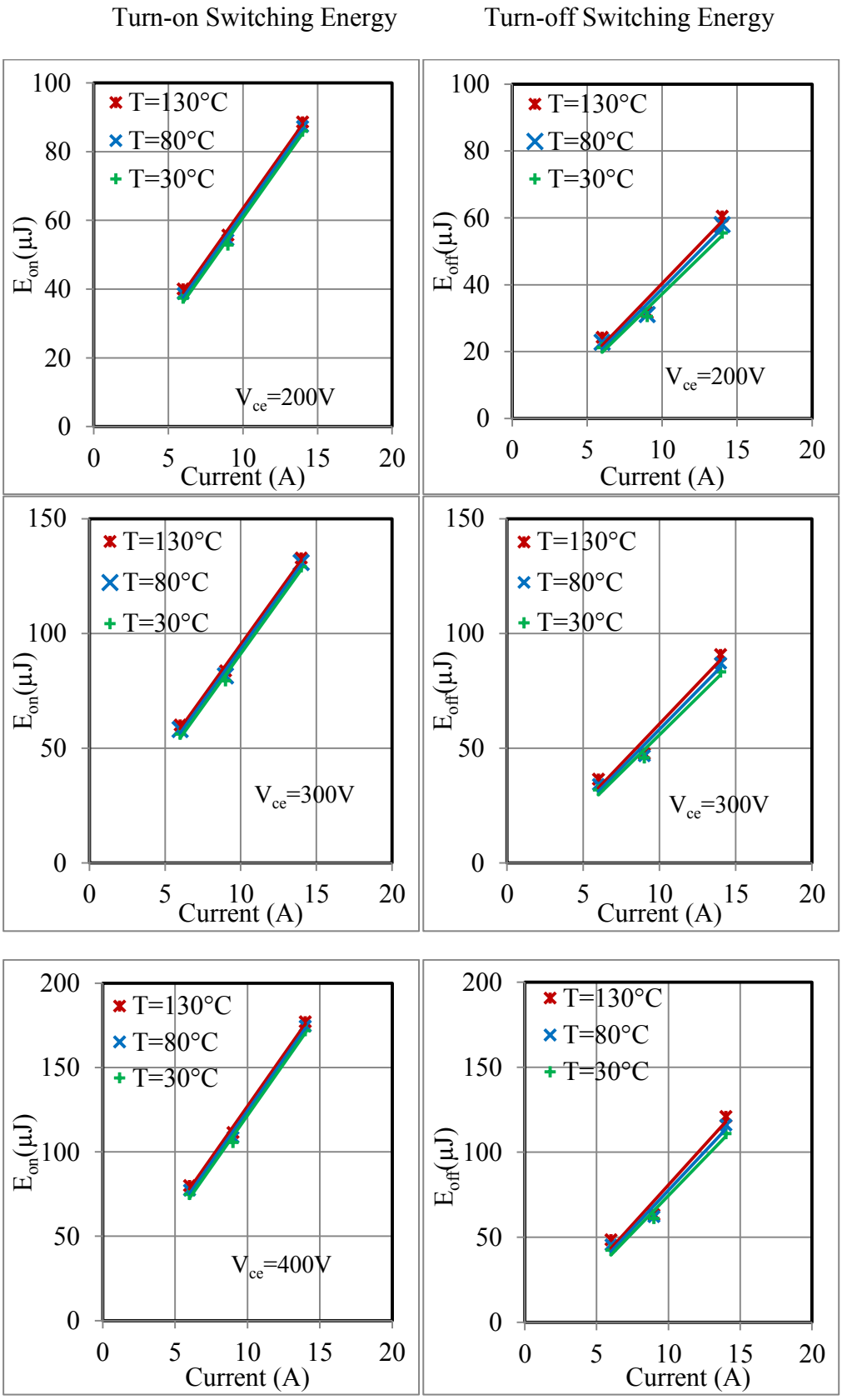



Figure 5.28: Switching energy losses of SiC BJT devices in different voltages, load currents and temperatures

## 5.5 Performance Comparison of the Selected Power Devices

Experimentally determined static and dynamic characteristics of the four different power semiconductor devices at the same operating conditions enable an analytical assessment of the device performance for different power semiconductor technologies. One of the most important quantities for assessing static characteristics of the power devices is the on-state resistance. Figure 5.29 shows the on-state resistance of the different power devices at different temperatures. It can be seen from Figure 5.29 that the on-state resistance of the SiC MOSFET is the highest, while the on-state resistance of the SiC BJT is the lowest. It is also observed that the on-state resistance of the SiC BJT is the least temperature-dependent, which indicates constant conduction losses with varying temperature. It should be noted that the on-state resistance of the Si IGBT is very close to the on-state resistance of the SiC JFET and BJT.

It should be noted that the on-state voltage of the device has also effect on the on-state power loss of the power devices. But the Si IGBT is the only power device which has this characteristic and the other SiC power devices which is considered in this study did not present this feature.

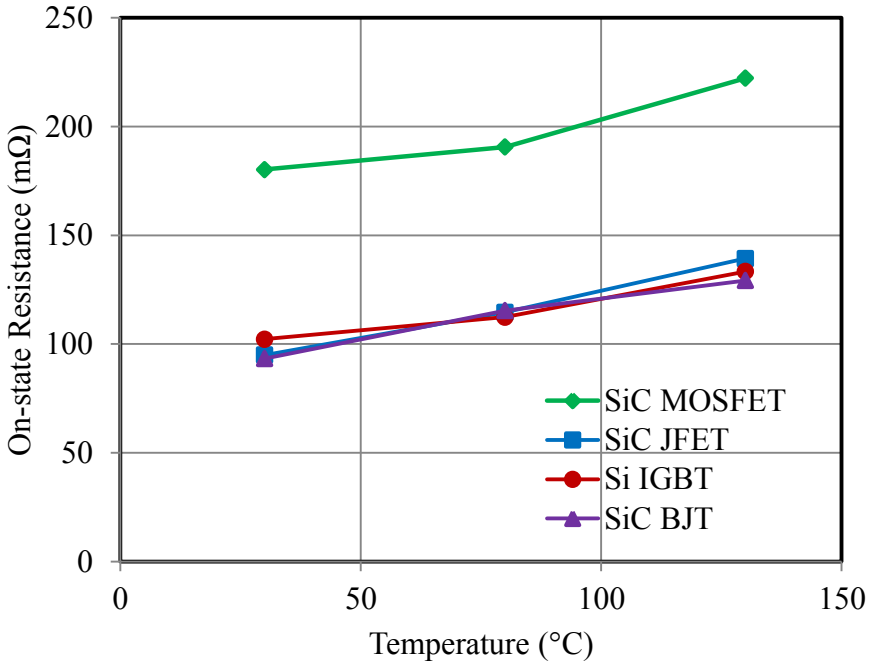



Figure 5.29: On-state resistance versus temperature for the different power devices

The total switching energy has been considered for comparison of the dynamic characteristics of the four different power devices. Figure 5.30 shows the total switching loss energy of the four different power devices versus load current when the voltage and temperature of device are 400V and 130°C . It can be seen from Figure 5.30 that the SiC power devices have very low total switching energy in comparison with the Si IGBT. It should also be noted that the MOSFET and SiC JFET feature the lowest total switching loss energy and that the total switching energy of SiC BJT is slightly more than the two other SiC devices.

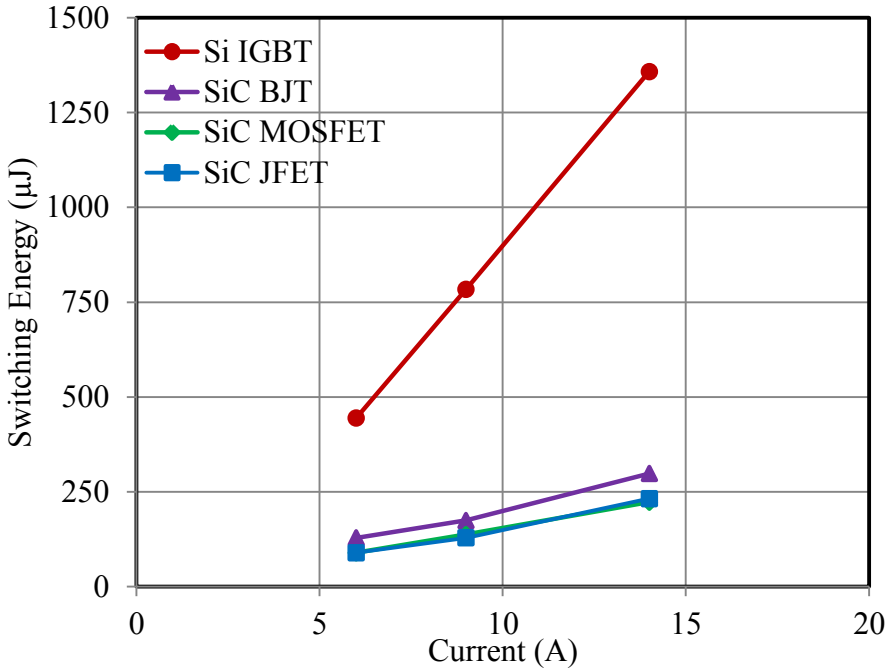



Figure 5.30: Total switching energy versus current for different power devices at 400V and 130°C

## 5.6 Power Losses Evaluation of Matrix Converter

This section presents an analytical method for evaluating power losses of the three-phase matrix converter with Si and SiC power devices and then comparison of them. Power device losses of the matrix converter consist of drive, conduction, and switching losses of diodes and power switching devices such as Si IGBT and SiC JFET, MOSFET or BJT. The approach used to estimate these device loss components is explained in this section. The analysis is based on the assumption that the input voltages and output currents of the matrix converter are sinusoidal and balanced and contain negligible switching ripple. The commutation scheme and modulation method considered in this section are the four-step current commutation and the double side space vector modulation which have been presented in Chapter 3 respectively. In the

calculation of power losses, the measured on-state resistance, on-state voltage and switching energies of power devices in the previous section have been used while for the calculation of driving power losses some parameters have been extracted from the power device datasheets.

### 5.6.1 Drive Losses

Power consumption in the drive circuit is required in determining the power losses of the whole converter. The drive losses in various power devices are different and depend on the characteristics of the power semiconductor device and drive circuit.

The drive loss of the SiC MOSFET and Si IGBT only consists of the charging of the gate capacitance during each turn-on transient. Therefore, it can be stated as:

$$P_{drive-MOSFET\ or\ IGBT} = V_{gs\ or\ ge} Q_g f_{sw} \tag{5.9}$$

where $V_{gs}$ and $V_{ge}$ are the forward voltage bias of MOSFET and IGBT respectively, $Q_g$ is the gate charge of MOSFET or IGBT at the forward bias voltage, and $f_{sw}$ is the switching frequency.

For the normally-off SiC JFET, three contributions of the power consumption must be considered in the calculation of drive losses based on the developed gate drive circuit in the Chapter 4. The first one is associated with charging of the gate capacitance during each turn-on transient. The second one is due to the on-state resistance of the gate drive and the last one is associated

with charging of the speed-up capacitor in the gate drive. Therefore, the total drive loss for the normally-off SiC JFET can be presented as:

$$P_{drive-JFET} = V_{gs}Q_g f_{sw} + I_{grms}^2 R_g + C_s f_{sw}(V_{cc} - V_{gs})^2 \quad (5.10)$$

where $V_{gs}$ is the forward voltage bias, $Q_g$ is the gate charge of the JFET at the forward bias voltage, $f_{sw}$ is the switching frequency, $I_{grms}$ is the rms value of the gate current, $R_g$ is the gate resistor, $C_s$ is the speed-up capacitor, and $V_{cc}$ is the supply voltage in turn-on time.

For determining the base drive losses of SiC BJT, one more contribution of power consumption in comparison with the normally-off SiC JFET, which is due to the voltage drop across the base emitter of BJT in on-state duration, should be considered. Therefore, the total base drive losses for the SiC BJT based on the used base drive circuit in this work can be expressed as:

$$P_{drive-BJT} = I_{bav}V_{be(sat)} + V_{be(sat)}Q_b f_{sw} + I_{brms}^2 R_b + C_s f_{sw}(V_{cc} - V_{be(sat)})^2 \quad (5.11)$$

where $I_{bav}$ is the average base current, $V_{be(sat)}$ is the voltage drop across base-emitter of the BJT, $Q_b$ is the base charge of the BJT at the base saturation voltage, $f_{sw}$ is the switching frequency, $I_{brms}$ is the rms value of the base current, $R_b$ is the base resistor, $C_s$ is the speed-up capacitor, and $V_{cc}$ is the supply voltage in turn-on time.

Therefore, by considering a typical double-sided space vector modulation with twelve switching per period for the matrix converter and four-step current

commutation scheme, the total driving loss of the three-phase matrix converter can be calculated by:

$$P_{drive} = 12P_{drive-JFET\ or\ MOSFET\ or\ BJT\ or\ IGBT} \quad (5.12)$$

### 5.6.2 Conduction Losses of Bidirectional Switch

Conduction losses of switching devices in the matrix converter have been covered in [8, 104]. It depends on the static characteristics of semiconductor power device, the commutation strategy and the output current of matrix converter. The output current flows through one bidirectional switch of matrix converter at any instant; thus, based on the balanced three-phase output currents, the static characteristics of power device and considering the four-step current commutation scheme, some equations can been derived to determine conduction losses.

Based on the developed electrical model for Si IGBT and diode, the conduction losses of the three-phase matrix converter when the bidirectional switch consists of Si IGBT and diode, by assuming a sinusoidal output current of rms magnitude $I_o$, is given by [15]:

$$P_{con} = \frac{6\sqrt{2}}{\pi} V_{ce-on} I_o + 3r_{ce-IGBT} I_o^2 + \frac{6\sqrt{2}}{\pi} V_F I_o + 3r_{diode} I_o^2 \quad (5.13)$$

Furthermore, the conduction losses of the three-phase matrix converter with SiC MOSFET bidirectional switch based on the developed electrical models of the SiC MOSFET and its body diode and by considering four-step current commutation strategy is given by:

$$P_{con} = \begin{cases} 3(R_{ds-MOSFET} + R_{sd-MOSFET})I_o^2, & if \quad I_o \le \dfrac{V_F}{R_{sd-MOSFET}} \\ 3R_{ds-MOSFET}I_o^2 + \dfrac{3R_{sd-MOSFET}R_{diode}I_o^2 + \dfrac{6\sqrt{2}}{\pi}R_{diode}V_F I_o^2}{R_{sd-MOSFET} + R_{diode}}, & if \quad I_o > \dfrac{V_F}{R_{sd-MOSFET}} \end{cases} \tag{5.14}$$

It should be noted that due to reverse conduction feature of SiC MOSFET, during conduction mode both forward and reverse SiC MOSFET in bidirectional switch are conducting, so both of them have been considered in calculating conduction losses. But when the output current is more than $\frac{V_F}{R_{sd-MOSFET}}$, the body diode of reverse SiC MOSFET in the bidirectional switch conducts and current will share between reverse SiC MOSFET and its body diode.

For the normally-off SiC JFET as it is unipolar power device and can conduct in forward and reverse paths and also with four-step current commutation scheme both power devices are turned on during conduction, therefore the average conduction losses for three-phase matrix converter by assuming a sinusoidal output current of rms magnitude $I_o$, is given by:

$$P_{con} = \begin{cases} 3\left(R_{ds-JFET} + R_{sd-JFET}\right)I_o^2 & I_o \le \dfrac{V_F}{R_{sd-JFET}} \\ 3R_{ds-JFET}I_o^2 + \dfrac{3R_{sd-JFET}R_{diode}I_o^2 + \dfrac{6\sqrt{2}}{\pi}R_{diode}V_F I_o^2}{R_{sd-JFET} + R_{diode}} & I_o > \dfrac{V_F}{R_{sd-JFET}} \end{cases} \tag{5.15}$$

It can be noted that the conduction losses depends only on the forward and reverse on-state resistance of the normally-off SiC JFET when value of the output current is less than $\frac{V_F}{R_{sd-JFET}}$ , but if the output current rises more than this value, the antiparallel diode in the bidirectional switch conducts and current will share between reverse SiC JFET and diode.

Moreover based on the developed electrical model for SiC BJT and diode, the conduction losses of the three-phase matrix converter when the bidirectional switch consists of SiC BJTs and diodes, by assuming a sinusoidal output current of rms magnitude $I_o$, is given by:

$$P_{con} = 3r_{ce-BJT}I_o^2 + \frac{6\sqrt{2}}{\pi}V_F I_o + 3r_{diode}I_o^2 \qquad (5.16)$$

It is obvious that the conduction losses of the matrix converter is depends on the power semiconductor characteristics, the commutation strategy and the rms value of the output current, therefore the operation conditions such as modulation index or switching frequency do not have any effect.

### 5.6.3 Switching Losses

The relationship between switching energy loss and blocking voltage and load current have to be established to allow for switching loss values to be determined at any blocking voltage and load current combinations occurring in a matrix converter circuit. The variation of switching loss with blocking voltage and load current were shown to be approximately linear in dynamic characterizations of different power semiconductor devices sections. Hence,

the rate of turn-on and turn-off of switching energy losses at the reference voltage and current are computed using the following equations:

$$\tau_{on} = \frac{2E_{on}}{V_R I_R} \tag{5.17}$$

$$\tau_{off} = \frac{2E_{off}}{V_R I_R} \tag{5.18}$$

where $E_{on}$ and $E_{off}$ are the turn-on and turn-off switching energy losses of the power switching device, respectively. $V_R$ is the reference voltage in the drain–source or collector–emitter of the JFET and MOSFET or BJT and IGBT, respectively. $I_R$ is the reference current in the drain or collector of the JFET and MOSFET or BJT and IGBT, respectively.

Similarly, the rate of diode reverse recovery or turn-off switching energy loss is determined using:

$$\tau_{rec} = \frac{2E_{rec}}{V_R I_R} \tag{5.19}$$

where, $E_{rec}$ is the diode recovery or turn-off energy loss. $V_R$ is the reference voltage across the diode and $I_R$ is the reference current of the diode.

The approach discussed in Chapter 3 to determine the different switching types for the commutation between two bidirectional switches can be used to calculate the average switching power losses of a three-phase matrix converter at some given operating conditions. A repeat period that contains an integral multiple of the input and output and switching periods is identified and all switching instants within this period are determined. The changes in device voltage and device current in the devices undergoing commutation are then

identified for each commutation instant. The polarity of these voltage and current values allow classification of the hard switching loss at each instant as either hard turn-on or hard turn-off energy loss. The sum of all the energy losses associated with the hard turn-on and hard turn-off events during the repeat period can then be determined and the average switching power losses computed.

The derivation of the average switching power losses is based on the following simplifying assumptions:

- The input voltages and output currents are sinusoidal and balanced, and contain negligible switching ripple;
- The device hard switching energy losses vary linearly with the voltage and current at the switching transient and can be therefore be modelled by equations (5.17)-(5.19);
- A four-step current commutation technique is used;
- Soft commutation losses can be neglected;
- The switching frequency is much higher than the converter input and output frequencies to enable good synthesis of reference signals

The switching pattern for the double side space vector modulation of output phase *a* in the first sextant follows a C-A-B-B-A-C symmetrical pulse sequence as shown in Figure 5.31. Given such a pattern and that $i_a$ does not reverse during the sequence period, if a hard turn-on energy loss occurs when output phase *a* is switched from input phase X to input phase Y, then a hard turn-off loss results when phase *a* is switched back from Y to X. This rule can also be applied to the case where current reversal occurs during the sequence

as the turn-on and turn-off energy losses will be low due to the near zero current and the resulting error will be negligible.

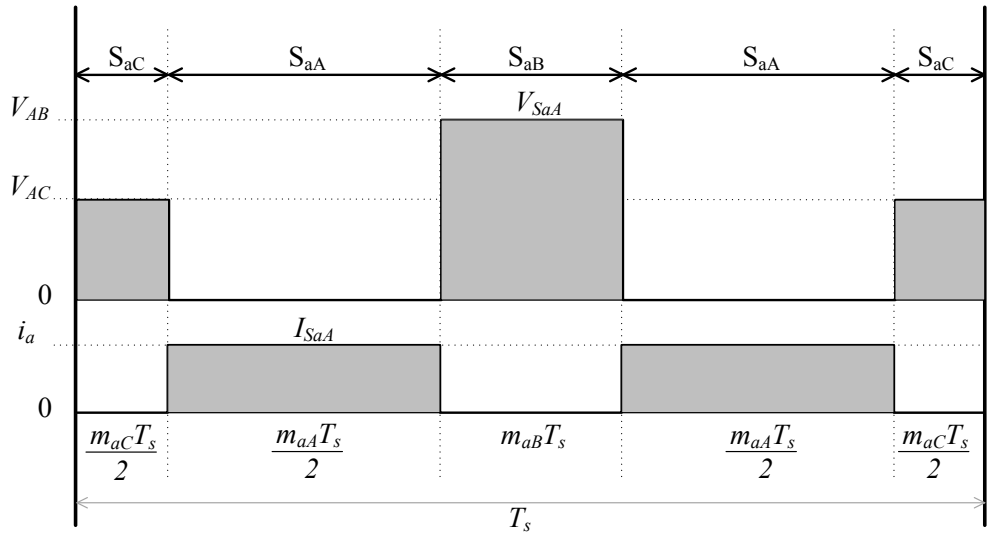



Figure 5.31: Schematic representation of switching function for switch $S_{aA}$ with double sided space vector modulation

The total converter loss for a switching sequence as in Figure 5.31 is therefore:

$$E_{sw} = (\tau_{on} + \tau_{off} + \tau_{rec})(|V_{AB}| + |V_{AC}|)(|i_a| + |i_b| + |i_c|) \quad (5.20)$$

As the instantaneous sum of the output phase currents is zero, then for $|i_a| = |i_o|_{max}$ and$|i_a| = |i_b| + |i_c|$:

$$|i_a| + |i_b| + |i_c| = 2|i_o|_{max} \quad (5.21)$$

Also for unity power factor operation, the space vector modulation switching sequence depends on the measured input voltage vector direction.

This insures that for a general sequence X-Y-Z-Z-Y-X, $|v_Y| = |v_i|_{max} =$ max( $|v_A|, |v_B|, |v_c|$) at all times. It can be shown that for a balanced set of voltages, this gives:

$$|v_{YX}| + |v_{YZ}| = 3|v_Y| = 3|v_i|_{max} \tag{5.22}$$

Therefore, by substituting (5.21) and (5.22) into (5.20), the converter switching loss can be expressed as:

$$E_{sw} = 6|v_i|_{max}|i_o|_{max}(T_{on} + T_{off} + T_{rec}) \tag{5.23}$$

Provided that $|v_i|_{max}$ and $|i_o|_{max}$ vary independently, the mean switching energy power loss per sequence is given by:

$$\overline{P_{sw}} = 6\overline{|v_i|}_{max}\ \overline{|i_o|}_{max}\ (\tau_{on} + \tau_{off} + \tau_{rec})f_{sw} \tag{5.24}$$

The mean terms $\overline{|i_o|}_{max}$ and $\overline{|v_i|}_{max}$ can be expressed in terms of the output rms line current $I_o$ and input rms line-to-line voltage $V_i$ as:

$$\overline{|i_o|}_{max} = \frac{3\sqrt{2}}{\pi} I_o \tag{5.25}$$

$$\overline{|v_i|}_{max} = \frac{\sqrt{6}}{\pi} V_i \tag{5.26}$$

Substituting (5.25) and (5.26) into (5.24) gives the mean commutation power loss in the converter:

$$P_{sw} = \frac{36\sqrt{3}}{\pi^2} V_i I_o \big(\tau_{on} + \tau_{off} + \tau_{rec}\big) f_{sw} \qquad \varphi_i = 0 \tag{5.27}$$

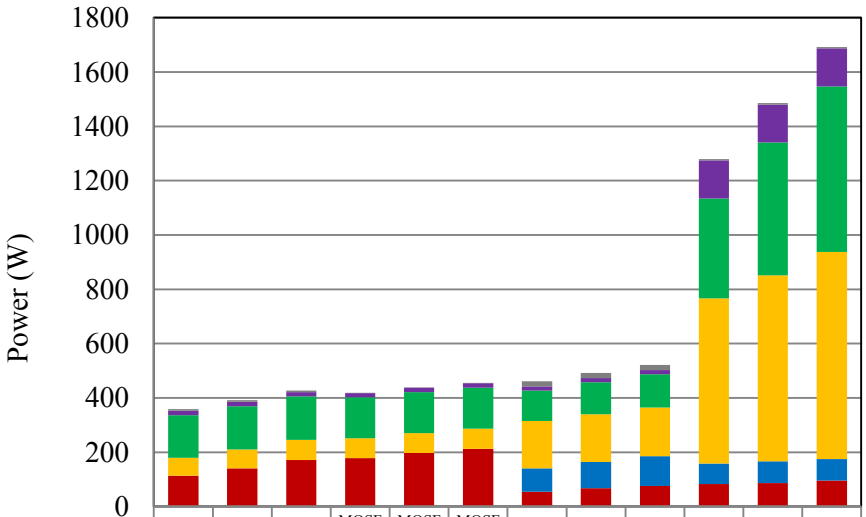
### 5.6.4 Comparative Power Losses Analysis

To determine and evaluate power losses in matrix converter with various power semiconductor devices a three-phase matrix converter is considered and the four-step current commutation strategy is applied. Four different switch devices which are used in evaluation of matrix converter are listed in Table 5.1. A converter with rms output line current of 14A at an rms line to line output voltage of 340V and an rms line to line supply voltage of 400V is used in these calculations.

Based on the mentioned equations for calculating drive, conduction and switching losses, determined on-state resistances and switching energies in previous section and some parameters from the gate or base drive circuit and datasheet of power devices, the drive, conduction and switching losses of matrix converter for various switching devices are determined. Figure 5.32 shows the comparison of the drive loss, conduction loss and switching loss between SiC JFETs, SiC MOSFETs, SiC BJTs, and Si IGBTs three-phase matrix converters for different temperatures when switching frequency and output power of converter are 80 kHz and 8.2 kW respectively. It can be stated that there is a significant decrease in the switching losses of the SiC matrix converter because of low switching energy losses of the SiC JFET, MOSFET and BJT in comparison with the Si IGBT. It should be noted that due to high on-state resistance of SiC MOSFET in compare by other devices, the total conduction loss of SiC MOSFETs are more than Si IGBTs and other SiC devices in matrix converter, although there is no on-state voltage across drain-source of SiC MOSFET. Moreover, the amount of drive loss of SiC BJT is not

significant in compare by other kind of losses so the total power losses of a SiC BJT matrix converter has not been affected dramatically due to drive loss of SiC BJTs. Additionally, there is a significant difference between turn-off power losses of Si diode and SiC Schottky diode due to there is no reverse recovery current in SiC Schottky diode in compare with Si diode.

It should be noted that by using the four-step current commutation, the reverse conduction feature of the SiC MOSFET and JFET can be used and so there is no diode conduction power loss in these kinds of bidirectional switches.




| | JFET 30°C | JFET 80°C | JFET 130°C | MOSFET 30°C | MOSFET 80°C | MOSFET 130°C | BJT 30°C | BJT 80°C | BJT 130°C | IGBT 30°C | IGBT 80°C | IGBT 130°C |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| Driving Loss | 6.0 | 6.0 | 6.0 | 0.0 | 0.0 | 0.0 | 18.5 | 18.5 | 18.5 | 5.2 | 5.2 | 5.2 |
| Power Diode Switching Loss | 15.8 | 15.8 | 15.8 | 15.8 | 15.8 | 15.8 | 15.8 | 15.8 | 15.8 | 139.6 | 139.6 | 139.6 |
| Power Device Turn-off Switching Loss | 157.2 | 158.7 | 159.9 | 150.5 | 150.9 | 151.3 | 112.2 | 117.2 | 122.3 | 368.7 | 488.8 | 609.0 |
| Power Device Turn-on Switching Loss | 65.7 | 69.9 | 74.1 | 72.8 | 73.2 | 73.7 | 173.8 | 176.4 | 179.1 | 607.8 | 685.7 | 763.7 |
| Power Diode Conduction Loss | 0.0 | 0.0 | 0.0 | 0.0 | 0.0 | 0.0 | 86.2 | 95.9 | 109.3 | 75.7 | 79.6 | 78.7 |
| Power Device Conduction Loss | 114.0 | 140.9 | 171.4 | 178.9 | 197.3 | 213.2 | 54.9 | 67.8 | 76.0 | 82.8 | 86.5 | 95.8 |

Figure 5.32: Drive, conduction and switching losses of Si and SiC power devices for an 8.2 kW three phase matrix converter when switching frequency is 80 kHz at different temperatures

The variation of the calculated total matrix converter power losses with varying switching frequency for different Si and SiC power devices operated at

rated output voltage and current at temperature of 130°C is presented in Figure 5.33. The SiC JFET matrix converter is the most efficient as the power losses of it increase by 57% in the considered switching frequency range of 10 kHz to 80 kHz. It is also obvious that the power losses of a three phase matrix converter which is built by SiC power devices is doubled by raising the switching frequency by a factor of eight compared with a Si matrix converter whose power loss is more than quadruple.

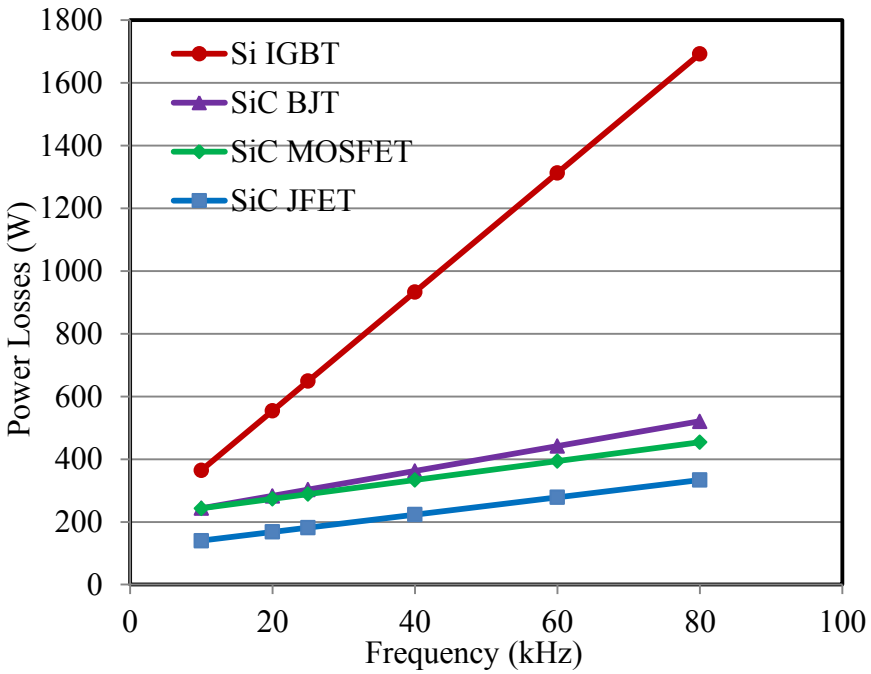



Figure 5.33: Variation of calculated matrix converter losses with switching frequency at rated load and temperature of 130 ºC for various devices

The surfaces in Figure 5.34-5.35 show the variation of the matrix converter power losses for each of power semiconductor devices with output current level and switching frequency when temperature is 30°C and 130°C. It should be noted that by increasing the temperature, there is no significant change in the power losses of the SiC JFET, MOSFET and BJT matrix converter

compared to the Si IGBT matrix converter in high switching frequency and rated output current. The power loss of Si IGBT matrix converter is three times higher than the power loss of the SiC JFET at temperature of 130°C and rated output current.

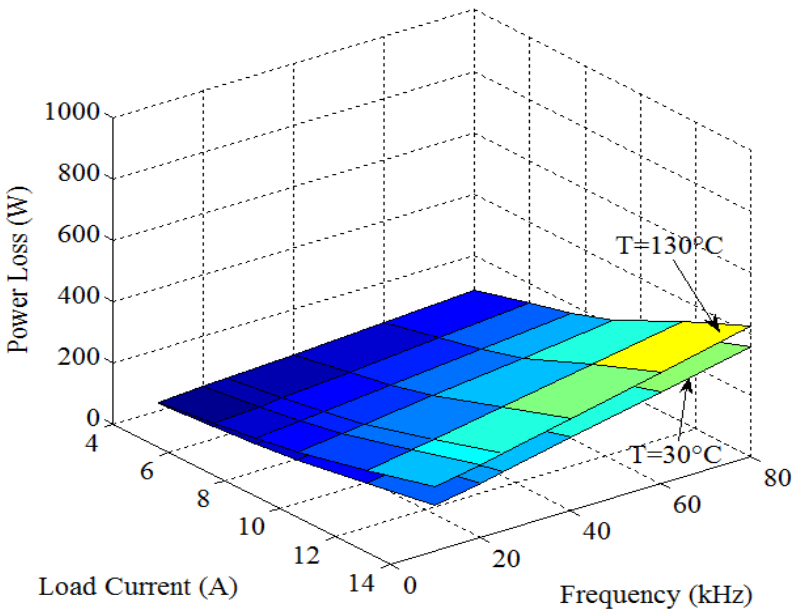



Figure 5.34: SiC JFET matrix converter power losses surface

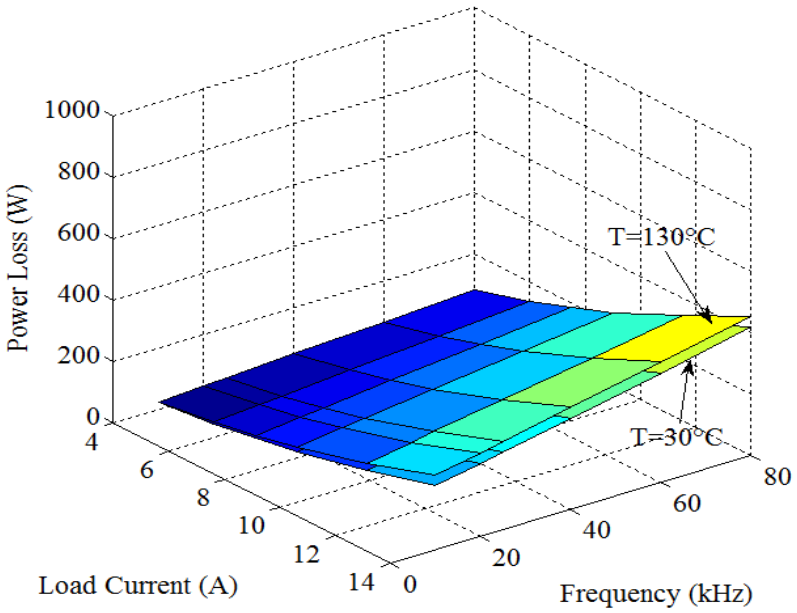



Figure 5.35: SiC MOSFET matrix converter power losses surface

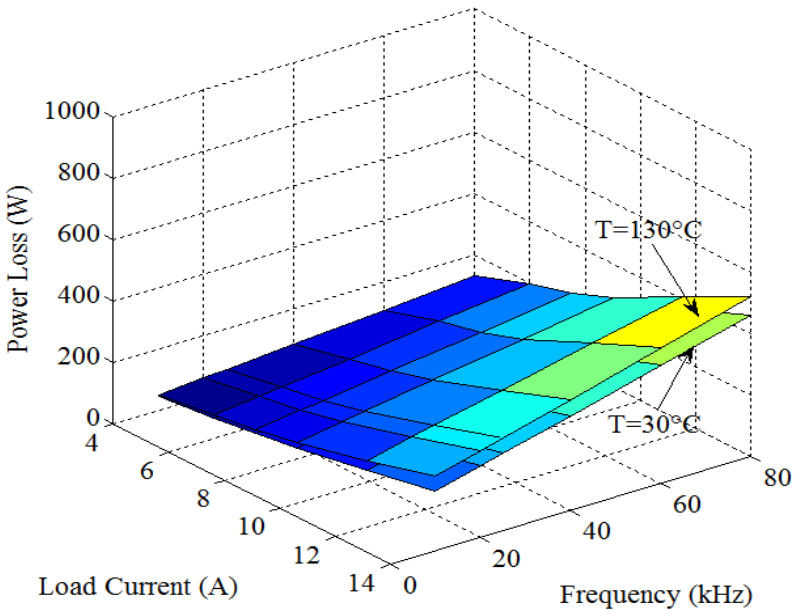



Figure 5.36: SiC BJT matrix converter power losses surface

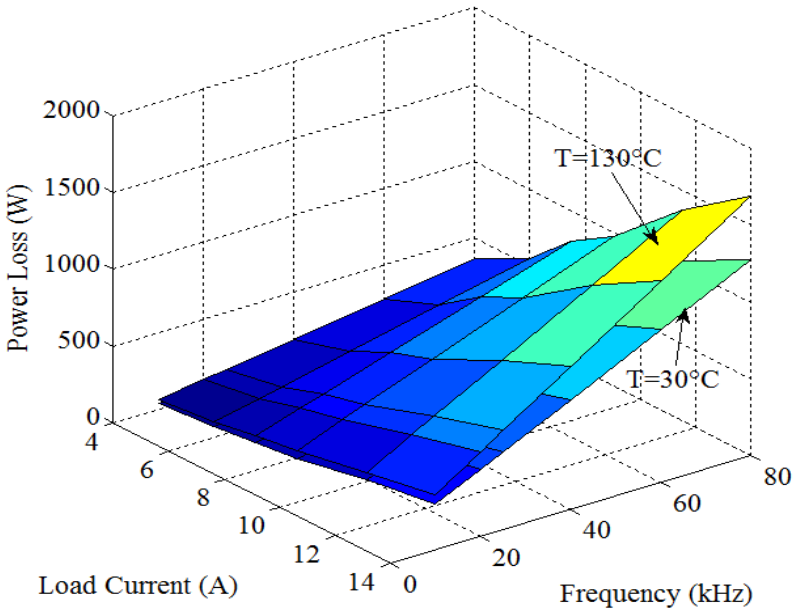



Figure 5.37: Si IGBT matrix converter power losses surface

## 5.7 Summary

In order to study power losses performance of matrix converter with different semiconductor technologies, the static and dynamic characterizations of various available SiC and Si power semiconductor devices which are suitable for high frequency applications have been done at different voltages, currents and temperatures. An electrical model has been developed for power semiconductor devices based on the static characterization. It has also been revealed that SiC power semiconductor devices have significant lower switching energy losses compared to the Si power device.

Analytical descriptions for calculating drive, conduction and switching losses in the matrix converter have been presented for different power semiconductor devices based on the four-step current commutation strategy

and the double-side space vector modulation scheme. Then based on the developed equations, the distributions of the power losses in the matrix converter for different power semiconductor devices were analysed under rated power condition. Also power losses of Si and SiC matrix converters are determined of various switching frequencies, load currents and temperatures and it has been revealed that the SiC matrix converts have lower power losses in comparison with the Si matrix converter in high switching frequency and high temperature for the rated load current. The SiC JFET matrix converter is the most efficient as its power losses are the lowest when increasing the switching frequency by a factor of eight compared to other SiC power semiconductor devices. It can be concluded that the power semiconductor devices realized with SiC have very promising performance which will ensure the power losses reduction and the improvement of power density in the future.

# Chapter 6
# Passive Components Minimization

Passive components such as capacitors and inductors play an important role in converters. They are used to filter the switched discontinuous input currents of the matrix converter in order to enable compliance with power quality standards [99]. The passive components have a significant effect on the overall volume and weight of power converter because of the physical properties of inductors and capacitors.

One of the main goals in designing power converters in recent years is improving power density. Especially for applications such as aerospace and

electric vehicles, this is a very important issue due to limited space and weight constraints. Reducing the weight and volume of passive components in filters can help in achieving higher power density for the power converters [22]. Therefore, it is desirable to minimize the passive components value and size to achieve the design of high power density in power converters.

The values of the passive components in a matrix converter are related to the control strategy, performance requirements and switching frequency. Generally higher switching frequency leads to smaller passive components [22]. This is especially important for high switching frequency matrix converter based on SiC power devices as it will reduce the volume of the input filter and improve the power density of the system. However higher switching frequencies lead to higher switching loss; as presented in Chapter 5. Therefore, a trade-off exists between volume and power loss which needs to be investigated.

This Chapter aims to evaluate the influence of the switching frequency on the input filter volume of the matrix converter. The design of the input filter is performed in order to obtain optimum volume taking into account the power quality standard requirements. This procedure is presented in the following section, starting with the power quality standard, explaining the filter design procedure, dimensioning of the filter components and presenting the obtained results. The influence of the switching frequency on the volume of passive components and the power converter density is presented by taking into account the power loss of converter for different power devices. Finally

simulation and experiment have been conducted to show the performance of the designed filter.

## 6.1 Power Quality Standards

To avoid unacceptable voltage distortion and to limit the overall harmonic distortion of the mains voltage, power quality standards are used to limit the harmonic current injection from individual loads into the supplying mains. The commonly used power quality standard are IEC 61000 (IEC 61000-3-4), EN5006, IEEE 519 and VDE 0838 [105].

In IEEE 519 there is a shared responsibility between the consumer and power supplier for controlling the harmonic voltage and current levels. The power supplier has to control the harmonic voltage distortion, whereas the consumer has to ensure that the current harmonics injected at the Point of Common Coupling (PCC) are within given limits [106].

One of the important figures for assessing the input power quality of a power converter is the Total Harmonic Distortion (THD). For the current, the THD is defined by:

$$THD = \frac{\sqrt{\sum_{h=2}^{h=\infty} I_h^2}}{I_1} \qquad (6.1)$$

where $I_1$ is the amplitude of the fundamental harmonic of the current and $I_h$ is the amplitude of h harmonic of the current.

The limit on maximum current THD that a power electronic converter and other nonlinear load are allowed to inject into the utility system can be based

on IEEE 519 as summarized in Table 6.1. In this work the maximum current THD is limited to 5% because the ratio of the short circuit current to the fundamental of the load current for the power supply is assumed to be less than 20.

| $I_{sc}/I_l$ | Maximum Current THD (%) |
|---|---|
| < 20 | 5.0 |
| 20 - 50 | 8.0 |
| 50-100 | 12.0 |
| 100-1000 | 15.0 |
| > 1000 | 20.0 |

Table 6.1: The maximum current THD based on the IEEE 519 ($I_{sc}$ is the maximum short circuit current at PCC) [90]

Other power quality standards may impose different limits to the individual currents and/or THD, but they are not considered here.

## 6.2 Input Filter Topology

The input filter is used as interface between the AC supply voltage and the matrix converter to prevent unwanted harmonic current flowing into the AC supply and to avoid significant fluctuation in the converter input voltage. The matrix converter behaves as a current source on the input side and produces current harmonics due to the discontinuous input currents. The current harmonics are injected into the power supply and result in voltage distortions that could affect operation of the AC system, so they have to be managed.

# Chapter 6: Passive Components Minimization

The matrix converter input filter design has been addressed in [10, 14, 107, 108] and different configurations have been introduced. The most commonly used input filter is a second order LC filter with a damping resistor in parallel to the inductor, as shown in Figure 6.1.

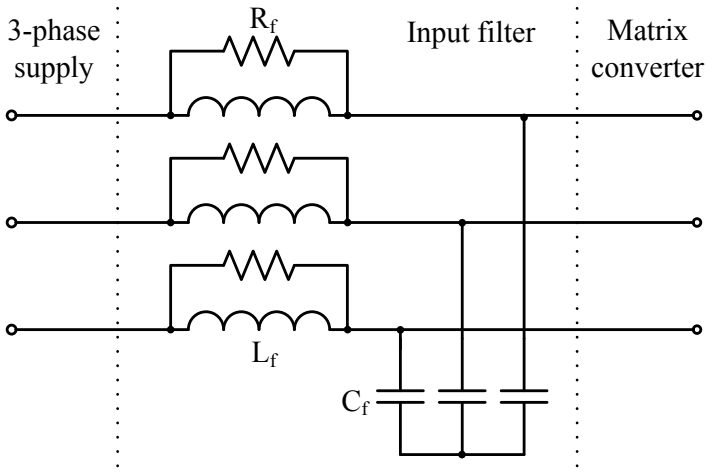



Figure 6.1: LC filter with parallel damping resistor

In order to analyse the input filter characteristics of the matrix converter, an equivalent single-phase matrix converter operating under balanced input and output conditions is considered as shown in Figure 6.2. It should be noted that the matrix converter can be considered as a current sink on the input side and as a voltage source on the output side.

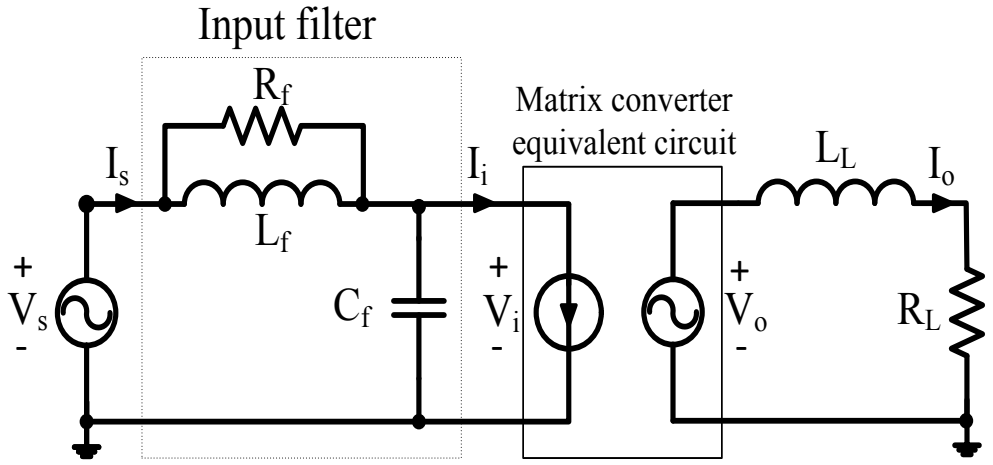



Figure 6.2: Single-phase equivalent circuit of the matrix converter

The relationship between the voltage and current of the input filter can be described using a Laplace transfer function. The relationship between output and input voltages and currents of the filter in the Laplace domain based on Kirchhoff's Voltage Law (KVL) and Kirchhoff's Current Law (KCL) can be expressed as:

$$V_s(s) - V_i(s) = \frac{sR_fL_f}{R_f+sL_f} I_s(s) \tag{6.2}$$

$$I_s(s) - I_i(s) = sC_fV_i(s) \tag{6.3}$$

where, $V_s(s)$, $V_i(s)$, $I_s(s)$ and $I_i(s)$ are the Laplace transforms of the source voltage, the converter input voltage, the source current and the converter input current respectively and $s$ is the Laplace operator. Therefore, the input current can be determined by:

$$I_s(s) = \frac{(R_f + sL_f)I_i(s)}{s^2R_fL_fC_f + sL_f + R_f} + \frac{(R_f + sL_f)sC_fV_s(s)}{s^2R_fL_fC_f + sL_f + R_f}$$

$$= H_i(s)I_i(s) + H_v(s)V_s(s) \quad (6.4)$$

where $H_i(s)$ is the transfer function related to the converter input currents and $H_v(s)$ is the transfer function related to the source voltage. The denominators of $H_i(s)$ and $H_v(s)$ are identical and form a second order system. The natural or cut-off frequency is represented by $\omega_c$ and damping factor is represented by $\xi$.:

$$\omega_c = 2\pi f_c = \frac{1}{\sqrt{L_f C_f}} \quad (6.5)$$

$$\xi = \frac{1}{2R_f}\sqrt{\frac{L_f}{C_f}} \quad (6.6)$$

## 6.3 Calculation of Required Filter Attenuation

Idealized current waveforms for each filter component of a phase are shown in Figure 6.3. The ideal input current is a pure sin wave with amplitude of $I_I$ and a frequency of $f_s$. It is assumed that the current of matrix converter has a fundamental sinusoidal component with a frequency of $f_s$ and a superimposed switching ripple current. For the purpose of this simplification, the ripple current can be sinusoidal with constant amplitude, $I_{HF}$, with the dominant harmonic content which appears at switching frequency, $f_{sw}$ [109].

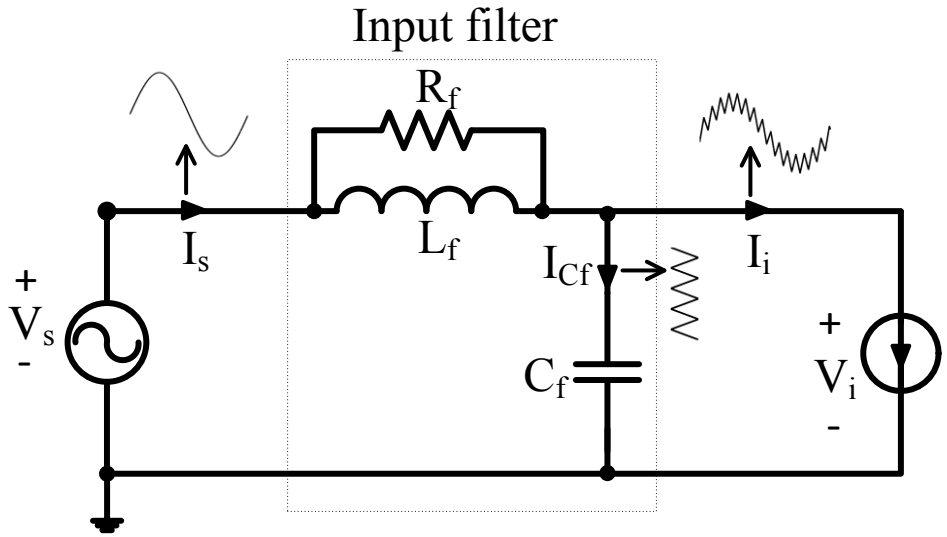



Figure 6.3: Idealized current waveforms for each filter component

Based on the THD definition from equation (6.1), the THD of input current without filter is approximated by:

$$THD_{HF} = \frac{I_{HF}}{I_1} \tag{6.7}$$

The required attenuation of the input filter in order to satisfy the maximum THD of input current constraint can then be determined:

$$Att_{req} = 20\log_{10} THD_{max} - 20\log_{10} THD_{HF}$$

$$= 20\log_{10} THD_{max} - 20\log_{10} \frac{I_{HF}}{I_1} \text{ (dB)} \tag{6.8}$$

The cut-off frequency as a function of the required attenuation and the switching frequency for a second order LC filter can then be determined:

$$f_c = f_{sw} 10^{\frac{Att_{req}}{40dB}} \tag{6.9}$$

## 6.4 Component Limits

In the selection of the input filter, it should be ensured that the reactive power exchange with the supply is minimized. Additionally, the voltage ripple across the input filter capacitor should be small enough to limit the switching frequency ripple content at the output of matrix converter.

Regarding to the reactive power constraint, by considering the rated power of the matrix converter and the required performance (e.g. $\cos(\varphi_i) > 0.9$ for $P_{out} > 10\%$ of rated power), the maximum filter capacitance (star connection), $C_{f,max}$, can be determined by [110]:

$$C_{f,max} = \frac{\tan(\varphi_{i\_max}) \times P_{out}}{3 \times 2\pi f_s V_s^2} \tag{6.10}$$

where $\varphi_{i\_max}$ is the maximum input displacement angle at the minimum output power, $P_{out}$. The variables '$V_s$' and '$f_s$' are the magnitude and frequency of the supply voltage.

The voltage ripple of the input capacitor has to be dimensioned for a maximum peak to peak voltage value. The maximum peak to peak voltage ripple across the input capacitor in this work was limited to 20% of the maximum input voltage amplitude, so the minimum required capacitor can then be determined by [110]:

$$C_{f,min} = \frac{I_o}{4 \times \sqrt{3} \times 0.2 \times f_{sw} V_s} \tag{6.11}$$

Additionally, based on satisfying the requirement of minimizing the voltage drop across the input filter inductor, $\Delta V_{Lf}$ at rated input current, the maximum allowable input filter inductance can be determined [14]:

$$L_{f,max} = \frac{\sqrt{2\left(\frac{\Delta V_{Lf}}{V_s}\right) - \left(\frac{\Delta V_{Lf}}{V_s}\right)^2}}{2\pi f_s} \times \frac{V_s}{I_s} \tag{6.12}$$

It should be noted that the value of the damping resistance must be smaller than the inductor reactance at the cut-off frequency [14]. The damping resistance can be determined based on the inductance and the cut-off frequency:

$$R_f \leq 2\pi f_c L_f \tag{6.13}$$

## 6.5 Volume Estimation of Filter Components

To evaluate the impact of the input filter on the power density of the matrix converter, the volume of the components has to be determined. In this section the relationship between the volume and capacitance and inductance are derived based on commercially available components.

### 6.5.1 Capacitor

The most common used capacitor in the input filter of matrix converter is a metallized polypropylene film capacitor. These capacitors can be made from ferroelectric X7R dielectric [111]. The selected reference manufacturer is EPCOS for the component used in the hardware prototype. Also the component ratings from different manufacturers are very similar and do not need to be considered separately. The volume of the polypropylene capacitors

is derived from the physical dimensions given in the datasheet. Figure 6.4 presents the determined volume versus capacitance for 440V polypropylene film capacitors from EPCOS. By evaluating the relation between volume and capacitance it is found that the volume is proportional to the capacitance for a given rated voltage and proportional to the square of the rated voltage for a given capacitance:

$$Vol_C \propto C_f \; and \; V^2 \tag{6.14}$$

The reason is that, the volume of a capacitor is proportional to the stored energy. The resulting scaling for the volume of capacitor used in this work can be expressed as:

$$Vol_C = K_{C1} C_f V^2 + K_{C2} \qquad 0.5\mu F \leq C_f \leq 10\mu F \;\; and \; V = 440V \tag{6.15}$$

where $K_{C1} = 63.01 \; \frac{cm^3}{V^2 F}$ and $K_{C2} = 7.91 cm^3$ are coefficients for fitting the volume versus capacitance curve as a straight line.

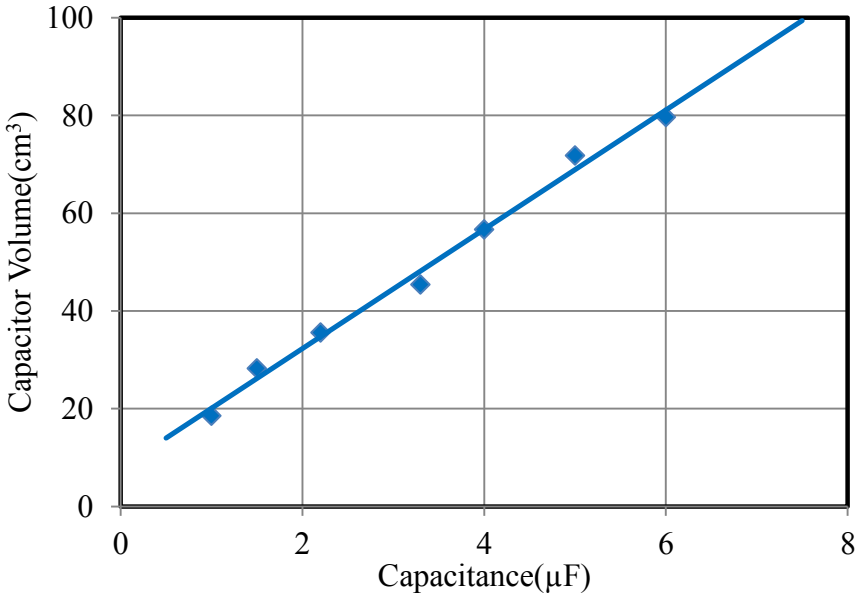



Figure 6.4: Volume versus capacitance of 440V polypropylene film capacitors from EPCOS

### 6.5.2 Inductor

An inductor is used in input filters in order to increase the high frequency impedance of the current path and to reduce the magnitude of the high harmonic currents. The inductance of an inductor is its most important characteristic and is the result of the geometrical configuration of conductors winded onto cores of various materials. A toroidal powder core inductor which provides a good compromise between the achievable inductance per volume as well as AC and DC magnetization properties is used in the input filter of matrix converters [8]. They feature a soft saturation curve, which is good for converter control [111]. The core material of the chosen inductor is Molypermalloy powder (MPP), which is very stable relative to flux density, temperature and current.

In [111] a relationship has been found between the inductor volume, the value of the inductance and the inductor current based on physical devices using their actual inductance and current ratings. Figure 6.5 presents this linear relation between the inductor volume and inductance for different peak values of inductor current.

Similar to the capacitors, the inductor's volume is approximately proportional to the inductance, $L$, for a given current, and also is proportional to the square of the current, $I^2$ for a given inductance:

$$Vol_L \propto L_f \; and \; I^2 \tag{6.16}$$

This finding confirms the expectation the volume of an inductor is approximately proportional to the stored energy.

From the curves shown in Figure 6.5, the dependency between the inductor volume and stored energy can be expressed as:

$$Vol_L = K_{L1} I^2 L_f + K_{L2} \qquad 10\mu H \leq L \leq 300\mu H \tag{6.17}$$

where $K_{L1}$ and $K_{L2}$ are coefficients for fitting the volume versus inductance curve as a straight line. For different currents, they are listed in Table 6.2.

| $I_{peak}$(A) | 5 | 10 | 15 |
|---|---|---|---|
| $K_{L1}(\frac{cm^3}{A^2H})$ | 5659.52 | 3235.94 | 3064.52 |
| $K_{L2}(cm^3)$ | 5.20 | 12.69 | 12.06 |

Table 6.2: Scaling factor of inductor volume

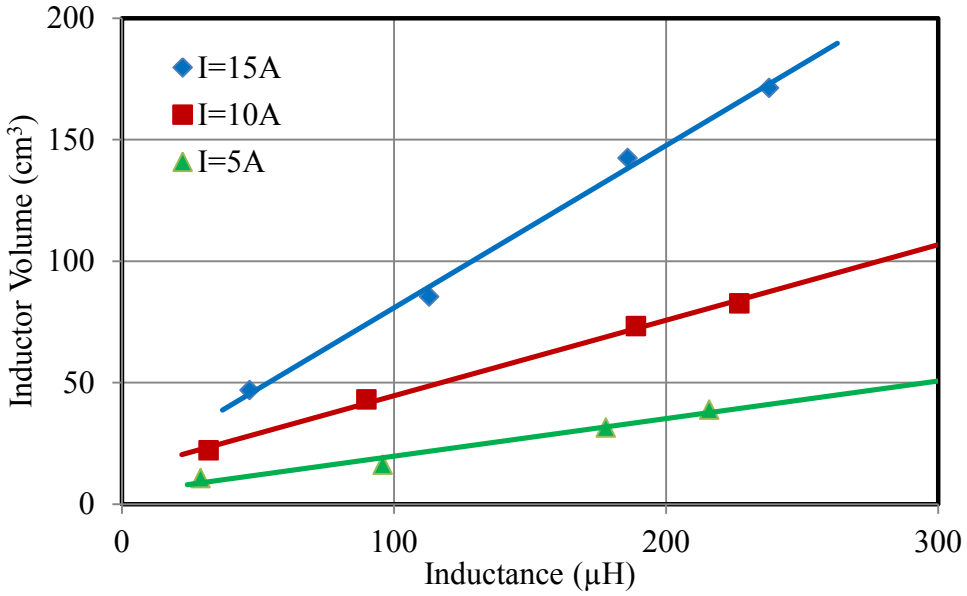



Figure 6.5: Volume versus inductance for toroidal inductors based on the MPP core material for a range of current ratings [97]

## 6.6 Input Filter Design

In order to guarantee that the designed filter is of a minimum volume, the component values can be derived as functions of two equations:

- The required attenuation at the frequencies of interest
- The total volume of the input filter.

The required attenuation of the filter to meet the current THD limit from the converter can be determined using (6.8). Based on the equations (6.5) and (6.9), it can be shown that:

$$LC = \frac{1}{\left(2\pi f_{sw} 10^{\frac{Att_{req}}{40dB}}\right)^2} \tag{6.18}$$

The second equation used in the minimization of the filter design is the total volume of the input filter, which is the sum of the volume of the inductor and capacitor as:

$$Vol_{filter} = Vol_L + Vol_C = K_{L1}L_f I_s^2 + K_{L2} + K_{C1}C_f V_s^2 + K_{C2} \quad (6.19)$$

Rearranging equation (6.18) in terms of $C_f$ and substituting into equation (6.19) gives:

$$Vol_{filter} = K_{L1}L_f I_s^2 + K_{L2} + \frac{K_{C1}V_s^2}{\left(2\pi f_{sw} 10^{\frac{Att_{req}}{40dB}}\right)^2 L_f} + K_{C2} \quad (6.20)$$

By differentiating equation (6.20) with respect to $L_f$ the minimum volume point can be found and the values for the input filter components determined:

$$L_f = \frac{V_s}{2\pi f_{sw} I_s 10^{\frac{Att_{req}}{40dB}}} \sqrt{\frac{K_{C1}}{K_{L1}}} \quad (6.21)$$

$$C_f = \frac{I_s}{2\pi f_{sw} V_s 10^{\frac{Att_{req}}{40dB}}} \sqrt{\frac{K_{L1}}{K_{C1}}} \quad (6.22)$$

where $V_s$ and $I_s$ are the peak values of input voltage and current of the matrix converter.

Filters with minimised volumes can therefore be designed based on the ratings of the components, the current THD limit and the chosen switching frequency of converter, also assuming that parasitic elements do not influence operation of converter.

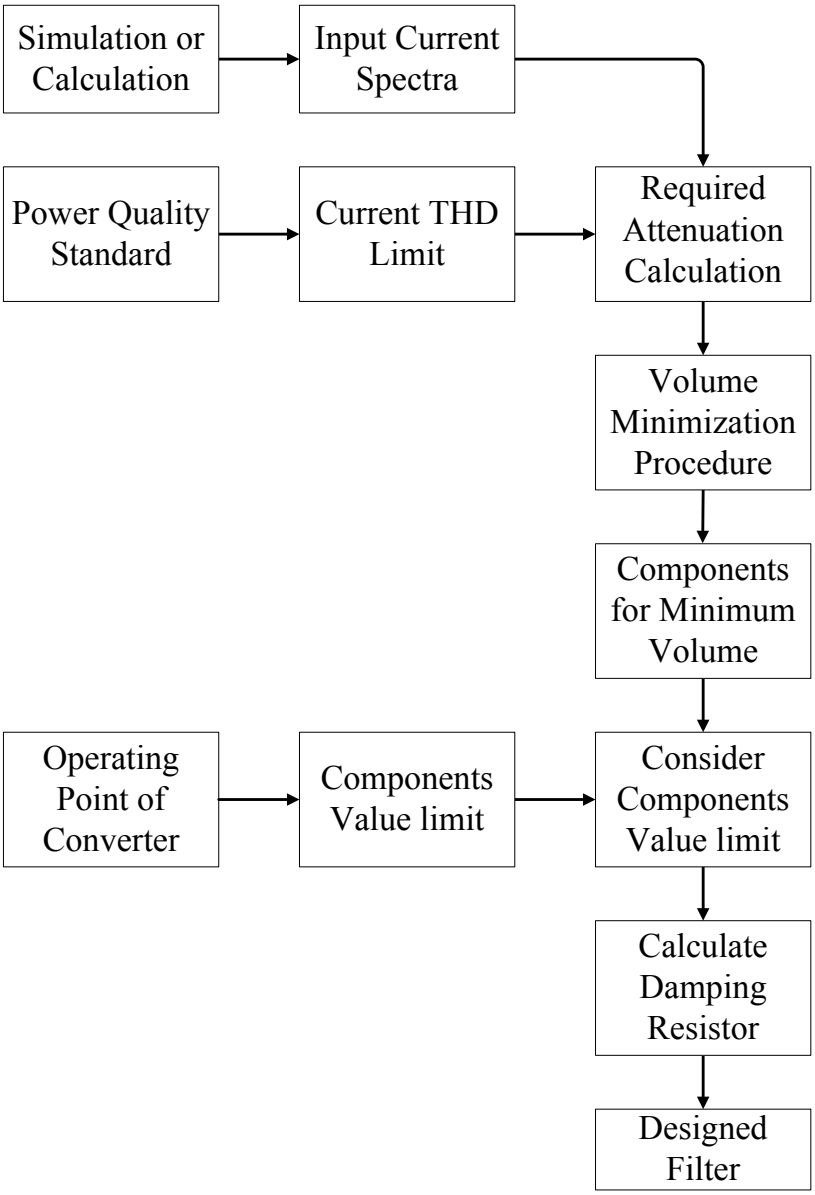



Figure 6.6: Flowchart showing the input filter design procedure

The input filter design procedure is shown as a flow chart in Figure 6.6. The procedure involves the following main steps:

1) Identify and analyse the spectrum of the input current of matrix converter, the spectrum can be calculated or simulated.
2) Determine the required attenuation according to the chosen power quality standard.

3) Calculate the filter component values based on volume minimization procedure and required attenuation.
4) Compare the obtained component value with the maximum and minimum allowable values of components
5) Calculate the damping resistor.

## 6.7 Design Outcomes

Using the above design procedures for input filter, the impact of the filter volume on the achievable power density as a function of switching frequency is considered in this section.

If a 2-phase to 1-phase matrix converter is considered, where the input phase voltage and frequency are 230V and 50Hz respectively and the output current is 7A. The THD limit of 4% is also chosen in order to have some safety margin in design of input filter.

A simulation study has been done using the Saber Software to find the theoretical amplitude of dominant harmonics in the input current of the matrix converter without a filter. Then, based on the obtained amplitudes of current harmonics and desirable THD, the required attenuation of filter can be calculated for different switching frequencies. Additionally the value and volume of the input filter capacitor and inductor can be determined to minimize the overall filter volume.

Figure 6.7 shows the input filter inductance and capacitance values for different switching frequencies. When increasing the switching frequency from

40 kHz to 80 kHz, the inductor and capacitor value is decreased at a lower rate when compared to the step between 10 kHz and 20 kHz.

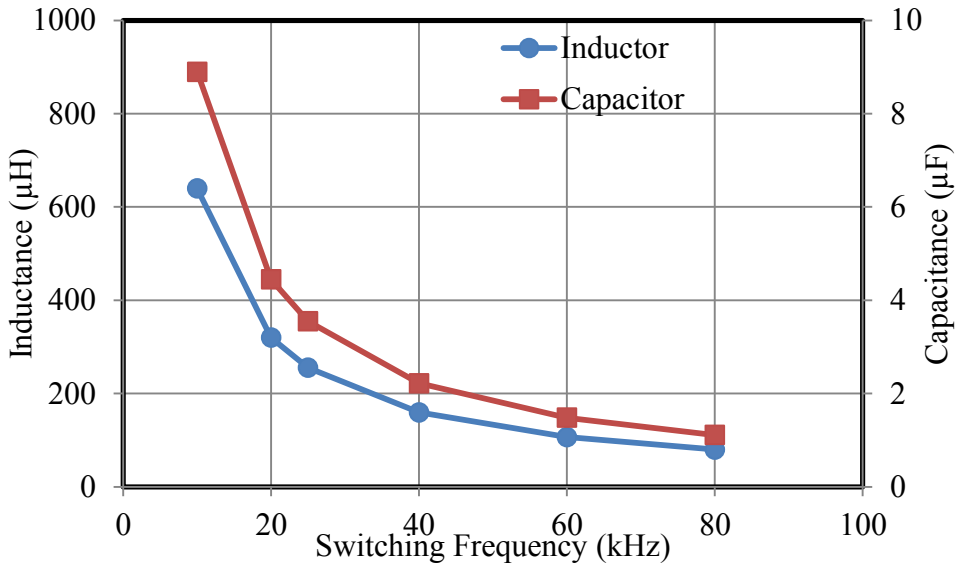



Figure 6.7: Inductor and capacitor values versus switching frequency for the considered input filter design

The input filter for a 2-phase to 1-phase matrix converter consists of two inductors and one capacitor. Figure 6.8 shows the volume of input filter versus switching frequency. It should be noted that the volume of passive components is reduced remarkably by increasing the switching frequency of the converter because the required cut-off frequency becomes higher.

A very useful quantity for investigating the influence of the switching frequency on the filter volume is the power density. It can be defined as the ratio between the rated power of converter and the total volume of the input filter. Figure 6.8 also shows the input filter power density versus the switching frequency of an 800W matrix converter. Figure 6.8 shows that there is a large

increase in the input filter power density gained by increasing the switching frequency.

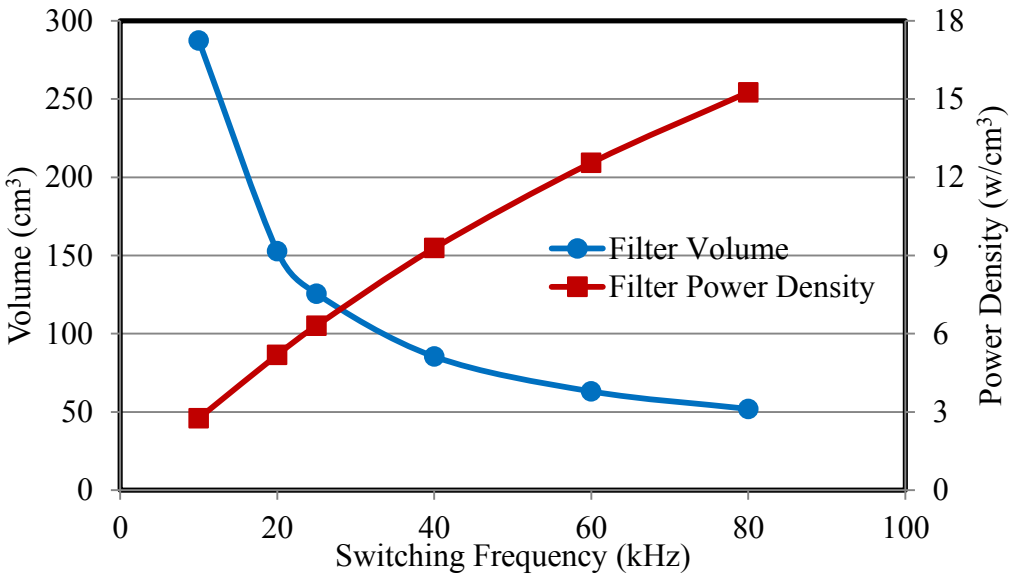



Figure 6.8: Volume and power density of input filter versus switching frequency for an 800W 2-phase to 1-phase matrix converter

Obviously an increase in switching frequency leads to a lower filter volume. However, increasing in the switching frequency leads to higher switching losses in the converter semiconductors. So it is important to investigate the trade-off between overall volume and the converter power losses for different switching frequencies and power device technologies to illustrate the benefit of new device technologies and higher switching frequencies. The power losses for a 2-phase to 1-phase matrix converter can be calculated for different switching frequencies based on the loss calculation method in Chapter 5 when the Si IGBT and SiC MOSFET power device are used. Figure 6.9 shows a plot of input filter volume versus power losses for a 2-phase matrix converter for a range of switching frequencies. The trade-off between power losses and filter

volume can be seen. It is clear that a higher switching frequency leads to higher losses especially for a Si IGBT matrix converter, but by utilizing SiC MOSFETs in the converter is possible to profit from a higher switching frequency without losing too much in converter efficiency.

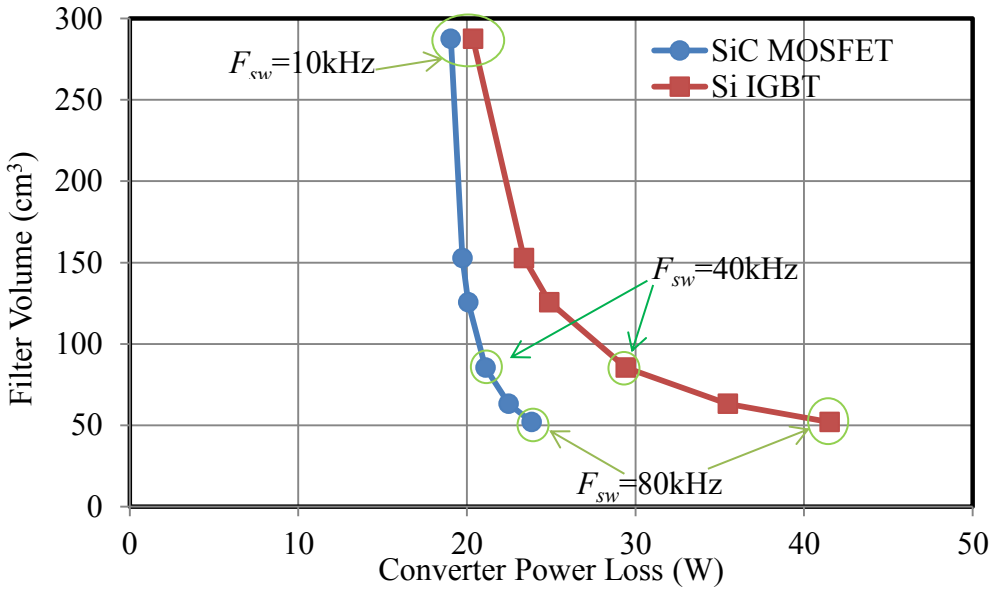



Figure 6.9: Input filter volume versus converter losses for a range of switching frequencies corresponding for 2-phase to 1-phase matrix converter

## 6.8 Simulation and Experimental Results

An input filter design has been selected for the investigation of the power quality requirements. The switching frequency was chosen to be 40 kHz for a converter with a rated power of 800W. Based on the obtained value of capacitor and inductor from the optimization of the input filter volume, capacitors and inductors with close ratings have been chosen from Farnell. The components used for evaluation of the input filter are listed in Table 6.3.

| Switching Frequency (kHz) | Output Power (W) | Capacitor (μF) | Inductor (μH) | Damping resistor (Ω) | Volume of filter ($cm^3$) |
|---|---|---|---|---|---|
| 40 | 800 | 2.2 | 180 | 30 | 95 |

Table 6.3: The used components in input filter

The 2-phase to 1-phase matrix converter circuit with the selected input filter design has been simulated using the Saber Software. The input current of filter is shown in Figure 6.10. The input current THD is 3.59% which is less than the THD constraint. Also the spectrum of the input current is shown in Figure 6.11. The maximum amplitude of the current harmonic around switching frequency is 0.186 A which is about 3.54% of the main harmonic of current.

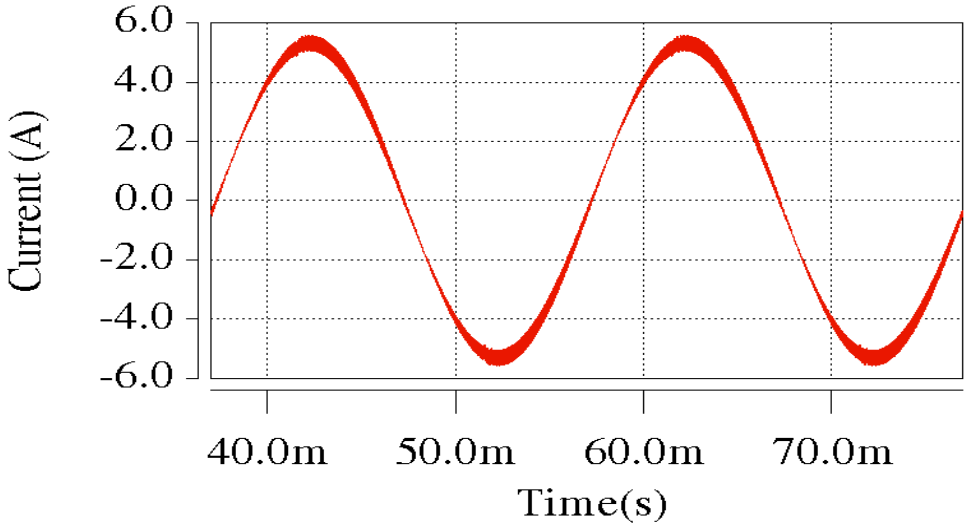



Figure 6.10: Simulated supply current waveform of the selected filter

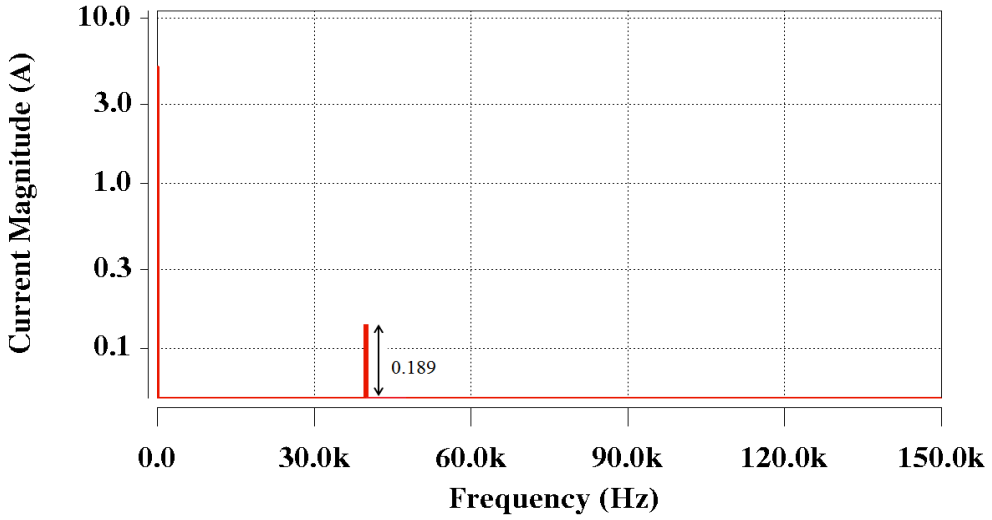



Figure 6.11: Spectrum of simulated filtered input current for the selected filter

Experimental measurement can be conducted to validate the calculations. The 2-phase to 1-phase SiC MOSFET matrix converter has been used for the experimental study. For the purpose of the investigation, the converter has been supplied from a sinusoidal supply with rated rms input phase voltage of 230V at 50 Hz. The connected load is composed of a 16Ω resistor and a 10.5 mH inductor. Figure 6.12 shows the experimental result for input current of matrix converter with the designed input filter while the spectrum of current is shown in Figure 6.13. It can be noted that there is no significant distortion in the input currents. The input current THD is 3.96% which is lower than the considered limitation in the design of filters. Also the maximum amplitude of current harmonic around the switching frequency is 0.196A which is about 3.93% of the main current harmonic.

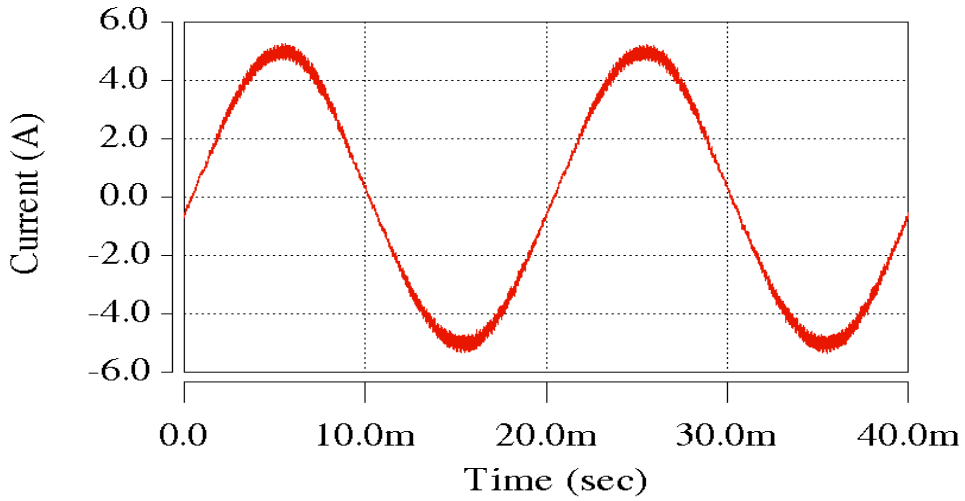



Figure 6.12: Measured input current waveform of matrix converter input filter

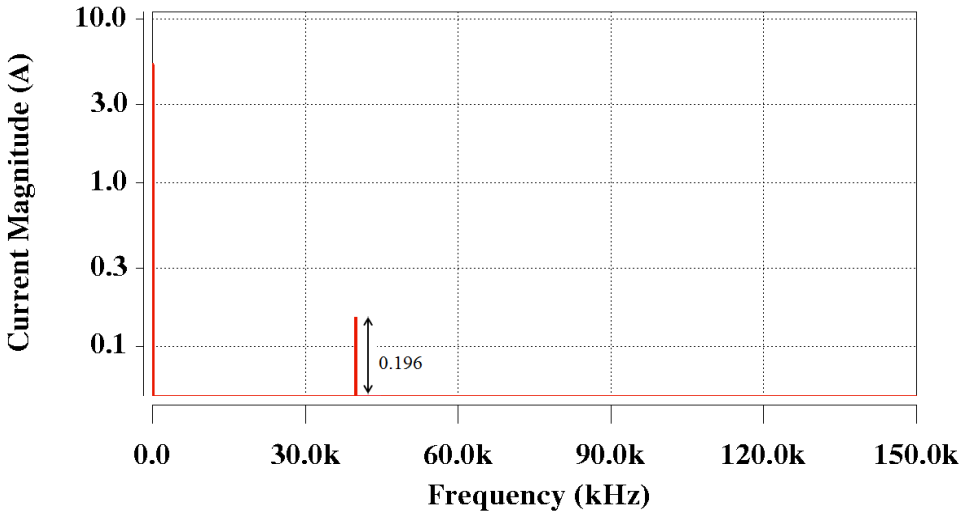



Figure 6.13: Spectrum of measured filtered input current of matrix converter for the selected filter

There is a small difference between the results of simulation and experiment which is due to the delay of the digital control and switching effect. However, the simulation and experimental results presented show the effectiveness of the designed input filter.

## 6.9 Summary

The design considerations and procedures to minimize the volume of passive components in a matrix converter input filter have been developed in this Chapter. The impact of the switching frequency on the filter cut-off frequency has been studied. It has been shown that a higher switching frequency will lead to a smaller input filter and can increase the power density of the converter. It has also been shown that there is a trade-off between the input filter volume and power losses in the converter and by utilizing SiC power devices in a matrix converter, it is possible to achieve higher power density with lower power loss in comparison with Si power devices.

# Chapter 7
# Challenges of SiC Power Devices

The SiC power semiconductor devices enable potentially increase in the switching frequency of power converters. The potential improvements of the matrix converter using the SiC power devices regarding the system efficiency and power losses performance and power density have been presented in Chapter 5 and 6. However by utilizing SiC power devices in matrix converter, issues such as output waveform nonlinear distortion and the effect of parasitic inductance become more dominant.

This Chapter deals with two important issues related to high switching frequency and high switching speed features of power SiC devices which are output waveform nonlinear distortion and the influence of parasitic inductance. First the performance of the matrix converter in terms of quality of output

waveforms which are related to the chosen switching frequency and the commutation time set by the commutation scheme is investigated to highlight the effect of the commutation time limitations at high switching frequency. Additionally, by applying three-step current commutation strategy and minimizing commutation time, the output waveforms quality of matrix converter is enhanced at high switching frequency.

In the second section of this Chapter, analytical and experimental investigations into the influence of parasitic inductance on the SiC power devices performance in matrix converter are carried out. This is done to highlight that the parasitic inductance of the device package and PCB board can cause severe ringing in the switching waveforms and penalties of worsened device stresses and electromagnetic interference (EMI) can be created by faster switching speed power device.

## 7.1 Output Waveform Nonlinear Distortion

The commutation procedure from one bidirectional switch to another one is very important for practical matrix converter as this has been described in Chapter 3. There is a commutation time or delay in the four-step current commutation strategy. The duration of the commutation time depends on the type of power device that is used in the matrix converter, the gate drive path propagation delay and output current, as well as temperature [112, 113]. In compared to the period of the low frequency modulation waveform, the commutation time is typically negligible. However, its cumulative effect over multiple cycles of the carrier waveform can increase the harmonic distortion of output waveform and reduce the amplitude of the fundamental output voltage.

These effects are more pronounced at high switching frequencies where the commutation time is a large portion of the total switching time.

Distortion of output waveforms due to the commutation time is reported in [112, 114-116]. Also in [112] an approach has been developed for determining the output voltage error due to commutation effect which is used in this work. However, the higher switching frequency that SiC power devices can offer is an important aspect which has significant effect on the output waveforms quality. Therefore, it is necessary to investigate the influence of the commutation time on output waveforms distortion at high switching frequency.

### 7.1.1 Commutation Time Effect

Commutation between bidirectional switches in matrix converter is an important issue. It should be done in a way to avoid input line to line short circuit and output open circuit. The four-step commutation based on output current direction technique is a well-known and reliable commutation scheme and is used here to analyse the commutation time effect [7].

The schematic of a two bidirectional switches representing input phase A and B and output phase *a* of a three-phase matrix converter, shown in Figure 7.1, is considered.

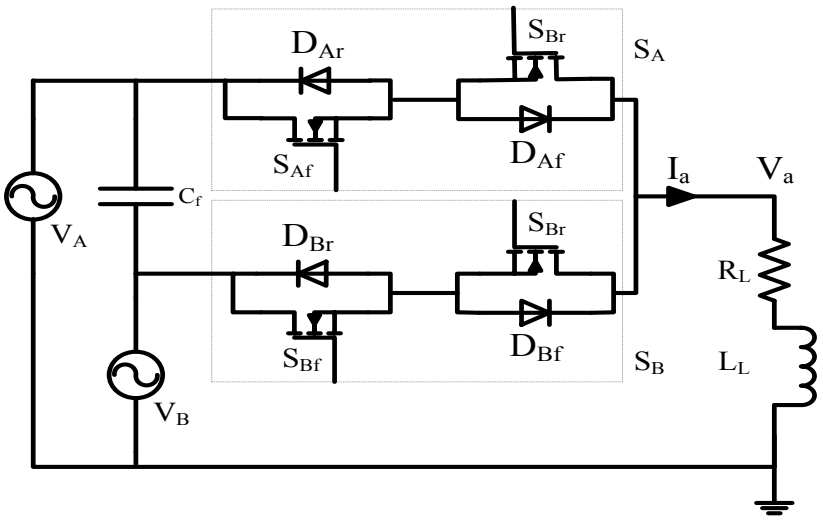



Figure 7.1: Schematic of two bidirectional switch

For a positive output current, the four-step current based commutation sequence needed to transfer the output voltage from input phase A to input phase B and vice versa as illustrated in Figure 7.2 and Figure 7.3 respectively.

Considering the commutation from phase A to phase B when the outgoing input voltage is higher than the incoming input voltage as shown in Figure 7.2. First step of commutation sequence is turning off the reverse switch of the input phase A, $S_{Ar}$; this step will not affect the output voltage. The new output voltage appears at the output voltage, $V_a$ , at the third step in the commutation sequence because $D_{Bf}$ is reverse biased and no commutation takes place when $S_{Bf}$ is turned on. This results in a hard turn-off switching in power switching device $S_{Af}$. In this case, voltage-time product error, $\Delta e_{cd}$, which is shown by shaded area in Figure 7.2 and caused by commutation time, is determined by:

$$\Delta e_{cd(A\rightarrow B)} = (t_{d1} + t_c + \frac{t_f}{2})V_{AB} \qquad (7.1)$$

where $t_f$ is the fall time of the power device.

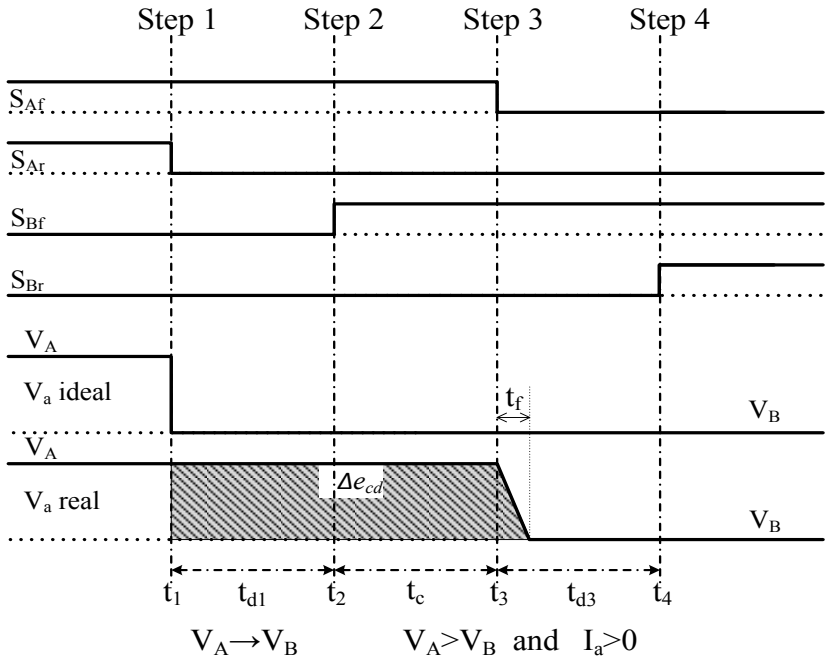



Figure 7.2: Four-step current base commutation sequence from phase A to phase B for positive output current ($I_a > 0$) and $V_A > V_B$

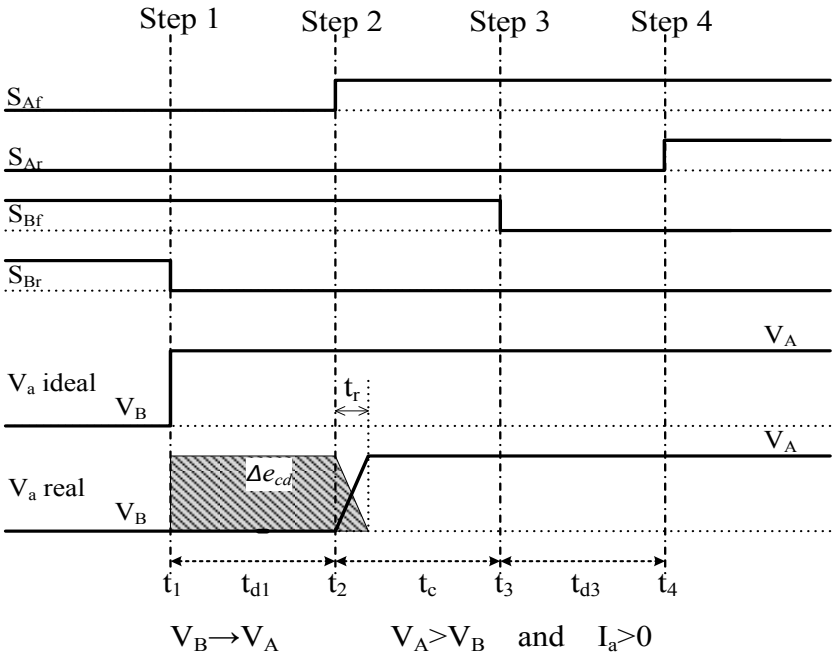



Figure 7.3: Four-step current base commutation sequence from phase B to phase A for positive output current ($I_a > 0$) and $V_A > V_B$

Furthermore, for the commutation from low voltage phase B to high voltage phase A as shown in Figure 7.3, first step of commutation sequence is turning

off the reverse switch of the input phase B, $S_{Br}$; this step will not affect the output voltage. The new output voltage appears at the output voltage $V_a$ at the second step in the commutation sequence because the diode $D_{Bf}$ is reverse biased and commutation takes place immediately at this step. Again, the voltage-time product error introduced by commutation time effect and shown in Figure 7.3 is given by:

$$\Delta e_{cd(B\rightarrow A)} = (t_{d1} + \frac{t_r}{2})V_{BA} \tag{7.2}$$

where $t_r$ is the rise time of the power device.

The total voltage-time product error of commutation A→B→A for positive output current can be calculated as:

$$\Delta e_{cd(A\rightarrow B\rightarrow A)} = \Delta e_{cd(A\rightarrow B)} + \Delta e_{cd(B\rightarrow A)} = (t_c + \frac{t_f - t_r}{2})V_{AB} \tag{7.3}$$

It can be seen from (7.3) that the effect of commutation sequence A→B→A can be considered as injecting of a voltage-time product error to the output voltage of matrix converter for positive output current.

Similarly, for the negative output current the commutation time effect for commutation from phase A to phase B and vice versa are presented in Figure 7.4 and Figure 7.5 respectively. The total voltage-time product error of commutation A→B→A in this case is:

$$\Delta e_{cd(A\rightarrow B\rightarrow A)} = \left(t_{d1} + \frac{t_r}{2}\right)V_{AB} + \left(t_{d1} + t_c + \frac{t_f}{2}\right)V_{BA}$$

$$= (t_c + \frac{t_f - t_r}{2})V_{BA} \tag{7.4}$$

In this case, the commutation time effect can be considered as the subtraction of an extra voltage-time product error from the output voltage of the matrix converter. The overall commutation time effect can be combined to give:

$$\Delta e_{cd(A\rightarrow B\rightarrow A)} = (t_c + \frac{t_f - t_r}{2}) V_{AB} sign(I_a) \qquad (7.5)$$

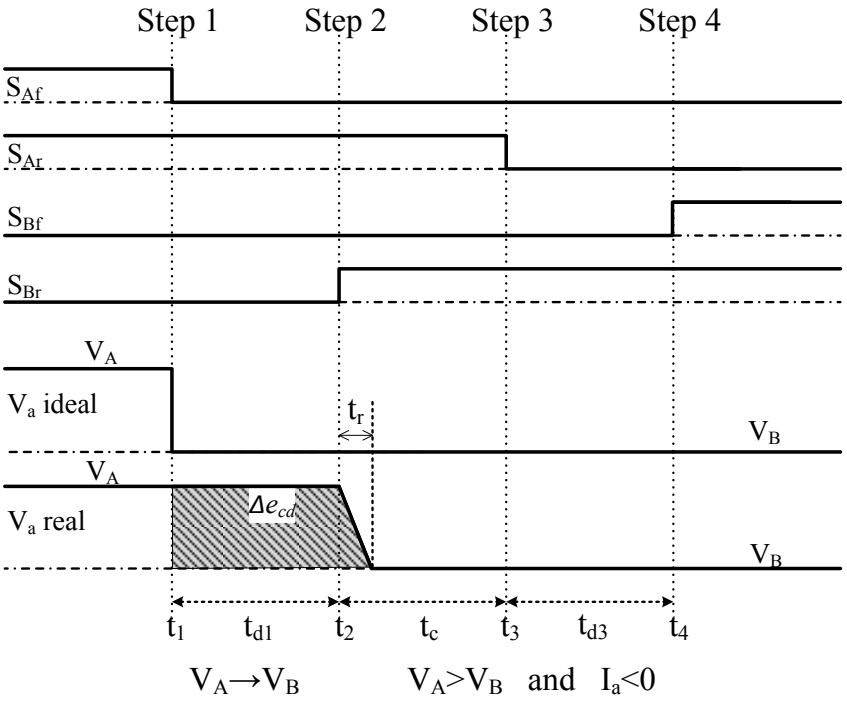



Figure 7.4: Four-step current base commutation sequence from phase A to phase B for negative output current ($I_a < 0$) and $V_A > V_B$

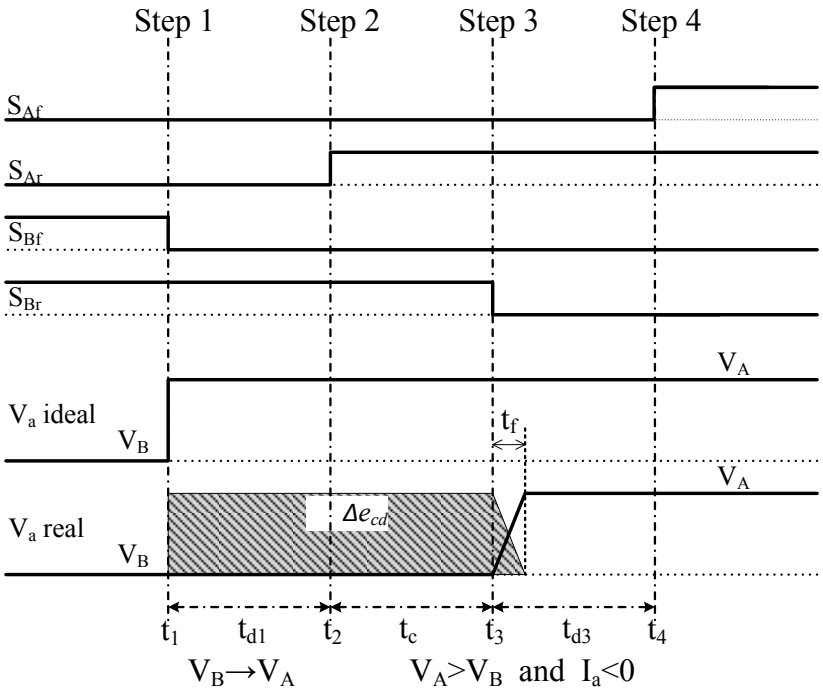



Figure 7.5: Four-step current base commutation sequence from phase B to phase A for negative output current ($I_a < 0$) and $V_A > V_B$

In order to quantify the total voltage error due to commutation time effect, the number of commutations per second and also the switching pattern are needed to know and consider. The switching pattern of the double side space vector modulation is considered in the determination of the total voltage error due to commutation time effect. The double-side switching pattern depends on the input voltage sectors as indicated in Figure 7.6. The total voltage error caused by the commutation time per PWM period can be determined for the switching pattern of input sector 1 as presented in Figure 7.7. It can be seen from Figure 7.7 that there are totally 12 commutations in each PWM period and four commutations for each output phase. The commutation sequence on each output phase in input sector 1 is ($V_C \rightarrow V_A \rightarrow V_B \rightarrow V_A \rightarrow V_C$). Furthermore, in the sector 1, there is $V_A > V_B$ and $V_A > V_C$; therefore, the total

voltage-time product error of the four commutation sequences for the output phase *a* in one PWM period is given by:

$$\Delta e_{cd-a(C\to A\to B\to A\to C)} = \Delta e_{cd(A\to B\to A)} + \Delta e_{cd(A\to C\to A)} =$$

$$= V_{AB}\left(t_c + \frac{t_f - t_r}{2}\right) sign(I_a) + V_{AC}\left(t_c + \frac{t_f - t_r}{2}\right) sign(I_a) =$$

$$= 3V_A\left(t_c + \frac{t_f - t_r}{2}\right) sign(I_a) \qquad (7.6)$$

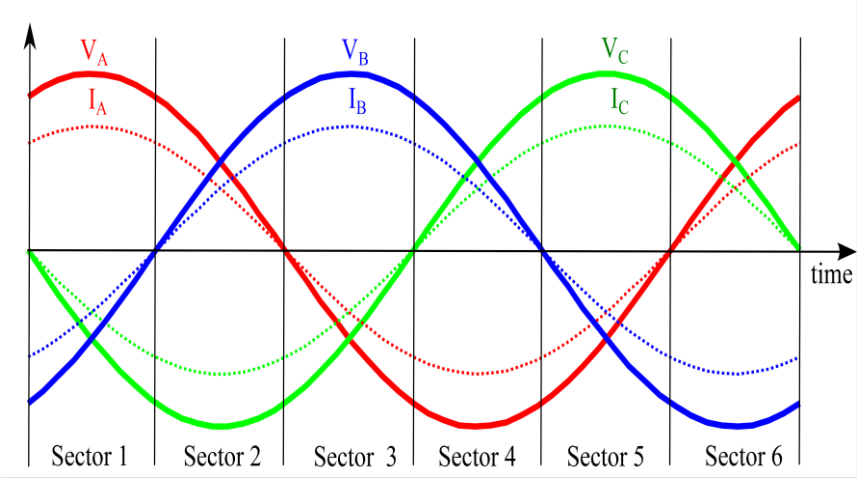



Figure 7.6: The input voltage sectors in matrix converter

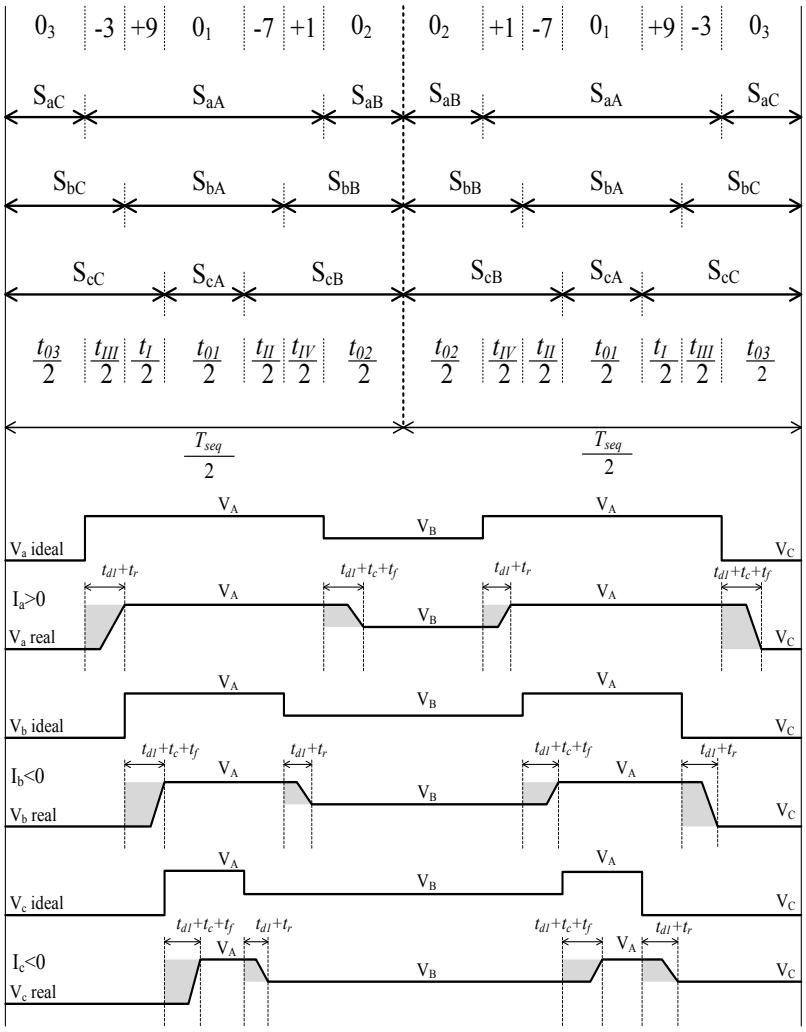



Figure 7.7: The double-sided switching pattern of SVM in input sector 1 in a PWM period

Similarly, the total voltage-time product error due to commutation time for output phases B and C can be determined as:

$$\Delta e_{cd-b(C\to A\to B\to A\to C)} = 3V_B\left(t_c + \frac{t_f - t_r}{2}\right) sign(I_b) \tag{7.7}$$

$$\Delta e_{cd-c(C\to A\to B\to A\to C)} = 3V_C\left(t_c + \frac{t_f - t_r}{2}\right) sign(I_c) \tag{7.8}$$

Therefore, the voltage error for each output phase in input sector 1 can be given by:

$$\Delta VE_{cdj} = \frac{\Delta e_{cd-a}}{T_{seq}} = 3V_A \frac{t_c + \frac{t_f - t_r}{2}}{T_{seq}} \, sign(I_j) \quad j = \{a, b, c\} \qquad (7.9)$$

where $T_{seq}$ is the period of the switching. The maximum and minimum values of the input phase voltage in sector 1 are $\tilde{V}_A$ and $\tilde{V}_A sin(\pi/3)$ respectively; therefore, the maximum and minimum values of voltage error due to commutation delay are determined as:

$$\Delta VE_{cdj-MAX} = 3\tilde{V}_A \frac{t_c + \frac{t_f - t_r}{2}}{T_{seq}} \, sign(I_j) \qquad j = \{a, b, c\} \qquad (7.10)$$

$$\Delta VE_{cdj-MIN} = 3\tilde{V}_A \sin\left(\frac{\pi}{3}\right) \frac{t_c + \frac{t_f - t_r}{2}}{T_{seq}} \, sign(I_j) \quad j = \{a, b, c\} \qquad (7.11)$$

The same analysis can be carried out for the other five input sectors by considering the new patterns of the input voltage commutations. The voltage errors for the all input sector are listed in Table 7.1.

It should be noted that the value of the voltage error due to commutation delay is independent of the sector because the value of the input voltages in sector 1, 3 and 5 are equal. Also the value of the input voltage in sector 2, 4 and 6 are equal, but of opposite sign of odd sectors. Therefore, the maximum and minimum values which have been calculated for sector 1 are also valid for the other sectors.

| Input Sector | Voltage error ($\Delta VE_{cd}$) |
|---|---|
| 1 | $3V_A \frac{t_c + \frac{t_f - t_r}{2}}{T_{seq}} sign(I_j) \quad j = \{a, b, c\}$ |
| 2 | $3V_C \frac{t_c + \frac{t_f - t_r}{2}}{T_{seq}} sign(I_j) \quad j = \{a, b, c\}$ |
| 3 | $3V_B \frac{t_c + \frac{t_f - t_r}{2}}{T_{seq}} sign(I_j) \quad j = \{a, b, c\}$ |
| 4 | $3V_A \frac{t_c + \frac{t_f - t_r}{2}}{T_{seq}} sign(I_j) \quad j = \{a, b, c\}$ |
| 5 | $3V_C \frac{t_c + \frac{t_f - t_r}{2}}{T_{seq}} sign(I_j) \quad j = \{a, b, c\}$ |
| 6 | $3V_B \frac{t_c + \frac{t_f - t_r}{2}}{T_{seq}} sign(I_j) \quad j = \{a, b, c\}$ |

Table 7.1: The voltage error due to commutation time effect introduced by matrix converter using four-step current commutation and double-side space vector modulation

It can be stated that due to commutation time effect, there is addition or subtraction of a voltage error in the output voltage of matrix converter depending on the current direction as is illustrated in Figure 7.8.

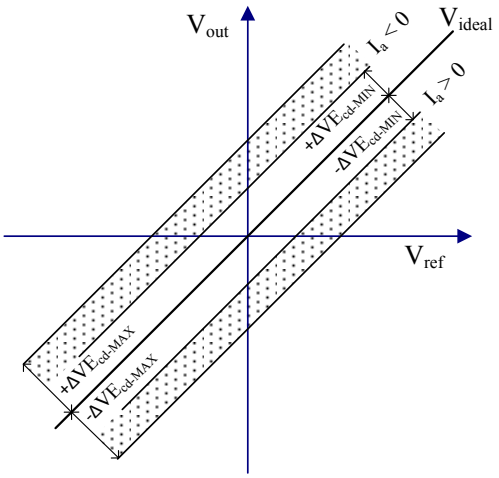



Figure 7.8: Output voltage of matrix converter due to commutation time effect

### 7.1.2 Enhance Waveform Quality Using Minimized Commutation Time

The voltage error caused by the commutation time for a matrix converter with different power devices, commutation times and switching frequencies are calculated and listed in Table 7.2. It can be noted from Table 7.2 that although the voltage error value due to commutation time effect for low switching frequency seems small, the associated adverse effect of commutation time on output performance becomes relevant at high switching frequency. So it is very important to decrease the commutation time as much possible to minimize its effect.

| Device | Switching frequency | Input voltage | Fall time | Rise time | Commutation time | Voltage error |
|---|---|---|---|---|---|---|
| Si IGBT | 10 kHz | 230 V | 275 ns | 55ns | 1µs | 6.25V |
| SiC MOSFET | 80 kHz | 230 V | 21 ns | 34ns | 1µs | 45.11V |
| SiC MOSFET | 80 kHz | 230 V | 21 ns | 34ns | 50ns | 2.29V |

Table 7.2: Voltage error due to commutation time effect for different switching frequencies and power devices

As the SiC power devices are fast speed switching devices, the commutation time can be reduced to zero in order to decrease the output waveform distortion. This means that the four-step output current commutation strategy reduces to a three-step current commutation strategy as shown in Figure 7.9. In this strategy the commutation time influence is obviously at a minimum, and the output waveform distortion can be effectively eliminated.

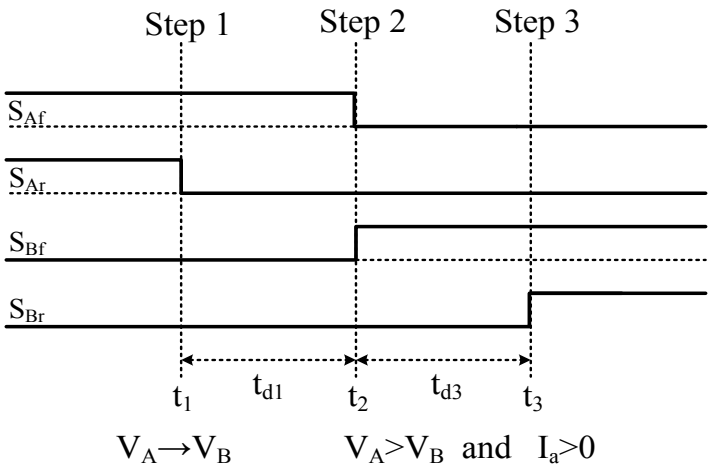



Figure 7.9: Three-step current commutation strategy

### 7.1.3 Experimental Results

Experiments have been performed to investigate the influence of the commutation time on output waveforms distortion of matrix converter at different switching frequencies and present performance of three-step current commutation strategy. For the purpose of the investigation, the SiC MOSFET matrix converter has been supplied by a sinusoidal supply at 50 Hz and the output connected to load. The load is composed of a 20Ω resistor and a 10 mH inductor. Also the commutation time has been varied from 0 to 2000nsec when the switching frequency of matrix converter was 10, 20, 40, 80 kHz.

Figure 7.10 shows the output current and voltage waveforms of a matrix converter when the switching frequency and the commutation time are 80 kHz and 2000nsec respectively. It is clear that the output current waveform has been deteriorated remarkably and there is significant distortion in the output voltage waveform especially when the value of the output current is near to zero as is highlighted in Figure 7.10. The harmonic spectrum of output current

also is shown in Figure 7.11 and it is obvious that output current harmonics values have very high value in compare with first harmonic.

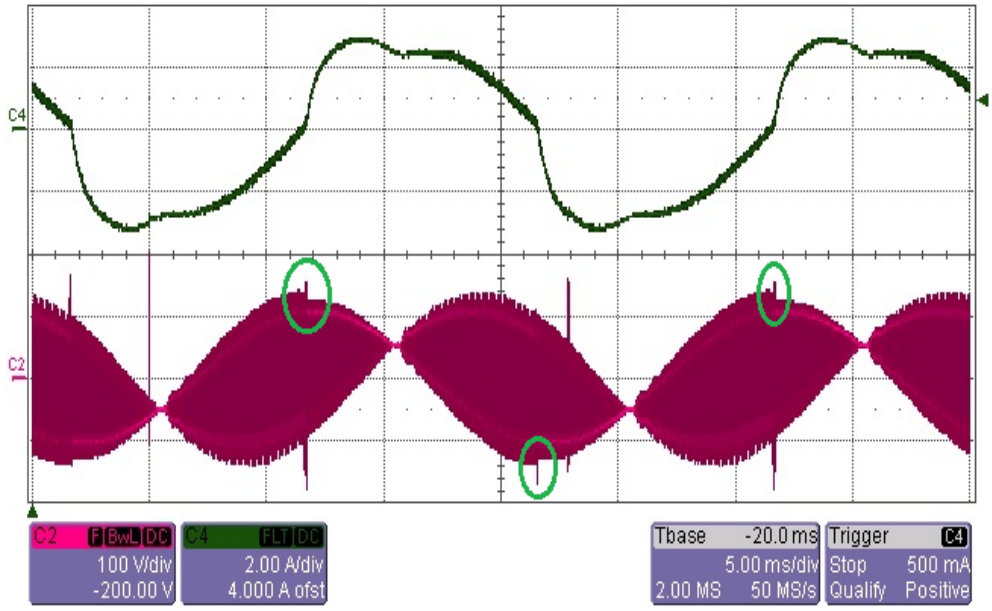



Figure 7.10: Output current (CH4:2A/div) and output voltage (CH2:100V/div) when the switching frequency and commutation time of matrix converter are 80 kHz and 2000 nsec respectively

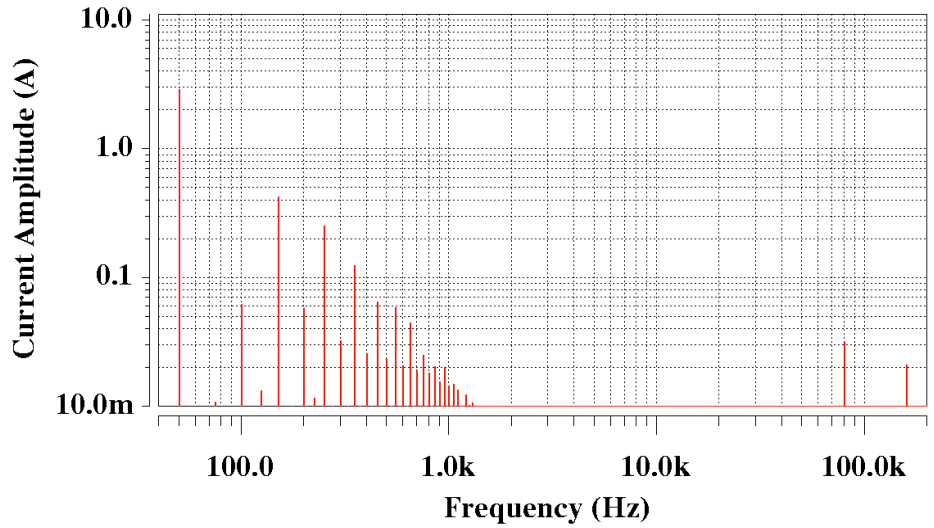



Figure 7.11: Harmonic spectrum of output current when the switching frequency and commutation time of matrix converter are 80 kHz and 2000 nsec respectively

Furthermore, the output current and voltage waveforms of a matrix converter when the switching frequency and the commutation time are 80 kHz

and 0nsec respectively are shown in Figure 7.12. It is clear from Figure 7.12 that by applying three-step current commutation strategy, there is no significant distortion in output current waveform. It can also be seen from current harmonic spectrum as shown in Figure 7.13 that 3rd, 5th, 7th and 13th current harmonics have very low values in comparison with the fundamental current harmonic.

Additionally by comparing Figure 7.10 and Figure 7.12 for different commutation times, it can be stated that the output waveform quality deteriorates as the commutation time is increased. However, output waveforms distortion can be avoided using three-step current commutation strategy at high switching frequency.

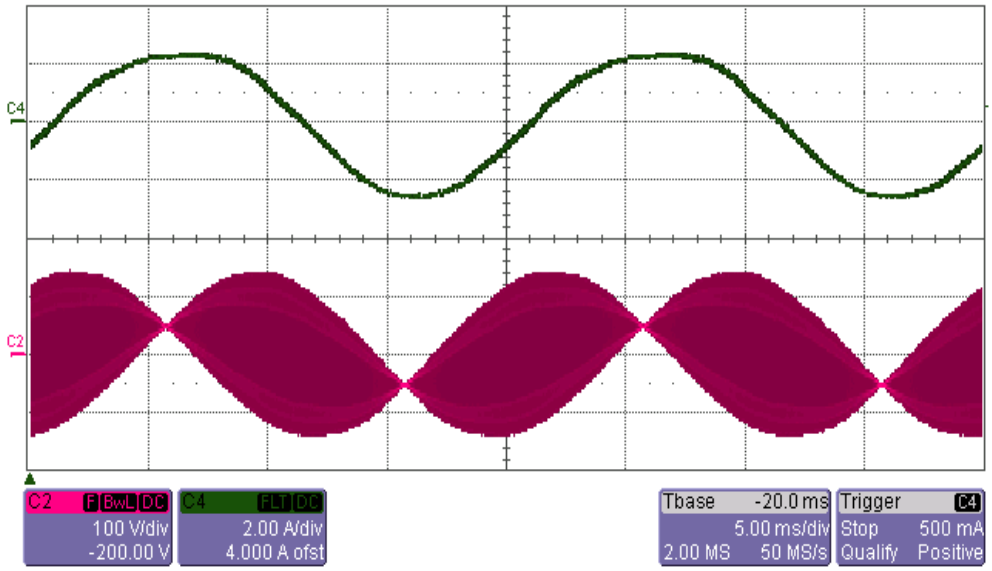



Figure 7.12: Output current (CH4:2A/div) and output voltage (CH2:100V/div) when the switching frequency and commutation time of matrix converter are 80 kHz and 0 nsec respectively

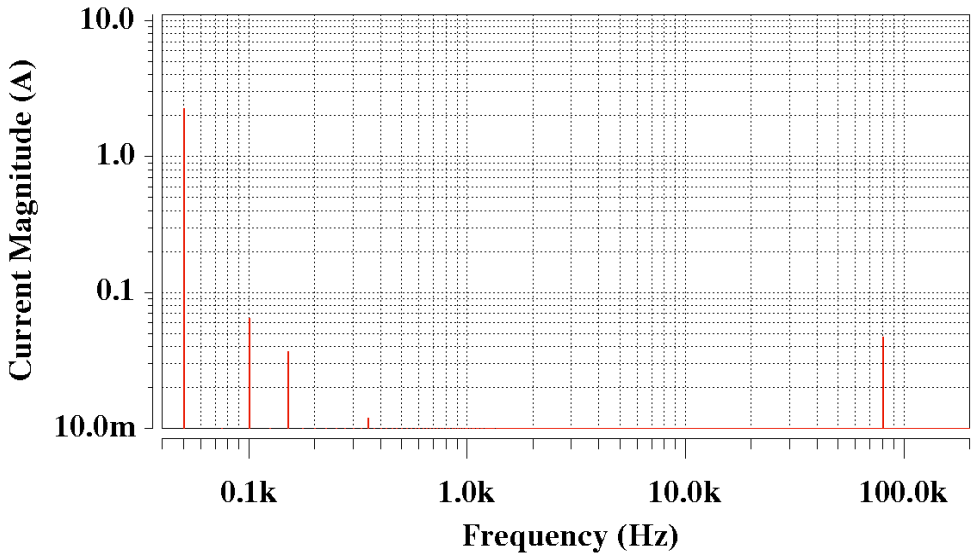



Figure 7.13: Harmonic spectrum of output current when the switching frequency and commutation time of matrix converter are 80 kHz and 0 nsec respectively

The output voltage and current waveforms for a range of switching frequencies and commutation times were exported from the oscilloscope as a data file and Matlab software was used for calculating the THD of the output current (up to 2 kHz) and third harmonic output voltage amplitude. Figure 7.14 shows the output current THD as the commutation time and switching frequency are changed. It can be seen that influence of commutation time on the output current THD is significant and high commutation time deteriorates quality of output current waveform.

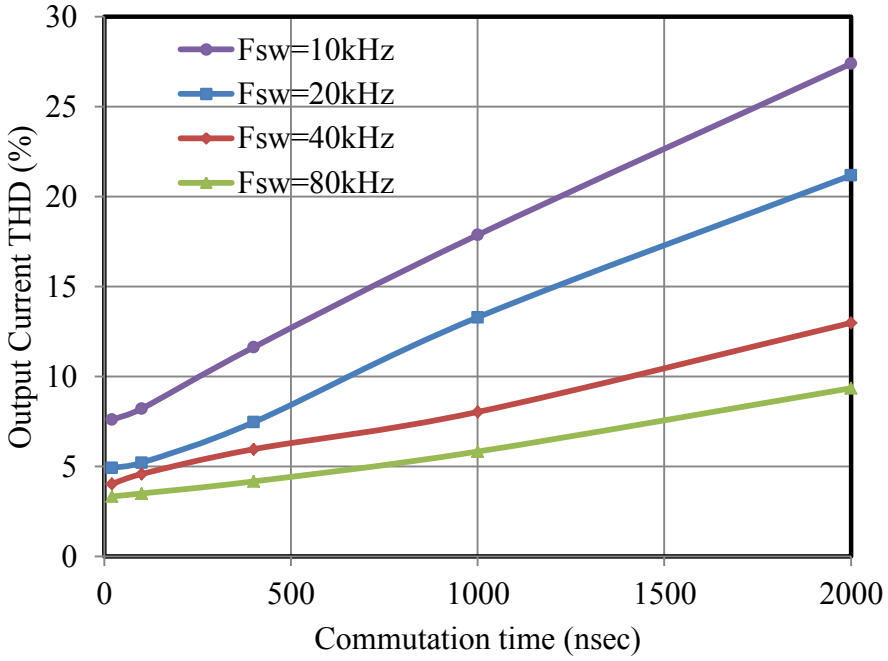



Figure 7.14: THD of the measured output current in various switching frequencies and commutation times

Furthermore, Figure 7.15 presents third harmonic of output voltage value for different switching frequency of matrix converter as the commutation time is varied. It can be noted that the value of third harmonic voltage is effectively increased by increasing the value of commutation time and the effect is more distinct under high switching frequency. Thus commutation time has to be zero in high switching matrix converter in order to obtain suitable performance in terms of output waveform quality.

As demonstrated, the commutation time is a very important issue in high frequency matrix converter and minimization of commutation process for high switching frequency matrix converter and using three-step current commutation is essential. Thus applying three-step current commutation

strategy gives the matrix converter superior waveform quality in high switching frequency.

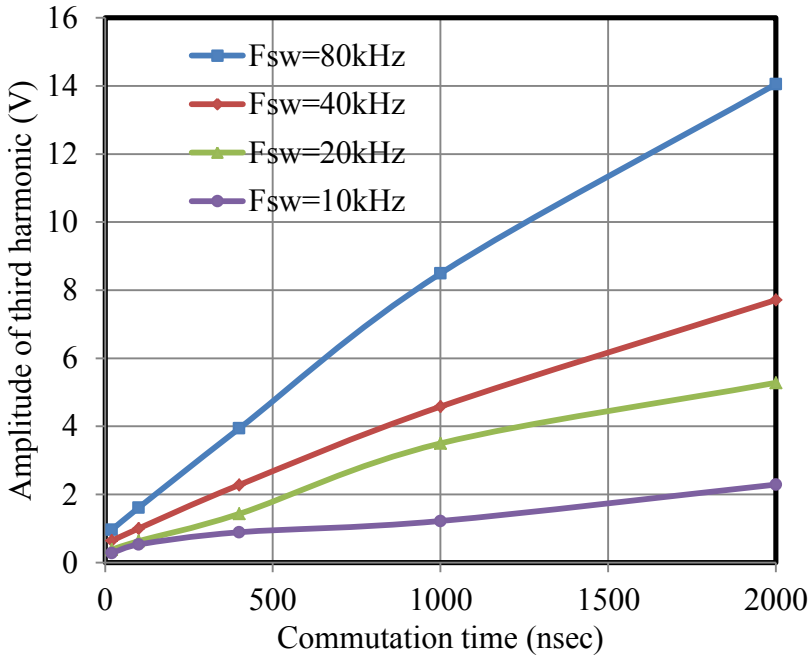



Figure 7.15: Third harmonic of the measured output voltage in various switching frequencies and commutation times

## 7.2 Influence of Parasitic Inductance

As it has been revealed the SiC power devices hold the promise of faster switching speed compared to Si power devices, which lead to superior converter performance in terms of power loss and efficiency. However, the ultimate achievable switching speed is determined not only by internal semiconductor device physics, but also by circuit parasitic elements. Therefore, analysing the effect of circuit parasitic is necessary to accurately predict switching losses and actual switching waveforms, including overshoot and ringing. The relative importance of circuit parasitic is increased as the switching speed of SiC power devices is increased.

# Chapter 7: Challenges of SiC Power Devices

Parasitic elements such as parasitic inductances and parasitic capacitances can be associated with practically every physical component in the power converter, including the power semiconductor devices, sensors, capacitors, inductors, PCB traces and connectors. The switching behaviour is primarily affected by semiconductor device parasitic capacitances and circuit layout parasitic inductances. A parasitic inductance in series with a semiconductor power device stores energy when current flows through it. When the device turn off, the stored energy in the parasitic inductance needs to be discharged and a voltage spike rated at *Ldi/dt* is added to the off state voltage of the device, which increases the voltage stress of the device. The effects of the parasitic inductances will be worse at higher frequencies, given the higher *di/dt*, limiting the maximum operating switching frequency of power devices. To optimize the performance of power converter, the parasitic inductance should be reduced as much as possible.

As the SiC MOSFET has the highest switching speed compared with the other available SiC power devices, it is chosen for this part of the study. So the objective of this section is to carry out a comprehensive investigation into the effect of parasitic inductance on the SiC MOSFET switching performance in matrix converter. A detailed model of the SiC MOSFET bidirectional switch which is employed in the 2-phase to 1-phase matrix converter and switch an inductive load current are derived. The analytical switching waveforms under the influence of the parasitic inductance are illustrated to visualize their effects. Then the analytical study is further verified by comparison with parametric study of test bench in terms of switching loss and device stresses.

### 7.2.1 Analytical Modelling of SiC MOSFET Switching Characteristics Due to Parasitic Inductance

A basic matrix converter circuit including two SiC MOSFET bidirectional switches is used in modelling of SiC MOSFET switching characteristics for investigating the effect of parasitic inductance. A circuit diagram of the 2-phase to 1-phase matrix converter for switching transient analysis is shown in Figure 7.16. Voltage $V_{IN}$ as the converter input voltage is equal $V_A$ - $V_B$, while the load current is represented as a constant current $I_L$. In analysing the circuit, two different commutation scenarios which are associated with the hard turn-on and turn-off the SiC MOSFET are considered and presented in the following section.

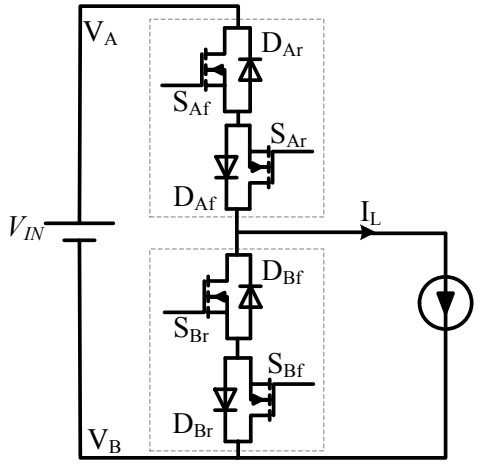



Figure 7.16: Circuit diagram of the 2-phase to 1-phase matrix converter

#### 7.2.1.1 Hard Turn-on Switching

To investigate the influence of the parasitic inductance on the hard turn-on switching behaviour of the SiC MOSFET in matrix converter, the following

commutation scenario is considered. The output voltage is changed from the input phase B to input phase A when the output current direction is positive and the incoming input voltage is more positive than the outgoing input voltage which means $V_{IN}$ is positive.

Equivalent circuit diagram of the commutation leg is presented in Figure 7.17. The input voltage supply is modelled as an ideal voltage source $V_{IN}$ with a parasitic inductance $L_{IN}$. The $S_{Ar}$ and $S_{Br}$ are switched off during commutation time, and are completely neglected in the analysis. The $S_{Bf}$ is permanently switched on, and as that, modelled as a resistor which is equal to drain-source on-state resistance ($R_{ds\text{-}on}$) of SiC MOSFET. The blocking diode of the SiC MOSFET $S_{Bf}$ is represented by an equivalent freewheel diode, $D_{Bf}$. The SiC MOSFET $S_{Af}$ in phase A is actively controlled device, and as that it has been represented by a small signal model. The model is composed of the current source $I_{dA}$ and device parasitic capacitances $C_{gd}$, $C_{gs}$ and $C_{ds}$. The SiC MOSFET interconnection and PCB trace inductance are denoted by $L_g$, $L_s$ and $L_d$ which are gate inductance, source inductance and drain inductance respectively. The parasitic inductance of the diode is lumped into the parasitic inductance $L_s$.

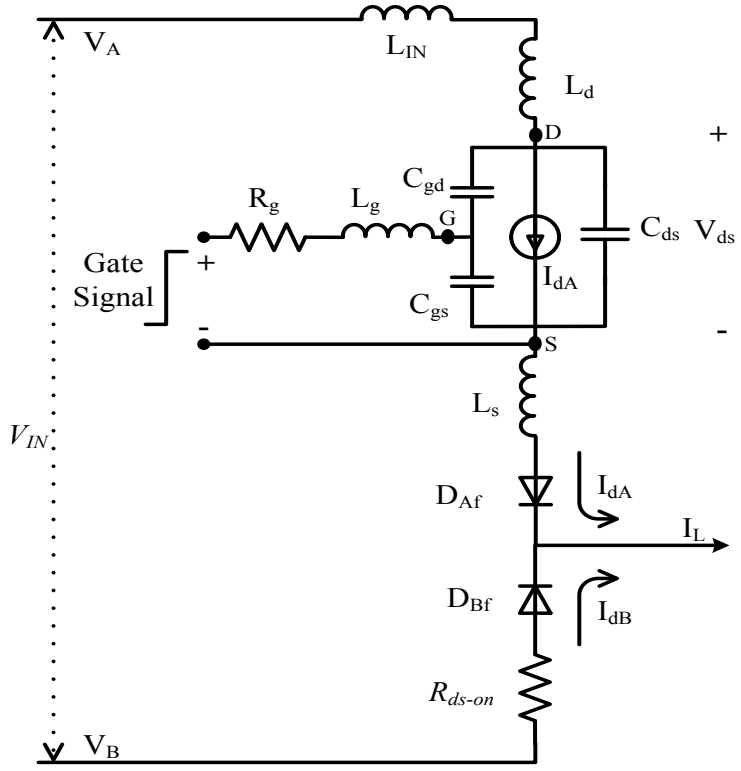



Figure 7.17: Equivalent circuit diagram of the commutation leg

It is assumed that the $S_{Af}$ is off and the $S_{Bf}$ is on and conducting the entire load current. Once the turn-on gate signal is applied, the load current commutes from $S_{Bf}$ to $S_{Af}$. This commutation scenario is well known as a hard turn-on switching. Relevant waveforms of entire turn-on switching process are depicted in Figure 7.18 and it can be divided into three stages. In the first stage, the gate-source voltage $V_{gs}$ of the $S_{Af}$ switch is equal to the negative gate supply voltage, $V_{EE}$. The turn-on gate signal is applied at the moment $t_{0on}$, and the gate-source voltage $V_{gs}$ begins to rise. Since the gate-source voltage is below the threshold voltage $V_{th}$, the drain current $I_{dA}$ remains zero. The stage two of process begins at the moment $t_{1on}$ when the gate-source voltage, $V_{gs}$, reaches the threshold voltage and the channel of the SiC MOSFET begins to

conduct current. As a result, the drain current of the SiC MOSFET, $I_{dA}$, begins to rise with a slope $(dI_{dA}/dt)_{on}$. The phase B still remains forward biased and conduct a part of the load current. By neglecting the voltage drop across $S_{Bf}$, $D_{Bf}$ and $D_{Af}$, the drain-source voltage of the SiC MOSFET ($S_{Af}$), $v_{ds}$ during this period can be given by:

$$v_{ds} = V_{IN} - L_{IN}\frac{dI_{dA}}{dt} - L_d\frac{dI_{dA}}{dt} - L_s\frac{dI_{dA}}{dt} \qquad (7.12)$$

The total commutation inductance ($L_{IN}$ + $L_d$ +$L_s$) and fast increase of the drain current generate an initial inductive voltage drop which is caused by rapid decrease in the drain-source voltage. The value of the voltage drop on the drain-source voltage of the SiC MOSFET can be calculated by:

$$\Delta V_{drop} = L_{IN}\frac{dI_{dA}}{dt} + L_d\frac{dI_{dA}}{dt} + L_s\frac{dI_{dA}}{dt} = L_P\frac{dI_{dA}}{dt} \qquad (7.13)$$

where $L_P$ is the total parasitic inductance of the current path.

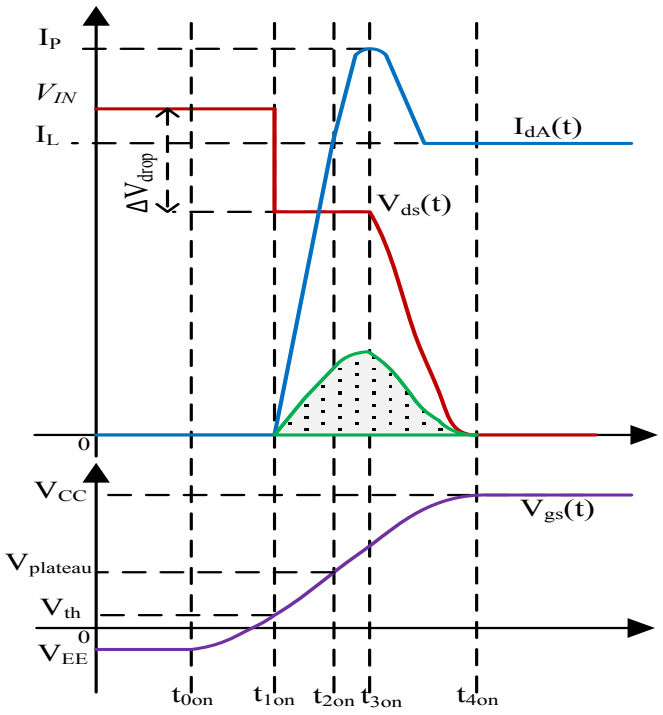



Figure 7.18: Switching waveforms of the SiC MOSFET during turn-on

At the moment $t_{3on}$ which third stage begins, the diode of the phase B ($D_{Bf}$) begins to block. The reverse recovery current of $D_{Bf}$ falls to zero and diode voltage builds up. This results in rapid decrease of the drain-source voltage of the SiC MOSFET. Then, the drain current of the $S_{Af}$ SiC MOSFET remains constant.

Based on the linearized analytical turn-on waveform of the SiC MOSFET, the following equations are derived for calculating the turn-on energy loss of the SiC MOSFET. It should be noted that the time interval between $t_{1on}$ and $t_{3on}$ is named $t_{13on}$ and time interval between $t_{3on}$ and $t_{4on}$ is named $t_{34on}$ in following description. The time interval $t_{13on}$ is related with peak load current and current rising rate. So it can be expressed by:

$$t_{13on} = \frac{I_P}{\left(\frac{dI_{dA}}{dt}\right)_{on}} \quad (7.14)$$

where $I_P$ is the peak of current during the turn-on switching. The instantaneous current passing through the SiC MOSFET, $i_d$, and the corresponding instantaneous voltage across the SiC MOSFET, $v_{ds}$, during time interval $t_{13on}$ respectively can be expressed by:

$$i_{d-13on} = \left(\frac{dI_{dA}}{dt}\right)_{on} t \quad (7.15)$$

$$v_{ds-13on} = V_{IN} - L_P \left(\frac{dI_{dA}}{dt}\right)_{on} \quad (7.16)$$

In addition, the time interval $t_{23on}$ can be determined from the SiC MOSFET drain-source voltage and the decreasing ratio of it, so it can be written by:

$$t_{34on} = \frac{V_{IN} - L_p\left(\frac{dI_{dA}}{dt}\right)_{on}}{\left(\frac{dv_{ds}}{dt}\right)_{on}} \quad (7.17)$$

The instantaneous current passing through the SiC MOSFET and the corresponding instantaneous voltage across the SiC MOSFET during time interval $t_{34on}$ respectively can be expressed by:

$$i_{ds34on} = \left(-\frac{I_P - I_L}{t_{34on}}\right) t + I_P \quad (7.18)$$

$$v_{ds34on} = \left(\frac{dv_{ds}}{dt}\right)_{on} t + V_{IN} - L_P \left(\frac{dI_{dA}}{dt}\right)_{on} \quad (7.19)$$

By substituting these equations in the energy loss equation which is expressed by:

$$E = \int_0^t v(t) i(t) dt \quad (7.20)$$

The turn-on energy loss of the SiC MOSFET for whole interval of turn-on process can be calculated by:

$$E_{sw-on} = \frac{1}{2}\left(V_{IN} - L_P\left(\frac{dI_{dA}}{dt}\right)_{on}\right)\frac{I_P^2}{\left(\frac{dI_{dA}}{dt}\right)_{on}} + \frac{\left(V_{IN} - L_P\left(\frac{dI_{dA}}{dt}\right)_{on}\right)^2}{\left(\frac{dv_{ds}}{dt}\right)_{on}}\left(\frac{1}{3}I_P - \frac{1}{6}I_L\right)$$

(7.21)

It can be noted from the equation (7.21) that the switching energy loss is decreased by increasing the parasitic inductance of the circuit and the rising rate of the SiC MOSFET current and voltage.

#### 7.2.1.2 Hard Turn-off Switching

The hard turn-off switching is of particular concern since over voltage due to the parasitic inductance may exceed the SiC MOSFET's blocking voltage and damage the device. So it is important to understand the mechanism of the hard turn-off switching of the SiC MOSFET in the matrix converter.

The following commutation scenario is considered to investigate the influence of the parasitic inductance on the hard turn-off switching behaviour of the SiC MOSFET in matrix converter. The output voltage is changed from the input phase A to input phase B when the output current direction is positive and the outgoing input voltage is more positive than the incoming input voltage which means $V_{IN}$ is positive.

The equivalent circuit diagram of the commutation leg for the hard turn-off switching of the SiC MOSFET is the same as the hard turn-on switching of the SiC MOSFET which was presented in Figure 7.17.

It is assumed that the $S_{Af}$ is on and conducting the entire load current and the $S_{Bf}$ is become on but due to $V_A$ is more than $V_B$, the diode $D_{Bf}$ is reverse biased and it cannot conduct until the $S_{AF}$ is become off and load current transfers. Figure 7.19 presents the relevant waveforms of the entire SiC MOSFET turn-off switching process and it could be divided into three stages.

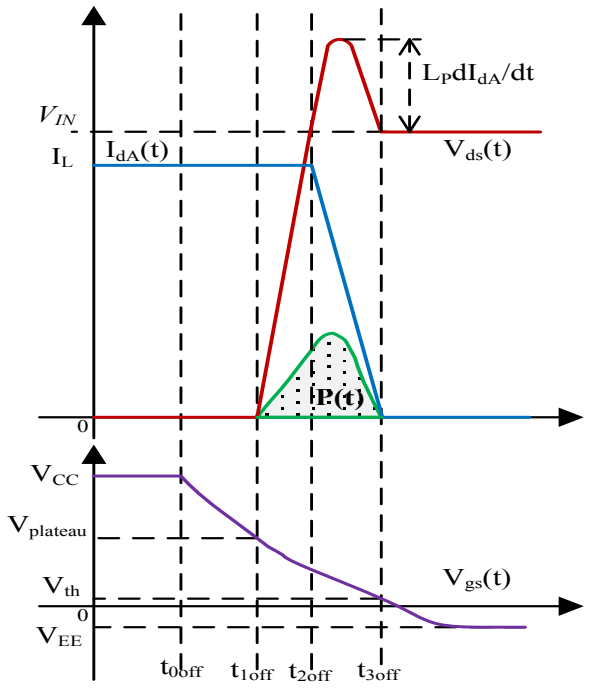



Figure 7.19: Switching waveforms of the SiC MOSFET during turn-off

In the first stage, the gate-source voltage $V_{gs}$ of the SiC MOSFET $S_{Af}$ is equal to the positive gate supply voltage $V_{CC}$. The turn-off gate signal is applied at the moment $t_{0off}$, and the gate-source voltage $V_{gs}$ begins to decrease and reach a value which is named plateau voltage $V_{plateau}$ but the SiC MOSFET is still completely on and it handles the entire load current. Then the stage two of process begins at the moment $t_{1off}$ when the gate-source voltage $V_{gs}$ decreases and reaches the threshold voltage and the drain-source voltage of the

SiC MOSFET begins to rise and reaches to $V_{IN}$ but still the SiC MOSFET is conducting.

At the moment $t_{2off}$ that third stage begins, the diode of the phase B, $D_{Bf}$ ceases blocking voltage and current begins to divert from the phase A to the phase B of matrix converter. This stage will extend until the drain current becomes zero and $V_{gs}$ reaches $V_{th}$. Also at the same time, the drain-source voltage of the SiC MOSFET, $V_{ds}$, keeps increasing because of the decreasing of drain current and parasitic inductance and then turns to the input voltage when the drain current reaches to zero. The same analytical method and parameters used at the turn-on transients can be used for determining the drain-source voltage of the SiC MOSFET in this stage as presented by:

$$V_{ds} = V_{IN} - L_{IN}\frac{dI_{dA}}{dt} - L_d\frac{dI_{dA}}{dt} - L_s\frac{dI_{dA}}{dt} \tag{7.22}$$

As the decreasing drain current will induce a voltage drop across the parasitic inductances, which will incur an extra stress on the SiC MOSFET, a voltage overshoot $\Delta V_{os}$ is expected to appear in $V_{ds}$ which is determined by:

$$\Delta V_{os} = L_{IN}\left(\frac{dI_{dA}}{dt}\right)_{off} + L_d\left(\frac{dI_{dA}}{dt}\right)_{off} + L_s\left(\frac{dI_{dA}}{dt}\right)_{off} = L_P\left(\frac{dI_{dA}}{dt}\right)_{off} \tag{7.23}$$

After the load current flow entirely through the phase B of the matrix converter, $V_{gs}$ reduces from $V_{th}$ to zero and the SiC MOSFET $S_{Af}$ is turned off completely. Eventually, the voltage overshoot in the power stage is damped by the parasitic resistance of the circuit.

It can be noted that the turn-off switching transients are a reversely symmetrical process of the turn-on switching transients. Based on the

linearized analytical turn-off waveform of the SiC MOSFET, the following equations are derived for calculating the turn-off energy loss of the SiC MOSFET. It should be noted that the time interval between $t_{1off}$ and $t_{2off}$ is named $t_{12off}$ and time interval between $t_{2off}$ and $t_{3off}$ is named $t_{23off}$ in following description. The time interval $t_{12off}$ is related to the input voltage, $V_{IN}$, and the drain-source voltage rising rate of the SiC MOSFET,$\left(\frac{dv_{ds}}{dt}\right)_{off}$. So it can be expressed as:

$$t_{12off} = \frac{V_{IN}}{\left(\frac{dv_{ds}}{dt}\right)_{off}} \tag{7.24}$$

The instantaneous current passing through the SiC MOSFET, $i_d$, and the corresponding instantaneous voltage across the SiC MOSFET, $v_{ds}$, during time interval $t_{12off}$ respectively can be presented by:

$$i_{d12off} = I_{dA} \tag{7.25}$$

$$v_{ds12off} = \left(\frac{dv_{ds}}{dt}\right)_{off} t \tag{7.26}$$

Furthermore, the time interval $t_{23off}$ can be determined based on the load current and the rate of decreasing drain current of the SiC MOSFET $S_{Af}$ as presented by:

$$t_{23off} = \frac{I_{dA}}{\left(\frac{dI_{dA}}{dt}\right)_{off}} \tag{7.27}$$

The instantaneous SiC MOSFET drain current and drain-source voltage during the time interval $t_{23off}$ respectively can be represented by:

$$i_{d23off} = \left(\frac{dI_{dA}}{dt}\right)_{off} t + I_{dA} \tag{7.28}$$

$$v_{ds12off} = \begin{cases} \frac{2L_P\left(\frac{dI_{dA}}{dt}\right)_{off}}{t_{23off}} t + V_{IN} & \left(0 \le t \le \frac{t_{23off}}{2}\right) \\ -\frac{2L_P\left(\frac{dI_{dA}}{dt}\right)_{off}}{t_{23off}} t + 2L_P\left(\frac{dI_{dA}}{dt}\right)_{off} + V_{IN} & \left(\frac{t_{23off}}{2} \le t \le t_{23off}\right) \end{cases} \tag{7.29}$$

By substituting these equations in the energy loss equation which was expressed using equation (7.20), the turn-off energy loss of the SiC MOSFET for whole interval of turn-off process can be calculated by:

$$E_{sw-off} = \frac{1}{2}\left(\frac{dv_{ds}}{dt}\right)_{off} I_{dA} t_{12off}^2 + \left(V_{IN} + \frac{1}{2}L_P\left(\frac{dI_{dA}}{dt}\right)_{off}\right)\left(I_{dA} t_{23off} + \frac{1}{2}\left(\frac{dI_{dA}}{dt}\right)_{off} t_{23off}^2\right) \tag{7.30}$$

It can be noted from the equation (7.30) that the parasitic inductances can significantly influence device stresses and switching energy loss.

### 7.2.2 Inductance Parasitic of PCB Trace

Estimation of the existing parasitic inductance of PCB traces in the PCB power circuit is required before doing experimental investigation. The effective parasitic inductance of the PCB trace can be determined by [117]:

$$L_t = 2l\left(\ln\left(\frac{2l}{w+\varepsilon}\right) + 0.5 + 0.2235\left(\frac{w+\varepsilon}{l}\right)\right) \quad nH \tag{7.31}$$

where $l$ is the length of trace in cm, $w$ is the width of trace in cm and $\varepsilon$ is the thickness in cm of trace on PCB board.

In order to verify the accuracy of equation (7.31), a test is performed using 2-phase to 1-phase matrix converter which is based on the switching loop resonance. The inductor in the switching loop resonance is the total series parasitic inductance and the capacitor is the drain-source capacitance of the SiC MOSFET. The oscillation in the $V_{ds}$ during turn-off switching is a result of the resonance between the drain-source capacitance, $C_{ds}$, illustrated in Figure 7.17 and the switching loop trace parasitic inductance, $L_p$. The oscillation frequency of the turn-off waveform can be obtained using an oscilloscope and the drain-source capacitance value of the SiC MOSFET form the datasheet of the power semiconductor device. The relationship between the oscillation frequency with the capacitor and inductor can be given by:

$$f_{osc} = \frac{1}{2\pi\sqrt{L_p C_{ds}}} \tag{7.32}$$

By substituting the value of capacitor and oscillation frequency in equation (7.32) the value of the total parasitic inductance can be determined. The measured oscillation frequency in the test bench and the drain-source capacitance of the SiC MSOFET at voltage 300 V are 37.31 MHz and 71.1 pF respectively, therefore, the value of the parasitic inductance which is determined by equation (7.32) is 259 nH. While by using equation (7.31) the calculated switching loop trace parasitic inductance is 286 nH. These results correspond to a percent difference of less than 9.4%, which indicates that equation (7.31) is a good approximation for any trace parasitic inductance calculation.

### 7.2.3 Experimental and Analytical Evaluation

Experiments have been done to verify analytical description and quantify the effect of parasitic inductance on the switching behaviour of SiC power devices in the matrix converter. The experiments have been done by the implemented 2-phase to 1-phase SiC MOSFET matrix converter. To vary the value of the inductance in the experiment, external inductances are added across the device terminals to emulate the bigger values. Therefore, the current path in the test circuit has been broken at several points, so small inductances can be inserted into the paths. Air-core coils are used to make the small inductances which are needed to insert in the current path. With 4 turns, 7 turns and 11 turns air core coil, it is possible to obtain respectively the corresponding inductances of 62 nH, 108 nH and 178 nH. The gate driver has been designed and placed as close electrically as possible to minimize the potential resonance from the gate loop inductance.

Figure 7.20 and Figure 7.21 displays the experimental turn-on drain-source voltage and drain current waveforms of SiC MOSFET under the influence of the parasitic inductance respectively. It is obvious that the voltage drop across the drain-source of SiC MOSFET during the turn-on switching has been increased by increasing parasitic inductance. Thus increasing parasitic inductance can decrease turn-on switching energy loss of power semiconductor device.

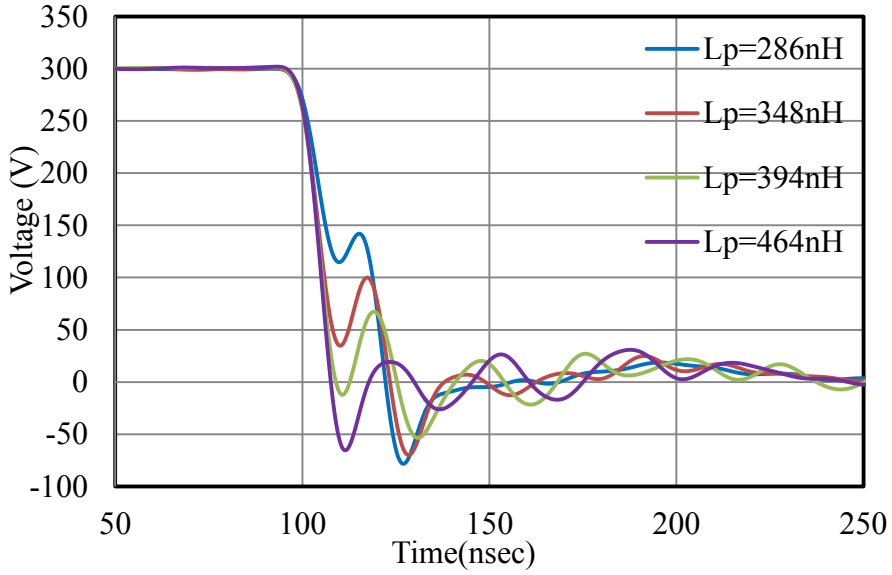



Figure 7.20: Experimental turn-on voltage switching waveform of SiC MOSFET at 300V and 12A for various values of parasitic inductance

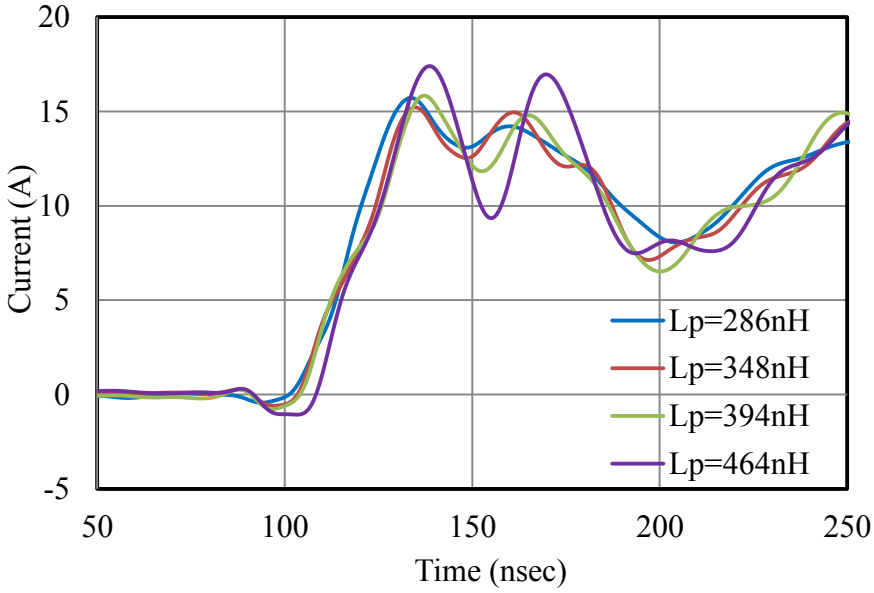



Figure 7.21: Experimental turn-on current switching waveforms of SiC MOSFET at 300V and 12A for various values of parasitic inductance

Furthermore, the experimental turn-off drain-source voltage and drain current waveforms of SiC MOSFET respectively under the influence of parasitic inductance are shown in Figure 7.22 and Figure 7.23. It can be noted

that the voltage overshoot across the SiC MOSFET during the turn-off switching has been increased by increasing source parasitic inductance significantly, thus by increasing parasitic inductance, the turn-off switching energy loss of power semiconductor device is increased.

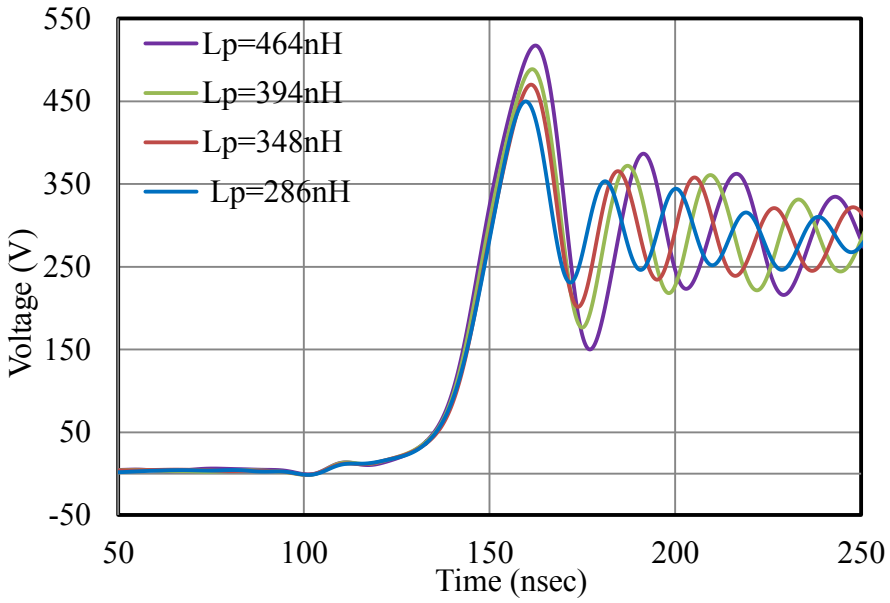



Figure 7.22: Experimental turn-off voltage switching waveform of the SiC MOSFET at 300V and 12A for various values of parasitic inductance

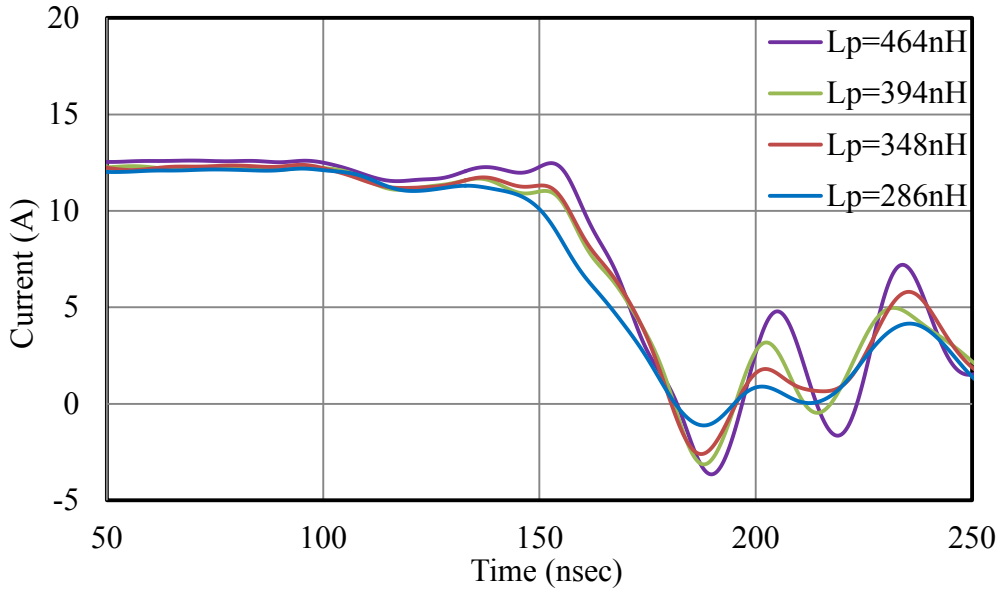



Figure 7.23: Experimental turn-off current switching waveforms of the SiC MOSFET at 300V and 12A for various values of parasitic inductance

To quantify the effects of the parasitic inductance and validate the analytical description about the switching energies, a parametric study has also been conducted. Based on the measured waveforms of the SiC MOSFET switching, the parameters which are required for calculating turn on and off switching energies by (7.21) and (7.30) are extracted and the switching energies are determined. Also switching energies have been obtained experimentally based on the method which is explained in Appendix C. Figure 7. 24 and 7.25 shows the parasitic inductance impact on the turn-off and turn-on switching energies analytically and experimentally. It is obvious that turn-off switching energy has been increased by increasing parasitic inductance of the circuit. But turn-on switching energy has been decreased by increasing parasitic inductance of the circuit. It is also clear that there is no significant difference between analytical and experimental results, so it can be concluded that the developed

equations for determining the switching energies is accurate and can be used for future works.

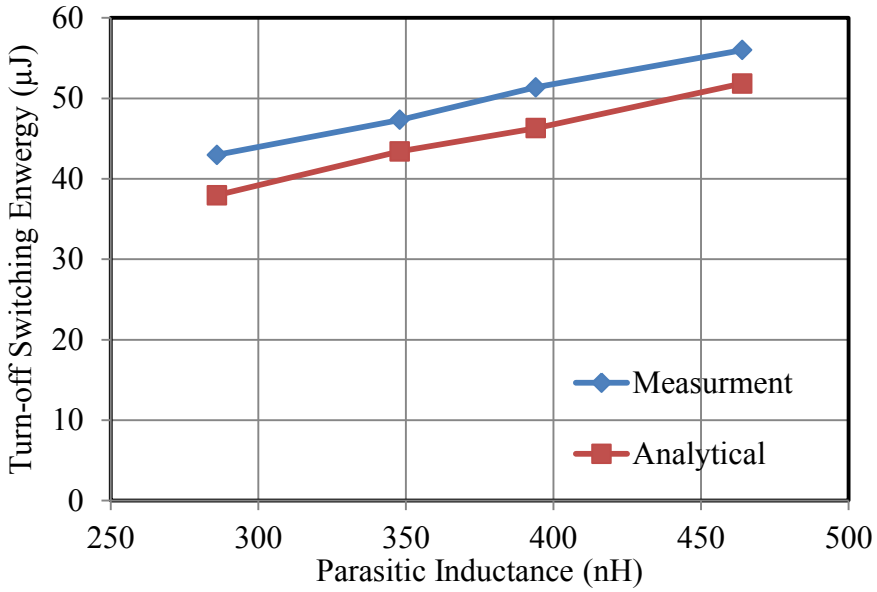



Figure 7. 24: Measured and analytical turn-off switching energy of the SiC MOSFET versus parasitic inductances. Turn-off switching of SiC MOSFET at 300V and 12A

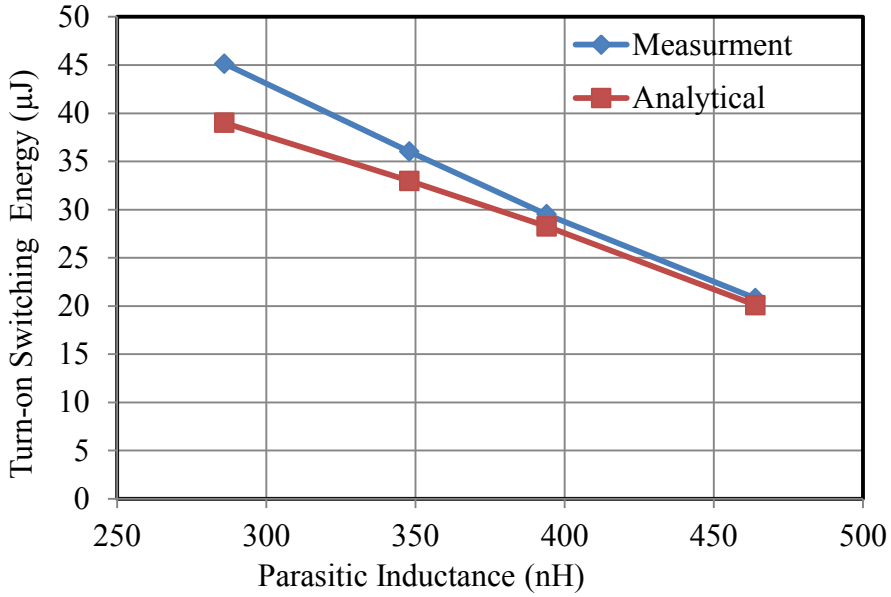



Figure 7. 25: Measured and analytical turn-on switching energy of the SiC MOSFET versus parasitic inductances. Turn-on switching of SiC MOSFET at 300V and 12A

## 7.3 Summary

The potential benefits that SiC power semiconductor devices can offer such as high temperature, high switching frequency and low power losses cannot be realised unless the whole power converter is optimised. Two of the important issues which require consideration in utilizing SiC power devices in matrix converter are output waveform distortion and influence of parasitic inductance.

In this Chapter, the cause of output waveform distortion in high switching frequency SiC matrix converter has been addressed. It has been shown that the effect of commutation time is significant on distortion of the output waveform quality when switching frequency of converter is more than 10 kHz. Thus commutation time value has to be minimizing as it is possible to reduce distortion in output waveforms. It has been shown that by applying the three-step current commutation strategy instead of four-step current commutation strategy, the output waveform distortion of the matrix converter can be avoided; giving the matrix converter superior waveform quality in high switching frequency range.

Furthermore, the influence of the parasitic inductance on the SiC power device switching behaviour, device stress and switching energy in matrix converter have been studied analytically and experimentally. It has been shown that the switching loop inductance is the major contributor to the parasitic ringing and overall stress of the device. Through the use of an optimal layout, the benefits of SiC power devices technology are further enhanced, providing additional efficiency gains and higher voltage operation capability.

# Chapter 8
# Conclusion and Future Work

This chapter presents the conclusions drawn for the work presented in this thesis and some ideas for related future research topics.

## 8.1 Conclusions

The circuit topology of matrix converters inherently provides more opportunity for higher power per volume densities. The use of new wide band gap power semiconductor devices, like those based on SiC, for different power converter applications is becoming more prevalent, mainly due to advantages realized at the system level when compared to conventional Si devices. The low switching losses allowing operation at high switching frequencies and the higher operating temperature of SiC devices allow for an increase in the power density of the power converter. As power converters with higher volumetric

densities are being pursued in some applications, matrix converter based on SiC semiconductor devices can provide a viable solution to exceed the current power density limits for AC/AC power conversion.

For these applications it is important to understand how SiC devices are different from the conventional Si devices and the effect these differences have on the design and performance of a matrix converter. Therefore research has been carried out to investigate the impact of SiC device technologies on matrix converter design and performance to achieve a design with high efficient and high power density.

In order to fully utilize the high speed switching capabilities of emerging semiconductor devices, specific gate drive circuits have been designed and implemented in this work. A simple 2-phase to 1-phase prototype matrix converter was constructed using different Si and SiC power devices. These circuits were used to analyse the commutation phenomena, parasitic inductance effects and performance of the input filter.

This thesis has also described the development of a method to evaluate the conduction and switching losses and performance for different Si and SiC power devices in the matrix converter circuit. Based on the extracted data for the chosen devices, losses for the circuit with a range of Si and SiC devices are calculated over a range of switching frequencies and operating temperatures. The SiC JFET matrix converter provides the lowest power losses, particularly if higher switching frequencies are used. It has been shown that using SiC power devices, the matrix converter power loss could be significantly lower compared to Si power devices at the same switching frequency and

temperature. So it can be concluded that the application of SiC power devices could increase the matrix converter power density, not only by reducing input filter size but also by reducing the cooling system requirements.

A design procedure for the matrix converter input filter has been proposed in order to fulfil power quality standard requirements and minimize the filter volume. The impact of the switching frequency on the filter cut-off frequency has been considered and it has been shown that a higher switching frequency will lead to a smaller input filter and can increase the power density of the converter. However, there is a trade-off between the input filter volume and power losses in the converter in given switching frequency.

The output waveform distortion due to commutation time in high switching frequency SiC matrix converters has been studied. It has been shown that the commutation time has a significant effect on the output waveform quality. Therefore the commutation delay has to be minimizing to reduce the distortion in output waveforms. It has been shown that by applying a three-step current commutation strategy, the output waveform distortion can be minimised, giving the matrix converter good waveform quality even with high switching frequencies.

Finally in this work, the influence of parasitic inductance on the behaviour of SiC power MOSFET in matrix converters has been studied. It has been shown that the switching loop inductance was the major contributor to the parasitic ringing and overall voltage stress on the semiconductor devices. Through the use of an optimal layout the benefits of SiC power devices

technology can be enhanced, providing additional efficiency gains and higher voltage operation capability.

## 8.2 Future Work

In order to fully illustrate the benefits of utilizing SiC power devices in the matrix converter, future work can be carried out in the following directions.

By utilizing SiC power devices and increasing switching frequency of power converter, EMI emission will become an important issue. An investigation and characterization of the EMI signature of SiC matrix converters, EMI filter structure and design as well as the filter behaviour at high frequencies is needed.

The capability of SiC power devices for operation at very high value of junction temperature can reduce size and expenditure of matrix converter cooling system. Regarding such a possibility, it is necessary to investigate and compare the thermal runaway of different SiC power devices and evaluate the relation between the maximum current loading and maximum junction temperature to avoid thermal runaway.

## 8.3 List of Publications

The work described in this thesis has resulted in the following journal and conference papers being published.

### 8.3.1 Journal Paper

1) **S. Safari**, A. Castellazzi, and P. Wheeler, "Experimental and Analytical Performance Evaluation of SiC Power Devices in the Matrix Converter," *Power Electronics, IEEE Transactions on,* vol. 29, pp. 2584-2596, 2014.

### 8.3.2 Conference Papers

2) **S. Safari**, A. Castellazzi, and P. Wheeler, " Impact of Switching Frequency on Input Filter Design for High Power Density Matrix Converter," in *Energy Conversion Congress and Exposition (ECCE), 2014 IEEE*, 2014.

3) **S. Safari**, A. Castellazzi, and P. Wheeler, "Influence of commutation delay on waveform distortion in high frequency SiC Matrix Converter," in *Power Electronics, Machines and Drives (PEMD 2014), 7th IET International Conference on*, 2014, pp. 1-6.

4) E. Zacharis, A. M. Cross, B. Godfrey, **S. Safari**, A. Castellazzi, P. Ward, and I. Mosely, "High efficiency SiC AC chopper for LV networks," in *Power Electronics, Machines and Drives (PEMD 2014), 7th IET International Conference on*, 2014, pp. 1-6.

5) **S. Safari**, A. Castellazzi, and P. Wheeler, "Performance evaluation of normaly-off SiC JFET in matrix converter without antiparrallel diodes," in *Industrial Electronics Society, IECON 2013 - 39th Annual Conference of the IEEE*, 2013, pp. 1815-1820.

6) **S. Safari**, A. Castellazzi, and P. Wheeler, "Comparative performance evaluation of SiC power devices for high temperature and high frequency matrix converter," in *Energy Conversion Congress and Exposition (ECCE), 2013 IEEE*, 2013, pp. 956-962.

7) **S. Safari**, A. Castellazzi, and P. Wheeler, "Experimental study of parasitic inductance influence on SiC MOSFET switching performance in Matrix converter," in *Power Electronics and Applications (EPE), 2013 15th European Conference on*, 2013, pp. 1-9.

8) **S. Safari**, A. Castellazzi, and P. Wheeler, "Performance evaluation of bidirectional SiC switch devices within Matrix converter," in *Power Electronics and Applications (EPE), 2013 15th European Conference on*, 2013, pp. 1-9.

9) **S. Safari**, A. Castellazzi, and P. Wheeler, "Evaluation of SiC power devices for a high power density matrix converter," in *Energy Conversion Congress and Exposition (ECCE), 2012 IEEE*, 2012, pp. 3934-3941.

10) **S. Safari**, A. Castellazzi, and P. Wheeler, "Evaluation of normally-off SiC JFET for a high power density matrix converter," in *Power Electronics and Motion Control Conference (EPE/PEMC), 2012 15th International*, 2012, pp. DS1a.9-1-DS1a.9-7.

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# Appendix A
# Lists of Acronyms and Symbols

## List of Acronyms

| | |
|---|---|
| Si | Silicon |
| Silicon carbide | SiC |
| IGBT | Insulated gate bipolar transistor |
| MOSFET | Metal-oxide-semiconductor field-effect transistor |
| JFET | Junction field effect transistor |
| BJT | Bipolar junction transistor |
| SBD | Schottky barrier diode |
| RB-IGBT | Reverse blocking IGBT |
| DMOSFET | Depletion MOSFET |
| T&FS | Trench and field-stop |
| JBS | Junction barrier schottky |
| PT | Punch-through |
| NPT | Non punch-through |
| THD | Total harmonic distortion |
| rms | Root mean square |
| PWM | Pulse width nodulation |
| DSP | Digital signal processor |
| FPGA | Field programmable gate array |
| DSK | DSP start kit |
| CCS | Code composer studio |
| IDE | Integrated development environment |
| PCB | Print circuit board |
| PCC | Point of common coupling |
| IPC | Interconnecting and packaging electronic circuits |
| EMC | Electromagnetic compatibility |
| EMI | Electromagnetic interface |

# Appendix A: List of Symbols

## List of Symbols

| | |
|---|---|
| $\omega_o$ | Frequency of the output voltage |
| $\omega_i$ | Frequency of the input voltage |
| $f_{sw}$ | Switching frequency |
| $f_s$ | Frequency of the supply voltage |
| $f_{out}$ | Frequency of the output voltage |
| $f_c$ | Cut-off frequency of the filter |
| $f_{ocs}$ | Oscillation frequency of a LC circuit |
| $Att_{req}$ | Required attenuation of the filter |
| $\omega_c$ | Cut-off frequency |
| $\xi$ | Damping factor |
| $T_{seq}$ | Period of the switching |
| $T_{ch}$ | Charging time |
| $f_{osc}$ | Oscillation frequency |
| $V_A$, $V_B$, $V_C$ | Three phase input voltages |
| $V_a$, $V_b$, $V_c$ | Three output line-to-supply neutral voltages |
| $V_s$ | Supply voltage |
| $V_i$ | Magnitude of input voltage vector |
| $V_o$ | Magnitude of output voltage vector |
| $V_R$ | Reference voltage |
| $V_{max}$ | Maximum permissible clamp voltage |
| $V_{int}$ | Initial voltage of the clamp capacitor |
| $V_{i\text{-}ll}$ | rms amplitude of the line-to-line input voltage |
| $\Delta V_{Lf}$ | Voltage drop across filter inductor |
| $V_{IN}$ | DC input voltage |
| $\Delta V_{drop}$ | Voltage drop due to parasitic inductance |
| $V_{os}$ | Voltage overshoot due to parasitic inductance |
| $V_{th}$ | Threshold voltage |
| $V_{ce}$ | Collector-to-emitter voltage of the IGBT or BJT |
| $V_{ce\text{-}sat}$ | Collector-to-emitter saturation voltage |
| $V_{ds}$ | Drain-to-source voltage of the MOSFET or JFET |
| $V_{diode}$ | Voltage across the diode |
| $V_F$ | Forward voltage drop across the diode |
| $V_{gs}$ | Gate-to-source voltage of the MOSFET or JFET |
| $V_{ge}$ | Gate-to-emitter voltage of the IGBT |
| $V_{be}$ | Base-to-emitter voltage of the BJT |
| $V_{be\text{-}sat}$ | Base-to-emitter saturation voltage |
| $V_{plateau}$ | Plateau voltage |
| $V_{cc}$ | Positive voltage of the driver |
| $V_{EE}$ | Negative voltage of the driver |
| $V_o$ | Positive output voltage of the driver |
| $I_L$ | Output Current |
| $i_A$, $i_B$, $i_C$ | Three phase input currents |
| $i_a$, $i_b$, $i_c$ | Three phase output currents |
| $I_i$ | Magnitude of input current vector |

# Appendix A: List of Symbols

| | |
|---|---|
| $I_o$ | Magnitude of output current vector |
| $I_R$ | Reference current |
| $I_s$ | Supply current |
| $\hat{I}$ | Amplitude of the over load current |
| $I_1$ | Amplitude of the fundamental harmonic of current |
| $I_h$ | Amplitude of h harmonic of current |
| $I_{HF}$ | Amplitude of switching frequency harmonic of current |
| $I_{sc}$ | Maximum short circuit current at PCC |
| $I_c$ | Collector current of the IGBT or BJT |
| $I_d$ | Drain current of the MOSFET or JFET |
| $I_F$ | Forward current of diode |
| $I_{rr}$ | Reverse recovery current of diode |
| $I_g$ | Gate current of the IGBT, MOSFET or JFET |
| $I_b$ | Base current of the BJT |
| $I_{bp}$ | Peak base current of the BJT |
| $I_p$ | Peak of current during the turn-on switching |
| $\varphi_i$ | Displacement angle of input currents with respect to input voltages |
| $\alpha_0$ | The direction of the reference output voltage vector |
| $\tilde{\alpha}_0$ | The angle of the reference output vector within the sector |
| $\beta_i$ | The direction of the reference input current vector |
| $\tilde{\beta}_i$ | The angle of the reference input vector within the sector |
| $q$ | Voltage transfer ratio |
| $d_I$, $d_{II}$, $d_{III}$, $d_{IV}$ | Duty cycles of the four active switch configurations |
| $t_I$, $t_{II}$, $t_{III}$, $t_{IV}$, $t_{01}$, $t_{02}$, $t_{03}$ | Time interval of the switching configuration |
| $t_{d1}$,$t_c$,$t_{d3}$ | Gap time of the commutation sequence |
| $t_{on}$ | Turned-on switching time for the power device |
| $t_{off}$ | Turned-off switching time for the power device |
| $t_{rr}$ | Reverse recovery time for the diode |
| $t_r$ | Rise time of the power device |
| $t_f$ | Fall time of the power device |
| $C_{clamp}$ | Clamp capacitor |
| $R_{clamp}$ | Clamp resistor |
| $L_f$ | Input filter inductor |
| $C_f$ | Input filter capacitor |
| $R_f$ | Input filter damped resistor |
| $L_L$ | Load inductor |
| $L_{IN}$ | Input parasitic inductor |
| $L_d$ | Drain parasitic inductor |
| $L_s$ | Source parasitic inductor |
| $L_g$ | Gate parasitic inductance |
| $L_p$ | Parasitic inductor |
| $L_t$ | Parasitic inductance of PCB trace |
| $R_L$ | Load resistor |
| $R_{ce}$ | On-state resistance of the IGBT or BJT |
| $R_{ds}$ | On-state forward resistance of the MOSFET or JFET |
| $R_{sd}$ | On-state reverse resistance of the MOSFET or JFET |

# Appendix A: List of Symbols

| | |
|---|---|
| $R_{diode}$ | On-state resistance of the diode |
| $R_c$ | Charge pump resistor |
| $C_c$ | Charge pump capacitor |
| $R_g$ | Gate resistor |
| $R_b$ | Base resistor |
| $C_{gd}$ | Gate to drain capacitance of the MOSFET |
| $C_{gs}$ | Gate to source capacitance of the MOSFET |
| $C_{ds}$ | Drain to source capacitance of the MOSFET |
| $W_L$ | Maximum energy stored in the load inductor |
| $W_C$ | Maximum absorbed energy by the clamp capacitor |
| $P_{con}$ | Conduction power loss |
| $P_{sw}$ | Switching power loss |
| $P_{drive}$ | Drive power loss |
| $P_{out}$ | Rated output power |
| $E_{on}$ | Turn-on switching energy of the power device |
| $E_{off}$ | Turn-off switching energy of the power device |
| $T$ | temperature |
| $\Delta T$ | Temperature increase |
| $A$ | Cross sectional area of copper |
| $\varepsilon$ | PCB copper thickness |
| $w$ | Track width |
| $\Delta e_{cd}$ | Voltage-time product error |

# Appendix B
# PCB Layers

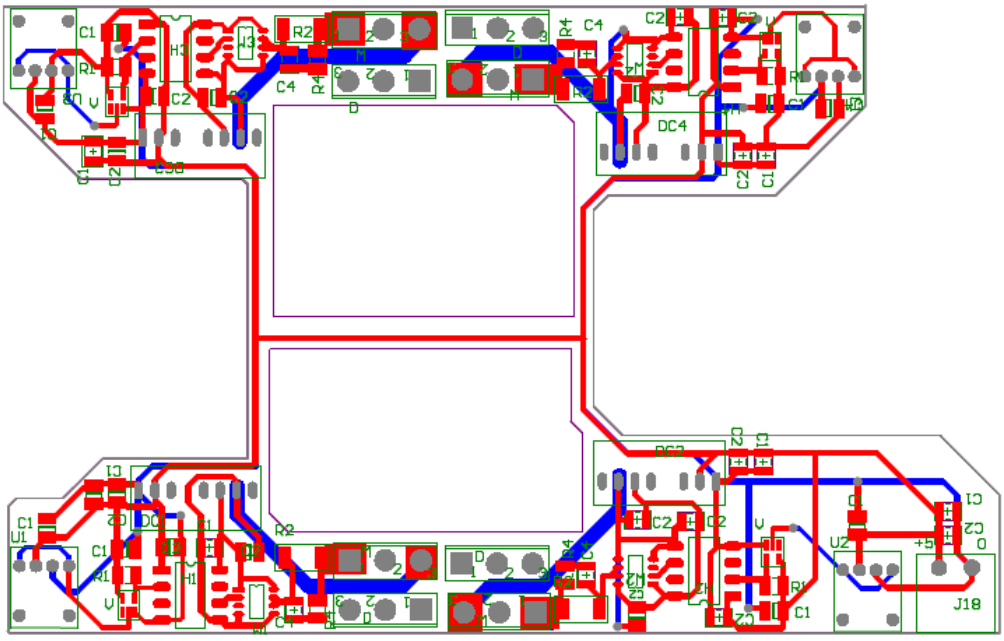

Figure B.1: Drive circuit PCB for the SiC BJT

# Appendix B: PCB Layers

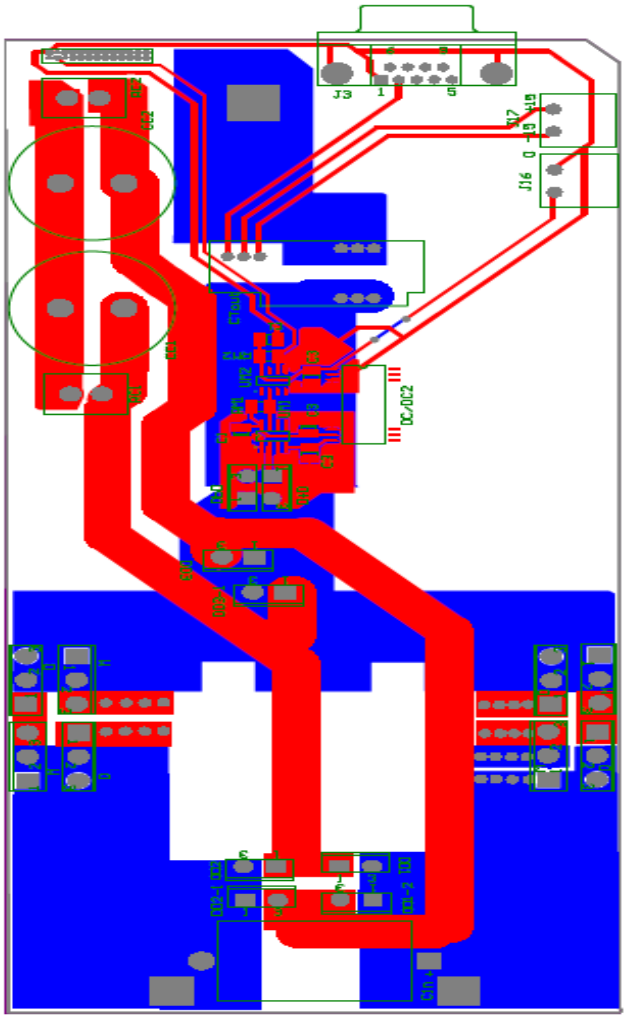

Figure B.2: Power circuit PCB for the 2-phase to 1-phase matrix converter

# Appendix C
# Switching Energy Calculation Approach

A calculation approach is necessary to determine the energy lost during switching transient in a power device based on the measured switching waveforms. In this section, the approach used to estimate and validate the switching energy of a power device is explained. For this study, a Si IGBT-diode (IKW15N120), a SiC MOSFET (CMF10120D) and a SiC diode (C4D20120D) have been considered to calculate the switching energies and then compare them with the datasheet values for the validation of the approach.

The ideal waveforms for a hard turn-on and off switching are shown in Figure C.1. For instance, the energy lost during the switching transient in an IGBT can be calculated by the integration of the instantaneous power waveform which is obtained by multiplying the IGBT collector–emitter

voltage waveform ($v_{ce}$) with the collector current waveform ($i_c$) of IGBT as expressed by:

$$E_{on\ or\ off} = \int_{t_{on1}or\ t_{off1}}^{t_{on2}\ or\ t_{off2}} v_{ce}(t) i_c(t) dt \qquad \text{(C.1)}$$

where $t_{on1}$ is defined as the time when the current has reached 10% of its load value and $t_{on2}$ is the time when the voltage falls to 2% of the blocking voltage value. Additionally, the $t_{off1}$ is defined as the time when the voltage rise to 10% of the blocking voltage value and $t_{off2}$ is the time when the current falls to 2% of its load value. This procedure is also used in [118].

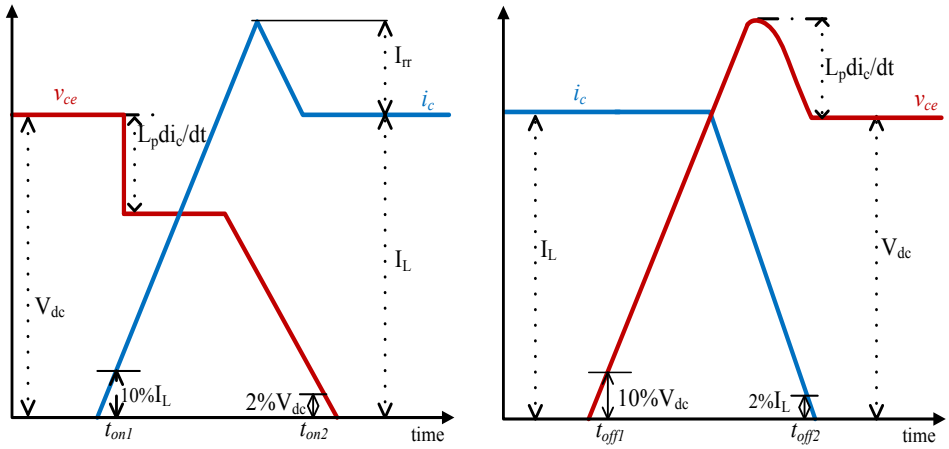


Figure C.1: Simplified switching waveforms of the IGBTs

The validation and comparison of the derived expression for determining the switching energies with the given switching energies of the device on the datasheet were studied by computing the switching loss energies.

# Appendix C: Switching Energy Calculation Approach

## Si IGBT

The switching energies of the Si IGBT on the datasheet have been determined at 600V when device temperature is 175°C. The switching waveforms of the Si IGBT have been measured when the voltage is 600V at a temperature of 130°C which is the closest possible operating point in our lab setup to the datasheet value. Figure C.2 shows the turn-on switching waveform of the Si IGBT in the circuit of the 2-phase to 1-phase matrix converter when the voltage and current are 600V and 4.5A at a temperature of 130°C respectively. Based on the equation (C.1), the Si IGBT turn-on switching energy has been calculated offline by importing the data and processing them in MATLAB. The calculated turn-on switching energy from the measured switching waveforms and the obtained turn-on switching energy from the datasheet for the Si IGBT are listed in Table C.1.

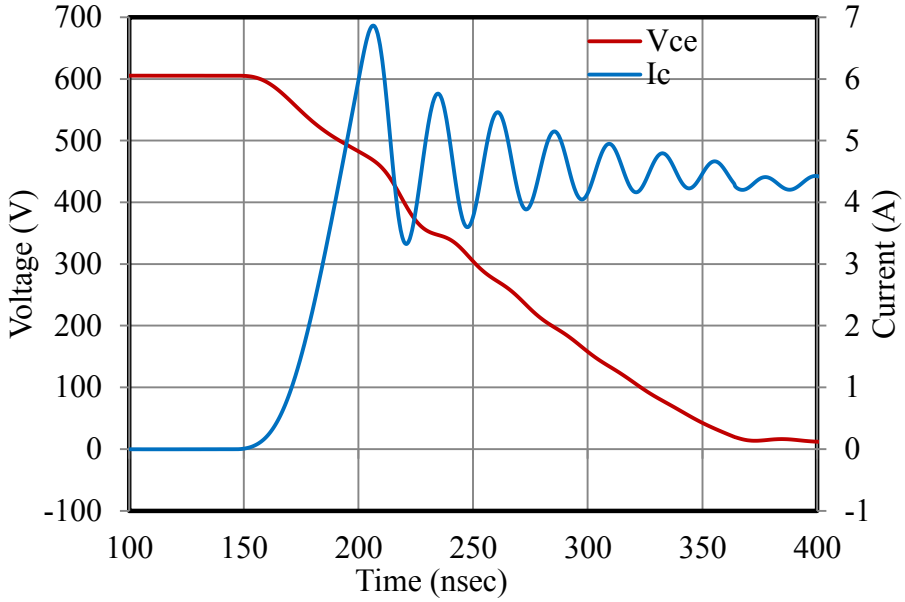


Figure C.2: Turn-on switching waveform of the Si IGBT at the temperature of 130°C

# Appendix C: Switching Energy Calculation Approach

| Test Condition | Turn on switching Energy | |
|---|---|---|
| | Value(μJ) | difference |
| $V_{ce}$=600V, $I_c$=4.5A, T=175°C from datasheet | 435.2 | |
| $V_{ce}$=600V, $I_c$=4.5A, T=130°C from measurement | 281.373 | 35.34% |

Table C.1: Calculated turn-on switching energy from the measurement and the obtained turn-on switching energy from the Si IGBT datasheet

It can be seen from Figure C.2 that there is about 100V voltage dip across the collector-emitter of the IGBT during the rising of the collector current when the device is switched on. This voltage dip which is about 16.66% of the blocking voltage may be due to the parasitic inductance of the circuit and results in reduction of the measured turn-on switching energy of the IGBT in comparison with the corresponding datasheet value. It can be seen from Table C.1, that the difference between the measured turn-on switching energy and the one obtained from the device datasheet is 35.34% which is higher than the 16.66% reduction in voltage due to parasitic inductance. It should also be noted that the remaining difference between the turn-on energies of the device may be due to different operating temperature. It is worth to mention that based on the IGBT datasheet information rate of increasing turn-on and off switching energy over temperature are 2.80μJ/°C and 2.85μJ/°C respectively, so it can be stated that by increasing temperature, the measured turn-on switching energy also is increased.

# Appendix C: Switching Energy Calculation Approach

The turn-off switching waveform of the Si IGBT in the circuit of the 2-phase to 1-phase matrix converter when the voltage and current are 600V and 5.3A at a temperature of 130°C is shown in Figure C.3. The current is higher because of ripple which decreases the turn-on current and increase the turn-off current. Based on the equation (C.1), the Si IGBT turn-off switching energy has been calculated. The calculated turn-off switching energy from the measured waveform and the obtained turn-off switching energy from the datasheet are listed in Table C.2. It can be seen form Table C.2 that there is no significant difference between the turn-off switching energies whereas the operating temperature of them is different. The reason for this is that because of higher parasitic inductance of the circuit, there is 10% voltage overshoot across the collector-emitter of the Si IGBT which increases the measured turn-off switching energy of the device in comparison with the datasheet value. Thus, it can be expected that at the operating temperature equal to the datasheet, the measured turn-off switching energy will be more than the datasheet value of the turn-off switching energy.

# Appendix C: Switching Energy Calculation Approach

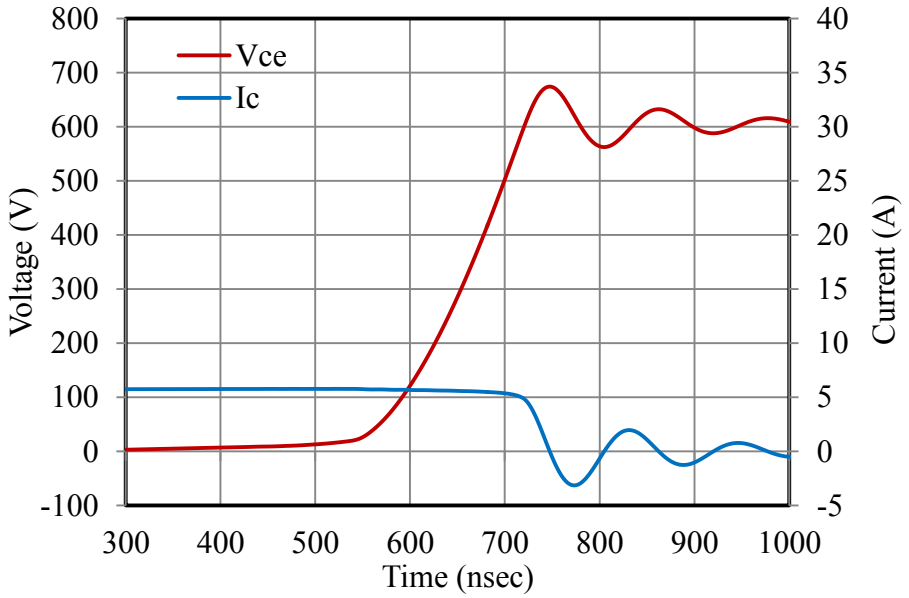


Figure C.3: Turn-off switching waveform of the Si IGBT at the temperature of 130°C

| Test Condition | Turn off switching Energy | |
|---|---|---|
| | Value(μJ) | difference |
| $V_{ce}$=600V, $I_c$=5.3A, T=175°C from datasheet | 317.4 | |
| $V_{ce}$=600V, $I_c$=5.3A, T=130°C from measurement | 303.70 | 4.31% |

Table C.2: Calculated turn-off switching energies from measurement and obtained switching energies from datasheet for the Si IGBT

It can be concluded that due to higher parasitic inductance and temperature being lower than specified in the datasheet, the measured turn-on switching energy is lower in comparison with the datasheet turn-on switching energy. However, the higher parasitic inductance caused the higher turn-off switching energy compared to the datasheet turn-off switching energy.

# Appendix C: Switching Energy Calculation Approach

## SiC MOSFET

The switching energies on the datasheet of the SiC MOSFET are provided for the switching voltage of 800V at a temperature of 25°C. The measurement of the SiC MOSFET switching waveforms in the circuit of the 2-phase to 1-phase matrix converter has been done at the voltage of 800V and temperature of 25°C. The turn-on switching waveform of the SiC MOSFET is shown in Figure C.4 when the voltage and current are 800V and 6.8A respectively at a temperature of 25°C. The SiC MOSFET turn-on switching energy has been determined based on the equation (C.1) which is presented in Table C.3.

It can be seen form Figure (C.4) that there is 209V voltage dip across the drain-source of the SiC MOSFET during the raising drain current when the device turns on. The voltage drop which is 26.12% of the blocking voltage is due to the parasitic inductance of the 2-phase to 1-phase matrix converter. It can also be seen from Table C.3 that the calculated turn-on switching energy from the measured waveform is 31.73% lower than the corresponding obtained value from the device datasheet. The main reason is the 26.12% lower voltage caused by the parasitic inductances of the circuits.

# Appendix C: Switching Energy Calculation Approach

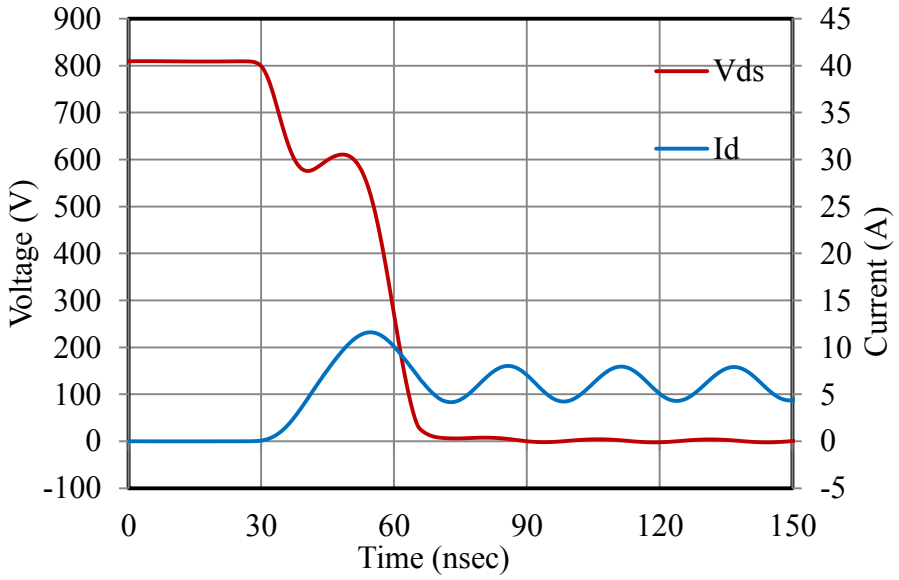


Figure C.4: Turn-on switching waveform of the SiC MOSFET at the temperature of 25°C

| Test Condition | Turn on switching Energy | |
|---|---|---|
| | Value(µJ) | difference |
| $V_{ds}$=800V, $I_d$=6.8A, T=25°C from datasheet | 87.28 | |
| $V_{ds}$=800V, $I_d$=6.8A, T=25°C from measurement | 59.58 | 31.73% |

Table C.3: Calculated turn-on switching energy from the measurement and obtained turn-on switching energy from datasheet for the SiC MOSFET

The turn-off switching waveform of the SiC MOSFET is shown in Figure C.5 when the voltage and current are 800V and 7.3A respectively at a temperature of 25°C. It is clear from Figure C.5 that there is an overshoot across the drain-source voltage of the SiC MOSFET during switching period which is 20.31% of the blocking voltage and is caused by the parasitic inductance of the circuit. The SiC MOSFET turn-off switching energy has been calculated based on the equation (C.1) which is presented in Table C.4.

# Appendix C: Switching Energy Calculation Approach

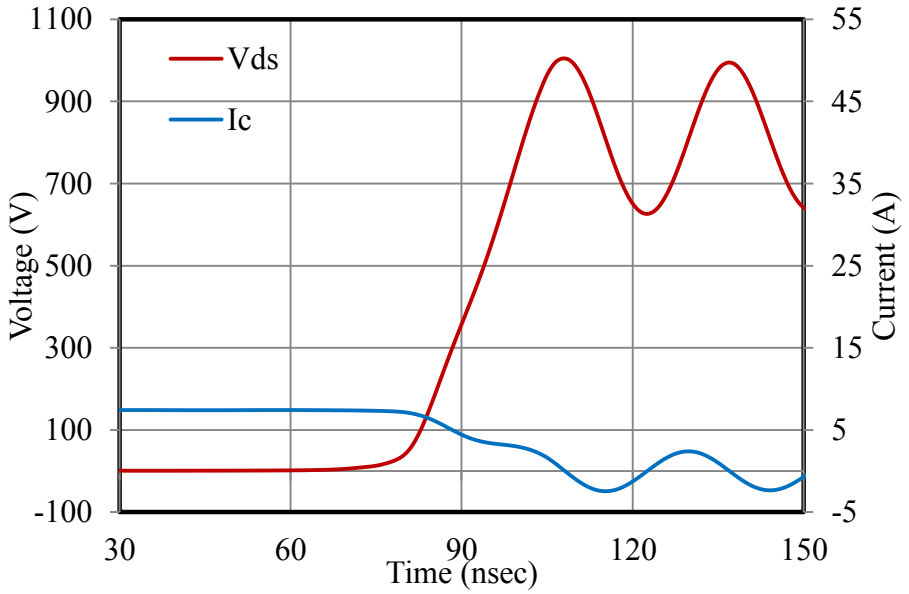


Figure C.5: Turn-off switching waveform of the SiC MOSFET at the temperature of 25°C

| Test Condition | Turn off switching Energy | |
|---|---|---|
| | Value(μJ) | difference |
| $V_{ds}$=800V, $I_d$=7.3A, T=25°C from datasheet | 110.27 | |
| $V_{ds}$=800V, $I_d$=7.3A, T=25°C from measurement | 128.087 | -16.15% |

Table C.4: Calculated switching energies from the measurement and the obtained switching energies from the datasheet for the SiC MOSFET

The measured turn-off switching energy of the SiC MOSFET is 16.15% more than the turn-off switching energy derived from the datasheet. This difference may be due to the difference between the parasitic inductances of the test circuits. The difference between the total measured switching energy and the one obtained from the datasheet is 4.86%, so it can be concluded that the calculated switching energies from the measured waveform can be reliably

used in the determination of the power losses of the converter and also that the used method for calculating switching energy is accurate.

## Diode Turn-off Switching Energy

The ideal waveform for a hard turn-off switching of a typical diode is shown in Figure C.6. The energy lost during the turn-off switching transient in a diode can be calculated by the integration of the instantaneous power waveform which is obtained by multiplying the diode voltage waveform ($v_{diode}$) with the diode current waveform ($i_{diode}$) expressed by:

$$E_{off} = \int_{t_{offd1}}^{t_{offd2}} v_{diode}(t) i_{diode}(t) dt \qquad \text{(C.2)}$$

where $t_{offd1}$ is defined as the time when the diode voltage has reached 10% of the diode reverse voltage, $V_r$, and $t_{offd2}$ is the time when the diode current falls to 2% of the reverse recovery current of the diode. This procedure is also used in [118].

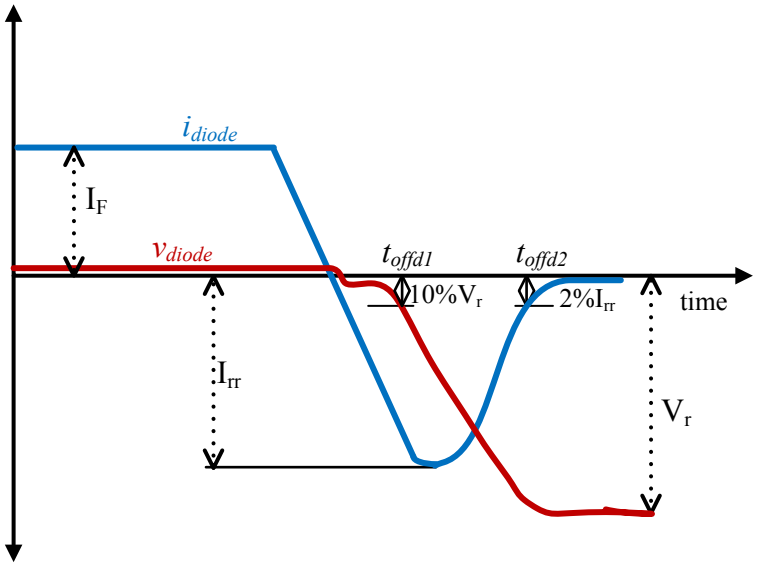


Figure C.6: Simplified turn-off switching waveform of the diode

As it has been stated in [119], due to some device manufacture only provide diode characteristic data, the turn-off switching energy of the diode can also be calculated based on the diode reverse voltage, $V_r$, and the diode reverse recovery charge, $Q_{rr}$ using following equation:

$$E_{off-diode} = V_r Q_{rr} \tag{C.3}$$

In the datasheet of the Si and SiC diodes which are used in this study only the diode characteristic data which are needed for calculating the diode turn-off switching energy are provided rather than a specified value for the diode turn-off switching energy. To calculate and validate the Si and SiC diodes turn-off switching energy, using equation (C.2) and the measured waveforms, the diodes turn-off switching energy is calculated and then compared with the determined diodes turn-off switching energy from the datasheet by the equation (C.3).

# Appendix C: Switching Energy Calculation Approach

The turn-off switching waveform of the Si diode in the circuit of the 2-phase to 1-phase matrix converter when the voltage and current are 600V and 14.77A at a temperature of 25°C is shown in Figure C.7. It can be seen from Figure C.7 that there is an overshoot on the Si diode current due to the reverse recovery effect. Also there is an overshoot across the Si diode voltage due to parasitic inductance of the circuit during turn-off transient. Based on the equation (C.2), the Si diode turn-off switching energy has been calculated. The calculated turn-off switching energy of Si diode from the measured waveform and the derived turn-off switching energy from the datasheet are listed in Table C.5.

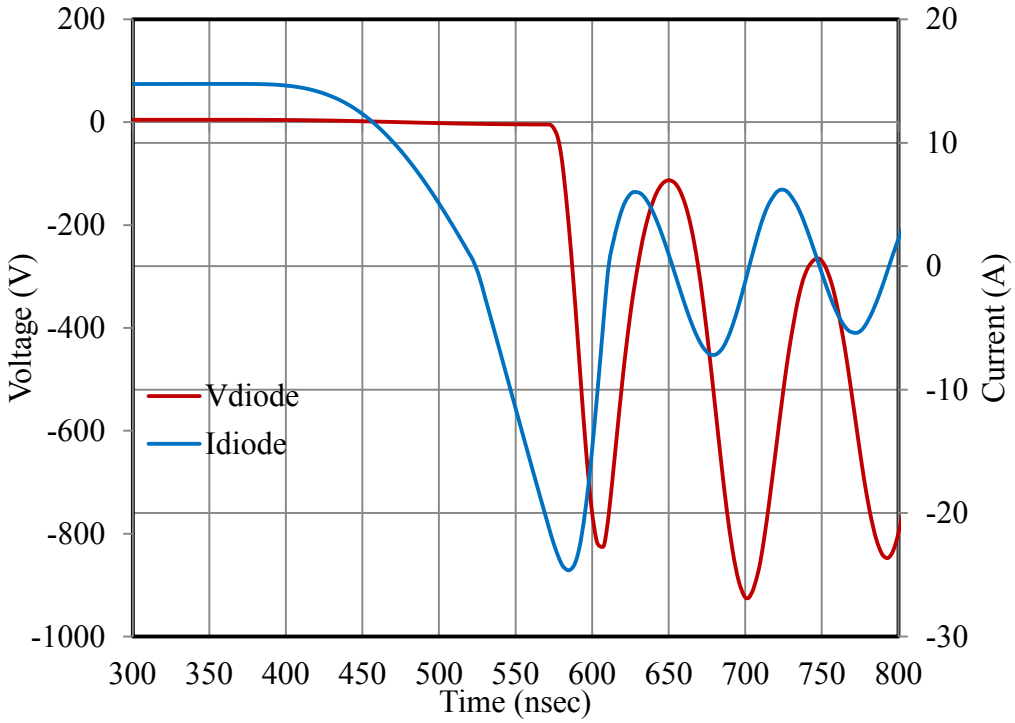


Figure C.7: Turn-off switching waveform of the Si diode at a temperature of 25°C

| Test Condition | Turn off switching Energy | |
|---|---|---|
| | Value(μJ) | difference |
| $V_r$=600V, $I_F$=15A, T=25°C from datasheet | 480 | |
| $V_r$=600V, $I_F$=14.77A, T=25°C from measurement | 538.26 | 12.13% |

Table C.5: Calculated switching energies from the measurement and the derived switching energies from the datasheet for the Si diode

It should be noted from Table C.5 that the measured turn-off switching energy of the Si diode is 12.13% more than the turn-off switching energy derived from the datasheet. This difference is due to the difference between the parasitic inductances of the test circuits which cause an overshoot on the turn-off voltage waveform.

The turn-off switching waveform of the SiC diode is shown in Figure C.8 when the voltage and current are 800V and 5.36A respectively at a temperature of 25°C. It is clear from Figure C.8 that the SiC diode has a very low reverse recovery time in comparison with the Si diode which results in significant reduction in the SiC diode turn-off switching energy. The SiC diode turn-off switching energy has been calculated based on the equation (C.2). The calculated turn-off switching energy of SiC diode from the measured waveform and the derived turn-off switching energy from the datasheet are listed in Table C.6.

It can be seen form Table C.6 that there is 20.18% difference between the datasheet and experimental values of the turn-off switching energies of the SiC

diode. Due to higher parasitic inductance of the circuit, there is 30% voltage overshoot across the anode-cathode of the SiC diode which increases the measured turn-off switching energy of the device in comparison with the datasheet value. But as the value of the SiC diode turn-off switching energy is much smaller in comparison with the switching energy of the active devices in the converter, it can be stated that using the datasheet turn-off energy of the SiC diode instead of the experimentally determined value which maybe depend on parasitic inductance will not affect significantly the converter power losses.

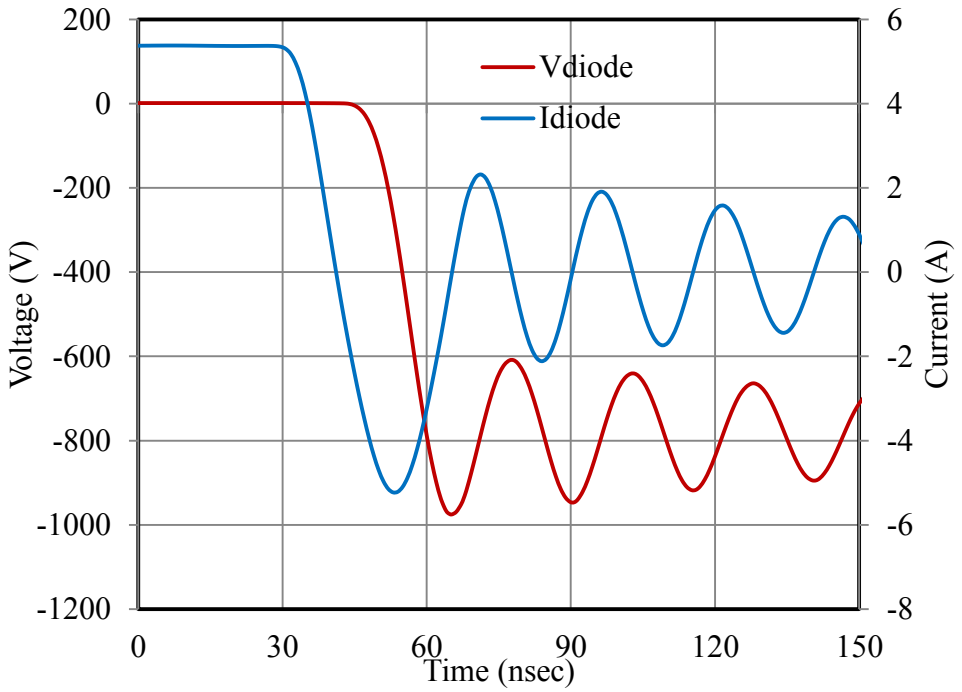


Figure C.8: Turn-off switching waveform of the SiC diode at a temperature of 25°C

| Test Condition | Turn off switching Energy | |
|---|---|---|
| | Value(μJ) | difference |
| $V_r$=800V, $I_F$=5A, T=25°C from datasheet | 21.60 | |
| $V_r$=800V, $I_F$=5.36A, T=25°C from measurement | 25.96 | 20.18% |

Table C.6: Calculated switching energies from the measurement and the derived switching energies from the datasheet for the SiC diode