Modulation Techniques for the Cascaded H-Bridge Multi-Level Converter

John Alan Vodden, MEng.

Thesis submitted to the University of Nottingham

for the degree of Doctor of Philosophy

July 2012

Abstract

This thesis investigates space-vector modulation and one-dimensional modulation applied to the cascaded H-bridge multi-level converter as a model for one port of the UNIFLEX-PM power converter system. The UNIFLEX-PM converter is a modular system including galvanic isolation at medium frequency intended to replace transformers in future distribution and transmission systems. Power converters in this application must produce good quality voltage waveforms with low power loss.

In this work, modulation methods are developed using theoretical analyses and simulation studies, before being verified experimentally using a low-voltage, laboratory-based power converter operating at the low switching frequencies applicable to high-power applications.

Using space-vector modulation, the relationship between the phase of the sampling process and the distortion of the line voltages is used to reduce the harmonic distortion of the output voltages. Different loads are attached to the cells of the cascaded H-bridge converter and limits are derived determining the range of loads for which it is possible to equalize the capacitor voltages. An algorithm which uses redundant states to balance the capacitor voltages without increasing the switching frequency is applied to space-vector modulation and one-dimensional modulation and its performance is compared to the derived limits.

The geometrical effect of capacitor voltage ripple on the space-vector diagram is used to derive the influence on the spectrum of the line-voltages. It is identified that second and fourth harmonics of the capacitor voltages contribute to fifth and seventh harmonics of the line voltages. A feed-forward scheme to compensate for the ripple of the capacitor voltage is derived and is shown to reduce the magnitude of un-wanted harmonics.

All the methods developed in this thesis can be applied to converters with any number of cells.

Acknowledgements

I would like to thank Professors Graham Holmes and Mark Sumner and Dr. Pericle Zanchetta for taking the time to examine this work. Thanks also to my supervisors Professors Pat Wheeler and Jon Clare for giving me opportunity to study and for their continued support throughout.

I would also like to thank the members of the PEMC group for their help and support. In particular, Dr. Alan Watson for his technical and moral support and for always being interested despite a heavy work-load.

Finally, thank you Michelle for you patience.

Contents

List of Symbols

Converter Components

C	Capacitance of the d.c. link
E	Nominal capacitor voltage (constant)
e_{xn}	Capacitor voltage in n^{th} cell of phase x (time varying)
L	Inductance on the a.c. side
N	The number of H-bridge cells per phase
R	Resistive load on the d.c. side
R_{ac}	Resistive component of a.c. circuit

Converter States and Outputs

d	Proportion of a sampling period to apply a given state
s_n	State of n^{th} cell, $n \in \{-1, 0, 1\}$
$s_{a,b,c}$	Sum of the states of the cells in each phase leg
$\hat{s}$	Modulation index
$u_{a,b,c}$	Supply voltage
v_{xn}	Output voltage of n^{th} cell of phase x
$\langle x \rangle$	Time-average of quantity x over a sampling period

Reference Frame Notation

In the following y can be replaced by output voltages, v, currents, i, switching states, s, supply voltages u or time averages of these quantities.

$y_{a,b,c}$	Three-phase quantities in natural co-ordinates
$\vec{y}$	Complex vector in stationary reference frame
$y_{\alpha,\beta}$	Components of three-phase vector in stationary frame
$y_{d,q}$	Components of three-phase vector in rotating frame
$y_{g,h}$	Components of three-phase vector in 60° skewed, space-vector co-ordinate system
θ	Angle of supply voltage vector
ω	Angular frequency of supply
$\Re(\vec{y})$	Real part of complex vector $\vec{y}$
$\Im(\vec{y})$	Imaginary part of complex vector $\vec{y}$

Notation Specific to Space-Vector Modulation

$\bar{S}(\vec{s})$	Mean of all the redundant states producing the switching vector $\vec{s}$
$\bar{s}_{a,b,c}$	Individual phase components of $\bar{S}$
S_l	State obtained by rounding the phase components of S towards $-\infty$
S_u	State obtained by rounding the phase components of S towards $+\infty$
$\vec{s}_{ul}$	State obtained by rounding the g and h components upwards and downwards respectively. Any combinations of u (upper) and l (lower) is possible

Miscellaneous Symbols

y^*	Demanded reference of quantity y
T_s	Sampling frequency
$\lfloor y \rfloor$	Floor function, rounds y towards $-\infty$
$\lceil y \rceil$	Ceil function, rounds y towards $+\infty$
$\mathrm{frac}(y)$	Fractional component of y
$\mathbb{Z}$	The set of integers

Chapter 1

Introduction

Grid-connected power-electronic converters are central to recent trends in the electrical generation, transmission and distribution industry. Should these trends continue into the future, power-electronic converters will become widespread, essential components of electricity networks.

There are several driving forces behind the increased interest in power electronics for such applications. First is the ever-increasing demand for electrical energy, fuelled in part by rising populations. Second is the strain placed on electrical networks by the increasing adoption of renewable energy sources, which are often intermittent and situated far from the load centres they supply. Finally, political and regulatory pressure to increase competition, to reduce the negative impact of power generation on the environment and to increase the diversity of primary energy sources [1] is leading to increased interest in *distributed generation.*

Figure 1.1 shows a conceptual structure of a conventional electricity network. Power is generated in bulk at centralized generating stations connected to the high voltage transmission network, which is a meshed network responsible for the bulk transmission of power from the generators to the distribution networks. The distribution networks are largely radial in nature and distribute power from the transmission network to many customer loads connected at different voltage levels depending on their power requirement. The greatest number of loads are residential and commercial properties connected at the

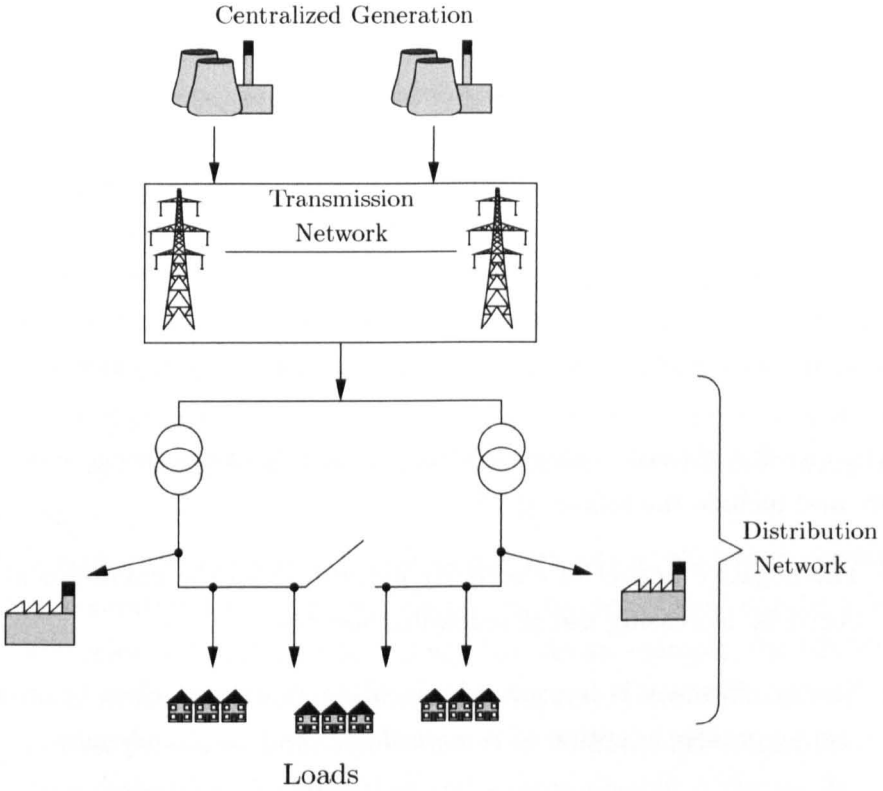


Figure 1.1: Conventional Structure of an Electricity Network

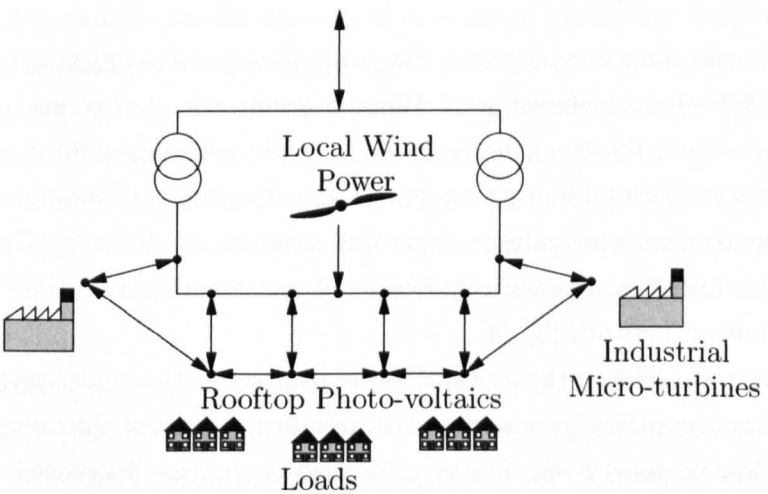


Figure 1.2: Distribution network including distributed generation

lowest voltage levels. The design and operation of the distribution network is targeted at delivery of power in one direction only: from the interconnection with the transmission network to the loads.

In contrast, a distributed generation system (Figure 1.2) contains many generation and storage facilities connected directly to the distribution network, including micro-generation at a domestic level and small-scale generation at commercial and industrial premises. The power demands of local loads are fed from generators in the same distribution network and if the generation within the local network exceeds the load power is injected back into the transmission network.

The benefits of small-scale generation are largely of a political or economic nature and include the following [2]:

- The negative impact of electricity generation on the environment is reduced by increasing use of renewable sources.
- Energy efficiency is improved by locating generation close to loads and also by greater adoption of *combined heat and power* schemes.
- Providers of small-scale generation can react more quickly to the market forces of modern electricity markets because of lower setup costs and a faster planning process.

Distributed generation satisfies the political objectives described above but comes with technical challenges. When customer loads become generators for some or all of the time, both the magnitude and direction of power flow in the network varies. Fault currents at the distribution level are increased by local generation and voltage control is made more difficult. Hence widespread distributed generation requires much more active, real-time control of the distribution network [3], [4].

Central to providing this control is the concept of the *smart grid*, which is a system incorporating greater levels of monitoring and sophisticated control over the flow of energy [4]. Smart grids also encompass increased use of energy storage media to compensate for intermittent renewable sources. Power-electronic converters are essential components of the smart-grid concept as

each distributed generation or storage facility requires a power electronic converter in order to interface with the grid [5], [6]. Furthermore, power-electronic converters allow unprecedented control over the flow of both real and reactive power allowing network infrastructure to be used more effectively and efficiently [7].

The smart-grid concept is a vision of how electrical networks may be deployed into the future. There is expected to be much less distinction between the parts of the network dedicated to transmission and those dedicated to distribution, with all parts of the network equipped to handle bidirectional power flow. Power-electronic converters will play an essential role in such networks by interfacing renewable sources, controlling power flow and improving power quality [8].

With such a wide range of applications for power electronic converters, there is a commercial need for flexible power converters that can be adapted to fit many roles and perform many functions. As an example, the UNIFLEX-PM project, which was a collaboration between several universities and industrial partners, presented a flexible structure for interfacing transmission and distribution systems with generation and energy storage in future European electricity networks [9].

The UNIFLEX-PM prototype is an example of a multi-level converter: a family of power-electronic converters capable of producing output voltages containing multiple discrete voltage steps. The multi-level output waveforms are high quality voltage waveforms with low harmonic distortion. By increasing the number of voltage steps, very high voltages can be reached without high voltage switching devices and without transformers [10], [11]. Hence, multi-level converters are well suited to grid-connected applications and have been described as an *enabling technology* for higher power applications of power electronics [12].

A simplified representation of the UNIFLEX-PM converter is shown in Figure 1.3. Each port is an example of a cascaded H-bridge multi-level converter, consisting of several full-bridge inverter circuits (or *H-bridges*) connected in series. The ports are connected together via isolated d.c. to d.c. converters and the whole converter can be controlled to transfer power in any direction

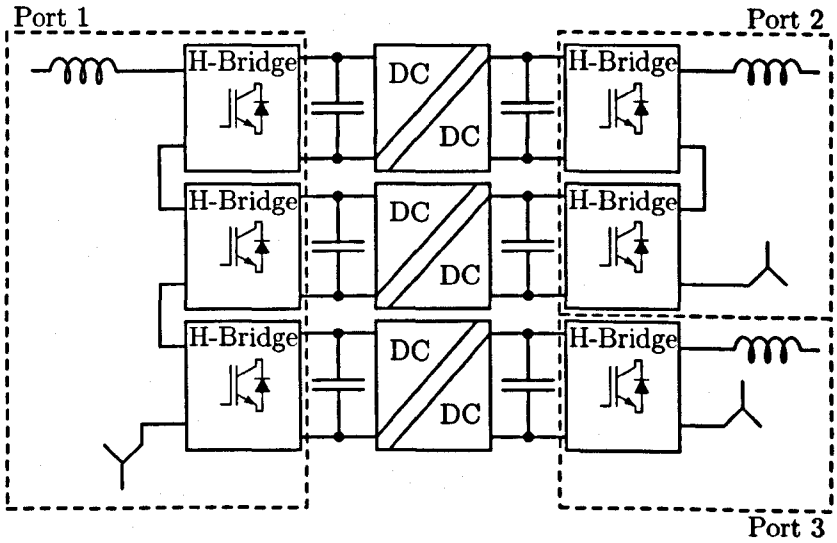


Figure 1.3: Single-Phase Representation of UNIFLEX-PM Converter in a Three-Port Configuration

between the ports. An example application of a three-port configuration is to interface two a.c. systems connected to ports one and two with an energy storage system connected to the third port. A key feature of the UNIFLEX-PM converter, in contrast to most applications of the cascaded H-bridge converter, is that the individual cells in each port can be connected to different systems so may be required to deliver different amounts of power.

Instead of studying the complete UNIFLEX-PM structure, the work in this thesis focusses on a three-phase cascaded H-bridge converter (Figure 1.4), which is intended to represent a single port of the UNIFLEX-PM converter. In the rectifying configuration shown in Figure 1.4, the resistive loads connected to each d.c. link can be varied in order to represent the requirement of the UNIFLEX-PM converter to deliver different amounts of power through each cell.

An important consideration when designing and implementing multi-level converters is the choice of modulation scheme, which is the algorithm that determines when to activate the switching devices that make up the converter and hence determines the shape of the output voltage waveform. The primary

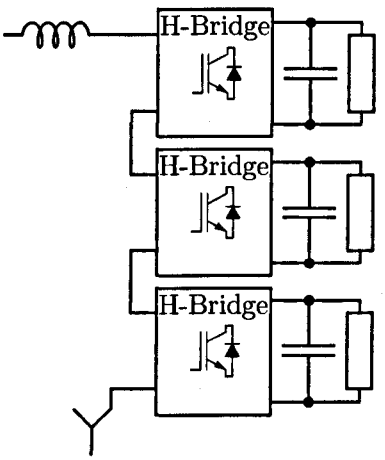


Figure 1.4: One phase of a cascaded H-bridge rectifier

requirement of the modulation process is to produce an output voltage waveform with the desired fundamental component. Switched waveforms inherently include other harmonic components and it is highly desirable that the distortion due to these harmonics is minimal. Low-order harmonics in particular should be low in magnitude.

Another important consideration, especially for grid-connected applications, is that the power losses in the converter should be small. As every switching operation contributes to power loss, high power applications require a low switching rate. A low switching rate, however, tends to produce low-order harmonics, in conflict with the requirement for good quality output waveforms. Careful study must therefore be made when choosing modulation schemes in order to balance the conflicting requirements for good quality waveforms and low switching frequency.

The prototype UNIFLEX-PM converter is modulated using phase-shifted carrier modulation, which is a popular modulation scheme for the cascaded H-bridge converter. Research has shown, however, that phase-shifted carrier modulation does not produce the optimal harmonic spectrum [13]. Therefore, this thesis investigates the application of other modulation techniques to the cascaded H-bridge multi-level converter at the low switching rate demanded

by high power applications. Space-vector modulation and one-dimensional modulation are studied, both for the case where the d.c. voltages are constant and for the more realistic scenario where the capacitor voltages vary. The effect of significant capacitor voltage ripple on the spectrum of the output line voltage is investigated and methods for the modulation scheme to compensate for the ripple are explored. Attention is also paid to the problem of maintaining equal capacitor voltages in each cell, even when the loads on each cell are not equal.

1.1 Thesis Structure

Following this introductory chapter, the work in this thesis is arranged in the following way:

Chapter 2 contains an introduction to multi-level converters and places the cascaded H-bridge converter in the context of other related topologies. Modulation schemes applicable to multi-level converters are also described, including carrier-based modulation, space-vector modulation, one-dimensional modulation and selective harmonic elimination.

In order to study the modulation schemes, simulation models have been developed and a low-voltage, experimental converter has been constructed as part of the work contributing to this thesis. Chapter 3 discusses the structure of the simulations and of the experimental converter including design of the control system and the means to synchronize the converter output to the supply voltage. Methods applied to analyse simulated and experimental results are also introduced. Results from the simulations and experimental work described in Chapter 3 are used to support arguments throughout the remainder of the thesis.

Chapter 4 analyses space-vector modulation of a cascaded H-bridge converter under the simplifying assumption that all the d.c.-link voltages are constant and equal. Existing space-vector algorithms are described and their behaviour analysed at low sampling frequency. In particular, it is observed that both the modulation index and the phase relationship between the sampling process and the reference voltage alter the total harmonic distortion of

the line voltages. A method is presented to exploit this behaviour to reduce the harmonic distortion of the line voltages.

In Chapter 5 the assumption of constant and equal d.c. links is removed and space-vector modulation is explored for time-varying capacitor voltages. The problem of maintaining equal capacitor voltages is investigated when the converter cells are subjected to different loads. This investigation is used to derive theoretical limits within which it is possible to balance the capacitor voltages. Then, a method is presented to balance the capacitor voltages without increasing the switching frequency and its performance is compared to the theoretical limits.

Chapter 5 also discusses the effect of low-frequency ripple of the capacitor voltages. Distortion of the space-vector diagram is used as the basis for spectral analysis of the output waveforms. A feed-forward method is then presented to compensate for the effect of ripple.

In Chapter 6, one-dimensional modulation is discussed, again for varying capacitor voltages, and a close relationship between one-dimensional modulation and level-shifted carrier modulation is observed. The existing implementation of one-dimensional modulation is then extended to apply to converters with a greater number of levels and an alternative implementation is proposed to address flaws identified in the original method.

Finally the thesis is concluded in Chapter 7. Common themes between the modulation methods are described and areas for future work are identified.

1.2 Identification of Original Contribution

In order to aid with the assessment of this work, this section states concisely the novel contributions contained in this thesis.

- **Operation of space-vector modulation at low sampling frequency**

  The basic space-vector modulation algorithms used in this thesis are well established but they are not usually studied at low switching frequencies. In this thesis, study of space-vector modulation at low sampling

rate identifies that the timing of the sampling process influences the harmonic distortion of the output. A novel method is presented to align the sampling times in order to avoid operating the converter at operating points that produce high distortion.

- **Derivation of Limits of Capacitor Balancing Algorithms**

  The cascaded H-bridge converter is usually assumed to have similar loads on each cell. The UNIFLEX-PM project identified that for greatest flexibility it may be desirable to use different converter cells for different purposes whilst interfacing with the same a.c. grid. Hence, in this work, limits have been derived for the imbalance of loads applied to each cell for which it is possible to keep the capacitor voltages equal.

- **Development of Capacitor Voltage Balancing Algorithm Applied to Space-Vector Modulation**

  An algorithm to balance the capacitor voltages of a cascaded H-bridge converter by using the redundant states is described. The method is applicable to space-vector modulation and does not increase the total device switching frequency. The performance of the method is compared to the derived theoretical limits.

- **Derivation of the Effect of Capacitor Voltage Ripple on Space-Vector Modulation**

  Ripple of the capacitor voltages is known to degrade the quality of the converter output waveforms but the effect is not usually quantified. In this work, the influence of capacitor voltage ripple on the space-vector diagram is analysed. The distortion of the space-vector diagram is then used to derive the effect of the interaction between the capacitor voltage ripple and the fundamental reference on the spectrum of the line-to-line voltage waveforms.

- **Feed-forward compensation based on the geometry of the space-vector diagram**

Having developed an understanding of the effect of capacitor voltage ripple on the space-vector diagram, this knowledge is used to derive a simple feed-forward compensation scheme to improve the quality of the output waveform when the capacitor voltages are not constant.

- **Improvements to One-Dimensional Feed-Forward Modulation** Finally, one-dimensional modulation is analysed and is shown to have a close relationship to carrier-based modulation schemes. Existing methods to balance the capacitor voltages by choosing redundant states are shown to increase the total device switching frequency so a novel method is presented to balance the capacitor voltages without increasing the switching frequency. The new method is more easily applied to converters with a greater number of cells than the original scheme.

Chapter 2

Multi-Level Converters

Multi-level converters are a family of power-electronic converters that produce output waveforms containing three or more discrete voltage levels [10], [12]. Examples of two, three- and five-level waveforms, all produced using the same fundamental reference, are shown in Figure 2.1. Two advantages of multi-level waveforms are evident from Figure 2.1:

- The multi-level waveforms contains smaller voltage steps than the two-level waveform with the same fundamental component. The smaller voltage steps place the switching devices under less stress and allow higher voltage waveforms to be produced with devices of lower ratings.
- The multi-level waveforms approximate the sinusoidal reference more closely and contain less harmonic distortion than the two-level wave.

Increasing the number of levels improves the output waveforms further by both reducing the size of the voltage step required for a given application and approximating a pure sinusoid more closely. The improved waveform quality comes, however, at the expense of increased converter complexity and more difficult control as converters with more levels contain more switching devices and more energy storage components.

This chapter presents an introduction to multi-level converters. The main multi-level circuit topologies and their principles of operation are described with particular attention paid to the cascaded H-bridge converter, which is

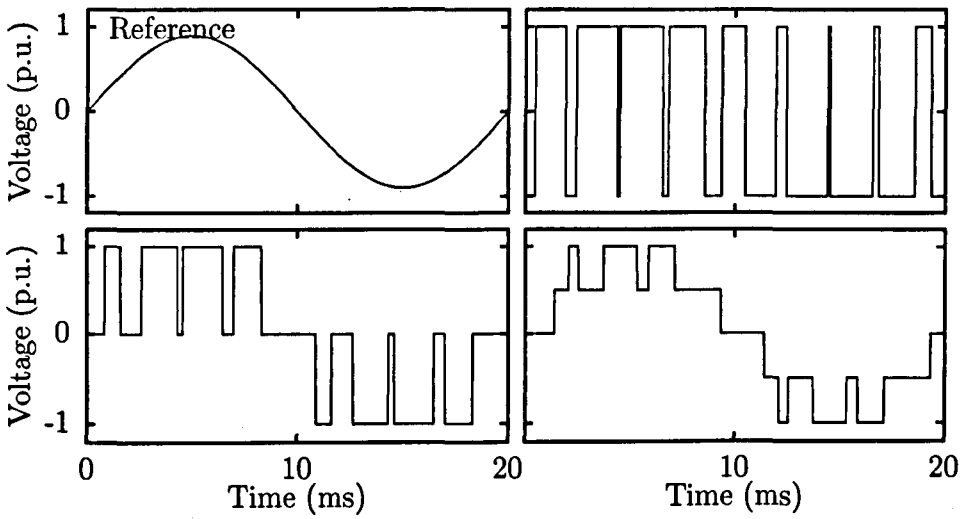


Figure 2.1: Example of two-, three- and five-level waveforms with with the same fundamental component

the topic of this thesis. The established modulation methods are presented, again concentrating on their application to the cascaded H-bridge converter.

2.1 Multi-Level Converter Topologies

The following multi-level converter topologies are discussed in this section:

- the diode-clamped converter,
- the flying-capacitor converter,
- the cascaded H-bridge converter,
- the modular multi-level converter and
- hybrid converter topologies.

The first three have received wide academic and industrial attention over several decades and are the most mature multi-level converters. The modular multi-level converter is a relatively new topology and has generated much research and commercial interest in recent years. Hybrid converters, which are

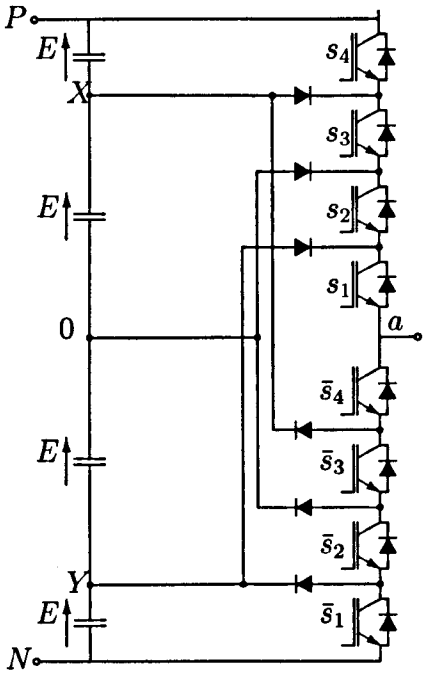


Figure 2.2: Five-level diode clamped converter

State				
s_4	s_3	s_2	s_1	v_{a0}
0	0	0	0	$-2E$
0	0	0	1	$-E$
0	0	1	1	0
0	1	1	1	E
1	1	1	1	$2E$

Table 2.1: Switching states of five-level, diode-clamped converter

created by connecting converter cells of different types in series, are also receiving research attention.

2.1.1 Diode-Clamped Converter

One phase leg of a five-level, diode-clamped converter is shown in Figure 2.2. The switching states of the circuit act to connect the output terminal to one of the points $P, X, 0, Y$ or N in the split d.c. link, producing the output voltages shown in Table 2.1. Note that only four of the eight switching devices are included in Table 2.1 because the switching devices operate in complementary pairs: the state of the switch $\bar{s}_x$ is always the complement of the switch s_x.

The three-level form of the diode-clamped converter, known as the neutral-point-clamped (NPC) converter [14], is the most widely adopted multi-level converter in industry, having been adopted in many traditional industrial ap-

plications, such as pumps, fans and compressors at high power levels [15]. An example of the NPC converter in a commercial, grid-connected application is ABB's *SVC Light* product [16].

Particular research attention into the diode-clamped converter has been paid to the problem of maintaining equal voltages in the split d.c.-link capacitors. The neutral point balancing of an NPC converter was modelled in [17] for the full range of operating conditions. Methods to equalize the capacitor voltages include selecting redundant states of a three-phase converter [18]–[20], modulating different pairs of switches with different reference waveforms [21], co-ordinating the control of both sides of a back-to-back converter [22] or including the balancing requirement in the cost function of predictive controllers [23].

One disadvantage of the diode-clamped topology is that commutations, and therefore switching losses, are not shared equally between the switching devices. Different devices then reach different operating temperatures and the most-used devices are prone to earlier failure. The *active* NPC converter, which replaces clamping diodes with active switches, has been proposed to allow the switches to be utilized equally and therefore to equalize the losses in each device [24].

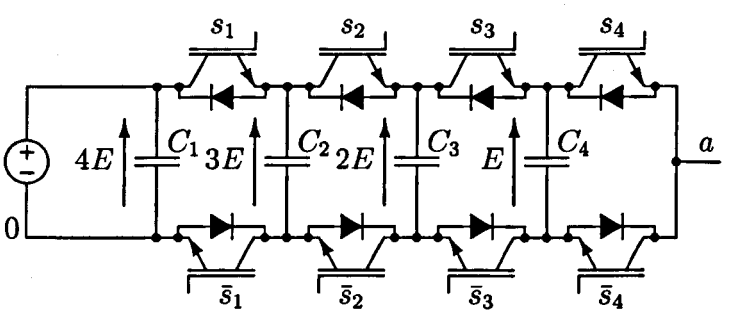


Figure 2.3: Five-level, flying capacitor converter

s_n	s_{n2}	s_{n1}	v_n
-1	1	0	$-E$
0	0	0	0
1	0	1	E

s_n: State of n^{th} bridge

Table 2.2: Definition of switching state notation for a single H-bridge

2.1.2 Flying Capacitor Converter

The flying-capacitor converter, a five-level version of which is shown in Figure 2.3, has also seen industrial use in high power drives and traction applications [25].

The switching state of the flying-capacitor circuit determines which capacitor voltages contribute to the output voltage. As for the diode-clamped converter the switching devices are operated in complementary pairs so, when all the upper switches are open, the output is connected to the negative d.c. terminal and the output voltage is at its lowest. Closing any upper switch contributes E to the output voltage, which is given by the following equation:

$$V_{a0} = E \sum_{n=1}^{N-1} s_n,$$

where N is the number of levels of the converter.

Unlike the diode-clamped converter, any combination of states of the upper switches is permitted. There is redundancy of the switching states so the switching losses can be distributed evenly among the switches by appropriate modulation methods [26].

Much research into the flying-capacitor topology has been focussed on understanding the natural balancing behaviour that maintains the correct charge in the capacitors [27]–[29].

2.1.3 Cascaded H-bridge Converter

The cascaded H-bridge converter, which is the topology considered in this thesis, is constructed from a number of single-phase, full-bridge inverters (H-

bridges) connected in series. This inherently modular structure reduces the cost of commissioning and maintenance [30] and, if the converter is controlled appropriately, increases the tolerance to faults [31].

A five-level version of the cascaded H-bridge, including two cells per phase, is shown in Figure 2.4. Each cell contains an isolated voltage source and the output voltage is the sum of the voltages across the cells, each of which can be $-E$, 0, or E. If the switching state of a single cell is defined as in Table 2.2 the output voltage of a phase leg can be expressed as follows:

$$V_{a0} = E\sum_{n=1}^{N} s_n,$$

where N is the number of converter cells. The result is that an N-cell converter can produce $2N - 1$ levels and, like the flying capacitor converter, there is redundancy of the switching states of a single-phase leg.

The cascaded H-bridge was first developed in the 1990s for medium-voltage a.c. drives [32] and for static synchronous compensation (STATCOM) [33]. In the drive application, the d.c. links are supplied by rectifiers which are, in turn, supplied by separate windings of a complex input transformer. The complexity and expense of this transformer limits the number of cells used in such applications.

The Cascaded H-bridge topology is most suited to the STATCOM application because, without the need to deliver real power, the d.c. links only contain

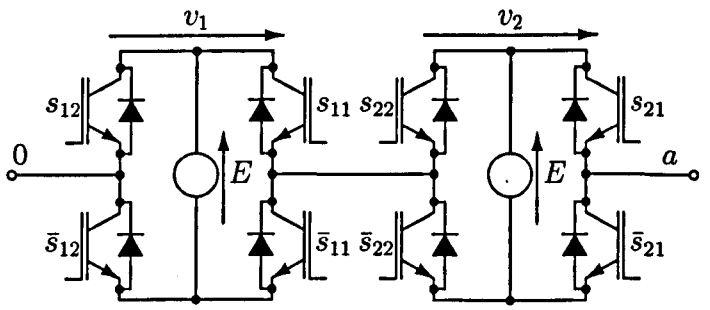


Figure 2.4: Five-level cascaded H-bridge converter

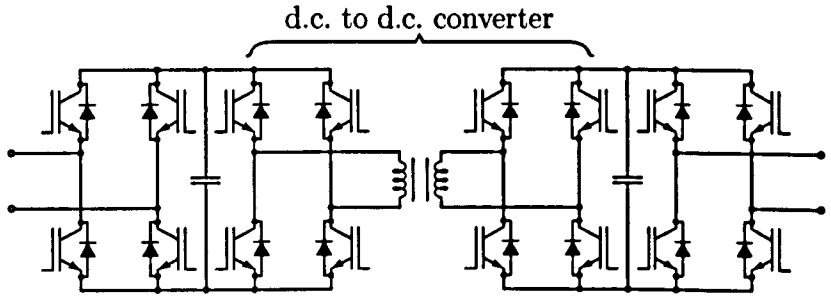


Figure 2.5: Back-to-back module used for UNIFLEX-PM converter

capacitors with no external supply [34], making the converter particularly compact. Other applications where independent voltage sources are inherent are photovoltaic power generation [35] and grid-connected battery storage [36].

If the d.c. voltage sources in the cells of the cascaded H-bridge allow regeneration then the cascaded H-bridge converter can support bi-directional power flow [37], [38]. In the UNIFLEX-PM project the d.c. links are each supplied by isolated d.c.-to-d.c. converters containing a medium frequency transformer with another H-bridge module on the other side (Figure 2.5). Both sides of the converter can be cascaded to interface with a.c. systems in a flexible way [9]. The design of the isolation stage for the back-to-back modules [39] and control challenges have also been the focus of research [40].

An example showing a single phase of the UNIFLEX-PM structure in a three-port configuration is shown in Figure 2.6. In this example, *Port 1* contains three cells and can produce seven levels, *Port 2* contains two cells and can produce five levels and *Port 3* contains a single cell and can produce three levels. Power flow between each port can be controlled, for example to interface two a.c. systems on ports one and two to an energy storage facility on port 3. Using the different modules to interface to multiple systems means that different cells on each port may be subject to different loads.

In this thesis, a three-phase cascaded H-bridge converter with three cells per phase is studied as a model for one port of the UNIFLEX-PM converter. The cascaded H-bridge converter is considered in two modes of operation. First is the inverting mode, in which the d.c. links are supplied by single-

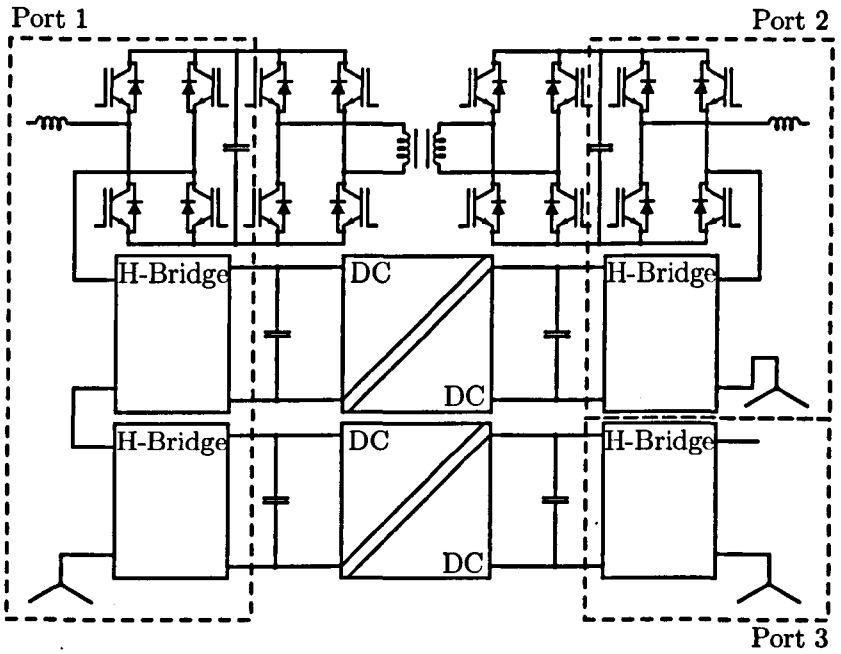


Figure 2.6: Simplified representation of one phase of a UNIFLEX-PM converter in a three-port configuration. One module is shown in full.

phase rectifiers and the modulation is operated in open-loop (Figure 2.7a), allowing the behaviour of the modulation strategies to be investigated without the influence of control systems. The second mode of operation is the rectifying mode, where the supply is connected to the output of the converter via an inductor and the output is synchronized to the supply frequency (Figure 2.7b). Power is drawn from the supply and fed to resistive loads connected to the d.c. side of each H-bridge cell. Varying these resistive loads models the requirement of the UNIFLEX-PM converter to use different cells to interface to different systems with different power requirements.

2.1.4 Modular Multi-Level Converter

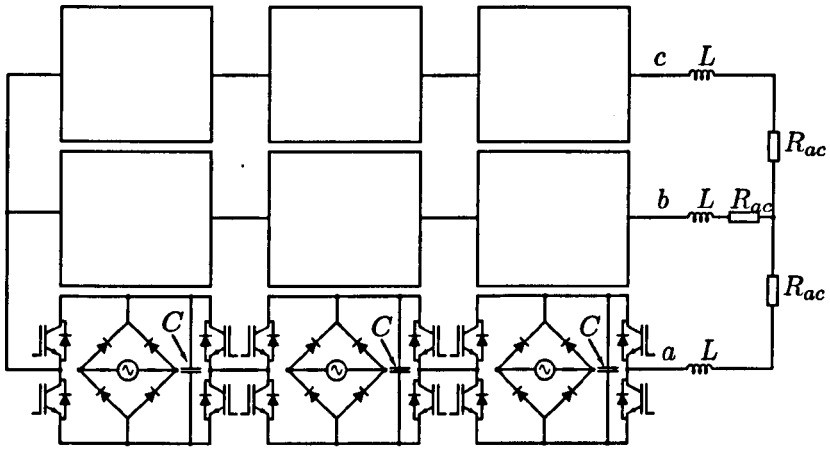
A recent addition to the multi-level converter family is the *Modular Multi-Level Converter* (MMLC), first proposed in 2003 [41]. This topology has inspired considerable research effort and has rapidly gained industrial acceptance with Siemens offering the MMLC circuit for high-voltage d.c. applications under the brand name *HVDC Plus* [42].

One phase leg of a three-level MMLC for HVDC applications is shown in Figure 2.8. The outputs of each cell sum to make a high-voltage d.c. bus with the a.c. output connected in between two strings of modules. Adjusting the number of cells in the *on* state from each string of cells allows the a.c. voltage to be controlled. A constant d.c. voltage is provided by keeping the total number of active cells constant. Every commutation of the upper string of cells is therefore matched by a complementary commutation from the lower string [43].

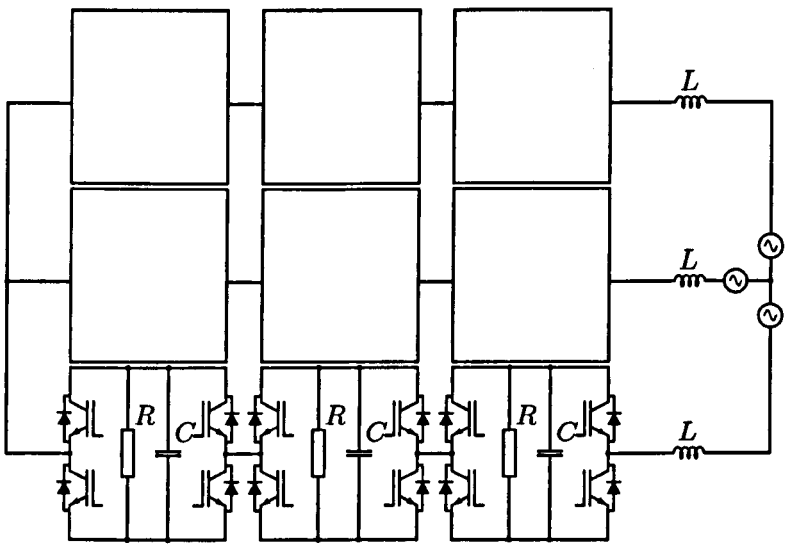
Much research into the MMLC topology has been focussed on understanding the dynamics of the topology and deriving control methods. [44], [45]. It has also been identified that the output voltages can be controlled independently so it is possible to use the same circuit topology for a.c.-to-a.c. conversion [46].

2.1.5 Hybrid Topologies

Hybrid multi-level converters are made up of different cells connected in series [47], the simplest form being a cascaded H-bridge with different voltage lev-



(a)



(b)

Figure 2.7: Converter structures considered in this thesis: (a) inverting and (b) rectifying configurations

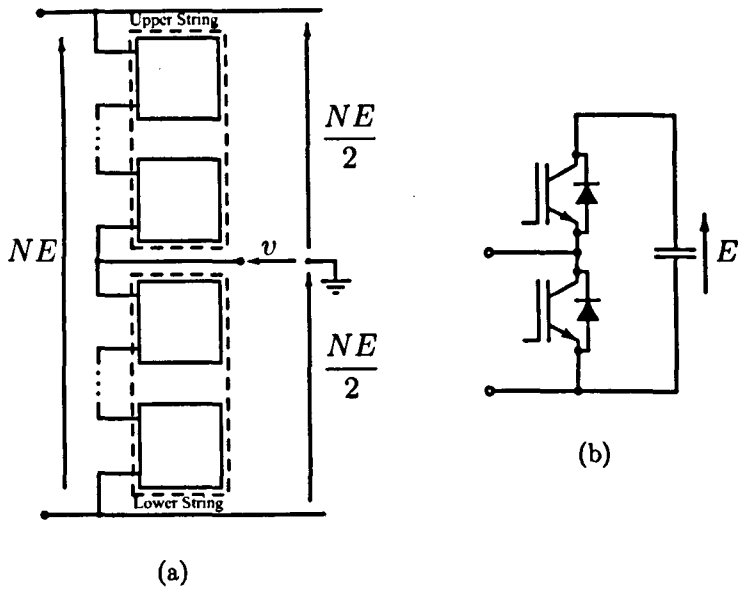


Figure 2.8: Modular Multi-level converter (a) Single-phase leg (b) Cell structure

els in each cell, also known as the *asymmetric* cascaded H-bridge converter [48]. Other hybrid converters include various series combinations of two-, three- and five-level cells operating at different voltage levels, providing a broad range of topologies to provide a given number of voltage levels [49]. One such arrangement is the combination of a three-level NPC converter with floating H-bridge modules reported in [50], [51] and depicted in Figure 2.9. This particular hybrid converter, with the ratio of capacitor voltages shown, can produce nine different voltage levels.

2.2 Modulation Schemes

The modulation scheme for a multi-level converter is the algorithm by which the switches are operated in order to produce the desired fundamental a.c. waveform, with acceptable harmonic distortion. The main modulation methods that have been applied to multi-level converters are outlined in the following sections, including carrier-based modulation, space-vector modulation,

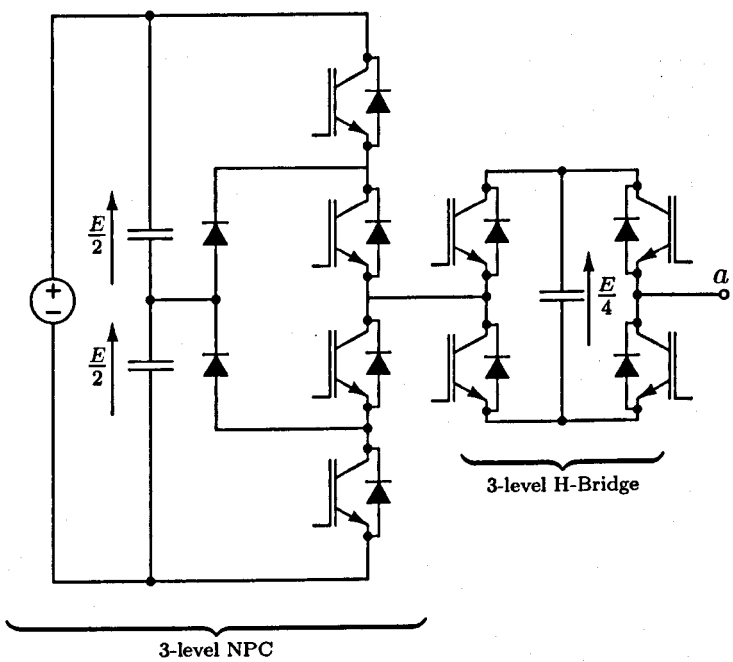


Figure 2.9: Hybrid converter comprising a three-level NPC converter in series with a floating H-bridge cell

one-dimensional modulation and selective harmonic elimination. Specific modulation methods tailored to individual forms of hybrid converter are not covered because they are not relevant to this thesis.

2.2.1 Carrier Modulation

Carrier-based modulation schemes have their origins in analogue control systems where the pulsed waveform required to operate a switching device can be created by comparing a sinusoidal reference to a triangular carrier waveform. Multi-level converters contain multiple switching devices and hence multiple carriers are required; for example an N-level waveform is produced using $N-1$ carrier signals. These carriers can be arranged in a number of different ways, including level-shifted-carrier (LSC) and phase-shifted-carrier (PSC) modulation, which are shown in Figures 2.10 and 2.11 respectively [13], [52]–[54]. In both these examples, an output voltage step is produced each time the reference crosses a carrier signal. Research has concluded that the level-shifted arrangement of carriers depicted in Figure 2.10, that is with all the carriers in phase, produces least harmonic distortion in a three phase system because a large harmonic at the carrier frequency cancels between the phases [13].

The harmonic spectrum of level-shifted carrier modulation can be further improved by adding a common-mode offset to the three-phase reference waveforms. The optimal common-mode offset for two-level modulation was derived in [55] and shown to produce identical waveforms to space-vector modulation. Similar methods were applied in [56] to identify the optimal common-mode offset for level-shifted carrier modulation. Example reference waveforms including the common mode offset are shown in Figure 2.12 for two- and multi-level modulation respectively.

Despite producing more harmonic distortion, PSC modulation is popular for the cascaded H-bridge converter because PSC modulation naturally draws power equally from each cell and utilizes the switches evenly [32], [53], [57]. The conventional implementation of LSC modulation, conversely, causes the cells of a cascaded H-bridge converter to operate at different switching frequencies and draws different amounts of power from each cell. LSC modulation has therefore

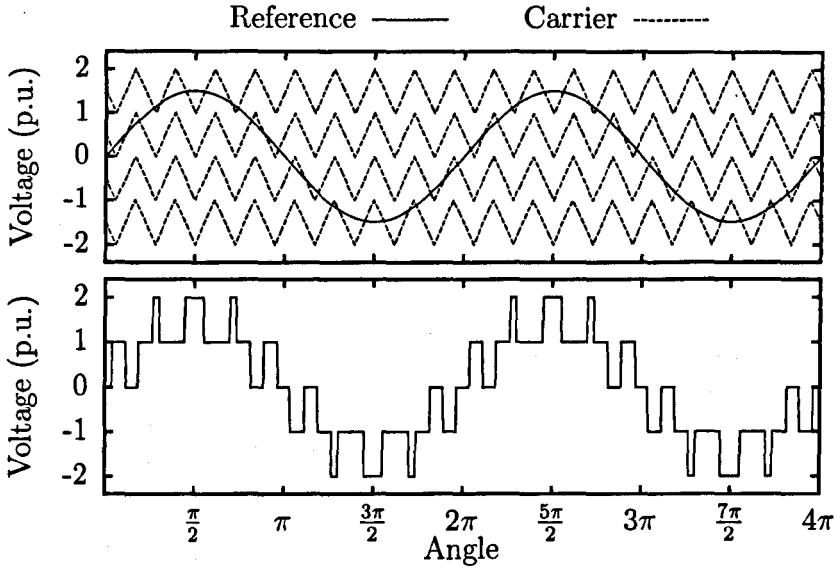


Figure 2.10: Level-shifted carrier modulation

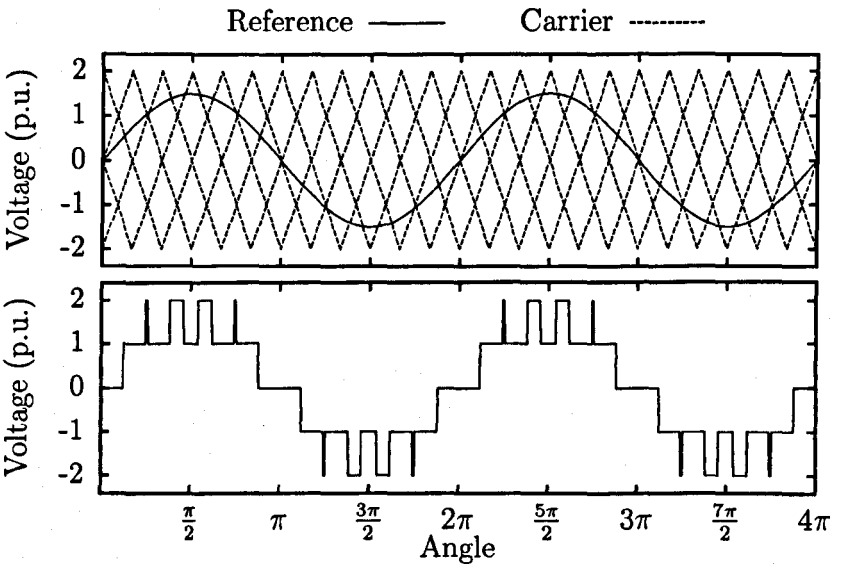


Figure 2.11: Phase-shifted carrier modulation

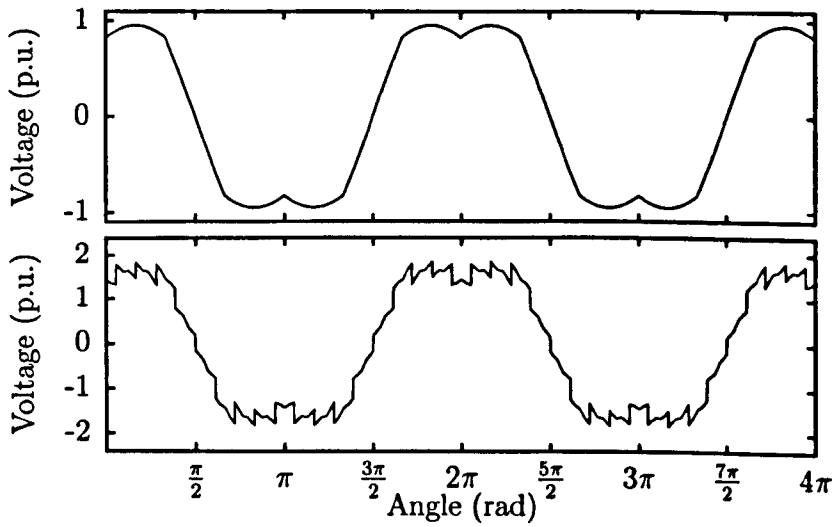


Figure 2.12: Reference waveform including optimal common-mode offset for two-level (top) and multi-level (bottom) modulation

been modified for use in the flying capacitor and cascaded H-bridge converters in order to draw power equally from each cell, whilst still benefiting from the superior harmonic performance of LSC modulation. These modifications involve using the redundant states of the phase legs to cycle the role of each bridge during consecutive fundamental cycles [13], [26], [58], [59].

Regular Sampling

In a digital control system, carrier-based modulation schemes are often implemented in a regularly sampled fashion, where the duty cycles are calculated based on sampled reference signals. Conceptually, regularly sampled modulation strategies are equivalent to comparing a sampled reference to the triangular carriers, where the reference is held constant during the sampling period. As shown in Figure 2.13, the reference can be sampled once per carrier period, known as *symmetrical* regularly sampled modulation, or twice per carrier period, known as *asymmetrical* regularly sampled modulation. The asymmetrical method is superior because, at a given switching frequency, more harmonics are cancelled than when using symmetrical regular sampling [60]. This ob-

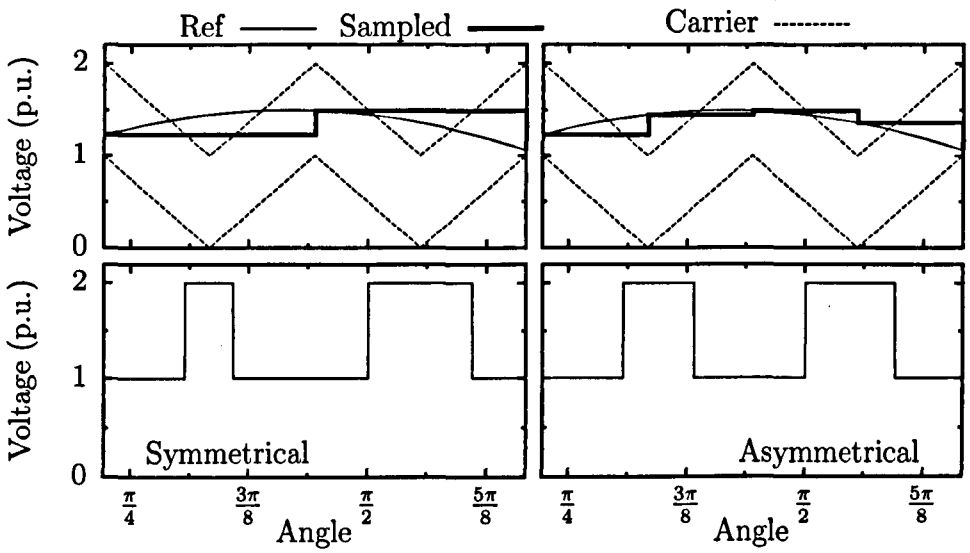


Figure 2.13: Symmetrical and asymmetrical regular sampling

servation has important implications for the implementation of space-vector modulation discussed in Chapter 4.

2.2.2 Space-Vector Modulation

Space-vector modulation is a regularly-sampled modulation technique for three-phase converters. Instead of modulating each phase leg individually, space-vector modulation chooses switching states of the entire three-phase converter based on a mathematical transformation of the reference and of the line voltages produced by each switching state. In contrast to carrier-based modulation, space-vector modulation is concerned with the line voltages and only implicitly produces the phase voltage waveforms.

The basis of space-vector modulation is the representation of three-phase switching states on the (α, β) plane [61]. Each three-phase switching state consists of three values, (s_a, s_b, s_c), which represent the output of each phase leg normalized by the capacitor voltages. In Figure 2.14 the possible switching states of a two-level, three-phase inverter are plotted with their a, b and c components contributing vector components in the direction of the axes shown. For example the switching state $(s_a, s_b, s_c) = (1, 1, 0)$ has a component parallel

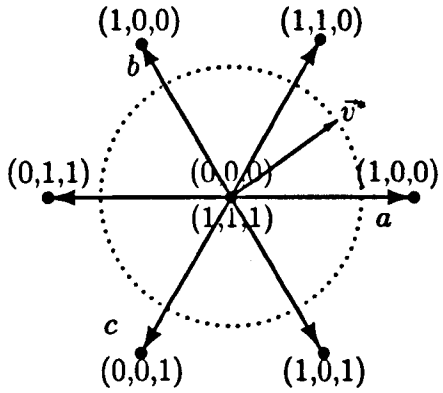


Figure 2.14: Space-Vector Diagram for a two-level Inverter

to the a axis and another component at 120° parallel to the b axis. The resultant vector is of unit magnitude at an angle of 60°. The eight possible switching states of a three-phase, two-level inverter therefore form the vertices of a hexagon; the states $(0,0,0)$ and $(1,1,1)$ both occupy the origin. Switching states occupying the same point on the space-vector diagram are known as *redundant* states.

Figure 2.14 also shows a three-phase reference voltage vector, $\vec{v}^*$, which traces a circular path on the space vector diagram. The task of space-vector modulation is to approximate samples of the continuous reference vector using the discrete switching vectors of the converter.

The switching states of a multi-level converter can be plotted in the same way, as shown for three- and five-level converters in Figure 2.15. In each case the switching states form a hexagon made up of discrete switching vectors at the vertices of triangles. Increasing the number of levels adds to the number of possible switching states and switching vectors, resulting in a larger hexagon.

As the number of levels is increased, the redundancy of the switching states also increases. Figure 2.16 shows that there are many switching vectors that can be produced by more than one switching state in the first sector of the 5-level space-vector diagram. The choice of redundant switching states, in addition to any redundancy in the phase legs, provides a degree of freedom that is an important feature of space-vector modulation.

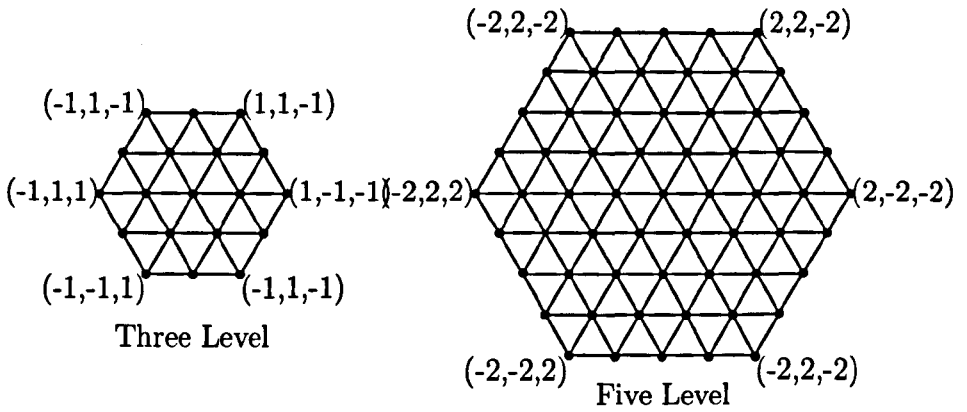


Figure 2.15: Space-vector diagram for three- and five-level converters

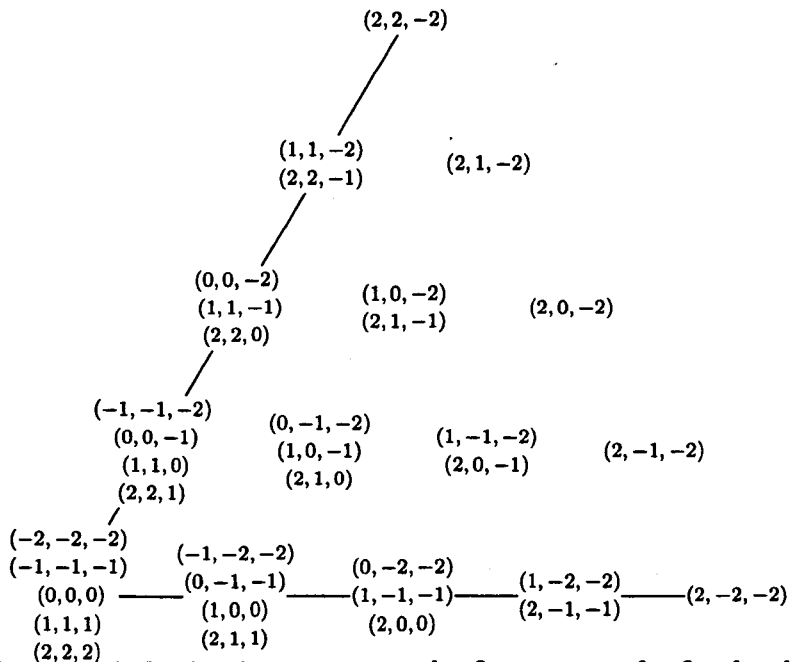


Figure 2.16: Redundant states in the first sector of a five-level converter

The first step of space-vector modulation is to sample the rotating reference voltage vector, $\vec{v}^*$, and to determine its location on the space-vector diagram relative to the switching vectors. The space-vector modulator locates the three vectors nearest to the reference, selects suitable redundant states and applies the chosen states for time intervals obeying (2.1) to produce a time-averaged vector equal to the reference.

$$\sum_{r=1}^{n} d_r \vec{s}_r = \vec{v}^* \tag{2.1}$$

In equation (2.1)

$\vec{s}_r$ is the r^{th} switching vector to apply during the sampling period,

d_r is the proportion of the sampling period to apply that vector and

n is the number of vectors to apply.

Multiple algorithms exist to locate the nearest three vectors, calculate the duty cycles [62], [63] and to choose redundant switching states [56], [64], [65]. More detail of the space-vector methods adopted in this thesis are given in Chapter 4.

Since its inception, two-level space-vector modulation has been known to be equivalent to carrier-based modulation with a suitable common-mode offset [61], [66]. Multi-level space-vector modulation has also been shown to be closely related to level-shifted carrier modulation, although the common-mode offset is more complex [56]. The inherent common-mode offset allows space-vector modulation to make better use of the d.c. link voltage than carrier modulation with a sinusoidal reference and also reduces the harmonic distortion of the output voltages [56]. The common-mode component of space-vector modulation can also be seen as a disadvantage of the modulation technique, so variants have been proposed to reduce the common-mode voltage using a different choice of redundant states [67].

Because of the relationship between space-vector modulation and level-shifted carrier modulation, space-vector modulation does not naturally utilize the switches of a cascaded H-bridge evenly or draw power equally from the cells.

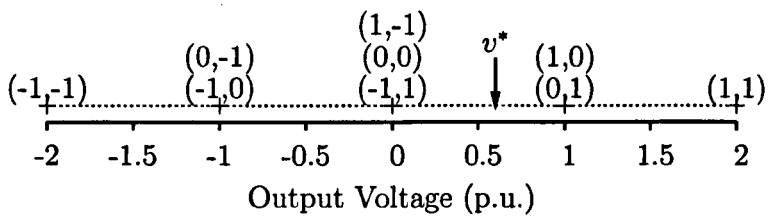


Figure 2.17: Control region for one-dimensional modulation with equal capacitor voltages

Similar modifications as were discussed for level-shifted carrier modulation must also be made to space-vector modulation if it is applied to a cascaded H-bridge converter.

2.2.3 One-Dimensional Modulation

One-dimensional modulation is another regularly sampled modulation scheme which, similar to space-vector modulation, allows freedom over the choice of redundant switching states [68]. Unlike space-vector modulation, one-dimensional modulation is a single-phase modulation technique so must be applied individually to each phase leg.

The basis of one-dimensional modulation is the so-called *one-dimensional control region*, such as the control region for a 5-level converter shown in Figure 2.17. In this diagram, switching states of a single-phase leg are expressed as row vectors listing the states of each bridge and the output voltage produced by each state is plotted against a horizontal voltage scale. At each sampling instant, the single-phase reference voltage is located in the control region and nearby switching states are chosen. The chosen switching states are applied for time intervals calculated to produce the same average output as the reference during the sampling period. Unequal and changing capacitor voltages can be accounted for by updating the control region at each sampling instant based on measured capacitor voltages [69].

As will be shown in Chapter 6, one-dimensional modulation is closely related to regularly-sampled, level-shifted carrier modulation hence it can also

be used to implement space-vector modulation [70].

2.2.4 Selective Harmonic Elimination

The modulation schemes described so far are based on approximating portions of a sinusoidal reference during fixed periods: the carrier period or the sampling period. Selective harmonic elimination (SHE) is different because the entire a.c. waveform is pre-programmed to produce the desired fundamental component and the switching edges are precisely timed in order to eliminate specific low-order harmonics. To operate in closed-loop, switching angles must be pre-calculated to eliminate the desired harmonics for the required range of modulation index.

To produce SHE waveforms, the angles of the switching edges are considered to be degrees of freedom. A multi-level waveform with n switching edges can be derived by solving a system of n equations defining the desired fundamental component and $n-1$ unwanted harmonics to eliminate [71]. In the example of a five-level SHE waveform shown in Figure 2.18, angles α_1, α_2 and α_3 have been calculated in order to eliminate the fifth and seventh harmonics assuming quarter- and half-wave symmetry. The number of degrees of freedom can be increased, allowing more harmonics to be cancelled, if the requirement for quarter-wave symmetry is removed [72].

The equations defining the position of the switching edges are transcendental with multiple solutions so it is usual to pre-calculate switching angles off-line. Solutions are required for every modulation index in the operating range of the converter so much research focusses on finding continuous solution trajectories over a range of modulation index using one of many numerical methods [71], [73], [74]. Specific challenges relating to using SHE in closed-loop have also been studied [75] as well as the challenges of charge balancing [76]–[78].

Other modulation schemes have been proposed where, instead of eliminating certain harmonics, switching edges are chosen to fit harmonics within a spectral envelope, such as the requirements of a specific grid code [79], [80].

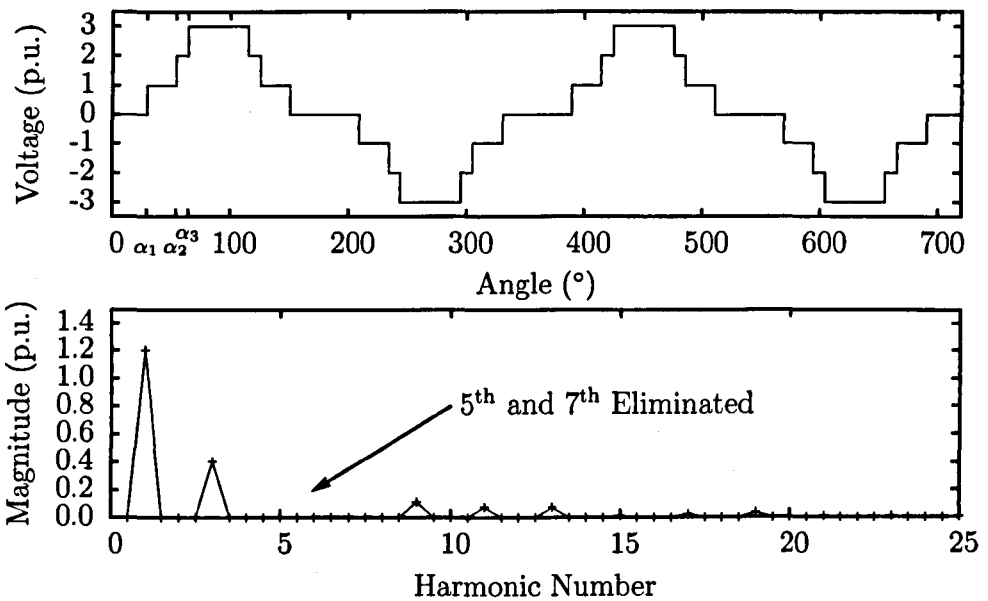


Figure 2.18: Five-level waveform eliminating fifth and seventh harmonics

2.3 Summary

This chapter has presented an introduction to multi-level converter technology. The main benefits of multi-level converters are the ability to produce high voltage waveforms with low harmonic distortion using switching devices of lower voltage ratings.

The three main multi-level converters, namely the diode-clamped, flying-capacitor and cascaded H-bridge converters, have been described including the main focus of research into the topologies. Emerging circuit topologies have also been described, including the modular multi-level converter, which has received particular attention for HVDC transmission, and hybrid converters, which are constructed by connecting various different types of converter in series. Of all the topologies described, the cascaded H-bridge converter is the only topology that is discussed further in this thesis because of its use in the UNIFLEX-PM project.

Modulation schemes for multi-level converters have also been discussed, including carrier-based modulation, space-vector modulation, one-dimensional modulation and selective harmonic elimination. The most popular modula-

tion scheme applied to the cascaded H-bridge converter is phase-shifted carrier modulation because power is naturally drawn equally from each cell and the switching devices are utilized evenly. Level-shifted carrier modulation and space-vector modulation produce a cleaner harmonic spectrum so have been modified to also use the switching devices of the cascaded H-bridge evenly.

When controlling a converter using a digital control system, it is convenient to use regularly sampled modulation schemes, such as digital implementations of carrier-based modulation, space-vector modulation or one-dimensional modulation. Asymmetrical regular sampling, where the reference is sampled twice per carrier period, produces less harmonic distortion than symmetrical modulation, where the reference is only updated once per carrier period. This observation is also relevant to the implementation of space-vector and one-dimensional modulation.

Chapter 3

Research Methods

The remaining chapters of this thesis discuss various modulation techniques applied to the cascaded H-bridge converter under differing operating conditions. Each chapter contains some theoretical work that is supported by results from simulation and from an experimental converter constructed during the course of study. This chapter documents the structure of the simulation models and the construction of the experimental converter. Included in the discussion is the derivation of the control system, which is common to both the simulated and experimental converter, and the mathematical methods adopted to analyse results.

3.1 Simulation Models

Computer models of a seven-level, three-phase cascaded H-bridge converter have been developed using the Saber simulation package from Synopsis, which allows event-based simulation of the modulation algorithms to be combined with continuous simulation of the electrical parts of the circuit. The event-based modulation code can be ported easily to the C programming language for later use in the experimental converter.

Models have been developed in three configurations:

- an inverting model with ideal d.c. links,
- an inverting model with d.c. links supplied by single-phase rectifiers and

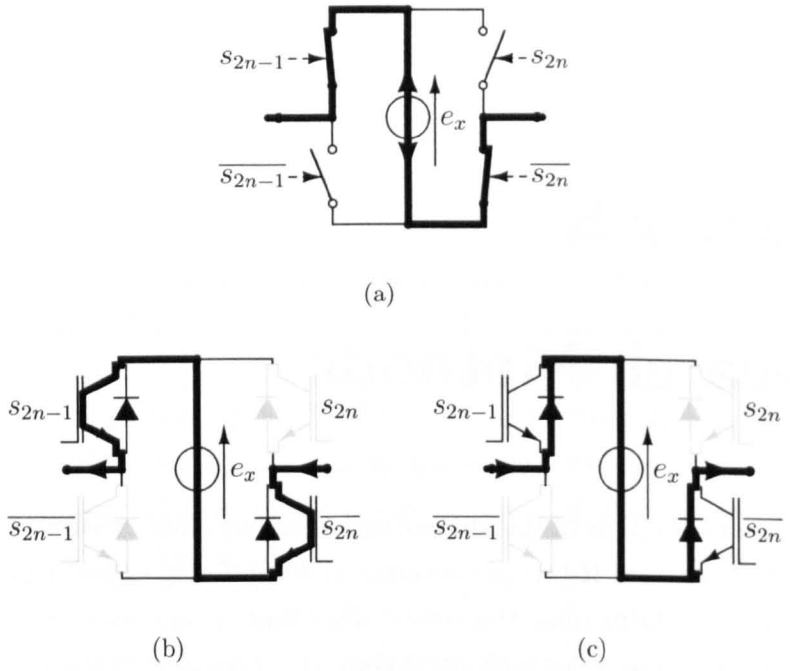


Figure 3.1: (a) H-bridge with ideal switches (b) H-bridge with positive current (c) H-bridge with negative current

- a closed-loop rectifying model.

In each model, switching devices are modelled as ideal switches to allow simulations to run quickly as the commutation behaviour of the power-electronic switching devices is not the focus of this work. Figure 3.1a shows an H-bridge in the negative switching state modelled with ideal switches. The ideal switches allow current to flow in either direction, as do the IGBTs with anti-parallel diodes in Figures 3.1b and 3.1c.

Open-Loop Models The simplest computer model is of a three-phase, seven-level cascaded H-bridge converter operating as an inverter in open loop (Figure 3.2). In the most ideal model, the H-bridge modules contain ideal d.c. sources (Figure 3.3a) and in a second model, the H-bridges are supplied by single-phase bridge rectifiers (Figure 3.3c). The a.c. load is a three-phase resistor-inductor combination.

The modulator block can be altered to produce gate signals for the

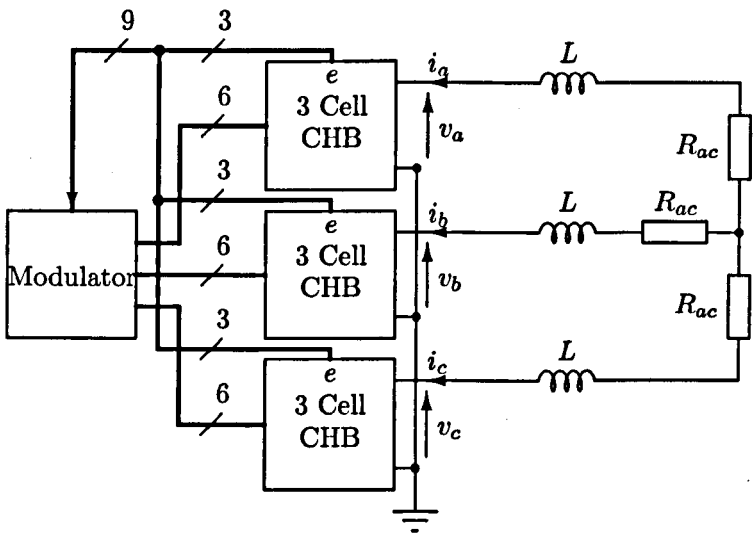


Figure 3.2: Schematic of open loop simulation model.

switching devices using any modulation scheme. Capacitor voltage measurements are available to the modulator block so that feed-forward modulation schemes can be investigated.

Rectifying Model A rectifying model is investigated because its control requires synchronization to the supply and includes some of the challenges relevant to grid-connected applications. The main structure of the rectifier model is shown in Figure 3.4. The H-bridge modules each include a capacitor and resistor connected in parallel with no d.c. supply (Figure 3.3b). Hence, this arrangement can only consume and not deliver active power. The a.c. reference voltages ($v^*_{a,b,c}$) are synchronized to a three-phase supply and control is implemented in the synchronous (d,q) frame using the control structure discussed in section 3.3.

3.2 Experimental Converter

The experimental converter (Figure 3.5) is a three-phase, seven-level cascaded H-bridge multi-level converter that can be configured to operate as an inverter

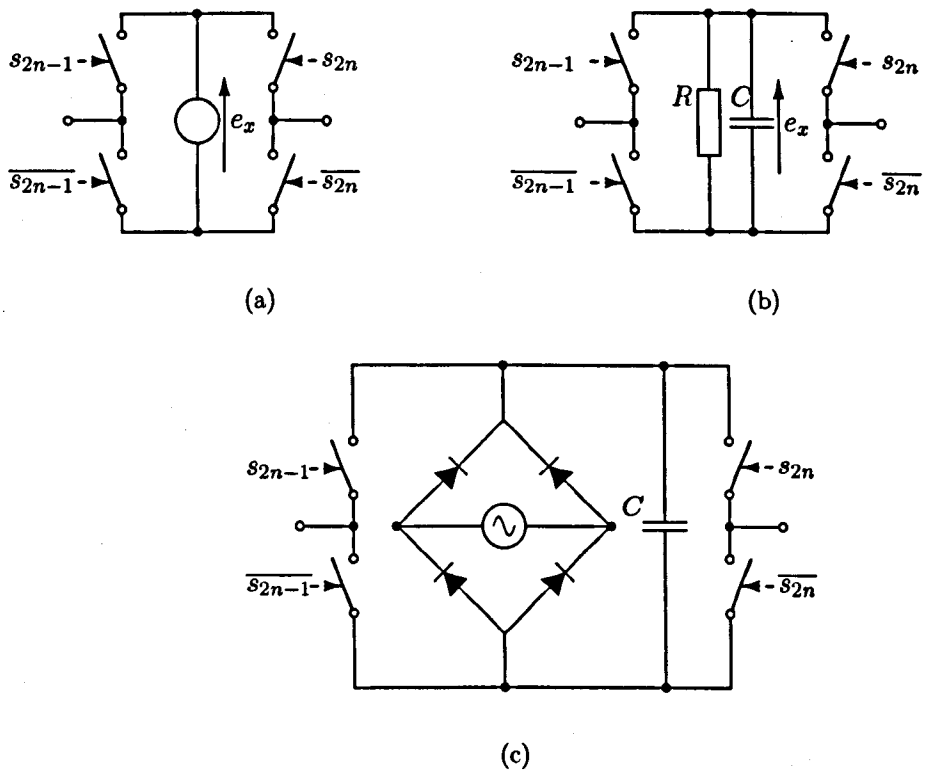


Figure 3.3: H-bridge modules using d.c. link comprising (a) an ideal voltage source, (b) a capacitor and load resistor and (c) a rectified a.c. voltage source

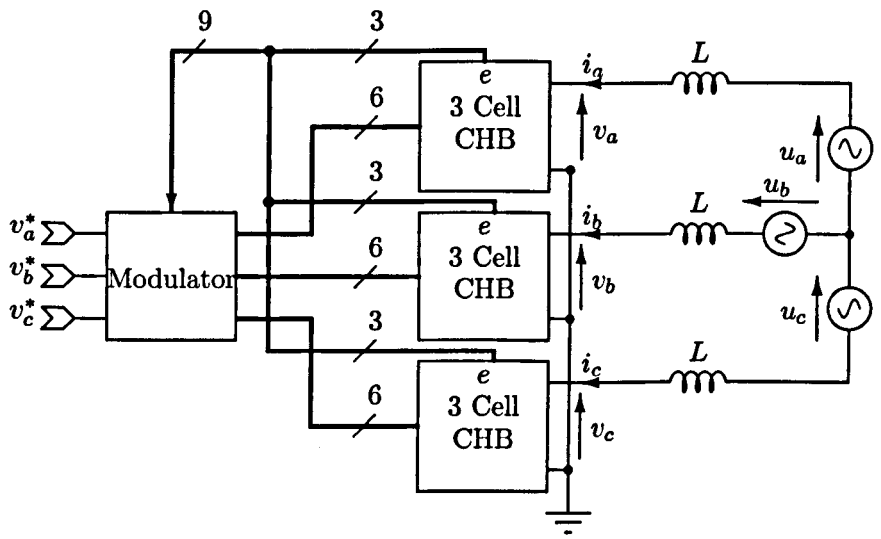


Figure 3.4: Schematic for closed loop simulation

or active rectifier. In the inverting configuration (Figure 3.6a), each H-bridge module is supplied by its own isolating step-down transformer. In turn, the transformers are supplied by a three-phase, variable auto-transformer which allows the converter to be started both simply and safely without any pre-charge system by gradually increasing the supply voltage.

In the rectifying configuration (Figure 3.6b) the transformers are disconnected from the d.c. links and the output from the auto-transformer is attached to the a.c. side of the converter via a smoothing inductor. Resistive loads are attached to each d.c. link and the converter is operated in synchronism with the supply.

3.2.1 H-bridge modules

The H-bridge modules are of an existing design that is widely used for similar projects in the PEMC group at the University of Nottingham. A simplified block diagram of the basic functionality of the H-bridge driver for one H-bridge leg is shown in Figure 3.7. The module contains two such circuits to control both legs of the H-bridge.

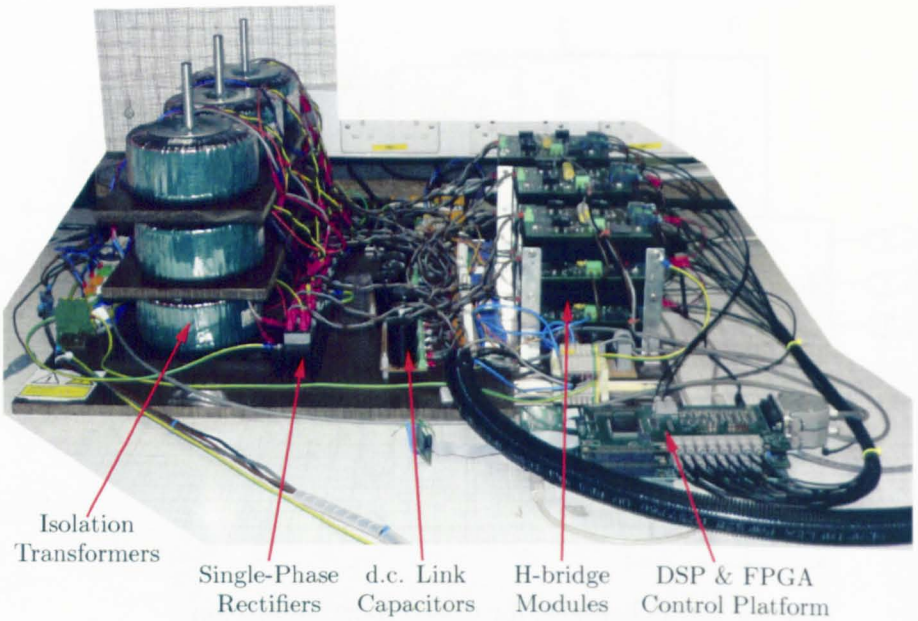


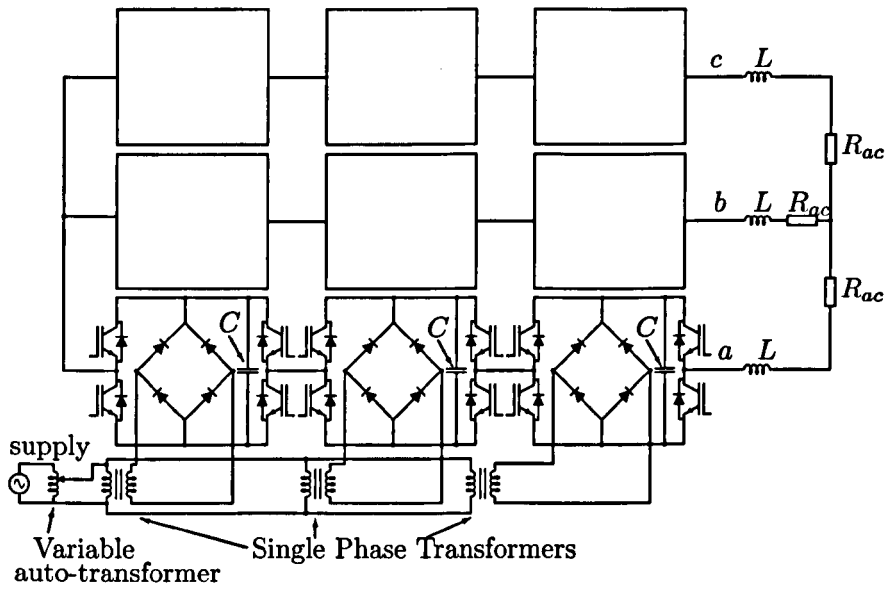
Figure 3.5: Experimental converter

One control input is required for each H-bridge leg as the complementary signal for the second switch in the leg is generated by the driver module. In order to prevent both switches from being active at the same time, which would short-circuit the capacitor through the devices and lead to their destruction, the on-state signal is delayed slightly in order to introduce a brief *dead-time* to allow one switch to turn off completely before activating the complementary switch.

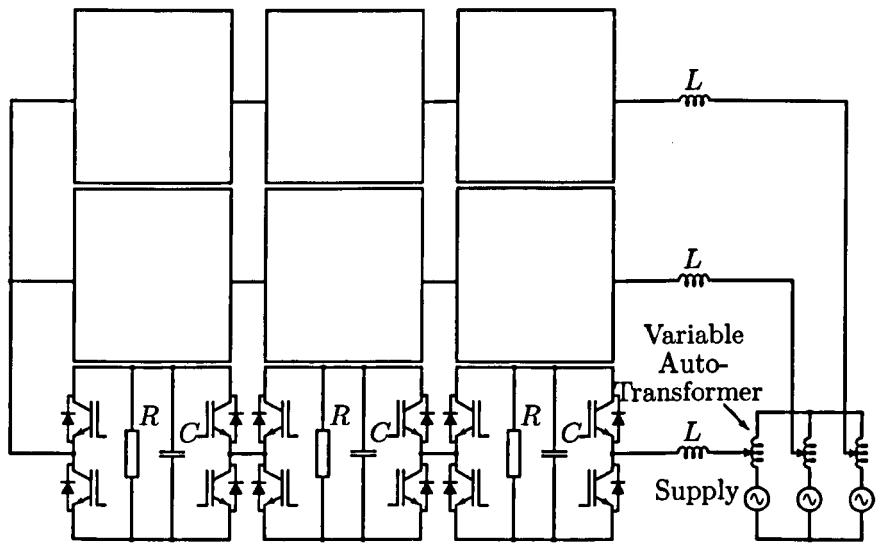
There is also an enable line that, when inactive, turns off all the switches so each H-bridge appears as a diode rectifier from the a.c. side.

3.2.2 Control Interface

The experimental converter is controlled using a Texas Instruments C6713 DSP Starter Kit (DSK) control board interfaced with two FPGA-based daughter boards of a design used to control most of the power-converter projects in the PEMC group at the University of Nottingham. The FPGA boards are accessed via the external memory interface (EMIF) of the DSP and perform



(a)



(b)

Figure 3.6: Structure of experimental converter in (a) inverting and (b) rectifying configurations

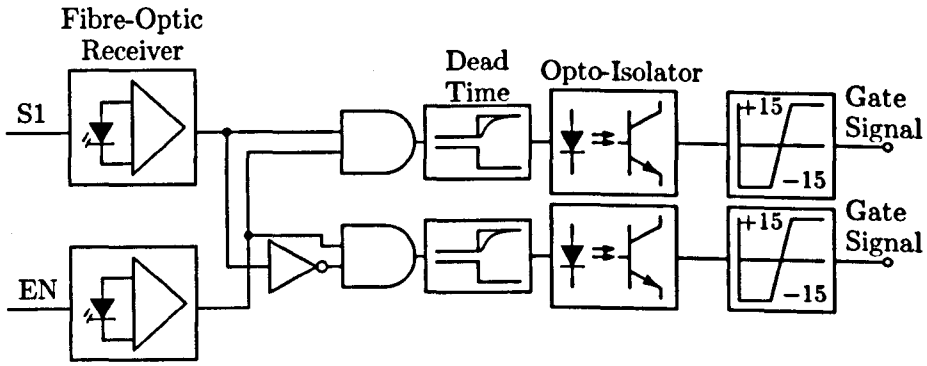


Figure 3.7: Functions of H-bridge interface board for one leg

several functions:

- timing of the DSP interrupt signal at the start of each PWM period,
- timing of the gate signals,
- analogue to digital conversion of measurement signals and
- tripping the converter if measurements fall outside a pre-defined range or if the DSP programme stops running.

Each daughter card has ten fibre-optic outputs, ten analogue-to-digital inputs and a number of general purpose input/output ports. To provide sufficient gate signals and measurements for this converter, two daughter cards are interfaced together. Measurements and gate signals are shared between the two cards as shown in Figure 3.8.

At the start of each PWM period, the primary FPGA triggers an interrupt in the DSP. The DSP responds by calculating switching states and associated time intervals based on the appropriate control laws and the chosen modulation technique. The switching states are stored in a FIFO register in the primary FPGA and are applied for the correct duration during the next PWM period (Figure 3.9). Note that this arrangement introduces a delay of one sampling period between the sampling and the control action, which must be accounted for in the design of controllers.

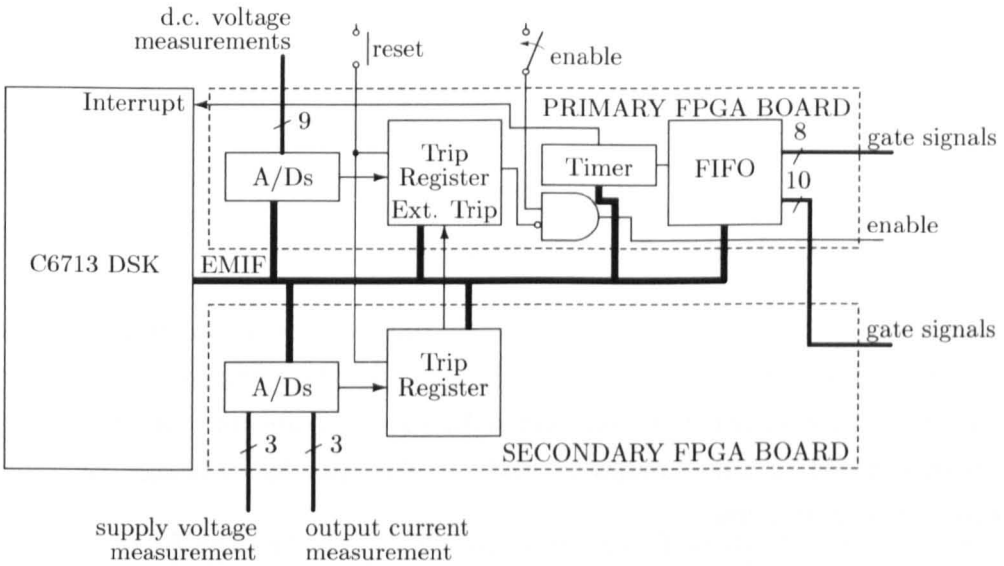


Figure 3.8: Structure of the DSK control board and two FPGA-based daughter cards.

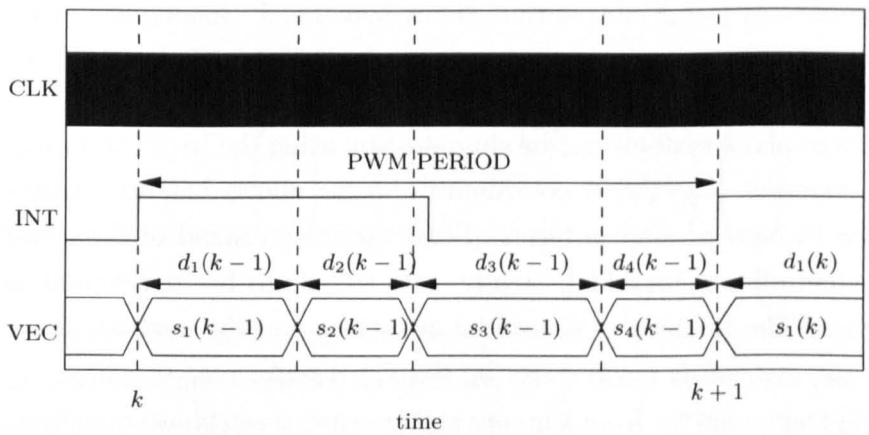


Figure 3.9: Example timing diagram showing production of switching vectors.

A trigger line is also available so that an oscilloscope can be triggered at the same time as control variables are recorded in the DSP memory for later analysis. This arrangement allows demanded switching functions to be closely compared to the converter output waveforms and allows the operation of control algorithms to be analysed and debugged.

3.3 Modelling and Control

Controllers have been designed to allow the converter to operate as a controlled rectifier in the configuration shown in Figure 3.4. The controllers, which have been used in simulation studies and with the experimental converter, were designed based on a mathematical model of the cascaded H-bridge converter, which is derived below.

3.3.1 Mathematical Model of the Cascaded H-bridge

A complete dynamic model of the cascaded H-bridge in the synchronously rotating (d, q) reference frame is given in [81]. The modelling process described in this section is based on [81] but is simplified to the level required to derive current and voltage controllers.

Reference Frames

Analysis of three-phase systems can be simplified by using the (α, β) and (d, q) co-ordinate systems. The (α, β) co-ordinate system allows balanced three-phase systems to be expressed in terms of two variables instead of three and the (d, q) system allows sinusoidal, steady-state signals to be represented as constant values. The tracking of sinusoidal quantities and the analysis of the dynamics of a.c. systems is made easier by the d, q transformation [82].

The (α, β) frame derives from the observation that three-phase quantities with no common-mode component lie, by definition, in the plane defined by (3.1).

$$y_a + y_b + y_c = 0, \tag{3.1}$$

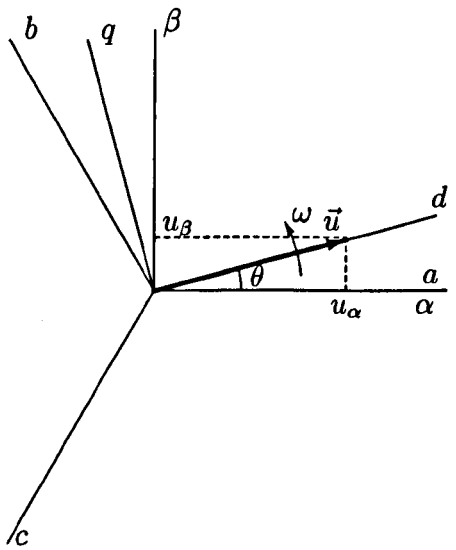


Figure 3.10: Alignment of (a, b, c), (α, β) and (d, q) co-ordinate systems with respect to the supply-voltage vector $\vec{u}$.

where three-phase voltages or currents can be substituted in place of the place-holder variable $y_{a,b,c}$.

The α and β co-ordinate axes lie in this plane and the third co-ordinate axis, the γ axis, is perpendicular to the plane and represents the common-mode component. The transformation from the (a, b, c) co-ordinate system to (α, β, γ) is defined as follows.

$$\begin{pmatrix} y_\alpha \\ y_\beta \\ y_\gamma \end{pmatrix} = \begin{pmatrix} 1 & -1/2 & -1/2 \\ 0 & \sqrt{3}/2 & -\sqrt{3}/2 \\ 1/\sqrt{2} & 1/\sqrt{2} & 1/\sqrt{2} \end{pmatrix} \begin{pmatrix} y_a \\ y_b \\ y_c \end{pmatrix} \tag{3.2}$$

Under this convention, vectors representing balanced, three-phase voltages or currents have constant magnitude of $\frac{3}{2}$ times the single-phase peak and rotate in the plane at the supply frequency ω. The γ, or common-mode, component of the vectors can be ignored because there is no path for common-mode currents in the three-wire systems studied in this thesis. The remaining α and β components can then be represented in complex notation, in which

the transformation (3.2) is equivalent to (3.3).

$$\vec{y} = y_a + y_b e^{j\frac{2\pi}{3}} + y_c e^{-j\frac{2\pi}{3}}, \tag{3.3}$$

where

$$y_\alpha = \Re(\vec{y}) \qquad \text{and} \qquad y_\beta = \Im(\vec{y}).$$

Steady-state vectors have constant magnitude and rotate at the same frequency on the (α, β) plane so they appear constant when analysed in a reference frame rotating at the same frequency, known as the (d, q) reference frame. For grid-connected applications it is most useful if the d axis of the rotating frame aligns with the supply voltage vector $\vec{u}$ (Figure 3.10). Continuing with the complex notation the transformation of a vector from (α, β) to (d, q) co-ordinates is as follows:

$$\vec{y}_{dq} = \vec{y} e^{-j\theta}. \tag{3.4}$$

Because the (d, q) frame is used to construct dynamic models of systems, it is useful to consider the effect that the rotation of the reference frame has on differentiation.

$$\begin{aligned} \frac{\mathrm{d}\vec{y}_{dq}}{\mathrm{d}t} &= \frac{\mathrm{d}}{\mathrm{d}t}(\vec{y} e^{-j\theta}) \\ &= \frac{\mathrm{d}\vec{y}}{\mathrm{d}t} e^{-j\theta} - j\omega \vec{y}_{dq} \end{aligned} \tag{3.5}$$

The j in the second term of (3.5) causes the d and q components to be coupled. This term will appear in the derivation of the model of the cascaded H-bridge and will later be accounted for in the control system using feed-forward decoupling terms.

Simplified Model of the CHB in the Rotating (d, q) Frame

Under the assumption that the H-bridges are identical and have equal capacitor voltages, an N-cell cascaded H-bridge converter in rectifying configuration can be modelled by the simplified equivalent circuit shown in Figure 3.11, in which

N is the number of bridges per phase,

E is the mean capacitor voltage,

s_x is the switching function of phase-x, which can take integer values between $-N$ and N, and

u_x is the instantaneous supply voltage of phase-x.

In this model, the d.c. sides of all the bridges are combined into a single d.c. circuit and the capacitor voltage, $3NE$, is the sum of all the capacitor voltages in all of the cells of the converter. Notice that, apart from the $3N$ multiplier on the d.c.-link voltage, Figure 3.11 is of the form that might be used to model a three-phase, two-level inverter operating in synchronism with the supply [83]. By combining all the capacitor voltages into a single d.c. link and using the average of the capacitor voltages, E, as a gain acting on the a.c. switching functions, the effect of capacitor voltage ripple is neglected. Hence this model is suitable for designing controllers but not for studying the detailed behaviour of the circuit topology.

Inspection of Figure 3.11 allows the simplified model to be expressed mathematically. The following equation is derived from the d.c. side of the equivalent circuit:

$$\frac{\mathrm{d}E}{\mathrm{d}t} = \frac{1}{3NC}(i_a s_a + i_b s_b + i_c s_c) - \frac{E}{RC}. \tag{3.6}$$

For each phase $x \in \{a, b, c\}$, the dynamics of the a.c. side are given by the following equation:

$$\frac{\mathrm{d}i_x}{\mathrm{d}t} = \frac{1}{L}(u_x - E s_x - R_{ac} i_x). \tag{3.7}$$

In the stationary (α, β) reference frame, the equations for the a.c. side (3.7) become

$$\frac{\mathrm{d}\vec{i}}{\mathrm{d}t} = \frac{1}{L}(\vec{u} - E\vec{s} - R_{ac}\vec{i}) \tag{3.8}$$

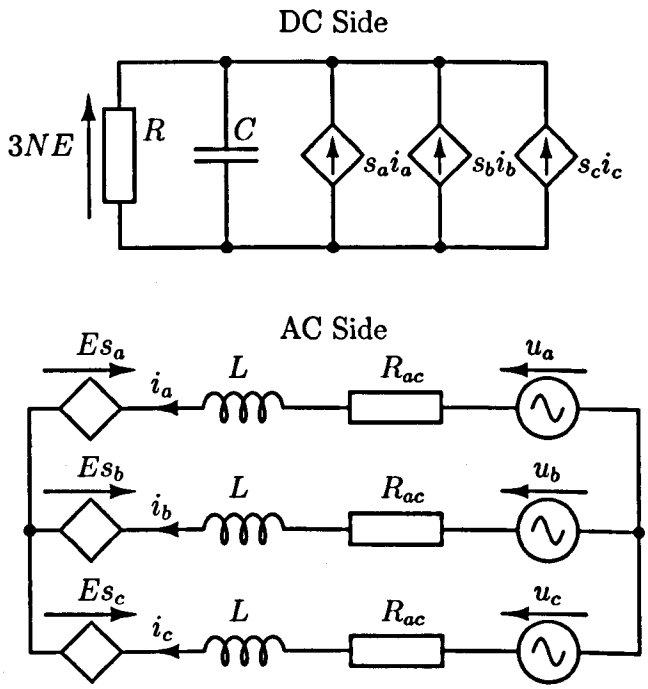


Figure 3.11: Simplified equivalent-circuit model of N-cell cascaded H-bridge in rectifying configuration

and, because the expression

$$s_a i_a + s_b i_b + s_c i_c$$

is the scalar product of the switching-function vector and the current vector in (a, b, c) co-ordinates, the equation for the d.c. side is given by (3.9):

$$\frac{\mathrm{d}E}{\mathrm{d}t} = \frac{2}{9NC}(\vec{s} \cdot \vec{i}) - \frac{E}{RC}, \tag{3.9}$$

where $(\vec{s} \cdot \vec{i})$ is the scalar product of the switching function vector and the current vector.

The extra factor of $\frac{2}{3}$ in the first term of (3.9) compared with (3.6) arises because the determinant of the transformation matrix in (3.2) is not unity: the scalar product in the (α, β) frame is $\frac{3}{2}$ times the scalar product in the (a, b, c) frame. Notice that even after the a.c. quantities have been converted to vectors, the d.c. parts of the circuit remain as scalar quantities.

After changing the reference frame from the stationary frame to the rotating (d, q) frame the a.c. equation (3.8) becomes

$$\frac{\mathrm{d}\vec{i}_{dq}}{\mathrm{d}t} = \frac{1}{L}\vec{u}_{dq} - \frac{E}{L}\vec{s}_{dq} - \left(j\omega + \frac{R_{ac}}{L}\right)\vec{i}_{dq} \tag{3.10}$$

where the $j\omega$ term is a cross-coupling term resulting from the rotation of the reference frame given in (3.5). On the d.c. side, the transformation to the rotating frame does not affect the scalar product; hence

$$\frac{\mathrm{d}E}{\mathrm{d}t} = \frac{2}{9NC}(\vec{s}_{dq} \cdot \vec{i}_{dq}) - \frac{E}{RC}. \tag{3.11}$$

3.3.2 Controller Design

So far, the $\vec{s}_{dq}$ term in the model has represented the discrete switching vector. To design controllers it more useful to use an averaged model, for which the average of the switching function over each sampling period, $\langle\vec{s}_{dq}\rangle$, is substituted in place of $\vec{s}_{dq}$. $\langle\vec{s}_{dq}\rangle$ is effectively the vector of the three-phase modulation index in the (d, q) frame and is a continuous vector. The simplified average

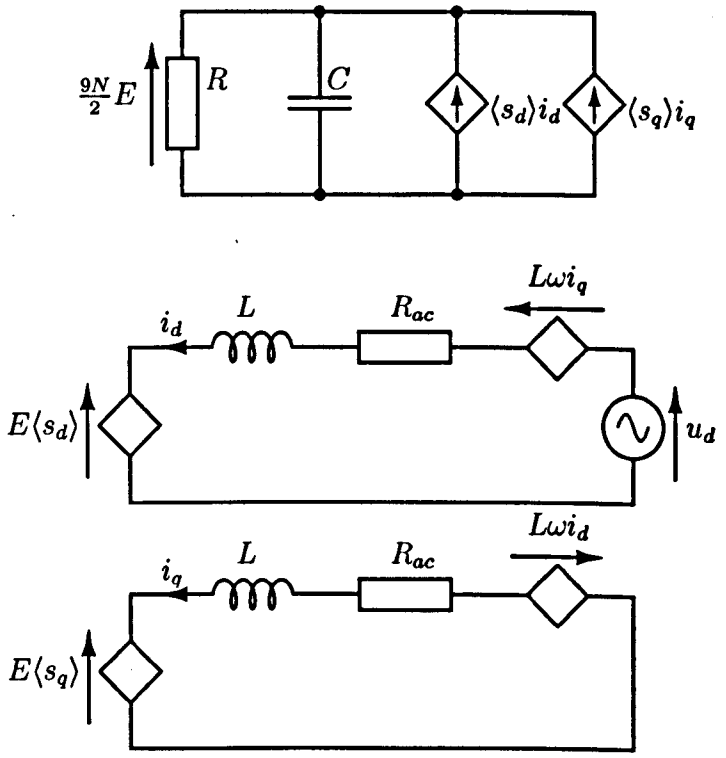


Figure 3.12: Simplified, averaged model of N-cell cascaded H-bridge in the rotating (d, q) reference frame

model is represented by the (d, q) equivalent circuit shown in Figure 3.12.

Operating Point

This equivalent circuit model, despite being simplified, is non-linear because it contains products of states: $E\langle \vec{s}_{dq} \rangle$ on the a.c. side and $\langle \vec{s}_{dq} \rangle \cdot \vec{i}_{dq}$ on the d.c. side. To apply classical control methods to the system the model must be linearized around a steady-state operating point, giving (3.12)

$$\frac{\mathrm{d}}{\mathrm{d}t}(\Delta\vec{i}_{dq}) = \frac{1}{L}(\Delta\vec{u}_{dq} - E_0\Delta\vec{s}_{dq} - \vec{s}_0\Delta E) - (j\omega + \frac{R_{ac}}{L})\Delta\vec{i}_{dq} \tag{3.12a}$$

$$\frac{\mathrm{d}}{\mathrm{d}t}(\Delta E) = \frac{2}{9NC}(\vec{s}_0 \cdot \Delta\vec{i}_{dq} + \vec{i}_0 \cdot \Delta\vec{s}_{dq}) - \frac{\Delta E}{RC} \tag{3.12b}$$

where the subscript 0 represents an operating point and Δ represents a small deviation from that operating point.

A suitable operating point can be derived by analysing the circuit shown in Figure 3.11 in steady-state operation. Analysing the equivalent circuit in this way, and also assuming that the converter should be controlled to give unity displacement power factor, gives the following equation for s_{d0}.

$$s_{d0}^2 - s_{d0}\frac{u_d}{E_0} + \frac{R_{ac}}{R}\frac{9N}{2} = 0$$

The important parameters are therefore

- the ratio of supply-voltage vector to d.c.-link voltage $\frac{u_d}{E_0}$,
- the number of H-bridge cells and
- the ratio of resistances on the a.c. and d.c. sides of the circuit.

The steady-state current can be calculated from the d.c. side of the circuit:

$$i_{d0} = \frac{9NE}{2Rs_{d0}}$$

and s_{q0} can be calculated to enforce zero q-axis current:

$$s_{q0} = -\frac{L\omega i_{d0}}{E}.$$

For the purposes of designing controllers, two operating points are considered: one placing the converter under light load and one under heavy load. The component values, of which only the d.c.-side resistance is changed between the two conditions, are given in Table 3.1 alongside the steady-state operating conditions. The operating conditions are also represented as phasors in Figure 3.13.

Current Controller

In this work, the d and q components of the a.c. current are controlled independently using PI controllers acting on the appropriate components of the

Light Load

Component Values		
R	57	Ω
C	1	mF
L	11	mH
R_{ac}	0.3	Ω

Operating Point		
E_0	100	V
$\vec{u}_0$	300	V
$\vec{i}_0$	3.52	A
$\vec{s}_0$	$2.99 - j0.12j$	

Heavy Load

Component Values		
R	10	Ω
C	1	mF
L	11	mH
R_{ac}	0.3	Ω

Operating Point		
E_0	100	V
$\vec{u}_0$	300	V
$\vec{i}_0$	20.4	A
$\vec{s}_0$	$2.94 - j0.71j$	

Table 3.1: Component values and associated steady-state operating points. Vector quantities are scaled to show their peak a.c. value.

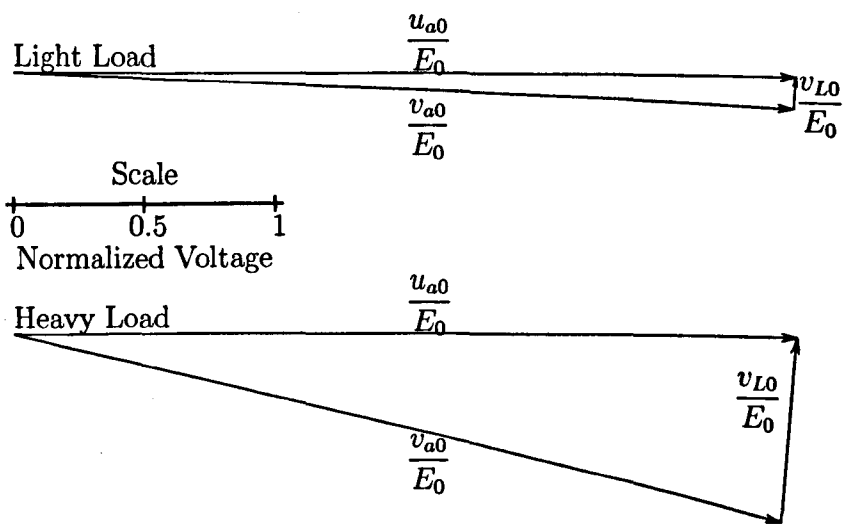


Figure 3.13: Phasor representation of steady-state operating points

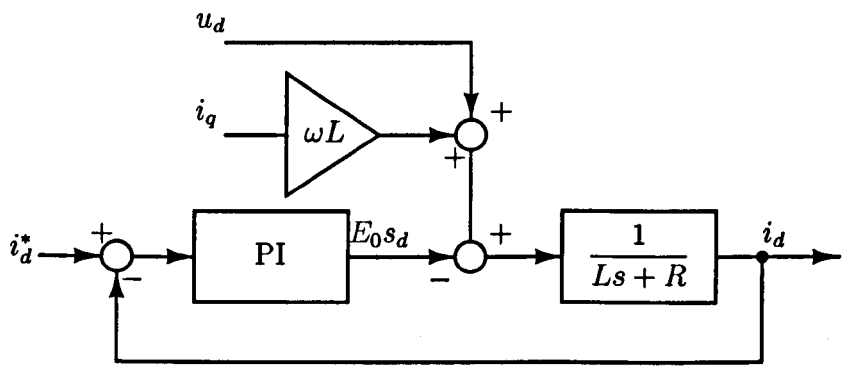


Figure 3.14: i_d current loop

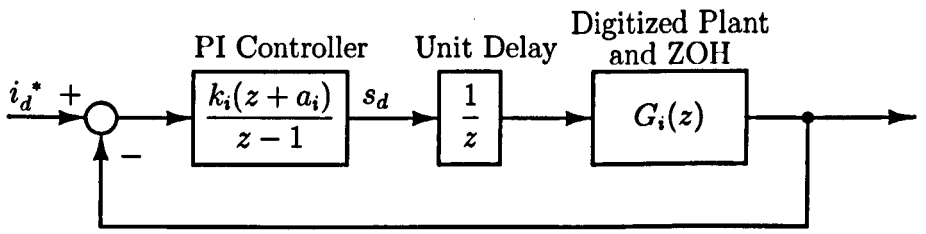


Figure 3.15: Current-control loop in the digital domain

d, q reference vector $\vec{s}^*$. Analysis of (3.12a) suggests the control structure in Figure 3.14 to control i_d using s_d as the control input [83]. The u_d and i_q inputs are fed forward to compensate for the other terms in (3.12a); the term in E is not fed forward because E is controlled by an outer control loop operating more slowly than the current-control loop. An analogous control loop can be derived for the i_q component, although care must be taken to ensure the de-coupling terms use the correct polarity.

The current controller is best designed in the digital domain because, as discussed in section 3.2.2, the outputs of the control system are delayed by one sampling period. This delay has a de-stabilizing effect that can be particularly significant at the low sampling frequency used for low frequency PWM. The delay can be accounted for during the design stage if the controller is designed in the digital domain.

It can be shown that the digitized transfer function of a inductor-resistor circuit, accounting for of a *zero-order hold* at the input [84], is given by the following equation:

$$G_i(z) = \frac{1}{R}\left(\frac{1 - e^{-\frac{R}{L}T}}{z - e^{-\frac{R}{L}T}}\right),$$

where

$G_i(z)$ is the plant transfer function,

R and L are the resistance and inductance respectively and

T is the sampling period.

The component values in Table 3.1 with a sampling frequency of 1500Hz give the following plant transfer function.

$$G_i(z) = \frac{0.06}{z - 0.9820}. \tag{3.13}$$

Figure 3.15 shows the current-control loop including a PI controller, the unit delay and the digitized plant. The system has three open-loop poles:

- a pole at the origin due to the unit delay in the control system,
- a pole at $z = 0.9820$ due to the digitized plant and
- a pole at $z = 1$ due to the integration of the PI controller.

The PI controller also includes a zero, which must be positioned as part of the design process. These open-loop poles and zeros are shown in Figure 3.16.

Also shown in Figure 3.16 is the root locus when the zero of the PI controller has been placed at $z = 0.85$. The zero was placed heuristically to provide a good balance between closed-loop damping ratio and natural frequency. The gain, k_i, of the current controller was set to produce a damping ratio close to 0.7. Any further increase in gain slows the response as the real pole in Figure 3.16 becomes dominant.

Pole	Damping Ratio	Natural Frequency (Hz)
0.63	1.0	109
$0.67 \pm 0.23j$	0.74	111

Table 3.2: Z-domain poles of the current loop

The final closed-loop poles, given in Table 3.2 and shown in Figure 3.16, are produced with the following controller parameters

$$k_i = 6.24, \qquad a_i = -0.85, \qquad T_i = \frac{1}{1500},$$

where k_i and a_i are parameters of the PI controller defined in Figure 3.15 and T_i is the sampling interval of the current controller.

Voltage Controller

The mean capacitor voltage, E, is controlled using another PI controller which regulates the average capacitor voltage using the d component of the a.c. current (Figure 3.17.) The continuous transfer function relating E and i_d is derived from (3.12).

$$G_v(s) = \frac{E(s)}{i_d(s)} = \frac{2s_0}{9N} \frac{R}{RCs + 1}$$

To produce a slower controller, the voltage loop operates at a quarter of the sampling frequency of the current controller. The z-domain root locus of the voltage control loop, including the dynamics of the current-loop at the new sampling rate, is given in Figure 3.18 for both loading conditions.

The parameters of the voltage controller have been selected in order to provide a good compromise between the system behaviour at the two operating conditions considered. The zero of the PI controller is positioned to cancel the plant pole under the more heavily loaded condition and the gain is set to provide good damping at the more lightly loaded condition. The expected closed-loop poles for each loading condition using the following controller pa-

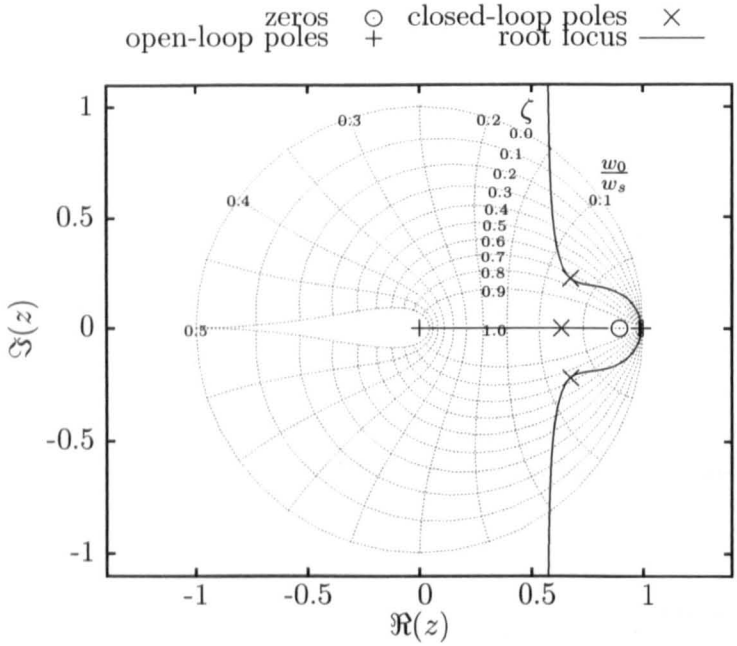


Figure 3.16: Z-Domain root locus for the design of the current controller

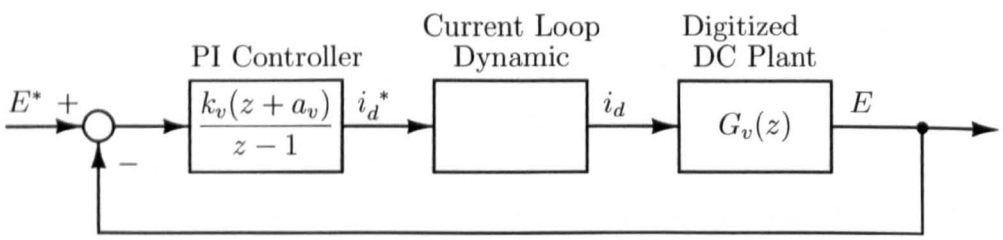


Figure 3.17: Voltage controller in the digital domain

Light Load		
Pole	Damping Ratio	Natural Frequency (Hz)
-0.173	0.49	214
$0.412 \pm 0.457j$	0.50	57
$0.810 \pm 0.208j$	0.58	18

Heavy Load		
Pole	Damping Ratio	Natural Frequency (Hz)
-0.1802	1.0	213
0.376 ± 0.518	0.43	62
0.766	1.0	16
0.745	1.0	18

Table 3.3: Closed-loop poles of voltage control loop under light and heavy load

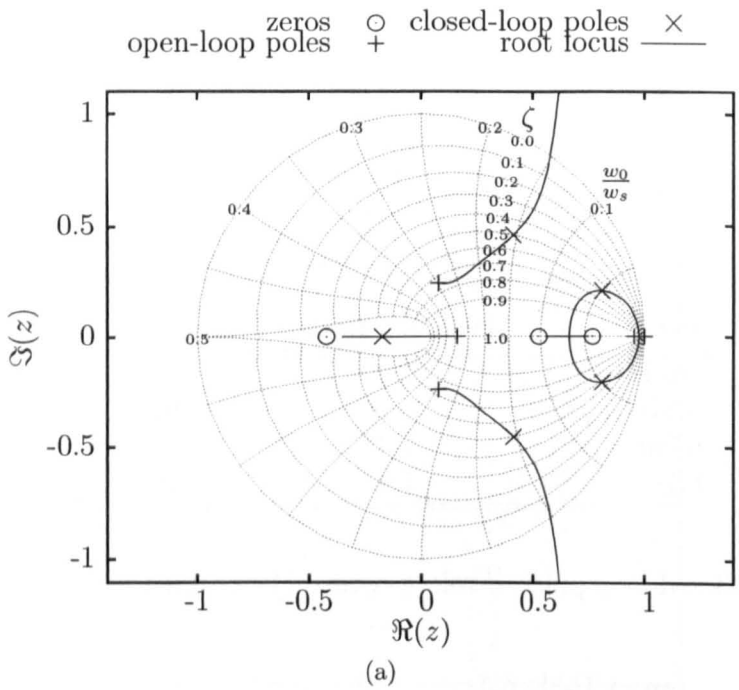
rameters are given in Table 3.3.

$$k_v = \frac{1}{s_0}, \qquad a_v = -\frac{0.766}{s_0}, \qquad T_v = \frac{4}{1500}.$$

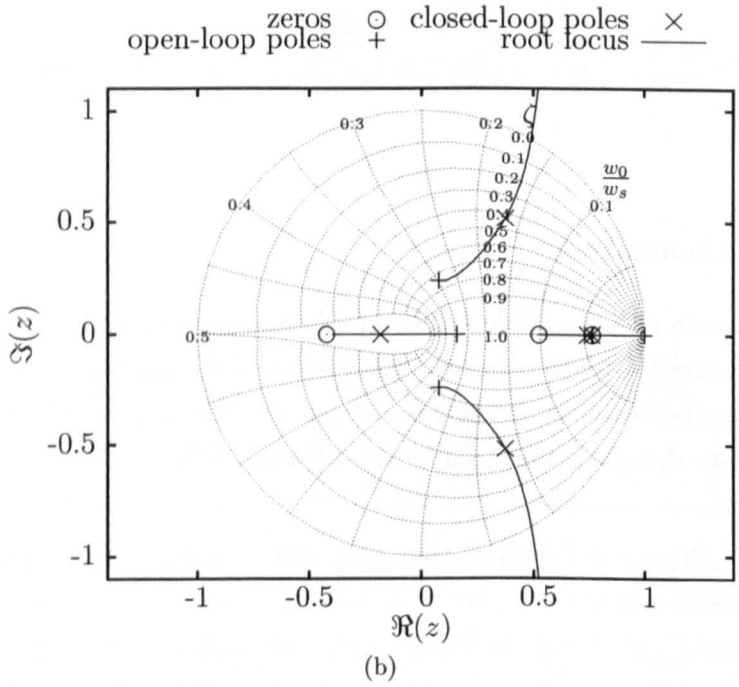
Complete Controller

A block diagram of the complete control scheme is shown in Figure 3.19. The diagram includes blocks to transform the measured signals into the (d, q) frame and the PI controllers for current and voltage control. The feed-forward terms that were introduced in Figure 3.14 are also included for both the d and q current loops.

To verify the control design, the responses of a linear averaged model, a switching model and the experimental converter to a 20% step-change in d.c. voltage demand are shown in Figure 3.20. In each case the systems begin at the steady-state operating conditions given in Table 3.1. Note that the current requirement of the heavily loaded condition is greater than the rating of the experimental converter so the d.c. voltage and the supply voltage have



(a)



(b)

Figure 3.18: Z-Domain root locus for design of voltage controller (a) with low load and (b) with high load

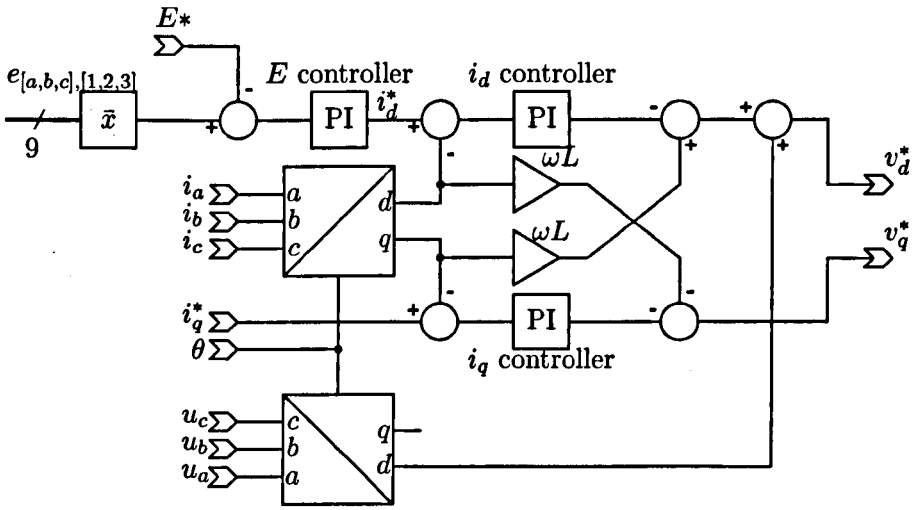


Figure 3.19: Control scheme in d-q frame.

been down-rated by 50% for the experimental test. The results are therefore presented in the per-unit system so that the responses can be compared. The bases of the p.u. system are the capacitor voltage at the initial operating point and the current drawn at that operating point with a 57Ω load on each d.c. link.

In Figure 3.20, the response of the highly loaded condition, $R = 10\Omega$, is shown to be slower in practice than design. The difference is likely to be because the speed of response at the highly loaded condition relies on the zero of the controller cancelling the plant pole (Figure 3.18). It is likely that the plant pole does not cancel exactly in the experimental converter, introducing a slow, dominant pole. Nevertheless, the response time is acceptable and there is no overshoot.

At the lower loading condition, $R = 57\Omega$, the responses of the linear model and the switching model agree. The response of the experimental converter is more damped than the models, which is likely to be because the models do not include properties of the switching devices, such as the voltage drop across the conducting devices. It is possible to produce a better correspondence between the model behaviour and the actual system behaviour, and even to design better controllers, by developing a more detailed model. However, the

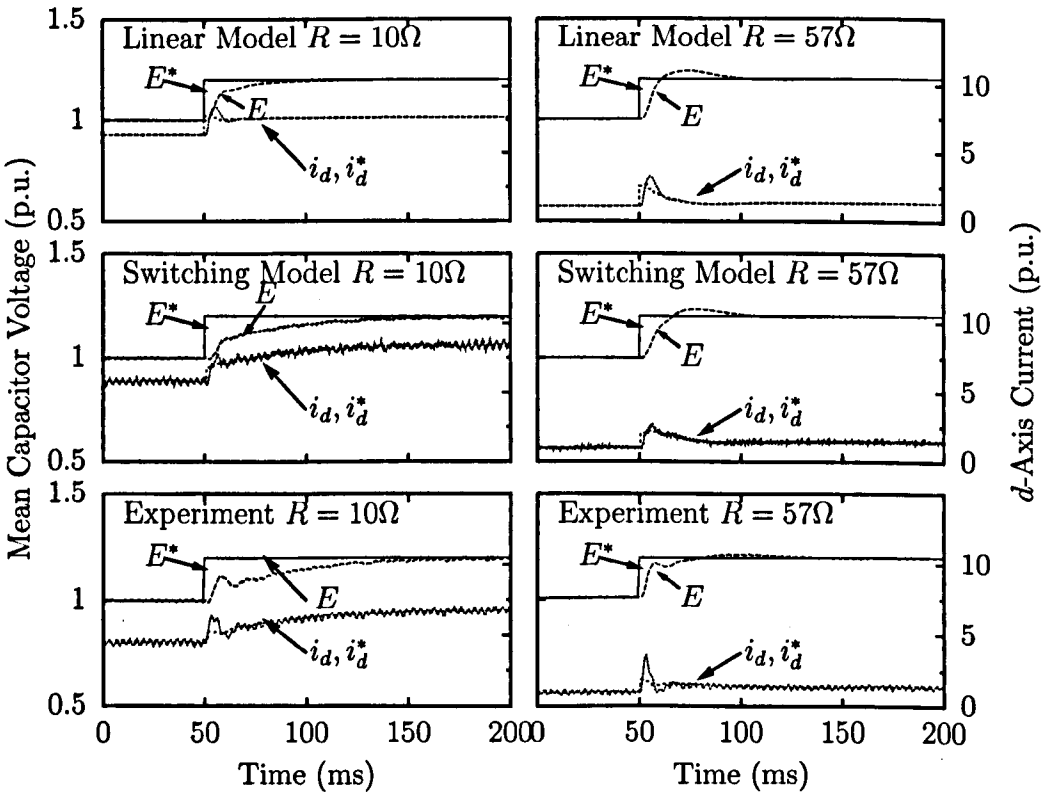
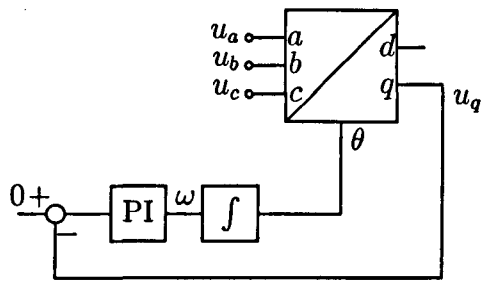
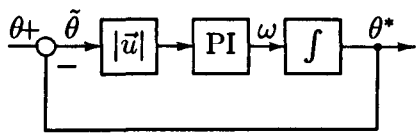


Figure 3.20: Response of linear averaged model, a switching model and the experimental converter to step-changes in d.c. voltage demand under two different loading conditions.



(a)



(b)

Figure 3.21: PLL Structures showing (a) (d, q) calculations and (b) linearized for small errors in θ

experimental studies in this thesis investigate the harmonics produced by the modulation in steady-state. The dynamic performance is a secondary consideration so the controllers do not require further optimization for this work.

3.3.3 Synchronization to the Supply

Closed-loop control of a grid-connected inverter or rectifier requires accurate synchronization to the grid frequency. In the (d, q) control scheme depicted in Figure 3.19, the co-ordinate transformations require an input of θ, the angle of the supply-voltage vector. Many synchronization methods have been published for single- and three-phase systems [85]. The method used in this work is a three-phase, phase-locked loop (PLL) operating in the (d, q) reference frame [86], which works on similar principles to the rest of the control system. The PLL (Figure 3.21a) functions by adjusting the (d, q) transformation angle to force the q component of the supply voltage to zero so that the transformation is aligned with the supply-voltage vector as in Figure 3.10.

With reference to (3.4), which gives the transformation between the (α, β) and the (d, q) reference frames, the q component of the supply voltage is related to the angle error, $\tilde{\theta}$, as follows:

$$\begin{aligned} u_q &= -u_\alpha \sin(\theta^*) + u_\beta \cos(\theta^*) \\ &= -|\vec{u}| \cos(\theta) \sin(\theta^*) + |\vec{u}| \sin(\theta) \cos(\theta^*) \\ &= |\vec{u}| \sin(\theta - \theta^*) \\ &= |\vec{u}| \sin(\tilde{\theta}), \end{aligned}$$

where

θ is the angle of the supply-voltage vector in the stationary reference frame shown in Figure 3.10,

θ^* is the angle used in the transformation and

$\tilde{\theta}$ is the error in the angle used for the transformation.

Hence, for small angle errors

$$u_q \simeq |\vec{u}|\tilde{\theta}.$$

The (d, q) transformation block in Figure 3.21a can then be replaced by a summing junction and a gain, giving a linearized model of the PLL (Figure 3.21b), which can be used to design the parameters of the PI controller used in the PLL. The continuous root locus of the linearized system with controller parameters $k = 296$ and $a = 222$ is shown in Figure 3.22. This produces a system with a natural frequency of 40Hz and a damping ratio of 0.7. The bandwidth is deliberately low to prevent the PLL from tracking harmonics in the lab supply.

Unusually for a control system, both the PI controller and the integrator plant must be implemented digitally as there is no real plant in the system. The integrator and PI controller can be implemented using a single difference equation but it is convenient to keep the roles of integrator and controller separate. Doing so allows both the angular frequency, ω, and the angle, θ, to be extracted from the PLL.

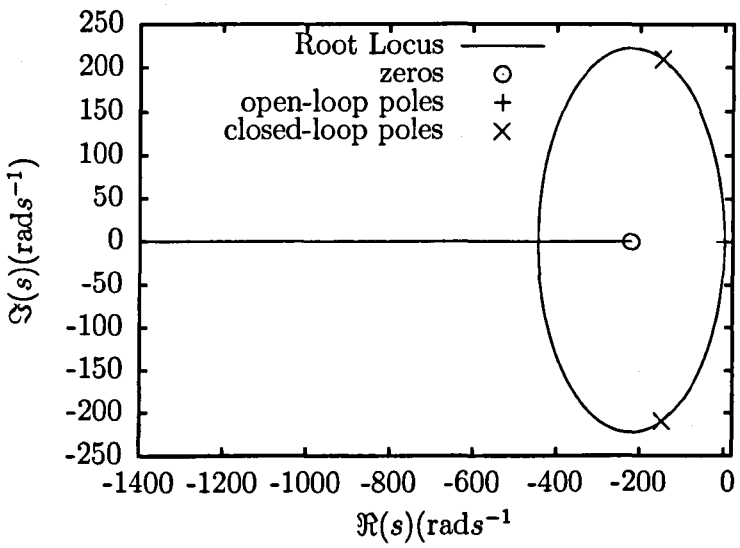


Figure 3.22: Continuous root locus of PLL system, with controller parameters $k = 296$ and $a = 222$

The PI controller can be discretized using the *backward differential* method [87], which gives the following z-domain transfer function and difference equation with a sampling frequency of 1500Hz.

$$G_c(z) = \frac{296z - 252}{z - 1} \tag{3.14}$$

$$\omega_k = \omega_{k-1} + 296\tilde{\theta}_k - 252\tilde{\theta}_{k-1} \tag{3.15}$$

In the difference equation

w is the calculated angular frequency,

$\tilde{\theta}$ is the error in transformation angle

and the subscripts k and $k-1$ indicate values calculated during the present and previous sampling intervals respectively.

The integration can be performed numerically using the following difference equation:

$$\theta_{k+1} = \theta_k + T_s\omega_k.$$

The output of the integration is an estimate of the supply angle at the next

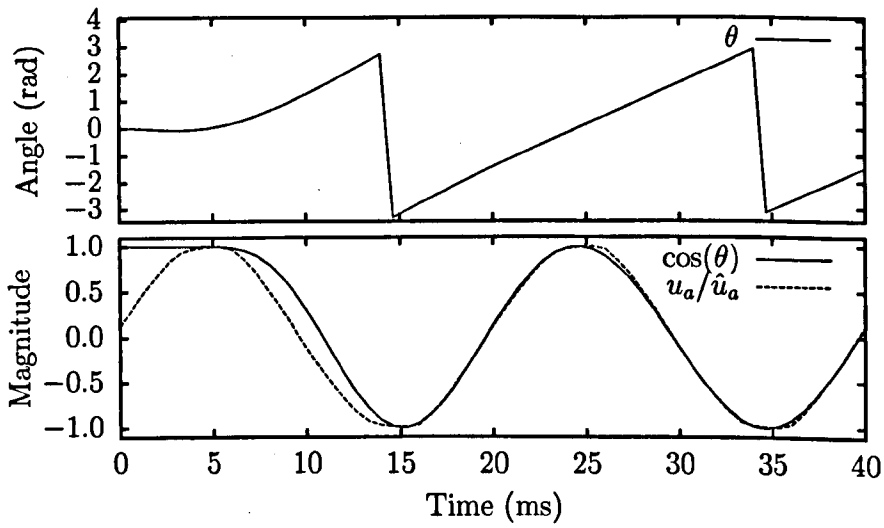


Figure 3.23: Synchronization of PLL to lab supply

sampling instant, which is useful in light of the delay of one sampling period introduced by the control architecture used in the experimental converter (see section 3.2.2.)

At each sampling instant, the control laws are calculated with (d, q) variables derived using the supply angle at that instant, θ_k. The output of these control laws is another vector in the (d, q) domain, which must be returned to the stationary frame before being applied to the converter. The delay of one sampling period between the vectors being calculated and applied to the converter introduces an error if θ_k is used to transform back to the stationary frame because the supply angle will have moved on to θ_{k+1} by the time the vectors are applied. This error can be avoided by using θ_k to convert variables into the rotating frame and then converting the demanded voltage vector back to the stationary frame using using θ_{k+1}, which is naturally produced by the PLL algorithm.

Figure 3.23 shows the behaviour of the PLL as it synchronizes to the lab supply.

3.4 Methods for Spectral Analysis of Results

Good quality frequency spectra are required in order to analyse and compare PWM methods. Depending on the type of signal being analysed, one of two methods is applied in this thesis to generate frequency spectra. Data samples obtained from a digital-storage oscilloscope are spaced equally in time so are suited to the discrete Fourier transform. Care must be taken over the duration of data analysed to avoid spectral leakage, as discussed in section 3.4.1.

It is also useful to analyse the spectra of the demanded switching functions. These signals consist of sequences of switching states applied for known durations and are not sampled at regular intervals. An alternative method, described in section 3.4.2, is applied to these signals.

3.4.1 Synchronized DFT

To avoid spectral leakage and to aid in the comparison of results, signals analysed using the discrete Fourier transform (DFT) must contain as close as is possible to a whole number of fundamental cycles.

The following procedure is used throughout this work to analyse the frequency spectra of experimental results:

1. The oscilloscope is set to a fixed sampling interval for a duration of 0.1s: approximately five fundamental cycles.

2. The supply frequency is calculated by the PLL algorithm while the rig operates and the time taken to complete four cycles is subsequently extracted from the DSP's memory.

3. The oscilloscope trace is truncated to this duration so that the remaining data contains four complete cycles. Four cycles has been chosen because if the supply is operating just below the nominal 50Hz the complete fifth cycle will not be available in the 0.1s oscilloscope trace.

As an example, Figure 3.24 shows two spectra obtained from the same data set when, according to the PLL calculations, the supply was operating

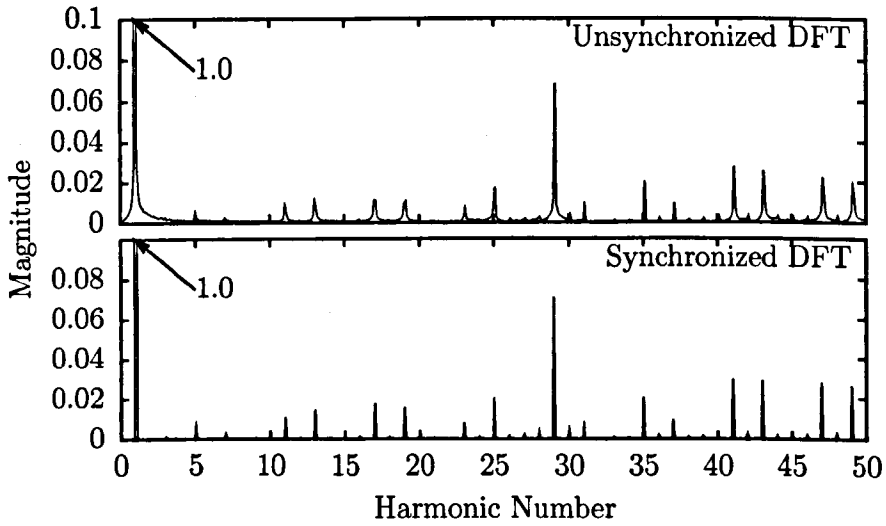


Figure 3.24: Spectrum produced using synchronized and unsynchronized DFT

at 50.15Hz. The first example, which was calculated using the entire oscilloscope trace, exhibits leakage in the spectrum as individual peaks are spread between neighbouring harmonics and sub-harmonics. The leakage around the fundamental component is of particular concern as it is important to identify which low frequency harmonics really exist. The extent of the spectral leakage depends on the exact supply frequency at the time that the results were taken, making it difficult to compare results. The peaks of the second spectrum in Figure 3.24, which was calculated from the truncated oscilloscope trace, are less spread out and tend to have greater amplitudes, more clearly representing the properties of the analysed waveform and making it possible to compare results taken at different times.

3.4.2 Multiple pulses

As well as analysing output voltage waveforms, it is useful to analyse the spectrum of the switching functions demanded by the modulator. When the switching states and corresponding time-periods are scheduled in the FPGA's FIFO register they can be stored for later analysis in the memory of the DSP. The stored data include lists of switching states and time periods, which are not

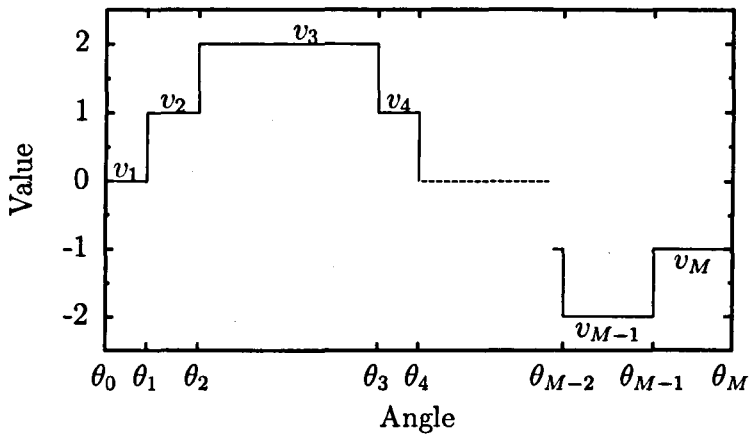


Figure 3.25: One cycle of an arbitrary periodic signal comprising multiple constant pulses.

regularly sampled so are not well suited to analysis using the discrete Fourier transform. Instead, an alternative method is applied, known as the method of *multiple pulses* [88], [89]. The derivation of this method, which is very similar to the description of PWM required to set up the selective harmonic elimination problem, is given below.

One cycle of a periodic signal consisting of M constant pulses is shown in Figure 3.25. The Fourier coefficients of the signal can be constructed based on the superposition of the Fourier series of each pulse. Hence, using the conventional notation

$$f(\theta) = \frac{a_0}{2} + \sum_{n=1}^{\infty} \left[a_n \cos(n\theta) + b_n \sin(n\theta) \right].$$

The Fourier coefficients of a periodic waveform with M switching edges per cycle are given by

$$\begin{aligned} a_n &= \frac{1}{\pi} \sum_{m=1}^{M} \int_{\theta_{m-1}}^{\theta_m} v_m \cos(n\theta) \mathrm{d}\theta \\ &= \frac{1}{\pi} \sum_{m=1}^{M} \frac{v_m}{n} \left[\sin(n\theta_m) - \sin(n\theta_{m-1}) \right] \end{aligned} \tag{3.16}$$

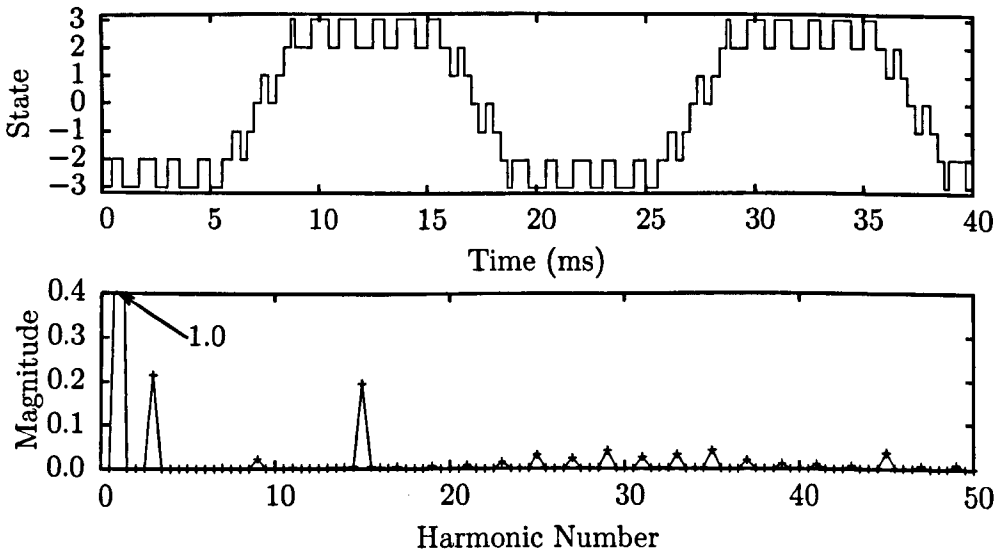


Figure 3.26: Single-phase switching function and its spectrum calculated using the multiple pulses method

and

$$b_n = \frac{1}{\pi}\sum_{m=1}^{M}\int_{\theta_{m-1}}^{\theta_m} v_m \sin(n\theta)\mathrm{d}\theta$$
$$= \frac{1}{\pi}\sum_{m=1}^{M}\frac{v_m}{n}\left[\cos(n\theta_{m-1}) - \cos(n\theta_m)\right]. \qquad (3.17)$$

These summations are easily calculated for signals with a moderate switching frequency.

By way of example, consider the switching function shown in Figure 3.26. This is a switching function for two cycles extracted from the memory of the DSP. The function is defined in terms of a starting value, an ending value and the location of 80 switching edges in between. The spectrum up to the 50^{th} harmonic, calculated using the *multiple pulses* method, is also shown.

To apply a discrete Fourier transformation to the switching function, the data must be re-sampled into a form giving the value of the function at fixed time intervals. To avoid losing resolution of the position of the switching edges, the re-sampled time step must be equal to the resolution of the signal used

to generate the pulses: in this case 100ns, corresponding to a 10MHz clock signal controlling the timers in the FPGA. Hence, the re-sampled function would consist of 400,000 data points representing a function which is already precisely defined with only 80 points.

3.5 Summary

This chapter has discussed a range of techniques which are employed throughout this thesis, including the structure of simulations, the operation of the experimental converter, design of controllers and means to analyse results. Key points from the chapter are summarized below.

- The simulation studies and the experimental work are concerned with a three-phase cascaded H-bridge converter containing three cells per phase.
- The computer models and the experimental converter can be configured to operate in open loop as an inverter or in closed-loop as a controlled rectifier.
- In addition, the simulated converter can operate with ideal and constant d.c.-link voltages.
- A control system has been developed for the rectifying mode based on a model of the converter in the (d, q) reference frame.
- A PLL has been designed allowing the modulation to be synchronized to the supply voltage.
- Methods have been described allowing the frequency spectra of switching waveforms to be determined whilst minimizing the effects of spectral leakage.

Chapter 4

Space-Vector Modulation with Ideal d.c. Voltage Sources

Space-vector modulation is normally implemented under two key assumptions: that the d.c. voltage sources are constant and equal [63], [65] and that the modulation sampling rate is very rapid [90]. In this chapter, the assumption of ideal voltage sources is maintained but the sampling frequency is reduced as far as is possible whilst still performing continuous space-vector modulation.

Section 4.1 contains a detailed description of the basic space-vector modulation algorithms adopted in this work. Although the algorithms are largly unchanged from existing literature, the wide variety of published modifications to space-vector modulation (for example [56], [65], [67], [91], [92]) make it essential to precisely define the implementation used.

Once the basic algorithm is defined, section 4.2 discusses the requirements of grid-connected applications. Specifically, the requirements for synchronous modulation and for low switching frequencies are considered. In light of these requirements, the basic space-vector algorithm is altered in order to precisely define the choice of states when consecutive samples are not close together in the space-vector diagram.

The behaviour of the space-vector modulation algorithm is studied in section 4.4 for a seven-level cascaded H-bridge across a range of modulation index. At the low sampling rate chosen, the timing of the sampling process is shown

to influence the distortion of the line voltages so a new method is presented to adjust the sampling instants to avoid operating conditions that produce high distortion. The methods are verified experimentally in Section 4.5.

4.1 Fundamentals of Space-Vector Modulation

4.1.1 Definition of Space-Vectors

A space vector is the encapsulation of a three-phase quantity into a single vector in the (α, β) co-ordinate space. The representation of three-phase quantities in the (α, β) plane was described in relation to modelling of the cascaded H-bridge in section 3.3.1. For clarity, the transformation from (a, b, c) co-ordinates to (α, β) co-ordinates is repeated here for the arbitrary three-phase quantity y.

$$\vec{y} = y_\alpha + jy_\beta = y_a + y_b e^{j\frac{2\pi}{3}} + y_c e^{-j\frac{2\pi}{3}} \tag{4.1}$$

Under this convention

- the positive α axis is aligned with the positive a axis,
- balanced, sinusoidal three-phase quantities in sequence (a, b, c) produce vectors of constant magnitude rotating anti-clockwise and
- the magnitude of the rotating vector representing a steady-state three-phase quantity is $\frac{3}{2}$ times the peak magnitude of the phase quantity.

4.1.2 Switching-States as Space-Vectors

If the switching states of a multi-level converter are plotted on the (α, β) plane using (4.1), the states form a hexagon made up of discrete points at the corners of many smaller triangles. These discrete points, shown for a seven-level converter in Figure 4.1, are known as *switching vectors* and, in this work, are denoted by the symbol $\vec{s}$. If all the valid switching states are considered, including the redundant zero-states of each cell, a three-phase cascaded H-bridge with N cells per phase can produce $(12N^2 + 6N + 1)$ switching vectors

using 2^{6N} switching states. In the case of a seven-level converter, $N = 3$ giving 127 switching vectors and 262,144 switching states.

As there are more switching states than switching vectors, some states produce the same switching vector and are said to be redundant. For the cascaded H-bridge, there are two effects that contribute to the redundancy of states. Firstly, in a single-phase leg there are more states (2^{2N}) than there are levels ($2N + 1$). For instance, a leg with three cells can produce the level 2 in six different ways, shown in Table 4.1.

The second form of redundancy is redundancy of the line voltages. Combinations of three-phase states that differ only by their common-mode components produce the same vector on the space-vector diagram. The redundant states caused by this second effect are shown in Figure 4.2 for the first sector of a seven-level converter. In this chapter only the line voltage redundancy is considered so the state of each phase leg is denoted by the output level without consideration of which state is used to produce that level. The redundancy internal to each phase leg remains as an extra degree of freedom to be exploited in Chapter 5.

4.1.3 Modulation Index

There are several definitions of modulation index applicable to the space-vector modulation of multi-level converters. All are the ratio of the reference amplitude to a datum but that datum varies between one of the following:

- the total capacitor voltage;
- the capacitor voltage of a single cell;

Switching States	
(0,0)(0,1)(0,1)	(1,1)(0,1)(0,1)
(0,1)(0,0)(0,1)	(0,1)(1,1)(0,1)
(0,1)(0,1)(0,0)	(0,1)(0,1)(1,1)

Table 4.1: Switching states of a 3-cell phase leg that produce the output level 2 – Each pair of states represents the state of the upper switches of a single cell

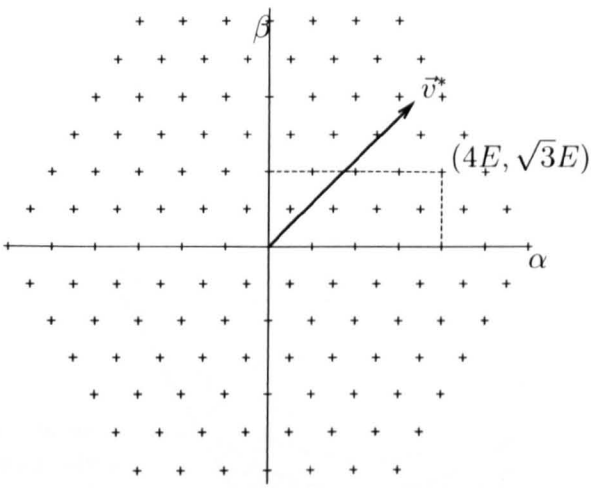


Figure 4.1: Switching vectors of a seven-level converter on the (α, β) plane

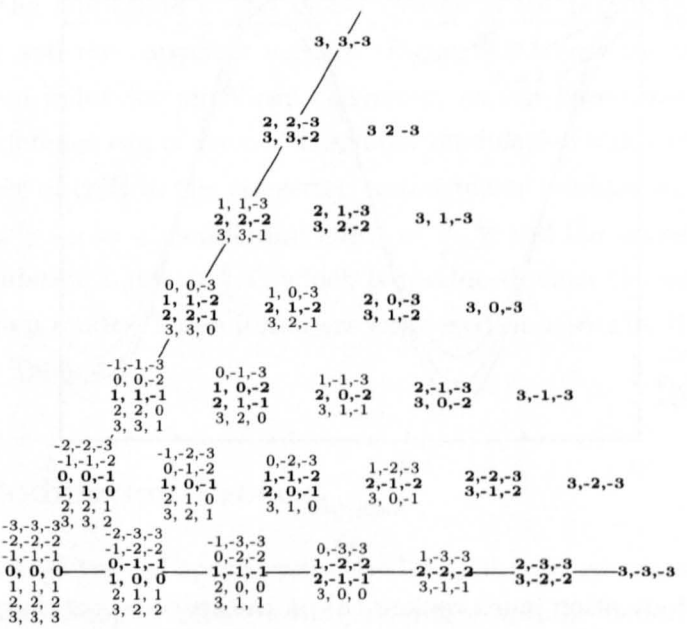
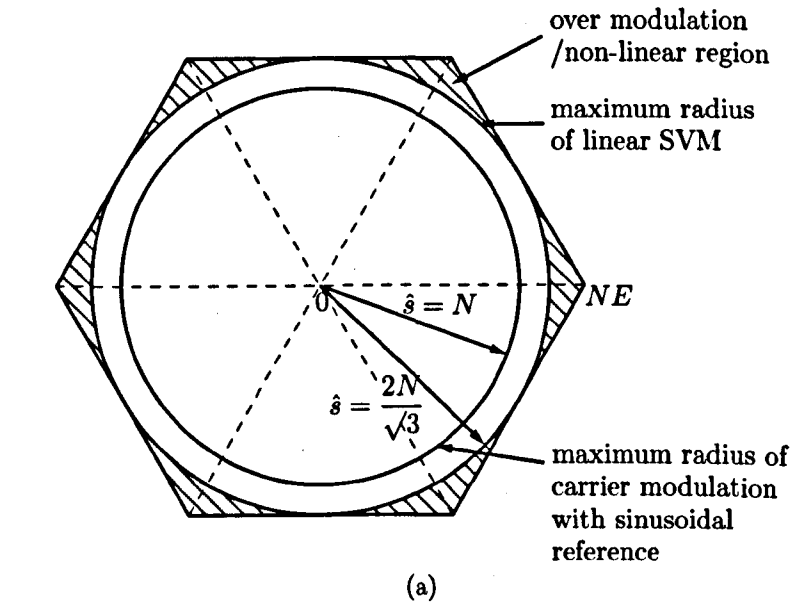
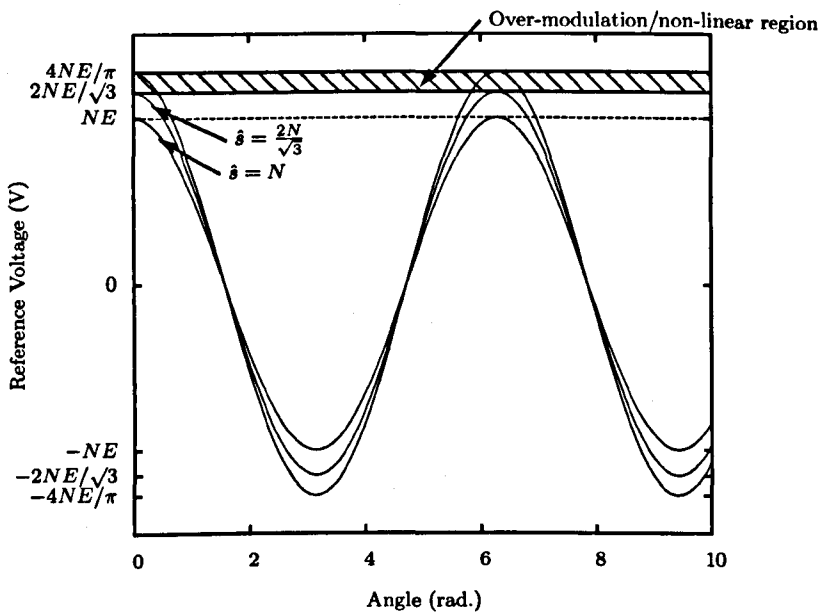


Figure 4.2: Vectors in the first sector and their redundant states



(a)



(b)

Figure 4.3: Modulation index regions (a) on the space-vector diagram and (b) in the time domain

Description	Modulation Index	
	N-Cell	3-Cell
Max. possible	$\frac{4N}{\pi}$	3.8197
Max. linear region	$\frac{2N}{\sqrt{3}}$	3.4641
Max. carrier modulation	N	3

Table 4.2: Modulation index boundaries for N-cell and 3-cell converters

- the extent of the linear region of space-vector modulation, that is the maximum radius of a circle that can be traced within the space-vector diagram; or

- the maximum possible output of the converter achieved when the converter output steps between the corners of the space-vector diagram.

In this thesis the modulation index, $\hat{s}$, is the ratio of the amplitude of the phase-voltage reference and the nominal cell capacitor voltage. Under this convention the amplitude of the phase voltage is the product of the modulation index and the capacitor voltage. Figure 4.3 shows the possible range of modulation index for an N-cell converter: carrier-based modulation with sinusoidal reference can achieve a maximum modulation index of N, where N is the number of cells in the converter; space-vector modulation can produce output linearly up to a modulation index of $\frac{2}{\sqrt{3}}N$ and the maximum possible output modulation index is $\frac{4}{\pi}N$, which is produced when the converter operates in six-step mode. These limits are expressed numerically for a three-cell converter in Table 4.2.

4.1.4 Modulation Process

The fundamental task of space-vector modulation is to use switching vectors to approximate samples of a rotating reference voltage-vector, such as the reference vector $\vec{v}^*$ shown in Figure 4.1. Discrete switching vectors are applied for time periods obeying (4.2) such that the average voltage vector during a

sampling period is equal to the sample of the continuous reference vector.

$$T_s \sum d_n \vec{s}_n = T_s \vec{v}^* \qquad \sum d_n = 1, \tag{4.2}$$

In (4.2)

$\vec{s}_n$ is the n^{th} switching vector applied during the sampling period,

d_n is the proportion of the sampling period for which $\vec{s}_n$ is applied and

T_s is the sampling period.

The space-vector modulator must perform three operations:

1. Select the vectors to apply.
2. Calculate the durations for which the vectors should be applied.
3. Select the redundant states used to produce the chosen vectors and the sequence in which they should be applied.

The optimization of these choices to minimize harmonic distortion of the synthesized voltage waveforms, whilst simultaneously minimizing the number of commutations produced at a given sampling frequency, has been the focus of research [56]. It is now conventional for a reference vector to be synthesized using the nearest three vectors in such a way that each phase leg commutates once for each sequence [54]. This is known as *continuous modulation.* An example of continuous modulation is shown in Figure 4.4 for two consecutive samples of the reference vector. To synthesize $\vec{v}_1^*$ in the figure, the selected vector steps around the vertices of the triangle starting from the state $(2, -2, -3)$ and ending on the state $(3, -1, -2)$, which is a different redundant state of the first vector. The following sequence, which synthesizes the vector $\vec{v}_2^*$, follows the same sequence in reverse with re-calculated duty cycles, ending on state $(2, -2, -3)$. Re-calculating the time-periods between the forward and reverse sequences improves the cancellation of harmonics in a similar manner as the asymmetrical sampling of carrier-based modulation discussed in Chapter 2.

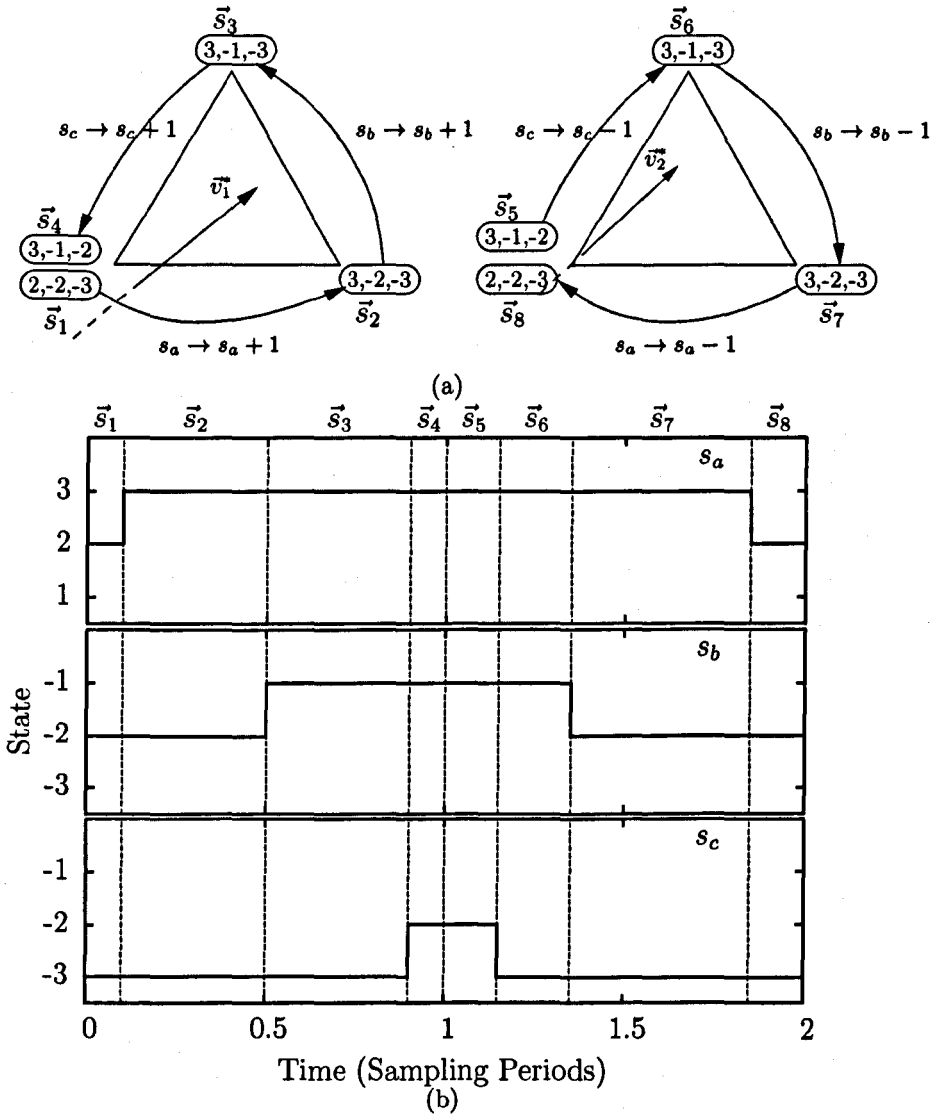


Figure 4.4: Example switching states synthesizing two adjacent reference vectors in the same triangle, shown (a) in a single triangle from the space vector diagram and (b) in the time domain.

For further reduction in distortion, the time period for the first and last vector in each sequence is split evenly between the two redundant states [56], [64]. For example, in Figure 4.4 the vector $\vec{s}_1$ is applied for the same period as $\vec{s}_4$ and $\vec{s}_5$ is applied for the same time period as $\vec{s}_8$.

4.1.5 Identifying the Nearest Three Vectors

Identifying the nearest three switching vectors using the (α, β) co-ordinate system is not straightforward because the available vectors have irrational co-ordinates, as shown for a single example in Figure 4.1. An alternative co-ordinate system was presented in [63], which simplifies the process by giving the switching vectors integral co-ordinates. To achieve this, two axes 60° apart, denoted g and h, are used and the output is normalized with respect to the d.c. voltage (Figure 4.5). Nearby vectors can be easily identified in this (g, h) co-ordinate system using simple rounding operations on the co-ordinates of the reference vector. The rounding operators are defined as follows:

$$\begin{aligned} \lfloor x \rfloor &= \text{floor}(x) \\ \lceil x \rceil &= \text{ceil}(x) \\ \text{frac}(x) &= x - \lfloor x \rfloor. \end{aligned}$$

The transformation from the (α, β) to the (g, h) co-ordinate systems can be derived with reference to Figure 4.6. The reference vector, $\vec{v}^*$, is resolved into two components, $\vec{v}_g^*$ and $\vec{v}_h^*$, parallel to the g and h axes respectively. From Figure 4.6

$$\begin{aligned} v_g^* &= \frac{1}{E}\left(v_\alpha^* - \frac{v_\beta^*}{\tan\frac{\pi}{3}}\right) & v_h^* &= \frac{1}{E}\left(\frac{v_\beta^*}{\cos\frac{\pi}{6}}\right), \\ &= \frac{1}{E}\left(v_\alpha^* - \frac{v_\beta^*}{\sqrt{3}}\right) & &= \frac{1}{E}\left(\frac{2v_\beta^*}{\sqrt{3}}\right). \end{aligned} \tag{4.3}$$

It is also useful to convert directly from a reference expressed in terms of

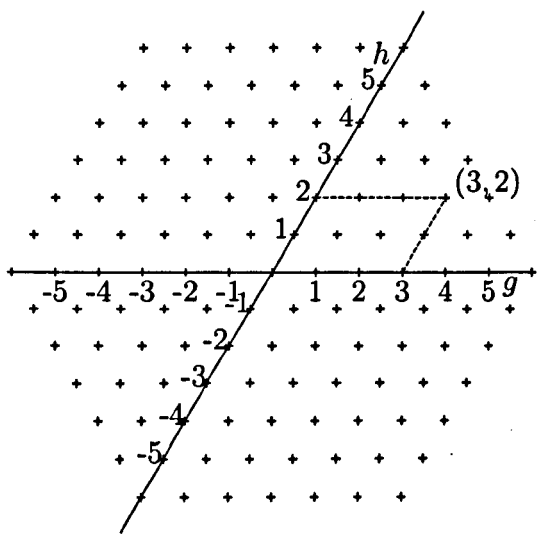


Figure 4.5: Switching vectors in terms of (g, h) axes

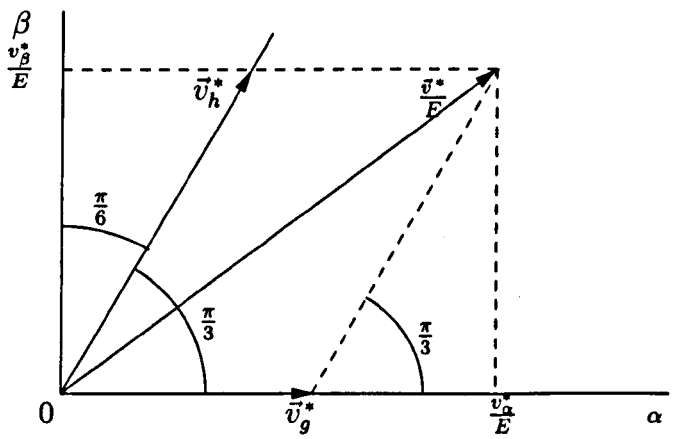


Figure 4.6: Conversion of a reference vector from (α, β) co-ordinates into the (g, h)

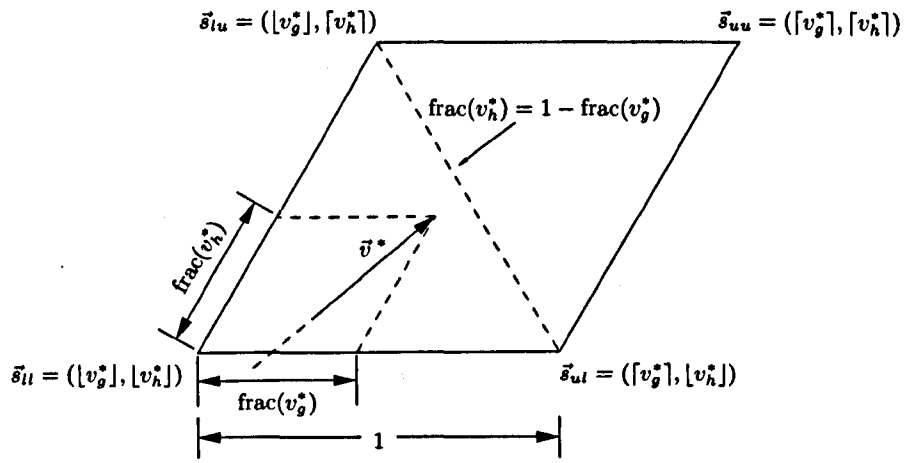


Figure 4.7: Identification of the three vectors nearest to the reference

natural (a, b, c) values, in which case substituting (4.1) into (4.3) gives

$$v_g = \frac{1}{E}(v_a - v_b) = \frac{v_{ab}}{E}, \qquad v_h = \frac{1}{E}(v_b - v_c) = \frac{v_{bc}}{E}. \tag{4.4}$$

This result is particularly useful as it shows that the (g, h) representation of the reference vector is simply a normalized version of two of the line-voltage components and is therefore a natural co-ordinate system for three-phase systems.

As the switching states of the converter occur at the lattice points of the (g, h) co-ordinate system, the nearest *four* switching vectors, $\vec{s}_{ll}$, $\vec{s}_{lu}$, $\vec{s}_{uu}$ and $\vec{s}_{ul}$, can be identified easily by rounding the reference co-ordinates, as depicted in Figure 4.7. The vectors $\vec{s}_{lu}$ and $\vec{s}_{ul}$ are always two of the nearest three vectors and the third vector, that is the closest of $\vec{s}_{ll}$ and $\vec{s}_{uu}$, can be identified from the following equation:

$$\vec{s}_3 = \begin{cases} \vec{s}_{ll} & \text{if } \text{frac}(v_h^*) < 1 - \text{frac}(v_g^*), \\ \vec{s}_{uu} & \text{otherwise.} \end{cases} \tag{4.5}$$

The duty cycle is easily calculated using the fractional parts of the co-ordinates.

$$d_{ul} = \begin{cases} \text{frac}(v_g^*) & \text{if } \vec{s}_3 = \vec{s}_{ll} \\ 1 - \text{frac}(v_h^*) & \text{if } \vec{s}_3 = \vec{s}_{uu} \end{cases} \tag{4.6a}$$

$$d_{lu} = \begin{cases} \text{frac}(v_h^*) & \text{if } \vec{s}_3 = \vec{s}_{ll} \\ 1 - \text{frac}(v_g^*) & \text{if } \vec{s}_3 = \vec{s}_{uu} \end{cases} \tag{4.6b}$$

$$d_3 = 1 - d_{ul} - d_{lu} \tag{4.6c}$$

Where d_{ul}, d_{lu} and d_3 are the proportions of the sampling period for which $\vec{s}_{ul}$, $\vec{s}_{lu}$ and $\vec{s}_3$ should be applied.

4.1.6 Choice of Redundant States

As well as the three commutations around the vertices of a triangle during the switching cycles, extra commutations are required as the reference moves from one triangle to the next. Minimizing the number of these commutations across the entire range of modulation depth constrains the choice of redundant states to only include those highlighted in Figure 4.2 or their equivalents in the other sectors [56].

To identify which vectors are used, it is useful to introduce the concept of the *mean state* of a vector, which is the arithmetic mean of all the redundant states that produce a given vector. The mean state of the switching vector $\vec{s}$ is defined as follows:

$$\bar{S}(\vec{s}) = \frac{1}{n} \begin{pmatrix} \sum_{r=1}^{n} s_{ar} \\ \sum_{r=1}^{n} s_{br} \\ \sum_{r=1}^{n} s_{cr} \end{pmatrix} = \begin{pmatrix} \bar{s}_a \\ \bar{s}_b \\ \bar{s}_c \end{pmatrix} \tag{4.7}$$

where

$\vec{s}$ is a given switching vector,

n is the number of redundant states that produce that vector and

s_{xr} is the phase-x component of the r^{th} state.

For vectors with an odd number of redundant states, the mean state is a valid switching state as all the components are integers. For example, Figure 4.2 shows that the switching vector with (g, h) co-ordinates $(3, 1)$ has three redundant states:

$$(1, -2, -3) \qquad (2, -1, -2) \qquad (3, 0, -1).$$

The mean state in this case is $(2, -1, -2)$, which is a valid switching state of the converter. However, the switching vector with (g, h) co-ordinates $(2, 1)$ has four redundant states:

$$(0, -2, -3) \qquad (1, -1, -2) \qquad (2, 0, -1) \qquad (3, 1, 0)$$

The mean state in this case is $(1.5, -0.5, -1.5)$, which is not a valid switching state. Hence, the lower state $S_l(\vec{s})$ and the upper state $S_u(\vec{s})$ are defined as the states obtained from rounding the mean state downwards and upwards respectively. In the example given above, $S_l = (1, -1, -2)$ and $S_u = (2, 0, -1)$.

Figure 4.2 shows that vectors with an odd number of redundant states are produced using only the mean state and vectors with an even number of redundant states are produced using both the lower and upper redundant states either side of the mean state [56]. Restricting the choice of states to this subset allows modulation across the full range of modulation index with the minimum number of additional commutations to step between triangles. The selection of switching states is also made simpler as many states are not considered.

To select switching states for an N-cell converter, it is useful to be able to determine the mean switching state of a vector directly from the (g, h) co-ordinates of that vector. The mean states of all the vectors in the first sector of the space vector diagram are shown in Figure 4.8. Inspection of Figure 4.8 allows (4.8) to be derived, which gives the mapping from (g, h) co-ordinates to

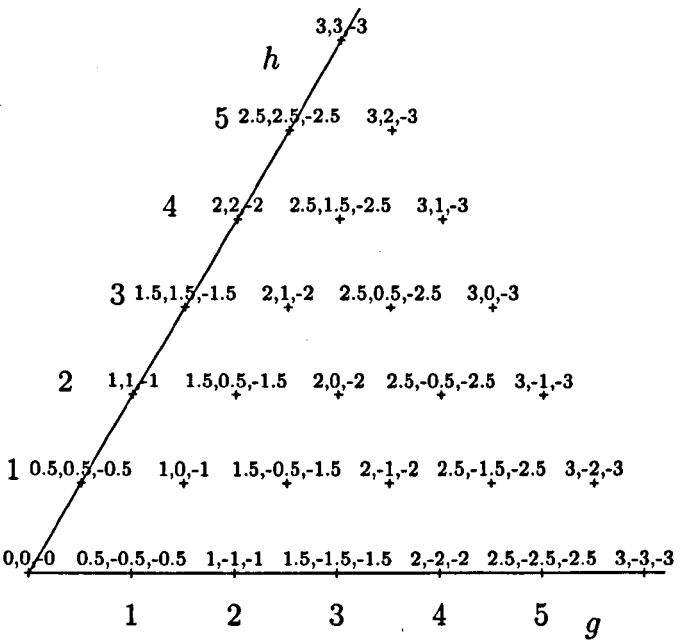


Figure 4.8: Mean states in the first sector

mean states in the first sector.

$$\begin{pmatrix} \bar{s}_a \\ \bar{s}_b \\ \bar{s}_c \end{pmatrix} = \frac{1}{2} \begin{pmatrix} 1 & 1 \\ -1 & 1 \\ -1 & -1 \end{pmatrix} \begin{pmatrix} s_g \\ s_h \end{pmatrix} \tag{4.8}$$

Similar mappings can be derived for the other sectors but it is not necessary because, as will be discussed in section 4.1.8, the modulation is implemented by mapping reference vectors into an equivalent first sector in which (4.8) applies.

4.1.7 Switching Sequences

Once the vectors have been identified the order in which they should be applied remains to be decided. The options depend on the redundant states of the nearest three vectors. In Figure 4.9, which shows two adjacent triangles from the space-vector diagram, triangle A includes one vector with an even number of redundant states and triangle B includes two.

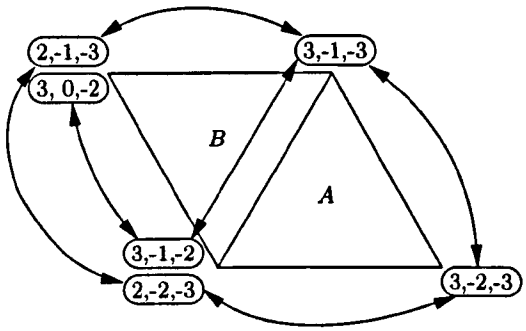


Figure 4.9: Switching sequences for two triangles. Arrows depict state changes that can be made by a single commutation.

Because many switching states have already been eliminated, triangles incorporating only one vector of even redundancy (such as triangle A) offer only one sequence of vectors in which each phase commutates once. In the specific example of triangle A, this sequence is

$$(2,-2,-3) \leftrightarrow (3,-2,-3) \leftrightarrow (3,-1,-3) \leftrightarrow (3,-1,-2).$$

In general, the sequence for such triangles is

$$S_l(\vec{s}_3) \leftrightarrow \bar{S}(\vec{s}_{ul}) \leftrightarrow \bar{S}(\vec{s}_{lu}) \leftrightarrow S_u(\vec{s}_3), \tag{4.9}$$

where $\bar{S}$ is the mean state defined in (4.7) and S_l and S_u are the states obtained when $\bar{S}$ is rounded downwards and upwards respectively.

Triangles incorporating two vectors of even redundancy offer two possible sequences, depending on which of those two vectors is used as the starting vector. For triangle B of Figure 4.9, these sequences are

$$(2,-2,-3) \leftrightarrow (2,-1,-3) \leftrightarrow (3,-1,-3) \leftrightarrow (3,-1,-2)$$

and

$$(2,-1,-3) \leftrightarrow (3,-1,-3) \leftrightarrow (3,-1,-2) \leftrightarrow (3,0,-2).$$

In general, for all triangles containing two vectors of even redundancy the permitted sequences are

$$S_l(\vec{s}_{ul}) \leftrightarrow S_l(\vec{s}_{lu}) \leftrightarrow \bar{S}(\vec{s}_3\ ) \leftrightarrow S_u(\vec{s}_{ul}), \tag{4.10}$$

where the starting vector is $\vec{s}_{ul}$, and

$$S_l(\vec{s}_{lu}) \leftrightarrow \bar{S}(\vec{s}_3\ ) \leftrightarrow S_u(\vec{s}_{ul}) \leftrightarrow S_u(\vec{s}_{lu}) \tag{4.11}$$

where the starting vector is $\vec{s}_{lu}$.

For triangles with an even number of vectors there is a choice of starting vector and it is conventional to start from the vector nearest to the reference sample [56]. A commutation occurs at the sampling instant when changing between starting vectors.

4.1.8 First-Sector Equivalence

The algorithm described so far applies equally across all of the space vector diagram. However, the relationship between a vector and its mean switching state, $\bar{S}(\vec{s})$, which is fundamental to the choice of switching states, varies between the six sectors. The implementation can be simplified by transforming the reference co-ordinates into *first-sector-equivalent* co-ordinates so that the relationship for the first sector can be used throughout. This is achieved most simply by swapping the phase voltages according to Table 4.3 before transforming into (g, h) co-ordinates. The mapping of Table 4.3 produces the first-sector-equivalent axes of Figure 4.10 and causes the equivalent reference to appear to move back and forth within the first sector. Other transformations can be applied [65], [93] to move the reference to the first sector, but the chosen method has the advantage that the forward and reverse transformation are applied simply by swapping over the representation of the phases without performing any explicit calculation.

	Equivalent Phase		
Sector	a_1	b_1	c_1
I	a	b	c
II	b	a	c
III	b	c	a
IV	c	b	a
V	c	a	b
VI	a	c	b

Table 4.3: Phase translations to produce co-ordinates equivalent to the first sector

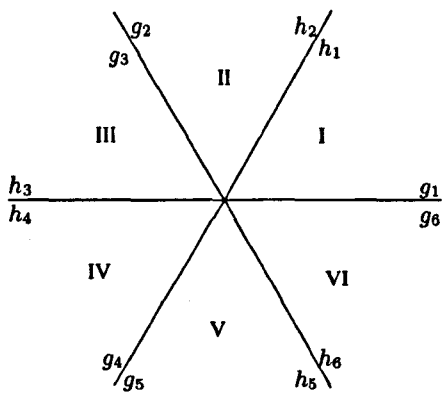


Figure 4.10: First-sector equivalent co-ordinate axes.

4.1.9 Complete Algorithm

The complete algorithm for space-vector modulation, including all the points discussed, is summarized in the flow chart of Figure 4.11. For ease of reference, the blocks of the flow chart refer to the relevant equations from this section.

4.2 Modulation for Grid-Connected Applications

The modulation of grid-connected power converters must be designed to compromise between two, largely conflicting, considerations:

- low switching frequency to reduce losses and
- high quality voltage and current waveforms capable of meeting the strict requirements of grid codes and standards.

Multi-level converters inherently help with this compromise but higher switching frequencies still produce higher losses. Hence it is useful to study the behaviour of modulation schemes at low switching frequencies.

4.2.1 Sequence Reversal

A common rule applied to space-vector modulation for multi-level converters is that once one of the switching sequences of (4.9) to (4.11) has been applied, that same sequence should immediately be applied in the reverse order [54], [56]. This rule is commonly applied in a way that is analogous to symmetric sampled modulation: by calculating the dwell times for the forward and reverse sequence using the same sample of the reference vector [53], [65], [67], [94]. If the reference vector is sampled again after the first sequence, as discussed in section 4.1.4, the resulting modulation is analogous to asymmetric regularly-sampled modulation, which is known to produce better harmonic cancellation than symmetrical regularly-sampled modulation [54].

If the reference sample is updated after the first sequence is applied, it is only appropriate to repeat the same sequence in reverse if both samples occupy

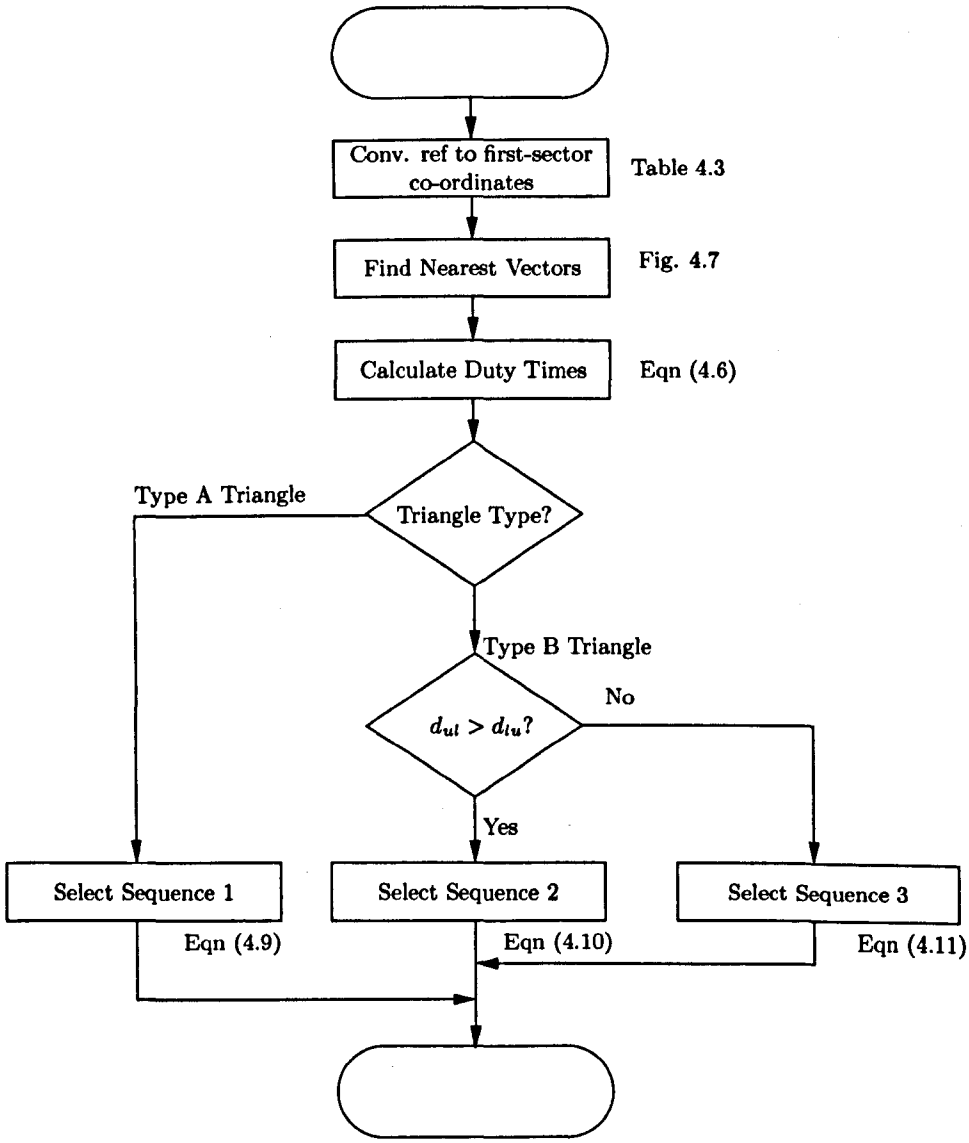


Figure 4.11: Flow-chart of Space Vector Modulation.

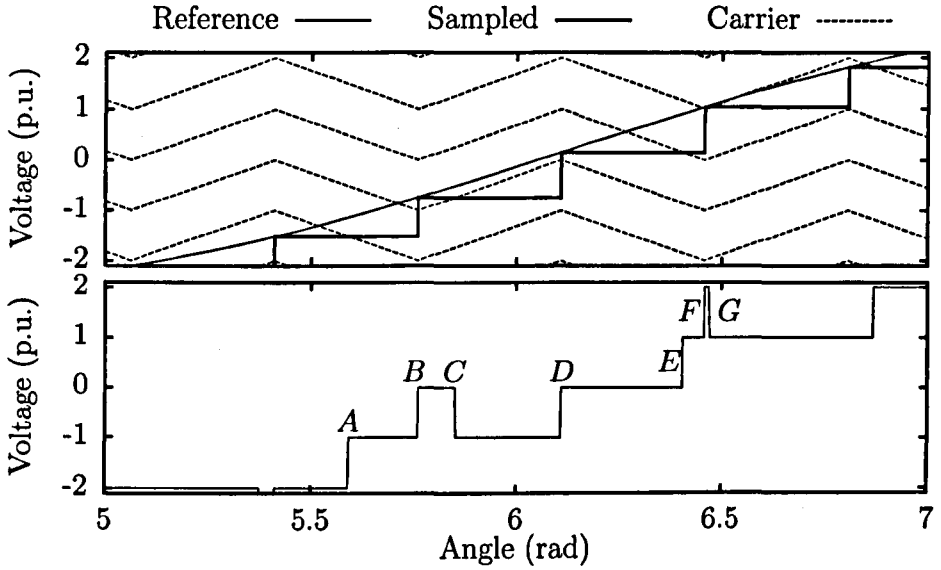


Figure 4.12: Asymmetrically sampled carrier modulation showing the reference moving between levels

the same triangle, as is the case for the example shown in Figure 4.4. At high sampling frequencies consecutive samples are close together in the space vector diagram and often do occupy the same triangle; at low switching frequencies the samples are further apart so such a special case is rare. An explicit rule is therefore needed to define the choice of switching states when adjacent samples do not occupy the same triangle.

To determine the appropriate rule, consider the behaviour of asymmetric regularly sampled level-shifted carrier modulation when the reference moves between levels. In Figure 4.12 the sampled reference signal moves between levels in consecutive sampling periods and the resulting switching edges can be categorized in two ways. Edges labelled A, C, E and G are produced when the horizontal segments of the sampled waveform intersect a carrier wave. It is the positions of these edges that are modulated in order for the converter to produce the correct averaged output. The remaining edges (B, D and F) all occur at sampling instants and are produced when the act of sampling causes a carrier to be crossed. The commutations at the sampling instants are analogous to the commutations required to move between triangles in the

space-vector diagram.

An important observation is that modulated edges in consecutive sampling intervals are always of opposite polarity, irrespective of any additional commutations at the intervening sampling instant. For example, edge A is a rising edge and edge C is a falling edge, despite the presence of edge B between them. The appropriate behaviour for space-vector modulation is therefore to ensure that the sequence of vectors in consecutive sampling intervals produce alternating rising and falling edges, irrespective of the additional commutations required to move to a new triangle.

The sequences of switching vectors (4.9) to (4.11) all begin on the lower redundant state of their respective starting vector, produce positive edges on each of the phase voltages and end on the upper redundant state of the starting vector. Negative edges are produced when any of the sequences are applied in the reverse order. Therefore, in order to produce alternating falling and rising edges, whilst also accounting for the possibility that consecutive samples do not occupy the same triangle, the modulator must adopt the following procedure. First, the appropriate sequence of vectors should be chosen based on the location of the sample in the space-vector diagram, entirely independent of the previous sequence. Then, the order in which the chosen sequences are applied must alternate from one sample to the next. The effect is that if one sequence ends on the upper redundant state of its starting vector, the next sequence begins on the upper redundant state of its starting vector, even if the starting vector has changed. In the special case where two samples do occupy the same triangle, the second sequence will, indeed, be the reverse of the first.

As an example, consider the two vectors marked by $\times$ in Figure 4.13a, which could be synthesized using the sequences depicted, starting from $\bullet$ and ending at $\circ$. The path around the first triangle produces a rising edge on each phase (Figure 4.13b) and the path around the second triangle produces falling edges. There is another commutation in phase b, indicated by the dotted arrow on the space-vector diagram, caused by the movement to the new starting vector. This transition occurs at the sampling instant because the final vector of the first sequence is not a vertex of the second triangle.

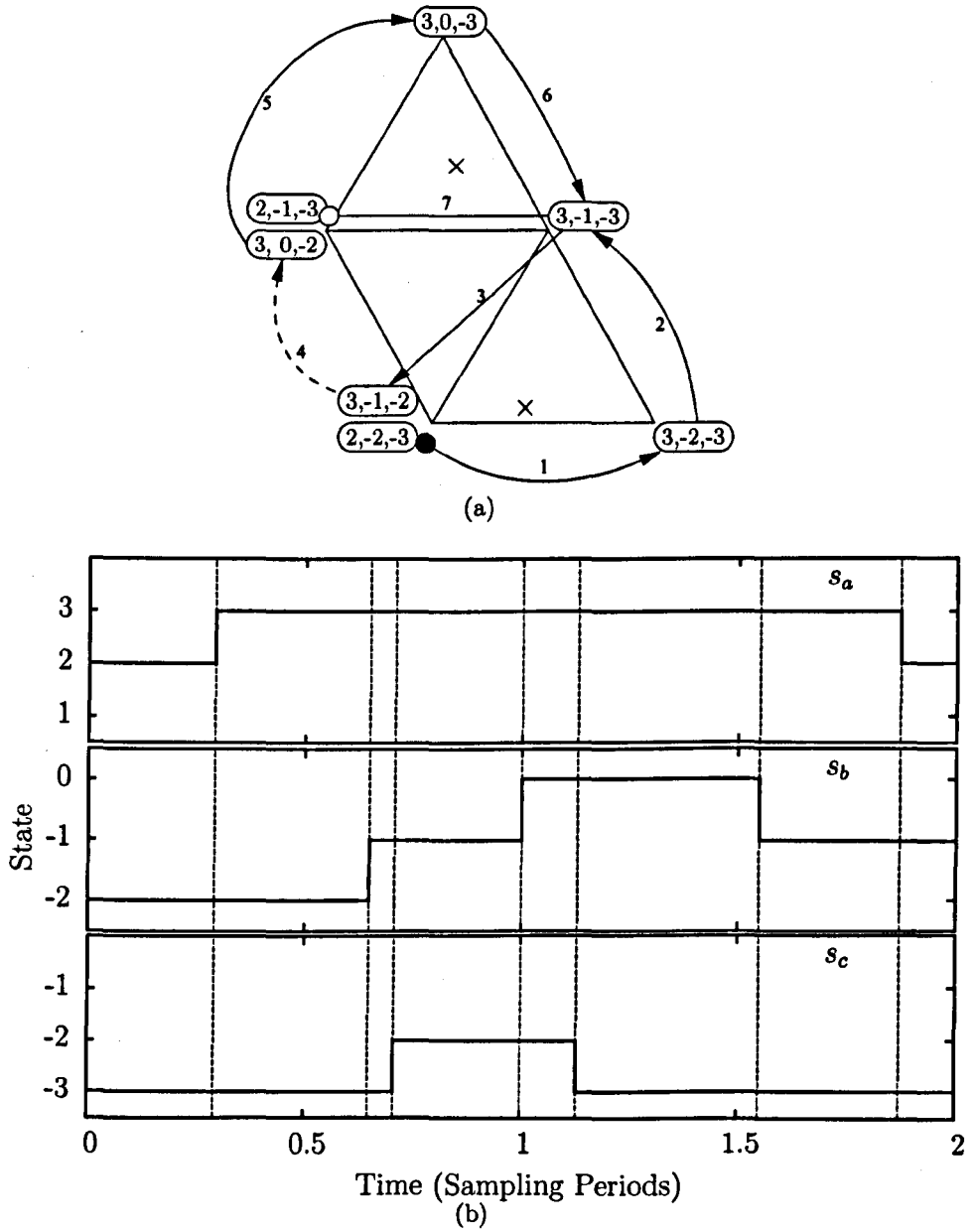


Figure 4.13: The state sequence used to synthesize adjacent samples in different triangles, shown (a) on the space-vector diagram from • to ○ and (b) in the time domain

4.2.2 Synchronization and Symmetry

The frequency spectra of pulse-width modulated waveforms comprise groups of side-band harmonics clustered around harmonics of the carrier frequency, or equivalent carrier frequency. The harmonic currents and voltages produced by grid-connected power converters are subject to strict regulations. Relevant standards include

- IEEE 519-1992 [95],
- IEC 61000-3-6 [96],
- ENA Engineering Recommendation G5/4-1 [97] and
- IEC 61000-4-7 [98].

The first two standards cover the limits of harmonic interference that can be tolerated in electrical networks. The third, G5/4-1, is a UK specific document based on IEC 61000-3-6. The measurement of harmonics is discussed in IEC 61000-4-7, which is the basis for measurements used to interpret IEC 61000-3-6 and G5/4-1. Future revisions of IEEE 519 are likely to adopt the same measurement standard [99].

Categories of harmonics that are particularly heavily regulated are even harmonics, harmonics whose order is a multiple of three and inter-harmonics, which are components at frequencies that are not exact multiples of the supply frequency. At high frequencies, inter-harmonics are not subject to any greater restriction than harmonics because the measurement system of [98] groups together harmonics and nearby inter-harmonics. Inter-harmonics close to the supply frequency are heavily restricted, however, because of their influence on flicker in lighting systems [96].

All these particularly restricted harmonics can be eliminated if the modulated waveform exhibits the following properties:

Periodicity

$$v_n(\omega t) = v_n(\omega t + 2\pi) \qquad n \in \{a, b, c\}$$

Inter harmonics are eliminated if the modulation process is synchronized to the supply so that the sampling frequency is a multiple of the supply frequency. As it is only low frequency inter-harmonics that are of concern, the modulation need not be synchronized if the switching frequency is sufficiently high [60]. As the equivalent carrier frequency is reduced non-integer side-bands begin to encroach towards, and even below, the fundamental frequency.

An important consideration when deciding if synchronized modulation is required is the rate at which the magnitudes of side-band harmonics reduce, or *roll off*, for frequencies away from the carrier harmonics. The rate of side-band roll-off is very high for two-level modulation [54] so the frequency spectra consist of isolated groups of side bands. The rate of side-band roll-off for multi-level modulation schemes is much lower than for two-level modulation [58]. Hence the groups of side-bands extend over a wider range of frequencies and tend to overlap. At the equivalent carrier frequency of 750Hz considered in this thesis the side-bands extend towards the fundamental and so the modulation must be synchronized to avoid the regulated, low-frequency inter-harmonics.

The effect of synchronized modulation is to produce periodic waveform where, in steady state, the modulated waveform is identical in each cycle.

Three-phase symmetry

$$v_b(\omega t) = v_a(\omega t - \tfrac{2\pi}{3}) \qquad v_c(\omega t) = v_b(\omega t - \tfrac{2\pi}{3})$$

If the three phase voltages are identical, only displaced by 120°, then harmonics whose order is a multiple of three cancel between the phases. Waveforms with three-phase symmetry are easily produced if the ratio of carrier to fundamental frequency is a multiple of three.

It is important to appreciate that the harmonic cancellation of three-phase symmetrical waveforms does not reduce the harmonic distortion compared to modulation at other carrier frequency ratios [60]. Because the waveforms have a common carrier and the references are displaced by

120°, the harmonics with the following orders cancel between the phases for any carrier frequency ratio.

$$\omega_c \pm 3n\omega \qquad\qquad n \in \mathbb{Z}$$

If the carrier frequency ratio is a multiple of three to produce three-phase symmetrical waveforms then these cancelled harmonics are the triple-n harmonics of the fundamental frequency.

Half-wave symmetry

$$v_n(\omega t) = -v_n(\omega t - \pi) \qquad\qquad n \in \{a, b, c\}.$$

Even harmonics, which are regulated more heavily than odd harmonics, are eliminated if the positive and negative half-cycles are the same shape.

These constraints of symmetry combine into a single constraint, which dictates the relationship between the phase voltages in each sector of the space-vector diagram.

$$\begin{aligned} v_a(\omega t + \tfrac{\pi}{3}) &= -v_b(\omega t) \\ v_b(\omega t + \tfrac{\pi}{3}) &= -v_c(\omega t) \\ v_c(\omega t + \tfrac{\pi}{3}) &= -v_a(\omega t) \end{aligned} \tag{4.12}$$

For (4.12) to be obeyed, samples must appear in the same place in each sextant and the choice of switching sequences and redundant states must be consistent throughout [92]. Also, because of the negative signs in (4.12), for every sample synthesized by positive edges in one sector the equivalent sample in the next sector must be produced by negative edges. This occurs naturally if there is an odd number of samples in each sector.

Equation 4.12 is the space-vector equivalent of the common *rule-of-thumb* for carrier-based modulation that the ratio of the carrier frequency to the fundamental frequency should be an odd multiple of three. Research has shown that such an approach does not inherently reduce the distortion of the modulated waveforms and that there is no fundamental reason to maintain synchro-

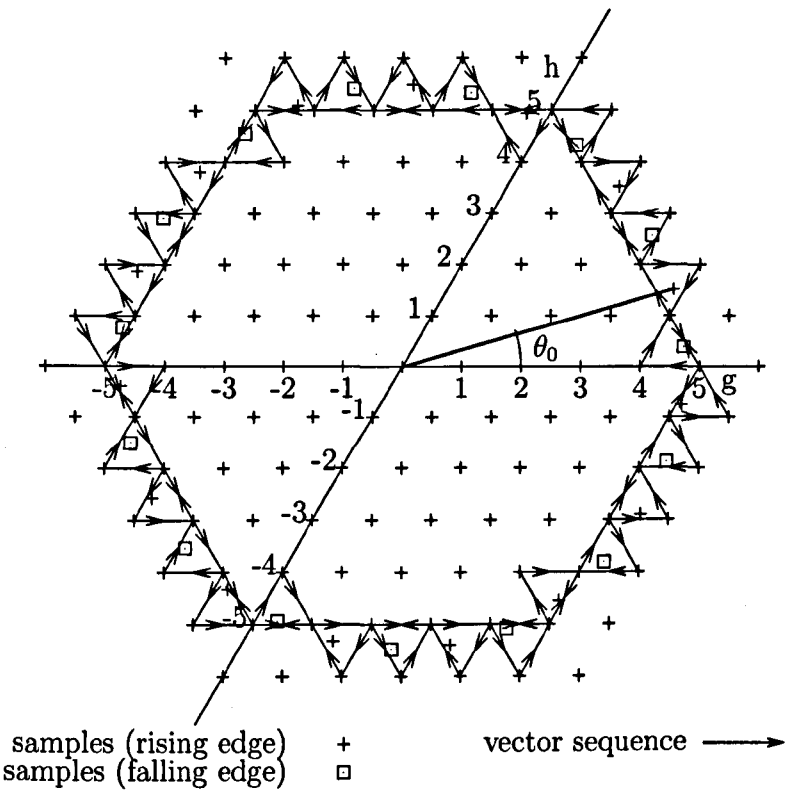


Figure 4.14: Sequence of voltage vectors and reference sample points for space-vector modulation. $\hat{s} = 3.2$

nized modulation if the switching frequency is high enough [54], [60]. However, in this case, where the switching frequency is low, the rate of side-band roll-off is low and grid-codes are relevant, it is appropriate to adopt synchronized modulation in order to avoid the specific categories of harmonics identified.

Example Waveforms

The samples of the reference vector and the corresponding sequence of switching vectors are shown in Figure 4.14 for a seven-level converter at a sampling rate of 1500Hz and a modulation index, $\hat{s}$, of 3.2. Diagrams similar to Figure 4.14 are reproduced throughout this thesis as a means to quickly compare the modulation under different conditions. The positions of the reference-vector samples are indicated, including an indication of whether the samples

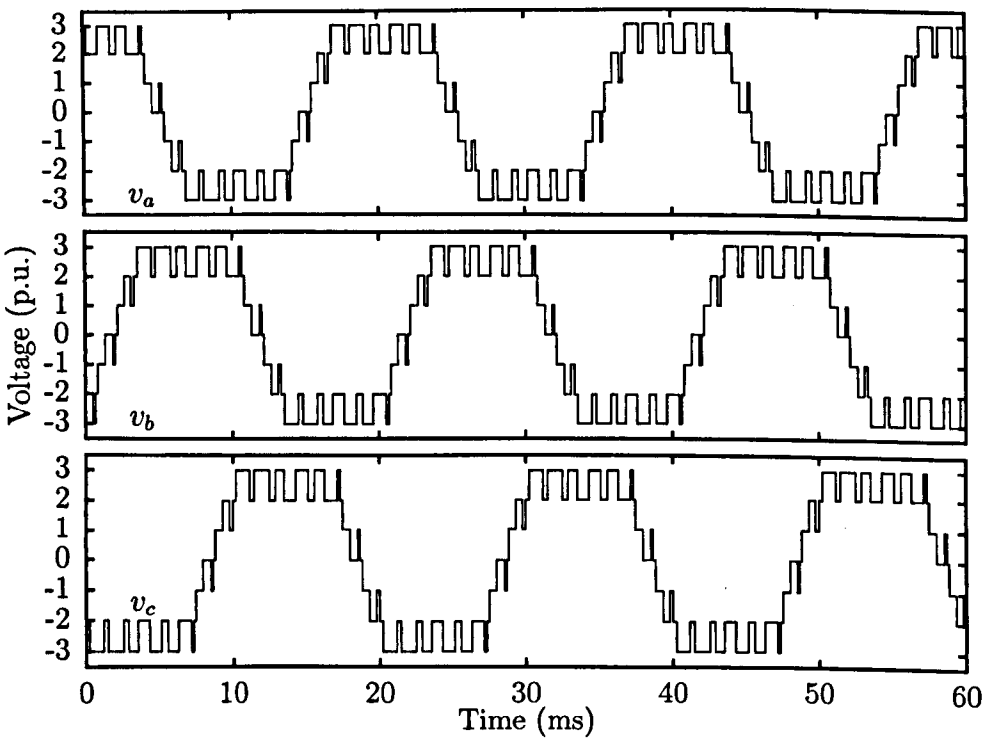


Figure 4.15: Phase voltages for space-vector modulation with ideal d.c. sources

are synthesized by rising or falling edges. Asymmetries in the space-vector diagram are helpful for debugging implementations of space-vector modulation as it is quickly possible to identify areas where incorrect vectors are applied. In this example, the samples of the reference vector occupy identical positions in each sector and are produced by alternating rising and falling edges. Hence, the modulated waveforms (Figure 4.15) obey the symmetry requirement of (4.12).

The sampling rate chosen for this example, 1500Hz, is the lowest practical sampling rate at which continuous space-vector modulation can be applied to a converter with three-cells per phase. Consecutive samples of the reference vector in Figure 4.14 never occupy the same triangle but are close enough that only a single commutation is required to move from one triangle to the next. If the sampling frequency is reduced further, the distance between the samples increases and multiple simultaneous commutations are required to step from one triangle to the next. Hence the same sampling rate is used throughout this thesis.

4.3 Carrier-Based Space-Vector Modulation

An alternative method to produce space-vector modulated waveforms using carrier-based modulation is described in [56]. The method modifies the reference waveforms by applying a common-mode offset in order to equalize the dwell times of the first and last vector applied in each half-carrier period.

The optimal common-mode offset for two-level modulation is given by (4.13) [55].

$$v_{\mathrm{cm}}(v_a, v_b, v_c) = -\frac{1}{2}\{\min(v_a, v_b, v_c) + \max(v_a, v_b, v_c)\} \qquad (4.13)$$

In (4.13) the min and max functions give the instantaneous minimum and maximum of the time-varying arguments.

For multi-level modulation, the common-mode offset is calculated in multiple steps [56]. Firstly, equation (4.13) is calculated as for two-level modulation. The result is constrained to the range $(0, E)$ using the *modulo* operator (4.14)

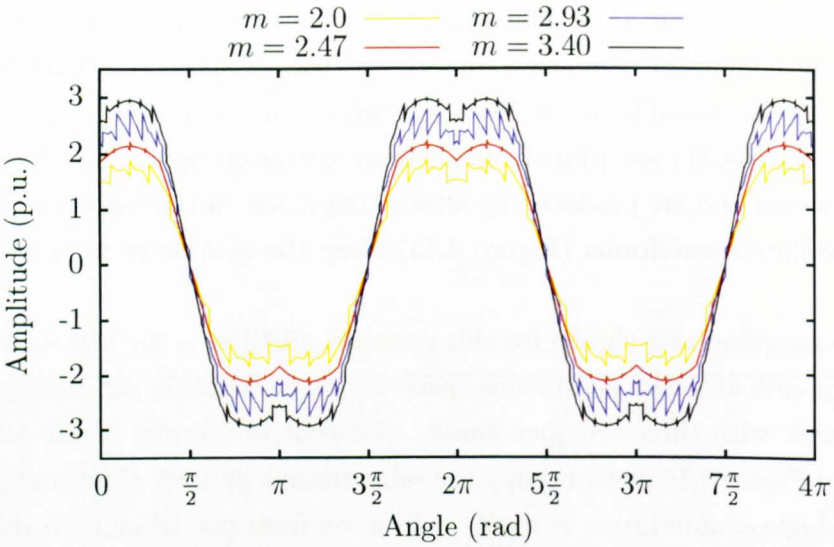


Figure 4.16: Modified reference waveforms for carrier-based, space-vector modulation

and the result of (4.14) is input again to (4.13), to produce the final common mode offset (4.15).

$$v_k{}' = \left(v_k + v_{\text{cm}}(v_a, v_b, v_c)\right) \bmod E \tag{4.14}$$

$$v_{\text{cm}}{}' = \frac{E}{2} + v_{cm}(v_a{}', v_b{}', v_c{}') \tag{4.15}$$

Modified references for a single phase, including the optimal common mode signal of (4.15), are shown in Figure 4.16 for a range of modulation index. For some values of modulation index, for example $m = 2.47$ in Figure ??, the multi-level reference closely approximates the optimized reference for two-level modulation. For other modulation indices, the reference becomes highly discontinuous.

To demonstrate the equivalence of space-vector modulation and the modified carrier modulation, Figure 4.17 shows the carrier diagram and the switching signals for a single reference sample. The leftmost example shows conventional level-shifted carrier modulation and the dwell times d_1 and d_4 are

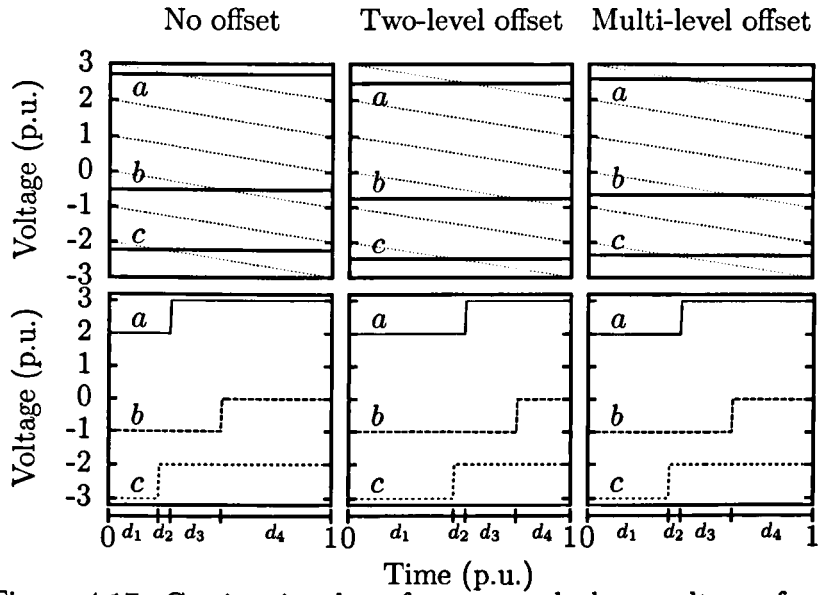


Figure 4.17: Carrier signals, references and phase voltages for one sample of level-shifted carrier modulation with three common-mode offsets

not equal. In the central example, the common-mode offset defined in equation (4.13) has been applied causing the dwell times d_1 and d_4 to change but these are not equal. Dwell times d_2 and d_3 are unchanged. The common-mode offset given in equation (4.15) has been applied to the rightmost example in Figure 4.17: d_1 and d_4 are equal, as they would be in space-vector modulation.

Finally, Figure 4.18 shows several cycles of carrier-based modulation with the offsets applied. This figure was produced using the same sampling frequency and modulation index as the space-vector modulated waveforms in Figure 4.15 and hence the resulting waveforms are identical.

4.4 Simulations

At low sampling rates, the exact positions of the samples of the reference vector influence the choice of switching state and duty cycles. Small changes in the positions of the samples can have a profound effect on the quality of the voltages and currents produced. The two factors influencing the location of the reference samples are the modulation index and the angle of each sample. For

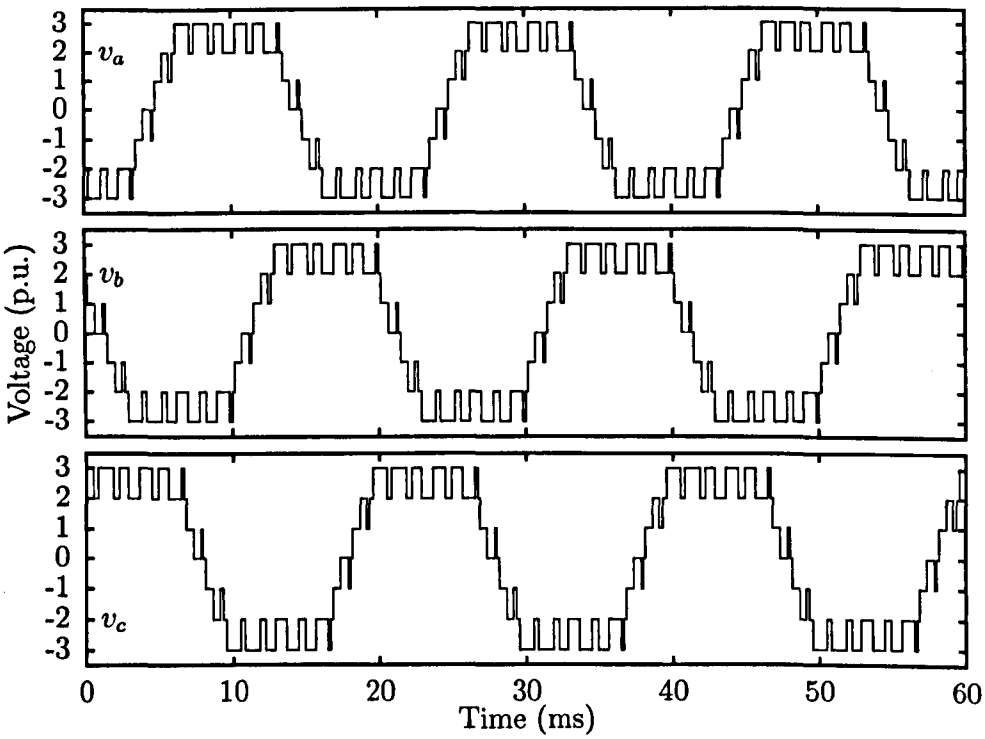


Figure 4.18: Waveforms produced using level-shifted carrier modulation with common mode offset. Compare with Figure 4.15

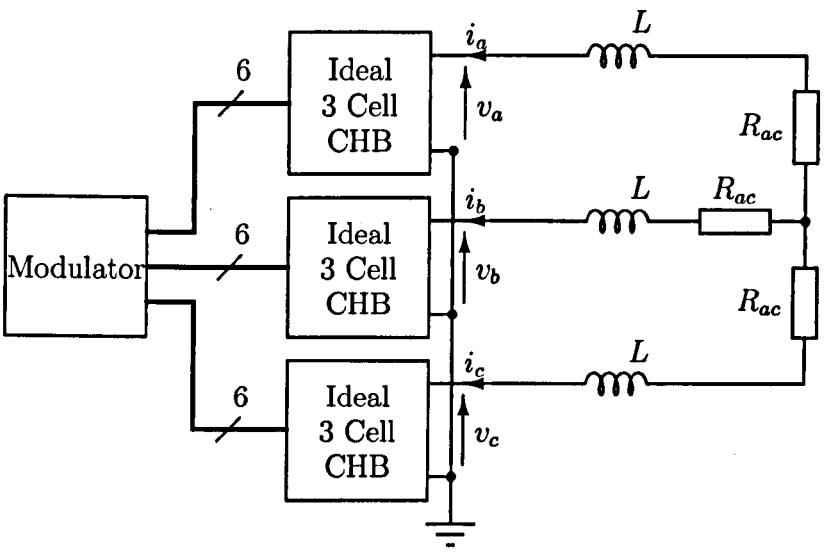


Figure 4.19: Structure of simulated converter

synchronized modulation the angle of each sample can be adjusted by changing the initial sampling angle, θ_0 in Figure 4.14, which is the first sampling in each cycle producing a negative edge.

To explore the effect of modulation index and initial angle, a seven-level cascaded H-bridge inverter has been simulated feeding an R-L load (Figure 4.19). The results presented are produced by space-vector modulation operating in open loop over a range of modulation index and initial angle. As before, the sampling rate is 1500Hz which gives 12° between each reference sample. The initial angle is therefore varied in the range $[0°, 24°]$. An offset of 12° places the samples in the same location as 0° but reverses the direction of the voltage step produced by each sample and an offset of 24° is identical to 0°.

4.4.1 Device Switching Frequency

The number of commutations per cycle per phase for the simulated range of modulation index and initial angle are represented by the shaded regions in Figure 4.20.

There are three distinct bands of modulation index in Figure 4.20. At

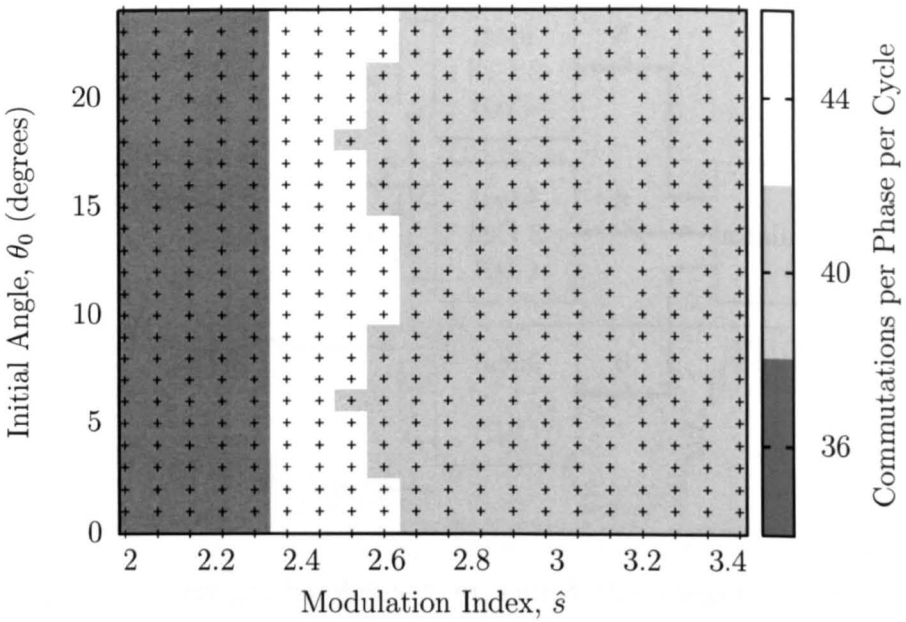


Figure 4.20: Variation in switching frequency with modulation index and initial angle.

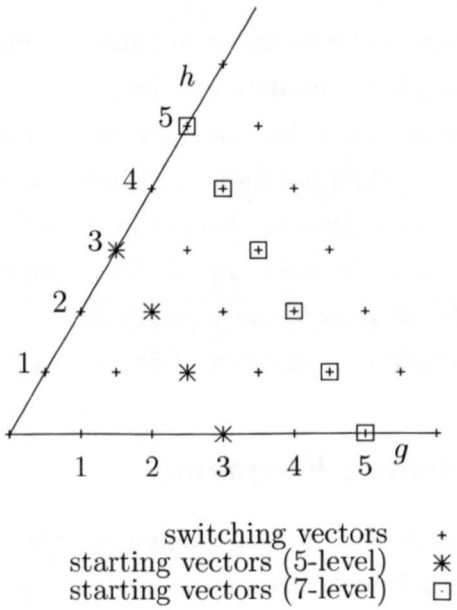


Figure 4.21: Starting vectors of space-vector switching sequences

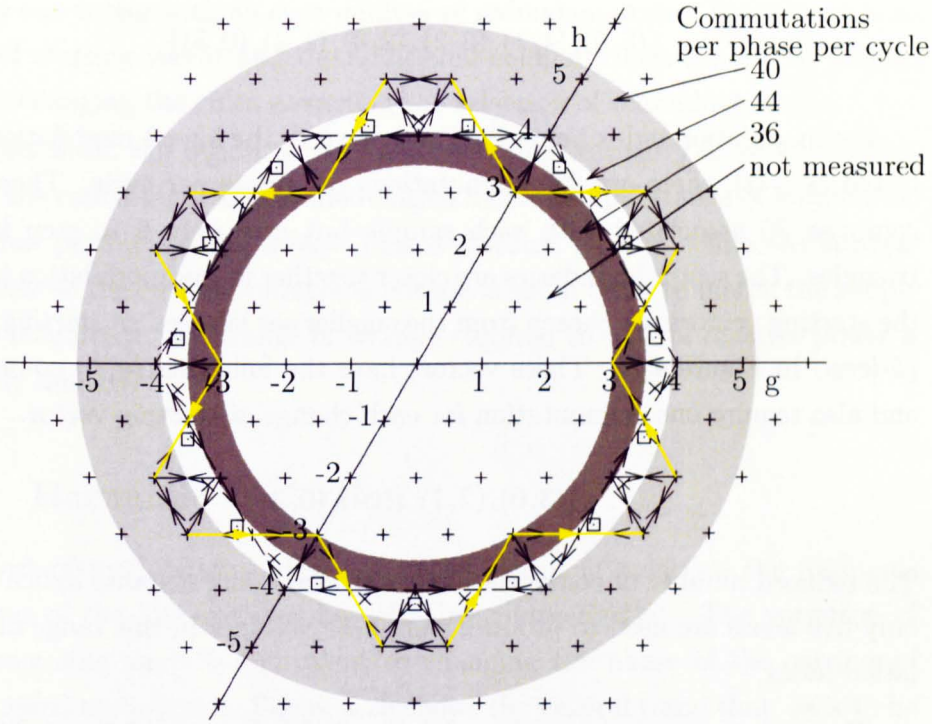


Figure 4.22: Space-vector diagram when $\hat{s} = 2.45$, showing approximate bands of constant device switching frequency.

high modulation index, above around $\hat{s} = 2.6$, there are 40 commutations per phase per cycle: thirty directly modulated edges and ten more occurring at the sampling instants allowing the starting vector of each sequence to move from triangle to triangle. In this range of modulation index, the starting vectors in the first sector belong to the set marked as *starting vectors (7-level)* in Figure 4.21. These vectors have the following (g, h) co-ordinates and one commutation is needed each time the starting vector changes.

$$\{(5,0),(4,1),(3,2),(2,3),(1,4),(0,5)\}$$

For modulation index below 2.45 and down to the lowest modulation index tested ($\hat{s} = 2$), there are 36 commutations per phase per cycle. These again comprise 30 associated with each sample but now only 6 to step between triangles. The sector boundaries are closer together at low modulation index so the starting vectors are chosen from the smaller set labelled as *starting vectors (5-level)* in Figure 4.21. These vectors have the following (g, h) co-ordinates and also require one commutation for each change of starting vector.

$$\{(3,0),(2,1),(1,2),(0,3)\}$$

The reduced number of commutations at the sampling instants indicates that only five levels are used to produce the phase voltages in this range of modulation index.

There is a narrow range of modulation index between 2.4 and 2.6 where the number of commutations increases to 44 per phase per cycle. The extra commutations occur because the reference samples are approximately equidistant from the two sets of starting vectors and extra commutations are required for the starting vector to change from one set to another. Instead of the single commutation required to change starting vectors within either of the sets described, two commutations are required to to move between sets.

An example space-vector diagram is plotted in Figure 4.22, along with bands representing ranges of modulation index identified from Figure 4.20. Note that the magnitudes of the vectors on the space-vector diagram are 1.5

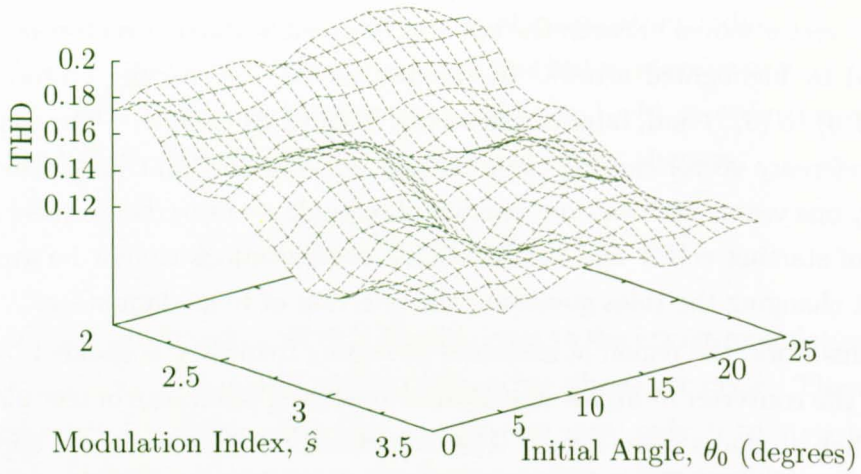
times larger than the modulation index values. The example plotted in Figure 4.22 has modulation index 2.45 and hence is in the region of increased switching frequency identified. The extra commutations that occur when the starting vector moves between the two sets of possible starting vectors are represented by highlighted arrows. In the first sector, the starting vector steps from $(3,0)$ to $(3,2)$ and, later in the sector, from $(2,3)$ to $(0,3)$. The samples of the reference vector causing these changes are contained in triangles including only one vector with an even number of redundant states; hence there is no choice of starting vector and the additional commutations cannot be avoided without changing the rules governing the selection of redundant states.

In this work, the region of increased switching frequency is avoided by operating the converter at higher modulation index well into range of modulation index that produces seven levels. This is justified for grid-connected applications because the output voltage magnitude is set in order to match the supply voltage magnitude. The range of voltage required to control reactive power is relatively limited.

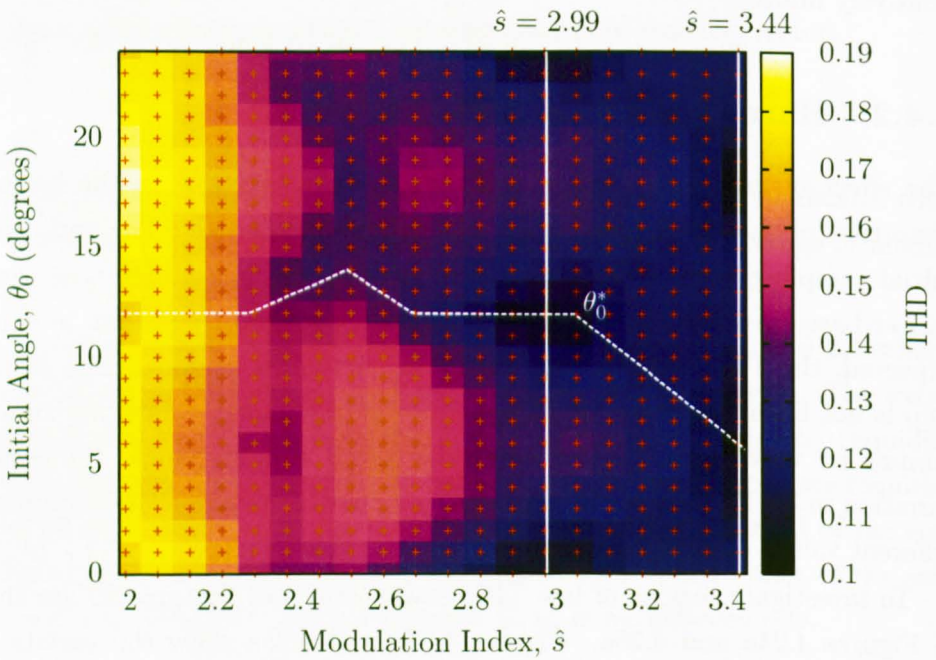
4.4.2 Harmonic Distortion

The effect of modulation index and initial sampling angle on the harmonic distortion of the line voltages has also been investigated. The variation of initial sampling angle is equivalent to changing the phase of the carriers of carrier-based modulation. Figure 4.23 shows the general trend that, as is to be expected, the THD reduces with increasing modulation index. The relationship is not linear, however, and Figure 4.23 shows multiple local maxima and minima for varying modulation index and initial sampling angle. Some of the variation in THD is due to the changing number of voltage levels produced at different values of modulation index.

To investigate regions of low THD, two sections of Figure 4.23 are shown in Figures 4.24a and 4.25a. Figures 4.24a and 4.25a show the variation of THD with initial sampling angle for constant modulation index, 2.99 and 3.44 respectively. Also shown in each case is the variation in the spectrum of the line voltage, where the harmonics are normalized by the magnitude of the



(a)



(b)

Figure 4.23: Variation of line voltage THD with modulation index and initial angle represented as (a) a three-dimensional projection and (b) a colour map. A locus of relatively low THD values, θ_0^* given by (4.17), is also plotted.

fundamental component. The fundamental component is suppressed from the plot so that the individual harmonics are visible.

In Figure 4.24a, a region of low THD is highlighted and the same region is highlighted in Figure 4.24b. Within the highlighted region there is a clear reduction in the magnitude of low-order harmonics. Similar local minima are highlighted in Figure 4.25a, with the corresponding regions also highlighted in Figure 4.25b. Again, a general reduction in the magnitude of harmonics is visible around the highlighted region, but the seventh harmonic is relatively high at the point where other harmonics are reduced.

It is also interesting to investigate if the change in distortion with initial sampling angle is caused by the space-vector modulation and whether the effect is visible in carrier-based modulation. For carrier-based modulation variation of the initial angle is equivalent to variation of the phase of the carrier signals with respect to the fundamental reference.

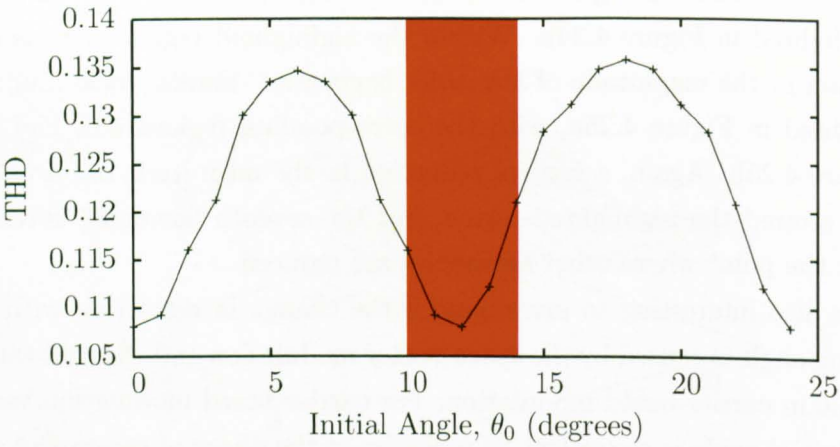
Figures 4.26 to 4.28 show the frequency spectra of naturally-sampled, regularly-sampled and space-vector modulation at a constant modulation index $\hat{s} = 2.6$.[1] The carrier-based modulation in these examples have a sinusoidal references: the modified common-mode component is not used here as it was shown in section 4.3 that this method produces identical waveforms to space-vector modulation.

In each figure, the initial angle is increased by 6°, starting from 6° in Figure 4.26, a local maximum of THD, and ending with 18° in Figure 4.28. At this carrier frequency ratio, an increment of 6° is a quarter of the carrier period.

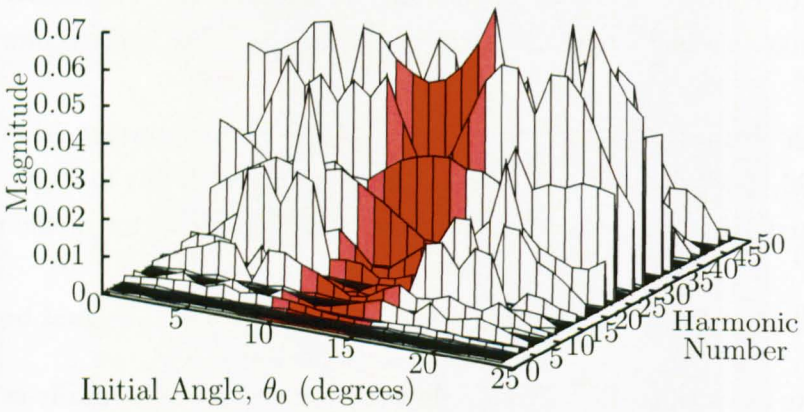
Some interesting features of Figures 4.26 to 4.28 are summarized below:

- There is a significant difference between the spectra of naturally sampled and regularly sampled modulation. During some half-carrier periods, where the gradient of the reference is greatest, the naturally sampled reference waveform does not intersect with a carrier and no pulse is produced. As the regularly sampled reference is constant in each half-carrier period, regular sampling includes a pulse in every half-carrier period. It

[1] Corresponding time-domain waveforms are included in Appendix B

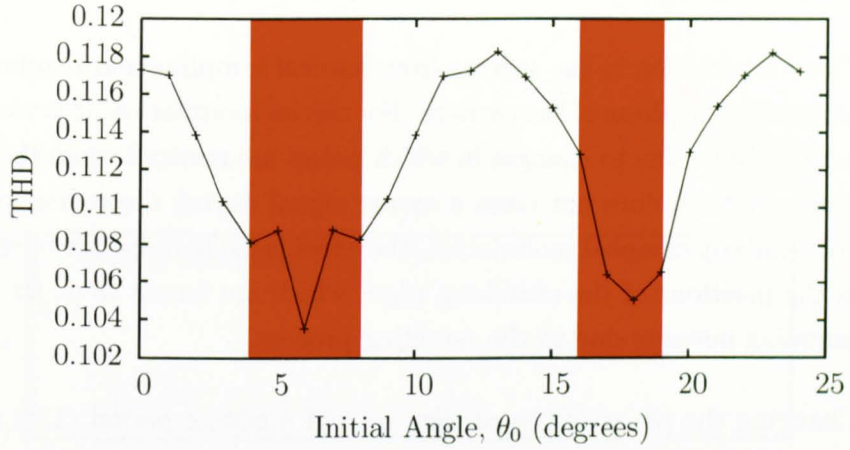


(a)

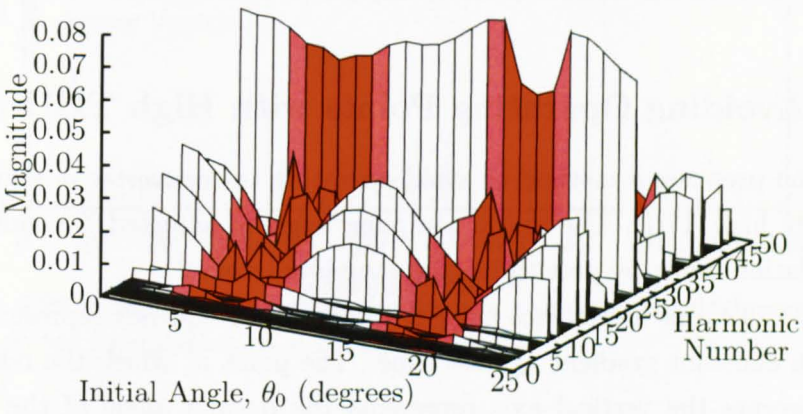


(b)

Figure 4.24: Variation of (a) THD and (b) harmonic spectrum with initial angle offset for constant modulation index $\hat{s} = 2.99$



(a)



(b)

Figure 4.25: Variation of (a) THD and (b) harmonic spectrum with initial angle offset for constant modulation index $\hat{s} = 3.44$

is likely that the change in the number of commutations is responsible for the significant differences in the spectra of naturally and regularly sampled modulation at this carrier frequency.

- There is variation in the spectra from natural sampling and regular sampling with the phase of the carriers. For carrier modulation, this variation is likely to be due to changes in which pulses are omitted when the reference waveform does not cross a carrier signal during the carrier period. For regularly sampled modulation, the effect is likely to be due to changes in the positions of the switching edges which are forced to occur at the sampling instants due to the sampling process.

- Changing the phase of the carriers by half a carrier period (12°) causes the spectra to be identical because the resulting output waveforms are the mirror-image of each other. This is in contrast to space-vector modulation. Because of the adjustment of the switching edges to centre the line-to-line pulses in the half-carrier period, space-vector modulation requires a change of full carrier cycle (24°) to produce the same spectrum.

4.4.3 Avoiding Operating Points with High THD

This section proposes a method to avoid operating the converter in regions of particularly high THD. The initial sampling angle is adjusted depending on the modulation index by perturbing the sampling interval.

Figure 4.29 shows a reference angle with constant frequency represented as a line with constant gradient against time. The point at which the reference angle intercepts the vertical axis represents the desired angle of the initial sample, θ_0^*. The angles θ_1 to θ_n represent the angle at which the reference vector is to be sampled with a constant sampling period, T_s. If the reference vector is sampled and the angle is found not be be one of θ_1 to θ_n, such as point P in Figure 4.29, the time to the next sampling instant, T', can be adjusted so that the next sample is taken at the correct angle.

The mechanism to align the sampled vectors is based on the index of the

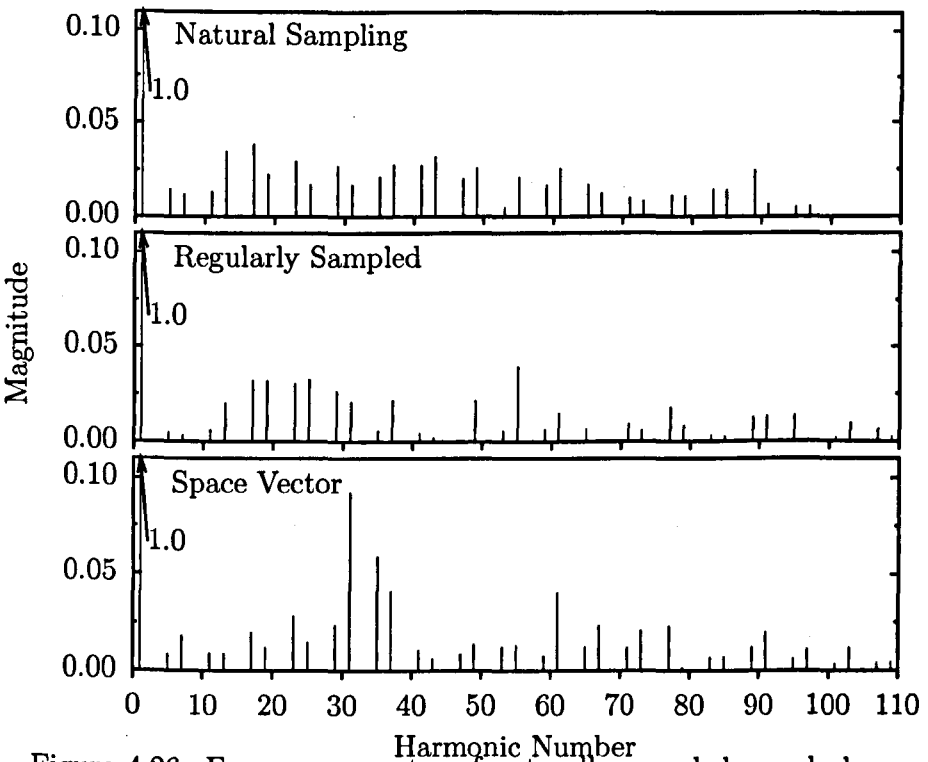


Figure 4.26: Frequency spectra of naturally sampled, regularly sampled and space-vector modulation. $\hat{s} = 2.6$ $\theta_0 = 6°$

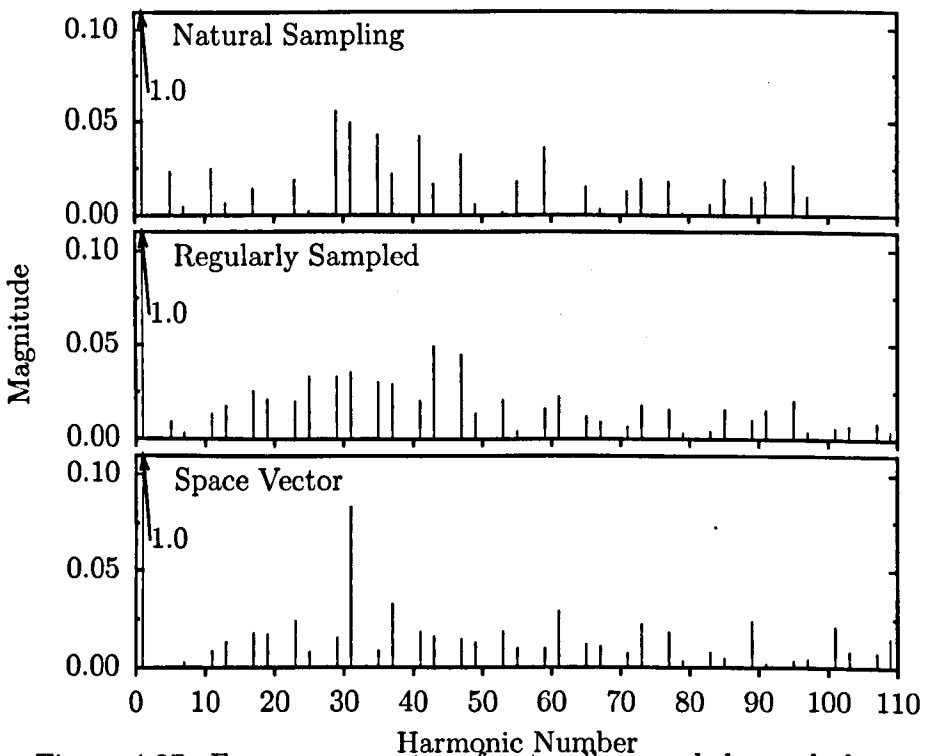


Figure 4.27: Frequency spectra of naturally sampled, regularly sampled and space-vector modulation. $\hat{s} = 2.6$ $\theta_0 = 12°$

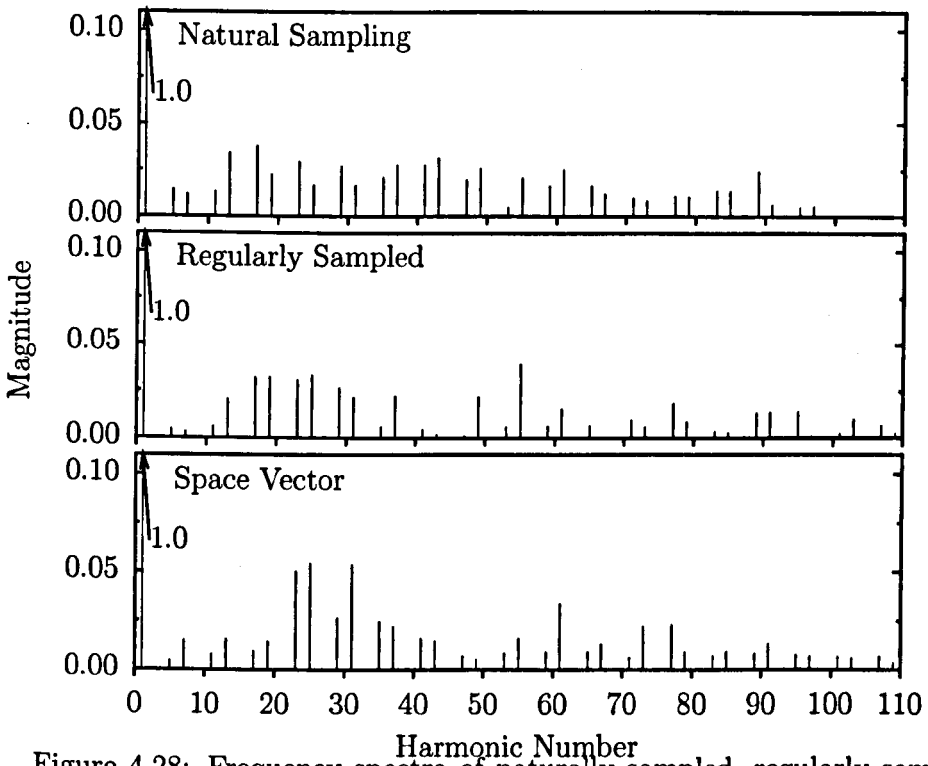


Figure 4.28: Frequency spectra of naturally sampled, regularly sampled and space-vector modulation. $\hat{s} = 2.6$ $\theta_0 = 18°$

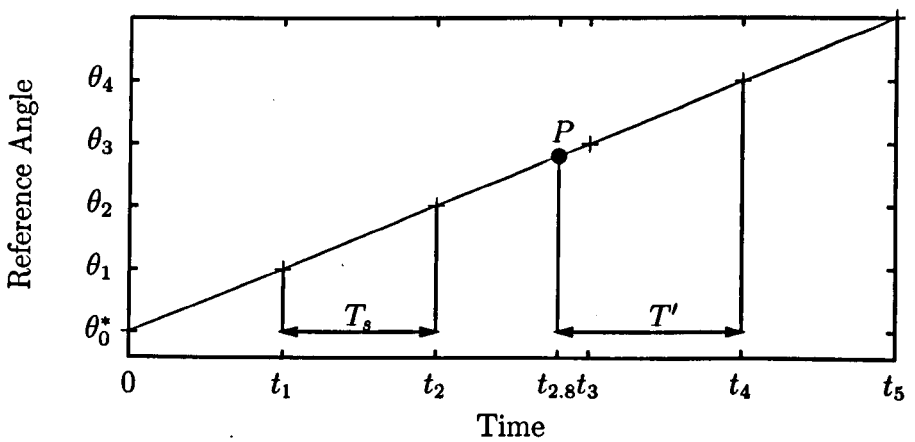


Figure 4.29: Reference angle against time for a constant frequency reference

sampled angle, n, which is given by

$$n = \frac{\theta - \theta_0^*}{\omega T_s},$$

where

θ is the sampled angle of the reference vector,

θ_0^* is the desired initial sampling angle,

ω is the supply angular frequency and

T_s is the intended sampling rate.

The index, n, is a continuous quantity that is an integer when the reference is sampled at one of the target sampling instants. The fractional component of n represents the difference between the actual and target sampling instant as a proportion of the sampling period. The frequency of the reference, w, is required in order to calculate n. ω is a known constant in simulation and can be derived from the PLL of the experimental converter, as discussed in section 3.3.3.

The index of a sample can be used to set the duration of the next sampling period, T', in order to align the angle of the next sample with a chosen index:

$$T' = T_s(n_{\text{next}} - n),$$

where

n is the index of the present sample,

n_{next} is the chosen index of the next sample and

T_s is the nominal sampling period.

The chosen index for the next sampling instant is dependant the location of P relative to the target sampling instants and is given by (4.16). The boundaries

between the sections prevent the modified sampling time from deviating too far from its nominal duration.

$$n_{\text{next}} = \begin{cases} \lceil n \rceil & \text{if } \text{frac}(n) \leq 0.1 \\ n + 0.9 & \text{if } 0.1 < \text{frac}(n) \leq 0.5 \\ n + 1.1 & \text{if } 0.5 < \text{frac}(n) \leq 0.9 \\ \lceil n \rceil + 1 & \text{if } \text{frac}(n) > 0.9 \end{cases} \tag{4.16}$$

Figure 4.30 shows an example of this algorithm in operation. The points marked as + represent the desired sampling angle and the points marked as × represent actual samples. The shaded bands represent the regions of (4.16) around each target sample time.

The first sample shown in Figure 4.30 has an index in the range

$$0.1 < \text{frac}(n) \leq 0.5.$$

As a result, the next sampling period is shortened so that following samples are progressively closer to the target angles. The fourth sampled angle is within ten percent of a sampling period from t_3 so the sampling period is then set to make the next sample align exactly with t_4. Once the samples align with their targets, the sampling period is returned to its nominal value and the angle of subsequent reference samples continue to align with the target locations.

The initial angle demand, θ_0^*, can be set to a constant value or can be linked to a mapping function relating θ_0^* to modulation index. One such mapping function, which tracks regions of low THD, is given in (4.17) and is also plotted in Figure 4.23b.

$$\theta_0{}^*(\hat{s}) = \begin{cases} 12 & \text{if } \hat{s} < 2.29 \\ -8 + 8.73\hat{s} & \text{if } 2.29 \leq \hat{s} < 2.52 \\ 47 - 13.09\hat{s} & \text{if } 2.52 \leq \hat{s} < 2.67 \\ 12 & \text{if } 2.67 \leq \hat{s} < 3.06 \\ 60 - 15.71\hat{s}) & \text{if } \hat{s} >= 3.06 \end{cases} \tag{4.17}$$

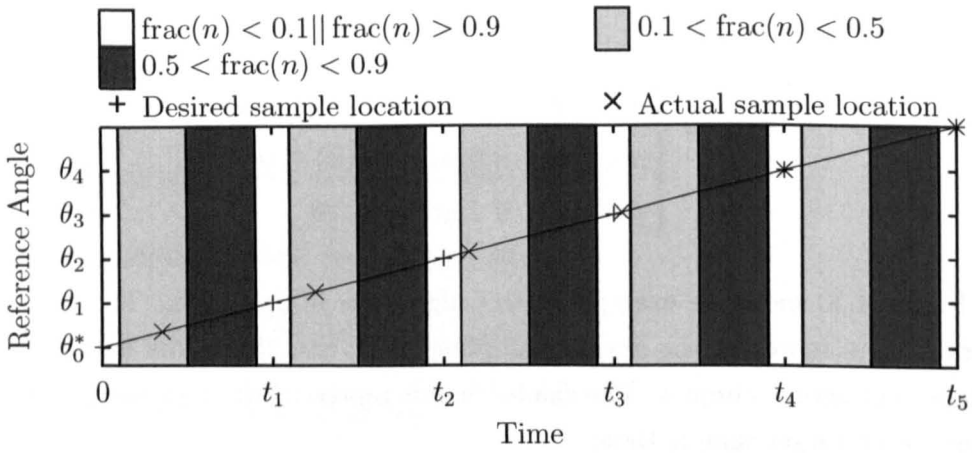


Figure 4.30: Alignment of reference sample instants to their target positions

Equation (4.17) was derived from inspection of Figure 4.23b to avoid the worst THD peaks. It is not possible to exactly track the minimum THD as large step-changes in initial angle in response to small changes in modulation index would be required. Such large changes are likely to disrupt closed loop operation. For similar reasons, it is best to filter the magnitude signal to ensure that the initial angle is constant in steady state and is not unduly influenced by noise in the control variables.

Simulations of Varying Initial Angle: Open Loop

To validate the process of varying the initial angle, the system shown in Figure 4.19 has been simulated for a range of open loop conditions. The initial sampling angle is varied with modulation index to follow the mapping function (4.17). The THD of the line voltages in steady state are shown in Figure 4.31. Figure 4.31 also shows the range of THD at each modulation index obtained from the original simulations. The envelope is effectively the shape of Figure 4.23a viewed from the side.

Especially for high modulation index, Figure 4.31 shows that the THD tracks close to the lower boundary of the envelope. The trough in THD values

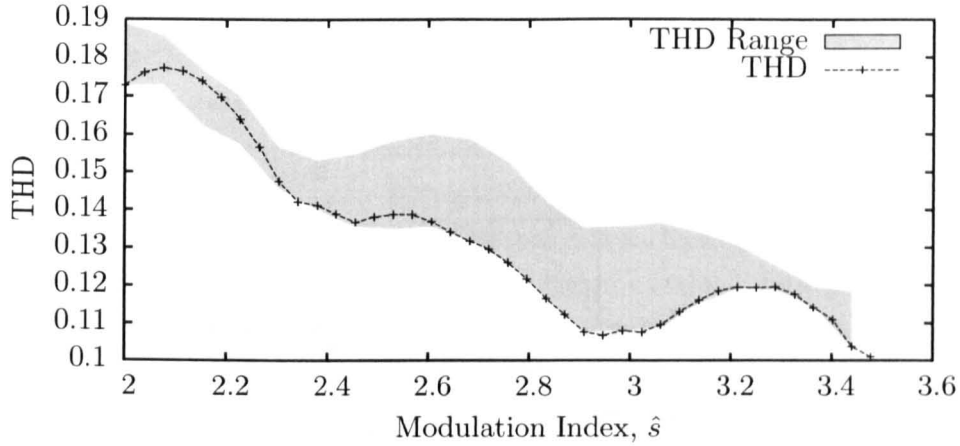


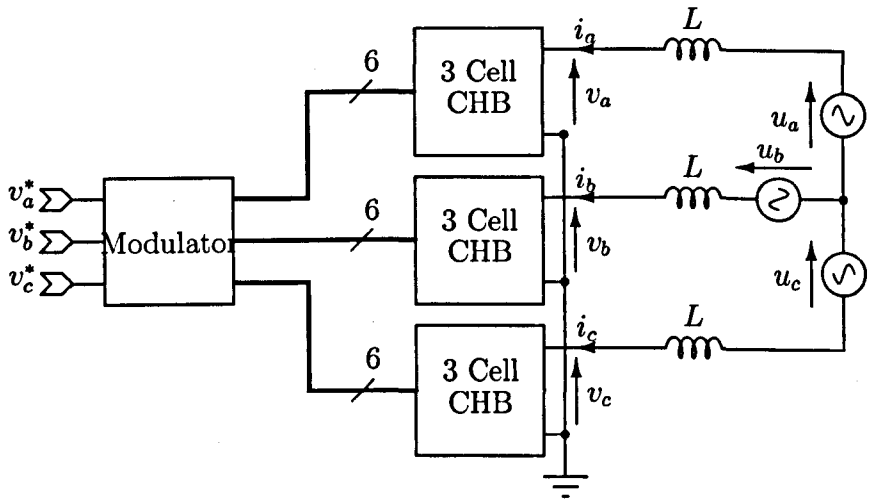
Figure 4.31: Variation of steady-state THD with modulation index when using initial angles defined by (4.17).

for modulation index between 2.9 and 3.1 provides a natural target operating point for an experimental converter.

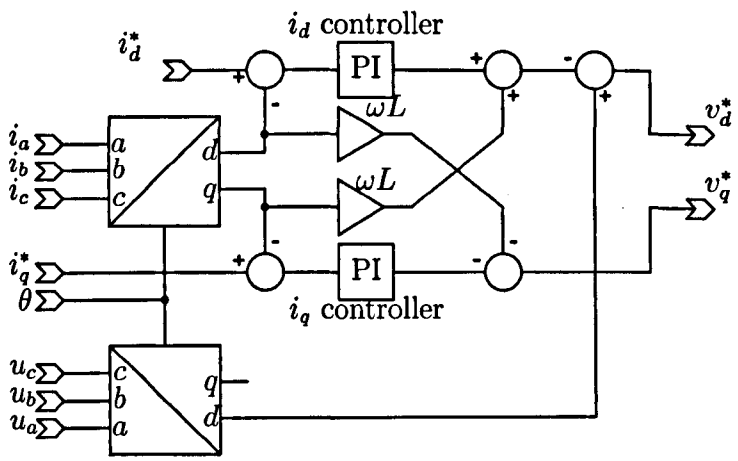
Simulations of Varying Initial Angle: Closed Loop

The method of aligning the samples has also been simulated in closed-loop operation. The circuit configuration and control scheme used is shown in Figure 4.32. Because the simulation includes ideal d.c. links, there is no voltage control loop in this case and the i_d^* reference is a direct input to the controller.

In Figure 4.33, the system is subjected to step changes in demands for real and reactive current at 200ms and 400ms respectively. The sampling frequency changes slightly during the first transient as the modulation is re-synchronized in response to the small change in phase required to increase the real current. The increase in reactive current at 400ms causes a larger change in the sampling frequency as the modulation index increases into the region of (4.17) in which θ_0^* varies with modulation index ($\hat{s} > 3.06$). After a short transient, the magnitude of which is determined by the boundaries defined in (4.16), the sampling frequency quickly returns to the nominal 1500Hz and the modulation successfully synchronizes to the new initial angle. The jitter of the sampling frequency is quantified in terms of the sampling period in Figure 4.34. The



(a)



(b)

Figure 4.32: (a) Circuit topology and (b) control scheme for closed-loop simulations.

minimum, maximum and the quartiles are shown as percentages of the nominal sampling period for samples between 440ms and 560ms. In this steady-state condition, the sampling time is always within the range $\pm 0.6\%$ of the nominal value, with an inter-quartile range of 0.2%.

Frequency spectra of the line voltage, v_{ab}, are shown in Figure 4.35 corresponding to each of the steady-state conditions highlighted in Figure 4.33. Each graph in Figure 4.35 includes the spectra obtained with fixed and controlled initial sampling angle. In all cases, controlling the initial angle reduces the magnitude of harmonics, especially the 11^{th}, 13^{th}, 17^{th} and 19^{th} harmonics. There is no evidence of inter-harmonics or spectral leakage suggesting that the modulation continues to produce periodic line voltages even when the sampling period is perturbed. Note that the spectra in Figure 4.35 do not show clear harmonic side-band groups. Multi-level modulation schemes do not exhibit the high rate of roll-off of side-band harmonics found in two-level modulation so side-band groups are not so clearly defined [58].

Finally, Figure 4.36 shows the first ninety degrees of the space vector diagrams of the three cases highlighted in Figure 4.33. The initial angle is un-controlled in the left-hand figures and the timing of the simulation results in an initial offset of around six degrees. This is a worst-case example because, as shown in Figure 4.23, an initial sampling angle of six degrees produces the highest THD for a wide range of modulation index.

The diagrams on the right hand side of Figure 4.36 show the case where the initial angle is controlled. For the first two cases, the initial angle is approximately 12° so samples are aligned precisely with the axes. In the third case, the increase in demand for reactive current raises the modulation index so the initial angle is reduced slightly, in accordance with (4.17).

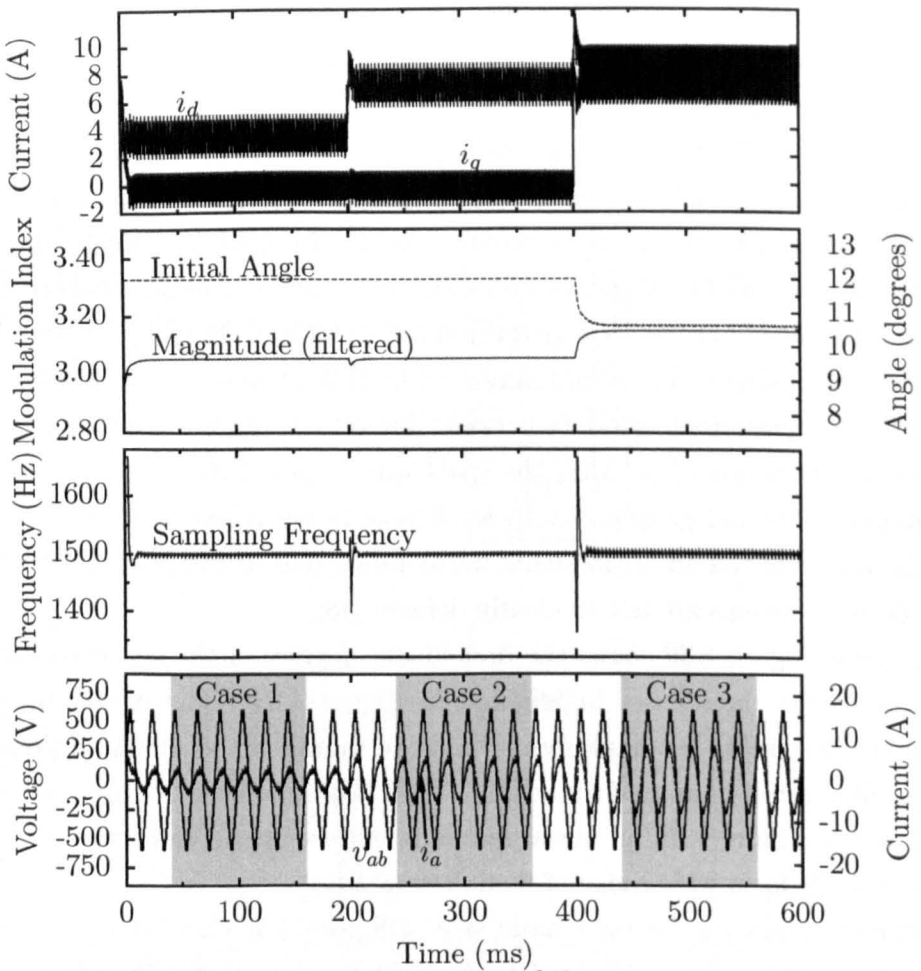


Figure 4.33: Simulated transient response of the current controller with ideal voltage sources including synchronization of the initial angle

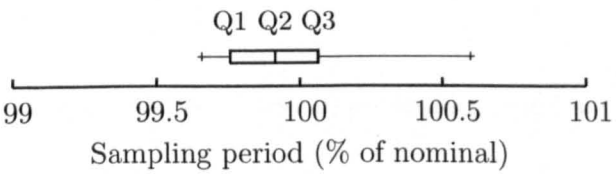


Figure 4.34: Box and whisker plot representing the jitter of the sampling period between 440ms and 560ms

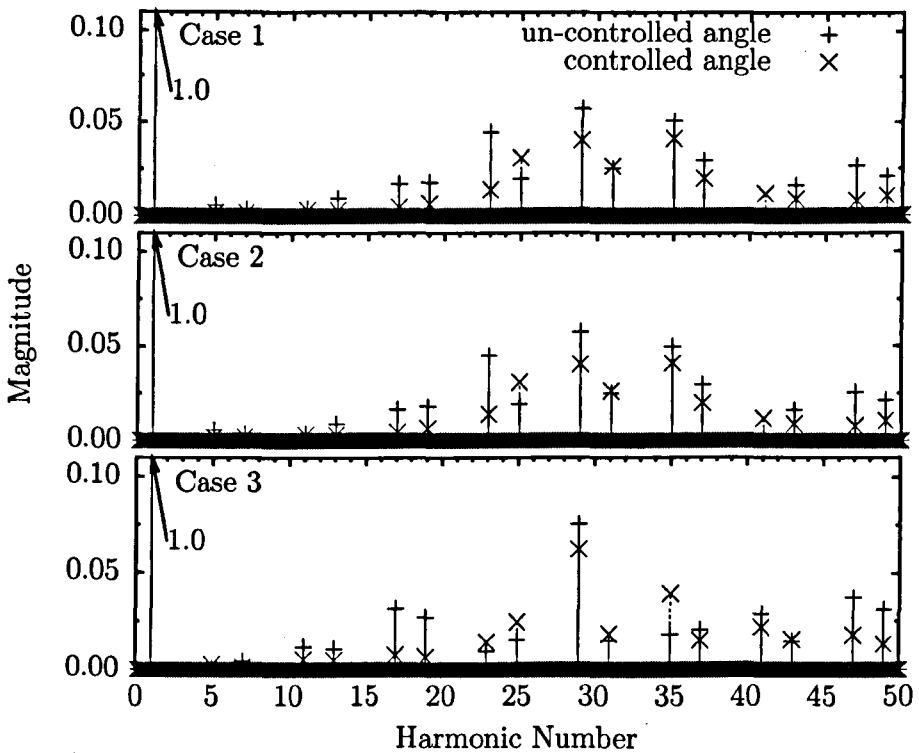


Figure 4.35: Spectra of simulated line voltage for the regions highlighted in Figure 4.33. Versions with controlled and uncontrolled initial angle are compared in each case.

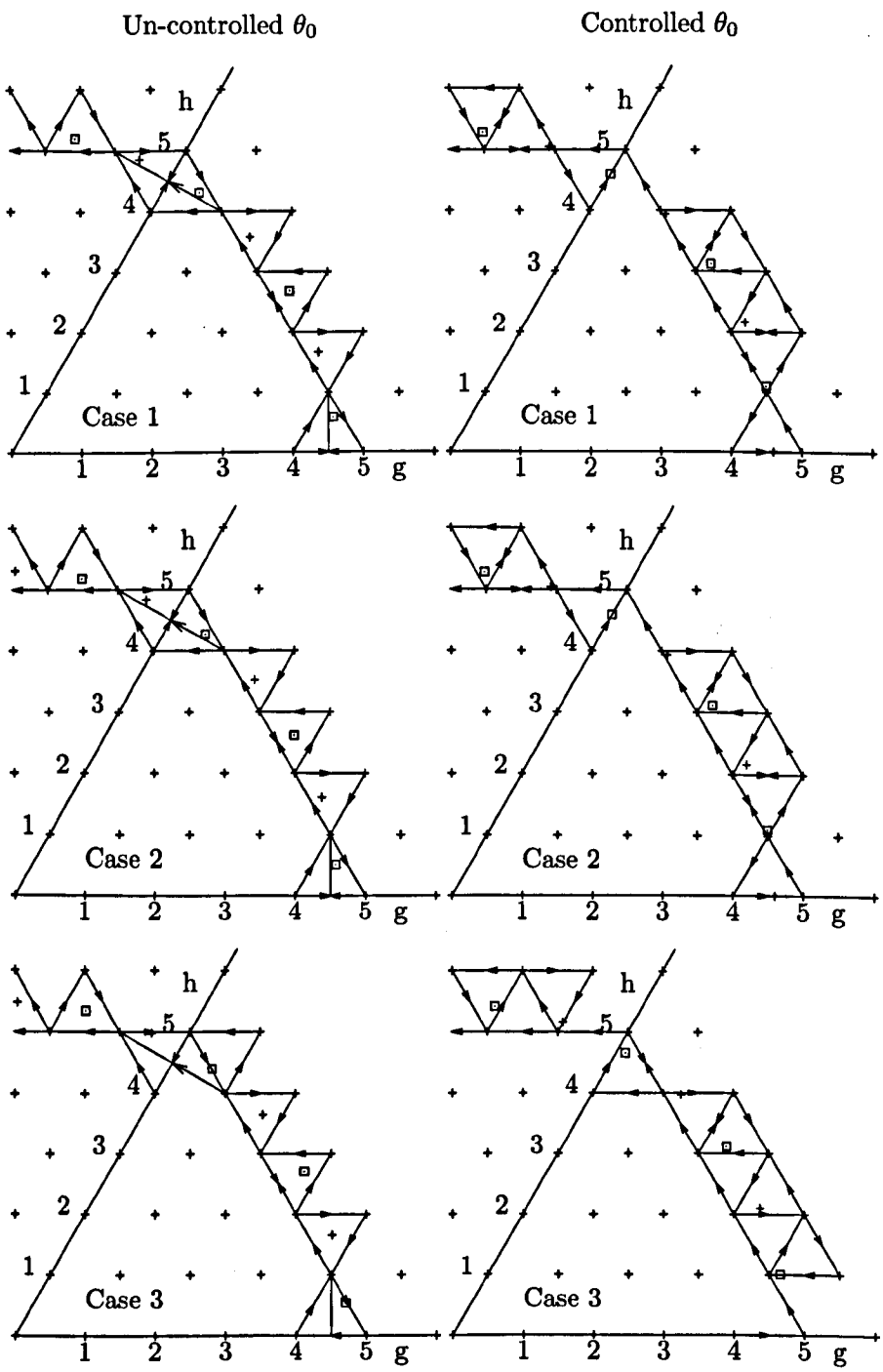
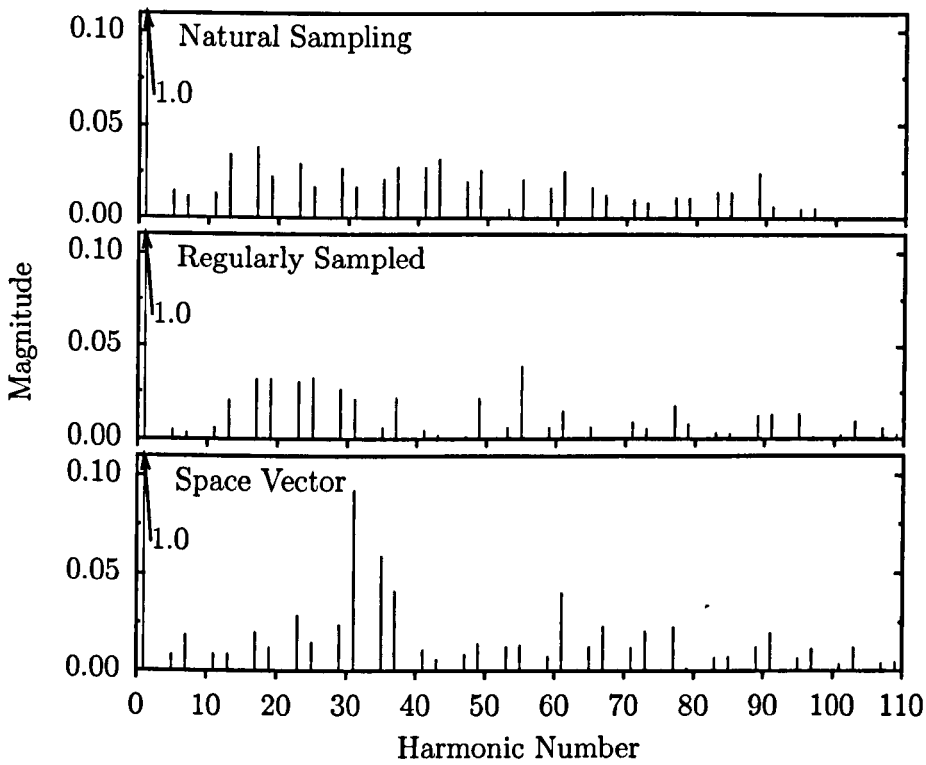


Figure 4.36: Space vector diagrams with uncontrolled (left) and controlled (right) initial angle for cases 1 (top), 2 (middle) and 3 (bottom) from Figure 4.33.



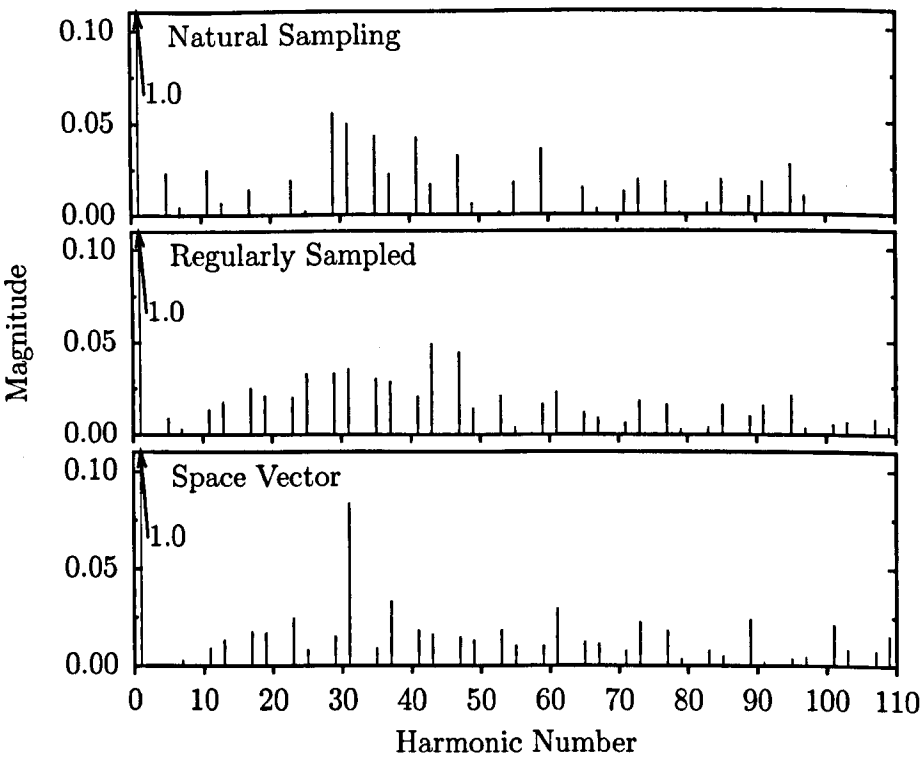
4.5 Experimental Results

The methods derived in earlier sections of this chapter are now verified experimentally. In order for the assumption of ideal d.c. links to be valid any ripple on the capacitor voltages of the experimental converter must be insignificant. The results presented in this section are therefore for very low current.

4.5.1 Modulation in Open Loop

First, the experimental converter is investigated in the open-loop inverting mode. To reduce the current so that there is minimal ripple on the capacitor voltages, the three-phase load has a large resistive component.

The voltages and currents produced by the experimental converter are shown in Figure 4.37. Voltages and currents are shown for ten cycles with two cycles shown on a larger scale. The modulation index is 3.0 and the initial sampling angle is synchronized to 12°, which correspond to the region of low

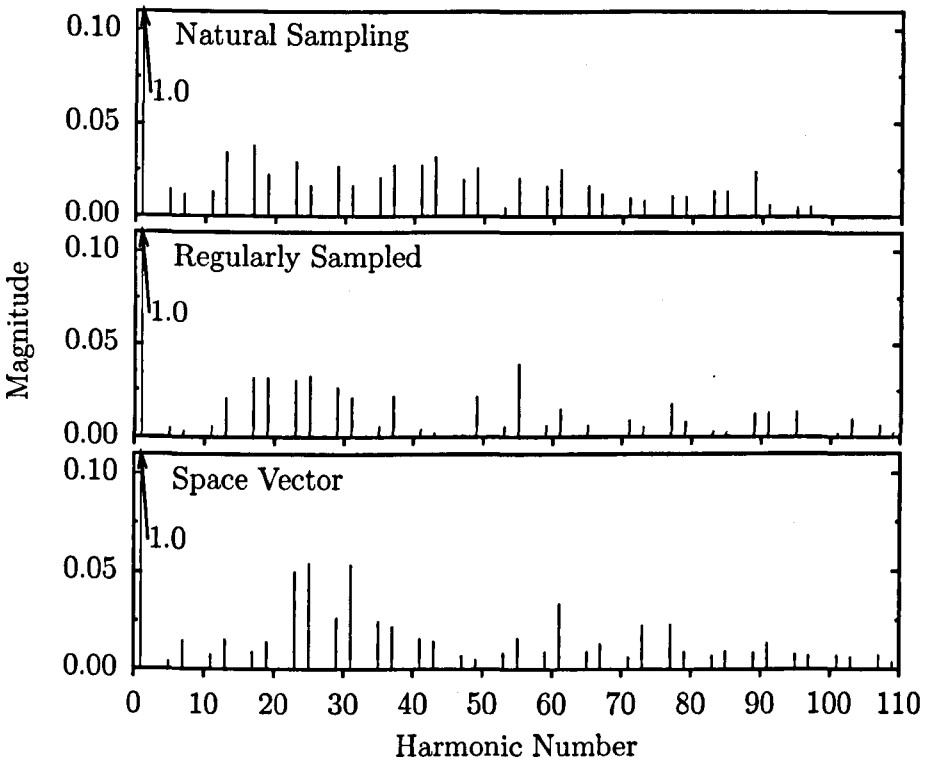


THD identified in Figure 4.23b. The voltage waveforms are clearly periodic and exhibit the half-wave and three-phase symmetries that, as discussed in section 4.2.2, are required in order to eliminate even harmonics, harmonics whose order is a multiple of three and inter-harmonics. The same symmetries are apparent in the current waveforms because of the balanced three-phase load.

4.5.2 Modulation in Closed Loop

The converter has also been operated using closed-loop current control with the same highly resistive load. For this test the converter is still operating as an inverter but the current is now controlled.

The voltage and current from phase a are shown in Figure 4.38 for three steady-state operating conditions. Details of the operating points are given in Table 4.4 and the frequency spectrum of the line voltages are shown in Figure 4.39. Each graph in Figure 4.39 includes spectrum of the measured line



voltage and the spectrum of the demanded switching function captured from the memory of the DSP.

Case 1 In the first case, the converter operates at the point of minimum THD identified in Figure 4.23b. Harmonics below the 23^{rd} are barely visible apart from a small fifth harmonic of the line voltage that is not present in the demanded switching function.

Case 2 The second example has a higher modulation index and the initial angle is synchronized to a constant at 12°. The line-voltage spectrum has a collection of harmonics around the 15^{th} which are not present in the first case.

Case 3 In the third case, the modulation index is the same as for Case 2 but the initial angle is controlled to obey (4.17). Low order harmonics are visibly reduced in magnitude compared to the second case, but not as far as in Case 1. This is to be expected as the operating point for Case

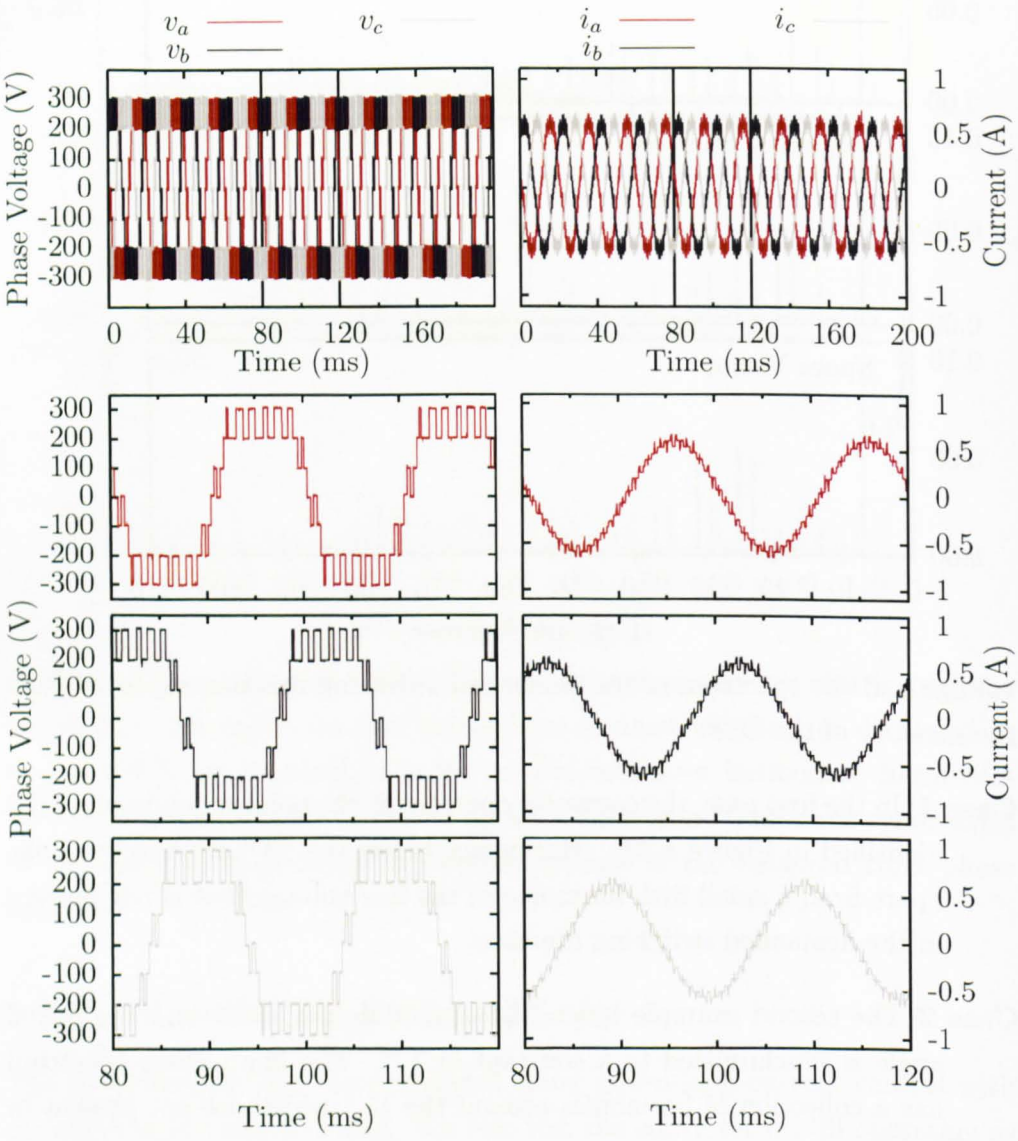


Figure 4.37: Phase voltages and currents from the experimental converter inverting in open-loop with $\hat{s} = 3$ and $\theta_0 = 12°$

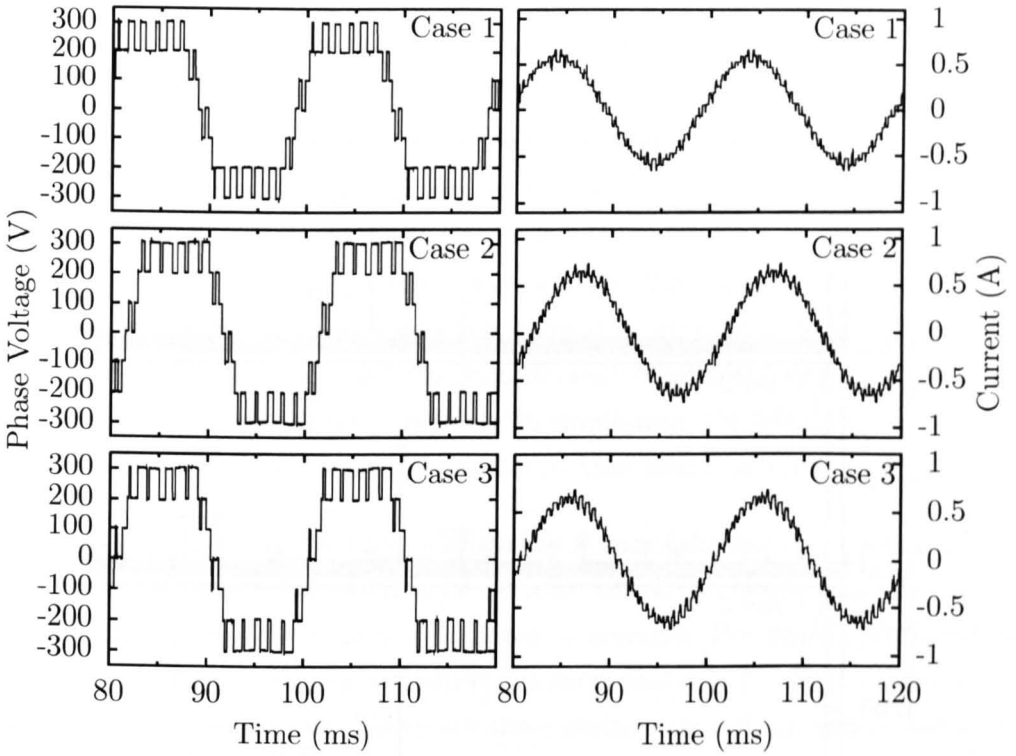


Figure 4.38: Phase-a voltages and currents from the converter operating in closed-loop, inverting mode in three steady-state conditions

Case	i_d^* (mA)	i_q^* (mA)	I_{a1} (mA)	θ_0 (°)	$\hat{s}$
1	870	0	410	12(fixed)	2.9
2	960	0	450	12(fixed)	3.3
3	960	0	450	8.5(variable)	3.3

Table 4.4: Operating points of closed-loop results in Figure 4.39.

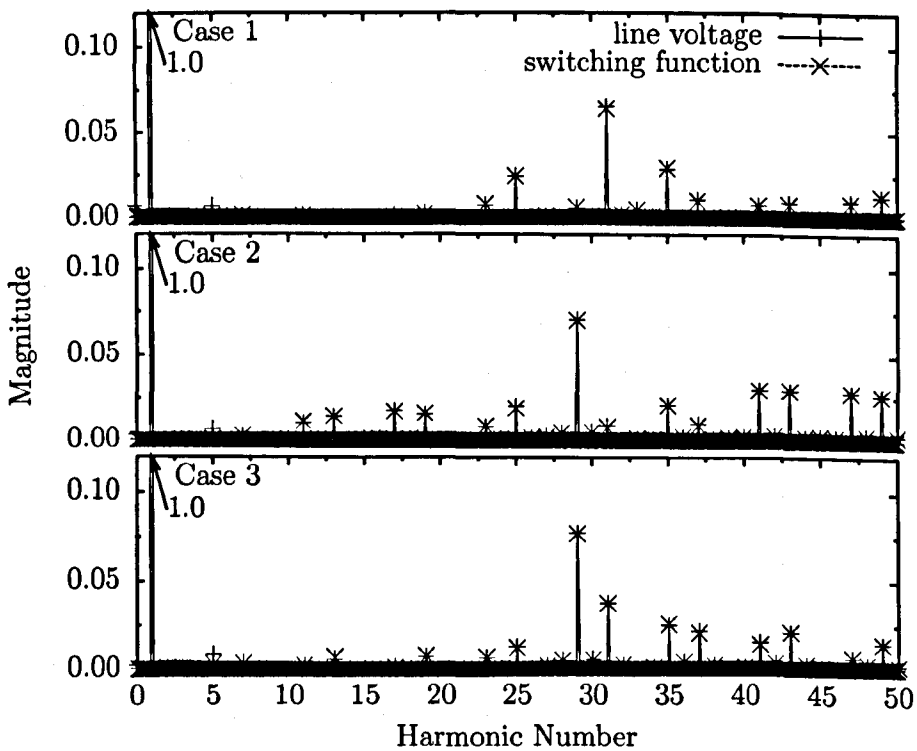


Figure 4.39: Line voltage spectrum from the experimental converter operating in closed-loop inverting mode with low current.

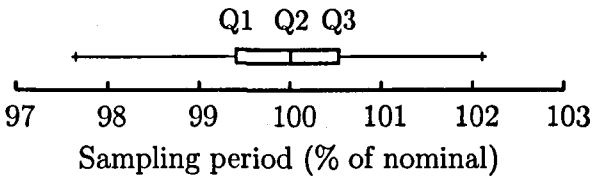


Figure 4.40: Jitter of sampling period for experimental case 3

1 was deliberately chosen to give the lowest achievable THD.

In the third case the converter is operated in a region where the sampling angles are controlled to vary with modulation index. As for the simulated examples, this causes jitter of the sampling period. The amount of sampling period jitter is shown in Figure 4.40. There is more jitter in the experimental case than was observed in simulations, with a range of $\pm 2.3\%$ and an inter-quartile range of 1.1%. The two major contributions to the jitter in the experimental converter are greater levels of noise in the control variables and the requirement to track the supply angle. Despite there being more jitter than in simulation, the frequency spectra in Figure 4.39 do not show any problems that could be attributed to jitter.

In all three cases there is a small fifth harmonic of the line voltage that is not present in the demanded switching functions, which can be identified by the + markers in Figure 4.39 without coincident × markers. Harmonics produced in the line voltage but not the switching function can only be due to differences between these two signals. There are three main causes of differences between the two signals:

1. The switching devices are not ideal switches and are not able to produce an instantaneous change in voltage level.

2. A short dead-time is introduced to prevent shoot-through.

3. Despite the low current, the capacitor voltages are not constant.

Differences between the demanded and actual waveforms due to capacitor voltage ripple are investigated further in Chapter 5

4.6 Summary

This chapter has discussed an implementation of synchronized space-vector modulation for multi-level converters subject to the assumption that the converter includes ideal, constant d.c. voltage sources. In order to make the best use of the available switching frequency, the modulation is asymmetrical so that the sequences of vectors used to produce each sample of the reference vector alternate between producing rising and falling edges on each phase. This property is maintained even though consecutive samples do not occupy the same triangle.

A simulation study has been used to investigate the quality of the output waveforms in terms of total harmonic distortion and total device switching frequency. The modulation index and the initial sampling angle have been varied and the effect on the total number of commutations and on the THD investigated. A band of increased switching frequency was observed at the boundary between 5- and 7-level output waveforms caused by the restriction of possible starting vectors for each sequence.

The effects of modulation index and initial sampling angle on the THD have been used to develop an algorithm that varies the initial sampling angle in response to the demanded modulation index. The proposed algorithm prevents the converter from operating under conditions that lead to particularly high THD and, where possible, acts to minimize the THD. The behaviour of the algorithm has been verified with simulations and using the experimental converter. The experimental tests were operated with low current in order for the assumption that the d.c. links have constant voltage to apply.

Chapter 5

Space-Vector Modulation when the d.c. Links are not Ideal

In Chapter 4, the details of space-vector modulation were discussed for the case where the d.c.-link voltages are constant and equal. In practice, the capacitor voltages are not constant and special attention must be paid to the modulation to ensure the capacitor voltages of each cell remain close to equal.

This chapter discusses modifications to space-vector modulation in order to handle two problems associated with non-ideal d.c. links. The first is the tendency for the capacitor voltages to diverge if different amounts of power are delivered to, or drawn from, each cell. Such differences in power flow can be due to the modulation scheme, external loads or different internal losses. The divergence of capacitor voltages is particularly relevant when the H-bridge cells are not supplied by d.c. sources as the divergence accumulates over time to produce large differences between the capacitor voltages.

In section 5.1 the problem of equalizing the capacitor voltages is studied for the case where different resistive loads are applied to the converter cells. Limits are derived defining the difference in loads for which the capacitor voltages can be kept equal. A method is then presented that applies redundant states in order to force the capacitor voltages to converge even when different loads are applied to each d.c. link. Because of the importance of not increasing the switching losses, the balancing algorithm is developed so that it does not cause

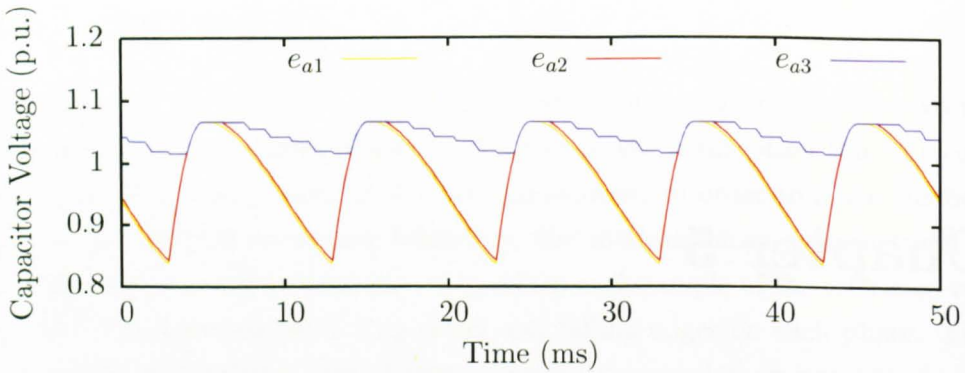


Figure 5.1: Imbalance of capacitor voltages when space-vector modulation is used without consideration of voltage balancing

the total device switching frequency to increase.

The second effect of non-ideal d.c. links is capacitor voltage ripple. Because the cascaded H-bridge is constructed of multiple single-phase converters, each cell is subject to power pulsations at twice the fundamental supply frequency that cause the capacitor voltages to vary. In section 5.2, the effects of ripple on the geometry of the space-vector diagram and on the spectra of the line-to-line voltages are analysed. A new geometrical feed-forward method is proposed to correct for the ripple in section 5.3.

5.1 Balancing of Capacitor Voltages

If the modulation scheme applied to a cascaded H-bridge converter does not draw power equally from each cell or if the loads or losses in each cell are different, then the capacitor voltages tend to diverge. In the case where there is no external supply this divergence leads to a steady-state condition with different capacitor voltages in each cell [100]; in extreme cases the capacitor voltage of one cell can collapse completely. If the bridges are supplied by a diode rectifier, the capacitor voltages diverge during the discharge period, as shown in Figure 5.1. Both of these effects influence the cancellation of harmonics between the cells and reduce the quality of the a.c. waveforms.

In Chapter 4, the redundant states of the line-to-line voltages of the three-

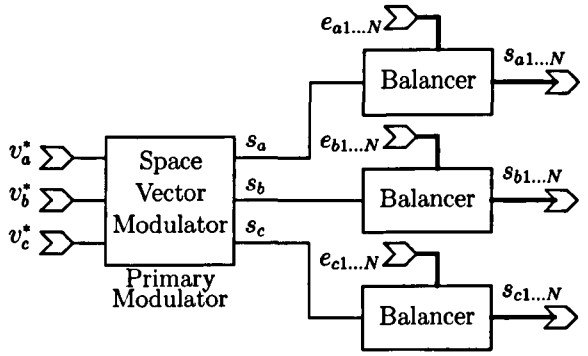


Figure 5.2: Relationship between primary modulation and balancing controller for three-phase converter

phase cascaded H-bridge were selected in order to minimize the total number of commutations required but no rule was applied to choose redundant states of the individual phase legs. The balancing methods discussed in this section use the redundancy of the phase legs in order to equalize the capacitor voltages on a single-phase basis. As shown in Figure 5.2, the primary modulation determines the switching function for each phase leg, $s_{a,b,c}$, and the balancing algorithm constructs the switching functions of the individual bridges in order to adjust the power flow to each cell.

Similar methods that use redundant states of the phase legs to balance the capacitor voltages have been presented previously in [26] and [101]. In [26], the commutations demanded by level-shifted carrier modulation are assigned to suitable bridges using a fixed rotation scheme that is easily implemented in an FPGA. This method does not measure the capacitor voltages and cannot force the capacitor voltages to converge if the loads of each bridge differ. In [101] the capacitor voltages are measured and a list of bridges that is sorted in order of the capacitor voltages is used to assess the balancing requirement. However, this balancing method explicitly allows the device switching frequency to increase above the rate demanded by the primary modulator.

The balancing method proposed in this chapter (section 5.1.2) can be seen as a combination of the methods in [26] and [101]. A list of bridges sorted in order of the capacitor voltages is used to assign individual commutations

to bridges in such a way as to balance the capacitor voltages but without introducing additional commutations.

5.1.1 Theoretical Limits of Balancing Algorithms

Before discussing the specific balancing algorithm, some general limits are derived for the degree of load imbalance for which it is possible to balance the capacitor voltages. By first deriving these limits it is possible to test the effectiveness of specific algorithms against the expected general case.

The system being considered in this section is the cascaded H-bridge converter in rectifying configuration with different resistive loads applied to each d.c. link (Figure 5.3a). Only one phase leg is considered because an independent balancing controller is applied to each phase of the three-phase system (Figure 5.2).

Figure 5.3b shows a simplified averaged-model circuit for a single-phase, N-cell converter, which is the basis for the following analysis. In the equivalent circuit, the averaged switching function is separated into individual components, $\langle s_n \rangle$, acting on each bridge. Current is delivered to the d.c. links and voltage to the a.c. side via controlled current and voltage sources. In this section, the averaged switching functions and the a.c.-side current are assumed to be sinusoidal.

Under these assumptions, the current on the d.c. side of each H-bridge in Figure 5.3 is given by the following equations.

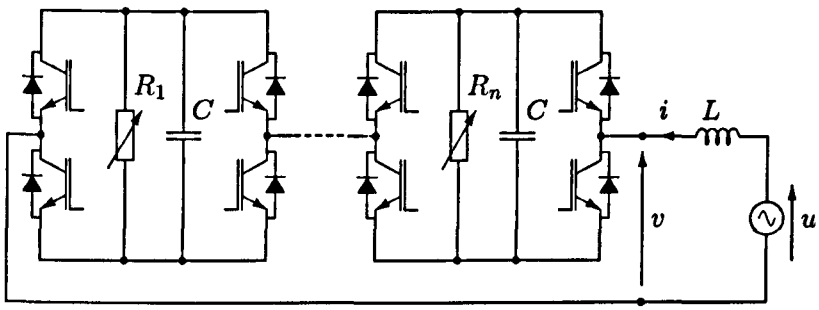
$$\begin{aligned} \langle s_n \rangle i &= \hat{s}_n \cos(\omega t) \hat{i} \cos(\omega t + \phi_n) \\ &= \frac{1}{2} \hat{i} \hat{s}_n \left[\cos(\phi_n) + \cos(2\omega t + \phi_n) \right], \end{aligned} \tag{5.1}$$

where

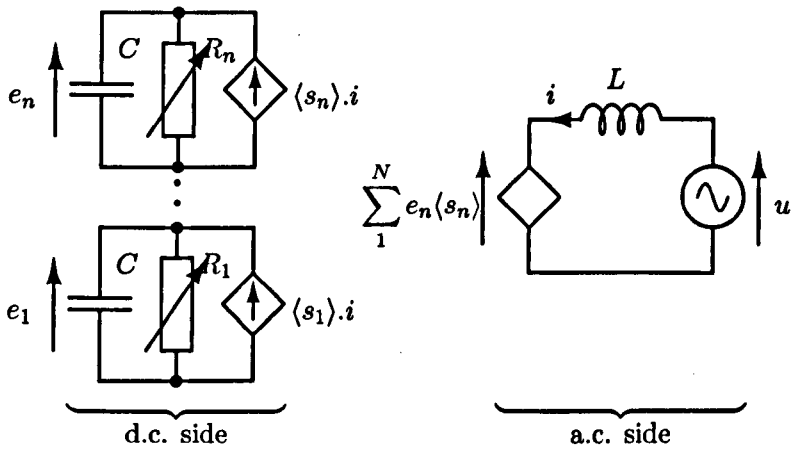
$\hat{s}_n$ is the modulation index of the n^{th} cell,

$\hat{i}$ is the peak, fundamental a.c. current and

ϕ_n is the phase difference between the a.c. current and the fundamental of the switching function of the n^{th} cell.



(a)



(b)

Figure 5.3: N-cell cascaded H-bridge in rectifying configuration with different resistances in each cell. (a) Power circuit (b) averaged equivalent circuit

The two terms of (5.1) show the mean, steady-state capacitor voltage, which is of interest in this section, and the single-phase voltage ripple, which is considered in more detail in section 5.2.

The constant term in (5.1) gives the mean, steady-state capacitor voltage of each cell:

$$\bar{e}_n = \frac{1}{2} R_n \hat{i} \hat{s}_n \cos(\phi_n).$$

If the modulation maintains balanced capacitor voltages then

$$\bar{e}_1 = \bar{e}_2 = \ldots = \bar{e}_N \tag{5.2}$$

and therefore

$$R_1 \hat{i} \hat{s}_1 \cos(\phi_1) = R_2 \hat{i} \hat{s}_2 \cos(\phi_2) = \ldots = R_N \hat{i} \hat{s}_N \cos(\phi_N).$$

In rectifying mode, where the active power demand is significantly greater than the reactive power demand, the phase angles are expected to be close to zero. Small variations in phase angle around zero have little influence on the values of the cosine terms so they can be assumed to be equal.

$$R_1 \hat{s}_1 = R_2 \hat{s}_2 = \ldots = R_N \hat{s}_N \tag{5.3}$$

Balancing algorithms act to distribute power flow between the individual cells but the total modulation index, $\hat{s}$, of the phase leg is set by the external demand. Continuing with the assumption that the cosine terms can be neglected, the total modulation index is the sum of the individual modulation indices.

$$\hat{s}_1 + \hat{s}_2 + \ldots + \hat{s}_N = \hat{s} \tag{5.4}$$

Hence the balancing procedure does not influence the fundamental voltage produced on the a.c. side.

Equations (5.3) and (5.4) have the same structure as the voltages and currents in the parallel combination of resistors shown in Figure 5.4, in which the modulation indices of the cells are represented by the currents in the resistors and the total modulation index, $\hat{s}$, is represented by a current source. Each

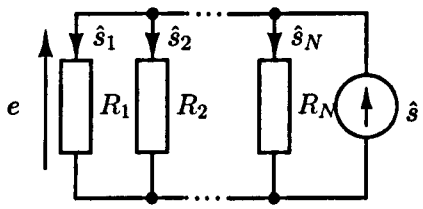


Figure 5.4: Circuit representation of equations (5.3) and (5.4)

modulation index can be determined from the current divider created by the parallel combination of resistors.

$$\hat{s}_n = \frac{\hat{s}}{1 + \frac{R_n}{R_{tn}}}, \tag{5.5}$$

where R_{tn} is the result of the parallel combination of all the resistors apart from the n^{th}:

$$R_{tn} = \left(\sum_{\substack{r=1 \\ r \neq n}}^{N} \frac{1}{R_r} \right)^{-1}.$$

The maximum possible modulation index of a cell is achieved when that cell produces a square wave between ± 1; hence

$$\hat{s}_n \leq \frac{4}{\pi}$$

which, when substituted into (5.5), gives

$$R_n \geq R_{tn}(\tfrac{\pi}{4}\hat{s} - 1). \tag{5.6}$$

For an N-cell converter, an equation of the form (5.6) applies to each resistor. For a seven-level converter there are three equations, which produce a three-dimensional region whose shape depends on the total modulation index. Two cases are plotted in Figures 5.5 and 5.6 for $\hat{s} = 3.3$ and $\hat{s} = 2.6$ respectively. In both figures, the region within which the capacitor voltages can be kept equal is contained between the three surfaces. The higher total

modulation index in Figure 5.5 results in a smaller region than in Figure 5.6 because there is less freedom to adjust the modulation indices of the individual cells before one cell reaches its maximum modulation index.

An interesting special case to consider is the case where one resistance, R_1, is varied and the others are held constant and equal with a value R. In the case of the seven-level converter $R_2 = R_3 = R$ so

$$R_1 \geq \frac{R}{2}(\tfrac{\pi}{4}\hat{s}) \tag{5.7}$$

and

$$R \geq \frac{RR_1}{R+R_1}(\tfrac{\pi}{4}\hat{s}). \tag{5.8}$$

These can be re-arranged to show the limits of the ratio $\frac{R_1}{R}$ in terms of the total modulation index $\hat{s}$:

$$\frac{R_1}{R} \geq \frac{1}{2}(\tfrac{\pi}{4}\hat{s})$$

and

$$\frac{R_1}{R} \leq \frac{1}{\frac{\pi}{4}\hat{s}-2} \text{ when } \hat{s} > \frac{8}{\pi}.$$

The resulting region of acceptable resistances is shown as the un-shaded region in Figure 5.7.

Figure 5.7 has three distinct regions:

$0 < \hat{s} < \frac{4}{\pi}$ In this region there is a steady-state condition for which it is possible to maintain equal capacitor voltages for any value of R_1. Although this region offers the most flexibility, it is unlikely that a multi-level converter would be operated in this region as such a low modulation index does not use the full number of levels and the capacitor voltages have to be very high in order to match the supply voltage with the converter output. Operating a multi-level converter in this region negates the advantages of the multi-level output waveform.

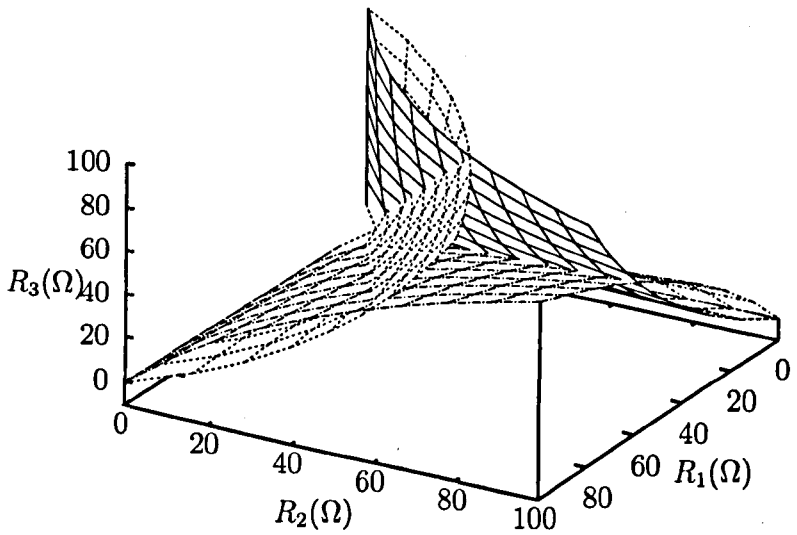


Figure 5.5: Limits of resistance for balancing with total converter modulation index $\hat{s} = 3.3$

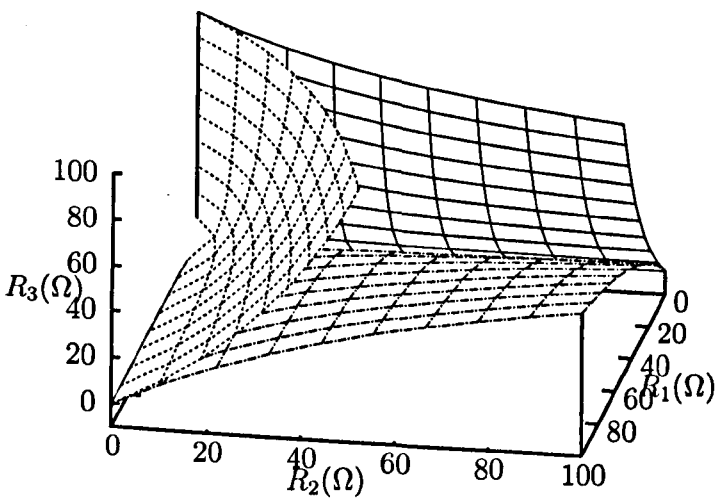


Figure 5.6: Limits of resistance for balancing with total converter modulation index $\hat{s} = 2.6$

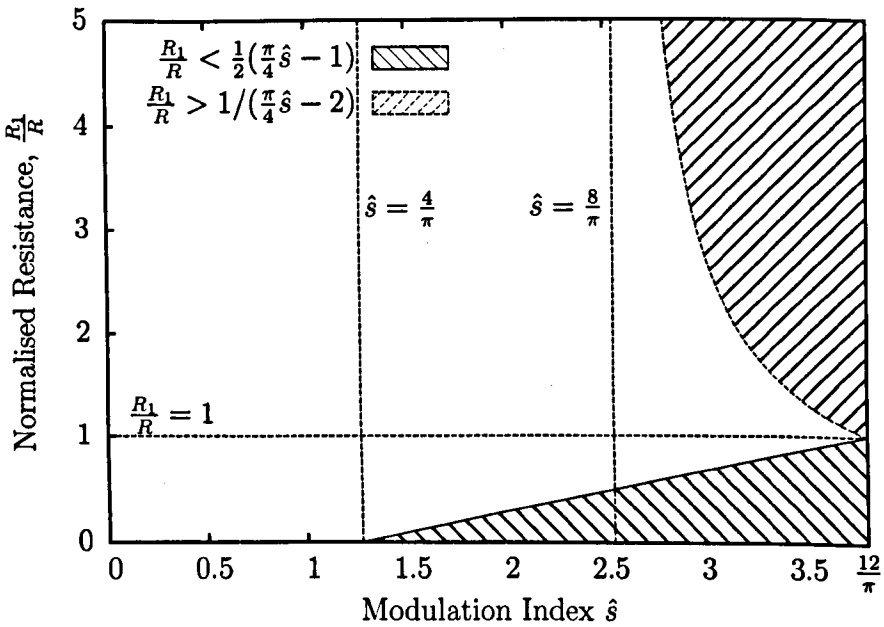


Figure 5.7: Ranges of $\frac{R_1}{R}$ for which capacitor voltages of a three-cell cascaded H-bridge can be balanced, where $R_2 = R_3 = R$

$\frac{4}{\pi} < \hat{s} < \frac{8}{\pi}$ In this region there is a limit to how low R_1 can be compared to the other resistor values, as defined in (5.7). There is no upper limit because (5.8) is true for all ratios in this range. The parallel combination of R and R_1 is always less than R and the $\frac{\pi}{4}\hat{s}$ term is less than one for this range of $\hat{s}$.

$\frac{8}{\pi} < \hat{s} < \frac{12}{\pi}$ In this region, low ratios are restricted as before and the upper limit reduces for increasing R_1 because the $\frac{\pi}{4}\hat{s}$ term increases the value of the right hand side of (5.8). When $\hat{s} = \frac{12}{\pi}$ there is no longer any scope for capacitor balancing as all three bridges produce square waves.

This analysis has shown the ranges of resistor values within which capacitor voltages can theoretically be kept equal whilst the converter is configured to draw real power. The external constraints of the a.c. circuit and control system, including the physical voltage and current limits of the converter, are not included in Figures 5.5 to 5.7. Before identifying whether or not the capacitor voltages can be balanced with a given load, phasor analysis must first be

performed to confirm that the loading condition is within the limits of the converter and to identify the required modulation index. The modulation index obtained from phasor analysis can then be used to refer to Figure 5.7 or to (5.6) to determine if the capacitor voltages can be balanced.

5.1.2 Capacitor Balancing Algorithm

Having discussed the limitations of capacitor balancing, a balancing algorithm applicable to space-vector modulation is now proposed. The proposed algorithm is of the form of Figure 5.2, where the primary modulator determines the overall switching functions of the phases and the balancing algorithm constructs the switching functions of each bridge to balance the capacitor voltages on a per-phase basis. Because the primary modulator determines the timing of the switching edges, neither the phases nor the modulation indices of the bridges are explicitly controlled.

The basis of the proposed balancing algorithm is the sign of the quantity $i\Delta s$: that is the product of the a.c. current, i, and the direction of the demanded state change, Δs. The importance of this quantity is derived from the path of the current through the capacitor in each of the switching states of a single bridge shown in Figure 5.8.

First consider a bridge in the negative state (Figure 5.8a). With the a.c.-side current flowing into the bridge as shown, the current flow causes the capacitor to discharge. A positive state change would place the bridge into the zero state (Figure 5.8b) causing the capacitor to stop discharging; a further positive step, now into the positive state (Figure 5.8c), would cause the capacitor to charge. Either of these changes, that is charging or ceasing to discharge the capacitor, is of most benefit to the bridge with the lowest capacitor voltage.

Alternatively, if the direction of the current is reversed, the effect of two positive state changes would be to stop the capacitor from charging and then to start discharging the capacitor. Either of these changes is of most benefit to the bridge with the greatest capacitor voltage. Similar arguments can be applied for negative steps with current flow in either direction.

The effects of every possible change of state for a single H-bridge are sum-

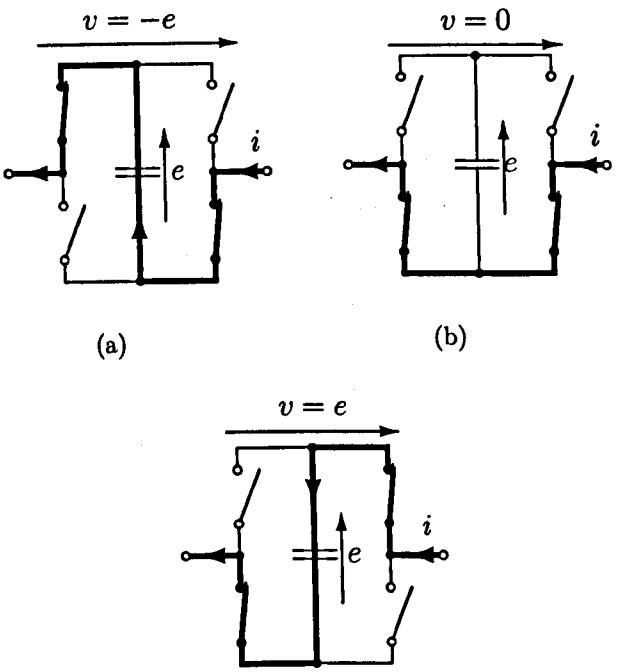


Figure 5.8: Influence of positive a.c.-side current in different H-bridge states. (a) The negative state discharges the capacitor, (b) the zero state does not affect capacitor and (c) the positive state charges the capacitor.

State Transition		Δs	sign i	$i\Delta s$	e Transition			e Net Change
$-1 \rightarrow$	0	+	+	+	$\Downarrow$	$\rightarrow$	=	$\uparrow$
$0 \rightarrow$	1	+	+	+	=	$\rightarrow$	$\Uparrow$	$\uparrow$
$1 \rightarrow$	0	−	+	−	$\Uparrow$	$\rightarrow$	=	$\downarrow$
$0 \rightarrow$	−1	−	+	−	=	$\rightarrow$	$\Downarrow$	$\downarrow$
$-1 \rightarrow$	0	+	−	−	$\Uparrow$	$\rightarrow$	=	$\downarrow$
$0 \rightarrow$	1	+	−	−	=	$\rightarrow$	$\Downarrow$	$\downarrow$
$1 \rightarrow$	0	−	−	+	$\Downarrow$	$\rightarrow$	=	$\uparrow$
$0 \rightarrow$	−1	−	−	+	=	$\rightarrow$	$\Uparrow$	$\uparrow$

Key: $\Downarrow$: Capacitor discharging, = Zero state, $\Uparrow$: Capacitor charging, $\downarrow$: Net reduction in capacitor voltage, $\uparrow$: Net increase in capacitor voltage

Table 5.1: The effect of voltage steps on the capacitor voltage

marized in Table 5.1 for positive and negative a.c. current. The important relationship deriving from Table 5.1 is that the polarity of $i\Delta s$ (shown in bold) is the same as the net change in capacitor voltage (also shown in bold) caused by the commutation of the bridge. The *net change* in capacitor voltage can be interpreted as the contribution of the commutation to the capacitor voltage; hence both charging the capacitor and ceasing to discharge it can be considered as positive contributions because in both cases the capacitor voltage after the commutation is greater than it would have been had the commutation not occurred.

The algorithm for choosing bridges to commutate based on the polarity of $i\Delta s$ is shown in Figure 5.9, in which the sign() function is defined in (5.9).

$$\text{sign}(x) = \begin{cases} 1 & \text{if } x >= 0 \\ -1 & \text{otherwise} \end{cases} \tag{5.9}$$

First the bridges are sorted into order of capacitor voltage with s_0 being the state of the bridge with the lowest capacitor voltage and s_N being the state of the bridge with the greatest capacitor voltage. Then the flow chart in Figure 5.9 is followed to determine which bridge should apply the demanded step, Δs.

If $i\Delta s$ is positive then the search begins at the bridge with the lowest

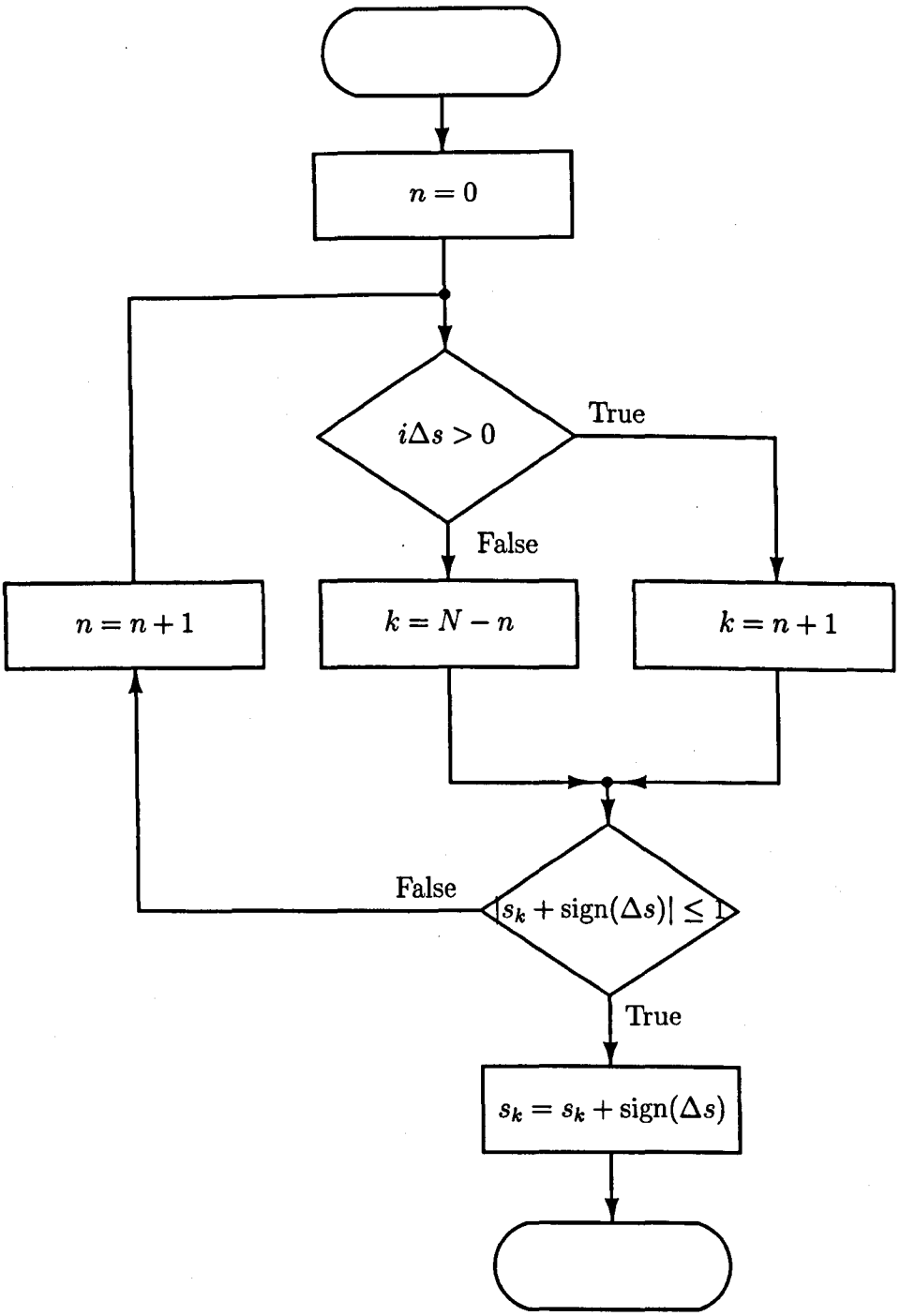


Figure 5.9: Choice of bridge to perform each commutation.

capacitor voltage or, if $i\Delta s$ is negative, the search begins at the bridge with the greatest capacitor voltage. The inequality (5.10) identifies whether or not the chosen bridge can produce a step in the required direction.

$$|s_k + \text{sign}(\Delta s)| \leq 1 \tag{5.10}$$

If (5.10) is false then the k^{th} bridge cannot provide a step in the desired direction, for instance if a positive step is demanded when the bridge is already in the positive state. In this case, the next bridge in the list is tried until a bridge is found that can perform the desired state change. If the primary modulator is working correctly and only demanding states within the range that the converter can output, this loop will always find a bridge to apply the voltage step.

When the modulator demands a state change greater than one, perhaps in response to a transient, each demanded step is assigned to a bridge through repeated application of the same algorithm.

This proposed balancing method is general and can be applied to converters containing any number of cells. The only difference in implementation is the number of capacitor voltages being sorted and the possible number of iterations in the search loop, both of which increase with the number of cells. Note also that the balancing algorithm does not require the primary modulation to be based on space-vectors. Carrier-based modulation could be used to choose the output level and commutation instant with the balancing algorithm assigning those edges to the appropriate bridge.

5.1.3 Limits of Proposed Balancing Algorithm

The balancing algorithm proposed in section 5.1.2 has been tested using a simulation of a three-phase, 7-level converter in rectifying configuration. To unbalance the power flow in each cell, the resistive loads can be altered (Figure 5.10). A number of loading conditions have been considered in order to to verify both the performance of the balancing algorithm and the applicability of the analysis of limits derived in section 5.1.1.

The converter has been simulated in each of the operating points marked

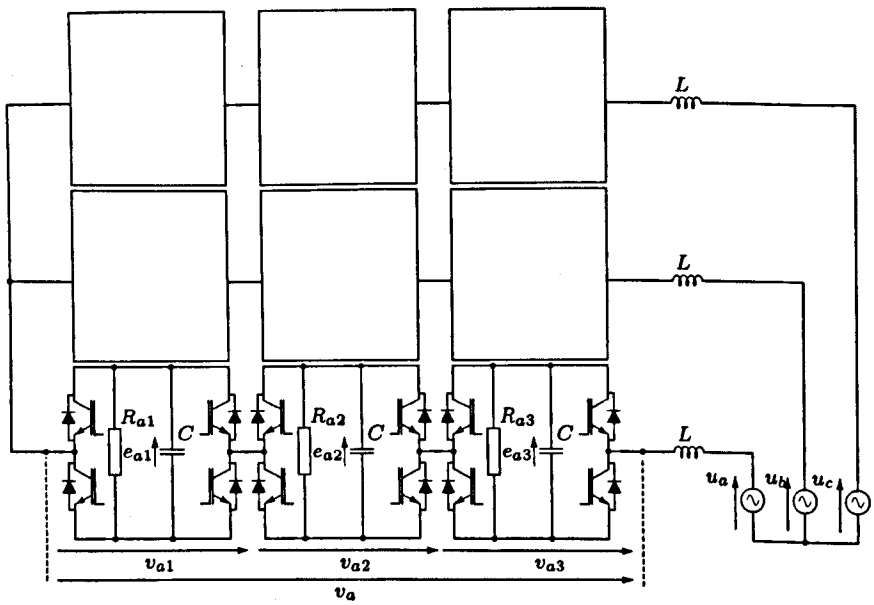


Figure 5.10: Circuit configuration for tests of the balancing algorithm

A to H in Figure 5.11. For each loading condition, two values of modulation index were considered by altering the ratio of supply voltage to d.c.-link voltage reference, $\frac{u}{E^*}$. The phasor diagrams in Figure 5.11 show the effect that the changes in load and in capacitor voltage have on the a.c. circuit.

Figure 5.12 shows that the balancing algorithm is successful at balancing the capacitor voltages for operating points tested within the unshaded region in Figure 5.11 (cases A and C to F). Outside this region, for cases B and H, the balancing algorithm is unable to balance the capacitor voltages. It is of particular interest that operating points A and G, for which the capacitor voltages can be balanced, share the same loads as operating points B and H, for which the capacitor voltages cannot be balanced. The only difference between cases A and B and between cases G and H is the modulation index of the converter. Hence, as derived in section 5.1.1, the converter modulation index influences the range of imbalanced loads for which it is possible to balance the capacitor voltages.

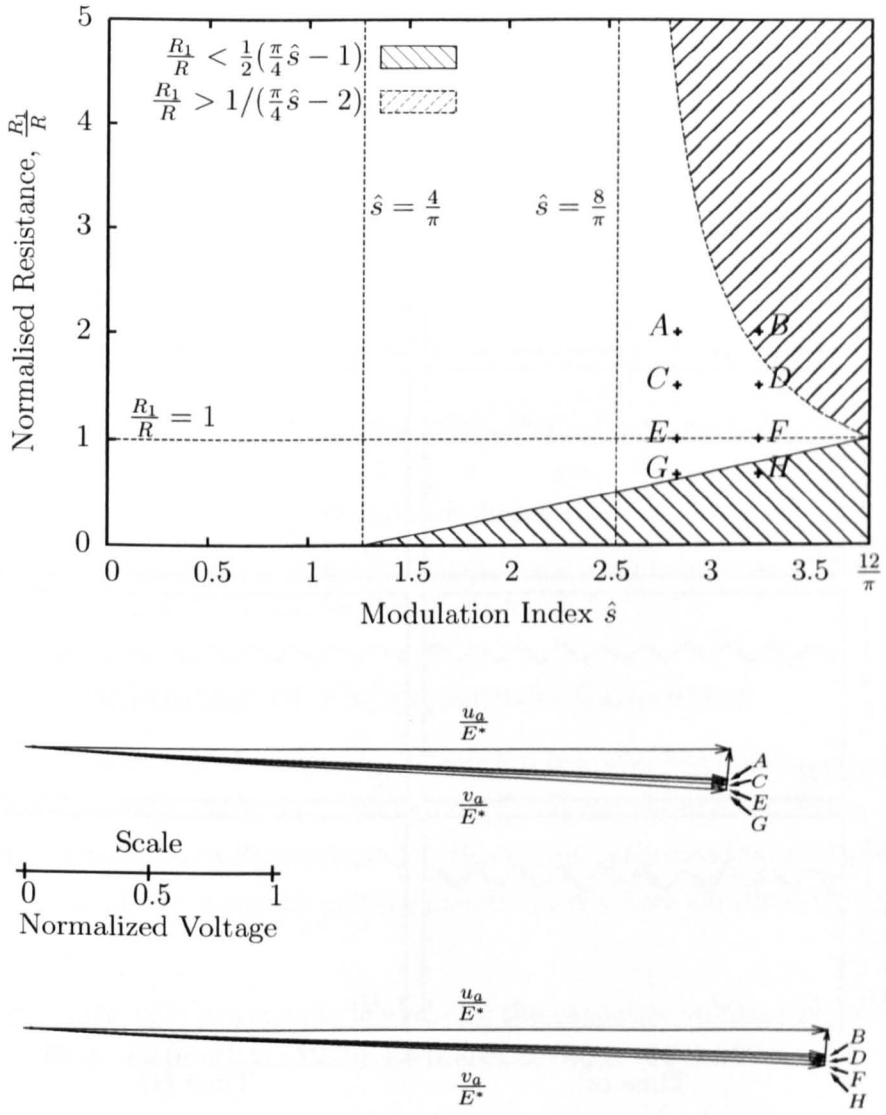


Figure 5.11: Operating points for simulations in relation to limitations defined in section 5.1.1 and as phasor diagrams

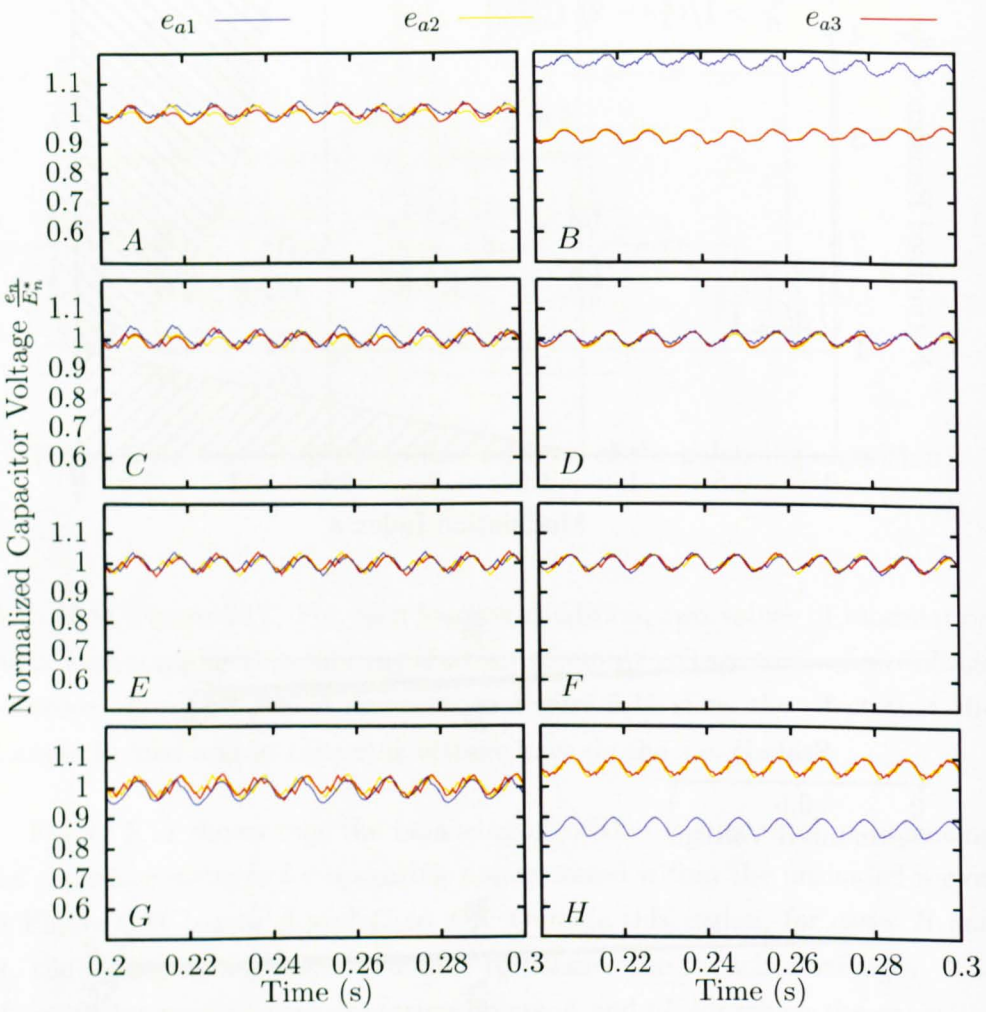


Figure 5.12: Simulated steady-state capacitor voltages at operating points corresponding to each of the points marked in Figure 5.11.

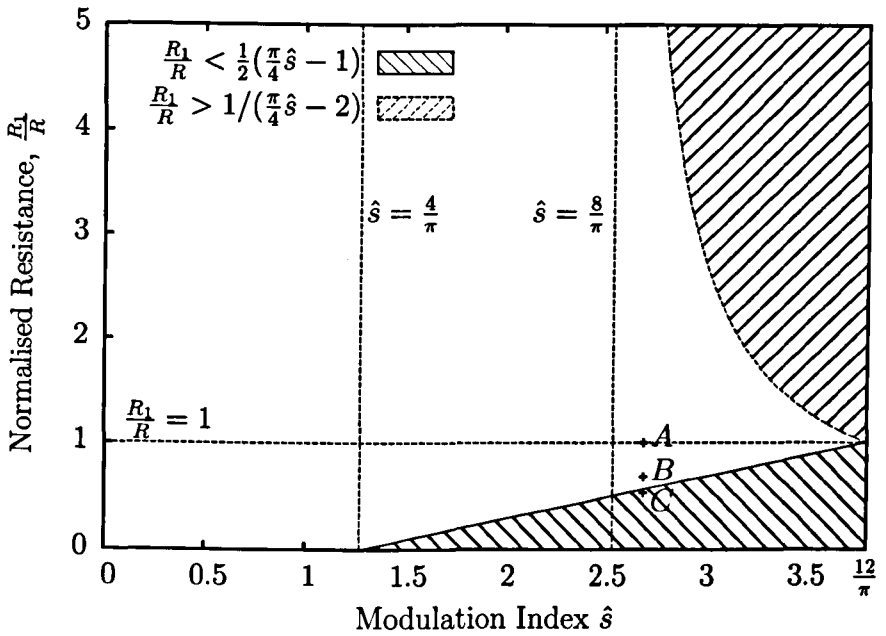


Figure 5.13: Operating points for experimental tests in relation to limitations defined in section 5.1.1 and as phasor diagrams

5.1.4 Balancing of Experimental Converter

The performance of the balancing algorithm has also been investigated using the experimental converter. The behaviour for the three cases shown in Figure 5.13 are shown in Figure 5.14. For this figure, the individual gate switching functions and the capacitor voltage measurements were captured through the DSP.

Case A The cells are equally loaded and the capacitor voltages are balanced. The commutations are spread evenly between the cells.

Case B The cells are imbalanced but the balancing algorithm is able to maintain balance. The third cell, which is most heavily loaded, commutates less often than the other two cells.

Case C The cells are heavily unbalanced and the converter is unable to keep the capacitor voltages equal because the operating point is beyond the limits defined in section 5.1.1.

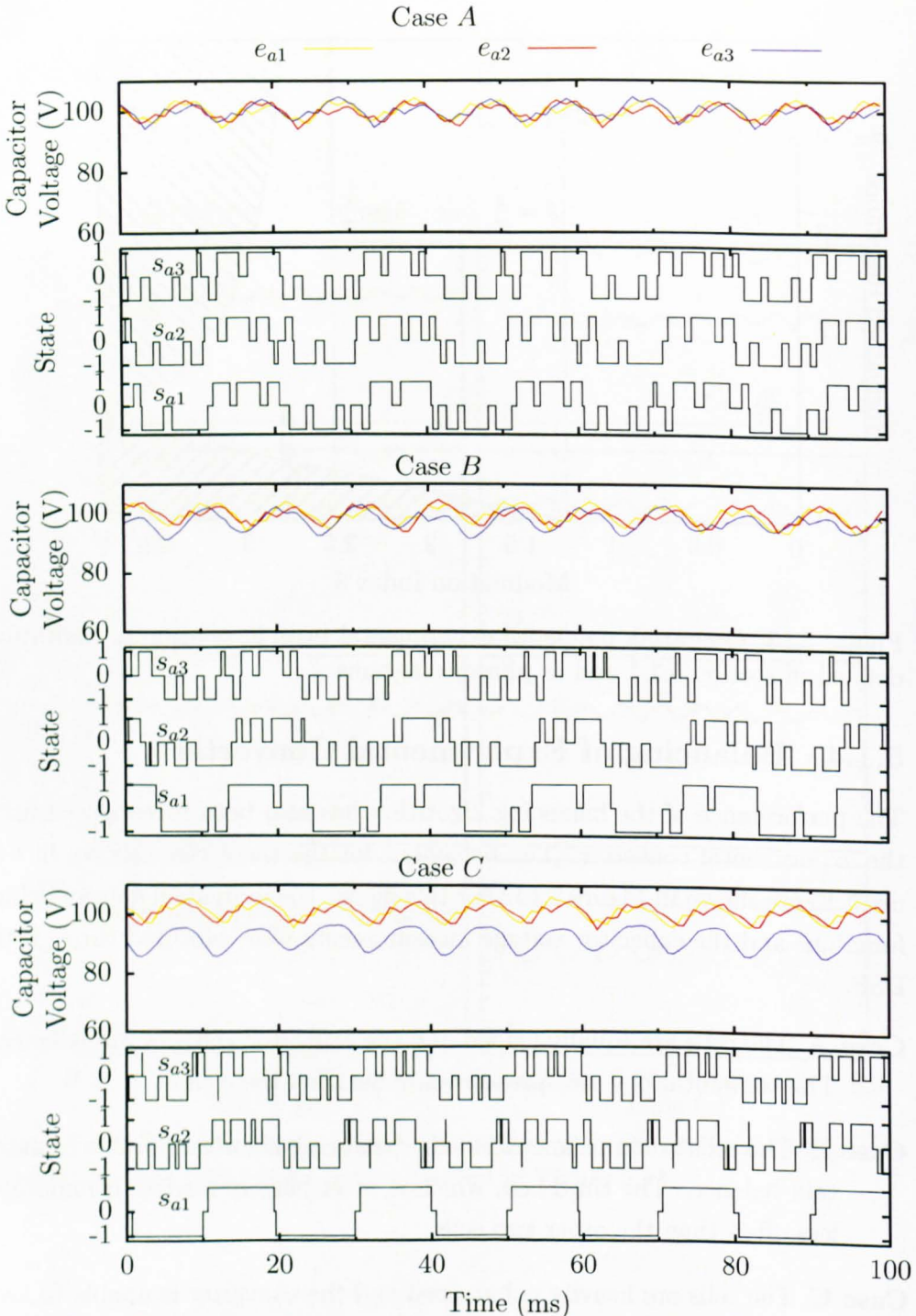


Figure 5.14: Capacitor voltages and bridge switching functions from one phase of a 7-level cascaded converter

Figure 5.14 shows that the balancing of the capacitor voltages is achieved by re-distributing the commutations between the converter cells. This approach has important implications for the lifetime of the converter as regularly operating the cells with different loads may cause one cell to fail early. Similarly, the converter cells must be able to tolerate the maximum switching frequency demanded by the balancing controller. It is possible that the level of imbalanced switching frequency that a full-scale converter can tolerate would define the loads that can be applied instead of the theoretical limits defined in section 5.1.1.

5.2 Capacitor Voltage Ripple

The second problem associated with non-ideal d.c. links is ripple of the capacitor voltages. Each phase leg of a three-phase cascaded H-bridge converter is a single-phase converter and is therefore subject to power pulsations that create capacitor voltage ripple at twice the fundamental modulating frequency. The ripple is due to the second term in (5.1) and is clearly visible in all the simulated and experimental results in section 5.1.

This section discusses the effect of ripple on space-vector modulation. The geometry of the space-vector diagram is analysed in order to investigate the effect of ripple on the spectrum of the line voltages. The same geometrical considerations are then used to propose a new method to compensate for ripple. Unlike the balancing algorithm, which works on a single phase basis, the analysis of the effect of capacitor voltage ripple is considered for the line voltages of a three-phase converter.

5.2.1 Refresher on Space-Vector Modulation

Before discussing the effects of capacitor voltage ripple it is useful to briefly repeat some details of the implementation of space-vector modulation discussed in Chapter 4.

The first key feature of the implementation is the (g, h) co-ordinate system, depicted in Figure 5.15. This co-ordinate system simplifies the implementa-

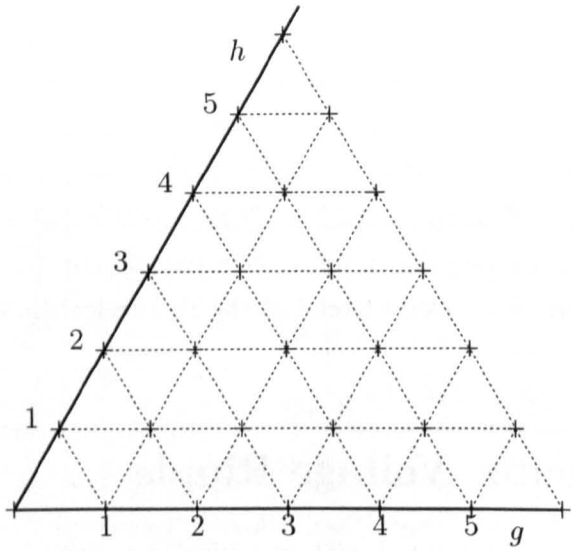


Figure 5.15: The (g, h) co-ordinate system

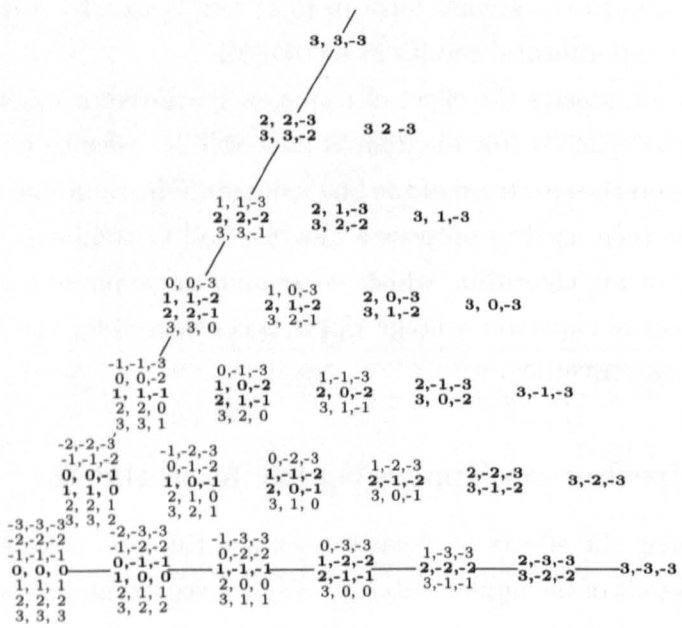


Figure 5.16: Redundant states in the first sector of the space-vector diagram

tion of space-vector modulation because the switching vectors have integer co-ordinates. Another important feature of the (g, h) co-ordinate system is that the g and h components of voltage vectors represent normalized versions of the $a - b$ and $b - c$ line voltages, respectively.

The second important feature of space-vector modulation is the choice of redundant switching states. In order to reduce the number of commutations required to fully traverse the space-vector diagram, only a subset of switching states are used. The states used in the first sector of a seven-level converter are shown in bold in Figure 5.16 and can be described in terms of the so-called *mean states*. The mean state of a given vector is simply the mean of all the switching states that can produce that vector. For vectors with an odd number of redundant states, this mean state has integer co-ordinates and hence is an actual switching state used for modulation. The mean state of a vector with an even number of redundant states is not a realizable state so the two redundant states obtained from rounding the mean state upwards and downwards are used to modulate.

Finally, it should be noted that the switching sequences applied in each sampling period start and end on a different redundant state of a vector with an even number of redundant states. The time for which this vector is applied is split evenly between the two redundant states at the start and the end of the sampling period.

5.2.2 The Effect of Ripple on the Space Vector Plane

The balancing algorithm described in section 5.1.2 works on a per-phase basis to equalize capacitor voltages but does not equalize the capacitor voltages in different phases. To demonstrate this, Figure 5.17 shows all of the capacitor voltages from the Case F simulation of the balancing algorithm from Figure 5.12. The capacitor voltages in each phase are balanced and the magnitude of the ripple is greater than the deviation of the individual capacitor voltages. Hence, the capacitor voltages of each phase leg can be considered in terms of the mean of the capacitor voltages in that leg.

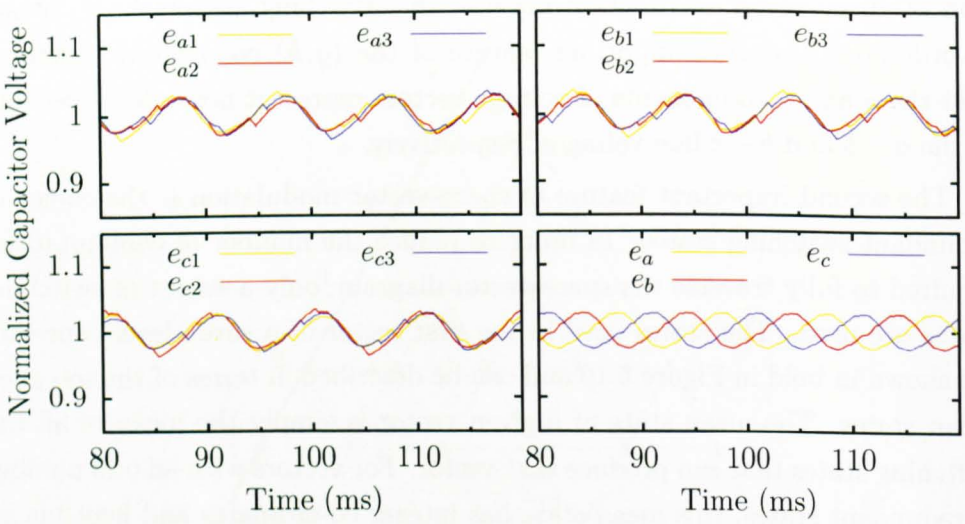


Figure 5.17: All the capacitor voltages from the Case F simulation in Figure 5.12

$$e_a(t) = \sum_{n=1}^{N} e_{an}(t), \quad e_b(t) = \sum_{n=1}^{N} e_{bn}(t), \quad e_c(t) = \sum_{n=1}^{N} e_{cn}(t).$$

Variations in the capacitor voltages cause the voltage vectors produced by each switching state to move on the space-vector diagram. Using the mean capacitor voltages, this movement can be described in terms of the (g, h) co-ordinate system.

$$\begin{pmatrix} v_g \\ v_h \end{pmatrix} = \frac{1}{E} \begin{pmatrix} 1 & -1 & 0 \\ 0 & 1 & -1 \end{pmatrix} \begin{pmatrix} e_a & 0 & 0 \\ 0 & e_b & 0 \\ 0 & 0 & e_c \end{pmatrix} \begin{pmatrix} s_a \\ s_b \\ s_c \end{pmatrix}, \tag{5.11}$$

where

$v_{g,h}$ are the g and h co-ordinates of the output voltage vector;

E is the mean of all the capacitor voltages, which normalizes the voltage vectors and the switching states to the same scale;

$e_{a,b,c}$ are the mean capacitor voltages in each phase and

$s_{a,b,c}$ are the switching states of each phase leg.

The mean capacitor voltages in (5.11) act as weighting factors for the contribution of each phase to the position of the output voltage vector. For the special case where $e_a = e_b = e_c$, the diagonal matrix of capacitor voltages is a simple gain so (5.11) is a generalization of (4.4).

Figure 5.18 demonstrates the effect of (5.11) by showing the voltage vectors produced by the first-sector states of a 7-level converter when the capacitor voltages in each phase are different. The states that are normally considered to be redundant do not produce identical voltage vectors because of the differences between e_a, e_b and e_c.

Fortunately, there is no need to consider all of the states in Figure 5.18 because many of the redundant states are not used by the space-vector modulation algorithm. It was discussed in Chapter 4, and again in section 5.2.1, that of all the redundant switching states available to produce a given vector, only the mean state, or states close to the mean state, are used. The voltage vectors produced by applying (5.11) to the mean states are shown in Figure 5.18 as $\times$. These voltage vectors form the lattice points of a new grid (Figure 5.19), which is the basis of a co-ordinate transformation between the demanded and actual converter output.

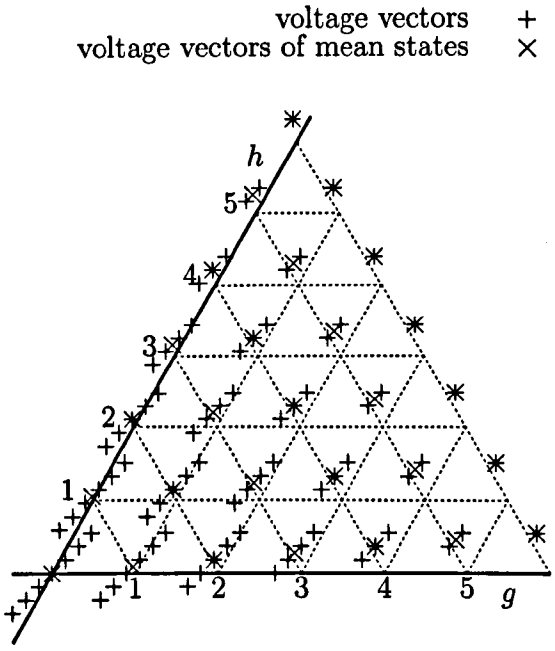


Figure 5.18: Voltage vectors on the (g, h) plane when $e_a = 0.89$, $e_b = 0.96$ and $e_c = 1.14$

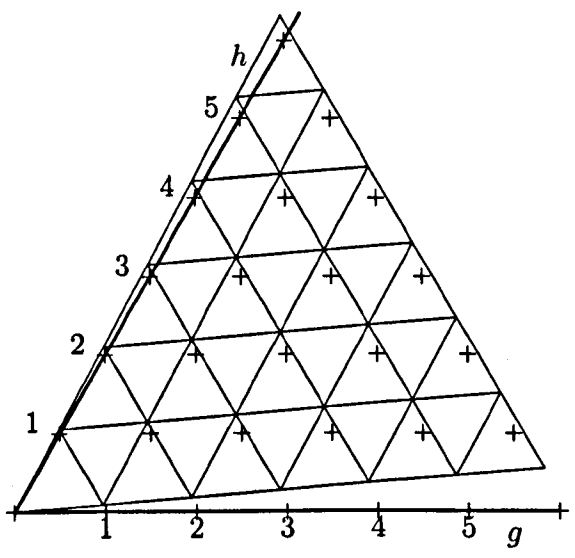


Figure 5.19: Spacial distortion of the (g, h) plane when $e_a = 0.89$, $e_b = 0.96$ and $e_c = 1.14$

Co-ordinate Transformation

The relationship between a given switching vector and the mean redundant state that produces that vector is given below:

$$\begin{pmatrix} \bar{s}_a \\ \bar{s}_b \\ \bar{s}_c \end{pmatrix} = \frac{1}{2} \begin{cases} \begin{pmatrix} 1 & 1 \\ -1 & 1 \\ -1 & -1 \end{pmatrix} \begin{pmatrix} s_g \\ s_h \end{pmatrix} & \text{in sectors 1 and 4,} \\ \begin{pmatrix} 2 & 1 \\ 0 & 1 \\ 0 & -1 \end{pmatrix} \begin{pmatrix} s_g \\ s_h \end{pmatrix} & \text{in sectors 2 and 5,} \\ \begin{pmatrix} 1 & 0 \\ -1 & 0 \\ -1 & -2 \end{pmatrix} \begin{pmatrix} s_g \\ s_h \end{pmatrix} & \text{in sectors 3 and 6.} \end{cases} \tag{5.12}$$

The relationship for the first sector was derived in Chapter 4 (equation (4.8) on page 87) and the derivation for the other sectors follows a similar procedure. When (5.12) is substituted into (5.11), three transformations are produced describing the positions of the lattice points in Figure 5.19, and for the other sectors, in terms of the switching vectors producing them.

$$\begin{pmatrix} \bar{v}_g \\ \bar{v}_h \end{pmatrix} = \frac{1}{2E} \begin{cases} \begin{pmatrix} e_a + e_b & e_a - e_b \\ e_c - e_b & e_b + e_c \end{pmatrix} \begin{pmatrix} s_g \\ s_h \end{pmatrix} & \text{in sectors 1 and 4,} \\ \begin{pmatrix} 2e_a & e_a - e_b \\ 0 & e_b + e_c \end{pmatrix} \begin{pmatrix} s_g \\ s_h \end{pmatrix} & \text{in sectors 2 and 5,} \\ \begin{pmatrix} e_a + e_b & 0 \\ e_c - e_b & 2e_c \end{pmatrix} \begin{pmatrix} s_g \\ s_h \end{pmatrix} & \text{in sectors 3 and 6.} \end{cases} \tag{5.13}$$

In (5.13) $\bar{v}_g$ and $\bar{v}_h$ are the components of the voltage vectors produced by the mean states with co-ordinates s_g and s_h.

When the time average over a sampling period is applied in order to syn-

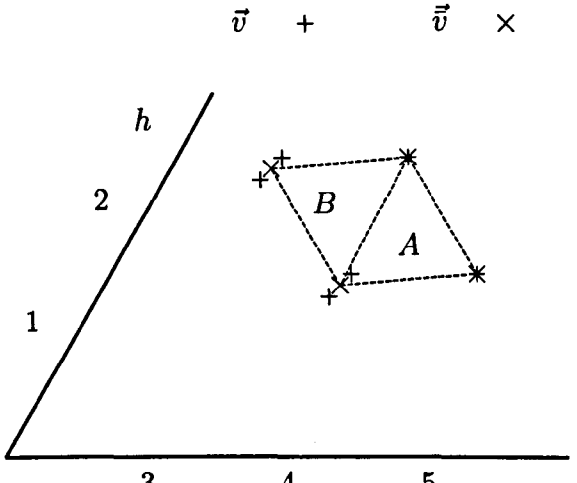


Figure 5.20: Output voltage vectors and mean output vectors for two triangles

thesize a reference vector, an approximate relationship is derived between the continuous, time-averaged switching vector, $\langle\vec{s}\rangle$, and the continuous, time-averaged voltage vector, $\langle\vec{v}\rangle$. Note that the time-averaged switching vector is the same as the modulator reference, $\vec{s}^*$.

$$\begin{pmatrix}\langle v_g\rangle\\ \langle v_h\rangle\end{pmatrix} \approx \frac{1}{2E}\begin{cases}\begin{pmatrix}e_a+e_b & e_a-e_b\\ e_c-e_b & e_b+e_c\end{pmatrix}\begin{pmatrix}s_g^*\\ s_h^*\end{pmatrix} & \text{in sectors 1 and 4,}\\ \begin{pmatrix}2e_a & e_a-e_b\\ 0 & e_b+e_c\end{pmatrix}\begin{pmatrix}s_g^*\\ s_h^*\end{pmatrix} & \text{in sectors 2 and 5,}\\ \begin{pmatrix}e_a+e_b & 0\\ e_c-e_b & 2e_c\end{pmatrix}\begin{pmatrix}s_g^*\\ s_h^*\end{pmatrix} & \text{in sectors 3 and 6.}\end{cases} \tag{5.14}$$

The validity of this approximation depends on the two kinds of triangle in the space-vector diagram. For triangles equivalent to triangle A in Figure 5.20, that is triangles containing only one vector of even redundancy, (5.14) is a good approximation if the capacitor voltage does not change significantly during the sampling period. The two vectors with odd redundancy are described exactly by (5.13) and the vectors of even redundancy are applied for equal time periods, producing the same time-averaged voltage vector as if the mean state were applied.

For triangles with two vectors of even redundancy, such as triangle B in Figure 5.20, the same arguments apply to the vector of odd redundancy and the vector of even redundancy used as a starting and ending vector. A small error is introduced by the second vector of even redundancy, as only one redundant state is used. The voltage vector produced by this single state is slightly different from that of the mean state. Hence (5.14) is an approximation to the effect of capacitor voltage ripple.

The validity of (5.14) can be explored further with reference to some simulated converter voltages. The circuit configuration shown in Figure 5.21a is for inverting mode with the H-bridges supplied by single-phase rectifiers. The rectifiers are attached in the same phase rotation as the output voltages and the modulation is synchronized to the supply. The resulting capacitor voltage ripple is balanced between the phases (similar to the capacitor voltages in Figure 5.17) so the distorted phase voltages continue to form a three-phase set (Figure 5.21b).

The reference vectors used to produce the waveforms in Figure 5.21 are compared to the average output voltage vectors during each sampling period in Figure 5.22. The vectors produced by calculating (5.14) using the reference vectors and samples of the mean capacitor voltages are also shown. Figure 5.22 shows that the average voltage vectors deviate from the circular path of the reference vectors and that (5.14) is a good model of this deviation. Also, because the phase voltages in Figure 5.21 continue to form a three-phase set, the deviation from the reference vectors is the same in each sector.

5.2.3 Theoretical Effect of Ripple on the Line Voltage Spectrum

In this section, the effect of ripple on the line-voltage spectrum is analysed in terms of the spacial distortion of the space-vector diagram that was derived above. The analysis is based on the (g,h) co-ordinates of the voltage vectors because, as derived in Chapter 4, the g and h co-ordinates are normalized versions of the $a-b$ and $b-c$ line voltages, respectively. Also, because (5.14) already includes the time-averaging of states in a sampling period, only the

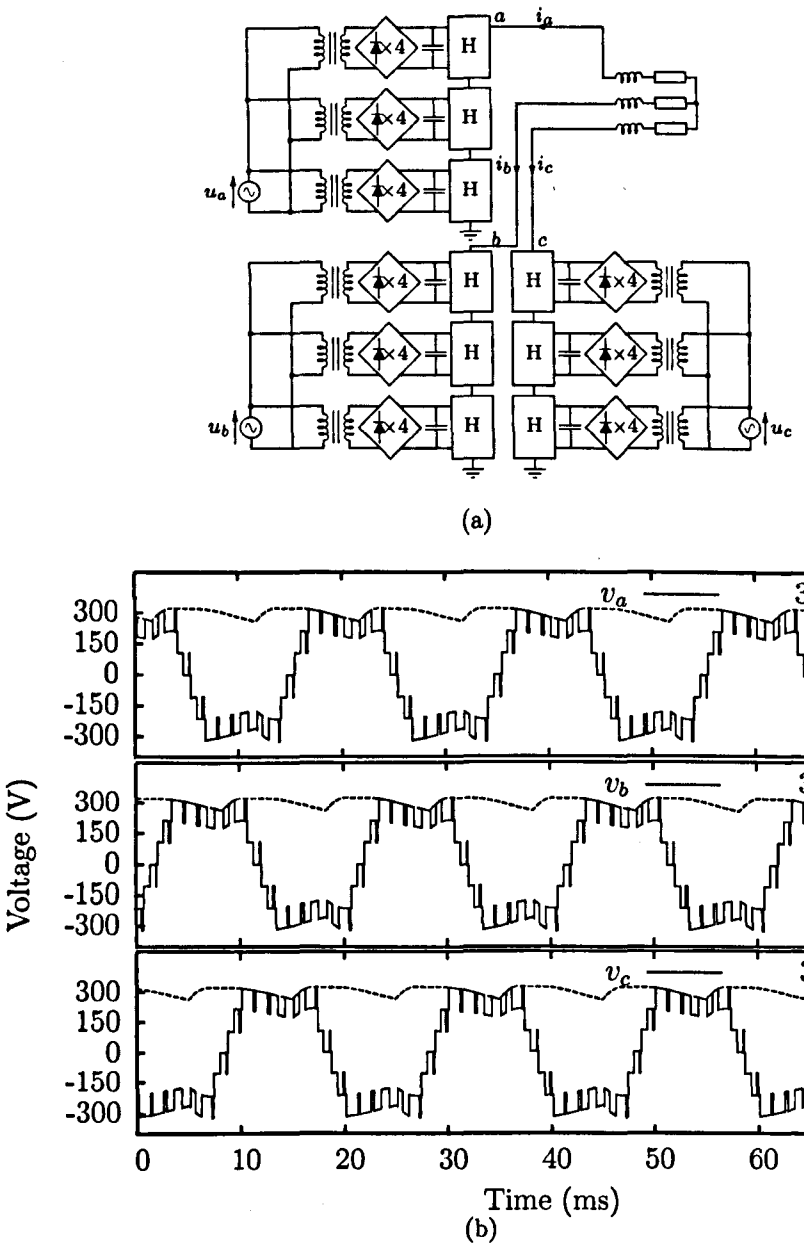


Figure 5.21: Inverting simulations. (a) Circuit configuration (b) Waveforms

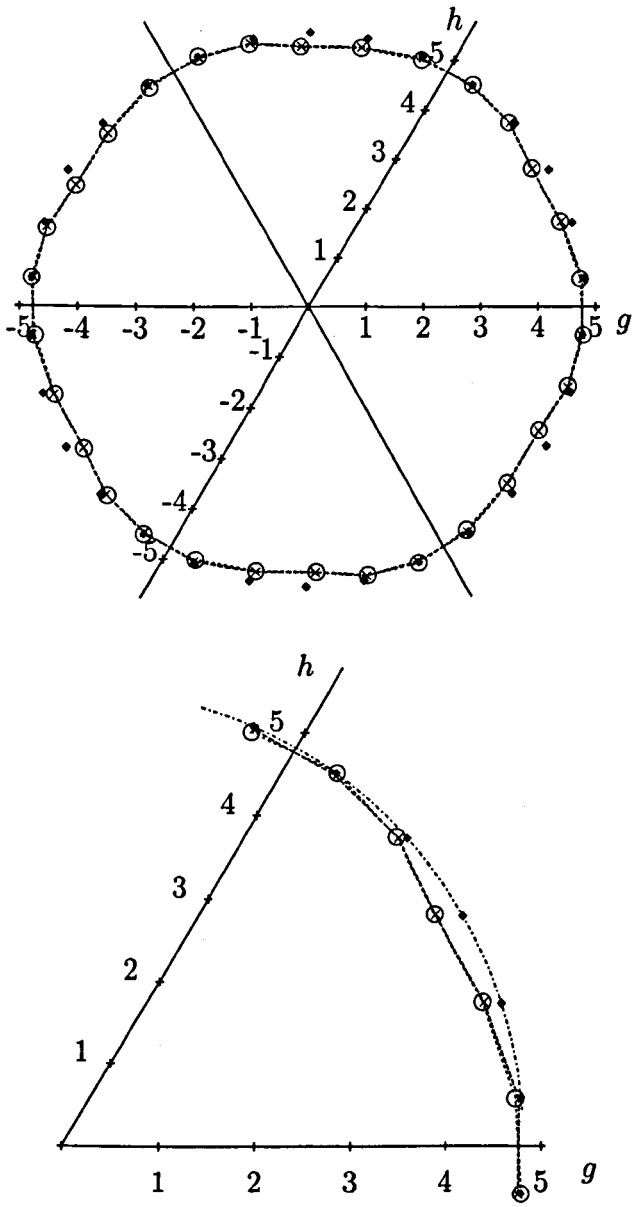


Figure 5.22: Distortion of voltage vectors due to capacitor voltage ripple

fundamental component of the reference is considered. This is a legitimate simplification because the interaction between the fundamental and the ripple has greatest effect on the low-order harmonics, which are of most concern.

The averaged, normalized line voltage $\langle v_g \rangle$, expressed in terms of its Fourier series is given by (5.15).

$$\langle v_g \rangle = \frac{1}{2\pi} \sum_{n=-\infty}^{\infty} V_n e^{jn\theta} \tag{5.15}$$

where the Fourier coefficients, V_n are given by

$$V_n = \int_{-\pi}^{\pi} \langle v_g \rangle e^{-jn\theta} \mathrm{d}\theta.$$

Considering only the fundamental component of the reference, as justified above, gives the following relationships:

$$\begin{array}{lll} s_a^* = \hat{s}\cos(\theta) & s_b^* = \hat{s}\cos(\theta - \frac{2\pi}{3}) & s_c^* = \hat{s}\cos(\theta + \frac{2\pi}{3}) \\ \Rightarrow s_g^* = \sqrt{3}\hat{s}\cos(\theta + \frac{\pi}{6}) & s_h^* = \sqrt{3}\hat{s}\cos(\theta - \frac{\pi}{2}) & \end{array}$$

In complex exponential form, the reference is

$$s_g^* = \frac{\sqrt{3}}{2}\hat{s} \sum_{m=\pm 1} e^{jm(\theta + \frac{\pi}{6})}, \qquad s_h^* = \frac{\sqrt{3}}{2}\hat{s} \sum_{m=\pm 1} e^{jm(\theta - \frac{\pi}{2})}. \tag{5.16}$$

The reference can be subjected to arbitrary capacitor voltage ripple, defined in terms of its Fourier series. The ripple in this case is assumed to form a three-phase set at twice the fundamental frequency, which is consistent with

the capacitor voltages in Figure 5.21.

$$\begin{aligned} e_a &= \sum_{n=-\infty}^{\infty} C_n e^{jn\theta} \\ e_b &= \sum_{n=-\infty}^{\infty} C_n e^{jn(\theta-\frac{2\pi}{3})} \\ e_c &= \sum_{n=-\infty}^{\infty} C_n e^{jn(\theta+\frac{2\pi}{3})} \end{aligned} \tag{5.17}$$

The underlying assumption defining the structure of the capacitor voltage spectrum in (5.17) is that the output voltage is synchronized to any sources of ripple. The assumption is that the ripple is predominantly caused by the single-phase power pulsations inherent to the circuit topology rather than any other source of ripple imposed on the d.c. links, such as would be caused by a rectifying stage from a supply operating at a different frequency to the converter output. The method that follows could be applied to systems with a more complicated ripple on the capacitor voltage by separating capacitor voltage ripple into harmonics synchronized to the output and those synchronized to a different source.

Line Voltage in Terms of Capacitor Voltage Harmonics

The relationship between the reference vector s^* and the average voltage vector $\langle \vec{v} \rangle$ varies between sectors according to (5.14). In the first and fourth sectors

$$\langle v_g \rangle|_{\sigma\in\{1,4\}} = \frac{1}{2}(e_a + e_b)s_g^* + \frac{1}{2}(e_a - e_b)s_h^*,$$

where σ denotes the sector number. Substituting for the ripple (5.17) and the reference (5.16) gives

$$\begin{aligned} \langle v_g \rangle|_{\sigma\in\{1,4\}} = \frac{\sqrt{3}\hat{s}}{4} \Bigg(& \sum_{n=-\infty}^{\infty} C_n e^{jn\theta}(1 + e^{-jn\frac{2\pi}{3}}) \sum_{m=\pm 1} e^{jm\theta} e^{jm\frac{\pi}{6}} \\ & + \sum_{n=-\infty}^{\infty} C_n e^{jn\theta}(1 - e^{-jn\frac{2\pi}{3}}) \sum_{m=\pm 1} e^{jm\theta} e^{-jm\frac{\pi}{2}} \Bigg), \end{aligned}$$

which simplifies to give

$$\langle v_g \rangle|_{\sigma\in\{1,4\}} = \frac{\sqrt{3}\hat{s}}{4} \sum_{n=-\infty}^{\infty} \sum_{m=\pm 1} C_n e^{j(n+m)\theta} \left(e^{jm\frac{\pi}{6}}(1+e^{-jn\frac{2\pi}{3}}) + e^{-jm\frac{\pi}{2}}(1-e^{-jn\frac{2\pi}{3}}) \right).$$

Applying the same procedure in the other sectors produces expressions of a similar form, allowing the line voltage to be expressed as

$$\langle v_g \rangle = \frac{\sqrt{3}}{4}\hat{s} \sum_{n=-\infty}^{\infty} \sum_{m=\pm 1} C_n e^{j(n+m)\theta} Z(\theta), \tag{5.18}$$

where

$$Z(\theta) = \begin{cases} e^{jm\frac{\pi}{6}}(1+e^{-jn\frac{2\pi}{3}}) + e^{-jm\frac{\pi}{2}}(1-e^{-jn\frac{2\pi}{3}}) & \text{in sectors 1 and 4,} \\ 2e^{jm\frac{\pi}{6}} + e^{-jm\frac{\pi}{2}}(1-e^{-jn\frac{2\pi}{3}}) & \text{in sectors 2 and 5,} \\ e^{jm\frac{\pi}{6}}(1+e^{-jn\frac{2\pi}{3}}) & \text{in sectors 3 and 6.} \end{cases}$$

Calculating the Fourier Integral

The harmonic series of the line voltage (5.15) can now be written as

$$\langle v_g \rangle = \frac{\sqrt{3}\hat{s}}{8\pi} \sum_{k=-\infty}^{\infty} \sum_{n=-\infty}^{\infty} \sum_{m=\pm 1} e^{jk\theta} \int_0^{2\pi} Z(\theta) e^{j(n+m-k)\theta} \mathrm{d}\theta. \tag{5.19}$$

The evaluation of the integral in (5.19) (henceforth designated I) depends on whether or not $k = n + m$. In both cases $Z(\theta)$ is constant within each sector so the integral can be evaluated sector-by-sector in a piece-wise fashion.

Firstly, when $k = n + m$:

$$\begin{aligned} I|_{k=n+m} &= \int_0^{2\pi} Z(\theta)\mathrm{d}\theta = \sum_{\sigma=1}^{6} Z_\sigma \int_{(\sigma-1)\frac{\pi}{3}}^{\sigma\frac{\pi}{3}} \mathrm{d}\theta \\ &= \frac{\pi}{3}\sum_{\sigma=1}^{6} Z_\sigma \\ &= \frac{4\pi}{3}\left(e^{jm\frac{\pi}{6}}(2 + e^{-jn\frac{2\pi}{3}}) + e^{-jm\frac{\pi}{2}}(1 - e^{-jn\frac{2\pi}{3}})\right) \end{aligned}$$

Where Z_σ is the value of $Z(\theta)$ in the σ^{th} sector.

Because, in this case, $n = m - k$,

$$\begin{aligned} I|_{k=n+m} &= \frac{4\pi}{3}\left(e^{jm\frac{\pi}{6}}(2 + e^{-j(m-k)\frac{2\pi}{3}}) + e^{-jm\frac{\pi}{2}}(1 - e^{-j(m-k)\frac{2\pi}{3}})\right) \\ &= \frac{4\pi}{3}\left([2e^{jm\frac{\pi}{6}} + e^{-jm\frac{\pi}{2}}] + [e^{jm\frac{5\pi}{6}} - e^{jm\frac{\pi}{6}}]e^{-jk\frac{2\pi}{3}}\right). \end{aligned}$$

As $m \in \pm 1$

$$I|_{k=n+m} = \frac{4\pi}{3}\sqrt{3}\left(1 - e^{-jk\frac{2\pi}{3}}\right). \tag{5.20}$$

The integral in (5.19) also needs to be evaluated for the remaining conditions, that is when $k \neq n + m$:

$$\begin{aligned} I|_{k\neq n+m} &= \sum_{\sigma=1}^{6} Z_\sigma \int_{(\sigma-1)\frac{\pi}{3}}^{\sigma\frac{\pi}{3}} e^{j(n+m-k)\theta}\mathrm{d}\theta \\ &= \frac{1}{j(n+m-k)}\sum_{\sigma=1}^{6} Z_\sigma \left[e^{j(n+m-k)\theta}\right]_{(\sigma-1)\frac{\pi}{3}}^{\sigma\frac{\pi}{3}} \end{aligned}$$

Z takes the same value in opposite sectors:

$$\begin{aligned} I|_{k\neq n+m} &= \tfrac{1+(-1)^{n+m-k}}{j(n+m-k)} \sum_{\sigma=1}^{3} Z_\sigma \left[e^{j(n+m-k)\theta}\right]_{(\sigma-1)\frac{\pi}{3}}^{\sigma\frac{\pi}{3}} \\ &= \tfrac{1+(-1)^{n+m-k}}{j(n+m-k)}\left(1-e^{-jn\frac{2\pi}{3}}\right) \\ &\left(e^{jm\frac{\pi}{6}}\left(e^{j(n+m-k)\frac{2\pi}{3}} - e^{j(n+m-k)\frac{\pi}{3}}\right)\right. \\ &\qquad \left. + e^{-jm\frac{\pi}{2}}\left(e^{j(n+m-k)\frac{2\pi}{3}} - 1\right)\right) \end{aligned}$$

Further simplification can be achieved by grouping the m terms in the exponential and using the fact that $m = \pm 1$.

$$I|_{k\neq n+m} = \tfrac{1+(-1)^{n+m-k}}{n+m-k}\left(1-e^{-jn\frac{2\pi}{3}}\right)m\left(e^{j(n-k)\frac{2\pi}{3}} - e^{j(n-k)\frac{\pi}{3}} + 1\right) \qquad (5.21)$$

The complete expression for the Fourier series of $\langle v_g \rangle$ is produced by substituting (5.20) and (5.21) into (5.19).

$$\begin{aligned} \langle v_g \rangle = \frac{\hat{s}}{2} \sum_{k=-\infty}^{\infty} \sum_{m=\pm 1} C_{k-m} \left(1 - e^{-jk\frac{2\pi}{3}}\right) e^{jk\theta} \\ + \frac{\sqrt{3}\hat{s}}{8\pi} \sum_{k=-\infty}^{\infty} \sum_{m=\pm 1} \sum_{\substack{n=-\infty \\ n\neq k-m}}^{\infty} \frac{C_n(1+(-1)^{n+m-k})}{n+m-k} \left(1 - e^{-jn\frac{2\pi}{3}}\right) \\ \left[m\left(e^{j(n-k)\frac{2\pi}{3}} - e^{j(n-k)\frac{\pi}{3}} + 1\right)\right] e^{jk\theta} \end{aligned} \qquad (5.22)$$

Simplified Expression

Equation (5.22) can be simplified in order to consider only the non-zero harmonics of the line voltages. To simplify (5.22) it is useful to assign a symbol

to one of the complex terms. Hence

$$\langle v_g \rangle = \frac{\hat{s}}{2} \sum_{k=-\infty}^{\infty} \sum_{m=\pm 1} C_{k-m} \left(1 - e^{jk\frac{2\pi}{3}}\right) e^{jk\theta} + \frac{\sqrt{3}\hat{s}}{8\pi} \sum_{k=-\infty}^{\infty} \sum_{m=\pm 1} \sum_{\substack{n=-\infty \\ n \neq k-m}}^{\infty} \frac{C_n(1+(-1)^{n+m-k})}{n+m-k} \left(1 - e^{-jn\frac{2\pi}{3}}\right) m\Psi e^{jk\theta} \quad (5.23a)$$

where

$$\Psi = e^{j(n-k)\frac{2\pi}{3}} - e^{j(n-k)\frac{\pi}{3}} + 1. \quad (5.23b)$$

The following simplification of (5.22) is based on two key assumptions:

1. Even and third-order harmonics of the line voltage have zero magnitude. This is proven in Appendix A, but is also intuitive from observation that the phase voltages in Figure 5.21 have half-wave symmetry and form a three-phase set. This assumption can be expressed mathematically as follows:

$$k \in \{6l \pm 1 | l \in \mathbb{Z}\}. \quad (5.24)$$

2. The capacitor voltages only contain even harmonics of the line voltage frequency.

The combined effect of these assumptions is that only odd values of $(n-k)$ are relevant to the evaluation of Ψ. The values of Ψ are plotted in Figure 5.23 for values of $(n-k)$ between ± 15. The odd values of $(n-k)$ for which Ψ is non-zero are highlighted in Figure 5.23 and given by the following expressions:

$$\begin{aligned} & n-k \in \{\ldots -9, -3, 3, 9 \ldots\} \\ \Rightarrow & (n-k) \in \{6r+3 | r \in \mathbb{Z}\} \end{aligned} \quad (5.25)$$

Hence substituting (5.24) into (5.25):

$$n \in \{6(r+l)+3 \pm 1\} \quad (5.26)$$

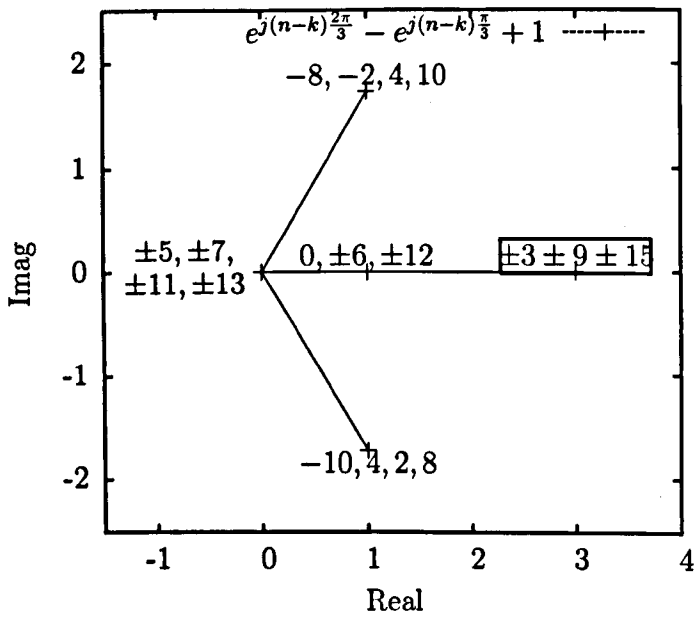


Figure 5.23: Complex values of Ψ for $(n-k)$ in the range $[-15:15]$. Labels indicate values of $(n-k)$ at each point.

Table 5.2 summarizes the simplification of the terms of (5.22) applicable for values of k and n for which (5.22) is non-zero. Combining each of these simplifications, the non-zero Fourier coefficients of the line voltage waveform can be written as follows:

$$V_{6l\pm1} = \sqrt{3}\frac{\hat{s}}{2}e^{\pm j\frac{\pi}{6}}(C_{6l} + C_{6l\pm2}) + \frac{9v}{8\pi}e^{\pm j\frac{\pi}{6}}\sum_{m=\pm1}\sum_{r=-\infty}^{\infty}\frac{2mC_{6(r+l)+3\pm1}}{6r+3+m}$$

Expanding the summation with respect to m gives the final, simplified expression.

$$V_{6l\pm1} = \sqrt{3}\frac{\hat{s}}{2}e^{\pm j\frac{\pi}{6}}(C_{6l} + C_{6l\pm2}) - \frac{9v}{8\pi}e^{\pm j\frac{\pi}{6}}\sum_{r=-\infty}^{\infty}\frac{C_{6(r+l)+3\pm1}}{(3r+1)(3r+2)} \qquad (5.27)$$

Equation (5.27) indicates the harmonics of the line voltage that are produced by the interaction of the fundamental component of the reference and

Term	Simplification
$1 - e^{jk\frac{2\pi}{3}}$	$3e^{\pm j\frac{\pi}{6}}$
$1 + (-1)^{n+m-k}$	2
$1 - e^{-jn\frac{2\pi}{3}}$	$\sqrt{3}e^{\pm j\frac{\pi}{6}}$
Ψ	3

Table 5.2: Simplification of terms from (5.22) for values of k given in (5.24) and n given in (5.26).

the capacitor voltage ripple. The first term represents the sum and difference frequency components that are usual when two sinusoidal quantities are multiplied. When $l = 0$ the first term indicates that there is a component of the output voltage proportional to the reference magnitude and to the d.c. component of the capacitor voltage; this is the point of the modulation and is the only component that appears when the capacitor voltages are constant. The $C_{6l\pm2}$ term indicates that the fundamental output voltage is also influenced by the second harmonic of the capacitor voltage.

The second term of (5.27) is of particular interest because it indicates that more harmonic components are produced than the straightforward sum and difference frequencies described by the first term. Key parts of the second term are the index to the capacitor voltages

$$6(r + l) + 3 \pm 1$$

and the quadratic denominator

$$(3r + 1)(3r + 2).$$

Table 5.3 gives the values of l for each line-voltage harmonic and the capacitor voltage harmonics that are indexed by a range of r. The capacitor voltage harmonics indexed when r is -1 or 0 are most important because, as shown in Figure 5.24, these components are attenuated least by the quadratic denominator. In particular, the second capacitor-voltage harmonic influences the fifth line-voltage harmonic and the fourth capacitor-voltage harmonic influences the

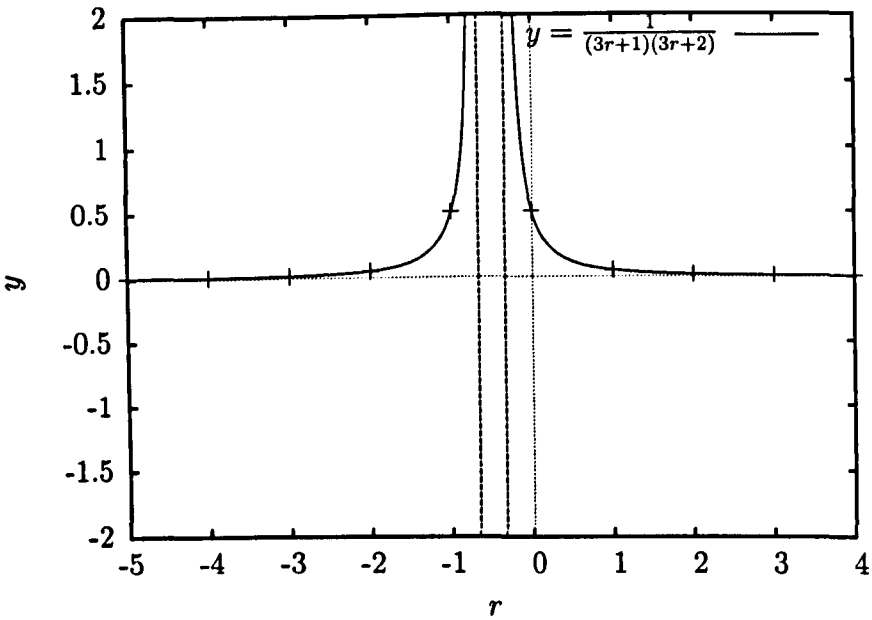


Figure 5.24: Value of the quadratic denominator in equation (5.27) against r

seventh line-voltage harmonic with $r = -1$. Other line-voltage harmonics are affected less because the contributions of the second and fourth capacitor voltages are attenuated more and because other capacitor-voltage harmonics are lower in magnitude. Hence the second term in (5.27) has most influence on the fifth and seventh line-voltage harmonics.

5.2.4 Measured Effect of Ripple

The theoretical influence of the capacitor voltage ripple will now be compared with simulation and experimental results using the inverting structure shown in Figure 5.21a. The modulation is operated in *open-loop* so that the measured harmonics are not influenced by the controller action. In order for the assumptions regarding capacitor voltage to be valid, that is that the capacitor voltages only contain even harmonics, the output frequency is synchronized to the supply frequency in the same way as for the rectifying configuration.

For the first simulation, the converter is operated with high switching frequency because the harmonic analysis in section 5.2.3 is based on averaging so

		$6(l+r)+3\pm1$			
k	l	$r=-2$	-1	0	1
1	0	-8	-2	4	10
5	1	-4	2	8	14
7	1	-2	4	10	16
11	2	2	8	14	20
13	2	4	10	16	22

Table 5.3: Index of which capacitor-voltage harmonics influence the line-voltage spectrum for a range of values of l and r according to (5.27).

is most valid when the switching frequency is high. The normalized spectrum of the line voltage is compared to that of the line-to-line switching function in Figure 5.25. When the capacitor voltages are constant, the spectra of the normalized line voltage and of the switching function are identical so any significant differences between the two spectra in Figure 5.25 can be attributed to the capacitor voltage ripple.

The most significant difference between the spectra shown in Figure 5.25 are large fifth and seventh harmonics of the line voltage which are not present in the spectrum of the switching function. This is consistent with the analysis presented in section 5.2.3.

To assess the validity of (5.27), Figure 5.26 compares the fundamental, fifth and seventh harmonics of the line voltages to predictions calculated by inputting the modulation index and the spectrum of the simulated capacitor voltages into (5.27). The values have been normalized to give a fundamental magnitude of one. Figure 5.26 shows that fifth and seventh harmonics at this high switching frequency match the predictions in both magnitude and phase.

To establish whether (5.27) is valid at lower switching frequencies, the converter has been simulated for a range of modulation sampling frequency with a fixed modulation index. The magnitudes of the fundamental, fifth and seventh harmonics are compared to their calculated magnitudes in Figure 5.27, which shows that (5.27) provides a good estimate of the these harmonics. At 750Hz the seventh harmonic is reduced slightly compared to the prediction.

There are several effects that can introduce error between the prediction

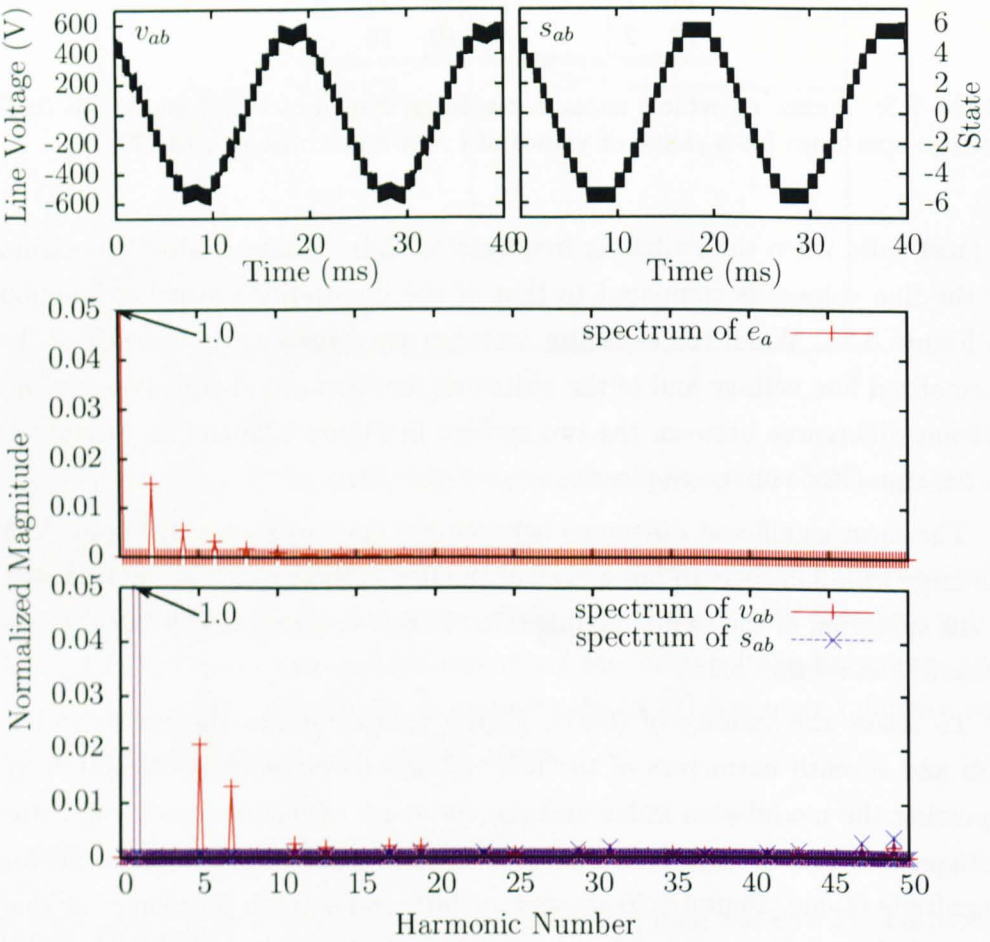


Figure 5.25: Line voltage, line switching function, capacitor voltage spectrum and comparison of line voltage and switching function spectra with sampling frequency of 5.5kHz

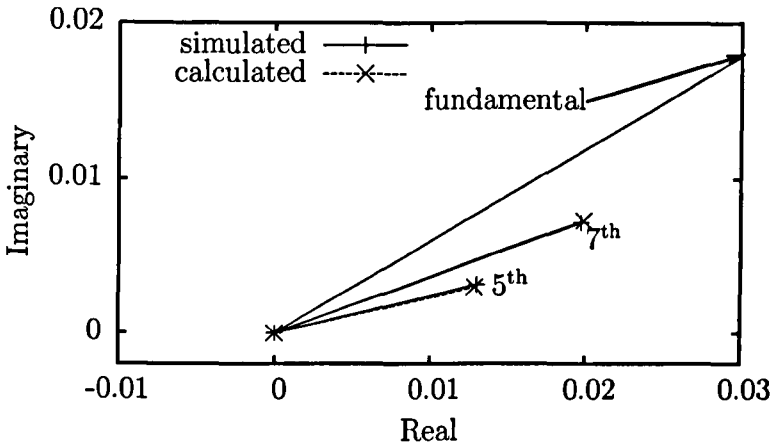


Figure 5.26: Comparison of 5^{th} and 7^{th} harmonics from simulated line voltages with calculation of (5.27) using simulated capacitor voltage spectrum

and measured results at low switching frequency. First is the fact that the harmonic analysis is based on averaging, which is less valid with lower switching frequency. Secondly, the deviation of the individual capacitor voltages from their mean is higher at low switching frequency because there is less opportunity for the balancing controller to act. Finally, sidebands of the first carrier harmonic interfere with harmonics introduced by the interaction of the fundamental and the capacitor voltage ripple.

The last set of results in this section are experimental results from the converter operating in inverting mode with the same modulation index used in Figure 5.27. Capacitor voltages, phase voltages and currents are shown in Figure 5.28 for phase a as well as the ab line voltage. The spectrum of the mean capacitor voltage is shown to consist only of even harmonics in Figure 5.29, which is consistent with the assumptions used in section 5.2.

The spectrum of the line voltage, calculated from an oscilloscope trace, is shown in Figure 5.30. Also shown is the spectrum of the switching function, which was calculated using demanded switching states and dwell times captured in the memory of the DSP while the converter was running. Comparing these two spectra shows a close match between the spectrum of the switching function and of the line voltage, except for an increased fifth harmonic of the

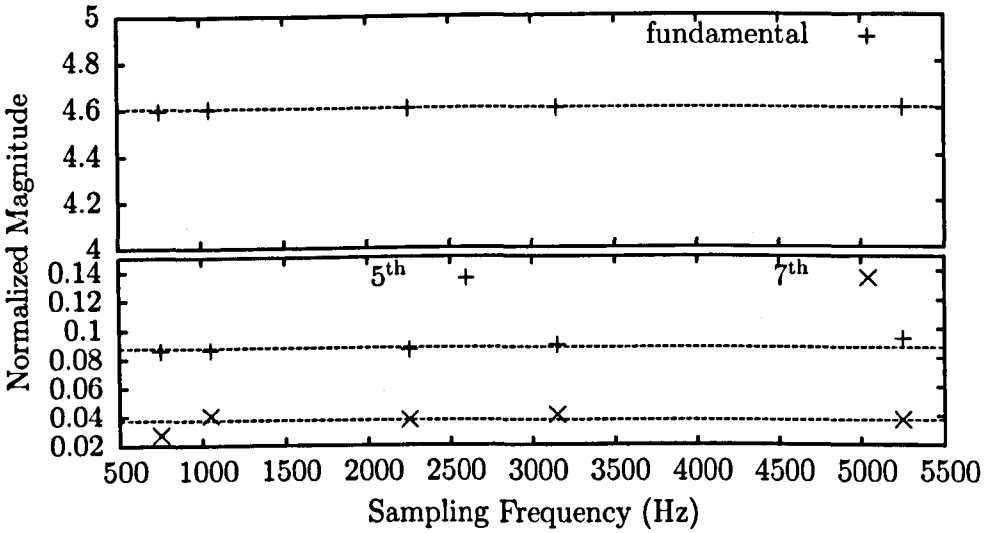


Figure 5.27: Comparison of fundamental, 5^{th} and 7^{th} harmonics of simulated converter with calculated values over a range of sampling frequency

line-voltage consistent with the analysis in section 5.2. Any increased seventh harmonic is not visible in the figure.

As for the simulated example, the fifth and seventh harmonics of the line voltages are compared to the values calculated using (5.27) in Figure 5.31. Some post-processing of the data was applied in order to align the fundamental components:

- The phase of v_{ab} was adjusted to account for a difference in timing between the DSP and the oscilloscope trigger and to account for the inherent delay of half a sampling period between the reference and output of a PWM waveform.
- The measured d.c. voltage was reduced to account for voltage drops across the switching devices.

After these adjustments there is an excellent match between the calculated and measured fundamental line voltage. The fifth and seventh harmonics were also a good match in magnitude but not as close in phase as was seen for the high-switching frequency simulation in Figure 5.26. Although the lower switching frequency appears to produce effects that are not modelled in the averaged

analysis, Figure 5.31 suggests that (5.27) is still a good approximation of the effect of capacitor voltage ripple at this switching frequency.

5.3 Feed-Forward Compensation of Capacitor Voltage Ripple

Section 5.2 showed that capacitor voltage ripple has a detrimental effect of on line voltage spectrum by increasing low-order harmonics. The effect of the ripple was modelled by a distortion in the space-vector co-ordinate system derived from the mean of the capacitor voltages in each phase leg and this model was verified through comparison of mathematical analysis, simulated and experimental results.

It follows that the line-voltage spectrum should improve if the modulator were to compensate for distortion in the space-vector diagram. This section derives a new geometrical approach to ripple compensation that alters the reference prior to modulation in order to account for the changes to the space-vector diagram. A block diagram for the modulation process including ripple compensation, space-vector modulation and balancing controllers is shown in Figure 5.32.

5.3.1 Compensation Scheme

According to (5.14) the relationship between the averaged line-voltage vector produced in a sampling period, $\langle\vec{v}\rangle$, and the reference vector, $\vec{s}^*$, in the first or fourth sector is given by

$$\begin{pmatrix}\langle v_g\rangle\\ \langle v_h\rangle\end{pmatrix} = \frac{1}{2E}\begin{pmatrix}e_a+e_b & e_a-e_b\\ e_c-e_b & e_b+e_c\end{pmatrix}\begin{pmatrix}s_g^*\\ s_h^*\end{pmatrix} \text{ if } \sigma\in\{1,4\}.$$

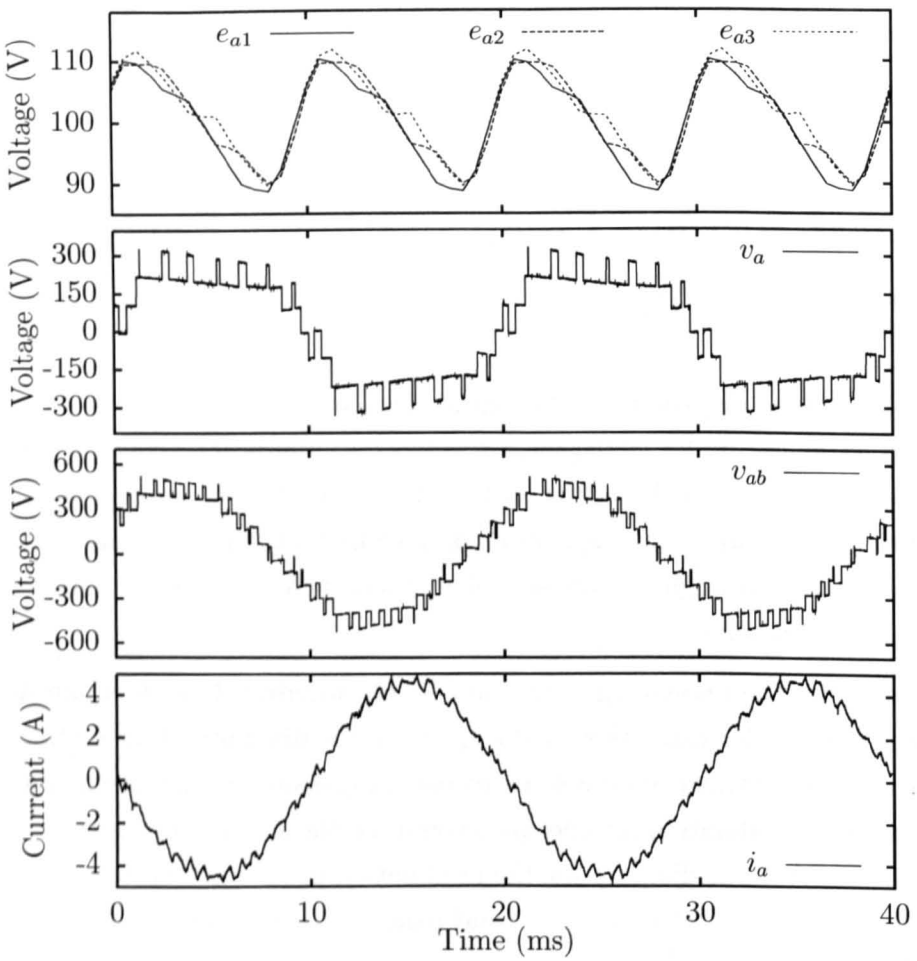


Figure 5.28: Experimental results for converter operating in open-loop inverting mode

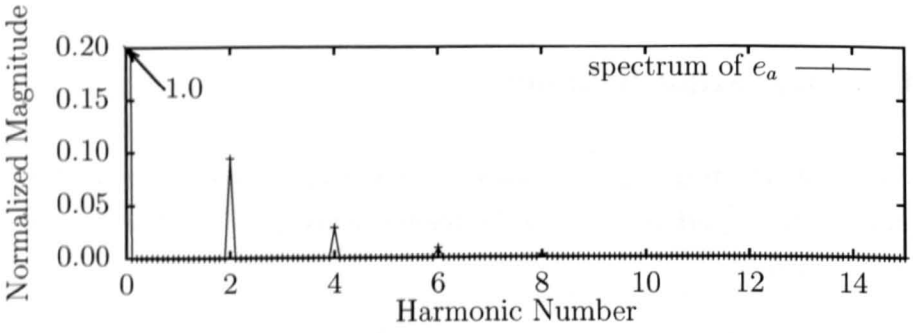


Figure 5.29: Spectrum of mean phase-a capacitor voltage

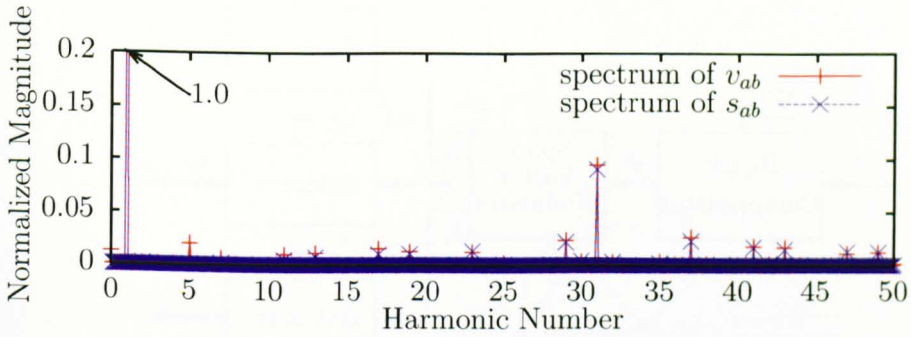


Figure 5.30: Comparison of spectra of the line voltage and switching function

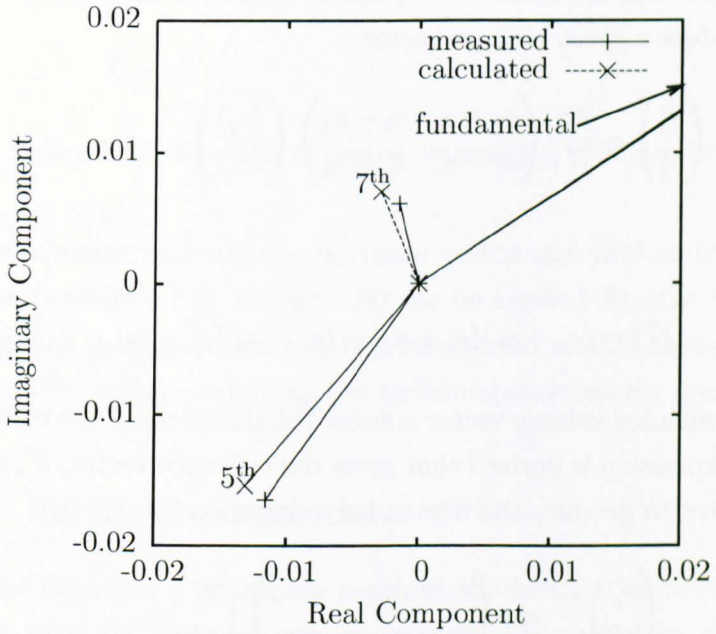


Figure 5.31: Comparison between calculated and measured fifth and seventh harmonics of line-to-line voltage

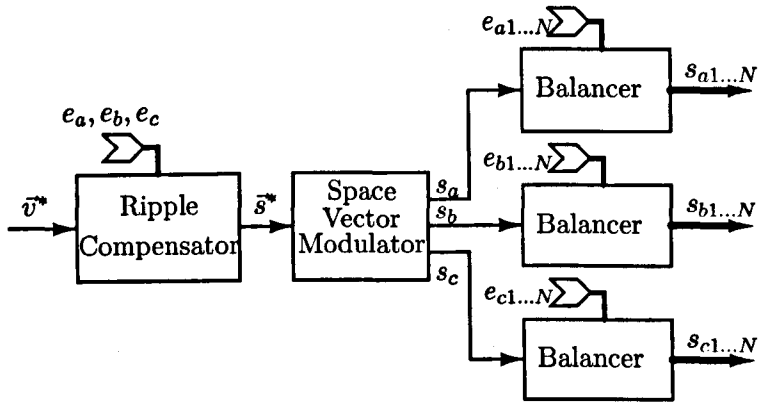


Figure 5.32: Modulation structure including ripple compensation and balancing

By inverting this transformation it is possible to derive the reference vector required to produce a given voltage vector.

$$\begin{pmatrix} s_g^* \\ s_h^* \end{pmatrix} = \frac{2E}{|T|} \begin{pmatrix} e_b + e_c & e_b - e_a \\ e_b - e_c & e_a + e_b \end{pmatrix} \begin{pmatrix} \langle v_g \rangle \\ \langle v_h \rangle \end{pmatrix},$$

where

$$|T| = (e_a + e_b)(e_b + e_c) - (e_a - e_b)(e_c - e_b).$$

Hence, if the demanded voltage vector is substituted in place of the voltage vector above, an expression is derived that gives the reference vector, $\vec{s}^*$, required for the modulator to produce the demanded voltage vector, $\vec{v}^*$.

$$\begin{pmatrix} s_g^* \\ s_h^* \end{pmatrix} = \frac{2E}{|T|} \begin{pmatrix} e_b + e_c & e_b - e_a \\ e_b - e_c & e_a + e_b \end{pmatrix} \begin{pmatrix} v_g^* \\ v_h^* \end{pmatrix}, \tag{5.28}$$

This equation is the basis of the ripple-compensation block in Figure 5.32.

Although (5.28) is only valid in the first and fourth sectors, there is no need to derive similar expressions for the other sectors because the space-

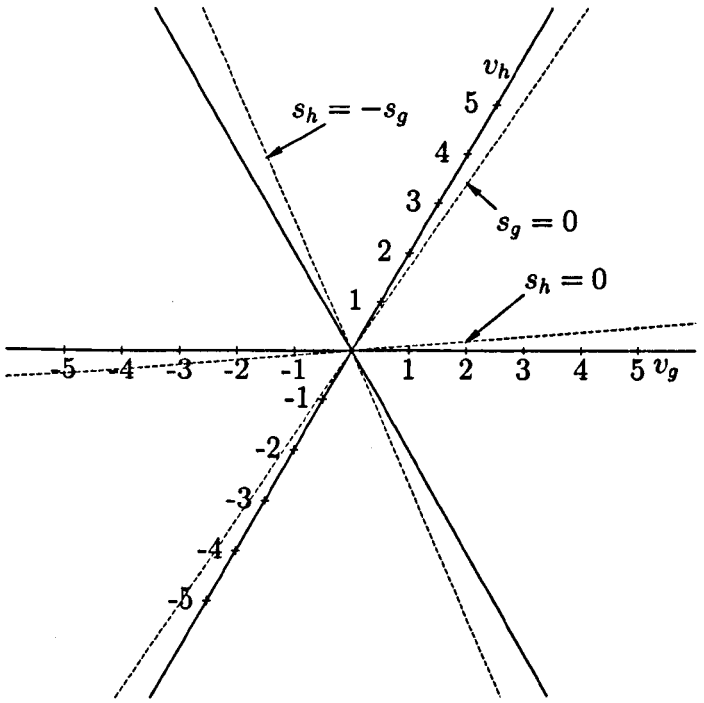


Figure 5.33: Position of sector boundaries with d.c. link ripple

vector modulator converts the reference vector into *first-sector-equivalent* coordinates (section 4.1.8) where (5.28) can be applied directly. However, before the reference voltage vector can be transformed to first-sector-equivalent coordinates, the sector containing the switching-state vector must be identified.

5.3.2 Sector Boundaries

When the capacitor voltages are constant the boundaries between the sectors occur at fixed 60° intervals and the sector is identified by the angle of the reference vector. When the capacitor voltages vary the sector boundaries of the switching states are transformed by (5.14) and do not occur at fixed angles.

As shown in Figure 5.33, the sector boundaries are defined by the following

equations:

$$s_h = 0 \qquad s_g = 0 \qquad s_h = -s_g.$$

First, consider the boundary between the sixth and first sectors, defined as $s_h = 0$. The voltage vectors produced by the mean states on this boundary can be obtained by evaluating (5.13) with $s_h = 0$.

$$\begin{pmatrix} \bar{v}_g \\ \bar{v}_h \end{pmatrix}\Big|_{s_h=0} = \frac{1}{2E}\begin{pmatrix} e_a + e_b & e_a - e_b \\ e_c - e_b & e_b + e_c \end{pmatrix}\begin{pmatrix} s_g \\ 0 \end{pmatrix}$$
$$\Rightarrow \begin{pmatrix} \bar{v}_g \\ \bar{v}_h \end{pmatrix}\Big|_{s_h=0} = \frac{s_g}{2E}\begin{pmatrix} e_a + e_b \\ e_c - e_b \end{pmatrix}.$$

When s_g is eliminated

$$\bar{v}_h = \left(\frac{e_c - e_b}{e_a + e_b}\right)\bar{v}_g \text{ if } s_h = 0. \tag{5.29}$$

Applying the same substitution in the portion of (5.13) applicable to sector six gives:

$$\begin{pmatrix} v_g \\ v_h \end{pmatrix}\Big|_{s_h=0} = \frac{1}{2E}\begin{pmatrix} e_a + e_b & 0 \\ e_c - e_b & 2e_c \end{pmatrix}\begin{pmatrix} s_g \\ 0 \end{pmatrix}$$
$$\Rightarrow \begin{pmatrix} \bar{v}_g \\ \bar{v}_h \end{pmatrix}\Big|_{s_h=0} = \frac{s_g}{2E}\begin{pmatrix} e_a + e_b \\ e_c - e_b \end{pmatrix}.$$

The same relationship is produced as (5.29), demonstrating that there is no discontinuity between the transformations at the sector boundaries.

The same procedure applied to the other sector boundaries (given by $s_g = 0$ and $s_h = -s_g$) applied to the appropriate parts of (5.13) produces the following

two equations:

$$v_g = \left(\frac{e_a - e_b}{e_b + e_c}\right) v_h \qquad \text{if } s_g = 0;$$

$$v_h = -\left(\frac{e_b + e_c}{e_a + e_b}\right) v_g \qquad \text{if } s_h = -s_g.$$

Hence the sector containing the reference vector is given by

$$\sigma = \begin{cases} 1 & \text{if } v_h \geq \left(\frac{e_c - e_b}{e_a + e_b}\right) v_g \text{ and } v_g \geq \left(\frac{e_a - e_b}{e_b + e_c}\right) v_h, \\ 2 & \text{if } v_h \geq -\left(\frac{e_b + e_c}{e_a + e_b}\right) v_g \text{ and } v_g \leq \left(\frac{e_a - e_b}{e_b + e_c}\right) v_h, \\ 3 & \text{if } v_h \leq -\left(\frac{e_b + e_c}{e_a + e_b}\right) v_g \text{ and } v_h \geq \left(\frac{e_c - e_b}{e_a + e_b}\right) v_g, \\ 4 & \text{if } v_h \leq \left(\frac{e_c - e_b}{e_a + e_b}\right) v_g \text{ and } v_g \leq \left(\frac{e_a - e_b}{e_b + e_c}\right) v_h, \\ 5 & \text{if } v_h \leq -\left(\frac{e_c + e_b}{e_a + e_b}\right) v_g \text{ and } v_g \geq \left(\frac{e_a - e_b}{e_b + e_c}\right) v_g, \\ 6 & \text{if } v_h \geq -\left(\frac{e_b + e_c}{e_a + e_b}\right) v_g \text{ and } v_h \leq \left(\frac{e_c - e_b}{e_a + e_b}\right) v_g. \end{cases} \tag{5.30}$$

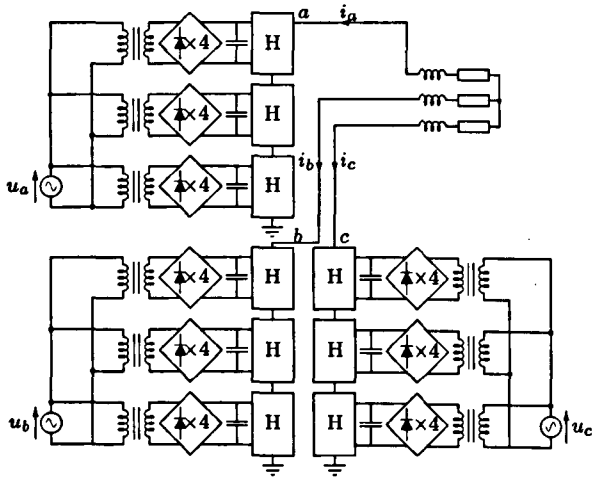
The sector can be identified from three comparisons of the co-ordinates of the demanded vector with quantities derived from capacitor voltage magnitudes.

5.3.3 Experimental Verification of Feed-forward Compensation

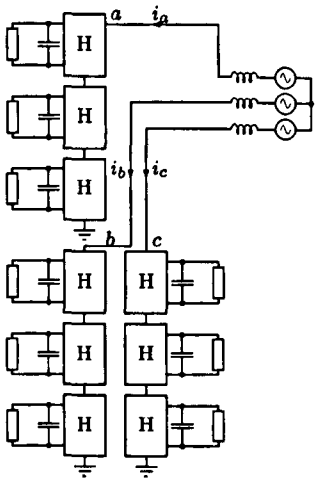
The feed-forward compensation scheme has been verified experimentally for the inverting (Figure 5.34a) and rectifying (Figure 5.34a) circuit configurations. In each case currents and voltages for compensated modulation are shown alongside results obtained at the same operating point without feed-forward compensation. The spectra of the line voltages with and without compensation are compared directly.

Figure 5.35 shows results for open-loop modulation of the experimental converter in inverting mode. The line voltage produced by uncompensated modulation contains a small fifth harmonic, which is reduced when the compensated modulation is used.

Figure 5.36 show results for closed-loop, rectifying operation. In this ex-



(a)



(b)

Figure 5.34: Circuit configurations: (a) inverting and (b) rectifying

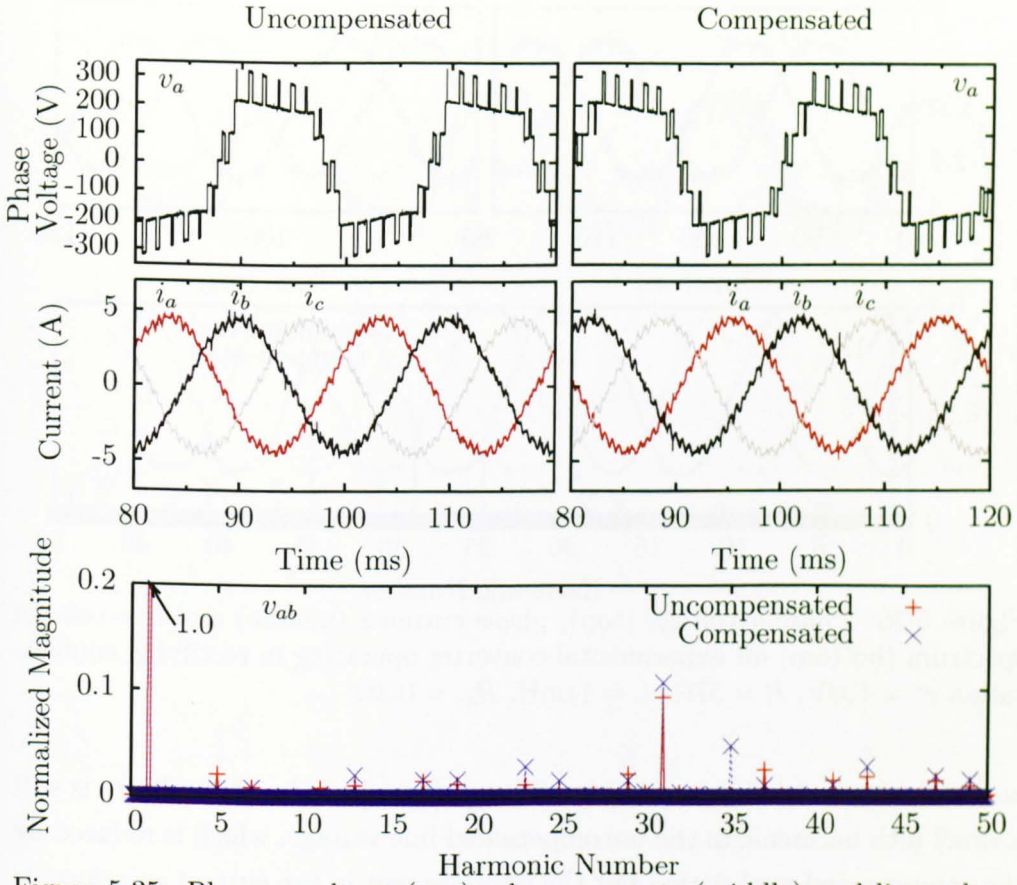


Figure 5.35: Phase-a voltage (top), phase currents (middle) and line-voltage spectrum (bottom) for the experimental converter operating in inverting configuration $e^* = 100\text{V}$, $L = 11\text{mH}$, $R_{ac} = 57\Omega$

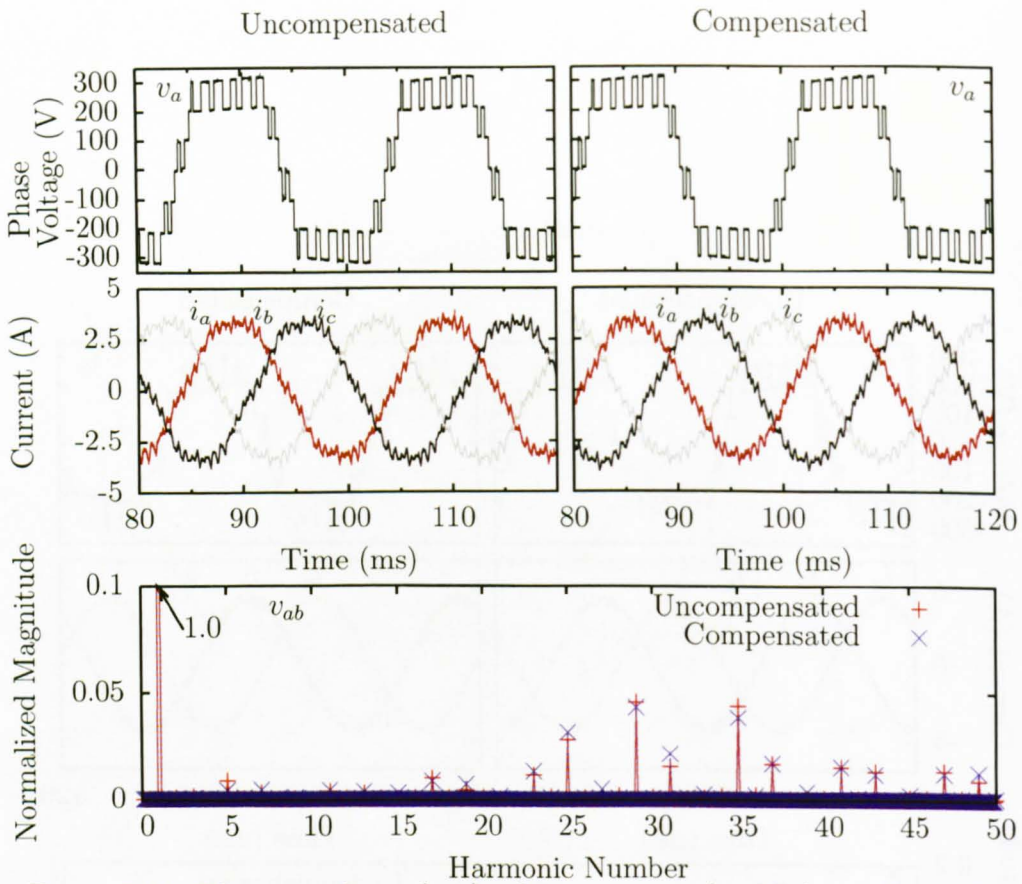


Figure 5.36: Phase-a voltage (top), phase currents (middle) and line-voltage spectrum (bottom) for experimental converter operating in rectifying configuration $e^* = 100\text{V}$, $R = 57\Omega$, $L = 11\text{mH}$, $R_{ac} = 0.3\Omega$

ample the current is low so the capacitor voltage ripple is small. There is still a small fifth harmonic in the uncompensated line voltage, which is reduced by the compensated modulation but the improvement in the current waveform is not visible.

In order to show the improvement caused by the compensation scheme more clearly, Figure 5.37 shows the converter operating under greater load and hence with more significant capacitor-voltage ripple. In order to remain within the current rating of the converter with this load, the supply voltage and capacitor voltage reference has been reduced. There is significant capacitor voltage ripple visible on the phase voltages, which causes a large fifth harmonic of the line voltages with uncompensated modulation. The fifth harmonic is

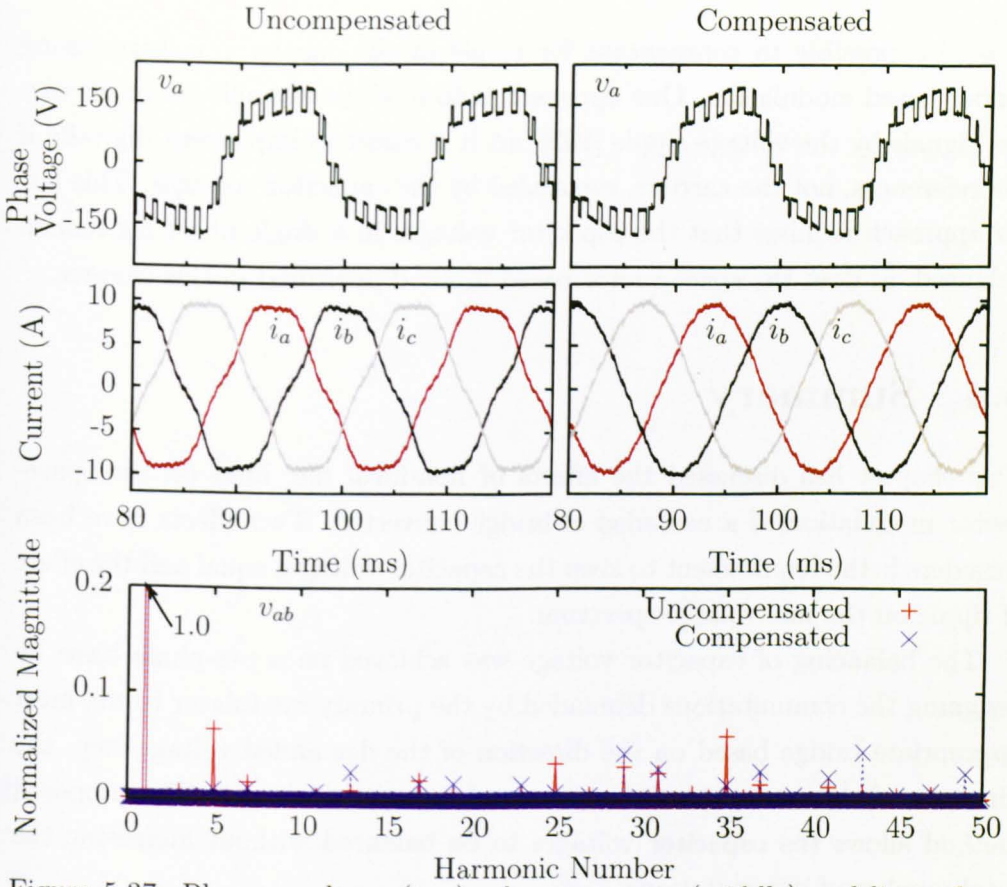


Figure 5.37: Phase-a voltage (top), phase currents (middle) and line-voltage spectrum (bottom) for experimental converter operating in rectifying configuration $e^* = 50\text{V}$, $R = 10\Omega$, $L = 11\text{mH}$, $R_{ac} = 0.3\Omega$

greatly reduced by compensated modulation and there is a visible improvement in the current waveforms.

5.3.4 Conceptual Comparison with Carrier-Based Modulation

It is also possible to compensate for ripple of the capacitor voltages using carrier-based modulation. One approach is to modulate amplitude of the carrier signals by the voltage ripple [102] but it is easier to implement digitally if the references, not the carriers, are scaled by the capacitor voltages. This latter approach requires that the capacitor voltages in a single phase leg remain balanced, as does the space-vector based method presented in this chapter.

5.4 Summary

This chapter has discussed the effects of non-ideal d.c. links on the space-vector modulation of a cascaded H-bridge converter. Two effects have been considered: the requirement to keep the capacitor voltages equal and the effect of ripple on the line-voltage spectrum.

The balancing of capacitor voltage was achieved on a per-phase basis by assigning the commutations demanded by the primary modulator to the most appropriate bridge based on the direction of the demanded voltage step, the direction of the current and the measured capacitor voltages. The proposed method allows the capacitor voltages to be balanced without increasing the total number of commutations.

The limitations of the capacitor balancing algorithm have been investigated for real power flow in terms that are applicable to any balancing method. It has been shown that operating points with lower modulation index allow greater flexibility over the loading of each bridge.

The effect of capacitor-voltage ripple on the line-voltage spectrum has also been investigated. Under conditions where the ripple is synchronized to the output, such as grid-connected applications where there is only one supply frequency, it has been shown that the second and fourth harmonics of the

capacitor voltage increase the fifth and seventh harmonics of the line voltage respectively. A compensation scheme has been developed which transforms the reference signal prior to modulation so that the desired reference is produced despite capacitor voltage ripple. This method has been shown to be effective at reducing the magnitude of the unwanted fifth harmonic.

Chapter 6

One-Dimensional Modulation

One-dimensional modulation is a single-phase modulation technique that synthesises an output voltage reference using selected switching states. This modulation method has been described extensively for two-cell converters [68], [103], [104] and has been shown to be capable of compensating for changing capacitor voltages [69] and of maintaining a specific ratio of capacitor voltages [105].

This chapter begins by describing the published implementation of one-dimensional modulation for a two-cell converter. In particular, it is shown that one dimensional modulation is closely related to regularly sampled, level-shifted carrier modulation and that these methods can be made to produce identical a.c. waveforms when the capacitor voltages are balanced.

Once the one-dimensional modulation scheme has been described for two-cell converters, section 6.2.2 describes the implementation of the same modulation method for a three-cell converter. Simplifications are introduced, taking advantage of symmetries of the states, so that the increased number of states does not make the implementation excessively complex.

Despite such simplifications, it is shown that it is difficult to apply the same methods to converters with more than three cells. It is also shown that the existing balancing method tends to increase the total device switching frequency. An alternative modulation scheme is therefore proposed in section 6.3, which is easily applicable to the N-cell converter and which balances the capacitor

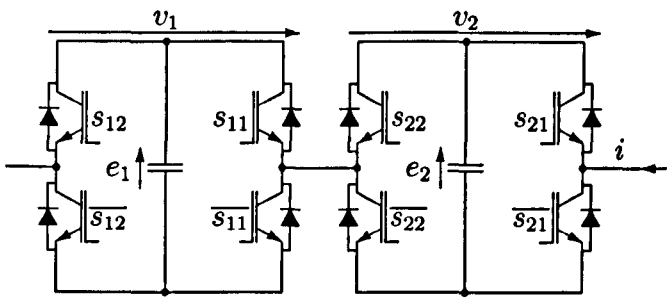


Figure 6.1: Two-cell cascaded H-bridge converter

s_n	s_{n2}	s_{n1}	v_n
-1	1	0	$-e_n$
0	0	0	0
1	0	1	e_n

s_n: State of n^{th} bridge

Table 6.1: Definition of switching state notation

voltages without increasing the device switching frequency.

6.1 Two-Cell Modulation

The one-dimensional modulation scheme has been described in detail for a two-cell converter in a range of publications [68], [69], [103]–[105]. For this reason, the initial discussion of one-dimensional modulation in this chapter also relates to a two-cell converter, an example of which is shown in Figure 6.1. The nomenclature of the switching states of each cell is defined in Table 6.1 in terms of the states of each half-bridge leg. The state of an entire phase, which comprises the states of the individual cells, is denoted as a row vector (s_1, s_2).

One-dimensional modulation relies on the representation of the output voltages produced by each switching state in a so-called *one-dimensional control region*, which is a plot of the output voltages of each state against a horizontal voltage scale. Figure 6.2 shows the control region for the two-cell converter with equal capacitor voltages. The redundant states of the phase leg are shown

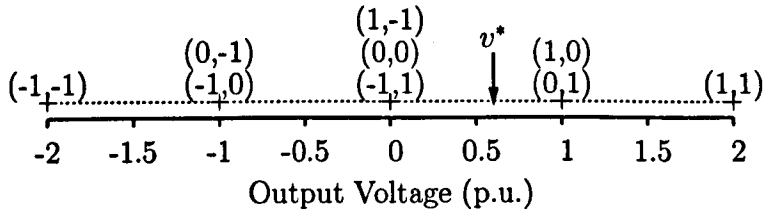


Figure 6.2: Normalized control region for two-cell converter with equal capacitor voltages

as several states labelling the same point.

At each sampling instant, the reference voltage (v^* in Figure 6.2) is sampled and the two states nearest to the reference are used to modulate. The choice of redundant states is left to the implementation, allowing optimization of the modulation.

When one-dimensional modulation is applied to converters with unequal capacitor voltages, the states move in the control region and cease to be redundant. The degree of imbalance determines the order of the states in the control region. A two-cell converter then has nine possible output voltages, which can be arranged in the four possible ways shown in Figure 6.3. The range of capacitor voltages for which each arrangement applies is also shown.

For the feed-forward version of one-dimensional modulation, the capacitor voltages are measured at each sampling instant and the control region is constructed by calculating output voltage of each state using (6.1):

$$V(s) = \sum_{r=1}^{N} e_r s_r, \tag{6.1}$$

where

s is the complete switching state of the phase leg,

e_r is the capacitor voltage of the r^{th} bridge and

s_r is the switching state of the r^{th} bridge, as defined in Table 6.1.

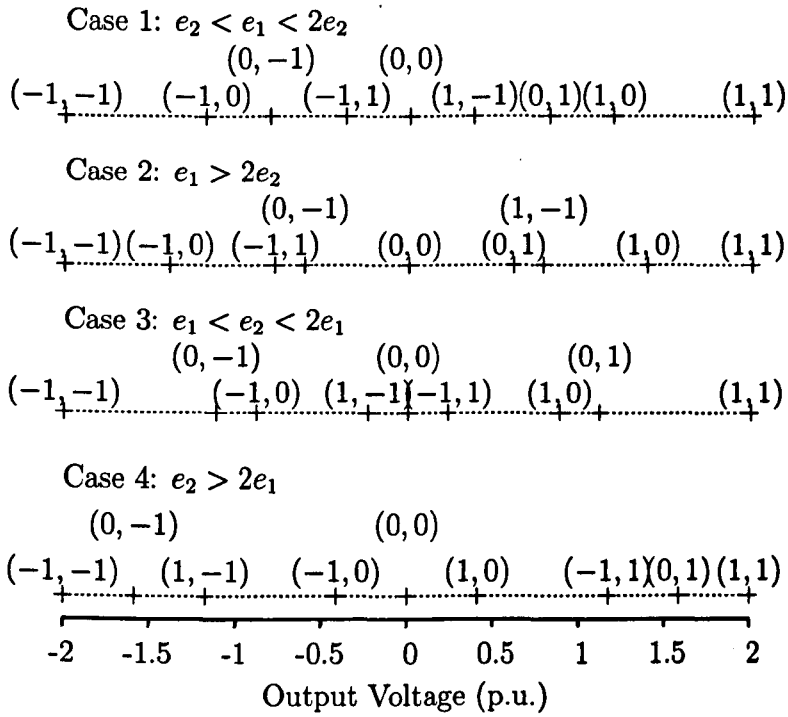


Figure 6.3: Control regions for two-cell converter with different d.c.-link voltages. State labels: (s_1, s_2)

Any reference voltage that lies within the control region can be synthesized accurately using two states that straddle the reference, assuming that the capacitor voltages do not change greatly during the sampling interval. The modulator must choose suitable states and calculate the period of time to apply each state.

The published implementation of one-dimensional modulation [69], [104] selects states using the following procedure. Firstly, the order of states in the control region is determined from measurements of the d.c.-link voltages. The measurements are compared against the conditions given in Figure 6.3 and a look-up table listing the states in order of their output voltage is chosen. The control region is then constructed by calculating the output voltage of each state using (6.1) and the two states nearest to the reference are located using an iterative search algorithm. The time for which each state should be applied is calculated using (6.2), such that the voltage-time area of the reference is

	Forbidden States	
d.c. Voltages	$i > 0$	$i < 0$
$e_1 > e_2$	$(1,-1),(1,0),(0,-1)$	$(-1,1),(-1,0),(0,1)$
$e_2 > e_1$	$(-1,1),(-1,0),(0,1)$	$(1,-1),(1,0),(0,-1)$

Table 6.2: Forbidden states under different conditions of capacitor voltages and a.c. current for two-cell case.

equal to that of the converter output voltage.

$$d_{S_1} = \frac{V(S_2) - v^*}{V(S_2) - V(S_1)} \qquad d_{S_2} = 1 - d_{S_1} \tag{6.2}$$

where

S_1 and S_2 are the switching states to be applied,

d_{S_1} is the proportion of the switching period for which S_1 should be applied,

d_{S_2} is the proportion of the switching period for which S_2 should be applied and

$V(s)$ is the output voltage produced by the switching state s, as defined in (6.1).

Although the principle of this algorithm is applicable to converters with any number of cells, it will be shown in section 6.2 that pre-determining all the possibilities for the order of states in the control region becomes cumbersome as the number of cells is increased.

6.1.1 Capacitor Balancing

One-dimensional modulation has been adapted to balance the capacitor voltages by eliminating states which cause the capacitor voltages to diverge [105]. At each sampling instant the set of forbidden states is chosen from Table 6.2 based on the direction of the current and the requirement to charge or discharge each capacitor. Of the remaining, permitted states, the two states nearest to the reference are used to modulate using duty cycles calculated using (6.2): the same duty-cycle calculation used for the non-balancing method.

6.1.2 Relationship to Carrier-Based Modulation

Although presented as a fundamentally different modulation technique, one-dimensional modulation is very closely related to regularly-sampled, carrier-based modulation. The relationship between these two modulation schemes is explored in this section.

Figure 6.4 shows a carrier-based representation of one-dimensional modulation for two sampling periods. The control region has been plotted on the vertical axis at the sampling instants and the horizontal axis represents the duration of the sampling interval T. To highlight the construction of the diagram, the two sampling periods are shown as separate plots and the position of the states in the control region are explicitly marked.

Calculation of the duty cycles using (6.2) is represented in Figure 6.4 by equivalent carrier signals, which have been constructed by joining the sampled position of adjacent states across the sampling time. As for regularly-sampled, carrier-based modulation, the switching state changes when the sampled reference, which is constant during a sampling interval, crosses a carrier signal. The second sampling interval in Figure 6.4 is constructed in the same way using new measurements of the capacitor voltages. As such, the control region is updated causing discontinuities in the carrier signals at each sampling instant.

The main difference between this representation and conventional carrier schemes, besides the discontinuous carrier signals, is that the carrier signals are not associated with individual gate signals. In some instances, multiple commutations are needed to change between neighbouring states. For example, when the reference shown in Figure 6.4 crosses from the $(0, 0)$ region to the $(1, -1)$ region, two commutations are required. When the capacitor voltages are equal these states are redundant so do not usually have their own regions in the carrier diagram.

A carrier-based diagram can also represent the voltage balancing method if carrier signals are constructed using only permitted states. Figure 6.5 is based on the same capacitor voltage values as Figure 6.4 but does not include all the possible converter states: only the states permitted for capacitor balancing with positive a.c. current are included. In the second sampling interval the set

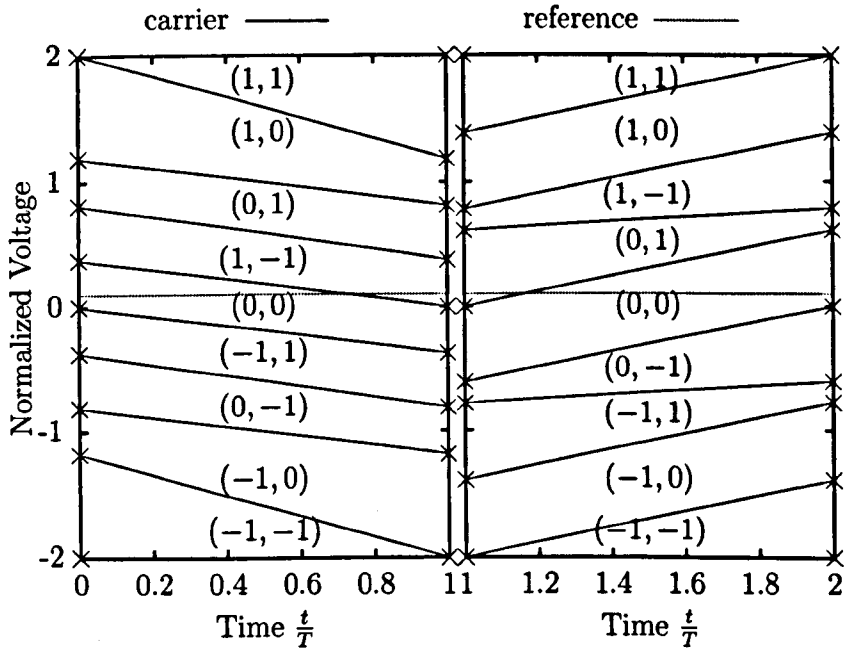


Figure 6.4: Carrier modulation showing all available states

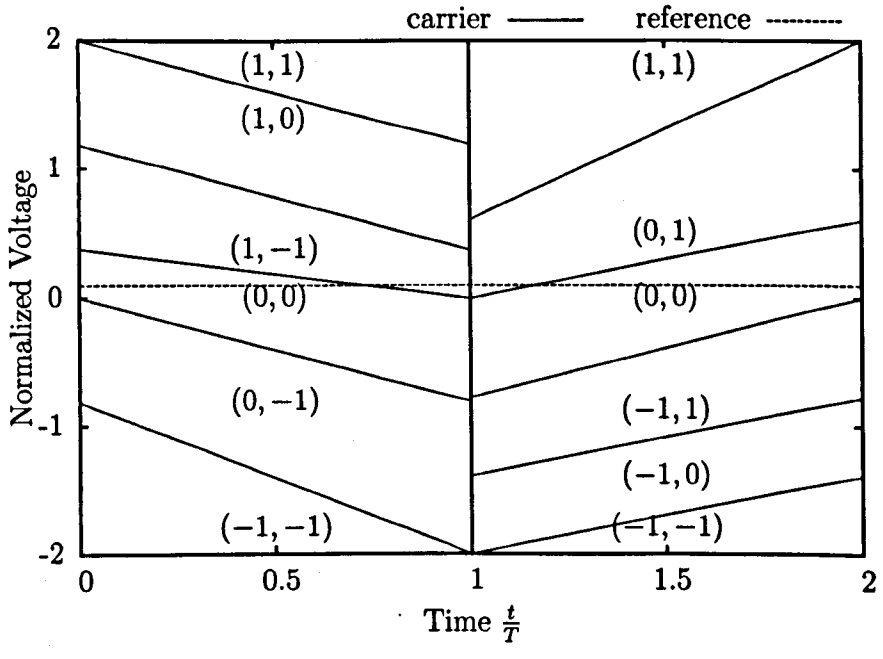


Figure 6.5: Carrier modulation with eliminated states

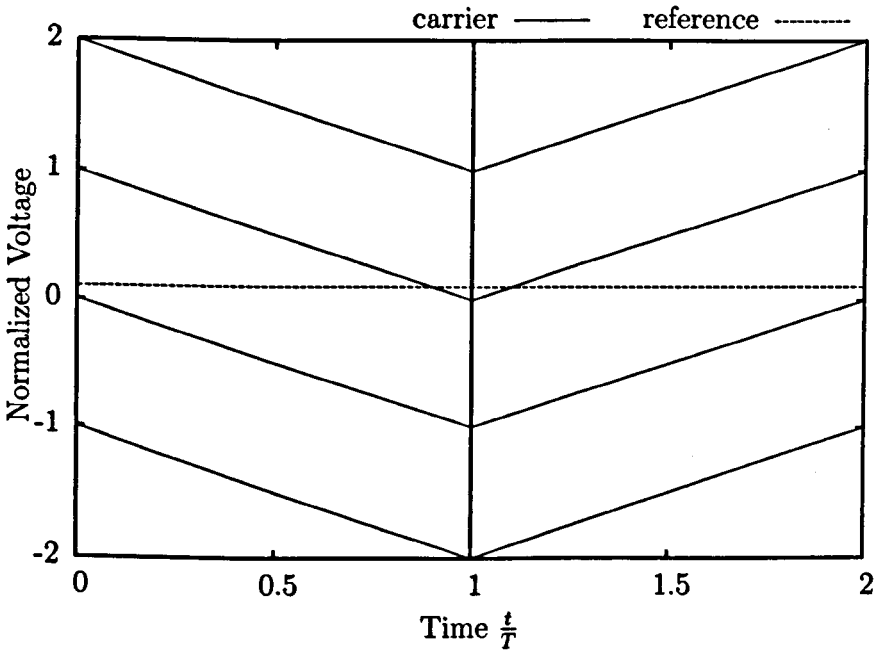


Figure 6.6: Carrier modulation with balanced d.c. links

of permitted states has changed, reflecting the possibility that the capacitor voltages cross during a sampling period.

The carrier signals in Figures 6.4 and 6.5 are shown alternating between falling and rising slopes in order to imitate the triangular carrier signals used in level-shifted carrier modulation (Figure 6.6). For this to be an accurate representation of one-dimensional modulation, the modulation must be implemented specifically to alternate between producing rising and falling edges in consecutive sampling periods, as was required of space-vector modulation in section 4.2.1. Existing publications do not specify the order in which the selected states should be applied but alternating the direction of the modulated switching edges causes one-dimensional modulation to produce identical voltage waveforms to asymmetrically-sampled, level-shifted carrier modulation when the capacitor voltages are balanced. To demonstrate this relationship, a two-cell converter has been simulated using ideal voltage sources. The resulting phase voltage and line-voltage spectrum are shown to be indistinguishable in Figure 6.7.

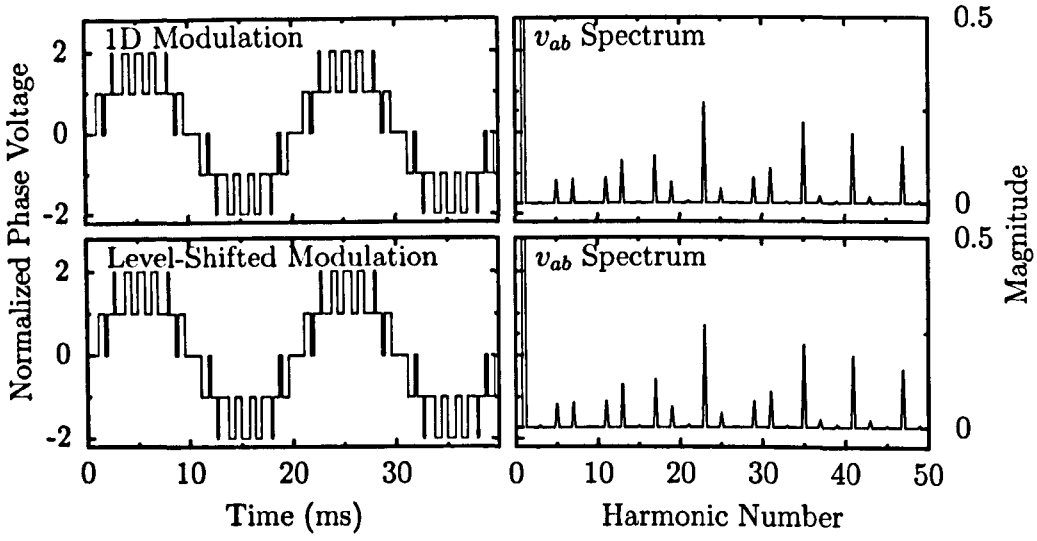


Figure 6.7: Phase voltage and line-voltage spectrum of simulated one-dimensional modulation and regularly-sampled, level-shifted carrier modulation

6.2 Application to More Cells

One-dimensional modulation can be applied to converters with more than two cells, but the implementation needs modifying in order to remain practical. For the two-cell case, all the possibilities for the order of states in the control region are pre-determined and stored in look-up tables. Working out all the possible arrangements of the 3^N states of an N-cell converter quickly becomes difficult as the number of cells increases.

In this section, the two-cell algorithm is simplified to reduce the number of look-up tables needed. These simplifications allow one-dimensional modulation to be applied to the three-cell converter in section 6.2.2.

6.2.1 Simplification of the Two-Cell Algorithm

The first simplification that can be applied to the one-dimensional modulation algorithm is to sort the bridges in order of their capacitor voltages. The capacitor voltages of a two-cell converter can then be designated $e_{\max}$ and $e_{\min}$,

where

$e_{\min}$ is lower capacitor voltage and

$e_{\max}$ is the greater capacitor voltage.

The switching states can be written as $(s_{\max}, s_{\min})$, where

$s_{\min}$ is the state of the bridge with lower capacitor voltage and

$s_{\max}$ is the state of the bridge with greater capacitor voltage.

When the states of the bridges are represented in this way, only the two sequences in Figure 6.8 need to be stored instead of the original four sequences in Figure 6.3. Cases 1 and 3 in Figure 6.3 and cases 2 and 4 differ only by which bridge has the greater d.c. voltage. Therefore, if the cells are considered in order of their capacitor voltages, cases 1 and 3 in Figure 6.3 are equivalent to case X in Figure 6.8 and cases 2 and 4 are equivalent to case Y.

When balancing the capacitor voltages, there are four possible arrangements of permitted and forbidden states: these are shown in Figure 6.9. Cases $X1$ and $X2$ are the result of eliminating the states listed in Table 6.2 from Case X for positive and negative current; cases $Y1$ and $Y2$ are produced in the same way for case Y. The remaining permitted states are in the same order in cases $X1$ and $Y1$ and also in cases $X2$ and $Y2$. Hence only two tables are needed.

Figure 6.9 also shows that the permitted states with positive current (cases $X2$ and $Y2$) are the complement of the states permitted when the current is negative (cases $X1$ and $Y1$). The positions of the permitted states in the control region with negative current are therefore the reflection about the origin of the permitted states when the current is positive. This observation allows the single set of states in Figure 6.10, which are the permitted states with positive current, to be used when the current flows in either direction. For negative current $-v^*$ can be used as the reference if, after choosing states and calculating duty cycles, the complement of the chosen states are applied to the converter.

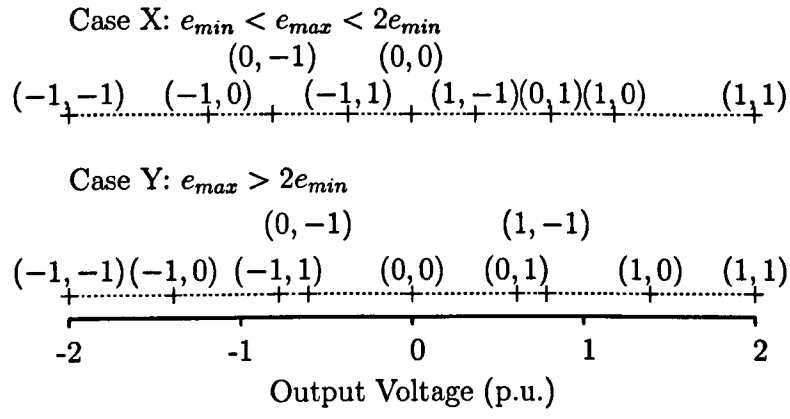


Figure 6.8: Control regions when bridges are stored by voltage magnitude. States are written as $(s_{\max}, s_{\min})$.

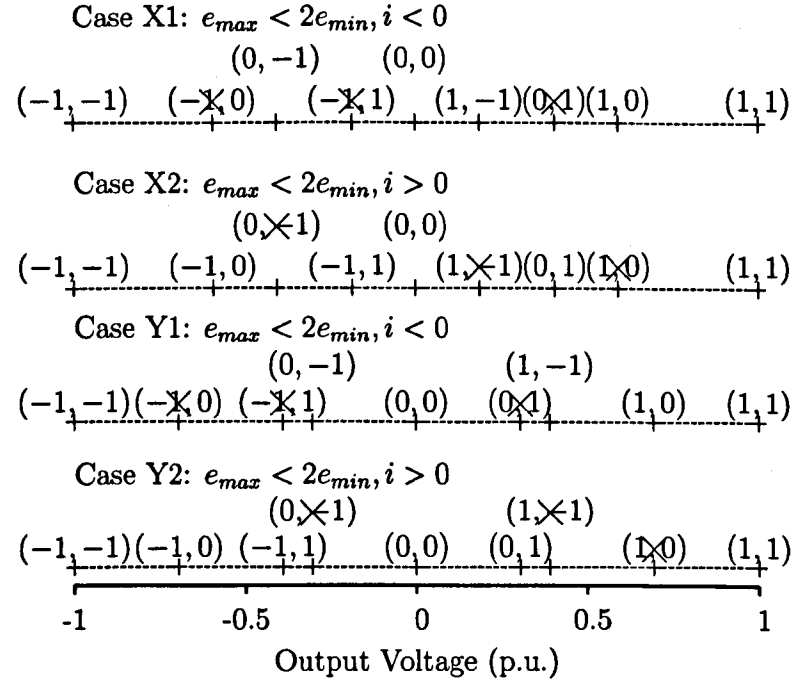


Figure 6.9: Control regions when bridges are sorted by voltage magnitude and states are eliminated for capacitor voltage balancing. States are written as $(s_{\max}, s_{\min})$.

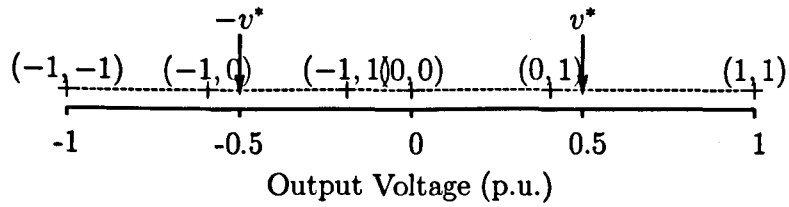


Figure 6.10: Two-cell control region using single set of permitted states

Hence, by considering the bridges in order of their capacitor voltages and taking advantages of the symmetry between the permitted states when current is positive and negative, one-dimensional modulation with balancing of the capacitor voltages can be applied to a two-cell converter using a single look-up table.

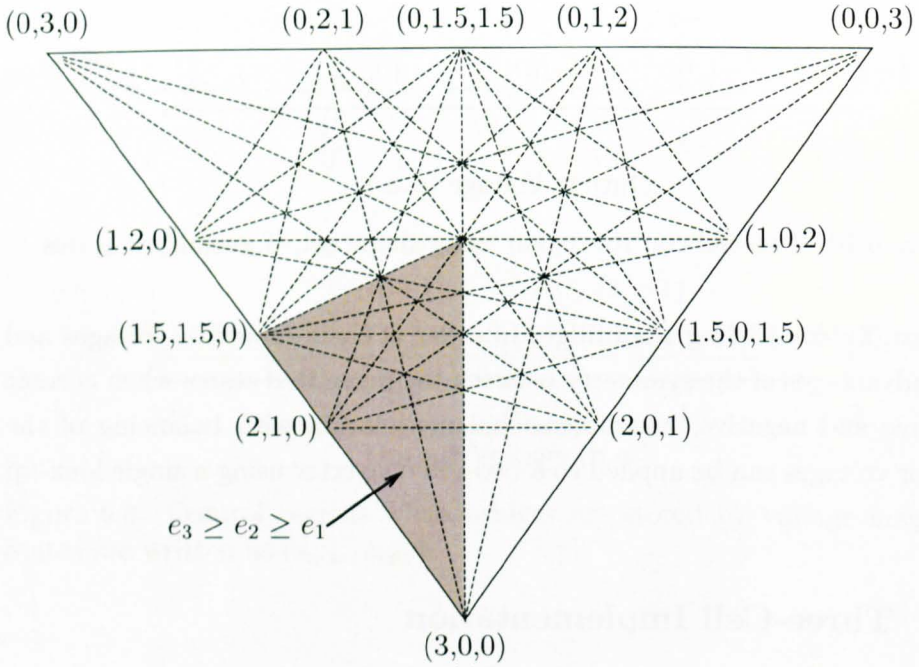
6.2.2 Three-Cell Implementation

Without the simplifications described in section 6.2.1, applying one-dimensional modulation to a three-cell converter is complex because of the large number of possible arrangements of states.

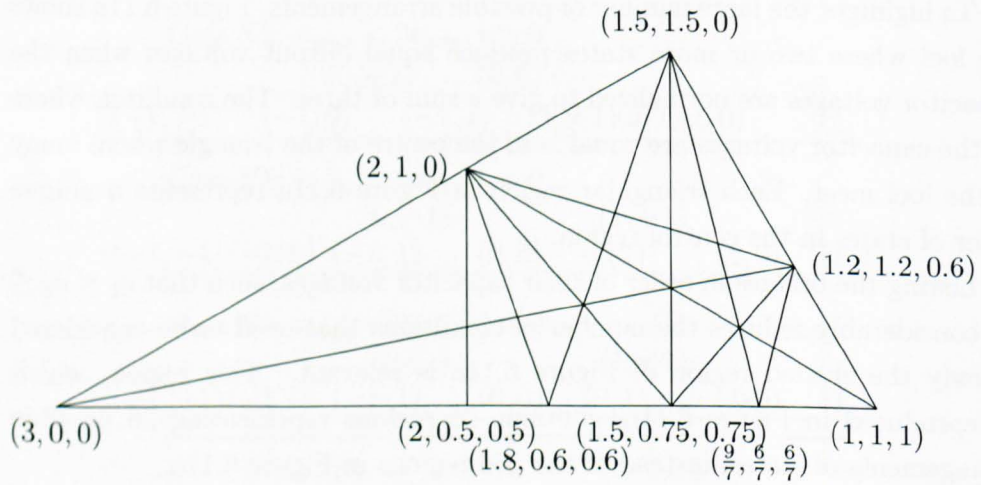
To highlight the large number of possible arrangements, Figure 6.11a shows the loci where two or more states produce equal output voltages when the capacitor voltages are normalized to give a sum of three. The condition where all the capacitor voltages are equal is in the centre of the triangle where many of the loci meet. Each triangular region in Figure 6.11a represents a unique order of states in the control region.

Listing the bridges in order of their capacitor voltages, such that $e_1 \leq e_2 \leq e_3$, considerably reduces the number of conditions that need to be considered as only the shaded region of Figure 6.11a is relevant. This region, which is reproduced in Figure 6.11b, contains 26 regions representing 26 possible arrangements of states, instead of the 156 regions in Figure 6.11a.

To apply one-dimensional modulation to a three-cell converter, the modulator uses measurements of the capacitor voltages to identify which region of Figure 6.11b the converter is operating in and selects a pre-calculated look-up table listing the states in order of their output voltage. Once the appropriate table is selected the modulation algorithm proceeds exactly as for the two-



(a)



(b)

Figure 6.11: Regions representing the possible order of states in the control region for a three cell converter (a) for the whole range of possible capacitor voltages (b) for the case where $e_3 \geq e_2 \geq e_1$ Labels: (e_3, e_2, e_1)

cell case: the control region is populated using measured capacitor voltages and then two nearest states to the reference are located and applied for time periods calculated using (6.2).

Capacitor Voltage Balancing

The capacitor voltages of a three-cell converter can be balanced by eliminating states from the modulation process in a similar manner as was described for a two-cell converter in section 6.1.1. Permitted states are those that charge the capacitor with lowest voltage or discharge the capacitor with greatest voltage. The states $(-1,-1,-1)$, $(0,0,0)$ and $(1,1,1)$ are always permitted, irrespective of their effect on the capacitor voltage, so that the output voltage range is not limited. The permitted states for both positive and negative current are shown in Figure 6.12, in which the states are listed in order (e_3, e_2, e_1) with $e_3 \geq e_2 \geq e_1$.

Reducing the number of permitted states also reduces the number of possible arrangements of those states in the control region. The twelve states are permitted when the current is positive can be arranged in one of five possible ways, instead of the 26 possibilities when all states are considered. The boundaries defining the order of states are shown in Figure 6.13 and example control regions corresponding to each region are shown in Figure 6.14. The highlighted states in Figure 6.14 are those whose order changes as each boundary in Figure 6.13 is crossed.

Figures 6.13 and 6.14 only include the states that are permitted when the current is positive but there is no need to produce similar diagrams for the reverse current direction. As for the two-cell converter, the states that are permitted when the current is negative are the complement of those that are permitted when the current is positive. Figures 6.13 and 6.14 are equally applicable for the reverse current direction if the reference voltage is first negated and then the complement of each chosen switching state is applied to the converter. This is the same procedure that was described for the two-cell converter in section 6.2.1.

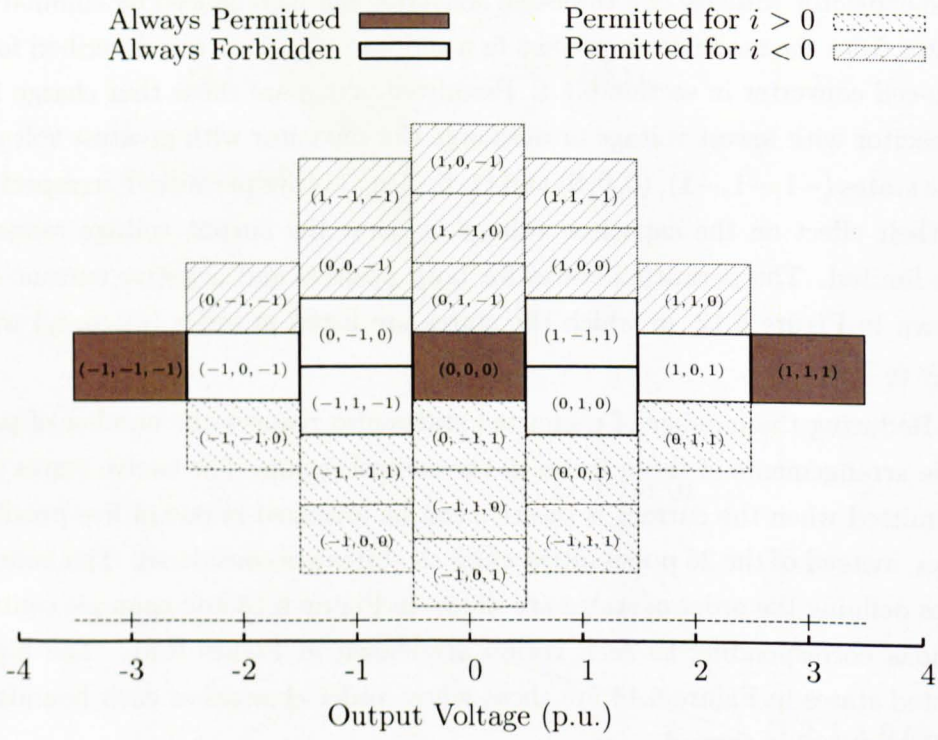


Figure 6.12: Permitted states for the capacitor balancing of a three-cell converter

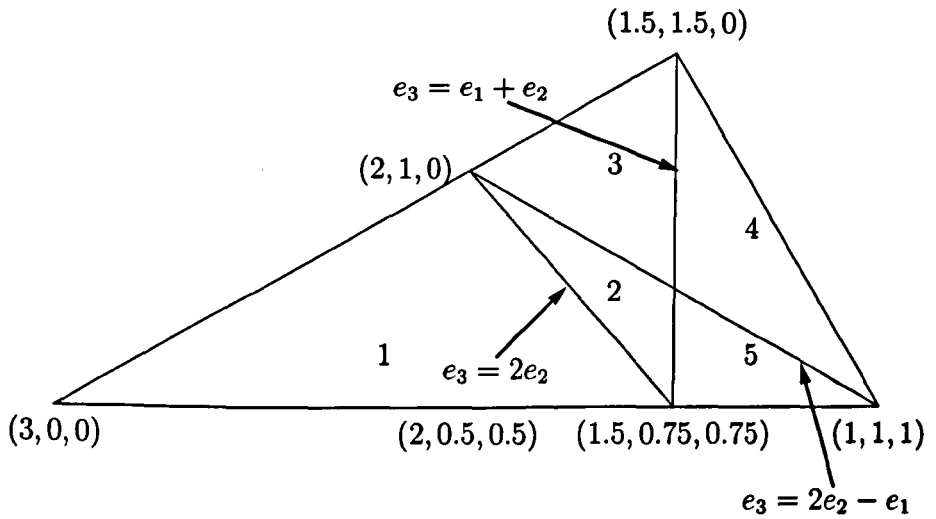


Figure 6.13: Boundaries between different sequences of states used for balancing with positive current

6.2.3 Simulations of the Three-Cell Converter

A converter with three cells per phase has been simulated in rectifying configuration (Figure 6.15) using the one-dimensional algorithm described. To demonstrate the performance of the balancing algorithm, the converter has been simulated in the three sets of conditions given in Table 6.3 and plotted in Figure 6.16. Also included in Figure 6.16 are the boundaries within which it is possible to balance the capacitor voltages, which were derived in Chapter 5.

Note that in feed-forward modulation schemes, the modulation index of the phase leg is not a constant value in steady state, as it varies in order to compensate for ripple of the capacitor voltages. The modulation index used to plot the operating points in Figure 6.16 is the steady-state modulation index that would produce the same operating point if the capacitor voltages were constantly equal to their reference.

Cases A and B in Figure 6.16 are within the limits defined in section 5.1.1 for which it is possible to equalize the capacitor voltages; case C is outside

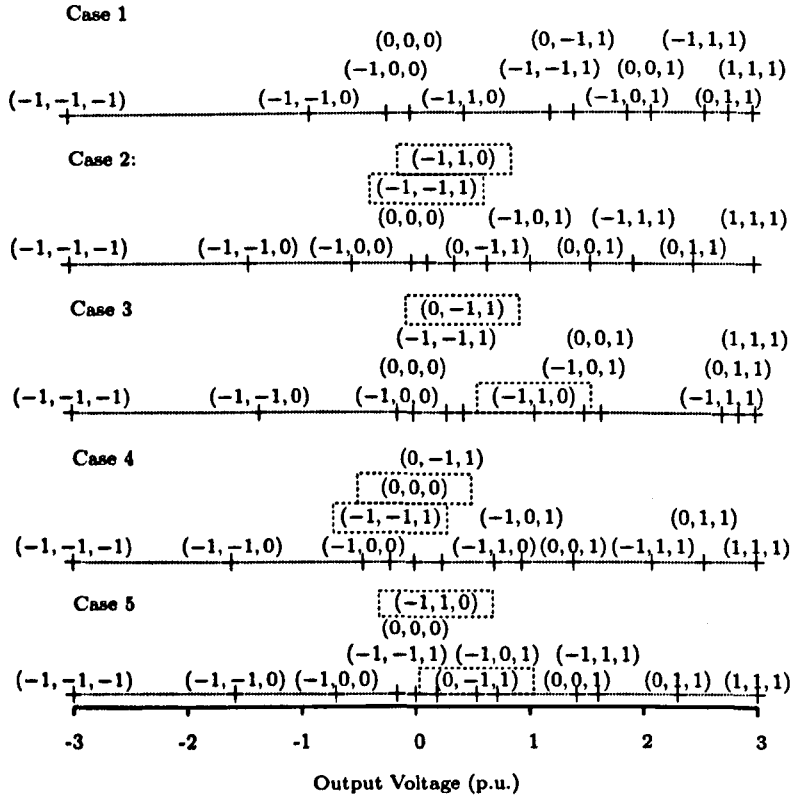


Figure 6.14: The five possible sequences of permitted states when the a.c. current is positive

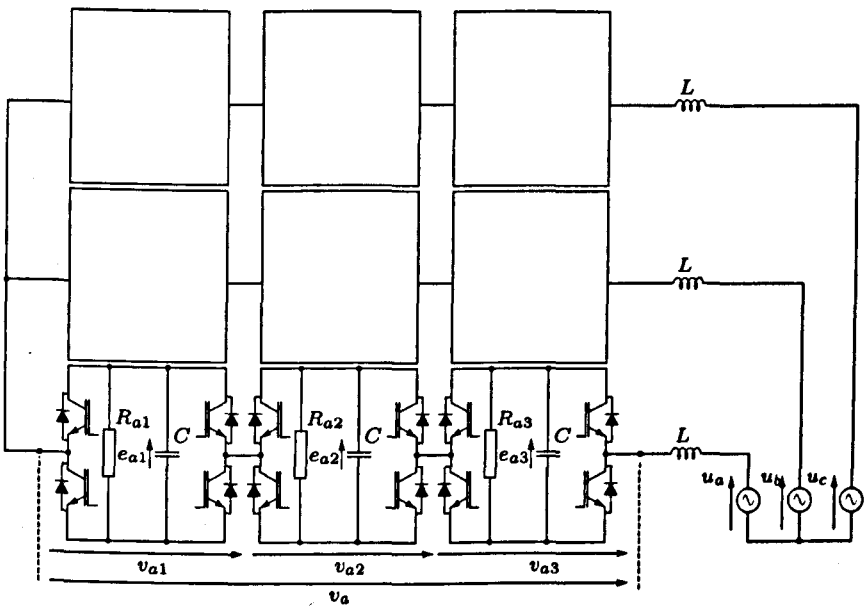


Figure 6.15: Circuit configuration for rectifying simulations and experimental tests

	E^*	$\hat{u}$	R_{a1}	R_{a2}	R_{a3}
Case A	100V	285V	57Ω	57Ω	57Ω
Case B	100V	285V	43Ω	57Ω	57Ω
Case C	100V	285V	29Ω	57Ω	57Ω

Table 6.3: Conditions for simulation

that range. Figure 6.17 confirms this as the capacitor voltages remain balanced for cases A and B but the voltage of the over-loaded cell reduces in case C. The switching waveforms shown in Figure 6.18 are for phase a of the case B simulation and show how the modulator distributes commutations between each bridge in response to differing loads. The switching rate is quantified in Figure 6.19, which shows the cumulative average rate of commutation for each bridge over the full duration of the case B simulation. The switching functions of the two bridges with equal capacitor voltage (s_{a2} and s_{a3}) commutate on average at the same rate of 30 commutations per cycle. Because of the imbalanced load, s_{a1} contains fewer commutations: 20 per cycle.

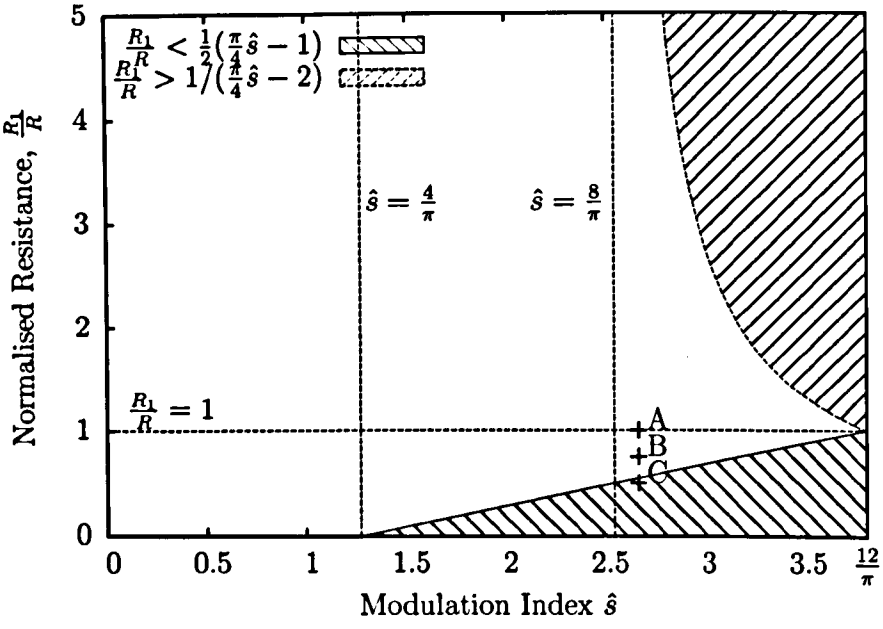


Figure 6.16: Loading conditions applied to three-cell simulations with the balancing capabilities derived in section 5.1.1

Figure 6.19 also shows the apparent rate of commutation derived from the phase-a switching function and the total sum of the commutations from each bridge. The fact that the phase-a switching function contains 40 commutations per cycle and the individual bridges produce a total of 70 commutations per cycle indicates that multiple commutations occur simultaneously and that the total device switching frequency is not minimized.

Simultaneous commutations are mostly caused by changes to the list of permitted states when the order of d.c. link voltages changes. For example, at the first sampling instant in Figure 6.20 (217.333ms) the capacitor voltages are in the following order:

$$e_{a1} < e_{a3} < e_{a2}.$$

During the sampling interval the capacitor voltages cross so at the next sampling instant (218ms) the order is different:

$$e_{a2} < e_{a3} < e_{a1}.$$

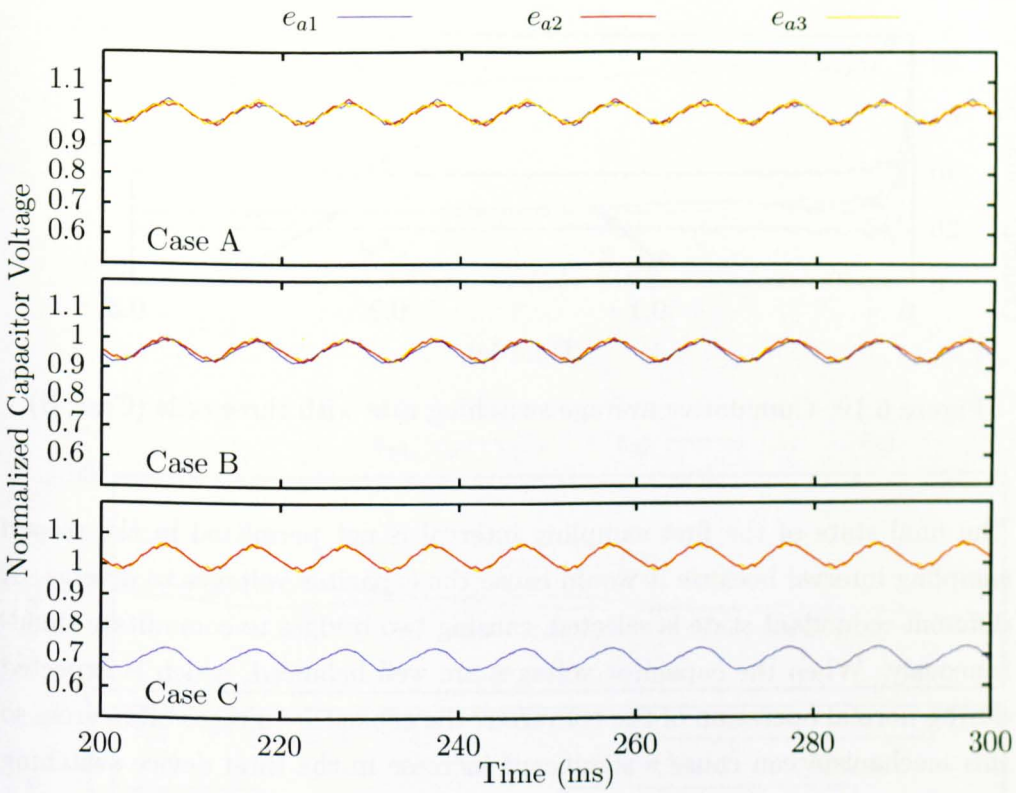


Figure 6.17: Simulated steady-state capacitor voltages at operating points corresponding to each of the points marked in Figure 6.16.

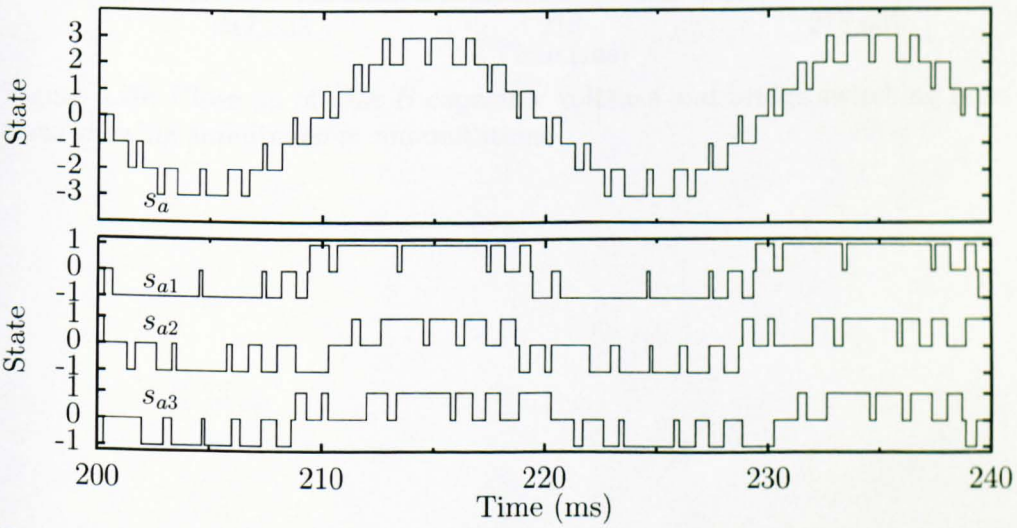


Figure 6.18: Phase-a switching function and individual bridge switching functions for case B

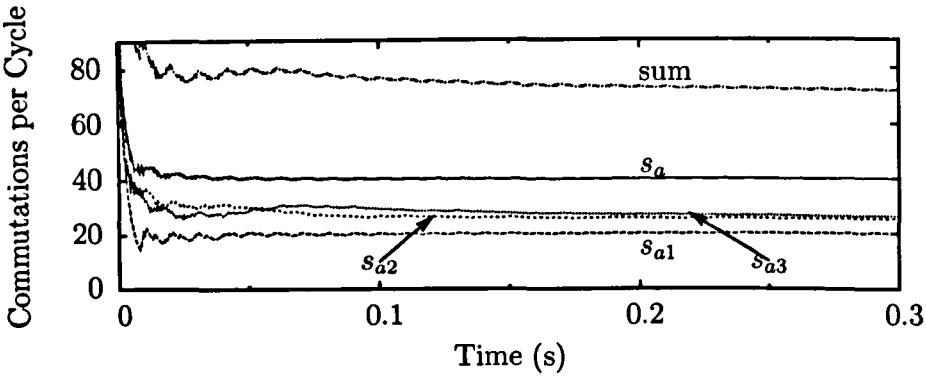


Figure 6.19: Cumulative average switching rate with three cells (Case B)

The final state of the first sampling interval is not permitted in the second sampling interval because it would cause the capacitor voltages to diverge. A different redundant state is selected, causing two bridges to commutate simultaneously. When the capacitor voltages are well balanced, which is expected during normal operation of the converter, the capacitor voltages often cross so this mechanism can cause a significant increase in the total device switching frequency.

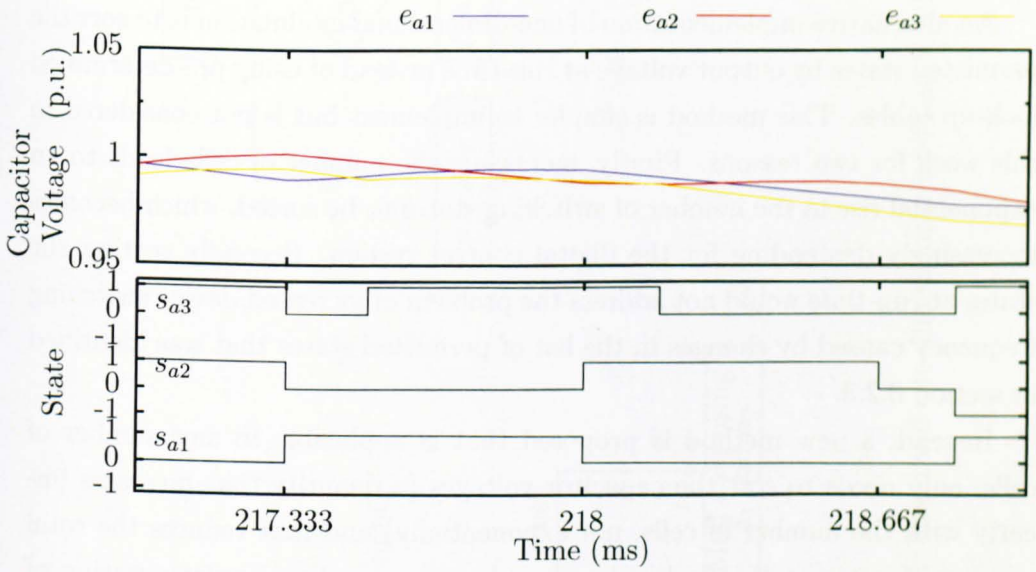


Figure 6.20: Close-up of case B capacitor voltages and bridge switching functions showing simultaneous commutations

6.3 Improved One-Dimensional Modulation for N-Cell Converters

Although the one-dimensional modulation scheme described so far can be applied to converters with any number of levels, it is not a truly N-cell algorithm. The analysis of the control region for the three-cell case is not applicable when a different number of cells is used. Equivalent, but increasingly complex, analysis must be performed every time that a different number of cells is considered in order to deduce the possible arrangements of states.

An alternative implementation of one-dimensional modulation is to sort the permitted states by output voltage at run-time instead of using pre-determined look-up tables. This method is simpler to implement but is not considered in this work for two reasons. Firstly, increasing the number of cells leads to an exponential rise in the number of switching states to be sorted, which becomes increasingly demanding for the digital control system. Secondly sorting the states at run-time would not address the problem of increased device switching frequency caused by changes in the list of permitted states that was identified in section 6.2.3.

Instead, a new method is proposed that is applicable to any number of cells, only needs to sort the capacitor voltages (a quantity that increases linearly with the number of cells, not exponentially) and that reduces the total number of commutations when compared to the previous implementation of one-dimensional modulation. The proposed algorithm operates in a similar way to the balancing algorithm described in Chapter 5 for space-vector modulation: by assigning demanded commutations to the most suitable bridge.

6.3.1 Balancing Algorithm

The proposed method for selecting switching states is made up of the two nested loops depicted in Figure 6.21 using the notation defined below.

S_1,S_2 Two switching states of the phase leg that are being considered for application during the upcoming sampling interval.

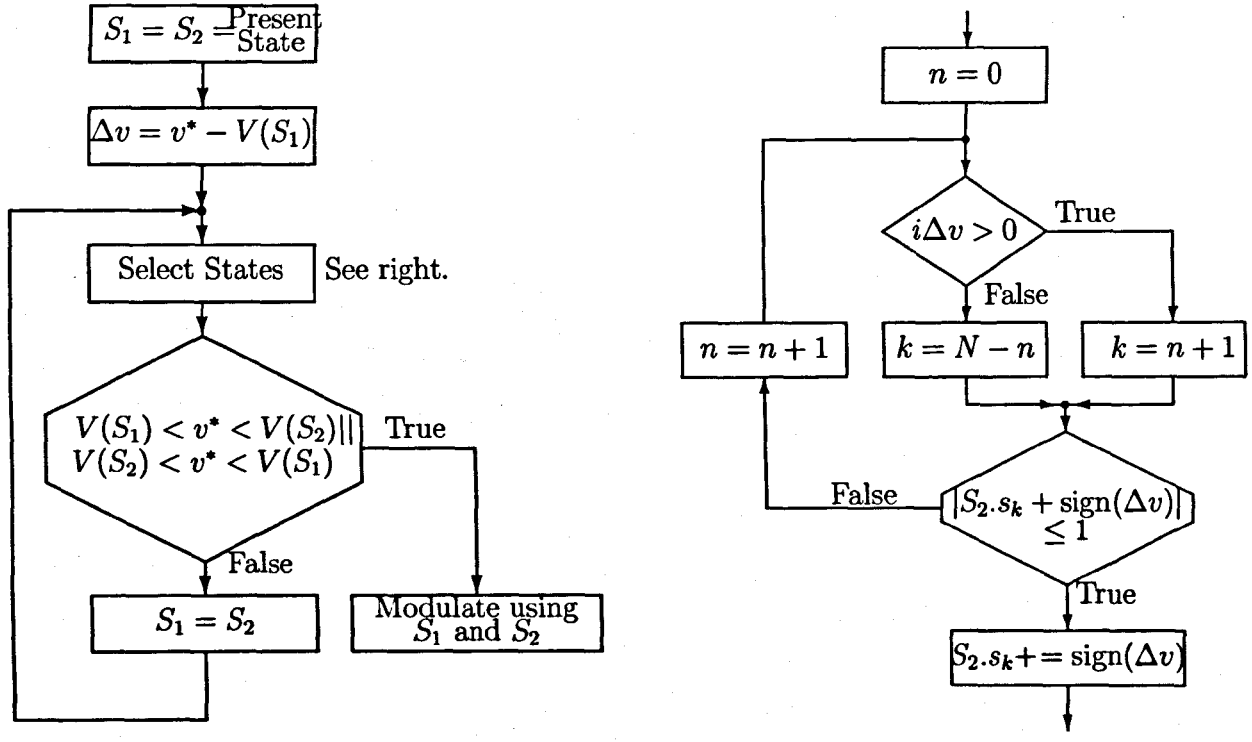


Figure 6.21: Improved one-dimensional modulation scheme

$S_1.s_k$ The component of S_1 representing the switching state of the bridge with the k^{th} smallest capacitor voltage.

$V(S)$ The output voltage of state S, defined in (6.1).

Δv The direction of the required voltage step.

At each sampling instant, the outer loop (on the left side of Figure 6.21) stores two possible switching states. Once the algorithm is completed these states become the two states to be applied during the next sampling period. Initially, S_1 and S_2 are set to the present state of the phase leg so that the possibility of not changing the switching state at the sampling instant is always considered.

The inner loop, on the right of Figure 6.21, modifies the second state, S_2, by a single commutation to produce a voltage step in the required direction. The most suitable bridge to commutate is identified in the same way as was applied to space-vector modulation in Chapter 5: by searching through a list of bridges sorted in order of their capacitor voltages. If the product of current and step direction $i\Delta v$ is positive then the search begins at the bridge with lowest capacitor voltage or, if $i\Delta v$ is negative, then the search begins at the other end of the list. There are strong similarities between this balancing algorithm and the algorithm applied to space-vector modulation so the inner loop of Figure 6.21 should be compared to Figure 5.9 on page 148.

Once S_2 has been changed, the outer loop assesses whether the two stored states, S_1 and S_2, straddle the reference voltage: if they do then those states are used to modulate with duty cycle calculated using (6.2), exactly as for conventional one-dimensional modulation. The order in which the chosen states should be applied are chosen in order to mimic one-dimensional modulation by alternating between falling and rising edges during the sampling period.

If the chosen states do not straddle the reference then another commutation is required and the inner loop is called again using S_2 as the new starting point. In this way, the algorithm performs a stepwise search of the control region to find states that can produce the required output, whilst biasing the choice of switching states towards those which improve the balancing of the capacitor voltages.

	E^*	$\hat{u}$	R_{a1}	R_{a2}	R_{a3}
Case A	75V	200V	57Ω	57Ω	57Ω
Case B	75V	200V	39Ω	57Ω	57Ω
Case C	75V	200V	30Ω	57Ω	57Ω

Table 6.4: Conditions for experimental tests

The key difference between the method described in this section and the balancing method applied to space-vector modulation in Chapter 5 is the order of the state-selection and dwell-time calculations. In the space-vector case, the balancing algorithm is invoked after the dwell times have been calculated so the loop must only search for the most suitable bridge that can provide a voltage step in the required direction. For the one-dimensional implementation, the voltage output of the chosen states must then be checked to ensure that they straddle the reference and the duty cycle is calculated after the states are chosen. The one-dimensional modulation should therefore be more tolerant to operation when the capacitor voltages are not balanced as the feed-forward capability does not rely on the average capacitor voltage being a good approximation of the capacitor voltage of a given cell.

6.4 Experimental Results

The original one-dimensional modulation scheme and the improved method have been tested using the experimental converter in the rectifying configuration shown in Figure 6.15. The configuration of each experiment is shown in Table 6.4 and plotted in Figure 6.22 alongside the theoretical balancing limits defined in Chapter 5. Capacitor voltages, phase voltages and switching functions for each case are shown in Figures 6.23 to 6.25. Key observations deriving from these figures are summarized below:

- Both methods maintain equal capacitor voltages for cases A and B, where the operating point is within the balancing limits derived in Chapter 5.
- Neither method can balance the capacitor voltage in case C, where the resistance of the load of one cell has been reduced sufficiently to place

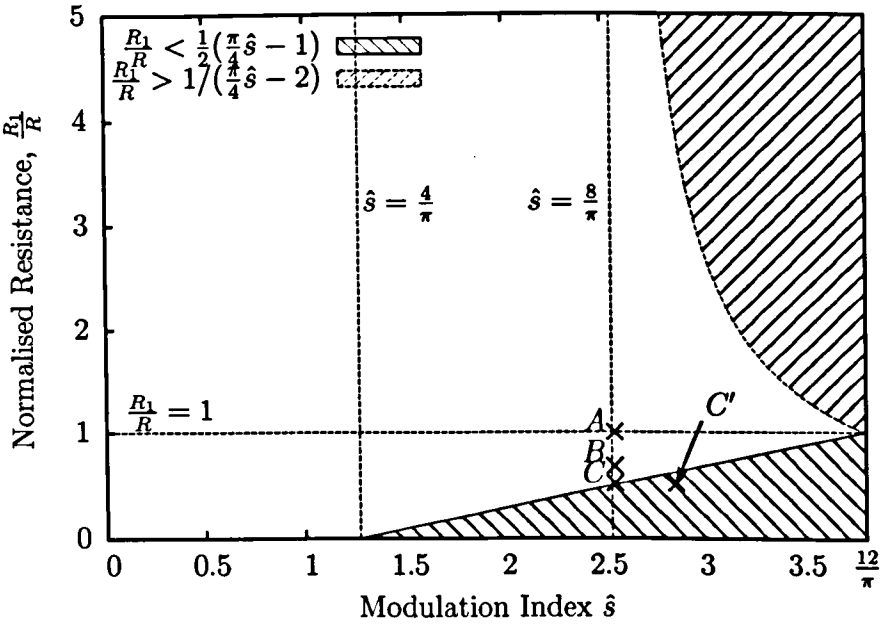


Figure 6.22: Loading conditions for experimental tests of one-dimensional modulation in regard to the theoretical balancing limits.

the operating point outside the limits of balancing.

- The original one-dimensional modulation method produces less deviation of the capacitor voltages during each cycle than the new method.
- The original modulation method produces a higher device switching frequency than the new method, despite the methods producing comparable leg switching functions.

Case C, in which the capacitors are not balanced, requires special attention because, although the operating point appears to be very close to the balancing limit, both modulation schemes fail to balance the voltages and the resulting voltage drop is large. It may be expected that only a small reduction in voltage would be visible when operating so near to the boundary.

There are two effects which contribute to the large reduction in voltage in case C. Firstly, the modulation index used to construct Figure 6.22 is the modulation index that would be required with constant capacitor voltages

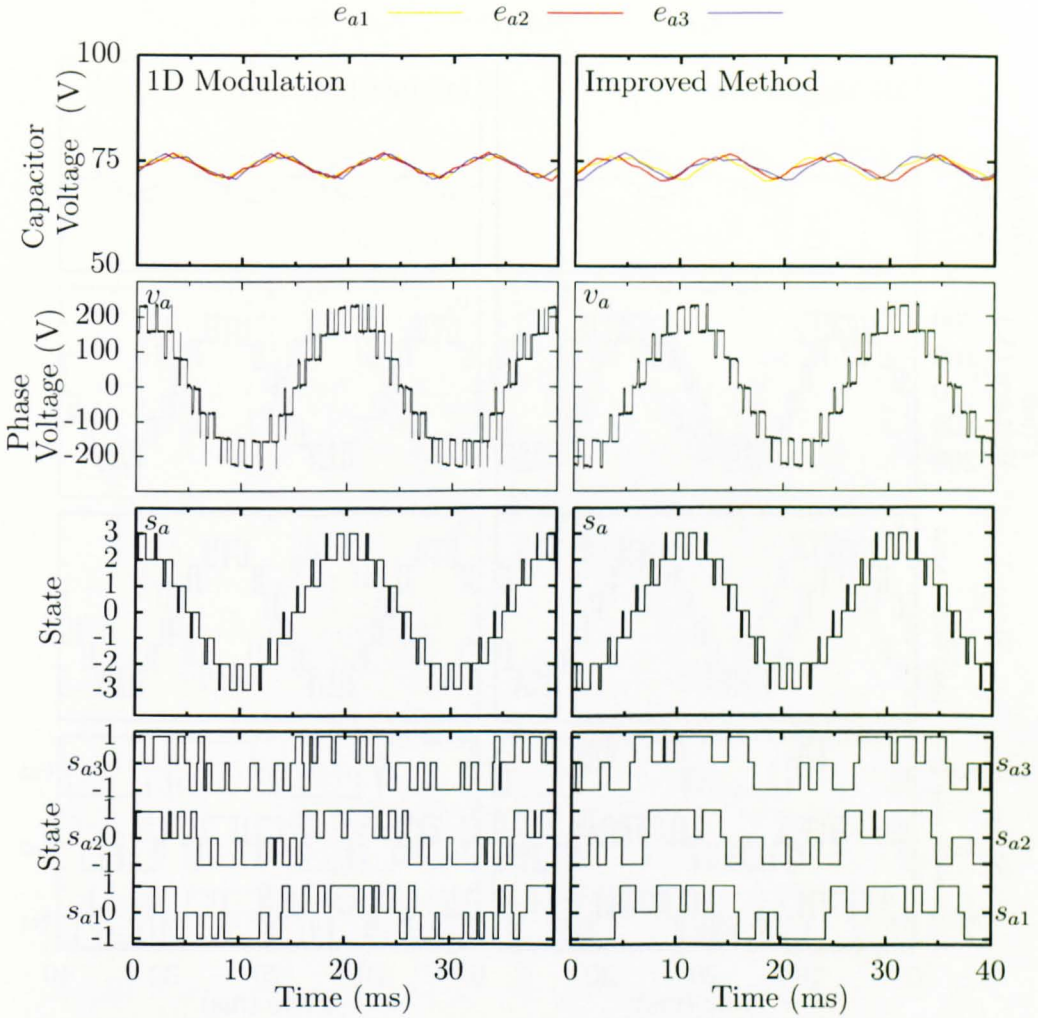


Figure 6.23: Capacitor voltages, phase voltages, switching functions and bridge switching functions for one-dimensional modulation and the improved method. Case A: $R_1 = R_2 = R_3 = 57\Omega$

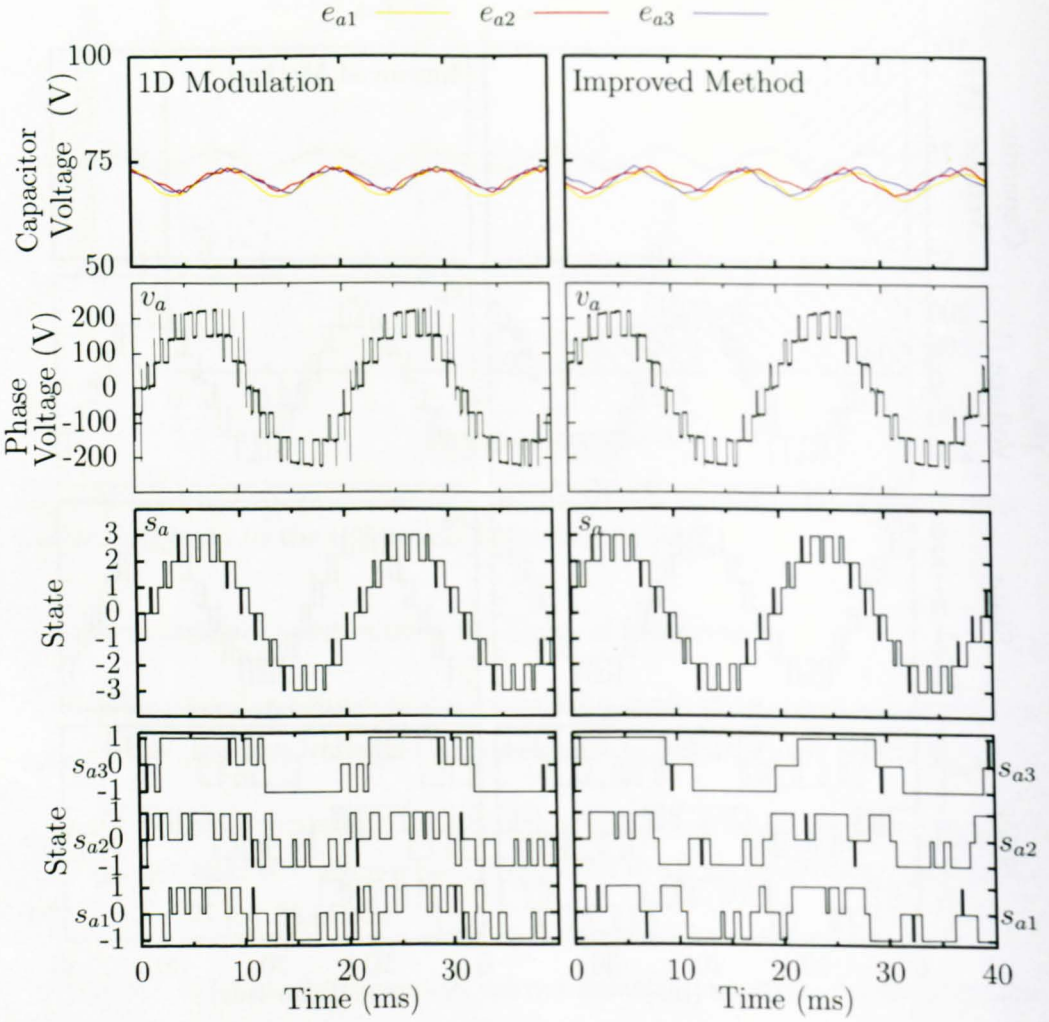


Figure 6.24: Capacitor voltages, phase voltages, switching functions and bridge switching functions for one-dimensional modulation and the improved method. Case B: $R_1 = R_2 = 57\Omega$, $R_3 = 39\Omega$

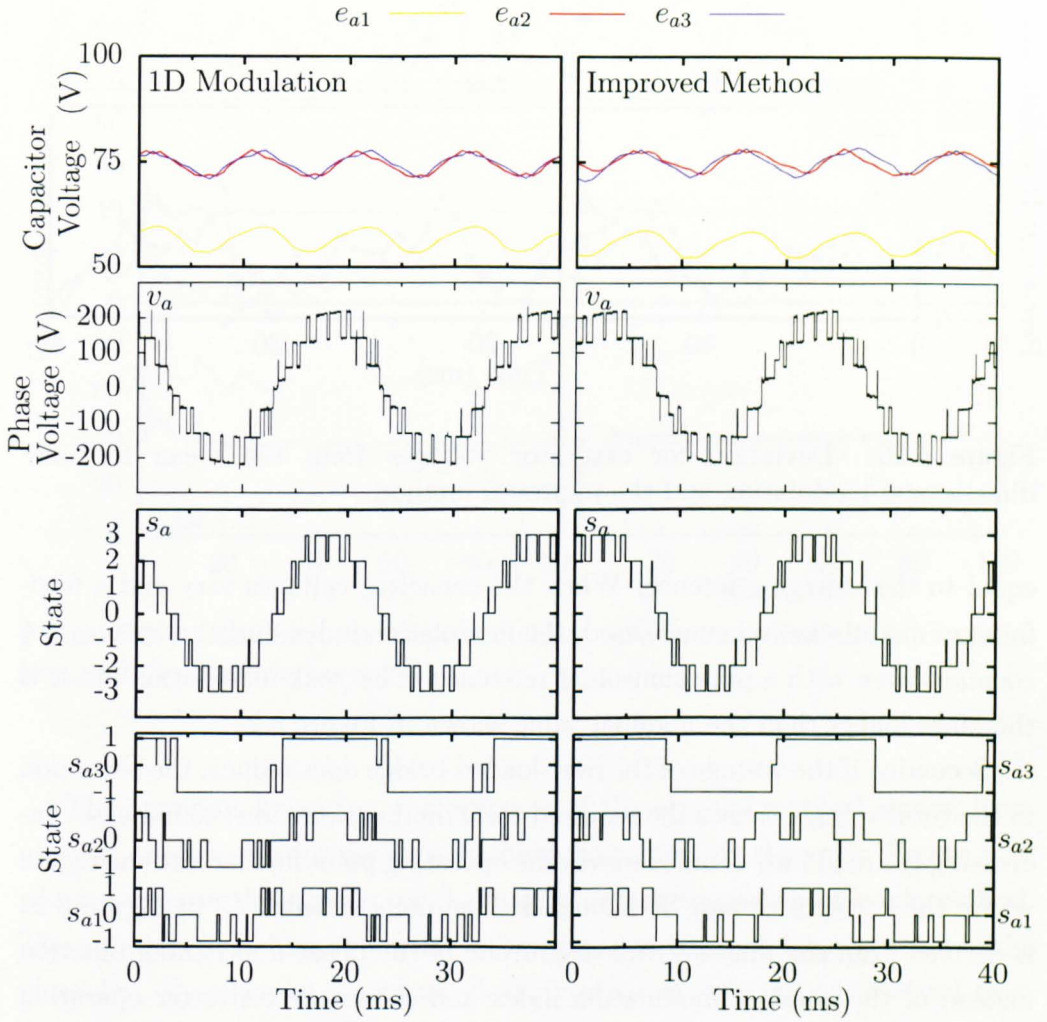


Figure 6.25: Capacitor voltages, phase voltages, switching functions and bridge switching functions for one-dimensional modulation and the improved method. Case C: $R_1 = R_2 = 57\Omega$, $R_3 = 30\Omega$

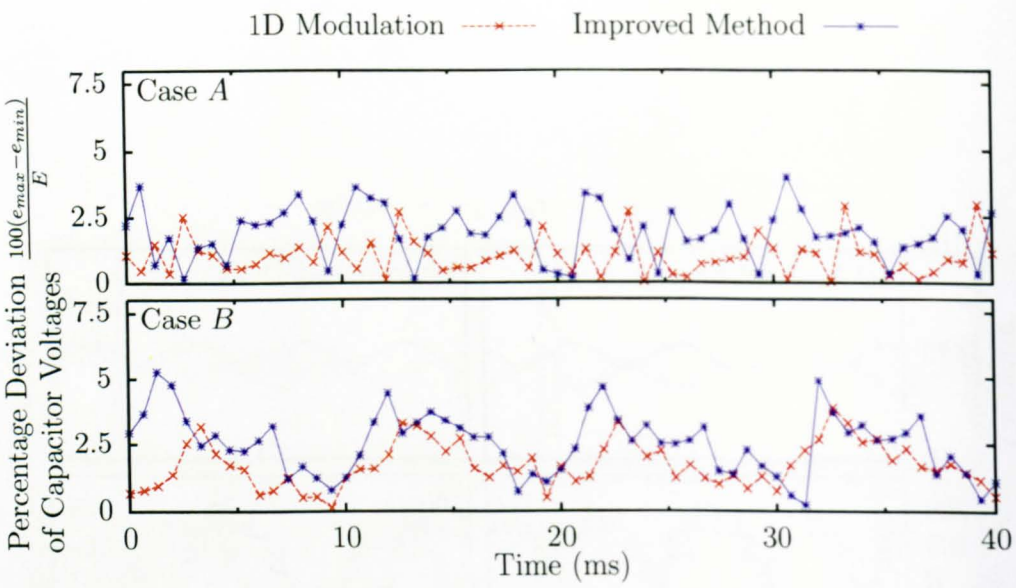


Figure 6.26: Deviation for capacitor voltages from the mean for one-dimensional modulation and the improved method

equal to the voltage reference. When the capacitor voltages vary and a feed-forward modulation scheme is used, the modulation index during a cycle is not constant even with a pure sinusoidal reference. The peak modulation index is therefore higher than the nominal value shown in Figure 6.22.

Secondly, if the voltage of the over-loaded bridge does reduce, the reduction in the total voltage causes the required total modulation index to increase. Increasing the modulation index moves the operating point further into the region where the voltages cannot be balanced. The point labelled C' in Figure 6.22 is derived from the fundamental magnitude of the phase-a switching function instead of the nominal modulation index and shows the converter operating well into the region where the capacitor voltages cannot be balanced.

For the balanced examples, Cases A and B, the difference in balancing performance of the original and modified modulation schemes is quantified in Figure 6.26, which shows the range of capacitor voltage expressed as a percentage of the reference at each sampling instant. The deviation of the new method is greater than the original for the majority of each cycle and reaches a greater peak.

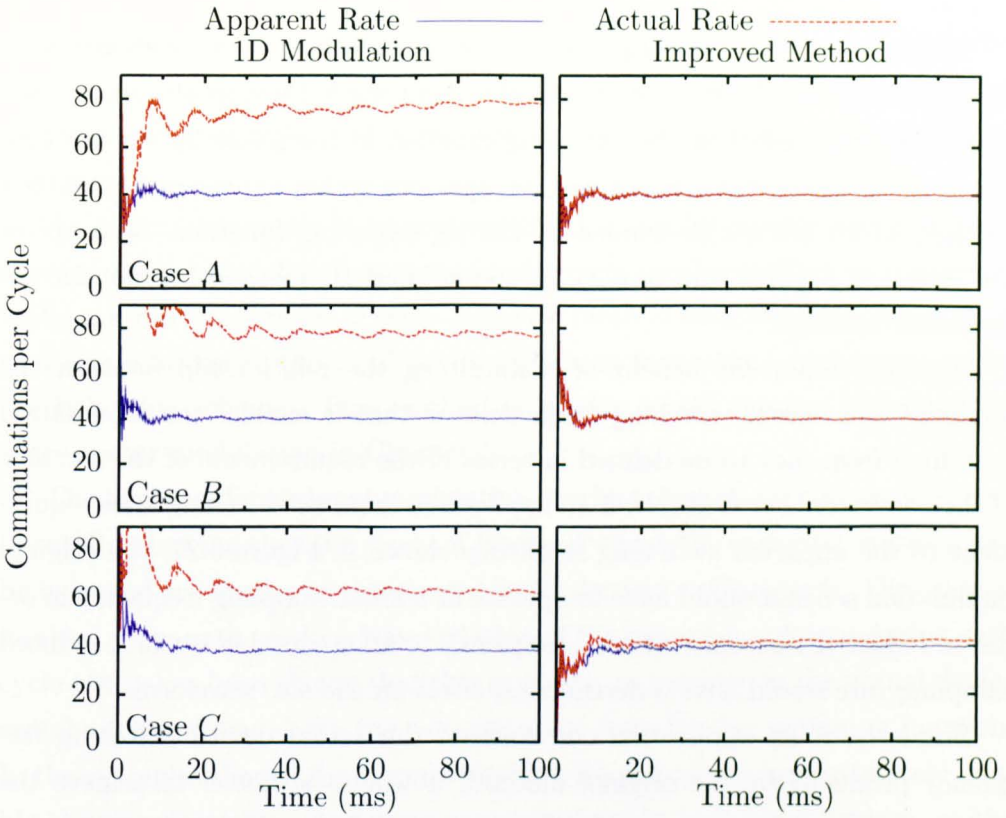


Figure 6.27: Cumulative average switching rate for one-dimensional modulation and the improved method

The apparent balancing performance of the original method comes, however, at the expense of device switching frequency, as shown in Figure 6.27 which compares the apparent and actual switching frequencies of each method. The apparent switching frequency is derived from the switching function of the phase-leg, s_a, whereas the actual device switching frequency is derived from the switching functions of the individual bridges. The original one-dimensional modulation method produces an actual device switching frequency approximately double the apparent switching frequency but the improved method maintains a close relationship between the two metrics. It is only when the capacitor voltages become unbalanced in Case C that new method exhibits a difference between the apparent and actual switching frequency. Even then, the difference is less than for the original method.

Differences between the apparent and actual switching frequencies are caused by simultaneous commutation of two cells operating in the opposite sense, such that no step is visible in the switching function of the phase leg. If the timing of the commutations is not precise, spurious spikes appear on the output voltage, which are not demanded by the leg switching function. Such spikes are visible in Figures 6.23 to 6.25 for the original 1D method but not for the improved method.

Another important benefit of maintaining the relationship between the apparent and actual switching frequencies is that it enables the modulation switching frequency to be defined in terms of the requirements of the a.c. side of the converter. For example, if an application requires switching losses equivalent to the apparent switching frequency shown in Figure 6.27, the original modulation scheme would have to operate at a lower sampling frequency in order to reduce the actual switching frequency to an acceptable level. A reduced sampling rate would have a detrimental effect on the a.c. waveforms.

Similarly, if an application can tolerate the actual device switching frequency produced by the original method, it would be better to achieve the higher switching frequency using the new method at a higher sampling frequency. For example, the actual device switching frequency of the one-dimensional method in Figure 6.27 is approximately double the apparent switching frequency. If this switching rate is acceptable to the application, a similar switching rate could be achieved using the new method with double the sampling rate, which would improve both the a.c. waveform and the balancing performance.

Hence, by assigning single commutations to single bridges, optimal use is made of the available switching frequency for both the a.c. and d.c. sides of the converter.

6.5 Summary

This chapter has discussed the relationship between one-dimensional, feedforward modulation and regularly-sampled, level-shifted carrier modulation and has demonstrated that the two modulation methods can produce the same a.c. waveforms when the capacitor voltages are equal. The one-dimensional

algorithm has been simplified so that it can be applied to a three-cell converter but it has been shown that the implementation becomes increasingly complex as the number of cells, and hence the number of possible switching states, increases.

An alternative means to choose switching states for one-dimensional, feed-forward modulation has been presented which can be applied to converters with an arbitrary number of cells. The new method assigns each commutation to a single bridge so the total device switching frequency is not increased by the balancing scheme. This method is similar to the method described for space-vector modulation in Chapter 5.

The two one-dimensional modulation methods have been compared experimentally, showing that the range of loads for which the capacitor voltages can be balanced are similar to the general limits derived in Chapter 5. The original method appears to produce less deviation of the capacitor voltages during each cycle but it has been shown that this is due to an increase in the actual device switching frequency above the rate apparent from the leg switching function. In the examples shown, the actual switching frequency was approximately double the apparent rate. Assigning commutations to individual bridges, as the new method does, allows optimal use of the available switching frequency for both the a.c. and d.c. sides of the converter.

Chapter 7

Conclusions

This thesis has covered modulation of the cascaded H-bridge multi-level converter using two modulation methods: space-vector modulation and one-dimensional modulation. Both of these modulation techniques are usually considered to be to be high-frequency PWM methods but, because of the need to reduce switching losses as the power level increases, the modulation techniques have been studied at a lower sampling frequency than is conventional.

This concluding chapter contains an overview of the work from earlier chapters and is intended to highlight the key conclusions that can be drawn. After discussing the two modulation methods individually, they are compared and contrasted and common themes identified in section 7.3. Finally, in section 7.4, opportunities for further work are identified.

7.1 Space-Vector Modulation

7.1.1 Ideal DC Links

In Chapter 4, space-vector modulation was discussed under the assumption that the d.c. links are supplied by constant and equal d.c. voltage sources. This assumption allowed fundamental properties of the modulation to be studied.

The first key observation is that when space-vector modulation is operated at low sampling frequency, adjacent samples of the reference vector do not occupy the same triangle on the space-vector diagram. Therefore it was iden-

tified that, even when consecutive samples do not occupy the same triangle, the sequences of states applied during the switching periods should alternate between starting on the upper and lower redundant state of the starting vector. For the special case where two consecutive vectors do fall in the same triangle, this rule provides the same result as the oft-quoted requirement that every other sample should be re-produced with the reverse sequence of states to its predecessor.

Using this modulation as the underlying algorithm, it was observed empirically that, for synchronized modulation, small changes in phase between the reference and the sampling process influence the harmonic distortion of the line voltages. A method was proposed to align the initial sampling angle to a locus of low distortion for varying modulation index and the approach was shown to be effective at reducing the distortion of the line voltages of both the simulated and experimental converters. Although the specific relationship between initial angle and modulation index applies only to a seven-level converter at a specific sampling rate, the principle applies equally to converters with a greater number of cells.

7.1.2 Non-Ideal DC Links

Having established the underlying space-vector algorithm, Chapter 5 discussed space-vector modulation for converters where the d.c.-link voltages are allowed to vary. The discussion handled two key problems:

- mechanisms to keep the capacitor voltages equal and
- compensation for ripple of the capacitor voltages.

Balancing of the Capacitor Voltages

The balancing problem was analysed on a single-phase basis with different resistive loads applied to the d.c. links of each cell. Such analysis is of benefit to applications such as the UNIFLEX-PM project, where the different bridges in the converter are intended to be used flexibly for different purposes.

The general limitations of balancing algorithms were derived, showing that the degree of load imbalance for which it is possible to balance the capacitor voltages depends on the modulation index of the converter. When the converter draws real power, the limiting condition is caused by the saturation of the modulation index of a single cell. A high converter modulation index reduces the freedom to change the modulation index of the cells before a single cell saturates.

A balancing algorithm applicable to space-vector modulation was also proposed and shown to operate correctly within the derived limits. The fundamental requirement of the balancing algorithm was that it must not increase the switching frequency and hence must not introduce commutations in addition to those demanded by the primary modulator. Therefore, instead of considering the effect of each redundant state, the balancing algorithm was derived considering the effect of each commutation and assigning demanded commutations to the most appropriate bridge. The response of this algorithm to imbalanced loads is to re-distribute the switching edges of the converter between different cells, causing different cells to operate at different switching frequencies. Although the limitations of the proposed algorithm were shown to be comparable to theory using simulated and experimental results, it is likely that the limits of a full-scale converter would be defined by thermal considerations due to the redistribution of switching edges, rather than the limits of modulation index.

Capacitor Voltage Ripple

The balancing algorithm cannot eliminate ripple caused by the single-phase nature of the phase legs so the effect of capacitor voltage ripple on the space-vector diagram was examined. The distortion of the space-vector diagram was then used to derive the influence of ripple on the spectrum of the line voltages. In particular, second and fourth harmonic ripple on the capacitor voltages cause fifth and seventh harmonics of the line voltages respectively.

The distortion of the space-vector diagram was also used to derive a simple feed-forward compensation scheme to improve the quality of the output

waveforms. The feed-forward method was shown experimentally to reduce the magnitude of the fifth harmonic caused by the capacitor voltage ripple.

7.2 One-Dimensional Modulation

In Chapter 6, one-dimensional modulation was discussed and shown to be closely related to regularly sampled, level-shifted carrier modulation. When the capacitor voltages are equal the methods can be made to produce identical output waveforms.

Issues of implementation were discussed as the number of bridges, and therefore the number of redundant states, is increased. In particular, it was identified that the original balancing method causes a significant increase in the device switching frequency.

A new implementation was proposed with the combined benefits of being easily applicable to an N-cell converter and of balancing the capacitor voltages without increasing the total device switching frequency. The balancing method was derived by applying commutations to specific bridges in exactly the same way as for the space-vector modulation algorithm.

7.3 Comparison of the Modulation Schemes

The modulation schemes discussed have two clear common themes:

- both methods are feed-forward modulation schemes that compensate for the capacitor voltage ripple and
- both methods balance the capacitor voltages by assigning single commutations to the most appropriate bridge without increasing the total device switching frequency.

The advantage of the balancing algorithm used in this thesis is that the balancing process does not influence the a.c. waveforms even when the loads on each cell are not equal. This is in contrast to balancing methods that modulate the cells individually where adjusting the power flow alters the shape of the

a.c. waveform and influences the cancellation of harmonics between the cells. However, the control action for the balancing methods used in this thesis is the distribution of switching edges between the cells. Hence, if the loads are not equal neither are the switching frequencies of the cells, potentially affecting the time before one cell fails. As alluded to above, it is likely that the degree of imbalanced load that a full-scale converter can tolerate would be defined in terms of the acceptable imbalance of switching frequency rather than the absolute limits derived in this thesis.

A key difference between the space-vector and one-dimensional modulation methods presented is the order of the choice of switching state and the calculation of duty cycles. The space-vector modulation method calculates the required duty cycles before invoking the balancing algorithm and only considers the average ripple on each phase leg. In contrast, the one-dimensional modulation method explicitly considers the measured capacitor voltages and calculates the duty cycles after the final choice of switching states has been derived. Hence one-dimensional modulation should produce superior output waveforms under conditions where the capacitor voltages are not balanced.

7.4 Further Work

There is scope for further work deriving from many areas of this thesis. Some areas of particular interest are outlined below.

Capacitor Voltage Ripple The effect of ripple has only been derived for the simple case where the ripple frequency is synchronized to the converter output frequency. Where two asynchronous a.c. systems are interfaced, for instance when the converter is acting as variable-speed drive, there are components of ripple synchronized to the frequency of both a.c. systems. The methodology used to analyse the simple case should be extended to investigate the influence of the more complex case and the effectiveness of the feed-forward schemes should be investigated.

Balancing Under Different a.c. Loading Conditions The limitations of the balancing algorithm were derived based on changing the loads on

the d.c. side of the converter but only for situations where the phase difference between the current and the converter output is small. If there is a significant phase shift between the voltage and the current the phase of the individual cells becomes as important a controlling factor as the modulation index, which should be taken into account in the limiting analysis.

Balancing behaviour with more cells One of the advantages of cascaded multi-level converters is the ability to connect to high voltage systems without step-up transformers if enough cells are connected in series. The algorithms used in this thesis have all been deliberately general in their implementation so they can easily be applied to converters with a greater number of levels but the behaviour of such converters has not been investigated. As an example, the problem of capacitor voltage balancing is likely to be more complex when there are more than three cells to balance.

Thorough Comparison with Carrier-Based Modulation Finally, it would be beneficial to perform a thorough and systematic comparison of space-vector modulation and carrier-based modulation to properly assess the pros and cons of each. An interesting aspect of such a study would be to look more closely at the mechanism causing the relationship between the phase of the reference and the harmonic distortion identified empirically in Chapter 4. Another aspect would be to investigate the effects of sampling the highly discontinuous reference waveform required to mimic multi-level space-vector modulation using carrier methods and whether aliasing of this complicated reference contributes to the low-order harmonics of the modulated waveforms.

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Appendix A

Cancellation of terms in the line-voltage spectrum

In Chapter 5, an equation was derived for the spectrum of the line voltage in terms of capacitor voltage ripple (see (5.23a) on page 171). Equation (5.23a) was then simplified assuming that all even harmonics and harmonics whose order is a multiple of three have zero magnitude. These assumptions are proved in this appendix.

Equations (A.1) is a re-statement of (5.23a).

$$\langle v_g \rangle = \frac{\hat{s}}{2} \sum_{k=-\infty}^{\infty} \sum_{m=\pm 1} C_{k-m} \left(1 - e^{jk\frac{2\pi}{3}}\right) e^{jk\theta} + \frac{\sqrt{3}\hat{s}}{8\pi} \sum_{k=-\infty}^{\infty} \sum_{m=\pm 1} \sum_{\substack{n=-\infty \\ n \neq k-m}}^{\infty} \frac{C_n(1+(-1)^{n+m-k})}{n+m-k} \left(1 - e^{-jn\frac{2\pi}{3}}\right) m\Psi e^{jk\theta} \quad \text{(A.1a)}$$

where

$$\Psi = e^{j(n-k)\frac{2\pi}{3}} - e^{j(n-k)\frac{\pi}{3}} + 1. \quad \text{(A.1b)}$$

A.1 Cancellation of Even-Order Harmonics

The cancellation of even harmonics relies, in part, on the capacitor voltage ripple containing only harmonic components at even multiples of the output

frequency, hence C_n is zero for odd values of n. It is also important to observe that m in (A.1) only takes the values ± 1 so is always odd.

Even harmonics of $\langle v_g \rangle$ are the components of (A.1) contributed by even values of k in the summations. Hence, the first term of (A.1) is zero for even harmonics because $k - m$ is odd for even values of k, making C_{k-m} zero.

The second term of (A.1) is also zero for even values of k. This can be deduced with reference to the following observation:

$$C_n(1 + (-1)^{n+m-k}) = \begin{cases} 0 & \text{for odd } n \text{ and} \\ & \text{for odd } n + m - k \\ 2C_n & \text{otherwise.} \end{cases} \tag{A.2}$$

Hence (A.2) is non-zero only when both n and $n+m-k$ are even. For $n+m-k$ to be even with even n and odd m, k must be odd. Hence (A.2), and therefore the second term in (A.1), is zero for even values of k.

Thus, both terms of (A.1) are zero for even value of k and so $\langle v_g \rangle$ contain no even harmonics and the line voltages maintain the property of half-wave symmetry.

A.2 Cancellation of Third-Order Harmonics

It is clear that the first term of (A.1) is zero for harmonics whose order is a multiple of three because the $(1 - e^{jk\frac{2\pi}{3}})$ term is zero for such values of k. Cancellation of the second term requires analysis of the various components for different values of n and k.

Firstly, note the values of n for which it is clear that (A.1) is zero:

1. Odd values because of the C_n term.

2. Multiples of three because of the $(1 - e^{-jn\frac{2\pi}{3}})$ term.

The remaining values of n belong to the following set of integers:

$$n \in \{6l + 3 \pm 1 | l \in \mathbb{Z}\} \tag{A.3}$$

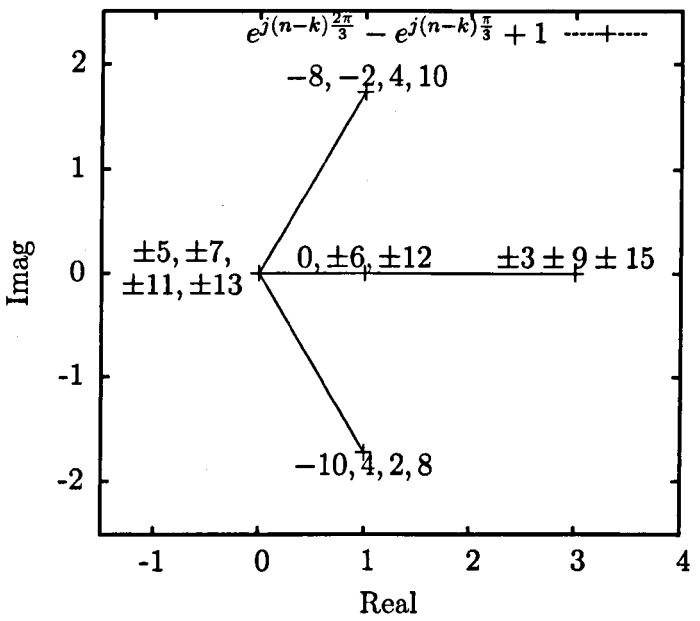

Figure A.1: Complex values of Ψ for $(n-k)$ in the range $[-15:15]$. Labels indicate values of $(n-k)$ at each point.

It has already been established that both terms of (A.1) are zero for even values of k so, for the remaining odd values of k that are also multiples of three:

$$k \in \{6l+3 | l \in \mathbb{Z}\}$$

Ψ is defined in terms of $n-k$, so for n and k in the sets defined above:

$$(n-k) \in \{6l \pm 1 | l \in \mathbb{Z}\}.$$

For example, this set includes the following integer values:

$$\{\pm 1, \pm 5, \pm 7, \pm 11, \pm 13...\}$$

Figure A.1 shows the value of Ψ for all values of $n-k$. In particular Ψ is zero for the values of $n-k$ given above. Hence both terms of (A.1) are zero when k is a multiple of three.

Appendix B

Comparison of Carrier and Space-Vector Modulation in the Time Domain

Section 4.4 includes comparisons of several frequency spectra of natural sampling, regular sampling and space vector modulation (page 115). The following figures are the time-domain representations of these modulation schemes with the same parameters.

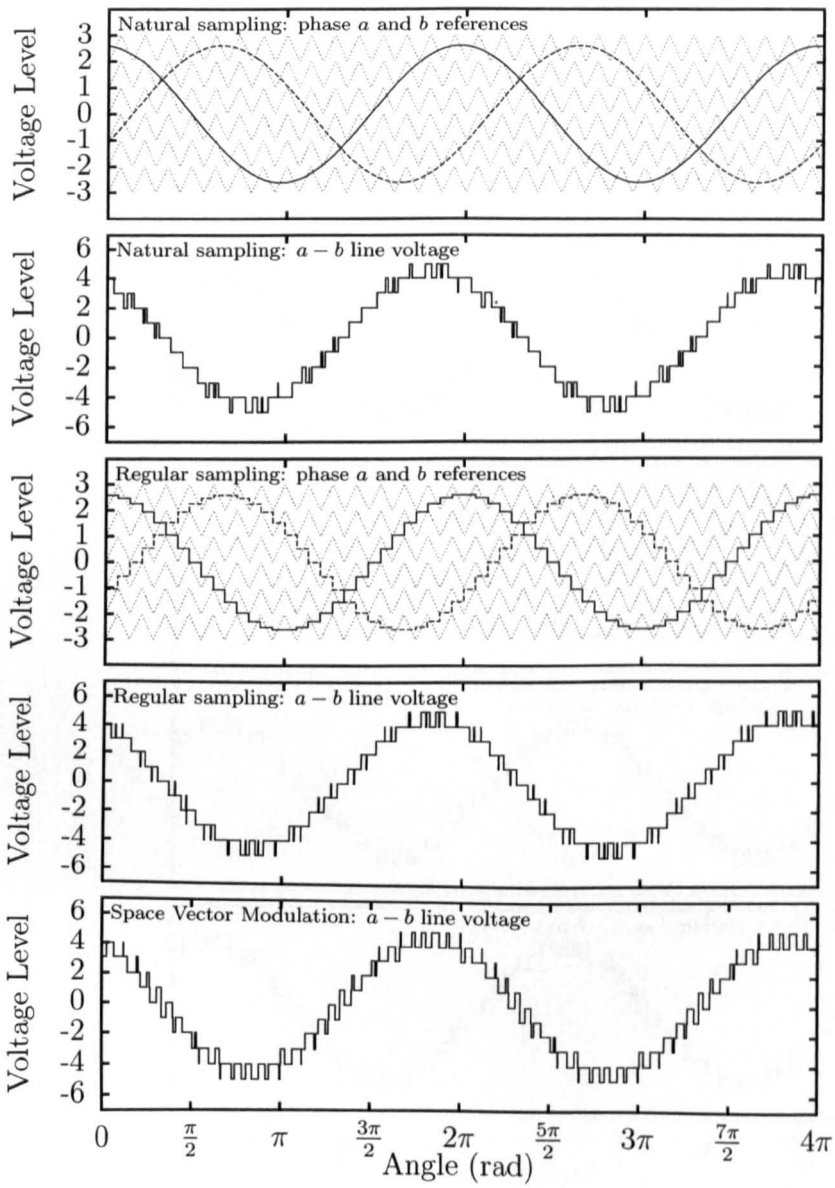

Figure B.1: Comparison of modulation schemes $\hat{s} = 2.6$, $\theta_0 = 6$

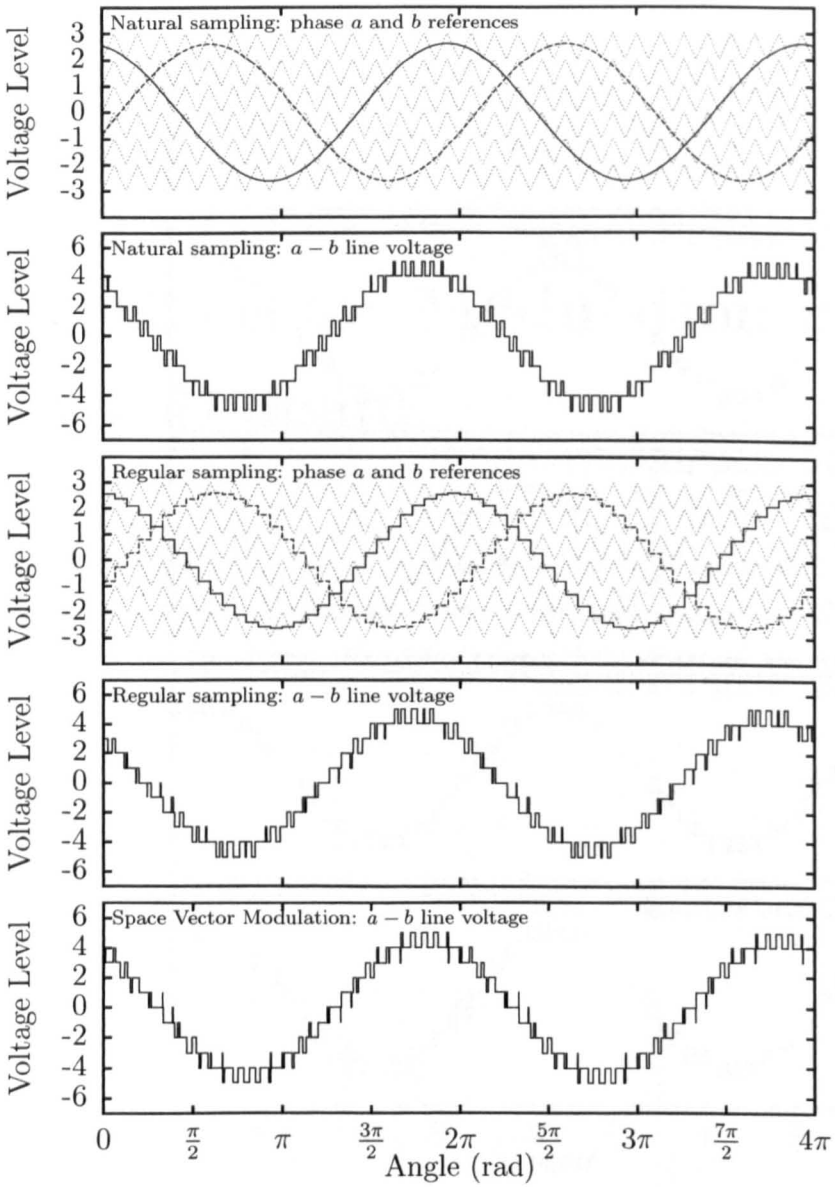

Figure B.2: Comparison of modulation schemes $\hat{s} = 2.6$, $\theta_0 = 12$

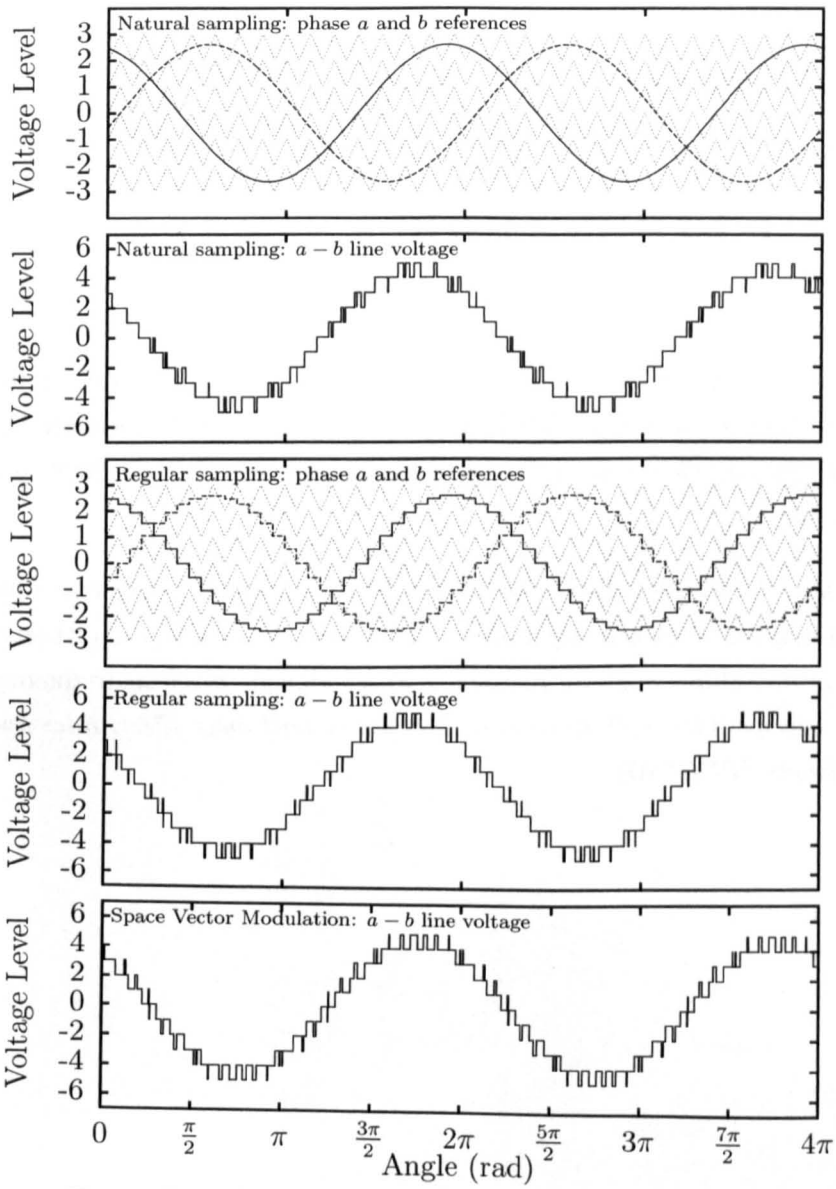

Figure B.3: Comparison of modulation schemes $\hat{s} = 2.6$, $\theta_0 = 18$

Appendix C

List of Publications

J. Vodden, P. Wheeler and J. Clare, "DC link balancing and ripple compensation for a cascaded-H-bridge using space vector modulation," in *IEEE Energy Conversion Congress and Exposition ECCE*, 2009, pp. 3093–3099

J. Vodden, P. Wheeler, L.G. Franquelo, J.I. Leon and S. Vazquez, "One dimensional feed-forward modulation of a cascaded H-bridge multi-level converter including capacitor balancing with reduced switching frequency" in *Proceedings of the 14th European Conference on Power Electronics and Applications (EPE)* 2011