CONTROL OF A STATCOM WITH SUPERCAPACITOR ENERGY STORAGE

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To my dear parents and my brother, for their love and support to my study.

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Abstract

STATCOM (STATic COMpensator) has been used in electrical power systems as a shunt-connected compensator for voltage support and to improve power quality. Compared with the conventional compensators such as the synchronous condenser and the SVC (Static Var Compensator), the STATCOM has a faster speed of response to deal with dynamic and transient impacts. Although the STATCOM is capable of reactive power support to improve power quality, the ability to support real power is limited due to the insufficient energy storage capability of the conventional DC-link capacitor. Therefore, the application of the STATCOM to improving power system stability has been limited.

This thesis proposes a solution to enhance the performance of the STATCOM by adding supercapacitor energy storage to the DC-link of the conventional STATCOM. With the fast charge/discharge characteristics of the supercapacitors, the enhanced STATCOM can absorb and inject real power to the ac power grid virtually instantaneously. The control design of the STATCOM based on a vector control strategy is presented, including the design of an instantaneous reactive power controller based on a small-signal model of the ac power system. The control design of the supercapacitor energy storage system (SCESS) based on small-signal models of the dc-to-dc converter is documented. The STATCOM and the SCESS are controlled together using a feed-forward control technique. In addition, this thesis also proposes that the enhanced STATCOM can be applied to reduce instability and tripping due to the rate of change of frequency (ROCOF) protection devices caused by large load impacts. The amount of the energy required for the enhanced STATCOM to maintain the stability of the system is also discussed.

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Chapter 1

Power system shunt-connected compensators

1.1 Introduction

The main constituent components of ac power systems are generators, transmission and distribution lines, and loads. The generators are rotating synchronous machines which converts mechanical power into usable electricity. The transmission and distribution lines are the electrical medium used to transport electricity from the generation sites to the load centres. The loads are components or equipment that consume energy. Both real and reactive power have to be supplied to loads. The operation of ac power systems is based on the fundamentals that 1) all the generators connected to the network must run in synchronism with each others in such a way that the corresponding frequency remains constant or varies within an acceptable

range and 2) the voltage levels at all buses should be kept constant or close to the ratings.

In transmission and distribution systems, the lines are characterised dominantly by the distributed reactance (series inductance and shunt capacitance), and the transmitted real power is generally associated with reactive power. Thus, when loading, the voltage profile along the line will differ from the desired level which may cause a large magnitude variation at the load buses and eventually lead to power quality problems and possible voltage instability. Undervoltage will cause low performance of the associated loads, while overvoltage will be the cause of equipment failure due to insulation breakdown. In addition, transient events such as faults, line and load switching, and other disturbances can cause a sudden change of the real power demand in the system. The sudden change of real power causes a generator or a group of generators to accelerate and others to decelerate away from their steady state speed resulting in a variation of the system frequency, and power oscillation. This may lead to the loss of synchronism and even in the separation of some components which can cause cascade failure of the system. Therefore the control of power flow is necessary and has been a priority since the early age of ac power systems in order to maintain good power quality and system stability.

It is clear that transient events always occur in ac power systems although the system operator will have taken every reasonable precaution to reduce the number of them including the improvement of the robustness of the loads. Therefore one of the solutions to limit the effects of the transients is to apply some form of the mitigation device such as a compensator.

In the past, transmission and distribution systems were designed with large stability margins. Permanently connected reactance and mechanically switched shunt capacitors (MSC) and reactors (MSR) have been used to ensure that the voltage profile along the transmission and distribution lines is

within the prescribed range. Although both MSC and MSR can be used for loads that vary from hour to hour as a daily variation, the operation of the MSC and the MSR cannot handle fast changes in the reactive power demand. Instead, synchronous condensers (rotating synchronous machines without a prime mover and turbine) were installed to handle the fast changes in reactive power demand, and to minimise power oscillations.

A power system can be interconnected for economic and environmental reasons - avoiding the construction of both new generation and transmission facilities, and for higher utilisation of the existing power systems. Basically the interconnected system provides an increase in stability limits, as more real and reactive power are available than in the separate power system. However to utilise the extra supply available for stability improvement, the control of power has to be rapid. Advances in the recent development of high power semiconductors and power electronic technology have made possible the development of fast compensators, without mechanical movement, for application in power systems. These provide a significant improvement compared to the classical forms of stability improvement such as MSC and MSR.

The aim of this project was to develop a new, fast power electronics based on compensation device capable of compensating quickly for both real and reactive power changes. The device includes supercapacitors as energy storage devices. Before describing the specific aims and objectives of this project, a brief review of existing compensation technology now follows.

1.2 Static VAr Compensators (SVCs)

Due to the slow response time of the mechanically switched reactor and capacitor shunt compensator, they are not suitable for use as dynamic compensation equipment in ac power systems where a transient event can be

severe. Their behaviour results in a steplike output and this is another reason why mechanically switched compensators are not preferable for dynamic compensation.

An SVC operates with the same principle of the MSC and MSR. It generates and absorbs reactive power, but the precise control of the firing angle of a thyristor switch gives the SVC the ability to provide reactive power continuously and sufficient speed of response to handle fast changes. Therefore an SVC can maintain a smooth voltage profile and improve the system stability under various conditions [1].

One of the first static VAr compensators was commercially installed for an electric arc furnace compensation in 1972 [1]. For the transmission level, the EPRI funded SVC project was installed in 1978 at the Shanon substation of the Minnesota Power and Light system [2]. In general the SVC can be a combination of a Thyristor Switched Reactor (TSR), a Thyristor Controlled Capacitor (TSR), and a Fixed Capacitor (FC) as shown in Figure 1-1 [1-4]. With the appropriate control coordination of that equipment, the combination can vary the reactive power to meet the required value.

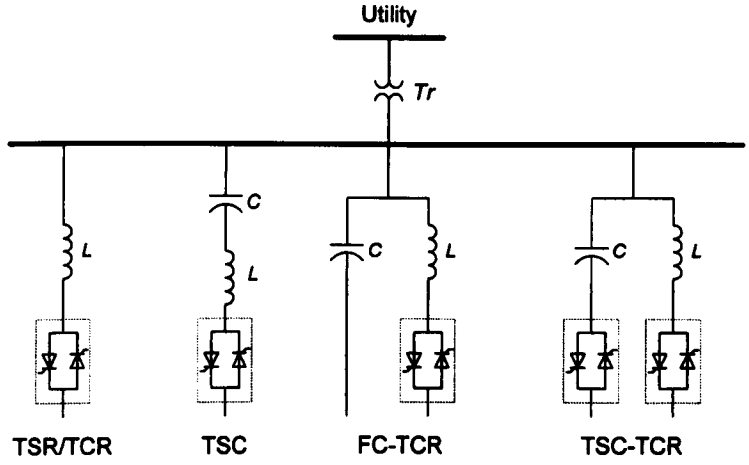

Figure 1-1 Static VAr Compensators (SVCs)

1.2.1 Thyristor Controlled Reactor (TCR)

A single-phase thyristor controlled reactor (TCR) consists of a linear reactance of inductance L connected in series with a bidirectional thyristor (a pair of inverse-parallel connected thyristors) as shown in Figure 1-1. The thyristors are made up of high power rating thyristors connected in series in order to gain higher total voltage and current ratings suitable for ac power system applications. In practice three sets of single phase TCRs are usually connected together in delta configuration in order to prevent the triplen harmonic currents i.e. third, ninth, fifteenth produced from the TCRs entering the power systems. The triplen harmonic currents will circulate in the delta configuration.

Reactive power compensation can be obtained and controlled from the minimum value (zero) to the maximum value by controlling the firing angle delay with respect to the applied voltage. A 90 degree firing angle is applied with respect to the ac bus voltage zero crossing to obtain full conduction of the thyristors (the valve is closed); while a 180 degree firing angle will result in no conduction (the valve is open). Unless the firing signals are applied repeatedly, the thyristors will automatically block (turned off) immediately after the current crosses zero [2, 3].

A single-phase thyristor switched reactor (TSR) has its physical arrangement similar to the mentioned TCR, but it is controlled by the firing angle delay at 90 and 180 degree only i.e. at maximum and minimum conduction or open and closed, thus the TSR will not generate harmonics, however with its on-off control operation its application is limited [3].

1.2.2 Thyristor Switched Capacitor (TSC)

A single-phase thyristor switched capacitor (TSC) is shown in Figure 1-1. It is comprised of a capacitor C, a bidirectional thyristor switch, and a relatively small surge reactor L all connected in series. The small reactor is included in the TSC for the purpose of limiting the magnitude of the inrush current under the worst case occasionally caused by severe transients such as when the uncharged TSC capacitor is initially energized. Without this reactor the inrush current may reach beyond the withstand rating of the thyristor. This reactor is also used to prevent the thyristor from severe damage due to the high surge current under abnormal operating conditions. It may be designed to avoid resonances of TSC with the system impedance [2]. A three-phase TSC application is also performed by three sets of the single-phase components connected in delta the same as for the configuration for the TCR/TSR.

However, unlike the TCR/TSR where the current through and the voltage across the reactor will automatically cease after the thyristor is turned off, the voltage across TSC capacitor will be at its peak value when the TSC branch current reaches zero. The capacitor voltage then remains charged at peak value. As a consequence, a double voltage stress appears on the nonconducting thyristor and it is necessary to increase the number of series thyristors in a valve string. Therefore the number of thyristors used is twice the number used for the TCR/TSR. Turning on the TSC branch should be made while the voltage across the thyristor valve is zero, when the applied voltage is equal to the capacitor residual voltage i.e. when $dv/dt = 0$ at peak value of the applied voltage to avoid any severe transients.

The gating causes the thyristor valve to conduct for a half cycle period. Therefore the TSC can not provide the capacitance continuously but in a discrete or step pattern.

1.2.3 Fixed Capacitor-Thyristor Controlled Reactor (FC-TCR)

A Fixed Capacitor-Thyristor Controlled Reactor (FC-TCR) is a combination of a permanently connected shunt capacitor or fixed capacitor and a TCR. A basic circuit for the FC-TCR is shown in Figure 1-1. The fixed capacitor provides a constant leading VAr. Some of this is cancelled by the variable lagging VAr of the TCR, resulting in a fully controlled and smooth compensation.

The operation of FC-TCR is dominated by the controlling of the TCR as explained in section 1.2.1. In principle the disadvantage of this SVC is the losses they produce; even at zero VAr output, standby losses exist. Because their operation is based on the cancellation of the current through both the fixed capacitor and the TCR, at zero VAr output, some current flows through the TCR to cancel the fixed capacitance and this generates loss. The overall losses increase with the TCR current, but conversely decrease with capacitive VAr output. It is good for industrial applications where high capacitive VAr is required for power factor correction, but has poor dynamic compensation which may be a disadvantage for transmission systems [2].

1.2.4 Thyristor Switched Capacitor-Thyristor Controlled Reactor (TSC-TCR)

The basic concept of a combined Thyristor Switched Capacitor-Thyristor Controlled Reactor (TSC-TCR) is indicated in Figure 1-1. In practice there may be many paralleled TSC branches in order to provide the coarse steps of capacitive VAr, and one large TCR to adjust a fine continuous control VAr in between them.

It was mainly developed with the intention to minimise the standby losses and for dynamic compensation. The basic principle operation is that the TSC branches will be switched in to provide compensation slightly (i.e typically above 5%) above the VAr required value, and then TCR will absorb the surplus VAr to get the precise output VAr. At zero VAr output the TSC branches will be switched out and no TCR is required to cancel the fixed VAr. Therefore the loss at the standby point is zero or nearly zero. At other operating points, the losses will vary depending on the surplus capacitive VAr [2, 3].

1.3 STATic COMpensator (STATCOM)

In the previous sections, reactive power generated by means of SVC is based on using thyristors as control elements to vary the reactive power produced by passive power components, the capacitor and reactor banks. However the recent developments in the field of high power, power electronic devices has demonstrated the use of static VAr generator which is not based on capacitor and reactor banks. Only a small DC-link capacitor is used, but the device can provide both capacitive and inductive VAr. Therefore it may be possible to improve the size and cost of the static VAr generator in the future [2].

A recently developed VAr generator is called STATic COMpensator (STATCOM). In principle, the operation of the STATCOM is comparable to a synchronous condenser. A simplified circuit arrangement of both the synchronous condenser and the STATCOM is shown in Figure 1-2 [1, 3].

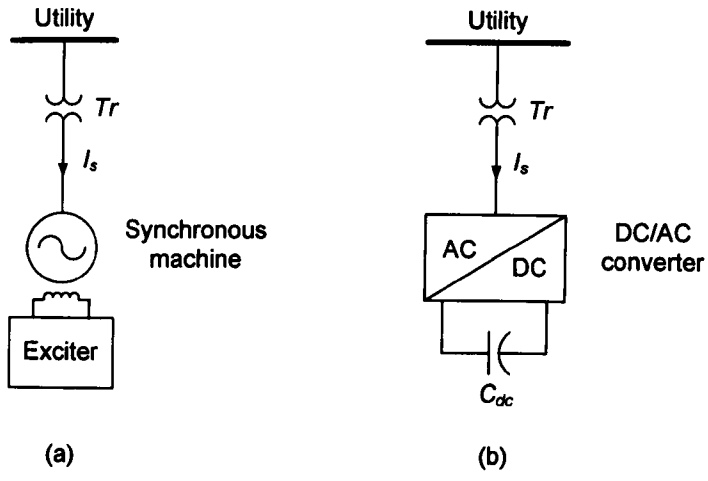

Figure 1-2 The simplified representation of (a) a synchronous condenser and (b) a STATCOM

The synchronous condenser shown in Figure 1-2 (a) consists of a rotating synchronous machine with its excitation system, and a transformer 'Tr' to adapt the voltage to the utility level at the point of common coupling, V_{pcc} (if required). The relationship of the synchronous condenser voltage and current during inductive and capacitive generation is shown in Figure 1-3.

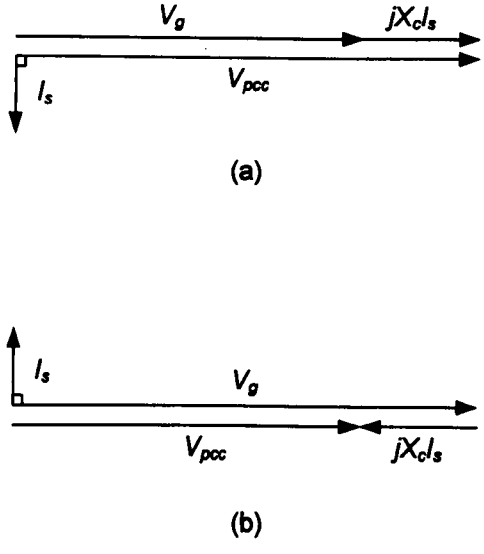

Figure 1-3 The simplified representation of a synchronous condenser voltage and current when operated as (a) inductive VAr generator, and (b) capacitive VAr generator

Where

V_g is the voltage generated by the synchronous condenser, V.

V_{pcc} is the voltage at utility bus at the point of common coupling, V.

I_s is the support current flowing between the utility bus and VAr generator, A.

X_c is the equivalent reactance of a coupling reactor and transformer, Ω.

In Figure 1-3 (a) when the synchronous condenser is underexcited, it generates a voltage V_g which is in-phase with the utility voltage V_{pcc} but with a magnitude lower than that of V_{pcc}. The resulting voltage drop across the equivalent reactance jX_cI_s gives a 90 degree lagging current I_s (with respected to the utility voltage). This example indicates that the synchronous condenser is operating in inductive VAr mode or is absorbing VAr from the V_{pcc} bus. On the other hand, Figure 1-3 (b) shows that the synchronous condenser is operating in capacitive VAr mode or is injecting VAr into V_{pcc} bus when the synchronous condenser is overexcited. The voltage V_g is raised to a level higher than that of utility voltage V_{pcc} (still in-phase with V_{pcc}) and the voltage drop across the equivalent reactance results in a 90 degree leading current I_s.

The operating principle of the synchronous condenser depends on the current flow through the equivalent reactance which is governed by the basic relationship as in Equations (1-1), (1-2) and (1-3)[5, 6].

$$I_S = \frac{V_g - V_{pcc}}{jX_c} \tag{1-1}$$

$$P = \left(\frac{V_g - V_{pcc}}{X_c}\right) \sin\delta \tag{1-2}$$

$$Q = \left(\frac{V_g V_{pcc}}{X_c}\right) \cos\delta - \left(\frac{V_{pcc}^2}{X_c}\right) \tag{1-3}$$

Where

P is the real power flows between the generated voltage and utility bus, W.

Q is the reactive power flows between the generated voltage and utility bus, VAr.

δ is the phase displacement angle between the generated voltage and utility voltage, degree.

In practice as the synchronous condenser is not driven by a mechanical input power from a prime mover, its overall losses are then supplied by the system utility. As a result, the generated voltages will not be in-phase ideally with utility voltage, but lags slightly by an angle δ which can be derived from Equation (1-2). Therefore, the current I_s will not be the ideal value of 90 degrees leading or lagging. There will also be a slight variation depending on losses as illustrated in Figure 1-4.

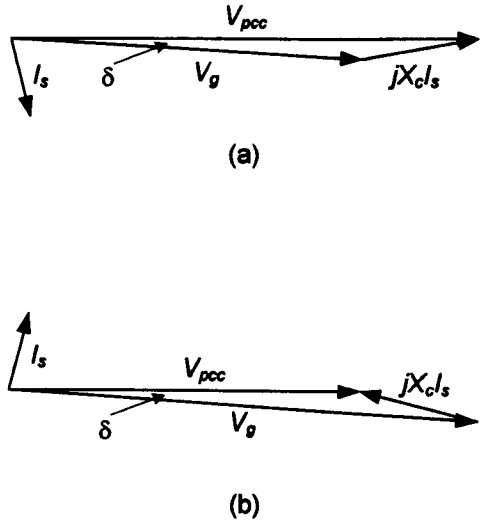

Figure 1-4 The representation of a synchronous condenser voltage and current when operated, with losses, as (a) inductive VAr generator, and (b) capacitive VAr generator

The STATCOM shown in Figure 1-2 (b), consists of a dc-to-ac voltage source converter VSC, a small DC-link capacitor C_{dc}, and a coupling reactor with a

transformer required to connect to the V_{pcc} bus. As mentioned above, the basic operating behaviour of the STATCOM resembles that of the synchronous condenser described with Figure 1-3 and Figure 1-4. If the voltage produced by the VSC is higher than the utility voltage at which it is connected to, the STATCOM operates as a capacitive VAr generator injecting reactive power to the utility. Conversely if the voltage produced is less than utility voltage, the STATCOM will absorb reactive power from the utility acting as a reactive load [2, 3, 5]. As with synchronous condenser operation, the losses of the STATCOM are usually supplied by the utility, not from the DC-link capacitor. A slight angle difference of the voltage generated by the STATCOM and utility voltage indicates the losses in the STATCOM system.

Compared to the synchronous condenser, the STATCOM has a faster response time for reactive compensation [7-11] although, apart from the way they create their voltage, their compensation principles are very similar. Furthermore, the STATCOM can be used with energy storage in order to improve the ability to increase power system stability [12]. Furthermore, unlike the rotating synchronous machine the STATCOM contributes less fault current when faults occur.

In ac power systems, there will be a significant improvement in the stability if the compensation equipment can contribute a sufficient amount of the real and reactive power to the system during short period disturbances [12, 13]. However, the ability of the standard STATCOM is limited as its operation will be actively possible for only reactive power compensation as described with Figure 1-3. The STATCOM DC-link voltage will vary massively when exchanging real power with the utility due to the limited energy storage capacity of the DC-link capacitor used. At any instance if the drop of DC-link voltage is obvious, due to the lack of energy in the dc side, the STATCOM cannot produce a sufficient output voltage, and this will cause the STATCOM to trip. Some examples of applications of the STATCOM have been reported in [11, 14-16].

To improve the STATCOM's performance, a significant amount of energy is needed in order to keep the DC-link voltage constant at the level that the STATCOM can produce the required voltage for real power compensation. A constant DC power supply would be ideal for this performance improvement, but if its primary source is the same ac supply for the ac side of the STATCOM, compensation is impossible. Adding energy storage to the DC-link capacitor is an option resulting in the STATCOM that can actively inject and absorb real and reactive power from the utility. The additional energy storage will give the STATCOM the flexibility to control the support current fully in all four quadrants as shown in Figure 1-5(b) compared to the standard STATCOM current shown in Figure 1-5 (a). This compensation with a mixed support of real and reactive power is the best solution for many cases in power systems [13].

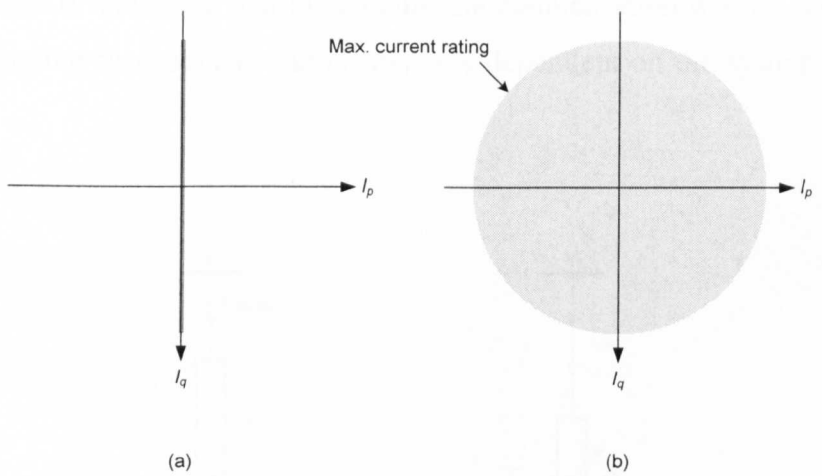

Figure 1-5 The comparison of the current controlled by the ideal (a) standard STATCOM, and (b) STATCOM with energy storage

In Figure 1-5(b) the shaded area indicates the active area for the current controlled by the STATCOM with a significant amount of energy in the dc side. Both the real power current I_p and the reactive power I_q can be controlled flexibly within the shaded area bounded by the STATCOM rating, while the standard STATCOM can control only the reactive current as shown in Figure

1-5(a). Some examples of STATCOM enhanced with energy storage can be found in the literature review in the technical research publication [17-21].

1.4 A comparison between STATCOM and SVC

The equivalent circuit of a STATCOM compared with that of a SVC is shown in Figure 1-6. The STATCOM is modelled using a variable voltage source $V_{statcom}$ connected in series with the impedance of the coupling reactor Z_c (and of the transformer) coupled to the power system voltage V_s. As a result, this circuit will operate as a current source connected to the ac power system with its capability depending on the output terminal voltage $V_{statcom}$ produced electronically [1]. In contrast, the SVC is modelled using a variable susceptance B indicating that the amount the compensation will be controlled by varying the susceptance, and clearly it is dependent on the system voltage V_s.

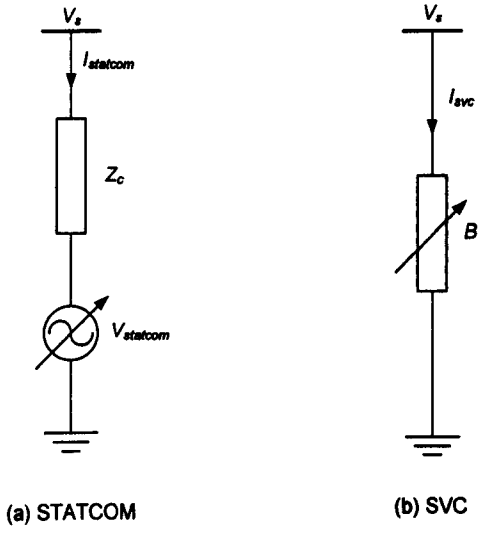

Figure 1-6 The equivalent circuit of (a) STATCOM and (b) SVC

The compensation characteristics of both the STATCOM and SVC are shown in Figure 1-7 and Figure 1-8 respectively. Typically they are required to operate with a specific slope reactance as illustrated in the figures in order to provide a linear operating region for the compensation. This slope is designed in order to prevent the severe oscillations which may occur at the limits if the compensator is designed to operate without a regulation droop (zero slope). In general, the regulation slope is in the range of 2 to 5% which allows the voltage variation of up to ±5% around the reference voltage [3, 4]. Therefore, the regulation droop of the V-I characteristic shown in Figure 1-7 and Figure 1-8 indicate that the terminal voltage will be allowed to be a value smaller than the nominal no-load value when it reaches full capacitive compensation, and also the terminal voltage will be allowed to be higher than the nominal voltage if it is at full inductive compensation.

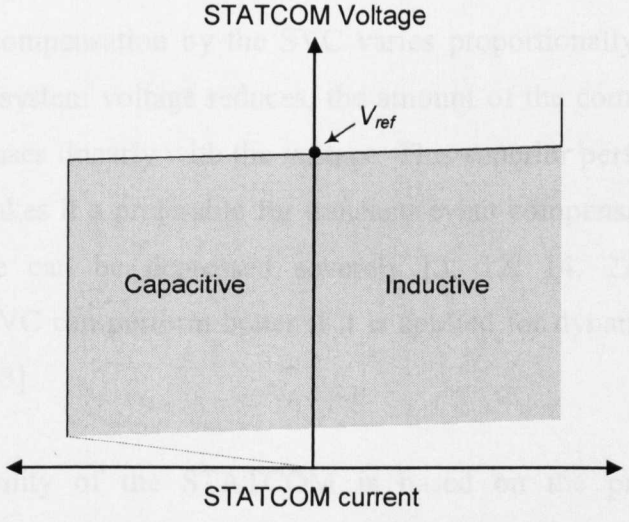

Figure 1-7 V-I characteristic of STATCOM

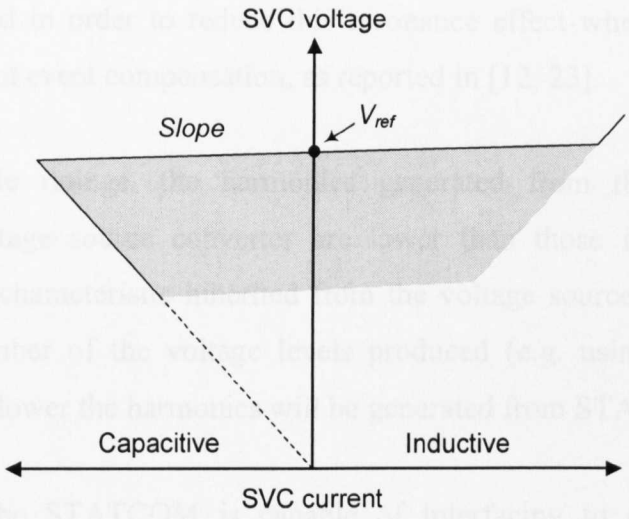

Figure 1-8 V-I characteristic of SVC

Considering both the V-I characteristics of the STATCOM and SVC, the STATCOM has a better performance. It can be seen clearly that the STATCOM can continue to operate with its rated current (as indicated by the shaded area) although the system voltage is reduced down to a very low level, while according to the characteristic of the passive elements (capacitor and inductor) the compensation by the SVC varies proportionally to the system voltage. If the system voltage reduces, the amount of the compensation from the SVC decreases linearly with the voltage. This superior performance of the STATCOM makes it a preferable for transient event compensation where the system voltage can be depressed severely [3, 12, 14, 22]. However a conventional SVC can perform better if it is applied for dynamic overvoltage compensation [3].

The controllability of the STATCOM is based on the production of a sinusoidal voltage with respect to the system voltage – both the magnitude and phase can be adjusted very rapidly (within milliseconds). For the SVC the compensation is controlled by varying the conduction period of the thyristor to adjust the susceptance of the capacitor and reactor. This may react with the system impedance to cause a severe resonance. Therefore the SVC control

speed is limited in order to reduce this resonance effect when applying the SVC to transient event compensation, as reported in [12, 23].

For comparable ratings, the harmonics generated from the STATCOM employing voltage source converter are lower than those from the SVC. Regarding the characteristic inherited from the voltage source converter, the higher the number of the voltage levels produced (e.g. using a multilevel converter), the lower the harmonics will be generated from STATCOM [12].

Furthermore, the STATCOM is capable of interfacing to energy storage devices in order to improve the performance in such a way that the compensation can be provided with a mixture of real and reactive power support, which makes it better to compensate for the transient stress as mentioned above.

1.5 Project objectives

For many cases in ac power systems, especially during transient stressed conditions the lack of real power support from system compensators may lead to the failure due to low stability margins. A STATCOM with the ability to support both reactive and real power dynamically can provide a significant improvement to the security of ac power systems, even if the real power is only supported for a short period of time.

The aim of this thesis is to investigate the use of a SuperCapacitor Energy Storage System (SCESS) to enhance the performance of a conventional STATCOM. The supercapacitor, a newly developed energy storage device, is suitable for short-period charge/discharge applications. The proposed STATCOM with SCESS will therefore offer a superior ability to compensate with a mixture of both real and reactive power that can be useful for the short-period stressed conditions in ac power systems. Simulation work will be

carried out to demonstrate the benefits to an ac power system using the STATCOM, and using the STATCOM plus SCESS, within a specific system scenario to support the proposed idea. Finally, experimental tests will be carried out to validate the proposed control technique. The main objectives of this project can be summarised as below:-

I. To investigate the use of the enhanced STATCOM with energy storage for improving the stability within the system with distributed generation (DG).

II. To determine the circuit configuration and control methods required for creating a STATCOM plus SCESS.

III. To investigate the SuperCapacitor Energy Storage System (SCESS) applied for enhancing the performance of the conventional STATCOM.

IV. To demonstrate the benefits of an ac power system using the enhanced STATCOM with SCESS.

1.6 Thesis overview

In order to accomplish the objectives of this project, this thesis presents the work undertaken in the following seven chapters which are briefly described below.

In chapter 2, power system improvement using the enhanced STATCOM with energy storage is described. The Distributed Generation (DG) plants are mentioned briefly. An analysis of instability within the system with DG is

discussed with mathematical support. The minimum amount of the energy required to be applied with the STATCOM is derived from the analysis, with the aim to minimise the instability caused by the rate of change of frequency (ROCOF). Simulations were carried out in order to support the idea.

In chapter 3 the details of the conventional or standard STATCOM including the operation and design are presented. The vector control strategy for the STATCOM is designed step by step including the current control, DC-link voltage control, and the external loop control design for the ac grid support is described. A simulation to demonstrate the benefits of an ac power system using the standard STATCOM that is implemented with digital controller is also explained in chapter 3.

In chapter 4 the brief review of energy storage technologies is presented in the beginning of the chapter. The SCESS and its control technique are described in greater detail including the dc-to-dc bidirectional power converter which is used as the main control device in SCESS. A simulation to demonstrate the benefits of an ac power system using the enhanced STATCOM with supercapacitor energy storage is then explained at the end of this chapter.

In chapter 5 the overall experimental setup regarding the system scenario used in the simulation work is described section by section from the major components to the supporting components. Practical circuit diagrams are explained fully with the graphical illustration and images of the hardware built for the experimental tests. The dSPACE digital controller board is also described.

In chapter 6 the experimental results are illustrated and the explanation of those results is clearly documented with each result. In order to experimentally validate the main idea of this thesis, the superior performance of the enhanced STATCOM is highlighted at the end of this chapter

Finally chapter 7 gives the conclusions of this project. Some useful suggestions for the future work that can be continued from this project are presented briefly.

Chapter 2

Power system stability improvement using STATCOM with energy storage

2.1 Introduction

The first priority for operating ac power systems is to secure the condition that the whole system can supply energy to meet the demand, even in the presence of system disturbances. An ac power system operating under this condition is generally called a stable system. The voltage magnitude and angle at each unit (bus) of the system reflects power flows from generating buses to load buses. Therefore this condition is a balance between generation and consumption. For stable systems, at the generation units the mechanical power input by the prime mover of the generator equals the electrical power consumed plus losses, transmitting to and from other buses. The stability of the ac power

system requires that the amount of the mechanical power converted is equal to the electrical power consumed.

Considering the generator in mechanical terms, this balance leads to the condition that the accelerating torque applied to the shaft of the prime mover equals the decelerating (retarding) torque caused by the electrical output of the generator. Zero net torque results if the shaft of the generator is rotating at a constant speed, generally called synchronous speed. In electrical terms, the system frequency is directly proportional to the speed of the generator. Thus, the constant speed of the rotating shaft gives the constant system frequency. Disturbances causing imbalance between the mechanical and electrical power will result in a change in the rotor speed and thus the system frequency. However if the systems are able to automatically return to the balanced condition again, they are called stable systems [6].

Recently the study of ac power systems has been concerned with embedded or distributed generation (DG) which has increasingly penetrated into the distribution networks, where generation can be located close to the consumers in order to minimise transmission losses. Although many utilities have brought the benefits of distributed generation to their systems, there are some other impacts which must be considered. In this chapter DG and its technical impacts on the system are described, and proposals are introduced to minimize these technical impacts.

2.2 Distributed generation

The aim of Distributed Generation (DG) is to provide power sources close to the demand centre i.e. DG is embedded in the distribution network. Therefore, unlike the conventional distribution network, DG provides the capability of interacting with the power system and becoming an active distribution network. DG can be classified as smaller generation (compared to the central

generation) which is embedded in or connected to distribution networks to supply the consumer demand locally, and it is not planned and dispatched centrally by the utility [24-27] .

2.2.1 DG plants

There are several types of the DG plants connected to distribution networks. According to the energy sources used to generate electricity, the DG can be categorised into two groups – the combined heat and power plant, and the renewable energy plant. The latter normally requires further compensation as it may be an intermittent primary source.

2.2.1.1 Combined heat and power plant

In general, primary energy sources such as coal, petroleum, natural gas and uranium are used to generate electricity through a thermal process. However they can not convert all of their thermal energy into electricity, and approximately half the energy (heat) is lost and emitted through the cooling systems as wasted heat.

In a combined heat and power plant (CHP), also known as cogeneration, the excess heat is captured and used locally on site or close to the site i.e. the CHP can produce electrical power and useable heat simultaneously. It is mostly implemented with a synchronous generator; however some plants may use an induction generator to generate electricity. CHP is the most significant distributed generation technology embedded in distribution networks [25].

2.2.1.2 Renewable energy plant

For renewable energy plants, unlike CHP, their siting is determined by the location of the primary renewable energy sources. Their electrical output power is also dependent on the availability of the energy source. The generator used must be operated when the primary energy is available, unless the plant is capable of energy storage.

The output of wind power plants is proportional to the wind speed, which differs depending on the locations. It is obvious that to integrate the wind power plant into an ac power network, wind turbines need to be located in areas where wind resource is available. Mostly the available positions for wind power plants are away from residential areas which can make it difficult to connect to the distribution network, and sometimes leading to a considerable amount of the investment.

For wind farm power plants, because of the fluctuation of the turbine speed according to windspeed variation, induction generators with the associated gearbox appear to have become the preferred choice due to their high reliability, robustness, and low cost and maintenance [25, 28-30]. If an adequate mechanical damping system or power electronic conversion system is included to complement the aerodynamics of the turbine, a synchronous generator can be used [21, 25, 31]. Similarly in the small and medium hydro-electric plants, induction or synchronous generators are installed for converting the flows of water to the consumable electricity dispersed within distribution networks.

In solar photovoltaic power plants, the electricity generation is not concerned with turbine generators, but is achieved using a power electronic converter. The primary output from the solar cells is dc, and a dc-to-dc converter may be

used to stabilise the output voltage. A dc-to-ac converter is therefore needed to produce the ac for the distribution network.

It is clear that the availability of the renewable energy source is not completely predictable resulting in a reduction of the reliability and stability of the system. Therefore, energy storage devices are included to store energy when the energy source is available and then supply during the peak period, or when the renewable resource is low in order to improve the quality of the system.

2.2.2 Impacts of DG on AC power system

In this section, the technical impacts of the DG on ac power systems such as power network fault level change, power network voltage change, and power quality and system stability are described briefly.

2.2.2.1 Network fault level change

DG will change the characteristics of the distribution network, turning it into an active network like the transmission network where it can reverse the flow of the power and contribute extra current to a fault [32, 33].

In planning to install DG in a system, the network fault level is one of the factors that must be considered. As almost all DG employs rotating machines as the generators, both synchronous and induction generators can contribute additional current increasing the fault level at the area near the DG installation. Furthermore, the fault level change will consequentially lead to impacts on the protection system. The protection cost will be increase if all the related protection equipment has to be uprated to match the fault level. The additional fault current due to the contribution from the DG may be reduced by inserting an appropriate impedance, reactor or transformer, as a current

limiter between the DG and the network but at the price of the increased losses and voltage change.

2.2.2.2 Network voltage change

In practice, distribution networks are traditionally arranged in the form of a radial system. Power therefore flows unidirectionally to loads. The voltage drop across the impedance along the radial line can cause a poor voltage profile, especially at the most remote bus. Installing the DG directly to the radial network is one of the benefits that can minimise the voltage variation. However the DG will cause bi-directional power flow along the radial line and then this will change the network voltage levels [25, 34, 35].

In a radial system, according to the loading condition and the impedance of each section of the radial line, the most remote load will suffer from a voltage variation. During operation at light load the voltage at the remote bus should be at a level not higher than the maximum allowed level. During full load operation this voltage should be at a level no lower than the acceptable minimum level. The additional DG installed in the system will affect the flow of the power as the DG can contribute reverse power flow in the line. Therefore for operation at light load the voltage at the remote bus may increase beyond the maximum allowed level.

As mentioned in section 2.2.2.1 that insertion of the current limiting impedance to increase the section impedance may cause a wider voltage variation at the remote bus. Therefore the voltage profile could possibly be used to indicate the maximum capacity of the DG to be installed.

2.2.2.3 Power quality

The voltage and power quality of the system can be improved by employing suitable DG. The DG will contribute reactive power in a way to improve the quality of the power consumed. However the transients caused by the DG and the nature of the DG if it relies on the renewable energy source may cause other power quality problems [24, 25]. System frequency variation is also one of the power quality problems caused by DG. The co-ordinated voltage control needs to be considered in order to improve power quality in systems with DG.

The current transients caused by the DG during connection and disconnection from the network may lead to a high magnitude transient voltage in the network. Also a significant transient voltage drop can occur when DG operating with high load is suddenly disconnected. This transient is one the causes of a phenomenon known as voltage flicker [25, 34, 36].

2.2.2.4 System stability

Depending on the circumstances, if the DG is installed in order to provide support for the system, the security of the associated DG is very important for the stability of the system. The previously mentioned impacts may be concerned with the security of the DG. For example, if a network fault occurs at F1 in Figure 2-1 which is not related to the DG, circuit breaker (CB) B1 will separate the faulted section from the system. This event may cause a change in the voltage magnitude leading to the unnecessary operation (nuisance tripping) of the protection system of the DG[25].

In Figure 2-1 when the DG is isolated from the network, for example when a fault occurs at F2, this faulted section will be separated and cleared by the relevant breakers B2 and B3. If the DG is designed to be capable of supplying Load1 and Load2, the distribution network load operation is not interrupted.

The operation of the DG in this situation, where there is no voltage and frequency reference, is called "islanding" or loss of main mode [25, 37-39]. However a severe failure can happen to this system after fault clearance if the section between B2 and B3 is re-connected without synchronizing. Operation in islanding mode thus means the system is at risk of damage to the plant, affecting the security and the stability of the whole system.

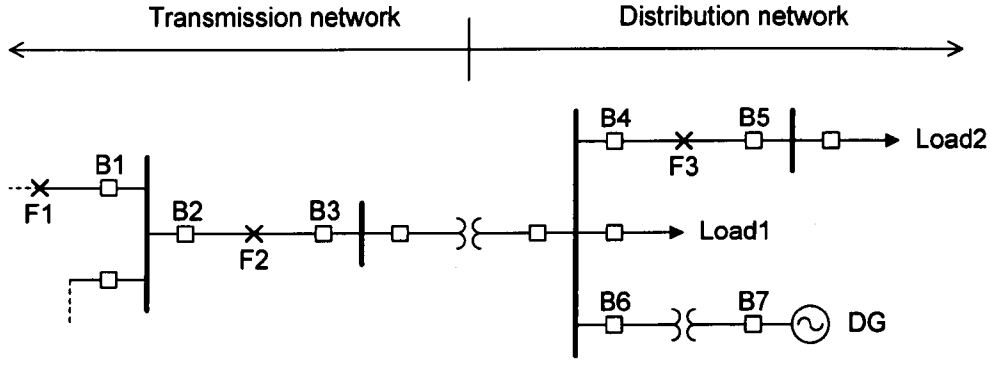

Figure 2-1 Protection relevant to distributed generation

In general, islanding mode operation is unacceptable [25, 38, 40], therefore all DG are installed with the appropriate protection that can separate the DG from the rest of the system when it is operating in islanding mode. Basically, at the beginning of islanding mode, the frequency will change as all the loads are transferred to the DG; the imbalance in power between the load and the supply (rate of change of power) causes a sudden change of frequency [41, 42]. A special protection relay called a "rate of change of frequency" (ROCOF) relay is used to monitor the change of frequency and trip the DG from islanding mode operation [41-43].

However the protection setup with the ROCOF relay is very sensitive. Load transient events could lead to the unnecessary tripping of this relay. For example a temporary fault at F3 in Figure 2-1 will result in the loss of the section between breakers B4 and B5. The re-connection of this section while Load 2 is still demanding full power will cause a sudden change in the power

supplied by the generator. However due to the delay in the mechanical prime mover, the generator cannot respond to this rapid change, and causes a rapid change of system frequency which may be detected by the ROCOF relay protection, causing a nuisance tripping of the breaker B7. This unnecessary tripping causes a reduction of security and stability of the system as the DG and the relevant generators are separated from the rest of the system, and may lead to further failure. Also if the system sees a large, sudden change in load 1 a change in frequency as mentioned will occur, leading to unnecessary trips.

The variation of generator shaft speed and the system frequency due to the transient events mentioned above may be mitigated by the use of energy storage within the power system. The potential improvement of system stability is described mathematically with the motion equation of the generators in the next section.

2.3 Analysis of instability within system with DG

Generally power system stability analysis is concerned with the balance of real power generated and consumed in an individual system. Ideally any ac power system that can keep the balanced condition between the electrical power generation and consumption during any disturbances operates stably. However, in practice, ac power systems have their individual limits of stability due to their own physical ability to respond to different types of disturbance. In this section, the causes of instability due to DG responding to the load impact and the proposed method to minimise this cause are described in section 2.3.1. The amount of the energy storage required to improve the stability is detailed in section 2.3.2.

2.3.1 Instability within system with DG

As generators are the main components used to produce electrical power supplied to the system, the nature of the conversion of mechanical input power to useful electrical power output is important. The response of the output power to the demand is then related directly to the response of the prime mover (effectively the mechanical input power). During transient events, the balance between the mechanical and electrical power can be seen in the simplified relationship of the electromagnetic torque and mechanical torque described by the rotational inertia Equations (2-1), (2-2), and (2-3) [6, 44], assuming that the losses are neglected.

$$T_a = T_m - T_e \tag{2-1}$$

where

T_a is the accelerating torque, N·m

T_m is the input mechanical generator torque, N·m

T_e is the output electrical torque, N·m

At the input, the generator shaft rotates according to the rotational inertia of both the generator turbine and the net torque (accelerating torque). Equation (2-1) can be re-written as shown in Equation (2-2) in order to relate the mechanical speed with the produced torque.

$$T_a = J\frac{d\omega}{dt} = T_m - T_e \tag{2-2}$$

where

J is the moment of inertia of generator and turbine, kg·m^2

ω is the an angular velocity of the rotor, rad/s

t is time, s.

At the output, neglecting the losses, the generator terminals give the electrical power proportional to the mechanical power described by production of generator shaft angular velocity and the produced torque as in Equation (2-3).

$$J\omega\frac{d\omega}{dt} = M\frac{d\omega}{dt} = P_m - P_e \tag{2-3}$$

where

P_m is the generator mechanical input power, W

P_e is the electrical output power, W

M is the inertia constant, J·s, and equal to J·ω.

In Equation (2-3) the balance condition is when the input mechanical power and the output electrical power of the generator are equal, the net power is zero, and in mechanical terms the net torque or accelerating torque in Equation (2-1) and (2-2) is equal to zero. As a consequence, the generator rotates at a specific, constant speed. Therefore, in electrical terms, this balance results in a specific constant frequency of the electrical output power.

However during transient events with a large disturbance, an immediate imbalance between the power generated and load demand will occur. Consequently the imbalance between the electromagnetic torque and mechanical torque will result in a change in generator shaft speed and therefore a change in frequency of the electrical power generated which can affect the system stability. The unbalanced condition originates from the delay of the mechanical input to the generator - the turbine and prime mover - when the generator is trying to match the new power demand.

If the power regulator for the prime mover – usually termed the governor - is slow to react, then the only way the generator can supply the additional load is if it slows down and releases stored kinetic energy to the load. If this happens only over a short period of time, the governor can react and the system can

resume stable operation. If the change in speed is very large, then the governor may not be able to prevent the generator losing synchronism and causing further failure within the system. Alternatively, the change of system frequency may cause ROCOF trips of DG and then a cascade failure of the system.

From Equation (2-2) and (2-3) this mismatch of power indicates that generator speed will not remain constant - $d\omega/dt$ is not equal zero. For example in the event of a fault occurring in the system which causes protection to operate and sudden loss of load, during the transient period the power P_e is less than the input power P_m (positive ΔP) and will result in a positive accelerating torque (speed and frequency increase). On the other hand, a sudden increase of load demand (negative ΔP) will result in a negative net torque or decelerating torque that immediately reduces the speed of the generator.

The variation of speed and frequency may change steadily or in an oscillatory manner depending on the system damping. This variation is an obvious abnormal condition directly concerned with stability. It can possibly pull the generator out of synchronism with the system and cause further technical problems and instability of the whole system.

To demonstrate how energy storage may be used to improve the stability of a power system, the aim here is to use energy storage coupled to a STATCOM to feed the sudden change of load (STATCOM-ES) whilst the slow governor of the prime mover has chance to react to the change, the energy storage is used for short term compensation only. Referring to Figure 2-2 the load is supplied by the STATCOM for a short time (the shaded area) until the main generator can respond – in this case the governor response has been approximated to a straight line. The requirement here is that the dynamic response of the STATCOM and its energy system are much faster than the speed of the governor.

Due to the rapid response of the power injected by the STATCOM, the net power of Equation (2-3) is balanced and therefore the frequency will be unchanged during the transient period. The generator will then reach the steady state condition to support the whole load without any significant change in frequency. Therefore this rapid support will help prevent the ROCOF relay tripping unnecessarily or nuisance tripping of the generator.

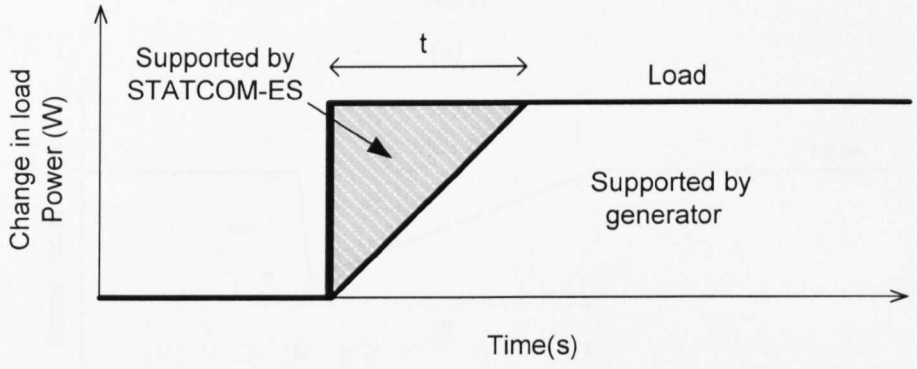

Figure 2-2 A sudden change of the load demand which is jointly supplied by the STATCOM-ES and a generator

For this proposed method, the amount of the energy required to limit the variation of the generator speed can be calculated as the shaded area in Figure 2-2, where the time "t" can be approximated as shown in the next section.

2.3.2 Energy storage required

An amount of energy required to keep the generator operating in a stable condition during the load impact described above can be estimated considering the speed variation as shown in Figure 2-3.

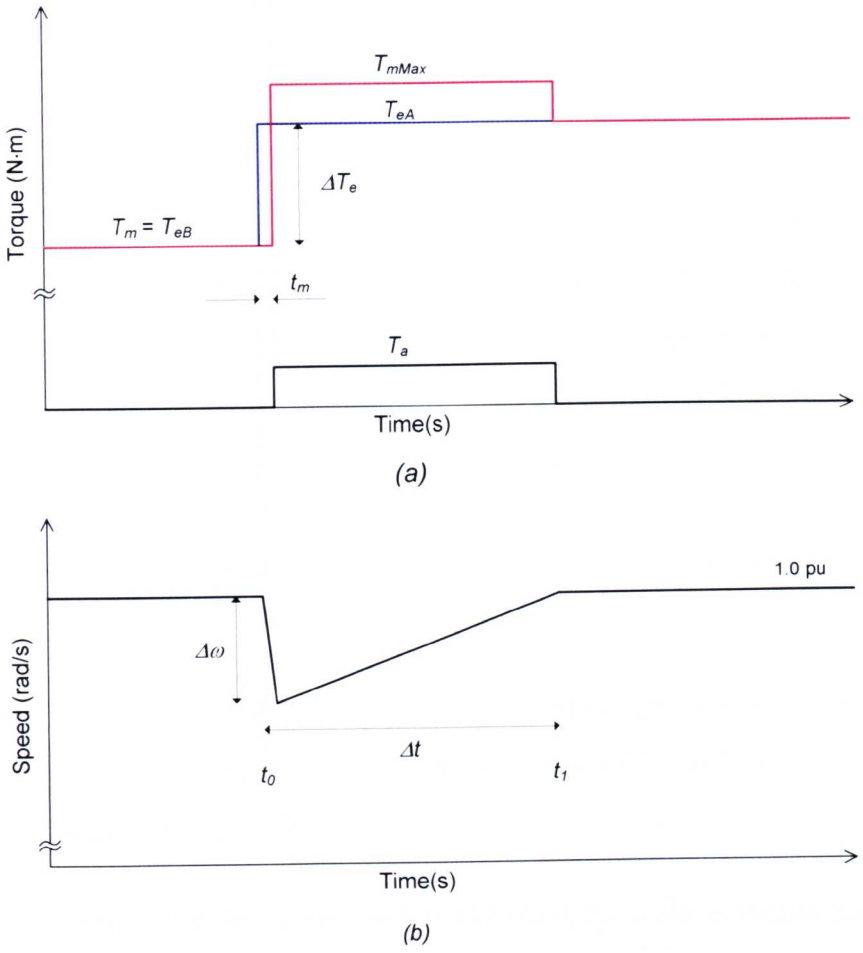

Figure 2-3 The simplified representation of (a) the mechanical, electrical and accelerating torque (b) the speed (ω) variation during load impact

Where

T_{eB} is the electrical torque before the load demand change, N·m.

T_{eA} is the electrical torque after the load demand change, N·m.

ΔT_e is the change in the electrical torque due to the change in the load demand, T_{eA}- T_{eB}, N·m.

T_{m_max} is the maximum (rated) generator torque, N·m.

t_m is the mechanical delay time, s.

Δt is the time the generator takes to develop the corresponding torque proportional to the load demand, s.

In Figure 2-3 during the time from the beginning to t_0, the generated power equals the load demand power - the generator is operating with balanced condition where the electrical torque T_{eB} equals the input mechanical torque T_m. Therefore, there is no accelerating or decelerating torque and the speed remains constant during this period. At time t_0, the sudden change in load demand occurs (i.e. the demand of electrical power increases suddenly to the maximum rating) resulting in the increase in the electrical torque from T_{eB} to the level represented by T_{eA} as shown in Figure 2-3(a). The rotor speed drops suddenly by $\Delta\omega$ as indicated in Figure 2-3(b).

The following assumptions have been made for the analysis presented in this section.

1) Before the change in load level, the generator supplies a light load that is very small compared to the main load. Therefore $T_{eB} << T_{eA}$ and thus $T_{eA} \Rightarrow \Delta T_e$.

2) After a period of the mechanical delay (t_m), the governor can react instantaneously to the change in load and is able to apply the maximum rating torque (T_{m_max}) to the generator as illustrated in Figure 2-3.

3) The change in rotor speed ($\Delta\omega$) is much smaller than the rated speed (ω). Therefore, $(\omega-\Delta\omega) \Rightarrow \omega$.

Regarding to the above assumptions and referring to Equations (2-1), (2-2) and (2-3) when the electrical power output of the generator changes due to load variation, the accelerating torque can be re-written as in Equation (2-4).

$$\begin{aligned} T_a &= T_{m\_max} - T_{eA} \\ &= T_{m\_max} - \frac{\Delta P_{load}}{\omega} \end{aligned} \tag{2-4}$$

In Equation (2-4), ΔP_{load} is the change in the load demand. It is assumed that the generator accelerates in a linear fashion to the new load torque level, then referring to the representation in Figure 2-3 the acceleration can be approximated as in Equation (2-5).

$$T_a = J\frac{\Delta\omega}{\Delta t} \tag{2-5}$$

In order to develop the corresponding torque, the generator takes a time of approximately Δt from the beginning of the change in load demand at t_0 to when the generated torque reaches the balanced point at t_1 (where the generated torque equals load torque). Therefore this period can be determined using Equation (2-4) and (2-5), and is given in Equation (2-6).

$$\Delta t \cong \frac{J\Delta\omega}{T_{m\_max}-\left(\frac{\Delta P_{load}}{\omega}\right)} \tag{2-6}$$

The minimum amount of the energy required if a STATCOM-ES were to be used during this period to minimise $\Delta\omega$ can be approximately calculated as in Equation (2-7) and is given in Equation (2-8).

$$\begin{aligned} E_{used} &= \int \Delta P_{load} dt \\ &\cong \Delta P_{load} \cdot \Delta t \end{aligned} \tag{2-7}$$

$$E_{used} \cong \frac{(\Delta P_{load})(J\Delta\omega)}{T_{m\_max}-\left(\frac{\Delta P_{load}}{\omega}\right)} \tag{2-8}$$

Therefore the capacity of the energy storage unit to be installed with STATCOM-ES can be estimated using the value of the maximum load

(P_{load_max}) and the maximum frequency change (Δf_{max}) allowed for a specific system which is related to $\Delta\omega_{max}$ for the generating unit as in Equation (2-9).

$$E_{req\_min} \cong \frac{(P_{load\_max})(J\Delta\omega_{max})}{T_{m\_max}-\left(\frac{P_{load\_max}}{\omega}\right)} \quad (2\text{-}9)$$

E_{req_min} is the minimum amount of the energy required for the STATCOM-ES, for a system with a generator with an inertia J.

In the next section, simulation studies will underline the benefits of a system with a STATCOM plus energy storage that can inject real power support instantaneously to the ac grid in order to keep the rate of change of the frequency within an acceptable range to prevent the mal-operation of the ROCOF relay.

2.4 Simulation of a generator supplying a system with a sudden load change

The system simulated comprises a diesel-engine generator supplying a load through a step-down transformer as illustrated in Figure 2-4. The load is switched on to the secondary of the transformer causing a sudden change in the demand for real power. The light load is used in the simulation to represent the quiescent system load.

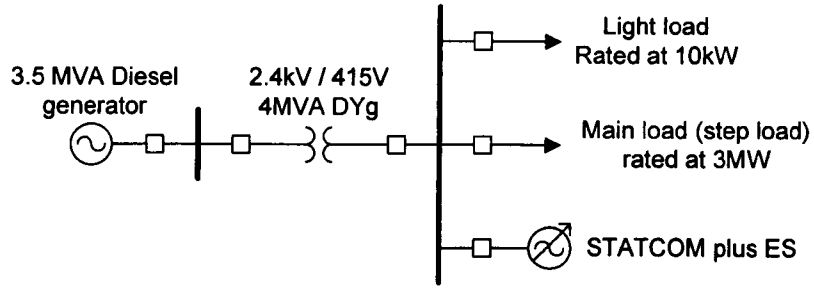

Figure 2-4 The power circuit diagram of the system used in the simulation

The STATCOM with energy storage is designed to be able to deliver a total energy of 7.8MJ to the grid (a ramp shape as the shaded area shown in Figure 2-2 with the maximum ramp power of 3 MW during the time of 5.2s).

The simulations are carried out using the MatLab/Simulink SimPowerSystems simulation package[45]. The details of the simulation including the generator model, its speed governor and excitation control are described in Appendix A.

A case study scenario with the power circuit shown in Figure 2-4 is simulated with and without the real power support from the STATCOM plus energy storage. The simulations are carried out focusing on the behaviour during the period when the governor responds to the new load, to demonstrate the improved system control.

2.4.1 A generator supplying a system with a sudden load change without support from STATCOM-ES

For comparison, the system described above in section 2.4 is simulated without the support from the STATCOM plus energy storage. Therefore all the load demand will be supplied solely by the generator. The results of the

load and generator currents are illustrated in Figure 2-5, while Figure 2-6 shows the variation of the generator speed and the terminal voltage.

Before the main load is switched on, from the beginning of the simulation to the time t=1.0s, the top trace of Figure 2-5 shows that the generator is supplying only a very small current of around 70A to the light load or for the quiescent system load.

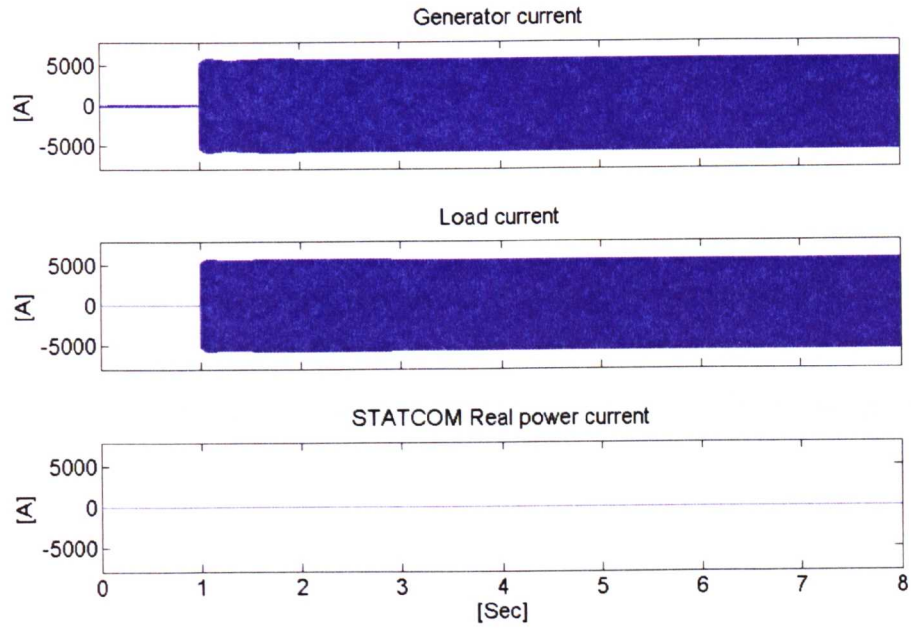

Figure 2-5 Generator current, load current, and support current during the operation of the system without real power support

At time t=1.0s the main load is switched on to the secondary side of the step-down transformer. A sudden load current change from 0A to approximately 5.9kA (peak) can be clearly seen in the middle trace of Figure 2-5. As mentioned above this load demand will be supplied only by the generator, the sudden change of the generator current also appears in the middle trace of Figure 2-5 with the same trend as of the load current. Also in Figure 2-5 the bottom trace shows that in this operation mode there is no support current from the STATCOM unit.

Focusing on the generator mechanism, the rotor speed deviation is measured in per-unit quantity (pu) shown in Figure 2-6 (the upper trace). At the beginning period of the simulation between time t=0s and t=1.0s where there is no impact on the generator, the rotor speed remains unchanged representing that the generator speed is constant at the synchronous speed. The terminal voltage also remains unchanged at 1.0 pu.

However with the impact of the sudden load change, the upper trace of Figure 2-6 shows the rotor speed deviation over the period t=1.00s and t=1.25s. This shows that the rotor speed and the frequency drop sharply by 7% during that period.

After that, from time t=1.25s onward, the generator governor control responds to this change by modulating the appropriate mechanical input power to the generator in order to match the electrical power at its output terminals. The rotor speed is then gradually increased until the mechanical and electrical power are in balance at time approximately t= 5.5s – the rotor speed also reaches a steady state.

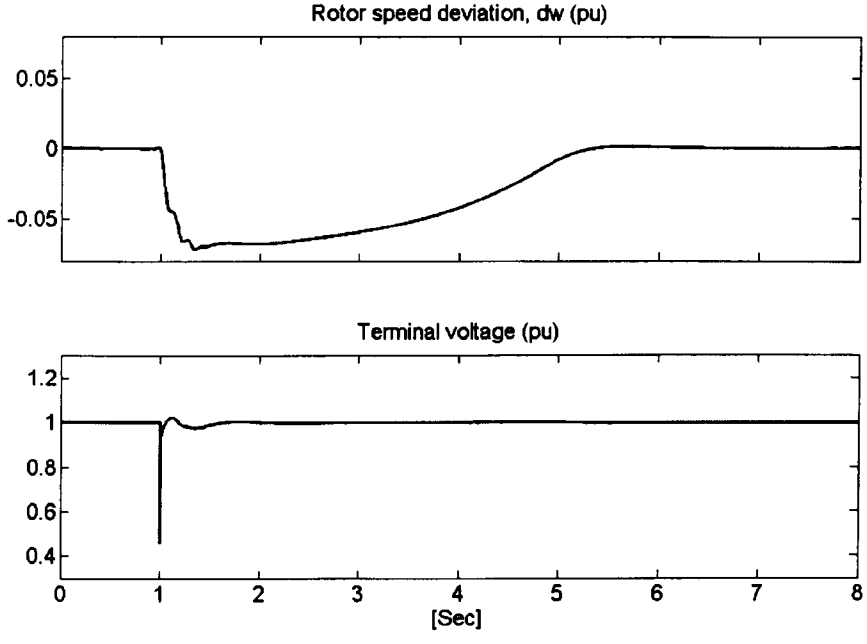

Figure 2-6 Rotor speed deviation and terminal voltage during the operation of the system without real power support

Meanwhile the impact of the main load on the terminal voltage is shown in the lower trace of Figure 2-6, where the sudden drop of voltage is regulated by the generator excitation control. According to the excitation control action, the variation of the terminal voltage - a small overshoot and oscillation can be seen during time t=1.0s to t=2.0s.

2.4.2 A generator supplying a system with a sudden load change with support from STATCOM-ES

In this section real power support produced from the STATCOM plus energy storage is included in the simulation. As mentioned previously the sudden

change of the load demand will be partly supplied by the STATCOM unit at the beginning of the load impact. Load current, generator current, and the support current are illustrated in Figure 2-7. The variation of rotor speed and the associate terminal voltage are shown in Figure 2-8.

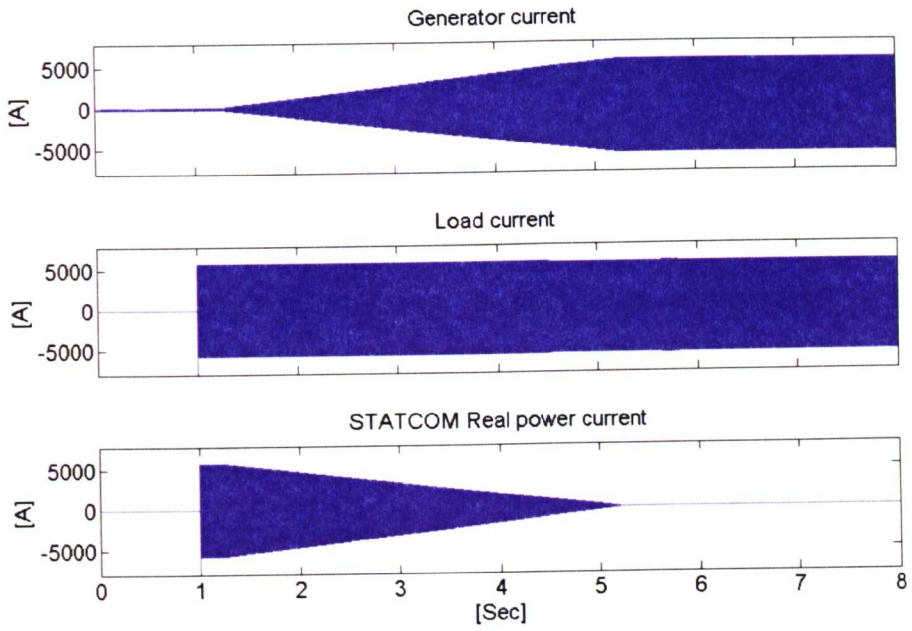

Figure 2-7 Generator current, load current, and support current during the operation of the system with real power support from the STATCOM plus energy storage

In Figure 2-7 from the time t=1.0s onward the same sudden change of the main load current from 0A to 5.9kA (peak) as described previously is seen in the middle trace of Figure 2-7. To minimise the impact on the generator, at the beginning of this transient condition, the load is supplied partly by the rapid real power injection produced from the STATCOM unit.

According to the limit in the amount of stored energy in the STATCOM unit, the rapid support current is designed to inject real power to the load with magnitude equal to the maximum load current at the beginning then reducing constantly to zero at time t=5.2s as shown in the bottom trace of Figure 2-7. As a consequence, at the beginning of the load impact the generator begins

with a low current at time t=1.0s and then increases constantly with the support current from the STATCOM unit until reaching the maximum current at time t=5.2s (when the support current becomes zero) as shown in the top trace of Figure 2-7.

As a result, with the support power, the impact on the generator due to a sudden change in the loading condition is reasonably reduced (also the degree of the imbalance between the power generated and load demand is reduced). The rotor speed variation is therefore minimised as illustrated in the upper trace of Figure 2-8. This also indicates that the frequency variation during the load impact will be minimised depending on the energy injected by the STATCOM unit. The lower trace of Figure 2-8 also shows that with the real power support from the STATCOM the terminal voltage variation is minimised. This obviously is a very good result at the expense of energy storage with high power and high energy rating. The value could be reduced (as could cost), whilst still keeping $\Delta\omega$ within regulations.

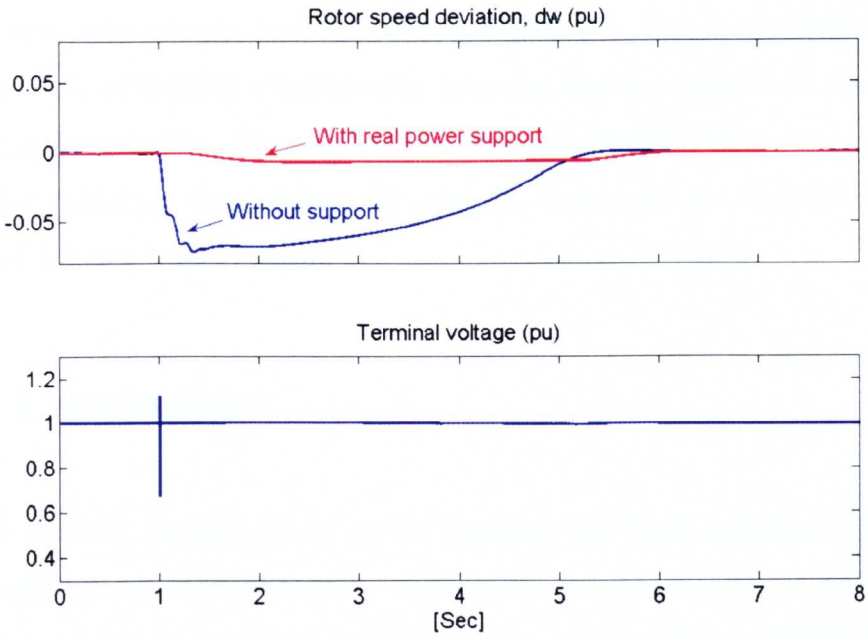

Figure 2-8 Rotor speed deviation and terminal voltage during the operation of the system with real power support from the STATCOM plus energy storage

From Figure 2-8, it can be seen that for the system simulated with $\Delta\omega_{max} \approx 22$ rad/s (7%). The load change, P_{load_max} was 3 MW, and T_{m_max} was 9947.16 Nm (assuming losses are neglected and the governor applies the maximum torque which was calculated from the generator rated power of 3.125MW to the generator), and the inertia constant, H = 0.69. The moment of inertia, J can be calculated using Equation (2-10) [6] where VA_{base} was the generator rated power, thus J = 43.7 kg.m^2.

$$J = \frac{2H}{\omega^2} VA_{base} \tag{2-10}$$

Therefore the estimated energy storage requirements using Equation (2-9) were 7.25 MJ. This compares to the value of 7.8 MJ measured from the simulation.

As described earlier, Equation (2-9) is derived based on the assumptions that rotor speed varies linearly during the beginning of the generator response as illustrated in Figure 2-3. In reality and in this simulation the rotor speed variation is not a straight line, as shown in Figure 2-8. This is the main reason why an error of 0.55MJ (7%) is seen from the above comparison. However this error is acceptable. As mentioned, the energy estimated using Equation (2-9) is the minimum requirement. In practice, this could be multiplied by a factor of 1.2 as a "rule of thumb".

2.5 Conclusions

Recent stability analysis of ac power systems has been involved with the system studies of local generation - distributed generation (DG) or embedded generation that is increasingly penetrating into power systems. Although DG has introduced benefits to the ac power systems, some technical impacts need to be considered.

The impact of the DG on system stability has been highlighted here. The unnecessary or nuisance tripping of DG by a ROCOF relay can have a large destabilizing effect as it can lead to cascade system shutdown. As the immediate power imbalance between the generation and consumption of the power during the transient events is the cause of the ROCOF relay event, the rapid power support by the proposed STATCOM-ES can minimise the generator speed and frequency variation and help prevent nuisance tripping of DG. Therefore the system stability can be improved using the STATCOM with energy storage. The simulation work carried out and explained in this chapter confirms the proposed idea.

The results clearly show that with the proposed STATCOM-ES the system stability will be improved. More detail of the STATCOM and the proposed STATCOM with supercapacitor energy storage are described in the next two chapters.

Chapter 3

STATCOM

3.1 Introduction

As discussed earlier, the principle for voltage compensation is to feed reactive power to the ac grid according to the drop in magnitude of the bus voltage. Similarly, to maintain constant power system frequency, an injection of real power may be required. Recently, a power electronic shunt compensator called Static VAr Compensator (STATCOM) has been employed in ac power systems and as a controlled source of reactive power is able to provide voltage control. Amongst other conventional reactive power compensators, STATCOM has a better dynamic response, higher reliability, and requires smaller space [46].

In this chapter, grid connected power converters are described in section 3.2. The flow of power between the converter and the ac power grid is explained in

section 3.3. The principle and control of the STATCOM based on a voltage source power converter is detailed section 3.4. Finally, in section 3.5, a simulation study highlights the benefits to an ac power system using a STATCOM.

3.2 Grid connected power converter

Due to the recent development of modern power electronic devices and their control topologies, dc-to-ac power converters have found application in ac power systems. Switching techniques are required for the dc-to-ac converter for the purpose of synthesizing close-approximation to a sinusoidal voltage. The converter produces a three-phase ac voltage using high frequency switching techniques. Therefore, a coupling reactor is needed to link between the converter and the ac grid, and to perform current smoothing, ensuring that the converter feeds an acceptable sinusoidal current into the ac grid. This reactor is also used to prevent damage to the DC-link capacitor which may occur due to the rapid charge/discharge when directly connected to the grid.

The configuration of the converter when the dc-side is a DC-link voltage is called "Voltage Source Converter" (VSC). The switching technique used to operate the grid connected power converter depends on its configuration which can be categorised into two groups: - two level converter and multilevel converter.

3.2.1 Two-level three phase power converter

The circuit configuration of a two-level power converter connected to the ac grid is shown in Figure 3-1. In this configuration, for each phase-leg, two switching devices are connected in series (six switches in total). The two switches in the phase-leg are operated in a complementary way. Thus, at any

instant of time, only one switch is on, the other one must be off. In order to prevent failure if both the switches are on at the same time due to the finite transition time of the switches, a small time delay (i.e. blanking time or dead time) is normally included in the switching pattern.

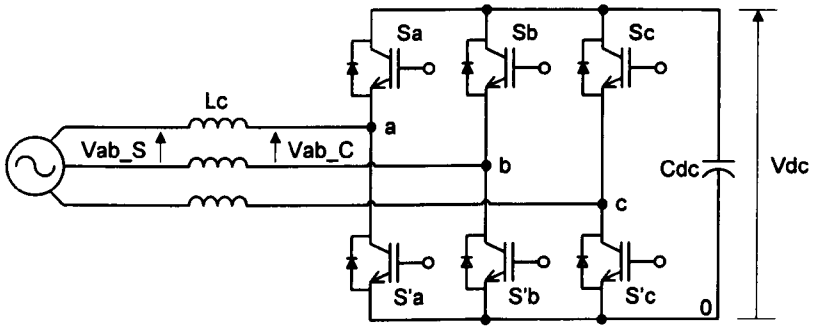

Figure 3-1 The conventional 6-pulse grid connected power converter

An example of the resulting voltage produced by a two-level converter is shown in Figure 3-2 (circuit without neutral point) where the conduction of the switch in each phase leg is set to 50% duty ratio [47]. When the upper switch (S_a, S_b or S_c) is on, the 'a' terminal is connected to V_{dc} resulting in the voltage V_{ao} equalling V_{dc}. The other phase legs are connected in the same way, but with a phase delay of 120° as in the standard three-phase ac system. These phase voltages indicate that there are two levels in the voltage waveforms (V_{dc} and zero). The line voltage, for example V_{ab}, is determined by measuring the voltage difference between terminal 'a' and 'b' which is equal $V_{ab}=V_{ao}-V_{bo}$ indicating in the top trace of Figure 3-2.

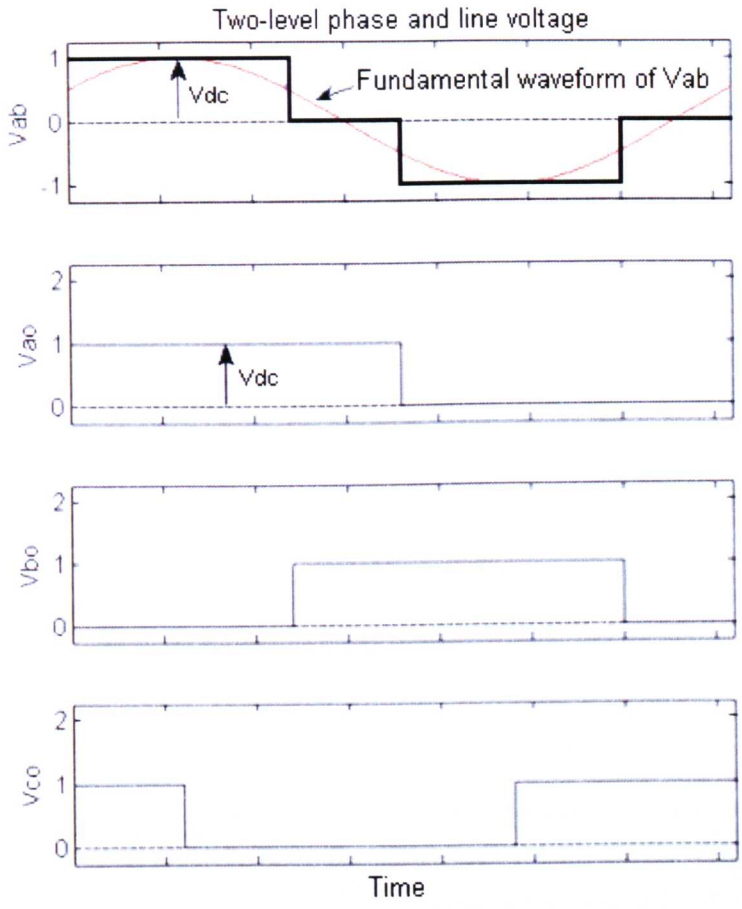

Figure 3-2 Phase and line voltage of the 2-level dc-to-ac converter

The top trace of Figure 3-2 shows that the resulting line voltage is a 3-level voltage waveform (V_{dc}, zero and $-V_{dc}$). It can be summarised that the levels of line voltage can be determined by (2M-1) where M is the number of levels of the phase voltage.

Pulse Width Modulation (PWM) is a switching technique which can be applied to this converter to give a better quality output voltage than the one shown in Figure 3-2. In this technique the width of the switching signals (pulses) is modulated according to the control input signals. The PWM signals are generated by comparing the three-phase sinusoidal control signals (V-

control) which are 120° out of phase, with a repetitive switching-frequency triangular waveform (V-tri) as shown in Figure 3-3.

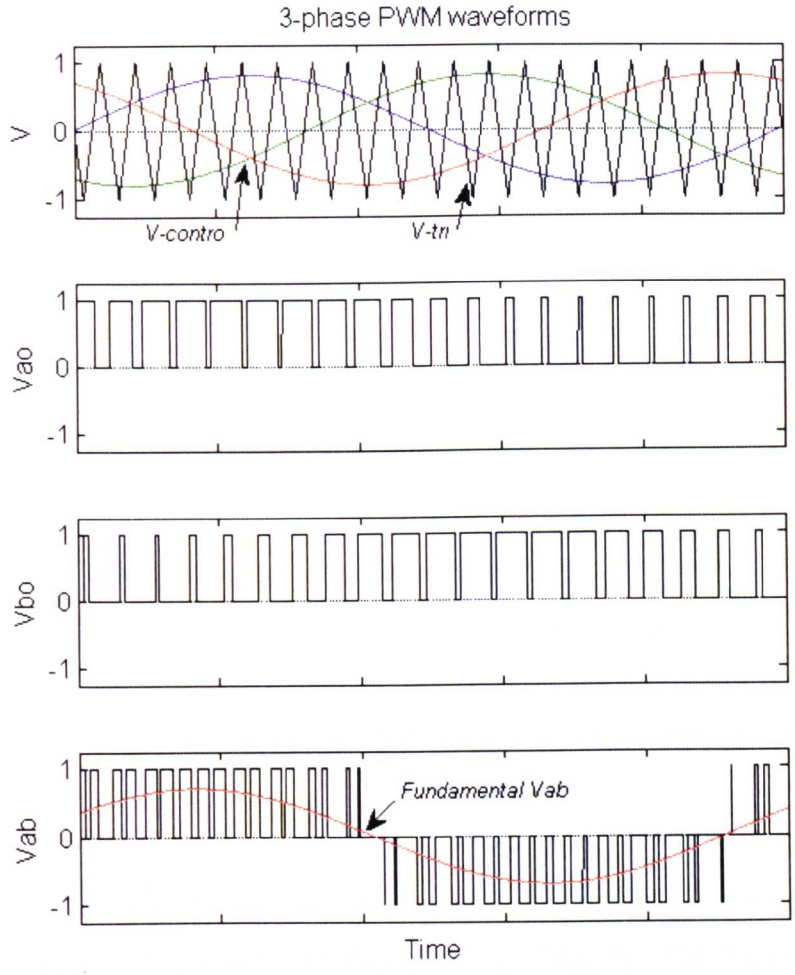

Figure 3-3 Phase and line voltage of the 2-level dc-to-ac converter with PWM switching technique

The PWM signals turn on and off the switches in the three phase-legs of the converter shown in Figure 3-1. The phase voltage (V_{ao}, V_{bo} and V_{co}) equals V_{dc} when the associated upper switch is turned on and the lower switch is turned off as they are switched as a complementary pair, resulting in a series of square wave pulses of different width as illustrated by V_{ao} and V_{bo} of Figure 3-3. The difference in the width of the pulses represents the magnitude of the voltage that is related to the sinusoidal modulation signal. The bottom

Figure 3-3 shows the line voltage, V_{ab} which results from $V_{ab}= V_{ao}-V_{bo}$ compared with the desired fundamental voltage.

3.2.2 Multilevel power converter

Over recent years there has been a move towards increasing the voltage compatibility of IGBT voltage source converters. One technique used to achieve this is the multi-level converter, and the main topologies used are the diode-clamped, flying-capacitor and cascaded converter.

3.2.2.1 Diode-clamped multilevel converter

Typically the diode-clamped M-level converter uses M-1 capacitors to make up DC-link [48-52]. For example the 5-level diode-clamped converter shown in Figure 3-4 (only phase 'a' and 'b' leg shown) has four capacitors (C_1, C_2, C_3, and C_4) connected in series indicating that the voltage across each capacitor is $V_{dc}/4$.

In Figure 3-4 the switches in each phase leg can be turned on and turned off in five different combinations. The phase voltage (V_{ao},V_{bo} and V_{co}) is a 5-level staircase waveform. As a result, the output line voltage ($V_{ab} =V_{ao}-V_{bo}$) is a 9-level (2M-1) staircase waveform.

For the diode-clamped multilevel voltage source converter, with the higher the number of levels the lower the harmonic content will be appeared on the output voltage waveforms. However, the converter with that many voltage levels will require many more switching devices.

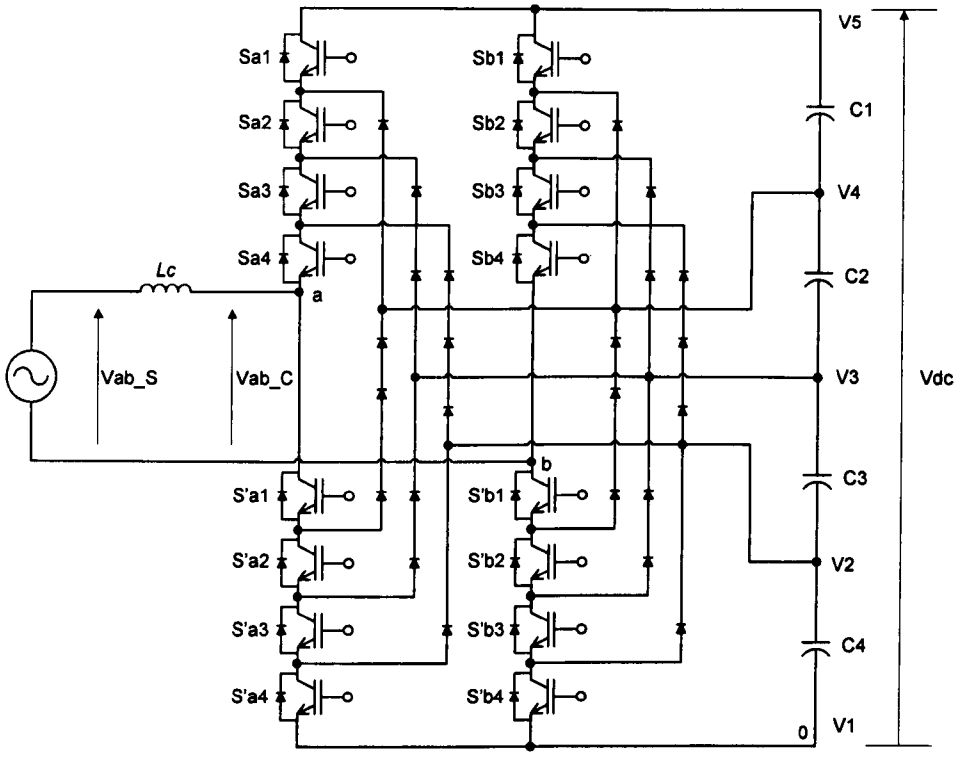

Figure 3-4 Circuit diagram of a 5-level diode-clamped converter

3.2.2.2 Flying capacitor multilevel converter

The basic circuit diagram of a flying capacitor multilevel converter is illustrated in Figure 3-5 [50, 51]. In the figure, the 5-level flying capacitor voltage source is detailed with the number of switches in phase leg 'a' and 'b', the arrangement of phase 'c' is identical. The number of capacitors used as the DC-link capacitor is the same as used for the diode-clamped converter (M-1). However, instead of using clamping diodes, the inner-loop capacitors are added to each phase in order to create the voltage levels.

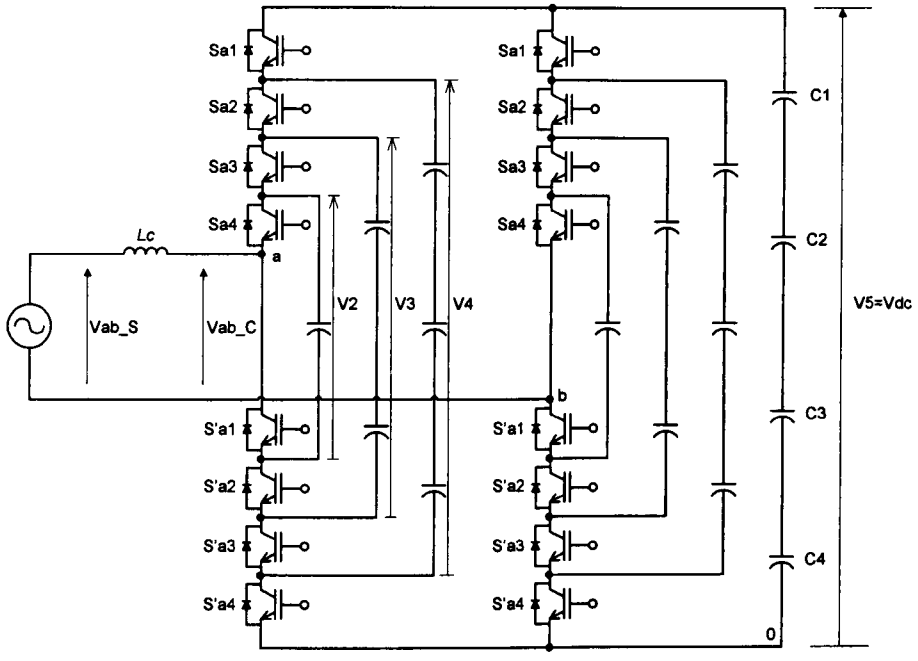

Figure 3-5 Circuit diagram of a 5-level flying capacitor converter

The voltage waveforms produced by a flying capacitor converter is similar to that produced by the diode-clamped converter, where the number of line voltage levels also follows the (2M-1) staircase waveform. Nevertheless, with the inner balancing capacitors, the converter has more flexibility to produce the voltage than the diode-clamped converter. However, the flying capacitor multilevel converter needs a large number of capacitors to produce a higher level voltage.

3.2.2.3 Cascaded multilevel converter

In order to avoid using clamping diodes or inner-voltage balancing capacitors, the multilevel voltage source converter can be constructed in a cascaded structure as shown in Figure 3-6 [50, 52]. A separate DC source for each DC-link is used for each single phase full-bridge converter. There are four switches for each single phase converter (S_1, S_2, S_3, and S_4) which is used to produce 3-level output voltage - equal $+V_{dc}$ when S_1 and S_4 are on the others

are off, equal $-V_{dc}$ when S_2 and S_3 are on the others are off, and equal zero when S_1 and S_3 and on, S_2 and S_4 are off.

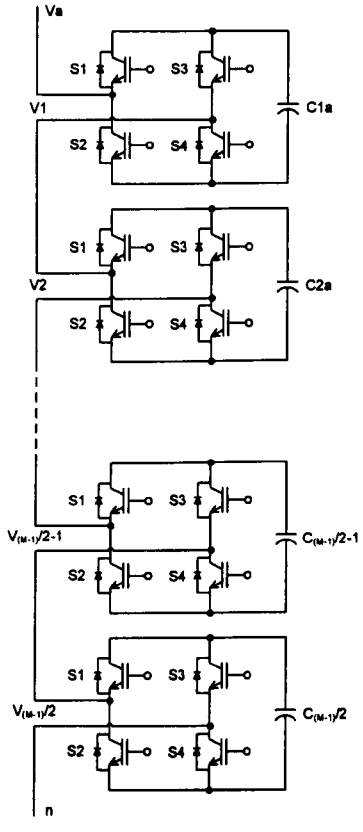

Figure 3-6 Circuit diagram of a single phase cascaded multilevel converter

For a cascaded converter, the phase voltage level can be defined by 2N+1, where N is the number of full-bridge converters used in each phase.

The configuration of single phase converter in Figure 3-6 can be connected in either star or delta to form the three phase cascaded multilevel voltage source converter. The star-connected three phase converter, for example, is illustrated in Figure 3-7.

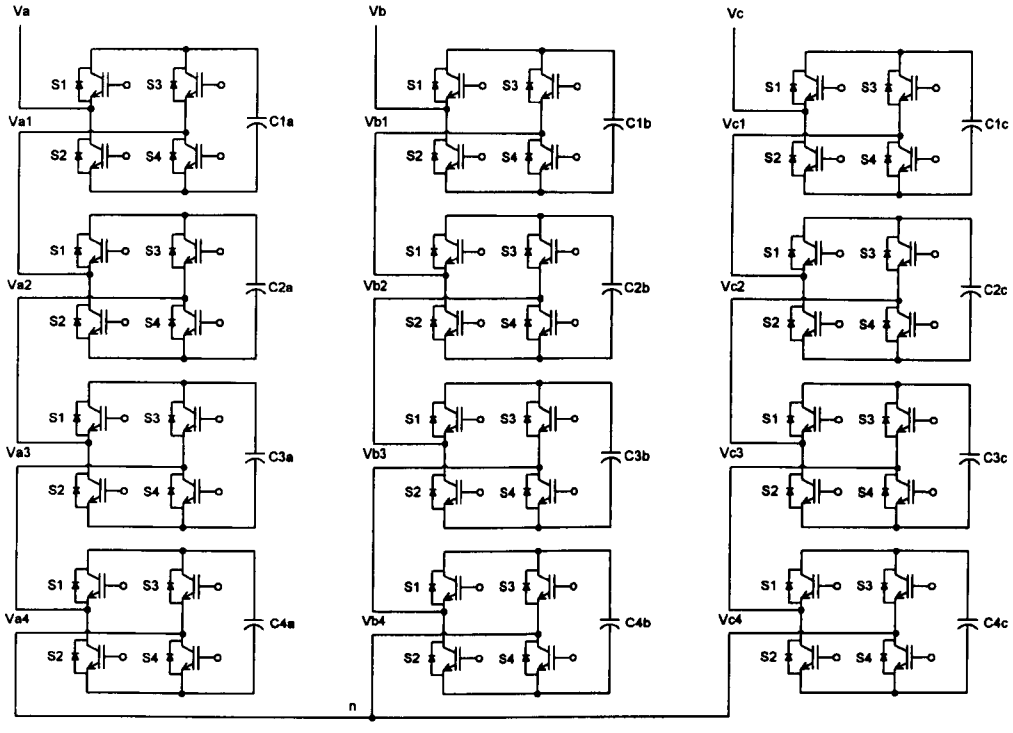

Figure 3-7 A star-connected cascaded 9-level converter

It is clear that the cascaded multilevel converter, compared to the other two multilevel converters mentioned above, requires fewer additional components to achieve the same number of the voltage levels. The full-bridge converter can also be built as a cell which makes it more reliable and flexible to expand the circuit.

The brief overviews of the grid connected converters in section 3.2.2 have pointed out that the multilevel power converters have advantages over the standard two-level converters. However in order to have the multilevel converters operate safely and with reliability, their complex configurations require even more complicated control techniques. Therefore, for simplicity and economic reasons, the two-level PWM converter is chosen for the experimental validation, and its switching technique is based on the standard sinewave PWM modulation. Also the simulation studies are carried out based on the setup with the two-level voltage source converter.

3.3 Power flows between converter and ac grid

An equivalent circuit diagram of the STATCOM configuration with a 2-level converter is illustrated in Figure 3-8, where V_a, V_b, and V_c represent the ac power grid voltage. V_{a_c}, V_{b_c}, and V_{c_c} represent the converter voltages. I_a, I_b, and I_c are the line currents flowing through the coupling reactor L. The internal resistance R of the coupling reactor is also included in the equivalent circuit.

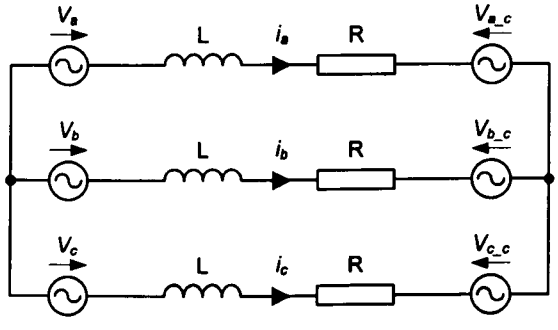

Figure 3-8 The equivalent circuit diagram of a three phase voltage source converter connected to the ac power grid

It is well-known that in the a-b-c reference frame the instantaneous active power (p) and reactive power (q) at any point can be defined by using the instantaneous three-phase voltage and current. The active power equation is in Equation (3-1).

$$p(t) = v(t) \cdot i(t) = v_a(t)i_a(t) + v_b(t)i_c(t) + v_c(t)v_c(t) \qquad (3\text{-}1)$$

For simplicity the (t) will be dropped, Equation (3-1) becomes

$$p = v \cdot i = v_a i_a + v_b i_c + v_c v_c \qquad (3\text{-}2)$$

and the reactive power equation is

$$q = v \times i = (v_a i_b - v_b i_a) + (v_b i_c - v_c i_b) + (v_c i_a - v_a i_c) \qquad (3\text{-}3)$$

To create references for active and reactive power control, the instantaneous power can be obtained by means of a vectorial interpretation of the instantaneous three-phase values using co-ordinate transformation. The stationary frame α-β transformation with the transform matrix shown in Equation (3-4) [53, 54] transforms the associated instantaneous phase voltages and currents to the instantaneous voltage and current vectors as in Equation (3-5), assuming a balanced supply and load. This approach is only applicable to the balanced case.

$$[C] = \frac{2}{3}\begin{bmatrix} 1 & -1/2 & -1/2 \\ 0 & \sqrt{3/2} & -\sqrt{3}/2 \\ 1/\sqrt{2} & 1/\sqrt{2} & 1/\sqrt{2} \end{bmatrix} \qquad (3\text{-}4)$$

$$\begin{bmatrix} V_\alpha \\ V_\beta \\ 0 \end{bmatrix} = [C]\begin{bmatrix} V_a \\ V_b \\ V_c \end{bmatrix} \quad , \quad \begin{bmatrix} i_\alpha \\ i_\beta \\ 0 \end{bmatrix} = [C]\begin{bmatrix} i_a \\ i_b \\ i_c \end{bmatrix} \qquad (3\text{-}5)$$

Using these vector quantities in the stationary α-β frame, the instantaneous active and reactive power given by Equation (3-2) and (3-3) can be rewritten in terms of α-β quantities as in Equation (3-6) and (3-7).

$$P = v \cdot i = \frac{3}{2}\{V_\alpha I_\alpha + V_\beta I_\beta\} \qquad (3\text{-}6)$$

$$Q = v \times i = \frac{3}{2}\{V_\alpha I_\beta - V_\beta I_\alpha\} \qquad (3\text{-}7)$$

For control, the synchronously rotating reference frame (d-q reference) is introduced to further manipulate the vector quantities. In this reference frame the d and q axes follow the trajectory of the phase voltage vector with the rotating angle,θ. Therefore the time-varying transform matrix in Equation (3-8) results in the dc quantities as in Equation (3-9).

$$[C_{dq}] = \frac{2}{3}\begin{bmatrix} cos(\theta) & cos\left(\theta - \frac{2\pi}{3}\right) & cos\left(\theta + \frac{2\pi}{3}\right) \\ -sin(\theta) & -sin\left(\theta - \frac{2\pi}{3}\right) & -sin\left(\theta + \frac{2\pi}{3}\right) \\ 1/\sqrt{2} & 1/\sqrt{2} & 1/\sqrt{2} \end{bmatrix} \quad (3\text{-}8)$$

$$\begin{bmatrix} V_d \\ V_q \\ 0 \end{bmatrix} = [C_{dq}]\begin{bmatrix} V_a \\ V_b \\ V_c \end{bmatrix} \quad , \quad \begin{bmatrix} i_d \\ i_q \\ 0 \end{bmatrix} = [C_{dq}]\begin{bmatrix} i_a \\ i_b \\ i_c \end{bmatrix} \quad (3\text{-}9)$$

Normally, the d-axis voltage vector is coincident with the instantaneous phase voltage vector of the ac power grid, thus the q-axis voltage is zero. Substituting the instantaneous d-q voltage and current components in Equation (3-2) and (3-3) gives

$$P = v \cdot i = \frac{3}{2} V_d I_d \quad (3\text{-}10)$$

$$Q = v \times i = \frac{3}{2} V_d I_q \quad (3\text{-}11)$$

From Equation (3-10) and (3-11), the instantaneous active and reactive power controls can be achieved directly by controlling the d and q axes current components. The possible power flow between three phase converter and the ac power grid is illustrated in Figure 3-9, where P is real power, Q is reactive power, V_{pcc} is voltage at the common coupling, V_{conv} is the controllable

voltage produced by the converter, and I_d and I_q are the d and q-axis current representing real and reactive power respectively.

It can be seen in the diagram of Figure 3-9 that to compensate the reactive power requires the control of the magnitude of the converter output voltage – i.e. if the magnitude of V_{conv} is higher than the magnitude of V_{pcc}, the converter is injecting reactive power to the ac power grid, indicated by 90 degree leading I_q in Figure 3-9 (b), (f), and (g). In the other hand, Figure 3-9 (a), (e), and (h) indicate 90 degree lagging I_q when the magnitude of V_{conv} is lower, showing that the converter is absorbing reactive power.

Figure 3-9 also indicates that the real power compensation can be achieved by controlling the phase displacement of the converter voltage. In this research, leading V_{conv} results in negative I_d (180 degree lagging the voltage) which indicates that the converter is injecting real power to the ac power grid, indicated by Figure 3-9 (c), (e), and (g). Lagging V_{conv} shown Figure 3-9 (d), (f), and (h) result in positive I_d (0 degree difference) indicating the converter is absorbing real power from the ac power grid.

The flexibility of the current controlled by the converter with enough energy storage can be seen throughout Figure 3-9. In the next section, a conventional STATCOM based on the voltage source converter is described. However, due to the limited energy storage capability of the usual DC-link capacitor, the current controlled by the STATCOM provides only reactive power control as shown in Figure 3-9 (a) and (b).

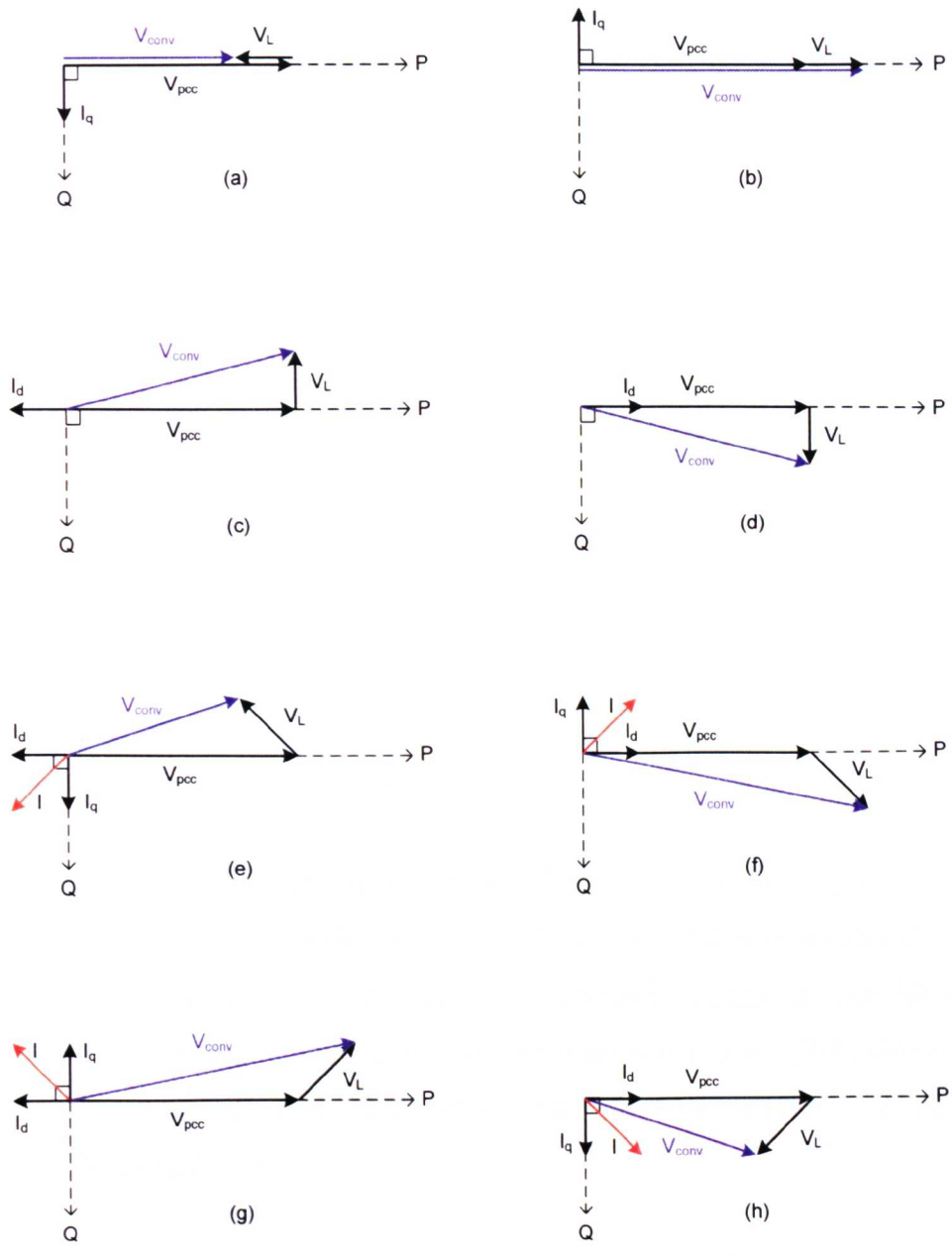

Figure 3-9 The possible power flow controls between voltage source converter and grid

3.4 STATCOM

In this project, a voltage source converter is adopted for use as the main component of the STATCOM. The power circuit diagram of the STATCOM based on a voltage source converter is illustrated in Figure 3-10, where six

IGBTs with its anti-parallel diodes and a DC-link capacitor are used to produce the three-phase voltage. The three-phase inductor L_c is used as the coupling reactor linking the converter to the ac power grid.

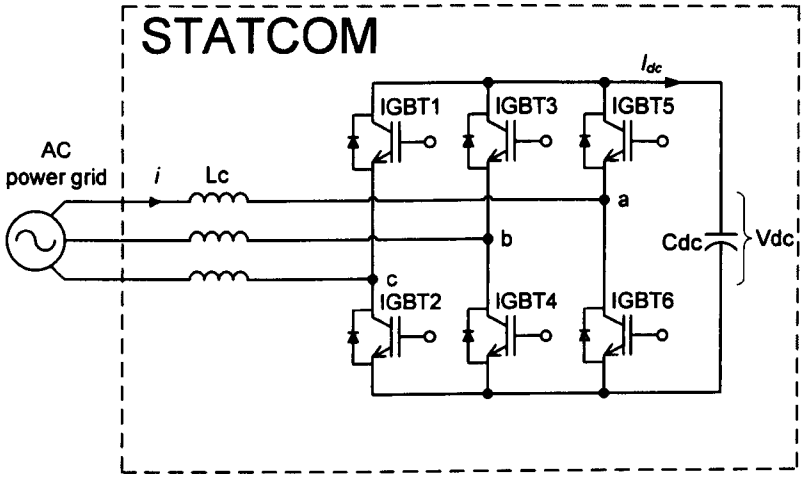

Figure 3-10 A power circuit diagram of a STATCOM

The basic principle of operation is that the amplitude and phase of the converter voltage is controlled with respect to the measured ac power grid voltage. This can only be achieved if the DC-link voltage is significantly larger than the peak line-to-line voltage of the ac power grid. The generation of the desired voltage at the front-end of the converter can be achieved by pulse width modulation.

Although the output voltage of the converter is a high frequency switching waveform, the coupling reactor acts as a filter and therefore sinusoidal current can be seen flowing in between the ac grid and the STATCOM unit. The strategies used to achieve instantaneous power control are discussed below.

3.4.1 Scalar control

In the scalar control strategy the controller is designed to operate in the stationary a-b-c reference frame, for example in [20, 55-58]. An outer loop is required to control the DC-link voltage to a value greater than the peak ac line-to-line voltage such that it behaves as a boost converter. The output of the DC-link voltage controller produces a demand for the current control in order to vary the magnitude of the controlled current as shown in Figure 3-11.

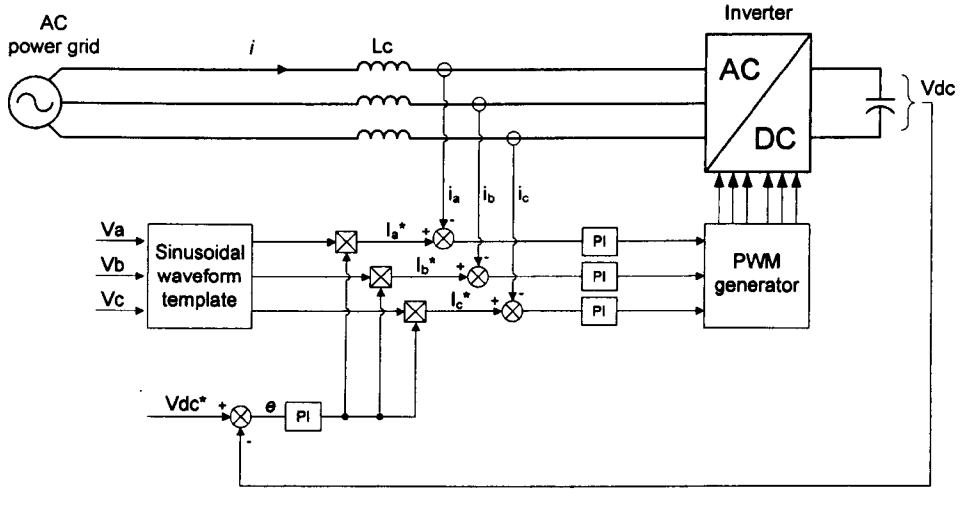

Figure 3-11 A simplified scalar control strategy

In Figure 3-11 the V_{pcc} voltages, V_a, V_b, and V_c are measured and fed to the sinusoidal waveform template. The sinusoidal waveform template is in-phase with the supply phase voltage. The output from the sinusoidal template is then multiplied by the output of the DC-link voltage controller, and therefore used as the reference current (I_a*, I_b*, and I_c*). These reference currents are compared with the measured currents (I_a, I_b, and I_c). The error, e, is modulated by another PI controller to generate PWM reference signals. Finally the desired voltage at the front-end of the converter is generated according to the controlled PWM signal.

However for this strategy the controllers are designed to operate with an ac signal reference input at the frequency of the ac grid voltage. Steady state current error can be seen. As it is based on the steady state relationships, this strategy gives a poor dynamic performance.

3.4.2 Vector control

To overcome the problems of the scalar control strategy mentioned above, rather than using the steady state relationships, the control scheme is based on the dynamic equations of the converter connected to an ac grid. A simplified vector control configuration is shown in Figure 3-12.

In this approach, the instantaneous supply voltage and current in the a-b-c three-phase ac system are measured and transformed to two-phase ac system by using the α-β transformation (described in section 3.3). The instantaneous angle,θ, corresponding to the rotating angle of the supply voltage is extracted from the transformed voltages, V_α and V_β. This angle is used as the reference angle for the transformations in order to synchronise the transformed signals with the supply voltage reference. With the angle θ, the voltage and current in α-β frame are further transformed to two dc signal components in the d-q synchronous reference frame which rotates at the ac grid supply voltage frequency [59].

In d-q control, if the d-axis voltage is aligned with the vector of the grid voltage, the d and q-axis current components account for the active power current and reactive power current respectively. In Figure 3-12 the DC-link voltage is kept reasonably constant by the DC-link voltage controller. The output from the DC-link voltage control gives the demand for active power. A reactive power resolver, which employs the measured grid voltages, is used as an outer control loop to set the reactive power demand in order to keep the voltage at the point of common coupling constant. The resulting voltages from

the control-loops are used as the input reference for PWM generator to produce the associated voltages at the ac terminals of the converter.

Therefore, using the vector control strategy, the ability to control the d and q-axis components separately leads to the direct control of the active and reactive power in order to improve the performance of the control loop during the transient period. Controlling the d-q DC quantities also enables the system to remove steady state error.

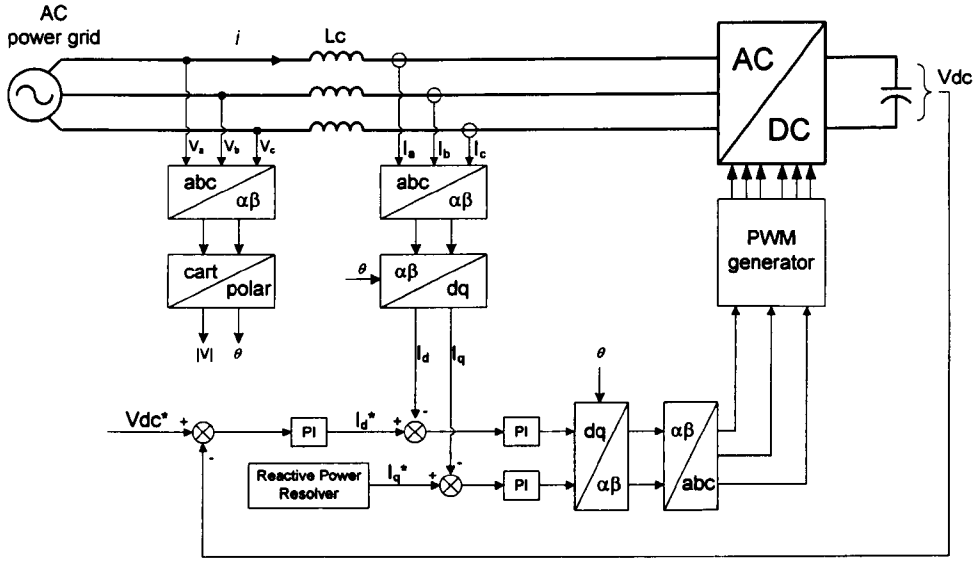

Figure 3-12 A simplified vector control strategy

The vector control strategy has been adopted for STATCOMs, as documented in [14-19, 21, 59-61], and is also preferable for this project.

3.4.3 Control design

Consider the equivalent circuit for the ac side of the STATCOM in Figure 3-8, where the direction of line currents indicating the STATCOM is absorbing power from the ac grid side. Therefore, deriving dynamic equations gives

$$\begin{bmatrix} V_a \\ V_b \\ V_c \end{bmatrix} = L\frac{d}{dt}\begin{bmatrix} i_a \\ i_b \\ i_c \end{bmatrix} + R\begin{bmatrix} i_a \\ i_b \\ i_c \end{bmatrix} + \begin{bmatrix} V_{a\_c} \\ V_{b\_c} \\ V_{c\_c} \end{bmatrix} \tag{3-12}$$

Applying the d-q transformation to Equation (3-12) gives

$$V_d = L\frac{dI_d}{dt} + RI_d - \omega_e LI_q + V_{d\_c} \tag{3-13}$$

$$V_q = L\frac{dI_q}{dt} + RI_q + \omega_e LI_d + V_{q\_c} \tag{3-14}$$

where ω_e is angular frequency of the rotating reference frame.

Consider the dc side of the STATCOM in Figure 3-10, the value of the DC-link voltage is dependent on the instantaneous power flowing along the line. Neglecting the losses (line losses, DC-link losses and switching losses) and using RMS values, the following equations can be written in the d-q reference frame where the q-axis voltage is zero as mentioned earlier.

$$\begin{aligned} I_{dc}V_{dc} &= 3V_dI_d \\ V_d &= m\frac{V_{dc}}{2\sqrt{2}} \\ I_{dc} &= 3m\frac{I_d}{2\sqrt{2}} \\ C\frac{dV_{dc}}{dt} &= I_{dc} - I_{bb} \end{aligned} \tag{3-15}$$

Where I_{dc} represents the associated dc side current of the STATCOM, I_{bb} represents the current flowing to a dc load explained in the chapter 4, and m is the converter's modulation index.

According to the algebraic definitions in Equation (3-13), (3-14) and (3-15), the equivalent circuit of the STATCOM can be illustrated in the d-q reference frame as shown in Figure 3-13.

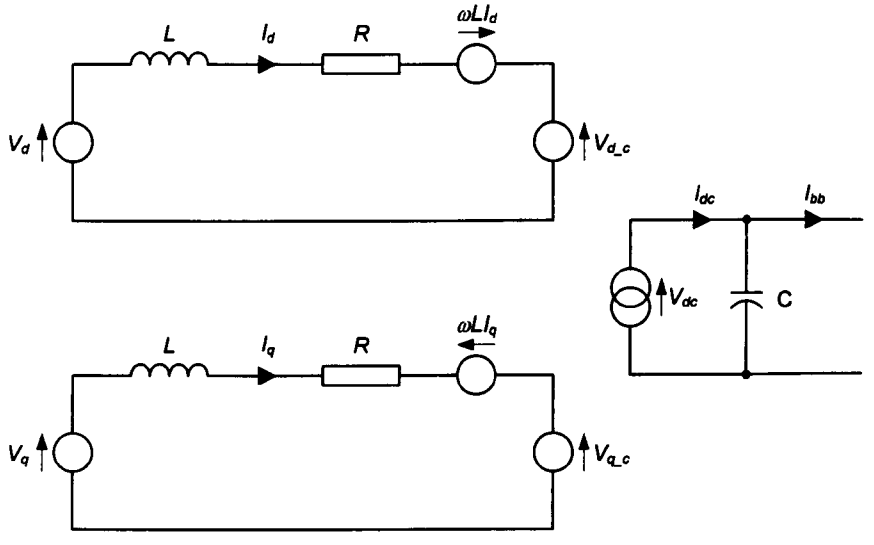

Figure 3-13 The d-q frame equivalent circuit diagram of STATCOM

According to Figure 3-13 and the associated equations, there are two control schemes – current control and DC-link voltage control. The current control will be applied to control I_d and I_q according to the desired active and reactive power demand, whilst the DC-link voltage control is applied to maintain the DC-link voltage constant during the operation of the STATCOM in order to allow the current control to operate in the linear region. Therefore, the overall control structure for the STATCOM in the rotating d-q reference frame is shown in Figure 3-14.

In the overall control structure for a STATCOM in Figure 3-14 shows that the output of the DC-link voltage control produces the demand for the active power current to flow between the ac grid and the converter, while the reactive power current demand is produced by an additional outer loop controller In this project, V_{pcc} controller is used to set the demand for the reactive power

current flowing to the ac grid – i.e. the amount of reactive power needed for the ac grid voltage compensation.

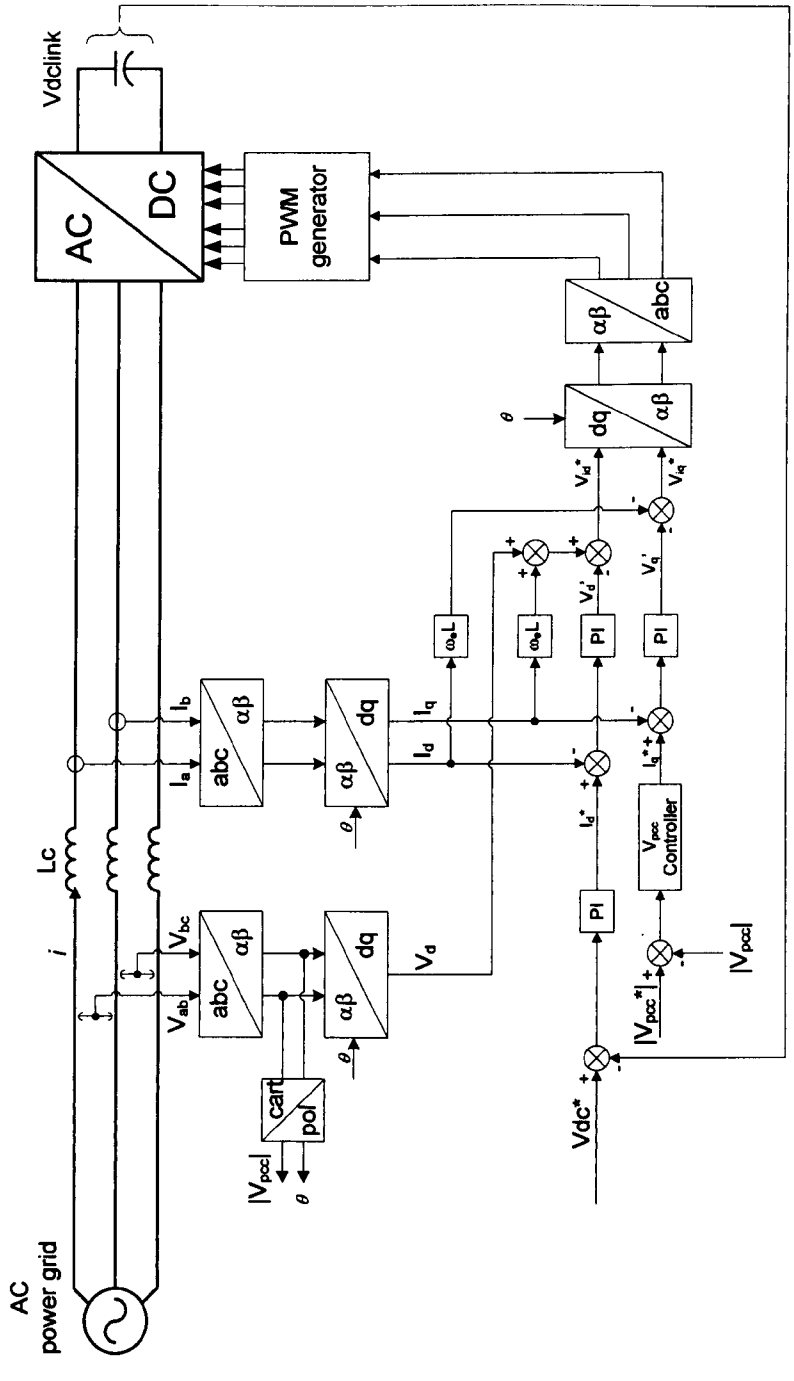

Figure 3-14 Control structure for STATCOM

Consider the principle described above. There will be three closed loop controls designed for the proposed STATCOM – current control, DC-link voltage control, and V_{pcc} control. A coupling reactor L=10mH with R=0.1Ω is used for the experimental validation described in chapter 5. Therefore, closed loop current control bandwidth of around 100Hz is desired. In order to avoid the effect on the dynamics of the current control loop, DC-link and V_{pcc} control loop must be designed to have a much lower bandwidth. For this project the control loop bandwidth of around 15Hz is preferable to regulate the DC-link and V_{pcc} voltage.

A 5 kHz switching frequency is used, and this is also the sampling frequency. It is at least twenty times greater than the required bandwidth. Therefore, the influence of sampling time is ignored, and the digital controllers for the current, DC-link voltage, and V_{pcc} can be designed in the s-domain [62, 63] as described in the next sections.

3.4.3.1 Current control design

Equation (3-13) and (3-14) defines again the voltage equations in a rotating reference frame aligned to the voltage vector.

$$V_d = L\frac{dI_d}{dt} + RI_d - \omega_e L I_q + V_{d\_c} \tag{3-16}$$

$$0 = L\frac{dI_q}{dt} + RI_q + \omega_e L I_d + V_{q\_c} \tag{3-17}$$

For control purposes, the voltage source converter needs to produce the associated output voltage according to the reference voltage signal determined from Equation (3-16) and (3-17) as shown in the following equations.

$$V_{d\_c}^{*} = -V_d' + (\omega_e L I_q + V_d) \tag{3-18}$$

$$V_{q\_c}^{*} = -V_q' - (\omega_e L I_d) \tag{3-19}$$

Noting that,

$$V_d' = L\frac{dI_d}{dt} + RI_d \tag{3-20}$$

$$V_q' = L\frac{dI_q}{dt} + RI_q \tag{3-21}$$

The current controller will determine the voltage demand, V_d' and V_q', to be used in order to calculate the reference voltage in Equation (3-18) and (3-19). Therefore, the plant for the current control loop design can be derived as in Equation (3-22).

$$\frac{I_d(s)}{V_d'(s)} = \frac{I_q(s)}{V_q'(s)} = \frac{1}{R + sL} \tag{3-22}$$

By using this plant, a standard design procedure can be applied with the block diagram for the current control loop as given in Figure 3-15, where I represents I_d or I_q, and V' represents V_d' or V_q'.

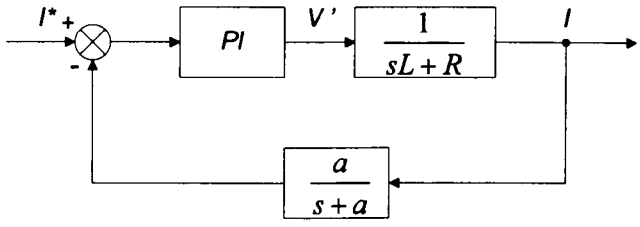

Figure 3-15 Current control loop

In Figure 3-15 an anti-aliasing filter (low-pass filter with the cut-off frequency of 1540Hz) is used in order to remove high frequency switching noise. This control loop is designed using MatLab SISO (Single Input Single Output) toolbox [45], with a damping ratio ζ=0.7 and the closed-loop bandwidth of 104Hz. The resulting current controller is given in Equation (3-23).

$$C(s) = \frac{6.01(s + 300)}{s} \tag{3-23}$$

For digital control, the controller transfer function in s-domain as in Equation (3-23) function is converted to z-domain equation using MatLab bilinear (Tustin) approximation, resulting in the controller in z-domain given in Equation (3-24).

$$C(z) = \frac{6.19z - 5.83}{z - 1} \tag{3-24}$$

3.4.3.2 DC-link voltage control loop design

According to the Equation (3-15), the plant for the DC-link voltage control design is given in Equation (3-25). In the experimental rig V_{pcc} is $110V_{rms}$ line-to-line voltage, the DC-link voltage will be regulated at 400V. Therefore, the modulation index (m) of the PWM converter is approximately 0.5.

$$\frac{V_{dc}(s)}{I_{dc}(s) - I_{bb}(s)} = \frac{1}{sC} \tag{3-25}$$

In the experimental setup, a low-pass filter with the cut-off frequency of 120Hz is used in the DC-link voltage measurement, and is therefore added in the feed back path of the control design. The cut-off frequency is chosen with a compromise between the speed of dynamic response of the DC-link control and the filtering of a high frequency switching noise. According to the plant in Equation (3-25) and the relationship of the STATCOM's dc-side current (I_{dc}) and the d-axis current (I_d) stated in Equation (3-13), the closed loop control design is shown in Figure 3-16. The standard PI controller obtained from this control loop design with a damping ratio ζ=0.7 and the bandwidth frequency of 12 Hz is then given in Equation (3-26).

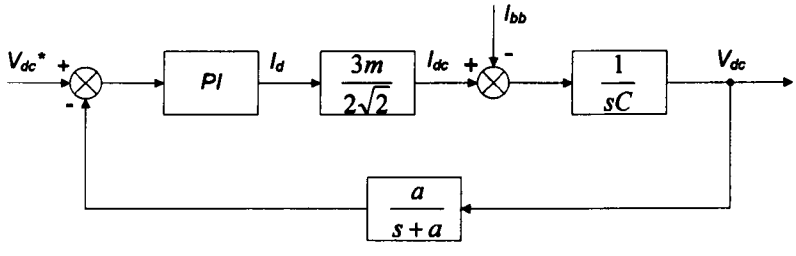

Figure 3-16 DC-link voltage control loop

$$C(s) = \frac{0.127(s + 47.2)}{s} \tag{3-26}$$

Using MatLab bilinear approximation transforms this s-domain controller function to z-domain function as shown in Equation (3-27).

$$C(z) = \frac{0.1276z - 0.1264}{z - 1} \tag{3-27}$$

3.4.3.3 V_{pcc} control loop design

To regulate the magnitude of the V_{pcc} in the power system shown in Figure 3-18 the STATCOM should introduce the optimum amount of the reactive power to the ac grid at PCC. As the change in the magnitude of V_{pcc} is due to the change of the current flowing between the three phase ac power supply and the PCC bus, the control concept for the V_{pcc} is therefore to use a small-signal model, derived in Appendix B and shown in Equation (3-28), that relates the change in the magnitude of the V_{pcc} to the reactive current in the line.

$$\frac{\Delta V_{pcc}}{\Delta I_q} = \omega_e L_s \tag{3-28}$$

Where ω_e is the angular frequency of the rotating reference frame, ΔV_{pcc} is the change in voltage at PCC, ΔI_q is the change in reactive power current flowing in the line, and L_s is the leakage inductance of the line (5 mH).

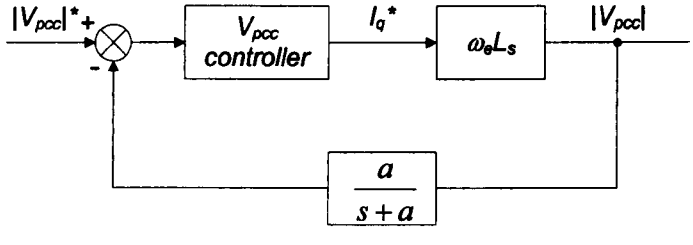

Figure 3-17 V_{pcc} control loop

The same low-pass filter as used in the current control loop is added in the control design in Figure 3-17, with the cut-off frequency of 1540 Hz. Using MatLab SISO toolbox, V_{pcc} controller is designed with a damping ratio ζ=0.7 and the bandwidth frequency of 9.75 Hz is shown in Equation (3-29).

$$C(s) = \frac{33.4(s + 30.3)}{s(s + 5)} \tag{3-29}$$

In designing the V_{pcc} controller as the open-loop transfer function results in a very high close-loop control bandwidth, with the aim for a low bandwidth controller in order to avoid the effect on the dynamic of the STATCOM current controls, an extra pole (s+5) is added to reduce the bandwidth. This additional pole gives the flexibility to design the controller resulting in a low bandwidth controller as desired.

The transfer function of V_{pcc} controller is then discretised using the bilinear transform in MatLab, resulting in a z-domain function shown in Equation (3-30).

$$C(z) = \frac{0.003368z^2 - 2.035e^{-5}z - 0.003348}{z^2 - 1.999z + 0.999} \tag{3-30}$$

3.5 Simulation of the STATCOM

The simulation study is implemented with the scenario based on the ac power system similar to the experimental validation setup described in chapter 5. The power circuit diagram for the simulation of a power system using STATCOM is shown in Figure 3-18. The simulation was carried out using MatLab/Simulink software package, and all the power circuit component models can be found in SimPowerSystems BlockSet. For the STATCOM model, the 3-arm IGBT-Diode Bridge is used and all its parameters are set as the MatLab/Simulink default.

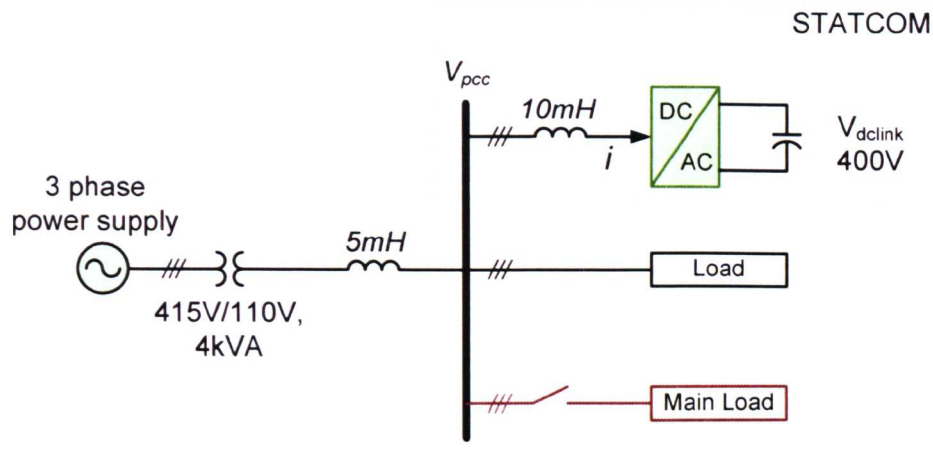

Figure 3-18 Power circuit diagram setup for simulation study

To interface the supercapacitor energy storage system (SCESS), described in chapter 4, to the STATCOM unit at the DC-link capacitor, the DC-link voltage has to be the same voltage rating as the SCESS. The supercapacitor terminal voltage is 200V, and the dc-to-dc converter in the SCESS unit boosts this voltage level up to the optimum at 400V. The STATCOM's DC-link voltage is therefore set to 400V.

To ensure that the PWM converter is operating in a linear region, the line-to-line peak voltage of the three phase supply must be lower than the DC-link voltage of 400V. A step-down transformer is used as shown in Figure 3-18 to lower the three-phase supply voltage to 110V - V_{pcc} is therefore rated at 110V.

An additional 5mH inductor is connected between the transformer and the V_{pcc} bus in order to highlight the voltage drop due to load current during the experiments. However, this additional inductance (including the leakage inductance of the transformer and the inductance of the power supply) will be the cause of an increase in the switching noise appearing on the voltage waveforms as explained by the equivalent circuit diagram shown in Figure 3-19.

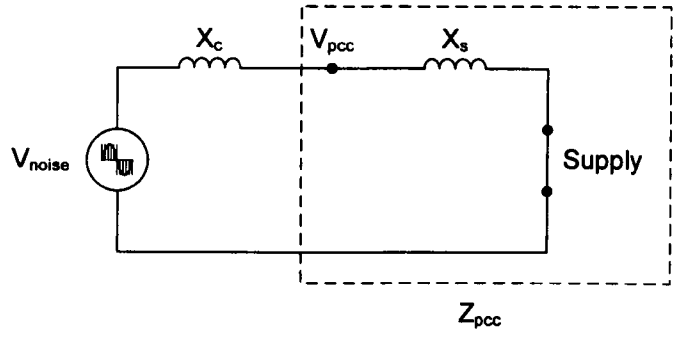

Figure 3-19 An equivalent circuit diagram of the voltage divider formed by the additional reactor, X_s, and the coupling reactor, X_c.

In Figure 3-19, Z_{pcc} is the equivalent impedance at PCC bus. V_{noise} represents the high frequency switching noise produced by the STATCOM. It can be seen in the equivalent circuit diagram that an increase in the noise ripple appears on the voltage waveforms at V_{pcc} and is proportional to the value of Z_{pcc}, which is equal X_s.

In the real application this switching noise would be reduced by using a passive switching frequency filter. For simplicity, in this system a light load (50Ω resistance) is connected in parallel with the X_s as shown in Figure 3-20 (therefore in Figure 3-18). Due to the smaller equivalent impedance Z_{pcc}, the noise ripple appearing on the waveforms of V_{pcc} will be reduced.

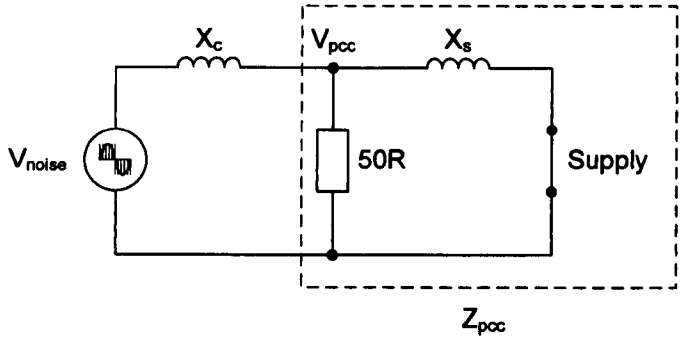

Figure 3-20 An equivalent circuit diagram showing Z_{pcc} is reduced by the 50 ohm resistor connected at V_{pcc}.

During the simulation, the main load of approximately 7A will be switched to PCC bus causing a sudden change in the load current, and to see the dynamic response of the system.

In the simulation, the control scheme was digitally implemented in a discrete closed loop control system with a sampling frequency of 5 kHz, which was generated by and synchronised with the standard sinewave PWM switching signal. For comparison, the simulation was carried out with and without the proposed STATCOM as in section 3.5.1 and 3.5.2 respectively. The results show the benefits to the ac power system as explained in the next sections.

3.5.1 Simulation of a power system without VAr support

First of all, for comparison purposes, the simulation of the system without VAr support was carried out. The overall results (V_{pcc}, load current, supply current, support current, and DC-link voltage) are shown in Figure 3-21, and for clarity the magnitude of V_{pcc} is plotted in Figure 3-22.

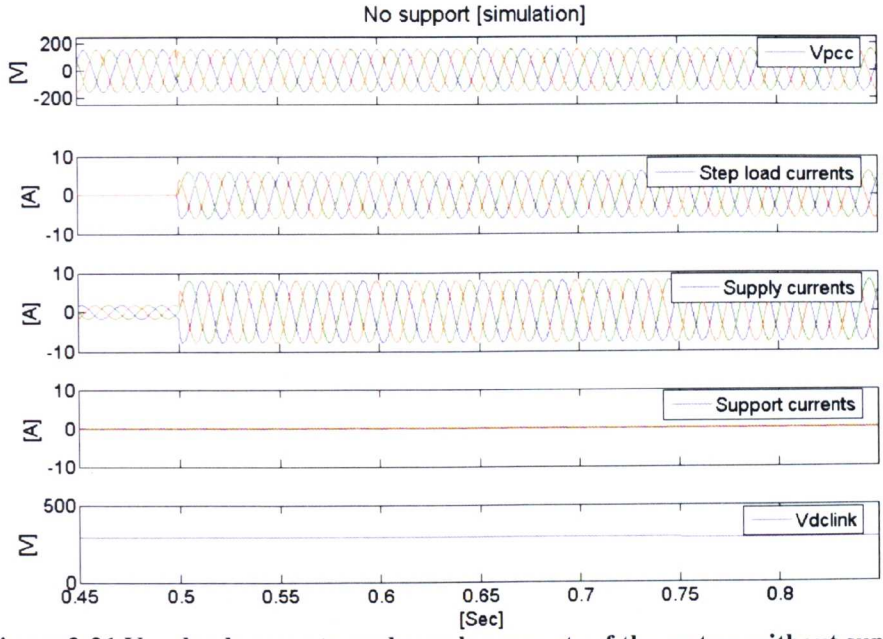

Figure 3-21 V_{pcc}, load currents, and supply currents of the system without support [simulation]

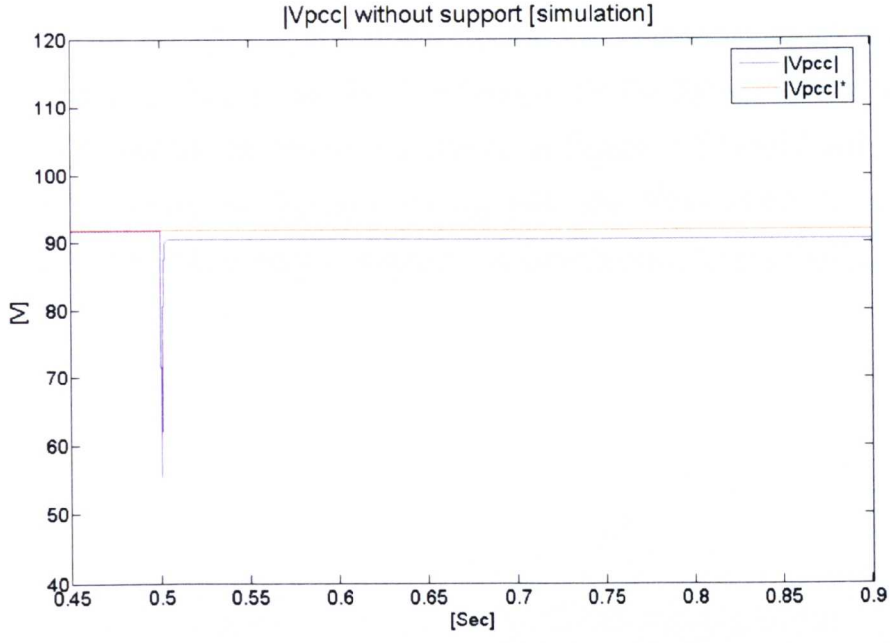

Figure 3-22$|V_{pcc}|$ of the system without support [simulation]

In Figure 3-21 from the beginning to time t=0.45s an approximate 1.5A supply current is seen as the current for the light load. At time t=0.45s the main load is switched on, and a sudden change of the load current from 1.5A to approximately 10A can be seen. In this simulation the DC-link voltage remains at 200V as no power is drawn from the DC-link, V_{pcc} drops as shown in the top trace of Figure 3-21, and its magnitude can be seen clearly in Figure 3-22. The drop of V_{pcc} simply indicates that there is a voltage drop across the system line inductance L_s relating to the load current drawn from the 3-phase ac power supply. The overall result also indicates that all of the load demand is fully supplied by the three-phase power system.

3.5.2 Simulation of a power system using a conventional STATCOM only

To see the benefits of the instantaneous reactive power compensation to the same power system, the simulation was carried out with a conventional STATCOM connected at V_{pcc} bus. The amount of the reactive power flowing to maintain the voltage V_{pcc} is regulated by the V_{pcc} controller, which employs the magnitude of V_{pcc} to set the I_q reference for the STATCOM's current control. The simulation results are shown in Figure 3-23 and Figure 3-24. From the beginning of the test at time t=0s the STATCOM is enabled, therefore the DC-link voltage is regulated at the reference level ($400V_{dc}$).

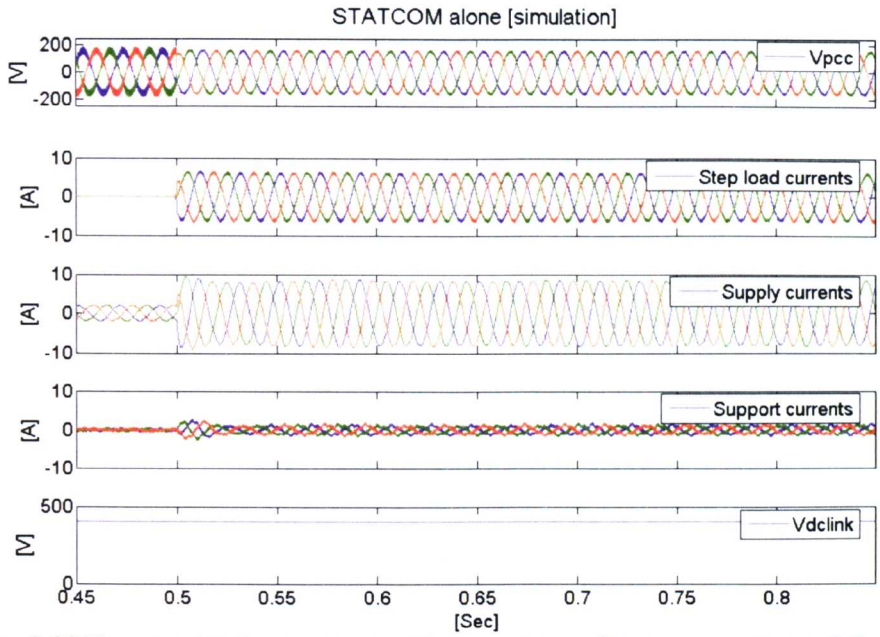

Figure 3-23 V_{pcc}, step load currents, supply currents, and support currents of the system with STATCOM only [simulation]

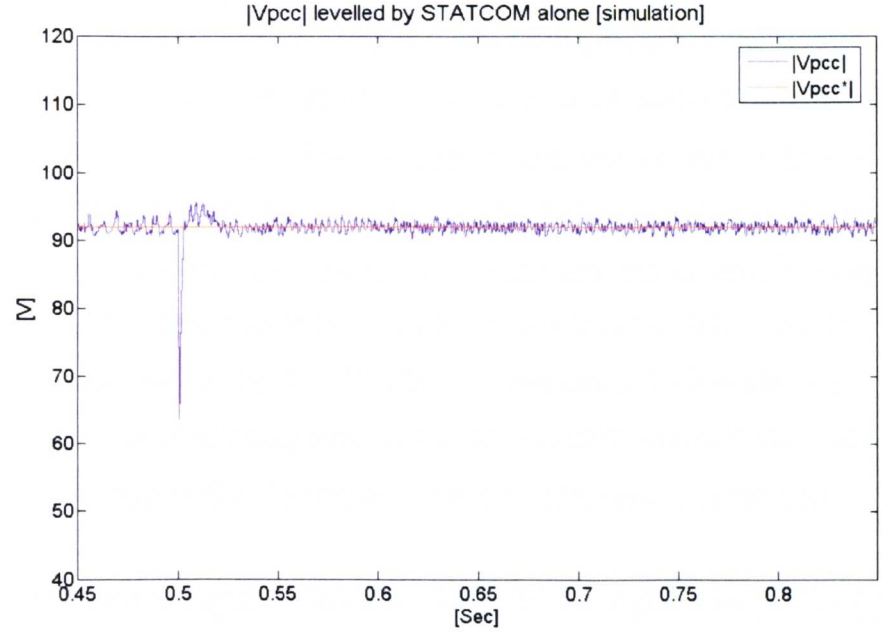

Figure 3-24 $|V_{pcc}|$ of the system with STATCOM only [simulation]

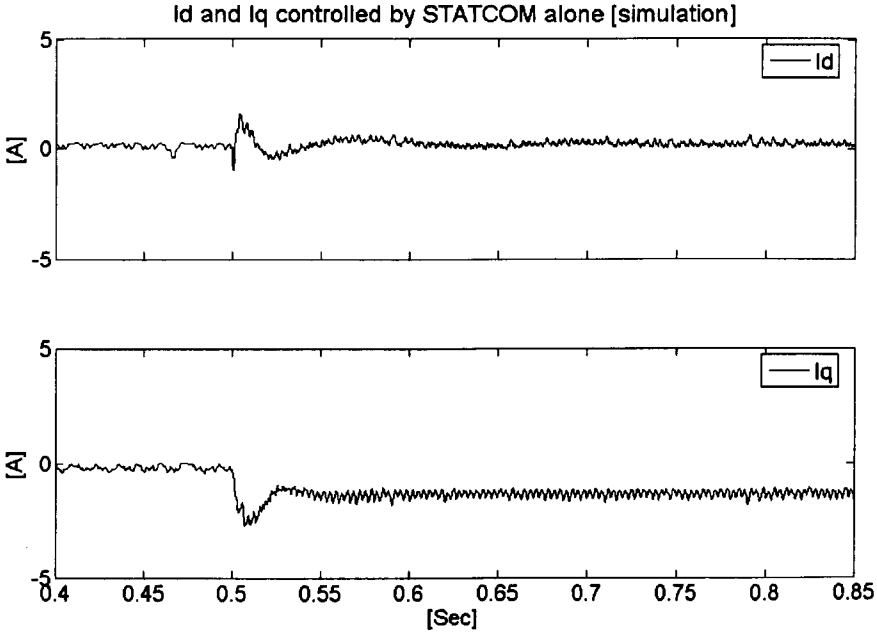

Figure 3-25 The controlled Id and Iq for the system with STATCOM only [simulation]

A comparison of the results obtained from the system without the STATCOM (Figure 3-23 and Figure 3-24) and the results from the system with the STATCOM (Figure 3-21 and Figure 3-22) shows that with the sudden change of load current due to the main load connected at time t=0.45s the DC-link voltage and V_{pcc} are regulated reasonably constant at their reference values (V_{dc}*=400V and V_{pcc}*=92V phase voltage). A noticeable support current can be seen in Figure 3-23 (current in a-b-c reference frame) and in Figure 3-25 (current in d-q reference frame). This support current is the reactive power current generated by the STATCOM. As expected, before the main load is turned on, a high frequency switching ripple appears on the voltage waveform. However, as expected it is reduced when the main load is connected.

From the result in Figure 3-23, it is clear that the 3-phase ac power system is still supplying all the full load real power demand as seen in the 3rd trace of Figure 3-23 - approximately 10A. Therefore, as expected, the STATCOM supports only the reactive power, but not the real power. In the next two

sections, the SCESS is added to the STATCOM with the aim to compensate both real and reactive power dynamically.

3.6 Conclusions

In this chapter, the STATCOM based on the voltage source converter and its proposed control has been explained. Vector control according to the relationship of the instantaneous power theory is chosen for this project. As expected, the independence of the control of the instantaneous real and reactive power is confirmed by the simulation results explained briefly in this chapter.

The simulation results of a power system using a STATCOM confirm that the proposed control concept is satisfied. The results shown in this chapter also confirm that STATCOMs can be used to compensate the reactive power dynamically in the ac power system. For this project, the reactive power flowing in order to compensate for V_{pcc} is regulated by the V_{pcc} controller, which designed using a small-signal model derived from the equivalent circuit diagram of the system.

However its capability to compensate the real power is limited due to a small amount of the energy in the conventional DC-link capacitor. In order to increase its ability to compensate real power, the STATCOM will be enhanced with supercapacitor energy storage system, and described in the next chapter.

Chapter 4

STATCOM with SuperCapacitor Energy Storage System

4.1 Introduction

This chapter presents the proposed STATCOM with energy storage. Section 4.2 presents an overview of electrical energy storage technologies. Section 4.3 presents the proposed energy storage system, the supercapacitor energy storage system (SCESS). The STATCOM plus SCESS is described in section 4.4. In section 4.5, the simulation of an ac system with STATCOM plus SCESS is presented with results. Finally the conclusions are documented in section 4.6.

4.2 Electrical energy storage technologies

Integrating energy storage into ac power systems provides the ability to store electrical energy at times of low demand or when generation cost is low. The electrical energy storing process is also dependent on the ac power system environment. The stored energy is usually released at times of high demand, normally with a high generation cost, or at times of specific events where the potential generation capability cannot support demand. Electrical energy storage can potentially improve power system stability, providing frequency and voltage regulation benefits. Energy storage can help the power system to cope with the impacts of loads, resulting in less interruption, and therefore giving an improvement in reliability. Furthermore, in economic terms, energy storage is a promising technology to help reduce investment costs for building an additional generation reserve. Having energy storage on board will reduce equipment cost as the power ratings can be lower when the peak load is reduced.

There are many kinds of energy storage technologies and they are different in their characteristics. Therefore the integration of energy storage to a specific ac power system is dependent on these characteristics and also the nature of the system under consideration.

This section provides brief descriptions of different types of energy storage with the potential for improving power system performance. Pumped-hydro energy storage, compressed-air energy storage (CAES), superconducting magnetic energy storage (SMES), flywheel energy storage (FES), Fuel Cells, battery energy storage (BES), and supercapacitor energy storage (SCES) are described.

4.2.1 Pumped-hydro energy storage

In this approach the energy is stored in a mass of water which is moved to a relatively high reservoir thus giving it potential energy. The stored energy will be converted to electrical energy by releasing the elevated water to a lower reservoir through hydro turbines i.e. converting the potential energy to kinetic energy. This process (discharge process) will normally take place when the generation does not match demand or when the price of the generation is high [64-66].

During the period of low generation cost the water will be pumped up from the lower reservoir to the higher reservoir. The reversible pump-turbines can be used as a single unit motor-generator set or using separate motors and turbines. Therefore the charge process will consume electrical energy, but however with a lower price rate. For the pumped hydro storage with adjustable speed machines installed, the system can also regulate the overall frequency.

The amount of stored energy available depends on the physical structure. Pumped-storage energy storage is the largest energy storage usually found in ac power systems, and can supply the highest amount of electrical energy compared to the other forms of energy storage. However, by its nature, the associated geography can reduce the efficiency of this energy storage [65, 66].

4.2.2 Compressed-air energy storage (CAES)

In a compressed-air energy storage system, the energy is stored in the form of compressed air using a compressor. The compressed air will be stored in the different kinds of reservoirs such as naturally occurring caverns, mine caverns, or artificial rock reservoirs [67, 68].

The compressed air will be used together with natural gas to power a turbine generator in order to generate electrical energy during the discharge process. To store the energy, the reverse process is carried out during charging - electrical energy is converted to mechanical energy powering the compressor to compress air (therefore to store energy). In a CAES system, a reversible turbine must be used, which requires special mechanical gears in order to allow the turbines to operate in both directions. More information for the compressed-air energy storage can be found in[67, 68].

Apart from the pumped-storage hydroelectric energy storage, compressed-air energy storage has the highest capacity. Also, with the nature of the reservoirs built as closed system, the CAES can store energy for longest period compared to the others. However in the CAES system a proper geological structure is needed as most of the reservoirs are built underground and that is of a critical concern.

4.2.3 Superconducting magnetic energy storage (SMES)

In a superconducting magnetic energy storage system, an electrical coil made from superconductor material is used as a medium to store energy in the form of a magnetic field (electrical form) surrounding the coil. The electrical energy is stored according to the current circulating through the superconductor coil. By using a superconductor material, the coil is a fairly losses-less component and is therefore expected to produce a magnetic field without losses. Using power electronics, the SMES is charged and discharged electrically to the power system. Therefore the SMES can provide a fast response to the demand change. More information can be found in research work published in [69-72].

However, in a SMES system a refrigeration system is necessary to maintain the superconductivity of the coils. This incurs losses. The superconductivity of the coil is sensitive to change in temperature, and problems with the stability of magnetic field have been reported [69]. The potential force produced by the interaction of the current circulating in the magnetic coils can be an obvious problem to deal with. A special structure must be provided to support this magnetic force. Therefore, because of the auxiliary systems, the SMES has high maintenance requirements, and is therefore very expensive.

4.2.4 Flywheel energy storage (FES)

A flywheel is a mechanical device that stores kinetic energy in a rotating mass. In flywheel energy storage systems, a motor-generator set is required to convert between mechanical and electrical energy. In the charging process, the energy is stored when the motor-generator set acts as a motor in order to convert electrical energy to the kinetic energy as a rotating mass stored in flywheel. This is achieved by accelerating the flywheel to higher speed. Conversely, in discharging process, the motor-generator set acts as a generator to convert the rotating mass back to electrical energy for the ac power network by decelerating the flywheel.

Therefore, in the FES, variable speed capability is necessary and additional power electronic control is required to control the speed of the flywheel. Details of the FES system are described in [68, 72-76].

The overall efficiency of the FES is defined by losses caused by the flywheel rotating friction. As a flywheel is normally built with light-weight and high strength composite material, therefore it must be rotating at a very high speed in order to store more energy.

According to the basic principle of FES whereby low bearing losses are essential, superconducting bearings are introduced to reduce friction losses, and this also introduces an extra cost. Besides, a very high speed rotating flywheel needs additional support for safety issues. In the long term, the high speed operation of flywheels will result in problems such as rotational losses and the increasing maintenance cost[68, 72].

4.2.5 Fuel cells

One of the promising energy sources is hydrogen which can be converted directly into electrical energy using a fuel cell. Fuel cells have the potential to store a higher energy per kilogram of fuel cell weight than that stored in batteries [77]. By using hydrogen, the fuel cells also produce clean and sustainable electrical energy [77-80].

One of the most important factors to be considered is the method used to produce hydrogen. If the production of hydrogen is powered from the electrical grid the electricity may well be produced by fossil fuel sources with the associated problems. However, the electrical energy may be created from renewable energy such as wind, solar or hydroelectric that has no polluting emissions.

The storage of hydrogen is also important and is a challenge for the use of fuel cells. The potential technologies that have been currently applied to hydrogen storage are compressed gas, liquefaction, absorption in metal hydrides, and adsorption in carbon nanotubes. Hydrogen storage by high-pressure compression is not safe, particularly for domestic and transport application means while liquefaction needs large amount of energy, and therefore both of these methods thus require the development of further technical solutions. Although the absorption in the form of chemical hydrides will offer safe

hydrogen storage, this method however results in slow kinetics and requires high temperature to release the stored hydrogen [81, 82].

At present, the physisorption of hydrogen in a porous carbon surface is of interest. Naturally, carbon is known to adsorb significant quantity of hydrogen due to its characteristic of attractive force between molecules. Porous carbon has a very high surface area due to its nanostructure technology, and is therefore able to store a relatively large amount of hydrogen [81]. Adsorption in carbon nanotubes is therefore a promising technology for storing hydrogen.

Many kinds of fuel cells have been developed such as alkaline fuel cells, PEM (Polymer Electrolyte Membrane) fuel cells, and methanol fuel cells. The alkaline fuel cell gives higher power but uses a poisonous electrolyte[78]. Methanol liquid fuel comes with technology that is environmentally safe and generates high power, but at a higher cost [79]. PEM fuel cells seem to be a promising technology that has been continuously developed and is now seen as a distributed power source in power systems [78].

Although the fuel cells are the potential technology for high energy systems, their nature is as an energy-conversion device, not an energy storage device[79]. For the charging process, they rely on the process of storing primary fuel (hydrogen), where the process can take a long time.

The electrical energy produced by fuel cells is dc and therefore requires a power electronic converter if it is to be interfaced to an ac grid. For PEM fuel cells, the discharging characteristics have been reported by [83] showing that the speed of delivery of power is quite slow. Therefore, rather than using fuel cells alone, a combination of fuel cells with other energy storage such as supercapacitors or batteries as a hybrid system is becoming a developing technology.

4.2.6 Battery energy storage (BES)

A battery is an electrochemical device that stores electrical energy in chemical form. Basically, a battery has two electrodes immersed separately in an electrolyte. During the charging process, electrical energy from a dc power source must be supplied to the battery's terminals which are directly connected to electrodes. The potential between electrodes causes an internal chemical reaction in the electrolyte. As a result, electrical energy transferred to the battery is electrochemically absorbed and stored. In the discharge process, batteries convert the stored energy back to electrical energy when the load (or equivalent) is connected to its terminals – they reverse the internal chemical reaction.

In order to store and utilise the energy in a power system, a dc-to-ac converter is required to connect the BES to the ac power grid. When required, a combination of series and parallel connected batteries can offer high energy density and high capability. There are several kinds of battery technologies can be designed for power systems applications. The three latest technologies are briefly described below, and greater details can be found in [67, 72, 75].

The Lead-acid battery has been developed for large energy storage and fast charge/discharge. However its charge/discharge characteristic has to be improved. This kind of batteries represents a low-cost option for large storage low energy density, but with limited cycle-life [72].

The Sodium-sulphur (Na-S) battery has been developed with the aim to improve the energy density of the batteries. For example in [66, 84] show that Na-S battery has energy density 4 times higher than that of the lead-acid battery. It has a solid electrolyte and liquid metal negative electrode, and the internal chemical reaction varies according to the changing temperature.

During charging, Na-S battery develops a very high resistance that can lead to failure of the battery, and its lifetime is quite short [67].

The Redox flow battery has been developed for use as a large energy storage facility in power systems. Electrolytes are pumped to electrodes circulating separately from each other. Therefore, the whole system generates a considerable noise originated from the circulating and cooling system. The operation looks like a generating plant rather than a stationary battery energy storage unit. The maintenance cost due to the circulating and cooling system and an environmental impact due to the noise generated are critical factors to be considered if the Redox flow battery system is to be installed [67].

It can be summarised that although the battery energy storage system seems to be a promising technology for near-term power system applications, environmental controls due to toxic product from the chemical reaction and future management of the used-batteries are clearly critical. In technical terms, for some specific applications, the rapid charging characteristic has to be improved. Due to the fact that the reaction inside batteries is sensitive to temperature[83], their lifetime and cycle life are quite short. Depending on the chemical reaction inside, batteries have a high maintenance cost.

4.2.7 Supercapacitor energy storage (SCES)

Supercapacitors or ultracapacitors are electrochemical energy storage devices that store energy electrostatically by means of separating (polarising) positive and negative ions in the electrolyte from each other. Unlike the conventional capacitors, its electrodes are specially made from highly porous materials immersed in electrolyte providing much more space for the ions to be separated in the cell [85, 86]. For clarity, an insight into supercapacitor cell is simplified and shown in Figure 4-1.

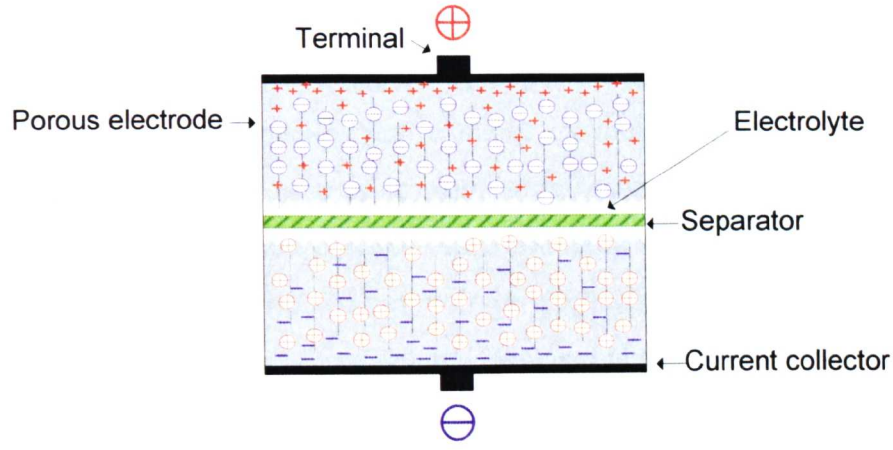

Figure 4-1 Insights into a simplified supercapacitor cell

In Figure 4-1 the energy storage mechanism starts when a dc voltage is applied to the supercapacitor terminals. In order to produce electric field distributed between the two terminals, current collectors are attached directly to both positive and negative terminals. The porous material is attached to the current collectors. Therefore if the voltage is applied to the terminals, the voltage potential will distribute fully over the porous material. Thus, due to the voltage applied across the terminals, the porous material becomes an activated electrode (positive and negative electrodes separated by a separator). The electrolytic ions under the influence of the electrical field provided by the activated electrodes are thus drawn to the opposite polarity. Positive ions travel into and attach to the negative porous electrode, whilst the negative ions travel to and attach to the positive porous electrode, resulting in energy being stored in the form of an electric field between the electrodes and ions. A separator which the ions can travel through is used to separate between the activated electrodes. Two layers of the electric field appear in the cell, and therefore they are called electrochemical double layer capacitors (EDLC). To discharge, the reverse process converts the stored energy into electrical energy as fast as its charging process. There is no chemical hazard produced from the reaction inside the cell, although it is an electrochemical device.

Supercapacitors have been used for decades in applications such as low-voltage low power back up. Recent advances in material technology have transformed the supercapacitor into a major technology back up for higher power applications, and as a promising energy storage device. In terms of dynamic benefits, over their lifetime supercapacitors can charge and discharge much faster than batteries. They can be recharged as fast as there are discharged. They can store energy at any level and at any level of voltage even at the condition of complete discharge [85] and provide a deep-discharge, with very little effect on their lifetime. Their cycle life is also much longer than that of battery.

In comparison to batteries, according to the report in [83], although batteries are cost effective and available in a large size range, their temperature sensitivity, maintenance requirements and limited cycle life make batteries less appealing for burst power applications, i.e. applications that require rapid charge/discharge characteristics.

When selecting an energy storage device for the STATCOM application, energy content becomes an important factor and varies with discharge rate. Batteries have a better energy content with long-term discharge (for example the discharge over 60 minutes). However during short-term discharge (of 1 minute) the same battery has around 10 times lower energy content. During this short-term discharge supercapacitors have higher energy content, for example more than two times higher [83].

As supercapacitors find their applications in high power areas [87-90], the increase in competition in marketplaces and the increase in manufacturers will reduce their production costs, therefore the overall price of supercapacitors will be reduced.

In this project, for the reasons described above, the supercapacitor has been chosen as the energy storage device in order to improve transient performance

of the conventional STATCOM. Power electronics and associated control are required to interface supercapacitors to the STATCOM unit as presented in the following section 4.3.

4.3 Supercapacitor Energy Storage System (SCESS)

A standard STATCOM cannot supply any significant real power to the ac power system due to the limited energy stored in its conventional DC-link capacitor. Their DC-link voltage will drop rapidly when trying to inject real power to the power grid. Therefore this project employs supercapacitors as the main energy store.

However connecting the supercapacitors directly to the DC-link of the STATCOM will affect the performance of the STATCOM due to the DC-link voltage variation during real power injection to the power grid. When the STATCOM supplies real power to the grid, the supercapacitors discharge energy which results in the supercapacitor voltage dropping (also the DC-link voltage) and the energy is exported to the grid. If the DC-link voltage drops to the level that lower than the ac side line-to-line peak voltage value, the operation of the STATCOM will be stopped.

Therefore a bi-directional dc-to-dc converter is used for interfacing between the supercapacitors and the STATCOM's DC-link in order to keep the DC-link voltage constant when energy is exported to the grid, by controlling the transfer of stored energy from the supercapacitors to the power grid, and from the power grid to the supercapacitors. The power circuit of the dc-to-dc converter with supercapacitors (SCESS) is shown in Figure 4-2.

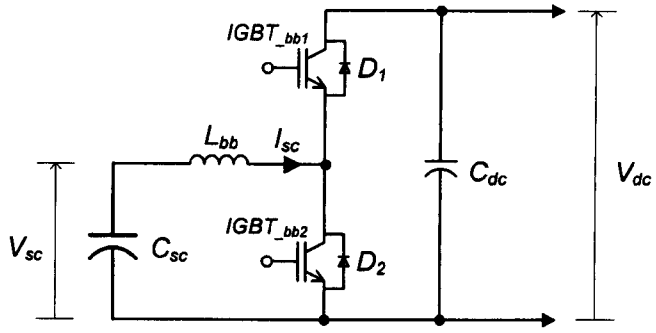

Figure 4-2 The power circuit of the SCESS

In Figure 4-2, C_{sc} is the supercapacitor unit comprising of 10 supercapacitor modules manufactured by ELIT connected in series, each module rated at 95F 20V 19kJ. C_{dc} is a conventional electrolytic DC-link capacitor. In order to utilise and store energy in the supercapacitor modules, two IGBTs with anti-parallel diodes, D, are used as switching devices. They are controlled using duty cycle-modulation in order to keep the DC-link voltage constant. The inductor L_{bb} is used as a medium to control the bi-directional power flowing between the DC-link voltage side V_{dc} and supercapacitor voltage side V_{sc}. The direction of supercapacitor current I_{sc} defines whether the SCESS is storing energy or utilising the energy.

4.3.1 Constraints on the operation of the SCESS

The aim of this application is to store energy in the supercapacitor modules and then deliver that energy to the ac power grid via the DC-link when required. The dc-to-dc converter will operate in "Buck Mode" to recharge the supercapacitor modules, whereas "Boost Mode" transfers the stored energy in supercapacitor modules to the DC-link.

In buck mode, according to the power circuit diagram shown in Figure 4-2 the energy storing or charging process is regulated by turning ON and OFF $IGBT_{\_bb1}$. When $IGBT_{\_bb1}$ is ON, I_{sc} flows transferring energy from the DC-

link side (C_{dc}) to stored magnetic energy in L_{bb}, when $IGBT_{bb1}$ is OFF, the induced back emf across L_{bb} causes D_2 to conduct allowing L_{bb} to release the energy to supercapacitors C_{sc}. As a result, the energy is transferred from the DC-link to the supercapacitor modules, and the amount of energy can be controlled through the duty cycle of the $IGBT_{bb1}$. During this process, the supercapacitor voltage, V_{sc}, is regulated. If it reaches the maximum limit, the charging process will be stopped.

In boost mode, the energy utilising or discharging process is regulated by turning ON and OFF $IGBT_{bb2}$. When it is ON, I_{sc} flows in the direction that first transfers the energy from supercapacitors C_{sc} to stored magnetic energy in L_{bb}, (V_{sc} acts as an energy supply for L_{bb}). When $IGBT_{bb2}$ is OFF, according to the potential at L_{bb}, D_1 conducts allowing L_{bb} to release energy to the DC-link capacitors, C_{dc}. Therefore, the energy in the supercapacitor modules is utilised by controlling the duty ratio of the $IGBT_{bb2}$. During boost mode operation, the DC-link voltage is kept constant at its rated voltage.

The supercapacitor voltage V_{sc} will drop to 0V if all the stored energy is utilised. However, this will affect the stability and efficiency of the operation of the dc-to-dc converter. Therefore a lower limit is placed on the supercapacitor voltage; if up to 75% of the stored energy is to be utilised, a reasonable minimum value for V_{sc} is 50% of the maximum value, i.e. the maximum voltage of the supercapacitor unit is set at V_{sc_max} = 200V (ten supercapacitor modules connected in series), and then V_{sc_min} =100V. The optimum point where the stored energy can be extracted from supercapacitors is at a duty ratio of about 0.5 for the dc-to-dc converter [47]. At this optimised operating point the DC-link voltage needs to be V_{dclink}= 400V.

4.3.2 Inductor design

By analysing current ripple, the value of the buck-boost inductor, L_{bb} in Figure 4-2 can be derived from the following equations. In boost mode, the DC-link voltage is expressed as in Equation (4-1) [47]. Assuming V_{sc} acts as a dc voltage source, and that $IGBT_{bb2}$ only is used for control, when $IGBT_{bb2}$ is ON, the inductor current which equals supercapacitor current Isc increases ideally with a ratio that can be calculated by Equation (4-2) (assuming the resistance of the inductor is negligible). When $IGBT_{bb2}$ is OFF, Equation (4-3) gives the reduction in inductor current (ΔI_L).

$$V_{dclink} = \frac{V_{sc}}{1-d} \tag{4-1}$$

$$\Delta I_{L(on)} = \left(\frac{V_{sc}}{L_{bb}}\right) T_{on} \tag{4-2}$$

$$\Delta I_{L(off)} = \left\{\frac{V_{sc}-\left(\frac{V_{sc}}{1-d}\right)}{L_{bb}}\right\} T_{off} \tag{4-3}$$

Where

V_{dclink} is the DC-link voltage, V

V_{sc} is the supercapacitor voltage, V

d is the duty cycle of $IGBT_{bb2}$

L_{bb} is the dc-to-dc buck-boost inductor, H.

$\Delta I_{L(on)}$ is the change in inductor current when $IGBT_{bb2}$ is on, A

$\Delta I_{L(off)}$ is the change in inductor current when $IGBT_{bb2}$ is off, A

T_{on} is the on-period of $IGBT_{bb2}$, Sec

T_{off} is the off-period of $IGBT_{bb2}$, Sec.

At steady state, assuming $\Delta I_{L(on)} = \Delta I_{L(off)}$ and continuous inductor current, the change in inductor current ΔI_L is expressed in Equation (4-4), where T is the switching period which equals $T_{on} + T_{off}$, also defined by $1/f_s$ (f_s is switching frequency).

$$\Delta I_L = \left(\frac{V_{sc}}{L_{bb}}\right) dT \tag{4-4}$$

To calculate the inductance L_{bb} using Equation (4-4), an acceptable range of ripple and duty ratio of the switching period must be specified. Normally the buck-boost converter is designed with a current ripple of 1% [47]. However, this can be relaxed for supercapacitors because the supercapacitor voltage can change between 95% and 105%, and therefore the desired ripple is set at 2%.

With the maximum power designed at 10kW and V_{sc_min} =100V (as mentioned in section 4.3.1), 2% of the maximum ripple current gives $\Delta I_{L(max)}$ =2A. Equation (4-4), then, gives the value of inductance at duty cycle of 1.0 (the maximum ripple occurs for a duty cycle of 1.0) and a switching frequency of 5 kHz; the required inductance is 10mH. A similar analysis has been applied to confirm that the ripple is limited to within 2% when operated in buck mode.

4.3.3 DC-link capacitor design

The DC-link capacitor is only required to function as a smoothing capacitor in order to limit voltage ripple during boost mode. In buck mode, energy will be stored in supercapacitor modules which have a very big capacitance. The design of the DC-link capacitor for this case is then focused on boost mode operation.

In boost mode when $IGBT_{bb2}$ is ON, it is the DC-link capacitor that supplies energy to the ac power grid – the supercapacitors transfer energy to L_{bb}. The

amount of charge Q stored in the DC-link capacitor decreases as it supplies the required real power via the STATCOM to the ac power grid, and the DC-link voltage drops. When $IGBT_{\_bb2}$ is OFF, the DC- link capacitor is charged from the SCESS. Therefore, the DC-link voltage increases to the control level. This cycle of store and supply of charge causes a ripple voltage, ΔV, written in Equation (4-5).

$$\Delta V = \frac{\Delta Q}{C_{dc}} = \frac{PdT}{C_{dc}V_{dclink}} \tag{4-5}$$

Where

V_{dclink} is the DC-link voltage, V

ΔV is the DC-link ripple voltage, V

ΔQ is the change in capacitor charge, Coulomb

C_{dc} is the DC-Link capacitor, F

d is the duty cycle of the $IGBT_{\_bb2}$

P is the power rating, W

I_{load} is load current supplied to the grid, A

T is switching period, s.

In Equation (4-5) if the maximum ripple voltage, ΔV_{max}, occurs when maximum power is supplied to the ac grid and is at a duty cycle d = 1.0. If the acceptable ripple voltage is set 2%, the required DC-link capacitor is calculated as 0.65 mF. A 1 mF electrolytic capacitor from a commercial inverter is used as the DC-link capacitor for this application.

4.3.4 SCESS control strategies

Two control strategies can be applied to operate the proposed dc-to-dc converter – voltage mode control and current mode control strategy described briefly in the following sections.

4.3.4.1 Voltage mode control

In the voltage mode control strategy, the switching devices (IGBTs) are controlled directly by the gating signals generated from the error between the reference and actual values of DC-link voltage. For example in the duty cycle modulation (DCM) generation blocks in Figure 4-3, a fixed frequency ramp can be used to compare the error from the voltage controller in order to generate the gating signals. Therefore, in this control strategy, the voltage error signal will adjust the amount of the energy to be stored or utilised.

For boost mode the control needs to regulate the DC-link voltage, and the DC-link voltage error is used to generate the gating signal for the upper switching device as in Figure 4-3. In this case the supercapacitor modules will act as a dc source. When buck mode control is used to regulate the supercapacitor voltage, the DC-link will act as a dc source and the supercapacitor voltage error is used to generate the gating signal to control the lower switching device directly.

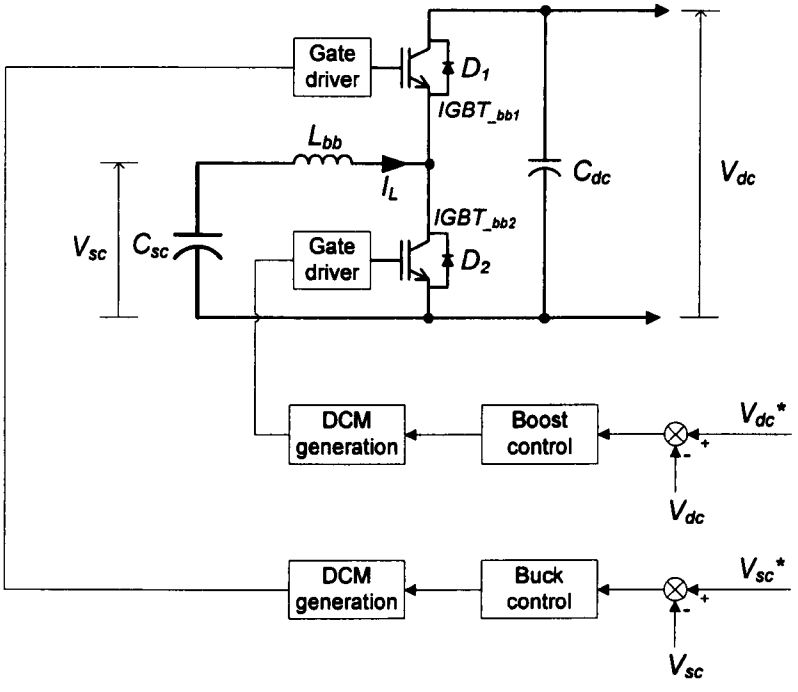

Figure 4-3 The voltage mode control structure

The levels of both the supercapacitor and DC-link voltages are proportional to the amount of energy transferred, and this is depended on the inductor current I_L. However, in this control strategy, the scheme does not control the inductor current directly. Therefore, the overall dynamic response of the voltage mode control dc-to-dc converter needs to be improved [91, 92].

4.3.4.2 Current mode control

For a dc-to-dc converter, the current mode control strategy regulates the inductor current I_L directly as illustrated in Figure 4-4.

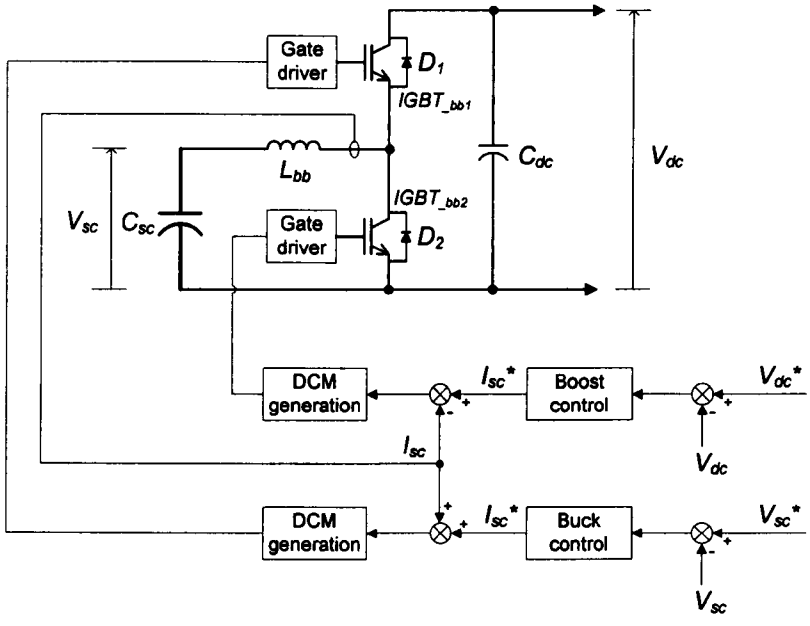

Figure 4-4 The current mode control structure

In this control strategy the inductor current is measured and fed back to be compared with the reference provided by the voltage error. The DC-link voltage needs to be controlled during boost mode, and the DC-link error is used to set the reference value for the inductor current. During buck mode operation, the supercapacitor voltage error is used to provide the reference value for the inductor current. The current errors are then used to generate the gating signal for the associated switching devices.

The current mode control strategy is preferable for this project as it provides fast, direct control over the energy transferred between the supercapacitor and the DC-link.

4.3.5 SCESS control design

The SCESS has two modes of operation. Boost mode takes power from the supercapacitors whereas buck mode recharges the supercapacitors. The two modes are described in more detailed in the following sections.

4.3.5.1 Boost mode control design

The control concept for boost mode operation is illustrated in Figure 4-5. An outer loop controls the DC-link voltage, whereas an inner loop controls the inductor current in the boost converter current control.

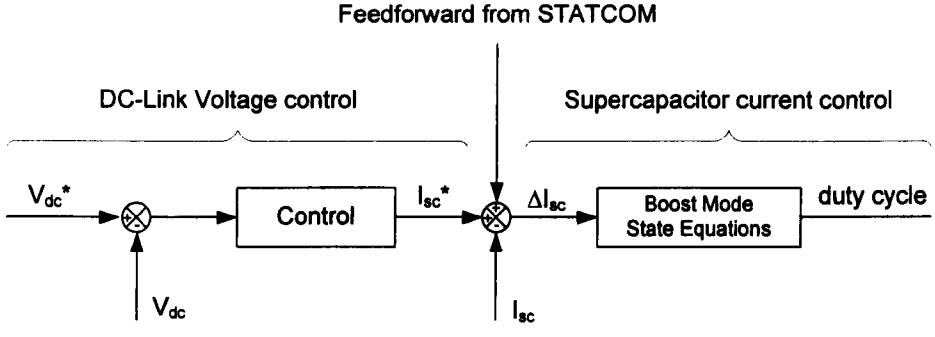

Figure 4-5 Boost mode control concept

A small signal model for the boost converter has been derived using state-space averaging which resulted in a linearised model described in Appendix C and given in Equation (4-6) [93, 94]. This model is used as a plant for the design of the outer voltage loop controller. For the whole system of this project, the SCESS will be combined with the STATCOM. Therefore, to avoid any dynamic effect on the STATCOM's current control, the bandwidth of the SCESS's control should be designed to be several times lower than the STATCOM's current control (i.e. less than 100Hz.)

$$\frac{\Delta V_{dc}}{\Delta I_{ref}} = \frac{k_1 k_2 (s + 1/k_2)(s + k_3)}{k_4 s^2 + k_5 s + k_6} \tag{4-6}$$

$$k_1 = \frac{r_s C_{dc}(1-d)V_{dc}}{2}$$

$$k_2 = \frac{T(1-d)^3 V_{dc} - 2LI_{dc}}{(1-d)^3 V_{dc}}$$

$$k_3 = \frac{1}{r_s C_{dc}}$$

$$k_4 = C_{dc}T(1-d)(V_{dc} - r_s I_{dc})$$

$$k_5 = \frac{C_{dc}V_{dc}}{2L}(2L + r_s T(1-d)^3) - I_{dc}(r_s C_{dc} + T(1-d))$$

$$k_6 = \frac{T(1-d)^3 V_{dc}}{2L} - I_{dc}$$

Where

C_{dc}	is the DC-Link capacitor, F.
L	is the buck-boost's inductor, H.
d	is the duty cycle of the IGBT operating in boost mode.
I_{dc}	is the DC-link current, A.
r_s	is the series resistance of the DC-link capacitor, Ω.
T	is the switching period, s.
V_{dc}	is the DC-link voltage, V.

With a sampling frequency of 5 kHz (more than 15 times higher than the control bandwidth), the proposed control loop implemented using discrete digital controller can be designed in the s-domain using the small-signal model in Equation (4-6). Using pole placement techniques the controller is designed with a damping ratio of 0.7 and bandwidth of about 14Hz. The resultant boost mode controller is given in Equation (4-7).

$$C_{boost}(s) = \frac{0.103(s + 24.7)(s + 10000)}{s(s + 3000)} \quad (4\text{-}7)$$

Using the MatLab bi-linear transformation 'c2d' function [45], the discretised version of the controller is given in Equation (4-8).

$$C_{boost}(z) = \frac{0.1589z^2 - 0.1581z}{z^2 - 1.538z + 0.5385} \quad (4\text{-}8)$$

For the inner loop, the state equations described in Appendix D are adopted for the boost operation to calculate the duty cycle (d) directly. During this mode the energy in the supercapacitor modules is released in order to maintain a constant DC-link voltage. The supercapacitor current is controlled according to the power demanded from the STATCOM unit (I_{dc}).

Although the control for this operation is designed with a low bandwidth, its transient response can be improved by using a feedforward signal from the STATCOM unit (I_{dc}) as indicated in Figure 4-5.

4.3.5.2 Buck mode control design

The buck mode control concept is illustrated in Figure 4-6. The major difference here is that the outer loop now controls the supercapacitor voltage. Again a small-signal model for the buck converter has been derived in Appendix C, given in Equation (4-9) and then used to determine a suitable outer loop controller. The inner loop also uses state equations to calculate the duty ratio (d). As shown in Figure 4-6, the current demand of this mode is fed forward to the STATCOM controller to improve the transient response of the STATCOM control unit.

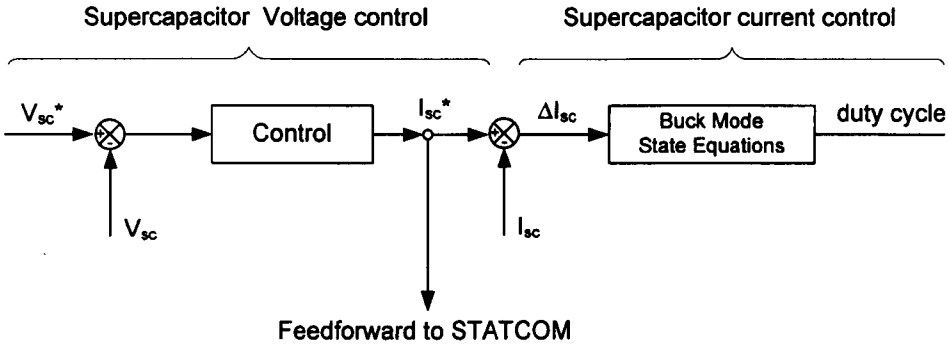

Figure 4-6 Buck mode control concept

$$\frac{\Delta V_{sc}}{\Delta I_{ref}} = \frac{c_1 c_2 (s + 1/c_2)(s + c_3)}{c_4 s^2 + c_5 s + c_6} \tag{4-9}$$

$$c_1 = 2R_s R_p L C_{sc}$$

$$c_2 = \frac{T(1-d)}{2}$$

$$c_3 = \frac{1}{R_s C_{sc}}$$

$$c_4 = 2LC_{sc}T(1-d)(R_p + R_s)$$

$$c_5 = 2LT(1-d) + R_p L C_{sc} - R_s R_p C_{sc} T(2d-1)$$

$$c_6 = 2L - R_p T(2d-1)$$

Where

C_{sc} is the supercapacitor modules, F.

L is the buck-boost converter's inductor, H.

d is the duty ratio of the IGBT operating in buck mode.

I_{sc} is the supercapacitor current, A.

R_s is the series resistance of supercapacitor modules, Ω.

R_p is the parallel resistance of supercapacitor module, Ω.

T is the switching period, s.

V_{sc} is the supercapacitor voltage, V.

The same techniques as used for boost mode operation controller design in section 4.3.5.1 are again applied to design the controller for buck mode operation. The s-domain controller, designed with a bandwidth of 13Hz and damping ratio equal to 0.7, is given in Equation (4-10) and the associating discrete form is in Equation (4-11).

$$C_{buck}(s) = \frac{0.231(s + 35.9)(s + 5000)}{s(s + 4.92)} \tag{4-10}$$

$$C_{buck}(z) = \frac{0.3476z^2 - 0.4609z + 0.1150}{z^2 - 1.999z + 0.999} \tag{4-11}$$

4.4 STATCOM plus SCESS

The overall power circuit diagram of the combined system is illustrated in Figure 4-7.

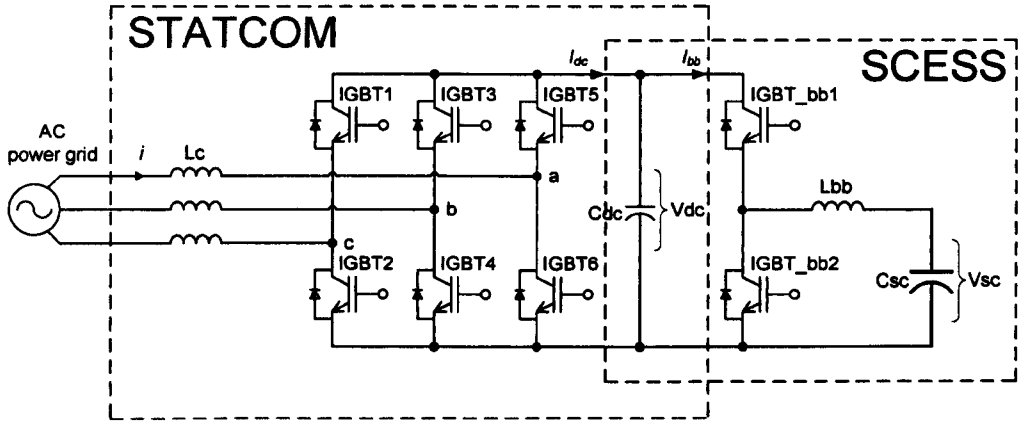

Figure 4-7 The power circuit diagram of the STATCOM plus SCESS

The overall control structure of the combination of the STATCOM and the SCESS is shown in Figure 4-8. The overall operation and control of the STATCOM plus SCESS can be classified into three main modes – STATCOM only mode, STATCOM plus SCESS boost mode, and STATCOM plus SCESS buck mode.

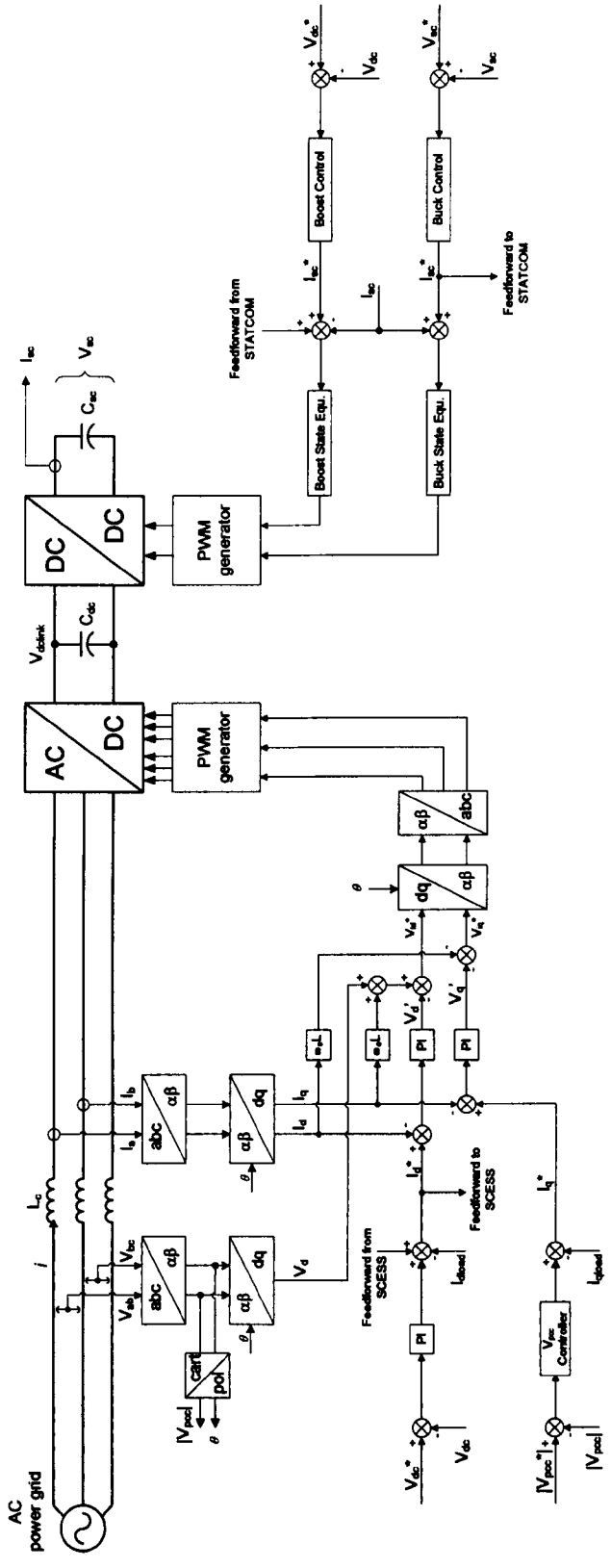

Figure 4-8 The overall control structure of the STATCOM plus SCESS

In the STATCOM only mode, only the magnitude of V_{pcc} will be monitored. The error in the magnitude of V_{pcc} is used to set the demands for the reactive power to be injected to the ac grid (I_q*). As a result, the ac grid side voltage will be kept constant by reactive power compensation from the STATCOM. During the injection of the reactive power, the DC-link voltage is kept constant by drawing real power from the ac power grid, which is regulated by the DC-link control (I_d*).

In the STATCOM plus SCESS boost mode, to prevent the DC-link voltage control by the STATCOM unit and the SCESS unit fighting each other, the STATCOM's DC-link voltage control will be disabled. Only the SCESS's DC-link voltage control will be enabled for modulating the energy transfer from the supercapacitor modules to the DC-link in order to keep the DC-link voltage constant at its demand level (400V). A feedforward current measurement from the ac grid event is used to quantify the demands of energy to be transferred from the supercapacitor modules. Therefore in this mode of operation, the STATCOM plus SCESS can supply both the real and reactive power. As a result, energy will be transferred from the supercapacitors to the ac power grid.

In the STATCOM plus SCESS buck mode (i.e. recharging the supercapacitors) the DC-link voltage will be regulated by the STATCOM's DC-link voltage control. Power is transferred from the ac grid to the DC-link; the SCESS's supercapacitor voltage (V_{sc}) control will transfer the DC-link power to the supercapacitors. In this mode, the supercapacitor recharging current will be used as the feedforward current for the STATCOM's current control in order to define the quantity of the power to be absorbed from the ac side.

To verify that the proposed STATCOM with supercapacitor energy storage can exchange both real and reactive power with the ac power grid, a

simulation study using MatLab/Simulink and the SimPowerSystems block set was performed and is described in the next sections.

4.5 Simulation of STATCOM plus SCESS

The simulation study is implemented with the scenario based on the same ac power system used in the simulations of the STATCOM system in Chapter 3 (and also the same as in the experimental validation setup in chapter 5). The enhanced STATCOM unit is shown in Figure 3-18.

A light load is used to reduce the ripple on the voltage waveform and to simulate the ancillary system locally within the site as described in Chapter 3. Other components (reactors and transformer) are described in section 3.5 of Chapter 3.

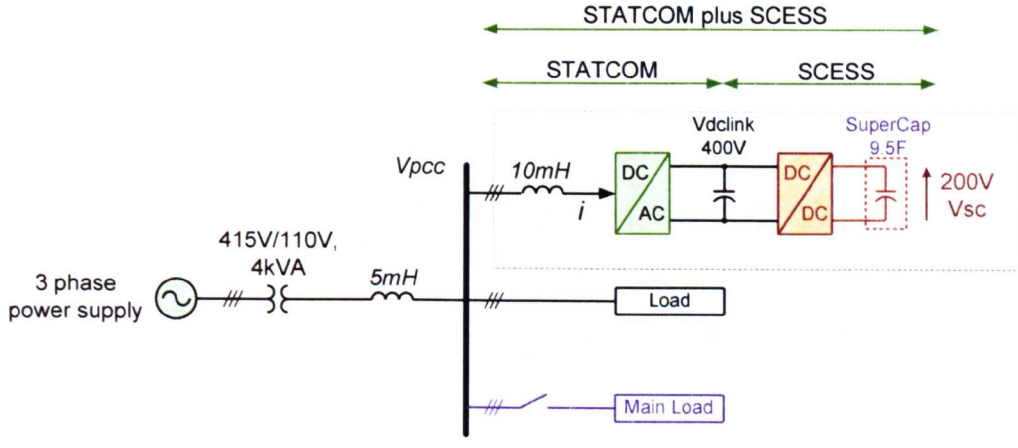

Figure 4-9 Power circuit diagram setup for simulation study

The control scheme was implemented digitally with a sampling frequency of 5 kHz which was generated by and synchronised with the STATCOM's PWM switching signal.

4.5.1 Simulation of basic operation of STATCOM plus SCESS

To verify that the control of the STATCOM plus SCESS model operates properly, simulations of only the STATCOM plus SCESS connected to the three-phase power supply were carried out in both boost and buck modes of operation, with an ideal step change current (I_d*) provided as the reference current. Therefore, the simulations were carried out as a functional validation of the enhanced STATCOM. The response of the proposed STATCOM to an ideal step change of the 10A in the d-axis current is shown in Figure 4-10, Figure 4-11 and Figure 4-12. This corresponds to boost mode operation.

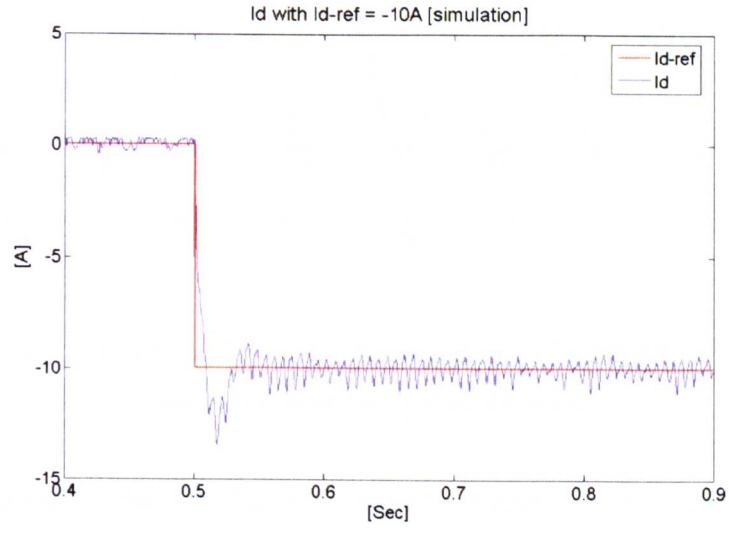

Figure 4-10 Response of d-axis current control to a step change of negative 10A [simulation]

The excellent current control performance is verified by way the actual d-axis current tracks the reference value as shown in Figure 4-10. The controlled current shows an overshoot of 26.4% which is close to the designed value of 25%. The settling time is approximately 35ms, while the designed value is 30ms. This error in the time constant is caused by the additional 5mH inductor

connected between the transformer and the V_{pcc}. This additional inductor was used to highlight the voltage drop at the V_{pcc} bus in order to show the performance of the STATCOM. In reality, there is no this inductor in the DG system, and it is not included in the design. This 5ms error is not significant for the validation of the proposed idea.

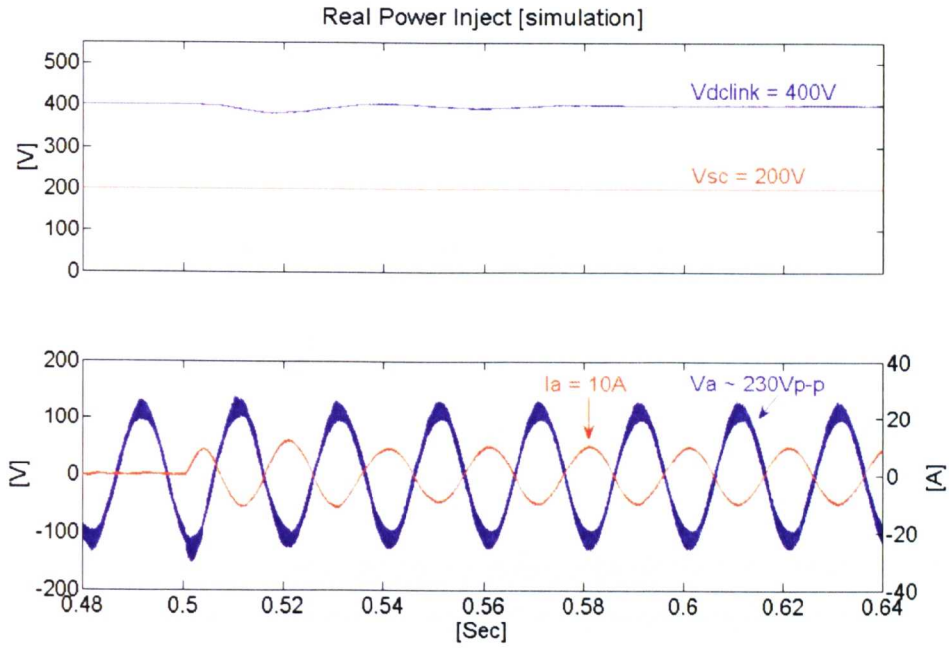

Figure 4-11 V_{dclink}, V_{sc}, V_a, and I_a during the period when the STATCOM plus SCESS inject real power to grid [simulation]

The simulation result for the real power injection mode can be seen in Figure 4-11, where from the initial change of the I_d reference at t=0.5s the angle displacement of the phase voltage and line current at V_{pcc} bus is 180 degrees (for clarity, only phase 'a' is shown in the bottom trace of Figure 4-11). The top trace shows about 6.5% drop of the DC-link voltage between t=0.5s and t=0.52s – this is the time taken for the boost mode control to become energized. The approximate 4.5% overshoot of the DC-link voltage and the settling time of around 57ms are close to the design of 4.25% overshoot and 55ms settling time. The supercapacitor terminal voltage V_{sc} decreases slightly. However due to the very large value of the supercapacitors,

and the short period of this process, the drop in V_{sc} is not obvious in Figure 4-11.

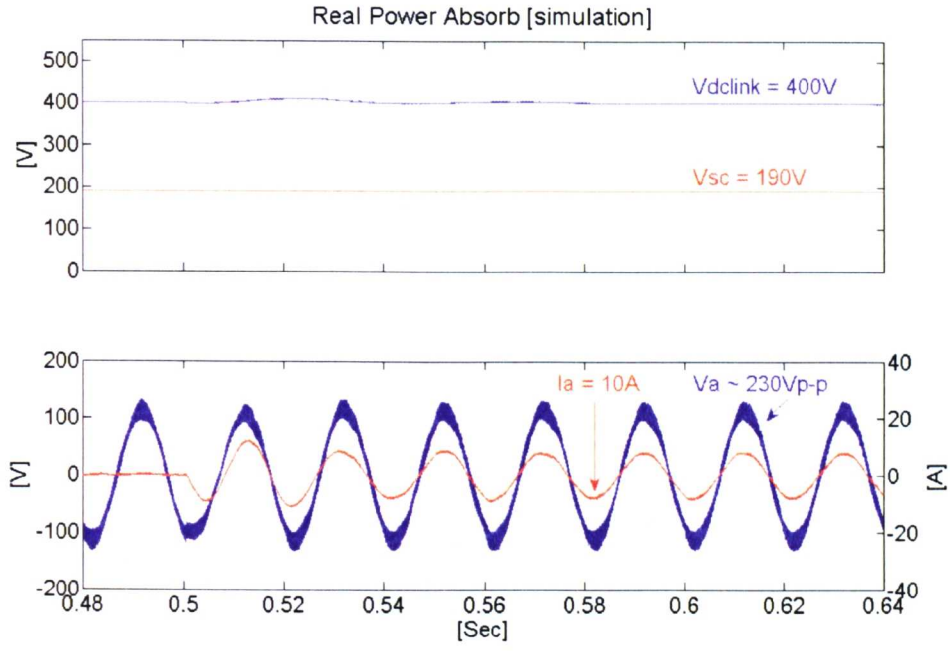

Figure 4-12 V_{dclink}, V_{sc}, V_a, and I_a during the period when the STATCOM plus SCESS absorbs real power from grid (i.e. charge the supercapacitors) [simulation]

When the STATCOM unit is triggered by a positive change in $+I_d$ current, the operation of buck mode or real power absorb mode is triggered. This can be seen from phase voltage V_a and line current I_a; they are in-phase from t=0.5s onwards (bottom traces of Figure 4-12). As the energy is transferred from the ac side to the DC-link, this excess energy causes an overshoot of about 3% during t=0.505s and t=0.53s before the SCESS's buck mode control can react. The overall result of the buck mode operation shows the process of energy storage by transferring ac side energy to the supercapacitors. As a consequence, the supercapacitor terminal voltage increases slightly, but as mentioned previously with the rating of supercapacitors and the short process period, the increase in V_{sc} can not be seen Figure 4-12.

4.5.2 Simulation of a power system using a STATCOM plus SCESS

A simulation to demonstrate the benefits to the ac power system using STATCOM plus SCESS was carried out in order to compare with the previous system which used only the STATCOM. The simulation results for this operation are illustrated below in Figure 4-13. For clarity the plot of the magnitude of V_{pcc} is shown separately in Figure 4-14, while Figure 4-15 shows the controlled I_d and I_q current relating to the power flows in the system.

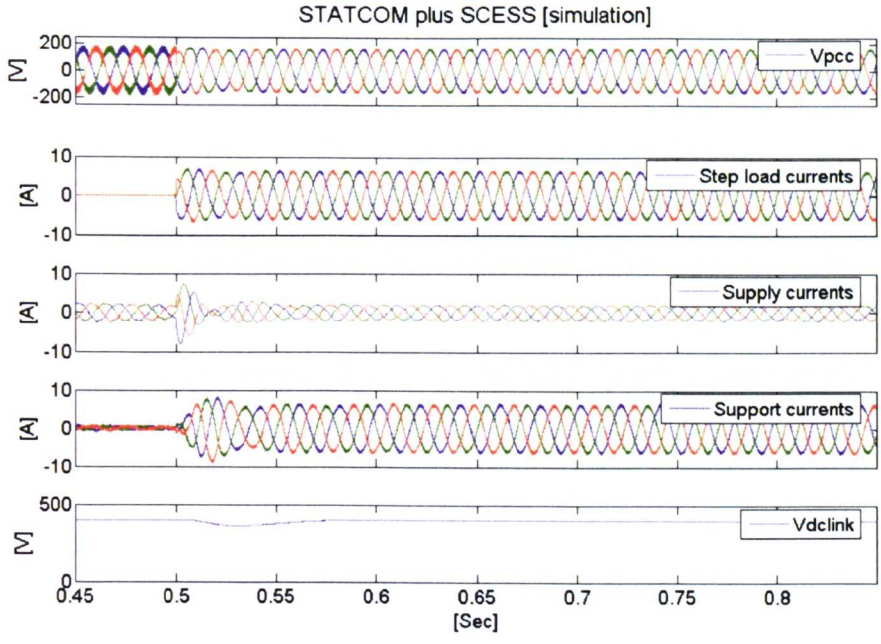

Figure 4-13 V_{pcc}, load currents, supply currents, and support currents for the system with STATCOM plus SCESS [simulation]

For normal operating conditions, as shown in Figure 4-13 from the beginning to time t= 0.5s, the system operates as a conventional STATCOM. There is only a light load current of about 1.5 A seen in the second trace of Figure 4-13, and the STATCOM supplies a very small reactive current (less

A) to the grid in order to keep the magnitude of V_{pcc} exactly constant at the reference. The high frequency switching ripple can be seen on the three-phase voltage waveforms. The DC-link voltage is kept constant at 400V.

The main load is switched on at t=0.5s and the load current is measured (only the main load current is measured and transformed to d-q components). The measured main load current is then used to trigger the STATCOM plus SCESS allowing it to operate with its full function. The ripple on the three-phase voltage waveforms is reduced due to the voltage divider effect described in Chapter 3. When the sudden change of load current occurs, an 8A peak of the supply current (the middle trace) is seen between t=0.50s and t=0.53s (settling time of the current control) in order to supply the main load before the support current from the STATCOM unit takes full control. The main load current (real power current) is fully supported by the STATCOM plus SCESS.

The light load (ancillary system) is permanently connected to the grid and its current is not measured -thus the STATCOM is not set to support this load. Therefore, only a small current due to the light load is seen in the supply current waveform. The DC-link voltage drops at the beginning of the load change, and is then regulated by the SCESS' boost mode control to be constant at 400V.

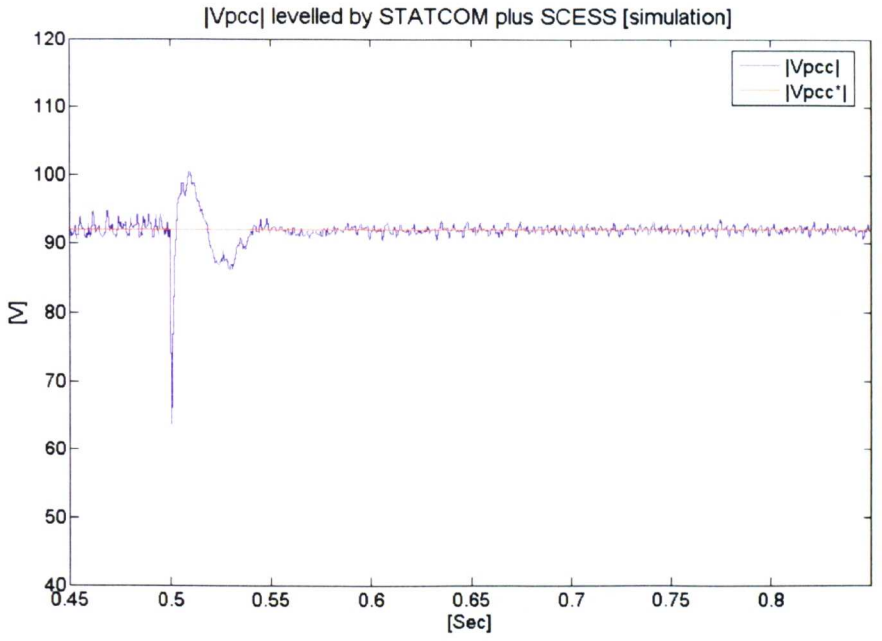

Figure 4-14 $|V_{pcc}|$ of the system with STATCOM plus SCESS [simulation]

During this period, the magnitude of V_{pcc} shown in Figure 4-14 is maintained constant by the reactive power compensation, and also the real power compensation by the STATCOM plus SCESS can be seen clearly in the greater detail of the support current shown in Figure 4-15, where the 7A negative controlled I_d current indicates that real power is being transferred to support the load at the ac power grid, and the negative I_q current of around 1.5A is the reactive power current for the voltage compensation at V_{pcc}.

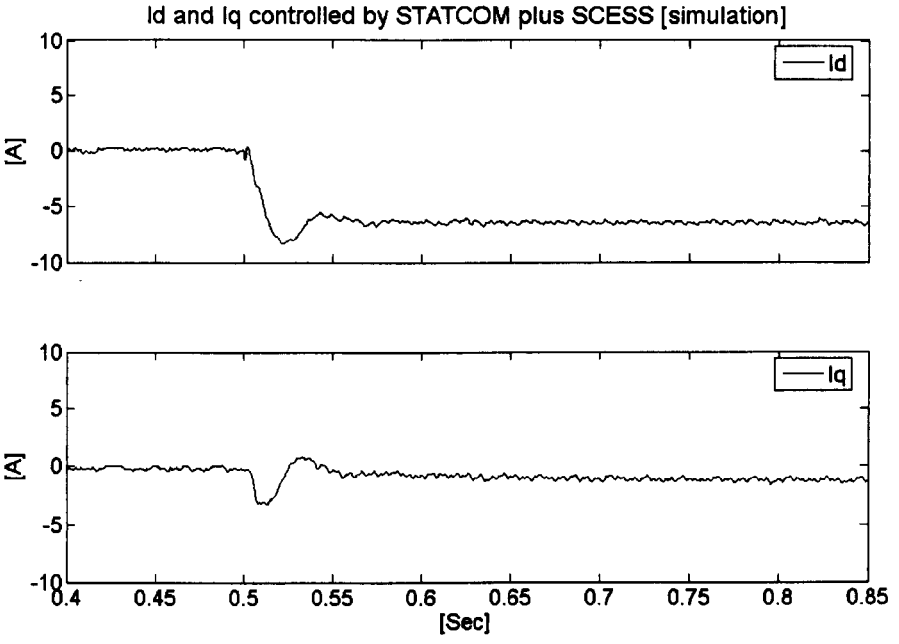

Figure 4-15 Controlled I_d and I_q for the system with STATCOM plus SCESS [simulation]

4.5.3 Comparison of the system with and without STATCOM plus SCESS

The same system as in the previous section is simulated in this section, but with the function of the STATCOM plus SCESS delayed from t=0.5s to t=0.575s in order to confirm the system behaviour with and without the STATCOM plus SCESS. Simulation results for the three-phase system are shown in Figure 4-16. The magnitude of V_{pcc} and the controlled current are shown in Figure 4-17 and Figure 4-18 respectively.

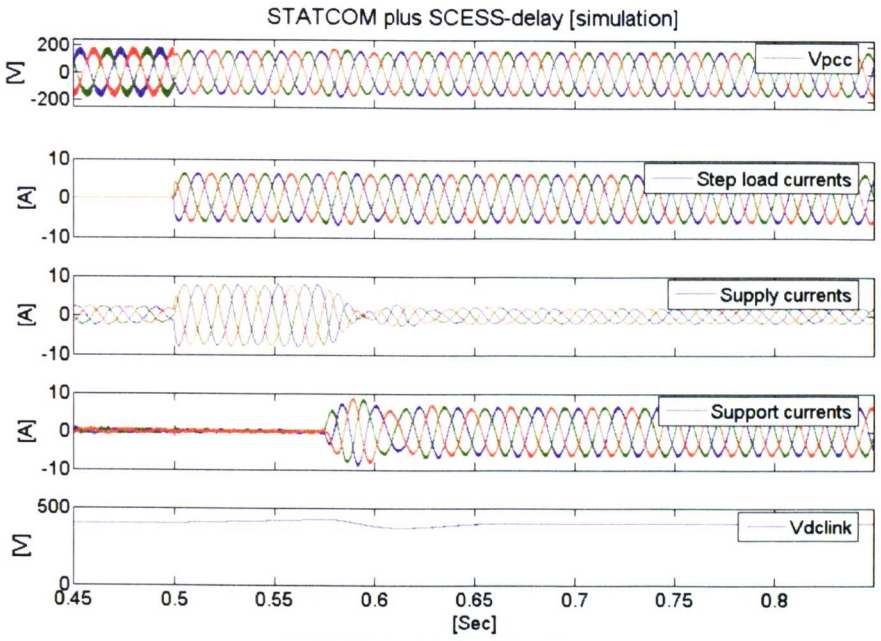

Figure 4-16 V_{pcc}, load currents, supply currents, and support currents of the system with STATCOM plus SCESS when its operation is delayed from t=0.5s to t=0.575s [simulation]

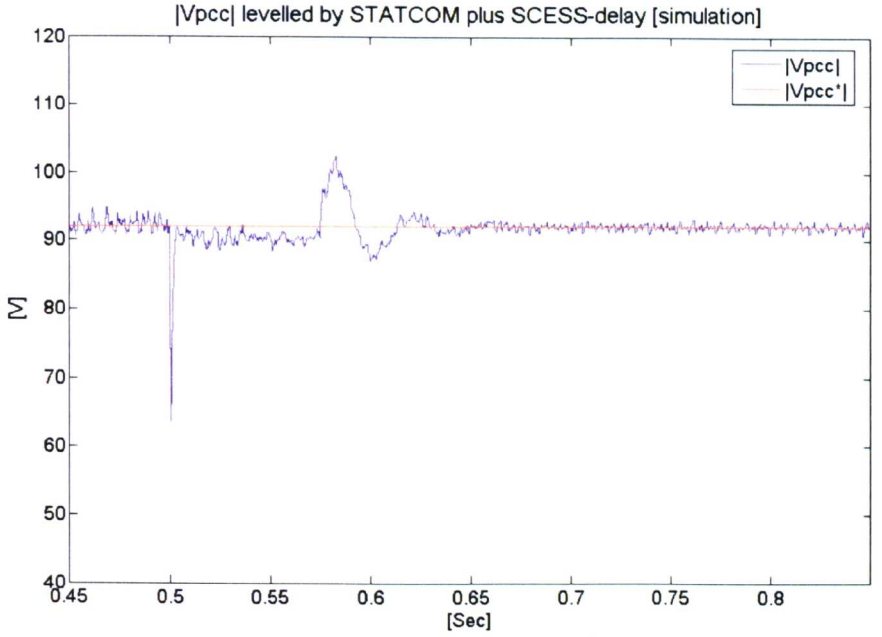

Figure 4-17 $|V_{pcc}|$ of the system with STATCOM plus SCESS when its operation is delayed by 75ms [simulation]

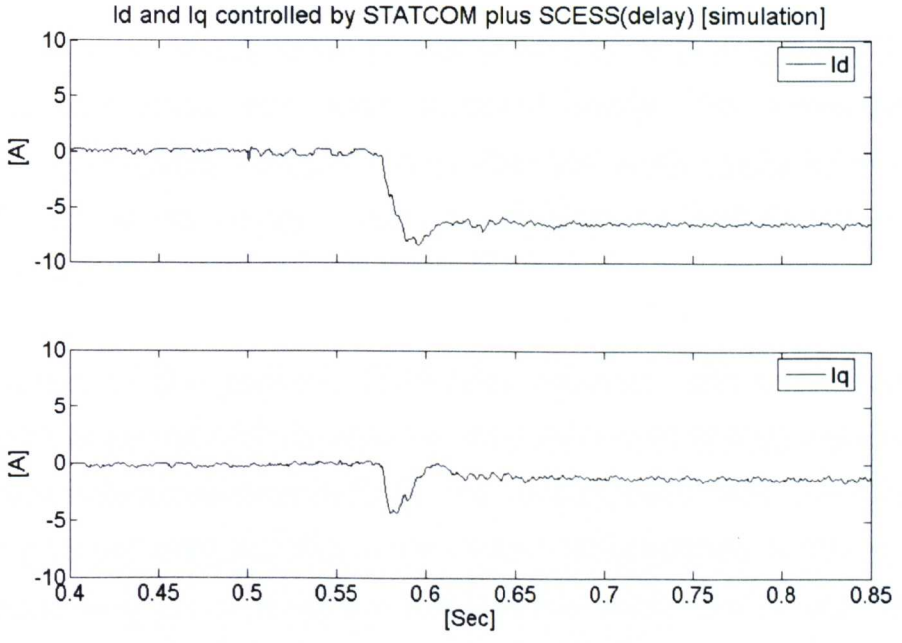

Figure 4-18 The controlled I_d and I_q for the system with STATCOM plus SCESS when its operation is delayed by 75ms [simulation]

At the beginning of the simulation period, the STATCOM plus SCESS operates as in the previous section – only the conventional STATCOM function is enabled. The same patterns of the results as described in section 4.5.2 are seen between t= 0.4s and t=0.5s.

During the period from t=0.5s to t=0.575s although the main load is switched on at t=0.5s, both real and reactive power support from the STATCOM unit is disabled. Therefore, there is no support from the STATCOM unit as shown the middle trace of Figure 4-16 and in Figure 4-18, resulting in the whole load is being supplied only by the ac power grid. This current causes the drop in the magnitude of V_{pcc} voltage as shown in Figure 4-17. However from time t= 0.575s onwards, the full function of the STATCOM plus SCESS is enabled to produce the support for both the real and reactive power compensation.

4.6 Conclusions

In this chapter, several different energy storage technologies for power systems applications have been described briefly. The advantages of supercapacitor energy storage have been discussed as the reason for selecting the SCESS as the storage device to improve the performance of the STATCOM.

The control of the proposed STATCOM enhanced with supercapacitors, (STATCOM plus SCESS) is presented. With the control strategy explained in this chapter, the simulations verify that the combination of the STATCOM and the SCESS can store and supply the energy instantaneously to the ac grid. Therefore, in terms of frequency stability, this ability can be used as the complement for the frequency variation due to the slow response of generators (mentioned in Chapter 2), and therefore to improve the transient stability of the ac system.

Chapter 5

Experimental setup

5.1 Introduction

This chapter describes the experimental setup designed with the aim to demonstrate the benefits to an ac power system using the enhanced STATCOM. For this research, a conventional STATCOM was built and was enhanced with the supercapacitor energy storage system (SCESS), as described in chapter 4. The overall experimental rig was constructed to validate that the proposed STATCOM can supply both real and reactive power to the ac power grid instantaneously and to compare with the simulation studies carried out by MatLab/Simulink SimPowerSystems BlockSet as explained in chapter 4.

The STATCOM plus SCESS was applied as a power electronic based power flow controller in the same scenario as used for the simulation studies. The

overall layout of the experimental rig is shown in Figure 5-1, where the parameters and symbols labelled in the circuit diagram are detailed in Table 5-1.

Figure 5-1 shows that the conventional STATCOM is a combination of a conventional DC-link capacitor, a voltage source inverter, and a coupling reactor. The SCESS comprises a supercapacitor unit, a bi-directional DC-DC converter, and a conventional capacitor. To enhance the performance of the conventional STATCOM, the SCESS is interfaced to the DC-link capacitor of the STATCOM. Therefore, in the diagram, they are sharing the same conventional DC-link capacitor. In this project, to operate this proposed system, a dSPACE DS1104 R&D controller board [95] is employed to perform the real-time digital control for the whole system as shown in Figure 5-1.

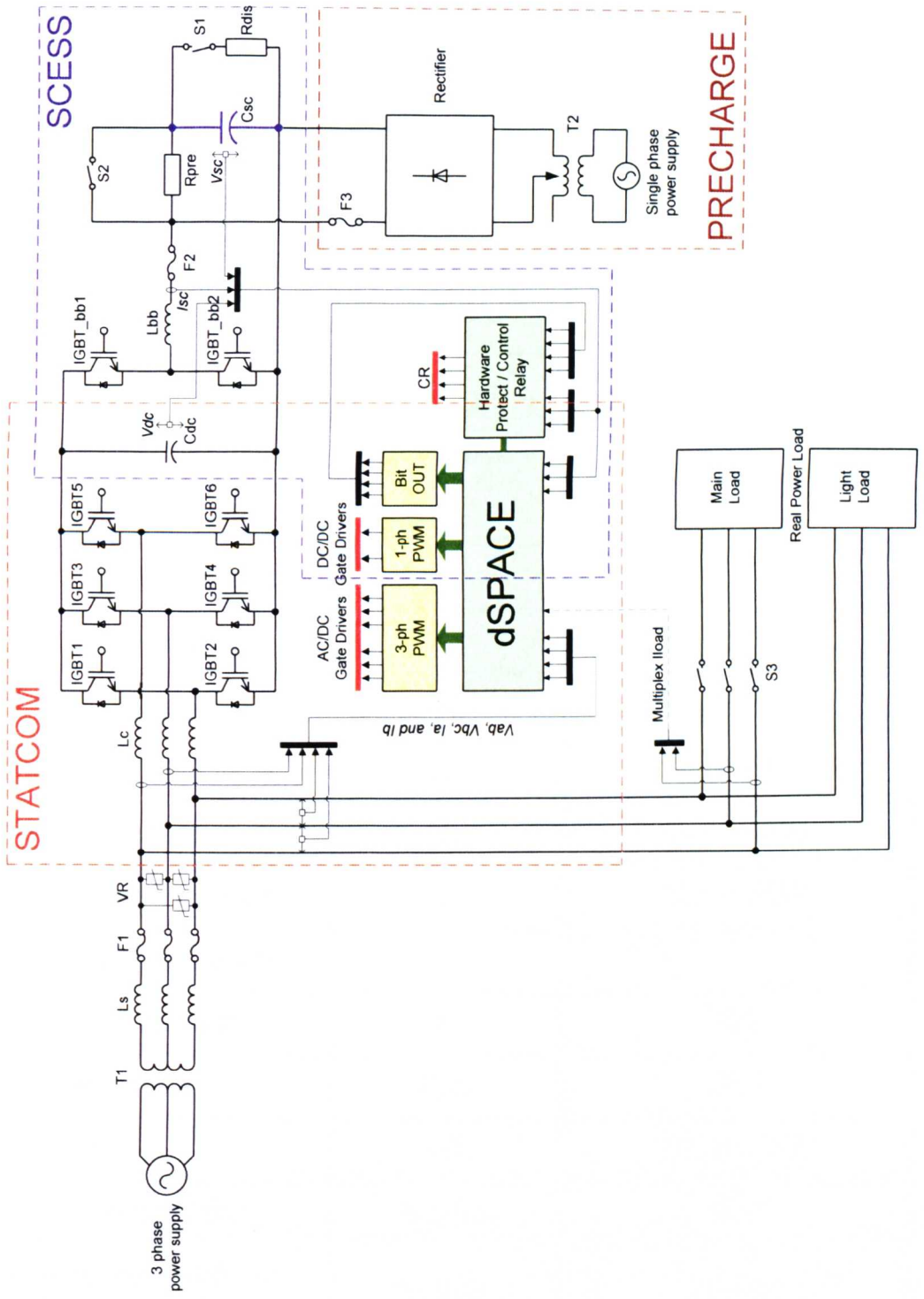

Figure 5-1The overall experimental setup

Table 5-1 Experimental rig parameters and symbols

Parameter	Symbol	Value
Supply voltage		415V, 50Hz
Step down transformer	T_1	415V/110V, 4kVA
Single phase isolating transformer	T_2	230V/115V, 2.5kVA
AC/DC Inverter rating	$IGBT_{1-6}$	10kVA
DC/DC Inverter rating	$IGBT_{\_bb1-2}$	5kW
DC-link capacitor	C_{dc}	1,000 μF, 800V
Supercapacitor module	C_{sc}	9.5 F, 200V
System line reactor	L_s	5mH
Coupling reactor	L_c	10mH
DC/DC inductor	L_{bb}	10mH
DC-link voltage	V_{dc}	$V_{dc}^* = 400V$
Supercapacitor voltage	V_{sc}	$V_{sc}^* = 200V$
Supercapacitor current	I_{sc}	
Semiconductor fuse	F_1	10A
General line fuse	F_2,F_3	25A
Varistor	VR	320Vac, 184J
High power resistor	R_{pre}, R_{dis}	4kW
High power switch (Magnetic contactor)	S_1, S_2,S_3	10kW
Control relays	CR	10A, 250Vac

According to the constraints on the application of the SCESS unit, the minimum voltage for the supercapacitors to be applied in this project is set to 100V. A further consideration was that the controller was designed using a small-signal model (described in chapter 3 and in appendix B). Initial charging of the supercapacitor was deemed to be outside this operating region, and therefore an additional precharge unit was included. The precharge unit was designed to charge the supercapacitor modules to a voltage of about 100V before operating the controller. Also, to ensure that the experiments were carried safely during precharging and discharging, the current was limited by two high power resistors (R_{pre} and R_{dis}) as shown in the circuit diagram of the SCESS in Figure 5-1.

The design considerations and constraints on the application of the proposed STATCOM are described in section 5.2. The experimental rig is detailed in section 5.3. Finally in section 5.4 the proposed experimental setup for demonstrating benefits to an ac power system using STATCOM plus SCESS is described.

5.2 Design considerations for STATCOM plus SCESS

As the inverter and the DC-DC converter used in this project are designed for utilising the supercapacitor's energy, the supercapacitor terminal voltage (V_{sc}) is then considered as the dominant rating that further defines the other voltage limitations. The constraints on the application of the SCESS described in chapter 3 indicates that the maximum and minimum voltage ratings of the 9.5F supercapacitor module are at – $V_{sc\_max} = 200V$ and $V_{sc\_min} = 100V$.

In order to make the use of the supercapacitor for the STATCOM, the proposed bi-directional DC-DC converter is placed in between the

supercapacitor modules and the STATCOM, with one side connected to the supercapacitor unit and the other side connected to the STATCOM's DC-link capacitor. This converter is designed to keep the DC-link voltage constant at 400V by operating at a duty ratio of about 0.5 - the optimum point [47] where the stored energy can be extracted from the supercapacitors by the DC-DC converter. With this optimised operating point, as the DC-DC converter is interfaced to the STATCOM's DC-link capacitor, this DC-link capacitor is therefore rated at $V_{dclink} = 400V$.

To operate the STATCOM with the ability to inject power to the ac power grid, three-phase PWM voltage should have a higher magnitude than the three-phase power supply voltage. With the DC-link voltage fixed at 400V, a step-down transformer (rating 415V/110V 4kVA) must be used to lower the supply voltage as shown in Figure 5-1, ensuring that the operation of the inverter, by the PWM technique, will be in linear region and will not reach over-modulation. The voltage at the point of common coupling in this research is therefore set to be V_{pcc}=110V (line-to-line RMS voltage).

5.3 Experimental rig

In this section, the STATCOM and the SCESS are designed depending on the considerations and constraints mentioned earlier. The other relevant devices used in demonstrating the benefits to the ac power system using STATCOM plus SCESS are also considered in greater detail.

5.3.1 The STATCOM

A 10kVA voltage source inverter was built for this project. It comprises three half bridge IGBTs modules (six IGBTs) and a conventional DC-link capacitor as shown in Figure 5-1. The value of the DC-link capacitor needs to be

suitable for the SCESS as they are combined together through this capacitor as discussed in section 5.2. In this project, a 1000μF capacitor (two commercial 2000μF 415V capacitors connected in series) was used as the DC-link capacitor; details concerning the design technique are described in chapter 3 where the voltage ripple is the major consideration for selecting this capacitor.

In practice, circuit stray inductance due to wiring and connections (including the internal stray inductance of the IGBTs itself) can initiate high frequency voltage oscillation across the IGBTs (an interaction caused by the stored energy in the stray inductance and the capacitance). This oscillation could possibly result in high-voltage overshoot that can degrade the performance of the inverter or possibly damage the IGBTs [96]. To reduce the effect of the stray inductance, polypropylene capacitors rated at 470nF 1000Vdc, whose dielectric is particularly suitable for high-frequency application, were added at the dc bus bar as shown in Figure 5-2.

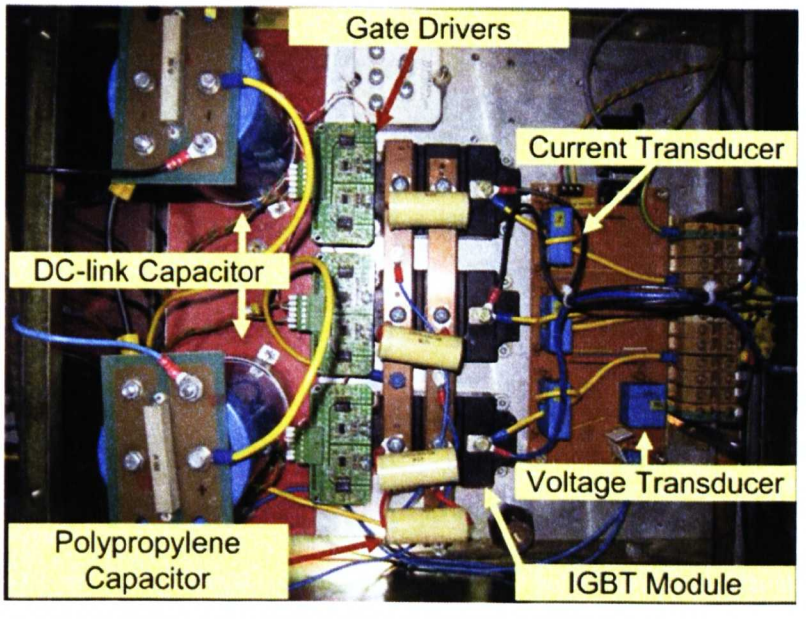

Figure 5-2 Top view of the inverter

A three-phase inductor (coupling reactor) is connected linking between the ac power grid (secondary side of the step-down transformer) and the front-end of the inverter. The inverter is being operated using the principle of PWM switching, the output voltage of the inverter is highly distorted due to the harmonic content from the switching process. The inductor acts as a current filter to smooth the current waveform before allowing it to flow to the ac power grid. The higher value of the coupling inductor gives smoother current waveforms, but in the other hand the higher value reduces the speed of the current control (it limits the maximum di/dt) and limits the size of the current that can be controlled. For this project, a three-phase coupling inductor of 10mH is chosen as a compromise between allowing reasonable current magnitude and reducing switching harmonics.

In credit, the inverter used for this research was constructed using the IGBTs and gate driver circuits first built by Dr Wanchak Lenwari for the project titled "High performance current control for shunt active filters using resonant compensators".

The inverter was applied as the controlled voltage source in order to control the power flow between the STATCOM terminals and the ac grid. The STATCOM voltage was produced using a sinewave PWM technique as illustrated in Figure 5-3. In principle, this switching technique compares the modulated signals ('V-control' - the signals that represent the three-phase voltage at V_{pcc} bus provided from the controller board) with the carrier voltage waveform ('V-tri' – the switching frequency triangular waveform) as shown in the top trace of Figure 5-3. The resulting signals of each phase are therefore used to generate the PWM switching signals for turn on and turn off of the IGBTs, corresponding to the controlled demand voltage.

The per-unit value of the output voltage at the ac side of the inverter is also shown in Figure 5-3, where V_{ao} and V_{bo} are the phase voltage waveforms and V_{ab} is the line-to-line voltage waveform. Although the output waveforms are

non-sinusoidal the harmonic content is suitable for the application, and is compared with the fundamental sinewave as shown in the bottom trace of Figure 5-3.

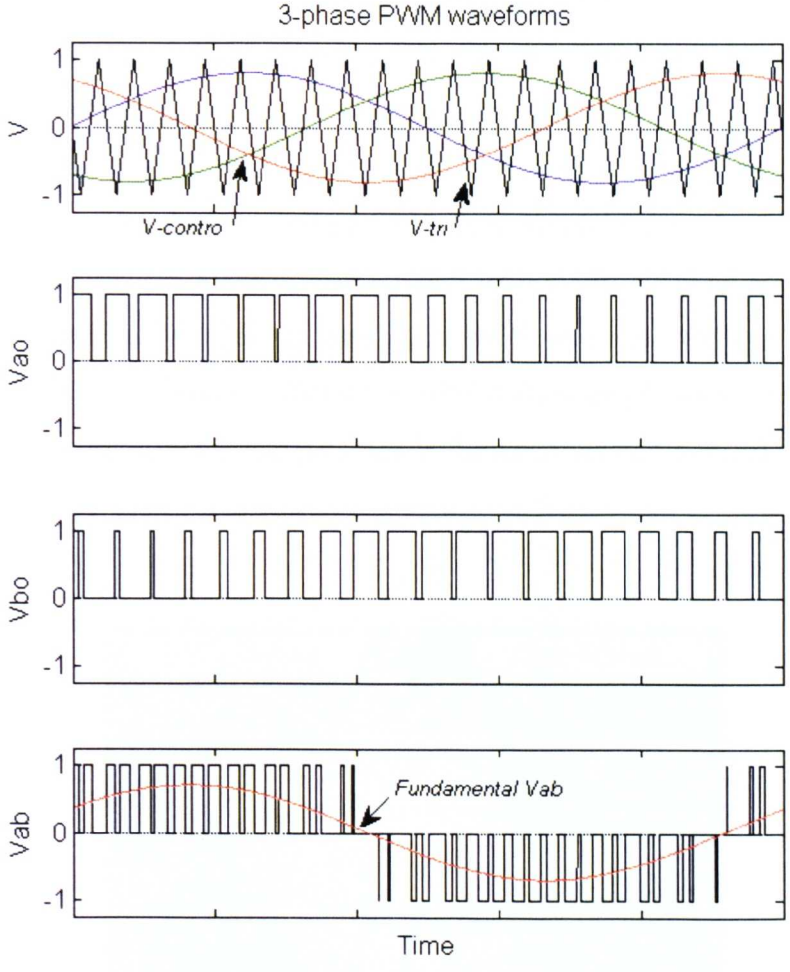

Figure 5-3 Sinewave PWM switching technique

For experimental tests, protection for the STATCOM's DC-link overvoltage and overcurrent are implemented both in hardware as described in section 5.3.5 and in software implementation described in appendix E.

5.3.2 The SCESS

A bi-directional power flow DC-DC converter rated at 5kW was constructed by using two IGBTs (half bridge IGBT module with gate drivers shown in Figure 5-4) and one inductor. The power circuit diagram of the SCESS depicted in Figure 5-1 shows that one end of the DC-DC converter (the inductor side) is connected to the supercapacitor unit; the other end is linked to the STATCOM's DC-link capacitor. The SCESS is designed to improve the performance of the STATCOM. Therefore, the considerations and constraints on the application of the SCESS described in chapter 4 define that the rating of the supercapacitors (ten modules of 95F 20V manufactured by ELIT) is the primary consideration for the other voltage ratings (the supercapacitor voltage V_{sc} = 200V and the DC-link voltage V_{dc} is 400V, and it is desirable to have the DC-link capacitor of about 1000 μF. A 10mH inductor (designed in chapter 4) is used as the medium for energy transfer between the two ends of the DC-DC converter

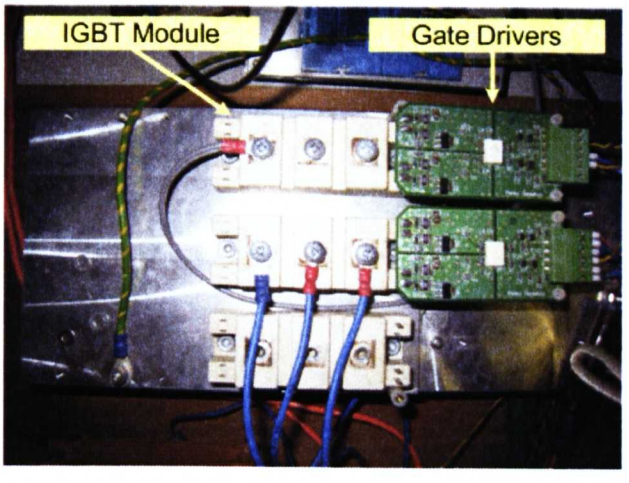

Figure 5-4 Top view of the DC-DC converter

Protection for the SCESS is implemented with both the primary protection by software described in Appendix E and in hardware as described in section 5.3.5. Also, the precharge unit shown in Figure 5-1 is used.

5.3.3 Current mirror and gate driver circuits

In this research the high frequency switching operation of both the inverter and the DC-DC converter generates the high-frequency switching noise that can influence the performance of any nearby digital electronic devices. In the noisy environment the low voltage PWM control signal can be vulnerable, especially when the signal is transmitted over a long distance. The effect of noise on the PWM gating signal can possibly lead to a failure of the IGBTs.

To improve the noise immunity of a signal transmitted over the long distance, the PWM voltage signal generated at the control board can be converted to a current signal before sending along the signal cable to the gate driver circuit which is normally mounted at the IGBT. Alternatively a fibre optic could be used but this is much more expensive. The PWM control signal is a logic level signal of 5V and 0V. On its own, it is not capable of turning on and off the high power switching devices. Therefore, a gate driver circuit board is required and constructed in order to adapt the PWM logic signal to a higher level for gating the high power IGBT modules.

In this project, a current mirror circuit was built for the inverter and the converter as described in section 5.3.3.1, while section 5.3.3.2 details the gate driver circuit.

5.3.3.1 Current mirror circuit

A current mirror circuit based on a Wilson current source configuration was used; more details can be found in [97]. The circuit arrangement in Figure 5-5 ensures that the output current to supply the gate driver circuit is equal to the input current to the transmission. The practical circuit board is shown in Figure 5-6 where six circuits were built for the voltage source inverter, and the other two circuits were built for the DC-DC converter.

The driver circuit is shown in Figure 5-5. The original PWM voltage signal is buffered using a 74ACT244 to ensure that the signal will be at +5V and 0V and to prevent loading error from the control board if any abnormal condition occurred at the current mirror. Using this buffer also has the advantage to enable and disable the PWM signal. The signal is then converted to be the preferable current signal by the current mirrors. This current signal is then transmitted to the gate driver circuit.

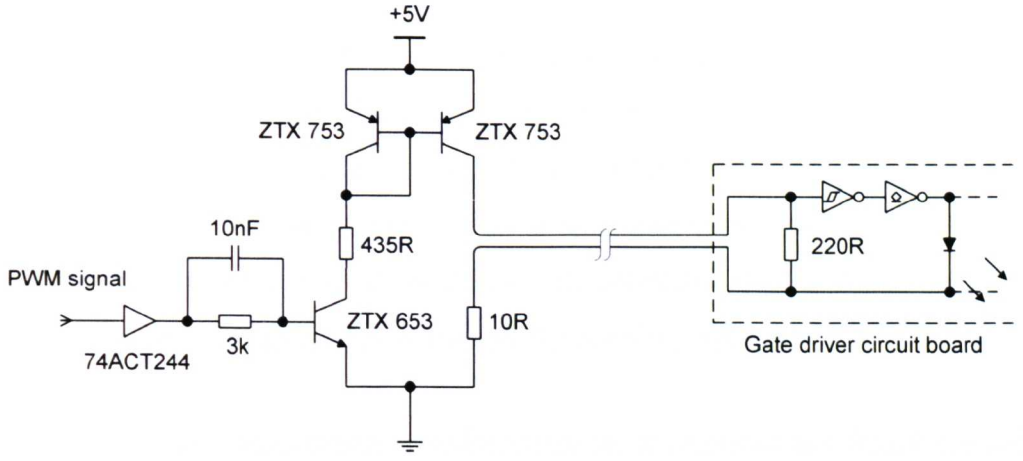

Figure 5-5 Current mirror circuit diagram

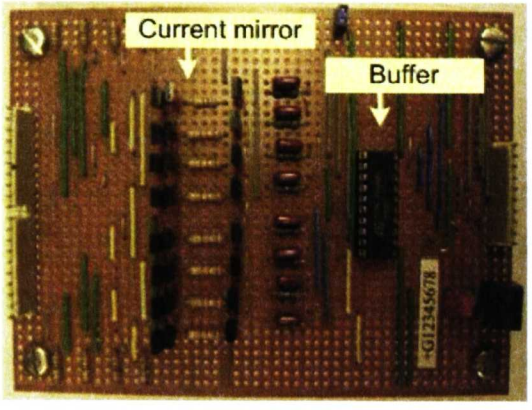

Figure 5-6 Top view of the current mirror circuit board

5.3.3.2 Gate driver circuit

As mentioned earlier, the main function of the gate driver circuit is to adapt the original low-power PWM signal to be an adequate signal that can turn on and off the IGBTs. Furthermore, by using optocouplers as shown in the arrangement of the circuit in Figure 5-7 the gate driver is not only capable of driving the switching devices, but also provides the electrical isolation between the control and the high power circuit.

Initially, in Figure 5-7 the PWM current signal coming from the current mirror circuit board is converted back to a voltage signal using the 220R resistor. This equivalent voltage signal is reinforced by the Schmitt trigger and open-collector logic gate. The Schmitt trigger is also used to provide noise rejection and improve the immunity of the circuit. The open-collector gate provides the buffer to allow enough power to turn on the optocoupler.

The HCPL-3120 optocoupler provides isolation to separate the digital ground of the logic circuit from the floating ground reference of the high power circuit. The output voltage from the optocoupler is directly fed to the two transistors to provide the gating voltage of +15V and -15V between the gate and the emitter of the IGBTs in order to provide turn on and turn off respectively.

Special care must be taken when considering the gate resistance, R_g; its value determines the speed of the turn on and off which depends on the characteristic of the IGBT module. In this research IGBTs manufactured by Dynex model GP200MHS12 were used, and the gate resistors of 5 ohm (two of 10R connected in parallel) were chosen.

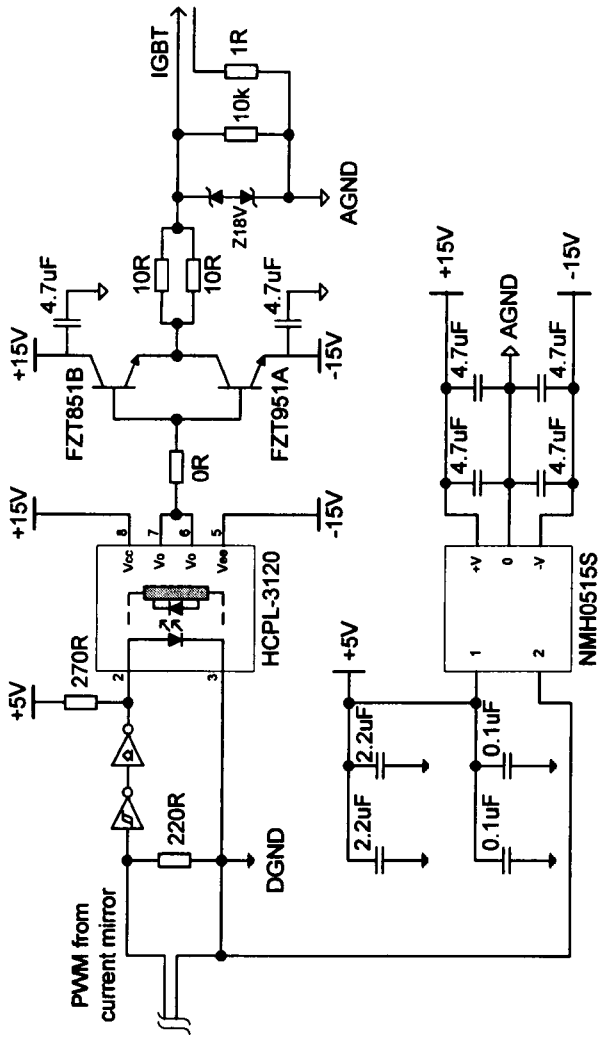

Figure 5-7 Gate driver circuit diagram

5.3.4 Voltage and current measurement

Four voltage and five current transducer circuits were built for the following measurements.

V_{ab} Line-to-line voltages at the V_{pcc}

V_{bc} Line-to-line voltages at the V_{pcc}

V_{sc} Supercapacitor voltage

V_{dclink} DC-link voltage

I_a Line current between ac power grid and the voltage source inverter (phase a)

I_b Line current between ac power grid and the voltage source inverter (phase b)

I_{sc} Supercapacitor current

I_{load_a} Load currents (phase 'a')

I_{load_b} Load currents (phase 'b')

Voltage and current transducers are detailed in section 5.3.4.1 and 5.3.4.2 respectively. There are nine signals in total to be fed to the control board as illustrated in Figure 5-1. However, there are eight ADC input channels provided by the control board. Hence, a multiplexer circuit board was required to extend the availability of the ADC inputs as explained in section 5.3.4.3.

5.3.4.1 Voltage measurement

In this research, the measurement of the ac grid voltage, the DC-link voltage, and the supercapacitor voltage were conducted by using the same voltage transducer, LEM LV25-P [98]. The additional components relevant to the voltage measurement circuit are arranged in Figure 5-8. In the figure, the primary resistor is placed at the input of the circuit, in series with the transducer to limit the current to a maximum value of about 10mA. At the secondary side, R_m is used as a measuring resistor to convert the transducer's output current to be an equivalent voltage signal proportional to the original voltage on the primary side.

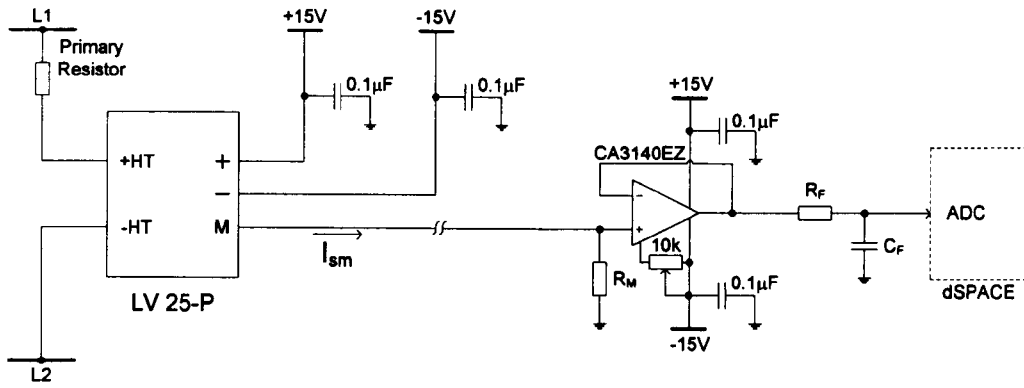

Figure 5-8 Voltage measurement circuit diagram

Before feeding the equivalent voltage signal to the ADC of the control board, it is conditioned by the passive low pass filter (anti-aliasing filter) formed the resistor R_F and capacitor C_F (cut-off frequency = 1.54 kHz, except the filter for DC-link voltage measurement which is designed with the cut-off frequency = 120 Hz). A voltage follower circuit is placed between the transducer's output signal and the filter circuit as shown in Figure 5-8. Both the voltage transducer and the op-amp are fed by the double power supply with +15V and -15V rails. Details concerning design for voltage measurement, including considerations and limitations, can be found in [98].

5.3.4.2 Current measurement

The current transducer is used with the circuit shown in Figure 5-9 to transform the primary current to an equivalent voltage signal. The current transducers, LA 55-P, were used to measure all the currents needed for the control scheme (line current, load current, and supercapacitor current). Details concerning design for the relevant components, including considerations and limitations, can be found in [99]. The voltage follower and the low-pass filter with cut-off frequency = 1.54 kHz are added in the circuit as described for the voltage measurement.

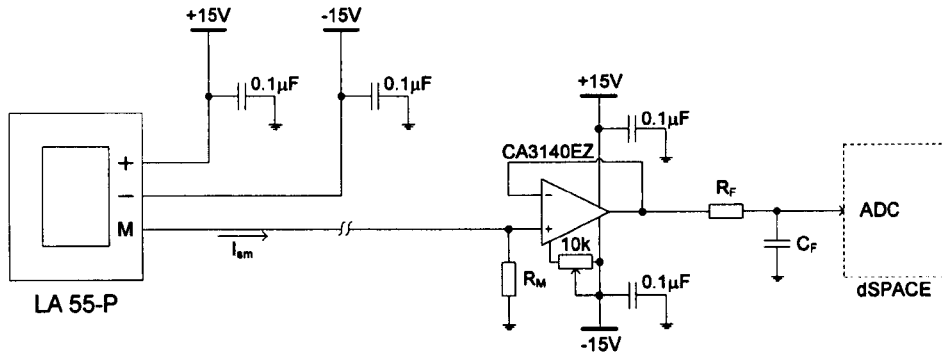

Figure 5-9 Current measurement circuit

5.3.4.3 Analogue data multiplexer

There are nine signals to be measured for this project, but the control board employed in this project has only eight ADC input channels. Therefore, an analogue data multiplexer board was built as shown in Figure 5-10 below.

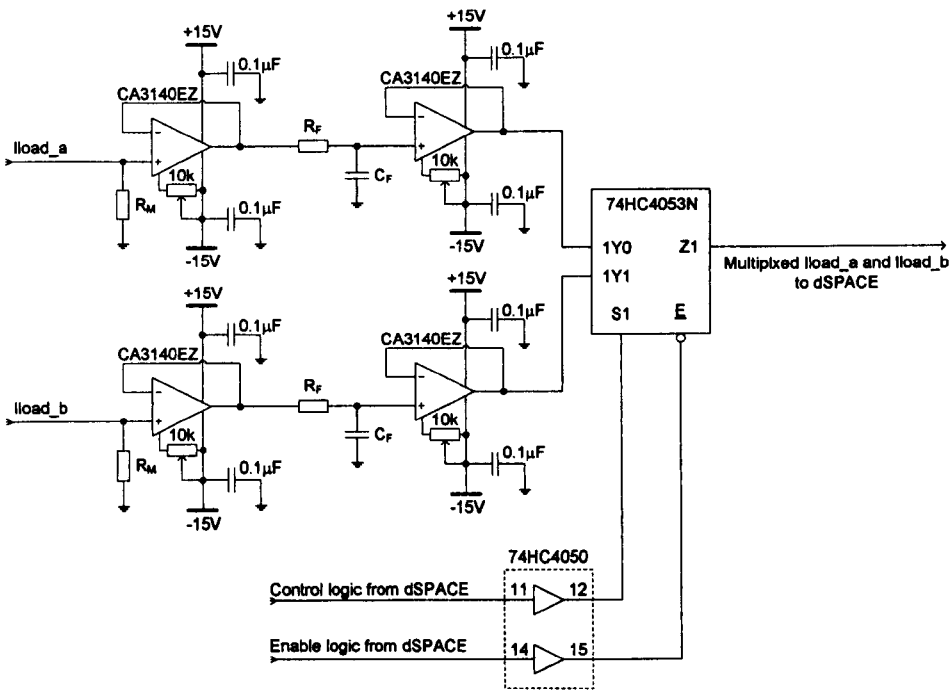

Figure 5-10 Analog multiplexer circuit board

In Figure 5-10, at the input of the board, load current (Iload_a and Iload_b) from the current transducers are fed through the measuring resistors, R_m, resulting in the equivalent voltage signals. These are passed to another voltage follower before feeding to the triple 2-channel multiplexer device MM74HC4053. The practical multiplexer circuit board is shown in Figure 5-11.

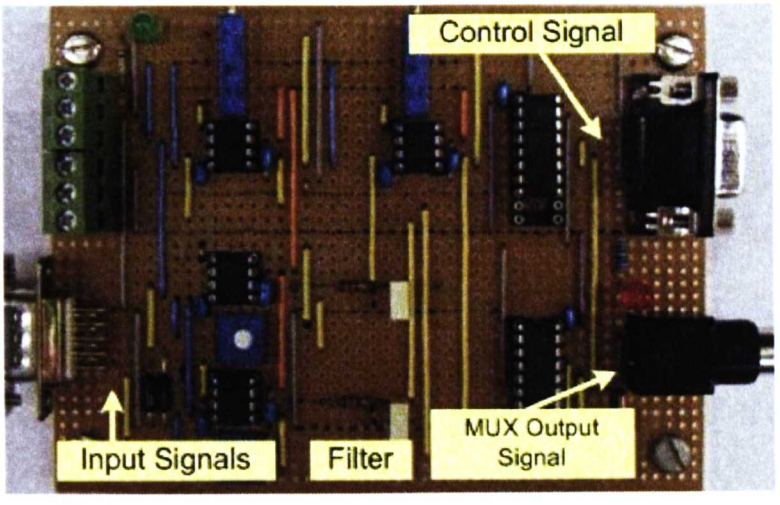

Figure 5-11 The analogue multiplexer board

The control and the enable logic signals are generated by dSPACE (the control board) as in the diagram shown in Figure 5-12. These logic signals are sent via high-speed Si-gate CMOS non-inverting buffers, again to avoid loading error between the multiplexer and the control board.

The multiplexed load current is read from the input ADC ch5, and de-multiplexed by the control logic signal produced by the toggle and flip-flop. This control logic signal is also sent via the master bit ch7 of the control board to the multiplexer board in order to synchronise the de-multiplexed output signal with the input load current signal at the multiplexer board.

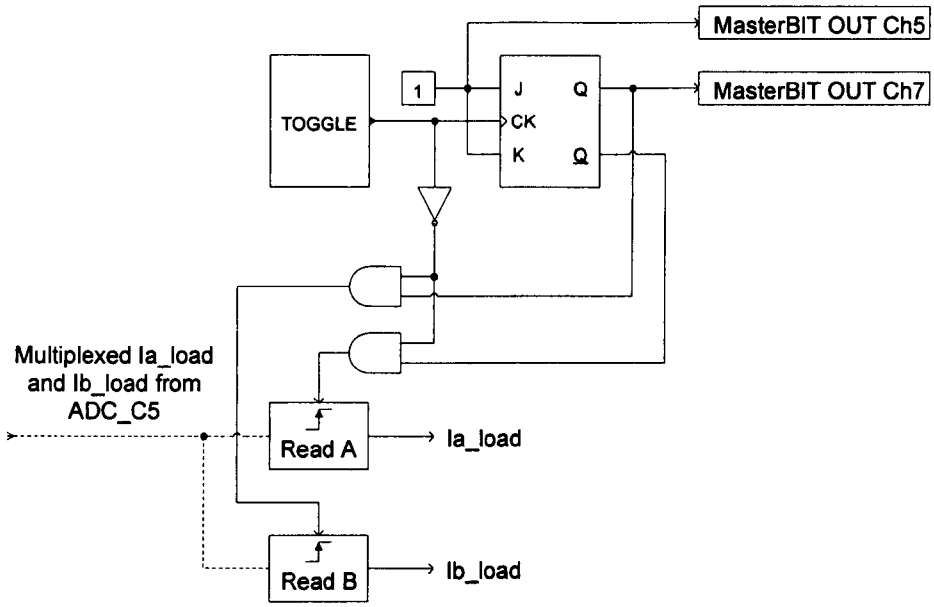

Figure 5-12 The de-multiplexer implemented in dSPACE

5.3.5 Hardware protection and control relaying board

As mentioned in the introduction both software and hardware protection are used. Over-current and over-voltage protection were implemented using hardware circuit. Semiconductor and general line fuses were used as a traditional backup for the over-current protection as shown in Figure 5-1.

Varistors and semiconductor fuses were placed at the front-end of the inverter to form the over-voltage and over-current protection for the STATCOM. An additional circuit board was designed for the over-voltage protection for the DC-link capacitor and the supercapacitor modules as shown in Figure 5-13, where the hardware circuit to control the operation of the high-power switches (S1, S2, and S3 shown in Figure 5-1) is included in this board.

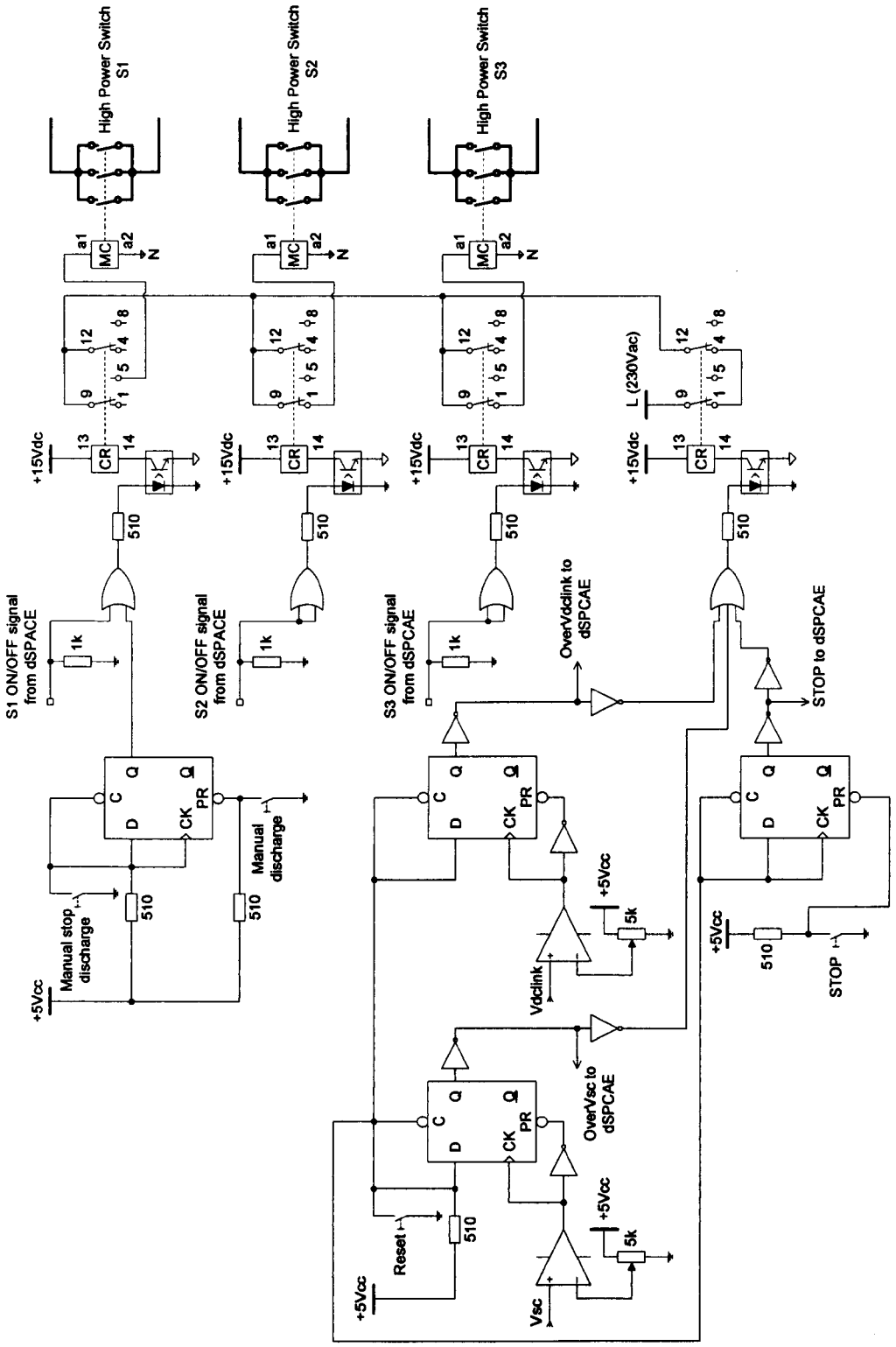

Figure 5-13 The circuit diagram for Vdclink and Vsc hardware protection and control relaying board

In Figure 5-13, the DC-link and Vsc voltage signal from the transducer and amplifier boards are passed to the comparator, LM392N. At the comparator, the reference voltage (setting level) can be adjusted by the 5k variable resistor. When the DC-link or the supercapacitor voltages is greater than the setting level, the output of the comparator will be held as logic high by a D-latch until the reset switch is pushed. The output logic from the D-latch is sent to the optocoupler HCPL 3120 in order to turn on the control relay, which is used to disconnect the power circuit from the power supply and to stop the control.

Furthermore, this board provides three input channels to turn on and turn off the high-power switch S1, S2 and S3. Switch S1 is used to discharge the supercapacitors, which can be controlled by either the signal from the control board or the manual switch as shown in the circuit diagram. Switch S2 is used to connect R_{pre} to the precharge circuit in order to limit the charging current, and is controlled by the control board. Switch S3 is also controlled by the control board to turn on the main load during the experiments. As the control signal cannot be used to turn on and off the high-power switch directly, in Figure 5-13 the optocouplers are used to separate the control from the high power circuit, and then the control relays are used as a power buffer in order to further turn on and off the high-power switches.

5.3.6 The control platform

In this research, the dSPACE DS1104 R&D controller board is employed. This controller board can be plugged into a PCI slot of a PC directly. The controller is based on a 603 PowerPC floating-point processor running at 250MHz. For advanced I/O purpose, the board includes a slave-DSP system based on the TMS320F240 DSP microcontroller [95]. The dSPACE board also comes with the ControlDesk software package standard version 2.5.6 [100] in order to monitor, automate and capture data during the experiments.

The control operation performed by the dSPACE board can be programmed using MatLab/Simulink software package, which is similar to the control operation programming for the simulation work described in chapter 4. More detail of how to program the dSPACE controller board (including the interrupt provided) is described in appendix E.

For the ControlDesk software package, when the control software is loaded into the dSPACE board, the main working area for the ControlDesk can be created as the layout for the relevant elements to be placed in. Basic control elements from the ControlDesk library such as Pushbutton, OnOff button, Slider control, and etc. can be dragged and dropped in the main layout and set linking to the associated variables in order to do online setting during the operation of the controller board. Some instrument panels can be added placing on the main layout. The ControlDesk built-in library also provides the elements for data monitoring such as graph plotters, data display screens or numeric displays. These display elements can be placed in the instrument panels and linked to the related variables. More detail of how to create user interface control layout for the dSPACE board using the ControlDesk software can be found in [100].

For this project, the controller board comes with a connector box which can be used as the input channels for the physical data from the transducer boards, and to pass the PWM signals from the controller board to gating the relevant gate drivers as shown in the functional block diagram of the control platform illustrated in Figure 5-14.

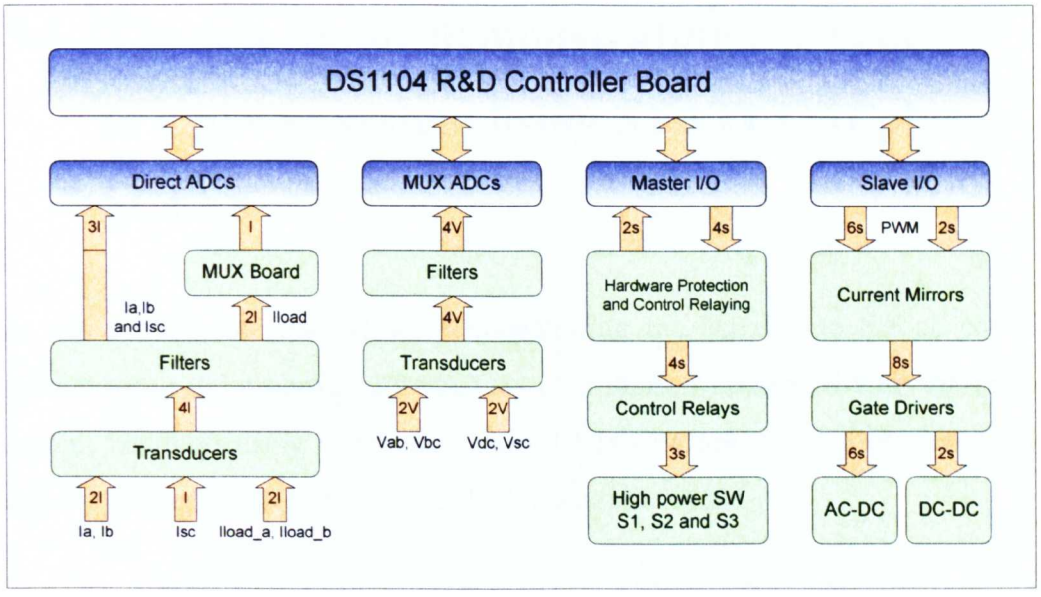

Figure 5-14 The functional block diagram of the control platform

For data acquisition, the connector box of the dSPACE provides eight ADCs channels – four direct ADCs and four multiplex ADCs channels. For this project, the current controller is the key to controlling power flow and is designed with a higher bandwidth than the bandwidth for voltage control. Therefore, to avoid the delay from the multiplexing process, the current signals from the transducers are all connected to the direct ADCs. The voltage signals are then connected to the multiplex ADCs as shown in Figure 5-14.

The master I/O unit is used for interfacing with the hardware protection and control relaying board in order to turn on and turn off the high-power switches (S1, S2 and S3). The slave I/O is used to generate the PWM signals for both the AC-DC voltage source inverter and the DC-DC converter as shown in Figure 5-14.

5.4 The test rig for demonstrating the benefits to a power system using STATCOM plus SCESS

In this section, the test rig for demonstrating the benefits to the ac power system using the proposed STATCOM plus SCESS compared with the same system but with using a conventional STATCOM are detailed section 5.4.1 and the conceptual control is described in section 5.4.2.

5.4.1 The hardware

The overall experimental setup as shown in Figure 5-1 is designed to validate that the ability of the conventional STATCOM is improved by utilising the energy stored in the supercapacitor modules in order to inject and also absorb real power from the ac grid. For clarity, according to the overall experimental setup in Figure 5-1, a single line diagram of the power circuit diagram for the experimental tests is shown in Figure 5-15.

In Figure 5-15 the step-down transformer is used to lower the three-phase supply voltage for the reasons discussed in section 5.3.1. The 5mH inductor is connected between the secondary side of the step-down transformer and V_{pcc} bus in order to highlight the voltage drop due to the load change during the experiments. However, this additional inductance (including the inductance of the step-down transformer and the inductance of the power supply) is the cause of the increase in the switching noise appearing on the voltage waveforms as explained by the equivalent circuit diagram shown in Figure 3-19.

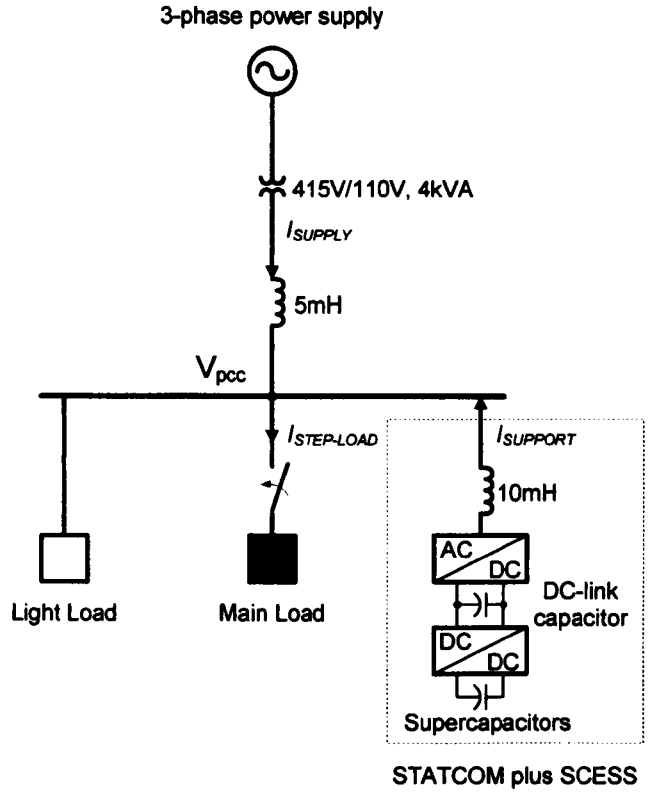

Figure 5-15 Single line diagram of the overall power circuit diagram

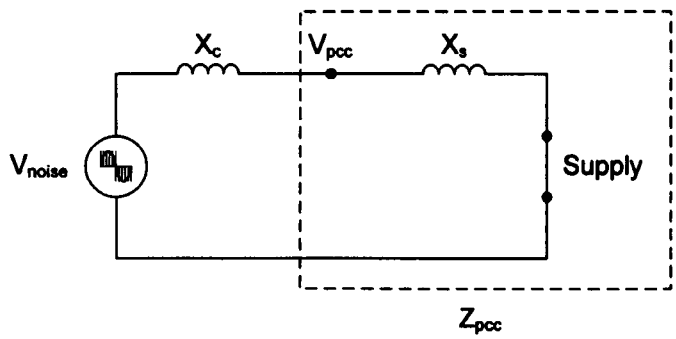

Figure 5-16 Equivalent circuit diagram of the voltage divider formed by the additional inductor.

In Figure 3-19, X_c is the coupling reactance, X_s is the total reactance of the additional 5mH inductor and the leakage of the transformer and the three-phase power supply, and V_{noise} represents the high frequency switching noise generated by the STATCOM unit. It can be seen that the increase in the noise

ripple appearing on the voltage waveforms at V_{pcc} increases with X_s in the equivalent circuit diagram.

In order to reduce the effect of the voltage dividing at Vpcc, the equivalent impedance Z_{pcc} must be reduced. Thus, the light load (50 ohm resistance) is connected in parallel with the X_s as shown in Figure 3-20. Due to the smaller equivalent impedance Z_{pcc}, the noise ripple at V_{pcc} should therefore be reduced.

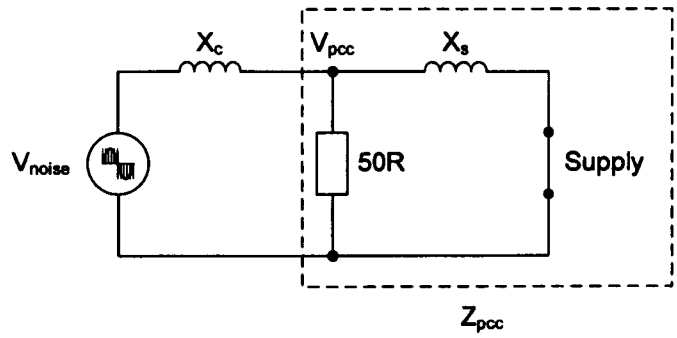

Figure 5-17 Equivalent circuit diagram of the voltage divider formed by the additional inductor and the 50 ohm resistor connected at V_{pcc}.

During the experiment tests, in order to cause the step change in the load current appearing in the system, the main real power load can be switched on to V_{pcc} at anytime by turning on the high-power switch S3. Note also the proposed STATCOM as shown in the diagram in Figure 5-15 can be operated with and without the SCESS in order to highlight the benefits to the ac power system.

5.4.2 The conceptual control

The overall control has three modes of operation i.e. (1) normal STATCOM operation (i.e. supplying reactive power only to the grid), (2) "buck mode"

recharging of the supercapacitors, and (3) "boost mode" supplying real power to the grid.

For mode (1) the DC-Link voltage is controlled by the STATCOM's DC-link voltage controller, and the SCESS can be ignored. In mode (2) "buck mode", the SCESS is controlled in buck mode according the explanation described in chapter 3. A feedforward of the supercapacitor charge current is added to the STATCOM control as shown in Figure 5-18 to draw real power from the ac power grid to the DC-link capacitor via the operation of the STATCOM's DC-link voltage controller. Real power is then transferred to the supercapacitor unit.

In mode (3) "boost mode", the mode is triggered by an external demand – in this case the measurement of a local load current – which acts as a feedforward demand for the controller. To prevent the SCESS "boost mode" control and the STATCOM control fighting each other, the STATCOM's DC link controller is disabled. The energy from the supercapacitors is fed to the ac power grid via the SCESS boost mode operation described in chapter 3, with a feedforward demand as shown in Figure 5-19.

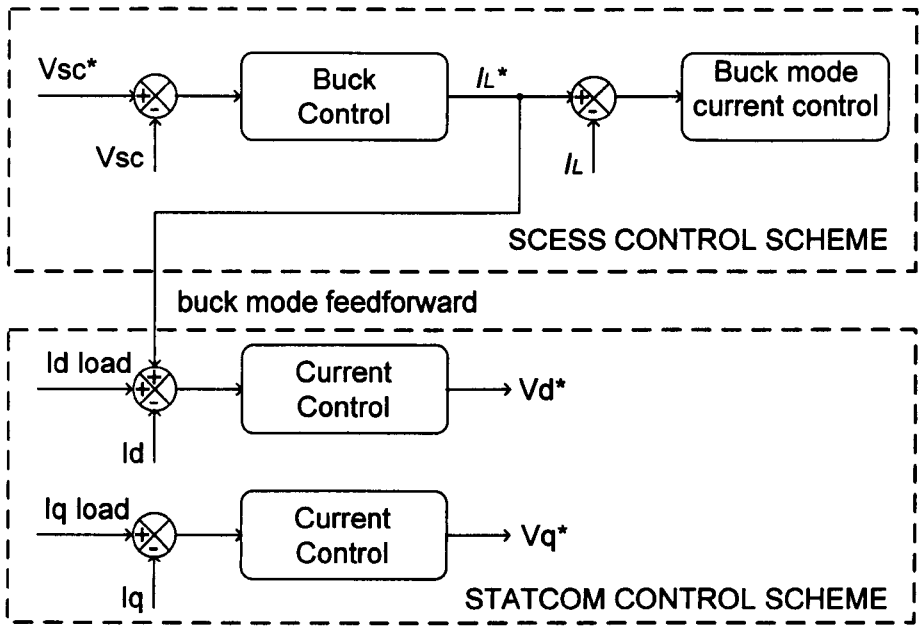

Figure 5-18 Buck mode control diagram (mode 2)

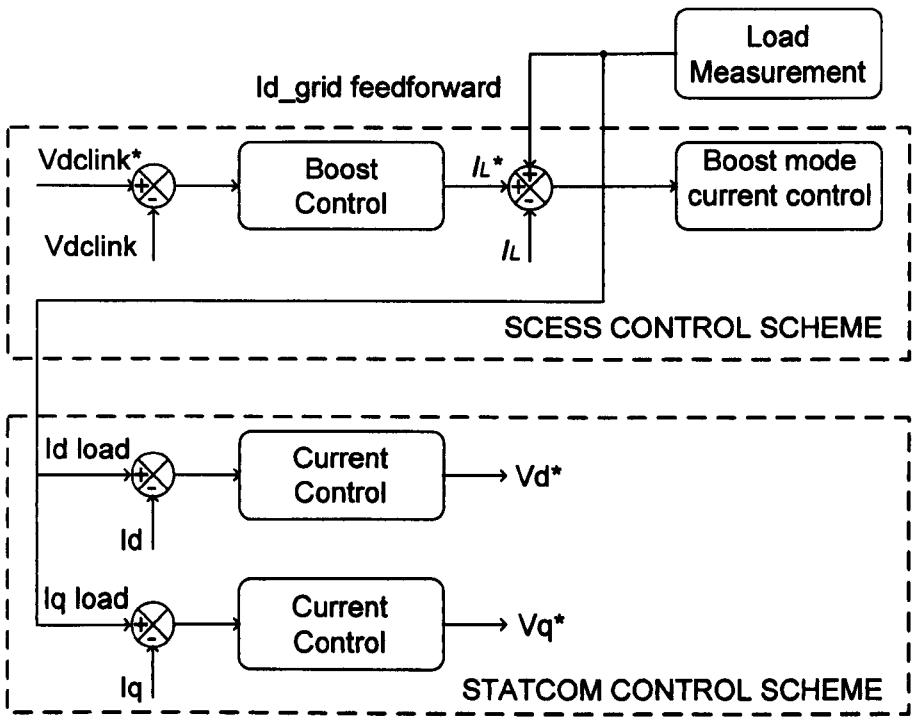

Figure 5-19 Boost mode control diagram (mode 3)

5.5 Conclusions

The experimental rig designed to demonstrate the benefits to the ac power system using STATCOM plus SCESS has been presented in this chapter. The overall rig was used to validate the ability of the enhanced STATCOM which can inject both the real and reactive power to the ac grid instantaneously. Furthermore, this enhanced STATCOM can absorb power from the ac grid and then store the energy in the supercapacitor modules. In the next chapter, the results obtained from the experimental tests using this rig will be described.

Chapter 6

Experimental results

6.1 Introduction

In this chapter results obtained from experimental rig designed and implemented for demonstrating the benefits of an enhanced STATCOM with Supercapacitor Energy Storage System, are presented in order to validate the simulation results of the proposed control scheme, in which the STATCOM control and SCESS control are operated in a coordinated manner.

The aim of this work is to demonstrate the fast dynamic response time of the STATCOM plus SCESS such that even step changes in load can be quickly and accurately tracked. The performance of the full system will be compared with that of the power system on its own, and that of the power system with a conventional STATCOM only.

All experiments described in this chapter are performed using the experiment rig presented previously in Chapter 5. The single line diagram of the experimental test system is shown here again in Figure 6-1.

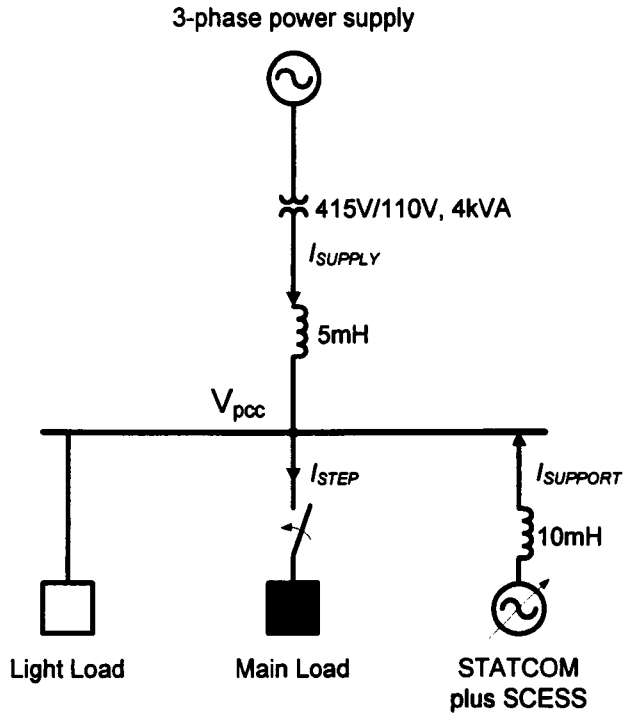

Figure 6-1 Single line diagram of the experimental rig

For clarity, to see the voltage drop due to the load, a 5mH inductance is connected between the three-phase power supply and V_{pcc} bus. However, as discussed in chapter 5, this inductance, including the inductance of the transformer and the three-phase power supply, forms a voltage divider resulting in the appearance of high frequency switching ripple at V_{pcc}. This ripple is at its highest under no-load. Therefore, a light load of about 1.5A is introduced to reduce the ripple as explained in greater detail in the previous Chapters.

The results in this chapter are presented in four main parts indicating the benefits of STATCOM alone and STATCOM plus SCESS. Firstly in section 6.2 the benefit to an ac power system of a conventional STATCOM is

explained by a comparison of experimental results from the system without VAr support and the same system supported by STATCOM alone. Secondly the basic operation of STATCOM plus SCESS, and it performance are presented with experimental results illustrated in section 6.3. Thirdly, the benefits of STATCOM plus SCESS compared with the conventional STATCOM are presented in section 6.4.

The performance improvement is illustrated explicitly in section 6.5. This describes the scenario showing the system operating uncompensated for a short period of time and then fully compensated by STATCOM plus SCESS. The difference and response can be clearly seen.

6.2 Benefits to a power system using conventional STATCOM only

In order to demonstrate the benefits of a conventional STATCOM, the experimental tests are carried out without any power electronic support, where the load is supplied only by the three phase ac power supply. The experimental procedure is as follows (and shown in Figure 6-1). At the beginning of the test, a light load current of around 1.5A is drawn from the three phase power supply. A main load of approximately 7A is switched on at time t=0s, causing a voltage drop of about 2V across the reactance (5mH) connected between the three-phase power supply and the point of common coupling.

At the point of common coupling (V_{pcc}) shown in the top trace of Figure 6-1, it is difficult to see any difference in the three-phase voltage waveforms with the displayed scale. Therefore, the magnitude of the phase voltage $|V_{pcc}|$ is shown separately in Figure 6-2, where it can be seen clearly that V_{pcc} reduces immediately when the main load is switched on. A large drop is seen initially as the power supply can not deliver full power at the instant of step load

demand. As previously mentioned there is no compensation for this first experimental test, and V_{pcc} settles at a voltage lower than rated voltage (V_{pcc}*).

From time t=0s onward, after the main load is connected to V_{pcc}, the supply current of about 8.5A shown in the middle trace of Figure 6-2 indicates that all the load demand is fully supplied by the three-phase power supply. As the power electronic support is not enabled, the DC-link shown in the bottom trace of Figure 6-2 shows that it is not controlled to the demand value of 400V, again indicates a drop in V_{pcc}.

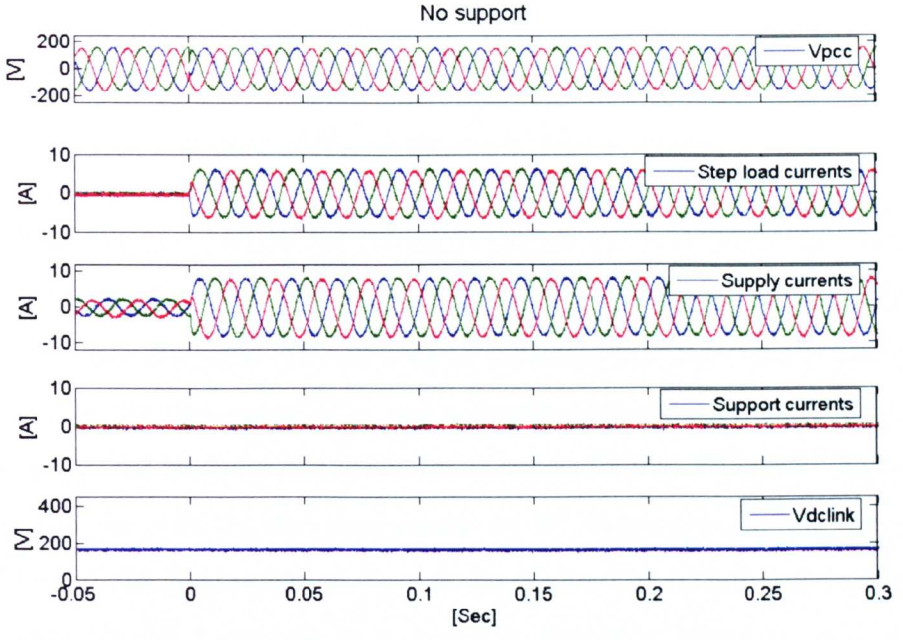

Figure 6-2 V_{pcc}, load currents, and supply currents of the system without support

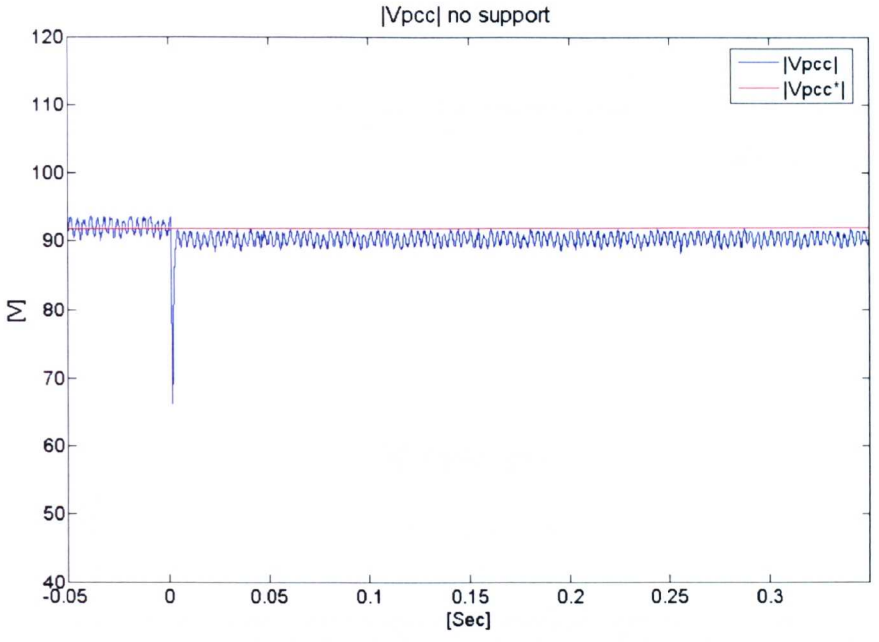

Figure 6-3 $|V_{pcc}|$ of the system without support

Even though this experimental system is carried out with no power electronic converter operating, it is obvious that the voltage waveforms at V_{pcc} shown in Figure 6-3 are distorted. This distortion indicates that the three-phase power supply used for this research is not a purely sinusoidal power supply. The distortion is due to some harmonic components, mainly 5^{th} and 7^{th} harmonics which can be seen in the appearance of 6^{th} harmonics in the frequency spectrum of the magnitude of V_{pcc} as shown in Figure 6-4 and Figure 6-5. Note that the 5^{th} harmonic is a negative sequence harmonic and the 7^{th} harmonic is a positive sequence harmonic, and both appear at 6^{th} harmonic in the magnitude of V_{pcc} when calculated in the rotating d-q frame of reference. This research will not consider these harmonics.

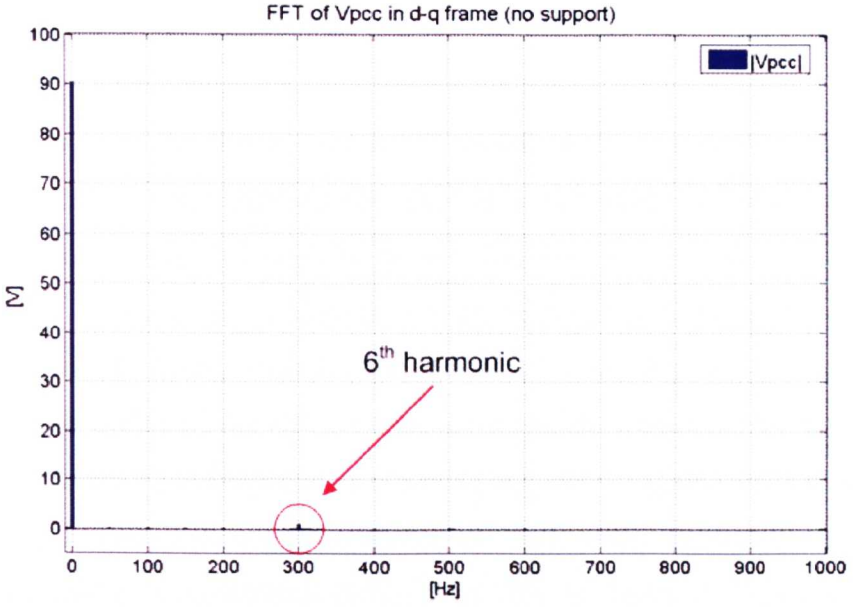

Figure 6-4 Harmonic contents of V_{pcc} in the d-q frame of reference

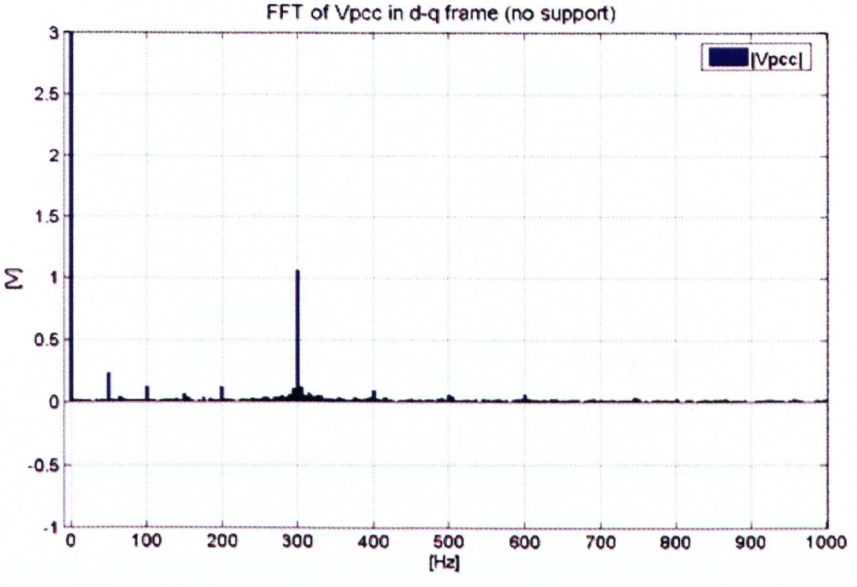

Figure 6-5 Zoom of the 6th harmonic appear in the magnitude of V_{pcc} in Figure 6-4.

Results shown in Figure 6-2 and Figure 6-3 indicate that a steady state voltage drop can be seen at V_{pcc}. Also at the initial instant of step load change, the short duration large amplitude spike in V_{pcc} indicates potential problems with system stability.

For comparison, the same system is tested with a conventional (VAr) STATCOM. This additional device aims to compensate the voltage drop by means of controlling the reactive power flowing between itself and the ac power grid. As described in chapter 3, reactive power control can be achieved by controlling the q-axis current component (I_q) in the d-q frame of reference, therefore the ability of the STATCOM is inevitably dominated by the current reference tracking performance of the current control scheme. In this research the current control is experimentally verified with the response of the proposed control to a step change in I_q* of 10A as shown in Figure 6-6. This result confirms the speed of the operation of the STATCOM used as a reactive power compensator for the proposed system.

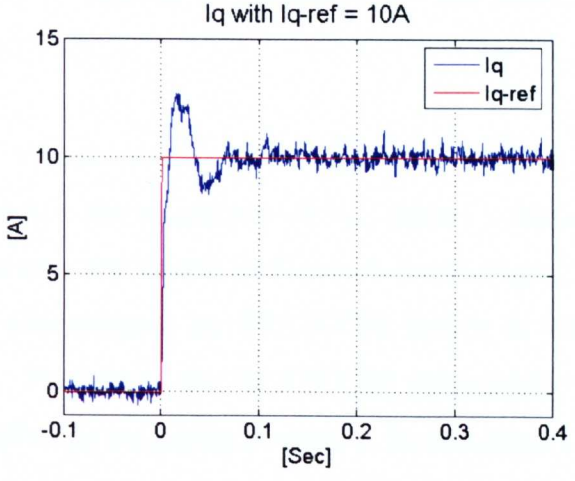

Figure 6-6 Response of q-axis current control to a step change of 10A

The response to a step change of the current control shown in Figure 6-6 is close to the simulation result described in chapter 4. Although a slight difference (oscillation) is seen at the beginning of the response, the overall

trend matches the simulation. More details of this response corresponding to the designed value are given below.

In term of the magnitude, I_q which is captured by the control board shows that it is the same value as the reference value, with no steady error and an overshoot of about 25%. In term of the time constant, its rise-time and setting time take longer than the designed value; the rise-time is about 5ms (2 ms longer than the design), setting-time is approximately 60ms (30ms longer than the design). The difference in time constant between the designed and the captured value is possibly due to the unknown inductance of the power supply, which is not included in the design, the delay of the dSPACE controlled, and also the delay due to the sample and hold effect of the PWM. However this difference is in the scale of milliseconds which is very small compared to the generator response (in seconds). This response confirms that the proposed STATCOM can be used as a power compensator in order to provide the fast power response for a 50Hz ac power system. Another validation for this current control, for both boost and buck mode with voltage and current in a-b-c reference frame, is detailed in section 6.3 - the basic operation of the STATCOM plus SCESS.

Results from the system implemented with a STATCOM are presented in Figure 6-7. For clarity, the magnitude of V_{pcc} (phase voltage) and the current in d-q reference frame are shown in Figure 6-8 and Figure 6-9 respectively. The system was compensated by STATCOM which is based on switching devices (IGBTs). Therefore, the STATCOM unavoidably generates noise components related to its switching frequency. In this research the STATCOM based on a voltage source inverter uses a switching frequency of 5 kHz. As a consequence, components of the switching noise of 5 kHz and its multiples are seen on the voltage waveforms as shown in Figure 6-7 and Figure 6-8.

In comparison of the results shown in Figure 6-7and Figure 6-8 to the simulation results described in chapter 3 (Figure 3-25 and Figure 3-26), it can

be seen that the results in Figure 6-7 match the simulation results described in chapter 3 (Figure 3-25) well although a slight difference is seen at the beginning of the 'support current' waveform. Also the same slight difference appears on the magnitude of V_{pcc} shown in Figure 6-8 compared to Figure 3-26.

The slight difference between the experimental results and the simulation results is due to the response of the current control as shown in Figure 6-9 compared to the simulation result shown in Figure 3-27 of chapter 3. Although the same current controller and V_{pcc} controller are implemented for both the simulation and the experiment, the delay due to the digital controller board including the transducer circuit boards, and the precision of the circuit components may cause this slight difference at the beginning of the response. However, the overall of the experimental results is very close to the simulation results as described in the followings.

In Figure 6-7 and Figure 6-8, prior to the load change, only the light load of about 1.5A is drawn from the three-phase power supply. The harmonics can be seen clearly as the switching noise on the voltage waveforms. The STATCOM is enabled and the DC-link is controlled at 400V, the magnitude of V_{pcc} is not different from the reference value, and therefore no compensation is needed.

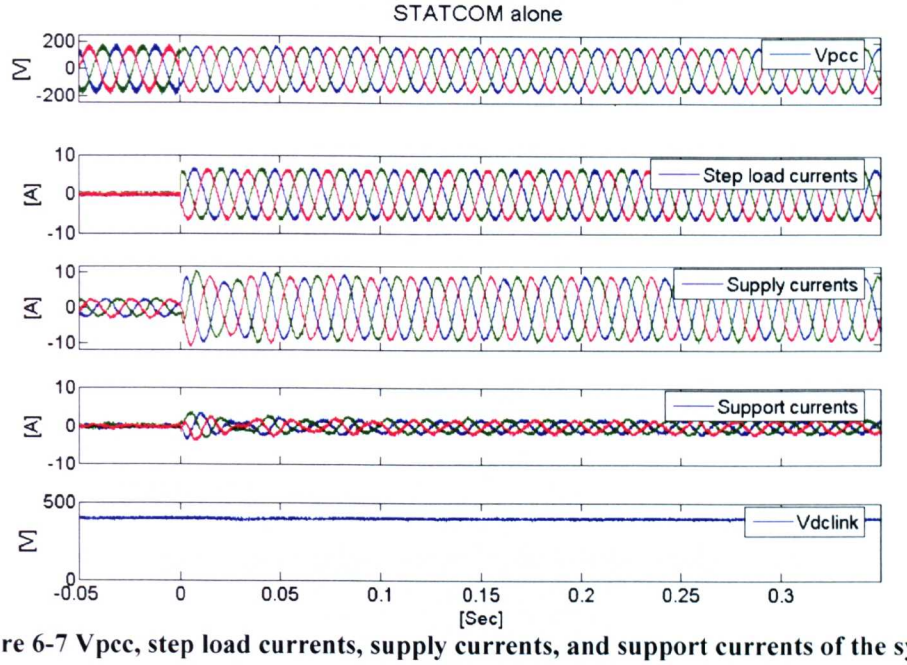

Figure 6-7 Vpcc, step load currents, supply currents, and support currents of the system with STATCOM only

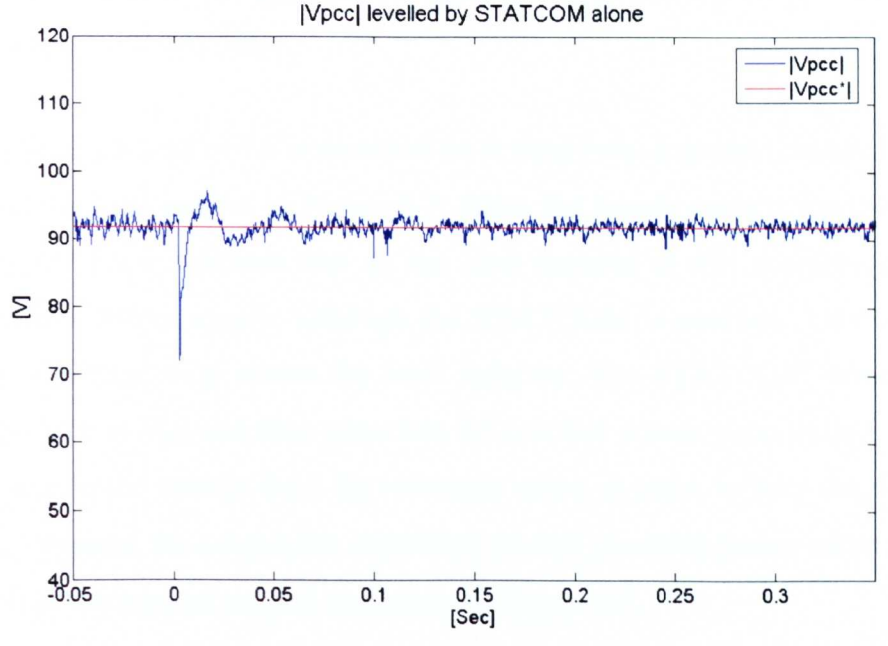

Figure 6-8 $|V_{pcc}|$ of the system with STATCOM only

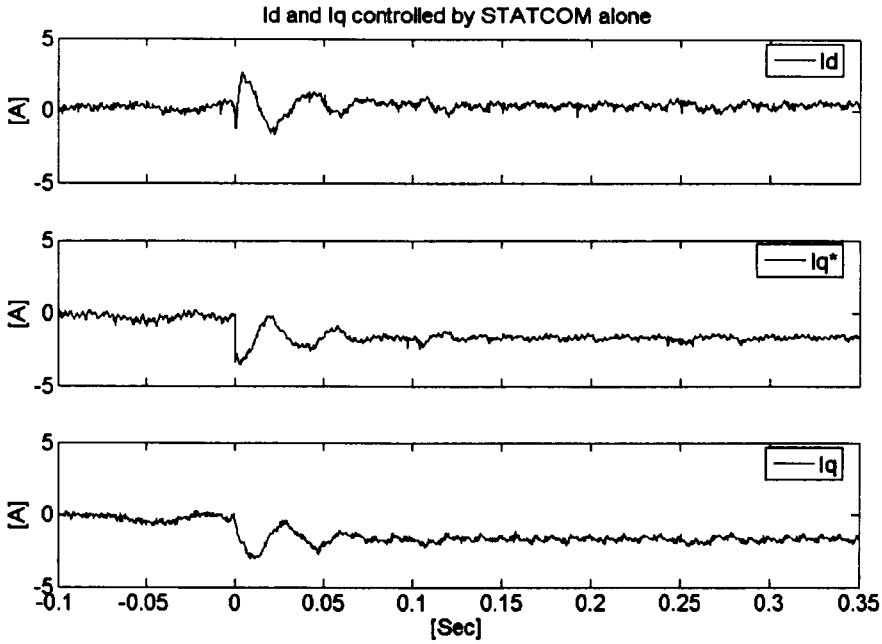

Figure 6-9 The controlled I_d and Iq for the system with STATCOM only

The harmonic spectrum of the phase voltage at V_{pcc} is shown in Figure 6-10 where the harmonics appear as sidebands centered around the switching frequency and its multiples.

When the main load of 7A is switched on at time t=0s, a sudden change can be seen on the load current in Figure 6-7. Also, the supply current waveform in the middle trace indicates that all the load demand is still supplied by the three-phase power supply, although the STATCOM is enabled. This current causes a voltage drop across the 5mH inductor. The STATCOM detects the voltage drop at V_{pcc} and then generates the reactive power, proportional to the difference in the voltage from the reference value, in order to keep the voltage at V_{pcc} constant. As a result the controlled current (reactive power current) can be seen as the support current waveform in Figure 6-7.

The controlled I_d and I_q are illustrated clearly in Figure 6-9 where the bottom trace shows the reactive power current produced by the STATCOM in responding to the drop in V_{pcc}. At the time when the main load is switched on,

the STATCOM quickly reacts to the sudden voltage drop by supplying the reactive power current (negative I_q) to the ac grid. According to this reactive power current, the magnitude of V_{pcc} increases rapidly as shown in Figure 6-8. Consequently, as V_{pcc} is controlled by the STATCOM, the amount of the reactive power injection is therefore reduced proportional to the increase of the magnitude of V_{pcc}. As a result, an overshoot in the magnitude of V_{pcc} relating to the controlled I_q current can be seen between time t = 0s and t = 25ms before V_{pcc} settles at 92V, and the I_q current settles at about -1.5A as shown in Figure 6-8 and Figure 6-9 respectively.

During this period, due to the STATCOM supplying current to the ac grid, a small drop in the DC-link voltage is seen, as some energy in the DC-link capacitor is needed to supply losses in the system, for example, the IGBT switching and conduction losses. According to the STATCOM's DC-link voltage control reacting to this drop in order to maintain the DC-link constant, a small amount of the active power current (I_d) is seen in the top trace of Figure 6-9, where the initial overshoot is the result from the reaction of the control to the DC-link voltage error during time t=0s and t=25ms before settling at the value of less than 0.5A.

As explained previously in section 3.5 of Chapter 3 that harmonic distortion due to the switching noise on the voltage waveforms in Figure 6-10 will be reasonably reduced when the main load is introduced to V_{pcc}. As shown in the circuit diagram of Figure 3-21 the reduction of switching noise is due to the system configuration of the coupling reactance (X_c) and the equivalent impedance at V_{pcc} (Z_{pcc}). The load change (increase in load current) results in a smaller impedance Z_{pcc}. The noise appearing on the voltage measured at V_{pcc}, due to the dividing of the noise voltage (V_{noise}) across Z_{pcc}, should therefore be reduced. As expected, after the load change, the spectrum of the voltage at V_{pcc} shown in Figure 6-11 confirms experimentally that the noise is reduced.

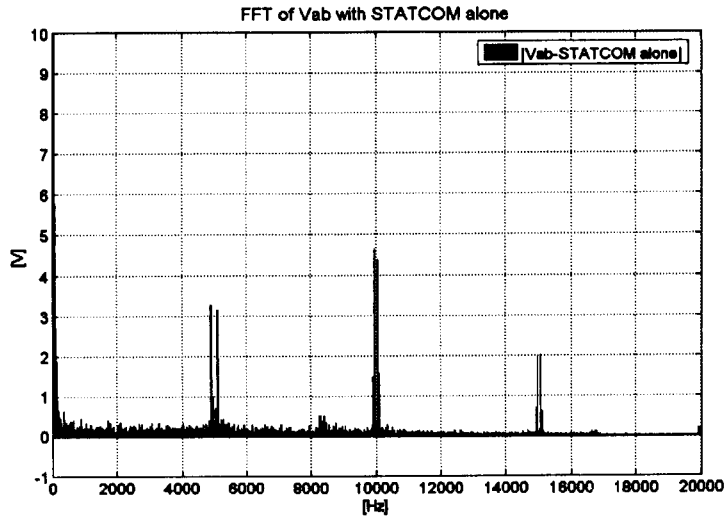

Figure 6-10 Harmonic content of V_{pcc} prior to the load change

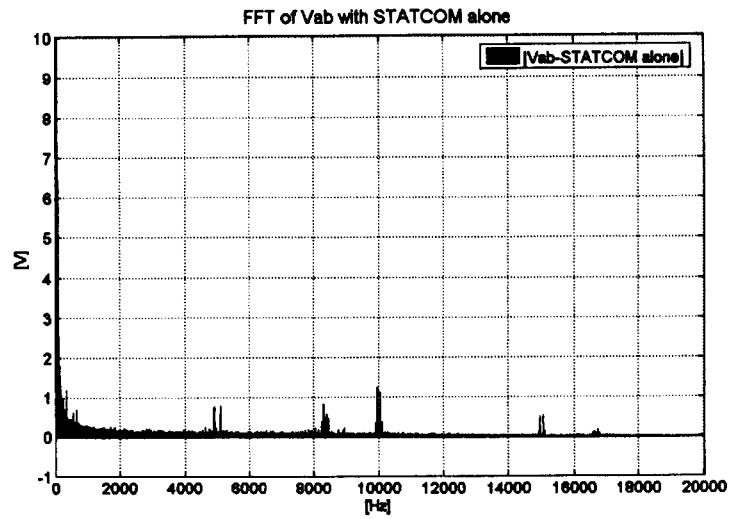

Figure 6-11 Harmonic content of V_{pcc} after the load change

A comparison of the system with and without a STATCOM (Figure 6-7 compared with Figure 6-2) shows approximately 1.25A of current flows from the STATCOM unit as support currents, i.e. that the voltage drop is being compensated by reactive current. Comparison of the results in Figure 6-8 with

Figure 6-3 shows a clear benefit of the STATCOM's capability as a voltage supporter. In Figure 6-8, according to the STATCOM's reactive power support, V_{pcc} is controlled at its rated value even under heavy load.

From the results it can be seen that the STATCOM can be applied as a reactive power flow controller. As explained in section 4.3 a STATCOM, however, with limited amount of stored energy in a conventional DC-link capacitor, can not deliver real power to ac grid. Even though the STATCOM can keep the ac bus voltage constant by means of reactive power injection, it is obviously noticeable that, in Figure 6-7, most of the load current is being supplied by power source side (generator side).

6.3 Basic operation of STATCOM plus SCESS

To improve the capability of the STATCOM used in section 6.2, its DC side is interfaced to an energy store in order to be able to inject and/or absorb real power from the ac grid. The SCESS maintains the DC-link voltage constant during the process of real power exchange between the STATCOM and the ac grid. Consequently this enhanced STATCOM can inject real power to the grid independently without interaction from the STATCOM's DC-link voltage control as described in Chapter 4 section 4.4. Moreover, with the SCESS unit, an excess power at the ac grid side can be transferred to the energy store when conditions allow it to operate in real power absorption mode.

The principle for a STATCOM to deliver real power is described in the d-q control in Chapter 4 where active or real power can be controlled by controlling the d-axis current component in the d-q reference frame. The performance of the current control used for real power compensation, the same controller as used in reactive power compensation in section 6.2, is verified again but this time by the reference tracking of the d-axis current component to a step response of 10A as shown in Figure 6-12. In reality, I_d is negative to

indicate the power boost mode. While positive I_d indicates the power buck mode.

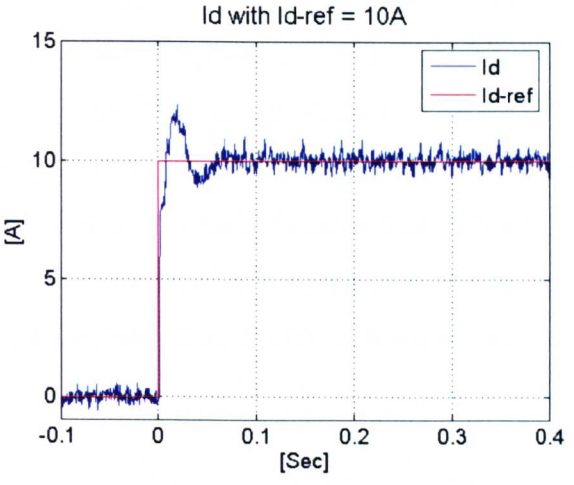

Figure 6-12 Response of d-axis current control to a step change of 10A

Compare to the simulation, the experimental result shown in Figure 6-12 matches the simulation results described in chapter 4 (Figure 4-10), although the slight difference in the settling time is seen as described previously for Figure 6-6.

In Figure 6-12 the same controller is applied for both I_d and I_q control. The response to the step current reference illustrated in Figure 6-12 is similar to the response shown in Figure 6-6, where the overshoot, steady state error, and time constant are the same as detailed in section 6.2. In this section the performance of this current control is also verified clearly with the phase voltage and current during the boost and buck operation.

The ability to supply and absorb real power of the proposed STATCOM plus SCESS is clearly presented with phase angle relationship of the current and voltage at V_{pcc} as shown in Figure 6-13, Figure 6-14, and Figure 6-15. The DC-link voltage, supercapacitor terminal voltage, and supercapacitor current during real power injection and absorption are presented in these figures.

In Figure 6-13 the proposed STATCOM plus SCESS unit is operated in boost mode and synchronised with a V_{pcc} phase voltage reference of $230V_{p-p}$, DC-link voltage of $400V_{dc}$, and supercapacitor voltage of $200V_{dc}$. The aim is to inject real power to the ac grid, and therefore a value of 10A real power current demand has been imposed on the STATCOM unit at time t=0s (negative I_d-demand), resulting in the sudden increase of phase current to a peak of 10A (only phase 'a' of the phase voltages and currents are shown in the figure for clarity). It can clearly be seen that the STATCOM is injecting real power into the ac power system –the phase voltage (V_a) and the line ac current (I_a) are 180 degree out of phase as seen in the lower trace of Figure 6-13.

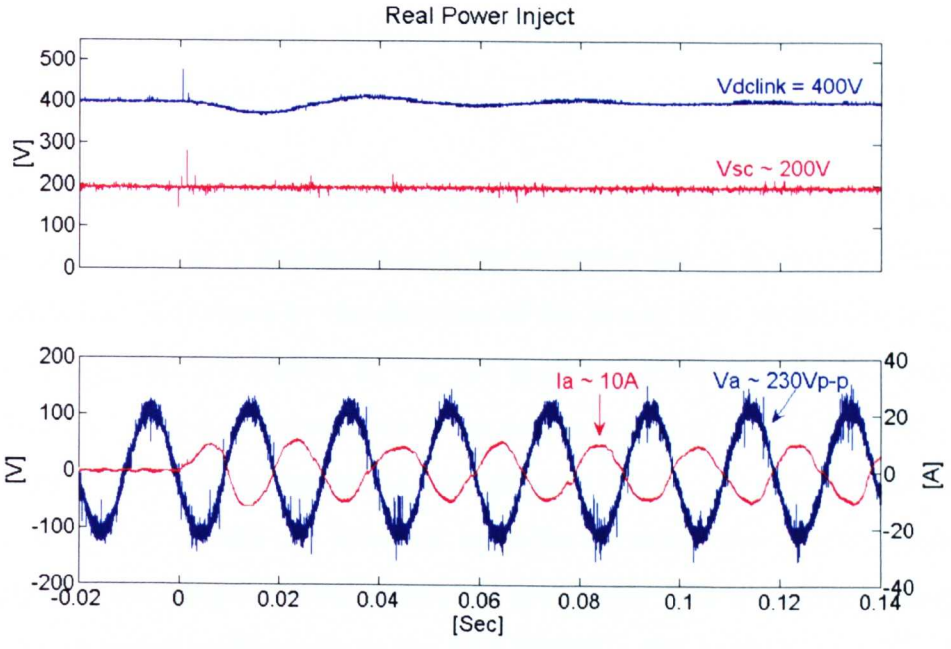

Figure 6-13 Vdclink, V_{sc}, V_a, and I_a during the period when the STATCOM plus SCESS inject real power to grid

Figure 6-13 shows that the experimental results during boost mode (real power inject to the ac grid) match well the simulation results presented in chapter 4 (Figure 4-11). Only the slight difference due to the highly noise is seen on

phase voltage waveform (the bottom trace of Figure 6-13) when compared to the simulation results. More details are described in the following.

A noticeable drop, approximately 7%, appears in DC-link voltage between t=0ms and t=30ms. During this period, the SCESS is not operating and energy from the DC-link capacitor at the STATCOM side is being transferred to the ac power system. This DC-link voltage however is controlled by the SCESS under boost mode and this quickly reacts; the boost mode operation takes stored energy from supercapacitor modules and feeds it to the DC-link capacitor to stabilise and maintain the DC-link voltage constant. The whole process in this mode shows stored energy is being utilised by the SCESS unit; controlling the flow of power from the supercapacitor modules to the ac side. The boost mode process finishes with the supercapacitor terminal voltage slightly lower, as seen in the middle trace of Figure 6-13. The drop is related to the energy transferred to ac power system and losses in the STATCOM.

In Figure 6-14 the results from supercapacitor charging mode are shown, where the real power is demanded from the ac power grid at time t=0s. Power absorption can be realised by the direction of the power flow. In this mode the phase voltage and line current at V_{pcc} are in-phase (lower traces); indicating real power is being transferred from the ac power system to the STATCOM dc side. The STATCOM I_d-demand is now positive. At the time the demand is made, the line ac current (I_a) increases up to the demand value of 10A, under the action of the current control mentioned previously. The transferred energy from the ac power system side to the STATCOM's DC side gives energy to the DC-link capacitor, causing the DC-link voltage to increases until the SCESS takes control as the overshoot of about 3.5% shown in the upper trace of Figure 6-14.

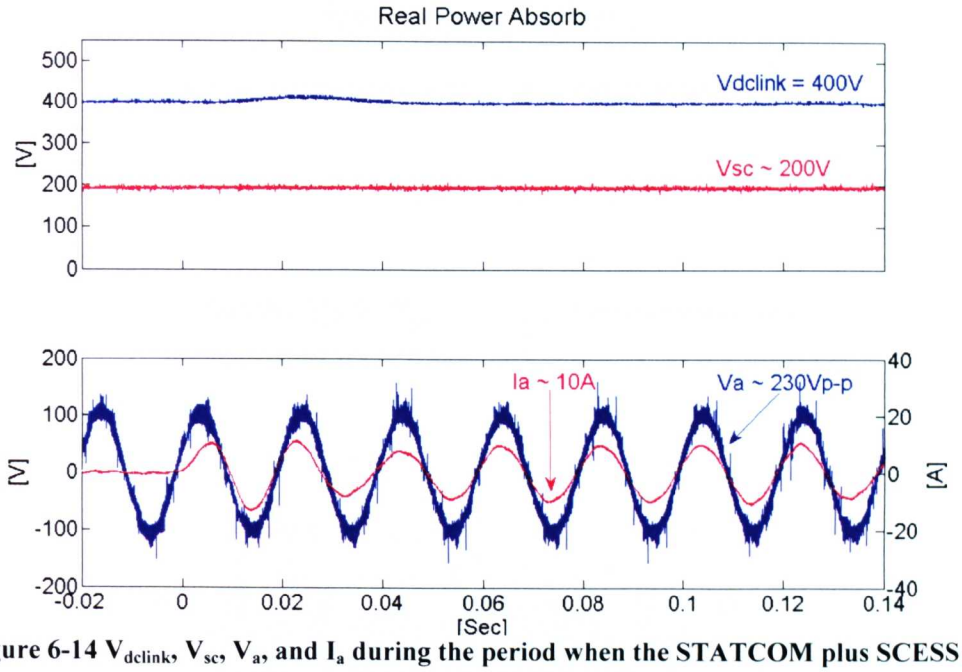

Figure 6-14 V_{dclink}, V_{sc}, V_a, and I_a during the period when the STATCOM plus SCESS absorbs real power from grid (i.e. charge the supercapacitors)

Figure 6-14 shows again that the experimental results match the simulation results well, only a slight difference due to the highly noise is seen in this result when compared to the simulation result in Figure 4-12 of chapter 4.

In this mode the over voltage (overshoot) at DC-link is controlled at 400V by buck mode operation of the SCESS control. The supercapacitor current is flowing in the direction such that energy can be stored in the supercapacitor modules, resulting in a slightly increase of supercapacitor voltage.

With a very large value of capacitance in the supercapacitor modules (9.5F at 200V) the decrease and increase in their terminal voltage following the process of energy injection and absorption is difficult to see over the short period of the experimental tests. For the purpose of showing the supercapacitor voltage clearly during the whole cycle, the experiments for both energy injection and absorption are set up to 30s and 40s duration respectively. The results are shown below in Figure 6-15.

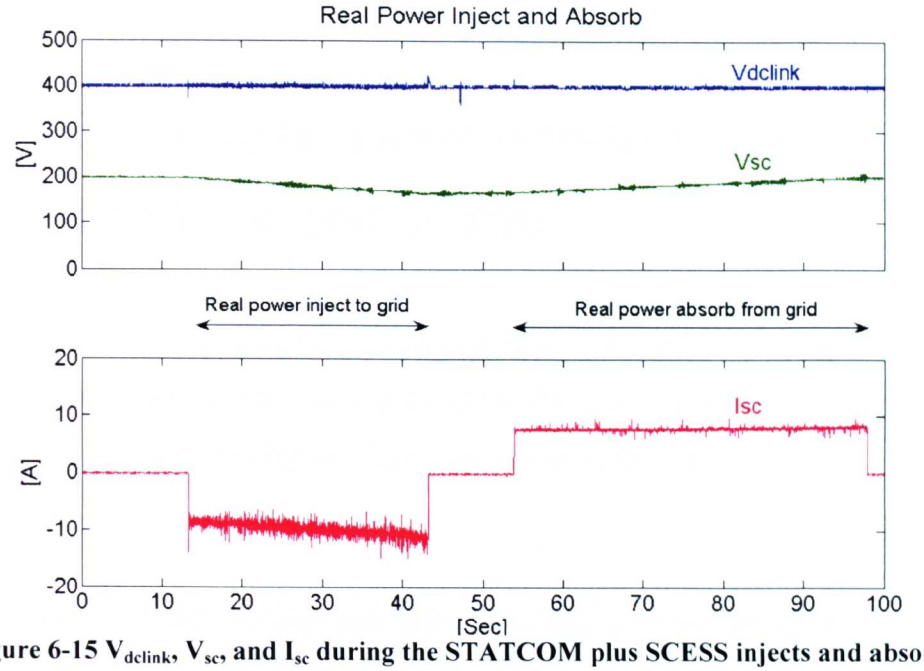

Figure 6-15 V_{dclink}, V_{sc}, and I_{sc} during the STATCOM plus SCESS injects and absorbs real power.

It can be seen clearly that the supercapacitor voltage, V_{sc} (middle trace of Figure 6-15), is 200V at the beginning of the real power injection cycle, and then reduces at a fairly constant rate (between time t= 13s to 43s) as the boost mode delivers approximately 10A to the grid. The decrease of the supercapacitor terminal voltage (V_{sc}) is due to the supercapacitor supplying its stored energy to the grid with approximately 10A current flowing out of supercapacitor modules. As the terminal voltage of the supercapacitors decreases, the supercapacitor current has to increase in order to maintain the same amount of power being transferred to the ac grid. It can be seen that the rate of the increase in supercapacitor current is similar to the rate of decrease of its terminal voltage.

Between time t = 53s and 98s real power is absorbed from the grid and stored in the supercapacitor modules. The value of V_{sc} from the previous power injection process is increased proportional to the current flow into the

supercapacitor modules. This demand current is controlled by the SCESS unit, constant at about 8A for this example result.

6.4 Benefits to the power system using a STATCOM plus SCESS

To demonstrate the benefits of STATCOM plus SCESS compared with STATCOM alone, it has been applied to the same system as described in section 6.2 and 6.3. Results are shown in Figure 6-16, Figure 6-17 and Figure 6-18.

As mentioned in the previous sections, it is difficult to see the dynamic of the three-phase voltage waveforms with the displayed scale in Figure 6-16. The magnitude of V_{pcc} is therefore shown separately in Figure 6-17, and for clarity the controlled currents are shown in Figure 6-18 . In Figure 6-16 and Figure 6-17, at the beginning period of this experiment (from time t= -50ms to t= 0ms), the STATCOM plus SCESS is only enabled to operate as a conventional STATCOM to maintain V_{pcc} voltage at the reference phase voltage of 92V. Therefore, the same results as described in section 6.2 can be seen during this period. The middle trace of Figure 6-16 shows approximately 1.5A flowing from the three-phase power supply to V_{pcc} bus –for supplying the light load and for the STATCOM to maintain its DC-link voltage at 400V (STATCOM's losses) as shown in the bottom trace of Figure 6-16.

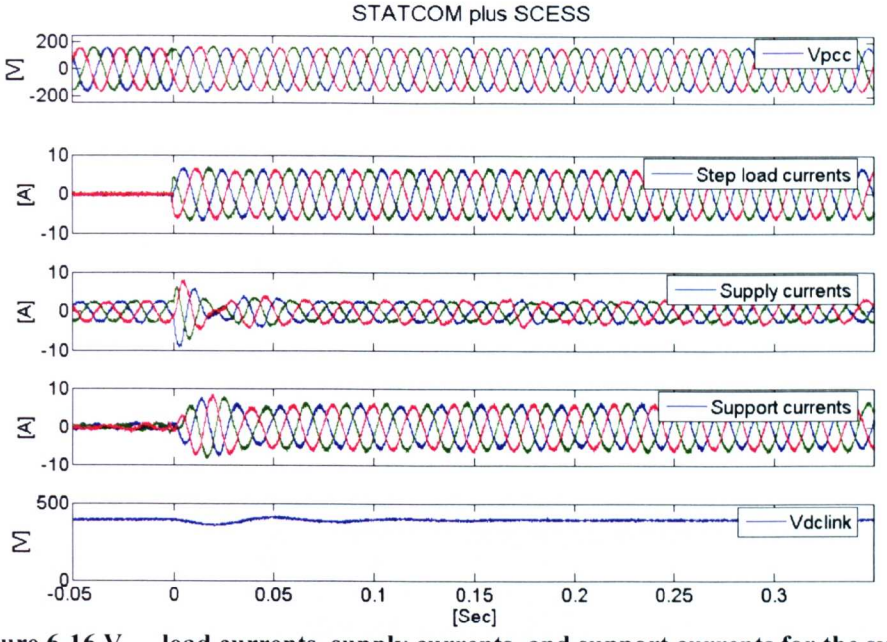

Figure 6-16 V_{pcc}, load currents, supply currents, and support currents for the system with STATCOM plus SCESS

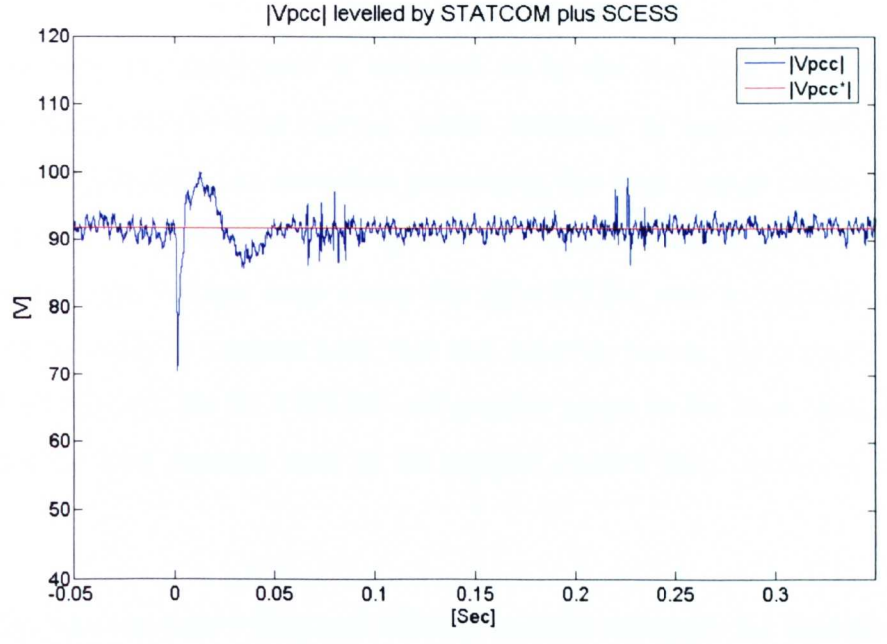

Figure 6-17 $|V_{pcc}|$ of the system with STATCOM plus SCESS

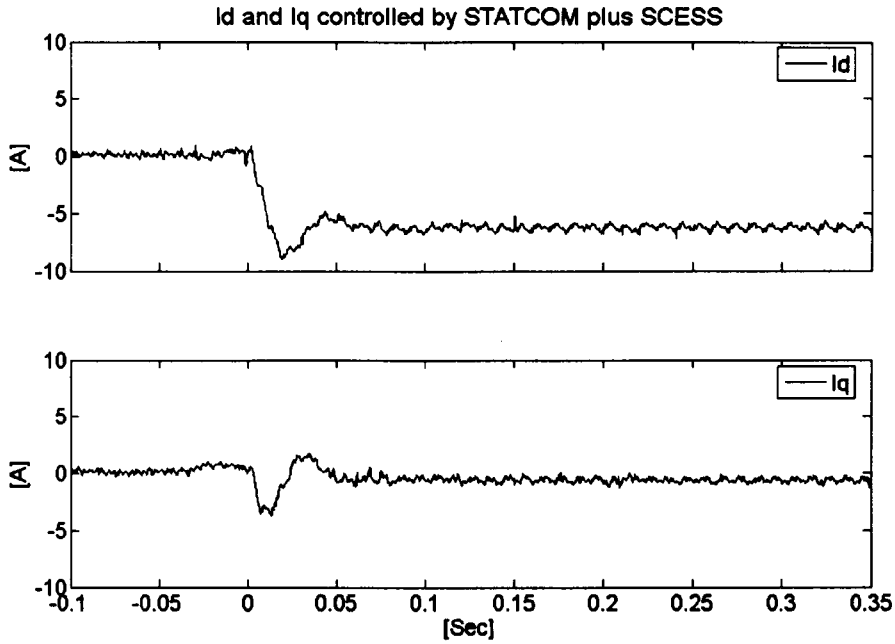

Figure 6-18 The controlled I_d and I_q for the system with STATCOM plus SCESS

At time t=0s, the main load is switched on to the V_{pcc} bus, resulting in a sudden change of the load current, which increases to approximately 7A as shown in Figure 6-16. As described previously, the load change causes a large voltage drop at V_{pcc} as shown in Figure 6-17. At this moment, the sudden load change and the voltage drop cause the STATCOM unit to operate in full function in order to support both real and reactive power. As a result, from time t=0s onward, the STATCOM unit quickly reacts to the load change, and supplies the load demand seen as the support current trace shown in Figure 6-16.

Initially, between time t=0ms and t=25ms, in order to supply the load demand, the STATCOM takes energy from the DC-link capacitor and delivers it to the ac side. During this period, the SCESS is not operating, resulting in a drop in the DC-link voltage until the SCESS starts operating at time approximately t=25ms as shown in the bottom trace of Figure 6-16. This DC-link voltage is

controlled by the SCESS. When it reacts in this boost mode operation, the SCESS takes the stored energy in the supercapacitor modules to the DC-link capacitor, resulting in the rise in the DC-link capacitor from time t = 25ms to t = 50ms. With the control, this rise in the DC-link voltage settles at rated value of 400V. As a consequence, an oscillation in DC-link voltage can be seen in Figure 6-16. For the whole process i.e. the boost mode described in section 6.3, the stored energy in the supercapacitor is utilised and transferred to the ac power system, with a rate that is proportional to the demand from the ac side. The supercapacitor terminal voltage reduces according to the amount of the energy transferred.

At the same time, the STATCOM control reacts quickly to the voltage drop at V_{pcc} and supplies reactive power to the V_{pcc} bus in order to maintain the magnitude of V_{pcc} constant as illustrated in Figure 6-17. The demand of this reactive power is extracted from the error in V_{pcc}, the same as in section 6.2. Both the active and reactive power currents are controlled as shown in Figure 6-18. For the real power support, according to the scenario described in the earlier sections, the real power support current (I_d) can be seen at the time when the main load is switched on. The demand for this real power injection to the ac grid is resolved from the main load current. As described in section 6.3, as the response to step load current, an overshoot in the controlled I_d is seen at the beginning of the support, and finally settles at about 7A.

Although the same interrupt signal is used for the whole control system, the PWM signals generated from the dSPACE controller board for the STATCOM and the SCESS are not synchronised with each other. As a result, this effect causes some distortion on the V_{pcc} waveform as shown in Figure 6-17.

For the reactive power support, the same behaviour as described in section 6.3 that the value of the reactive power to be injected to the ac grid is resolved from the error in V_{pcc}. However, the main load is fully supplied by the

STATCOM unit. As a result, the three-phase ac system supplies only a small current of approximately 1.5A to the light load, resulting in a much less voltage drop across the system reactance (X_s). A similar trend of the controlled I_q (reactive power support current) as described in section 6.3 is seen again, but this time it settles to only about -0.35A.

The results in Figure 6-16 can be compared with the results in Figure 6-7. The voltages of the two different systems are compensated when the step load is switched on at time t = 0s, There seems to be no difference between the three phase voltage waveforms of V_{pcc}, supported either by STATCOM alone or STATCOM plus SCESS. The significant difference can be seen on the current waveforms - both the supply current and the support current. There is a small support current in Figure 6-7, when the system is compensated by a STATCOM alone (only small amount of reactive current flowing to keep V_{pcc} constant). However in Figure 6-16 the STATCOM current is being generated to supply the main load current.

In comparison of the results in Figure 6-18 with the results in Figure 6-9, it is clearly indicated that the capability of the conventional STATCOM is enhanced by the SCESS. The combined system can supply real and reactive power to the ac grid – the controlled I_d in Figure 6-18 shows that the real power is being transferred to the ac power system, while the controlled I_d in Figure 6-9 shows that the conventional STATCOM absorbs some of the real power as it is needed to supply the losses as mentioned earlier. Also, the STATCOM plus SCESS can react quickly to the step change in load, and can therefore potentially be used to balance power flow when, for example, a slow mechanical governor is required to react.

6.5 Comparison of a system with and without STATCOM plus SCESS

In this section the experimental test is set up as in section 6.4, but with a slight delay in the operation of the STATCOM plus SCESS in order to highlight its behaviour. The STATCOM plus SCESS is enabled at time t= 70ms. Three-phase voltage and current, magnitude of V_{pcc}, and real and reactive power current are shown in results in Figure 6-19 , Figure 6-20 and Figure 6-21 respectively. At the beginning, from time t = -50ms to t = 0ms, the same initial setting as described in section 6.4 is applied to the experiment in this section. Therefore, during this period, the same results can be seen in the figures. Similar to the previous sections, for the STATCOM, in order to operate and maintain the DC-link voltage at the reference value of 400V, a very small current flows from V_{pcc} bus to the STATCOM unit as can be seen in the Figure 6-19 and Figure 6-21.

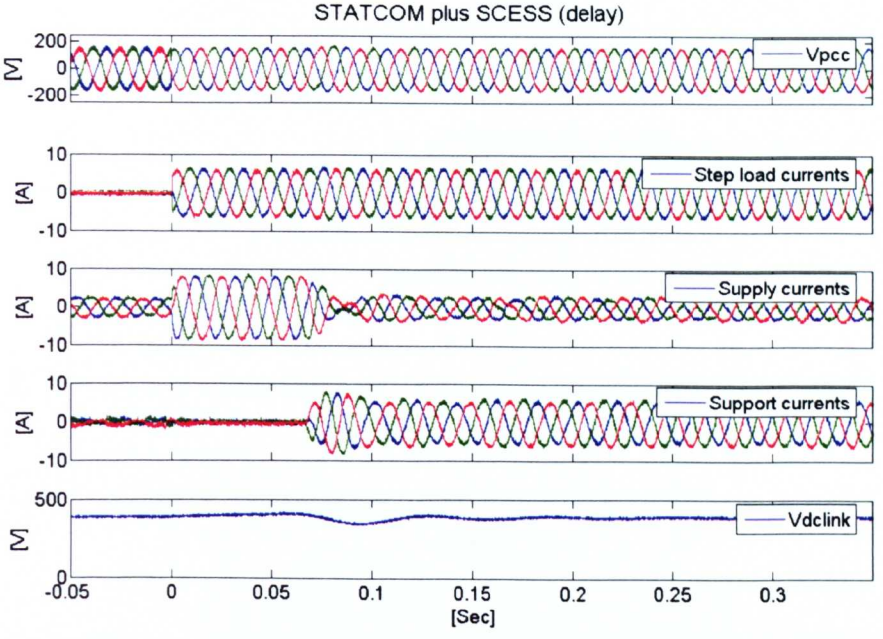

Figure 6-19 V_{pcc}, load currents, supply currents, and support currents of the system with STATCOM plus SCESS when its operation is delayed by 70ms.

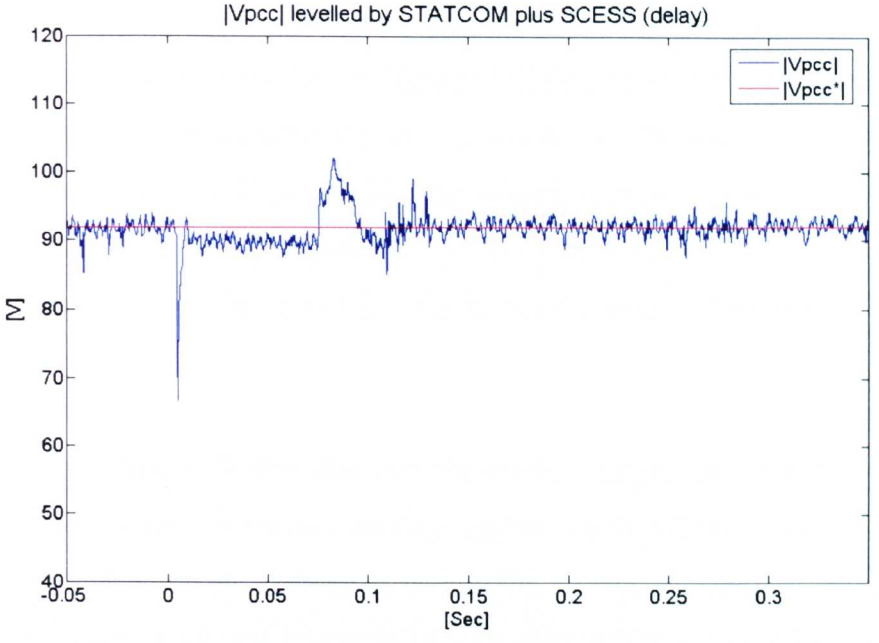

Figure 6-20 $|V_{pcc}|$ of the system with STATCOM plus SCESS when its operation is delayed by 70ms

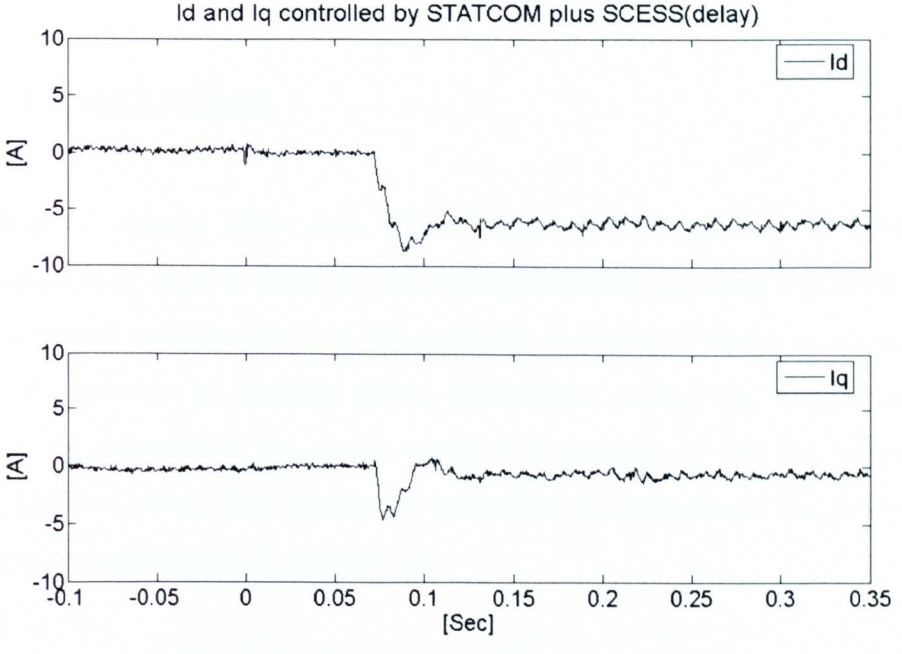

Figure 6-21 The controlled I_d and I_q for the system with STATCOM plus SCESS when its operation is delayed by 70ms.

Figure 6-19 shows that the STATCOM unit has not been enabled until time t = 70ms even through the main load has been switched on at time t = 0s. According to the explanation in section 6.2 during this period there is no compensation for the voltage drop at V_{pcc} caused by the load current, and this can clearly be seen in Figure 6-20. The supply current waveforms show the full load current is being supplied by ac side power system. Also, there is no support current, both the I_d and I_q current, can be seen in Figure 6-21 during this period.

At time t = 70ms both real and reactive power support are enabled and the STATCOM current increases rapidly up to approximately 7A. A small overshoot with some oscillations is seen in the voltage and current waveforms shown in Figure 6-19 and Figure 6-20. The magnitude of V_{pcc} settles at rated value (phase voltage of $92V_{peak}$) after a short period of time. The operation of the STATCOM and SCESS unit follow the same trend of amplitude of oscillation as described in section 6.4.

6.6 Conclusions

Experimental results show that STATCOMs can be applied for voltage compensation in order to keep the bus voltage constant by using instantaneous reactive power compensation. In this research, d-q control theory is applied to define the amount of reactive power undertaken during the compensation process. By controlling the q-axis component current in the d-q reference frame, reactive power flow is directly controlled to compensate the voltage at V_{pcc} as the results shown in section 6.2.

Results in section 6.3 verify the proposed control technique applied for this research. According to d-q control theory, the response of the proposed system is also validated by the tracking of the d-q reference components. The control technique allows the STATCOM unit to utilise stored energy in supercapacitor

modules during real power injection to the ac grid, and also allows it to store energy in the supercapacitors during real power absorption. This has been experimentally validated, as shown in Figure 6-13 and Figure 6-14. To improve STATCOM performance, the STATCOM and SCESS unit employ a feedforward control technique, resulting in a constant DC-link voltage during real power exchanging as shown in section 6.3.

Comparative results from the experiments for a system compensated by STATCOM and a STATCOM plus SCESS shown in section 6.4 confirm that the performance of STATCOM is noticeably enhanced by energy storage. There is an obvious difference in STATCOM current when comparing the results from the system supported by STATCOM alone and STATCOM plus SCESS. Even though the STATCOM alone can maintain V_{pcc} constant, the whole of load current is supplied by the ac power grid. In the system with STATCOM plus SCESS, the load is supplied by STATCOM unit in which the real power compensation is being realised as shown in Figure 6-16 and Figure 6-19.

The ability to inject both real and reactive power control into the ac power grid is validated. The results of real power injection, providing instant voltage support, also imply that the transient stability of the system is improved. It can be concluded that STATCOM plus SCESS can be applied as a power electronic based power flow controller, with the ability to provide real power support.

Chapter 7

Conclusions and future work

It is clear that reactive and active power compensators are important for ac power systems in order to secure stable conditions and to improve quality of the consumed power of the system. Compensators have been applied worldwide to maintain power quality and stability of ac power systems including shunt-connected compensators described in this project.

In many ac power systems, especially during transient stressed conditions the lack of real power support from the compensators may lead to the severe failure due to the stability concerns. The STATCOM enhanced with energy storage is one of the options that can provide the ability to support both the reactive and real power dynamically to the ac grid. This superior ability can give a significant improvement in the performance of the ac power systems. This project has investigated the use of STATCOM with energy storage. The supercapacitor was chosen for the energy storage. It is a newly developed

energy storage device with a characteristic suitable for short-period charge/discharge application.

At the beginning of the thesis, the benefits to an ac power system using the enhanced STATCOM with energy storage were described in chapter 2. It showed that by injecting real power support to the ac grid immediately after the main load was switched to the grid, the instability caused by the rate of change of frequency (ROCOF) was minimised. The instability of the system within distributed generation (DG) due to the rate of change of frequency was analysed, and the proposed idea to minimise the instability is explained. The simulation work showed that with the immediate real power support from the STATCOM the cause of the instability (ROCOF) was reduced.

In order to validate the idea experimentally, the experimental rig for this project was constructed as described in chapter 5. With the aim to keep the STATCOM's DC-link voltage constant during the interaction between the STATCOM and the ac power grid, the SCESS was built. It consists of a dc-to-dc converter and the supercapacitor modules. The dc-to-dc converter is the main component of the SCESS which is used to control the transfer of the energy between the STATCOM's DC-link and the supercapacitor modules depending on the events at the ac power grid. The operation of the SCESS is classified into two main modes, boost and buck actions. In the boost mode the stored energy in the supercapacitor modules is transferred to the STATCOM's DC-link capacitor resulting in the DC-link voltage being regulated constant at the desired value, while in the buck mode the energy is transferred to the supercapacitor modules.

The STATCOM and the SCESS are incorporated together by interfacing the SCESS to the STATCOM's DC-link capacitor. The operation of the combined system is controlled using the feed-forward technique as described in chapter 4.

The experimental results shown at the beginning of chapter 6 show that the reactive power in the ac power system using the standard STATCOM designed in chapter 3 is compensated dynamically with the amount regulated by the Vpcc controller. Later in chapter 6 the experimental results from the ac power system using the STATCOM plus SCESS confirm that the supercapacitor energy storage system gives the STATCOM the ability to inject and absorb real power from the ac power grid. The limited ability of the standard STATCOM is expanded with the use of the SCESS. The STATCOM plus SCESS can compensate both the additional real and reactive power dynamically. Therefore, by using the STATCOM plus SCESS, the support current to the ac grid can be controlled effectively in all four quadrants.

The work carried out over the course of this project can be summarised as in the following sections.

7.1 Power system stability improvement using the STATCOM with energy storage

The instability of the ac power system with distributed generation (DG) has been analysed. The dynamic behaviour of the rotating machine has been investigated focusing on the variation of the machine speed due to the imbalance between the electrical power output and the mechanical power input. The instability of the mentioned system is concerned with the rate of change of frequency (ROCOF) which is directly proportional to the speed of the rotating synchronous generator applied to the system. If the rate of change of frequency is beyond the acceptable range, the protecting system (which is originally designed to prevent the islanding or loss of main mode operation) will separate and stop the operation of the machine from the system. However the unnecessary tripping (mal-operation) of the protection system will occur

following transient events, resulting in a poor security and reliability of the whole system.

The idea to minimise the instability has been proposed by applying the instantaneous real power support produced by the STATCOM with energy storage to help the generator to handle the suddenly imbalanced conditions. The minimum amount of the stored energy (rating of the energy storage device) required to stabilise the system frequency has been derived. Furthermore the simulation of the application of the STATCOM with energy storage to minimise the instability is shown in chapter 2.

7.2 The standard STATCOM based on a small-signal modelling controller design

The instantaneous reactive power compensation using the STATCOM based on vector control strategy has been designed and built for this project. For the compensation, the STATCOM was operated with the quantity of the reactive power generated and optimised by the V_{pcc} controller. In the designing for the V_{pcc} controller, the relation of the change in the V_{pcc} and the change in the reactive power current ($\Delta V_{pcc}/\Delta Iq$) has been derived using small-signal modelling, and used in the closed-loop control design. The rapid compensation characteristic of the STATCOM has been confirmed by both the simulation and the experimental results.

7.3 The enhanced STATCOM with Supercapacitors

With the aim to enhance the performance of the STATCOM described in section 7.2, the supercapacitor energy storage system (SCESS) has been

designed and built interfacing to the STATCOM's DC-link capacitor. In the design for the two mode control of the SCESS (buck and boost modes), the small-signal model representing the change in the supercapacitor voltage related to the change in the reference for the supercapacitor current ($\Delta V_{sc}/\Delta I_{sc}^{*}$) has been derived and applied in the buck mode controller design, while the relation of the change in the DC-link voltage and the change in the reference for the supercapacitor current ($\Delta V_{dc}/\Delta I_{sc}^{*}$) has been derived and applied in the boost mode controller design.

The improved performance of the enhanced STATCOM, the STATCOM plus SCESS, has been confirmed both by the simulation and the experimental results. The STATCOM plus SCESS has a superior performance over the standard STATCOM, it can provide both real and reactive power to the ac grid immediately, while the standard STATCOM can provide only the reactive power. It can be summarised that the enhanced STATCOM can control the support current effectively in all four quadrants, which will be the benefit for the ac power system stability improvement.

7.4 Future work

The work carried out during the period of this project can be used as the basis for the future research work that probably focuses on the transient stability of the ac power system. However one of the limitations found when running the experimental tests is the practical control problem due to the dSPACE controller board. In the dSPACE the controllable PWM signals are generated using the dSPACE's built-in units. The three-phase PWM unit was used to generate the PWM for the STATCOM, while the single-phase PWM was used to control the SCESS. The operation of the single-phase was not synchronised with the three-phase PWM, although the interrupt signal that automatically produced by the three-phase PWM unit was used for the overall control. The suggestion for the future experimental tests is to use the DSP controller board

that can be programmed manually, coding the desired functions line by line. Therefore, the possible future work can be undertaken effectively based on this project as listed below.

1) The experimental validation with a single and multiple generators to demonstrate the improvement of the stability of the ac power system using the STATCOM plus SCESS. The knowledge of the rotating machine control, both the synchronous and induction machines, is necessary in order to investigate enhancing the system stability during transients.

2) The control of the enhanced STATCOM plus SCESS to improve the fault ride-through (FRT) capability of the generators. For the grid-connected generators, they are required to remain connected to the ac grid and able to supply adequate electrical power to the system loads after severe three-phase faults occur. In particular the research should focus on the application of the enhanced STATCOM to improve the fault ride through capability of the wind-turbine induction generators which is increasingly applied in the growing wind farm electrical power networks.

3) The control technique to operate the STATCOM in order to improve the system stability and power quality during the temporary ground faults – single line to ground and double line to ground faults. The temporary fault is the most frequent disturbance that may affect the system stability of the weak ac power system. The STATCOM with the ability to handle this kind of disturbances will not only improve the power quality but also the stability of the system.

7.5 Publications resulting from the project

The work carried out over the course of this project has resulted in the technical papers published as listed below.

[1] P. Srithorn, M. Sumner, Y. Liangzhong, and R. Parashar, *"Power System Stabilisation Using STATCOM with Supercapacitors,"* in IEEE Industry Applications Society Annual Meeting 2008 - IAS '08, 2008, pp. 1-8.

[2] P. Srithorn, M. Sumner, Y. Liangzhong, and R. Parashar, *"The control of a STATCOM with supercapacitor energy storage for improved power quality,"* in IET-CIRED2008 SmartGrids for Distribution, 2008, pp. 1-4.

[3] P. Srithorn, M. Sumner, Y. Liangzhong, and R. Parashar, *"A STATCOM with supercapacitors for enhanced power system stability,"* in IET Power Electronics, Machines and Drives-PEMD08, 2008, pp. 96-100.

[4] P. Srithorn, M. Aten, and R. Parashar, *"Series connection of supercapacitor modules for energy storage,"* in IET Power Electronics, Machines and Drives-PEMD06, 2006, pp. 354-360.

Appendix A

Simulink implementation for the simulation of a generator supplying a sudden load change with and without STATCOM-ES

A.1 Introduction

In order to support the main idea of this thesis, the simulation of an ac power system consisting of a synchronous generator, a transformer, and loads was carried out with and without the STATCOM with energy storage (STATCOM-ES). The additional energy storage device gives the STATCOM the ability to provide the real power instantaneously to the load demand. This ability minimises the variation of the speed of the synchronous generator and therefore the system frequency during the transient, in this case study, caused

by the sudden change of the main load connected to the V_{pcc} bus as described in chapter 2.

The details of the simulation using MATLAB Simulink/SimPowerSystems are presented in the followings sections.

A.2 The overall simulation models

The overall simulation model was implemented graphically as shown in Figure A-1 which consists of a synchronous generator with its associating speed governor and excitation control, a three-phase transformer connected between the different voltage levels of the load and the generator, a three-phase circuit breaker, a 2.5MW resistive load, and a STATCOM-ES connected at the V_{pcc} bus.

A light load of 0.1 MW is also included in the simulation as a representation of a local ancillary system connected at the generator terminals. The voltage and current at V_{pcc} terminals, STATCOM terminals, and load terminals are measured and monitored by 'PCC measurement', 'statcom measurement', 'load measurement' blocks respectively as indicated in Figure A-1.

More details of the synchronous generator including the frequency and voltage control are presented in section A.2.1. The STATCOM-ES model including its operation is described in section A.2.2. The parameters of the transformer, the circuit breaker, and the load models are listed in section A.2.3, A.2.4 and A.2.5 respectively.

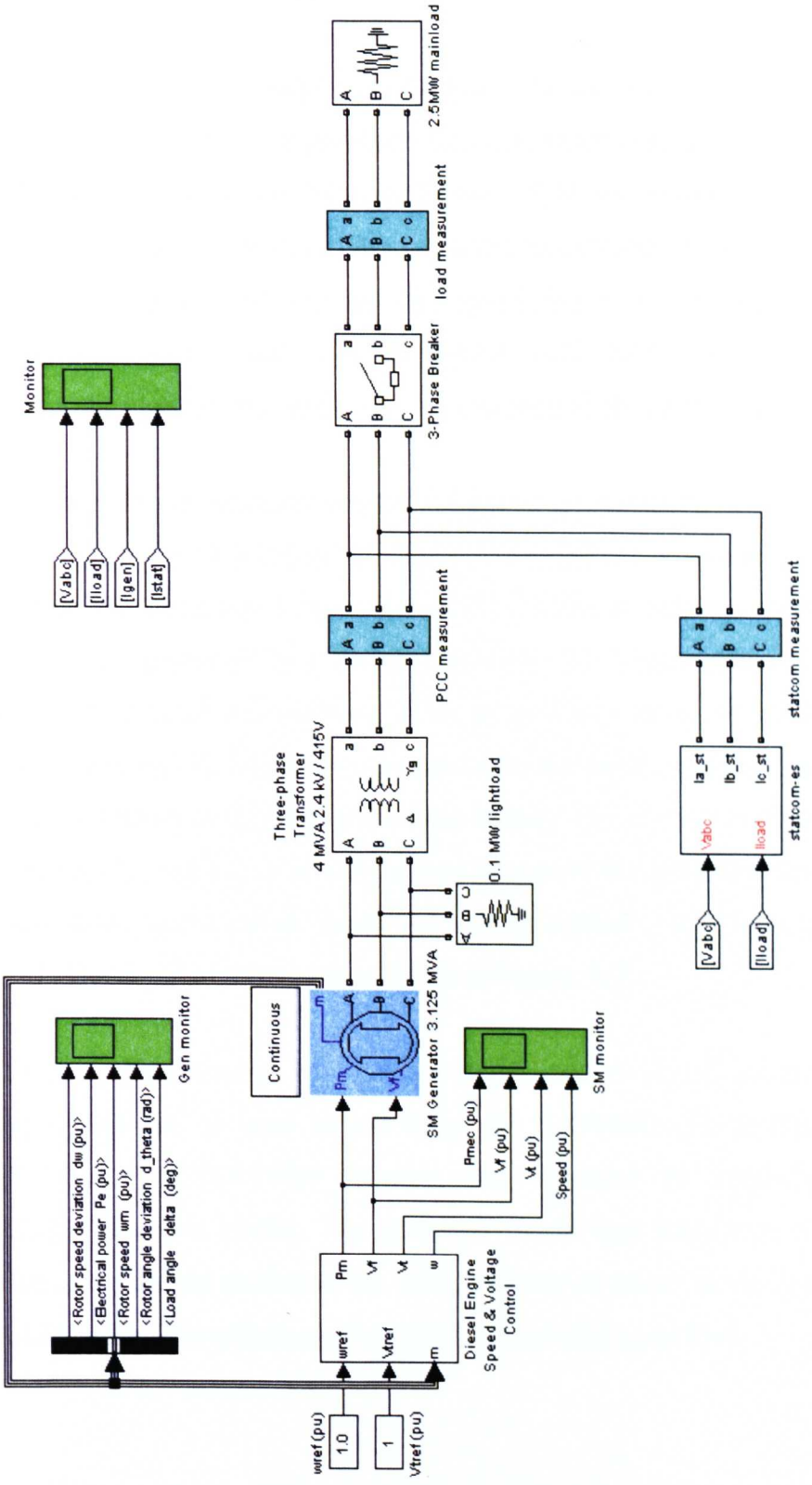

Figure A-1 The overall simulation model

A.2.1 Synchronous generator model

A synchronous generator model can be found in the machine library of SimPowerSystems BlockSet. In principle, this synchronous generator model is operated associating to the two input quantities - field excitation voltage (V_f) and mechanical input power (P_m). The generator model also gives the useful measured output signals 'm' such as rotor speed deviation, electrical power generated, rotor speed, rotor angle deviation, load angle etc., which is necessary for the closed-loop control of the operation of the generator.

The magnitude of the terminal output voltage is proportional to the field excitation voltage, and the ability to supply the electrical power to loads is dependant on the mechanical input power. Therefore in order to keep the operation of the generator in a stable condition, its output quantities are needed to be monitored and fed back to the control unit using the measured signals 'm', as shown in Figure A-1, to modulate the input values of both V_f and P_m corresponding to the electrical power output. The control of these two input quantities, V_f and P_m, is actually aimed to control the generator terminal voltage and speed, and is called "speed and voltage control" block indicated in Figure A-1. The detail of this block is shown in Figure A-2.

In Figure A-2, the reference speed and voltage are set at 1.0 pu and the measured signals 'm' is used as the input for 'GOVERNOR & DIESEL ENGINE' and 'EXCITATION' blocks. The standard PI controller is employed in these two blocks. The generator model and these two control block parameters are set similar to the default values as found in the example model found in SimPowerSystems/Demos/Machines and Load Flow.

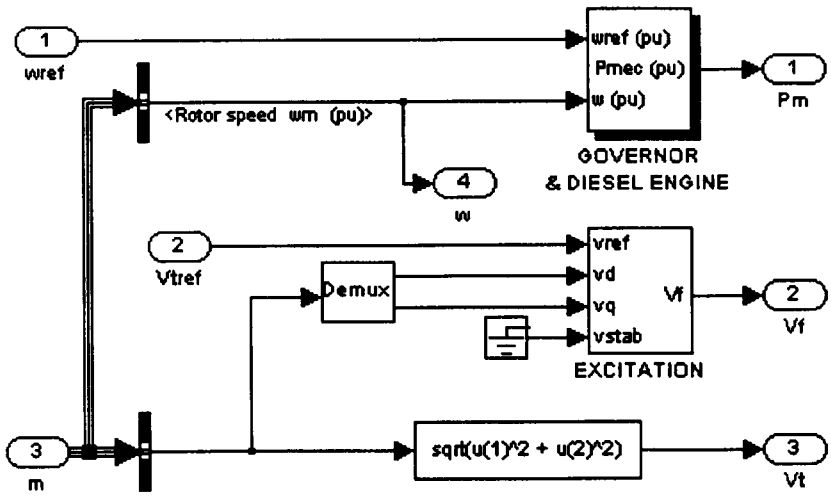

Figure A-2 Detail of the speed and voltage control block in Figure A-1

A.2.2 STATCOM-ES model

The detail of the STATCOM-ES model block used in this simulation is illustrated in Figure A-3 where the controlled current sources named 'CCS1', 'CCS2' and 'CCS3' are the main component models for phase 'a', 'b', and 'c' current generator. To prevent the simulation error caused by the series connection of the controlled current source and the transformer (which also acts as a current source) during the initial period before the main load is switched on, the 100kΩ resistor models are used in parallel-connected to the controlled current sources, and the 1mH inductor is connected in series with the controlled current sources.

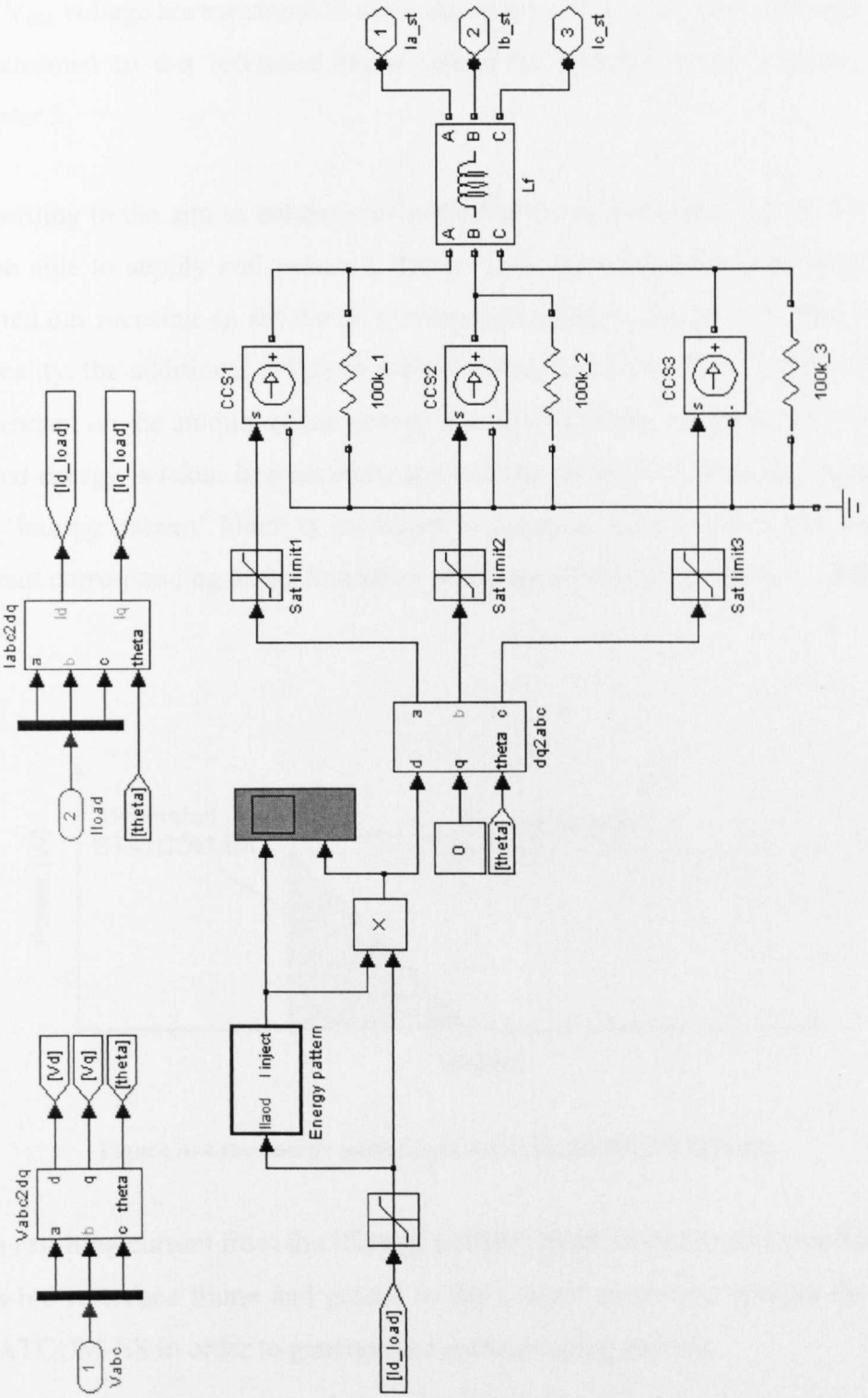

Figure A-3 Detail of the STATCOM-ES block in Figure A-1

The current produced by the STATCOM-ES (by the controlled current source) is dependant on the value from 'Energy pattern' block. The main load current and V_{pcc} voltage are measured in a-b-c stationary reference frame, and then are transformed to d-q reference frame using the transformation described in chapter 3.

According to the aim to enhance the performance of the standard STATCOM to be able to supply real power to the ac grid, the simulation was therefore carried out focusing on the d-axis current generation as shown in Figure A-3. In reality, the additional ability to supply real power of the STATCOM-ES is dependant on the amount of the energy stored. Therefore, the limitation of the stored energy is taken into account, and to simulate the use of energy storage the 'Energy pattern' block is modelled to produce the pattern of the d-axis current corresponding to the limitation of the stored energy as shown in Figure A-4.

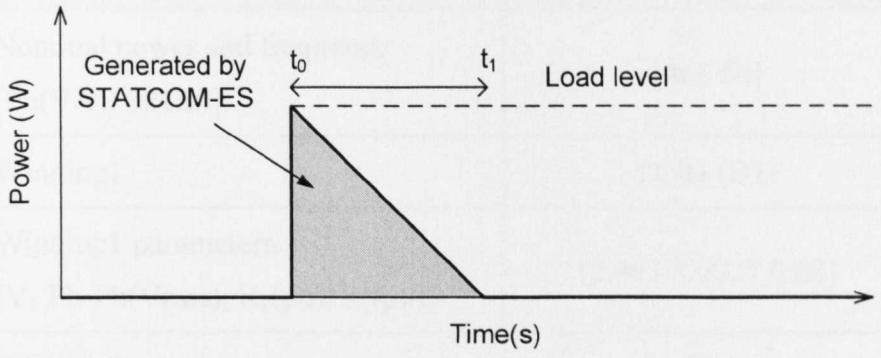

Figure A-4 the energy pattern produced by the STATCOM-ES

The resulting current from the 'Energy pattern' block is then transformed back to a-b-c reference frame and passed to the controlled current sources for the STATCOM-ES in order to generate the corresponding current.

According to the energy pattern shown in Figure A-4, at time t_0 the STATCOM-ES will supply the full load rating real power instantaneously to

the ac grid following the sudden change of the load current. This real power support is then reduced steadily to zero at time t_1. The slope of this real power support pattern is related to the quantity of the stored energy – real power support period between t_0 and t_1 can be longer if the stored energy is sufficient related to the load demand. For an ac power system, in order to minimise the system frequency variation, the minimum amount of the energy required for the STATCOM-ES is described in chapter 4.

A.2.3 Three-phase transformer model

The MatLab/Simulink three-phase two winding transformer model is set with parameters listed in Table A-1.

Table A-1 Three-phase transformer model parameters

Parameter	Value
Nominal power and frequency [Pn(VA), fn(Hz)]	[4e6 50]
Winding1	Delta (D1)
Winding1 parameters [V_1 Ph-Ph(Vrms), R_1(pu), L_1(pu)]	[2.4e3 0.0027 0.08]
Winding2	Yg
Winding2 parameters [V_2 Ph-Ph(Vrms), R_2(pu), L_2(pu)]	[415 0.0027 0.08]
Magnetization resistance R_m(pu)	500
Magnetization reactance L_m(pu)	500
Measurements	None

A.2.4 Three-phase circuit breaker model

The MatLab/Simulink three-phase two winding transformer model is set with parameters listed in Table A-2.

Table A-2 Three-phase circuit breaker model parameters

Parameter	Value
Initial status of breakers : (Switching of all phases)	Open
Transition times (s)	[1]
Breaker resistance R_{on}(ohms)	0.001
Snubbers resistance R_p(ohms)	1e5
Snubbers capacitance C_p(Farad)	inf
Measurements	None

A.2.5 Load model

The MatLab/Simulink three-phase load is set with the parameters list in Table A-3.

Table A-3 Three-phase load model parameters

Parameter	Value
Configuration	Y
Nominal phase-to-phase voltage Vn(Vrms)	415
Active power P(W)	3e6

Inductive reactance power Q_L (positive var)	0
Capacitive reactance power Q_C (negative var)	0
Measurements	None

Appendix B

Small-signal modelling for the STATCOM's V_{pcc} control design

B.1 Introduction

To regulate the V_{pcc} voltage, the STATCOM has to generate the optimum amount of the reactive power (Q) to the ac power grid. The amount of the reactive power is set proportional to the q-axis current reference (I_q*) by the outer control loop – the V_{pcc} controller. In order to design the proper V_{pcc} controller, according to the ac power system shown in Figure B-1, a small-signal model of the relevant V_{pcc} plant is needed. The V_{pcc} controller designed using the small-signal model of the V_{pcc} plant derived here in this section was also used in the simulation work and the experimental validation that also implemented based on the same ac power system shown in Figure B-1.

B.2 The proposed ac power system

In the case study scenario shown in Figure B-1, the STATCOM is connected to the ac grid at the PCC in order to keep V_{pcc} constant whether the main load is switched to the grid or not. In the figure, as the STATCOM is operated based on a high frequency switching technique, the system inductance (L_s and the leakage inductance of the transformer) and the coupling inductance L_c form a voltage divider that resulting in a high frequency switching noise appears on the voltage waveform of V_{pcc}. A constant light load is added in the circuit to minimise this effect, and to represent the ancillary system in the reality.

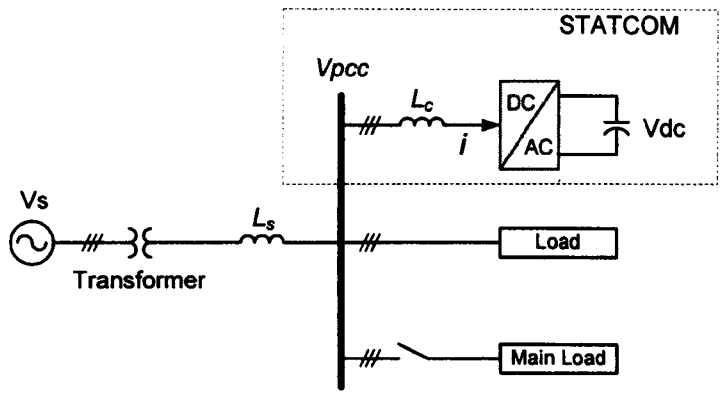

Figure B-1 The power circuit of the ac power system using a STATCOM

B.3 Small-signal modelling of the proposed system

According to its principle operation, the STATCOM can be modelled as a current source in the equivalent circuit as shown in Figure B-2, where the light load can be neglected due to it is drawing a constant current over the considered period.

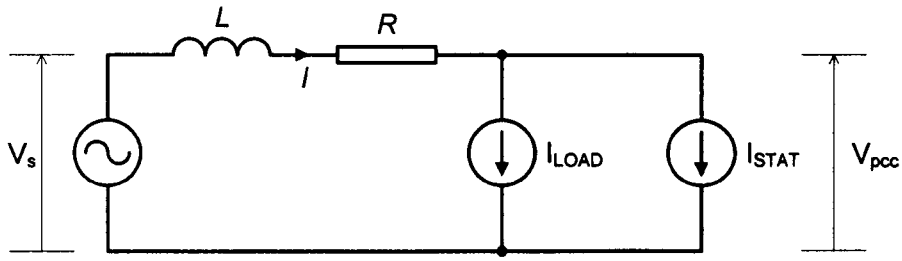

Figure B-2 The equivalent circuit of the system show in figure B-1

Where

V_s is the ac power supply, V.

V_{pcc} is the voltage at point of common coupling, V.

I_{load} is the main load current, A.

I_{STAT} is the STATCOM current, A.

L is the equivalent inductance between the ac power supply and the point of common coupling, H.

R is the equivalent resistance between the ac power supply and the point of common coupling, H.

From the equivalent circuit shown in Figure B-2, the relationship of the voltage and current can be summarised as shown in Equation (B-1).

$$\begin{bmatrix} V_{s\_a} - V_{pcc\_a} \\ V_{s\_b} - V_{pcc\_b} \\ V_{s\_b} - V_{pcc\_c} \end{bmatrix} = L\frac{di}{dt}\begin{bmatrix} i_a \\ i_b \\ i_c \end{bmatrix} + R\begin{bmatrix} i_a \\ i_b \\ i_c \end{bmatrix} \quad \text{(B-1)}$$

Where

V_{s_a} is the phase 'a' voltage of the three-phase ac power supply.

V_{s_b} is the phase 'b' voltage of the three-phase ac power supply.

V_{s_c} is the phase 'b' voltage of the three-phase ac power supply.

I_a is the phase 'a' current flowing from the three-phase ac power supply.

I_b is the phase 'b' current flowing from the three-phase ac power supply.

I_c is the phase 'c' current flowing from the three-phase ac power supply.

Applying the a-b-c to d-q transformation to Equation (B-1) gives the rotating reference frame voltage Equations (B-2) and (B-3).

$$V_{s\_d} - V_{pcc\_d} = L\frac{dI_d}{dt} + RI_d - \omega_e LI_q \quad \text{(B-2)}$$

$$V_{s\_q} - V_{pcc\_q} = L\frac{dI_q}{dt} + RI_q + \omega_e LI_d \quad \text{(B-3)}$$

Where

ω_e is the angular frequency of the rotating reference frame.

V_{s_d} is the d-axis voltage of the three-phase ac power supply.

V_{s_q} is the q-axis voltage of the three-phase ac power supply.

V_{pcc_d} is the d-axis voltage at V_{pcc}.

V_{pcc_q} is the q-axis voltage at V_{pcc}.

In the rotating reference frame where the voltage equation is aligned on the V_{pcc} voltage vector, then the q-axis voltage at the point of common coupling becomes zero, $V_{pcc\_q} \Rightarrow 0$.

In both Equation (B-2) and (B-3), the current in the rotating reference frame I_d and I_q represent the sum of the STATCOM and load current as given in Equation (B-4) and (B-5).

$$I_d = I_{d\_stat} + I_{d\_load} \quad \text{(B-4)}$$

$$I_q = I_{q\_stat} + I_{q\_load} \tag{B-5}$$

Due to the limited energy in the DC-link capacitor, the STATCOM cannot supply the d-axis current component, then $I_{d\_stat} \Rightarrow 0$.

Substituting Equation (B-4) and (B-5) in Equation (B-2) and (B-3) results in

$$V_{s\_d} - V_{pcc\_d} = L\frac{d(I_{d\_load})}{dt} + RI_{d\_load} - \omega_e L I_{q\_stat} \tag{B-6}$$

$$V_{s\_q} = L\frac{d(I_{q\_stat})}{dt} + RI_{q\_stat} + \omega_e L I_{d\_load} \tag{B-7}$$

Perturbing and applying Laplace transformation to Equation (B-6) and (B-7).

$$\Delta V_{s\_d} - \Delta V_{pcc\_d} = (sL + R)\Delta I_{d\_load} - \omega_e L(\Delta I_{q\_stat} + \Delta I_{q\_load}) \tag{B-8}$$

$$\Delta V_{s\_q} = (sL + R)(\Delta I_{q\_stat} + \Delta I_{q\_load}) + \omega_e L \Delta I_{d\_load} \tag{B-9}$$

Assuming the three-phase power supply voltage remains constant at all time, then $\Delta V_{s\_d} \Rightarrow 0$ and $\Delta V_{s\_q} \Rightarrow 0$. The q-axis component of the load current will remain constant compared to the change in the d-axis component due to the load being the active power component, thus $\Delta I_{q\_load} \Rightarrow 0$. Equation (B-8) and (B-9) can be re-written again as in Equation (B-10) and (B-12).

$$-\Delta V_{pcc\_d} = (sL + R)\Delta I_{d\_load} - \omega_e L \Delta I_{q\_stat} \tag{B-10}$$

$$0 = (sL + R)\Delta I_{q\_stat} + \omega_e L \Delta I_{d\_load} \tag{B-11}$$

From Equation (B-11),

$$\Delta I_{d\_load} = -\frac{(sL+R)}{\omega_e L}\Delta I_{q\_stat} \tag{B-12}$$

Substituting Equation (B-12) in Equation (B-10) gives the small-signal model representing the change in V_{pcc} due to the change in the reactive compensation current produced by the STATCOM as shown in Equation (B-13) where ΔV_{pcc_d} dominates the ΔV_{pcc} due to the $V_{pcc\_q} \Rightarrow 0$ as mentioned previously.

$$\frac{\Delta V_{pcc}}{\Delta I_{q\_stat}} = \frac{(sL+R)^2}{\omega_e L} + \omega_e L \tag{B-13}$$

Due to the value of the impedance connected between the three-phase ac power supply and the V_{pcc} bus is very small, thus the term $(sL+R)^2/\omega_e L$ in Equation (B-13) is not significant and can be neglected.

Appendix C

Small-signal models for the SCESS controller design

C.1 Introduction

Referring to the control concept of the SuperCapacitor Energy Storage System (SCESS) described in chapter 4, the controllers for both boost and buck mode operation are designed using the plants that are derived based on small-signal modelling of the system circuit shown in Figure C-1. The proposed small-signal equations for boost mode ($\Delta V_{dc}/\Delta I_{ref}$) and buck mode ($\Delta V_{sc}/\Delta I_{ref}$) are derived in section C.2 and C.3 respectively.

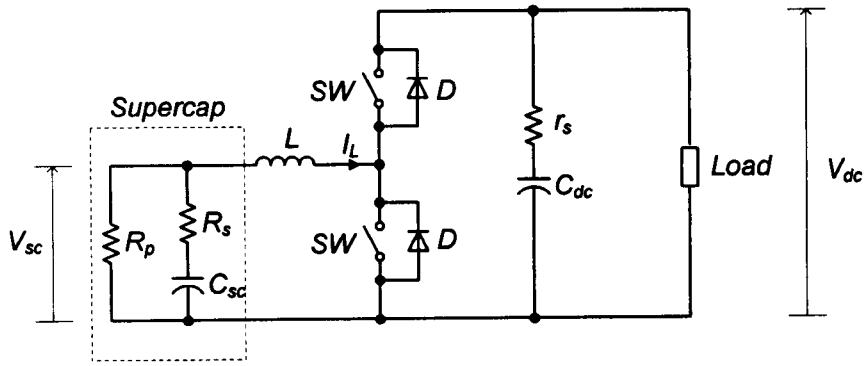

Figure C-1 Power circuit of the SCESS

Where

V_{sc}	is the supercapacitor voltage, V.
V_{dc}	is the DC-link voltage, V.
C_{sc}	is the supercapacitor modules, F.
C_{dc}	is the DC-link capacitor, F.
R_s	is the series resistance of supercapacitor module, Ω.
R_p	is the parallel resistance of supercapacitor module, Ω.
r_s	is the series resistance of DC-link capacitor, Ω.
L	is the inductor for buck-boost converter, H.
SW	is the switching device (or IGBT for this project).
D	is the anti-parallel diode.

The small-signal analysis in this appendix is based on the following assumptions.

1) The inductor L has no resistive component. Therefore rate of change in inductor current ($\Delta I/\Delta T$) is proportional to V_L/L.

2) Over one sampling period, the change in the supercapacitor terminal voltage (V_{sc}), the DC-link voltage (V_{dc}), the reference current (I_{ref}), load current (I_{dc}), and the current representing loss in R_p (I_{Rp}) is relatively slow compared to the change in the inductor current shown in Figure C-2.

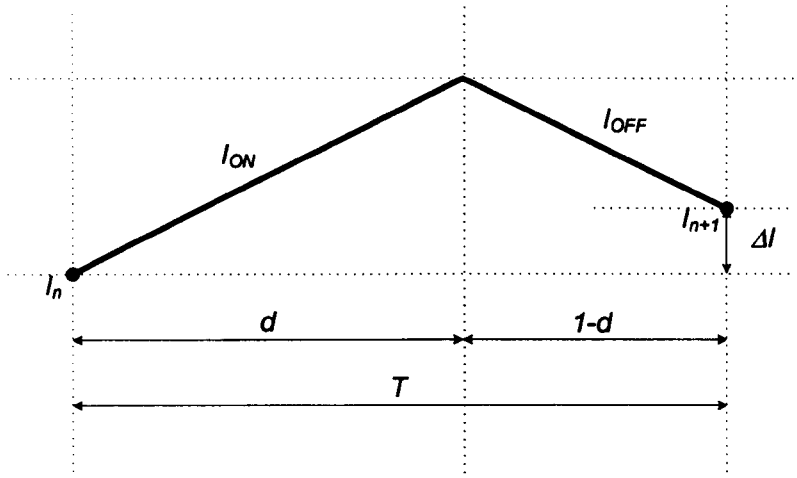

Figure C-2 Change in inductor current over one sampling period

Where I_n is the inductor current, I_{ON} and I_{OFF} are the inductor current when the associated switch is turned on and off during one sampling period (T) respectively. The duty cycle of the switching pattern is indicated by'd'.

In steady state, the inductor current reaches its peak at the reference current and the change in the current becomes zero ($\Delta I \Rightarrow 0$ and $I_{n+1} = I_n$).

C.2 Boost mode small-signal equations

In boost mode, the supercapacitor module will supply energy to the DC-link, therefore in this analysis a dc power source is used as the supercapacitor model. The inductor current (I_L) is the current supplied from the supercapacitor modules (I_{sc}). The simplified circuit diagram of the SCESS operating in boost mode is shown in Figure C-3.

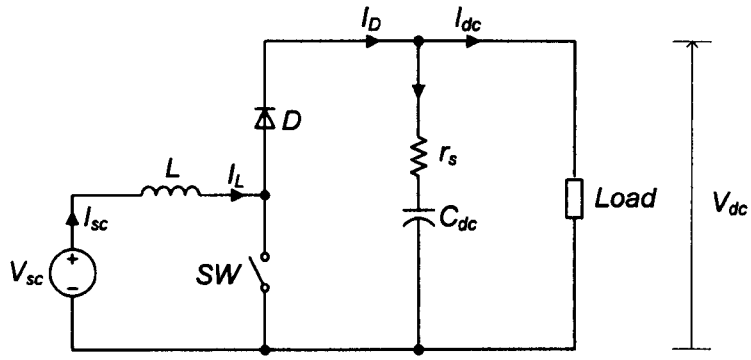

Figure C-3 Boost mode circuit diagram

The system equations of boost mode operation illustrated in Figure C-3 are summarised below.

$$V_{dc} = \frac{V_{sc}}{1-d} \tag{C-1}$$

$$I_{dc} = (1-d)I_{sc} \tag{C-2}$$

$$V_{dc} = \left(I_{D_{av}} - I_{dc}\right)\left(r_s + \frac{1}{sC_{dc}}\right) \tag{C-3}$$

$$I_{D_{av}} = (1-d)\frac{I_{ref}+I_n}{2} \tag{C-4}$$

I_{Dav} is the average diode current. Perturbing and linearising Equation (C-3) and (C-4) gives

$$\Delta V_{dc} = \left(\Delta I_{D_{av}} - \Delta I_{dc}\right)\left(r_s + \frac{1}{sC_{dc}}\right) \tag{C-5}$$

$$\Delta I_{D_{av}} = \frac{1-d}{2}\left(\Delta I_{ref} + \Delta I_n\right) - \frac{I_{dc}}{1-d}\Delta d \tag{C-6}$$

The change in inductor current over one sampling period (ΔI_n) can be derived from the following equations.

When the SW is on:-

$$I_{ref} - I_n = \frac{dTV_{sc}}{L} \tag{C-7}$$

When the SW is off:-

$$I_{ref} - I_{n+1} = \frac{(1-d)T(V_{dc}-V_{sc})}{L} \tag{C-8}$$

(C-7) - (C-8) resulting in Equation (C-9)

$$I_{n+1} - I_n = \frac{T}{L}\{V_{sc} + (d-1)V_{dc}\} \tag{C-9}$$

Equation (C-9) is perturbed and linearised

$$\Delta I_{n+1} - \Delta I_n = \frac{T}{L}\{\Delta V_{sc} + (d-1)\Delta V_{dc} + \Delta d V_{dc}\} \tag{C-10}$$

, and

$$\frac{\Delta I_{n+1}-\Delta I_n}{T} = \frac{d\Delta I_n}{dt}$$

Therefore,

$$\Delta I_n = \frac{1}{sL}\{\Delta V_{sc} + (d-1)\Delta V_{dc} + \Delta d V_{dc}\} \tag{C-11}$$

Δd can be determined by perturbing Equation (C-7) as given in Equation (C-12), and the resulting Δd is in Equation (C-13).

$$\Delta I_{ref} - \Delta I_n = \frac{T}{L}\{\Delta d V_{sc} + d\Delta V_{sc}\} \tag{C-12}$$

$$\Delta d = \frac{L}{TV_{sc}}\left\{\left(\Delta I_{ref} - \Delta I_n\right) - \frac{dT}{L}\Delta V_{sc}\right\} \tag{C-13}$$

To determine the proposed small-signal model ($\Delta V_{dc}/\Delta I_{ref}$), small-signal equations mentioned above are used in implementation of a block diagram representing the relation of the above equation as shown in Figure C-4.

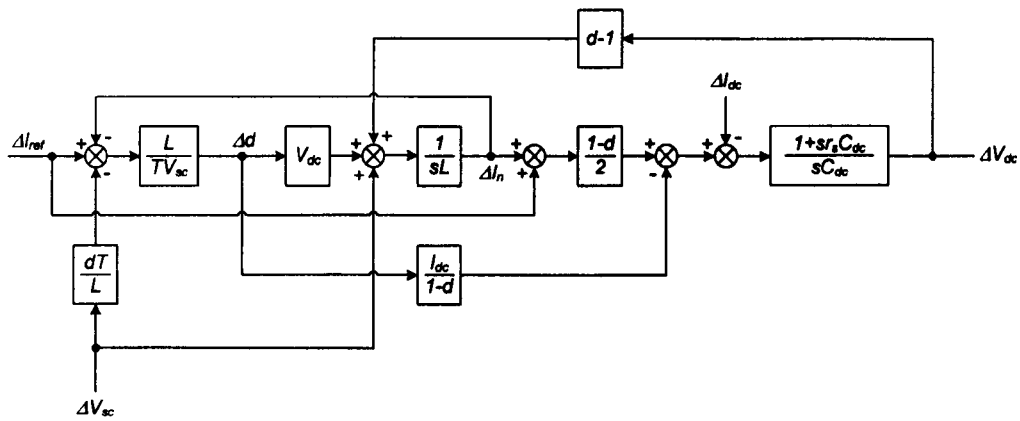

Figure C-4 Small-signal block diagram of the SCESS operating in boost mode

The proposed transfer function representing the change in DC-link voltage due to the change in reference current can be obtained from Figure C-4 using signal flow graph and Mason's rule. However, it is convenient to first obtain the relationships of the sub-transfer function from ΔI_{ref}, ΔV_{dc}, and ΔV_{sc} to ΔI_{Dav} before finishing the block diagram with the analysis of the load condition.

The forward path from ΔI_{ref} to ΔI_{Dav} gives the product of the path gain and path determinant P_{1_boost}.

$$P_{1\_boost} = \frac{1}{2sT}\left\{1 + \frac{(1-d)^3 TV_{dc} - 2LI_{dc}}{(1-d)^2 V_{dc}}\right\}$$

The forward path from ΔV_{dc} to ΔI_{Dav} gives the product of the path gain and path determinant P_{2_boost}.

$$P_{2\_boost} = -\frac{(1-d)^2}{2sL}$$

And the product of the path gain and determinant of the forward path from ΔV_{sc} to ΔI_{Dav} is P_{3_boost}.

$$P_{3\_boost} = \frac{1}{2sL}\left\{1 + \frac{2LI_{dc}(sdT+1)}{(1-d)^2 V_{dc}}\right\}$$

Thus, the simplified small-signal diagram of the boost mode SCESS with the effect of load added in for analysing is shown in Figure C-5, where

$$DClink = \frac{1 + sr_s C_{dc}}{sC_{dc}}$$

and Δ_{sub} is the sub-system determinant for P_{1_boost}, P_{2_boost}, and P_{3_boost}.

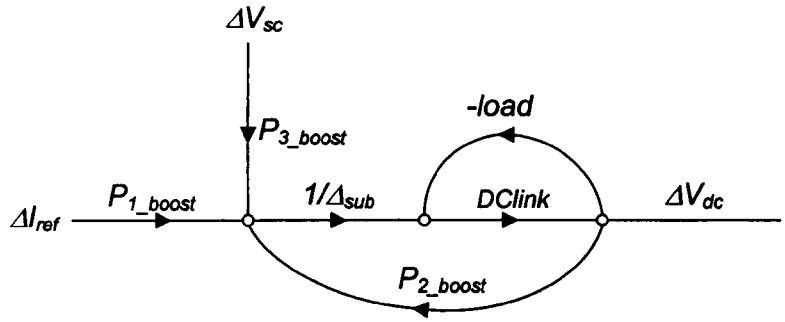

Figure C-5 the simplified small-signal diagram of the boost mode SCESS

The overall transfer function obtained from the simplified diagram in Figure C-5 is given in Equation (C-14).

$$\frac{\Delta V_{dc}}{\Delta I_{ref}} = \frac{k_1 k_2 (s + 1/k_2)(s + k_3)}{k_4 s^2 + k_5 s + k_6} \tag{C-14}$$

Where

$$k_1 = \frac{r_s C_{dc}(1-d)}{2}$$

$$k_2 = \frac{T(1-d)^3 V_{dc} - 2LI_{dc}}{(1-d)^3 V_{dc}}$$

$$k_3 = \frac{1}{r_s C_{dc}}$$

$$k_4 = C_{dc} T(1-d)(1 + r_s load)$$

$$k_5 = \frac{C_{dc}}{2L}(2L + r_s T(1-d)^3) + load(r_s C_{dc} + T(1-d))$$

$$k_6 = \frac{T(1-d)^3}{2L} + load$$

For this project the SCESS will be interfaced to the STATCOM, therefore load of the SCESS operating in boost mode can be modelled as a constant power load with the perturbed current shown in Equation (C-14).

$$I_{dc} = \frac{P_{dc}}{V_{dc}}$$

$$\Delta I_{dc} = -\frac{I_{dc}}{V_{dc}} \Delta V_{dc} \tag{C-15}$$

Therefore, load is ($-I_{dc}/V_{dc}$) and substituting for the load into the small-signal Equation (C-14), where the constants $k_1 - k_6$ become

$$k_1 = \frac{r_s C_{dc}(1-d)V_{dc}}{2}$$

$$k_2 = \frac{T(1-d)^3 V_{dc} - 2LI_{dc}}{(1-d)^3 V_{dc}}$$

$$k_3 = \frac{1}{r_s C_{dc}}$$

$$k_4 = C_{dc}T(1-d)(V_{dc} - r_s I_{dc})$$

$$k_5 = \frac{C_{dc}V_{dc}}{2L}(2L + r_s T(1-d)^3) - I_{dc}(r_s C_{dc} + T(1-d))$$

$$k_6 = \frac{T(1-d)^3 V_{dc}}{2L} - I_{dc}$$

C.3 Buck mode small-signal equations

The STATCOM's DC-link will supply energy to the SCESS in order to charge up the supercapacitor modules. The DC-link is therefore modelled as a dc source (V_{dc}) as shown in Figure C-6, where the supercapacitor current is the same as the inductor current ($I_{sc}=I_L$).

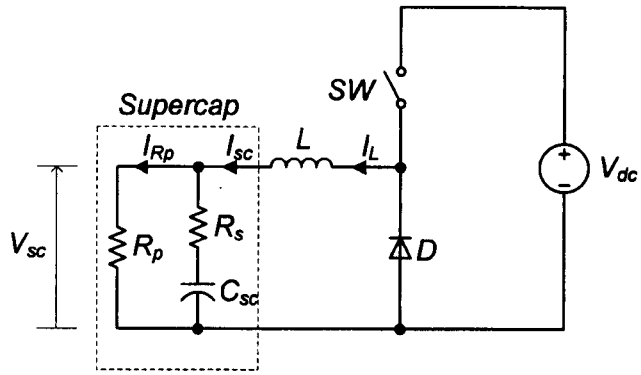

Figure C-6 Buck mode circuit diagram

The system equations of buck mode operation illustrated in Figure C-6 are listed as the following equations.

$$V_{sc} = dV_{dc} \tag{C-16}$$

$$I_{sc} = \frac{I_{dc}}{d} \tag{C-17}$$

$$V_{sc} = \left(I_{sc} - I_{Rp}\right)\left(R_s + \frac{1}{sC_{sc}}\right) \tag{C-18}$$

$$I_{sc} = \frac{I_{ref}+I_n}{2} \tag{C-19}$$

Equation (C-18) and (C-19) are perturbed and linearised as given.

$$\Delta V_{sc} = \left(\Delta I_{sc} - \Delta I_{Rp}\right)\left(R_s + \frac{1}{sC_{sc}}\right) \tag{C-20}$$

$$\Delta I_{sc} = \frac{\Delta I_{ref}+\Delta I_n}{2} \tag{C-21}$$

For the above equations, ΔI_n can be derived when the SW is on and off as the followings.

When the SW is on:-

$$I_{ref} - I_n = \frac{dT(V_{dc}-V_{sc})}{L} \quad \text{(C-22)}$$

When the SW is off:-

$$I_{ref} - I_{n+1} = \frac{(1-d)T(V_{sc})}{L} \quad \text{(C-23)}$$

(C-22) - (C-23) resulting in Equation (C-24)

$$I_{n+1} - I_n = \frac{T}{L}\{dV_{dc} - V_{sc}\} \quad \text{(C-24)}$$

Equation (C-24) is perturbed and linearised

$$\Delta I_{n+1} - \Delta I_n = \frac{T}{L}\{\Delta d V_{dc} + d\Delta V_{dc} - \Delta V_{sc}\} \quad \text{(C-25)}$$

, and

$$\frac{\Delta I_{n+1}-\Delta I_n}{T} = \frac{d\Delta I_n}{dt}$$

Therefore,

$$\Delta I_n = \frac{1}{sL}\{\Delta d V_{dc} + d\Delta V_{dc} - \Delta V_{sc}\} \quad \text{(C-26)}$$

Δd is needed for Equation (C-26) and can be determined from Equation (C-22).

$$\Delta I_{ref} - \Delta I_n = \frac{T}{L}\{\Delta d(V_{dc} - V_{sc}) + d(\Delta V_{dc} - \Delta V_{sc})\} \quad \text{(C-27)}$$

$$\Delta d = \frac{L}{T(V_{dc}-V_{sc})}\left\{(\Delta I_{ref} - \Delta I_n) - \frac{dT}{L}(\Delta V_{dc} - \Delta V_{sc})\right\} \quad \text{(C-28)}$$

All the perturbed and linearised equations above are used to implement the buck small-signal block diagram as illustrated in Figure C-7. For clarity, the transfer functions from ΔI_{ref} ,ΔV_{sc}, and ΔV_{dc} to ΔI_{sc} are obtained before finishing with parallel resistance of the supercapacitor to the block diagram.

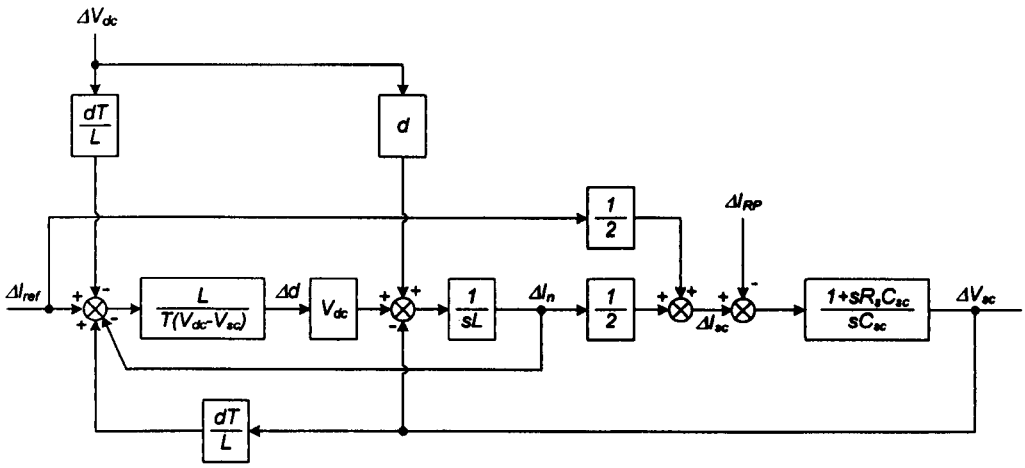

Figure C-7 The small-signal block diagram of the SCESS operating in buck mode

The forward path from ΔI_{ref} to ΔI_{sc} gives the product of the path gain and path determinant P_{1_buck}.

$$P_{1\_buck} = \frac{1}{2sT(1-d)}\{2 + sT(1-d)\}$$

The forward path from ΔV_{sc} to ΔI_{sc} gives the product of the path gain and path determinant P_{2_buck}.

$$P_{2\_buck} = \frac{1}{2sL}\left(\frac{2d-1}{1-d}\right)$$

And the product of the path gain and determinant of the forward path from ΔV_{dc} to ΔI_{sc} is P_{3_buck}.

$$P_{3\_buck} = -\frac{d^2}{2sL(1-d)}$$

The parallel resistance of the supercapacitor is added to the simplified small-signal diagram of the buck mode SCESS as shown in Figure C-8, where

$$SuperCap = \frac{1+sR_sC_{sc}}{sC_{sc}}$$

and Δ_{sub} is the sub-system determinant for P_{1_buck}, P_{2_buck}, and P_{3_buck}.

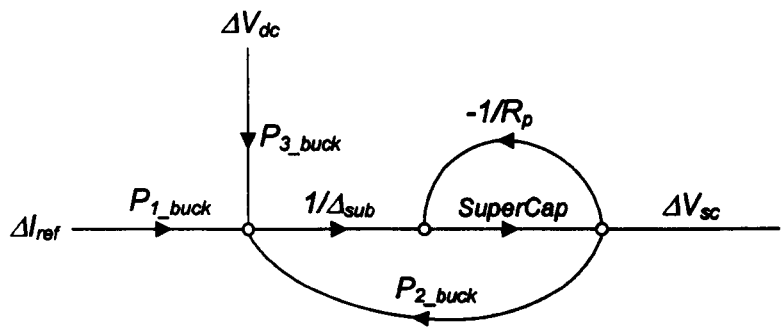

Figure C-8 The simplified small-signal diagram of the SCESS operating in buck mode

The overall transfer function obtained from the simplified diagram in Figure C-8 is given in Equation (C-29).

$$\frac{\Delta V_{sc}}{\Delta I_{ref}} = \frac{c_1 c_2 (s + 1/c_2)(s + c_3)}{c_4 s^2 + c_5 s + c_6} \tag{C-29}$$

Where

$$c_1 = 2R_s R_p L C_{sc}$$

$$c_2 = \frac{T(1-d)}{2}$$

$$c_3 = \frac{1}{R_s C_{sc}}$$

$$c_4 = 2LC_{sc}T(1-d)(R_p + R_s)$$

$$c_5 = 2LT(1-d) + R_p L C_{sc} - R_s R_p C_{sc} T(2d-1)$$

$$c_6 = 2L - R_p T(2d-1)$$

Appendix D

State equations for the SCESS control

D.1 Introduction

A power circuit of the SCESS shown in Figure D-1 indicates that the control of the inductor current (I_L) dominating the control of the energy transferred between the two sides of the SCESS (V_{dclink} and V_{sc}). The inductor current is directly related to the gating of the two SWs. Therefore, to control the inductor current is to control the period that SW is on by means of Duty Cycle Modulation (DCM) of the SW.

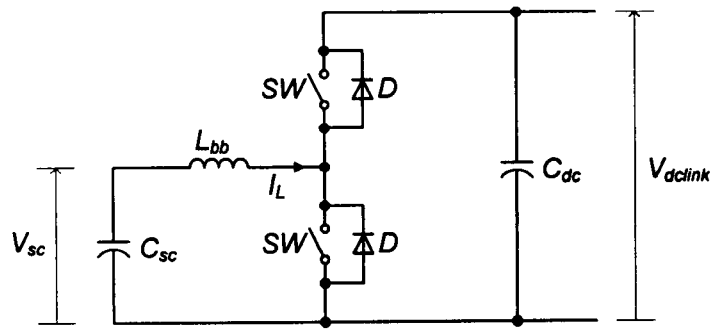

Figure D-1 Power circuit of the SCESS

Where

V_{sc} is the supercapacitor voltage.

V_{dclink} is the DC-link voltage.

C_{sc} is the supercapacitor modules.

C_{dc} is the DC-link capacitor.

L_{bb} is the inductor for buck-boost converter.

SW is the switching device.

D is the anti-parallel diode.

In this project, the IGBT modules with the built-in anti parallel diode inside are used. The DC-link capacitor is directly connected to the STATCOM dc side.

In DCM switching strategy, the value of the duty cycle provided for the dSPACE controller board and also for the simulation is based on the state equations derived in following sections.

D.2 State equation for boost mode operation

In boost mode, the supercapacitor modules in Figure D-1 will act as the dc source supplying energy to the DC-link capacitor when the SCESS is operated in boost mode. The upper SW is turned off all the time, while the lower SW is

gated corresponding to the controlled DCM switching signal as shown in Figure D-2.

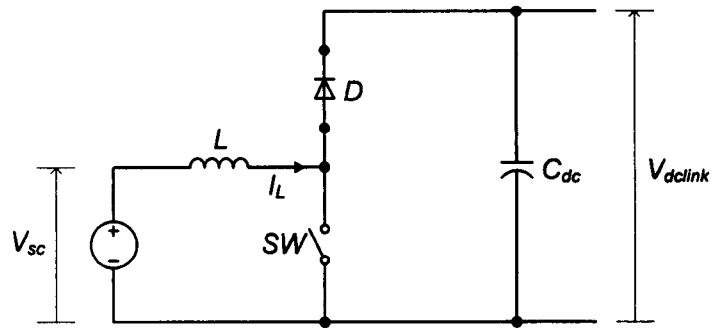

Figure D-2 The SCESS boost mode power circuit.

During one sampling period, according to the DCM switching strategy, when the SW is turned on, the supercapacitor energy is transferred to stored magnetic at the inductor; and then later transferred to the DC-link capacitor through the diode when the SW is turned off. Therefore the resulting inductor current waveform is indicated in Figure D-3.

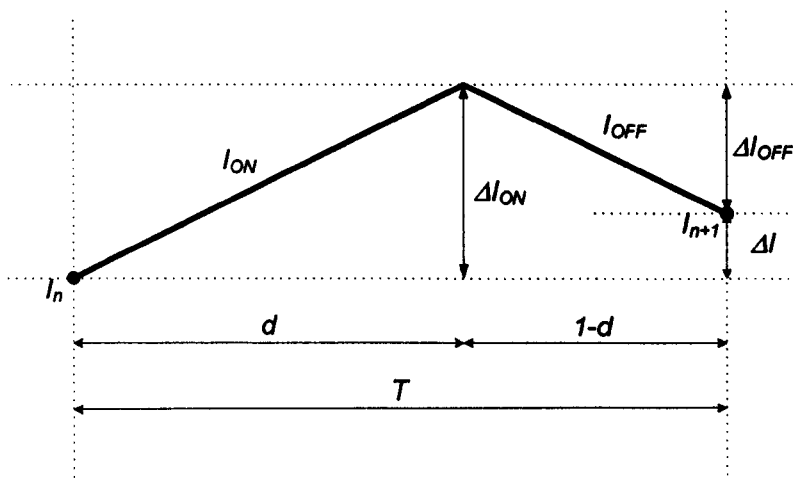

Figure D-3 Inductor current waveform during one sampling period

Where

T	is the sampling period, s.
'*d*'	is the on-period during one switching time, s.
'1-*d*'	is the off-period during one switching time, s.
I_n	is the inductor current at the beginning of the switching period, A.
I_{n+1}	is the inductor current at the end of the switching period, A.
I_{ON}	is the inductor current during on-period, A.
I_{OFF}	is the inductor current during off-period, A.
ΔI_{ON}	is the change in the inductor current during on-period, A.
ΔI_{OFF}	is the change in the inductor current during off-period, A.
ΔI	is the change in the inductor current over one sampling period, A and $\Delta I = \Delta I_{ON} - \Delta I_{OFF}$.

According to the control concept described in Figure 4-5 of chapter 4 and shown here again in Figure D-4, the inductor current is controlled by the reference current (I_{sc}*) produced from the voltage loop control.

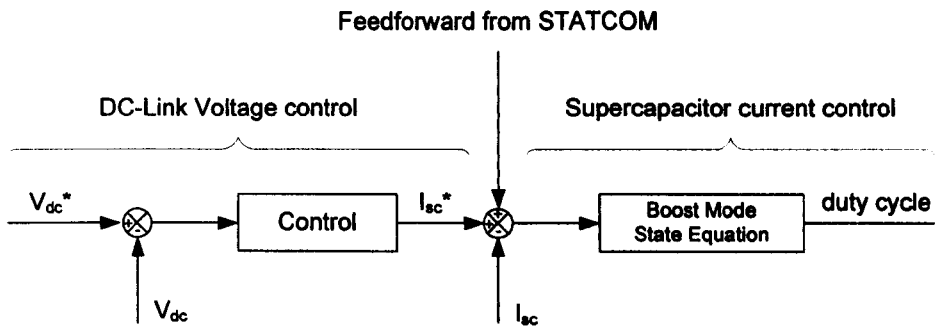

Figure D-4 Boost control concept

Where the supercapacitor current (I_{sc}) and the inductor current (I_L) is the same current. The change in the inductor current (ΔI) is related to the controlled reference current (I_{sc}*) – if the controlled reference current is increased, the change in the inductor current (ΔI) will be increased (with the duty cycle '*d*'

also increased). Therefore, to control the inductor current is to control the duty cycle of the switching device. These two parameters are related to each other as derived below.

When the SW is on, the voltage across the inductor (V_L) is equal to the voltage at the supercapacitor terminals (V_{sc}) as in Equation (D-1).

$$V_L = V_{sc} = \frac{L\Delta I_{ON}}{\Delta t_{ON}} \tag{D-1}$$

The period Δt_{ON} is the on-period and referring to Figure D-3 it equals to'd'. Assuming that there is no loss due to the internal resistance of the inductor, thus the inductor current increases linearly and the change in the current during the on-period (ΔI_{ON}) can therefore be calculated using Equation (D-2),

$$\Delta I_{ON} = \frac{dV_{sc}}{L} \tag{D-2}$$

When the SW is off, the voltage across the inductor (V_L) is given as in Equation (D-3).

$$\begin{aligned} V_L &= V_{dclink} - V_{sc} \\ &= \frac{L\Delta I_{OFF}}{\Delta t_{OFF}} \end{aligned} \tag{D-3}$$

The period Δt_{OFF} is the off-period and equals to'1-d'. The change in the current during the off-period (ΔI_{OFF}) can be found in Equation (D-4).

$$\Delta I_{OFF} = \frac{(1-d)(V_{dclink}-V_{sc})}{L} \tag{D-4}$$

Therefore, the change in the inductor current is given below.

$$\begin{aligned} \Delta I &= \Delta I_{ON} - \Delta I_{OFF} \\ &= \frac{dV_{sc}}{L} - \frac{(1-d)(V_{dclink}-V_{sc})}{L} \end{aligned} \tag{D-5}$$

From Equation (D-5), the change in the current over one sampling period is given in Equation (D-6) and the boost mode duty cycle is given in Equation (D-7).

$$\Delta I = \frac{1}{L}\{(d-1)V_{dclink} + V_{sc}\} \tag{D-6}$$

$$d_{boost} = \frac{L\Delta I - V_{sc}}{V_{dclink}} + 1 \tag{D-7}$$

In Equation (D-7), 'LΔI' relates to the controlled reference current as described above and is provided by the voltage control loop.

D.3 State equation for buck mode operation

In buck mode, only the gating of the upper SW in Figure D-1 is controlled under the DCM switching technique, the lower SW will be gated OFF all the time. The buck mode circuit is shown in Figure D-5. Assuming that it is interfaced to the STATCOM's DC-link capacitor, where the STATCOM's DC-link acts as dc source (V_{dc}) supplying energy to the SCESS.

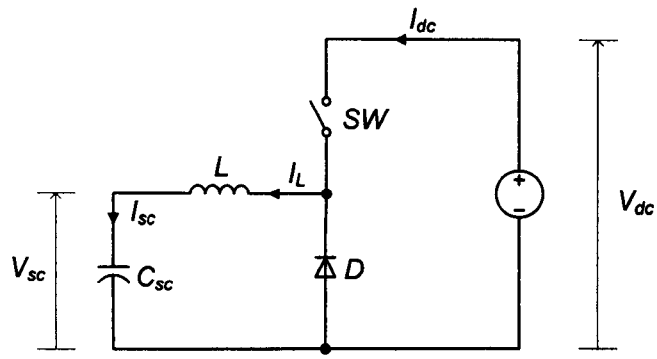

Figure D-5 The SCESS buck mode power circuit

Similar to boost mode operation, the inductor current is the main control parameter for controlling the flow of the energy, but the direction of the current is reverse – the energy will be transferred from the DC-link side to the supercapacitor modules. The control concept for buck mode operation described as in Figure 4-6 of chapter 4 and is shown again here in Figure D-6. The change in the inductor current during one sampling period is the same as the inductor current waveform shown in Figure D-3.

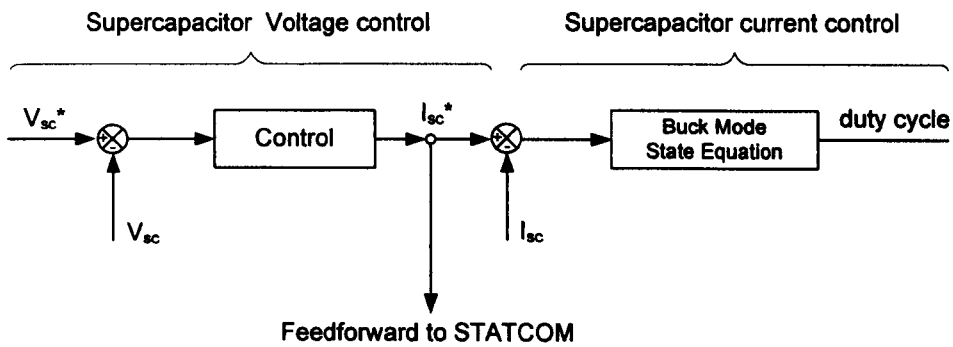

Figure D-6 Buck mode control concept

In Figure D-3, the supercapacitor current (I_{sc}) equals the inductor current (I_L). The same relationship as described for boost mode control, the change in the inductor current (ΔI) is related to the controlled reference current (I_{sc}^*), and the inductor current will be controlled proportional to the duty cycle due to the state equation derived below.

When the SW is on, the voltage drop across the inductor is given in Equation (D-8).

$$V_L = V_{dclink} - V_{sc} = \frac{L\Delta I_{ON}}{\Delta t_{ON}} \quad \text{(D-8)}$$

During on-period Δt_{ON}, the inductor current increases linearly without losses, the change in the inductor current during this period in defined by Equation (D-8).

$$\Delta I_{ON} = \frac{d(V_{dclink} - V_{sc})}{L} \quad \text{(D-9)}$$

When the SW is off, the supercapacitor voltage (V_{sc}) equals the inductor voltage (V_L) as shown in Equation (D-10) due to the conduction of the diode.

$$V_L = V_{sc} = \frac{L\Delta I_{OFF}}{\Delta t_{OFF}} \quad \text{(D-10)}$$

The change in the inductor current during off-period Δt_{OFF} is defined in Equation (D-11).

$$\Delta I_{OFF} = \frac{(1-d)V_{sc}}{L} \quad \text{(D-11)}$$

Again referring to Figure D-3, the overall change in the inductor current during one sampling period (ΔI) is given.

$$\begin{aligned} \Delta I &= \Delta I_{ON} - \Delta I_{OFF} \\ &= \frac{d(V_{dclink}-V_{sc})}{L} - \frac{(1-d)V_{sc}}{L} \end{aligned} \tag{D-12}$$

From Equation (D-12), the change in the inductor current over one sampling period under buck mode is given in Equation (D-13) and the buck mode duty cycle is given in Equation (D-14).

$$\Delta I = \frac{1}{L}\{dV_{dclink} - V_{sc}\} \tag{D-13}$$

$$d_{buck} = \frac{L\Delta I+V_{sc}}{V_{dclink}} \tag{D-14}$$

Appendix E

Simulink implementation for the simulation of a power system using STATCOM plus SCESS And for dSPACE controller board

E.1 Introduction

With the aim to build the experimental rig to demonstrate the benefit of the system using the conventional STATCOM and the enhanced STATCOM with supercapacitor energy storage system (STATCOM plus SCESS), the simulation of the proposed system is necessary. Referring to the proposed experimental validation system shown in Figure E-1, the operation of the STATCOM plus SCESS is designed using dSPACE digital controller board

which can be programmed with the software implemented using MatLab/Simulink package similar to the graphical coding for the simulation using MatLab / Simulink / SimPowerSystems blockset. Therefore, the simulation work described in the next sections is implemented digitally in order to be ready for applying directly to the controller board.

All the simulink implementation described in this appendix can be applied directly for the dSPACE digital controller board except the power circuit, measurement block, interrupt signal generation, and filter block. More additional details are added to these blocks explaining the difference between the simulink implemented for the simulation and for dSPACE board.

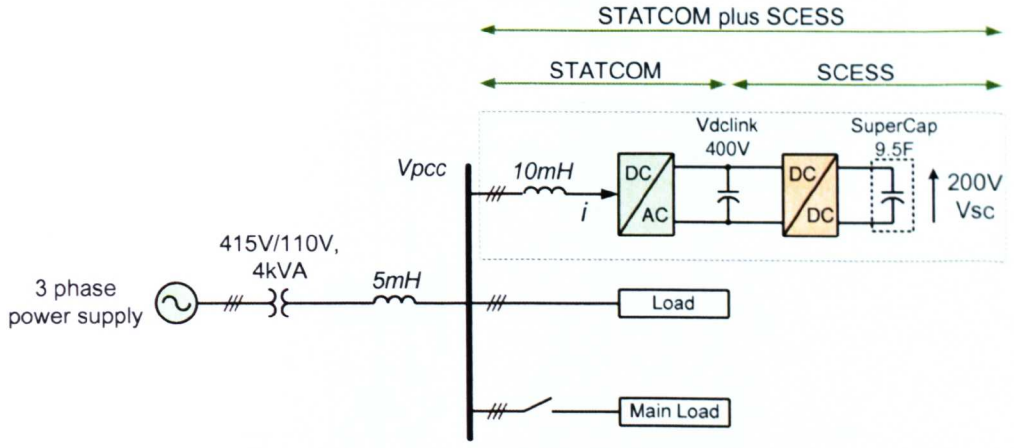

Figure E-1 The single line diagram of the proposed system

E.2 A power system using STATCOM and STATCOM plus SCESS

The overall power circuit model for the simulation work implemented using MatLab / Simulink / SimPowerSystems is shown in Figure E-2 and Figure E-3. The experimental rig built based on this power circuit is described in chapter 5.

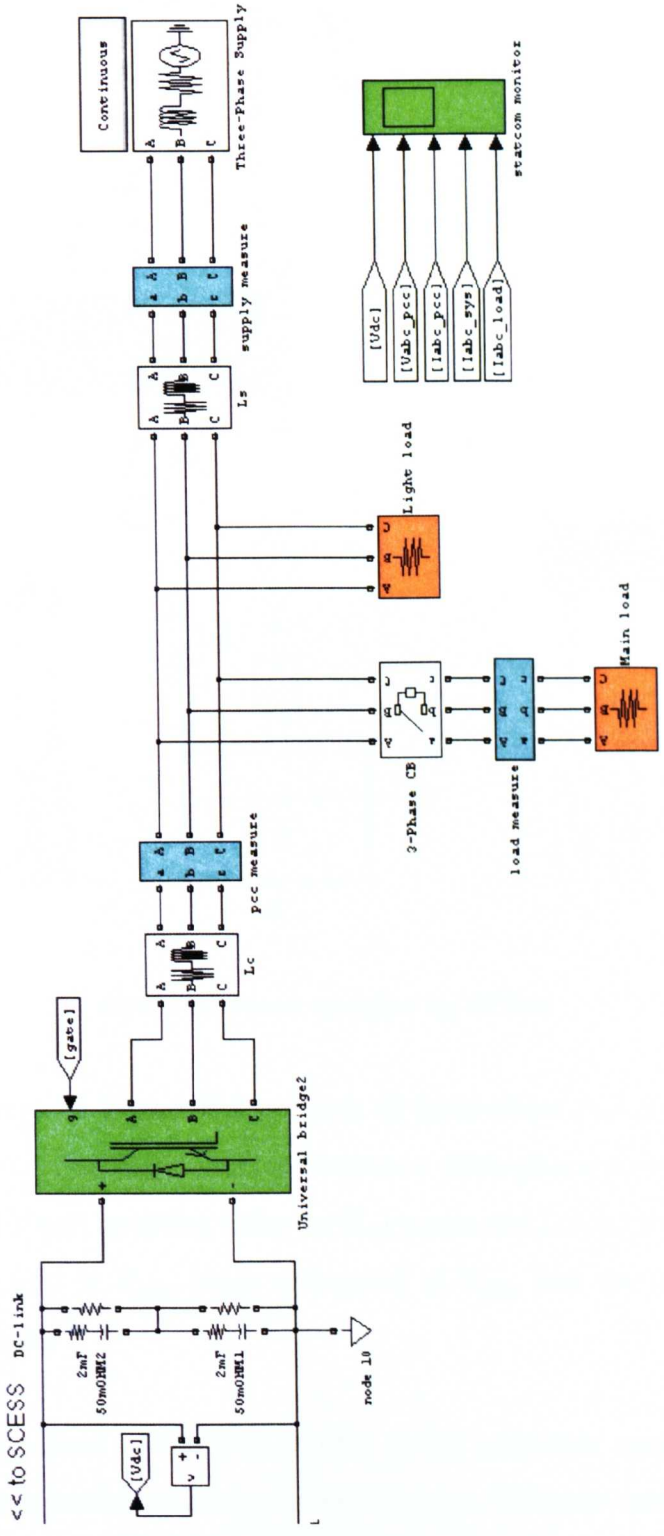

Figure E-2 Power circuit of a system supplying a sudden load using STATCOM

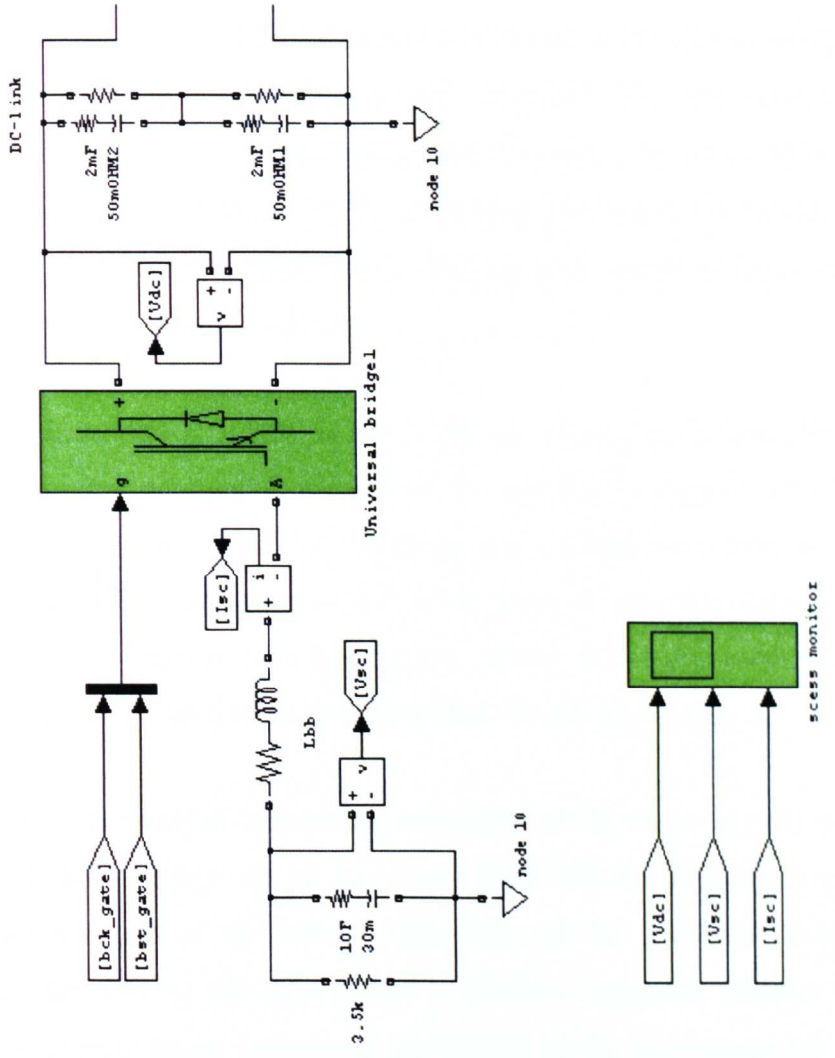

Figure E-3 Power circuit of the SCESS

The model shown in Figure E-2 consists of three-phase power supply, 0.1Ω 5mH system inductor (L_s) connected between three-phase power supply and V_{pcc} bus, 0.1Ω 10mH coupling inductor (L_c) connected linking the STATCOM unit to the ac grid at V_{pcc}, loads connected at V_{pcc}, and the measuring and monitoring blocks.

The main component of the STATCOM is the converter named 'universal bridge2' which is modelled using universal bridge. This universal bridge is set to be the 3-arm IGBT/Diode bridge with all the parameters set as its simulink's default. The ac side of the bridge is connected to the ac grid

through the coupling inductor Lc, while the dc side is connected to the DC-link capacitor which is comprised of two conventional capacitors rating 400V 2mF connected in series (resulting in 1mF capacitor). The two capacitors are also modelled with 50mΩ internal resistance. The operation of the STATCOM is controlled using sinewave PWM switching technique described in the STATCOM plus SCESS control model. Voltage and current of the SCESS are monitored at 'scess monitor' block.

The three-phase power supply is set to be an 110V line-to-line 50Hz Y-g source. The other parameters are left as its simulink's default. Three-phase power circuit breaker is used to switch on and off the main load to V_{pcc} as shown in Figure E-2. The main load is set to draw an approximate 8A current from V_{pcc} bus when it is switched on, while the light load will take approximately 1.5A continuously as proposed for the experiments.

In Figure E-3, the SCESS is modelled consisting of the dc-to-dc converter that uses a universal bridge set to be 1-arm IGBT/Diode bridge - the other parameters are left as its default. One side of the universal bridge1 is connected interface to the STATCOM's DC-link capacitor, another side is connected to buck-boost inductor (L_{bb}) linking to the supercapacitor model. Lbb is used as the medium to transfer the energy between the supercapacitor and the DC-link according to the universal bridge1's switching function. The supercapacitor is modelled using 10F 200V capacitor with 30mΩ series internal resistance and 3.5kΩ parallel resistance as shown in Figure E-3. The operation of the SCESS is controlled by DCM (Duty Cycle Modulation) switching technique described in the STATCOM plus SCESS control model section.

E.3 STATCOM plus SCESS control

The control implemented for both the simulation and dSPACE controller board is illustrated graphically in Figure E-4. The overall model consists of measurement blocks and the model blocks named 'filter', 'control', 'statcom pwm', 'bst dcm' and 'bck dcm'. All these blocks including the interrupt signal generation are described in the following sub-sections.

In order to demonstrate the benefits of the STATCOM plus SCESS, the STATCOM unit can be able to operate with and without SCESS according to the operation mode described in the 'statcom control' block. The results explained in both chapter 3 the simulation of an ac power system using the standard STATCOM and chapter 4 the simulation of an ac power system using the enhanced STATCOM with supercapacitors are from the simulation based on the Simulink implemented in this appendix.

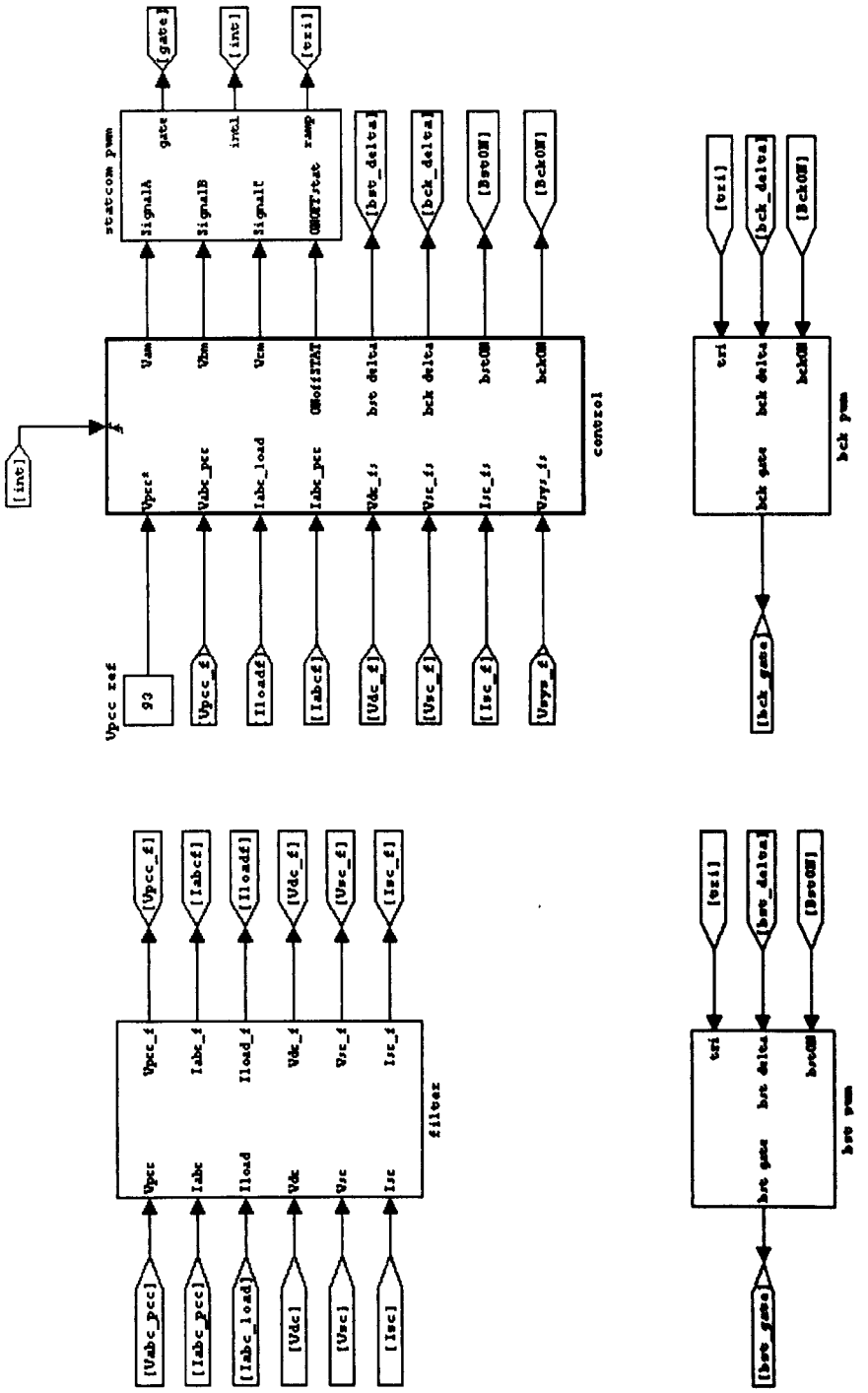

Figure E-4 The STATCOM plus SCESS control model

E.3.1 Measurement blocks

For the simulation, the blocks named 'pcc measure', 'load measure', and 'supply measure' blocks are added to measure voltages and currents and to display the values using scope named 'statcom monitor' block. These measurement blocks are modelled using the standard simulink's voltage and current measurement that can also provide the necessary input data for the control system.

For the experimental, transducers are built to measure all the relevant voltage and current and pass to dSPACE controller board. For the dSPACE board, the software implemented for reading the measured data fed from the transducers is shown in Figure E-5.

In Figure E-5, the dSPACE analog input blocks DS1104ADC are used to read all the input data as listed in Table E-1below.

Table E-1 dSPACE ADC input channels and its associating input data

dSPACE ADC channels	Input data
DS1104MUX_ADC_C1	V_{sc} – Supercapacitor voltage
DS1104MUX_ADC_C2	V_{dc} – DC-link voltage
DS1104MUX_ADC_C3	V_{ab} – line to line voltage at V_{pcc}
DS1104MUX_ADC_C4	V_{bc} – line to line voltage at V_{pcc}
DS1104ADC_C5	I_{sc} – Supercapacitor current
DS1104ADC_C6	I_{a_load} and I_{b_load} – Load current
DS1104ADC_C7	I_a – STATCOM's current
DS1104ADC_C8	I_b – STATCOM's current

Due to the input channel is limited up to 8 channels (4 direct-input and 4 multiplexed-input channels), DS1104ADC_C6 is therefore implemented with hardware multiplexer (block named 'I load') in order to read load currents I_{a_load} and I_{b_load}.

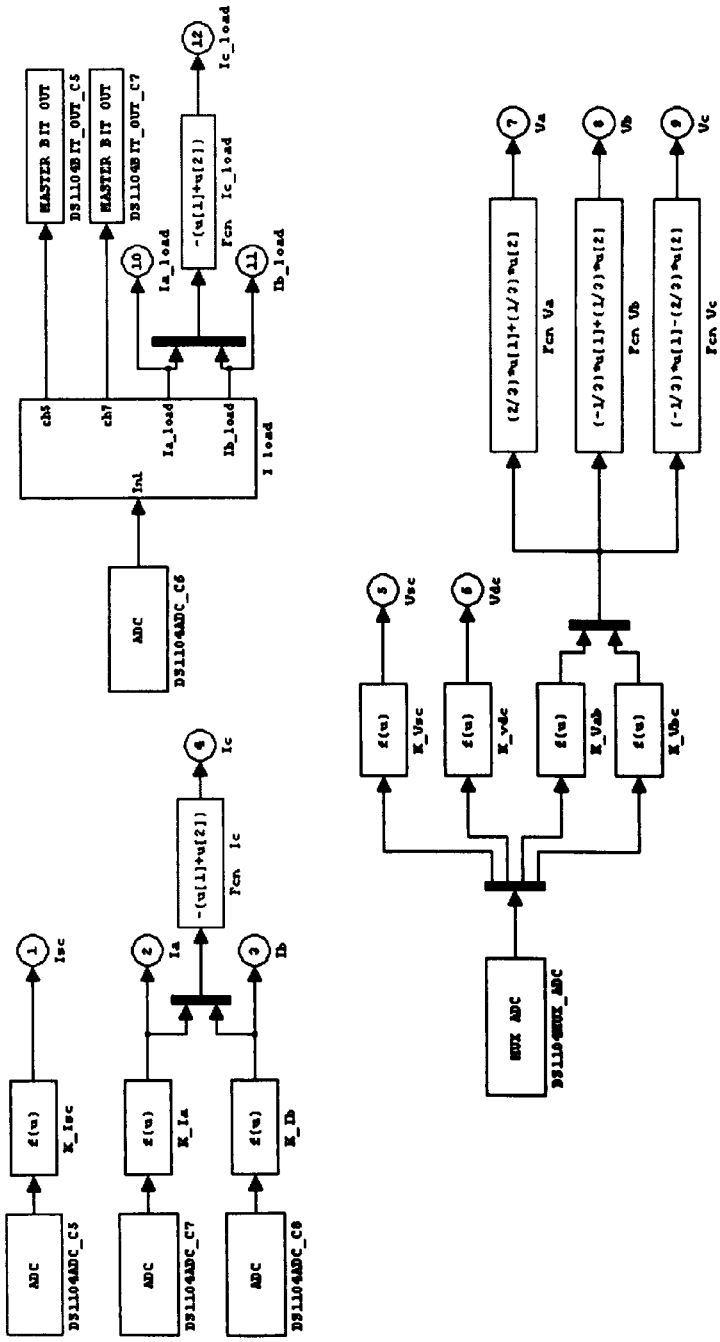

Figure E-5 Simulink implemented for dSPACE to read the input data

Phase 'c' current of the STATCOM and of the main load is calculated using Equation (E-1). While phase voltage of V_{pcc} is calculated using Equation (E-2).

$$I_c = -(I_a + I_b) \tag{E-1}$$

$$\begin{bmatrix} V_a \\ V_b \\ V_c \end{bmatrix} = \begin{bmatrix} 2/3 & 1/3 \\ -1/3 & 1/3 \\ -1/3 & -2/3 \end{bmatrix} \begin{bmatrix} V_{ab} \\ V_{bc} \end{bmatrix} \tag{E-2}$$

E.3.2 Interrupt signal generation

For the simulation the interrupt signal is generated in the 'statcom pwm' block by producing a narrow pulse whenever the triangular carrier wave of the switching frequency reaches 95% as shown in the top trace of Figure E-6 and defined as 'int' signal.

For the dSPACE controller board the interrupt signal is generated, automatically from the dSPACE built-in functional block named 'DS1104SLAVE_PWM INT' as shown in Figure E-7. The interrupt signal is produced, with the same principle as in Figure E-6, corresponding to the three-phase PWM generated by dSPACE built-in block 'DS1104SL_DSP_PWM3'. Another functional block named 'DS1104SYNC_IO_SETUP' is placed in order to synchronise the input data reading with the interrupt signal.

The concept for synchronising the signals in dSPACE controller board is to feed the trigger port of the main block with the interrupt signal as shown in

Figure E-7; all the simulink implemented for dSPACE is contained and manipulated in the main block.

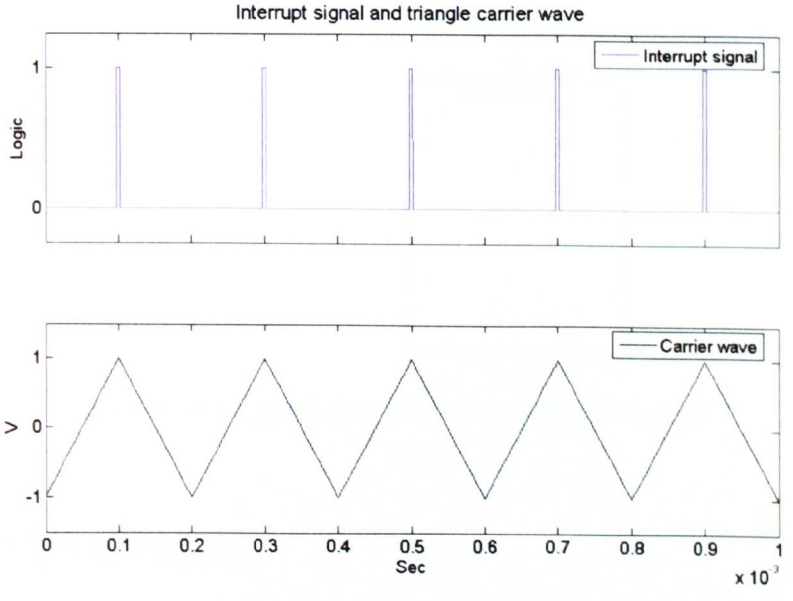

Figure E-6 Interrupt signal for the simulation

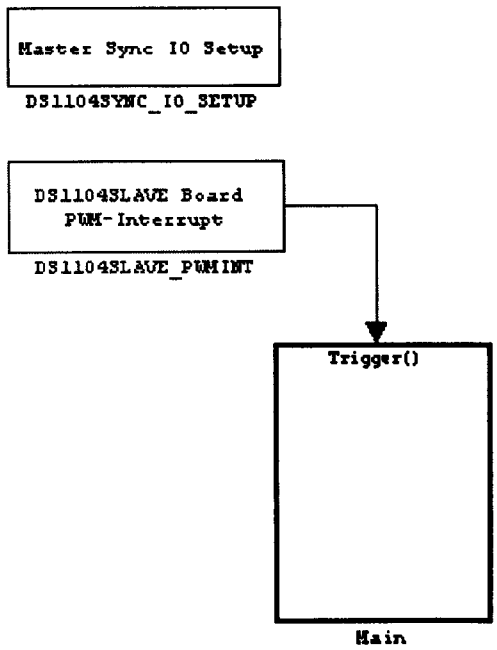

Figure E-7 Interrupt signal for dSPACE controller board

E.3.3 'filter' block

In simulation, the 'filter' block takes the data from the measurement blocks then filters to get rid of the switching noises, for example the filter model for the three-phase current filtering implemented in the 'filter' block is shown in Figure E-8, where the first order transfer function is used as the low pass filter. The cur-off frequency of the filter is mentioned in chapter 3. The output signals from the 'filter' block are passed directly to the control block.

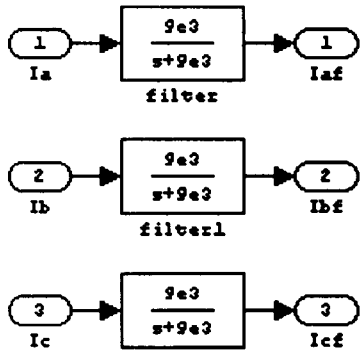

Figure E-8 The filter model for the three-phase current

In practice, analog low pass filter boards are built for filtering all the data from transducer boards before passing the data to the dSPACE controller board as described in chapter 5.

E.3.4 'control' block

The 'control' block takes the filtered data from the 'filter' block and then performs the control process with the aim to produce the demand voltage in order to control the flow of power between the STATCOM terminals and the ac grid at V_{pcc}. More detail of the 'control' block is illustrated in Figure E-9.

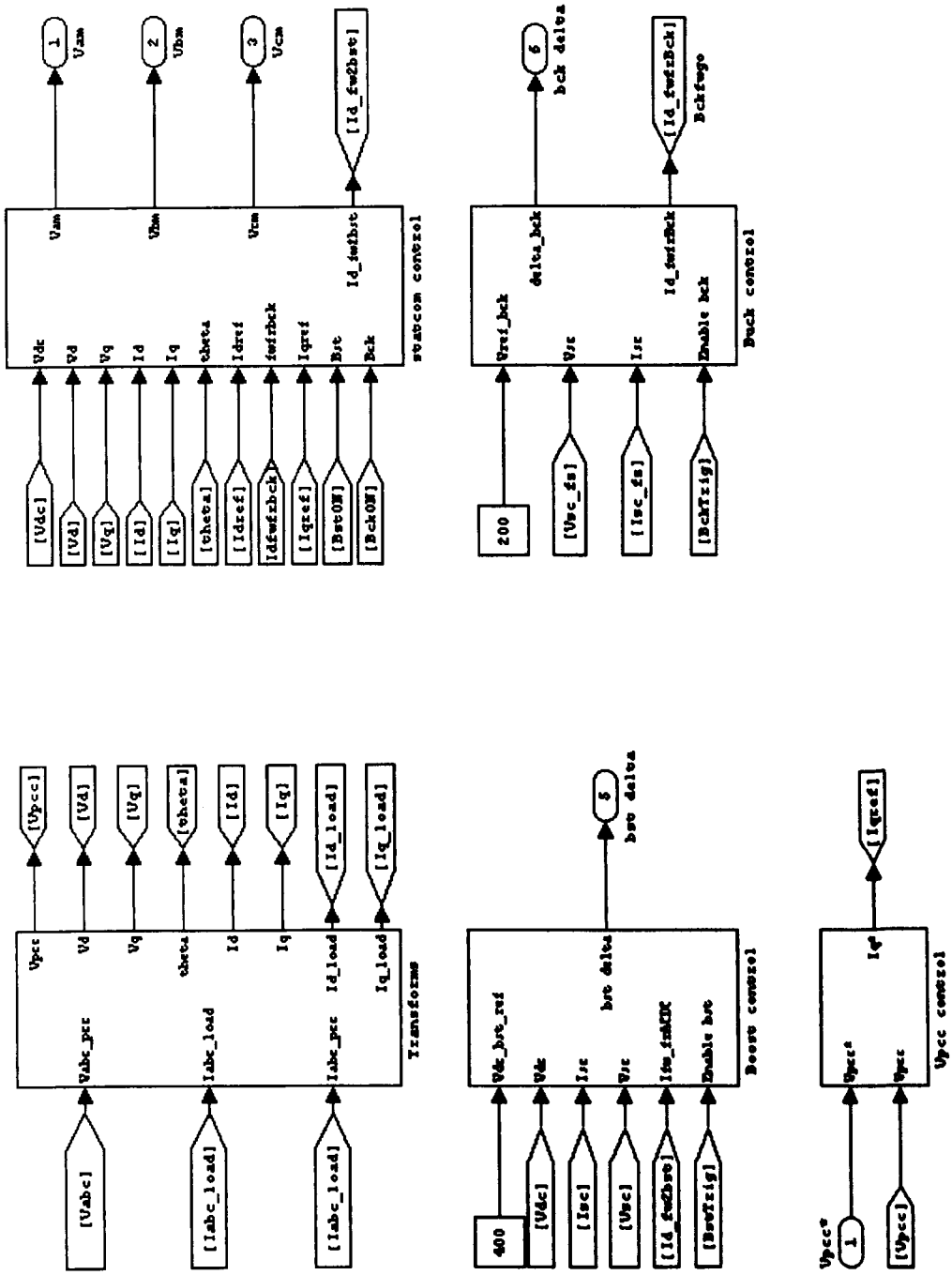

Figure E-9 The 'control' block

The 'control' block consists of five more sub-blocks named 'transforms', 'statcom control', 'V_{pcc} control', 'boost control', and 'buck control' described below.

E.3.4.1 'transform' block

In order to modulate the flow of the power between V_{pcc} and the dc-to-ac converter using vector control strategy, all the three-phase voltage and current are needed to be in the d-q rotating frame. The 'transforms' block is used to apply the transformation described in chapter 3 to the Vpcc voltage, STATCOM current, and load current as shown in Figure E-10.

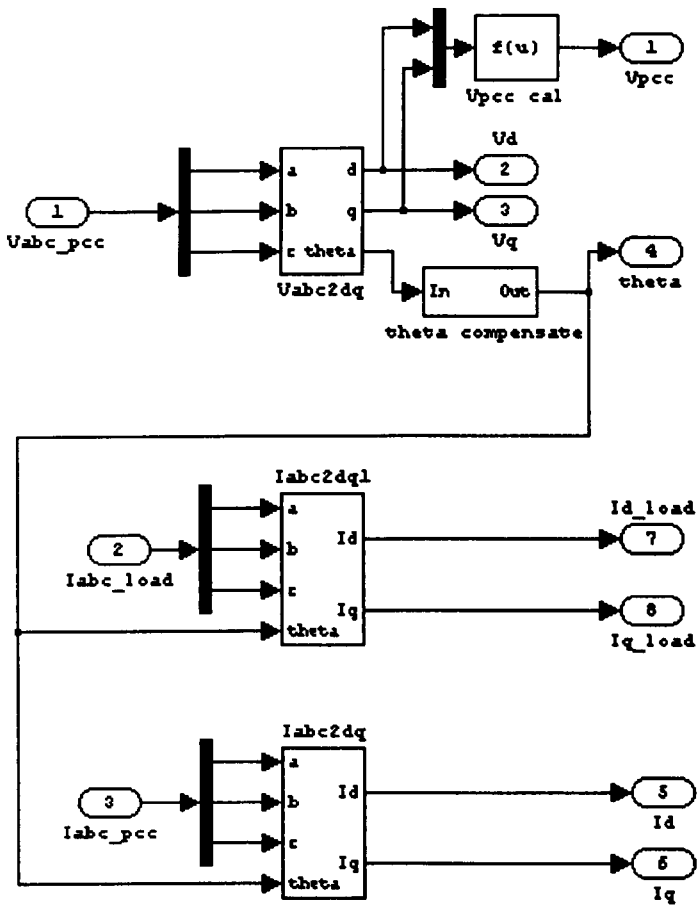

Figure E-10 The 'transform' block

In Figure E-10, due to the delay in the control-loop the time of one sampling period is added in the angle of the transformation by the block named 'theta

compensate'. The 'V_{pcc} cal' block calculates the peak voltage of V_{pcc} using Equation (E-3).

$$V_{pcc} = \sqrt{(V_d^2 + V_q^2)} \tag{E-3}$$

This 'transform' block is used in both the software implementation for the dSPACE controller board and for the simulation.

E.3.4.2 'statcom control' block

More detail inside 'statcom control' block is the vector control graphically shown here in Figure E-11. The STATCOM's DC-link voltage and current controller are implemented using simulink as shown in Figure E-12 and Figure E-13 respectively based on the PI controller discrete transfer function equation (3-24) and (3-27) described in chapter 3, and given again in Equation (E-4) and (E-5) respectively.

$$C(z) = \frac{0.1276z - 0.1264}{z - 1} \tag{E-4}$$

$$C(z) = \frac{6.19z - 5.83}{z - 1} \tag{E-5}$$

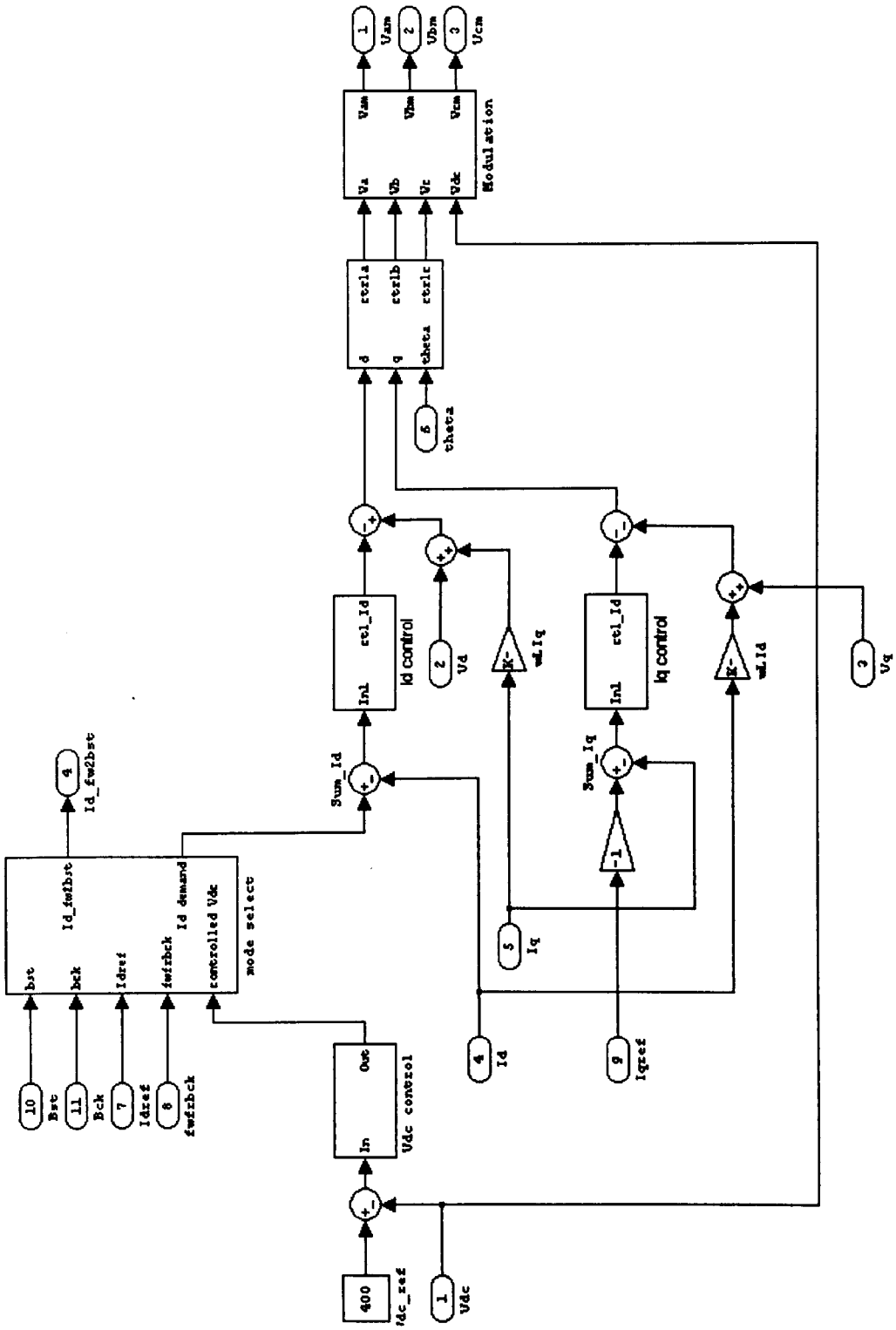

Figure E-11 'statcom control' block

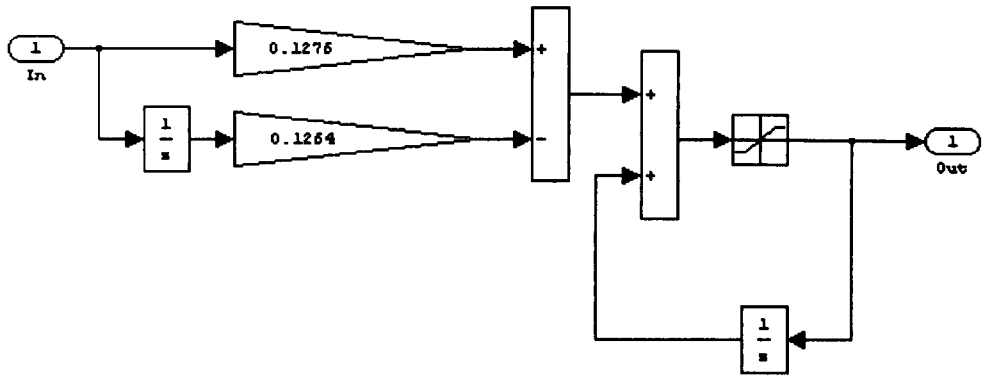

Figure E-12 DC-link control implemented using simulink

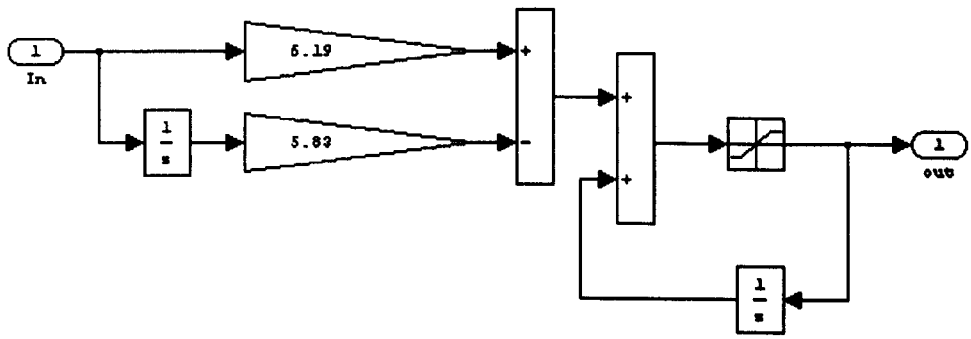

Figure E-13 Current control implemented using simulink

The 'modulation' sub-block in Figure E-11 modulates the resulting voltage from the control using Equation (E-6).

$$V_m = \frac{2V}{V_{dc}} \tag{E-6}$$

Where

V is the input phase peak voltage of 'modulation' sub-block.

V_m is the modulated output voltage of 'modulation' sub-block.

V_{dc} is the DC-link voltage.

The sub-block named 'mode select' is added in order to produce different modes for the d-axis current control. For example during the period the STATCOM is delivering real power to the ac grid, the STATCOM's DC-link voltage control will be ignored. The DC-link voltage will be regulated by boost mode of the SCESS. The 'mode select' block will set the d-axis current reference corresponding to load current and provide the feedforward current to the SCESS.

During the buck mode where the SCESS will absorb energy from the ac grid, the DC-link voltage will be regulated by the STAT COM's DC-link control and the feedforward current from the SCESS will define the additional power transferring to the supercapacitor modules. While performing STATCOM only mode, the 'mode select' will feed only the output of the STATCOM's DC-link control to be the d-axis current reference and the q-axis current reference will be defined by the V_{pcc} controller. More detail of the STATCOM plus SCESS control operation can be found in chapter 4.

In 'mode select' block, a logic circuit is implemented using the truth table designed as shown in Table E-2. This block will define the three operation modes described above – real power inject, real power absorb, and STATCOM only modes.

Table E-2 The truth table designed for mode selection

INPUT		OUTPUT		
A	B	Y1	Y2	Y3
0	0	0	0	0
0	1	1	0	0
1	0	0	1	0
1	1	0	0	1

Where

A	is the boost logic produced from 'auxiliary control' block.
B	is the buck logic produced from 'auxiliary control' block.
Y1	is the output logic defined for the real power injection mode.
Y2	is the output logic defined for the real power absorption mode.
Y3	is the output logic defined for the STATCOM only mode.

For the additional 'mode select' block, the resulting output logic equations from Table E-2 are shown in Equation (E-7) and implemented using simulink based as shown in Figure E-14.

$$\begin{aligned} Y1 &= \bar{A} \cdot B \\ Y2 &= A \cdot \bar{B} \\ Y3 &= A \cdot B \end{aligned} \tag{E-7}$$

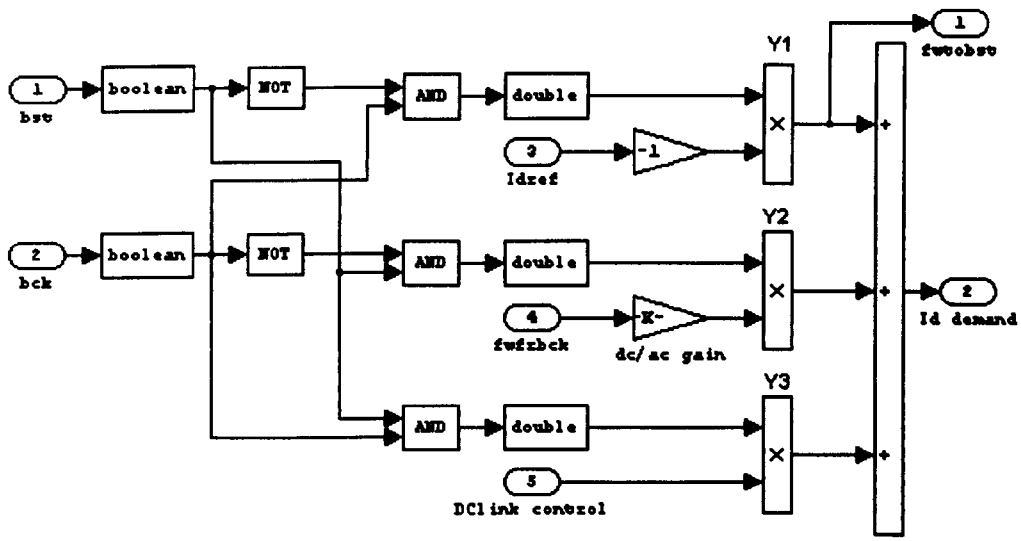

Figure E-14 Detail of 'mode select' block

In Figure E-14, 'bst' and 'bck' logic are fed from the 'auxiliary control' block to input port 1 and 2 respectively. The d-axis current extracted from load current is fed to input port 3; feedforward current from the SCESS is fed to input port 4, and the output from the STATCOM's DC-link control is fed to

input port 5. The output port 1 gives the feedforward current to the SCESS and the output port 2 is used as the d-axis current reference as shown in Figure E-11.

E.3.4.3 V_{pcc} control block

V_{pcc} controller is designed in chapter 3 and resulted in the discrete transfer function Equation (3-30), rewriting again in Equation (E-8) and is implemented in this section using the simulink based control block as shown in Figure E-15.

$$C(z) = \frac{0.003368z^2 - 2.035e^{-5}z - 0.003348}{z^2 - 1.999z + 0.999} \quad \text{(E-8)}$$

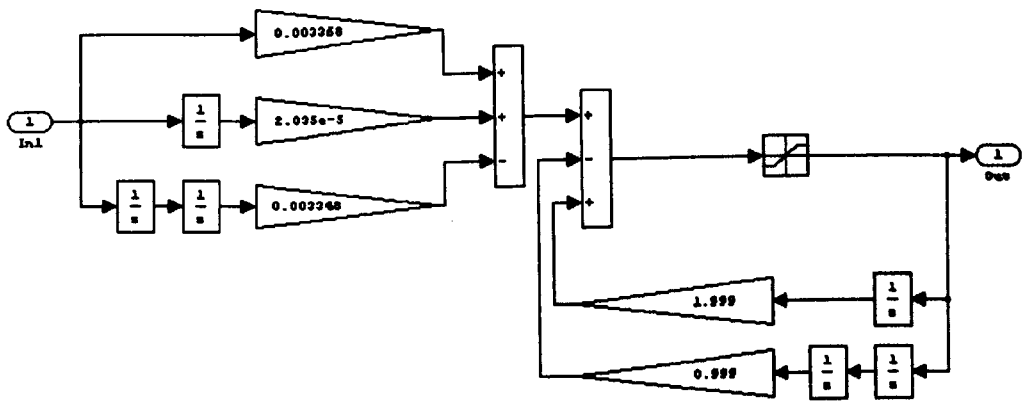

Figure E-15 V_{pcc} controller implemented using simulink

E.3.4.4 Boost control block

The control concept for the boost mode dc-to-dc converter described in chapter 4 is implemented using simulink based control block in the 'boost control' block shown in Figure E-16.

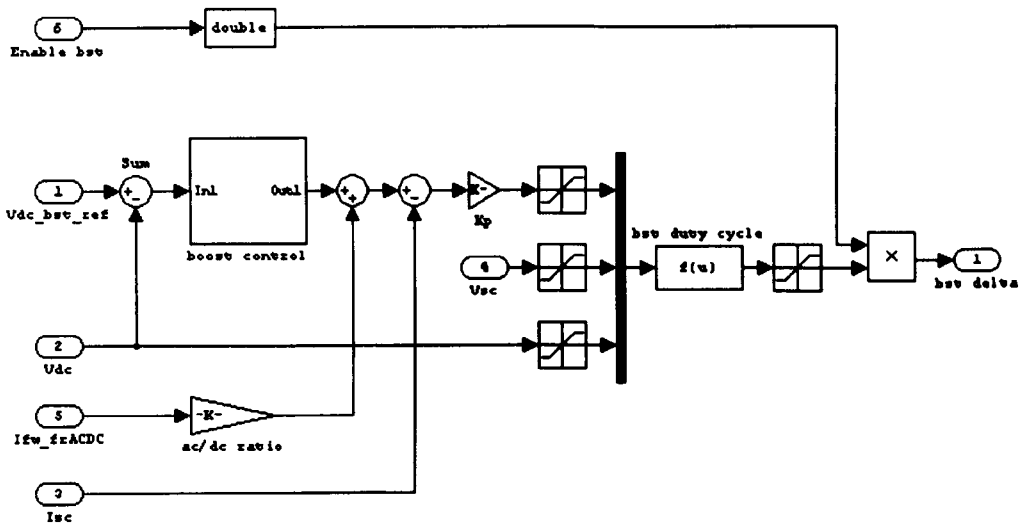

Figure E-16 'boost control' block

In Figure E-16, the outer voltage control loop is designed to regulate the DC-link voltage (or the dc side voltage of the STATCOM). This voltage controller is implemented based on the discrete transfer function Equation (4-8) designed for the boost mode operation of the dc-to-dc converter described in chapter 4 and rewritten again in Equation (E-9). The simulink based controller implementation using Equation (E-9) is illustrated in Figure E-17.

$$C_{boost}(z) = \frac{0.1589z^2 - 0.15810z}{z^2 - 1.538z + 0.5385} \qquad \text{(E-9)}$$

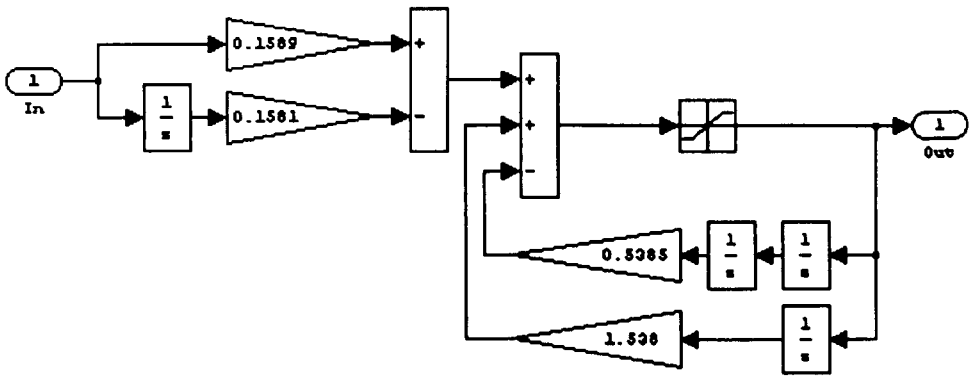

Figure E-17 Boost mode controller

For the inner current control loop, boost mode state equation described in appendix D is applied in the functional block named 'bst duty cycle' in order to produce the duty cycle for the dc-to-dc converter operating in the boost mode according to the duty modulation technique during the process of injecting energy to the ac grid. The response performance of the proposed control is improved with the feedforward current from the STATCOM unit feeding into the input port 5.

E.3.4.5 Buck control block

In 'buck control' block, the simulink based on the buck mode control concept described in chapter 4 is implemented as shown in Figure E-18, where the outer loop voltage control is designed to regulate the supercapacitor voltage. The buck mode state equation derived in appendix D and implemented in the functional block named 'bck duty cycle' in defines the value of the duty cycle for the buck mode operation dc-to-dc converter in order to regulate the current during energy storage process.

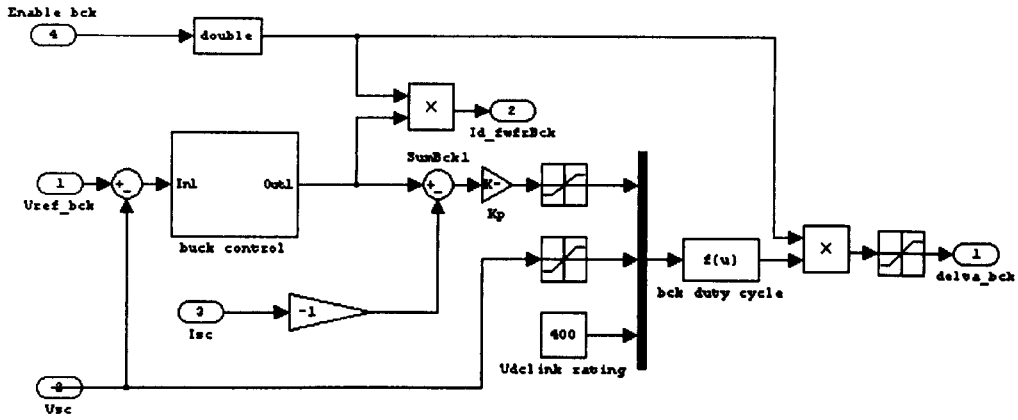

Figure E-18 'buck control' block

The controller for the supercapacitor voltage regulation designed in chapter 4 is Equation (4-11) and given again here in Equation (E-10).

$$C_{buck}(z) = \frac{0.3476z^2 - 0.4609z + 0.1150}{z^2 - 1.999z + 0.999} \qquad \text{(E-10)}$$

Based on Equation (E-10), the buck mode controller is implemented using simulink as shown in Figure E-19.

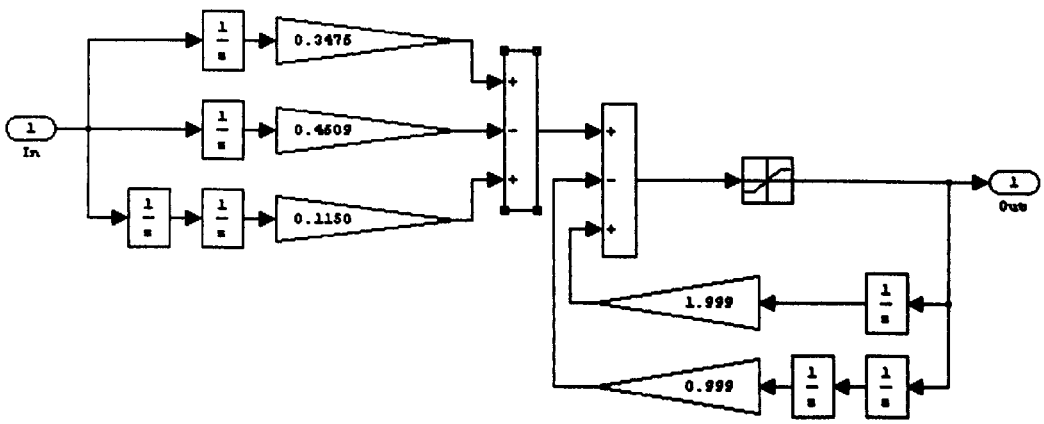

Figure E-19 Buck mode controller

E.3.5 'statcom pwm' block

For the simulation, the resulting signals from the 'control' block, the modulated three-phase voltage signals, are passed to 'statcom pwm' block in order to generate PWM switching signal for the universal bridge2. In 'statcom pwm' block, the triangular carrier wave locally generated to produce the interrupt signal is also used to compared with the modulated three-phase voltage signals coming from the input port '1' to '3' to generate the associated PWM switching signal as shown in Figure E-20.

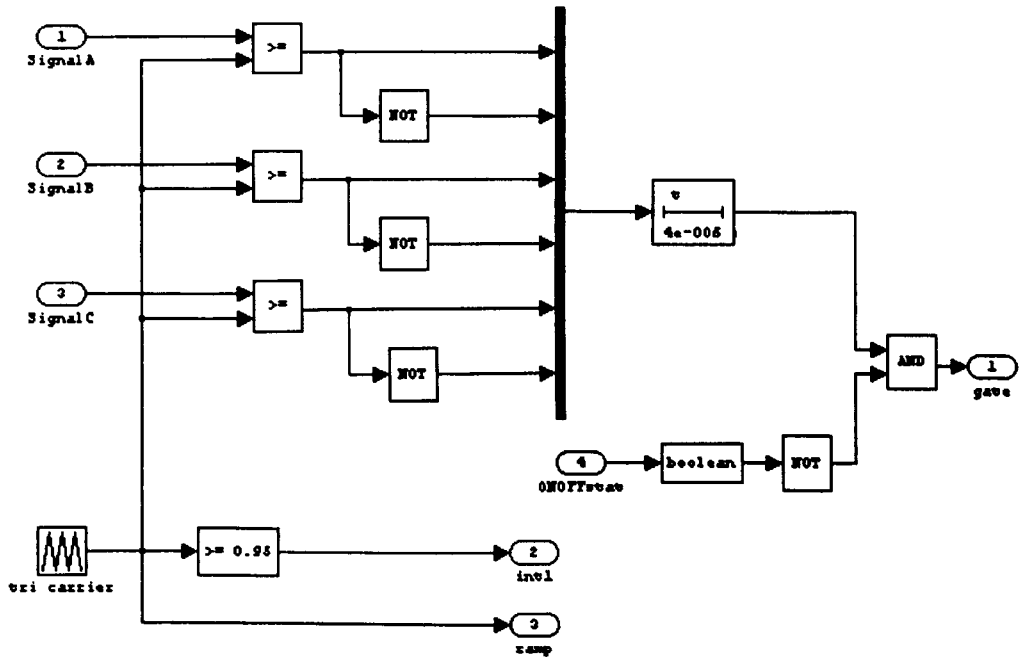

Figure E-20 PWM generation for the simulation

In Figure E-20, on/off delay is used to manipulate the resulting output signals from the comparison in order to adjust the delay time (dead-time) of the switching devices. This PWM signal is then sent to the input port 'g' of the universal bridge2 for turning on and off the IGBTs according to the modulation technique employed the standard sinewave PWM. According to input port 'ONOFFstat' the output PWM signal 'gate' can also be blocked or

allowed according to the protection implemented in the 'Protection' block described in section E.3.7.4.

For the dSPACE controller board, the modulated three-phase voltage signals from the 'control' block are fed directly to the built-in functional block named DS1104SL_DSP_PWM3 shown in Figure E-21, at the input port 'Duty cycle a' 'b', and 'c' respectively corresponding to the three-phase voltage.

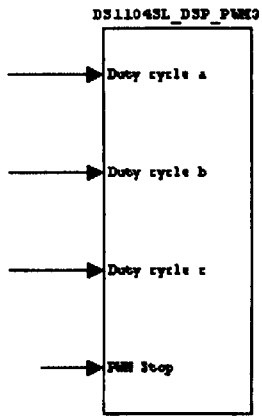

Figure E-21 dSPACE built-in three-phase PWM generator block

DS1104SL_DSP_PWM3 will automatically generate the PWM switching signal relating to the modulated signals fed into its input ports. This standard sinewave PWM signal is then used to turn on and off the IGBTs practically in order to generate the voltage at the STATCOM terminals respecting to the voltage at PCC bus.

E.3.6 'bst dcm' and 'bck dcm' block

For the simulation, the duty cycle produced from 'boost control' and 'buck control' blocks are passed into Duty Cycle Modulation (DCM) signal generation block named 'bst dcm' and 'bck dcm' in order to generate the gating signal for the dc-to-dc converter. The duty cycle from buck and boost

control are compared with the triangular carrier wave generated from 'statcom pwm' block, the same signal used for generating the interrupt signal, to produce the switching pulse gating signal. This pulse gating signal is then fed to the input port 'g' of the universal bridge1 to turn on and turn off the IGBTs inside the bridge corresponding to the DCM switching technique.

For the dSPACE controller board, in order to produce the DCM switching signal, the controlled duty cycle produced from 'boost control' and 'buck control' blocks are passed directly to the dSPACE built-in functional block named DS1104SL_DSP_PWM. By passing the boost and buck mode duty cycle to the input port 'PWM channel 2' and 'PWM channel 4' respectively as shown in Figure E-22, dSPACE controller board will automatically produce two of the switching signals separately according to the operation modes.

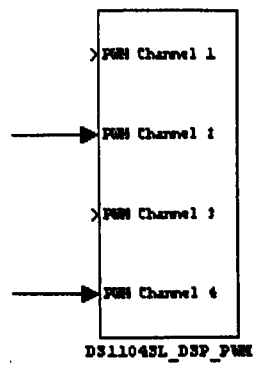

Figure E-22 dSPACE built-in 4-channel PWM generator block

E.3.7 Auxiliary control blocks

There are four auxiliary control blocks as illustrated in Figure E-23. They are designed to support the main control operation in order to be able to decide whether the operation should be controlled in buck or boost mode, to offer the manual start/stop control using the ControlDesk software package, and to

check if the STATCOM plus SCESS is operated under the acceptable condition as described in the following sub-sections.

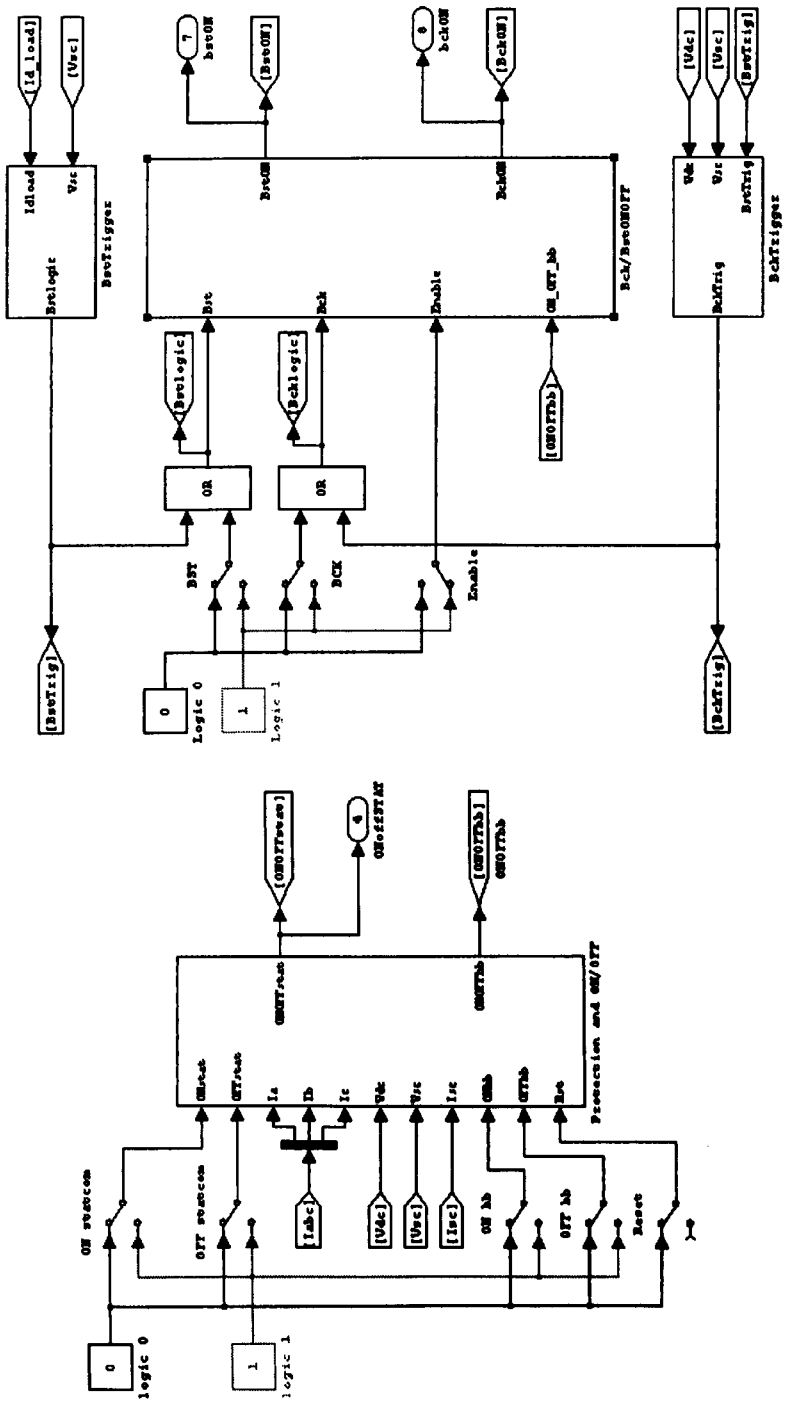

Figure E-23 Auxiliary control blocks

E.3.7.1 Boost Trigger block

This block is implemented in order to produce a logic signal telling the main control that the STATCOM plus SCESS should be operated in boost mode. Simulink implemented in Boost Trigger block employs SR-flip flops as indicated in Figure E-24. The block will detect if the main load is switched on (by checking load current), it will send output logic "1" to 'Bck/Bst ONOFF' block in order to provide the selected mode logic for the main control.

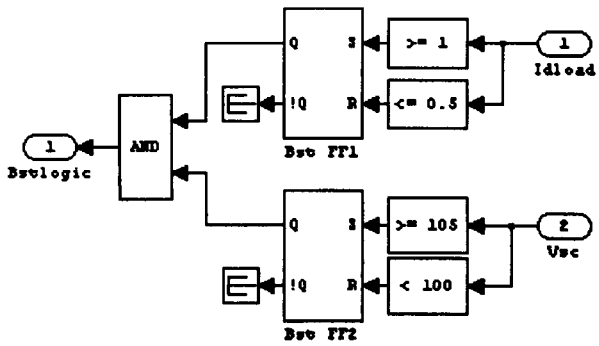

Figure E-24 'Boost Trigger' block

This block also check if the supercapacitor voltage is lower than its half rating, 'Boost Trigger' output logic will tell the main control to stop boost mode operation.

E.3.7.2 Buck Trigger block

In Figure E-25 a similar simulink model as implemented for 'Boost Trigger' block is used in 'Buck trigger' block, but it designed to tell the main control if the condition is allowed to operated in buck mode by checking the supercapacitor voltage and the DC-link voltage. If the STATCOM is not operated in boost mode operation ('BstTrig' logic is "0") and the DC-link

voltage and the supercapacitor voltage are in the acceptable range, the block will signal the main control to charge the supercapacitors.

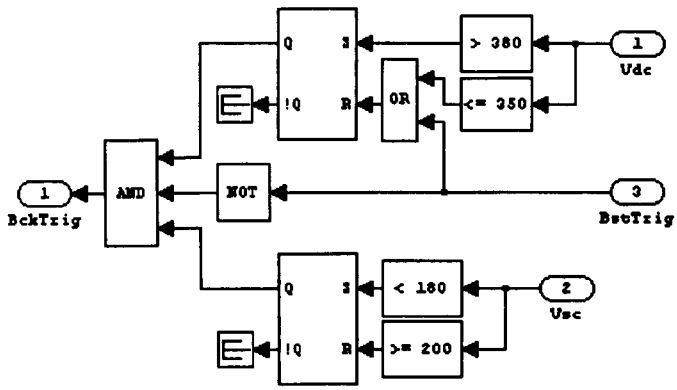

Figure E-25 'Buck Trigger' block

E.3.7.3 Bck / Bst ONOFF block

'Bck/Bst ONOFF' block is designed using logic gates as shown in Figure E-26. The purpose of this block is to provide the main control with the logic signals indicating mode of the operation. The operation mode signals are named 'BstON' and 'BckON' referring to boost and buck mode respectively. The boost mode means the SCESS is operating under boost control transferring the stored energy from the supercapacitors to the STATCOM's DC-link capacitor, and the STATCOM will further transfer the energy to the ac grid. In this project, boost mode is also called 'real power inject' mode. The buck mode means the SCESS is in buck control mode due to the operation to store the energy into the supercapacitors, with the STATCOM help in drawing the energy from the ac grid. This mode is also called 'real power absorb' mode.

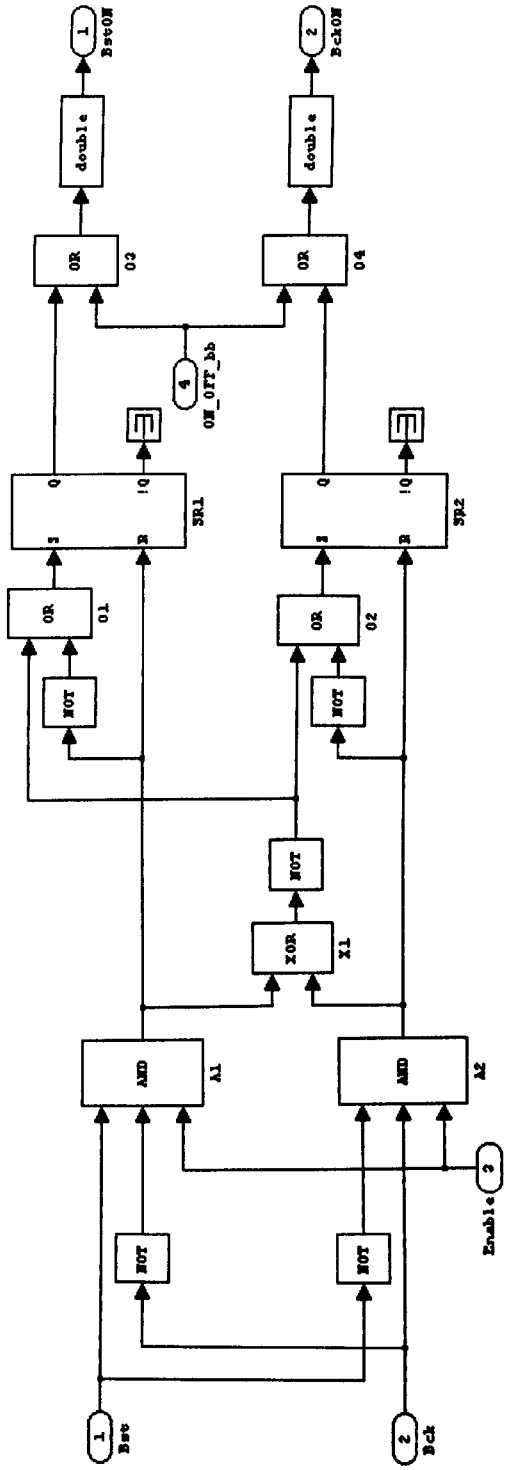

Figure E-26 'Bck/Bst ONOFF' block

There are four input ports for the logic gate combination in 'Bck/Bst ONOFF' block ('Bst', 'Bck', 'Enable', and 'ONOFF_bb') and two output ports (BstON and BckON). The input port 'Bst' and 'Bck' are fed with the logic produced from 'BstTrigger' and 'BckTrigger' blocks where the operation mode is selected upon the condition. The condition can also be selected manually using ControlDesk software package, which can be programmed to enforce the status of simulink constant named 'logic 0' and 'logic 1' shown in Figure E-23.

The logic combination will check if the input ports are fed with the same logic or if the manual logic from ControlDesk is not activated or if the 'Enable' port is not enabled by logic "1", it will set both SR-flip flops to hold the output (BstON and BckON) at logic "1". This means the STATCOM plus SCESS will operate in STATCOM only mode. If the input logic from 'BstTrigger' and 'BckTrigger' blocks are not identical to each other or manual logic from the ControlDesk is selected properly, the corresponding output logic will be sent to the additional 'mode select' block of the main control.

Both the output logic 'BstON' and 'BckON' will be held "1" whenever there is logic "1" from 'Protection block' is fed to the input port 'ONOFF_bb'. This indicates that the operation is in abnormal condition. If the STATCOM plus SCESS is injecting or absorbing real power, it will be back to the STATCOM only mode and finally stopped by the protection.

E.3.7.4 Protection block

Protection block shown in Figure E-27 is implemented as the primary protection (software protection) for the overall experimental test system. The secondary protection implemented using hardware circuit component is described in chapter 5. In the software protection shown in Figure E-27, it is designed to check if the STATCOM plus SCESS is operated under the ac the

acceptable condition or not. If the condition becomes overlimited, the protection will tell the control to stop the operation of the STATCOM plus SCESS immediately.

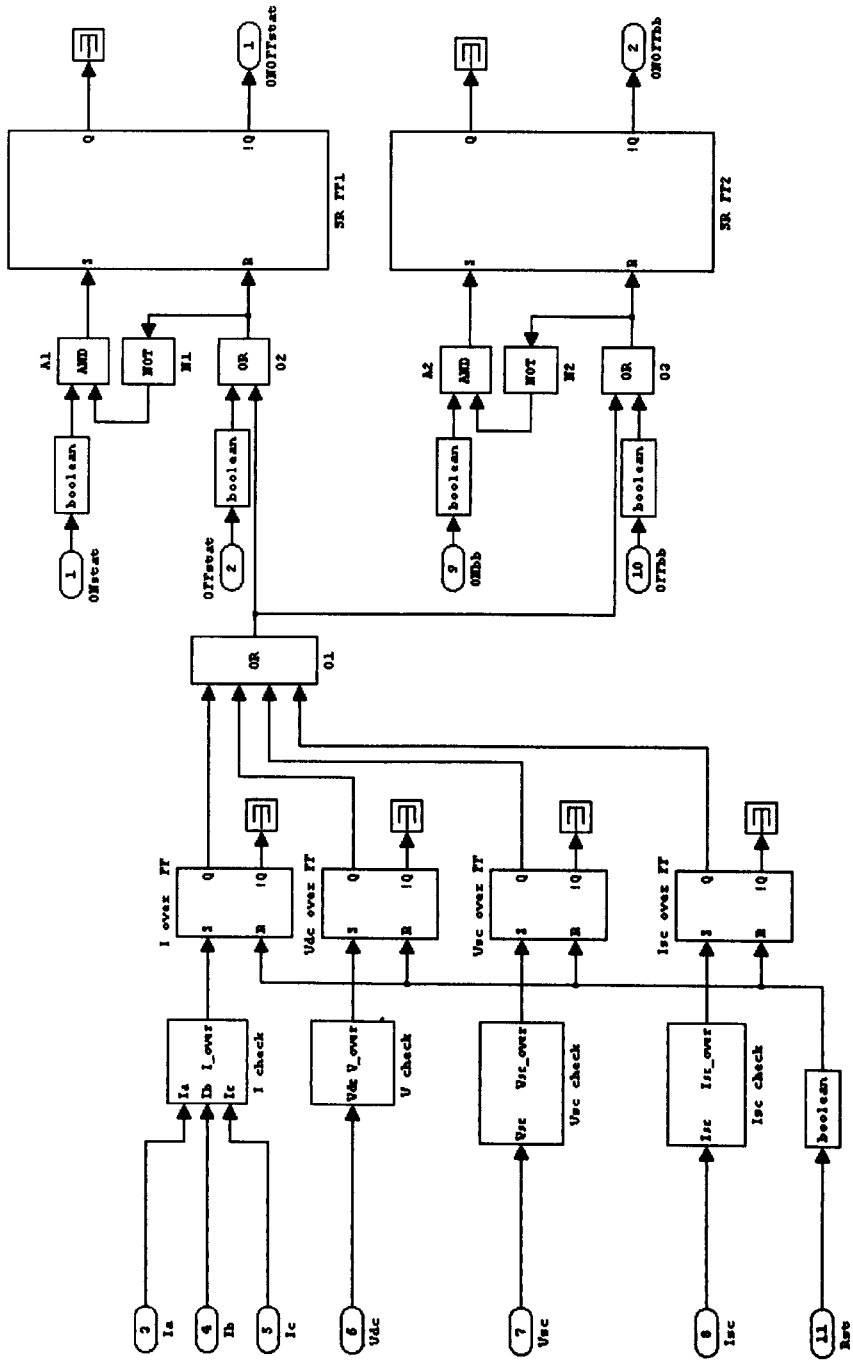

Figure E-27 'Protection' block

In the protection block, the STATCOM's current (I_a, I_b and I_c), the supercapacitor's current and voltage (I_{sc} and V_{sc}), and the DC-link voltage (V_{dc}) are checked by comparing them with the settling values. For example in the sub-block 'I check' shown in Figure E-28 if the STATCOM's current is higher than the maximum positive and negative settling values, the output logic will be "1" and using SR flip flop to hold the output logic indicating the STATCOM had been operated with unacceptable overcurrent condition (and should be stopped). This resulting output signal and the output signals from the other comparison blocks are further passed to SR FF1 in order to turn off the STATCOM and to SR FF2 in order to turn off the SCESS. Manual control by linking the ControlDesk software interface to input port '1' and '2' of SR FF1, and input port '9' and '10' of SR FF2, resulting that the STATCOM and the SCESS can also be stopped manually.

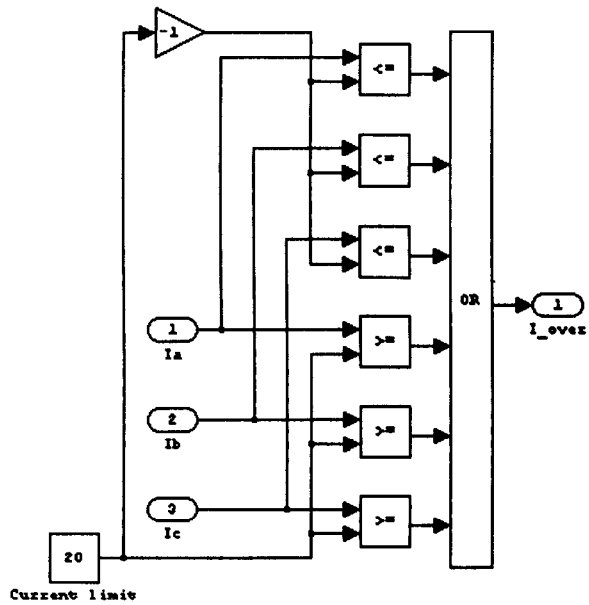

Figure E-28 'I check' block

Input port 11 is also linked to ControlDesk in order to provide reset signal 'Rst' to refresh the protection after the condition becomes normal and safe to re-operate.

In experimental tests, the resulting output logic 'ONOFFstat' is used as the stop logic for the functional built-in block named DS1104SL_DSP_PWM3 that is used to generate the three-phase PWM signals for the STATCOM. While the generation of the DCM signals for the SCESS using the built-in block named DS1104SL_DSP_PWM will be stopped by the output logic 'ONOFFbb', the SCESS control will also be disenabled by this output logic.

In simulation, the output signal 'ONOFFstat' is passed to input port 4 of 'statcom pwm' block (Figure E-20) to be used as the enable logic for the STATCOM PWM generation. The signal 'ONOFFbb' is used to enable or disenable the SCESS control - boost and buck controls shown in Figure E-16 and Figure E-18 respectively.

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