ASIC BASED RECORDERS OF ELECTROPHYSIOLOGICAL SIGNALS

by

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ABSTRACT

The ability of application specific integrated circuits (ASICs) to minimise the size and power consumption of electronic circuitry, makes their application to the design of ambulatory monitoring equipment, an attractive option. To this end, a multi-purpose mixed analogue and digital ASIC has been fabricated and incorporated into both a long-term recorder of adult heart rate (HR) and a recorder of electrophysiological signals.

The adult HR recorder has been employed in a study of long-term daily HR patterns, which verified the ambulatory nature of this instrument, as well as its suitability for investigating HR variability.

The electrophysiological signal recorder uses the ASIC to amplify, filter and digitise signals, which are then stored directly into static RAM. The analogue front-end of this instrument is flexible in terms of gain, bandwidth and sampling frequency allowing it be applied to a whole range of signals.

This instrument has been used to record the antepartum fetal HR, as part of the development of an ambulatory, ASIC based recorder of fetal HR (FHR). These recordings have shown that a usable signal can be obtained from a mother in her home environment, whilst in various postures.

The electrophysiological signal recorder has also been used to record the electrohysterogram (EHG), which is the name given to the electrical activity of the uterus, from abdominal electrodes during labour. A strong correlation was found to exist between tocographs derived from the EHG and tocographs produced by conventional means.

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CHAPTER 1

INTRODUCTION

1.1. Long term ambulatory recording.

Long term ambulatory recording allows important medical variables, such as blood pressure or heart rate (HR) to be monitored over several hours or days. These recordings may be made in various environments, such as the home or at work, and during diverse activities, such as sleep or exercise. The information provided by such recordings is often unobtainable from short term monitoring, both because of the reduction in data and the fact that such studies are generally undertaken in the arguably artificial environment of a hospital or laboratory.

Ambulatory monitoring can be performed on any physiological parameter that is of an electrical nature or that can easily be transduced into an electrical signal. Commonly monitored parameters include: arterial blood pressure, respiration, posture and the electrical activity of the heart, brain, eyes and muscle [Olson, 1978]. Three examples of ambulatory monitors are presented below. The first type of monitor records an electrical signal direct from the skin; whereas the other two monitors require some type of electrical transducer.

Holter monitoring is the ambulatory recording of the electrical activity of the heart and is named after N.J. Holter who first published this technique in 1961 [Holter, 1961]. These monitors continuously record two channels of the electrocardiogram (ECG), taken from chest electrodes, over a 24 hour period.

Ambulatory beat-to-beat arterial blood pressure can be monitored indirectly using the Volume Compensation Technique. This method detects the variation in arterial volume using a transmission infra-red photoelectric plethysmograph (TIPP), together with a pneumatic finger cuff which is controlled by a servosystem in order to maintain a constant arterial volume [Kawarada et al., 1991].

The automatic measurement of physical activity and posture can be achieved by attaching either accelerometers or inclinometers to various positions on the body [Tanaka et al., 1994]. Ambulatory posture monitoring is usually performed in conjunction with blood pressure monitoring because the latter is posture dependent. Recording of physical activity is also used together with Holter monitoring in order to investigate the heart's reaction to exercise [Meijer et al., 1989].

Traditionally data is stored onto a miniature tape, but in recent years solid state recorders have become possible due to the ever increasing capacity of this type of memory device, together with the availability of low power microprocessors, capable of performing real time data compression.

In designing ambulatory monitoring equipment, it is important to produce an instrument which is both unobtrusive and comfortable enough to be worn over many hours or days. Therefore any means of reducing the overall size and power consumption of such equipment would seem to be of value. The ability of Application Specific Integrated Circuits (ASICs) to minimise the size and power consumption of electronic circuitry, makes their application to the design of long term ambulatory monitoring equipment an attractive option. The ability of ASICs to incorporate an element of real time processing could also be useful in extending recording times.

This thesis is concerned with the application of ASICs to ambulatory monitoring, and in particular, the development of long term ambulatory recorders of electrophysiological signals.

1.2. Electrophysiological signals

Electrophysiological signals (also referred to as biopotentials or bioelectrical signals) are electrical signals produced by various parts of the normally functioning human, which appear on the surface of the body. It is possible to detect, amplify and record these signals with electronic instrumentation via cutaneous (skin) electrodes. Such instrumentation also usually incorporates an element of filtering which is required in order to suppress various types of noise and interference. The three most common types of noise and interference found in electrophysiological signals are baseline drift, muscle noise and 50 Hz interference. A more detailed description of these phenomena can be found in Appendix B.

Examples of electrophysiological signals include the electrocardiogram (ECG), electromyogram (EMG), electroencephalogram (EEG), electrooculogram (EOG) and electrogastrogram (EGG); all these signals are related to the operation of a particular part of the body i.e. heart, muscle, brain, eyes or stomach respectively. The normal operation of these organs can be investigated by analysing the related electrophysiological signal. This analysis has led to the use of electrophysiological signals as clinical tools in the detection and diagnosis of organ dysfunction.

1.3. Initial application areas of ASIC based ambulatory monitors

Initially two areas of study were chosen as vehicles for investigating the value of ASICs to ambulatory monitors: long term heart rate variability (HRV) and monitoring in obstetrics. As well as investigating the suitability of ASICs for

ambulatory monitors, it was intended that by targeting these particular application areas, this work would interface well with other research work within the Medical Electronics group at Nottingham [Herbert, 93], [Gibson, 93].

1.3.1. HRV studies

The standard method of collecting long-term HR data is to use a Holter monitor, but such systems are expensive in terms of both the price of the individual monitors and that of the analysing systems (both hardware and software). In addition, the suitability of these systems for producing accurate enough HR data for certain types of HRV studies has been questioned [Pinna et al., 1994]. This is because the requirement of Holter monitors to record two channels of raw ECG for 24 hours limits the sampling frequency that can be used (usually 128 Hz).

An instrument which just records HR should be able to increase both the accuracy of HR data obtained and the maximum record time. By designing the instrument such that recorded data can be downloaded to a general purpose PC, savings on the cost of analysing the data will also be made. However, it should be noted that recording just HR rather than the full ECG may limit the clinical use of such a recorder to subjects with predominantly normal ECGs. The ECG of cardiac patients generally contains many abnormal beats, which need to be eliminated before certain types of HRV analysis can be performed.

1.3.2. Monitoring in obstetrics

Work on the development of a portable fetal and maternal heart rate (FHR + MHR) recorder [Mohd Ali et al., 1993] had reached a stage where the basic idea had been shown to be feasible using discrete components. By integrating

as much of this design as possible onto an ASIC, it should be possible to produce a truly ambulatory version.

During the development of this instrument it became apparent that a similar device capable of recording uterine contractions from abdominal electrodes would also be of value in the area of obstetrical monitoring [Marque, private communication]. Such an instrument could be useful in monitoring for premature contractions antenatally, as well as providing a more convenient means of monitoring uterine activity during labour. (Obviously the latter application does not necessarily require the monitoring equipment to be ambulatory.)

Therefore it was proposed that the existing FHR recorder design be modified so that it could also be configured to record uterine activity from the electrohysterogram (EHG), which is the name given to uterine EMG signals recorded on the abdomen.

1.4. Initial recorder requirements

Two instruments were proposed: a long term recorder of adult HR for use in HRV studies and a general electrophysiological signal recorder for use in obstetrical monitoring. Although the primary application of the second instrument would be as a long term recorder of FHR, it would also be used as a means of investigating the potential for monitoring uterine activity from abdominal electrodes.

1.4.1. Adult HR recorder

The adult HR recorder would need to be capable of storing HR data with an accuracy acceptable for HRV studies over a 24 hour period. The recorded HR information would then be downloaded to a standard PC for further analysis. It

was hoped that by integrating as much of the circuitry as possible onto a single ASIC, a small instrument could be constructed, using simply the ASIC, RAM and a PC interface IC.

1.4.2. General electrophysiological signal recorder

By allowing the gain, bandwidth and sampling frequency of the existing FHR recorder design to be reconfigurable, a more general recorder would be realised. This flexibility would allow the instrument to be applied to many other electrophysiological signals, and in particular the recording of uterine activity from abdominal electrodes.

It was intended that ultimately a digital signal processor (DSP) would be used for the various real time processing procedures, such as extraction of FHR or detection of uterine contractions. After completion of the recording, data would need to be transferred to a standard PC for further analysis. The ASIC would thus be used for signal conditioning and digitising of the raw electrophysiological signal, as well as providing the glue-logic used in interfacing to the DSP. It was envisaged that such an instrument could be constructed using simply the ASIC, RAM, a DSP with external erasable programmable ROM (EPROM) and a PC interface IC.

Although the eventual aim is to produce a DSP based instrument, the initial instrument did not include a DSP. Instead raw electrophysiological signals were stored directly to RAM. This instrument was used to investigate the quality of raw signals obtainable using an ASIC based front end. Once downloaded to a PC these raw signals could be processed off-line. A collection of raw signal recordings will prove useful for developing algorithms which will eventually run in real time on the final DSP based instrument.

1.5 Initial ASIC design

Initially a multipurpose ASIC was proposed having two modes of operation. It was intended that these modes would be used as the basis for one of two different ambulatory recorder designs:

1) Adult HR recorder (mode 1)

2) General electrophysiological signal recorder (mode 2)

As much of the circuitry as possible was to be integrated on to the ASIC in order to keep the final instruments as small as possible. By including the circuitry for both modes on a single ASIC, two different designs could be tried out for the cost of one design run, with minimal increase in overall ASIC size. This is because much of the circuitry is common to both designs, in particular the analogue front end circuitry needed for signal conditioning and the digital circuitry for interfacing with the serial port of a PC.

1.5.1. Adult HR recorder (mode 1)

It was intended that all the circuitry required for an adult HR recorder with the exception of RAM and PC interface chip, could be included on the ASIC. This would consist of analogue signal conditioning and heart beat detection, followed by digital heart beat interval timing and RS-232 interface circuitry.

1.5.2. General electrophysiological signal recorder (mode 2)

In mode 2 an on-chip analogue to digital converter (ADC) placed after the analogue signal conditioning circuitry would be used to digitise raw electrophysiological signals before being either stored directly in off chip RAM, or processed in real time by a DSP.

In order that the instrument could be used to record many different electrophysiological signals it should be made as flexible as possible in terms of gain, bandwidth, sampling frequency and ADC resolution. This flexibility would allow the instrument to be used to record signals of differing amplitude and frequency content. The simplest way to achieve maximum gain and bandwidth flexibility is to use off chip resistors and capacitors. Although this philosophy would lead to an increase in ASIC input/output (I/O) pins, the improvement in programmability and hence flexibility of the recorder warranted this.

When configured with a DSP, responsibility for writing and reading from RAM, as well as interfacing with the serial port of the PC during downloading would, be transferred from the ASIC to the DSP.

The flexibility of the ASIC front-end, together with the programmability of the DSP, will produce a general recording instrument which could have numerous applications within the field of ambulatory monitoring. It would, in fact, be possible to use mode 2 to record adult heart instead of mode 1. However the argument for developing mode 1 is still strong, as a mode 2 DSP based adult heart rate recorder would have the disadvantages of increased size and complexity, power consumption, and a higher cost.

A DSP based mode 2 instrument would also be able to overcome the problem of using a mode 1 instrument on cardiac patients. This would require algorithms, running on the DSP, to either detect and remove abnormal beats from HR data, or to compress the full ECG sufficiently well that a higher sampling frequency (than 128 Hz) could be used.

1.6. Development strategy

A major drawback in using ASIC technology to implement new circuit ideas, is the risk factors involved in going straight to silicon with an unproven design. As well as the cost of resubmitting an erroneous design, there is the time penalty induced in turning round the corrected design. It takes at least a month and more often three, from submitting a design to receiving the fabricated chips. To reduce these risk factors, certain parts of the design were initially prototyped in order to prove their validity.

The digital logic used in the 24 hour adult HR recorder design was first prototyped with an Actel field programmable gate array (FPGA). A printed circuit board (PCB) was then built, containing the FPGA together with discrete ICs for the analogue circuitry, in order to prove the complete mode 1 design. Once the decision had been made to fabricate the ASIC design using the European Silicon Structures (ES2) 1.5 μm process via Solo1400 CAD tool (ES2 computer aided design software package), various other parts of the design were prototyped using ES2 sample chips. Important analogue sections of the design, such as a sample and hold circuit and a dual slope ADC were tried out, as the ability of Solo1400 software package to simulate analogue circuitry is very limited.

The time and effort spent in proving much of the design in this manner, increased the confidence in the design and the ability to get the ASIC circuitry right first time.

1.7. Structure of thesis

This thesis contains a total of 8 chapters together with several appendices, beginning with this chapter, which is a general introduction to the area of research.

An introduction to ASIC technology is presented in Chapter 2. This section briefly describes the advantages of using ASICs, together with the various types of ASICs that are currently available. Also included in this section is an introduction to FPGA technology, highlighting the relative merits of these devices in comparison to discrete ICs as well as more conventional mask ASICs.

Chapter 3 describes how the adult HR recorder design was prototyped by implementing all of the digital circuitry onto a single FPGA. Circuit diagrams of the FPGA based recorder are presented, together with a description of the instrument's operation. This is followed by a results section which includes HR recordings both at rest and during exercise.

The work involved in the design and realisation of a mixed analogue and digital ASIC for use in various long term ambulatory recorders of electrophysiological signals is contained in Chapter 4. Justification is given for selecting the ES2 foundry via the Solo1400 CAD tool, highlighting the importance of the Eurochip scheme in this decision. A description of the operation of the ASIC including the design of a dual slope integrating ADC is followed by a section on designing the ES2 ASIC using Solo1400.

In Chapter 5 the design of an ambulatory adult HR recorder based on the ES2 ASIC is described (mode 1). Details of the improvements made to the FPGA version, which have been incorporated into the ASIC based instrument, are presented. Results obtained with this instrument include long term recording of daily beat-to-beat HR, HR during sleep and HR during exercise. The 0.3 Hz component of HRV which is associated with respiration [Sayers, 1973] is shown to be present in several recordings of HR during sleep.

Chapter 6 is concerned with the development of the general electrophysiological signal recorder based upon the ES2 ASIC (mode 2). A description of the recorder's operation is presented together with various circuits and system diagrams. Examples of some of the 119 abdominal FECG recordings made with this instrument are included, together with a selection of FHR and MHR traces extracted from these raw signals using a PC based software package.

Results of an initial investigation into the feasibility of monitoring uterine activity from abdominal electrodes are presented in Chapter 7. The signals obtained for this study were produced by the general electrophysiological signal recorder when configured as an EHG recorder.

Conclusions are contained in Chapter 8 together with suggestions for further work. Finally several appendices are included, giving guidelines on the electrical safety requirements of battery powered medical equipment, the reduction of noise and 50 Hz interference in biopotential amplifiers, plus a full set of ASIC schematic diagrams.

CHAPTER 2

INTRODUCTION TO ASIC TECHNOLOGY

2.1. Introduction

This chapter provides a brief introduction to application specific integrated circuit (ASIC) technology, including the advantages of ASICs and a description of the various types of ASICs that are currently available. An introduction to field programmable gate array (FPGA) technology is also included, highlighting the relative merits of these devices, in comparison to discrete ICs, as well as more conventional mask ASICs.

An ASIC is produced by the integration of an electronic circuit on to a single custom IC. The first generation of custom ICs became available around 1960 and were fabricated using small scale integration (SSI). These SSI devices were limited to a few simple logic gates requiring of the order of 10 transistors. By 1970, reductions in the minimum feature size and increasing silicon areas led to medium scale integration (MSI). MSI devices contain in the region of 1,000 transistors, enough to realise more complex circuitry such as adders and counters. The first large scale integration (LSI) circuits appeared around 1980 and were capable of integrating more than 10,000 transistors onto a single IC. The latest level of integration is referred to as very large scale integration (VLSI) and strictly refers to ICs containing over 100,000 transistors. VLSI processes capable of sub-micron feature sizes have facilitated the integration of whole microcomputer processors, containing millions of transistors, on to a single IC. It has now become common practice to refer to any ASIC design which is realised using state-of-the-art custom IC techniques as a VLSI design, even if it contains far fewer than 100,000 transistors.

2.2. Advantages of ASICs

The advantages of applying VLSI technology to the design of a battery powered ambulatory recorder are a reduction in the overall size and power consumption of the instrument leading to a more portable design capable of longer recording times. ASIC technology can also lead to increased reliability, due to a reduction in the number of soldered joints and components needed. In addition, from a commercial viewpoint, a higher level of design security is achieved with an ASIC, since a VLSI design is virtually impossible to copy.

2.3. Custom IC design

A custom IC or ASIC is simply an IC designed for a specific application. This may be an exclusively digital or analogue IC or alternatively a mixed ASIC, which will contain both. ASICs can be designed using any of the following methods. Full custom design, as the name implies, means the designer has the option of designing the whole chip, down to the transistor level, exactly as required. The next level, standard cell design, presents the designer with a clean slice of silicon but provides standard cells (e.g. gates, flip-flops, counters, op-amps etc.) which can be automatically placed and routed (connected together) on the chip as required. Both of these levels of design complexity are used for analogue and digital design, and are characterised by long development times and high prototyping costs. One method of reducing prototyping costs involves the merging of designs to form a multi-project wafer (MPW) [Haskard, 1990]. This technique allows several different circuits to be implemented simultaneously on a single wafer, resulting in shared processing costs.

A less complex, and hence cheaper option is a gate array design. Here the designer has no input into the placing of gates on the IC, but is presented with a "sea" of universal logic gates, and has only to determine how these gates are

to be connected. Gate array design routes are at present only available for digital designs.

Until the late 1980s the cheapest route to a digital ASIC was via the use of a mask programmable gate array. The operation of these devices is determined by the final layer of the production mask which is provided by the designer. These mask programmable (gate array) ASICs are still available but since the late 1980s have had to face strong competition from field programmable digital ASICs or FPGAs as they are known.

2.4. Introduction to FPGA technology

FPGAs allow digital circuitry to be integrated onto a single device without the long time penalty incurred with mask programmable ASICs. With FPGAs, the chip is not only designed on a PC or workstation but then also "fabricated" (i.e. programmed) using a device similar to an Erasable Programmable Read Only Memory (EPROM) programmer, connected via a card to the computer [Weste and Eshraghian, 1993]. The programming is achieved via either fuses or memory cells. In addition to this, the relatively low cost of FPGAs at low volume, compared to mask programmable ASICs make them an excellent prototyping option.

At present FPGA performance is still below that of certain mask programmable ASICs which continue to have an advantage when any of high performance (high speed, lower power consumption), high gate density or large volume runs are required. At the moment, all the FPGA devices on the market are of a purely digital nature.

CHAPTER 3

ADULT HR RECORDER USING AN FPGA

3.1. Introduction

This chapter describes how the adult heart rate (HR) recorder design was prototyped by implementing all of the digital circuitry onto a single field programmable gate array (FPGA). Circuit diagrams of the FPGA based recorder are presented together with a description of the instrument's operation. This is followed by a results section which includes HR recordings both at rest and during exercise. The chapter begins by introducing the electrocardiogram (ECG), HR and commercially available instruments for measuring HR

3.1.1. The ECG

The ECG is the electrophysiological signal produced by the electrical activity of the heart, a small proportion of which propagates all the way to the surface of the body. This electrical activity results from a process of electrical depolarisation and repolarisation of the surface membrane of the cardiac muscle cells. Depolarisation begins in the sino atrial node of the right atrium and spreads via the A-V (atrial-ventricular) node through the A-V bundle to the ventricles. The normal ECG is composed of a P wave, a QRS complex and a T wave (Figure 3.1). The P wave is caused by the depolarisation of the atria, the QRS complex by the depolarisation of the ventricles and the T wave by the repolarisation of the ventricles.

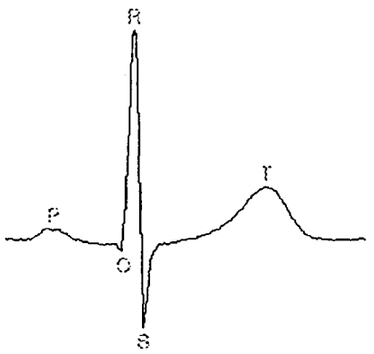


Figure 3.1: The Electrocardiogram.

Analysis of the ECG is a standard procedure in the diagnosis of myocardial infarction and other cardiac diseases such as electrical conduction defects [Guyton, 1991]. The size and shape of the ECG is heavily dependent upon electrode position. For diagnostic applications ECG recordings are made from a standard 12 lead configuration [Thakor, 1988]. Most lead configurations will give an ECG amplitude of between 1 and 5 mV (R-peak height), provided the electrodes are placed on either side of the heart. Thakor and Webster (1985) investigated the optimum electrode position of a single channel ECG in terms of maximising the signal (QRS complex) to noise (artefact) ratio (SNR) and suggested two possible pairs of locations (Figure 3.2); manubrium-left midclavicular / 7^{th} rib (1 and 2) and midsternum-left axillary / 9^{th} rib (3 and 4), both of which are thoracic equivalents of the standard Einthoven lead II. Maximising the ECG SNR is of particularly importance in Holter monitoring due to the increased physiological interference caused by patient movements.

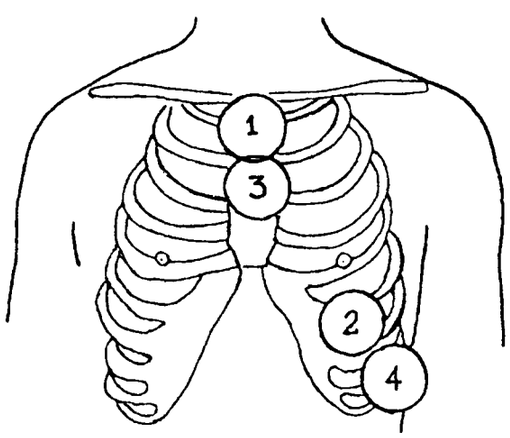


Figure 3.2: Optimum electrode positions for maximum ECG SNR [Thakor, 1984].

3.1.2. Heart rate

Instantaneous beat-to-beat HR in beats per minute (BPM) can be determined easily from the ECG as it is the reciprocal of the time interval in seconds between two successive heart beats multiplied by 60. The reference point for a heart beat is generally taken to be the peak of the R-wave as this is the most distinguishable component of an ECG.

3.1.2.1. Clinical importance of HR

Abnormal heart rhythms are known as cardiac arrhythmias. A fast HR (>100 BPM) is known as "tachycardia" and can be caused by increased body temperature, stimulation of the heart by the sympathetic nerves or toxic conditions of the heart. A slow heart rate (<60 BPM) is known as "bradycardia" and can be caused by stimulation of the parasympathetic nerves.

The amount of variability in beat-to-beat HR can be an indicator of the health of the heart. Decreased heart rate variability (HRV) can be a sign of severe coronary artery disease, heart failure, ageing or diabetic neuropathy [Kleiger et al., 1987], [Murray et al., 1975]. HRV, also known as sinus arrhythmia, can result from any one of many circulatory reflexes, or other nervous effects, that alter the strength of the sympathetic and parasympathetic nerve signals to the sinus node. Calculation of the P-P interval is the most direct method of investigating sinus arrhythmia. However, the relatively small P-wave can often be swamped by muscle noise, causing its detection to become unreliable. For this reason, the calculation of R-R interval is accepted as the standard method of investigating HRV. Any errors introduced by using R-R, rather than P-P interval tend to be minimal, as in general the P-R interval does not vary significantly from beat-to-beat [Kitney and Rompelman, 1987].

The study of HRV has also been shown to give information about various biological control functions of the body, such as respiration, thermoregulation and blood pressure [Sayers, 1973]. HRV has also been investigated as a predictor of long-term survival after Acute Myocardial Infarction (AMI) [Kleiger et al., 1987].

3.1.2.2. HR in sports and exercise

The measurement of HR has also been applied to the field of sport and exercise. In recent years it has become common for athletes to monitor HR during training sessions. This is particularly true of long distance runners, cyclists and swimmers who wish to increase their aerobic efficiency, by exercising at just below their anaerobic threshold. Conconi et al., (1982) demonstrated the relationship between HR, running speed and blood lactate levels in runners showing how anaerobic activity may be monitored noninvasively by measuring HR, although the results of this work have since been challenged [Trowbridge, 1992].

3.1.3. Commercially available HR monitors

The growing interest in measuring HR during exercise has lead to a large increase in commercially available HR monitors [Creative Health Products, commercial communication, 1991]. These instruments are usually worn on the wrist and display HR in BPM, with readings being updated approximately every 5 seconds. HR is obtained by either detecting the ECG in the chest or the hand area, or by detecting the pulse in the ear lobe or finger, using an infrared sensor [Creative Health Products, commercial communication, 1991]. The systems which detect the ECG from the chest area are the most accurate and reliable. This type of monitor detects the ECG using a chest band which contains two conductive electrode pads with a separation of around 150 mm. It

is recommended that these conductive pads are first wetted before the band is strapped horizontally around the chest, just below the nipples.

The HR information is either transmitted to the display using direct wires or with telemetry. A basic wrist watch style HR monitor can be purchased for less than £30. More advanced, and hence more expensive, monitors have the additional capability of storing HR at various intervals (5,30,60 secs), over several hours. Once the exercise session is complete the HR data can be downloaded via a computer interface to a PC for display and analysis. None of these sports orientated instruments either display or record HR on a beat-to-beat basis as athletes are not interested in HRV but rather in the underlying HR trends. Furthermore, it is desirable in sports applications, that HR readings remain constant for at least a couple of seconds, rather than being continuously updated.

Commercially available Holter monitors record 24 hours of continuous beat-to-beat HR. In these instruments R-R interval values are calculated digitally from ECG signals sampled at 128 Hz [Pinna et al., 1994]. This sampling frequency results in an R-R interval accuracy of +/- 3.9 ms, which relates to around +/- 0.25 BPM, at 60 BPM. This method is instantaneous, contains no averaging, and therefore does not smooth the results. The major disadvantage in using this method compared to averaging methods, is the increased amount of memory required to store HR continuously for 24 hours. Again, assuming an average HR of 60 BPM and an 8 bit R-R interval resolution, this would require 128 kbytes of RAM.

3.2. Description of FPGA based HR recorder

An Actel FPGA [Actel, 1993] designed using the Viewlogic computer aided design (CAD) package [Viewlogic, 1991], was used to prototype the digital

circuitry of the adult HR recorder design. This design measures continuous beat-to-beat HR by calculating the R-R interval of the ECG.

A block diagram of the FPGA based recorder is shown in Figure 3.3 which can be considered in two sections, namely analogue and digital. The analogue circuitry is used to detect the R-peak of the QRS complexes in the ECG, with the corresponding R-R intervals then timed and recorded by the digital section. This data, stored in static RAM (SRAM), can then be subsequently downloaded to a PC, via its serial port, over an RS-232 interface, for display and analysis. The analogue and digital circuits will now be described in more detail.

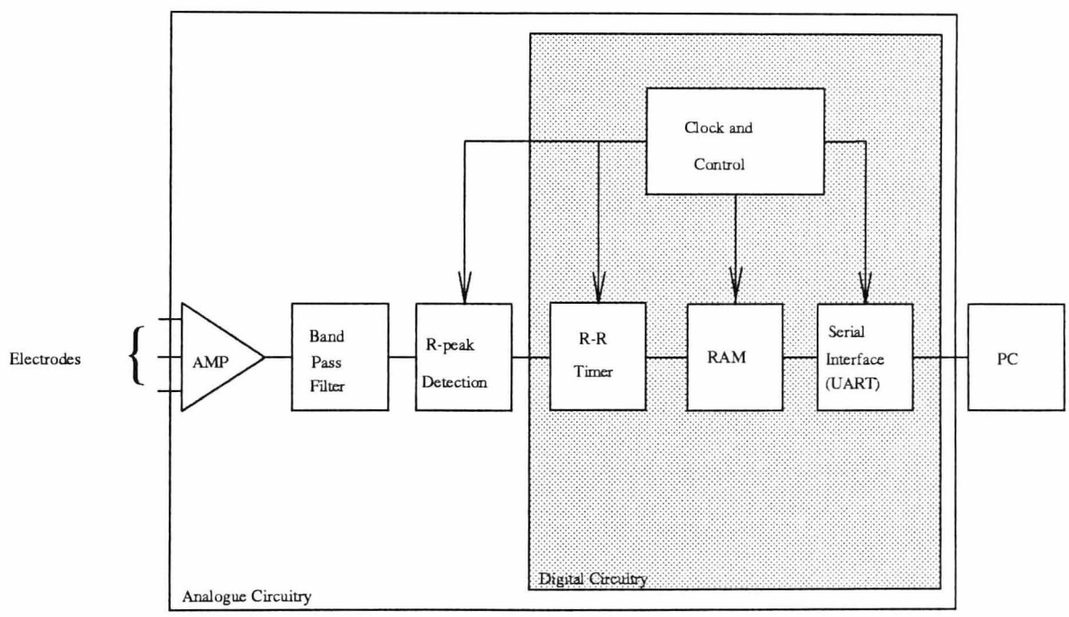


Figure 3.3: FPGA based HR recorder block diagram.

3.2.1. Analogue front end circuitry

Figure 3.4 shows the analogue front end of the instrument. Two chest electrodes are used to detect the ECG which is amplified and band-pass filtered to reject baseline drift, 50 Hz interference and high frequency noise. R-peaks are then detected via an adaptive thresholding technique, in which the incoming signal is compared with approximately 70% of the last R-peak value. The

reference voltage used is obtained by sampling and holding the ECG signal, at a fixed time interval after the R-peak. This results in a reference signal being stored of about 70% of the last R-peak, which can then be used to threshold the incoming signal, and so determine the next R wave occurrence. This technique will result in a maximum error of around 4 ms, if the R-peak amplitude changes dramatically between successive beats. However, given that the R wave amplitude is usually constant, the error in the R-R interval will typically be about 1 ms. The comparator used to compare the threshold with the incoming signal serves to produce a pulse. This pulse is then used as the input to the digital circuitry, that is activated on the positive edge. Both the input ECG and the resulting output from the comparator are shown in Figure 3.5.

3.2.2. Digital FPGA circuitry

The R-R interval timer logic calculates the time between successive R-peaks and stores this value into a 128K by 8 bit SRAM. This is achieved by simply counting the number of system clock cycles within each R-R interval. The count is performed in two stages: firstly, a fixed period (i.e. a set number of clock cycles are counted) and secondly, the time between the end of this fixed period and the next R-wave (main count). It is the latter that is stored in memory. This technique allows a smaller counter to be used without compromising accuracy. The sequence of events are shown as a timing diagram in Figure 3.6 and the corresponding digital circuitry is shown in Figure 3.7. During the fixed count the previous variable count value is written to RAM and the main count is reset to zero.

A clock frequency of 2.4 kHz is used with the fixed count comprising 384 clock cycles (160 ms). A 14 bit counter is used to record the second variable count, giving a (theoretical) range of R-R intervals from 160 ms (i.e. a count of

zero) to 7 s, with a resolution of 0.42 ms (although this does not fix the overall accuracy of the recorder which will be primarily dependent on the analogue processing as described earlier). R-R intervals of 7 s are obviously not expected, but allowing for such values means the failure to detect several R-waves within otherwise valid data becomes clear upon inspection of the record. The R-R-interval data is stored in 16 bit memory as two bytes. The two bits not holding the count are used as timing and event markers.

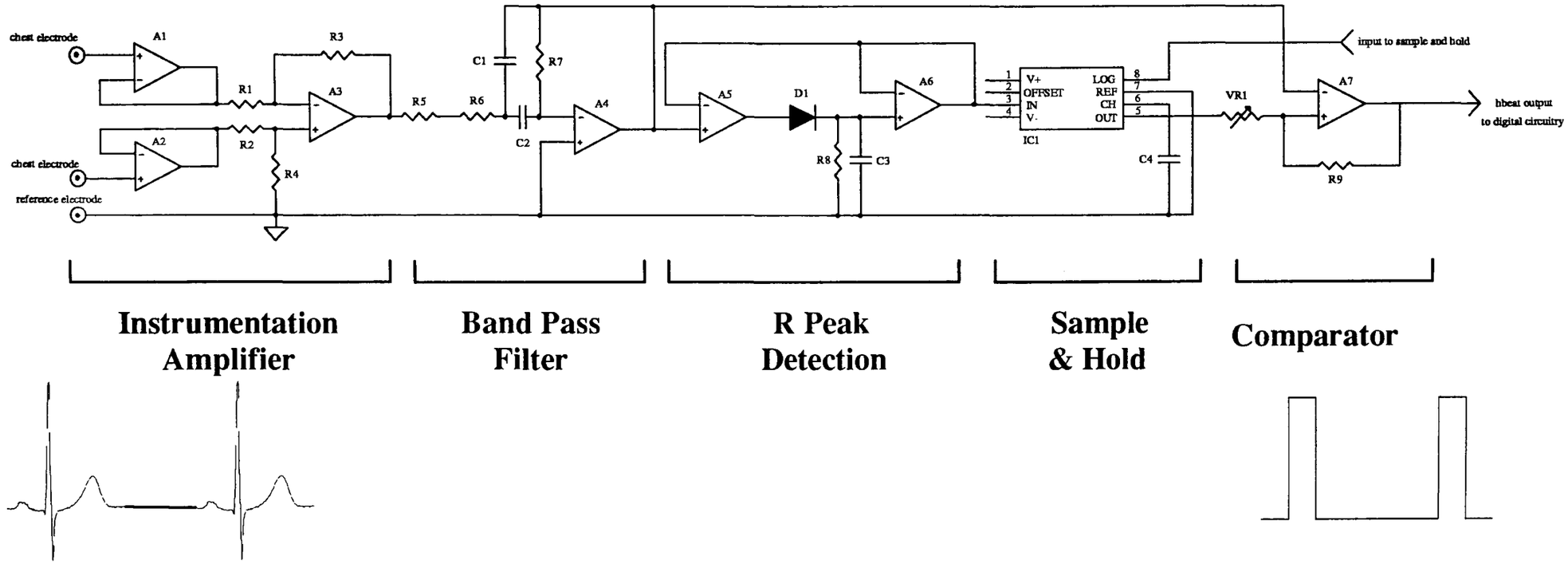
Since the pulses produced by the analogue circuit are asynchronous with the system clock, the first task is to achieve synchronisation, hence a heart beat synchroniser is shown in Figure 3.7. This signal is then used to stop the main 14 bit count and load a "1" into the 6 bit shift register. This shift register is clocked by the system clock, divided down by 64, during the 160 ms of the fixed count. The 6 outputs from this shift register, (Q0-Q5) which sequentially go high, are passed to a combinational logic circuit whose outputs are used to control:-

1. The resetting of the shift register input to zero and writing the high byte of the count to RAM
2. Incrementing of the RAM address
3. Writing the low byte (containing the remaining 6 bits of the count plus timing and event markers) to RAM.
4. Incrementing the RAM address and activating the sample and hold circuit used to record the R-peak amplitude.
5. Resetting the main 14 bit counter.
6. Halting the fixed count and initiating the variable main count.

The 14 bit output of the main count is tagged with time and event markers. If the event button has been pressed during the previous R-R interval a '1' is

latched into the 16th bit of the R-R interval count. Similarly a time marker is latched into the 15th bit every 14.56 minutes (2^{21} clock cycles).

Every time an R-peak is detected 14 bits of R-R interval data plus two bits for time and event markers are stored in two bytes of a 128 K x 8 bit SRAM. This memory capacity will allow almost 18 hours of continuous R-R data to be stored given an average heart rate of 60 BPM. Once recording is completed the stored data is transferred from SRAM to a PC for further analysis. This is achieved by reading in parallel R-R data from the SRAM to the FPGA, one byte at a time, converting it from parallel to serial RS-232 format, and then transmitting it serially to a PC via a MAX232 driver. This downloading process is controlled by a C program running on the PC. When the PC is ready to receive data the Data Terminal Ready (DTR) pin of the serial port is toggled and the FPGA begins transmitting data. Once all the data has been transmitted the information is saved on the hard disk of the PC for further analysis.



Component values:	R1,R2 = 4K7	R3,R4 = 620K	R5 = 10K	R6 = 6K9
(all resistors < 5 % tolerance)	R7 = 330K	R8 = 300K	R9= 500K	VR1 = 500K
(all capacitors polyester 10 % tolerance)	C1,C2,C4 = 0.1µF	C3 = 1µF		
	D1 = UF4001	IC1= NE5537	A1-7 = TL071	Power supply +/- 5 V

Figure 3.4: Analogue front end circuitry.

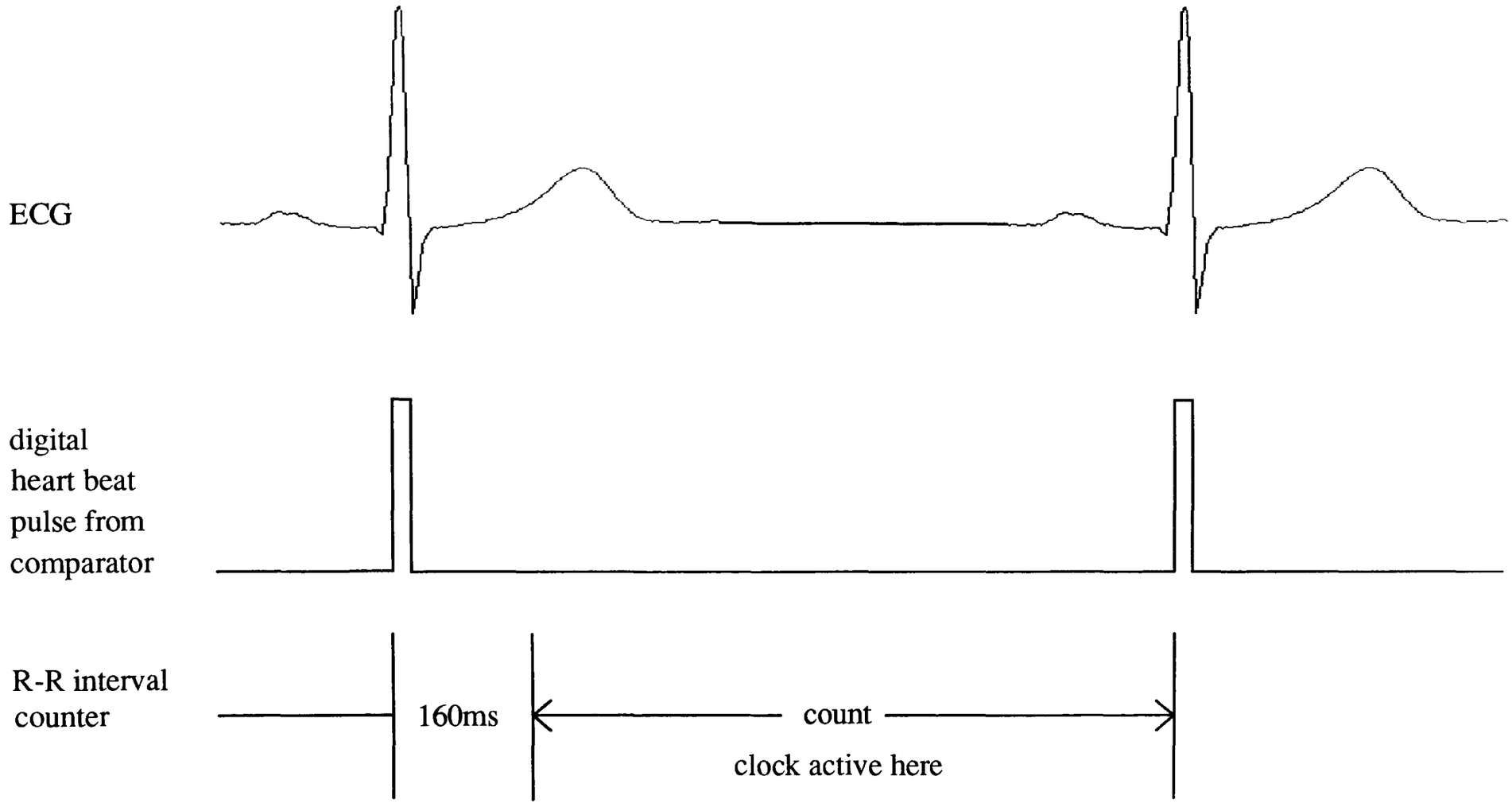


Figure 3.5: Two stages of the R-R interval count.

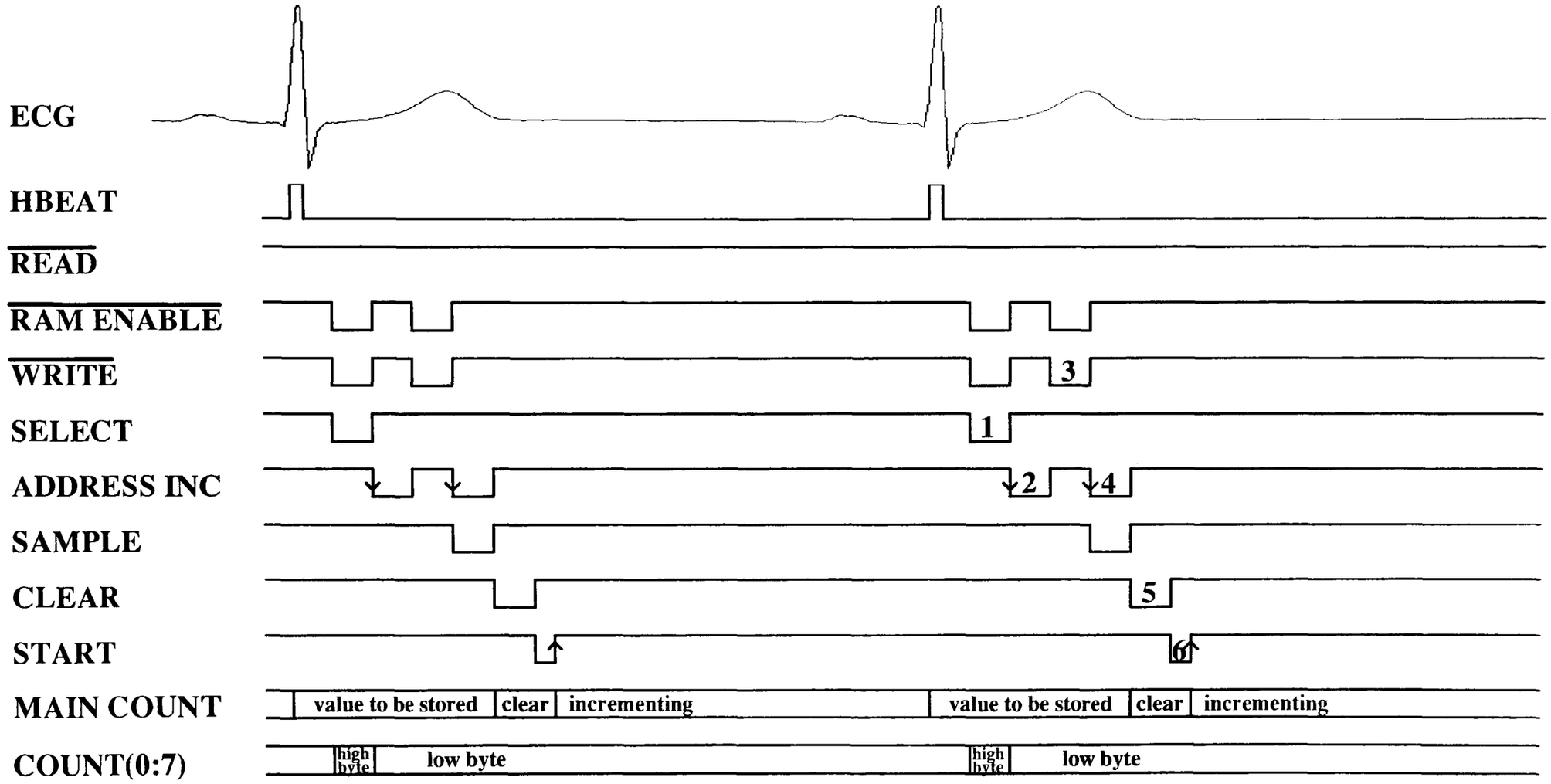


Figure 3.6: Timing diagram of R-R interval counter and interface to RAM.

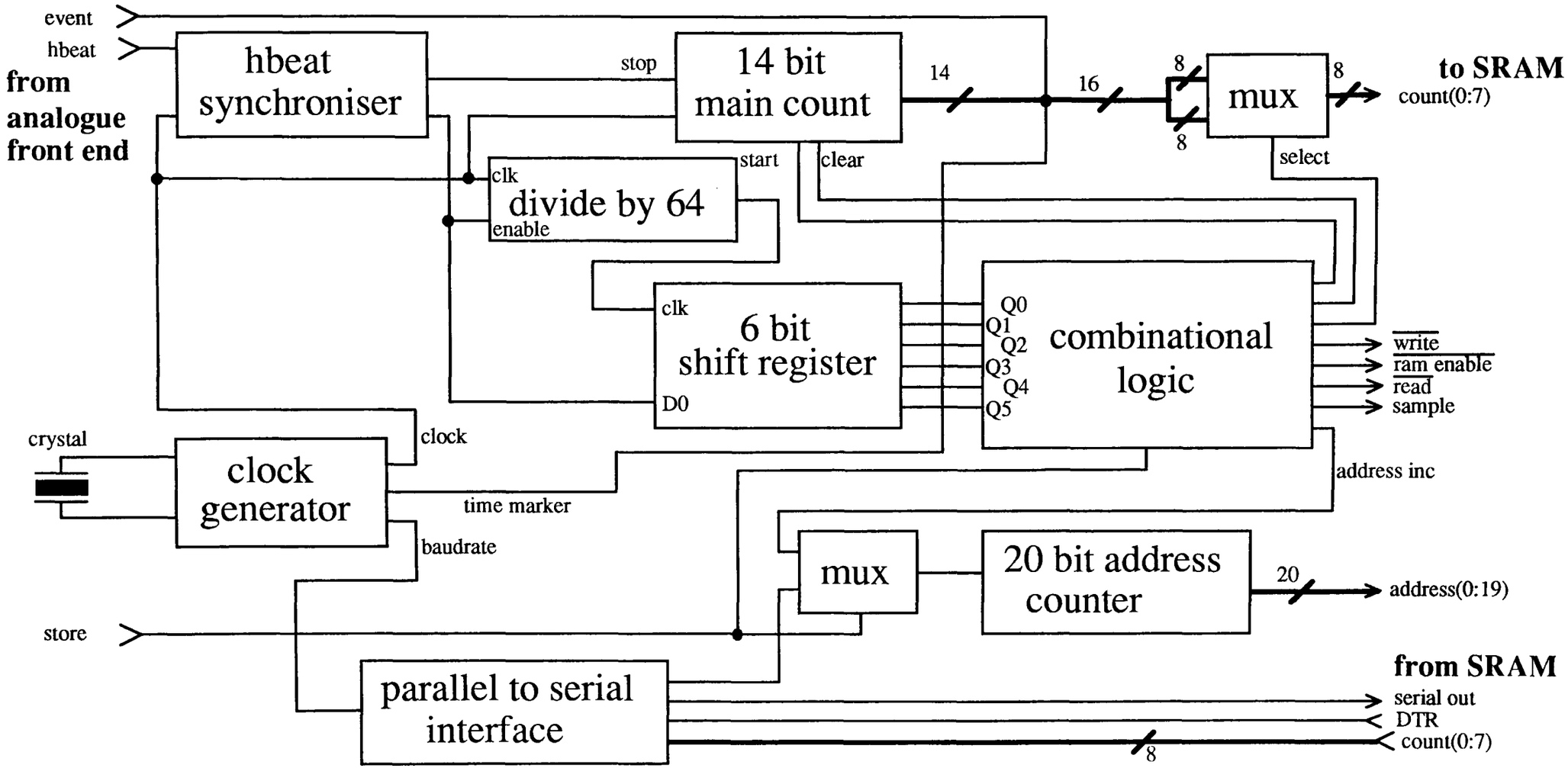


Figure 3.7: Digital FPGA circuitry.

3.3. Results

The FPGA based prototype of the adult HR recorder (see photograph in Appendix D) was used to record the HR of five different individuals (four males and one female aged 21 to 25). Each recording covers between 1 and 2 hours of the subject's typical daily working routine, which consists mainly of sitting at a computer terminal. Three disposable, foam-backed, silver-silver chloride, pre-gelled electrodes were used in all the HR recordings. Before attaching the electrodes, the subject's skin was prepared with an alcohol saturated swab and left to dry for around 5 minutes. The two differential input electrodes were positioned on the subject's chest as recommended by Thakor and Webster [Thakor and Webster, 1985]. The third 'common' electrode was placed on the subject's wrist. Extracts from the five recordings are shown below in Figures 3.8 to 3.12. In each case 4000 successive R-R intervals are displayed as beat-to-beat HR (in BPM) against beatnumber. Beatnumber can be converted into a true time axis by simply summing all the previous R-R intervals. However, problems can arise if the recording contains several successive missed beats or false detections leading to an apparent R-R interval which is less than 160 ms or greater than 7 s.

The five recordings shown below contain a total of four missed beats and no false detections. This consists of two missed beats in Figure 3.9 and one missed beat in both Figures 3.10 and 3.11. A single missed beat will cause the HR to halve and is therefore easily detected in HR data which has been calculated on a beat-to-beat basis. A single false detection will result in successive HR values which will have an average value that is twice the underlying HR. These errors can be corrected at the expense of beat-to-beat information (in the case of missed beats). Such corrections would be much more difficult to achieve if the HR data had been calculated using some element of averaging. Figures 3.13 to

3.22 contain the HR data from the same five recordings displayed on a variety of beatnumber scales.

An example of a beat-to-beat HR trace during exercise is given in Figure 3.23. HR was recorded as the subject ran up 15 flights of stairs from the ground floor, stopped, caught the lift back to the 7^{th} floor and then sat down to recover. The HR trace shows much variability in the form of accelerations and decelerations as the subject walked to the bottom of the stairs. As the subject begins to run up the stairs the HR accelerates sharply from around 80 BPM to 160 BPM and then slowly to a maximum of around 170 BPM. During this period the amount of variability in the HR is substantially reduced. Once the top of the stairs is reached, the HR begins to recover and more variability begins to appear in the HR trace. This reduction of HRV with exercise is a well known phenomena [Baselli et al., 1991].

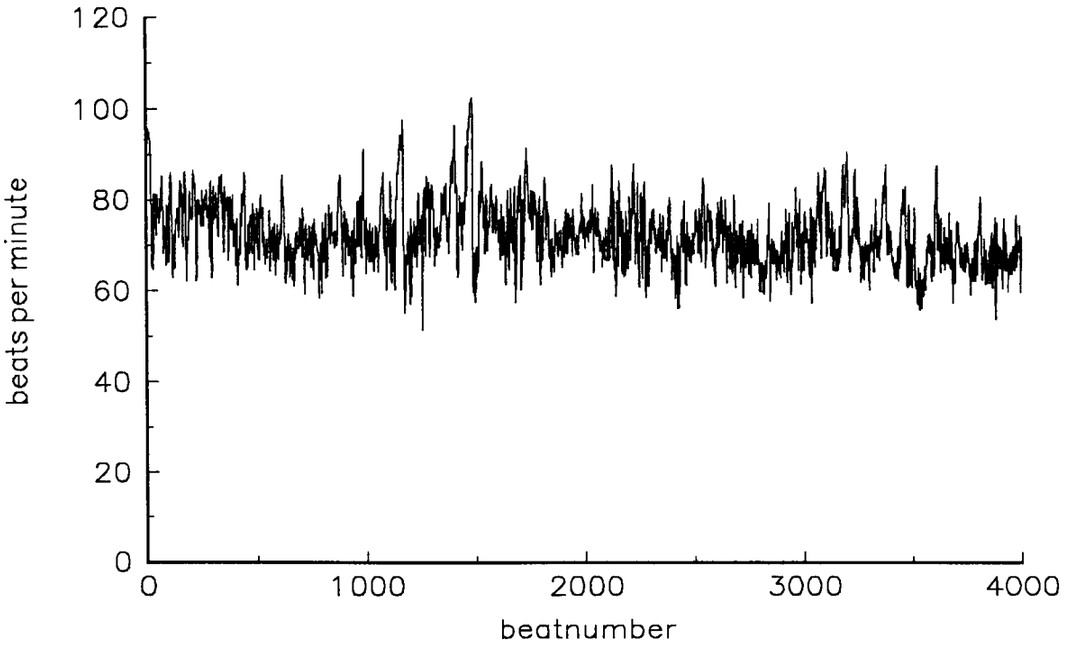


Figure 3.8: 4000 consecutive beat-to-beat HR values of subject A working at a PC.

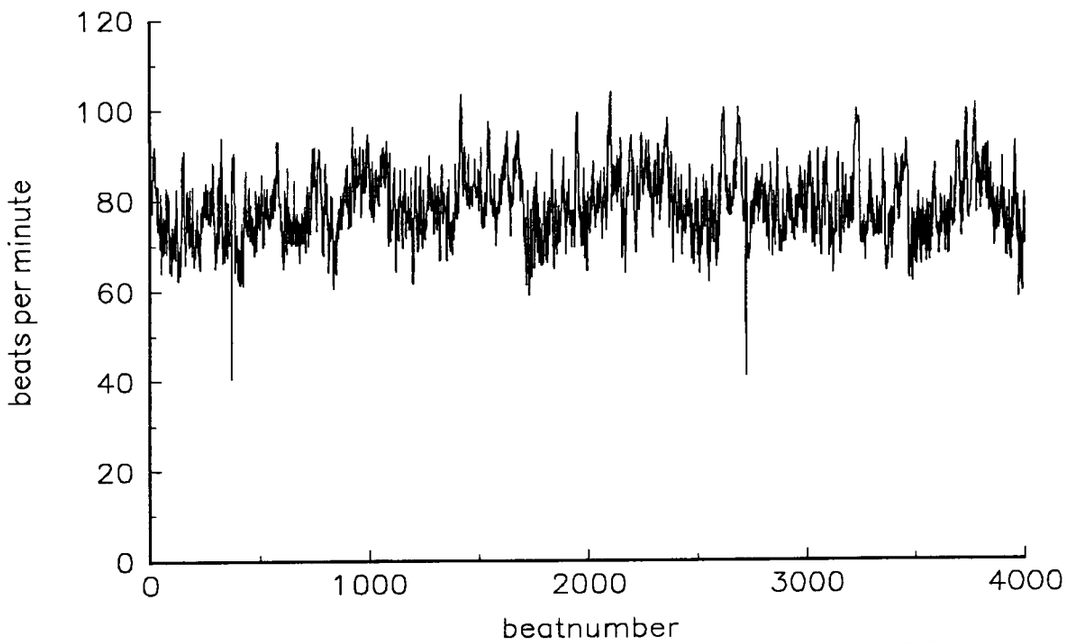


Figure 3.9: 4000 consecutive beat-to-beat HR values of subject B working at a PC.

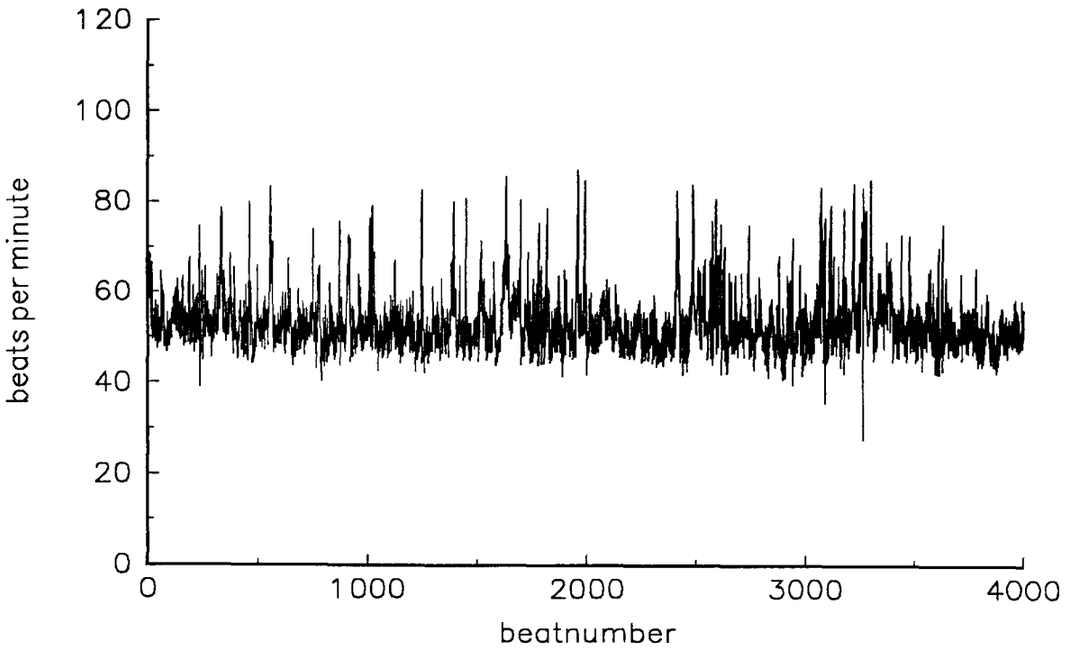


Figure 3.10: 4000 consecutive beat-to-beat HR values of subject C working at a PC.

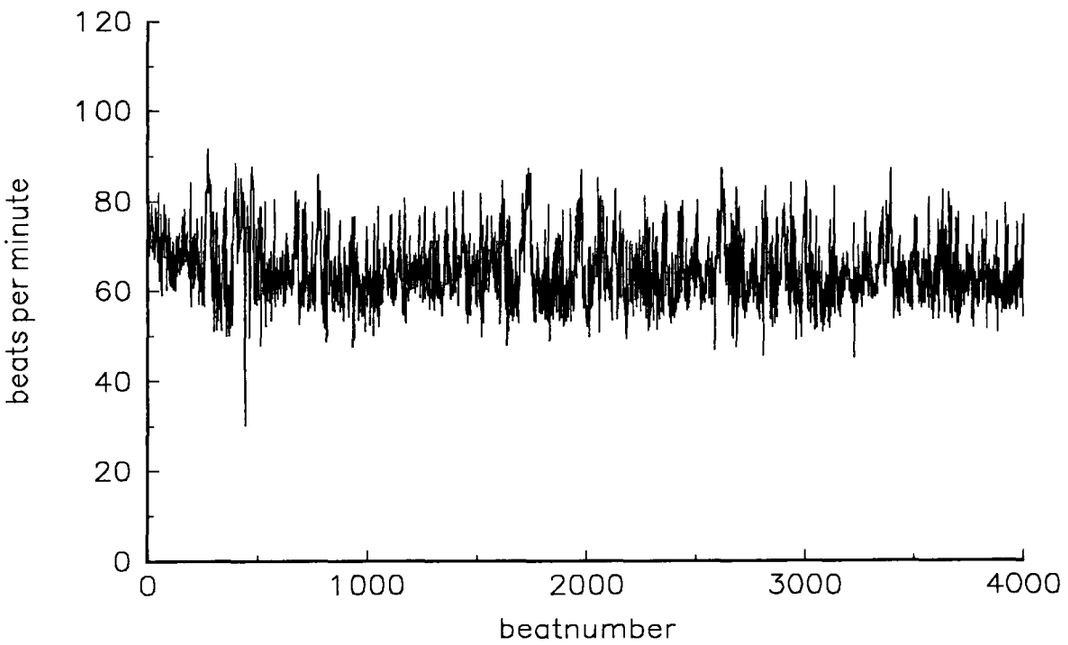


Figure 3.11: 4000 consecutive beat-to-beat HR values of subject D working at a PC.

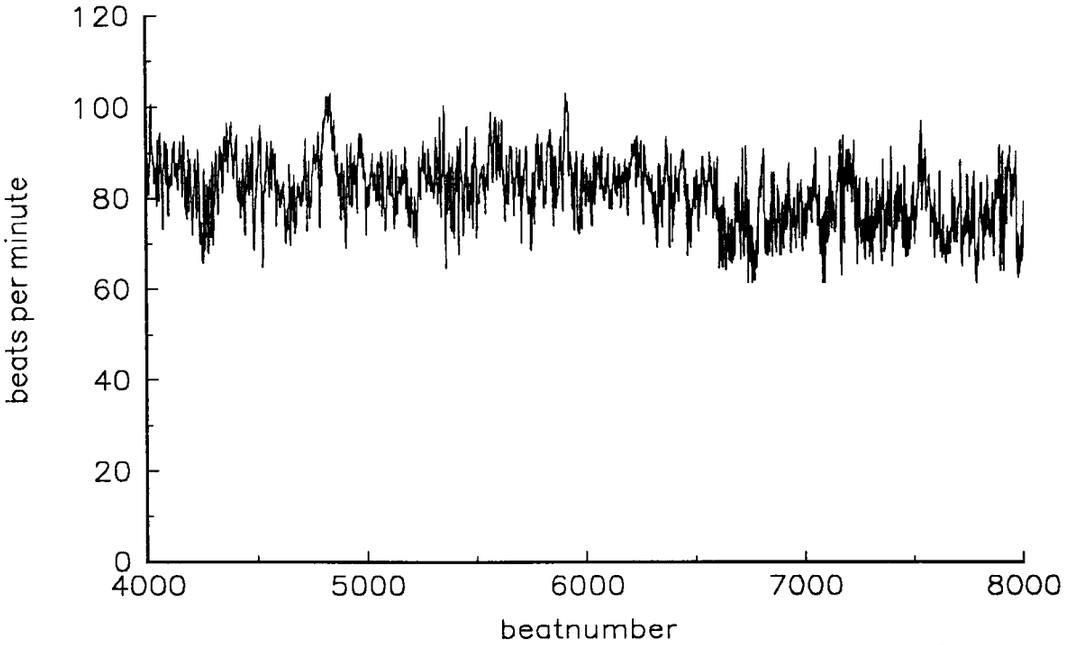


Figure 3.12: 4000 consecutive beat-to-beat HR values of subject E working at a PC.

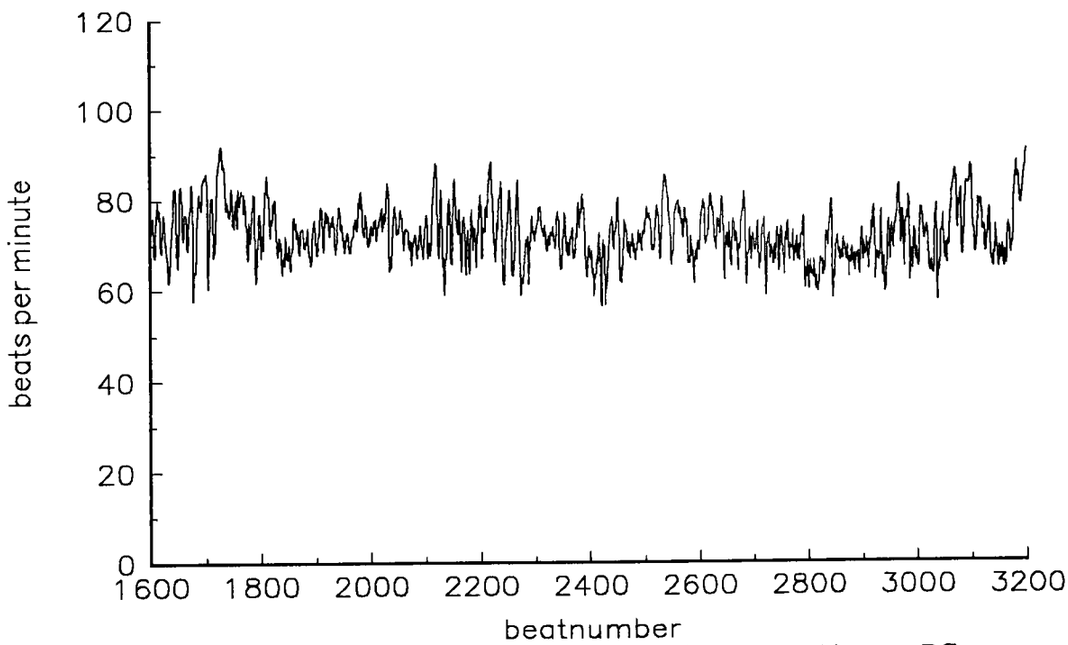


Figure 3.13: 1600 consecutive beat-to-beat HR values of subject A working at a PC.

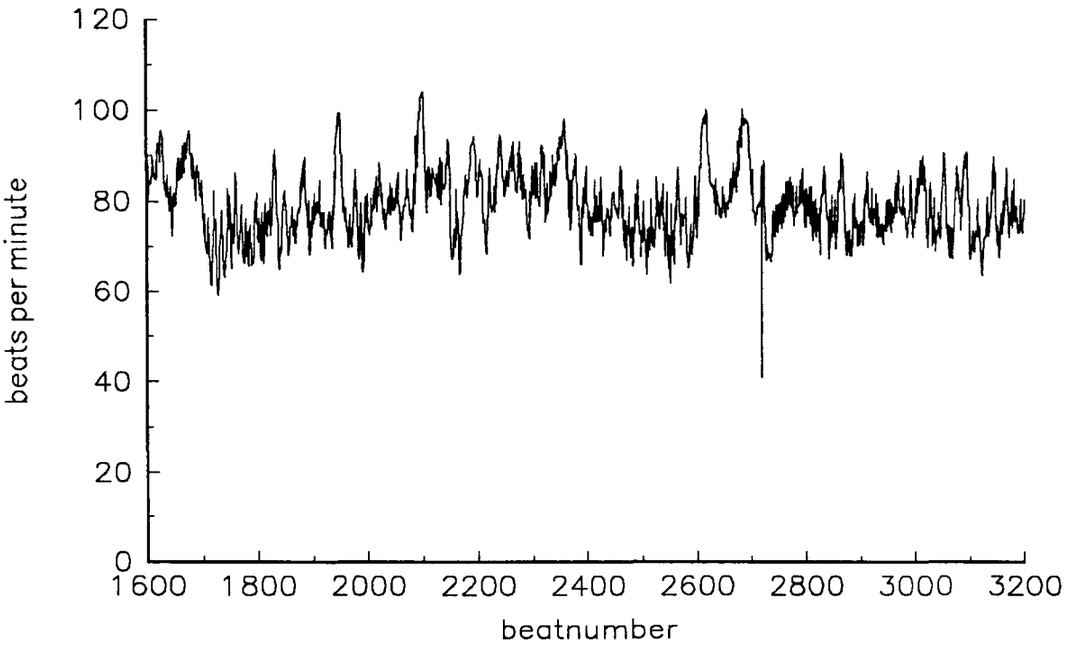


Figure 3.14: 1600 consecutive beat-to-beat HR values of subject B working at a PC.

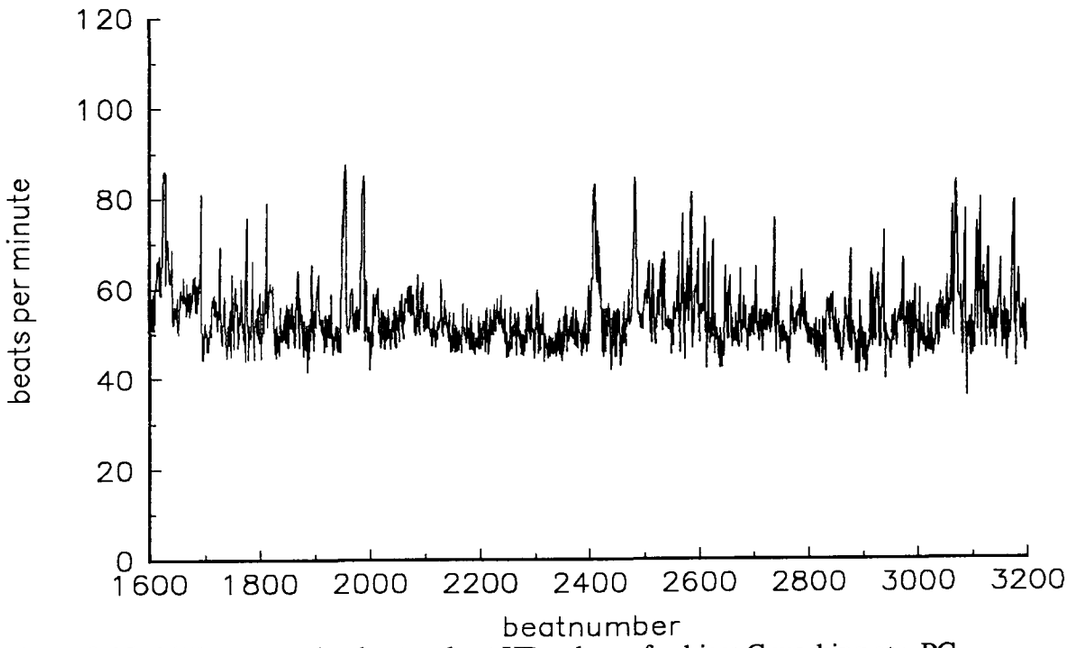


Figure 3.15: 1600 consecutive beat-to-beat HR values of subject C working at a PC.

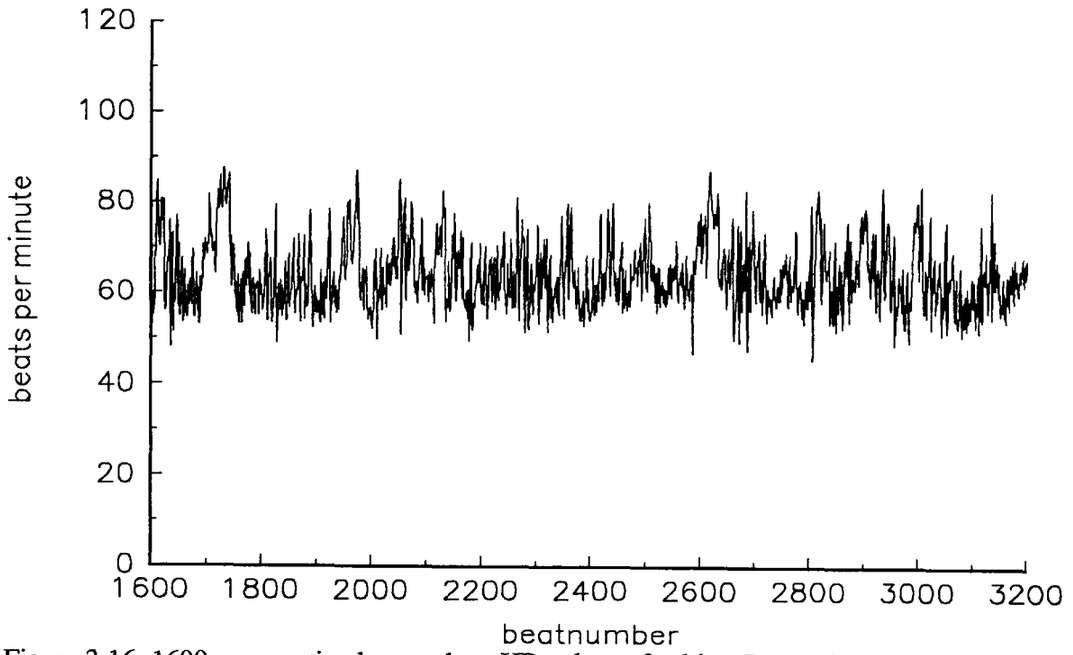


Figure 3.16: 1600 consecutive beat-to-beat HR values of subject D working at a PC.

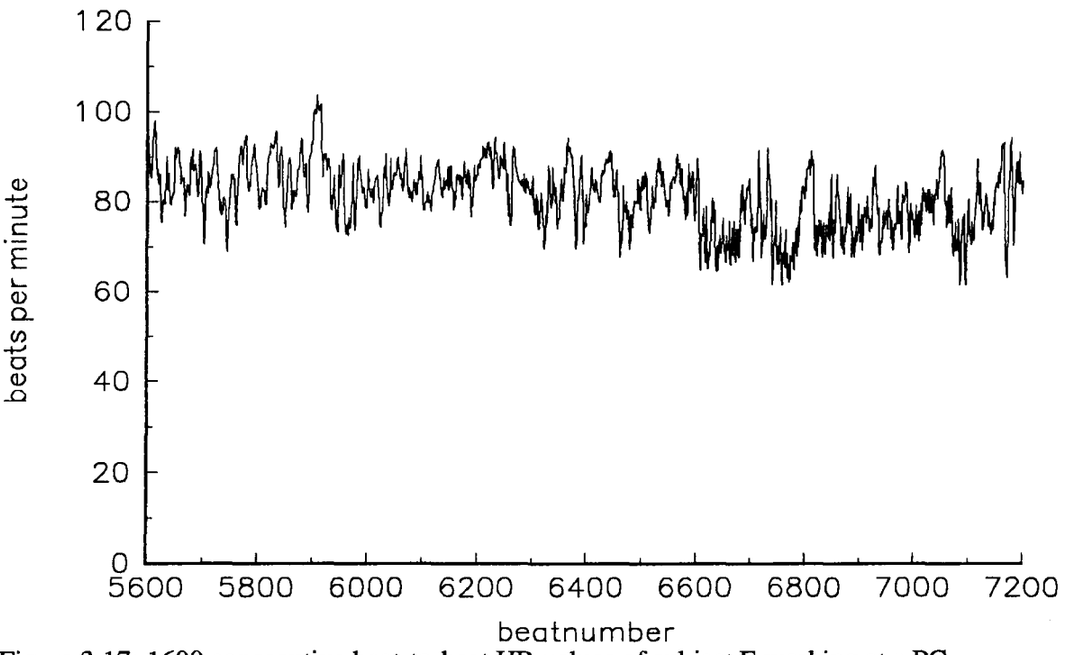


Figure 3.17: 1600 consecutive beat-to-beat HR values of subject E working at a PC.

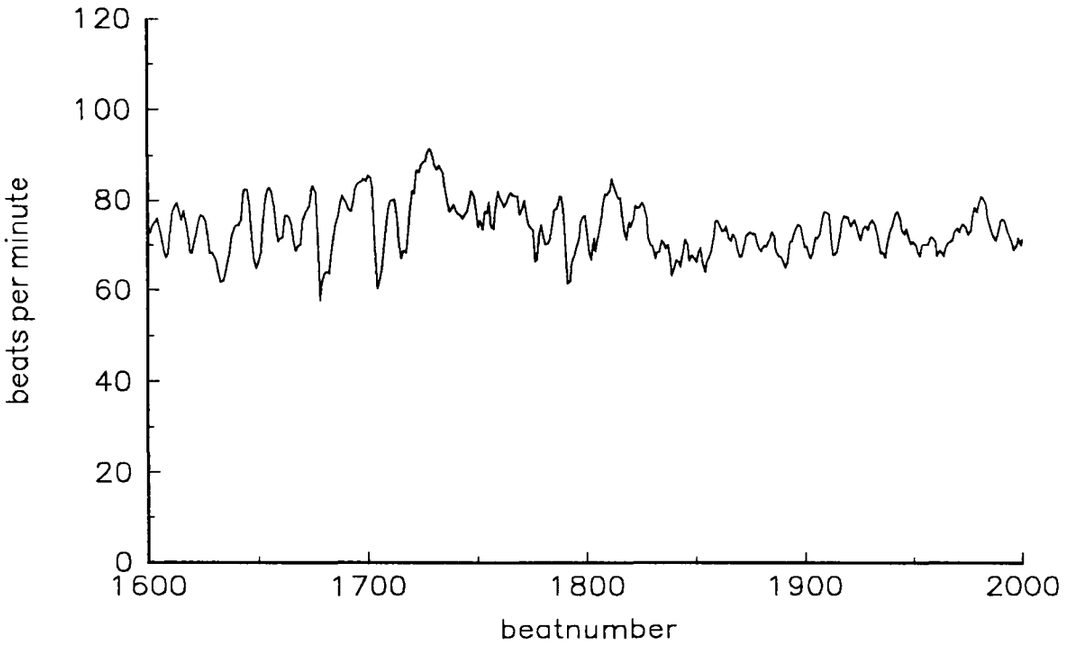


Figure 3.18: 400 consecutive beat-to-beat HR values of subject A working at a PC.

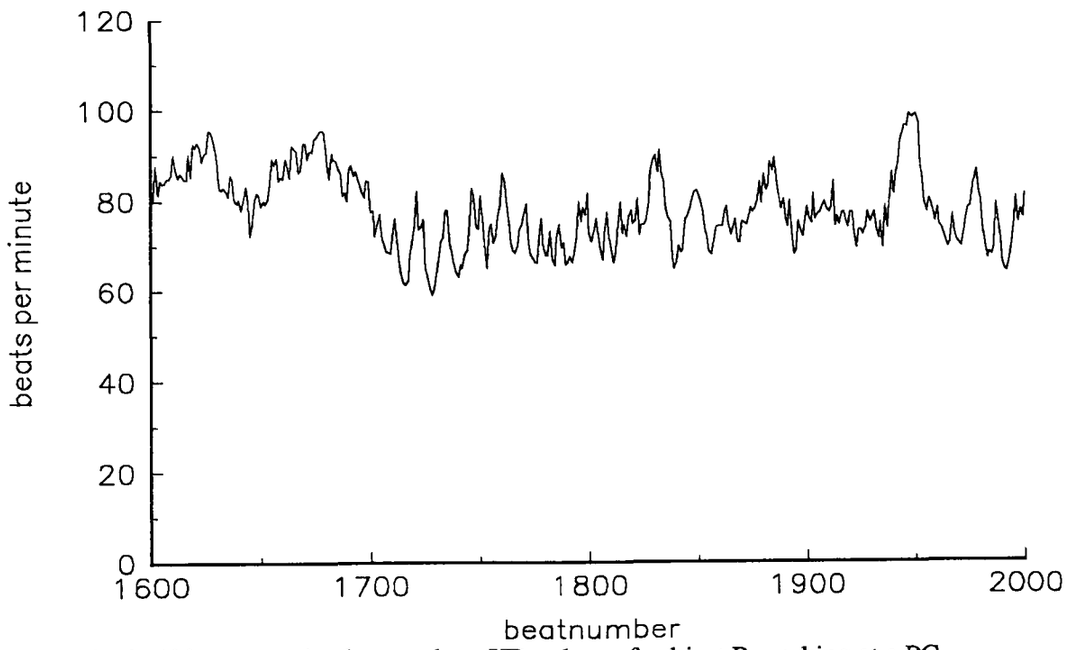


Figure 3.19: 400 consecutive beat-to-beat HR values of subject B working at a PC.

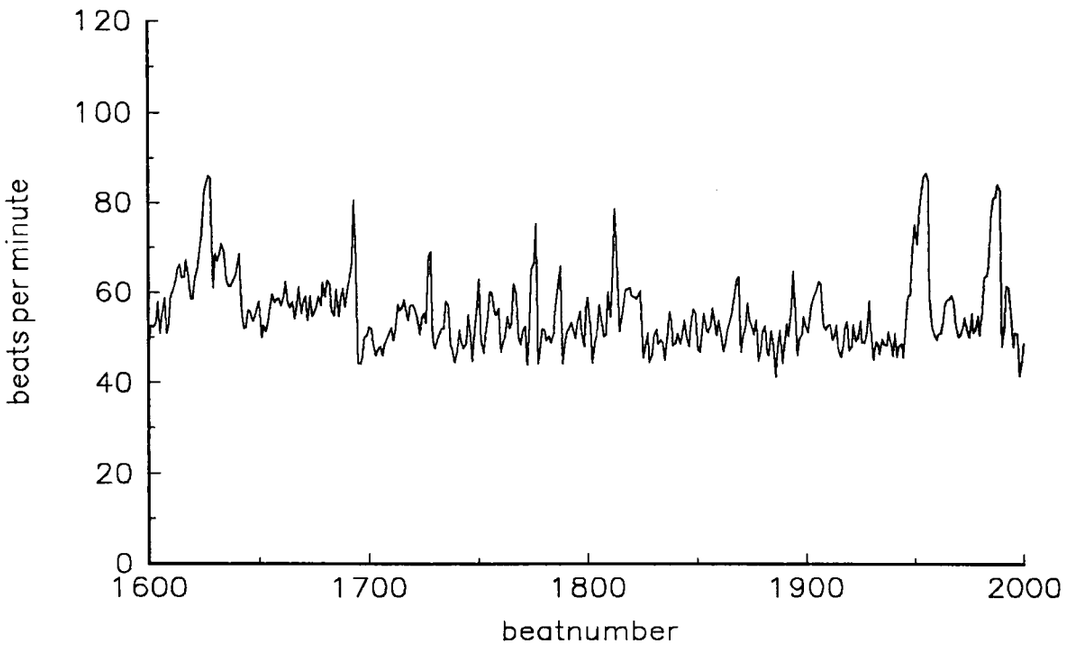


Figure 3.20: 400 consecutive beat-to-beat HR values of subject C working at a PC.

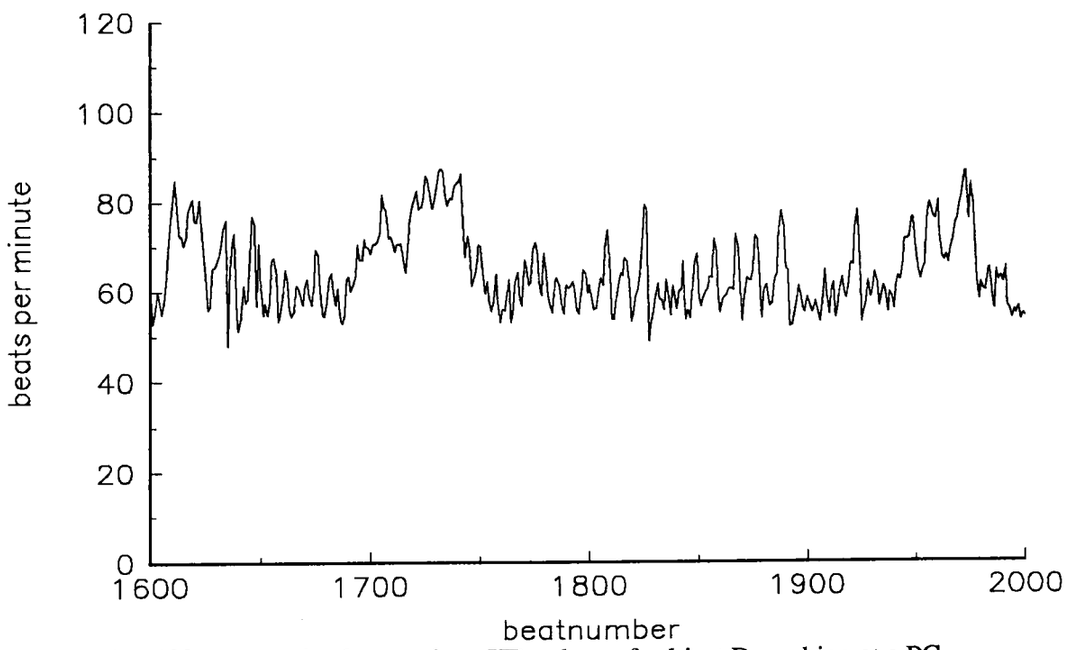


Figure 3.21: 400 consecutive beat-to-beat HR values of subject D working at a PC.

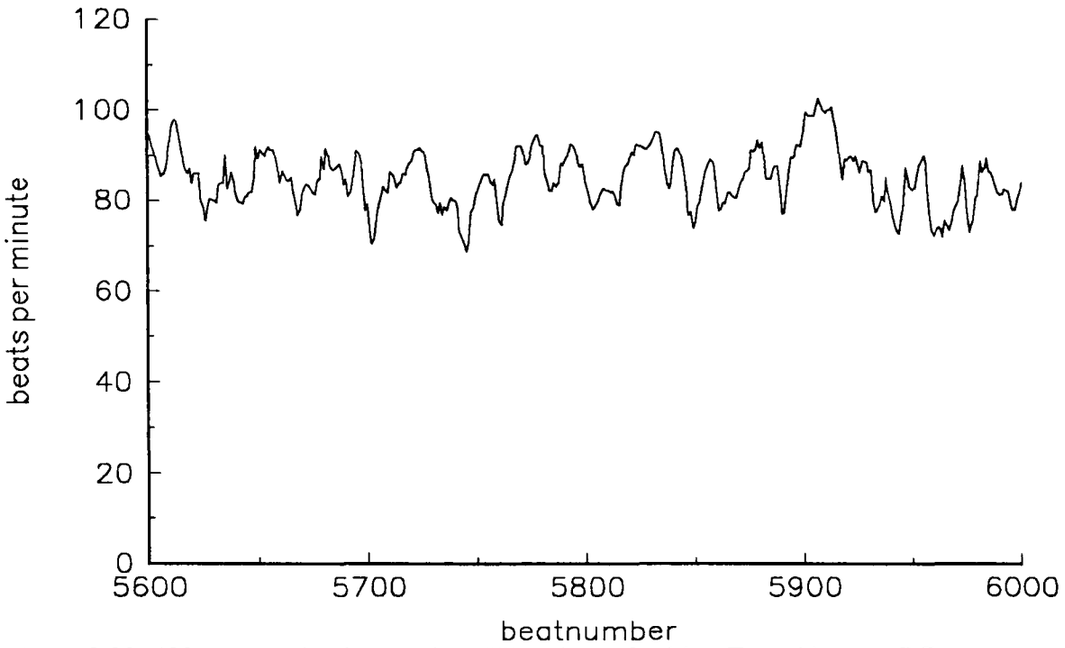


Figure 3.22: 400 consecutive beat-to-beat HR values of subject E working at a PC.

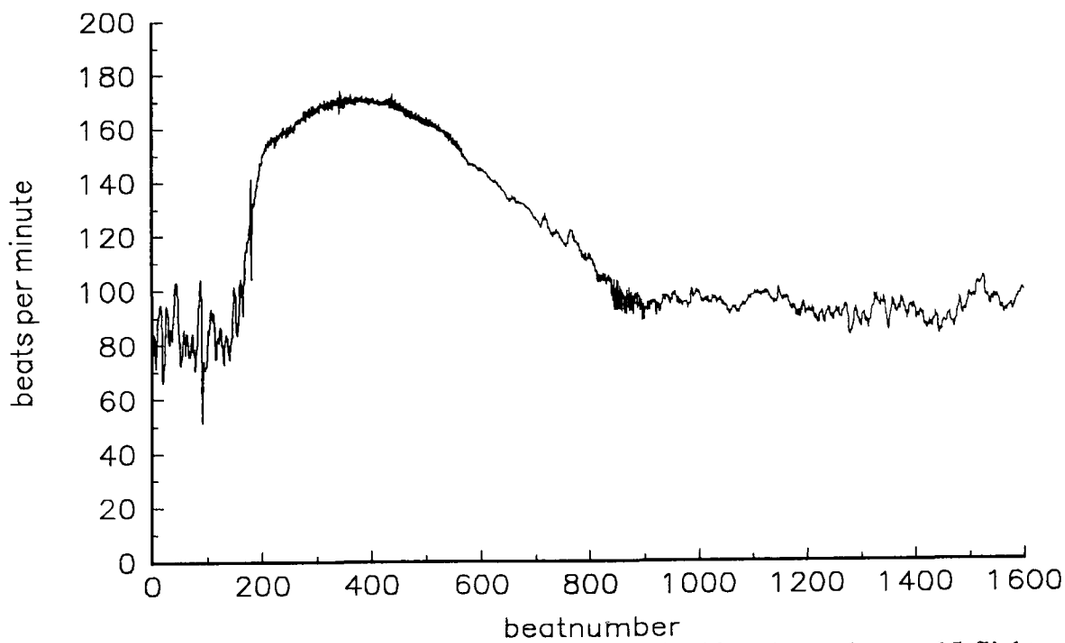


Figure 3.23: 1600 consecutive beat-to-beat HR values of subject A running up 15 flights of stairs.

3.4. Conclusions

The digital circuitry of the Adult HR recorder was successfully implemented using an Actel FPGA. This proved to be a neat and cost effective method of verifying the HR recorder design. The ability of the FPGA to integrate a large proportion of the circuitry onto a single device facilitated the development of a usable FPGA based prototype. This working prototype was used to successfully record the HR of several adults as well as to detect any design flaws. From these recordings it can be seen that the amount of HRV differs from individual to individual. Being able to test the HR design with a working prototype may have saved several design iterations which are an inevitable characteristic of an evolving design. The relative low cost of FPGAs and the ability of these devices to be programmed in the laboratory, allows design iterations to be made, without incurring the large financial and time penalties associated with resubmitting masked ASIC designs.

When the HR recorder design was migrated to the ES2 process (see Chapter 4), the success of the FPGA based prototype took the onus off the ASIC simulations. The HR recorder circuitry was transferred from the Actel FPGA design to the ES2 ASIC design, by simply re-entering the schematics. The successful operation of the FPGA based prototype HR recorder increased the likelihood of the ASIC based HR recorder circuitry being right first time.

The ability of FPGAs to implement the various circuits described in this thesis is limited by the purely digital nature of these devices. A mixed FPGA device containing a limited range of analogue components would prove to be a real alternative to masked ASICs for both circuit development and realisation of the final design, particularly if the power consumption could also be reduced.

CHAPTER 4

THE DESIGN OF A MIXED ANALOGUE AND DIGITAL ASIC

4.1. Introduction

This chapter describes the work involved in the design and realisation of a mixed analogue and digital application specific integrated circuit (ASIC) for use in various ambulatory recorders of electrophysiological signals. Justification is given for selecting the European Silicon Structures (ES2) foundry via the Solo1400 computer aided design (CAD) tool, highlighting the importance of the Eurochip scheme in this decision

4.2. Overall ASIC design

The final ASIC designed, contains all the components shown in Figure 4.1 apart from the RAM. The ASIC has two modes of operation, each mode being used as the basis for one of two different ambulatory recorder designs:

1) Adult heart rate (HR) recorder (Mode 1)
2) General electrophysiological signal recorder (Mode 2)

Similarities in the operation of these two recorder designs means that much of the ASIC circuitry is common to both instruments. This is particularly true for the analogue front end circuitry needed for signal conditioning and the digital circuitry used for interfacing with the serial port of a PC.

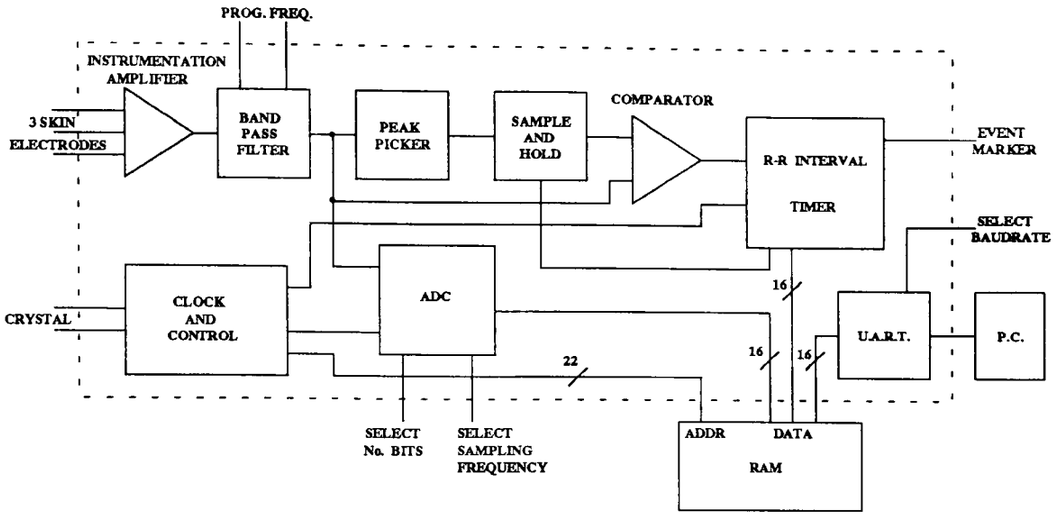


Figure 4.1: Overall ASIC design.

When configured as an adult HR recorder (Mode 1), the electrocardiogram (ECG), detected by skin electrodes on the chest, is amplified and filtered to enhance the R-wave, while suppressing baseline drift and high frequency noise. The combination of a peak picker, a sample and hold circuit and a comparator acts as an analogue R-peak detection scheme, which provides a digital rising edge to the R-R interval timer circuitry, every time an R-peak is detected. Successive R-R intervals are continuously stored in off-chip RAM until recording is complete, at which point the R-R interval data can be transferred, by the on-board universal asynchronous receiver transmitter (UART), to a PC, via its serial port.

When configured as a general electrophysiological signal recorder (Mode 2), the ASIC amplifies, filters and digitises the raw signal detected by the 3 skin electrodes. The gain and bandwidth of this signal conditioning circuitry is adjustable, as is the sampling frequency and resolution of the analogue to digital converter (ADC). This flexibility allows the instrument to be applied to a whole range of electrophysiological signals. The ASIC is designed so that the digitised signal can be either stored directly in off-chip RAM or first processed by an off-chip digital signal processor (DSP) (not shown in Figure 4.1.).

In the initial mode 2 recorder (without DSP), stored data is transferred to a PC, via its serial port, again using the on-board serial interface (UART). The clock and control circuitry controls the digital R-R interval timer circuitry, the sampling frequency of the ADC and the addressing of the external RAM. However, in the DSP based version of the mode 2 recorder both the addressing of the RAM and the downloading of data to a PC are controlled by the DSP.

4.3. Choosing a process and a CAD tool

Before the work on an ASIC design can begin it is important to choose an appropriate process and a suitable CAD tool. The process that is chosen will determine the method in which the circuit will be realised in silicon. Different process options have differing characteristics (full custom/standard cell/gate array, analogue/digital, on-chip resistors/capacitors), as well as different minimum feature sizes. The software packages (CAD tools) used to design ASICs vary greatly in complexity and capability. Some packages are generic, capable of full custom design and full analogue simulation, whereas others may be tied to a particular process and only be suitable for digital designs.

4.3.1. The Eurochip scheme

The cost of both CAD tools and fabrication can be expensive, often running into many thousands of pounds. One method of reducing the cost is to access the Eurochip scheme. Eurochip is a European initiative to provide low cost access to both processes and CAD tools, for academic institutions in the European Union. In addition, heavily discounted routes are also available to industry.

4.3.2. Process options

The various process options available at the time were:

1. Mietec 2.4μm double metal, double poly, CMOS mixed analogue and digital

   Advantages:

   - Analogue components in core of chip
   - Double layer poly for accurate capacitors
   - Full custom design possible

   Disadvantages:

   - Requires a more complex CAD tool (Mentor/Cadence)
   - No accurate resistors
   - No macros available for ADCs etc.
   - No simulation models available for analogue cells (at the time)
   - D-type flip flops with propagation delay less than hold time

2. ES2 1.5μm double metal, single poly, CMOS mainly digital standard cell

   Advantages

   - Full custom design possible
   - Macros available for ADCs(8 bit)
   - Pseudo analogue simulation available in the digital environment
   - Previous experience of using within the Department
   - Analogue samples available

   Disadvantages

   - Analogue components are located around the I/Os
   - Unsure about the performance of the op-amps
   - No resistors/capacitors available - must be off chip

3. MCE 3μm mixed analogue and digital gate array

Advantages

- Small range of resistors and capacitors available
- Good range of analogue library (8 bit ADC)
- SPICE analogue models available

Disadvantages

- Gate array mainly
- No large digital macros i.e. multipliers
- Limited to less than 1000 digital gates
- Not part of Eurochip

4.3.3. CAD options

In addition to the selection of a suitable process, it is also necessary to chose a CAD package that is appropriate in terms of its complexity, capability and compatibility with the desired process. The various CAD package options available at the time were:

1. Mentor Graphics

Advantages:

- Good generic package
- Full custom capability
- Analogue simulation plus interface to SPICE
- Previous experience of using within the Department

Disadvantages

- Version 7 to version 8 transition bugs
- Poor Eurochip support
- Complex software package

2. ES2 Solo1400

Advantages:

- Easy to learn, simple to use system
- Previous experience of using within the Department
- Good Eurochip support
- Designed specifically for the ES2 process

Disadvantages:

- Can only be used with the ES2 process
- No full custom design capability
- Only limited analogue simulations possible

3. Cadence

Advantages:

- Full custom design possible
- Good Eurochip support

Disadvantages:

- No previous experience of using within Department
- Complex software package

4. MCE

Advantages:

- Good support from MCE
- Easy to learn, simple to use, PC based software
- Analogue simulation possible using SPICE
- Designed specifically for the MCE processes

Disadvantages:

- Can only be used with the MCE process
- No full custom CAD capability

4.3.4. Process and CAD selection

In choosing a suitable process and CAD tool, it is important to remember that for this project it was necessary to produce an ASIC as quickly and as cheaply as possible, which contained as much, if not all, of the analogue and digital circuitry required for both of the different recorder designs. Speed was important because sufficient time was needed for both laboratory based tests and clinical measurements to be taken.

After considering all the options it was decided that the ASIC would be fabricated using the ES2 process via the Solo1400 CAD tool [ES2, 1991]. This tried and tested route uses an easy to learn, simple to use software package, with good Eurochip support, which has been specifically designed for use with the ES2 process. However, the lack of a full custom design capability (with Solo1400), restricts the ASIC circuitry to components which are available in the ES2 standard cell library, and the limited power of the analogue simulator, also restricts the complexity of any analogue simulations.

Although the ES2 1.5μm process is intended for purely digital designs, it does contain some analogue components in the standard cell library. Any analogue components which are used in a design are automatically placed by the software in the periphery of the ASIC, together with all the I/O pads. This has the disadvantage of increasing the periphery of the ASIC which tends to make designs which contain several analogue components, more likely to be pad limited. i.e. the area of silicon required for the design is determined by the number of I/O pads rather than the number of gates in the core of the chip. However, by keeping all the sensitive analogue components of the design together, in the periphery of the ASIC, away from "noisy" digital circuitry, the problem of switching noise is more likely to be reduced.

The ES2 standard cell library does not contain any resistors or capacitors, therefore all the resistors and capacitors required for the ASIC design have to be connected externally. This is not a major problem, as most of the resistors and capacitors needed for the design are required to be programmable, as their values determine the gain and bandwidth of the analogue front-end circuitry. Rather than having a series of selectable, potentially inaccurate resistors and capacitors on-chip, it is safer and more flexible to connect resistors and capacitors externally, even if this may require a few more I/O pins.

A major concern in using ES2 analogue components is the quality and performance of the ES2 op-amps. Although there have been hundreds of ES2 ASICs fabricated under the Eurochip scheme [Eurochip, 1993], virtually all of these designs have been purely digital. It is therefore difficult to obtain information regarding the quality of the ES2 op-amps, other than that which can be found in the ES2 data books. For a design which is intending to detect signals which are as small as the abdominal fetal electrocardiogram (FECG) (often less than 10 μV), then information on the quality of the op-amps in terms of noise, offset voltage and linearity is obviously important.

Under Solo1400 analogue circuits can be simulated using a pseudo analogue simulator in the digital environment. All analogue signals are represented as 8 bit digital signals and are simulated, together with other digital signals, in a multi-level analogue and digital simulator (MADS). This simulator only works at a resolution of 8 bits which is not accurate enough to simulate the part of the ASIC design which includes a 16 bit ADC. Hence, an alternative strategy was employed.

4.4. Testing out the analogue circuitry with ES2 sample chips

In order to get over some of the problems faced by using ES2 analogue components, such as op-amp performance and the limited power of the ES2 analogue simulator, sample chips were obtained from ES2, which contained various analogue components from the standard cell library. By prototyping the desired analogue circuitry using the components on these sample chips, valuable information on the performance of the ES2 op-amps and the suitability of the ES2 analogue components in general, was obtained. In effect, bread-boarding the analogue parts of the design with sample chips, acted as an alternative to analogue simulation, and provided a great confidence boost that the mixed ES2 ASIC design would work first time.

The ES2 1.5 μm process is a 5 Volt process (a voltage that can be obtained by the use of 4 NiCd AA batteries - typically 1.25 V each). The analogue circuitry requires a bipolar power supply in order to amplify and filter electrophysiological signals that are of a bipolar nature. A bipolar supply is achieved by connecting the analogue common to the centre of the batteries i.e. 2.5 V of the full 5 V supply (again easily achieved with 4 individual AA cells). Before a description of the analogue circuitry can be given, it is important to employ a naming convention, to be used when referring to analogue voltages. From this point forward the analogue circuit common i.e. the centre point of the 4 AA cells will be referred to as 0 V. The positive analogue supply voltage i.e. the most positive end of the 4 AA cells will be referred to as +2.5 V (called avdd in ES2 terminology), with the corresponding negative analogue supply voltage referred to as -2.5 V (confusingly called agnd in ES2 terminology). Note, the ES2 digital supply pins are called vddc (core), vddx (periphery), gndc (core) and gndx (periphery).

4.4.1. The dual slope integrating ADC

The ASIC designed for this thesis includes an ADC. This ADC is required in mode 2 and must be capable of digitising a variety of different electrophysiological signals. The ADC available in the ES2 1.5 μm library is only 8-bit and is thus not accurate enough for recording fetal ECG signals, which require at least 12 bit resolution. It was therefore necessary to investigate the possibility of designing a more accurate ADC, using the existing ES2 1.5 μm library components.

Various different types of ADCs were considered including successive approximation ADCs, flash ADCs and dual slope integrating ADCs [Horowitz and Hill, 1985]. Successive approximation ADCs require a digital to analogue converter (limited to 8 bit with ES2), flash ADCs require a large number of comparators (impractical with ES2), whereas a dual slope integrating ADC although frequency limited, has a reputed high accuracy and can be implemented relatively easily using components available in the ES2 1.5 μm library [Allen and Holberg, 1987]. It is also possible to change the resolution (i.e. number of bits) of a dual slope integrating ADC quite simply, allowing a programmable resolution ADC to be constructed. The analogue components needed for such an ADC consist of an op-amp (op 23), a comparator (comp23) and 3 analogue input multiplexers (as shown in Figure 4.2). The capacitor and resistor are connected externally since reproducible large values are difficult to achieve with integrated circuits. The resolution of the ADC is determined by the N bit counter. A maximum resolution of 16 bits was considered adequate for this application.

The operation of a dual slope integrating ADC is based around a simple integrating op-amp circuit, whose output Vr is used to control the clock of an N bit counter which outputs the result of the conversion. The overflow output

of the N bit counter is used to control a 3-to-1 analogue multiplexer which determines the voltage that is seen by the input of the integrator.

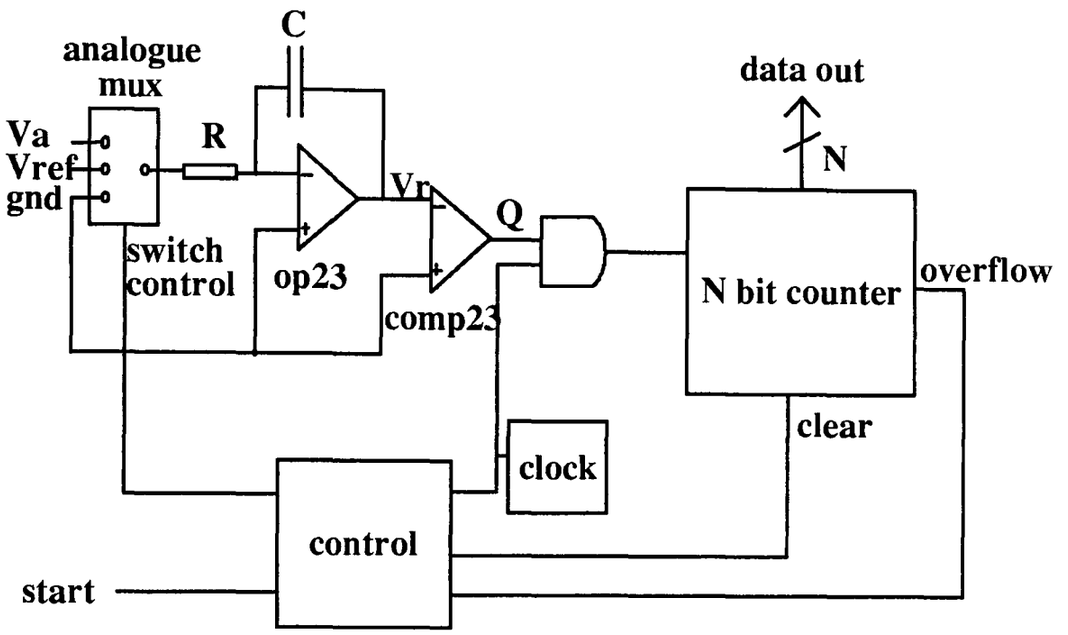


Figure 4.2: An N bit dual slope integrating ADC using ES2 sample chips.

The operation of a dual slope integrating ADC requires a reference voltage, Vref, which is at least as negative as the maximum analogue input voltage is positive. As the power supply for the analogue circuitry is set at +/-2.5 V, the analogue input range of the ADC is therefore restricted to 0 to +2.5 V, with Vref set at -2.5 V. In order to prevent negative voltages being input to the ADC, a bias circuit is used to attenuate the output of the signal conditioning circuitry by a factor of two, as well as to bias the voltage up by 1.25 V. This circuit has the effect of converting a +/-2.5 V range to a 0 to 2.5 V range.

Before conversion begins the input of the integrator is connected to 0 V (gnd) and the N bit counter is reset. A rising edge on the start input to the control logic begins the analogue conversion. The analogue signal to be converted (Va) is selected as the input to the integrator. As the analogue signal is somewhere in the range 0 V to 2.5 V, it follows that Vr will begin to go negative at a rate

of Va/RC volts per second (as shown in Figure 4.3). As soon as Vr drops below 0 V, the output of the comparator Q goes high and the N bit counter begins to increment. When the N bit counter reaches full scale, after 2^N clock cycles, the overflow output goes high, which causes the analogue multiplexer to switch to Vref (-2.5V). At this point the output of the N bit counter is zero. Vr now begins to return to 0 V at a rate of 2.5/RC volts per second, while the N bit counter continues to increment. As soon as Vr reaches 0 V, Q goes low, the N bit counter ceases to increment, the counter output is latched into a register (not shown) and the analogue multiplexer switches to gnd (0 V). The N bit counter is then reset until the next rising edge appears on the start input, at which point the next analogue conversion begins.

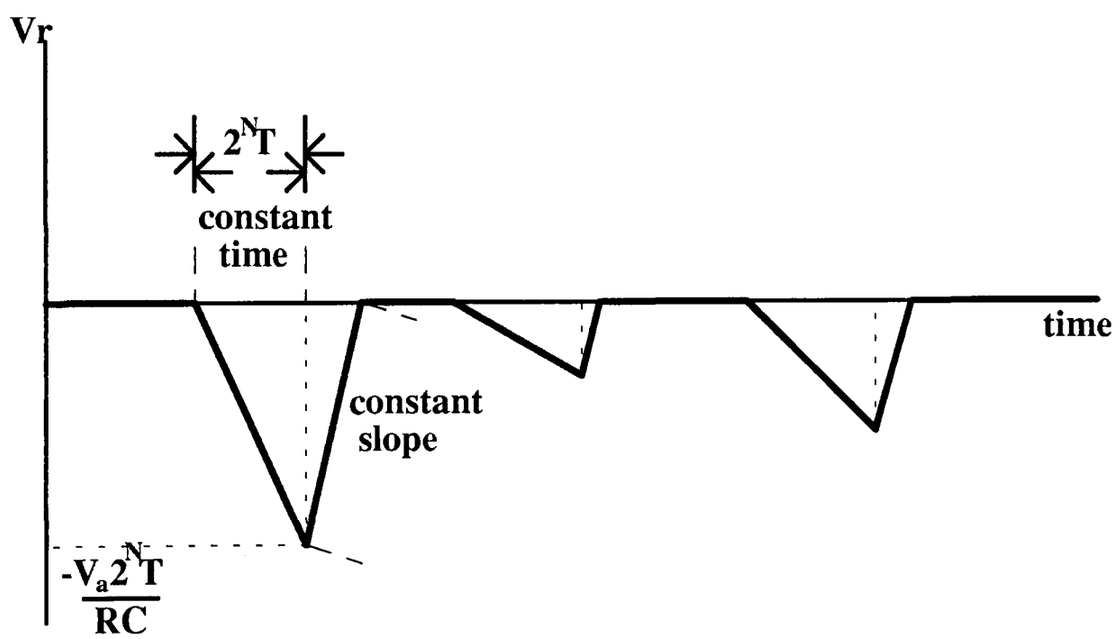


Fig 4.3: The voltage at the output of the integrator (Vr) as a function of time during 3 consecutive analogue conversions.

It should be noted that from the point at which Va is connected to the integrator, the N bit counter counts for a constant time of 2^NT seconds, where T is the period of the counter clock. During this time, Vr will decrease linearly at a rate of Va/RC volts per second. Hence the minimum value of Vr is proportional to Va. After 2^NT seconds, Vref (-2.5 V) is connected to the input

of the integrator which causes Vr to increase linearly towards 0 V at a constant rate of 2.5/RC volts per second. The length of time taken to reach 0 V determines the final digital output of the N bit counter and is directly proportional to the minimum value of Vr, which is in turn directly proportional to the value of Va. Hence the overall circuit acts to produce a digital output which is directly proportional to the analogue input voltage.

4.4.2. ADC Design Factors

The conversion time of the ADC is dependent upon the counter clock period and the value of N. The worst case conversion time is $2 \times 2^{N}T$. A fast counter clock and a low value of N will thus give a short conversion time. A shorter conversion time, will allow a faster sampling frequency to be used. However the bit resolution of the ADC is determined by the value of N. Hence there is a trade-off between resolution and sampling frequency, which is fundamentally limited by the clock frequency of the N bit counter.

It is also important that suitable values of R and C are chosen which maximise the dynamic voltage range of Vr. It is desirable that a maximum analogue input voltage (2.5 V) should cause Vr to integrate down to -2.5 V, as this will minimise the influence of any noise on the digital output. For instance, if a larger value of RC was chosen such that an input of 2.5 V(Va) caused Vr to integrate down only as far as -0.25 V, then a noise signal of 0.25 mV would cause an error in the digital output of the order of 0.1%. If, however the value of RC is such that an analogue input of 2.5 V causes Vr to integrate down to -2.5 V, then the same noise signal of 0.25 mV will introduce an error in the digital output of only 0.01%.

Care must also be taken that the value of RC is not so small as it causes Vr to saturate negatively when an analogue input approaching 2.5 V is applied. This

would have the effect of reducing the range of the digital output, in that a full scale digital output would be produced by analogue inputs of both 2.5 V and 2.4 V (say). The optimum value of RC is that which is half the sampling period, but it is probably prudent to chose a combination which gives a slightly larger value, given the tolerance of the components, even if this is at the expense of a slight increase in noise susceptibility.

As the ADC that is needed for the ASIC is required to digitise various different raw electrophysiological signals, it would be desirable if an ADC could be designed which can digitise at 16 bit resolution and with a sampling frequency of several kHz. However, with a dual slope integrating ADC implemented using the ES2 process, the maximum sampling frequency obtainable at 16 bit is limited by the maximum recommended clock speed of the ES2 1.5 μm process. This maximum clock speed is given as 30 MHz in the ES2 data book as this is the recommended maximum crystal frequency which can be connected across the specially designed crystal input pads contained in the standard cell library.

As the existing R-R interval timer and UART circuitry requires several different clock signals all of which can be easily obtained from a standard 19.6608 MHz crystal, it is this frequency that was chosen to be the main clock frequency of the ASIC. Hence the maximum sampling frequency of the ADC at 16 bit resolution is thus limited to:

$$f_{max} = \frac{f_{clock}}{2 \times 2^{N}}$$

$$f_{\substack{max \\ @16bit}} = \frac{19.6608 \times 10^{6}}{2 \times 2^{16}}$$

$$= \mathbf{150\ Hz}$$

This frequency is in fact more than adequate for several types of electrophysiological signals which are of relatively low frequency content.

By making the value of N programmable, it is possible to adapt the ADC for use at higher sampling frequencies at the expense of bit resolution. A reduction of 1 bit of resolution allows a doubling of the maximum sampling frequency. In hardware terms, reducing N by 1 can easily be achieved by altering the logic which produces the overflow pulse. This involves simply 'anding' the existing overflow signal with the output of the previous bit of the binary counter. Thus the overflow signal goes high after only half as many clock pulses.

Eight different ADC resolutions were chosen ranging from 9 to 16 bits, with the selection being determined by the combination of three input pins. In addition, eight corresponding sampling frequencies were chosen ranging from 75 Hz to 9.6 kHz. Although in theory it should be possible to set the sampling frequency range to be from 150 Hz to 19.2 kHz, there was a concern that problems may arise with an analogue input of 2.5 V when 16 bits and 150 Hz are selected. In this case any slight input offset may prevent Q (in Figure 4.2) from going low before the next sampling pulse arrives. Providing the option of setting the sampling frequency to 75 Hz allows sufficient time for Q to go low, the digital output to be latched and the N bit counter to be cleared, before the next sampling pulse arrives.

The lower the sampling frequency, the longer the record time. Hence a sampling frequency of 75 Hz could prove useful in extending the maximum record time of the raw electrophysiological signal recorder. This is particularly the case when the signal to be recorded is of a low frequency content as in the case of the electrohysterogram (EHG). With a 512 K x 8 bit SRAM and a 75 Hz sampling frequency (at 16 bit), the recording time is limited to:

$$\frac{1}{75} \times 256\text{Kwords} = 56.89 \text{ mins}$$

In order to maintain complete flexibility in terms of sampling frequency an external pin was included which allows the main crystal frequency to be overridden by an external clock signal.

4.4.3. Bread-boarding the dual slope ADC

The dual slope ADC was bread-boarded in the laboratory using ES2's analogue sample components and standard HCT devices for the digital part. The programmable dual slope integrating ADC was successfully prototyped on a bread-board with 16 bit resolution at a sampling frequency of 7.5 Hz. The selection of a 7.5 Hz sampling frequency, rather than a 75 Hz sampling frequency, results from the use of a 2 MHz crystal rather than a 19.6608 MHz crystal, as is the case for the final ASIC design. This lower frequency crystal was chosen so as to overcome timing constraints, caused by the parasitic capacitance of the breadboard and the propagation delays of the HCT devices. As the ES2 1.5 µm process has a reputed maximum clock speed of 30 MHz, these timing problems should not arise for the final ASIC design.

The linearity of the ADC was tested by connecting the analogue input (Va) to the output of a potentiometer, which ranged from 0 V to +2.5 V. The value of Va was varied in steps of 0.1 V from 0 V to 2.5 V, with each corresponding digital output being noted. The value of Va was measured on a multimeter to an accuracy of +/- 10 mV, which corresponds to a digital accuracy of around 8 bits. Figure 4.4 shows the 16 bit digital output changing with good linearity (at least 8 bit) as the input to the ADC is varied from 0 V to 2.5 V. The digital output at any given analogue input was stable to around 12 bits, which corresponds to an analogue voltage stability of 0.6 mV. The stability of the

analogue voltage was later improved by introducing a decoupling scheme which resulted in an improved digital stability of 15 bits.

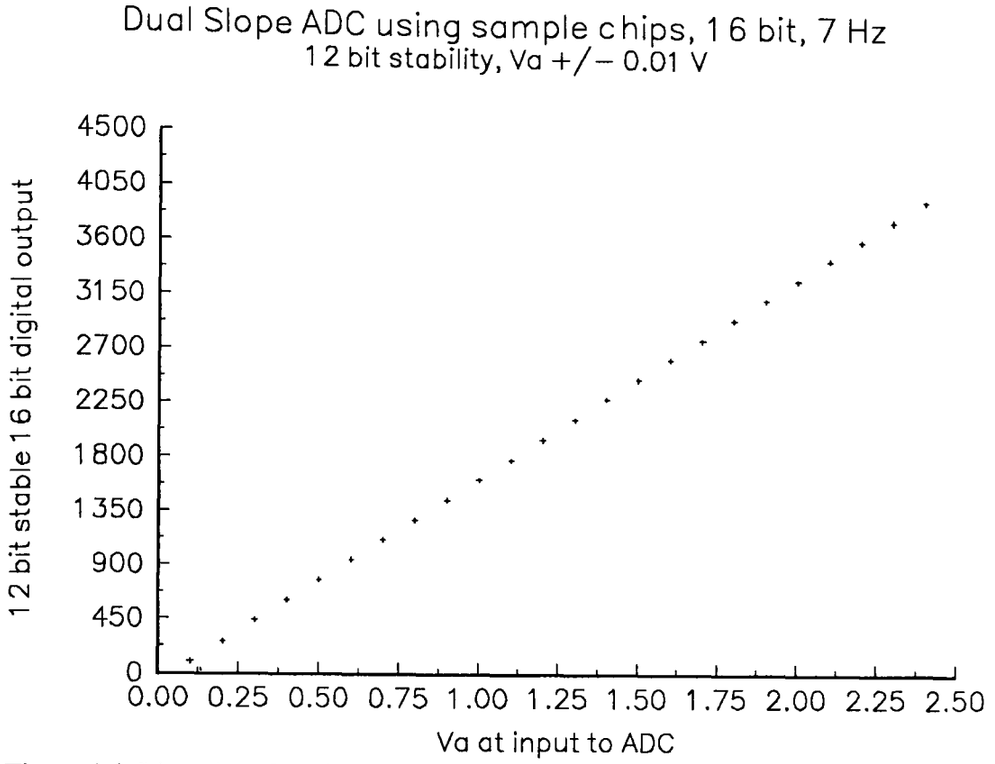


Figure 4.4: Linearity of dual slope ADC prototyped using ES2 sample chips.

4.4.4. Performance of ES2 op-amps

There are three types of op-amps and comparators in the ES2 1.5 μm library- op13, op23 and op33 [Table 3.1]. The first number in the code refers to the type of op-amp, while the second number refers to the number of I/O pads that are connected (which can vary from 1 to 3). In order that every pin of the op-amp is externally accessible, an op-amp with a second number of 3 is required. Although the op33 low power op-amps would seem to be ideal for the battery powered recorder design, they have the major disadvantage of a limited output voltage range. A reduced output voltage range would severely restrict the performance of the dual slope integrating ADC and therefore it was decided to use the op23 op-amp. The major problem with using op23 op-amps, is the relatively large increase in power consumption that this entails. However, it was calculated that the batteries could cope with this increase in power consumption, without an increase in battery volume and therefore weight:

AA alkaline cell capacity = 2.7 Ah

$$\text{maximum current for 24 hour operation} = \frac{2.7}{24} = 112.5 \text{ mA}$$

$$\text{op23 current} = \frac{13.4 \text{ mW}}{5 \text{ V}} = 2.68 \text{ mA}$$

(10 op-amps + 1 comparator) x 2.68 mA = 29.48 mA

op-amp	op13	op23	op33
type	high speed	high drive	low power
DC power R_L=1MΩ	15 mW	13.4 mW	450 μW
input noise @ 10 Hz	370 nV/√Hz	280 nV/√Hz	1400 nV/√Hz
CMRR @ 1 kHz	81 dB	84 dB	102 dB
output range R_L=600 kΩ	0 V - 5 V	0 V - 5 V	1.25 V - 3.75 V

Table 4.1: ES2 1.5 mm op-amp comparison table.

4.5. Design of the ES2 ASIC using Solo1400

The Solo1400 CAD package provides the ASIC designer with the ability to draw, simulate and layout an ES2 ASIC design. A list of the software tools which make up the Solo1400 CAD package is presented in Figure 4.5. Each of the names (in capital letters) is an individual program which is run within the Solo1400 environment, whereas the terms in brackets refer to the different options that can be set. This diagram is also intended to give an indication of each tools position in the general flow from schematic capture, through simulation to layout and packaging.

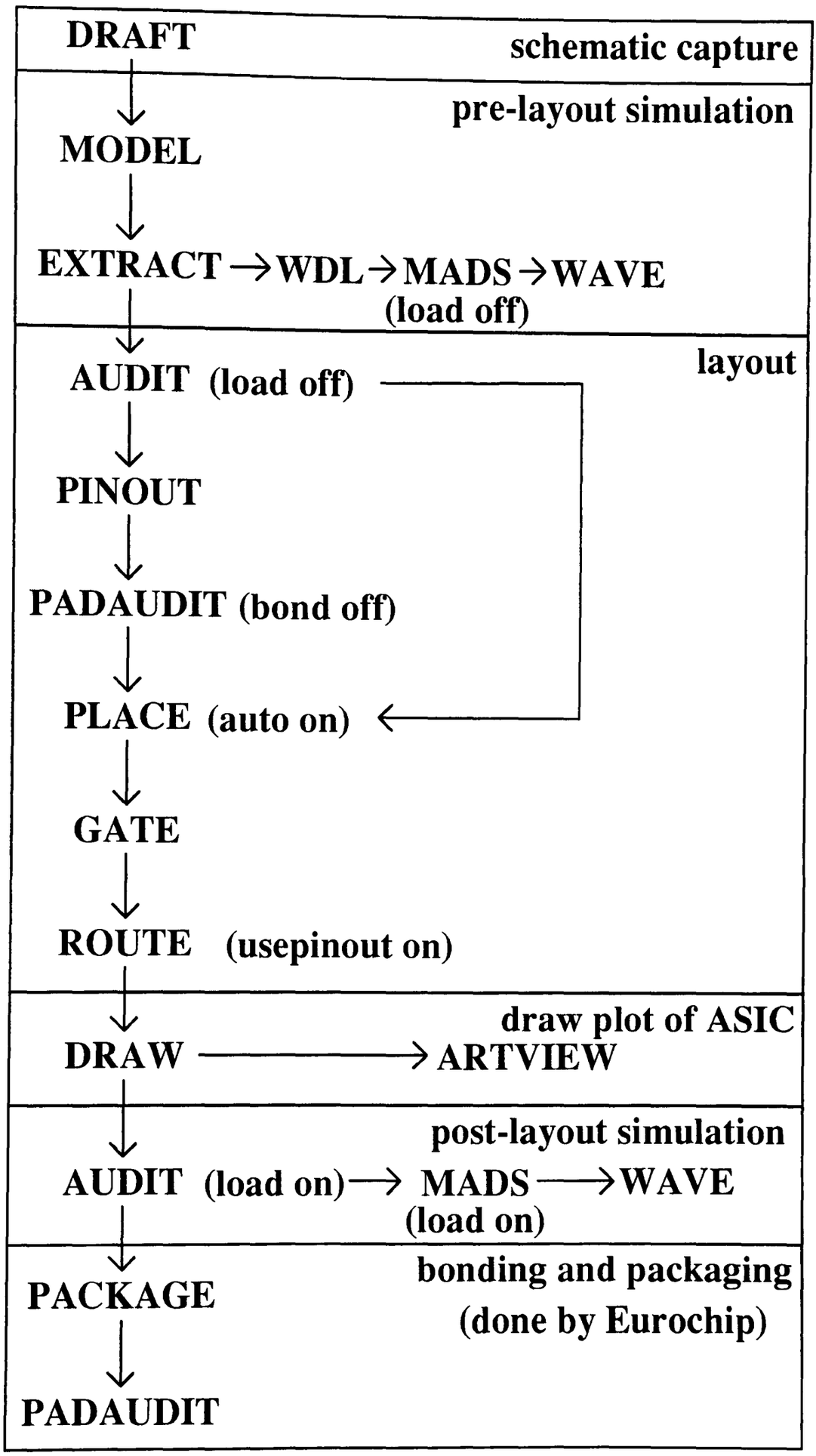


Figure 4.5: Solo1400 CAD tools flow diagram.

4.5.1. Schematic capture

In general, most ASIC designs are entered into a CAD package via a graphical interface which is usually referred to as schematic capture. There are other methods such as VHDL (Very high speed integrated circuit Hardware Description Language) [Lipsett et al., 1989], which is a text based high level design language, but these methods of design entry are usually intended for higher level system designers, who generally have little interest in individual gates and transistors.

The Solo1400 schematic capture package is called DRAFT and allows the designer to select various components from the ES2 standard cell library which can then be placed on a schematic sheet and connected together as required.

4.5.2. Description of ASIC schematics

Figure 4.6 gives an overview of the ASIC circuitry highlighting in this case the more important signals. For a more detail circuit description a copy of all the detailed ASIC schematics can be found in Appendix C

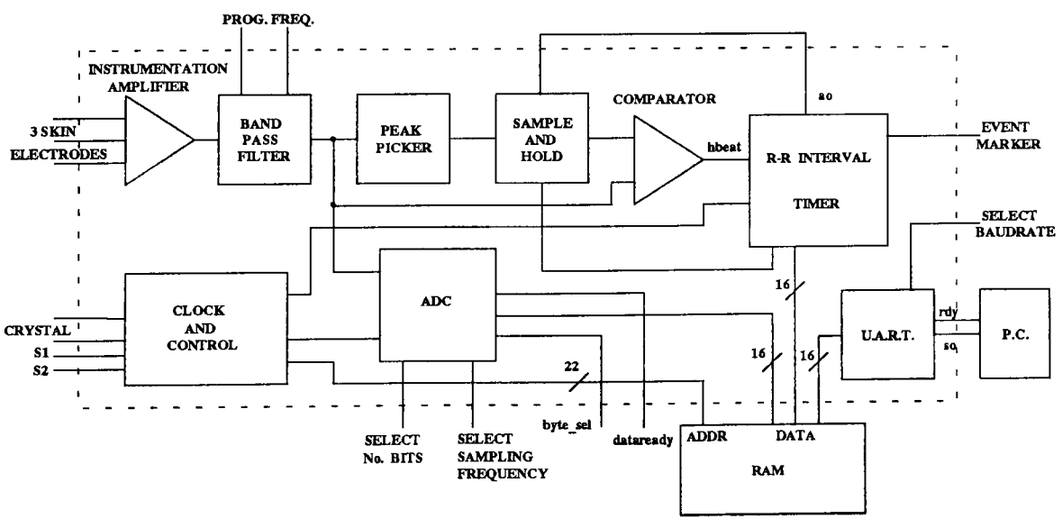


Figure 4.6: Overview of ASIC design including important signals.

It is standard practice to enter ASIC designs with some element of hierarchy [Naish and Bishop, 1988], starting with simple building block circuits at the lowest level which are then used to form more complex circuitry, building up to the top sheet. Each block of circuitry in an ES2 design is known as a part, and as such can be copied and saved in the standard cell library for use in another area of the ASIC design (or for that matter in any other design).

This ES2 ASIC contains 12 such parts starting with 'chip' (the name of the part on the top sheet) and going down to such as 'word16', which is 3 levels below. A diagram illustrating the hierarchy of the ES2 ASIC is shown in Figure 4.7.

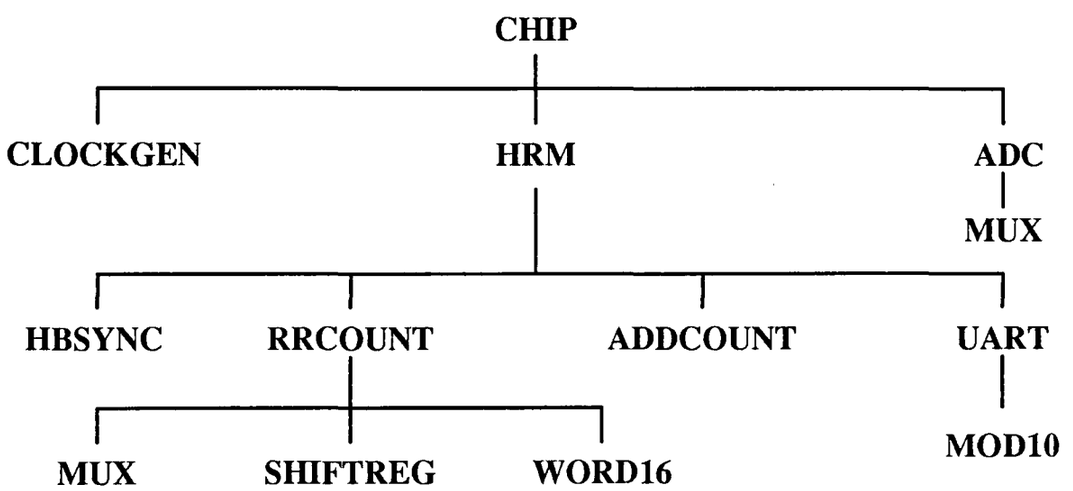


Fig 4.7: Hierarchy of all the parts that are used in the ES2 ASIC design.

The top sheet part 'chip' contains three other parts as well as all the I/O pads. As the analogue components in the ES2 library are classified as I/O pads, all these components must be placed on the top sheet. The analogue components consist of 10 op-amps, one comparator, three analogue multiplexers and two analogue input pads. These analogue components are needed for the instrumentation amplifier, the bandpass filter, the peak picker and the sample and hold circuit as well as for part of the ADC.

The part 'adc' contains all the digital circuitry required to control the operation of the dual slope integrating ADC, including all the writing to RAM operations required in mode 2 operation. The 'adc' part includes a 16-to-8 multiplexer (partname 'mux') which converts the 16 bit digital output of the ADC into two 8 bit bytes, a low byte and a high byte, ready for writing to 8 bit wide SRAM (in mode 2 operation). The 'byte-sel' signal is used to control 'mux' and so determines whether the DSP reads the high or the low byte. The output signal 'dataready' is used in mode 2 operation to tell the DSP that an analogue to digital conversion is complete and that the digital output is stable and is ready to be read.

The part 'clockgen' is used to produce all the clock signals that are required by all the different parts of the design. This part basically consists of a 31 stage divider chain which is driven by a 19.6608 MHz crystal, connected externally to the crystal input pads.

The part 'hrm' contains the majority of the ASIC circuitry required for mode 1 operation including the downloading circuitry and is basically all the digital circuitry that was prototyped on the Actel field programmable gate array (FPGA) - see Chapter 3. This part contains 4 smaller parts 'hbsync', 'rrcount', 'addcount' and 'uart'.

The part 'hbsync' is used in mode 1 operation to synchronise the asynchronous 'hbeat' signal, produced by the analogue front-end, to the 2.4 kHz mode 1 system clock.

The part 'addcount' is used to control the addressing of the external RAM, which is used in both the store and download operations, of both mode 1 and

mode 2. This part includes circuitry which allows the size of the external RAM that is to be addressed, to be set by the input pins 's1' and 's2'.

The part 'uart' is used to convert data which is stored in external RAM, from parallel to serial RS-232 format, this is achieved by loading the data into a shift register. Once in the shift register, the appropriate start and stop bits are added and the data is clocked out serially, via the output pad 'so'. This pad is connected to the serial port of the PC, where a program stores the data on to the hard disk. The input signal 'rdy' (referred to as DTR in Chapter 3) is used by the PC to tell the 'uart' circuit when it is ready to receive data and also when to stop sending data, if, for instance, a block of received data needs to be written to the hard disk. The signal 'rdy' controls the transmission of data by either enabling or disabling the clock which is used to clock out the serial data. Included in part 'uart' is a modulo 10 counter ('mod10'), which is used to divide the signal, used to clock out the serial data, by a factor of 10. This new clock frequency is used to load a new data byte into the 'uart' shift register, ready for serial transmission to the P.C.

The part 'rrcount' contains the circuitry which is used to time and then store in external RAM the R-R intervals which are produced during mode 1 operation. This part contains a further 3 parts, 'shiftreg', 'word16' and another instance of 'mux'.

The part 'shiftreg' is used to control the writing of the R-R interval counts to external RAM, as well as to provide a sampling signal 'ao', to the sample and hold circuit of the analogue R-peak detection scheme.

The part 'word16' contains a 14 bit counter, which is used to count the R-R interval. The output of this count is then combined with a 2 bit time and event

marker to form a 16 bit output. This 16 bit data is then split into two 8 bit bytes ready for storing in the 8 bit wide external RAM.

4.5.3. ASIC simulation

Once the ASIC design has been entered into the CAD package, the design needs to be simulated, in order to check that the ASIC operates as intended. With large ASIC designs that use hundreds of standard cell components, it is very likely that errors will have been introduced during schematic capture. Simulation can be used to spot these errors, as well as other genuine design flaws. Timing problems, such as set-up and hold time violations, spikes, hazards and glitches can also be spotted by the simulator.

The simulation process involves the application of input vectors, to the ASIC design that has been entered via schematic capture. The simulation software then outputs the resulting output vectors, which are usually displayed graphically in the form of timing diagrams. The skill in simulating is the ability to write a set of input vectors which thoroughly tests every function of the ASIC design, using the minimum number of input vectors.

The simulation files used to simulate the ES2 ASIC are written in Waveform Description Language (WDL), which has a very similar format to that of a conventional C program. The Solo1400 multi-level analogue and digital simulator (MADS) provides an output which can be converted into a graphical format using WAVE. There are 2 types of simulation, pre-layout simulation and post-layout simulation. Pre-layout simulation includes gate delays but does not include wiring delays, as this information is unknown before layout has taken place. Post-layout simulation includes both gate and wiring delays and provides more accurate timing information, which is particularly important if the design contains any speed critical circuitry.

4.5.4. ASIC pinout and power supplies

The ES2 process uses three different types of power supply pads, one type of pad is for the analogue circuitry and the other two types of pads are for the digital circuitry. The digital power supplies are split into those which are used to power the digital core and those that are used to power the digital I/O pads. Individual power supply pads are limited in the number of I/O pads or core gates that they can supply. Therefore, it is important that the ASIC design contains a sufficient number of power supply pads, to power both the circuit and the I/O pads.

The PINOUT software allows the designer to determine the position of all the ASIC I/O pads. This allows the designer to move power supply pads nearer to I/O pads which are not receiving enough current. In addition the designer can use the PINOUT software to modify the ASIC pinout to that which is desired. Ultimately however, there may simply not be enough supply pads to power all the circuitry and I/O pads. In this case extra sets of power supply pads must be included on the top sheet of the schematics. The PADAUDIT software checks that each I/O pad is receiving enough power and that there is enough current being supplied to the core of the ASIC. Any deficiencies in the power supply are reported to the designer in the form of errors. In order to pass the PADAUDIT tests, all the analogue circuitry must be separated from the digital circuitry. This entails placing the analogue pads (containing the analogue components) around the top left hand corner of the ASIC periphery, with the analogue supply pads being positioned at either end, i.e. analogue ground at one end, and analogue VDD at the other. These analogue supply pads contain an isolation region which terminates the analogue supply rails and shields the analogue circuitry from the noisy digital I/O pads.

4.5.5. ASIC layout and bonding

Once the ASIC design has been successfully simulated and a suitable pinout selected, the next step is to layout the ASIC design onto a clean piece of silicon. The layout process involves the placing of all the standard cell components used in the ASIC design on to the silicon followed by the routing of all the connections. Solo1400 allows this step to be performed by the designer. However, it is much quicker to let the CAD package do the placing and routing automatically by setting the 'auto option' to on. Setting the 'usepinout' option to "on", causes the router to use the pinout that has been chosen by the designer in PINOUT software.

After successfully laying out the ASIC design, it is possible to do a post-layout simulation by setting the 'load option' to on. A post-layout simulation using MADS can use the same WDL file that was successfully used in the pre-layout simulation. Once again, the output can be displayed graphically using WAVE.

The Solo1400 package also contains software that allows the designer to select an appropriate package and pinout for the ASIC. The pinout or bonding of the ASIC determines which pin of the package is connected to which I/O pad. For ES2 designs that are to be fabricated through the Eurochip scheme, the packaging and bonding information is provided separately on a bonding diagram, rather than from within Solo1400.

4.6. The ES2 ASIC I/Os

The designed ASIC uses 107 pins of a 120 pin PGA (pin grid array) consisting of 38 analogue I/Os, 2 crystal I/Os, 8 bi-directional pins, 21 digital input pins, 26 digital output pins and 12 power supply pins.

4.6.1. Multiplexing the I/Os

The fully laid out ASIC design was quite severely pad limited, mainly due to the large number of analogue components that have to be placed around the periphery of the ASIC. In order to reduce the extent of this pad limiting effect, a multiplexing scheme was devised for the I/Os. This involved certain I/O signals sharing I/O pads, which is made possible by the fact that the ASIC is only ever configured in one of the two modes of operation, at any one time. Some of the I/O signals that are required for mode 1 are not needed for mode 2 and vice versa. This means that an I/O pad that is used for a particular I/O signal while in one mode, can then be switched to a different I/O signal when the ASIC is configured in mode 2.

4.6.2. Function of I/Os

The following 6 tables give the pinout and a brief description of the functionality of all of the I/Os used in the ES2 ASIC.

Crystal pads:

signal	pin	description
xin xout	A11 B10	pins across which to connect the external crystal to provide the main ASIC system clock

Table 4.2: A description and pinout of all the crystal pads

Power supply pads:

signal	pin	description
vddc	B12 H12	power supply to the digital core
vddx	A12 C5 H1	power supply to the digital periphery (I/O pads)
avdd	C13	power supply to the analogue circuitry (in periphery)
gndc	B6 N5	digital core ground
gndx	C7 M5 D1	digital periphery ground (I/O pads)
agnd	L6	analogue circuitry ground (in periphery)

Table 4.3 a description and pinout of all the power supply pads

Digital input pads:

signal	pin	description
adc_hrm	A5	select mode 1(high) or mode 2(low)
resetb	C6	system reset (active low)
store	B5	select store (high) or download (low)
selclock	B11	select source of main system clock
event_osc	K3	event marker (mode 1) / clock input (mode 2)
hbeat-q	K2	hbeat input (mode 1) / Q from ADC (mode 2)
selsysclk_ram_dsp	M1	select external or internal clock input (mode 1) /selection of RAM(high) or DSP(low) (mode 2)
exsysclk_bytesel	L1	external clock (mode 1) / byte select (mode 2)
bit 0 bit 1 bit 2	M4 L5 N4	ADC resolution selection pins
samp 0 samp 1 samp 2	L4 M3 N3	ADC sampling frequency selection pins
ram_sel 0 ram_sel 1	B4 A3	RAM size selection pins
selbaudrate	A10	select internally or externally derived baud rate
exbaudrate	C9	external baud rate input
baudrate 0 baudrate 1	L2 N1	baud rate selection pins
rdy	A4	PC is ready to receive download data

Table 4.4: A description and pinout of all the digital input pads

Digital output pads:

signal	pin	description
A0 A1 A2 A3 A4 A5 A6 A7 A8 A9 A10 A11 A12 A13 A14 A15 A16 A17 A18 A19	A2 C4 B3 A1 C3 B2 B1 D3 C2 C1 D2 E3 E2 E1 F3 F2 F1 G2 G3 G1	address lines
memfull	K1	memory full - indicates that RAM is full (active high)
wrb	J2	write bar - enables data to be written to RAM (active low)
oeb	J1	output enable bar - enables data to be read from RAM (active low)
ramenb	H3	ram enable bar - RAM chip select (active low)
dataready	C10	informs DSP that the digital output of the ADC is stable and ready to be read (active low)
so	J3	serial out - serial output from UART in RS-232 format

Table 4.5: description and pinout of all the digital output pads

Analogue pads:

signal	pin	description
inst1+ inst1- inst1o	J12 K13 J11	op-amp to be used in standard 3 op-amp configuration instrumentation amplifier
inst2+ inst2- inst2o	K12 L13 L12	op-amp to be used in standard 3 op-amp configuration instrumentation amplifier
inst3+ inst3- inst3o	N9 L8 M8	op-amp to be used in standard 3 op-amp configuration instrumentation amplifier
highpass+ highpass- highpasso	N12 N11 M10	op-amp to be used as a highpass filter in feedback of the instrumentation amplifier
gain+ gain- gaino	N8 N7 L7	op-amp to be used as a gain stage
filter+ filter- filtero	G11 G12 H13	op-amp to be used as a low pass filter
peakpick1+ peakpick1- peakpick1o	M7 N6 M6	op-amp to be used in a 2 op-amp peak picker circuit as part of the analogue R-peak detection scheme used in mode 1
peakpick2+ peakpick2- peakpick2o	H12 H11 J13	op-amp to be used in a 2 op-amp peak picker circuit as part of the analogue R-peak detection scheme used in mode 1
sah1_adc1+ sah1_adc1- sah1_adc1o	F12 F13 G13	op-amp to be used in a 2 op-amp sample and hold circuit as part of the analogue R-peak detection scheme used in mode 1 or as part of ADC in mode 2
sah2_adc2+ sah2_adc2- sah2_adc2o	D12 E11 D13	op-amp to be used in a 2 op-amp sample and hold circuit as part of the analogue R-peak detection scheme used in mode 1 or as part of ADC in mode 2
comp+ comp- compo	E13 F11 E12	comparator to be used as part of the R-peak detection scheme used in mode 1 or as part of the ADC used in mode 2
muxa muxb muxc	M9 N10 L9	analogue switches to be used as a 3 to 1 analogue multiplexer as part of the ADC used in mode 2
va	K11	input to muxa (analogue input to adc)
half	L18	input to muxc (0 V input to adc)

Table 4.6: A description and pinout of all the analogue pads.

4.6.3. I/O settings

Several functions of the ASIC's digital circuitry are programmable, such as ADC resolution, sampling frequency and baud rate for downloading. These functions are programmed by applying the appropriate level to the relevant programming pins. The following section describes which signals need to be applied to which pins, in order to programme these functions.

ADC resolution: bit (2:0)

bit 2	0	0	0	0	1	1	1	1
bit 1	0	0	1	1	0	0	1	1
bit 0	0	1	0	1	0	1	0	1
resolution	16	15	14	13	12	11	10	9

ADC sampling frequency: samp (2:0)

samp 2	0	0	0	0	1	1	1	1
samp 1	0	0	1	1	0	0	1	1
samp 0	0	1	0	1	0	1	0	1
sampling frequency	9.6k	4.8k	2.4k	1.2k	600	300	150	75

External RAM size: ram_sel (1:0)

ram_sel 1	0	0	1	1
ram_sel 0	0	1	0	1
ram size	128kbyte	512kbyte	256kbyte	1024kbyte

Baud rate: baudrate (1:0)

baudrate 1	0	0	1	1
baudrate 0	0	1	0	1
baud rate	76.8kbaud	38.4kbaud	19.2kbaud	9.6kbaud

ASIC master clock: selclock

selclock	1	master clock derived from crystal connected to crystal I/O pads.
selclock	0	master clock taken from clock connected to input pad osc.

Mode 1 system clock: selsysclk

selsysclk	1	mode 1 system clock derived from ASIC main clock.
selsysclk	0	mode 1 system clock from clock connected to input pad exsysclk.

Baud rate source: selbaudrate

selbaudrate	1	baud rate derived from ASIC main clock.
selbaudrate	0	baud rate from clock connected to input pad exbaudrate.

Byte to be read by external DSP: byte_sel

byte_sel	1	MSB.
byte_sel	0	LSB.

4.7. Testing and Results.

On the return of the ES2 ASICs after fabrication, it was discovered that the chips had been bonded in a different orientation to the bonding diagram sent with the design. This can be seen when the lid is removed and the ASIC is viewed through a magnifying glass. After the chip had been powered up and the power consumption checked, a single op-amp was tested. All the op-amps on chip are individually accessible and it was therefore quite simple to connect up a voltage follower circuit, to check the op-amp's performance. The voltage follower gave a good linear response with the output following the input across the full 5 V range. An instrumentation amplifier was then constructed and tested with an ECG signal. A clean ECG trace was obtained with minimal 50 Hz interference. This demonstrated that the common mode rejection ratio (CMRR) of the op-amps was satisfactory.

The ASIC was then connected to a veroboard using a zero insertion force (ZIF) socket for ease of ASIC insertion and configured for mode 2 operation at a sampling frequency of 300 Hz with 15 bit resolution. Rather than being connected to the analogue front end, the input of the ADC was connected to a dc voltage source. This arrangement allowed the linearity of the ADC to be tested in system. Figure 4.8 shows the digital output increasing with good linearity as the analogue input is increased from 0 V to 2.5 V. The digital output at any given analogue input was stable to around 12 or 13 bits. The instability of the least significant 2 or 3 bits could be due to noise on the analogue input or on the ADC power supply, which may be reduced by decoupling. This in-system result agrees with the results obtained from the sample chip prototype, as discussed in section 4.4.3. and shown in Figure 4.4.

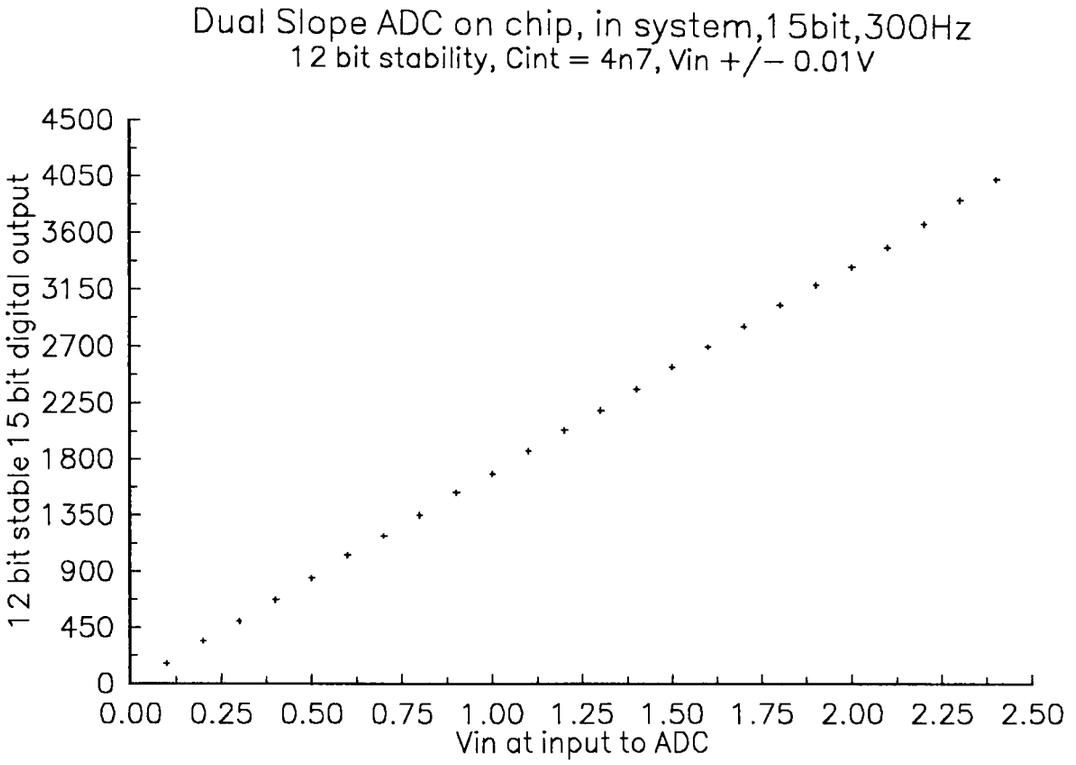


Figure 4.8: Linearity of dual slope ADC on chip tested in system.

4.8. Conclusions

A mixed analogue and digital ASIC has been designed that can be incorporated into either an adult HR recorder (see Chapter 5) or a general electrophysiological signal recorder (see Chapter 6). The circuit was designed with the Solo1400 CAD package and realised using the ES2 1.5 μm CMOS process. The lack of a suitable ADC in the ES2 library necessitated the design of a more appropriate ADC using standard ES2 library components. A dual slope integrating ADC was selected for reasons of high accuracy and circuit simplicity.

All the functions of the digital circuitry implemented on the ASIC were simulated rigorously, prior to fabrication using the Solo1400 CAD package, with the digital R-R interval timing circuitry additionally prototyped in the FPGA based HR recorder. Analogue functions of the ASIC design were prototyped using ES2 sample chips, including the dual slope integrating ADC. This approach was necessary due to the limited ability of Solo1400 to simulate

analogue circuits. When these analogue functionality tests were repeated on the fabricated ASICs, similar results were obtained. A voltage follower circuit gave a linear response across the full 5 V range, the instrumentation amplifier produced a clean ECG with minimal 50 Hz interference and the ADC demonstrated good linearity, with between 12 and 13 bit stability, when configured at 15 bit resolution and 300 Hz sampling frequency.

The ASIC design contains approximately 9000 digital transistors, has a silicon area of 38 mm^2 and is packaged in a standard 120 pin PGA (see plot in Appendix D). The overall power consumption of the ASIC is 150 mW which is almost completely due to the op-amps (13.4 mW each).

Overall, the ES2 1.5 μm process with the Solo1400 CAD tool, proved to be a successful vehicle for realising this particular mixed analogue and digital circuit. For similar designs of a mainly digital nature, which require a limited number of analogue components for front end instrumentation, the ES2 1.5 μm process with Solo1400 is highly desirable, being extremely simple to use, well documented and very cost effective. The ES2 1.5 μm process is available through Eurochip at a cost of 35 ECUs per mm^2. The number of devices received is dependent on the size of the circuit, 10 devices for designs which are less than 25 mm^2 and 20 devices for designs which are greater than 25 mm^2. The major drawback for low power designs is the power consumption of the op-amps. For designs requiring more complex analogue circuitry, the limited range of analogue cells and the limited power of the analogue simulator may prove too restrictive. For designs containing many analogue components, the constraint of placing these components around the periphery, may lead to an ASIC which is very pad limited. Although such placement may help in the reduction of interference from the digital circuitry.

CHAPTER 5

ADULT HR RECORDER USING AN ES2 ASIC

5.1. Introduction

This chapter describes the design of an ambulatory adult heart rate (HR) recorder using a European Silicon Structures (ES2) application specific integrated circuit (ASIC). The circuit for this instrument is based on the field programmable gate array (FPGA) prototype adult HR recorder described in Chapter 3. Experience gained from using this working prototype resulted in several improvements to the design being incorporated into the ASIC based instrument.

Results obtained with the ASIC based adult HR recorder include long-term (8 hours) recordings of daily beat-to-beat HR, HR during sleep and HR when exercising. The ability of this instrument to record the 0.3 Hz component of heart rate variability (HRV) associated with respiration, demonstrates its suitability for investigating HRV in normal adults.

5.2. Improvements made to HR recorder design

The advantages gained by migrating the FPGA design to an ES2 ASIC include a reduction in instrument size, owing to the integration of the analogue circuitry on to the ASIC, as well as a reduction in power consumption. The FPGA based recorder drew over 100 mA whereas the ES2 ASIC based recorder requires less than 40 mA. By integrating the analogue circuitry onto the ASIC, the recorder is reduced to essentially a 3 chip system i.e. ASIC, RAM and serial interface (MAX232). Unfortunately an error in the polarity of the signal used to control the analogue switch in the sample and hold circuitry,

resulted in the addition of a fourth chip in order to overcome this bug. The schematic of the ASIC based adult HR recorder is shown in Figure 5.1.

5.2.1. Improvements to the analogue circuitry.

The analogue front-end circuitry that is used in the ES2 ASIC based HR recorder is illustrated in Figure 5.2. Improvements made to the analogue front-end circuitry that is used in the FPGA version include, sharper filtering and a more robust R-peak detection scheme.

5.2.1.1. Instrumentation amplifier with filtering

The instrumentation amplifier of the ASIC based recorder contains low pass filtering around the differential amplifier (INST3) as well as high pass filtering in the feedback (HP) (see frequency response in Appendix F). This new filtering combined with the existing bandpass filter provides a total bandwidth of 10 to 40 Hz. This bandwidth is the same as for the FPGA based instrument except that the cut-offs are sharper i.e. 40 dB/decade rather than 20 dB/decade as the filtering contains four poles and two zeros rather than two poles and one zero. Sharper filtering helps to further reduce the effects of baseline drift and power line interference (50 Hz), while enhancing the frequency components of the R-wave.

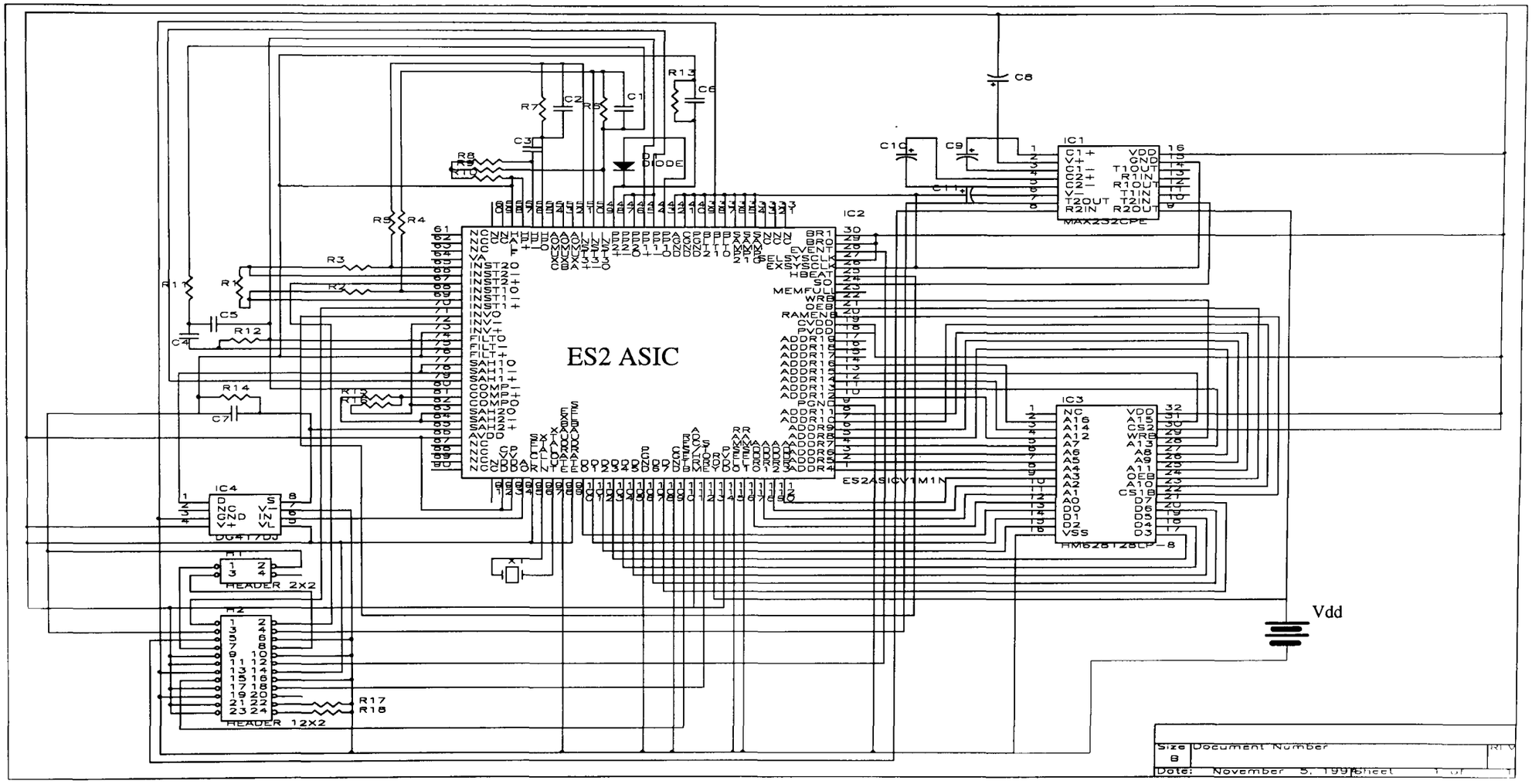


Figure 5.1: Circuit diagram for ES2 ASIC based adult HR recorder.

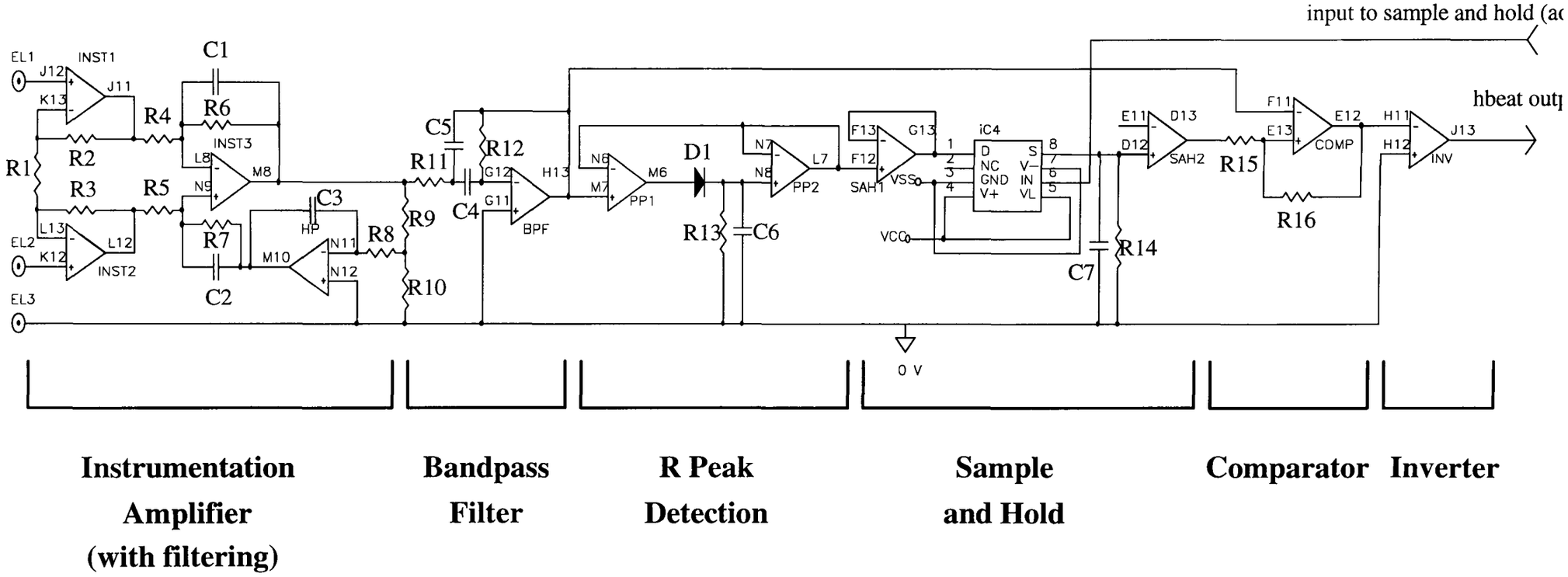


Fig. 5.2: Analogue front end circuitry for ES2 ASIC based adult HR recorder

Component	Value
R1	270Ω (all resistors < 5 % tolerance)
R2 - R7	20K
R8 - R9	510K
R10	100K
R11	18K
R12	330K
R13	68K
R14	620K
R15	62K
R16	470K
R17	1.2K
R18	1.6K
C1 - C2	0.22μF (polyester - 10 % tolerance)
C3	4.7nF (ceramic - 10 % tolerance)
C4 - C5	0.1μF (polyester - 10 % tolerance)
C6	1μF (polyester - 10 % tolerance)
C7	22μF (tantalum - 20 % tolerance)
C8 - C11	10μF (tantalum - 20 % tolerance)
IC1	MAX232CPE
IC2	ES2 ASIC
IC3	128K x 8 SRAM (HM628128LP-8)
IC4	Analogue switch (DG417DJ)
D1	Diode (OA47)
X1	19.6608 MHz crystal (IQD A182A)
H1	Ribbon cable header (2 x 2) to batteries
H2	Ribbon cable header (12 x 2) to switches, I/Os etc
power supply	+/- 2.5 V (4 x AA cells)

Table 5.1: Component values for ES2 ASIC based adult HR recorded

5.2.1.2. R-peak detection circuit

The performance of the R-peak detection circuitry used in the FPGA based instrument is limited by two factors. Firstly, the inability of the NE5537 sample and hold IC to produce an R-peak detection threshold of less than 1.4 V. This problem leads to the inability of the circuitry to detect the heart beat of subjects whose electrocardiogram (ECG) is of a particularly small amplitude. This is because, the 70% value of the R-peak amplitude, after amplification, fails to exceed this 1.4 V threshold, for these particular subjects. One solution to this problem would be to increase the gain of the front end so that every subject's

R-wave amplitude exceeds the threshold. However, an increase in the front end gain would also cause saturation to occur for other subjects whose R-peak height is much greater than the threshold after amplification.

The ASIC based instrument overcomes this minimum threshold problem by dispensing with the NE5537 and replacing it with a sample and hold circuit made up of two ES2 op-amps and an analogue switch. This circuit can have a threshold as low as 0 V, as the analogue switch is powered from +/- 2.5 V. As mentioned previously, the sample and hold circuit originally intended to use an ES2 analogue switch on the ASIC. Unfortunately, an error in the ASIC design (see section 5.2) rendered the analogue switch on the ASIC useless, and so an external analogue switch IC was used, namely the DG417DJ device.

The second limitation of the FPGA based recorder's R-peak detection capabilities lies in the large time constant that is associated with the hold section of the sample and hold circuit. In the FPGA based instrument (see Figure 3.4) the 0.1 μF capacitor used to store the sampled voltage has no parallel resistor, through which to discharge. If the sample and hold circuit samples a particularly large R-peak or noise spike, which is subsequently followed by several much smaller R-peaks, then a problem of missed beats can occur. This is caused by the threshold being set far too high for the normal R-peak amplitude by the previous uncharacteristically large R-peak or noise spike. Eventually the threshold voltage will discharge through parasitic resistances so that a normal R-peak amplitude will trigger the R-peak detection threshold. This 'recovery time' can be greatly reduced by inserting a suitable resistance in parallel with the hold capacitor. This modification has been implemented with the ASIC version of the recorder. The choice of resistor value should be such that the R-peak threshold voltage will decay substantially within several heart beats, in order that minimal missed beats occur. If the time

constant is set too low then there is a danger that the threshold will decay too rapidly and false detections may occur. The combination of a 22 μF capacitor with a 620 KΩ resistor has a time constant of 13.64 seconds, which satisfied the above conditions.

5.2.1.3. Other modifications to analogue circuitry.

Two other modifications to the FPGA version that have been implemented in the ASIC based instrument are a reduction of the R-peak detection time constant and an inversion of the heart beat output of the comparator. This first modification is to take account of the reduction in the length of the fixed count (see section 3.2.2) of the R-R interval timing circuitry in migrating from FPGA to ES2 ASIC. The pros and cons of this change will be discussed later in this chapter (see section 5.2.2.1). The second modification is needed to fix an error caused by an over-sight when transferring the digital FPGA circuitry to the ASIC.

In moving from FPGA to ASIC the fixed count was reduced from 160 ms to 52 ms (see section 5.2.2.1). In order to maintain a threshold at around 70 % of the R-peak amplitude, the time constant of the R-peak detection circuit therefore needs to be reduced from 0.3 s to 0.1 s:

While developing the FPGA based instrument, the comparator circuit was enhanced from a simple comparator to a version with hysteresis. This was needed to overcome a problem of multiple heart beat detections, caused by a 'noisy' output signal from the sample and hold circuitry. The move from a comparator without hysteresis to a comparator with hysteresis, had the result of providing a falling edge heart beat output, as opposed to a rising edge heart beat output. As the FPGA had already been programmed to expect a positive going edge, an extra external inverter was used to interface the output of the

hysteresis comparator to the FPGA. When migrating the FPGA design to the ASIC design this extra external inverter was mistakenly omitted from the ASIC circuitry. This problem was solved by implementing the inversion of the heart beat pulse using a spare ES2 op-amp. This avoids the need for an external inverter, which in turn prevents any increase in recorder size, that an extra IC would entail.

5.2.2. Improvements made to the digital circuitry

The two improvements made to the digital circuitry are a reduction in the length of the fixed count, from 160 ms to 52 ms, as well as a reduction in the interval between time markers, from 14.56 mins to 1.82 mins.

5.2.2.1. Reduction of the fixed count

The fixed count occurs straight after the arrival of a heart beat pulse from the analogue front end. During this period all other potential heart beat pulses are masked out while various operations are carried out (see section 3.2.2). These operations include the writing of the R-R interval count to RAM, the resetting of the R-R interval counter and the setting of a new R-peak detection threshold. The longer the fixed count the greater the possibility of true R-peaks being masked out and therefore undetected.

It is important to minimise the length of the fixed count in order to prevent errors being introduced due to false detections. If a spurious noise spike were to occur 100 ms before a genuine R-peak, the FPGA based instrument would detect the spike as a valid R-peak. Once an R-peak is detected, any other potential R-peaks occurring during the following 160 ms would be masked out by the R-peak detection scheme and so the genuine R-peak would go undetected. Applying the same scenario to the ES2 ASIC based instrument would result in both the spurious noise spike and the genuine R-peak being

detected, as the fixed count has been reduced from 100 ms to 52 ms. Although this would still cause an error in the R-R interval data, it is an error that may be corrected later by looking at the R-R interval trend to see which of the two possible R-peaks is most likely to be genuine.

The minimum length that this fixed count can be before the next R-peak is sought, is limited by two factors. Firstly, if the next R-peak search begins as soon as an R-peak is detected, then the R-peak detection threshold is likely to be exceeded by the same R-peak that has just been detected. It is therefore important to ensure that the amplitude of the R-peak, which has just been detected, has fallen well below the R-peak detection threshold, before the next R-peak is sought. With this in mind, a fixed count that is greater than the width of an R-peak (about 40 ms) should be sufficient.

The second factor is due to the R-peak detection threshold being obtained by sampling at about 70% of the R-peak height. In order to achieve this, the R-peak follower part of the R-peak detection circuit needs to have decayed to around 70% of the R-peak height before it is sampled. This second factor also suggests that it would be wise to chose a fixed count length that is at least the width of an R-peak together with an appropriate R-peak follower time constant.

5.2.2.2. Reduction of the interval between time markers

In the FPGA based recorder, R-R intervals are tagged with a time marker every 14.56 minutes. The time markers are useful when displaying HR data on a real time axis rather than against beatnumber. This is particularly the case when the HR data contains unrecoverable errors i.e. more than just simple missed beats and false detections. A substantial amount of unrecoverable errors will cause a time axis, that is produced by a cumulative addition of the R-R intervals, to

become distorted. Any distortions in a cumulative time axis will become apparent when compared against the time markers. The interval between time markers for the ES2 ASIC based instrument was reduced to 1.82 mins in order to increase the resolution of the time axis, such that any unrecoverable R-R interval errors can be located more effectively.

5.3. Validation of HR data and initial testing

The accuracy of the ES2 ASIC based HR recorder was checked by recording HR simultaneously with the raw ECG. The raw ECG was recorded using the general electrophysiological signal recorder (Mode 2), described in Chapter 6. The HR was extracted visually from the recording of the full ECG by measuring the time location of each R-peak. The results of the validation exercise are presented in Table 5.2. These results are taken from a set of eight successive R-R intervals and show that the HR recorder has an accuracy of between 1 and 2 ms. The raw ECG was recorded at a sampling frequency of 600 Hz (13 bit) which has a time resolution of 1.67 ms and may explain some of the small discrepancies between the two recordings.

R-R interval number	ECG derived (Mode 2)	HR recorder (Mode 1)
1	830 ms	830 ms
2	792 ms	790 ms
3	788 ms	789 ms
4	800 ms	799 ms
5	812 ms	813 ms
6	822 ms	822 ms
7	787 ms	787 ms
8	763 ms	762 ms

Table 5.2: Validation of HR recorder by simultaneous recording of the full ECG.

During the validation exercise a design flaw was observed when downloading recorded data to PC. The downloading procedure is controlled by software running on the PC. Initially recorded data was stored to disk in a series of blocks. As the data in RS-232 format is received it is first stored in a temporary buffer. Once the buffer is full, transmission of new data is interrupted and this block of data is written to file on the hard disk. The buffer is then cleared and transmission of data resumes. Occasionally data would be lost at the beginning of a block of data. This is possibly caused by inadequate handshaking between recorder and PC.

The problem was overcome by altering the software which controls the downloading. Instead of storing the data in a series of blocks the program was changed so as to store the data in a single block. This means that any lost data will only occur at the very beginning of the recording. The maximum size of any temporary buffer is limited by the availability of the PC's conventional memory (maximum 640 K)

A further problem was encountered concerning the time markers. Occasionally these markers did not appear in the downloaded data, resulting in a doubling of the interval between time markers. It was also observed that these markers did not synchronise with the start of the HR recording. The first problem could be caused by the time marker coinciding with the R-R interval fixed count. The time marker may occur just after the high byte is written to RAM and just before the R-R interval is cleared. The second time marker problem is probably due to the circuitry used to reset the time marker count.

5.4. Results

Once built, tested and validated, the ES2 ASIC based HR recorder was used to investigate the author's long term daily HR. This consisted of 54 long term

recordings, with each recording averaging around 8 hours in duration. A photograph of the adult HR recorder is included in Appendix D. Of the 54 recordings in total, 30 were made during the night, usually between midnight and 8.00 am. Out of the remaining 24 recordings, 21 were made on weekdays, 2 were made at the weekend and 1 recording was made during a weekday evening. Virtually all the weekday recordings occurred while the author was undertaking a normal working day. On the whole, these recordings were made between 9.00 am and 5.00 pm. Three disposable, foam backed, silver-silver chloride, solid gel electrodes (3M 2237) were used in all the HR recordings. Before attaching the electrodes, the subject's skin was prepared with an alcohol saturated swab and left to dry for around 5 minutes. The two differential input electrodes were positioned on the subject's chest as recommended by Thakor and Webster (1985). The third 'common' electrode was placed just above the subject's right hip.

5.4.1. Displaying the results

In this section HR results are presented in three different formats: HR versus beatnumber scatter plots; R-R interval spectral plots; and R-R interval histograms.

HR versus beatnumber scatter plots are useful for investigating accelerations and decelerations as well as changes in the HR baseline. Spectral analysis is useful for detecting the presence of the particular frequency components of HRV that are associated with the autonomic nervous system. R-R interval histograms are a useful method of investigating more general HRV, with a tall thin histogram being representative of low variability.

The HR versus beatnumber scatter plots, plot every individual HR value in a recording against the relevant beatnumber. However, the limited resolution of

the screen (VGA), used to display the scatter plots (before being imported into this document via a bit map), results in several HR values being printed at the same x-axis location (many of the plots contain well over 30,000 beats). The fixed length of the x-axis (width of a page) leads to a different x-axis scale for each recording (dependent on the total number of beats). This method of displaying the time domain features of the recording is the simplest and neatest method of displaying the full recording on a single graph. As the majority of the recordings contain a similar amount of beats, comparisons between the plots are still valid. Comparisons between the time domain characteristics of recordings, which contain substantially more or substantially fewer beats, need to take this difference in x-axis scale into account.

All the R-R interval spectral plots are obtained using a spectral analysis software package developed by N.M. Gibson (1995). Each plot is produced by taking a frame of consecutive R-R intervals and transforming the data into the frequency spectrum, using the Maximum Entropy spectral estimation Method (MEM). Each frequency spectrum that is produced is plotted along the y-axis using a 16 bit grey scale. Consecutive spectra are plotted sequentially along the x-axis, in order to show how the frequency content of the R-R interval data varies with time, throughout the period of the recording. All the MEM derived frequency spectra that are displayed in this chapter are derived from a frame size of 50 beats and a model order of 20.

The R-R interval histograms contain all the beats in the recording separated into 200 bins, each 10 ms wide. The maximum R-R interval value of 2.0 s relates to a HR of 30 beats per minute (BPM), which is well below the normal HR for an adult.

5.4.2. HR patterns at night

In this section, examples taken from the 30 HR recordings made during the night, while the subject was asleep, will be presented.

5.4.2.1. HR versus beatnumber scatter plots.

An example of a typical night time HR pattern is given in Figure 5.3. This particular recording contains 28245 HR values, over a time period of 8 hours and 35 mins. As the author falls asleep his HR falls from an average of over 70 BPM to an average of less than 60 BPM, over a time period of around 30 mins. Once asleep, the average HR remains somewhere between 50 and 60 BPM for the remainder of the night, until the author begins to wake up, at which point the average HR begins to increase towards 70 BPM.

During the night a typical HR trace shows many short term accelerations, with the instantaneous HR often exceeding 80 BPM for several beats at a time. The frequency of these accelerations tends to increases with time. As well as these short sharp accelerations, a typical, night time HR trace often contains several more sustained accelerations and decelerations, which appear in the scatter plots as sudden changes in the HR baseline. The most graphic example of this phenomena can be seen in the night time recording presented in Figure 5.4.

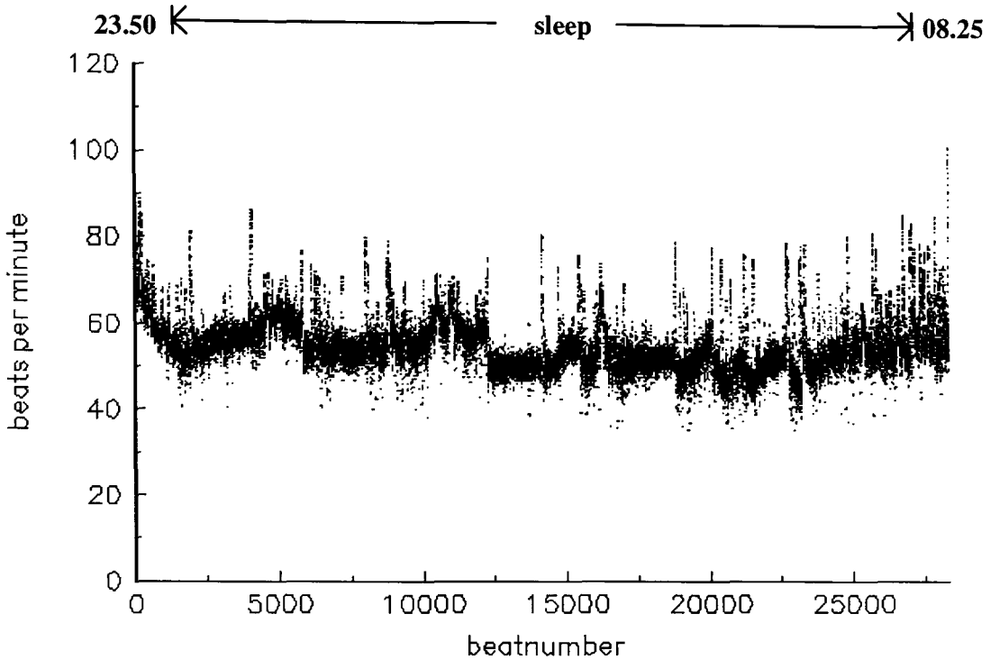


Figure 5.3: Typical HR versus beatnumber scatter plot during sleep.

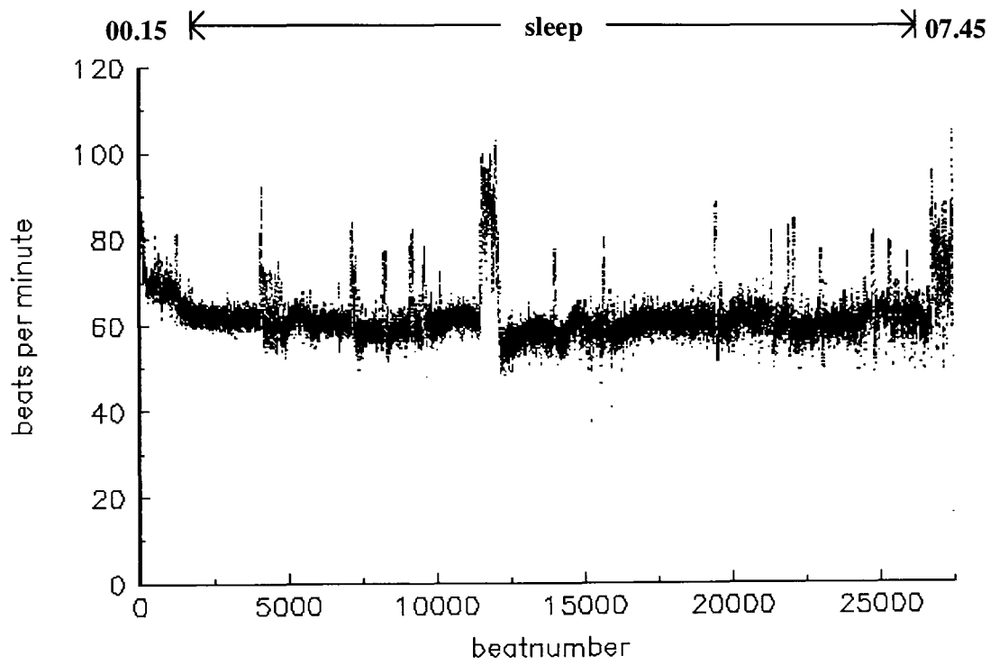


Figure 5.4: HR versus beatnumber scatter plot showing a sudden, sustained increase in HR while asleep.

5.4.2.2. R-R interval spectral plots

All the recordings of HR at night displayed a strong frequency component at or around 0.3 Hz, for at least part of the record time. This component is associated with respiration, and is produced due to the action of the autonomic nervous system. A typical example of the presence of this component can be seen in Figure 5.5. The 0.3 Hz component in a typical recording is present for more than half of the total record time. Figure 5.6 shows a night time recording which contains the 0.3 Hz component for virtually the total record time of 8 hours.

Although the respiration frequency component is usually at about 0.3 Hz, the exact frequency often drifts around between 0.2 Hz and 0.4 Hz. This drifting effect can be seen in Figure 5.6 and was also found to occur in many of the other night time recordings not shown here. The lack of a true time axis for the R-R interval data could be a possible explanation for this effect, as many of the changes in frequency of the respiration coincide with accelerations and decelerations in HR. An example of a large change in respiration frequency can be seen at the beginning of Figure 5.7.

Several R-R interval spectral plots showed a tendency to be periodic i.e. the 0.3 Hz frequency component tends to appear and disappear at regular intervals. The periodic nature of the night time recordings is illustrated in Figure 5.8.

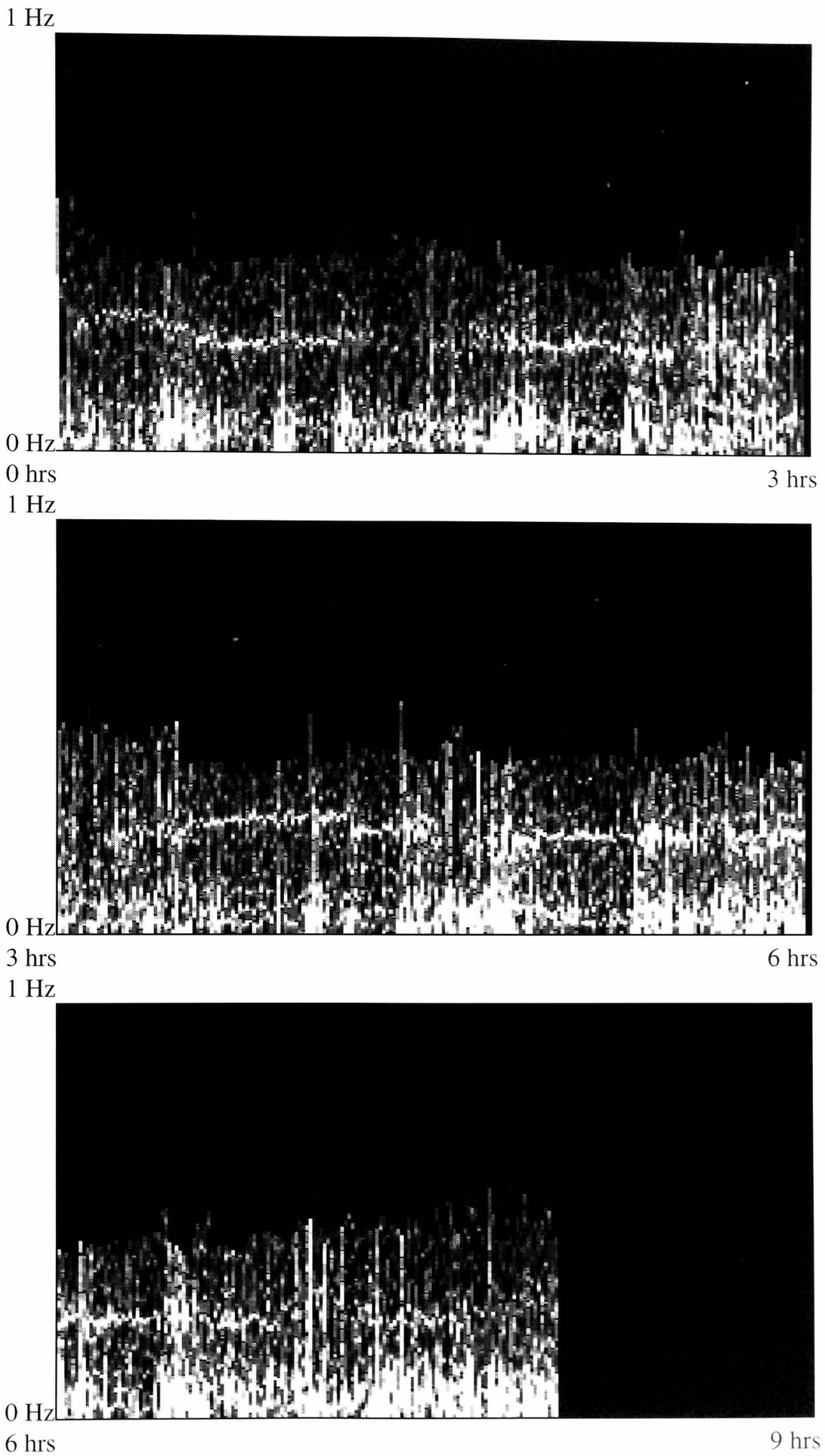


Figure 5.5: A typical night time R-R interval spectral plot containing 0.3 Hz component.

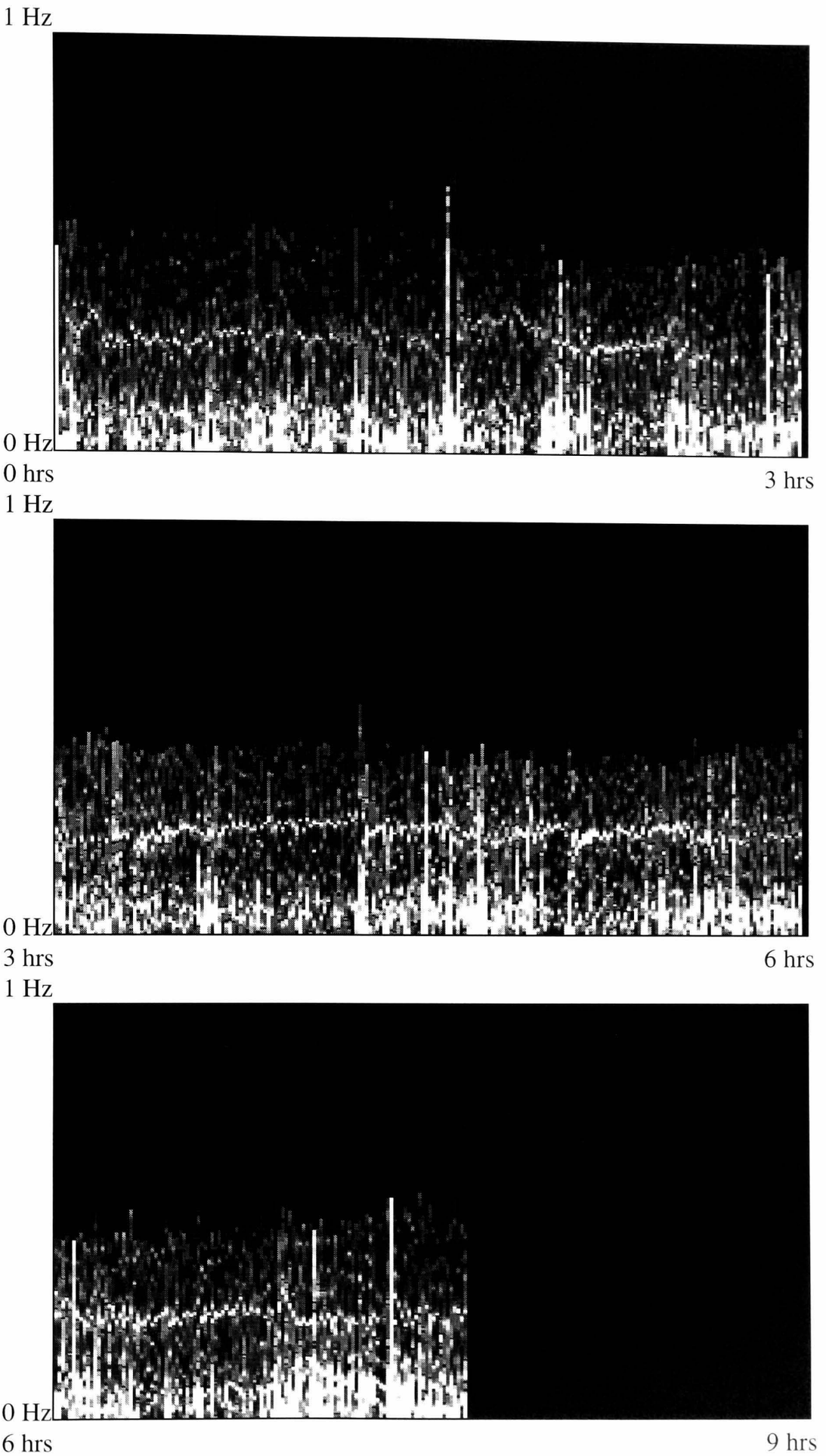


Figure 5.6: A night time R-R interval spectral plot with a 0.3 Hz component always present.

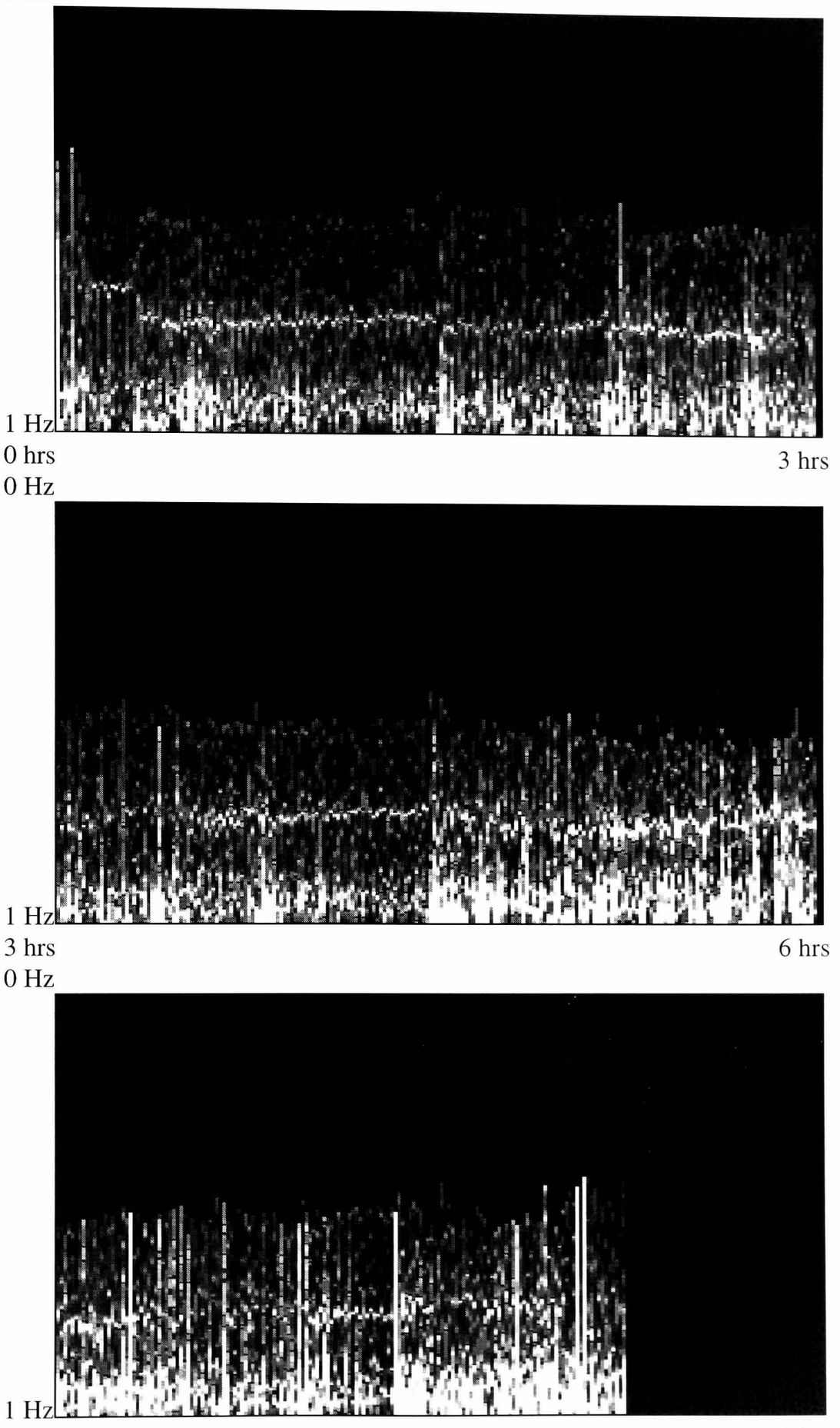


Figure 5.7:R-R interval spectral plot showing changing frequency of respiration component

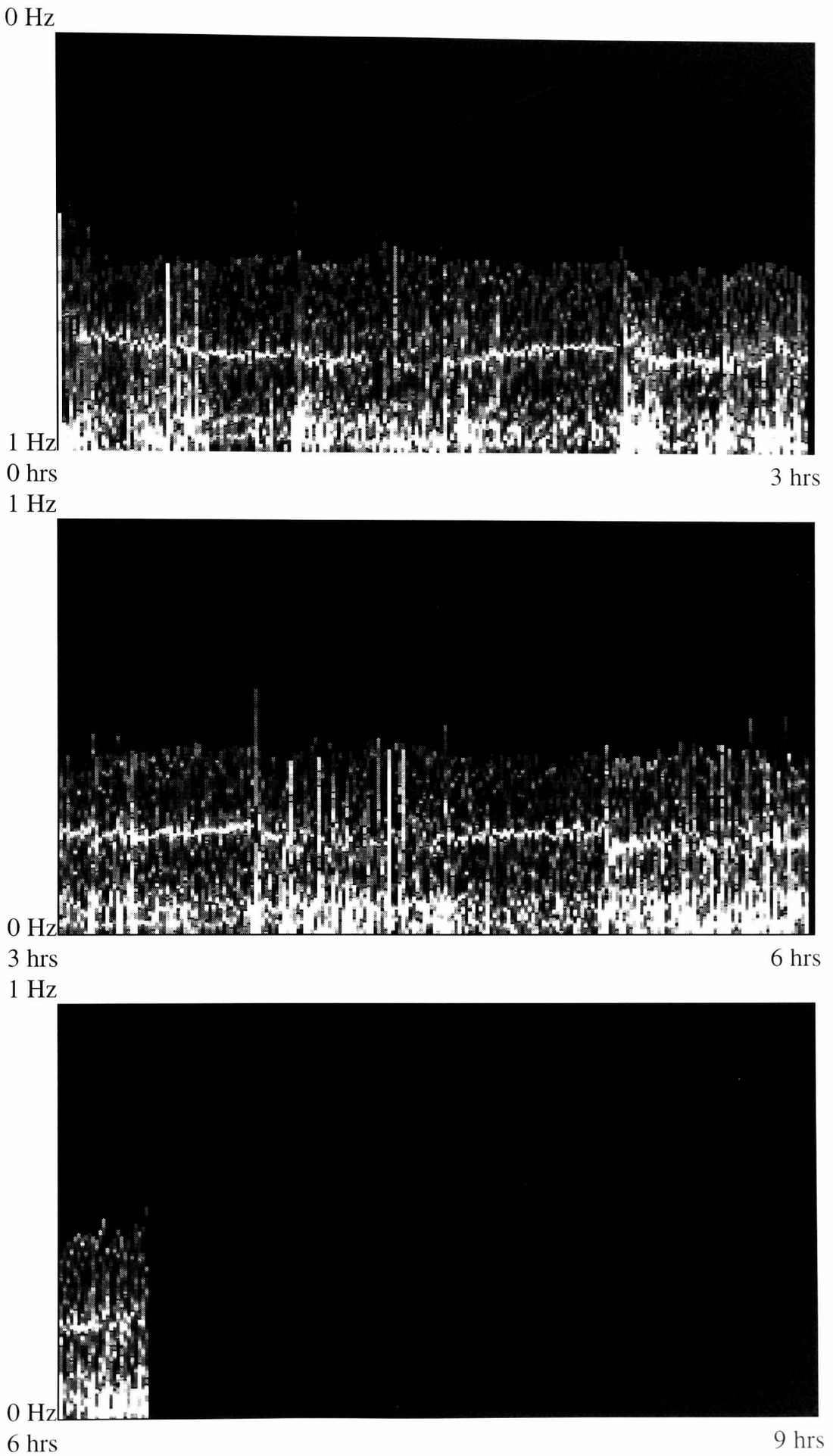


Figure 5.8: R-R interval spectral plot showing periodic occurrence of 0.3 Hz component.

5.4.2.3. R-R interval histograms

Figure 5.9 contains the R-R interval histogram of a typical night time recording. As can be seen the majority of the R-R values are in the range from 0.8 s to 1.4 s (75 BPM to 43 BPM) with the most common R-R interval values in the middle of this range, at around 1.1 s (55 BPM).

An interesting effect was observed when a night time recording followed shortly after the consumption of alcohol. On these occasions the R-R interval histograms showed a significant reduction in HR variability as well as an increase in HR distribution peak to around 68 BPM (0.88 s). The most graphic example of this loss of variability can be seen in Figure 5.10. On this particular occasion, 10 units of alcohol had been consumed, within a few hours of the beginning of the record time.

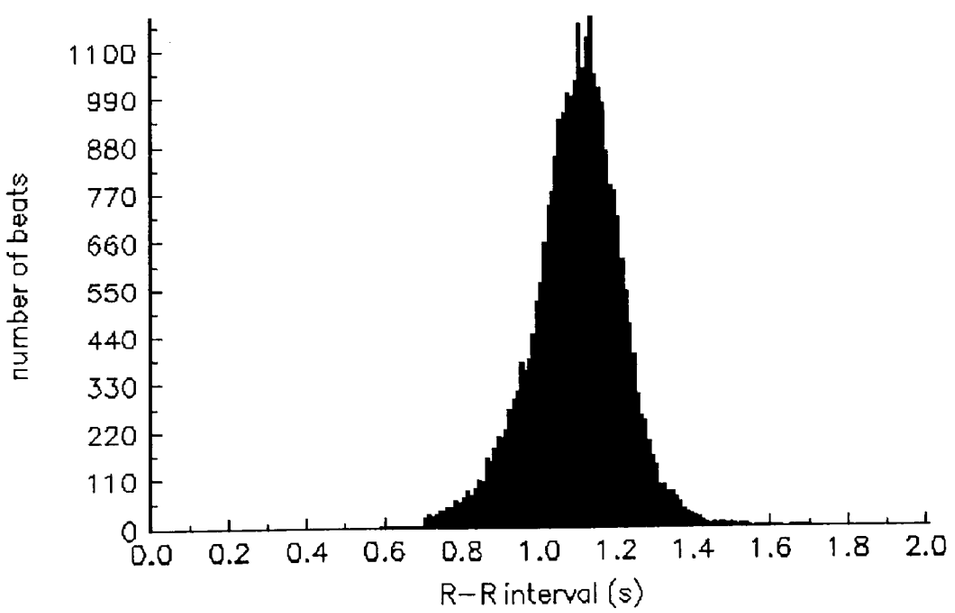


Figure 5.9: A typical night time R-R interval histogram.

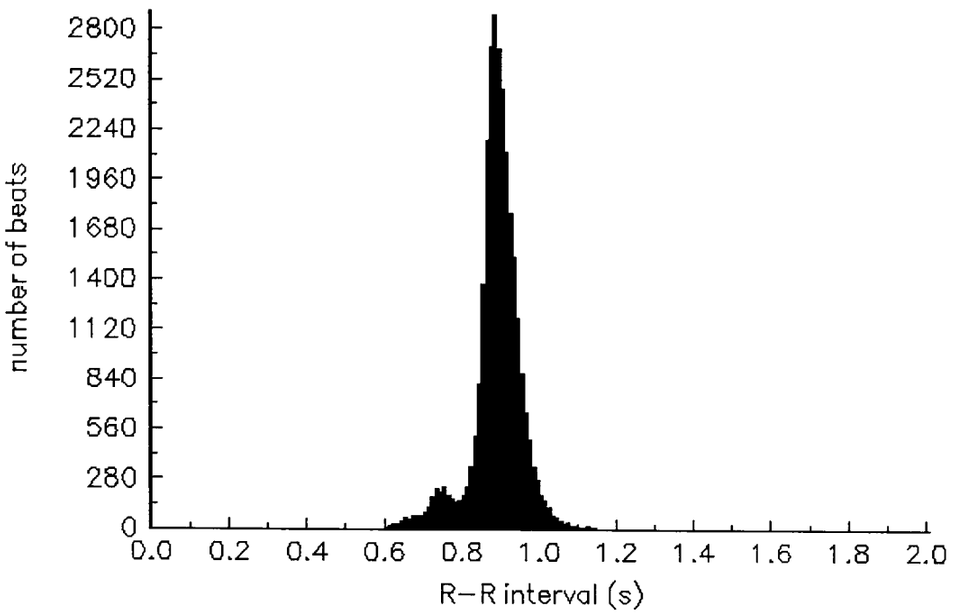


Figure 5.10: An example of the effect of alcohol on a night time R-R interval histogram.

5.4.3. HR patterns during the day

In this section, examples taken from the 24 HR recordings made during the day and evening, while the subject was awake, will be presented.

5.4.3.1. HR versus beatnumber scatter plots.

Most of the daytime recordings took place during the subject's routine working day in the research laboratory. The length of daytime recordings averaged around 8 hours, usually between 9.00 am and 5.00 pm. Laboratory activities mainly consisted of working at a PC and soldering at a work bench.

A recording of a typical working day is shown in Figure 5.11. The recording begins around 9.00 am, 45 mins after waking up, and 15 mins after taking a shower. Breakfast is eaten around 9.30 am and is shortly followed by the 10 mins walk to work. At about 11.00 am, the subject makes the short trip to the hospital and back, which is followed by lunch at around midday. The rest of the

afternoon is spent soldering in the laboratory. The recording is completed at around 5.00 pm, shortly before the subject returns home.

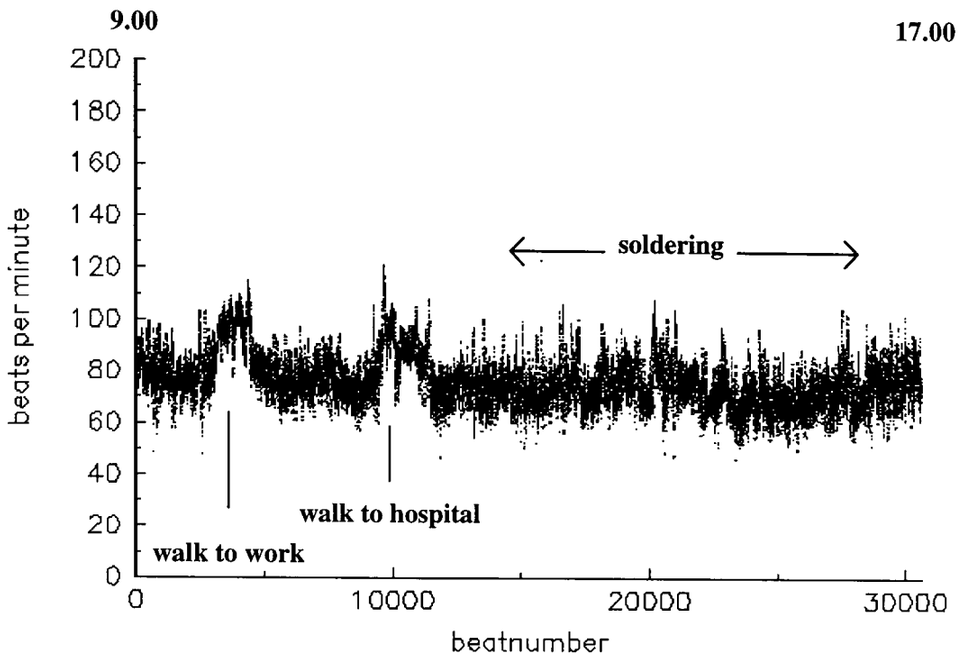


Figure 5.11: HR versus beatnumber scatter plot of a typical working day.

A scatter plot of HR variations during an evening is presented in Figure 5.12. The recording begins just after 6.00 pm, shortly before leaving the laboratory and returning home. After arriving home, the subject watches TV until tea is eaten at around 7.20 pm. From about 8.30 pm until the end of the recording at just after midnight, the subject sits at a desk and works on a PC. While working at the PC the subject consumes a strong cup of coffee at around 8.45 pm followed by around 3 units of alcohol about two hours later.

In general, an increase in HR coincides with a decrease in HR variability. This can be seen in both Figure 5.11 and Figure 5.12, when the subject is walking to and from work. Other examples of the effect of exercise on HR are illustrated in Figure 5.13 and Figure 5.14.

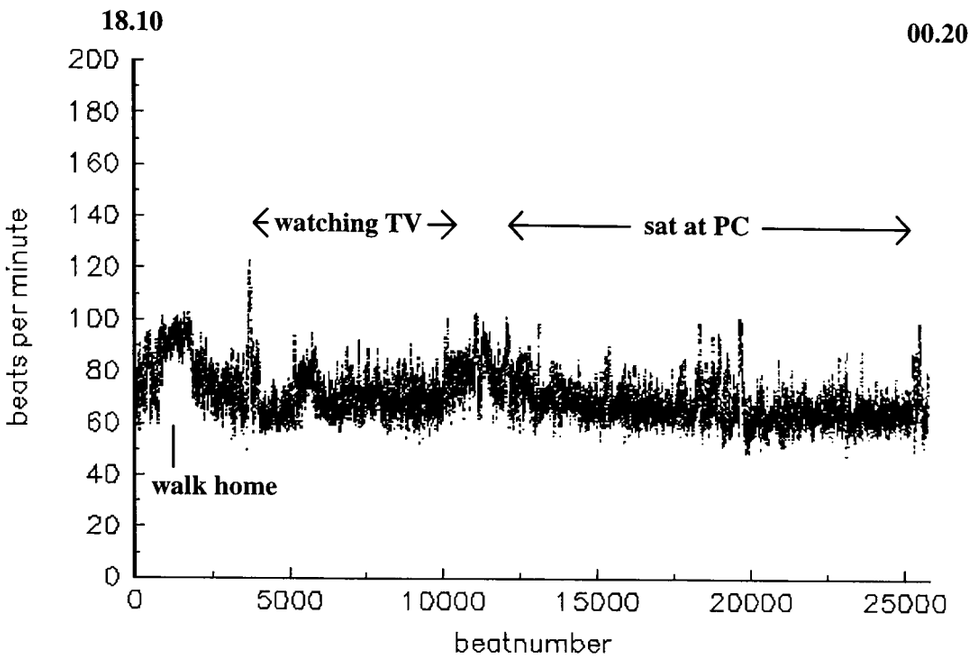


Figure 5.12: A scatter plot showing HR variation during an evening.

Figure 5.13 contains two, twenty minute cycle rides, during which the subject's HR averages around 130 BPM. The second cycle ride is followed by a game of cricket, in which the subject is part of the fielding team. At the very end of the recording the HR trace reaches 160 BPM as the subject bowls an over.

The HR recording in Figure 5.14 was made at the weekend and includes a 7 mile walk, which lasted around 3 hours. During the period of the walk the subject's average HR increased from around 70 BPM to around 80 BPM and remained fairly constant, at this level, for the duration of the walk. While walking the subject's HR contained marginally less variability. The reduction in variability was far less pronounced than for the recording of HR while cycling as can be seen in Figure 5.13.

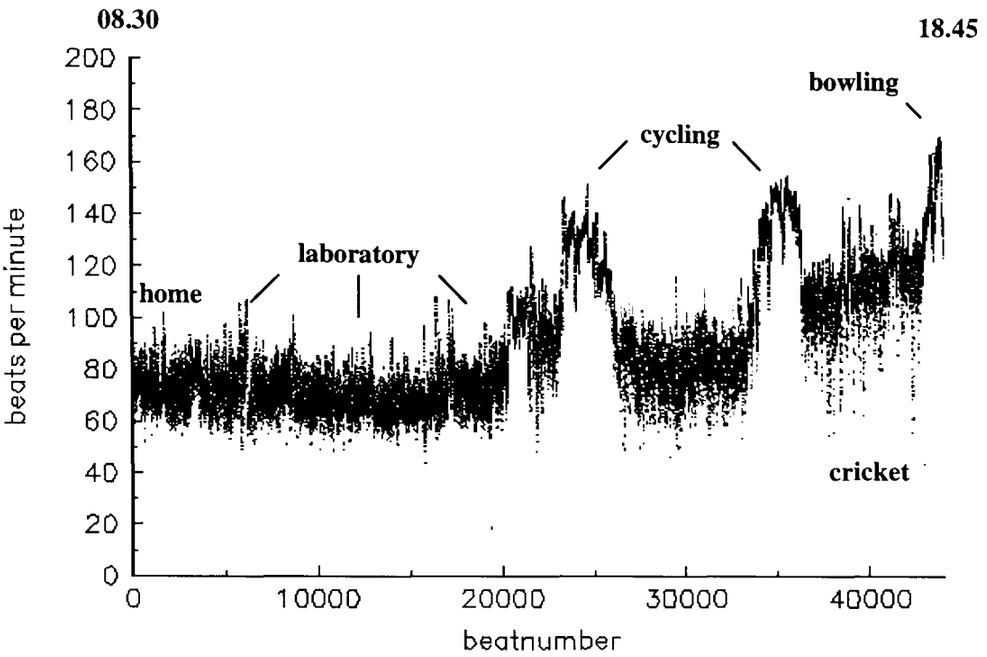


Figure 5.13: HR scatter plot when cycling and playing cricket.

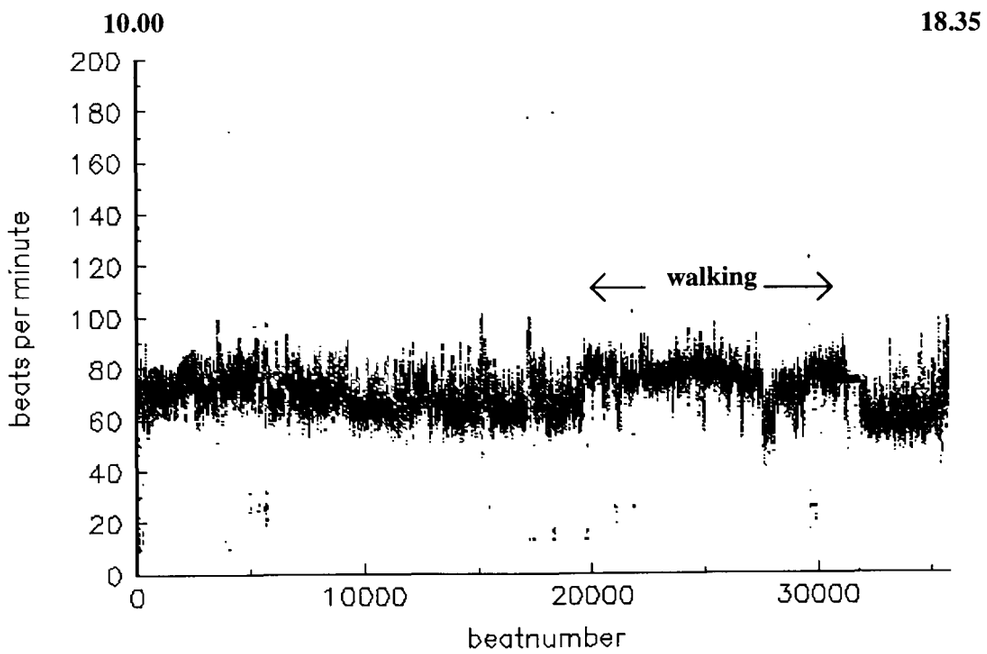


Figure 5.14: HR scatter plot while walking for 7 miles.

5.4.3.2. R-R interval spectral plots

Spectral plots of R-R interval recordings made during the day time show a frequency content with roughly a 1/f distribution. This can be seen in the spectral plot of a typical working day that is shown in Figure 5.15. Only one of the 23 day time recordings contained a strong 0.3 Hz component, as can be seen towards the end of Figure 5.16. However, the 0.3 Hz component can be seen in the evening recording that is shown Figure 5.17. In this recording the 0.3 Hz is strongest towards the end of the recording.

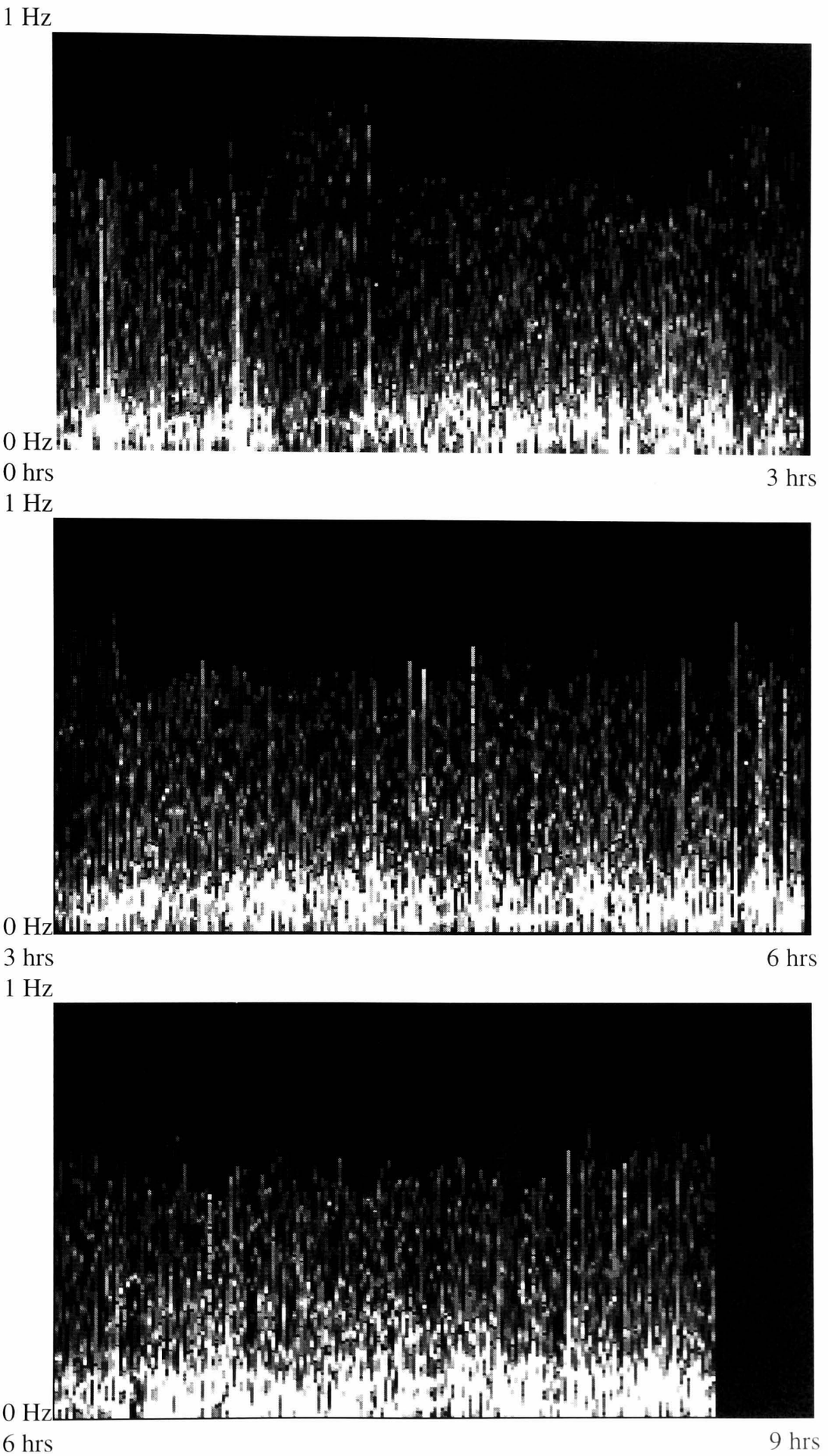


Figure 5.15: R-R interval spectral plot of a typical working day.

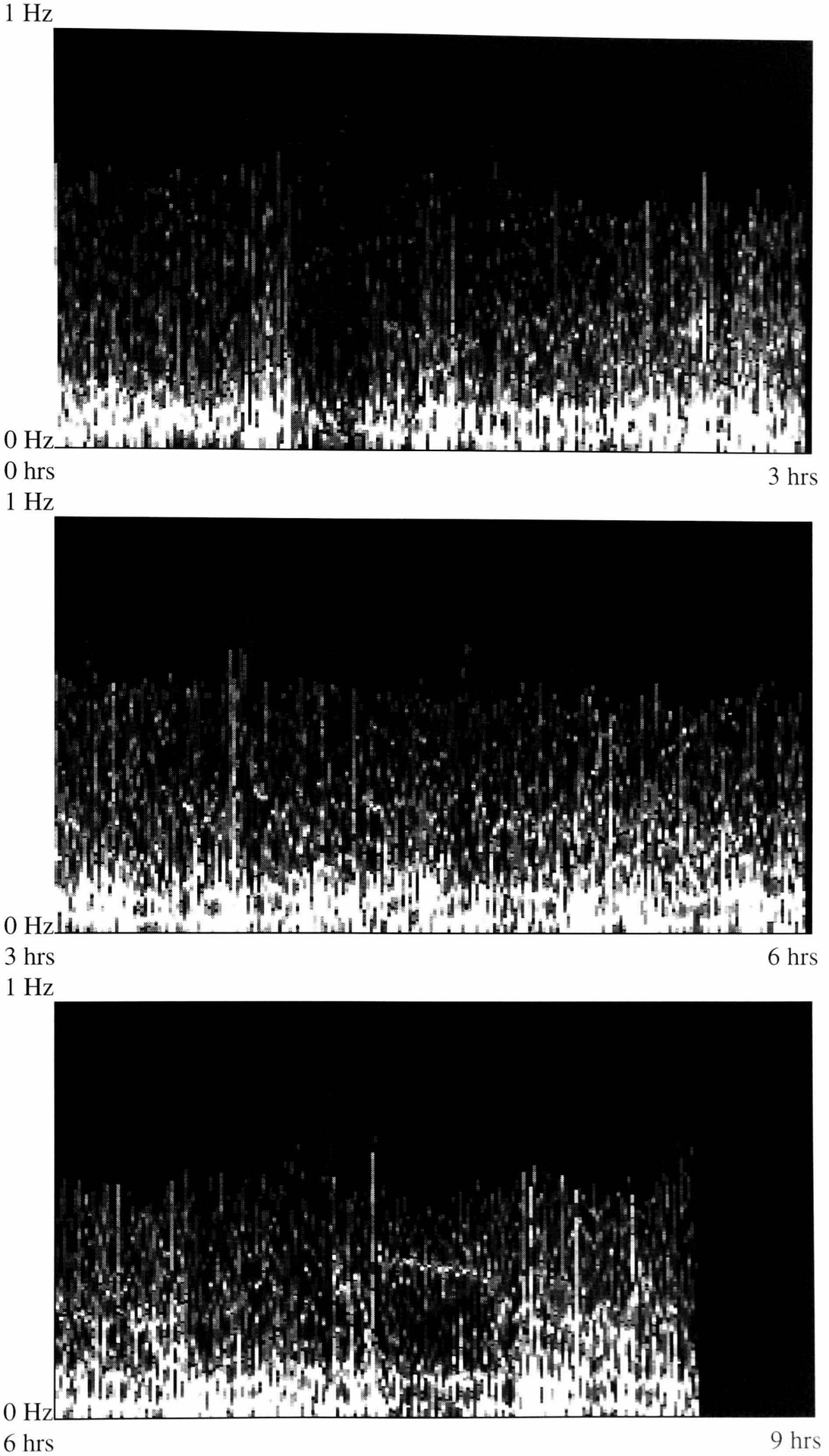


Figure 5.16: R-R interval spectral plot of a working day containing the 0.3 Hz component (bottom trace).

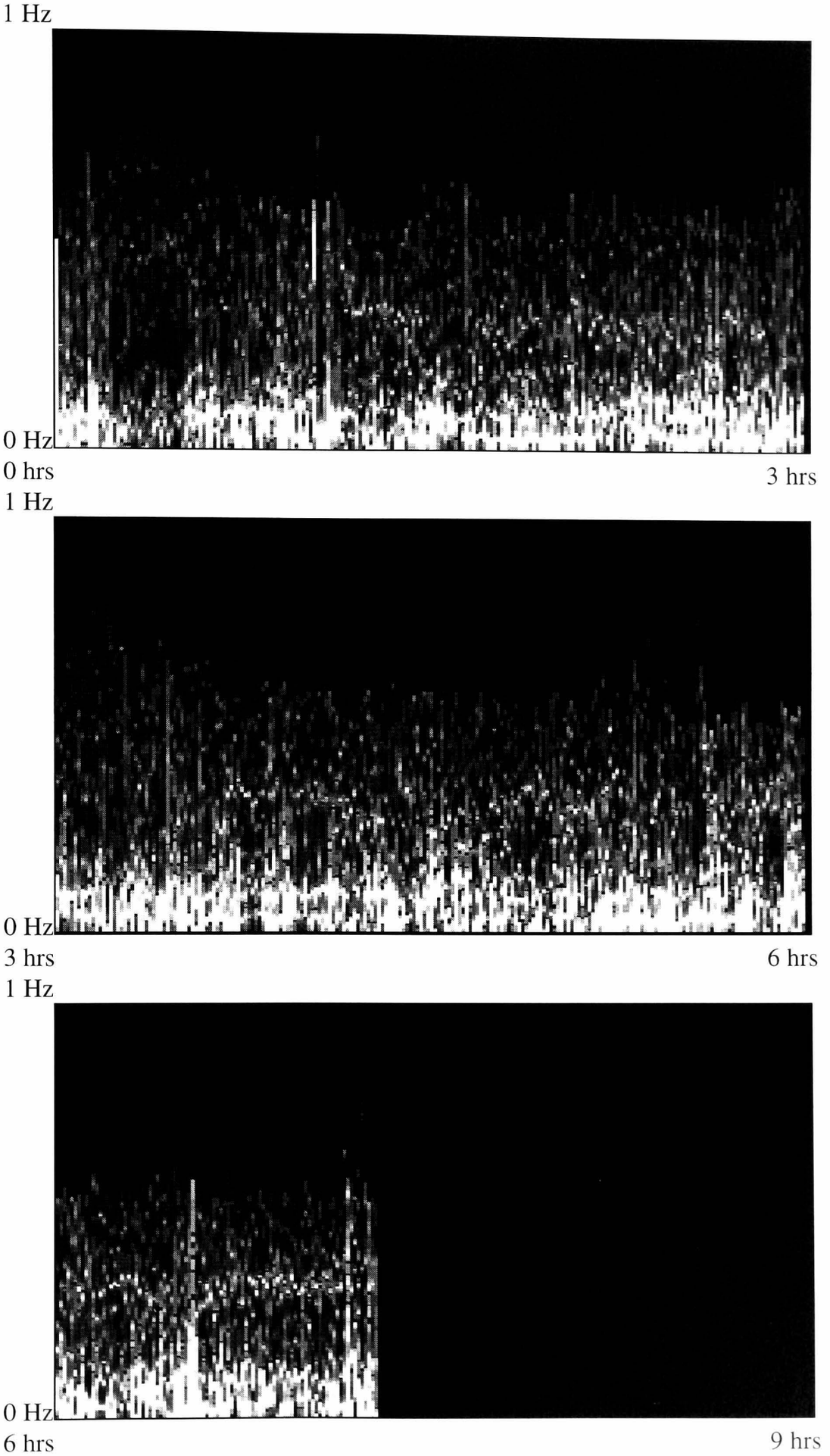


Figure 5.17: R-R interval spectral plot of an evening recording.

5.4.3.3. R-R interval histograms

Day time HR is generally in the region of 15 BPM higher than night time HR with a typical R-R interval range of between 0.6 s and 1.0 s (60 BPM to 100 BPM). A typical example of an R-R interval histogram from a working day is shown in Figure 5.18. The R-R interval histogram of the evening recording that is shown in Figure 5.19 is very similar to that of a typical working day.

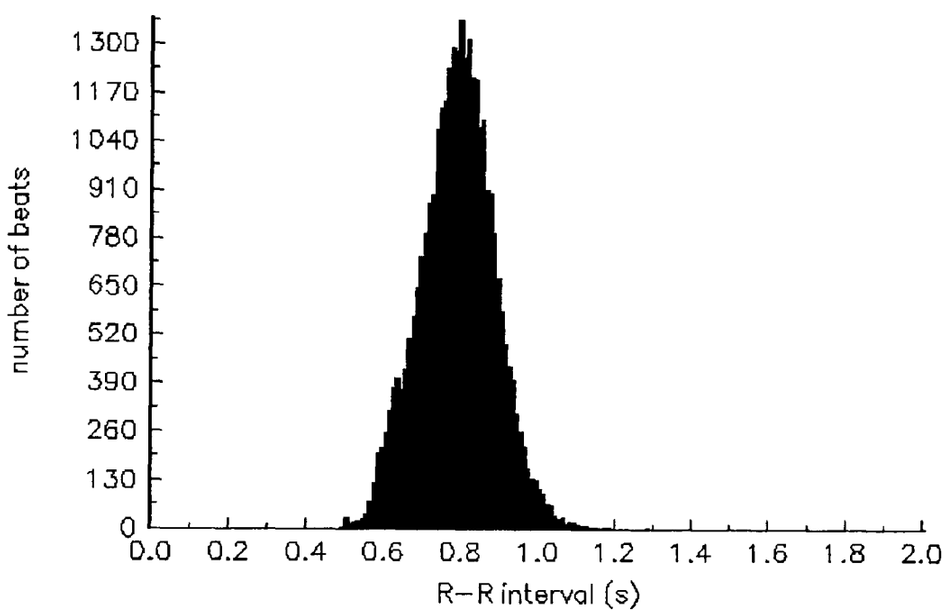


Figure 5.18: R-R histogram of a typical working day.

The biggest differences in day time R-R histograms can be found in recordings which contain significant periods in which the subject was exercising. This is most graphically illustrated in Figure 5.20 which corresponds to the day in which the subject cycled and played cricket. Figure 5.20 contains a histogram with two very distinct peaks. The lower peak relates to the R-R intervals recorded during periods of exercise, whereas the higher peak is much more similar to the R-R interval histogram of a typical working day as can be seen in Figure 5.18. Another example of the effect of exercise on an R-R interval histogram can be seen in Figure 5.21, which corresponds to the recording that was made at the weekend and includes a 3 hour walk.

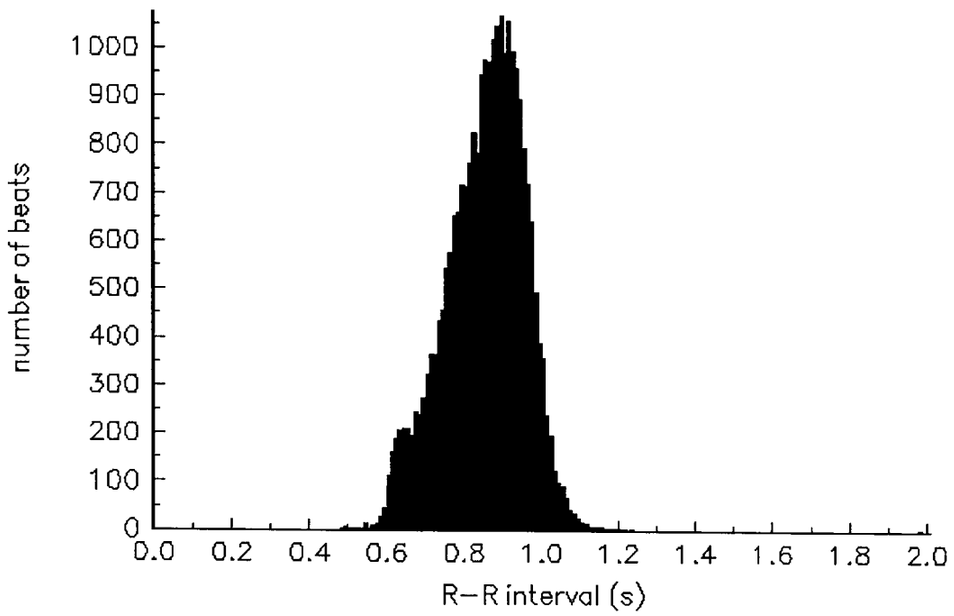


Figure 5.19: R-R interval histogram of an evening recording.

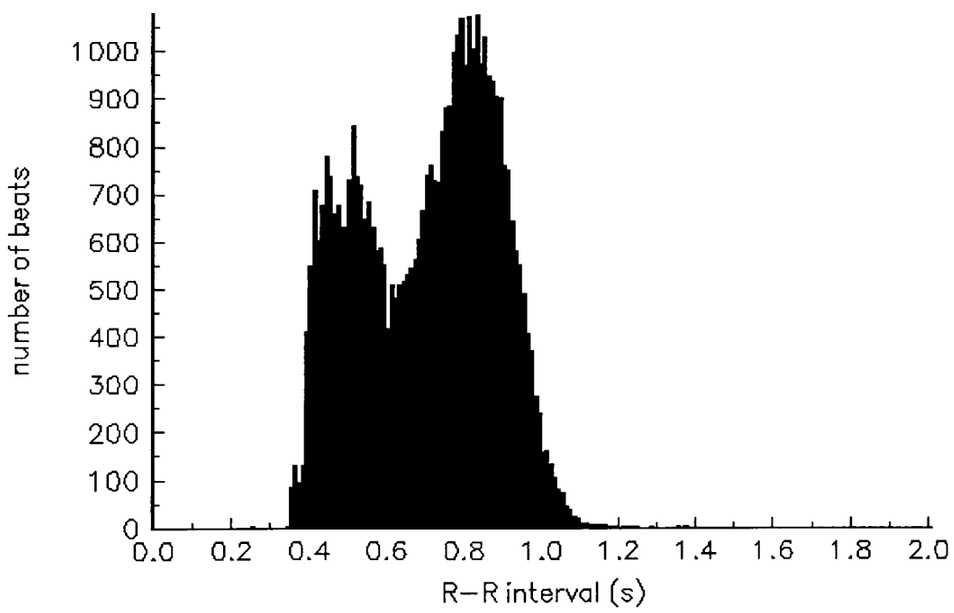


Figure 5.20: R-R interval histogram of a recording that includes cycling and cricket.

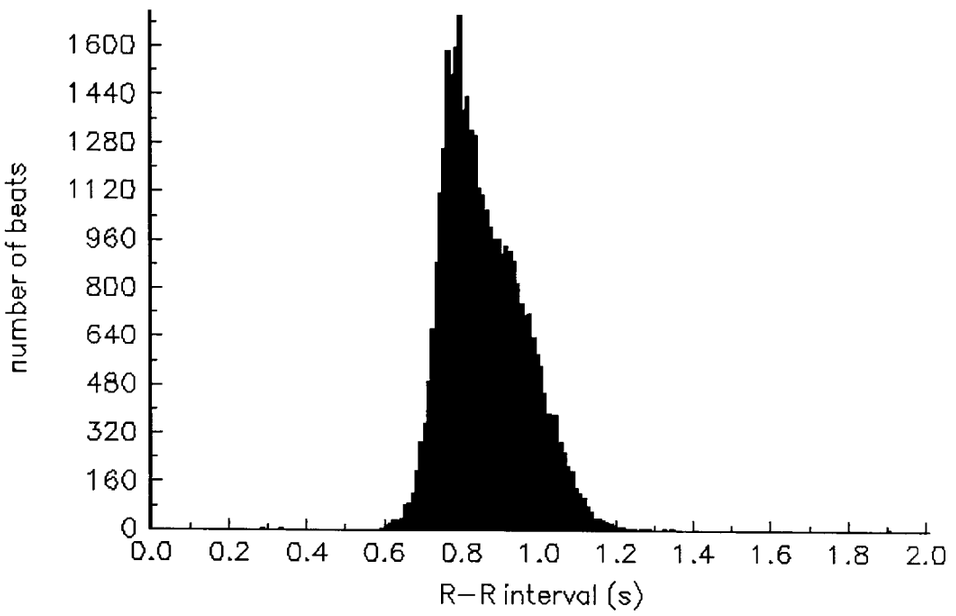


Figure 5.21: R-R interval histogram of a weekend recording including a 3 hour walk.

5.5. Conclusions

An ambulatory long-term recorder of beat-to-beat adult HR incorporating an ES2 ASIC has been constructed in order to investigate the suitability of ASICs for long-term ambulatory monitoring. A long-term study of the author's daily HR patterns has been undertaken which has verified the ambulatory nature of this instrument as well as its ability to cope with vigorous exercise, including a cycle ride and a 7 mile walk. Although there are many ambulatory instruments currently available capable of recording long-term HR (i.e. Holter monitors), their use in studying the long-term daily HR patterns of normal subjects is not usually reported.

The long-term HR study included a total of 54 recordings (over a five week period) which averaged 8 hours in duration. This consisted of 30 night time recordings and 24 daytime recordings, with, on average, the recorder being worn for 16 out 24 hours. In general, daily HR patterns were found to be most

heavily dependent upon the level of subject activity. As activity levels increase, average HR increases and HRV decreases. The effect of activity on HRV is illustrated by the strong 0.3 Hz respiration component of HRV found in each of the 30 night time recordings, when activity is at a minimum. In contrast, the same component appeared only once in recordings made during the working day. The presence of this component in the R-R interval spectral plots demonstrated that the ASIC based HR recorder possess the necessary R-R interval measurement accuracy to be capable of picking up such components and is therefore a suitable instrument with which to investigate HRV. A further feature of the long-term HR study was observed in several different recordings of night time HR. On these occasions, a reduction in HRV was found to occur following the consumption of alcohol

The instrument used in this study was constructed on veroboard, using point-to-point wiring and then enclosed in a pocket sized, plastic case (155 mm x 90 mm x 30 mm), that includes a battery compartment for four AA cells (see Appendix D). This version is capable of storing up to 65,536 consecutive R-R intervals which is sufficient capacity for just over 12 hours of data, given a HR of 90 BPM. The instrument has a battery life of 20 hours when powered with four fully charged NiCd AA batteries (0.8 Ah).

Following the successful operation of the HR recorder during the long-term study a further two PCB based instruments have been built for the Department of Cardiovascular Medicine, Queen's Medical Centre, Nottingham. The storage capacity of these two instruments has been increased by a factor of four which is sufficient for just over 48 hours of continuous beat-to-beat HR, given a HR of 90 BPM. In order to take advantage of this increased capacity it is necessary to use four fresh alkaline AA cells (2.7 Ah), giving a battery life of 67.5 hours.

One possible investigation requiring a 48 hour record time would be an investigation into the effect on HR of wearing an ambulatory recorder. The hypothesis being that for the first few hours a patient who has never use an ambulatory monitor will be very aware of its presence, to such an extent that HR may be affected.

It is appreciated that similar instruments to the one described in this chapter already exist which are capable of recording long-term beat-to-beat HR (i.e. Holter monitors). This instrument records only R-R intervals and does not differentiate between normal and abnormal ECG morphologies, which may limit its performance when used on cardiac patients. However, it must be stressed that the aim was to test the suitability of ASICs for ambulatory monitoring applications, whilst constructing a recorder which may be used for HRV studies (noting its limitations) within the Medical Electronics group at Nottingham. In addition, the low cost (< £200) and increased record times (> 48 hours @ 90 BPM) may still prove attractive where the long-term beat-to-beat HR patterns of normals or diabetics are of interest.

CHAPTER 6

GENERAL ELECTROPHYSIOLOGICAL SIGNAL RECORDER AND FECG RECORDINGS

6.1. Introduction

This chapter is concerned with the development of a general electrophysiological signal recorder using the European Silicon Structures (ES2) application specific integrated circuit (ASIC). It is intended that the final instrument will include a digital signal processor (DSP) on which electrophysiological signals that have been digitised by the ASIC can be processed in real time. One application of such an instrument is as a long-term ambulatory recorder of antepartum (before labor) fetal heart rate (FHR) and maternal HR (MHR), derived from the abdominal fetal electrocardiogram (FECG). As an intermediate step, a recorder capable of storing digitised electrophysiological signals directly to static RAM (SRAM) has been built and used to investigate the quality of abdominal FECG signals that can be obtained with such an instrument. Therefore, as well as a vehicle to test the suitability of ASICs for ambulatory monitoring, the instrument described in this chapter has been used to record data of significant clinical interest.

This chapter includes an introduction to FHR monitoring, a description of the recorder's operation and a results section, in which recordings of the raw abdominal FECG and examples of FHR and MHR traces extracted from these recordings, are presented.

6.2. FHR monitoring

Monitoring of the FHR is a routine procedure during both the antepartum and the intrapartum periods of pregnancy [Spencer, 1994]. FHR can be used to

assess fetal condition during labour, as it is an indirect measurement of the amount of oxygen being supplied to the brain. The cardiotocograph (CTG), which produces a record of FHR and uterine contractions, has become the primary means of monitoring for potential cases of fetal hypoxia. The FHR trace of the CTG can be obtained by either Doppler ultrasound or from the direct FECG, which is the electrophysiological signal produced by the electrical activity of the fetal heart. During labour, the most reliable FECG signal is obtained via a scalp electrode, connected directly to the baby's head [Colenbrander et al., 1994].

During the antepartum period FHR is increasingly used as a means of assessing fetal development and status in high risk pregnancies. As the direct FECG is not available antenatally, antepartum FHR is usually obtained via Doppler ultrasound or simple stethoscopic auscultation. Both of these techniques require the subject to be stationary (usually lying on a bed) and in the presence of a midwife. For these reasons it is unusual if FHR monitoring sessions last much longer than an hour. One example of a study in which longer recordings of antepartum FHR were obtained using Doppler ultrasound, has been reported by Mori et al. (1993).

The potential application of Doppler ultrasound based techniques, to the development of a long-term ambulatory recorder of FHR, is limited for a variety of reasons. These include the long-term exposure to ultrasound, the problem of maintaining the ultrasound beam focused on the heart of the moving fetus, the bulky nature of the transducer and the power requirements. In addition, the beat-to-beat accuracy of FHR recordings made with this technique, may not be sufficient for fetal HR variability (FHRV) analysis [Dawes, 1990], a method which may be useful for assessing the condition of the fetal nervous system [Ferrazzi et al., 1989].

Long-term FHR recordings have also been reported using phonocardiology, which is basically an automated electronic form of auscultation [Bassil and Dripps, 1989]. Although this technique is non-invasive, its potential application to the development of a long-term ambulatory FHR recorder, is limited by the susceptibility of the transducer to corruption by pressure waves from maternal and fetal movements, which restricts its use to resting mothers. It has also been reported that FHR recordings produced with this technique are unlikely to be accurate enough for FHRV studies [Goovaerts et al., 1994].

Antenatal FHR recordings have been reported based on the detection of the indirect FECG [Peasgood, 1993]. In the antepartum period, when direct connection is not possible, the FECG can be detected via cutaneous electrodes placed on the mothers abdomen (Figure 6.1), a technique first developed by Cremer in 1906. The main limitation of this approach is the unreliability of obtaining usable FECG complexes. Difficulties in detecting the abdominal FECG can occur when the level of the FECG signal (rarely > 50 μV) falls below either the background muscle noise (usually > 10 μV) or the input noise voltage of the electronic circuitry, being used to detect the FECG (dependent on the quality of components used but usually < 10 μV). Previous workers in this field have reported success rates of between 50 % and 70 % [Carter et al., 1980], [Crowe et al., 1995]. However, success rates can be measured in several different ways. A 70 % success rate can mean 70 % of recordings or 70 % of patients or 70 % of complexes. It has also been reported that a usable FECG is less likely to be obtained from certain mothers between 26 and 34 weeks gestation [Oostendorp et al., 1989]. It is thought that this is due to the covering of the fetus with vernix, which is a poor conductor, during this period.

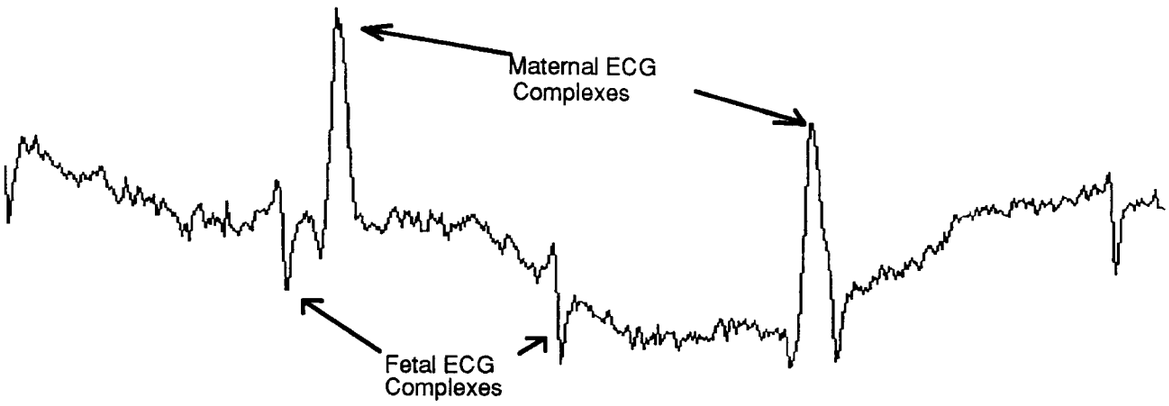


Figure 6.1: Antepartum abdominal ECG detected via skin electrodes (from Peasgood (1993))

At present the development of a long term ambulatory FHR recorder based on the abdominal FECG would seem to be the only feasible approach. This technique is completely non-invasive, unobtrusive (requiring only three electrodes) and has been shown to be capable of producing continuous records of both MHR and FHR, given the presence of a fetal signal [Mohd Ali, 1994]. In addition, FHR records obtained with technique have been shown to be sufficiently accurate for FHRV analysis to be performed [Cerutti et al., 1986].

6.3. Circuit description

A block diagram of the general electrophysiological signal recorder can be seen in Figure 6.2. This design consists of an instrumentation amplifier with band pass filter, variable gain, analogue to digital converter (ADC), SRAM, universal asynchronous receiver transmitter (UART) and some clock and control circuitry. All the circuitry is contained within the ASIC described in Chapter 4 except the SRAM, an RS-232 interface IC and several resistors, capacitors and switches.

Several decoupling capacitors are included in order to reduce the extent to which the recorded electrophysiological signal is contaminated by digital switching noise. Switching noise (see section 6.4.) on the power supply lines of

the sensitive analogue front-end op-amps, such as those within the instrumentation amplifier, can propagate through to the output of the analogue front-end. In order to reduce this effect, all the power supply pins of the ASIC (analogue and digital, positive and negative) are decoupled to the analogue circuit common (0 V in Figure 6.3), using large tantalum capacitors (100 μF). The SRAM IC is also decoupled using a 100 μF tantalum resistor connected directly between Vdd and Vss.

The raw electrophysiological signal to be recorded is detected via skin electrodes connected to the inputs of an instrumentation amplifier. The signal is filtered and amplified before being digitised by the ADC and stored in SRAM. After recording is complete, the stored data is transferred to the hard disk of a PC by the UART, which sends the data in RS-232 format via the serial port.

The recorder is designed for use with a variety of electrophysiological signals. In order to achieve this flexibility, the instrument needs to have a degree of programmability. The different amplitude and frequency content of various electrophysiological signals, requires the gain and the bandwidth of the signal conditioning circuitry (see Figure 6.3) and the resolution and sampling frequency of the ADC, to be selectable.

6.3.1. Variable bandwidth

The bandwidth of the instrument is varied by changing the filtering of the instrumentation amplifier (see frequency response in Appendix F). This involves changing 3 internal capacitors C1, C2 and C3. C1 and C2 determine the low pass cut-off and must always be the same value, while C3 determines the high pass cut-off. In order to simplify this procedure, these three components are placed in IC sockets from which they can easily be removed.

6.3.2 Variable gain and the optical link

There are two gain controls in the electrophysiological signal recorder VR1 and VR2. VR1 sets the gain range at either 250 to 1750 or 570 to 4000 and is only accessible internally. VR2 is positioned on the front panel and can be altered easily with a screw driver. VR2 is used to alter the amplitude of the analogue input to the ADC. The gain should be set high enough as to use the full 2.5 V input range, without being set so high as to cause saturation and clipping.

In order to set the gain appropriately, the amplitude of the signal to be recorded is required. For many electrophysiological signals the amplitude can vary significantly for different patients and different electrode positions. To overcome this problem, the input to the ADC is accessible externally, in order that the signal can be viewed on a nearby oscilloscope. For safety reasons connection to an oscilloscope is achieved with an optical link, as this method allows the patient to remain electrically isolated from the mains powered oscilloscope. The analogue signal to be digitised is converted into an optical signal by simply modulating the output of a light emitting diode (LED) (as shown in Figure 6.3). The optical signal is converted back into an electrical signal using a photo diode (SFH250V). The photo diode is simply connected across the input of the oscilloscope (Hameg HM 205-3), using the large input impedance of the oscilloscope to convert the small current produced by the incoming light, into a voltage.

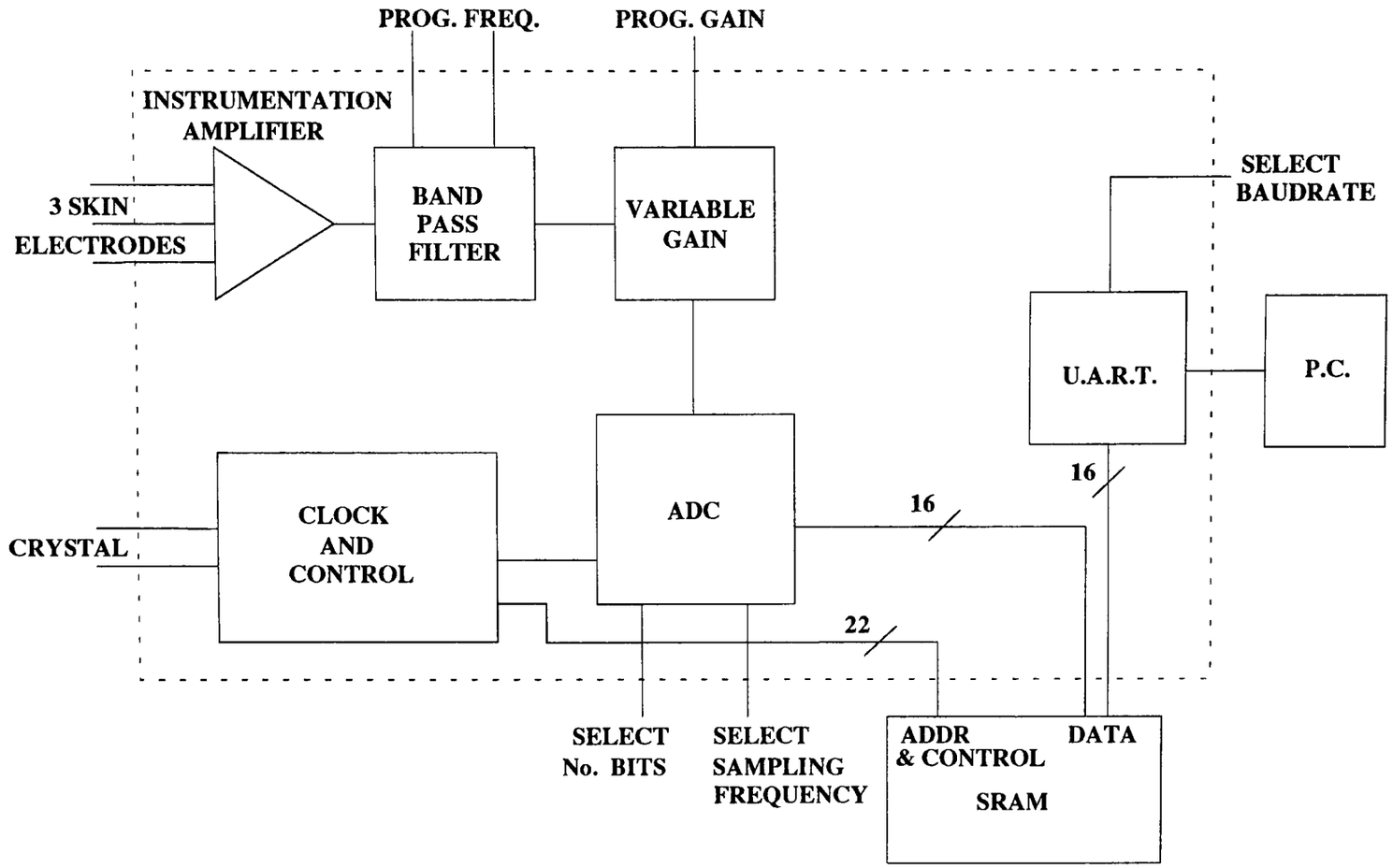


Figure 6.2: Block diagram of raw electrophysiological signal recorder

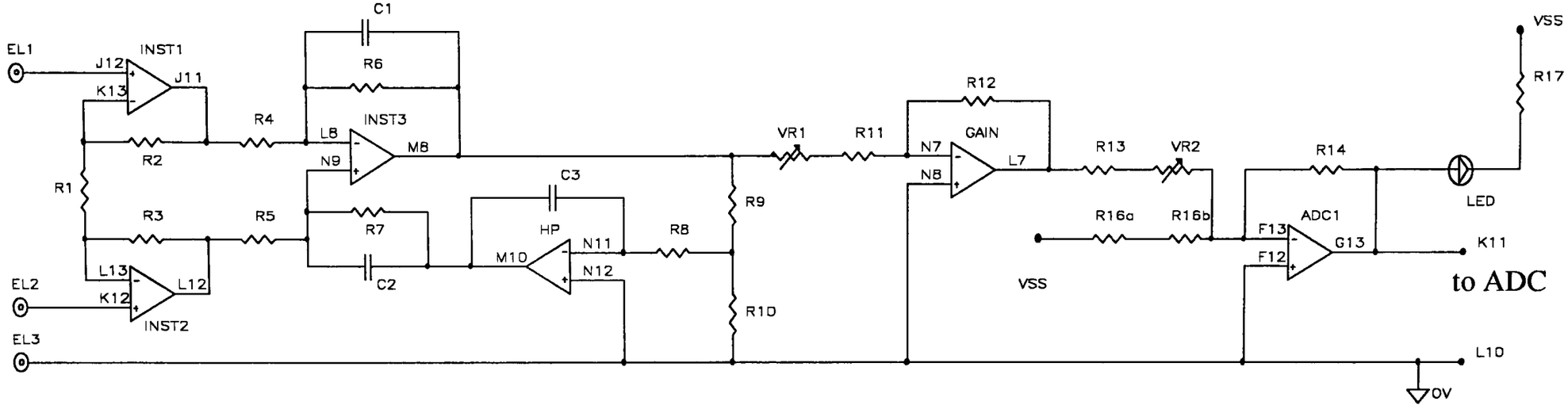


Figure 6.3: Analogue signal conditioning circuitry; all op-amps are incorporated within the ASIC while the capacitors, resistors and LED are connected externally

6.3.3. Programming the ADC and reducing aliasing

A description of the operation of the programmable dual slope integrating ADC can be found in Chapter 4. The sampling frequency and resolution of the ADC should be set as appropriate for the frequency content and dynamic range of the signal to be digitised. In particular, a sampling frequency should be selected that will not lead to aliasing problems. The conventional method of reducing the effects of aliasing is to include an anti-aliasing filter before the ADC. This filter will normally have a cut-off of high order (around 6) at a frequency which is just below half the sampling frequency. The higher the filter order, the closer the cut-off can be to half the sampling frequency.

The only low pass filtering in the electrophysiological signal recorder is contained in the band pass filtering of the instrumentation amplifier and is only first order. To reduce aliasing without using a specific anti-aliasing filter, a sampling frequency should be selected which is much greater (an order of magnitude) than the low pass cut-off of the instrumentation amplifier filtering.

6.4. FECG recorder

The raw electrophysiological signal recorder was configured as an FECG recorder, in order to investigate the possibility of determining FHR, from cutaneous electrodes placed on the maternal abdomen. The FECG recorder is an intermediate stage in the development of an ASIC based long-term ambulatory recorder of FHR. The potential for such an instrument was investigated, by recording the FECG from several mothers, in various locations and postures, and at various times of the day.

When configured to record FECG signals, the ADC is set to digitise at 600 Hz with a resolution of 13 bits. When configured with a 512K x 8 bit SRAM, this instrument has a maximum record time of just over 7 mins. As the only

parameter to be extracted from the recorded FECG is the FHR, the bandwidth of the recorder is set between 3.8 and 48 Hz. The choice of a high pass cut-off at 3.8 Hz is high enough to overcome baseline drift, without being too high as to cause excessive ringing of the maternal and fetal QRS complexes. The choice of a low pass cut-off at 48 Hz is high enough to obtain most of the frequency content of the R-wave, without being too high as to cause aliasing problems. Table 6.1 contains the component values used in the analogue front end of the FECG recorder. For FECG recordings the gain was set at 4000 (VR1 = 0, VR2 = 0), unless it appeared likely that the signal would saturate, in which case the gain was reduced by increasing the value of VR2.

Component	Value
R1	750Ω (all resistors < 5 %)
R2-R7	20K
R8-R9	510K
R10	100K
R11	33K
R12	330K
R13	62K
R14	620K
R16	2 x 620K
R17	1.6K
VR1 *	50K
VR2 *	470K
C1-C2 *	220nF (polyester 10 % tolerance)
C3 *	10nF (polyester 10 % tolerance)
LED	SFH450V

Table 6.1: Component values for analogue front end of FECG recorder with programmable components indicated *.

During initial testing it was found that the performance of the general electrophysiological recorder, was limited by the corruption with switching noise, of signals detected by the analogue front. Frequency components at both multiples and divisions of the sampling frequency could be seen on both the analogue and digital power rails. These same components could also be seen at

the input to the ADC as well as at various other points of the analogue circuitry. Once downloaded only the components at divisions of the sampling frequency remained, as the components at multiples of the sampling frequency, are filtered out in the ADC circuitry. The amount of interference varied from recording to recording and was completely absent on several occasions. When present this type of interference introduced a noise component of typically 10 μV, when referred to the recorder input. This problem was greatly reduced by a decoupling scheme (as described in section 6.3.) but not completely eliminated.

Another problem was encountered with the ADC of the general electrophysiological recorder. When the analogue input to be digitised became negatively saturated, the ADC failed to digitise, resulting in a loss of data. This problem arose when the analogue input to the ADC (Va) became slightly negative (see section 4.4.1.). In theory, this should not occur as a bias circuit is employed to ensure that Va is always between 0 V than +2.5 V. One possible cause of a negative Va could be a slight negative offset inherent in the op-amp used for the bias circuit. In the recordings made for this study the negative saturation problem was avoided by making sure the front-end gain was not set too high.

6.5. FECG results

A total of 119 abdominal FECG recordings were taken from 8 different mothers ranging from 17 to 39 weeks of gestation. These recordings are split into two groups, recordings taken from patients in the Pregnancy Assessment Centre, Queen's Medical Centre (QMC), Nottingham, which will be referred to as hospital recordings and recordings taken from a single volunteer mother in her home environment which will be referred to as the longitudinal study.

6.5.1. FECG traces

The morphology of the FECG and maternal ECG (MECG) complexes within the abdominal signals shown in this chapter are partly determined by the bandwidth of the front end amplifier and partly determined by a second 2nd order bandpass filter. This second filter is a digital filter and is applied to the digitised signal after it has been downloaded to the PC, using the Hypersignal software package. A bandwidth of 10 to 33 Hz (2 pole Butterworth IIR filter) was chosen in order to eliminate any dc. offset as well as to enhance both the FECG and MECG complexes in preparation for FHR and MHR extraction.

6.5.2. HR traces

HR traces described in this chapter were extracted from the abdominal recordings made with the raw electrophysiological signal recorder using a windows based real-time abdominal FECG analysis program [Huang et al., 1994]. The FECG analysis package is designed for use with an abdominal recording system, which also records the MECG from thoracic electrodes, simultaneously, on a separate channel. The thoracic channel is used as part of the MECG subtraction routine, which is necessary because both the FECG and the MECG appear on the abdominal channel (see Figure 6.1). A simple threshold detection scheme is employed in the thoracic channel, in order to time locate the MECG complexes within the abdominal channel. To use the FECG analysis program with recordings made by the general electrophysiological signal recorder, both a thoracic channel and an abdominal channel are required. This is achieved by using the same signal for both the thoracic and the abdominal channel.

Using the abdominal channel for the expected thoracic channel works well, as long as the MECG complexes are much larger than the FECG complexes and any noise spikes. The ability of the FECG analysis program to extract FHR

traces from the abdominal recordings made with the electrophysiological signal recorder, is therefore, not only dependent on the quality and size of the FECG complexes, but also the quality and size of the MECG complexes. It is important to begin the MECG detection with several clear MECG complexes which are larger than any surrounding FECG complexes and noise spikes, because large noise spikes can cause the threshold, used to detect the MECG complexes, to be set too high. FECG complexes which are as large as the surrounding MECG complexes, will cause erroneous MECG subtractions from the abdominal signal. This will result in a distorted MHR trace, as the program gets confused between which complexes are MECG and which are FECG. The resulting HR trace will be characterised by a degree of 'crosstalk' between the MHR trace and the FHR trace.

After MECG subtraction, FECG complexes can be detected in either of two ways. Firstly, using a simple bandpass filter and threshold scheme or secondly using a matched filter. On the whole, the matched filtering scheme is better at extracting an FHR trace. However, the quality of the FHR extracted can be very sensitive to the starting point of the FECG detection scheme. It is important that FECG complexes are present at the beginning of the recording. If this is not the case, then it can be advantageous to begin the FHR extraction at a point, later in the recording, when good FECG complexes are present. The starting point is not as important for the bandpass filtering scheme as this type of filter does not change its response to match the signal. In order to determine a good starting point for the matched filtering scheme, all the abdominal recordings were first analysed using the bandpass filtering scheme.

6.5.3. Averaged FECG complexes

The windows based real-time abdominal FECG analysis program used to produce the FHR and MHR traces was also used to produce an average FECG

complex. Although the primary aim is to develop an ambulatory recorder of FHR, a instrument capable of full FECG analysis, in addition to HR, would also be of interest.

One example of an averaged FECG from each of the two study groups is presented, in order to demonstrate that some of the FECG recordings are of a high enough quality, to perform full FECG analysis. Both of these averaged FECGs contain 50 equally weighted complexes. Of course, the morphology of the averaged FECG complex is highly distorted by the various filtering stages as explained in section 6.5.1. [Tayler and Vincent, 1983], although some, if not all of the timing points may still be valid. An instrument intending to analyse the full FECG would require a much wider bandwidth (0.05 to 250 Hz) which may in turn introduce serious baseline drift problems, as is often encountered during intrapartum FECG analysis.

6.5.4. Hospital recordings

All the recordings described in this section were taken in the Pregnancy Assessment Centre of the QMC, Nottingham. A total of 9 recordings were taken from 7 different mothers ranging from 24 to 39 weeks of gestation, lying on a hospital bed. Before the general electrophysiological recorder could be used on patients, the equipment needed to safety tested by the Medical Equipment Servicing Unit (MESU) at the QMC. In order to pass this test the equipment must comply with the BS5724, electrical safety of medical equipment, the relevant parts of which are summarised in Appendix A. A copy of the documentation required in order to meet the requirements of BS5724 is contained in Appendix E, together with a set of operating instructions.

6.5.4.1. Electrode type and position

Three disposable, foam-backed, silver-silver chloride, pre-gelled electrodes (con-med) were used in all the hospital recordings. Before attaching the electrodes, the patient's skin was prepared with an alcohol saturated swab and left to dry for around 5 minutes. The two differential input electrodes were positioned vertically in the midline, 10 cm above and 10 cm below the umbilicus (fundal and supra pubic). The third 'common' electrode was placed on the mother's wrist.

6.5.4.2. Hospital FECG traces

FECG complexes could be seen in 5 of the 9 hospital recordings from 3 of the 7 mothers. Examples of these recordings can be seen in Figures 6.4 to 6.8. Each trace contains 2 seconds of abdominal signal, with the fetal and maternal R-waves indicated by F and M respectively. The signals in Figures 6.4 to 6.7 were recorded with a 2nd order bandwidth of 0.2 Hz to 38 Hz (C1, C2, C3 = 220 nF), whereas the signal in Figure 6.8 was recorded with a 2nd order bandwidth of 3.8 Hz to 48 Hz (C1, C2 = 220 nF, C3 = 10 nF). Note the difference in morphology between the fetal complexes in Figure 6.6 and Figure 6.7, which may relate to different fetal positions.

Figure 6.4: Raw abdominal signal recorded from mother A at 24 weeks gestation.

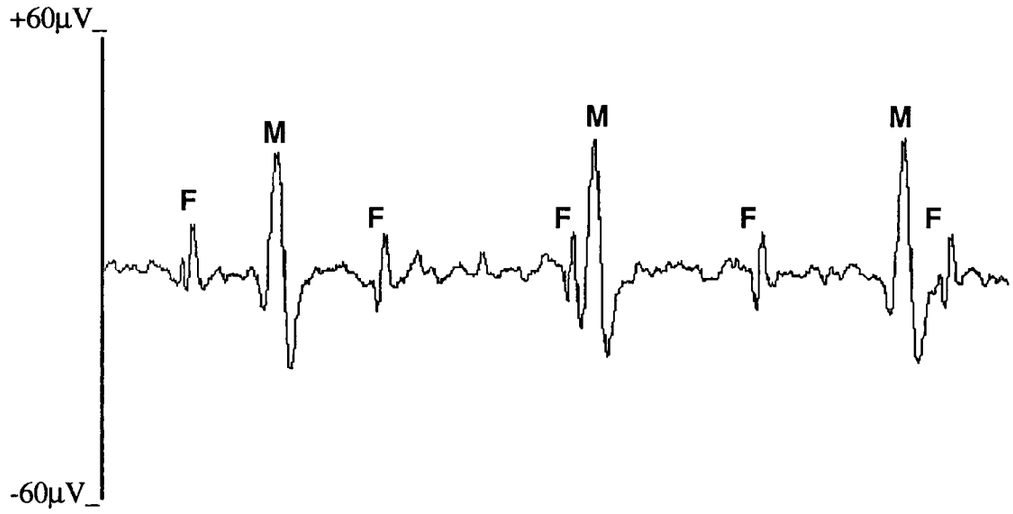


Figure 6.5: Raw abdominal signal recorded from mother A at 25 weeks gestation.

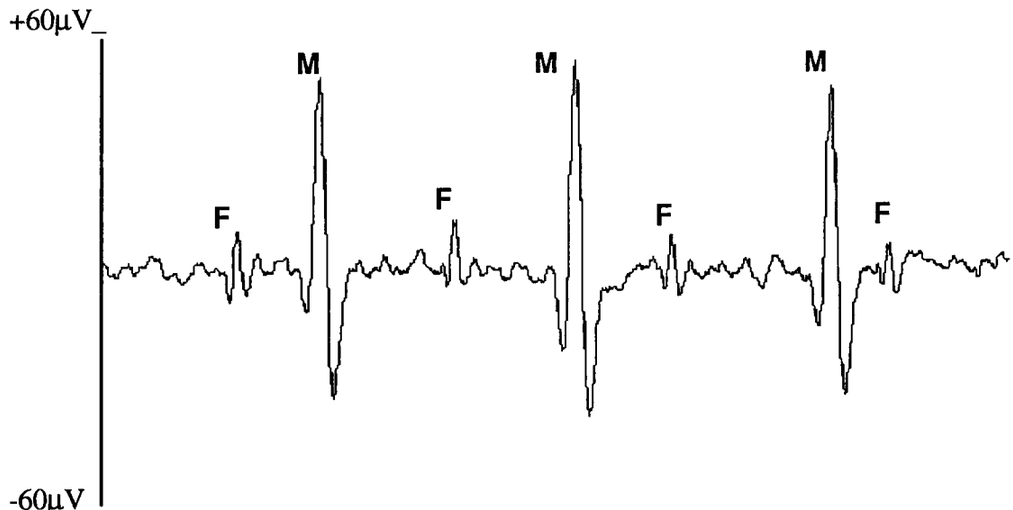


Figure 6.6: Raw abdominal signal recorded from mother A at 26 weeks gestation.

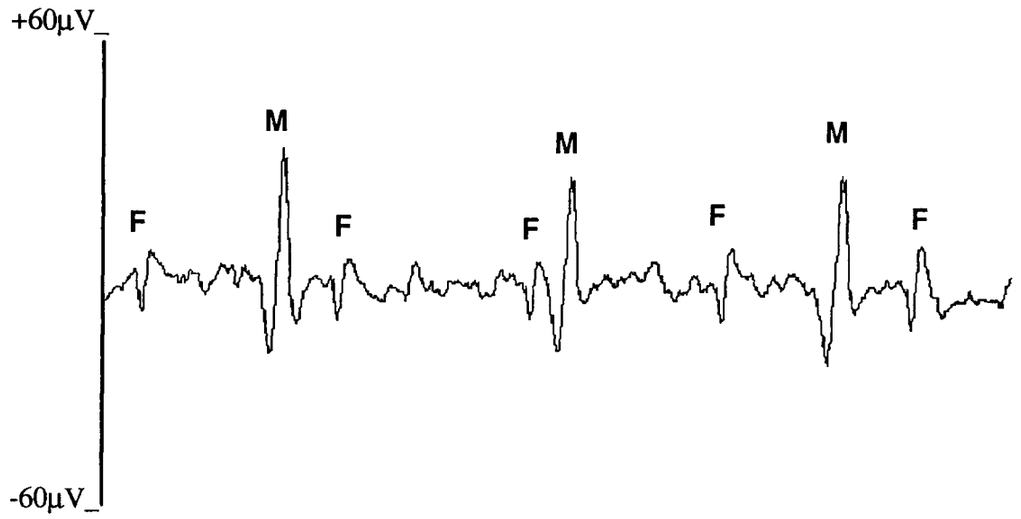


Figure 6.7: Raw abdominal signal recorded from mother B at 31 weeks gestation.

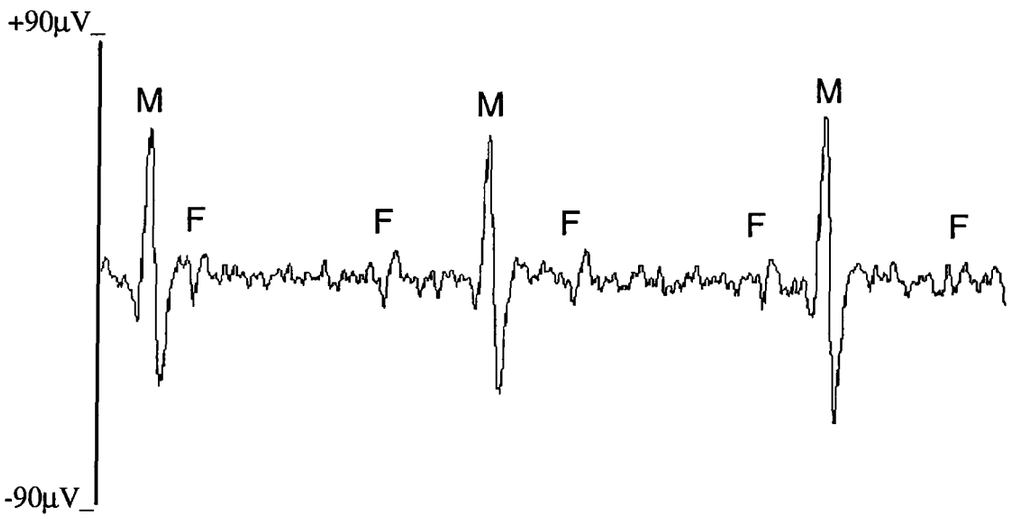


Figure 6.8: Raw abdominal signal recorded from mother C at 33 weeks gestation.

It can be seen that the signal in Figure 6.8 contains a small amount of 50 Hz interference. Most workers involved in the recording of electrophysiological signals acknowledge the presence of this type of interference. An analysis of the causes of 50 Hz noise is presented in Appendix B, culminating in a set of guidelines, which if followed, will reduce, if not completely eliminate, this type of interference. Wherever possible these guidelines were followed both in the design of the equipment and in the FECG recording procedures.

6.5.4.3. Hospital HR traces

Figures 6.9 to 6.13 show FHR and MHR traces extracted from the 5 abdominal signals shown in Figures 6.4 to 6.8. Each trace is plotted on a beat-to-beat

basis with all points shown. This allows the concentration of points to be used as an indicator of HR trace quality.

The HR trace in Figure 6.9 is taken from mother A at 24 weeks gestation. This trace contains a clean MHR with several short sections of FHR being visible from around 1 minute into the recording.

Figure 6.10 is taken from the same mother at 25 weeks gestation. In this recording, clean traces are obtained for both the FHR and the MHR.

The HR traces in Figure 6.11 were obtained at 26 weeks gestation and are of almost as high a quality as at 25 weeks gestation, apart from a section of around 40 seconds, about 3 minutes into the recording. During this period the FHR trace is temporarily lost.

The HR values below the MHR trace in Figure 6.11 are due to missed fetal beats, which leads to a halving of the FHR. This lower 'missed fetal beat' line is also present in Figure 6.12, which is taken from mother B at 31 weeks gestation. In this particular HR trace the FHR seems to posses a cyclic pattern, with a period somewhere in the region of 20 seconds.

The HR trace in Figure 6.13 is taken from mother C at 33 weeks gestation. In this recording a clear MHR is extracted, whereas only a fraction of the FHR trace is obtained.

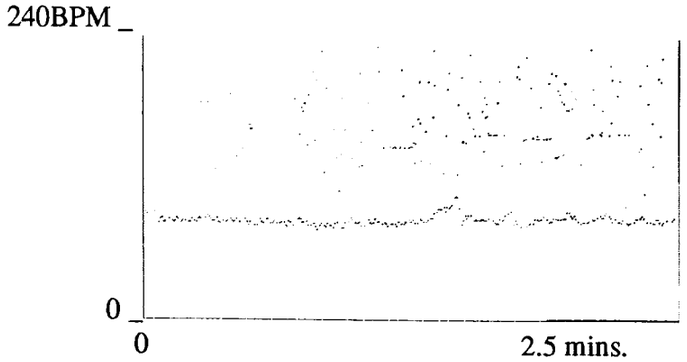


Figure 6.9: FHR (upper) and MHR (lower) extracted from mother A at 24 weeks gestation.

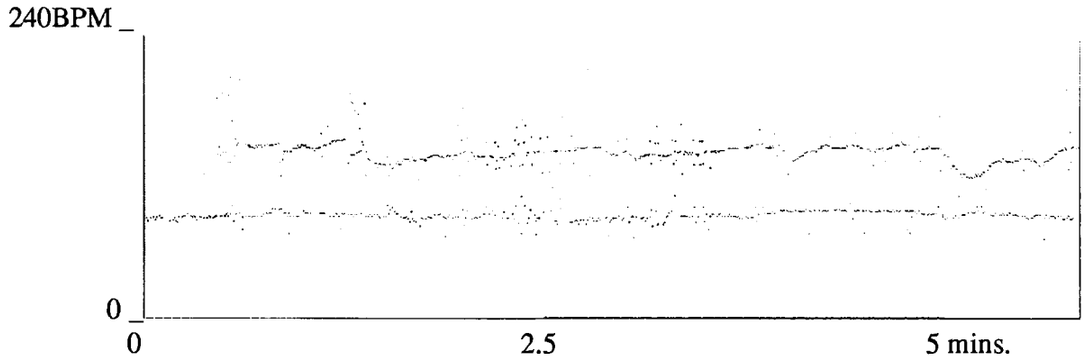


Figure 6.10: FHR (upper) and MHR (lower) extracted from mother A at 25 weeks gestation.

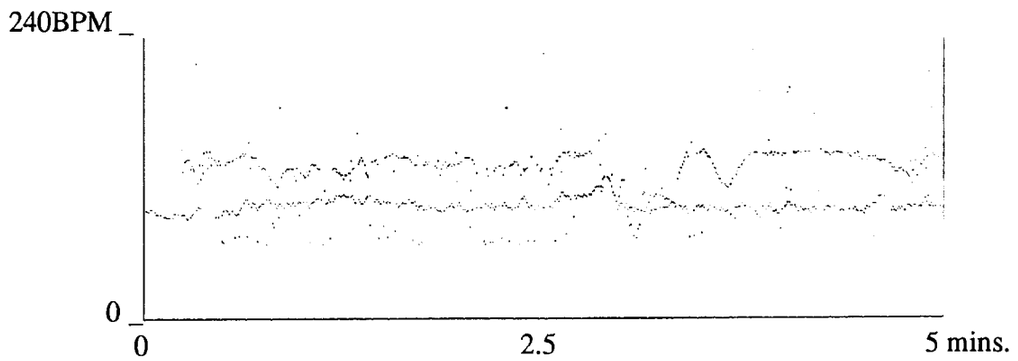


Figure 6.11: FHR (upper) and MHR (lower) extracted from mother A at 26 weeks gestation.

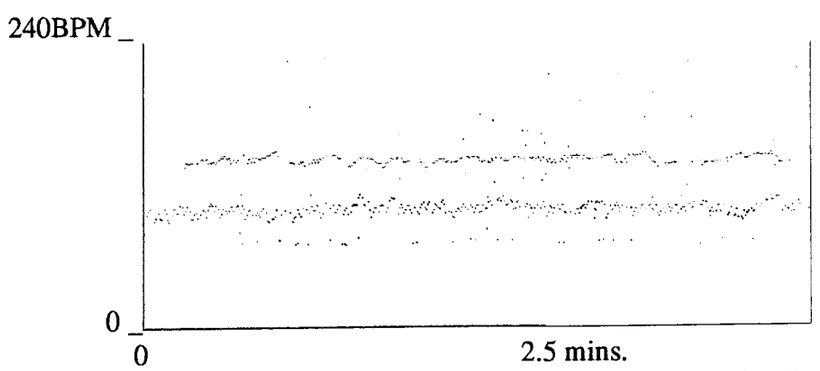


Figure 6.12: FHR (upper) and MHR (lower) extracted from mother B at 31 weeks gestation.

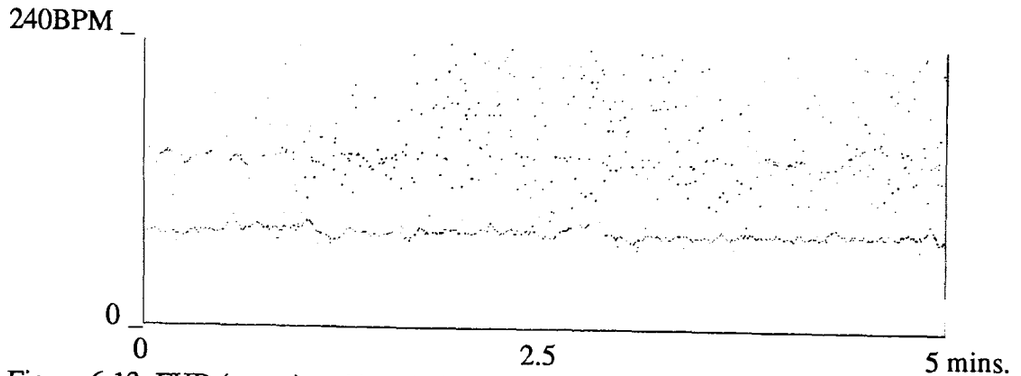


Figure 6.13: FHR (upper) and MHR (lower) extracted from mother C at 33 weeks gestation

6.5.4.4. Hospital averaged FECG complexes

Figure 6.14 contains an average FECG complex taken from mother A at 25 weeks gestation (see Figure 6.5). In addition to the QRS wave, the average contains a P-wave.

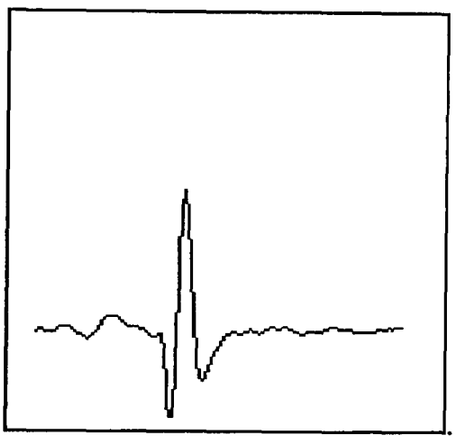


Figure 6.14: Averaged FECG from 25 weeks

6.5.5. Longitudinal study

All the recordings described in this section were taken on the same mother at weekly intervals from the 17th week of gestation through to term. A total of 110 recordings were made, mainly in the subjects own home. Initially (weeks 17 to 23), recording sessions lasted around 90 minutes, in which time three or four recordings would be made. These sessions took place midweek and were supervised by the author. During this time, the optical link was used to determine the optimal gain setting and electrode positions.

Once a suitable gain and electrode arrangement had been found, the recorder and a laptop PC were taken to the home of the volunteer mother every

weekend (except at 32 weeks gestation). The mother then made the recordings, performing all stages of data acquisition (i.e. electrode attachment, operation of the recorder and download of data) herself. Typically, over a weekend, six recordings of around 6 minutes duration would be made. At 32 weeks gestation the subject was monitored midweek by the author, using the optical link to visually examine the abdominal signal for the presence of FECG complexes, using a variety of electrode positions and subject postures.

6.5.5.1. Electrode type and position

Three disposable, foam backed, silver-silver chloride, solid gel electrodes (3M 2237) were used in all the longitudinal study recordings. Before attaching the electrodes the patient's skin was prepared with an alcohol saturated swab and left to dry for around 5 minutes. In the vast majority of cases the two differential input electrodes were positioned vertically in the midline 2.5 cm above and 10 cm below the umbilicus. The third 'common' electrode was placed on the mothers wrist. In the first seven recording sessions the upper differential input electrode alternated between 2.5 cm and 10 cm above the umbilicus. During the recording session made at 27 weeks gestation, various other differential input electrode positions were tried, including a horizontal arrangement. The only other electrode positions used were at 31 weeks gestation. On this occasion the 2.5 cm above and 10 cm below the umbilicus arrangement was offset from the midline by about 5 cm, so as to be positioned above the back of the fetus, as located by the mother.

6.5.5.2. Longitudinal study FECG traces

FECG complexes could be seen in 52 of the 110 recordings from 16 of the 22 recording sessions. FECG complexes could be seen in the recording session from 20 to 28 and from 33 to 39 weeks gestation. However, only a few complexes were seen at 33 and 34 weeks gestation. These complexes were

very small and tended to drift in and out, over a period of a few seconds. FECG complexes ranged in size from around 10 μV to around 60 μV (peak to peak), with the largest signals being found at 23 and 39 weeks gestation. The MECG complexes decreased with increasing gestational age, from around 100 μV to around 50 μV (peak to peak), with electrodes 2.5 cm above and 10 cm below the umbilicus.

Examples of FECG complexes found in the longitudinal study can be seen in Figures 6.15 to 6.20. Each trace contains 2 seconds of abdominal signal with the fetal and maternal R-waves indicated by F and M respectively. The signals in Figures 6.15 to 6.16 were recorded with a 2nd order bandwidth of 0.2 Hz to 38 Hz, whereas the signals in Figures 6.17 to 6.20 were recorded with a 2nd order bandwidth of 3.8 Hz to 48 Hz.

The signal in Figure 6.15 is taken from the recording session made at 20 weeks gestation, the first week that FECG complexes were successfully recorded. This particular recording was made outside, in the garden, with the mother lying down. A similar result was found at 21 weeks gestation.

Between 22 and 26 weeks gestation FECG complexes were found in all of the 22 recordings taken. During this period of pregnancy, the size of the FECG was independent of the mothers posture (i.e. lying down, sitting, standing up and kneeling) and, if anything, was slightly larger while the mother was standing up. The amount of muscle noise did however, vary with posture, being at a minimum when the mother was lying down.

The signal in Figure 6.16 is taken from the recording session made at 23 weeks gestation, while the mother was standing up. Note the increased amount

muscle noise compared to Figure 6.15. This particular recording contains some of the largest FECG complexes seen in the whole of the longitudinal study.

The signals shown in Figure 6.17 and 6.18 were taken at 27 and 34 weeks gestation respectively and contain the clearest FECG complexes found in these particular recording sessions. For most of these recording sessions no FECG complexes could be seen in the abdominal signal, save for the occasional run of small complexes which would drift in and out of the recording, over a time scale of several seconds. Any FECG complexes that were found tended to be during periods of the recording session in which the mother was lying down. Similar results were found at 28 and 33 weeks gestation.

In the 22 recordings made at 29, 30 and 31 weeks of gestation no clear FECG complexes were found. At week 32 no abdominal recordings were made as the recording session was used to experiment with different electrode positions and postures. Abdominal signals were inspected visually using the optical link. No FECG signals were found except for a period of around 1 minute, when a series of FECG complexes could be clearly seen.

35 to 39 weeks of gestation saw a gradual increase in FECG size. All the recordings were made, during this period, with the mother either lying or sitting. Figure 6.19 shows some of the clearest FECG complexes found at 37 weeks gestation. This recording was made while the mother was lying down. Figure 6.20 is taken from one of six recordings made at 39 weeks. In this particular recording the FECG complexes are the largest seen in the longitudinal study and are present throughout the whole recording. Surprisingly, no clear FECG complexes were found in any of the other five recordings taken over this weekend.

Figure 6.15: Raw abdominal signal recorded at 20 weeks gestation while lying down.

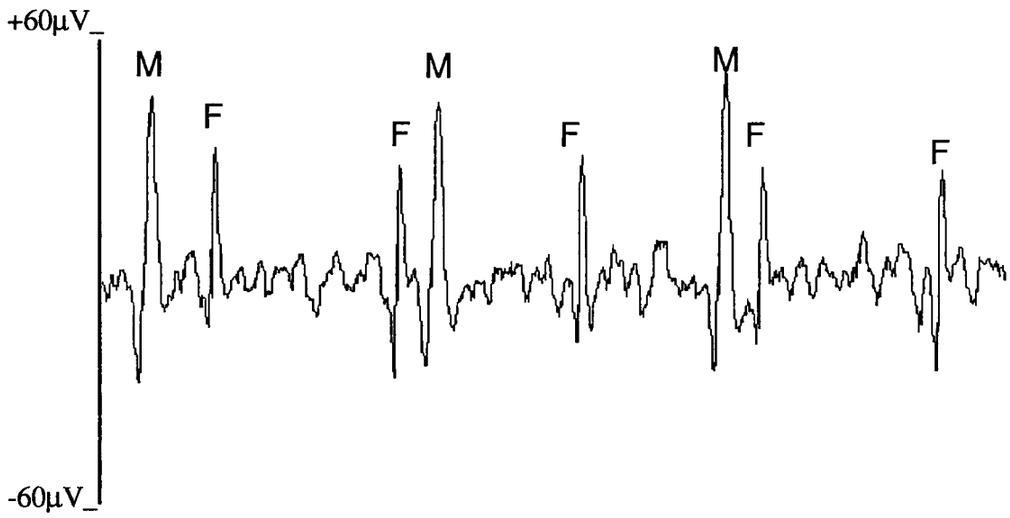


Figure 6.16: Raw abdominal signal recorded at 23 weeks gestation while standing up.

Figure 6.17: Raw abdominal signal recorded at 27 weeks gestation while lying down.

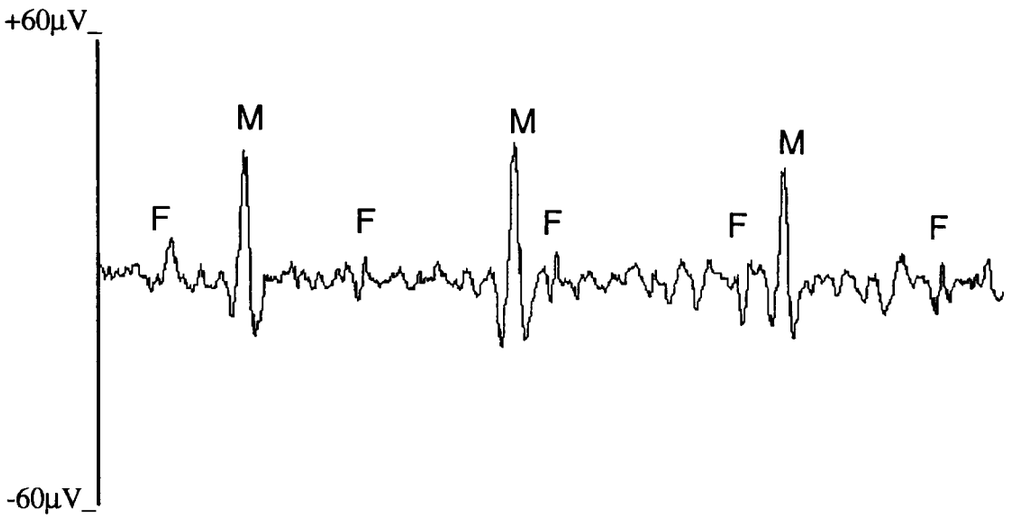


Figure 6.18: Raw abdominal signal at 34 weeks gestation while sitting.

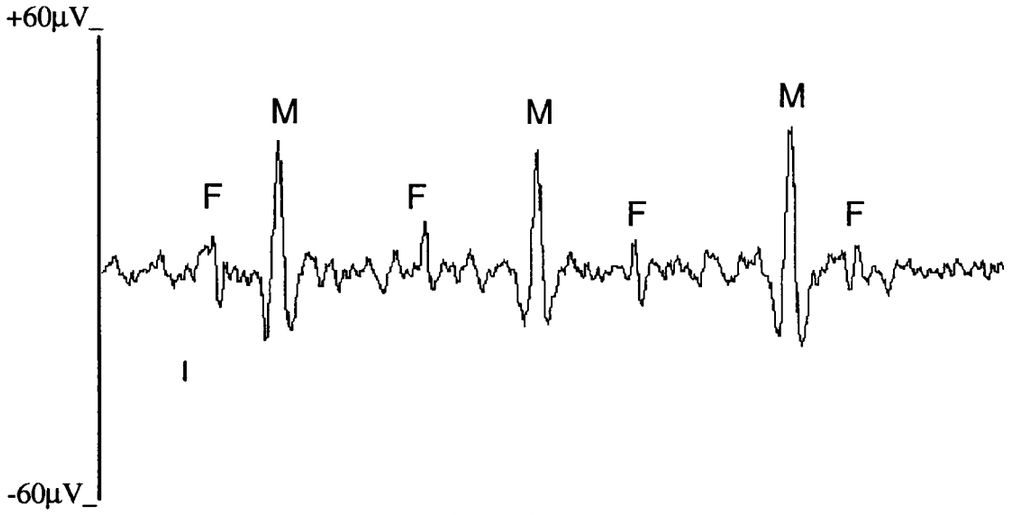


Figure 6.19: Raw abdominal signal at 37 weeks gestation while lying down.

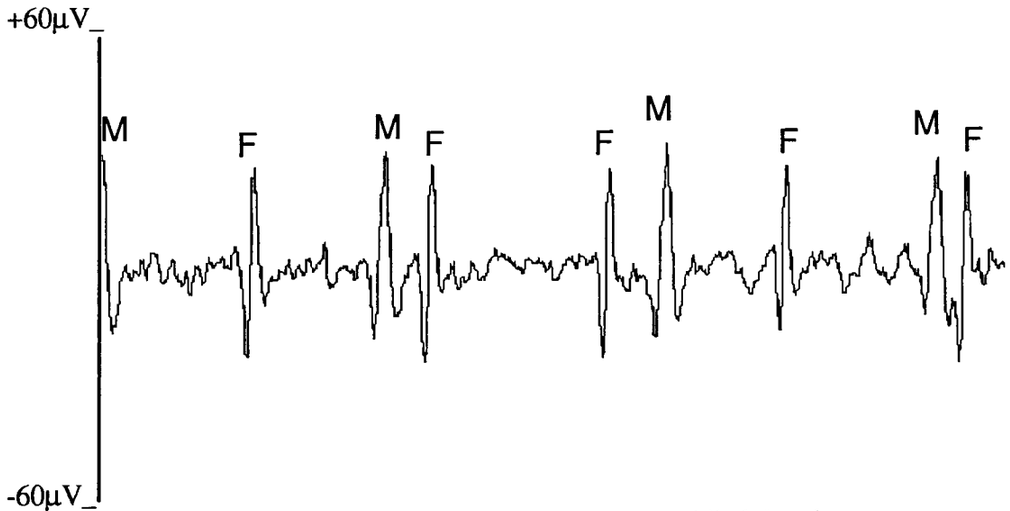


Figure 6.20: Raw abdominal signal at 39 weeks gestation while lying down.

6.5.5.3. Longitudinal study HR traces

Figures 6.21 to 6.27 show FHR and MHR traces extracted from the abdominal recordings of the longitudinal study. As expected, good HR traces were extracted from recordings which contained strong FECG complexes. The best FHR traces were obtained from recordings made between 23 and 27 weeks gestation. Examples of HR traces taken from recordings made during this period are shown in Figures 6.21 to 6.26.

The cleanest FHR trace obtained is shown in Figure 6.21. This recording was made at 26 weeks of gestation while the mother was lying down. The HR trace in Figure 6.22 was taken at 23 weeks gestation. For the first 3 minutes of this recording the mother was sitting, whereas for the last 3 minutes the mother was standing up. Initially, the quality of the FHR trace deteriorates, as the mother moves from sitting to standing up. However, after 2 minutes of poor quality FHR, the trace suddenly improves, with the last minute of the FHR trace being as good, if not better, than the high quality trace found in the first 3 minutes.

Another example of the ability to obtain an FHR trace while the mother is standing up, can be found in Figure 6.23., which is taken from a recording made at 25 weeks gestation. The HR traces in Figure 6.24 are taken from another recording made at 25 weeks gestation, with the mother sitting, immediately after some light exercise.

The HR traces in Figure 6.25 are taken from a recording made at 24 weeks gestation, while the mother smoked her one daily cigarette. The HR traces in Figure 6.26 are taken from a recording made at 24 weeks gestation while the mother was lying down. There seems to be a large deceleration in the FHR trace during the final minute of this recording. No clean FHR traces were obtained between 29 and 34 weeks gestation.

Although many of the recordings made after 34 weeks gestation contained strong FECG complexes, the FECG analysis program was unable to extract clean FHR traces. The best FHR trace obtained is shown in Figure 6.27. This recording was made at 37 weeks gestation while the mother was lying down.

The inability of the software to successfully extract a clear FHR trace during the later stages of pregnancy is due to the reduced size of the MECG as explained in section 6.5.2.. Clearly the extraction of a clear FHR trace could be achieved using modified software, particularly if the FECG is as large as that found at 39 weeks.

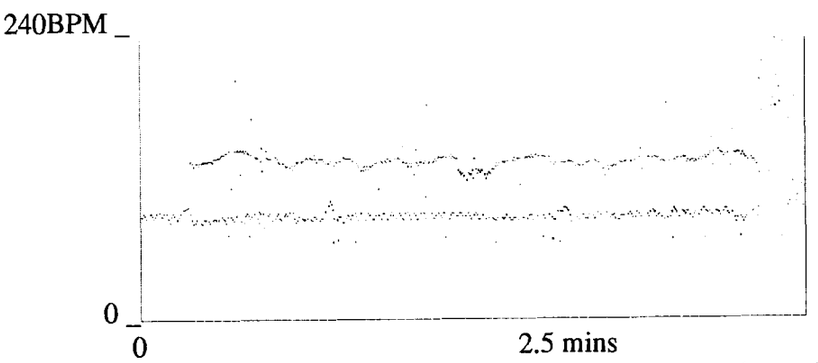


Figure 6.21: FHR (upper) and MHR (lower) from volunteer mother at 26 weeks gestation.

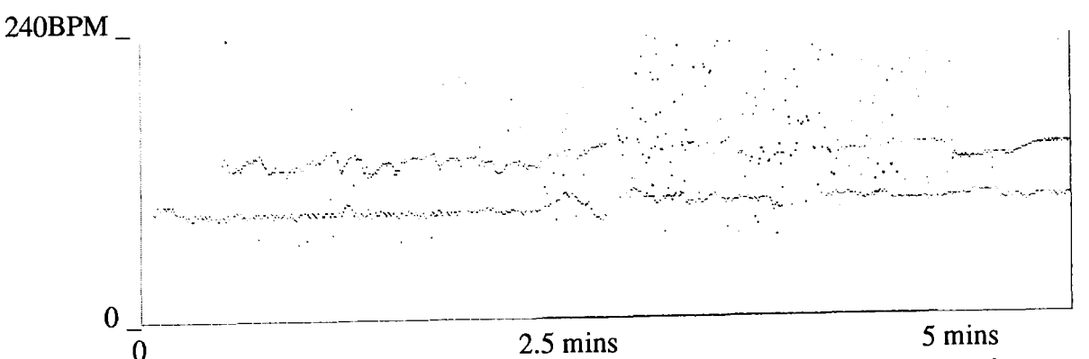


Figure 6.22: FHR (upper) and MHR (lower) from volunteer mother at 23 weeks gestation.

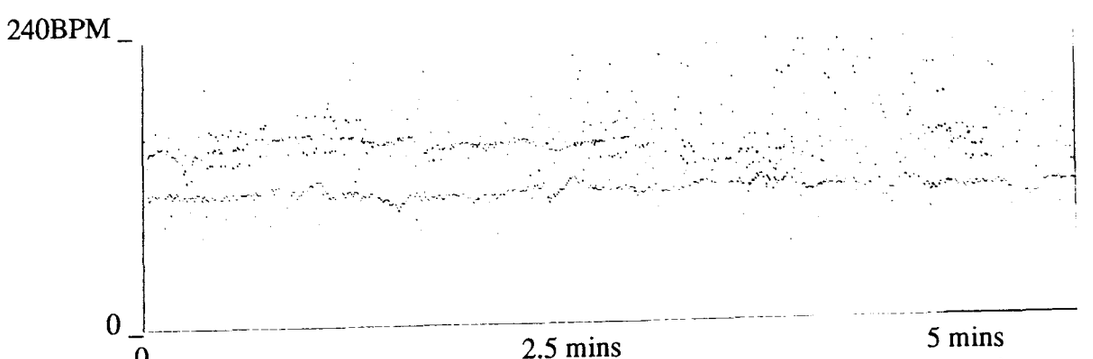


Figure 6.23: FHR (upper) and MHR (lower) from volunteer mother at 25 weeks gestation.

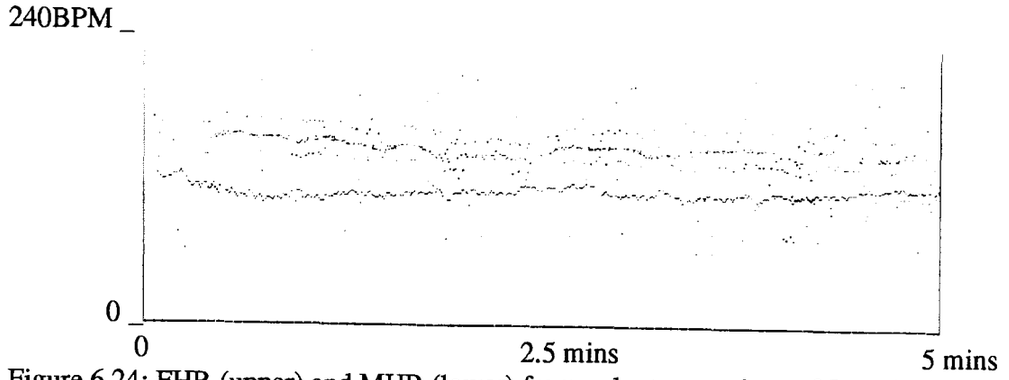


Figure 6.24: FHR (upper) and MHR (lower) from volunteer mother at 25 weeks gestation.

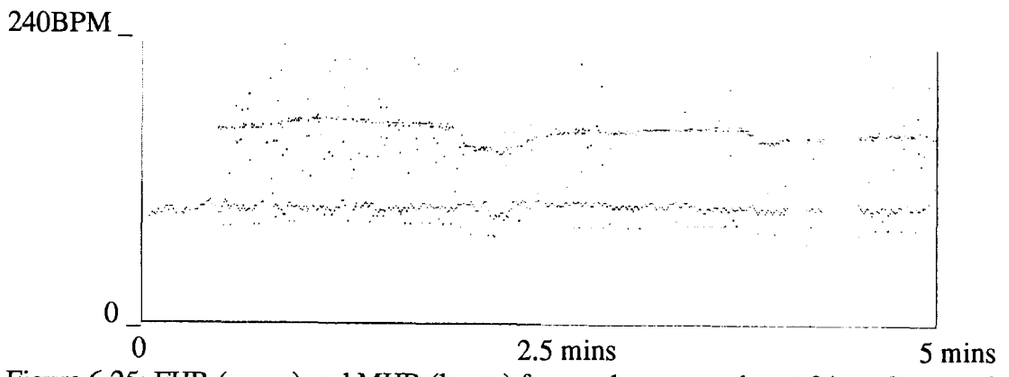


Figure 6.25: FHR (upper) and MHR (lower) from volunteer mother at 24 weeks gestation..

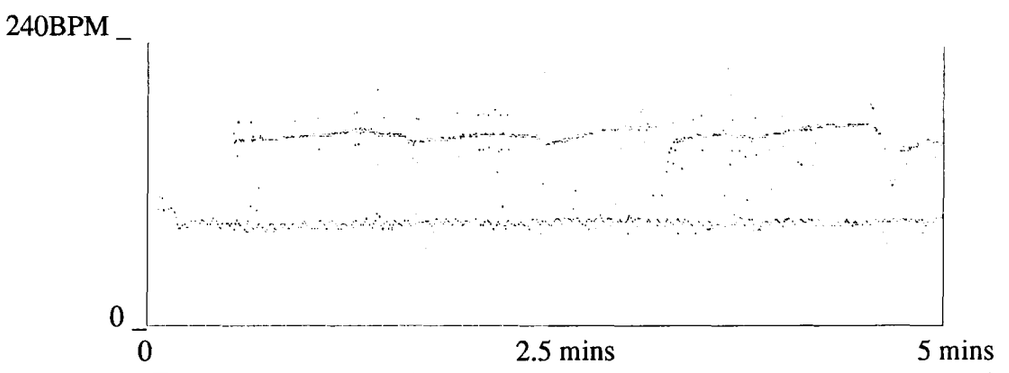


Figure 6.26: FHR (upper) and MHR (lower) from volunteer mother at 24 weeks gestation.

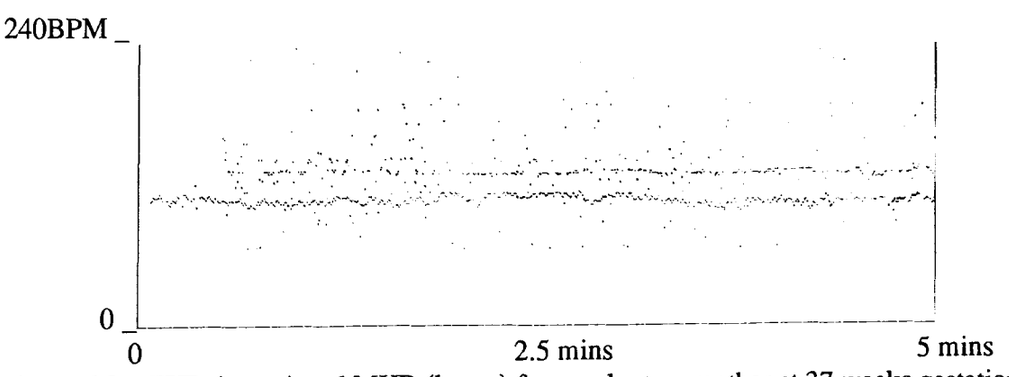


Figure 6.27: FHR (upper) and MHR (lower) from volunteer mother at 37 weeks gestation.

6.5.5.4. Longitudinal study averaged FECG complex

Figure 6.28 contains an average FECG complex taken at 23 weeks gestation while the mother was sitting. In addition to the QRS wave the average seems to contain quite a large P-wave. Again, the lack of a clear T-wave is to be expected, given the filtering used.

Figure 6.28: averaged FECG from 23 weeks

6.6. Conclusions

An intermediate version of the general electrophysiological signal recorder has been built which stores digitised electrophysiological signals directly to RAM. The gain, bandwidth, sampling frequency and bit resolution of this instrument are flexible in order that a variety of electrophysiological signals can be recorded. The final instrument was constructed on veroboard using point-to-point wiring and enclosed in a plastic case measuring 155 mm x 90 mm x 45 mm, which includes a compartment for four AA cells (see photograph in Appendix D). This instrument proved to be easy to use, borne out by the numerous recordings (including signal acquisition and downloading to the PC) performed by the subject of the longitudinal study. The mother was previously unfamiliar with the recorder, the download program or PCs.

In this chapter the general electrophysiological signal recorder has been configured as an FECG recorder and used to make a total of 119 FECG

recordings, of which 57 contained FECG complexes, a recording detection rate of 48 %. 110 of these recordings were taken from the same mother, between 17 and 39 weeks of gestation. The remaining 9 recordings were taken from 7 different mothers, ranging from 24 to 39 weeks gestation. Observable FECG complexes were obtained from 4 of the 8 mothers recorded, a patient detection rate of 50 %. Of the 48 % of recordings which contained detectable FECG complexes, the number of complexes obtained, varied from just two or three to every complex.

During the longitudinal study the FECG detection rate varied significantly with gestational age. FECG complexes were obtained from 20 to 28 weeks and from 33 to 39 weeks gestation, with the largest complexes recorded at 23 and 39 weeks. In the period between 29 and 33 weeks no observable FECG signals were obtained. This result agrees strongly with the findings of other workers who attributed this effect to the covering of the fetus with vernix.

The amount of noise and interference in the FECG recordings was largely dependent on posture, being at a minimum when the mother was lying down. In this position abdominal muscle noise of around 10 μV was observed. Several of the recordings were corrupted by switching noise. The extent of this type of interference varied from recording to recording, usually being of the order of 10 μV, which may account for success rates being below the levels reported by other workers

Several abdominal recordings were characterised by the sudden appearance and disappearance of FECG signals. This effect could be due to the fetus moving in and out of positions from which a good FECG can be obtained. The time scale for these changes varied from a matter of seconds, in recordings made between 27 and 34 weeks, to a matter of minutes, in the recordings made at 39 weeks.

These findings present a strong case for the development of a long-term recorder, as they suggest that although initially no FECG is obtained, a usable complex may appear if the recording period is extended.

In addition to the potential clinical applications of a long-term ambulatory recorder of FHR, such an instrument may prove to be of value as a research tool. To date, the lack of suitable instrumentation has prevented long-term studies of continuos beat-to-beat FHR from ever being undertaken. This fact alone could be justification for investigating normal antepartum long-term FHR patterns. Such a study could be used to investigate the effect on FHR of various maternal activities, such as smoking, drinking, drugs, exercise and eating, as well as to investigate the possible correlation between FHR and MHR.

In order to obtain long-term FHR and MHR recordings from abdominal electrodes, a suitable method of extracting the HR values is required. HR traces described in this thesis were obtained using an existing software package, designed for use with both an abdominal and a thoracic channel. This program runs in real time on a 386 PC.

The most important factor determining the quality of FHR and MHR traces that can be obtained with this (and any) package is, not surprisingly, the size of the FECG complexes with respect to the background noise. However, it is also important to be able to detect and subtract the MECG. In a system which records only an abdominal signal, a more robust method than simple threshold detection is required. This is particularly the case when the MECG is small and is of a similar size to the FECG. MECG detection would be improved by the use of a matched filtering scheme, provided that a reliable method of obtaining an initial template can be found. It should be possible to differentiate between

MECG and FECG complexes of a similar size by measuring the corresponding QRS widths.

The FECG was recorded in order to assess the potential of an ASIC based ambulatory long-term FHR recorder. Once downloaded to a PC the FECG recordings were processed by a windows based FECG analysis package in order to extract FHR and MHR traces. The eventual aim is to produce a DSP based version of the general electrophysiological signal recorder which can be configured as an ambulatory FHR recorder. This instrument will use the DSP to extract the FHR and MHR. It is important to remember that for an ambulatory FHR recorder, all processing must be done in real time. Therefore it is important to choose a processor which is powerful enough to implement all the processing steps, whilst small and low power enough, that the ambulatory nature of the recorder is not compromised.

CHAPTER 7

EHG RECORDINGS

7.1. Introduction

In this chapter, the recording of the electrohysterogram (EHG), using the general electrophysiological signal recorder (described in Chapter 6), is investigated, as a possible alternative means of identifying uterine contractions during labour. In the longer term, it is hoped that the findings of this study may lead to the development of an ambulatory recorder of premature contractions and antepartum fetal heart rate (FHR). As well as a preliminary investigation into the usefulness of the EHG, this study provides a further opportunity to test the general electrophysiological signal recorder both in terms of its performance and its flexibility. Although it is accepted that for monitoring during labour an ambulatory instrument is not required, the general electrophysiological signal recorder, being small and battery operated, is relatively unobtrusive and poses no problems of electrical isolation. A description of how this instrument can be configured to record EHG signals is included, together with a results section, in which uterine contractions traces derived from the EHG, are presented. The chapter begins by introducing the EHG as a potential measure of uterine activity.

7.2. The Electrohysterogram

The EHG is the name given by Steer and Hertsch in 1950 to the uterine electromyogram (EMG) signal when recorded via electrodes placed on the abdomen of pregnant women. Contraction of the uterine muscle in a pregnant woman causes an increase in intrauterine pressure (IUP). This increase in IUP, measured with a catheter positioned in the uterine cavity, occurs in phase with EHG activity [Devedeux et al., 1993]. Uterine EHG activity can be recorded

from as early as the 18th week of pregnancy [Gondry et al., 1993]. The amplitude of the EHG signal increases, relative to noise, as the pregnancy progresses.

It has been reported that the EHG contains two types of signal: a slow wave, which is in phase with IUP and a fast wave superimposed on top of this slow wave [Marque et al, 1986]. The slow wave ranges from 0.01 to 0.03 Hz with amplitude between 0.5 and 15 mV, whereas the fast wave ranges from 0.2 to 3 Hz and has an amplitude between 0.02 and 0.5 mV. Marque also observed that the fast wave could be further split into two frequency components: a low frequency band (FW_L) always present in every contraction (0.2 to 0.45 Hz), and a high frequency band (FW_H) related to efficient parturition contractions (0.8 to 3 Hz). This work led to the conclusion that abdominal activity is representative of genuine uterine EMG activity only when it is observed in the frequency band corresponding to the fast wave.

The cardiotocograph (CTG), which produces a record of uterine contractions and fetal heart rate (FHR), is the primary means of monitoring for potential cases of fetal hypoxia during labour. In the main, uterine contractions are obtained using an external strain gauge tocometer which can be both uncomfortable for the mother and unreliable when used on obese women. The alternative to the external tocometer is an internal pressure transducer which provides a much more accurate measure of intra uterine pressure (IUP) but has the disadvantage of being invasive. An EHG based tocograph, requiring only abdominal electrodes, would be both non invasive and unobtrusive.

A previous attempt to record uterine contractions from abdominal electrodes has been reported by Nagel and Schaldach (1983). This work made use of much higher frequency components than are usually recognised as being part of

the EHG (150 Hz to 250 Hz). In basing their recordings on the upper frequency range of uterine EMG, they argued that suppression of the traditional sources of interference, namely the maternal and fetal ECG, as well as artefact due to movement, is easily achieved. In addition, the selection of this frequency range means that recordings include components due to the EMG of the abdominal wall. This is claimed to be desirable as contractions of the abdominal wall also contribute to an increase in IUP.

7.3. EHG recorder

The general electrophysiological signal recorder was configured as an EHG recorder in order to record uterine activity from cutaneous electrodes placed on the maternal abdomen. The aim was to investigate the possibility of monitoring uterine contractions during labour using cutaneous electrodes.

When configured to record EHG signals, the ADC is set to digitise at 75 Hz and at a resolution of 16 bits. With a 512K x 8 bit SRAM this configuration gives a record time of just under 1 hour. The bandwidth of the recorder is set between 0.2 and 8 Hz. The high pass cut-off is chosen to be 0.2 Hz as this is the lower end of the EHG fast wave, while the low pass cut-off is chosen to be at 8 Hz in order to prevent aliasing. Table 7.1 contains the component values used in the analogue front-end of the EHG recorder (see Figure 6.3).

The general instrument was changed from FECG recorder (see Chapter 6) to EHG recorder and vice-versa on numerous occasions. This involved the setting of six dual-in-line switches, the replacement of 4 plug-in capacitors and the adjustment of two potentiometers (used to set the gain). The whole procedure takes no more than a couple of minutes to complete.

Component	Value
R1	750Ω (all resistors < 5 %)
R2-R7	20K
R8-R9	510K
R10	100K
R11	33K
R12	330K
R13	62K
R14	620K
R16	2 x 620K
R17	1.6K
VR1 *	50K
VR2 *	470K
C1-C2 *	1μF (polyester 10 % tolerance)
C3 *	220nF (polyester 10 % tolerance)
LED	SFH450V

Table 7.1: Component values for analogue front end of EHG recorder with programmable components indicated *.

7.4 EHG results

A total of twelve EHG recordings were taken from eight different mothers during the first stage of labour. All these recordings were taken on the labour ward at the Queen's Medical Centre, Nottingham. The general electrophysiological signal recorder was situated in the delivery room, with the mother, while the author sat in a nearby room observing the EHG signal on an oscilloscope, connected to the recorder via the optical link. Simultaneous recordings of uterine contractions were made using an external tocometer or an internal pressure transducer. These records of uterine contractions were used to validate the presence of possible contractions found in the corresponding EHG recordings. Of the twelve EHG recordings taken eleven were made simultaneously with an external tocometer and one with an internal pressure transducer.

7.4.1. Electrode type and position

Three disposable, foam backed, silver-silver chloride, solid gel electrodes (3M 2237) were used in all the EHG recordings. Before attaching the electrodes, the patient's skin was prepared with an alcohol saturated swab and left to dry for around 5 minutes. The two differential input electrodes were positioned vertically in the midline, 10 cm above and 10 cm below, the umbilicus (fundal and supra pubic), with the third 'common' electrode placed on the mother's wrist. In one recording a horizontal electrode configuration was tried.

7.4.2. Processing of EHG signals

In order to compare the EHG recordings with the contractions obtained using an external tocometer or an internal pressure transducer it is necessary to process the EHG recording into a trace of a similar form. The necessary processing is implemented in three stages, once the data has been successfully downloaded to a PC. The various processing steps are illustrated in Figures 7.1 to 7.4 with the corresponding tocograph shown in Figure 7.5. Each trace is 26 minutes long and is displayed on a scale of 0.5 cm per min. Firstly, the raw EHG recording (Figure 7.1) is band passed filtered from 0.2 to 4 Hz (Figure 7.2), in order to maximise the frequency components pertaining to the EHG fast wave. The envelope of the band passed signal is then extracted by full wave rectifying (Figure 7.3) and finally smoothed, using a low pass filter with a cut off at 0.01 Hz (Figure 7.4). Both filtering stages are implemented using digital FIR filters designed with the Hypersignal software package. An example of the raw EHG pertaining to a single contraction is shown in more detail in Figure 7.6. This particular trace contains a one minute extract from the raw EHG shown in Figure 7.1, which relates to the third contraction at approximately ten minutes. The upward spikes are due the maternal ECG whilst the underlying oscillations are considered to be related to uterine contractions.

Figure 7.1: Raw EHG recording, duration 26 minutes

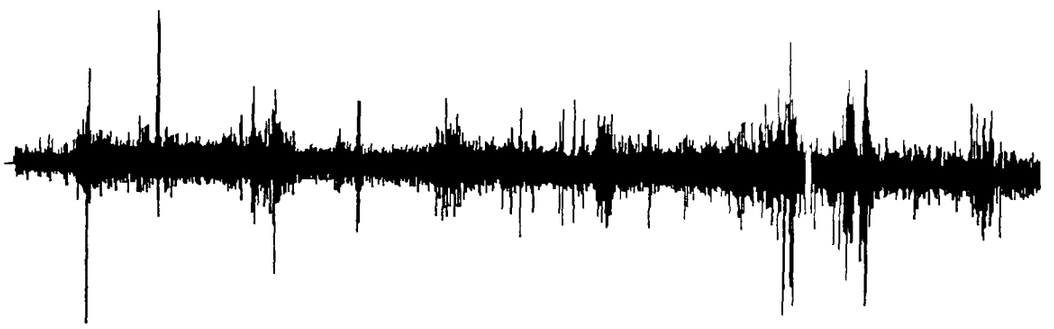


Figure 7.2: Bandpass filtered signal (0.2-4 Hz)

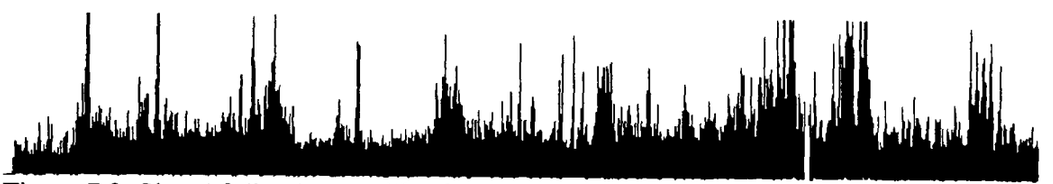


Figure 7.3: Signal following rectification

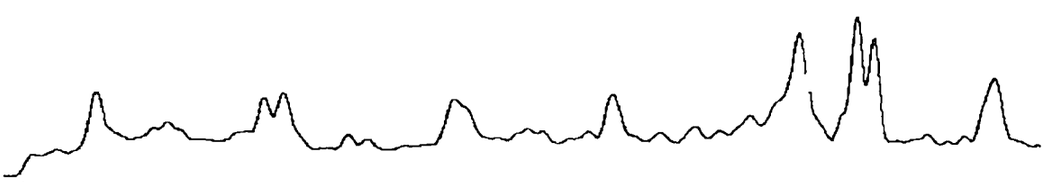


Figure 7.4: Signal following low pass filtering (< 0.01 Hz)

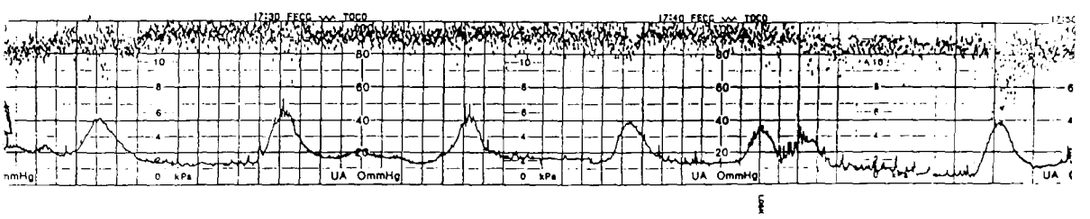


Figure 7.5: Corresponding CTG trace recorded using an internal pressure transducer

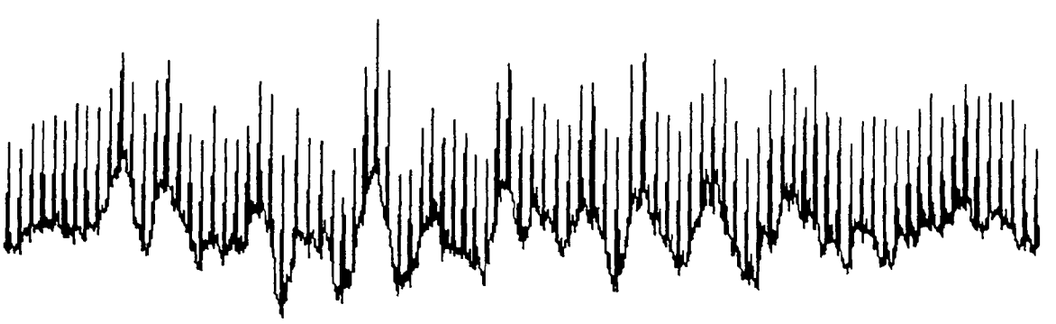


Figure 7.6: Raw EHG signal, duration 1 minute taken from recording in Figure 7.1

7.4.3. EHG and CTG tocographs

Examples of processed EHG signals can be seen in Figures 7.7 to 7.10 together with their corresponding CTG trace. Each trace is 24 minutes long and is displayed on the standard scale of 1 cm per min.

Figure 7.7 is taken from mother A with an external tocometer based CTG. Both the EHG and the CTG contractions are of a high quality, with every contraction clearly identifiable. It can also be observed that the EHG contractions appear to be of a shorter duration.

Figure 7.8 is taken from mother B with an external tocometer based CTG. Once again the EHG contractions tend to be marginally narrower than the corresponding CTG contractions. In addition, the EHG tocograph contains what seems to be an extra smaller contraction around 15 minutes into the trace. Similar extra, small contractions were found in other sections of this and other EHG recordings. This could be due to interference from movement artefacts or may represent some other uterine electrical activity, with little or no corresponding mechanical activity.

The trace in Figure 7.9 is taken from mother C with an external tocometer based CTG. Moderate quality tocographs are obtained from both the EHG and the CTG.

The trace in Figures 7.10 is taken from mother D with an internal pressure transducer based CTG which, as expected, is of a high quality. In this example a moderate quality EHG tocograph is obtained. Note the extra EHG activity located around 19 minutes into the recording. Once again, this could be due to interference from movement artefacts or may represent some other uterine electrical activity, with little or no corresponding mechanical activity.

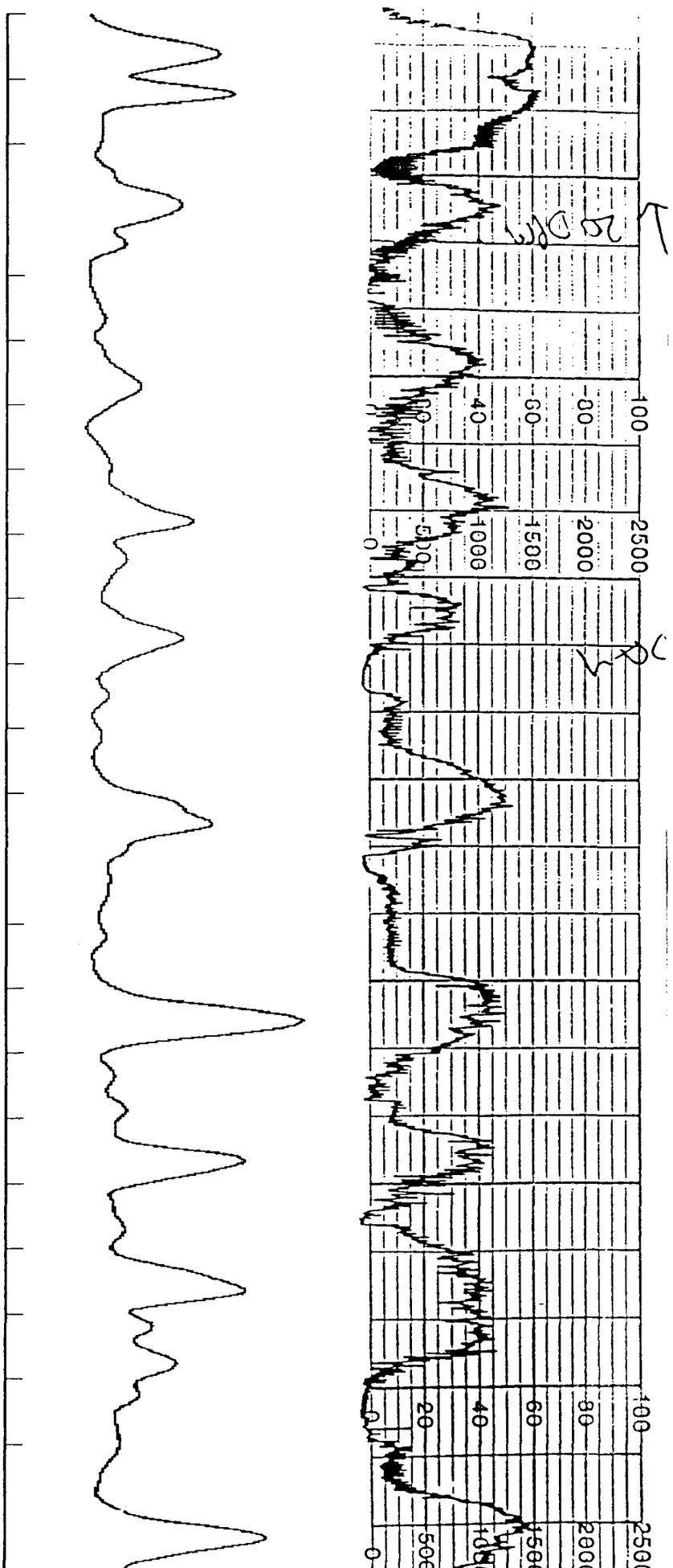


Figure 7.7: CTG tocograph (upper) and EHG tocograph (lower) taken from mother A.

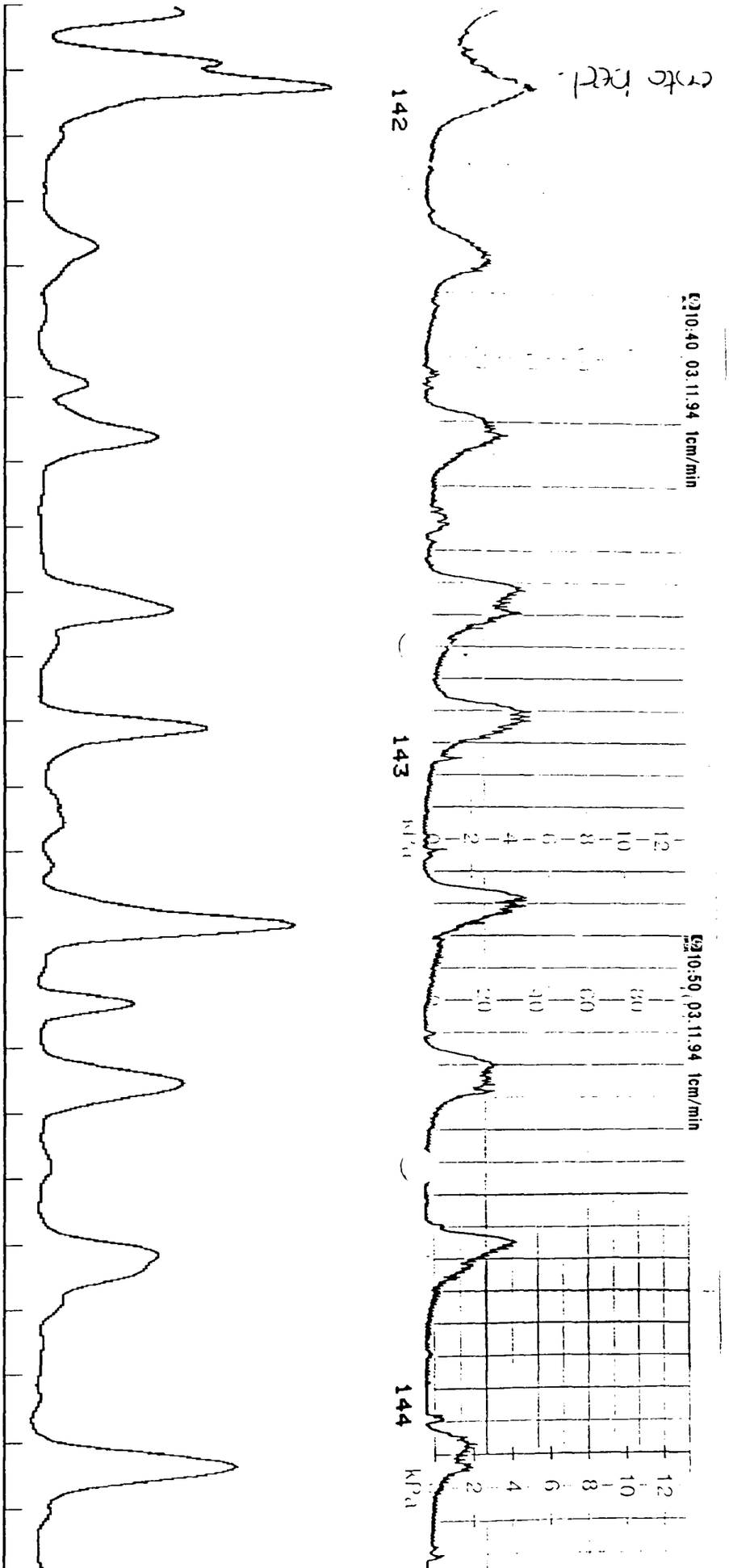


Figure 7.8: CTG tocograph (upper) and EHG tocograph (lower) taken from mother B.

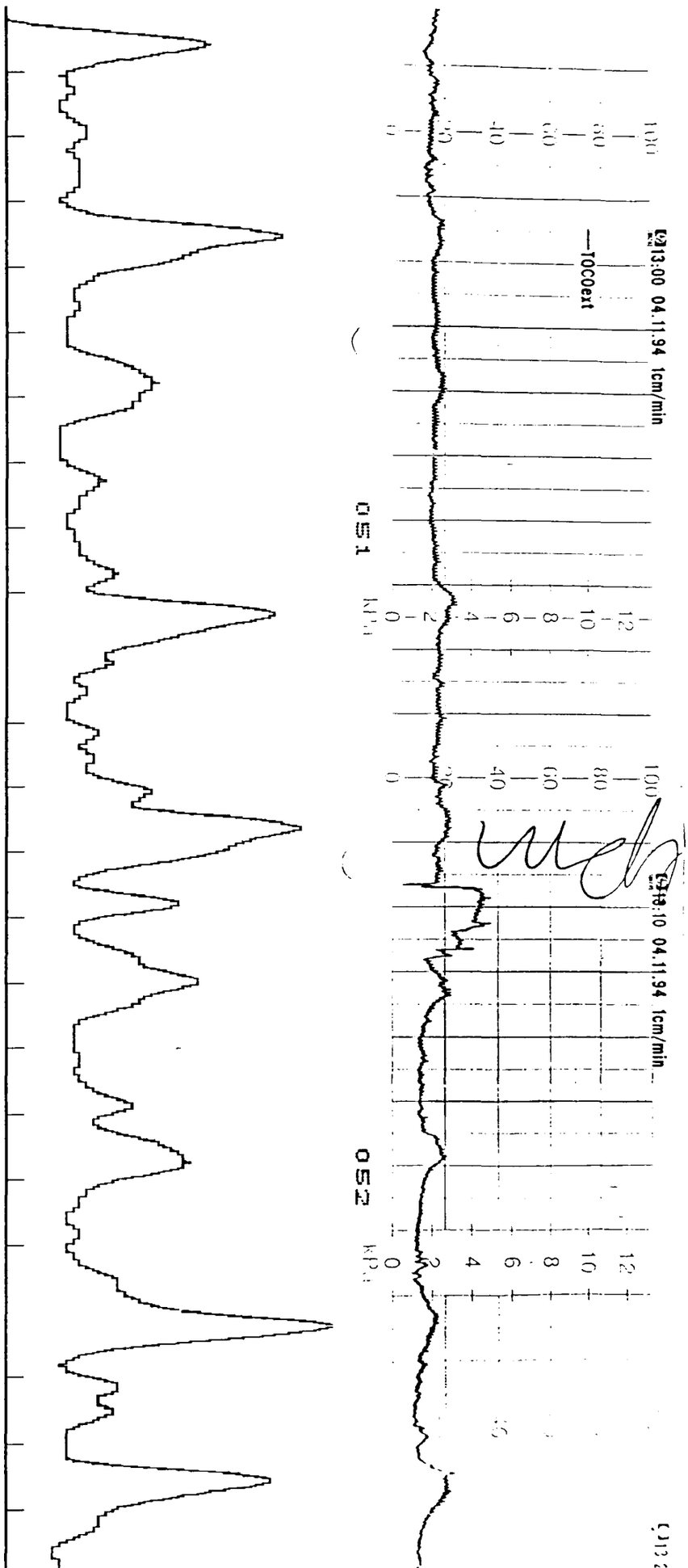


Figure 7.9: CTG tocograph (upper) and EHG tocograph (lower) taken from mother C.

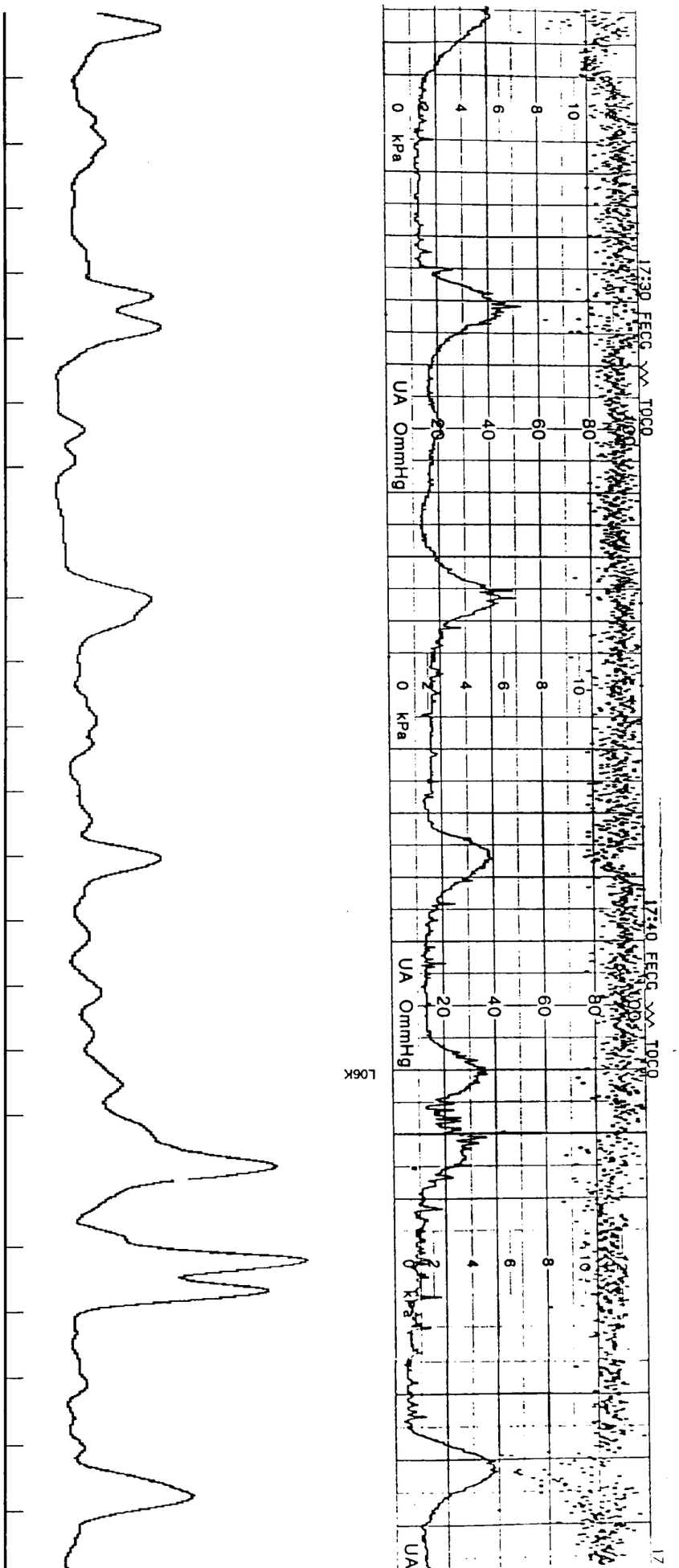


Figure 7.10: CTG tocograph (upper) and EHG tocograph (lower) taken from mother D.

7.5 Conclusions

The general electrophysiological signal recorder has been used to record the EHG. Twelve recordings were taken from eight different mothers all during the first stage of labour. Once downloaded to a PC, these recordings have been processed into tocographs and compared with tocographs made simultaneously using a conventional CTG machine. Eleven of the EHG recordings demonstrated a strong correlation, whilst the remaining recording could not be assessed due to the extremely poor quality of the corresponding CTG. In this case, the mother concerned was the most obese woman in this particular study, and therefore the low quality of the external tocograph was not unexpected.

The EHG tocographs were often characterised by the presence of extra smaller contractions. This could be due to interference from movement artefacts, the electrical activity of the intestine and bladder, changing electrode potentials, skin potentials or may represent some other electrical uterine activity. In addition, it was observed that the EHG derived contractions tended to be slightly narrower than those of the corresponding CTG, which may be due to their electrical as opposed to mechanical nature.

Interestingly, the EHG recording obtained using a horizontal electrode configuration provided a contractions trace of similar quality to those obtained using a vertical electrode configuration. This suggests that the positioning of the electrodes is not too critical.

The processing employed to produce the contractions trace from the raw EHG utilises the frequency components between 0.2 Hz and 4 Hz, which are reported to be present during uterine contractions. Other signals in this bandwidth include elements of both the MECG and FECG as well as motion artefact caused by electrode movements. Possible methods of reducing these

interfering signals could include, subtraction of the MECG and better electrode positioning.

It may also be advantageous to investigate the contribution to contraction strength of voluntary abdominal wall EMG. These signals are generally of a much higher frequency content (around 100 Hz) than the EHG and hence are filtered out using the existing processing scheme. By employing a series of bandpass filters, a better understanding of the frequency components of the abdominal recordings required to produce a high quality tocograph, may be investigated.

Following the initial success of this preliminary study several other applications of the EHG recordings become worthy of investigation. Firstly, by using a multi-channel instrument a measure of contraction propagation may be possible. Good quality, efficient parturation contractions will propagate down the mothers abdomen in order to push the fetus down the birth canal. For this to occur there needs to be a degree of co-ordination in the contraction of the individual uterine muscles. A multi-channel instrument would provide a means of assessing the quality of contractions in terms of the amount of co-ordination of the individual uterine muscles. Secondly, by correlating EHG derived contraction traces with simultaneously recorded IUP traces, the possibility of using the EHG as a non-invasive measurement of IUP could be investigated. If successful, the need for the highly unpopular, invasive IUP transducer would be eliminated. If the actual strength of the contractions could be assessed it would allow the more rational augmentation of contractions with synthetic oxytocin.

But perhaps the most valuable potential application of the EHG is the possibility of detecting premature contractions at an earlier stage of pregnancy

than is currently possible. This application would require an ambulatory monitor with the necessary processing power to detect low level EHG activity. The DSP based general electrophysiological signal recorder would seem to be the ideal device to use for this application.

CHAPTER 8

CONCLUSIONS AND FURTHER WORK

8.1. Conclusions

The ability of application specific integrated circuits (ASICs) to minimise the size and power consumption of electronic circuitry makes their application to the design of long-term ambulatory monitoring equipment an attractive option. Two areas of study were chosen as vehicles for investigating the value of ASICs to ambulatory monitoring: long-term heart rate variability (HRV) studies and monitoring in obstetrics. It was proposed that two ASIC based instruments should be developed: a long term recorder of adult heart rate (HR) and a general electrophysiological signal recorder.

As part of the investigation into the suitability of ASICs for ambulatory monitoring, the value of field programmable gate arrays (FPGAs) was tested by prototyping the digital circuitry of the adult HR recorder with such an IC. The advantages of low cost, at low volume and fast design turn around times make FPGAs ideally suited for this purpose. In addition, the inclusion of the FPGA within a prototype instrument provided a means of testing not only the operation of the digital circuitry but also the performance of the adult HR recorder design as a whole.

A multi-purpose mixed ASIC was then designed, containing both the adult HR recorder and the general electrophysiological signal recorder circuits. This approach allowed both circuits to be tested for the price of one design run, with minimal increase in overall size and power consumption, as much of the circuitry is common to both designs.

Once fabricated, the ASIC was firstly incorporated into an ambulatory long-term adult HR recorder, which was then employed in a study of long-term daily HR patterns. This study verified the ambulatory nature of this instrument as well as its suitability for investigating HRV.

Secondly, the ASIC was incorporated into a general electrophysiological signal recorder. This initial version records electrophysiological signals directly into static RAM (SRAM), with the intention being that the next version would include a digital signal processor (DSP), capable of processing signals in real time. This instrument was used then to obtain data of clinical interest.

Firstly, recordings of the antepartum abdominal fetal electrocardiogram (FECG) have been taken which show that a usable signal can be obtained from a mother in her home environment, and in various postures. The sudden appearance and disappearance of FECG signals in several of these recordings suggests that although initially no signal may be obtained, a usable complex may appear if the recording period is extended. The results of this study have shown both the feasibility and the value of developing an ASIC based long-term recorder of both fetal and maternal HR (FHR, MHR). However, the absence of a clear FECG complex in many of the recordings, suggests that such an instrument is unlikely to be able to obtain a FHR trace all of the time. This is most likely to be the case between 29 and 33 weeks gestation when the occurrence of the FECG signal was noted to decrease, in agreement with other workers in this field.

Secondly, the general electrophysiological signal recorder was used to record the electrohysterogram (EHG), which is the name given to the electrical activity of the uterus, from abdominal electrodes during labour. A strong correlation was found to exist between tocographs derived from the EHG and

tocographs produced by conventional methods. As well as testing both the operation and the flexibility of the ASIC based general electrophysiological signal recorder, this study investigated the recording of EHG as a basis for a possible alternative, noninvasive, unobtrusive method of measuring uterine activity during labour, which may in turn lead to the development of an ambulatory, antenatal monitor of premature contractions.

8.2. Possible improvements to the ES2 ASIC design

The ES2 ASIC has shown the feasibility of an ASIC based adult HR recorder and an ASIC based general electrophysiological signal recorder. In order to optimise the performance of both of these instruments in terms of size and power consumption it would be advantageous to fabricate both circuits individually rather than to further develop a multi-purpose ASIC.

Other improvements in terms of size, power consumption and speed could be achieved by migrating to a superior mixed analogue and digital process, such as the Mietec 0.7 μm process. Lower power op-amps within the core would reduce the power consumption, which in turn would reduce the size of the batteries, as well as reducing the pad limited nature of the ASIC. However, care would need to be taken in isolating these op-amps from the noisy digital circuitry. A process which could integrate some or all of the external resistors and capacitors would be useful in minimising the overall instrument size.

8.3. Possible improvements to adult HR recorder

Improvements to the existing HR design could include an automatic gain scheme and the inclusion of a PCMCIA card (Personal Computer Memory Card International Association), on which to store the HR data. Automatic gain would make the R-peak detection scheme more robust and less prone to missed beats. It would also allow the sensing electrodes to be placed on

different parts of the body. This would be particularly useful for subjects possessing large amount of chest hair. Storing HR data on PCMCIA cards would greatly increase the rate at which data can be downloaded to a PC and would solve the download problem. As PCMCIA cards are non-volatile, the need to download recorded data immediately would be eliminated. The major drawbacks to PCMCIA cards are the cost and size of the cards and connectors. Another possible addition to the HR recorder design could be the inclusion of a real time clock IC, capable of date stamping the data. Although this would require an extra component it would eliminate the need for time markers.

A further reduction in the size of the HR recorder design would be best achieved by reducing the power consumption, as this would allow smaller batteries to be used. One method of reducing power consumption would be to implement the existing recorder design using 3 V technology. A smaller recorder would also be obtained if surface mount components were used.

8.4. Possible improvements to the general electrophysiological signal recorder

The flexibility of a DSP based instrument would allow it to be applied to many different electrophysiological signals. This flexibility could be taken one step further by redesigning the ASIC to be multi-channel. A multi-channel recorder would allow the simultaneous recording of different, but related, physiological parameters, such as ambulatory HR, with blood pressure and posture, although this would require the inclusion of suitable transducers. A multi-channel system could also prove to be a useful tool in determining optimum electrode positions.

A thorough investigation into the source of the switching noise is necessary in order to eliminate this type of interference from future recordings. When

present this type of interference introduces a noise component which is equivalent to around 10 μV when referred to the recorder input. For abdominal recordings, the minimum amount of muscle noise is of a comparable amplitude (when mother is lying down). Therefore, for recordings taken with the mother in this position, the ability to detect FECG complexes may, to a limited extent, be compromised by the switching noise.

8.5. Recent developments

Following on from this work a second ES2 ASIC has recently been fabricated with only the front-end circuitry needed for the DSP based general electrophysiological signal recorder included from the original ASIC design, together with some additional logic to improve the interface with the TMS320C50 DSP [Texas Instruments, 1991]. In this design the download problem will be solved by using the DSP to transfer data to the PC. A reduction of the switching noise present with the original ASIC design has also been attempted. The method was to include more analogue power supply pads and place them directly next to sensitive op-amps. It is hoped that interfering digital switching noise can be further reduced by decoupling closer to individual op-amps. A DSP based general electrophysiological signal recorder incorporating the new ASIC has now been constructed and is currently undergoing initial tests. It is intended that this instrument will be used as a recorder of long term FHR and MHR, as a recorder of adult ECG arrhythmias, to investigate the possibility of monitoring premature uterine contractions and to investigate the electrophysiological signal emanating from the stomach (the electrogastrogram (EGG)).

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APPENDIX A

A. Electrical safety of battery operated medical equipment

The safety of medical electrical equipment is covered by the British Standard 5724 [BS5724]. This Appendix highlights the parts of BS5724 that are relevant to the design of battery operated medical equipment.

The general requirement of BS5724 states that equipment shall when, operated in normal use, cause no safety hazard which could reasonably be foreseen, in normal condition and in single fault condition.

A.1. Terminology and definitions

"shall" means that compliance is mandatory.

"should" means that compliance is recommended but is not mandatory.

Applied Part - Entirety of all parts of the equipment including the patient leads which come intentionally into contact with the patient to be examined or treated.

Patient auxiliary current - Current flowing in the patient in normal use between parts of the applied part and not intended to produce a physiological effect.

Patient leakage current - Current flowing from the applied part via the patient to the enclosure of battery powered equipment.

Normal condition - Condition in which all means provided for protection against safety hazards are intact.

Single fault condition - Condition in which a single means for protection against a safety hazard in equipment is defective or a single external abnormal condition is present.

A.2. Equipment classification

Equipment is classified according to the type of protection against electric shock. Mains powered equipment is classified as either class1 or class 2 whereas battery powered equipment is simply classified as internally powered equipment.

Battery powered equipment can be classed as one of three types, B, BF or CF, according to the degree of protection against electric shock: Type BF has the same degree of protection as type B but contains an isolated (floating) applied part. Type CF has a higher degree of protection than type BF and is required for equipment which contacts directly to cardiac muscle.

Equipment containing a non isolated applied part which is connected to skin electrodes is classed as being of type B.

A.3. Identification, marking and documentation.

Identification and markings shall be permanently affixed and clearly visible i.e. removable with a tool only or by appreciable force, with instructive statements being legible from the operators position.

Markings shall include an indication of origin, a model or type reference and a symbol indicating the type of equipment (B, BF or CF). Different positions of switches shall be indicated by figures, letters or other visual means.

Red indicator lights shall be used exclusively to indicate a warning of danger and/or a need for urgent action. Green indicator lights should be used to indicate that the equipment is ready for action (power on). Yellow indicator lights should be used to indicate caution or attention required.

Equipment shall be accompanied by documents containing at least instructions for use, a technical description and an address to which the user can refer. Instructions for use shall contain all information necessary to operate the equipment in accordance with its specification. This shall include explanation of the function of the controls, displays and signals, the sequence of operation and the connection and disconnection of detachable parts. Instructions for use of equipment containing primary batteries shall contain a warning to remove these batteries if equipment is not likely to be used for some time.

The technical description shall contain a statement that the supplier will make available on request circuit diagrams, component part lists, descriptions, calibration instructions, or other information which will assist the user's appropriately qualified technical personnel to repair those parts of equipment which are designated by the manufacturer as repairable.

A.4. Protection against electric shock hazards

Equipment shall be so designed that the risk of electric shock on normal use and in single fault condition is obviated as far as is practicable. For equipment of type B under normal conditions the patient leakage current must not exceed 100 μA and the patient auxiliary current must not exceed 10 μA (dc.). Under single fault conditions the maximum allowable patient leakage current is limited to 500 μA and the maximum patient auxiliary current is limited to 50 μA (dc.)

The patient leakage current shall be measured in type B equipment, from all patient connections connected together or with applied parts loaded according to the manufacturer's instructions. The patient auxiliary current shall be measured between any single patient connection and all other patient connections connected together.

APPENDIX B

B. Reduction of noise and 50 Hz interference in biopotential amplifiers

This appendix is intended as a guide to minimising the various interference and noise sources, which are characteristic of electrophysiological recordings, derived from cutaneous electrodes. A description of the various noise sources is given together with a set of recommended recording procedures, which, if implemented, should keep noise and interference to a minimum. The work described in this appendix is taken from several publications which are concerned with the reduction of noise and 50 Hz interference in biopotential amplifiers, [Huhta and Webster, 1973], [Thakor and Webster, 1980], [Winter and Webster, 1983] and [Thakor, 1988].

The three most common artefacts found in recordings of electrophysiological signals are baseline drift, muscle noise and 50 Hz interference.

B.1. Baseline drift (baseline wander)

Baseline drift or wander, as it is also known, is the term given to very low frequency changes in d.c. baseline that are often found in recordings of electrophysiological signals. Variations in the baseline are often far greater than the electrophysiological signal of interest. This can lead to problems of saturation, with the signal drifting out of the range of the recorder's amplifier. A reduction in gain can overcome problems of baseline drift, at the expense of resolution and dynamic range. Static voltages, skin potentials and motion artefacts are three causes of baseline drift.

Static voltages are built up on the body when friction, due to patient movement, causes Cb to charge up (see Figure B.1).

Skin potentials are either biopotentials generated by the epidermal layers of the skin or electrochemical potentials due to the interface of metallic electrode, conductive gel and skin (similar to a battery).

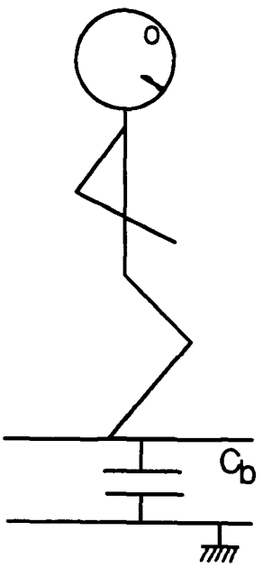


Fig B.1: Static voltage.

Motion artefacts are caused by deformation of the skin and the disturbance of the skin-electrode interface.

Baseline drift can be eliminated from many types of electrophysiological recordings by high pass filtering. For electrophysiological signals which contain important information at very low frequency (i.e.electrohysterogram), care must be taken in the selection of an appropriate high pass cut-off. If the cut-off of the high pass filter is too high, the low frequency components of the desired signal may be lost. A high pass filter, which removes frequency components that are below 1 Hz, will eliminate baseline drift in most cases. Other methods used to reduce skin potentials and motion artefacts include abrasion of the skin and punctuation of the epidermal skin layers.

B.2. Muscle noise.

The electrical activity of muscle often referred to as the electromyogram (EMG) is present to some degree in all electrophysiological signals. The level of muscle noise is dependent on the amount of patient movement as well as electrode position. In general, muscle noise is of a slightly higher frequency (order of 100 Hz) than other electrophysiological signals such as the

electrocardiogram (ECG). This means that a low pass filter can be used to remove muscle noise that is of a higher frequency than the signal of interest. Muscle noise can also be reduced by keeping patient movement to a minimum and by keeping electrodes away from large muscle groups.

B.3. 50 Hz interference.

50 Hz interference also referred to as a.c. pickup, hum and power line or mains interference, derives from two types of a.c. fields, magnetic or B fields measured in Webers per m^2 and electric or E fields measured in Volts per m. Common sources of a.c. fields include lights, a.c. wiring, a.c. power points and nearby electrical equipment. For a magnetic field to occur a current must flow. One common source of magnetic fields are the transformers found in power supplies. For electric fields a current need not flow. Any equipment connected to a power point will be a source of an electric field even when switched off.

The best way to eliminate the effects of 50 Hz interference is to try to eliminate all the a.c. fields at source i.e. by unplugging all nearby equipment. Another method of reducing the effect of a.c. fields is to use shielding. Shielding from electric fields requires a highly conducting surface (i.e. copper or aluminium). Shielding from magnetic fields requires a ferromagnetic material (i.e. a mu metal). Of course the elimination of all a.c. fields is impractical i.e. lighting is required to see and therefore other means are required, of reducing the amount of a.c. interference entering the electrophysiological signal amplifier.

There are four ways that a.c. interference can enter an amplifier.

- Magnetic induction into the patient leads
- Displacement current coupled into the patient leads
- Displacement current coupled into the patient
- Amplifier imperfections

B.3.1. Magnetic induction into the patient leads

Voltage induced in a conductive loop in the vicinity of a changing B field

$$\text{induced potential} = -\frac{dB}{dt}S$$

$$S = \text{area of loop, } B = 3.2 \times 10^{7}\ {}^{wb}/_{m^2}$$

$$\text{induced potential} \propto S$$

$$\text{induced potential} \cong 10\mu V \text{ for } S = 0.1\ m^2$$

Interference due to magnetic induction effects can be reduced by making the loop area S as small as possible. This can be achieved by keeping the patient leads short, close to the body and twisted together.

B.3.2. Displacement current coupled into the patient leads

The effects of displacement currents coupled into the patient leads can be modelled using the circuit diagram in Figure B.2. C_1 and C_2 represent the parasitic capacitance between the a.c. power line and the patient leads, through which displacement current is coupled. Points A and B represent the differential inputs of the amplifier, Z_1 and Z_2 represent the impedance of the electrode skin interfaces and Z_g represents the total impedance between the ground electrode and the amplifier common (including skin/ground electrode interface). Z_b represents the parasitic impedance between the patient and earth and Z_{iso} represents the parasitic impedance between the amplifier common and earth. Z_{IN1} and Z_{IN2} are the common mode input impedances of the differential inputs of the amplifier with Z_D being the differential input impedance. The internal body impedance is assumed to be negligible (usually <100 Ω). Z_{iso}, Z_D and Z_{IN} are assumed to be much larger than Z_1, Z_2 and Z_g.

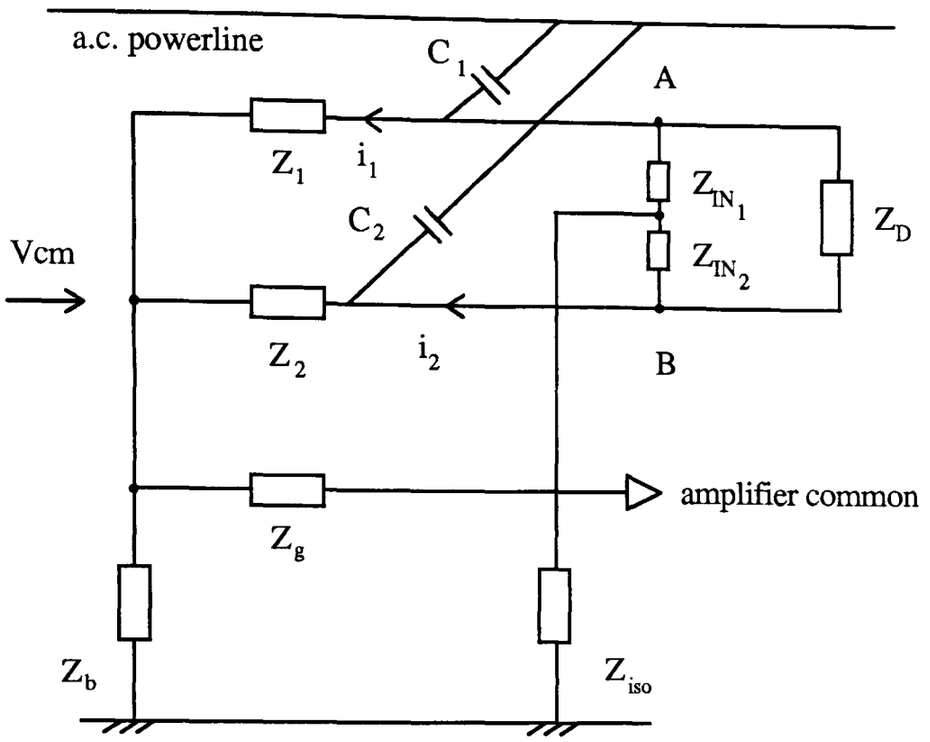


Fig B.2: Power line interference due to displacement currents coupled into the patient leads.

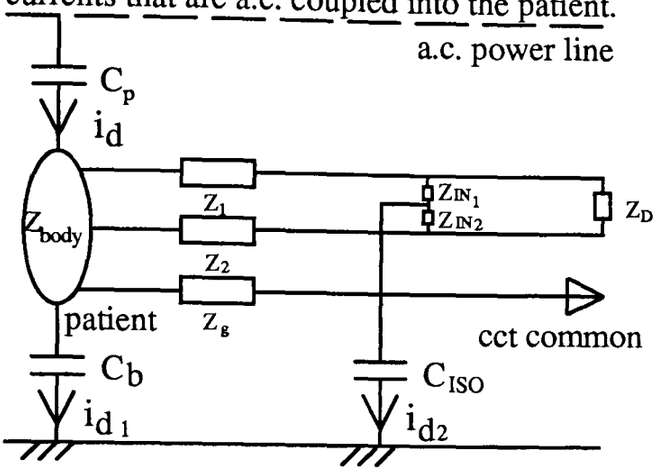
Any displacement current that is coupled into the patient leads will flow to earth by the path of least resistance. Power line interference will enter the amplifier if the displacement current coupled into the patient lead produces a voltage at point A which is different than the voltage at point B.

$$\mathbf{V_A - V_B = Z_1 i_1 - Z_2 i_2}$$

From the above equation it follows that this type of power line interference will occur if there is a large electrode impedance imbalance or if i_1 differs from i_2. However, as Z_b and Z_{iso} are usually much greater than Z_1 and Z_2 then $V_A - V_B$ should be negligible. If not, then i_1 and i_2 can be reduced by shielding the patient leads.

B.3.3. Displacement current a.c. coupled into the patient.

The circuit in Figure B.3 can be used to model the effect of displacement currents that are a.c. coupled into the patient.



Typical Values:

Z_1=30KΩ, X_b=10MΩ, i_d=0.1μA,

Z_2=20KΩ, X_p=1GΩ, i_{d1}=0.1μA,

Z_g=20KΩ, X_{iso}=1GΩ, i_{d2}=1nA,

Z_d=Z_1-Z_2=10KΩ,

Z_{IN1}=Z_{IN2}=Z_{CM}=100MΩ,

C_p=C_{iso}=2pF, C_b=200pF

Figure B.3: Displacement current a.c. coupled into the patient.

Huhta and Webster 1973, reported that the value of the displacement current i_d "will rarely exceed 1 μA even when holding onto an a.c. line cord and will more likely be about 0.1 μA". They also reported that "because the body has finite impedance, the displacement currents entering the body through the arms, legs and torso will cause different parts of the body to be at slightly different potentials". This could lead to a differential voltage at the input to the amplifier. The impedance of the body (Z_{body}) is around 20 Ω through the torso and can be as high as 400 Ω from shoulder to finger. As long as X_b is very much larger than Z_{body} then differential voltages should be negligible. If this is not the case then differential voltages may be reduced by putting electrodes closer together, although this may also result in reduction of the desired signal.

Assuming there is no significant differential voltage then the only interference caused by displacement currents in the patient will be due to a common mode voltage being converted into a differential mode voltage by the inadequacies of

Common mode voltage, $V_{cm} = Z_g.i_{d2}$. Therefore, good circuit common to earth isolation is important for battery powered amplifiers.

The differential voltage due to $V_{cm} = i_{d2}Z_g\left[\frac{1}{CMRR} + \frac{Z_d}{Z_{cm}}\right]$

Where CMRR is the common mode rejection ratio of the differential amplifier, Z_{cm} is the input impedance and Z_d is the electrode imbalance. Hence this type of interference can be reduced by increasing X_{iso}, CMRR and Z_{cm} and by decreasing Z_g and Z_d.

With CMRR = 1000;

$$V_{diff} = 1nA \times 20K\Omega\left[10^{-3} + 10^{-4}\right]$$
$$\approx 0.02\ \mu V$$

Winter and Webster 1983, presented a method of further reducing common mode voltages by implementing a right-leg-driver circuit. This circuit reduces the effective resistance between the patient and the amplifier common i.e. Z_g. This can be useful for cases of poor electrode contact between patient and circuit common. The right-leg-driver is more useful for mains powered amplifiers, when the circuit common is not isolated from earth. In this case, the patient should not be connected directly to the circuit common as this would introduce a safety hazard. The right-leg driver overcomes this problem by allowing only a safe amount of current to flow through the ground electrode.

B.4. Conclusion

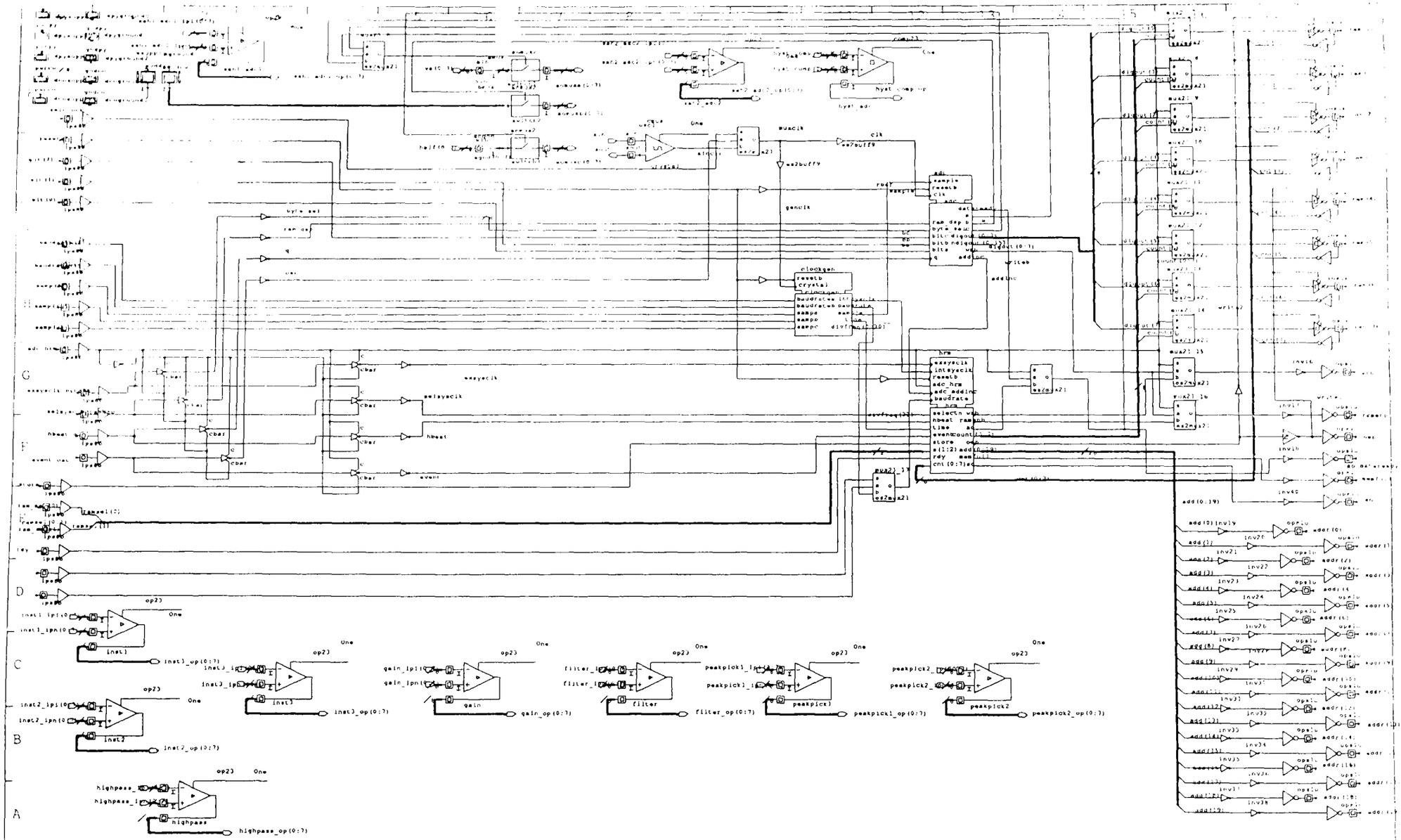
The amount of noise and 50 Hz interference in a biopotential amplifier can be summarised in the following equation :

$$V_n = KBS + i_1 Z_1 - i_2 Z_2 + i_d Z_{body} + i_{d2} Z_g \left[\frac{1}{CMRR} + \frac{Z_d}{Z_{cm}} \right]$$

To reduce the amount of noise and 50 Hz interference:

- Twist patient leads together and keep close to patient body.
- Shield patient leads.
- Place electrodes as close together as possible.
- Maximise: Isolation of amplifier common, CMRR and input impedance.
- Minimise: Electrode impedance imbalance, ground electrode impedance.

APPENDIX C: ASIC SCHEMATICS



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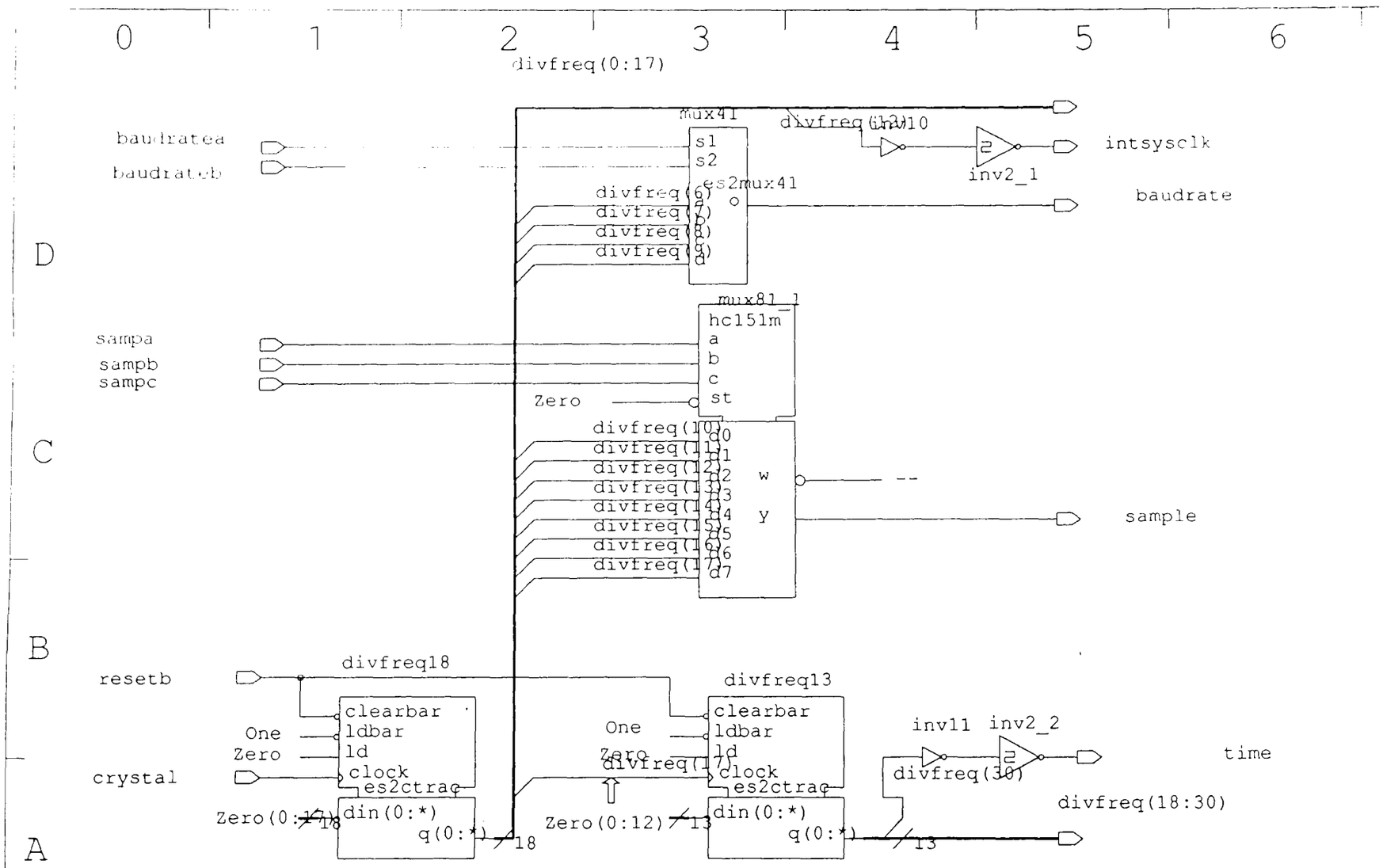

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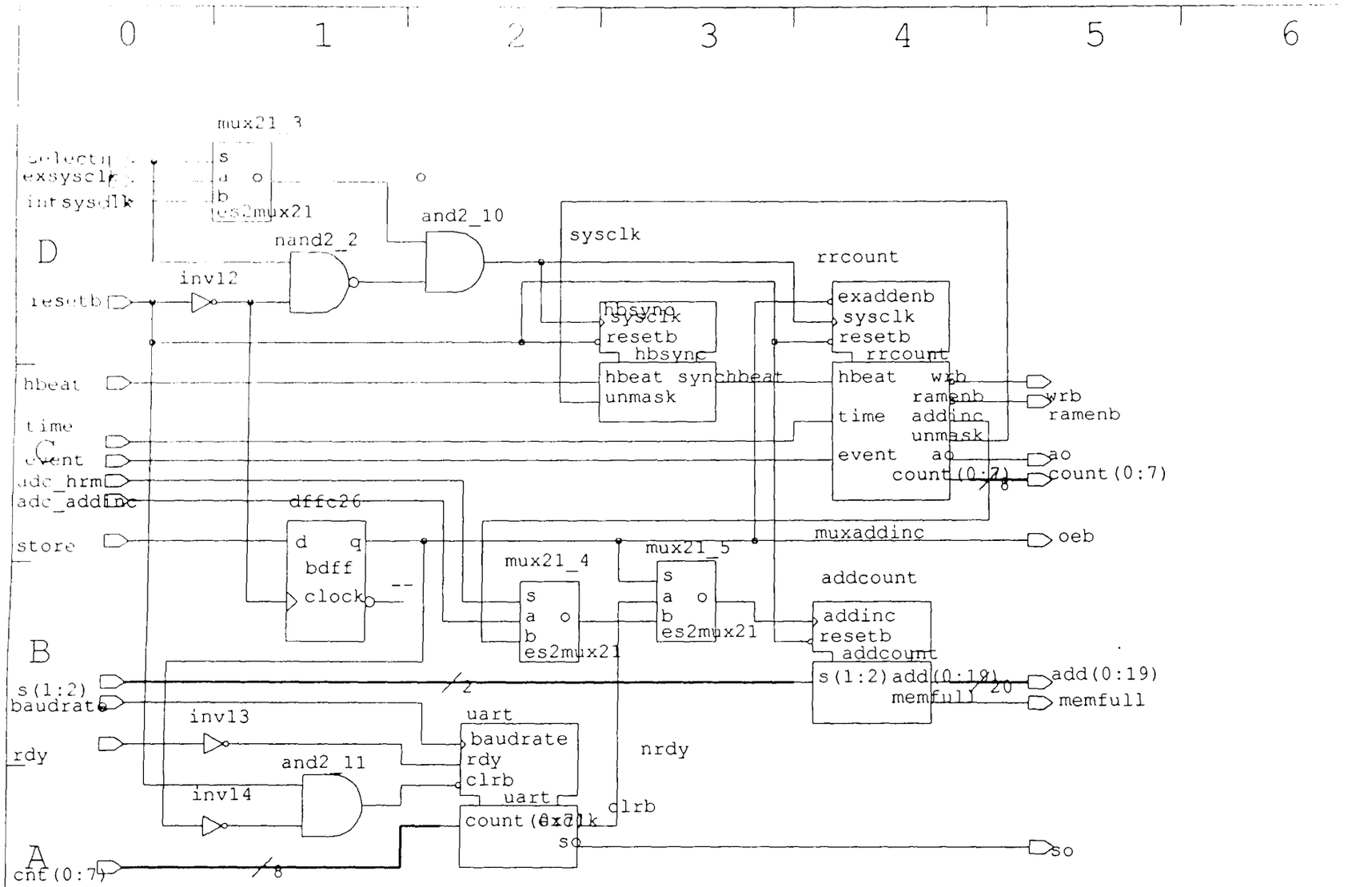

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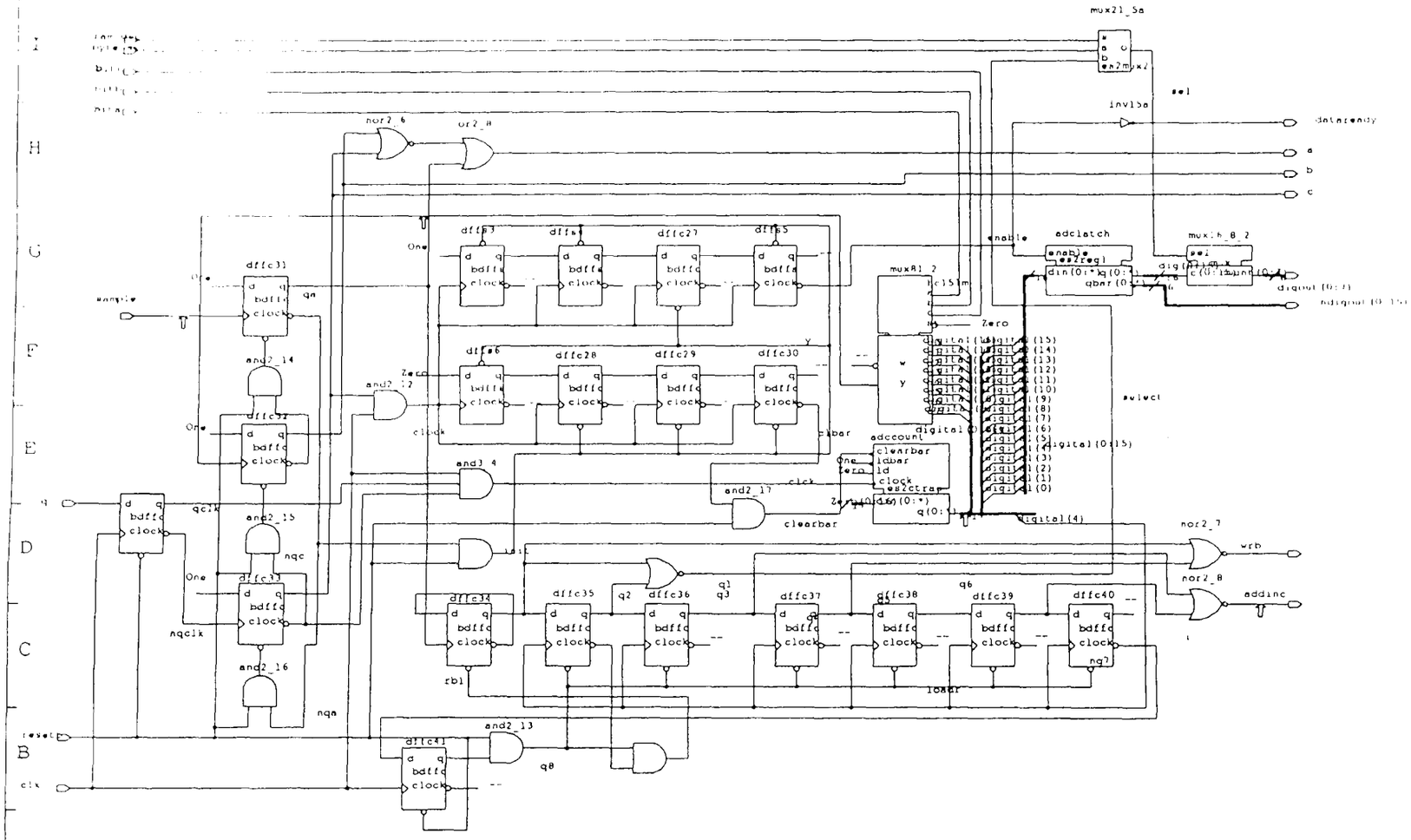

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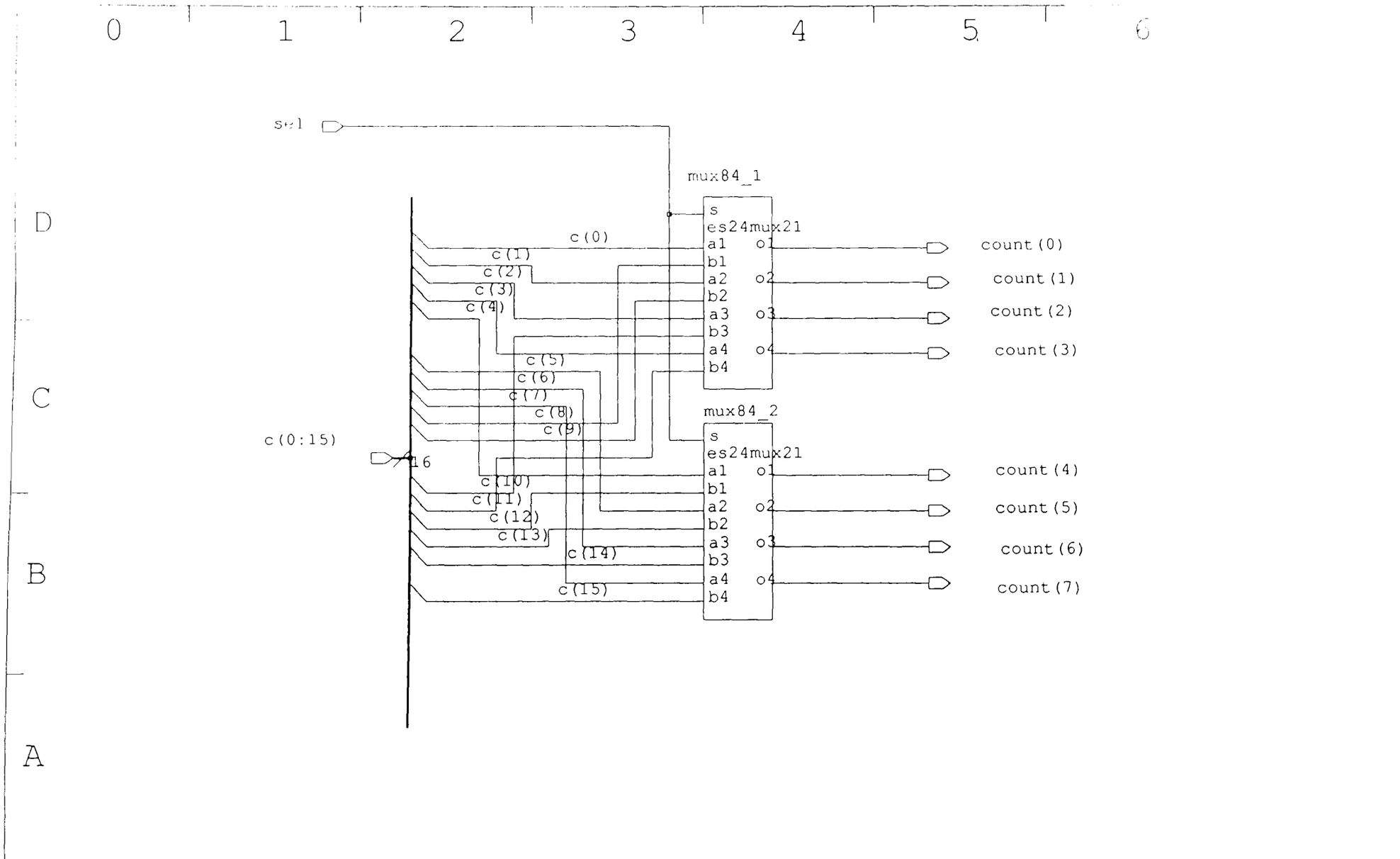

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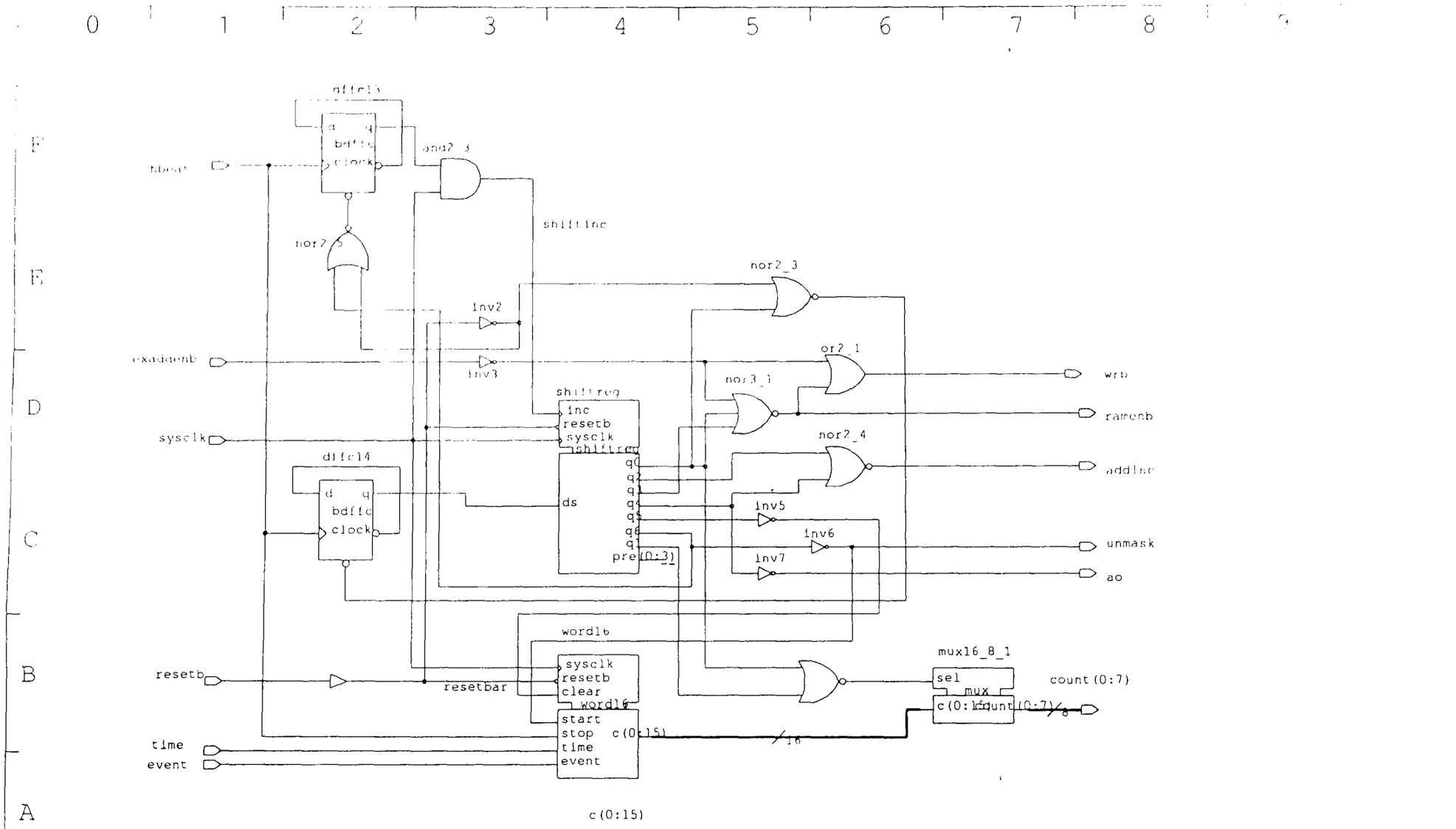

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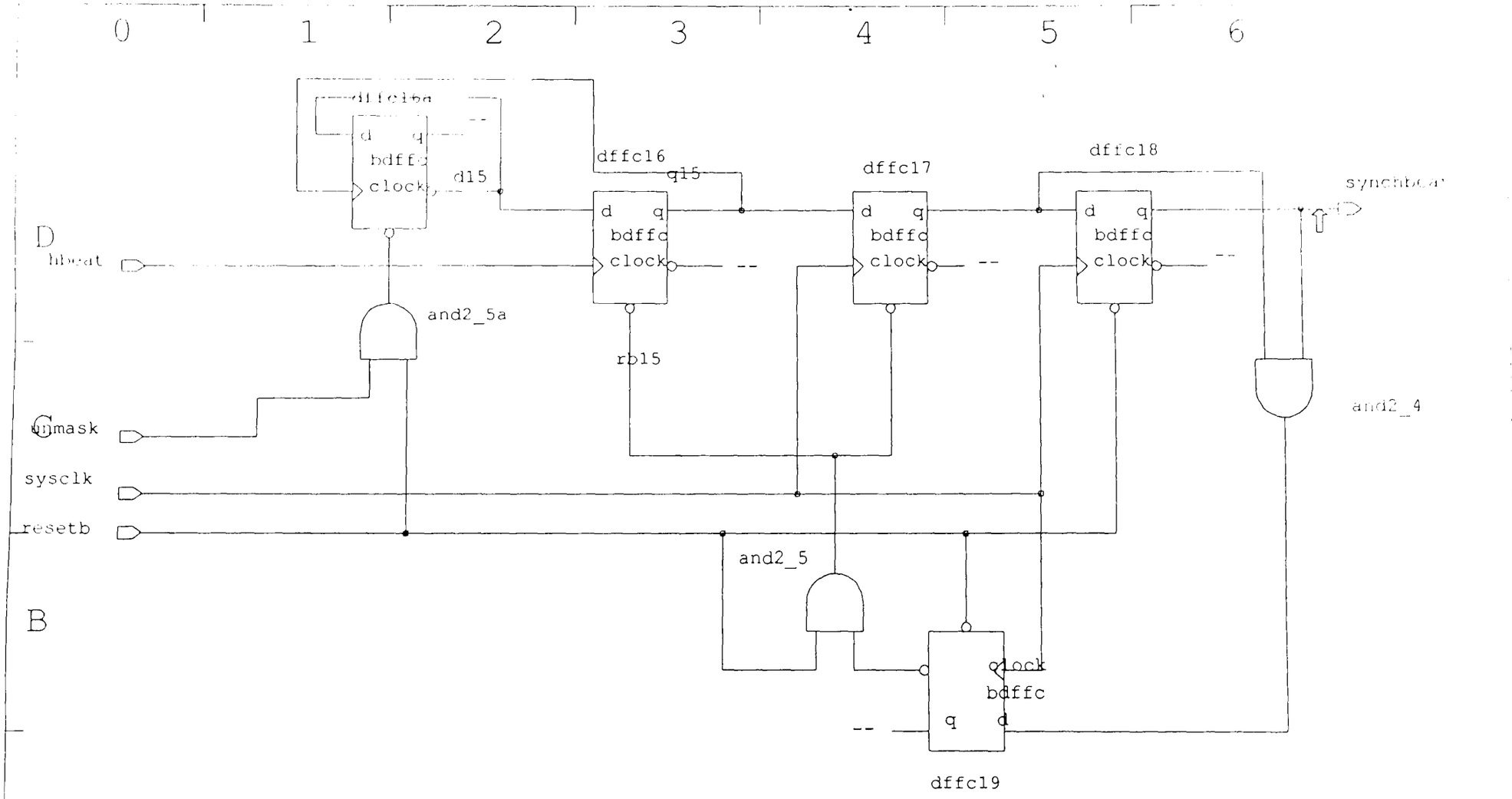

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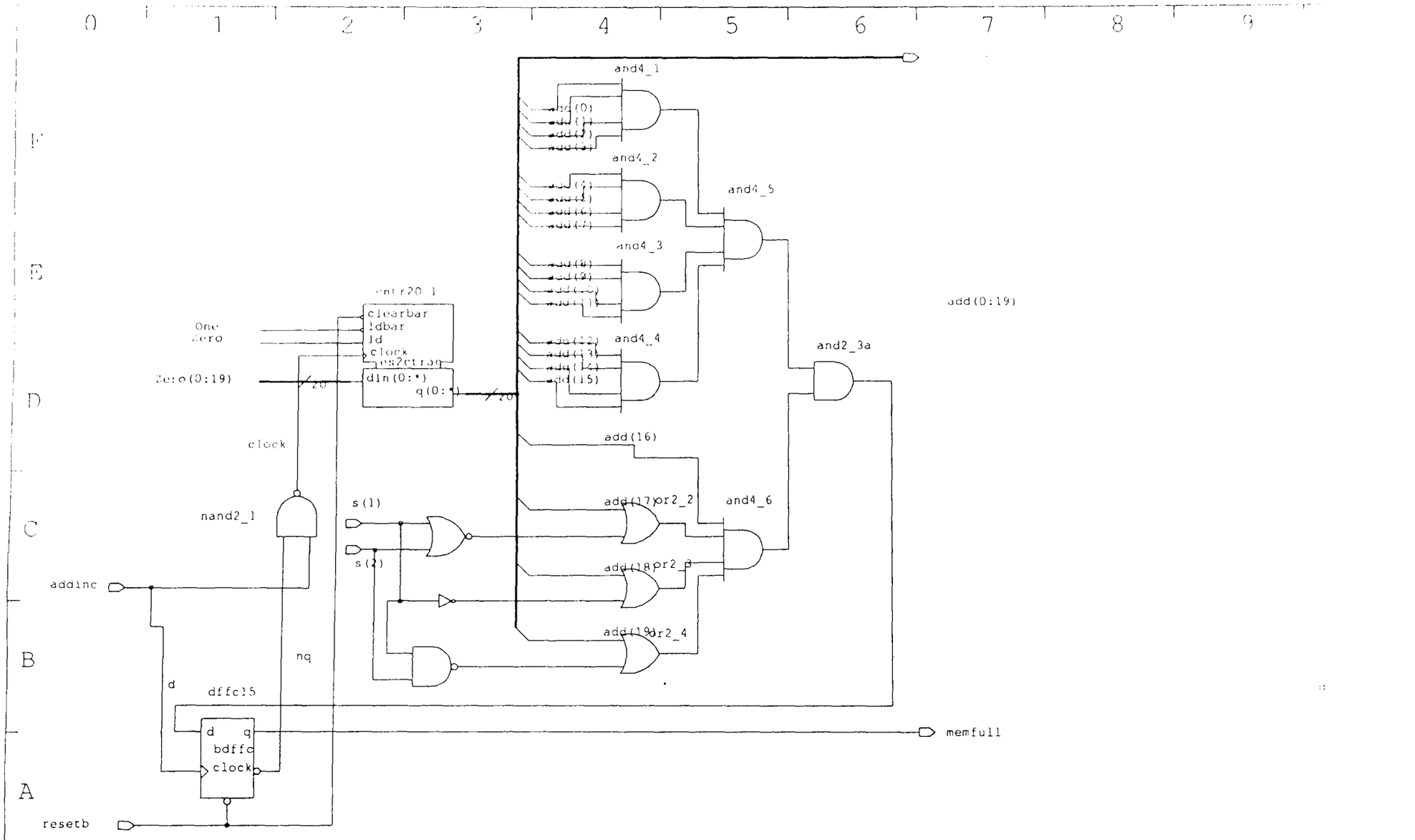

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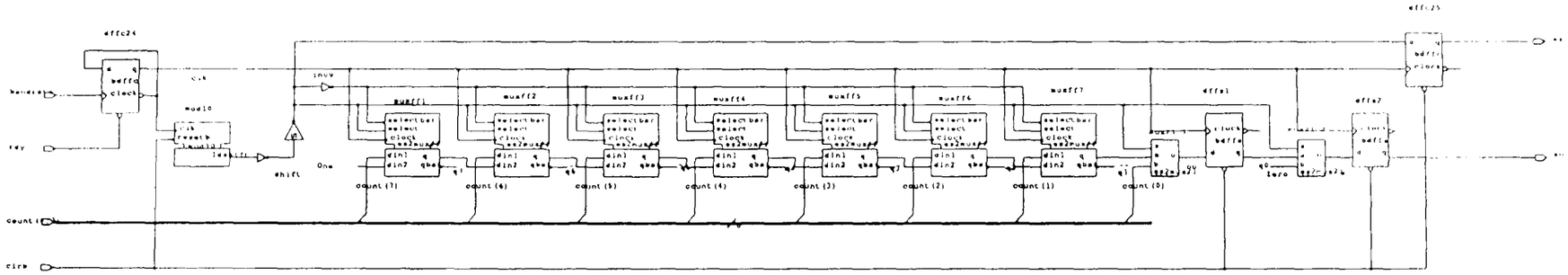

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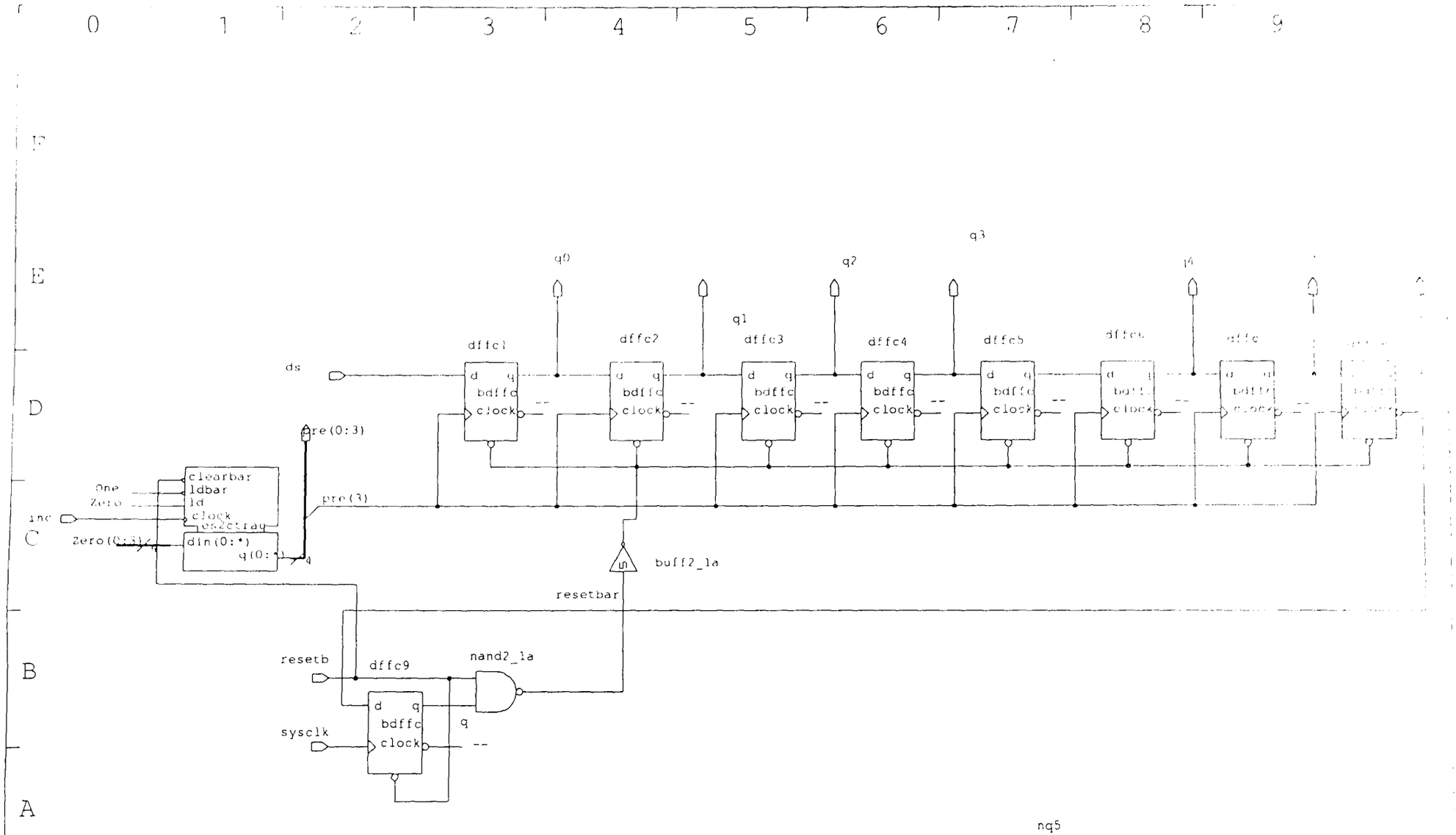

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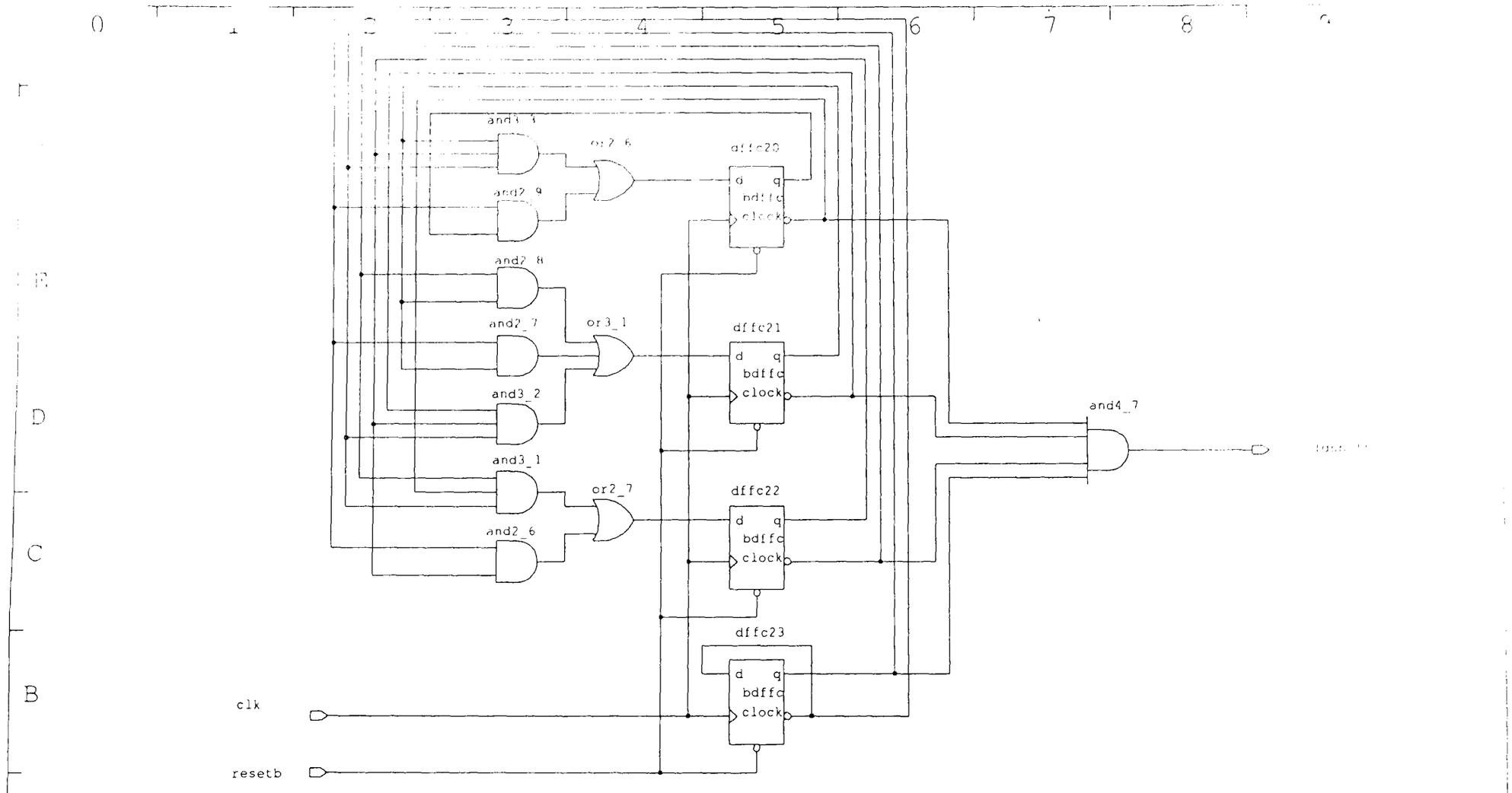

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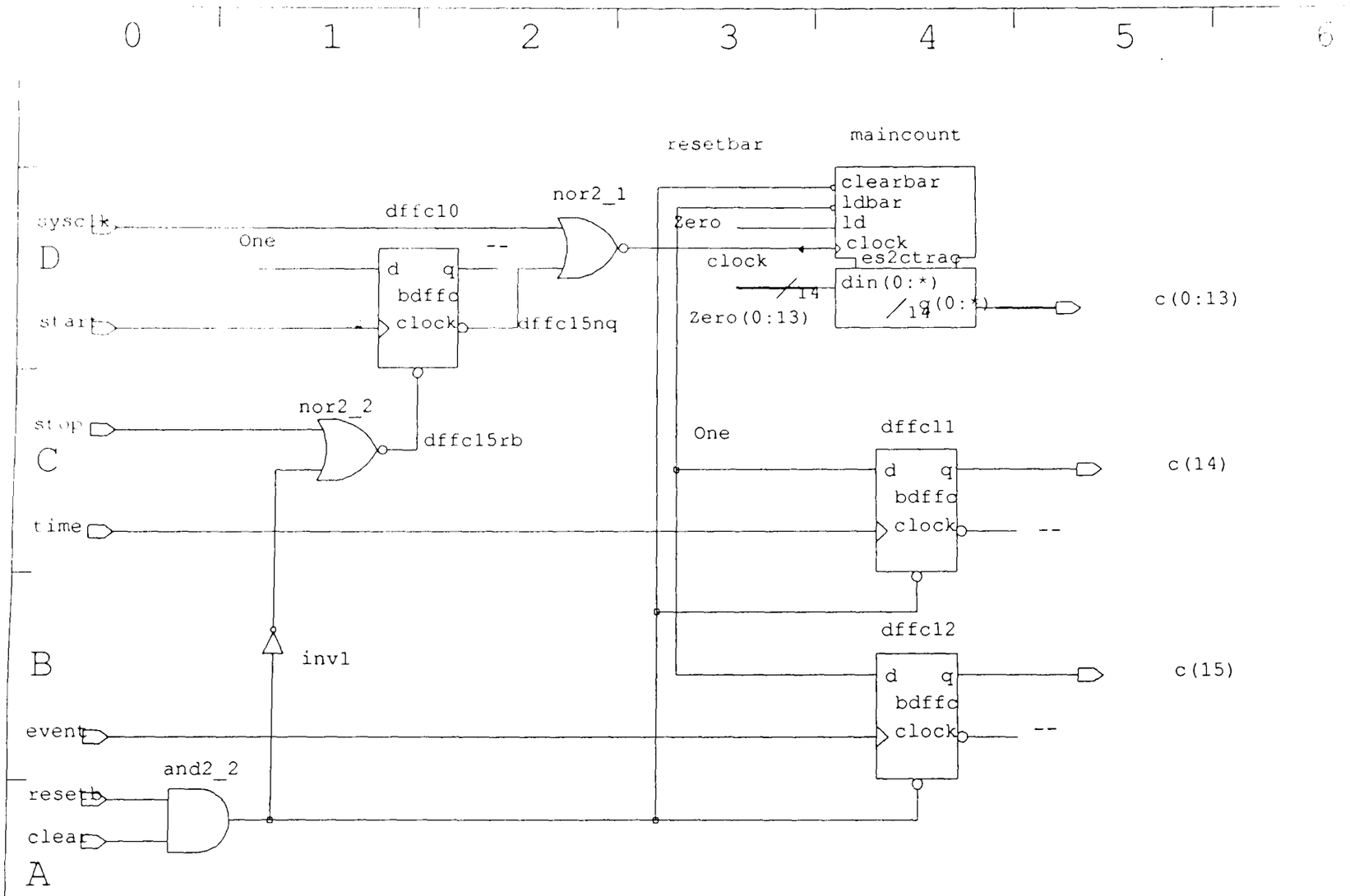

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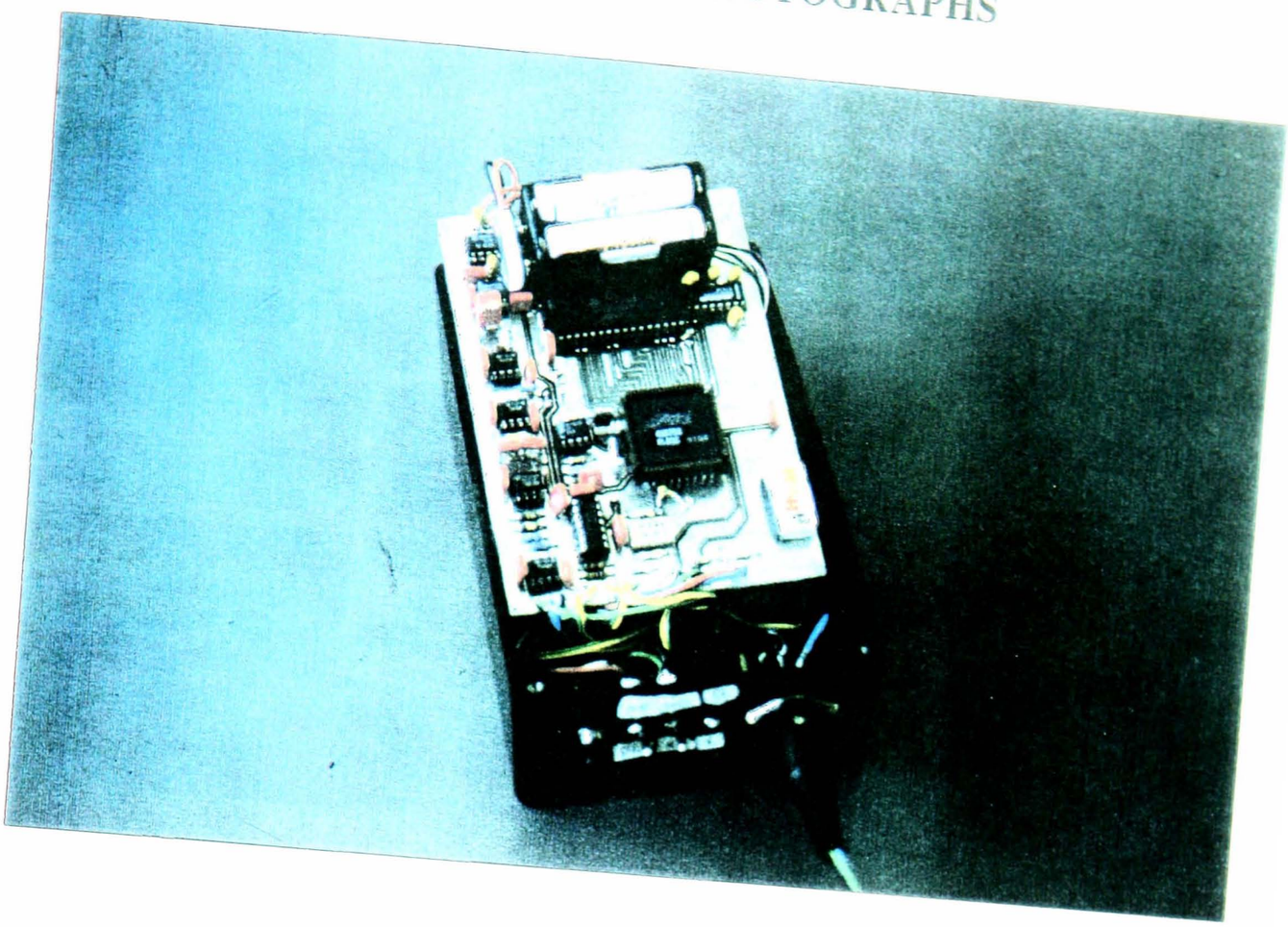
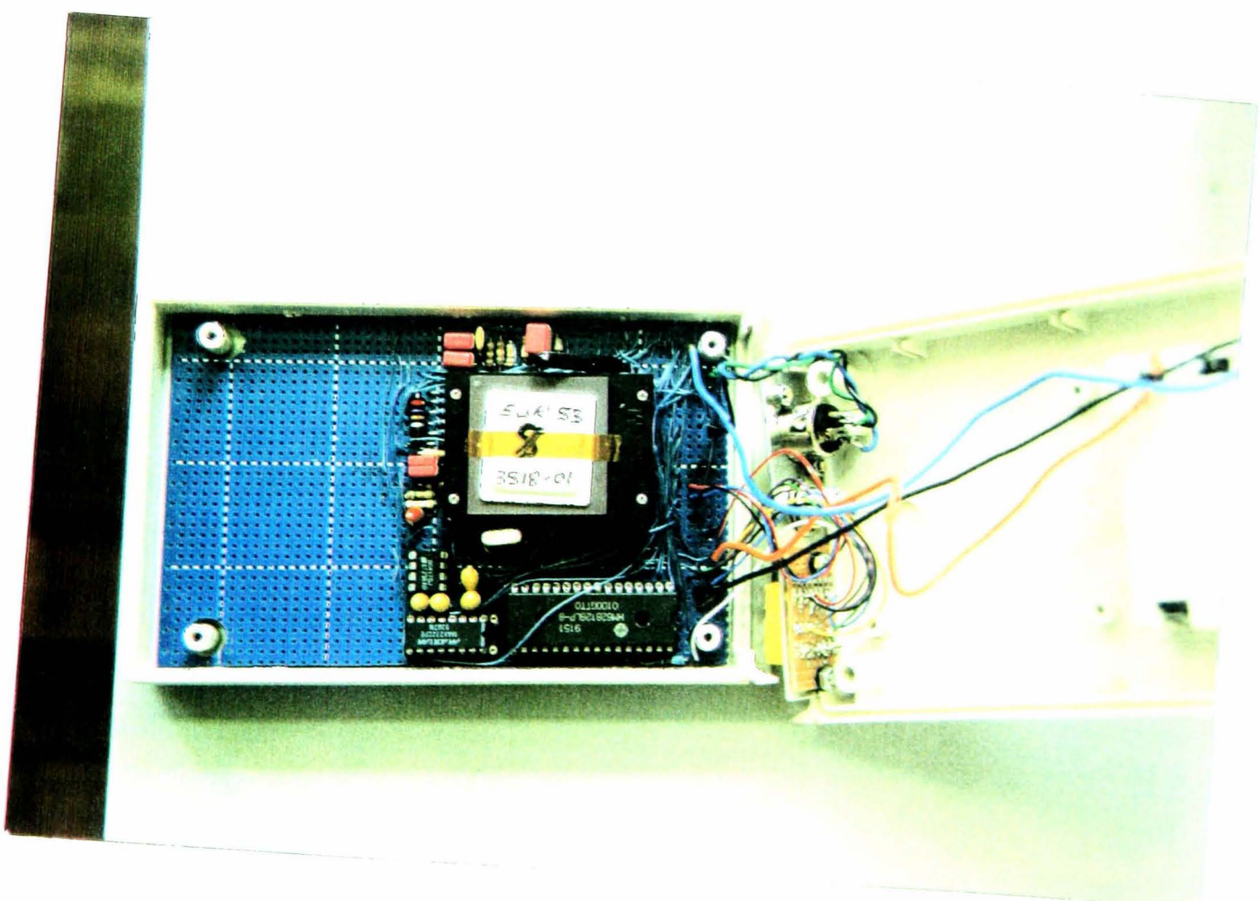
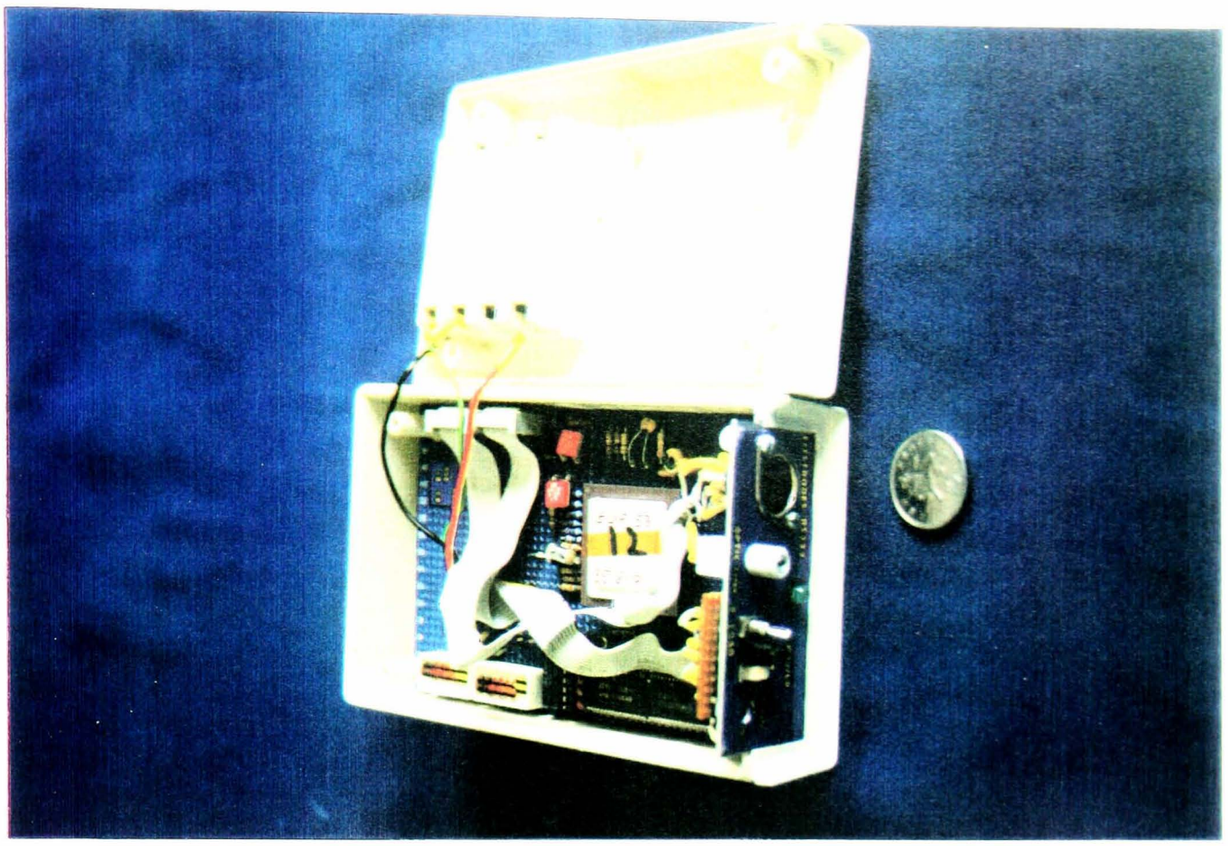
APPENDIX D: PHOTOGRAPHS



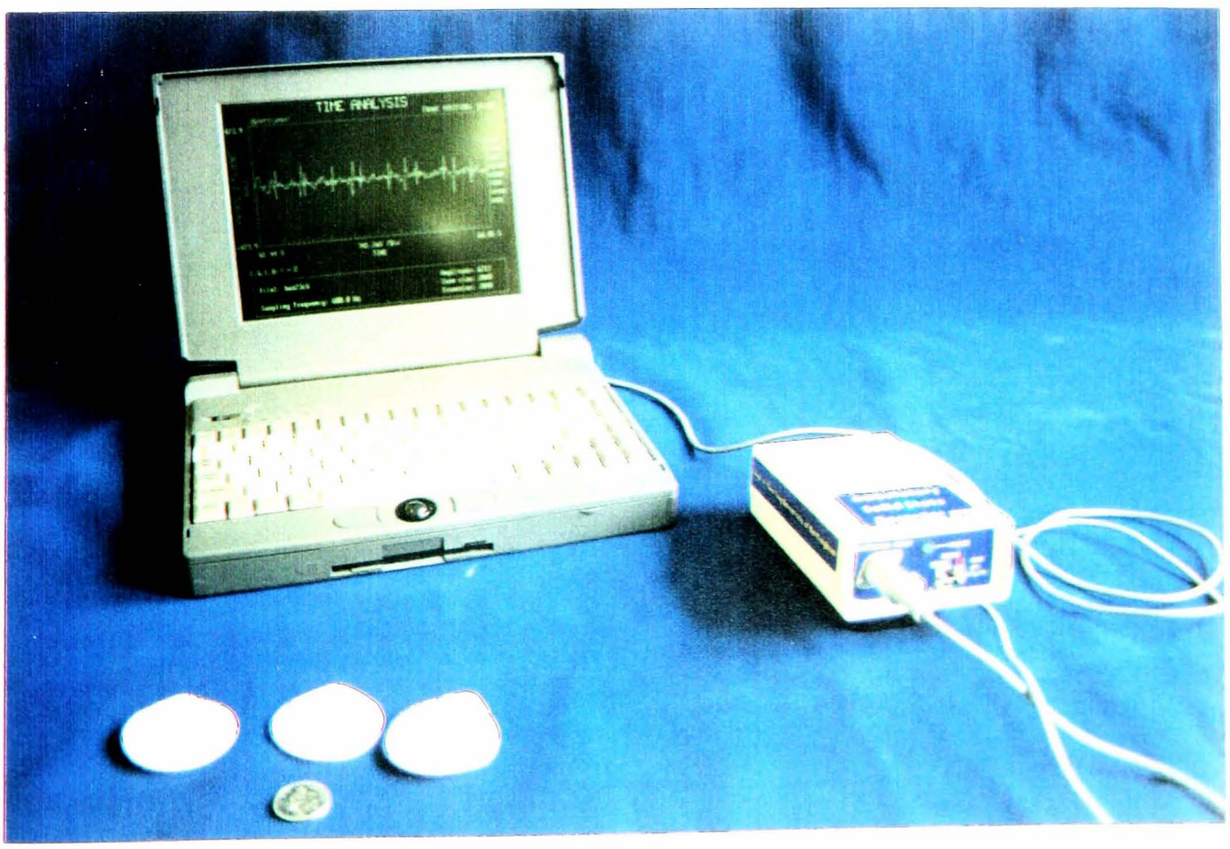
D.1. FPGA HR recorder



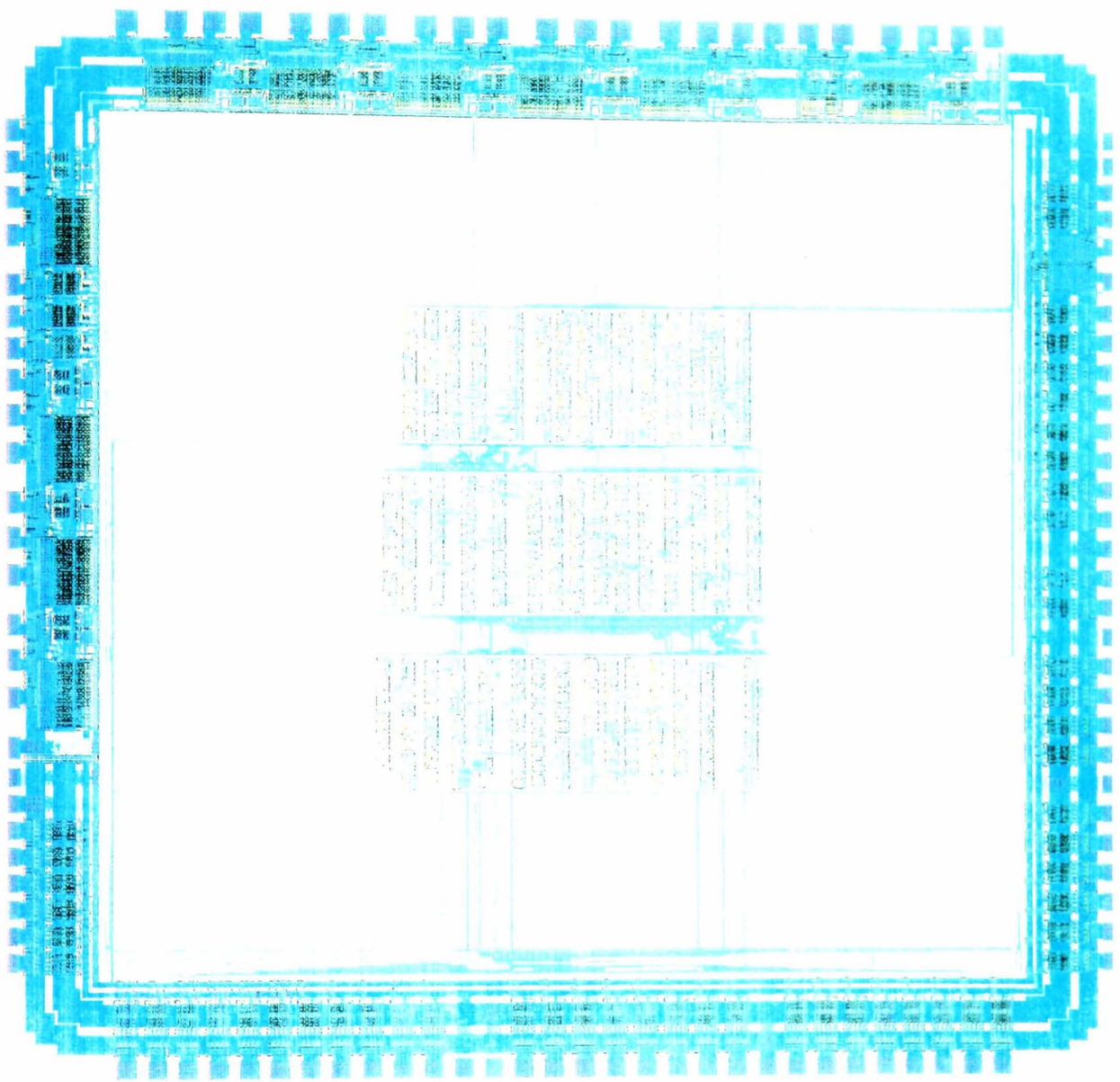
D.2. ES2 ASIC HR recorder



D.3. General electrophysiological signal recorder



D.4. Downloading data to the laptop PC



D.5. ES2 ASIC layout plot

APPENDIX E: MESU DOCUMENTATION

0602
515547
BRHG/SEH

9 June 1994

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Dear Mark

Thank you for spending the time to carry out a safety check on our "Ambulatory Solid State Recorder (Ver 2)". I have read your indemnity form and I am happy with the appropriate conditions of use. As you know, Andy Harrison will normally be carrying out the measurements. However, in the event of a member of staff from the QMC using the equipment the indemnity is signed subject to our operating instructions as detailed in document "mode2v2.doc" being followed.

Thanking you once again for your time.

Best regards

Dr B R Hayes-Gill

cc D Redshaw
Dr J A Crowe
A Harrison

Loan No 4672

NATIONAL HEALTH SERVICE

FORM OF INDEMNITY A
EQUIPMENT ON LOAN
FOR TRIAL OR TESTING

QUEEN'S MEDICAL CENTRE, NHS TRUST, NOTTINGHAM

AN AGREEMENT made the 6 day of JUNE 1994
BETWEEN QMC UNI NHS TRUST ("the Authority") and
CLIC ENG DEPT (MEDICAL ELECTRONICS) UNIVERSITY OF NOTTINGHAM ("the Supplier").

WHEREAS

(1) The Supplier is the owner of the equipment described in the Schedule ("the Equipment").

(2) The Supplier wishes the Authority to use the Equipment for the benefit of the Supplier for the purpose of evaluation, testing, research, design investigation or trial demonstration.

IT IS HEREBY AGREED that the Supplier shall lend and the Authority shall borrow and use free of charge the Equipment for the period specified in the Schedule in the premises specified in the Schedule ("the Premises") on the terms set out below.

1. The loan of the Equipment shall be deemed to be a contract for the hire of goods as defined by Section 6 of the Supply of Goods and Services Act 1982.

2. The Supplier shall be liable for and shall indemnify the Authority and the Secretary of State for Health against all liability in respect of personal injury to or the death of any person, loss of or damage to property and any loss or expense in consequence of or in any way arising out of the installation, presence, use or removal of the Equipment on or from the Premises provided that this indemnity shall not extend to liability resulting from the negligence of the Authority's own servants or agents.

3. 3.1 The Supplier shall insure against its liability under Condition 2 in the minimum sum of £2 million in respect of any one incident.

9.3 The Supplier will be responsible for the cost of reinstating the Premises including the services therein to the satisfaction of the Authority.

10. The Equipment shall remain continuously at the Supplier's risk during and after the period of loan.

SIGNED on behalf of the Authority _____

SIGNED on behalf of the Supplier _____

THE SCHEDULE

1. The Equipment AMBULATORY SOLID STATE RECORDER

Model/Mark No: VER 2

Serial No: VER 2

Value: £2,000

Description:

2. Period of Loan

2 years months commencing the 1ST day of JUNE 1994

3. The Premises

QMC PREGNANCY ASSESSMENT CENTRE WARD C30 AND C L S.

Ambulatory Solid State Recorder (Ver 2)
Documentation and Operating Instructions

Description of Equipment's Function

This battery operated solid state recorder is designed to digitise and record in SRAM any electrophysiological signal that can be detected from skin electrodes. After recording is complete the data can be downloaded to a PC via an RS232 connection to the serial port.

This recorder has been designed and built by Mr A. Harrison of the Department of Electrical and Electronic Engineering, University of Nottingham. as part of a PhD research project to design an ambulatory fetal heart rate recorder. Experimental recordings are required of raw fetal ECG signals obtained from cutaneous electrodes placed on the mothers abdomen. As well as recording fetal ECG signals it is intended that the ambulatory solid state recorder will be used to investigate the feasibility of recording maternal uterine contractions also obtained from cutaneous electrodes placed on the mothers abdomen. This work is being carried out in collaboration with the Department of Obstetrics and Gynaecology which is based at both the QMC and the City Hospital, Nottingham. The Department of Obstetrics & Gynaecology have kindly arranged to provide pregnant women on which the recorder can be used to obtain the necessary data.

Operating Instructions

To start recording:

- Connect electrode lead to 3 skin electrodes
  2 Red differential inputs (EL1 & EL2)
  1 Black reference lead (EL3)
- Switch "power" switch to "on"
- Set left hand switch to "store"
- Press the "reset" button
- Data recording will now start
- Begin timing the recording

To stop recording: (Before maximum record time is reached)

- Set left hand switch to "d/load" (download)
- Press the "reset" button
- Return recorder to Engineer for downloading data

After recording is completed:

- Following steps to be undertaken by the Engineer
- Replace electrode lead with RS-232 lead
- Connect other end of RS-232 lead to COM1 of PC
- Press the "reset" button
- Run download software from PC

Safety Requirements (BS 5724)

If equipment that is powered by an internal power supply is to comply with BS 5724 section 3 (protection against electric shock hazards) it must meet with the requirements laid down in clause 19 concerning leakage currents and patient auxiliary currents. For equipment of type B under normal conditions the patient leakage current must not exceed 100μA and the patient auxiliary current must not exceed 10μA (d.c.). Under single fault conditions the maximum allowable patient leakage current is limited to 500μA and the maximum patient auxiliary current is limited to 50μA (d.c.). The values of maximum a.c. current do not appear to apply as the equipment is powered by a 5V d.c voltage (4 AA cells).

The patient auxiliary current under normal conditions is determined by measuring the current between any single patient connection and all other patient connections connected together. The patient auxiliary current of the ambulatory solid state recorder when measured with a digital multimeter was 0 Amps (on 200μA range).

Under single fault conditions the maximum allowable patient auxiliary dc current is limited to 50μA. In order to meet this requirement it is important to have as large a resistance as possible between the patient leads and the parts of the equipment circuitry likeliest to experience a single fault condition.

Firstly, the 2 red differential patient leads are connected to pins J12 and K12 on the ASIC. Both these pins are non inverting inputs to CMOS op-amps internal to the ASIC (see attached circuit diagram). The black reference patient lead is connected to the equipment common and therefore to several pins on the ASIC (N12,N8,F12,D12,E13&L10). As the CMOS op-amps have a very large input impedance of the order of 10GΩs, it follows that the 3 patient leads must be isolated from each other by a resistance of similar magnitude. The lead isolation has been verified with a digital multimeter being connected between all combination of patient leads. In every case the resistance exceeded 20MΩ (maximum value of multimeter). Secondly, it may be possible for a single fault of 2.5 Volts (dc) to appear between either electrodes 1 or 2 and the reference electrode (EL3). The issue is the prevention of tissue necrosis for 'long term monitoring'. However, the system will be used for less than 1 hour in any one session and hence it is felt that this is not classed as 'long term monitoring'.

The patient leakage current of type B equipment is determined by measuring the current between all the patient connections connected together and any part of the enclosure of the equipment. The patient leakage current of the ambulatory solid state recorder when measured with a digital multimeter was 0 Amps (on 200μA range).

Under single fault condition the maximum patient leakage current is limited to 500μA. In order to meet this requirement it is important to have as large a resistance as possible between the conductive parts of the equipment enclosure and the parts of the equipment circuitry likeliest to experience a single fault condition.

The only part of the enclosure which is conductive is the front panel. In order to eliminate patient leakage current it is important to isolate the front panel and any nuts

and bolts coming into contact with the panel from any of the equipment circuitry as well as the patient leads. The front panel isolation has been verified with a digital multimeter connected between all the patient leads connected together and the front panel (including all of the protruding switches and sockets). The front panel isolation from the equipment circuitry has been verified by measuring the resistance between the front panel (including all of the protruding switches and sockets) and every pin of the two ribbon cable connectors connecting the main circuit board to the front panel. In every case the resistance exceeded 20MΩ (maximum value of multimeter).

Component list

Capacitors :

C1, C2, C3, C4 : 1μF
C5, C6, C7 : 220nF
C8 : 10μF
C9 : 470pF
C10, C11 : 22μF (decoupling capacitors)
C12-17 : 10μF (decoupling capacitors underneath IC1, not shown on cct diag

Resistors :

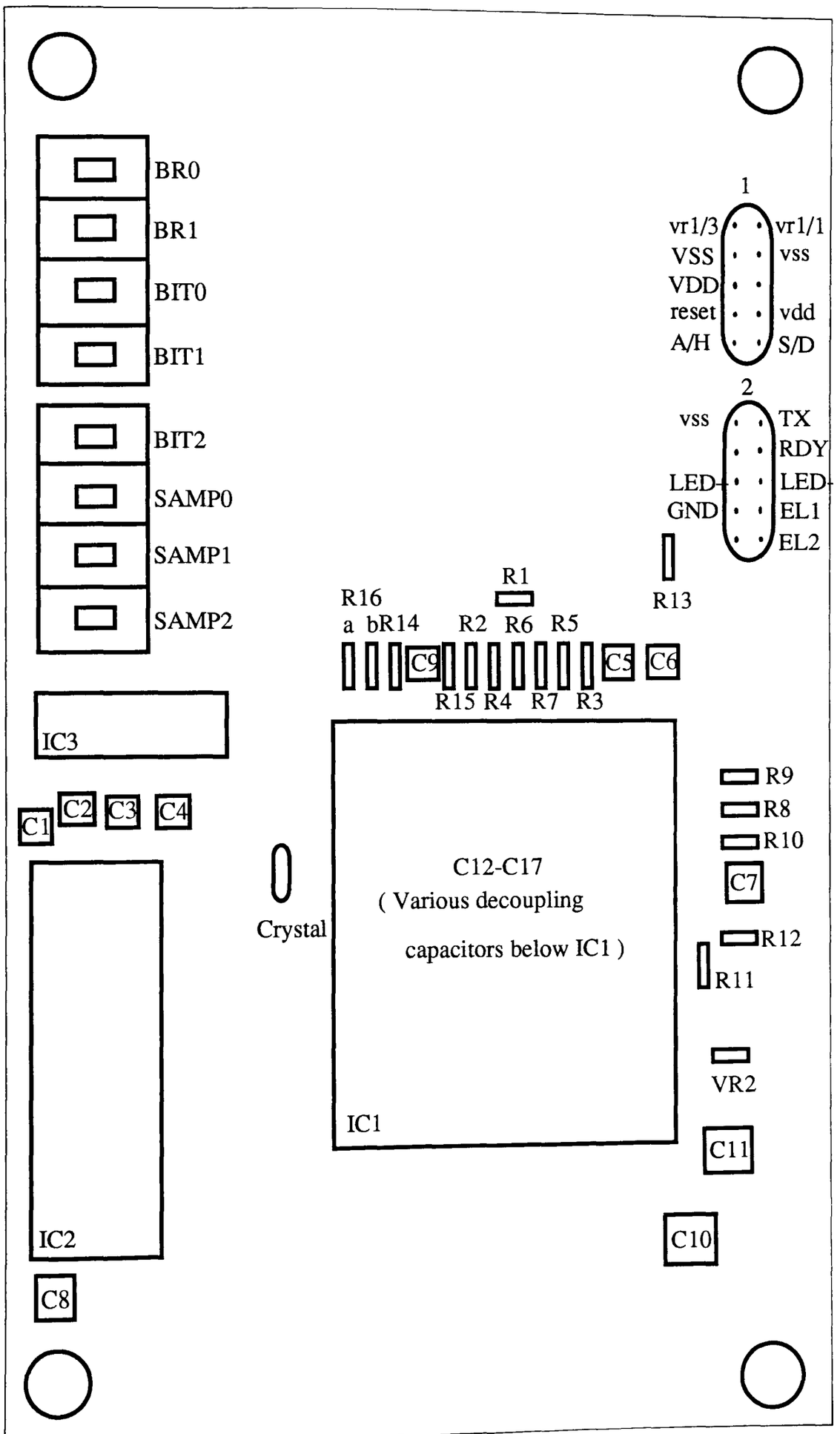
R1 : 750Ω
R2-7 : 20KΩ
R8, R9 : 510KΩ
R10 : 100KΩ
R11 : 33KΩ
R12 : 330KΩ
R13 : 62KΩ
R14, R15 : 620KΩ
R16 : 1.2MΩ (2 x 620KΩ)
R17 : 1.6KΩ (on front panel board)

VR1 : 470KΩ
VR2 : 50KΩ

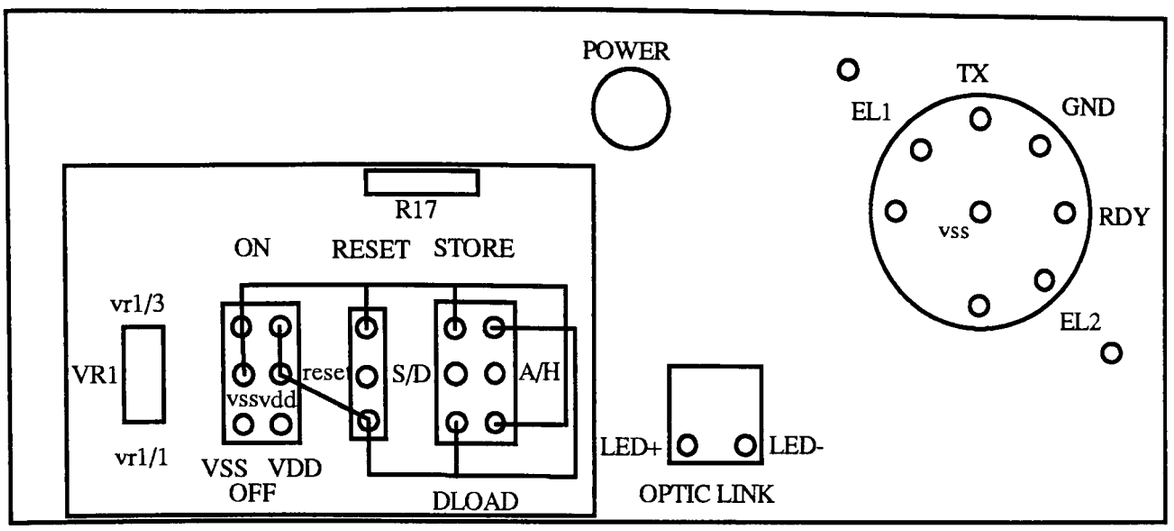
ICs :

IC1 : ES2 ASIC
IC2 : SRAM, DPS 512 S8 PL - 70C
IC3 : MAX 232 (RS-232 interface)

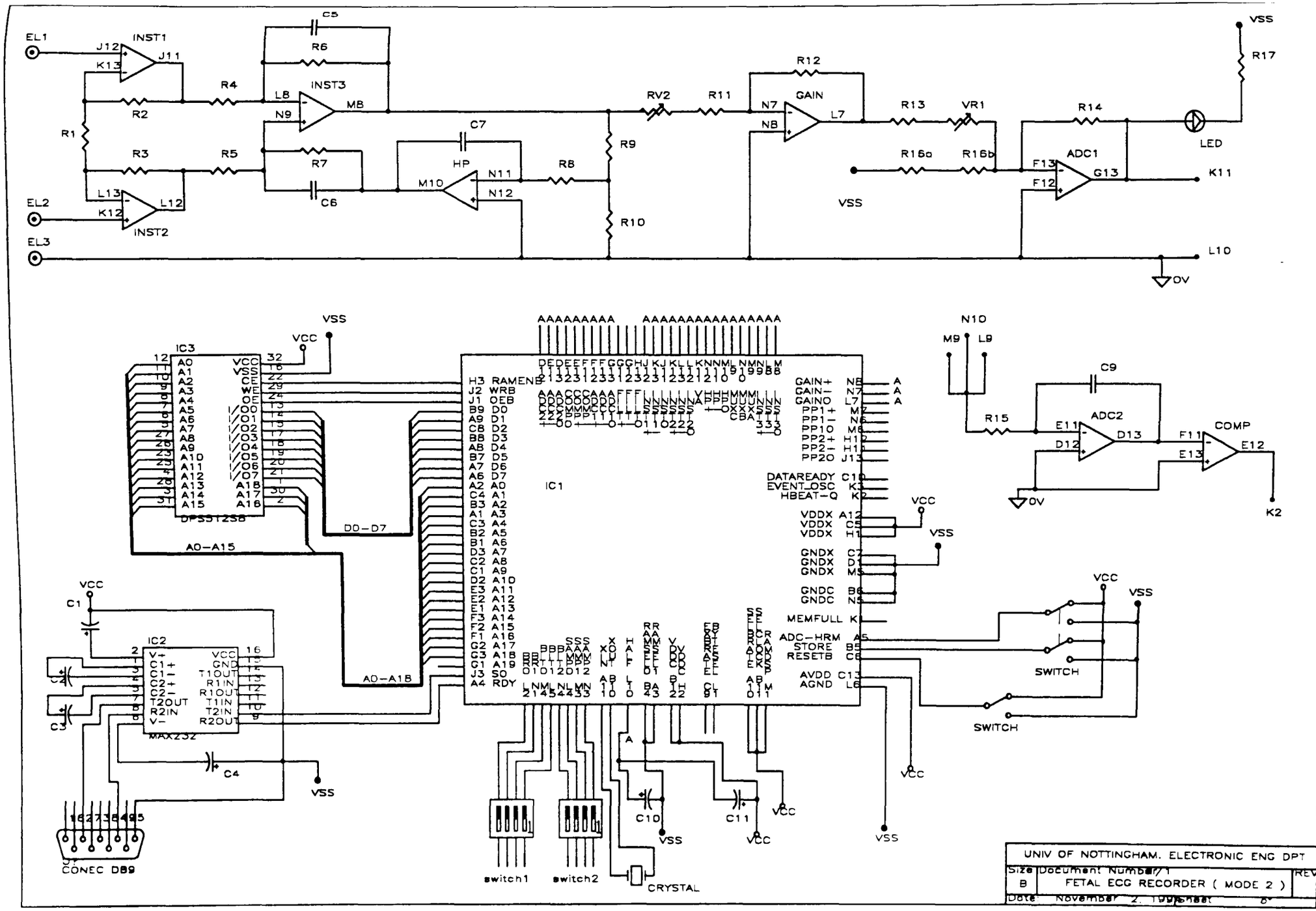
Crystal : 19.6608 MHz



Board map of ambulatory solid state recorder



Back view of the front panel



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B	FETAL ECG RECORDER (MODE 2)	
Date	November 2. 1990 Sheet	8

APPENDIX F

F. Frequency and phase response of instrumentation amplifier with filtering

The graph below shows a typical example of the frequency and phase response of an instrumentation amplifier with filtering (see figures 5.1 and 6.3). In this case the bandwidth is set at 0.2 to 38 Hz as is used in several FECG recordings. In the ES2 ASIC based adult heart rate recorder (see Chapter 5), the instrumentation amplifier with filtering is cascaded with a Butterworth band pass filter to give an overall bandwidth of 10 to 40 Hz.