A Current Source Inverter with Series AC Capacitors for Transformerless Grid-Tied Photovoltaic Applications

Chonlatee Photong, MSc

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Abstract

The Current Source Inverter (CSI) is one of the simplest power converter topologies that can convert DC to AC and feed power generated from photovoltaic (PV) cells into the AC grid with a single power conversion stage over the whole PV voltage range. The CSI also provides smooth DC current which is one of the requirements of the PV cells as well as preventing reverse current using unidirectional switches. However, the CSI operates with low efficiency at lower PV voltages, which is where the PV cells produce maximum output power. This low efficiency is caused by large differences in voltage levels between the PV side and the grid side across the converter.

This thesis presents an alternative topology to the three-phase CSI by connecting an AC capacitor in series with each AC phase line of the CSI circuit. The presence of the series AC capacitors in the CSI topology allows the AC voltage levels to be adjusted to match the voltage levels of the PV cells. Therefore, the CSI with series AC capacitors is able to operate with optimal DC-AC voltage levels.

Performance of the proposed topology is evaluated in comparison to the standard CSI and five other converter topologies based on transformerless circuit concepts selected from those already available in the market and suitable converters discussed in the literature. All converter topologies were modeled and simulated with the SABER simulation software package. The CSI with series AC capacitors prototype was constructed in order to validate the feasibility of the proposed topology and the performance of the proposed topology in comparison to the standard CSI. Simulation results show that the CSI with series AC capacitors provides improved efficiency and better input/output power quality in comparison to the standard CSI. The proposed topology also achieves the lowest output line current distortion, lowest voltage stress across the circuit components and lowest estimated cost of power semiconductors when compared to all considered topologies. Experimental results are also presented to validate the simulation results.

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1. C. Klumpner, C. Photong, and P. Wheeler, "A more efficient current source inverter with series connected ac capacitors for photovoltaic and fuel cell applications," in *PCIM Europe Conference*, 2009.

2. C. Photong, C. Klumpner, and P. Wheeler, "A current source inverter with series connected AC capacitors for photovoltaic application with grid fault ride through capability," in *Industrial Electronics, 2009. IECON '09. 35th Annual Conference of IEEE*, 2009, pp. 390-396.

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Chapter 1

Introduction

The rapid depletion of fossil based energy resources such as coal, natural gas and oil together with an effort to reduce CO_2 emission into the atmosphere has required a demand for a larger share of clean energy to be produced from renewable energy sources. The sun is the primary energy source that subsequently creates substantial diversity of renewable energy sources on the Earth, e.g. the energy from the sun (or *solar energy*) that is captured by the Earth's atmosphere creates the wind energy; when absorbed by oceans creates warm ocean currents and indirectly when absorbed through photosynthesis creates bioenergy; or when causing water evaporation that produces rainfall, creates hydroenergy [1]. However, solar energy that can be collected directly on the Earth's surface still accounts for the largest amount of renewable energy compared to all other renewable sources, i.e. 3,850,000 EJ/year compared to 7,400 EJ/year for ocean energy, 6,000 EJ/year for wind energy, 1,548 EJ/year for bioenergy and 147 EJ/year for hydroenergy [2]; where 1 EJ = 1×10^{18} joules. The current annual world energy demand (517 EJ/year) could be covered with only 0.02% of the direct solar flux of energy [3]. Therefore, using solar energy could be sufficient for securing the future energy requirements.

In addition, direct solar energy can be converted directly to electricity (the most convenient energy form to be used [4]) using devices called *Photovoltaic* (PV) cells, whilst producing electricity from wind, ocean and hydro energies must create mechanical motion first and then electricity or from bioenergy must burn biomass to create heat first, then mechanical motion and then electricity [5]. This leads to a simpler system for solar-PV electricity production. Producing electricity directly from

sunlight using PV cells also provides several advantages [6],[7], as shown by the following list:

- PV cells emit absolutely no pollution during the process of energy conversion.

- PV cells have no moving parts and thus require very little maintenance (cost) compared to turbine engines used for wind, ocean, hydro and biomass. The cells also have a long lifetime with typically 20-25 years guarantee.

- PV cells can be used anywhere where there is sunlight including remote areas such as deserts, oceans and even in space where the grid utility is not available, or the cost of installation becomes prohibitive.

- PV cells can also be easily installed or removed, allowed the solar-PV power plant to be resized after the first installation.

Unfortunately, there is only 0.000008% (0.31EJ/year) of solar energy currently installed and utilised to produce electricity [3]. The major problem that limits the utilisation of solar energy for electricity production is related to the high installation cost per unit energy ($/kWh). Solar-PV electricity has one of the highest prices compared to other energy source as shown in Figure 1.1 [8]. The capital cost of solar-PV electricity results from the cost of the PV cells as integrated into sealed panels, the cost of a large installation area for higher energy production and the cost of energy storage devices (for instance, in battery) or an auxiliary source used to recover the required output energy (e.g. during the night-hours) [5],[9]. Therefore, in order to promote the utilisation of solar-PV electricity, additional research efforts should be made to enable the reduction of its associated cost per unit energy ($/kWh). This can be achieved by reducing the related costs and/or improving solar conversion efficiency in terms of raising the kWh of electric energy generated throughout the PV power plant.

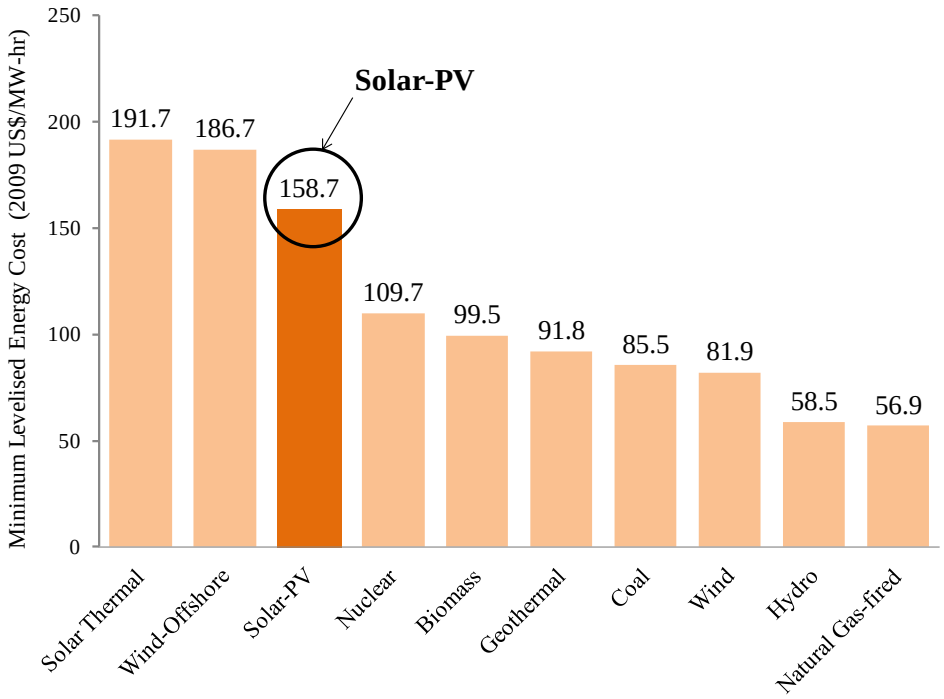


Figure 1.1 Minimum cost of electricity production for different power plant types [8]

There are two basic types of solar-PV systems: stand-alone (or off-grid) system and grid-tied (or grid-connected) system [10]. The stand-alone PV system is the obvious solution for the loads that are located in remote areas, far from any power grid infrastructure. However, a support battery and/or a backup energy source have to be included in the stand-alone PV system in order to supplement the load requirements during the absence of sunlight, whilst the grid-tied PV system can use the energy supplied from the grid instead, reducing overall system cost. In addition, oversized power conversion equipment mainly in terms of current/power ratings is essentially to be used for stand-alone PV systems to guarantee that the system can deliver the peak load power. These additional battery/source and the use of over rating the converter equipment add to the cost for electricity produced from the stand-alone PV system [11]. Therefore, when considering the economic aspects, a grid-tied PV system would be more attractive than a stand-alone PV system.

However, PV cells produce electric DC voltage/current/power, which cannot be connected directly to the AC grid. Therefore, in order to facilitate this connection, a power converter that converts DC power delivered at variable voltage and current to

AC power, known as *grid-tied PV inverter*, is needed. The grid-tied PV inverter affects the production cost of solar-PV electricity in that a low efficiency inverter can lead to low output power (W) production, which then causes a higher cost per unit power ($/W) for solar-PV electricity. Therefore, a grid-tied PV inverter is required to have high efficiency, which is the capability to extract the full amount of available power from the PV cells and transmit that power into the grid with the lowest losses. Converting this into practical terms, besides being able to operate at maximum (open-circuit) voltage of the PV cells for proper connection compatibility, the grid-tied PV inverter is also required to operate efficiently in the low PV voltage region (typically 0.6-0.9 of open-circuit voltage) where the PV cells can produce their maximum output power.

Besides the ability of full PV power extraction, the preferable grid-tied PV inverter is also required to comply with all relevant grid codes and regulations [12-16], which are the requirements to produce good quality of output waveforms with low levels of harmonic emissions, have the capability to ride-through grid faults (i.e. grid voltage or frequency deviations), to preserve or enhance power network stability and provide safe operation by disconnecting /not supplying power to the grid when the connection with the main grid is lost by accident or for maintenance purposes, known as anti-islanding.

There are three alternative technologies currently available for grid-tied PV inverters using either a traditional low frequency (LF) step-up transformer, a high frequency (HF) transformer or without transformer (*transformerless*) [17]. Each technology has its own merits or features:

- The grid-tied PV inverter with a LF step-up transformer is the simplest technology. This inverter type consists of a traditional DC-to-AC converter and a LF transformer. The DC-to-AC converter converts DC power from the PV cells to AC power at the grid frequency. The LF transformer steps up the voltage to the grid voltage level. The use of a step-up transformer in the inverter circuit provides the benefit of electrical isolation between the inverter and the grid, which helps to prevent any potential safety hazards that may be

caused by the common connection between the PV and the grid [18]. In addition, due to the use of simple components, this inverter type can use the simplest control. However, the inherently large size and weight of the LF transformer results in this inverter being the bulkiest and heaviest topology [19].

- The grid-tied PV inverter with a HF transformer is also an inverter type that provides galvanic isolation, but being much smaller and lighter compared to the inverter with the LF transformer [20],[21]. However, there are several conversion stages involved:
    - First the DC/AC inverter converts DC power from the PV cells into AC power at high frequency.
    - Then the HF transformer steps up the voltage to the sufficient level.
    - Then the AC/DC rectifier converts AC power back to DC power.
    - Finally, the DC/AC inverter converts again the DC power to AC power with the voltage and frequency suitable for the grid.

  Since multiple power conversion stages are used, this inverter type has a more complicated configuration with higher cost and power losses [22], [23].

- The transformerless inverter does not require any transformers; thus, this inverter type is the smallest and lightest among the three technologies. Moreover, due to the possibility of single-stage power conversion, this inverter type can achieve the highest efficiency recorded (up to 98%) [24]. However, as this inverter type does not provide galvanic isolation, an additional fault monitoring circuits/systems have to be included in order to meet the requirements of the grid codes and safety regulations. These additional circuits/systems add more complexity to this inverter type.

Therefore, when considered in terms of efficiency, the grid-tied PV inverter made from transformerless technology seems to be the most suitable solution, which could be used to reduce solar-PV electricity cost.

Depending on the grid connection, transformerless grid-tied PV inverters can be single-phase or three-phase configurations [21], [25-27]. Single-phase inverters usually used in lower PV power generation (typically up to $5kW_p$) compared to three-phase inverters (e.g. up to $10\text{-}15kW_p$ for rooftop applications) [28]. The utilization of power switches in three phase converters is better and also the installed cost per unit power for solar-PV electricity ($/W) decreases when the installed power of the solar-PV system increases (as shown in Figure 1.2) [29]; thus, three-phase grid-tied PV inverters could become more cost effective compared to the single-phase inverters, justifying therefore the choice for three phase systems as a worthwhile topic of research.

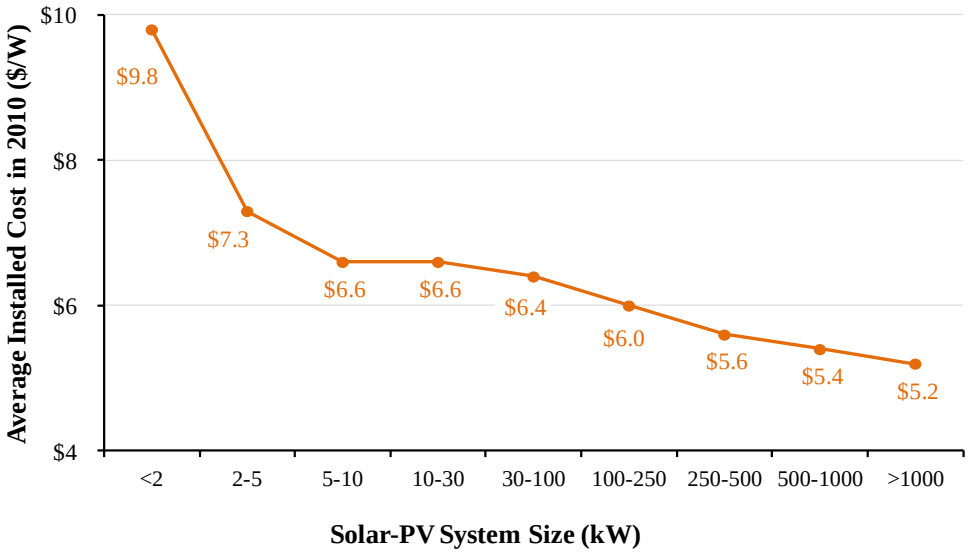


Figure 1.2 Average installed cost for different solar-PV system size (kW) [29]

Voltage Source Inverters (VSI) and Current Source Inverters (CSI) are the two basic topologies used in the three-phase transformerless PV inverters as discussed in the literature. These topologies have a minimum number of semiconductors used (6 switching devices and 6 diodes) and potentially high conversion efficiency due to the single-stage power conversion approach. However, the VSI topology has some problems when operating with a large voltage variation of the DC-link source (between zero and no-load voltage) which is characteristic for PV cells. Since the VSI topology is a DC-to-AC voltage step-down converter, the VSI topology cannot

operate properly and extract the PV power when the DC (PV) voltage is lower than the peak grid voltage. In order to fulfil this requirement, a PV string with a high enough voltage rating has to be used (with a typical value of the no-load PV voltage string of 1.2-1.3 of the peak grid voltage), e.g. for the three-phase 415V power grid, a PV cell string with the voltage greater than 586V and no-load voltage greater than 703-762V must be used. The high PV string voltage results in the need of higher voltage ratings for the components used in the VSI circuit (and hence higher cost) as well as causing higher internal resistance (and hence higher losses) within the PV string since several individual PV cells have to be connected in series to produce sufficient PV voltage [30]. A DC-to-DC voltage boost converter could be used to step up a low PV string voltage to a sufficient level for the VSI topology to operate properly and for the designer to achieve minimum installed power in the switches for a given level of processing power and hence using a high enough PV string voltage rating is no longer required. In fact, the two-stage VSI with a boost converter is currently the most popular converter type used in several industrial PV products [31]. However, using the boost converter in the VSI's circuit can lead to a more complex circuit configuration and control as well as adding higher cost and higher losses to this inverter type.

Unlike the VSI topology, the CSI topology is a DC-to-AC voltage step-up converter. The CSI topology can operate and extract the power from the PV cells in a whole PV voltage range as long as the PV voltage does not exceed 0.866 (or $\sqrt{3}/2$) of the peak grid voltage (e.g. PV voltages lower than 508V are required for the 415V three-phase power grid). As a result, the CSI topology is more preferable than the VSI topology in terms of the PV-inverter voltage matching between the PV source and the inverter as well as in terms of low voltage rating of the circuit devices. In addition, since the PV cells create electric current through the active p-n junctions which are characterised as a current source connected with a large-scale shunt diode [32], a smooth DC-link current drawn from the PV cells therefore is required. This results in the need of an additional inductive filter at the DC side of the inverter and leads the CSI topology to be the ideal choice. Moreover, advance switching devices such as reverse voltage blocking (or RB-) IGBTs [33] which have configuration equivalent to the switches used in the CSI circuit (an IGBT connecting in series with a diode) could be used to reduce the semiconductors used and losses as well as to simplify the circuit for the

CSI topology [34]. Additionally, as the CSI topology operates with unidirectional DC current unlike the VSI topology, a diode used to prevent a reverse current for the PV source is not required for the CSI topology. A DC-to-DC voltage buck converter could be used to step down an excessively high PV string voltage and hence enable the use of a higher PV voltage rating than imposed by the limit of the CSI operating range. However, adding the buck converter into the CSI topology can lead to more complexity for the circuit configuration and control as well as higher cost and higher losses.

Alternatively, three-phase transformerless, grid-tied PV inverters could be constructed using Impedance Source Inverters (also called Z-Source Inverters or ZSIs) [35]. The ZSI topologies are inverter types that have the capability of both DC-to-AC step-down and step-up operation due to the use of a more complex DC-link network (LC components and a diode). These inverter types have two main configurations: the voltage fed ZSI topology which is the modified topology of the VSI topology and the current fed ZSI which is the modified topology of the CSI topology. By using specific modulation patterns that use shoot-through states, the voltage fed ZSI can step up low PV voltages and embed similar functionality to a boost converter. On the other hand, by using specific modulation patterns that use open-circuit states, the current fed ZSI can step down high PV voltage and embed similar functionality to a buck converter. Although these additional complex DC-link networks and special modulation patterns provide added features suitable to be used for grid-tied PV applications compared to the VSI topology and the CSI topology, these inverter types have high voltage and current stress on the circuit components [36], [37], as well as causing a more complex circuit and control, higher cost and higher losses.

Several advantages of the CSI topology raise the possibility to be used for grid-tied PV applications in order to achieve high PV power production with an ability of operation over the whole PV voltage range and single-stage power conversion, as well as making use of the minimum number of semiconductors, simple power circuit by using RB-IGBTs and better DC-link current smoothing suited for interfacing to the PV cells. However, during the PV voltage range where the PV cells produce the maximum output power (i.e. 0.6-0.9 of the no load voltage), the CSI topology operates with lower efficiency. This is because of the fact that when the PV voltage at

the DC side reduces whilst the AC grid voltage is constant, the voltage difference between the DC side and AC side of the inverter will be increased; especially at very low PV voltage levels. This voltage difference requires the output AC current to be reduced, in order to equalise the power between the DC side and AC side of the inverter. The reduced AC current leads to a low DC-to-AC current transfer ratio (modulation depth), which then degrades the power conversion efficiency for the CSI topology.

This thesis proposes an alternative topology to the three-phase CSI topology, by connecting an AC capacitor in series with each of the AC phase line of the standard CSI topology, which is referred as *CSI with series AC capacitors* (CSI+SCaps). The proposed topology allows the CSI topology to operate with higher/maximum modulation depth for the whole PV voltage range, including at low and very low PV voltages. The concept behind the success of this inverter topology contributed from the use of series AC capacitors in the CSI's AC circuit. In essence, the added series capacitors allow the AC voltages "seen" at the AC side of the inverter to be reduced to match to the low and very low PV voltages at the DC side, and thus the DC-to-AC current transfer ratio (modulation depth) between the DC side and the AC side is always maximised. The use of series AC capacitors and high/maximum modulation depth results in the following improved features (compared to the standard CSI topology):

- Better input power quality with lower DC-link current ripple caused by high/maximum modulation depth operation, which is suitable to connect to the PV cells or to facilitate the design with smaller DC-link inductors.

- Better output power quality resulted from better AC output harmonics filtering formed by the added series AC capacitors and the conventional LC filters at the AC side of the inverter.

- Lower voltage stress on semiconductors and lower switching losses, as well as lower estimated semiconductor cost in terms of power installed in the devices.

It is noted that the proposed topology was firstly published in [38] , which was used to reduce switching voltage stress of semiconductors in a shunt active power filter application. However, the utilisation of this topology for grid-tied PV applications has never been considered. Details of the proposed topology related to the design of series capacitors, operation principles, analytical models, modulation methods and control strategies when used for grid-tied PV applications are presented in this thesis.

In order to broadly evaluate the performance and efficiency of the proposed CSI+SCaps topology, the six other three-phase transformerless inverter topologies presented earlier are also taken into consideration. This results in seven candidate inverter topologies as listed in Table 1.1. Their circuit configurations, modulation and control strategies and component designs are presented in this thesis. All candidate topologies are modeled and their operation is evaluated using the SABER simulation program and dedicated models. The obtained simulation results are used to evaluate the performance and efficiency of the proposed topology against the other candidates. An experimental test-rig is constructed and tested in order to validate the feasibility of the proposed topology and its performance in comparison to the standard CSI topology.

Inverter Topology	**Symbol**
Standard Voltage Source Inverter	VSI
Standard Current Source Inverter	CSI
Two-stage VSI with a Boost converter	VSI+Boost
Two-stage CSI with a Buck converter	CSI+Buck
Voltage fed Z-Source Inverter	ZSI-V
Current fed Z-Source Inverter	ZSI-I
CSI with Series AC Capacitors	CSI+SCaps

Table 1.1 Candidate grid-tied PV inverter topologies under investigation in this thesis

1.1 Thesis Objectives

The objectives of this thesis are:

- *To understand basic characteristics and models of the PV cells.*
  Understanding the characteristics of the PV cells is essential for the design of a compatible grid-tied PV inverter. Understanding the models of the PV cells is useful for simulation work and the design of a controller for an analogue PV emulator that works in conjunction to a controllable DC voltage source, to be used in experimental work.

- *To understand the requirements for a grid-tied PV inverter.*
  Understanding the requirements for a grid-tied PV inverter is important for the design of a high efficient and high performance inverter complying with all relevant grid codes and standards.

- *To review available topologies for three-phase, transformerless grid-tied PV inverters.*
  Reviewing available inverter topologies provides preliminary information which can be used for further improvement and for assessment of new candidate inverter types. The selected topologies are a standard VSI, a standard CSI, a two-stage VSI with a boost converter, a two-stage CSI with a buck converter, a voltage fed ZSI and a current fed ZSI.

- *To propose an alternative topology of the CSI with series AC capacitors.*
  Several advantages of the CSI topology and the possibility to achieve variable AC voltage by using series AC capacitors that can lead to high efficient and high performance power conversion.

- *To simulate and evaluate the performance of the CSI with series AC capacitors compared to the other available transformerless topologies.*

- *To construct a prototype CSI with series AC capacitors.*

  The prototype CSI with series AC capacitors is used to validate the feasibility of the topology.

- *To experimentally evaluate the performance of the CSI with series AC capacitors in comparison to a standard CSI topology and simulation results.*

1.2 Thesis Structure

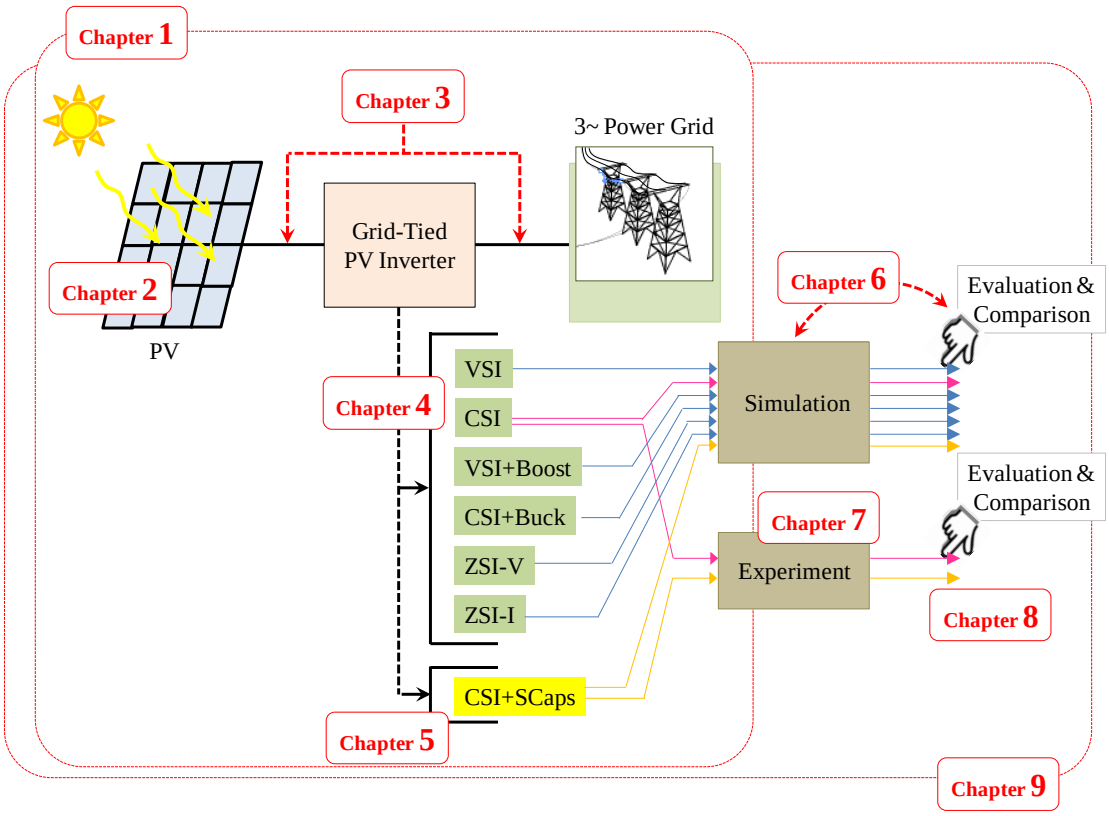


Figure 1.3 Thesis structure

Figure 1.3 shows the structure of this thesis. The thesis consists of nine chapters which are detailed as follows:

Chapter 1 introduces the background and objectives of this research work together with the structure of this thesis.

Chapter 2 presents the basic background knowledge of the PV cells including cell structures, materials, operation principles, electrical characteristics and models, and modeling methods for the PV cells from the datasheet to be used in the simulation work.

Chapter 3 details the typical requirements for the grid-tied PV inverters including the requirements on the PV cells, the requirements on the AC grid (grid codes, standards and regulations) and the other relevant requirements.

Chapter 4 presents a review of six potential topologies of transformerless, grid-tied PV inverters. The topologies under investigation are a standard VSI, a standard CSI, a two-stage VSI with a boost converter, a two-stage CSI with a buck converter, a voltage fed ZSI and a current fed ZSI. Details of their circuit configurations, modulation and control methodologies, and component design as derived from interfacing a PV string of same power level to the grid are presented; where the voltage and current can vary to best suit each topology.

Chapter 5 presents details of circuit configuration, analytical models and equations, operation principles, modulation and control strategies, and component design for the CSI with series AC capacitors. Possible applications of this inverter type are also discussed, e.g. reduced component voltage rating, improved AC output current with better high frequency harmonic reduction and reduced size of the DC-link inductor.

Chapter 6 presents a performance evaluation for the proposed topology compared to the six other topologies (Chapter 4) by using the simulation models and results. The evaluation in terms of required PV voltage and current ratings, operating modulation depths, required circuit components, input and output power quality, voltage and current stresses on power semiconductors, estimated cost of power semiconductors based on the power installed in the devices, semiconductor power losses and efficiency are presented.

Chapter 7 presents the detailed design and construction for the experimental test rig which is used to validate the feasibility of the proposed topology.

Chapter 8 presents the experimental results obtained from the experimental test-rig presented in Chapter 7. There are two sets of the results presented. The first set is used to validate the functionality of the test-rig whilst the second set is used to experimentally evaluate the performance of the proposed topology in comparison to the standard CSI as well as to validate the simulation results presented in Chapters 5 and 6.

Chapter 9 presents the overall conclusions of the thesis, the summary of the achievements and the suggestions for the future work.

Chapter 2

Characteristics and Models of Photovoltaic Cells

As mentioned in Chapter 1, this thesis considers power converter topologies based on transformerless concepts which could be used to convert and feed electric power generated from photovoltaic (PV) cells into the grid. In order to facilitate the design for the converters so that the converters can extract the maximum power from the PV cells, a knowledge and model of the PV cell characteristics is essential.

This chapter presents the basic characteristics and associated models of the PV cells required for the converter design (presented in Chapters 3, 4, 5 and 7) and the simulation studies (presented in Chapters 5, 6 and 8). The chapter begins with a general overview of the PV cells related to their structures, materials and operating principles. The equivalent circuit models and equations, including the electrical characteristics, of the PV cells are then examined, followed by the methods used to form a PV module (panel) from several individual PV cells (or a PV array from several PV modules) for higher power production. Finally, a procedure to determine equivalent circuit models using the specifications given in the manufacturing datasheets is proposed and demonstrated.

2.1 Structures of PV Cells

PV cells are devices that can convert sunlight directly into electrical DC power using the *photovoltaic effect* discovered by Becquerel in 1839 [39] . PV cells are made from materials that can absorb solar energy, or *photons* [40], which then create electrons and hence can generate an electric current. The basic structures of PV cells can be considered as a stack of several layers of light absorbing material. Figure 2.1 shows

eight available PV cell structures and their typical materials. These structures are the *Homojunction*, *Heteroface*, *Heterojunction*, *n-i-p* (or *p-i-n*), *Schottky-Junction*, *Dye-Sensitised*, *Organic* and *Multijunction* [41-45].

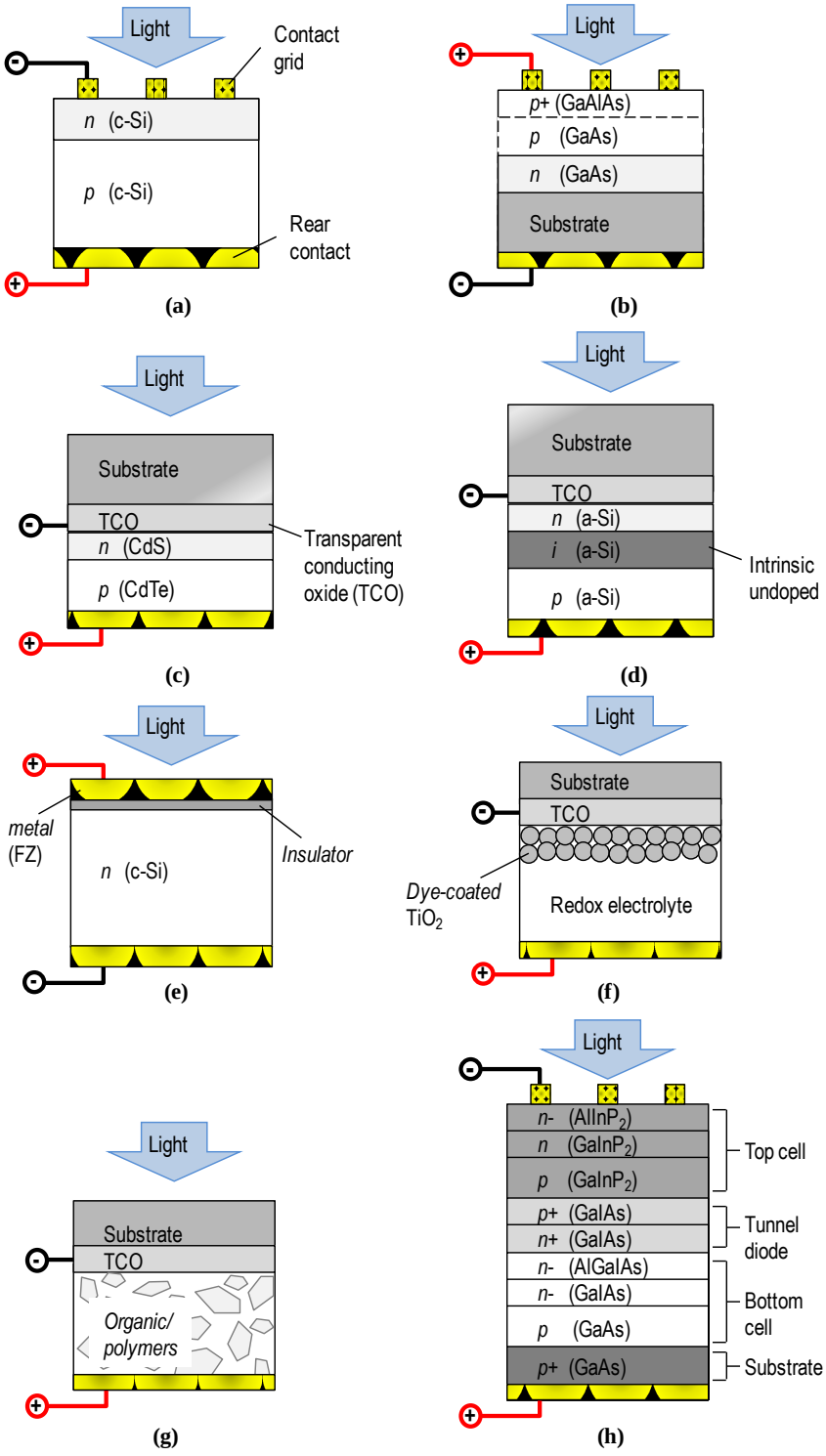


Figure 2.1 Basic structures of a PV cell: (a) Homojunction, (b) Heteroface, (c) Heterojunction, (d) n-i-p (or p-i-n), (e) Schottky-Junction, (f) Dye-Sensitised, (g) Organic and (h) Multijunction

The PV cell structures shown in Figure 2.1 have the following features:

- *Homojunction* (Figure 2.1a), also called *Single-Junction*, is the most popular and simplest structure. This structure consists of only one material type (e.g. c-Si) but with different impurity (doping) rates on each side.

- *Heteroface* (Figure 2.1b) has a similar structure to Homojunction except a thin layer of a large band-gap semiconductor material is added to reduce surface charge recombination [41], for example, a layer of GaAlAs is added in a GaAs Heteroface cell (see explanation about the band-gap in Section 2.2).

- *Heterojunction* (Figure 2.1c) has two different semiconductor materials: a high band-gap material (e.g. CdS) on the top and a low band-gap material (e.g. CdTe) on the bottom [45].

- *p-i-n* (or *n-i-p*) structure (Figure 2.1d) is a three layer sandwich configuration. A layer of intrinsic undoped material (*i*-type) is inserted in the middle between the thin layers of *p*-type and *n*-type materials to separate electric fields produced by holes and electrons. The amorphous silicon thin-film (a-Si) cells and cadmium telluride (CdTe) cells are the typical examples for this structure [45].

- The *Schottky-junction* structure (Figure 2.1e) creates the *p-n* junction barrier by the contact of metal (e.g. FZ) and a semiconductor material (e.g. c-Si). A very thin layer of insulating material (in a few nanometres) is inserted between them to prevent charge recombination (see more explanation of *p-n junction* in Section 2.3).

- The *Dye-sensitised* cell (Figure 2.1f) is classified as a photoelectrochemical device. The structure of this cell type consists of a dye-sensitised material and a liquid conductor (electrolyte). The dye-sensitised material, e.g. dye-coated titanium dioxide (TiO_2), absorbs sunlight, generates electrons and then returns the electrons through the electrolyte [42].

- The *Organic* cell (Figure 2.1g), also called *plastic* cell or *polymer* cell, has a flexible structure. This PV cell structure consists of organic semiconductor materials such as polymers (e.g. MEH-PPV, MDMO-PPV and P3OT) to absorb sunlight and create electrons-holes [43].

- *Multijunction* (Figure 2.1h), also called *Cascade* or *Tandem* structure, is the most complicated structure but has the highest efficiency. The structure can be formed as a monolithic structure or as a stack of several individual PV cells with different band-gap materials on top of one another (the highest band-gap on the top and the lowest band-gap on the bottom). By summing all the individual band-gaps together more of the sun's energy can be absorbed and so a higher output power is produced by the same PV cell area [45].

The Homojunction and Heteroface are the common structures for monocrystalline PV cells (i.e. c-Si cells) that can provide high efficiency whilst using only one type of material and a smaller installation area. Thus, these structures are suitable for the PV cells used in PV power system that are required to have a small installation area, e.g. residential (roof-top) applications. The Heteroface, Heterojunction, p-i-n (or n-i-p), Schottky-junction, organic and dye-sensitised are the popular structures for amorphous (non-crystalline) and/or thin film PV cells. These structures allow various materials (including low cost materials e.g. thin film, organic or dye-sensitised materials) to be used for the PV cells. However, these structures provide lower efficiency than monocrystalline PV cells; therefore, a larger installation area is required in order to provide the same output power as monocrystalline PV cells. As a result, these structures are suitable for lower cost solar power systems where the large installation area is available or the cost for large installation area is not prohibitive. The Multijunction structure is usually used for concentrator PV cells (where several beams of sunlight are focused into the cells for high power production), which leads this structure to have the most efficiency. However, since several layers of materials are used, this structure is the most complicated and the most expensive. Therefore, the Multijunction PV cells are suitable for large-scale PV power systems in order to reduce the production cost per unit power generated.

2.2 Materials of PV Cells

The materials used for the construction of PV cells are light absorbing materials which absorb sunlight, create electrons-holes and hence can generate electric current. Figure 2.2 shows some typical PV materials for different degrees of crystallinity and sunlight concentration factors [46],[47]. PV cells made from materials with higher degrees of crystallinity and sunlight concentration factors usually have a higher efficiency but are typically more expensive due to more difficult fabricating processes and the larger quantity of material needed.

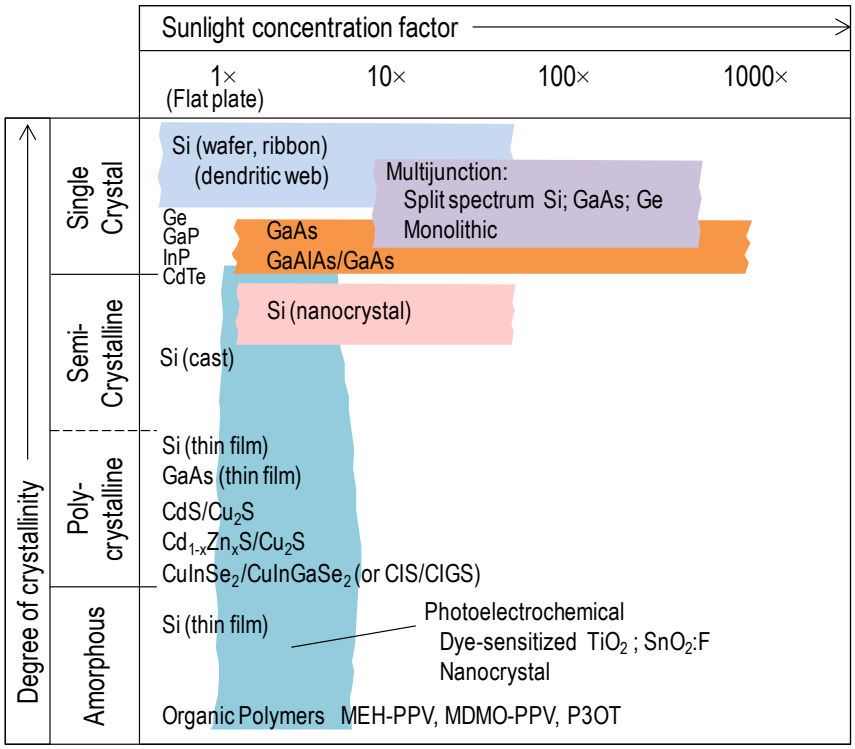


Figure 2.2 Typical PV materials for different degrees of crystallinity and sunlight concentration factors [46]

It can be seen from Figure 2.2 that:

- Silicon (Si) is the most widely used material for most PV cell formats.
- Silicon (Si), gallium arsenide (GaAs) and germanium (Ge) are the most commonly used materials for high sunlight concentrating PV cells, which usually have a format of single crystalline (Homojunction structure).

- Thin film materials such as amorphous silicon (a-Si), cadmium telluride (CdTe), copper indium gallium diselenide ($CuInSe_2$ or $CuInGaSe_2$), organic materials and dye-sensitised materials are usually used for poly crystalline (or multi-crystalline) PV cells and amorphous thin film PV cells (*n-i-p* structure). These materials are low cost materials, flexible with various producing methods, lighter (with a thickness of a few nanometres to tens of micrometres) and ease of integration.

- Other types of thin film materials are a compound of the group I, III and VI elements in the periodic table, [Cu Ag Au]:[Al Ga In]:[S Se Te]$_2$. The most reliable compounds for large scale PV production would be ones from the family of $CuInSe_2$.

The term which is usually referred to when considering the PV cell materials is *band-gap* (E_g). The band-gap is the light absorbing property of semiconductor materials. The band-gap is the minimum energy that is required to free an electron from the orbit of the materials and has the unit in eV (1eV= 1.602 $\times 10^{-19}$ J). Each semiconductor material will have a maximum power conversion efficiency at a specific band-gap. Figure 2.3 shows the typical band-gaps of the semiconductor materials and their corresponding maximum power conversion efficiencies. It can be seen that most materials provide their maximum efficiencies (18-23%) in the band-gap range of 1-1.7 eV.

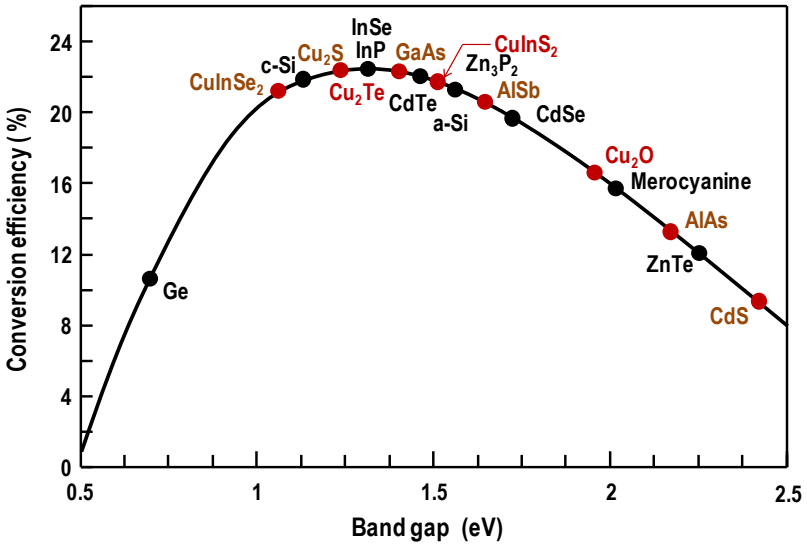


Figure 2.3 Band-gaps of semiconductor materials and their maximum theoretical power conversion efficiencies at room temperature (298K)

The progress achieved in energy conversion efficiency of different PV cell structures and materials over the past forty years is shown in Figure 2.4 [48], [49]. It can be seen from Figure 2.4 that Multijunction concentrating PV cells can achieve the best efficiency figures (32.8-42.8%), followed by Single-Junction (Homojunction) concentrating PV cells (28.8%), crystalline silicon PV cells (20.4-27.6%), thin film PV cells (12.5-20%), dye-sensitised (11.1%) and organic materials (7.9-9.7%).

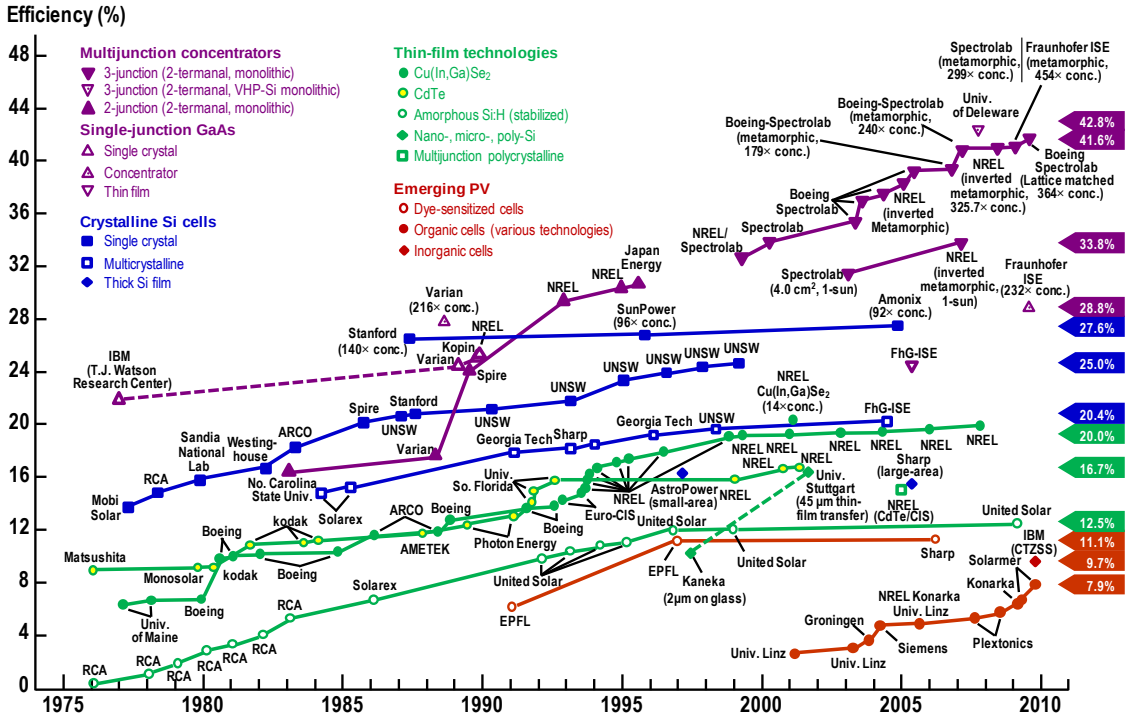


Figure 2.4 Timelines of energy conversion efficiencies of different PV cell structures and materials with their developers [48], [49]

2.3 Operation Principle of PV Cells

The process of converting sunlight to electricity in PV cells depends on the cell structures and materials. However, many have a similar concept of operation to a Heterojunction PV cell shown in Figure 2.5.

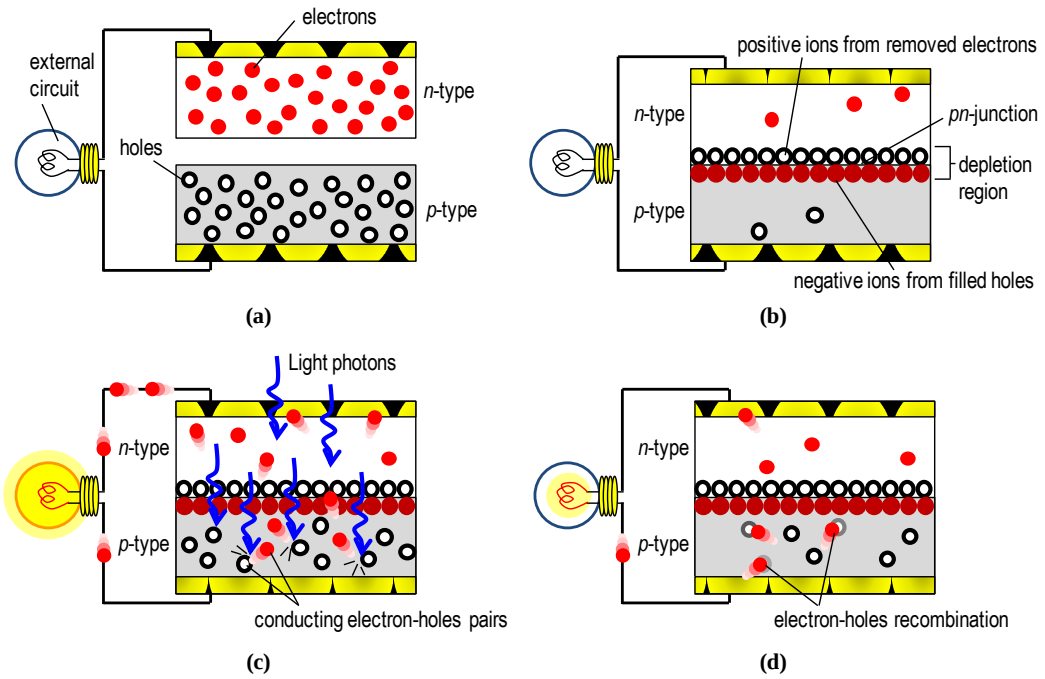


Figure 2.5 Basic PV operations; (a) before contacting *p*-type and *n*-type layers, (b) after contacting *p*-type and *n*-type layers, (c) under activating light photons and (d) after activating light photons

The Heterojunction PV cell consists of two semiconductor layers: *n*-type which contains negative charge carrier (electrons) and *p*-type which contains positive charge carriers (holes). Before contacting these two layers, electrons and holes can move freely within their respective layers, as shown in Figure 2.5a. Once the contact appears (Figure 2.5b), a migration of the electrons and holes occur in both layers and a *p*-*n* junction is created. Some of electrons from the *n*-type layer diffuse to combine with holes in the *p*-type layer and vice versa. This process creates a charge separating barrier known as the *depletion region* which will force the electrons to flow from the *n*-type layer to an external circuit (load) rather than directly to the *p*-type layer. There is very little electric current flowing in this situation since most free electrons and holes are virtually recombined.

In order to produce a significant current, many more free electrons and holes are required. More electrons and holes are produced by the action of the solar energy (or photons). The photons break the covalent bonds that join electrons to the nuclei in the lattices of the layers and release free electrons and holes. Then free electrons diffuse through the junction to the *n*-type layer and generate a potential difference between

the two electrodes and a consequent current in the external circuit that can be seen in Figure 2.5c. After that electrons from the external circuit return to recombine with holes in the p-type layer as shown in Figure 2.5d. If sunlight is continuously supplied, free electrons and holes will be continuously produced and hence a continuous current will be generated.

2.4 PV Equivalent Circuit Model and Equations

PV cells can be represented by the equivalent electrical circuit model, as shown in Figure 2.6. The model consists of four components:

- A DC current source (I_{ph}), which is used to represent the photocurrent generating mechanism of the PV cells.
- A diode (D_1) is used to represent the charge recombination process.
- Series resistor R_s which represents the total resistance that appears on the material surfaces and contacting interfaces.
- The parallel resistor R_p which represents any parallel high-conductivity paths within and at the edges of the cells.

The output current and output voltage of the cells (also called *cell current* and *cell voltage*) are denoted by I_{pv} and V_{pv}.

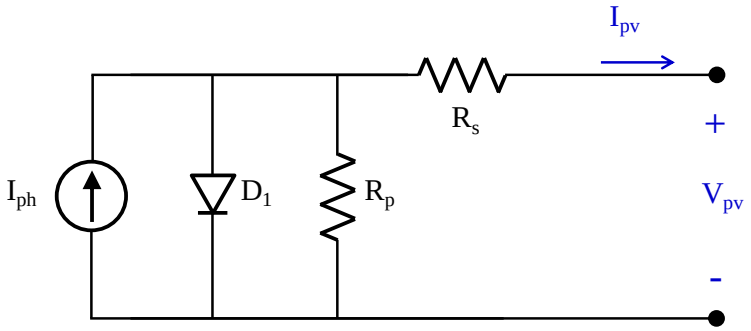


Figure 2.6 PV equivalent circuit model

From Figure 2.6, the cell current (I_{pv}) can be expressed as shown in (2.1).

$$I_{pv} = I_{ph} - I_{so}\left(e^{\left[\frac{q(V_{pv}+I_{pv}R_s)}{nkT}\right]} - 1\right) - \frac{(V_{pv}+I_{pv}R_s)}{R_p} \quad (2.1)$$

where I_{pv} = PV cell output current
V_{pv} = PV cell output voltage
I_{ph} = photogenerated current
I_{so} = diode reverse saturation current
R_s = cell series resistance
R_p = cell shunt resistance
n = diode ideality factor (or diode quality factor)
T = ambient temperature (in K)
q = elementary electric charge (1.6021765×10^{-19} C)
k = Boltzmann's constant (1.3806504×10^{-23} J.K^{-1})

The first term of the equation (2.1) refers to the photocurrent generated by the mechanism of the cells. The second term refers to the reverse current drawn by a diode D_1. The last term refers to the current drawn by the parallel resistor R_p.

The diode ideality factor (n) is a parameter that defines how closely the behaviour of the actual diode compares to a theoretical diode. The higher the value of n the higher the level of power can be produced from the PV cells, which can vary depending on technology and materials of the PV cells. Some typical values of n are presented in Table 2.1 [50].

Material-Technology	Diode Ideality Factor (n)
Si-mono	1.2
Si-poly	1.3
a-Si:H	1.8
a-Si:H tandem	3.3
a-Si:H triple	5.0
CdTe	1.5
CIS	1.5
AsGa	1.3

Table 2.1 Diode ideality factor (n) for different cell materials and technologies [50]

2.5 Electrical Characteristics of PV Cells

The maximum power that can be generated by the PV cells varies depending on two main external factors: sunlight intensity per unit area (*sun irradiance*; W/m^2) and voltage seen at the output terminals of the cells (cell voltage). The typical relationship between the output PV power and these two factors is presented with the P-V characteristic curves as shown in Figure 2.7.

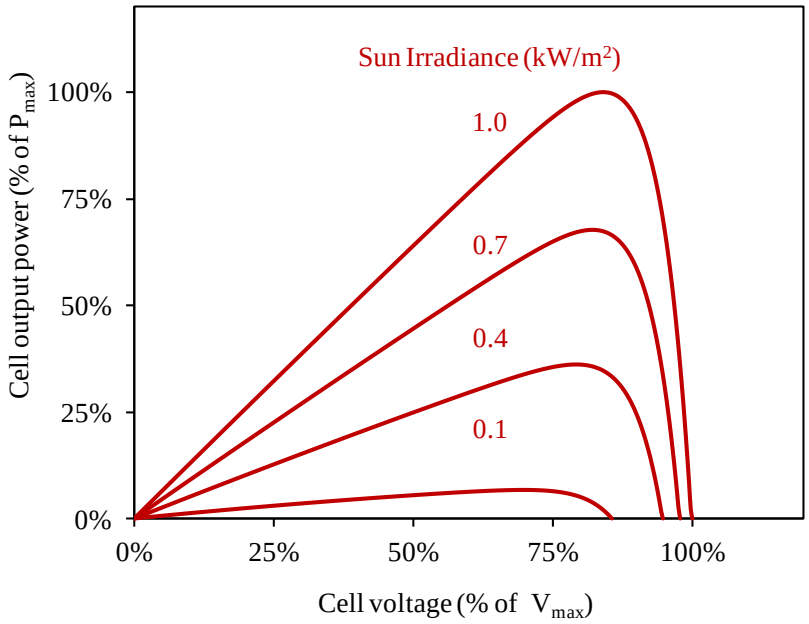


Figure 2.7 Typical power-voltage (P-V) characteristic curves of the PV cells

It can be seen from Figure 2.7 that:

- The maximum output PV power will increase when the level of sun irradiance increases.
- Under constant sun irradiance, the maximum output cell power varies with the cell voltage which has a range between zero and the maximum cell voltage (V_{max}). There is no power generated when the cell voltage is zero. Then the cell power increases with the increase of the cell voltage (in the range of 0% to 80% of V_{max}). After that the cell power decreases quickly and reaches zero output power again at V_{max} (100%). The maximum power points (*MPP*) of the PV cells are in the cell voltage range of 60%-90% of V_{max}.

In practice, electrical characteristics of the PV cells are usually represented by the current-voltage characteristic curves since they directly show the relationship between voltage and current of the cells. The typical current-voltage characteristic curves of the PV cells are shown in Figure 2.8.

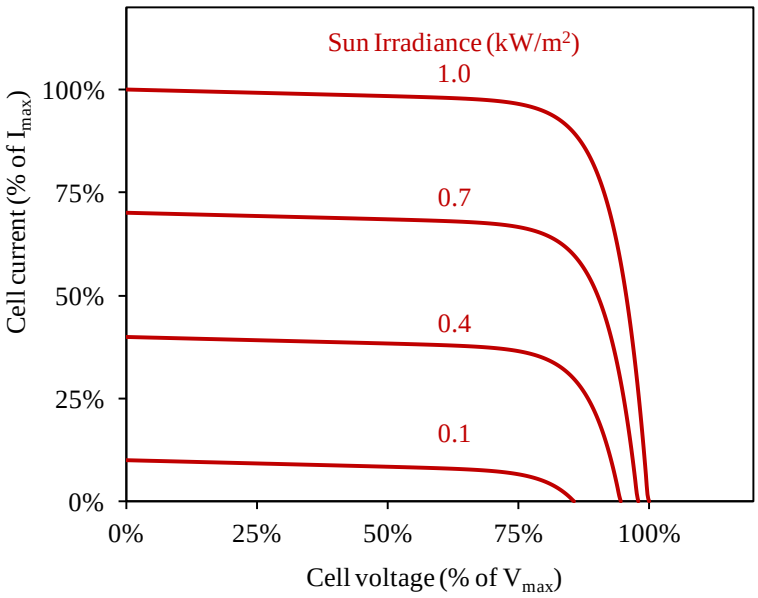


Figure 2.8 Typical current-voltage (I-V) characteristic curves of the PV cells

From Figure 2.8, it can be seen that:

- The PV cell current increases proportionally to the sun irradiance level (e.g. the maximum cell current (I_{max}) increases from 10% to 100% when the sun irradiance level increases from 10% to 100%).
- The PV cell voltage increases only in a narrow range when the sun irradiance level increases (e.g. the maximum cell voltage (V_{max}) increases from 80% to 100% when the sun irradiance level increases from 10% to 100%).
- Under constant sun irradiance, the output cell current varies nonlinearly with the cell voltage. The cell current retains almost constant in the cell voltage range of 0% to 75% of V_{max}. The cell current drops quickly when the cell voltage is higher than 75% of V_{max} and becomes zero at V_{max}.

The power-voltage characteristic curves are useful for the design of a power converter in order to be able to always extract maximum power from the PV cells. The current-

voltage characteristic curves are useful for the design of a power converter in order to have the current and voltage ratings compatible with the ratings of the PV cells.

2.6 PV Modules

Since a single PV cell can produce only a limited output power, several single cells are usually combined together for higher power generation. The combination of several single cells is commonly known as a PV *module* or PV *panel* and the composition of several PV modules is known as a PV *array*. There are three common ways to form a PV module [30], which can be achieved by connecting the cells in series or in parallel or both series and parallel as shown in Figures 2.9a-c.

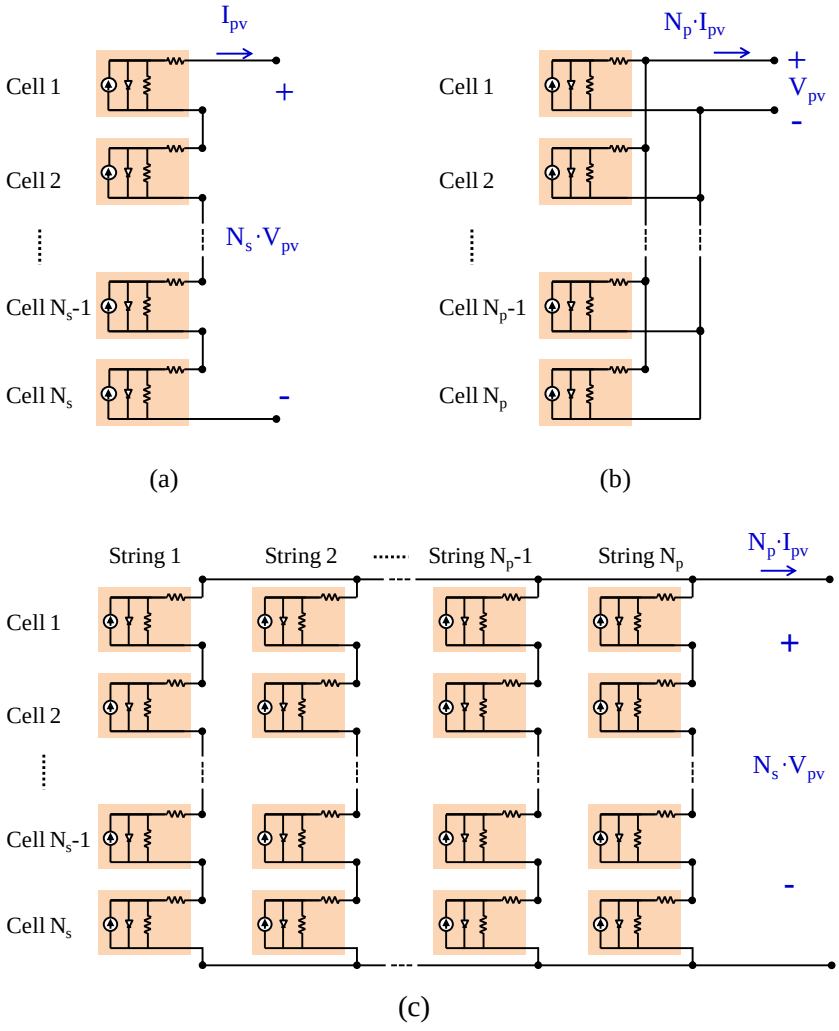


Figure 2.9 Three common ways to form a PV module with single PV cells: (a) by connecting single PV cells in series, (b) by connecting single PV cells in parallel and (c) connecting single PV cells in both series and parallel

When considering a PV module with N_s cells connected in series (or a string of N_s single PV cells) as shown in Figure 2.9a, the total module output voltage will increase by N_s times the output voltage of a single cell while the module output current will be the same as the one of a single cell. When considering a PV module with N_p cells connected in parallel (or N_p strings of a single PV cell) as shown in Figure 2.9b, the total module output current will increase by N_p times the output current of a single cell while the module output voltage will be the same as the one in a single cell. In order to provide the module output voltage of N_s times of the output voltage of a single cell and the module output current of N_p of the output current of a single cell at the same time, a PV module with N_p strings of N_s single PV cells as shown in Figure 2.9c will be used. The same concept can be extended to series and parallel connected PV modules in order to form a PV array. The equation for a PV module (or a PV array) with N_P strings of N_S series cells is expressed by (2.2).

$$I_{pv} = N_p \cdot \left[I_{ph} - I_{so} \left(e^{\frac{\frac{q}{N_S} \cdot \left[V_{pv} + \left(I_{pv} \cdot \frac{N_S R_S}{N_p} \right) \right]}{nkT}} - 1 \right) - \frac{\frac{1}{N_S} \cdot \left[V_{pv} + \left(I_{pv} \cdot \frac{N_S R_S}{N_p} \right) \right]}{R_p} \right] \qquad (2.2)$$

Figure 2.10 shows the equivalent circuit model for a PV module (or a PV array) with N_P strings of N_S series connected cells. It can be seen that a higher number of series PV cell (*Ns*) can cause a higher internal PV resistance. This can cause a dip in level of the output cell current and therefore a potentially lower output power (see more details in Section 2.7.3).

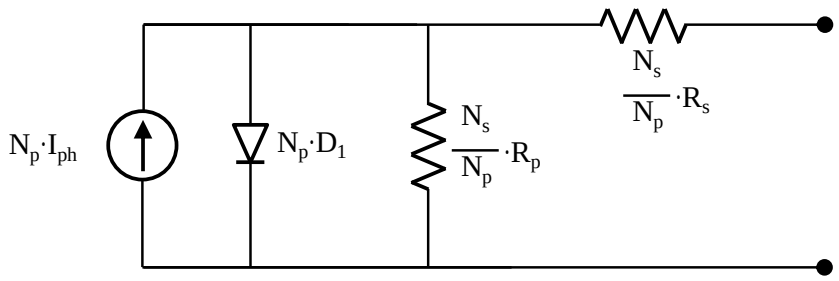


Figure 2.10 An electrical PV equivalent circuit model of a PV module with N_p strings of N_s series connected cells

2.7 PV Equivalent Circuit Modelling from the Datasheets

As presented in Section 2.4 and Section 2.6, any PV cells (or modules or arrays) can be represented by the PV equivalent model and equations. The equivalent model and equations are usually used in simulation work, which helps to reduce development costs and provide controllable test conditions. Unfortunately, most commercial PV products do not directly provide the equivalent model in their published datasheets. In fact, most datasheets provide typical specifications obtained from the specific test conditions only.

2.7.1 Typical PV Specification Parameters in the Datasheets

This section presents typical PV specification parameters which are usually included in the datasheets. In Section 2.7.2 it will be shown how typical PV parameters given in the datasheets can be used to determine the PV model of the actual PV products. Figure 2.11 shows typical PV specification parameters of a PV module on the PV characteristic curves; using the definitions presented in Table 2.2.

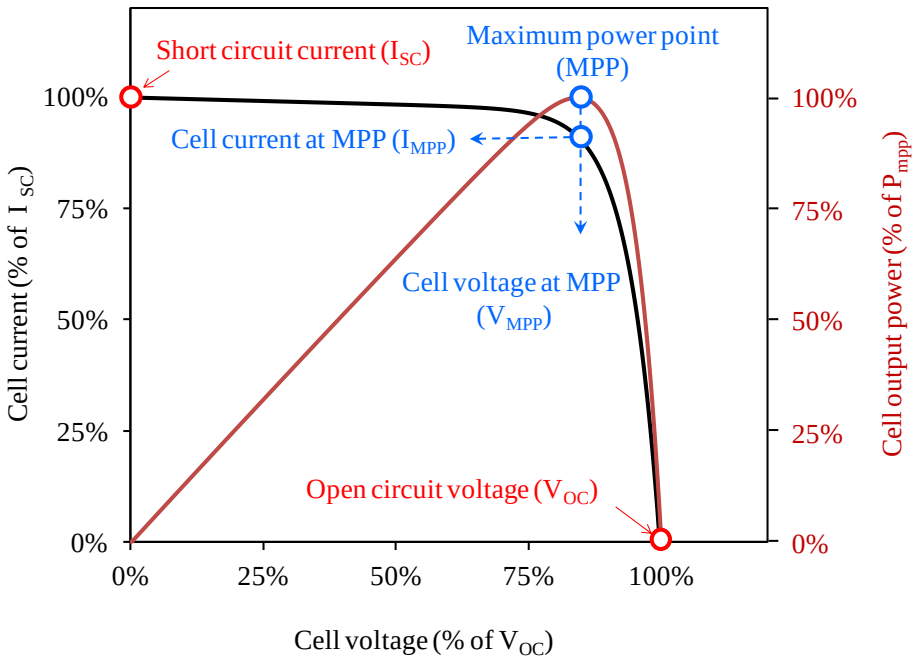


Figure 2.11 Typical PV Specification parameters in the datasheets

PV Specification Parameter	Name	Definition
I_{SC}	Short-circuit current	Maximum current of the PV cell with a short-circuit at the PV terminals
V_{OC}	Open-circuit voltage	Maximum voltage of the PV cell with an open-circuit at the PV terminals
P_{max}	Maximum Power	Maximum output power of the PV cell
V_{mpp}	Voltage at P_{max}	Output voltage of the PV cell at maximum power point
I_{mpp}	Current at P_{max}	Output current of the PV cell at maximum power point
FF	Fill Factor	• The ratio of the actual maximum obtainable power to the theoretical maximum power. • $FF = (I_{mpp} \times V_{mpp})/(I_{SC} \times V_{OC})$ • Typical commercial PV modules should have a *FF* greater than 0.7 whilst the modules with a *FF* between 0.4-0.7 are considered as grade B modules

Table 2.2 PV Specification parameters and their definitions

The PV module is usually tested under the conditions called *Standard Test Conditions* (STC), which are under sun irradiance of 1 kW/m^2, ambient temperature of 25^{o}C and 1.5 Air Mass (Air Mass is a measure of the thickness of the atmosphere that influences the solar spectrum; 1 Air Mass refers to that at the earth's surface). Some datasheets also provide the effect of the ambient temperature on the electrical characteristics of the PV modules, which would be shown either with numbers (e.g. -80±10mV/^{o}C) or with curves (e.g. the one shown in Figure 2.11).

2.7.2 PV Equivalent Circuit Modelling Procedure

This section presents a procedure to determine the PV equivalent circuit model using the information given in the PV specification datasheets. In order to complete the model, the parameters I_{ph}, I_{so}, n, R_s and R_p must be known. These parameters can be determined by using the steps shown in Tables 2.3. It is noted that the calculated values of these parameters are only the initial values for the model. A more accurate model which provides electrical characteristics close to the actual PV module would be achieved by tuning the values of these parameters in the way presented in Section 2.7.3.

Step	PV Parameter	Description
1	n	Select n from Table 2.1 by considering the cell material and the cell technology of a PV cell
2	I_{ph}	Considering short-circuit condition where $I_{pv}=I_{SC}$ and $V_{pv}=0$. Assume that R_s is very small and R_p is very large and with the use of (2.2), I_{ph} can be calculated from (2.3) $$I_{ph} = \frac{I_{sc}}{N_p} \quad (2.3)$$
3	I_{so}	Considering open-circuit condition where $I_{pv}=0$ and $V_{pv}=V_{OC}$. Assume that R_p is very large. Substituting all known parameters for (2.2), I_{so} can be determined from (2.4) $$I_{so} = \frac{I_{sc}}{e^{\left(\frac{qV_{oc}}{N_s nkT}\right)}-1} \quad (2.4)$$
4	R_s	Differentiating (2.2) by V_{pv} and considering the curve at the V_{OC} point, R_s can be estimated by (2.5); where dI_{pv}/dV_{pv} is the slope of the I-V curve at the V_{OC} point $$R_s = -\frac{N_p}{N_s}\left(\frac{1}{\left(\frac{dIpv}{dVpv}\right)\Big\|_{V_{oc}}} + \frac{1}{X_v}\right) \; ; X_v = \frac{qI_{so}}{N_s nkT} e^{\left(\frac{qV_{oc}}{N_s nkT}\right)} \quad (2.5)$$
5	R_p	Substituting all known parameters for (2.2) and at MPP, R_p can be determined by (2.6) $$R_p = \frac{1}{N_s} \cdot \frac{\left(V_{mmp}+I_{mmp}\cdot\frac{N_S R_S}{N_p}\right)}{I_{sc}-\frac{I_{mmp}}{N_p}-I_{so}\left(e^{\frac{q\left(V_{mmp}+I_{mmp}\cdot\frac{N_S R_S}{N_p}\right)}{N_S nkT}}-1\right)} \quad (2.6)$$

Table 2.3 PV modelling procedure using the information given from the datasheets

2.7.3 Effects of PV Equivalent Parameters on the PV Characteristic Curves

This section presents the effects of PV equivalent circuit parameters (R_s, R_p, n and I_{so}) on the characteristic curves of the PV module. This knowledge is useful for tuning the parameters in order to obtain a more accurate PV equivalent model. The effects of these parameters can be observed in Figure 2.12. It is noted that the numbers shown are only the examples. The actual values should be obtained using the procedure presented in Table 2.3.

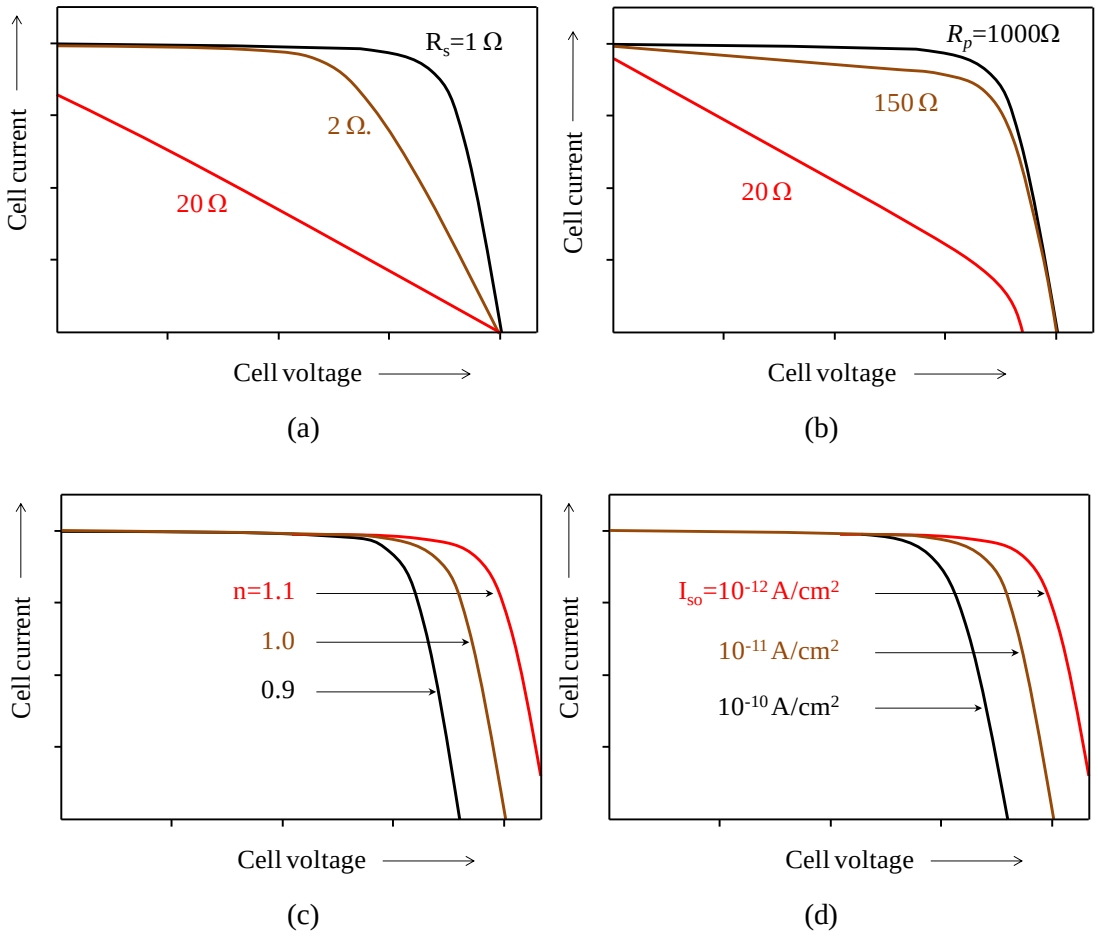


Figure 2.12 Effects of PV equivalent parameters on the PV characteristics of the PV cell caused by the effects of (a) R_s, (b) R_p, (c) n and (d) I_{so}

It can be seen from Figure 2.12 that:

- From Figure 2.12a, only a small change of R_s can cause a significant change of the PV curves, i.e. a slightly increase in the value of R_s (from 1Ω to 20Ω) can cause a large dip in the PV cell current of more than 50%.

- From Figure 2.12b, a large change in R_p is needed in order to cause a significant change of the PV curves, i.e. a much smaller value of R_p (from 1000Ω to 20Ω) is needed in order to cause a large dip in the PV cell current more than 50%.

- From Figure 2.12c, increasing the value of n will increase the maximum cell voltage and hence lead to a wider range of PV cell voltage.

- From Figure 2.12d, the inverse result of n will be seen for I_{so}. Increasing I_{so} will reduce the maximum PV cell voltage and hence cause a narrower range of PV cell voltage.

Besides the parameters R_s, R_p, n and I_{so}, ambient temperature (T) is also one of the major factors that can cause a significant change of characteristic curves of the PV module. Figure 2.13 shows the effect of ambient temperature on the characteristic curves of a crystalline silicon (c-Si) PV module [51]. It can be seen that when the ambient temperature increases, the maximum PV cell current will increase whilst the maximum PV voltage decreases. This is because of the fact that when the ambient temperature increases, the PV cells absorb more energy and releases more electrons and holes. As a result, the excessive electrons cause a higher output cell current and a larger amount of electron-hole pairs causes a higher rate of charge recombination inside the cell and hence causes a drop of the output cell voltage.

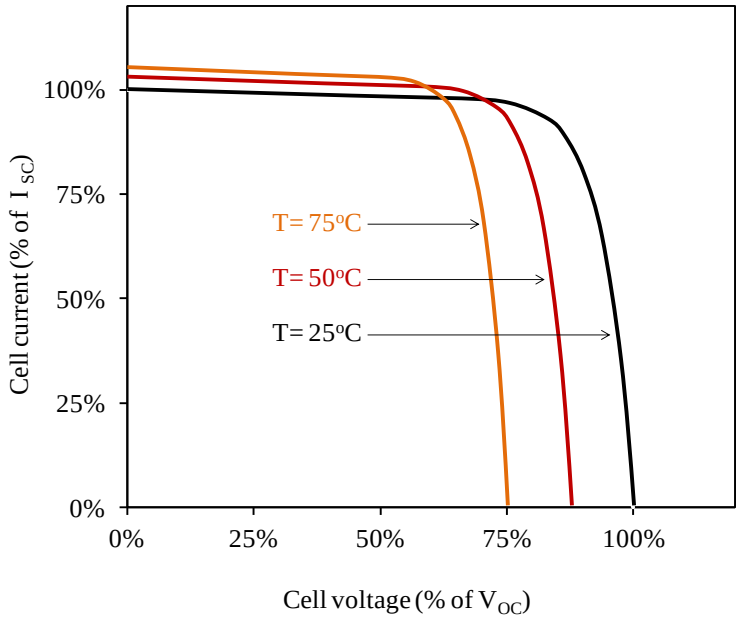


Figure 2.13 Effect of ambient temperature on the characteristics of c-Si PV cells [51]

When variation of the ambient temperature (T) is also considered for the PV equivalent model, the PV equivalent parameters I_{ph}, I_{so}, R_s and R_p can be expressed as (2.7)-(2.10) [52], [53].

$$I_{ph}(T) = \left(I_{ph1} + K_1(T - T_1)\right) \cdot G_{sun} \tag{2.7}$$

$$I_{so}(T) = I_{so1} \cdot \left(\frac{T}{T_1}\right)^3 \cdot \left(e^{\frac{-qE_g}{nk}\left[\frac{1}{T} - \frac{1}{T_1}\right]}\right) \tag{2.8}$$

$$R_s(T) = R_{s1} \cdot \left(1 - K_2(T - T_1)\right) \tag{2.9}$$

$$R_p(T) = R_{p1} \cdot e^{(-K_3 T)} \tag{2.10}$$

where

I_{ph}(T) = photogenerated current at any temperature T (in K)

I_{so}(T) = diode reverse saturation current at any temperature T (in K)

R_s(T) = series resistance of the PV cell at any temperature T (in K)

R_p(T) = parallel (shunt) resistance of the PV cell at any temperature T (in K)

I_{ph1} = photogenerated current at room temperature T_1 (298°K)

I_{so1} = diode reverse saturation current at room temperature T_1 (298°K)

R_{s1} = series resistance of the PV cell at room temperature T_1 (298°K)

R_{p1} = shunt resistance of the PV cell at room temperature T_1 (298°K)

G_{SUN} = sun irradiance level (0 to 1; 1Sun=1kW/m^2)

K_1 = photogenerated current temperature coefficient

K_2 = series resistance temperature coefficient

K_3 = parallel (shunt) resistance temperature coefficient

E_g = band gap (in eV; 1eV=1.6021765×10-19 J)

The knowledge of the effect of ambient temperature on the PV characteristic curves is useful for fine tuning the parameters of the PV equivalent circuit model in the simulation studies where the ambient temperature is also considered.

2.7.4 An Example of PV Equivalent Circuit Modelling

This section demonstrates how to construct the PV equivalent circuit model from the datasheet information. A commercial PV module BP SX30 [54] with the specification datasheet shown in Figure 2.14 is used for this example.

Typical Electrical Characteristics[1]	BP SX 30
Maximum Power (P_{max})[2]	30W
Voltage at P_{max} (V_{mp})	16.8V
Current at P_{max} (I_{mp})	1.78A
Warranted minimum P_{max}	27W
Short-circuit current (I_{sc})	1.94A
Open-circuit voltage (V_{oc})	21.0V
Temperature coefficient of I_{sc}	(0.065±0.015)%/°C
Temperature coefficient of V_{oc}	-(80±10)mV/°C
Temperature coefficient of Power	-(0.5±0.05)%/°C
NOCT[4]	47±2°C

Notes

1. These data represent the performance of typical modules in 12V configuration as measured at their output terminals, and do not include the effect of such additional equipment as diodes or cables. The data are based on measurements made in accordance with ASTM E1036-85 corrected to SRC (Standard Reporting Conditions, also known as STC or Standard Test Conditions), which are:
   - illumination of 1 kW/m² (1 sun) at spectral distribution of AM 1.5 (ASTM E892-87 global spectral irradiance);
   - cell temperature of 25°C.
2. During the stabilization process which occurs during the first few months of deployment, module power may decrease approximately 3% from typical Pmax.
3. U versions.
4. The cells in an illuminated module operate hotter than the ambient temperature. NOCT (Nominal Operating Cell Temperature) is an indicator of this temperature differential, and is the cell temperature under Standard Operating Conditions: ambient temperature of 20°C, solar irradiation of 0.8 kW/m², and wind speed of 1 m/s.

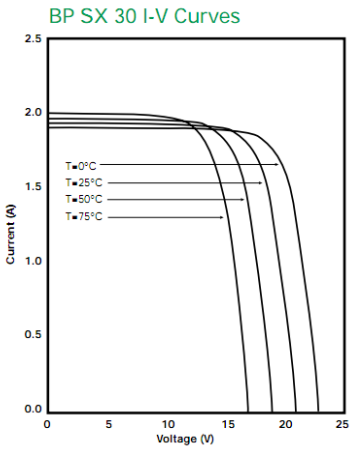


Figure 2.14 Specification datasheet of the PV module BP SX30 [54]

By following the procedure proposed in Section 2.6.2 and using the given information from the datasheet shown in Figure 2.14, the PV equivalent model parameters can be determined giving the values shown in Table 2.4.

PV Parameter	**Value**				**Unit**
	T=0°C	**T=25°C**	**T=50°C**	**T=75°C**	
n	1.3	1.3	1.3	1.3	-
I_{ph}	1.91	1.94	1.97	2.00	A
I_{so}	2	50	900	4500	nA
R_s	0.63	0.63	0.63	0.63	Ω
R_p	1.8	1.8	1.8	1.8	kΩ

Table 2.4 Calculated values of the PV equivalent parameters for the commercial PV module BP SX30 [54]

The PV equivalent model of the BP SX30 module was implemented in the SABER simulation program for verification. Figure 2.15 shows the simulation results obtained from the PV equivalent circuit model in comparison to the actual specifications of the datasheet.

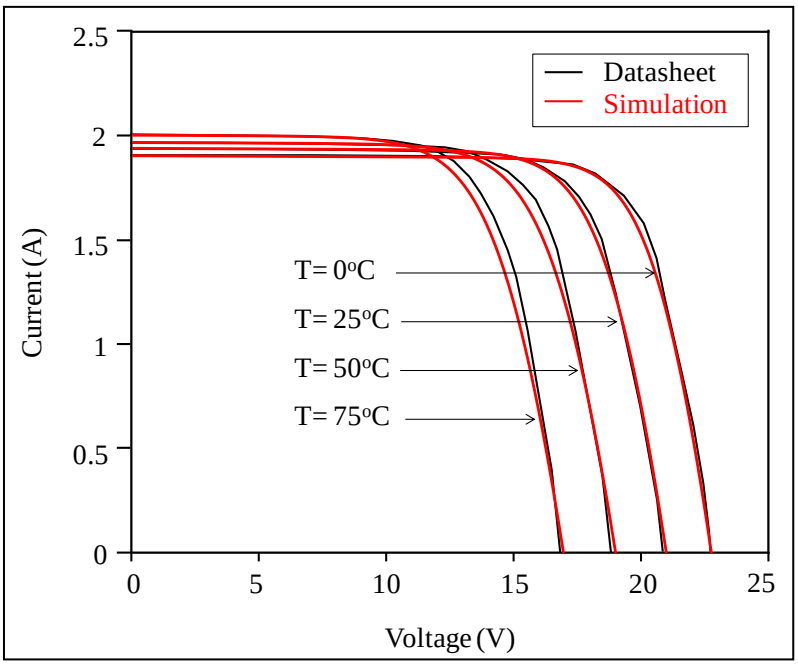


Figure 2.15 Comparison of the characteristic curves between the simulation PV equivalent model and the specifications of the datasheet

It can be seen from Figure 2.15 that the PV equivalent model can provide similar simulation results to the datasheet curves provided by the manufacturer. Small differences (around the corners of the compared curves) are the results of variation in the internal resistance (R_s and R_p) variation caused by thermal drift with the actual PV module. The effect of ambient temperature on the PV resistance is not considered in this simulation for simplification. Thus, the better curve fitting can be achieved by considering also the effect of thermal drift on R_s and R_p using (2.9) and (2.10). However, this will lead to a more complex and slower simulation module.

In the case that individual BP SX30 PV modules are connected in four strings of fourteen series connected modules (N_p=4, N_s=14), the modules form a PV array that gives the simulation results shown in Figures 2.16 and 2.17 and the specifications as shown in Table 2.5.

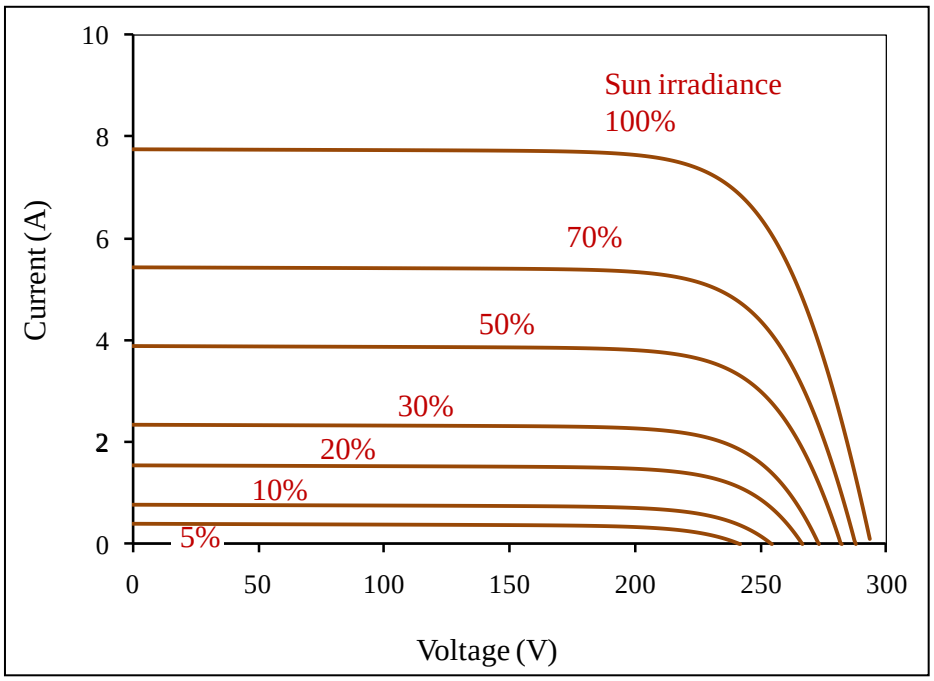


Figure 2.16 V-I characteristic curve obtained from the simulation PV equivalent model made from the 4 strings of 14 series-connected BP SX30 PV modules

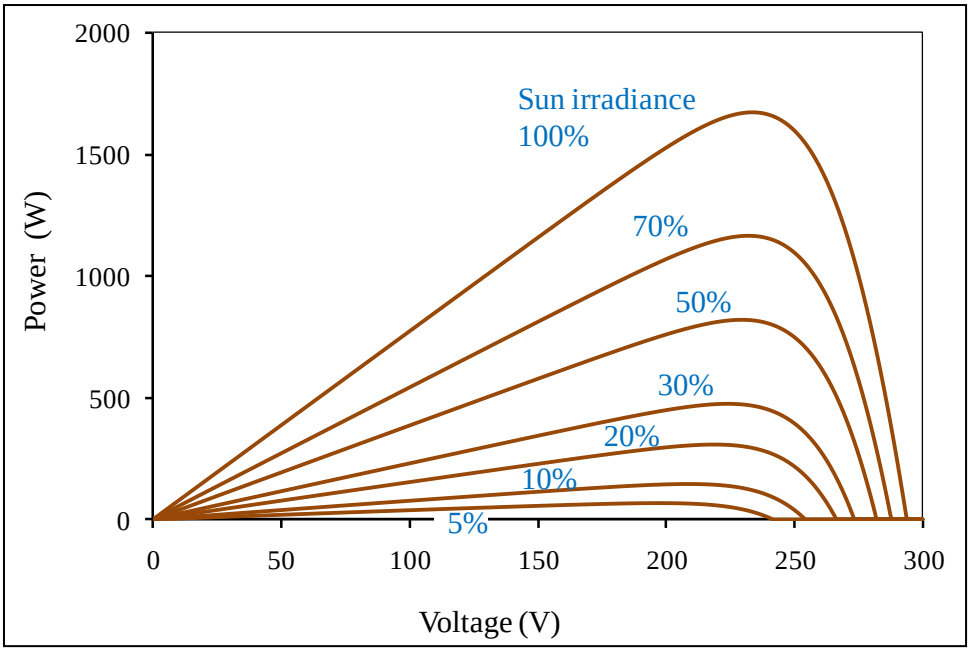


Figure 2.17 V-P characteristic curve obtained from the simulation PV equivalent model made from the 4 strings of 14 series-connected BP SX30 PV modules

PV Parameter	Value	Unit
P_{mpp}	1.67	kW
V_{mpp}	233.7	V
I_{mpp}	7.17	A
I_{SC}	7.76	A
V_{OC}	294	V
FF	0.73	-

Table 2.5 Specifications of the PV array of 4 strings of 14 series connected BP SX30 modules at the ambient temperature of 25^{o}C

It can be seen from Figures 2.16-2.17 and Table 2.5 that the PV equivalent model can provide the PV characteristic curves and specifications as required. As expected, the model produces an output voltage 14 times greater than a single PV module (V_{OC} of 294V compared to 21V) and an output current 4 times greater than a single PV module (e.g. I_{SC} of 7.76A compared to 1.94A). These PV specifications were used for the design of the PV emulator which has been used in the experimental work (Section 7.2 and Section 8.1).

2.8 Summary

This chapter has presented the fundamental characteristics of the photovoltaic (PV) cells, with insight into cell structures and materials. After a brief description of the principle of operation of the PV cells, the equivalent circuit model and the electrical characteristics of the PV cells are introduced. This knowledge is essential for the design of the power converter introduced in Chapters 3, 4 and 5 so that the use of PV cells is optimised to deliver the maximum possible power. The equivalent circuit model is used for the simulation work in Chapters 5 and 6 and the experimental work presented in Chapters 7 and 8.

Chapter 3

Characteristics of Grid-Tied PV Inverters

As mentioned in Chapter 1, this thesis considers power converter topologies which can convert and feed power from photovoltaic (PV) cells to the power grid. In order to understand fully the design of these topologies, the desirable characteristics required for these topologies should be studied, which are presented in this chapter. The characteristics on the PV side of the inverters, the characteristics on the grid side of the inverters and the other characteristics are presented.

3.1 PV Side Characteristics

The desirable characteristics for the PV side of the inverter aim to achieve maximum power extraction from the PV cells and connection compatibility between the inverter and the PV cells. The inverter is required to have the following basic features:

i. *ability to operate efficiently at the MPP of the PV cells*

ii. *ability to operate over the whole MPP range of the PV cells*

iii. *have a power rating matching to the maximum power rating of the PV cells*

iv. *withstand the maximum voltage and current of the PV cells regardless of the variation of ambient temperature*

The first and second requirements (*i* and *ii*) are a consequence of the maximum PV power extraction. The inverter should be able to operate at the *Maximum Power Point* (MPP) of the PV cells. As presented in Chapter 2, the MPP of the PV cells is usually within the PV cell voltage range of 60-90% of the maximum PV voltage rating.

Therefore, the inverter should also be able to operate with these voltages over the whole range for full PV power range extraction. The actual MPP and MPP range for the inverter based on these characteristics are shown in Figure 3.1.

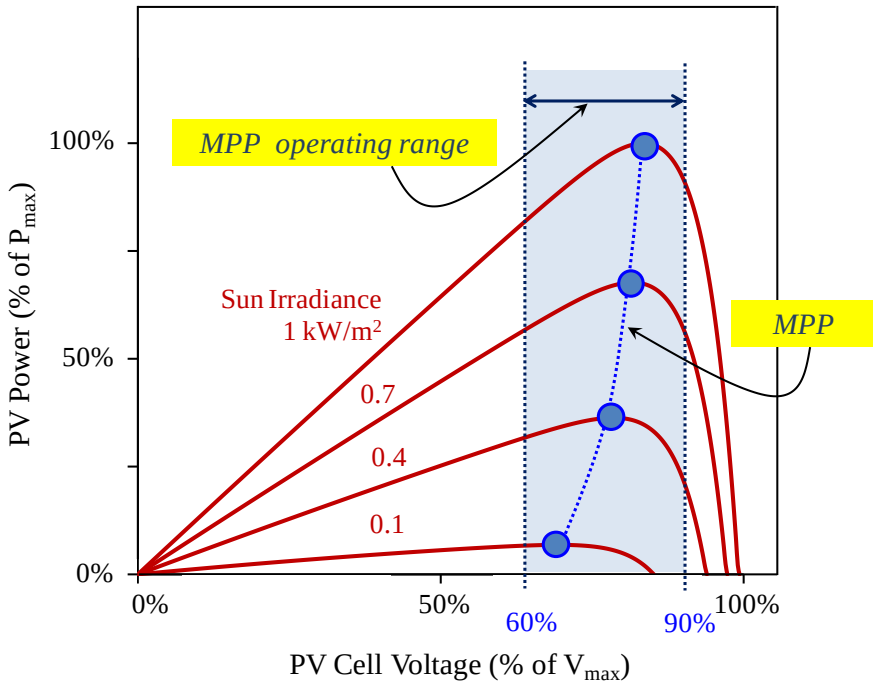


Figure 3.1 MPP and MPP range for the grid-tied PV inverter in order to achieve maximum PV power extraction and connection compatibility

The third and fourth requirements (*iii* and *iv*) are related to the connection compatibility between the inverter and the PV cells in the following points:

- The power rating of the inverter shall never be less than 90% of the maximum power of the PV cells in order to avoid overload conditions [55]. An inverter with a power rating lower than this could be applicable only for the areas where the output power from the PV cells does not reach its maximum rating.

- The inverter is required to withstand the maximum voltage of the PV cells. This limit should also consider the effect of the ambient temperature since high temperature can lead the PV current to be higher than its maximum rating whilst low temperature can cause the same effect but for the PV voltage (see more details in Section 2.7.3). Operation with a voltage exceeding the limit ratings of the inverter should be avoided because the excessive voltage can age electrical components of the inverter more quickly, reduce the working life

and potentially damage the inverter [56]. Therefore, the voltage rating of the inverter should be higher than maximum voltage of the PV cells as shown in Figure 3.2. The current must also be controlled to be less than the maximum under high temperature operation.

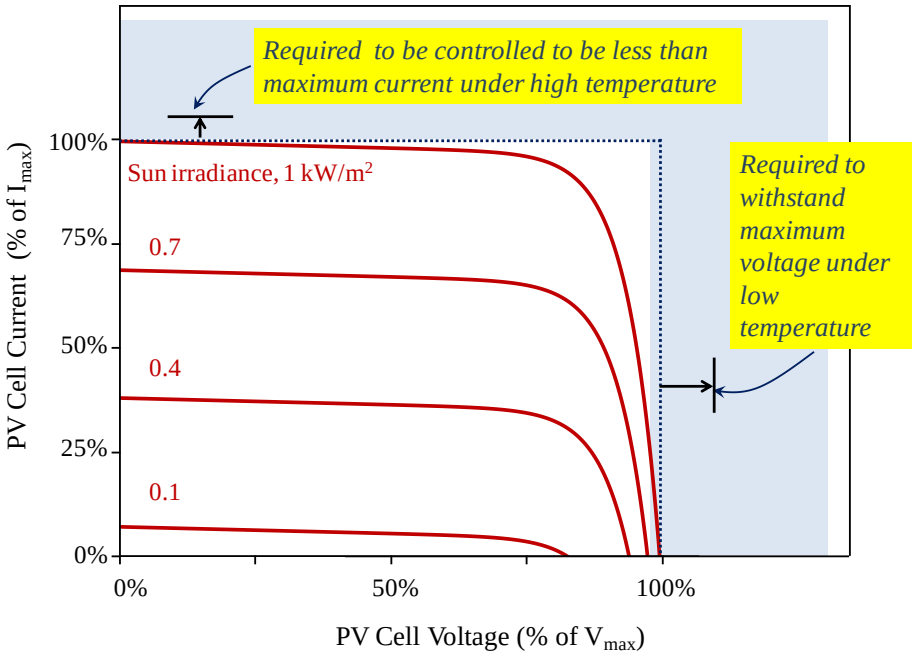


Figure 3.2 Required area for the grid-tied PV inverter to withstand the maximum voltage and maximum current of the PV cells

3.2 Grid Side Characteristics

The characteristics for the grid side of the power inverter are usually referred to as the *grid codes*. The grid codes are the technical specifications defined by an authority for permitting equipment connection to the power grid (e.g. connecting an independent power generating plant such a PV array to the grid). The main purpose of the codes is to ensure the safe and stable functionality of the grid. The grid codes vary from country to country. The E.On-Netz 2006 grid code [12] and UK-National Grid 2010 code [13] are the main references used in this thesis.

Besides the grid codes, in most cases, the grid-tied PV inverters are also required to comply with relevant *Standards*. The standards are the technical specifications published by independent global organizations. Standards IEC 61727, IEEE 1547 and

UL 1741 [14-16] are the main references used in this thesis. Basic requirements on the grid side for the grid-tied PV inverters required by the grid codes and standards are related to high output power quality, grid fault ride through capability and islanding prevention [24],[26],[28],[57].

3.2.1 High Output Power Quality

Grid-tied PV inverters are devices that may potentially contribute to power quality concerns, such as the degradation of the quality of grid voltage available to other users of the network. Grid-tied PV inverters are required to produce good quality output waveforms, which are synchronised with the voltage waveforms of the grid. The most common tools for measuring the power quality are *Total Harmonic Distortion* (THD) and *Power Factor* (PF) [14],[16].

3.2.1.1 Total Harmonic Distortion (THD)

The total harmonic distortion (THD) defines how much the ideal sine waveform is contaminated by harmonics. The higher the THD value the higher the distortion will be. The formula for calculating the THD of a waveform is derived and defined by the following analysis.

Any periodic, non-sinusoidal waveforms $U(t)$ can be expressed as a Fourier series as shown in (3.1). The first term of the series is the fundamental component whilst all others are the harmonics. The total harmonic distortion up to the h harmonic order is defined as (3.2).

$$U(t) = U_1 sin\omega t + \sum_{n=2}^{\infty} U_n \sin(n\omega t + \alpha_n) \quad ; \text{n= 2, 3, 4 … } \infty \tag{3.1}$$

$$THD = \frac{\sqrt{U_2^2 + U_3^2 + \cdots + U_h^2}}{U_1} \times 100\% \tag{3.2}$$

Table 3.1 shows the current harmonic emission limits at the point of common coupling (PCC) for grid voltages lower than 69kV as specified by the standards IEEE 1547 and IEC 61727. These specifications will be used to evaluate the performance of the considered inverter topologies in Chapter 6.

Bus Voltage	Maximum individual current harmonic order in % of load current (Odd harmonics)					THD (%)
	$h<11$	$11 \leq h < 17$	$17 \leq h < 23$	$23 \leq h < 35$	$35 \leq h$	
<69kV	4.0	2.0	1.5	0.6	0.3	5.0
	*even harmonics are limited to 25% of the odd harmonic limits above					

Table 3.1 Current harmonic emission limits specified by the Standards IEEE 1547 and IEC 61727 [14], [16]

3.2.1.2 Power Factor (*PF*)

Power Factor (PF) is defined as the ratio of the active (or real) power to the total apparent power. In terms of the waveforms, the PF is the cosine of the displacement angle between the fundamental (50/60Hz) voltage waveform and current waveform; therefore, the PF has a value between zero and one. Most electric power systems usually transfer the power with a PF equals to one (unity power factor). This is because the power systems with a PF lower than one have to draw more current in order to transfer the same amount of real power. As a result a power system with a low PF has higher losses and requires larger wires and other equipment than the one with a PF close to unity.

There is no requirement for the PF in the standard IEEE 1547. Only the standard IEC 61727 provides a recommendation for the PF as follows:

- *The PV power factor shall have an average lagging power factor greater than 0.9 when the output is greater than 50% of rated PV power*

Similar specifications can also be applied for an average leading power factor. Figure 3.3 shows a graphical illustration of this requirement.

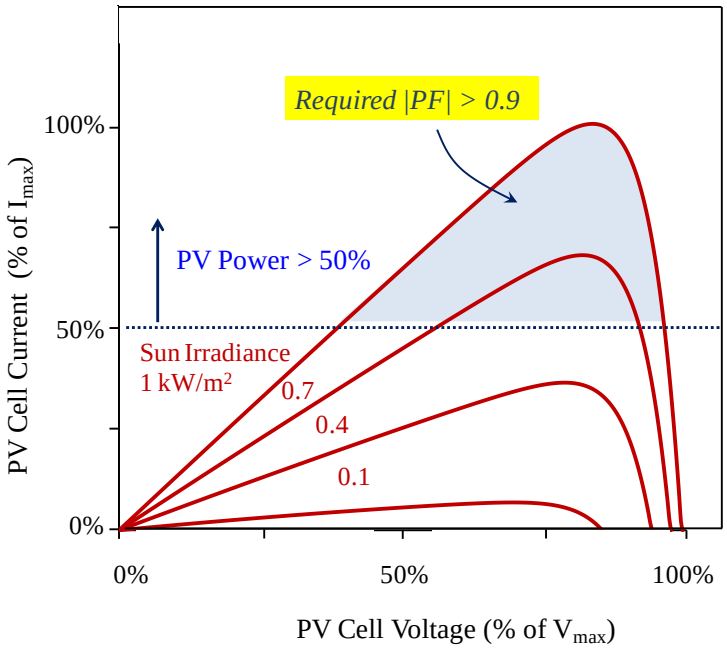


Figure 3.3 Required operating power factor recommended by Standard IEC 61727

3.2.2 Grid Fault Ride-Through Capability

Grid-tied PV inverters shall have the capability to ride-through grid faults in order to ensure safe and stable operation of the electrical network. The capability of grid fault ride-through is an ability to remain transiently stable and stay connected to the grid without tripping for a specified time during a grid fault disturbance. The inverters shall also be able to support the grid with a reactive current during fault and supply power to the grid immediately after fault clearance [12, 13], [58-60].

Figure 3.4 shows the required "stay-connected" time according to the level of the grid voltage based on the requirements of E.On-Netz 2006 grid code [12]. The inverter is required to stay connected to the grid for 150ms when the grid voltage drops to zero before the disconnection is permissible. A longer stay-connected time is required at higher voltage levels (e.g. 750ms when the grid voltage drops to 40% of its nominal level). The inverter must never disconnect from the grid if the grid voltage is higher than 90% of its nominal level. Active power must be injected into the grid immediately after fault clearance with an increasing rate of increase of at least 20% of the rated power per second.

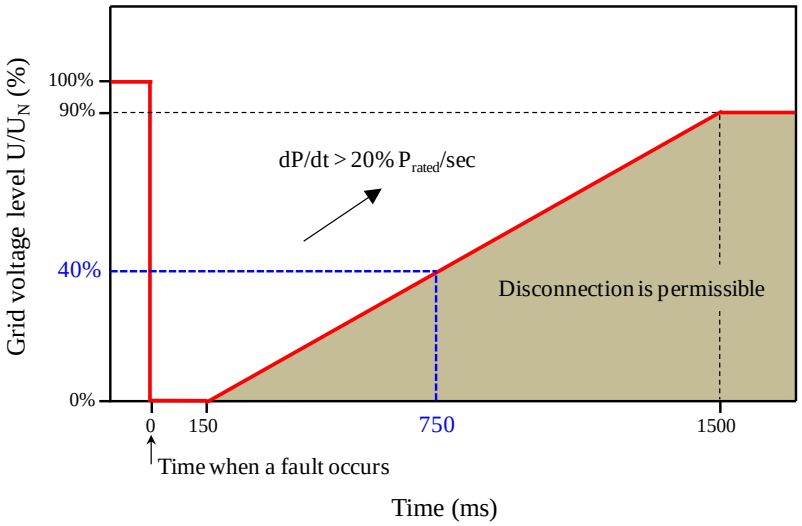


Figure 3.4 Required stay-connected time for a particular level of grid voltage required by the E.On-Netz 2006 grid code [12]

It should be noted that the stay-connected time for the grid fault ride-through varies from country to country. For example, grid voltage drops of 85% of the nominal level may last up to 625ms in the USA but last up to 140ms in the UK [61].

Grid-tied PV inverters are also required to inject a reactive current to support the grid when the grid voltage drops to less than 10% of the nominal level (outside the Dead band), as shown in Figure 3.5. Inverters must inject a reactive current at a rate of 2% of rated current for every one percent of grid voltage drop. For example, a reactive current of 50% of rated current is required for a grid voltage drop of 25%. A reactive current of up to100% must be possible if necessary.

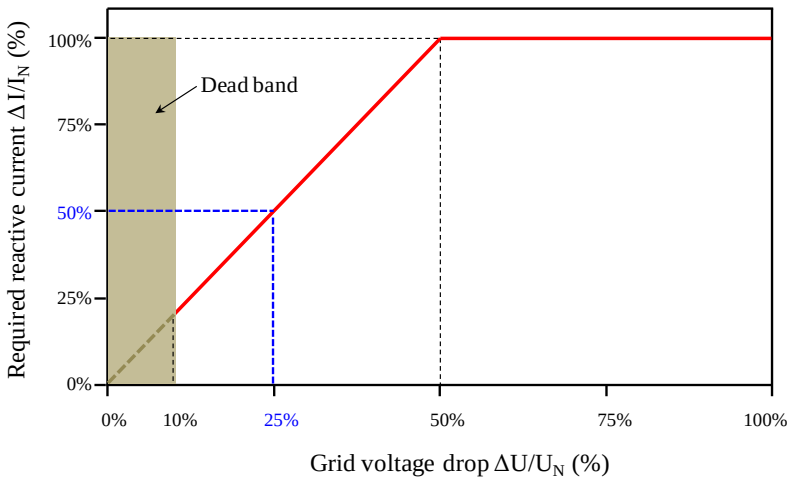


Figure 3.5 Required reactive current for a particular drop of the grid voltage level by the E.On-Netz 2006 grid code [12]

3.2.3 Islanding Prevention

Islanding is the situation when the grid-tied PV inverters continue injecting electric power from the PV cells to a subsection of the grid even if the main grid is already tripped by the utility due to fault conditions or for maintenance purposes. Islanding can be dangerous for the utility workers who may not realize that the grid section is still powered and may damage equipment due to asynchronous phase closure [24]. In order to avoid these problems, inverters are required to have a protection system to disconnect the inverters automatically from the grid when islanding is detected. This protection system is known as *anti-islanding*. The standards IEEE 1547 and UL 1741 provide the specification as follows:

- *The inverter shall detect and cease to energise the grid within 2 seconds*

There are several techniques available for islanding detection [62-65]. Most techniques utilise some combination of a sudden change in system frequency, voltage magnitude, rate of change of frequency (df/dt) and increasing rate of the active power or/and reactive power well beyond the expected nominal level.

3.3 Other Characteristics

Besides the characteristics on the PV side and grid side of the power inverters, grid-tied PV inverters are also required to have high power conversion efficiency, accurate MPP tracking and minimum costs. Details for these characteristics will be presented in the following sections.

3.3.1 High Power Conversion Efficiency

Like most power electronic devices, grid-tied PV inverters are required to operate with high efficiency at every operating point, which is at the MPP of the PV cells in this application. As the MPP of the PV cells varies depending on the levels of sun irradiance (see Section 2.5), the efficiency of the inverters operating at different levels of sun irradiance can be different. Moreover, different inverter types may require

different MPP ratings. These would lead to difficulty in comparing the efficiency of different types of grid-tied PV inverters.

The *European Efficiency* (η_{euro}) is one of the most widely used methods to calculate the efficiency of grid-tied PV inverters [12]. This method also allows efficiency of different types of grid-tied PV inverters to be compared. This method averages the efficiencies of the inverters when they operate at MPP under 5%, 10%, 20%, 30%, 50% and 100% sun irradiance; where each of a particular efficiency is weighted with the probability of seeing that sun irradiance level in the central Europe. The formula for calculating η_{euro} is shown in (3.3); where $\eta_{5\%}$, $\eta_{10\%}$, $\eta_{20\%}$, $\eta_{30\%}$, $\eta_{50\%}$ and $\eta_{100\%}$ are the efficiency of the inverter operating at MPP under 5%, 10%, 20%, 30%, 50% and 100% sun irradiance; and the numbers are the probability for those sun irradiance levels in the central Europe.

$$\eta_{euro} = 0.03\eta_{5\%} + 0.06\eta_{10\%} + 0.13\eta_{20\%} + 0.1\eta_{30\%} + 0.48\eta_{50\%} + 0.2\eta_{100\%} \qquad (3.3)$$

From (3.3), the efficiency at 50% sun irradiance has the highest contribution to the European Efficiency since this point has the highest probability of almost a half (48%) of the total probability. Inverters with efficiencies up to 98% can be achieved for sun irradiance over 25% [66]. An example of the calculation for a 94.5% European efficiency inverter is shown in Figure 3.6 [55].

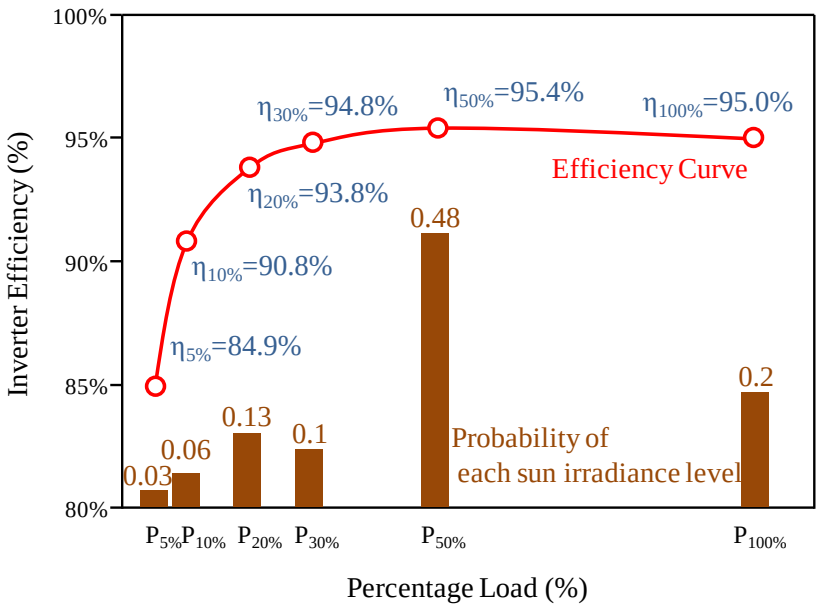


Figure 3.6 Typical efficiency curve of the 94.5% European efficiency inverter [55]

3.3.2 Accurate MPP Tracking

Grid-tied PV inverters are required to include a system called *maximum power point tracking* (MPPT) in order to ensure that the inverters always operate at the MPP of the PV cells. There are several MPPT techniques available in the literature, many of them are summarised in **Appendix A** [67]. However, among all of those techniques, the *Perturb and Observe* (P&O) and the *Incremental Conductance* (IncCond) techniques [68, 69] are the most simple and widely used MPPT techniques. These techniques are presented in the following Sections.

3.3.2.1 Perturb and Observe (P&O) Technique

The concept behind the P&O technique [68] is to adjust the operating voltage of the PV cells until the MPP is determined. The algorithm flowchart of this method is shown in Figure 3.7. This method provides the simplest algorithm and the easiest implementation. However, this method has the drawbacks in that the output power always fluctuates even in the steady state as well as having a risk of tracking in the wrong direction under rapid changes in solar irradiance levels.

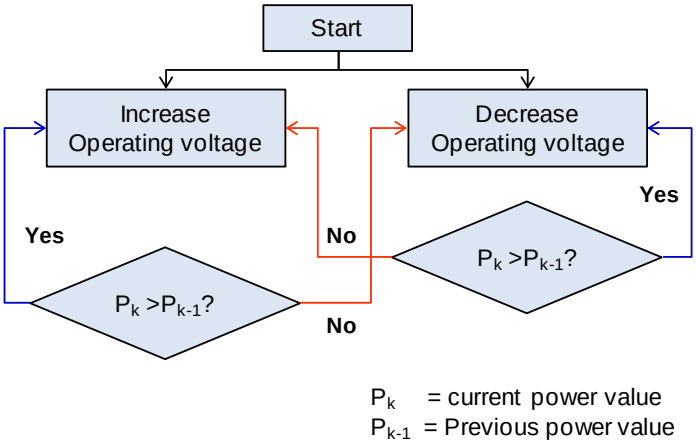


Figure 3.7 Flowchart of the Perturb and Observe algorithm [70]

3.3.2.2 Incremental Conductance (IncCond) Technique

The IncCond technique [69] takes an advantage of the fact that the slope of the power-voltage curve (dP/dV) is zero at the MPP, as shown in (3.4). The slope is positive at the left of the MPP and negative at the right of the MPP as shown in (3.5).

$$\frac{d(P)}{dv} = \frac{d(vi)}{dv} = v\frac{di}{dv} + i = 0 \tag{3.4}$$

$$\frac{di}{dv} = -\frac{i}{v} \approx -\frac{I_{pv}}{V_{pv}} \tag{3.5}$$

The flowchart of the IncCond technique is shown in Figure 3.8. The MPP is determined by comparing the instantaneous conductance (I/V) to the increment conductance (ΔI/ΔV). Once the MPP is determined, the system will maintain that operating point without any fluctuation until the change in ΔI/ΔV occurs and the system starts to search for a new MPP again. As a result, the IncCond technique solves the problems of the P&O technique by obtaining the MPP without oscillating in steady state as well as being able to withstand rapid change of sun irradiance. However, this technique is more complicate to implement than the P&O technique.

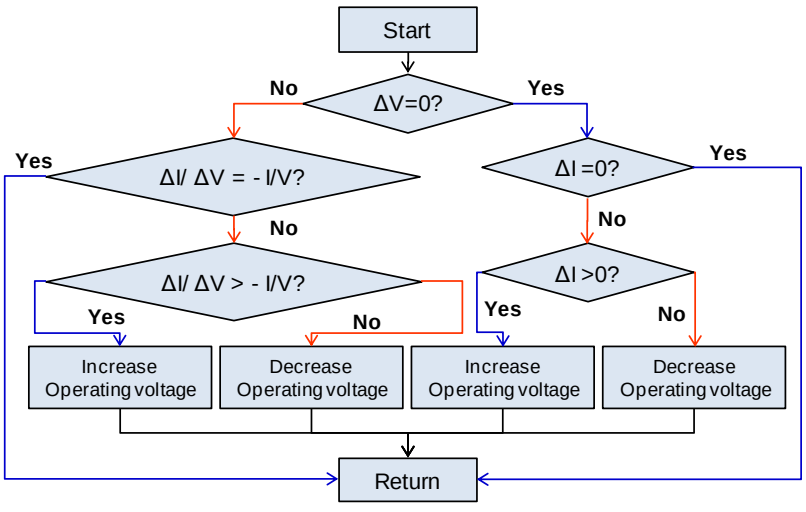


Figure 3.8 Flowchart of the Incremental Conductance algorithm [70]

3.3.3 Minimum Costs

Although the current cost of grid-tied PV inverters is not the main contributor to the total cost of grid-tied PV system (forming only 6-9% of the total cost), the cost of the inverters should be still minimised. In some countries the reduction of the inverter cost is set as a clear action plan, e.g. USA plans to achieve the inverter price of $0.25-0.3/Wp by 2020 from the present (2010) cost of $0.716/Wp [71].

The cost breakdown of a grid-tied PV inverter (Figure 3.9) shows that the cost of printed circuit boards (PCB) is the major contributor to the capital cost (31%) of the inverter, followed by the costs of production (23%), enclosure (19%), power electronics components (12%), magnetic components (10%) and test (5%) [72]. In this thesis the estimate costs of PCB, power electronic and magnetic components for different inverter types will be considered in Chapter 6.

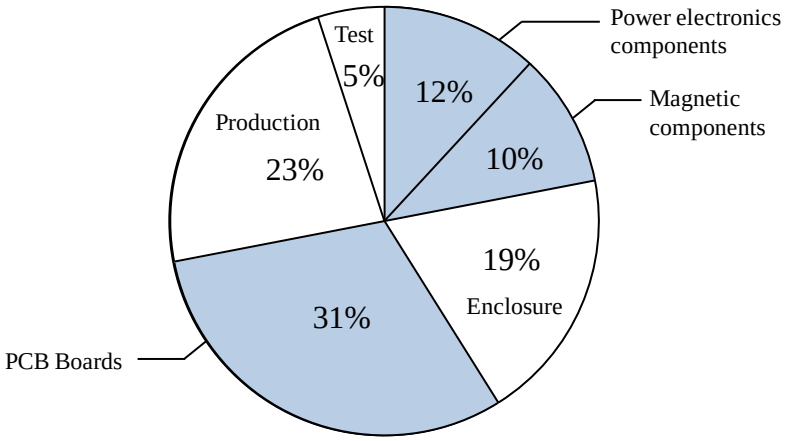


Figure 3.9 Cost breakdown of a grid-tied PV inverter [72]

Besides the aforementioned characteristics, grid-tied PV inverters should have a small size and light weight, which help to reduce the transportation and installation cost [29]. Grid-tied PV inverters should also have a long operational lifetime since most PV module manufacturers usually offer a warranty of 20-25 years on 80% of initial efficiency [6]. The electrolytic capacitors used inside the inverters are the main components that limit the lifetime of the inverters. Their operational lifetimes reduce more quickly, by the factor of power two for every increasing of ambient temperature of 11-12 ^{o}C [21].

3.4 Summary

This chapter has presented the basic required characteristics of grid-tied PV inverters. The characteristics are divided into three types: PV side characteristics, power grid side characteristics and the other characteristics.

The PV side characteristics aim to achieve the maximisation PV output power and connection compatibility between the inverter and the PV source. The inverters should always operate at the MPP, be able to operate over the whole MPP range of the PV cells, have the power rating matching to the rating of the PV cells and withstand the maximum voltage of the PV cells regardless of any variation in the ambient temperature.

The grid side characteristics are related to output power quality and safe operation complying with all relevant grid codes and standards. The inverters should not emit high levels of harmonics at the grid connection over the limits specified in the grid codes and standards (e.g. standard IEEE 1547). The inverters should provide an average power factor higher than 0.9 when operating with the output power over than 50% of the rated PV power (standard IEC 61727). The inverters should also be able to ride-through grid faults as required by the grid codes (e.g. E.On-Netz) and have the ability of islanding prevention (standards IEC 61727 and UL1741).

Inverters are also required to have high power conversion efficiency when operating at the MPP with good MPP tracking. Inverters are also required to have low costs, small size, light weight and a long operational lifetime.

These characteristics will be used in the choice of the topologies for grid-tied PV inverters presented in Chapters 4 and 5 as well as in an evaluation of the performance of the topologies as presented in Chapters 6 and 8.

Chapter 4

Three-Phase Transformerless Grid-Tied PV Inverter Topologies under Investigation

This chapter presents a review of transformerless inverter topologies used for three-phase grid-tied photovoltaic (PV) applications. The topologies under investigation are selected from those currently used or already presented in the published papers. Six inverter topologies are examined, which are the voltage source inverter (VSI), the current source inverter (CSI), the two-stage VSI with a boost converter, the two-stage CSI with a buck converter, the voltage fed Z-source inverter and the current fed Z-source inverter. Details of the circuit configuration, modulation and control methodology and typical passive component design procedure for each of these topologies are presented.

4.1 Introduction

The voltage source inverter (VSI) and the current source inverter (CSI) are the very basic power converter topologies presented in the literature that can convert DC power into AC power in a single conversion stage. However, these topologies have some shortcomings when required to operate with a large DC voltage variation source such as a PV array. Below, the choice between the various inverter topologies suitable for connection of PV arrays to the grid is discussed.

The VSI is a DC-to-AC voltage step down converter [73]. This topology cannot operate with a low PV voltage since the topology requires the PV voltage to be higher than the peak line-to-line grid voltage in order to enable power to be transferred to the grid. Therefore, in practice a DC-to-DC boost converter (also called a boost converter) is usually added to allow the resulting two-stage VSI to step up a low PV

voltage to the required level [74]. In contrast, the CSI is a DC-to-AC voltage step up converter [75]. This topology can operate over a wide PV voltage range (down to zero) without the need of any additional components. However, the PV voltage must be limited upwards to be less than 0.866 of the peak line-to-line grid voltage. Therefore, an additional DC-to-DC buck converter (also referred as a buck converter) could be added to the CSI topology in order to step down a high PV voltage when a high voltage PV array is used. The addition of the boost or buck converters however adds cost, complexity and losses to these inverter topologies, but has the advantage that it allows the stabilisation of the DC-link voltage and therefore facilitates a better usage of the VSI/CSI switches. Alternatively, Z-source inverters (ZSI) are types of converter topologies that can both step up and step down the voltage from the DC side to the AC side due to the use of an additional DC impedance circuit [26]. This means that the ZSI is able to operate over a wide DC voltage range of the PV source in order to convert and feed power into the grid. Two basic configurations of ZSI topologies have been proposed: the voltage fed ZSI and the current fed ZSI. One major drawback of the ZSI topologies is that these topologies are subject to high voltage and current stress on their circuit components, especially the switching devices [35, 36]. This may require a careful design or the use of components with higher voltage and current ratings, which can be more expensive.

Table 4.1 summarises the list of inverter topologies that are investigated in this chapter. It is noted that in Chapter 5, a new candidate topology, named *the CSI with series AC capacitors*, which is a modified topology of the CSI will be proposed. Chapter 6 will evaluate the performance of the proposed topology in comparison with the topologies presented in this chapter.

Inverter Topology	Symbol
Voltage Source Inverter	VSI
Current Source Inverter	CSI
Two-stage VSI with a boost converter	VSI+Boost
Two-stage CSI with a buck converter	CSI+Buck
Voltage fed Z-Source Inverter	ZSI-V
Current fed Z-Source Inverter	ZSI-I

Table 4.1 Three-phase grid-tied PV inverter topologies under investigation

4.2 Circuit Configurations

4.2.1 Voltage Source Inverter

Figure 4.1 illustrates the circuit configuration of a standard three-phase voltage source inverter (VSI). This topology is the most commonly used inverter topology for grid interfacing applications [76]. The circuit consists of six unidirectional switches having fast recovery diodes connected in anti-parallel to provide reverse conduction of the AC current for the situation when the opposite switch is off. The topology is fed from a DC voltage source connected in parallel with a DC-link voltage smoothing capacitor C_{dc}. The switching devices are arranged such that each AC output phase can be connected to either the upper or lower DC-link voltage. The inductive filters L_f are placed on the AC side to decouple the inverter and the grid and to smooth the current ripple created by the inverter switching. A diode is usually placed in series with the PV source to avoid reverse PV current which is likely to occur during night.

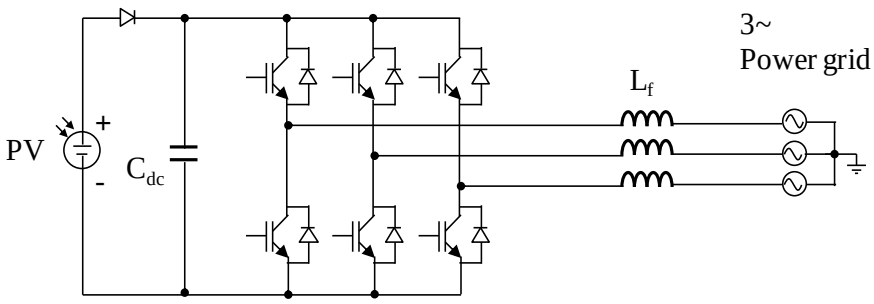


Figure 4.1 Circuit configuration of a standard three-phase VSI

4.2.2 Current Source Inverter

Figure 4.2 shows the circuit configuration of a standard three-phase current source inverter (CSI). Six unidirectional switches connected in series with reverse voltage blocking diodes are used in this topology. These diodes are not necessary if reverse blocking switches (GTOs or IGBTs) are used to construct the power circuit. The topology is fed from either a DC current source or a DC voltage source connected in series with a DC-link inductor L_{dc}. Filtering capacitors C_f are placed on the AC side to

smooth the grid voltage ripple caused by the rapid change in the converter's current (*di/dt*) caused by the circuit commutation of the constant DC-link current. The AC inductors, L_f, are added to smooth the AC line current ripple caused by the switching of the inverter.

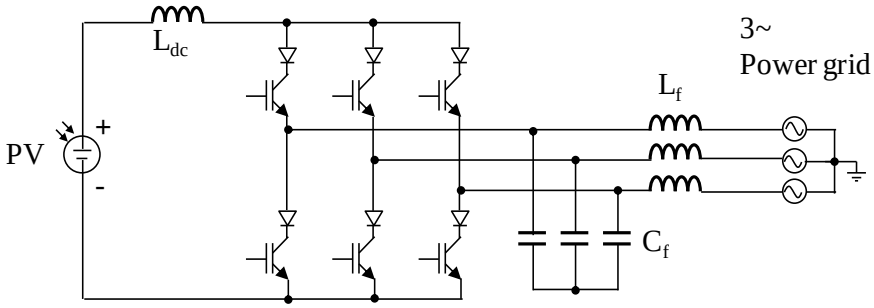


Figure 4.2 Circuit configuration of a standard three-phase CSI

4.2.3 Two-Stage VSI with a Boost Converter

Figure 4.3 shows the circuit configuration of the three-phase, two-stage VSI with a boost converter (VSI+Boost) [77]. A boost converter is added to the VSI topology in order to step up and stabilise the DC-link voltage level when the PV voltage is insufficiently low. The boost converter consists of a diode, a switch and an inductor L_{boost}. The duty time of the boost switch controls the voltage boosting ratio: the higher the duty time, the higher the DC side voltage that is boosted when compared to the PV voltage. When the boost switch is turned on, the PV source is shorted via the boost inductance and the current in the inductor increases and stores energy. When the boost switch is turned off, the DC voltage produced by the inductance (*-Ldi/dt*) tops up the PV voltage and then all this energy is transferred, through the diode to the boosted DC part as the current level in the inductor decreases. The diode controls the current direction to flow from the PV source to the grid only, which is used to prevent reverse conduction through the PV array. The size of the boost inductor L_{boost} depends on the smoothing requirement of the input PV current but should be large enough to provide continuous conduction current. Section 4.4.3 and Section 4.5 contain more details for the operation and component design for this topology.

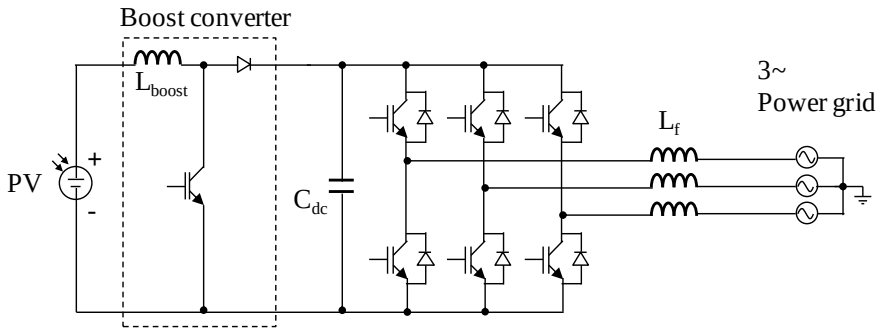


Figure 4.3 Circuit configuration of the three-phase, two-stage VSI with a boost converter

4.2.4 Two-Stage CSI with a Buck Converter

Figure 4.4 shows the circuit configuration of the three-phase, two-stage CSI with a buck converter (CSI+Buck) [77]. A buck converter is added into the CSI topology in order to step down the DC-link voltage level during the period where the PV voltage is above the voltage transfer limit of the CSI for a particular given grid voltage level. A buck converter consists of a diode, a switch and an inductor L_{dc} which is shared with the CSI circuit. The duty time of the switch controls the voltage reduction ratio: the lower the duty cycle, the lower the DC side voltage that is reduced when compared to the PV voltage. The diode provides a freewheeling path for the operating current when the switch is off. The inductor L_{dc} should also be large enough to provide a continuous conduction current. More details for the operation and component design for this topology are presented in Section 4.4.4 and Section 4.5.

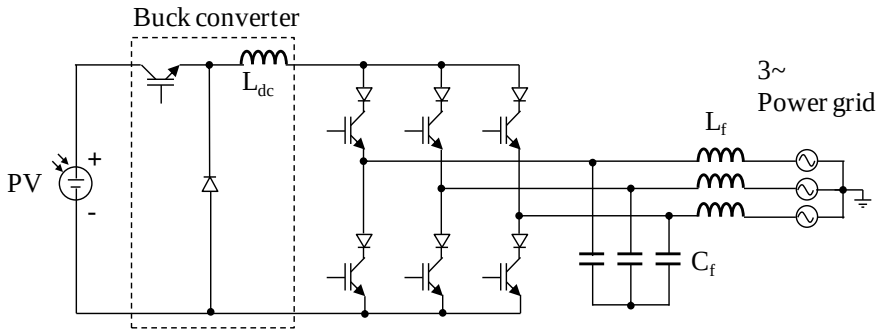


Figure 4.4 Circuit configuration of the three-phase, two-stage CSI with a buck converter

4.2.5 Voltage Fed Z-Source Inverter

A voltage fed Z-source inverter, or a ZSI-V, is a modified topology of the VSI [35]. An X-shaped impedance circuit is added into the DC side of the VSI as shown in Figure 4.5. The X-shaped impedance circuit consists of two DC inductors (L_1 and L_2), two DC capacitors (C_1 and C_2) and a diode. The value of L_1 is equal to L_2 and the value of C_1 is equal to C_2 for symmetry. The diode is connected in series with the PV array to prevent reverse conduction current through the PV array. This impedance circuit allows the ZSI-V topology to be able to operate with a shoot-through state (short-circuit of the DC side of the inverter), which is a forbidden switching state for the standard VSI because a very high current powered by the DC-link capacitor will occur and damage the switching devices. In contrast, the voltage fed ZSI topology utilises the shoot-through switching states to provide the DC-to-AC voltage boosting property (similar to a boost converter) by the control of the duty time of the shoot-through switching state. More details for the operation and component design for the ZSI-V topology are presented in Section 4.4.5 and Section 4.5.

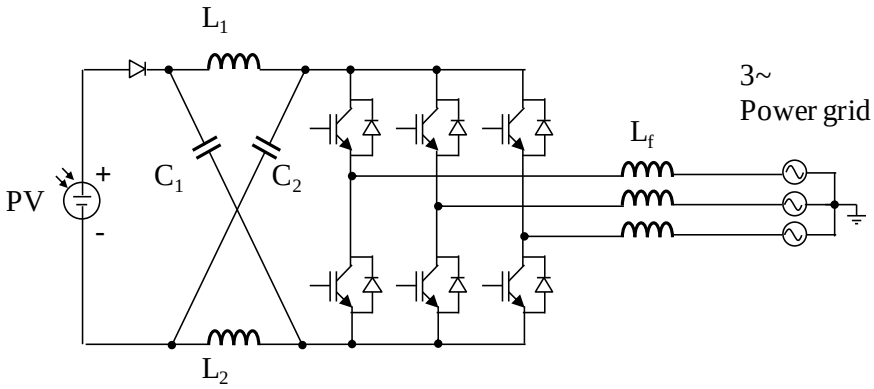


Figure 4.5 Circuit configuration of the three-phase, voltage fed ZSI

4.2.6 Current Fed Z-Source Inverter

A current fed Z-source inverter, or a ZSI-I, is a modified topology of the CSI [35]. An X-shaped impedance circuit is added into the DC side of the CSI as shown in Figure 4.6. The impedance circuit consists of two DC inductors (L_3 and L_4), two DC capacitors (C_3 and C_4) and a diode. The value of L_3 is equal to L_4 and the value of C_3 is equal to C_4 for symmetry. The diode is connected in parallel with the PV array to provide a freewheeling path for the current of the current source if the DC side of the

inverter is opened. This impedance circuit allows the ZSI-I topology to be able to operate with an open-circuit state (open-circuit of the DC side of the inverter), which is a forbidden switching state for the standard CSI since a very high voltage will occur and damage the switching devices. In contrast, the current fed ZSI topology utilises the open-circuit switching states to provide the DC-to-AC voltage reduction property (similar to a buck converter) by the control of the duty time of the open-circuit switching state. More details for the operation and component design for the ZSI-I topology are presented in Section 4.4.6 and Section 4.5.

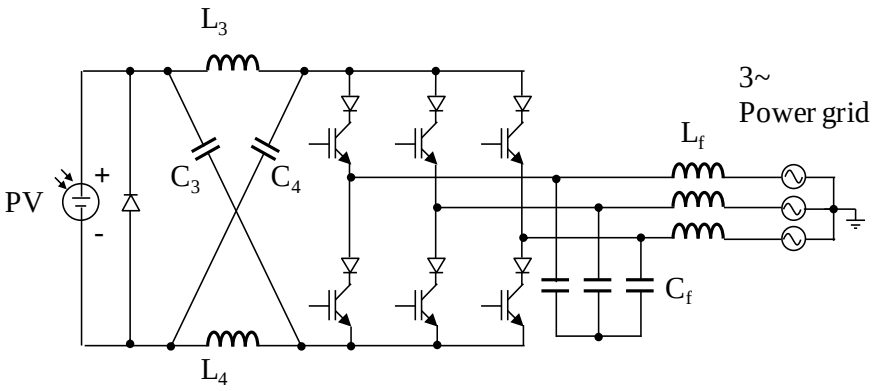


Figure 4.6 Circuit configuration of the three-phase, current fed ZSI

4.3 Modulation Strategies

In order to produce the desired AC sinusoidal waveforms at the grid side, the switching of the devices in the power converters must be modulated in a suitable manner [73]. Several modulation techniques can be used for three-phase power converters [73, 78-82]. However, among those techniques the *Space Vector Modulation* (SVM) [83, 84] seems to be the most popular technique. This would be because the SVM allows a three-phase system to be analysed as a whole instead of each individual phase. The SVM is also able to operate in real-time and digital-based modulation which allows the SVM to have a fast on-line calculation using a software-based controller (e.g. a microprocessor or a digital signal processor) [85]. This section highlights the modulation techniques used by each of the different circuit topologies previously introduced. The principle of the SVM is firstly described and then details of the three modulation types used for the VSI-based topologies, CSI-based topologies and ZSI topologies are presented: VSI modulation, CSI modulation and ZSI modulation.

4.3.1 Principle of the Space Vector Modulation

Any balanced three-phase, sinusoidal time-varies waveforms (x_a(t), x_b(t) and x_c(t)) can be represented by only a single rotating vector $\overrightarrow{x_r}$, as defined by (4.1).

$$\overrightarrow{x_r} = \frac{2}{3}[x_a(t) + \vec{a} \cdot x_b(t) + \vec{a}^2 \cdot x_c(t)] \quad ; \text{where } \vec{a} = e^{j\frac{2\pi}{3}} \text{ and } \vec{a}^2 = e^{j\frac{4\pi}{3}} \tag{4.1}$$

This vector $\overrightarrow{x_r}$ rotates on a stationary complex plane (referred as a α-β space vector plane) with the same angular speed (ω_o) as the three-phase waveforms. The magnitude and direction of the vector $\overrightarrow{x_r}$ change depending on the instantaneous values of the three-phase waveforms, which can be obtained from the vectorial summation of the three phasors $\overrightarrow{x_a}$, $\overrightarrow{x_b}$ and $\overrightarrow{x_c}$ as shown in Figure 4.7. The phasor $\overrightarrow{x_a}$ is usually aligned with the axis and the other two phasors $\overrightarrow{x_b}$ and $\overrightarrow{x_c}$ are placed with 120 degrees apart in the same vector plane.

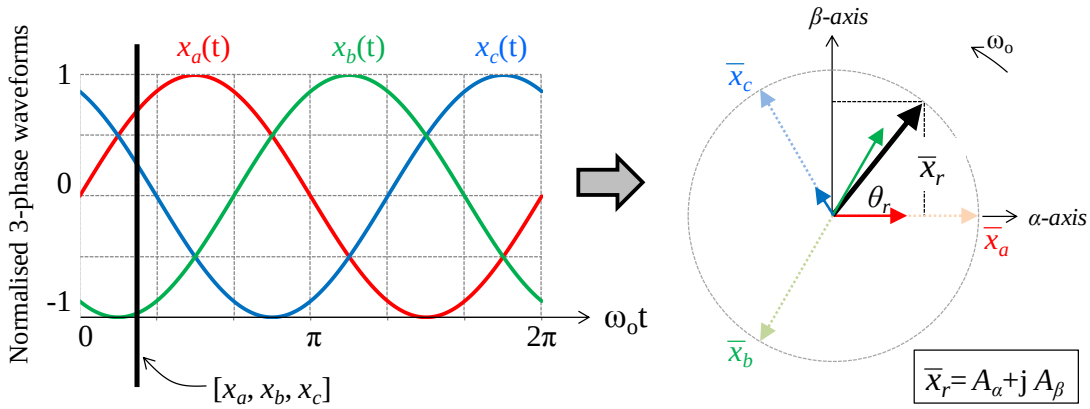


Figure 4.7 Transformation process between the three-phase waveforms and the representative vector rotating on the α-β space vector plane

As a result, the vector $\overrightarrow{x_r}$ can be derived in terms of the two elements of the α-β plane ($\overrightarrow{x_r} = A_\alpha + jA_\beta$) using (4.2). Alternatively, if the rotating space vector plane (usually referred as a direct-quadrature or d-q plane) is used, the vector $\overrightarrow{x_r}$ can also be derived in terms of the two elements of the d-q vector plane ($\overrightarrow{x_r} = A_d + jA_q$) using (4.3).

$$\begin{bmatrix} A_\alpha \\ A_\beta \end{bmatrix} = \frac{2}{3}\begin{bmatrix} 1 & \frac{-1}{2} & \frac{-1}{2} \\ 0 & \frac{\sqrt{3}}{2} & \frac{-\sqrt{3}}{3} \end{bmatrix}\begin{bmatrix} x_a \\ x_b \\ x_c \end{bmatrix} \tag{4.2}$$

$$\begin{bmatrix} A_d \\ A_q \end{bmatrix} = \frac{2}{3}\begin{bmatrix} \cos(\theta_r) & \cos\left(\theta_r - \frac{2\pi}{3}\right) & \cos\left(\theta_r + \frac{2\pi}{3}\right) \\ -\sin(\theta_r) & -\sin\left(\theta_r - \frac{2\pi}{3}\right) & -\sin\left(\theta_r + \frac{2\pi}{3}\right) \end{bmatrix}\begin{bmatrix} x_a \\ x_b \\ x_c \end{bmatrix} \quad (4.3)$$

The SVM utilises the advantage of the above knowledge to select the suitable switching states and calculate the duty time for each of those selected switching states for the inverter. This can be achieved using the procedure shown in Figure 4.8.

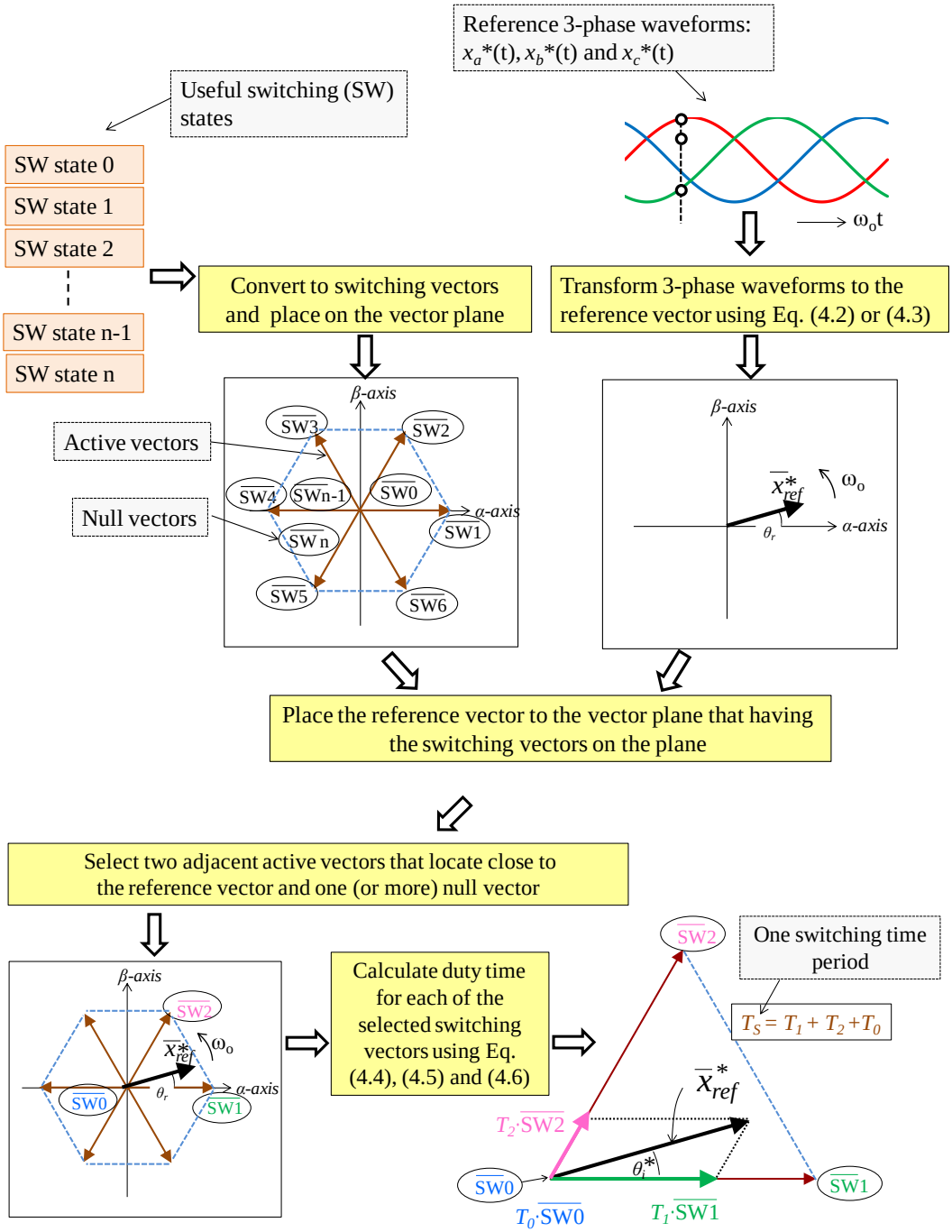


Figure 4.8 Procedure to select the switching states and calculate the duty time for each of the selected switching states in the SVM

The procedure shown in Figure 4.8 is described below:

- Convert all the switching states that can be used for a particular inverter topology to the switching vectors, which can be active switching vectors or null switching vectors. These vectors have the following characteristics:
    - The active switching vectors allow the power to be transferred between the DC side and the AC side. These vectors have identical magnitudes and are located by 60 degrees from each other on the space vector plane. These vectors split the vector plane into six sectors.
    - The null switching vectors do not allow any power to be transferred between the DC side and the AC side. These vectors have no magnitude and no specific direction.
- Transform the reference three-phase waveforms (x^*_a(t), x^*_b(t) and x^*_c(t)) into the reference rotating vector $\vec{x}^*_{ref}$ using (4.2) or (4.3). Then place the vector $\vec{x}^*_{ref}$ on the vector plane that already contains the switching vectors on the plane.
- The operating active switching vector is selected from the two adjacent active vectors that create the sector where the reference vector $\vec{x}^*_{ref}$ locates. The null switching vector that has the minimum change of switching states compared to the selected active vectors is usually selected in order to minimise switching losses.
- Calculate duty time for each of the selected switching vectors using (4.4), (4.5) and (4.6); where the parameters T_1, T_2 and T_o are the duty times for the first active vectors, the second active vectors and the null vector, T_s is the switching time period, m^* is the modulation index (having a value between 0 and 1) and θ_i^* is the angle of the reference vector within the sector (having a value between 0 and 60 degrees).

$$T_1 = m^* T_s \sin\left(\frac{\pi}{3} - \theta_i^*\right) \quad ; \text{for } 0 \leq \theta_i^* < \pi/3 \tag{4.4}$$

$$T_2 = m^* T_s \sin\left(\theta_i^*\right) \quad ; \text{for } 0 \leq \theta_i^* < \pi/3 \tag{4.5}$$

$$T_0 = T_s - T_1 - T_2 \tag{4.6}$$

After the operating switching vectors and their duty times are determined, these switching vectors have to be sequenced and operate for the calculated duty times. These switching vectors can be split and sequenced in different patterns as far as the total duty time for each of the switching vectors is still equal to the calculated value. This creates a number of possible switching sequences. In this thesis the criteria used to form the switching sequence are:

- Only the minimum number of the switches (up to two switches) is allowed to be switched (on and/or off) per one vector transition in order to minimise switching losses.
- The first and the last vectors of the switching sequence in one switching period must be the same in order to provide the continuity of the switching sequence for the next switching cycle when repeated.

The SVM techniques and the switching sequences based on the above criteria applied for the different types of the inverter topologies under study are presented in the following sections (Sections 4.3.2 to 4.3.4).

4.3.2 VSI Modulation

The techniques described in this section are equally applicable to both the standard VSI and the two-stage VSI with a boost converter. The switching devices used in these inverter topologies must be modulated such that a short circuit of the DC-link voltage source must never occur; otherwise, a high current (*shoot-through*) that is powered by the DC-link capacitor will occur and damage the switching devices. In practical terms, this means that the upper switch and lower switch of any inverter leg must never turn on at the same time, which also means that the "on" and "off" state of an inverter leg can be represented by "1" or "0" showing the state of the upper switch. This results in a total of eight switching states that are allowable for the VSI modulation as shown in Figure 4.9.

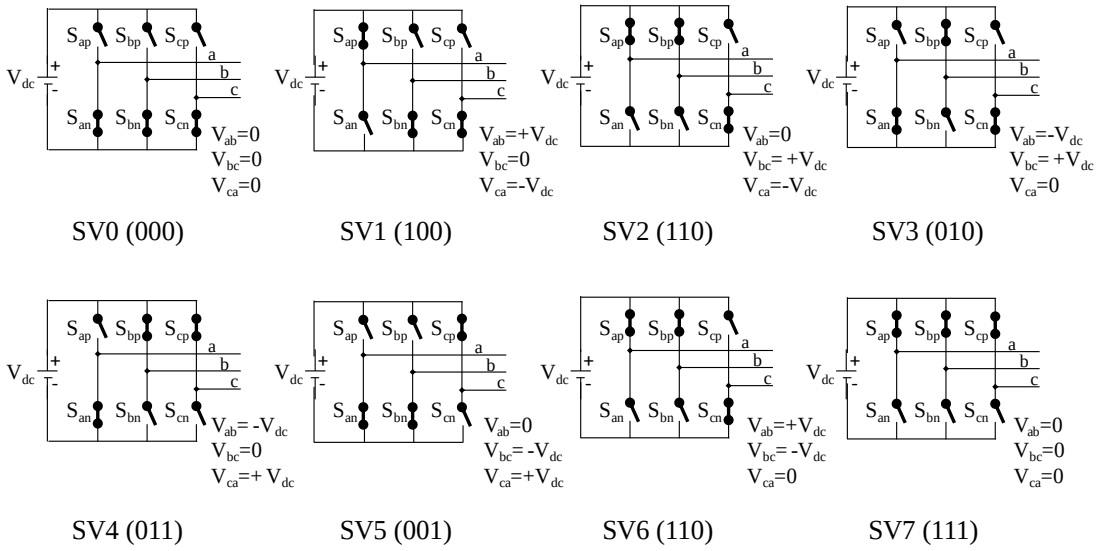


Figure 4.9 Eight allowable switching states used in the VSI modulation

These eight switching states are classified into two groups: *active switching states* (SV1 to SV6) and *null switching states* (SV0 and SV7). The active switching states allow the power to be transferred between the DC voltage source (V_{dc}) and the grid whilst the null switching states cause a short circuit of the AC side and an open-circuit of the DC side and thus do not allow any power to be transferred. For example, the active switching state SV1 will apply a voltage of $+V_{dc}$ and $-V_{dc}$ to the grid line *ab* and line *ca*, but the null switching state SV0 will connect all the grid lines to the lower DC-link voltage rail and thus no power can be transferred between the DC side and the AC side.

In order to operate with the SVM technique, these eight allowable switching states (SV0 to SV7) are converted to the switching vectors: the active switching states SV1 to SV6 are converted to active vectors $\overrightarrow{SV1}$ to $\overrightarrow{SV6}$ and the null switching states SV0 and SV7 are converted to null vectors $\overrightarrow{SV0}$ and $\overrightarrow{SV7}$. These switching vectors have characteristics as shown in Table 4.2. All of the active vectors ($\overrightarrow{SV1}$ to $\overrightarrow{SV6}$) have identical magnitudes of $(2/3)\cdot V_{dc}$ whilst all of the null vectors ($\overrightarrow{SV0}$ and $\overrightarrow{SV7}$) have no magnitude. The active vector $\overrightarrow{SV1}$ is aligned with the α-axis and all the other active vectors have 60 degrees displacement from each other whilst the null vectors have no specific direction. The active vectors split the vector plane into six different sectors (Sector 1 to Sector 6) as shown in Figure 4.10.

Switching Vector	Switching Code	Vector Type	Magnitude	Direction	PWM Output		
					V_{ab}	V_{bc}	V_{ca}
$\overrightarrow{SV0}$	[000]	Null	0	-	0	0	0
$\overrightarrow{SV1}$	[100]	Active	$(2/3)\cdot V_{dc}$	e^{j0}	$+V_{dc}$	0	$-V_{dc}$
$\overrightarrow{SV2}$	[110]	Active	$(2/3)\cdot V_{dc}$	$e^{j\pi/3}$	0	$+V_{dc}$	$-V_{dc}$
$\overrightarrow{SV3}$	[010]	Active	$(2/3)\cdot V_{dc}$	$e^{j2\pi/3}$	$-V_{dc}$	$+V_{dc}$	0
$\overrightarrow{SV4}$	[011]	Active	$(2/3)\cdot V_{dc}$	$e^{j\pi}$	$-V_{dc}$	0	$+V_{dc}$
$\overrightarrow{SV5}$	[001]	Active	$(2/3)\cdot V_{dc}$	$e^{j4\pi/3}$	0	$-V_{dc}$	$+V_{dc}$
$\overrightarrow{SV6}$	[101]	Active	$(2/3)\cdot V_{dc}$	$e^{j5\pi/3}$	$+V_{dc}$	$-V_{dc}$	0
$\overrightarrow{SV7}$	[111]	Null	0	-	0	0	0

Table 4.2 Switching vectors and their characteristics used for the SVM-VSI

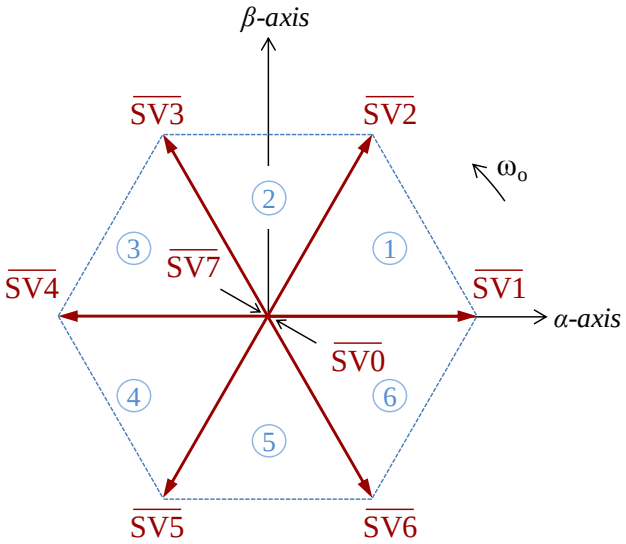


Figure 4.10 Space vector plane for the SVM-VSI

For the given reference voltage vector $\vec{V}^*_{ref}$ and with the use of the SVM procedure described in Section 4.3.1, the switching vectors and the duty times for each sector used in the SVM-VSI will be determined as summarised in Table 4.3. The parameter m_v refers to the VSI modulation index which is the ratio of the peak line-to-line voltage seen at the AC side of the inverter ($|V_{vsi}|$) to the peak DC-link voltage seen at the DC side of the inverter ($\hat{V}_{dc}$) as shown in (4.7).

$$m_v = \frac{|V_{vsi}|}{\hat{V}_{dc}} \qquad ; 0 < m_v \leq 1 \tag{4.7}$$

Sector	Selected Switching Vectors		Duty Time
	Active vectors	Null vectors	
1	$\overrightarrow{SV1}$, $\overrightarrow{SV2}$	$\overrightarrow{SV0}$, $\overrightarrow{SV7}$	$T_1 = m_v T_s \sin(\frac{\pi}{3} - \theta_i^*)$ $T_2 = m_v T_s \sin(\theta_i^*)$ $T_0 = T_s - T_1 - T_2$; where $0 \leq \theta_i^* < \pi/3$ and $0 < m_v \leq 1$
2	$\overrightarrow{SV2}$, $\overrightarrow{SV3}$	$\overrightarrow{SV0}$, $\overrightarrow{SV7}$	
3	$\overrightarrow{SV3}$, $\overrightarrow{SV4}$	$\overrightarrow{SV0}$, $\overrightarrow{SV7}$	
4	$\overrightarrow{SV4}$, $\overrightarrow{SV5}$	$\overrightarrow{SV0}$, $\overrightarrow{SV7}$	
5	$\overrightarrow{SV5}$, $\overrightarrow{SV6}$	$\overrightarrow{SV0}$, $\overrightarrow{SV7}$	
6	$\overrightarrow{SV6}$, $\overrightarrow{SV1}$	$\overrightarrow{SV0}$, $\overrightarrow{SV7}$	

Table 4.3 Switching vectors and duty times used in the SVM-VSI

By applying the criteria used to form the switching sequence that have been presented in Section 4.3.1, the seven-segment switching sequence (referred as a *double-sided symmetrical switching sequence*) is used to operate over one switching time period for the VSI modulation. For example, the sequence $\overrightarrow{SV0} - \overrightarrow{SV1} - \overrightarrow{SV2} - \overrightarrow{SV7} - \overrightarrow{SV2} - \overrightarrow{SV1} - \overrightarrow{SV0}$ (which has a switching code of 000-100-110-111-110-100-000) is used when the reference vector $\vec{V}_{ref}^*$ is located in Sector 1. This switching sequence allows only two switches to turn on and off per a vector transition whilst having the vector $\overrightarrow{SV0}$ to be the first and the last vectors of the sequence as shown in Figure 4.11. The similar switching sequences can be applied for the other sectors (Sector 2 to Sector 6) using Table 4.4.

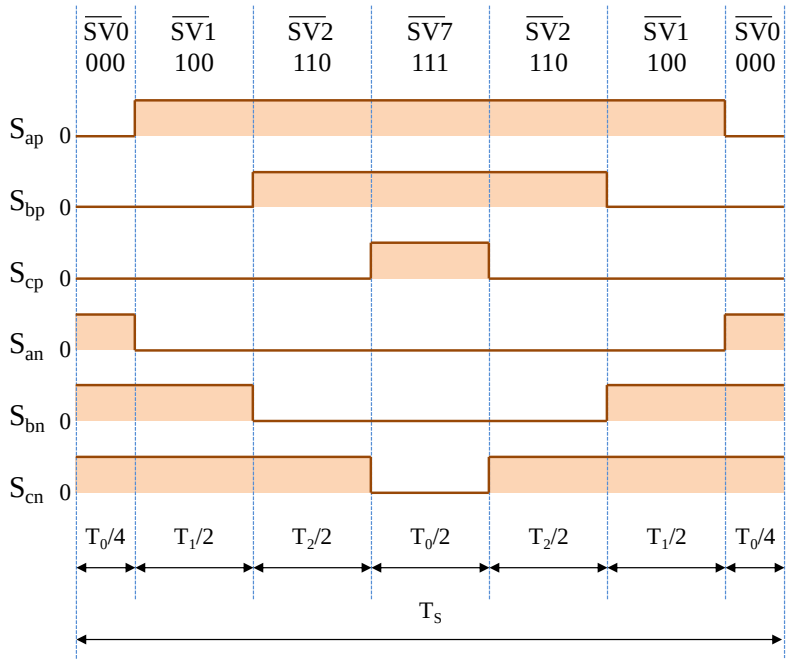


Figure 4.11 Double-sided symmetrical switching sequence of the VSI modulation over one switching period when the reference vector is located in the Sector 1

Sector	Double-sided Symmetrical Switching Sequence for SVM-VSI						
1	$\overrightarrow{SV0}$	$\overrightarrow{SV1}$	$\overrightarrow{SV2}$	$\overrightarrow{SV7}$	$\overrightarrow{SV2}$	$\overrightarrow{SV1}$	$\overrightarrow{SV0}$
	000	100	110	111	110	100	000
2	$\overrightarrow{SV7}$	$\overrightarrow{SV2}$	$\overrightarrow{SV3}$	$\overrightarrow{SV0}$	$\overrightarrow{SV3}$	$\overrightarrow{SV2}$	$\overrightarrow{SV7}$
	111	110	010	000	010	110	111
3	$\overrightarrow{SV0}$	$\overrightarrow{SV3}$	$\overrightarrow{SV4}$	$\overrightarrow{SV7}$	$\overrightarrow{SV4}$	$\overrightarrow{SV3}$	$\overrightarrow{SV0}$
	000	010	011	111	011	010	000
4	$\overrightarrow{SV7}$	$\overrightarrow{SV4}$	$\overrightarrow{SV5}$	$\overrightarrow{SV0}$	$\overrightarrow{SV5}$	$\overrightarrow{SV4}$	$\overrightarrow{SV7}$
	111	011	001	000	001	011	111
5	$\overrightarrow{SV0}$	$\overrightarrow{SV5}$	$\overrightarrow{SV6}$	$\overrightarrow{SV7}$	$\overrightarrow{SV6}$	$\overrightarrow{SV5}$	$\overrightarrow{SV0}$
	000	001	101	111	101	001	000
6	$\overrightarrow{SV7}$	$\overrightarrow{SV6}$	$\overrightarrow{SV1}$	$\overrightarrow{SV0}$	$\overrightarrow{SV1}$	$\overrightarrow{SV6}$	$\overrightarrow{SV7}$
	111	101	100	000	100	101	111

Table 4.4 Double-sided symmetrical switching sequences for each sector of the SVM-VSI

Additionally, in order to avoid a shoot-through condition, a delay time called *dead time* is added to the rising edge of the gate signal for the incoming switch. This is to ensure that the outgoing switch is completely turned off before the incoming switch in the same inverter leg can conduct. However, the added dead time will shorten or lengthen the gate signal pulses (depending on the direction of the current). Therefore, if this distortion is not compensated, the implementation of the dead time in the VSI will cause AC current waveform distortion and degrade the VSI capability to operate at very low and at near maximum DC-to-AC voltage transfer ratio [86].

4.3.3 CSI Modulation

The techniques described in this section can be used for both the standard CSI and the two-stage CSI with a buck converter. The switching devices used for these inverter topologies must be modulated in order to never open circuit the DC-link current source; otherwise, a high voltage (L*di/dt) will result and damage the switches. In practical terms, one of the upper switches and one of the lower switches, must be always turned on in order to always provide the path for the circulating current. This results in a total of nine switching states that are allowable for the CSI modulation as shown in Figure 4.12.

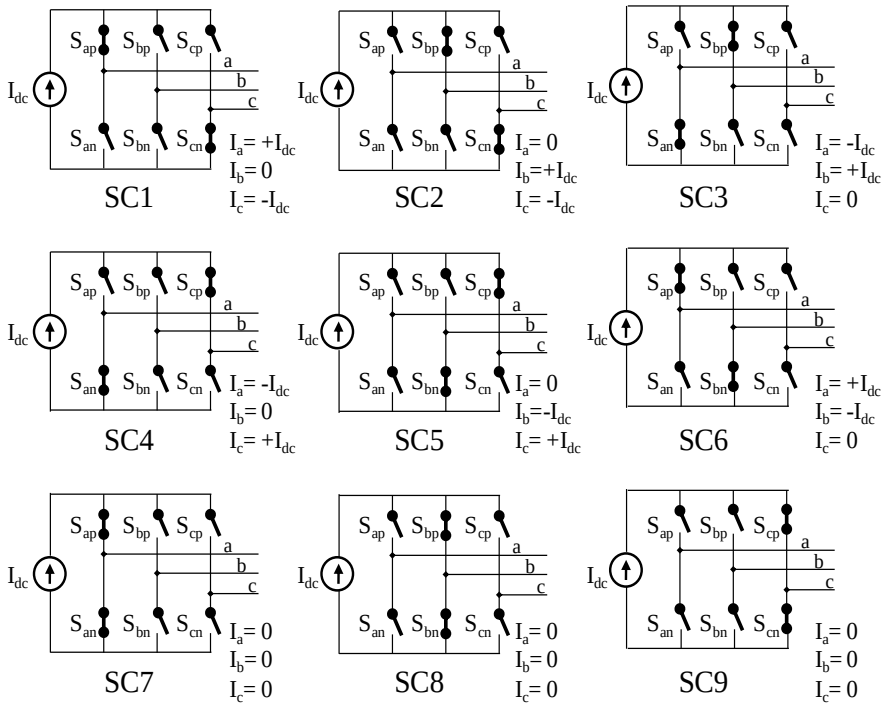


Figure 4.12 Nine allowable switching states used in the CSI modulation

Similar to the VSI modulation, the nine allowable switching states for the CSI modulation are classified into two groups: *active switching states* (SC1 to SC6) and *null switching states* (SC7 to SC9). The active switching states allow the power to be transferred between the DC current source (I_{dc}) and the grid whilst the null states causes a short circuit of the DC source via the DC-link inductance and thus do not allow any power to be transferred. For example, the active switching state SC1 will apply a DC current of $+I_{dc}$ to the grid phase *a* and $-I_{dc}$ to the grid phase *c*, whilst the null state SC0 will cause a short circuit of the DC current source and therefore no power can be transferred between the DC side and the AC side.

In order to operate with the SVM technique, the active switching states SC1 to SC6 are converted to the active vectors $\overrightarrow{SC1}$ to $\overrightarrow{SC6}$ and the switching states SC7, SC8 and SC9 to the null vectors $\overrightarrow{SC7}$, $\overrightarrow{SC8}$ and $\overrightarrow{SC9}$. These switching vectors have the characteristics as shown in Table 4.5. The first and second letters used in the switching codes indicate the location of the "on" switches for the upper and lower switches respectively, e.g. the switching code [ac] means that the switch S_{ap} and switch S_{cn} are on (see Figure 4.12).

Switching Vector	Switching Code	Vector Type	Amplitude	Direction	PWM Output		
					I_a	I_b	I_c
$\overrightarrow{SC1}$	[ac]	Active	(2/3)·I_{dc}	$e^{j\pi/6}$	+I_{dc}	0	-I_{dc}
$\overrightarrow{SC2}$	[bc]	Active	(2/3)·I_{dc}	$e^{j\pi/2}$	0	+I_{dc}	-I_{dc}
$\overrightarrow{SC3}$	[ba]	Active	(2/3)·I_{dc}	$e^{j5\pi/6}$	-I_{dc}	+I_{dc}	0
$\overrightarrow{SC4}$	[ca]	Active	(2/3)·I_{dc}	$e^{j7\pi/6}$	-I_{dc}	0	+I_{dc}
$\overrightarrow{SC5}$	[cb]	Active	(2/3)·I_{dc}	$e^{j3\pi/2}$	0	-I_{dc}	+I_{dc}
$\overrightarrow{SC6}$	[ab]	Active	(2/3)·I_{dc}	$e^{j11\pi/6}$	+I_{dc}	-I_{dc}	0
$\overrightarrow{SC7}$	[aa]	Null	0	-	0	0	0
$\overrightarrow{SC8}$	[bb]	Null	0	-	0	0	0
$\overrightarrow{SC9}$	[cc]	Null	0	-	0	0	0

Table 4.5 Switching vectors and their characteristics used for the SVM-CSI

From Table 4.5, all of the active vectors ($\overrightarrow{SC1}$ to $\overrightarrow{SC6}$) have identical magnitudes of (2/3)·I_{dc} whilst all of the null vectors ($\overrightarrow{SC7}$, $\overrightarrow{SC8}$ and $\overrightarrow{SC9}$) have no magnitude. The active vectors have 60 degrees displacement from each other whilst the null vectors have no specific direction. The active vectors split the vector plane into six different sectors (Sector 1 to Sector 6) as shown in Figure 4.13. As the AC currents obtained from the CSI modulation will be displaced by 30 degrees leading when using the same reference vector plane as the SVM-VSI, all switching vectors of the SVM-CSI therefore are compensated by 30 degrees leading in order to allow the CSI modulation to be analysed in the same way as the VSI modulation.

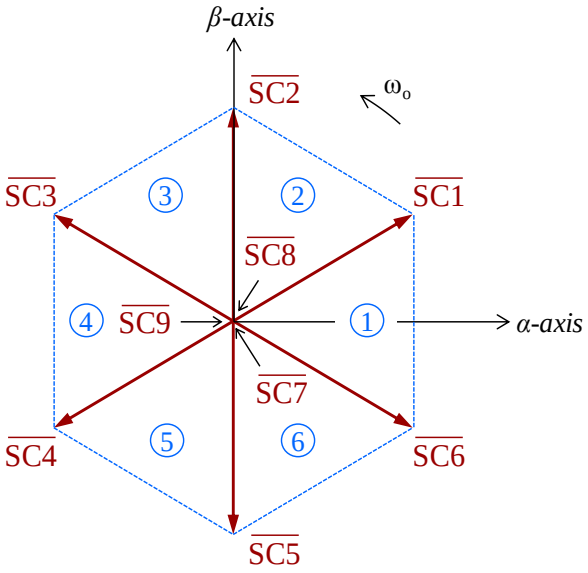


Figure 4.13 Space vector plane for the SVM-CSI

For the given reference current vector $\vec{I}^*_{ref}$ and with the use of the SVM technique described in Section 4.3.1, the switching vectors and the duty times for each sector used in the SVM-CSI will be determined as summarised in Table 4.6. The parameter m_i refers to the CSI modulation index which is the ratio of the peak line-to-line current seen at the AC side of the inverter ($|I_{csi}|$) to the peak DC-link current seen at the DC side of the inverter ($\hat{I}_{dc}$) as shown in (4.8).

$$m_i = \frac{|I_{vsi}|}{\hat{I}_{dc}} \qquad ; 0 < m_i \leq 1 \tag{4.8}$$

Sector	Selected Switching Vectors		Duty Time
	Active vectors	Null vectors	
1	$\overrightarrow{SC6}$, $\overrightarrow{SC1}$	$\overrightarrow{SC7}$, $\overrightarrow{SC8}$, $\overrightarrow{SC9}$	$T_1 = m_i T_s \sin(\frac{\pi}{3} - \theta_i^*)$ $T_2 = m_i T_s \sin(\theta_i^*)$ $T_0 = T_s - T_1 - T_2$; where $0 \leq \theta_i^* < \pi/3$ and $0 < m_i \leq 1$
2	$\overrightarrow{SC1}$, $\overrightarrow{SC2}$	$\overrightarrow{SC7}$, $\overrightarrow{SC8}$, $\overrightarrow{SC9}$	
3	$\overrightarrow{SC2}$, $\overrightarrow{SC3}$	$\overrightarrow{SC7}$, $\overrightarrow{SC8}$, $\overrightarrow{SC9}$	
4	$\overrightarrow{SC3}$, $\overrightarrow{SC4}$	$\overrightarrow{SC7}$, $\overrightarrow{SC8}$, $\overrightarrow{SC9}$	
5	$\overrightarrow{SC4}$, $\overrightarrow{SC5}$	$\overrightarrow{SC7}$, $\overrightarrow{SC8}$, $\overrightarrow{SC9}$	
6	$\overrightarrow{SC5}$, $\overrightarrow{SC6}$	$\overrightarrow{SC7}$, $\overrightarrow{SC8}$, $\overrightarrow{SC9}$	

Table 4.6 Switching vectors and their duty times used in the SVM-CSI

By applying the criteria used to form the switching sequence presented in Section 4.3.1, a four-segment switching sequence (referred as a *single-sided asymmetrical switching sequence*) is required to operate over one switching time period for the CSI modulation. For example, the sequence $\overrightarrow{SC7} - \overrightarrow{SC6} - \overrightarrow{SC1} - \overrightarrow{SC7}$ (which has a switching code of *aa-ac-ab-aa*) is used when the reference vector $\vec{I}^*_{ref}$ is located in Sector 1. This switching sequence allows only two switches to turn on and off per vector transition whilst having the null vector $\overrightarrow{SC7}$ to be the first and the last vectors of the sequence as shown in Figure 4.14. Similar switching sequences can be applied for the other sectors (Sector 2 to Sector 6) using Table 4.7.

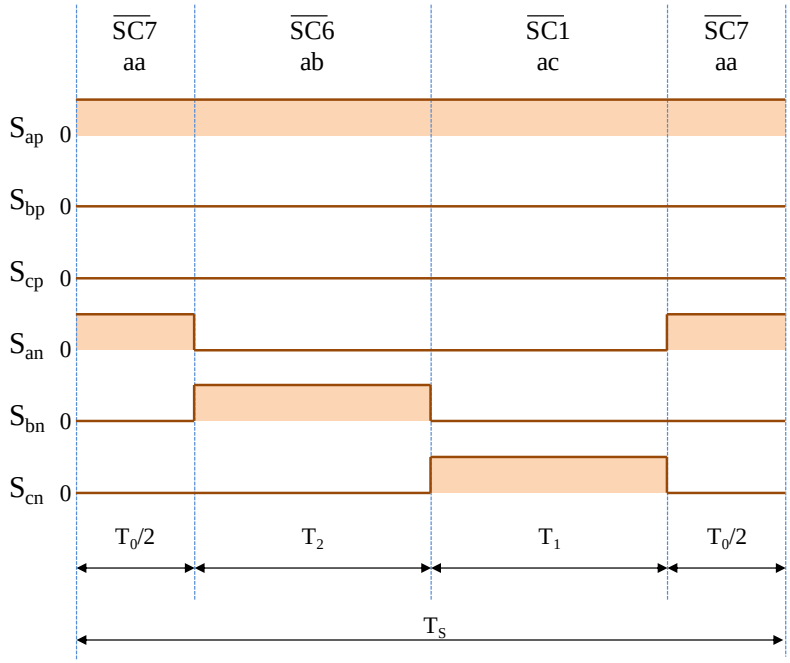


Figure 4.14 Single-sided asymmetrical switching sequence of the CSI modulation over one switching period when the reference current vector is located in the Sector 1

Sector	Single-sided Asymmetrical Switching Sequence for SVM-VSI			
1	$\overrightarrow{\overline{SC7}}$	$\overrightarrow{\overline{SC6}}$	$\overrightarrow{\overline{SC1}}$	$\overrightarrow{\overline{SC7}}$
	aa	ab	ac	aa
2	$\overrightarrow{\overline{SC9}}$	$\overrightarrow{\overline{SC1}}$	$\overrightarrow{\overline{SC2}}$	$\overrightarrow{\overline{SC9}}$
	cc	ac	bc	cc
3	$\overrightarrow{\overline{SC8}}$	$\overrightarrow{\overline{SC2}}$	$\overrightarrow{\overline{SC3}}$	$\overrightarrow{\overline{SC8}}$
	bb	bc	ba	bb
4	$\overrightarrow{\overline{SC7}}$	$\overrightarrow{\overline{SC3}}$	$\overrightarrow{\overline{SC4}}$	$\overrightarrow{\overline{SC7}}$
	aa	ba	ca	aa
5	$\overrightarrow{\overline{SC9}}$	$\overrightarrow{\overline{SC4}}$	$\overrightarrow{\overline{SC5}}$	$\overrightarrow{\overline{SC9}}$
	cc	ca	cb	cc
6	$\overrightarrow{\overline{SC8}}$	$\overrightarrow{\overline{SC5}}$	$\overrightarrow{\overline{SC6}}$	$\overrightarrow{\overline{SC8}}$
	bb	cb	ab	bb

Table 4.7 Single-sided asymmetrical switching sequences for each sector of the SVM-CSI

Additionally, in order to prevent a high voltage caused by the open-circuit of the DC-link current, a delay time called *overlap time* is added to the falling edge of the gate signal to the outgoing switch to ensure that a freewheeling path is always provided for the DC-link current. In other words, the overlap time is used to ensure that the incoming switch is completely turned on before the outgoing switch is turned off and

thus gives the continuity of the DC-link current. However, depending on the sign of the line-to-line AC voltage that controls the commutation process, the commutation can take place before or after the overlap time and if not compensated, the implementation of the overlap time in the CSI modulation will cause waveform distortion and degrade the capability to operate at very low and at near maximum DC-to-AC current transfer ratio [87].

4.3.4 ZSI Modulation

The modulation techniques used for the voltage fed ZSI and the current fed ZSI depend on the PV voltage conditions as shown in Table 4.8.

Topology	PV Voltage Condition	Modulation Type
Voltage fed ZSI	> peak line-to-line grid voltage	VSI modulation
	≤ peak line-to-line grid voltage	ZSI modulation using shoot-through switching states
Current fed ZSI	< $\sqrt{3}/2$ peak line-to-line grid voltage	CSI modulation
	≥ $\sqrt{3}/2$ peak line-to-line grid voltage	ZSI Modulation using open-circuit switching states

Table 4.8 Modulations types required for the voltage fed ZSI and the current fed ZSI under different PV voltage conditions

From Table 4.8, as the voltage fed ZSI is the VSI-type of operation, when the PV voltage is greater than peak line-to-line grid voltage, the VSI modulation presented in Section 4.3.2 can also be used for the voltage fed ZSI. On the other hand, as the current fed ZSI is the CSI-type of operation, when the PV voltage is lower than $\sqrt{3}/2$ peak line-to-line grid voltage, the CSI modulation presented in Section 4.3.3 can also be used for the current fed ZSI.

This section presents the modulation for the voltage fed ZSI when the PV voltage is lower than the peak line-to-line grid voltage using the shoot-through switching states and the modulation for the current fed ZSI when the PV voltage is greater than $\sqrt{3}/2$ peak line-to-line grid voltage using the open-circuit switching states.

As presented in Sections 4.2.5 and 4.2.6, the shoot-through switching states can be used to step up the low PV voltage for the voltage fed ZSI when the PV voltage is insufficient whilst the open-circuit switching states can be used to step down the high PV voltage for the current fed ZSI when the PV voltage exceeds the voltage transfer limit. The shoot-through switching states are obtained when the switches in the same inverter leg (of one or two or all of inverter legs) are turned on at the same time whilst the open-circuit switching states are obtained when all of the switches on the same DC-link rail (either upper and/or lower) are turned off at the same time. Table 4.9 and Table 4.10 show the shoot-through switching states and open-circuit switching states that are used in the voltage fed ZSI modulation and the current fed ZSI modulation [88, 89].

Shoot-through Switching State	**Switching State**						**Short-Circuiting Inverter Leg(s)**
	S_{ap}	S_{bp}	S_{cp}	S_{an}	S_{bn}	S_{cn}	
ST01	1	0	0	1	1	1	phase “a”
ST02	0	1	0	1	1	1	phase “b”
ST03	0	0	1	1	1	1	phase “c”
ST04	1	1	1	1	0	0	phase “a”
ST05	1	1	1	0	1	0	phase “b”
ST06	1	1	1	0	0	1	phase “c”
ST07	1	1	0	0	1	1	phase “a” and “b”
ST08	1	1	0	1	0	1	phase “b” and “c”
ST09	0	1	1	1	0	1	phase “c” and “a”
ST10	0	1	1	1	1	0	phase “a” and “b”
ST11	1	0	1	1	1	0	phase “b” and “c”
ST12	1	0	1	0	1	1	phase “c” and “a”
ST13	1	1	1	1	1	1	phase “a”, “b” and “c”

Table 4.9 Shoot-through switching states for the voltage fed ZSI modulation

Open-Circuit Switching State	**Switching State**						**Open-Circuiting DC-link rail (s)**
	S_{ap}	S_{bp}	S_{cp}	S_{an}	S_{bn}	S_{cn}	
OC01	1	0	0	0	0	0	Lower
OC02	0	1	0	0	0	0	Lower
OC03	0	0	1	0	0	0	Lower
OC04	0	0	0	1	0	0	Upper
OC05	0	0	0	0	1	0	Upper
OC06	0	0	0	0	0	1	Upper
OC07	0	0	0	0	0	0	Lower and Upper

Table 4.10 Open-circuit switching states for the current fed ZSI modulation

The SVM-VSI and SVM-CSI techniques described in Sections 4.3.2 and 4.3.3 can also be used for the ZSI modulations. The only difference is the addition of the shoot-through in the voltage fed ZSI modulation or the open-circuit switching states in the current fed ZSI modulation. The rate of the DC-to-AC voltage boosting in the voltage fed ZSI modulation and the rate of the DC-to-AC voltage reducing in the current fed ZSI modulation are proportional to the duty time of the shoot-through switching state (T_{ST}) and duty time of open-circuit switching state (T_{OC}).

Since both the shoot-through and open-circuit switching states do not allow the power to be transferred between the DC side and the AC side which is the characteristics of the null switching state, these switching states therefore should be implemented as part of the null switching state time interval (T_0). Figures 4.15 and 4.16 show the switching sequences used for the voltage fed ZSI modulation and the current fed ZSI modulation when the reference vector is located in Section 1.

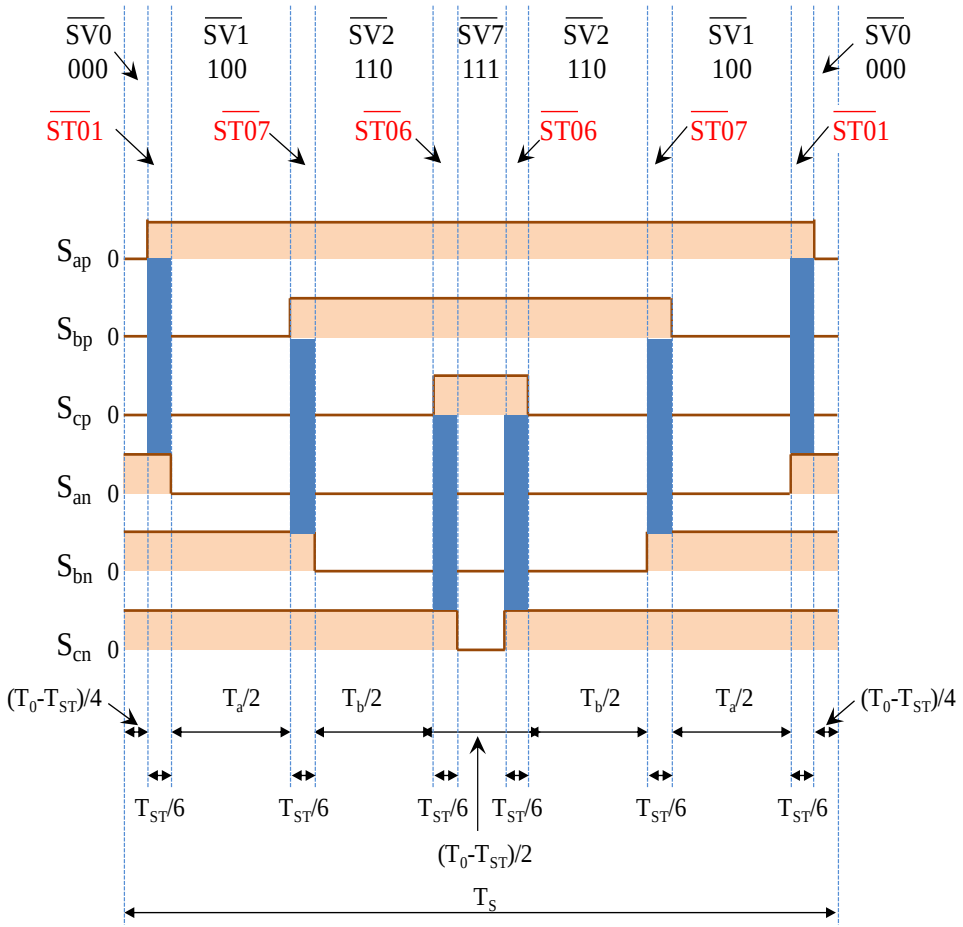


Figure 4.15 Double-sided symmetrical switching sequence of the voltage fed ZSI modulation for one switching period when the reference vector is located in Sector 1

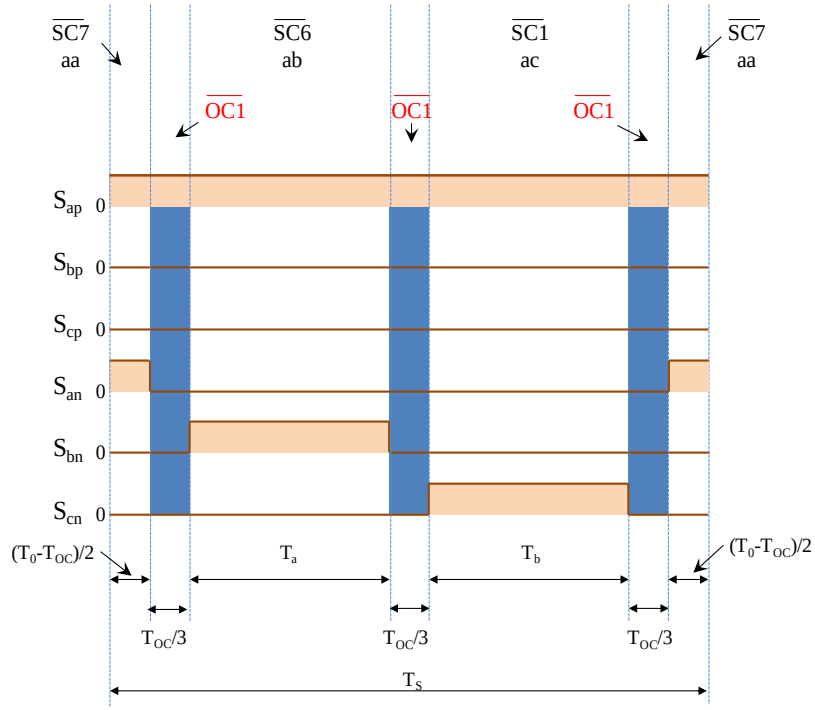


Figure 4.16 Single-sided asymmetrical switching sequence of the current fed ZSI modulation for one switching period when the reference vector is located in Sector 1

It can be seen from Figures 4.15 and 4.16 that:

- The switching sequence of the voltage fed ZSI modulation is derived from the sequence of the VSI modulation. Only the shoot-through switching states are inserted "during" every vector transition of the VSI modulation, which allows the voltage fed ZSI sequence and the VSI sequence to have the same total number of the switchings per one switching period.

- The switching sequence of the current fed ZSI modulation is derived from the sequence of the CSI modulation. Only the open-circuit switching states are inserted "during" every vector transition of the CSI modulation, which allows the current fed ZSI sequence and the CSI sequence to have the same total number of the switchings per one switching period.

- Since the shoot-through switching states and the open-circuit switching states are implemented as part of the null state duty time interval, these switching states do not affect the operating modulation depth.

Similar switching sequences to the sequences shown in Figures 4.15 and 4.16 can be applied for the other sectors (Sector 2 to Sector 6) for the voltage fed ZSI modulation and the current fed ZSI modulation using Table 4.11 and Table 4.12.

Sector	Switching Sequences for the Voltage Fed ZSI modulation												
1	$\overrightarrow{SV0}$	$\overrightarrow{ST01}$	$\overrightarrow{SV1}$	$\overrightarrow{ST07}$	$\overrightarrow{SV2}$	$\overrightarrow{ST06}$	$\overrightarrow{SV7}$	$\overrightarrow{ST06}$	$\overrightarrow{SV2}$	$\overrightarrow{ST07}$	$\overrightarrow{SV1}$	$\overrightarrow{ST01}$	$\overrightarrow{SV0}$
2	$\overrightarrow{SV7}$	$\overrightarrow{ST02}$	$\overrightarrow{SV2}$	$\overrightarrow{ST08}$	$\overrightarrow{SV3}$	$\overrightarrow{ST06}$	$\overrightarrow{SV0}$	$\overrightarrow{ST06}$	$\overrightarrow{SV3}$	$\overrightarrow{ST08}$	$\overrightarrow{SV2}$	$\overrightarrow{ST02}$	$\overrightarrow{SV7}$
3	$\overrightarrow{SV0}$	$\overrightarrow{ST02}$	$\overrightarrow{SV3}$	$\overrightarrow{ST09}$	$\overrightarrow{SV4}$	$\overrightarrow{ST04}$	$\overrightarrow{SV7}$	$\overrightarrow{ST04}$	$\overrightarrow{SV4}$	$\overrightarrow{ST09}$	$\overrightarrow{SV3}$	$\overrightarrow{ST02}$	$\overrightarrow{SV0}$
4	$\overrightarrow{SV7}$	$\overrightarrow{ST03}$	$\overrightarrow{SV4}$	$\overrightarrow{ST10}$	$\overrightarrow{SV5}$	$\overrightarrow{ST04}$	$\overrightarrow{SV0}$	$\overrightarrow{ST04}$	$\overrightarrow{SV5}$	$\overrightarrow{ST10}$	$\overrightarrow{SV4}$	$\overrightarrow{ST03}$	$\overrightarrow{SV7}$
5	$\overrightarrow{SV0}$	$\overrightarrow{ST03}$	$\overrightarrow{SV5}$	$\overrightarrow{ST11}$	$\overrightarrow{SV6}$	$\overrightarrow{ST05}$	$\overrightarrow{SV7}$	$\overrightarrow{ST05}$	$\overrightarrow{SV6}$	$\overrightarrow{ST11}$	$\overrightarrow{SV5}$	$\overrightarrow{ST03}$	$\overrightarrow{SV0}$
6	$\overrightarrow{SV7}$	$\overrightarrow{ST01}$	$\overrightarrow{SV6}$	$\overrightarrow{ST12}$	$\overrightarrow{SV1}$	$\overrightarrow{ST05}$	$\overrightarrow{SV0}$	$\overrightarrow{ST05}$	$\overrightarrow{SV1}$	$\overrightarrow{ST12}$	$\overrightarrow{SV6}$	$\overrightarrow{ST01}$	$\overrightarrow{SV7}$

Table 4.11 Double-sided symmetrical switching sequences for each sector of the voltage fed ZSI modulation

Sector	Switching Sequences for the Current Fed ZSI modulation						
1	$\overrightarrow{SC7}$	$\overrightarrow{OC1}$	$\overrightarrow{SC6}$	$\overrightarrow{OC1}$	$\overrightarrow{SC1}$	$\overrightarrow{OC1}$	$\overrightarrow{SC7}$
2	$\overrightarrow{SC9}$	$\overrightarrow{OC6}$	$\overrightarrow{SC1}$	$\overrightarrow{OC6}$	$\overrightarrow{SC2}$	$\overrightarrow{OC6}$	$\overrightarrow{SC9}$
3	$\overrightarrow{SC8}$	$\overrightarrow{OC2}$	$\overrightarrow{SC2}$	$\overrightarrow{OC2}$	$\overrightarrow{SC3}$	$\overrightarrow{OC2}$	$\overrightarrow{SC8}$
4	$\overrightarrow{SC7}$	$\overrightarrow{OC4}$	$\overrightarrow{SC3}$	$\overrightarrow{OC4}$	$\overrightarrow{SC4}$	$\overrightarrow{OC4}$	$\overrightarrow{SC7}$
5	$\overrightarrow{SC9}$	$\overrightarrow{OC3}$	$\overrightarrow{SC4}$	$\overrightarrow{OC3}$	$\overrightarrow{SC5}$	$\overrightarrow{OC3}$	$\overrightarrow{SC9}$
6	$\overrightarrow{SC8}$	$\overrightarrow{OC5}$	$\overrightarrow{SC5}$	$\overrightarrow{OC5}$	$\overrightarrow{SC6}$	$\overrightarrow{OC5}$	$\overrightarrow{SC8}$

Table 4.12 Single-sided asymmetrical switching sequences for each sector of the current fed ZSI modulation

4.4 Control Strategies

This section presents the control methods used for the six inverter topologies which have been previously introduced in this chapter. The purposes of the control methods presented in this section are to control the AC line currents to be in phase and synchronised with the grid voltages and to control the DC side voltage to have a suitable level for the different types of the inverter topologies to operate.

4.4.1 VSI Control

The method that is used to control the AC currents to be in phase and synchronised with the grid voltages for the three-phase VSI topology is by converting the three-phase AC currents into a single current vector rotating in the grid voltage space vector plane using the technique described in Section 4.3.1 and using PI controllers to control the current vector to be in phase and synchronised with the grid voltage vector [90, 91]. The schematic for the VSI control is shown in Figure 4.17, which can be described as below:

- The grid voltages ($v_{s(abc)}$) are measured and transformed into a single vector rotating in the α-β vector plane using the technique described in Section 4.3.1.
- The actual line currents ($i_{s(abc)}$) are measured and transformed into a single vector rotating in the grid voltage d-q rotating reference frame, which give the d-q current components: i_{sd} (real current) and i_{sq} (reactive current).
- The PI current controllers compare i_{sd} and i_{sq} with the reference current demands (i_{sd}* and i_{sq}*). The real current demand i_{sd}* is generated from the maximum power point tracking (MPPT) controller and the reactive current demand i_{sq}* is set to be zero in order to control the AC currents to be in phase with the grid voltages, by means of unity power factor operation.
- The output of the real current controller is fed forward by v_{sd} which is offset by $i_{sq} \cdot \omega L$ and the output of the reactive current controller is offset by $-\omega L i_{sd}$. The offsets are added in order to compensate for the phase shift caused by the voltage drop across the inductive AC filters L_f. This results in the reference d-q voltage components (v_{rd}* and v_{rq}*).
- Then, v_{rd}* and v_{rq}* are transferred back into the stationary frame ($v^*_{r(abc)}$) and supplied to the VSI modulator to determine the suitable switching vectors and calculate the duty times for the switching devices using the procedure described in Section 4.3.1.
- The PI controllers control the errors between the actual AC currents and the reference current demands to be zero and thus give the AC currents that are in phase and synchronised with the grid voltages as required.

The VSI modulation index (m_v) is the parameter that is used to control and match the different voltage levels between the DC side of the VSI (constant if the grid voltages are stable) and the PV array (variable depending on the maximum power point of the PV array). m_v is defined in (4.7), and m_v for this case can be estimated using (4.9).

$$m_v \approx \frac{\left|v^*_{r(abc)}\right|}{v_{pv}} \qquad ; 0 < m_v \leq 1 \tag{4.9}$$

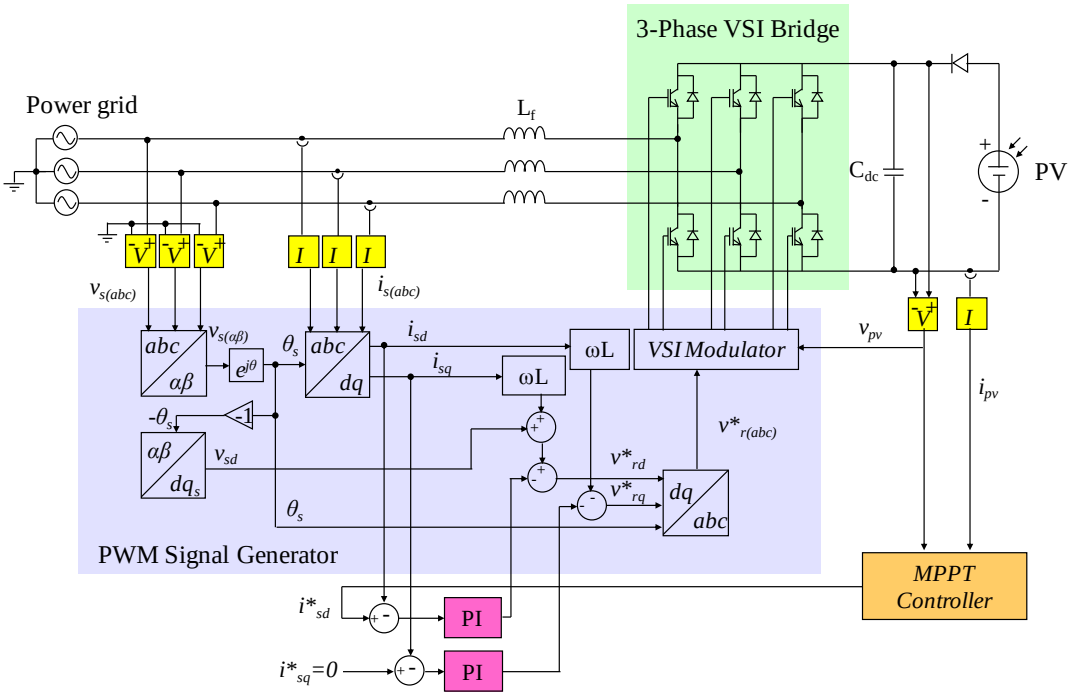


Figure 4.17 Schematic for the VSI control

4.4.2 CSI Control

The CSI control utilises the same concept as the VSI control in order to control the AC currents to be in phase and synchronised with the grid voltages. However, as the CSI topology usually has a constant DC-link current, the CSI control can synthesise the current vector using the measured PV current rather than using the measured AC currents. As a result, a single PI controller can be used to control the DC-link current level for the CSI control [92]. Figure 4.18 shows the schematic for the CSI control, which can be explained as the following process:

- The grid voltages ($v_{s(abc)}$) are measured and transformed into a single voltage vector rotating in the α-β vector plane using the technique described in Section 4.3.1. This creates the rotating angle θ_s that can be used to be the reference angle for the AC line current vector.

- The phase shift caused by the capacitive currents in the AC capacitors C_f is compensated using $i_{sq}^* = \omega C_f v_{sd}$ in order to achieve unity power factor operation. Then the reference current demands i_{sd}^* and i_{sq}^* are used to determine the reference rotating angle for the line current vector (θ_r^*); where i_{sd}^* is received from the MPPT controller.

- The actual PV current (i_{pv}) is compared with the reference PV current demand (i_{pv}^*) that is generated from the MPPT controller. This gives the errors to the PI controller to determine the reference modulation depth demand (m_i^*).

- m_i^* in conjunction with θ_r^* produces the duty times for the switching devices using Table 4.6.

As the CSI can synthesises the reference current vector using the PV current, the line current transducers are no longer necessary. This implies that the CSI topology potentially has a simpler control circuit and an easier way to interface with the MPPT controller compared to the VSI topology, as the DC-link current is the only parameter. Moreover, as the DC-link current level is controlled, the DC-link voltage level will be automatically adjusted according the change of the operating CSI modulation index (m_i) and for this case can be determined from (4.10); where ΔV is the output error from the DC-link current PI controller.

$$m_i = \frac{(v_{pv} - \Delta V)}{1.5 v_{sd}} \qquad ; 0 < m_i \leq 1 \qquad (4.10)$$

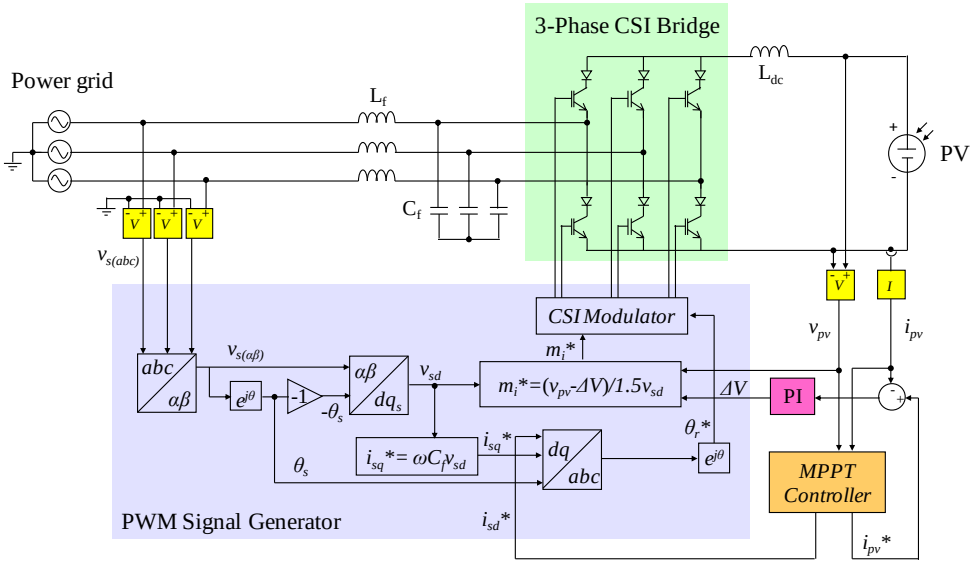


Figure 4.18 Schematic for the CSI control

4.4.3 Two-Stage VSI with a Boost Converter Control

A two-stage voltage with a boost converter is controlled in the same manner as the VSI when the PV voltage is sufficiently large to force the anti-parallel diodes in the VSI to be reverse biased and enable operation in inverter mode which requires the DC-link voltage to be higher than the peak line-to-line grid voltage. When the PV voltage is insufficient, the PV voltage can be boosted with the use of the boost converter. The voltage boost ratio (B_{boost}) is dependent on the ratio of the DC-link voltage to the PV voltage. In practical terms, the B_{boost} is the ratio of the turn-on time (T_{ON}) to the switching cycle time of the boost switch (T_{SB}) as defined by (4.11). The longer the boost switch is on, the higher the PV voltage is boosted.

$$B_{boost} = \frac{V_{dc}}{V_{pv}} = \frac{1}{(1-T_{ON}/T_{SB})} \quad ; \; B_{boost} \geq 1 \tag{4.11}$$

Figure 4.19a shows the operation of the two-stage VSI with a boost converter when the boost switch is turned on. The inductor L_{boost} is charged and stores energy whilst the capacitor C_{dc} supplies the power to the grid. Figure 4.19b shows the situation when the switch is turned off. The boost inductor L_{boost} discharges its stored energy and produces an additional voltage (v_L) that tops the PV voltage to match the higher DC-link voltage level (v_{dc}). If the inductor is large enough and/or the switching frequency is high enough, a continuous inductive current (i_L) will be achieved [77].

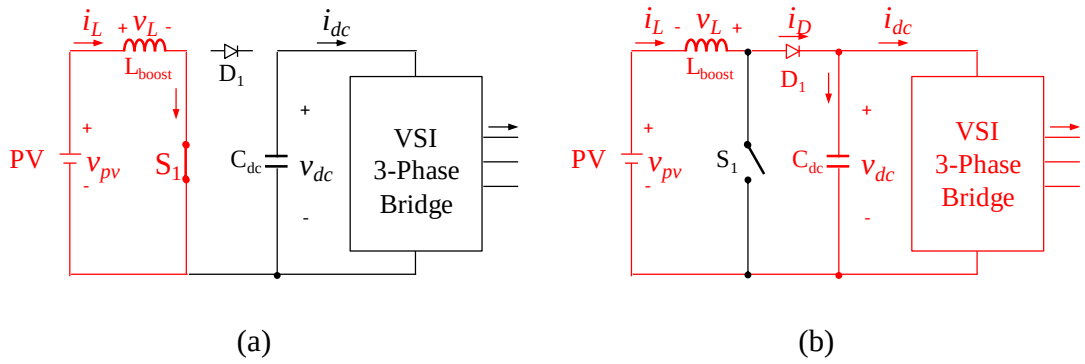


Figure 4.19 Diagrams of the two-stage VSI with a boost converter when the boost switch is (a) turned on and (b) turned off

The scheme for the two-stage VSI with a boost converter is shown in Figure 4.20. The DC-link voltage level adapter is added into the VSI control which has been already presented in Section 4.4.1. The actual DC-link voltage is compared to the reference DC-link voltage (v_{dc}*) and then the resulting error is put into the DC-link voltage PI controller to generate a suitable turn-on time for the boost switch (T_{ON}) over one switching period (T_{SB}). The reference DC-link voltage (v_{dc}*) is usually set to be higher than peak line-to-line grid voltage, which is the minimum required voltage level for the VSI.

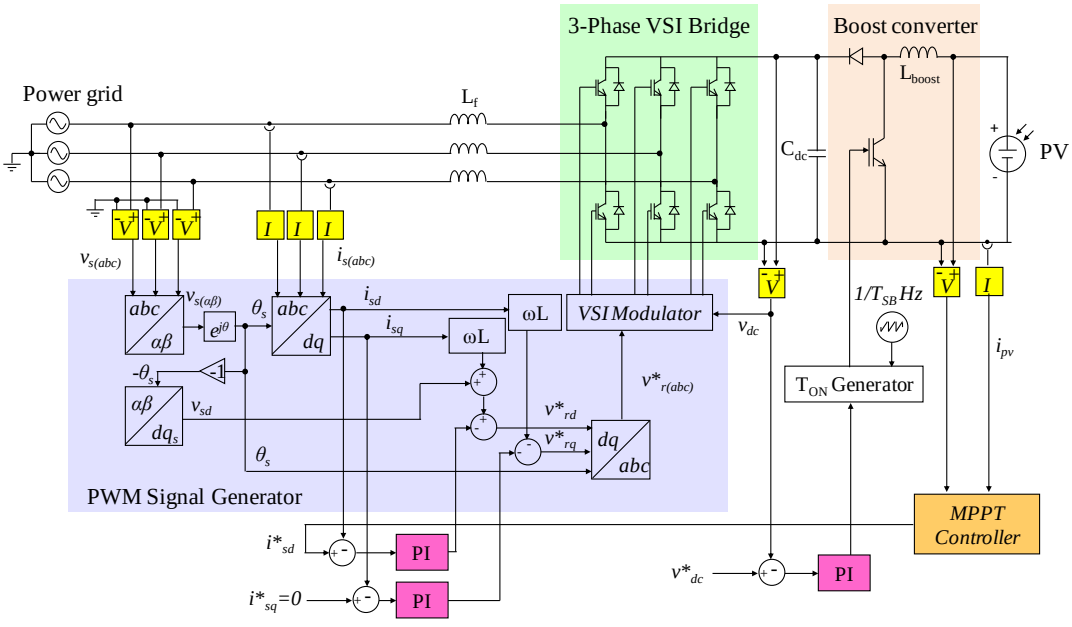


Figure 4.20 Schematic for the two-stage VSI with a boost converter control

4.4.4 Two-Stage CSI with a Buck Converter Control

A two-stage CSI with a buck converter is controlled in the same manner as the CSI when the PV voltage is less than the limit (lower than $\sqrt{3}/2$ peak line-to-line grid voltage) in order to operate in the inverter mode as well as avoid over modulation. In this situation the buck converter stage is disabled (the buck switch is continuously turned on). When the PV voltage is over the CSI voltage transfer limit, the buck converter will operate in order to reduce the DC-link voltage to the level that allows the CSI stage to operate properly. The voltage reduction ratio (B_{buck}) is dependent on the ratio of the PV voltage to the DC-link voltage level. In practical terms, the B_{buck} is the ratio of the turn off time (T_{OFF}) to the switching cycle time (T_{SB}) of the buck switch as expressed by (4.12). The longer the buck switch is off, the lower the PV voltage is reduced.

$$B_{buck} = \frac{V_{pv}}{V_{dc}} = 1 - (T_{OFF}/T_{SB}) \qquad ; \text{where } B_{buck} \leq 1 \tag{4.12}$$

Figure 4.21a illustrates the operation of the two-stage CSI with a buck converter when the buck switch is turned on. At this time the inductor L_{dc} is connected between the voltage from the PV source (v_{pv}) and the DC-link voltage (v_{dc}). The stored inductor energy is increased. Figure 4.21b shows the situation when the switch is turned off and the PV source is disconnected. The inductor L_{dc} discharges its energy and supplies the current to the grid. In average, this results in a lower voltage than the PV source. If the inductor is large enough and/or the switching frequency is high enough, a continuous inductive current will be produced.

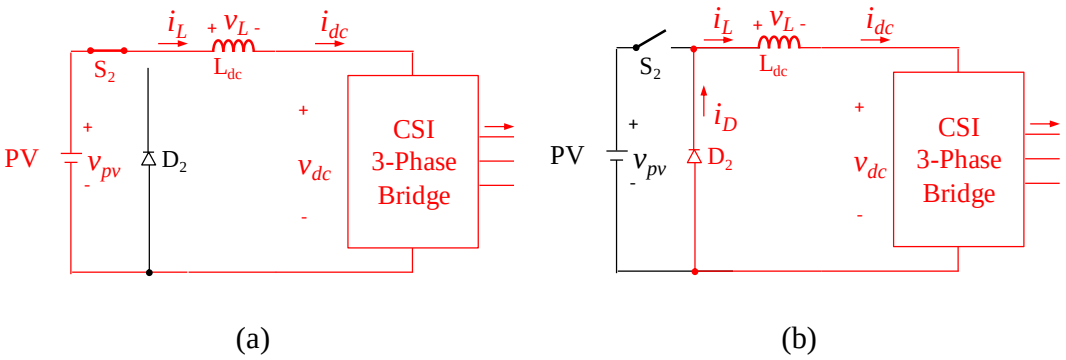


Figure 4.21 Diagrams of the two-stage CSI with a buck converter when the buck switch is (a) turned on and (b) turned off

The scheme of the two-stage CSI with a buck converter control is shown in Figure 4.22. The DC-link voltage level adapter is added into the CSI control scheme which has been already presented in Section 4.4.2. The actual DC-link voltage (v_{dc}) after filtered using a low pass (LF) filter is compared to the reference DC-link voltage (v_{dc}*) and then the resulting error is put into the DC-link voltage PI controller to generate a suitable turn-off time for the buck switch (T_{OFF}) over one switching period (T_{SB}). The reference DC-link voltage (v_{dc}*) is set to be less than $\sqrt{3}/2$ peak line-to-line grid voltage, which is the maximum voltage transfer limit of the CSI.

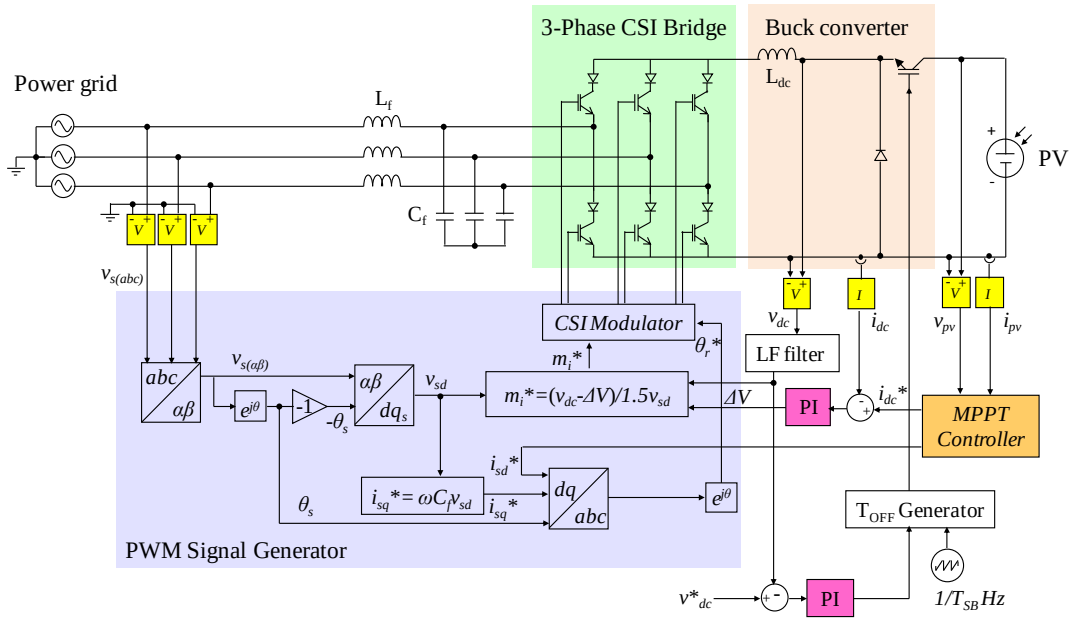


Figure 4.22 Schematic for the two-stage CSI with a buck converter control

4.4.5 Voltage Fed Z-Source Inverter Control

As presented in Section 4.3.4, when the PV voltage is high enough (greater than peak line-to-line grid voltage), the voltage fed ZSI will behave in the same manner as the standard VSI. Therefore, the VSI modulation presented in Section 4.3.2 and the control method presented in Section 4.4.1 can be used. On the other hand, when the PV voltage is too small for correct operation, the shoot-through switching states will also be used in order to step up the PV voltage to reach the suitable level.

Figure 4.23a presents the operation of the voltage fed ZSI topology when operating in one of the eight allowable (non-shoot-through) switching states. In this situation, the topology operates in the same manner as the VSI and gives the output voltage and

current to the grid where the DC-link voltage is sufficient for the VSI-type inverter to operate. Figure 4.23b shows the situation when the topology operates in the shoot-through state. In this situation, the AC side terminals of the VSI 3-phase bridge are short-circuited that causes a zero voltage at the DC side of the inverter and thus no power transferred between the DC side and the AC side. A high DC-link current (i_{dc}) is created but its rate of rising is limited by the inductance of the X-shaped impedance circuit. The summation of the voltage of the two capacitors (C_1 and C_2) is greater than the PV voltage (v_{pv}), where the diode is reversed bias and does not allow the current to flow back in the PV array. The capacitors (C_1 and C_2) release their power to charge the inductors (L_1 and L_2). The rate of the voltage boosting ($B_{zsi\text{-}v}$) is dependent on the shoot-through time which can be determined using (4.13).

$$B_{zsi-v} = \frac{v_{dc}}{v_{pv}} = \frac{1}{(1-2T_{ST}/T_s)} \quad ; \; B_{zsi-v} \geq 1 \tag{4.13}$$

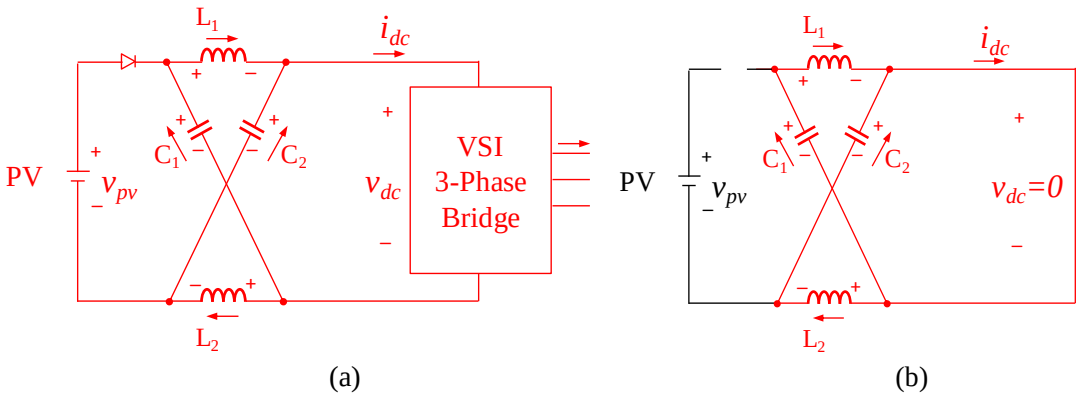


Figure 4.23 Diagrams of the voltage fed ZSI when operating with (a) non shoot-through switching states and (b) shoot-through switching states

There are several control methods to implement the shoot-through time in order to step up the PV voltage to match the DC-link voltage level [35-37, 88, 93]. The choice of the control method is dependent on the tradeoffs between the voltage boost capability, voltage stress across the switches, output ripple and control complexity. The simple boost control [35] has the simplest control scheme but this method provides the highest voltage stress on the circuit components. The maximum boost control [88, 93] can achieve the minimum voltage stress, but the method has problems with low frequency ripple. The maximum constant boost control [36] can eliminate the low frequency ripple and minimum voltage stress, but this method has a complex

control scheme. The modified VSI SVM control [37] provides simple switching sequences, the highest boost capability and maximum modulation depth operation capability, but the method produces high voltage stress. The third harmonic injection technique could be used for a further voltage stress reduction as well as an increased boost capability; however, this method has a much more complex control [94]. In this thesis, the modified SVM control method is used.

The scheme of the voltage fed ZSI control is shown in Figure 4.24. The control used for the voltage fed ZSI is similar to the VSI control. The difference is only that the DC-link voltage level adapter block and the shoot-through time (T_{ST}) generator have been inserted. If the PV voltage is lower than the required DC-link voltage level v_{dc}* (lower than peak line-to-line grid voltage, which is $\sqrt{3}vsd + isq\omega L_f$), the shoot-through switching states will be implemented for the time of T_{ST} as shown in the control scheme (derived from (4.13)). The limiter is used to ensure that T_{ST} is implemented as part of the null state time interval, which is less than the time of (1-m*)·T_S. The filter capacitor C_{pv} also is added to decouple the inverter and the PV source and to smooth the PV voltage and PV current during operating in the shoot-through switching states.

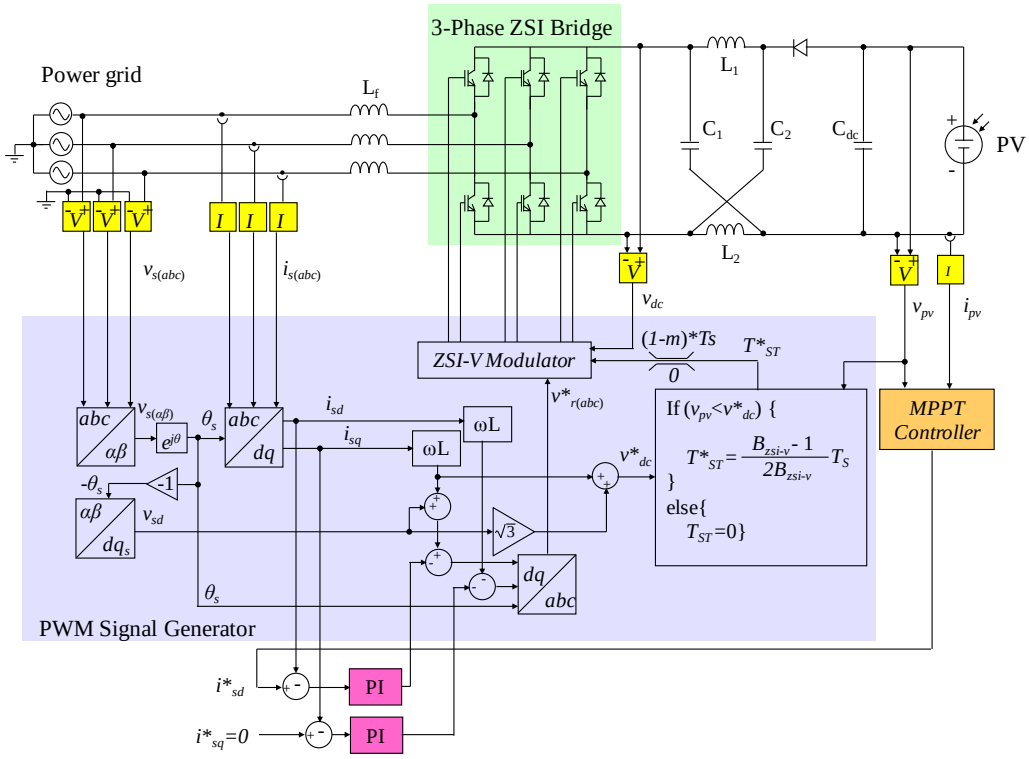


Figure 4.24 Schematic for the voltage fed ZSI Control

4.4.6 Current Fed Z-Source Inverter Control

Similar to a voltage fed ZSI, a current fed ZSI can operate in both, DC-to-AC voltage step-up mode and step-down mode [89, 95, 96]. In the voltage step-up mode where the PV voltage is below the limit for correct operation, the current fed ZSI will behave in the same way as the standard CSI. Therefore, the CSI modulation presented in Section 4.3.3 and the CSI control method presented in Section 4.4.2 can be used. In the voltage step-up mode where the PV voltage is over the limit, the open-circuit switching states have to be used in order to step down the PV voltage to be lower than the limit level.

Figure 4.25a shows the situation when the current fed ZSI operating in one of the nine allowable (non open-circuit) switching states. In this situation, the topology operates in the same manner as the standard CSI and delivers power to the grid. Figure 4.25b shows the situation when the topology operates in one of the open-circuit switching states. In this situation, The DC side of the topology is open circuit, which then causes a zero DC-link current (i_{dc}=0) and delivers no power to the grid. A high DC-link voltage (v_{dc}) is created but it is limited by the impedance of the X-shaped circuit. The diode operates and conducts the current of the two inductors (L_3 and L_4), which is greater than the input PV current (i_{pv}). Since the average power seen at the input side and the output side of the X-shaped circuit should be equal, when the current of the inductors increases, the DC-link voltage seen at the DC side of the inverter will be reduced. The rate of the voltage reduction ($B_{zsi\text{-}i}$) is dependent on the open-circuit time which can be determined using (4.14).

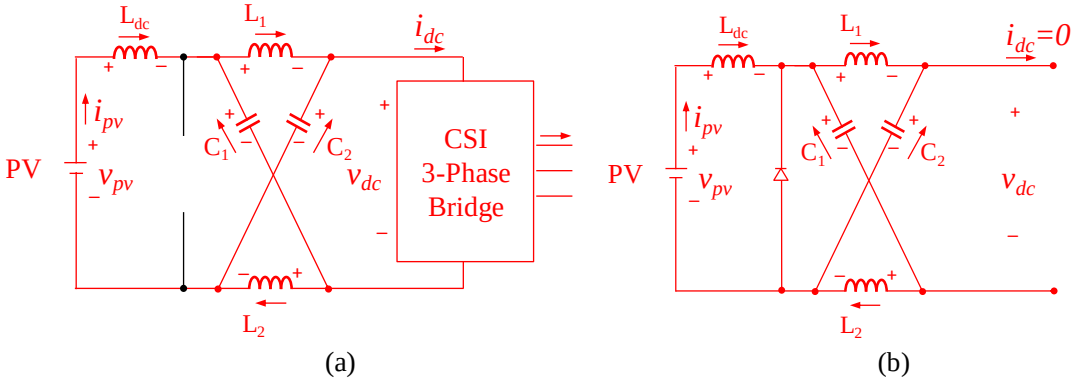


Figure 4.25 Diagrams of the current fed ZSI when operating in (a) non open-circuit switching states and (b) open-circuit switching states

$$B_{zsi-i} = \frac{v_{dc}}{v_{pv}} = \frac{i_{pv}}{i_{dc}} = 1 - 2T_{OC}/T_s \qquad ;\ B_{zsi-i} \leq 1 \tag{4.14}$$

The scheme of the current fed ZSI control is shown in Figure 4.26. The control used for the current fed ZSI is similar to the CSI control. The difference is only that the DC-link voltage level adapter block and the open-circuit time (T_{ST}) generator have been inserted. If the PV voltage is greater than the required DC-link voltage level v_{dc}* (greater than $\sqrt{3}/2$ peak line-to-line grid voltage, which is $1.5vsd$), the open-circuit switching states will be implemented for the time of T_{OC} as shown in the control scheme (derived from (4.14)). The limiter is used to ensure that T_{OC} is implemented as part of the null state time interval, which is less than the time of (1-m*)·T_S. The filter inductor L_{dc} is used to decouple the topology and the PV source and to smooth the PV voltage and current during operating in the open-circuit switching states.

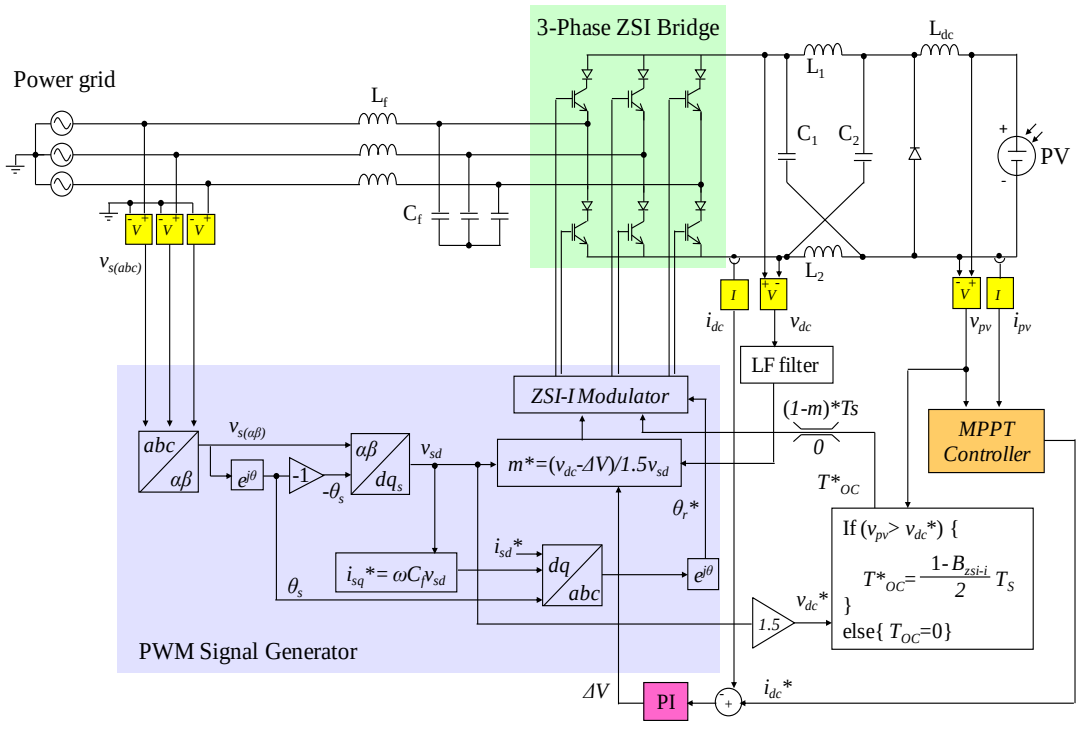


Figure 4.26 Schematic for the current fed ZSI control

4.5 Design Methodology for the Passive Components

4.5.1 Filtering Component Design

4.5.1.1 DC-Link Filtering Component Design

Normally, the criteria for the selection of the filter components can be based on the required limit of the ripple, the damping effect, or the resonant frequency [97]. Figure 4.27 shows the equivalent circuit of the filter when reactive components (L_{dc} and C_{dc}) are used. The input DC filter should be rated to be able to carry the input inductor current (i_L) in continuous mode and keep the ripple to be less than a specified value. The ripple of the output capacitor voltage (v_C) less than a specified value should also be taken into account.

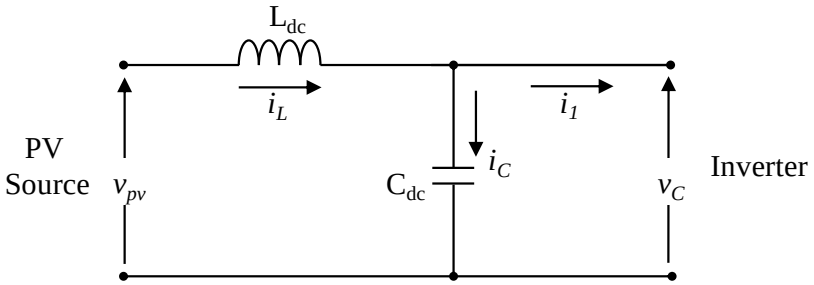


Figure 4.27 Equivalent circuit of the LC filter

Assuming that the PV source provides a constant voltage (v_{pv}) and the DC-link filter inductor (L_{dc}) is small, the minimum value of the input filter capacitor (C_{dc}) for the three-phase power converters, the standard VSI and the two-stage VSI with a boost converter can be calculated using (4.15) [98]; where $\Delta v_{c(max)}$ is the maximum permissible peak-to-peak voltage ripple and f_s is the converter switching frequency.

$$C_{dc(\min)} = \frac{i_L}{6 f_s \Delta v_{c(max)}} \tag{4.15}$$

On the other hand, assuming that the DC-link filter capacitor (C_{dc}) is large and the input filter inductor (L_{dc}) is used to reduce the current ripple, the minimum required value of the inductor L_{dc} for the three-phase power converters, the standard CSI and the two-stage CSI with a buck converter, can be determined by using (4.16) [98];

where $\Delta i_{L(max)}$ is the maximum permissible peak-to-peak current ripple, f_s is the switching frequency of the inverter and V_{line} is the grid line-to-line rms voltage.

$$L_{dc(\min)} = \frac{\sqrt{2}V_{line}}{4f_s\Delta i_{L(max)}} \tag{4.16}$$

In the case that both the inductor and capacitor are used in the DC-link filter circuit, the resonant frequency of the filter should be well below the switching frequency of the inverter as expressed by (4.17).

$$\frac{1}{2\pi\sqrt{L_{dc}C_{dc}}} < f_s \tag{4.17}$$

4.5.1.2 AC Filtering Component Design

The reactive AC components (AC inductors and/or AC capacitors) are usually used to construct the AC filters for most power converters in order to suppress the switching harmonics at the AC side [82, 99-101]. The resistors (commonly known as damping resistors) are sometimes required to attenuate the resonant effect of the filters and to improve system stability.

For the inverters with the VSI-type of operation (the standard VSI, the two-stage VSI with a boost converter and the voltage fed ZSI), only the inductive filters L_f could be used. These inductors should be chosen such that they can absorb all of the switching ripple cause by the VSI switching and cause a current ripple (peak-to-peak) to be below the imposed limit. Therefore, the design presented in Section 4.5.1.1 can be used. Alternatively, the AC inductors can be designed using the FFT analysis of the PWM voltage and should be chosen such that their impedance at the worse harmonic of the AC currents is below an imposed limit [99]. In this thesis, the design based on the current ripple limit is used.

For the inverter with the CSI-type of operation (the standard CSI, the two-stage CSI with a buck converter and the current fed ZSI), LC filters are usually used [99]. In this thesis the design method used for these filters based on the criteria of high output power factor in order to eliminate effect of reactive current drawn by the filters. The

reactive current drawn by the capacitive filter C_f must never cause the power factor to be less than a specified allowable limit. The maximum allowable value of C_f can be determined using (4.18); where P_{out} is the rated output active power, $\varphi_{\max}$ is the maximum allowable power factor angle (greater than $\cos^{-1}(0.95)$ is used in this thesis), f_l is the line frequency and V_s is the rms line voltage. And with the designed cut-off frequency of the LC filter (f_{LC}), the required L_f can be determined by using (4.19) [82].

$$C_{f(\max)} < \frac{P_{out}\tan(\varphi_{max})}{6\pi f_i V_s^2} \tag{4.18}$$

$$L_f = \frac{1}{4C_f\pi^2 f_{LC}^2} \tag{4.19}$$

It is important to note that the cut-off frequency of the LC filter (f_{LC}) should be well below the switching frequency of the converter and provide lower ripple less than the required limit. The optimum design for the cut-off frequency for the CSI-type topologies could be found in [100]. Damping resistors (R_{damp}) with a resistance higher than the inductive filter impedance as defined in (4.20) are usually connected in parallel with the filter inductor L_f [101].

$$R_{damp} > \omega L_f \tag{4.20}$$

4.5.2 Additional Component Design

4.5.2.1 A Boost Converter

The minimum required value of the boost inductor L_{dc} used in the two-stage VSI with a boost converter shown in Figure 4.3 can be determined from (4.21) [77]; where $\Delta i_{L(max)}$ and $\Delta v_{o(max)}$ are the maximum peak-to-peak DC-link current and voltage ripple respectively, T_{ON} is the turn-on time of the boost switch. The maximum value of T_{ON} is usually used in the calculation. Section 4.5.1.1 already presented the design used to determine the minimum required value of the capacitor C_{dc} using (4.15), here the required value for the capacitor C_{dc} in terms of the turn-on time of the boost switch is presented, as shown in (4.22).

$$L_{dc} \geq \frac{v_{pv} T_{ON}}{\Delta i_{L(max)}} \tag{4.21}$$

$$C_{dc} \geq \frac{i_o T_{ON}}{\Delta v_{o(max)}} \tag{4.22}$$

4.5.2.2. A Buck Converter

In Section 4.5.1.1 the minimum required value of the inductor L_{dc} used in the two-stage CSI with a buck converter has been already presented using (4.16), here the required value for the inductor L_{dc} in terms of the turn-off time of the buck switch (T_{OFF}) is presented, as shown in (4.23) [77].

$$L_{dc} \geq \frac{v_o T_{OFF}}{\Delta i_{L(max)}} \tag{4.23}$$

4.5.2.3 X-Shape Impedance Circuits

The minimum required values of the inductors and the capacitors in Figure 4.5 (for a ZSI-V topology) and Figure 4.6 (for a ZSI-I topology) can be determined by using (4.28)-(4.29) and (4.30)-(4.31) respectively [102]; where $\Delta i_{L(max)}$ is the maximum allowable inductor current ripple and $\Delta v_{c(max)}$ is the maximum allowable capacitor voltage ripple. T_{ST} and T_{OC} are the shoot-through time and the open-circuit time respectively. T_s and f_s are the switching time cycle and the switching frequency.

For the ZSI-V topology:

$$L_1 = L_2 \geq \frac{v_c T_{ST}}{2\Delta i_{L(max)}} \tag{4.28}$$

$$C_1 = C_2 \geq \frac{i_L T_{ST}}{2\Delta v_{c(max)}} \tag{4.29}$$

For a ZSI-I topology:

$$L_3 = L_4 \geq \frac{v_o (T_S - T_{OC})}{2\Delta i_{L(max)}} \tag{4.30}$$

$$C_3 = C_4 \geq \frac{1}{16 L_{dc}} \cdot \frac{v_o (T_S - T_{OC})}{f_S \Delta v_{o(max)}} \tag{4.31}$$

4.6 Summary

In this chapter the transformerless, grid-tied PV inverter topologies selected from those already proposed in the papers and suitable converters from the literature have been presented. These are the Voltage Source Inverter (VSI), the Current Source Inverter (CSI), the two-stage VSI with a boost converter, the two-stage CSI with a buck converter, the voltage fed Z-Source Inverter and the current fed Z-Source Inverter. Details of the circuit configurations, modulation and control strategies and the methodology to design the passive components required for these topologies have been presented. A brief summary of the details are as below:

- The VSI and the CSI have the simplest circuit configurations. However, since the VSI requires a PV voltage greater than the peak line-to-line grid voltage in order to transfer power from the PV source to the grid, a boost converter is usually added to step up and regulate the PV voltage to the required (constant) DC-link voltage level. In contrast, the CSI is a DC-to-AC step up converter that can operate over a wide PV voltage range (down to zero) but a PV voltage lower than 0.866 peak line-to-line grid voltage must be used to avoid CSI overmodulation and thus a buck converter could be used to step down and regulate the PV voltage to be less than the limit for the CSI. The addition of a boost or buck converter adds more cost, complexity and losses for these two-stage VSI/CSI topologies. Alternatively, the two types of the ZSI topologies, the voltage fed ZSI and the current fed ZSI, have the capability of both DC-to-AC voltage step-up and step-down regardless of the DC voltage levels and thus can operate in a wide PV voltage range. This can be achieved by the use of the added X-shaped impedance circuit and the use of the shoot-through switching states (for the voltage fed ZSI) or the open-circuit switching states (for the current fed ZSI). However, the ZSI topologies inherently have high voltage and current stress on the circuit components and a high number of passive components used in the circuits.

- The switching devices of the power converters must be modulated in suitable manner in order to provide desired sinusoidal AC currents at the grid side. The principle of Space Vector Modulation (SVM) and the criteria used to form the

switching sequence in this thesis have been presented, which then is applied for the different types of the inverter topologies under study in this chapter. Three types of the modulation techniques have been presented, which are the VSI modulation, CSI modulation and ZSI modulation. Brief details are as follows:

- The SVM utilises the fact that any three-phase sinusoidal waveforms can be converted into a single vector rotating on the complex plane. If the switching states of an inverter also are converted to the active vectors (allow power to transfer) and the null vectors (do not allow power to transfer), and then properly placed on the complex space plane with suitable magnitudes and directions, the rotating vector can be used to select two of the most suitable active vectors and one null vector (or more) and calculate the duty times for all of the switches.

- After the switching vectors are selected and the duty times for the selected switching vectors are calculated, those switching vectors have to be sequenced and operate for the calculated duty times. The switching sequences used in this thesis must allow only the minimum number of switching (up to two switching) per a vector transition to minimise switching loss and must have the same vector for the first and the last of the sequence in order to provide the continuity for the next switching period when repeated.

- VSI modulation must never cause a short circuit of DC-link voltage source since a high current will occur and damage the switches, which means that the switches on the same inverter leg must never turn on at the same time. This creates a total of eight allowable switching states for the VSI modulation. Using the SVM technique, these eight allowable switching states are converted to six active vectors and two null vectors. The active vectors split the vector plane into six sectors whilst the null vectors have no magnitude and direction. The reference voltage vector rotating on the plane is used to select two active vectors and null vectors from a particular sector. When applying the defined

criteria for switching sequence, the seven-segment (double-sided symmetrical) sequence is required.

- CSI modulation must never cause an open circuit of the DC-link current since a high voltage will occur and damage the switches. This creates a total of nine allowable switching states for the CSI modulation. Using the SVM technique, these nine allowable switching states are converted to six active vectors and three null vectors. The active vectors split the vector plane into six sectors as does the SVM-VSI but having 30 degrees twisted in leading compared to the VSI space plane to correct the phase of the AC currents. The four-segment (single-sided asymmetrical) sequence can be used for the CSI modulation in order to satisfy the defied switching sequence criteria.

- ZSI modulation used for the ZSI topologies is dependent on the PV voltage conditions. As the voltage fed ZSI is the VSI-type of operation, when the PV voltage is sufficiently higher than peak line-to-line grid voltage the VSI modulation will be used; otherwise, the shoot-through switching states will also be used. On the other hand, as the current fed ZSI is the CSI-type of operation, when the PV voltage is lower than 0.866 of the peak line-to-line grid voltage the CSI modulation will be used; otherwise, the open-circuit switching state will also be used. Since the shoot-through or open-circuit switching states do not allow the power to be transferred which is the characteristics of the null switching state, these switching states are inserted as part of the null switching state time interval. The shoot-through and open-circuit switching states are implemented during every vector transition in order to have the same number of switchings per switching period as the VSI or CSI modulation.

- The passive component design methodology used in the inverter topologies under investigation has been also presented in this chapter. These include the calculation of the passive components used in the DC filters, AC filters, the inductor in the boost converter, buck converter and the X-shaped impedance

circuits. The criteria of the ripple limit and the suitable cut-off frequency are used for the design of the DC components whilst the minimum power factor criteria and the suitable cut-off frequency are used for the design of the AC components.

The performance of the inverter topologies under investigation in this chapter will be evaluated and compared against the proposed CSI with series AC capacitors topology in Chapter 6.

Chapter 5

The Current Source Inverter with Series AC Capacitors

In Chapter 4, six power inverter topologies selected from those currently evaluated in research papers for three-phase transformerless, grid-tied PV applications have been presented. In this chapter, an alternative candidate topology, referred as the Current Source Inverter with series AC capacitors (CSI+SCaps), is proposed. This topology was firstly used in [38] to reduce voltage stress on semiconductor devices for the shunt active power filter application but the topology is firstly introduced for the PV inverter application in this thesis. This proposed topology is a modified topology of the CSI topology. Three AC capacitors are added in series connection with each AC phase of the standard CSI as shown in Figure 5.1. The topology utilises the advantages of the CSI topology in order to achieve a simple circuit, potential high efficiency with a single stage power conversion and operation over the whole (down to zero) voltage range of the PV array without the need of additional components. The added AC capacitors are used to improve the efficiency of the inverter during operation with a low PV voltage and to provide better AC power quality, lower voltage stress on the circuit components and low input PV current/voltage ripple compared to the standard CSI topology.

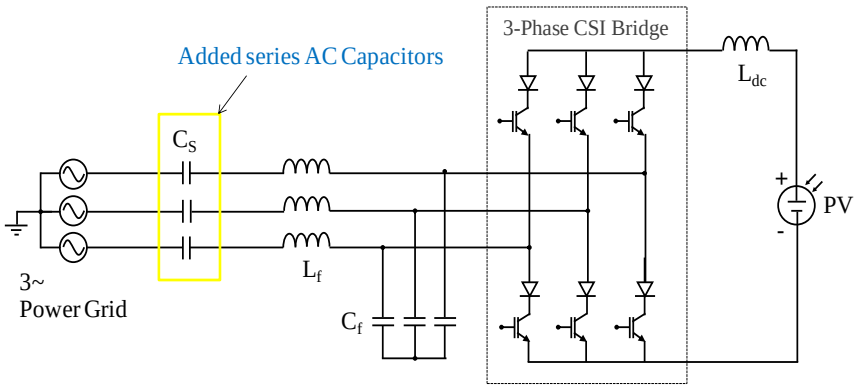


Figure 5.1 Circuit configuration of the CSI with series AC capacitors (CSI+SCaps)

This chapter contains details of the operating characteristics, analytical model and equations, modulation and control methodologies, design of series AC capacitors and other potential applications for the CSI+SCaps topology. The performance of this topology will be evaluated via simulation in Chapter 6, which will be compared against the six other inverter topologies that have been presented in Chapter 4.

5.1 Fundamental Characteristics

When the standard CSI topology is used to interface the PV array to the grid, the voltage across the AC side of the topology is the grid voltage. This AC voltage level cannot be changed to match the large variation of the voltage level of the PV array at the DC side as shown in Figure 5.2. This leads to an inefficient power conversion and non-optimum voltage transfer between the DC side and the AC side across the inverter.

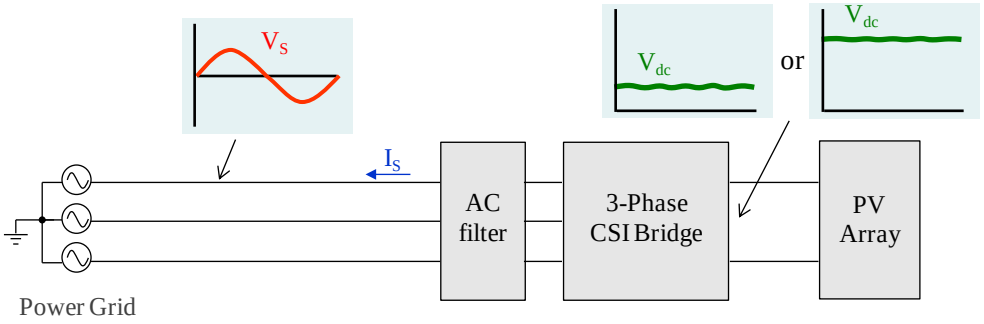
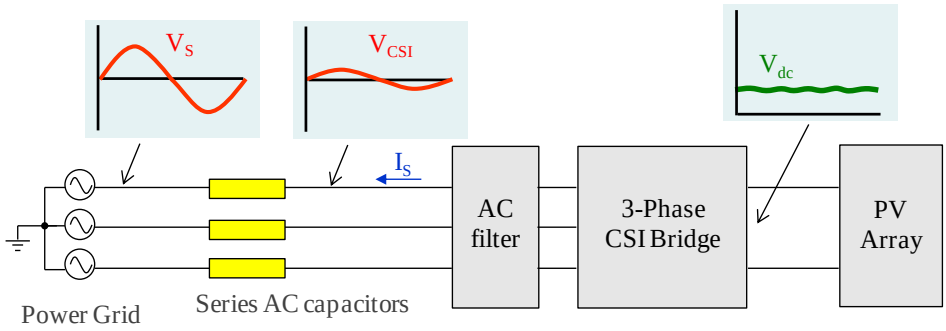
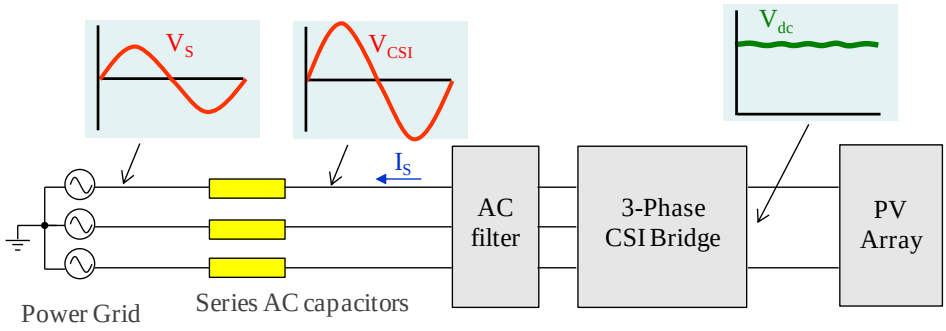


Figure 5.2 Standard CSI when operating with a low or high PV voltage level

In contrast, the presence of the series AC capacitors in the CSI+SCaps topology allows the voltage level at the AC side of the topology to be adjusted. This is possible because when the AC current flows through the series AC capacitors, the voltage across the capacitors will be created. This voltage can be used to add to or subtract from the grid voltages and thus provide an adjustable phasor voltage seen at the AC side of the inverter to be low or high to respond to a low or high PV voltage level at the DC side as shown in Figure 5.3. As a result, the CSI+SCaps has a possibility to always operate with an optimum voltage transfer between the DC side and the AC side.



(a)



(b)

Figure 5.3 CSI+SCaps when operating with (a) a low PV voltage level and (b) high PV voltage level

5.2 Analytical Model and Equations

To facilitate the explanation of the operation and control methodologies and the design of the series AC capacitors used for the CSI+SCaps, its analytical model and equations are derived. The model based on the phasor diagram is used to show magnitudes and phases of the AC side parameters when the CSI+SCaps operates in different situations whilst the equations are used in the control methodologies and the design of the series AC capacitors.

The circuit configuration of the CSI+SCaps in Figure 5.1 can be represented by the per-phase equivalent circuit as shown in Figure 5.4. The terms of the parameters shown in the figure are described in Table 5.1. These parameters will be used to derive the model and equations for the CSI+SCaps topology.

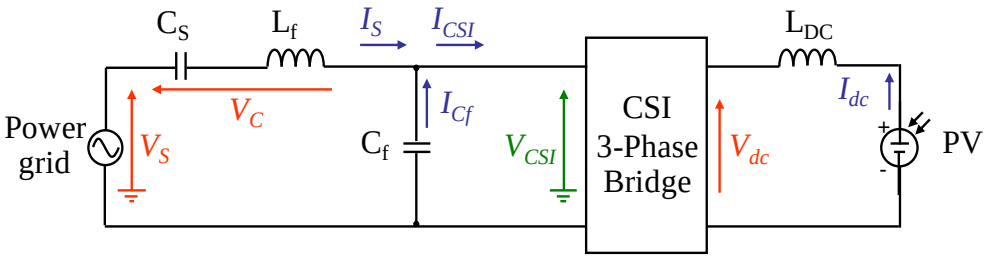


Figure 5.4 Per-phase equivalent circuit of the CSI+SCaps topology

Parameter	Description
V_S	grid voltage phasor
I_S	AC line current phasor
V_C	AC voltage phasor across the series AC capacitor C_S and the filter inductor L_f
I_{Cf}	AC current phasor drawn by the filter capacitor C_f
V_{CSI}	AC voltage phasor seen at the AC side of the inverter
I_{CSI}	AC current phasor seen at the AC side of the inverter
V_{dc}	DC-link voltage
I_{dc}	DC-link current

Table 5.1 Parameters used for the analysis of the analytical model and equations of the CSI+SCaps topology

By applying the phasorial summation theorem for the parameters on the AC side of the equivalent circuit in Figure 5.4, a model based on the phasor diagram for the CSI+SCaps can be derived as shown in Figure 5.5 and the magnitudes of the phasors can be derived as shown in (5.1)-(5.4); where θ and φ refer to the phase displacement angle between V_S and I_S (power factor angle) and between V_{CSI} and I_{CSI}.

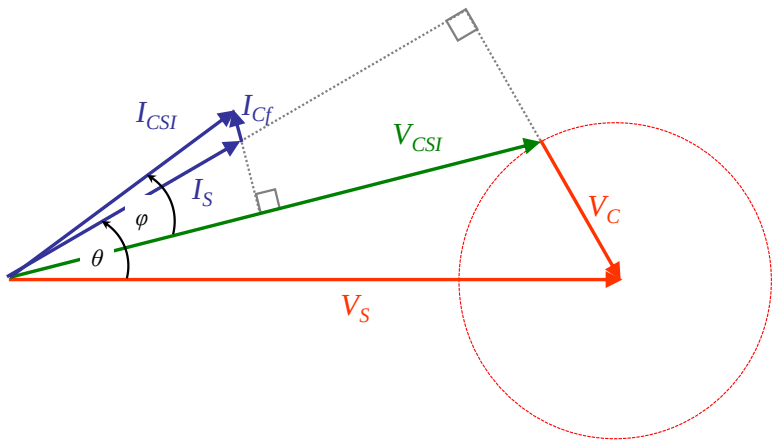


Figure 5.5 Phasorial diagram representation of the analytical model of the CSI+SCaps

$$V_C = I_S X_C \qquad ; X_C = (1/\omega C_s) - \omega L_f \tag{5.1}$$

$$V_{CSI} = \sqrt{V_S^2 + (I_S X_C)^2 - 2V_S I_S X_C sin\theta} \tag{5.2}$$

$$I_{Cf} = \frac{1}{X_{Cf}} \cdot \sqrt{V_S^2 + (I_S X_C)^2 - 2V_S I_S X_C sin\theta} \quad ; X_{Cf} = (1/\omega C_f) \tag{5.3}$$

$$I_{CSI} = \sqrt{I_s^2 \left(1 + \frac{X_C}{X_{Cf}}\right)^2 + \left(\frac{V_S}{X_{Cf}}\right)^2 - 2I_S \left(1 + \frac{X_C}{X_{Cf}}\right)\left(\frac{V_S}{X_{Cf}}\right) sin\theta} \tag{5.4}$$

By applying the complex AC power theorem and using (5.2) and (5.4), the active (P_{CSI}) and reactive power (Q_{CSI}) seen at the AC side of the inverter can be derived as shown in (5.5) and (5.6).

$$P_{CSI} = \frac{3}{2} V_S I_S cos\theta \tag{5.5}$$

$$Q_{CSI} = -\frac{3}{2}\left[V_S I_S sin\theta \left(1 + \frac{2X_C}{X_{Cf}}\right) + \frac{V_S^2}{X_{Cf}} + I_S^2 X_C \left(1 + \frac{X_C}{X_{Cf}}\right)\right] \tag{5.6}$$

When considering the situation of the power equilibrium between the AC side and DC side of the inverter, the components of the AC current phasor (i_{sd} and i_{sq}) can be derived as shown in (5.7) and (5.8); where P_{dc} is the power seen at the DC side of the inverter. The components i_{sd} and i_{sq} are used in the modulation and control for the CSI+SCaps (see more detail in Section 5.3).

$$i_{sd} = I_S cos\theta = \frac{2P_{dc}}{3V_S} \tag{5.7}$$

$$i_{sq} = I_S sin\theta = -\left[\frac{V_S}{(X_{Cf}+2X_C)} + I_S^2 \cdot \frac{X_C X_{Cf}(X_{Cf}+X_C)}{V_S(X_{Cf}+2X_C)}\right] \tag{5.8}$$

The terms of the component i_{sq} in (5.8) can be simplified where the estimated value of the AC current (I_s) can be derived using the definition of CSI modulation index (m_i). The m_i is the control parameter used to provide the desired current transfer ratio between the DC side and the AC side for the CSI-type inverters, which is defined as the ratio of the AC current magnitude seen at the AC side of the inverter to the peak DC-link current seen at the DC side, as shown in (5.9). And by substituting (5.9) for (5.4), the estimated AC current can be derived as shown in (5.10).

$$m_i = \frac{I_{CSI}}{I_{dc}} \qquad ; 0 < m_i \leq 1 \tag{5.9}$$

$$I_S = \frac{V_S sin\theta + \sqrt{\left(m_i I_{dc} X_{Cf}\right)^2 - (V_S cos\theta)^2}}{\left(X_{cf} + X_c\right)} \quad ; -\pi/2 \leq \theta \leq \pi/2 \tag{5.10}$$

The analytical model based on the phasor diagram is used to shown the magnitudes and phases of the AC side parameters when the CSI+SCaps operates in different operating points. The equations are used in the modulation and control for the topology presented in Section 5.3 and the design of the series AC capacitors presented in Section 5.5.

5.3 Modulation and Control Methodologies

Since there are no additional switches or switching states used in the CSI+SCaps when compared to the standard CSI, the modulation techniques used for the standard CSI topology (Section 4.3.3) can be used also for the CSI+SCaps topology. This section presents the control principle and the possible control methods that could be used for the CSI+SCaps topology.

5.3.1 Control Principle

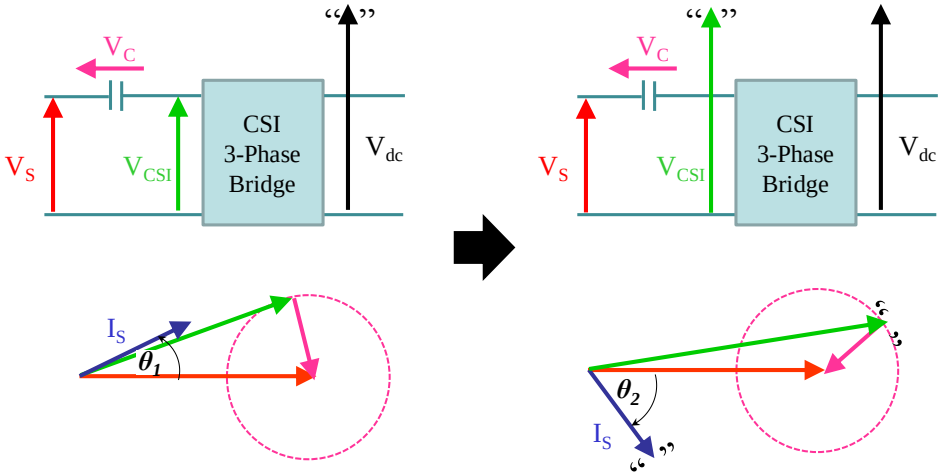
As presented in Section 5.1, in order to control the CSI+SCaps so that the AC voltage level seen at the AC side of the inverter can be adjusted to match the voltage level at the DC side, the voltage across the series AC capacitors has to be controlled. Since the magnitude of the series AC capacitor voltage is dependent on the AC current, as defined in (5.1), it means that the magnitude of this voltage can be controlled via the control of the AC current. By substituting (5.10) for (5.1), the magnitude of the voltage across the series AC capacitors (V_C) will be derived as shown in (5.11) whilst the phase of V_C can be derived from the phasor diagram shown in Figure 5.5, which is shown in (5.12).

$$V_C = \frac{V_S sin\theta + \sqrt{\left(mI_{dc} X_{Cf}\right)^2 - (V_S cos\theta)^2}}{\left(X_{cf} + X_c\right)} \cdot X_C \tag{5.11}$$

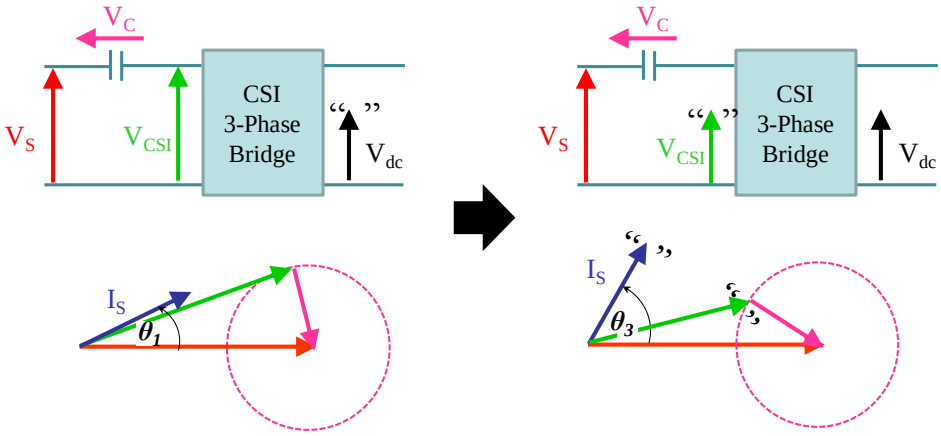
$$\angle V_C = \left(\theta - \frac{\pi}{2}\right) \tag{5.12}$$

It can be seen from (5.11) and (5.12) that for the given grid voltage (V_S), available DC-link current (I_{dc}) and known values of X_{Cf} and X_C, the magnitude and phase of the V_C can be controlled using the power factor angle (θ) and the modulation index (m_i).

Figure 5.6 shows how the power factor angle (θ) can be used to control the series AC capacitors (V_C) and provide the AC voltage at the AC side of the CSI+SCaps topology (V_{CSI}) matching the voltage level at the DC side (V_{dc}). In the situation that V_{dc} is high (Figure 5.6a), the leading of θ can be used to adjust the phase of V_C and increase V_{CSI} to be higher than the grid voltage (V_S) in order to match the high V_{dc}. Alternatively, in the situation that V_{dc} is low (Figure 5.6b), the lagging of θ can be used to adjust the phase of V_C and decrease V_{CSI} to be lower than V_s in order to match the low V_{dc}.



(a)



(b)

Figure 5.6 Diagrams to show how the power factor angle can control the AC voltage level of the CSI+SCaps topology to match (a) a high DC voltage level and (b) a low DC voltage level

Table 5.2 shows the range of the power factor angle (θ) required for a particular increase/reduction rate of V_{CSI} when compared to V_S; where θ_n (5.13) refers to the power factor angle that causes V_{CSI} to have the same magnitude as V_S, which is derived from (5.2),(5.4) and (5.10) by considering the different ratios between V_{CSI} and V_C.

$$\theta_n = sin^{-1}\left(\frac{X_C}{2X_{cf}} \cdot \sqrt{\frac{\left(\frac{mI_{dc}X_{cf}}{V_S}\right)^2 - 1}{\left(\frac{X_C}{X_{cf}}\right) + 1}}\right) \tag{5.13}$$

Ratio of V_{CSI}/V_S	Power Factor Angle (θ)
> 1	$\theta_n < \theta < \pi/2$
= 1	$\theta = \theta_n$
< 1	$-\pi/2 < \theta < \theta_n$

Table 5.2 Required power factor angle (θ) for a particular rate of V_{CSI}/V_S

Besides the power factor angle (θ), the magnitude of the AC line current (I_S) is also the important parameter that affects the level of V_C and V_{CSI}. The parameter that is used to control I_S is the modulation index (m_i) as shown in (5.1) and (5.10): the higher the modulation index, the higher the level of I_S and V_C, but the magnitude of I_S cannot be greater than the peak DC-link current (I_{dc}) as restricted by the definition of m_i (see (5.9)). Figure 5.7 shows the effect of I_S on the level of V_C and V_{CSI}. It can be seen that when θ is constant, a higher AC line current (I_{S2}) causes a larger series AC capacitor voltage (V_{C2}) but a smaller amplitude of V_{CSI} than a lower AC line current (I_{S1}).

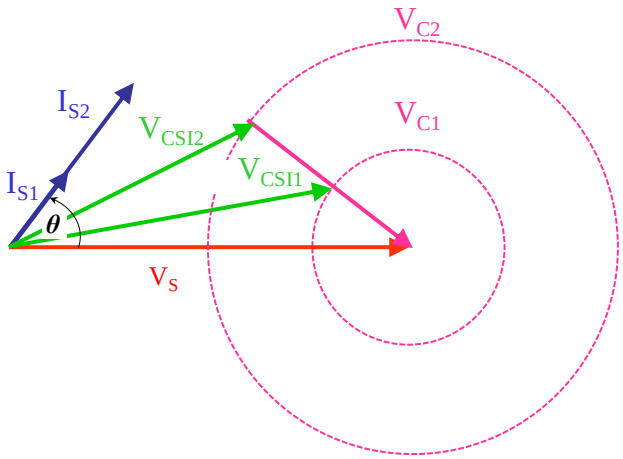


Figure 5.7 Diagrams to show how the magnitude of AC line current (I_S) can affect the voltage level at the AC side of the inverter (V_{CSI})

The control method for the CSI topology is normally designed to achieve unity AC power factor [103], and so called the *Unity Power Factor* (UPF) control (the schematic and operation of the UPF methods has been presented in Section 4.4.2). The UPF control can be used also for the CSI+SCaps topology. However, if the UPF control is used for the CSI+SCaps, the higher voltage level than the grid voltage will be created at the AC side of the inverter as shown by the phasor diagram in Figure 5.8. This high AC voltage may lead to higher voltage stress on the switching devices and increases switching loss.

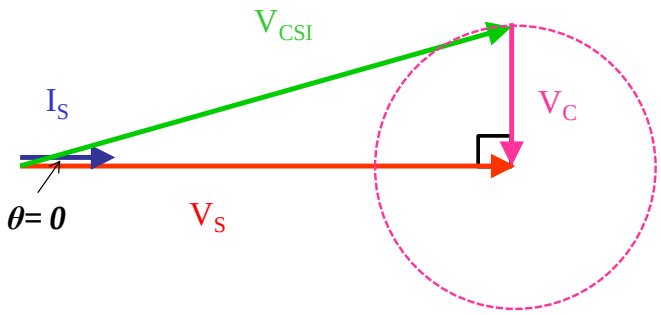


Figure 5.8 Phasor diagram when the CSI+SCaps operating with UPF control

In this section, two novel control methods suitable to be used for the CSI+SCaps topology are proposed: the *Minimum Switching Voltage* (MSV) control and the *Optimum Power Factor* (OPF) control. These methods have the tradeoffs between the minimum switching voltage (AC side voltage of the inverter) and the maximum power factor. The MSV control aims to control the CSI+SCaps topology to achieve the operation with the minimum switching voltage and the OPF control be used to achieve the operation at the optimum point between low switching voltage and high power factor.

5.3.2.1 Minimum Switching Voltage Control

The Minimum Switching Voltage (or MSV) control allows the CSI+SCaps topology to operate with the minimum switching voltage, by means of minimum voltage level across the inverter. This leads the topology to achieve the lowest voltage stress on the circuit components (power semiconductors, DC-link inductance). The control utilises the fact that the AC side or switching voltage (V_{CSI}) of the topology will have the minimum level when the maximum voltage across the series AC capacitor (V_C) is

created and hence can be used to subtract from the grid voltage (V_S), as described by (5.14):

$$V_{CSI(min)} = V_S - V_{C(max)} \tag{5.14}$$

Therefore, in order to maximise V_C, the series AC capacitors have to be rated to carry full AC line current (I_S), as described by (5.1). In practical term, this can be achieved by setting the CSI+SCaps topology to always operate with the maximum modulation index (m_i=1) so that the AC line current can fully draw the current from the DC side as suggested by (5.9).

Figure 5.9 presents the schematic of the CSI+SCaps topology when operating with the MSV control. The MSV control has the same schematic as the UPF control (Figure 4.18). The difference is that the AC line current components i_{sd}* and i_{sq}* calculated from (5.7) and (5.8) are used to be the reference current vector for the SVM-CSI modulator that sets the modulation index to operate near its maximum value (m_i* ≈1).

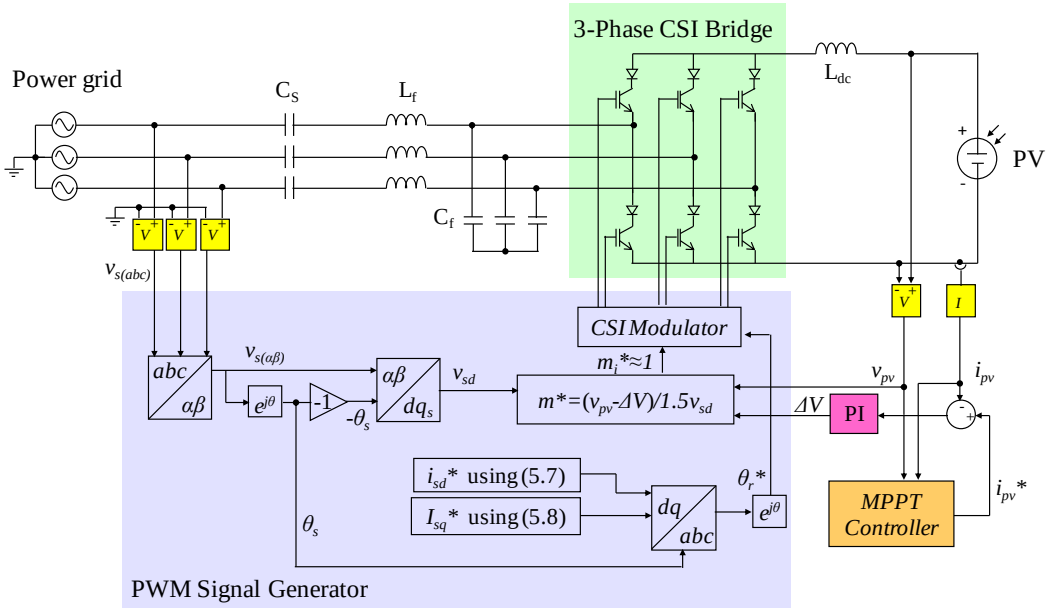


Figure 5.9 Schematic of the CSI+SCaps topology when operating with the MSV control

5.3.2.2 Optimum Power Factor Control

In some applications where the allowable range of the power factor is restricted, the *Optimum Power Factor* (or OPF) control would be more preferable. In this case both the modulation index (m_i) and the power factor angle (θ) are controlled in order to enable the CSI+SCaps topology to maximise the power factor and to minimise the switching voltage at the same time.

The point that the CSI+SCaps can provide the optimum balance between the minimum switching voltage (by means of the minimum amplitude of V_{CSI}) and the maximum power factor (by means of the highest value of $cos\theta$) is the point where the phasors V_S, V_C and V_{CSI} form a right triangle shape as shown in Figure 5.10. At this point, the phasor I_S will be in-phase with the phasor V_{CSI} and the ratio of V_{CSI}/V_S will be equal to $cos\theta$ (power factor). In practice, this control method can be achieved by controlling the AC line current phasor (I_S) to be always in phase with the AC voltage phasor seen at the AC side of the inverter (V_{CSI}).

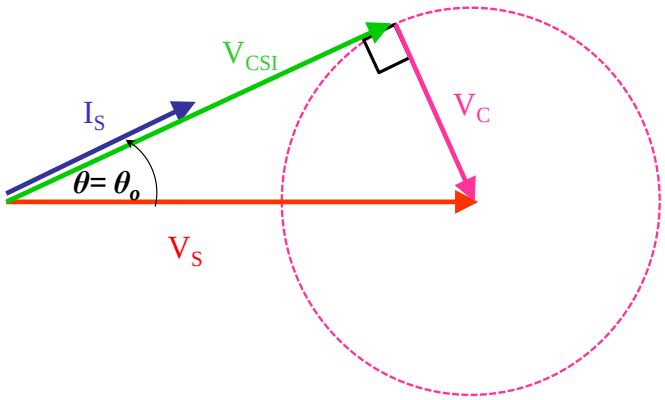


Figure 5.10 Phasor diagram for the CSI+SCaps operating with the OPF control

The concept of the OPF control has been firstly utilised for the control a shunt active power filter in [38]. The method directly measured the actual V_{CSI} from the circuit and used the phase-locked loop (PLL) techniques [104, 105] to synthesise the reference current vector for the SVM-CSI modulator to generate the switching signals, which is complicated and required additional V_{CSI} voltage transducers.
In this thesis, a simpler technique to implement the OPF control is proposed. Unlike in [34], the proposed technique directly synthesises the desired power factor angle

(θ_o*) from the measured DC-link current (I_{dc}) and the operating modulation index (m_i); where θ_o* can be determined using (5.15), which is derived from (5.2) when using $V_{CSI}/V_S=cos\theta$. Therefore, this control technique does not require any additional transducers for measuring V_{CSI}.

$$\theta_o = sin^{-1}\left(\sqrt{\frac{1-\left(\frac{X_{Cf}mI_{dc}}{V_S}\right)^2}{1-\left(\frac{X_{Cf}}{X_C}\right)^2}}\right) \tag{5.15}$$

Figure 5.11 shows the schematic of the CSI+SCaps when operating with the OPF control. The OPF control has the same control schematic as the UPF control. The difference is only that the reference current vector for the SVM-CSI modulator is synthesised using (5.10) and (5.15).

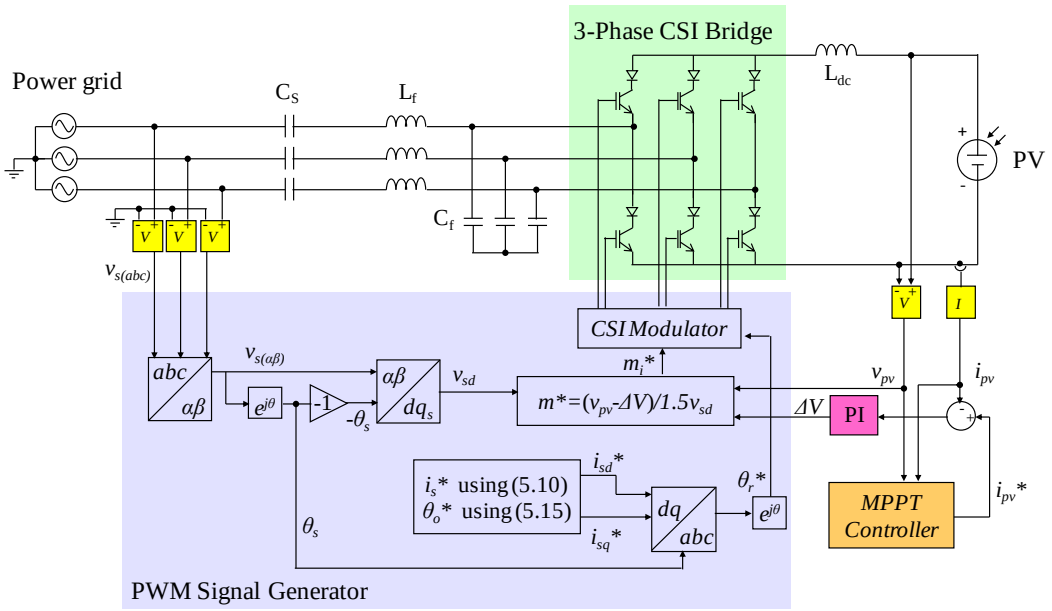


Figure 5.11 Schematic of the CSI+SCaps topology operating with the OPF control

5.3.3 DC-Link Current Control Design

This section presents the analysis for the design of a PI controller used in the DC-link current control. This control method can be used for both the standard CSI topology

and the CSI+SCaps topology. Figure 5.12 shows the DC side equivalent circuit of the topology; where R_S is the internal equivalent series resistance of the PV source (Section 2.4).

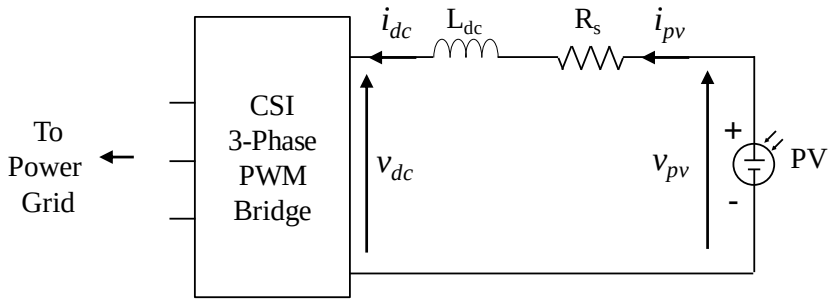


Figure 5.12 DC side equivalent circuit of the CSI-type topology

Applying the Kirchhoff's voltage law, the dynamic equation of the DC side equivalent circuit can be derived as shown in (5.16). Transferring (5.16) into the S-domain and rearranging terms, the open-loop DC-link current transfer function $G(s)$ will result as shown in (5.17).

$$-v_{pv} + i_{dc} \cdot R_s + L_{dc} \cdot \frac{di_{dc}}{dt} + v_{dc} = 0 \tag{5.16}$$

$$G(s) = \frac{i_{dc}(S)}{\Delta V(S)} = \frac{1}{sL_{dc}+R_s} \quad ; \ \Delta V(S) = v_{pv}(S) - v_{dc}(S) \tag{5.17}$$

Figure 5.13 shows the control diagram when a PI controller is used to control the DC-link current. The PI controller is expressed in the S-domain as shown in (5.18) [106]; where k_p and k_i refer to the proportional gain and the integral gain of the controller.

$$PI(s) = k_p + \frac{k_i}{s} \tag{5.18}$$

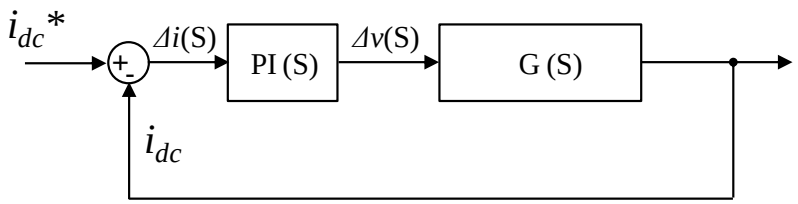


Figure 5.13 Diagram of the DC-link current control for the CSI-type topology

Applying the closed-loop control theorem and using (5.17) and (5.18), the closed loop transfer function ($G'(s)$) can be derived as shown in (5.19).

$$G'(s) = \frac{P(s)\cdot G(s)}{1+P(s)\cdot G(s)} = \frac{\frac{k_i}{L_{dc}}\cdot\left(\frac{Sk_p}{k_i}+1\right)}{S^2+S\left(\frac{R_S+k_p}{L_{dc}}\right)+\frac{k_i}{L_{dc}}} \tag{5.19}$$

If $k_i >> k_p$ is used, (5.19) can be simplified as shown in (5.20).

$$G'(s) = \frac{\frac{k_i}{L_{dc}}}{S^2+S\left(\frac{R_S+k_p}{L_{dc}}\right)+\frac{k_i}{L_{dc}}} \tag{5.20}$$

As a result of comparing (5.20) to the standard second order transfer function ($G_s(s)$) as shown in (5.21); where ω_n is the natural frequency and ξ is the damping factor. Hence,

$$G_s(s) = \frac{\omega_n^2}{s^2+2\xi\omega_n s+\omega_n^2} \tag{5.21}$$

Hence, k_p and k_i can be formulated as (5.22) and (5.23) respectively.

$$k_p = 2\xi\omega_n L_{dc} - R_s \tag{5.22}$$

$$k_i = \omega_n^2 L_{dc} \qquad \text{; where } k_i >> k_p \tag{5.23}$$

The selection of ζ and ω_n will be made by considering the specifications that define the step response shown in Figure 5.14. The parameter M_p refers to the peak overshoot (in % of the final value), t_p to the time to the peak value, τ to the equivalent time constant and t_r to the rise time (from 0.1 to 0.9 of the final value); the time unit is in seconds. These parameters are defined as shown in (5.24)-(5.27) [106].

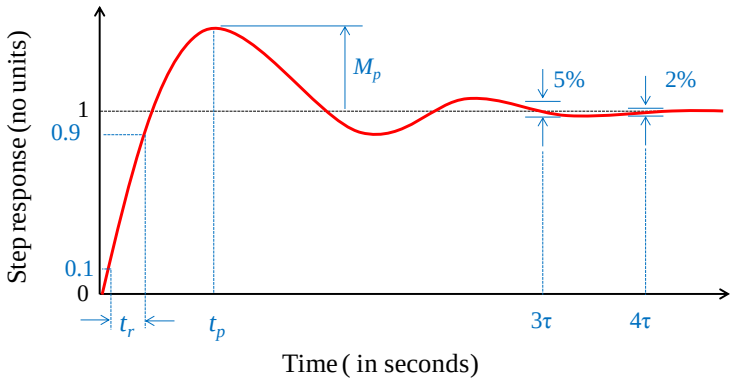


Figure 5.14 Specification parameters for the step response

$$M_p = exp\left(\frac{-\xi\pi}{\sqrt{1-\zeta^2}}\right) \times 100\% \tag{5.24}$$

$$t_p = \frac{\pi}{\omega_n\sqrt{1-\zeta^2}} \tag{5.25}$$

$$\tau = \frac{1}{\zeta\omega_n} \quad ; \text{settles to 5\% of the final value in } 3\tau = \frac{3}{\zeta\omega_n}$$
$$; \text{settles to 2\% of the final value in } 4\tau = \frac{4}{\zeta\omega_n} \tag{5.26}$$

$$t_r \simeq \frac{3\zeta}{\omega_n} \quad ; \text{for } 0.6 < \zeta < 0.9 \tag{5.27}$$

Figure 5.15 shows the simulation waveforms of the DC-link current demand (I_{dc}*) and the corresponding DC-link current (I_{dc}) when the PI controller with the design specifications and the simulation parameters in Table 5.3 are used for the CSI+SCaps topology.

Item	Parameter	Value and Unit
Design specifications	ω_n	350 rad/sec
	ζ=0.7	0.7
Simulation parameters	V_S	415V/50Hz
	V_{dc}	425V
	L_{dc}	10mH
	R_S	0.5Ω
	C_S	500μF
Calculated PI parameters	k_p= 4.4 k_i=1225	-

Table 5.3 Design specifications and simulation parameters used to observe functionality of the designed PI controller

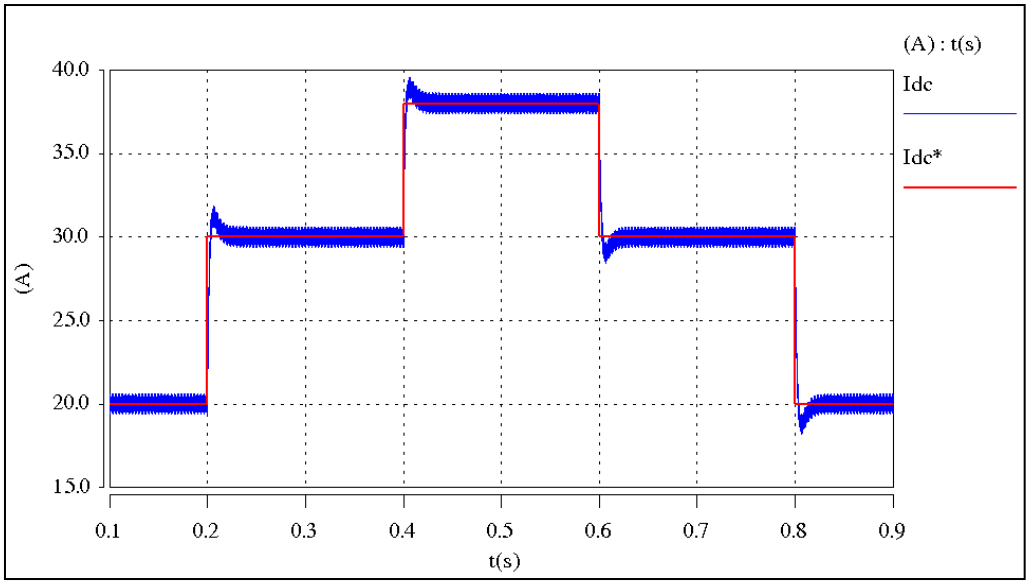


Figure 5.15 Comparison of the DC-link current demand (I_{dc}*) and the corresponding DC-link current (I_{dc}) obtained from the CSI+SCaps when operating with the PI controller using the simulation parameters from Table 5.3

Table 5.4 shows the comparison of the step response parameters M_p, t_p, τ(2%) and t_r between the calculation using the design specifications (5.24)-(5.27) and the measured values from the waveform in Figure 5.15.

Parameter	Design Value	Measured Value	Unit
M_p	4.6	4.9	%
t_p	12.5	11.8	msec
τ(2%)	16.5	17	msec
t_r	6	6.5	msec

Table 5.4 Comparison of step response parameters between the design values and the measured values

It can be seen from Figure 5.15 that the designed PI controller can control the DC-link current levels to have the same final levels as demanded. Similar results between the design and the measured values of the step response parameters in Table 5.4 confirms that the DC-link current PI controller design presented in this section can provide the correct response as the design specifications require.

5.4 Design of the Series AC Capacitors

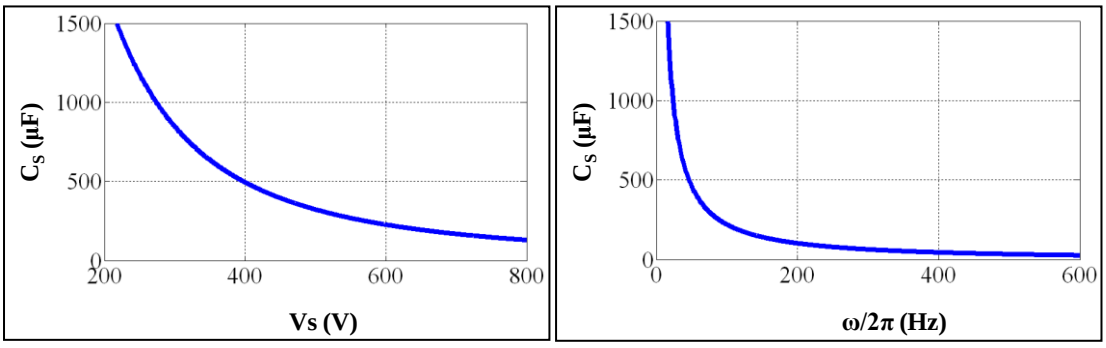
This section presents detailed analysis and design of the series AC capacitors used in the CSI+SCaps topology. All other circuit components used in the topology can be designed using the procedures presented in Section 4.5.

To facilitate the design, the parameter *a* is defined, which is the ratio of the magnitude of the voltage seen at the AC side of the inverter to the magnitude of the grid voltage, as shown in (5.28). This parameter is used to indicate how much the AC side voltage level of the inverter is reduced in comparison to the grid voltage level. By substituting (5.28) for (5.2) and using (5.5), the required value of the series AC capacitors can be formulated as shown in (5.29). Therefore, the required value of the series AC capacitor is dependent on grid voltage and frequency (V_S and ω), power factor angle (θ), required AC voltage level (a), load power (P_{dc}) and AC filter inductance (L_f).

$$a = \frac{V_{CSI}}{V_S} \qquad ; a \geq 0 \tag{5.28}$$

$$C_S = \frac{2P_{dc}}{2\omega^2 L_f P_{dc} + 3\omega V_S^2 \cos\theta\left(\sin\theta + \sqrt{a^2 - \cos^2\theta}\right)} \tag{5.29}$$

Figures 5.16a and 5.16b show the required value of the series AC capacitors for the different grid voltage and frequency levels. It can be seen that a smaller AC capacitor is required for a higher grid voltage and a higher grid frequency level. This implies that a smaller size of series AC capacitors could be required for aerospace and aircraft applications where high supply frequency of 400Hz is usually used [107].



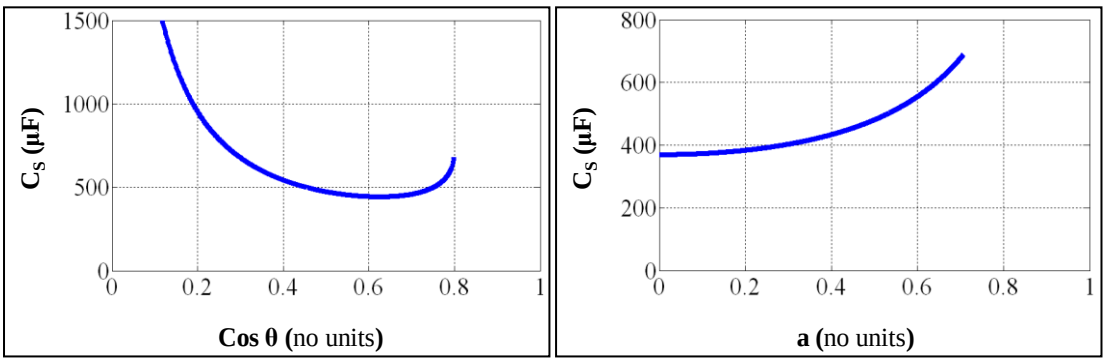
(a) (b)

Figure 5.16 Values of the series AC capacitors required for different (a) grid voltage V_S and (b) grid frequency ω; where $\theta = \pi/4$, a=0.8, P_{dc}=20kW and L_f=1mH

Figures 5.17a and 5.17b show the required value of the series AC capacitors for the different power factor (cosθ) and different AC voltage (a). It can be seen that:

- The largest size of the series AC capacitors is required when the power factor ($cos\theta$) is low and then becomes smaller when the power factor has a low-medium value. The capacitors' size becomes larger again when the power factor has a medium-high value and reaches the largest size in the high power factor range at the point where "$cos\theta=a$"; (see Figure 5.17a where $cos\theta=a=$ 0.8 for this case).

- A smaller series AC capacitor is required for a lower level of the required AC side voltage (a). If differentiating the terms in (5.29) by a, it will be found that the maximum value of the series AC capacitors will be determined at the point where "$a=cos\theta$" (see Figure 5.17b where $a= cos\theta=$ 0.707 for this case).



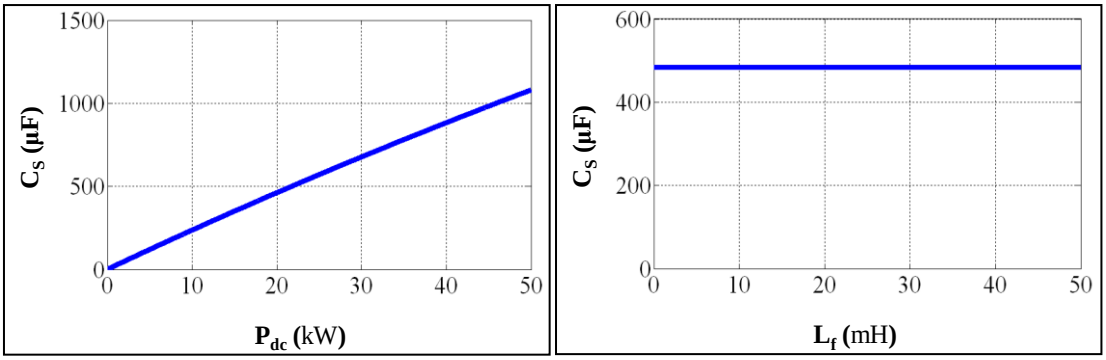
(a) (b)

Figure 5.17 Values of the series AC capacitors required for different (a) power factor θ and (b) required AC side voltage compared to the grid voltage (a); where Vs=415V/50Hz, $\omega/2\pi$=50Hz, P_{dc}=20kW and L_f=1mH

Figures 5.18a and 5.18b show the required value of the series AC capacitors for the different load power (P_{dc}) and different AC filter inductance (L_f). It can be seen that:

- A larger series AC capacitor is required for a higher operating load power.

- The value of AC filter inductance (L_f) does not affect to the required size of the series AC capacitors.



(a) (b)

Figure 5.18 Values of the series AC capacitors required for different (a) load power (P_{dc}) and (b) different AC filter inductance (L_f); where Vs=415V/50Hz, ω/2π=50Hz, θ= π/4 and a=0.8

As mentioned previously and shown in Figure 5.17, the largest size of the series AC capacitors is required for the condition where $a = cos\theta$. Using this constraint for (5.29), the largest value of the series AC capacitors that is required for a particular level of the AC side voltage of the inverter can be formulated as shown in (5.30).

$$C_{s,max} = \frac{2P_{dc}}{2\omega^2 L_f P_{dc} + 3\omega V_s^2 a\left(\sqrt{1-a^2}\right)} \tag{5.30}$$

Figure 5.19 shows the plots of (5.30), which indicate the maximum values of the series AC capacitors required for the different AC side voltage of the inverter ($0 < a \leq 1$) and different DC load power (P_{dc}) levels.

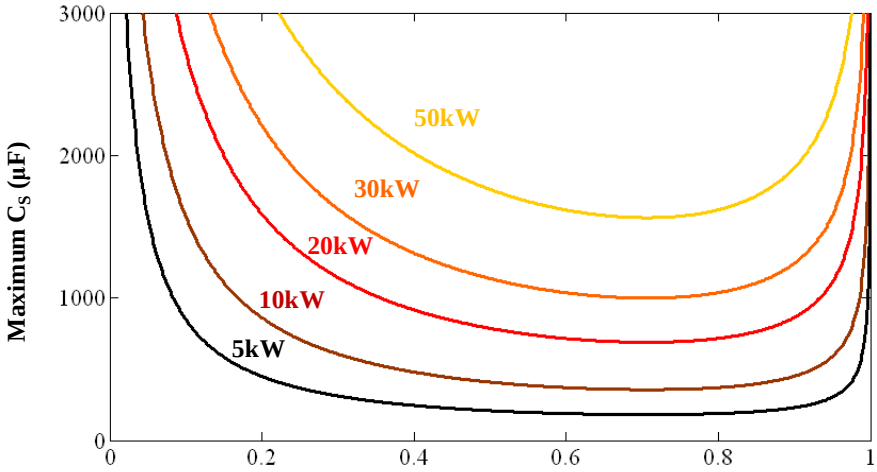


Figure 5.19 Maximum values of the series AC capacitor required for different AC side voltage of the inverter and different load power levels; V_S=415V/50Hz, L_f=1mH

It can be seen from Figure 5.19 that the size of the series AC capacitors required for all the load power levels can be minimised when the required AC side voltage of the inverter is in the range of 0.5-0.9 when compared to the grid voltage. In fact, this reduced voltage range is the required operating range for the grid-tied PV inverters since it is the range where the PV array delivers maximum output power (see more detail in Section 3.1). This means that the reduced sizes of the series AC capacitors are even favoured for practical applications.

5.5 Operating Results of the CSI with Series AC capacitors

In Section 5.3 three alternative control methodologies for the CSI+SCaps (UPF, MSV and OPF control) have been presented. In this section the simulation results of the CSI+SCaps when operating with these control methodologies are presented. There are two operating scenarios considered in this simulation work: the operation under normal grid voltage and the operation under low grid voltage sags.

5.5.1 Operating Results under Normal Grid Voltage Conditions

As mentioned in Section 3.1, under normal grid voltage the grid-tied PV inverters are required to operate at the maximum power points (MPP) of the PV array as well as at/near the maximum PV voltage (no load voltage) where the inverters start-up their operation. In this section the operating results of the CSI+SCaps when operating with the UPF, MSV and OPF control at three different MPPs (100%, 50% and 10% power levels) and near no load PV voltage are presented. The results of the standard CSI with the UPF control when operating at the same points are also presented and used to compare with the results of the CSI+SCaps.

5.5.1.1 Operating Results at Different Power Levels

Figure 5.20 presents three operating points (OP1, OP2 and OP3) that are used to observe the performance of the CSI+SCaps with the UPF, MSV and OPF control and the standard CSI with the UPF control when operating with different power levels at MPPs (100%, 50% and 10%). Table 5.5 presents the conditions and parameters used in this simulation. The value of the series AC capacitors is calculated using (5.30).

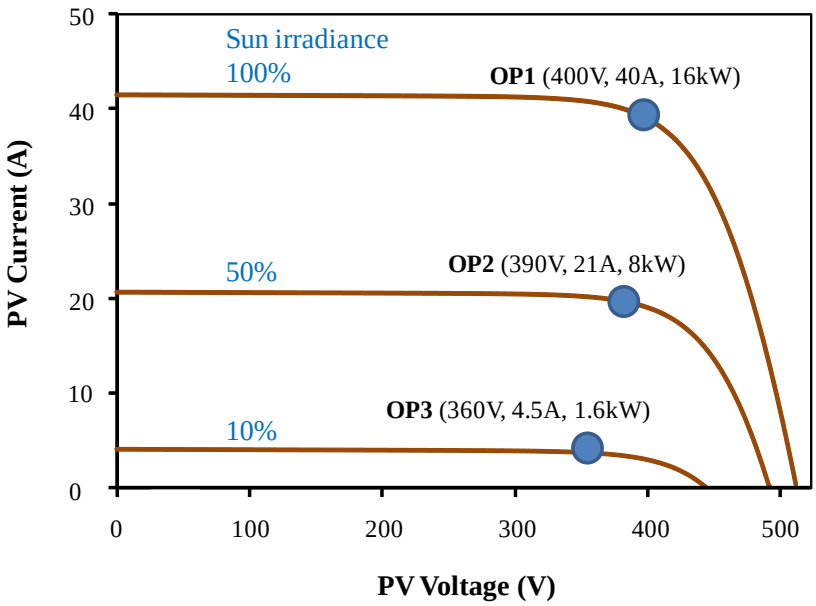


Figure 5.20 Three operating points (OP1, OP2 and OP3) used to observe the performance of the inverter topologies under investigation at different power levels

Inverter Topology	Circuit Components				Grid-PV Specifications	
	L_f/ph	C_f/ph	C_S/ph	L_{dc}	Grid	PV Array
Standard CSI	1mH	10µF	-	10mH	3-phase 415V/50Hz	22 strings of 24 series connected PV panels: module BP SX30 P_{max}=16kW, V_{max}=508V and I_{max}=45A @STD 25°C
CSI+SCaps	1mH	10µF	560µF	10mH		

Table 5.5 Simulation model parameters used to observe the performance of the inverter topologies under investigation at different power levels

Figures 5.21, 5.22 and 5.23 show the simulation waveforms at the DC side and the AC side of the standard CSI and the CSI+SCaps when they operate at the operating points and simulation conditions shown in Figure 5.20 and Table 5.5. The DC side waveforms are the PV voltage (V_{pv}), the PV current (I_{pv}) and the DC-link voltage (V_{dc}) and the AC side waveforms are the AC side inverter voltage (V_{CSI}), the grid voltage (V_S) and the AC line current (I_S). The mean values and the ripple of the PV voltage and current as well as the peak values of the DC-link voltage/current according to the DC side waveforms are presented in Table 5.6, whilst the equivalent phasor diagrams according to the AC side waveforms are presented in Table 5.7.

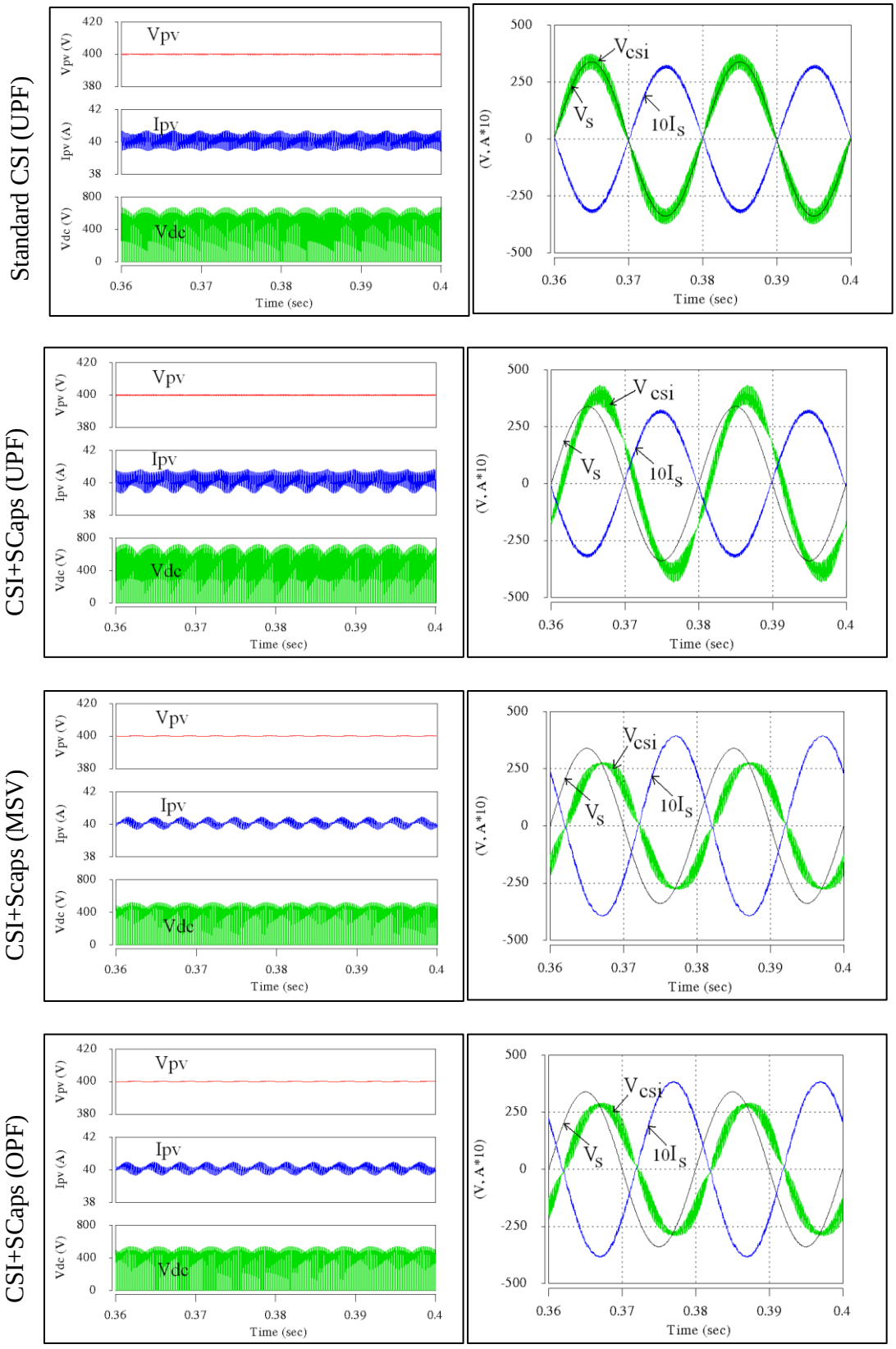


Figure 5.21 DC side (left) and AC side (right) simulation waveforms of the standard CSI with UPF control and the CSI+SCaps with UPF, MSV and OPF control when operating at 100% load power (OP1)

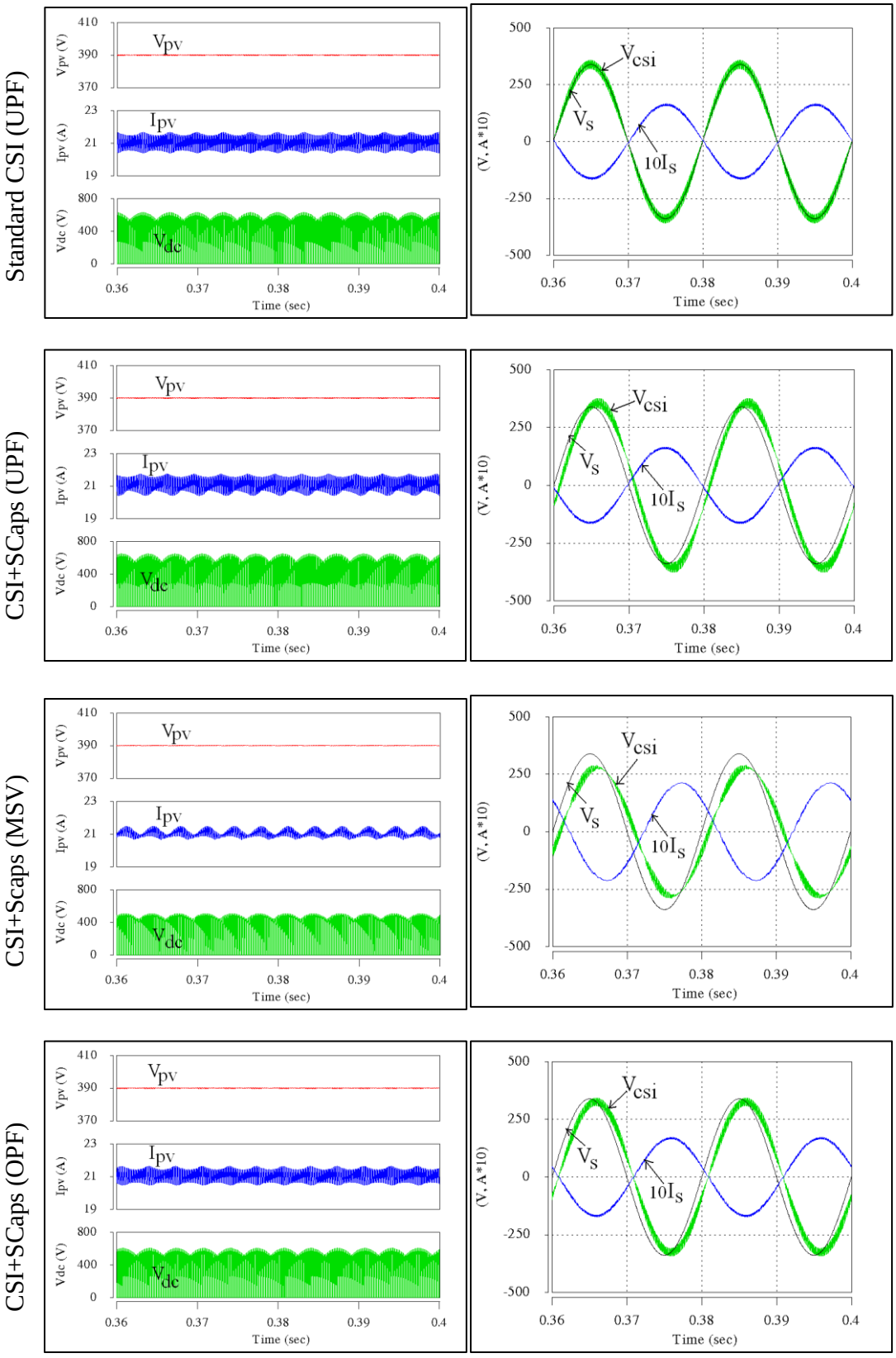


Figure 5.22 DC side (left) and AC side (right) simulation waveforms of the standard CSI with UPF control and the CSI+SCaps with UPF, MSV and OPF control when operating at 50% load power (OP2)

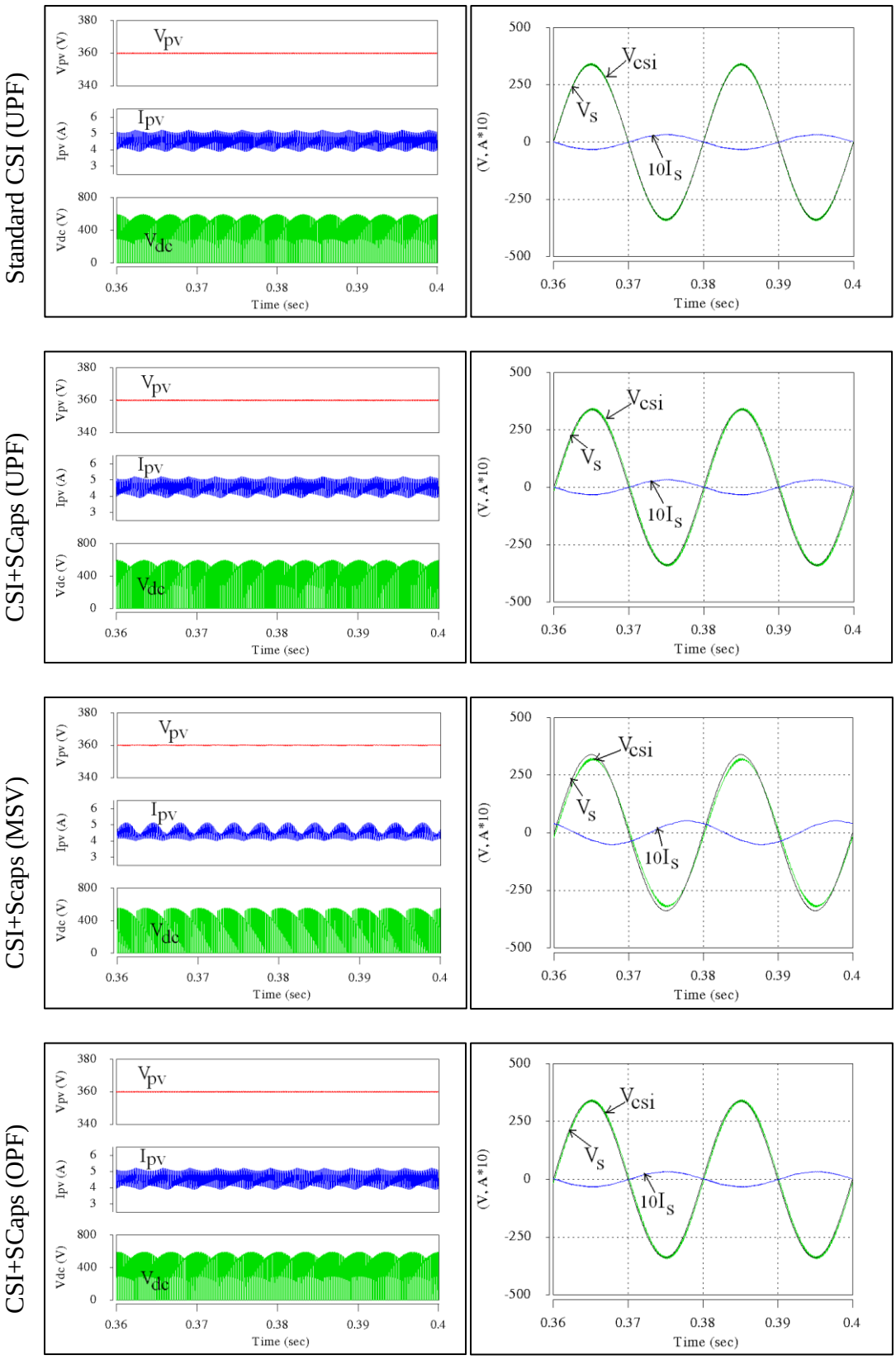


Figure 5.23 DC side (left) and AC side (right) simulation waveforms of the standard CSI with UPF control and the CSI+SCaps with UPF, MSV and OPF control when operating at 10% load power (OP3)

PV Operating Point	Topology and Control	Operating Results on the DC Side					
		V_{pv} (mean) (V)	I_{pv} (mean) (A)	$\%\Delta V_{pv}$ (ripple) (V)	$\%\Delta I_{pv}$ (ripple) (A)	V_{dc} (peak) (V)	I_{dc} (peak) (A)
OP1 (MPP 100%)	Standard CSI (UPF)	400	40	0.2%	3.5%	673	40.7
	CSI+SC (UPF)	400	40	0.2%	4.3%	725	40.8
	CSI+SC(MSV)	400	40	0.1%	1.7%	520	40.5
	CSI+SC(OPF)	400	40	0.1%	2.3%	539	40.4
OP2 (MPP 50%)	Standard CSI (UPF)	390	21	0.2%	6.2%	633	21.7
	CSI+SC(UPF)	390	21	0.3%	6.7%	650	21.8
	CSI+SC(MSV)	390	21	0.1%	3.8%	510	21.5
	CSI+SC(OPF)	390	21	0.2%	5.2%	608	21.6
OP3 (MPP 10%)	Standard CSI (UPF)	360	4.5	0.2%	28.9%	595	5.2
	CSI+SC(UPF)	360	4.5	0.2%	28.9%	596	5.2
	CSI+SC(MSV)	360	4.5	0.1%	24.4%	558	5.1
	CSI+SC(OPF)	360	4.5	0.2%	28.9%	595	5.2

Table 5.6 Mean values and ripple of the PV voltage (V_{pv}) and current (I_{pv}) and the peak values of the DC-link voltage (V_{dc}) and current (I_{dc}) collected from the DC side waveforms shown in Figures 5.21, 5.22 and 5.23

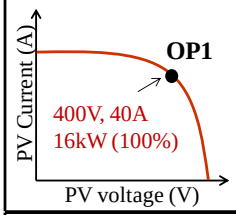
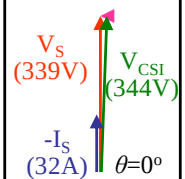
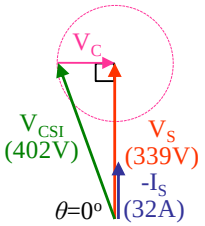
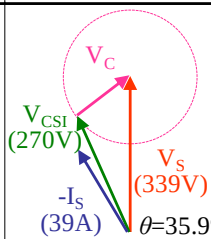
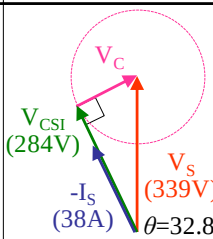
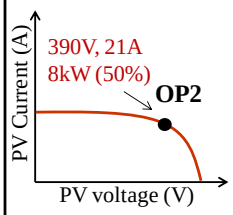
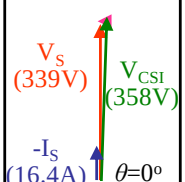
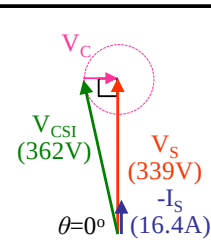
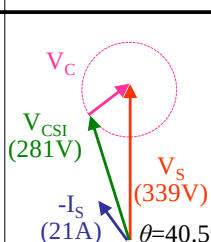
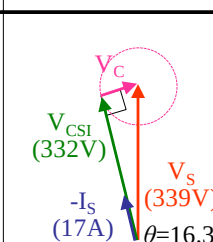
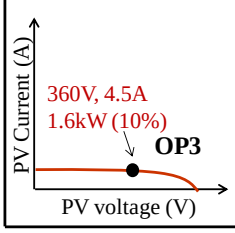
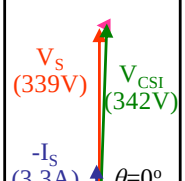
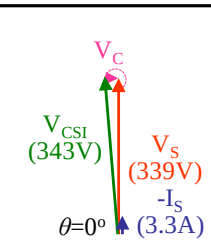
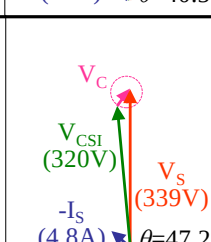
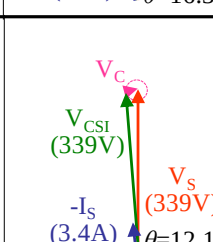
Operating Point	Standard CSI (UPF control)	CSI+SCaps		
		UPF control	MSV control	OPF control
				
				
				

Table 5.7 Equivalent phasor diagrams representing the operation of the standard CSI with UPF control and the CSI+SCaps with the UPF, MSV and OPF control according to the AC side waveforms shown in Figures 5.21, 5.22 and 5.23

It can be seen from Figures 5.21, 5.22 and 5.23 and from Tables 5.6 and 5.7 that:

- The standard CSI with the UPF control can achieve operations of unity power factor (I_S is in-phase to V_S) for all the investigated operating points. However, the AC side voltage of the inverter (V_{CSI}=342-358V) remains high and almost constant with the similar magnitude to the grid voltage (V_S=339V) even if the PV voltage level at the DC side is reduced (from 400V to 360V) when the load power decreases (from 16kW to 1.6kW). These mismatched voltage levels between the DC side and AC side can be adjusted by reducing the operating modulation index (m_i) but this can cause a high peak DC-link voltage (595-673V) at the DC side. In addition, reducing the modulation index means that larger zero voltage intervals are created on the PWM waveforms due to a longer operating time of the CSI null switching states (see Section 4.3.3). These larger zero voltage intervals require a longer time to be filtered and thus cause a high peak-to-peak ripple in the PV current (I_{pv}) waveforms for the standard CSI (3.5%-28.9%).

- The CSI+SCaps with the UPF control can achieve operations of unity power factor for all the investigated operating points as does the standard CSI. However, the voltage drop across the series AC capacitors is summed to the grid voltage that causes a larger AC side voltage (V_{CSI}=343-402V) compared to the standard CSI. This results in an even higher peak DC-link voltage (596-725V) and the higher peak-to-peak PV current ripple (4.3%-28.9%) for the CSI+SCaps with the UPF control compared to the standard CSI.

- With the control principle presented in Section 5.3.2.1, the CSI+SCaps with the MSV control can achieve low AC side voltage levels (V_{CSI}=270-320V) matching to the change of the PV voltage levels at the DC side. Therefore, the CSI+SCaps with the MSV control can always operate with the optimum voltage transfer ratio (by means of maximum modulation index, $m_i \approx 1$). This reflects by the lower peak DC-link voltage levels (520-558V) and the lower peak-to-peak PV current ripple (1.7%-24.4%) compared to the standard CSI. However, the power factor obtained from the CSI+SCaps with this control method is relatively low (0.68-0.81) compared to the standard CSI, which is

also reflected by a larger phase shift between V_S and I_S as shown in Figures 5.21, 5.22 and 5.23.

- With the control principle presented in Section 5.3.2.2, the CSI+SCaps with the OPF control can achieve low AC side voltage levels (V_{CSI}=284-339V) compared to the standard CSI and the CSI+SCaps with the UPF control, whilst providing an improved power factor (0.84-0.98) compared to the CSI+SCaps with the MSV control. However, the CSI+SCaps with the OPF control provides higher peak DC-link voltage (539-608V) and higher peak-to-peak PV current ripple (2.3-28.9%) compared to the CSI+SCaps with the MSV control.

If the level of the AC side voltage (V_{CSI}) and the peak DC-link voltage (V_{dc}) designate the level of the switching voltage stress across the inverters, the CSI+SCaps with the MSV control would provide the lowest switching voltage stress on the switching devices and thus potentially has the lowest switching losses; following by the CSI+SCaps with the OPF control, standard CSI with the UPF control and the CSI+SCaps with the UPF control. If the PV current ripple designates the size of the inductor required the DC-link current filter, the CSI+SCaps with MSV control would require the smallest size of the inductor; following by the CSI+SCaps with the OPF control, standard CSI with the UPF control and the CSI+SCaps with the UPF control. However, when evaluating in terms of power factor, the topologies with the UPF control should be used whilst the CSI+SCaps with the MSV control provides the lowest power factor among all the control methods. The CSI+SCaps with the OPF control would be the best choice if both high power factor and low switching voltage stress are considered. Table 5.8 presents a summary for the above comparisons.

Comparison Item	Standard CSI (UPF)	CSI+SCaps (UPF)	CSI+SCaps (MSV)	CSI+SCaps (OPF)
Switching voltage stress	High	Highest	Lowest	Medium-Low
Size of the DC-link filter	Large	Largest	Smallest	Small
Power factor	Highest	Highest	Lowest	Medium-Low

Table 5.8 Comparison of the potential switching voltage stress, size of DC-link filter and power factor among the standard CSI with the UPF control and the CSI+SCaps with the UPF, MSV and OPF control

5.5.1.2 Operating Results during Start-up

This section presents the simulation results when the standard CSI with the UPF control and the CSI+SCaps with the UPF, MSV and OPF control operating near no load voltage (maximum voltage) of the PV array where these inverter topologies start-up their operation. The simulation circuit components and the grid-PV specifications used in Section 5.5.1.1 and the operating point (OP4) at the PV voltage/current and power of 500V (98% of the no load voltage), 1A and 0.5kW are used in this simulation work. Figure 5.24 shows the simulation waveforms of the standard CSI and the CSI+SCaps when they operate with the aforementioned simulation parameters and operating point. The mean values and the ripple of the PV voltage and current and the peak values of the DC-link voltage/current according to the DC side waveforms in Figure 5.24 are presented in Table 5.9, whilst the equivalent phasor diagrams according to the AC side waveforms are presented in Table 5.10.

PV Operating Point	**Topology and Control**	**Operating Results on the DC Side**					
		V_{pv} (mean) (V)	**I_{pv}** (mean) (A)	**$\%\Delta V_{pv}$** (ripple) (V)	**$\%\Delta I_{pv}$** (ripple) (A)	**V_{dc}** (peak) (V)	**I_{dc}** (peak) (A)
OP4 (500V,1A,0.5kW)	Standard CSI (UPF)	500	1	0.1%	68.0%	578.3	1.36
	CSI+SC (UPF)	500	1	0.1%	73.0%	581.9	1.39
	CSI+SC(MSV)	500	1	0.1%	67.0%	578.0	1.36
	CSI+SC(OPF)	500	1	0.1%	67.0%	578.0	1.36

Table 5.9 Mean values and ripple of the PV voltage (V_{pv}) and current (I_{pv}) and the peak values of the DC-link voltage (V_{dc}) and current (I_{dc}) collected from the DC side waveforms shown in Figure 5.24

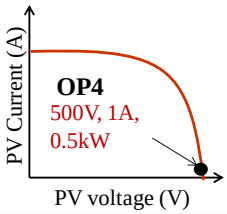
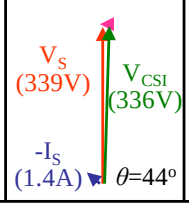
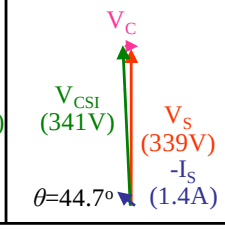
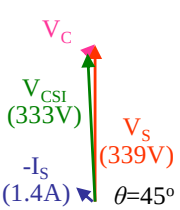
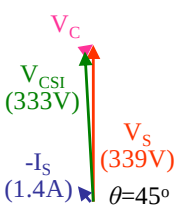
Operating Point	Standard CSI (UPF control)	CSI+SCaps		
		UPF control	MSV control	OPF control
				

Table 5.10 Equivalent phasor diagrams representing the operation of the standard CSI with UPF control and the CSI+SCaps with the UPF, MSV and OPF control according to the AC side waveforms shown in Figure 5.24

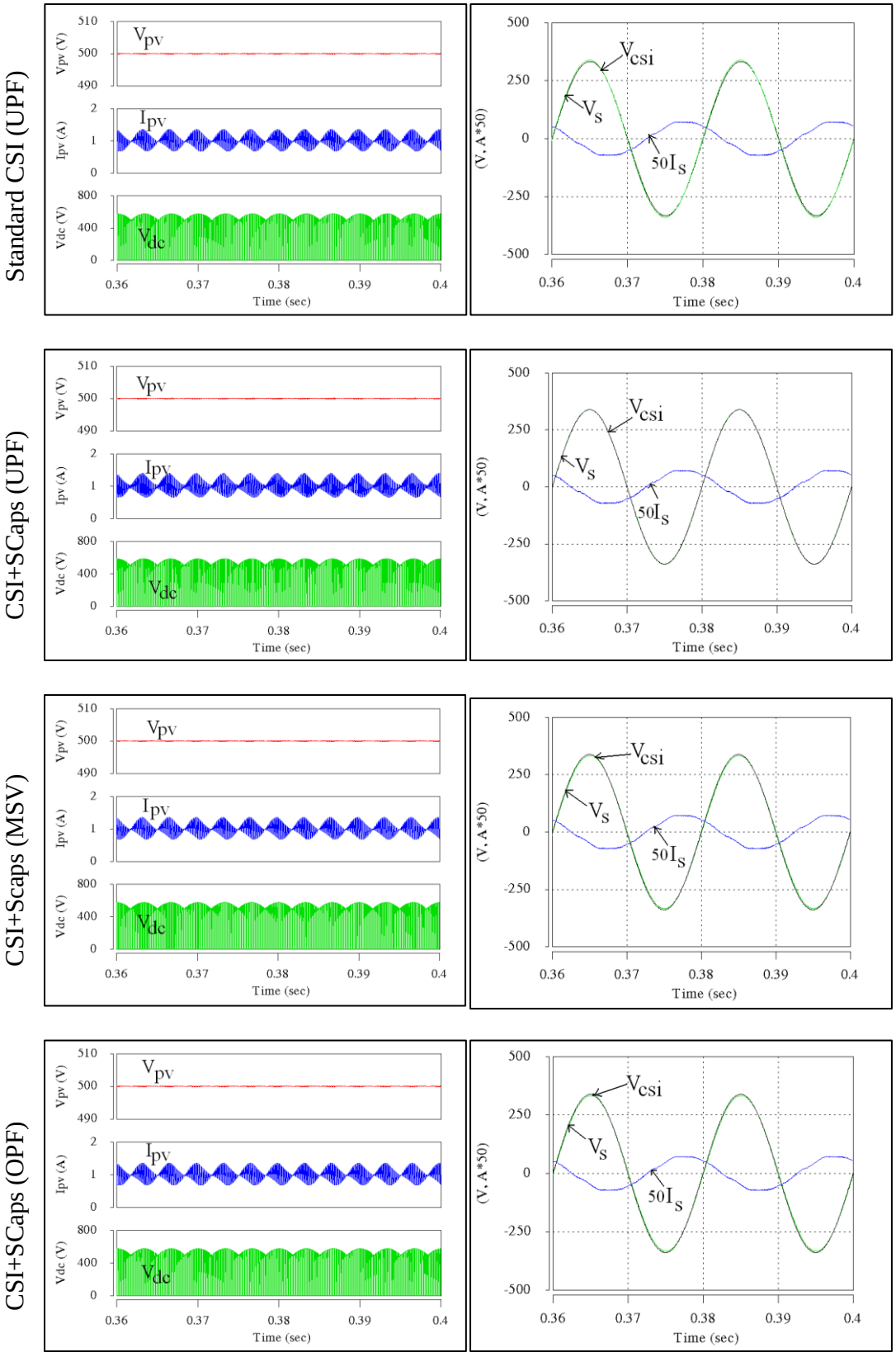


Figure 5.24 DC side (left) and AC side (right) simulation waveforms of the standard CSI with UPF control and the CSI+SCaps with UPF, MSV and OPF control when operating near no load PV voltage (OP4)

It can be seen from Figure 5.24 and Tables 5.9 and 5.10 that all the topologies and control methods have a similar operation when operating near no load PV voltage (OP4), reflected by the similar operating waveforms and operating phasor diagrams. This is because both of the standard CSI and the CSI+SCaps operate with a small fraction of the PV current (I_{pv}=1A) when operating near no load voltage (500V). The small PV current can be used to create only a small AC line current ($1.4A_{peak}$) and thus a small voltage across the series AC capacitors in the CSI+SCaps topology. This small series capacitor voltage therefore does not provide significant difference in the operation of the CSI+SCaps and their associated control methods compared to the standard CSI. Only a slight deviation of the AC side voltage amplitude (V_{CSI}=333-341V) compared to the grid voltage amplitude (V_S=339V). As the voltage across the inverter topologies are similar, the topologies operate close to the maximum modulation index and thus the phase shift between V_S and I_S (θ=44^o-45^o), by means of reducing power factor, have to be used to avoid over modulation.

5.5.2 Operating Results under Low Grid Voltage Sag Conditions

As mentioned in Section 3.2.2, grid-tied PV inverters should have the capability to ride-through low grid voltage faults (sags) to ensure safe and stable operation of the electrical network as required by the grid codes. The inverters should be able to stay-connected to the grid during a significant grid voltage fault (sag) for a given time before a trip is allowed, support the grid with reactive current during the fault and supply power to the grid immediately after the grid voltage fault clearance. In this section, the operating results of the CSI+SCaps in comparison to the standard CSI when operating during low grid voltage sags are presented.

As the reactive current is required at the grid side during the low grid voltage faults, the unity or optimum power factor control is no longer relevant. This leads the MSV control to be the most obvious choice for the CSI+SCaps whilst the phase shift between I_S and V_S must be used for the standard CSI. In this section, the operating results of the standard CSI and the CSI+SCaps when operating during low grid voltage sags are presented. The simulation circuit components and the PV array used in Section 5.5.1.1 are also used in this simulation work. Table 5.11 shows the simulation conditions for the grid and the PV array used in this simulation work. Two

operating points when the grid voltage dips by 30% (OP5) and 70% (OP6) from the nominal levels (415V/50Hz) are investigated; where the reactive current required to support the grid during these grid voltage dips based on the E.On Netz 2006 grid code [12] (see Figure 3.5) are used.

Operating Point	Grid Condition		PV Condition		
	V_S	Required Reactive Current	V_{pv}	I_{pv}	P_{pv}
OP5	30% dip	60% (equivalent to θ=54°)	200V	44.5A	8.9kW
OP6	70% dip	100% (equivalent to θ=90°)	~ 0V	45A	0kW

Table 5.11 Simulation parameters used to observe the operation of the standard CSI and the CSI+SCaps when operating during the grid voltage sages

Figures 5.25 and 5.26 show the simulation waveforms at the DC side and the AC side of the standard CSI and the CSI+SCaps when they operate at the operating points OP5 and OP6. The mean values and the ripple of the PV voltage and current as well as the peak values of the DC-link voltage/current according to the DC side waveforms are presented in Table 5.12, whilst the equivalent phasor diagrams according to the AC side waveforms are presented in Table 5.13.

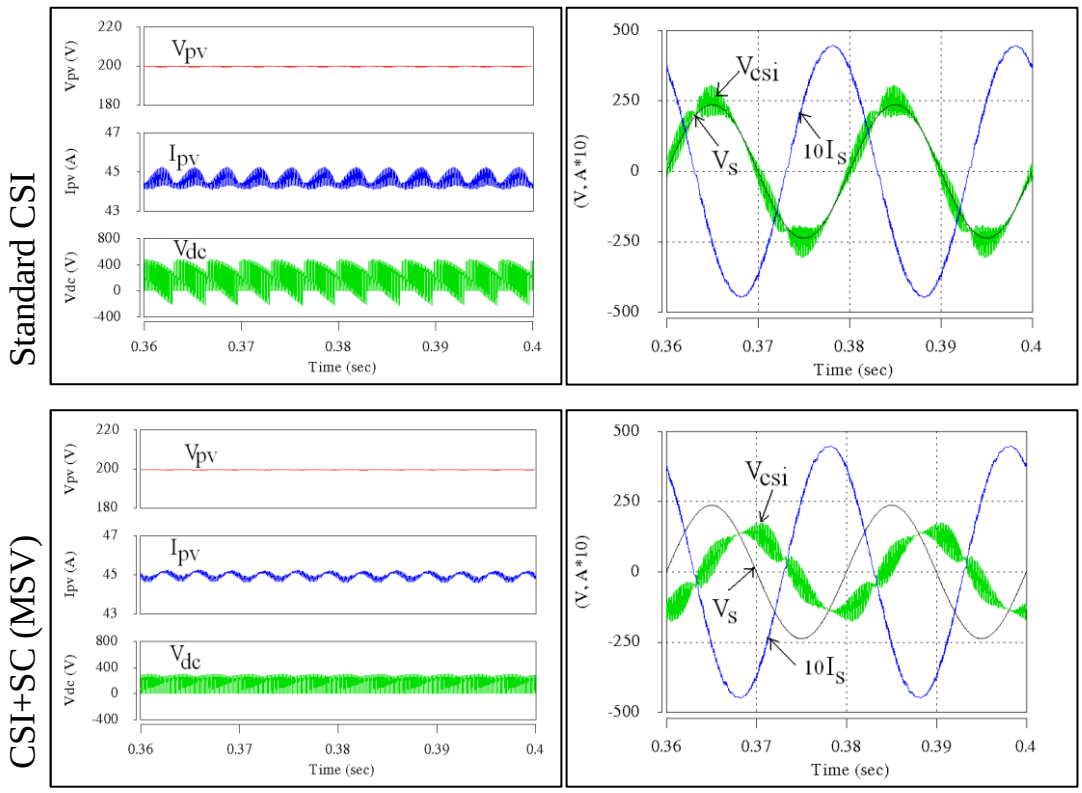


Figure 5.25 DC side (left) and AC side (right) simulation waveforms of the standard CSI and the CSI+SCaps when operating during 30% grid voltage dip (OP5)

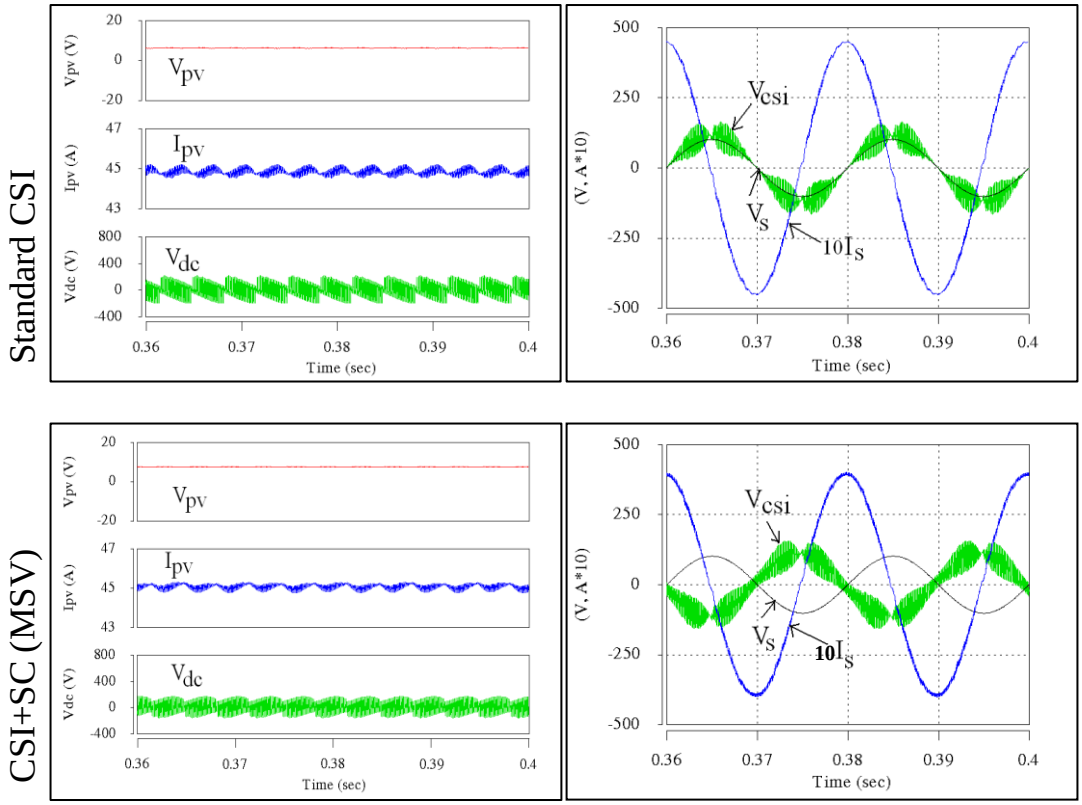


Figure 5.26 DC side (left) and AC side (right) simulation waveforms of the standard CSI and the CSI+SCaps when operating during 70% grid voltage dip (OP6)

Operating Point	Topology and Control	Operating Results on the DC Side					
		V_{pv} (mean) (V)	I_{pv} (mean) (A)	$\%\Delta V_{pv}$ (ripple) (V)	$\%\Delta I_{pv}$ (ripple) (A)	V_{dc} (peak) (V)	I_{dc} (peak) (A)
OP5	Standard CSI	200	44.5	0.3%	2.5%	488.4	45.2
	CSI+SC (MSV)	200	44.5	0.1%	1.6%	298.6	45.3
OP6	Standard CSI	6	45	5.0%	1.6%	220.1	45.4
	CSI+SC (MSV)	6	45	4.7%	1.1%	177.2	45.3

Table 5.12 Mean values and ripple of the PV voltage (V_{pv}) and current (I_{pv}) and the peak values of the DC-link voltage (V_{dc}) and current (I_{dc}) collected from the DC side waveforms shown in Figures 5.25 and 5.6

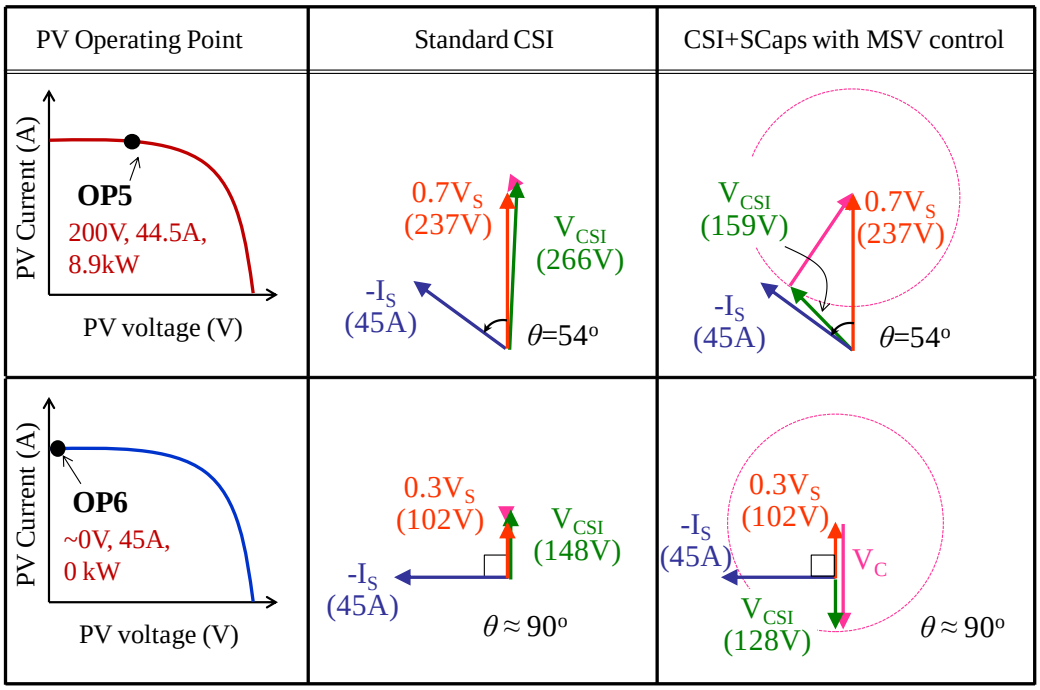


Table 5.13 Equivalent phasor diagrams representing the operation of the standard CSI and the CSI+SCaps with the MSV control according to the AC side waveforms shown in Figures 5.25 and 5.26

It can be seen from Figures 5.25-5.26 and Tables 5.12-5.13 that:

- During a grid voltage dip of 30% (OP5) and 70% (OP6), both the standard CSI and the CSI+SCaps can inject a reactive current of 60% and 100% of the rated current to support the grid as required. This are reflected by the phase shift between V_S and I_S of approximately 54^o when operating at OP5 and 90 ^{o} when operating at OP6 for both the converters, as shown in Figures 5.25-5.26 and Table 5.13.

- However, with the use of the voltage drop across series AC capacitors (V_C) which can be used to reduce the AC side voltage of the CSI+SCaps to match the low voltage level at the DC side as shown by the phasor diagrams in Table 5.13, the CSI+SCaps provides lower peak DC-link voltage levels (298.6V, 177.2V) compared to the standard CSI (488.4V, 220.1V) as well as lower PV current ripple levels (1.1-1.6%) compared to the standard CSI (1.6-2.5%) when operating at OP5 and OP6.

In summary, during a low grid voltage fault, both the standard CSI and the CSI+SCaps can inject the correct amount of the reactive current into the grid. However, the CSI+SCaps topology provides a lower peak DC-link voltage and a lower PV current ripple than the standard CSI. The performance of the CSI+SCaps and the standard CSI in terms of the capability to ride through the low grid voltage faults will be evaluated in Chapter 8.

5.6 Other Potential Applications

5.6.1 Reduced Component Voltage Rating

Since the CSI+SCaps topology has the capability to reduce the voltage level at the AC side of the converter, the voltage across the components used in the converter should also be reduced. This leads to the possibility of using this inverter topology in order to achieve reduced component voltage rating. In [38], the CSI+SCaps topology was used to reduce the voltage rating of the IGBTs for a three-phase shunt active power filter application. In that application, the CSI+SCaps topology was connected to a DC inductive load (L_{dc}) that forms a shunt active filter generating harmonic current waveforms to cancel the actual current harmonics produced from a non-linear load (e.g. a full bridge diode rectifier with an RL load). As a result, the sinusoidal supply currents (I_S) can be produced.

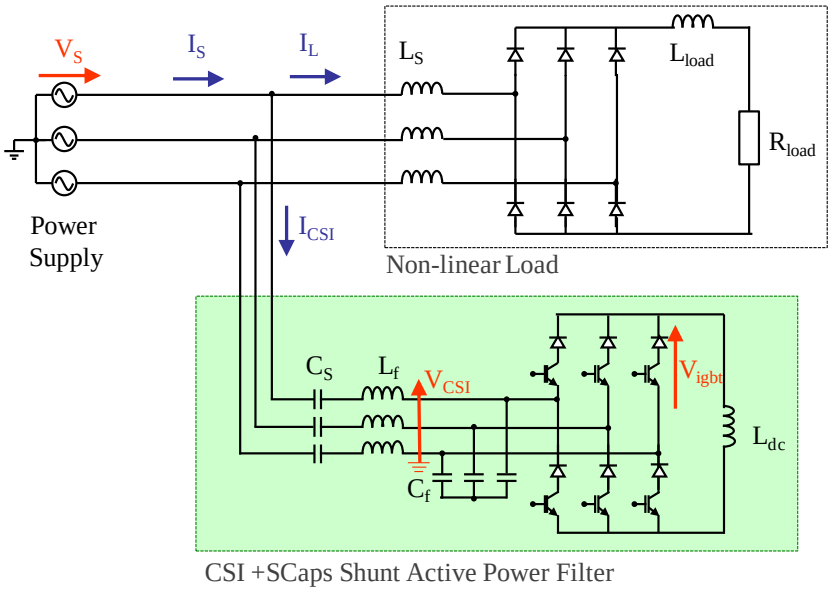


Figure 5.27 The CSI+SCaps shunt active power filter

Figure 5.28 shows the simulation waveforms obtained from the CSI+SCaps shunt active power filter and the traditional CSI shunt active power filter. A 20kVA non-linear load connected to the 690V/50Hz three-phase power supply and with the simulation parameters in Table 5.14 is considered. The waveform I_L refers to the nonlinear load current, I_{CSI} refers to the harmonic current generated from the shunt active filter, V_S and I_S refer to the phase supply voltage and phase supply current, V_{CSI} refers to the voltage at the AC side of the CSI+SCaps shunt active filter and V_{igbt} is the voltage across the IGBT and series diode.

Symbol	Description	Value
L_S	Series inductor	1.5 mH/ph
C_S	Series AC capacitor	30 µF/ph
L_f	AC filter inductor	2.3 mH/ph
C_f	AC filter capacitor	6 µF/ph
L_{dc}	DC inductor	140 mH
L_{load}	Load inductor	20 mH
R_{load}	Load resistor	50 Ω

Table 5.14 Circuit components and their values for the CSI+SCaps and the traditional CSI shunt active power filter

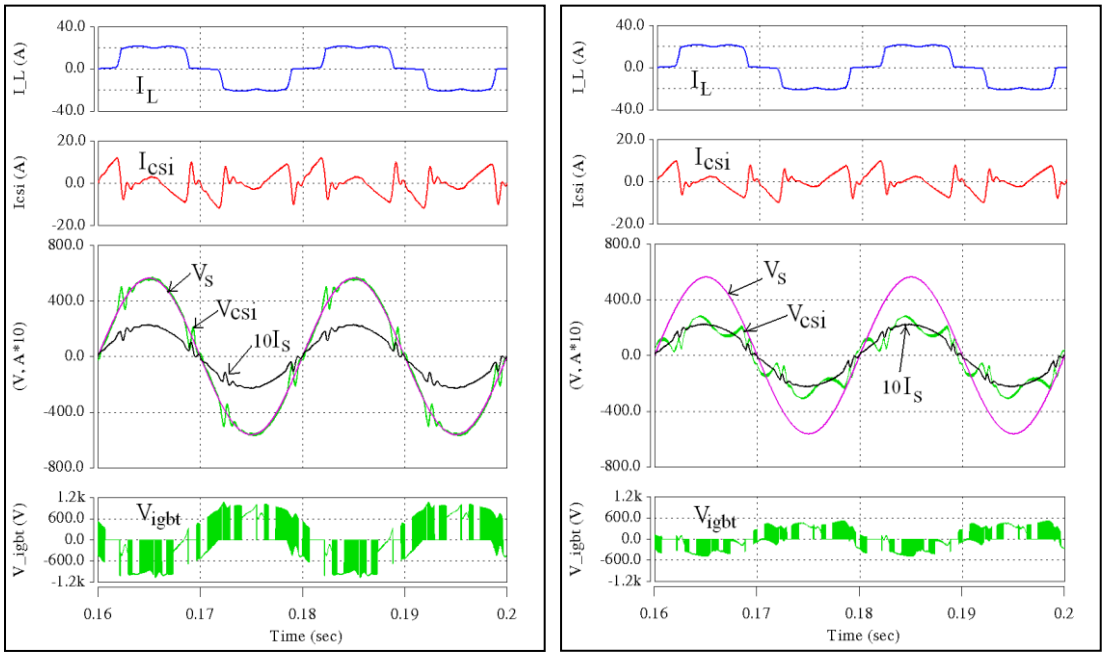


Figure 5.28 Simulation waveforms when compensating 20kVA RL-type load in 690 supply voltage with the harmonic generated from (a) the traditional CSI active power filter and (b) the CSI+SCaps active power filter

From Figure 5.28, both the traditional CSI filter and the CSI+SCaps filter generate the similar harmonic current waveform (I_{CSI}) to cancel the actual harmonics for the load current waveform (I_L) and hence produce similar sinusoidal supply current (I_S) at the supply side. However, the CSI+SCaps filter can achieve a lower peak voltage across the IGBT (V_{igbt}) (up to 526V) when compared to the traditional CSI filter (up to 1071V). Therefore, lower voltage ratings of the IGBT can be used for the CSI+SCaps shunt active filter. In addition, only small series AC capacitors (30μF) are used for this application.

5.6.2 High Frequency Harmonics Reduction

Figure 5.29 shows the per-phase equivalent circuit of the AC filter of the CSI+SCaps topology when the damping resistor (R_f) and series resistor (R_S) are also considered. By applying the voltage divider theorem, the transfer function of the filter in terms of $j\omega$ for the CSI+SCaps topology and the standard CSI topology (without C_S) can be derived as shown in (5.31) and (5.32).

$$H_{CSI+SC}(j\omega) = \frac{V_{CSI}(j\omega)}{V_S(j\omega)} = \frac{R_f + j\omega L_f}{\left(R_f + \frac{C_f R_f}{C_S} - \omega^2 L_f C_f (R_s + R_f)\right) + j\left(\omega C_f R_s R_f + \frac{\omega C_f L_f}{C_S} + \omega L_f\right)} \quad (5.31)$$

$$H_{CSI}(j\omega) = \frac{R_f + j\omega L_f}{\left(R_f - \omega^2 L_f C_f (R_s + R_f)\right) + j\left(\omega C_f R_s R_f + \omega L_f\right)} \quad (5.32)$$

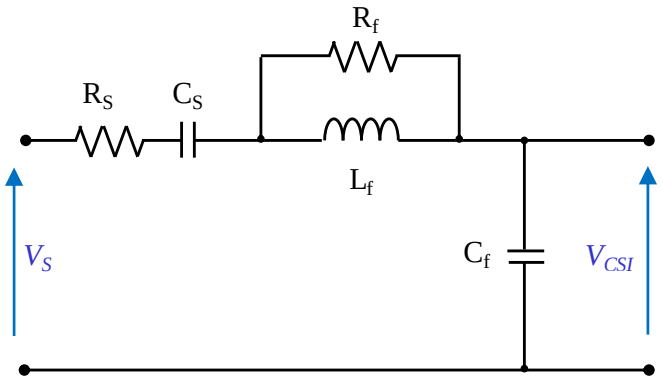


Figure 5.29 Equivalent circuit of the AC filter of the CSI+SCaps topology

Figure 5.30 presents the plots of the filter gain for the CSI+SCaps topology and the standard CSI topology when these topologies operate at the maximum PV power point (OP1) with the parameters in Table 5.5; where R_f=47Ω and R_S=0.5Ω. Both filters are the second order low-pass filters; having a similar cut-off frequency at around $(1/2\pi\sqrt{L_f C_f})$, which is 1.59 kHz for this case.

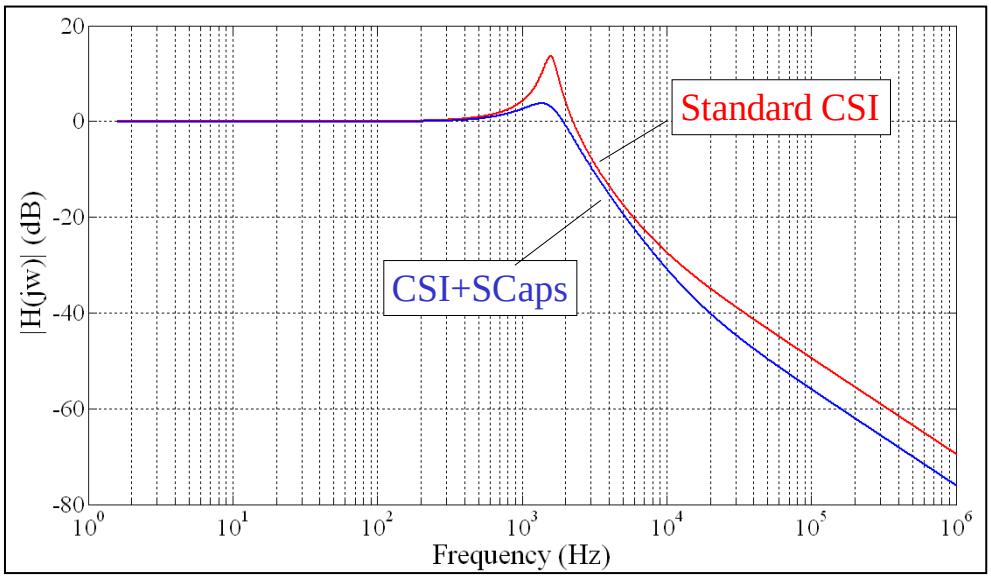
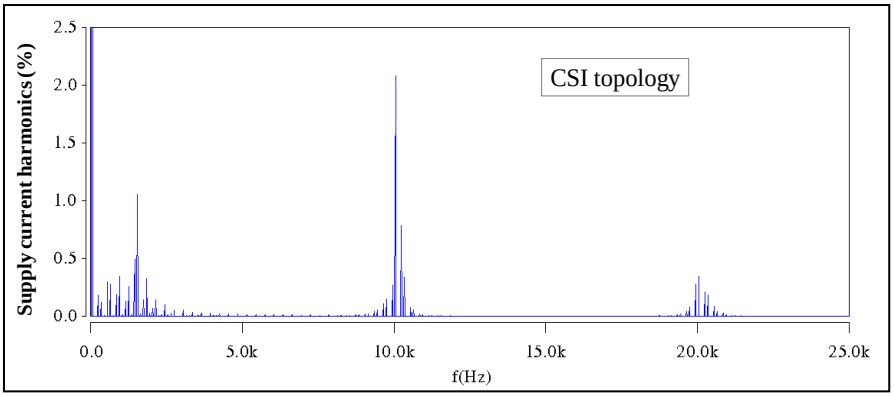


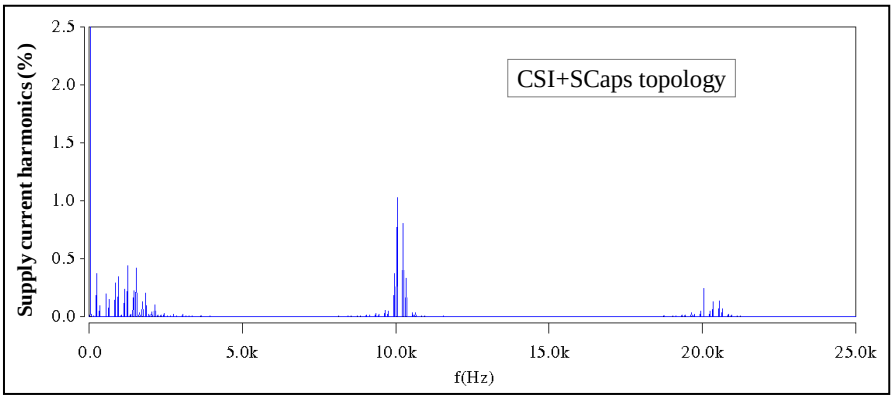
Figure 5.30 Comparison of the harmonic amplitude attenuation performance of the AC filters used in the standard CSI topology versus the CSI+SCaps topology

It can be seen from Figure 5.30 that the filter of the CSI+SCaps topology provides better high harmonic attenuation than the conventional LC filter of the standard CSI topology, which is reflected by lower filter gains at higher frequencies. This implies that the CSI+SCaps topology should produce better AC output power quality with a low harmonic distortion when compared to the standard CSI topology.

Figure 5.31 shows the comparison of the harmonic profiles (FFT) of the AC line current produced by the standard CSI topology and the CSI+SCaps topology when operating at the maximum PV power point (OP1) and using the simulation parameters in Table 5.5.



(a)



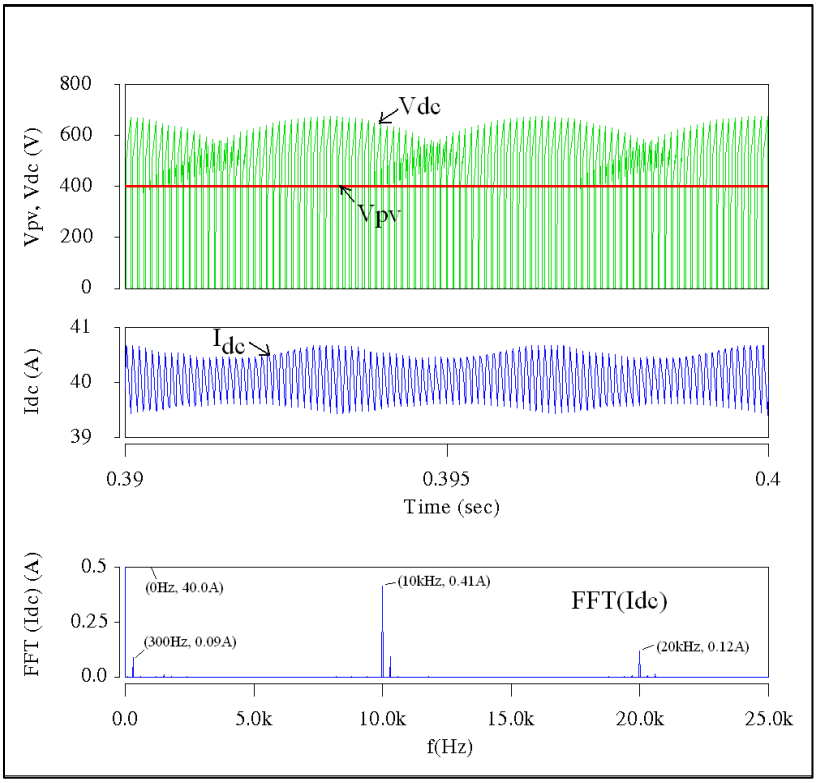
(b)

Figure 5.31 Supply current harmonic amplitudes of (a) the standard CSI topology and (b) the CSI+SCaps topology when operating at the maximum PV power point (OP1) and using simulation parameters in Table 5.5

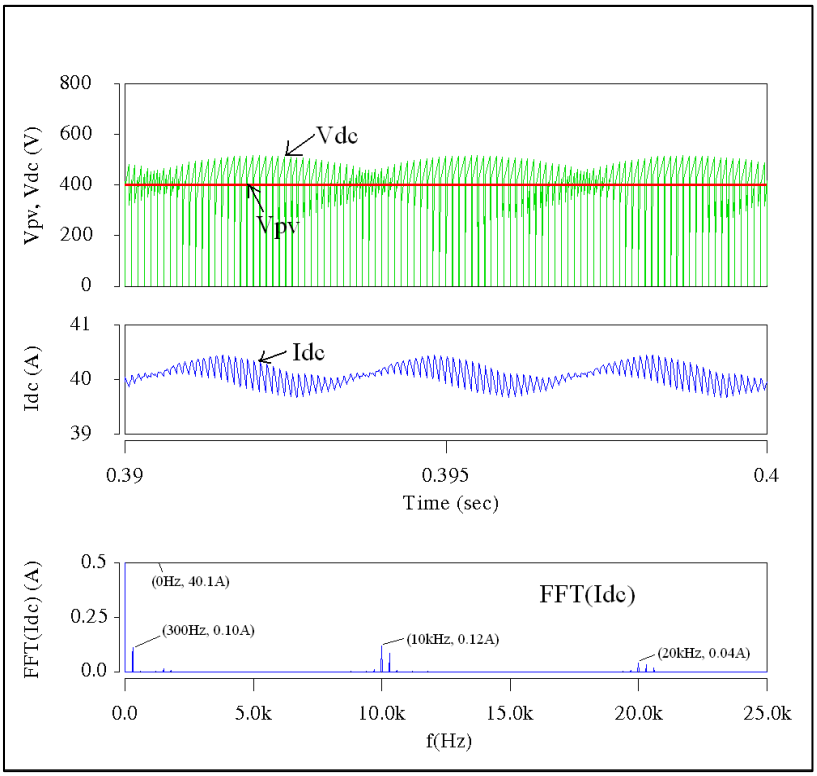
From Figure 5.31, it can be seen that the filter of the CSI+SCaps topology can reduce the amplitudes of the switching harmonics above the cut-off frequency and higher frequencies compared to the standard CSI topology. The harmonic amplitudes around the sampling frequency (10 kHz) and the multiples of the sampling frequencies (e.g. 20 kHz) are significantly reduced by approximately 50%.

5.6.3 Reduced Size of the DC-link inductor

Figure 5.32 shows the waveforms of the PV voltage (V_{pv}), the DC-link voltage (V_{dc}) and the DC-link current (I_{dc}) of the standard CSI topology and the CSI+SCaps topology when they operate at the maximum power point (OP1) and with the simulation parameters specified in Table 5.5.



(a) Standard CSI



(b) CSI+SCaps

Figure 5.32 PV voltage (V_{pv}), DC-link voltage (Vdc) and DC-link current (I_{dc}) simulation waveforms when (a) the CSI topology and (b) the CSI+SCaps operate at the maximum PV power point (OP1)

From Figure 5.32 it can be seen that even if the operating PV voltage and current levels are similar (400V and 40A), the CSI+SCaps provides a much lower peak DC-link voltage ($V_{dc,peak}$ =520V) and a much lower DC-link switching current ripple ($I_{dc,ripple}$=0.12A at 10kHz and 0.04A at 20kHz) compared with the standard CSI topology ($V_{dc,peak}$ =673V and $I_{dc,ripple}$=0.41A at 10kHz and 0.12A at 20kHz). This is because of the fact that the CSI+SCaps topology can operate with a reduced voltage at the AC side of the inverter due to the use of the voltage drop across the series AC capacitors. Since the CSI+SCaps topology provides a lower DC-link current ripple than the CSI topology, the smaller and lighter magnetic cores could be used for the DC-link inductor for the CSI+SCaps topology compared to the standard CSI topology.

5.7 Summary

In this chapter, an alternative three-phase, transformerless grid-tied PV inverter topology to the current source inverter (CSI), called the CSI with series AC capacitors (CSI+SCaps), has been proposed. Details of the circuit configuration, fundamental characteristics, analytical model and equations, modulation and control methodologies, design of the series AC capacitors, simulation results and other possible applications of the proposed topology have been described. The following lists are a brief summary for each of these details:

- The CSI+SCaps topology has the same circuit configuration as the standard CSI topology. The difference is only that three AC capacitors are added by connected in series with each of the three AC phase of the CSI topology.

- When the AC currents flow through the series AC capacitors, the AC voltages will be created across these capacitors. These voltages can be controlled to add to or subtract from the grid voltage and cause the voltages seen at the AC side of the inverter to be higher or lower than the grid voltage levels. This characteristic allows the voltage at the AC side of the CSI+SCaps topology to be adjusted to response to the high or low level of the PV voltage at the DC side. As a result, the CSI+SCaps topology can operate with the optimum voltage transfer ratio between the DC side and the AC side of the converter,

which leads to a lower switching voltage stress on the circuit components and a lower input DC current ripple compared with the standard CSI topology.

- The analytical model of the CSI+SCaps topology is constructed based on the phasor diagram. The analytical equations are derived from the analysis model using the phasorial summation theorem. The analytical model is used to show the magnitudes and phases of the AC side parameters when the topology operates in different situations. The analytical equations are used to design the series AC capacitors and the modulation and control strategies.

- The same modulation techniques used for the standard CSI topology presented in Chapter 4 can also be used for the CSI+SCaps topology. Three control methodologies: the Unity Power factor (UPF) control, the Minimum Switching Voltage (MSV) control and the Optimum Power Factor (OPF) control have been presented in this chapter.

    - The UPF control is the commonly used control technique for the standard CSI topology in order to provide unity power factor outputs at the grid. However, this control method can cause a problem of needing a higher AC side voltage than the grid voltage when using for the CSI+SCaps topology.

    - The MSV control set the modulation index to the maximum and allows only the phase of the AC current to be adjusted. With this way this control method always provides the lowest switching voltage level and a better matching of the AC side voltage to the DC side voltage of the topology in both the normal grid voltage and the grid voltage sags. However, the MSV control provides a low output power factor.

    - The OPF control allows the CSI+SCaps topology to always operate with the optimum point between a high power factor and a low switching voltage level.

- However, only the MSV control can be used for the CSI+SCaps topology during the situation of low-voltage grid faults where the reactive current (partial or full rated level) is required to be injected into the grid to support voltage recovery.

- The required size of the series AC capacitors for the CSI+SCaps topology depend on five parameters: the grid voltage level, the grid frequency, the power factor, the level of voltage reduction at the inverter AC side, and the DC power level. Smaller series AC capacitors are required for a higher grid voltage level and a higher grid frequency. Larger series AC capacitors are required for a higher DC power level and the largest size are required for the point that the power factor angle is equal to the amplitude ratio between the AC side voltage of the inverter and the grid voltage (i.e. $cos\theta=a$).

- The operation and control principle of the CSI+SCaps topology when operating with the UPF, MSV and OPF control have been verified via the simulation and in comparison to the standard CSI topology when operating with the UPF control. The operating results show supporting results to the theoretical control principles.

- The CSI+SCaps topology could be used in applications where reduced component voltage rating or improved high frequency harmonic attenuation or smaller DC-link inductor are needed.

    - The potential to use the CSI+SCaps topology to reduce the voltage rating of the IGBTs in a shunt active power filter application has been demonstrated.

    - It was also shown that the added series AC capacitors in the CSI+SCaps topology are also part of the filters which provide better capability to attenuate high frequency switching current harmonics and therefore provide a low harmonic distortion of the AC output waveforms compared with the traditional LC filters in the standard CSI topology.

    - As the CSI+SCaps topology also provides low DC-link current ripple compared to the standard CSI topology which is where a smaller DC-link inductor could be used.

Chapter 6

Evaluation of the CSI with Series AC Capacitors in Comparison to the Other Inverter Topologies under Investigation

In Chapter 5 an alternative inverter topology to the Current Source Inverter (CSI) for transformerless grid-tied PV applications, called *the CSI with series AC capacitors* (CSI+SCaps), has been proposed. This chapter presents an evaluation of the performance of the CSI+SCaps in comparison with the standard CSI and five other inverter topologies (which have been presented in Chapter 4). Table 6.1 shows a list of all the candidate inverter topologies. To facilitate the evaluation, the topologies are divided into two groups based on the type of core PWM bridge circuits (VSI based inverters or CSI based inverters) as shown in Table 6.1.

Core PWM Bridge Circuit	Inverter Topology	Symbol
VSI based	Standard Voltage Source Inverter	VSI
	Two-stage VSI with a Boost converter	VSI+Boost
	Z-Source Inverter (Voltage fed)	ZSI-V
CSI based	Standard Current Source Inverter	CSI
	Two-stage CSI with a Buck converter	CSI+Buck
	Z-Source Inverter (Current fed)	ZSI-I
	CSI with Series AC Capacitors	CSI+SCaps

Table 6.1 Candidate inverter topologies under evaluation

In this study, all of the candidate inverter topologies were designed to convert and feed the power from a PV source into a 415V/50Hz power grid. A PV source with the specifications shown in Table 6.2 was used (definition of the PV specification parameters can be seen in Section 2.7.1).

PV specifications	Value
Peak power under 10%-100% sun irradiance	1.8 -16 kW
Voltage at peak power under 10%-100% sun irradiance	0.6-0.8 of rated maximum voltage
Fill Factor	0.7

Table 6.2 Specifications for the PV source used for evaluation

All the candidate inverter topologies were modelled in the SABER simulation program. The simulation results are used as part of the evaluation and analysis. The candidate topologies are evaluated in terms of the required PV voltage and current ratings, operating modulation depths, required circuit components, input and output power quality, voltage and current stress on power semiconductors, estimated cost of power semiconductors, semiconductor power losses, European efficiencies and overall performance.

6.1 Comparison of PV Voltage and Current Ratings

As presented in Section 3.1, grid-tied PV inverters should have voltage and current ratings higher than the voltage and current rating of the PV source in order to provide proper connection compatibility between them. Therefore, higher PV voltage and current ratings require higher voltage and current ratings of the inverters and hence cause higher losses within the inverters. In addition, a higher PV voltage can lead to a higher resistance within the PV cells (see Section 2.7.3), and hence cause higher losses within the PV source.

With the given specifications of the PV source in Table 6.2 and the grid, the voltage and current ratings required for each candidate topology when operating at the same power levels can be determined as shown in Figure 6.1. The parameters V_{mpp}, I_{mpp} and P_{mpp} refer to the output voltage, current and power of the PV source at the rated MPP, V_{OC} and I_{SC} refer to the open circuit voltage and the short circuit current (maximum voltage and current) of the PV source.

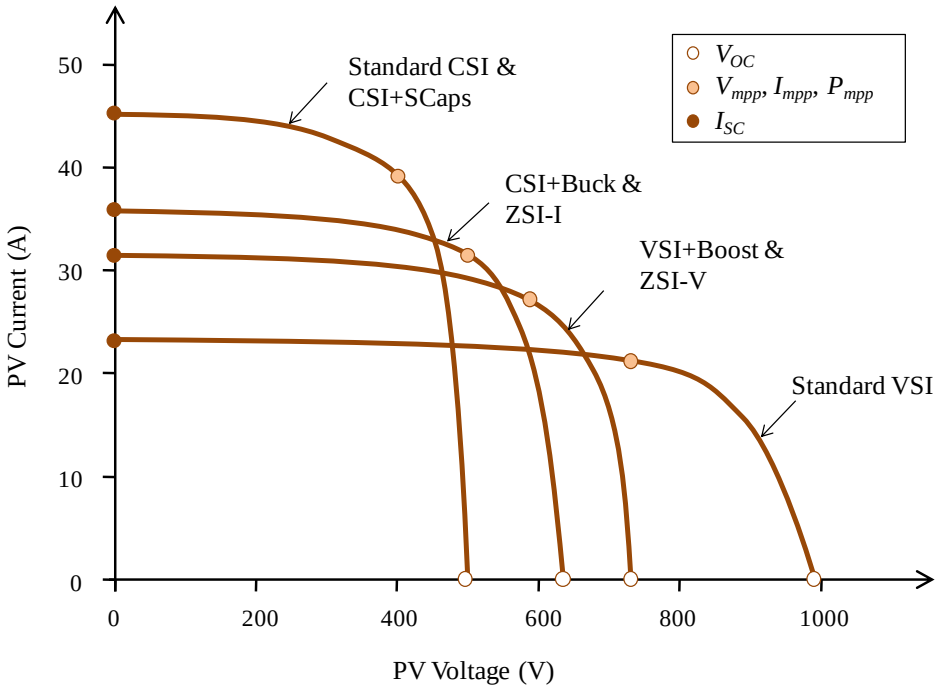


Figure 6.1 PV voltage and current ratings required for each candidate inverter topology

From Figure 6.1 it can be seen that:

- The CSI+SCaps requires the same PV ratings as a standard CSI
- The CSI+SCaps and a standard CSI have a lower PV voltage rating but a higher PV current rating compared to all the other candidate topologies

As the CSI+SCaps has the same PV ratings as a standard CSI, the topology can be directly connected to the PV source in the same way as a standard CSI. A lower PV voltage rating may lead the CSI+SCaps and a standard CSI to potentially have lower switching losses within their circuits and lower internal losses within the PV cells. However, since the CSI+SCaps and a standard CSI have the highest PV current rating, these topologies potentially have the highest conduction losses within their circuits (this issue is discussed in more detail in Section 6.8).

6.2 Comparison of Operating Modulation Depths

Modulation depth or *modulation index* (*m*) is a control parameter used in the modulation for all the candidate inverter topologies (as presented in Section 4.3 and Section 4.4). The definitions of *m* are as follows:

- For the VSI based topologies, *m* is the ratio of the AC output voltage magnitude ($|\hat{V}_{ac}|$) "seen" at the AC side of the PWM circuit of the topologies to the peak DC input voltage ($\hat{V}_{dc}$) as shown in (6.1).

$$m_{(vsi)} = \frac{|\hat{V}_{ac}|}{\hat{V}_{dc}} \quad ; 0 \leq m_{(vsi)} \leq 1 \tag{6.1}$$

- For the CSI based topologies, *m* is the ratio of the AC output current magnitude ($|\hat{I}_{ac}|$) "seen" at the AC side of the PWM circuit of the topologies to the available DC input current (I_{dc}) as shown in (6.1). Assuming no power loss within the topologies and under power equilibrium between the DC side and AC side ($\hat{P}_{dc} = |\hat{P}_{ac}|$), *m* for the CSI based topologies can be also defined as (6.3).

$$m_{(csi)} = \frac{|\hat{I}_{ac}|}{\hat{I}_{dc}} \quad ; 0 \leq m_{(csi)} \leq 1 \tag{6.2}$$

or

$$m_{(csi)} = \frac{\hat{V}_{dc}}{|\hat{V}_{ac}|} \quad ; \text{if } \hat{P}_{dc} = \hat{V}_{dc}\hat{I}_{dc} = |\hat{V}_{ac}||\hat{V}_{ac}| = |\hat{P}_{ac}| \tag{6.3}$$

From the definitions of *m*, a higher *m* designates a higher utilization of the DC input voltage (or current) from the PV source and a more optimum voltage and current levels between the DC side and the AC side. For example, if $m_{(csi)}$=1, the required DC input will be equal to the AC output magnitude ($\hat{I}_{dc} = |\hat{I}_{ac}|$) but if $m_{(csi)}$=0.5, the DC input current with two times higher than the AC output magnitude is needed ($\hat{I}_{dc} = 2|\hat{I}_{ac}|$).

Using (6.1) and (6.3), *m* as a function of operating PV voltage (V_{pv}) for each candidate topology can be derived as shown in Table 6.3. The supply voltage amplitude (V_S) is assumed to be constant. The voltages drops across the filtering components are neglected. The plots of the functions in Table 6.3 when V_{pv} varies from 0.6 to 1 of the rated no load voltage (rated maximum PV voltage) are shown in Figure 6.2.

Inverter Topology		Modulation Depth (m)
VSI	Standard VSI	$m \approx \frac{\sqrt{3}V_s}{V_{pv}}$
	VSI+Boost	$m(boost) \approx 1$; $m(buck) = \frac{\sqrt{3}V_s}{V_{pv}}$
	ZSI-V	$m(shoot\ through) = \frac{\sqrt{3}V_s(1-2D_o)}{V_{pv}}$; $m(buck) = \frac{\sqrt{3}V_s}{V_{pv}}$
CSI	Standard CSI	$m \approx \frac{2V_{pv}}{3V_s}$
	CSI+Buck	$m(boost) \approx \frac{2V_{pv}}{3V_s}$; $m(buck) \approx 1$
	ZSI-I	$m(boost) = \frac{2V_{pv}}{3V_s}$; $m(open\ circuit) = \frac{2V_{pv}(1-2D_o)}{3V_s}$
	CSI+SCaps	$m \approx \frac{2V_{pv}}{3V_s cos\theta} \approx 1$

Table 6.3 Theoretical modulation depth (m) as a function of operating PV voltage (V_{pv}) of each candidate inverter topology; parameters V_S is the phase grid voltage amplitude, D_o is the switching duty cycle and $cos\theta$ is the output power factor

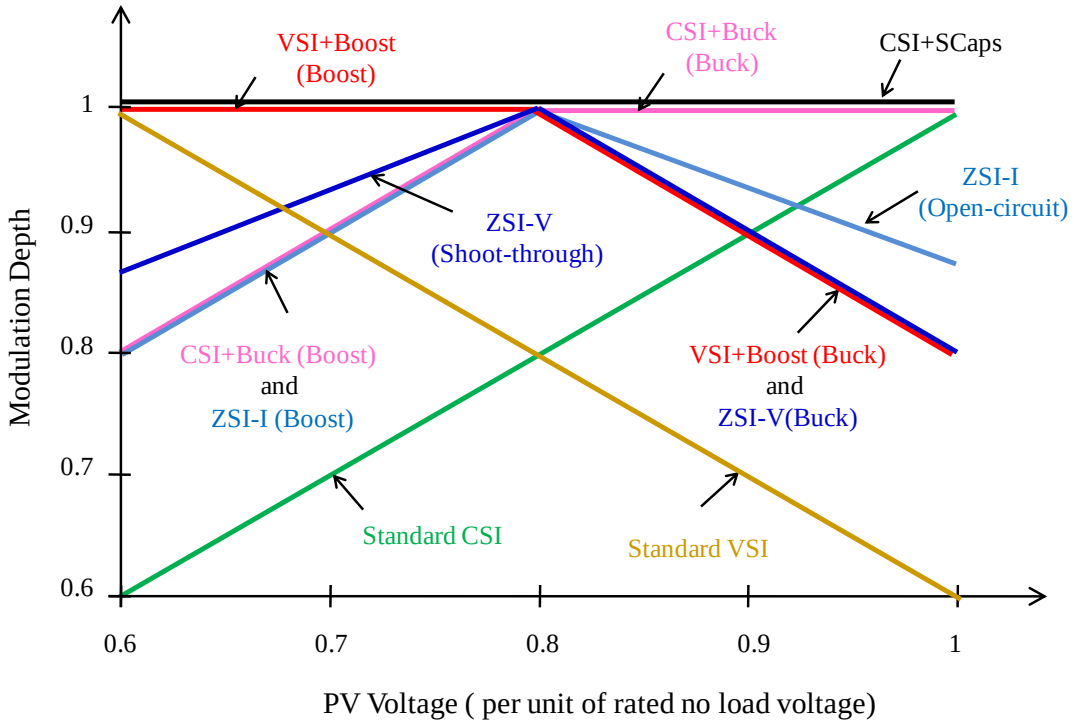


Figure 6.2 Plot of modulation depth (m) curves as a function of operating PV voltages for each candidate inverter topology (according to Table 6.3)

It can be seen from Figure 6.2 that:

- The CSI+SCaps can operate with the highest modulation depth (m≈1) for the whole PV voltage operating range.
- If the candidate inverter topologies are prioritised to operate within a typical MPP range (0.6-0.8 of rated no load voltage) and then a higher PV voltage (0.8-1 of rated no load voltage), the candidate inverter topologies which provide the best performance in terms of high operating modulation depth would be ordered as follows: CSI+SCaps, VSI+Boost, ZSI-V, CSI+Buck, ZSI-I, standard VSI and standard CSI respectively

The presence of the series AC capacitors in the CSI+SCaps allows the AC output converter voltage to be adjusted to have almost the same level as the DC input voltage from the PV source. This is the reason why the CSI+SCaps always operates with high operating modulation depth regardless of any change of input PV voltage (see more details in Section 5.4 and Section 5.5).

6.3 Comparison of Circuit Components

6.3.1 Number of Active Components

Active components in this study are considered to be any power semiconductor devices, voltage and current transducers and controllers in both the power circuits and control circuits of the candidate topologies. A larger number of active components would represent higher complexity and power consumption in the control circuits of the topologies.

According to the control schematics of the candidate topologies presented in Section 4.4 and Section 5.5.2, the required active components for each topology can be found in Figure 6.3.

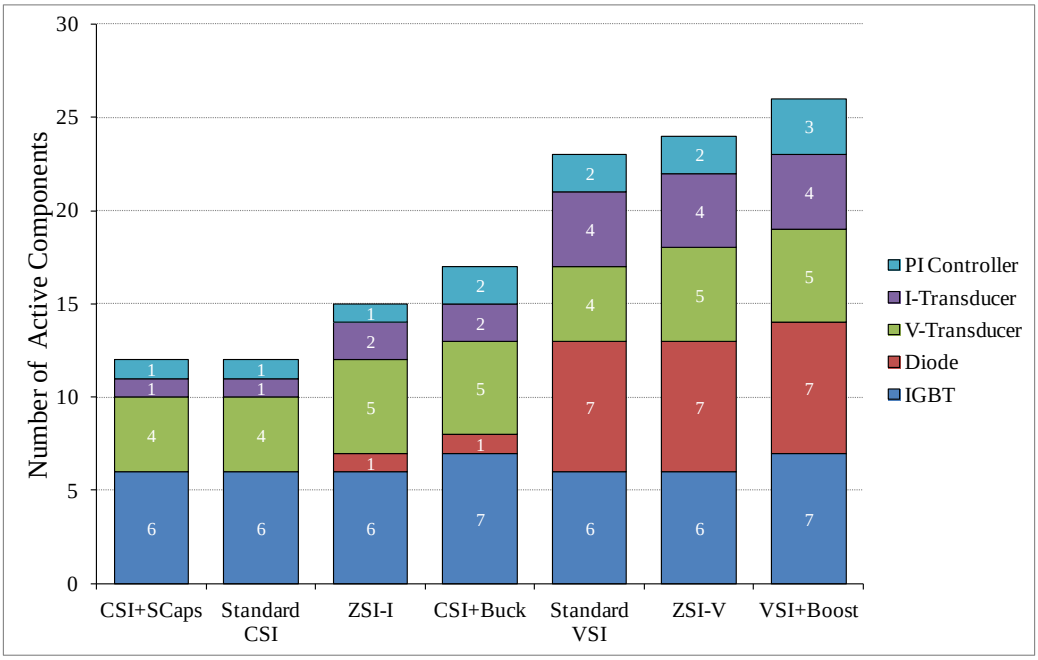


Figure 6.3 Required active components for each candidate inverter topology

It can be seen in Figure 6.3 that the CSI+SCaps and the standard CSI require the minimum number of active components compared to all the other candidate inverter topologies. With the possibility of using RB-IGBTs [34], the CSI+SCaps and all the CSI based inverters (a standard CSI, a CSI+Buck and a ZSI-I) would no longer require any series power diode for their circuits and hence need fewer power semiconductors than the VSI based inverters (a standard VSI, a VSI+Boost and a ZSI-V). As a result, the CSI+SCaps and the standard CSI would have the simplest power circuits and control circuit configuration as well as the lowest control circuit power consumption compared to the other candidate topologies.

6.3.2 Size of Passive Components

The PV voltage and current ratings presented in Section 6.1 could be used to predict the size of passive components (inductors and capacitors) for the candidate topologies. If this is the case, the VSI+Boost, CSI+Buck, ZSI-V and ZSI-I may have a preferable size of passive components when compared to the standard VSI, standard CSI and CSI+SCaps as a result of their optimum PV ratings. However, in most cases, the passive components used in the converter topologies are usually part of a filter,

used to provide an improved power quality of input and output waveforms. As a result, the size of passive components based on the power quality criteria is worth considering, which is discussed in this section.

The size of passive components required for the candidate topologies in order to meet a specific input and output power quality can vary depending on the operating point of the PV source. Figure 6.4 shows three different PV operating points, which are used to observe the size of passive components for each candidate topology in this study. These operating points are chosen from the extreme conditions of the operating voltage and power of the converters within their normal operating ranges.

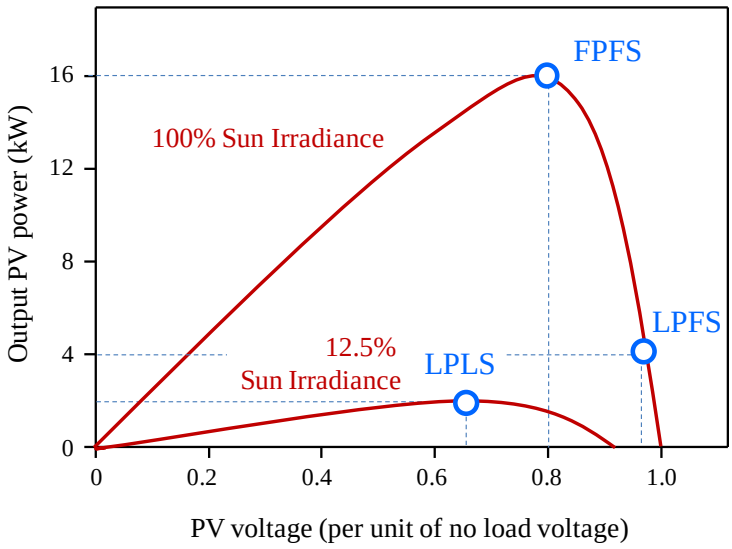


Figure 6.4 Three different PV operating points for observing the size of passive components required for each candidate topology

As shown in Figure 6.4, the first point is called *Full Power and Full Sun* (FPFS), which is where the candidate topologies operate with the maximum output PV power (16kW) at rated MPP under 100% sun irradiance. The second point is called *Low Power and Full Sun* (LPFS), which is where the candidate topologies operate close to the maximum PV voltage (0.95 of rated no load voltage) and with low output PV power (4kW) under 100% sun irradiance. The third point is called *Light Power and Light Sun* (LPLS), which is where the candidate topologies operate close to the lowest PV voltage (0.65 of rated no load voltage) and with low output PV power (2kW) at MPP under 12.5% sun irradiance.

With the use of the circuit component design procedure presented in Section 4.5 and the given operating points shown in Figure 6.4, the values of the passive components required for each candidate topology in order to provide an input PV voltage and current ripple of $0.5\%V_{pk\text{-}pk}$ and $10\%A_{pk\text{-}pk}$ and an output line current THD of 5% are shown in Table 6.4.

PV Operating Point	**Inverter Topology**	**Required Passive Component**				
		AC side		DC side		Additional Component
		L_f (mH/ph)	C_f (μF/ph)	L_{dc} (mH)	C_{dc} (μF)	
FPFS	Standard VSI	1.6	-	-	280	-
	VSI+Boost	1.4	-	1.3	300	-
	ZSI-V	1.35	-	-	170	C1=C2=150μF; L1=L2=0.2mH
	Standard CSI	1.1	5	3.2	-	-
	CSI+Buck	0.65	5	0.9	120	-
	ZSI-I	0.55	5	1.8	-	C1=C2=10μF; L1=L2=0.5mH
	CSI+SCaps	0.65	5	2.2	-	3×Cs=500 μF/ph
LPFS	Standard VSI	17	-	-	170	-
	VSI+Boost	8.5	-	0.025	40	-
	ZSI-V	5.5	-	-	300	C1=C2=50μF; L1=L2=0.2mH
	Standard CSI	0.45	5	11	-	-
	CSI+Buck	0.65	5	11	650	-
	ZSI-I	0.6	5	13	-	C1=C2=60μF; L1=L2=2.5mH
	CSI+SCaps	0.45	5	11	-	3×Cs=200μF/ph
LPLS	Standard VSI	25	-	-	90	-
	VSI+Boost	25	-	38	1000	-
	ZSI-V	22.5	-	-	6000	C1=C2=500μF; L1=L2=0.2mH
	Standard CSI	1.5	5.5	24	-	-
	CSI+Buck	1.5	5	6	130	-
	ZSI-I	0.6	5	13	-	C1=C2=30μF; L1=L2=2.5mH
	CSI+SCaps	0.45	5	13	-	3×Cs=100μF/ph

Table 6.4 Required passive components for each candidate inverter topology when operating at PV operating points in Figure 6.4 (FPFS, LPFS and LPLS)

If the maximum values of the required passive components on both the AC side and the DC side in Table 6.4 are selected in order to provide input ripple and output THD lower than specified values over the whole considered operating range, and if the sizes of those components vary with their values, the size of total required passive components of each candidate topology (after normalised with the maximum value of total passive components) has a result as shown in Figure 6.5.

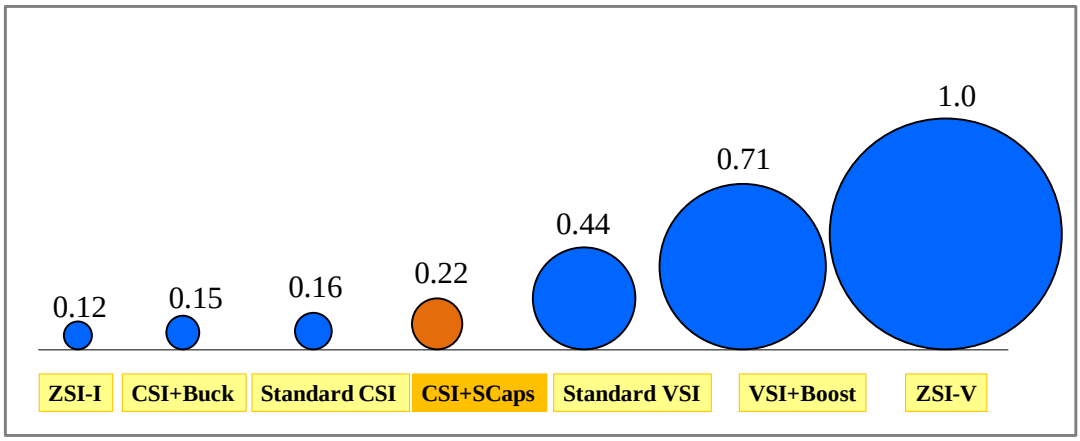


Figure 6.5 Size of total required passive components of each candidate topology

It can be seen from Figure 6.5 that, in order to reach the specification required:

- The CSI+SCaps and all the CSI based topologies (a standard CSI, a CSI+Buck and a ZSI-I) have a smaller size of total passive components compared to all the VSI based topologies (a standard VSI, a VSI+Boost and a ZSI-V)
- The CSI+SCaps has the largest size of total passive components compared to all the other CSI based topologies

The series AC capacitors leads to the larger size of a CSI+SCaps (approximately 40% larger) compared to a standard CSI. However, if the size of a DC-link inductor (L_{dc}) is considered (see Table 6.4), the CSI+SCaps would require a smaller DC-link inductor (2.2-13mH) compared to all the other CSI based topologies (0.9-24mH). The CSI+SCaps also requires the smallest AC filtering inductor (L_f) (0.45-0.65mH) compared to all other candidate topologies (0.45-25mH).

6.4 Comparison of Input Power Quality

In this section, the input power quality of the CSI+SCaps is evaluated in comparison to all the candidate topologies. The input power quality in terms of input voltage and current ripple is considered. A high level of input voltage and current ripple can reduce the accuracy of the MPP since the "real-time" voltage and current are usually measured and used for the MPP computations in most MPP tracking controllers [108].

The high input voltage and current ripple also reduces working life of the PV cells [21]. Therefore, high input voltage and current ripple should be avoided.

In Section 6.3.2 the different sizes of passive components which are required to meet a specified ripple content for the input voltage and current in all the candidate topologies has been presented. In this section, the similar sizes of passive components are used and the input voltage and current ripple are observed. The selected components are primitively designed to provide similar input and output power quality for a standard VSI and a standard CSI at the rated MPP. Then, the same sets of the components are used for all the same type topologies, as shown in Table 6.5. The additional components are used to ensure proper operation for the topologies. All the candidate topologies are modelled and tested in the SABER simulation at the same operating points described in Section 6.3.2. Simulated waveforms of the input voltage and current are shown in Figures 6.6-6.8 and measured input voltage and current ripple are presented in Table 6.6.

Inverter Topology		**Passive Component**				
		AC side		DC side		Additional Component
		L_f (mH/ph)	C_f (μF/ph)	L_{dc} (mH)	C_{dc} (μF)	
VSI	Standard VSI	5	-	-	1000	-
	VSI+Boost	5	-	10	1000	-
	ZSI-V	5	-	-	1000	C1=C2=500μF; L1=L2=0.2mH
CSI	Standard CSI	2	5	10	-	-
	CSI+Buck	2	5	10	1000	-
	ZSI-I	2	5	10	-	C1=C2=50μF; L1=L2=2.5mH
	CSI+SCaps	2	5	10	-	3×Cs=500 μF/ph

Table 6.5 Passive components used for an evaluation of input power quality for each candidate inverter topology

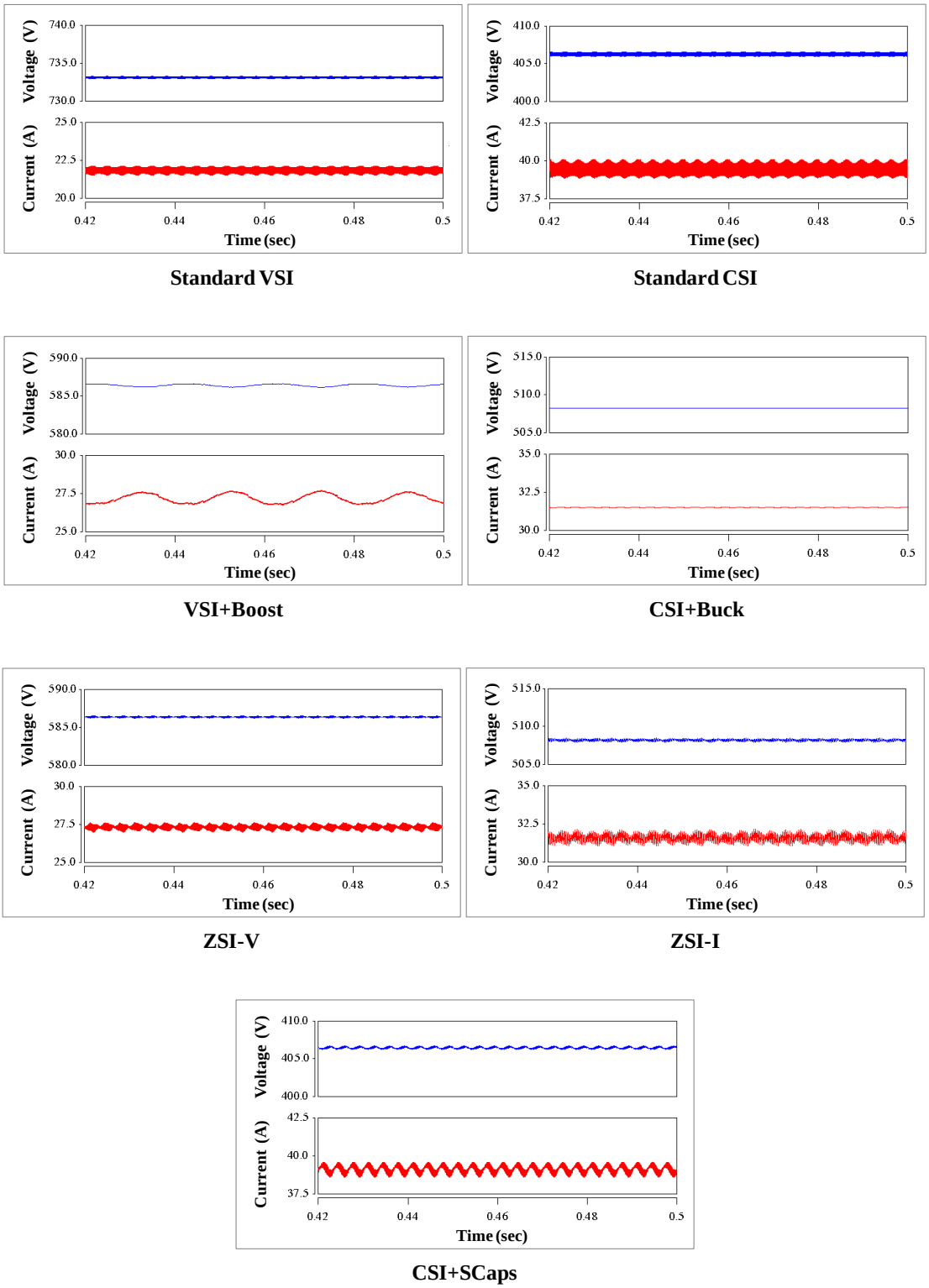


Figure 6.6 Input voltage and current simulation waveforms for all the candidate topologies operating at Full Power and Full Sun (FPFS)

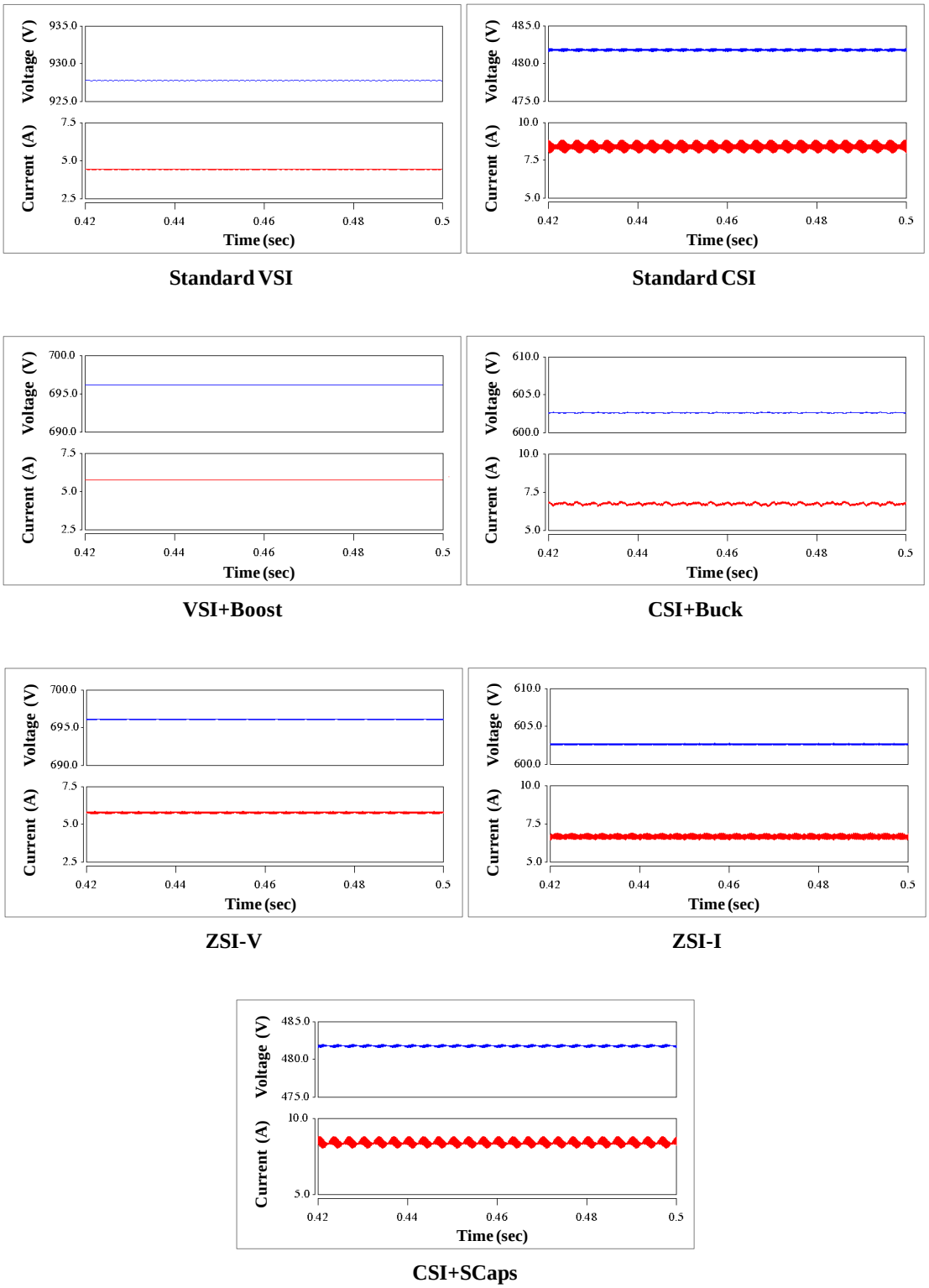


Figure 6.7 Input voltage and current simulation waveforms for all the candidate topologies operating at Low Power and Full Sun (LPFS)

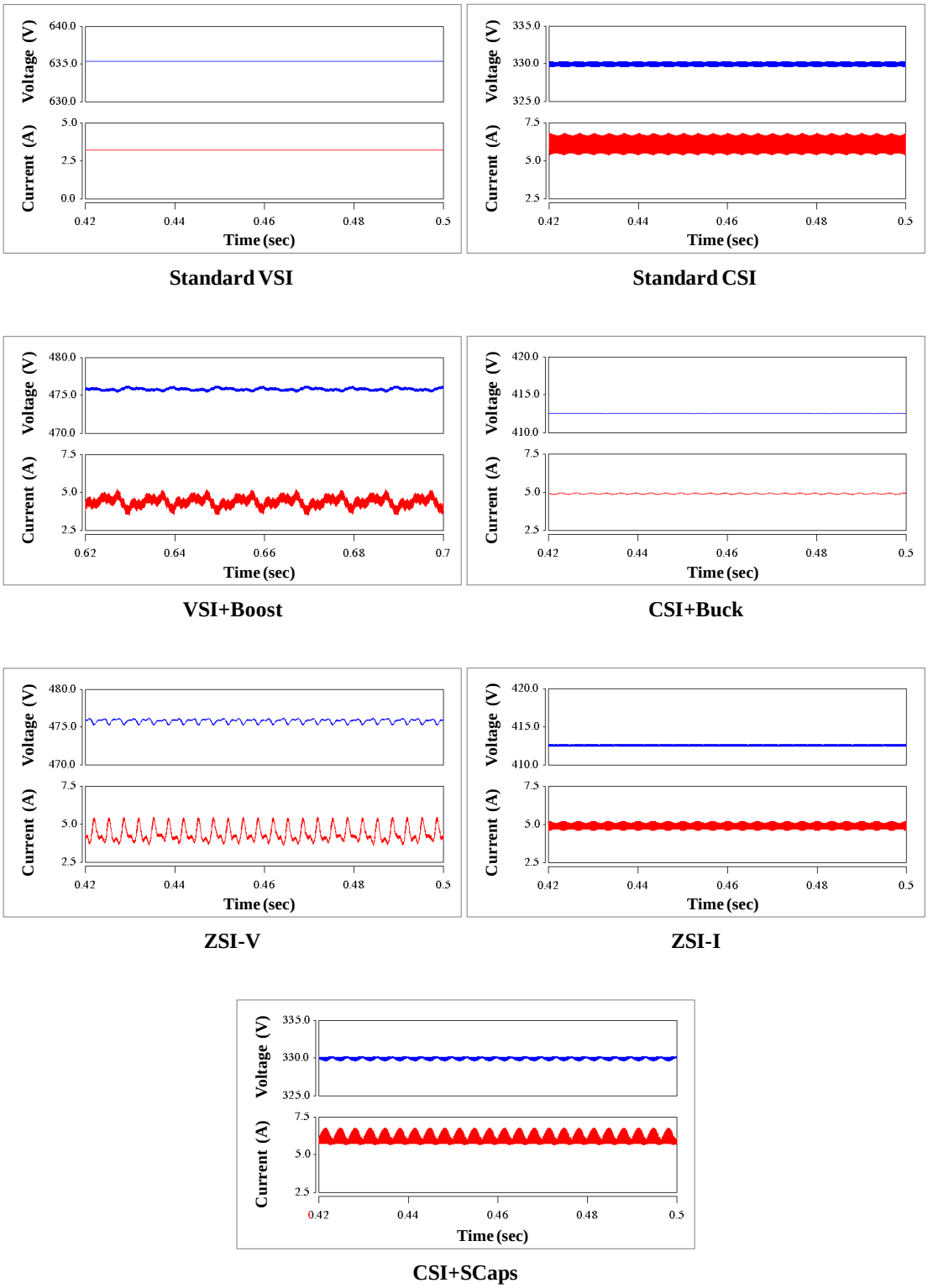


Figure 6.8 Input voltage and current simulation waveforms for all the candidate topologies operating at Light Power and Light Sun (LPLS)

Inverter Topology		Measured Input Voltage and Current Ripple					
		at FPFS		at LPFS		at LFLS	
		V(%pk-pk)	I(%pk-pk)	V(%pk-pk)	I(%pk-pk)	V(%pk-pk)	I(%pk-pk)
VSI	Standard VSI	0.04	2.9	0.00	1.7	0.00	1.1
	VSI+Boost	0.17	7.3	0.00	0.2	0.20	44.7
	ZSI-V	0.05	2.3	0.01	3.0	0.20	44.3
CSI	Standard CSI	0.16	3.1	0.09	10.5	0.22	23.6
	CSI+Buck	0.01	0.3	0.03	6.3	0.01	2.4
	ZSI-I	0.11	3.6	0.04	7.1	0.08	12.7
	CSI+SCaps	0.12	2.5	0.08	9.2	0.17	18.3

Table 6.6 Measured input voltage and current ripple for each candidate topology

It can be seen from the waveforms in Figures 6.6-6.8 and Table 6.6 that:

- All the candidate topologies produce different waveform shapes and different ripple levels despite the use of similar passive components. These are the effects of different modulation and control strategies used between the topologies.

- Most candidate topologies provide the lowest input voltage ripple (up to 0.9%) at LPFS, which is where the input voltage is sufficient for the VSI based topologies and most CSI based topologies can operate with high modulation depths. On the other hand, most candidate topologies provide the highest input voltage ripple (up to 0.22%) at LPLS, which is where the input voltage is insufficient for the VSI based topologies and thus their voltage step-up mechanism has to operate, leading to increased fluctuation of the input voltage level.

- Most VSI based topologies have the lowest current ripple (up to 3%) at LPFS; where these topologies can operate with high modulation depths, whilst most CSI based topologies have the lowest current ripple (up to 3.6%) at rated MPP (FPFS); where these topologies can operate with medium-high modulation depths and high operating current at the same time (a more ideal current source). On the other hand, most candidate topologies provide the highest current ripple (up to 44.7%) at LPLS, which is the same point and has the same causes to where these topologies provide the highest voltage ripple.

- The CSI+SCaps provides the better input power quality than a standard CSI with both a lower input voltage ripple and a lower input current ripple for all the considered operating points.

- A clearer comparison for the input power quality of all the candidate topologies can be made by considering the average DC input voltage and current ripple of the three considered operating points. The results are shown in Figures 6.9-6.10. It can be seen that:

    - The CSI+SCaps gives a relatively high level of input voltage ripple and is ranked 5th out of the seven candidate topologies (see Figure 6.9).

    - The CSI+SCaps gives a medium level of input current ripple and is ranked 4th out of the seven candidate topologies (see Figure 6.10).

    - The CSI+SCaps has a lower input voltage ripple and input current ripple compared to a standard CSI by approximately up to 20%.

The input voltage and current ripple of the CSI+SCaps can be improved by adding a DC-link capacitor into the DC side of its circuit. The CSI+SCaps provides lower input voltage and current ripple than a standard CSI because the topology can operate with a higher modulation depth than a standard CSI, as described in Section 6.2.

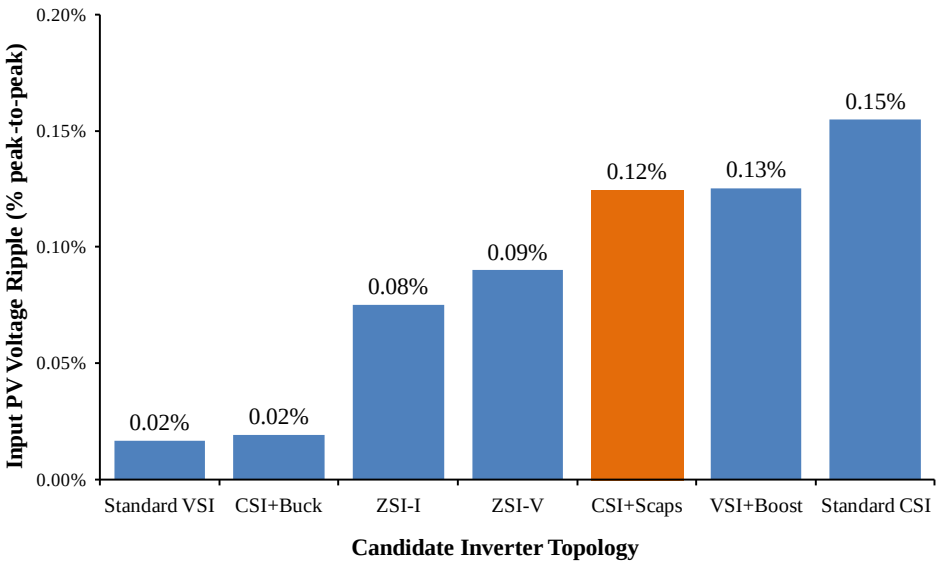


Figure 6.9 Average input PV voltage ripple for each candidate topology

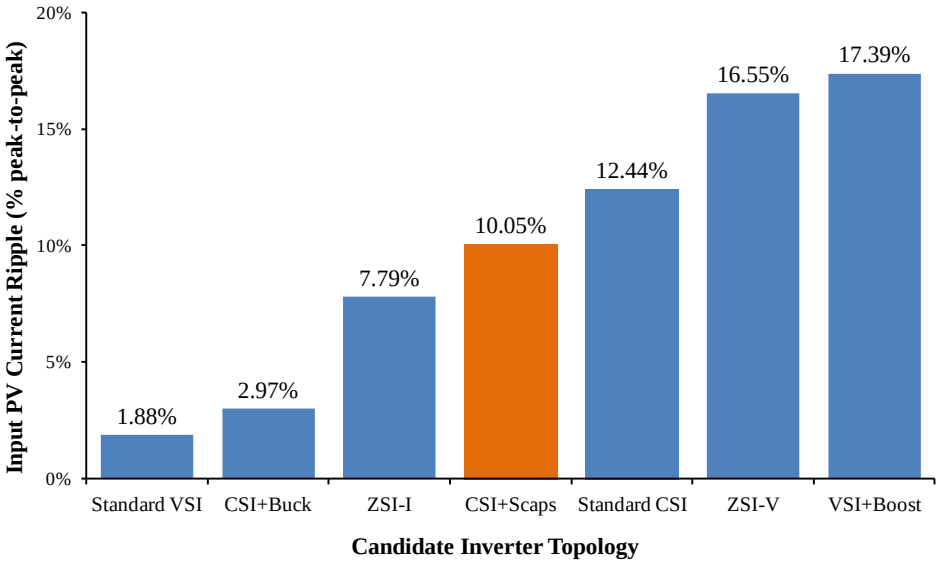


Figure 6.10 Average input PV current ripple of each candidate topology

6.5 Comparison of Output Power Quality

As mentioned in Section 3.2.1, grid-tied PV converters are required to produce high output power quality complying with all relevant grid codes and standards. In this Section the output power quality in terms of Total Harmonic Distortion (THD) and Power Factor (PF) produced by the CSI+SCaps is evaluated in comparison to all the other candidate topologies. In this study, the topologies are required to operate with a current THD lower than 5% (specified by IEEE 1547) and provide a PF higher than 0.9 for the PV power greater than 50% of the rated power (IEC 61727).

Similar to the evaluation in Section 6.4, all the candidate topologies were implemented in the SABER simulation program using the simulation parameters in Table 6.5 and the same operating points as described in Section 6.3.2. Since an ideal balanced and harmonic free utility connection is used in the simulation, the only source of harmonic distortion is from the power converters. As a result, the THD of the supply current can be used to represent the output power quality of the candidate topologies. Simulated waveforms for the output phase supply voltage (u_{sa}), phase supply current (i_{sa}) and FFT spectra for the phase supply current (FFT(i_{sa})) for each candidate topology are shown in Figures 6.11-13. Measured supply current fundamental amplitude ($I_{s@50Hz}$), THD and PF are presented in Table 6.7.

Inverter Topology		Measured Output Supply Current Parameters								
		at FPFS			at LPFS			at LPLS		
		$I_{s@50Hz}$ (A)	$I_{s(THD)}$ (%)	PF (-)	$I_{s@50Hz}$ (A)	$I_{s(THD)}$ (%)	PF (-)	$I_{s@50Hz}$ (A)	$I_{s(THD)}$ (%)	PF (-)
VSI	Standard VSI	28.3	1.57	1.00	3.0	17.04	1.00	1.7	25.55	1.00
	VSI+Boost	29.2	1.43	1.00	5.0	8.68	1.00	1.7	25.50	1.00
	ZSI-V	31.4	1.35	1.00	7.9	5.51	1.00	4.5	15.45	1.00
CSI	Standard CSI	31.8	4.13	1.00	7.8	3.14	0.99	4.0	5.32	0.98
	CSI+Buck	31.3	3.11	1.00	8.0	3.78	0.99	4.0	4.61	0.98
	ZSI-I	31.7	3.37	1.00	7.9	3.06	1.00	4.0	3.19	0.99
	CSI+SCaps	38.0	2.99	0.84	8.4	2.80	0.94	6.3	3.32	0.62

Table 6.7 Measured phase supply current parameters: fundamental amplitudes ($I_{s@50Hz}$), THD and PF

It can be seen from the waveforms in Figures 6.11-6.13 and the figures in Table 6.7 that:

- All the candidate topologies can achieve quasi sinusoidal output supply current waveforms for all the operating points but with different amplitudes, phases and quality.
- The CSI based topologies operate with higher supply currents (31-38A) than the VSI based topologies (28-31A) for all the operating points. The CSI+SCaps operates with the highest supply current (38A) among all the topologies.
- All the CSI based topologies can achieve lower supply current THD levels (2.8-5.3%) than the specified limit (5%) at all the operating points. All the VSI based topologies can achieve lower THD levels (1.3-1.6%) than the specified limit only at rated MPP (FPFS) whilst providing the high and even higher supply current THD levels at LPFS (5.5-17%) and LPLS (15-25.5%).
- All candidate topologies can achieve a high PF in the range of 0.98-1, except the CSI+SCaps, which has a low PF in the range of 0.62-0.94.

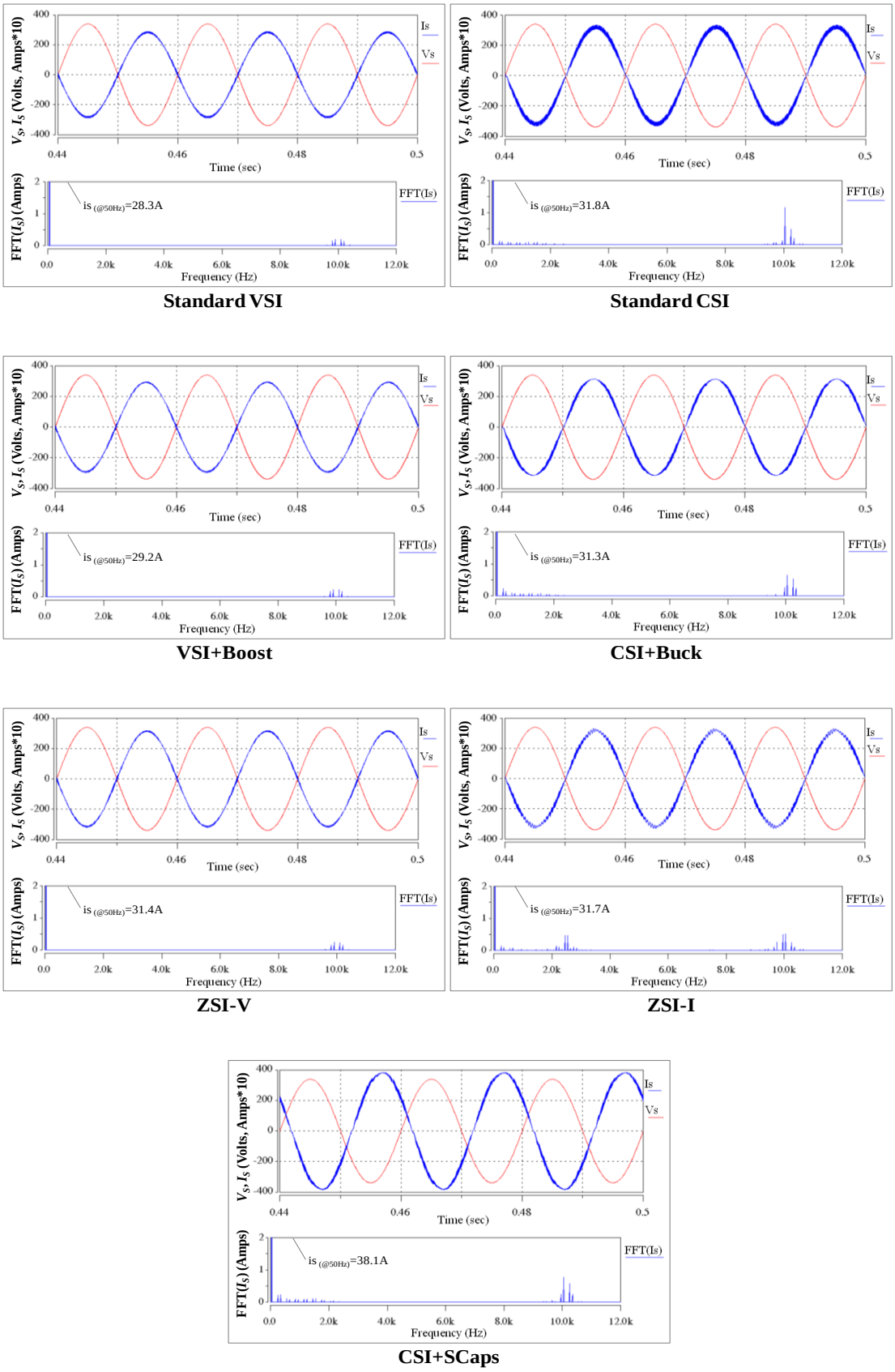


Figure 6.11 Output phase supply voltage (V_s) and phase supply current (I_s) simulation waveforms and the FFT spectra of phase supply current (FFT(i_s)) for all the candidate topologies operating at Full Power and Full Sun (FPFS)

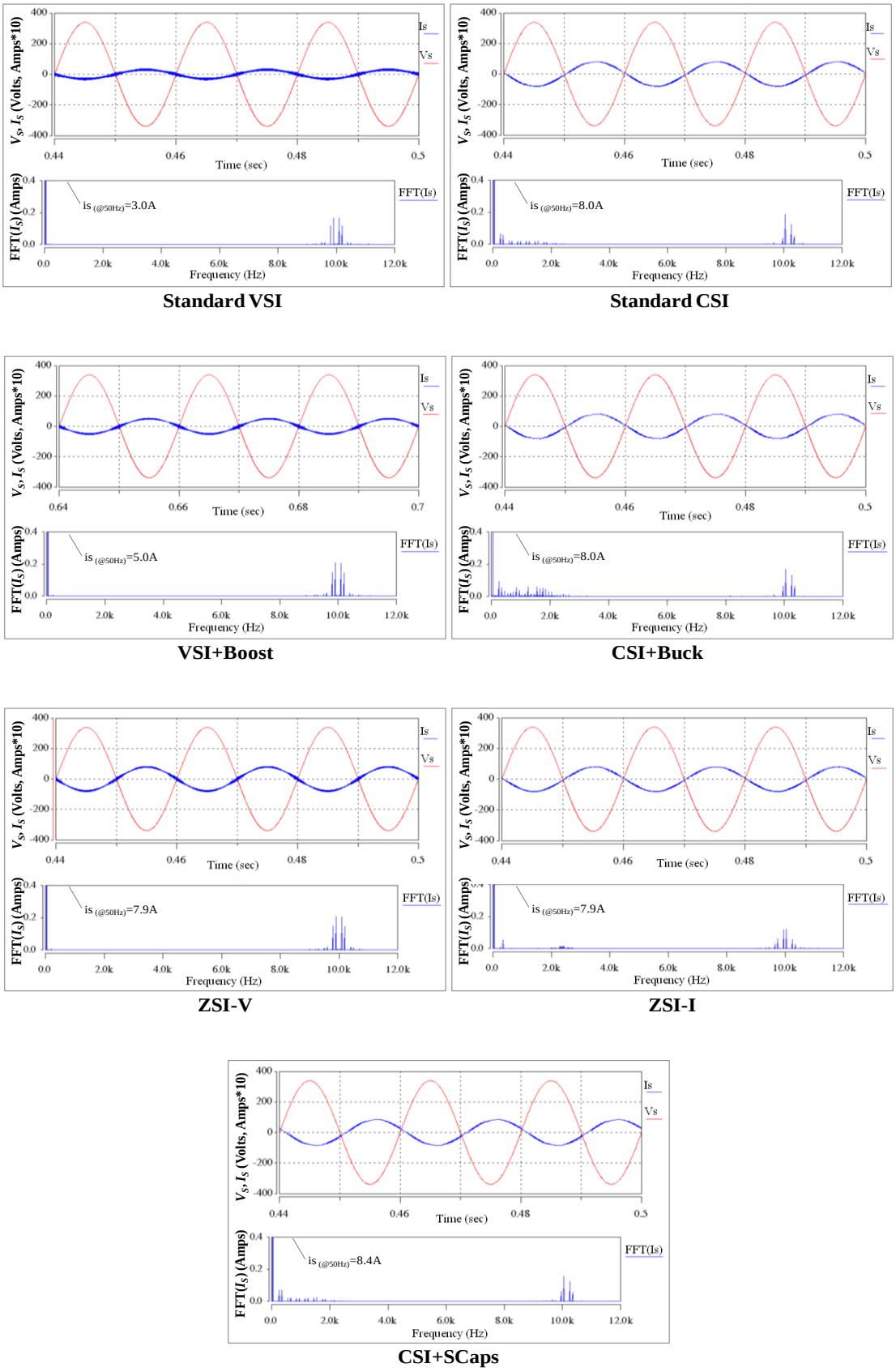


Figure 6.12 Output phase supply voltage (V_s) and phase supply current (I_s) simulation waveforms and the FFT spectra of phase supply current (FFT(I_s)) for all the candidate topologies operating at Low Power and Full Sun (LPFS)

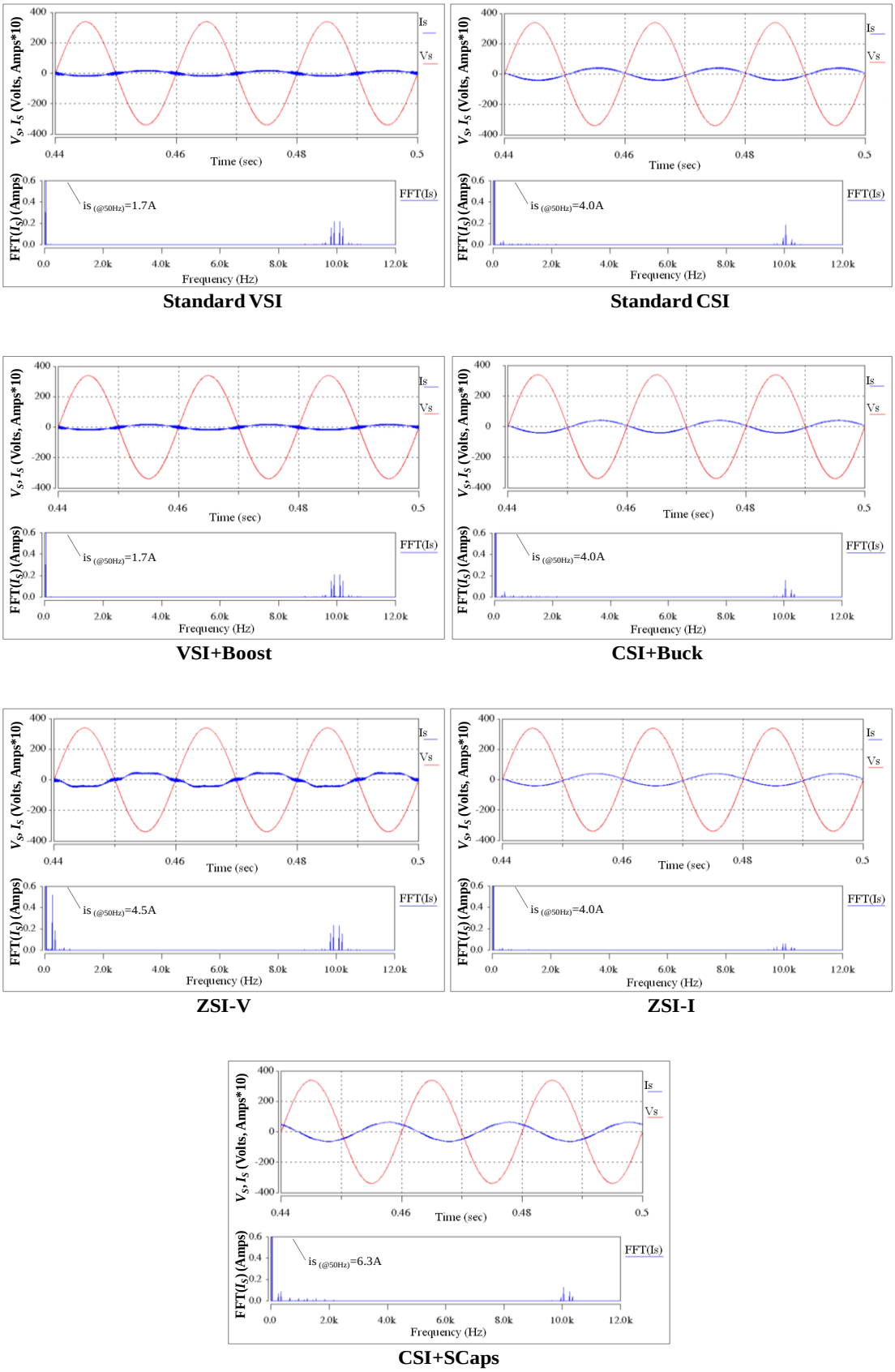


Figure 6.13 Output phase supply voltage (V_s) and phase supply current (I_s) simulation waveforms and the FFT spectra of phase supply current (FFT(I_s)) for all the candidate topologies operating at Light Power and Light Sun (LPLS)

The comparison of the average supply current THD and the output power factor for all the three operating points (in Table 6.7) for all the candidate topologies are shown in Figures 6.14-6.15.

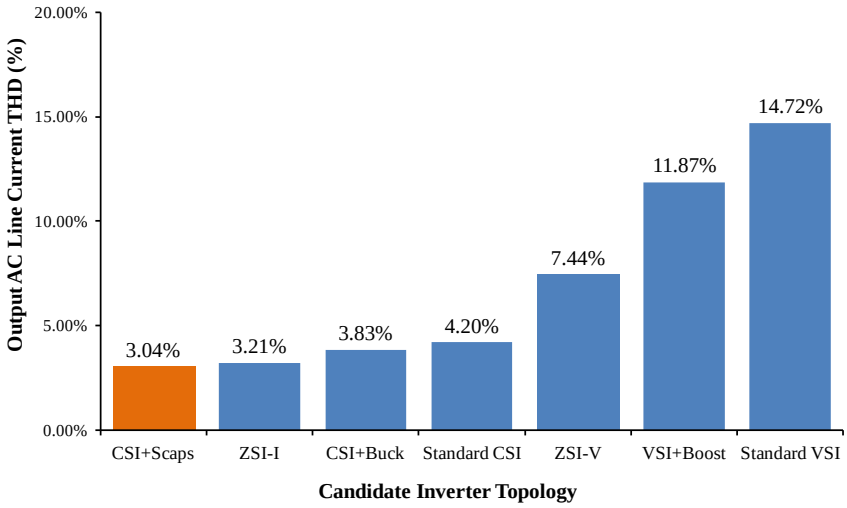


Figure 6.14 Average output supply current THD of each candidate inverter topology

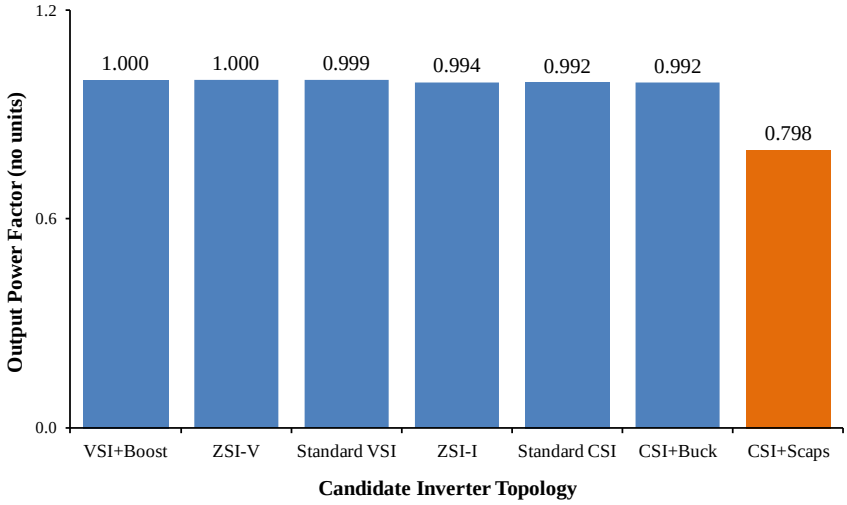


Figure 6.15 Average output power factor of each candidate inverter topology

It can be observed from Figures 6.14-6.15 that:

- The CSI+SCaps provides the lowest (the best) average output supply current THD among all of the candidate topologies
- The CSI+SCaps provides the lowest (the worst) average output AC power factor among all the candidate topologies

The low output current THD of the CSI+SCaps is a result of the addition of the series AC capacitors to the CSI circuit. As presented in Section 5.7.2, the series AC capacitors form a narrower low-pass band filter with the traditional LC filters. Therefore, the switching frequency harmonics generated from the converter are better attenuated using the CSI+SCaps topology. However, as presented in Section 5.5, the power factor is one of the control parameters used for the CSI+SCaps in order to achieve the minimum switching voltages and the optimum voltage-current transfer ratio (high modulation depth). As a result, the output power factor in the case of the CSI+SCaps cannot be independently controlled.

6.6 Comparison of Stress on Power Semiconductors

This section evaluates the voltage and current stress on the power semiconductors used in the CSI+SCaps in comparison with all the other candidate topologies. High voltage and current stress may shorten the working lifetime of the semiconductor devices more quickly and increase the potential for device destruction, which should be avoided. In this study, the voltage and current stress on the semiconductors are measured from the peak DC-link voltage and peak DC-link current.

Similar to the evaluation in Sections 6.4 and 6.5, all the candidate topologies were modelled and tested in the SABER simulation with the simulation parameters shown in Table 6.5 and the operating points explained in Section 6.3.2. Simulated waveforms of the DC-link voltage (v_{dc}) and DC-link current (i_{dc}) for all the candidate topologies are shown in Figures 6.16-6.18 and measured peak DC-link voltages and peak DC-link currents are summarised in Table 6.8.

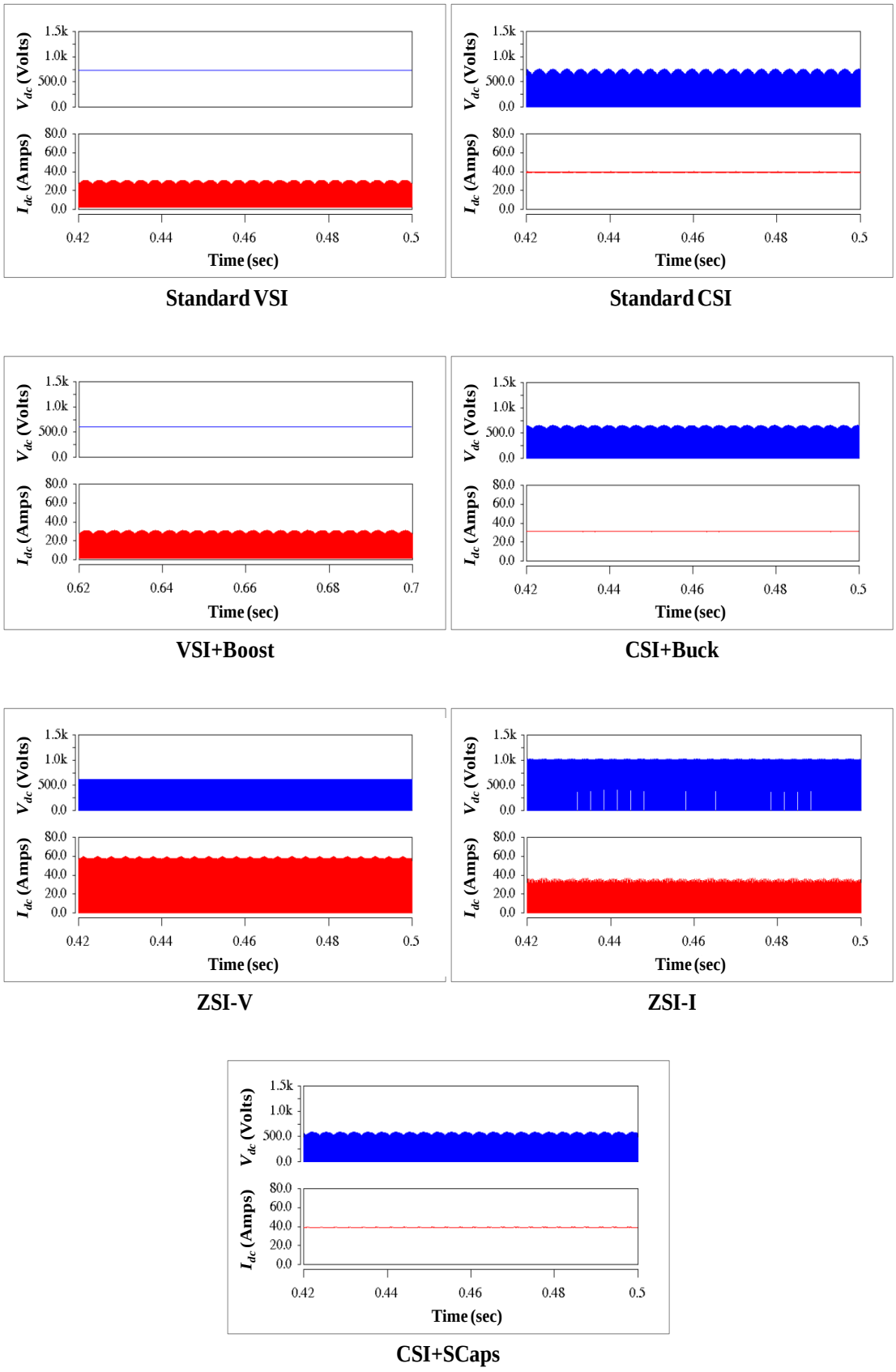


Figure 6.16 DC-link voltage (V_{dc}) and DC-link current (I_{dc}) simulation waveforms for all the candidate topologies operating at Full Power and Full Sun (FPFS)

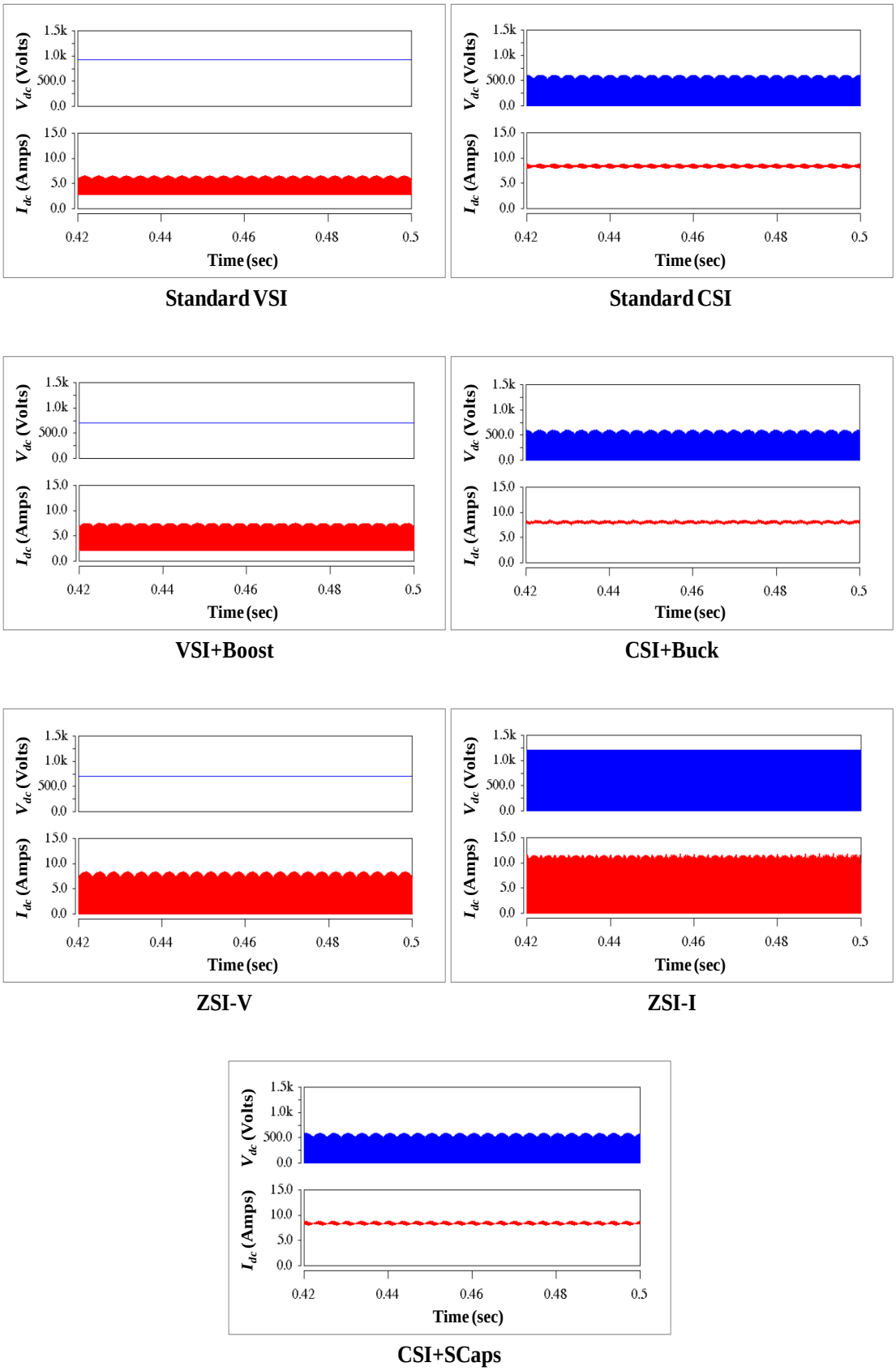


Figure 6.17 DC-link voltage (V_{dc}) and DC-link current (I_{dc}) simulation waveforms for all the candidate topologies operating at Low Power and Full Sun (LPFS)

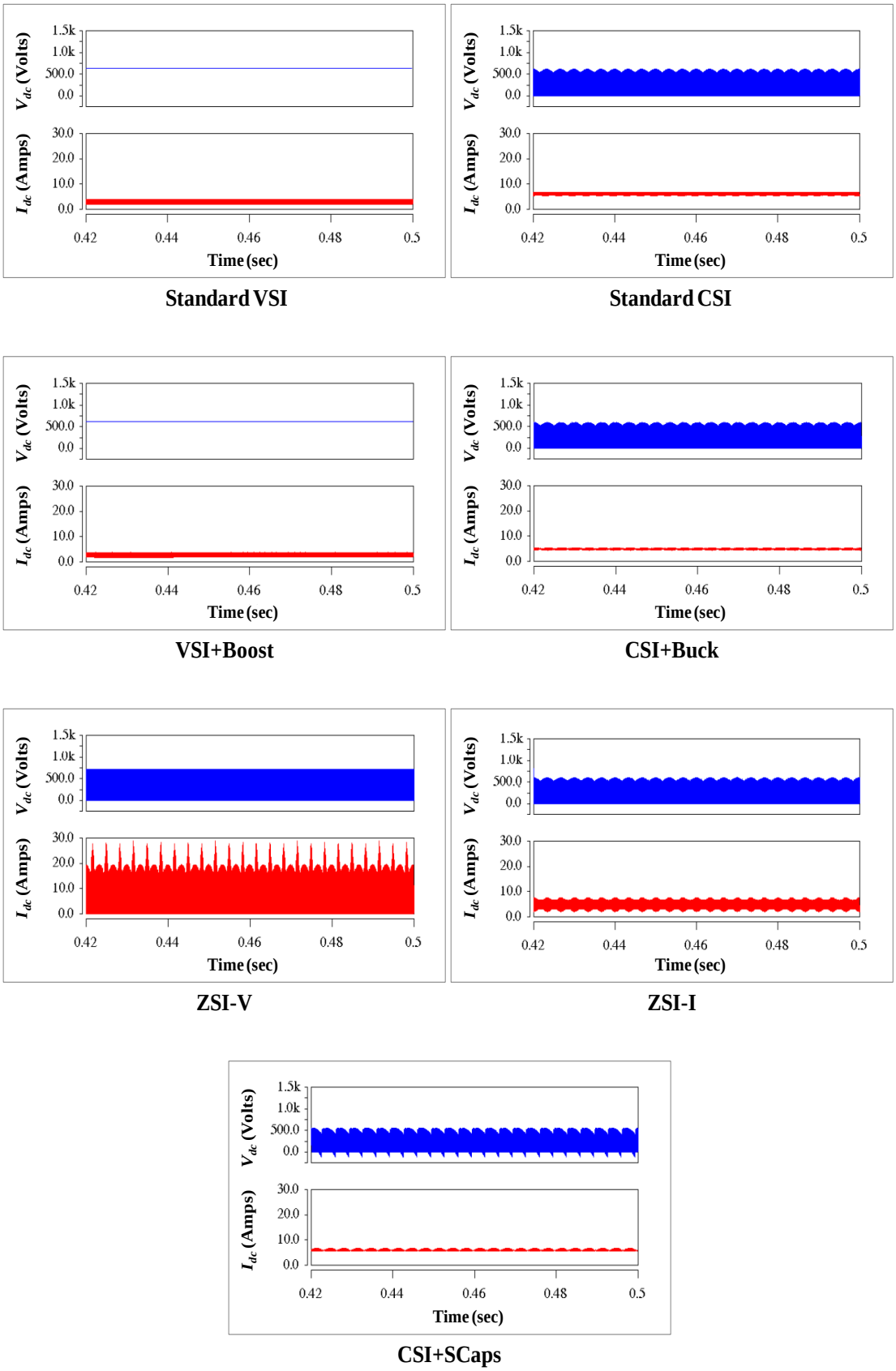


Figure 6.18 DC-link voltage (V_{dc}) and DC-link current (I_{dc}) simulation waveforms for all the candidate topologies operating at Light Power and Light Sun (LPLS)

Inverter Topology		Measured Peak DC-Link Voltage and Current					
		at FPFS		at LPFS		at LPLS	
		$v_{dc,pk}$ (V)	$i_{dc,pk}$ (A)	$v_{dc,pk}$ (V)	$i_{dc,pk}$ (A)	$v_{dc,pk}$ (V)	$i_{dc,pk}$ (A)
VSI	Standard VSI	733	31.0	928	6.6	635	4.0
	VSI+Boost	601	31.4	696	7.6	620	3.9
	ZSI-V	625	59.8	696	8.4	719	28.9
CSI	Standard CSI	752	40.1	611	8.9	614	6.8
	CSI+Buck	659	31.8	613	8.6	605	5.5
	ZSI-I	1023	37.0	1207	11.8	596	7.7
	CSI+SCaps	587	39.6	586	8.8	557	6.8

Table 6.8 Measured peak DC-link voltage and current for each candidate topology

It can be seen from the waveforms in Figures 6.16-6.18 and the figures in Table 6.8 that:

- In most cases, the VSI based topologies have an almost constant DC-link voltage but a large variation of the DC-link current, whilst the CSI based topologies have an almost constant DC-link current but a large variation of the DC-link voltage. However, when the ZSI-V operates with the "shoot-through" states (at FPFS and LPLS) and the ZSI-I with the "open-circuit" states (at FPFS and LPFS), these topologies have a large variation of both the DC-link voltage and DC-link current (see Figures 6.16 and 6.18 for the ZSI-V and Figures 6.16 and 6.17 for the ZSI-I).
- When not considering the ZSI topologies, the VSI based topologies have the highest levels of voltage stress (up to $927V_{pk}$) at the no load (LPFS) whilst the CSI based topologies have (up to $752V_{pk}$) at the rated MPP (FPFS). All the candidate topologies have the highest current stress at the rated MPP (FPFS). However, the CSI based topologies have the higher current stress (up to $40A_{pk}$) compared to the VSI based topologies (up to $31A_{pk}$).
- The ZSI-I provides the highest voltage stress ($1207V_{pk}$ at LPFS) and the ZSI-V provides the highest current stress ($59.8A_{pk}$ at FPFS) among all the candidate topologies.
- The CSI+SCaps have lower voltage and current stress (587V and 39.5A) than the standard CSI (752V and 40A) at all the operating points.

The maximum values of peak DC-link voltage and peak DC-link current of each candidate inverter topology in Table 6.7 can be used to represent the maximum voltage and current stress on the power semiconductors, a comparison of the maximum voltage and current stress on power semiconductors, for each topology, is shown in Figures 6.19-6.20.

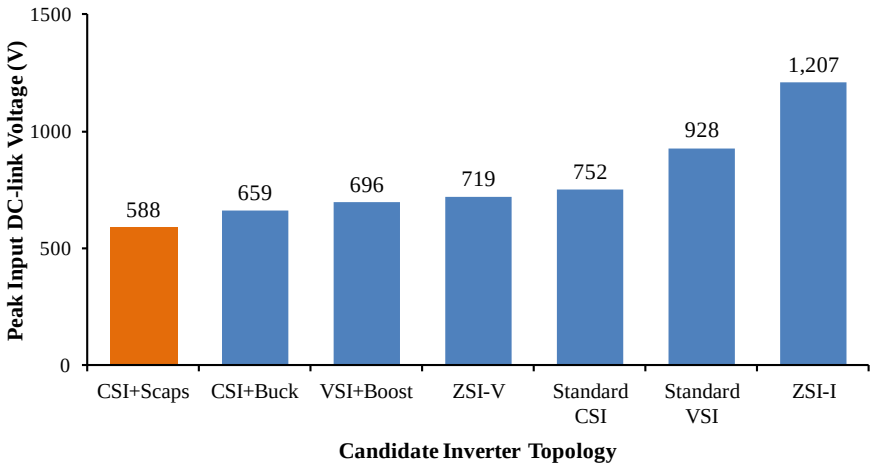


Figure 6.19 Maximum voltage stress on power semiconductors for each candidate topology

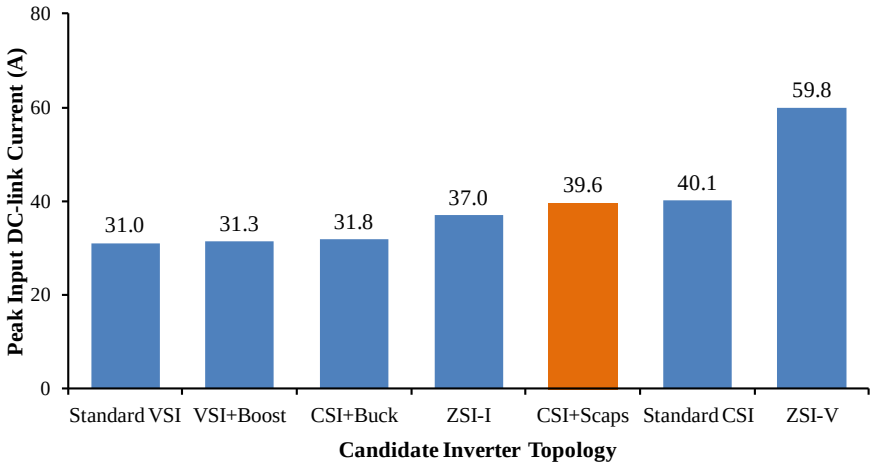


Figure 6.20 Maximum current stress on power semiconductors for each candidate inverter topology

It can be seen from Figures 6.19-6.20 that:

- The CSI+SCaps has the lowest voltage stress on power semiconductors among all the candidate topologies (see Figure 6.19).

- The CSI+SCaps has the high current stress on power semiconductors and is ranked 5th out of the seven candidate topologies (see Figure 6.20).

The low peak DC-link voltage (stress) on power semiconductors of the CSI+SCaps is a result of its high operating modulation depth, which transfers power from the DC side to the AC side with an optimum voltage and current level (as described in Section 6.2). The high peak DC-link current (stress) on power semiconductors is the effect of high operating PV current rating of the CSI+SCaps. However, despite the same PV current rating as a standard CSI, the CSI+SCaps provides lower (better) peak DC-link current than a standard CSI.

6.7 Comparison of Estimated Cost of Power Semiconductors

Besides high efficiency and high performance, minimum cost is also a main requirement of an ideal grid-tied PV converter. As presented in Section 3.3.3, power semiconductors are the most expensive components for the power circuit (12% of total converter cost). In this section, the estimated cost of power semiconductors for the CSI+SCaps topology is assessed in comparison to all of the other candidate topologies.

The power semiconductor cost estimation method proposed in [109] is used. The method utilses the maximum voltage and current stress (peak DC-link voltage and current) to identify a specific power installed in the power semiconductors ($\Sigma P_{sw}/P_{in}$) as expressed by (6.4). The parameter n_{sw} is the number of power semiconductors used, $V_{(dc,pk)}$ is the peak DC-link voltage, $I_{(dc,pk)}$ is the peak DC-link current, V_{pv} and I_{pv} are the average input voltage and average input current of the PV source.

$$\left(\sum \frac{P_{sw}}{P_{in}}\right) = n_{sw} \times \frac{\max\,(V_{dc,pk})\cdot\max\,(I_{dc,pk})}{\bar{V}_{pv}\bar{I}_{pv}} \qquad (6.4)$$

Using the information in Table 6.8 and the equation (6.4), the estimated cost of power semiconductors based on the specific power installed in power semiconductors for each candidate topology can be calculated as shown in Figure 6.21.

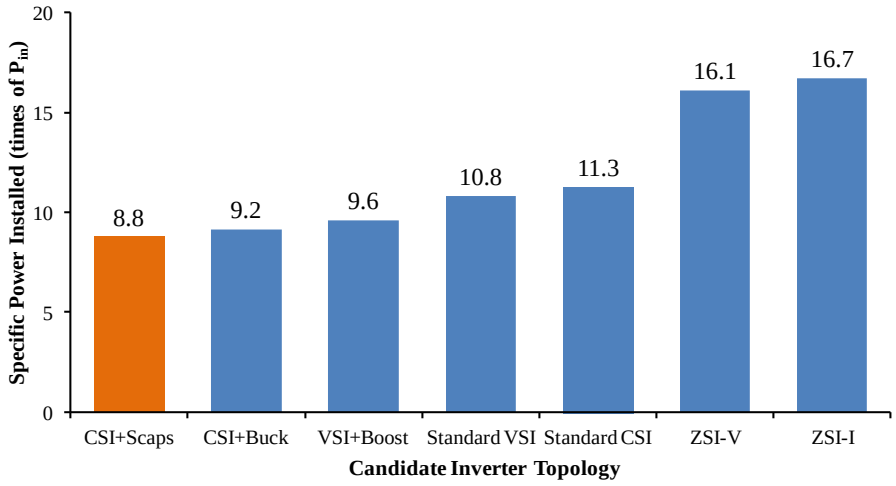


Figure 6.21 Specific power installed in power semiconductors (Estimated cost of power semiconductors) of each candidate inverter topology

It can be seen from Figure 6.21 that the CSI+SCaps has the lowest power installed in the power semiconductors. This result in the lowest cost of power semiconductors compared to all the other candidate topologies. The low installed power of the semiconductors for the CSI+SCaps is a result of the reduced number of semiconductors used in its circuit and the capability to operate with high modulation depth.

6.8 Comparison of Estimated Semiconductor Power Losses

This section evaluates the power losses of the power semiconductors for the CSI+SCaps in comparison with all of the other candidate topologies. The semiconductor power losses are the major losses that reduce the overall power conversion efficiency of the power converters.

The semiconductor power losses can be divided into two types: *conduction power loss* (P_{cond}) and *switching power loss* (P_{sw}) [77]. The conduction power loss is that associated with the device conduction of current whereas the switching power loss is a result of the imperfect operation of the semiconductors when changing from the "on" to "off" (or "off" to "on") states. In this study, the semiconductor power losses for all the candidate topologies were estimated using the methods proposed in [34,

110, 111]. These methods define the conduction power loss and the switching power loss as (6.5)-(6.9); where the parameters in (6.5)-(6.9) are described in Table 6.9.

$$P_{cond} = \frac{1}{T_{sim}} \int_0^{T_{sim}} [(V_{CEO} + r_d \cdot I_{c-on}) \cdot I_{c-on}] \cdot dt \quad (6.5)$$

$$P_{sw-on} = \frac{1}{2T_{sim}} \sum_{t=0}^{T_{sim}} [(V_{ce-on} \cdot I_{c-on}) \cdot t_{on+rr}] \quad (6.6)$$

$$P_{sw-off} = \frac{1}{2T_{sim}} \sum_{t=0}^{T_{sim}} \left[\left(V_{ce-off} \cdot I_{c-off}\right) \cdot t_{off}\right] \quad (6.7)$$

$$t_{on+rec} = \frac{2 \cdot (E_{on} + E_{rec})}{\{V_{CE} \cdot I_C\}_{datasheet}} \quad (6.8)$$

$$t_{off} = \frac{2 \cdot (E_{off})}{\{V_{CE} \cdot I_C\}_{datasheet}} \quad (6.9)$$

Parameter	Description	Type	Unit	Data Source
t	simulation time	variable	sec	-
$V_{ce\text{-}on/off}$	collector-emitter voltage during turning on/off state	variable	V	from measurement
$I_{c\text{-}on/off}$	collector current during turning on/off state	variable	A	from measurement
T_{sim}	ending time of the simulation	constant	sec	defined by user/program
V_{CEO}	internal conducting collector-emitter voltage	constant	V	estimated from datasheet
r_d	device conducting resistor	constant	Ω	estimated from datasheet
t_{on+rec}	turn on + reverse recovery time	constant	sec	estimated from datasheet
t_{off}	turn off time	constant	sec	estimated from datasheet
E_{on+rec}	turn on + reverse recovery Energy	constant	J	taken from datasheet
E_{off}	turn off Energy	constant	J	taken from datasheet
V_{CE}	collector-emitter voltage at the test condition	constant	V	taken from datasheet
I_C	collector current at the test condition	constant	A	take from datasheet

Table 6.9 Parameters and description of the parameters used for the estimation of the semiconductor power losses

From Table 6.9, the parameters $V_{ce\text{-}on/off}$ and I_c can be directly measured from the simulation waveforms whilst the other parameters can be determined from the datasheets. The method to determine the estimated values for the parameters V_{CEO}, r_d, t_{on+rr} and t_{off} from the datasheets can be determined using the procedure described in Table 6.10 and Figures 6.22-6.23 [34].

Parameter	Procedure
V_{CEO}	Considering the I_C-V_{CE} curve in the datasheet. Using a straight line to represent the average I_C-V_{CE} curve as shown in Figure 6.22, V_{CEO} can be found at the crossing point between the line and the V_{CE} axis (where I_C is equal to zero)
r_d	Using the same procedure used to determine V_{CEO}, but r_d is the slope of the straight line (see Figure 6.22).
t_{on+rec}	Considering the E_{on-rec}-I_C curve in the datasheet. Using the operating current (I_C) to find E_{on} and E_{rec} from the curve and using the given V_{CE} specification for that test condition in the datasheet (see Figure 6.23a), t_{on+rec} can be determined from (6.8).
t_{off}	Considering the E_{off}-I_C curve in the datasheet. Using the operating current (I_C) to find E_{off} from the curve and using the given V_{CE} specification for that test condition in the datasheet (see Figure 6.23b), t_{off} can be determined from (6.9).

Table 6.10 Procedure used to determine the parameters V_{CEO}, r_d, t_{on+rr} and t_{off} for the estimation of the semiconductor power losses

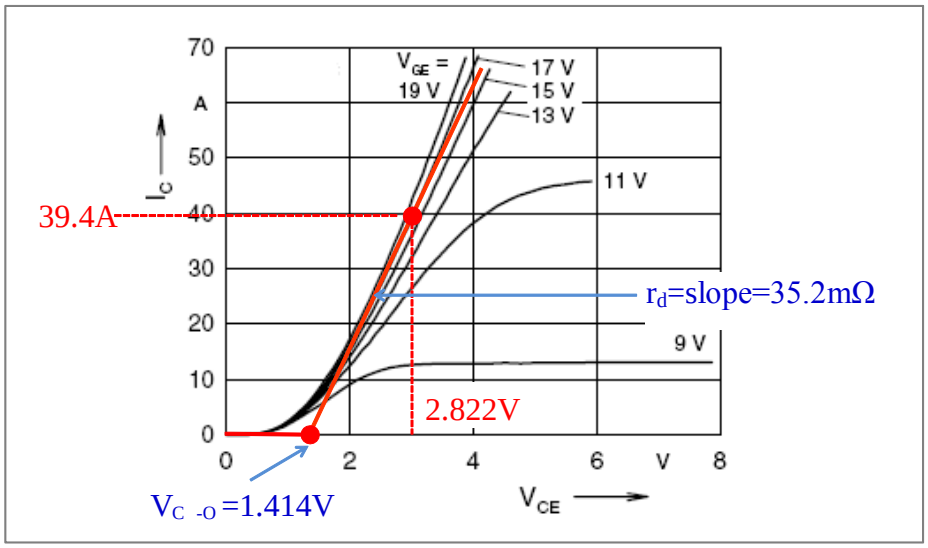
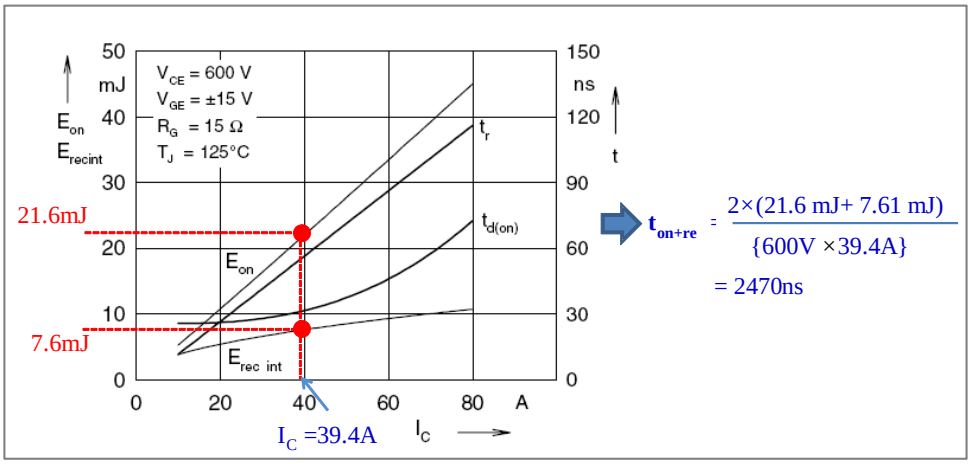
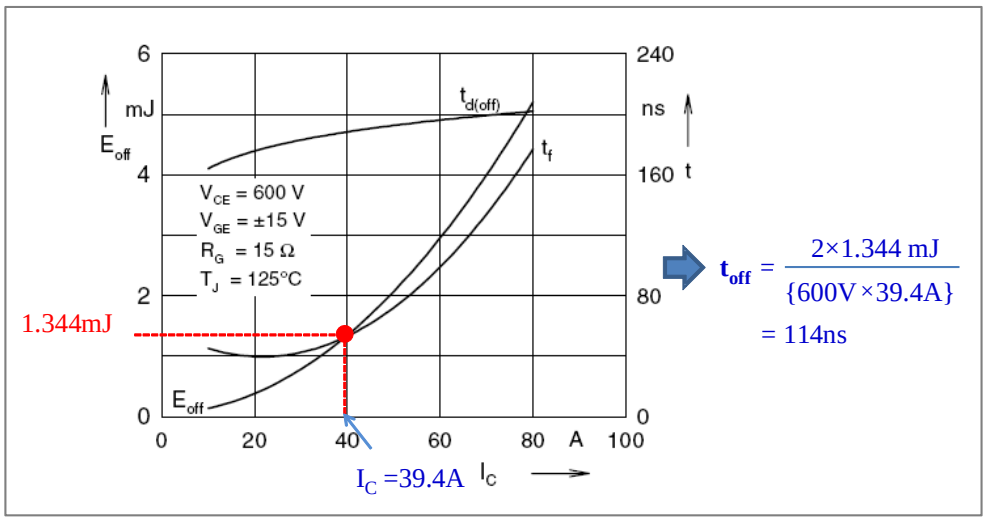


Figure 6.22 Methods used to determine V_{CE-O} and r_d for the estimation of the semiconductor power losses



(a)



(b)

Figure 6.23 Methods used to determine (a) t_{on+rr} and (b) t_{off} for the estimation of the semiconductor power losses

In this study, the IGBTs and Diodes of type MWI25-12E7 [112] are used for the VSI based candidate topologies and the RB-IGBTs of type IXRH 40N120 [113] are used for the CSI based candidate topologies. These power semiconductors have similar typical V_{CE} and I_C ratings (1200V and 52-55A), which are selected to match to the specifications of the electricity network and the PV source used for the evaluation in this chapter (as presented in Table 6.2). By following the procedure shown in Table 6.10 and Figures 6.22-6.23 and using the specifications of the selected power semiconductors, the values of the parameters used for the semiconductor power loss estimation at the operating points described in Section 6.3.2 for all the candidate topologies are determined, as shown in Table 6.11.

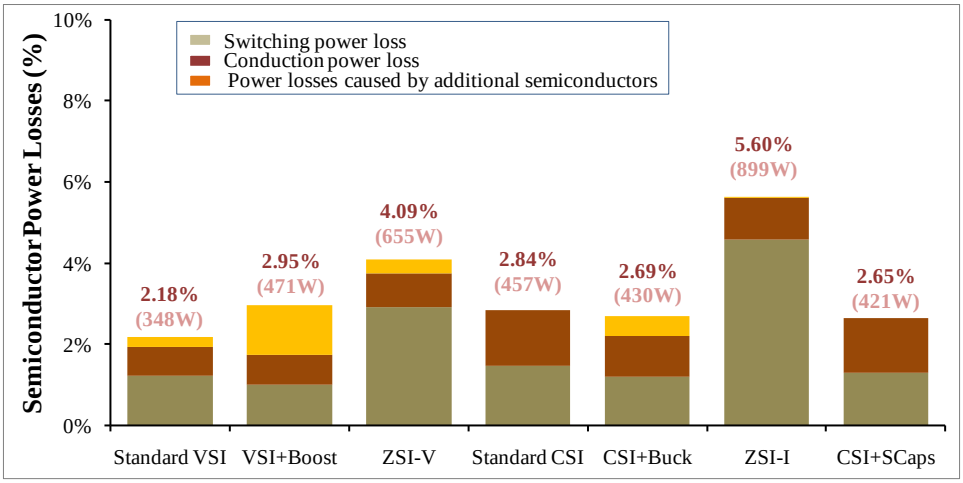
Inverter Topology		Parameters and Their Values											
		at FPFS				at LPFS				at LPLS			
		$V_{ceo\text{-}IGBT}$, ($V_{ceo\text{-}FRD}$) (V)	$r_{d\text{-}IGBT}$, ($r_{d\text{-}FRD}$) (mΩ)	$t_{on+rrec}$ (ns)	t_{off} (ns)	$V_{ceo\text{-}IGBT}$, ($V_{ceo\text{-}FRD}$) (V)	$r_{d\text{-}IGBT}$, ($r_{d\text{-}FRD}$) (mΩ)	$t_{on+rrec}$ (ns)	t_{off} (ns)	$V_{ceo\text{-}IGBT}$, ($V_{ceo\text{-}FRD}$) (V)	$r_{d\text{-}IGBT}$, ($r_{d\text{-}FRD}$) (mΩ)	$t_{on+rrec}$ (ns)	t_{off} (ns)
VSI	Standard VSI	1.208 (1.120)	38.1 (29.4)	700	268	1.208 (1.120)	38.1 (29.4)	909	485	1.208 (1.120)	38.1 (29.4)	1094	563
	VSI+Boost	1.208 (1.120)	38.1 (29.4)	696	253	1.208 (1.120)	38.1 (29.4)	816	414	1.208 (1.120)	38.1 (29.4)	1031	496
	ZSI-V	1.208 (1.120)	38.1 (29.4)	696	253	1.208 (1.120)	38.1 (29.4)	816	414	1.208 (1.120)	38.1 (29.4)	1031	496
CSI	Standard CSI	1.414	35.2	2470	114	1.414	35.2	3095	63	1.414	35.2	3388	55
	CSI+Buck	1.414 (1.120)	35.2 (29.4)	2709	95	1.414	35.2	3383	55	1.414	35.2	3673	68
	ZSI-I	1.414 (1.120)	35.2 (29.4)	2709	95	1.414	35.2	3383	55	1.414	35.2	3673	68
	CSI+SCaps	1.414	35.2	2470	114	1.414	35.2	3095	63	1.414	35.2	3388	55

Table 6.11 Parameters and their values used for the estimation of the power semiconductor power losses for all the candidate topologies at the operating points FPFS, LPFS and LPLS

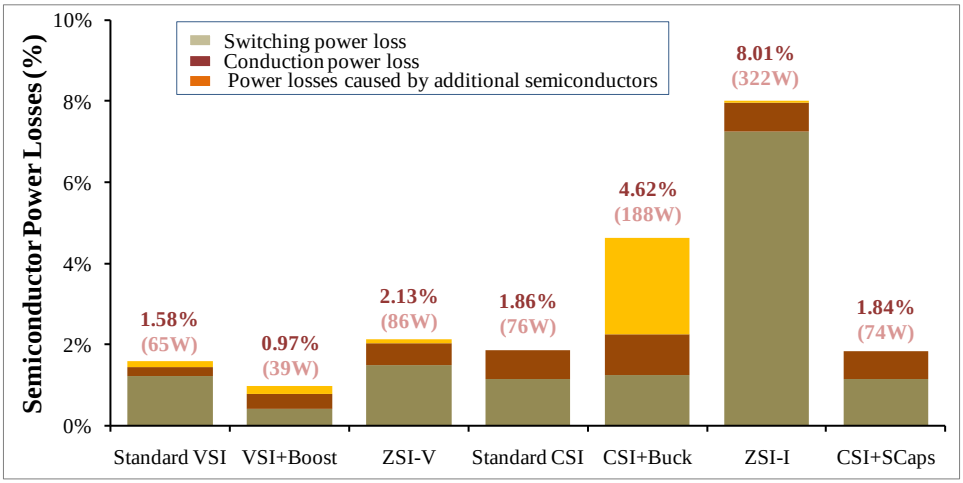
With the use of the equations (6.5)-(6.9) and the parameters in Table 6.11, the estimated conduction power loss (P_{cond}), switching power loss (P_{sw}), power losses caused by the additional components (P_{add}) and total semiconductor power loss ($P_{loss\text{-}tt}$) for each candidate topology can be calculated and obtained as shown in Table 6.12. Figure 6.24 shows the graphical presentation of the information in Table 6.12. It is noted that P_{add} is the summation of the conduction losses and switching losses of the semiconductors in the additional circuits.

Inverter Topology		Estimated Semiconductor Power losses											
		at FPFS				at LPFS				at LPLS			
		P_{sw}	P_{cond}	P_{add}	$P_{loss\text{-}tt}$	P_{sw}	P_{cond}	P_{add}	$P_{loss\text{-}tt}$	P_{sw}	P_{cond}	P_{add}	$P_{loss\text{-}tt}$
VSI	Standard VSI	196W (1.23%)	113W (0.71%)	38W (0.24%)	348W (2.18%)	50W (1.21%)	10W (0.24%)	6W (0.14%)	65W (1.58%)	25W (1.21%)	6W (0.30%)	4W (0.19%)	35W (1.70%)
	VSI+Boost	158W (0.99%)	119W (0.75%)	193W (1.21%)	471W (2.95%)	16W (0.41%)	15W (0.38%)	7W (0.19%)	39W (0.97%)	21W (1.03%)	6W (0.29%)	59W (2.83%)	86W (4.15%)
	ZSI-V	467W (2.92%)	133W (0.83%)	55W (0.34%)	655W (4.09%)	60W (1.50%)	22W (0.54%)	4W (0.10%)	86W (2.13%)	91W (4.37%)	16W (0.78%)	6W (0.30%)	114W (5.45%)
CSI	Standard CSI	236W (1.47%)	220W (1.37%)	-	457W (2.84%)	47W (1.15%)	29W (0.71%)	-	76W (1.86%)	34W (1.69%)	20W (0.98%)	-	54W (2.67%)
	CSI+Buck	192W (1.20%)	159W (0.99%)	79W (0.50%)	430W (2.69%)	50W (1.24%)	41W (1.01%)	96W (2.37%)	188W (4.62%)	30W (1.47%)	15W (0.77%)	8W (0.38%)	53W (2.62%)
	ZSI-I	736W (4.59%)	162W (1.01%)	1W (0.0%)	899W (5.60%)	291W (7.24%)	29W (0.72%)	2W (0.05%)	322W (8.01%)	42W (2.09%)	16W (0.77%)	-	58W (2.86%)
	CSI+SCaps	204W (1.28%)	217W (1.36%)	-	421W (2.65%)	46W (1.13%)	29W (0.71%)	-	75W (1.84%)	31W (1.53%)	20W (0.98%)	-	51W (2.51%)

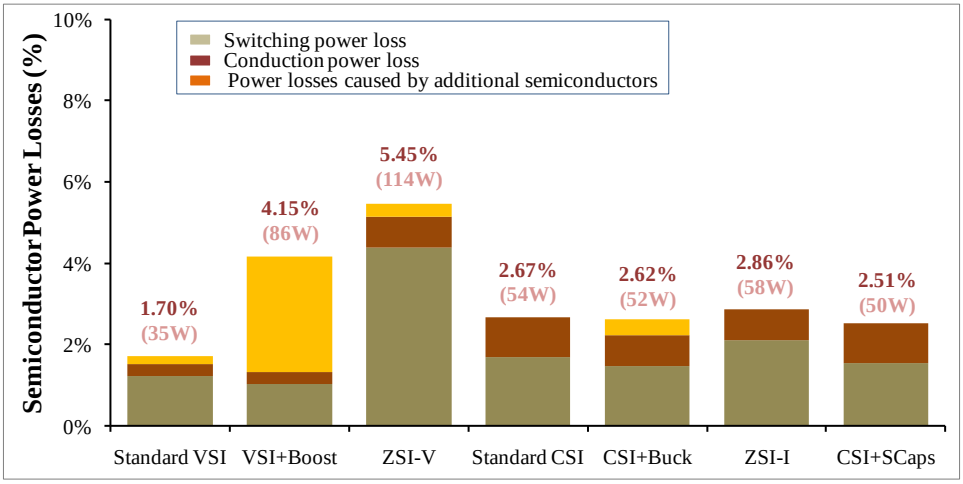
Table 6.12 Estimated semiconductor power losses for all the candidate topologies at the operating points FPFS, LPFS and LPLS



(a) FPFS



(b) LPFS



(c) LPLS

Figure 6.24 Estimated semiconductor power losses for each candidate inverter topology at (a) FPFS, (b) LPFS and (c) LPLS

It can be seen from Table 6.12 and Figure 6.24 that:

- All the candidate topologies provide higher total power loss when operating at higher power levels, as expected for most hard switched power converters, i.e. the converters generate the total loss up to 899W at FPFS (16kW), 322W at LPFS (4kW) and 114W at LPLS (2kW).
- In most cases, the switching loss is the major loss for the candidate topologies with 55-61% of the total loss; where the conduction loss and additional loss contribute 24-33% and 11-14% respectively. The ZSI topologies have the highest switching loss compared to all the other candidate topologies, due to their high DC-link voltage and increased current stress (as explained in Section 6.6).
- The CSI based topologies provides higher conduction loss (55% on average) than the VSI based topologies at all the operating points. The CSI+SCaps and standard CSI provide higher conduction loss than all the other topologies. However, the CSI+SCaps has lower total loss than the standard CSI (up to 7.9%).
- The VSI+Boost and the CSI+Buck have high additional losses when the boost and buck converters operate whilst only the CSI+SCaps and the standard CSI do not have additional power losses.

If the total semiconductor power loss for all the three operating points is considered, the comparison of total semiconductor power loss for all candidate topologies would result as shown in Figure 6.25. It can be seen that the CSI+SCaps can achieve low total semiconductor power loss and is ranked 2nd out of the seven candidate topologies.

Although the CSI+SCaps has a high conduction power loss (as does a standard CSI), the CSI+SCaps has low total semiconductor loss. This is because of the fact that the CSI+SCaps does not have any other power loss caused by the additional components. Moreover, the CSI+SCaps can operate with a reduced DC-link voltage where the power semiconductors can switch a lower voltage level and therefore lower switching loss. This leads to a great reduction in the overall power loss in the semiconductors for the CSI+SCaps topology.

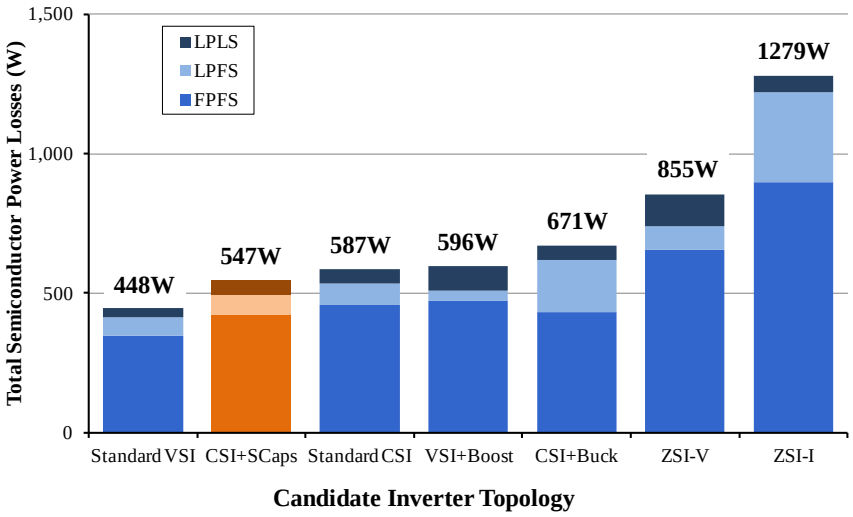


Figure 6.25 Total semiconductor power loss for each candidate inverter topology

6.9 Comparison of Estimated Inverter Efficiency

As mentioned in Chapter 3, grid-tied PV power converters are required to operate with high efficiency at every MPP of the PV source for high PV power extraction. However, different converter types may require different MPP ratings, which would be difficult for comparison. Therefore, in order to allow the efficiency of different converter types to be compared, an efficiency calculation method such as *European Efficiency* (η_{euro}) should be used (details of this method can be seen in Section 3.3).

In this section, the efficiency of the CSI+SCaps based on the European Efficiency consideration is compared for all of the candidate topologies. As required by the European Efficiency equation (equation (3.3) in Section 3.3), the efficiencies (η) of the topologies operating at the MPP under 5%, 10%, 20%, 30%, 50% and 100% sun irradiance levels are needed. The methods used to estimate the semiconductor power loss described in Section 6.8 are utilised to determine these efficiencies using (6.10).

$$\eta_x = \frac{P_{mpp(x)} - P_{loss(total,x)}}{P_{mpp(x)}} \times 100\% \quad ; x = 5\%, 10\%, 20\%, 30\%, 50\% \text{ and } 100\% \qquad (6.10)$$

The estimated efficiencies for all the candidate topologies at the operating points required for the European Efficiency calculation are determined by the following procedures:

- First, the input voltage (V_{mpp}), current (I_{mpp}) and power (P_{mpp}) of the PV source when the candidate topologies operate at the rated MPP under 5%, 10%, 20%, 30%, 50% and 100% sun irradiance levels are determined. The specifications of the PV source presented in Table 6.2 and the operating modulation depths shown in Figure 6.2 are used to calculate these parameters and give the results shown in Table 6.13.

- Then, the information in Table 6.13 is used to determine the values of the parameters $E_{on+rrec}$, E_{off}, $T_{on+rrec}$ and T_{off}; where the parameters V_{CEO} and r_d can be used from Table 6.11. These parameters can be determined by following the methods described in Section 6.8. The values of these parameters are shown in Table 6.14.

- Substituting the parameters in Table 6.14 for equations (6.5)-(6.7), the estimated power losses are obtained, as shown in Table 6.15.

- Finally, substituting the values of P_{mpp} (from Table 6.13) and $P_{loss(total)}$ (from Table 6.13) for equation (6.10), the estimated efficiencies can be determined. The results are presented in Table 6.16. The plots of the results in Table 6.16 are illustrated in Figure 2.26.

Sun Irradiance level	Inverter Topology	PV Parameters		
		V_{mpp} (V)	I_{mpp} (A)	P_{mpp} (W)
100%	Standard VSI	733	21.8	15979.4
	VSI+Boost	586	27.3	15997.8
	ZSI-V	586	27.3	15997.8
	Standard CSI	406	39.4	15996.4
	CSI+Buck	508	31.5	16002.0
	ZSI-I	508	31.5	16002.0
	CSI+SCaps	406	39.4	15996.4
50%	Standard VSI	700	11.4	7980.0
	VSI+Boost	560	14.3	8008.0
	ZSI-V	560	14.3	8008.0
	Standard CSI	388	20.6	7992.8
	CSI+Buck	485	16.5	8002.5
	ZSI-I	485	16.5	8002.5
	CSI+SCaps	388	20.6	7992.8
30%	Standard VSI	670	7.2	4824.0
	VSI+Boost	536	9.0	4824.0
	ZSI-V	536	9.0	4824.0
	Standard CSI	371	13.0	4823.0
	CSI+Buck	464	10.4	4825.6
	ZSI-I	464	10.4	4825.6
	CSI+SCaps	371	13.0	4823.0
20%	Standard VSI	650	4.9	3185.0
	VSI+Boost	520	6.2	3224.0
	ZSI-V	520	6.2	3224.0
	Standard CSI	360	8.9	3204.0
	CSI+Buck	450	7.1	3195.0
	ZSI-I	450	7.1	3195.0
	CSI+SCaps	360	8.9	3204.0
10%	Standard VSI	635	3.2	2032.0
	VSI+Boost	476	4.3	2046.8
	ZSI-V	476	4.3	2046.8
	Standard CSI	330	6.1	2013.0
	CSI+Buck	413	4.9	2023.7
	ZSI-I	413	4.9	2023.7
	CSI+SCaps	330	6.1	2013.0
5%	Standard VSI	610	1.3	793.0
	VSI+Boost	450	1.8	810.0
	ZSI-V	450	1.8	810.0
	Standard CSI	315	2.5	787.5
	CSI+Buck	395	2.0	790.0
	ZSI-I	395	2.0	790.0
	CSI+SCaps	315	2.5	787.5

Table 6.13 Input voltage (V_{mpp}), current (I_{mpp}) and power (P_{mpp}) of the candidate topologies operating at the MPP under 5%, 10%, 20%, 30%, 50% and 100% sun irradiance levels

Sun Irradiance level	Inverter Topology	Power Loss Estimation Parameters						
		V_{CE} (V)	I_C (A)	E_{rr} (mJ)	E_{on} (mJ)	E_{off} (mJ)	T_{on+rr} (ns)	T_{onff} (ns)
100%	Standard VSI	600	21.8	1.5	3.08	1.75	700	268
	VSI+Boost	600	27.3	1.7	4	2.07	696	253
	ZSI-V	600	27.3	1.7	4	2.07	696	253
	Standard CSI	600	39.4	7.6	21.6	1.33	2470	113
	CSI+Buck	600	31.5	7.2	18.4	0.9	2709	95
	ZSI-I	600	31.5	7.2	18.4	0.9	2709	95
	CSI+SCaps	600	39.4	7.6	21.6	1.33	2470	113
50%	Standard VSI	600	11.4	0.94	1.62	1.06	749	310
	VSI+Boost	600	14.3	1.11	2	1.28	725	298
	ZSI-V	600	14.3	1.11	2	1.28	725	298
	Standard CSI	600	20.6	5.6	11.2	0.39	2718	63
	CSI+Buck	600	16.5	5.2	9	0.3	2869	61
	ZSI-I	600	16.5	5.2	9	0.3	2869	61
	CSI+SCaps	600	20.6	5.6	11.2	0.39	2718	63
30%	Standard VSI	600	7.2	0.68	0.94	0.81	750	375
	VSI+Boost	600	9	1.11	1.28	0.91	885	337
	ZSI-V	600	9	1.11	1.28	0.91	885	337
	Standard CSI	600	13	4.4	7	0.2	2923	51
	CSI+Buck	600	10.4	4	5.4	0.16	3013	51
	ZSI-I	600	10.4	4	5.4	0.16	3013	51
	CSI+SCaps	600	13	4.4	7	0.2	2923	51
20%	Standard VSI	600	4.9	0.51	0.94	0.72	986	490
	VSI+Boost	600	6.2	0.6	1.02	0.74	871	398
	ZSI-V	600	6.2	0.6	1.02	0.74	871	398
	Standard CSI	600	8.9	0.38	5	0.16	2015	60
	CSI+Buck	600	7.1	0.34	4.5	0.14	2272	66
	ZSI-I	600	7.1	0.34	4.5	0.14	2272	66
	CSI+SCaps	600	8.9	0.38	5	0.16	2015	60
10%	Standard VSI	600	3.2	0.3	0.75	0.54	1094	563
	VSI+Boost	600	4.3	0.5	0.83	0.64	1031	496
	ZSI-V	600	4.3	0.5	0.83	0.64	1031	496
	Standard CSI	600	6.1	3	3.2	0.1	3388	55
	CSI+Buck	600	4.9	2.8	2.6	0.1	3673	68
	ZSI-I	600	4.9	2.8	2.6	0.1	3673	68
	CSI+SCaps	600	6.1	3	3.2	0.1	3388	55
5%	Standard VSI	600	1.3	0.25	0.5	0.47	1923	1205
	VSI+Boost	600	1.8	0.27	0.56	0.52	1537	963
	ZSI-V	600	1.8	0.27	0.56	0.52	1537	963
	Standard CSI	600	2.5	1.5	1.3	0.08	3733	107
	CSI+Buck	600	2	1.3	1.1	0.08	4000	133
	ZSI-I	600	2	1.3	1.1	0.08	4000	133
	CSI+SCaps	600	2.5	1.5	1.3	0.08	3733	107

Table 6.14 Power loss estimation parameters and their values for all the candidate topologies operating at the MPP under 5%, 10%, 20%, 30%, 50% and 100% sun irradiance levels

Sun Irradiance level	Inverter Topology	Semiconductor Power Losses								
		PWM Bridge Circuit				Additional Circuit				Total
		$P_{sw\text{-}on+rr}$ (W)	$P_{sw\text{-}off}$ (W)	$P_{cond\text{-}igbt}$ (W)	$P_{cond\text{-}frd}$ (W)	$P_{sw\text{-}on+rr}$ (W)	$P_{sw\text{-}off}$ (W)	$P_{cond\text{-}igbt}$ (W)	$P_{cond\text{-}frd}$ (W)	$P_{loss(total)}$ (W)
100%	Standard VSI	136.97	55.42	101.40	11.81	-	-	-	38.46	344.06
	VSI+Boost	113.30	43.85	115.06	4.43	116.21	43.92	7.49	17.01	461.27
	ZSI-V	333.19	141.75	126.69	5.92	-	-	-	55.21	662.76
	Standard CSI	235.03	3.99	220.24	-	-	-	-	-	459.26
	CSI+Buck	178.25	3.15	158.66	-	-	-	-	79.46	419.52
	ZSI-I	653.14	43.47	161.66	-	-	-	-	0.78	859.05
	CSI+SCaps	203.17	3.04	217.13	-	-	-	-	-	423.34
50%	Standard VSI	65.70	30.62	38.09	3.57	-	-	-	16.71	154.69
	VSI+Boost	58.00	26.00	42.12	2.03	67.58	29.01	14.60	20.13	259.47
	ZSI-V	194.62	107.96	54.78	2.70	-	-	-	23.37	383.43
	Standard CSI	112.00	1.74	87.82	-	-	-	-	-	201.56
	CSI+Buck	91.51	1.37	65.69	-	-	-	-	13.75	172.32
	ZSI-I	155.77	3.01	66.25	-	-	-	-	-	225.03
	CSI+SCaps	98.25	1.48	88.41	-	-	-	-	-	188.14
30%	Standard VSI	36.37	19.53	19.26	1.31	-	-	-	9.54	86.01
	VSI+Boost	33.64	16.45	21.09	0.77	44.80	20.41	9.40	11.04	157.6
	ZSI-V	126.85	90.03	31.71	1.33	-	-	-	13.06	262.98
	Standard CSI	68.70	1.01	48.49	-	-	-	-	-	118.2
	CSI+Buck	56.10	0.74	36.93	-	-	-	-	10.90	104.67
	ZSI-I	94.89	1.67	36.97	-	-	-	-	-	133.53
	CSI+SCaps	60.81	0.91	48.85	-	-	-	-	-	110.57
20%	Standard VSI	20.22	13.38	9.97	0.42	-	-	-	5.68	49.67
	VSI+Boost	21.35	12.04	11.94	0.37	34.00	16.85	8.65	6.86	112.06
	ZSI-V	89.73	87.26	21.60	0.77	-	-	-	8.51	207.87
	Standard CSI	49.16	0.72	30.63	-	-	-	-	-	80.51
	CSI+Buck	39.48	0.58	23.56	-	-	-	-	8.26	71.88
	ZSI-I	63.71	1.33	23.61	-	-	-	-	-	88.65
	CSI+SCaps	42.85	0.67	30.70	-	-	-	-	-	74.22
10%	Standard VSI	13.38	11.14	5.98	0.12	-	-	-	3.93	34.55
	VSI+Boost	11.30	8.43	5.99	0.09	26.74	15.07	9.10	4.32	81.04
	ZSI-V	47.33	58.46	18.57	0.41	-	-	-	6.32	131.09
	Standard CSI	34.63	0.60	19.79	-	-	-	-	-	55.02
	CSI+Buck	30.70	0.50	15.48	-	-	-	-	7.78	54.46
	ZSI-I	43.07	1.22	15.57	-	-	-	-	-	59.86
	CSI+SCaps	31.25	0.56	19.84	-	-	-	-	-	51.65
5%	Standard VSI	5.30	8.07	1.72	0.01	-	-	-	1.54	16.64
	VSI+Boost	4.18	5.90	1.67	0.01	15.88	11.70	4.40	1.60	45.34
	ZSI-V	25.01	30.35	5.22	0.24	-	-	-	1.54	62.36
	Standard CSI	16.26	0.45	7.80	-	-	-	-	-	24.51
	CSI+Buck	13.96	0.44	5.92	-	-	-	-	2.68	23
	ZSI-I	17.51	2.10	5.92	-	-	-	-	-	25.53
	CSI+SCaps	14.51	0.42	7.50	-	-	-	-	-	22.43

Table 6.15 Estimated semiconductor power losses for all the candidate topologies operating at MPP under 5%, 10%, 20%, 30%, 50% and 100% sun irradiance levels

Inverter Topology		Estimated Efficiency (%)						
		$\eta_{5\%}$	$\eta_{10\%}$	$\eta_{20\%}$	$\eta_{30\%}$	$\eta_{50\%}$	$\eta_{100\%}$	η_{euro}
VSI	Standard VSI	97.9	98.3	98.4	98.2	97.8	97.8	**98.0**
	VSI+Boost	94.4	96.0	96.5	96.7	97.1	97.1	**96.7**
	ZSI-V	92.3	93.6	93.6	94.5	95.9	95.9	**95.1**
CSI	Standard CSI	96.9	97.3	97.5	97.5	97.1	97.1	**97.2**
	CSI+Buck	97.1	97.3	97.8	97.8	97.4	97.4	**97.7**
	ZSI-I	96.8	97.0	97.2	97.2	94.6	94.6	**95.4**
	CSI+SCaps	97.2	97.4	97.7	97.7	97.4	97.4	**97.6**

Table 6.16 Estimated efficiencies ($\eta_{5\%}$, $\eta_{10\%}$, $\eta_{20\%}$, $\eta_{30\%}$, $\eta_{50\%}$ and $\eta_{100\%}$) at the MPP under 5%, 10%, 20%, 30%, 50% and 100% sun irradiance levels and the European efficiencies (η_{euro}) for all the candidate topologies

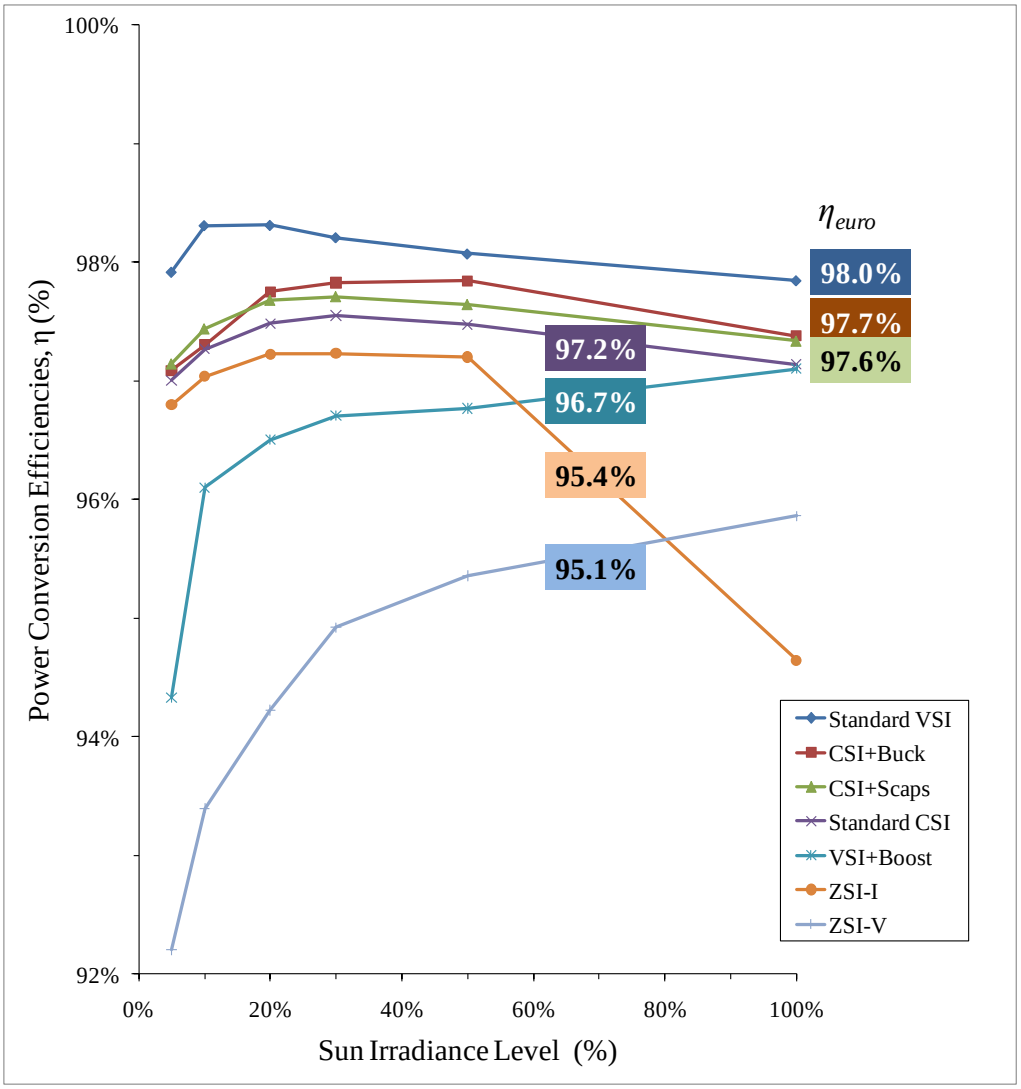


Figure 6.26 Efficiency curves and European efficiencies (η_{euro}) for all the candidate topologies

It can be seen from Table 6.16 and Figure 6.26 that:

- Most candidate inverter topologies provide high efficiency under the sun irradiance levels of between 20% and 50%, except the VSI+Boost and ZSI-V which provide a higher efficiency at higher sun irradiance levels (50% to 100%).

- The CSI+SCaps can operate with a higher efficiency than the standard CSI, VSI+Boost, ZSI-I and ZSI-V at all the operating points.

- The CSI+SCaps has a high European efficiency (97.6%) and is ranked 3rd out of the seven candidate topologies. The standard VSI (98.0%) and CSI+Buck (97.7%) are the 1st and 2nd of the ranking, following by the standard CSI (97.2%), VSI+Boost (96.7%), ZSI-I (95.4%) and ZSI-V (95.1%) for the 4th to 7th of the ranking respectively.

6.10 Overall Performance Evaluation

Performance evaluations of the CSI+SCaps in comparison to the other candidate topologies for the specific criteria have been presented in Sections 6.1-6.9. In this section the overall performance of all the candidate topologies when considering all of those criteria is presented.

Table 6.17 shows the list of the evaluation criteria, assessment parameters and numbers 1 to 7. The assessment parameters are used to justify the numbers whilst the numbers are used to score the performance for each evaluation criteria. The methods to justify the number are as follows:

- Firstly, the maximum and minimum values for a particular assessment parameter are selected from the information provided in Sections 6.1-6.9. For example, the values of the maximum PV voltage rating 1000V and 508V are selected from Figure 6.1 for the criteria of low internal power losses within a PV source.

- Secondly, the range between these maximum and minimum values is divided "equally" into seven sub-ranges. For example, (<1000V, <927, … , <562) as shown for the criteria of low internal power losses within a PV source.

- Finally, the numbers 1 to 7 are assigned for all the sub-ranges by using 7 for the best performance and 1 for the worst performance.

Evaluation Criteria	**Assessment Parameters**	**Score**							**Data Source**
		1	2	3	4	5	6	7	
Low internal power losses within a PV source	Max. PV voltage rating (Volts)	< 1000	< 927	< 854	< 781	< 708	< 635	< 562	Figure 6.1
High power transfer ratio	Min. operating modulation depth (no units)	> 0.60	> 0.66	> 0.77	> 0.78	> 0.84	>0.90	>0.96	Figure 6.2
Simple control and low control circuit power consumption	Min. number of active components (pieces)	> 23	> 21	> 19	> 17	> 15	> 13	> 11	Figure 6.3
Small size and light weight	Max. size of passive components (times of max. size)	< 1.03	< 0.88	< 0.73	< 0.58	< 0.43	< 0.28	< 0.13	Figure 6.5
Low input voltage ripple	Max. input voltage ripple (%)	< 0.15	< 0.13	< 0.11	< 0.09	< 0.07	< 0.05	< 0.03	Figure 6.9
Low input current ripple	Max. input current ripple (%)	< 17.5	< 14.9	< 12.3	< 9.7	< 7.1	< 4.5	< 1.9	Figure 6.10
Low output line current THD	Max. average line current THD (%)	< 14.8	< 12.9	< 11.0	< 9.1	< 7.2	< 5.3	< 3.4	Figure 6.14
Unity output power factor	Min. Power factor (no units)	> 0.79	> 0.82	> 0.85	> 0.88	> 0.91	> 0.94	> 0.97	Figure 6.15
Low voltage stress on power semiconductors	Max. peak DC-link voltage (Volts)	< 1210	< 1107	< 1004	< 901	< 798	< 695	< 592	Figure 6.19
Low current stress on power semiconductors	Maximum peak DC-link current (Amps)	< 60.0	< 55.2	< 50.4	< 45.6	< 40.8	< 36.0	< 31.2	Figure 6.20
Low estimated cost of power semiconductors	Max. specific installed power ($\Sigma P_{sw}/P_{in}$) (no units)	<16.8	< 15.5	< 14.2	< 12.9	< 11.6	< 10.3	< 9.0	Figure 6.21
Low semiconductor power losses	Max. total semiconductor power losses (Watts)	< 1280	< 1142	< 1004	< 866	< 728	< 590	< 452	Figure 6.25
High European efficiency	Max. η_{euro} (%)	< 95.2	< 95.7	< 96.2	< 96.7	< 97.2	< 97.7	< 98.2	Figure 6.26

Table 6.17 All evaluation criteria and their scores for the overall performance evaluation

Using the justification criteria and the information provided from the data sources listed in Table 6.17, the overall performance of the candidate topologies is given, as shown in Table 6.18.

Evaluation Criteria	**Inverter Topology**						
	VSI			**CSI**			
	Standard VSI	VSI+Boost	ZSI-V	Standard CSI	CSI+Buck	ZSI-I	**CSI+SCaps**
Low internal power losses within a PV source	1	4	4	7	5	5	7
High power transfer ratio	1	6	5	1	6	5	7
Simple control and low control circuit power consumption	2	1	2	7	4	6	7
Small size and light weight	4	3	1	6	6	7	6
Low input voltage and current ripple	7	2	3	1	6	4	3
Low output line current THD	1	2	4	5	5	7	7
Unity output power factor	7	7	7	7	7	7	1
Low voltage and current stress on power semiconductors	5	6	3	5	6	3	7
Low estimated cost of power semiconductors	5	6	1	5	6	1	7
Low semiconductor power losses	7	5	4	6	5	1	6
High European efficiency	7	4	1	5	6	4	6
Total Score	**47**	**46**	**35**	**55**	**62**	**50**	**64**

Table 6.18 Overall performance of the candidate topologies

It can be seen from Table 6.15 that the CSI+SCaps provides the best overall performance with the highest total score in this evaluation; followed by a CSI+Buck, a standard CSI, a ZSI-I, a standard VSI, a VSI+Boost and a ZSI-V. However, it should be noted that the ranking of the topologies can be different from this if only specific requirements are considered. For example, the CSI+SCaps may be less attractive if the criteria of the unity power factor are the critical requirements for a particular application.

6.11 Summary

In this chapter, the performance evaluation of the proposed transformerless, grid-tied PV inverter topology, called *the CSI with series AC capacitors* or (CSI+SCaps), in comparison with the six other candidate topologies has been presented. The six other topologies are a standard VSI, a standard CSI, a two-stage VSI+Boost, a two-stage CSI+Buck, a ZSI-V and a ZSI-I.

There are several evaluation criteria discussed. Those are the required PV ratings, operating modulation depths, required circuit components, input and output power quality, voltage and current stress on power semiconductors, estimated cost of power semiconductors, semiconductor power losses, European efficiencies and overall performance evaluation. The evaluation results are summarised as shown in the following points:

- The CSI+SCaps requires the same PV ratings as a standard CSI. The topology has the lowest PV voltage rating (potentially low internal losses within the PV module) but the highest current rating (potentially high conduction losses within its circuit) among all of the other candidate topologies.

- The CSI+SCaps can operate with the highest modulation depth ($m \approx 1$) for the whole voltage range of the PV source. This means that the CSI+SCaps provide a higher power transfer ratio with a more optimum voltage-current level between the input and output side of the converter topology.

- The CSI+SCaps requires the minimum number of active components (as does a standard CSI). As a result, the CSI+SCaps and a standard CSI can achieve the simplest control circuit and the lowest control circuit power consumption compared with the other candidate topologies.

- The CSI+SCaps has a large size of total passive components (ranked 4^{th} out of all the seven topologies). This is because of the use of the series AC capacitors in its circuit.

- The CSI+SCaps provides a relatively high input voltage ripple (ranked 5^{th} out of the seven topologies) whilst providing a medium input current ripple

(ranked 4th out of the seven topologies). However, the CSI+SCaps CSI gives a lower input voltage and current ripple when compared with a standard CSI (approximately 20%).

- The CSI+SCaps provides the best quality of output supply current with the lowest average THD. However, the topology provides low output power factor compared with all of the candidate topologies.

- The CSI+SCaps gives the lowest voltage stress on the power semiconductors but high current stress compared with all of the other candidate topologies.

- The CSI+SCaps can achieve the lowest estimated cost of power semiconductors compared with all of the candidate topologies.

- The CSI+SCaps has low total power losses and is ranked 2nd out of all the seven candidate topologies. However, the CSI+SCaps (and also the standard CSI) have relatively high conduction losses compared with all of the other candidate topologies, the ZSI topologies have the highest switching power losses and the VSI+Boost and the CSI+Buck have the highest total power losses caused by their additional semiconductors.

- The CSI+SCaps has high European efficiency (97.6%) and is ranked 3rd out of all the seven candidate topologies. The topology can operate with a higher efficiency for all the considered operating points when compared with the standard CSI, VSI+Boost, ZSI-V and ZSI-I.

The results of overall performance evaluation shows that The CSI+SCaps can achieve the best performance; followed by the CSI+Buck, standard CSI, ZSI-I, standard VSI, VSI+Boost and ZSI-V respectively. This is a result of the use of the series AC capacitors which leads the CSI+SCaps to be able to operate with high operating modulation depth, reduced switching voltage levels and better AC filtering created by the connection of the standard LC filter and the series AC capacitors.

Chapter 7

Design and Construction of Experimental Test-Rig

This chapter presents details of the design and construction of the experimental test-rig, which has been used to experimentally validate the performance of the proposed CSI with series AC capacitors (CSI+SCaps) topology in comparison to a standard CSI topology when using for grid-tied photovoltaic (PV) applications. The test results obtained from this experimental test-rig are presented in Chapter 8.

7.1 Overview of the Experimental Test-Rig

Figure 7.1 shows the block diagram of the experimental test-rig. The test-rig has four main elements:

- The PV emulator
- The prototype CSI+SCaps
- The interfacing and control circuits
- The three-phase power supply

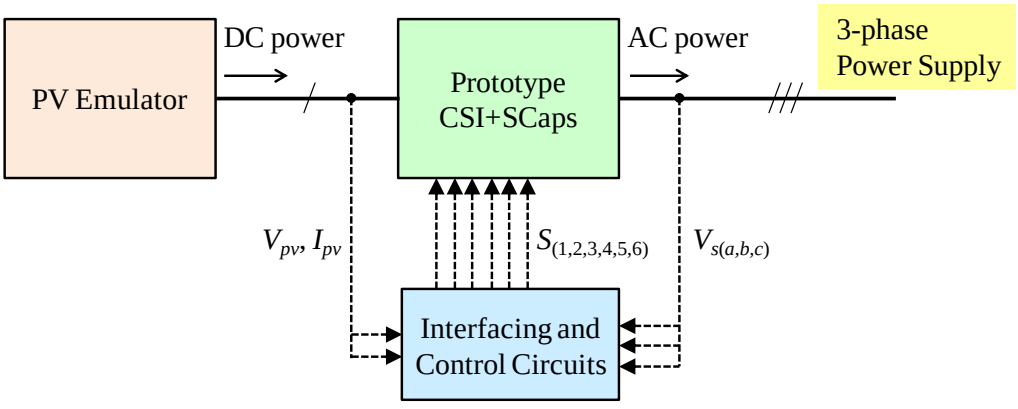


Figure 7.1 Block diagram of the experimental test-rig

The elements of the test-rig shown in Figure 7.1 have the following functions:

- The PV emulator is used as a PV source generating DC power to supply the prototype CSI+SCaps.
- The prototype CSI+SCaps converts the DC power from the PV emulator into AC power which is then connected to the three-phase power supply.
- The interfacing circuits measure voltages ($V_{s(a,b,c)}$, V_{pv}) and current (I_{pv}) from the main circuit. The control circuits utilise these measured parameters to generate the gate signals ($S_{(1,2,3,4,5,6)}$) to control the switches in the prototype CSI+SCaps to produce the desired AC output waveforms.

Figure 7.2 shows the overview hardware of the experimental test-rig. The computer is also a part of the control circuit used for editing, compiling and uploading control programs. Details of the design and construction for each element are presented in Sections 7.2-7.7.

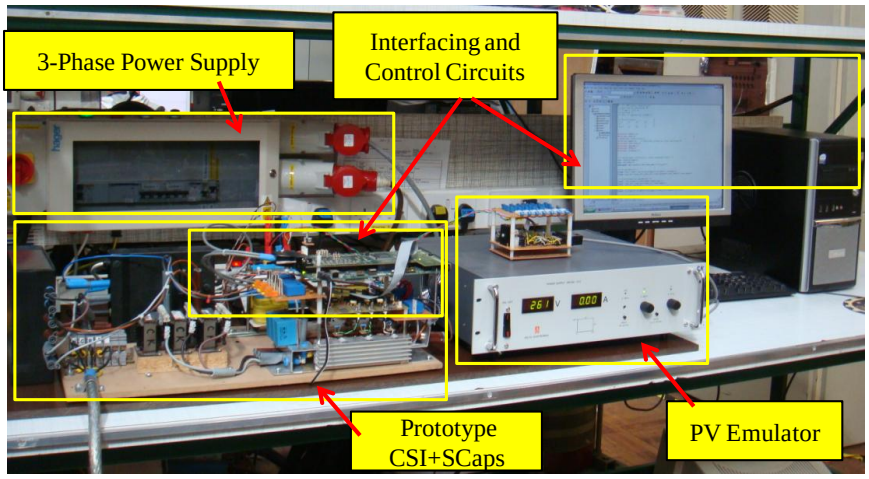


Figure 7.2 Photograph of the experimental test-rig

7.2 PV Emulator

A PV emulator is a power electronic device that can be programmed to emulate a PV panel by tracking a given voltage/current characteristic. The PV emulator is usually used in the experimental work because the device requires less operating space than the actual PV source as well as allowing the PV system to be analysed in a controlled environment [114-117]. The PV emulator used in these tests is designed to have

characteristics equivalent to a PV array built from the four strings of fourteen series-connected PV panels (model BP SX30 [54]), which has following specifications:

- Generate peak output power of 1.6 kW with the output voltage and current in the range of 0-295V and 0-7.8A and having typical PV specifications and characteristic curves as defined in Table 2.5 and Figures 2.16-2.17 (see Section 2.7.4). These specifications are selected to match to the capability of the components used in the emulator circuit.

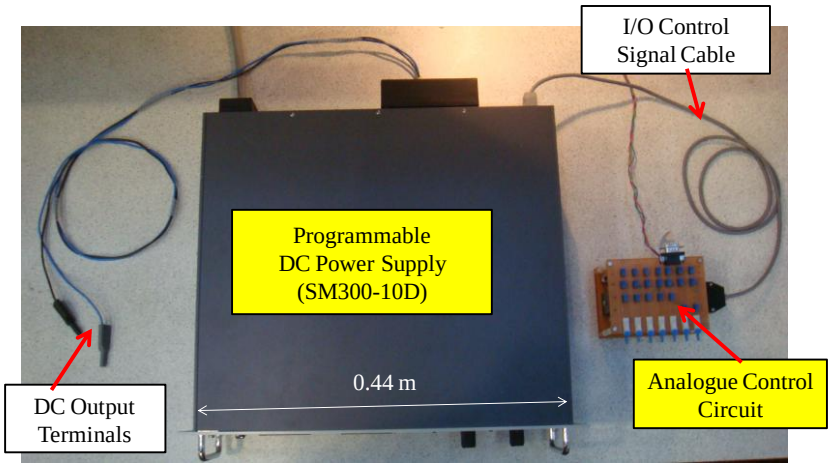
- Provide seven environmental test conditions: 5%, 10%, 20%, 30%, 50%, 70% and 100% sun irradiance. This selection allows the prototype CSI+SCaps to be evaluated in terms of European Efficiency (see definition in Section 3.3.1) [12].

7.2.1 Overview of Hardware

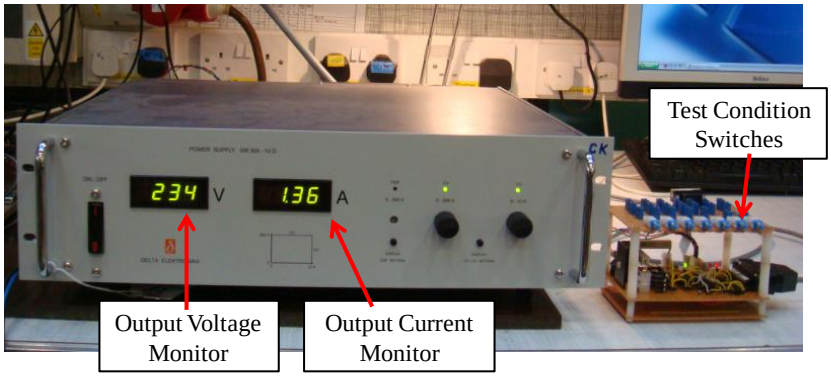
Figure 7.3 shows the overview of hardware configuration of the PV emulator used in this experimental work. The PV emulator consists of two elements: a programmable DC power supply (model SM300-10D [118]) and an analogue control circuit. These elements have the following features:

- The power supply SM300-10D is a general purpose programmable DC power supply. The power supply can be programmed to produce output voltage and current in the range of 0-300V and 0-10A using the analogue control signals of 0-5V. The power supply also gives output voltage and current monitoring signals (0-5V) which can be used for the analogue control circuit. A detailed specification of this power supply is given in [118].

- The analogue control circuit provides seven selectable switches for seven sun irradiance test conditions. When the test condition is selected, the circuit will issue two analogue control signals to program the power supply. The first signal is used to limit the maximum output current of the power supply for a particular selected test condition. The second signal is used to program the output voltage of the DC power supply for a particular output current (via a current monitoring signal) so that the PV emulator can produce output voltage and current as designed characteristic curves.



(a) Top view



(b) Front view

Figure 7.3 Hardware configuration of the PV emulator

Figure 7.4 shows an operational diagram for the PV emulator. The DC power supply measures and converts the output current (I_{pv}) of 0-7.8A to a current monitoring signal (I_{mon}) of 0-3.9V. When the test condition (SW_x) is selected, the analogue control circuit will issue the following signals to control the DC power supply:

- The control signal (I_{prog}) which is used to limit the maximum output current of the DC power supply. The value of I_{prog} is depended on the sun irradiance condition, which can be calculated from (7.1).

$$I_{prog} = (3.9) \cdot \frac{x}{100} \text{ V} \quad ; x = 5\%, 10\%, 20\%, 30\%, 50\%, 70\% \text{ and } 100\% \tag{7.1}$$

- The control signal (V_{prog}) which is used to program the output voltage of the DC power supply for a particular measured current (I_{mon}). The control voltage range of 0-4.9V is used for V_{prog} in order to produce an output voltage of 0-295V from the PV power supply.

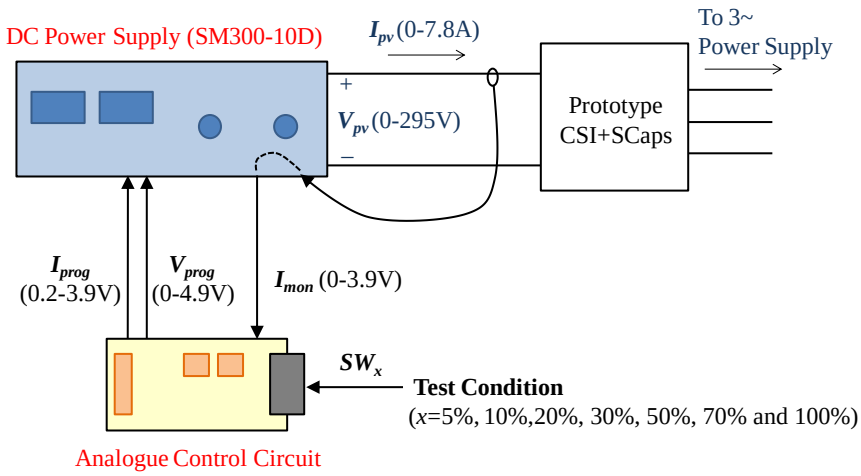


Figure 7.4 Operational diagram for the PV emulator

7.2.2 Analogue Control Circuit

This section presents more detail about the design and construction of the analogue control circuit. The analogue control circuit consists of a test condition selecting circuit, an I/O interfacing circuit and a PV equivalent circuit, as shown in Figure 7.5. These circuits have the following functionality:

- The test condition selecting circuit provides seven selectable switches for seven sun irradiance test conditions. When the test condition is selected, this circuit will connect the setting values of the potentiometers (R1, R2, R3 and R4) for a particular selected switch to the I/O interfacing circuit.
- The I/O interfacing circuit uses the values of R1, R2, R3 and R4 obtained from the test condition selecting board to adjust the gains of the buffers A1, A2 and A3 to provide suitable voltage levels for the input/output signals (I_{mon}, I_{prog} and V_{prog}) for a particular selected test condition. The control signal I_{prog} is directly generated from this circuit by adjusting the gain of the buffer A3.
- The PV equivalent circuit is a “small” PV source which provides similar output V-I characteristics as the actual PV source, but with a reduced output voltage (V_o) in the range of 0-4.95V, which is suitable to be used as a control signal V_{prog} to program the output voltage of the DC power supply. The output current monitoring signal (I_{mon}) is required for the circuit used to specify the location of the operating point on the designed PV characteristic curves.

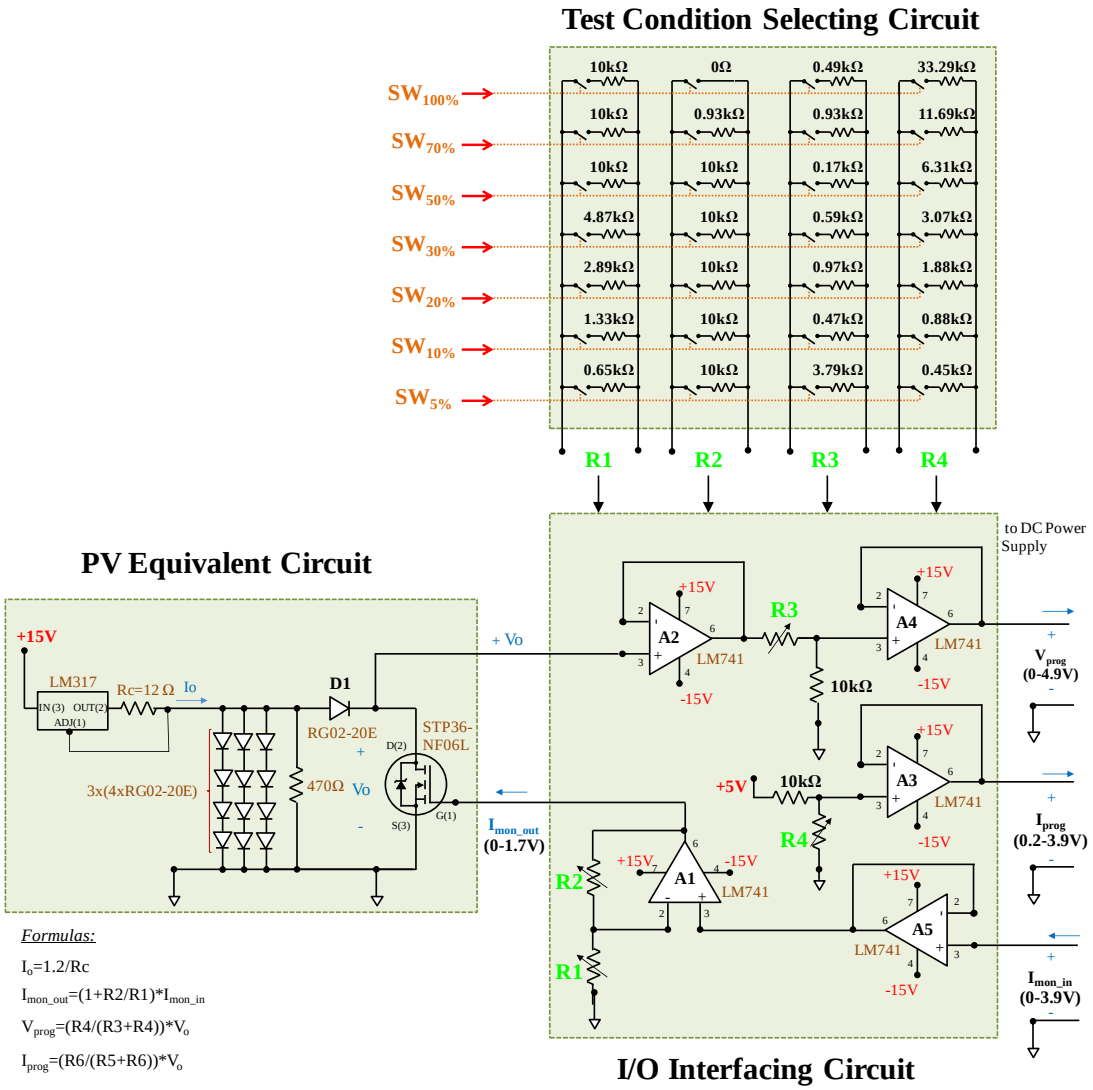


Figure 7.5 Circuit diagram of the analogue control circuit

7.2.2.1 Test Condition Selecting Circuit

The hardware used for the test condition selecting circuit is shown in Figure 7.6. The seven switches made from four pole single throw push-button switches are used to manually select the sun irradiance test conditions for the PV emulator. These switches allow four potentiometers to connect to the I/O interfacing circuit at the same time with a single press as well as releasing the previous active switch when pressed. Therefore, only one test condition can be selected at a time.

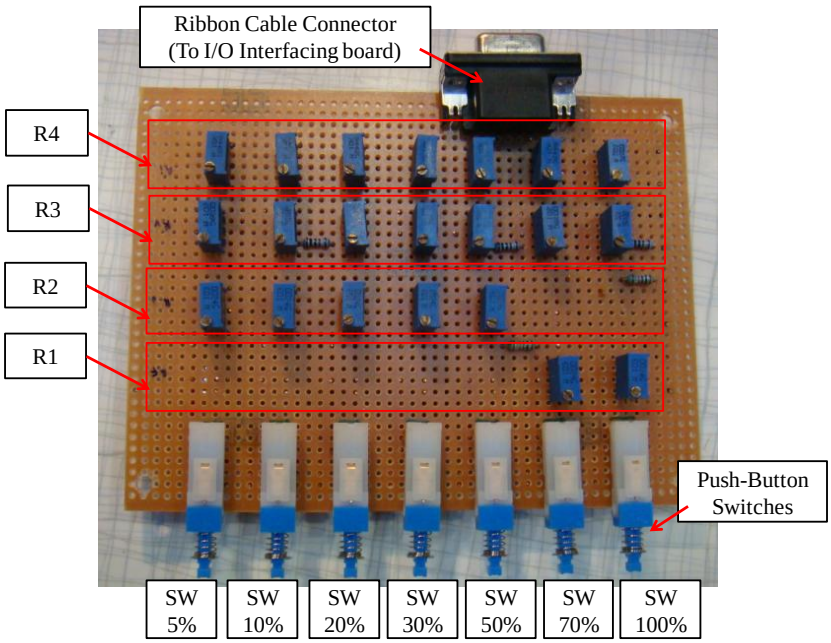


Figure 7.6 Hardware configuration used for the test condition selecting circuit

7.2.2.2 I/O Interfacing and PV Equivalent Circuits

Figure 7.7 shows the hardware of the I/O interfacing circuit and the PV equivalent circuit. These two circuits built in the same board.

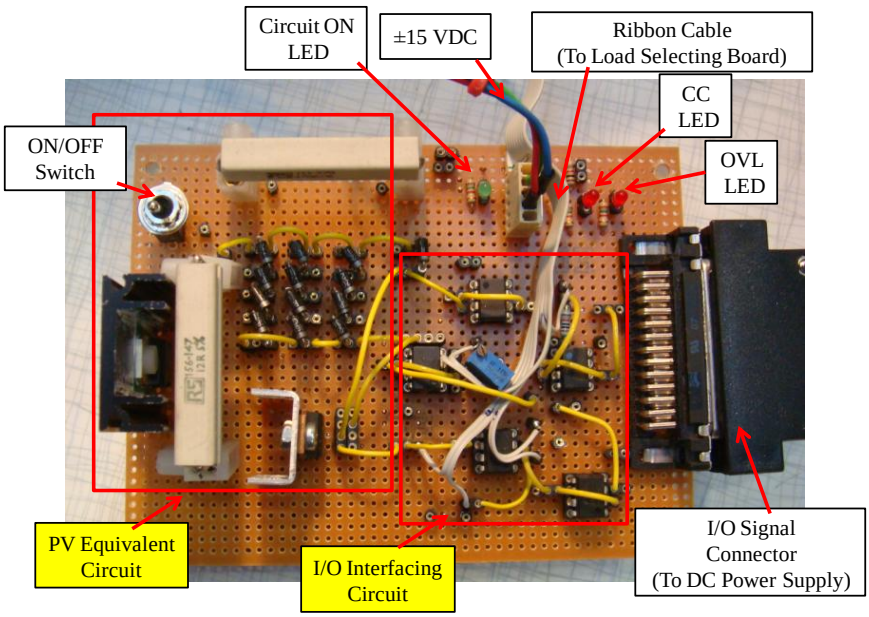


Figure 7.7 Hardware configuration used for the I/O interfacing circuit and the PV equivalent circuit

From Figure 7.7, the I/O interfacing circuit is built from five operational amplifiers A1 to A5 (op-amp LM741CN). These components have the following functionality:

- The non-inverting amplifier (A1) made from an op-amp LM741CN with two potentiometers R1 and R2 is used to fine tune the voltage level of I_{mon} in order to match to the operation voltage range of the MOSFET.
- The voltage attenuator A2 (an op-amp LM741CN with a potentiometer R3) is used as an output buffer as well as fine tuning the voltage level of V_{prog}.
- The voltage attenuator A3 (an op-amp LM741CN with a potentiometer R4) is used to generate I_{prog}, which then is used to program the output current of the DC power supply.
- The Op-amps A4 and A5 are used to be a buffer for V_{prog} and I_{mon} respectively.

From Figure 7.7, the PV equivalent circuit consists of a current source, a large scale diode, a resistor, a reverse current blocking diode (D_1) and a power MOSFET. This circuit is an equivalent circuit of the designed PV array but is 78 times smaller in size in order to allow the circuit to operate up to 5V (control voltage range). These components have the following functionality:

- The current source is made from a voltage regulator (LM317) and a series resistor (12Ω) generate a constant current (I_o) of 100mA [119].
- The three strings of four series connected diodes (RG02-20E) effectively form a large scale diode. The connection of four series diodes (typically V_F=1.65 V) produces a total voltage during open circuit of 6.8 V, but the net output voltage after compensating the voltage drops across the series diode D_1 is 4.95 V. This voltage level is suitable for producing V_{prog} to program the DC power supply. The three strings are used to reduce the diode current on each string which helps to reduce voltage variation due to thermal drift.
- The parallel resistor (R_p) and series resistor (R_s) of the original PV equivalent circuit (Table 2.4) are reduced to 470Ω and 0.15Ω respectively. However, since the value of R_s is small, this can be neglected.

- The power diode D_1 (RG02-20E) is used to block the reverse current.
- The MOSFET (type ST36NF06L) interfaces the actual output current of the DC power supply (0-10A) to the PV equivalent circuit current (0-100 mA). In this sense the MOSFET functions as a voltage controlled current sink, which receives the input control voltage of 0-5V (I_{mon}) from the DC power supply and varies the output current of 0-100mA on the output side for the PV equivalent circuit. The output current of the PV equivalent circuit decreases as I_{mon} decreases and becomes zero when the MOSFET is completely turned off (I_{mon}=0V). The high current rating of the MOSFET (30A) is used in order to give stable operation regardless of any temperature variation.

Figure 7.8 shows the complete hardware of the analogue control circuit with the cover box. The experimental results obtained from the PV emulator in comparison to the design specifications are discussed in Section 8.1.

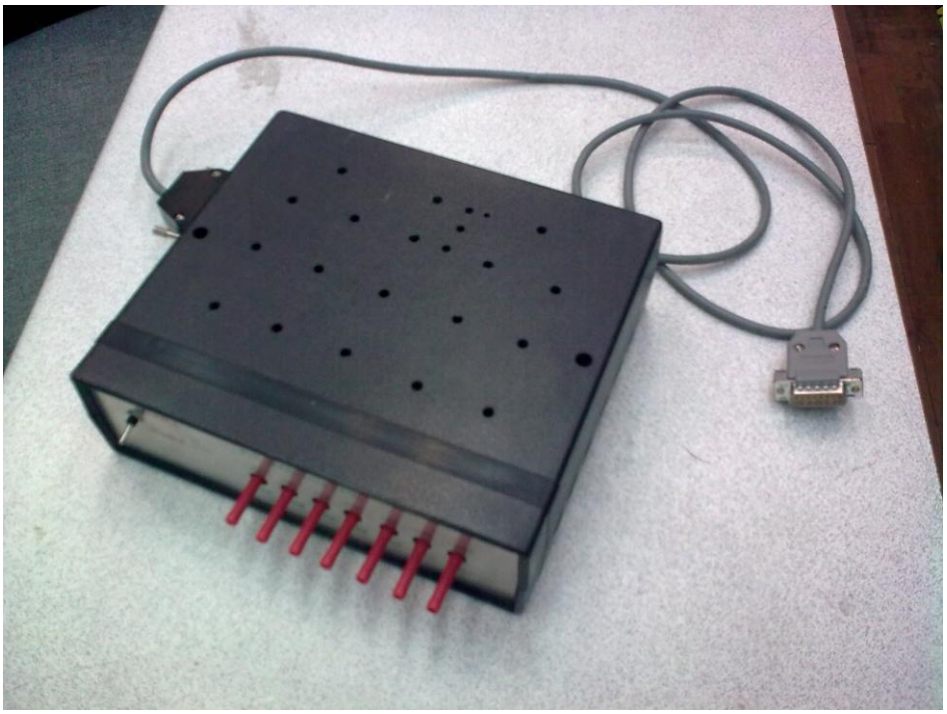


Figure 7.8 Complete hardware for the analogue control circuit

7.3 Prototype CSI+SCaps

Figure 7.9 shows a photograph of the hardware for the prototype CSI+SCaps. The hardware consists of the following components:

- The CSI power module
- The filtering components
- The series AC capacitors

Details of these components are presented in Sections 7.3.2-7.3.4.

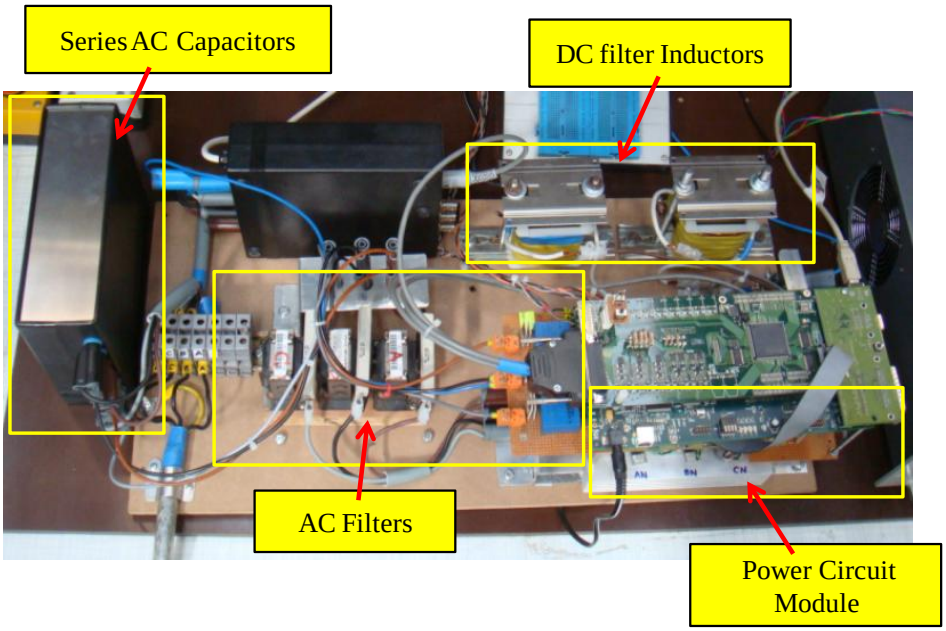


Figure 7.9 Photograph of the prototype CSI+SCaps

7.3.2 CSI Power Module

Figure 7.10 shows a photograph of hardware of the CSI power module. The module includes all relevant components used in the power conversion stage as listed below:

- The semiconductor devices (IGBTs)
- The power bus bars
- The heatsink

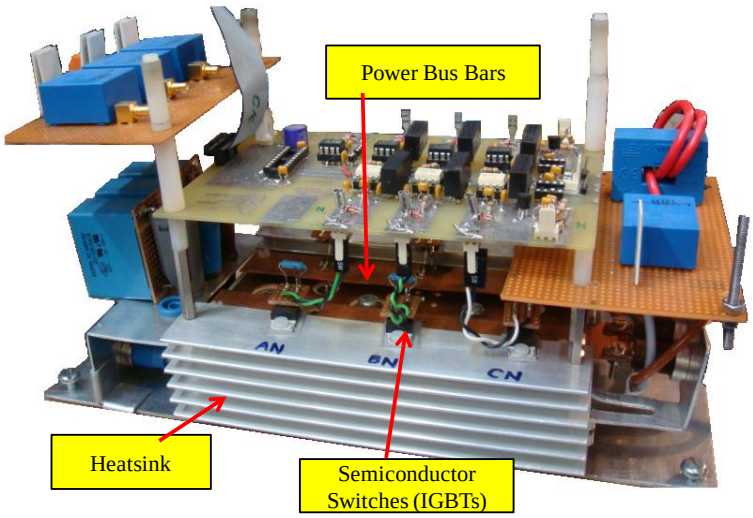
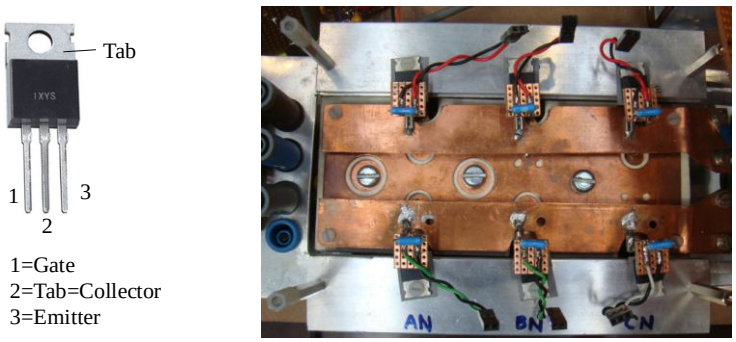


Figure 7.10 Photograph of the CSI power module

7.3.2.1 The Selection of Semiconductor Devices

Normally, the discrete switches made from a IGBT connected in series with a power diode are used in a standard CSI and a CSI with series AC capacitors [73],[120]. Alternatively, devices such as *Reverse-Blocking IGBTs* (RB-IGBTs) could be used. These devices include the series connected diode function and would provide a simpler and smaller CSI power circuit. RB-IGBTs also provide lower power semiconductor losses compared to standard IGBTs as well as the possibility of being more cost effective with mixed devices configurations [34]. Figure 7.11 shows photographs of the RB-IGBTs (model IXRA15N120) and the mounting layout of the devices on the converter prototype. The specifications of the devices are presented in Table 7.2



(a) (b)

Figure 7.11 Photographs of (a) the RB-IGBT model IXRA15N120 and (b) the mounting layout of the RB-IGBTs

Symbol	Description	Specification	Conditions
V_{CE}	Collector-emitter voltage	±1200 V	max, @25-125°C
I_C	Collector current	25 A 15 A	max, @ 25°C max, @125°C
V_{GE}	Gate-emitter voltage	±20 V	max, continuous
$V_{CE(sat)}$	Collector-emitter saturated voltage (when the device is gated-on)	2.5 V / 2.95 V 3.3 V	typ/max, @25 °C typ, @125°C I_C =10A; V_{GE} =15V
$t_{d(on)}$ t_r $t_{d(off)}$ t_f E_{on} E_{off} $E_{rec\ int}$	Internal diode turn-on time Rise time Internal diode turn-off time Fall time Turn-on energy Turn-off energy Initial Reverse recovery energy	17.5 ns 16 ns 212 ns 41 ns 3 mJ 0.1 mJ 0.65 mJ	typ. ; Inductive load; @125°C; V_{CE} =600V; I_C =10A; V_{GE} =±15V; R_G=47Ω
t_{rr}	Reverse recovery time	300 ns	Typ, @125°C; V_{CE} =-600V; I_F=10A; V_{GE} =±15V; dI_c/dt=-800A/μs
R_{thJC} R_{thJC}	Thermal resistance (junction to case) Thermal resistance (junction to heatsink)	0.65 °C/W 0.25 °C/W	typ. typ, with heatsink

Table 7.1 Technical specifications of the RB-IGBT model IXRA15N120

7.3.2.2 The Design of Power Bus Bar Module

Loop inductance which appears between the bus bars and in the power device package can cause high-dynamic overvoltage during fast commutations ($V=L\mathrm{d}i/\mathrm{d}t$). Therefore, the distributed inductance throughout the inverter and its components should be minimised[121, 122]. This section considers the inductance contributed from the bus bars.

In this prototype, low inductance bus bars using planar plate configurations are used [123, 124]. The total bus bar stray inductance between two parallel conducting planar plates that are separated by a dielectric material with relative permeability (μ_r) can be approximated using (7.2) and the estimated overvoltage spike using (7.3); where L_t is the total bus bar inductance, L_i is the internal inductance caused by the skin effect and the proximity effects; L_e is the external inductance depended on the geometry of the two conducting planar plates; μ_o is the permeability of free space = $4\pi\times10^{-7}$ NA^{-2}; *w*, *l*, *t* are the width, length and thickness of a conducting plate respectively; I_{max} is the maximum possible conducting current.

$$L_t \approx L_i + L_e = \frac{\mu_o \mu_r}{8\pi} \cdot l + 2\mu_o \mu_r \frac{t \cdot l}{\pi(t+w)} \tag{7.2}$$

$$V_{over} \approx L_t \cdot \frac{I_{max}}{min\{t_r, t_f\}_{IGBT,datasheet}} \tag{7.3}$$

In order to reduce electromagnetic interference (EMI), EMI suppression capacitors (C_{EMI}) are used [125]. These capacitors should be large enough to provide a higher self-resonance frequency f_o (given by the datasheets) than the bus bar resonance frequency (f_r) caused by the bus bar inductance (L_t), as expressed in (7.4). The inductance (L_c) of the EMI capacitor can be estimated using (7.5).

$$C_{EMI} = \frac{1}{(2\pi f_r)^2 L_t} \qquad ; f_r < f_{o\{datasheet\}} \tag{7.4}$$

$$L_c = \frac{1}{(2\pi f_o)^2 C_{EMI}} \tag{7.5}$$

With the available information and using (7.4), 0.47μF EMI capacitors (PHE 844R) were selected. From the datasheet, these capacitors have a self-resonance frequency f_o of 1.5MHz, which is greater than the calculated bus bar resonance frequency f_r (1.32MHz). Using (7.5), the inductance of the EMI capacitors can be calculated, as 23.95nH.

Figure 7.12 shows the geometrical structure of the 3-phase AC planar bus bar module used in this prototype. The bus bars are made from the copper plates; having the width, length and thickness (*w*, *l*, *t*) of 60×150×2 mm (see the drawings in **Appendix B**). The thin layer dielectric sheets (Nomex type410) with the thickness of 0.25mm and μ_r of 2.7 are used to separate the copper plates. The EMI suppression capacitors of 0.47μF are mounted between the power bus bars. The DC-link bus bars are also made from the copper plates and are located above the AC bus bars as shown in Figure 7.12.

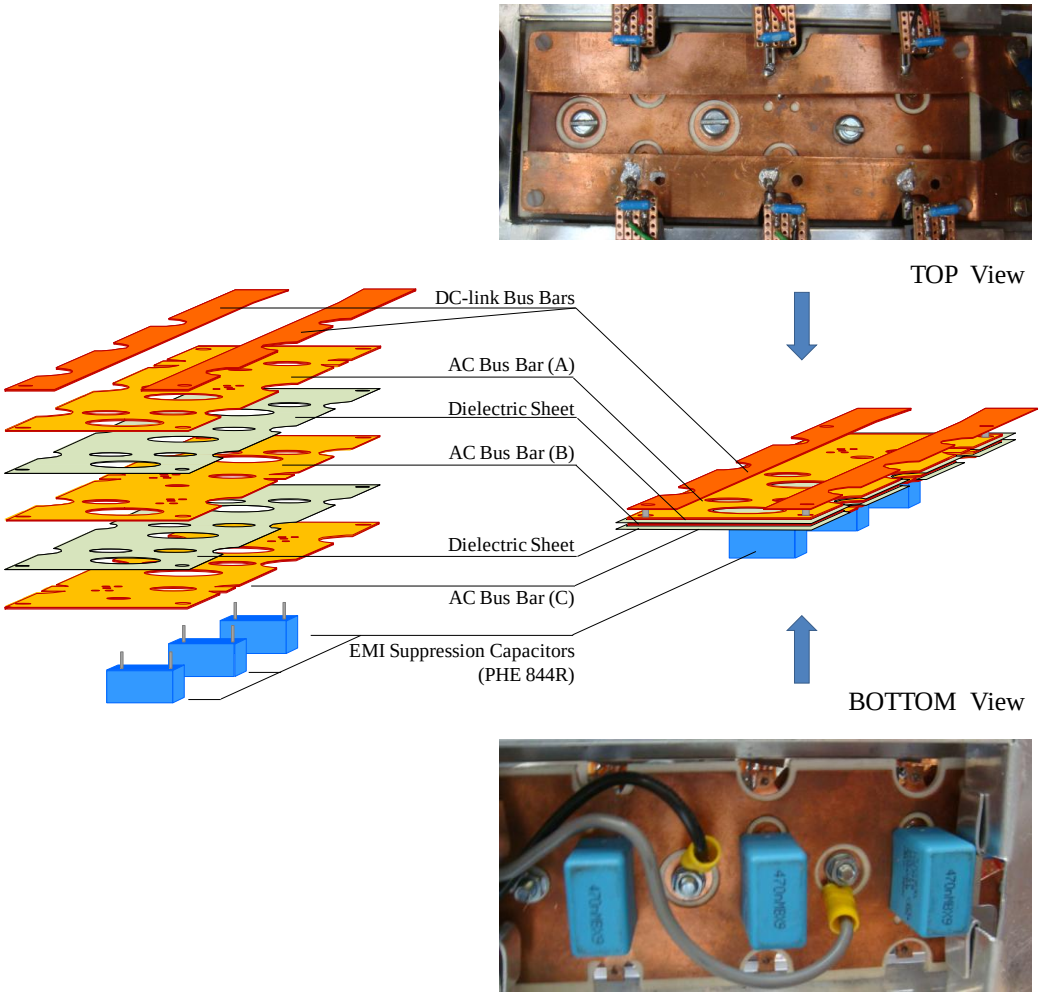


Figure 7.12 Geometrical structure of the Power Bus Bars of the prototype CSI+SCaps

7.3.2.3 The Design of Heatsink

In this prototype, a natural air cooling heatsink is used to dissipate the power losses (heat) from the RB-IGBTs. The term *thermal resistance* R_{th} (^{o}C/W) is usually referred to in the design of heatsink [126], [127]. R_{th} is the ratio of the temperature difference across the system (ΔT) to the dissipated power (P_D) as defined by (7.6). The heatsink must have the thermal resistance less than a specified value.

$$R_{th} = \frac{\Delta T}{P_D} \tag{7.6}$$

Figure 7.13 shows a simple structure of the CSI power circuit module and relevant parameters where the power module operates with the PV output power of 3kW and dissipates power losses of 47.09W (estimated using the method presented in Section

6.8). When the ambient temperature of 40°C and the maximum temperature of the heatsink less than 70°C are chosen (to ensure proper functionality of power circuit components which may malfunction at very high temperature), the thermal resistance of the heatsink calculated using (7.6) should be lower than 0.64 °C/W.

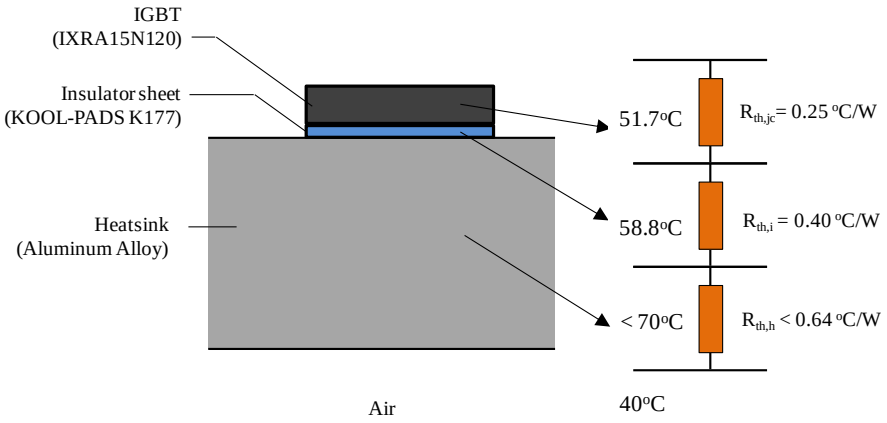


Figure 7.13 Structure of the CSI power module and all relevant parameters when the converter prototype operates at PV output of 3 kW

An Aluminium Alloy heatsink with a standard extruding configuration (Figure 7.14) was used in this prototype. The heatsink was split into two sheets with the AC bus bars placed between them. This structure provides a large air gap area, which allows a larger area for the cooling air to circulate around the power circuit module.

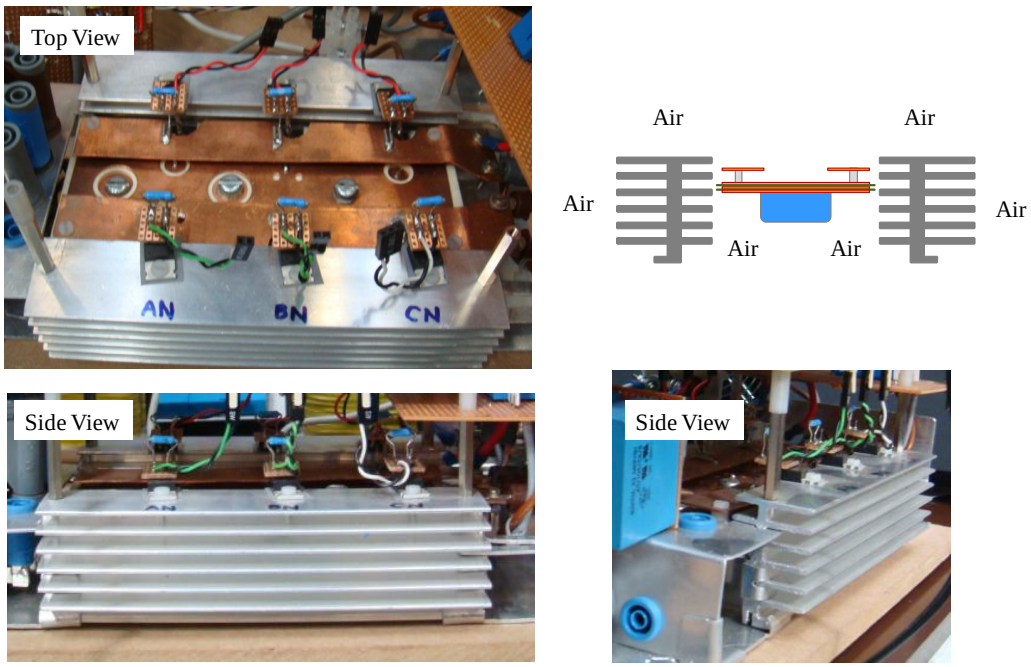


Figure 7.14 Photographs of the designed heatsink

7.3.3 Filtering Components

7.3.3.1 The DC-link Inductor

The DC-link inductor is designed to provide current ripple lower than 10% peak-to-peak at rated MPP. Using (4.16) presented in Section 4.5.1.1, the calculated value of the DC-link inductor is 11.3mH. Two inductors with a value of 6.5mH and designed by Dr. Junaidi [128] were used in this prototype, which provides the total inductance of 13mH. Photographs of the DC-link capacitors are shown in Figure 7.15.

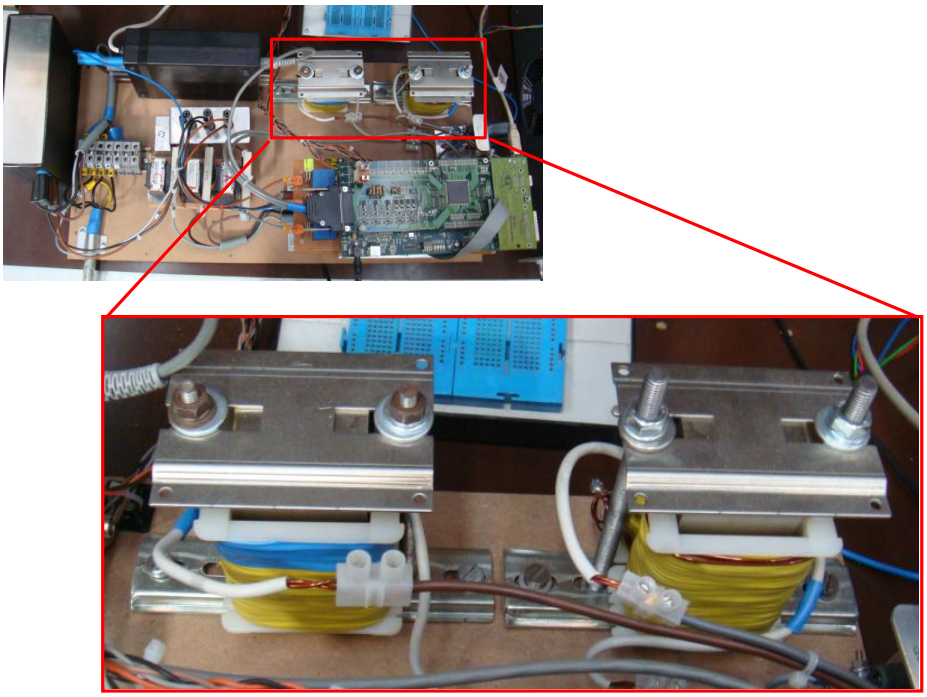


Figure 7.15 Photographs of the DC-link inductors

7.3.3.2 The AC Filters

The AC filter capacitors (C_f) are designed to ensure that the converter achieves a power factor higher than 0.99 at rated maximum power. Using (4.18) presented in Section 4.5.1.2, the required value of C_f can be determined. With the designed cut-off frequency of 1.7 kHz and using (4.19) and (4.20), the required values of the AC filter inductors (L_f) and the damping resistor (R_{damp}) can also be determined:

$$C_{f(\max)} < \frac{(1.67kW)\tan(\cos^{-1}(0.99))}{6\pi\times50\times(230)^2} = 4.8\mu F$$

$$L_f = \frac{1}{4\times(4.7\mu F)\times\pi^2\times(1.7kHz)^2} = 1.9mH$$

$$R_{damp} > 2\pi \times 50 \times 1.9mH = 0.59\Omega$$

In this prototype, polypropylene film capacitors model PH450 ($250V_{AC}$) of 4.7µF, AC filter inductors of 1.92mH and damping resistors of 47Ω were selected. The photographs of the AC filter components are shown in Figure 7.16.

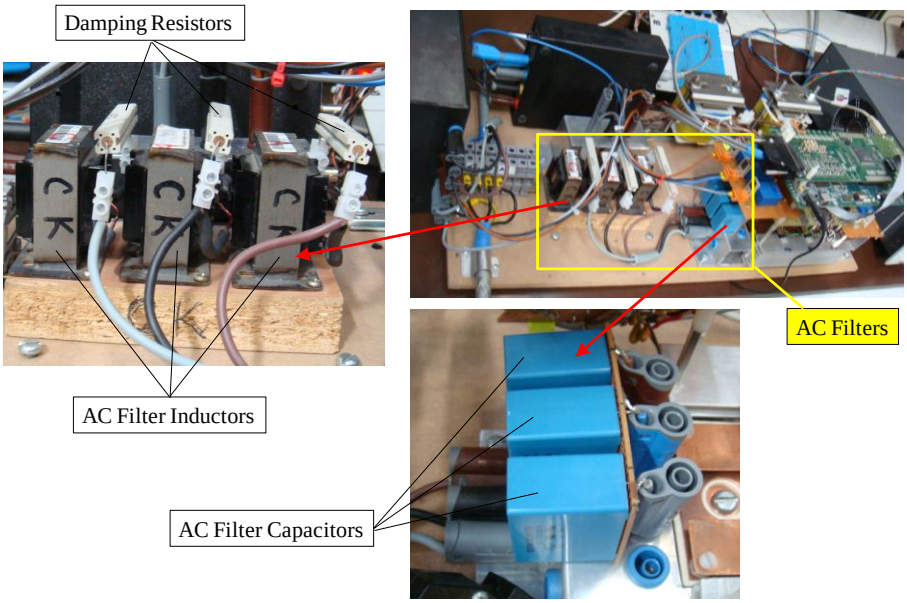


Figure 7.16 Photographs of the AC filter components

7.3.4 Series AC Capacitors

Using (5.14) presented in Section 5.3, the required value of series AC capacitors can be determined:

$$C_s > \frac{2(1.6kW)}{(2\times(2\cdot50)^2\times1.9mH\times1.6kW) + 3\times(2\pi)\times0.8\left(\sqrt{1-0.8^2}\right)} = 160.25\mu F$$

In order to minimise the construction cost of the experimental test-rig, the AC motor capacitors of 33µF with an over voltage rating of $640V_N$ (available in the lab) were adapted to be used. Five capacitors are connected in parallel that provide total capacitance of 165µF/phase as shown in Figure 7.17. Since the voltage rating of the

capacitors is 4.5 times larger than the AC voltage rating, a very large capacitor volume of 19×29×18 (W×L×H in cm) = 9918 cm^3 resulted. In practice, much smaller capacitors can be used, e.g. general purpose AC capacitors model GP84-416.84 with the capacitance of 175μF/phase at $250V_N$ [129] can have a total volume of 3×6.5×6.5×15 (W×L×H in cm) = 634 cm^3, which is 15 times smaller than the ones used in this prototype.

Figure 7.17 Photographs of the series AC capacitors

7.4 Interfacing Circuits

7.4.1 Gate Drive Circuit

In this experiment a gate drive circuit designed by Dr. Klumpner and Dr. Junaidi [101] was used with some modifications. Figure 7.18 shows a circuit diagram of the gate drive circuit for each IGBT. An optocoupler (HCPL3120) is used to individually receive a control input PWM signal from the FPGA (0V for gated-off and +3.5V for gated-on), which then produces an output control signal to drive the IGBT (-15V for gated-off and +15V for gated-on). The optocoupler also provides the galvanic isolation between the input and the output signals. A 15Ω gate resistor is used to limit gate circuit resonances and control the flow of gate current into the device.

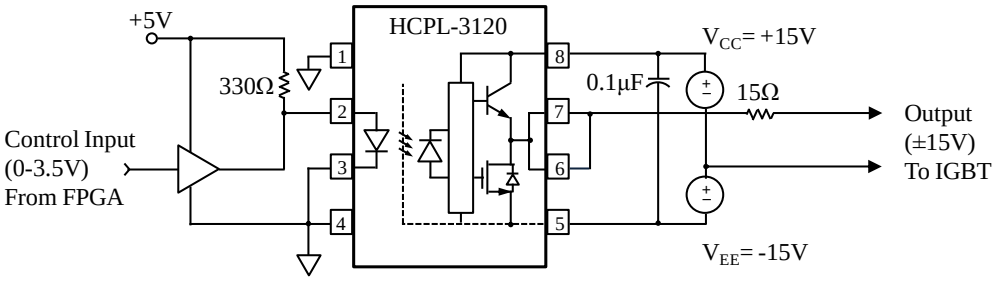


Figure 7.18 Circuit diagram of the gate drive circuit for each single IGBT

Figure 7.19 shows the complete gate drive circuit board connected to the IGBTs on the power module. This board was actually designed to drive eight IGBTs with auto-inverted output signals between IGBT pairs (e.g. +15V output for S_{ap} will automatically give -15V output for S_{an}). However in this prototype, only six gate drivers are used since there are only six RB-IGBTs used in the power module. Each driver on this board is also modified to be controlled independently in order to facilitate the implementation of the overlap-time for the CSI modulation in the FPGA (see Section 7.5.2). The gate driver board is supplied by a single +5V source, which will be shared and converted into ±15V for the optocouplers using miniature DC/DC converters (NMA0515SC). Zener diodes [BZX79-C18] are used to avoid IGBT destruction by gate-emitter over voltage.

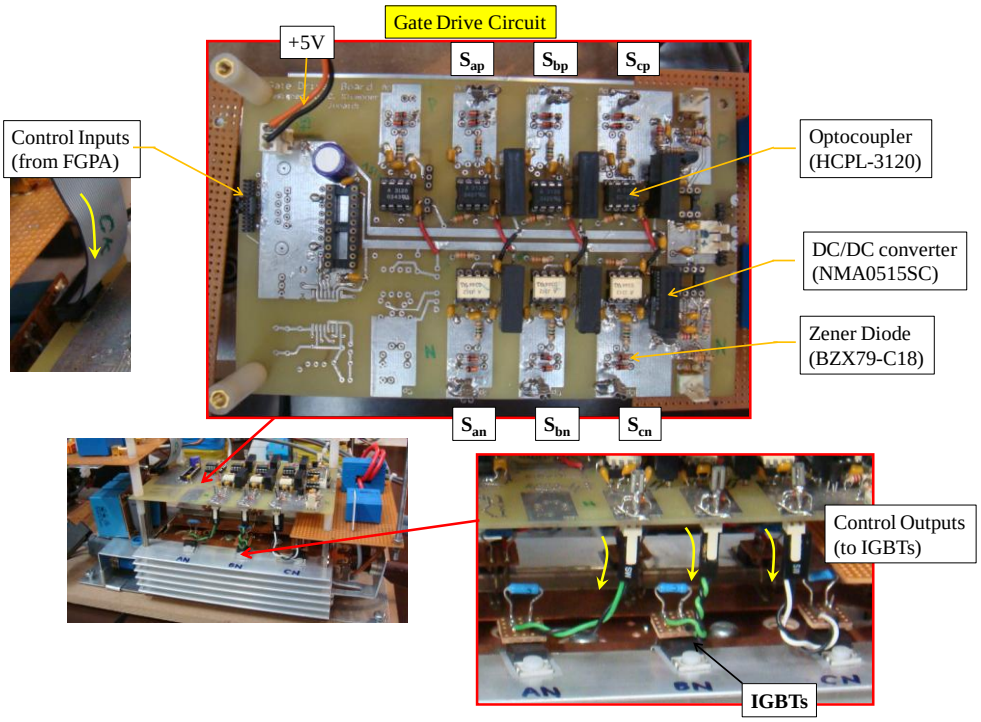


Figure 7.19 Photographs of the gate driver circuit board

7.4.2 Measurement Circuits

7.4.2.1 AC Voltage Measurement Circuits

There are two types of AC voltage measurement circuits used in this converter. Each circuit is comprised of three voltage transducers, which are used to measure the 3-phase voltages. The first circuit is constructed based on the technology of voltage dividers with electrical isolation (designed by Dr. Klumpner [101]). The circuit is used to measure and convert phase to neutral grid voltages (< $\pm 350V_{peak}$) into a level of ±5V suitable for the controller (FPGA) to process. The second circuit is constructed using the commercial transducers (LEM LV25-P) and is used to measure the voltage at the AC side of the CSI PWM bridge circuit and is designed to have the similar measuring capability to the first circuit. The detailed design for the first voltage measurement circuit can be seen in [101]. The second circuit is explained in this section.

Figure 7.20 shows the circuit diagram of the AC voltage measurement circuit using the transducers (LEM LV25-P). An input 50kΩ resistor (5W) produces 7mA maximum primary current for the AC input voltage of $\pm 350V_{peak}$. With the conversion ratio of the transducers of 1:2.5, the maximum current at the secondary side will be 17.5mA. Using a 200Ω resistor at the secondary side, the output voltage within the range of ±3.5V will be produced. Figure 7.21 shows the photographs of the voltage measurement circuits: one is placed close to the AC grid and the other to the inverter main body. It is noted that the 200Ω resistors are not shown in the picture, since these resistors are placed on the FPGA board.

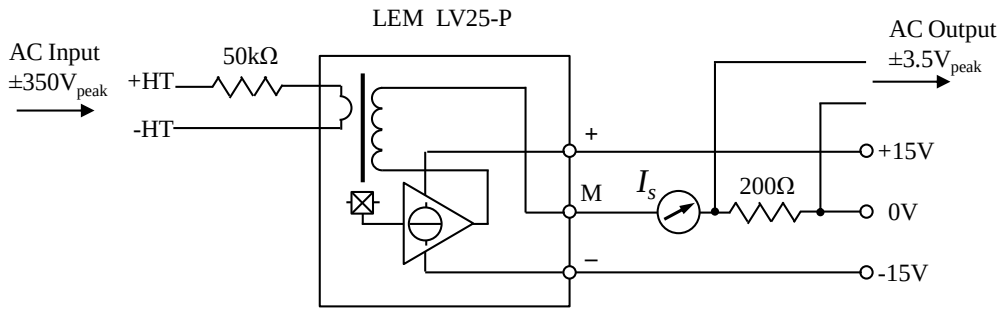


Figure 7.20 Circuit diagram of the AC voltage measurement circuit using LEM LV25-P voltage transducers

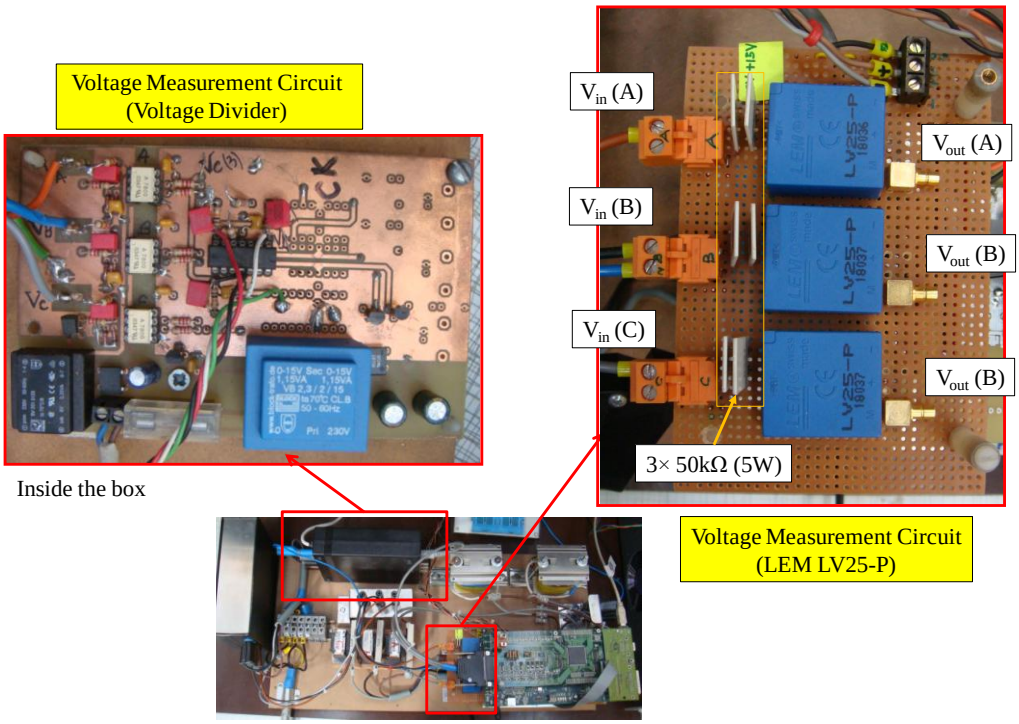


Figure 7.21 Photographs of the AC voltage measurement circuits: using voltage divider technology and using commercial LEM LV25-P voltage transducers

7.4.2.2 DC Voltage and Current Measurement Circuit

The DC voltage and current measurement circuits are used to measure the output voltage and current of the PV emulator. These measured voltage and current are used by the controller for the DC-link current control.

The LEM LV25-P transducer is used for the DC voltage measurement circuit. Hence, a similar design method presented in Section 7.4.2.1 can be used. With the maximum DC-link voltage value of $500V_{peak}$ and the use of a 50kΩ resistor at the primary side results in a 10mA current drawn in the primary side. With the conversion ratio of 1:2.5 of the transducer, a 25mA current will be drawn in the secondary side, which is then converted to voltage with the range of ±4.675V by a 187Ω resistor.

For the DC current measurement circuit, a current transducer LEM LA55-P is used to measure the maximum DC current of $\pm 15A_{peak}$. In order to maximise the measuring resolution to be close to the transducer's full rating (55A), three primary turns are used on this transducer, which will produce the total primary current of $\pm 45A_{peak}$ as

shown in Figure 7.22. With the transducer conversion ratio of 1:1000, the ±45mA$_{peak}$ current will be drawn at the secondary side. With the use of 100Ω resistor an output voltage in the range of ±4.5V is achieved. Figure 7.23 shows a photograph of the DC voltage and current measurement circuit. The circuit is placed on the DC side of the prototype CSI+SCaps.

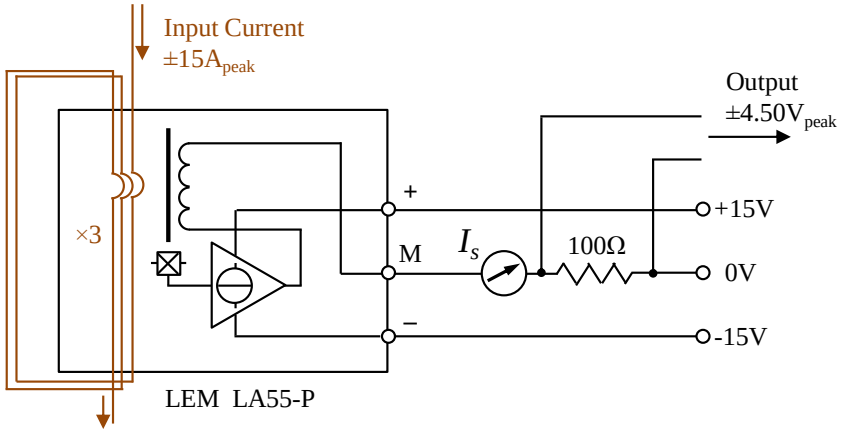
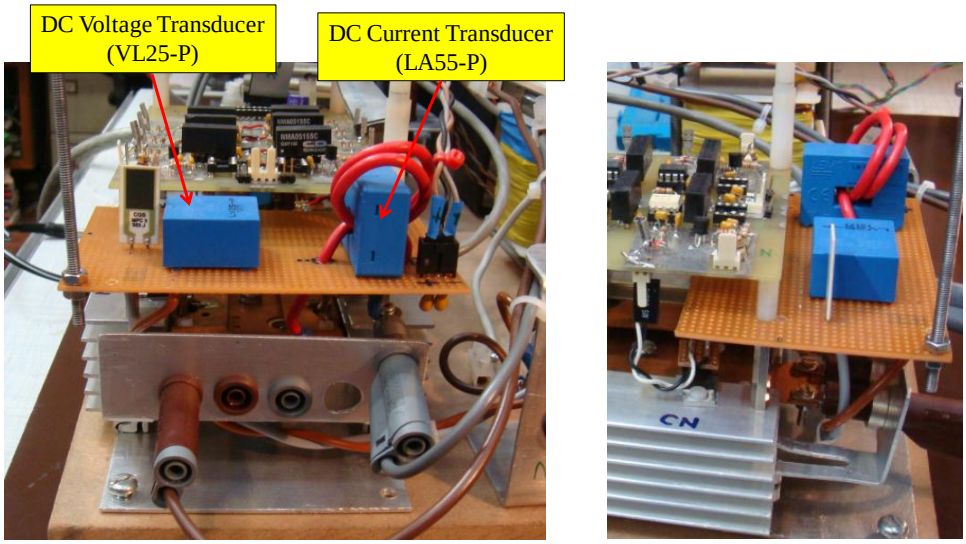


Figure 7.22 Circuit diagram of the DC current measurement circuit



(a) Front side (b) Left side

Figure 7.23 Photographs of the DC voltage and current measurement circuit

7.5 Control Circuits

7.5.1 Overview of the Control Platform

Figure 7.24 shows a diagram of the control platform for the prototype CSI+SCaps. The core controller consists of a Digital Signal Processor (DSP) and a Field Programmable Gate Array (FPGA). The DSP is used as a central processing unit that performs the functions associated with mathematical calculations and processing control commands. The FPGA is used as an interfacing unit that converts the analogue signals from the voltage/current measurement circuits into digital signals suitable for the DSP. The FPGA also sends the control pulses out to the gate drive circuit as the commands of the DSP as well as providing safe operation for the prototype using programmable overvoltage/current protection. The computer is used as a programming workspace for editing, debugging and uploading the programs for both the DSP and FPGA as well as being a host interface for the prototype via a Host Port Interface (HPI) daughter card.

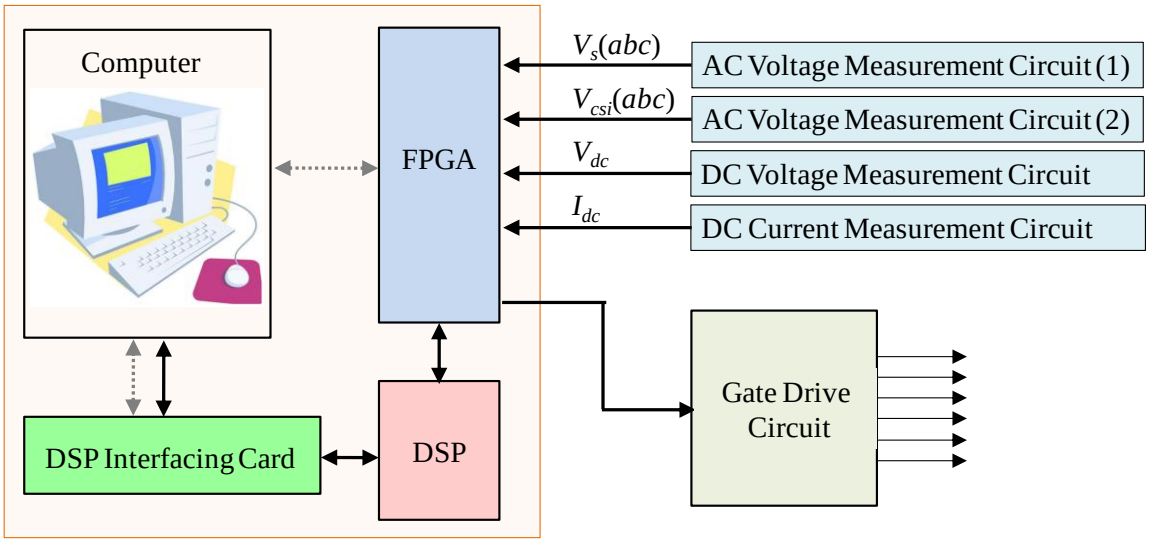


Figure 7.24 Overview of the control platform of the prototype CSI+SCaps

7.5.2 DSP Board

In this prototype, the DSP board module TMS320C61713 [130] is used. Figure 7.25 shows a photograph of this board. The control methodologies of a standard CSI and the CSI+SCaps presented in Section 4.4.2 and Section 5.5.2, are interpreted and implemented on the DSP using the C language codes through the use of CCstudio 3.1 code composer.

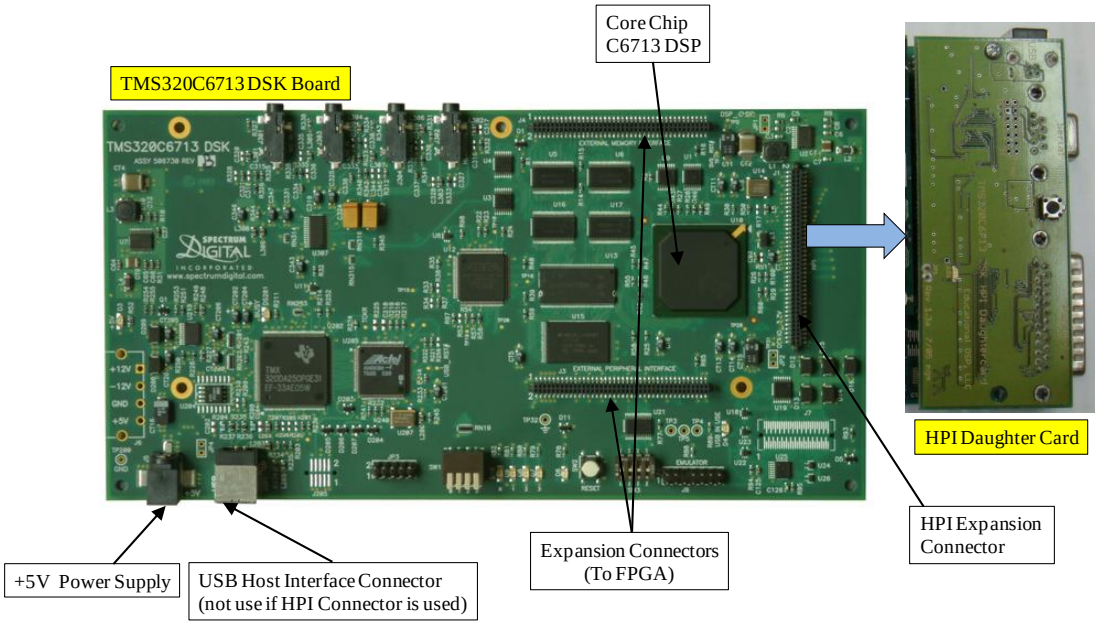
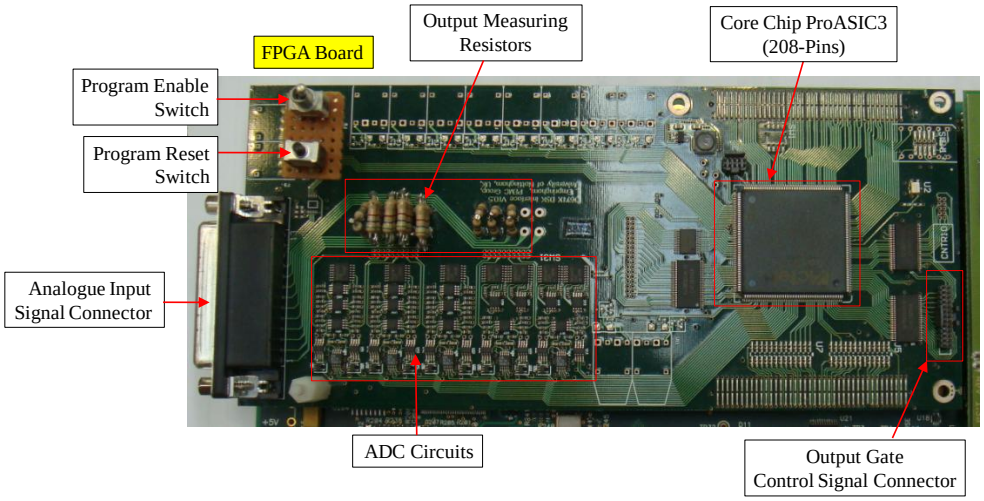


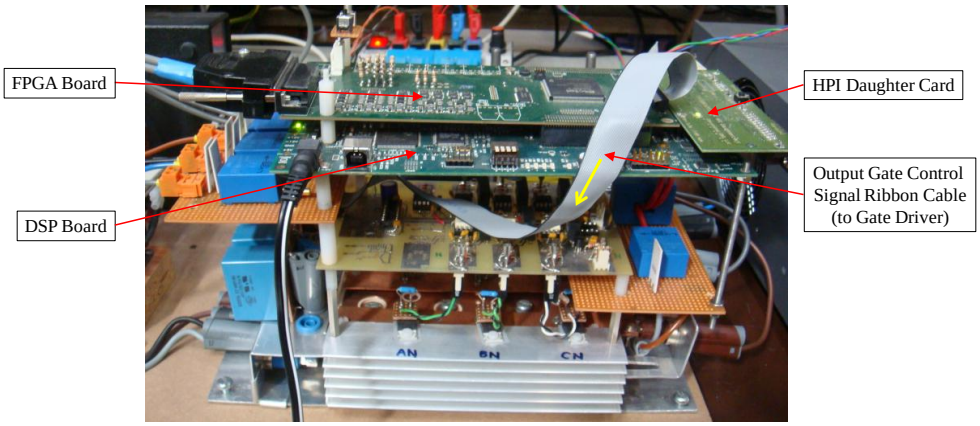
Figure 7.25 Photograph of the DSP board

7.5.3 FPGA Board

An FPGA board (Figure 7.26) which was designed by Dr. Lee Empringham and Dr. Liliana de Lillo, of the PEMC group in the University of Nottingham, is used in this work. The FPGA board operates with fixed clock frequency of 10MHz and provides 10 channels of 12-bit analogue to digital converters (ADC). The ±5V analogue signals are converted into 0 to 2.5V, which are required by the ADC circuits. The fault trip level for each ADC channel can be set individually using an onboard potentiometer and comparator circuit.



(a)

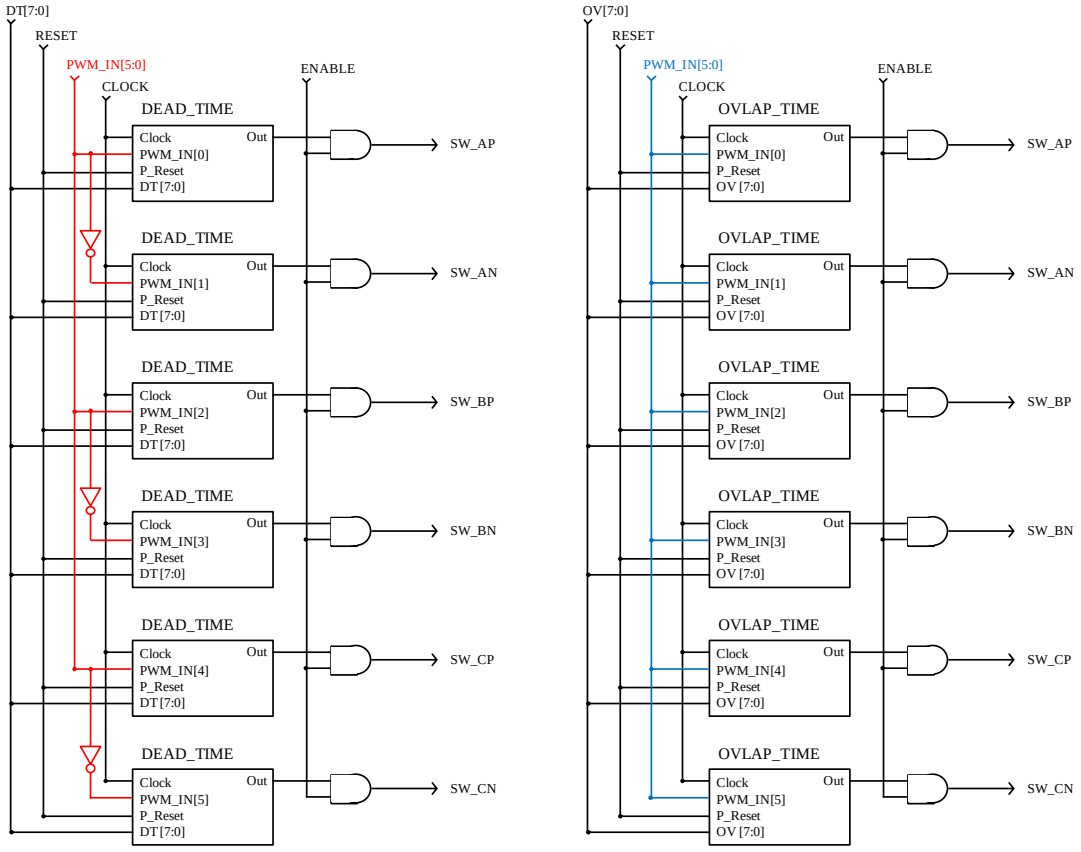


(b)

Figure 7.26 Photographs of (a) the FPGA board and (b) its connections

The Actel Libero IDE v.8.0 program is used to create and edit the control source codes of the FPGA using Very-high speed Hardware Description Language (VHDL). The most popular and easiest technique is to use the schematic editor tool, which allows the users to build their own circuit schematics using standard components from the program library or user defined components. Then the complete schematics can be converted later into VHDL using the program complier. In this work the FPGA schematic code for the Space Vector Modulation (SVM) for a three-phase voltage source inverter (VSI) developed by Dr. Liliana de Lillo is used [131]. However, some modifications are needed in order to be used for the three-phase CSI.

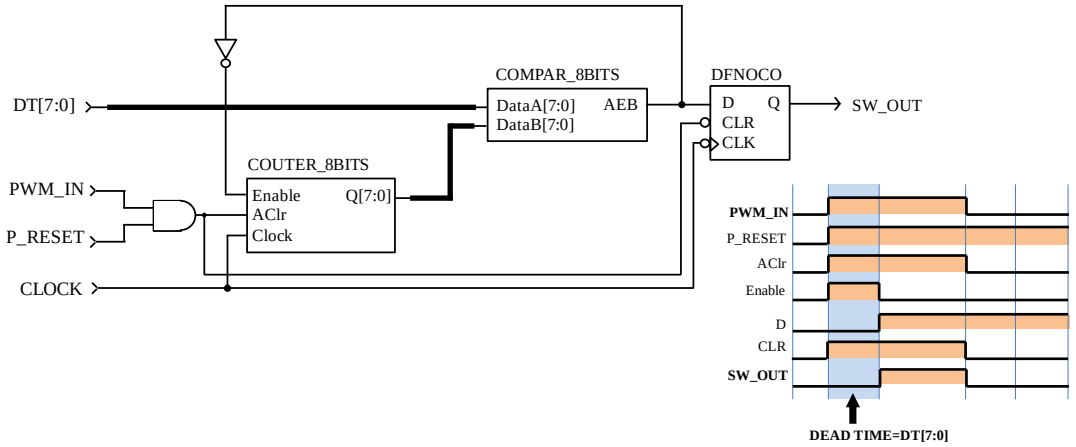
Figure 7.27 presents the first modification, which is required to separate the gate control signals for each switch to be independent rather than sharing the command signals as previously used for the voltage source inverter (VSI) applications.



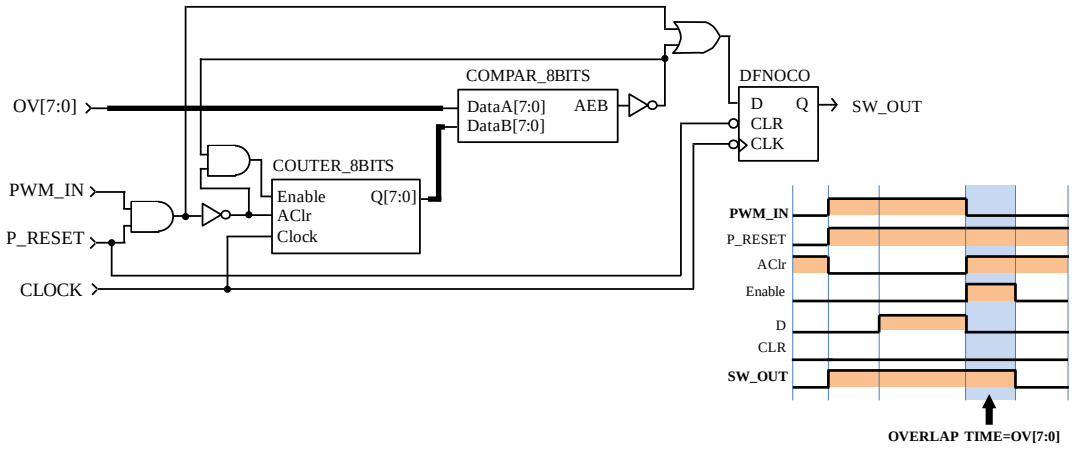
(a) Original schematic (b) modified schematic

Figure 7.27 Comparison of (a) original schematic and (b) modified schematic for the FPGA code in order to achieve independent gate control signals required for the CSI

The second modification is shown in Figure 7.28. The FPGA schematic is modified for the implementation of the overlap time for the CSI rather than the implementation of the dead time which was used for the voltage source inverter (VSI) in the previous work (see more details about the overlap time and the dead time in Section 4.3.1-4.3.2).



(a) Original schematic (dead time implementation)



(b) Modified schematic (overlap time implementation)

Figure 7.28 Comparison of (a) original schematic and (b) modified schematic for the FPGA code in order to achieve the overlap time implementation for the CSI

7.6 Protection Circuit

Figure 7.29 shows the circuit diagram and a photograph of the clamp circuit, which is used to limit high voltage spike caused by the demagnetisation of the DC-link inductors during shutdown the prototype CSI+SCaps (e.g. during fault conditions). The circuit consists of two power diodes, two capacitors and two resistors. The diodes are used to control the direction of current flow during the demagnetisation whilst the capacitors and resistors are used to restore and release the energy during and after the

demagnetisation of the DC-link inductors. The clamp circuit is placed between the DC input of the CSI power module and the DC-link inductors. It is noted that the reverse DC current blocking circuit, which is used to control the direction of the current flow (from PV emulator to the inverter), is also shown.

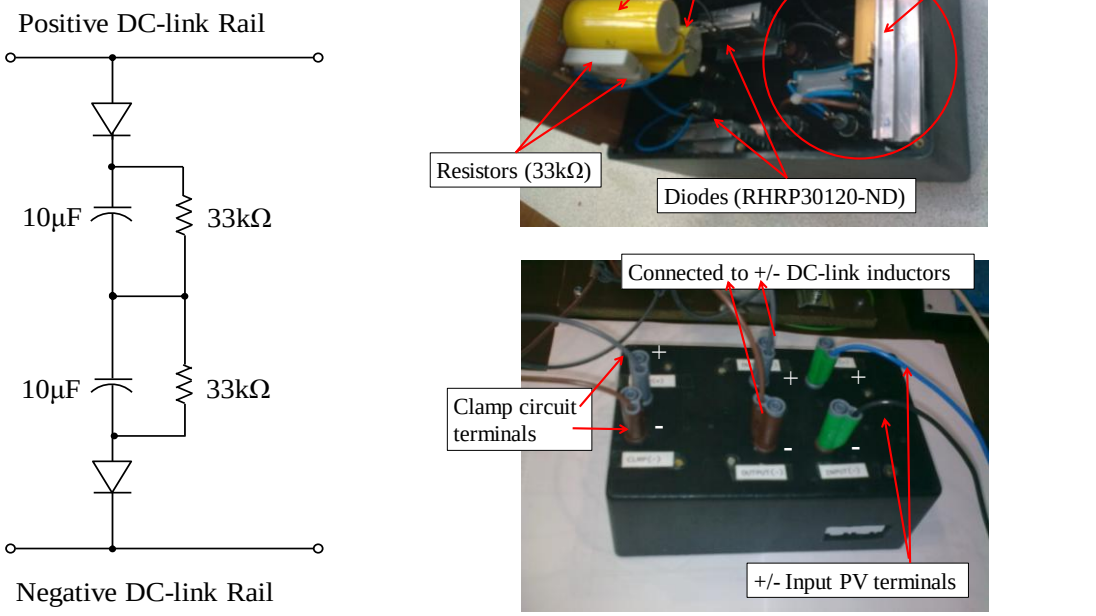


Figure 7.29 DC-link clamp circuit: (a) the circuit diagram and (b) photographs of the DC-link clamp circuit shown the inside view (top right) and the outside (bottom right) of the cover box

7.7 Three-Phase AC Electrical Network

Figure 7.30 shows the photographs of three-phase AC electrical network connection. The main circuit breaker, known as Residual-current Circuit Breaker with Overload protection (RCBO), is used to limit current (trip when a current over than its rating of 32A flows and provide earth leakage protection). The emergency stop switch is used to cut-off all power when pressed. The power ON/OFF switch is used to enable/disable the power from the AC power supply. The three-phase variac is used to vary the supply voltage amplitudes, which is used to observe the performance of the

converter prototype under the supply (grid) voltage deviation. In this work the electrical network operates at its nominal voltage of 230V/50Hz.

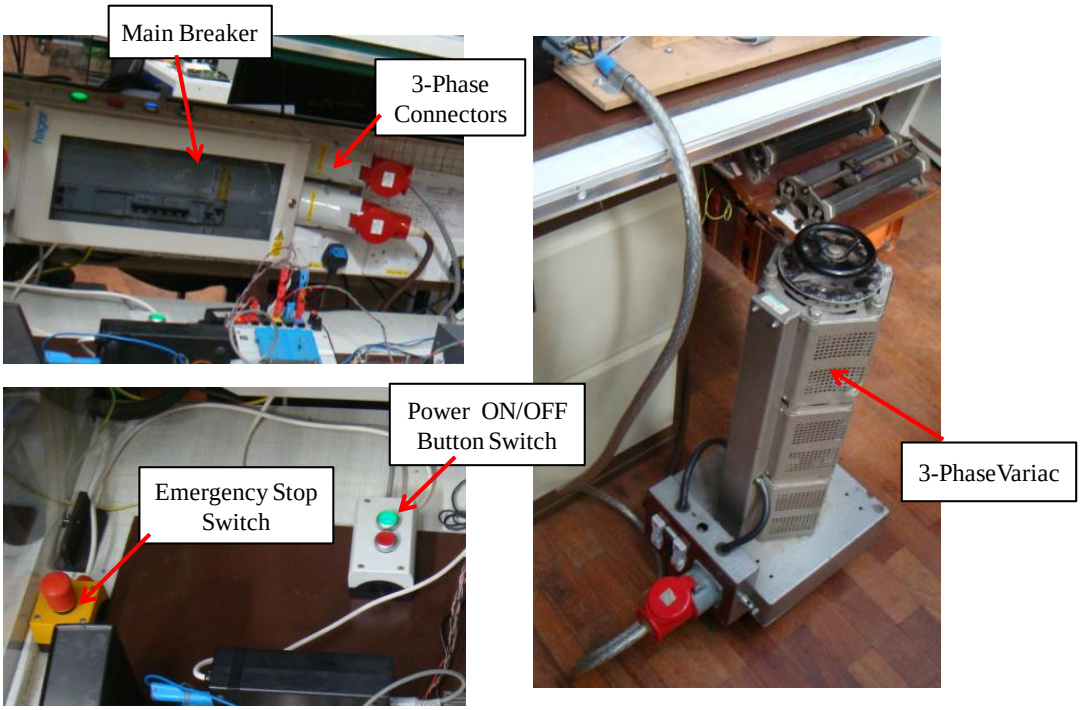


Figure 7.30 Photographs of the three-phase AC electrical network

7.8 Summary

This chapter presents the detailed design and construction of the experimental test-rig, which has been used to experimentally validate the performance of the proposed CSI with series AC capacitors (CSI+SCaps) in comparison to a standard CSI. The experimental test-rig consists of four main elements: the PV emulator, the prototype CSI+SCaps, the interfacing and control circuits and the three-phase AC electrical network.

The PV emulator is used to be a PV source providing output electrical characteristics similar to the actual designed PV array built from four strings of fourteen series connected PV panels (model BP SX30). The PV emulator consists of two elements: a programmable DC power supply (model SM300-10D) and an analogue control

circuit. The power supply generates desired output voltage and having a maximum output current limited as commanded by an analogue control circuit. The analogue control circuit is made of a small scale PV equivalent circuit that can produce control signals similar to the PV characteristics to program a DC power supply. The analogue control circuit includes also the test condition selecting circuit, which allows different sun irradiance conditions to be tested and facilitates the evaluation of the prototype CSI+SCaps in terms of the European efficiency.

The prototype CSI+SCaps is designed to operate as both the CSI+SCaps and a standard CSI. The prototype consists of the power circuit module, the filtering components and the series AC capacitors. The power circuit module is constructed from six RB-IGBTs, low stray inductance power bus bars with the planar plate configurations and air cooling heatsinks. The filtering components are included of the split DC-link inductors on the DC side and the LC filters with damping resistors at the AC side.

The interfacing and control circuits consist of the gate drive circuit, the voltage and current measurement circuits, the DSP and FPGA, the HPI daughter card and the computer. The gate drive circuit produces suitable gate voltage levels to operate the RB-IGBTs, limits gate control current and provides electrical isolation between the controller and the power module. The voltage and current measurement circuits measure the voltages and currents required by the controllers for using in the control programs. The DSP is the central processing unit that functions in all mathematical calculations and processing control commands. The FPGA is the interfacing unit that converts the measured analogue signals from the voltage and current measurement circuits into digital signals suitable for the DSP to process. The HPI daughter card is the data interfacing port for sending and receiving the commands or data between the DSP card and the computer. The computer is the programming workspace that allows the users to create, to edit, to compile and to upload the control programs for the DSP and FPGA.

The three-phase AC electrical network consists of a three-phase variac, a circuit breaker, a power on/off switch and an emergency stop switch. The three-phase variac allows the supply voltage level to be varied, which is used to observe the performance

of the prototype under supply voltage deviation. A circuit breaker disconnects the experimental test-rig from the power network if a current higher than its rating (32A) flows. A power on/off switch is used to enable/disable the power from the power supply. An emergency stop switch is used to cut-off all the power when pressed.

In addition, the DC-link clamp circuit is placed between the DC input of the prototype CSI+SCaps and the DC-link inductors. The circuit is used to limit DC-link voltage spike caused by demagnetisation of the DC-link inductors during shutdown the prototype.

Chapter 8

Experimental Results

This chapter presents the experimental results obtained from the test-rig designed in Chapter 7. Results are presented in two sets. The first set is used to verify the functionality of the test-rig. The second set is used to experimentally evaluate the performance of the CSI with series AC capacitors (or CSI+SCaps), which is the novel topology for transformerless, grid-tied PV applications proposed in Chapter 5. The results are compared to the standard CSI topology and also used to validate the simulation results given in Chapters 5 and 6.

8.1 Test-Rig Verification

As presented in Chapter 7 the experimental test-rig comprises of four main elements: the PV emulator, the CSI+SCaps prototype, the interfacing and control circuits and the 3-phase electrical network. This section provides the experimental results which verify the functionality of these elements in comparison to the design specifications.

8.1.1 PV Emulator

As described in Section 7.2 the PV emulator operates as an emulator of the PV source for the test system. The emulator is designed to generate the output voltage, current and power as specified by the PV characteristic curves shown in Section 2.7.4. Figure 8.1 shows the test circuit diagram which was used to verify the PV emulator. Figures 8.2 and 8.3 show the experimental results which can be compared with the design specifications.

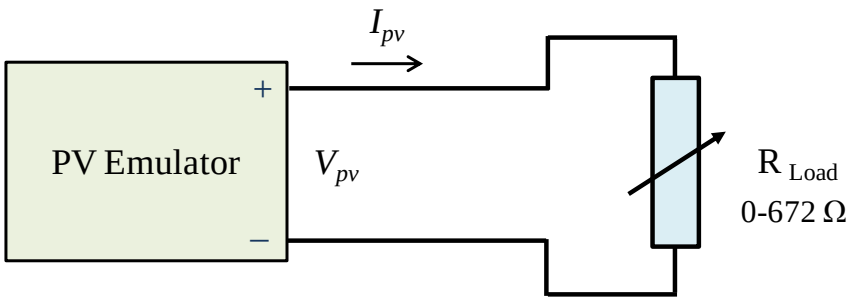


Figure 8.1 Circuit diagram used to verify the PV emulator

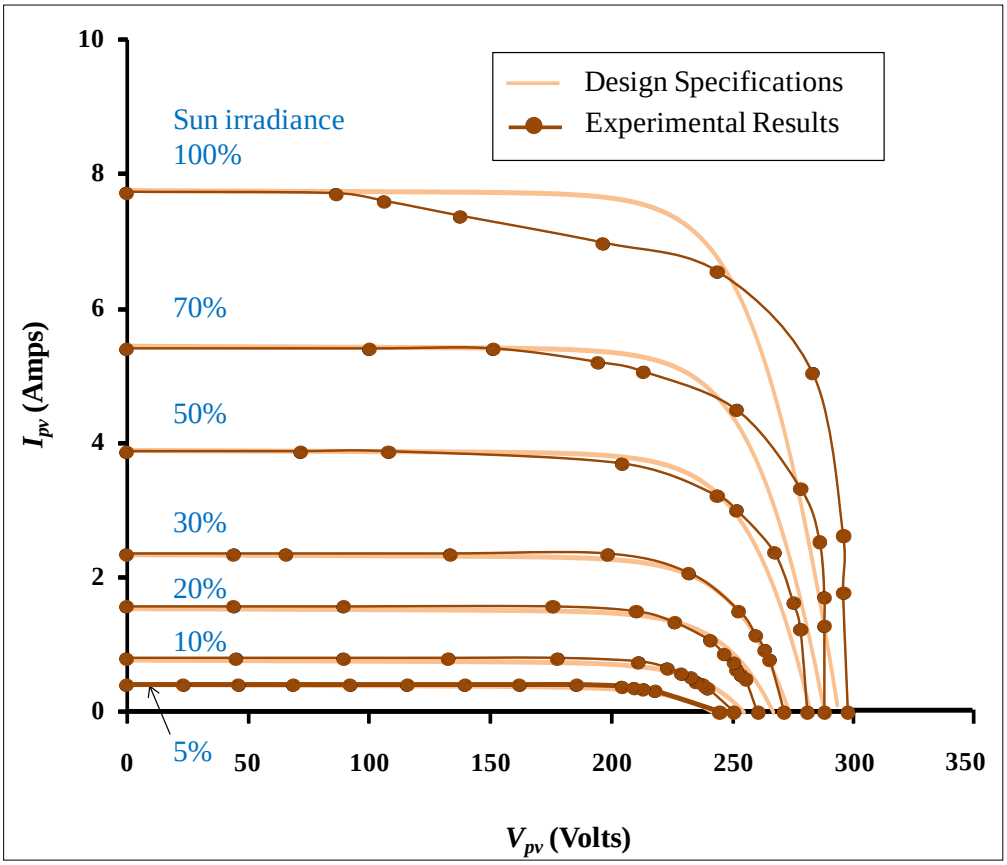


Figure 8.2 Experimental results for the PV emulator and design specification I-V characteristic curves at varying sun irradiance levels; where V_{pv} is the output PV voltage and I_{pv} is the output PV current

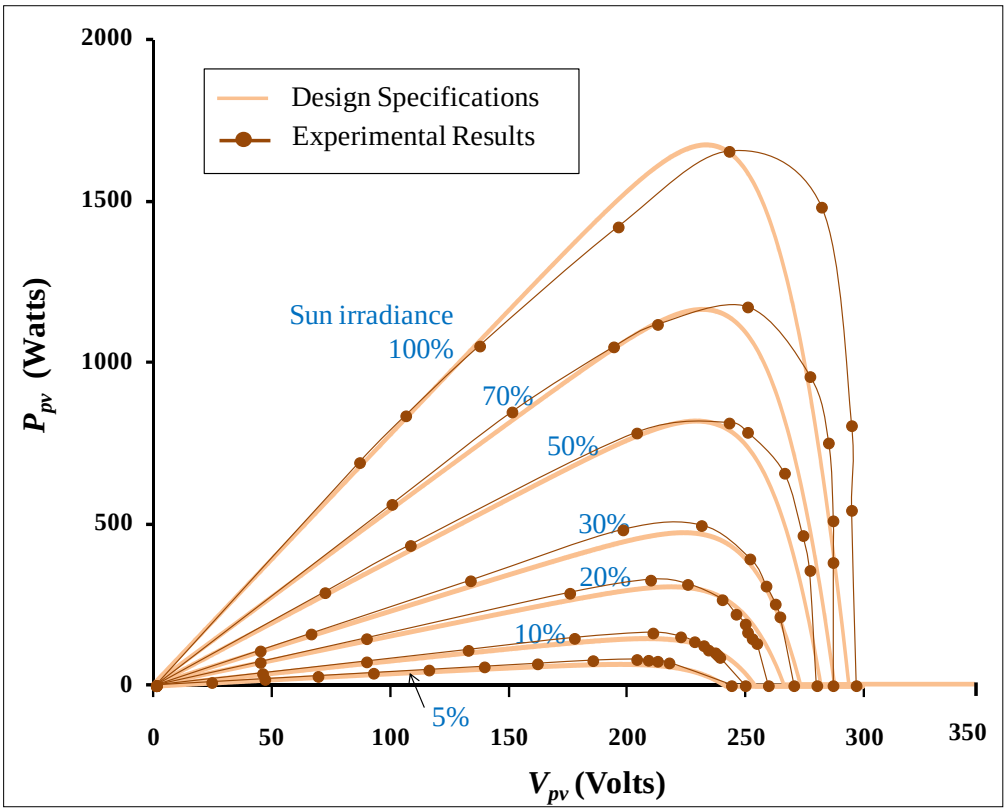


Figure 8.3 Experimental results for the PV emulator and design specification P-V characteristic curves at varying sun irradiance levels; where V_{pv} is the output PV voltage and P_{pv} is the output PV power

It can be seen from Figures 8.2 and 8.3 that the PV emulator exhibits output current, voltage and power profiles similar to the design specification. A very close match can be observed at 5%-50% sun irradiance levels. However, at higher sun irradiance levels (70% and 100%) the PV emulator has a PV current which decays more rapidly and has a higher current at high voltage than the specification as shown in Figure 8.2. This has an effect on the higher PV output power when compared to the design specification as shown in Figure 8.3. The difference between the experimental results and the design specifications at high sun irradiance levels is caused by the non-linear characteristics of the components used in the analogue control circuit of the emulator. For example, the power MOSFET (STP36NF06L) which is used to convert a current of 0-10A into a control signal of 0-5V will begin to have a nonlinear relationship when operating above 4-5A (see more details in Section 7.2.3). However, this difference will not affect the evaluation of the CSI+SCaps topology and a standard CSI topology as the same PV emulator will be used for both circuits. Therefore comparable results can be obtained.

Figure 8.4 shows the experimental waveforms of output PV voltage (V_{pv}) and output PV current (I_{pv}) of the emulator when sun irradiance levels change in steps from 5% to 100% and from 100% to 5% whilst R_{load} is fixed at 56Ω.

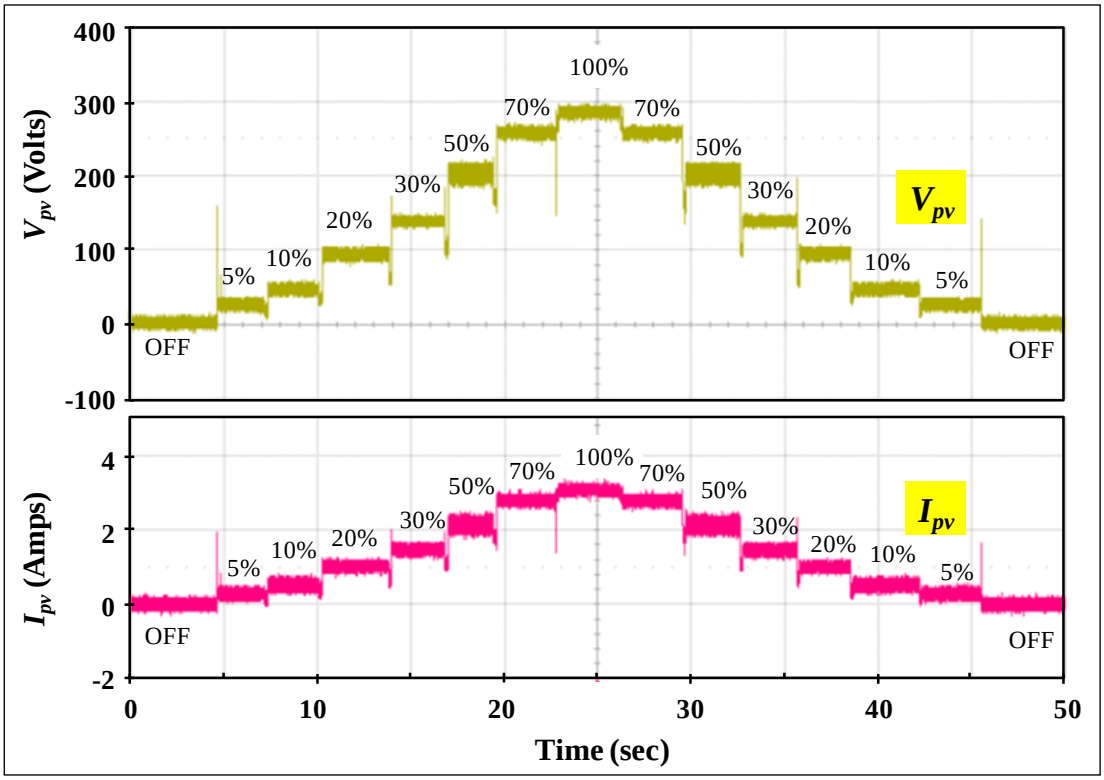


Figure 8.4 Experimental waveforms of output PV voltage (V_{pv}) and output PV current (I_{pv}) of the PV emulator when R_{load} is fixed at 56Ω and sun irradiance levels change in steps from 5% to 100% and 100% to 5%

It can be seen from Figure 8.4 that the PV emulator can produce stable and consistent output PV voltage and current waveforms for each constant sun irradiance level and can provide continuous output waveforms when sun irradiance levels change. Stable and consistent output waveforms from the PV emulator are important for the experimental tests as one may need to repeat tests at specific operating points or test for long periods of time (e.g. inverter efficiency tests in Section 8.2.4). Continuous output waveforms from the PV emulator will provide a realistic behaviour similar to an actual PV source. The short drops in the output waveforms during the transitions of sun irradiance levels of the emulator are caused by the overlap of two switches on the analogue control circuit board of the emulator (see more details in Section 7.2.3).

8.1.2 CSI with Series AC Capacitors Inverter Prototype

As presented in Section 7.3 the CSI with series AC capacitors (CSI+SCaps) prototype is the main focus of the experimental testing. The inverter prototype is designed to convert and transmit power from the PV emulator into a 280V/50Hz three-phase grid connection. The inverter prototype is also designed to operate as a standard CSI so that comparable test results can be produced. Figure 8.5 shows experimental set up used to test functionality of the inverter prototype together with the interfacing and control circuits.

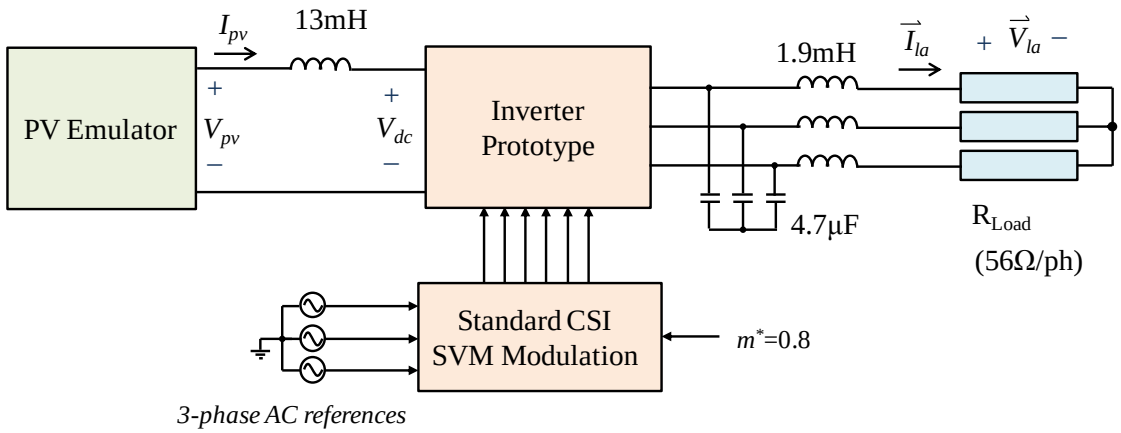
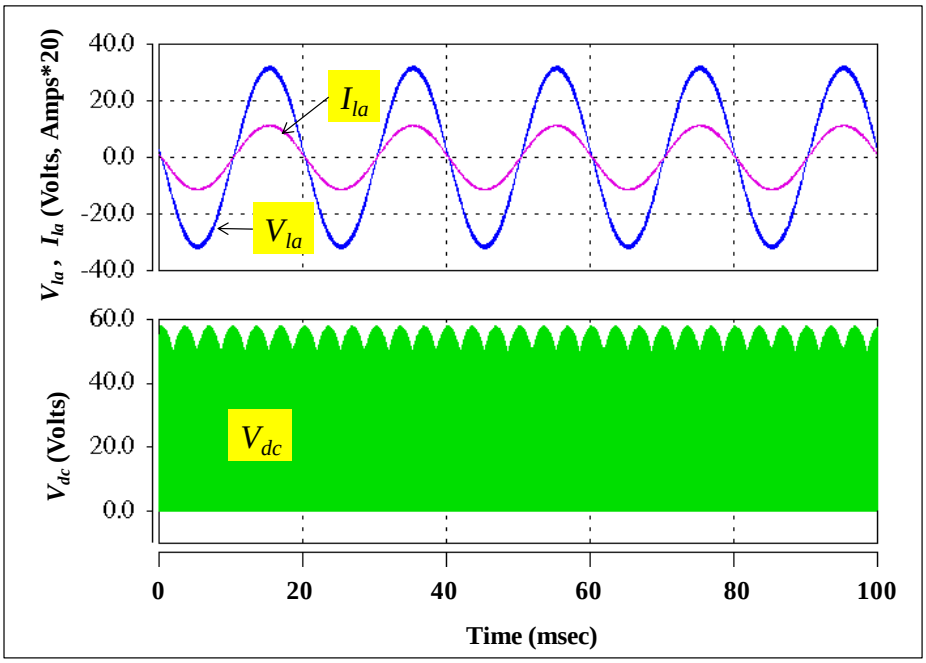
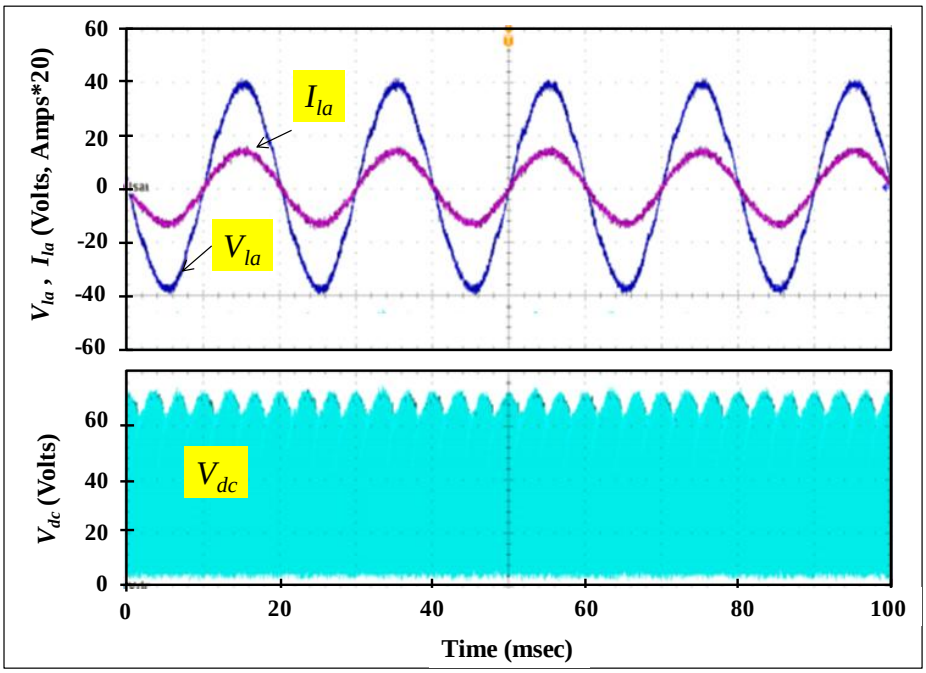


Figure 8.5 Circuit diagram used to verify the CSI+SCaps inverter prototype

In the circuit shown in Figure 8.5, in order to simplify the testing of the inverter prototype, the inverter is operated as a standard CSI and is connected to a three-phase resistive load rather than directly to the grid in order to allow simple open-loop control to be used. The inverter operates with a fixed modulation depth (m^*=0.8) and with standard CSI SVM modulation (see Section 4.3.2), which generates more ideal gate control signals and therefore allows good comparisons to be made with the simulation results. The corresponding experimental results obtained from the inverter prototype when operating at 10% sun irradiance and a comparison to the simulation results are shown in Figure 8.6.



(a)



(b)

Figure 8.6 (a) Simulation and (b) experimental results of the CSI+SCaps inverter prototype when operating as a standard CSI with the modulation depth of 0.8 at 10% sun irradiance

It can be seen from Figure 8.6 that the inverter prototype can provide similar results to the simulation. The prototype produces sinusoidal and in phase waveforms of the AC load voltage and the AC load current as expected for standard CSI VSM modulation.

The output AC load current amplitude is 0.65A with an input PV current of 0.8A (see Figure 8.4), which gives a modulation index of 0.81. This result confirms the proper operation of the inverter prototype.

Figure 8.7 shows the experimental results of the inverter prototype when sun irradiance changes from 10% to 20% and from 20% to 30%. It can be seen that the inverter prototype can provide continuous and stable output AC load waveforms for each constant sun irradiance level and during transitions. The small drop in the load voltage and current during the transition are caused by overlap in the switches as explained in Section 8.1.1.

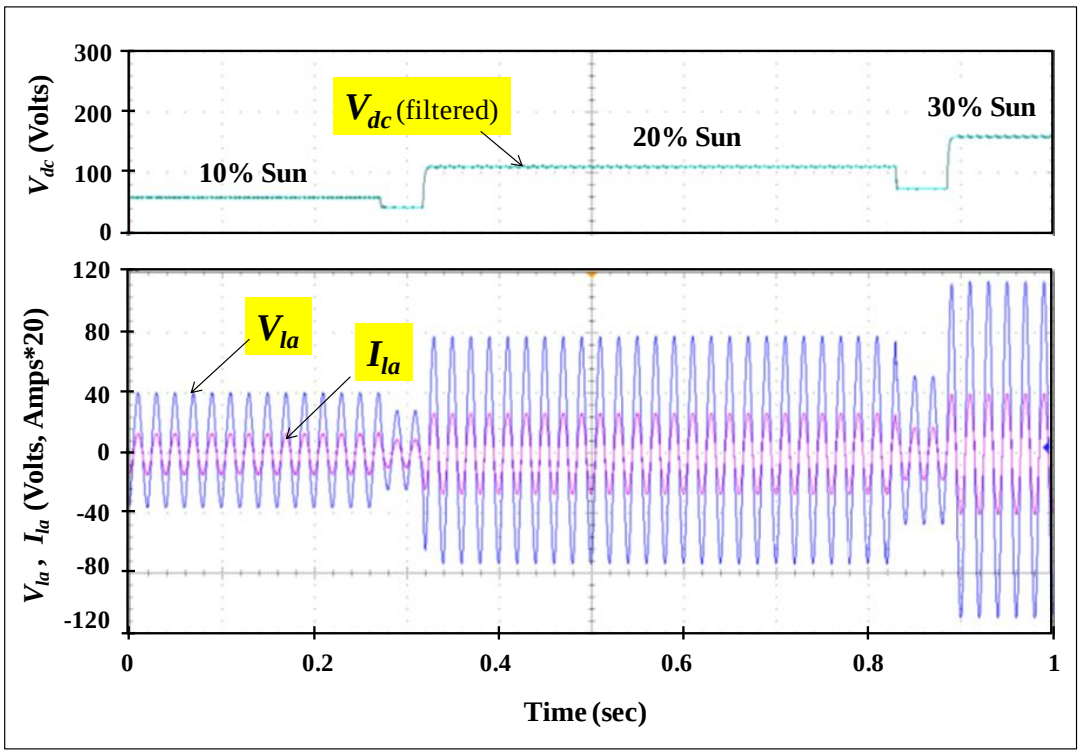


Figure 8.7 Experimental results of the inverter prototype when operating under the sun irradiance changes from 10% to 20% and 30%

8.2 Evaluation of the CSI with Series AC Capacitors

In this section the experimental results obtained from the testing of a complete grid-tied PV system with the CSI+SCaps topology (shown in Figure 8.8) are evaluated in comparison to the standard CSI topology. The results are presented in four sets. The

first set is related to safe operation of the topology during start-up and shutdown. The second set and the third set of results are the performance of the topology when operating at normal grid voltage and at low grid voltage respectively. The forth set of results is the efficiency evaluation for the topology.

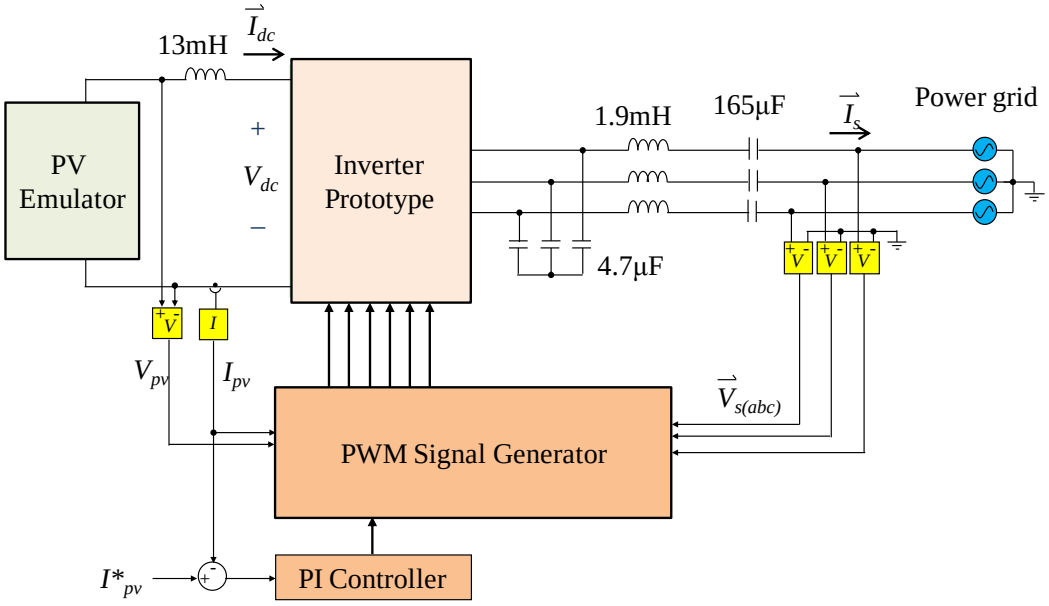
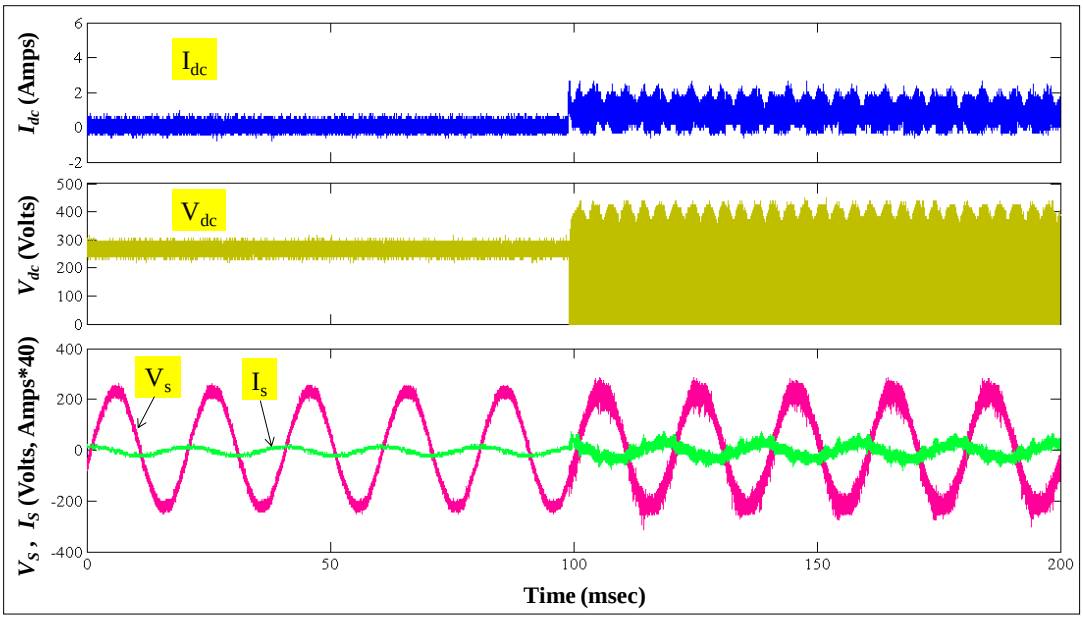


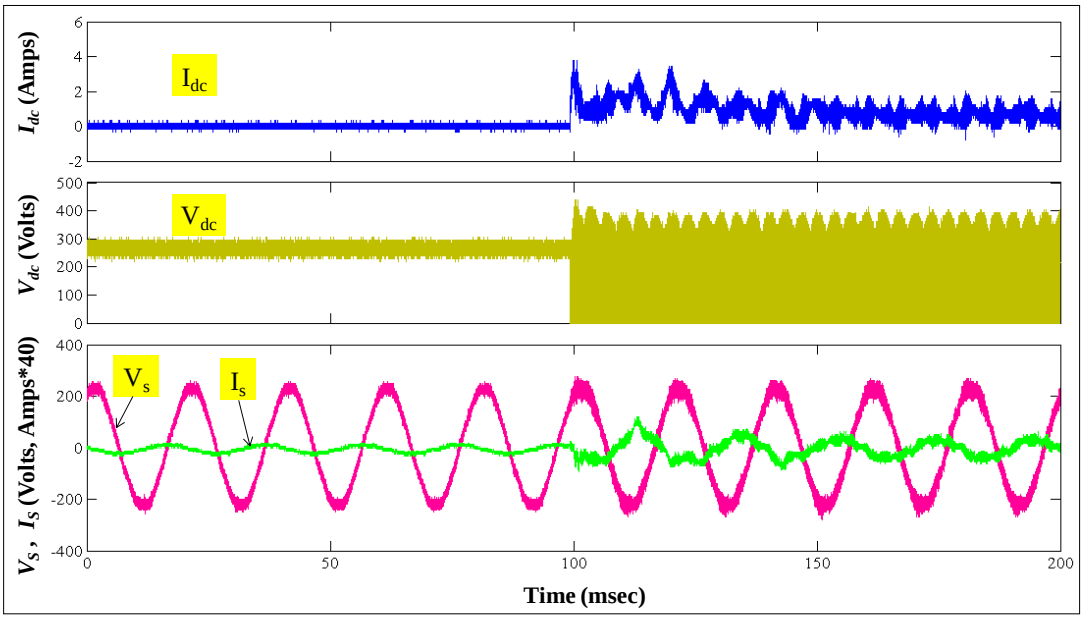
Figure 8.8 Diagram of the grid-tied PV test system based CSI+SCaps topology

8.2.1 Performance during Start-Up and Shutdown Conditions

This section presents converter performance related to the safe operation of the CSI+SCaps topology during start-up and shutdown tests in comparison to a standard CSI topology. The same circuit components and PI-controller are used for both topologies so that the results can be directly compared. Figures 8.9 and 8.10 show the experimental results of the CSI+SCaps topology and the standard CSI topology during the start-up and shutdown tests.

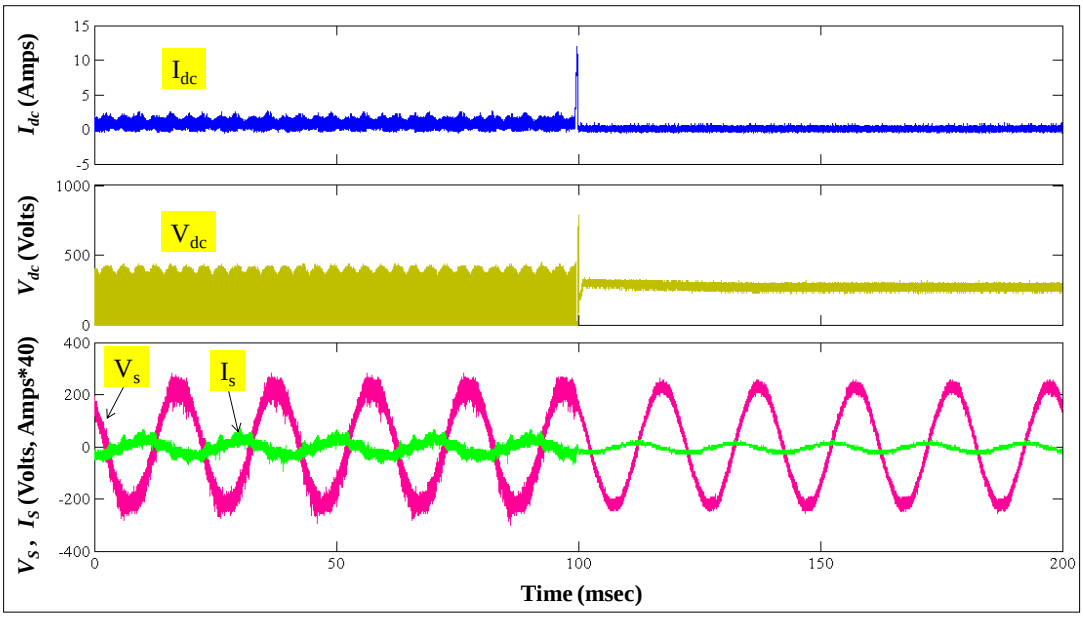


(a) Standard CSI

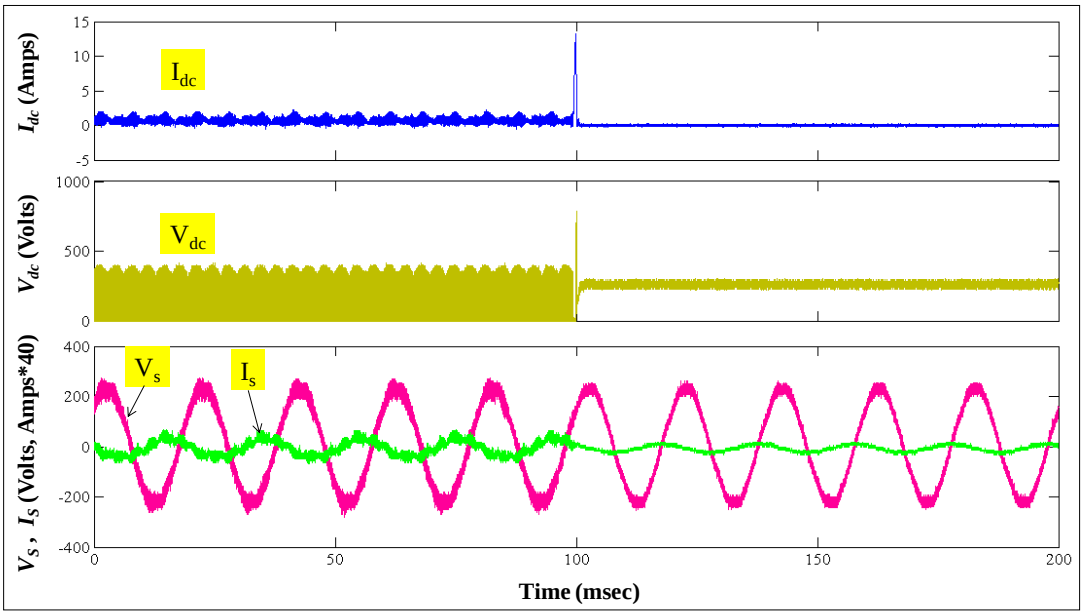


(b) CSI+SCaps

Figure 8.9 Experimental results for (a) the standard CSI topology and (b) the CSI+SCaps topology during start-up at time= 100msec



(a) Standard CSI



(b) CSI+SCaps

Figure 8.10 Experimental results for (a) the CSI topology and (b) the CSI+SCaps topology during shutdown at time= 100msec

As it can be seen from Figure 8.9 both the CSI+SCaps topology and the CSI topology can operate safely during start-up with low DC-link voltage and current overshoots (V_{dc}< 450V and I_{dc}< 4A) compared to the ratings of the switches (1200V and 25A). The CSI+SCaps topology has slightly higher DC-link voltage and current overshoots and a slower dynamic response than the CSI topology, which is caused by the large series AC capacitors (165μF) used in the AC circuit of the CSI+SCaps topology. However, the CSI+SCaps topology has a lower DC-link current ripple than the CSI topology.

As it can be seen from Figure 8.10 both the CSI+SCaps topology and the CSI topology have higher DC-link voltage and current overshoots during shutdown compared to start-up. However, both topologies can provide safe operation as the voltage and current overshoots (V_{dc}< 900V and I_{dc}< 15A) are lower than the ratings of the switches. The high voltage and current overshoots are caused by the demagnetisation of the large DC-link inductor (13mH) used on the DC side.

8.2.2 Performance during Normal Grid Voltage Conditions

This section presents the experimental results for the CSI+SCaps topology and the standard CSI topology when operating under normal grid voltage conditions. The results are presented in three sets. The first and second sets show the steady state and dynamic operation of the topologies under constant sun irradiance. The third set shows steady state operation under different sun irradiance levels. The Minimum Switching Voltage (MSV) control (see Section 5.3.2.1) is used for both the topologies in these tests.

8.2.2.1 Steady State Results under Constant Sun Irradiance

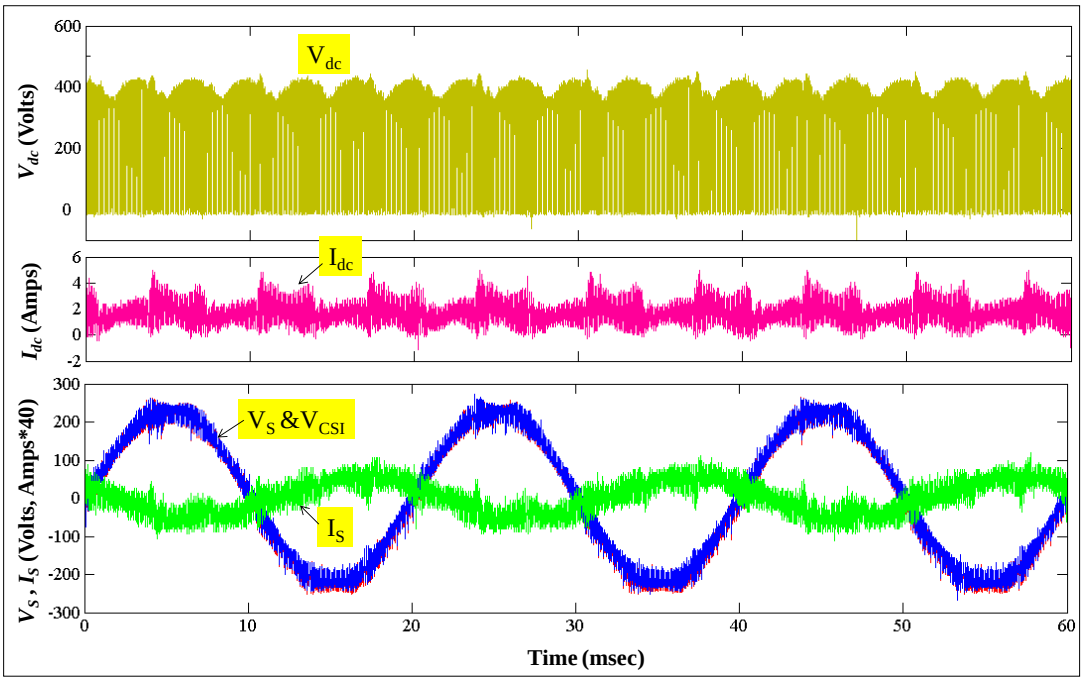
As mentioned in Section 3.1 grid-tied PV inverters are required to operate at the maximum voltage, current and power ratings of the PV source for proper connection compatibility between the PV source and inverters. Under normal grid voltage and constant sun irradiance, the maximum voltage rating of the PV source is the open-circuit PV voltage and the maximum current and power ratings are the current and

power at the maximum power point (MPP) of the PV source. This section presents the experimental results for the CSI+SCaps topology and the standard CSI topology when operating close to these maximum PV ratings.

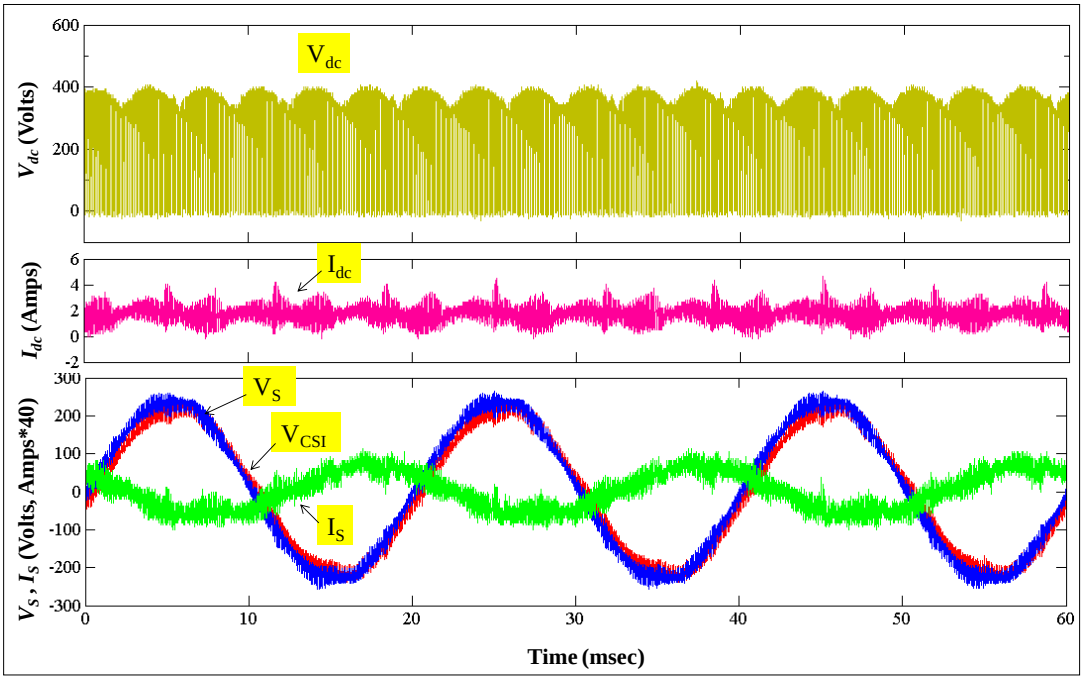
Figures 8.11 and 8.12 show the experimental results for the topologies operating close to the maximum PV voltage ratings (OP1) and at the MPP (OP2) under 50% sun irradiance. The frequency spectrum of the supply current waveforms for each topology at OP1 and OP2 are shown in Figures 8.13 and 8.14. The measured magnitudes of the waveforms in Figures 8.11, 8.12, 8.13 and 8.14 are summarised in Table 8.1.

Measured Parameter		OP1		OP2	
		Standard CSI	**CSI+SCaps**	**Standard CSI**	**CSI+SCaps**
DC Side	$\mathbf{V_{dc\ (peak)}}$	456V	419V	463V	381V
	$\mathbf{V_{dc\ (average)}}$	271V	283V	246V	251V
	$\mathbf{I_{dc\ (peak)}}$	5.2A	4.2A	6.9A	5.2A
	$\mathbf{I_{dc\ (average)}}$	1.7A	1.7A	3.2A	3.2A
	$\mathbf{\Delta I_{dc\text{-}ripple(peak\text{-}peak)}}$	5.4A	4.1A	6.2A	3.2A
	$\mathbf{P_{dc\ (average)}}$	461W	481W	787W	803W
AC Side	$\mathbf{V_{S\ (rms)}}$	161V	162V	163V	162V
	$\mathbf{V_{CSI\ (rms)}}$	163V	156V	163V	138V
	$\mathbf{I_{S\ (rms)}}$	1.1A	1.2A	1.7A	2.2A
	Power Factor	0.86	0.84	0.98	0.78
	$\mathbf{I_{S\ (fundamental)}}$	1.56A	1.69A	2.40A	3.11A
	$\mathbf{I_{S\ (THD)}}$	18.5%	13.5%	15.6%	7.8%

Table 8.1 Measured magnitudes of the waveforms in Figures 8.11 to 8.14

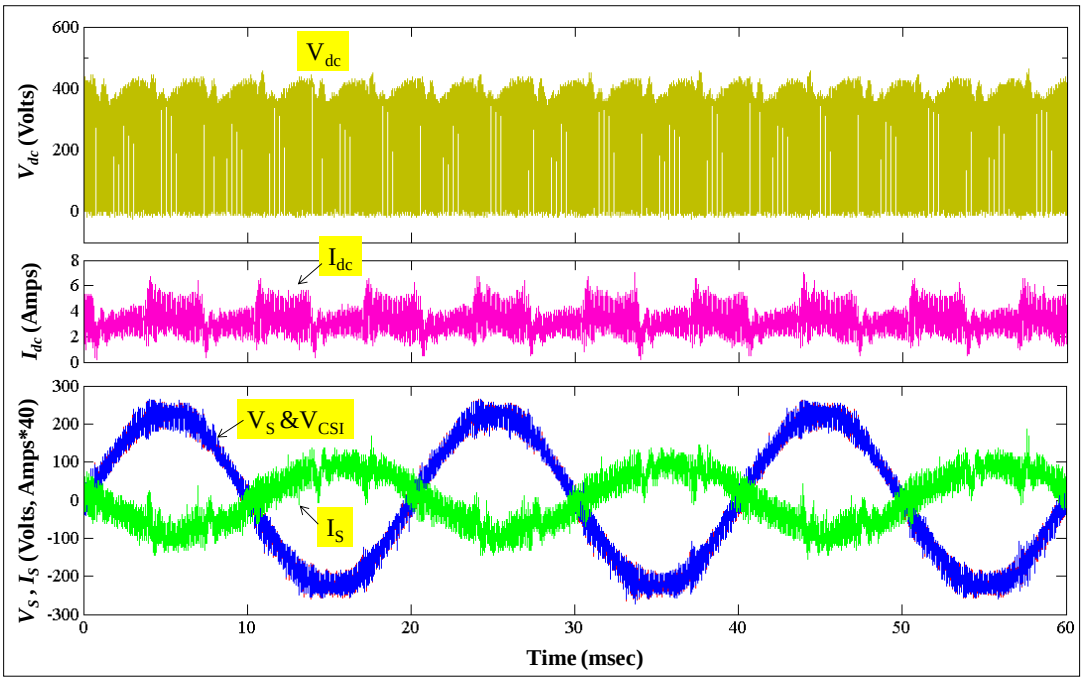


(a) Standard CSI

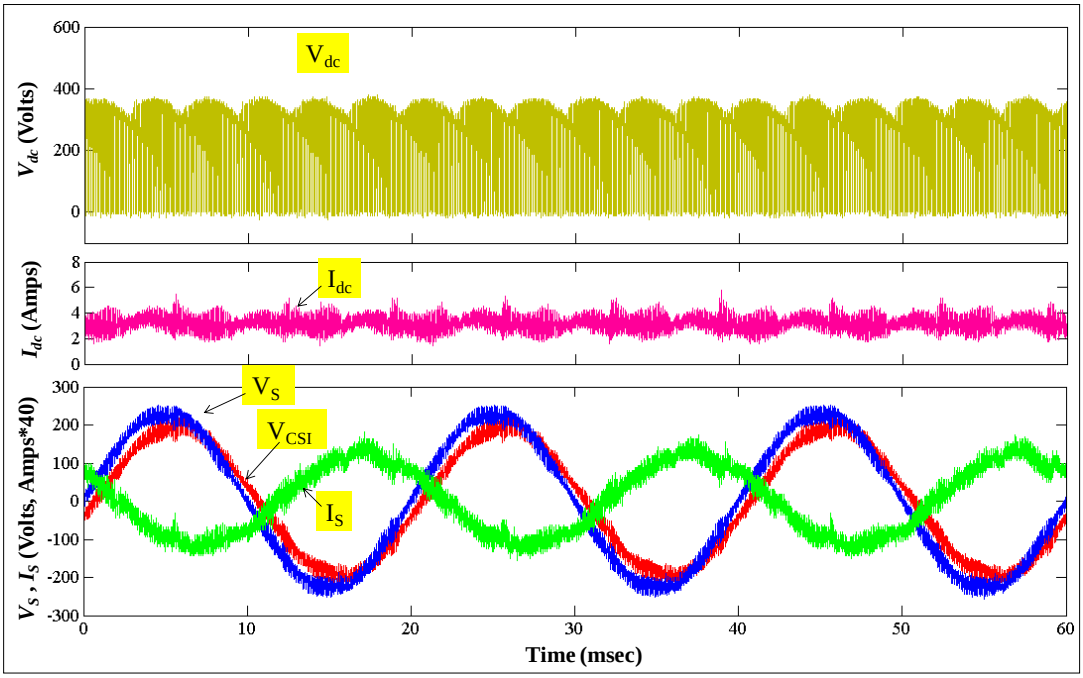


(b) CSI+SCaps

Figure 8.11 Experimental results of (a) the CSI topology and (b) the CSI+SCaps topology operating at the point close to the maximum PV voltage rating (OP1)

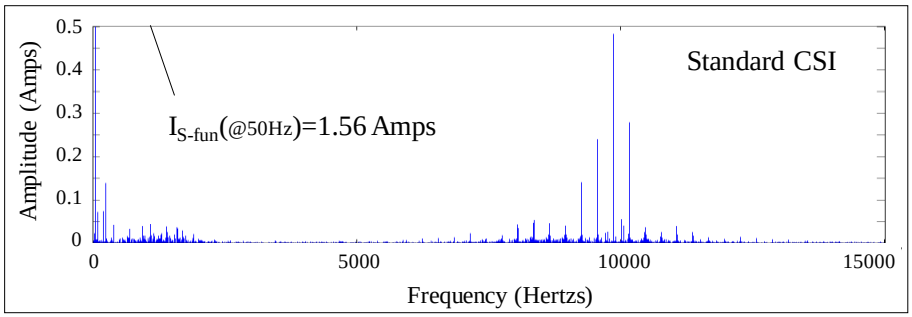


(a) Standard CSI

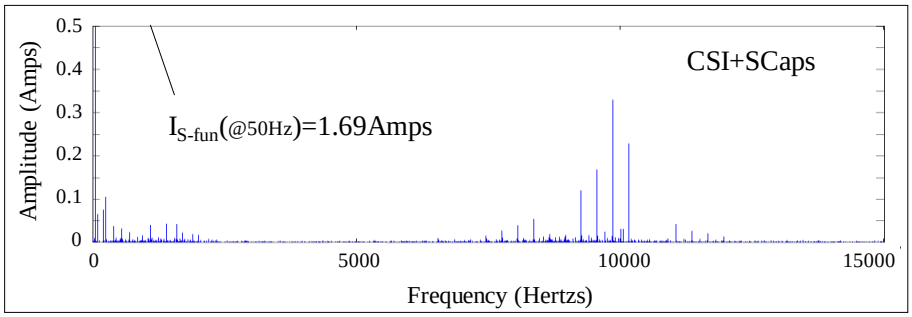


(b) CSI+SCaps

Figure 8.12 Experimental results of (a) the CSI topology and (b) the CSI+SCaps topology operating at the maximum PV current and power point (OP2)

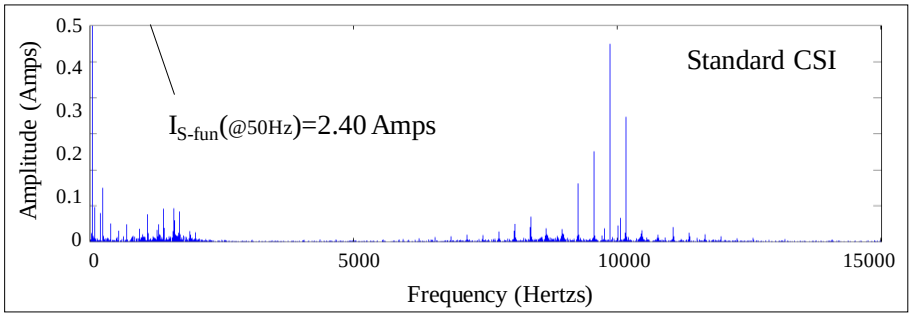


(a) Standard CSI

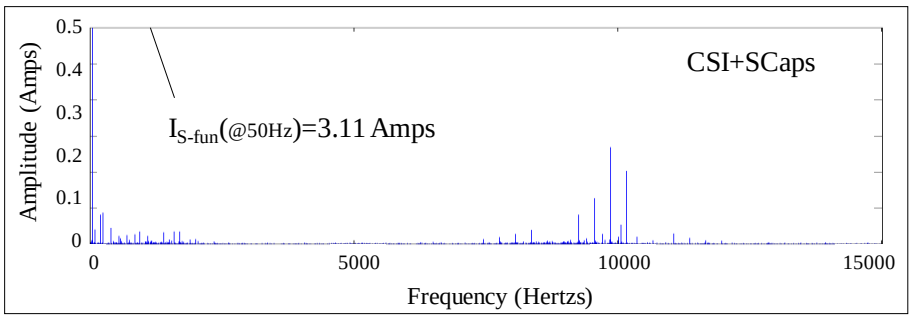


(b) CSI+SCaps

Figure 8.13 Frequency spectrum of the supply current (I_S) waveform in Figure 8.11



(a) Standard CSI



(b) CSI+SCaps

Figure 8.14 Frequency spectrum of the supply current (I_S) waveform in Figure 8.12

It can be seen in Figures 8.11 to 8.14 and Table 8.1 that:

- The experimental waveforms in Figures 8.11 and 8.12 agree with the results of the operation principles presented in Section 5.5.1 and simulation waveforms shown in Figures 5.22 and 5.24.

- As expected, in Figure 8.11, the CSI+SCaps topology and the standard CSI topology provide similar waveforms when operating close to the maximum PV voltage rating (OP1); whereas the CSI+SCaps topology draws low PV current (1.7A) and produces only insignificant voltages across the series AC capacitors.

- At the maximum power point (OP2), the CSI+SCaps topology draws higher PV current (3.2A) and produces higher voltages across the series AC capacitors. These voltages are used to reduce the AC side voltages (V_{CSI}) for the CSI+SCaps topology, as shown in Figure 8.12. In contrast, the CSI topology has the same V_{CSI} levels to the supply voltage level (V_S).

- When both operating points are considered, the CSI+SCaps topology has more advantages than the standard CSI topology because it has:

    - Lower peak DC-link voltage (381-419V) than the CSI (456-463V) and therefore a lower voltage stress on the circuit components than the CSI.

    - Lower peak DC-link current (4.2-5.2A) than the CSI (5.2A-6.9A) and thus a lower current stress on the circuit components than the CSI.

    - Lower peak-to-peak DC-link current ripple (3.2-4.1A) than the CSI (5.4-6.2A) and therefore a better input power quality and allowing the use of a smaller DC filter inductor than the CSI.

    - Lower supply current THD (7.8-13.5%) than the CSI (15.6-18.5%) and therefore a better output power quality than the CSI, as shown in Figures 8.13 and 8.14.

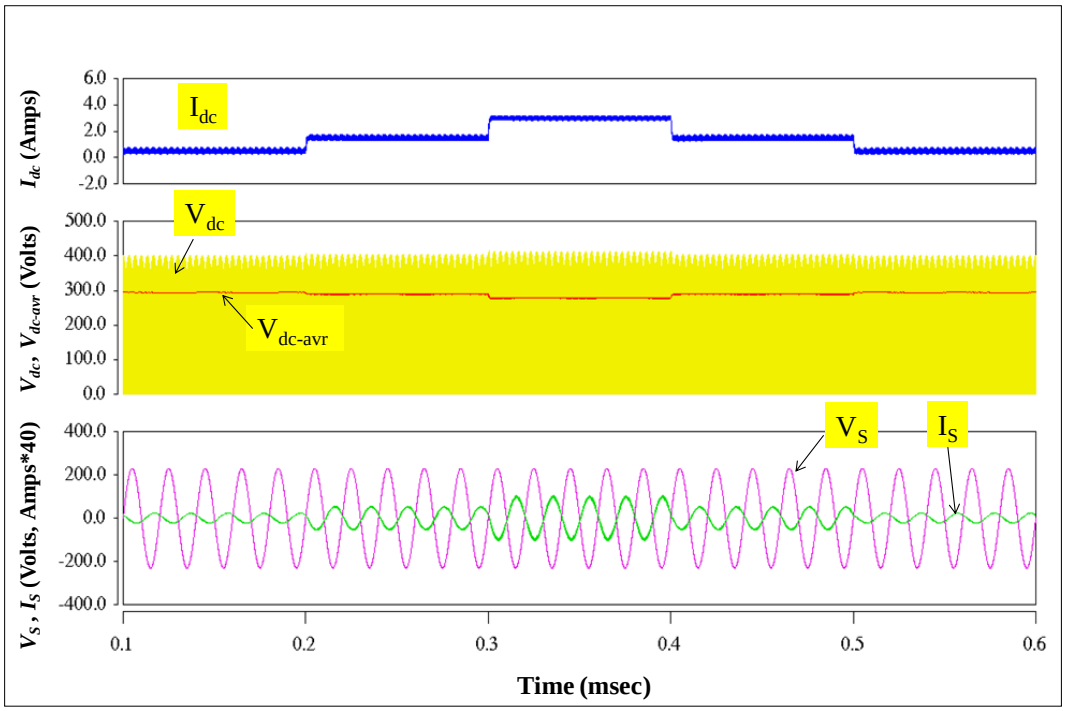
- The CSI+SCaps topology has some disadvantages when compared to the CSI topology in that it has higher fundamental supply current (1.7-3.1A) than the CSI (1.6-2.4A) and a lower power factor (0.78-0.84) than the CSI (0.86-0.98). These characteristics lead to the need for slightly larger wires for connection

to the power transmission network for the CSI+SCaps topology when compared to the CSI topology.

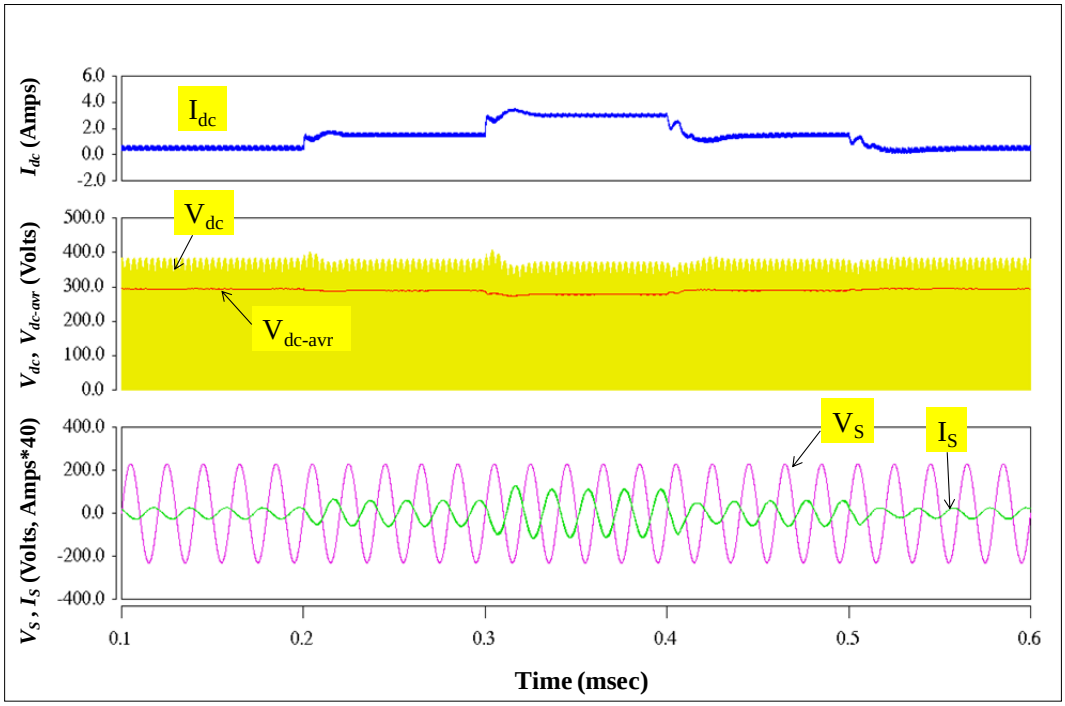
8.2.2.2 Dynamic Results under Constant Sun Irradiance

Figures 8.15 and 8.16 show the simulation and experimental results for the CSI+SCaps topology and the standard CSI topology operated at 70% sun irradiance. In order to observe the dynamic response of the topologies, the PV current is stepped up from 0.5A to 1.5A at time=100ms and from 1.5A to 3.0A at time=200ms and then decreasing from 3.0A to 1.5A at time=300ms and from 1.5A to 0.5A at time=400ms. The circuit components and parameters used in both the simulation and experimental tests are the same as ones shown in Figure 8.8. It can be seen from Figures 8.15 and 8.16 that:

- The converter prototype provides similar results to the simulation. The CSI+SCaps topology and the standard CSI topology can track closely the change of the DC-link current reference and reach the demand values in steady state.
- With the use of the same circuit components and a PI-controller both the experimental results and the simulation results show that:
    - The CSI+SCaps topology provides a slower dynamic response compared to the standard CSI topology. This would be reflected in more fluctuations during transients and longer settling times for the CSI+SCaps topology when compared to the standard CSI.
    - The CSI+SCaps topology provides lower DC-link current/voltage ripple and lower peak DC-link voltage compared to the standard CSI. Additionally, the CSI+SCaps provides lower line current THD, especially at higher loads (3.0A at the time duration between 200ms and 300ms).

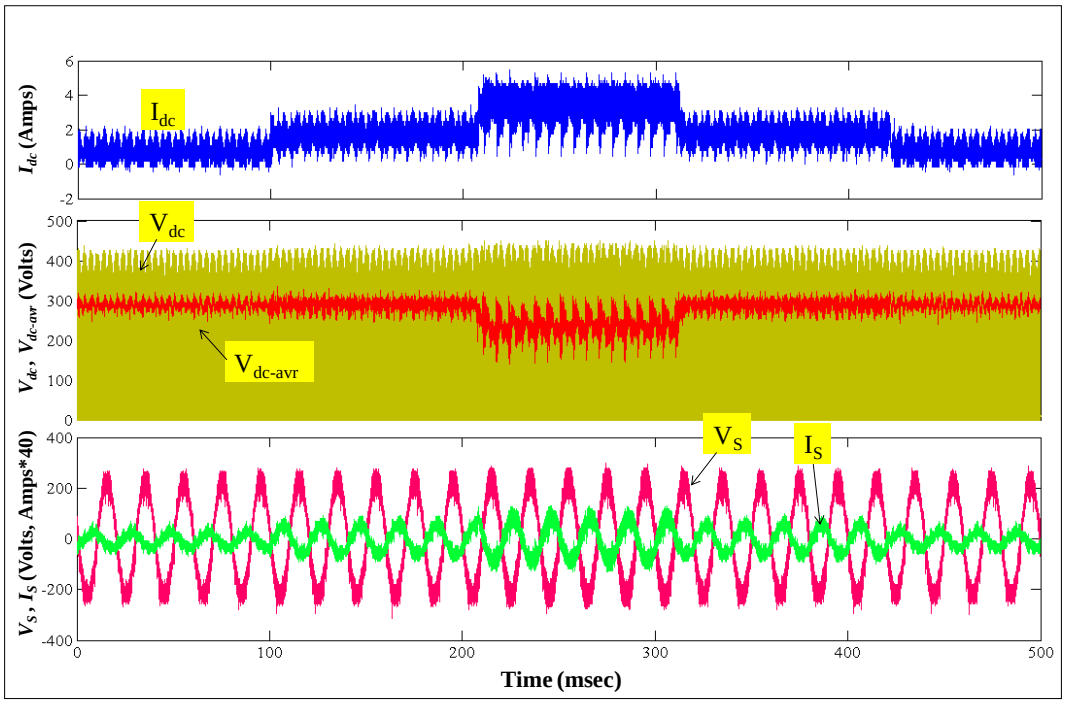


(a) Standard CSI

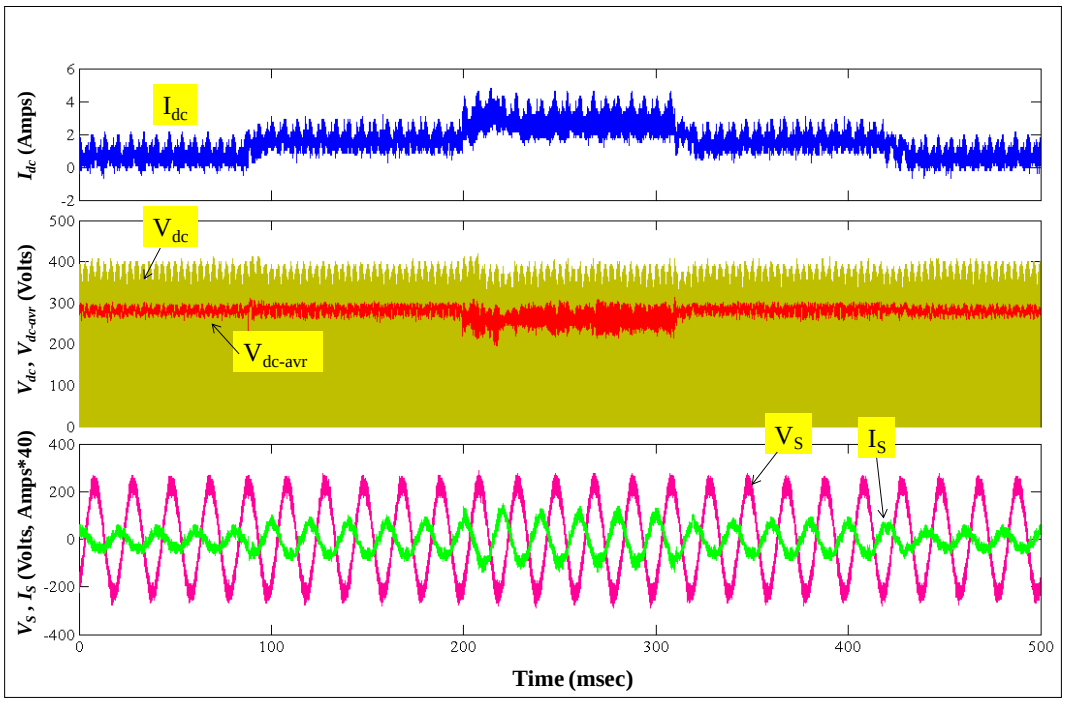


(b) CSI+SCaps

Figure 8.15 Simulation results of (a) the CSI topology and (b) the CSI+SCaps topology operating under 70% sun irradiance and PV current steps from 0.5A to 1.5A at time=100msec, 1.5A to 3.0A at time=200msec, 3.0A to 1.5A at time=300msec and 1.5A to 0.5A at time=400msec



(a) Standard CSI



(b) CSI+SCaps

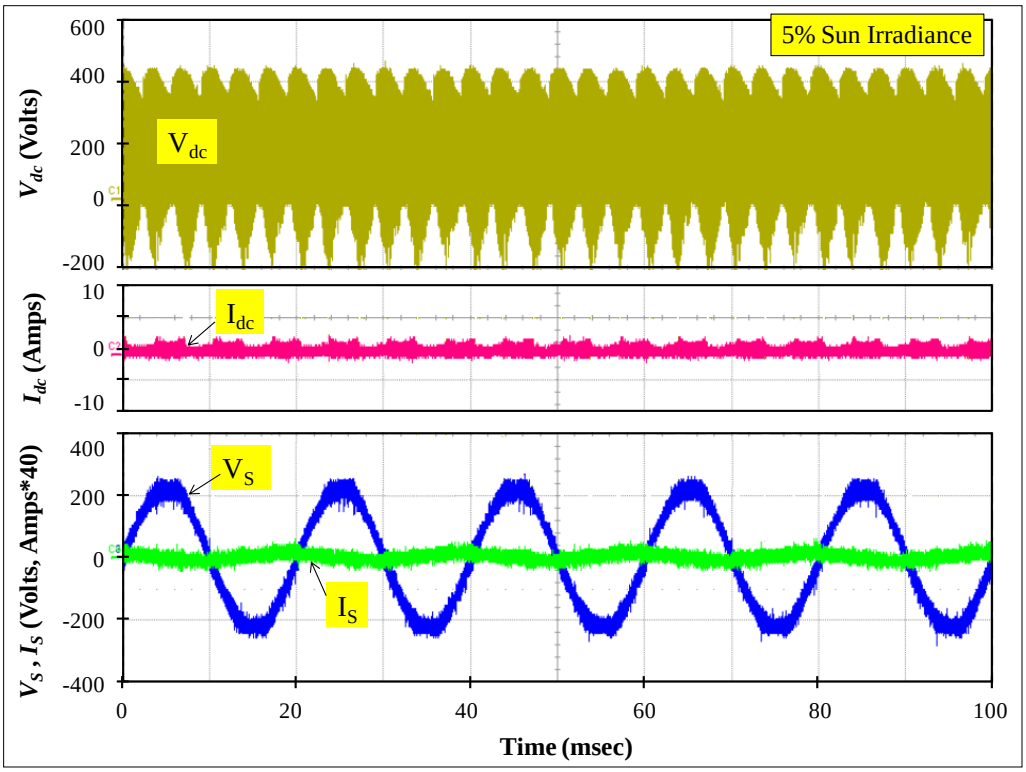
Figure 8.16 Experimental results of (a) the CSI topology and (b) the CSI+SCaps topology operating under 70% sun irradiance and PV current steps from 0.5A to 1.5A at time=100msec, 1.5A to 3.0A at time=200msec, 3.0A to 1.5A at time=300msec and 1.5A to 0.5A at time=400msec

8.2.2.3 Steady State Results at Different Sun Irradiance Levels

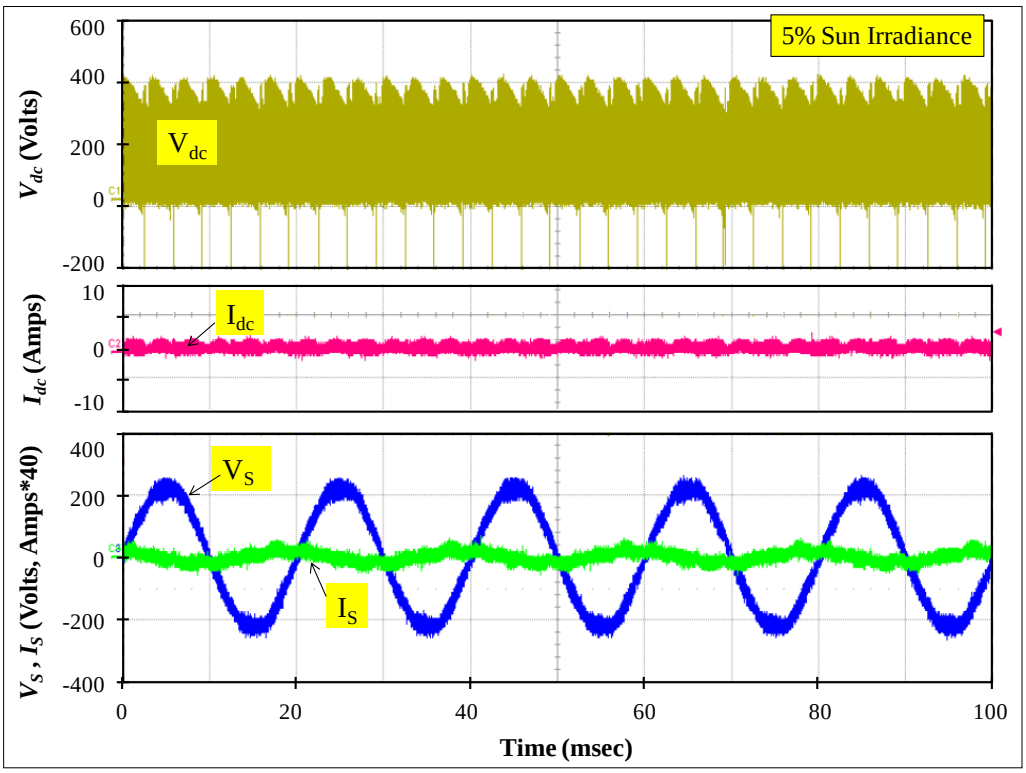
Performance of the CSI+SCaps topology when operating under constant sun irradiance has been evaluated in Sections 8.2.2.1 and 8.2.2.2. This section presents the performance of the CSI+SCaps topology in comparison to the standard CSI topology when operating under different sun irradiance levels. Steady state operation of the topologies at the MPP for each sun irradiance level is tested. Figures 8.17 to 8.21 show the experimental results at the MPP under 5%, 10%, 20%, 30% and 50% sun irradiance. The frequency spectrums of the supply current waveforms from Figures 8.17 to 8.21 are shown in Figures 8.22 to 8.26. The measured magnitudes of the waveforms in Figures 8.17 to 8.21 and Figures 8.22 to 8.26 are summarised in Table 8.2.

Inverter Topology	Measured Parameter	Sun Irradiance Level					Unit
		5%	10%	20%	30%	50%	
Standard CSI	$V_{dc\ (average)}$	203.8	209.9	217.6	232.1	236	V
	$I_{dc\ (average)}$	0.702	1.1	1.85	2.42	3.52	A
	$P_{dc\ (average)}$	143	231	403	562	831	W
	$V_{dc\ (peak)}$	443	449	449	449	468	V
	$I_{dc\ (peak)}$	3.1	4.1	5.7	6.6	7.6	A
	$\Delta I_{dc\text{-}ripple\ (peak\text{-}peak)}$	4.41	5.31	6.88	7.5	7.19	A
	$V_{S\ (rms)}$	160.8	162	161.6	161.7	163.1	V
	$I_{S\ (rms)}$	0.696	0.855	1.11	1.33	1.8	A
	Power Factor	0.42	0.48	0.67	0.8	0.92	-
	$I_{S\ (fundamental)}$	0.61	0.74	1.08	1.51	2.26	A
	$I_{S\ (THD)}$	18.9	19.4	23.6	21.5	18.6	%
CSI+SCaps	$V_{dc\ (average)}$	204	215	220	234	236	V
	$I_{dc\ (average)}$	0.76	1.08	1.82	2.4	3.56	A
	$P_{dc\ (average)}$	155	232	400	562	840	W
	$V_{dc\ (peak)}$	405	393	386	386	380	V
	$I_{dc\ (peak)}$	3.2	3.2	4.1	4.8	6.0	A
	$\Delta I_{dc\text{-}ripple\ (peak\text{-}peak)}$	4.38	4.38	4.69	4.69	4.38	A
	$V_{S\ (rms)}$	160	160	161	163	163	V
	$I_{S\ (rms)}$	0.86	1.07	1.4	1.72	2.32	A
	Power Factor	0.33	0.42	0.56	0.64	0.715	-
	$I_{S\ (fundamental)}$	0.97	1.26	1.79	2.30	3.18	A
	$I_{S\ (THD)}$	27.3	23.8	16.8	11.3	7.2	%

Table 8.2 Measured magnitudes of the waveforms in Figures 8.17 to 8.26

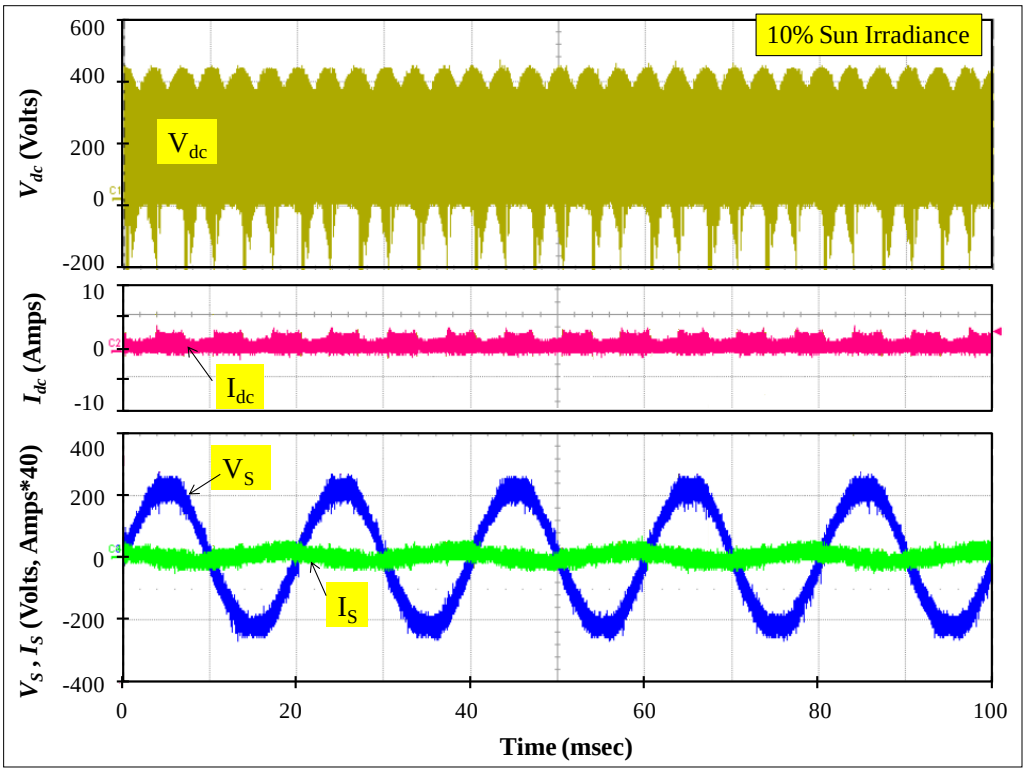


(a) Standard CSI

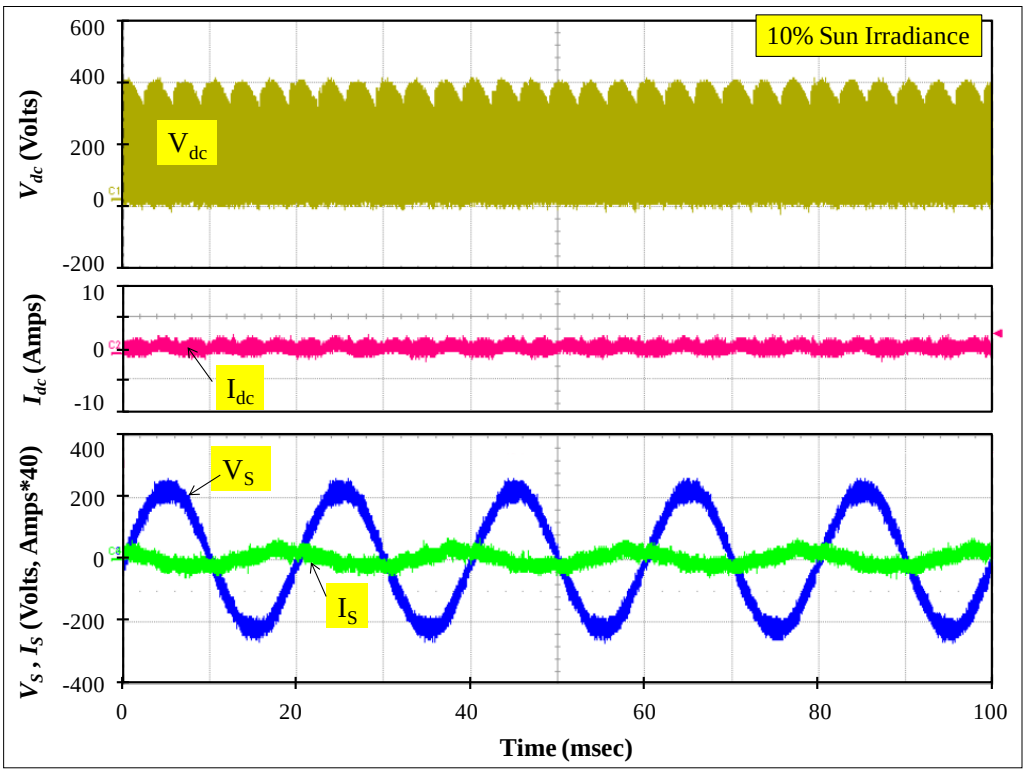


(b) CSI+SCaps

Figure 8.17 Experimental results of (a) the standard CSI topology and (b) the CSI+SCaps topology operating at the MPP under 5% sun irradiance

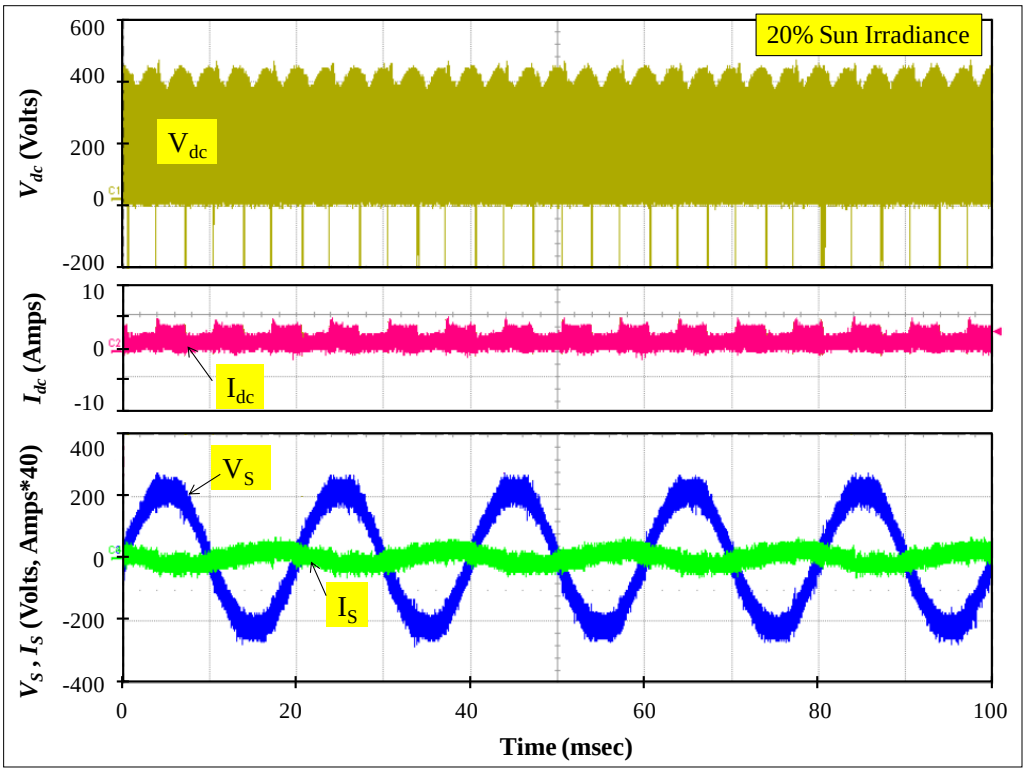


(a) Standard CSI

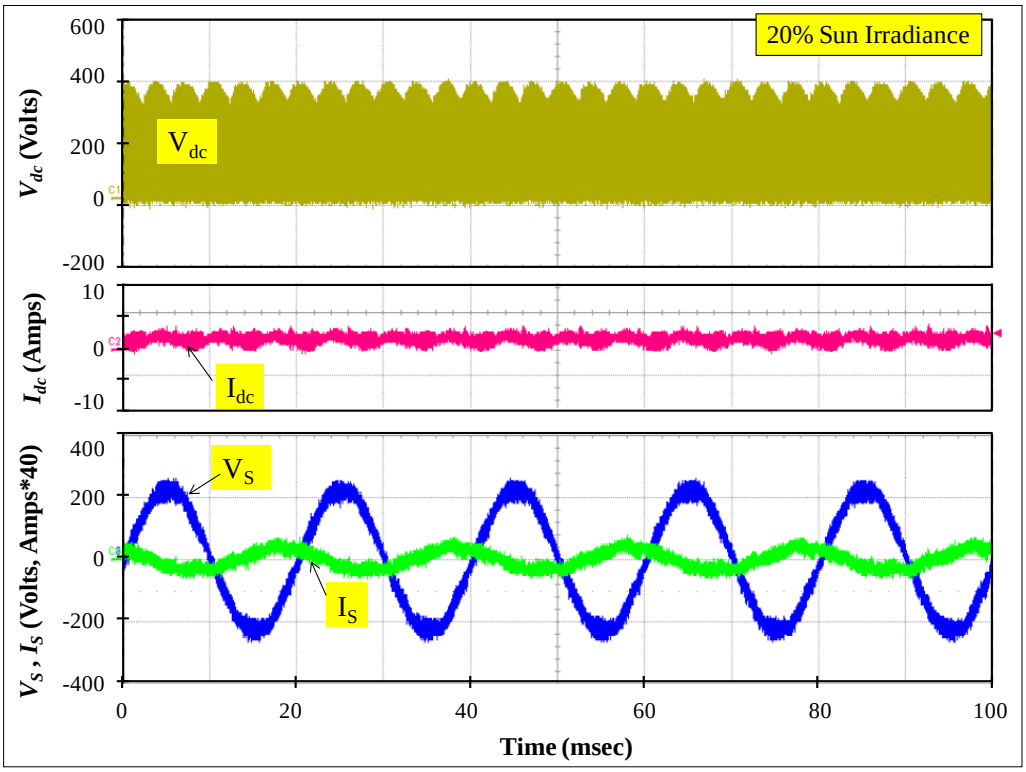


(b) CSI+SCaps

Figure 8.18 Experimental results of (a) the standard CSI topology and (b) the CSI+SCaps topology operating at the MPP under 10% sun irradiance

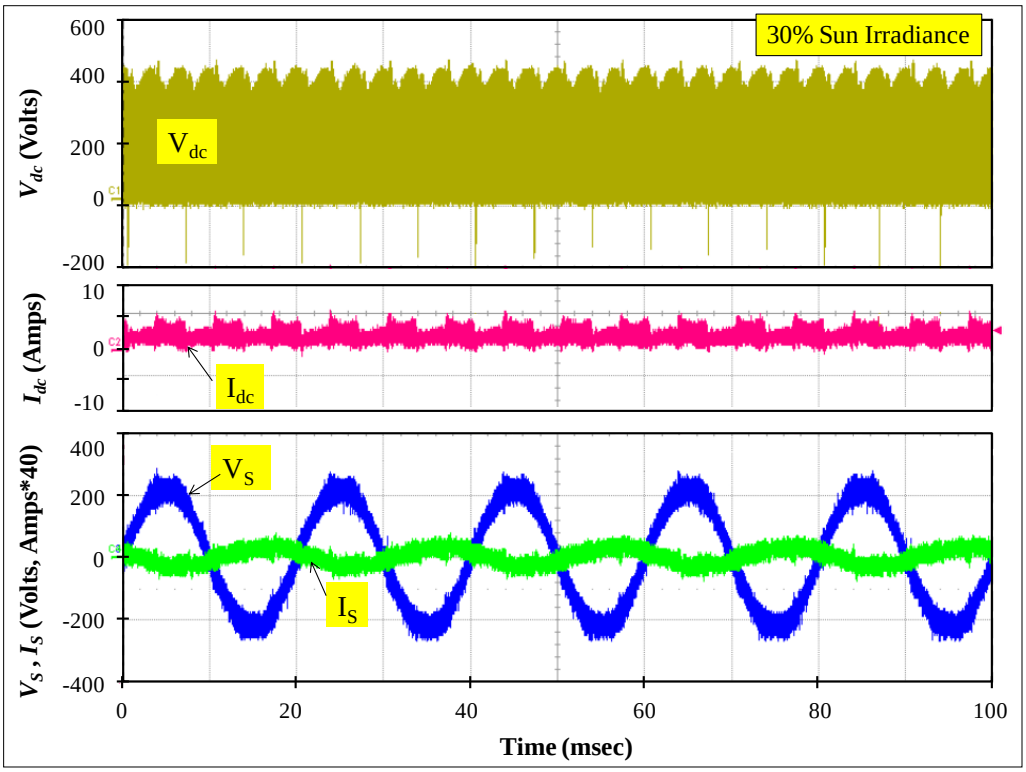


(a) Standard CSI

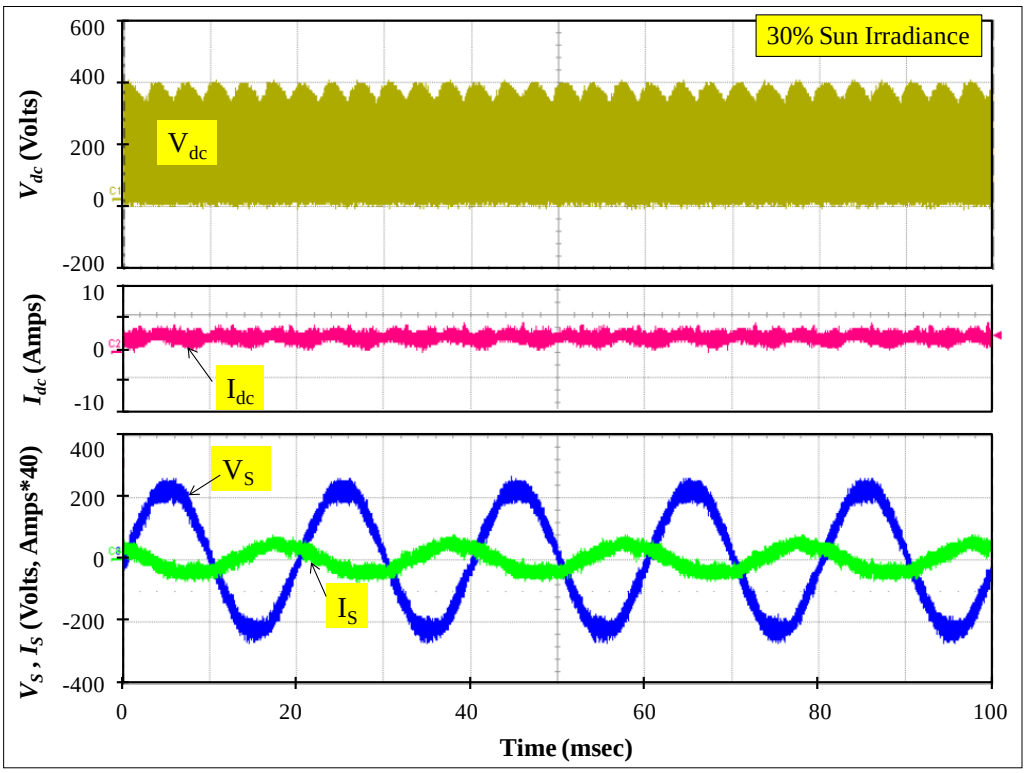


(b) CSI+SCaps

Figure 8.19 Experimental results of (a) the standard CSI topology and (b) the CSI+SCaps topology operating at the MPP under 20% sun irradiance

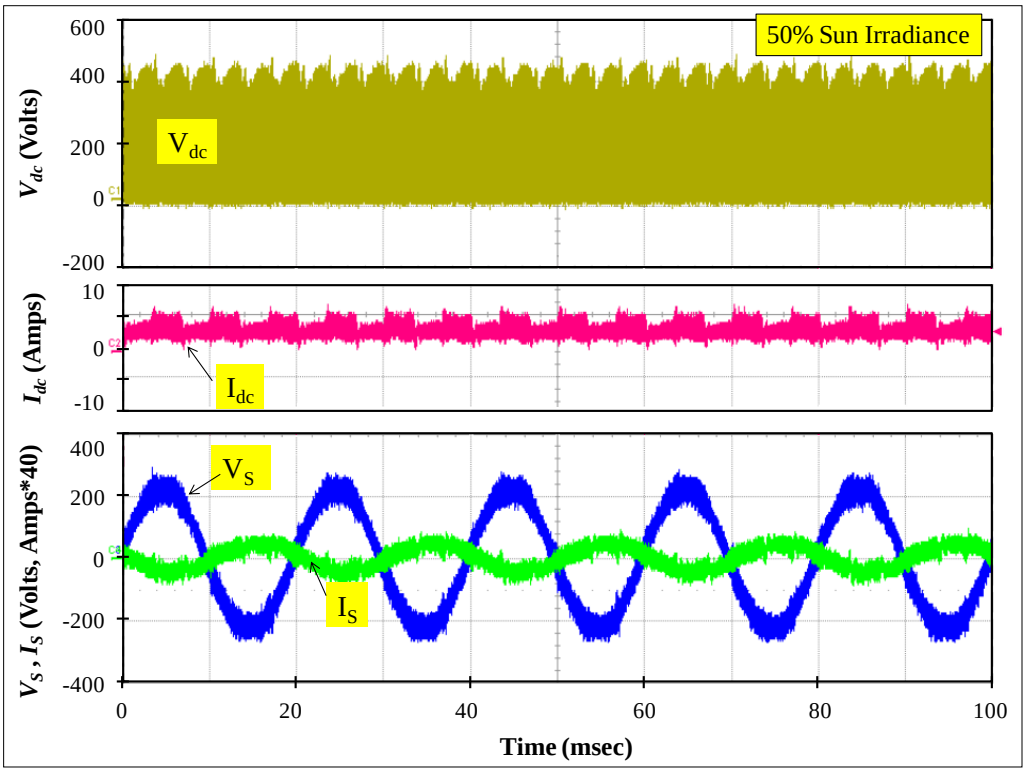


(a) Standard CSI

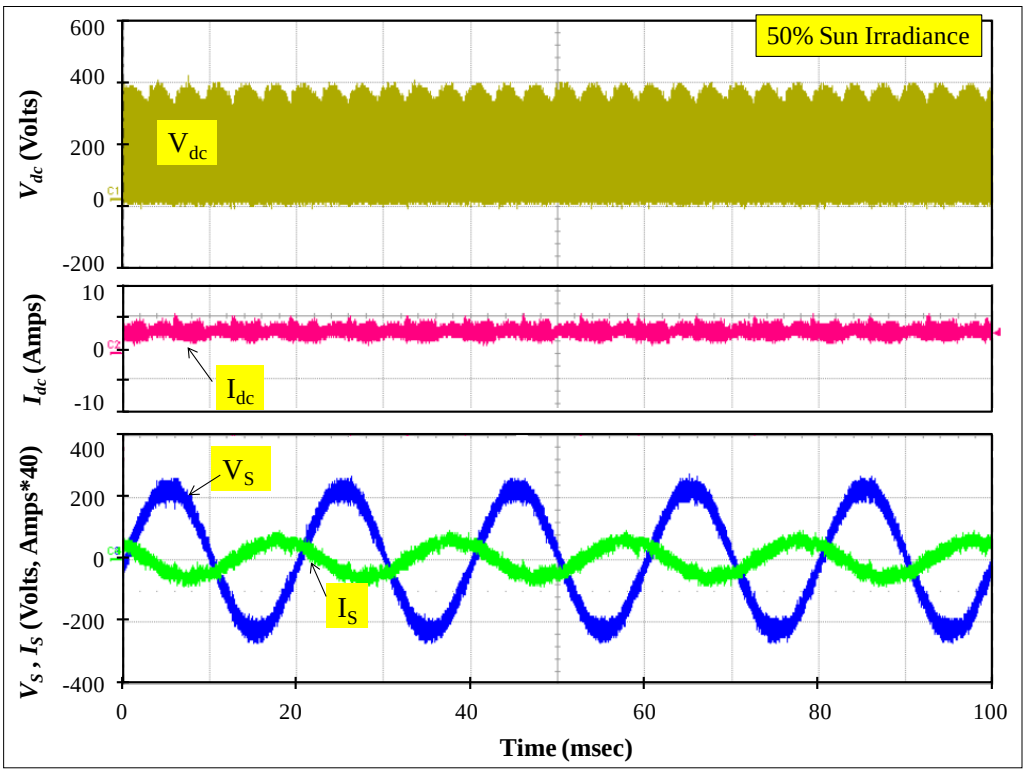


(b) CSI+SCaps

Figure 8.20 Experimental results of (a) the standard CSI topology and (b) the CSI+SCaps topology operating at the MPP under 30% sun irradiance

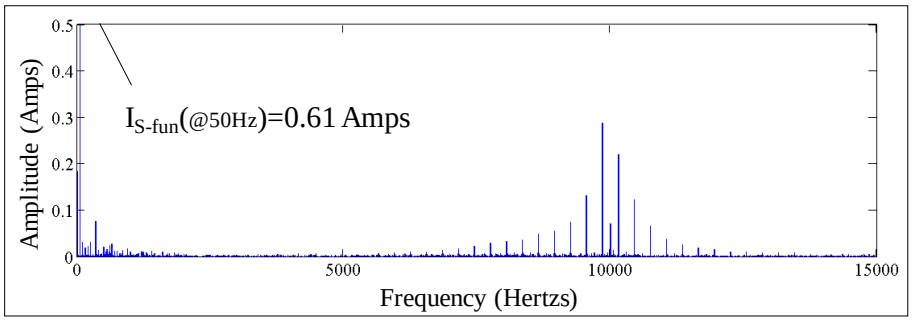


(a) Standard CSI

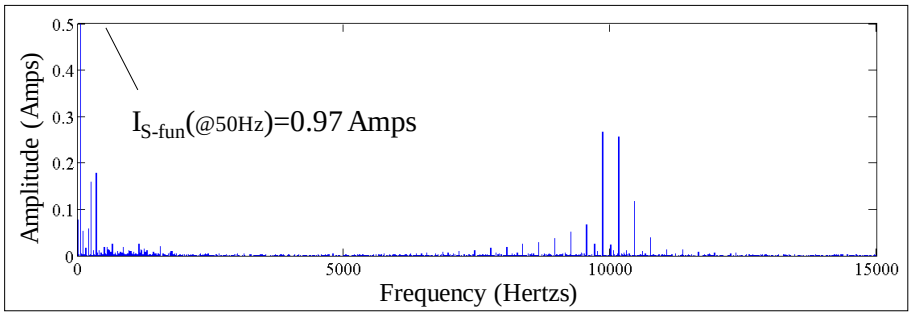


(b) CSI+SCaps

Figure 8.21 Experimental results of (a) the standard CSI topology and (b) the CSI+SCaps topology operating at the MPP under 50% sun irradiance

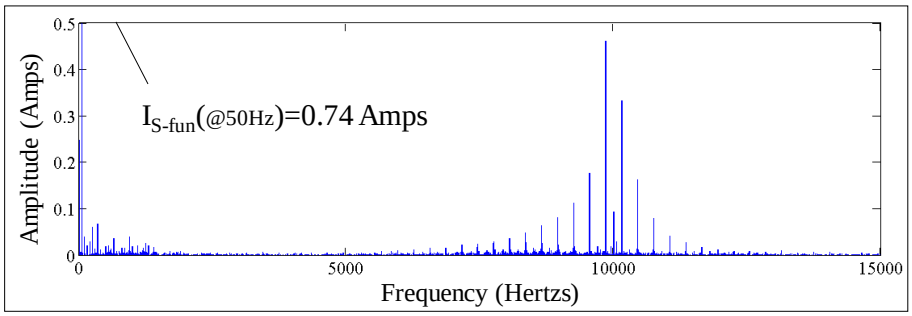


(a) Standard CSI

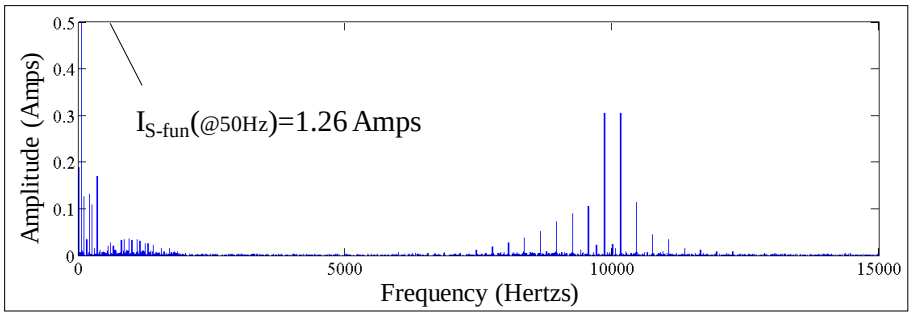


(b) CSI+SCaps

Figure 8.22 Frequency spectrum of the supply current (I_S) waveform in Figure 8.17

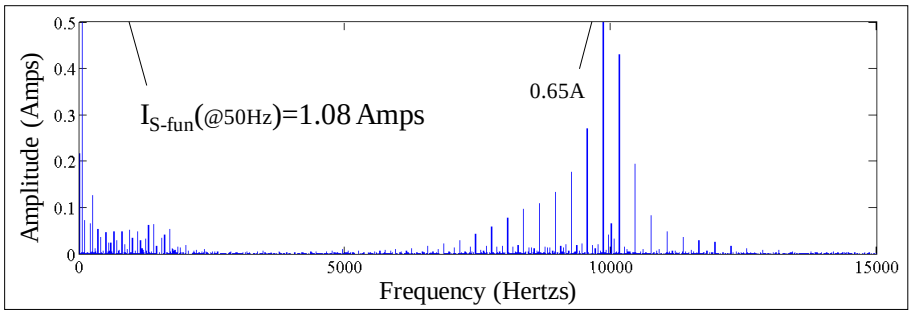


(a) Standard CSI

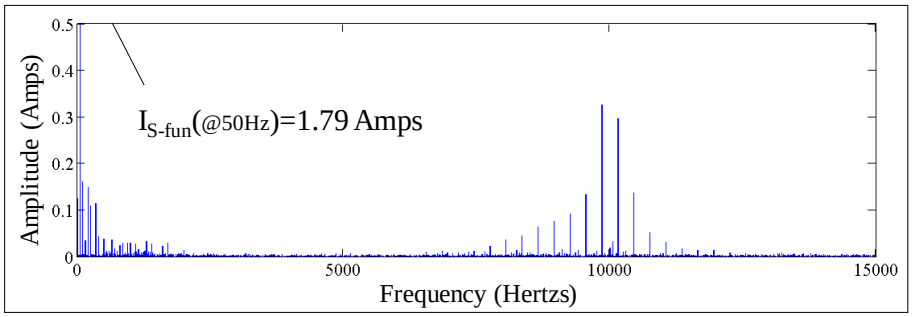


(b) CSI+SCaps

Figure 8.23 Frequency spectrum of the supply current (I_S) waveform in Figure 8.18

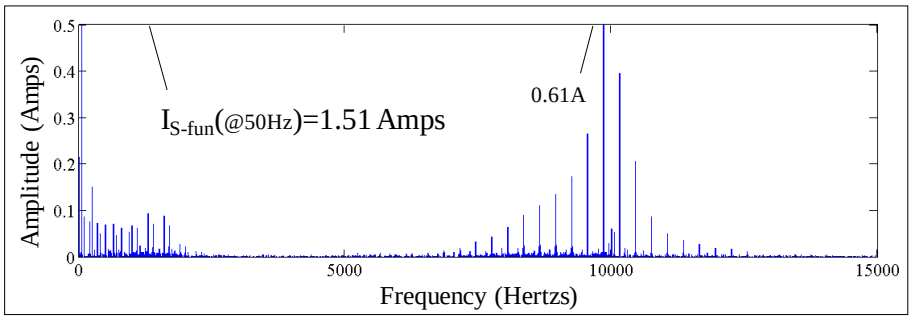


(a) Standard CSI

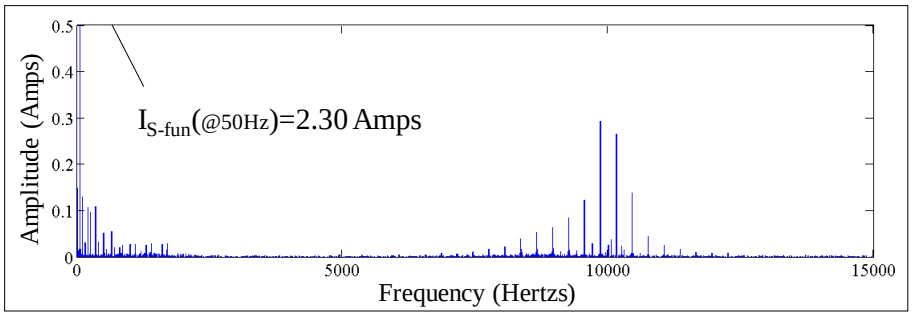


(b) CSI+SCaps

Figure 8.24 Frequency spectrum of the supply current (I_S) waveform in Figure 8.19

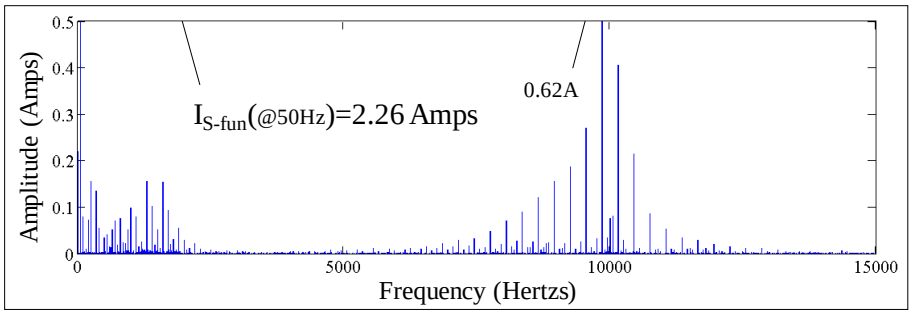


(a) Standard CSI

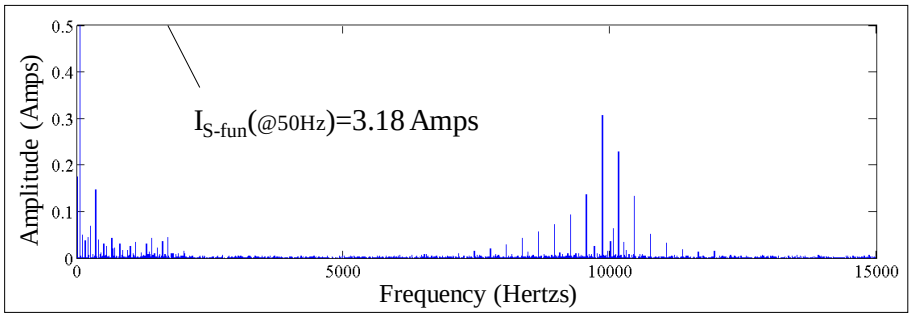


(b) CSI+SCaps

Figure 8.25 Frequency spectrum of the supply current (I_S) waveform in Figure 8.20



(a) Standard CSI



(b) CSI+SCaps

Figure 8.26 Frequency spectrum of the supply current (I_S) waveform in Figure 8.21

It can be seen from Table 8.2 and Figures 8.17 to 8.26 that:

- The average input voltage (V_{dc}), current (I_{dc}) and power (P_{dc}) are similar for the CSI+SCaps topology and the standard CSI topology. Table 8.2 confirms that both topologies operate at similar PV points. Thus, the experimental results obtained from them both can be directly compared and evaluated.

- Both the CSI+SCaps topology and the CSI topology can provide sinusoidal output AC current waveforms for all of the operating points as shown in Figures 8.17 to 8.21.

- The CSI+SCaps topology has a lower peak input DC-link voltage (380-405V) than the standard CSI topology (443-468V) for all the operating points. This leads to lower voltage stress on the circuit devices for the CSI+SCaps topology compared to the CSI topology. Moreover, when the operating power increases (increase in sun irradiance), the CSI+SCaps topology provides a lower peak DC-link voltage than the standard CSI topology.

- The CSI+SCaps topology has a lower peak input DC-link current (3.2-6A) than the standard CSI topology (3.1-7.6A) for all of the operating points. This means that the CSI+SCaps topology has lower current stress on the circuit devices when compared to the CSI topology. Peak DC-link current for both of the topologies increases as sun irradiance increases.

- The CSI+SCaps topology has lower input current ripple (4.38-4.69A_{pk-pk}) than the standard CSI (4.41-7.5A_{pk-pk}) for all of the operating points. This means that the CSI+SCaps provides better input power quality than the standard CSI and hence a smaller DC filter inductor can also be used for the CSI+SCaps. Both of the topologies have higher input current ripple at higher sun irradiance levels.

- The CSI+SCaps topology has a better supply current THD than the standard CSI when the sun irradiance is greater than 20% and achieve the minimum THD of 7.2% (compared to 18.6% for the standard CSI) at 50% sun irradiance. At very low sun irradiance (i.e. 5%) the THD of the CSI+SCaps topology (27.3%) is higher than the standard CSI (18.9%). Based on sun irradiance profiles in the central Europe, 91% of total solar energy comes from sun irradiance over 20% [23]. This means that the CSI+SCaps topology would provide better output power quality than the standard CSI topology for most of the time.

- The CSI+SCaps topology produces a higher output supply current (0.97-3.18A) than the standard CSI (0.61-2.26A). The CSI+SCaps also produces a lower output power factor (0.33-0.72) than the standard CSI (0.42-0.92). This would lead to higher AC side current stress for the CSI+SCaps topology, which may require larger wires and higher current rating equipment for transmission system. The power factor will be improved when both of the topologies operate at higher power (sun irradiance increases).

The experimental results show several improved features compared to the standard CSI topology which can be achieved using the CSI+SCaps topology. These are the lower voltage and current stress on the circuit devices with lower peak DC-link voltage and lower peak DC-link current; better input power quality with lower input current ripple and the better output power quality with lower supply current THD.

8.2.3 Performance during Low Voltage Grid Faults

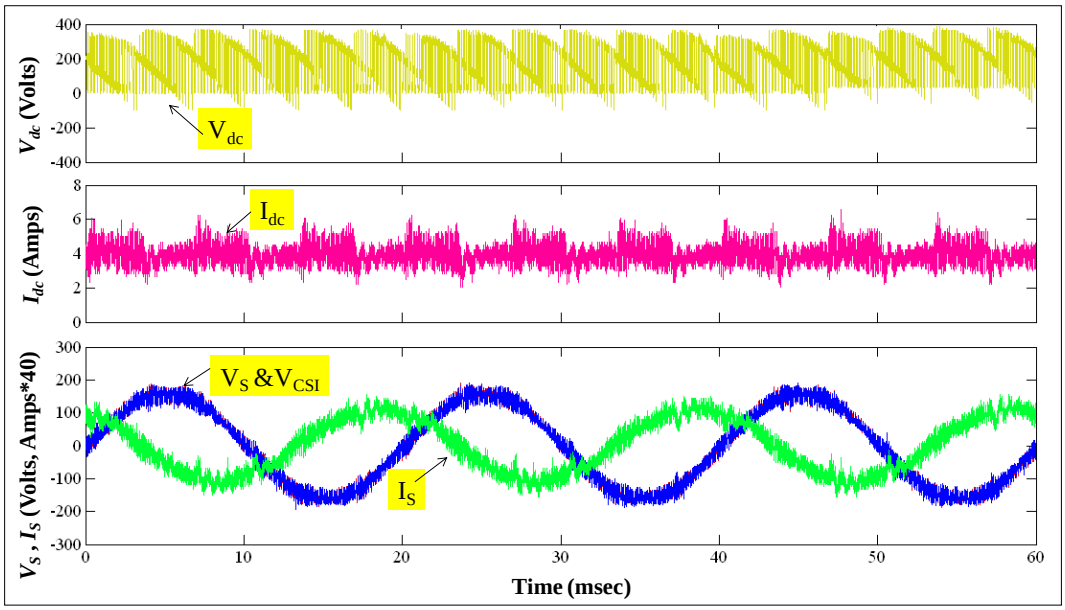
As specified by the grid codes in Section 3.2.2, grid-tied PV inverters must be able to ride-through low grid voltage faults by stay-connecting to the grid without tripping when the faults occur; supporting the grid with a reactive current during the faults and supplying power into the grid immediately after the fault clearance (details in Section 3.2.2). In this section the experimental results for the CSI+SCaps topology in comparison to the standard CSI topology when operating during low grid voltage faults are presented. The steady state and dynamic response are presented.

8.2.3.1 Steady State Results

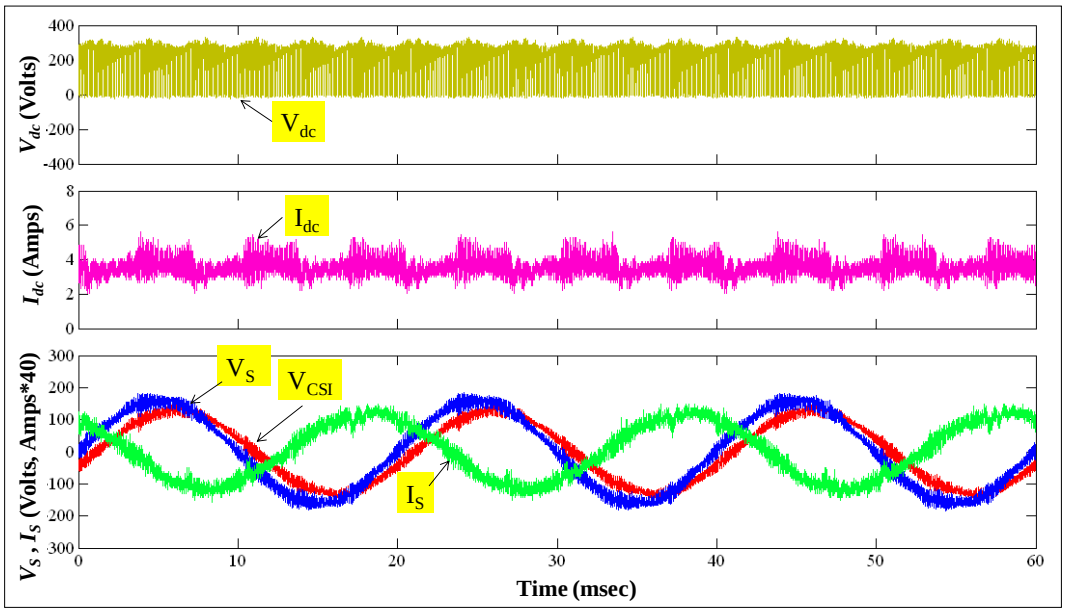
Figures 8.27 and 8.28 show the experimental results when the CSI+SCaps and the standard CSI topology operate during 30% and 70% grid voltage dips under 50% sun irradiance. The frequency spectrum of the supply current waveforms from Figures 8.27 and 8.28 are shown in Figures 8.29 and 8.30. The measured values of the waveforms in Figures 8.27, 8.28, 8.29 and 8.30 are summarised in Table 8.3.

Measured Parameter		**30% Grid Voltage Dip**		**70% Grid Voltage Dip**	
		Standard CSI	CSI+SCaps	Standard CSI	CSI+SCaps
DC Side	$\mathbf{V_{dc\ (peak)}}$	412V	331V	223V	219V
	$\mathbf{V_{dc\ (average)}}$	122V	128V	2V	3V
	$\mathbf{I_{dc\ (peak)}}$	6.9A	6.1A	5.5A	5.4A
	$\mathbf{I_{dc\ (average)}}$	3.8A	3.6A	4.0A	3.8A
	$\mathbf{\Delta I_{dc\text{-}ripple(peak\text{-}peak)}}$	4.1A	3.2A	2.5A	2.7A
	$\mathbf{P_{dc\ (average)}}$	464W	461W	14W	11W
AC Side	$\mathbf{V_{S\ (rms)}}$	114V	114V	49V	50V
	$\mathbf{V_{CSI\ (rms)}}$	115V	108V	51V	52V
	$\mathbf{I_{S\ (rms)}}$	2.0A	2.1A	2.2A	2.1A
	Power Factor	0.52	0.49	<0.1	<0.1
	$\mathbf{I_{S\ (fundamental)}}$	2.83A	3.0A	3.1A	3.0A
	$\mathbf{I_{S\ (THD)}}$	11.9%	12.8%	8.8%	7.6%

Table 8.3 Measured values from the waveforms in Figures 8.27 to 8.30

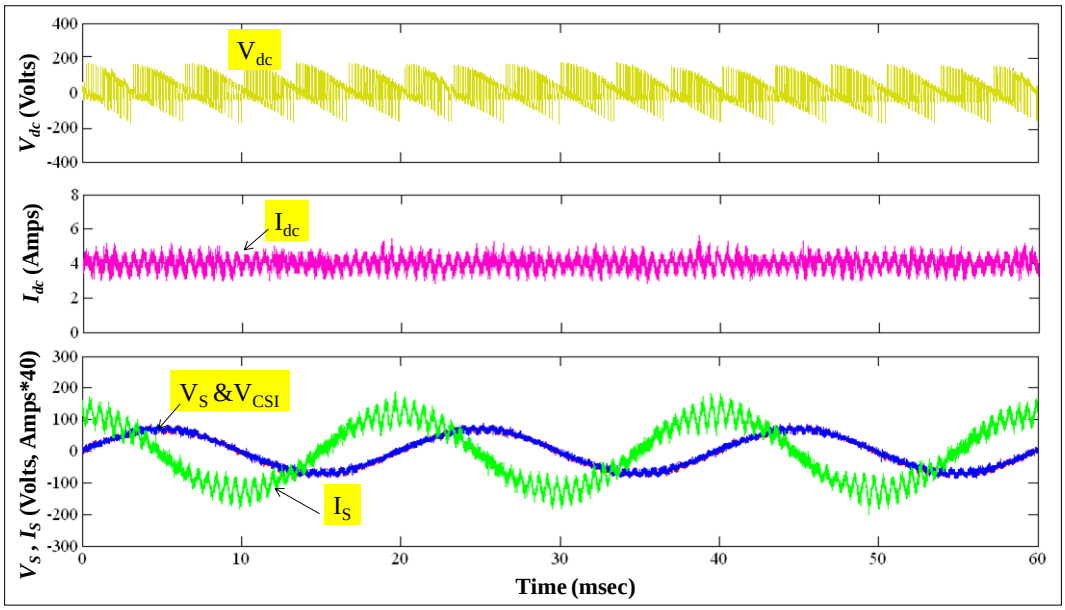


(a) Standard CSI

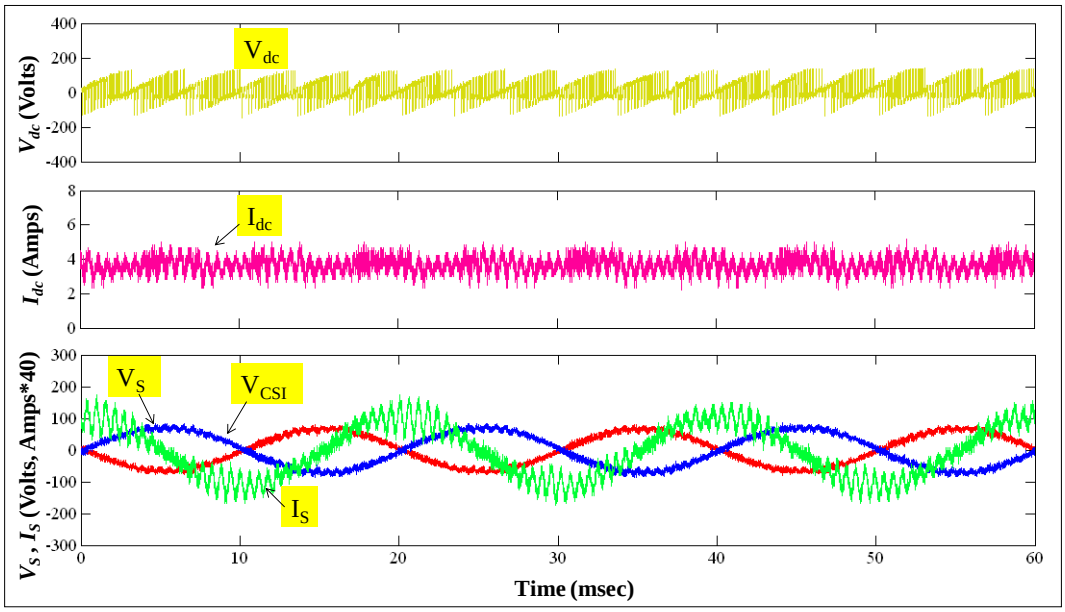


(b) CSI+SCaps

Figure 8.27 Experimental results of (a) the CSI topology and (b) the CSI+SCaps topology operating at 30% grid voltage dip

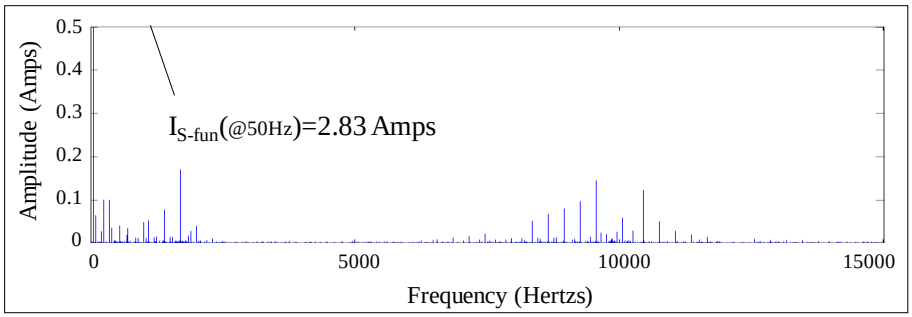


(a) Standard CSI

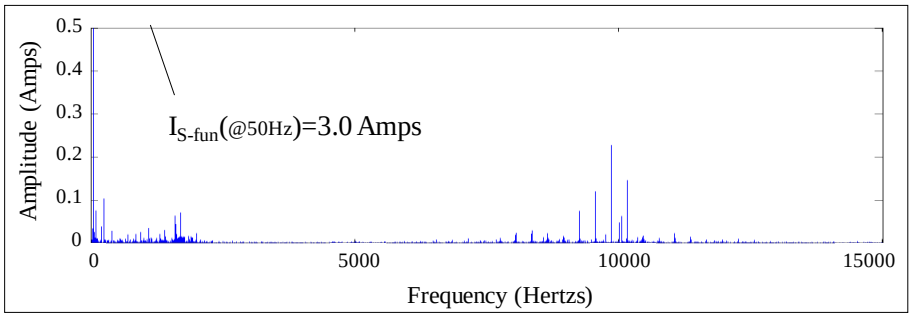


(b) CSI+SCaps

Figure 8.28 Experimental results of (a) the CSI topology and (b) the CSI+SCaps topology operating at 70% grid voltage dip

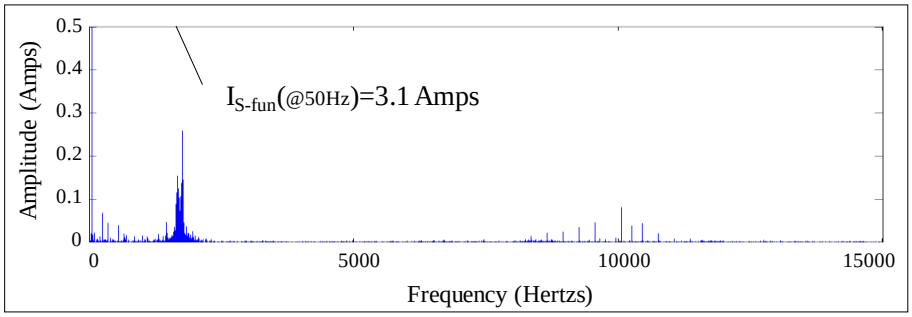


(a) Standard CSI

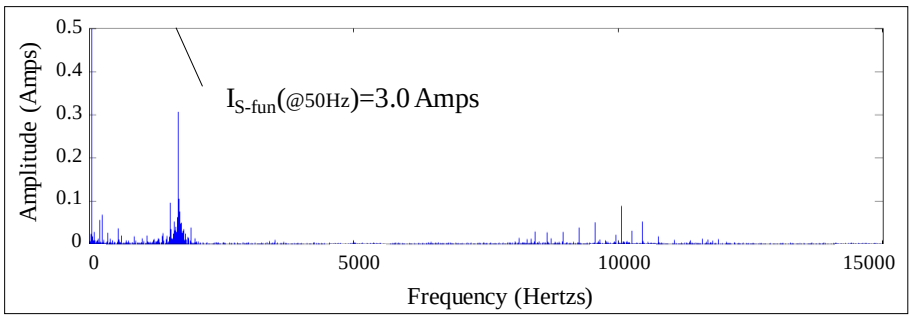


(b) CSI+SCaps

Figure 8.29 Frequency spectrum of the supply current (*Is*) waveform in Figure 8.27



(a) Standard CSI



(b) CSI+SCaps

Figure 8.30 Frequency spectrum of the supply current (*Is*) waveform in Figure 8.28

It can be seen from Table 8.3 and Figures 8.27 and 8.30 that:

- The Experimental waveforms in Figures 8.27 and 8.28 support the results shown in Section 5.5.2 and simulation results in Figures 5.18 and 5.19. The CSI+SCaps topology and the standard CSI topology can ride through in both cases of grid voltage faults.

- During the 30% grid voltage dip (Figure 8.27) both of the topologies operate with slightly higher input current (3.6-3.8A compared to the rated value of 3.2A) but a much reduced input voltage (122-128V compared to the rated value of 246-248V). Both topologies inject similar amount of reactive current to support the grid (48-51%) which is reflected in the low power factor (0.49-0.51). Under these conditions the CSI+SCaps topology still provides lower AC side voltage and peak DC-link voltage as well as lower input current ripple than the CSI topology.

- During the 70% grid voltage dip (Figure 8.28) the CSI+SCaps topology and the standard CSI topology operate near the short-circuit PV source with a short-circuit current of 3.8-4A. Very little active power (11-14W) is produced from the PV source. Full reactive current (≈100%) can be observed at the grid connection for both of the topologies. The CSI+SCaps and the standard CSI have similar input and output waveforms at this operating point.

- The CSI+SCaps topology provides similar levels of the THD to the standard CSI topology for both the cases of 30% grid voltage dip (7.6-8.8%) and 70% grid voltage dip (11.9%-12.8%).

8.2.3.2 Dynamic Results

Figures 8.31 and 8.32 show the simulation results for the CSI+SCaps topology and the standard CSI topology riding through a low grid voltage fault profile as required by the E.On Netz grid code (Section 3.2.2). Figures 8.33 and 8.34 show the simulation results when the topologies ride through low voltage fault of 30% and 70% of the nominal level. Constant sun irradiance of 50% is considered for these tests.

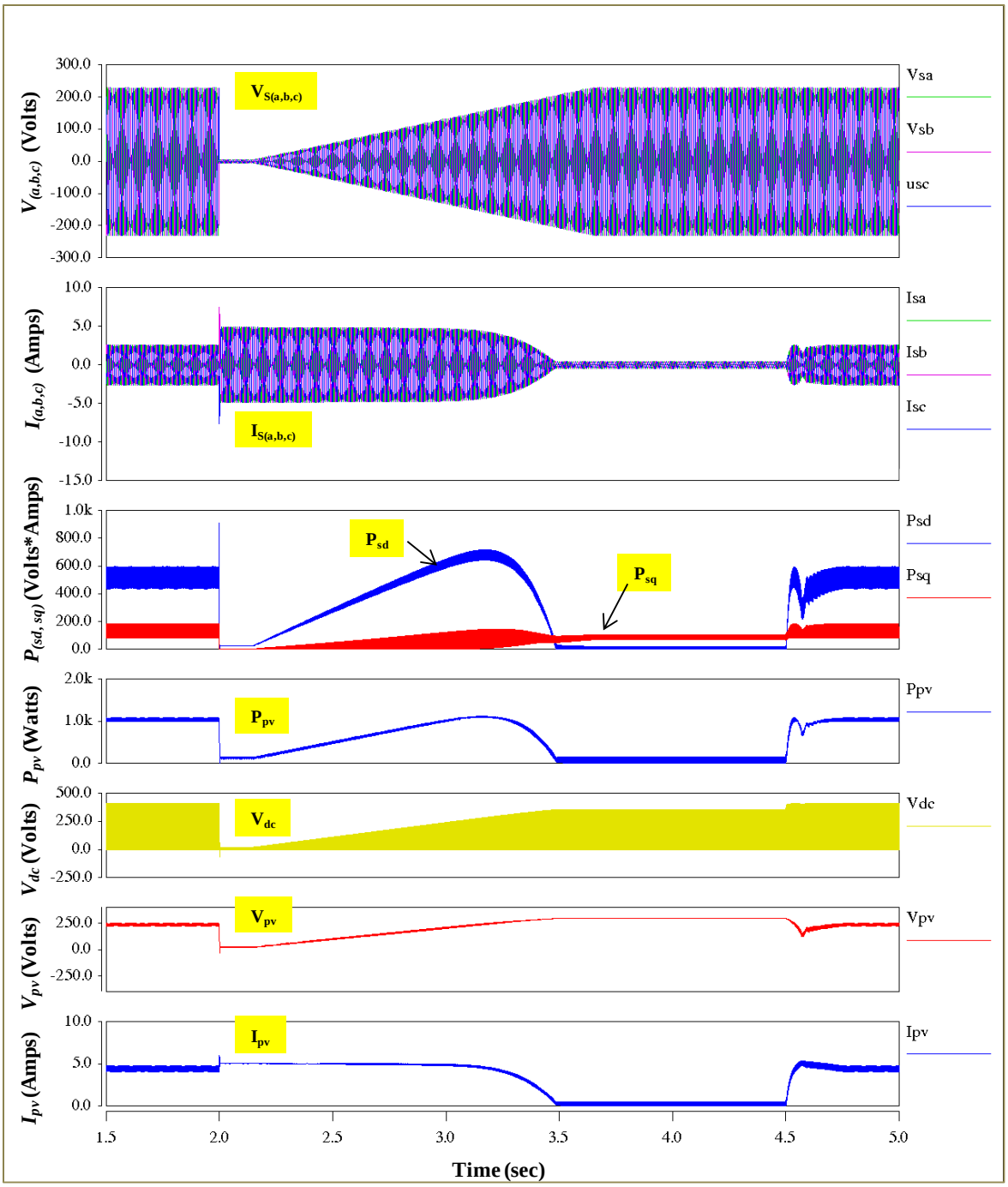


Figure 8.31 Simulation results of the Standard CSI topology when riding through a low voltage fault profile as required by E.On Netz grid code; a fault occurs at time=2.0sec and disappear at time=3.65sec

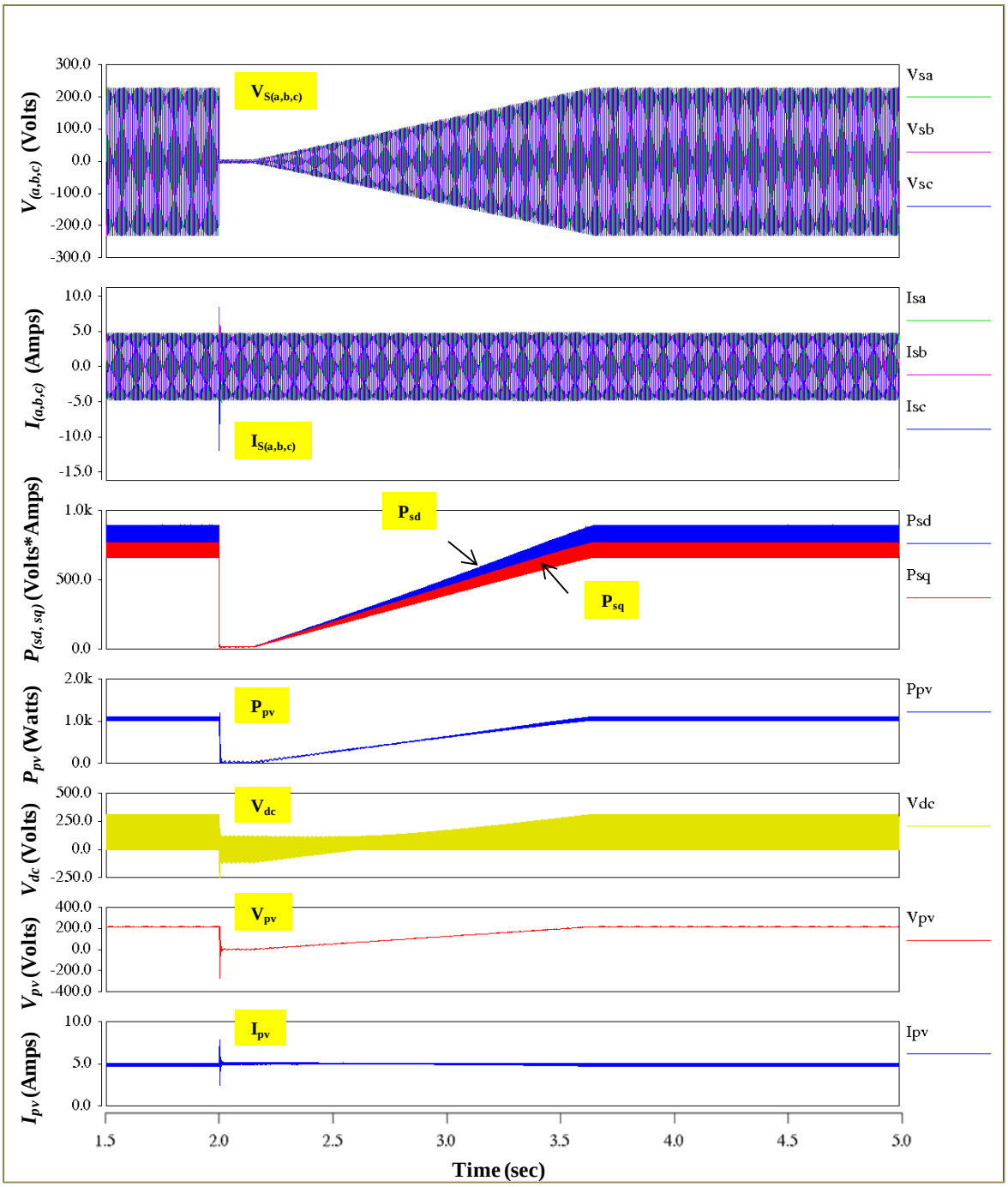


Figure 8.32 Simulation results of the CSI+SCaps topology when riding through a low voltage fault profile as required by E.On Netz grid code; a fault occurs at time=2.0sec and disappear at time=3.65sec

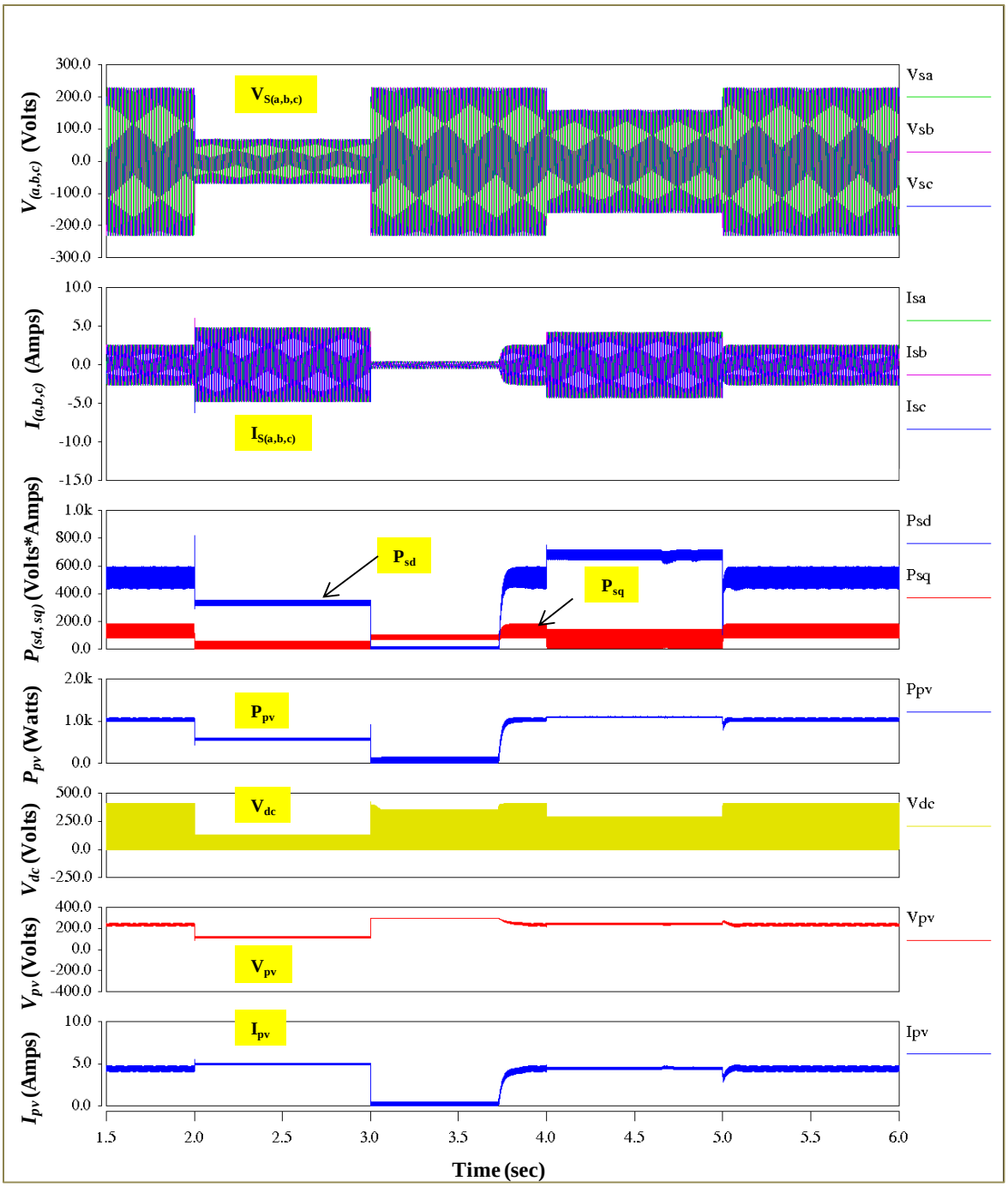


Figure 8.33 Simulation results of the standard CSI topology when riding through a low voltage fault of 70% from its nominal level at time=1.0sec and then returns to its nominal at time=2.0sec and dips again by 30% at time=3.0sec and then returns to the nominal level at time=4.0sec

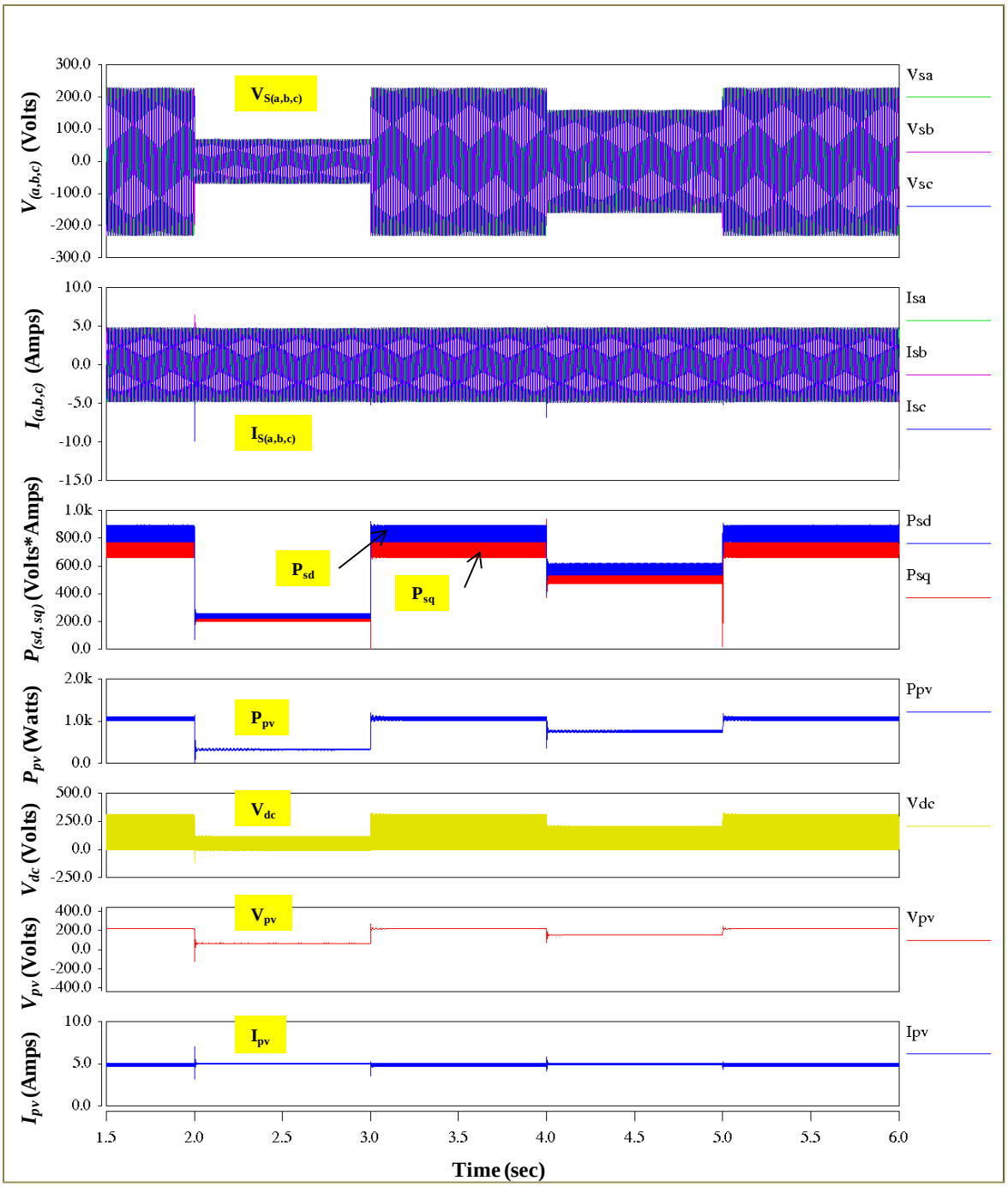


Figure 8.34 Simulation results of the CSI+SCaps topology when riding through a low voltage fault of 70% from its nominal level at time=1.0sec and then returns to its nominal at time=2.0sec and dips again by 30% at time=3.0sec and then returns to the nominal level at time=4.0sec

From Figures 8.31 and 8.32 it can be seen that:

- Both the standard CSI topology and the CSI+SCaps topology can ride through the low voltage profile of the E.On Netz grid code but with slightly different dynamic responses.

- When a fault occurs, the CSI+SCaps topology can maintain constant supply current amplitude (I_S) at the rated value and can support the grid with reactive current. In contrast the standard CSI topology cannot maintain constant supply current amplitude. In fact, the standard CSI topology supplies current which varies in amplitude depending on the available DC current at the DC side. The standard CSI topology can also produce only a small amount of reactive current to support the grid compared to the CSI+SCaps topology.

- The CSI+SCaps can immediately supply full active power (P_{sd}) into the grid after fault clearance, but the standard CSI topology requires a longer time (of almost 1sec in this example) to stabilise the fault and to search for a new maximum power point before full active power is supplied into the grid.

Figures 8.33 and 8.34 show a more realistic situation of short-time grid voltage dips of 70% and 30% from the nominal level which occur at time=2sec and time=4 sec for 1 sec. It can be seen from these figures that:

- Both the standard CSI topology and the CSI+SCaps topology can maintain their stable operation during the fault and after the fault clearance. However, the CSI+SCaps can return to operate at the nominal MPP point after the fault clearance more quickly than the standard CSI topology. This is because the CSI+SCaps topology can operate at rated current during the fault.

- The CSI+SCaps topology provides lower peak DC-link voltage and lower input current ripple than the standard CSI topology for all operating points.

8.2.4 Inverter Efficiency

In this section power conversion efficiency of the CSI+SCaps topology based on European Efficiency calculation (see Section 3.3.1) is experimentally evaluated and compared to the standard CSI topology. In order to calculate European efficiency of these inverters, individual efficiencies for the inverters operating at the MPP under 5%, 10%, 20%, 30%, 50% and 100% sun irradiance levels are tested. These tests are achieved using two power analysers; one to measure the input power (P_{in}) from the PV emulator and the other to measure the output power (P_{out}) at the grid side. The European Efficiency of the inverters can then be determined by using (8.1) and (8.2).

$$\eta_x = \frac{P_{out,x}}{P_{in,x}} \times 100\% \qquad ; x = 5\%, 10\%, 20\%, 30\% \text{ and } 50\% \tag{8.1}$$

$$\eta_{euro} = 0.0375\eta_{5\%} + 0.075\eta_{10\%} + 0.1625\eta_{20\%} + 0.125\eta_{30\%} + 0.6\eta_{50\%} \tag{8.2}$$

The measured values obtained from the power analysers when testing both of the topologies at the MPP nominal grid voltage under 5%, 10%, 20%, 30% and 50% sun irradiance are summarised as shown in Table 8.4.

Inverter Topology	Sun Irradiance Level	V_{in} (V)	I_{in} (A)	P_{in} (W)	P_{out} (W)		
					Data 1	Data 2	Data 3
Standard CSI	5%	208.03	0.85	139.35	89.19	88.47	88.98
	10%	224.65	1.24	229.71	154.35	152.88	153.42
	20%	233.40	1.96	410.64	303.93	299.07	298.86
	30%	240.37	2.41	540.88	425.01	419.19	419.46
	50%	246.57	3.82	918	766.80	763.64	765.36
CSI+SCaps	5%	207.62	0.80	135.89	102.03	102.12	99.69
	10%	224.60	1.15	228.41	183.57	183.18	179.19
	20%	234.51	1.84	410.44	355.50	354.48	351.03
	30%	241.65	2.30	541.3	480.36	480.90	478.35
	50%	245.28	3.76	914.43	819.03	821.19	818.79

Table 8.4 Measured values obtained from the power analysers when the standard CSI topology and the CSI+SCaps topology when operating at the MPP nominal grid voltage at 5%, 10%, 20%, 30% and 50% sun irradiance

By using the information in Table 8.4 and equations (8.1) and (8.2), the European Efficiency (η_{euro}) for the standard CSI topology and the CSI+SCaps topology can be determined as shown in Figure 8.35.

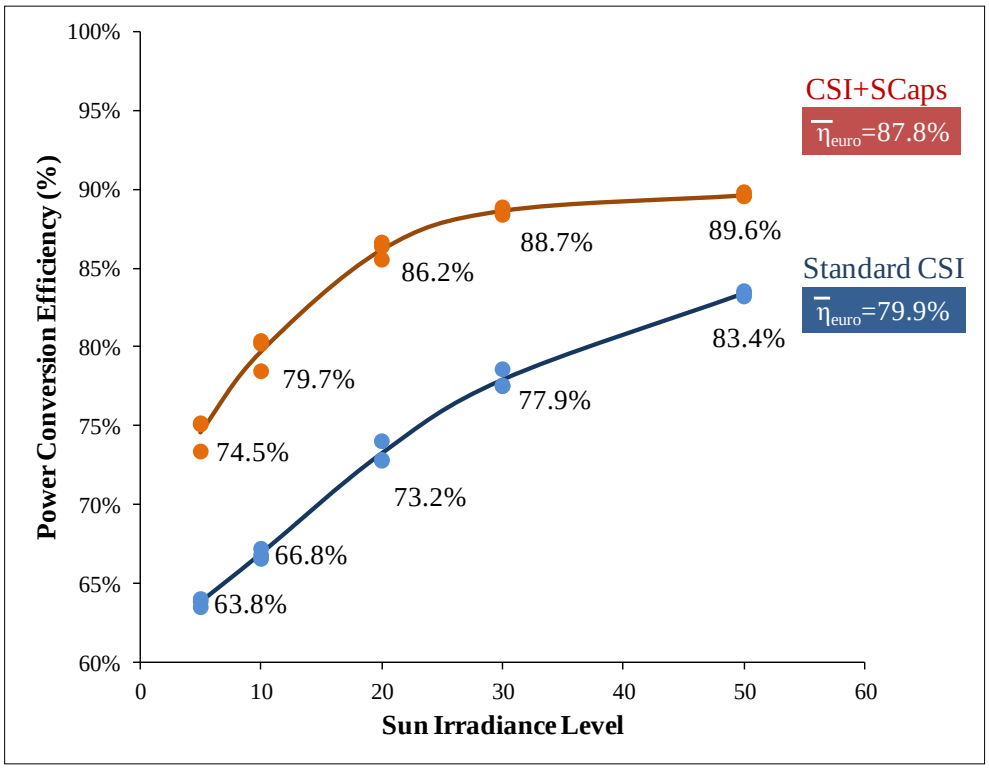


Figure 8.35 Power conversion efficiency curves and European efficiencies of the CSI+SCaps topology and the standard CSI topology

It is clearly shown in Figure 8.35 that the CSI+SCaps topology has higher power conversion efficiencies at all operating points and higher European Efficiency than a standard CSI topology. The measured efficiencies that are obtained from a particular test point show similar results with deviations less than 1.1% from the average value. This reflects to high accuracy of these results. The error in the measurement is caused by the difference in the ambient temperature during the tests which is proportional to the time that is used to collect the measured data. High ambient temperature can reduce the efficiency of heat transfer of the heatsink and also degrade the performance of the circuit components. The experimental results show similar results to the simulation results presented in Section 6.9. However, the inverter efficiencies that are obtained from the experiment are lower than the simulation because all power losses over the whole test system are measured in the experiment results but only the estimated semiconductor power losses are measured in the simulation results.

8.3 Summary

In this chapter experimental results are used to verify the functionality of the experimental test-rig and evaluate the performance of the CSI+SCaps topology in comparison to a standard CSI topology.

The results show that the experimental test-rig, which consists of the PV emulator, the CSI+SCaps inverter prototype, the interfacing and control circuits and the 3-phase electrical network, can operate properly. The PV emulator can produce similar PV characteristic curves as the designed specifications. The CSI+SCaps inverter prototype together with the interfacing and control circuits confirm the similar operating waveforms to the simulation results. The results also show that the CSI+SCaps topology can provide safe operation during start-up and shutdown, as does the standard CSI topology. However, the series AC capacitors in its circuit would lead the CSI+SCaps topology lead to a slower dynamic response compared to a standard CSI topology.

Similar results to the simulation can be observed from the experimental tests, which show that the CSI+SCaps topology provides several advantages and disadvantages compared the standard CSI topology.

The experimental results also show that both the CSI+SCaps topology and the standard CSI topology can ride through a low voltage grid fault. However, the CSI+SCaps topology can support the grid with reactive current during a fault and can inject full power into the grid immediately after the fault clearance, whilst the standard CSI can produce only a relatively small reactive current and requires longer time to recover before full power can be injected into the grid.

In addition the experimental results also show that the CSI+SCaps topology has a higher European efficiency than the standard CSI topology, which confirms similar results found by simulation in Section 6.9.

Chapter 9

Conclusions

Energy from the sun is abundant. Direct solar energy gives also several benefits such as no pollution emission, low maintenance costs and the ability to easily adjust the size of power plant and installation in remote areas. However, electricity from solar energy is currently expensive. To solve this problem, its production cost per unit power ($/W) must be reduced. One potential way to achieve this is to convert solar energy to electricity with the highest possible efficiency.

Photovoltaic (PV) cells are devices that convert sun energy to electricity. The devices require a grid-tied PV inverter to convert their electric DC power into controllable AC suitable for connection the power grid. The efficiency of a grid-tied PV inverter directly affects the overall efficiency of solar energy-to-electricity production. There are three main technologies available for the grid-tied PV inverters. Those are ones with low frequency transformers, ones with high frequency transformers and ones without transformers (transformerless). Among these technologies, the transformerless inverter potentially provides the highest efficiency due to the possibility of single-stage power conversion.

This thesis considers several topologies of transformerless grid-tied PV inverters in an effort to evaluate their efficiency and hence the ability to achieve a low cost for the electricity produced from solar energy. Six available topologies existing in today's market and currently discussed in the literature and one new candidate topology have been presented. The six available topologies are a Voltage Source Inverter (VSI), a Current Source Inverter (CSI), a VSI with a Boost converter (VSI+Boost), a CSI with a Buck converter (CSI+Buck), a Z-Source Inverter which is voltage fed (ZSI-V) and a

ZSI which is current fed (ZSI-I). The new candidate topology is a CSI with series AC capacitors (CSI+SCaps).

Before considering the characteristics of these inverters in detail, this thesis has presented fundamental knowledge of PV cells and typical characteristics for an ideal grid-tied PV inverter. This information is essential for the design of the inverter in order to achieve high efficiency, high reliability and high performance.

A summary of basic knowledge of the PV cells are as follows:

- PV cells generate nonlinear output DC power. The PV output power is dependent on the level of solar energy density (sun irradiance) and the voltage seen at the output terminals of the cells (cell voltage). PV cells generate higher output power at higher levels of sun irradiance. Under constant sun irradiance, output cell power varies with the cell voltage which has a range between zero and the maximum cell voltage (0-1pu). The cell power is zero when the cell voltage is zero (0pu) and then increases with the increase of the cell voltage in the range of 0-0.8pu. After that the cell power decreases quickly and reaches zero output again at the maximum cell voltage (1pu). The Maximum Power Point (MPP) for PV cells is in the range of 0.6-0.9pu.

- Single PV cells can be combined to form a PV module which provides higher output power with designable voltage and current ratings. In order to increase the voltage rating for a PV module by *m* times of the rating of a single PV cell, *m* PV cells are required to be connected in series. In order to increase the current rating for a PV module by *n* times of the rating of a single PV cell, *n* PV cells are required to be connected in parallel. In order to increase both voltage rating and current rating by *m* and *n* times, a PV model requires *n* parallel connections of *m* series connected cell strings. The connection of a larger number of single PV cells in series may result in a higher internal series resistance and hence higher internal losses within the PV module. In contrast, connecting a larger number of single PV cells in parallel can reduce the internal resistance and hence lower internal losses within the PV module.

- Any PV cells and PV modules can be represented by the PV equivalent model which consists of four components: a DC current source, a diode and two resistors. This thesis has presented the procedure to determine and characterise these components by using the information given in the specification datasheets of PV cells. Simulation results show that the model obtained from the proposed procedure can provide similar results to ones given in the datasheets. In this thesis, the PV equivalent model was used for simulation work and the design of an analogue control circuit for a PV emulator in experimental work.

A summary of typical characteristics for an ideal grid-tied PV inverter are as follows:

- Based on the characteristics of the PV cells, the inverter should be able to:
    - operate in a whole PV voltage range for full power extraction
    - operate at the maximum voltage-current-power ratings of the PV cells for connection compatibility
    - always operate at the MPP for maximum power extraction
- Based on the grid side characteristics, the inverter should comply with relevant grid codes and standards. Grid codes are the technical specifications issued by an authority for connection to the electricity grid (e.g. E.On-Netz). Standards are the technical specifications recommended by independent global organizations (e.g. IEEE-1547 and IEC-61727). The inverter should be able to:
    - emit voltage and current harmonics lower than the specifications of the grid codes and standards (e.g. IEEE-1547)
    - produce output power factor greater than 0.9 when the PV cells generate an output power greater than 50% of their ratings (IEC-61727)
    - have the capability to ride-through grid faults, which is the ability to remain stable and stay connected to the grid during grid fault

disturbances, support the grid with a reactive current and supply power to the grid immediately after the fault clearance (E.On-Netz 2006)

- The inverter should have high efficiency, small size, light weight and low cost. This thesis has utilised an efficiency evaluation method called the *European Efficiency*. The method averages the maximum efficiencies of the inverter at different sun irradiance levels based on the sun energy profile of the central Europe.

Reviews of the six available topologies for the transformerless inverters have been undertaken. Details of their circuit configurations, modulation and control methodologies, and component designs have been presented. A summary of the reviews are as follows:

- The VSI and the CSI are the simplest topologies of the transformerless inverters in the literature. The VSI cannot operate in a whole PV voltage range since the VSI requires a PV voltage higher than the peak grid voltage in order to allow controllable power to flow from the PV cells into the grid. As a result, increased voltage ratings for the PV cells are required. In contrast, the CSI can operate in a whole PV voltage range by its nature but with a PV voltage lower than 0.866 (or $\sqrt{3}/2$) of the peak grid voltage. However, the CSI has low efficient operation at low PV voltage caused by a large difference of the voltage levels between the PV side and the grid side.

- The VSI+Boost uses a Boost converter to "step up" low PV voltages to the sufficient level for the VSI. Therefore, extra-high voltage ratings of the PV cells are no longer necessary. On the other hand, the CSI+Buck uses a Buck converter to "step down" high PV voltages to be lower than the limit level of the CSI. Therefore, PV voltage rating PV cells higher than the CSI limit can be used (if required). However, these additional converters lead to a more complicated circuit and control, higher cost, and higher power losses.

- The ZSI-V and ZSI-I are modified topologies of the VSI and CSI respectively. A unique impedance circuit (Z-circuit) is added on the DC side of their circuits. The ZSI-V operates exactly the same as the VSI and the ZSI-I as the CSI when the PV voltage is in the permitted ranges. When the PV voltage is

insufficient for the VSI, the ZSI-V will step the voltage up by operating with the "shoot-through" switching states. Similarly, when the PV voltage exceeds the limit of the CSI, the ZSI-I will step the voltage down by operating with the "open-circuit" switching states. In fact, the shoot-through and open-circuit switching states are not permitted for the VSI and the CSI but can be utilised for the ZSI-V and the ZSI-I due to the use of a Z-circuit. Implementation of these switching states in a modulation strategy has been also detailed in this thesis.

This thesis has proposed an alternative topology to the CSI, which is the CSI with series AC capacitors (CSI+SCaps). This topology utilises the advantage of the CSI and the improved efficiency during low PV voltage which results from the use of the series AC capacitors. Details of the topology presented are circuit configuration, analytical model and equations, series AC capacitor dimension calculations, operation principles, modulation and control strategies, and potential applications. A summary of details are as follows:

- The CSI+SCaps has the same circuit configuration as the standard CSI except the series AC capacitors are added into the AC circuit.

- An analytical model of the CSI+SCaps based on the phasor diagram and the analytical equations have been derived by using the vector summation theorem. The analytical model is used to explain the operation of the CSI+SCaps in different situations whilst the analytical equations are used to derive the dimensions of the series AC capacitors and the control methodologies.

- The size of the series AC capacitors is dependent on five parameters: grid voltage, grid frequency, output power factor, AC voltage of the inverter and DC-link current. A smaller capacitor is required for a higher grid voltage level and a higher grid frequency. A larger capacitor is required for a higher DC-link current. The largest size capacitor is required for the point at which the output power factor is equal to the ratio of the AC voltage amplitude of the inverter to the grid voltage amplitude ($cos\theta=a$).

- Modulation techniques used for the standard CSI can be directly used for the CSI+SCaps. However, control techniques used for the standard CSI with Unity Power Factor (UPF) control can result in a high AC voltage "seen" at the AC output of the inverter when using with the CSI+SCaps. Two alternative methods proposed in this thesis would be more preferable instead: Minimum Switching Voltage (MSV) control and Optimum Power Factor (OPF) control. The MSV control always operates with the maximum operating modulation depth and always provides minimum switching voltage. However, the MSV control provides low output power factor. The OPF control always operates with the maximum power factor whilst providing low switching voltage at the same time. However, the OPF control cannot be used during the low grid fault ride-through where a large reactive current is required.

- The CSI+SCaps could be useful for low switching voltage applications. In this thesis, an example is shown where the converter is used to reduce the voltage rating of a shunt active power filter. Since the added series capacitor forms a better high harmonics attenuation capability with the conventional LC filter of the standard CSI circuit, the CSI+SCaps topology can achieve providing better AC output quality than the standard CSI. Therefore, the CSI+SCaps would be useful for the applications which require further high harmonic reduction. The CSI+SCaps could also be useful for the CSI applications requiring a smaller size of the DC filter (DC-link inductor). This is because the CSI+SCaps can be controlled to operate with the maximum modulation depth where a shorter time (or no time) for the zero DC voltage caused by the short-circuit operation of the CSI PWM null states is needed to be filtered.

The performance of the CSI with series capacitors has been evaluated and compared with all of the six considered topologies. All the topologies are modelled and tested in the SABER simulation program. The obtained simulation results are used for the performance evaluation. A summary of the evaluations and comparisons are as follows:

- The CSI+SCaps requires the same PV ratings as the standard CSI. The topology requires the lowest PV voltage rating but the highest PV current rating among all the candidate topologies. Since lower PV voltage rating and

high PV current rating requires a lower internal resistance within the PV module, the PV modules for the CSI+SCaps and the standard CSI have the lowest internal power losses.

- The CSI+SCaps can operate with the highest modulation depth ($m \approx 1$) over the whole PV voltage range among all the candidate topologies. A higher level of modulation depth designates a higher power transfer ratio and a more optimum voltage-current level between the input and output of the inverter.

- The CSI+SCaps requires the minimum number of active components used (as does a standard CSI). As a result, the topology has a less complex control methodology and a lower power consumption by the control circuit compared to the other topologies.

- The CSI+SCaps is a medium-size inverter (ordered in the 4^{th} rank) among all of the seven candidate topologies based on the criteria of the required size of total passive components.

- The CSI+SCaps provides high input PV voltage ripple (ordered in the 5^{th} rank) but medium PV current ripple (ordered in the 4^{th} rank) among all of the seven candidate topologies. However, the CSI+SCaps provides approximately 20% lower input voltage and current ripple compared to the standard CSI. High input PV voltage and current ripple can degrade the accuracy for the MPP tracking system, generate heat and lead to low efficiency and shorten the lifetime of the electronic components and PV cells.

- The CSI+SCaps can achieve the lowest peak DC-link voltage and hence the lowest voltage stresses on power semiconductors among all the candidate topologies.

- The CSI+SCaps provides the best quality of output AC line current (the lowest THD) among all the candidate topologies. This is caused by the improved high harmonics attenuation filters formed by the series AC capacitors and conventional LC filters in the AC side of the CSI+SCaps circuit. However, the presence of the series AC capacitors in this inverter topology makes the

impossible approach for independent power factor control; therefore, the topology would have low power factor compared to all of the other topologies.

- The CSI+SCaps can achieve the lowest estimated cost of power semiconductors among all the candidate topologies based on the criteria of specific power installed in the power semiconductors.

- The CSI+SCaps can achieve low semiconductor power losses ordered in the 2nd rank when compared to all of the seven candidate topologies. The CSI+SCaps also has lower semiconductor power losses than the standard CSI (approximately 7.3% lower). The standard VSI can achieve the lowest power losses.

- The CSI+SCaps can achieve high efficiency with European efficiency of 97.6% ordered in the 3rd rank of all seven candidate topologies and higher efficiency compared to the standard CSI (96.7%) based on the consideration of semiconductor power losses solely.

- An overall performance evaluation shows that the CSI+SCaps can achieve the best performance among all the seven candidate topologies when all the considered evaluation criteria are weighed equally; following by the CSI+Buck, standard CSI, ZSI-I, standard VSI, VSI+Boost and ZSI-V.

An experimental test-rig was designed and constructed in order to experimentally validate the feasibility and the performance of the CSI+SCaps in comparison to the standard CSI. The test-rig consists of four main elements: a PV emulator, a CSI+SCaps prototype, interfacing and control circuits and a three-phase power supply. The PV emulator is designed to be used as a PV source generating the peak output PV power of 1.6kW for the converter. The CSI+SCaps prototype is designed to operate with both the CSI+SCaps and the standard CSI in order to produce comparable results between them. The interfacing and control circuits contain the elements required for voltage and current measurements, gate drives, signal processing and program control. The three-phase power supply is used to facilitate the connection to the electrical network.

The experimental results have been taken from the experimental test-rig. There are two sets of the results presented. The first set of the results is used to verify the functionality of the experimental test-rig and the second set of the results is used to experimentally evaluate the performance of the CSI+SCaps in comparison to the standard CSI and to validate the simulation results. A summary of the results are as follows:

- The experimental results show that all the elements of the experimental test-rig operate as expected. A PV emulator can provide similar PV characteristics as the designed specifications. The CSI+SCaps prototype incorporating with the interface and control circuits can produce similar operating waveforms to the simulation results. The prototype can provide safe operation during start-up and shutdown.

- The experimental results support the simulation results in all of the evaluation aspects. A summary of the results are as follows:

    - The CSI+SCaps provides lower input PV current ripple (3.2-4.1$A_{pk\text{-}pk}$) compared to the standard CSI (5.4-6.2$A_{pk\text{-}pk}$).

    - The CSI+SCaps provides lower peak DC-link voltage (381-419V_{pk}) compared to the standard CSI (456-463V_{pk}).

    - The CSI+SCaps provide lower peak DC-link current (4.2-5.2A_{pk}) compared to the standard CSI (5.2-6.9A_{pk}).

    - The CSI+SCaps provides better output line current waveforms with a lower value of THD (13.5-7.8%) compared to the standard CSI (15.6-18.5%).

    - However, The CSI+SCaps provides lower power factor (0.78-0.84) compared to the standard CSI (0.86-0.98).

    - The CSI+SCaps can achieve higher European efficiency (87.8%) compared to the standard (79.9%), which is a 7.9% improvement.

- The experimental results when the CSI+SCaps and the standard CSI operate at the grid voltage dips by 30% and 70% from the nominal voltage level show

that both the CSI+SCaps and the standard CSI can operate properly during the faults. However, the dynamic results show that with the same MPP tracking method the CSI+SCaps provide a more efficient operation than the standard CSI. The CSI+SCaps can stabilise its operation and "find" the new MPP more quickly than the standard CSI. The topology can also inject full active power into the grid immediately after the fault clearance whilst the standard CSI requires a delay time.

This thesis has discovered that by adding series AC capacitors into the standard CSI topology, input voltage and current ripple of PV cells can be reduced and thus a smaller DC filter than the standard CSI is required. The inverter can operate with higher operating modulation depth along the whole PV voltage range that consequently reduces voltage and current stresses on semiconductor devices. The inverter can provide better output waveforms with an improved efficiency (7.9%). The CSI+SCaps provides a more efficient way to ride-through low voltages caused by grid faults with fully supporting reactive current. The topology is also able to immediately inject full active power after the fault clearance.

9.1 Summary of Achievements

The achievements of this thesis are summarised as follows:

- A literature review of basic knowledge of the PV cells and typical characteristics for an ideal grid-tied PV inverter have been made.
- A review of six available transformerless, grid-tied PV inverter topologies has been also made.
- An alternative topology to the CSI with the use of series AC capacitors for a grid-tied PV interface and other possible applications has been proposed. Two novel control methods in order to achieve minimum switching voltage and maximum power factor have been also proposed.
- Simulation circuits for all of the six available topologies and one proposed topologies have been modelled and tested.

- An evaluation of the performance of the proposed topology in comparison with the six other transformerless topologies by using the simulation results has been carried out. The evaluation results show several advantages of the proposed topology.

- An experimental test-rig which was used to validate the feasibility of the proposed topology and to experimentally evaluate the performance of the proposed topology to the standard CSI was constructed and tested.

- Experimental results that show the feasibility of the proposed inverter and support the simulation results have been provided.

9.2 Future Work

The following list provides suggestions for future research work:

- The CSI+SCaps can be controlled to always operate at the maximum modulation depth. It means that the PWM null switching states may be omitted. In this case, reduced switching state or lower switching frequency modulation techniques may be used. This could provide an interesting area for future research.

- Further research on the benefit of the series AC capacitors for harmonic reduction should be considered. This would require a design of the cut-off frequency of the filters in order to achieve the maximum harmonic reduction with the optimum size of series capacitor.

- It is noted that the semiconductor power losses and the inverter efficiencies presented in this thesis were calculated and measured for a few commercial products only. The results would be different if IGBTs with different characteristics and specifications are used, especially the developing devices such as RB-IGBTs, which would have improved ratings. Therefore, the efficiency of the inverter based on a variety of different IGBT types should be considered.

- Since only the experimental results of the CSI+SCaps and the standard CSI have been presented in this thesis, in future work the experimental results of all the other candidate topologies should be taken into consideration for validation.

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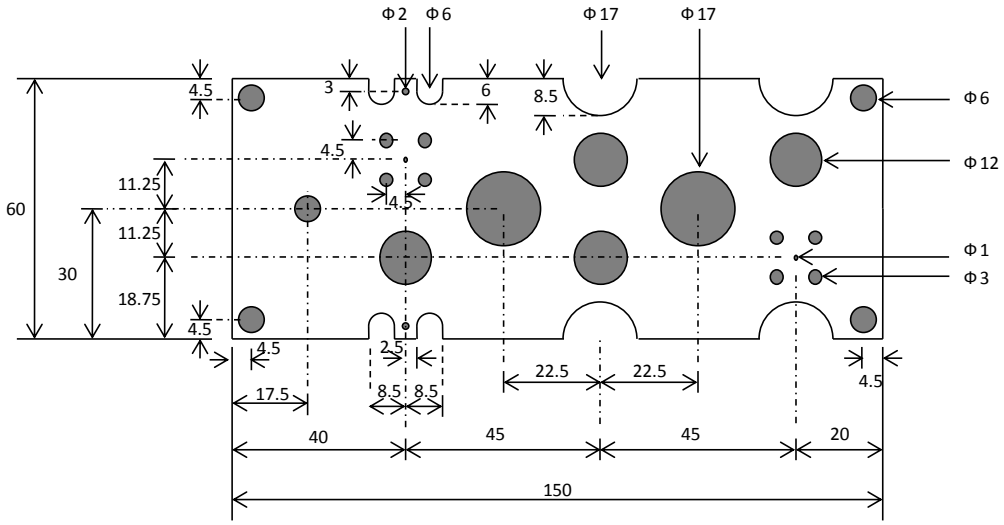
Appendices

Appendix A MPPT Techniques

MPPT technique	Symbol	PV array Dependent?	True MPPT?	Analogue or Digital?	Periodic Tuning?	Convergence Speed	Implementation Complexity	Sensed Parameters
Perturb & Observe	P&O	No	Yes	Both	No	varies	Low	V, I
Incremental Conductance	IncCond	No	Yes	Digital	No	varies	Medium	V, I
Fractional Voc	FOV	Yes	No	Both	Yes	Medium	Low	V
Fractional Isc	FSI	Yes	No	Both	Yes	Medium	Medium	I
Fuzzy Logic Control	FLC	Yes	Yes	Digital	Yes	Fast	High	varies
Neural Network	NN	Yes	Yes	Digital	Yes	Fast	High	varies
Ripple Collection Control	RCC	No	Yes	Analogue	No	Fast	Low	V, I
Current Sweep	CS	Yes	Yes	Digital	Yes	Slow	High	V, I
DC-link Capacitor Drop Control	CDC	No	No	Both	No	Medium	Low	V
Load I or V Maximization	LM	No	No	Analogue	No	Fast	Low	V, I
dP/dV or dP/dI feedback Control	FBC	No	Yes	Digital	No	Fast	Medium	V, I
Array Reconfiguration	AR	Yes	No	Digital	Yes	Slow	High	V, I
Linear Current Control	LCC	Yes	No	Digital	Yes	Fast	Medium	Irradiance
I_{mmp} & V_{mmp} Computation	CP	Yes	Yes	Digital	Yes	N/A	Medium	Irradiance, Temperature
State-based MPPT	SB	Yes	Yes	Both	Yes	Fast	High	V, I
One-cycle control	OC	Yes	No	Both	Yes	Fast	Medium	I
Best Fixed Voltage	BFV	Yes	No	Both	Yes	N/A	Very Low	None
Linear Reoriented Coordinates	LRC	Yes	No	Digital	No	N/A	High	V, I
Slide Control	SC	No	Yes	Digital	No	Fast	Medium	V, I
Temperature Gradient	TG	Yes	Yes	Digital	Yes	N/A	Medium	V, Temperature
Temperature Parametric	TP	Yes	Yes	Digital	Yes	N/A	Medium	V, irradiance Temperature

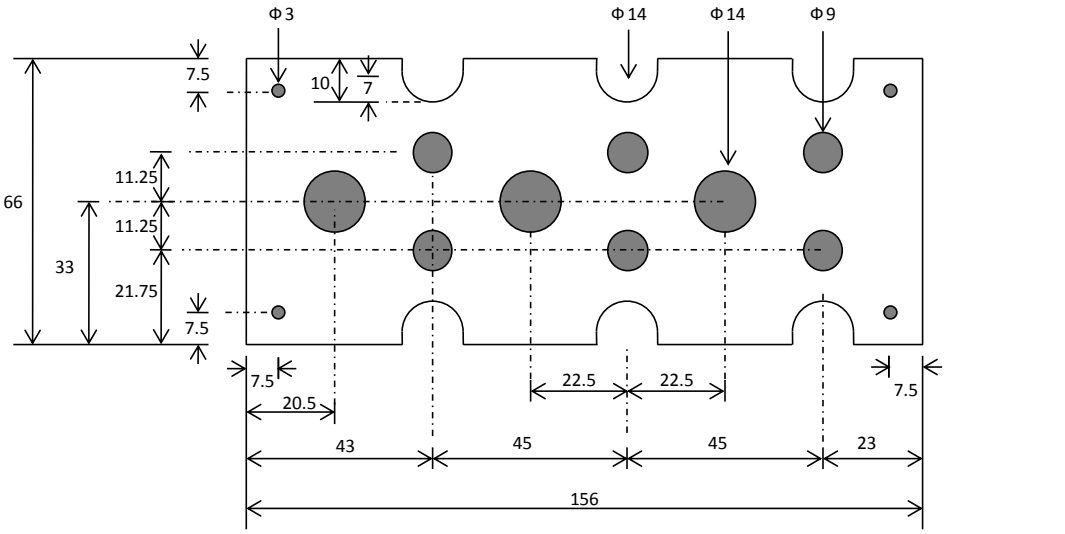
Table A.1 MPPT techniques and their characteristics [67]

Appendix B Drawings of Three-Phase Power Bus Bars



(*Unit in mm*)
:thickness 2mm

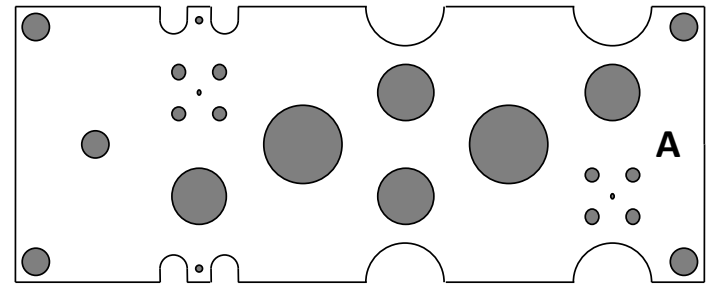
(a) Planar Bus Bars



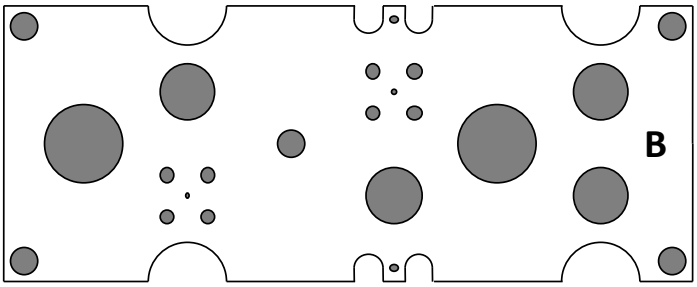
(*Unit in mm*)
:thickness 0.25mm

(b) Dielectric Sheets

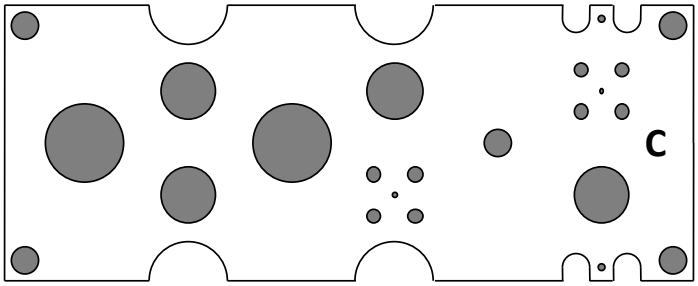
Figure B.1 Dimensions of (a) the planar bus bars and (b) the dielectric sheets



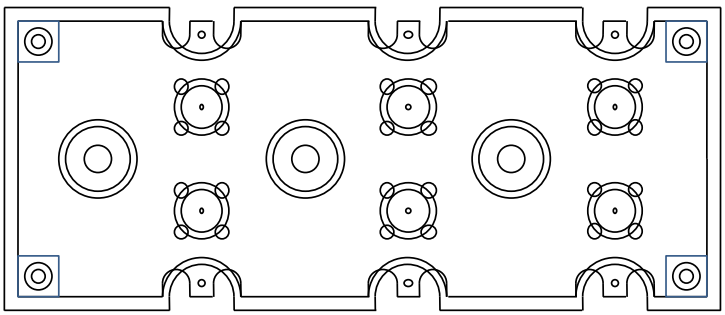
(a) Phase A



(b) Phase B



(c) Phase C



(d) Completed Module

Figure B.2 Sketches of power bus bar for phase A, B, C as shown by (a),(b),(c) and (d) the complete bus bar module